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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

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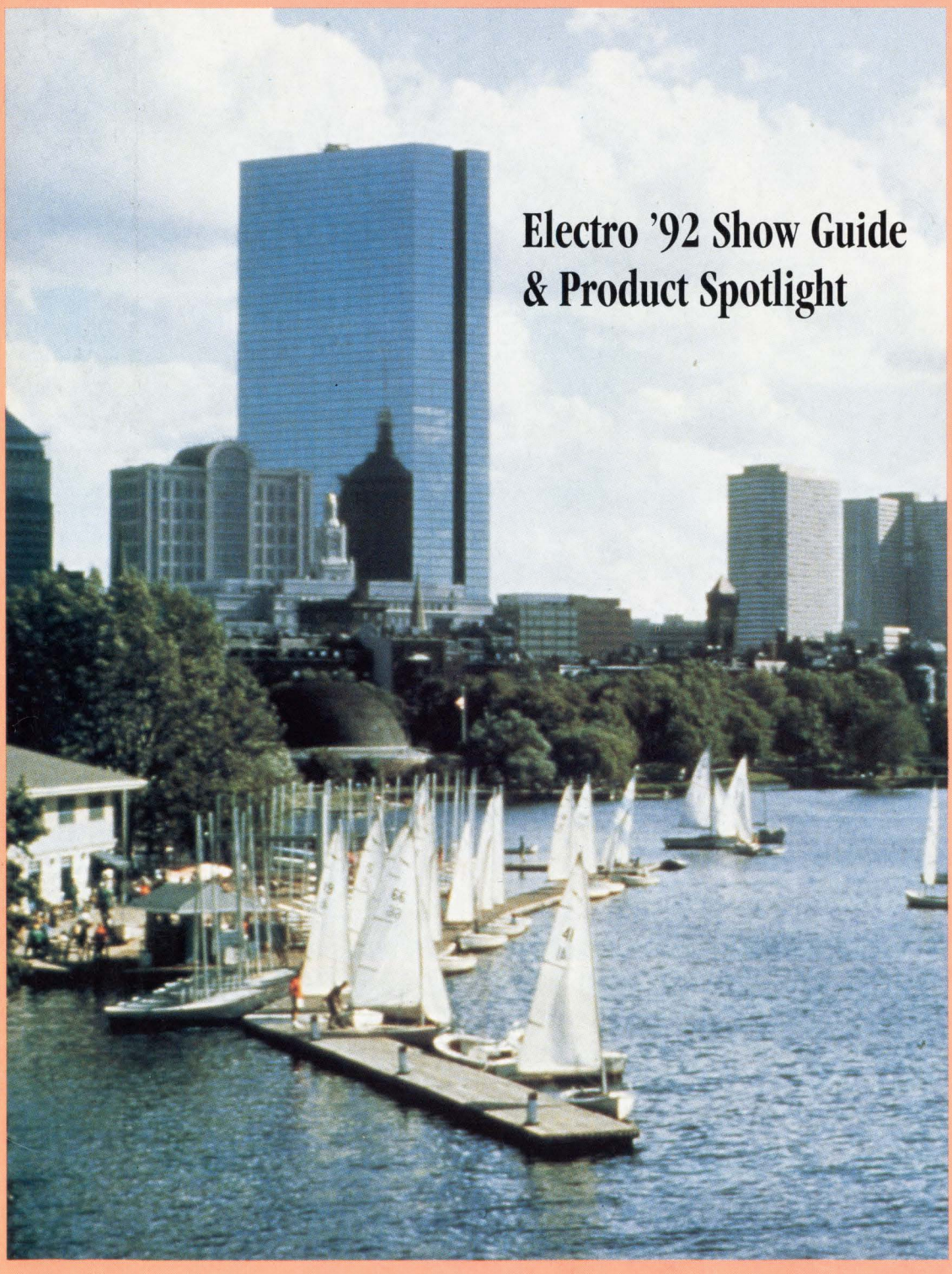
A CAHNERS PUBLICATION

May 7, 1992



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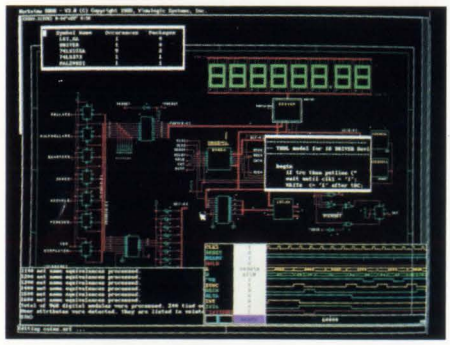

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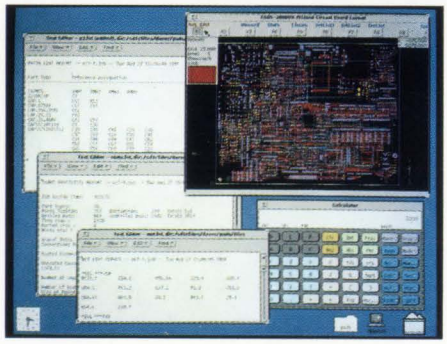

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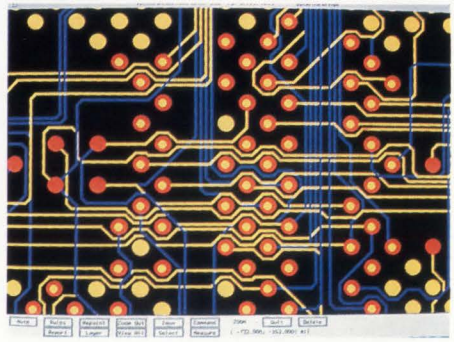

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MAGAZINE EDITION

MAY 7, 1992 VOLUME 37, NUMBER 10B

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SHOW DIRECTORY

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PRODUCT & PROCESSOR UPDATES

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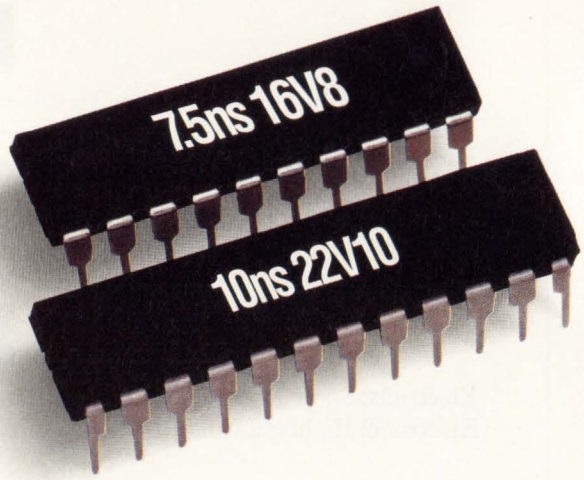

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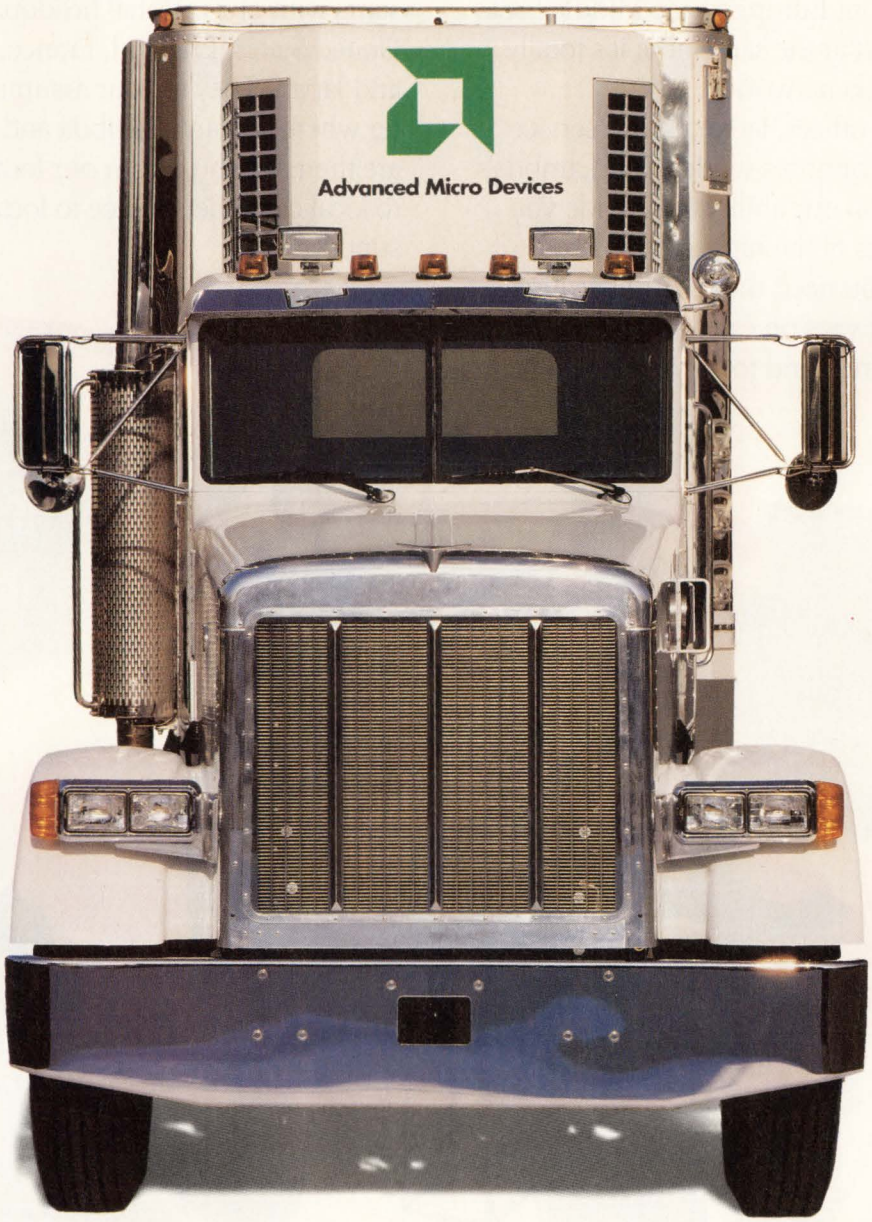

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CIRCLE NO. 12

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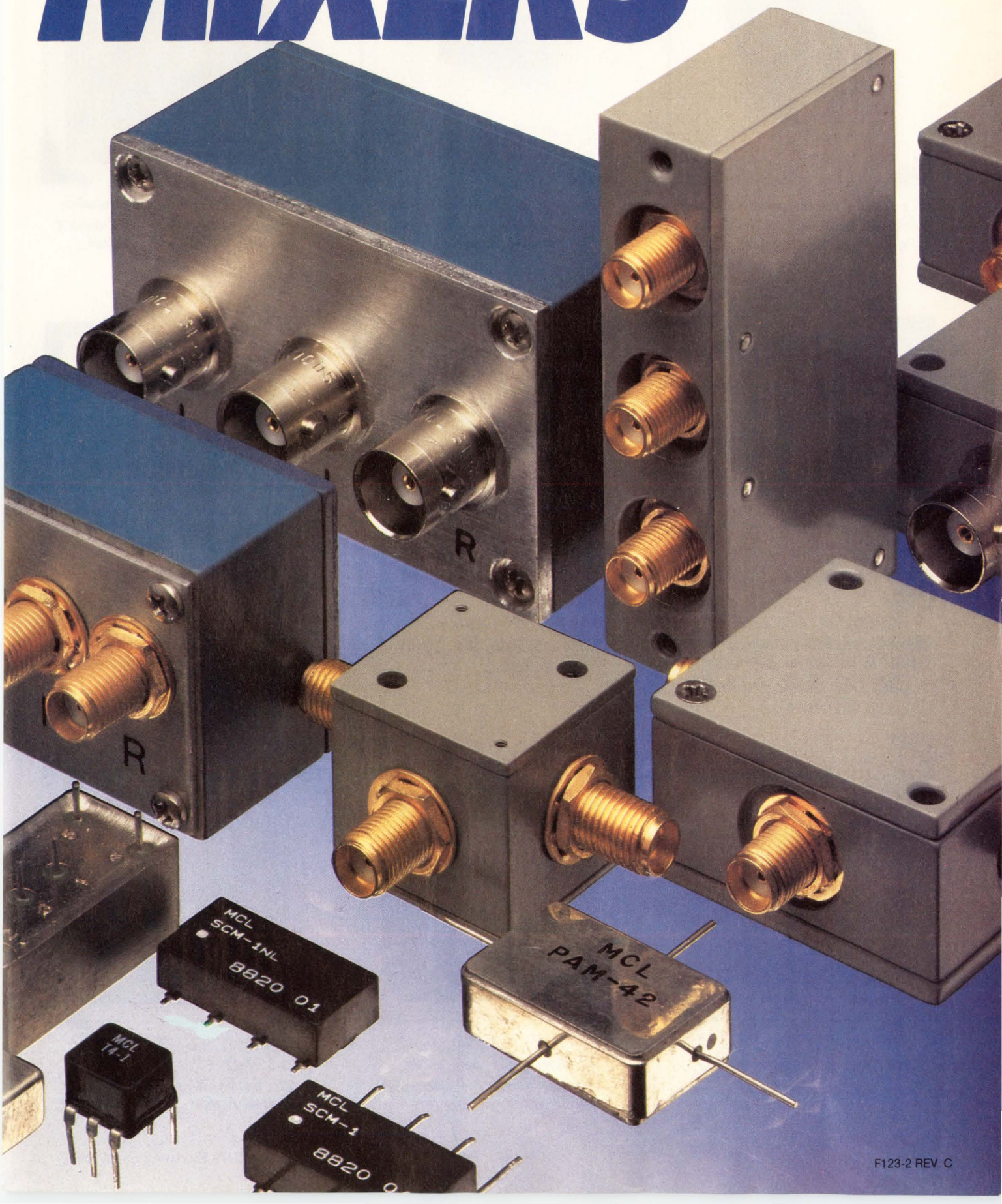
MIXERS



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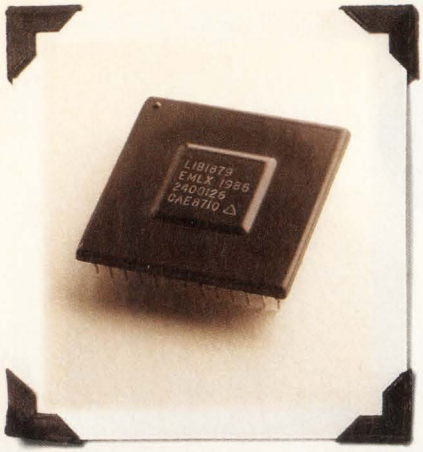
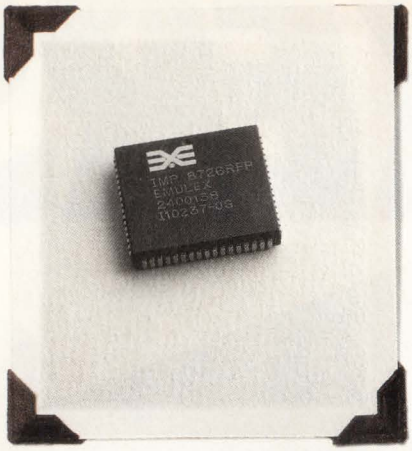


1986-MAC100. We introduce a combined disk formatter and buffer controller in a single disk controller chip.

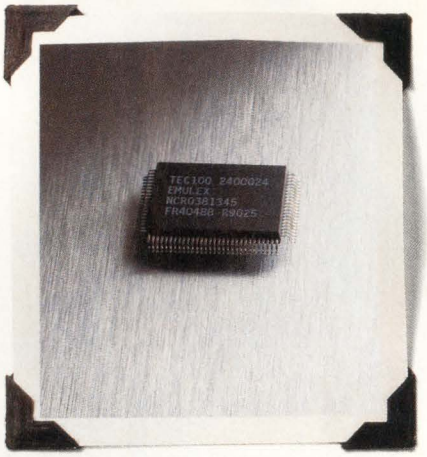


1987-ESP100. The industry's first high-performance SCSI chip is born at Emulex.

1988-ESP200. Second-generation SCSI arrives with SCSI-2 support and parity pass-through.

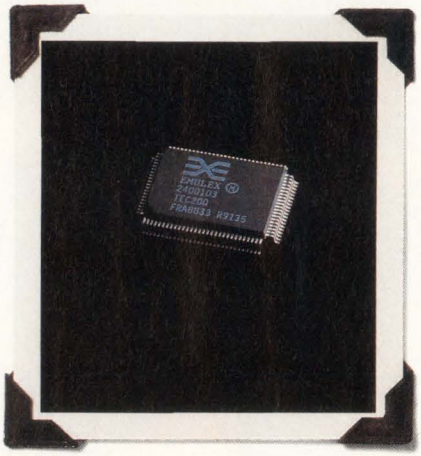
1988-MAC200. Our advanced merged architecture controller is the first to include an automated Data Flow feature for faster data handling.

1989-BC200. A dynamic 4-Port DMA controller for DRAMs is created.



1989-TEC100. EMD combines disk, buffer, and SCSI controllers in a single chip.

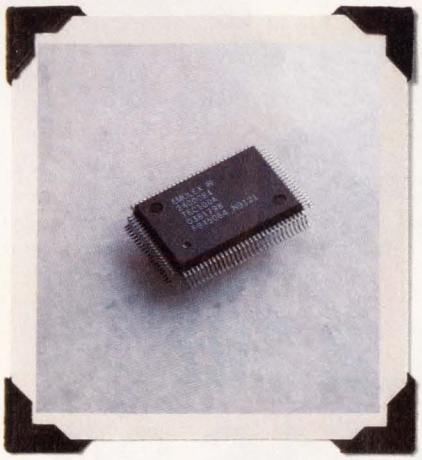
1990-FAS236. We deliver the first Fast SCSI chips with a 16-bit DMA port.



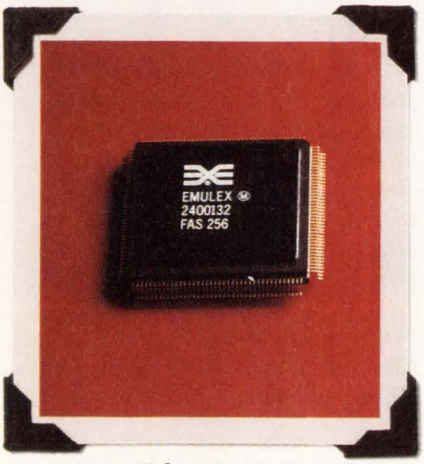
1991-TEC200. Our second-generation TEC becomes the industry's first Fast single-chip disk controller.

1991-TEC256. The first Fast and Wide SCSI disk controller also boasts the fastest disk data rate and highest system bandwidth.

1988: ESP2X6. We give SCSI a 16-bit split-bus architecture for greater efficiency and throughput.



1990: TEC 100A. Mid-to-low capacity SCSI drives get a reduced-price version of the TEC100.



1991- FAS256. 16-Bit Fast and Wide SCSI brings SCSI-2 support to host adapters and peripherals including drive array applications.

WE CREATED A FAMILY OF FIRSTS. WE'RE NOT DONE YET.

In all honesty, we've been building a history of innovative microcontroller products for disk and system applications right from the start.

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And now we're preparing to launch a new generation of products—a whole new family of microcontrollers...to again pioneer new industry standards in SCSI and other bus interfaces.

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Firsts are part of our tradition. And we're not done yet.

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CIRCLE NO. 14

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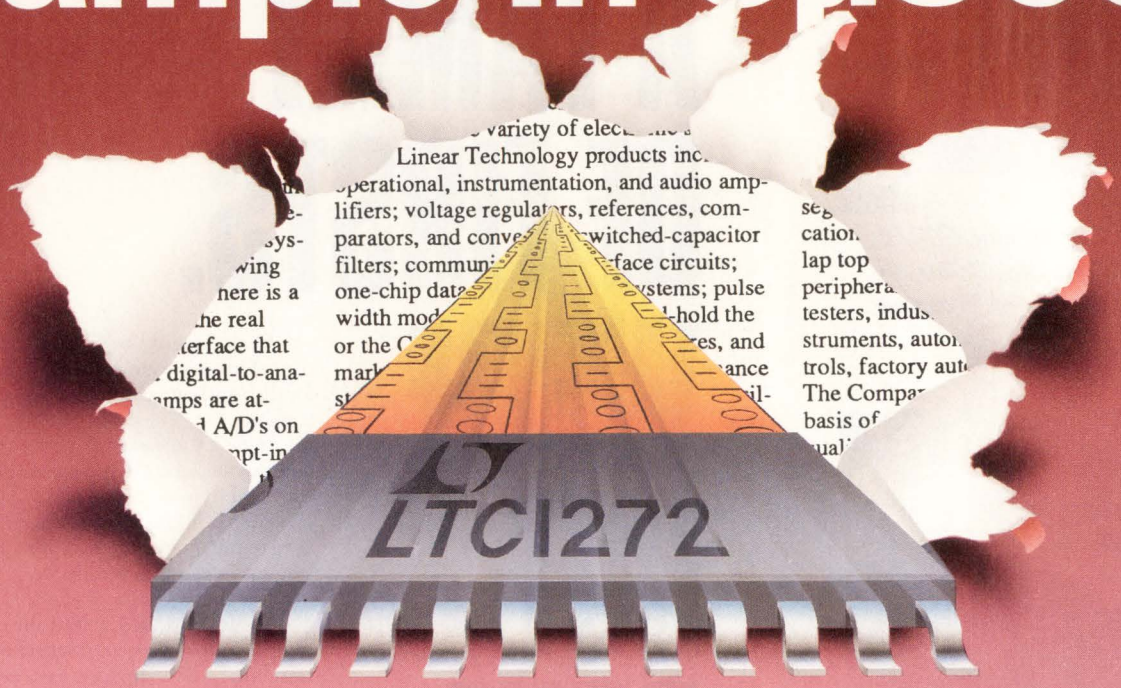

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Linear Technology delivers 12 bit samples faster and cheaper using less power and less board space.

The new LTC1272 is a 3μsec, 12 bit sampling ADC that blows the doors off non-sampling 7572 and 574 type parts and their sampling upgrades. In the 7572 pinout, it samples at 250kHz and typically draws only 75mW from a single 5V supply.

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	LTC1272	AD7572	AD574	AD1674	MAX162
INTERNAL REFERENCE	✓	✓	✓	✓	✓
7572 PINOUT	✓	✓			✓
3μsec CONVERSION TIME	✓				✓
S & H INCLUDED	✓			✓	
LOW POWER CONSUMPTION	✓				
250 kHz SAMPLE RATE	✓				
SINGLE 5V SUPPLY OPERATION	✓				

With on-board voltage reference, the LTC1272 is a complete, sampling ADC solution. Get it now in your choice of 3, 5, and 8μsec speeds for military and commercial temperature grade applications. Packaging is plastic DIP, SO and hermetic. For details contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call **800-637-5545.**.

LINEAR TECHNOLOGY

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FOR TOUGH APPLICATIONS.

CIRCLE NO. 15

Electro® International

Electronics Conference and Exhibition
May 12-14, 1992 / Boston, Massachusetts

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Boston, MA 02115

Tuesday, May 12, 9:00AM -- 5:00PM
Wednesday, May 13, 9:00AM -- 5:00PM
Thursday, May 14 9:00AM -- 4:00PM

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Cherry Electrical Products	3404 3406 3408 3503 3505 3507
Circuit Assembly Corporation	1311
Claflin Associates	2018
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Coiltronics International Corp.	4529
Communication Cable Inc.	5526
Compunetics, Inc.	1012
Computer Design Magazine	1024 1026
Concord Electronics Corporation	2217 2219
Contact East, Inc.	2312 2314
Contex/Moldcon	1530
Conxall Corporation	1335
Cornell Dubilier Electronics, Inc.	3508
Cosmo Corporation	4206
Croft Corporation	3220
CTS Microelectronics	1318
CUI/Stack, Inc.	4609
Current, Inc.	3204
Curtis Industries Inc.	4633
Custom Connector Corporation	4208

D

Daburn Electronics & Cable Corp.	4219
Data Check Corporation	2402
Data Delay Devices	4004
Data I/O Corporation	1210 1212
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Dempa Publications	5020
Design Mark Industries	4627 4629
Dexter Magnetic Materials Division	4230
Digital Equipment Corporation	2305
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DMA Marketing	4314 4407
Dsp Development	1136
Du Pont Company	4234 4236 4333 4335

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Hartwell Corporation, The	3304
Harwin Inc.	3524
Hasco Components International Corp.	5208
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Irish Trade Board	1336
Iten Industries	4026
ITT Schadow Inc.	4408
ITW Switches	1228 1230

I

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IEEE	1116 1120 1215 1217 1219

J

J.S.T Corporation	2222 2224

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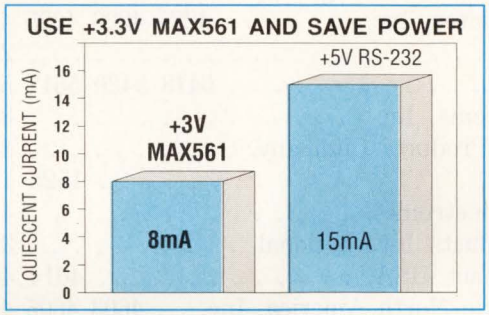
+3V POWERED RS-232 IS HERE!

Eliminate +5V RS-232, Use 1/2 the Power and Meet the New EIA/TIA-562 Requirements

- **Guaranteed Operation Down to 3.0V**
- **4 Drivers, 5 Receivers**
- **Meets New EIA/TIA-562 Standards**
- **1μF External Capacitors**
- **Guaranteed RS-232 Compatibility***
- **1μA Shutdown Mode**

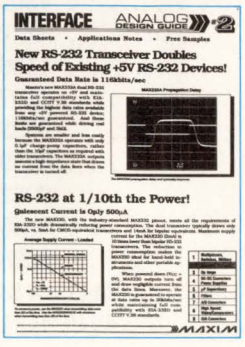


The +3.3V powered MAX561 uses 1/2 the power of +5V RS-232 devices.

Maxim's new MAX561 is the first device to implement the new EIA/TIA-562 standard that guarantees operation with output voltages as low as ±3.7V. The MAX561 consumes **1/2 the power** of +5V RS-232 and operates from a 3.3V power supply. And, as stated in its forward, EIA/TIA-562 *"allows for electrical interoperation with equipment designed to conform to EIA/TIA-232D interfaces."*

Choose a +3.3V Transceiver and Save Power

	+3V MAX561	+5V RS-232
Quiescent Current	**8mA**	15mA
Data Rate	20kbits/sec	20kbits/sec
Output Driver Voltage, Min	**±3.7V**	±5V
Receiver Input Voltage, Min	±3V	±3V
Receiver Input Voltage, Max	±30V	±30V
T_X Load Impedance	3kΩ to 7kΩ	3kΩ to 7kΩ
R_X Input Resistance	3kΩ to 7kΩ	3kΩ to 7kΩ
Instantaneous Slew Rate	<30V/μs	<30V/μs



FREE Interface Design Guide

Includes: Application Notes ♦ Data Sheets ♦ Cards For Free Samples

To receive your free design guide, simply circle the reader response number, or contact Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.

MAXIM

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* As stated in the EIA/TIA-562 specification.

ELECTRO/92 EXHIBITOR LIST

STEP-UP DC-DC REGULATORS DELIVER 90% EFFICIENCY!

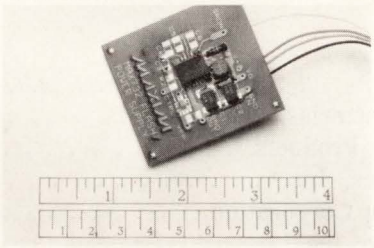
Compact Solutions for +5V, +12V, +15V or Adjustable Outputs

Use the new MAX731, MAX732, MAX733, and MAX752 step-up regulators to build complete 85% to 95% efficient power supplies that fit into less than 0.65in^2 of board space. Low input voltages (2.5V) and miniature external components make these compact regulators ideal for portable and board-level DC-DC conversion in 3V, 5V, or battery-powered systems. High-frequency 170kHz pulse-width modulation (PWM) current-mode control provides excellent transient response and minimum ripple.

- **Evaluation Kits – SOIC and DIP**
- **Guaranteed Output Current:**
  200mA @ 5V (MAX731, V_{IN} > 2.7V)
  150mA @ 12V (MAX732, V_{IN} > 4.5V)
  100mA @ 15V (MAX733, V_{IN} > 4.5V)
- **Regulates From Low Input Voltage:**
  2.5V & Up (MAX731/MAX752)
  4.0V & Up (MAX732/MAX733)
- **Logic-Controlled 6µA Shutdown**
- **8-Pin DIP & 16-Pin SOIC**

Part	Input Voltage Range	Output Voltage	Output Current	Power Eff. Range	Price† (1000-up)
MAX731	2.5V to 4.65V	+5V	200mA	85%-90%	$3.20
MAX732	4V to 9.3V	+12V	200mA	85%-95%	$2.60
MAX733	4V to 11V	+15V	125mA	85%-95%	$2.60
MAX752	2.5V to 15V	Adjustable 2.7V to 15.75V	200mA	85%-95%	$3.20

EVALUATION KITS GIVE IMMEDIATE RESULTS

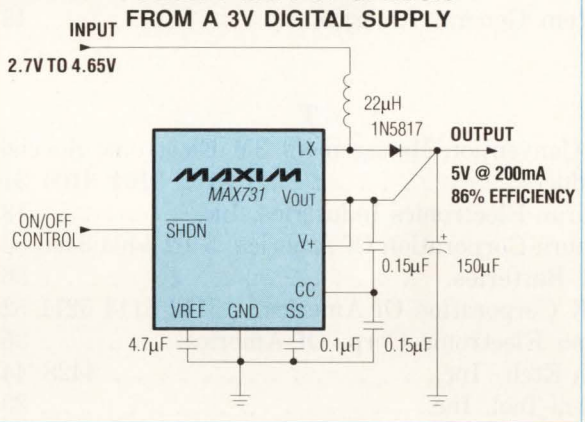


MAX732 Surface-Mounted EV Kit

Each complete surface-mount or through-hole kit contains a PC board and all external components, including inductor. $20.00 each.†

MAX731EVKIT – DIP
MAX732EVKIT – DIP
MAX733EVKIT – DIP
MAX752EVKIT – DIP
MAX732EVKIT – SO*

POWER 1 WATT OF 5V-LOGIC FROM A 3V DIGITAL SUPPLY



The MAX731 surface-mount circuit fits in 0.65in^2 (4.2cm^2) and has 86% efficiency while delivering 200mA at 5V from a 3V source.


POWER SUPPLIES ANALOG DESIGN GUIDE

Data Sheets • Applications Notes • Free Samples

+5V To ±15V DC-DC Converter Delivers 30W

No Design Required—Just Drop It In

Evaluation Kit Simplifies Prototyping

Production Kit Eases Procurement and Increases Reliability

MAXIM

FREE Power Supply Design Guide

Includes: Application Notes ♦ Data Sheets ♦ Cards For Free Samples

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*Flash Memory Programming Supply. †FOB USA recommended resale.

ELECTRO/92 EXHIBITOR LIST

COMPANY NAME	BOOTH NUMBERS
Schaal Associates	3322 3324 3326
Schroff, Inc.	5424 5426 5428 5523 5525 5527
Seastrom Manufacturing Company, Inc.	4126 4128
Seiko Instruments Usa Inc.	5232 5234 5236
Selco Products Company	4305
Senior Industries Inc.	5610
Serco Products	5409
Shindengen America, Inc.	4531
Simco	1423
Singatron Enterprise Co., Ltd.	2223 2225
Sir Associates	2329 2331 2333 2335
Solico/MEC	3526 3528
Spira Manufacturing Corporation	1306
Sprague Electric Company	4401 4403
Sprague-Goodman Electronics Inc.	3417
Stanford Research Systems	2012
Star-Tron Corporation	4108
Stewart Connector Systems, Inc.	1307 1309
Stone Components Sales Corp.	4623 4625
Sturdy Corporation	1403
Switching Systems International	1028
System General America	1315

T

3M Convention Management 3M Electronic Specialty Products	3102 3104 3106 3108
Tadiran Electronics Industries, Inc.	1330
Tamura Corporation Of America.	5402 5404 5406 5408
TDI Batteries	5627
TDK Corporation Of America.	5112 5114 5211 5213
Teapo Electronic Corp. Of America	3527
Tech-Etch, Inc.	4428 4430
Techni-Tool, Inc.	3318
Technical Materials Inc.	5611
Tectrol, Inc.	5505 5507
Teka Interconnection Systems	5501
Telco Intercontinental Corporaition	1516
Teledyne Kinetics	4330
Telpar, Inc.	2308
Temp-Flex Cable Inc.	1532
Tempil	2317
Tenney Engineering, Inc.	2403
The J.M. Ney Company	2310
Test & Measurement World	**2324 2326 2328 2330 2332 2423 2425 2427**
The Mac Innis Company	4412 4414
The Potomac Edison Company	3217
The Zippertubing Company	4110
Thermalloy, Inc.	5136
Tocos America	1418
Todd Products Corporation	5308 5310
Tokin America, Inc.	4306
Tom Maguire Associates, Inc.	4113
Topflight Corporation	2234 2236
Toroid Corp Of Maryland	2210
Total Power International, Inc.	1329
Trend Circuits, Inc.	1416
Tri-Mag, Inc.	5530
Tritek, Inc.	2307
Trompeter Electronics, Inc.	5304
TUV Product Service, Inc.	2319

U

U.S. Elco, Inc.	1405
U.S. Tech	5132
Ulveco, Inc.	4107
Unicable Inc.	2004
Unimax, A Division Of C&K	3420
United Chemi-Con, Inc.	1301 1303
USD Products	1531

V

Valid	1224
Varta Batteries, Inc.	4201
Vemaline Products	1541
Ventronics, Inc.	1433
Vernitron Corporation	1406 1408
Victoreen, Inc.	5207
Vimex International Corporation	1435
Virginia Plastics Company	4409
Vishay Electronic Components	4304
VME Microsystems International Corp.	5329
Volgen America, Inc.	1529
Von Roll Isola Inc.	3208

W

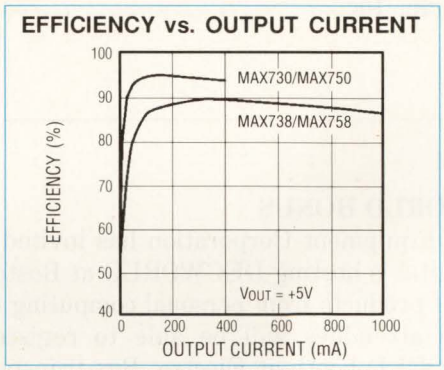
W.L. Gore And Associates	1519 1521 1523
W.W. Fischer Electronic Connectors	4010
Wago Corporation	3419 3421
Warren G-V Inc	5522
Wayland Engineering Sales Inc.	2002
Wearnes Hollingsworth Corporation	5121 5123
Weco Electrical Connectors, Inc.	4320 4322
Weigh-Tronix, Inc.	1526 1528
Welch Allyn, Inc.	5006
Westcon	2517
Westvaco - Static Control System	3112
Wieland Inc.	3512 3514
Wiko, Ltd.	4020
Wintek Corporation	1216
Wire-Pro, Inc.	4103

SMALL +5V & ADJUSTABLE DC-DCs HAVE 94% EFFICIENCY!

No Design Required for Guaranteed 300mA (1.5W) or 750mA (3.75W) Outputs

The new MAX730/MAX738 and MAX750/MAX758 step-down switching regulators are compact and simple solutions for battery-powered portable applications. They extend battery life by providing 85% to 95% efficient step-down regulation. Pre-selected components simplify design work and the standard application circuit delivers the guaranteed power over all specified line, load, and temperature conditions. High-frequency 160kHz pulse-width modulation (PWM) current-mode control provides low-noise operation and reduces output ripple to less than 50mVP-P.

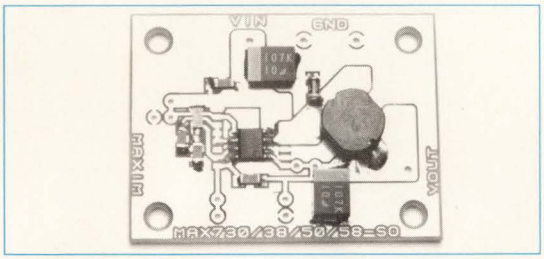
- **Evaluation Kits – SOIC and DIP***
- **Guaranteed Output Current:**
  750mA for V_{IN} > 10.2V (MAX738/MAX758)
  300mA for V_{IN} > 6.0V (MAX730/MAX750)
- **Regulates From Low Input Voltage:**
  +5.2V to +11.0V (MAX730/MAX750)
  +6.0V to +16.0V (MAX738/MAX758)
- **Logic-Controlled 6µA Shutdown**
- **Adj. Output: 1.25V to V_{IN} (MAX750/MAX758)**
  Fixed Output: +5V ± 5% (MAX730/MAX738)
- **Space-Saving Footprint:**
  8-Pin SOIC and 8-Pin DIP (MAX730/MAX750)
  16-Pin SOIC and 8-Pin DIP (MAX738/MAX758)



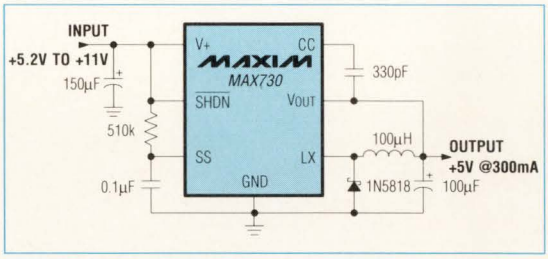
The MAX730/MAX750 and MAX738/MAX758 deliver high efficiency over a wide load range.

Evaluation Kits* Reduce Design Cycle & Provide Immediate Results

Surface-mount and through-hole kits are available for all four products, and contain a PC board and all external components, including inductor.*



The MAX730 application circuit components fit into ½ in² (3.2cm²) of board space.



The MAX730/MAX738 evaluation kit has all the components needed to build a complete +5V step-down circuit.

FREE Power Supply Products Guide

Includes: Application Notes ♦ Data Sheets ♦ Cards For Free Samples

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*Four Kits Available — MAX730/MAX738EVKIT-DIP;MAX730/MAX738EVKIT-SO; $20 each. MAX750/MAX758EVKIT-DIP;MAX750/MAX758EVKIT-SO.

ELECTRO/92 EXHIBITOR LIST

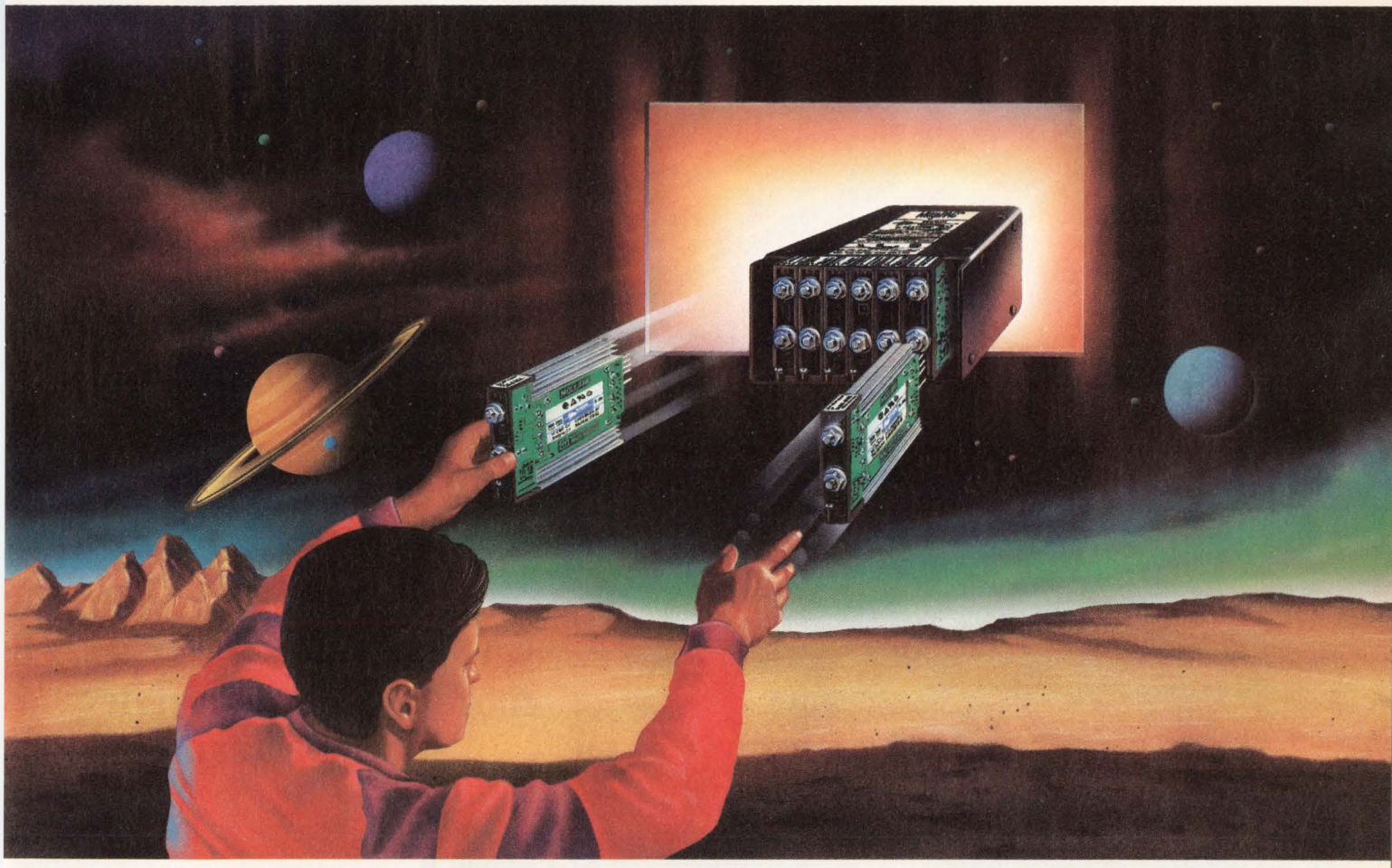
COMPANY NAME	BOOTH NUMBERS
X	
Xenotronix, Inc.	5605
Y	
Yamaichi Electronics, Inc.	5421 5423
Yellow Springs Instrument Co.	1515 1517
Yuasa-Exide, Inc.	3424 3426
Z	
Zenith Electronics Corporation.	1101 1103 1105
Zero Corporation.	4417 4418 4419 4420 4421 4422 4423 4424

DECWORLD BONUS

Digital Equipment Corporation has invited Electro/92 attendees to be special guests at DECWORLD '92. Digital is hosting DECWORLD at Boston's World Trade Center from April 27 - May 15, presenting a line of products from personal computing to supercomputing.

Electro attendees will be able to register for specially scheduled tours of DECWORLD at the DECWORLD booth at Electro. Bus transportation will be provided between the Hynes and the World Trade Center.

POWER To Configure



MegaPAC™

Power: Up to 1200 Watts
Input: 110/220 VAC, strappable; 300 VDC
Outputs: 1 to 8 isolated and fully regulated, 2 to 95 VDC
Size: 11.8"L x 6.0"W x 3.4"H

Plug into *instant power supply configurability* with the new MegaPAC switcher from our Westcor division. MegaPAC outputs can be configured in virtually an infinite number of voltage and power combinations using up to 8 slide-in **ModuPAC™** assemblies. Want to change a voltage or power level at your factory or at a customer site? No problem. . .shut down input power, slide out the ModuPAC you want to replace and slide in the new one. It's that simple.

MegaPAC's instant configurability takes Westcor's popular StakPAC to the next level of customization and flexibility. And its improved manufacturability means a substantial price reduction too! At the heart of each plug-in ModuPAC is a standard Vicor VI-26X series DC-DC converter module. . .over 1 million are operating reliably in systems world-wide. With potential applications around the globe, MegaPAC is designed to meet stringent UL, CSA, and IEC safety standards (approvals in process).

So take the risk out of specifying your system power supply. Contact us today and request ordering information. . .then sit back and relax. . . your custom-tailored MegaPAC will be delivered within four weeks.

Call VICOR EXPRESS (800) 735-6200 for information and be sure to ask for a MegaPAC data sheet. Or call WESTCOR (division of Vicor) at (408) 395-7050. Fax us at (508) 475-6715 or (408) 395-1518.

VICOR

***VICOR* Corporation**
23 Frontage Road, Andover, MA 01810

Component Solutions For Your Power System

POW

Harness the power of DIN 41612:

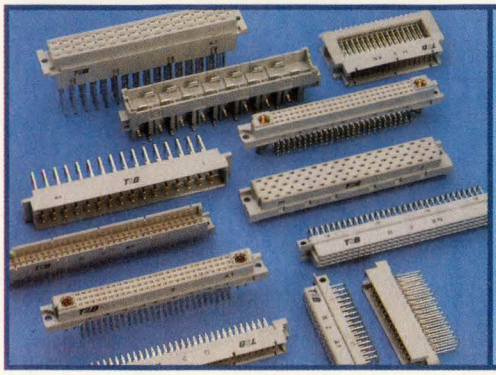
More connector types, more termination styles, more performance.

The extensive line of DIN connectors from Thomas & Betts brings you the versatility you need – with a complete range of DIN 41612 types for signal, coax, and power applications up to 40 amps per line.

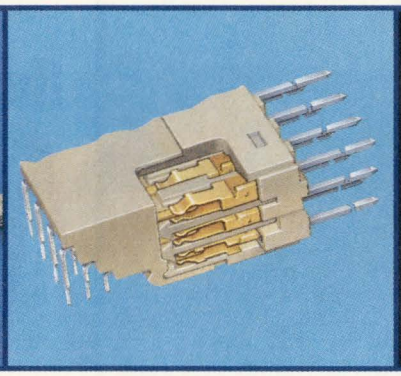
Our broad product line offers pin counts and termination options to fit almost every application – we've eliminated the need for expensive custom solutions.

• ***NORTH AMERICA*** - **Mexico:** Naucalpan, 905-393-85-10 • ***PACIFIC*** - **Australia:** Knoxfield, Victoria, 61-3-764-9589; **Hong Kong:** Kowloon, 852-739-1286; **Japan:** Tokyo, 81-3-3791-6411; **Singapore:** 65-747-0244; **Taiwan:** Hsinchu, 886-2-713-0509

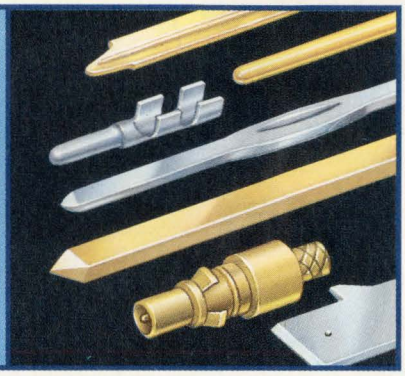
VER



A full range of DIN 41612 connector types – Standard and Inverse, Low Profile and Heavy Duty Power connectors, and Modular Coax/Signal/Power combinations.



Built-in high performance design features – pre-loaded, dual-opposing beam female contacts with coined and polished mating surfaces for maximum reliability.



A complete selection of termination styles – solder tails and posts, wire wrap, compliant pin, crimp/snap, and coax. Post lengths and plating options for every requirement.

With the high performance features designed as standard into every Thomas & Betts DIN connector, we can solve even your most difficult packaging problems.

Off-the-shelf availability through our authorized distributors means you get what you need when you need it.

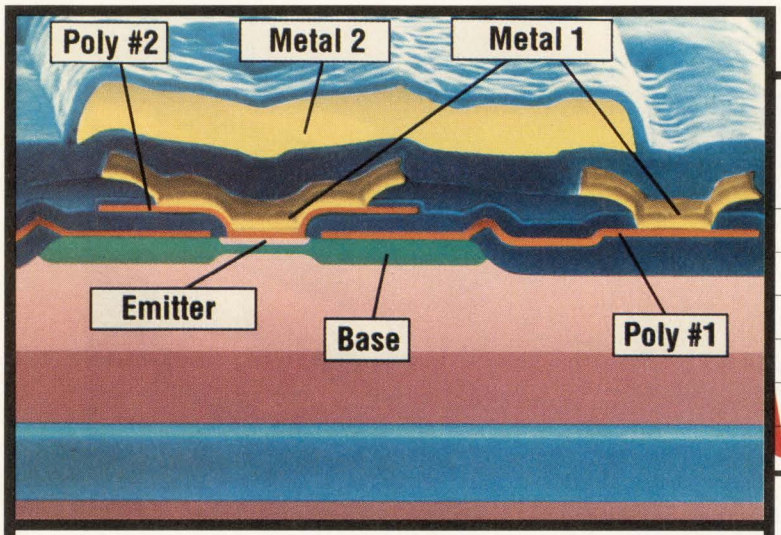
Now there's a reliable source with the breadth and depth you need to harness the full power of DIN 41612 versatility. For more information call or fax: Thomas & Betts Corporation, Electronics Division, 200 Executive Center Drive, Greenville, SC 29616. Phone: 803-676-2900. Fax: 803-676-2991.

For the new DIN Catalog call 1-800-344-4744.

Thomas&Betts

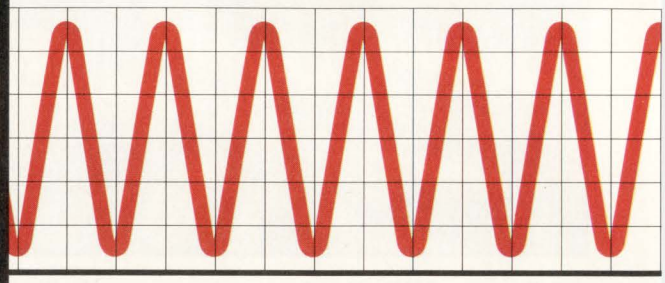
• *EUROPE* - **Belgium:** Brussels, 32-2-645-7711; **England:** Marlow, 44-6284-6055; **France:** Rungis Cedex, 33-1-4687- 2385; **Germany:** Egelsbach, 49-6103-4040; **Italy:** Milano, 39-2-6120451; **Luxembourg:** Foetz, 35-255-0002; **Spain:** Barcelona, 34-3-3002252; **Sweden:** Upplands Vasby, 46-760-88110.

HARRIS GENERATES ASTOUNDING

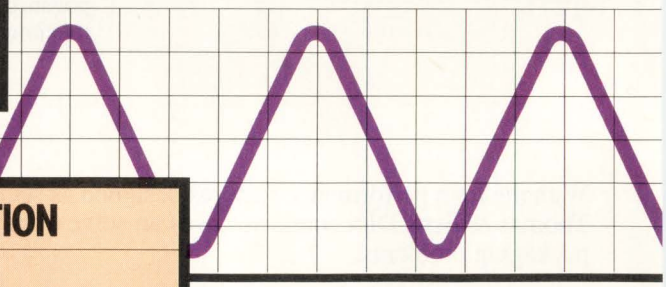


This HFA1100 family's fast performance is made possible by Harris' unique UHF-1 process. The shallow structure of UHF-1 transistors is the result of bonded wafer technology.

Harris HFA1100



Ordinary high-speed op amp

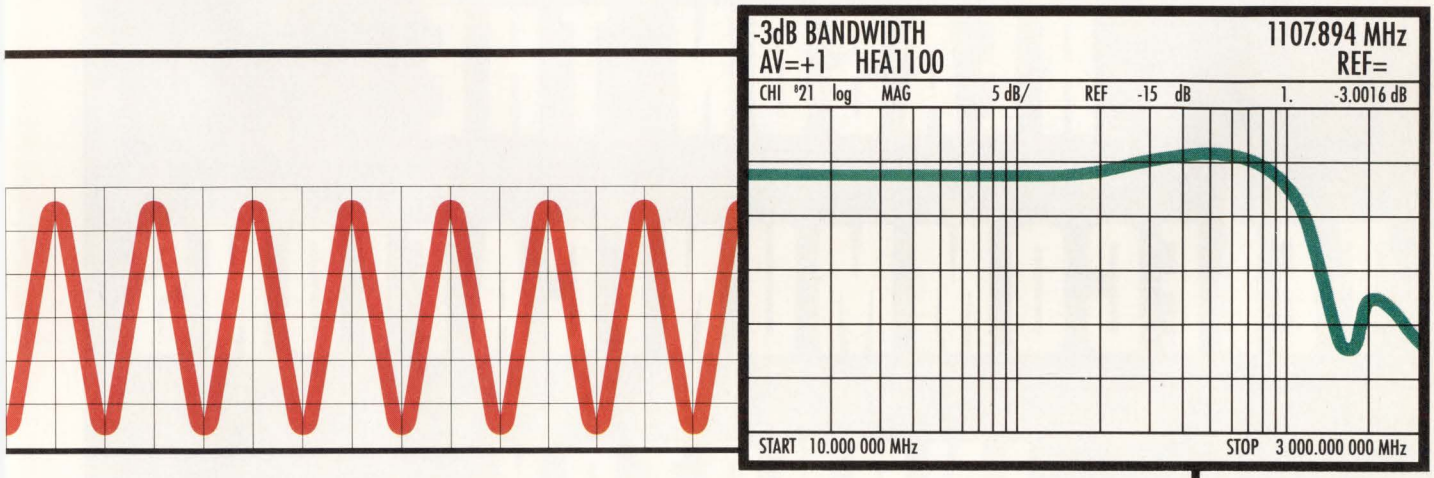


PRODUCT	CONFIGURATION
HFA1100 op amp	Standard pinout
HFA1120 op amp	Output offset adjust
HFA1130 clamped op amp	User-defined output clamp
HFA1110 buffer	Standard buffer pinout
HFA1112 buffer	Standard op amp pinout

Once again, the latest breakthrough in ultra-high-speed op amps comes to you from Harris.

This time, it's the HFA1100. Three times as fast as the old record holder. And just what fast-thinking engineers like you have been waiting for. Quickly imagine what you can do with a bandwidth so huge. Providing excellent phase linearity and a remarkable gain flatness of 0.14 dB to 100 MHz. And your creativity

INNOVATIONS WITH FREQUENCY.



APPLICATIONS

- High-Resolution Displays
- RF Transmitters/Receivers
- Medical Imaging Systems
- Radar Systems
- Flash A/D Drivers
- Video Switching and Routing/Line Drivers
- Fiber Optics

	HFA1100/20/30	HFA1110/12
-3dB Bandwidth	870 MHz	700MHz
Slew Rate	2500V/µsec	2500V/µsec
Settling Time (0.1%)	11 ns	7 ns
High Current Output	60 mA	60 mA
Temperature Range	-40°C to 85°C	-40°C to 85°C
Packages	8-pin PDIP, CerDIP, SOIC	8-pin PDIP, CerDIP, SOIC
Prices (100s)	$9.95	$5.95

needn't stop with standard products. Because the UHF-1 process is available in semicustom, as part of Harris' industry-leading FASTRACK™ design system.

So rev up your oscilloscopes. And get your hands on some HFA1100s today. Just call 1-800-4-HARRIS, ext. 1173.

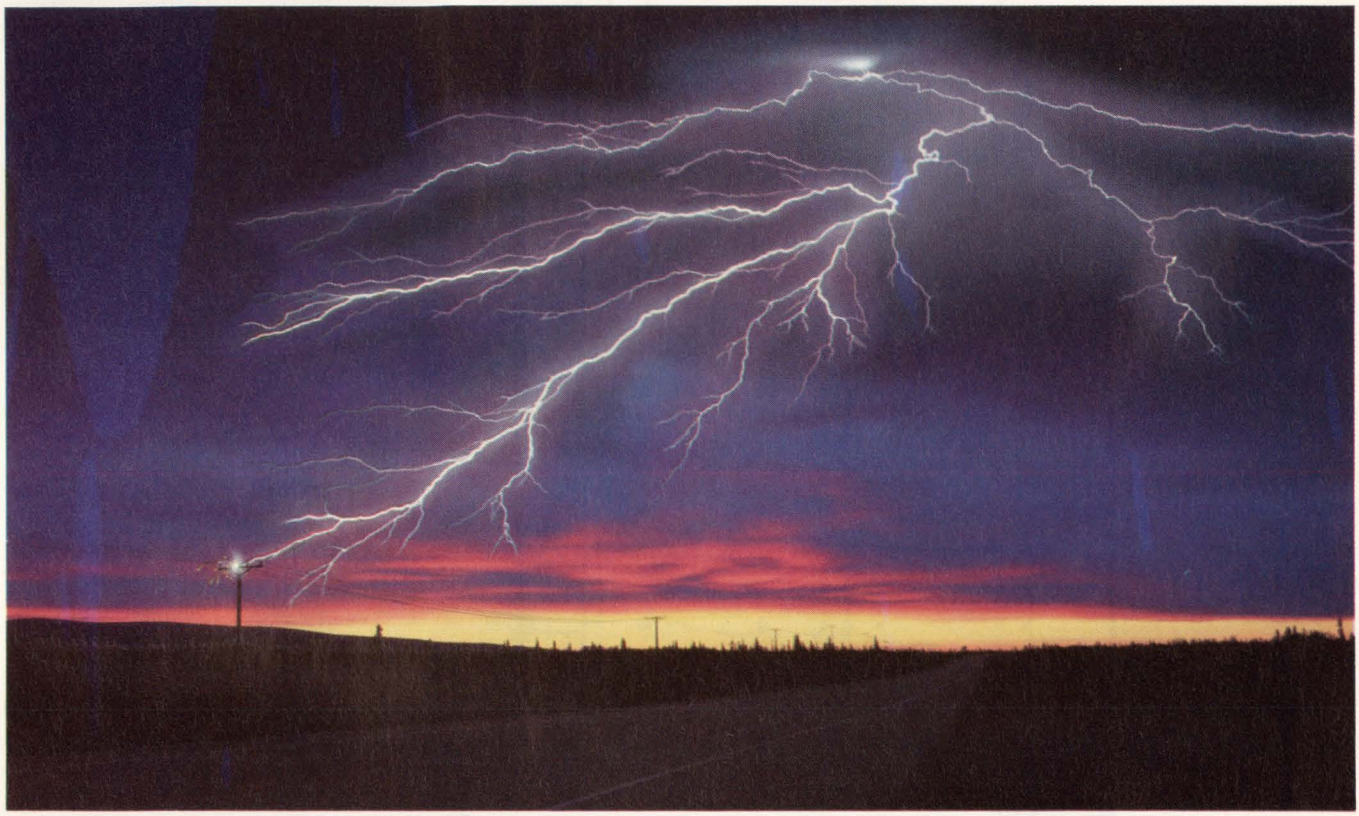
HARRIS SEMICONDUCTOR

CIRCLE NO. 20

Recently, the telecommunications industry needed a new breed of low-signal relay — a relay that could withstand a shocking 2,500 volts, almost double the present standard, yet small enough for dense PCB mounting. They turned to Omron.

Omron responded with the G6N relay. It not only withstands a 2.5KV surge between coil and contacts, its footprint is almost 40% smaller than the previous standard. The G6N is the latest product to join Omron's family of low-signal relays for telecommunications, computer peripherals, office automation and more.

Why did the telecom industry turn to Omron? Because we not only have the broadest line of relays, switches and photomicrosensors in the industry, we also have a proven



track record of innovation. Last year alone, we invested over $170 million in R&D, employed over 1,000 R&D engineers and introduced nearly 100 new products. The telecom industry was also impressed with our highly-automated manufacturing systems, which enable us to provide products of consistent quality in high volumes. The G6N, for example, undergoes 100% automated inspection on 13 critical performance parameters.

With more than 90 affiliates and subsidiaries, 1,500 sales locations and 17,000 employees worldwide, Omron also met the telecom industry's need to provide product and service support around the globe.

Omron's ability to meet the rigorous demands of the telecom industry may come as a shock to some people. But it effectively demonstrates our ability to meet the control demands of any industry, both now and in the future. For complete information on our broad line of control components, call us at 1-800-62-OMRON.

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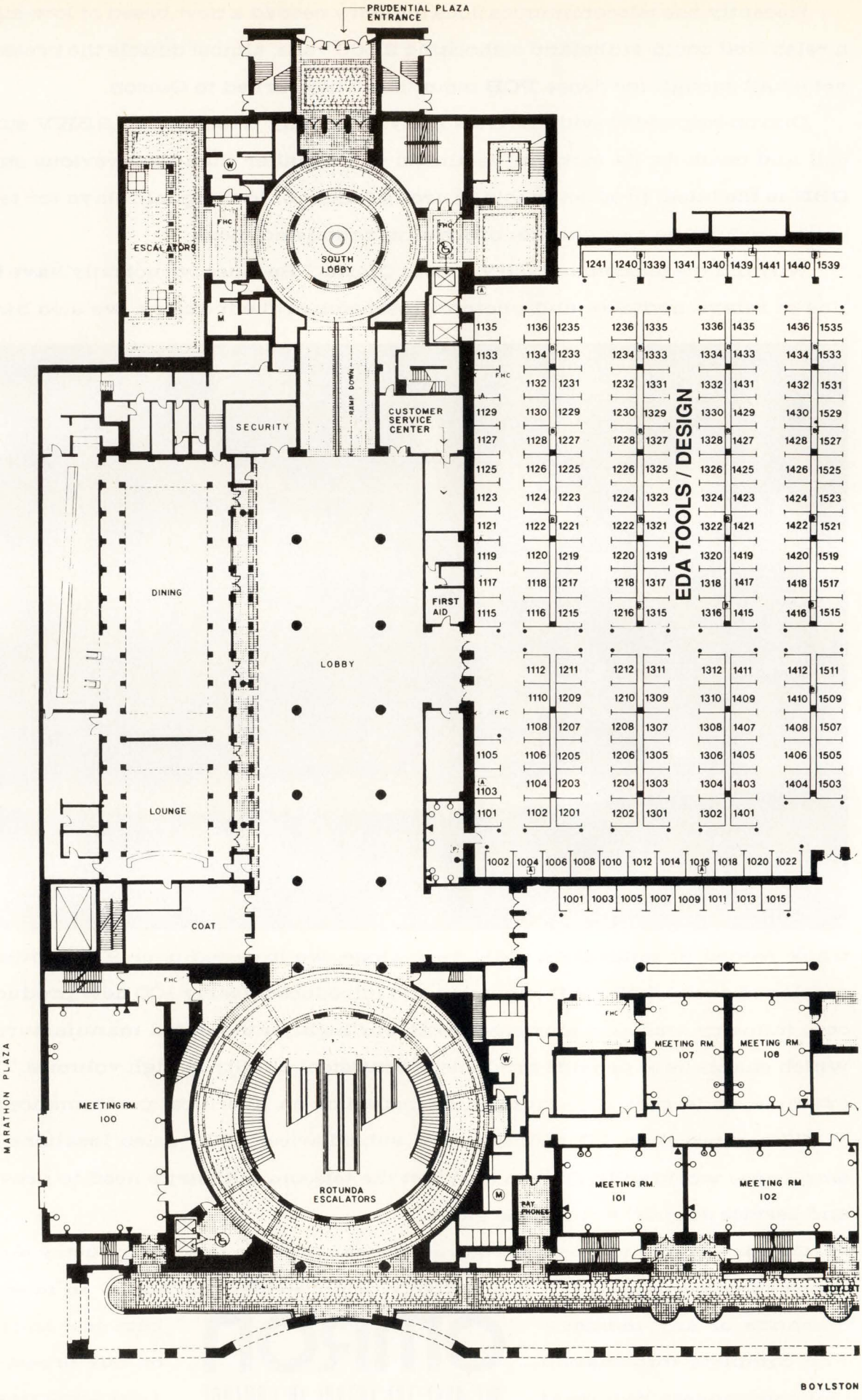
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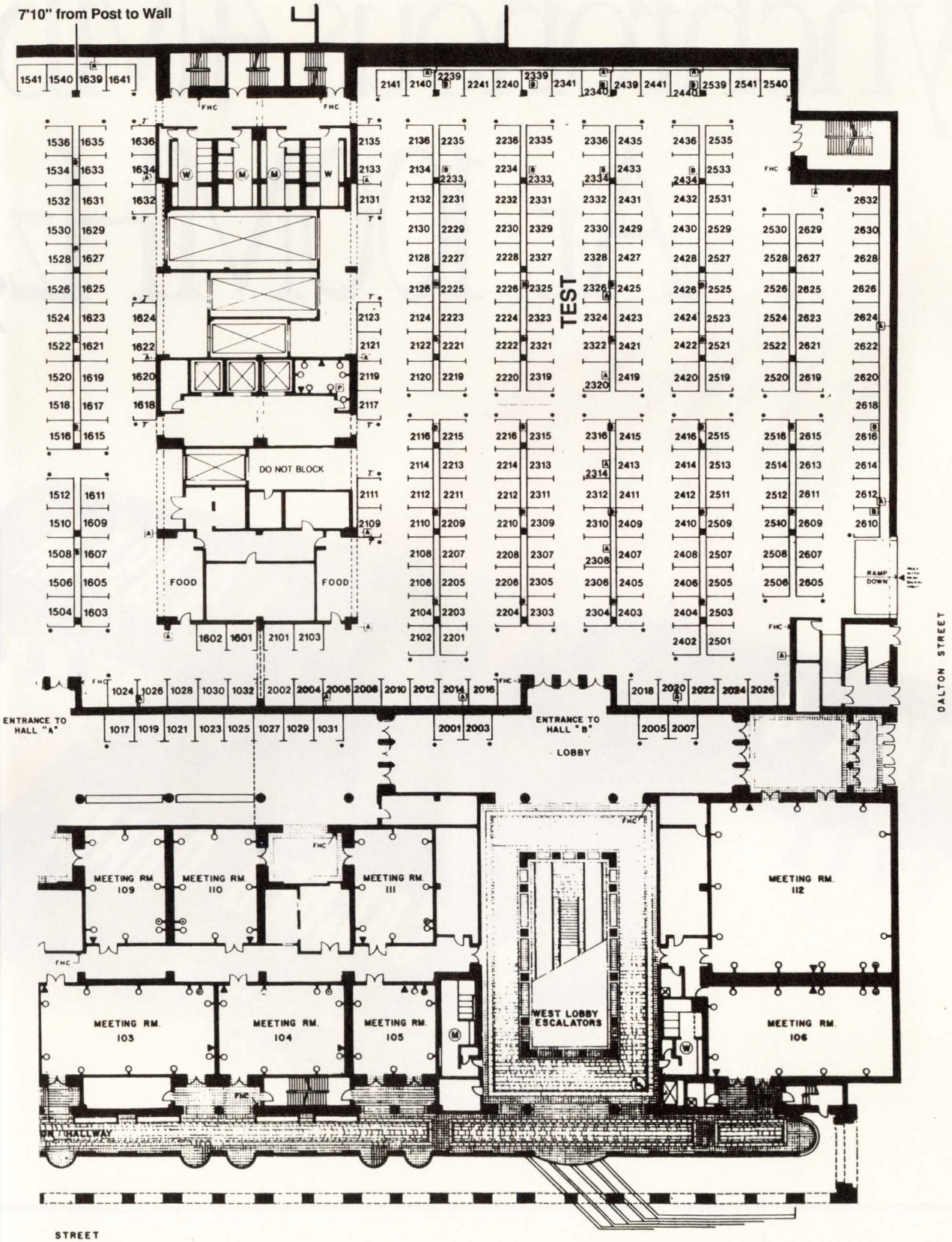
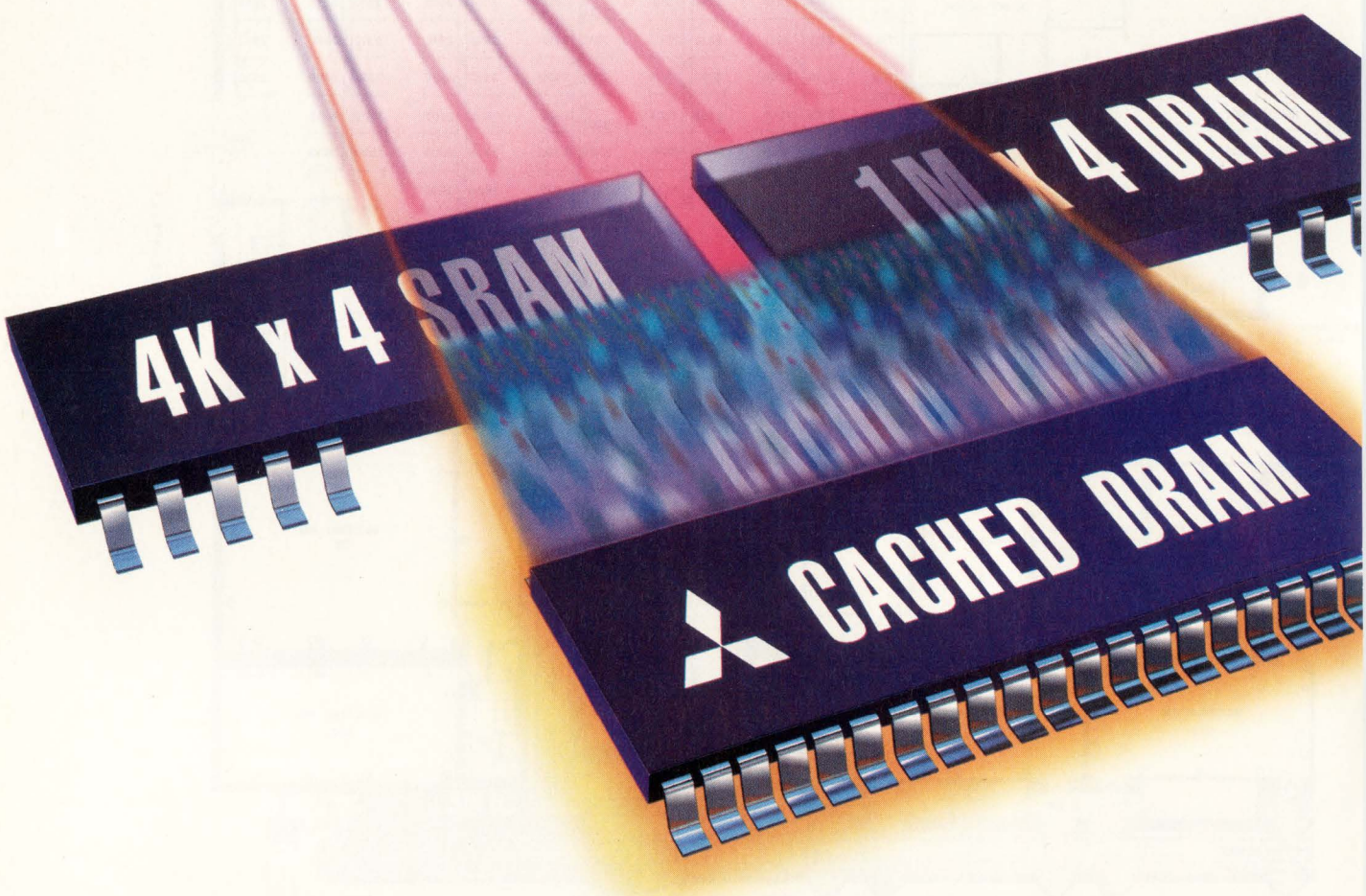


Synchronous 4Mb
At 100MHz



Cached DRAM. It Screams!

Matching low-cost DRAM technology with today's high-speed CPUs can be a design engineer's nightmare. Until now. **Introducing the 100MHz 4Mb Cached DRAM from Mitsubishi.**

FIRST SYNCHRONOUS DRAM

Mitsubishi combined a fast, 4K x 4 SRAM and a 1M x 4 DRAM with a wide, 16 x 4 bit internal bus and a synchronous clock design, all into one tiny TSOP IC. The result is the industry's first synchronous DRAM with on-board cache.

100MHz OPERATION

The Cached DRAM's large, 16 x 4 bit internal data path can transfer a 16-line data block in just one cycle, allowing the small on-chip cache to perform like a much larger external cache. The result is fast, 100MHz performance at a much lower cost than separate cache configurations. Plus, the Cached DRAM's fast copy-back scheme significantly reduces the miss cycle penalty time.

COST-EFFICIENT, SMALL SIZE

The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

LOW POWER OPERATION

With a clock that can be stopped to reduce power consumption to as low as 1mW, the Cached DRAM is ideal for portable and highly integrated applications where low power consumption, compact size and fast operation are essential.

MITSUBISHI'S CACHED DRAM PERFORMANCE

Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.

Samples Available June 1992

Standard 4Mb DRAM.

Actual size.

4Mb Cached DRAM is only 7% larger than a standard 4Mb DRAM.

Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**

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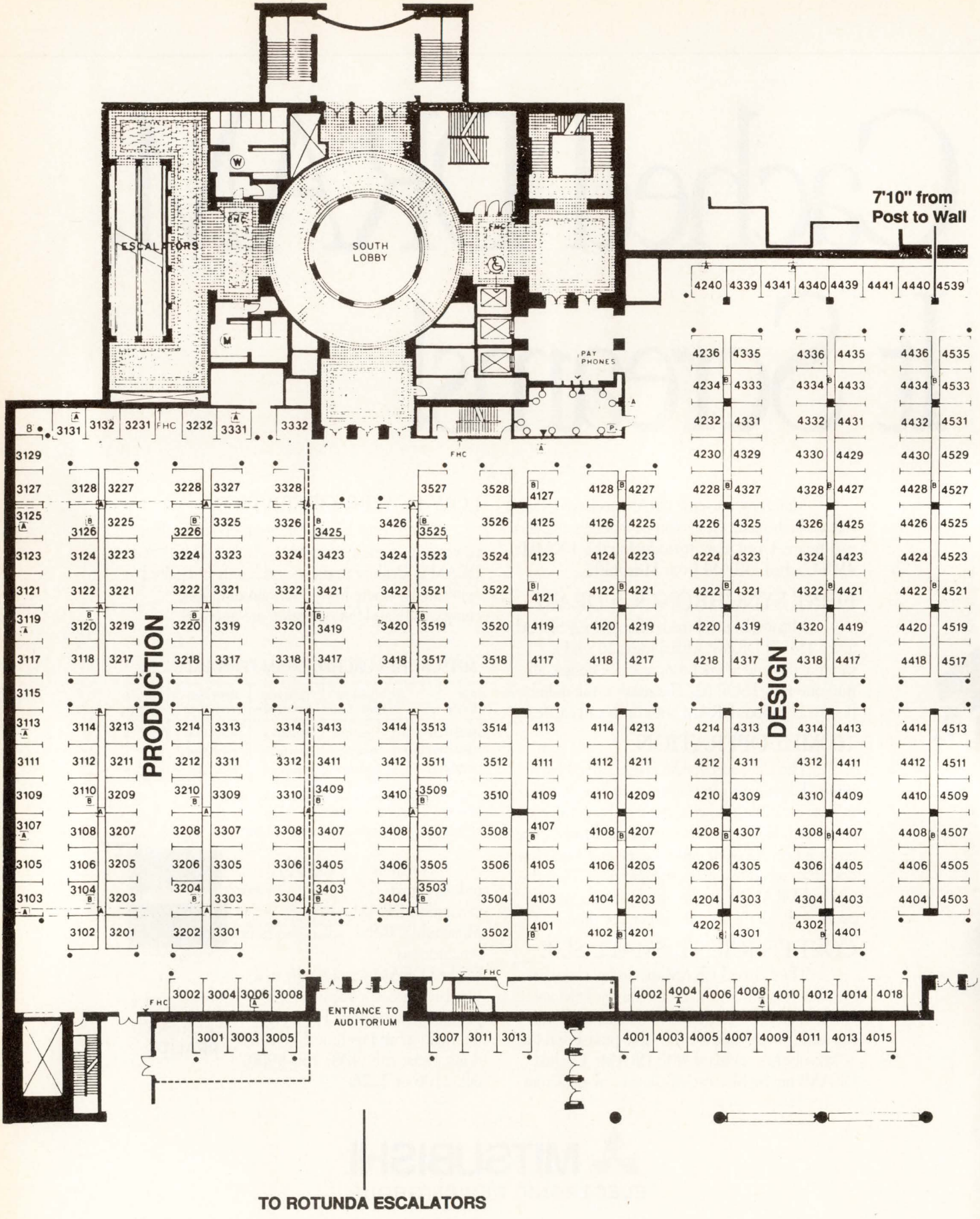
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ESCALATORS
PAY
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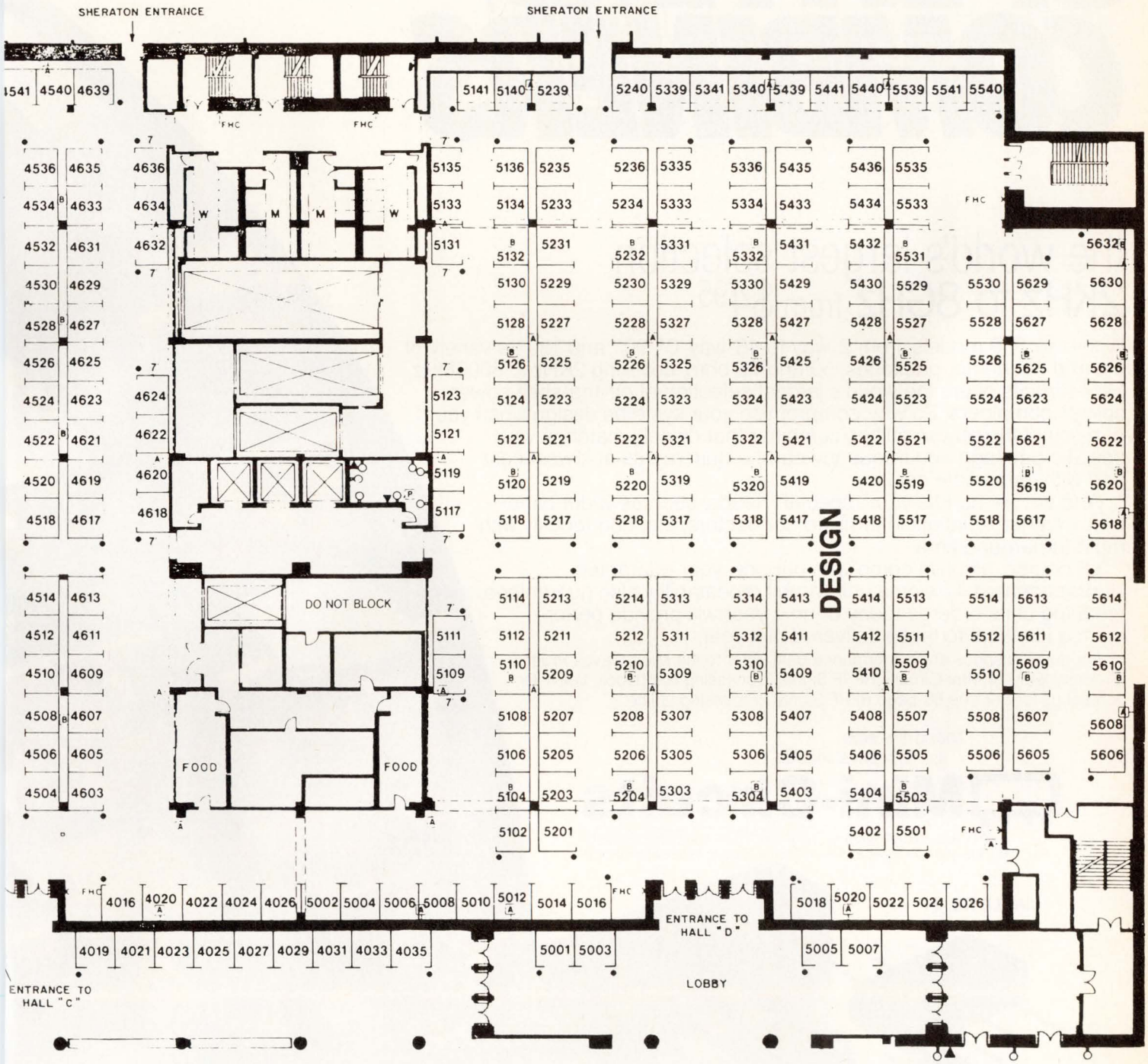

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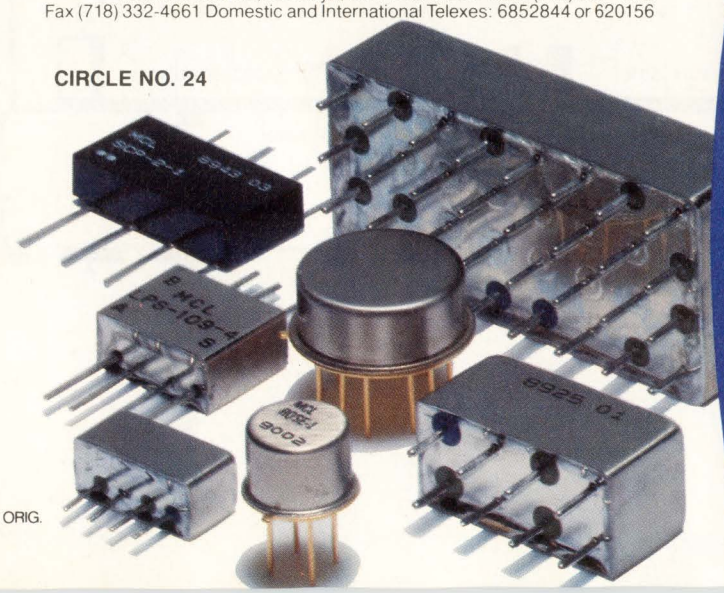

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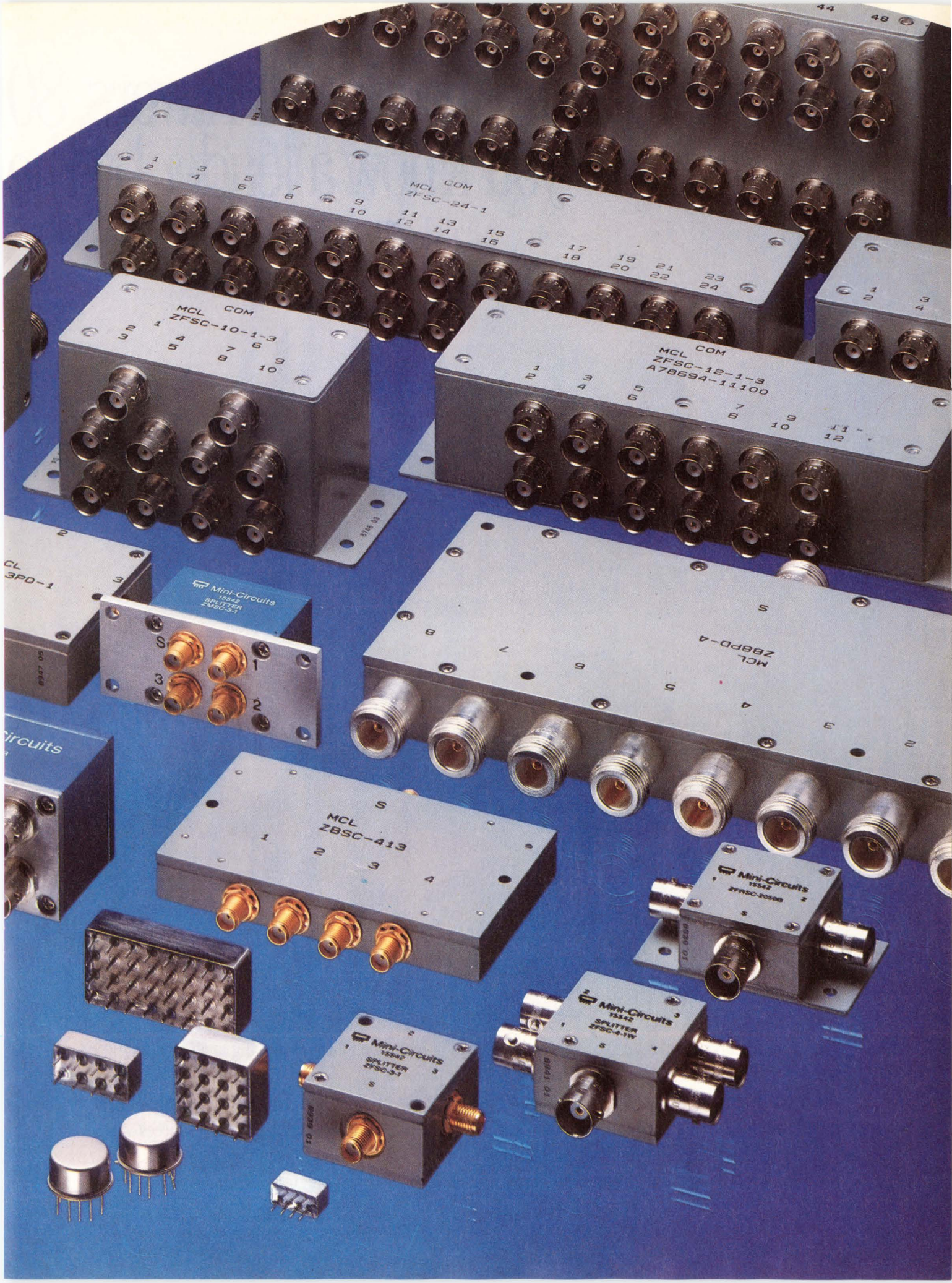
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ZFSC-24-1
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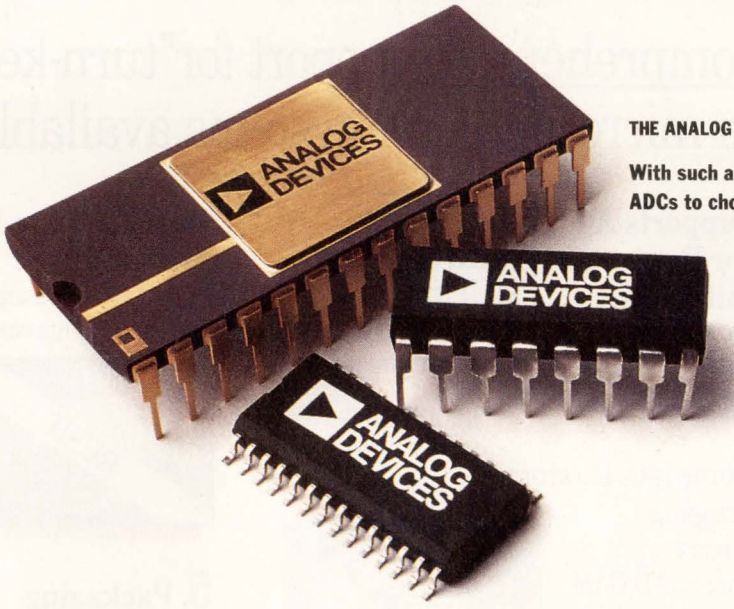
billion served, or 35 sampling ADCs, breadth of its product line.



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expertise at integrating high-performance analog and digital circuitry on the same IC. And it is this same expertise that has made us the acknowledged leader in advanced mixed-signal technology.

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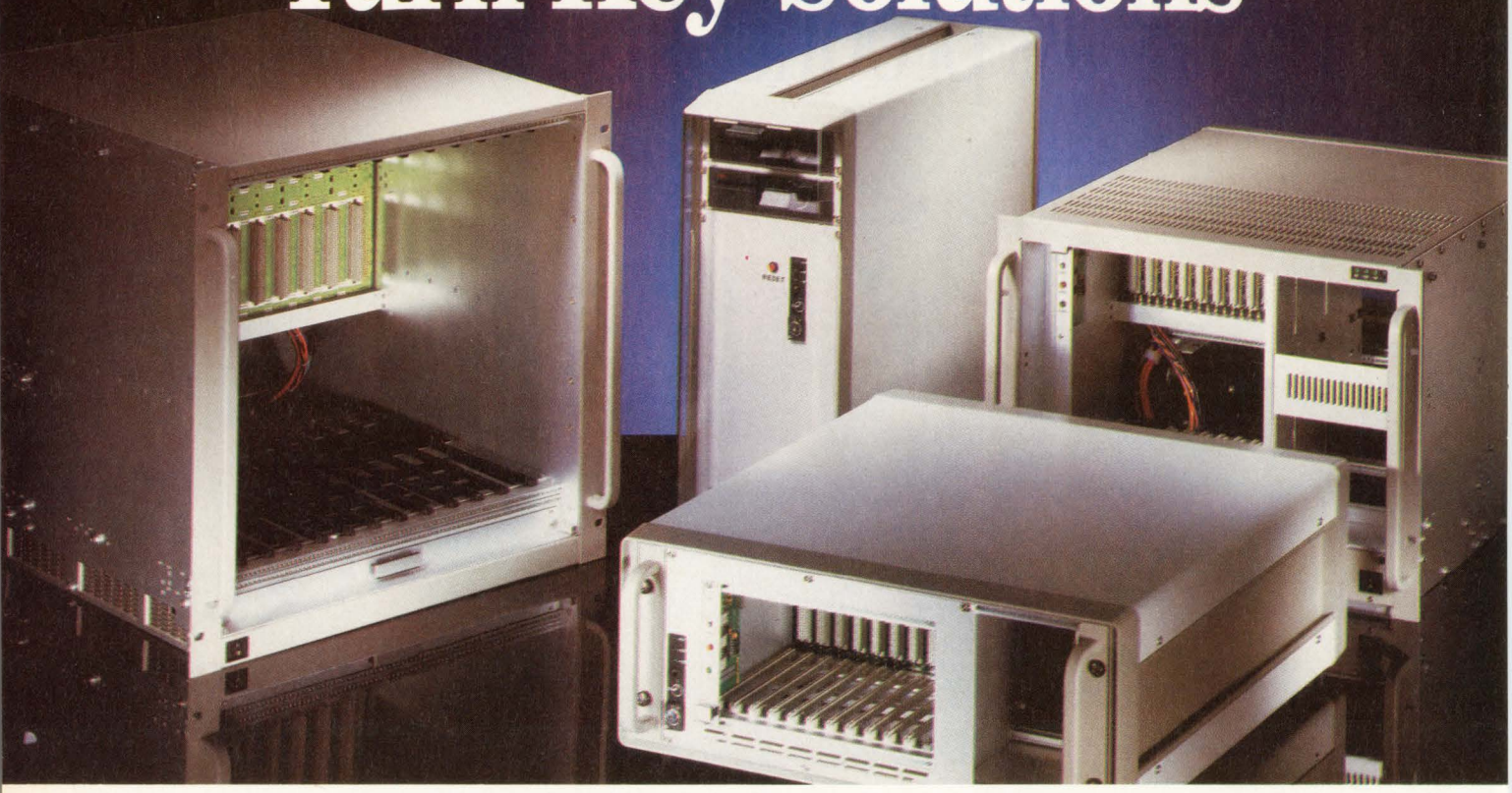

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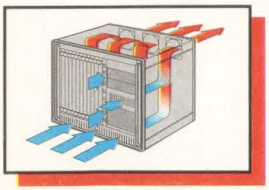

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BOSTON GUIDE

TRANSPORTATION

Driving in and around Boston is not for the faint of heart. A stranger is likely to become confused by the one way traffic on the city's older narrow streets and the endless number of squares and circles that make driving seem more like understanding geometry than covering distance. Don't feel badly, many natives are in the same predicament. Major highways circle the city and an extension of the Mass. Turnpike splits it. Once you get into Boston, park in a garage--metered spaces are scarce--and walk, take the subway, or a cab. The city is small and you can't be too far off.

GETTING IN:

From the North: Rts. 95, 1, and 93 enter Boston. Four major exits--STORROW DRIVE is best for the Back Bay, Beacon Hill, Cambridge, and Government Center; DOCK SQUARE provides access to Logan Airport, North End, Waterfront, and Faneuil Hall Marketplace; HIGH STREET goes downtown; KNEELAND STREET takes you to Chinatown and the Theatre District.

From the South: Rts. 94, 24, and 3 lead into Rt. 128 East which becomes Rt. 93 North inbound. Two major exits--KNEELAND ST/CHINATOWN is best for Back Bay and Theatre District; DOCK SQUARE leads to Logan Airport, North End, Waterfront, and Faneuil Hall Marketplace.

From the West: The Mass. Pike is the best of all available choices. Three major exits--EXIT 18-20 (Cambridge/Allston) provides access to Cambridge and Charles River locations; EXIT 22 (Prudential Center/Copley Square) is best for Back Bay, Fenway, and Kenmore Square; EXIT 24 (Expressway/Downtown) is best for Downtown, North and South highway access.

GETTING OUT:

To the North: Rt. 93 leads out of Boston and splits into Rt. 93 and Rt. 1. This fork is particularly treacherous; it is best to know exactly which Rt. to take before the moment of reckoning arrives. Rt. 93 heads to the Northwest suburbs and New Hampshire. Rt. 1 is best for Mystic River (Tobin) Bridge, the North Shore, coastal New Hampshire, and Maine.

To the South: Leaving Boston for the South would test the patience of Job because Rt. 93 (Southeast Expressway) is the only choice. Entrances are found at KNEELAND STREET, DOCK SQUARE, and STORROW DRIVE.

To the West: Rt. 90 (Mass Pike) is the best choice. From Downtown enter the Pike at ARLINGTON STREET, COPLEY SQUARE, and MASS. AVENUE.

GETTING AROUND:

To and from airport:

Logan Airport is linked to the city by cabs, subways, and shuttle buses that stop at the major hotels. The Blue Line on the "T" (subway) takes you to Airport Station at Logan where a shuttle bus will drop you off at your particular terminal.

BUS:

One major bus terminal serves Boston: Greyhound, 10 St. James Ave., 423-5810, now called Greyhound-Trailways.

SUBWAY:

Boston's was America's first subway system and on it you may meet the famous "Charlie" who is condemned to ride the "T" till the rates come down. With luck you won't share his fate. The "T" has four lines, known by the colors Blue, Red, Orange, and Green. Each line passes through at least two of the downtown stations--Park Street, Washington Street, State Street, and Government Center. In most cases the fare is $.85¢.

TRAIN:

Amtrak provides national service from South Station, Atlantic Ave., Boston (South Station "T"). Call 482-3660 for information.

The Boston and Maine Lines serve suburban stops from North Station, 150 Causeway St., Boston (North Station "T"). Call 722-3200 for information.

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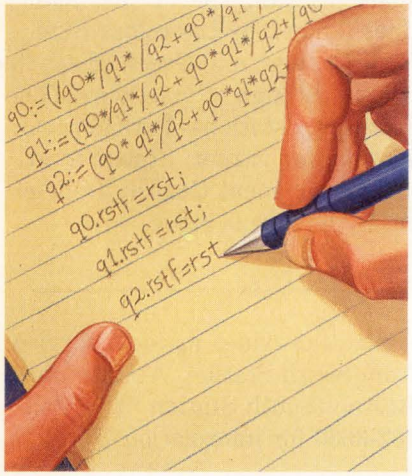
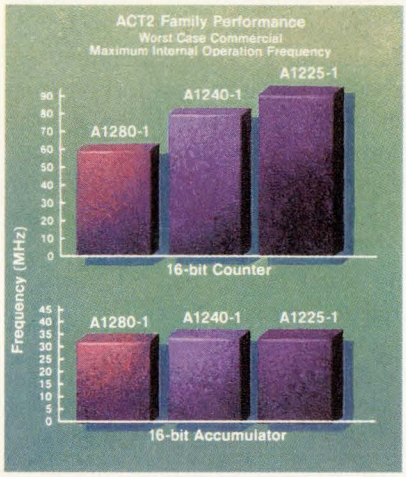
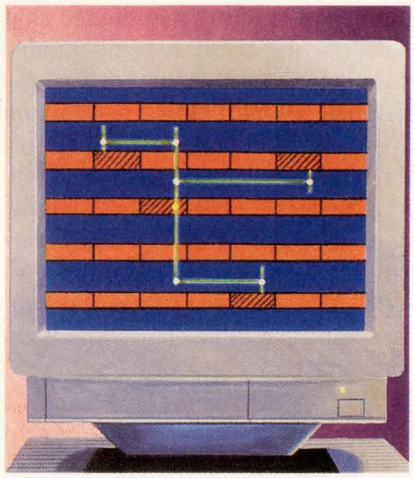
You Design Actel FP You Do A PLD. But Th







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Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.

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Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

Announcing A Simple Way To Get From PLDs To FPGAs.

If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

First of all, you don't have to give up your existing PLD design tools or Boolean equations. Actel's ALES™ 1 program translates the output of PLD tools like CUPL™ and LOG/iC™ into logic optimized for our ACT™ devices. ABEL™ 4.0 includes optimization for Actel devices. Entire FPGA designs can be developed with PGADesigner.™

Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, field-programmable, channeled gate arrays.

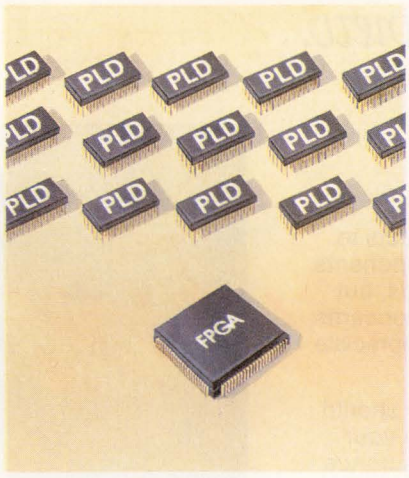
Other FPGA manufacturers fall short on design verification. Our exclusive Actionprobe® diagnostic tools, give you 100% observability of internal logic signals. So you don't have to give up testability for convenience.

It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-

GAs The Same Way e Similarity Ends There.

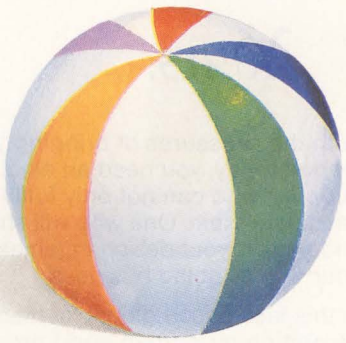
More Flexibility And Capacity.

Designing with Actel FPGAs gives you more freedom than you ever imagined. More gates. More flip-flops. More I/O. In fact, our new A1280 is the largest FPGA in the world.



Small Footprint.

Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.



More Fun.

Designing Actel FPGAs is so simple that you'll have more time to do the things that made you want to become an engineer in the first place. Or just relaxing. You've earned it.

ful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

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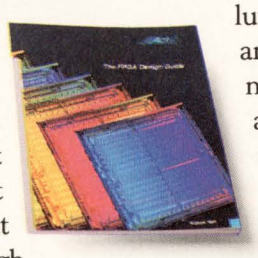

The FPGA Design Guide

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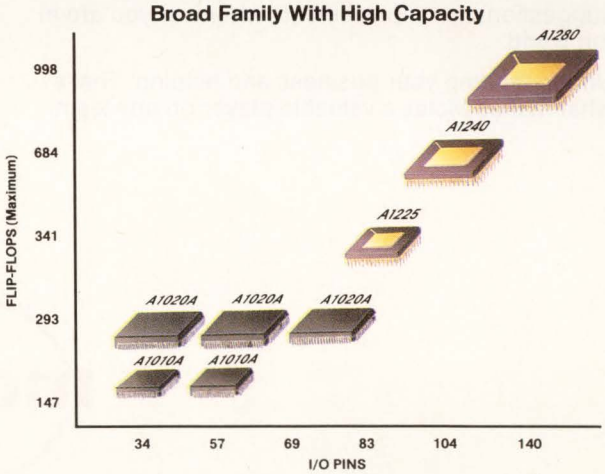

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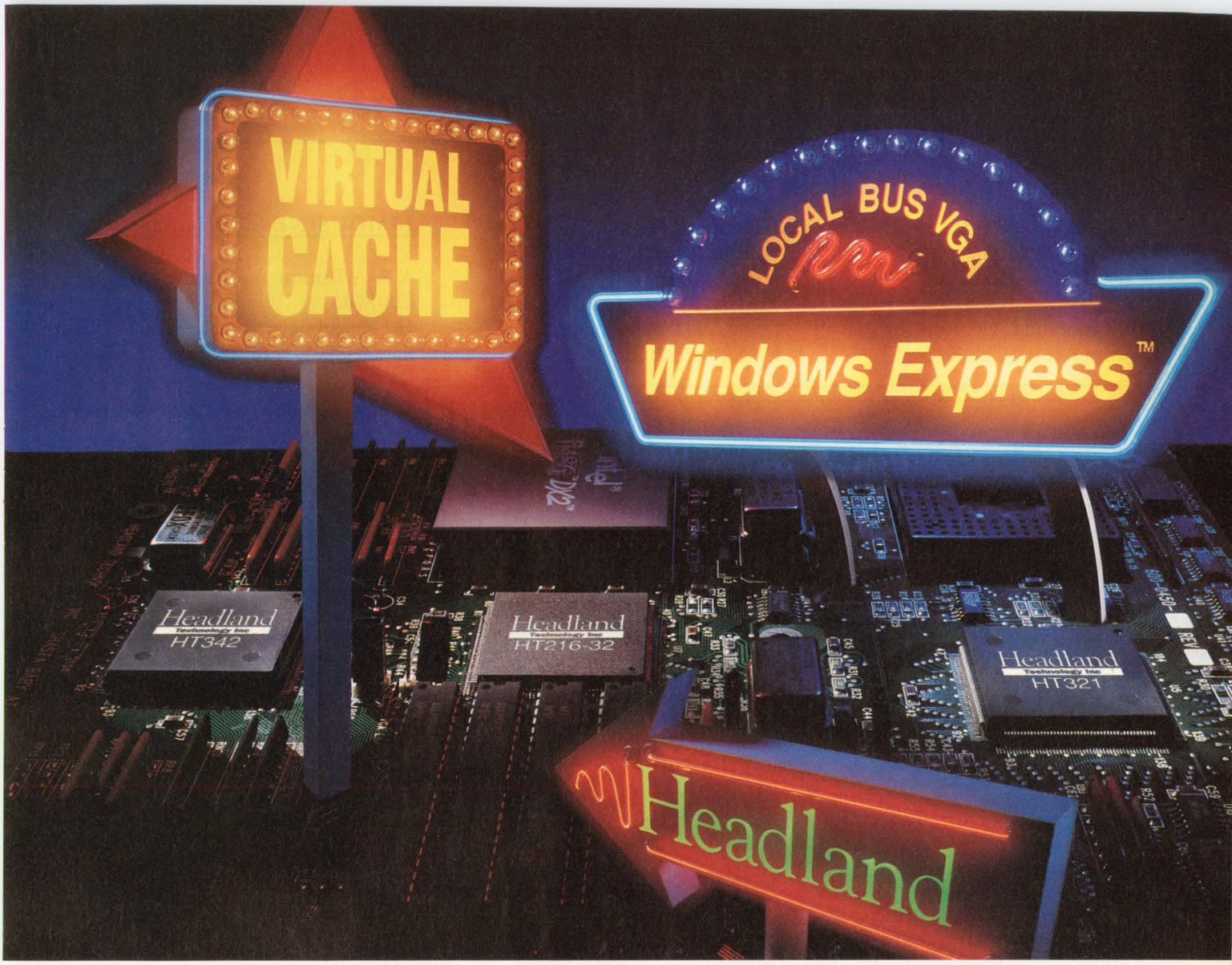
CIRCLE NO. 28



MORE SIGNS OF THE TIMES.

The signs of the times are everywhere. Designers are demanding greater speed and greater functionality at lower cost. And they're turning to Headland's Virtual Cache™ 486 Chip Set and Windows Express™ Local Bus VGA for unbeatable price/performance.

HTK340
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Team up Headland's HTK340 Virtual Cache 486 core logic chip set with Intel's new super-fast 486DX2. The result is a blistering 29.3 MIPS—*without external cache.* With special features like byte gathering write buffer and out-of-order operations, the HTK340 offers the best price/performance in the business.

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(486DX2) + (HTK340) = 29.3 MIPS
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HT216-32
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GRAPHICS
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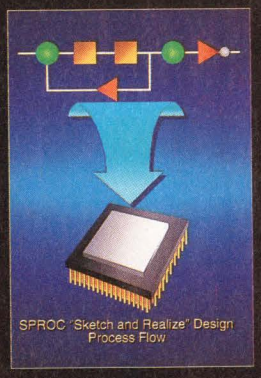
Town Taxi, 536-5000

SIGHTS

The Hynes Convention Center Area: 900 Boylston St., is located near the Copley Square section of Boston and near the renovated South End neighborhood. Copley Square, the Prudential Center, John Hancock Tower, Symphony Hall, the Institute of Contemporary Art, Copley Place and the prestigious Newbury Street shopping district are all within easy walking distance from here.
On a good weather day an energetic visitor may take a 20-minute to half-hour walk out of this heart of Boston to the Public Garden, then into the Boston Common to reach the Downtown Crossing shopping area.

Back Bay: The Back Bay was created from marsh and tidal flats 120 years ago and is now the city's

Changing the Signal Processing World Forever.



ZAP! Sometimes the best ideas come suddenly. With one great flash of insight, the problem is illuminated and quickly solved. Provided, of course, you are working with SPROC™ signal processing technology from STAR Semiconductor.

Before SPROC, many bright ideas produced little more than a flash of light and wasted energy. And you have probably seen more than one enlightened solution bogged down in the time-consuming prototyping of an analog board or the agonizing handcoding of a DSP chip.

Now SPROC can help you transform your bright ideas into brilliant signal processing solutions in a flash. By integrating an advanced, programmable signal processing chip and a powerful, easy-to-use development system, SPROC technology allows you to create and modify an application in a matter of minutes . . . without writing code.

How? The SPROClab™ development system uses the unique "Sketch and Realize"™ design approach to allow rapid transformation of signal processing designs from signal flow block diagrams. SPROClab automatically converts your diagrams into code optimized for the SPROC chip, which contains multiple on-chip processors for real-time signal processing performance.

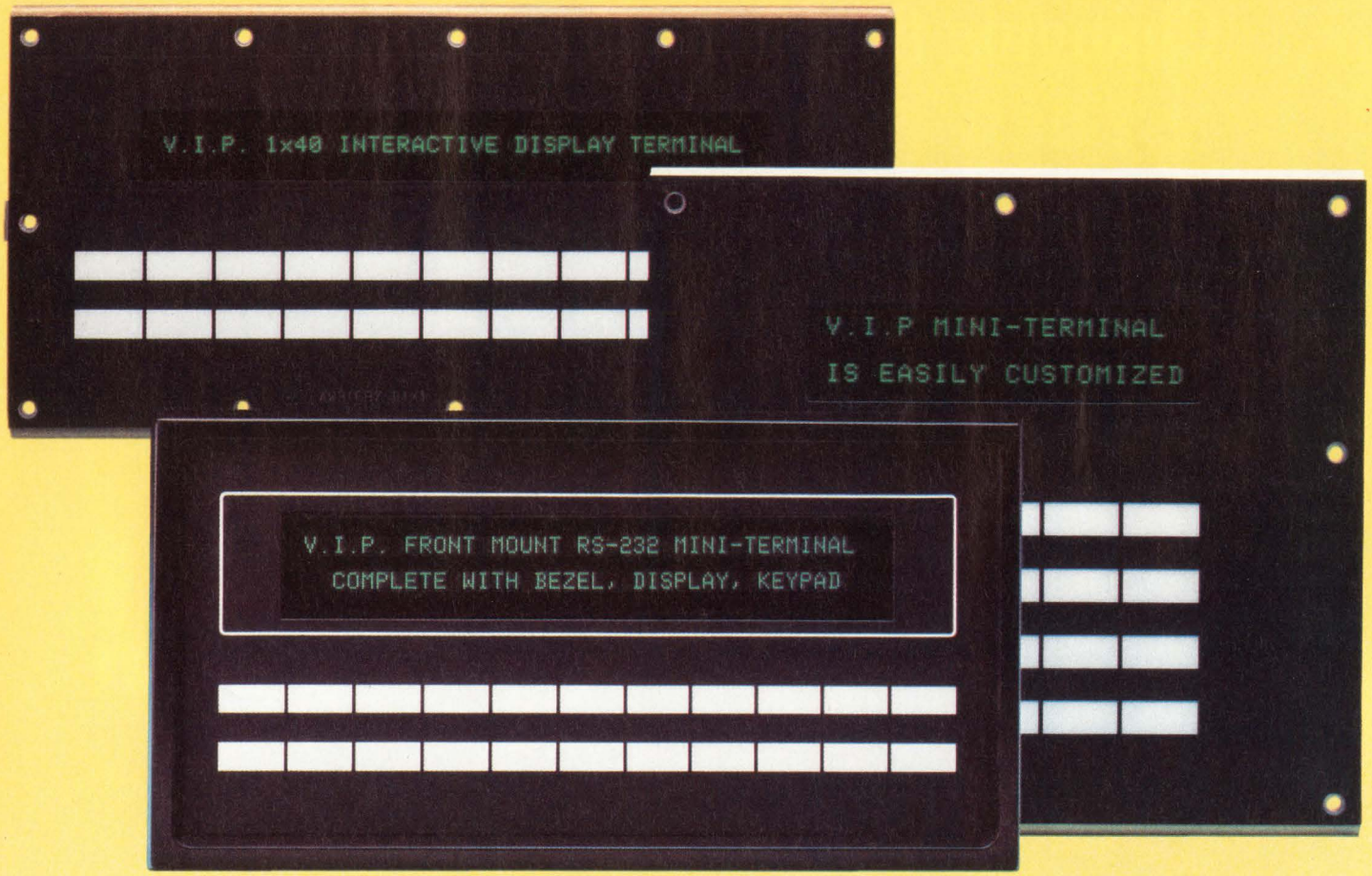
To learn more about the new SPROC technology, specially-designed to handle the needs of real-time signal processing, call for your ***free*** 350-page DataBook and demonstration disk. **(908) 647-9400.**

STAR SEMICONDUCTOR
The Signal Processing Company

25 Independence Boulevard, Warren, NJ 07059

CIRCLE NO. 30

A Flash of Brilliance.



You have better things to do than reinventing the operator interface.

You **could** spend hours selecting displays, switches, and encoders for your operator interface. Of course, you'd still have to fabricate a wiring harness and individual panel cutouts for all those components. Then you'd be set, until the next configuration change meant redoing half your work.

But why do things the hard way, when you can choose a **V.I.P.**™ instead? This integrated display/keyboard system from IEE costs less than integrating "bits and pieces" yourself and also saves time. You see, **V.I.P.** is a ready-made "mini-terminal"—a plug-in operator interface with lots of convenient features:

- Bright, easy-to-read vacuum fluorescent display.
- Operates on +5 VDC.
- Tactile dome membrane switches, with "slide-in" changeable legends. Ask about custom artwork and legends.
- One DB-25 RS-232C connector for display and switch I/O.
- On-board EPROM-based canned messages.
- Compact package easily seals to your front panel.

So what else is new? An optional front-mounted package—with a die-cast bezel—for our popular two-line by 40-character model. And other new models are in the works.

Call today for ideas on how to use **V.I.P.** You'll have to come up with your own ideas for what to do with the time and money you'll save.

Industrial Electronic Engineers, Inc.
Industrial Products Division
7740 Lemona Avenue
Van Nuys, CA 91405
Tel. (818) 787-0311, ext. 418
Fax (818) 901-9046

IEE® THE DISPLAY MAKERS™

See us at the Eastern EDN Caravan — now through June '92 CIRCLE NO. 31

WE'VE GOT TWO WORDS FOR PEOPLE LIKE YOU.

FAX VOdem™ \faks-vō-dem\ *n* [origin: Yamaha LSI] **1**: world's first single-chip **multimedia communications device** **2**: Fax/data/ADPCM voice and caller I.D. **3**: transfers data, fax and voice via a single line

If you're one of those people who goes around integrating communications devices into PCs, laptops and other hardware, we've got two words for you — FAX VOdem™.

What do they mean? In a word, plenty. Yamaha defined FAX VOdem on September 26,1991, as a major breakthrough in multimedia communications. And now it's going to change the way you communicate. Because with FAX VOdem, you'll be able to integrate Fax. Data. ADPCM voice communications. And caller I.D. All on a single line. And all with a single-chip LSI that'll give your products multimedia communications capabilities you never thought possible.

Sound too good to be true? It's not. And we'd like to prove it to you. Just call us at 1-800-543-7457 or write and we'll send you all the nitty gritty technical details that wouldn't fit in this ad.

So start integrating FAX VOdem into your new products. And when your colleagues notice what a great communicator you've become, just tell them you've got two words for people like them.

YAMAHA® LSI

Yamaha Corporation of America
Systems Technology Division
981 Ridder Park Drive, San Jose, CA 95131
(408) 437-3133 FAX (408) 437-8791

beautiful combination of commercial, historical, cultural and residential properties. Stroll, run, bike, or skate down the Charles River "Esplanade" and wind up at the Hatch Concert Shell where the Boston Pops perform each summer and mix with veteran people watchers.

Beacon Hill: Walking the "Hill" is a must for people whose heart can be charmed by gas lights, cast-iron boot scrapes, and front doors with brass knockers that lead into elegant brownstone lodgings.

Boston Common and Public Garden: These two parks are bordered by Beacon Hill and Back Bay. The swan boats swim every spring and summer; so wear a sheepish grin and head to the Public Garden for a ride.

Copley Place: Boston's newest mall houses gourmet and designer shops for every taste. The complex contains a 9-screen movie theatre and connects to the Westin Hotel.

Downtown Crossing: The busiest intersection in New England is closed to automobile traffic. The pedestrian shoppers and strollers at the intersection of Washington and Summer Streets are often audience to impromptu performances by street musicians. Home of the famous Filene's Basement.

Faneuil Hall Marketplace: Whatever you want to eat, they got. A wide variety of shops help fill the marketplace. Go down and take a look. Eventually you'll see a familiar face or an interesting stranger.

Fenway Park: Home of the Red Sox and described by John Updike as the "jewel" among baseball parks. In the shadow of the "Green Monster" are two of the best sports shops to be found anywhere.

Freedom Trail: Start at the Boston Common Visitor Information Booth near Park Street subway station and proceed to 16 historic sites of our colonial and revolutionary days. Stops include Paul Revere's House, Old North Church, U.S.S. Constitution--"Old Ironsides," and the Bunker Hill Monument.

Harbor Islands: Picnic, swim, camp, or visit historic ruins at the Harbor Islands State Park. Boats leave from Long Wharf and for information contact Boston Harbor Islands State Park 727-5290.

SURFACE MOUNT MIXERS

ULTRA·REL™ MIXERS
*5-YR. GUARANTEE **

1-2500MHz FROM $3.30 (1000 qty)

The opportunity for automated, low-cost assembly is a key benefit of surface-mount technology but is often wiped out by the high price of surface-mount components. Now Mini-Circuits offers a new series of mixers to meet the pricing and quality demands of SMT...only $3.30 in 1,000 quantity ($3.95 in quantity of 10)...lower than most conventionally-packaged mixers.

The Ultra-Rel™ SCM-series spans 1 to 2500 MHz and is housed in a rugged non-hermetic 0.38 by 0.75 by 0.2 in. high (max. dimensions) plastic/ceramic package. Spacing between connections is 0.2 in.

Each SCM is built to meet severe environmental stresses including mechanical shock/vibration as well as temperature shock. Operating and temperature storage range is -55° to +100°C. Ultra-Rel™ SCM mixers come with a five-year guarantee, ready for off-the-shelf delivery, and available in tape-and-reel format (500 qty, 32 mm).

Unprecedented 4.5 sigma unit-to-unit repeatability is also guaranteed, meaning units ordered today and next year will provide performance identical to those delivered for your initial prototype design.

When you think SMT for low-cost production, think of Mini-Circuits' low-cost Ultra-Rel™ SCM mixers.

*** ULTRA·REL™ MIXERS 5 yr. Guarantee**
with extra long life due to unique HP monolithic diode construction, 300°C high temp. storage, 1000 cycles thermal shock, vibration, acceleration, and mechanical shock exceeding MIL requirements.

SPECIFICATIONS

MODEL	SCM-1		SCM-2		SCM-5		SCM-2500	
Freq. Range (MHz)								
LO, RF	1-500		10-1000		1250-1800		500-2500	
IF	DC-500		DC-500		DC-500		DC-500	
Conversion Loss (dB)								
mid-band	6.0		6.0		5.5		5.7	
total range	6.5		7.0		5.5		6.4	
Isolation (dB)	(L-R)	(L-I)	(L-R)	(L-I)	(L-R)	(L-I)	(L-R)	(L-I)
low-band	60	50	50	55	28	18	35	18
mid-band	45	45	40	40	28	18	35	18
high-band	40	40	35	30	28	18	35	18
PRICE (1000 qty)	3.30		4.15		8.85		8.85	
(1-9 qty)	4.25		5.45		11.95		11.95	

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

finding new ways...
setting higher standards

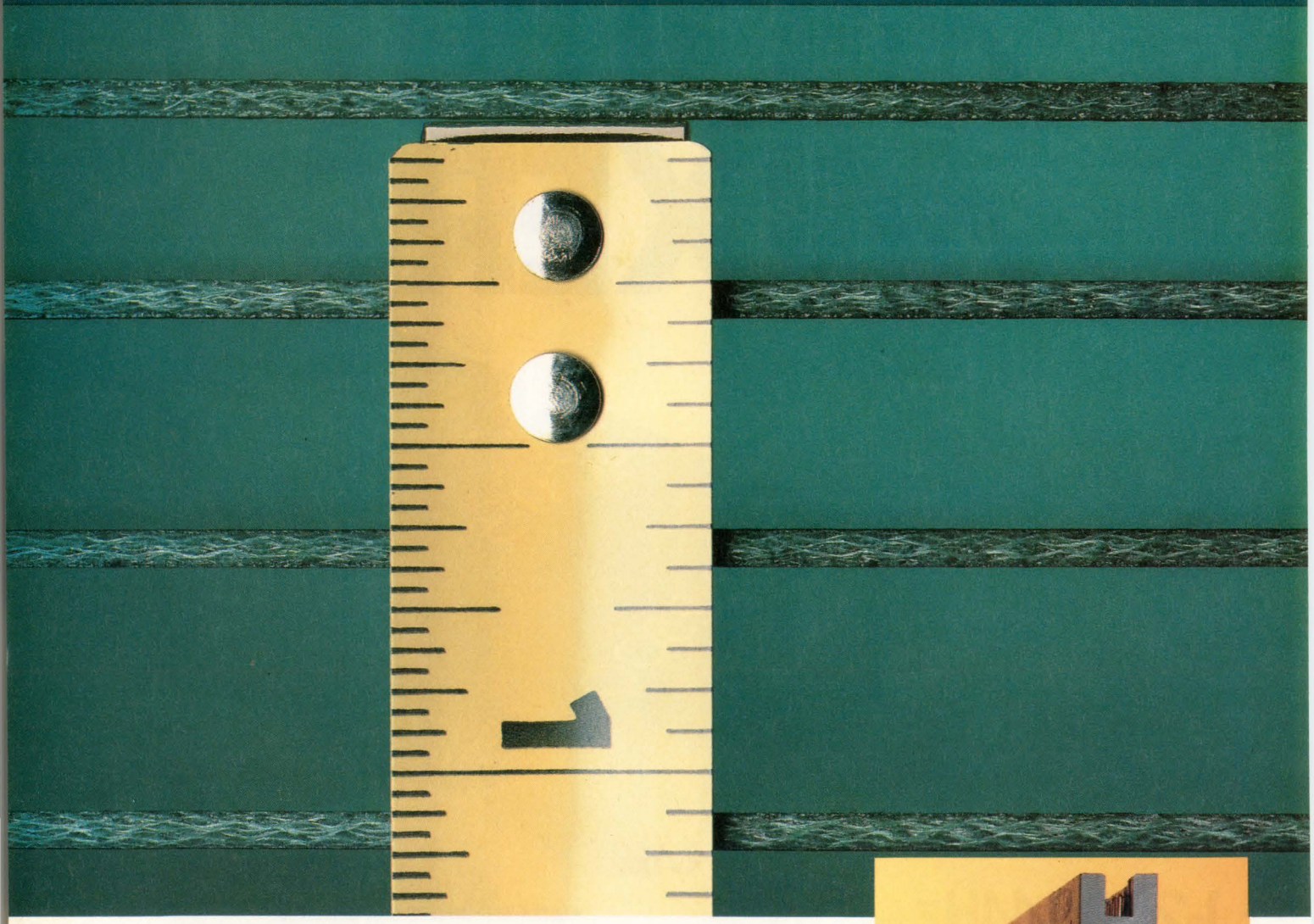
Mini-Circuits

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

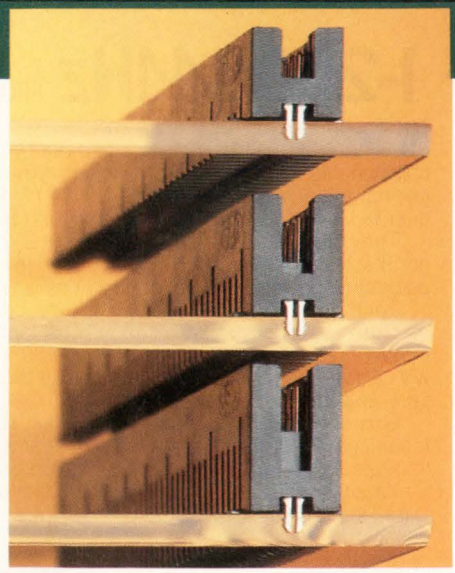
CIRCLE NO. 33

C115 REV. F

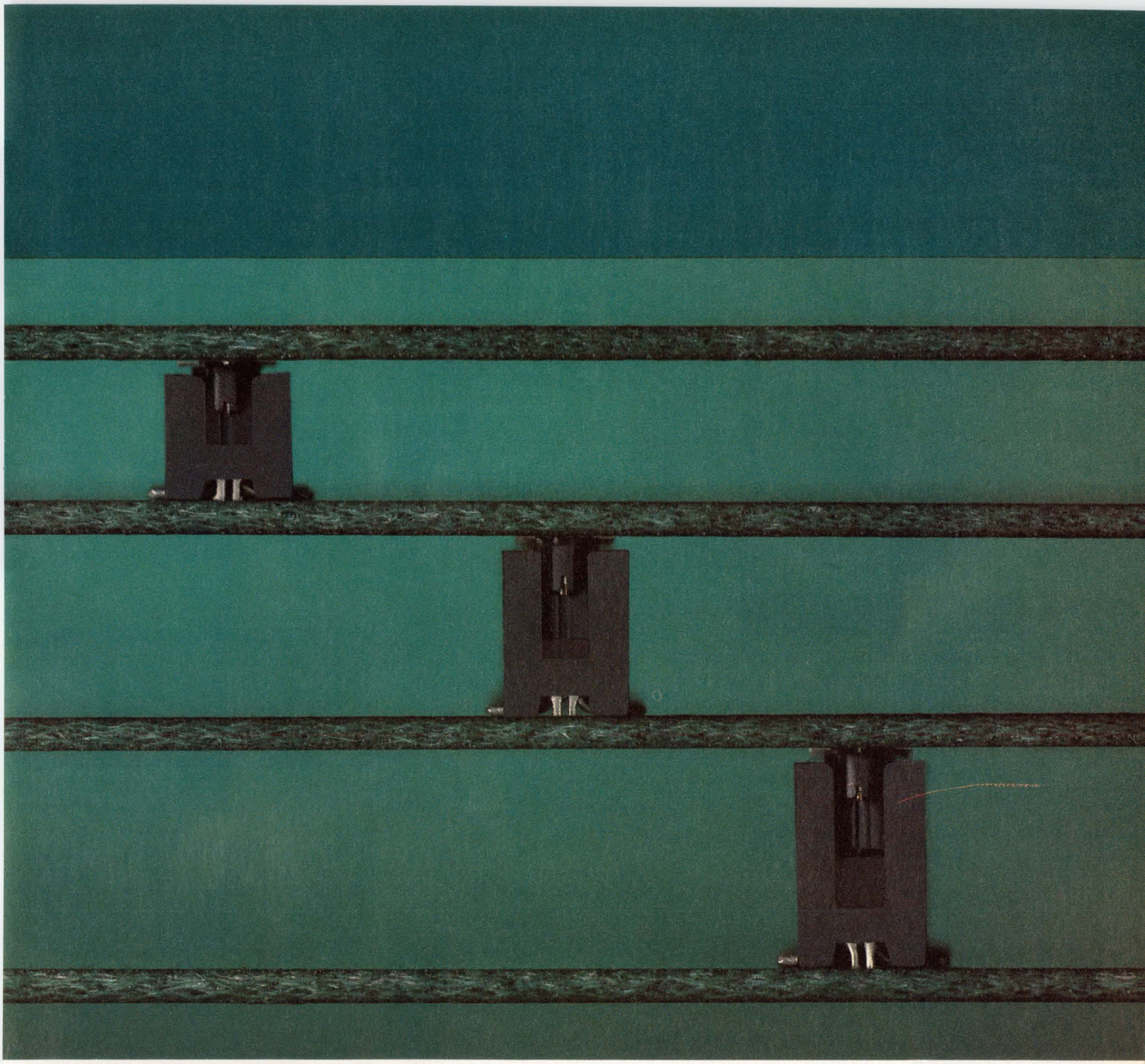
.050 centerline stackers. Close, closer, closest.



THIS IS AMP TODAY.



Surface-mount stack heights: .250"/.320"/.390"



AMPMODU 50/50 Grid Connectors give you a choice of parallel pcb stack heights: .390", .320", and a very close .250" (the tightest in the industry). So you can squeeze everything possible out of (or into) your design.

This surface-mount system utilizes a .050" contact grid in double row, polarized shrouded headers and receptacles, and offers our exclusive plated copper alloy holddowns . On standard .062" thick boards, the barbed holddowns do their job without protruding through, allowing surface mounting on both sides. And holddowns are soldered during reflow, providing long-term strain relief.

Dual-beam receptacle contacts and duplex gold plating provide high reliability, in selected sizes from 10 to 100 positions. Dimensional tolerances, reference datums, holddown characteristics, and packaging support robotic application; materials are fully compatible with IR and vapor phase reflow processing.

Ask us for more information on the AMPMODU 50/50 Grid Surface-Mount Connector System. Call the AMP Product Information Center at 1-800-522-6752 (fax 717-986-7575). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP

CIRCLE NO. 34

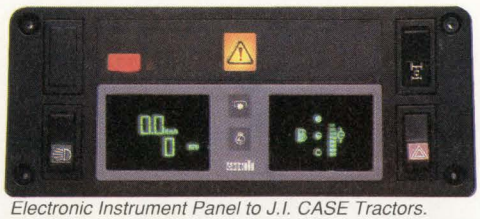
FUTABA

Sets the Standards in Custom Vacuum Fluorescent Displays and Vacuum Fluorescent Modules

CUSTOM DESIGN

Futaba is the leading global supplier of vacuum fluorescent displays and modules. We have the capability, technology, and market knowledge to provide you with the most cost effective display system tailored to your specific application.

Futaba's high brightness fluorescent display products range from simple numeric and dot matrix displays to large multi-color graphic panels.



Electronic Instrument Panel to J.I. CASE Tractors.

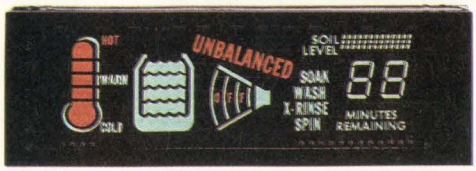
TECHNICAL SUPPORT

Futaba engineers have a broad range of application experience including automotive, point of sale, appliance, medical, and instrumentation products. They are ready to assist you in optimizing your display system design.

NCR "S1" Supplier.

U.S. MANUFACTURING

Futaba's state-of-the-art SMD manufacturing facility in Schaumburg, Illinois provides local service, JIT delivery, and reinforces its commitment to supply the North American market.



Appliance Control Display.

QUALITY

Futaba's number one commitment is supplying products having the highest level of quality. Quality begins with the initial design and is controlled throughout the manufacturing process by using SPC and having well trained and motivated employees.

Futaba is dedicated to the principal of continuous improvement and always strives to provide the highest level of customer satisfaction.

Pick up the phone - take advantage of our superior technical background and design expertise. Call or write for more information on Futaba custom vacuum fluorescent display modules.

FUTABA

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Schaumburg, IL 60173
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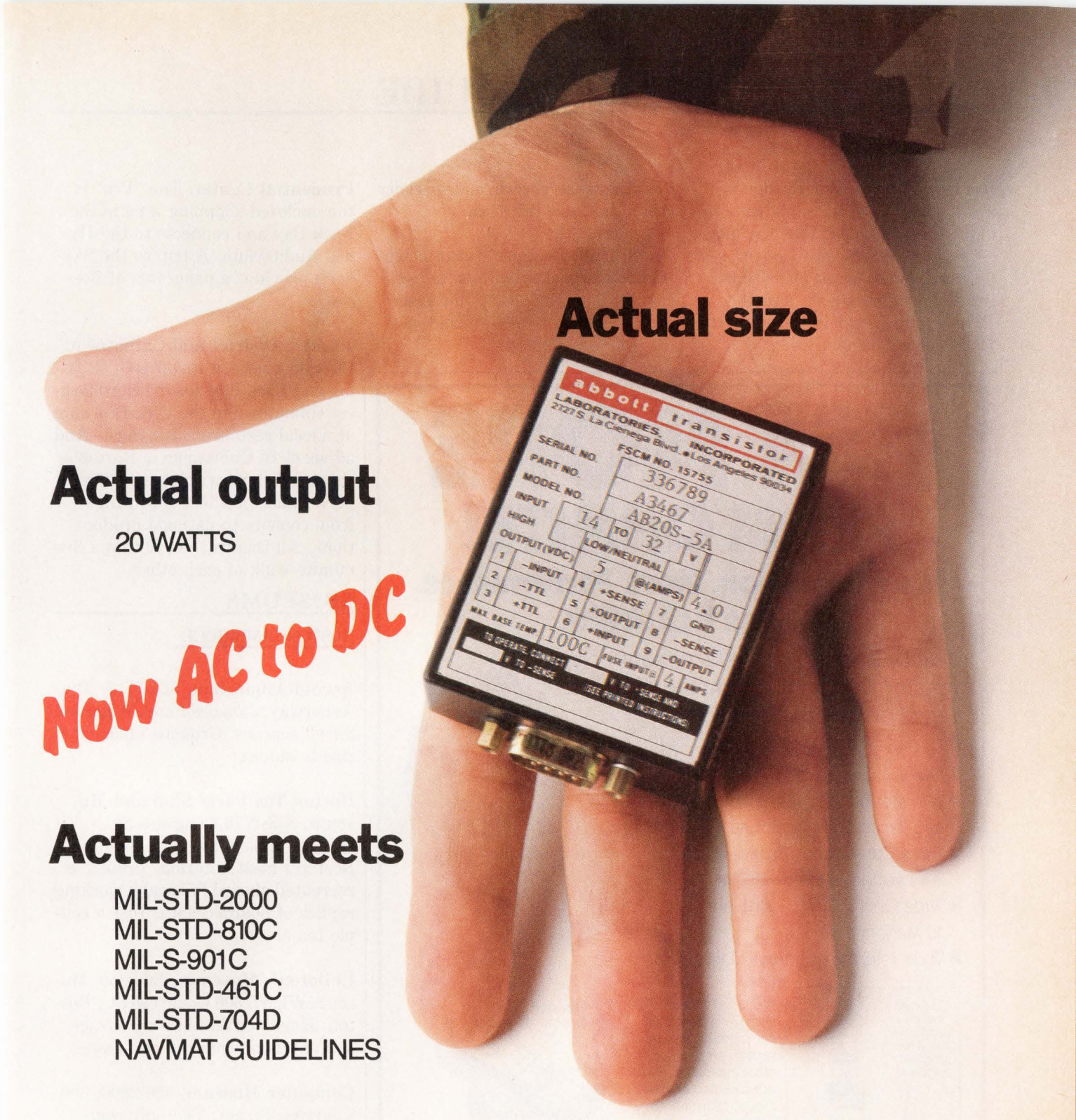
FAX 708-884-1635



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20 WATTS

Now AC to DC

Actually meets

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MIL-STD-810C
MIL-S-901C
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MIL-STD-704D
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Mil/Pac™ high-density military power supplies. Now you can order Abbott's full mil-qualified compact power supplies in both DC *and* AC input models.

Mil/Pacs come in 20W, 35W and 50W configurations, with single (5, 12, 15, 24, or 28V) or dual (±12V; ±15V) outputs.

DC-to-DC models accept input from 14V to 32V. AC-to-DC models accept 103.4 to 126.5V rms, 47-440 Hz single phase.

All Mil/Pacs operate at temperature extremes from −55°C to +100°C. All are designed with a field-proven topology that has been verified by rigorous environmental stress screening.

Mil/Pacs are available with or without MIL-STD-2000. Either way, the specs are worth reading. Just write us at 2727 South La Cienega Bl., Los Angeles, CA 90034. Or call (213) 936-8185.

abbott

WHEN RELIABILITY IS IMPERATIVE.™

CIRCLE NO. 36

Harvard Square: Where tomorrow's leaders are spending time today. Harvard University, the oldest in the country, has exerted a profound influence on the Square. Stroll down Brattle St. and Tory Row--where Longfellow lived in the 19th century, or go modern and visit the book, record, and specialty stores that dot the area.

North End: Boston's Italian neighborhood is packed with cafes, restaurants, and bakeries. In the summer, street festivals are held just off Hanover St.

Prudential Center: The "Pru" is the enclosed shopping area in the Back Bay and connects to the Hynes Auditorium. A trip to the Skywalk provides a panorama of Boston.

Theatre District and Chinatown: Nestled between Downtown Crossing and Back Bay lies the third largest Chinatown in the U.S. Dim sum at a local restaurant is a must. And adjacent to Chinatown is Boston's theatre district with seven different performance centers that range from comedy to national productions. All theatres are within a five minute walk of each other.

MUSEUMS

BOSTON/CAMBRIDGE

Arnold Arboretum, 524-1717, The Arborway, Jamaica Plain. A garden for all seasons. Grounds open sunrise to sunset.

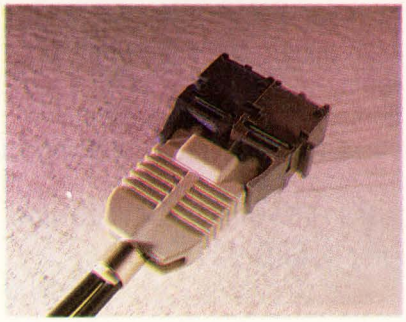
Boston Tea Party Ship and Museum, 338-1773,Congress St. Bridge, Museum Wharf, Boston. Boston's most notorious protest is recreated aboard full-scale, working replica of boarded ship. Toss a couple tea chests.

Children's Museum, 426-8855, Museum Wharf, 300 Congress St., Boston. Hands-on exhibits encourage and entertain children of all ages.

Computer Museum, 426-2800, 300 Congress Street. The only computer museum in the country featuring exhibits from historic to state-of-the-art equipment.

Institute of Contemporary Art, 266-5152, 955 Boylston St., Boston. The nation's oldest museum of contemporary art. The "Currents" program goes on.

HP's 50 MBd Plastic Fiber-Optic Data Links. Anything else would be twisted.



Our new data links are so fast and cost-effective, it would be crazy to stick with twisted pair.

Sure, optical fiber is immune to noise, but who can afford it? With HP's new high-speed plastic fiber links, the answer is anyone.

That's because our new links rely on plastic optical fiber cable which keeps costs way below glass fiber, while offering far greater voltage isolation and noise immunity than twisted pair wire.

A quick turn for the best.

With data rates soaring to 50 MBd, HP's plastic fiber links offer the fastest solution for designing computer, telecommunications, or industrial applications. So you can avoid bottlenecks, and design in data multiplexing.

Perfectly flexible.

You can choose interlocking horizontal or vertical mounts for greater mechanical design flexibility. The analog in/out provides the electrical design flexibility you need to meet your cost and performance goals.

The whole ball of wax.

What's more, as the largest optoelectronic supplier in the U.S., HP offers you the industry's most complete package of products and support services. To find out more about HP's 50 MBd Plastic Fiber-Optic Data Links, call **1 (800) 752-0900, ext. 2948** in the U.S.* You'd be crazy not to.

There is a better way.

HEWLETT PACKARD

*In Europe, FAX to: (49) 7031-14-1750.

CIRCLE NO. 37

A GIANT IN COMPUTERS, A WELL KNOWN MEDICAL FIRM AND A MAJOR TELECOMMUNICATIONS COMPANY HAVE ALL CHOSEN HUGHES FLEX CIRCUITS.

WHY?

Unless you're one of the above, you're probably surprised about this. Because we've been so busy expanding our efforts in commercial flex circuits we forgot to tell anyone.

We've been too busy delivering high speed, high density solutions like fine line with 2 mil spacing, and Gold Dot™, the highest density flex circuit interconnects on the planet. Too busy perfecting true high volume SPC manufacturing for six sigma quality. And far too busy producing products like single-sided, double-sided and multi-layer flex circuits with up to 24 layers. Plus, a variety of integrated assemblies.

And frankly, we plan to stay busy. So if you need unique flex circuit experience for everything from 3D electronic packages and multichip modules to semiconductor test heads and ABS braking systems, call Hughes. We'll send you the new Hughes Interconnect Systems brochure and show you what we're talking about.

Oh, about those companies we mentioned above. Did you ever get the feeling that there's a lot going on at Hughes you might not know about? We're ready to connect you to more than 25 years of flex know-how.

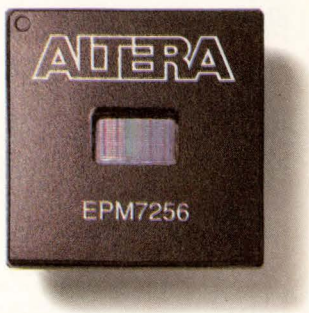
Call toll-free **1-800-821-2998**.

HUGHES

INTERCONNECT SYSTEMS DIVISION

Industrial Electronics Group

"When I think about density, a few things come to mind. For example, the Earth is the densest planet in our solar system–5.515 times denser than water. The most densely populated place on the densest planet is Macao, on the coast of China. 479,000 people in an area of 6.5 square miles. Hope they like each other. As for programmable logic, the award for the highest density goes to Altera's MAX 7000. With 1,000 to 20,000 usable gates. And more I/O than any other PLD family. Bye-bye masked gate arrays. That's as dense as it gets. Well, there is Rocko Miller, my old college roommate. 30-inch neck, crushed empty beer cans into his head. You know the type."



They're big. They're fast. They're everything you've asked for. Find out more big news. Call 800-800-7256. **MAX 7000**

BOSTON GUIDE

Isabella Stewart Gardner Museum, 566-1401, 280 The Fenway. A sumptuous Italian style palace which was built by Mrs. Gardner to house her collection. Renaissance & Dutch art, tapestries, sculptures, flowering courtyard, period furnishings.

Museum of Fine Arts, 267-9300, 465 Huntington Ave., Boston. From all there is to choose--and there is a lot--choose the Impressionist and post-Impressionist Room.

John Fitzgerald Kennedy Library, 929-4523, Columbia Point on Dorchester Bay, Boston. Trace the life of the 35th President through the use of photographs, memorabilia, tapes, and 30-minute film.

John Hancock Observatory, 572-6000. Copley Square, Boston. Take a peek from the top of the town.

Museum of Science, 523-6664, Science Park, Boston. Over 400 participatory exhibits range from astronomy to zoology.

New England Aquarium, 973-5200, Central Wharf,Boston. Over 200 species of aquatic life on display.

The Skywalk, 236-3318. Fiftieth Floor Observation Deck, Prudential Center, Boston. Experience Boston's only 360 degree panoramic view.

TOURS

SIGHTSEEING TOURS CUSTOM & GROUP TOURS

Bay Colony Historical Tours, 523-7303. JFK Post Office Box 9186 Boston, MA 02114

SIGHTSEEING TOURS/-REGULARLY SCHEDULED

BUSES

Greyline, Inc., 426-8805. Daily tours of Boston, Cambridge, Lexington, & Concord.

Trolley Tours of Boston, 269-7010, 329 West Second St., South Boston 02127. A one and a half hour tour of Boston aboard a modern trackless trolley. Departs hourly 9am-4:30pm. Also Cambridge tour available.

BOATS

Boston Harbor Cruises, 227-4320, One Long Wharf, Boston 02210. Call for times for the Constitution Cruise, Sightseeing Cruise and Sunset Cruise.

Swanboats. Every Spring and Summer since 1877 the Swanboats have sailed the Frog Pond in the Public Garden. Join the tradition of watching people watching you.

WALKING TOURS

Boston by Foot, 367-2345, 77 North Washington St., Boston 02114. Regularly scheduled walking tours highlight the architecture and history of Boston. Starts May.

Uncommon Boston, Ltd., 731-5854, 437 Boylston St., Boston 02116. A personal view of Boston's townhouses,gardens and galleries, private clubs, and libraries.

DINING

A—American Express
C—Carte Blanche
D—Diner Card
M—Master Card
V—Visa
$—Inexpensive (Most entrees less than $10)
$$—Moderate (Most entrees $10-$15)
$$$—Expensive (Most entrees $15-$20)
$$$$—Very Expensive (Most entrees over $20)

BOSTON/BROOKLINE

Another Season, 97 Mount Vernon St., 367-0880. For a romantic evening, take a stroll through the quaint streets of Beacon Hill to discover the delights of this restaurant. The diverse menu may offer anything, from squash with apple and curry soup to sauteed perch and ginger cheesecake. Open Tues-Fri, noon to 2pm, Mon-Sat, 6-10pm. (AMV) $$$

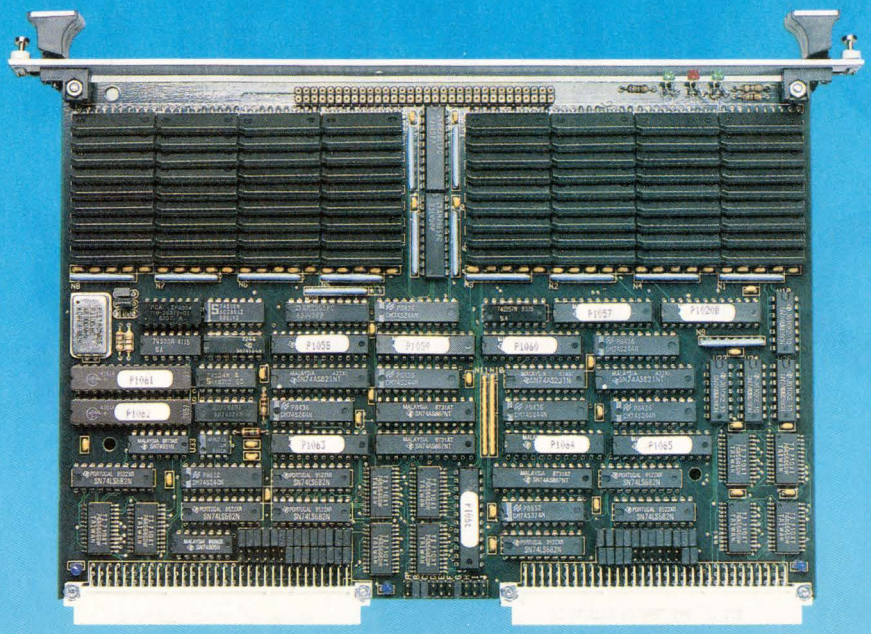
Anthony's Pier 4 Restaurant, 140 Northern Ave., 423-6363. Fine dining with outstanding views of Boston Harbor and the city's skyline. Menu combines fresh seafood with hearty New England fare. (ADMV) $$$

Atlantic Fish Company Restaurant, 777 Boylston St., 267-4000. Many varieties of fish with different preparations are offered. Also a raw bar and homemade chowder. (AMV) $$

Aujord'hui at the Four Seasons, 200 Boylston St., 451-1392. Formal dining with views of the Public Garden. Specialties include terraine of duck, foie gras, creamed wild mushroom soup, roasted smoked Maine lobster with crayfish fritters. Reservations recommended. (ACDMV) $$$$.

Back Bay Bistro, 565 Boylston St., 536-4477. Seasonal American Cui sine. (ACDMV) $$

40 MB/SEC DUAL-PORT VME/VSB MEMORY



CI-VME40

The CI-VME40 is the ultimate high-speed, high-capacity DRAM memory board with a dual-port interface to the VME and VSB Busses. The CI-VME40 is optimized for Block Transfer Cycles yielding a bus transfer rate up to forty megabytes per second. Chrislin is the only memory supplier to offer such an advanced and versatile dual-ported VME/VSB memory!

THE CI-VME40 FEATURES:

- 20ns write/20ns read ACCESS TIMES in BLOCK CYCLE
- 90ns write/140ns read ACCESS TIMES in SINGLE CYCLE
- 63ns write/83ns read CYCLE TIMES in BLOCK CYCLE
- 195ns write/195ns read CYCLE TIMES in SINGLE CYCLE
- 4MB, 8MB, 16MB, 32MB, 64MB in one VMEbus/VSB slot
- Byte Parity Error Detection
- Memory start and end addresses selectable on 256KB boundaries
- VMEbus and VSB memory start and end addresses configured independently

ALSO AVAILABLE FOR THE VMEBUS ARE...

THE CI-VMEmory FEATURES:

- Low-cost high-power VME memory with 4, 8, or 16MB
- VME Revision C.1 compatibility
- Lower and upper memory addressses independently selectable in 64K byte increments
- Byte Parity Error Detection with selectable trap on Parity Error
- On-board Control Status Register

THE CI-VSB-EDC FEATURES:

- Low-cost high-power dual-ported VMEbus/VSB EDC (Error Detection and Correction) memory
- 4, 8, 16, 32 or 64MB in one VMEbus/VSB slot
- VME Revision C.1 compatibility, VSB Revision C
- Lower and upper memory addressses independently selectable on 256K byte boundaries
- Single-Bit Error Detect and Correct, Double-Bit Detect

Chrislin Industries, Inc.
31312 Via Colinas, Suite #108, Westlake Village, CA 91362
TEL: (818) 991-2254 FAX: (818) 991-3490

Providing Top Quality Memory for Over 16 years!

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Soon, Eight Ho Computing Will

(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

Two standard dry-cell batteries. There's really nothing special about them. Aside from the fact that they can run a powerful, portable 386 computer for a full eight hours. Provided, of course, that portable is built around a low-voltage Am386™ microprocessor.

The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

Thanks to the low-voltage Am386 microprocessors, laptop, palmtop and notebook computer designs will become smaller, lighter, and more powerful than ever before.

With battery life of up to eight hours or more. That's a full day's worth of 386 performance—the per-

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BOSTON GUIDE

Bay Tower Room, 60 State St., 723-1666. A place to impress someone, maybe even yourself. Elegant dining 33 floors above the Faneuil Hall Marketplace with a view of Boston Harbor. Creative American and international cuisine using fresh regional ingredients. Dancing in the piano bar. Reservations required. Reduced rate parking in building. (ACDMV)$$$$

Bernardos, 24 Fleet St., 723-4554. One of the North End's best bets. Northern Italian cuisine featuring light wine sauces, rather than heavy tomato sauces. Delights include veal saltimbocca, shrimp marinara and a tortellini in cream sauce appetizer. This fairly small establishment serves beer and wine, only. A fine place for a romantic dinner or a party. (ACDMV)$$

Bertucci's 39-45 Stanhope St., 247-6161. Fire stoked ovens produce great pizzas. (MV)$

Biba, 272 Boylston St., 426-7878. Lydia Shire's new restaurant features food for the serious gourmet. (ACDMV)$$$$

Bnu, 123 Stuart St., 367-8405. Reasonably priced upscale Italian food. Spaghetti with grilled Italian sausage, small crisp pizzas, half roast chickens. The before-theater crowd meets here (AMV)$$

Brandy Pete's, 267 Franklin St., 439-4165. A popular spot for home cooking and afterwork cocktails. (MV)$

Bull & Finch Pub, 84 Beacon St., 227-9605. The inspiration for the television series, "Cheers" serves burgers, nachos and sandwiches. Downstairs from the elegant Hampshire House Restaurant. (ACDMV)$

Cactus Club, 939 Boylston St., 236-0200. A trendy restaurant serving southwestern food and delicacies. (AMV)$$

Cafe Budapest, 90 Exeter St., 266-1979. Top-notch fine dining specializing in Hungarian cuisine. Very attentive service. Warm and romantic dining amidst old world decor and elegance. Major credit cards accepted. $$$$

Cafe Fleuri, Hotel Meridien, 250 Franklin St., 451-1900. French-American bistro featuring a glass-roofed atrium. It's also a busy downtown favorite for business lunches. Dinner menu includes grilled lamb chops with garlic potato gratin; poached scrod; and pasta primavera. (ACDMV)$$$

Cafe Marliave, 10 Bosworth St., 423-6340. One of the best Italian Restaurants in the city and the best outside of the North End. The downstairs dining room features a cozy old world atmosphere with wooden booths that can make diners feel as if they're eating on the Via Venetro rather than in downtown Boston. Upstairs is a terrace-style dining room with balconies overlooking small sidestreets. Lasagna, veal scallopini, swordfish a la Columbo. (AMV)$$

Commonwealth Brewing Co., 138 Portland St., 523-8383. Near North Station this restaurant actually brews its own beer and ale on premises. Good appetizers, beer and steaks. Sports fans often gather here before a game at the nearby Boston Garden. (ACDMV)$

Cornucopia, 15 West St., 338-4600. Housed in a cozy building that Ralph Waldo Emerson frequented in the 18th century. Elegantly simple presentations. Menus change monthly. Located near Downtown Crossing, the restaurant prides itself in being "a sophisticated culinary adventure in the new American style". Reservations suggested. Adjacent parking is available. $$.

DuBarry, 159 Newbury St., 262-2445. Boston's oldest French restaurant. Traditional French cuisine, including escargot and Crepes Suzette. (ACDMV)$$

Durgin Park, Faneuil Hall Marketplace, 227-2038. Upstairs, New England favorites served in rooming house style by boisterous waitresses makes this place fun. Share a table, family style, with other patrons, sample fresh seafood, prime rib, Boston baked beans, Indian pudding and corn bread. Downstairs is good for a quick pint and a bowl of the creamiest chowder in town. No credit cards. Lines form for dinner. $$

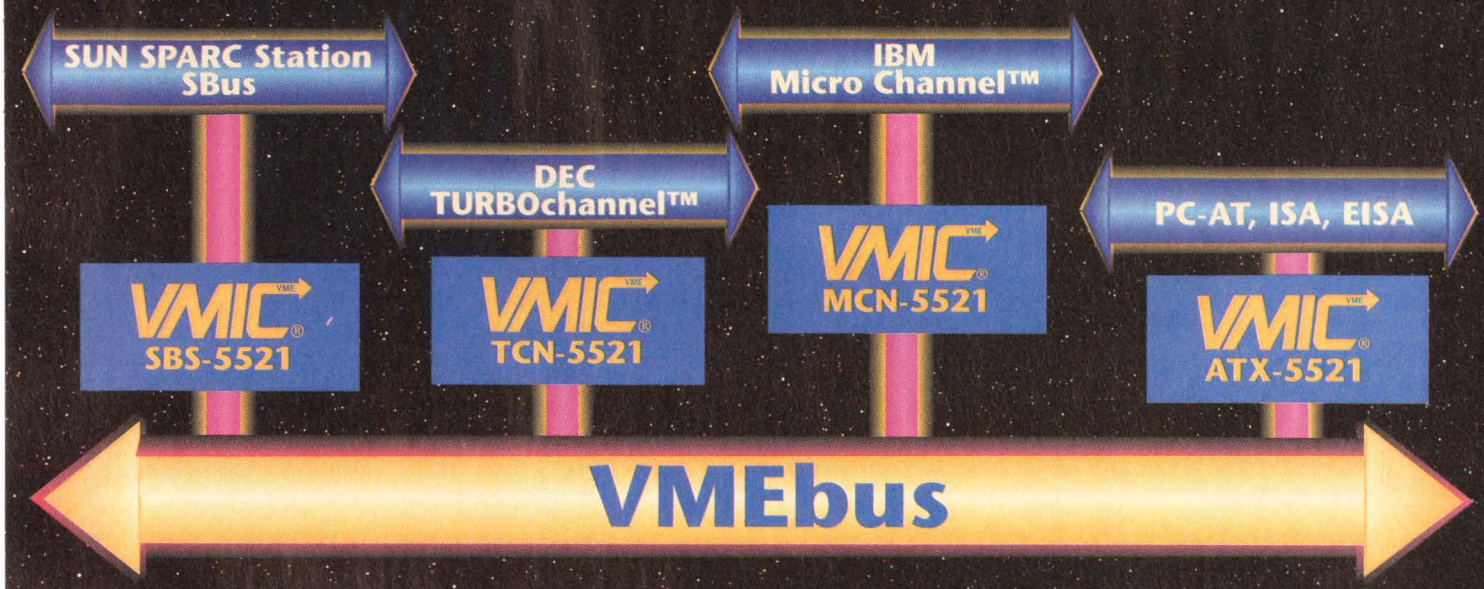
European, 218 Hanover St., 523-5694. A Boston favorite since 1917. Large North End restaurant divided into manageable rooms. Casual dining. Great pizzas! (ACDMV)$

Gyuhama of Japan, 827 Boylston St., 437-0188. A semi-formal, tranquil, beautiful oasis to enjoy authentic Japanese cuisine. (ADMV)$$

Hard Rock Cafe, 131 Clarendon St., 424-7625. The Massachusetts Institute of Rock. High priced hamburgers and sandwiches served in this rock 'n' roll museum chain. Major credit cards accepted. $

Hamersley's Bistro, 578 Tremont St., 267-6068. A terribly chic, cozy little black and white bistro in the South End. Cuisine includes braised rabbit, spicy hot sausage,

We Like to Illustrate How Well We Adapt



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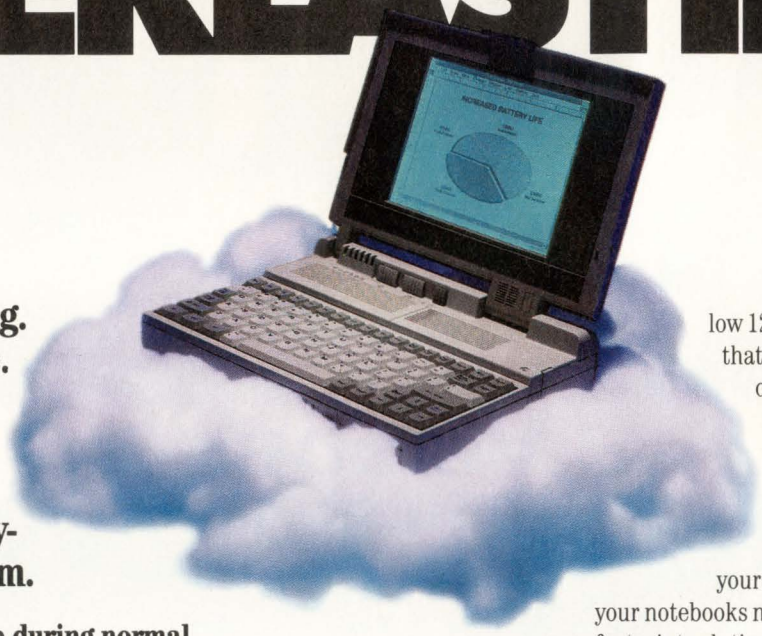

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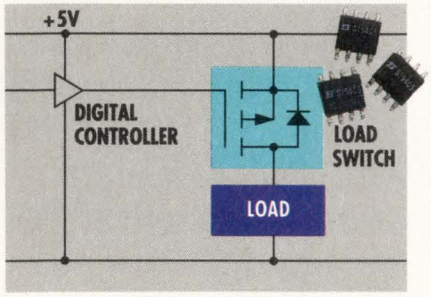

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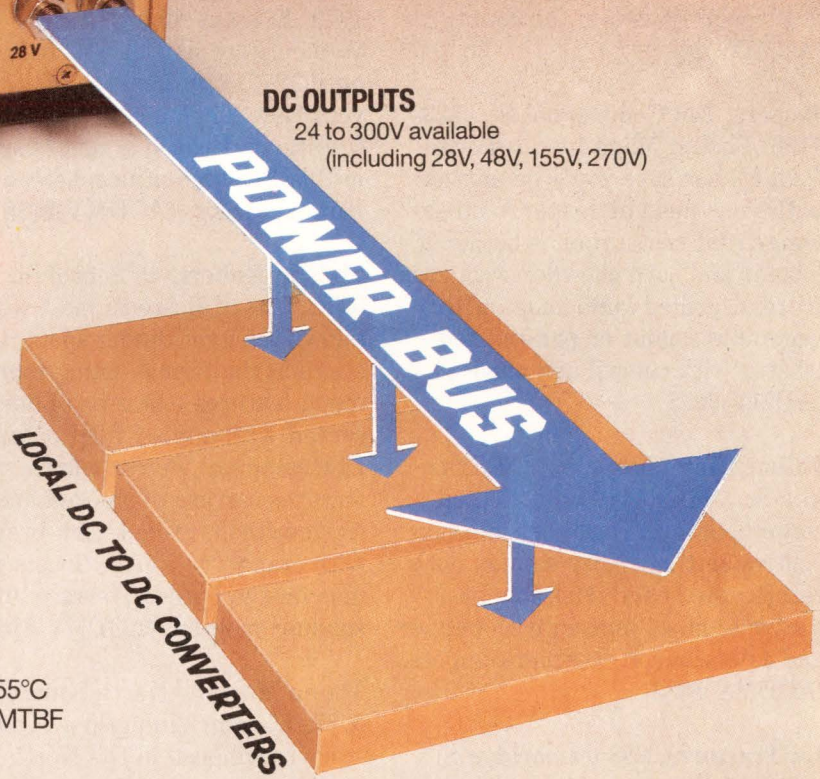

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CIRCLE NO. 44

chicken roasted with lemon and garlic and bouillabaisse. (MV)$$$$

Hampshire House, 84 Beacon St., 227-9600. Fine dining in a Beacon Hill mansion. Entrees include filet mignon, veal marsala, lobster. (ACDMV)$$$$

J. C. Hillary's Ltd., 793 Boylston St., 536-6300. Good steaks, fish specials, broiled breast of chicken. (AMV)$$

Jacob Wirth's, 31 Stuart St., 338-8586. Founded in 1868 this German beer hall style restaurant features hearty meals. Pork chops, pigs knuckles, ham, boiled bacon, herring. Has what may be the oldest draft beer system in the country. (ACMDV)$$

Jaspers, 240 Commercial St., 523-1126. Boston Magazine food critic Paul Fisher says you'll be amazed with your meal at Jasper White's waterfront restaurant, whether it's lobster and corn chowder with corn fritters, grilled lamb chops with vegetable ragout or pan-roasted lobster with chervil and chives. (ADMV)$$$$

Julien, Hotel Meridien, 250 Franklin St., 451-1900. Sophisticated contemporary French cuisine. Executive setting. Crisp salmon with sesame seeds and duck foie gras; sauteed loin of venison with pepper and a persimmon chestnut compote. (ACDMV)$$$$

La Trattoria, 288 Cambridge St., 227-0211. Small chef-owned Italian restaurant at the foot of Beacon Hill. Full range of Italian specialties and a good wine list. (ACDMV)$$

Legal Sea Foods, Park Plaza Hotel, 35 Columbus Ave., 426-4444. Very well prepared fresh fish. No reservations required but waits can be long. (ADMV)$$

L'Espalier, 30 Gloucester St., 262-3023. Posh Victorian establishment features tempting foie gras, sweet breads, venison loin, native pheasant, roast veal chop and lobster-truffle ravioli. The waiters will remind you of Buckingham Palace guards. Fixed price menu, either 50 odd dollars per person or 70 odd dollars per person. (MV)$$$$

Lafayette Swissotel, 1 Avenue de Lafayette, 451-2600. Cafe Suisse features New England cooking and traditional Swiss/Italian specialties. (ACDMV)$$$.

Locke-Ober's, 3 Winter Place, 542-1370. Elegant dining since 1875. Women were not allowed in here until 1970, but don't let that stop you. New England cuisine with a traditional French accent is served in this Brahmin atmosphere with baroque decor. (ACDMV)$$$$

Maison Robert, 45 School St., 227-3370. One of Boston's most well-known, elegant dining spots. Upstairs in the formal dining room the menu features foie gras of duck served with apples; fillet of lamb. Downstairs at Ben's Cafe the menu features tartare of smoked and fresh salmon; grilled duck breast with cranberry sauce. Guests may dine on the outdoor terrace during summer months. (ACDMV)$$$$

Mama Maria, 3 North Square, 523-0077. Elegant dining in a three-story townhouse in the North End, near Paul Revere's house. Gourmet Italian food served with a wide selection of fine wines. Accept most major credit cards. $$$.

Michael's on the Waterfront, 85 Atlantic Ave., 367-6425. Excellent, fresh seafood and other delicacies are served in this formal dining area, complete with book-filled bookcases. (ACDMV)$$$

Morton's of Chicago, One Exeter Plaza, 266-5858. Downstairs in the "Darth Vader" building (so named by critical architects of this black looming structure). This Chicago steakhouse chain has terrific Caesar salads and superb steaks as well as Maine lobster and fresh seafood. Valet parking available. (ACDMV)$$$$

No Name Restaurant, 15½ Fish Pier, 338-7539. Some of the freshest fish in Boston served in a family-style atmosphere. Located directly in the waterfront of Boston Harbor. $

Plaza Dining Room at the Copley Plaza Hotel, 138 St. James Ave., 267-5300. Enjoy contemporary French cuisine magically created by acclaimed chef, Philippe Reininger. Elegant atmosphere. Reservations accepted. (ADMV)$$$$

Ritz Carlton Main Dining Room, Ritz Carlton Hotel, 15 Arlington St., 536-5700. Superb service beneath chandeliers. Roasted rack of lamb, broiled scrod, veal chops, lobster in bourbon whiskey sauce. (AMV)$$$$

Rowes Wharf Restaurant and Cafe, Boston Harbor Hotel, 70 Rowes Wharf, 439-3995. Incredible view of the waterfront and Logan Airport. Elegant dining. A wide choice of fish as well as other specialties. (ACDMV) $$$$

Seasons, Bostonian Hotel, across from the Faneuil Hall Marketplace, 523-4119. Refined multi-level dining atop the Bostonian Hotel. The food not only looks beautiful it is scrumptious. Fresh, in-season ingredients are used. (ACDMV)$$$

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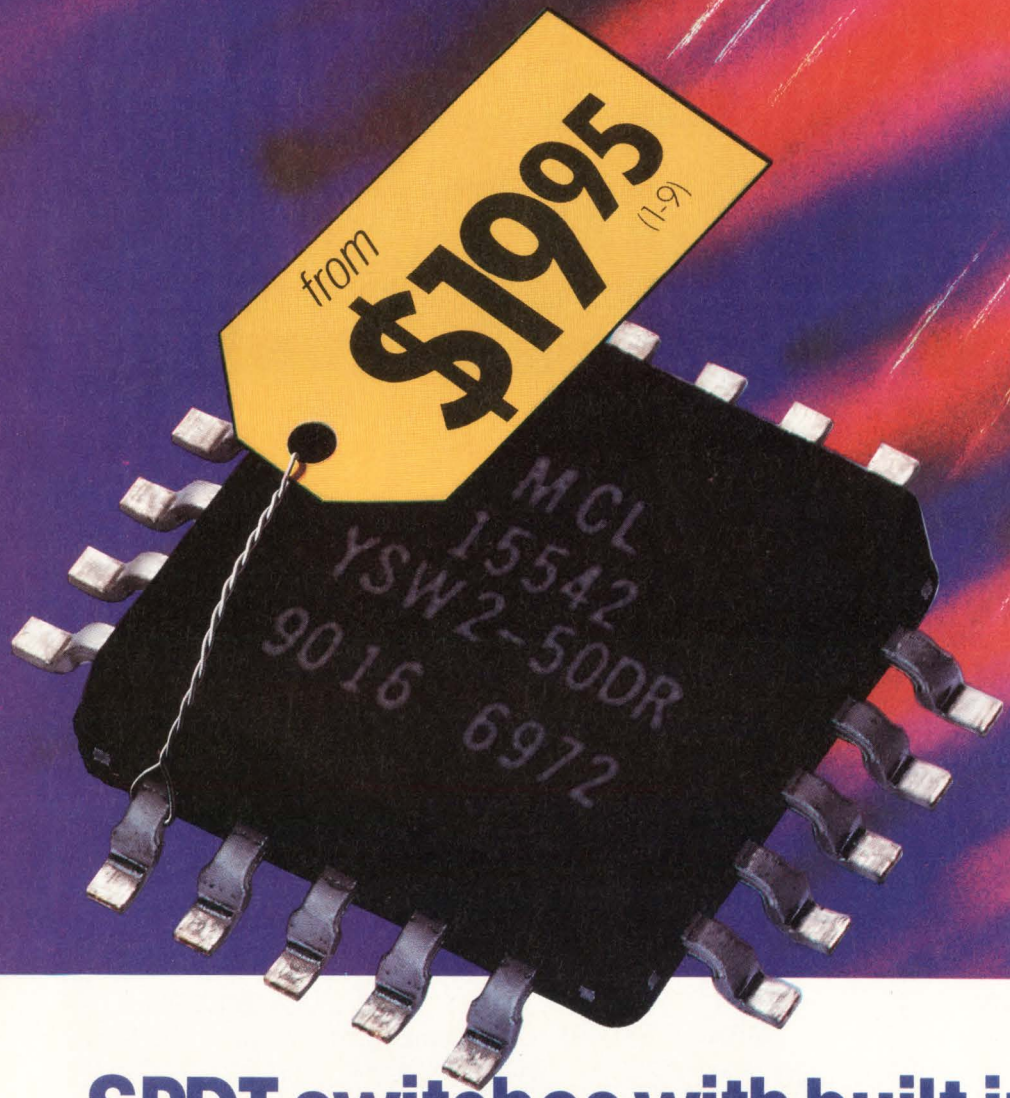

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Isolation (dB)	42	31	20	50	40	28
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RF Input (max dBm)	—	20	—	22	22	26
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BOSTON GUIDE

St. Botolph, 99 St. Botolph St., 266-3030. Continental cuisine in a charming, restored 19th century brick townhouse. Conveniently located behind the Colonnade Hotel, 3 minutes from Copley Place. Reservations recommended. (AMV)$$$

Union Oyster House, 41 Union St, 227-2750. Established in 1826 it is the city's oldest restaurant with continuous service. Famous patrons have included Daniel Webster and J.F.K., whose favorite booth is clearly marked with a plaque. Specializes in fresh seafood and other New England favorites. (ADMV)$$$

CAMBRIDGE

Acropolis, 1680 Mass Ave., 492-0900. Shishkebob and moussaka are featured at this Greek restaurant. (ACDMV) $

Border Cafe, 32 Church St., Cambridge, 864-6100. Cheap to moderately priced Mexican dining where the Marqueritas flow and the salsa flies amid the lines of customers waiting around dinner time. (AMV) $

Casa Mexico, 75 Winthrop St., 491-4552. A wide assortment of Mexican dishes are served in this restaurant that is adorned with hand painted wall tiles. (ACDMV) $$

Charlie's Kitchen, 10 Eliot St., 492-9646. Offer praise to Bacchus that such a tavern as Charlie's exists among the trendy settings of Harvard Square. The double cheeseburger special is the best deal in town. $

Coffee Connection, 36 JFK St., 492-4881.Sample a wide selection of international coffees while nibbling on light foods and desserts. (MV) $

Harvest, 44 Brattle St., 492-1115. Roast duck and grilled salmon highlight this restaurant's international menu. (AMV) $$$

La Groceria, 853 Main St., 547-9258. Once you're finished waiting downstairs, head for a table upstairs and order one of the homemade fettucini dishes. That's Italian. $$

Middle East Restaurant, 472 Mass Ave., 354-8238.Your only problem at this authentic Middle East setting is choosing among cous cous, tabouleh, falafel, kibbe, and kafta. $

The Regattabar, One Bennett St., Cambridge, 661-5000 or 864-1200. Talented jazz vocalists and groups play in this formal room at the elegant Charles Hotel. Adjacent to the hotel is an upscale shopping mall. (AMV)$$

T.T. the Bear's Place, 10 Brookline St., 492-0082.Three differently decorated dining rooms serve seafood dishes that include scallop pie, Maryland crab cakes, and fillet of sole. (AM) $$

33 Dunster St., 354-0636. The best salad bar in town is supplemented by burgers, quiche, and spinach lasagna. (ACDMV) $$

Upstairs at the Pudding, 10 Holyoke St., 864-1933.The dining room of Harvard University's Hasty Pudding Club adorned with a gallery of theatre posters and serving northern Italian fare. (AMV) $$$

NIGHTLIFE

BOSTON

The Boston Pops

The Boston Pops Orchestra's season runs from May 6, through July at Symphony Hall, Huntington Ave. at Mass Ave., 266-1492. The orchestra, made famous by the late Arthur Fiedler, is now conducted by John Williams. Williams has composed numerous movie scores including Star Wars and Born on the Fourth of July. Light classical to popular music is played. Table seats where refreshments are served are available. Tickets cost between $10 to $32.

Theater

Some plays hit the Boston area before heading for Broadway. They are usually held at the larger theaters such as:

Shubert Theater, 265 Tremont St., 426-4520
Wilbur Theater, 246 Tremont St., 423-4000
The Colonial Theater, 106 Boylston St., 426-9366

Some local theater companies include:

Huntington Theater Company, 264 Huntington Ave., 266-0800
Charles Playhouse, 74-76 Warrenton St., 426-5225.
American Repertory Theater at Harvard's Loeb Theater, 64 Brattle St., Cambridge, 547-8300.

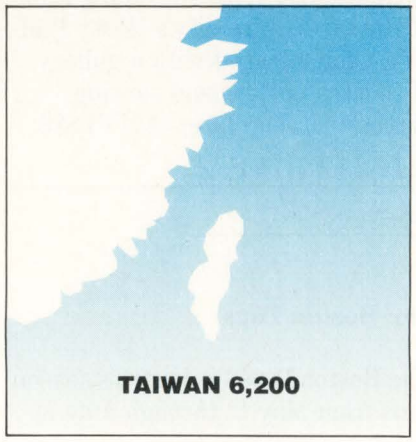
Tickets can sometimes be purchased at half-price, the day of the show, at Bostix, next to Faneuil Hall. They do not accept credit cards and all sales are final. Bostix is open Tuesday through Saturday, 11am to 6pm and on Sunday, from 11am to 4pm.

Comedy

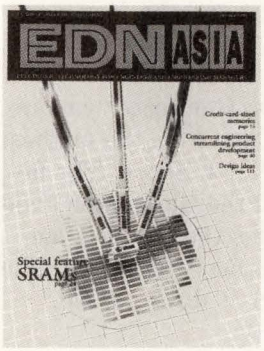
Boston recently experienced a comedy boom. Young local talent has prospered here for most of the past decade. Many of the comedians that

FOOD FOR

CIRCULATION CHART



THOUGHT



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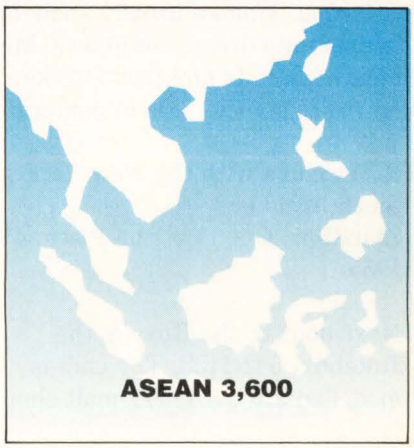


started in local clubs and restaurants here have gone on to stardom or at least an appearance on the Johnny Carson Show, including Steven Wright, Barry Crimmons, Lenny Clark and Jimmy Tingle.

Some outstanding talent can usually be seen at:
Nicks Comedy Stop, 100 Warrenton St., 482-0930
Comedy Connection, 76 Warrenton St., 426-6339
Stitches, 835 Beacon St., 424-6995
Catch a Rising Star, 30-B John F. Kennedy, Cambridge, 661-9887

Nightclubs

Bostonians are forced to start clubbing early because of a law that closes bars and nightclubs at 2AM. Still there are a myriad of places featuring a variety of musical entertainment to be seen.

The Roxy, 279 Tremont St., 227-7699. A formal nightclub for person of all ages. The New York style club is housed in the former Bradford ballroom and features a balcony, several bars, an adequately sized dance floor and a stage. On most nights a live swing band takes turns with a disc jockey who plays loud dance music. Sometimes a jazz singer accompanies the live band. The band plays for about 20 minutes and then the d.j. takes over for another 20 minutes. This goes on throughout the night. Dress here is formal. Women usually show up in elaborate dresses or gowns. Most men wear suits and ties. Drinks are on the expensive side of moderate.

Other clubs with the New York touch, include:
Zanzibar, One Boylston Place, 451-1955

Next door to the Roxy is the **Jukebox,** 542-1123. The club is modelled after a 1950's malt shop. Oldies from the 50's and 60's are played to an energetic crowd that make the dance floor sizzle. Draft beers are served in Coca-Cola glasses. Lines start to form here early on Friday and Saturday nights.

For some live rock music, which sometimes features raw local talent, check out:

Avenue C, 120 Boyston St., 423-3832. Usually open Thursday through Saturday, this hot spot features live bands and a disc jockey.

The Rat, 528 Commonwealth Ave., 247-8309 or 536-9438 concert line. For adventurous types, the Rat in Kenmore Square features blaring and sometimes bizzare avante guard groups. College crowd on the Bohemian side.

The Paradise, 967 Commonwealth Ave., 254-2052. Usually features nationally acclaimed rock groups playing in a dark setting.

For some good bar hopping, there is no place like Faneuil Hall. **Cityside,** in the center building, usually features live bands for a nominal fee. **The Purple Shamrock,** across the street from the flower shop in the marketplace, features Irish music as does the **Black Rose,** 160 State St. Explore!

BEYOND BOSTON

Lexington and Concord: These two towns, where the American Revolution broke out, are only a half hour to the west of Boston. Battle Green in Lexington is where men first shed blood in the colony's struggle against Britain. Concord shares in the revolutionary heritage but also contains the more serene Orchard House of Louisa May Alcott, Author's Ridge in Sleepy Hollow Cemetery, and Walden Pond--the site of Thoreau's famous cabin.

Marblehead and Salem: Out on Boston's North Shore, Marblehead is a yachting capital and sailor's paradise. Hanging in the Town Hall is the original painting of "The Spirit of '76". Salem is best known for its grisly executions of witches in the late 17th century, but also is host to the birthplace of Nathaniel Hawthorne and the House of Seven Gables.

Gloucester: At Gloucester you are approaching Cape Ann, the furthest point on the North Shore. The famous statue of the Gloucester Fisherman overlooks the ocean, a memorial to fishermen lost at sea. The coastal scenery is unsurpassed.

Plymouth: Thirty nine miles south of Boston is Plymouth, where the Pilgrims landed in 1620. Historic Plymouth Rock is here along with the Mayflower II, a full scale replica of the vessel that carried the Pilgrims to the New World. A little further south is Plymouth Plantation, a reconstruction of the Pilgrims' village as it appeared in 1627.

New Bedford: This old whaling town remains true to the sea. The large Portuguese community continues to fish for a living. The Whaling Museum features original whale boats, harpoons, and exhibits that stir memories of Ahab and the White Whale.

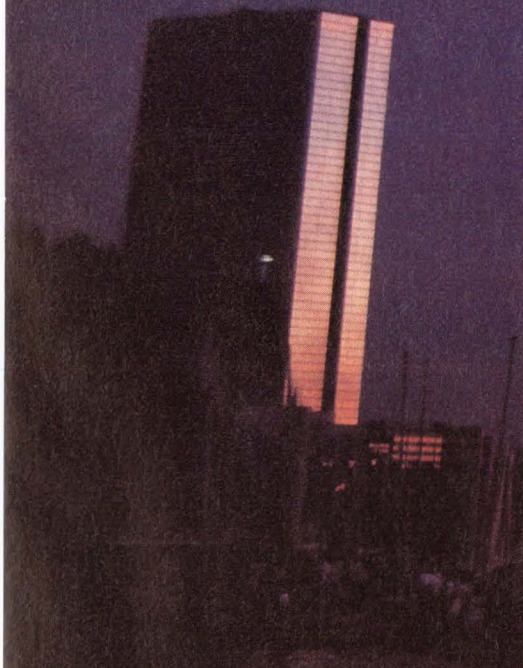
Cape Cod: Fifty seven miles south of Boston is a flat, narrow, sandy, elbow-shaped peninsula affectionately known as "the Cape". An area unspoiled by industry and almost entirely residential that caters to the tourist. Carouse in crowded Hyannis or stroll stretches of beach near Provincetown in near solitude. From the Cape you can cruise to Martha's Vineyard or Nantucket.

ELECTRO'92

BOSTON

Focusing on the needs of design engineers, Electro/92 will offer more than 60 technical sessions and 800 exhibits. Technical courses and management seminars round out the program.

Dave Pryce, Technical Editor



THE CITY OF BOSTON, noted for its cultural and historical attractions, will host Electro/92 on May 12, 13, and 14. This year, all Electro events will be held at the Hynes Convention Center, which is located on Boylston Street adjacent to the Prudential Center in downtown Boston.

The theme of Electro/92 is "New Directions in High-Tech Innovation." In keeping with this theme, and in response to the increasing significance of software innovation, this year's show will feature several sessions on software in engineering. You'll be exposed to the most current software programs and methods, and be able to meet the experts at the forefront of software development.

Helping to kick off Electro/92 will be Jim P. Manzi, president and CEO of Lotus Development Corp. Manzi will deliver the keynote address, entitled "Networks and Mobile Users: Personal Computing in the 90s." The keynote program will take place at a luncheon at noon, Tuesday, May 12, in the Hynes Convention Center. Tickets are $25.

Following the keynote luncheon, IEEE life members are invited to attend the seminar on

Photography by Kevin Bryan

"The Father of Radio: E H Armstrong." Professor William Siebert, Ford Professor of Engineering at MIT, will deliver the talk at 2:30 pm in the Hynes Convention Center.

In addition to the focus on software engineering, Electro/92 includes more than 50 other technical sessions (see **table**). The categories for these sessions are

- Concurrent-engineering methodologies
- Concurrent-engineering technology
- Semiconductor-device technology
- Manufacturing, quality, and reliability
- Engineering and technical education
- Going international
- Current topics.

Complementing the technical sessions are several conferences, technical short courses, and management seminars. An all-industry

Electro/92 technical-session schedule

Day/time	Concurrent-engineering methodologies	Concurrent-engineering technologies	Semiconductor device technology	Manufacturing, quality, and reliability	Software engineering	Engineering and technical education
Tuesday May 12, 1992 9:15 am to 11 am		**Session 1** New trends and techniques in system-level verification	**Session 2** Model availability and how we achieve it	**Session 3** Total-quality-management trends	**Session 4** A re-engineering process for large software systems	**Session 5** Competitive engineering methodology
1 pm to 2:45 pm	**Session 8** Expert-system development and application	**Session 9** TCAD for total quality control	**Session 10** Modern solid-state microwave design	**Session 11** Customer-driven product design	**Session 12** Software-engineering process trends and overviews	**Session 13** Restructuring the engineering resource for the 21st century
3:15 pm to 5 pm	**Session 16** Knowledge-based engineering/expert systems	**Session 17** Impact of integrated-component information management	**Session 18** Building design-for-test into your ASICs	**Session 19** Supportability-assessment systems and model-development environments	**Session 20** Software reliability engineering	**Session 21** Systems for keeping world-class engineers up to date
Wednesday May 13, 1992 9:15 am to 11 am	**Session 24** Product data sharing using STEP	**Session 25** Innovations in CAD for electromechanical design	**Session 26** FPGAs—Where is the industry going?	**Session 27** Design-to-cost	**Session 28** Object-oriented design	**Session 29** Education for total quality management
1 pm to 2:45 pm	**Session 32** ECAD frameworks: standardization in the marketplace	**Session 33** PC-board technology trends	**Session 34** FPGA design technology enhances design productivity	**Session 35** SMT processing	**Session 36** Software development and applications using object-oriented and other technologies	**Session 37** Software education for open systems
3:15 pm to 5 pm	**Session 40** Improving the design process—the best of theory and practice	**Session 41** Computer-aided-design tools for solid-state-device development	**Session 42** Programmable architectures	**Session 43** An approach to building distributed applications on the plant floor	**Session 44** Software re-use issues	**Session 45** Career planning for the 1990s
Thursday May 14, 1992 9:15 am to 11 am	**Session 48** Managing concept-to-commercial-ization cycle time: opportunities and expectations	**Session 49** Concurrent engineering in ASIC design	**Session 50** Multichip modules			
1 pm to 2:45 pm	**Session 53** Concurrent engineering	**Session 54** Current issues in thermal management	**Session 55** Cache-memory design: what's new?			
3:15 pm to 5 pm			**Session 58** Specialty memory: applications and innovations			

Admission to technical sessions and exhibits is complimentary.

*Sessions 7 and 39 require special registration.

conference, titled "How the Northeast Can Grow in the World Marketplace," will be held Tuesday, May 12, from 9:15 to 11:00 am. Tickets are $20. A purchasing conference, titled "Teambuilding: The Ultimate Vendor," will be held Wednesday, May 13, from 1:00 to 2:45 pm. Again, tickets are $20.

The technical short courses include full-day seminars on such topics as programming with the X-Window system, the Demeter method for object-oriented design, surface-mount technology, use of Spice for modern analog simulation, and concurrent engineering. The cost of these technical courses ranges from $300 to $400.

The management seminars feature idea-generating topics such as project management, doing business with the Japanese, and preparing and delivering effective presentations. These seminars cost $300 each. The technical short courses and the management seminars will be held on Monday, May 11, from 9 am to 5 pm.

Exhibits abound

Engineers attend Electro as much for the diverse exhibits as for the technical sessions and other programs. Perhaps nowhere else can an engineer gain as much knowledge of available products as in the aisles of these exhibits.

	Going international	Current topics
	Session 6 Global engineering	**Session 7*** All-industry conference
	Session 14 Government support to international trade	**Session 15** Super glue: high-speed logic for the 1990s
	Session 22 European perspective: overview of Europe on becoming a single market	**Session 23** Current topics in medical electronics
	Session 30 Avoiding legal landmines in global marketing strategies	**Session 31** Getting started: the right steps in starting and growing your own high-tech company
	Session 38 Third-world manufacturing	**Session 39*** Purchasing conference
	Session 46 International finance	**Session 47** Marketing in Asia
	Session 51 Specs and standards go international	**Session 52** Recent developments in high-performance storage batteries
	Session 56 Forming international relationships	**Session 57** Energy management from utility to customer
	Session 59 The use of on-line resources for scientific, technical, and marketing research	

Traveling to Electro

The site of this year's Electro show is the Hynes Convention Center, located at 900 Boylston Street adjacent to the Prudential Center in the Back Bay section of Boston.

From the west, you can reach the Convention Center by taking the Massachusetts Turnpike (Route 90) to the Prudential Center exit.

From Logan Airport and points north, take Route 93, which runs north and south through Boston, to the Storrow Dr exit at Copley Square. Turn right on Beacon St, left on Massachusetts Ave, and left on Boylston St.

From the south or east, take the Southeast Expressway (Route 93/3) to the Massachusetts Ave exit. Continue on Massachusetts Ave to Boylston St.

Park 'n ride locations

To avoid the rush-hour traffic and to address the limited parking available in downtown Boston, four park-and-ride locations will operate Tuesday through Thursday, May 12 to 14. You can park in one of three suburban locations and take the free Electro shuttle to the Hynes Convention Center.

The shuttle location for the north is the Showcase Cinema in Woburn; for the west, Shoppers World in Framingham; and for the south, the Showcase Cinema in Dedham.

Shuttle buses will leave at 20-minute intervals from 7:40 to 9:00 am and return from the Convention Center from 4:00 to 5:30 pm on Tuesday and Wednesday and 3:00 to 4:30 pm on Thursday.

Bayside parking

"In-town" parking will be available at the Bayside Expo Center in Boston. The cost to park will be $5. Shuttle service to the Hynes Convention Center will run from 8:30 am to 5:30 pm and will operate at 20-minute intervals most of the day.

You can reach Bayside from the north or south by taking exit 15 from Route 93/3. From the west, take the Massachusetts Turnpike east until it merges with the Fitzgerald Expressway and Route 93 in Boston; follow the signs to Route 93 South.

Electro/92

Nearly 400 manufacturers will display products ranging from components, hardware, and semiconductors to CAD/CAE tools, test equipment, power supplies, and production equipment.

Exhibits will be open from 9 am to 5 pm on Tuesday and Wednesday (May 12 and 13), and from 9 am to 4 pm on Thursday, May 14. Registration at the door is $5 for IEEE members and $10 for nonmembers. However, if you bring a complimentary registration form with you to Electro, you'll receive free admission to the show. Registration will be located on the second floor of the Hynes Convention Center.

Digital Equipment Corp has invited Electro/92 attendees to DECWorld '92, which is being held at Boston's World Trade Center from April 27 through May 15. DECWorld will present a line-up of personal computing and supercomputing products. The exhibits will highlight new services and business practices and will feature advanced business applications available from DEC and hundreds of its business partners.

Electro attendees will be able to register for specially scheduled tours at the DECWorld booth in the Hynes Convention Center. Bus transportation will be available between the Hynes Center and the World Trade Center.

With its wealth of historical attractions and its notably good food and entertainment, Boston is always a favorite spot for Electro visitors. After a full day of attending technical sessions and visiting the exhibits, you can relax and enjoy the best that the city has to offer. EDN

Dave Pryce, Technical Editor, can be reached at (617) 558-4326; FAX (617) 558-4470.

Article Interest Quotient
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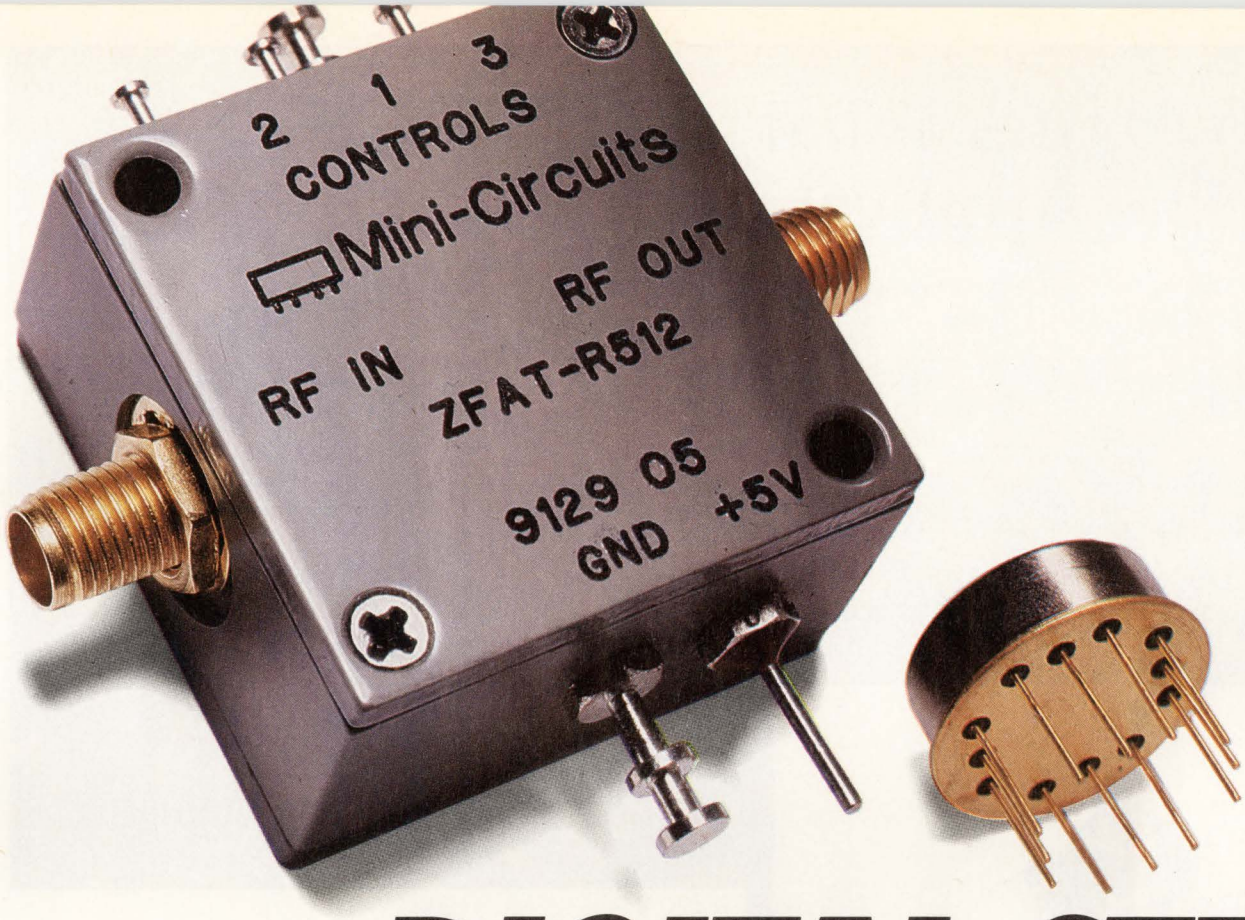

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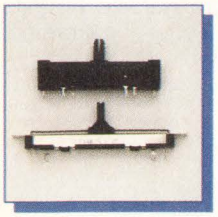
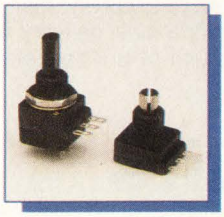
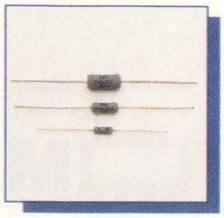


Slide Potentiometers



Modular Potentiometers

Trimmer Series



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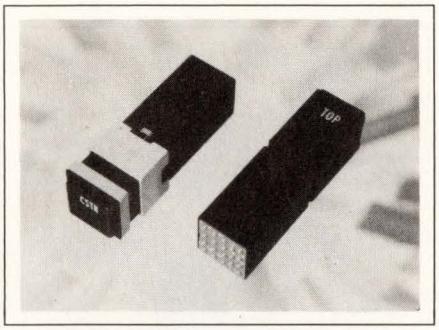


Lighted Pushbutton Switches

The Series 584 lighted pushbutton switches includes an extended-capsule model that provides a 75° cone of vision. Other models are a rod-mount model that permits gang-mounting into small panel openings and a termination system that permits easy assembly and disassembly of wires. The 5/8-in. switches and indicators have an 8A rating. Matrix-mount switches accept poke-home terminals conforming to the MIL-C-39029/57-354 standard. Options include RFI/EMI protection, drip- or slash-proof seals, switch guards, and spacers for light-plate thicknesses. $95 to $285 (1000).

Eaton Corp, Aerospace and Commercial Controls Div, 4201 N 27th St, Milwaukee, WI 53216. Phone (414) 449-7326. Booths 2233 and 2235. **Circle No. 400**

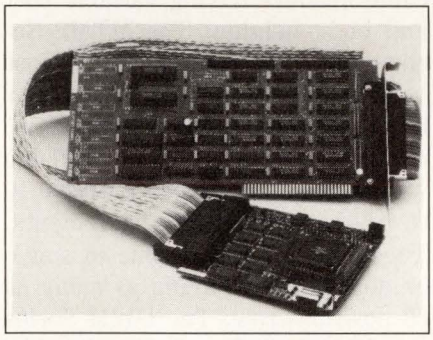
Fine-Pitch Sockets

The Socket/Adapter System lets you temporarily surface mount a quad flatpack (QFP) on a pc board. The lower portion of the socket surface mounts to a footprint pattern of the QFP via a gull-wing lead frame. The upper portion of the socket, which houses the QFP device, connects to the lower assembly. When the QFP device no longer requires a socket, you can surface mount the device directly to the board without redesign costs. The unit accepts any QFP having lead pitches of 0.025 in. or less. Units are available for 100-, 128-, 132-, 164-, 196-, and 208-pin devices. 100-pin unit, $272.

Advanced Interconnections Corp, 5 Energy Way, West Warwick, RI 02893. Phone (401) 823-5200. FAX (401) 823-8723. Booths 3412 and 3414. **Circle No. 401**

In-Circuit Emulator

The Emul16/300-PC is an in-circuit emulator for Motorola's 16-bit 68HC16 and 32-bit 68300 μCs. The emulator consists of an ISA bus plug-in board, a 5-ft twisted-pair ribbon cable, a pod board, and an optional trace board. The software runs under Windows 3.0, which lets



you monitor several functions at the same time. For example, you could link the contents of a shadow-RAM to an Excel cell while the emulator is running at full speed. The emulator provides real-time emulation at 16.78 MHz. The pod board has 256 kbytes of emulation RAM, and the ISA bus board has 1 Mbyte of shadow RAM that writes to both external and internal memory at full speed. $1995.

Nohau Corp, 51 E Campbell Ave, Campbell, CA 95008. Phone (408) 866-1820. FAX (408) 378-7869. Booths 5403 and 5405.

Circle No. 402

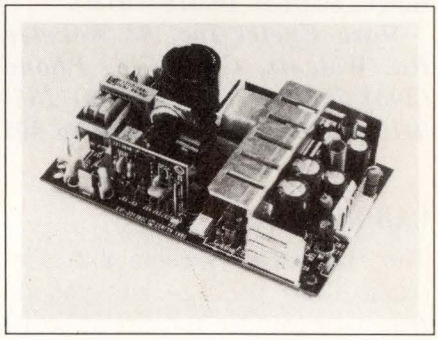
Universal Programmer

You can use the BP-1200 universal programmer to program EPROMs, EEPROMs, bipolar PROMs, PLDs, and all microcontrollers. The unit can change the voltage on any pin, which eliminates the need for DACs. The programmer weighs less than 6 lbs and measures 9.56×6.75×3 in. You can choose among versions with 32-, 40-, or 48-pin driver cards; all versions come with a 48-pin ZIF DIP IC socket. The universal SMT-84 surface-mount socket accepts 20- to 84-pin plastic leaded chip carriers and small-outline packages. BP-1200/32, $2500; BP-1200/40, $3000; BP-1200/48, $3500. SMT-84 surface-mount socket, $750; individual plastic-leaded-chip-carrier sockets, $90.

BP Microsystems Inc, 10681 Haddington Dr, Houston, TX 77043. Phone (800) 225-2102; (713) 461-9430. Booth 1106. **Circle No. 403**

Switching Power Supply

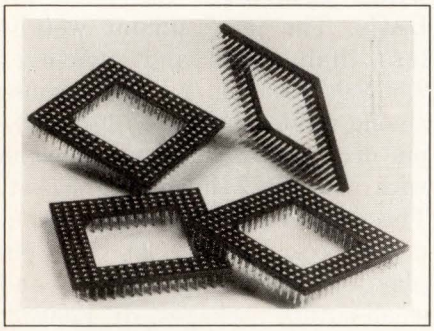
The ZPS-45 switching power supply operates with a single-phase 85 to 265V ac or 120 to 364V dc input voltage. The unit provides 40W max using convection cooling and 45W max using air-flow cooling. The triple-output unit supplies 5V dc at 5A; 12V dc at 2A; and −12V dc at 0.7A. The 5V output has a



±3% load regulation. The ±12V outputs have ±5% load regulation. The supply resides on a 3×5-in. pc board and has a 1.25-in. profile. The supply meets FCC Part 15J Class B and VDE 0871/B EMI emission standards and has a 100,000 MTBF. $55.

Zenith Magnetics, 1000 Milwaukee Ave, Glenview, IL 60025. Phone (708) 391-8510. FAX (708) 391-7078. Booths 1101 to 1105.

Circle No. 404



PGA Sockets

The Series MD cold-formed pin-grid-array (PGA) sockets come in five grid sizes ranging from 11×11 to 17×17 pins. The sockets have 68 to 168 pins. Seamless BeCu contacts require a typical insertion force of 1.5 oz. Molded standoffs and a liquid-crystal-polymer insulator allow vapor-phase or IR soldering. A cold-form sleeve prevents solder wicks from forming in the contact area. Features include 10-mΩ contact resistance, 3A contact rating, 2-pF contact-to-contact capacitance, 1×10^6-MΩ insulation resistance, 1000V ac (rms) dielectric withstanding voltage, and a −55 to +125°C operating temperature range. $0.01 to $0.018 (OEM).

Marc Eyelet Inc, 63 Wakelee Rd, Wolcott, CT 06716. Phone (203) 756-8847. FAX (203) 755-9410. Booth 4318. **Circle No. 405**

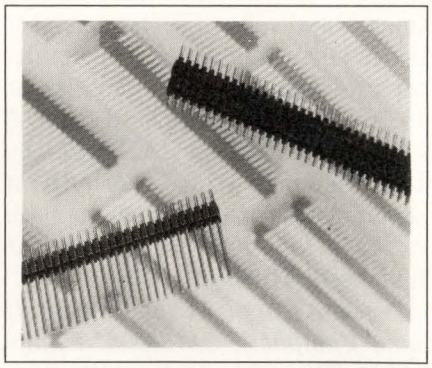
CAD Software

The HiWire II Version 2.2 electronic CAD package lets you do schematic capture and circuit-board design. A menu-driven executive program automatically organizes projects and files. A graphical editor uses a single pull-down menu, which contains frequently used commands. You can draw schematics and circuit-board drawings having as many as 200 ICs within the 640-kbyte MS-DOS limit. In addition, the editor supports 32 Mbytes of expanded memory and 15 Mbytes of extended memory for more complex designs. The drawing grid can be in inch or millimeter scales. A utility for rubber bands and rats nests simplifies both editing and placement. Two autorouters feature 1-mil resolution and support buried and through-hole vias. From $995 to $2395.

Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; (317) 742-8428. FAX (317) 448-4823. TLX 709079. Booth 1216. **Circle No. 406**

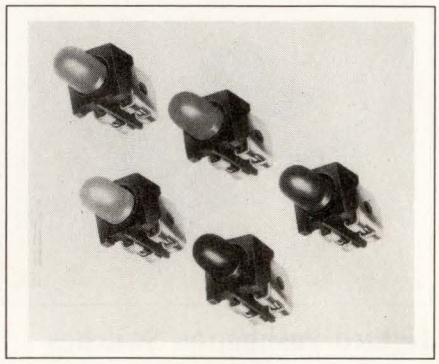
Terminal Strips

The company has expanded its line of 0.05-in. microconnectors to include headers having variable post and body heights. The MTMS Series lets you order custom post heights without long lead times or minimum orders. The 0.05×0.10-in. centerline terminal strip is available with post heights ranging from 0.10 to 0.605 in. in 0.005-in. increments. The terminal strips come in single or double rows having as many as 50 positions/row. The DWM Series provides flexibility in board stacking. The 0.05×0.10-in. terminals permit board spacings of 0.38 to



0.92 in. when they mate with the company's SLM and SMS Series socket strips. Plating options and a variety of lead styles are available for both series. MTMS and DWM Series, from $0.028 and $0.031 per pin, respectively.

Samtec Inc, Box 1147, New Albany, IN 47151. Phone (800) 726-8329. FAX (812) 948-5047. Booth 3322. **Circle No. 407**



Surface-Mount LEDs

The SMT LEDs are a line of T-1 and T-1 3/4 surface-mount LEDs. The LEDs are available in five colors—red, green, amber, yellow, and blue. Bicolor (red/green) LEDs are also available. The units withstand IR and vapor-phase mounting and have standoffs to ease cleaning solder flux. The LEDs mount at right angles to the board and have built-in resistors for 5 or 12V operation. A black-molded housing meets the UL 94V-0 rating. Solder-coated terminals employ a self-aligning 6-point attachment to ensure electrical and mechanical integrity. The units come in antistatic tape and reel packages that conform to EIA 481 specifications. From $0.78 (1000).

Industrial Devices Inc, 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. FAX (201) 489-6911. Booth 1430. **Circle No. 408**

Arc Suppression Networks

The Type LNEM metalized-polyester suppression network suits arc-suppression and snubber applications. The network provides a series-connected capacitor and resistor in a single component. Laser-produced patterns create 60 to 1000Ω resistors that dissipate 0.5 to 2W. Capacitance is 0.1 or 0.5 μF (±20%), rated for 600V dc or 250V ac. The unit has been tested to withstand one billion 330V peak-to-peak pulses. The axial-lead networks are available in bulk quanti-

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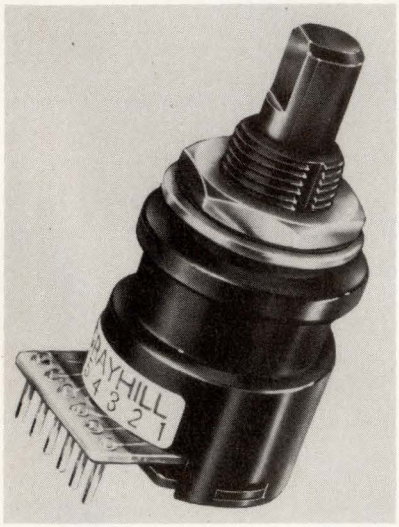
Aerovox, 742 Belleville Ave, New Bedford, MA 02745. Phone (508) 999-1000. FAX (508) 990-8696. Booth 2221. **Circle No. 409**



Optical Rotary Encoder

The Series 61 optically coupled rotary-encoder switch provides two quadrature encoded output signals. The switch produces the output signals by interrupting a light beam or allowing light to fall on a pair of phototransistors. Because there are no metal-to-metal contacts, the switch's rated lifetime is one million cycles of operation. An integral pushbutton switch lets you set the 2-bit output code for a desired setting. $10.50 (100).

Grayhill Inc, 561 Hillgrove Ave, LaGrange, IL 60525. Phone (708) 354-1040. FAX (708) 354-2820. Booths 3504 and 3506. **Circle No. 410**

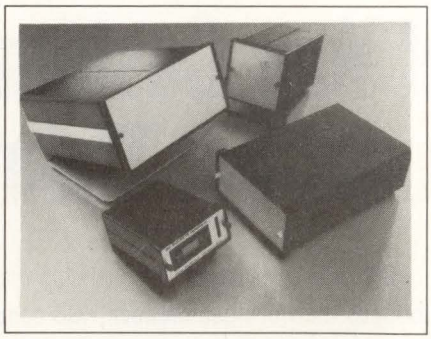
Switching Power Supplies

The MSC Series includes 350, 400, and 750W triple-output and a 400W dual-output switching power supplies. The supplies power multiple synchronous disk-drive systems. Each supply can maintain 1% regulation on the 12V line when powering as many as 16 disk drives. The 350 and 400W triple-output units deliver 35A from a primary 5V output and 26A peak from secondary ±12V outputs. The 750W unit delivers 120A from 5V, 27A from 12V, and 6A from −12V. The 400W dual-output unit has input and output connectors instead of standard barrier strips. The dual-output unit delivers 20A at 5V and 25A from 12V. An autorange option automatically selects a 115 or 230V ac range. $300 to $500.

Todd Products Corp, 50 Emjay Blvd, Brentwood, NY 11717. Phone (800) 223-8633; (516) 231-3366. FAX (516) 231-3473. Booths 5308 and 5310. **Circle No. 411**

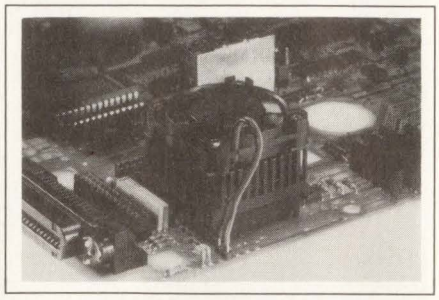
DIN Enclosures

The E Series DIN-standard enclosures are available in a black wrinkle-finish powder coat. The enclosures are made from extruded aluminum shapes that lock together to create rectangular or square enclosures of any length. Standard units are 6- or 8-in. deep and have integral grooves that are 0.08-in. wide on



0.2-in. centers. The spacing lets you mount boards vertically or horizontally. Side bars lock the units in place when you mount them in a panel. The enclosures have a PVC vinyl-coated tilt handle. A 44×91-mm, 6-in.-deep case, $16.05 (25).

Buckeye Stamping, 555 Marion Rd, Columbus, OH 43207. Phone (614) 445-8433. Booths 4404 and 4406. **Circle No. 412**



PGA Cooling Modules

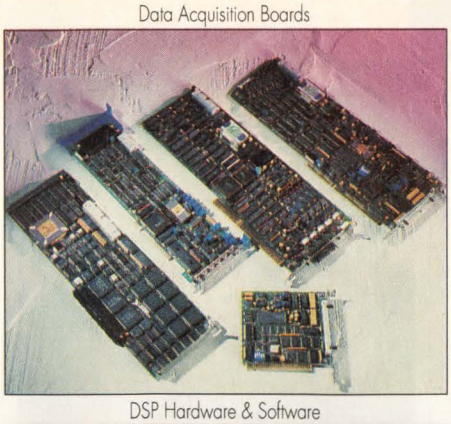
The Thermalloy Cooling Modules consist of a pin-fin heat sink and a brushless dc fan. The five standard modules cool Intel's i486, i860, i960, Advanced Micro Devices' Am29000, and Motorola's 68040 μPs. The units also fit on pin-grid arrays (PGAs) having 15×15, 17×17, 18×18, or 21×21 pins. You can select a 5 or 12V fan for the module. Cooling with a 5V fan is 5 to 9 times more efficient than natural convection cooling and 2.7 times more efficient than forced-air convection at a 400 ft/min (fpm) linear airflow. For example, a module for a 17×17-pin PGA has a thermal resistance of 1.4°C/W as compared with 10°C/W for natural convection cooling and 3.9°C/W for 400-fpm forced-air cooling. $13.24 (500).

Thermalloy Inc, Box 810839, Dallas, TX 75381. Phone (214) 243-4321. FAX (214) 241-4656. TLX 203965. Booth 5136. **Circle No. 413**

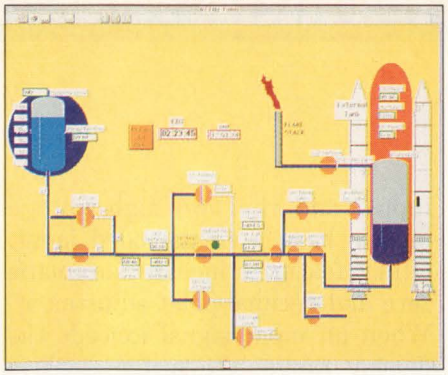
Impact Printers

The TG and TXG Series impact printers come in an injection-molded housing having a 7.8×6-in. footprint. The nine models provide a range of 24 to 42 print columns and have an RS-232C, RS-422, or Centronics parallel port. The 24-column model prints 144 dots/line; the 42-column model prints 252 dots/line. An input buffer and bit-image graphics are standard on all models. The TXG Series has a 6912-character input buffer, and the TG Series has a 2048-character input buffer. The units operate from a

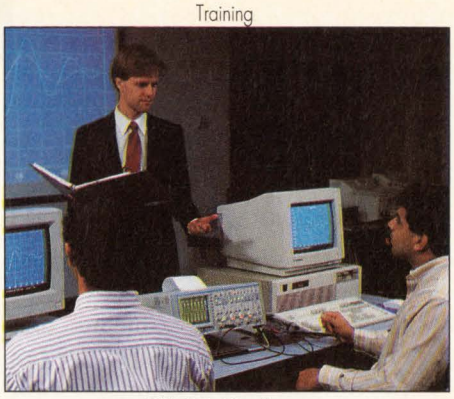
Data Acquisition Boards



LabVIEW ®

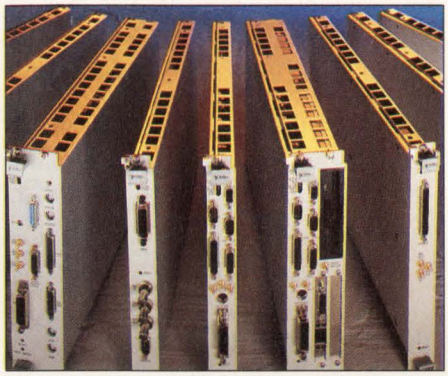


Training

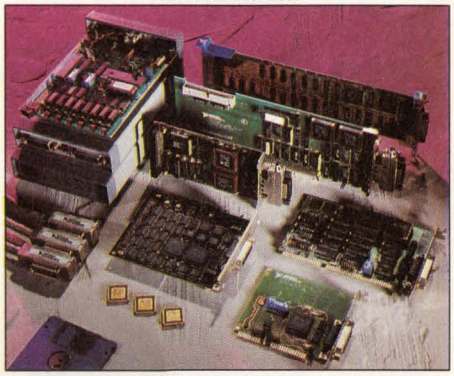


DSP Hardware & Software

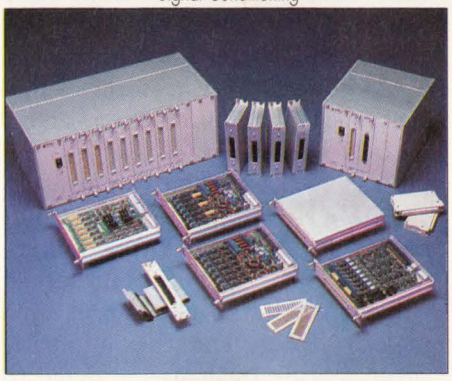
VXI Controllers



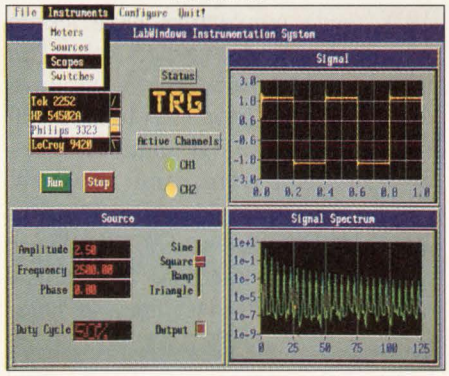
IEEE-488.2 Interfaces



Signal Conditioning



LabWindows ®



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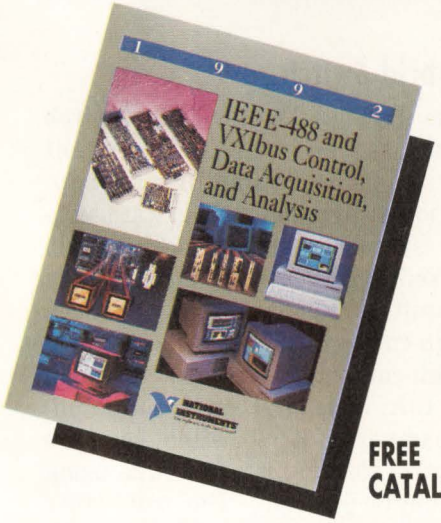

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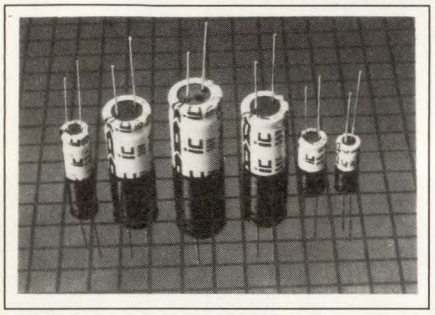
See us in Booth #2201

CIRCLE NO. 53

120V ac wall-mount power supply; a 12V dc power input is available as an option at no extra cost. Options for the TG series include one or two cash-drawer drivers for point-of-sale applications. From $177 (100). Delivery, 8 to 10 weeks ARO.

Telpar Inc, Box 796, Addison, TX 75001. Phone (214) 233-6631. FAX (214) 233-8947. Booth 2308.

Circle No. 414



Aluminum Capacitor

A line of low-leakage, radial-lead, aluminum capacitors offers an alternative to tantalum capacitors. The devices feature a 0.1- to 1000-μF capacitance range, a working voltage range of 10 to 50V dc, a minimum leakage current of 0.4 μA; an operating temperature range of −40°C to +85°C; and a storage temperature range of −55°C to +85°C. Standard capacitance tolerance is ±20%; ±10% tolerance is optional. From $0.04 (1000).

Illinois Capacitor Inc, 3757 W Touhy Ave, Lincolnwood, IL 60645. Phone (708) 675-1760. FAX (708) 673-2850. TLX 724361. Booth 4514. **Circle No. 415**

Digital Voltmeter

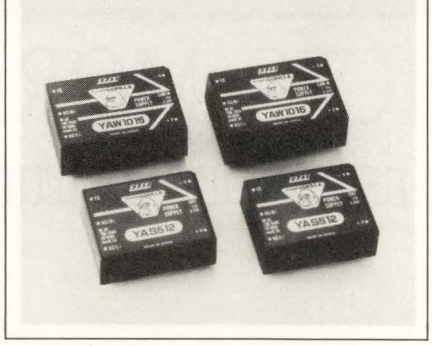
AP-501 Series digital voltmeters have a 3½-digit LED display and a measurement accuracy of 0.1% of the reading or 1 digit at room temperature. The four meters in the series span the measurement range from 200 mV to 200V. The two low-voltage models have a differential input, and the two high-voltage models have a single-ended input. Other features include automatic zero and decimal-point adjustment. When an input signal exceeds the display range, the meter displays an overrange indicator. The meters measure 48×96×12.2 mm and weigh 50 grams. The meter's conversion rate is 2.5 sec. $71.

Delco Products Co, 7580 Stage Rd, Buena Park, CA 90621. Phone (800) 257-3526; (714) 521-8673. FAX (714) 739-1507. Booth 4305.

Circle No. 416

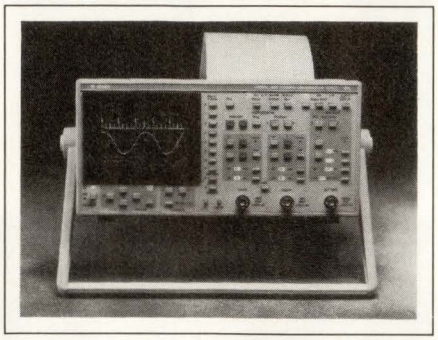
PC-Board AC/DC Converters

The YAS and YAW series 5 and 10W ac/dc converters have single and dual outputs, respectively. The units mount to a pc board and have autoranging inputs that handle 100 to 240V ac. The 5W units measure 58×45×19.5 mm, and the 10W units measure 65×45×21 mm. Both series come in 5V, ±12V, or ±15V output models. Other features include 20-msec holding time,



47- to 440-Hz frequency range, typical inrush current of 20A for 100V ac inputs and 40A for 200V ac inputs, and automatic recovery from overcurrent operation. The units operate from 0 to 55°C. They can withstand 10g vibration from 10 to 55 Hz and an impact of 50g for 11 msec. $41 to $48 (100).

US Elco Inc, 2930 Scott Blvd, Santa Clara, CA 95054. Phone (800) 888-3526. FAX (408) 980-9754. Booth 1405. **Circle No. 417**



Portable Digital Oscilloscope

The 465 portable digital oscilloscope can simultaneously sample two channels at 200 Msamples/sec, thus providing a 100-MHz signal bandwidth for both channels. The unit has a 2-Gsample/sec equivalent time-sampling rate for repetitive signals. Other features include 8-bit resolution for all input sensitivities, three nonvolatile waveform memories, 400V input protection, and a battery option for field-service applications. The scope conforms to the IEEE-488.2 Standard Commands for Programmable Instruments (SCPI) standard. On-screen cursors facilitate voltage and time measurements, and the automatic setup feature evaluates a signal to optimize scope settings. $3490.

Gould Inc, Test and Measurement Group, 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7263. FAX (216) 328-7400. Booth 2303. **Circle No. 418**

Hybrid Switch

The Hybrid Double-Pole Switch consists of two independent switches—a double-break snap-action switch and a solid-state optical switch—that are mechanically linked together. The unit permits simultaneous switching of both high-current and logic-level loads. High-current loads can be as high as 10A; logic-level loads can be microamperes. The switch lets you control three isolated circuits using a single package. The solid-state switch is immune to bounce and

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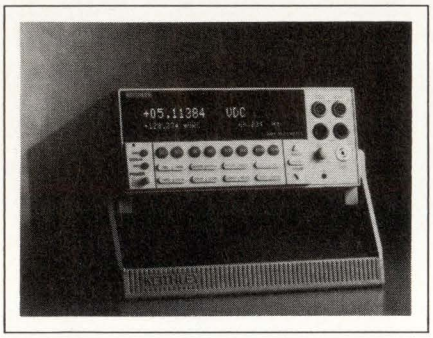
CIRCLE NO. 54

contact contamination, and the mechanical switch employs a butterfly configuration. $10 (1000). Delivery, 12 weeks ARO.

ITW Switches, 6615 W Irving Park Rd, Chicago, IL 60634. Phone (312) 282-4040. FAX (312) 545-4450. Booth 1228. **Circle No. 419**

Digital Multimeter

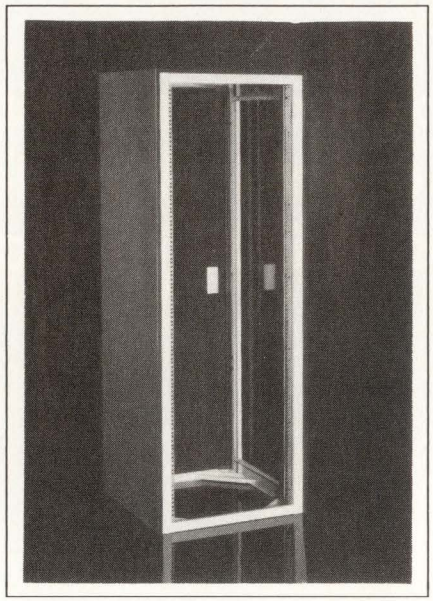
The Model 2001 digital multimeter (DMM) has a resolution range of 4½ to 7½ digits. Other features include 18-ppm dc voltage accuracy (90 days); 0.05% ac voltage accuracy; average, rms, and peak ac measurements; frequency measurement to 15 MHz; a 1100V input rating; and a resistance resolution of 1Ω. You can program the DMM's 10-channel scanner to measure different functions on each channel. In addition, the DMM can simultaneously display multiple measurements of the same signal. The DMM can take as many as 45 readings/sec, and you can specify the reading rate. The unit can change ranges and functions in 20 to 150 msec, and the trigger delay is 20 μsec. $2695.



Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; (216) 248-0400. FAX (216) 248-6168. Booth 2418. **Circle No. 420**

Vertical Enclosures

Models in the Frugal Frame line of vertical enclosures incorporate top and base cowlings as part of the frame. The enclosures accept most of the company's accessories, including cooling devices, mounting channels, hardware, shelves, power strips, drawers, writing surfaces, panels, and doors. The enclosures are available in 21- to 78-in. panel heights having 19-in. widths. Depths of 25½ or 30 in. are optional. The enclosures have a textured finish, and panels, doors, and tops are available in a variety of standard colors. A modular design permits series-mounted and multibay configurations. Typical cost for a 61×19×25½-in. console is $450 including frame, top panel, side panels, and rear door.



Amco Engineering Co, 3801 N Rose St, Schiller Park, IL 60176. Phone (800) 833-3156; (708) 671-6670. FAX (708) 671-9469. TWX 910-227-3152. Booths 1415 and 1417. **Circle No. 421**

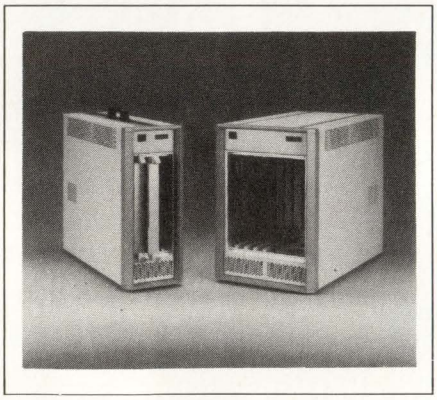
Spectrum Analyzer

The Model 2610 portable RF spectrum analyzer can operate at 1.0 GHz. The 4.5×11.8×13.4-in. unit weighs 20 lbs and runs from ac or battery power. For communications measurements, you can select a fixed RF bandwidth of 1 MHz regardless of the scan-width setting. The analyzer has a rechargeable battery and battery charger as well as a 100-MHz, 80-dBμV calibration signal. The unit has a switch-selectable input impedance that matches either 50 or 75Ω cable. The analyzer comes with a 75Ω input cable, BNC-to-F connector adapter, CRT hood, adjustment tool, spare fuses, and a manual. $2995.

B+K Precision, 6770 W Cortland Ave, IL 60635. Phone (312) 889-1448. FAX (312) 794-9740. Booth 2132. **Circle No. 422**

Futurebus+ Products

A line of Futurebus+ floor-standing tower chassis meets Profile A, B, and F specifications. The multilayer 64-bit, 192-pin backplane has three I/O slots. The chassis feature RFI/EMI shielding and come with a fan and power supply. A line of backplanes that meet Profile A, B, and F specifications is also available. The multilayer, impedance-controlled backplanes have 3 to 14 slots and 192 I/O pins for 64-bit data transfers. The backplanes feature surface-mount terminators, distributed and central arbitration, and 2-mm metric connectors. Chassis, from $3000. Backplanes, from $850 for a 3-slot version; $2150 for a 14-slot version.



Schroff Inc, 170 Commerce Dr, Warwick, RI 02886. Phone (800) 451-8755; (401) 732-3770. FAX (401) 738-7988. Booth 5424.

Circle No. 423

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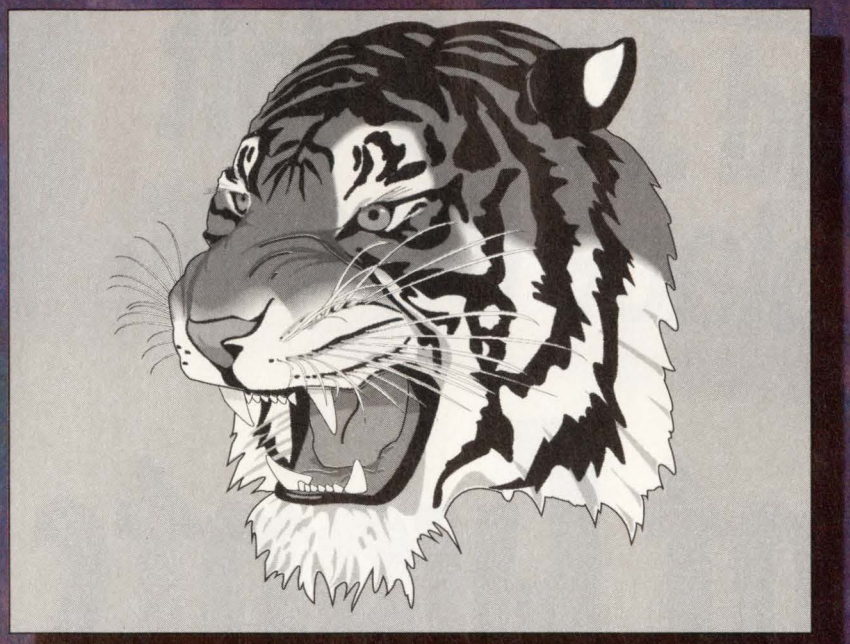

On a much larger scale.

At last. A personal output device that combines the best features of a desktop laser printer with the ability to produce large format drawings. It's called ProTracer — a 360 dpi desktop printer/plotter that produces A, B, as well as C-size output.

ProTracer's speed and quiet operation come from the latest Canon inkjet technology and an Intel i960 processor. Drawings that take up to half an hour to print on a pen plotter take only five minutes on ProTracer!

And, unlike other large format devices, ProTracer isn't limited to plotting. Start with the ProTracer base unit that incorporates resident IBM ProPrinter and Epson LQ-1050 emulations, as well as an ADI plotter driver for AutoCAD users. Then, depending on your needs, choose from a variety of optional accessories including HP-GL® and PostScript® language emulation cards.

Optional Printer Accessories

HP-GL emulation card	$399
PostScript language emulation card	$499
2 MB memory upgrade	$299
4 MB memory upgrade	$499
8 MB memory upgrade	$899
Sheet feeder I (100 sheet)	$149
Sheet feeder II * (100 sheet)	$129
PacificTalk (AppleTalk interface module)	$199

*Sheet feeder I is required for use

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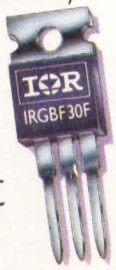
Current Events.

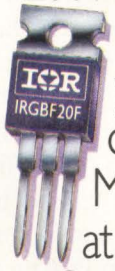
It's now official. Bipolar is yesterday's news. IR announces 900v and 1200v IGBTs in TO-3P and TO-220 packages.

They're the more efficient, faster switching, easier-to-design alternative to bipolar.

They're also more rugged, take up less board space, and less budget space. And like their 600v predecessors, they're bound to set new performance standards wherever they're designed in.



For more information about the new 900v and 1200v TO-3P and TO-220 IGBTs, just phone your local IR rep, or the IR IGBT Marketing Group at 310/640-6534.



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CIRCLE NO. 55

Module-generation tool eases top-down FPGA design

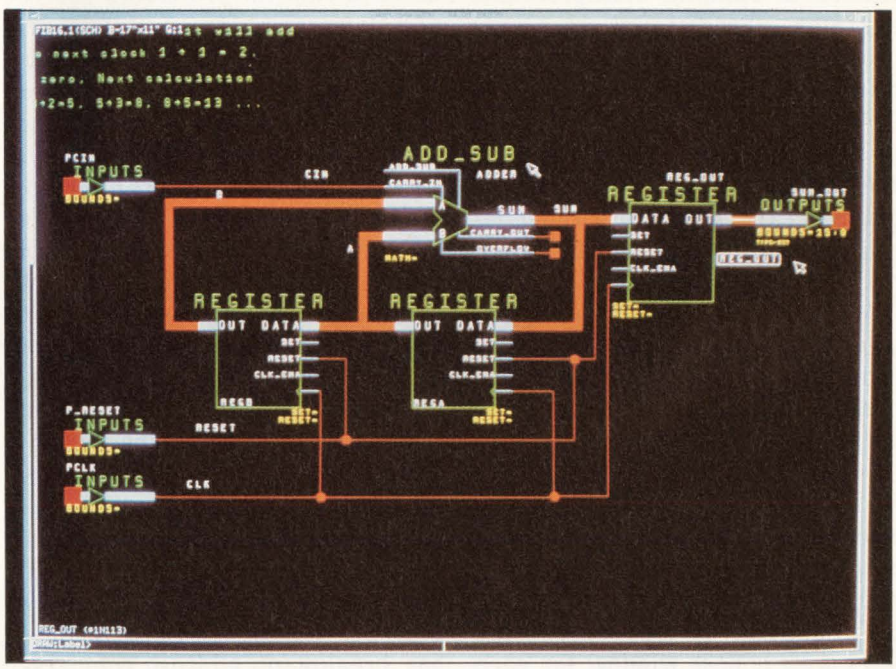
Engineers no longer need to face a Hobson's choice between low-level gate delay or high-level language for FPGA design. With Xilinx's Blox tool, which uses high-level module generation, engineers can define their designs graphically with parameterized functional blocks similar to those in silicon-module or data-path compilers.

Blox comprises 30 logic modules, including adders, subtracters, registers, static RAMs, comparators, multiplexers, accumulators, shift registers, PROMs, bus interfaces, counters, 3-state buffers, and bus functions.

With this tool, you don't need to learn a new front-end tool. Instead, you can continue to use current schematic editors, such as Viewlogic's Viewdraw, Mentor's Neted, Futurenet's Dash, the Cadence editor, and the OrCAD-SDT. Blox accepts netlist entry from these popular editors, and has the ability to specify a design in higher-level, parameterized models.

By simply changing a parameter, a module such as an adder can have its size automatically changed. Thus, modules can be changed from 9 to 10 bits without having to redraw anything. In addition, the tool is "smart"; it can take one parameter size and backtrack to other modules that feed the labeled entity—and change their sizes as well. A single parameter change can scale a design up or down.

The software then converts a generic design to a standard, hierarchical Xilinx netlist file (XNF) and feeds the file to the tool for processing. This design is then synthesized into an FPGA implementation. But unlike most gate-level designs, Blox has the advantage of top-down design information. This grouping of function and location helps to ensure efficient routing.



Engineers can define designs at a functional block level *using Blox's schematic capture.*

The Blox tool does the following operations on the netlist:

- *Scales data-path widths*
- *Assigns clock and high fanout signals to buffers*
- *Assigns master reset signal*
- *Remaps arithmetic functions to use XC4000 fast-carry logic*
- *Moves registers/flip-flops to I/O blocks on the chip periphery (these I/O blocks have built-in flip-flops)*
- *Expands and merges the logic modules.*

Blox is built with a rule-based system, which makes it easy to map designs into the underlying RAM-based logic architecture. The software has an advantage over the older gate-based mapping: Blox has high-level design knowledge, which aids in mapping the logic into the FPGA architecture.

Engineers no longer have to use pure module-based design; they can mix design representations. The circuit structure and major blocks can be defined graphically. But, control logic, such as state machines, can be defined in a number of ways, such as schematics or equations.

Blox links into the standard Xilinx XACT 4000 development system and costs $2995 for a PC and $4995 for a workstation version.

—Ray Weiss

Xilinx Inc, 2100 Logic Dr, San Jose, CA 95124. Phone (408) 559-7778. FAX (408) 559-7114. TWX 510-600-8750.

In-circuit emulator supports multiprocessing debugging

Debugging software is a major barrier to building multiprocessor systems. Traditional test approaches, such as ICEs, become unaffordable for large numbers of CPUs. However, a Texas Instruments's hardware/software team, the TMS32C40, with on-chip debugging, and the XDS 510 parallel debugger, lets you debug DSP multiprocessing systems.

With the XDS 510 debugger you can control multiple C40s. They can stop and start all or just one processor; halt one or more CPUs with breakpoints; and single-step one or all processors. The processors can be stopped within a few clock steps. Also, you can group and control processors by a defined name. And, executing software can be debugged at the source-code level with a host window for each processor.

Each TMS320C40 has a JTAG (IEEE JTAG 1149.1 test bus) serial port for onboard test and real-time execution control. The JTAG serial port links to an on-chip analysis module and can be used to control the processor. The CPU can be halted, registers and status read or set, breakpoints set, and events monitored. Multiple C40 processors are linked via a JTAG serial link.

The XDS 510 parallel In-System Emulator development system utilizes the C40's JTAG interface to control one or more C40 processors. The emulator runs on a PC. It has a PC half-card, which drops into the PC host bus. A target cable runs from the half-card to an Active Buffer Pod and a short cable that links to an onboard, 14-pin JTAG connector. A full C/assembler source-code debugger also comes as part of the package. The debugger provides a set of interactive windows for each C40 CPU; they allow users to view the processors' source and disassembled code, memory, function call, and a watch window.

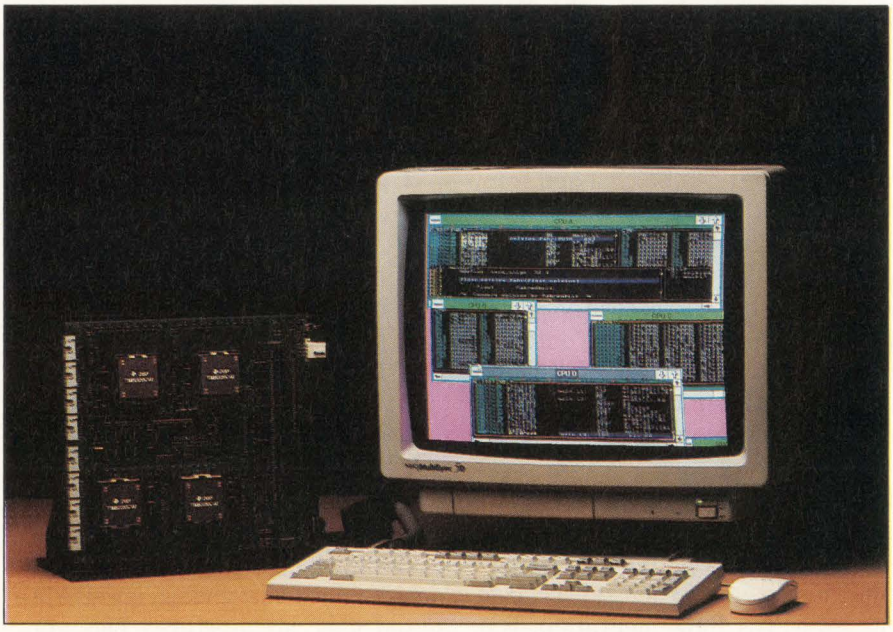
The XDS 510 comes with a TMS320C40 C compiler, which has a parallel runtime support library. Library functions support interprocessor communications via the C40's six communication-link ports (each C40 has six ports for point-to-point links with other C40s). Each 8-bit port has a peak throughput of 20 Mbytes/sec. A parallel-processing assembler/linker partitions code between processors. The assembler/linker has directives for mapping program and data code to specific processors.

Each C40 has an on-chip DSP analysis module, which takes on key ICE-like functions. Each module has breakpoint address comparators for program, data, and DMA addresses. Discontinuities—program trace address changes—are saved in a program discontinuity stack, which holds the from, to, and PC addresses. Also included is an event counter for benchmarking and profiling execution.

Currently, the XDS 510 runs on a PC under OS/2. The development software runs on PCs (DOS, OS/2) and the Apple Macintosh, as well as Sun and DEC workstations.

The company is also fielding a parallel development system (PDS), which integrates four C40s onto a single board. These DSP processors each have no-wait-state 64k×32-bit words or static RAM (SRAM) and 8 kbytes of EPROM. The system also has a shared global memory on a common bus with 128k×32 words of one-wait-state SRAM. A board JTAG connector links in the XDS 510 emulator. The debugger system costs $8000; the compiler costs $1500.—***Ray Weiss***

Texas Instruments, Semiconductor Group, Box 809066, Dallas, TX 75380. Phone (800) 336-5236.



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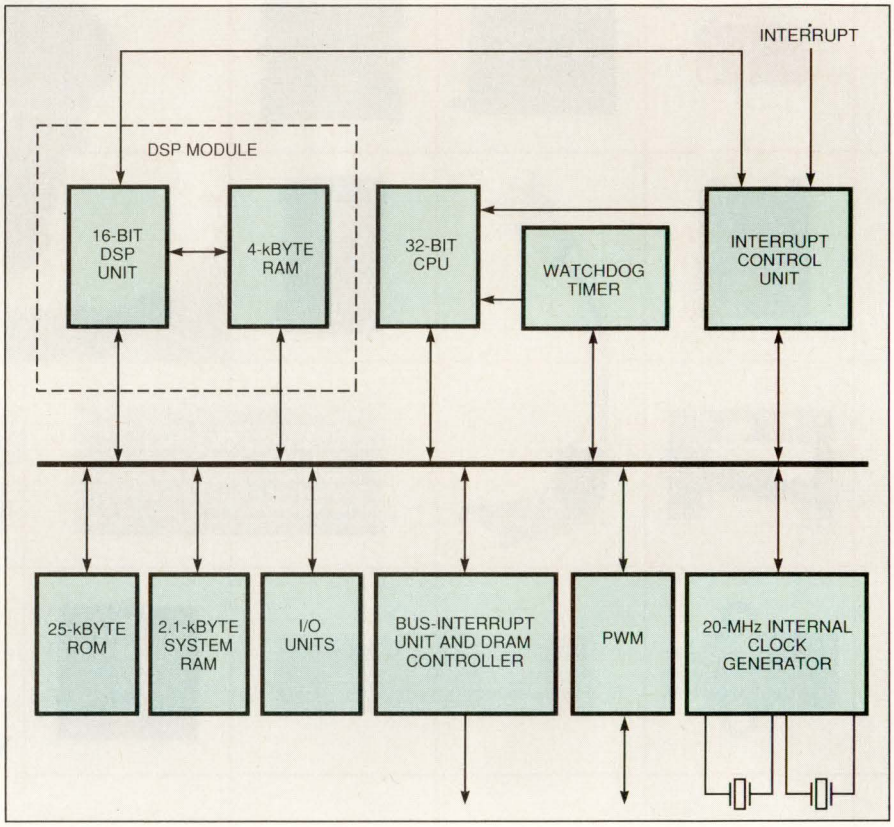
CIRCLE NO. 56

Microcontroller combines CISC and DSP for low-end voice processing

The NS32AM160 microcontroller (μC) is part of a 3-chip set for low-end voice processing. When combined with two chips, an ARAM (audio-quality DRAM that's flawed) and a codec, the μC performs voice processing. It handles voice synthesis, recording, and playback, as well as modem and phone-line processing.

In addition, the company provides application software and algorithms for voice processing. Also available is a set of turnkey answering-machine software. You can modify this generic code to build tailored applications or run it as is for a fast out-of-the-box implementation.

The μC has a dual-processor arrangement. It combines the company's 32-bit embedded CISC- (complex-instruction-set-computer) core processor with a 16-bit DSP processor. In this arrangement, the host 32-bit CISC CPU handles overall system control and I/O, as well as setting up and kicking off DSP. Both processors run at 20 or 25 MHz.



The 32AM160 microcontroller controls voice processing *by combining a 32-bit CISC CPU with a dedicated DSP module.*

The chip contains a 25-kbyte ROM to hold program and constants and a 2.1-kbyte RAM for dynamic data and code. Off-chip memory can hold processing parameters and data. The DSP processor runs from its own 4-kbyte RAM. However, one on-chip memory space serves both the CISC and DSP processors, allowing data exchanges between the processors. The DSP processor runs as a slave to the host CPU and executes out of on-chip memory.

The DSP module is a pipelined, vector-processing engine. In many ways, it resembles the old-fashioned display-list processors for vector graphics. The host CPU sets up the initial program and initializes processing by setting a program pointer to nonzero. The DSP module runs the program to completion and then stops, waiting for its next assignment. It can pass data to the host via shared memory, as well as trigger a host interrupt for immediate response. A 16-bit processor, the DSP module provides a simplified instruction set, having 52 instructions. It's a DSP processor that handles complex math calculations.

At 25 MHz, the μC executes an FIR-filter algorithm at 40 nsec/tap and a complex FIR-filter algorithm at 160 nsec/tap. The chip has a dynamic-RAM controller, a 1-MHz PWM unit, a timer, a watchdog timer, a 4-level interrupt control unit, and 16 bit-programmable I/O lines. For off-chip memory, the μC relies on an 8-bit bus and 11 address lines.

The chip sells for $17 (10,000) and comes in a 68-pin plastic-leaded-chip-carrier package.—***Ray Weiss***

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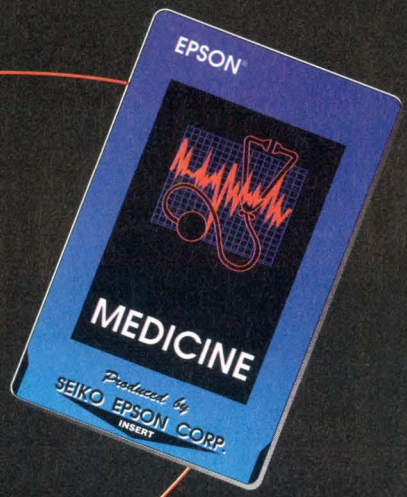

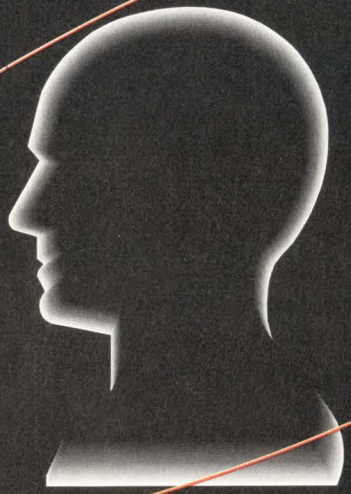

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CIRCLE NO. 58

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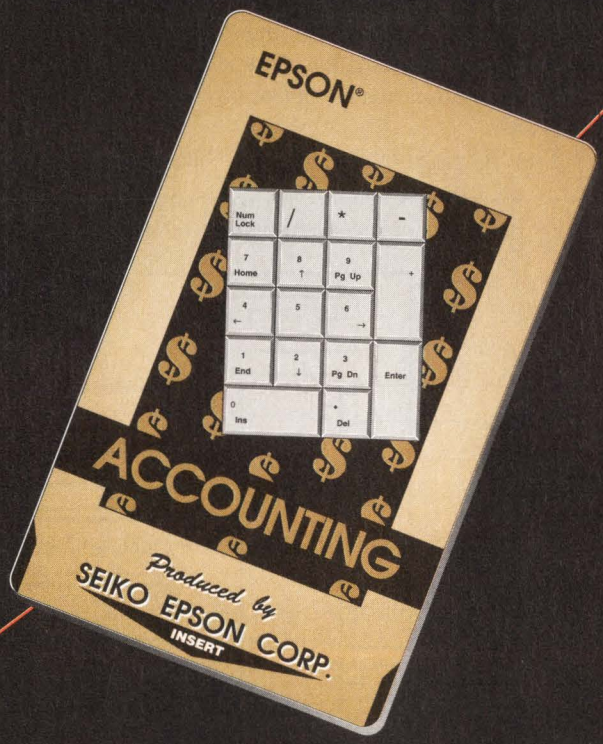

IC encodes RGB or YCrCb inputs to produce NTSC or PAL outputs

The Bt858 digital encoder IC converts computer-graphics images to formats used with television display standards. It can drive NTSC video devices used in the USA and PAL (phase-alternation-line) units that are common in Europe. It also provides Y and C outputs for S-Video display applications and can accept input data in RGB (red-green-blue) or YCrCb color-space formats.

The IC provides one of the key capabilities needed in multimedia systems. Boards that use the encoder can output computer-generated presentations directly to televisions or to consumer video-tape recorders. Other applications include video editing and using the IC with video peripherals such as scanners and cameras and photo databases.

The IC's generated 4-field, 525-line NTSC signals are considered nearly studio quality. For PAL applicatioms, the chip produces an 8-field, 625-line image. In NTSC, PAL, or S-video modes, the IC provides pixel clock rates ranging from 12 to 18 MHz. You can also program the number of pixels generated for each scan line, allowing you to use the IC in applications other than standard 12.27-MHz NTSC, 13.5-MHz CCIR601, and 14.75-MHz PAL.

Fig 1 depicts the internal architecture of the Bt858. The IC has three 256×8-bit lookup-table RAM arrays. A separate stack of 15 24-bit registers stores overlay information. The IC also has an on-chip color-bar generator and can handle mixing of computer-generated graphics and captured video images.

The IC accepts composite sync or separate horizontal and vertical sync signals for timing control. It can also accept the CCIR601 H, V, and F control signals, or it can generate horizontal and vertical sync signals. The color-conversion blocks perform RGB to YIQ/YUV for NTSC applications and YCrCb to YIQ/YUV for PAL applications.

The video encoder represents the first in a family of ICs from the company that targets multimedia applications. The CMOS device requires a 5V power supply and typically dissipates 900 mW. It comes in a 132-pin quad flatpack and costs $67 (100).—***Maury Wright***

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (800) 843-3642; (619) 452-7580. FAX (619) 452-1249.

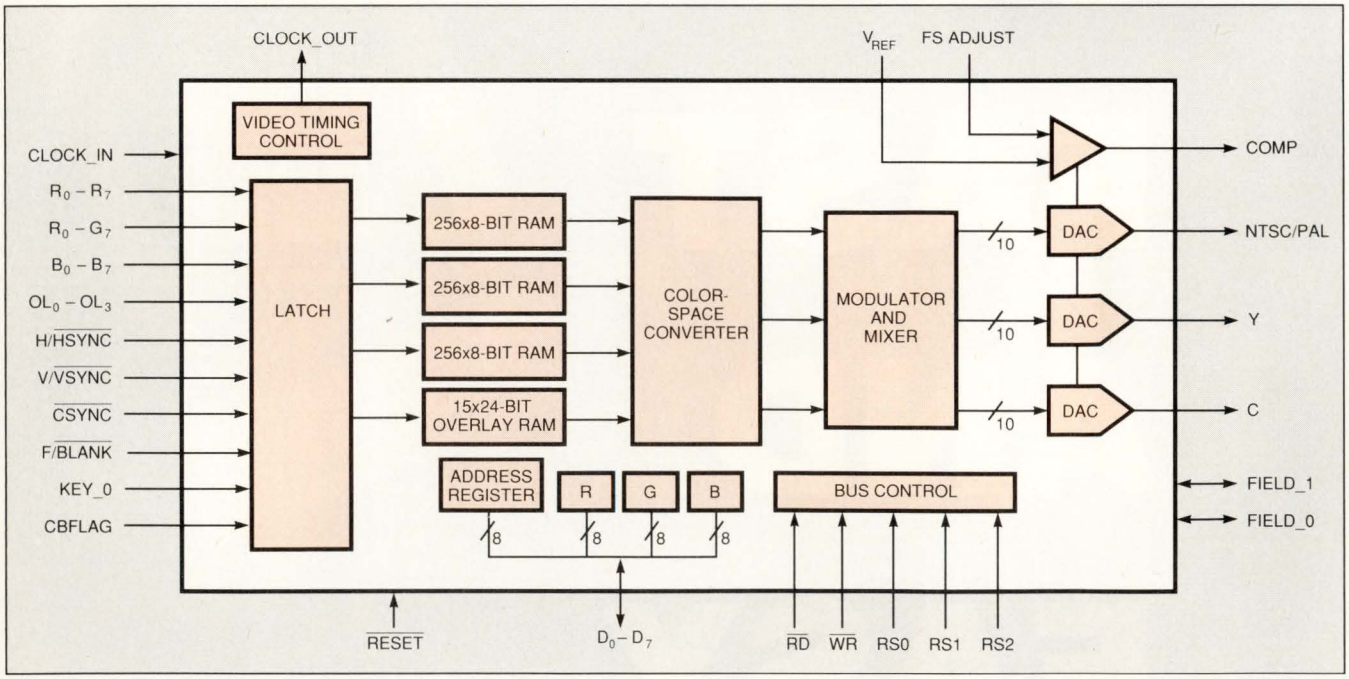

Fig 1—A choice of S-Video, NTSC, or PAL *outputs makes the Bt858 video-encoder IC useful in applications that require compatibility with different international television standards.*

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Gyroscope allows 3-D motion sensing for robotics and desktop computers

The Gyropoint pointing device lets you add to your computer the ability to sense either linear or angular motion with three degrees of freedom. A miniature gyroscope is the key to the pointer's unique ability and is available to system developers for other motion-sensing applications.

The pointing device resembles a 3-button mouse, but it's a mouse with wings. Instead of being confined to a flat surface, the pointer works in unrestricted free space and allows you three degrees of freedom. If you're using it in its mouse-compatible mode, the pointer gives you X- and Y-axis position data. You can either slide the pointer along a flat surface (it has a Teflon bottom for easy sliding) or wave it around in mid-air.

If your application software signals the pointer that it can accept 3-D data, the pointer operates as an angular sensor, giving you direct measurements of roll, pitch, and yaw. The pointer's mode switch lets you signal the application software whether to interpret the pointer's data as linear or angular motion. It also has an activate switch, allowing you to turn the pointer when you're not pointing with it.

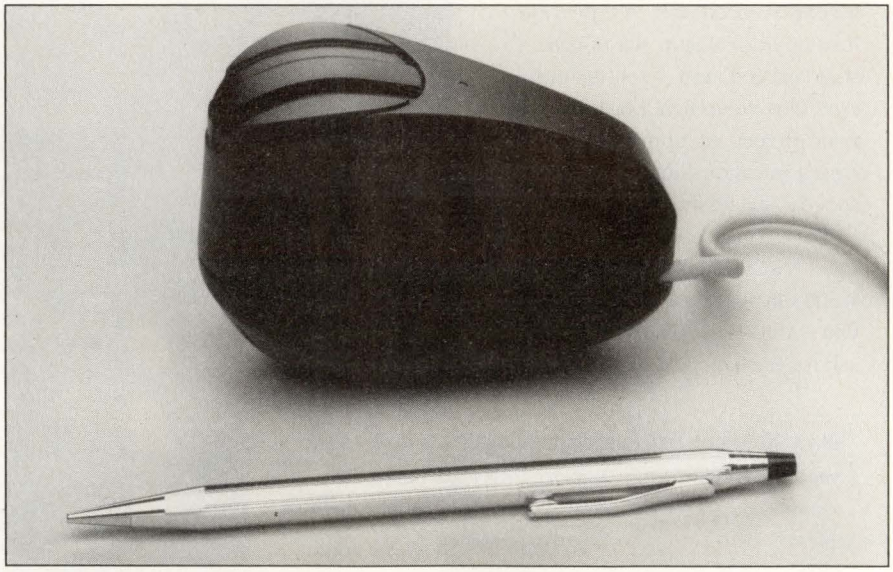
An embedded microcontroller handles all the pointer's interface functions and translation between angular and linear data in mouse-compatible mode. At rates from 1200 to 4800 baud, the device will handle RS-232C, RS-423, and Apple Desktop Bus protocols.

The key element of this pointer is a miniature spin gyroscope, the Gyroengine. The pointer uses two of these devices to provide three degrees of freedom. Like a conventional gyroscope, the Gyroengine uses a spinning motor inside a double-gimbaled housing to establish an inertial reference axis. The gimbals allow the axis to remain stable if the housing moves. Optical sensors detect the housing's movement relative to the axis and an onboard microcontroller translates that movement into a serial data stream.

The gyroscope is small, measuring 1.75 in. high by 1.25 in. in diameter. It weighs 1.2 oz and draws a nominal 0.1W at 3V when running. Its microcontroller handles all of the gyroscope's control functions, including spinning up the motor, sampling the position data, and recovery from out-of-range motion. The gyroscope's range is 360° for yaw and ±80° for roll and pitch, with an angular resolution of 10 bits/degree. It has a drift of <2°/min.

The gyroscope is also fairly rugged. It will operate in 0 to 70°C temperature at unlimited altitude. It will also tolerate shocks as great as 1000G for 3 msec.

Although the Gyropoint is available to OEMs as a product for bundling with 3-D application software, it is intended to be a demonstration vehicle for the Gyroengine. The engine suits a range of motion-sensing applications. Electronic navigation, robotic arm movement, and platform stabilization are among the possibilities. A developer's kit that includes a pointer, interface schematics, and documentation costs $1000. Production pointers will be available in early 1992.



You can't see the wings on this mouse, *but it has them. The Gyropoint 3-D pointer can operate like a mouse, but it doesn't need to stay on a table.*

—Richard A Quinnell

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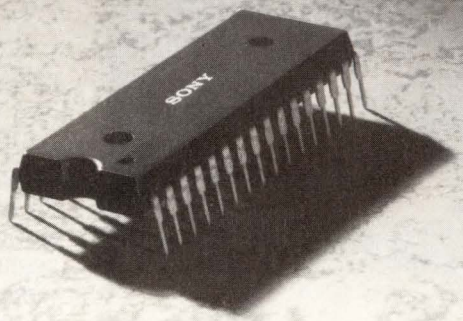

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CXK581100YM	100/120	TSOP (rev.)	12/50	
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CXK581001M	70/85	SOP 525 mil	12/50	
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Note: All packages 5V, 32 pin, 128K x 8, unless otherwise noted.

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Fractal geometry compresses video images that have independent resolution

In the late 1970s Benoit Mandelbrot, a professor at the Massachusetts Institute of Technology, demonstrated that you can create abstract pictures by the repeated use of some fundamental mathematical formulas called fractals. This work stimulated the interest of scientists as to whether still or moving video images could be represented by a fractal model. The P.OEM series uses fractals for image compression in hardware and image decompression in software.

In the mid-1980s, Dr Michael Barnsley discovered that you can describe an image using a mathematical breakthrough called the "fractal transform." In May of 1987, Dr Barnsley helped found Iterated Systems Inc to put the fractal transform into practical use in image-compression applications. The company currently offers a family of fractal-based, image-compression products for the OEM, software development, and system-integration market. The product family name, P.OEM, stands for Pictures for OEMs.

The company has developed an ASIC that performs the fractal transform and offers an ISA bus board having eight fractal-transform ASICs, 256 kbytes of RAM, and an Intel 80960 μP. The board accepts data from a frame grabber or a scanner and the eight fractal-transform chips operate in parallel to compress an image into fractal-image-format (FIF) files. The board can compress a 768-kbyte image to 10 kbytes in 240 sec or less. The company recently announced a price reduction for this board, called the FTC-8B, from $8850 to $2995.

A 20-kbyte fractal-image-format (FIF) file *generated these three photographs. By applying the fractal transform to successive sections of the file, the pictures display compression ratios of 154:1, 614:1, and 2456:1, while maintaining 1280 × 800-pixel resolution.*

In addition, a lower-cost version of the board, called the FTC-1B, has one fractal-transform ASIC. The $1995 board calculates the fractal transform at a much slower rate, however. An $8850 board, called the FTC-II, uses eight fractal-transform chips, 1 Mbyte of RAM, and an 80960 μP. This board operates with the latest version of the company's software development kit, called P.OEM Color Stillframe Developer's Kit version 2.1, which performs decompression in software.

By taking advantage of a feature of fractal-transform technology called fractal Zoom, version 2.1 of the developer's kit can demonstrate compression ratios as high as 2456:1. This feature can scale sections of a compressed image file to create a "zoom effect" without degrading the resolution. Because of the resolution-independent nature of fractal image compression, the resolution is limited only by the display circuitry. The $2995 software package consists of MS-DOS linkable modules, which can be ac-

UPDATE

cessed by a C language program for OEM use.

To illustrate the power and viability of fractal image-compression, the company is offering a $79 software package that has a "clip-art library" of 250 color images having 640 × 400 × 24-bit resolution. This software, called the Fractal Formatter, occupies less than 4 Mbytes of hard-disk space and represents 192 Mbytes of uncompressed color-image data. The images are in FIF format and are compressed using the P.OEM compression algorithm.

In addition, Fractal Formatter accepts image files from a variety of formats including Targa, Tiff, and Raster files for editing or conversion to FIF files. You can cut and paste images, rotate images, and shrink the dimensions. Because the software runs under Microsoft Windows, you can extract images from the "clip-art library" into a graphic design with the click of a mouse.—***John Gallant***

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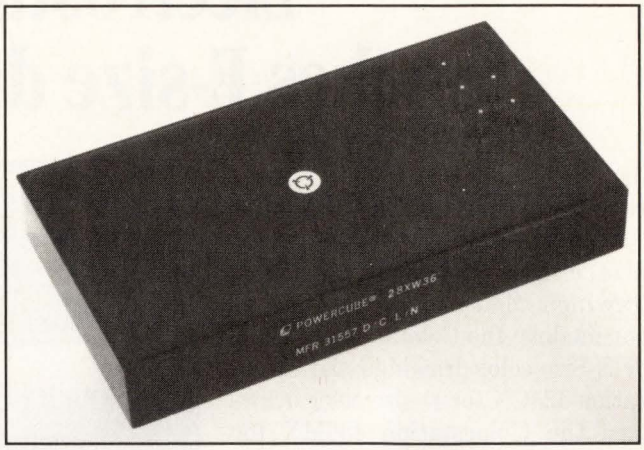

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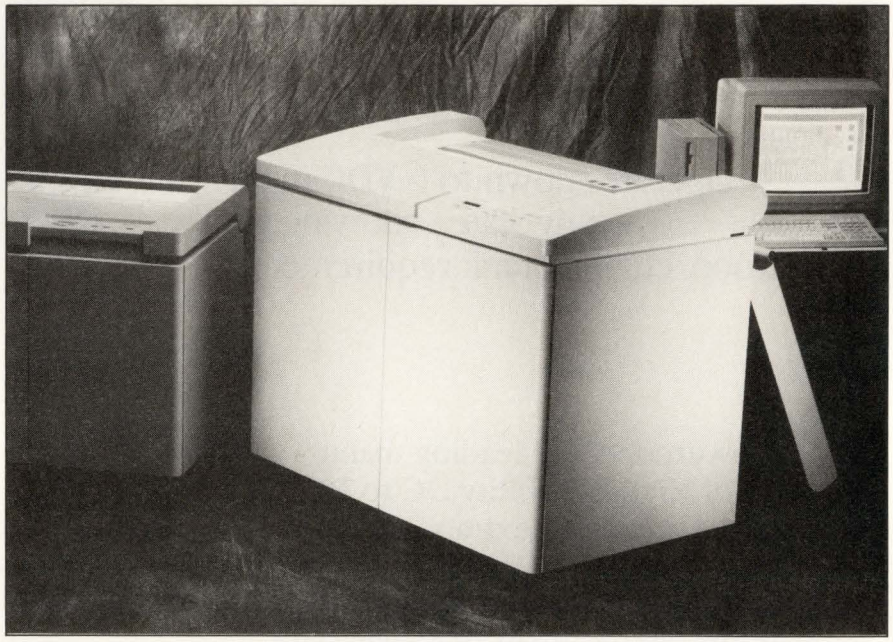
Electrostatic plotter makes E-size drawings at 6 ips

The Colorstation 400X family of electrostatic plotters produces color or monochrome, E-size (36 × 50-in. cut-sheet) or D-size (24 × 36-in. cut-sheet), drawings. The series consists of four models: the Colorstation 436CX for E-Size color drawings; the Colorstation 424CX for D-size color drawings; the Colorstation 436MX for E-Size monochrome drawings; and the 424MX for D-size monochrome drawings. The plotters boast a writing speed of 6 ips—considerably faster than competitive models that write between 0.8 and 2 ips.



Providing switch-selectable 200- or 400-dpi resolution, the Colorstation 400X Series color and monochrome electrostatic plotters produce plots at 6 ips.

The plotters achieve their high plot speed by employing a patented Silicon Imaging Bar writing head. Conventional electrostatic plotters employ a multiplexed writing head to transfer electrical charge to the media. A multiplexer transfers charge from a common source to multiple nibs. The Silicon Imaging Bar writing head consists of a dedicated driver for each nib. Because a multiplexed driver necessitates a time delay before applying charge to subsequent nibs, it is slower than these dedicated drivers.

In addition, the Colorstation Series can accurately register the location of dithered color dots. Conventional electrostatic plotters employ a multipass reel-to-reel media-transport system, which rewinds on each pass to deposit the four primary colors. On the first pass, reel-to-reel systems place registration marks on the edge of the media to provide servo information for subsequent passes. However, during the toning process, any paper stretching can distort this registered information.

The Colorstation Series locks the cut-sheet media onto a belt using a vacuum. Registration marks are fixed on the vacuum-locked belt, which rotates past the nibs on each color pass. Because the media cannot shift or stretch while locked to the belt, the vacuum-locked system ensures registration from one color application to the next. The Colorstation series has an overall plot-accuracy specification of 0.05%.

For a print controller, the Colorstation Series plotters employ an Intel 80960CA RISC μP that delivers 66 MIPS peak. The plotters also offer 200-dpi plots for quick drafts and 400-dpi plots for fine detail. You switch between modes with the press of a button. Competitive models offer only one of these resolutions. In 200-dpi mode, the 436CX can produce a full-color, E-size plot in less than 3 minutes.

A plot-nesting feature places A- through E-size drawings on a single sheet. For example, an E-size model can plot 16 A-size, 8 B-size, 4 C-size, 2 D-size, or a combination of these sizes on a single E-size sheet. A plot-tiling feature lets you plot large panels by automatically splitting a drawing into several images and plotting the im-

Table 1—Electrostatic plotter prices

Model	Hard-drive capacity		
	42 Mbytes	100 Mbytes	234 Mbytes
424MX	$22,895	$23,895	$24,895
424CX	$34,895	$35,895	$36,895
436MX	NA	$28,895	$29,895
436CX	NA	$44,895	$45,895

NA = Not available

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100 channels, 100 MHz sync	YES	YES	YES
Dynamic cache control	YES	NO	NO
Data cycles fully labeled in disassembly	YES	NO	NO
Maximum trace depth	128K	128K	4K
Maximum synchronous rate	200 MHz	100 MHz	100 MHz
Maximum asynchronous rate	1GHz	400 MHz	500 MHz
Split timebase on a single card	YES	NO	YES
Setup+Hold time	3.0 nsec	5.0 nsec	3.5 nsec
Price performance value	High	Low	Moderate

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*Such as 80486 or beyond, or 68040 or beyond.

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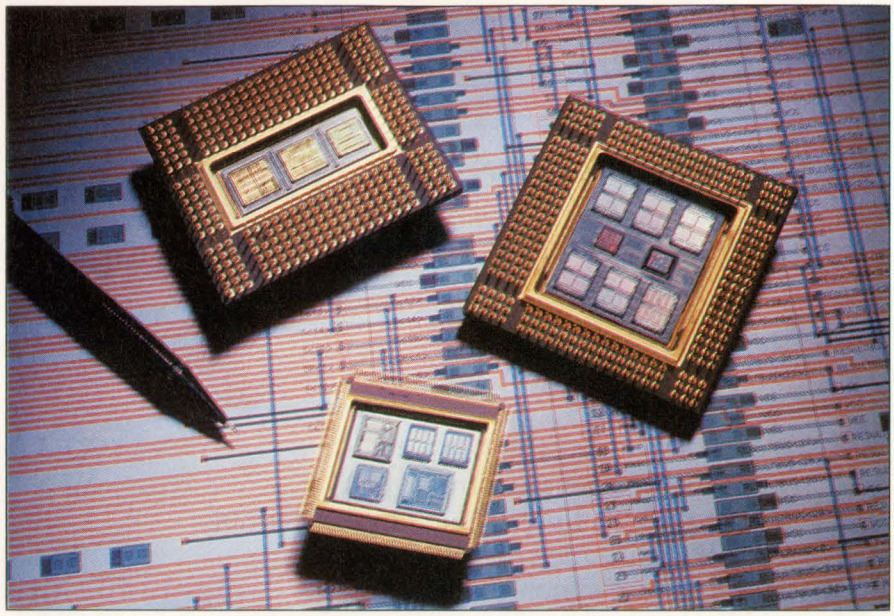
Multichip-module substrate handles 200-MHz signals and has copper interconnects

System designers are approaching a clock/transfer rate barrier for their board-level designs. Today's boards are stalling at clock rates as low as 70 MHz, as noise and transmission-line effects limit system speeds. To overcome this barrier, many designers are turning to high-speed multichip modules (MCMs)—high-density subsystems with fast substrates and packageless ICs for high-speed subsystems. MCM developers are rising to the challenge: nChip's second-generation MCM, the nC2000, can handle clock and data-transfer rates as fast as 200 MHz.

Multichip modules let designers partition systems into board-level logic and critical modules that incorporate high-speed, interlinked chips. An example of a critical module is a CPU and its cache and floating-point coprocessor. MCMs can handle these modules' critical logic speeds, thus removing the need to boost system board speeds.

Company engineers achieved high subsystem speeds on an MCM by using IC design techniques for layout and a high-speed silicon substrate instead of slower board polymers. One advantage to using silicon as a base is that these MCMs can be built by established, older, less-precise silicon foundries. Also, silicon substrates provide a high thermal conductivity as well as a thermal-expansion coefficient that closely follows that of silicon chips.

To handle fast signals and data transfers, company engineers thickened the first-generation nC1000's signal and dielectric substrate layers, thus lowering the nC2000's signal-line resistance by as much as 75%. They also added as an optional layer a resistive film for termination resistors. Engineers can use this layer to design and build in termination resistors to minimize transmission-line effects. The resistive layer eliminates the need for surface-mounted chip resistors.



The base for a new RISC multiprocessor module *from Control Data Corp (Bloomington, MN) is the nC2000 multichip module. The multichip module supports fast CMOS, BiCMOS, ECL, and GaAs ICs.*

The nC2000 MCM is built on a silicon base with individual power and ground planes, each separated by a dielectric layer. These layers have a built-in, integral decoupling capacitor with a capacitance of ≥50 nF/cm^2. These four layers are covered with a 10.5-μm-thick silicon dioxide insulator layer.

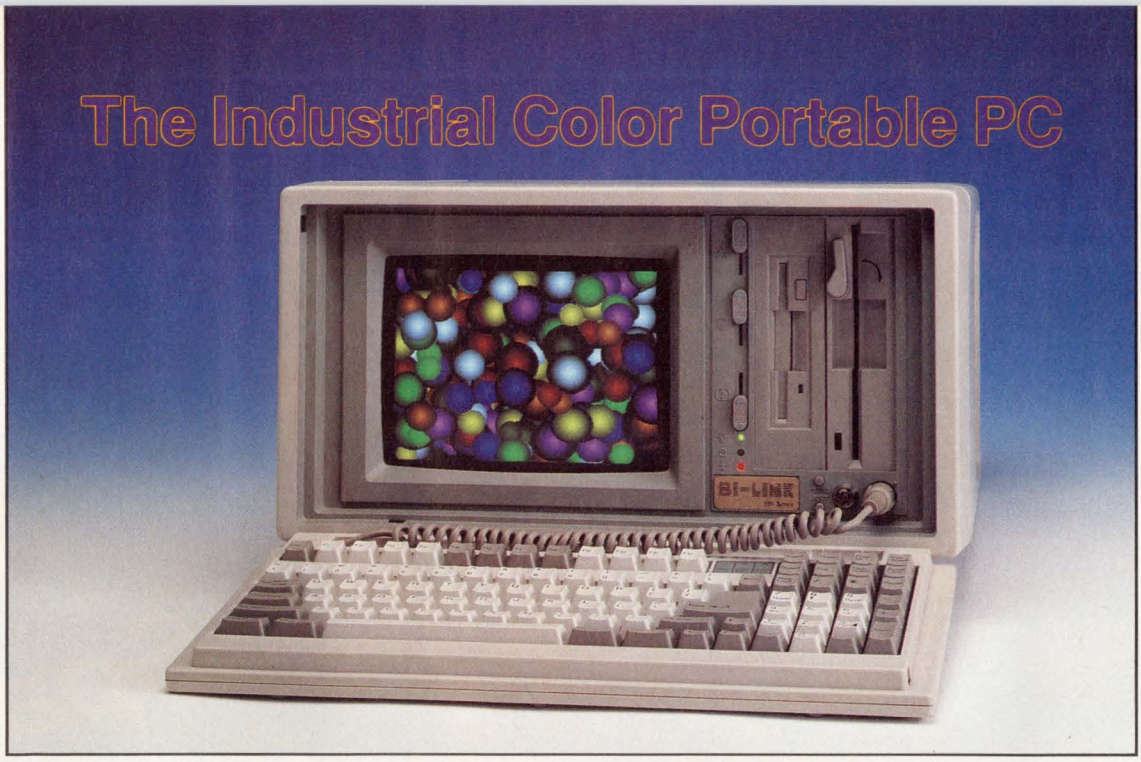
The MCM has two metal interconnect layers. These layers sit on top of the silicon dioxide insulator layer. The nC2000 has copper interconnects instead of the nC1000's aluminum traces, which have a higher resistance. The interconnect layers are 3.3-μm-thick electroplated copper. Termination resistors built into the optional resistive layer can connect to the lower metal layer. The metal layers are each covered with SiO_2.

Chip wire bonds connect to a pad layer of 0.2-μm aluminum on the top of the MCM substrate. This pad layer links to the upper metal layer. The maximum signal-wiring density is 1333 lines/in^2. The typical line propagation delay is 62 psec/cm.

nChip designers lay out and fabricate the nC2000 Silicon Circuit Board; typical design-turnaround time is 16 weeks. Prices for an nC2000 module start at $50, not including die costs.—***Ray Weiss***

nChip Inc, 1971 N Capitol Ave, San Jose, CA 95132. Phone (408) 945-9991. FAX (408) 945-0151.

The Industrial Color Portable PC



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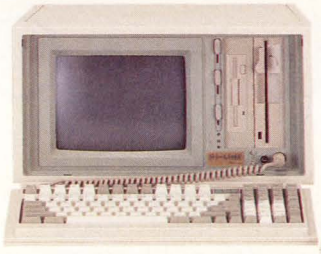

PORTABLEdesktop System
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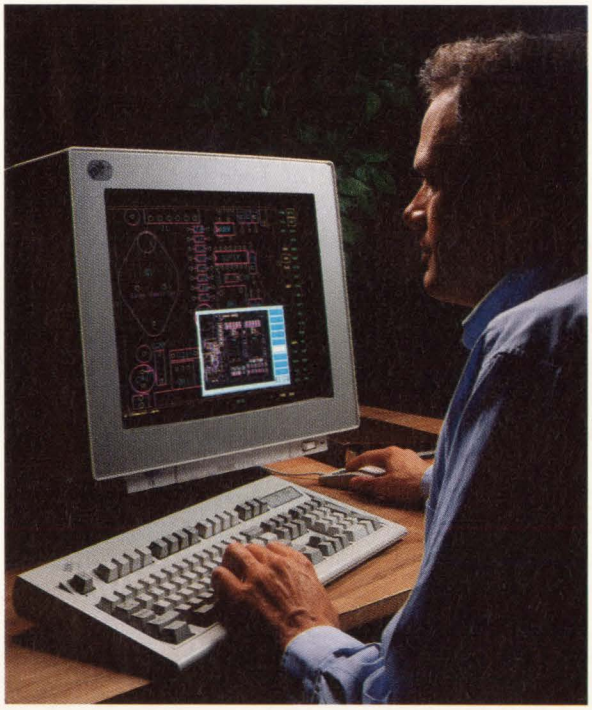

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Analog IC combines five functions for battery power management

Many system designers are extending the lifetime of their battery-powered systems by incorporating power-management logic. The ML4860 power-control IC integrates many of the analog elements needed to execute the logic's commands; it also provides voltage regulators and other power functions commonly found in battery systems. If the device's combination of power functions is not a perfect match to your system's needs, you can arrange for some modifications. The device is based on a semistandard analog array that the manufacturer can easily adapt.

The standard ML4860 chip provides the basic elements of a 100-kHz dc/dc converter and buck regulator on chip (**Fig 1**), allowing you to create a 3A, 5V regulated power supply from a 5.5 to 20V dc source. You need add only two power-switching transistors and some passive components. The voltage can come from a battery, an ac adapter, or both. When you use an adapter, the device will automatically drive an external power switch to disconnect the battery from the system.

In addition to the buck regulator, the device provides boost and linear regulators to generate a 12V and a second 5V source. The 12V source has an on/off control. You can therefore use the 12V source for in-system programming of EEPROM devices, then turn off the programming voltage to prevent inadvertent data changes.

The device supports your power-control logic by providing several control and output signals. For example, it generates a 2.5V reference and compares that signal internally against the battery. It provides a Battery Low signal if the battery voltage falls below 2.5V. It also supplies the reference signal on a separate pin.

Your power-management logic can also control the ML4860 chip. The device offers both a standby mode and a sleep mode. In standby mode, it turns off all of its functional blocks except the Low Battery indicator and the second 5V source. The sleep mode also turns off the indicator. Because the second 5V source always remains active, you can use it to power your power-management logic when you turn off the rest of the system. The device consumes 4 mA when active, but only 75 μA in sleep mode.

You will probably want to use n-channel transistors to switch power in your system because they are less expensive than p-channel types of similar resistance. Your system's power-control logic signals, however, cannot drive n-channel power transistors directly. The ML4860 has three translators for giving your logic signals the drive they need to handle n-channel devices. The output signals for battery switching and the buck regulator also handle n-channel transistors. The device comes in a 28-pin plastic leaded chip carrier and costs $4.95 (1000).—**Richard A Quinnell**

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. FAX (408) 432-0295. Contact Jon Klein.

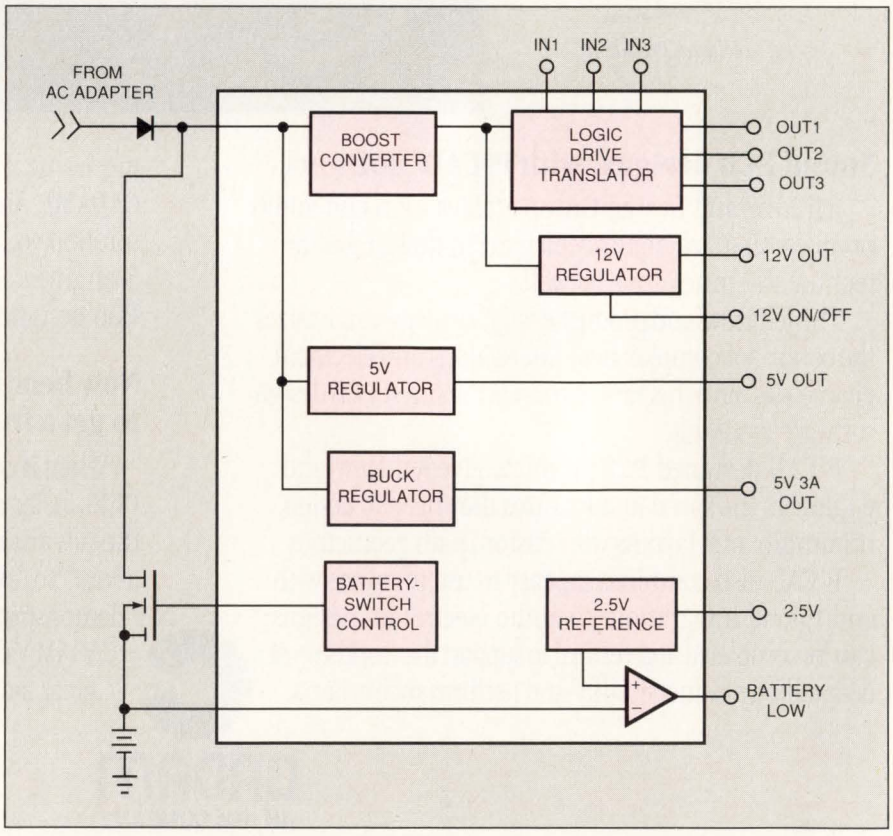

Fig 1—Systems with power-management logic still need analog circuits to execute commands. The ML4860 device combines many circuits like this in one IC.

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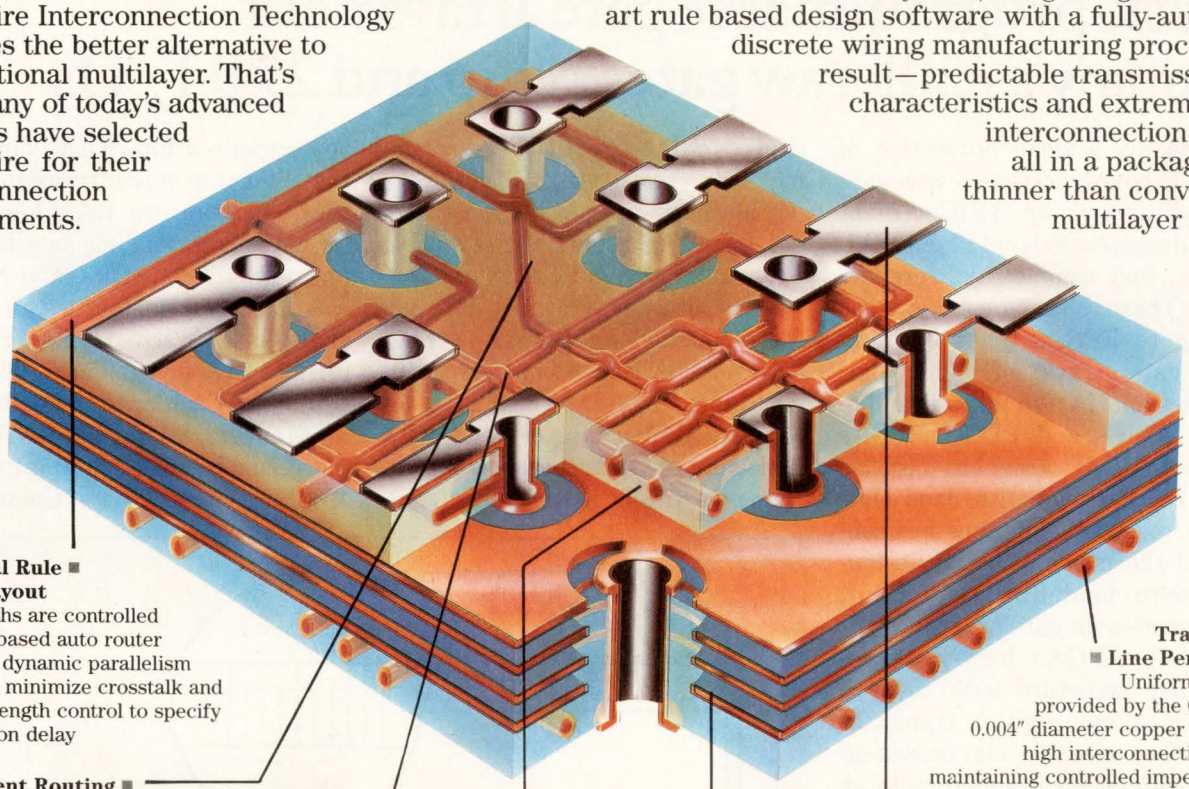

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Mask-programmable gate arrays field as many as 20k raw gates/chip and 270 I/Os

Only a small proportion of board designers use gate arrays or ASICs; most board designers rely on PLAs, PAL devices, and complex discrete devices. These board designers are turning to FPGAs (field-programmable gate arrays) for higher logic densities and I/Os to fill the gap between ASICs and PLDs. FPGAs appeal to PLD designers because of a PLD heritage with fixed logic cells. Crosspoint Solutions has considered the needs of board designers when modeling its CP20K FPGA series on gate arrays.

CP20K FPGAs have a gate-array-like structure with rows of basic gate and register transistor cells. They offer an almost sea-of-gates, gate-array granularity in an FPGA form. Taking advantage of this similarity, the manufacturer has integrated the array libraries and tools with workstation CAE tools from Mentor Graphics, Viewlogic, and Cadence. Thus, gate-array designers can switch to these FPGAs without changing tools. Even better, they can prototype their designs using a relatively low-cost FPGA, thereby minimizing nonrecurring engineering costs.

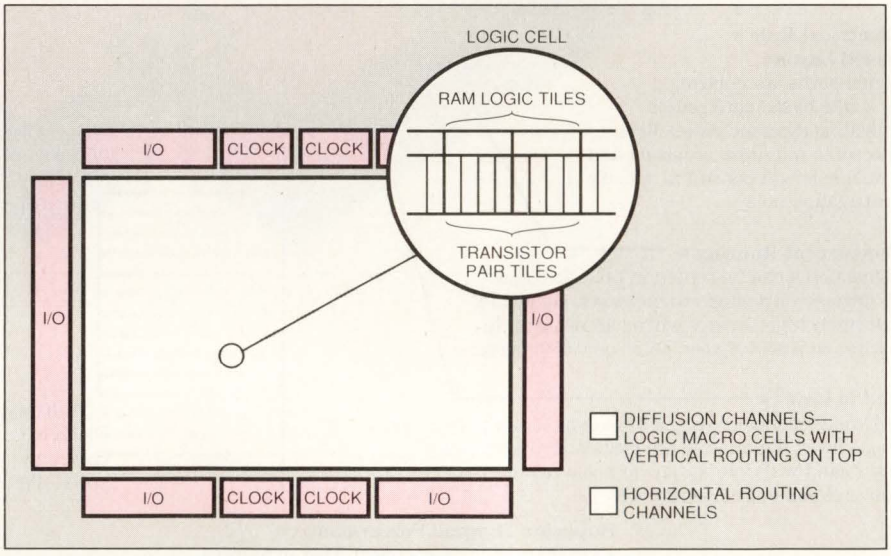
The one-time-programmable FPGAs fall below current gate-array densities and speeds. Densities range from 2.2 to 20.6k raw gates and reach clock speeds as high as 40 MHz for a counter and 52 MHz for a flip-flop driving three gate levels (fanout = 3) to another flip-flop. FPGAs are slower because of their programmable interconnections. As many as 7 million programmable interconnections may be in the large 20k-gate array, although the company expects only 3 to 5% to be programmed for a typical design. The FPGAs do, however, approach mainstream gate-array I/O counts, with available I/Os running from 91 to 270 pads.

Each array has rows of diffusion layers. A row of gate pairs overlaid with register cells constitutes a single diffusion layer. The FPGA alternates diffusion-layer rows with horizontal rows of routing resources. Lying vertically across these rows is vertical routing metal for local, as well as long routing.

Unlike most FPGAs, which have complex logic cells, the granularity of the Crosspoint cells is at the basic gate level. This fine logic granularity allows designers to work at the gate level. The array's gate transistors are ordered into transistor pairs called transistor-pair tiles, two of which make up a 2-input NAND gate. Register resources are organized into RAM logic tiles that sit on top of four transistor-pair tiles. You can use RAM-logic tiles for combinatorial logic as well, such as multiplexers, XORs, and NORs.

An innovative feature of these arrays is their structuring for register-intensive designs as well as control logic. Each array has a built-in register grid, linking the RAM-logic-tile resistor resources to a memory structure (Read, Write, Column Selects, and Data signals). Consequently, you can access any one bit independently of the transistor-pair-tile logic. This feature also makes testing easy—you can implement scan-level testing without degrading the flip-flop or logic performance.

The FPGAs incorporate a mix of logic and registers. The company projects gate utilization to range from 60 to 90+%, depending on the combinatorial logic to register/



Transistor-pair tiles (TPTs) *come from pairs of the array's gate transistors. Two TPTs make up a 2-input NAND gate. RAM logic tiles, organized from register resources, sit on top of four TPTs.*

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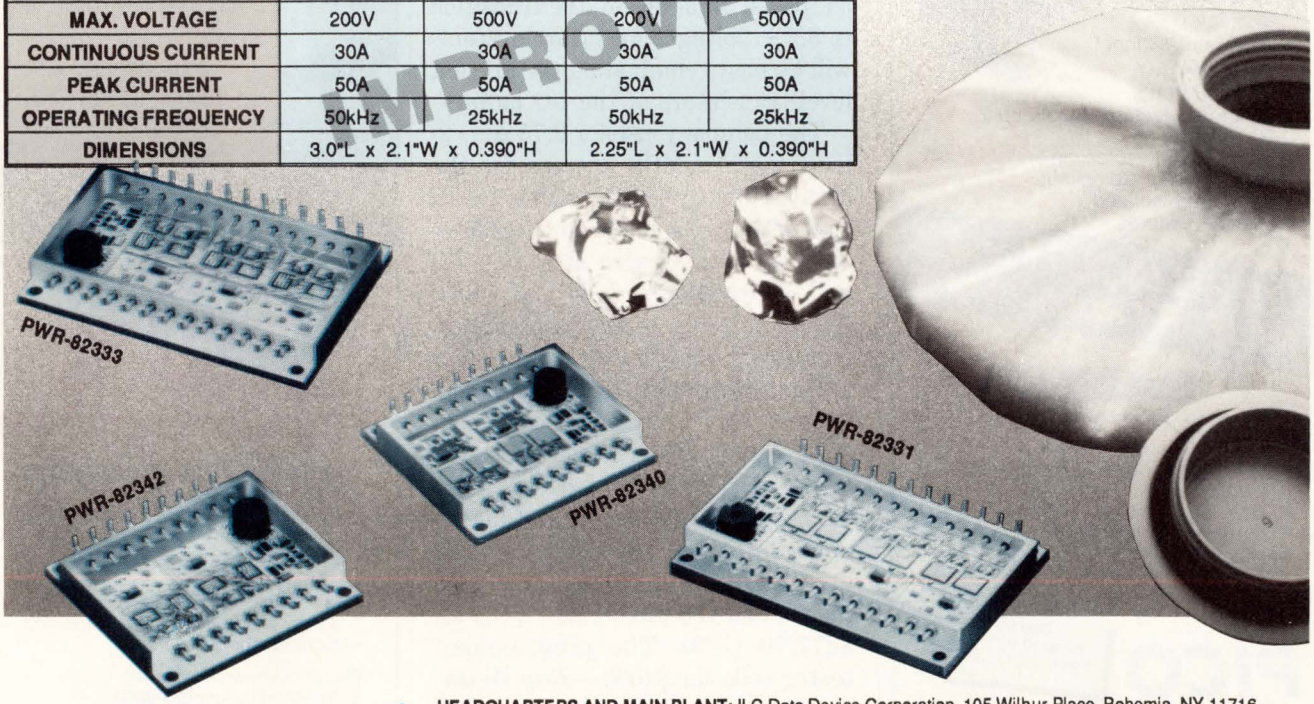
RATED POWER	4.2kW	10.5kW	4.2kW	10.5kW
MAX. VOLTAGE	200V	500V	200V	500V
CONTINUOUS CURRENT	30A	30A	30A	30A
PEAK CURRENT	50A	50A	50A	50A
OPERATING FREQUENCY	50kHz	25kHz	50kHz	25kHz
DIMENSIONS	3.0"L x 2.1"W x 0.390"H		2.25"L x 2.1"W x 0.390"H	



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memory mix. The more registers there are, the higher the density should be. A built-in clock-distribution network minimizes skew, holding it to 1.3 nsec/clock.

The manufacturer is also fielding a programmer/tester for its arrays. The device ties into the arrays via a standard JTAG (Joint Test Action Group) port, taking four I/O pins running at 20 MHz. In addition, it provides parts pretests: a simple, 2-minute programming test and a production test. A JTAG boundary scan can test the programmed part. A developmental tool set back-ends standard CAE tools. It allows engineers to interactively hand-place and route, as well as automatically place and route. The tool set handles engineering change orders, and it allows users to freeze or thaw portions of the design for rework. The set provides a delay calculator and a pin and package editor.

The FPGAs use 3.5V internal logic, mainly to support 10V programming. As a side effect, the arrays consume less power than standard 5V parts. In addition, the transition to 3.3+ voltages for future systems will be easy, eliminating the present level translators at the I/O buffers.

The company uses a 0.75-μm, 2-level metal CMOS process for the arrays. The programmable interconnection is a metal-to-polysilicon antifuse with a native R_{OFF} of 1 GΩ and a programmed R_{ON} of 100Ω. Each connection has low capacitance, measuring 0.65 fF per antifuse.

Each chip has five power and ground planes that have four decoupling capacitors. The devices come in ceramic PGAs (pin grid arrays), ceramic quad flatpacks, and plastic quad flatpacks. The CP20420 4245-gate FPGA will be available next month in a 155-pin ceramic PGA for $277.70 (100). The programmer/tester sells for $4000.—***Ray Weiss***

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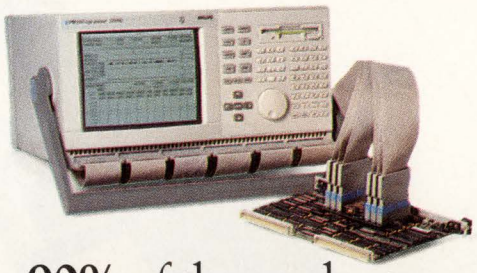

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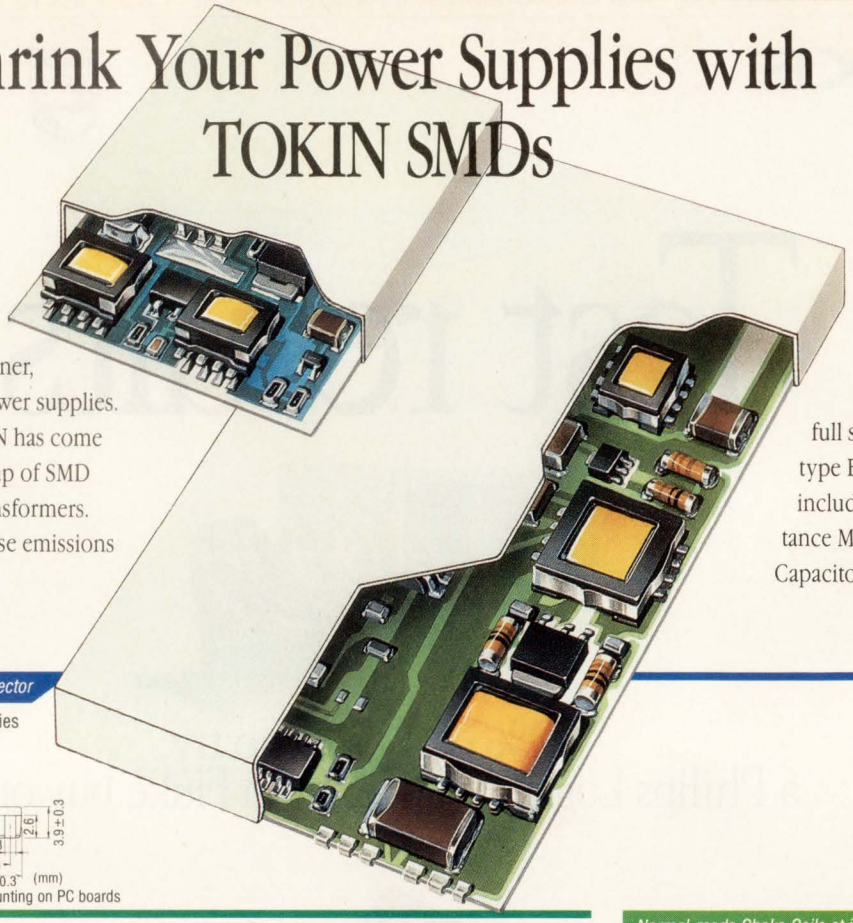

Common-mode Choke Coils at output sector

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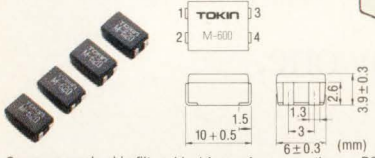

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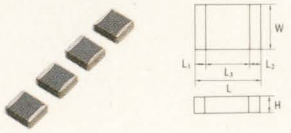

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C408 (SA)	4.0 ± 0.4	8.0 ± 0.5	3.2 max.	0.3 ~ 2.5	0.3 min.
C610 (SB)	6.3 ± 0.4	10.0 ± 0.5	4.5 max.	0.3 ~ 2.5	0.3 min.
C812 (SC)	8.0 ± 0.4	12.5 ± 0.5	4.5 max.	0.3 ~ 2.5	0.3 min.

Products above are sold only in the U.S.

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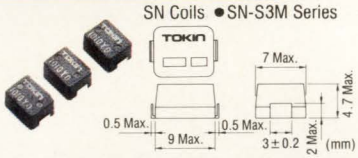

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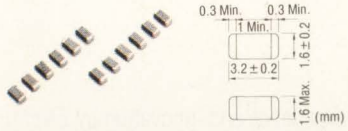

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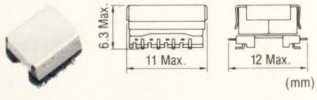
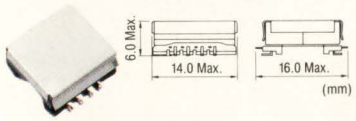
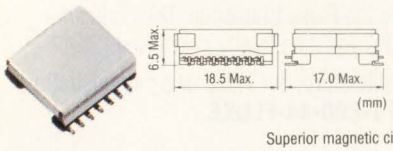


●FEY12.8/11.5

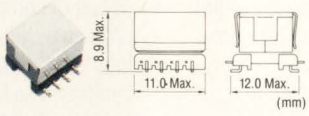


●FEY15.3/13.0

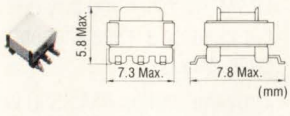


●FED11.6

●FEP7T



●FEE5



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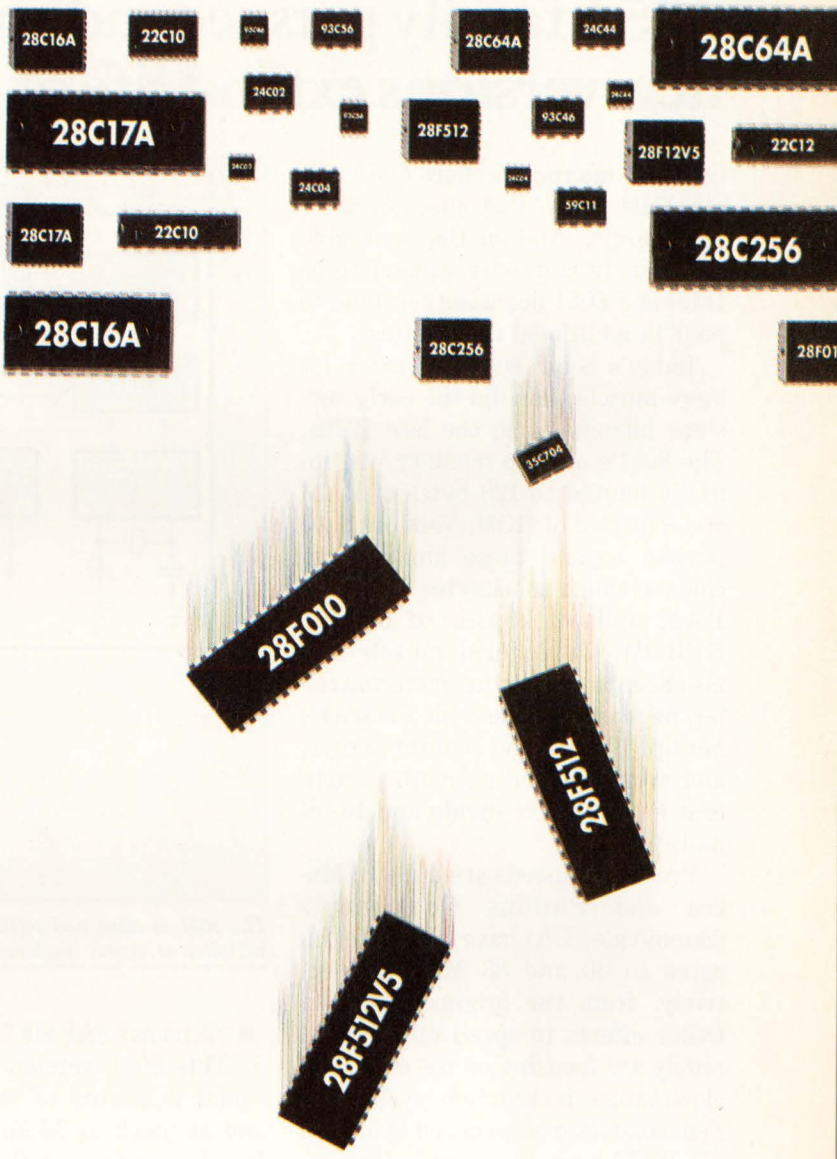

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CIRCLE NO. 72

8051 family gets second wind; new versions extend life of classic μC

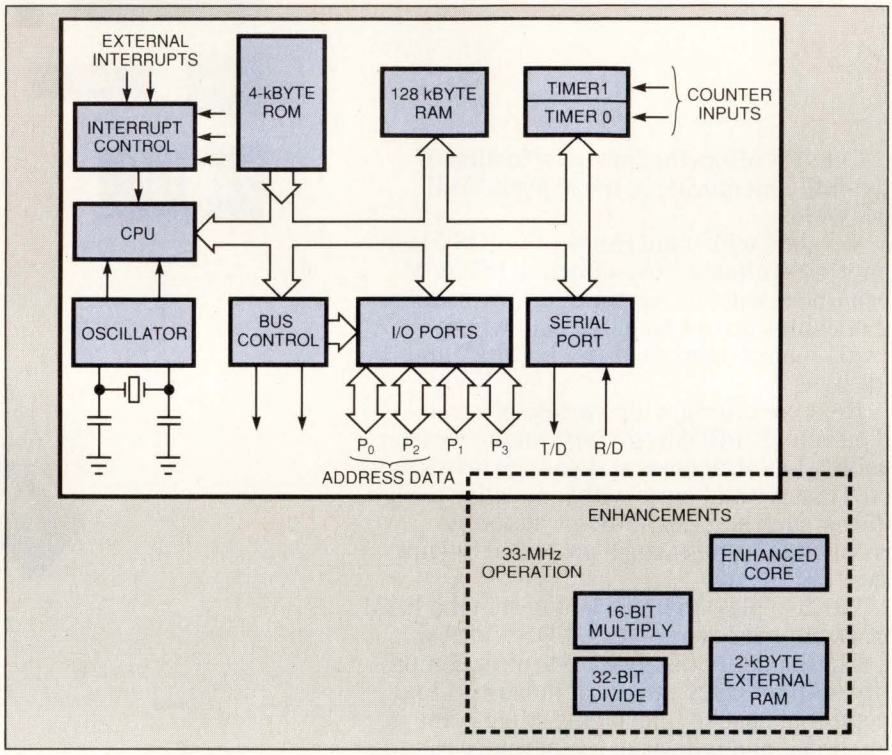
Old 8-bit microcontrollers don't quietly fade away, they just get more peripherals. And so the venerable 8051 family is quietly expanding as Intel and 8051 licensees continue to pour in additional capabilities.

Today's 8-bit 8051 carries a lot more muscle than did the early versions introduced in the late 1970s. The 8051's on-chip memory was initially limited to 128 bytes of RAM and 8 kbytes of ROM. Vendors have pushed beyond those limits to include as much as 2 kbytes of on-chip RAM and 32 kbytes of on-chip EPROM. Peripheral muscle has also been added to the microcontroller: as many as nine 8-bit I/O ports, multiple timers and counter arrays, and even a beefed-up math peripheral with a 32-bit divide and 16-bit multiply.

Processor speeds are up, too. Matra and Phillips Components (Sunnyvale, CA) have pushed clock rates to 30 and 33 MHz, respectively, from the original 12 MHz. Other efforts to speed up the 8051 family are focusing on the core's 12-clock-stage instruction cycle. Oki Semiconductor's reworked 8051, the nX 65 K series, executes instructions in four clock cycles, compared with the original 8051's 12 cycles.

New 8051 versions include

- Oki Semiconductor's one-time-programmable version of its nX 65K series. The architecture of this series is a superset of the 8051 architecture. The series has a fast core and 4, 8, or 16 kbytes of ROM and 128, 256, or 384 bytes of RAM. Prices start at $6.51 (5000). Oki Semiconductor Inc, 785 N Mary Ave, Sunnyvale, CA 94086; (408) 702-1900.



The 8051 is alive and well. *The 8-bit microcontroller unit is gaining capability through new peripherals, faster implementations, and higher clock rates.*

- Siemens's SAB/80C517A/83C517A-5. This 8051 version has an additional 2 kbytes of external RAM and as much as 32 kbytes of ROM. Its clock rate is as fast as 18 MHz. The device also has seven I/O ports, a 10-bit ADC (8 channels), six counters, eight 16-bit data pointers, a 16-bit-multiply and 32-bit-divide unit, and a 21-channel PWM. Prices start at $15 (1000). Siemens Integrated Circuit Div, 2191 Laurelwood Rd, Santa Clara, CA 95054; (408) 980-4500.

- Signetics's 83C524/87C58. This 512-byte-RAM version has as much as 32 kbytes of ROM or EPROM and runs as fast as 16 MHz. The chip includes two serial ports, three timer/counters, and the company's I^2C (Inter Integrated Circuit Bus) serial interface. Prices start at $7.50 (10,000). Signetics Co, 811 E Arques Ave, Santa Clara, CA 94088; (408) 991-2000.

- Matra's high-speed 8051s. Based on a fully static design, the 80C52, 80C32, and 80C154 now come in 25- and 30-MHz versions. The 80C154 also comes in 16- and 32-kbyte-ROM versions. The chips have three counter/timers, a full-duplex serial port, and 256 bytes of RAM. The 80C31Ω-30 costs $6 (10,000). Matra Design Semiconductor, 2895 Northwestern Pkwy, Santa Clara, CA 95051; (408) 986-9000; FAX (408) 748-1038.

And over the last year, several vendors made some significant extensions to the 8051. Intel introduced its 87C58/80C58, which has as much as 32 kbytes of EPROM, and the 87C51FX, which has a set of programmable counter functions. And Signetics pushed out more microcontroller units with its chip-level serial bus, the I^2C. This bus is part of Digital Equipment Corp's proposed Access Bus for low-speed desktop peripherals. It may become a standard.

Vendors continue to modify and extend the 8051 because of the device's popularity. Many engineers like the 8051 because of its many versions and the wide range of on-chip peripherals available. "With the 8051, if I need more power or different peripherals I can just go to another chip," says Jim Manley, director of electronic design at Span Instruments Inc (Costa Mesa, CA). Many take advantage of this prolific processor family to move to a higher-level language like C from assembly language. They pay for the additional overhead by moving to a more powerful chip.

The 8051 microcontroller has a rather baroque architecture. On one hand, it provides a complete set of processing operations including complex addressing and bit operations. The architecture provides memory-mapped I/O control.

On the other hand, Intel designers made some design compromises that complicate programming the device. For example, the 8051 has a complex addressing scheme that includes indexed, direct, and indirect addressing. But some addressing capabilities apply to only some areas, thus segregating entities that share the same address space (special-function registers share the same space as external RAM, for example). Also, bit operations are confined to an addressing set of 128 bits in local RAM.

On the positive side, the 8051 has direct bit addressing, four register sets in RAM, and a pseudo-Harvard architecture with as much as 64 kbytes each for program and data memory. On the down side, off-chip memory accesses take an additional instruction cycle, making off-chip access expensive. Competing microcontroller units, such as the Motorola 68HC11, take the same time for on- and off-chip accesses. Also, the 8051 has one 16-bit pointer, which makes off-chip addressing difficult. However, Siemens has added a set of eight pointer registers to its 80C517A.

Many engineers find the 8051 easy to learn and program, but they find its peripherals complex. Intel, for example, has gone beyond the original two counter/timers by adding more counters, a programmable counter array, and an up/down counter. Similarly, other vendors have added their own versions of advanced counter peripherals.

Designing in 8051s can be easy. Dallas Semiconductor Corp (Dallas, TX) offers an 8051 superchip, the DS5000. The device is a hybrid: Inside is an 8051 CPU, 8 or 32 kbytes of RAM, and a battery backup—in other words, a complete system.

—Ray Weiss

Intel Corp, 5000 W Chandler Blvd, Chandler, AZ 85226. Phone (602) 554-2388.

Transceiver IC handles both T1 CSU and ISDN primary-rate interfaces

The LXT310 transceiver integrates most of the elements of a T1-rate telephone channel-service unit (CSU) with ISDN primary-rate interface compatibility into one IC. The device allows you to build CSU capability into other customer premise equipment rather than having to add separate units.

The transceiver has separate transmit and receive ports, each capable of either bipolar or unipolar operation. Both ports integrate most of the active components needed for connection to the telephone network, requiring only isolation transformers and impedance-matching resistors to complete the interface. The device complies with relevant industry standards, including ANSI T1.403 and 408, FCC part 68, and AT&T Pub 62411.

The transmit port can drive signals through twisted-pair cable as long as 6000 feet. To handle shorter cables without needing tuned output circuits, the port offers selectable frequency-dependent line build-outs. You can select 7.5, 15, 22.5, or 0 dB of attenuation.

The receive port has a programmable receive equalizer. To increase noise margin in shorter loops, you can limit the maximum equalizer gain to 26 dB; otherwise, you can allow the gain to range to 36 dB. Using a status I/O pin, the receive channel reports on the line insertion loss as indicated by the equalizer gain setting.

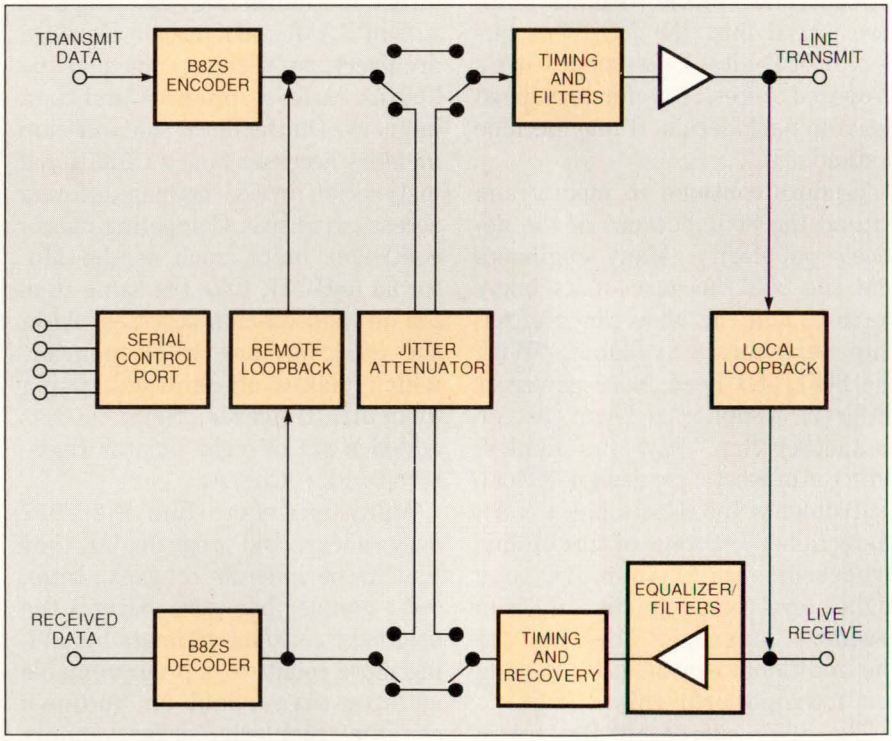
The transmit and receive channels both have selectable B8ZS encoder/decoders. In addition, the channels share a low-frequency (3-Hz) jitter-attenuator circuit. You can select which channel uses the attenuator. The attenuator stores incoming data in a FIFO register, then reclocks the data. The output clock adjusts by intervals as small as ⅛ of the clock period.

The transceiver offers several diagnostic features. For example, you can set the transmit section to produce a continuous stream of 1s at the transmit clock frequency to test the cable. You also have a choice of two loopback tests. The local loopback test routes the transmit output lines to the receive input lines, allowing you to test the entire on-chip data path. The remote loopback test routes the recovered receive data to the transmitter section so that the device acts as a repeater. You can activate the remote loopback test either at the chip or through the telephone network.

You have a choice of hardware or software methods for controlling the device. The hardware method uses hardwired control pins and coded signals on data pins to select the various operating conditions. If you prefer software control, the device offers a serial communications port for exchanging commands and status information.

The LXT310 operates from a 5V supply and typically consumes 300 mW. It comes in a 28-pin PLCC (plastic leaded chip carrier) and ceramic and plastic 28-pin DIPs. Prices are $30 to $33, respectively (1000). ***—Richard A Quinnell***

Level One Communications Inc, 105 Lake Forest Way, Folsom, CA 95630. (916) 985-3670. FAX (916) 985-3512.



Packing most of a channel service unit (CSU) into one IC, *the LXT310 allows you to embed CSU capability into other types of equipment.*

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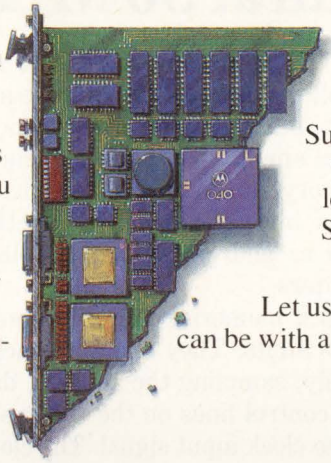

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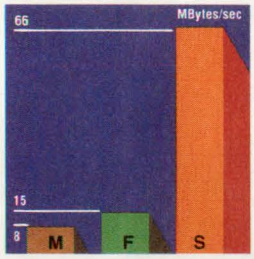
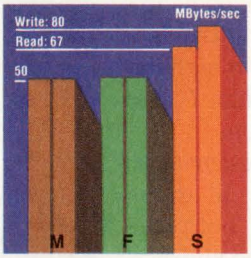


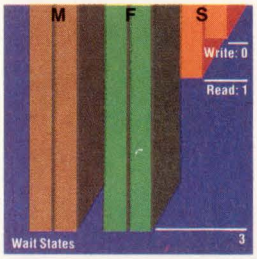
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



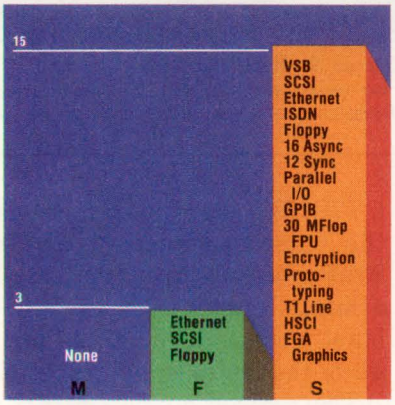
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



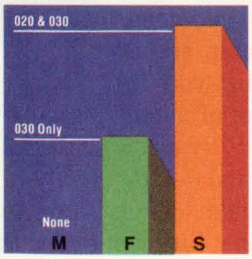
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



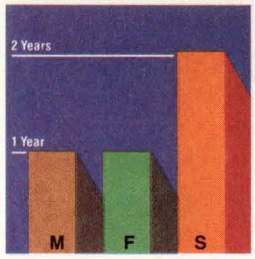
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



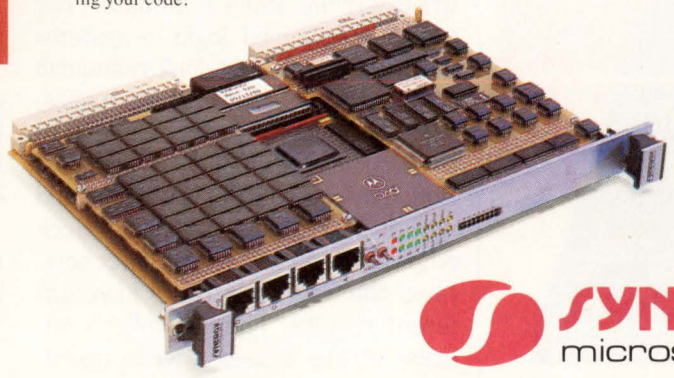
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. I. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

CIRCLE NO. 76

Synchronous cache RAMs run at 50 MHz

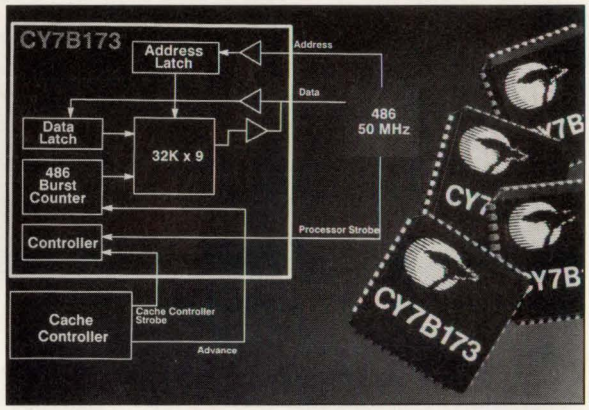
The CY7B173 and CY7B174 synchronous cache RAMs operate at 50 MHz, but they offer more than just high speed. To simplify cache-memory subsystem design, the devices incorporate logic functions such as address latches and burst counters.

Both memories are organized as 32k × 9 bits. They operate synchronously, sampling the address, data, and control lines on the rising edge of the clock input signal. The clock's minimum cycle time is 20 nsec, allowing operation at 50 MHz. Only the output-enable line operates asynchronously, setting the data output lines to high impedance within 7 nsec of de-assertion.

For the memories to respond to a given clock cycle, both the chip select and address-strobe lines must be properly asserted. The devices have two complementary chip select lines, allowing you to use two banks of memory in your system without external decoding logic. The devices also have two address strobe lines: one for the system processor and one for the cache controller. Having two address strobe lines eliminates the need for external logic in systems with processors that don't relinquish control in the event of a cache miss.

Both address strobe lines have the same effect during a read operation. The data output becomes valid within 14 nsec of the rising clock edge. For write operations, however, the address strobes have different results. The controller's address strobe causes a write operation to complete in a single clock cycle. The processor's address strobe, however, causes the memory to delay one clock cycle before completing the write operation. This delay lets cache-tag RAM or other logic time identify a cache miss and prevent the write operation if necessary. If both address strobes are active, the processor address strobe takes precedence.

The memories support burst access for read and write operations by supplying an address latch and a built-in burst counter. The CY7B173 has a counter that follows the burst sequence of the Intel 80486 processor. The CY7B174 offers a linear counter. You can use the burst mode with either the processor or the controller address strobes.



***Running as fast as 50 MHz**, the CY7B173 and CY7B174 cache RAMs also speed system design. The devices include data latches, burst counters, and other design-simplifying logic on chip.*

The devices operate at 5V and consume 250 mA. They come in 44-pin PLCC (plastic-leaded-chip-carrier) packages and cost $69 (100).

—Richard A Quinnell

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. FAX (408) 943-2741.

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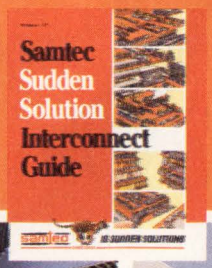

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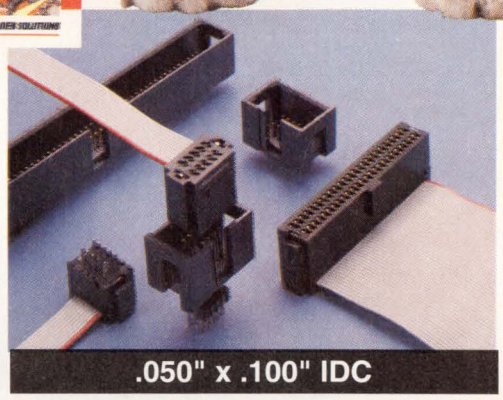

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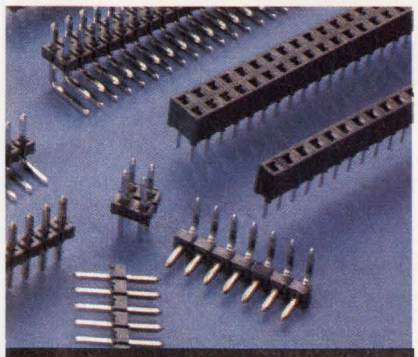

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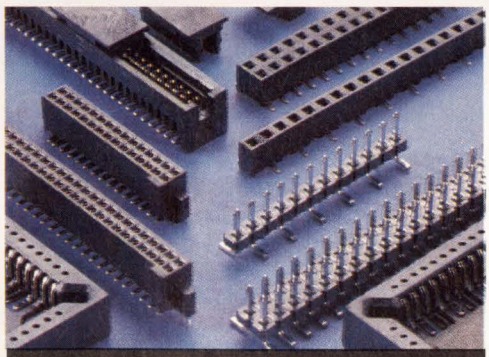
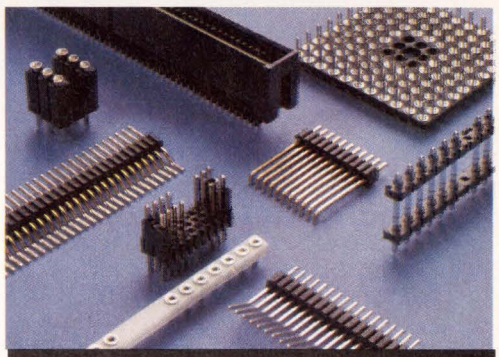


SURFACE MOUNT



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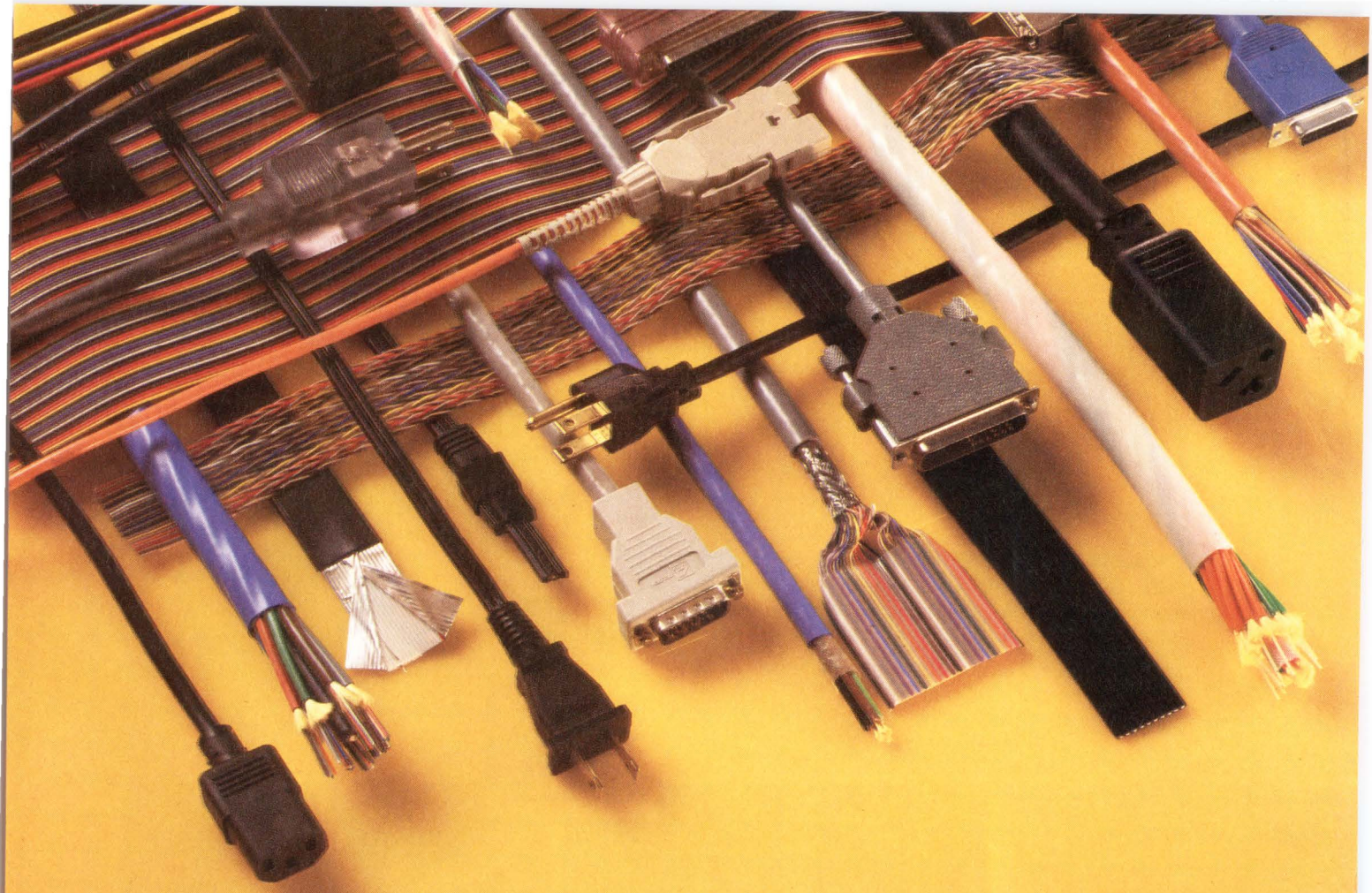
CIRCLE NO. 78



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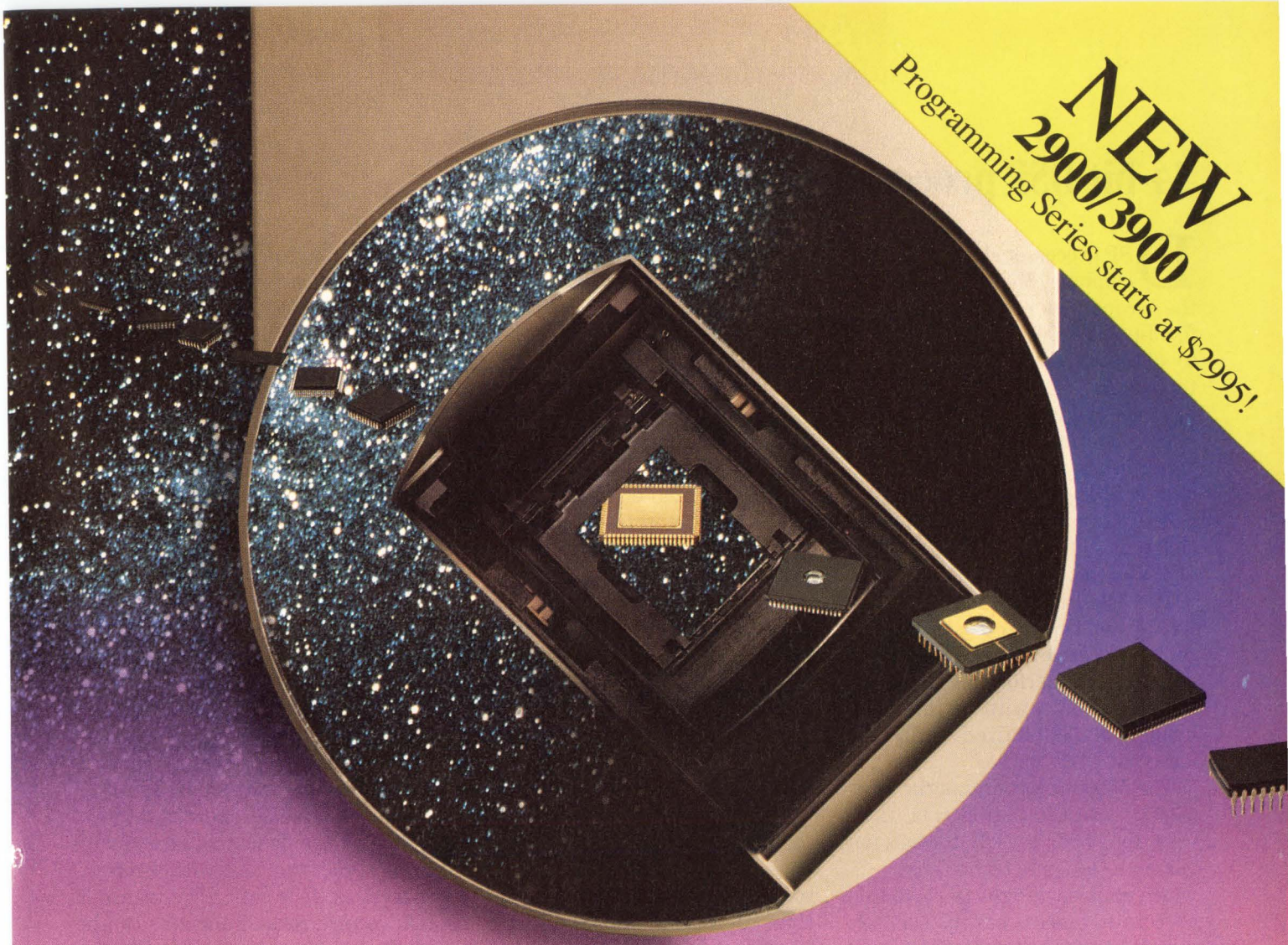

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CIRCLE NO. 80

DATA I/O

24-bit DSP processor runs at 40 MHz

DSP processor clock rates are climbing. Motorola's 56002 is the second generation of the 24-bit, fixed-point 56001. The 56002 runs to 40 MHz, whereas the 56001 topped out at 33 MHz; this speed increase yields an improved performance of more than 20%. The 56002 peaks at 20 MIPS and 120 million operations/sec: it performs a MAC (24-bit add and multiply, result to 56-bit accumulator) with X and Y data transfers.

The 56001/2 is the only 24-bit, fixed-point DSP processor currently available. It provides higher accuracy and performance than basic 16-bit DSPs, without the larger memory of a 32-bit fixed- or floating-point DSP.

The 56002 incorporates the 56001's core and peripherals. However, the 56002 uses Motorola's universal-design-rule technology, which enables designs to move from process to process easily. The current implementation is on 1.0-μm CMOS but eventually will be moved to 0.8-μm CMOS. The design is fully static with clocks to dc frequencies. The PLL is programmable with a clock multiple to 4096.

Motorola added on-chip-emulation features of the 32-bit 96002 to the 24-bit DSP. Using on-chip emulation, designers can debug their application code, controlling the DSP processor via a 6-wire serial interface. Thus, engineers can opt to start and stop the processor, set breakpoints, and monitor and change memory and register values. Breakpoints trigger on program or data access, either addresses or address ranges. On-chip-emulation features include a breakpoint or pass counter to trigger a breakpoint on the *n*th compare iteration; the features also furnish a trace counter, specifying the number of instructions to be executed for each trace step.—**Ray Weiss**

Motorola Inc, Microprocessor and Memory Technologies Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-2000. FAX (512) 891-2652.

56002 DSP processor

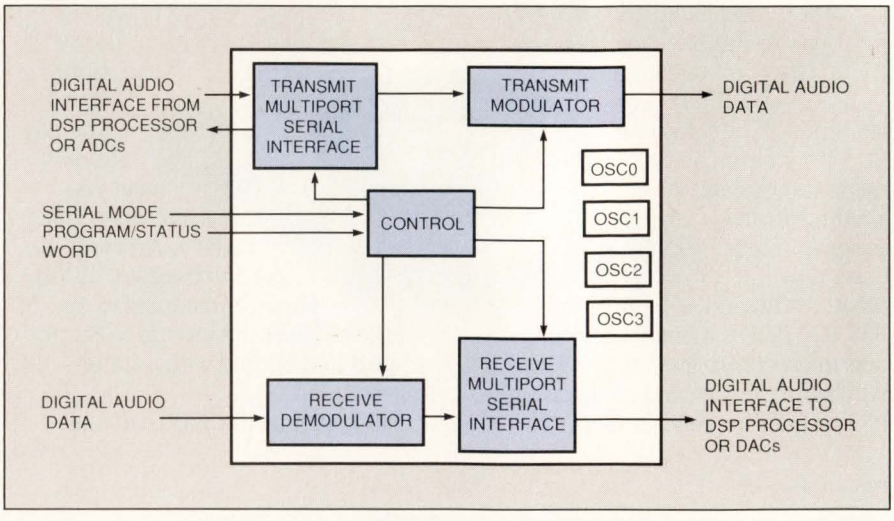
Clock	to 40 MHz internal (PLL input, to 4096×)
Instruction cycle	2 clock cycles, 50 nsec
Registers	2 24-bit; 2 56-bit accumulator
Address space	3 64-kbyte×16 bit: program, X, Y
On-chip memory	512×24-bit ROM (Instruction) 2 256×24-bit RAM 2 256×24-bit ROM
Arithmetic	56-bit ALU (24-bit logic) 48-bit multiply (24×24)
Interrupt	3 external interrupts
I/O	24 pins
Serial	asynchronous serial interface synchronous serial interface A/D, D/A, AES/EBU
Other	automatic loop control, on-chip emulation, host and DMA interfaces
Package types	132-pin pin-grid array or plastic quad flatpack
Price	$79 (sample qty)

Chip links DAT devices and DSP μPs

Digital audio brings the ease and interchangeability of today's plug-in audio jacks. Motorola's single-chip digital audio chip, the DSP56401, links DAT (digital audio tape) devices to DSP processors. The chip acts as a transceiver to multiple digital-audio devices, linking them directly to DSP56001/2 DSP processors.

The device meets the AES/EBU and EIAJ CP-340 digital-audio standards. It takes in unidirectional, self-clocked, stereo digital-audio formats in a single serial channel. It acts as a DAT transmitter and receiver and contains a transmit serial interface, transmit demodulator, receive demodulator and a receive serial interface with a common clock generator. The transmit and receive serial interfaces can be clocked independently if needed. The hardware implements preamble detection and synchronization, parity and CRC checks, and block and frame synchronization.

A phase-locked loop (PLL) detects and recovers the bit clock from the modulated serial input. For



With this single-chip digital-audio transmitter/receiver, you can link DAT devices to DSP processors, ADCs, and DACs.

transmission, a modulator state machine generates the preambles, parity, and CRC data incorporated in the transmitted frame with audio and nonaudio data. DAT transmission uses the LSB-first, biphase-mark Manchester decoding for transmission and receive. Multiple DAT devices interface to a single DSP56401. Combined with the DSP56001/2, it provides two chips for processing DAT applications.

In addition, the chip interfaces directly to Motorola D/A and A/D converters. The chip includes four oscillators and a jitter clock recovery system.

The DSP56401 comes in a 64-pin plastic quad flatpack and costs $25 (sample qty). An evaluation board is available from Spectrum Signal Processing Inc (Burnaby, BC, Canada). This 5 × 5.75-in., 4-layer board includes DAT input/output ports as well as ports to the DSP56001/2 and to audio converters such as those made by Burr-Brown. Audio connectors for AES/EBU optical lines, balanced-line XLR connectors, and unbalanced RCA connectors are also available.—**Ray Weiss**

Motorola Inc, Microprocessor and Memory Technologies Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-2000.

80C51 family hits 33-MHz clock rates

Memory costs—especially for high speed parts—are a major limiting factor for embedded systems. Signetics has raised 8051 clock rates to an unprecedented 33 MHz and held down memory access time, keeping memory costs down as well. Other 8051 vendors such as Matra MHS and Siemens are supplying 30-MHz parts.

Two 80C51 family members, the 80C51 and 80C52, run at rates to 33 MHz but require only a 90-nsec memory access time for external memory. As designers moved clock rates out, they recharacterized the parts, reducing interface requirements and gradually improving process upgrades.

The 8051 architecture is designed for both single-chip and external-memory applications. An 8051 supports a single 64-kbyte external address space or two 64-kbyte address spaces: one for instructions and one for data. External references are slower than referencing internal RAM; they must go through the accumulator and take extra cycles. The 80C51 and 80C52 differ in their amounts of scratchpad RAM and on-chip ROM: The 80C52 doubles 80C51 RAM and ROM to 256 bytes of RAM and 8 kbytes of ROM.

An 8051 takes 12 external clocks (6 internal clocks) for an instruction cycle, which includes an instruction and a potential data fetch. At 33 MHz, a base instruction takes 360 nsec. The instruction access time for external memory is specified at 90 nsec, which under previous specs would have been 60 nsec.

Recharacterized 80C51 timing results in memory access times that are lower across the entire line: a 24-MHz 8xC51 now uses a 120-nsec memory, compared with 90 nsec previously required.—**Ray Weiss**

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000. FAX (408) 991-2311.

The 80C51/52 family

Clock	3.5 to 33 MHz
Instruction cycle	12 clocks
Memory	128- to 256-byte scratchpad, 4- or 8-kbyte 64-kbyte instruction address space 64-kbyte data address space
Timers	2/3 16-bit timers
I/Os	Four ports: 32 lines
Interrupts	2 external
Package types	40-pin DIP, LCC, 44-pin quad flatpack
Price	$3.50 (10,000); $17.50 for one-time-programmable version (1000)

Workstation brood adds low-end machine and servers

An entry-level workstation, four servers, and two high-end, 24-plane graphics boards expand the utility of the HP 9000 Series 700 family of PA-RISC-based workstations. The Series 700 Model 710 has an entry-level price of $7490 and delivers 49.7 SPECmarks, 57.9 MIPS, and 12.2 Mflops from its 50-MHz CPU. These metrics contrast with the $11,990 Model 720, whose performance of 59.5 SPECmarks, 57.9 MIPS, and 17.9 Mflops represents a compiler-enhancement-based improvement from its introductory numbers. Two mechanisms that reduce price and improve performance of the Model 710 workstation are the smaller caches: the 32-kbyte instruction cache and 64-kbyte data cache are from one-quarter to one-half the size of those of the other family members.

The base machine comes diskless, with 16 Mbytes of memory, graphics supporting eight image planes, and a 19-in., 1280 × 1024-pixel-resolution gray-scale monitor. Graphics options allow you to configure the machine with color monitors: a 16-in. 1024 × 768-pixel monitor ($4000) or a 19-in. 1280 × 1024-pixel monitor ($6500). All three graphics options are integrated into the CPU and utilize hard-coded graphics primitives to achieve 7292 X11 performance and 950,000 2- or 3-D vectors/sec. Integration onto the CPU is another cost-saving feature.

You can add as much as 840 Mbytes of internal disk storage in four half-height slots or 9.4 Gbytes using external disk arrays. The low-end workstation also supports 1.44-Mbyte, 3½-in. floppy-disk drives, CD-ROM storage, or 2-Gbytes of 3.5-in. DDS (direct-digital-synthesizer) tape. You can also increase your main memory from 16 Mbytes to as much as 64 Mbytes, using error-correction code SIMMs.

The four servers come in four configurations ranging in price from $23,440 to $87,638. The servers enhance network capacity via an internal disk capacity of as much as 2.6 Gbytes and an external capacity of 236 Gbytes. All servers offer two 8-Gbyte, 4-mm DAT (digital-audio-tape) drives and a 600-Mbyte CD-ROM. You can stuff the main memory with 32 to 384 Mbytes of RAM.

The existing workstation family previously offered three graphics choices. These choices featured circuit boards with 8-plane gray-scale or color and a board with as many as four i860 CPUs.

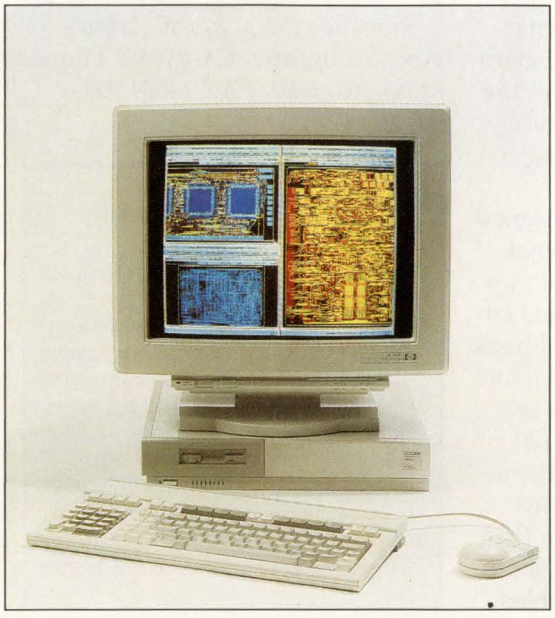
Two new boards for the higher-end 720, 730, and 750 workstations are called the CRX-24 and CRX-24Z. They provide a 24-plane single buffer or 12 + 12-plane double buffer and offer eight overlay planes for additional storage. The CRX-24Z supplements the features of the CRX-24 with a hardware Z-buffer, accelerated shading, and antialiasing.

Because both boards operate at greater than 30 frames/sec, they both support video. These two graphics options range in price from $13,500 to $21,500. A $2000 software product called Power Shade adds shading capabilities to the existing graphics products or to the new CRX-24; it comes with the CRX-24Z.

In contrast to the relative dearth of software vendors committed to the Series 700 at introduction, HP announces that almost 2000 applications are possible on the workstations today.

Prices are not yet firm and could be lower than quoted. All products are available except for the graphics boards, whose delivery takes four to eight weeks ARO.

—Michael C Markowitz
Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.



Extending the low end of its RISC-based workstation line, Hewlett-Packard's Series 9000 Model 710 runs at almost 50 SPECmarks.

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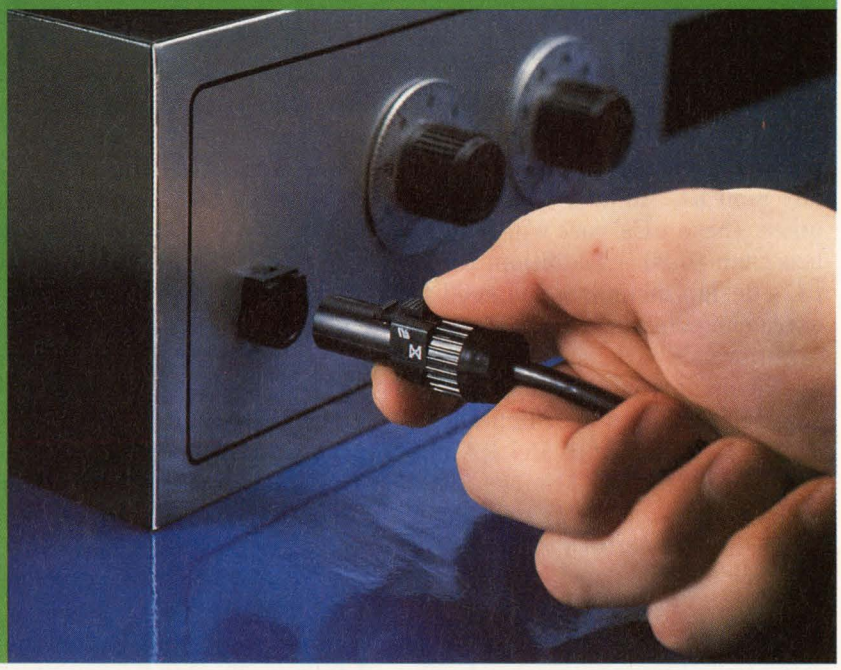

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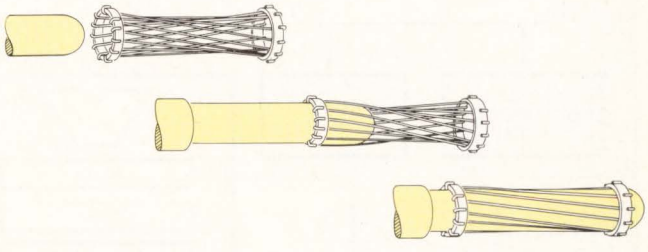

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8-bit 68HC05K microcontroller minimizes cost and fits in 16-pin DIPs and SOICs

Engineers who need to watch their design pennies will like a low-end version of the Motorola 68HC05 8-bit microcontroller (μC). The 68HC05K series brings the μC's architecture down to a 16-pin DIP, the smallest pin package for any 8-bit μC. In large OEM volumes, these μCs' cost will fall to less than $0.90. In addition, the μC's design minimizes the need for extra components.

Motorola's 68HC05 is a simple μC with a single accumulator and index register. It comes with limited on-chip ROM or EPROM and RAM, typically with 2 to 4 kbytes of ROM and 176 bytes of RAM. It has no provisions for accessing off-chip memory and has four 8-bit I/O ports and a counter/timer system.

The series takes the 68HC05 architecture down another level. Although it has the standard 6805 processor core, the 68HC05K's peripherals have been cut back. It has two I/O ports—one has eight and one has two I/O lines. On-chip memory has been reduced to a 1-kbyte address space, with 504 bytes of ROM or EPROM (including eight interrupt vectors) and 32 bytes of RAM. A new μC option is a 64-bit personality EPROM, which holds version or design data.

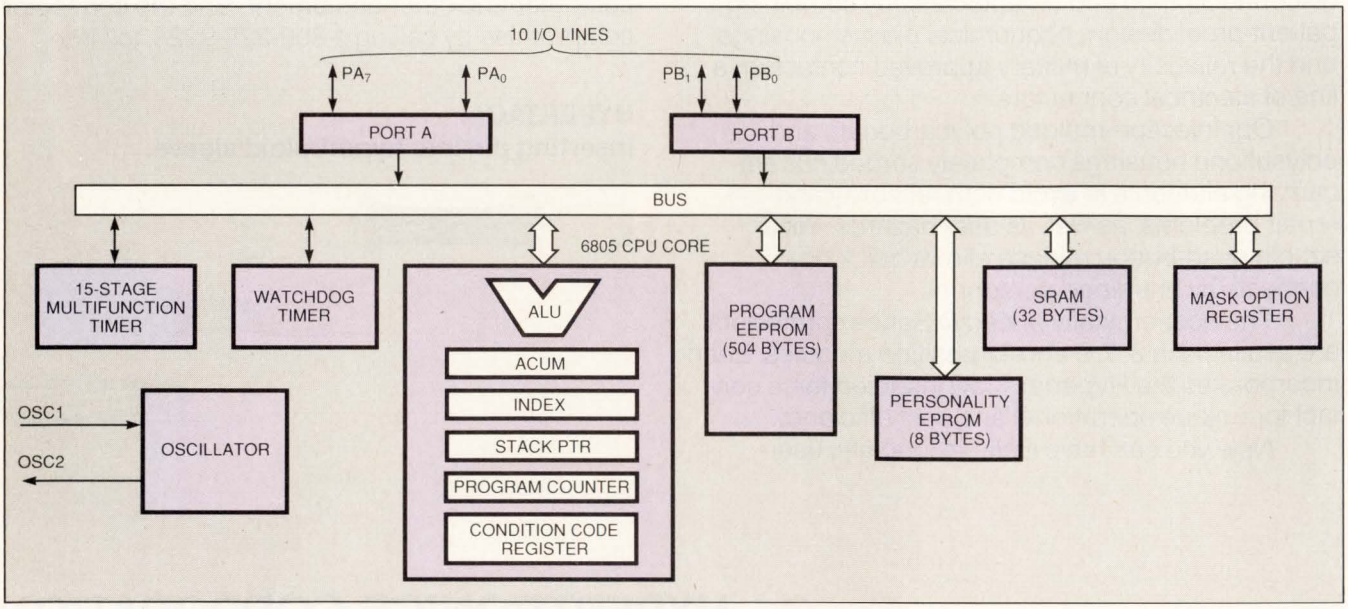
Reduced stack-pointer size is a result of the series' limited addressing space. The μCs have a reduced, multifunction 15-stage timer. A programmable watchdog timer catches runaway software. Both watchdog-timeout and timer-overflow conditions trigger interrupts.

The μCs feature the standard IRQ external-interrupt line as well as a programmable option for four I/O lines. The I/O lines can be ORed to IRQ, creating five external-interrupt sources. The μC series runs with a 4-MHz external oscillator or clock; internal clocks are 2 MHz divided down from the rate.

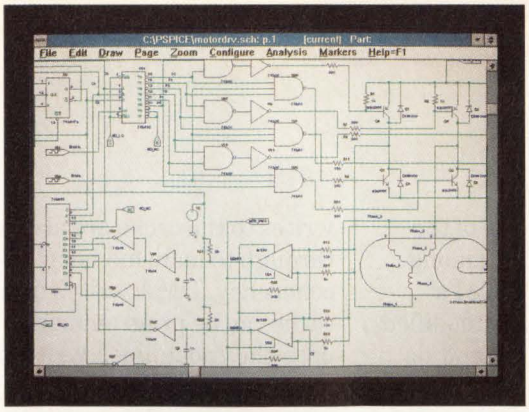
Three new μCs enlarge the 68HC05K family: the base level 68HC05K0; the 68HC05K1 with personality EPROM; and a one-time-programmable 68HC705K1 with EPROM.

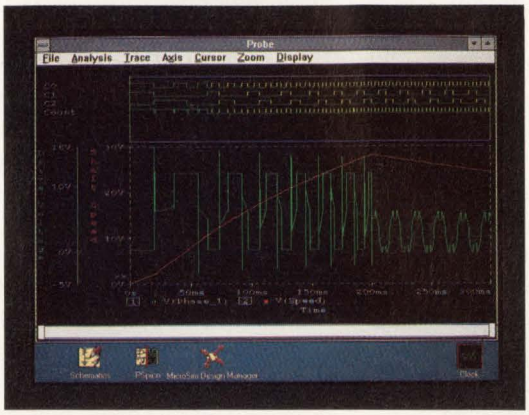
To save external components, four of the I/O lines can sink 4 mA to drive LEDs directly, eliminating drivers. Port I/O pins have software-programmable pull-down resistors (100 μA), eliminating external pull-down resistors.

Shortly, the company will introduce a new PC-based integrated-development-software package for the 68HC05K. Developed by P&E Microsystems (Woburn, MA), the package includes a macro assembler, an editor, a simulator, and a



This low-end, 8-bit μC family, the 68HC05K microprocessor series, has a 1-kbyte address range with 504 bytes of ROM or EPROM and 32 bytes of RAM. The series also has a reduced set of peripherals and 10 I/O pins.





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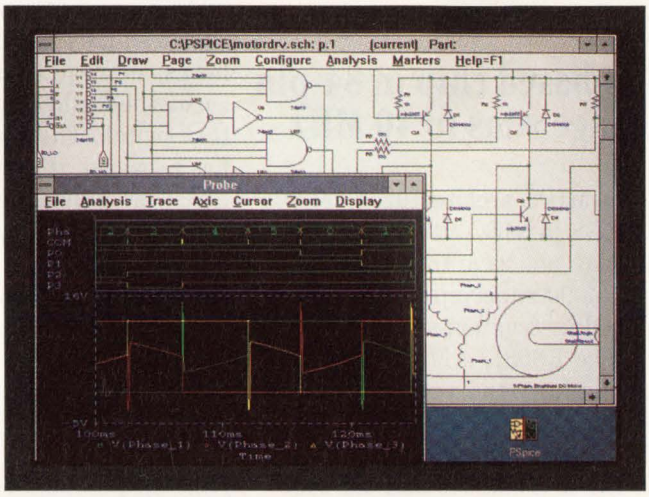

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windowed source-code debugger, all combined in an integrated environment.

The low-end 68HC05 parts cost $1.20 for the 68HC05K0, $1.85 for the 68HC05K1, and $2.75 for the one-time-programmable 68HC705K1 (10,000). Samples of the chips are available now.

—**Ray Weiss**

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr, Austin, TX 78735. Phone (512) 891-3434.

MIPS-based chip in 84-pin package runs to 40 MHz

The MIPS-architecture-based ACE, a RISC alternative to PCs, may not have to wait for the Mips R4000 superpipelined RISC (reduced-instruction-set computer) chip. The R3081, a MIPS-based chip, is a high-end version of IDT's R3051/2 family of embedded RISC CPUs. The R3081 is compatible with the Mips R3000 and can run the emerging Microsoft Windows/NT operating system, the core of the ACE (advanced-computing environment) architecture, and Unix. R3081 clock rates run from 20 to 40 MHz.

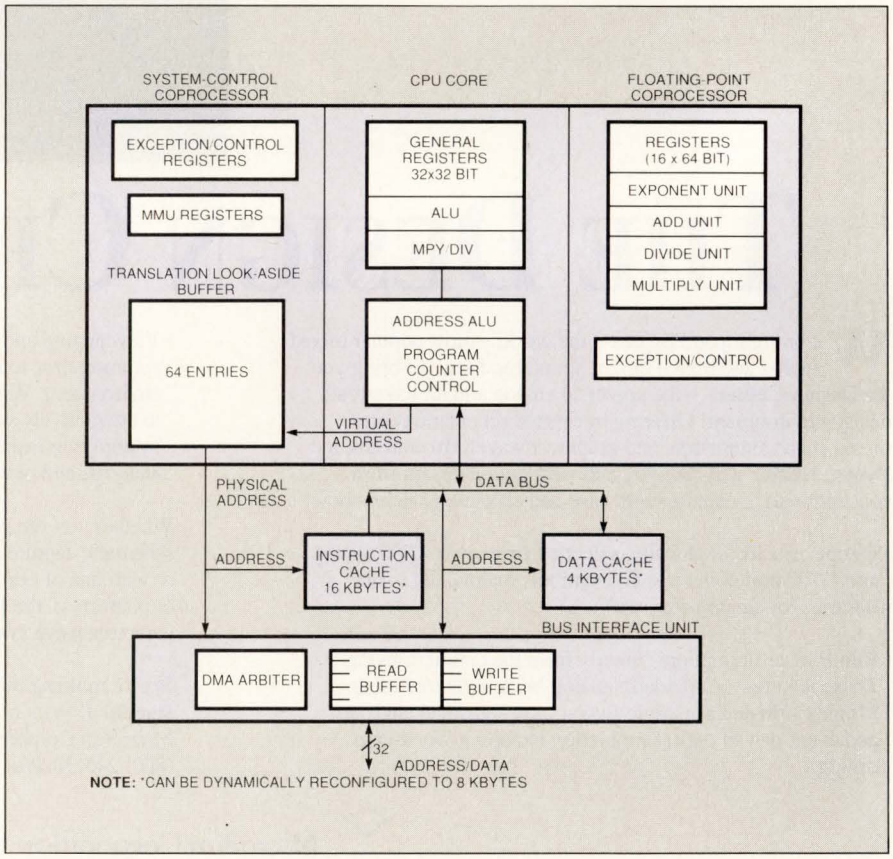
IDT has solved some of the design obstacles of the original Mips R3000 architecture. For example, the R3081 incorporates a 16-kbyte instruction cache and a 4-kbyte data cache, eliminating the R3000's need for sequential accesses to two caches in a single cycle. Also, the chip has a simple, minimal glue logic interface and uses standard dynamic RAMs (DRAMs) instead of more-expensive static RAMs (SRAMs). The chip integrates an FPU on chip, saving board space and wiring.

The R3081 is pin compatible with earlier R3051 CPUs; existing designs can be upgraded without redesign. The R3081 has one of the largest instruction caches among RISC processors. The R3081's caches can be dynamically modified to an 8-kbyte instruction and data cache configuration, creating a more-balanced configuration. Thus, the operating system can configure the hardware for large-scale applications; the only limitation is that the caches must be flushed before reconfiguring them.

The R3081 caches are direct mapped (only one cached item per address) and are physically, rather than virtually, addressed. This relieves the requirement that virtual caches be flushed on a process context switch. The instruction cache has a 4-word, 16-byte line size (smallest cached element is four words). The data cache has a word or 4-byte line size. The R3081 has a write-through cache policy—writes to the cache are also written through to main memory. For cache coherency, DMA writes from the cache can be programmed to invalidate the cache lines written, eliminating potential data conflicts (the main memory data now is the valid data).

Like the R3051, the R3081 CPU uses a multiplexed address and data bus to help minimize pin count. This approach does not markedly hamper CPU-memory performance: It shifts from address to data in ½ a clock cycle and has read/write buffering. With fast enough DRAMs, reads can take two memory cycles, and writes two or three cycles, depending on decode-logic times. The multiplexed bus does, however, require external logic to latch the address and hold it during the data-presentation phase of a memory cycle.

IDT designers improved CPU



The latest IDT revision of the MIPS RISC architecture, the R3081 combines large on-chip cache with an FPU and a multiplex bus, fitting a small-package IC.

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performance by adding read and write buffers. These 4-word-deep read and write buffers allow the CPU to continue processing: Writes are buffered for later execution and burst or block reads can be picked up independently of the CPU.

In addition, the R3051 and R3081 support DMA for peripherals (the DMA takes over the CPU's external bus). Also, the bus interface has been improved with a higher drive, clock output, a half-frequency bus operation option (to have memory bus speeds relative to the CPU bus rates), and a slow bus turnaround feature that eliminates 3-state contention problems for external memory reads followed by writes. The 20-, 33-, and 40-MHz parts cost $98, $146, and $196, respectively, (10,000). Samples of the R3081 will be available in March.—**Ray Weiss**

Integrated Device Technology Inc, 3236 Scott Blvd, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674.

4-bit microcontroller supports 16 kbytes of EPROM and 1k nibbles of static RAM

Engineers shouldn't treat 4-bit (1-nibble) microcontrollers (μCs) as outdated technology. Four-bit μCs are alive and kicking. In fact, they're busy attacking the low end of the 8-bit μC market with specialized peripherals. A 4-bit μC, the μPD75P316A, combines 16 kbytes of EPROM with low power consumption, direct drive for LEDs, and an LCD controller.

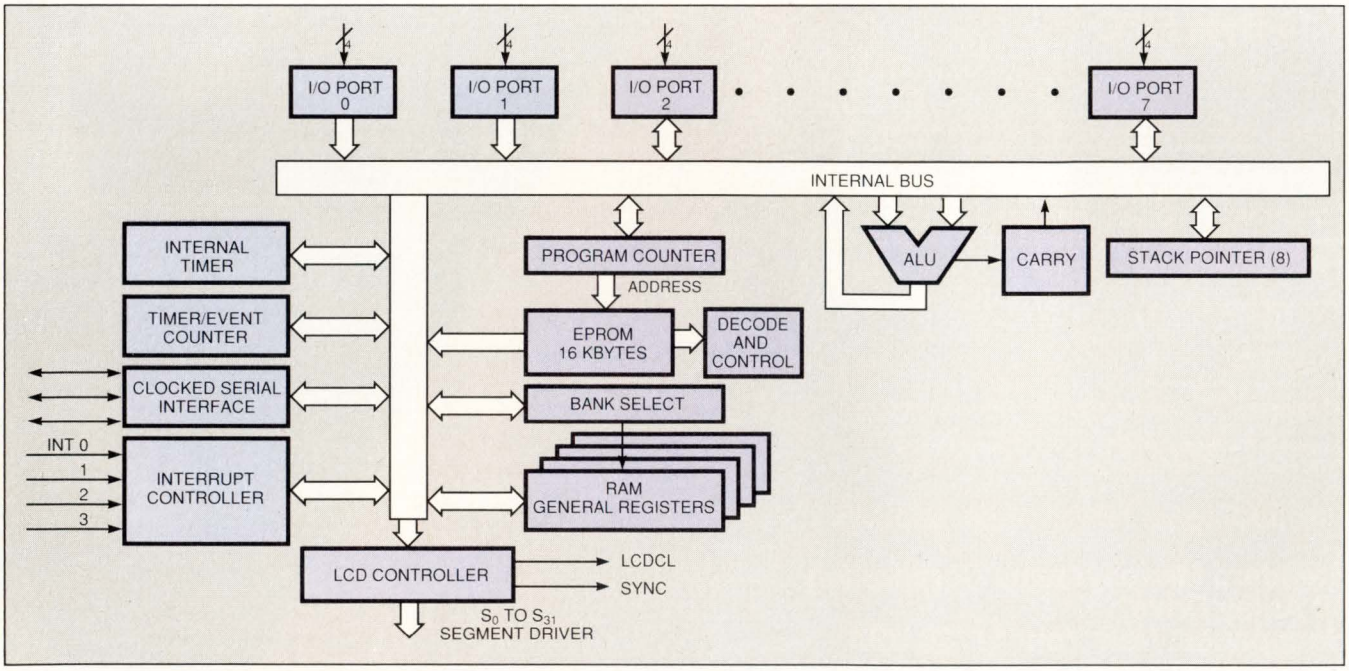
Four-bit μCs are a variation of 8-bit μCs, in that they sport 8-bit instruction sets but use 4-bit arithmetic and data. Thus, they have the same control capabilities of 8-bit μCs but suit applications that don't need 8-bit arithmetic or long data words. The μUPD75P316A, a single-chip μC with no external memory capability, has 16 kbytes of programmable EPROM on chip and 1k nibbles for data storage.

The chip runs with a 4.19-MHz clock and has an execution cycle of 0.95 μsec. The CPU has a set of general-purpose registers, eight 4-bit registers, or four 8-bit registers. These are not minimal processors; they have more than 100 instructions, including bit manipulation and table-reference operators. Six data-addressing modes comprise 1-, 4-, and 8-bit direct; 4-bit register indirect and 8-bit register indirect; and bit-manipulation addressing.

This chip is an extension of an existing 4-bit μC, the μPD75P316. The new chip has doubled data memory and additional EPROM. Both chips can run at low voltages, minimizing operating power dissipation: Voltage ranges are 2.7 to 6V.

RAM is organized into four banks of 256 nibbles each. The first bank is for CPU registers, interrupt vectors, and the program stack. The μC peripherals are memory mapped and are in memory bank 15.

The μPD75P316A chip comes with peripherals that include an LCD controller, a watchdog timer, an 8-bit binary counter with comparator and count register, a serial bus for interfacing with other processors, and three 4-bit I/O ports.



This 4-bit μC, the NEC μPD75P316A, is a full-fledged microcontroller with sophisticated peripherals, including an LCD controller.

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V_{OLV}*	0.8	1.0
V_{IHD}*	1.5	1.7
V_{ILD}*	0.8	0.8

*V_{OLP} = Peak Ground Bounce V_{OLV} = Undershoot
V_{IHD} = Dynamic Input High V_{ILD} = Dynamic Input Low

Performance's FCT-T vs. Leading Competitor's FCT-T

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☐ 10-bit Inverting	FCT828T

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☐ Non-inverting Registered	29FCT53AT
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☐ Non-inverting Buffered	FCT643T
☐ Non-inverting Registered	FCT646T
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☐ Non-inverting w/ Odd/Even Parity	FCT657T
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☐ Diagnostic Scan	29FCT818T
☐ Octal D Flip-Flop w/ Master Reset	FCT273T
☐ 8-Input Universal Shift	FCT299T
☐ Octal D Flip-Flop w/ Output Enable	FCT374T
☐ Octal D Flip-Flop w/ Clock Enable	FCT377T
☐ Quad Dual-port w/ True Outputs	FCT399T
☐ Octal D Flip-Flop w/ Inverted Outputs	FCT534T
☐ Octal D Flip-Flop w/ Flow-Thru Pinout	FCT574T
☐ 10-bit Non-inverting Buffered	FCT821AT
☐ 9-bit Non-inverting Buffered	FCT823AT
☐ 8-bit Non-inverting Buffered	FCT825AT

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☐ Up/Down Binary Counter	FCT193T

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To save on component costs, the I/O-port pins have programmable pullup resistors. Three ports can drive LEDs directly, eliminating the cost of drivers or buffers.

The on-chip LCD controller has four modes, which drive 32, 64, 96, or 128 LCD segments. The controller saves the LCD data in the upper 32 nibbles of RAM bank 1. The controller has built-in timer functions (using the μC timer) to refresh the LCD displays automatically. Signals coordinate multiple μCs acting as LCD controllers.

The μPD75P316A comes in an 80-pin quad flatpack for one-time-programmable versions and in an 80-pin leadless chip carrier with a window for reprogramming. To program the EPROM, 12.5V are needed. The chips meet commercial −40 to +85°C temperature ranges.

Development support for the 4-bit μC includes a structured assembler preprocessor, which incorporates high-level control constructs into assembly code, making it easier to structure a program.

The μPD75P316A costs $27.95 (10,000) for the one-time-programmable part and $65 for the reprogrammable part (small qty).

—**Ray Weiss**

NEC Electronics Inc, 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. FAX (800) 729-9288.

16-bit μC combines 200-nsec instructions with low power and 64-kbyte EPROM or ROM

American engineers can now design in Hitachi's 16-bit, high-end microcontroller (μC) H8/500 series. Because a patent-infringement suit between Motorola and Hitachi has been settled, the H8/500 is now available in the United States. The H8/500 is a 16-bit μC having a 200-nsec basic instruction cycle backed up with as much as 62 kbytes of on-chip EPROM or ROM and 2 kbytes of static RAM.

The previous-generation 300 series μCs have a 64-kbyte address space, 8- or 16-bit registers, a register operation orientation, and fixed 2- or 4-byte instructions. In contrast, the 500 series can address 16 Mbytes using paged addressing. The series also features an orthogonal instruction set, a 32-bit-long word for 32-bit processing, and a peripheral set.

The H8/500 μCs support a single address space—with as much as 16 Mbytes of external memory—using memory pages. The CPU works within a 64-kbyte page, which is defined by page registers. The three major memory modes of the chip include Expanded Minimum, which addresses 64 kbytes of external memory; Expanded Maximum, which addresses 1 Mbyte of external memory (16 pages); and Single Chip, which addresses on-chip memory only. The μCs have an 8- or 16-bit external memory bus. Internal-memory accesses take two internal clock cycles, and external-memory accesses take three cycles.

The series has eight general-purpose 16-bit registers—two of which are dedicated as stack and frame pointers. Running at 10 MHz, the μCs deliver a 200-nsec add, a 1.6-μsec multiply, and a 2.6-μsec divide. The series has a variable instruction length with 63 instructions. The μCs' seven addressing modes include a register indirect with an increment/decrement option, which is effective for optimized table-entry processing. The instruction set also includes bit manipulation and test instructions.

The instruction-processing rate increases by laying out instruction object code in reverse order in memory. Instead of having the op code as the leading byte for an instruction, it is presented last, trailing the effective address information. This reversal speeds execution because the effective address fetches can parallel instruction decoding.

The μCs have as much as 62 kbytes of on-chip program memory, which is the largest amount of on-chip memory for any commercial 16-bit μC. This factory-programmed memory is either mask ROM or one-time-programmable EPROM (zero turnaround time) for fast delivery and prototyping. For program development, windowed reprogrammable EPROM parts will be available in 80-pin, plastic-leaded-chip-carrier versions of standard 84-pin, zero-

Table 1—Hitachi H8/500 Series Microcontrollers

H8 Version	Features	Price (quantity)
Common to all	Seven or more ports, duplex serial channel, 10-bit A/D converter (13.8 μsec) watchdog timer, 9 external interrupts, DMA controller, wait-state controller, 8-bit multifunction timer, 2 or more 16-bit timers, 3V power versions	NA
510	ROMless controller 16-bit external bus, on-chip DRAM refresh 112-pin quad flatpack	$11.85 (5000)
520	Low-end controller 64-pin package 16-kbyte ROM/EPROM, 512 bytes of RAM	$11.45 ROM (10,000) $22.22 EPROM (1000)
532/534	Midrange controller, 3 PWM timers, extra 16-bit timer, 32-kbyte ROM/EPROM, 1- to 2-kbyte RAM 84-pin plastic leaded chip carrier or 80-pin quad flatpack	$14.20 ROM (10,000) $25.80 EPROM
536	High-end controller, 3 PWM timers, extra 16-bit timer, 62-kbyte EPROM/ROM	$19.40 ROM (10,000) $34.10 EPROM (1000)

Note: NA=Not applicable.

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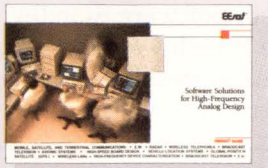

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turnaround-time parts. These devices can be programmed in a standard 27256-type EPROM programmer.

These 16-bit μCs also have a large set of on-chip peripherals, which include two or three 16-bit timers, an 8-bit free-running timer, a DMA controller, seven to nine I/O ports, an interrupt controller, a 10-bit A/D converter, a serial communications interface (duplex), and a watchdog timer.

The μCs have built-in power management. You can choose three programmable power-down states: Sleep, where the clock and support peripherals run, but the CPU is halted; Software Standby; or Hardware Standby—in both standby modes everything is halted. In all power-down modes, RAM and register values are held. Recovery is triggered by combinations of interrupts and special pin inputs. Typical current dissipation is 30 mA running, and 20 mA and 0.01 μA, respectively, for sleep and standby modes.

Software tools are available for the μC series: two C compilers from Avocet Systems Inc (Rockport, ME) and Software Environments Ltd (Dallas, TX), as well as a Forth system, and a Fuzzy-Logic compiler from Togai Infralogic (Irvine, CA). In-circuit emulators are also available from a number of vendors.

—**Ray Weiss**

Hitachi America Ltd, Semiconductor and IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207.

Programmable I/O processor services device interrupts

Device and I/O channel management processing can quickly load a system down, bringing a host CPU to its knees. To combat this, in the 1960s, IBM developed programmable I/O channel processors to offload device channel processing from the 360 and later-version host CPUs. Now, desktop, server, and dedicated-systems designers can apply the same solution to their designs with an I/O processor chip, the Signetics SC26C460.

When a device needs service, it triggers a request line; the SC26C460 processor will then queue these requests, servicing them by assigned priority. The chip can interrupt the host CPU to pass data or request service.

The chip is a dedicated I/O processor that can handle as many as 32 device channels, directing and controlling their I/O data streams. The chip is programmable, with 15 instructions; the processor offloads the host CPU by fielding device interrupts and managing the device data transfers between the peripherals and main memory. The processor can address as many as 16 Mbytes of memory with an 8- or 16-bit bus.

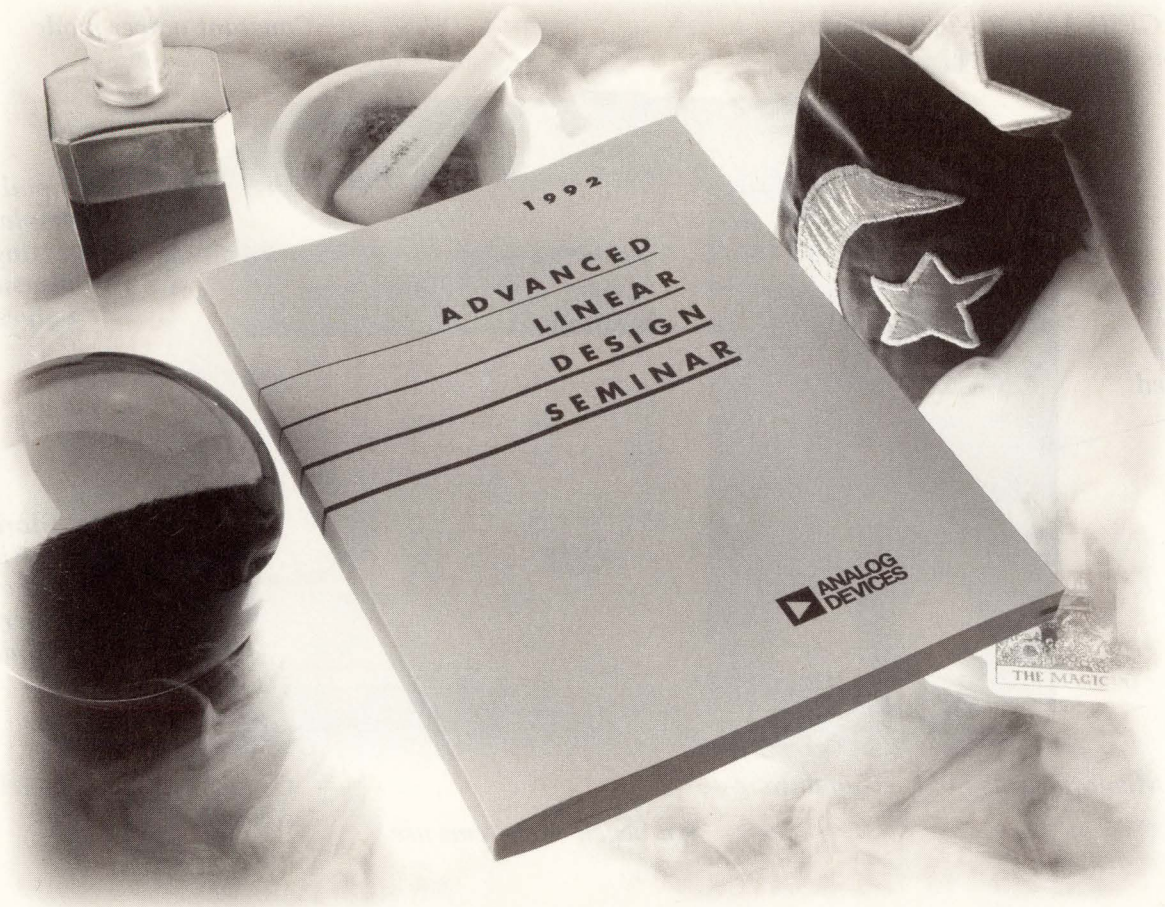
The processor does not buffer device data. Instead, it directs the data flow, managing device access to a common memory. The processor can be used directly with the host CPU's main memory or with a dual-port memory scheme, which isolates device and host access without creating contention on the host memory bus.

The processor stores separate memory addresses and buffer lengths for each device channel; each device channel has a separate channel program-entry point. The processor can interrogate and check device status, read and write a peripheral, and branch to a different processing stream. It can also translate device code via decision tables.

The SC26C460 I/O processor comes in a 68-pin plastic leaded chip carrier and costs $18.50 (1000).—**Ray Weiss**

Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000. FAX (408) 991-2311.

If you've always thought linear design involved a little black magic, here's where you can learn a few of the tricks.



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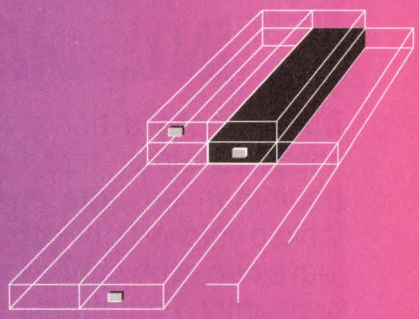

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			Charging Current (mA)	Time (Hrs.)	L (mm)	W (mm)	T (mm)	
KF-A600	1.2	600	60	14-16	67.0	17.0	6.1	23
KF-A900	1.2	900	90	14-16	67.0	17.0	8.1	30
KF-A1200	1.2	1200	120	14-16	67.0	17.0	10.3	38
KF-B600	1.2	600	60	14-16	48.0	17.0	8.1	21
KF-B400	1.2	400	40	14-16	48.0	17.0	6.1	16

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Trio of software tools tailors MS-Windows to test applications

If you use an MS-DOS PC to develop and run test applications, Hewlett-Packard figures that sooner or later—probably sooner—you're going to be doing your development and running your programs under MS-Windows V3.0 or higher. Therefore, the firm is announcing a trio of Windows-based test-development packages.

Of the three latest offerings, Instrument Basic for Windows provides the best place for neophyte test programmers to get started. The language is designed for engineers and scientists who want to write their own test software to run under Windows. (Despite Basic's reputation as a beginner's language—Basic stands for *Beginners'* all-purpose symbolic instruction code—HP claims that test engineers still program as many test applications in Basic as in all other languages combined.)

This Basic is interpreted, preserving the language's interactive flavor, and is much more test oriented than other Windows languages. Unlike earlier versions of HP Instrument Basic, the Windows version runs on 80x86-based PCs *without* a 680x0-based coprocessor board.

ITG II is a tool for programmers looking for assistance in creating Windows-based test programs. It doesn't allow you to program solely by creating, interconnecting, and manipulating icons. (Last year, for people totally averse to text-based programming, the vendor introduced a workstation-based package called VEE that lets you control instruments and data solely by working with icons.)

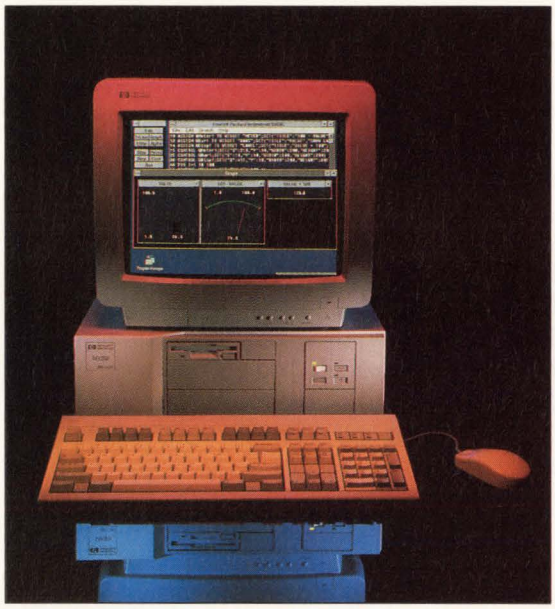
ITG II targets test engineers with programming experience who will find the graphics-based features handy for generating code segments in several languages. But text-based code will still be needed for linking the segments, which themselves are text based, into working applications. ITG II is the successor to the vendor's earlier ITG/DOS, a package that does not support MS-Windows.

One of ITG II's new features is a driver-writing tool. Although you cannot use the tool for writing complex instrument drivers, you can use it to rapidly write drivers that control an instrument's most-often-used functions. You write the drivers by following a structured question-and-answer process that is embedded in the tool.

The vendor characterizes the third package, HP-IB for Windows and DOS, as a safety net for DOS/Windows programmers who are working with Windows-compatible languages and applications and want to control IEEE-488 instruments. In other words, if you are using a language that doesn't handle instrument control, you can enhance this language with the instrument-control functions you need by using HP-IB for Windows and DOS. If, instead of a language, you are using a Windows application, such as Excel, and you want to do instrument control and data acquisition from your spreadsheet, this Windows and DOS package will allow you to do the job.

HP E2200A, Instrument Basic for Windows, costs $395; HP E2020B, ITG II, including a library of 220 instrument drivers, costs $1495. HP 82335B, HP-IB for Windows and DOS, including an ISA bus IEEE-488 interface card, costs $525.—**Dan Strassberg**

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900 for information; (800) 452-4844 for orders.



Graphics displays that appear in windows while you develop and debug your test program are just one of the features of Instrument Basic for Windows. The language is one of three packages the vendor is targeting at test engineers who use MS-DOS-based PCs to develop and run test applications.

EPLD combines 80-MHz counter rate with 256 logic cells and 164 I/Os

Logic designers carve out their creations under tight constraints, limited by logic delays, interconnection costs, and available I/O pins. They can, however, use the Altera MAX 7000 series EPLDs (erasable programmable logic devices) to gain some sorely needed design elbow room. The top-of-the-line EPM7032 brings together an 83.3-MHz (f_{CNT}) counter clock rate, with 256 logic macrocells, special shared logic-expander terms, a fixed cell-to-cell signal delay of 3 nsec, and 164 I/O pins. Logic delay for a signal, coming on chip through a gate to a flip-flop, is 12 nsec (t_{PD}).

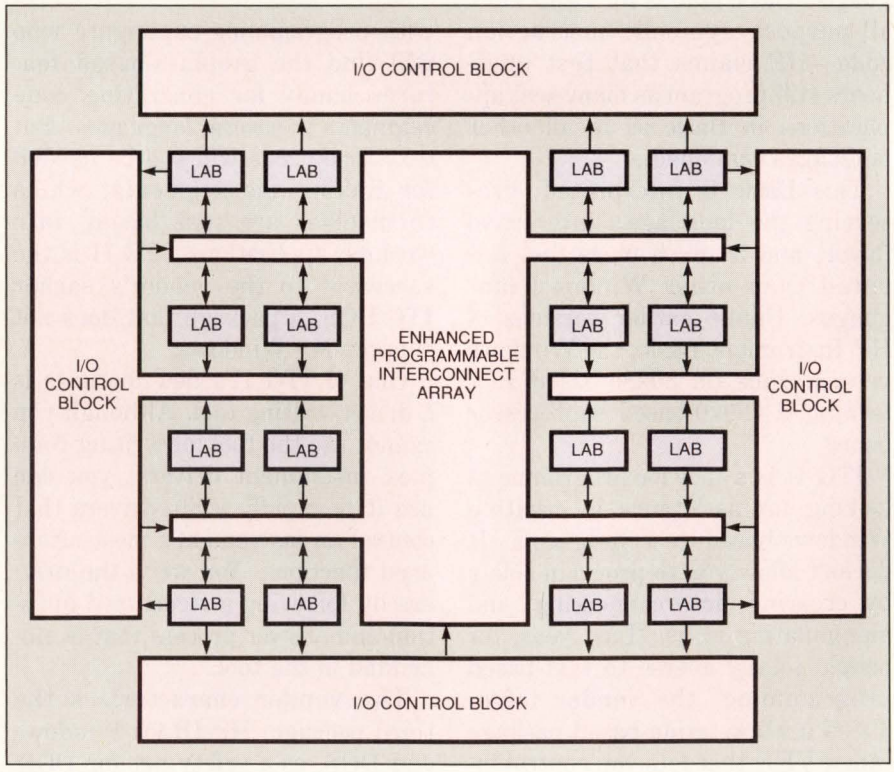
Engineers can build designs from the logic macrocells using expander terms to widen logic product terms. The company furnishes a comprehensive macro design library of SSI and MSI parts that are mapped onto the MAX macrocells from the earlier MAX 5000 line. The MAX 7000 series supports faster clocks, a minimized intercell delay to 3 nsec, and higher I/O pin counts. In addition, for the first time the MAX programmable logic is available in an electrically erasable PLD (EEPLD).

The first two members of the MAX 7000 family are the EPM7256GC192, a 10,000-gate EPLD with 192 I/Os; and the EPM7032LC44, a 1250-gate EEPLD with 36 I/Os (4 dedicated inputs). Most applications can use approximately 50% of these gates. Future chips will push to 300 pins and 20,000 usable gates.

The MAX family sits in the middle of the large-scale programmable logic world. On one hand, RAM-based FPGAs (field-programmable gate arrays), like Xilinx's, have an array of logic cells that are programmed by setting underlying RAM control bits. This RAM controls each cell as well as on-chip interconnects. On the other hand, antifuse FPGAs modeled after gate arrays have an array of cells with one-time-programmable interconnects. Vendors such as Actel, Quicklogic, and Crosspoint use low-impedance antifuses to program macrocell interconnects. MAX EPLDs are reprogrammable, but they must be taken out of the system to do so.

Altera's approach to complex FPGAs is to build fixed hierarchies of macrocells. For example, the EMP7032 has 256 macro or logic cells. These cells are ordered into logic array blocks. An EPM7256 has 16 logic blocks, each with 16 macrocells. Each logic block is like a mini PAL—the macrocells share a logic array or bus of signals. These signals are routed to an individual cell input term by programming its EPROM connection bit, just like a PAL. Each macrocell logic input acts as an implicit AND gate with multiple product terms. Thus, you can build fairly complex logic using a simple macrocell.

However, the MAX EPLDs differ from PALs in that Altera engineers added a programmable interconnect array for linking signals between logic blocks. This array is



With this EPLD architecture, intercell signal delays are held to 3 nsec. Using the MAX 7000 series, you can build complex logic without worrying about unconstrained routing delays.

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laid out so routing delays between any two logic-block signals remain constant at 3 nsec. This tactic eliminates the routing problems that many designers experience with other FPGAs, where timing depends on efficient routing. MAX timing delays are fixed, with perhaps higher delays than an efficiently routed FPGA layout.

To increase potential logic complexity, Altera engineers added expander product terms to the logic blocks. These are unallocated AND gates that can be programmed and shared by the logic-block macrocells. With expanders, designers can fit as many as 76 product terms into a single macrocell using one additional logic level of delay.

The MAX7000 macrocell is a simple logic block. It consists of a product term-select matrix (5 PAL-like AND gates) with simple logic ORed and the result fed to a flip-flop or directly out. Without expanders, a macrocell takes as many as 32 product terms. The logic handles D, T, JK, and SR flip-flops. Global clocks, clears, and output enables are also provided.

The company's development software, MAX+PLUS II, is for the MAX programmable logic and runs on a PC under Windows 3.0. This tool set includes a graphic schematic editor, a text editor, a waveform editor, and a logic simulator for testing designs. It includes Altera's Hardware Description Language for textually defining designs such as state machines. The system also provides a tool for partitioning large designs into multiple chips.

The 192-pin pin-grid-array EPM-7256GC192 costs $395 (single qty). The 44-lead plastic-leaded-chip-carrier EPM7032LC44 costs $14.75 (100).—**Ray Weiss**

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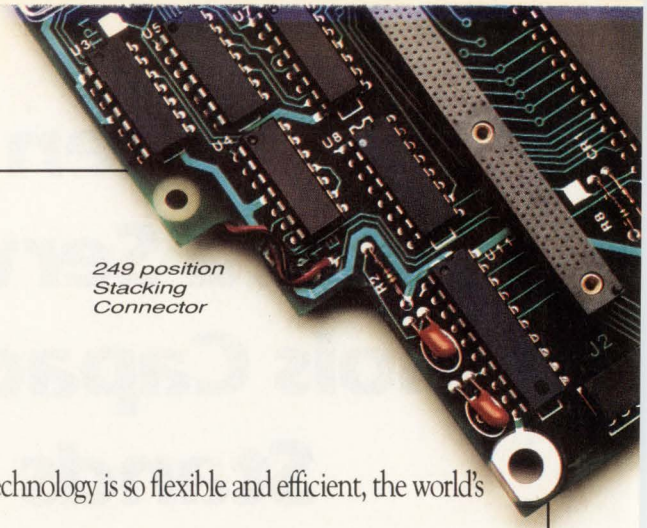
1,156 position
LGA Socket



249 position
Stacking
Connector

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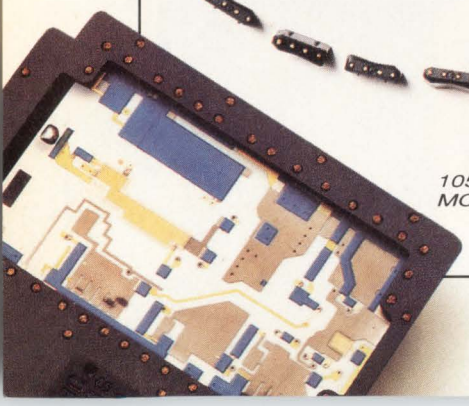

105 position
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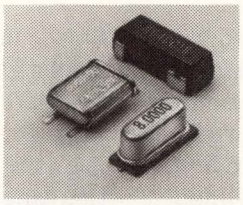

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µP/peripheral-function building blocks speed system-design tasks

Having a library of microprocessors and peripheral functions allows you to design complex ASICs quickly, much as you'd build a breadboard. The Coreware library contains three groups of building blocks: 16- and 32-bit microprocessors, floating-point processors, and peripheral functions.

Several ASIC-vendor libraries contain 4-, 8-, and 16-bit microprocessor cores. One ASIC vendor, VLSI Technology, offers a core of its Acorn 32-bit RISC (reduced-instruction-set-computer) processor. LSI Logic's Coreware library offers familiar 32-bit RISC cores that allow you to customize designs by tailoring the cache or peripherals to meet your application's special needs. These building blocks are high-speed, standard components with existing software bases and large installations of native hosts.

At introduction, the library contains embedded SPARC and Mips microprocessor cores and a 1750A 16-bit processor core. Among the range of pipelined and nonpipelined IEEE-754-compliant floating-point units are 32- and 64-bit ALUs and multipliers as well as a pipelined 32-bit divider. Initially, peripheral functions are limited to a SCSI-1 controller, a generic multiprocessor bus interface, an SBus DMA controller, and a Mips read-write buffer. JPEG (Joint Photographic Experts Group) Image Compression, a Reed-Solomon Codec, and the Mips integrated FPU/CPU functions are currently in the works.

Each function block, like ASIC primitives, consists of a schematic representation and a gate-level simulation model in LSI Logic's proprietary format. In addition, the function blocks also offer behavioral-level simulation models. These C-code models are kept in an intermediate format that the vendor can translate to VHDL (VHSIC Hardware Description Language), Verilog, and its own behavioral-simulation language.

In addition, the function blocks feature existing test vectors. These vectors allow the vendor to perform comprehensive in-circuit manufacturing tests on each of the blocks. The test method that each pattern uses varies depending on the particular functional blocks; the embedded SPARC module uses an internal scan chain whereas the embedded Mips module uses parallel-input vectors that require you to provide pin access to the block's borders. These tests reduce your design responsibility to just providing observation and control of nodes within the random logic and non-Coreware library functional blocks.

The roughly 20,000-gate embedded SPARC core is a bare-bones processor. The core is based on the early SPARC instruction set; it doesn't perform direct multiplication or division. In addition, the core offers no floating-point coprocessor interface and requires two memory cycles for load instructions. The core, which runs at 20 MHz, does provide on-chip cache support or offers an interface to off-chip cache.

The Mips family is represented by two core processors, which can run at 25, 33, and 40 MHz. Both the roughly 35,000-gate embedded core and the 25,000-gate CPU are fully static designs that implement most of the Mips I instruction set. Using 1-µm fabrication, you can surround the core with approximately 65,000 gates of additional logic. The embedded core provides a 4- or 8-kbyte instruction cache, an optional data cache, a DRAM (dynamic RAM) controller, a bus-interface unit, and three counter/timers.

A direct data-bus interface bypasses the bus-interface unit and provides single-cycle data transfers between the embedded CPU and dedicated on-chip static RAM or ROM. The cores offer provisions for DMA, although they sacrifice coprocessor support, a memory-management unit, and translation look-aside buffers (TLBs). Without the TLB registers, the CPUs don't offer instructions to manipulate them; if your code contains them, these instructions will cause exceptions.

Pricing depends on several factors, including the core, volume, and design requirements. The access fee, which includes function-block royalties, starts at $30,000. This fee supplements the nonrecurring engineering cost, which starts at $30,000. If your needs require it, the vendor will actively participate in the design.—**Michael C Markowitz**

LSI Logic Corp, M/S D102, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 954-4875.

Low-cost package links 68HC16 to PC

Debugging critical code for an embedded µC is a bit easier with Motorola's ICD16 debugging tool for the 16-bit 68HC16 microcontroller (µC). This tool links a PC host computer to a 68HC16 target system. The ICD16 module plugs into a PC parallel port. Using the module, users can directly control µC target code's execution.

The ICD16 takes advantage of the background mode, which Motorola added for on-target debug-

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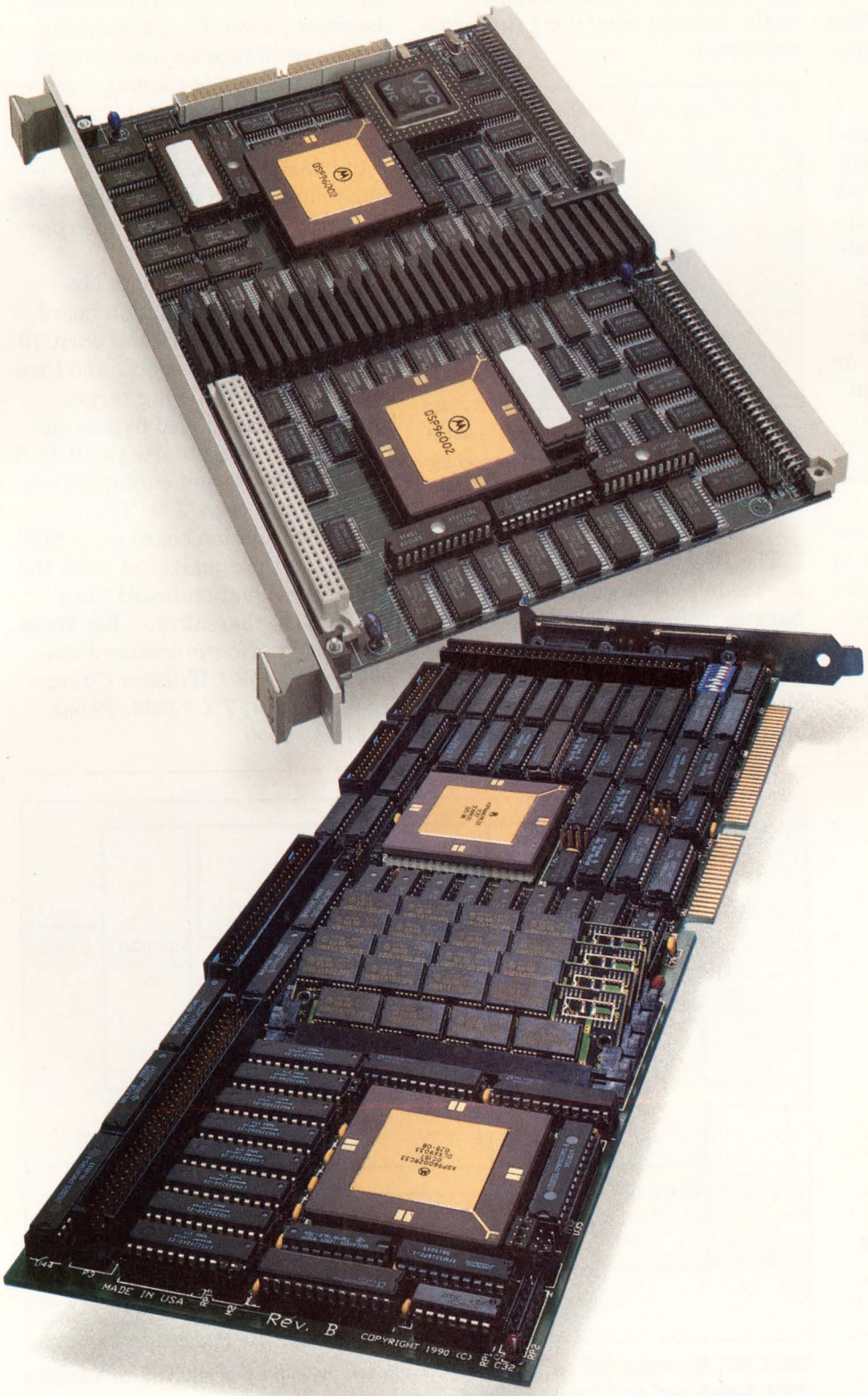

ISA, EISA, or VMEbus, Ariel processor boards unleash all the power of Motorola's DSP96002. Both the MM-96 for ISA/EISA and V-96 for VMEbus combine lightning-quick speed with large memory arrays, versatile I/O with 120 Mbyte/sec. total bandwidth, and the ability to deliver almost unlimited signal-crunching power via Ariel's two exclusive high-speed expansion buses. And Ariel's steadfast commitment to service and support ensures that once you've become an Ariel customer, you'll never work alone.

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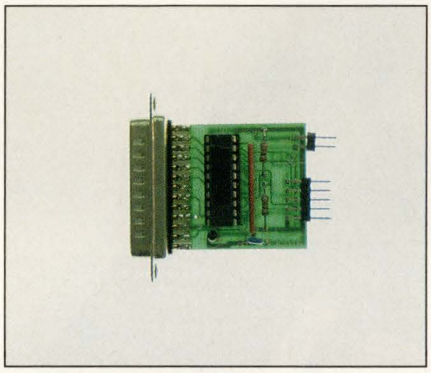
CIRCLE NO. 95

ging, of the 68HC16. In background mode, normal processor execution is halted and an external host can control the processor via eight control pins. In background mode, a remote user can interrogate or set register or memory values as well as set breakpoints. When execution hits a breakpoint, processor execution halts and control passes to background mode.

Unlike an ICE (in-circuit emulator), the debug tool requires some board space for wiring and a 10-pin header. In addition, the ICD16 operation is intrusive: Debugging affects code execution. The ICD16 uses processor resources, mainly execution time, to execute breakpoints, retrieve and set memory or register values, and communicate with the host PC. However, once you set a breakpoint, you can monitor execution in real time until the code hits it and breaks.

In contrast, ICEs are mainly nonintrusive. They collect trace data in separate buffers, not affecting performance until the trace buffer is full. A breakpoint will, of course, stop execution. The ICD16 approach is less intrusive than that of using a monitor—a small debug kernel, which takes up memory and processor resources. In addition, the ICD16 does not need to use the μC's serial port to link to a host; it uses special pins. You could actually run a monitor—linked via a serial port—and the ICD16 simultaneously, because they don't share link resources.



You can debug 68HC16 target code without an ICE. To monitor and control execution, the ICD16 links to the target μC via background mode.

The ICD16 package consists of the module, a target cable, and debugging software. The software is a more advanced version of the integrated assembler furnished with Motorola's 68HC16 evaluation board. This version provides a windowed development environment, which integrates a macroassembler, an editor, and a source-code debugger with a host-to-target communications link.

The source-code debugger enables you to debug target code at the source level (C or assembly). It adds performance monitoring (address reference counts), macroscripts, a dumb terminal window, file verification, and interrogation of the 68HC16 multiply-and-accumulate unit. P&E Microsystems Inc (Woburn, MA) developed the core software for Motorola.

The ICD16 supplements Motorola's 68HC16 evaluation board; initially, you can work the 68HC16 with the evaluation board, and then use the ICD16 to debug target boards. You could also bypass the evaluation board and use the ICD16 with a simple target configuration.

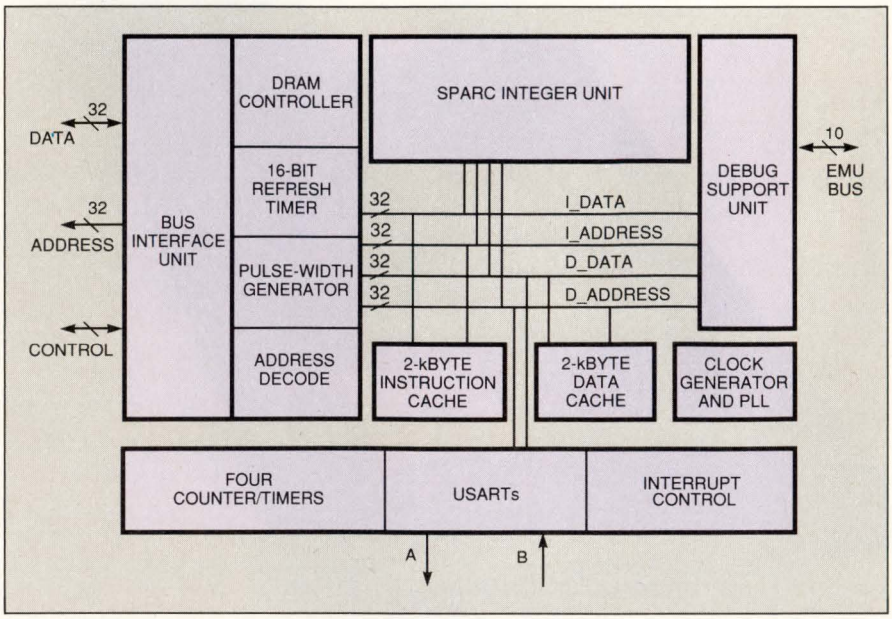
The ICD16 costs $99. The 68HC16 evaluation board costs $168 during the first quarter of 1992; the standard evaluation-board price will be $320 thereafter.—**Ray Weiss**

Motorola Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2000.

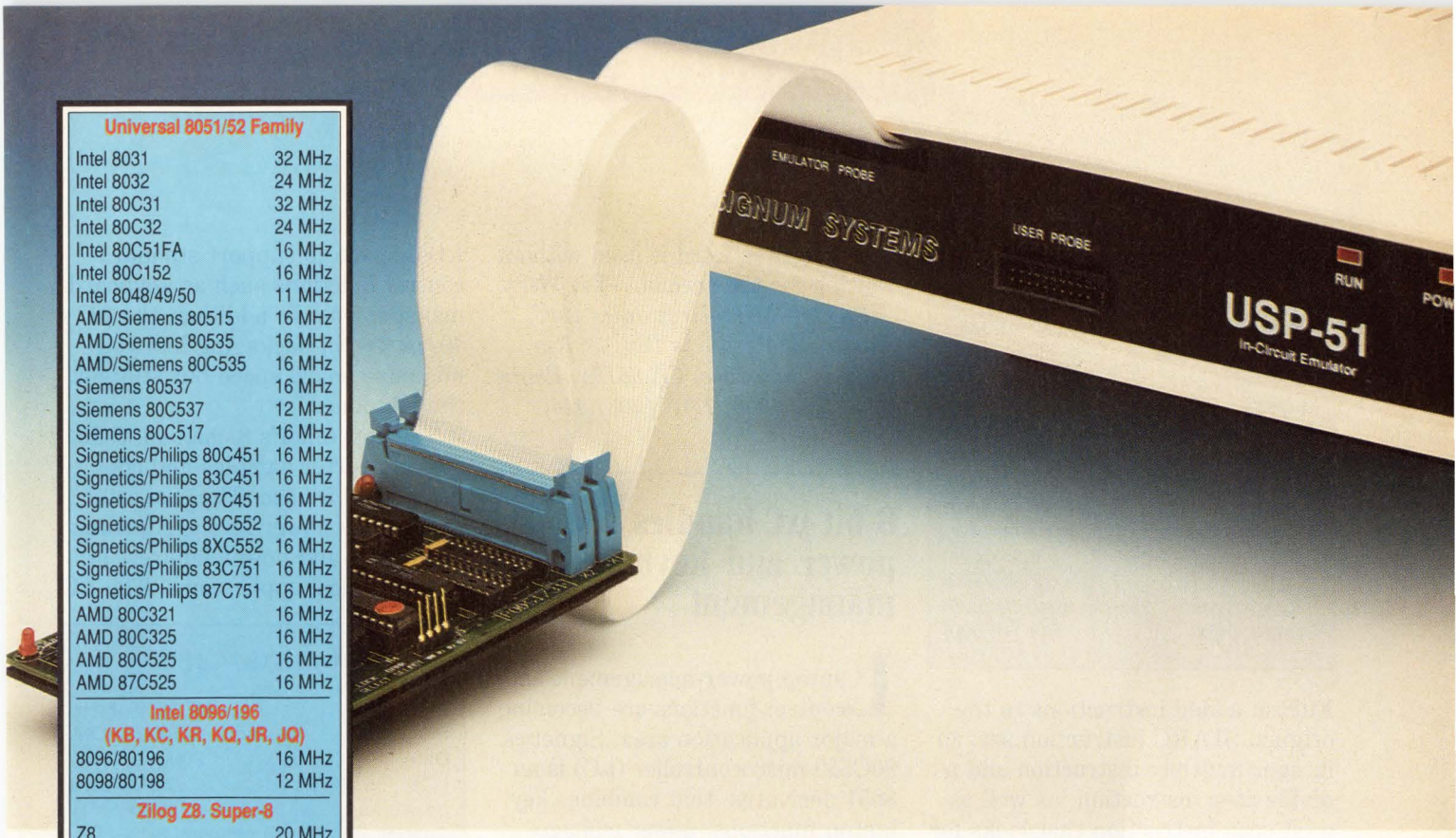
32-bit μC integrates SPARC with embedded peripherals

Fujitsu's 32-bit SPARClite MB86931 integrates the SPARC RISC (reduced-instruction-set-computer) architecture with a set of μC peripherals tailored for embedded processing. The SPARClite "event processor" handles real-time events. The chip integrates the SPARC integer processor with 2 kbytes each of on-chip instruction and data cache, an interrupt controller, counter/timers for monitoring external events, and a dynamic-RAM controller.

To increase execution speed,



SPARC RISC fits embedded systems. The SPARClite μC combines a SPARC CPU with on-chip cache, timers, and an interrupt controller.



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Intel 80C51FA	16 MHz
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AMD/Siemens 80535	16 MHz
AMD/Siemens 80C535	16 MHz
Siemens 80537	16 MHz
Siemens 80C537	12 MHz
Siemens 80C517	16 MHz
Signetics/Philips 80C451	16 MHz
Signetics/Philips 83C451	16 MHz
Signetics/Philips 87C451	16 MHz
Signetics/Philips 80C552	16 MHz
Signetics/Philips 8XC552	16 MHz
Signetics/Philips 83C751	16 MHz
Signetics/Philips 87C751	16 MHz
AMD 80C321	16 MHz
AMD 80C325	16 MHz
AMD 80C525	16 MHz
AMD 87C525	16 MHz
Intel 8096/196 (KB, KC, KR, KQ, JR, JQ)	
8096/80196	16 MHz
8098/80198	12 MHz
Zilog Z8. Super-8	
Z8	20 MHz
86C94	30 MHz
Super-8	20 MHz
Texas Instruments DSP's	
320C10/15	33 MHz
320C16	35 MHz
320C17	20 MHz

Let's talk real 8051 8096/196 in-circuit emulation. . . . and DSP's too!

Signum Systems' in-circuit emulators offer more standard features than you'd expect, and some you wouldn't.

Features You'd Expect

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- Flash download 115 k-baud
- Debug in C and PL/M
- Non-intrusive to target or PC
- Full speed emulation

Signum Extras

- C-51 and C-96 HLL debugger with locals support
- Full bank switching support
- Up to 256K emulation program RAM
- Graphic trigger window
- 32K x 80 real-time trace
- Access on-the-fly to:
  - All emulation RAM contents
  - 3 complex trace triggers
  - 8 level sequencer
  - Trace and execution displays
  - 256K address breakpoints
  - 2 16-bit event counters
- Performance analysis
- Unlimited user support

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Switzerland	**(41) (91) 568-721**
Poland & Eastern Europe	**(48) (71) 484-221**

* System capable of 32 MHz; actual emulation speeds limited by currrent device speeds.

SPARClite MB86931

Clock	20, 49 MHz
Instruction cache	2 kbytes
Data cache	2 kbytes
Memory	Dynamic-RAM support: Wait-state generator, Refresh controller
Timers	4 counter timers, Refresh timer
Miscellaneous	Interrupt controller, 15 interrupts, 2 USARTs
Package type	256-pin quad flatpack
Sample price	$49 (10,000)

Fujitsu added instructions to the original SPARC instruction set: an integer multiply instruction and a divide step instruction, as well as a bit-scan instruction that looks for the first nonsign bit. This bit-scan instruction helps in processing bit maps.

In addition, the chip is a fully static design. SPARClite cleans up a number of problems of earlier SPARC implementations. For example, loads and store are typically one instruction cycle, compared with two and three cycles for earlier SPARC CPUs. Some of these speed-ups are a result of a Harvard architecture with divided dual instruction and data caches, unlike Sun SPARC's single unified cache.

Also, this family has on-chip hooks for embedded system test and built-in, in-circuit-emulator/monitor support. The processor has six breakpoint registers. To monitor code execution, users can set two instruction, two data-value, and two data-address breakpoints.

The chip has small on-chip caches. These 2-kbyte caches are generally effective if inner loops fit into the caches. Cache entries can be locked in, enabling critical code to be kept in the 2-way set associative caches for continuous processing. The CPU doesn't wait for the 2-word cache line to be filled from external memory: The first word is used without waiting for the second.—**Ray Weiss**

Fujitsu Microelectronics Inc, Advanced Products Div, 77 Rio Robles, San Jose, CA 95134. Phone (408) 922-9000. FAX (408) 943-9293.

8-bit μC handles power and keyboard management

Laptop power-management and control functions are becoming a major application area. Signetics 80C550 microcontroller (μC) is an 8051 derivative that combines key laptop functions: power management and keyboard control. The 8-bit μC crams the 8051 architecture (with 30 I/O pins and A/D converter) into a 40-pin DIP or 44-lead PLCC (plastic leaded chip carrier).

This chip fills a gap in the 8051 world: It supplies enough peripherals to handle power management and provides the I/Os and program-ROM space to support standard control functions such as keyboard management. In addition, the μC's 40- or 44-pin packaging lets you minimize board space but still get the job done.

The controller's 8-channel, 8-bit A/D converter samples and converts in 40.5 μsec. The converter can sample power levels, signaling brownout, and power failures, in power-critical applications. The μC

80/83/87C550

Clock	3.5 to 16 MHz
Program	4 kbytes ROM/EPROM
Data	128-byte RAM
I/Os	30/32 pins
Interrupts	2 external
Special	8 channel, 8-bit ADC (6 channel on DIP), 2 16-bit counters, watchdog timer, UART
Package types	40-pin DIP, 44-lead plastic leaded chip carrier or quad flatpack
Price	$4.60 DIP ROM (10,000) $17.83 one-time-programmable DIP (1000)

Power-management design kit

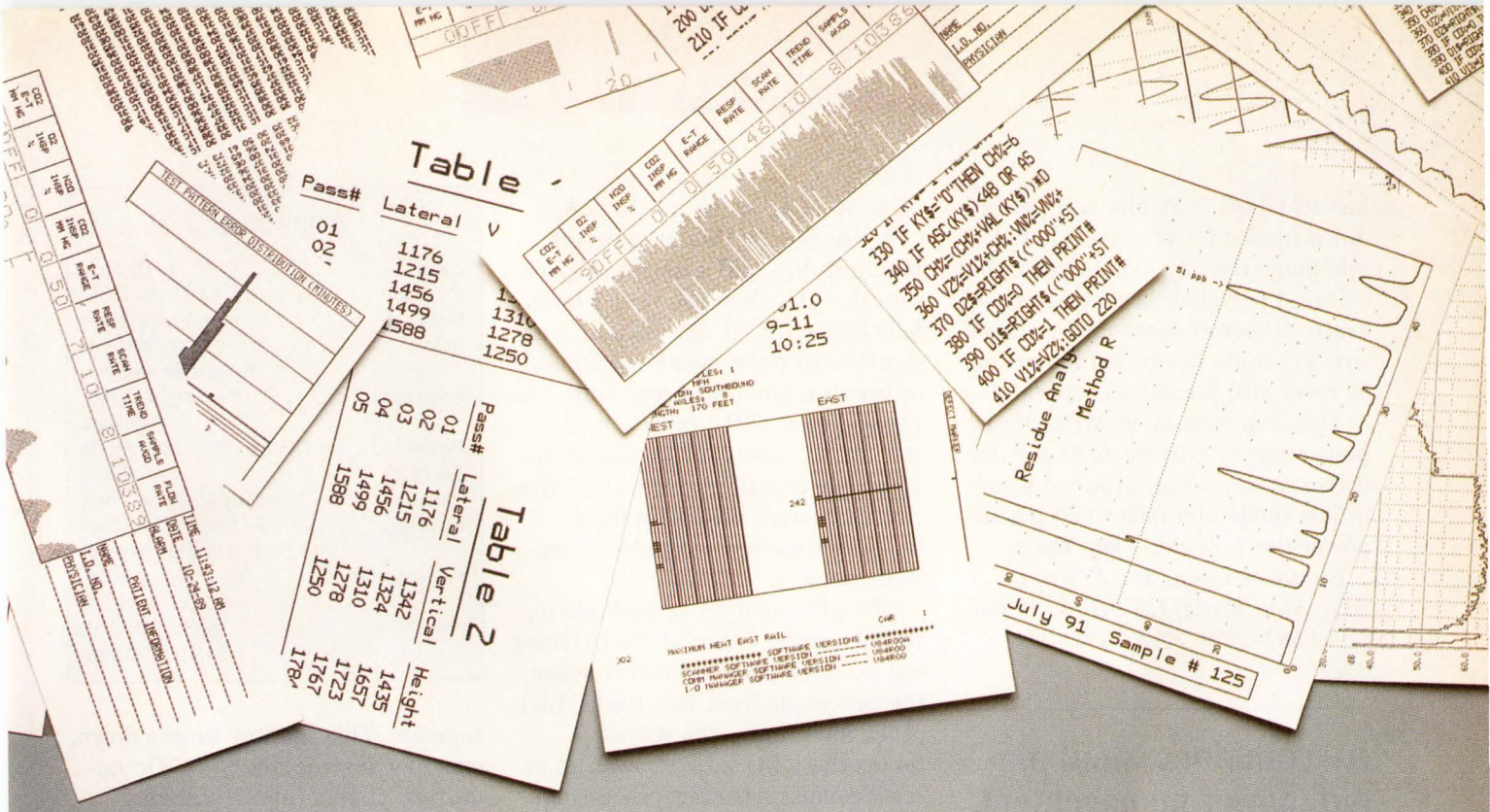
Today, laptops are hot and laptops require power management. The Signetic's design kit lets engineers design in 80C752/550 μCs for laptop power management.

The kit consists of an application note, which defines the design; a schematic of the complete design; and the application source code.

Using this kit, you can modify the design for your own needs or use it to understand a power-management application. This baseline design saves time by providing an easy-to-understand base to start from. The kit defines a Signetics optimizer board that monitors power. It controls the system frequency generator for clocks and the system-memory, dynamic-RAM-refresh cycles. Keyboard and peripheral activity drives the state machine that controls power management.

An on-chip A/D converter monitors the system battery level and V_{CC}. The optimizer drives the clock-frequency generator and controls the system-refresh generator. Six operational modes include full power; doze, when the clock rate is halved; shutdown, when power to specific peripherals is turned off; shutdown-doze; sleep, when power is removed from display backlight and LCD regulator; suspend, when the μC takes over memory refresh task and removes power from the rest of the system; and off, when all power is turned off.

The design kit is free of charge.



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Here's how B-G Instruments' OEM printer family can simplify production of high-quality data printout.

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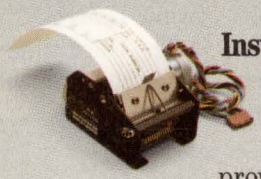
Multiple choices. Hardware options include print mechanisms like those listed here — plus a powerful array of control boards and accessories. So custom systems can be configured quickly and easily to meet your precise needs.

DataPlot Thermal Print Mechanisms

Model Number	Paper Width	Columns Across[2]	Dots / Inch	Dots / Line	OEM Price[1]
PM1224	2.6 inches	18 to 37	100	224	$311
PM1320	2.6 inches	23 to 53	150	320	$296
PM1416	4.5 inches	29 to 69	100	416	$443

1 This is the 300-piece OEM price. It is subject to change without notice.

2 The maximum number of columns depends on the font and size selected. The higher number is for 5 x 7 characters, approximately 16 characters/in.



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B-G INSTRUMENTS

has standard 8051 idle and power-down modes for power saving. In idle mode the CPU shuts down, but selected peripherals continue to operate. In power-down mode, the entire μC shuts down. An interrupt or reset will resume μC operations.

The chip runs at 16 MHz. Its power-supply current is 35 mA for active mode, which drops to 6 mA in idle mode and falls to 50 μA in power-down mode.—**Ray Weiss**

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000. FAX (408) 991-2311.

μC combines small pin-out, power management, application protection

Designing controllers for low-cost appliances and industrial controllers is a tough compromise among low cost, multiple functions, and safety. National Semiconductor's 8-bit COP820CJ microcontroller (μC) can take a little of the pain out of appliance design. It combines a 1-μsec CPU core with power management, brownout detection, direct display drive, A/D conversion, pulse generation for motor or sound generation, and multiple timers.

The μC is built around the National COP800 CPU core. This core is an accumulator-based implementation (six registers), with 1-kbyte program ROM and 64 bytes of data RAM. This μC is designed for low-end appliance applications such as toasters, coffee makers, vacuum cleaners, and food processors. These applications require fail-proof safety, moderate program capability, multiple hardware interfaces, and power management.

Safety features are built in to the μC. Brownout, power failure, infinite software loops, and other error conditions will automatically force a CPU reset. To save power, a hold mode drops power consumption in the static device from 8 mA at a 10-MHz clock to 10 μA.

A brownout-protection circuit monitors V_{CC} and automatically resets the μC when the power level falls below 3V. It also detects transients with pulse widths of 70 nsec or greater. On a transient fault, the μC will stop CPU execution, returning to normal-mode operation when the transient ends. Detection circuitry saves designers from building external, discrete protection circuitry.

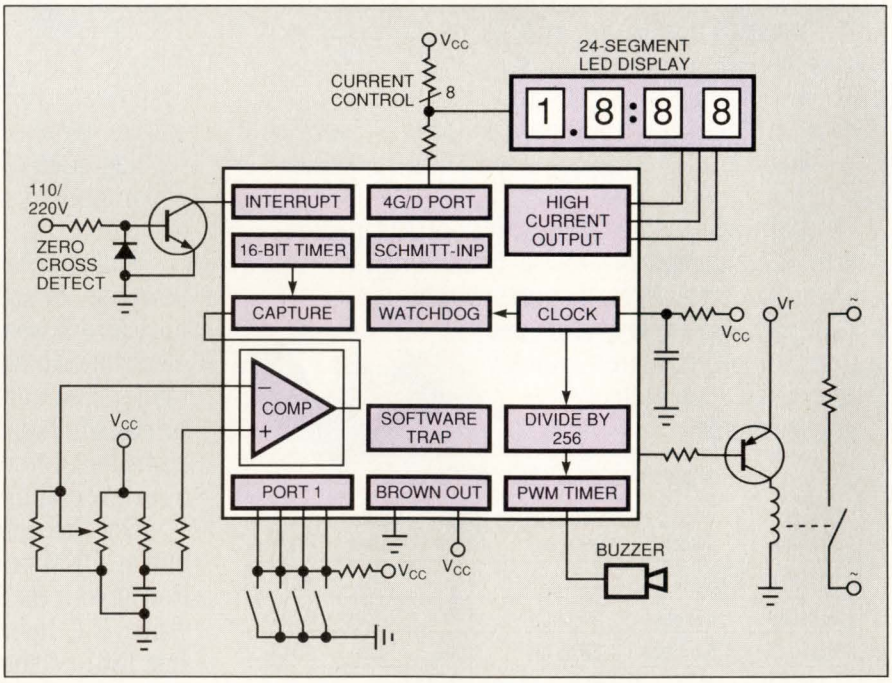
The μC responds to multiple external events. Eight of the I/O lines can be edge programmed to wake the processor from halt mode. Like other interrupts, the wake-up forces the CPU into a power-up or reset condition to start processing.

This controller has three timers. The 8-bit programmable watchdog timer has a divide-by-256 prescaler and can detect runaway software. The 8-bit PWM timer enables code to generate high-frequency pulses, including variable duty-cycle pulses (PWM) for motors or other electronic control.

The third timer is a 16-bit general timer/counter with a load/compare register. This counter counts down, once per instruction cycle. On underflow, it generates a pulse for output or for interrupting the CPU. At the same time, it loads from the load/capture register. The counter can be programmed as an event counter, counting down for external signal pulse (500 kHz max). It can also serve as an input timer, counting down until an external signal triggers, whereupon the current count is saved to the load/compare register.

COP820CJ

Clock	.1, 4, 10 MHz
Program	.1-kbyte ROM
Data	.64-byte RAM
I/Os	.12 to 24 lines 16 Schmitt triggers
Interrupts	3 external, timer, Software
Power	2.5 to 6V, HALT mode
Serial	Serial bus
Timers	Watchdog, 16-bit timer
Special	Analog comparator Brownout detector
Package types	20- or 28-pin DIP, 16-pin SOIC
Price	$1.25 (10,000) $1.15 (100,000)



Smart appliances can be controlled with a single low-end, 8-bit μC, the COP820CJ. In a 20-pin DIP, the chip supports small displays, motor control, power management, and user appliance control.

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System clock rates up to 80 MHz. And a propagation delay of only 15ns pin-to-pin. That's the kind of performance you get with our new pLSI™ family of high density PLDs. Comprised of four devices ranging in density from 2,000 to 8,000 PLD gates, they give you absolute timing predictability, right from the data sheet. Lattice also offers the ispLSI™ family—an in-system programmable (isp) version of the pLSI family that delivers non-volatile, 5-volt only in-system programming capability.

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CIRCLE NO. 98

The COP820CJ doesn't have a full A/D converter. Instead, it has an analog comparator to test external voltages. With the proper program, you can use the comparator to build a single- or dual-slope A/D converter.

In addition, the μC supports as many as 24 I/Os. These I/Os comprise a 4-bit output port, a 4-bit input port, and two 8-bit programmable ports. The programmable-port pins can be set at a high-impedance input (weak pull-up) or a push-pull output. Four of the programmable pins can directly drive LEDs with as much as 15 mA. The 16-pin DIPs or SOICs have only 12 I/Os.

—**Ray Weiss**

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 721-5000. FAX (408) 730-0764.

μC and software kit tames Appletalk

PCs and workstations can now take advantage of the Appletalk network for desktops and offices. Zilog is releasing a design kit for the two lower layers of the 6-layer Appletalk protocol. With this kit, developers can link peripherals and systems using the Appletalk network. The Appletalk protocol transfers data at 230.4-kbits/sec.

The kit implements the toughest part of the Appletalk protocol, the data-link level—the Local Talk Link Access Protocol (LLAP). The Local Talk protocol is implemented as an assembly-language program running on the Zilog Z80181, an 8-bit microcontroller (μC) for communications processing.

The remaining higher levels of the Appletalk protocol are less timing and processor dependent. They can be implemented on a back-end or host CPU: The Z80181 serves as a front-end communications processor, buffering packets for transmission or for passing back to the host. However, the Z80181 has enough headroom for the complete protocol. It can address as much as 1 Mbyte, and the LLAP implementation takes up only 5 kbytes.

The LLAP supports node-to-node transmission and receipt of data and control packets. Because of tight signal-timing and synchronization constraints, this transmission is the most difficult part of Appletalk to implement. LLAP is a CSMA/CA (carrier-sense multiple-access and collision-avoidance) protocol with synchronous pulse generation and frame transmission and reception for each node.

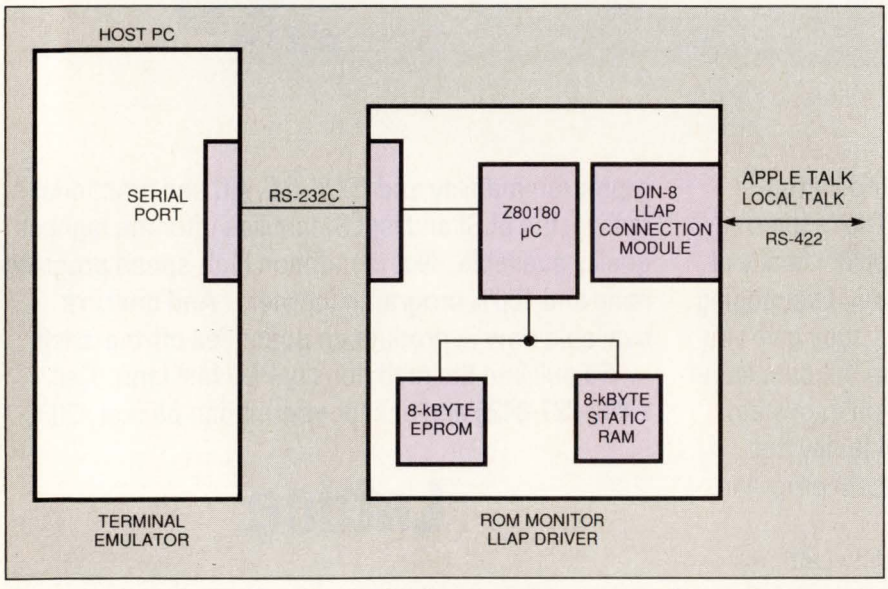
The software kit includes assembly source code for the first two layers of the Appletalk protocol, a hardware evaluation board with a 10-MHz Z80181 μC, the LLAP driver in an 8-kbyte EPROM, 8 kbytes of static RAM (SRAM) for additional user programs, RS-422 drivers, and a DIN-8 LLAP connection module. For PC-host-based debugging, the kit provides a debug monitor and a terminal emulator.

The Local Talk implementation of the physical layer uses an SDLC (synchronous data-link control) frame format with FM0 bit encoding (checks for bit transition on line) and RS-422 as a physical medium with a differential driver and 3-state signals.

Appletalk also defines data-link and physical levels for Ethernet (Ether Talk) and Token Ring (Token Talk). The data-link levels, including Local Talk, encapsulate or strip packets for a network level, which defines a Datagram Delivery Protocol (DDP). The data-link level supports node-to-node packet transmission and receipt. (It does not guarantee packet delivery but does deliver error-free packets.)

The Appletalk LLAP driver kit costs $5,000, including source code. There is no run-time licensing fee.—**Ray Weiss**

Zilog Inc, 210 E Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056.



Help for the toughest part of the Appletalk communications protocol is available in a kit that includes source code and a Z80181 μC-based board.

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Dale® is the partner you need to convert surface mounting from concept to reality. We can save you time by providing a wide range of functions from one proven source.

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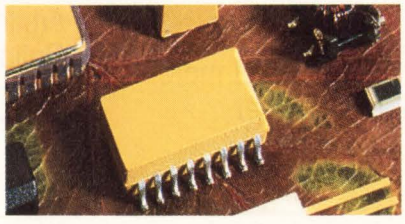

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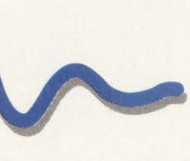
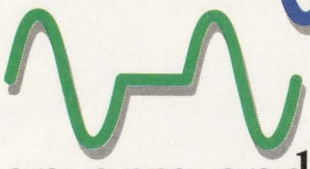
CIRCLE NO. 99

Looking for a function generator with all the bells and whistles, like direct digital synthesis, arbitrary waveforms, and modulation, that doesn't cost an arm and a leg?





Take a look at the DS345 from SRS.

At $1895, it's the only function generator you need.

It's a general purpose signal generator with standard waveforms, frequency sweeps, and synthesized accuracy. It's a 40 Msample/sec arbitrary waveform generator with 16k points of non-volatile memory. It's a complex signal source with amplitude, frequency, and phase modulation, complete with synthesized modulation waveforms. It's a remarkably agile source capable of making phase continuous frequency jumps in only 25 ns. And it's all available at the touch of a button.

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- 30 MHz direct digitally synthesized source
- 1 μHz resolution
- 12 bit arbitrary waveforms
- Fast phase continuous frequency switching
- Low phase noise and distortion
- Sine, square, ramp, and triangle waveforms
- Linear and log sweep with markers
- Frequency, amplitude, and phase modulation
- Arbitrary and burst modulation
- Optional GPIB/RS232 interfaces with Arbitrary Waveform Composer Software

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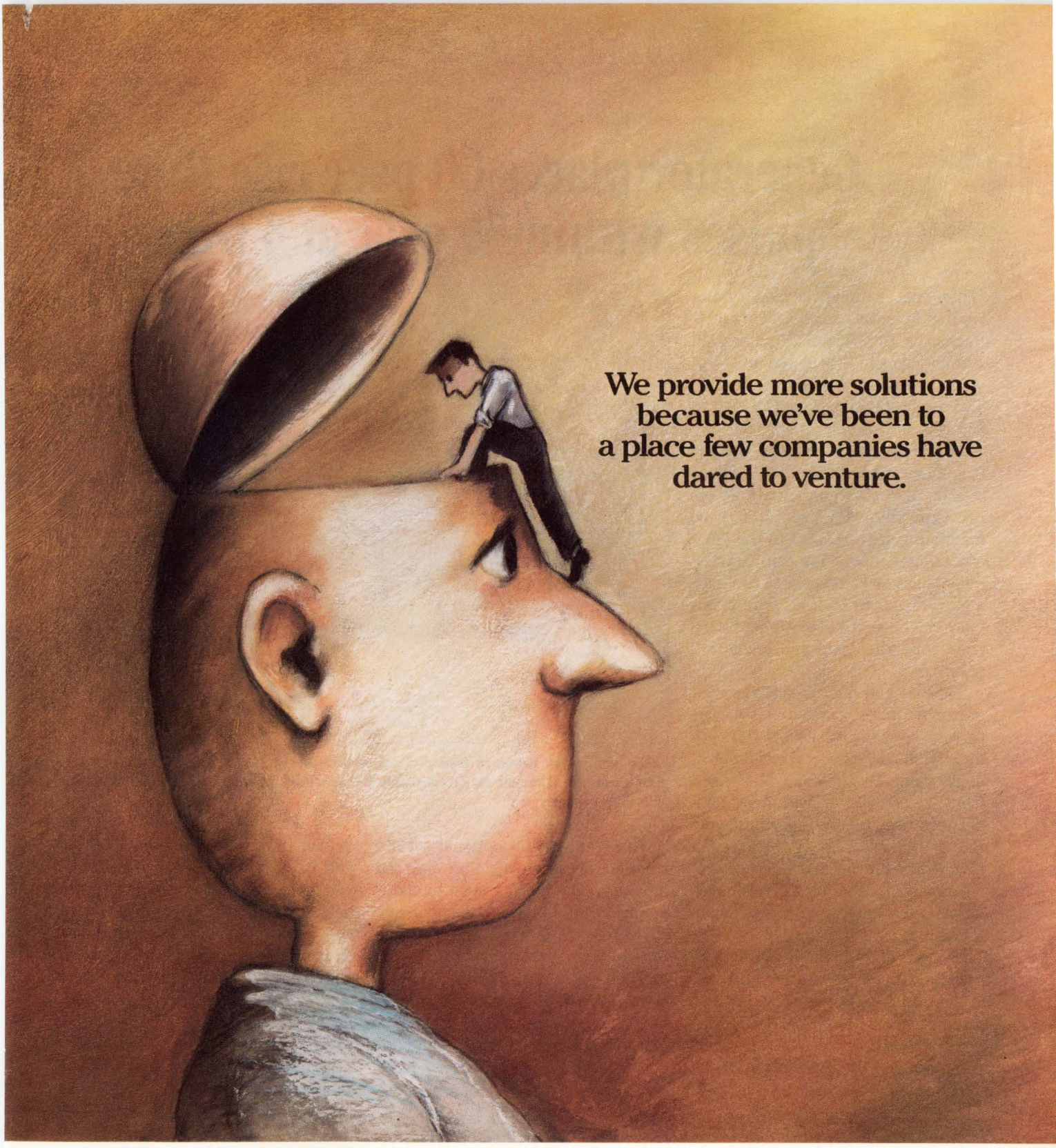

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CIRCLE NO. 101

Generator places 60-psec rise-time pulses within 75 psec at 3 GHz

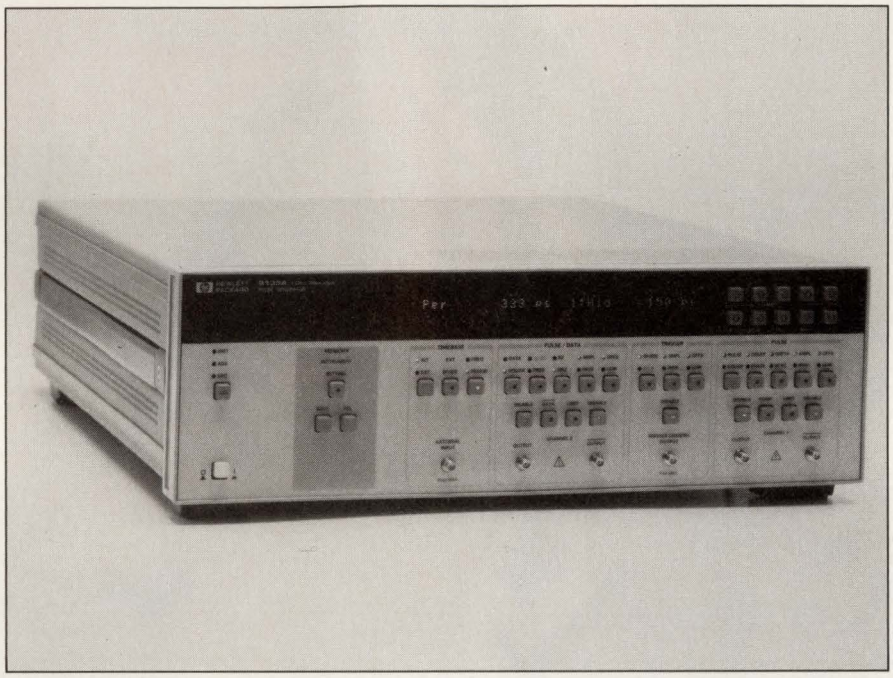
When you examine the fidelity and timing specifications of Hewlett-Packard's 8133A pulse generator, you may conclude that the unit provides just what you are looking for. The price ranges from $27,100 to $45,900, depending on options.

The instrument, whose output frequency extends from 33 MHz to 3 GHz, places its pulses with an error typically <75 psec (150 psec maximum) with respect to the edge of a trigger input. You can vary the pulse delay with respect to the trigger from −5 to 15 nsec. The maximum jitter in this placement is 5 psec rms; the typical jitter is <2 psec rms.

The rise and fall times of the generator's square waves and 150-psec to 10-nsec-wide pulses are 100 psec maximum—60 psec typical—measured from 10 to 90%. Measured from 20 to 80%, which some competitors use in their specifications, the worst-case and typical transition times are 60 and 40 psec, respectively. The generator produces pulses and square waves whose amplitudes into a 50Ω load are 0.1 to 3V.

You can obtain simultaneous normal- and inverted-polarity outputs. If you connect your 50Ω load to ground, you can vary the output offset from −2 to +4V. For work with ECL circuits, you can connect the 50Ω load to −2V. In this case, you can vary the offset from −3 to +3V.

Another feature that's unusual is the generator's optional second output that has some of the attributes of a data generator. Data generators usually have many channels and back each channel with pattern memory; but unlike pulse generators, they rarely offer much control over pulse parameters, such as delay and amplitude.



Pulses and square waves of fidelity at frequencies as high as 3 GHz emanate from this pulse generator. The unit can accommodate a channel that provides many of the attributes of a data generator.

This generator's optional second channel provides a 64-bit pattern memory. Though not deep by data-generator standards, this memory suits testing devices and systems for pattern sensitivity. Moreover, you can connect two or three of the generators in a master/slave configuration, thereby obtaining a 6-channel generator. Instead of choosing a data generator as the instrument's second channel, you can choose a second pulse channel.

A related convenience—for example, for eye-pattern testing of high-speed communications channels—is the generator's ability to produce pseudo-random binary sequences. The length of these sequences can be as great as $2^{23}-1$ periods.

The instrument's designers sacrificed one convenience for the sake of maintaining the unit's output fidelity: If you want to vary the rise and fall times of the output pulses, you must connect accessory filters between the output connector and the cable that drives your load. Making the rise and fall times variable from the front panel would degrade the generator's peak performance.

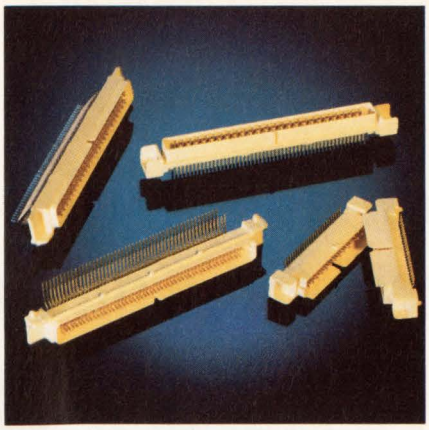
Aside from transition times, you can control just about every other aspect of the unit's output from its panel. A display provides warnings under conditions that degrade performance, such as when you select a pulse width that would produce a duty cycle approaching or exceeding 100%. Estimated delivery time is six weeks ARO.—**Dan Strassberg**

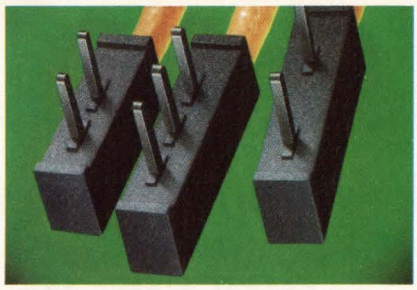
Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

High Density Hermaphroditic Connectors

- *Identical contacts on mating halves*
- *Close pitch .050″ centers*

Meritec 50 ohm, impedance matched Hermaphroditic Connectors feature .050″ centers, with board spacing as close as .394″ (10 mm), making them ideal for dense package applications. Two, three and four row connectors are available, in straight or right angle versions, with through hole or SMT contact tails. Precision, high strength molded terminations are reliable in the most critical applications. The connectors are designed to meet IR or vapor phase reflow requirements.





Impedance matched PCB Solderable Interconnects

- *Solders directly to the PCB*
- *Low profile*

Meritec's PCB Solderable Interconnects can be soldered directly to the PCB for a permanent connection. Pin lengths of .110″ and .160″ are available for different board thicknesses. The impedance matched connectors feature precision, high strength molded terminations for reliability in critical applications. Available in 1×2 and 1×3 configurations, the connectors are side-to-side stackable and feature heights as low as .150″ from the PCB, making them ideal for dense package applications. The connectors can be terminated to a variety of different cable styles.

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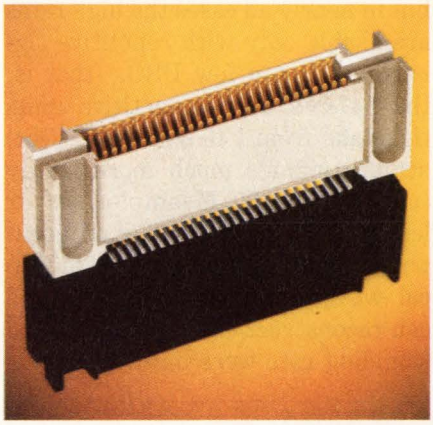


Close Pitch Card Edge Connectors

- *.050″ centers*
- *50 Ω impedance matched*

Meritec's high density Card Edge Connectors are designed with .050″ centers to minimize board space requirements. The 50 Ω, impedance matched connectors are ideal for high density board-to-board applications. The connectors are designed to meet IR or vapor phase reflow requirements. Through hole and SMT contact tail configurations are available. Precision, high strength molded terminations provide reliability in critical applications.

Modular scope takes 4G 8-bit samples per sec in real time on two channels

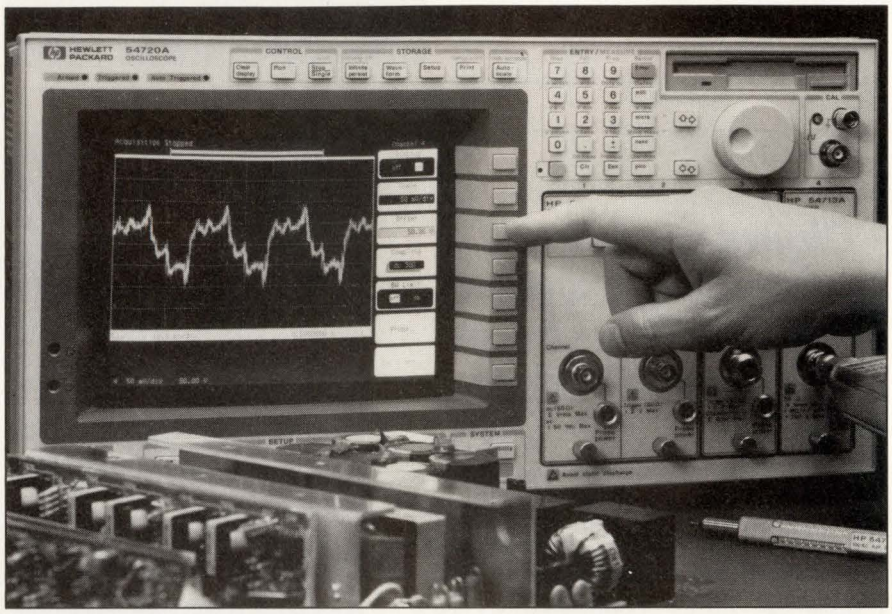
If you've wanted a good picture of transient signals containing frequencies higher than approximately 0.5 GHz, you've had to use specialized instruments such as scan converters. Although such instruments are faster than most digital storage oscilloscopes (DSOs), they are also more expensive. Hewlett-Packard's 54720A DSO solves this problem for single-shot signals to 1 GHz by taking 4G 8-bit samples/sec on each of two channels. The 54710A scope takes 2G 8-bit samples/sec on each of two channels. See **Table 1.**

You can find many DSOs that offer *effective* sampling at GHz rates, but in nearly all cases the high rates are usable only with repetitive signals. All but a few DSOs (that is, the 547xx's and competitive units that take from 1 to 2 Gsamples/sec) acquire signals much more slowly (usually at 200 Msamples/sec or less). By capturing data at different points on many repetitions of identical waveforms, the slower scopes can reconstruct the signals as if the sampling rate were much greater.

Table 1—HP547xx sampling rates vs channels

Model	Number of channels	Sampling rate for each channel (in Gsamples/sec)
54720A	2	4
	4	2
54710A	2	2
54710A (with upgrade)	2	4
	4	2

But repetitive sampling doesn't work with signals that don't repeat or that repeat only once in a blue moon—metastable states are a good example. If you try to view such signals with a repetitive-sampling scope, you may not live long enough to acquire the samples you need to get a good idea of what's going on.



A high-resolution, touch-sensitive, color display; a numeric keypad; a floppy-disk drive; a numeric keypad; and room for four single-width (or two double-width) plug-in modules distinguish the HP 54720A's front panel.

To capture transients, you need fast *real-time* sampling, but suppliers differ on the number of samples per cycle a scope must take to provide adequate waveform reconstruction. Although, in theory, you can reconstruct a signal that you have sampled slightly more than twice in each cycle, a rate of 4 samples/cycle is more practical and 10 or more samples/cycle are better yet. Using the DSP technique of reconstruction filtering, a scope can do a respectable job of waveform reconstruction at the lower 4-sample/cycle rate. This ratio limits the 54720A's single-shot bandwidth to 1 GHz. For repetitive signals, both the 54720A and the 54710A have a bandwidth of 1.5 GHz.

Other specifications worth noting are measurement of time intervals with less than 30-psec error and a resolution of less than 1 psec; timing jitter of less than 5 psec rms; triggering on glitches as narrow as 500 psec; less than 300-μV rms noise; 9-bit resolution at 500 Msamples/sec; and 12-bit resolution with averaging. The scopes offer 32k words of memory on two channels and 16k words on four. They have high-resolution color displays.

The 54720A scope costs $42,900, and the 54710A DSO costs $29,900. Prices for plug-in modules range from $2400 to $4700, and a 2.5-GHz active probe with power supply costs $3500. Delivery takes approximately 16 weeks ARO.

—Dan Strassberg

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA, 95014. Phone (800) 752-0900.

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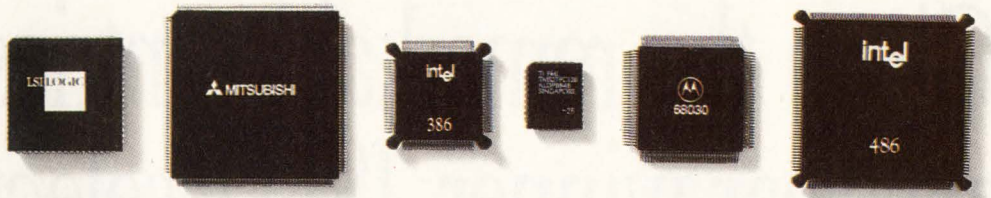

It seems like every time you turn around, another device appears on the scene. Smaller SMDs, finer pitched leads, congested boards. Device testing has become a real challenge.

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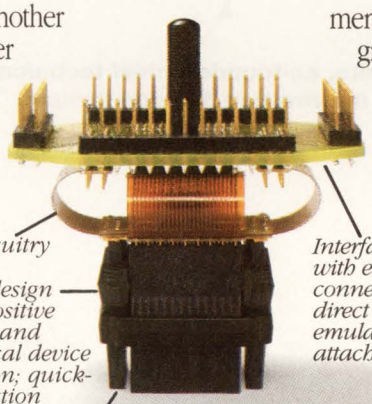

FIN clips "lock-on" to high pin count (100-, 132- and 196-pin) JEDEC plastic or ceramic QFPs, and you can choose from three styles in each pin count to work best with your equipment. There's a platform with .100" headers for easy grabber attachment or connection to industry standard (IDC) connector cables, another with .050" connectors on flex circuitry for direct attachment to your own emulation board, or a FIN clip with integral .050" connectors for interface with most instrument ribbon cable assemblies.

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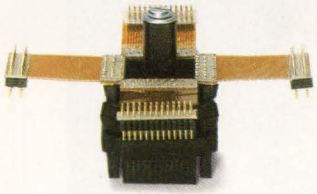
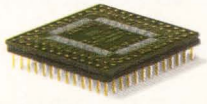


PQFP clip with flex-circuitry-to-.050" connector interface.



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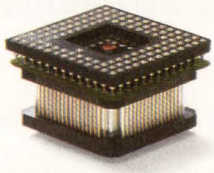

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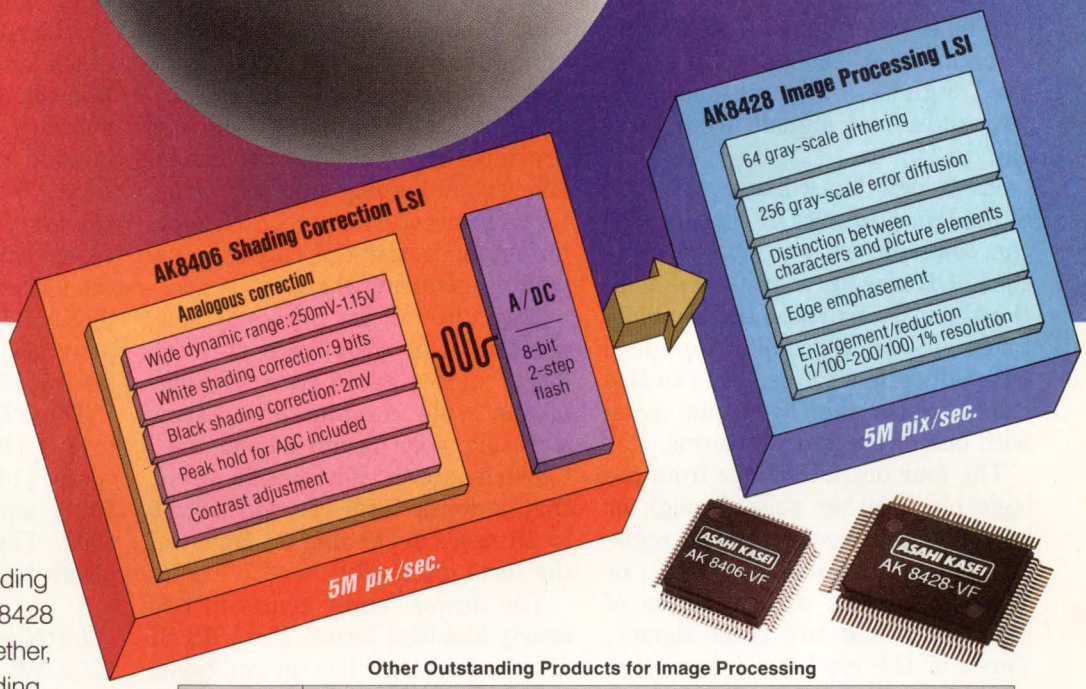

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High-density PLD offers speed and in-system programmability

The PLSI 1032 and ISPLSI 1032 are the first two members of a high-density programmable-logic-device (PLD) family based on electrically erasable CMOS. The base technology allows the ISPLSI device to be in-system programmable.

The basic logical unit of the devices is a logic block, offering 20 product terms. The terms can use the true and complemented forms of as many as 16 internally generated signals and have access to two additional signals from dedicated I/O pins.

Each logic block has two 4-, one 5-, and one 7-input OR circuits. You can combine the output signals of these OR circuits if you need additional width or bypass the combinatorial circuitry if you need top speed with only a few terms. You can also Exclusive-OR the OR output signal with one of the product terms.

The four output signals from the logic block either pass through or bypass output registers. The registers are configurable as D-, JK-, or T-type registers with a choice of four clocks and two reset signals. Three of the clocks and one reset signal are common to all the logic blocks; the remaining signals are product terms from the block. The devices offer one register for each OR gate, but the registers are not dedicated to the gates.

Although all logic-block output signals are available internally to the product terms, signals destined for the outside world must pass through an output routing pool before reaching I/O cells. The devices group eight logic blocks together on each device edge, with each group having its own output routing pool and 16 I/O cells.

The routing pool gives you flexibility in I/O pin selection. Each of the 32 logic-block output signals in the group has a choice of four I/O cells. As with the combinatorial circuitry in the logic blocks, you can bypass the routing pool for greater speed but no choice in I/O pin.

You can configure the I/O cells as input ports, output ports, or bidirectional ports, with each port type offering options. Input ports can simply buffer signals, latch them, or register them. Output ports can buffer signals, either with or without inverting them. They can also provide 3-state buffers, with the enable signal coming from a product term. Bidirectional ports can simply buffer, or buffer the output signal while registering the input signal.

If you use all the bypass options, a signal can propagate through either device in 15 nsec. Because of the wide combinatorial terms available, your design may not need to use feedback. If it does, however, the feedback term can add from 9 to 16 nsec, depending on fanout of the term internally.

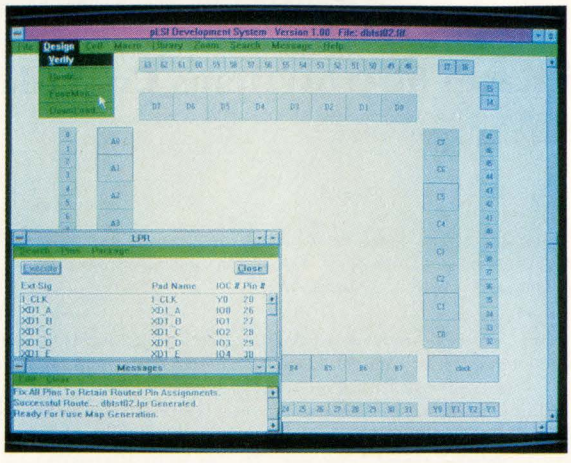
The device family comes in two nearly identical forms. The ISPLSI device, however, has an additional attribute. Four of the device's I/O pins serve double duty as programming pins, allowing you to clock in and load a serial programming pattern while the device is in a system. This in-system programmability lets you build your system, even your prototype, without sockets for the PLD, thus decreasing noise and increasing system speed.

The company supports its devices with an array of programming tools. The basic software runs on a DOS-based computer under Windows and allows schematic and Boolean design entry. It comes with a library of 240 macro functions that include most common TTL functions. You can also edit these macros or create your own. If you already have a design entry system, the software can serve as back-end, place-and-route software. The company also offers an engineering kit for the ISPLSI device.

The PLSI 1032 ranges from $49 to $81 (1000). The ISPLSI device costs $142 (100). Software costs $995, and the engineering kit is $395. The devices come in 84-pin plastic-leaded-chip-carrier packages.

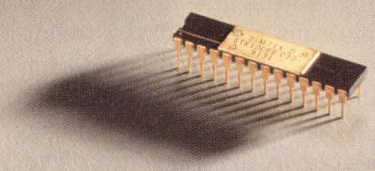
—Richard A Quinnell

Lattice Semiconductor Corp, 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-0347. TLX 277338.



The PLSI and ISPLSI programmable logic devices offer combinatorial logic blocks with flexible I/O pin mapping. They are supported by Windows-based design, place, and routing software.

Batteries not included.



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CIRCLE NO. 105

Cache tag RAMs offer 12-nsec validated match with extras

The CY7B180 and CY7B181 cache tag RAMs not only offer 4k × 16-bit tag memory, they include functions such as chip-select decoding and the logic needed for validating matches. They also include two status bits for each memory location and an additional data port to speed copy-back cache designs.

The devices' base structure is 4k × 18 bits. Each word location stores a 16-bit tag and two status bits. You use the devices for storing the lower-order address bits for the memory you have copied into cache. When the processor addresses a memory location, the tag RAMs respond with a match signal within 12 nsec if that address has been cached.

Several built-in functions can simplify your cache design. You can read from and write to the tag data and status bits independently. This operation allows you to update status without having to do a read-modify-write on a combined tag and status word. Another function allows automatic generation of a write output signal to the cache RAM when the tag RAMs detect a valid write hit.

A design-simplifying attribute comprises two separate ports: one for tag data and one for the address-match comparison data. The latter port provides the contents of a tag RAM whenever a match occurs. With a single port, you would have to multiplex address and data lines to the tag RAM in order to read back tag data. The separate ports eliminate that need. All ports, as well as the command lines, are internally latched and can operate in latch or clocked mode.

When replacing a cache line that has "dirty" data, you need to use the tag data to find the address in main memory that needs changing. Having that data available automatically when the tag RAM is addressed, rather than having to read it back through the match-comparison port, speeds the copy-back process.

The tag-RAM array (**Fig 1**) includes status bits for each tag location. The CY7B180, intended for use in a multiprocessing application, uses the two bits to code the corresponding tag data's status as modified, exclusive, shared, or invalid. The CY7B181, intended for use in a uniprocessing application, uses one status bit to represent whether or not the tag data is valid. It uses the other status bit to let you know whether the data is "dirty,"—that is, modified but not yet updated in main memory. The device automatically sets the "dirty" bit if it detects a write hit.

The 181's on-chip valid bit allows it to perform validated matches. When you present the address in question to the RAM, it will respond by indicating whether that location has been tagged and whether the tag is valid. You can clear individual valid bits in a memory cycle or clear all valid bits simultaneously in two memory cycles.

The devices have four chip-select lines—two low-true and two high-true. When the device is not selected, all of its outputs switch to high impedance. This combination of features allows you to cascade as many as four devices, forming a 16k-word RAM array, without suffering a speed penalty. Simply use the two most significant address bits to drive the appropriate chip selects and wire-OR the output signals.

The CY7B180 and CY7B181 come in 68-pin plastic leaded chip carriers and cost $72.05 (100).

—Richard A Quinnell

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. FAX (408) 943-2741.

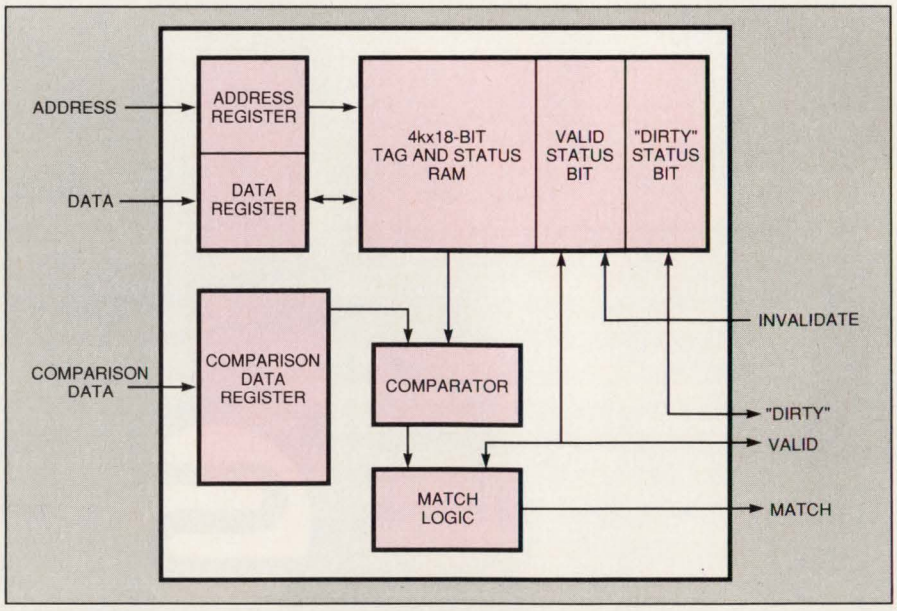

Fig 1—More than just tag RAMs, the CY7B180 and CY7B181 devices incorporate status bits, validation logic, and an additional data port.

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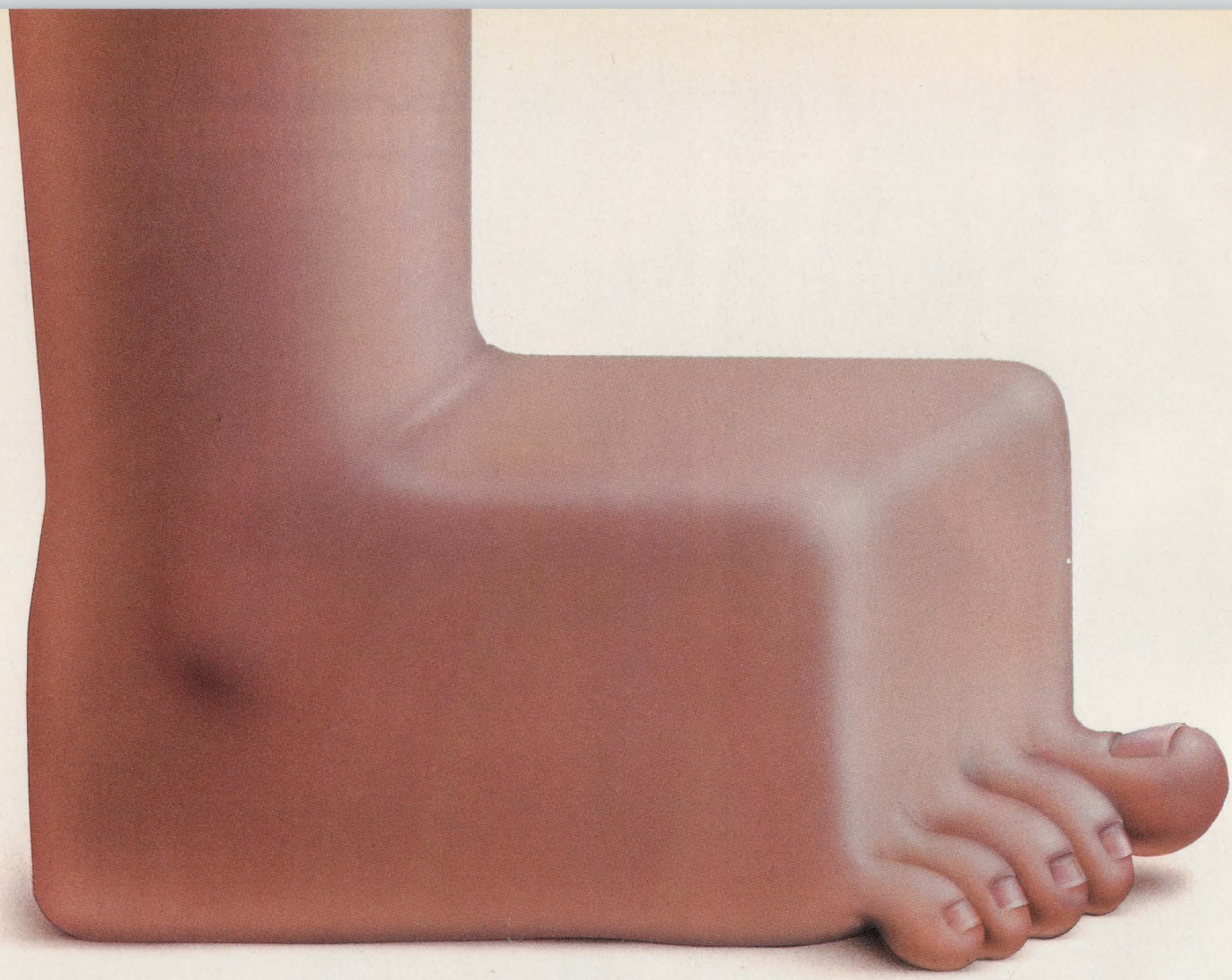

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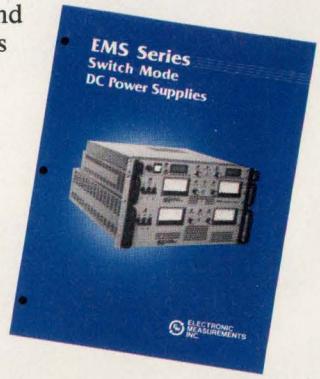

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CIRCLE NO. 38

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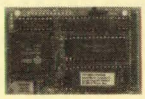

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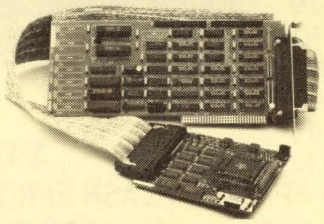

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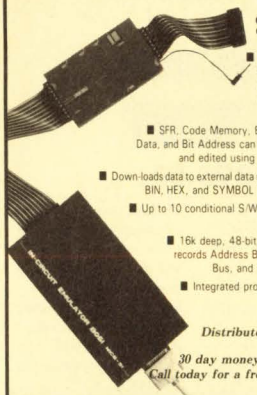

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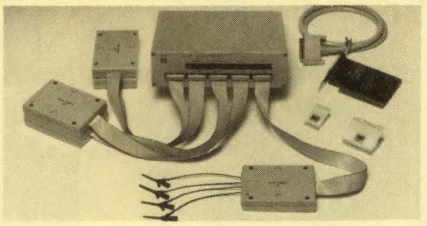

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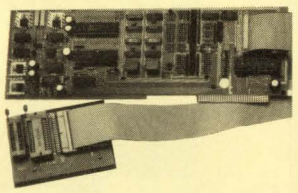

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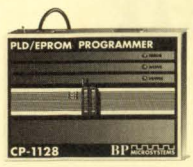

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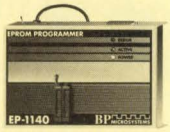

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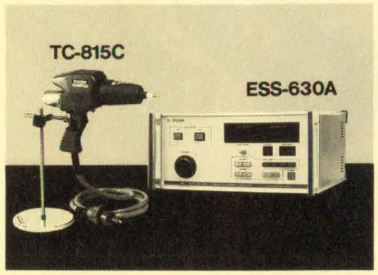

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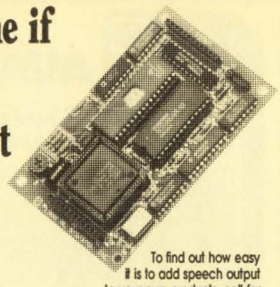

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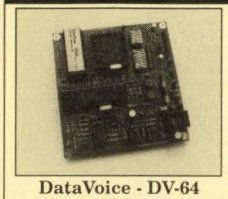

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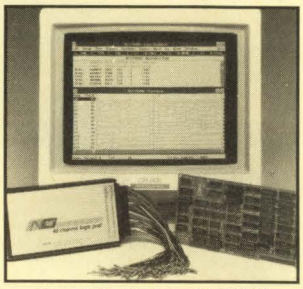

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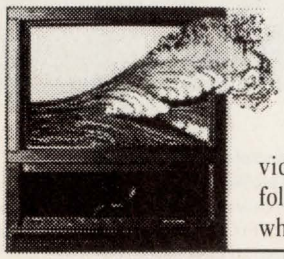

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Manage SWQA group including functional, system and performance testing; development/implementation of release processes, system life cycle, QA measurements and automated testing. Requires at least 5 years' experience managing a SWQA function. Experience in Com-munications or Systems QA would be helpful.

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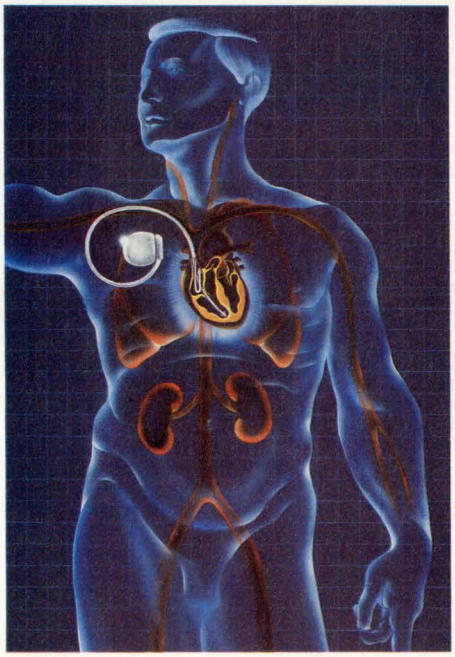

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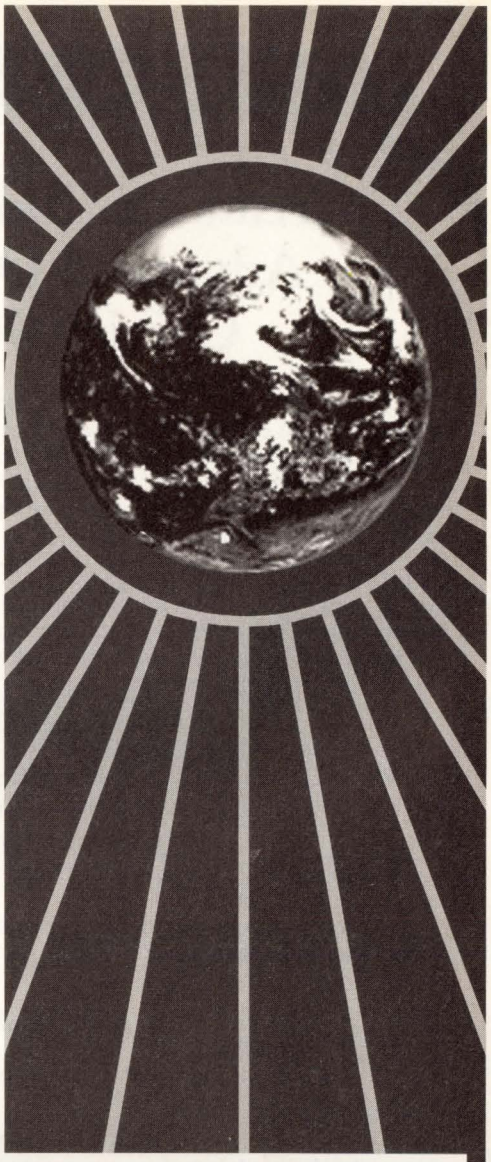

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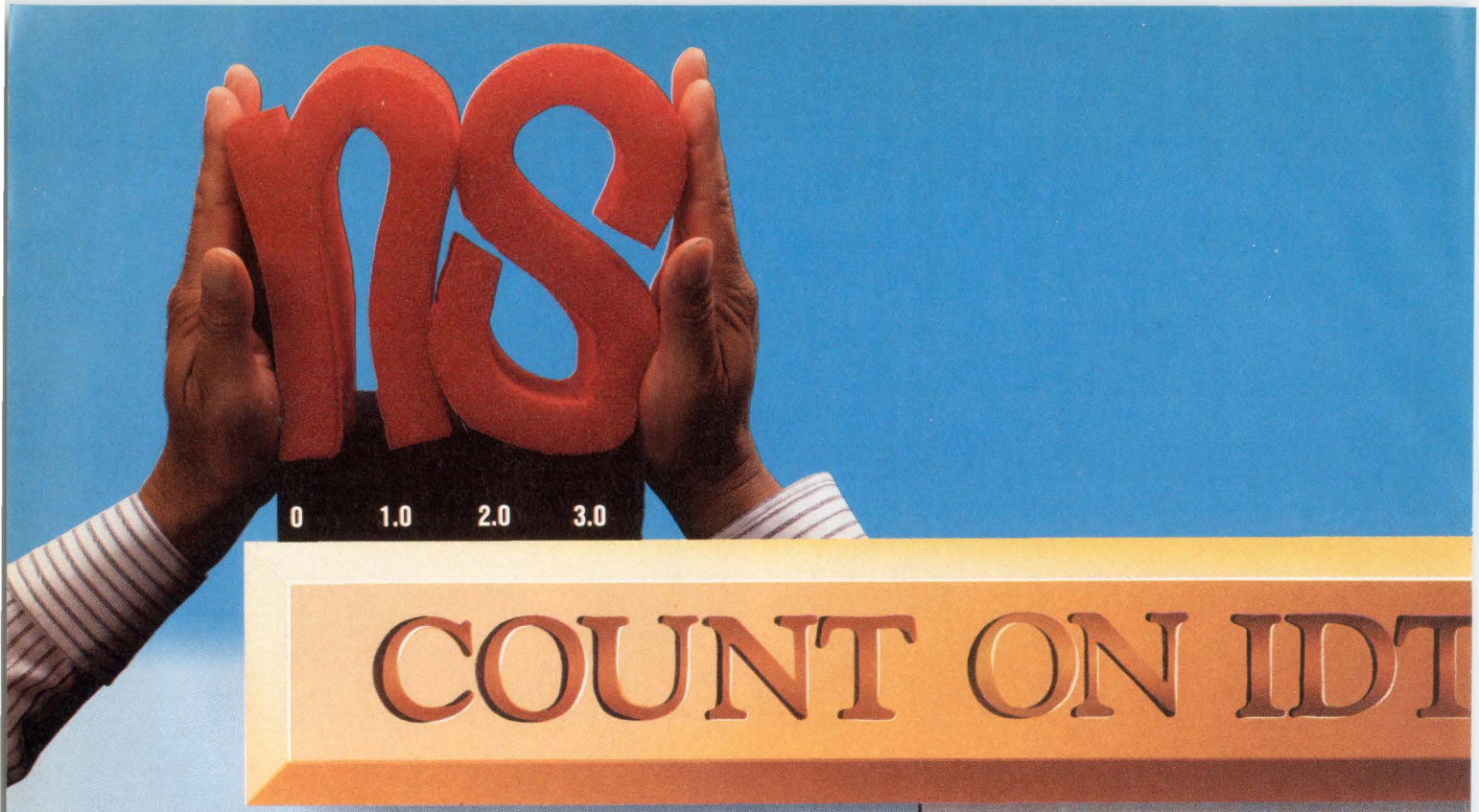

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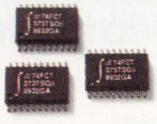

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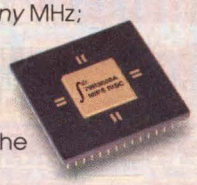

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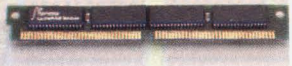

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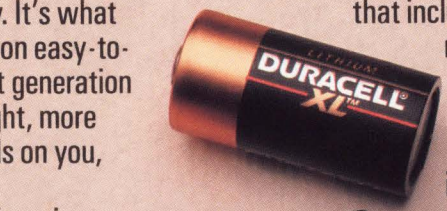

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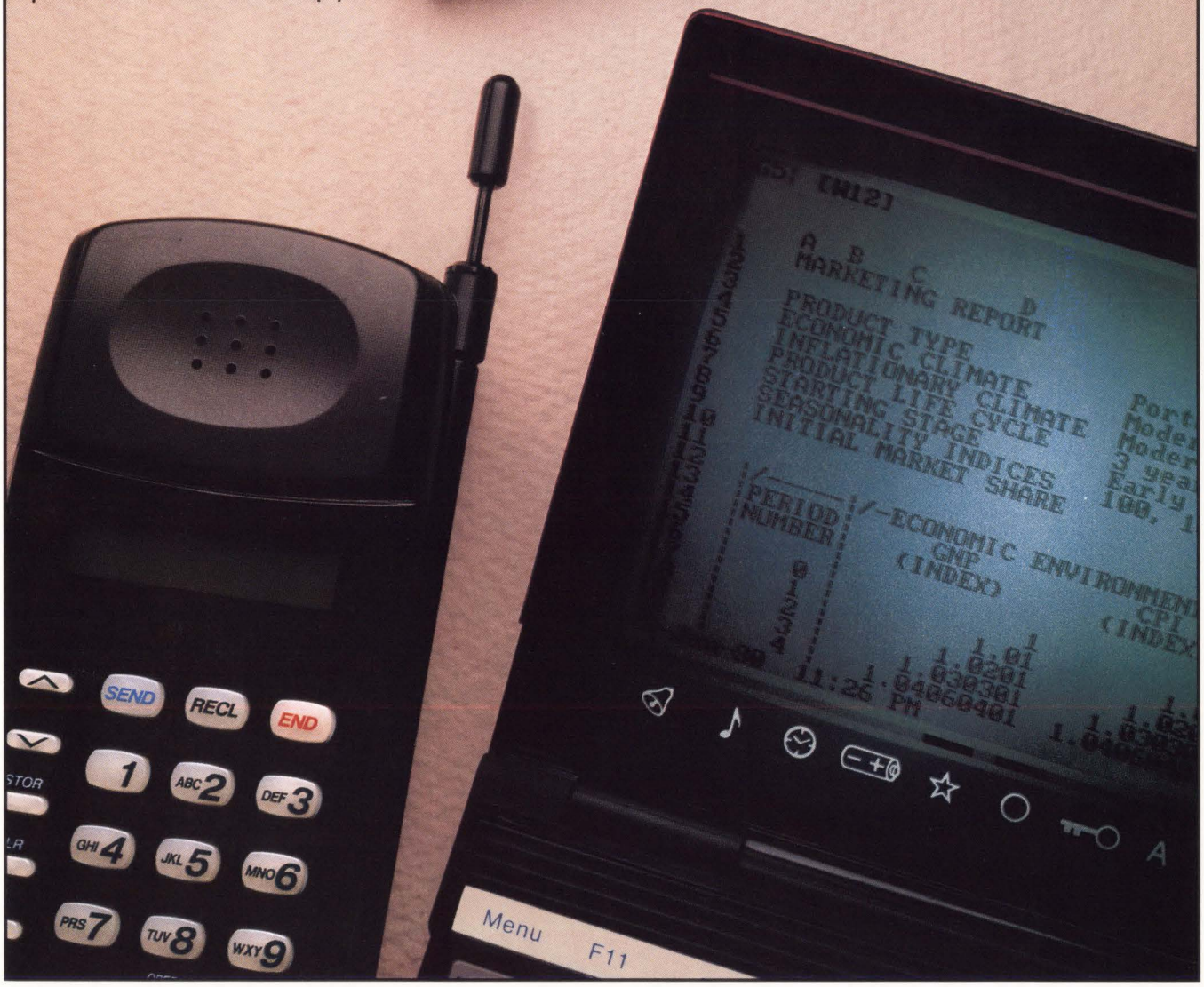

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