PROCESSOR UPDATES PG 114

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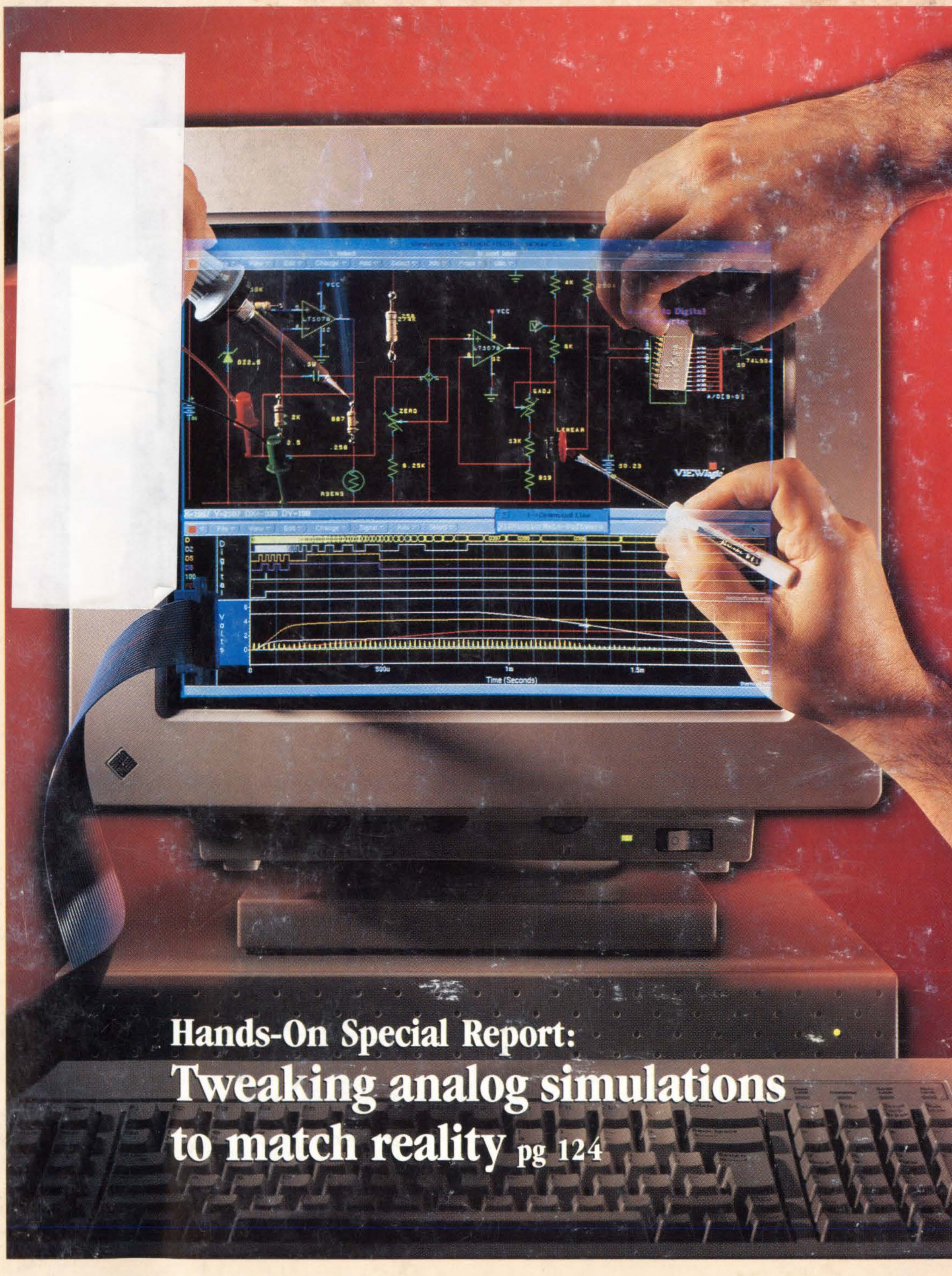
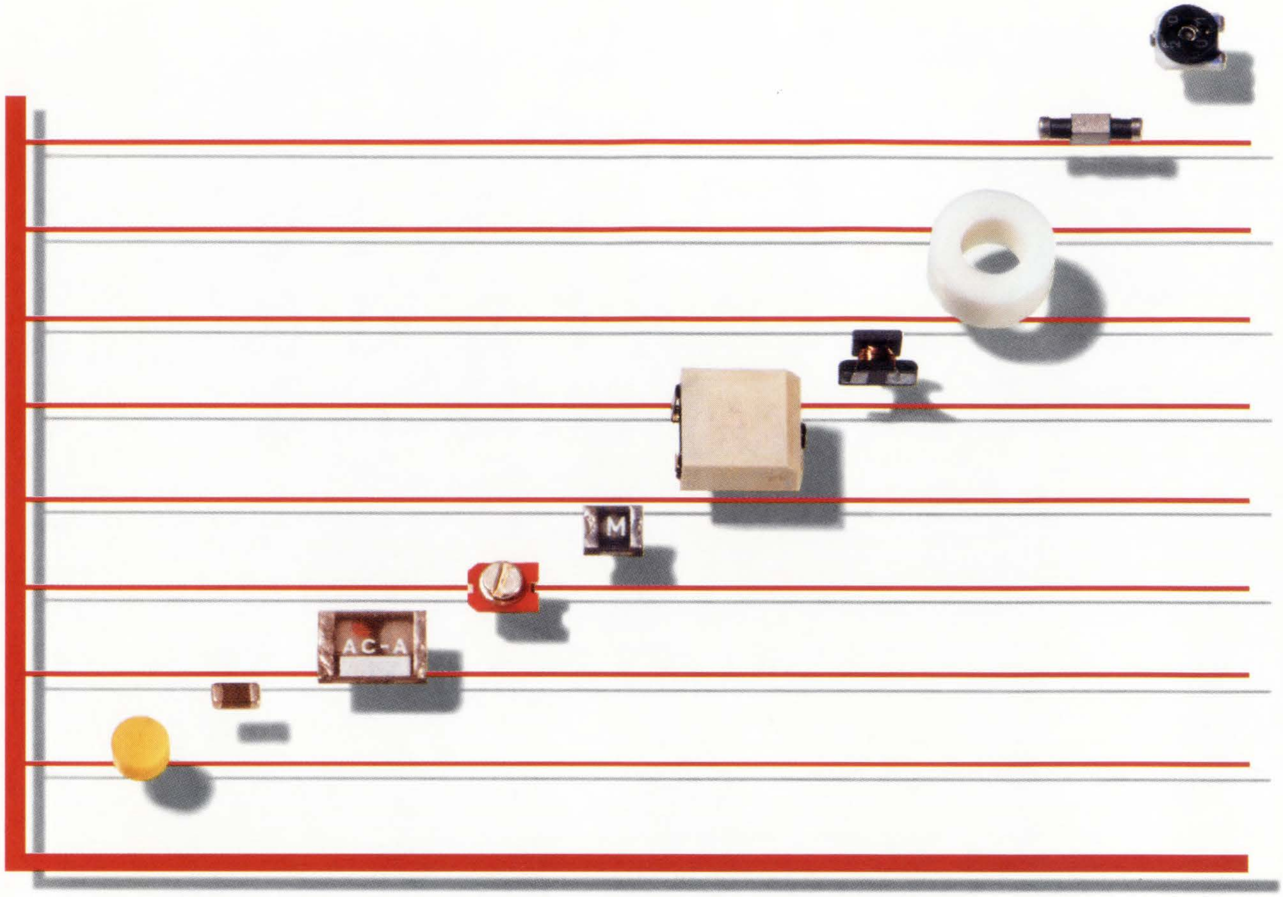
A CAHNERS PUBLICATION

MAY 21, 1992

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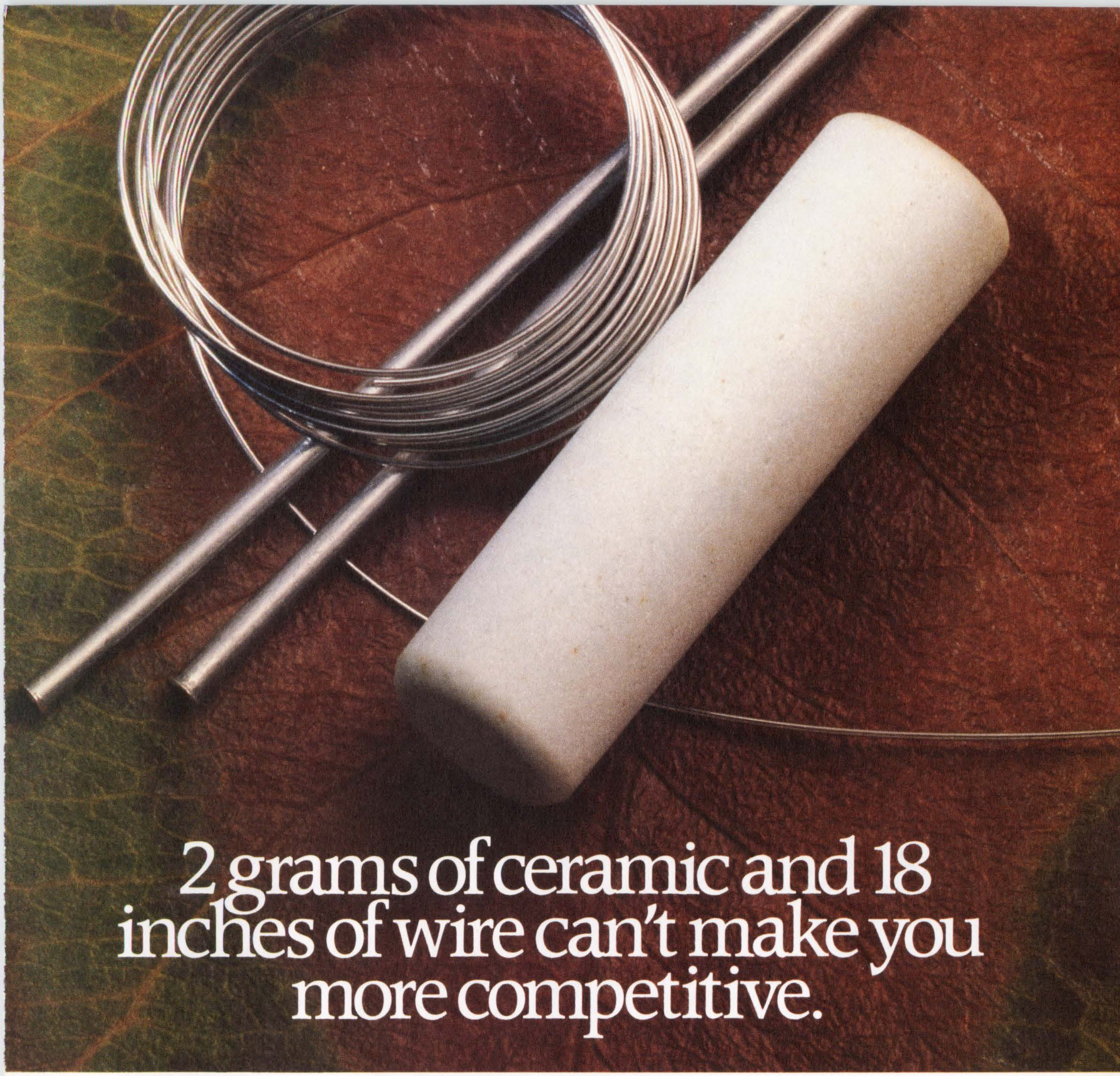

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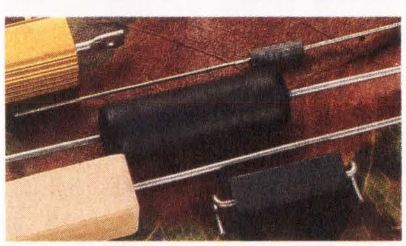

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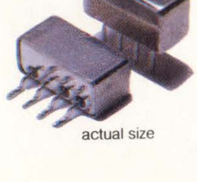

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SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\overline{X}$	Conv. Loss (dB) δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9..95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
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TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.
■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_U/2$)
δ = Sigma or standard deviation

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CIRCLE NO. 4

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EDN
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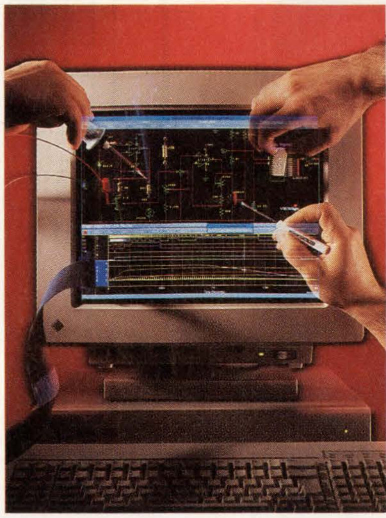
MAY 21, 1992 VOLUME 37, NUMBER 11

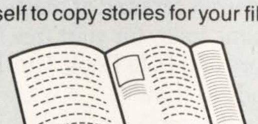
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: EDN's Hands-On Special Report puts DOS-based analog-simulation software to the test and finds out how it measures up to several circuits' actual performance. (Photo courtesy Viewlogic Systems; photography by Jon Chomitz) . . . . **PAGE 124**

Foldout contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



ANALOG TECHNOLOGY SPECIAL ISSUE

Continued on page 7

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EDN
MAGAZINE EDITION

MAY 21, 1992

Continued from page 5

EDN's technical editors selected National Semiconductor's Dispatch chip set and software as an innovative new product and thus named it this issue's *Editors' Choice*. Turn to the Processor Update section to learn how this product can enhance your office-machine technology. . . . . **PAGE 114**

PRODUCT UPDATES

PROCESSOR UPDATES

DESIGN IDEAS

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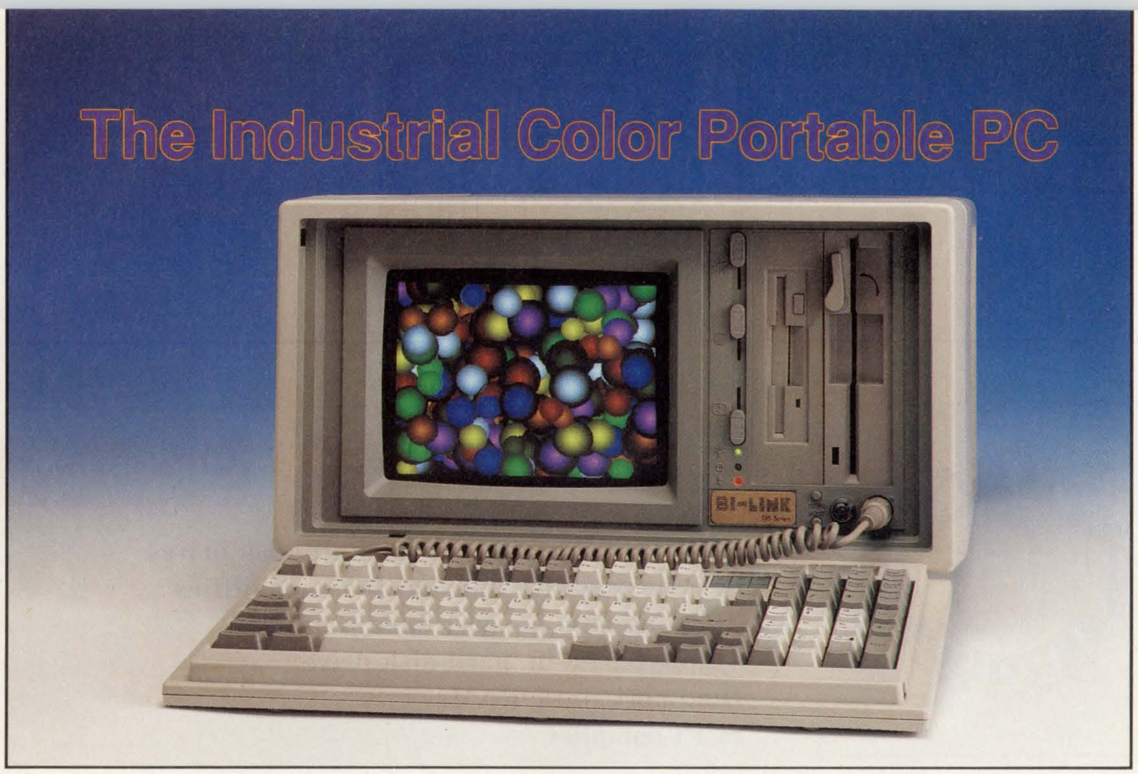

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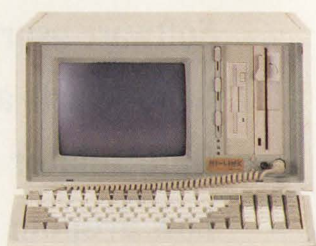

9" Color SVGA Monitor
This high resolution color monitor is suitable for all industrial and commercial applications. It is ideal for special project cabinets, data acquisition stations, point of sales machines, system control centers, vending machines, security systems and on.

PORTABLEworkstation System
A portable computer that comes with a choice of 486-33, 386-33 and 386-25 CPUs and a hard disk drive of up to 500MB! Three full length ISA or EISA expansion slots are available for add-on peripherals. The display is a high contrast gas plasma screen.

PORTABLEdesktop System
The PORTABLEdesktop is a desktop computer in disguise. This portable come with a choice of 3 processors: 486-33, 386-33 and 386-25. An affordable scientific instrument as well as a powerful PC complete with a built-in color SVGA monitor.

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The IPC comes with a built in 9" color SVGA or a monochrome MGA monitor. An 8 slot ISA backplane is standard for add-on CPU cards for the lowest MTBR. Two 3.5" drive slots for floppy and hard disk drive are standard and available CPU cards including 286, 386SX/DX and 486SX/DX CPU.

Bi-Link Computer Inc. 11606 E. Washington Blvd. Suite AB, Whittier, California 90606 Tel: (310)692-5345 Fax: (310)695-9623.

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MAY 21, 1992

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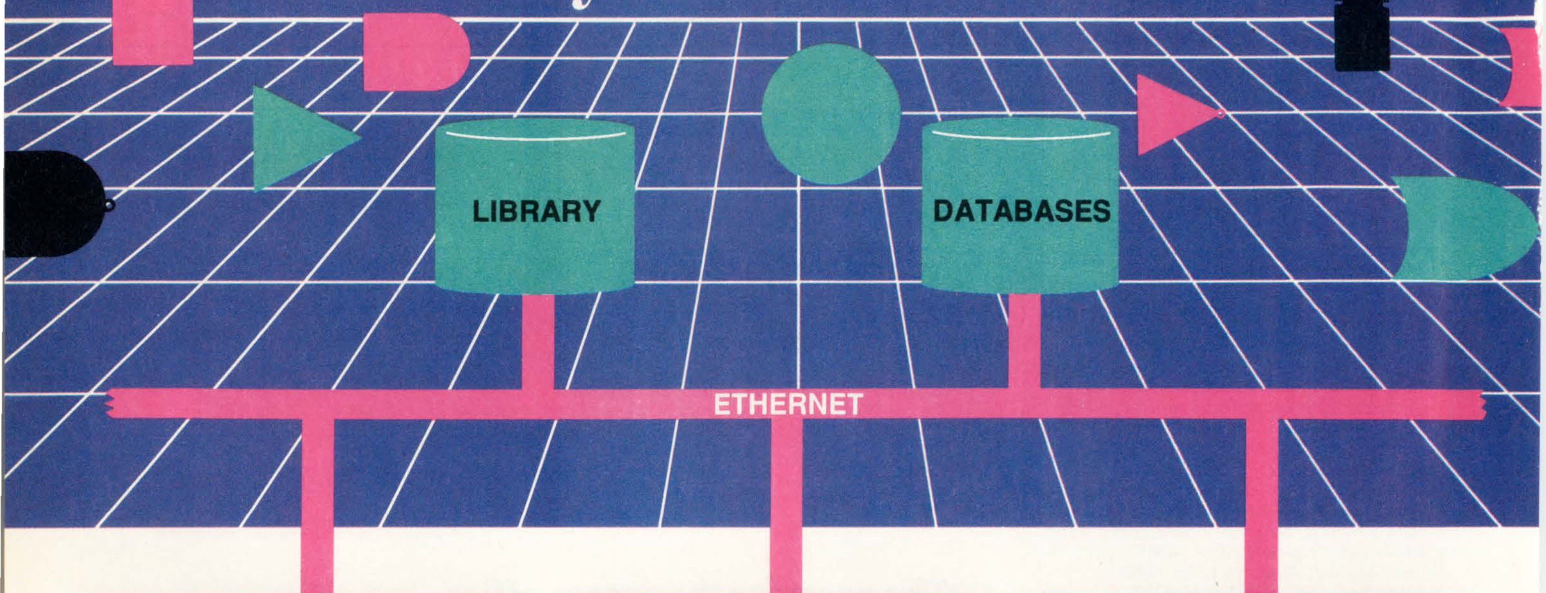
EDITORIAL

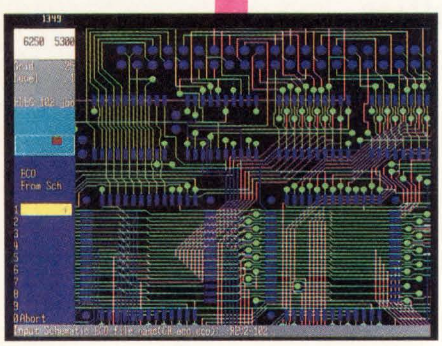
PROFESSIONAL ISSUES

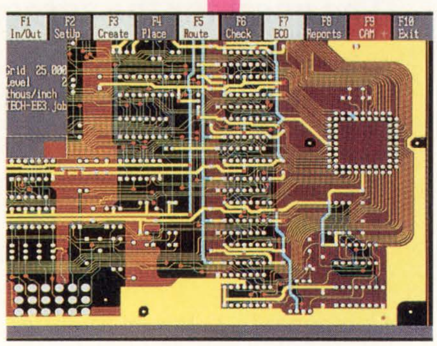
NEW PRODUCTS

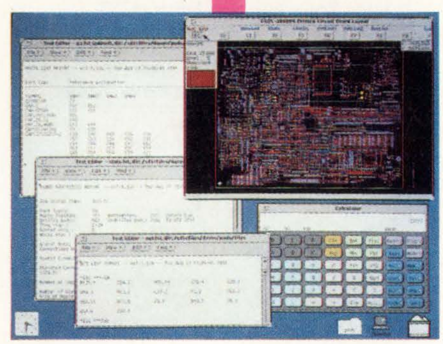
DEPARTMENTS

FINALLY, One Company Offers an Integrated Design Solution for Every Hardware Platform









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INSIDE EDN

A summary and analysis of articles in this issue

In this issue's Special Report, Technical Editor Anne Swager evaluates several **DOS-based analog simulators.** For this test, veteran analog writers Jim Williams of Linear Technology and Bob Pease of National Semiconductor contributed analog circuits that they had built, tested, and written about. The test circuits really stress the simulators' component-simulation models and the ability of the simulators to model the second-order interactions between circuit components.

We gave these four well-documented and -characterized analog circuits to eight simulator vendors to see how well their simulators could predict the behavior of these admittedly difficult circuits. The results varied widely. Read the article to discover why and to find out Anne's conclusions. You'll also want to read Anne's sidebar "Ask reasonable questions to get reasonable answers," which summarizes her hard-won recommendations for getting the best results from any analog simulator.

The Special Report examines DOS-based analog simulators.

Schematic-entry and pc-board-layout software has become far more pervasive than simulation, and vendors offer a large number of competing products, especially in the hotly-contested PC arena. To help you pick a product, Technical Editor Doug Conner presents the first of a series of hands-on product reviews in his Technology Update. In this issue, Doug reviews Accel Technologies' Tango-Schematic and Tango-PCB Plus.

Doug is using these packages to design a pc board for the record-and-playback circuit he created during his hands-on FPGA design project that ran in our April 9 and April 23, 1992 issues. By designing and building a real board, Doug is exercising all of the features you'd use. Consequently, he's learning a lot about these software products. In future issues, Doug will discuss similar products from other vendors.

Although we focused on software in this issue, we didn't neglect hardware. Technical Editor Richard A Quinnell looks at **specialized PLDs** in his Technology Update. These parts can save you board space, power, or component cost by providing a design solution that is more efficient than general-purpose devices. PLD specialization ranges from high-output-current drivers to the speed-optimized architectures of PLD-based address decoders. Richard also discusses the reasons why you might *not* want to use specialized PLDs in your design.

Steven H Leibson
Executive Editor

Am386 Microprocessors.

And of course, they're proven-compatible with the IBM® standard.

Best of all, they're available now, available in quantity, and available at surprisingly low prices.

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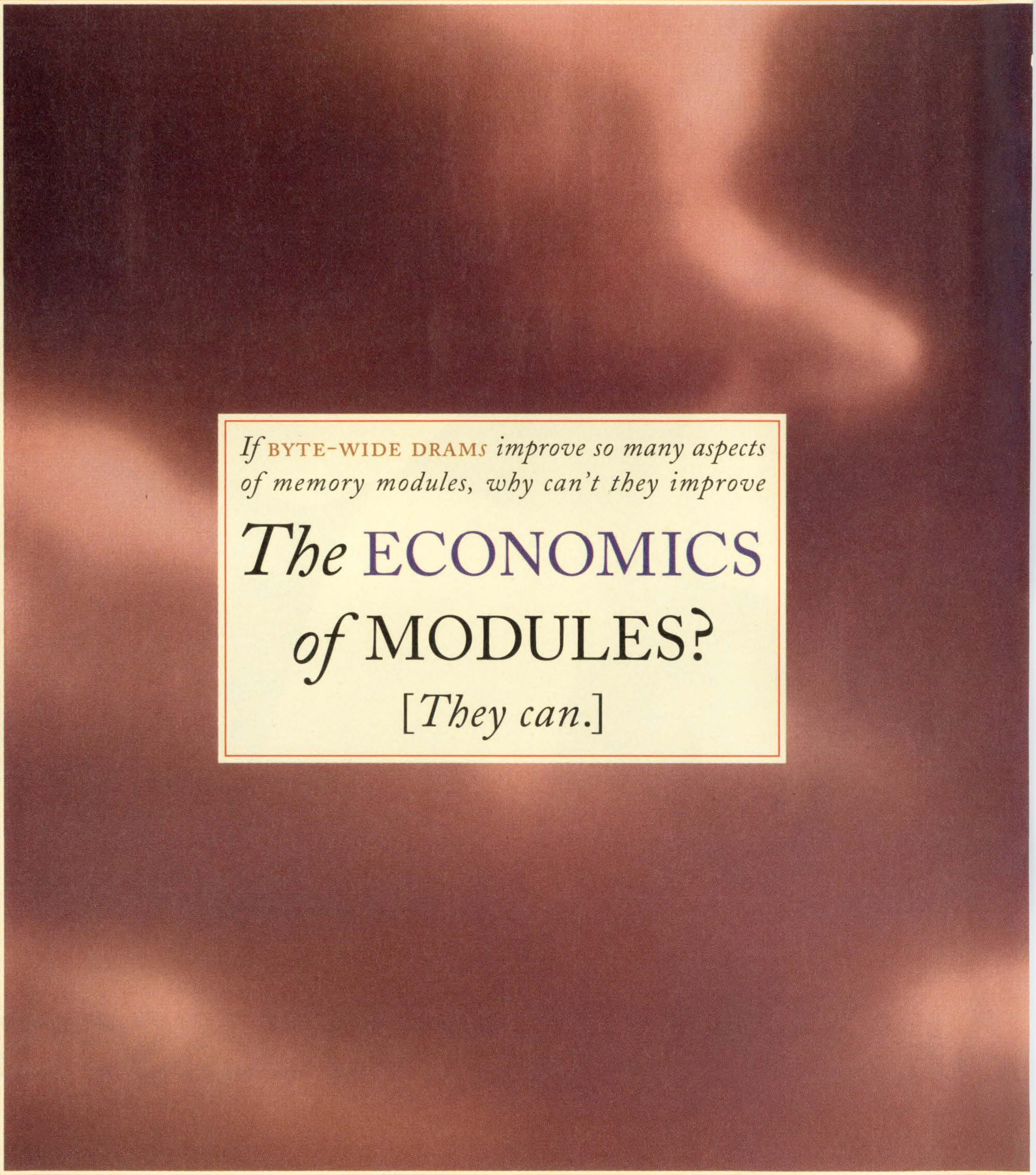

If BYTE-WIDE DRAMs *improve so many aspects of memory modules, why can't they improve*

The ECONOMICS *of* MODULES?

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Byte-wide DRAMs in memory modules. When you compare a 4-meg byte-wide with the normal combination of 1-megs and 256K's, you find that one chip can replace six.

Now that in itself sounds pretty good. And it gives you lots of design advantages.

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But now byte-wides also give you an advantage in *cost*—on x36 modules like the 256Kx36 and 512Kx36.

Because the single byte-wide costs less than the six chips it replaces.

HOW ENGINEERING SEES OUR NEW 32-BIT INTEGRATED PROCESSOR.

Actually, a bullet doesn't do it justice. But you get the picture. Motorola's new 68330 integrated microprocessor is fast.

And well it should be. After all, it gets its firepower from a 68020-based core processor that's optimized to run on a 16-bit data bus. So you get 32-bit microprocessor performance with the economy of a 16-bit memory system.

68000 MICROPROCESSOR FAMILIES					
68000 CPUs Architectural Integration	000	020	030	040	
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68300 INTEGRATED Functional Integration	302	330	331	332	340

Motorola's 68000 families let you choose the performance and integration that's right for your application.

As the simplest and lowest priced member of the 68300 family, the '330 is an ideal companion to your favorite peripheral circuits. Even if you've already combined them into an ASIC or custom circuit.

What's more, the 68330's Systems Integration Module comes already loaded with system glue logic. Saving you the trouble of designing in functions like clock

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HOW PURCHASING SEES IT.

generation, chip selects and interrupt control.

And, since the '330 is fully binary software compatible with all members of the 68000 and 68300 families, it provides a seamless migration path, reams of reusable code, popular operating systems and familiar development tools.

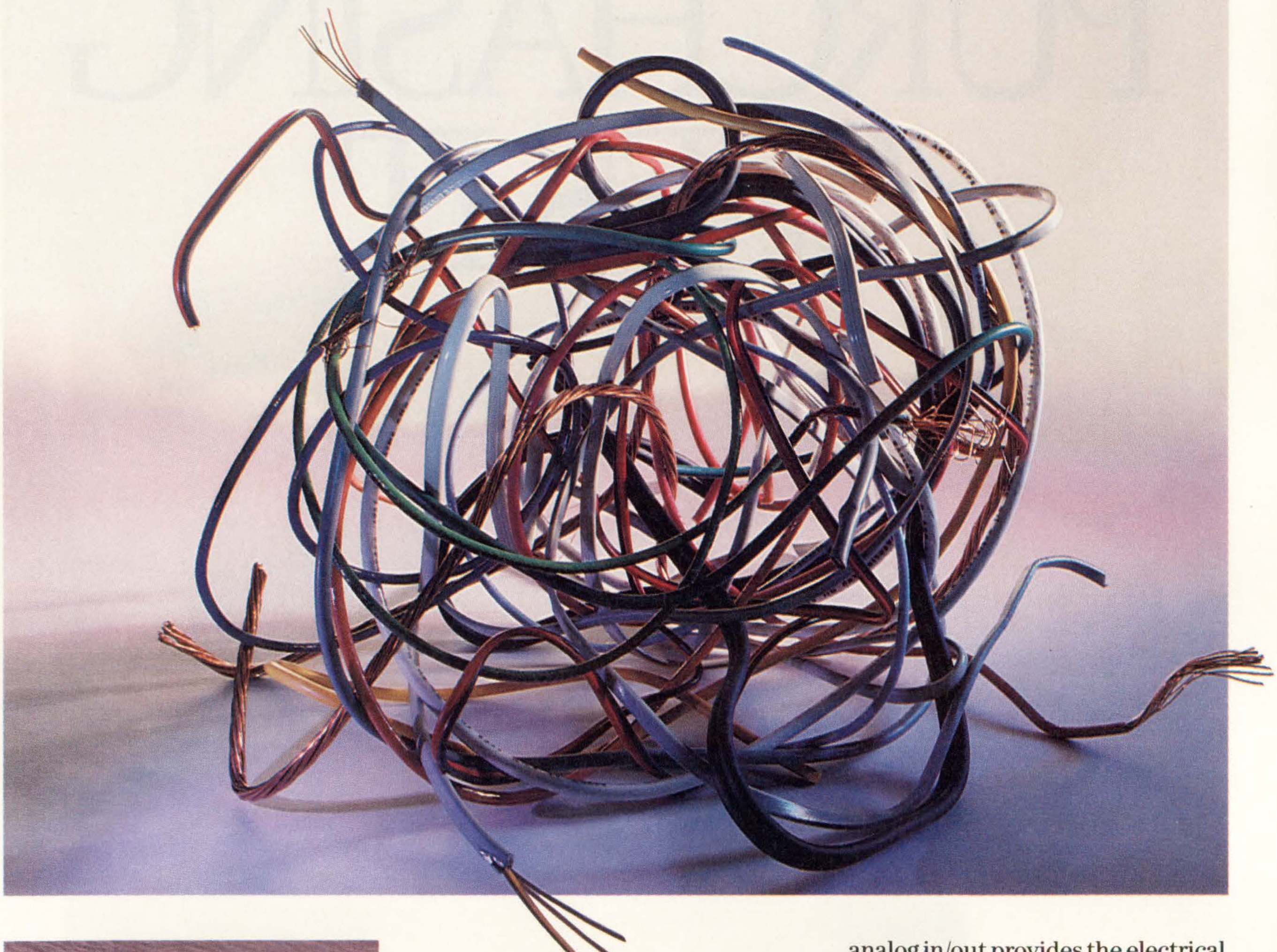
All of which can save you a lot of trouble, while lowering overall system costs and raising your accountants' morale.

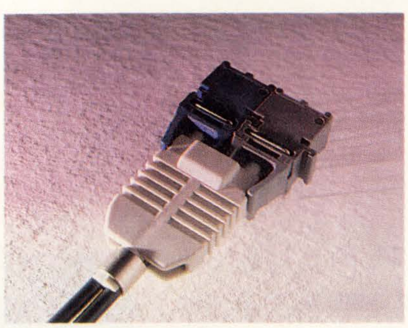
So if you're looking for 32-bit performance at a 16-bit system price, call 1-800-845-MOTO. Ask for a free 68330 product sample* and discover a high-caliber value.

MOTOROLA

CIRCLE NO. 17

HP's 50 MBd Plastic Fiber-Optic Data Links. Anything else would be twisted.





Our new data links are so fast and cost-effective, it would be crazy to stick with twisted pair.

Sure, optical fiber is immune to noise, but who can afford it? With HP's new high-speed plastic fiber links, the answer is anyone.

That's because our new links rely on plastic optical fiber cable which keeps costs way below glass fiber, while offering far greater voltage isolation and noise immunity than twisted pair wire.

A quick turn for the best.

With data rates soaring to 50 MBd, HP's plastic fiber links offer the fastest solution for designing computer, telecommunications, or industrial applications. So you can avoid bottlenecks, and design in data multiplexing.

Perfectly flexible.

You can choose interlocking horizontal or vertical mounts for greater mechanical design flexibility. The analog in/out provides the electrical design flexibility you need to meet your cost and performance goals.

The whole ball of wax.

What's more, as the largest optoelectronic supplier in the U.S., HP offers you the industry's most complete package of products and support services. To find out more about HP's 50 MBd Plastic Fiber-Optic Data Links, call **1 (800) 752-0900, ext. 2948** in the U.S.* You'd be crazy not to.

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CG080203

CIRCLE NO. 20

EDITED BY SUSAN ROSE

ECL IC integrates 200-MHz ATE pin electronics

The Bt612 monolithic IC includes the timing generation, formatting, and pin-logic error functions required in ATE equipment. The IC features a 200-MHz maximum data rate, and can therefore be used to test even the fastest static RAMs. Specifically, the IC includes two timing memories, eight 8-bit counters, and two 8-bit verniers that combine to generate 32 programmable timing events with 10-psec resolution. You can select from 16 time sets on the fly, which lets you change timing on a cycle-by-cycle basis. The format and error functions combine the timing information and pin data to directly control the pin-electronics driver or monitor the pin-electronics receiver. The IC was interfaces directly to the company's Bt698 driver/load/comparator IC, and therefore reduces the IC count in an ATE pin channel to two.

The company also designed a development system that you can use to evaluate the channel-controller IC. The system includes a pc board with dual 200-MHz channels. You interface the system to an IBM-compatible PC and use an oscilloscope to evaluate the IC's performance. The system includes software to control the development board and manuals. You can buy samples of the Bt612 now; production quantities will ship by the fouth quarter of 1992. The IC, packaged in a 132-pin PGA, costs $425 (100). Brooktree Corp, San Diego, CA, (619) 452-7580, FAX (619) 452-1249.—Maury Wright

View, print, and plot your CAD drawings

Autosight's Mini 4.0 drawing and viewing program displays, prints, and plots DWG, DXF, HPGL, HPGL/2, and PCX graphics. The program also offers 3-D viewing. The software runs on PCs with DOS 2.1 or higher, allows keyboard or mouse operations, and has a 1024×768-pixel maximum resolution in 256 colors. A single-user license costs $99; a 5-user license for network operation costs $399. The company is offering user upgrades to current customers for $39 plus shipping and handling through June 1. Autosight Inc, Melbourne, FL, (407) 242-5865, FAX (407) 255-1052.—Susan Rose

CAE system eases DSP-chip design

Many designers may face a design hurdle when they try to go from standard DSP designs to those that require a custom chip. Instead of switching from a DSP-only development system to an ASIC-design system, you can use Mentor Graphics' DSP Station. The software integrates DSP-system design operations into the company's existing tools for ASIC design, simulation, and layout. If you decide to forgo an ASIC for your application, you can create DSP assembly-language code that will run on commercial DSP chips. The $33,000 software operates from the company's Falcon Framework 8.0 on Hewlett-Packard Apollo workstations. The company expects to have the software operating on Sun SPARCstations by July. Mentor Graphics, Wilsonville, OR, (503) 685-7000, FAX (503) 685-1202.

—Jon Titus

Vendor breaks 50+-year tradition

Hewlett-Packard Co is breaking tradition by selling and servicing VXI modules that carry the names of three other firms. Since its 1939 beginning, the company has sold and serviced products only if they carried its own name. (In a few cases, other firms have manufactured these products for the company, and on occasion the company's catalogs have indicated where customers could obtain products that complement its own.) The first companies and products are communications test products from Tasco Electronic Services Inc (Anaheim, CA) and ILC Data Device Corp (Bohemia, NY); an angular-position monitoring instrument from ILC; and a time-code processor from Datum/Bancomm (San Jose, CA). Moreover, the company won't rule out the possibility of other such cooperative arrangements in the future, at least in the VXI area. Hewlett-Packard Co, Cupertino, CA, (800) 752-0900.—Dan Strassberg

Clock generator allows edge placement

The GA1000 digital clock-generator IC from Triquint Semiconductor lets you derive a variety of clock signals from a single reference clock. Each of the device's six output signals is phase-locked to the 20- to 80-MHz reference. The output clocks can have frequencies that are integer multiples (2× to 8×) or submultiples (1/2× to 1/21×) of the input frequency. The output clocks can have a 160-MHz max frequency.

The device provides more than simple frequency multiplication. You can divide each output clock period into a number of equal intervals, from 4 to 22, and place four clock edges—two rising and two falling—on the interval boundaries. This edge placement lets you, for example, create an output clock with a

Text continued on pg 20

Heard any good jokes lately?

Who says engineers don't know how to have a good time? Certainly not Oak Ridge Public Relations. The firm is so sure that humor abounds in the electronics industry that it is soliciting jokes, one-liners, and riddles for *The Book of High Tech Humor*. The book will include such categories as "Components of Humor," "Thanks for the Memories," and "Gigglabytes." If you send a joke to Oak Ridge, include your name, and they'll give you credit (unless your modesty prevents you from allowing your name to be used.)

All jokes must meet a few specifications: They must be about some aspect of high technology or a closely related subject (such as physics, mathematics, or underwater basket weaving). The staff will read dirty jokes but won't publish them. In case of multiple submissions, the first one received will get the credit. And the company reserves the right to edit any submission.

Pricing for this product is $0.00 (1). The product is still under development, but the company plans to start beta testing by the third quarter of 1992 and will ship by the fourth quarter. To enter your $0.02 worth, write Oak Ridge Public Relations Inc, 21771 Stevens Creek Blvd, Suite 203, Cupertino, CA 95014, FAX (408) 253-0936.—Susan Rose

Text continued from pg 19

pulse as narrow as 2.7 nsec corresponding to each reference-clock edge.

The IC has a propagation delay of 250 psec if you set up an output-clock output to be a copy of the reference. If output clocks are identical to each other, the typical clock-to-clock skew is ±250 psec. Each output pin provides a symmetrical 24-mA drive current at TTL I/O levels. The device is available in 16-pin DIPs and 28-pin ceramic leaded chip carriers costing $34 and $39 (1000), respectively. Triquint Semiconductor, Santa Clara, CA, (408) 982-0900, FAX (408) 982-0222, contact Sunil Sanghavi.

—Richard A Quinnell

Connector wafer simplifies host-system modifications

TRW's μdisc is a micromachined silicon chip the size of a quarter that fits into the space where 2-piece electrical connectors mate. You can directly monitor what's happening in a cable by slipping the chip into the space between the connectors. The mating process takes one minute, requires no modification of existing hardware, and has no effect on the normal operating characteristics of the mated connector.

The chip slides over the connector pins; contacts are located at appropriate feedthrough points in the wafer to feed the signals in the lines to monitoring equipment located outside the connector via a plastic optical fiber. Optical-to-electrical signal conversions are monitored at the exterior of the connector assembly to minimize losses associated with plastic fiber. Depending on your system, prices range from $10 to $300 (1000). TRW, Albuquerque, NM, (505) 880-1990, FAX (505) 880-5165.—Tom Ormond

Company acquires programming tools

Borland International has acquired two programming tools from Solution Systems (part of the Software Developer's Company): Brief is a programmer's editor and Sourcerer's Apprentice is a network version-control system that manages large software projects. Under the agreement, Borland will own, develop, and market both products. Borland International, Scotts Valley, CA, (408) 439-4825.

—Susan Rose

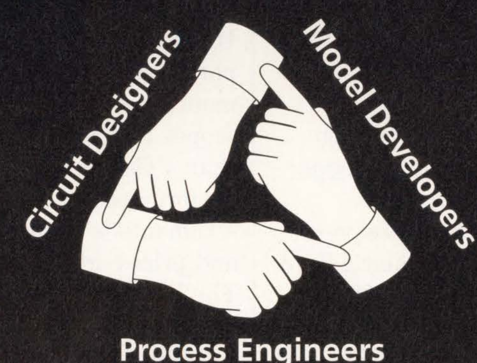
Partial-scan technology for test synthesis

At the Design Automation Conference (Anaheim, CA, June 8 to 12) this year, Synopsys Inc will demonstrate a constraint-driven partial-scan technology and automatic synthesis for JTAG boundary scan. The new IC-design product will be called Test Compiler Pscan. Partial-scan technology will enable users to trade off degrees of test coverage with area and performance constraints in designing ICs for test. Both partial scan and automatic boundary scan will be incorporated into new versions of existing products for shipping during the fourth quarter of 1992.

Partial scan turns some of the registers in an IC into "scan registers" or elements that are controllable and observable. Partial scan is a variation on full scan, in which all of the sequential elements are turned into scan registers. Partial scan is attractive for designs that are tightly constrained by performance and area requirements because fewer sequential elements are scanned than with the full scan approach. The company's existing product, called the Test Compiler, allows users to back off to about 95% fault coverage by manually deselecting registers. The company claims that Test Compiler Pscan will go as low as 40 to 60% testability.

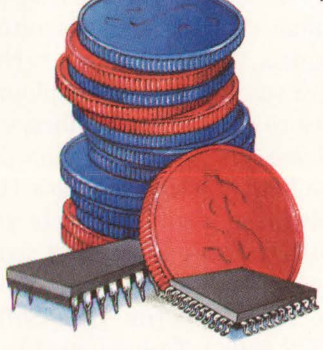
Automatic JTAG synthesis will be added to both the Test Compiler and the Test Compiler Pscan products. This option will generate test vectors in 1149.1 protocol and require no knowledge of 1149 by the engineer. USA pricing from $50,000. Synopsys Inc, Mountain View, CA, (415) 694-4255, contact Lois DuBois.—John C Napier

When the chips are down, the finger pointing starts.



Every company experiences finger pointing when a design doesn't work.

Your circuit designers claim the models are not accurate. The model developers claim the process shifted since the time they began work on the models. The process engineers claim the model developers aren't tracking the process.



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CIRCLE NO. 21

Software/hardware tools for 32-bit RISC μP

VLSI Technology Inc is offering software-development kits and evaluation and development cards for its Arm (advanced RISC machine) 32-bit processor family. The $995 software-development kits are configured for Sun OS, MS-DOS, and Macintosh operating systems. Each of the kits provides a C compiler, assembler, linker, symbolic debugger, and instruction-set emulator so that developers can write C or assembly-language programs for the Arm6 family.

The Platform Independent Evaluation (PIE) card for the Arm60 processor and the Platform Independent Development (PID) card for the Arm600 processor can both debug user-written software, thus letting users prototype the system before committing to silicon. The $595, RS-232C-compatible PIE card uses 512 kbytes of onboard static RAM (2 Mbytes optional) for download code and 128 kbytes of EPROM (upgradable to 512 kbytes) with an 8-bit monitor and self-test firmware. A remote debugger interface and source code come with the card.

The $995 PID card has both serial and parallel interfaces. The card comes with 1 Mbyte of dynamic RAM (upgradable to 16 Mbytes) and 128 kbytes of EPROM (upgradable to 512 kbytes). VLSI Technology Inc, San Fernando, CA (408) 434-7899, FAX (408)263-2511, mention ARMDEV.—Susan Rose

Alliance yields Unix software for test

Digital Equipment Corp, which has already formed strategic alliances with several vendors of test, measurement, and data-acquisition software and hardware, has announced an alliance with Tektronix Inc. The alliance has already produced its first fruits—a Unix-based, icon-driven software package called DECrti (for real-time integrator). The workstation software, priced at $3000 for a development kit and $600 for a run-time license, will collect, archive, reduce, and present test results in manufacturing and laboratory settings in the pharmaceutical, chemical, automotive, aerospace, and electronics industries.

The two companies are porting virtual-instrument drivers first developed by Tektronix for its TekTMS MS-DOS-based software to Unix. The software will support the company's entire family of modular instruments for the VXIbus, as well as IEEE-488 instruments from a large number of other firms. Compared with MS-DOS-based systems for instrument control, the firms claim Unix-based systems offer more powerful multitasking. Tektronix Inc, Beaverton, OR, (800) 426-2200. Digital Equipment Corp, Marlboro, MA, (508) 467-6679.—Dan Strassberg

Fast DSO prices drop yet again

During the last few months, EDN's Newsbreaks and Product Update sections have reported several developments in digital storage scopes that sample faster than 1 Gsample/sec. The performance of such instruments is increasing, and prices are dropping. The latest firm to join the race is Gould Inc, whose $10,950 2-channel Model 4096 can lay claim, at least for the moment, to being the lowest-priced DSO that takes more than 1 Gsample/sec in real time. The instrument takes 1.6 Gsamples/sec, but at that sampling rate, you can use only one channel. (You can use both channels simultaneously at 800 Msamples/sec/channel.) With repetitive signals, the scope's effective sampling rate increases to 5 Gsamples/sec, and you can simultaneously use both channels' full bandwidth, which exceeds 200 MHz.

The most nearly comparable scopes are Tektronix's TDS620 ($13,540 with probes), which simultaneously samples two channels in real time at 2 Gsamples/sec/channel, and Hewlett-Packard's 54510B ($11,950), which simultaneously samples two channels in real time at 1 Gsample/sec/channel. Options for the Gould 4096 include a color plotter that fits inside the scope. Gould Test and Measurement, Valley View, OH, (216) 328-7000, FAX (216) 328-7400.

—Dan Strassberg

Basic-syntax macroassembler speeds Windows

GFA-Basic gives you the speed and power of C to develop Windows applications. The $195 development program, which has a 12-month money-back guarantee, offers 700 commands and functions, includes visual programming tools, and accepts a maximum data-array size of 20 Mbytes. Graphics capabilities include Bezier curves, splines, ellipses, and arcs. The program's editor checks your code for syntax and structure errors. You can create programs that directly access and monitor all your computer's serial ports without implementing inefficient library functions. The program also comes with a dBase III/IV engine that lets you read, update, and search spreadsheet fields and records. GFA Software Technologies Inc, Salem, MA, (508) 744-0201, FAX (508) 744-8041.

—J D Mosley

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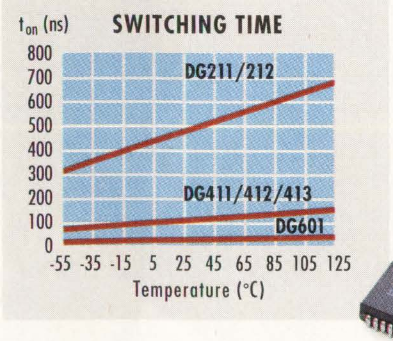

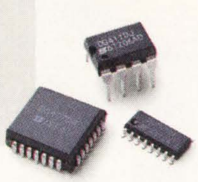

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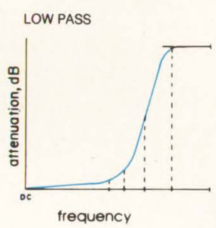
low pass, Plug-in, dc to 1200MHz



Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200
PLP-10.7	DC-11	19-24	24-200
PLP-21.4	DC-22	32-41	41-200
PLP-30	DC-32	47-61	61-200
PLP-50	DC-48	70-90	90-200
PLP-70	DC-60	90-117	117-300
PLP-90	DC-81	121-137	167-400
PLP-100	DC-98	146-189	189-400
PLP-150	DC-140	210-300	300-600
PLP-200	DC-190	290-390	390-800
PLP-250	DC-225	320-400	400-1200
PLP-300	DC-270	410-550	550-1200
PLP-450	DC-400	580-750	750-1800
PLP-550	DC-520	750-920	920-2000
PLP-600	DC-680	840-1120	1120-2000
PLP-750	DC-700	1000-1300	1300-2000
PLP-800	DC-720	1080-1400	1400-2000
PLP-850	DC-760	1100-1400	1400-2000
PLP-1000	DC-900	1340-1750	1750-2000
PLP-1200	DC-1000	1620-2100	2100-2500

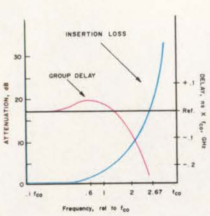
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570 MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

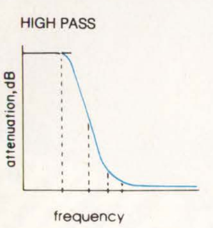
Flat Time Delay, dc to 1870 MHz



Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	2fco X̄	2.67fco X̄
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

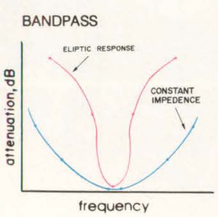
high pass, Plug-in, 27.5 to 2200 MHz



Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1
PHP-50	DC-20	20-26	41-200	1.5:1
PHP-100	DC-40	40-55	90-400	1.8:1
PHP-150	DC-70	70-95	133-600	1.8:1
PHP-175	DC-70	70-105	160-800	1.5:1
PHP-200	DC-90	90-116	185-800	1.6:1
PHP-250	DC-100	100-150	225-1200	1.3:1
PHP-300	DC-145	145-170	290-1200	1.7:1
PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70 MHz



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95, BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70 MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

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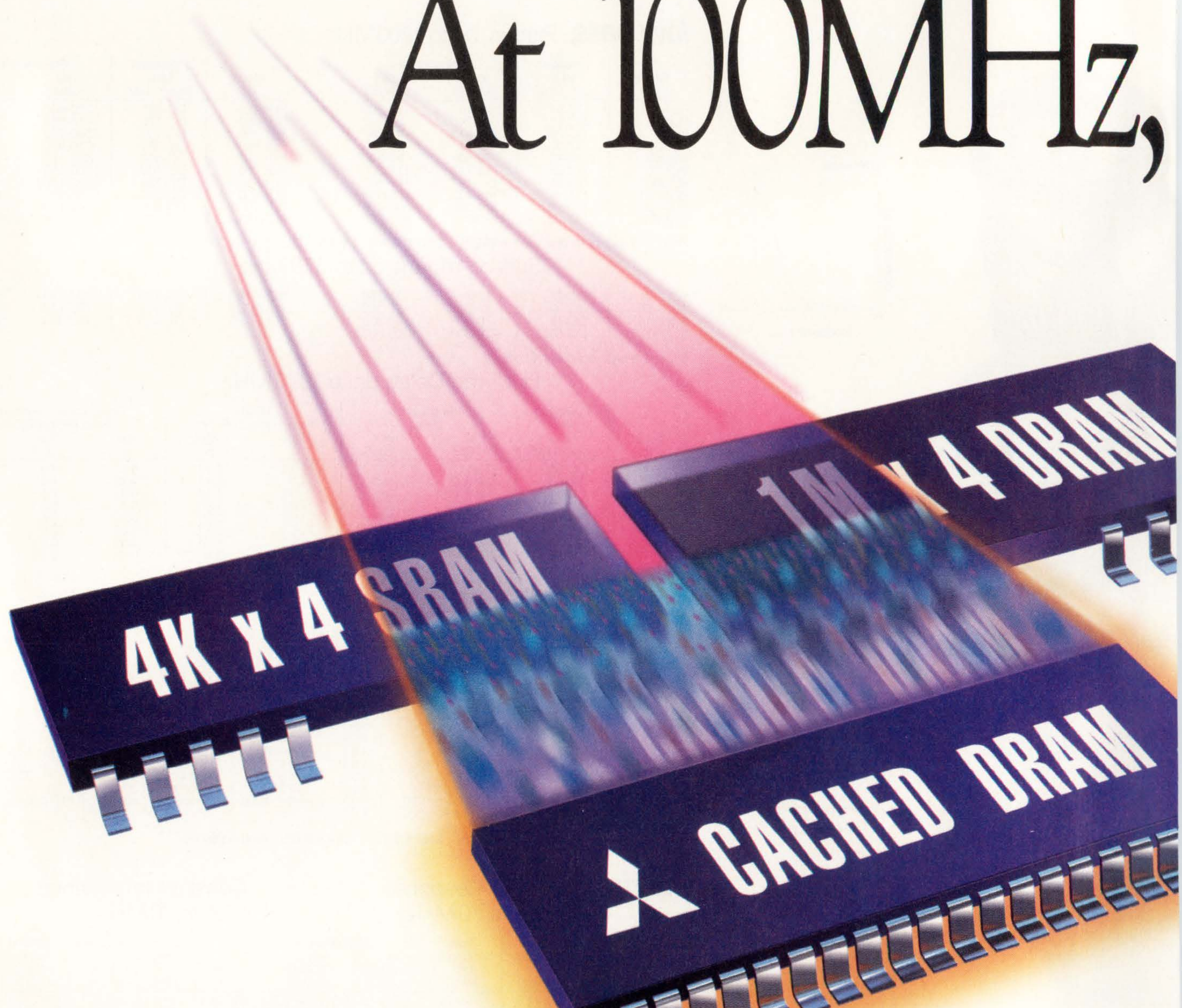

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The Cached DRAM die and package are only 7% larger than those of a standard 1M x 4 DRAM. And, since they are manufactured with the same process and on the same production line as Mitsubishi's standard 4Mb DRAMs, Cached DRAMs are highly cost-efficient to manufacture.

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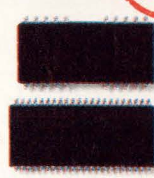
Part Number	Cache Hit Access/Cycle	Cache Miss Access/Cycle	Direct Array Access/Cycle	Package
M5M44409TP-10	10ns/10ns	70ns/280ns*	70ns/140ns	TSOP**
M5M44409TP-15	15ns/15ns	75ns/300ns*	75ns/150ns	TSOP**
M5M44409TP-20	20ns/20ns	80ns/320ns*	80ns/160ns	TSOP**

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

**TSOP Type II. Also available in reverse pin-out TSOP.

Samples Available June 1992



Not your ordinary next-generation DRAM, Mitsubishi's 4Mb synchronous Cached DRAM sets a totally new standard for cost-effective, high performance memory. For more information and technical specifications, please call **(408) 730-5900, ext. 2106 or 2226.**

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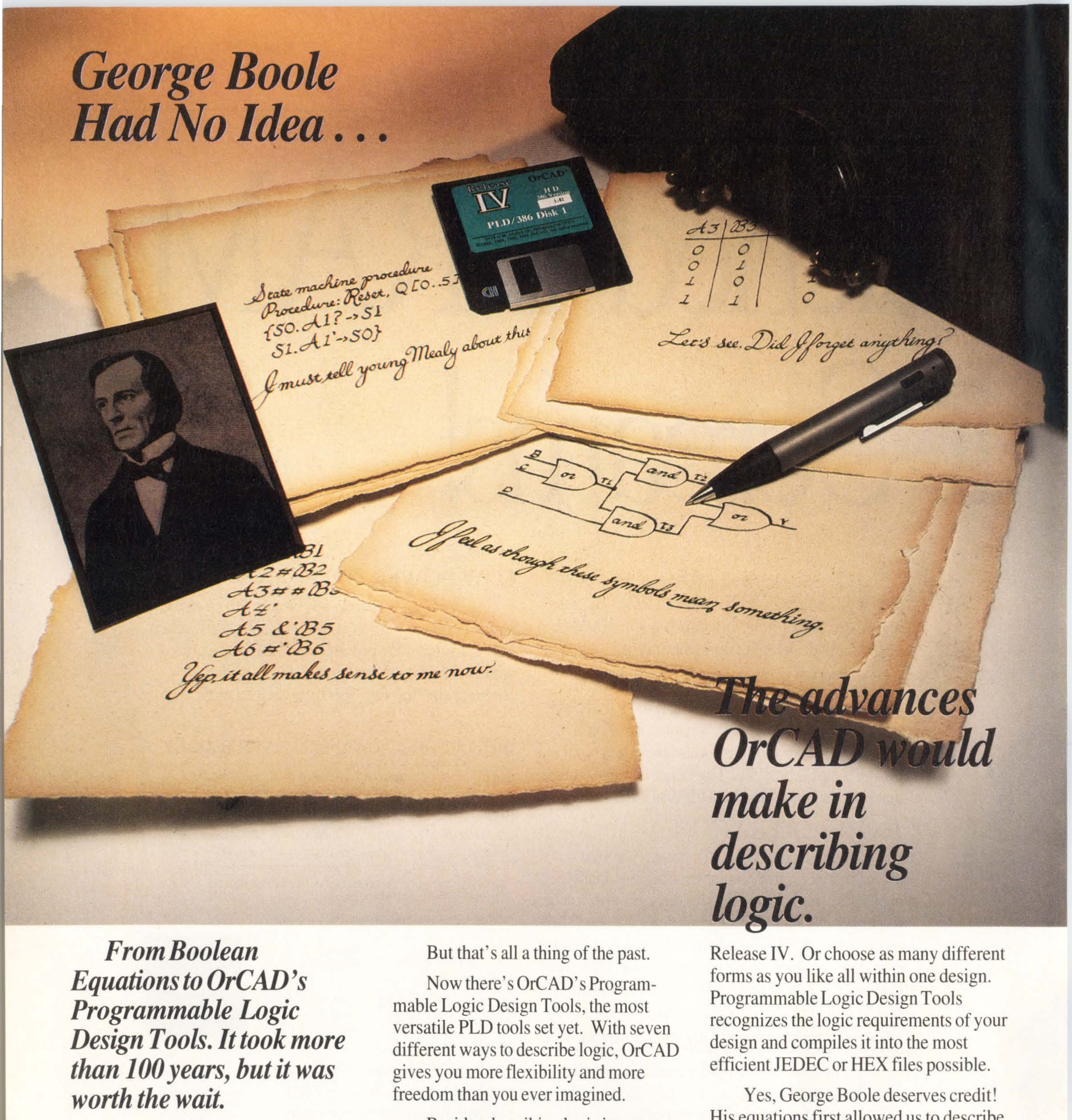

From Boolean Equations to OrCAD's Programmable Logic Design Tools. It took more than 100 years, but it was worth the wait.

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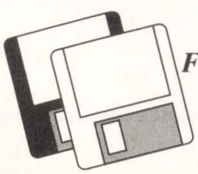

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CIRCLE NO. 25

Prediction of headlines 10 years from now

My comment about Dan Strassberg's editorial question, "Where have all the investments gone?" (EDN, February 17, 1992, pg 55) is that his question is so naive that it must only be rhetorical and intended for abstract discussion.

Why? Because a literal answer to the question is too painful to contemplate in public: we engineers, like most Americans, have sold out to Asia. We are not yet hurting enough to take remedial action.

Dan should run his editorial in 10 years when future headlines may be saying, "Engineers' Movement tosses MBAs from management," or "Engineers riot to take over top management spots," or "Unions prohibited from US industry," or "It's law now: All products must be labeled with true manufacturer ownership."

One clue to the answer to Dan's question is printed on the Thermos bottle package for sale at thousands of US stores. It says, "An American Original"—but all the profits go to Asia (and therefore all the R&D).

John Clothier, EE
Chino, CA

National Health Care is a closed-loop control system

All morality issues aside, the first utterance of the phrase, "National Health Care" should send shivers through the body of any engineer who has ever been involved in the design of a closed-loop control system, regardless of its complexity.

That is precisely what national health care is—a closed-loop control system of mind-boggling complexity. The quantities to be controlled are the price and quality of health care. The input to the proposed system is a government agency's subjective valuation of factors such as demand for health care, the available supply of health-care providers, and the fed-back value quality of health care. Additionally, the inputs are littered with sources of "noise" such as pressure from lobbyists and media-inflated hype. The controller, ultimately, is Congress, [whose members] must pass legislation to alter the price or quality of health care.

Even ignoring the fact that every major element in the system is inherently nonlinear, noncharacterizable, and nonrepeatable, and that all of the inputs are subjective by nature, such a complex control system still possesses insurmountable problems. First, the time constants in the dynamics of the system span periods from shorter than a few months to longer than a decade. The short-term "impulse" disturbances such as medical and scientific breakthroughs would cause short-term differences in market demand and controlled supply that could cause temporary shortages of available health care. Even worse, the slowly changing factors such as the emigration or immigration of health-care professionals and an increase or decrease of students in the medical field could cause a severe, long term surplus or a shortage of health-care professionals.

Demographics presents additional problems for the system. For instance, in which cities is health care sampled? Ethics presents even more problems. How good must the quality of health care be? By whose standards?

The cause for alarm, however, is not merely that national health care is a very complex closed-loop system, but that it is being proposed, designed, and implemented by people who have never heard of concepts such as closed-loop stability, regenerative feedback, or Nyquist criterion. The thought of designing a closed-loop system with a settling time of many decades, an inherently fallible observer, and a sampling controller whose transfer function took into consideration that it had to be reelected every two to four years should instill fear into any competent control-system engineer. An infinitely scarier prospect, however, is that such a system would directly affect every individual's health and well being.

Mike Harris
Electrical Engineer

Sorry, wrong number

In the article on multichip modules (EDN, January 2, 1992, pg 40), the phone number for AT&T Microelectronics should be (800) 372-2447.

NEXT IN EDN MAGAZINE AND EDN NEWS EDITION

In the next EDN News Edition (May 28), look for the latest on new products, including transceivers. The Careers section will carry an article on jobs in the EDA software field and will look at opportunities in Texas, Oklahoma, and Kansas.

The June 4 issue of EDN Magazine will feature a Special Report written by Senior Technical Editor Charles Small on converting FPGA designs into ASICs. Also look for Technology Updates on DSP μP evaluation kits, interoperability in networking, and 3V circuits. Lots of new-product information is on tap as well.

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Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
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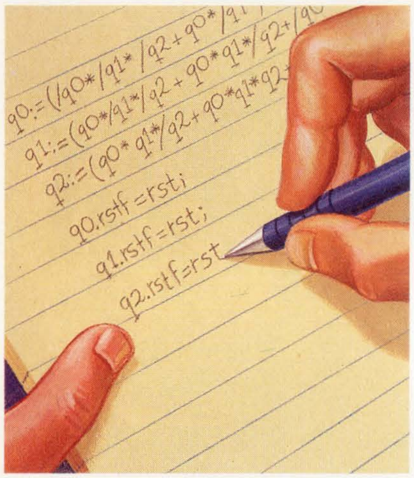

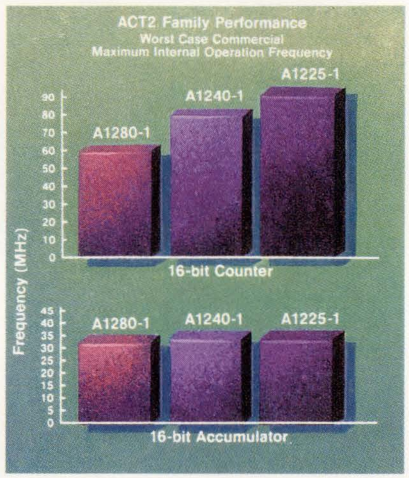

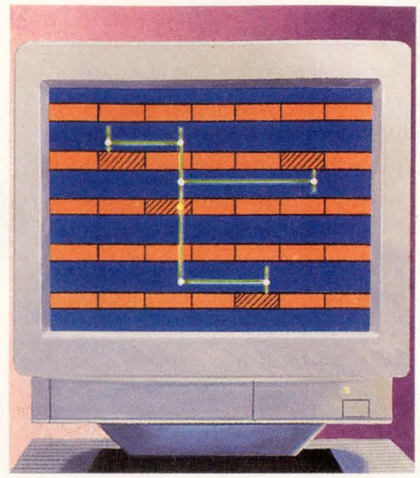

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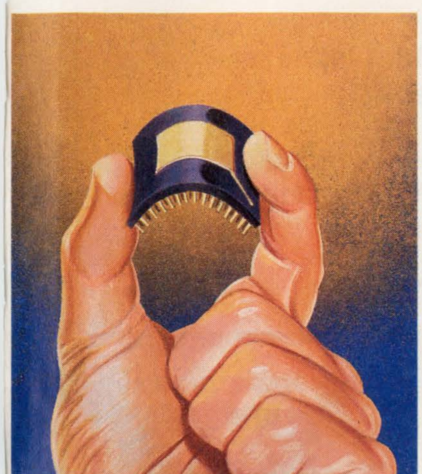

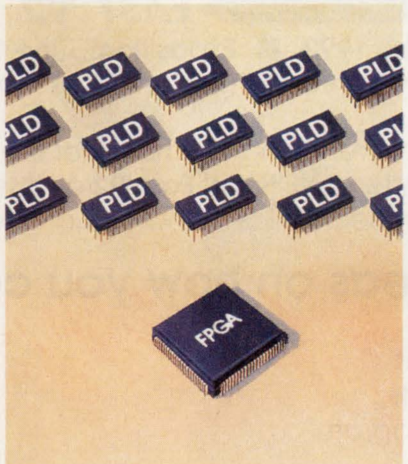

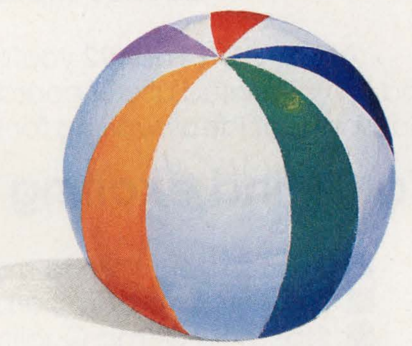

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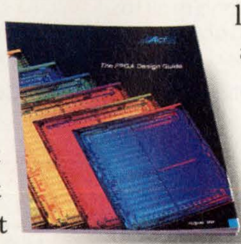

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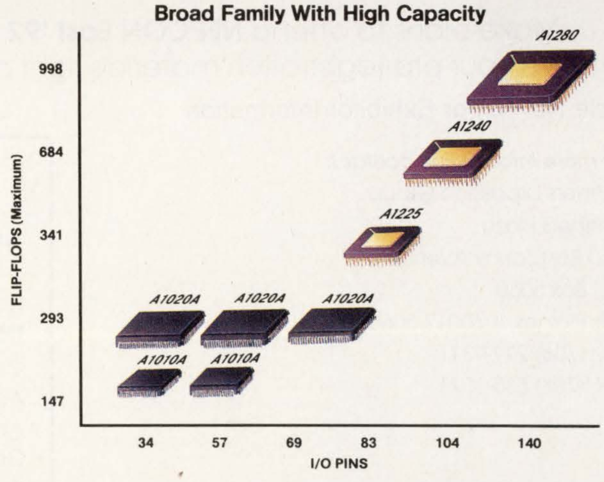

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EDITED BY JULIE ANNE SCHOFIELD

Address found for European Free Trade Association

In the February 17, 1992, issue of EDN, Brian Kerridge mentions the European Free Trade Association (EFTA) in his article, "European manufacturing contractors encourage close relationships," (pg 58). Could you give me the EFTA's address and FAX and phone numbers?
Victor Meeldijk
DRS Military Systems
Oakland, CA

The information is

European Free Trade
Association Secretariat
9-11 Rue de Varembé
CH-1211 Geneva
Switzerland
(41) (22) 749-1111
FAX (41) (22) 733-9291.

Real-time-programming book is in print

Some months ago, EDN published a series of articles based on my book, *An Implementation Guide to Real-time Programming*. Since then, many people have reported that they were having difficulty locating the book. (Murphy's Law had struck; the notice of publication was never sent to *Books in Print*). The book is very much in print. It is available from Prentice Hall (phone (800) 223-1360) as ISBN 0-13-451873-X.
David L Ripps
Industrial Programming Inc
Jericho, NY

Thanks for the information. For those who missed Mr Ripps' series on real-time programming, in 1990 it ran in the September 17; October 1, 11, and 25; and November 8 and 22 issues. The series continued into 1991 in the January 3 and 21, and February 4 and 18 issues. The book on which the series was based costs $51.

LCD bar-graph module may have to be a custom part

For many months I have been attempting to find an LCD bar-graph module for a range of instruments my company is hoping to introduce soon. The module is to accept an analog input and display a corresponding amount on the bar graph either as a moving segment or as a bar. I have located drivers from Teledyne and Philips but cannot locate suitable displays. I have also located bar-graph displays but not suitable drivers. There always seems to be a disparity in the number of segments or the arrangements of the backplanes.

I have contacted semiconductor manufacturers and some LCD manufacturers without success. The best I have achieved is the offer of a custom display. At the current stage of our project, the risk is too great for this commitment.

Can you suggest a ready-made module or a driver-display pair? I am looking for between 20 and 100 segments in either a straight-line or circular format. The dimensions should be in the order of 50 to 100 mm long for a line or 50 mm in diameter for a circle.
S Morris-Jones
Actferry Ltd
Harrow, Middlesex, UK

The LCD manufacturers we contacted indicated that what you are looking for would most likely be a custom part. However, if any reader knows of any such devices that are available in small quantities for this project, please share the information with Ask EDN.

View Windows 3.0 in a rainbow of colors

Does anyone know how—or if—it's possible to change the color of the topic text (the text you click on for more information) in Microsoft's Windows 3.0 software? I use an off-white background color because I find the white hard on my eyes, but the green the help program uses for the topics provides too low a contrast for me to read easily. I cannot determine if the color information is stored in the help.exe file or in the individual help files.
Gary Treible
Fincor
York, PA

Microsoft's applications engineers say there's no documented way to change the color of the text. However, Jack DeLand, a consultant with Adam Charles Consulting Inc, does know how to change the Help jump-text color in Windows 3.0: First, open the Color dialog box from the Control Panel. Find the color you want and write down the red, green, and blue values. Edit the [Windows Help] section of the win.ini file thus:

JumpColor=<RGB value>
PopUpColor=<RGB value>

For example,

JumpColor=0 0 130
PopUpColor=130 0 0

yields deep blue for jump topics and dark red for glossary terms. Because you're changing the win.ini file, the change affects all the help files.

Consultant has hot tip for parts source

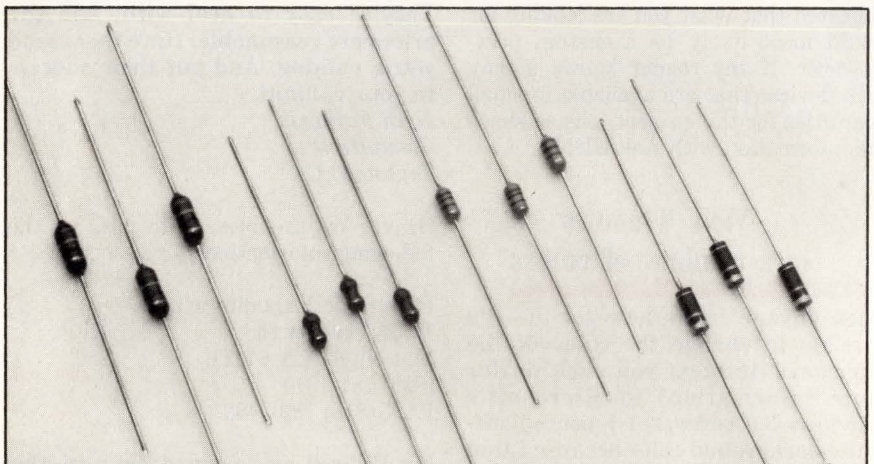
Here's the place you probably suspected was lurking somewhere all along—the treasure trove of old electronic parts: Electronic Expediters Inc. I highly recommend them. They've gotten me out of several jams. They're easy to deal with, and the prices are reasonable. Have them send you a catalog. And put their address in your column.
John Fallwell
Consultant
Topanga, CA

Bravo! We are pleased to pass on the following information:

Electronic Expediters Inc
14828 Calvert St
Van Nuys, CA 91411
(818) 781-1910
FAX (818) 782-2488.

Mr Fallwell also pointed out that this company has a supply of the Signetics S8233 and the Texas Instruments SBP9989. The March 2, 1992, Ask EDN included letters from readers Clancy Sloan and Jeroen van der Wateren, who were searching for these parts.

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.



Annual Symposium on Frequency Control, Hershey, PA. Michael Mirarchi, Synergistic Management Inc, 3100 Route 138, Wall Township, NJ 07719. Phone (908) 280-2024. May 27 to 29.

1992 Mathematica Conference, Boston, MA. Wolfram Research Inc, 100 Trade Center Dr, Champaign, IL 61820. Phone (217) 398-0700. FAX (217) 398-0747. May 27 to 31.

Silicon Mountain Symposium, Colorado Springs, CO. Colorado Marcom Network, Box 49462, Colorado Springs, CO 80919. Phone (719) 540-1842. May 31 to June 2.

Windows Solutions: International Conference and Exposition for Windows Application Builders and Systems Integrators, New York, NY. Windows Solutions, Boston University Corporate Education Center, 72 Tyng Rd, Tyngsboro, MA 01879. Phone (508) 649-4200. FAX (508) 649-2162. June 1 to 5.

International Microwave Symposium, Albuquerque, NM. IEEE, Box 1331, Piscataway, NJ 08855. Phone Tammy Ferguson, (505) 845-8806. June 1 to 5.

EEsof Users' Group Meeting, Albuquerque, NM. Linda Harmon, 5601 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 879-6200. FAX (818) 879-6467. June 2.

International VLSI Multilevel Interconnection Conference, Santa Clara, CA. Dr Thomas Wade, College of Engineering, University of South Florida, 4202 Fowler Ave, Tampa, FL 33620. Phone (813) 974-3786. FAX (813) 974-5094. June 2 to 3.

Test & Design Expo, Somerset, NJ. Miller Freeman Expositions, 1050 Commonwealth Ave, Boston,

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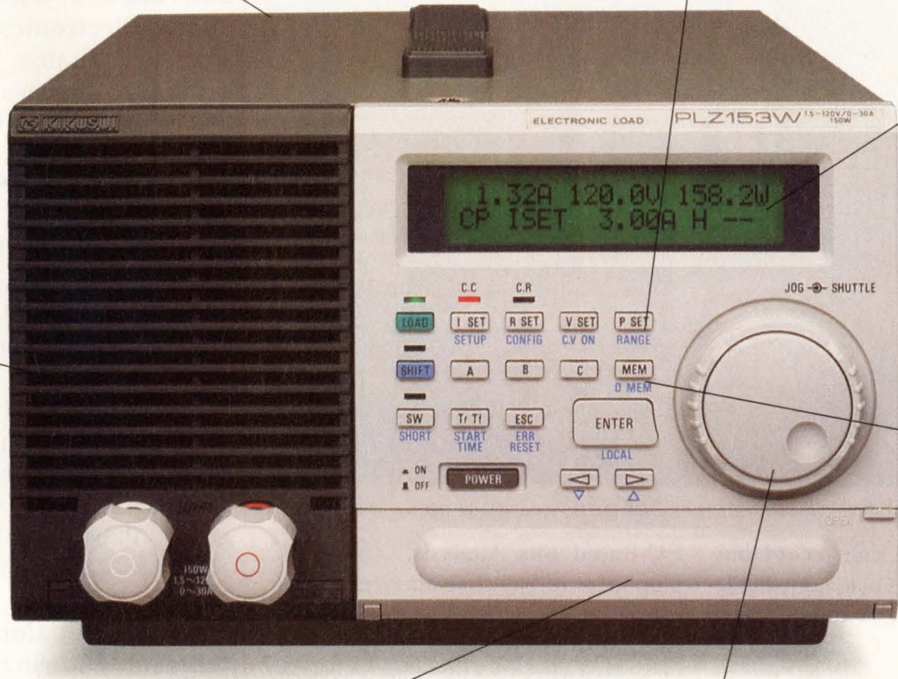

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MA 02215. Phone (800) 223-7126; (617) 232-3976. FAX (617) 730-5708. June 2 to 4.

International Conference on Consumer Electronics, Rosemont, IL. Diane Williams, 67 Raspberry Patch Dr, Rochester, NY 14612. Phone (716) 392-3862. June 3 to 5.

ACM/IEEE-CS Design Automation Conference, Anaheim, CA. Dan Schweikert, Cadence Design Systems, 555 River Oaks Pkwy, Bldg 4, San Jose, CA 95132. Phone (408) 944-7297. June 8 to 12.

Usenix Association Technical Conference, San Antonio, TX. Usenix Conference Office, 22672 Lambert St, Suite 613, El Toro, CA 92630. Phone (714) 588-8649. FAX (714) 588-9706. June 8 to 12.

International Conference on Intelligent Tutoring Systems, Montreal, PQ, Canada. Claude Frasson, University of Montreal, 2900 boul Edouard-Montpetit, Dept IRO, Montreal, PQ H3T 1J4, Canada. Phone (514) 343-7019. June 10 to 12.

Software Development 92 Exhibition and Conference, London, England. Blenheim House, 630 Chiswick High Rd, London W4 5BG, UK. Phone (81) 742-2828. FAX (81) 747-3856. June 16 to 18.

European Fibre Optics and LAN Exposition, Paris, France. IGI Europe Inc, Clarastrasse 57, Box 6, CH-4005 Basel, Switzerland. Phone (61) 691-8888. FAX (61) 691-8189. June 22 to 26.

Statistical Process Control in Semiconductor Manufacturing (short course), University of California, Berkeley, CA. University of California Extension, Dept B, 2223 Fulton St, Berkeley, CA 94720. Phone (510) 642-4151. FAX (510) 643-8683. June 29 to July 1.

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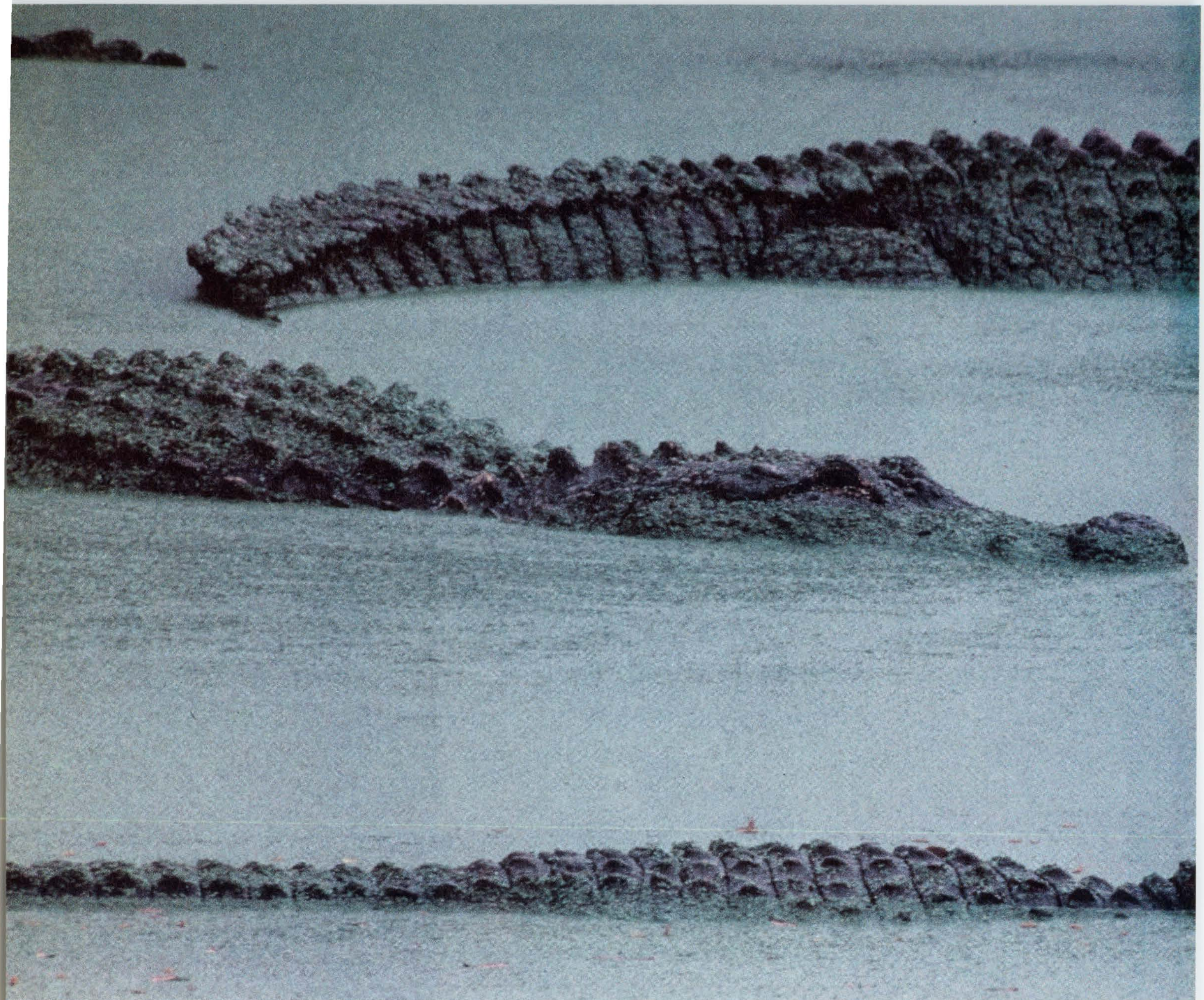

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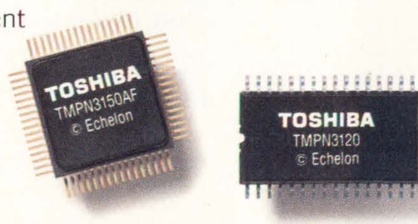

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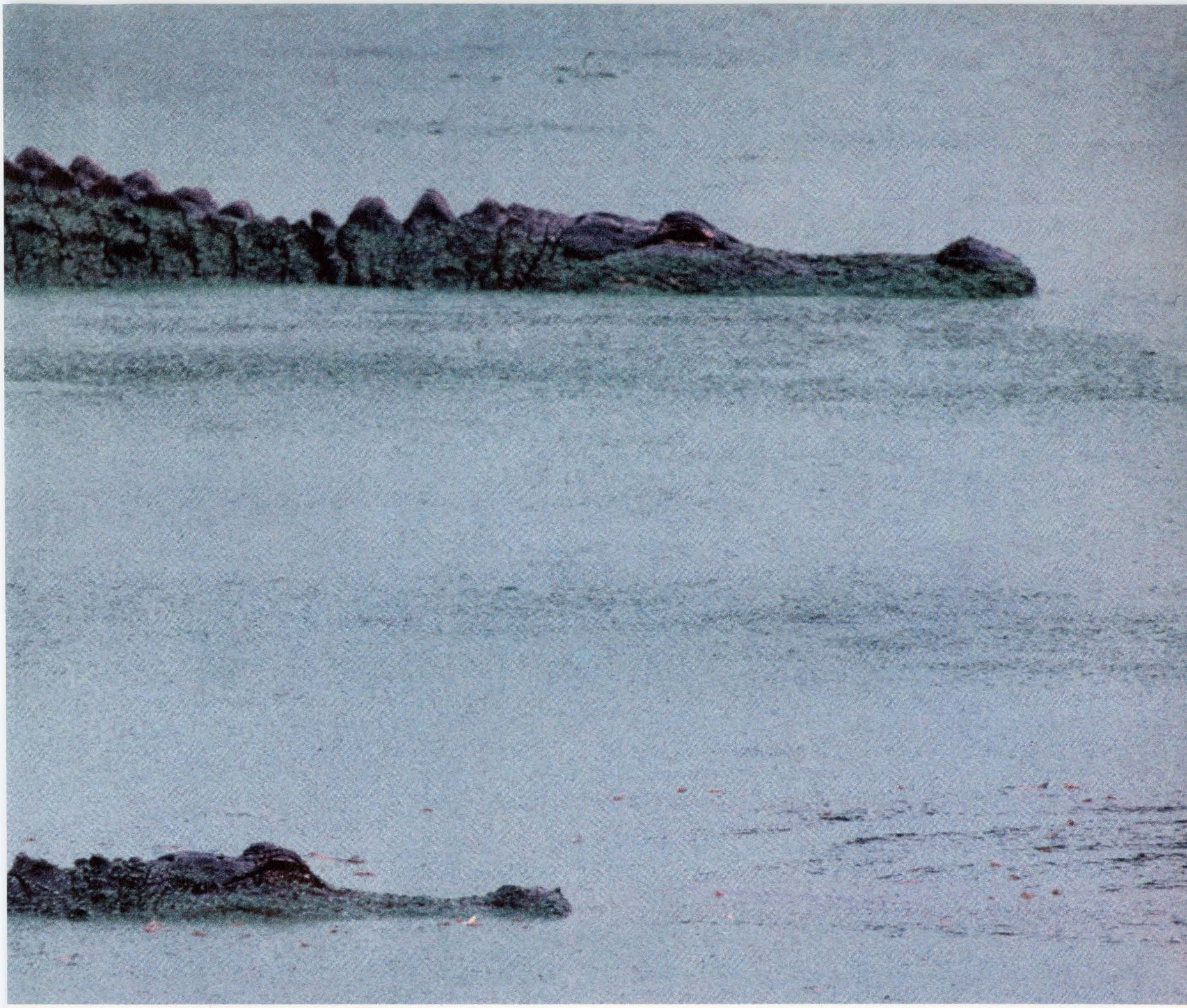


CIRCLE NO. 37

In praise of freedom

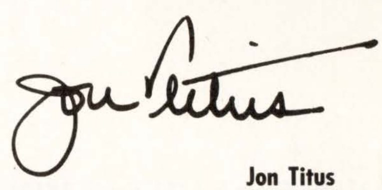
When my father died earlier this year, I wondered what it was that helped create such a strong bond between us. Our bond went deeper than the love between a father and son. One of the things that I think contributed to that, and that I most thank my Dad for, is the freedom he gave me to try new things, to experiment, and to fail.

Once when I was eight or nine, some friends and I disassembled a large dry cell in the basement just to see what was inside. If we knew what was inside, maybe we could make our own batteries. The black powdery insides of the battery went all over the floor, permanently staining the concrete. When he discovered what we had done, Dad gave us a lecture about placing newspapers under experiments and then he showed us how to make a battery out of a lemon and a stack of coins.

At about the same time, Dad helped out when we had trouble setting up a telegraph from one bedroom to another. Dad let us run strands of thin wire salvaged from an old transformer to make the connection. When the telegraph didn't work and we didn't know why, Dad told us about the high resistance in the thin wire and suggested using heavier wire. He never said a word about how we had "neatly" stapled and taped the wires to the hall molding. Instead he suggested running the new wires out one window and in another to avoid tripping people in the hall. We got the point. The newly wired telegraph worked the first time.

Some years later, my brother Chris decided to build his own submarine with which he could explore the harbor near where we lived. Chris was about 12. Dad knew the submarine would sink, but he gave Chris the freedom to build it and to take over half the garage as he did. Dad drew the line at launching the sub from the town dock and instead took us to a shallow beach where the submarine dove into two feet of water and never surfaced on its own power—or ours. Even though the sub had failed, Chris had the opportunity to try it. He went on to take up scuba diving and enjoyed it for many years.

As I look at my own children, I hope that I've given them the freedom they need to develop their own personalities and interests. Although no parent likes to see a child fail, part of freedom is watching offspring try, fail, try something new, and eventually, we hope, succeed. Encouragement and praise play roles, too. Along with the enjoyment of freedom comes the responsibility to pass it on to others without condition. Then it's up to them to decide what to do with it.



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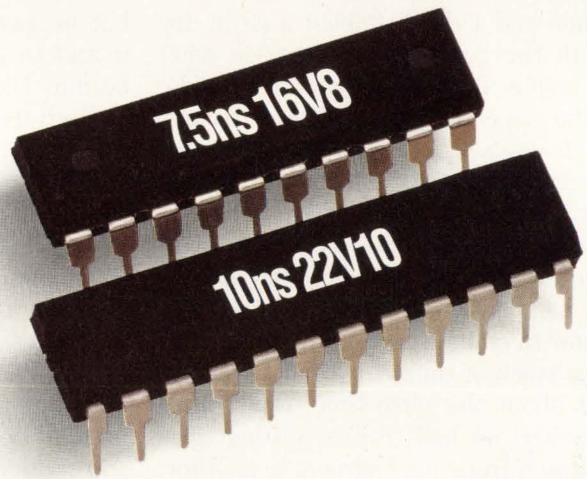

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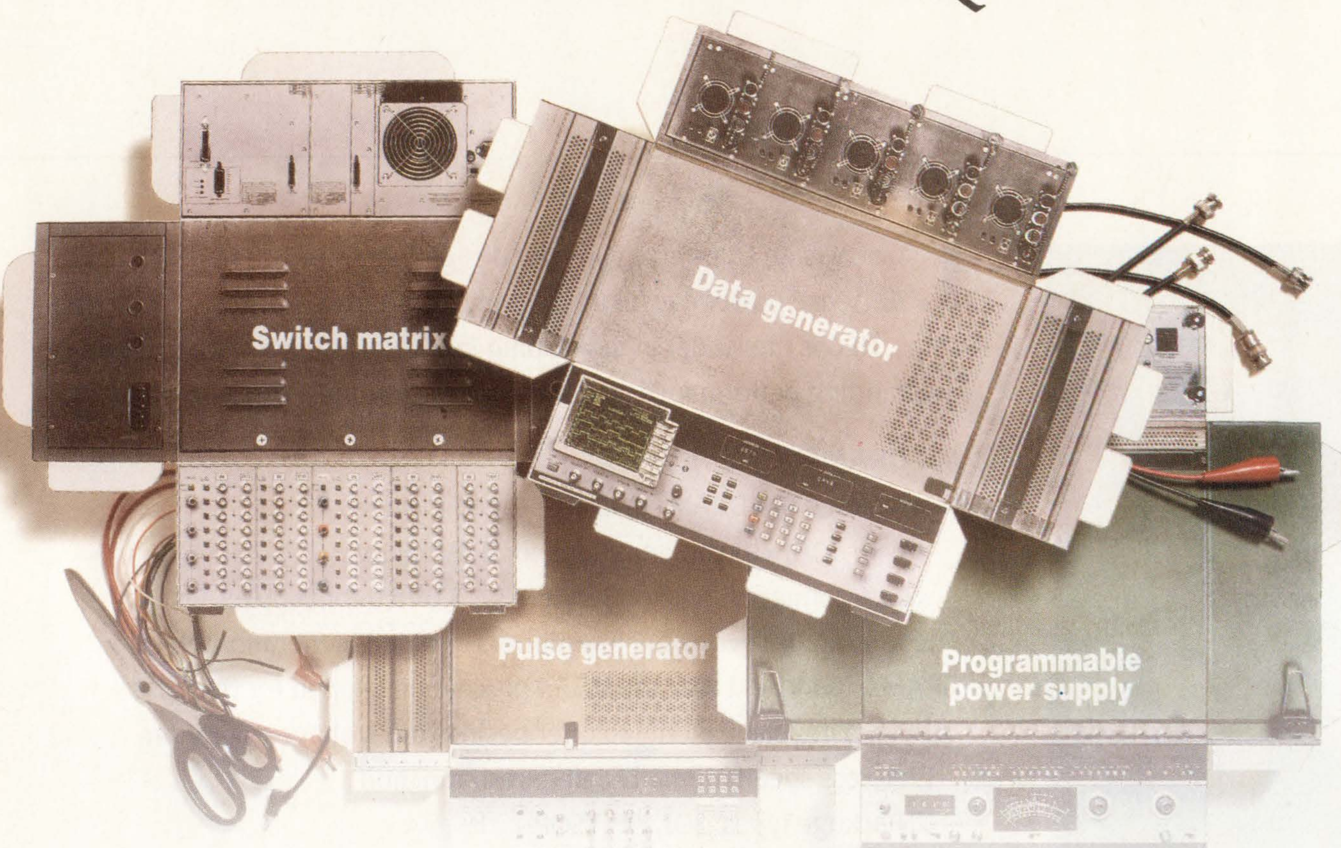

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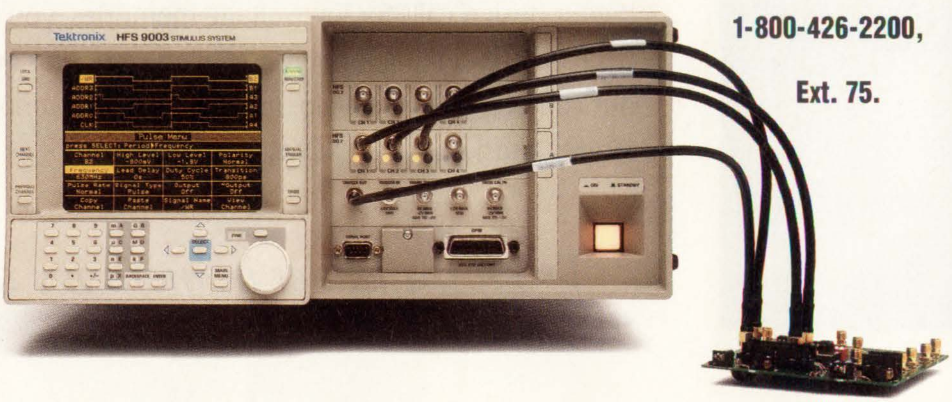

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CIRCLE NO. 40

85W-188515

PC-BASED DESIGN SOFTWARE

Schematic capture and pc-board layout on $1600

DOUG CONNER, Technical Editor

You can get a surprising amount of utility from low-cost schematic-entry and pc-board-layout software.

Dozens of companies sell schematic-entry and pc-board-layout software for personal computers. I chose Accel's Tango-Schematic and Tango-PCB Plus products to design the pc board I used in my FPGA hands-on series, which ran in the April 9 and April 23 issues of EDN. However, many other products fit the same general price and performance range (**Ref 1**). *(Editor's note: EDN will review other schematic-entry and pc-board-layout software packages in the future.)*

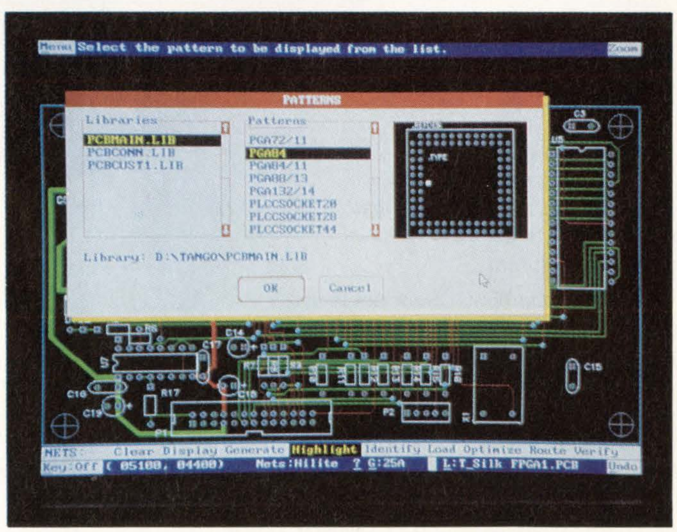
You can create simple to moderately complex board designs with low-cost software such as Accel's Tango products. You can also design more complex pc boards using such software. But as you move beyond 4-layer designs you may find the capabilities of higher-priced pc-board-layout software—such as creating padstacks, blind and buried vias, and copper pours; automatic placement; and autorouting—to be worth the extra money.

Using software always starts with installing it on your computer. Tango products work with as much as 32 Mbytes of expanded memory—much more than the standard 640 kbytes available in DOS. Because I have extended memory on my computer, I used MS-DOS 5.0's ability to emulate expanded memory with extended memory.

I've used schematic-entry software on both workstations and personal computers and seldom notice significant differences between the two. The critical hardware factors are the size and resolution of the display and the speed of the computer. Tango-Schematic works with displays that have resolutions as great as 1024×768 pixels; I used a VGA display, which has a 640×480-pixel resolution. I ran the software on a 33-MHz 486-based computer, which provides nearly instantaneous screen redraws and compares favorably with workstation-level performance.

Significant software factors are the time you need to learn the software and the time you'll take to design a circuit once you've become familiar with the software. In theory, you should only have to learn software once. But if you're an occasional user and the software is difficult to use, you may end up relearning it every time you use the system.

A package's menu structure can aid or hamper learning and using software.



When looking for components or patterns for schematic-entry or pc-board layout, a graphics- and text-based browse feature helps you zero in on the correct part quickly.

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PC-BASED DESIGN SOFTWARE

I give Tango-Schematic's flexible menu structure high marks. Menus are two levels deep, although some operations call up dialog boxes when you need to make more decisions. The shallow menu structure helps you learn the menus and how to navigate through them quickly.

If you prefer to select functions using a mouse, you can do so from the standard menus; the quick menus at the bottom of the screen; and, for special functions like zoom, the hot spots in the corners of the screen. I find using a mouse satisfactory for learning software and for menus I use infrequently.

For functions I perform often, such as moving a component, I prefer to select using the key letters or function keys on the keyboard. On Tango-Schematic, the key letters are underlined on the menu for easy learning. Once you learn the software, you'll find you can work fastest by using one hand on the keyboard to make function selections and one hand on the mouse to select and place objects on the schematic.

You can quickly create custom macros with a record function and assign them to a function key or the middle key of the mouse. The software also has an auto-pan feature, which lets you move the cursor off the edge of the screen to pan to the new area.

I went through the supplied tutorial to become familiar with the software and then went to work on my schematic.

Probably the most time-consuming part of schematic entry—outside of actually dreaming up the circuit—is creating components that aren't in the software's library. Tango-Schematic has a library of about 11,000 components, which includes 7400-series logic chips, microprocessors, memory chips, and linear and discrete parts.

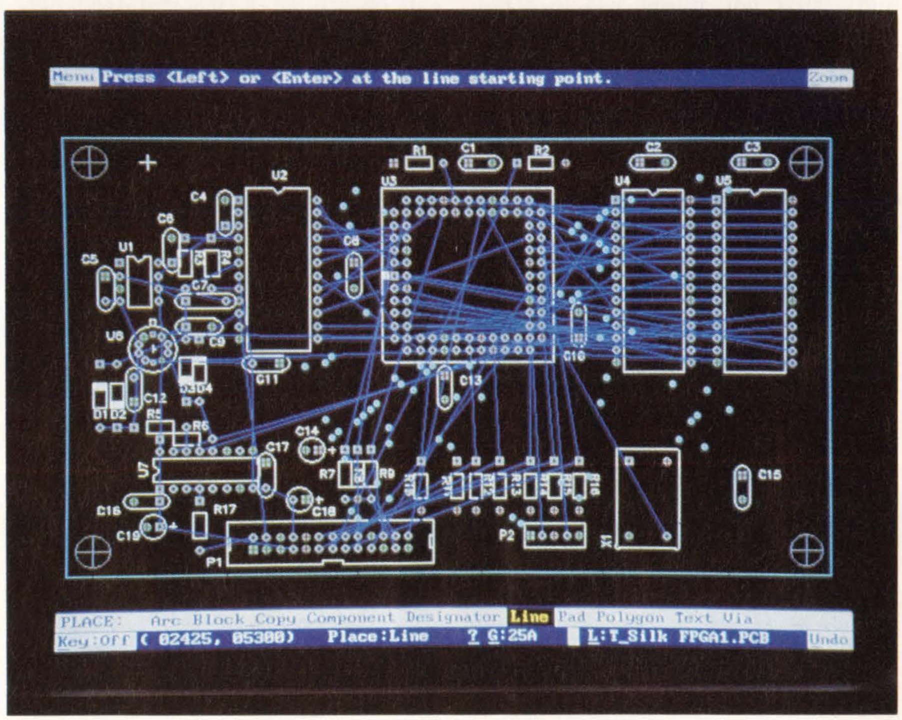
The library includes both ANSI and IEEE representations of parts. Where appropriate in the digital libraries, you'll also find Demorgan equivalents. You can browse through libraries by looking at the schematic symbol while searching through a list. You can also use wild-card searches to help you find components. When you go to place parts, you can rotate and flip symbols to get the best representation for your schematic.

The library classifies components in two categories: homogeneous and heterogeneous. An example of a homogeneous component is a 7400 logic chip in which the 2-input NAND gates are schematically identical except for the pin numbers. An example of a heterogeneous component is a relay whose coil and contacts are schematically different elements but electrically linked. Heterogeneous parts let you show the symbols and wiring to—in the case of the relay—both the coil and the contacts on the schematic, yet still keep them logically linked in the same part.

In the real world, you almost always have to create some components for your schematic. My design was no exception. The 84-pin FPGA I created and several linear and data-conversion parts weren't in the library. The NEC RAM I used wasn't in the library either, but a similar version from Toshiba was, so creating that part was a simple renaming. Even on my relatively small circuit I had ample opportunity to use the software's schematic library editor.

When you can't find the component you need in one of the component libraries, you can jump directly to the library editor without leaving your schematic. There, you draw the component and add it to the library. The software's tutorial takes you through the steps. Creating components, including those with multiple parts such as a dual comparator, is easy.

Reworking a schematic symbol is also easy. In some cases I find that after I've created a symbol and placed it in the schematic, it needs some changes. Perhaps I want to



The rats nest helps you arrive at a satisfactory component placement before you start to route the board.

move some of the pins around or change a pin name. Editing the component, placing it in the library, and updating the schematic takes only a minute or two.

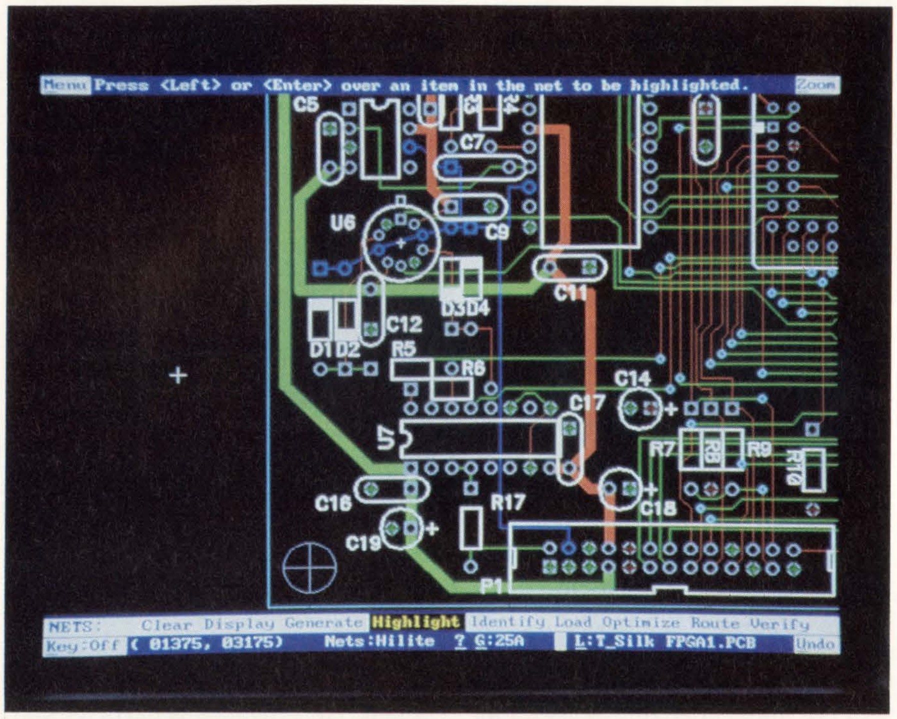
Hierarchical design

Tango-Schematic lets you produce a hierarchy of schematics using top-down or bottom-up design. Hierarchical designs make a complex design easier to understand and can be a timesaver if your circuit has many repetitive function blocks. You can draw the schematic for the block once and then let the software keep track of multiple copies or views. If you have to make changes to the function block, you have to do it only once. The software creates all the schematics for the repeated blocks.

The software also lets you select a block of logic from the schematic and perform copies, moves, and saves. Saving blocks is an easy way to move a portion of a design from one sheet to another. Block saves also let you save portions of a schematic that you might use in other designs.

Postprocessing operations

After you've finished creating the schematic, you can run postprocessing operations. A cleanup step removes any overlapping lines you might have created. An archive-library command creates a library of the parts you used in the design. Having such a record is important if later revisions to the main library affect the components you used in the design.



The highlighted selection shown in blue lets you check the connections of individual nets. The software can also check the entire board for differences from the netlist.

Creating a netlist—a file that describes how all your components connect—is the most critical postprocessing function. The software can create an EDIF-standard netlist, a Tango format for use with the Tango-PCB Plus pc-board-design software, and several formats compatible with other software packages. Another postprocessing operation, back annotation, updates the component identifiers on the schematic after you've laid out and routed the board.

One postprocessing function Tango-Schematic doesn't do that I consider important for documentation control is adding a date and time attribute to the drawing title block. This attribute would automatically stamp the time and date on a schematic when you saved it. Having this information on a schematic would make it easy to determine which drawing is the most recent when you have several hard copies on your desk.

PC-board layout

To start laying out a pc-board, you need to input a netlist that identifies the components and how they are electrically connected. If you've created the schematic with software that's compatible with the layout software, this step is easy. In fact, if you use schematic-capture and pc-board-layout software from the same company, you'll find that many of the commands are identical and that you have to learn only one menu structure.

If a component is available in multiple package types, such as through hole and surface mount, pick the appropriate pattern from the library or create one yourself. Unlike the libraries of schematic-

Table 1—Accel Technologies pc-board design software

	Product	Description	Price
Accel Technologies 6825 Flanders Dr San Diego, CA 92121 (619) 551-1000 FAX (619) 554-1019 Circle No. 710	Tango—Schematic	Schematic-entry tool	$595
	Tango—PCB Plus	PC-board-layout tool	$995
	Tango—Route	Autorouter	$595
	Tango—Route Plus	Autorouter	$995
	Tango—Route Pro	Autorouter	$5500

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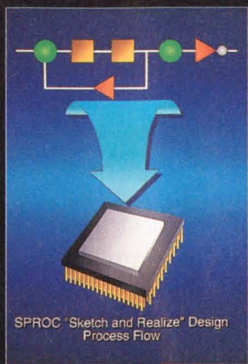

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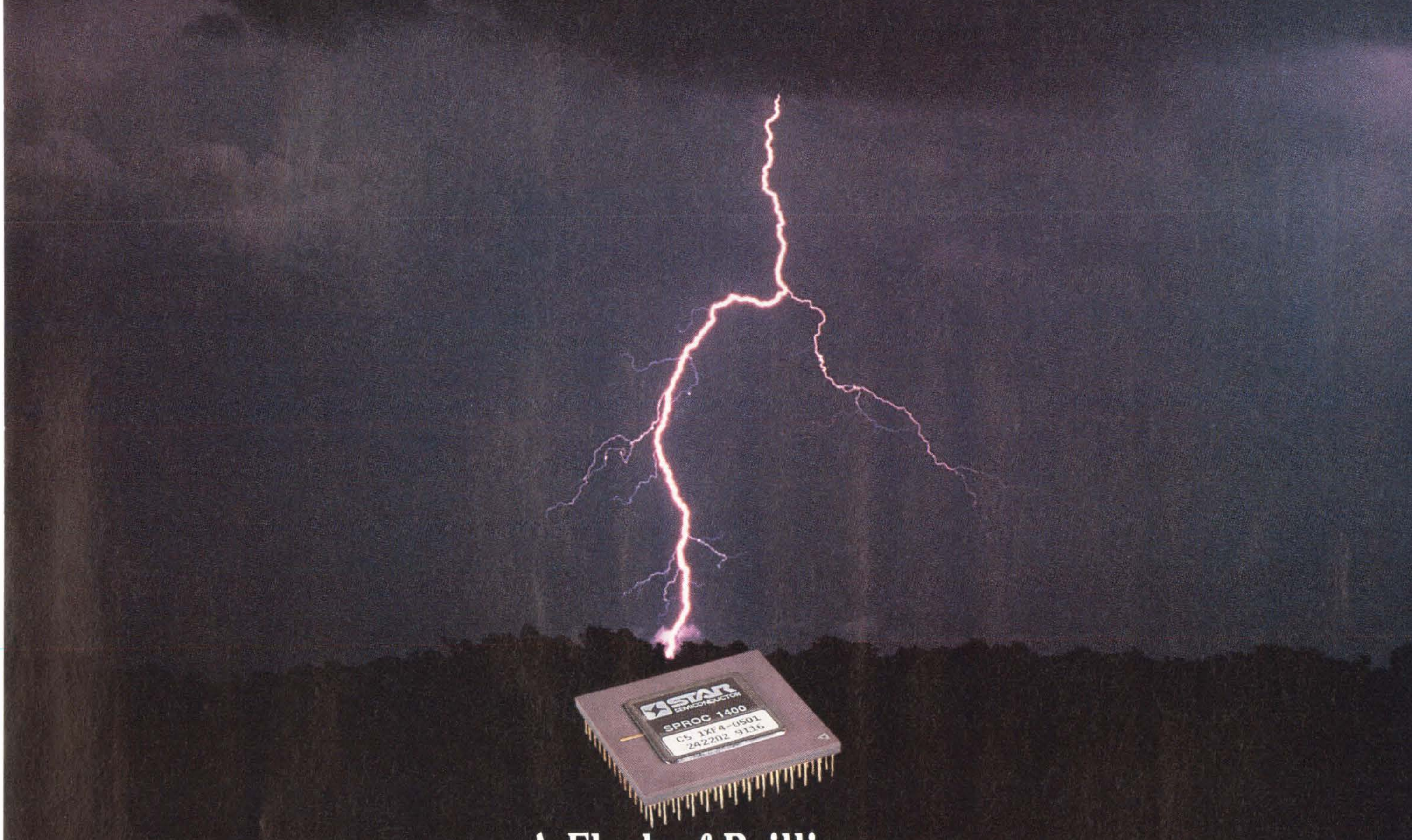


A Flash of Brilliance.

PC-BASED DESIGN SOFTWARE

capture software, a pattern library should cover most of your needs. Although I had to create most of the schematic symbols for the ICs in my design, I only had to create one pattern—a 10-pin T0-5 package. Creating new patterns using Tango-PCB Plus isn't difficult, and you can modify existing patterns.

To lay out a pc-board design with Tango-PCB Plus, you first select the signals for the power and ground planes. The software can make as many as 23 layers available. Two layers are for power and ground, two for top and bottom circuit layers, and eight for internal circuit layers. The other layers are for top and bottom silk screens, top and bottom solder masks, a board-outline layer, top and bottom assembly drawings, and several other manufacturing and assembly drawings.

Once you've created a board-outline drawing and have the netlist information and patterns for the components, you're ready to place the components. The approaches for laying out components fall into three categories: manual, interactive, and automatic. These categories can be confusing because different vendors use the terms differently. If you read that a software package has automatic layout, be sure you understand what the company means by "automatic."

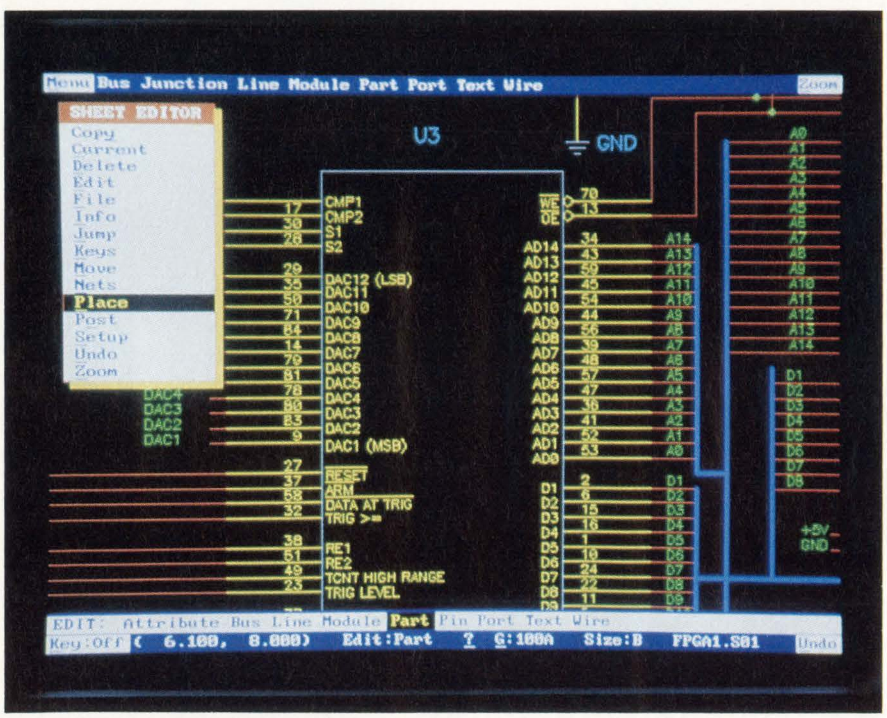
Accel defines the manual-placement feature of Tango-PCB Plus as assigning a component a pattern and placing the pattern on the drawing. You can do this type of placement with or without a netlist. The company defines interactive placement as automatically bringing up the parts one at a time and having you place them on the layout. During automatic placement, the software automatically places all the components above or to the side of the board outline.

Parts placement is one of the most difficult steps in pc-board design. Even if the software can perform a fully automatic placement, you shouldn't assume the software has done an optimal job. You need to check the layout to see if you can improve it. Several tools are available to help you create a good placement. A rats nest, which shows the point-to-point connections of all nets, is one of the most useful.

Tango-PCB Plus provides a dynamic rats-nest display. When you select and move a part, you can see the rubber-banded connections move with the part. This action helps you separate the clutter of nets from the net you have selected. Using a different color for nets connected to selected component also helps you make sense of the clutter.

The usual goal in placing parts is reducing the total track lengths on the layout. You can get a qualitative idea of how you are doing by viewing the rats nest. For a quantitative measure, you can get a sum of the total connection lengths. This number is available in both the Manhattan connection length (x, y distance) and the direct connection length. If you're trying several layouts, you can see which is best by using this tool. Of course, you may have other constraints such as minimizing the length of certain critical nets and may prefer a longer total connection length if you can keep the critical connections short.

Another placement aid is having the software reconnect the nets in an optimal order. If more than two component pins are connected by a net, the length of the connections will depend on the order in which the pins are connected. Tango-PCB Plus has a nets-optimize command that reorders the nets to obtain the shortest connection lengths possible for the current parts placement.



Tango-Schematic and PCB Plus let you bring up the main menu by hitting M or the spacebar or by using a pointing device. You can select choices from the menu by typing the underlined letter or using a pointing device.

Routing the design

Once you've placed all the components, you're ready to route the board. You can route a board manually or use an autorouter. Tango-PCB Plus does not include an auto-

router, although Accel sells three of them that are compatible with its layout software and range in price from $595 to $5500.

I didn't use an autorouter on my design. Although an autorouter can save a significant amount of time, you should still expect to do some manual routing. Manual routing may be necessary to finish routes the autorouter was unable to complete or to make improvements to the design after the router is done. Sometimes you may want to route critical signals before autorouting.

Routing a design manually using Tango-PCB Plus involves selecting a net from the rats nest and specifying each corner or layer change as you place the net. You can disable all other connections in the rats nest to see the connections better, or you can select all the nets going to one component. As you route a net, the software automatically inserts a via every time you change layers.

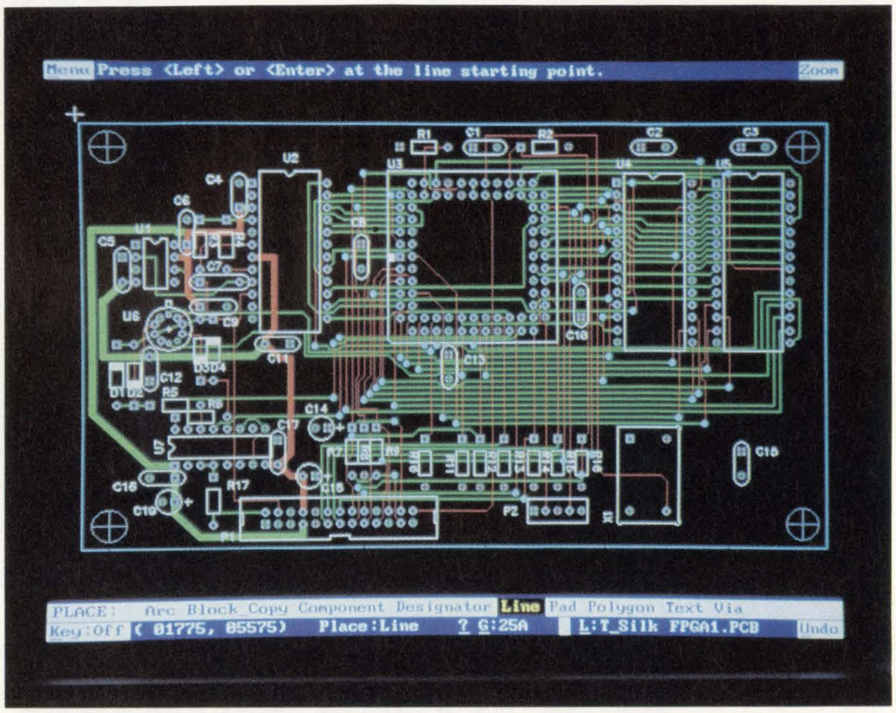
You may want to use curved traces on some designs. Tango-PCB Plus can create curved traces and square and elliptical pads, including round ones.

Copper fills and pours

Other routing operations are making copper fills and copper pours. A copper fill is usually the filling of a polygon you create on one or more of the board layers with copper. You cannot pass a track through the region because a copper fill does not create clearances inside the copper-fill area.

A copper pour does provide clearance around tracks, pads, and vias. Making copper pours is the more difficult operation because the copper pour provides clearances but should not create any unconnected copper areas. Tango-PCB Plus lets you create copper fills but not copper pours.

After you've routed your design, you need to make sure that the connections have all been made correctly and that you have designed the board with proper clearances between pads, tracks, and vias. Tango-PCB Plus lets you automatically verify that the connections match the netlist. The software also checks clearances using design-rule checking.



I designed this board with ample space between components for easy routing. I could compress the design considerably and still route it on two layers.

On Tango-PCB Plus, design-rule checking runs as a batch operation. You specify what clearances you want between pads, vias, and tracks, and the software writes errors to a file. The file includes complete identification of the nets involved in errors, where the violations occur, and what the actual clearances are. After seeing the listing, you can jump to the errors, correct them, and verify that you've fixed all the violations. Design-rule checking found a dozen violations on my design, all of which I easily corrected.

Once you have routed and verified your design, you need to assign components new identifiers. The initial component identifiers are from the schematic and are usually in a random order on the pc-board until you update them. Typically, you assign them in some orderly sequence, such as starting with number 1 in the upper left-hand corner.

Output files

The two outputs generally necessary to manufacture a pc board are a Gerber-format photoplot file and an Excellon-compatible N/C drill file. Both of these file formats are industry standard.

The Gerber-format photoplot file is used to create films for fabricating circuit boards. Because you can create an error when translating your design to the Gerber-format photoplot, you should plot the pc-board design from the Gerber-format photoplot file before you have the film made. Tango-PCB Plus includes the software to perform the translation.

For those interested in saving money, the reference manual for

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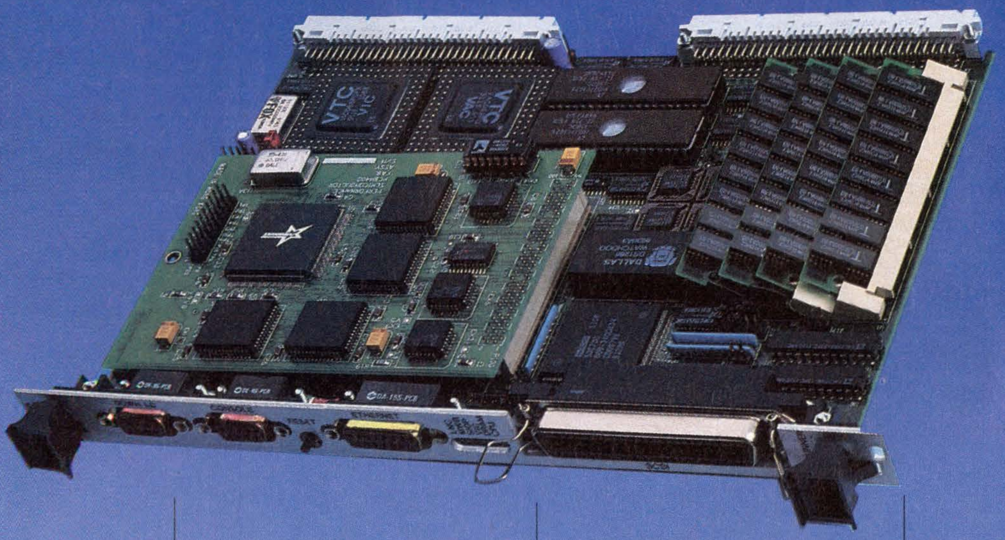

VME

PaceRunner3400 SBC (6U Form Factor)

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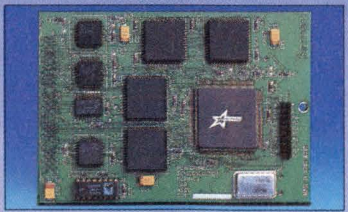
PCBM/3400 MIPS Module

The PCBM3400 (Printed Circuit Board Module) is a highly integrated 32-bit RISC processor module. It can be purchased as a standalone product or as part of the PaceRunner 3400 SBC.



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Additional Software Available for the PaceRunner3400

Company	*Software*
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USL	UNIX
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Benchmarks for PaceRunner3400 VME System 40MHz, 64K Cache

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CIRCLE NO. 44

EDN-TECHNOLOGY UPDATE

PC-BASED DESIGN SOFTWARE

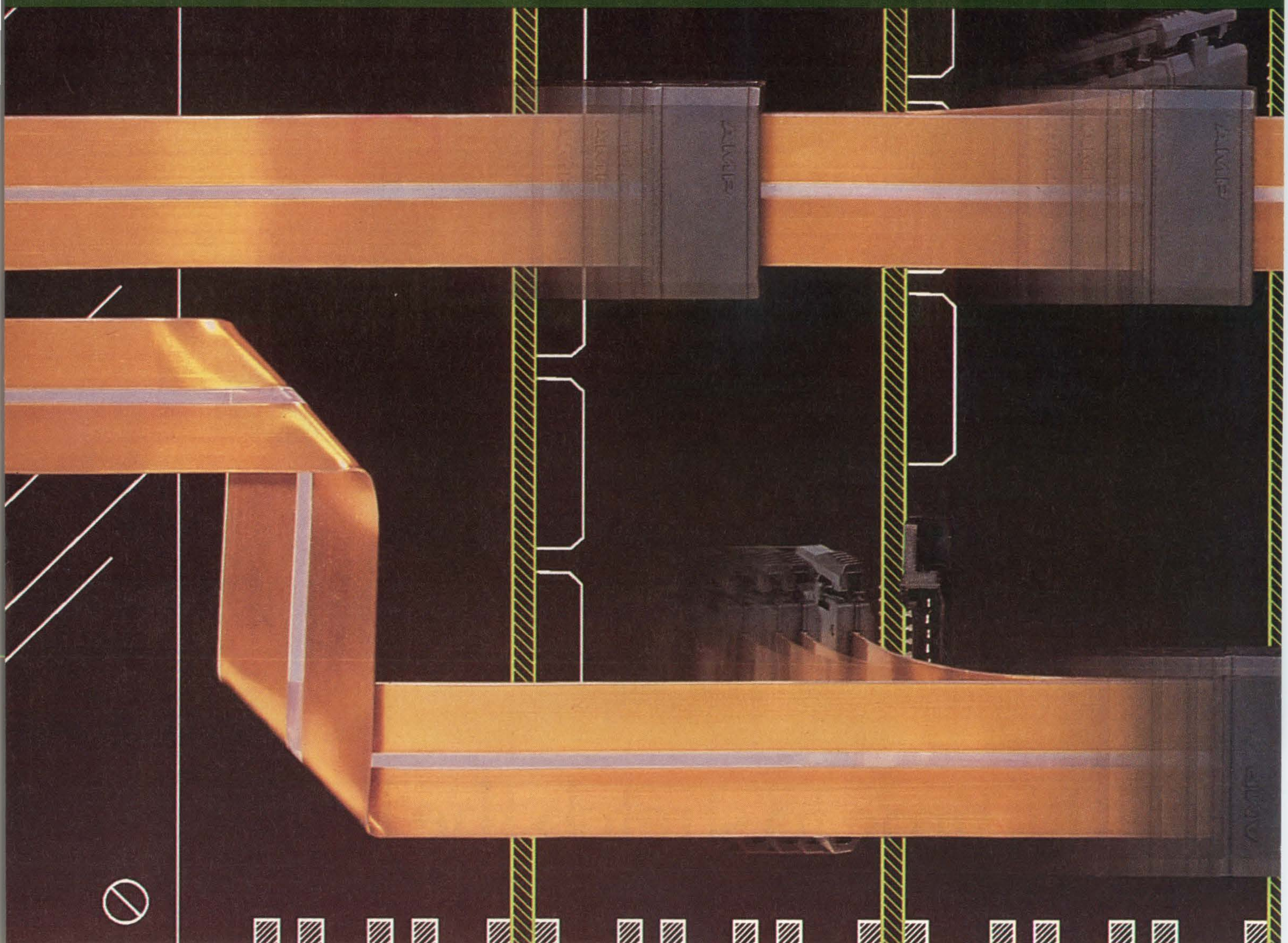
Tango-PCB Plus suggests creating PostScript-compatible outputs, which is the format phototypesetting services prefer. These services can plot film directly from PostScript files. Phototypesetting equipment offers resolutions of 600 to more than 3300 dpi and gives you excellent resolution and fast turnaround on the films. EDN

Reference

1. Conner, Doug, "Low-cost pc-board design tools," *EDN*, June 6, 1991, pg 126.

Article Interest Quotient
(Circle One)
High 479 Medium 480 Low 481

Putting high-performance power distribution on the fast track.



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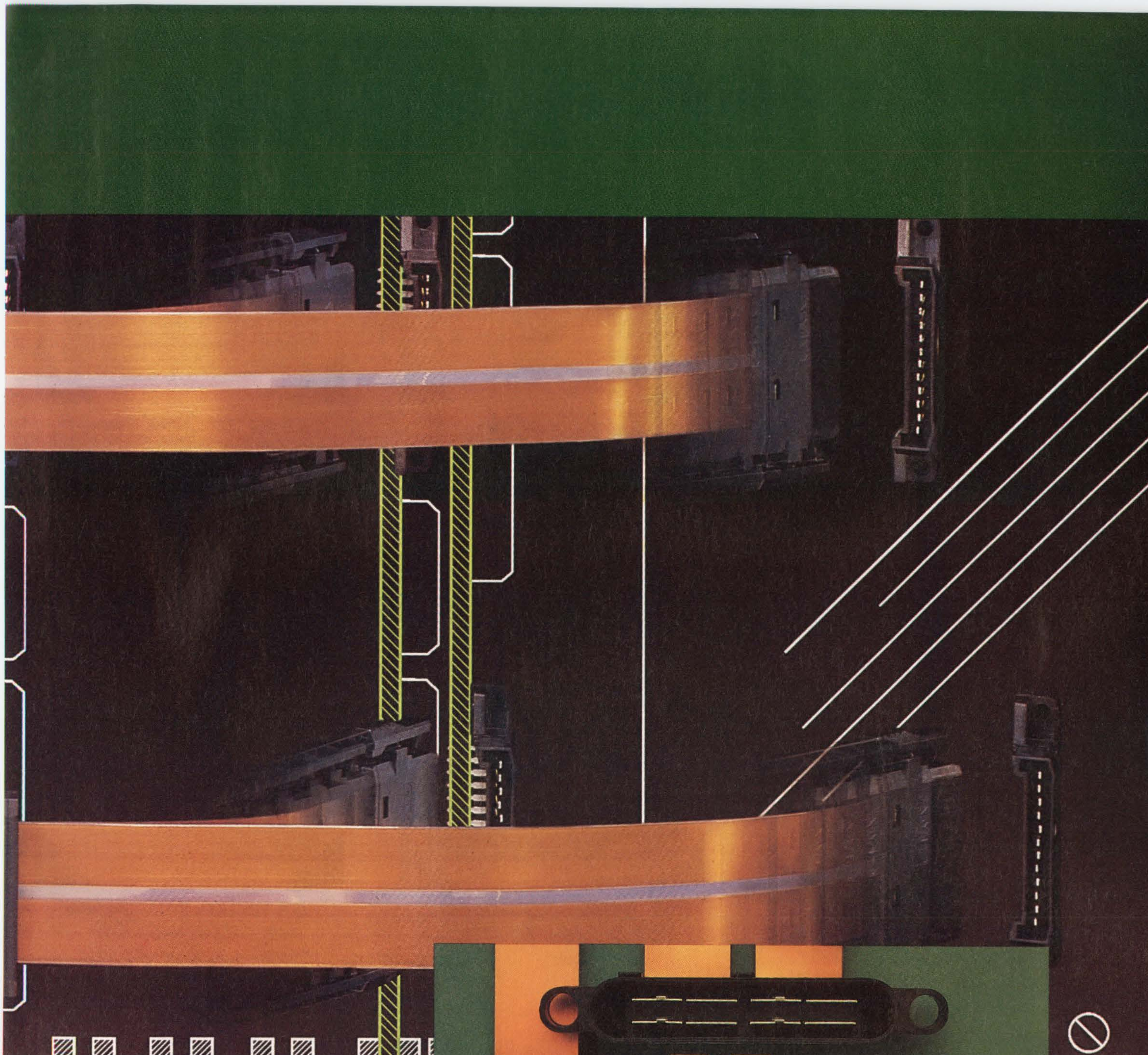
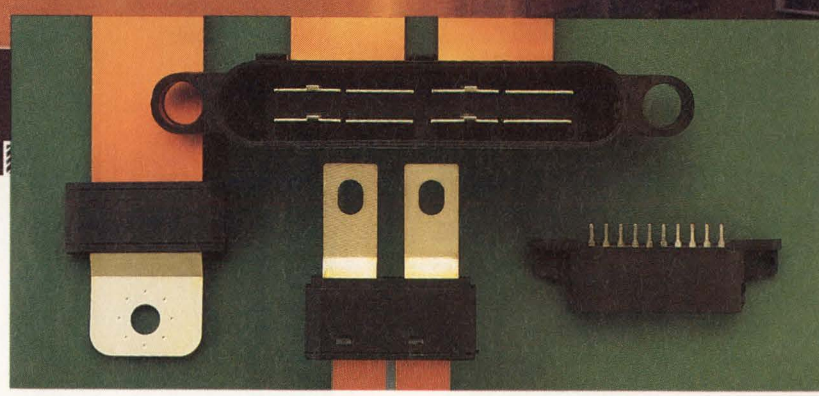
Our newest invention not only makes flat conductors practical, it adds powerful new options to the way you can design your 'flat power' PDS.

AMPOWER Wave Crimp





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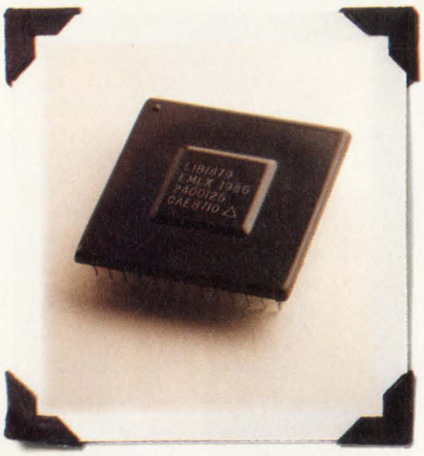
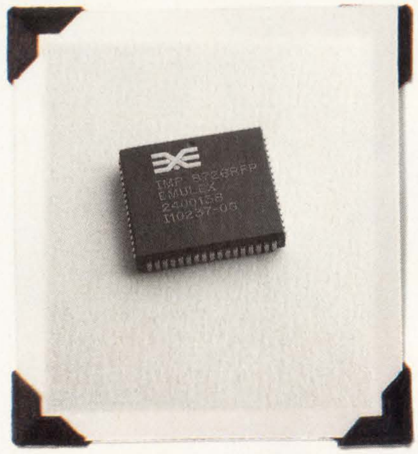
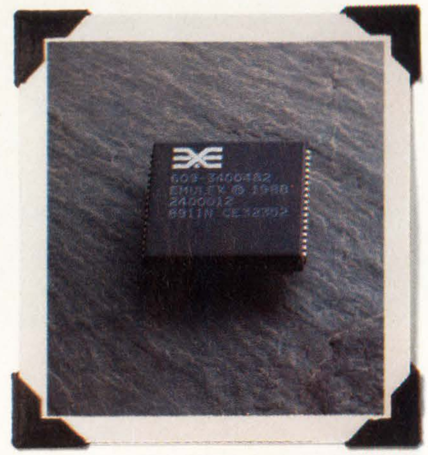


1986-MAC100. We introduce a combined disk formatter and buffer controller in a single disk controller chip.



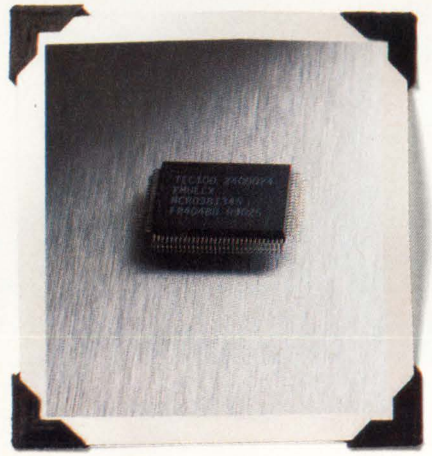
1987-ESP100. The industry's first high-performance SCSI chip is born at Emulex.



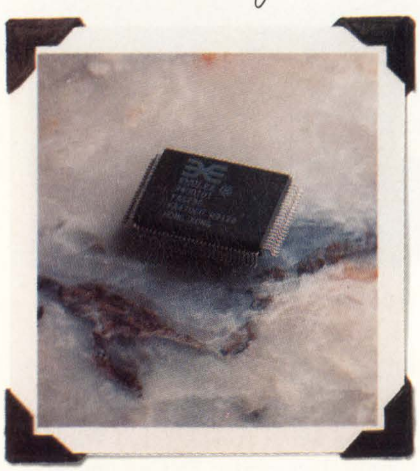
1988-ESP200. Second-generation SCSI arrives with SCSI-2 support and parity pass-through.

1988-MAC200. Our advanced merged architecture controller is the first to include an automated Data Flow feature for faster data handling.

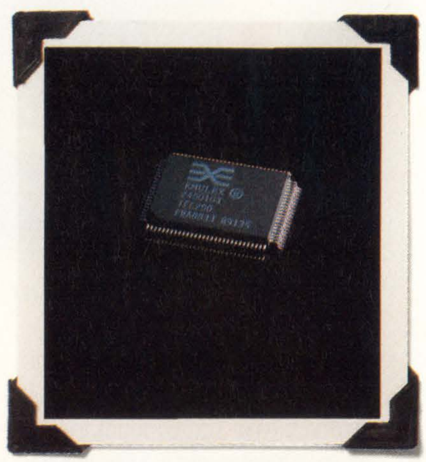
1989-BC200. A dynamic 4-port DMA controller for DRAMs is created.



1989-TEC100. EMD combines disk, buffer, and SCSI controllers in a single chip.



1990-FAS236. We deliver the first Fast SCSI chips with a 16-bit DMA port.



1991-TEC200. Our second-generation TEC becomes the industry's first Fast single-chip disk controller.

1991-TEC256. The first Fast and Wide SCSI disk controller also boasts the fastest disk data rate and highest system bandwidth.

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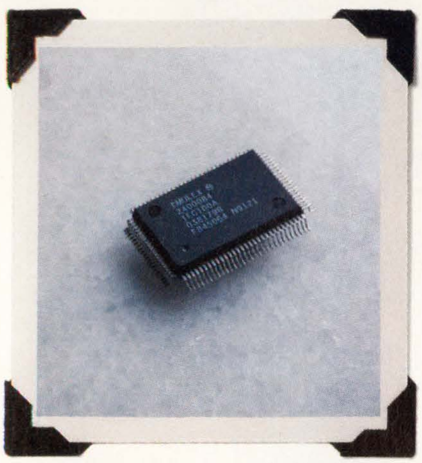
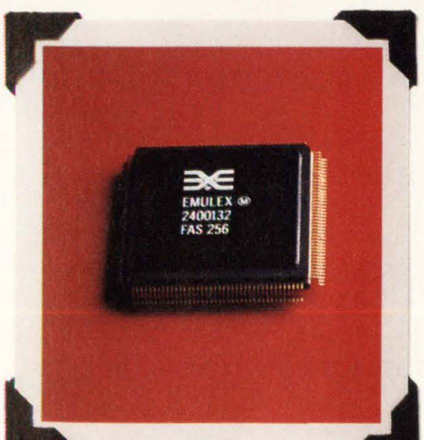


1990-TEC 100A. Mid-to-low capacity SCSI drives get a reduced-price version of the TEC100.



1991-FAS256. 16-Bit Fast and Wide SCSI brings SCSI-2 support to host adapters and peripherals including drive array applications.

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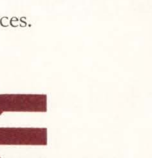

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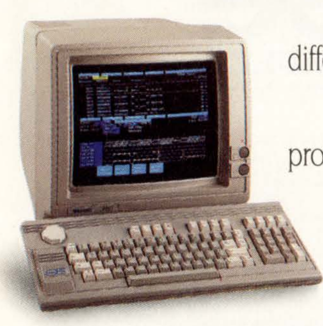

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CIRCLE NO. 48

Application-tailored PLDs streamline designs, bring speed and lower cost

RICHARD A QUINNELL, Technical Editor

PLDs tailored for specific applications offer many performance advantages. The question is, do you want to learn a new architecture?

Between small, general-purpose programmable logic devices (PLDs) and large field-programmable gate arrays (FPGAs) lies a little-known class of programmable logic: application-tailored PLDs. The right tailored device can encompass a design that is too small for an FPGA yet would occupy two to four general-purpose PLDs. The resulting single-chip implementation will be faster, cheaper, and more compact.

The types of application-tailored PLDs available fall roughly into three categories: address decoding, state machine, and system functions. Representative devices in each of these categories appear in **Tables 1, 2,** and **3,** respectively. The amount of tailoring involved varies greatly. Some devices deviate only slightly from a general-purpose architecture, whereas others are built to fit only one application.

At the less-tailored end, classification of a PLD as application-tailored is somewhat arbitrary. Consider, for example, the PALCE16V8-HD from Advanced Micro Devices (**Table 3**). It only deviates from the more general 16V8 by virtue of its drive capability; 64 mA as compared with a more typical 24 mA. The Lattice Semiconductor GAL20XV10B (**Table 1**) deviates from the 20L10 by an exclusive-OR gate in the sum-of-terms path.

At the other extreme are devices like the Altera EPB2001 Micro Channel Architecture interface and the Intel 85C960 bus-control PLDs (**Table 3**), both of which stretch the definition of programmable logic. The bulk of each device is fixed system-interface logic that applies to a single bus structure. The only programmable features are chip-select decoding, ID and status-register coding, and wait-state generation.

Modifying general-purpose PLDs

Most application-tailored PLDs split the difference, however. They resemble general-purpose devices but also include several variations that focus them toward one application. To understand how they deviate from general-purpose devices, compare application-tailored PLDs to the 22V10, a popular general-purpose PLD. **Fig 1** shows the structure

Because third-party design tools may lag new application-tailored PLD architectures, most PLD vendors, like National Semiconductor, offer their own tools.

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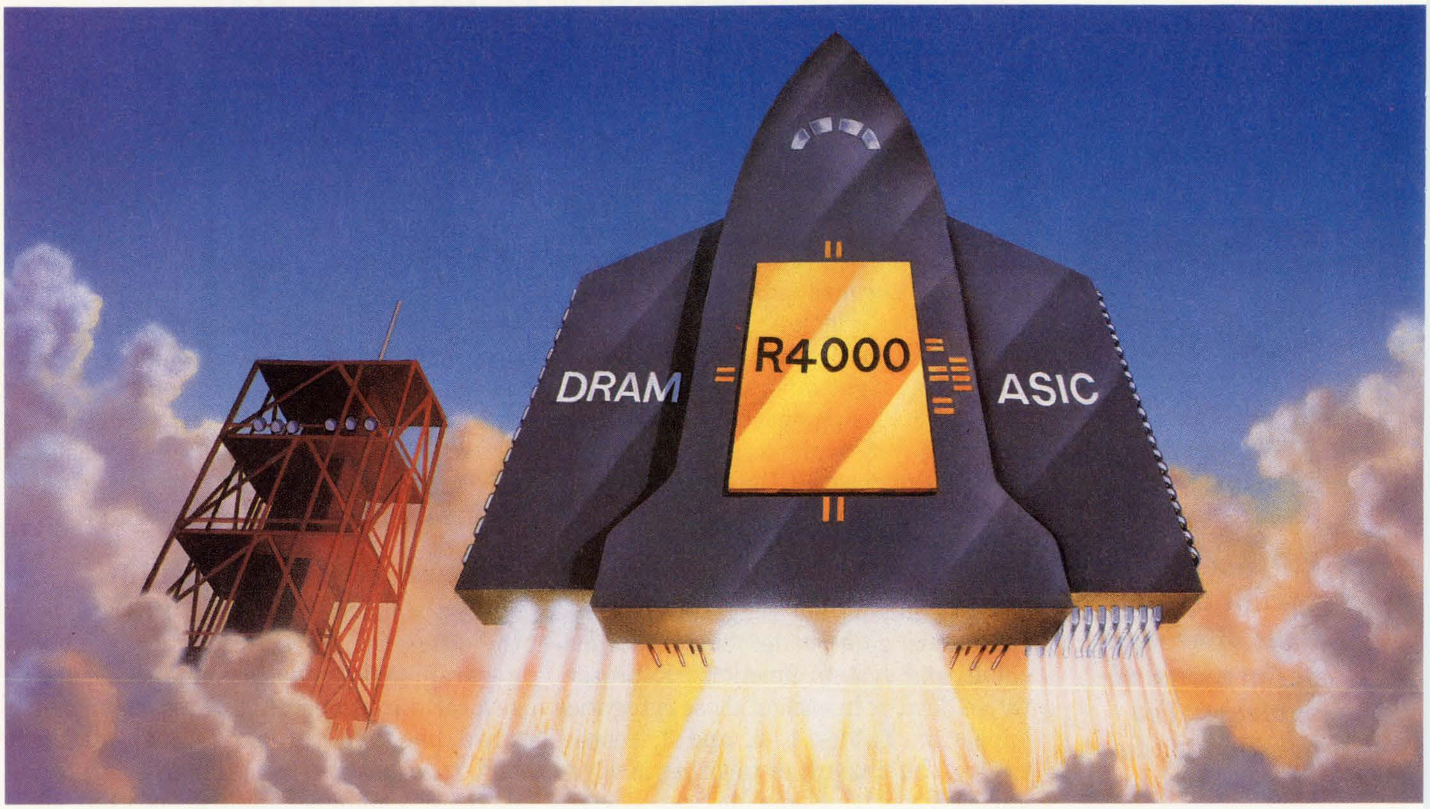

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of one 22V10 output macrocell. The device has 10 macrocells and 12 dedicated input pins.

One way application-tailored devices differ from this type of general-purpose PLD is that they trade unnecessary circuits for more useful additions. Address-decoder PLDs, for example, eliminate the flip-flops and feedback multiplexers found in the **figure** and increase the number of input pins or the summing width over that of the 22V10. Some may also offer input- or output-signal latches for handling pipelined or multiplexed signals.

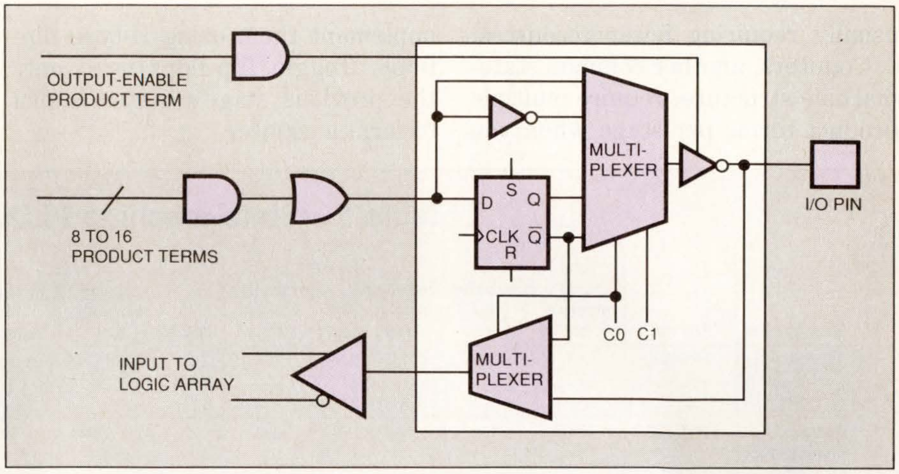

Fig 1—The ever-popular 22V10's output cell structure serves as a good reference for understanding application-tailored PLDs.

Small circuit changes within a general-purpose architecture constitute another common group of variations. State-machine PLDs can resemble a 22V10 but offer J-K, S-R, or toggle-type flip-flops, instead of the D-type flip-flops shown in the **figure**. Some state-machine PLDs also offer one extra gate in the product-term summing path: an exclusive-OR. Both changes seem small, but they will increase a PLD's efficiency in implementing state machines by reducing the design's demand on the device's resources.

For example, state-machine designs often require that a state register be set and held for several clock cycles. To hold the output of a D-type flip-flop in a given state while the flip-flop is being clocked, however, requires the logic array to decode all possible input and state signal combinations that maintain the state. A J-K flip-flop, because it can freeze in a given state, requires only that the logic array decode the set and clear conditions,

Table 1—Decoder PLDs

Manufacturer	Part no.	Input pins	Output pins	Output product terms	Sum terms per output pin	Vendor supplied tool	Third-party tool support	Package type[1]/pins	Price (1000)	Comments
Cypress Semiconductor Corp	CY7C332	13	12	192	9 to 19	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$10.70 (100)	
	CY7B336	12	8	16	NA	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$12.05	Registered inputs, individual output-enable control.
	CY7B337	12	8	32	4	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$12.05	Registered inputs, individual output-enable control.
	CY7B338	12	8	16	NA	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$12.05	Latched output, individual output-enable control.
	CY7B339	12	8	32	4	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$12.05	Latched output, individual output-enable control.
Intel Corp	85C508	16	8	32	NA	PLD Shell Plus (Free)	Yes	DIP/28	$6.10	Latched outputs.
Signetics Co	PHD48N22	36	22	73	1, 7, 12	Slice (Free) Snap ($995)	Yes	PLCC/68	$18	Twelve output pins can be used as input pins
	PLUS153	8	10	32	32	Slice (Free) Snap ($995)	Yes	DIP/20, PLCC/20	$7.74	Output pins can be used as input pins
	PLUS173	12	10	32	32	Slice (Free) Snap ($995)	Yes	DIP/24, PLCC/28	$11.66	Output pins can be used as input pins.

Notes:
1. DIP=Dual in-line package; PLCC=plastic leaded chip carrier; LCC=leadless chip carrier.
2. NA=Not applicable.

usually requiring fewer resources.

Counters, another common state-machine structure, require multiple product terms per stage when you implement them using D-type flip-flops. Toggle flip-flops need only the previous stage's output signal to form a counter.

Another circuit change common to state-machine PLDs is one that allows you to create buried registers without sacrificing I/O pins.

Table 2—State-machine PLDs

Manufacturer	Part no.	Total state registers/ no. buried	Dedicated input pins	Dedicated output pins	I/O pins	Transition product terms	Clocks	Vendor supplied tool	Third-party tool support	Package type/pins[1]	Price (1000)	Comments
Altera Corp	EPS448	448	8	16	NA	768	1	SAM+PLUS ($995)	Programming only, no design	DIP/28, PLCC/28	$12	Microprogrammed sequencer.
Cypress Semiconductor Corp	CY7C330	16/4	11	NA	12	258	2	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$10.15 (100)	Can bury six additional registers without losing I/O pins.
	CY7C331	12	13	NA	12	192	See Note 3	PLD Toolkit ($95)	Yes	DIP/28, PLCC/28, LCC/28	$7.15 (100)	Exclusive-OR gates.
	CY7C335	16/4	12	NA	12	258	3	PLD Toolkit ($95)	Planned for June	DIP/28, PLCC/28, LCC/28	$17.15	Can bury six additional registers without losing I/O pins; available June 1992.
	CY7C361	32	8	10	4	See Note 4	1	Warp 1 ($195)	No	DIP/28, PLCC/28, LCC/28	$24.15	Internal clock doubler.
Lattice Semiconductor	GAL20XV10B	10	11	NA	10	40	1	None	Yes	DIP/24, PLCC/28	$9	Exclusive-OR gates.
	GAL6002B	18/8	11	NA	10	64	1	None	Yes	DIP/24, PLCC/28	$12	Exclusive-OR gates, individually controlled output enables.
	GAL20RA10	10	10	NA	10	80	See Note 5	None	Yes	DIP/24, PLCC/28	$15	Exclusive-OR gates.
National Semiconductor Corp	MAPL128	24/8	9	4	12	128	1	Opal ($495)	Yes	PLCC/28	$15.50	Logic array in eight pages, only one page is active at a time.
	MAPL144	24	9	12	12	128	1	Opal ($495)	Yes	PLCC/44	$20	Logic array in eight pages, only one page is active at a time.
	GAL6001	18/8	10	NA	10	64	2	Opal ($495) Opal Jr (free)	Yes	DIP/24, PLCC/28	$9.45	Registered inputs.
Signetics Co	PLC42VA12	10	10	NA	12	64	1	Snap ($995) Slice (free)	In review	DIP/24, PLCC/28		Can bury any register without loss of I/O pin.
	PLUS105	6/6	16	8	NA	48	1	Snap ($995) Slice (free)	Yes	DIP/28, PLCC/28	$14.21	Output registers offer no feedback.
	PLUS405	8/8	16	8	NA	64	2	Snap ($995) Slice (free)	Yes	DIP/28, PLCC/28	$17.68	Output registers offer no feedback.
Texas Instruments	TIBPLS506A	16/16	13	8	NA	97	1	Prologic (free)	Yes	DIP/24, PLCC/28	$10.50	Output registers offer no feedback.
	TIBPSG507A	8/8	13	8	NA	80	1	Prologic (free)	Yes	DIP/24, PLCC/28	$10.50	6-bit binary counter on chip; output registers offer no feedback.
Xilinx Inc	XC7236	9	2	4	30	57	4 See Note 3	XEPLD ($995)	Yes	PLCC/44, CLCC/44	$11.30	Arithmetic logic unit output cell.
	XC7272	72	12	18	42	456	2	XEPLD ($995)	Yes	PLCC/68/84, CLCC/68/84, PGA/84	$24.60	Arithmetic logic unit output cell; any register can be buried without loss of I/O pin.

Notes:

1. DIP = Dual in-line package; PLCC = plastic leaded chip carrier; CLCC = ceramic leadless chip carrier; PGA = pin-grid array; LCC = leadless chip carrier.
2. NA=Not applicable.
3. State registers individually clocked from product terms.
4. Logic array offers product of product and sum, not simple product terms.
5. State registers have individual preset, reset, and clock.

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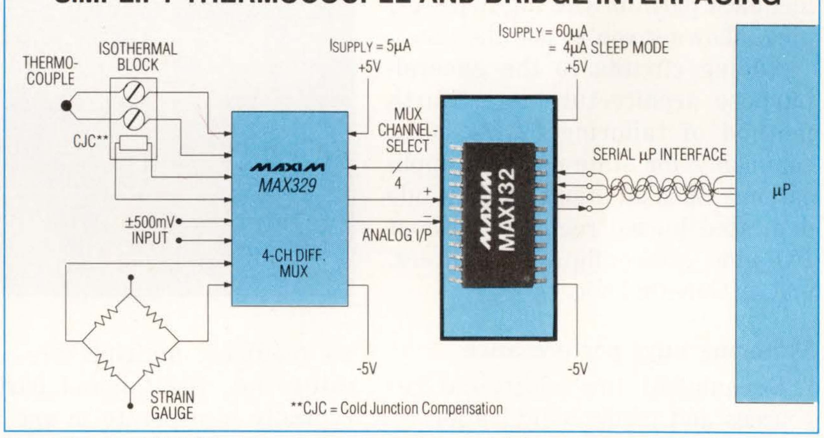

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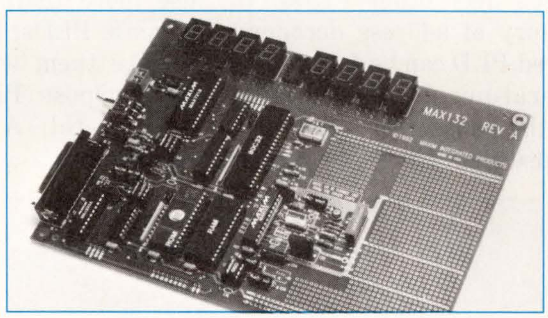

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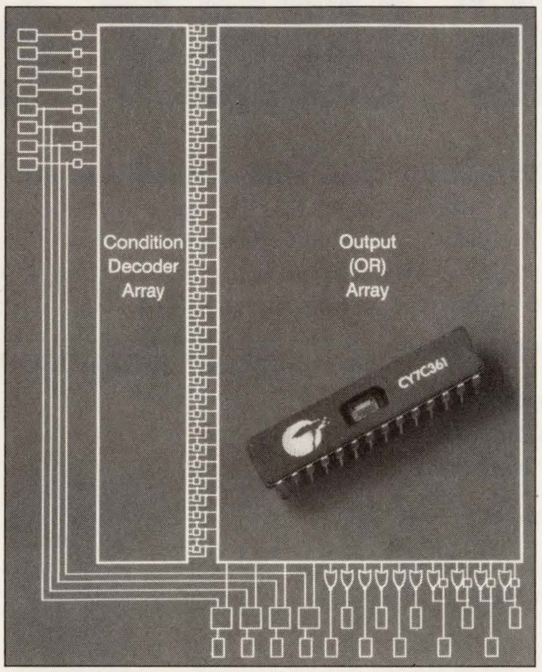
CIRCLE NO. 70

APPLICATION-TAILORED PLDs

Buried registers are flip-flops that hold state values they feed back into the logic array but don't provide as an output signal. As shown in **Fig 1**, when you route a flip-flop's output signal back into the logic array on the 22V10, you cannot use its I/O pin as an input line. If you don't need to bring the signal out, the pin is wasted. Application-tailored PLDs provide an alternate feedback path for the flip-flop's I/O pins, allowing you to use the pin.

Adding circuits to the general-purpose architecture is a fourth method of tailoring PLDs, most commonly for state-machine applications. Such additions may include dedicated buried registers without I/O pins, preconfigured counters, and arithmetic logic.



State-machine needs are the most common target of application-tailored PLDs. The CY7C361 from Cypress Semiconductor, for example, supports concurrent state machines and multiple simultaneously active states, features not readily implemented in general-purpose PLDs.

Tailoring buys performance

Because of the additional resources and resource-utilization efficiency offered by their specialized architecture, application-tailored PLDs possess cost and performance advantages over other PLDs. In the category of address decoders, the tailored PLD can be faster than its general-purpose equivalent made in the same process technology because the tailored device has no feedback multiplexers. In all categories, the tailored parts can typically incorporate in one device a design that would require two to four general-purpose PLDs, saving board space and parts cost. (If you use more than 10 or 12 general-purpose PLDs, however, you could replace them with one large general-purpose PLD such as those from Actel, Altera, and Xilinx (**Ref 1**).)

Table 3—System PLDs

Manufacturer	Part no.	Application	Vendor-supplied tools	Third-party tool support	Package type*/pins	Price (1000)	Comments
Advanced Micro Devices	PALCE16V8HD	Bus Interface	PALASM 4 ($100)	Yes	DIP/24, PLCC/28	$3.95	16V8 with 64-mA output drive.
Altera Corp	EPS464	Synchronous timing	MAX+PLUS II	No	PLCC/44, QFP/44	$23	Produces video-timing waveforms.
	EPB2001	Micro Channel interface	MCMAP ($650)	No	PLCC/84	$17	Only chip-select and POS codes are programmable.
Intel Corp	85C960	Interface to 80960KA/B	iPLS II	No	DIP/28, PLCC/28	$14.20	Only chip-select and wait-state table are programmable.

Note:
*DIP=Dual in-line package; PLCC=plastic leaded chip carrier; QFP=quad flatpack.

Compacting your design into a single device also can boost system performance or reduce the cost of other system components. A design spread over several devices almost always has output signals that cascade through two or more devices, increasing the final signal's propagation delay. By keeping the design in a single device, you eliminate the additional delay. This streamlining can speed your overall system or add to the timing margin on another device, such as static RAM, lowering its speed requirement and cost.

Another advantage of application-tailored PLDs is that they give you the opportunity to create more robust designs. You can try to squeeze your address-decoding design into one general-purpose PLD, for example, but you'll have to sacrifice complete decoding. A 22V10 has at most 21 input pins available, even when you dedicate the entire PLD to decoding one chip select. In a 32-bit address space, the smallest block a 21-input decoder can resolve is 2048 words.

Such incomplete decoding wastes 90% of the 22V10's logic. It also wastes your system's address

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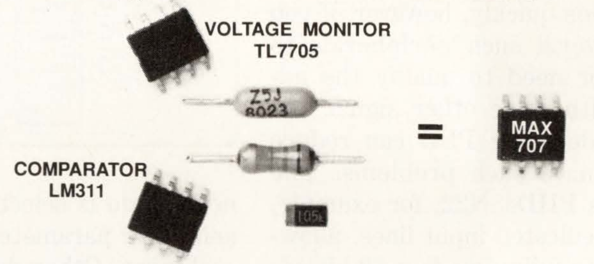

The MAX707 eliminates a TL7705, LM311, 0.1µF capacitor, resistor and tantalum surface-mount capacitor saving design time and space while providing guaranteed performance.

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MAX705	4.65	✔	✔		✔		1.02
MAX706	4.40/3.08/2.93/2.63	✔	✔		✔		1.02
MAX707*	4.65	✔	✔			✔	0.88
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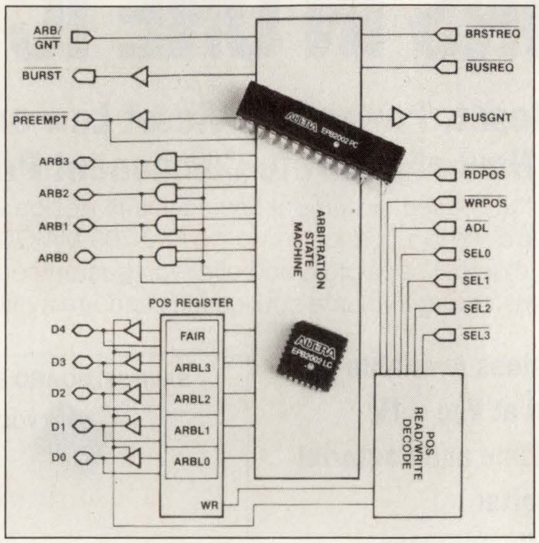
CIRCLE NO. 71

APPLICATION-TAILORED PLDs



The range of application-tailored PLDs runs from minor variations of general-purpose devices to almost fully specified logic. This Micro Channel Architecture arbitration PLD from Altera, for example, only has programmable logic in its register-address and address-decode sections.

space. You have to dedicate the entire decoded block to one peripheral, even if it doesn't need that many addresses. In addition, logical images of the device will fill the remaining space, leaving open the possibility of inadvertently accessing one of the images of a peripheral rather than the peripheral itself.

If your system can tolerate the wasted addresses and multiple peripheral images, fine. The wastage compounds quickly, however, if you have several such peripherals to handle or need to qualify the address with some other signal. An address-decoding PLD can reduce or eliminate such problems. The Signetics PHD48N22, for example, has 36 dedicated input lines, allowing you to fully decode a 32-bit address with address qualifiers (such as read or write) for as many as 22 peripherals.

System PLDs save design time

System-level PLDs have the benefit of simplifying your design task. In the case of the bus-interface PLDs, all of the system-interface logic is preconfigured. All you need to do is select the addressing and other parameters that vary for each user. Other devices offer predesigned system functions in their support software. The Altera EPS464 synchronous timing generator's software, for example, includes predesigned circuits for creating such waveforms as NTSC, SECAM, and PAL video-timing signals.

Despite their advantages, there are several reasons you may not want to use an application-tailored PLD. For one, every additional PLD type you wish to use is another architecture to support. You will need to learn the architecture and add the device to your company's stocking system. Adding a part to your system can include qualifying the vendor, preparing specification documents, establishing incoming inspection procedures, testing the device, and purchasing an initial stocking quantity. You

For more information . . .

For more information on the application-tailored PLDs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

Actel Corp
955 E Arques Ave
Sunnyvale, CA 94086
(408) 739-1010
FAX (408) 739-1540
Contact Andy Haines
Circle No. 700

Advanced Micro Devices Inc
Box 3453
Sunnyvale, CA 94088
(800) 222-9323;
(408) 749-5703
Circle No. 701

Altera Corp
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San Jose, CA 95134
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FAX (408) 435-1394
Contact Craig Lytle, x2189
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Hillsboro, OR
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FAX (503) 681-3037
Contact Steve Stark
Circle No. 705

National Semiconductor Corp
2900 Semiconductor Dr
Box 58090
Santa Clara, CA 95052
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FAX (408) 721-5559
Contact Dennis Swan
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Sunnyvale, CA 94088
(408) 991-2362
FAX (408) 991-2268
Contact Jesse Jenkins
Circle No. 707

Texas Instruments
8330 LBJ Freeway
Dallas, TX 75243
(214) 997-5470
FAX (214) 997-5452
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APPLICATION-TAILORED PLDs

may not have the time, inclination, or corporate funds to take those steps.

The definition of support includes the need for PLD design and programming tools. That may mean acquiring and learning a new tool as well as a new architecture. Not all application-tailored PLDs are supported by popular third-party design and programming tools. In addition, when a vendor releases a new PLD, there is often a lag between the part's introduction and third-party support. In some cases, this lag lasts as long as a year.

Devices that are significant departures from general-purpose architectures also initially may not receive adequate third-party support. These tool vendors' engineers must explore the new architecture's subtleties before they can design the best tools. Thus, the first version of third-party tools may not allow you to take full advantage of the new architecture's features. While you wait for the third-party tool vendors to catch up, you will have to rely on the PLD vendor's design tools.

PLD vendors are sensitive to tool-support problems and are taking steps to reduce them. Some vendors concentrate on providing high-quality tools of their own. Many others try to keep their architectures as similar to existing devices as possible to make third-party tool support easier to obtain. An increasingly common approach, however, is to assist the third-party vendors by providing software fitters, that is, software that maps a logic design into this specific architecture.

The fitter approach reflects the changes tool vendors are making in the way they add to their device libraries. Instead of providing a single tool that handles all PLD types and making revisions to add types, they are providing frameworks that accept additional fitters (**Ref 2**). The PLD vendors can take the responsibility to supply fitters for their parts, ensuring speedy and adequate tool support. They know that, without adequate tool support, an application-tailored PLD won't suit your system's needs. EDN

References

1. Conner, Doug, "High-density PLDs," *EDN*, January 2, 1992, pg 77.
2. Quinnell, Richard A, "Synthesis tools speed PLD design efforts," *EDN*, April 11, 1991, pg 73.

Article Interest Quotient
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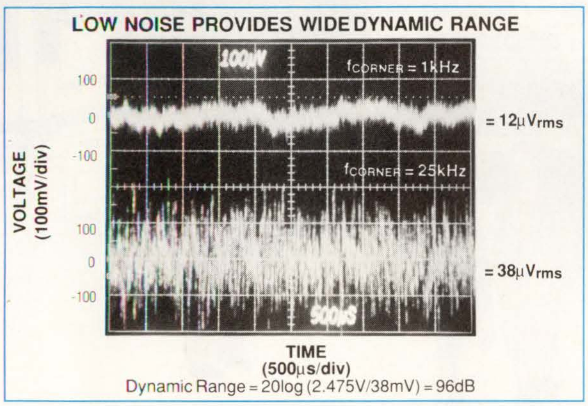

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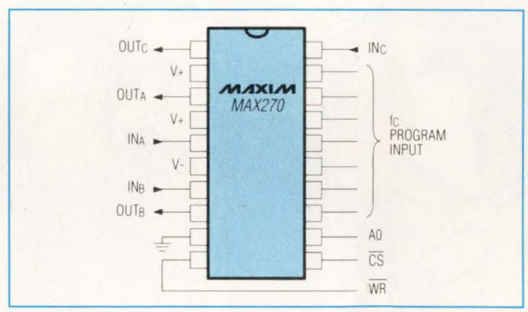

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CIRCLE NO. 75

EDN CARAVAN ELECTRONIC SHOW TOURS

The Electronic Trade Show on Wheels

DATE	TIME	LOCATION
5/1 Friday	9:00-11:00 AM	HONEYWELL INC. 1100 Virginia Drive, Fort Washington, PA
5/1 Friday	12:30-2:30 PM	UNISYS CORP., East Coast Dev. Ctr. 2476 Swedesford Road, Paoli, PA
5/4 Monday	9:00-11:00 AM	GE ASTROSPACE DIVISION 230 Goddard Blvd., King of Prussia, PA
5/4 Monday	1:00-3:00 PM	GE ASTROSPACE DIVISION Jct. Routes 571 & 535, East Windsor, NJ
5/5 Tuesday	9:00-11:30 AM	AT&T BELL LABORATORIES Crawfords Corner Road, Holmdel, NJ
5/5 Tuesday	12:30-2:00 PM	AT&T BELL LABORATORIES 200 Laurel Avenue, Middletown, NJ
5/5 Tuesday	3:00-4:30 PM	AT&T BELL LABORATORIES 307 Middletown-Lincroft Rd., Lincroft, NJ
5/6 Wednesday	11:00-1:30 AM-PM	AT&T BELL LABORATORIES 600 Mountain Avenue, Murray Hill, NJ
5/7 Thursday	8:30-11:00 AM	AT&T BELL LABORATORIES 67 Whippany Road, Whippany, NJ
5/7 Thursday	12:00-1:30 PM	SMITHS INDUSTRIES, INC. 7-11 Vreeland Road, Florham Park, NJ
5/8 Friday	9:00-11:00 AM	GEC MARCONI ELECTRONICS 150 Parish Drive, Wayne, NJ
5/8 Friday	1:00-3:00 PM	BENDIX GUIDANCE & CONTROL SYSTEMS Route 46, Teterboro, NJ
5/11 Monday	9:00-12:00 AM	GRUMMAN CORPORATION Stewart Avenue, Bethpage, NY
5/11 Monday	1:30-3:30 PM	GRUMMAN CORPORATION Maxess Road, Melville, NY
5/12 Tuesday	9:00-11:00 AM	LORAL ELECTRONICS Ridge Hill, Yonkers, NY
5/12 Tuesday	1:30-3:30 PM	PERKIN ELMER CORP. 50 Danbury Road, S. Wilton, CT
5/13 Wednesday	8:00-10:30 AM	SIKORSKY AIRCRAFT 6900 N. Main Street, Stratford, CT
5/13 Wednesday	12:30-2:00 PM	PITNEY BOWES INC. One Waterview Drive, Shelton, CT
5/13 Wednesday	3:00-4:15 PM	PITNEY BOWES INC. 1 Parrot Drive, Shelton, CT
5/14 Thursday	8:30-10:30 AM	GENERAL DATA COMM, INC. Straights Turnpike, Middlebury, CT
5/14 Thursday	1:00-2:30 PM	BRISTOL BABCOCK INC. 1100 Buckingham Street, Watertown, CT
5/15 Friday	11:00-1:30 AM-PM	RAYTHEON CO., Submarine Signal Div. 1847 West Main Road, Portsmouth, RI
5/18 Monday	9:00-10:30 AM	CODEX CORPORATION 85 Dan Road, Canton, MA
5/18 Monday	11:30-1:00 AM-PM	NORTHROP CORPORATION 111 Morse Street, Norwood, MA
5/18 Monday	2:00-3:30 PM	FOXBORO COMPANY 38 Neponset Ave., Foxboro, MA
5/19 Tuesday	8:30-11:00 AM	POLAROID CORPORATION 565 Technology Square, Cambridge, MA
5/19 Tuesday	12:30-2:30 PM	BOLT, BERANEK & NEWMAN, INC. 70 Fawcett Street, Cambridge, MA
5/20 Wednesday	8:00-10:30 AM	AT&T BELL LABORATORIES 1600 Osgood Street, North Andover, MA
5/20 Wednesday	11:30-1:30 AM-PM	RAYTHEON CO., Missile Systems Div. 50 Apple Hill Drive, Tewksbury, MA
5/21 Thursday	8:30-10:00 AM	LOCKHEED/SANDERS ASSOCIATES 65 River Road, Hudson, NH
5/21 Thursday	11:00-12:30 AM-PM	LOCKHEED/SANDERS ASSOCIATES 95 Canal Street, Nashua, NH
5/21 Thursday	1:30-3:30 PM	KOLLSMAN CORPORATION 220 Daniel Webster Hwy., Merrimack, NH
5/22 Friday	10:00-12:30 AM-PM	DIGITAL EQUIPMENT CORPORATION 126 Main Street, Maynard, MA
5/26 Tuesday	8:30-10:00 AM	RAYTHEON COMPANY, Equipment Div. 528 Boston Post Road, Sudbury, MA
5/26 Tuesday	11:00-12:30 AM-PM	RAYTHEON COMPANY, Equipment Div. 430 Boston Post Road, Wayland, MA
5/26 Tuesday	2:00-3:30 PM	RAYTHEON COMPANY, Equipment Div. 1001 Boston Post Road, Marlboro, MA
5/27 Wednesday	10:00-1:00 AM-PM	GTE GOVERNMENT SYSTEMS CORP. 197 First Street, Needham, MA
5/27 Wednesday	2:30-4:00 PM	DATA GENERAL CORPORATION 4400 Computer Drive, Westboro, MA
5/28 Thursday	9:00-11:30 AM	IBM CORPORATION Neighborhood Road, Kingston, NY
5/28 Thursday	1:30-3:30 PM	IBM Corporation Boardman Road, Poughkeepsie, NY
5/29 Friday	9:00-11:30 AM	GENERAL ELECTRIC COMPANY 1 River Road, Schenectady, NY
5/29 Friday	12:30-2:30 PM	GENERAL ELECTRIC COMPANY CR&D Center, Schenectady, NY
6/1 Monday	9:00-11:30 AM	CAE-LINK CORPORATION Kirkwood Industrial Park, Binghampton, NY
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6/3 Wednesday	9:00-11:00 AM	SMITH CORONA CORP. 839 Route 13, South, Cortland, NY
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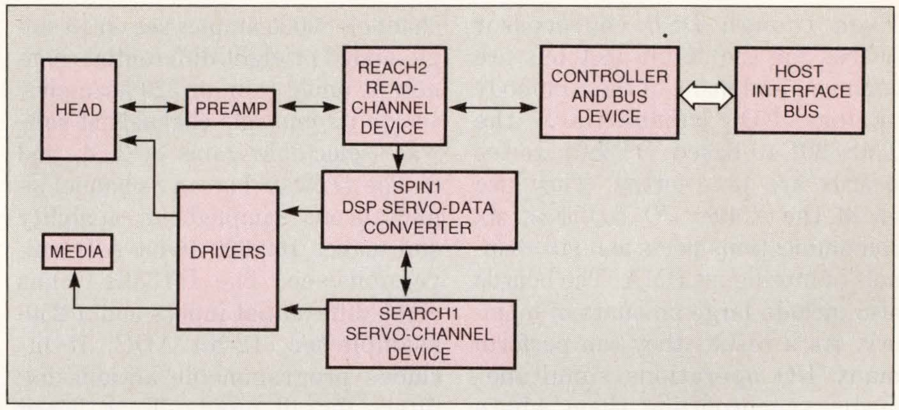
6/5 Friday	8:30-11:00 AM	ALLEN-BRADLEY COMPANY 747 Alpha Drive, Highland Heights, OH
6/5 Friday	12:30-2:30 PM	WESTINGHOUSE ELECTRIC CORP., Naval Systems 18901 Euclid Avenue, Cleveland, OH
6/8 Monday	9:00-11:00 AM	RELIANCE ELECTRIC COMPANY 6065 Parkland Blvd., Cleveland, OH
6/8 Monday	12:30-2:00 PM	PICKER INTERNATIONAL 595 Miner Road, Highland Heights, OH
6/9 Tuesday	9:00-11:00 AM	SYSTEMS RESEARCH LABORATORIES 2800 Indian Ripple Road, Dayton, OH
6/9 Tuesday	1:30-4:00 PM	NCR CORPORATION Brown & Caldwell Streets, Dayton, OH
6/10 Wednesday	9:00-12:00 AM	LEXMARK INTERNATIONAL 740 New Circle Drive, Lexington, KY
6/11 Thursday	9:00-11:30 AM	AT&T CONSUMER PRODUCTS LABS 6612 E. 75th Street, Indianapolis, IN
6/11 Thursday	1:30-3:30 PM	GM/DELCO ELECTRONICS 2150 East Lincoln Road, Kokomo, IN
6/12 Friday	9:00-11:00 AM	MAGNAVOX GOV'T & INDUSTRIAL ELECTRONICS 1313 Production Road, Fort Wayne, IN
6/12 Friday	12:30-2:30 PM	ITT Aerospace/Communications Div. 1919 West Cook Road, Fort Wayne, IN

CIRCLE NO. 77

Programmable chip set lowers power and reduces size of disk drives

Hard-disk-drive designs typically require custom analog circuits to handle data and servo functions, but a 3-chip set, called Search1, may change that. The set combines programmable analog and digital signal-processing techniques to achieve flexibility in a standard product.

The three chips are the Search1 servo-channel device, the Reach2 read-channel device, and the Spin1 servo-processor interface. Collectively, they dissipate <1W when active. The set typically uses less power, however, because it offers numerous power-saving modes.



Search1 from AT&T integrates most of the functions needed in a hard-disk drive in a 3-chip set. Together, the devices consume <1W when fully active and offer some 600 power-saving operating modes.

The Search1 (ATT93C010) incorporates three independent processors: a general-purpose microcontroller (μC), a digital signal-processing (DSP) μP, and a timing processor. The general-purpose μC, based on a 30-MHz 80C31 with 256 bytes of RAM, manages the host interface and data-path control. The DSP μP handles digital filtering and compensation for the servo channel. The timing processor generates and monitors servo timing signals as well as clocks for other chips in the set.

The Reach2 (ATT91C020) contains all of the analog read-channel and servo-demodulator circuits. Its functions include a programmable frequency synthesizer, AGC circuits, a 7-pole data-channel filter, a third-order servo filter, pulse and peak detectors, a write-precompensation circuit, a data synchronizer, a servo demodulator, and an RLL (1,7) encoder/decoder (ENDEC). The device offers separate channels for the servo and data circuits, allowing you to turn off the data circuits to save power when operating the disk drive in a track-follow mode.

The Spin1 (ATT93C010) includes 10-bit ADCs and DACs, a 6-channel analog multiplexer, six digital-output storage registers, an 8- or 16-bit multiplexed processor interface, and an internal voltage reference. The data converters let you monitor and control the disk's voice-coil actuator and monitor servo bursts.

The chip set's programmability provides multizone, constant-density recording at data rates from 6.67 to 40 Mbps. Factors such as pulse-detector qualification thresholds, analog-filter corner frequencies, data precompensation, and data-synchronizer window shift let you control virtually all of your drive's operating parameters and qualification levels.

The programmability comes in many forms. The processors use RAM-based programming. The filters use signals from the frequency synthesizer together with phase-locked loops to set corner frequencies. Many of the other programmable elements are accessible through a serial interface.

The set's programmability also extends to its power consumption. Because CMOS logic's power consumption is frequency dependent, you can control the power of a functional block by adjusting its clock rate. Many of the set's functional elements depend on clocks from the frequency synthesizer. Therefore, you can reduce average power consumption by slowing the clocks to sections not in use.

A development kit is available to help speed your system design. It includes an evaluation board, source code for actuator and servo spindle control, DSP and μC assemblers, and application notes. The board is usable with any 80C31 emulator for debugging control software. Its prototyping area lets you add the magnetic head preamplifiers and drivers, then connect the board to your drive prototypes. Sample prices are <$10 for the Search1 and Reach2 chips and <$4 for the Spin1. The devices come in shrink quad flatpacks.

—Richard A Quinnell

AT&T Microelectronics, Dept 52040420, 555 Union St, Allentown, PA 18103. Phone (800) 372-2447, ext 829; in Canada (800) 553-2448. FAX (215) 778-4106. **Circle No. 735**

DSP boards pack lots of memory and unusual I/O capabilities

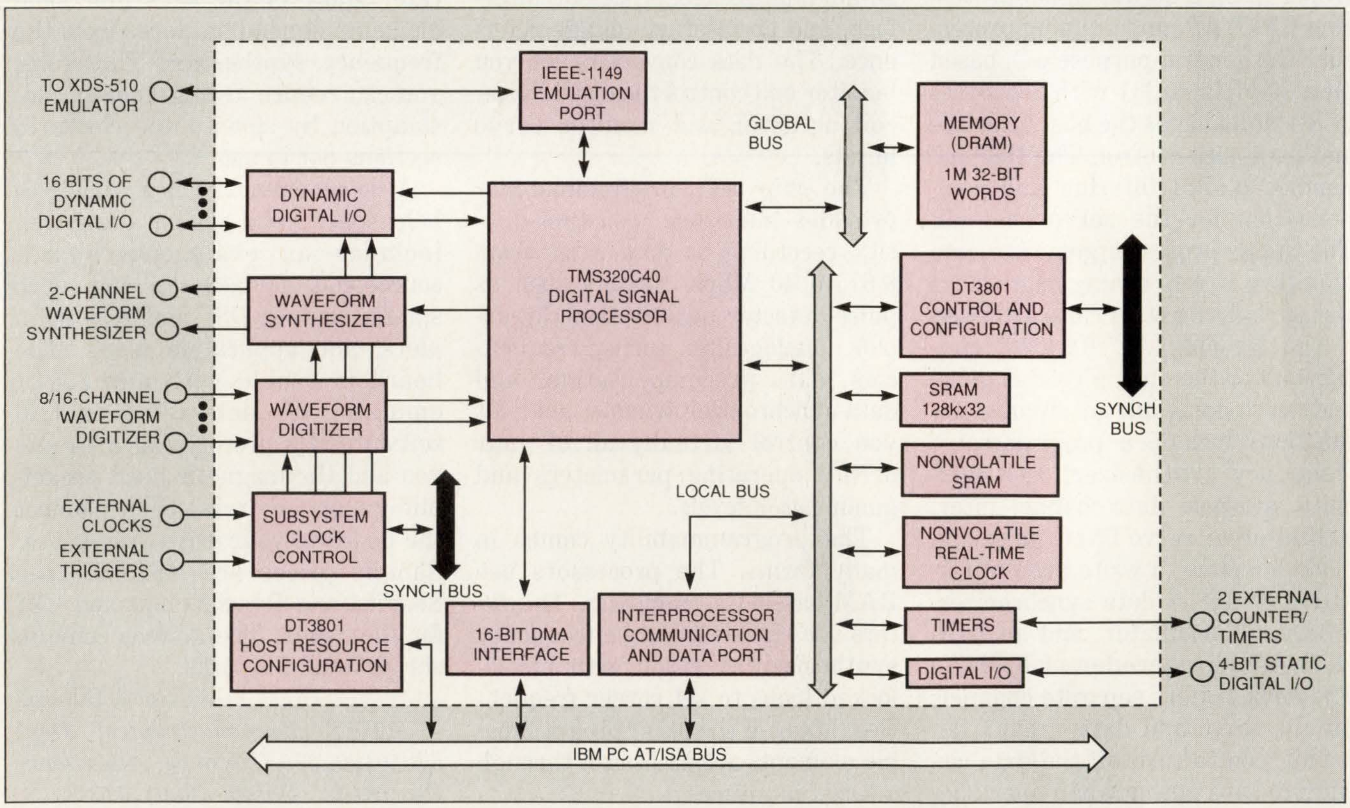
Even though DSP coprocessor boards for the 16-bit ISA bus are common, and many of them embody analog I/O capabilities, the TMS320C40-based DT3801 series boards are noteworthy. They use all of the 'C40's I/O facilities: six communications ports and six channels of intelligent DMA. The boards also include large amounts of memory. As a result, they can perform many I/O operations simultaneously, synchronizing them where appropriate. The architecture also allocates computing tasks optimally: the host PC's CPU handles data management; the DSP µP does the number crunching.

The DT3809 has a 12-bit ADC and takes 1 Msample/sec on one channel, 800 ksamples/sec on 16 single-ended or eight differential channels at unity gain, or 320 ksamples/sec on its multiple channels at software-selectable gains of 2, 4, and 8. The DT3808 has an 8-channel simultaneous sample/hold capability and makes 160,000 16-bit A/D conversions/sec. The DT3801-G has eight differential inputs and a 250-ksample/sec, 12-bit ADC. It includes programmable antialiasing filters for all inputs. Each board also includes two 200k-point/sec, 16-bit DACs and 16 channels of digital I/O that operates to 4 Mbytes/sec.

All models have 4 Mbytes of DRAM, 512 kbytes of SRAM, and 256 bytes of nonvolatile SRAM, in addition to 8 kbytes of configuration RAM (also nonvolatile). The volatile memory is organized in 32-bit words. The densely packed boards use surface-mount components on both sides. The design allows adding still more memory on daughter boards or on additional ISA bus boards. Prices range from $7195 to $7595. A developers' software kit, which includes Spectron's Spox DSP operating system, costs $2995. An emulator for the DSP µP takes advantage of the chip's IEEE-1149 port and costs $8000.

—Dan Strassberg

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. **Circle No. 732**



These boards for the 16-bit ISA bus capture, manipulate, and output waveform data. Nevertheless, the block diagram relegates the I/O functions to a small area at the right. The computational capabilities, implemented in the TMS320C40 DSP µP and several memory subsystems show up much more prominently.

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FAST ANSWERS

FLUKE®

CIRCLE NO. 78

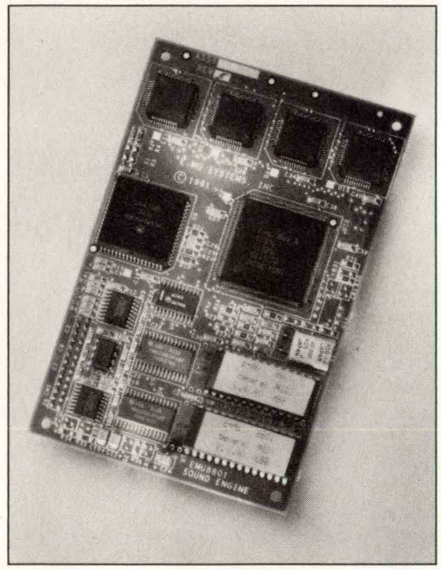
Module adds high-quality sound to multimedia units

High-quality sound can be as important to a multimedia presentation as dazzling graphics displays. The EMU8801 embedded module lets Multimedia Personal Computer (MPC) designers add professional audio to their products via Musical Instrument Digital Interface (MIDI) sequences. Repeated access to digitally stored sound samples conserves system memory space and provides a high degree of interactivity.

The module employs the company's Soundengine technology, which consists of three components—Soundfile ROMs, a dedicated DSP chip called the G1.5 chip, and licensed firmware. The Soundfile ROMs contain 16-bit linear CD-quality digital samples. The 4-Mbyte ROM has more than 210 samples and waveforms, including a selection of musical instruments and sound effects.

The G1.5 chip contains an audio-mixing function that allows the module to generate 32 discrete voices simultaneously. Besides generating addresses to access samples from the Soundfile, the chip performs the timing tasks to generate a 20-Hz to 20-kHz frequency response. It also dynamically controls amplitudes and pitch shifts and drives two DACs and associated reconstruction filters. The two stereo output signals can deliver 4 dBm into 600ω loads. The total-harmonic-distortion plus noise and intermodulation-distortion specifications are less than 0.05%

A 10-MHz 68000 μP controls the Soundengine whose firmware resides in two 64k × 8-bit EPROMs and functions as an operating system for the μP. The firmware also interprets standard MIDI commands from a host computer or a MIDI keyboard via a 26-pin MIDI-compatible connector. The host computer, which generates, stores,



The EMU8801 module lets you add MIDI-controlled professional-quality sound to a multimedia personal computer. Proprietary Soundengine technology contains 16-bit digital samples and generates 32 simultaneous voices.

and edits MIDI sequences, communicates with the board using standard MIDI protocols.

The 3.5 × 5.5-in. Soundengine requires a regulated 5V supply at 500 mA max for the digital sections. The DACs and output op amps require 100 mA max from regulated ±12V supplies. The board sells for $200 (5000). The company also sells the module as a 4-chip set, called the EMU8305, for $99 (50,000).

—John Gallant

Emu Systems Inc, Box 660015, Scotts Valley, CA 95067. Phone (408) 438-1921. FAX (408) 438-8612. **Circle No. 733**

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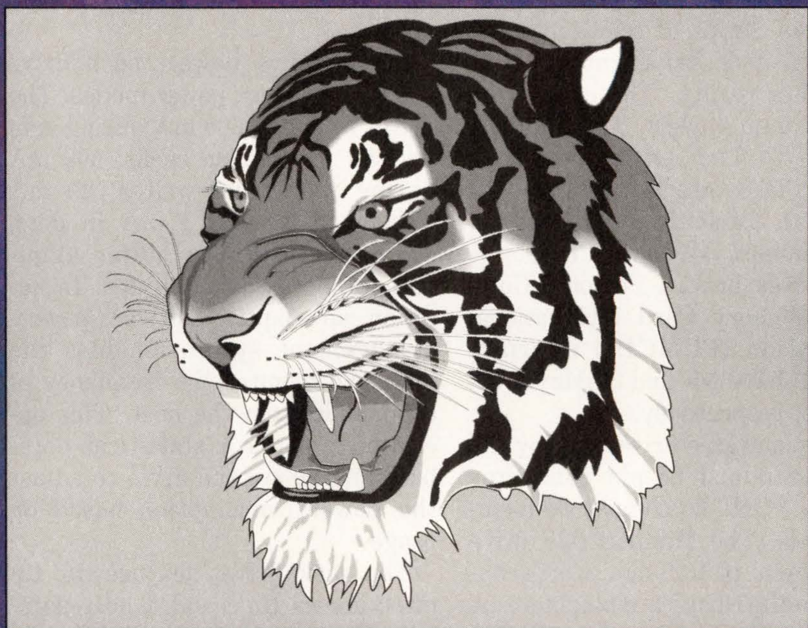

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At last. A personal output device that combines the best features of a desktop laser printer with the ability to produce large format drawings. It's called ProTracer — a 360 dpi desktop printer/plotter that produces A, B, as well as C-size output.

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PACIFIC DATA PRODUCTS

CIRCLE NO. 81

1.8-in. hard-disk drive provides 64 Mbytes

You've probably never thought you'd carry a 64-Mbyte hard-disk drive in your shirt pocket. The Portables Series of removable 1.8-in. hard-disk drives makes this thought a reality. The series consists of four models. The Miniport 64 and 32 fixed embedded drives have an IDE interface and 64- and 32-Mbyte capacities, respectively. The Miniport 64P and 32P removable drives have a Personal Computer Memory Card International Association (PCMCIA) interface and also have 64- and 32-Mbyte capacities, respectively.

The removable drives employ the same standard 68-pin connector used by PCMCIA-compatible memory cards. The Miniport 32P drive has a height of 10.5 mm, which conforms to the thick-card height of the PCMCIA Type III standard. The Miniport 64P has a custom height of 13.5 mm. The 32-Mbyte drive weighs less than 2.3 oz, and the 64-Mbyte drive weighs less than 2.65 oz. Each drive is 2.0 in. wide.

To meet the durability requirements of a portable computer, each drive can withstand a 20g shock while operating and a 200g shock when it's not operating. A mechanical actuator securely parks the head. In addition, a shock-sensor circuit senses jarring movements during write commands to prevent writing on the wrong track. The drives feature a patented spindle-motor design that is shock resistant.

To conserve power, each drive has five different power modes. The drives consume 600 mA during spin up; 300 mA during seeks; 500 mA during reads and writes; 20 mA during sleep; and 1 mA in deep sleep. A 256-kbyte buffer eliminates unnecessary spin-ups. In addition, an adaptive software power-management system enables the drives to monitor the frequency of commands from the host. This operation creates a statistical database and allows the drive to adjust the power consumption based on usage.

The disk drives feature an 18-msec access time and a host data-transfer rate as fast as 5 Mbytes/sec. Other key specifications include average latency of 6.67 msec; track density of 2400 tpi; bit density of 56,000 bpi; spindle speed of 4500 rpm; operating altitude of 40,000 ft; and an MTBF of 250,000 hours. Evaluation units are available for $425, and production quantities will be available in the third quarter of 1992.—**John Gallant**

Ministor Peripherals Corp, 2801 Orchard Pkwy, San Jose, CA 95134. Phone (408) 943-0165. FAX (408) 434-0784. **Circle No. 730**

This series of removable and fixed 1.8-in. disk drives can withstand the rugged requirements for portable and mobile computers.

MAY 1992

NEWS

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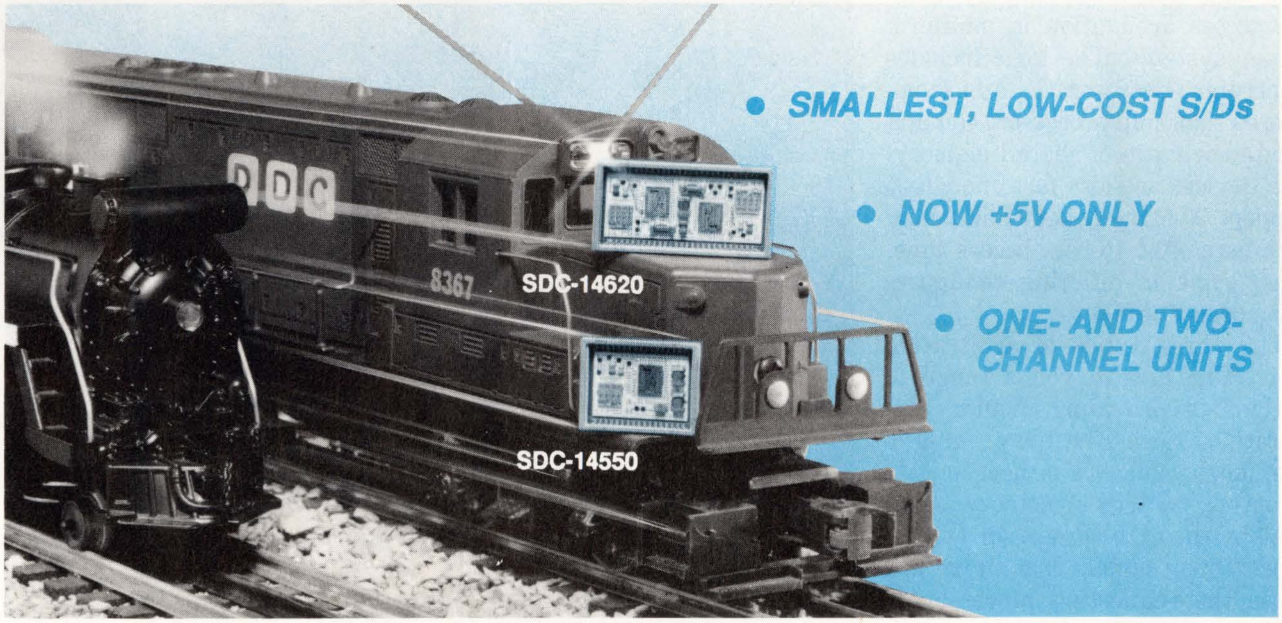

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Circle No. 82 For Literature

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Dual-port SRAMs provide semaphores for software memory arbitration

A 4-member family of dual-port static RAMs (SRAMs) provides on-chip logic that helps simplify memory-access arbitration in multiprocessor systems. The logic includes interrupts, busy signals, and semaphores that help processors communicate their use of shared memory. The devices are also fast enough to support 50-MHz systems; all family members offer 15-nsec access time. They come in differing configurations (See **Table**).

The three types of arbitration logic (**Fig 1**) give you a range of options in providing memory arbitration. First, the busy signal is the most basic. A processor attempting to access memory being used by the other processor will receive a busy signal. That signal will cause the requesting processor to execute wait states until the memory becomes available.

Second, the interrupt signal allows you to avoid wasting time in wait states by allowing processors a basic form of communication. The processor on one port can write a message into a reserved area of the SRAM, causing the SRAM to generate an interrupt to the other processor. The second processor can then read the message to clear the interrupt. This message-passing interrupt scheme allows one processor, for example, to signal the other that the shared memory is now stocked with data for a specific task.

Third, semaphores provide a more sophisticated memory-use signal. The semaphore is a latch that is controlled by only one port at a time; its meaning is determined by system software. When a processor wants to use a semaphore, it addresses that latch and attempts to write a zero. If successful, it will have control of that semaphore. The other processor will read a one and be unable to write a zero to that semaphore until the first processor releases its control. Each device in the family offers eight independent semaphores.

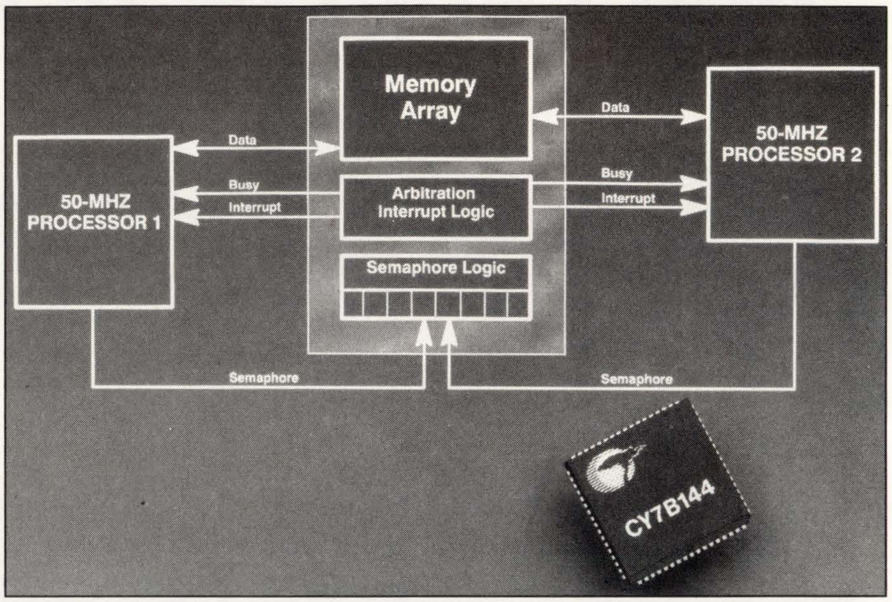

Fig 1—Dual-port SRAMs offer on-chip arbitration and semaphore logic as well as a 15-nsec access time.

The semaphores allow you to set up a complex memory-arbitration scheme in your system software. For example, you can use the semaphores to define eight regions in an SRAM that is serving as a disk buffer. The host processor asserts the semaphores, begins filling the SRAM with data for transfer to disk, and alerts the disk controller to begin reading data.

As the processor finishes filling each region, it releases the corresponding semaphore so that the disk controller can assert the semaphore and begin to read. When the disk controller finishes with a region, it can release the semaphore and allow the host processor to fill the region with additional data. A single block transfer can thus fill the SRAM many times over without forcing either the host processor or disk controller to idle.

The SRAM family offers 8- and 9-bit-wide devices. If your memory system is wider, you can still make use of the semaphore, busy, and interrupt signals without additional logic. The devices are pin-configurable to function as either a master or a slave, allowing you to deal with only a single device's signals when arbitrating memory access.

Dual-port SRAMs

Part No. and size	Price
CY7B134...4k×8	$42.10
CY7B135...4k×8	$48.40
CY7B1342...4k×8	$48.40
CY7B138...4k×8	$63.15
CY7B139...4k×9	$63.15
CY7B144...8k×8	$84.20
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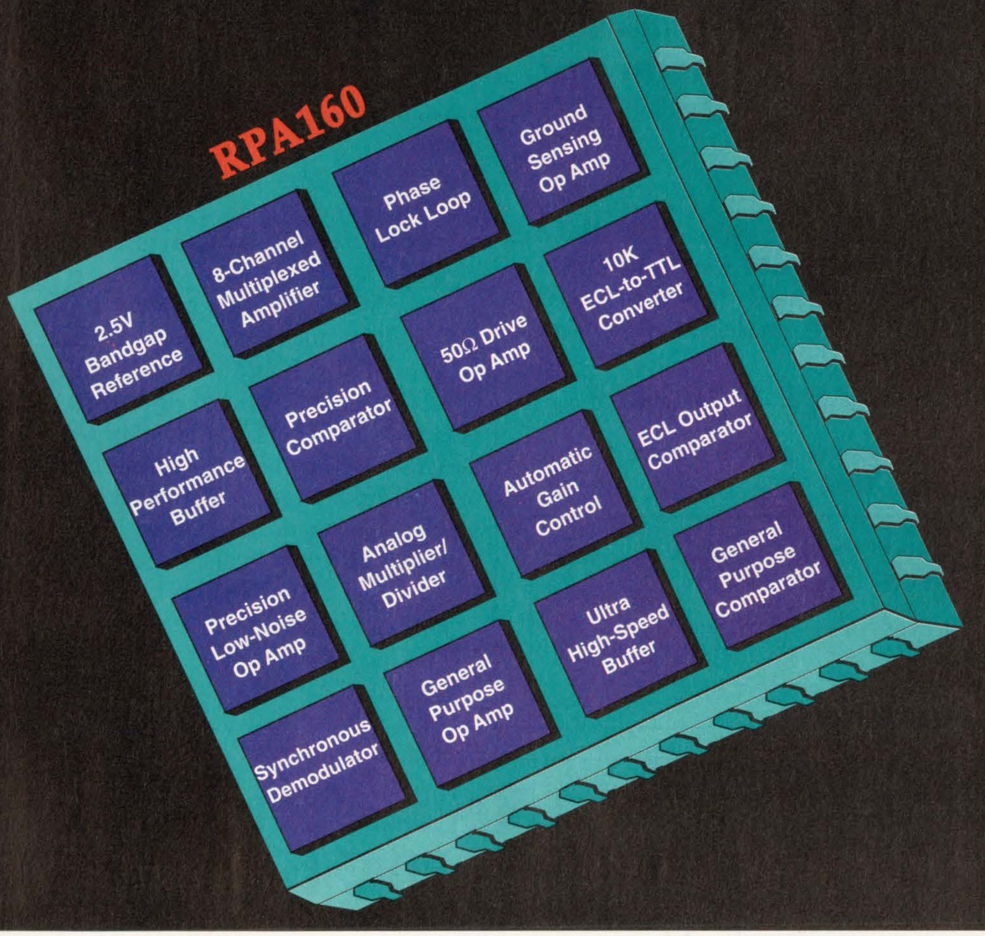

RPA 160
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Bandwidth — 160 MHz
Slew Rate — 700 V/µs

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Supply Sensitivity — 0.2%/V

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CIRCLE NO. 84

Three devices related to the SRAM family are also available. They are the CY7B134, 135, and 1342 4k×8-bit dual-port SRAMs. These devices are stripped-down versions in smaller packages running at 20-nsec speeds. The CY7B1342 offers semaphores without the interrupt or busy signals; the other two offer no arbitration logic.

The four family members with full arbitration logic come in 68-pin LCC, plastic-leaded-chip-carrier (PLCC), or pin-grid-array (PGA) packages. The CY7B134 stripped-down version comes in a 48-pin DIP or LCC package. The other two stripped-down devices come in 52-pin LCC or PLCC packages.

—Richard A Quinnell

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CIRCLE NO. 88

SCPI compiler boosts VXI's speed without requiring complex programs

Although the VXI (VME extensions for instrumentation) standard includes a register-based protocol that is inherently speedy, many users have balked at the difficulty of programming register-based modules. Instead, most users have opted for message-based VXI instruments, which you can usually control as if the instruments were communicating via the familiar IEEE-488 bus. This choice has meant sacrificing the potential VXI instruments have to run much faster than their IEEE-488-based rack-and-stack counterparts.

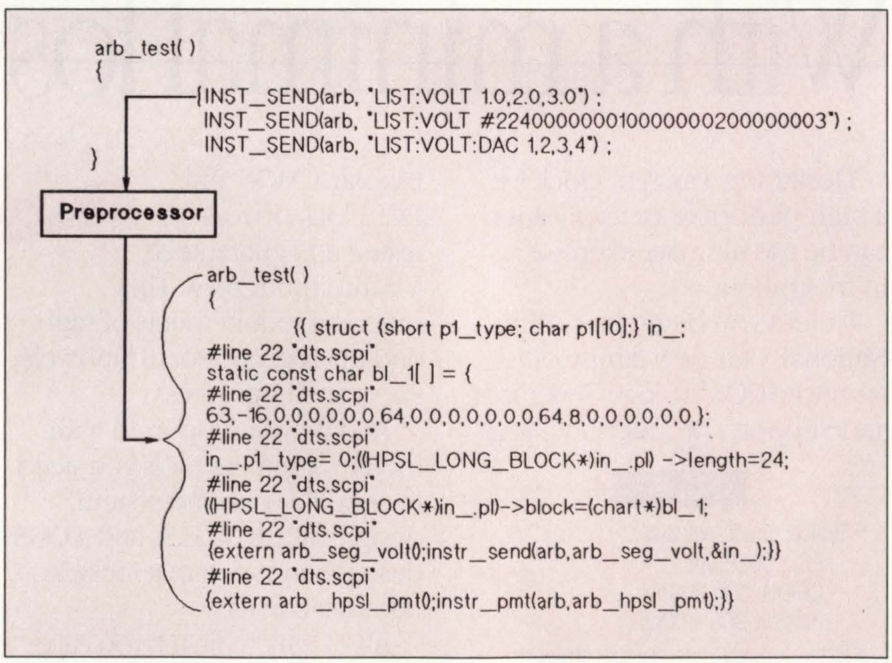
Hewlett-Packard hopes to eliminate this sacrifice with a software package called C-SCPI—for compiled SCPI. Many message-based VXI instruments support the recently developed SCPI (standard commands for programmable instruments) syntax, which is easy to learn and makes short work of porting programs to new instruments. C-SCPI can help you make a smooth transition from message-based to register-based programming without requiring you to sacrifice the fast program-execution speeds inherent in register-based communication. You also won't have to learn the intricacies of communicating with the modules' registers. Using C-SCPI, you write your instrument-control programs in ANSI C, but you program register-based VXI modules in the same way you would program message-based units.

One previous alternative to HP's approach has been to use smart slot-0 controllers that convert messages (including SCPI messages) on the fly into a form that register-based modules can use. However, using any instrument-control scheme that requires interpreting verbose messages at run time incurs a speed penalty. With C-SCPI, a preprocessor converts the SCPI code to ANSI C, from which the compiler produces code that talks to the modules' registers. Because there is no on-the-fly message interpretation at runtime, programs run much faster than the original SCPI commands would run on message-based hardware.

HP has tested the speed of its register-based VXI modules performing certain operations under the direction of code produced by the SCPI compiler and compared it with the speed of various IEEE-488 and message-based VXI instruments performing similar operations. On average, the register-based modules using compiled code run about 30× as fast. Some operations run 150× as fast.

To many people, the term "compiled" evokes images of major debugging hassles. However, by using the vendor's intelligent slot-0 controllers, you can debug your SCPI code in the interpreted mode and obtain immediate feedback about operational problems and your proposed remedies. You submit your SCPI code to the compiler only after you have the code running to your satisfaction in the interpreted mode. Switching from the interpreted to the compiled mode does not necessitate reconfiguring the system; the controller recognizes and interprets the code that requires interpretation and passes register-level commands on to the register-based modules without a speed penalty.

The controllers' ability to handle both SCPI and register-level com-



As this arbitrary-waveform example shows, the compiler lets you program register-based VXI modules in the same way you would program message-based units. A preprocessor converts SCPI commands within a C program to ANSI C, and the compiler produces object code that talks to the modules' registers. The object code runs register-based modules at much greater speeds than the SCPI commands would run message-based units.

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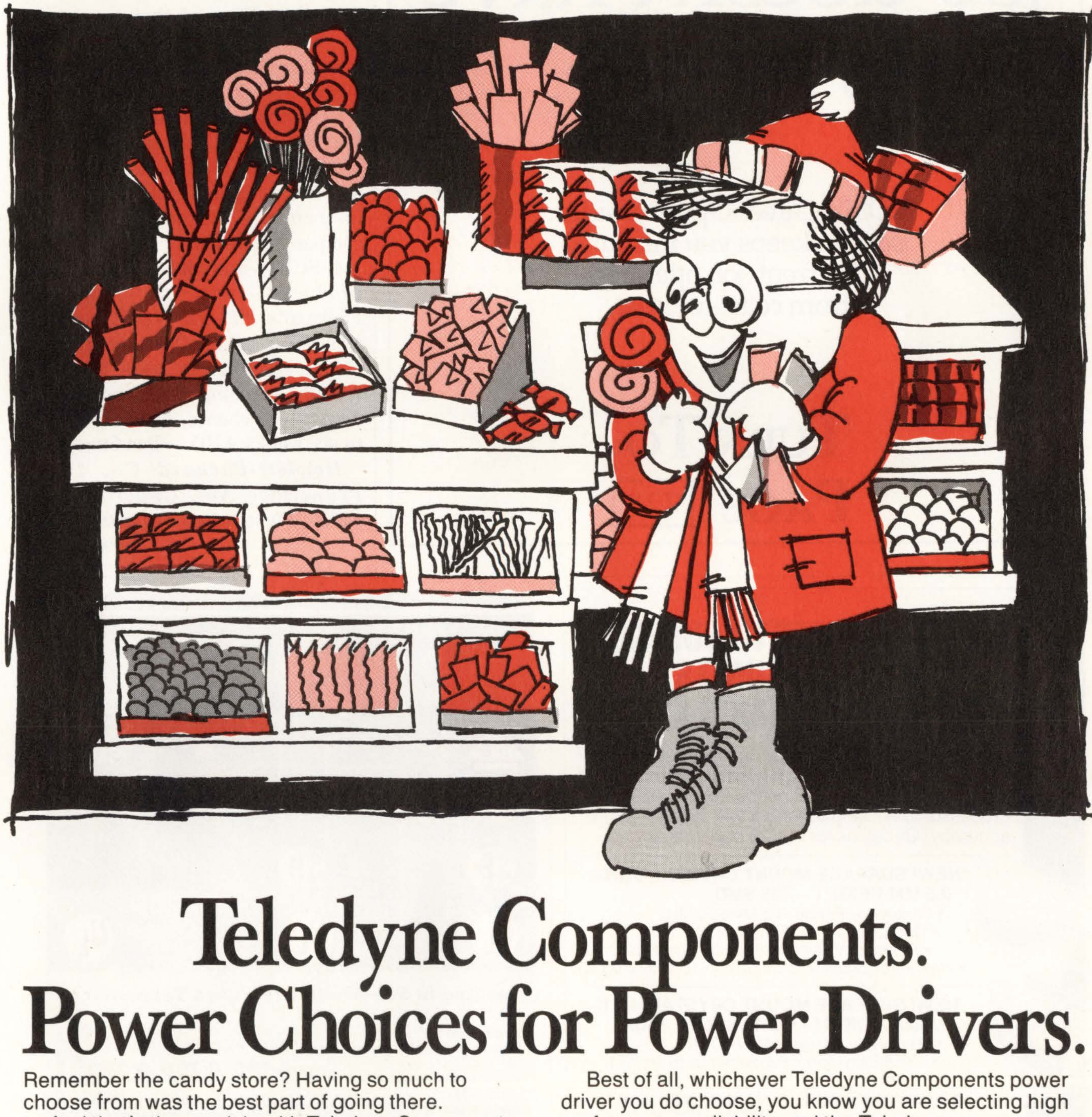

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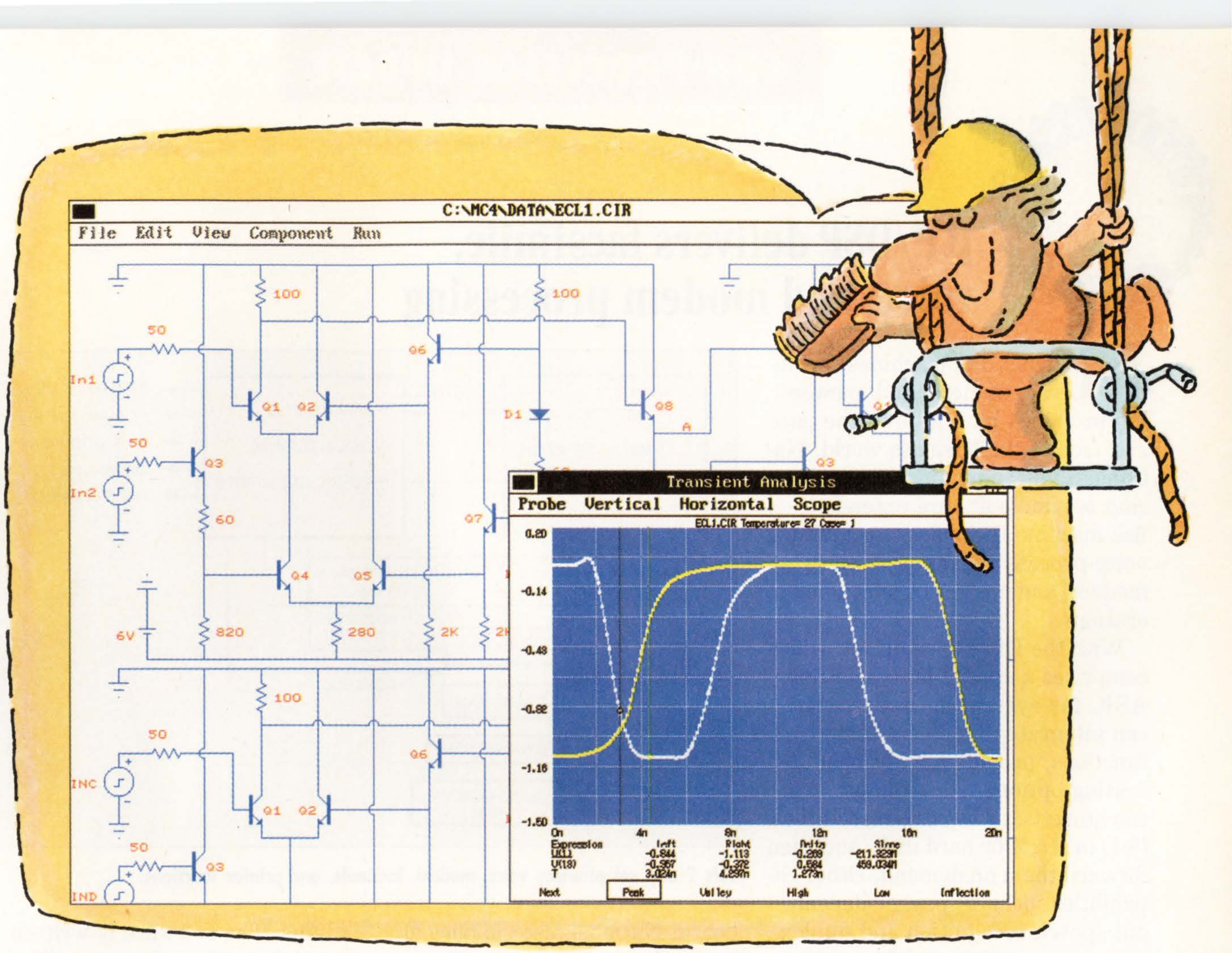
CIRCLE NO. 92

mands gives users another option; they need convert only the time-critical portions of their programs to directly manipulate the VXI modules' registers. Moreover, in systems that mix IEEE-488 and VXI instruments, and even in those that mix message-based and register-based VXI units, the compiler lets a C program control *all* of the instruments, regardless of what company made them.

C-SCPI—and the object code it produces—runs on Hewlett-Packard's HP-UX V/382 controllers. You order the compiler as model E1570A. It costs $2500 to $6600, depending on the instrument drivers you choose. Delivery is four to six weeks ARO.—**Dan Strassberg**

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 734



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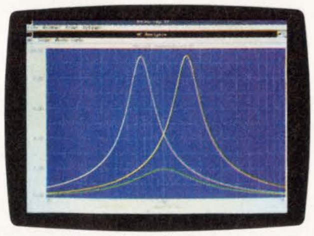

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EDITORS' CHOICE EDN

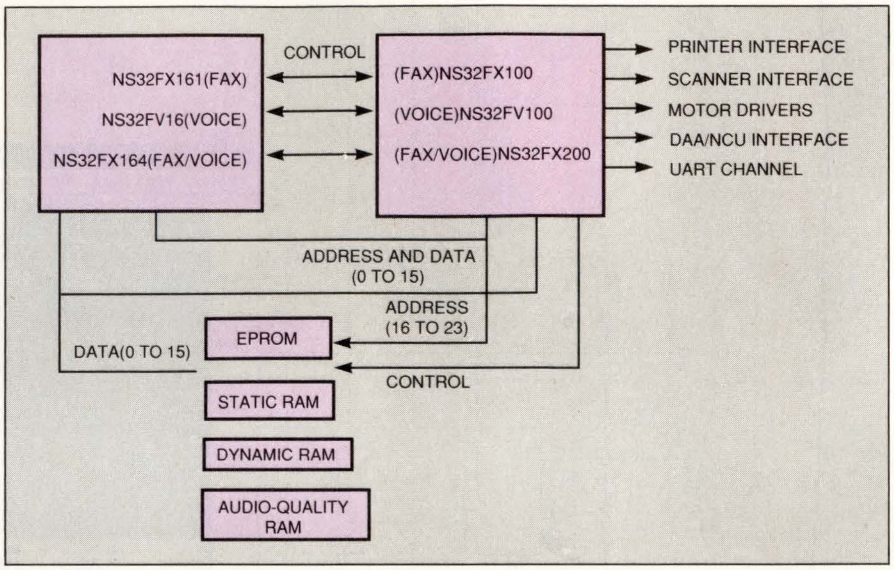
μP/DSP delivers facsimile, voice, and modem processing

Modems, fax machines, printers, scanners, and answering machines have altered the pace and face of the business world. National Semiconductor's Dispatch chip set and software extends office-machine technology, combining voice-processing, fax-processing, modem, and answering-machine operations.

With the Dispatch chip set, which comprises a special processor and ASIC fax-system controller, you can integrate all office-machine functions, providing additional operating options. For example, you can store faxes as compressed files (8:1) in RAM or hard disk, and then forward them on demand. Other capabilities include speaker-dependent speech recognition and duplex-modem operation, enabling users to call in and remotely access their answering machines as well as forward faxes to remote sites.

Dispatch furnishes three chip-set combinations each made up of a 32FX16x fax/modem controller processor and a 32FXx00 fax-system-controller ASIC, which drives system peripherals. The 32FX164/32FX100 combination supports high-end V.17 fax and voice processing (answering machines). The NS32FV16/NS32FV100 supports voice-only processing; the NS323-FV161/NS32FX100 supports fax-only processing.

The chip set's software/hardware combination compresses and holds as much as 30 minutes of voice storage, providing record, play, skip, and erase functions, as well as variable-speed playback and private-mailbox storage. The chip sets include an automatic voice/fax switch, as well as touch-tone generation, voice synthesis, and laser-printer support. A fully integrated office system fits on a 5×4-in., 4-layer board; National also supplies an evaluation board that can be dropped in for prototyping products. Dispatch handles V.17 and V.22bis fax and V.29 low-cost thermal fax.



This 2-chip set provides voice, modem, facsimile, and printer functions.

The chip set includes both run-time and development software for voice, modem, and fax functions. The software is written mainly in C, and source code is available. Low-end chip set costs $45 up (1000) (sample qty).

—Ray Weiss

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-6816. FAX (408) 730-6241. **Circle No. 736**

NS32FX164 fax/modem processor

- 15-, 20-, 25-MHz external clock
- Multiplexed address/data bus: 24-bit address/16-bit data
- 2 execution units: 32-bit CPU (32) 32-bit registers; 2 address machines; 6-Mbyte address space; DSP module processor; 15 registers (in memory); vector instruction set; Display List-processing; Multiply/Accumulate (MAC); automatic X,Y,Z addressing; 2- or 4-kbyte internal RAM
- Data passed to DSP for processing as Display List
- Graphics processing
- Frame buffer support: pixel addressing (linear and X-Y); bitblt operations
- Shares memory space with fax system controller

NS32FX100/200 fax-system controller

- 15-, 20-MHz external clock
- Drives 2 stepper motors
- Supports operator panel
- Duplex UART
- 4 DMA channels
- 16 level interrupts
- Scanner controller, video processor
- Printer controller
- Microwire serial channel (synchronous)
- DRAM controller: as much as 2-Mbyte DRAM; 16-Mbyte SRAM; 512-kbyte EPROM
- Programmable wait states
- 3 timers
- Full-duplex sigma delta codec (telephone interface)

4-bit μC expands peripheral low-power applications

Four-bit microcontrollers (μCs) are single-chip solutions for small low-power applications. They offer enough processor and peripheral variations to minimize external support circuitry, providing a low-cost alternative to more powerful 8-bit μCs. S-MOS's expanded SMC6200 line of 4-bit μCs has a number of key peripherals: dot-matrix LCD drive, twin clocks, external memory access, resistance-to-frequency conversion, A/D conversion, a buzzer driver, and a melody circuit.

Applications for 4-bit μCs like the SMC6200 include portable infrared controllers, thermostats and thermometers, refrigerator- and oven-temperature control, flow meters, utility-meter reading, and smart cards.

Like most 4-bit μCs, the SMC6200 μC is based on a simple accumulator architecture with 4-bit A and B accumulator registers fed through a 4-bit adder. Data paths are 4 bits or a nibble wide, whereas the instruction words are 12 bits wide, providing more program capability. The SMC6200 architecture supports as much as 8k, 12-bit words of program and 4k nibbles of data memory. A program counter increments the program address; two 8-bit index registers, coupled with a 4-bit bank address, simplify program addressing. Program memory is divided into two memory banks of as many as 16 pages, each holding 256 words. Using the two index registers, a program can easily pick up a value from one memory location and move it to another in a single instruction.

The system has more than 108 instruction opcodes; an instruction takes 5, 7, or 9 clock cycles, depending on its complexity. The processor handles as many as 85 levels of subroutine nesting with an 8-bit stack pointer. I/O is memory mapped to ease programming, and the processor supports 15 interrupt vectors.

This μC supports the dual clock architecture developed for the digital-watch market. A 32.78-kHz clock provides the base for low-speed, low-power operation. For higher-speed operations, a 455-kHz clock is switched on for short processing bursts. This clock combination enables devices to run for a long time on low power, yet still do relatively significant processing when needed.

Four-bit μCs tend to lag 8-bit μCs in low-cost development tools, relying mainly on vendor-supplied ICEs and simulators. You can buy or rent an ICE from S-MOS to debug SMC6200 code. For prototyping, a one-time-programmable version of the SMC6200 family will be available by the end of August.

—**Ray Weiss**

S-MOS Systems Inc, 2460 N First St, San Jose, CA 95131. Phone (408) 922-0200. FAX (408) 922-0238. **Circle No. 737**

8052 μC combines 3V power and 16-MHz clock

With Matra MHS's 3V 8052 derivative, you don't have to trade higher clock rates for low power. This microcontroller (μC), a static design, handles power rails

S-MOS 4-bit SMC-6200 μC series

Part number (SMC)	Voltage	Twin-clock option	ROM (×12)	RAM (x4)	I/O	External interrupts	Features	Package (quad flatpack)	Price (10,000)
621A	3V	Yes	4096	208	22	2	Infrared remote-control circuit, analog comparator, LCD driver, watchdog timer	80-pin	$3.50
6215	3V	Yes	4096	488	26	2	Infrared remote-control circuit, analog comparator, LCD driver, programmable timer, watchdog timer	100-pin	$4.62
6244	3 or 5V	Yes	4096	384	32	2	Dot-matrix LCD driver, external data-memory access, watchdog timer	128-pin	$5.21
6246	3 or 5V	Yes	6144	640	44	2	Dot-matrix LCD driver, external data-memory access, watchdog memory	128-pin	$5.79
6248	3 or 5V	Yes	8192	768	44	2	Dot-matrix LCD driver, external data-memory access, watchdog timer	144-pin	$7.43
6251/L51	1.5 or 3V	No	1024	80	12	2	Low cost, resistance-to-frequency converter, LCD driver	64-pin	From $3.10 to $3.28
6266	3V	Yes	6144	1024	40	3	No LCD driver, asynchronous and synchronous serial ports, two analog comparators, watchdog timer	60-pin	$4.56
6282/L82/A82	1.5 or 3V	Yes	2048	144	15	2	Melody circuit, analog comparator, LCD driver	80-pin	From $3.28 to $3.45

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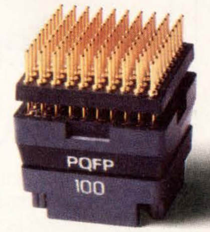
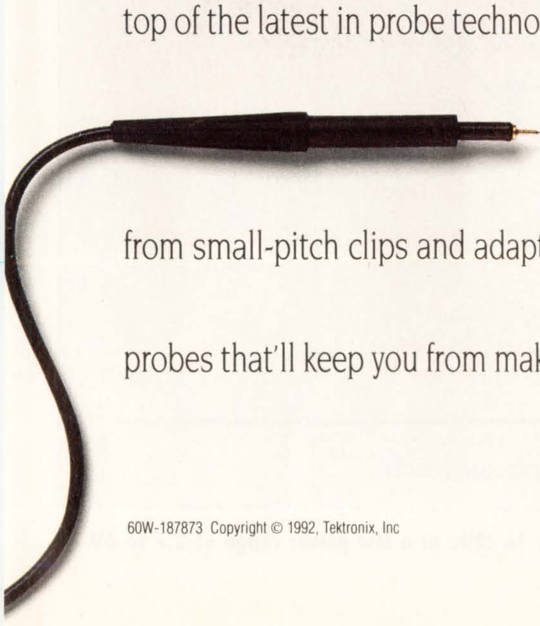




Tektronix
Test and Measurement

CIRCLE NO. 94

to 3V while running at clock rates to 16 MHz (12 external clocks make a typical instruction cycle for an 8051). In addition, the static core allows engineers to lower power consumption further by simply dropping the clock rate—down even to dc.

Matra 80C32µ-L/83/C154µ-L

- 0- to 16-MHz external clock
- 12-clock instruction cycle
- 256-byte RAM
- 8- or 16-kbyte ROM (or ROMless) version
- 64-kbyte instruction-address space 64-kbyte data-address space
- 3 16-bit timers, including watchdog function
- 4 I/O ports: 32 pins
- 2 external interrupts
- Duplex serial I/O
- 2 power-management modes
- PDIP, PLCC, QFP packages
- 80C52/80C32µ-L, $12.50 (1000); 83C154/80C154µ-L, $14.50 (1000)

The 8051 is the "Model T" of the 8-bit µC world: It can be applied in a range of applications. The large base of 8051 development tools and boards has made it extremely popular with designers. The 8051's architecture supports dual address spaces and bit-level data manipulation. The 8051 is supported by Intel, the initial developer, as well as licensees such as Siemens, Oki, Signetics, and Matra MHS.

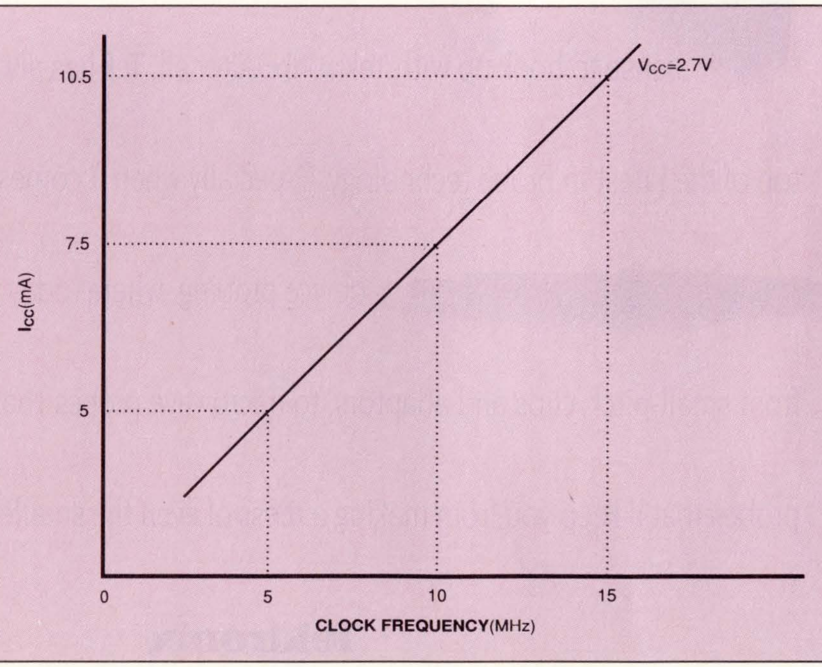
Power dissipation for Matra's 8052-based 80C32L/80C154L is linear. At 2.7V, I_{CC} is 5 mA, 7.5 mA at 10 MHz, and 10.5 mA at 15 MHz. In contrast, a standard 80C32 and 80C154L have an I_{CC} of 27 and 32 mA, respectively, at 5V running at 16 MHz.

The low-power chips are specified for 2.7 to 6V, ±10%. Previous nonstatic Matra chips handled the low-power 2.7 to 6V range but were limited to a 6-MHz clock rate.

The 80C52µ-L is a low-power 80C52 with 256 bytes of RAM and 8 kbytes of ROM. Although the 83C154µ-L is a low-power 83C154, an even later family member, with 16 kbytes of ROM. ROMless low-power versions—the 80C32µ-L and 80C154µ-L—are also available.

—**Ray Weiss**

Matra MHS, 2201 Laurelwood Rd, Santa Clara, CA 95056. Phone (408) 748-9362. FAX (408) 748-0439. **Circle No. 738**



Static 80C52/83C154 µCs run from 0 to 16 MHz at a low power range of 2.7 to 6V.

Oh no. Please, not now. Not with manufacturing release next week.

THE PROTOTYPE DOESN'T WORK.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

THE PROTOTYPE DOESN'T WORK.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

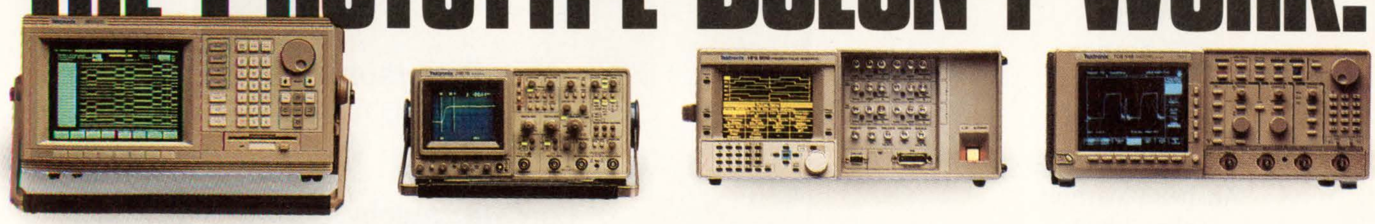
THE PROTOTYPE DOESN'T WORK.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

THE PROTOTYPE DOESN'T WORK.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

THE PROTOTYPE DOESN'T WORK.



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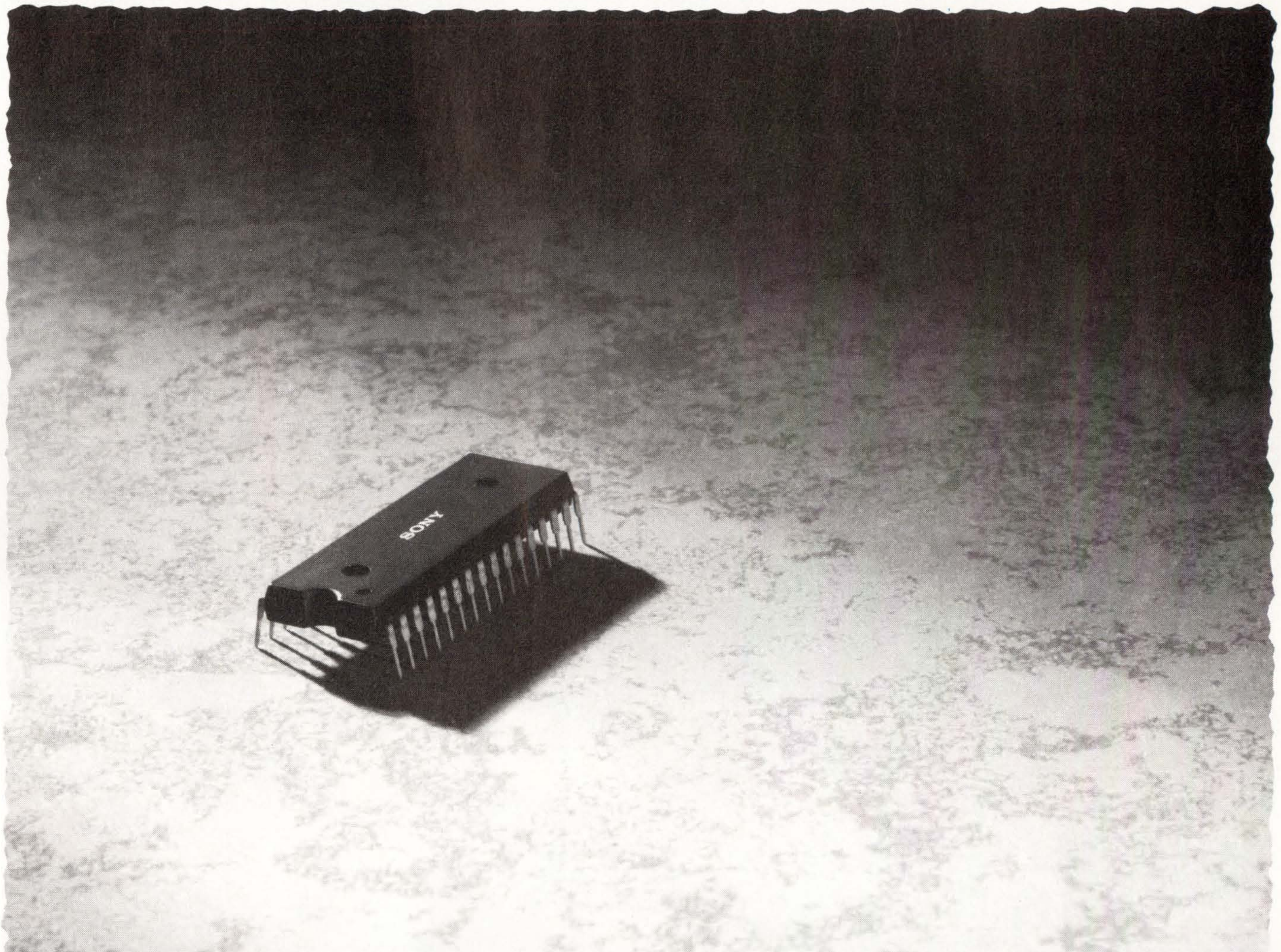

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The Sony 1 Megabit SRAM Family

Model	Speed (ns)	Package	Standby Current (µA)	Special Features
CXK581000P	100/120	DIP 600 mil	12/50	-25˚ - +85˚C
CXK581000M	100/120	SOP 525 mil	12/50	-25˚ - +85˚C
				-40˚ - +85˚C
CXK581100TM	100/120	TSOP	12/50	
CXK581100YM	100/120	TSOP (rev.)	12/50	
CXK581001P	70/85	DIP 600 mil	12/50	
CXK581001M	70/85	SOP 525 mil	12/50	
CXK581020SP	35/45/55	DIP 400 mil		
CXK581020J	35/45/55	SOJ 400 mil		
CXK581021J	47	SOJ 400 mil		
CXK581120J	15/17/20	SOJ 400 mil		
CXK77910J	20	SOJ 400 mil		Sync., 128K x 9

Note: All packages 5V, 32 pin, 128K x 8, unless otherwise noted.

SONY

CIRCLE NO. 93

You can verify a circuit's general operation via simulation, but measuring distortion and settling time to high levels of accuracy is best done from a breadboard. (Photo courtesy Intusoft)

HANDS-ON PROJECT

DOS-based analog-simulation software

"A good circuit designer's output can be increased a hundred fold with a simulator; the inexperienced designer can get into trouble a thousand times faster."
—Fred Ebert, Tatum Labs

"Our success was due as much to the diligence of the engineers who ran the simulations as it was to the power and flexibility of our simulator."
—Andrew Thompson, Spectrum Software

"If we knew before what we know now, we would have breadboarded these circuits."
—Anonymous

The results of eight vendors simulating the same circuits make it clear that behind every good simulation is a very good engineer.

Anne Watson Swager, Technical Editor

Analog simulation holds tremendous promise as a useful design and verification tool, but it still raises doubts among the most demanding skeptics, analog-circuit designers. To take a serious look at analog simulation—its capabilities, limitations, and pitfalls—EDN invited vendors of DOS-based analog-simulation software, including—but not exclusively—makers of Spice, to simulate four circuits whose performance is well documented and characterized from actual hardware measurements. (The study does not include Unix-based simulators that run on workstations.) We asked these vendors to prove that the circuits functioned as designed and then asked them to answer some tough questions about each circuit's performance.

The results of the simulations detailed in the following pages offer some promising surprises but also sound many alarms. Models continue to be the biggest stumbling block to successful simulations. Pre-existing models—those designed by semiconductor manufacturers or by the software vendors—don't necessarily closely match their physical counterparts. The models may exclude certain effects critical to a particular design. Even if you have all the necessary models at your disposal and recognize their shortcomings, getting specific circuit-performance answers from a simulator can require ingenuity and skillful use of software features. Also, simulation may not be the best tool for answering certain questions such as settling time (see **box,** "Ask reasonable questions to get reasonable answers").

In general, the results indicate that any designer running a simulation has to make hard decisions about the simulation's goals. Designers must trade off the time available to spend on a simulation with the accuracy necessary for the results to provide useful information (see **box,** "Editor's analysis"). The experiences

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400/9600 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "SR #468".

of the vendors who participated in this exercise prove that despite using the best simulator on the market with the most comprehensive simulation abilities, the smoothest user interface, and the most comprehensive library of components, behind every successful simulation is a thoughtful and thorough engineer.

Vendors answered the challenge

The circuits we asked the vendors to simulate have been well designed and characterized by two accomplished designers. Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), provided three circuits of his own design: a linearized platinum thermometer **(Fig 1)**, a Wien-bridge oscillator **(Fig 2)**, and a micropower V/F converter **(Fig 3)**. Williams also suggested a fourth circuit **(Fig 4)** designed by Bob Pease, a staff scientist at National Semiconductor (Santa Clara, CA). Pease's circuit is embodied in the 4701 V/F converter module originally manufactured by Teledyne Philbrick and now made by Teledyne Components (Mountain View, CA).

We chose these four circuits for the following reasons. First, all these circuits exist in some form and have been proven as breadboards and in production, particularly Bob Pease's V/F converter, which is a standard product. The three circuits Jim Williams designed have been published, many of them in EDN **(Refs 1 through 6)**. Extensive documentation and performance data is available for each. Second, these circuits span a range of difficulty, from a strictly dc circuit to ac circuits including oscillators and voltage-to-frequency converters.

Third, IC parasitics do not necessarily set the performance limits of these circuits. Instead, those limits are set by the interconnection and interaction of all components. If all the ICs were absolutely perfect, you wouldn't necessarily see much difference in the circuits' performance. Even if the models for the ICs were perfect, you wouldn't necessarily get the answers. Thus, simulating these circuits goes beyond testing the models themselves. It requires an understanding of the various second-order interactions between individual components.

The final reason for choosing these four circuits was curiosity. We wanted to know how difficult

Ask reasonable questions to get reasonable answers

Several of the circuit questions we asked these vendors were too much effort and bother for their engineers to answer using simulators. Specifically, measuring distortion and settling time to high levels of accuracy are questionable simulation pursuits. Many vendors didn't measure the distortion values or plot the waveforms we requested because they thought the exercise was futile. Fred Balistreri of Contec Microelectronics said, "It's not the circuits that were tough to simulate, but some of the questions asked of the simulator were tough to answer."

The vendors said that making distortion measurements using information from the simulation models was futile. Models have a tremendous bearing on the data a simulator produces. For example, macromodels are good for simulation because they're faster than a transistor model would be. However, simplified macromodels don't include many real circuit effects. Anytime you use a macromodel that doesn't include the real device's sources of distortion, you've thrown out one of the overall circuit's distortion components. Only you as the designer will know if these components are the dominant sources of distortion or if they can be overlooked.

Two vendors had essentially the same opinion of the distortion measurements. Intusoft's Charles Hymowitz said, "Measuring the distortion in the Wien-bridge oscillator was a challenge because it was difficult to know whether you were measuring the actual circuit distortion or the numerical inaccuracies of Spice." Anthony Stone of Meta-Software concurred, "The simulated distortion will depend a great deal on how good the models are and the simulation's time and frequency steps. The simulator itself will also introduce some numerical errors."

Hymowitz added that measuring distortion realistically also depends on the type of analysis. He said part-per-million distortion resolutions are entirely possible when using Spice's ac analysis but are not possible when doing transient analysis.

Simplified models and simulators' numerical accuracy aren't the only obstacles to obtaining high levels of accuracy. Time and available system memory also are factors, especially when measuring settling time. For example, looking for settling-time accuracy of 0.01% in a circuit that spans 0 to 10 kHz requires resolving differences of 0.001 Hz. One team ran a simulation with 5-nsec time steps for nearly two days. The team concluded that because of the time required, predicting settling time was probably not a worthwhile exercise. Most of the vendors ultimately suggested that some of these answers are easier to obtain from a breadboard or a quickly designed test rig.

answering detailed questions about these circuits would be for engineers using the various simulators. In some cases, we knew the answers to the questions. In other cases, we didn't know the answers but were interested in what a simulator's prediction would be. Jim Williams knew how much he sweated over each circuit on the bench and wondered how the simulation vendors would fare given the same task.

In a sense, this exercise is an example of reverse engineering: Take a known working circuit and see how closely a simulation can match its behavior. This exercise shows the steps you have to go through to produce accurate results.

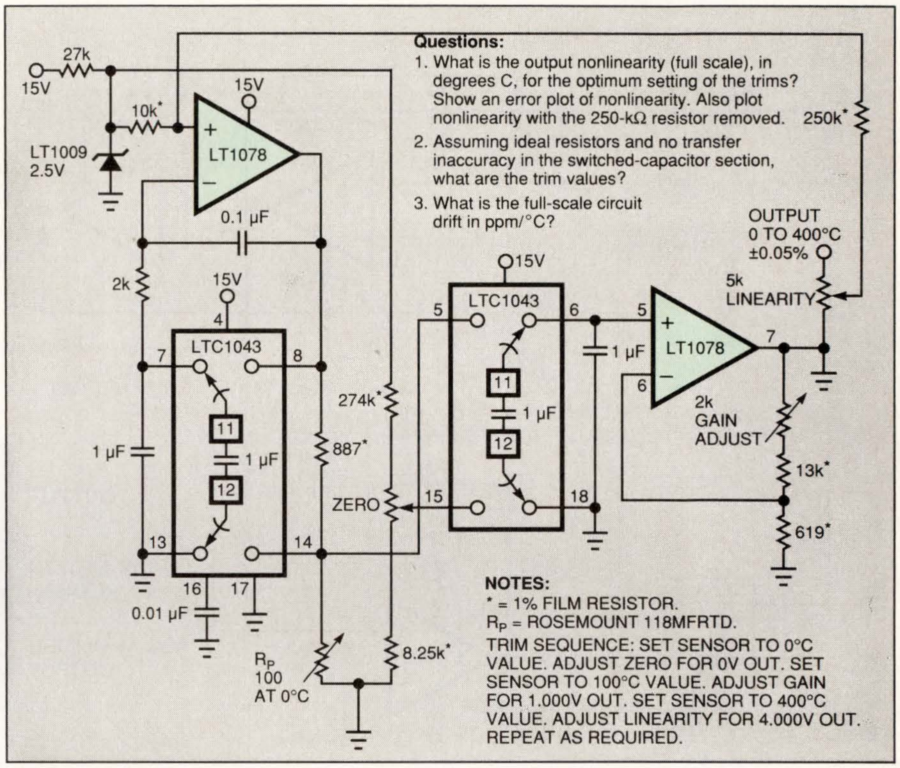

Fig 1—A current source drives one leg of this linearized platinum RTD bridge, which lets the voltage across the RTD sensor vary directly with the sensor's temperature-induced resistance shift. The difference between the sensor's potential and that of the opposing bridge leg is the bridge's output.

More than Spice

Calling this report a Spice story would be misleading. Although six of the eight vendors—Contec Microelectronics, Intusoft, Microsim, Meta-Software, Spectrum Software, and Viewlogic—have Spice-based programs, Dolphin Integration's Smash and Tatum Labs' ECA-2 are proprietary products not derived from Berkeley Spice. However, Smash is Spice-compatible for netlists and sources. Viewlogic Systems has an OEM agreement with Meta-Software and Microsim to include the HSpice and PSpice analog-simulation programs in its Viewsim mixed-mode simulator. For this project, Viewlogic used HSpice for the analog parts of the simulation. **Table 1** describes the simulators and their features, including cost.

Tables 2 through 5 contain the vendors' answers to the questions that we asked about each circuit. Not all vendors simulated all of the circuits. Some vendors concentrated their efforts on only one circuit: Dolphin Integration simulated the linearized-platinum-thermometer circuit **(Fig 1)** only; Microsim simulated each circuit but only answered our questions about the micropower V/F converter **(Fig 3)**. Contec Microelectronics simulated all the circuits except the micropower V/F converter. Meta-Software and Viewlogic split their efforts: Meta-Software's engineers simulated one circuit, Viewlogic's engineers the other three. (Note: All of the simulation files these vendors used are available for downloading on the EDN BBS.)

In many cases, the answers listed in the tables are within factors of 2 or 3 of the real circuits, which we considered an acceptable level of accuracy for this exercise. In other cases, the numbers are off by orders of magnitude. The results were given in a variety of units, which we converted to one common unit for easy comparison.

There are no clear-cut reasons why some answers came close to the real hardware, whereas others are off by orders of magnitude. You can't blame the variations on the simulators, nor can you place the blame exclusively on models. Making the correct assumptions about the circuit is critical. For the most part, vendors accurately predicted the general functions of a circuit, such as frequency range and amplitude. However, distortion and settling-time answers varied widely.

In addition to models and assumptions, time is also a huge factor. The task of performing accurate simulation should not be taken lightly. The vendors spent anywhere from 20 hours on a single circuit to three weeks for all the circuits. Some of this time included waiting for long simulation runs.

Numbers don't tell half the story

Judging the simulation results on a numerical basis alone is a meaningless oversimplification. As An-

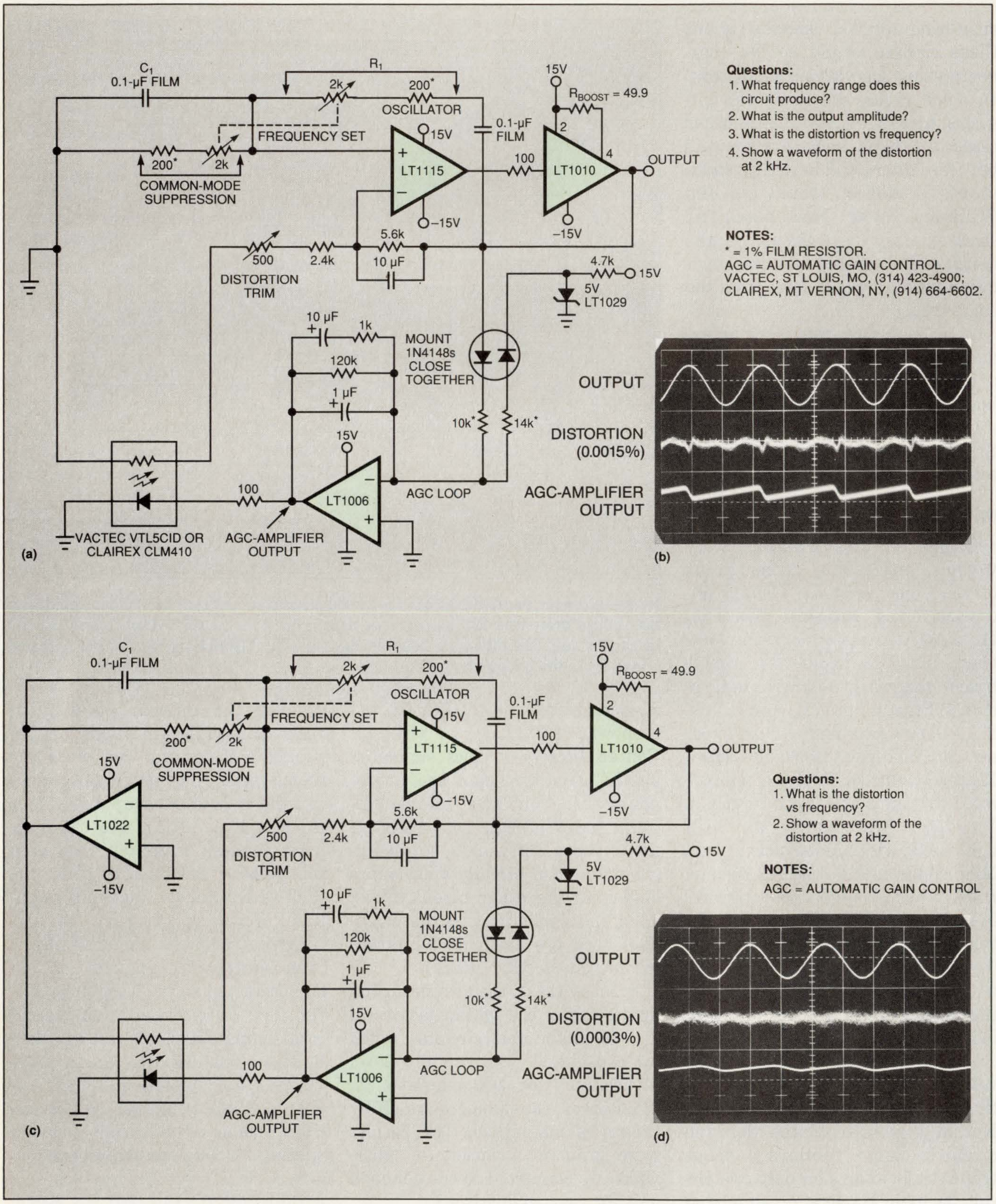

Fig 2—The Wien-bridge oscillator in (a) didn't achieve the designer's desired low distortion level (b). The circuit in (c) includes an additional amplifier, the LT1022. This amplifier eliminates the common-mode swing at the main Wien-bridge oscillator amplifier, the LT1115, thereby reducing the distortion from 0.0015% to 0.0003% (d).

drew Thompson of Spectrum Software reported, "It was quite easy to create each of the four circuits and produce a working simulation. It was much harder to refine the circuit, models, and testing methods to reflect the presumed circuit performance. Our success was due as much to the diligence of the engineers who ran the simulation as it was to the power and flexibility of our simulator."

The real story is how the vendors acquired their answers, what assumptions they made, and what models produced superior results. How close or far the simulations were from reality has everything to do with the methods and models each vendor applied to the simulation.

The simulation exercise illustrates that there are three distinct phases of simulation: thinking about the circuit and making some simplifying assumptions, choosing or creating the necessary models, and actually running the simulation and devising ways for the simulator to indicate a circuit's various performance characteristics. For this exercise, those characteristics include general functionality, linearity, drift, distortion, and settling time. Each of these simulation phases takes a disproportionate amount of time, as you'll see in the following examples.

The vendors' results demonstrate the importance of carefully analyzing a circuit before jumping into the simulation. You may be able to simplify various components to shorten simulation time, and you'll save yourself from countless hours of work that in the end don't add up to much. Intusoft's Charles Hymowitz said that one of the biggest hurdles in this exercise was making assumptions for both the modeling and analysis. Hymowitz adds that these assumptions pervaded every simulation, and although making them was not difficult, it was time consuming because the company verified each assumption with simulation.

For each circuit, certain clues exist that make simplifying the simulation easier. Miss those clues and you can spend time and effort on models or simulation parameters that have little bearing on the circuit's performance. Worse, you can end up on a path to nowhere—as some of these vendors did—and wind up with no realistic answers. Catch the clues and you'll arrive at a reasonably accurate simulation result without too much pain or angst.

For example, two primary clues exist for the linearized-platinum-thermometer circuit in **Fig 1**: The circuit primarily operates at dc, and the switched-capacitor network contributes negligible error. The charge-injection specifications given on the data sheet of the LT1043 switched-capacitor building block combined with the large, 1-μF capacitors used eliminates switched-capacitor-section errors from consideration. Thus, you can model the switched-capacitor block

Table 1—Participating vendors and corresponding simulators

Vendor	Simulator	Description	Price
Contec Microelectronics USA Inc	ContecSpice	Spice 3C.1-based, mixed-level simulator	$4700 to $18,200 depending on options
Dolpin Integration	Smash	Spice 2G.6-compatible simulator with a behavioral language (ANSI C)	$3950 to 4950 (requires Microsoft C 6.X or Borland Turbo C++)
Intusoft	IsSpice with ICAP/3	Spice 2G.6-based simulator	$1481 ICAP/3 includes simulator and numerous options such as schematic entry, model libraries, circuit optimizer, and post-processor.
Meta-Software Inc	HSpice	Spice 2G.6-based simulator	$3500
Microsim Corp	PSpice with Design Center	Spice 2G.6-based simulator	$2450 or $8200 for System 2 or 3 of the Design Center, which packages the simulator with numerous options including analog behavioral modeling. (System 2 includes non-Windows DOS versions; System 3 runs under Windows 3.0.)
Spectrum Software	Micro-Cap IV	Spice-based circuit simulator	$2495 (Includes two simulator versions, model library, schematic editor, waveform review and analysis, and analog behavioral modeling.
Tatum Labs Inc	ECA-2	Proprietary (not a Spice derivative) electronic-circuit-analysis program	$775 (Additional schematic-entry program is $495.)
Viewlogic Systems Inc	Viewsim with Workview	System-wide digital and mixed-signal simulator that includes HSpice for analog circuits	$17,000

Note: These prices don't necessarily reflect the range of packages offered by these vendors, but they do reflect the packages necessary to simulate the circuits presented in this story.

fairly simply. The second Wien-bridge oscillator circuit (**Fig 2c**) has only one difference from **Fig 2a**. That difference—an additional amplifier—is a clue to why the first circuit has higher-than-desired distortion. The additional amplifier eliminates the common-mode swing of the main Wien-bridge oscillator amplifier.

The reference section of the micropower V/F converter (**Fig 3**) provides some clues about that circuit's operation. The first question you should ask is why the designer put nominally high-drift transistors (Q_2, Q_3, and Q_4) in series with precision references (two LT1004s) and a high-drift current source (the LM334). The answer is that some other component or group of components in the circuit drifts the other way, namely Q_5, Q_6, and the 0.001-μF polystyrene capacitor. Again, these clues are a form of reverse engineering, but they highlight the need to think about the circuit, look for circuit clues, and apply those clues to your models and simulation runs.

In addition to looking for simplifying circuit clues, you should think about the types of data you're after from the outset. Keeping your intended analysis type in mind and creating, modifying, and simplifying models accordingly will save you time in the long run. For example, simplifying a switched-capacitor block as a unity-gain amplifier, as some of the vendors did, provides information through a basic dc analysis instead of the cumbersome transient analysis.

Once you've made some preliminary assumptions about circuit operation, you can apply those assumptions to the models you choose or create. Choosing or creating models is the most important aspect of producing accurate and meaningful simulation results. In fact, modeling alone can eat up most of the time you've allocated for simulation.

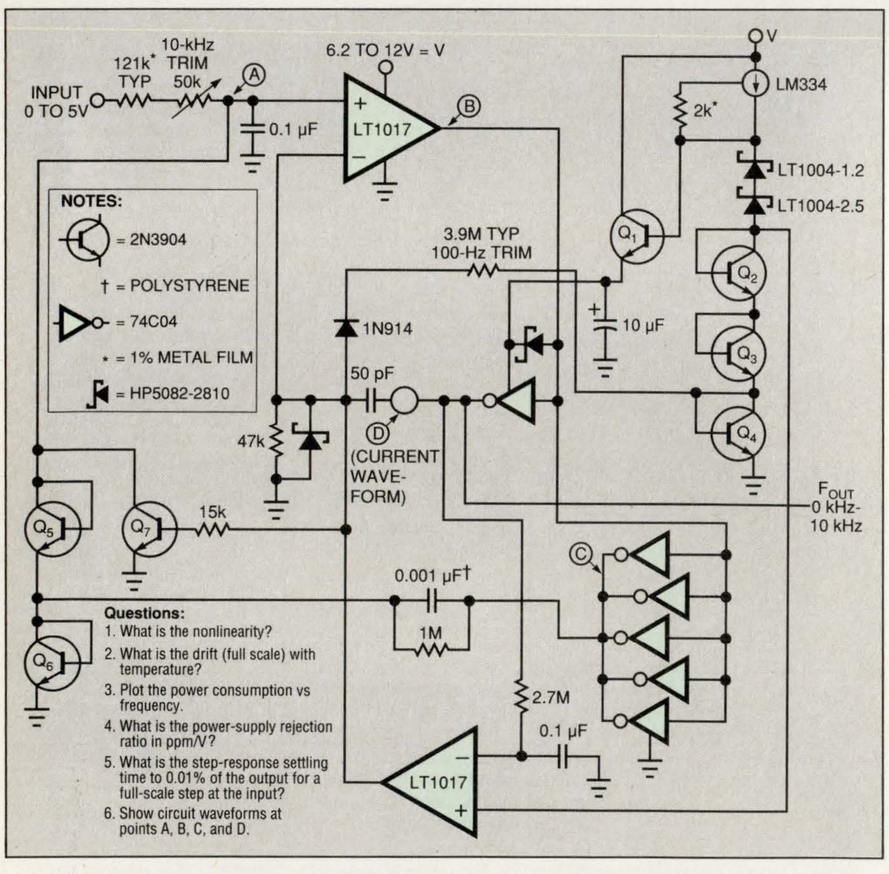

Fig 3—Consuming between 80 and 145 μA, this micropower V/F converter produces a 0- to 10-kHz output from a 0 to 5V input.

Many of the vendors' libraries already contained some of the specified components. In a few rare cases, all models for a circuit already existed. For example, all the necessary models for Bob Pease's V/F converter were in Contec Microelectronic's library. However, having 100% of the models at your disposal is the exception rather than the rule. Some models not already in a simulator vendor's library were available from Linear Technology Corp. Still others had to be created from data sheets.

The vendors' approaches to modeling the same components were strikingly varied. Their approaches teach three important modeling lessons: thoroughly evaluate the circuit and each component's function before jumping in and wasting time on modeling some noncritical component; beware the dangers of misapplying existing models; and understand a model's limitations.

Modeling the switched-capacitor blocks in the linearized-platinum-thermometer circuit initially threw some vendors off balance and illustrates how some initial analysis can save you modeling time. Spectrum Software's engineers initially tried to model the switched-capacitor blocks by emulating their exact function. They first tried using two sets of clock-dependent resistors that switched each 1-μF capacitor from one side of the block to the other. They discovered that using this approach, the output voltage had a long transient associated with it. Simulations of the model were long, and the initial results were not as expected. Something had to be reworked.

The engineers then sat back and

thought about the function of these blocks. Their assessment was that both of the switched-capacitor blocks transfer a differential voltage to a single-ended output with unity gain. By replacing each block with a unity-gain voltage-dependent voltage source, the Spectrum Software engineers achieved predictable circuit behavior and simplified the circuit to a dc problem.

Both the Dolphin Integration and Tatum Labs engineering teams, however, studied the circuit and recognized a clue at the outset. Dolphin engineers recognized that all our questions concerned static characteristics of the thermometer. They assumed no transfer inaccuracy in the switched-capacitor section and replaced the LTC1043 with simple Spice primitives for dc analysis. Tatum Labs engineers, looking at the problem in a slightly different way, recognized that the switched capacitor would draw a negligible amount of current and that this component could be virtually ignored. Thus, they modeled the LTC1043 as a unity-gain amplifier. This model let them use a dc analysis instead of the cumbersome transient run that they would have had to do had they fully modeled the switching capacitors.

Table 2—Linearized-platinum-thermometer results

Vendor	Simulator	Output non-linearity (°C)	Open-loop nonlinearity (°C)	Trim values (Ω)	Full-scale drift (ppm/°C)
Jim Williams	None (breadboard results)	±0.05	2 to 4	Unknown	150 (assume 5 ppm/°C resistors)
Contec Microelectronics USA Inc	ContecSpice	0.021	16.08	R_{ZERO}=21.5k/28.5k R_{GAIN}=1735 $R_{LINEARITY}$=4505/495	151
Dolphin Integration	Smash	+0.046, −0.0924	±4	R_{ZERO}=22.2324k/27.7675k R_{GAIN}=141 $R_{LINEARITY}$=2.9925k/2.0075k	22.9
Intusoft	IsSpice	0.0321	2.71	R_{ZERO}=22.25k/27.75k R_{GAIN}=923 $R_{LINEARITY}$=1.885k/3.115k	NA
Spectrum Software	Micro-Cap IV	+0.068, −0.075	+6.8, −7.5 (approximately)	R_{ZERO}=22.228k/27.772k R_{GAIN}=230.5 $R_{LINEARITY}$=2.992k/2.002k	NA
Tatum Labs Inc	ECA-2	NA	NA	R_{ZERO}=22.226k/27.774k R_{GAIN}=236.75 $R_{LINEARITY}$=3.001k/1.999k	7360
Viewlogic Systems Inc	Viewsim with HSpice	−0.02, +0.1	−15, +10	R_{ZERO}=22.2376k/27.7624k R_{GAIN}=924.611 $R_{LINEARITY}$=3.09654k/1.90346k	700

Note: NA=Not answered.
Trim values listed for (top of potentiometer to wiper)/(wiper to bottom of potentiometer).

Models aren't infallible

The second lesson has to do with misapplying existing models. Because every component needs a model, your first goal is just to fill in the blanks. Many IC models, but not all, are available from semiconductor vendors. Some IC models are also available for downloading from the EDN BBS's Spice Special Interest Group. Even when available, models don't necessarily include all the effects that are important to your particular circuit. Worse, in the drive to have a model for a device, you can easily pick the wrong one. The ensuing simulation certainly won't scream out at you that you've erred, and the results may even look plausible. But you've added a source of uncertainty to your simulation, which makes it less reliable and certainly less accurate.

In many cases, vendors used models that wouldn't be true performance indicators for a circuit just to be able to demonstrate a circuit's general functions in a reasonable amount of time. For example, the Contec Microelectronics team replaced the model of the LT1006 precision, single-supply op amp in the Wien-bridge oscillator with a model of an LF411 JFET-input op amp. The team made the switch because the LT1006-based simulation showed some strange behavior at the op amp's inputs, and the LF411 appeared to work correctly. The frequency-range and output-amplitude numbers looked plausible after the replacement.

However, the one catch is that the LF411 would never work in the real circuit. In the real circuit, the LT1006 is running from one supply rail, and its noninverting input is grounded. Thus, the inverting input also functions at ground. For any op amp to work at ground, its input common-mode range must include ground or, put another way, must be able to swing close to the minus rail. The common-mode range of the LF411 doesn't go anywhere near the minus rail but is 3.5V above it. So, in the real world, the LF411 wouldn't behave like an op amp in this circuit. This case is an example of changing models for the simulation's sake instead of understanding why the model of the actual circuit component doesn't work with the simulator.

Other cases of mistaken modeling involved the LT1017 micropower comparator in **Fig 3.** Because a model for this component isn't available from Linear Technology, vendors used other models having vastly different performance characteristics. For the most part, these vendors ran out of time and wanted to at least demonstrate the circuit's primary function. For example, Viewlogic engineers used an LM339 comparator with a 1-kΩ pull-up resistor to model the LT1017. They knew this replacement would cause the power in the circuit to go way up. However, they thought the replacement was useful to demonstrate the circuit's performance and show how to obtain the power plots.

Intusoft also replaced the LT1017 with a much higher power comparator, the LM393 from Texas Instruments' comparator library. Company engineers attempted to bring the model in line with the 1017's specifications. Their effort produced higher power results than those of the real circuit but is a good example of modifying an existing model to approximate a nonexisting one. To make the modified model, the engineers added a pull-up resistor with a separate power supply and adjusted the 393's reverse transit time, forward transit time, and junction capacitance.

The final modeling lesson is the importance of recognizing a model's limitations. Said Anthony Stone of Meta-Software, "Blindly accepting models is not good—an educated acceptance is the best option because totally regenerating each component for every design takes too much time." No model behaves exactly as its physical counterpart. Unfortunately, knowing which effects are included in the model and which aren't isn't easy to determine. An op-amp model in Bob Pease's V/F converter is an example of this point. When Pease designed his V/F converter he put a diode across the LM301A's compensation pins **(Fig 4)**. The diode prevents the LM301A, which operates as a comparator in the circuit, from drawing excessive current.

Regardless of the model's source, the output stage of most op-amp macromodels doesn't resemble the real device's output stage at all. Thus, using a diode across the compensation pins, which limits current by preventing the output stage from saturating, won't have nearly the same effect on the model as it does in the actual circuit. All the vendors found this statement to be true. The Intusoft team noted that the macromodel didn't have the correct connections or characteristics to handle the benefits that the diode would provide. The team used a generic bipolar model instead of the LM301A model. Contec and Viewlogic engineers took a different tack by installing capacitors of 2 and 5 pF, respectively, across the compensation pins instead of using the diode. Spectrum Software engineers left the compensation pins open.

According to Pease, leaving the pins open or using small capacitors shouldn't make much difference in the circuit's operation. Large capacitors, however, would slow down the amplifier. Contec engineers found the frequency span of the V/F converter to be 0 to 8559 Hz; Viewlogic's team found the span to be 104 Hz to 10 kHz. But Pease suspects that the different capacitor values probably had little to do with the different frequency ranges. More than making the numerical results suspect, this example shows that models are far from exact representations of real parts.

The previous examples illustrate the pitfalls inherent in choosing and using existing models. But the vendors also had to create many models from scratch. To aid in creating new models, vendors used special features of their simulator software or used software tools that create models from data-sheet values.

Table 3—Wien-bridge-oscillator results

Vendor	Simulator	Frequency range (Hz)	Output amplitude (V_{P-P})	Distortion at 2 kHz (Fig 2a/Fig 2c)
Jim Williams	None (breadboard results)	750 to 7500	20	0.0015%/0.0003%
Contec Microelectronics USA Inc	ContecSpice	721 to 7875	18	NA
Intusoft	IsSpice	721 to 7930	28.6	0.00013%/0.000001%
Meta-Software Inc	HSpice	730 to 7300	20	1.54%/1.81%
Spectrum Software	Micro-Cap IV	723 to 7931	18.8 to 19.44	0.002 to 0.185% 0.0023 to 0.0117%
Tatum Labs Inc	ECA-2	723 to 7875	15.5	0.002% (Fig 2a)

Note: NA = Not answered.

The software feature these vendors used most extensively was behavioral modeling. The Dolphin Integration team used five behavioral models in one circuit. Behavior modeling is the attempt to imitate the general function of a device without modeling that device's exact structural details **(Ref 7)**. Op-amp macromodels are a type of behavioral model because they don't replicate every transistor in the actual device.

However, the term "behavioral models" usually refers to models that are more abstract than macromodels. Examples of this type of behavioral model include using one or more of the following to model a component: voltage-controlled sources, polynomial sources, transfer-function and Laplace statements, and look-up tables. Using a look-up table involves entering a series of values into a table. During the simulation, the program compares an expression that you define for this set of values and interpolates between entries.

In this exercise, the vendors made use of voltage-controlled sources, Laplace statements, and look-up tables. For example, the Contec Microelectronics engineers modeled the LT1115 op amp and LT1010 buffer in the Wien-bridge oscillators as voltage-controlled voltage sources and used Laplace transfer-function statements to model the poles. Although the Microsim team didn't completely answer the questions we asked, it proved the overall function of the Wien-bridge oscillator by using a behavioral model for the LED-driven photocell. The team created a table look-up device that modeled the resistance on the output terminals of the photocell based on current flowing into the input terminals.

Software helps create models

In some cases, vendors used software tools to create the necessary models. Intusoft engineers made extensive use of its SpiceMod program ($150 to $200), which helps generate models from data sheets. The company created models of the LT1009 and LT1029 zener-diode-based references by entering values for the zener voltage, zener test current, and power dissipation into SpiceMod. The program estimated the rest of the data-sheet parameters and produced a model compatible with the company's simulator. Meta-Software engineers used HSpice's op-amp generator along with manufacturers' data sheets to create models, such as the LT1115, that weren't available in their component library. The Microsim team used the company's Parts program and data-sheet values to model the LT1017 micropower comparator. Correct delays and a weak current-source pull-up resistor at the output proved critical to the micropower V/F converter's performance **(Fig 3)**.

Vendors ultimately created many models from scratch, and three devices that illustrate the variation in modeling approaches are the RTD (resistive-temperature-detector) sensor (Rosemount part number 118MFRTD) in the linearized-platinum-thermometer circuit **(Fig 1)**, the LED-driven photocell (Vactec and Clairex part numbers VTL5C10 and CLM410, respectively) in the Wien-bridge oscillator **(Fig 2)**, and the 74C04 inverter in the micropower V/F converter **(Fig 3)**.

Creating the RTD-sensor model turned out to be a simple task. Most of the vendors created models directly using the device's temperature-vs-voltage profile obtained from the manufacturer. Dolphin Integration engineers modeled the RTD as a voltage-dependent resistor. Intusoft engineers entered the RTD's temperature-vs-resistance data into a Spice text file. Using this data, they generated a 9th-order polynomial response, the coefficients of which they used to construct a polynomial resistance that would vary with a voltage proportional to the temperature. Thus, the simulator could sweep the temperature of the sensor by sweeping the voltage controlling the sensor's resistance value.

Creating the LED-driven-photo-

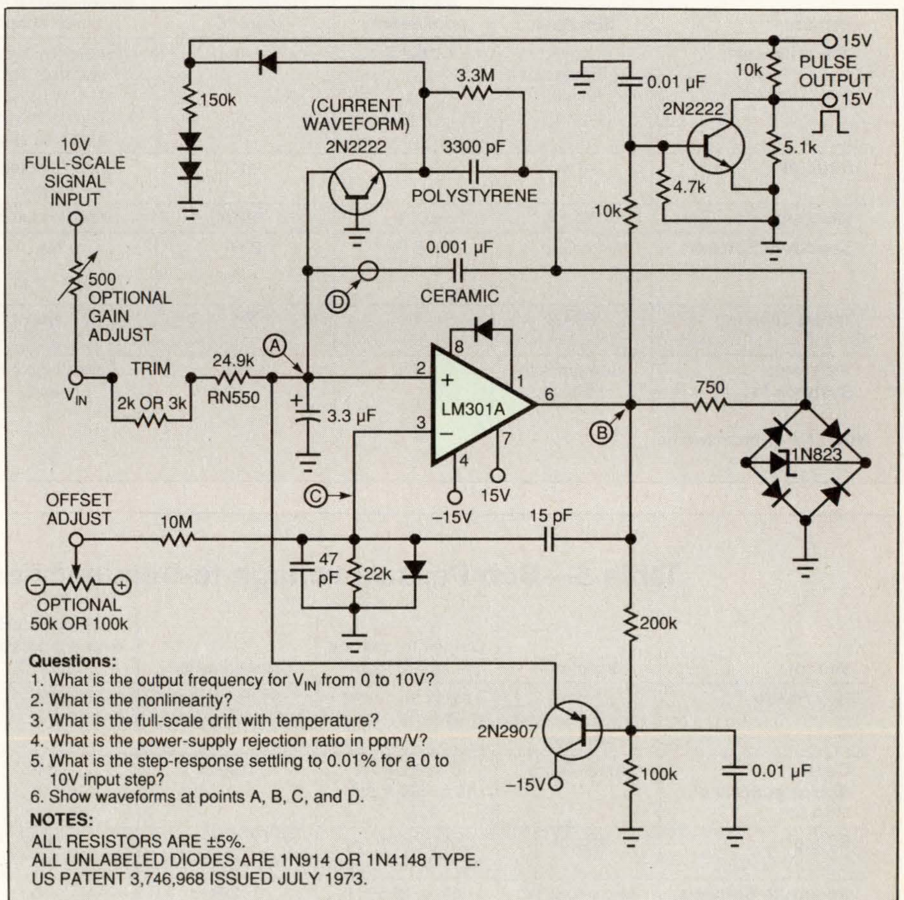

Fig 4—This V/F converter designed by Bob Pease produces a 10-Hz to 10-kHz output pulse train from a 10-mV to 10V signal. The converter features a typical nonlinearity of ±0.008% of full scale. This design is embodied in the 4701, now manufactured by Teledyne Components (Mountain View, CA).

cell model was a little trickier. The Contec engineers modeled the photocell as a piece-wise constant resistor. The engineers didn't think this model was very accurate, but it did let them simulate the circuit in the time domain. Intusoft engineers created a model for the photocell starting with a diode. They added a current-controlled voltage source to convert the diode current into a voltage. They then filtered the voltage to get the correct transient response for the low-resistance state of the resistor. Finally, this voltage controls an analog behavioral model for a switch, thereby implementing a voltage-controlled resistor. Tatum Labs engineers modeled the photocell as a diode in series with a 100Ω resistor, but they weren't confident that this model realistically portrayed the photocell.

The Spectrum Software team modeled the photocell using a table-function source. This source converts input current to output voltage using an input-output table. A resistor whose value is defined to be equal to the table-source output voltage converts the output voltage to a resistance. A standard diode models the input nonlinearity. The team set this diode's saturation-current parameter to 10^{-32} to model the voltage-drop characteristic of the LED input. The diode model's 35Ω series resistance accounts for the incremental resistance of the LED input. The team gleaned the table of values for output resistance vs input current, the voltage drop, and the incremental input resistance from the CLM410 photocell's data sheet.

A simple inverter required a fair amount of modeling effort. The Intusoft team created the 74C04 model by first inputting data-sheet parameter estimates into its

Table 4—Micropower-voltage-to-frequency-converter results

Vendor	Simulator	Maximum nonlinearity	Full-scale drift (ppm/°C)	Power-vs-frequency curve shape	PSRR (ppm/V)	Step-response settling time
Jim Williams	None (breadboard results)	0.02%	40	Increases linearly with frequency (0 kHz=80 μA, 10 kHz=145 μA, 6.5 μA/kHz slope)	40	2 to 3 cycles to 0.25%
Intusoft	IsSpice	0.14%	1420	Doesn't increase linearly	990	76.5 μsec
Microsim	PSpice	0.08%	180	Increases linearly	50	8 msec to 0.01%
Spectrum Software	Micro-Cap IV	0.057%	226	NA	283	Never settled to 0.01%. Settled to final value within 4 cycles.
Tatum Labs Inc	ECA-2	NA	NA	NA	NA	More than a few cycles
Viewlogic Systems Inc	Viewsim with HSpice	1.5%	1100	Doesn't increase linearly	280	Output settled within one cycle

Note: NA=Not answered.

Table 5—Bob Pease's voltage-to-frequency-converter results

Vendor	Simulator	Output frequency (0 to 10V input)	Nonlinearity	Full-scale drift with temperature (ppm/°C)	PSRR (ppm/V)	Step-response settling time (to 0.01%, 10V step)
Bob Pease	None (production-unit results)	10 Hz to 10 kHz (0.01 to 10V input)	±0.008% typ ±0.05% full scale	100	3300	1 or 2 cycles of new frequency plus 20 μsec
Contec Microelectronics USA Inc	ContecSpice	0 to 8559 Hz (0 to 10V input)	0.95%	~140	3700	No more than 3 cycles
Intusoft	IsSpice	2.4 to 8346 Hz (0.05 to 10V input)	0.037%	~6600	10,372	429 μsec (approximately 4 cycles plus 20 μsec)
Spectrum Software	Micro-Cap IV	1856 to 9266 Hz (2 to 10V input)	0.0294%	~75	1500	Within 3 cycles
Viewlogic Systems Inc	Viewsim with HSpice	104 to 10,000 Hz (0.1 to 10V input)	1%	~2000	5490	Output settled within one time period

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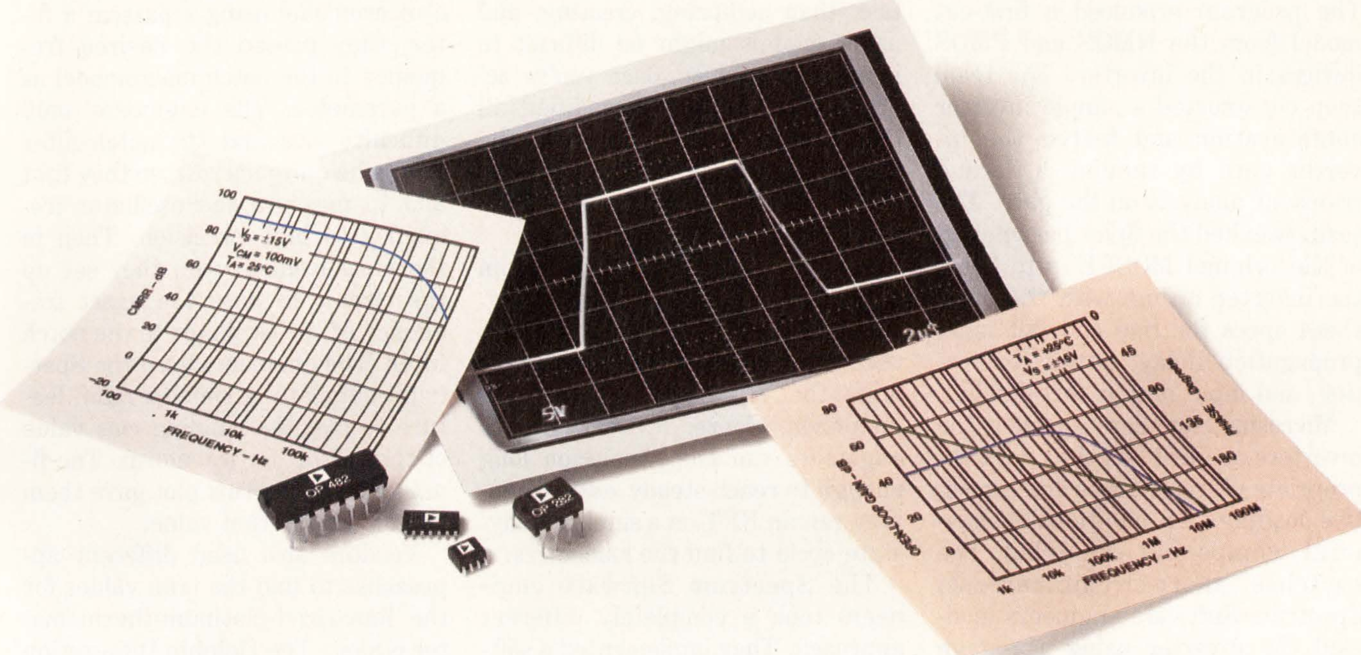

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SpiceMod spreadsheet program. The program produced a first-cut model from the NMOS and PMOS devices in the inverter. The team then constructed a simple inverter configuration and tested the inverter gate by running a dc and transient analysis on the gate. The team tweaked the Spice parameters of the original MOSFETs to bring the inverter in line with the data-sheet specs for rise and fall time, propagation delay, power dissipation, and input/output thresholds.

Microsim engineers modeled the inverters as ideal switches with appropriate on-resistances and capacitive loading. An additional behavioral component modeled the switches' short-circuit current. Spectrum Software engineers modeled the inverter using a 1-stage CMOS configuration. They decided that one stage was sufficient to isolate the voltage-reference branch from the feedback capacitors. And the Viewlogic Systems team modeled the inverters with piece-wise-linear look-up tables and input/output loads.

At this point, a more monumental task than acquiring, creating, and using models might be difficult to imagine. However, once you've acquired, created, and modified all the models, you've got to face the third step in simulation: devising tests for and running the simulation.

Obtaining specific answers from a simulation can require creativity. For example, different vendors used different approaches to determine the Wien-bridge oscillator's distortion. Contec Microelectronics engineers ran the simulation long enough to reach steady state. Then, they ran an FFT on a single steady-state cycle to find the harmonics.

The Spectrum Software engineers took a completely different approach. They implemented a software-based distortion analyzer to simulate the distortion produced by the Wien-bridge circuits. They put the oscillator output through a notch filter tuned to the oscillator frequency. The notch filter removed the fundamental leaving only the residual distortion. The engineers implemented the filter as a macromodel using a passive π filter; they passed the desired frequency to the notch macromodel as a parameter. The engineers' only difficulty was that the notch filter had to be quite narrow, so they first had to measure the oscillator frequency to high precision. Then in the measurement run, they set up the circuit to pass the exact frequency of the oscillator to the notch filter. The engineers used the Spectrum simulator's rms-operator feature to plot the running rms value of the distortion waveform. The final value of the rms plot gave them the final distortion value.

Vendors also used different approaches to find the trim values for the linearized-platinum-thermometer circuit. The Dolphin Integration team developed a set of behavioral modules that automatically looked for the best set of trim values. During one dc simulation, the simulator accomplished the trim procedure outlined by Jim Williams.

Intusoft engineers used a parameter-sweeping feature to nar-

Participating manufacturers of DOS-based analog-simulation software

For more information on the circuit simulators and simulation techniques described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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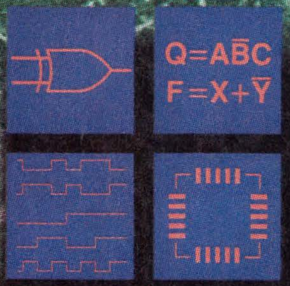

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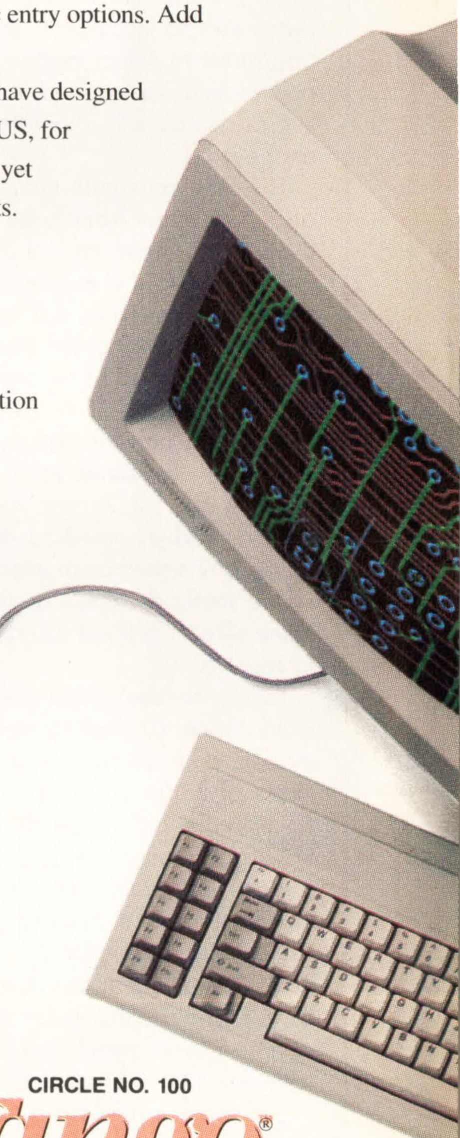

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row in on the correct trim values after following the outlined calibration procedure described in **Fig 1.** They stepped the value of the gain resistor from 0 to 2 kΩ in 100Ω steps and optimized the value for the linearity resistor at each step. The objective was to linearize the output-voltage-vs-temperature curve. The Intuscope program plotted the output voltage vs temperature, performed a first-order polynomial regression on the curve, and minimized the rms error. The results yielded the optimal linearity-resistor value at each step of the gain resistor, from which the engineers selected the best pair.

Editor's analysis

The outcome of this series of simulations left me with both positive and negative impressions. At times, the simulations came extremely close to predicting the real circuits' performance. At other times, the vendors' efforts seemed incomplete and flawed, and the vendors appeared to select models hastily. However, the companies that participated in this exercise have competitive pressures and expended much effort to get as far as they did.

The time pressures the companies' engineers faced are no different from those of any designer who faces a deadline. Many ran out of time to do their simulations justice. And if the engineers seemed to select models hastily at times, they did so to prove the circuit. Given more time, they could have tweaked the models to provide the level of accuracy necessary to answer all our questions.

The trials and tribulations the engineering teams endured are the same you'll face when you attempt to simulate a circuit. Even if you're using the best simulator on the market, one fact remains: Faulty methods will cause any simulator to produce faulty results. But using sound methods won't assure you perfection because some effects are just too difficult for today's simulators to resolve.

Failing to use good engineering judgment—especially when a simulator tempts you to place faith in models and software—can lead to trouble fast. Fred Ebert of Tatum Labs made this point most succinctly, "Simulators aid—they do not replace—solid design skills, good judgment, and experience."

Up front, you'll have to make decisions about your expectations and the time you're willing to spend simulating. A half-hearted effort may prove the concept of your circuit, but it won't take you much further than that. If you're striving for any sort of simulation accuracy—a close correlation between simulation and reality—you'll have to pay close attention to many details.

Simulation involves understanding the circuit and your goals for the simulation, making first-order approximations and assumptions, matching or creating models compatible with those approximations and assumptions, and properly using or manipulating your simulator to give you the answers you want. This process isn't always linear and can require multiple iterations.

Finally, you have to analyze the answers using common sense and acknowledge that any of the simulated "answers" can be off by a factor of 2. Differences between a simulation and a breadboard that span orders of magnitude are the errors you're trying to avoid, not factors of 2 or even 3.

Throughout simulation, vendors may supply varying amounts of support. The vendors are software experts but not necessarily circuit-design experts. Nonetheless, technical support for both evaluation and any future questions you might have will be important to your simulation success.

The vendors' results show how easy it is to get hung up on some part of the simulation that has little bearing on the actual circuit's performance. Constantly evaluating whether simulation is the right tool to provide the necessary answers will save wasted simulation time in the long run. Jim Williams furthered this point by saying, "Good engineers should always question the tool, whether its an oscilloscope, connector, or simulator."

The continued value of some sort of breadboarding is also apparent from this exercise. Tatum Labs' Ebert added, "Simulation allows many 'what if' tries, but breadboarding can truly prove the 'how come' of the overall circuit and provide important details of the individual components." Charles Hymowitz of Intusoft said that his team could have obtained more accurate results if it had access to breadboards—a strategy his company also recommends to its customers.

In some cases, breadboarding a circuit to look for detailed performance aspects after you've simulated the circuit's general operation makes sense. For example, the vendors didn't have much trouble verifying the general operation of each circuit, but they did have trouble answering questions, particularly determining settling times to 0.01%. If you're looking for this kind of accuracy and precision, simulation isn't a timely and practical way to get those answers. The engineer who understands the circuit and surrounding system has to decide what risks lie in trusting the simulation alone.

DOS-BASED ANALOG-SIMULATION SOFTWARE

Devising models and test procedures took most of the engineering teams' time. The teams didn't report much difficulty in the mechanics of running the simulations. Just a few cases of nonconvergence, or the potential for it, required attention. For example, convergence was a problem for Spectrum Software's simulation of the micropower V/F converter. The circuit did converge when the company's team added initial-conditions statements on three nodes: the input, the output, and the voltage-reference capacitor.

In other cases, initial conditions had to be saved from one run to use in a second simulation. Also, in some cases, oscillators had to be kick-started.

Don't allow all defaults

In all simulations, the vendors carefully constrained the time steps (the incremental movement in time during which the simulator attempts to solve the circuit) and often extended the values of various Spice ITL numeric-control options to allow the circuit more chances to converge. For example, ITL4 sets the limits of the upper iteration of the time step. If the program doesn't converge to a solution in ITL4 iterations, the program discards the current time point, shortens the time step, and attempts a new solution. By changing ITL4 from its default value of 10 to 100, many vendors gave their simulation runs more time to converge.

Choosing the maximum time step requires thinking about the test requirement of the circuit. Measuring certain characteristics to high levels of precision demands that the time step be within the same precision. We asked vendors to measure the 10-kHz micropower V/F converter's settling time to 0.01%. To make this measurement, the time-base resolution of the simulations had to be no larger than 0.01% of the output period to obtain meaningful settling-time results. The Spectrum Software team set the maximum time step to 0.01%×(1/10 kHz)=10 nsec.

To aid convergence of the Wein-bridge oscillators, Meta-Software engineers set the maximum change in node voltages, the dc parameter, to 5.0; the internal pivoting algorithm setting to 1; and DELMAX, the maximum time step, to 4 μsec. The Intusoft team set the parameters ITL1 and RELTOL to 400 and 0.003, respectively, to speed the Wien-bridge circuits' dc- and transient-analysis convergence. ITL1 sets the limit of allowed iterations for convergence during a dc operating-point calculation. RELTOL sets the relative error tolerance for voltage and current convergence. A solution must converge within the percentage equal to RELTOL of the previous value of voltage or current.

Simulated oscillators often have trouble starting up. Spectrum Software's Wien-bridge oscillator required a long start-up time to reach the initial conditions for a measurement. Micro-Cap IV saved the final conditions of the start-up run in a disk file for use by the measurement run as initial conditions. To initialize the Wien-bridge circuits, the Intusoft team added a bias voltage in the ground leg of the C_1-R_1 network. This voltage turns off at start-up to give the circuit an initial transient. The team placed another pulse source in series with the compensation capacitors in the control circuitry and adjusted the pulse's value to get approximately the cor-

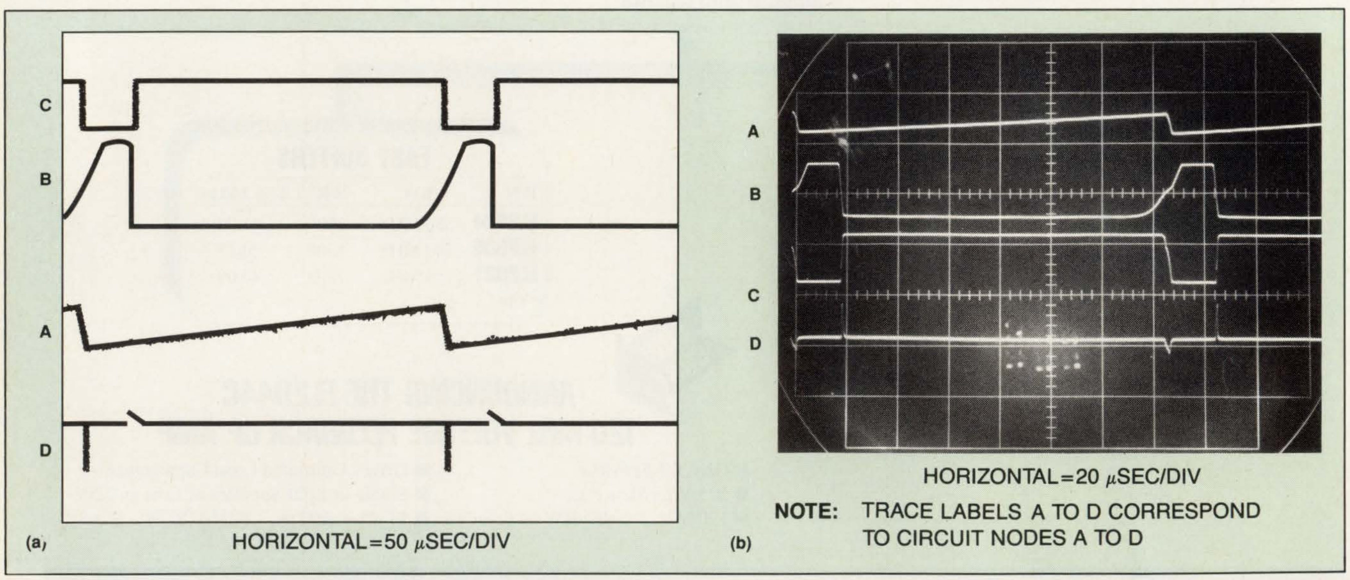
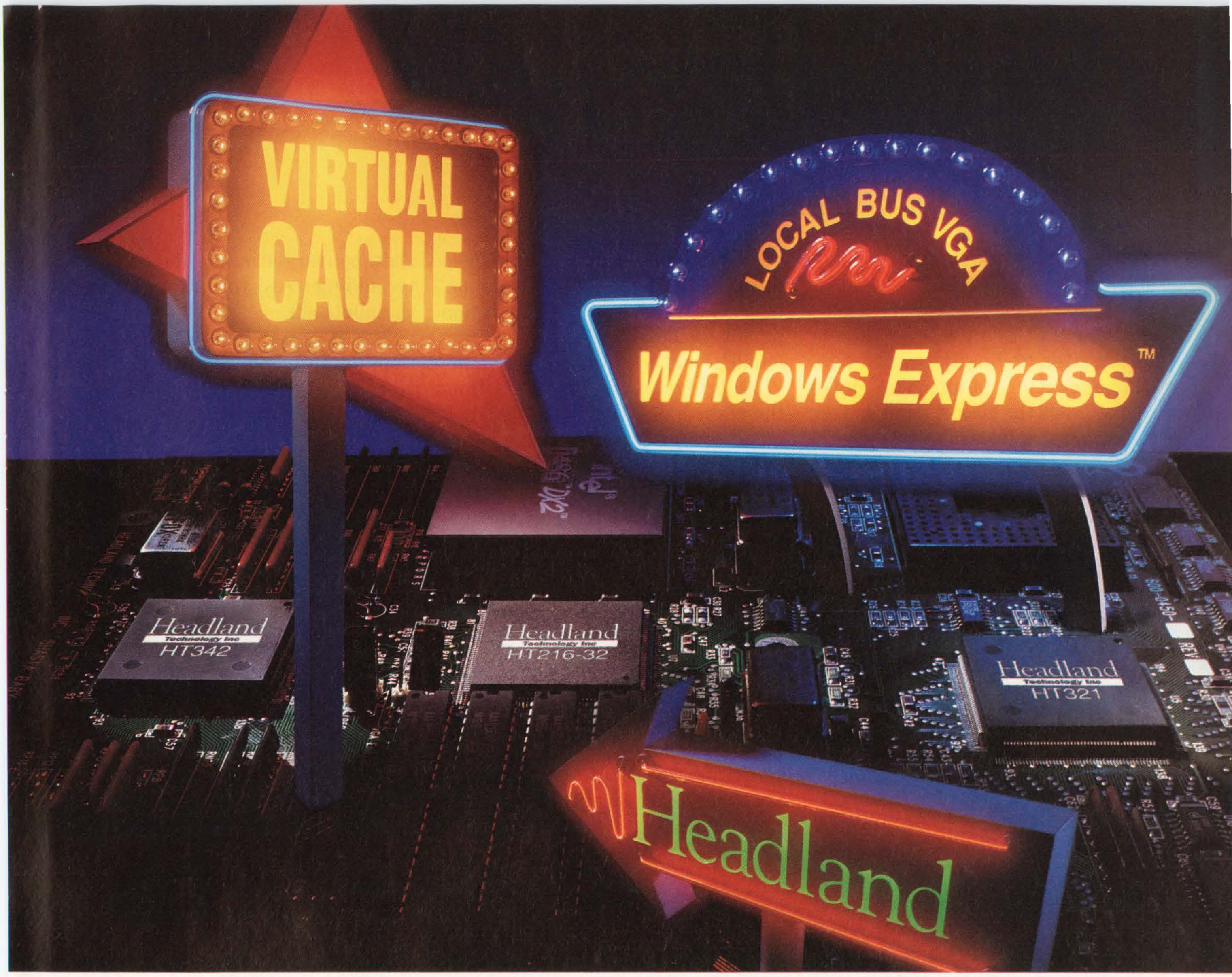


Fig 5—Trace B of Tatum Labs' simulation of the micropower V/F converter (a) is in close agreement with trace B of the scope photo taken of the actual breadboard (b). Traces A to D correspond to circuit nodes A to D in Fig 4.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rect initial control current to minimize the required start-up time. The Intusoft team also added a voltage source to Bob Pease's V/F converter after finding the circuit's initial operating point. The pulse source helps the circuit immediately come to a stable oscillating state.

Despite the difficulties associated with creating the models and simulating the circuits for this exercise, certain surprises point to the potential of simulation. In some cases, the simulation waveforms came extremely close to those of the actual circuit. Tatum Labs' waveforms of the micropower V/F converter **(Fig 5)** show close agreement with those of the working circuit. The comparator's output waveform (trace B) is especially close to the real thing.

While simulating the same circuit, Microsim engineers discovered the existence of a long-settling-time tail. They saw that the output apparently settles within a couple of cycles of its final frequency. When they zoomed in on this tail and individually measured the time period of each cycle after the input step, they saw that the frequency did indeed jump close to 10 kHz within two cycles. The engineers also saw, however, that the output continues to settle and indeed varies by about 20 Hz over approximately 80 cycles. This settling caused considerable frustration in trying to simulate the circuit because the engineers initially thought the tail was a simulation artifact. After reviewing the circuit, however, they came up with a valid explanation. Essentially, they surmised that the emitter voltage of Q_1 asymptotically approaches its final value, which is approximately 20 mV below its starting value.

Many vendors discovered the Wien-bridge oscillator's high sensitivity to loop gain and likewise the control current. According to Jim Williams, this circuit does indeed operate at the edge of stability, which provides the best distortion performance. The Intusoft team found that the circuit zeros of the Wien-bridge oscillator flipped from the right half plane to the left half plane for just a small increase in control current. Typically the circuit would be unstable for a control resistance of 299.96Ω and would become very stable when the zeros moved to the left half plane when the resistance was increased to 299.993Ω.

Meta-Software engineers also found that the bridge circuits were extremely sensitive to changes in the loop gain. Eventually, they chose a distortion trim resistance of approximately 300Ω for stability. Spectrum Software engineers discovered that the Wien-bridge circuits produce stable oscillation only if the dc gain of the oscillator is precisely 3.0.

Perhaps the most dramatic example of instability in this oscillator was the "squegging" problem Tatum Labs' team encountered. (Squegging, which rhymes with pegging, refers to oscillations that occur within a modulating envelope.) The team's first simulation with a time step of 100 μsec and a 386 processor lasted more than an hour and required 640 kbytes of hard-disk space. An extended run, which lasted overnight, did not show convergence, nor did a run after adding a resistor in parallel with the photocell.

All of these insightful results came after many simulation trials. None of the answers came easily. Each vendor made use of many of the features unique to its software. Although these features clearly made performing some parts of the simulation easier, the implication of this exercise is that any reasonably accurate simulation requires extreme diligence on the part of the engineer running it. Although software tools can provide amazing insight into the way circuits function, that insight is a direct result of an engineer's perception of a circuit, selection of the right models, and manipulation of a simulator to provide reasonable answers to reasonable questions. EDN

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Acknowledgments

Much thanks goes to Jim Williams not only for offering the use of three of his circuits but for being available to answer vendors' questions, provide models and data sheets, and help this editor (who dabbled in analog design in a former lifetime) analyze the results. Also, many thanks to all the vendors and their software/hardware engineers who made time to participate in this project: for Contec Microelectronics, Fred Balistreri and Raj Raguram, PhD; for Dolphin Integration, Christian Dupillier; for Intusoft, Charles Hymowitz, Matthew Archambault, and Larry Meares; for Meta-Software, Anthony Stone; for Microsim, John Horan and Graham Bell; for Spectrum Software, Andrew Thompson, James Wilburn, and John D Szymanski; for Tatum Labs, Colin May (Polytechnic of Central London).

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CIRCLE NO. 107

Analog Technology

Circuit options boost photodiode bandwidth

Jerald Graeme, Burr-Brown Corp

The number of circuit-design techniques you can use to widen the bandwidth of photodiode circuits is surprisingly large. Even the way you bias the detector can have a profound effect on the frequency response and noise.

Photodiodes' large capacitance severely restricts the bandwidth of basic photodiode circuits. Three methods overcome this restriction: signal isolation, photodiode bias, and photodiode bootstrapping. An op amp connected as a current-to-voltage (I/V) converter provides signal isolation; it removes the signal voltage from the photodiode and prevents the diode's capacitance from shunting the signal away from the amplifier.

Reverse biasing the photodiode, a function readily performed with the I/V converter, reduces the effect of the diode capacitance and improves the circuit bandwidth. Although such bias introduces significant offset and noise errors, the common-mode rejection of the converter's op amp can remove most of them.

Bootstrapping the photodiode increases the bandwidth in much the same way that using the I/V converter does. Bootstrapping again removes signal voltage from the photodiode capacitance. In addition, the bootstrap configuration reduces phase compensation requirements. This reduction gives the bootstrap circuit a bandwidth advantage when photodiode capacitance is low. Finally, bootstrapping combines with I/V conversion to make the bandwidth immune to the effects of the photodiode capacitance.

The op-amp I/V converter of **Fig 1a** removes the signal voltage from the photodiode capacitance. The op amp and its feedback resistor translate the diode current to a buffered output voltage. Added to the figure is a feedback capacitance, C_L, which provides phase compensation as described later. An ideal amplifier holds its two inputs at the same voltage. In **Fig 1a**, such an amplifier would hold the signal voltage across the photodiode (and across the diode capacitance) to zero. The op amp transfers the signal voltage to its output and isolates the signal voltage from the diode.

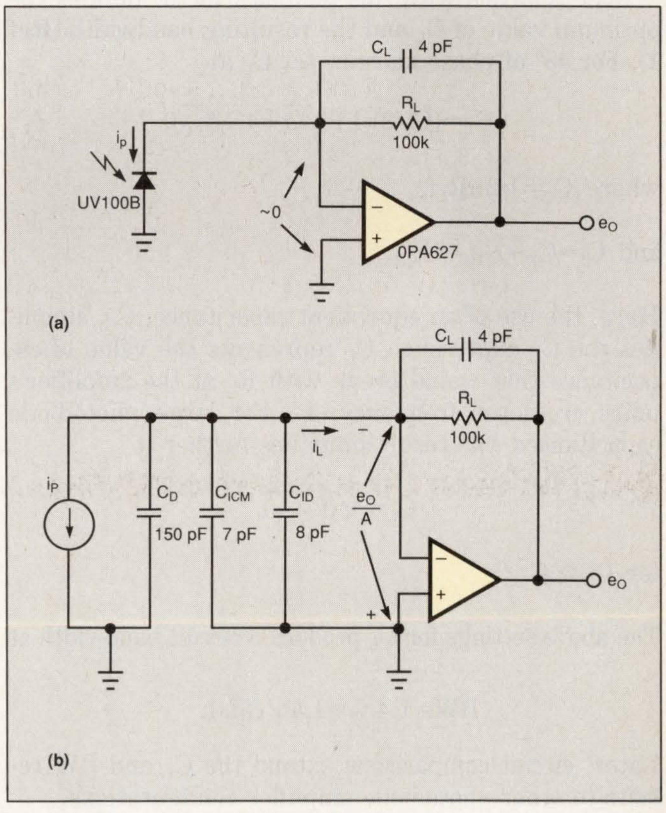

Fig 1—The current-to-voltage converter isolates the photodiode from the e_O swing, leaving only the residual e_O/A across the diode capacitance.

In practice, the amplifier's high, but finite, open-loop gain limits the isolation of **Fig 1a**'s circuit. Part of the circuit's output voltage remains on the photodiode and produces a new bandwidth limit. **Fig 1b** illustrates this isolation limit. Here, a current source and a capacitance, C_D, replace the photodiode. Also, the op-amp input capacitance is separated from the amplifier. These capacitances support the amplifier's gain-error signal, e_O/A. The resulting capacitive currents shunt part of the photodiode current, i_P, producing a new bandwidth limit.

The capacitances also compromise frequency stability, affect bandwidth, and require phase compensation. Together with feedback resistor R_L, the capacitances introduce a feedback pole. Compensation capacitor C_L introduces a feedback zero, counteracting the effect of the pole. The feedback factor, or fraction of the output fed back to the input, reflects the pole and zero in

$$\beta=(1+s/2\pi f_L)/(1+s/2\pi f_I),$$

where $f_L=1/2\pi R_L C_L$,

and $f_I=1/2\pi R_L(C_D+C_{ID}+C_{ICM}+C_L)$.

Bode analysis with this feedback factor defines the optimum value of C_L and the resulting bandwidth (**Ref 1**). For 45° of phase margin, set C_L at

$$C_L=(C_C/2)(1+\sqrt{(1+4C_I/C_C)}),$$

where $C_C=1/2\pi R_L f_C$,

and $C_I=C_D+C_{ID}+C_{ICM}$.

Here, the use of an equivalent capacitance, C_C, simplifies the C_L expression. C_C represents the value of capacitance that would break with R_L at the amplifier's unity crossover frequency, f_C. For large photodiode capacitances, the result simplifies further to

$$C_L=\sqrt{(C_I C_C)},$$

for $C_D \gg C_L$.

The above settings for C_L produce a circuit bandwidth at

$$BW=1.4\ f_P=1.4\sqrt{(f_I f_C)}.$$

Later, circuit comparisons extend the C_L and BW results to other photodiode amplifier configurations.

Even with the I/V converter, the photodiode capacitance remains a primary limitation to the bandwidth. The most common solution is simple reverse bias of the photodiode. This bias reduces the diode capacitance at the expense of other performance. The diode capacitance results from the diode junction and responds to a reverse-bias voltage V_R according to

$$C_D=C_{D0}/\sqrt{(1+V_R/\phi_B)}.$$

Here, C_{D0} is the photodiode capacitance at zero bias and ϕ_B is the built-in voltage of the diode junction. For silicon photodiodes, $\phi_B \sim 0.6V$. With a nonzero V_R above, C_D is smaller than its zero-voltage value of C_{D0}. For example, making $V_R=10V$ reduces the capacitance by a factor of 4.2. From the previous BW expression, the photodiode-amplifier bandwidth is proportional to $1/\sqrt{C_D}$, so making $V_R=10V$ improves the bandwidth by a factor of a little more than 2.

With the basic photodiode amplifier, you can easily apply reverse bias to the diode by returning the diode to a voltage source instead of to common. **Fig 2** illustrates this configuration along with its compromises. You can greatly reduce these compromises by making use of the differential nature of the amplifier. The op-amp input in **Fig 2a** holds the anode of D_1 at 0V. The dc voltage source, V_B, sets the reverse bias at $V_R=V_B$. This bias reduces the diode capacitance as described, but increases the dc error and noise. The dc leakage

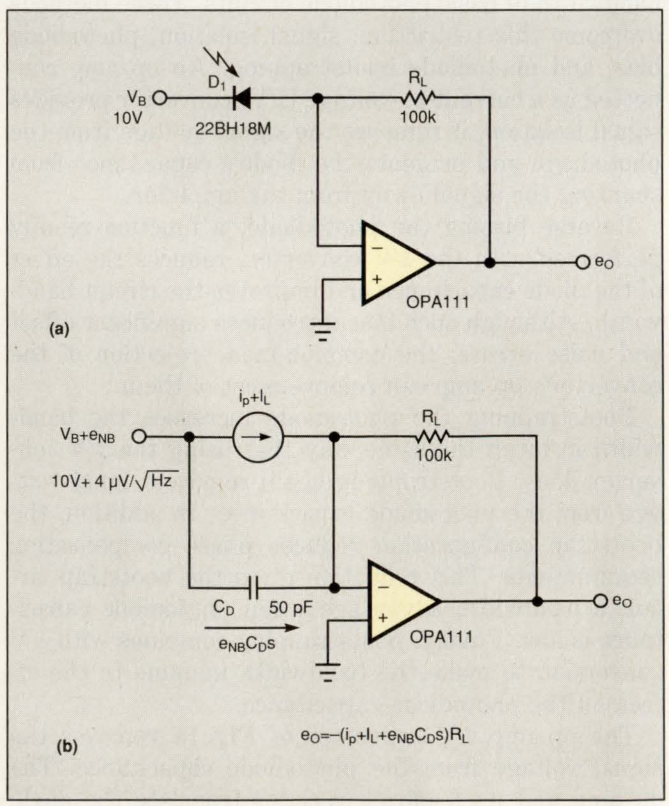

Fig 2—DC bias reduces photodiode capacitance, but increases errors from diode leakage current and bias-source noise.

current of the photodiode and a noise current from V_B, both of which flow through R_L, limit the accuracy of high-gain photodiode amplifiers that use large values of R_L.

In the absence of diode bias, (for example, in **Fig 1**), the photodiode is across the op-amp inputs with virtually no voltage that might produce a diode leakage current. Then, the input errors of the op amp dominate the dc error. Selecting an appropriate op amp minimizes this error. Because of their low bias currents, FET-input amplifiers are a logical choice. With the OPA111 shown, the amplifier input current is 1 pA. This current develops an output offset of 100 nV across the 100 kΩ R_L shown. At 100 nV, the offset effect of the amplifier input current is negligible compared with the amplifier's 100-μV input offset voltage. In **Fig 1**, the amplifier transmits this offset voltage to its output with unity gain, producing an output offset of 100 μV.

Diode bias increases errors

Adding reverse bias to the typical photodiode produces a diode leakage current (I_L in **Fig 2b**) that overwhelms the dc error. To significantly reduce the photodiode capacitance, the diode reverse bias must be large, which raises the diode leakage to its full saturation level, I_S. This leakage current is typically far greater than the FET leakage that produces the amplifier input current. The difference in leakage currents results primarily from the relative junction areas of the photodiode and the amplifier input FET. Leakage current is proportional to junction area, and photodiodes usually have large areas to enhance their photosensitivity. Conversely, amplifier input FETs are as much as 1000 times smaller in order to reduce amplifier input leakage and input capacitance.

With only a moderate size photodiode, like the 0.023 cm^2 device of **Fig 2**, a 10V reverse bias produces a 5-nA leakage current. The flow of this leakage in the 100-kΩ R_L produces a 500-μV output offset that adds to the 100-μV offset error of the op amp. Thus, the diode bias increases the dc error by 6:1 in return for the 2:1 bandwidth improvement.

Noise also increases with photodiode bias through an added noise source impressed on the diode capacitance. In the zero-biased case of **Fig 1**, the photodiode is across the op amp inputs. There, the amplifier input noise voltage, e_{NI}, is impressed on the diode capacitance C_D. Then, e_{NI} produces a noise current in C_D that flows through R_L. This noise current produces an output noise voltage amplified from the op-amp input by a gain of R_LC_Ds. The response zero of this noise gain produces noise-gain peaking (**Ref 2**) and can increase the effect of e_{NI} by a factor of 5 to 10. Added to this amplifier noise is the noise of the resistor. The resistor noise transfers to the circuit output with unity gain. This added noise is $\sqrt{4KTR_L}$ where T is Kelvin temperature and K is Boltzman's constant or 1.38×10^{-23}.

With unbiased photodiodes, the amplifier and resistor noise sources determine the circuit's noise performance. However, the addition of photodiode bias nearly always makes the bias source the dominant source of noise. With the OPA111 of **Fig 2**, the input noise voltage density of the amplifier is 7 nV/$\sqrt{Hz}$ and gain peaking typically amplifies this noise to an effective 50 nV/$\sqrt{Hz}$. With the 100-kΩ R_L shown, the resistor introduces 41 nV/$\sqrt{Hz}$. These two noise signals combine in root-sum-squared fashion to produce a net circuit output noise of 65 nV/$\sqrt{Hz}$.

However, the photodiode bias overrides this noise. The voltage noise of the bias source, e_{NB}, also appears across the diode capacitance of **Fig 2b**. There, it produces a capacitive current of $e_{NB}C_Ds$. This current flows through R_L. The resulting noise gain for e_{NB} is C_DR_Ls or the same as the gain for the amplifier noise, e_{NI}. If the bias source is a 10V reference, its output noise density is typically 4 μV/$\sqrt{Hz}$. Typical noise gain raises this noise to around 30 μV/$\sqrt{Hz}$ at the circuit output. Thus, in **Fig 2**, the diode bias increases the output noise by a factor of about 460 from the 65 nV/$\sqrt{Hz}$ otherwise determined by the op amp and the resistor.

Differential inputs reduce bias errors

Making use of the differential nature of the op amp inputs greatly reduces both the dc and noise errors introduced by photodiode biasing. If you add a second, matching photodiode, as in **Fig 3**, the amplifier's common-mode rejection can reduce the two errors. You also add a second current-to-voltage conversion resistor that is matched to the first resistor. Only the original photodiode, D_1, remains open to light input. The second diode, D_2, is blocked from the light source. The added diode's sole purpose is error cancellation.

Only D_1 supplies a signal current, i_P, but both diodes supply leakage and noise currents to the op amp. The two diodes connect to opposite-polarity amplifier inputs so that the diode error currents produce counteracting effects. Because the anodes of two diodes connect to the op-amp inputs, the anodes are at the same potential. Also, the bias source connects to the cathodes of both photodiodes. Thus, the two diodes have the same voltage drops whether from the dc or the noise outputs of the bias source. The resulting diode leakage currents, I_L, are equal, as are the noise currents of $e_{NB}C_Ds$. Flow of these matched currents in the two R_L resistors produces equal voltages. These equal voltages produce canceling effects in the circuit output voltage. With two photodiodes from the same manufacturing lot, the matching is within about 5% yielding a 20:1 error reduction.

The matched-photodiode solution, although simple to implement, still presents a noise compromise compared with the zero-bias connection. Compared with the zero-bias case of **Fig 1**, the circuit of **Fig 2** produces a 6:1 offset increase and a 460:1 increase in noise. With matched diodes, the circuit of **Fig 3** reduces these effects by a factor of 20. This circuit removes the offset increase, but still lets the noise increase by 23:1. In return for this increased noise, the circuit bandwidth increases by a factor of only 2.

Bootstrap extends bandwidth further

To improve the bandwidth without the bias compromise, use bootstrapping. The I/V converter of **Fig 1** improves the bandwidth by removing the load signal voltage from the capacitance of the photodiode source. This circuit avoids capacitive currents that otherwise absorb signal current at higher frequencies. Bootstrapping can also remove the load signal swing from the source. For photodiodes, bootstrapping either replaces or works with the I/V converter. In either case, the bandwidth is greater than that of the basic I/V converter.

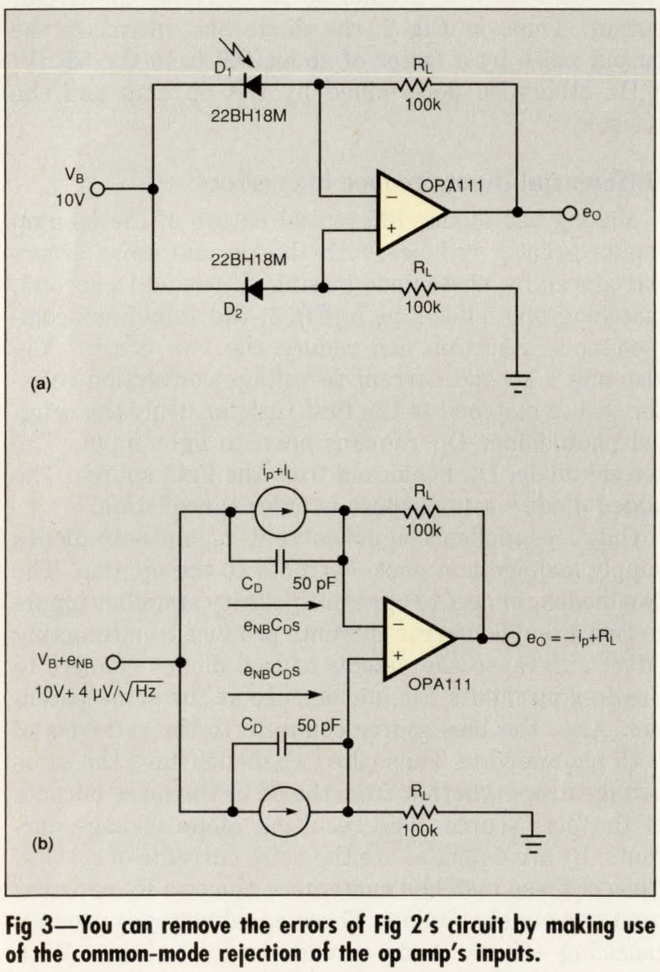

Fig 3—You can remove the errors of Fig 2's circuit by making use of the common-mode rejection of the op amp's inputs.

Conventional bootstrapping drives the common return of a voltage source with the voltage developed on the circuit load. Translating this concept directly to photodiode sources produces results very similar to those described for the I/V converter. Phase compensation requirements and the resulting bandwidth closely follow the earlier discussion, but with added bandwidth in low-capacitance cases. **Fig 4** illustrates bootstrapping applied to the photodiode through a voltage follower. Without the follower, the circuit would ground the anode of the photodiode along with the load, R_L. This shared ground return places the load voltage swing across the photodiode capacitance, resulting in limited bandwidth. **Fig 4**'s circuit uses the voltage follower to drive the diode's anode return. The follower monitors the load-resistor voltage and drives the anode of the photodiode to the same voltage. In the ideal-amplifier case, zero voltage remains across the diode capacitance.

In practice, limited op amp gain leaves a residual signal voltage on the diode capacitance, just as the in the case of the I/V converter of **Fig 1**. As before, this residual signal determines the bandwidth of the bootstrap circuit. To find this bandwidth, **Fig 4b** models the circuit in a manner similar to that used for **Fig 1b**. A current source represents the photodiode. The diode capacitance, C_D, and the op amp input capacitance appear across this source. With respect to the amplifier capacitances, **Fig 4b**'s circuit differs from that of **Fig 1b**. In **Fig 1b**, both C_{ID} and C_{ICM} are across the photodiode, but in **Fig 4b**, C_{ICM} is across R_L instead. This change is what produces the improved bandwidth. To achieve this added bandwidth, you must accept an additional amplifier error: In **Fig 4**, the load voltage is a common-mode voltage for the op amp. This voltage, attenuated by the amplifier's common-mode rejection, results in a small error.

You could perform the bandwidth analysis for **Fig 4** by following the same method used for the I/V converter. However, you need not repeat this detailed analysis when you examine the source of **Fig 4**'s bandwidth limit. The poles of this circuit result from the signal e_O/A that appears on the circuit capacitances. The resulting capacitive currents shunt a portion of i_P away from R_L. This bandwidth-limiting action is identical to that described for the I/V converter. The only difference is that e_O/A appears across slightly different capacitances in the two circuits. In **Fig 4**, this signal is across C_D+C_{ID} and in **Fig 1** the signal is across $C_D+C_{ID}+C_{ICM}$. The difference is C_{ICM}, which in **Fig 4** parallels C_L.

Thus, by accounting for these capacitor differences, you can adapt results of the I/V converter analysis to **Fig 4**'s bootstrap circuit. Specifically, you modify the earlier results by replacing $C_D+C_{ID}+C_{ICM}$ with C_D+C_{ID}. Similarly, you replace C_L of the earlier results with C_L+C_{ICM}. As described later, C_{ICM} acts as part of the circuit phase compensation and less capacitance is required for C_L. The reduced C_L is significant when C_D is small. Then, **Fig 4**'s bootstrap circuit provides greater bandwidth than does the equivalent I/V converter.

The choice of C_L for the remaining bypass requirement otherwise follows directly from the discussion of **Fig 1**. Applying **Fig 1**'s feedback analysis to **Fig 4b** yields very similar results. For this analysis, you determine the circuit's feedback factor. **Fig 4b** shows an op amp with both negative and positive feedback. The feedback combination determines the net feedback factor. From the amplifier's voltage-follower connection, the negative-feedback factor is unity. Capacitances C_D and C_{ID} supply added feedback to the load circuit. These capacitors form a voltage divider with the load; the voltage divider fraction is the added feedback factor. This additional feedback is positive because it drives the noninverting input of the amplifier. The net feedback factor is the difference between the negative and positive feedback factors (**Ref 3**) or $\beta=\beta_- - \beta_+$. For **Fig 4**,

$$\beta=(1+s/2\pi f_L)/(1+s/2\pi f_I),$$

where $f_L=1/2\pi R_L(C_L+C_{ICM})$,

and $f_I=1/2\pi R_L(C_D+C_{ID}+C_{ICM}+C_L)$.

This bootstrap feedback factor is almost identical to that of **Fig 1**'s I/V converter. The only difference is the presence of C_{ICM} in the expression for f_L. Once again, the feedback factor has a pole at f_I formed by R_L and the total capacitance connected to the input circuit. Now, however, C_{ICM} adds to the feedback zero at f_L. Otherwise, the two response singularities produce the same feedback response as described for **Fig 1b**. Phase compensation of **Fig 4**, then, follows the earlier guideline with C_L chosen to produce 45° of phase margin.

Design equations for selecting C_L follow from the **Fig 1** results with a simple modification for the bypass effect of C_{ICM}. As mentioned, this capacitance provides part of the phase-compensating bypass, so the value of C_L decreases by an equal amount. Then, for larger photodiode capacitances, in **Fig 4**

$$C_L=\sqrt{(C_I C_C)}-C_{ICM},$$

where $C_L \ll C_D+C_I$,

and where $C_C=1/2\pi R_L f_C$,

and $C_I=C_D+C_{ID}+C_{ICM}$.

As before, f_C is the op amp's unity-gain crossover frequency. In cases where bootstrapping is most useful, the photodiode capacitance is small and you must use the more complex equation with **Fig 4**.

$$C_L=(C_C/2)\sqrt{(1+4C_I/C_C)}-C_{ICM},$$

where $C_C=1/2\pi R_L f_C$,

and $C_I=C_D+C_{ID}+C_{ICM}$.

As described for **Fig 1**, selecting C_L for 45° of phase margin sets the bandwidth at $BW=1.4\ f_P=1.4\sqrt{(f_I f_C)}$. For the specific components of **Fig 4**, the result is a bandwidth of 2.7 MHz. The equivalent implementation with an I/V converter results in a bandwidth of 2.2 MHz—22% lower than with bootstrapping.

An even greater bandwidth improvement results

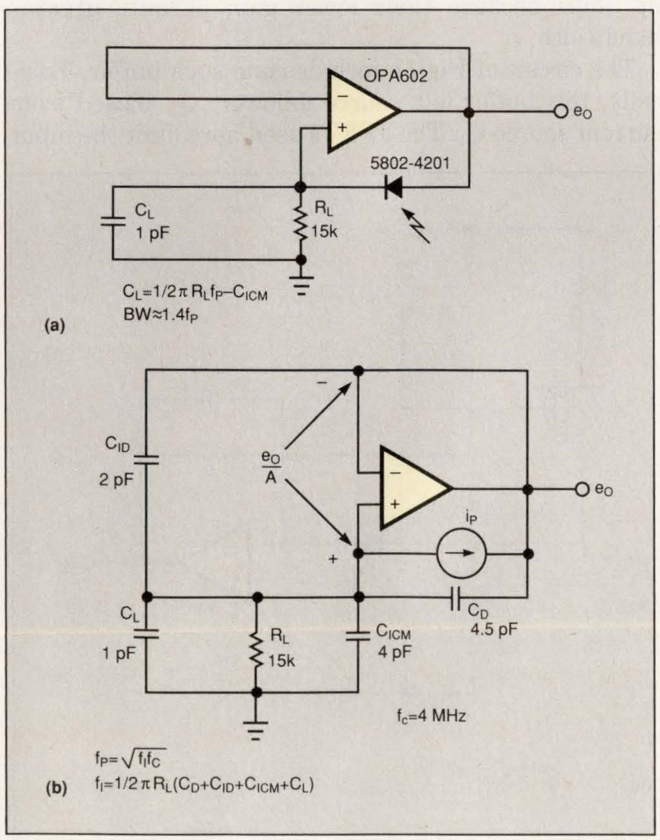

Fig 4—Bootstrap bias replaces the I/V converter, allowing lower values of C_L and increasing the bandwidth.

from combining the benefits of the I/V converter and bootstrapping. **Fig 5** illustrates this combination with the bootstrapping provided by a unity-gain buffer (**Ref** 4). The buffer replicates e_O/A from the I/V converter input at the anode of the diode. Both terminals of the diode have the same signal and there is zero signal across the diode capacitance.

The combination shown in **Fig 5** makes photodiode monitoring immune to the photodiode capacitance as long as the buffer meets several requirements. These requirements are wide bandwidth, low output impedance and low noise. The bandwidth of the buffer must be much greater than that of the op amp used in the I/V converter. This condition limits a new gain error signal that appears across the diode capacitance. As described with **Fig 4**, the bootstrap amplifier has a gain error signal of its own and this signal appears across the photodiode. This error increases with frequency and determines the bandwidth limit in **Fig 4**'s circuit. **Fig 5**'s circuit keeps this buffer error small throughout the op amp's useful frequency range. Also, over this range, the output impedance of the buffer remains low. The roll-off caused by this impedance and the diode capacitance has little effect on the bandwidth. With such a buffer, the I/V converter of **Fig 5** determines the circuit's bandwidth; the bandwidth is independent of the diode capacitance.

How well you can remove the diode-capacitance effects also depends on how well you can control noise from the buffer. In the basic I/V converter of **Fig 1**, the dominant output noise originates with the input noise voltage of the op amp (**Ref 2**). That input noise appears across the photodiode capacitance and the resulting noise current flows through R_L. In **Fig 1**, the end result is a noise gain that peaks at high frequencies and dominates the output noise. **Fig 5**'s circuit bootstraps the photodiode capacitance on the op-amp input noise as well as on the gain error signal. Thus, in **Fig 5**, the op-amp noise does not receive increased high-frequency gain. However, the noise of the buffer now appears across the diode capacitance and does receive this gain. Thus, in **Fig 5**'s circuit, the buffer replaces the op amp in setting the output noise performance.

Fortunately, the circuit relaxes other demands on the buffer performance, letting simple circuits serve as buffers. The buffer does not require the high open-loop gain normally expected of op amps. Buffer gain accuracy is not critical as long as the accuracy does not start to decline at too low a frequency. Relatively small gain error signals impressed on the photodiode do not significantly alter the diode's response. The high-gain op amp of the I/V converter ensures that the circuit response remains accurate. Thus, low-gain, wide-bandwidth circuits are sufficient for the buffer. Furthermore, such circuits are preferable to complete op amps because their lower gain permits greater bandwidth.

The circuit of **Fig 5b** includes one such buffer. Basically, this buffer is a source follower, Q_3, biased from current source Q_4. The JFETs used here limit the input

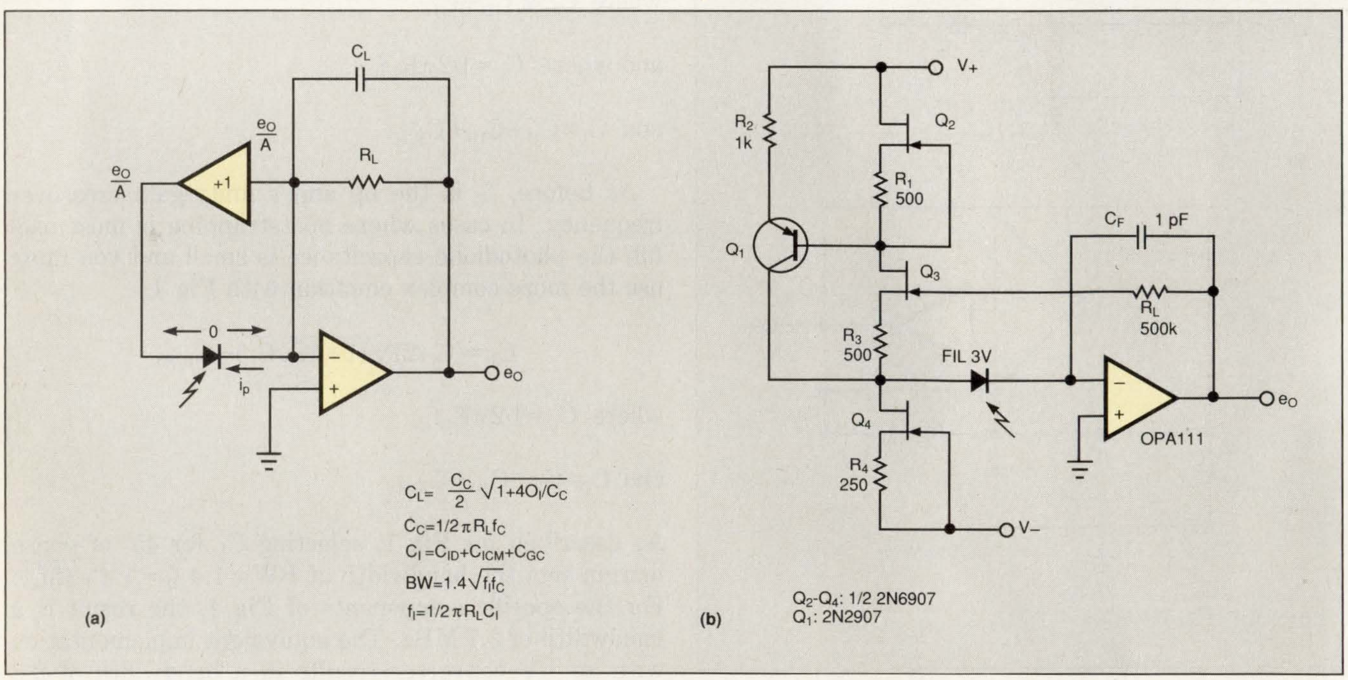

Fig 5—Bootstrapping in combination with use of the I/V converter makes the bandwidth limit essentially independent of the photodiode capacitance.

current drawn by the buffer and permit a simple realization of the current source. Note that the buffer input current flows through R_L, causing increased output offset voltage. Other components of the buffer produce low output impedance. Without Q_2 and Q_1, the buffer output resistance would be $R3+1/gm_3$ where gm_3 is the transconductance of Q_3. Without these added components, which add loop gain and feedback that counteracts current changes in R_3 and Q_3, the output resistance would be too high and would react with the photodiode capacitance at too low a frequency.

The loop gain driving the feedback starts with Q_2. This FET acts as a current-source load to the drain of Q_3. Any change in the current through Q_3 reacts with the high impedance of current source Q_2 to drive the base of Q_1. This transistor responds and supplies the current demanded from the buffer output. Just about the only change in current through R_3 and Q_3 is the change in Q_1's base current. Thus, the added components reduce the buffer output resistance by a factor approximately equal to the current-gain β of Q_1.

Biasing for **Fig 5b**'s buffer avoids dc voltages across the photodiode. As discussed earlier, the typical photodiode has a large junction area capable of producing high-leakage current under bias. To keep the diode's dc bias at zero, Q_2 and Q_3 have equal source resistors. The gate of current source Q_2 returns to the bottom of its bias resistor, R_1. This arrangement establishes a voltage on R_1 equal and opposite Q_2's gate-source voltage. Essentially the same current flows in Q_2 and Q_3 so that, with the matched devices shown, the FETs have equal gate-source voltages. Making $R_3=R_1$ adds just the right dc voltage drop in series with the buffer output. The dc voltage across R_3 is equal and opposite to the gate-source voltage of Q_3, so the buffer introduces no dc offset.

As mentioned, if the buffer meets its requirements, the photodiode capacitance does not affect the bandwidth of **Fig 5**'s circuit. Capacitances remaining at the input of the I/V converter now determine the bandwidth. These capacitances are the input capacitances of the op amp and buffer. For the op amp, the input capacitance is $C_{ID}+C_{ICM}$ as described for **Fig 1b**. For the buffer of **Fig 5b**, the input capacitance is essentially the gate-drain capacitance of Q_3 or C_{GD3}. Note that adding the bootstrap buffer adds this capacitance to the basic circuit. The added capacitance must be smaller than the bootstrapped diode capacitance or the bandwidth will not improve.

Together, the capacitances at the op-amp input of **Fig 5** react with R_L just as described for **Fig 1**. Thus, choosing phase compensation for 45° of phase margin again produces a bandwidth of $1.4\sqrt{(f_I f_C)}$. The compensation for **Fig 5** follows from the discussion of **Fig 1**. Capacitive bypassing of the feedback resistor, R_L, counteracts the feedback pole introduced by the capacitance at the op-amp input. As before, two expressions define C_L depending on the relative size of the diode capacitance C_D. In each expression, you must replace the previous C_D term by the small buffer-input capacitance, C_{GD2}. Substituting C_{GD2} for C_D in the small-capacitance equation for **Fig 3** defines **Fig 5**'s phase compensation as

$$C_L=(C_C/2)\sqrt{(1+4C_I/C_C},$$

where $C_C=1/2\pi R_L f_C$,

and $C_I=C_{ID}+C_{ICM}+C_{GD3}$.

With the specific components in **Fig 5**, the bootstrap delivers a 7.7:1 bandwidth improvement. The components shown have $C_{ID}=1$ pF, $C_{ICM}=3$ pF, $C_{GD3}=1.3$ pF, and $C_D=300$ pF. Also, the imaginary C_C is 0.16 pF for **Fig 5**'s $R_L=500k$ and $f_C=2$ MHz. Setting the phase compensation with the last equation yields $C_L=1$ pF. For these circuit conditions, previous equations define $f_I=1/2\pi R_L(C_{ID}+C_{ICM}+C_{GD3})=60$ kHz and the bandwidth as $1.4\sqrt{(f_I f_C)}=485$ kHz. By comparison, **Fig 5**'s circuit without the bootstrap buffer contends with an input capacitance of $C_D=300$ pF instead of $C_{GD3}=1.3$ pF, so the bandwidth decreases to 63 kHz.

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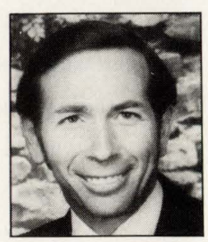
4. O. Compastro, "Utilizacion de fotodetectores de gran area en sistemas de gran ancho de banda," *Revista telegrafica electronica*, July 84, pg 832.

Author's biography

Jerry Graeme, a prolific contributor to EDN, manages instrument-components design for Burr-Brown Corp in Tucson, AZ. At Burr-Brown, he has personally designed many analog ICs. He holds a BSEE from the University of Arizona and an MSEE from Stanford.

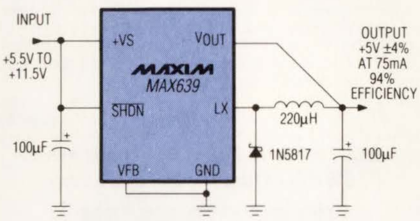


Article Interest Quotient (Circle One)
High 476 Medium 477 Low 478

MAXIM
DESIGN NEWS
Analog Design Insights from Maxim Integrated Products No. 24

Analog Solutions For Tough Design Problems

94% Efficient +5V Step-Down Converter



The **MAX639** switching regulator has greater than 90% efficiency at output currents from 2mA to 200mA due to ultra-low 20μA quiescent current. Features pre-set +5V or adjustable output and logic-controlled shutdown. Available in 8-pin DIP or SO. Evaluation kit also available.

(Circle 50)

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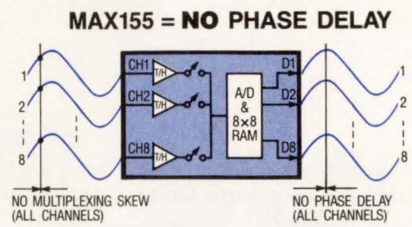

The **MAX155** monolithic ADC simultaneously samples 8 input signals, then sequentially digitizes them to 8-bit accuracy in 3.6μs per channel. Includes +2.5V voltage reference, 8x8 RAM, and 8-bit μP interface. Evaluation kit also available.

*Channel-to-channel phase delay is <4μs. **(Circle 51)**

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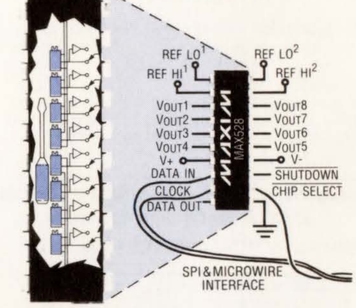

MAX528/MAX529 combine eight 8-bit DACs, output buffer amplifiers, and serial interface logic on a single chip, providing a compact alternative to 8 trimpot-amplifier pairs. Operates from single or dual supplies.

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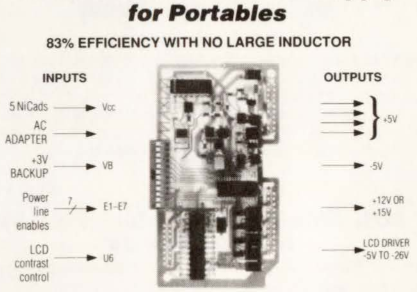

MAX714-MAX716 combine up to four +5V low dropout linear regulators, three DC-DC switching regulators and power-supervisory functions all in one IC. High 83% efficiency saves power and extends battery life. Ideal for 5- or 6-cell inputs. Evaluation kit also available.

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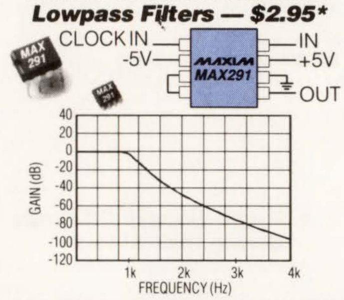
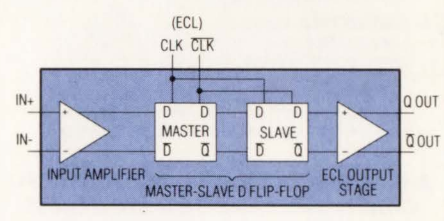


MAX291/MAX295 (Butterworth) and **MAX292/MAX296** (Bessel) 8th-order low-pass switched capacitor filters come in space-saving 8-pin DIP and SO packages, and require no external components. The corner frequency is clock-programmable over a range of 0.1Hz to 50kHz, and THD + Noise is a low -70dB. All devices operate from +5V or ±5V supplies.

*1000-up FOB USA

(Circle 54)

2ns Comparators Resolve 3mV Signals with No Oscillation



The **MAX905/MAX906** ultra high-speed, precision single and dual ECL comparators eliminate oscillation caused by unwanted parasitic feedback. Resolves inputs as small as 3mV over its common-mode range, and prop delay is independent of input overdrive.

(Circle 55)

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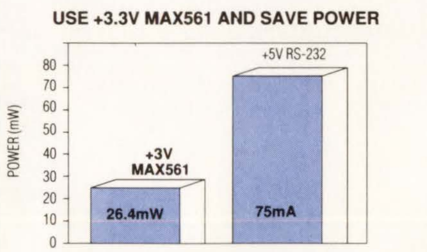
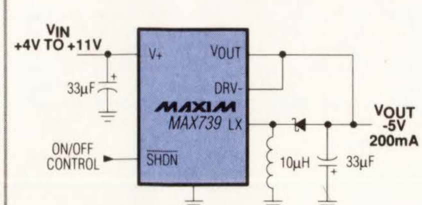


The **MAX561** is the first device to implement the new EIA/TIA-562 standard that guarantees operation with output voltages as low as ±3.7V. The MAX561 consumes **1/3 the power** of +5V RS-232 and operates from a 3.3V power supply.

(Circle 56)

83% Efficient Negative Power Supplies



The new **MAX739/MAX759** pulse-width modulated DC-DC CMOS inverters are the outstanding choice for battery-powered portable equipment. Compact size (0.65in²), high efficiency (83%) and 1μA pin-controlled shutdown make these DC-DC converters unbeatable for extending battery life. Evaluation kit also available.

(Circle 57)

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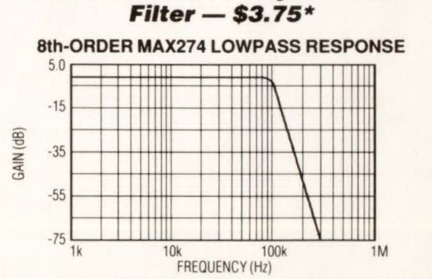
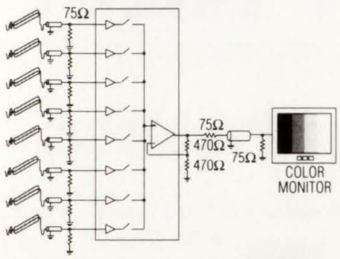


The **MAX274/MAX275** 8th-order/4th order filters combine a proprietary low-noise circuit design with a continuous-time architecture to provide 120μVRMS noise floor and 92dB dynamic range for both bandpass and lowpass applications. Eliminate clock noise and aliasing problems common with switched-capacitor solutions, while achieving 1% accuracy up to 300kHz frequencies. Evaluation kit also available.

*1000-up FOB USA **(Circle 58)**

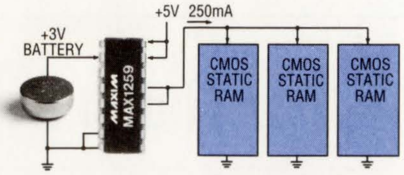
160MHz Video Mux/Amps Pixel Switch in 15ns



MAX440/441/442 combine a 160MHz, unity-gain stable video amp plus 8-, 4-, or 2-channel multiplexer in a single DIP/SO. Pin-selectable frequency compensation (MAX440/441) allows the amp's AC response to be optimized without external components (110MHz for gains ≥ 6dB) and output-disable allows multiple MAX440s to be paralled for larger switch matrices.

(Circle 59)

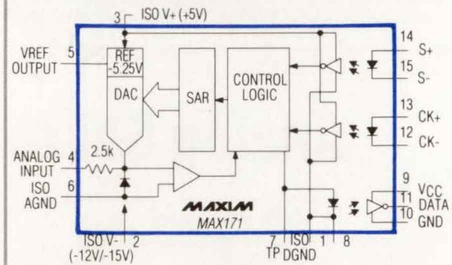
Battery Manager Reduces Power Consumption 1/3



The new **MAX1259** battery manager consumes only 100nA supply current in back-up mode, 3.3mA in operating mode. When power fails, it switches CMOS RAM, real time clocks, or other continuously powered circuits to the backup battery. Commercial/military temperature range.

(Circle 60)

UL-Approved 1500V, Opto-Isolated 12-Bit ADC with Ref

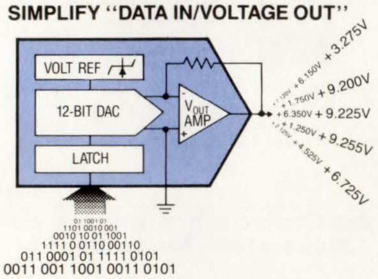


The **MAX171** is a complete 5.8μs 12-bit ADC that provides over 1500 VRMS electrical isolation between its analog input and the digital interface pins. It combines an ADC, three high-speed opto-couplers, and a low-drift buried-zener reference, to produce an isolated data aquisition system.

(Circle 61)

Complete 12-Bit Voltage-Output DACs with Reference

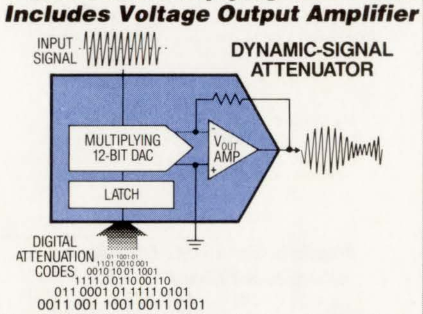
SIMPLIFY "DATA IN/VOLTAGE OUT"



MX7245/MX7248 complete, 12-bit, voltage-output DACs combine a laser-trimmed DAC, a BiCMOS output amplifier with +10V out drive capability, and a +5V ±30ppm/°C buried-zener reference on a single IC. Double-buffered logic inputs are offered in both a 12-bit wide (MX7245) and a 8+4-bit wide (MX7248) data bus for fast interface to 8- and 16-bit microprocessors.

(Circle 62)

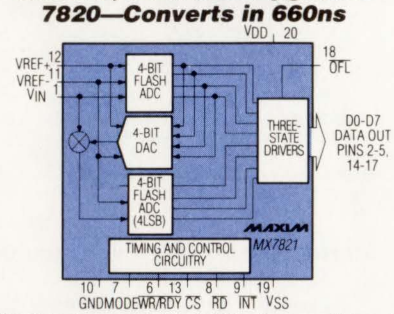
4-Quadrant Multiplying 12-Bit DAC Includes Voltage Output Amplifier



The **MX7845** 12-bit, 4-quadrant, voltage-output multiplying DAC combines a BiCMOS amplifier with ±10V drive capability and a laser-trimmed, thin-film-resistor DAC on a single chip.

(Circle 63)

MX7821, 8-Bit ADC Upgrades 7820—Converts in 660ns



MX7821 high-speed, 8-bit ADC is μP-compatible and uses a half-flash technique to reduce conversion time to 660ns. In addition to unipolar operation, it includes a VSS pin to support dual power supplies and bipolar inputs (rail-to-rail). Track-and-hold function digitizes dynamic input signal—no external clock required.

(Circle 64)

Adjustable Output Step-Down DC-DC Converters Have 94% Efficiency!

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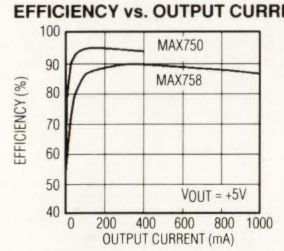
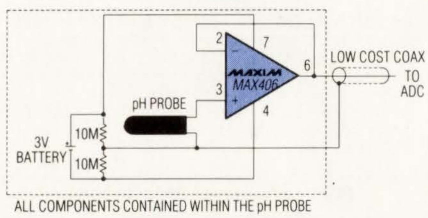


The **MAX750/758** high-efficiency 160kHz PWM step-down regulators have adjustable outputs down to 1.25V. The inputs can be as high as 11V and 16V respectively—88% to 94% efficiency, 6.0μA logic-controlled shutdown, and compact 0.65in² circuit size make them an outstanding choice for battery-powered, portable equipment. Evaluation kit also available.

(Circle 65)

1μA Single Supply Op Amps Swing Rail-to-Rail



The **MAX406/407** single/dual op amps operate from a single supply as low as +2.5V and consume less than 1.2μA per amplifier. Outputs swing rail-to-rail while sourcing up to 2mA and the input range extends from the negative supply rail to within 1.2V of the positive supply. And, unlike other CMOS op amps, the MAX406/MAX407 maintain stability without external compensation while driving loads in excess of 1000pF.

(Circle 66)

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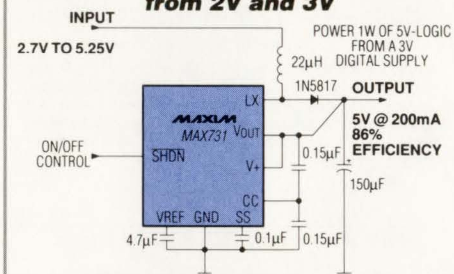

The **MAX731/MAX752** step-up regulators are used to build 85% to 90% efficient power supplies that fit into less than 0.65in² of board space. The MAX731 has fixed +5V output voltage and the MAX752 has an adjustable +2.7V to +15.75V output voltage. Evaluation kit also available.

(Circle 67)

MAX639	(Circle 50)	MAX561	(Circle 56)	MX7245/MX7248	(Circle 62)
MAX155	(Circle 51)	MAX739/759	(Circle 57)	MX7845	(Circle 63)
MAX528/529	(Circle 52)	MAX274-275	(Circle 58)	MX7821	(Circle 64)
MAX714-716	(Circle 53)	MAX440/441/442	(Circle 59)	MAX750/758	(Circle 65)
MAX291-296	(Circle 54)	MAX1259	(Circle 60)	MAX406/407	(Circle 66)
MAX905-906	(Circle 55)	MAX171	(Circle 61)	MAX731/752	(Circle 67)

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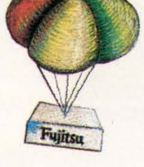

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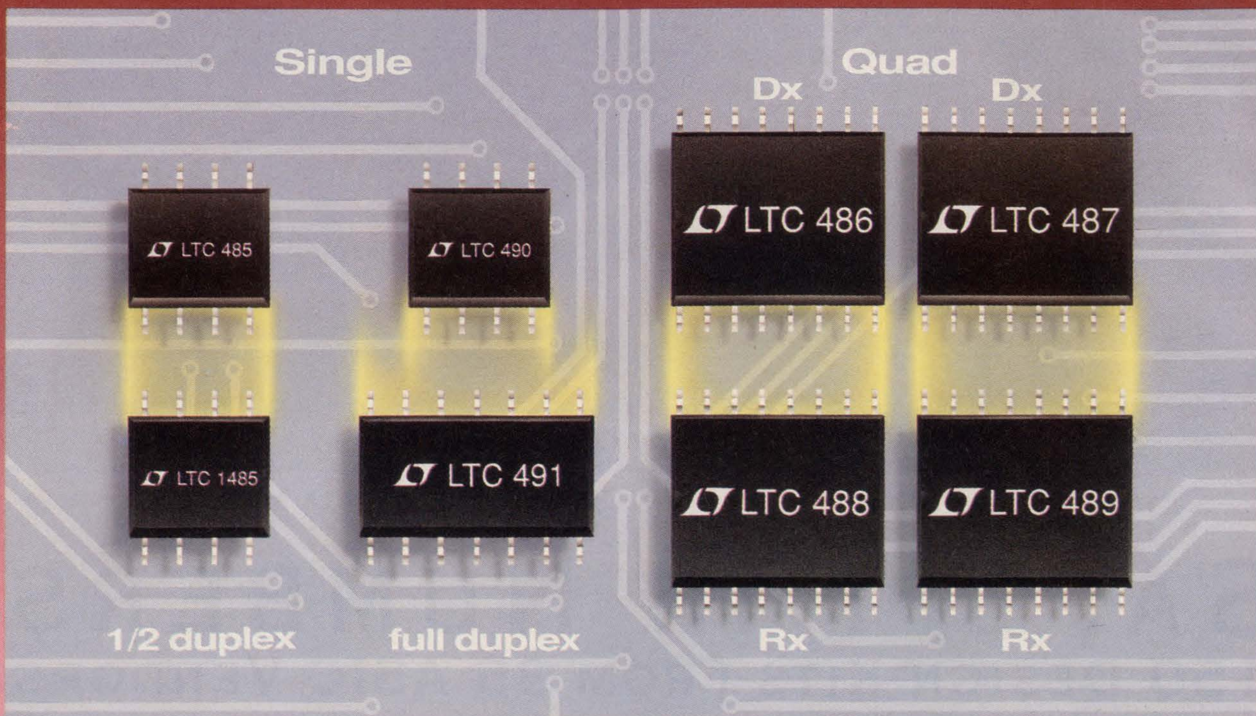

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LTC PART NUMBER	DESCRIPTION	LTC POWER SAVINGS	I_{CC} MAX	STD PINOUT
LTC485	Half Duplex Transceiver	60X Lower	500μA	75ALS176B
LTC486	10Mbs Quad Driver	400X Lower	150μA	75172
LTC487	10Mbs Quad Driver	400X Lower	150μA	75174
LTC488	10Mbs Quad Receiver	7X Lower	10mA	75173
LTC489	10Mbs Quad Receiver	7X Lower	10mA	75175
LTC490	Full Duplex Transceiver	140X Lower	500μA	75179B
LTC491	Full Duplex Transceiver	60X Lower	500μA	75ALS180
LTC1485	10 Mbs Half Duplex Transceiver	8X Lower	3.5mA	75ALS176B

LTC490/491 are full duplex versions of the LTC485, containing a single driver and receiver. Power dissipation is the same as the LTC485 —a mere 2.5 milliwatts. The LTC1485 is a true 10Mbs version of the LTC485 with only 17.5 milliwatts of power consumption.

All LTC RS485 parts withstand forced voltages above and below the supplies without latchup. Driver skew is less than 10ns and outputs stay glitch free during power up/down.

All parts are available in DIP and SOIC packages in commercial and industrial temperature grades. 100-up pricing in plastic DIP starts at $1.35. For more information contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call **800-637-5545.**

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CIRCLE NO. 111

EPROM and latch detect digital peak

Yongping Xia, EBT Inc, Torrance, CA

The circuit in **Fig 1** uses two chips to detect and hold the highest value of the digital input. An 8-bit input signal is sent to the lower 8-bit address of a 64k×8 EPROM, the 27512. The output of the EPROM is stored in an 8-bit register, a 74HC273. The output of the register feeds back to the EPROM's higher 8-bit address. Using this arrangement, you can program the EPROM so that its output equals the higher value of two 8-bit addresses. Assume the low address is 21H and high address is 32H. Then, the content in address 3221H should be 32. Any time the input value is larger than the stored value, a strobe signal will latch the new value into the register. Thus, the register's output will be the highest input value since the last reset. The circuit can be reset by setting RESET to low, which clears the register. **Listing 1**'s program, which you can also download using EDN's BBS, helps to prepare the binary data for the EPROM.
EDN BBS /DI_SIG #1130

To Vote For This Design, Circle No. 742

Listing 1—C program for EPROM binary data

```
#include <stdio.h>
long high_byte, low_byte, number;
main(void)
{
  FILE *stream;
  if ((stream = fopen("HIGHEST.DAT", "wb")) = = NULL)
                                        /* open file HIGHEST.DAT */
   {
     fprintf(stderr, "Cannot open output file.\n");
     return 1;
   }
  for (number=0; number<65536; number++)
   {
   high_byte= number/256;
   low_byte=number-high_byte*256;
   if (high_byte>low_byte)
   fwrite(&high_byte, 1, 1, stream);
   else fwrite(&low_byte, 1, 1, stream);
   }
  fclose(stream);
  return 0;
}
```

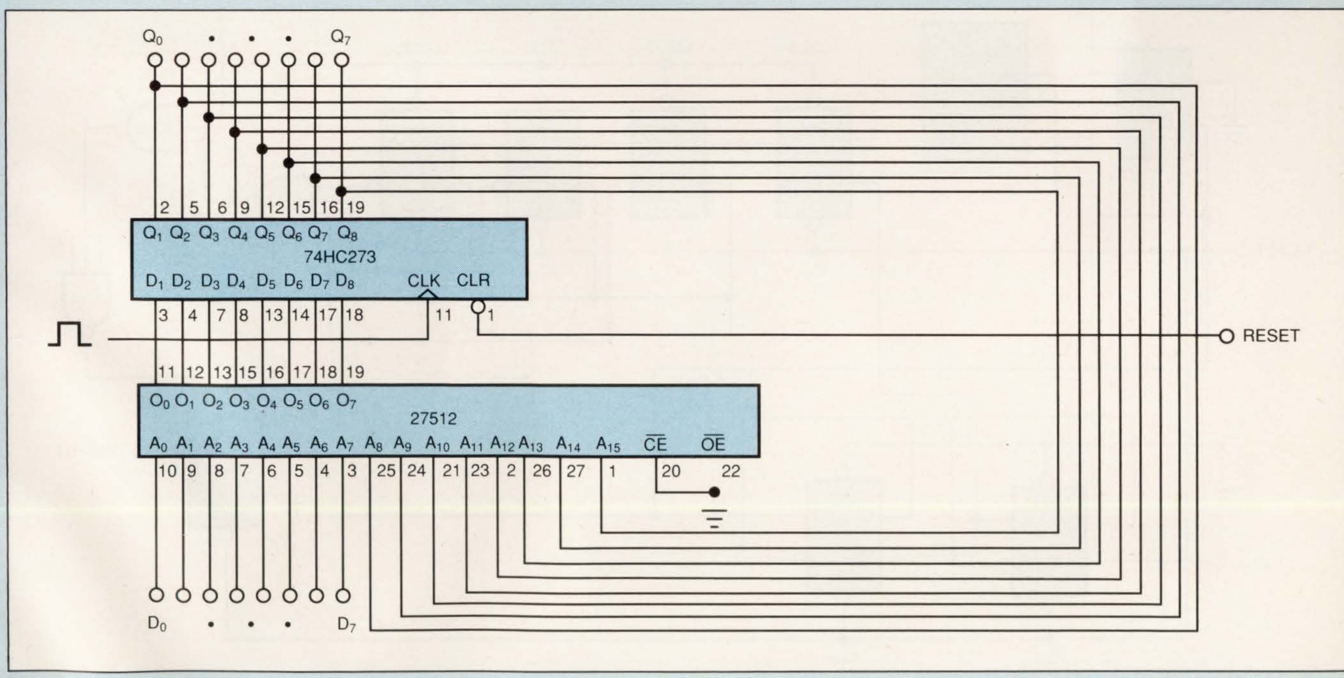

Fig 1—Incoming data bits D_0 to D_7 drive the lower 8 bits of a 64k×8 EPROM, and the latched output of the EPROM drives the higher bits. With the EPROM programmed so that its output equals the higher value of two 8-bit addresses, the register's output will be equal to the highest value input since the last reset pulse.

Digital delay line adds windows

Larry Decker, Cincinnati Microwave Inc, Cincinnati, OH

When it's necessary to compare a signal with an event that occurred at some earlier predetermined time, a shift register can function as a digital delay line. The desired resolution (or quantization) determines the number of register buckets. Because the input signal is usually a digitized analog signal, such as a recovered radar pulse or a biomedical parameter (eg, heartbeat or respiration rate), the input will not be perfectly synchronized with the register's clock. Therefore, a signal could be teetering on the edge of a bucket's quantization time. If this occurs, the probability of detection is seriously degraded. In addition, the signal may have some natural dither associated with it, such as the interval of a heart beat. In this case, each bucket may have a large hole at its beginning and end. The signal will go undetected because in one period it appears in bucket n and the next signal is in $n-1$ or $n+1$.

One quick solution to this problem is to add a window by ORing the desired bucket's output with the one before and the one after. An immediate consequence is that the resolution of the delay line is now cut to one third of its previous value. Thus, regaining that resolution requires you to use three times as many buckets. Also, the window now has a fixed value of three times the quantization time. Another possibility is to stretch the input so it is two buckets wide, but this too requires twice as many buckets as before, and the window is two times the quantization time.

The circuit in **Fig 1** presents an alternative windowing scheme. Shift register IC_5 has enough resolution to account for the signal plus the window size. The number of buckets will be N_S. IC_5's actual length is N_S-1. The amount of dither the signal may have and still be valid determines the window size. The minimum clock frequency, CLK_4, gives the proper delay time, t_{delay}: $CLK_4=N_S/t_{delay}$ Hz. The required window size determines the maximum clock frequency, which is a binary multiple of CLK_4. If the dither time is t_{dither}, then CLK is less than or equal to $1/t_{dither}$.

The circuit adds a stage of shift register after IC_5 for each intermediate clock frequency up to and includ-

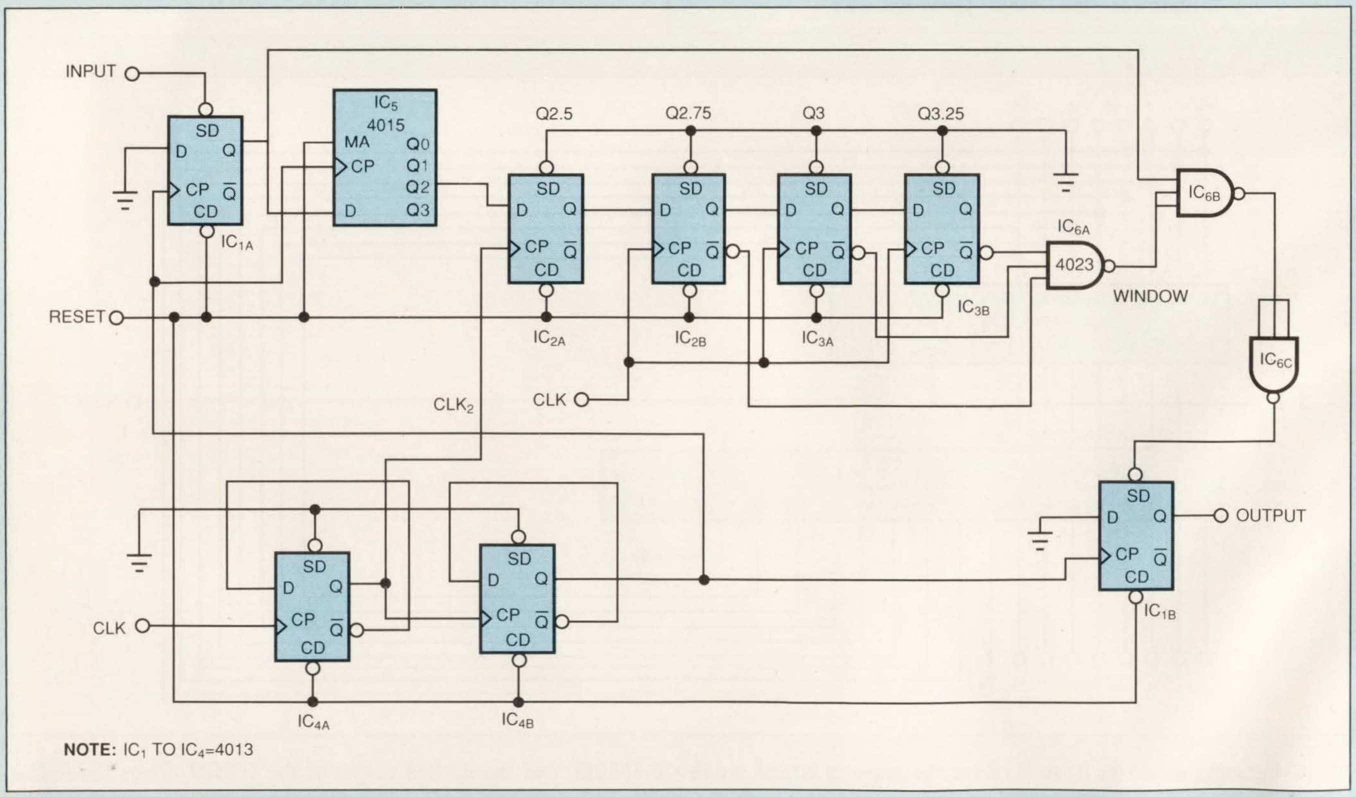

Fig 1—This circuit adds a window to a digital delay line.

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††Midband $10f_L$ to $f_{U/2}$, ±0.5dB † 1dB Gain Compression ◊Case Height 0.3 in.
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CIRCLE NO. 112

C118 REV. F

ing CLK. Each stage's clock will be twice as great as the stage before, until the stage's clock reaches the CLK frequency. The first stage that runs at CLK frequency will be the $-t_{dither}$ bucket. The circuit adds two more stages running at CLK to produce the middle bucket and the $+t_{dither}$ bucket. ORing together the last three stages (all those running at CLK) will give the required $t_{delay} \pm t_{dither}$.

If the buckets use positive-edge clock inputs, a down counter, such as IC_4, is necessary to generate all the clocks. If you use negative-edge clocked buckets, then you'll require an up counter. These counters produce clocks that have the proper phase relationships. In the **figure,** IC_{1A}'s latch holds the input until the shift register is ready to receive it. IC_2 and IC_3 are the stages that provide the windowing transformations. The circuit ORs the proper outputs via IC_{6A} and compares the delayed signal with the real-time signal via IC_{6B}. IC_{1B} stretches the output pulse and synchronizes its trailing edge with CLK_4. IC_4 provides the additional two clock frequencies in proper phase for the positive-edge 4013s. The signal RESET initializes the circuit at startup. **EDN BBS /DI_SIG #1128** EDN

To Vote For This Design, Circle No. 743

Controller keeps temperature within ±0.5°C

James L Engle, Institute for Cancer Research, Philadelphia, PA

The circuit in **Fig 1** isn't as precise as a good ovenized temperature control, but it will hold the temperature within ±0.5°C in a normal room. Q_2 and its load serve as a heat source. The thermistor senses the resultant temperature and feeds a correction voltage back to Q_2 via Q_1. The circuit to be stabilized, which for this design is a voltage-controlled oscillator having a range of ±10%, is located near the thermistor, and the whole assembly is mounted on a small 1-mm-thick copper plate to provide quick reaction and prevent thermal oscillation. The components are soldered to push-in terminals.

Q_2 is a power MOSFET. This component's 4V threshold gate voltage is uncomfortably close to the 5V supply. A MOSFET with a 3V threshold would be better. An on-board regulator provides the 5V supply. The set temperature depends on the circuitry at Q_1's gate, including the threshold voltage of the gate. With the components used, regulation occurs at 40°C (104°F). The thermistor, a Fenwal bead having a negative temperature coefficient, is glued to the copper plate. At room temperature, it has a resistance of 1 kΩ. The copper plate lies on a copper-clad ground plane with other circuitry. The cladding is milled off around the border of the copper plate, except for a few soldered ground points.

Without using this temperature control, the oscillator frequency slowly decreases by 300 ppm, but if you use the temperature control, the frequency decreases by only 20 ppm (and the temperature increases by 0.5°C). The highest power dissipation is about 10W, which occurs at turn-on when Q_2's collector is shorted to ground. The 5W resistor does not have time to heat up to harmful levels. After the temperature has stabilized, the dissipation is much lower and depends on ambient temperature, heat conduction, and heat radiation from the copper plate. **EDN BBS /DI_SIG #1131** EDN

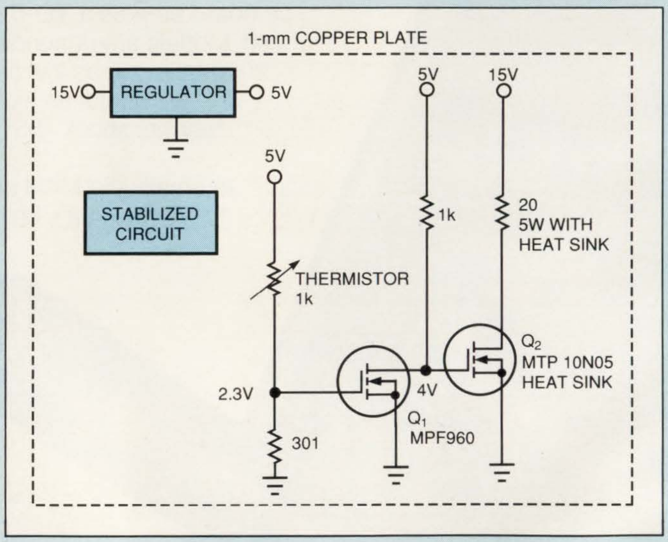

Fig 1—To hold the temperature of the stabilized circuit within ±0.5°C, this circuit senses the temperature using a thermistor that feeds a correction voltage to Q_2 via Q_1.

To Vote For This Design, Circle No. 744

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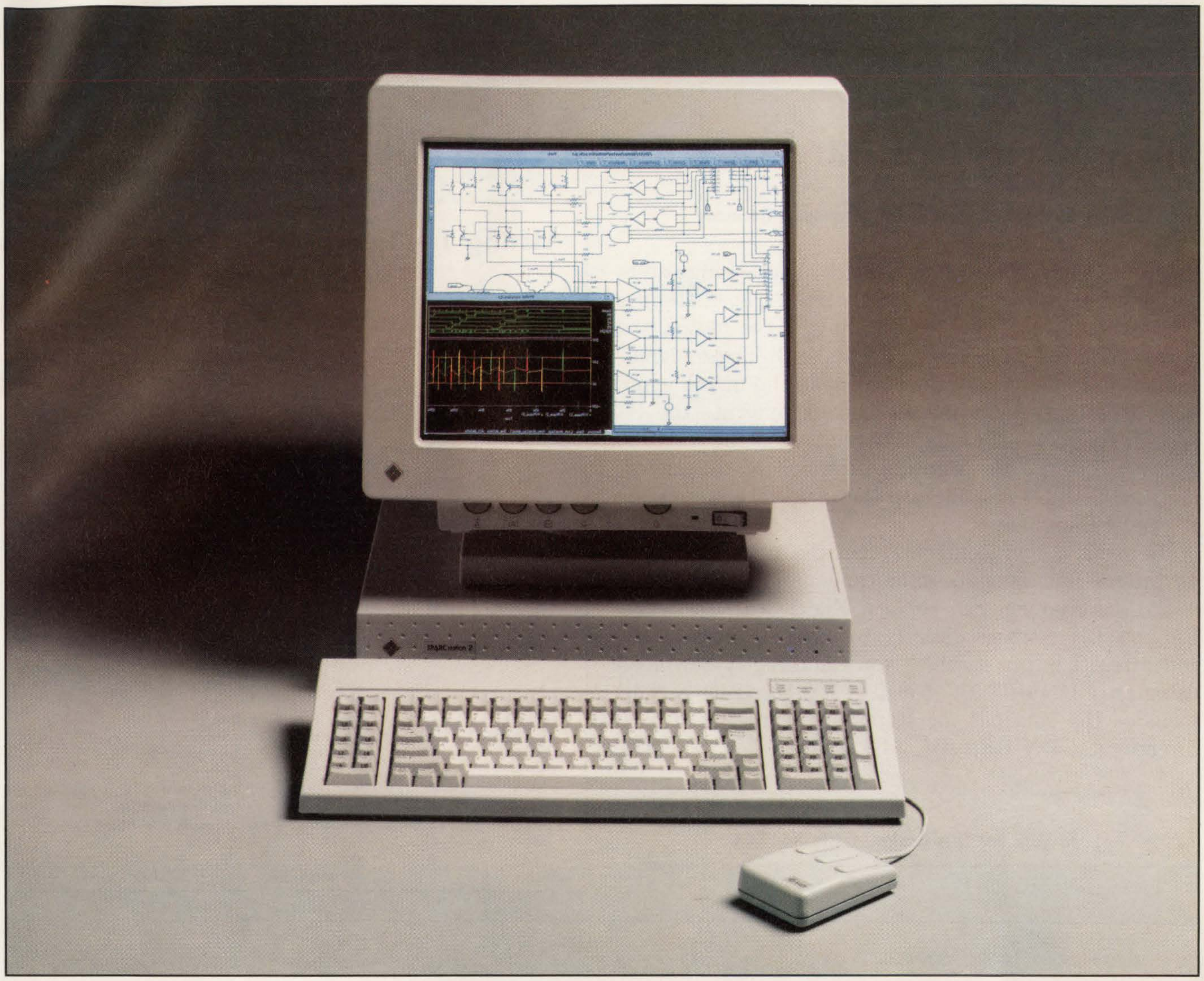

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CIRCLE NO. 113

Software usurps hardware motor controller

Hans-Herbert Kirste, Sensycon GmbH, Hannover, Germany

Driver ICs such as the 3717A full-bridge stepper-motor driver can control 2-phase stepper motors. To control the coils of the motor, the driver requires two signals, PA and PB. These signals control the direction of the current in the motor windings. **Fig 1** presents one method to generate the PA and PB signals. The simple circuit uses the 74HC86 gates to change the rotation direction of the motor, and the 74HC74 to generate the proper timing of the PA and PB signals.

By using a microcontroller that can use its I/O pins as inputs and outputs simultaneously, such as the 80C51 family, you can replace **Fig 1** with software. PA and PB connect directly to two I/O pins of the controller. **Listing 1,** which you can directly download using the EDN BBS (617-558-4241,300/1200/2400,8,N,1,) includes the routines for stepping the motor in both directions. **EDN BBS /DI_SIG #1055** EDN

To Vote For This Design, Circle No. 745

Listing 1—Two-phase stepper-motor drive routines

```
                STEP_ROUTINE   SEGMENT CODE
                ;
----                   RSEG    STEP_ROUTINE
                ;
 0090           PA     EQU     90h            ; phase A = P1.0
 0091           PB     EQU     91h            ; phase B = P1.1
                ;
                ;      LISTING 1 routines to drive 2-phase stepper motor with 3717A
                ;      ==========================================================
                ;
                StepForward:
0000 A290              mov     c,PA           ; get the status of PA
0002 92E0              mov     acc.0,c        ; save it
0004 A291              mov     c,PB           ; get status of PB
0006 B3                cpl     c              : reverse status
0007 9290              mov     PA,c           ; is new status for PA
0009 A2E0              mov     c,acc.0        ; get old status of PA
000B F591              mov     PB,a           ; is new status for PB
000D 22                ret
                ;
                ;
                StepBackward:
000E A291              mov     c,PB           : get the status of PB
0010 92E0              mov     acc.0,c        : save it
0012 A290              mov     c,PA           ; get status of PA
0014 B3                cpl     c              : reverse status
0015 9291              mov     PB,c           : is new status for PB
0017 A2E0              mov     c,acc.0        : get old status of PB
0019 F590              mov     PA,a           : is new status for PA
001B 22                ret
                       END
```

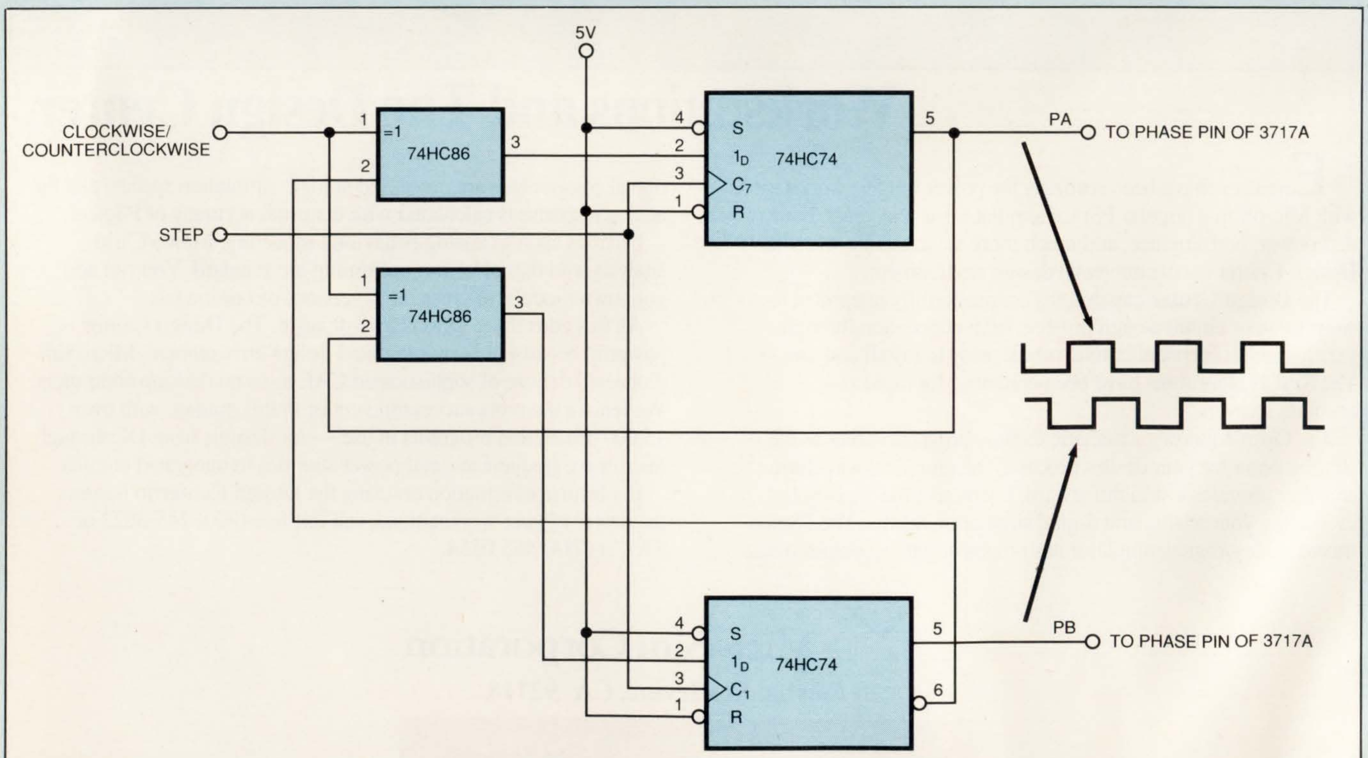
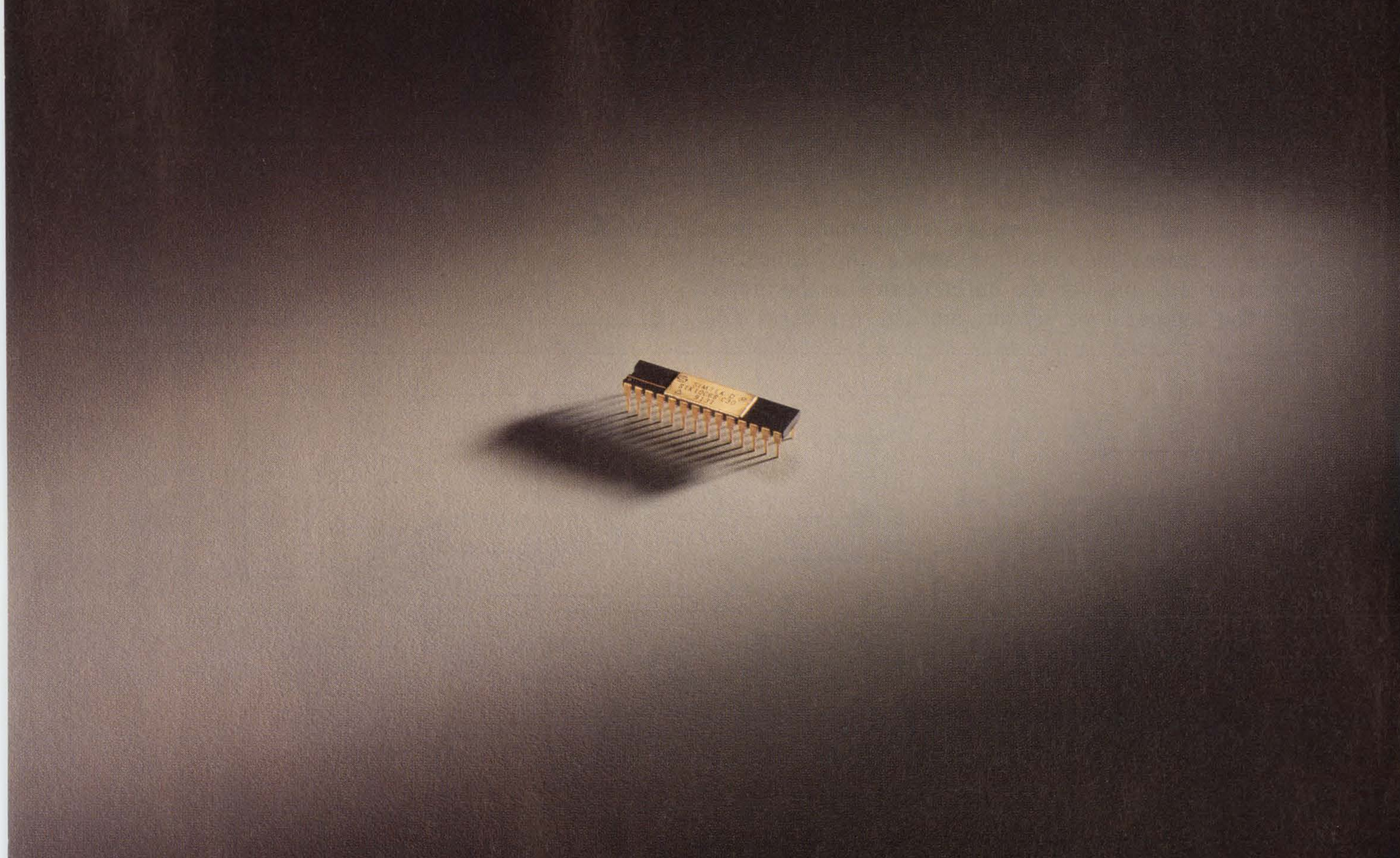


Fig 1—This circuit generates direction and timing signals for the 3717A full-bridge stepper-motor driver.

Batteries not included.



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CIRCLE NO. 114

Ground acts as thermocouple reference

Adolfo Garcia, Analog Devices, Santa Clara, CA

The simple circuit in **Fig 1** accomplishes two objectives: accurate and linear amplification of very low thermocouple output voltages, and the use of the signal-conditioning amplifier's ground as the thermocouple's reference.

The calibration procedure requires only two simple steps. After an initial 5- to 10-minute warmup period to allow the resistors, the REF-01, the AD592CN, and the OP-177A to stabilize, place the thermocouple in an ice bath and adjust R_1 so that V_{OUT} equals 0V. Next, place the thermocouple in a hot environment within its temperature range and adjust R_2 for the correct V_{OUT}. Another option is to apply a voltage that is representative of a known hot environment in place of the thermocouple. The first step of the calibration procedure accounts for the initial offsets in the amplifier, the temperature sensor, and the resistors. The second step corrects the gain, or span, of the thermocouple amplifier.

Once calibrated, the major sources of error in the design are the nonlinearity of the thermocouple and the drift characteristics of the op amp, the resistors, the REF-01, and the AD592CN. A worst-case analysis of the thermocouple amplifier indicated that with 1%, low-drift resistors, the maximum error due to component drifts was under ±1°C over the −25 to 105°C operating range. The analysis indicated that the resistor temperature coefficients and the matching of resistor temperature coefficients were the largest sources of errors, assuming perfectly linear thermocouples. **EDN BBS /DI_SIG #1116**

To Vote For This Design, Circle No. 746

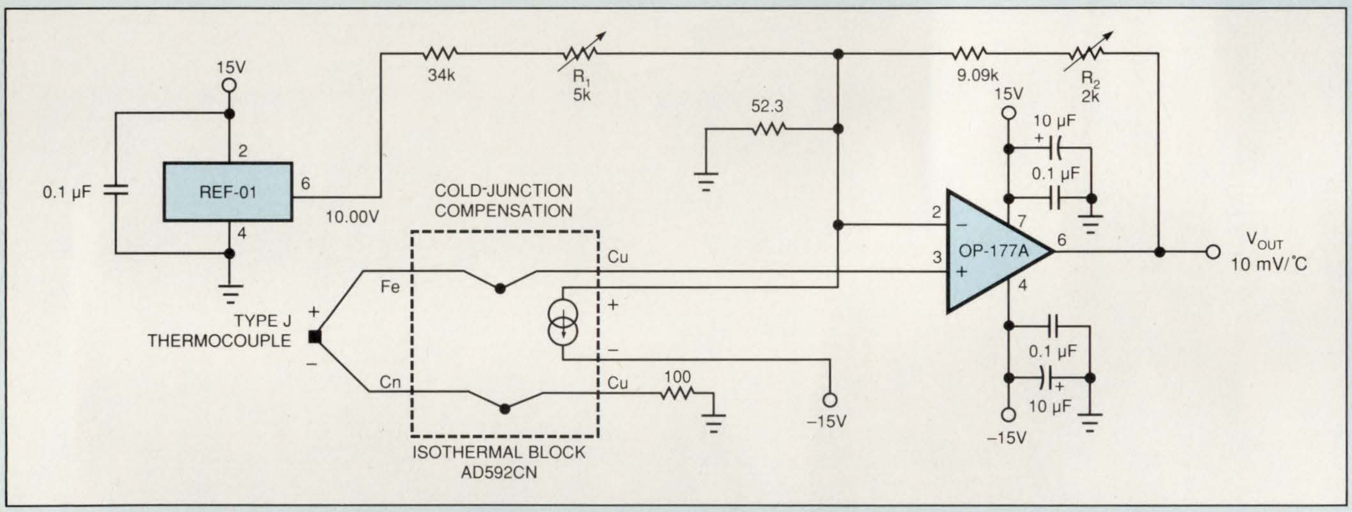


Fig 1—This cold-junction compensated thermocouple amplifier takes its reference from ground.

Optoisolator maximizes op amp's range

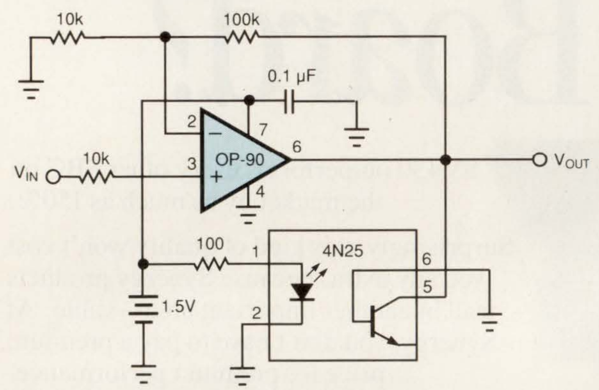
John Guy, Analog Devices, Santa Clara, CA

The technique of using coupling capacitors to get bipolar outputs from a single-supply amplifier is limited because it doesn't provide a response down to dc. The circuit in **Fig 1** instead uses low-cost parts to provide operation at dc and down to 1.5V, an input voltage range which goes below ground, and full output swings to −500 mV. The circuit is useful for buffering low-level, high-impedance, ground-referenced transducers such as moving-coil microphones and piezoelectric sensors.

The key to using the amplifier's full input range is the optoisolator, the 4N25, attached to the base of the amplifier. The LED current is set to 4 mA, and light

from the LED energizes the base-collector junction, yielding V_{BC} of −500 mV under no-load conditions. Output impedance is very high at 8.5 MΩ. Because the total supply current for this amplifier is only 20 μA, the output stage operates in class-A mode, yielding low total harmonic distortion.

The input and the output of the op amp must be capable of going below ground. The input of the OP-90 op amp can go down to −300 mV. The circuit's total supply current is 4 mA, primarily due to the LED. Lowering the LED current to 2 mA reduces dissipation but also reduces both negative output voltage, V_{OL}, and output drive capability (see table in **Fig 1**). The circuit will work not only with the 4N25 shown, but also with almost any optoisolator that uses a bipolar-transistor detection device. Note that the circuit uses the optoisolator's collector, not its emitter. Although the emitter also generates a negative voltage, its low breakdown voltage—approximately 7.5V—with respect to the base makes it unsuitable for higher-voltage operation. **EDN BBS /DI_SIG #1113**



NOTE: 4N25 MADE BY MOTOROLA AND TRW

I_{LED}(mA)	$I_{CURRENT\ SOURCE}$(μA)
2	8.4
4	20.0
6	37.5
8	54.0
10	69.7
12	85.8
14	102.4

Fig 1—Without using capacitors, this circuit takes advantage of a single-supply op amp's range by operating with supply voltages as low as 1.5V and is useful for buffering low-level, high-impedance ground-referenced transducers.

To Vote For This Design, Circle No. 747

Low-dropout charger works from battery

Isaac Eng, University of Ottawa (ESTCO), Ottawa, Ontario, Canada

The battery charger in **Fig 1** provides a 100-mA constant-current charge with a 0.2V dropout voltage. At higher currents, the dropout increases slightly (3.2 mV/100 mA).

IC_1, an LM10, contains an op amp and an internally trimmed 0.2V reference. The op amp, IC_{1A}, buffers the reference. IC_{1B} applies negative feedback to Q_1's gate to maintain constant current flow from drain to source by maintaining a constant voltage at Q_1's source. Select R_1 to achieve your desired current flow. Choose Q_1 for low ON resistance. The dc supply must be greater than 4.2V to develop sufficient gate bias for Q_1. You can reduce the dropout voltage further by dividing V_{REF}. **EDN BBS /DI_SIG #1069**

To Vote For This Design, Circle No. 748

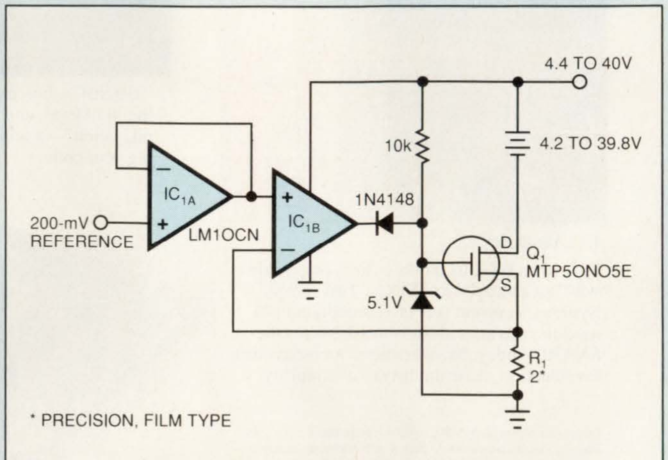


Fig 1—This battery charger has a 0.2V dropout voltage.

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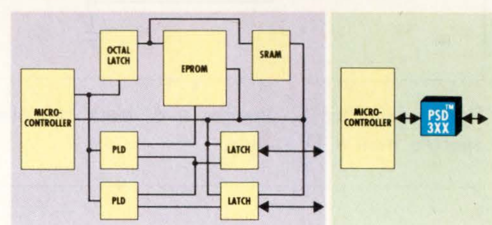

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CIRCLE NO. 116

Cascode circuit works from 1V supply

Ian M Wiles, IPR Technology, Basingstoke, Hants, UK

Cascode circuits are often used in RF amplifiers because of these circuits' excellent gain and reverse-isolation performance. One drawback of the conventional cascode circuit in **Fig 1a** is that it requires a supply of 3V or more to stabilize the current in the transistor pair. R_1 and R_2 fulfill this function. You should set the collector voltages at about 0.8V and calculate R_1 and R_2 accordingly, bearing in mind the characteristics of the transistor chosen for the job.

One way to avoid this requirement is to provide a dc block between the two transistors and supply current to each transistor separately, while retaining the same RF circuit. In **Fig 1b**, C_1 is the dc blocking capacitor, R_1 and R_2 set the current in the common-emitter transistor, and R_3 sets the current in the common-base transistor ($I=0.4/R_3$). One advantage of this circuit, aside from the low supply voltage, is the fact that the common-emitter-stage and common-base-stage currents may be different, thus allowing both transistors to operate under optimum conditions.

The value of C_1 should be high enough to present negligible impedance when compared with the common-base input, which is usually about 50Ω. The tank circuit component values will depend on the application frequency.

Although cascode circuits are generally used for RF circuits (10 to 1000 MHz), there is no reason why you shouldn't use this circuit for other frequency bands such as audio. Using this circuit, a supply voltage of less than 1V is adequate to ensure constant currents, despite varying transistor characteristics. The circuit's RF performance is not affected by these altered biasing arrangements. **EDN BBS /DI_SIG #1129** EDN

To Vote For This Design, Circle No. 749

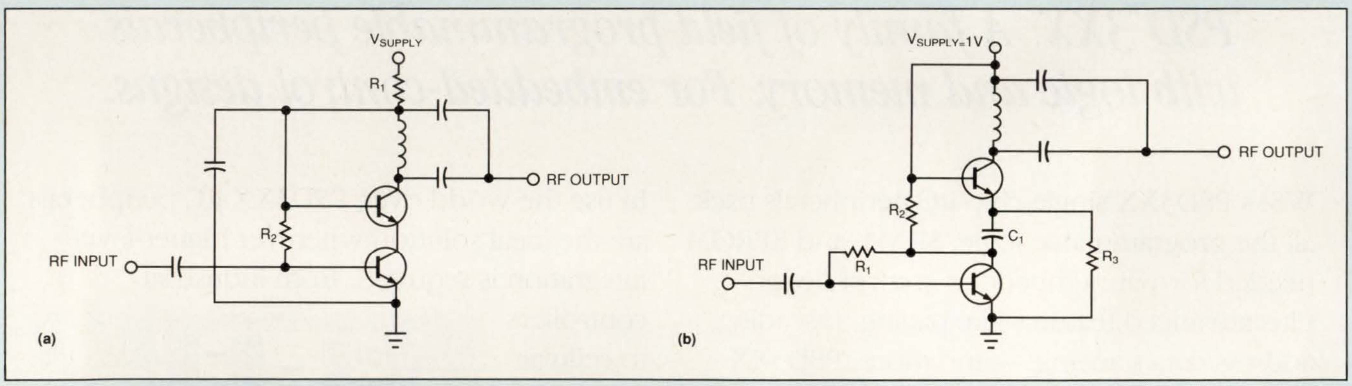


Fig 1—Capacitor C_1 provides a dc block between two transistors in (b) but retains the same RF circuit as in (a) to allow the circuit to operate from a 1V supply.

Quad DAC controls state-variable filter

Joe Buxton, Analog Devices Inc, Santa Clara, CA

The circuit in **Fig 1** uses DACs to control accurately the cutoff frequency, Q, and gain of a 2-pole state-variable filter. A state-variable filter's pole frequency is generally set by the RC combination of the individual integrator stages according to the equation

$$F_C = 1/2\pi RC.$$

Adjusting either the resistor or capacitor sets the frequency. Previous digital-control methods replaced the resistor with a DAC and relied on the DAC's changing internal resistance to vary the frequency. Although this method works, the absolute value of the DAC's internal resistance can vary as much as ±50% from device to device, translating into a ±50% error in the

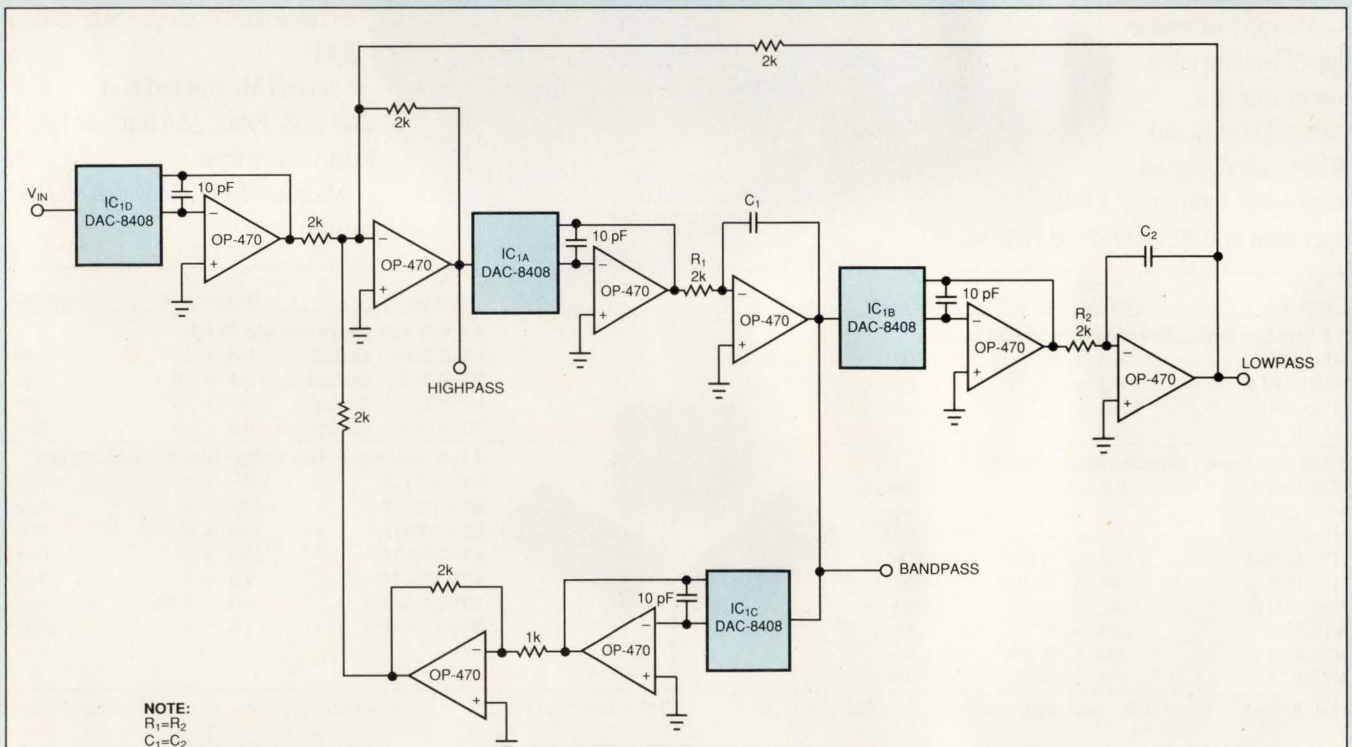
cutoff frequency. These large variations make mass production not feasible. Hand selecting the capacitors or screening the DAC resistances is time consuming and costly.

The method in **Fig 1** eliminates the dependence on DAC resistance tolerance. This circuit exploits the inherent accuracy of the DAC by operating it in a standard voltage-output multiplying configuration. Adjusting DAC IC_{1A} changes the signal amplitude across R_1. Thus, the DAC's attenuation multiplied by R_1 determines the amount of signal current that charges the integrating capacitor, C_1. For example, increasing the attenuation lowers this current by decreasing the amount of signal across R_1. This frequency control is accurate within the resolution of the DAC and follows the equation for F_C given in the figure. Note that both DACs IC_{1A} and IC_{1B} should have the same digital code and that $R_1=R_2$ and $C_1=C_2$.

Using the equation for F_C in the **figure**, with $R_1=R_2=2\ k\Omega$ and $C_1=C_2=1000$ pF, the filter's maximum cutoff frequency is 80 kHz. This maximum occurs when both IC_{1A} and IC_{1B} are at full scale. Using the equation, the 1-LSB case sets the minimum frequency at 1/256 of the maximum, or approximately 310 Hz. Network-analyzer plots closely agree with both of these values. Setting all the DAC bits to zero is the one prohibited case. This condition breaks the feedback loop and causes the op-amp outputs to swing to the power-supply rails.

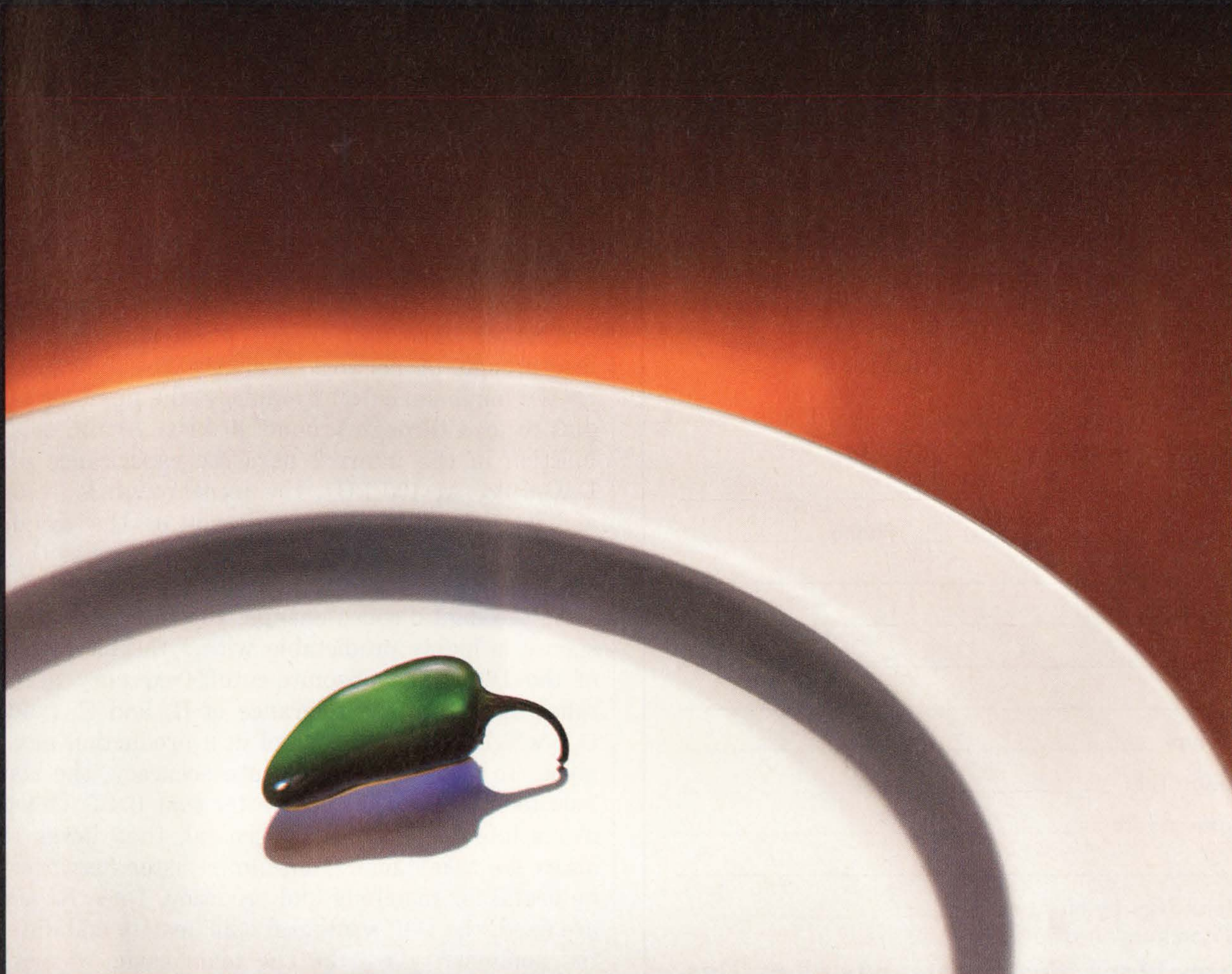
The Q control adjusts the amount of signal at the bandpass node that the circuit feeds back to the input-summing node. Adjusting the attenuation of IC_{1C} changes the Q. As with the frequency control, this adjustment does not rely on the absolute value of the DAC's ladder resistance, but rather on the internal resistance ratios. Adjusting IC_{1C} changes only the Q, as per the second equation in **Fig 1**. Lastly, adjusting IC_{1D} changes the filter's gain according to the gain equation in **Fig 1**, which is the normal operating condition for a DAC.

Bandwidth and loop stability are important considerations for state-variable filters. Too much phase shift in the feedback loop, caused by the multiple op amps, may result in oscillations. Stability is even more important when including the DACs because they add phase shift. For the DAC-8408, as for most CMOS DACs, the internal ladder resistance, in combination with parasitic capacitances, limits the bandwidth to approximately 500 kHz. Also, the full-power bandwidth of the circuit further limits the frequency for large-level input



$$F_C=\frac{1}{2\pi R_1C_1}\left(\frac{D_1}{256}\right) \qquad Q=\frac{R_3}{R_4}\left(\frac{256}{D_2}\right) \qquad GAIN=\frac{R_5}{R_6}\left(\frac{D_3}{256}\right)$$

Fig 1—Because this digitally programmable state-variable filter does not depend on the absolute DAC internal resistance, its pole frequencies are highly predictable and easy to control.



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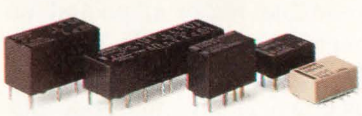

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CIRCLE NO. 118

Design Entry Blank

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I hereby submit my Design Ideas entry.

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Entry blank must accompany all entries. Design entered must be submitted exclusively to EDN, must not be patented, and must have no patent pending. Design must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested. Fully annotate all circuit diagrams. Please submit software listings and all other computer-readable documentation on a 5¼-in. IBM PC disk in plain ASCII.

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In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

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ISSUE WINNER

The winning Design Idea for the February 17, 1992, issue is entitled "Miniature power supply works off line," submitted by David A Johnson of David Johnson and Associates (Littleton, CO).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now,** by circling the appropriate number on the reader inquiry card.

signals, due to the effects of charging the feedback capacitors. The maximum frequency of the filter should be kept below 100 kHz to ensure stability with 20V p-p inputs. Using the values in **Fig 1**, the maximum frequency is 80 kHz, and the circuit is stable.

Another important frequency consideration is ac feedthrough. A network analyzer plot indicates that for the minimum cutoff frequency, the input signal begins to feed through around 40 kHz. Again, this is a function of the internal parasitic capacitance of the DAC-8408. At 100 kHz, the feedthrough is −75 dB, and it rises at 20 dB per decade as the frequency increases. This rise continues until it reaches the OP-470's 6-MHz bandwidth.

As the digital codes change, the filter's relative response is highly predictable within the bit resolution of the DAC. The absolute-cutoff-frequency accuracy relies mainly on the tolerance of R_1 and C_1 (and R_2, C_2), which is easy to control in a production environment. To achieve 8-bit absolute accuracy, the component tolerances need to be better than 0.4%. However, if absolute accuracy is not critical, then lower tolerances are acceptable. Thin-film resistor networks can be useful for matching and accuracy. Once R_1 and C_1 are fixed, the DAC's integral nonlinearity and differential nonlinearity will be the main cause of error in setting the filter's response. The accuracy is not limited to 8 bits. Using a 12-bit or higher multiplying DAC increases the precision and frequency-control range.
EDN BBS /DI_SIG #1127 EDN

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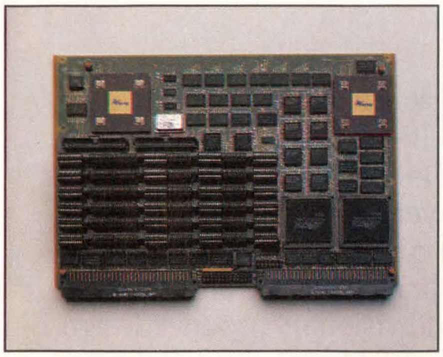
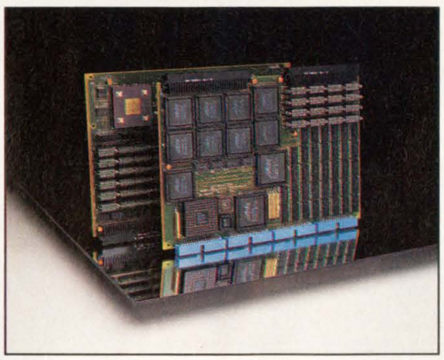


400 MOPS FOR 6U VMEbus SYSTEMS

This 6U VMEbus board performs 400 million operations per second and is optimized for frequency domain processing such as FFTs and finite impulse response (FIR) filters using fast convolution. The FDaP features a private 32-bit, 20 MHz high-speed data I/O bus and extensive double buffering for continuous processing of real-time data. An additional 32-bit complex output provides phase/magnitude data. The a66540 is available in 25 MHz and 40 MHz versions. A single 40 MHz version can execute a 1K point FFT in 132.7 µs and a 64K point FFT in 13.1 ms. These times are nearly halved for real input. Multiple FDaPs can be cascaded to achieve almost linear improvement in FFT performance. Plug 400 MOPs into your system by calling **array** Microsystems' Hotline: 719-540-7999.



CORNERTURN PROVIDES QUANTUM LEAP IN 2D IMAGE PROCESSING PERFORMANCE

The a66545 Cornerturn™ board, used in conjunction with the a66540 FDaP board for real-time two-dimensional image processing, is the first capable of processing an entire 256 x 256 pixel frame of image data in 15.2 milliseconds. This equates to a continuous, real time rate of 65 frames per second. For 512 x 512 images, the board set transforms images in 71 milliseconds, or 14 frames per second. Designed for medical imaging, radar, sonar, machine vision, and other real-time 2D image processing applications, the board set features performance of 400 MOPS at a clock rate of up to 40 MHz. The Cornerturn accepts 32-bit complex I/O data through 10 MHz double-buffered external I/O connectors or through the VMEbus and stores it in one of four on-board frame store memory buffers. For technical assistance, call **array** Microsystems' Hotline: 719-540-7999.

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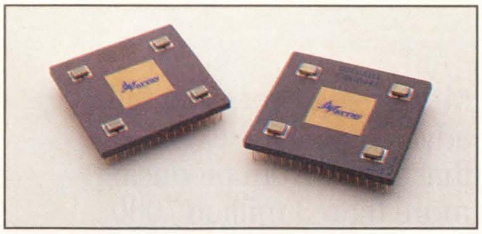
arraysoft, a complete DSP software development system supporting **array** Microsystems' a66 Family of Products, provides a menu driven user interface allowing easy access to a suite of powerful development tools at the click of a mouse. This development system features a DaSP/PaC code generator, assembler, disassembler, window generator, full DaSP/PaC program control, on-screen display of data, and board-level diagnostics. For technical information or original program assistance, call **array** Microsystems' Hotline: 719-540-7999.



THE DaSP/PaC CHIPSET:

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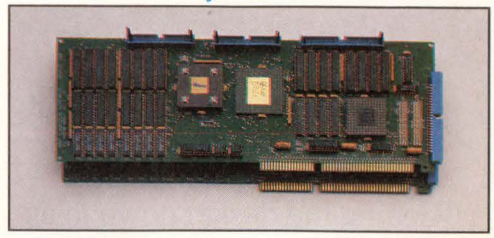
The Digital array Signal Processor (DaSP) executes 16 high-level instructions, including FFT butterflies, windowing, complex multiplies, and general-purpose functions. The Programmable array Controller (PaC) manages the entire system, including address generation for the DaSP and memory, and I/O up to 80 MHz. Using a single chipset, for example, a 1024 point FFT requires only 12 instructions and can execute in only 131 µsec; a complex FIR filter, using 28 instructions, processes at a 2.3 MHz rate. For even higher performance, you can cascade the chipset. Both utilize a 144-pin PGA format and are available in 30 and 40 MHz versions. To receive complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



PC-FDaP PERFORMS 250 MOPS!

The a66550 Frequency Domain array Processor (FDaP) brings high performance FFT processing to any PC-AT compatible computer. The two board set will fit into two full size PC-AT slots, operate on the 16 bit PC-AT (ISA) bus, and allow real or complex input from either the high speed connectors on the back panel or from the PC-AT bus. The FDaP accommodates an optional complex I-and-Q to magnitude-and-phase converter for post-FFT processing. Available in two memory configurations, the a66550 handles complex FFTs up to 32K points and real FFTs up to 64K points. The a66550 can compute a 1024 point complex FFT in just 210 µs. For complete technical information, call **array** Microsystems' Hotline: 719-540-7999.

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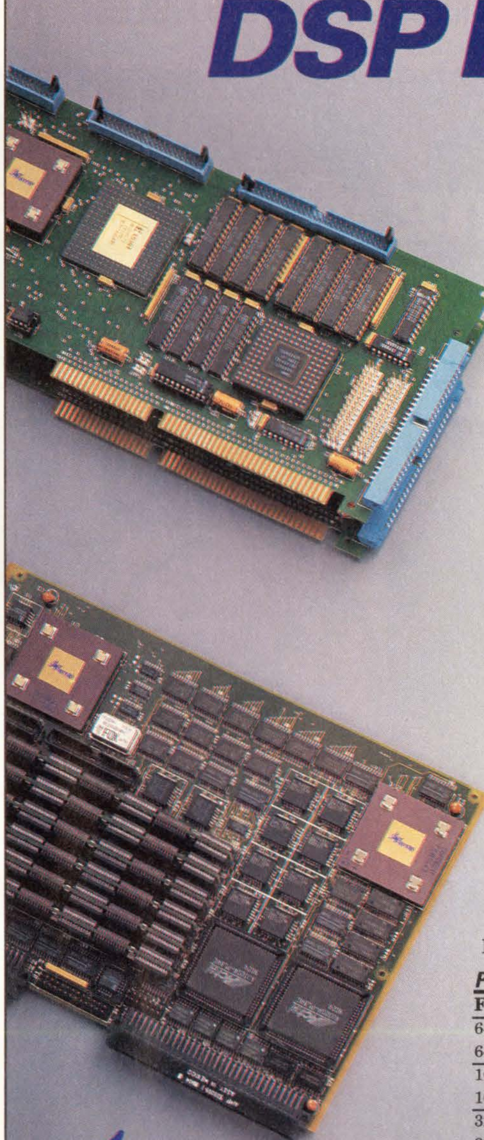


PC-AT DSP

1K FFT/126µs

DSP engine for the 16-bit PC-AT Industry Standard Architecture (ISA) bus

Performance Benchmarks

FFT size	a66550/32K @25MHz
64 Real	7.2 µs
64 Complex	10.9 µs
1024 Real	125.9 µs
1024 Complex	209.9 µs
32K Real	5.90 ms
32K Complex	10.49 ms
64K Real	15.73 ms
64K Complex	N/A

VME DSP

1K FFT/79.6µs

DSP engine for industry-standard VMEbus

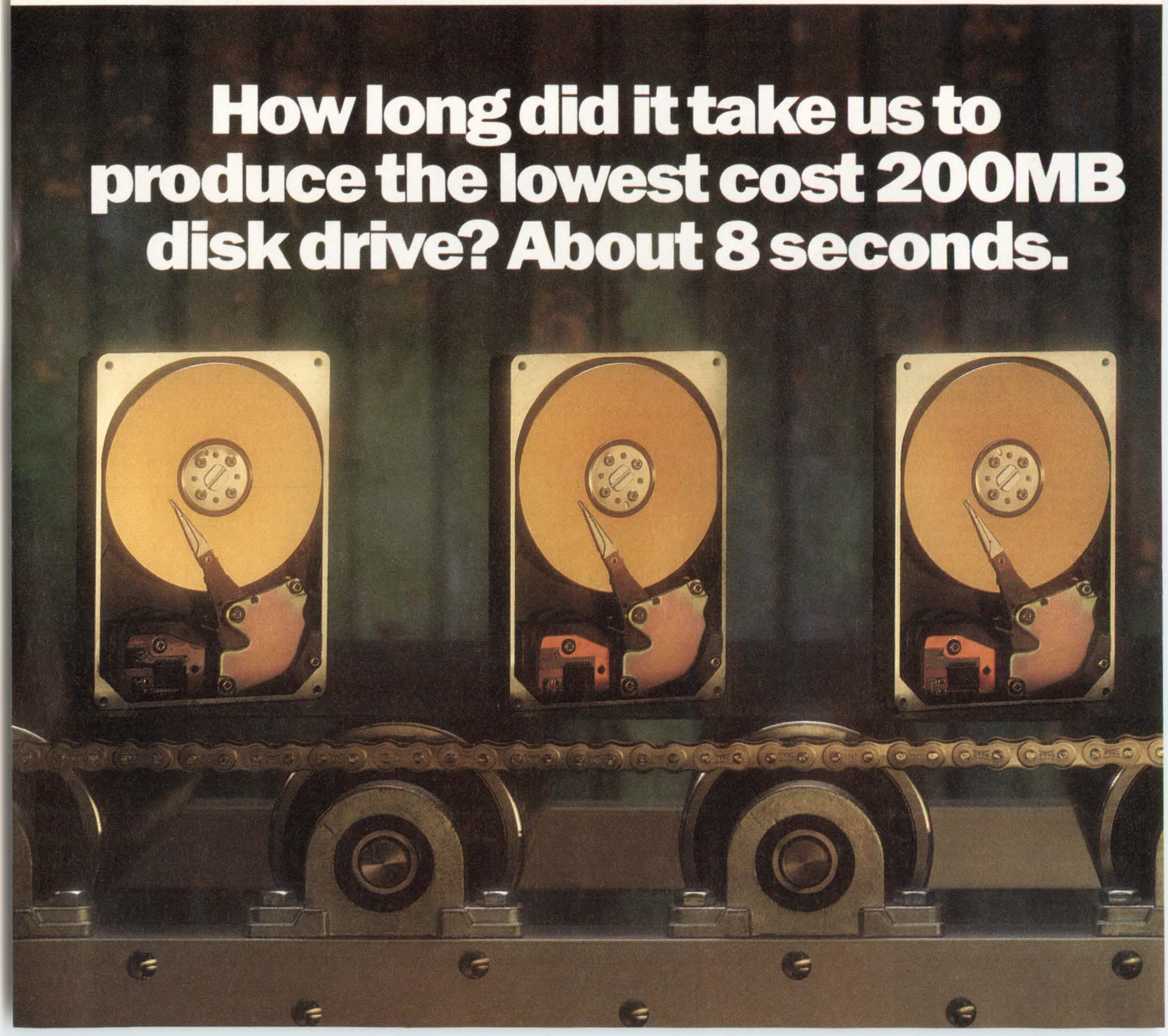
Performance Benchmarks

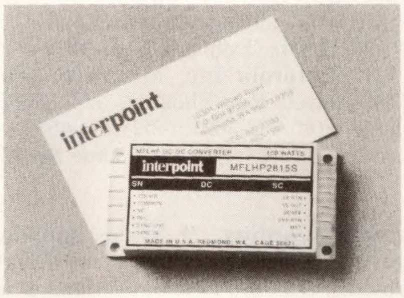
FFT size	a66540A @40MHz	a66540A Cascade Sys.
64 Real	5.1 µs	2.9 µs
64 Complex	5.0 µs	3.7 µs
1024 Real	79.6 µs	29.6 µs
1024 Complex	132.7 µs	59.1 µs
32K Real	3.69 ms	0.91 ms
32K Complex	6.56 ms	1.82 ms
64K Real	7.37 ms	1.82 ms
64K Complex	13.11 ms	3.64 ms

array™ MICROSYSTEMS

Call the DSP Hotline: 1-719-540-7999

1420 Quail Lake Loop, Colorado Springs, CO 80906


How long did it take us to produce the lowest cost 200MB disk drive? About 8 seconds.



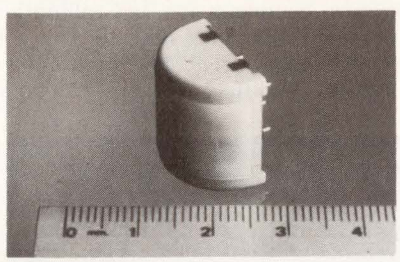
DC/DC converters. MFLHP Series dc/dc converters provide as much as 100W of output power and come in a 2.5×1.5×0.38-in. case. The units' power density equals 70W/in^3. The units employ PWM techniques and feature a −55 to +85°C operating range. The converters accept inputs of 19 to 40V—a range that complies with the conditions defined by MIL-STD-704. The series includes single- and dual-output models with levels of 5, 12, 15, ±12, and ±15V; operating efficiencies range to 84%. $699 (100). **Interpoint Corp,** Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 882-1990. **Circle No. 358**

Rotary switches. P and P65 Series rotary switches are fully sealed and offer BCD, BCD-complement, hexadecimal, and hexadecimal-complement outputs. Both lines are available with straight or right-angle mounting options. The units have a 10,000-operation lifetime and contacts rated for 400 mA at 24 Vdc. P101, $1.96; P65101, $1.79 (1000). **MORS/ASC,** Box 544, Wakefield, MA 01880. Phone (617) 246-1007. FAX (617) 245-4531. **Circle No. 359**

VME chassis. This 19-in., EMI-gasket VME chassis includes mountings for a 5 ¼-in. disk drive as well as a 300W power supply. Four fans provide 300 cfm of horizontal cooling; honeycomb EMI filters are also standard on the chassis. A 5-slot VME backplane also is installed in the chassis. From $4995. **ACT/Technico,** 1 Ivybrook Blvd, Suite 180, Ivyland, PA 18974. Phone (800) 445-6194; (215) 957-9071. **Circle No. 360**

Photoelectric sensor. S18 Series photoelectric sensors feature diagnostic capabilities. Complementary outputs allow one output to be used as an alarm when sensing conditions become marginal. Retroreflective models use a corner-cube reflector to achieve a 2m range; opposed mode models use separate emitter and receiver pairs to achieve a sense range of 20m. A diffuse-mode model has a 10-cm sensing range. $36. **Banner Engineering Corp,** Box 9414, Minneapolis, MN 55440. Phone (612) 544-3164. **Circle No. 361**

Connectors. Switching DIN 96-position connectors feature integral switching capability. The switches automatically jumper the signal path when a daughter card is removed from a connector. By providing a continuous path on the backplane, the unit eliminates the need for mechanical jumpers, DIP switches, relays, or software to achieve continuous operating in serial systems. The connector can accommodate as many as 48 switches. $8 to $25 (1000). Delivery, four to six weeks ARO. **Augat Inc,** 425 John Dietsch Blvd, Attleboro Falls, MA 02763. Phone (508) 699-9800. **Circle No. 362**



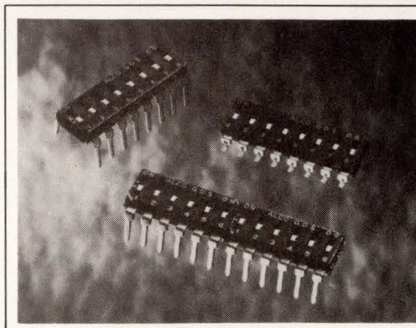
Infrared detector. The PIRL180-100 passive infrared detector features a 180° field of view. The device contains a series of detectors patterned on a ferroelectric polymer film. This array is geometrically formed and integrated with a built-in Fresnel lens. The dual-channel outputs allow for externally balanced gain and common mode rejection of unwanted signals generated by ambient temperature changes, vibration, and other noise sources. Detector, $3.96 (100,000); demonstration board, $99. **Elf Atochem Sensors Inc,** Box 799, Valley Forge, PA 19482. Phone (215) 666-3500. FAX (215) 666-3509. **Circle No. 363**

Coaxial adapter. Model PE9341 BNC male to mini-UHF female coaxial adapters operate over a dc to 4-GHz range. They feature a brass nickel-plated body, teflon insulation, and gold-plated contacts. Operating range spans −65 to +165°C. $5.95. **Pasternack Enterprises,** Box 16759, Irvine, CA 92713. Phone (714) 261-1920. FAX (714) 261-7451. **Circle No. 364**

Power supplies. CV Series power supplies come with one to five outputs and deliver 300 to 600W of power. Efficiency equals 80% typ. A power-fail monitor, thermal-shutdown monitor, TTL-logic inhibit input, and auto-ranging circuitry are available as options. From $390. Delivery, six to eight weeks ARO. **Deltron Inc,** Box 1369, North Wales, PA 19454. Phone (215) 699-9261. FAX (215) 699-2310. **Circle No. 365**

Panel meters. Series 96000 panel meters are available with RTD, thermocouple, voltage, and current inputs. Accuracies of ±1° are available. The units feature a 3 ½-digit LED readout with 0.56-in.-high characters. Thermocouple and RTD units include automatic sensor burn-out indication and a built-in analog output. $159 (OEM qty). **S-Products Inc,** 35 Kings Hwy E, Fairfield, CT 06430. Phone (203) 331-9546. FAX (203) 335-2723. **Circle No. 366**

Power supplies. 36M Series supplies have a 2000W output capability. Units feature as many as nine outputs with levels of 2 to 56V and 5 to 300A. All models conform with UL, FCC, CSA, EN, and VDE safety and EMI requirements. $1622 for a 4-output model. **Qualidyne Systems Inc,** 3055 Del Sol Blvd, San Diego, CA 92154. Phone (619) 575-1100. FAX (619) 429-1011. **Circle No. 367**

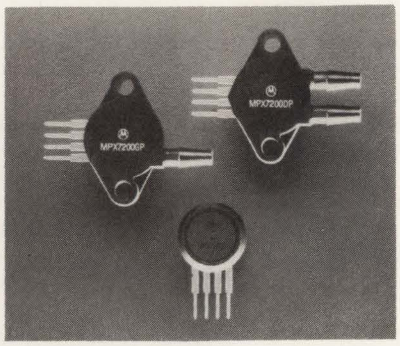


DIP switches. GDS Series DIP switches measure 0.102×0.244 in.. The units feature flush slide actuators, are end-to-end and side-by-side stackable, and come with 0.25-μm-thick gold-plated contacts. The switches employ a corner notch, which eases tape removal. Utilizing kapton tape and high-temperature polymer housings, the switches are process compatible with reflow soldering temperatures as high as 260°C. The devices are available in

2-, 4-, 6-, 8-, and 10-position models and have gull-wing or J-lead surface-mount terminations. $0.80 (10,000) for an 8-position model. Delivery, stock to 12 weeks ARO. **Augat Inc,** Box 779, Attleboro, MA 02703. Phone (508) 222-2202. FAX (508) 222-0693. **Circle No. 368**

Prototype cards. EISA prototype cards come with power and ground signals routed and distributed throughout the board. The plated-through holes are on 0.1-in. centers, and the boards have provision for installing electrolytic and bypass capacitors. Prototype card, $35; EISA extender card, $65. **Advanced Microcomputer Systems Inc,** 1321 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (305) 975-9515. FAX (305) 975-9698. **Circle No. 369**

Connectors. ODU-Bus connectors are available with as many as 180 contacts spaced on 0.050-in. centers. Models are designed for straight or right-angle mounting. The connectors can be ordered with a mix of power and signal contacts. Contact rating equals 1A for signal and 3A for power. $0.10 per mated contact (1000). **ODU USA,** 4620 Calle Quetzal, Camarillo, CA 93012. Phone (805) 484-0981. FAX (805) 484-7458. **Circle No. 370**



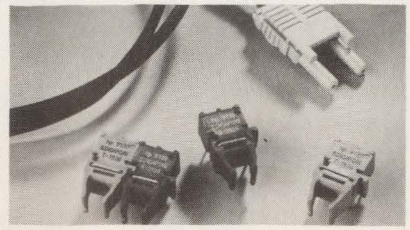
Pressure sensors. MPX7100 and MPX7200 series sensors incorporate a high-impedance input for portable low-power and battery-operated applications. The devices include on-chip temperature compensation and calibration circuitry. Both lines operate over a 0 to 85°C range. MPX7100 sensors have a 0- to 15-psi differential-pressure capability; MPX7200 units have a 0- to 30-psi differential-measurement capability. $11.50 (1000). Delivery 8 to 12 weeks ARO. **Motorola Inc,** MD Z208, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (800) 752-3621; (602) 244-4556. **Circle No. 371**

Power supplies. M Series supplies provide a 3500W output. The design provides true n+1 configurations of as many as 8 units. Standard features include overvoltage, overcurrent, and overtemperature protection, power-fail flag, remote margining, and bidirectional synchronization signals. $2495. **OPT Industries Inc,** 300 Red School Lane, Phillipsburg, NJ 08865. Phone (908) 454-2600. FAX (908) 454-3742. **Circle No. 372**

Inverter drives. TFR 600S is rated for 0.5 hp continuous, and as high as 0.75 hp for intermittent duty. The unit operates over a 0- to 400-Hz range, accepts 220V ac single-phase inputs, and has adjustable acceleration/deceleration figures of 0.2 to 4 sec. RFI filtering is provided at input and output. $295 (OEM qty). **Infranor Inc,** 45 Great Hill Rd, Naugatuck, CT 06770. Phone (203) 729-8258. **Circle No. 373**

Optical connector. FC II optical connectors are compatible with existing FC/PC connector hardware. The units feature a prepolished contact profile with a convex spherical radius. Typical insertion loss is 0.08 dB, and the typical return loss is 48 dB in single-mode versions. Single-mode model with a zirconia ferrule, $11.48 (100). **Molex Fiber Optic Interconnect Technologies Inc,** 2111 Oxford Rd, Des Plaines, IL 60018. Phone (708) 803-3600. **Circle No. 374**

Proximity sensor. Type E516P+ sensors are epoxy filled to make them compatible with NEMA Type 3, 4, 4X, 6, 6P, 11, and 13 service. Models are available for top or side sensing applications. The units are available in NO or NC switch configurations. From $164. **Eaton Corp,** Cutler-Hammer Products, 4201 N 27th St, Milwaukee, WI 53216. Phone (414) 449-6480. **Circle No. 375**

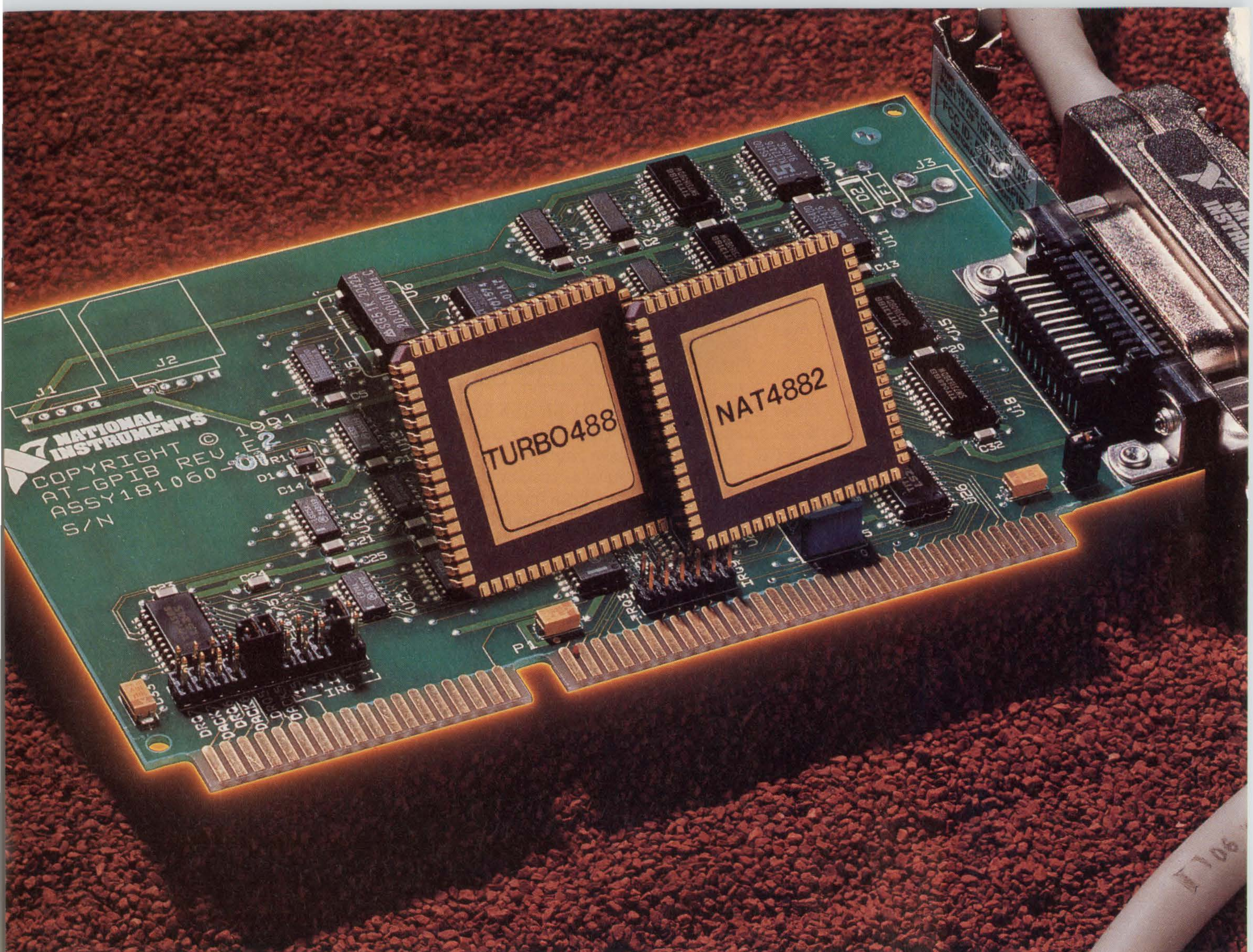


Fiber-optic data links. HFBR-15XX/25XX plastic fiber-optic transmitter and receiver pairs handle data rates of 2 to 50 Mbaud. The units have a transmission capability of 15m. Transmitter, $6.40; receiver, $10.70 (500). **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 376**

Chip carrier sockets. These JEDEC-compatible sockets are available in 20-, 24-, 32-, 68-, and 84-position models. The high-temperature insulators are compatible with all soldering processes. The beryllium copper contacts feature tin plating. All sockets are compatible with automatic insertion equipment, and they can be supplied with or without a polarizing locater. $1.15 (100) for a 20-position model. **Socket Express Inc,** 100 Jersey Ave, Bldg B-202, New Brunswick, NJ 08903. Phone (908) 247-9500. FAX (908) 247-9816. **Circle No. 377**

Power splitter. The LRPQ-700 2-way power splitter operates over 500 to 700 MHz with 0.2-dB insertion loss. The unit features 1° phase unbalance, 0.6-dB amplitude unbalance, 23-dB isolation, and 1.17:1 VSWR. The unit is rated for 1W of RF power and operates over a −55 to +10°C range. $9.95. **Mini-Circuits,** Box 350166, Brooklyn, NY 11235. Phone (718) 934-4500. **Circle No. 378**

Power supplies. PF500 Series units feature power-factor correction as well as universal-input capability. The units output 375 to 400V dc at a maximum power level of 500W. Line and load regulation equal 2 and 3%, respectively. $149 (100). Delivery stock to six weeks ARO. **Switching Systems International,** 500 Porter Way, Placentia, CA 92670. Phone (714) 996-0909. FAX (714) 996-2753. **Circle No. 379**



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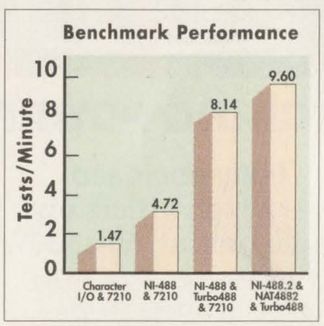

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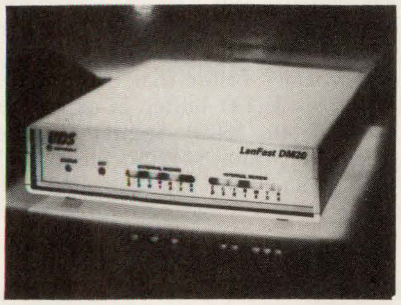
CIRCLE NO. 123

Computers & Peripherals

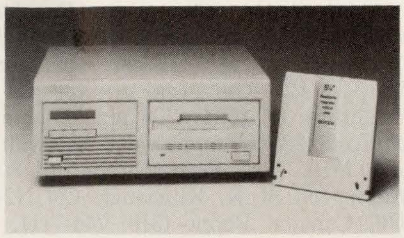


Ethernet network modem. The Lanfast DM20 dual-port modem directly connects to an Ethernet LAN and uses Novell's Netware operating system to provide remote transparent LAN access. The network modem comes with the company's Lanfast communications software, which permits dial-in or dial-out access. The modem can also transfer Netware IPX packets over ordinary phone lines to provide LAN-to-LAN communications. The modem conforms to V.32bis and V.42bis standards for 14.4 kbps data transfers. You can connect a second modem via an RS-232C port to provide simultaneous dial-in or dial-out access. $1995. **UDS Motorola,** 5000 Bradford Dr, Huntsville, AL 35805. Phone (205) 430-8000. FAX (205) 430-8208. **Circle No. 380**

3½-in. magneto-optical drive. The LD-320 provides 128 Mbytes of removable, rewritable storage for DOS, PS/2, and Macintosh computers. The drive comes in external and internal subsystem configurations. The drive has an average seek time of less than 45 msec and an embedded SCSI port. External drive, media, and software $2995. **Laser Magnetic Storage,** 4425 ArrowsWest Dr, Colorado Springs, CO 80907. Phone (719) 593-7900. FAX (719) 599-8713. **Circle No. 381**

40-MHz SPARCstation. The PM 5124 contains a 40-MHz CPU and is binary compatible with hardware and software supplied by Sun Microsystems. The workstation is available in configurations ranging from a mother board to a turnkey desktop system. The workstation supports 1024×768-pixel monitors and has a $2500 graphics accelerator option to render 2-D and 3-D models. $7205 for diskless workstation with 16 Mbytes of RAM and a color-frame buffer. **Opus Systems Inc,** 329 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 960-4040. FAX (415) 960-4001. **Circle No. 382**

RISC-based X terminal. The TekXpress XP330 Series features a 20-MHz Mips R3000 μP and a 40-MHz TI TMS43020 graphics processor. Each model has 256 kbytes of ROM and 5 Mbytes of RAM, which is expandable to 52 Mbytes. The terminals connect to TCP/IP, DECnet, LAT, and SLIP networks. Models come with 17- or 19-in. displays. $3495 to $5995. **Tektronix Inc,** Box 1000, Wilsonville, OR 97070. Phone (800) 225-5434; (503) 685-2840. FAX (503) 682-4948. **Circle No. 383**



Multifunction optical-disk drives. The Optipac 7636 and 7656 provide dual modes of operation. The units combine a magneto-optical (MO) disk drive that has 650 Mbytes of storage with either a 300- or 500-Mbyte hard-disk drive. The drives run Hewlett-Packard computers having an IEEE-488 port and running HP-UX, Basic, Pascal, RTE-A, MPE-V, or MPE-XL operating systems. The 7636, $9990; 7656, $11,190. **Bering Industries,** 246 E Hacienda Ave, Campbell, CA 95008. Phone (800) 237-4641; (408) 379-6900. FAX (408) 374-8309. **Circle No. 384**

Scramnet network adapter. Model P1600 allows 386- or 486-based computers to transfer data at 150 Mbytes/sec over the company's Scramnet fiber-optic network. The product consists of an ISA bus card and an external enclosure that houses replicated shared memory. The host can access as much as 2 Mbytes of replicated shared memory in protected mode. $6900 to $9800. **Systran Corp,** 4126 Linden Ave, Dayton, OH 45432. Phone (800) 252-5601; (513) 252-5601. FAX (513) 258-2729. **Circle No. 385**

Laserjet network-interface cards. The Etherflex cards automatically configure a Hewlett-Packard Laserjet printer for either Postscript or PCL print formats. The cards directly connect the printer to an Ethernet cable and support Novell's Netware 286/386, Netware Lite, and Apple's Ethertalk network operating systems. The cards have 10Base-T, 10Base-2, and AUI connectors. $695 to $795. **Extended Systems,** 6123 N Meeker Ave, Boise, ID 83704. Phone (800) 235-7576; (406) 587-7575. **Circle No. 386**

VMEbus DOS-compatible single-board computer (SBC). The XVME-688 VMEbus SBC runs DOS-compatible software. The board features a 25-MHz 80386SX μP and 0, 1, or 4 Mbytes of dynamic RAM (DRAM). Four SIMM (single-inline-memory-module) sockets let you add as much as 16 Mbytes of zero-wait-state DRAM. An on-board ISA bus connects to the VMEbus via an interface chip that provides slot 1 functions and bus-master capabilities. The ISA bus signals are available to add peripherals such as Ethernet and SCSI devices. The all-CMOS board operates from 0 to 65°C. Less than £1000. **Xycom Europe Ltd,** 21 Tenter Rd, Moulton Park, Northampton NN3 1AX, UK. Phone (604) 790-767. FAX (604) 790-722. **Circle No. 387**

ISA bus graphics board. The Flash-XGA modified graphics adapter board for the ISA bus has its CRTC chip replaced with an S3 GUI accelerator chip. The chip implements bitblt, line draw, image transfer, and hardware clipping functions. The board employs a bus-master coprocessor chip that accelerates ISA bus transactions using a fly-by transfer mode. In this mode, the board reads pixel data from system memory and writes the data to video memory in a single bus cycle. The board has 1 Mbyte of video RAM and supports non-interlaced displays having 1024×768 pixels and 256 simultaneous colors. $599. **Video Dynamics Inc,** 1550 Bryant St, San Francisco, CA 94103. Phone (800) 243-3527; (415) 863-3023. FAX (415) 863-2979. **Circle No. 388**

VMEbus i960 development system. The CVME962 features a 25-MHz i960 μP, 128 kbytes of static RAM, 8 Mbytes of dynamic RAM, 1 Mbyte of flash ROM or 4 Mbytes of EPROM, and an 82596 Ethernet controller. In addition, the 6U board has a master/slave VMEbus interface, two serial ports, a real-time clock, and an interrupt controller. The board supports Tartan's i960MC Ada development system. $8600. **Cyclone Microsystems,** 25 Science Park, New Haven, CT 06511. Phone (203) 786-5536. FAX (203) 786-5025. **Circle No. 389**

Computers & Peripherals

StarLAN 10 network-adapter units. The Lanpacer and Lanpacer+ connect an ISA bus computer to a 10Base-T local-area network. The Lanpacer+ provides an AUI port and operates on 16- and 8-bit buses. The Lanpacer has a 16-bit onboard architecture but operates only on an 8-bit bus. Both cards have 16 kbytes of buffer memory. Lanpacer+, $399; Lanpacer, $299. **NCR Corp,** Public Relations, Dayton, OH 45479. Phone (612) 638-7391; (908) 221-3909. **Circle No. 390**

Passive ISA bus single-board computer. The SBC386IE is a passive 16-bit ISA bus single-board computer with EISA bus connectors. The passive ISA design provides 21 ground pins compared with 4 on a standard ISA bus board. The board has a 40-MHz Chips and Technologies' Super386 μP. The board also has as much as 128 Mbytes of RAM, a 128-kbyte cache RAM, a shadow RAM, a programmable watchdog timer, and a PS/2-style keyboard. $1818. **Monolithic Systems Corp,** 7050 S Tucson Way, Englewood, CO 80112. Phone (303) 790-7400. **Circle No. 391**

14-in. color monitor. The ECM 1420 is a super-VGA color monitor that has automatic horizontal-scan rates from 30 to 40 kHz and vertical-scan rates from 45 to 90 Hz. The 14-in. monitor has a resolution of 1024×768 pixels, a dot pitch of 0.28 mm, and a video bandwidth of 40 MHz. $795. **Electrohome Ltd,** 809 Wellington St N, Kitchener, ON N2G 4J6, Canada. Phone (519) 744-7111. **Circle No. 392**

VMEbus-to-HSD link adapter. The VMEHSD provides a path between a VMEbus system and a 32-bit peripheral that employs the Encore High-Speed-Data (HSD) protocol. The 6U board provides a communications link that is at least 5 times faster than Ethernet. A 1k×32-bit FIFO buffer is expandable to 4k×32 bits. $6650. **Applied Data Sciences Inc,** Box 814209, Dallas, TX 75381. Phone (214) 243-0113. FAX (214) 243-0217. **Circle No. 393**

3½-in. hard-disk drive. The ST3243A stores 214 Mbytes on a 3.5×1-in. form factor. The drive has an average seek time of 16 msec and features a multisegmented, adaptive 128-kbyte cache buffer. The drive operates in DOS-compatible computers and includes a 128-bit error-correction code. $395. **Seagate Technology,** 920 Disc Dr, Scotts Valley, CA 95066. Phone (408) 438-6550. **Circle No. 394**

Micro Channel Architecture graphics controller. The UDC-8000-TI has a Type 5 form factor for use in IBM's RISC/6000 and PS/2 Models 90 and 95 computers. This latest member of the Piranha family features a TI TMS34020 graphics controller and has an option for a TMS34082 floating-point unit. The board drives displays as large as 1600×1280×8 bits and provides 4 bits for independent overlay planes. $4695. **Univision Technologies Inc,** 3 Burlington Woods, Burlington, MA 01803. Phone (617) 221-6700. **Circle No. 395**

ISA bus motion-control card. The PMAC-Lite is a single ISA bus board that employs a DSP chip to control as many as four axes of motion simultaneously. A 16-bit D/A converter provides servo updates at 55 μsec/axis. The board controls brushless dc, ac induction, variable reluctance, and stepper motors. The board accepts encoder rates as fast as 20 MHz and performs multiaxis interpolation and synchronization. $2499. **Delta Tau Data Systems,** 21119 Osborne St, Canoga Park, CA 91304. Phone (818) 998-2095. FAX (818) 998-7807. **Circle No. 396**

33-MHz 80486 PCXI module. The PX1261 is an EISA CPU module for PCXI (PC extended for industry) computers. The module has as much as 64 Mbytes of RAM and controls six 32-bit EISA master slots and nine EISA slave slots. The module can transfer data at 33 Mbyte/sec using DMA burst mode. $4995. **Rapid Systems Inc,** 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX (206) 548-0322. TLX 265017. **Circle No. 397**

VGA-to-NTSC/PAL converter. Model 701 attaches to a VGA-port connector on a Notebook or laptop computer. The unit converts VGA signals into NTSC/PAL format for display on a standard TV set using an S-video or composite-video port. The unit measures 2×3.5×1-in. and operates from a 110V 60-Hz or 220V 50-Hz wall-mount supply. $399. **Telebyte Technology Inc,** 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; (516) 423-3232. FAX (516) 385-8184. **Circle No. 398**

Embedded DOS-compatible computer module. The Little Board/386SX is a 5.75×8-in. module that provides all the functions of a full-sized 80386SX mother board. The 5W module operates from a single 5V supply and accommodates 16 Mbytes of RAM. The module has two serial ports, a parallel port, a floppy-disk drive controller, and an IDE hard-disk drive port. $720 (100). **Ampro Computers Inc,** 990 Almanor Ave, Sunnyvale, CA 94086. Phone (408) 522-2100. FAX (408) 720-1305. **Circle No. 399**

Operator microterminals. The CTM-380 and CTM390 have a 1-line×24-character display that is visible in low-light environments. The units have either a 51-key alphanumeric keypad or a 23-key numeric keypad. The units weigh 1.7 lbs and have an ABS plastic case that measures 9×5×1.5 in. The CTM380 communicates with a host via an RS-232C port; the CTM390 uses an RS-422 port. $795 (OEM qty). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 400**

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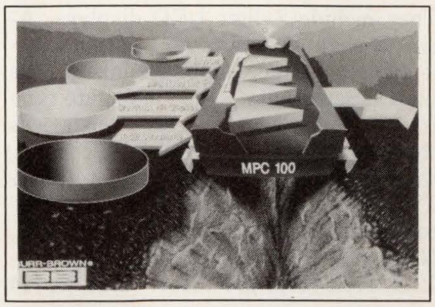
CIRCLE NO. 125

Integrated Circuits



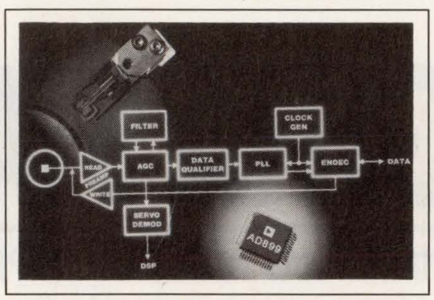
4:1 video multiplexer. The MPC100 multiplexer contains four identical open-loop buffer amplifiers sharing a common output connection. It features a large-signal bandwidth of 100 MHz, crosstalk of −60 dB at 30 MHz, and differential gain and phase errors of 0.05% and 0.01°, respectively. Second- and third-harmonic distortion is −53 and −67 dBc, respectively. In 14-pin DIPs and SOIC packages, from $7.20 (100). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 419**

Microprocessor supervisory circuits. Drawing a quiescent current of 200 μA typ, the MAX705 and MAX706 reduce the component count and circuit complexity for monitor power-supply and battery functions in μP systems. They provide four key functions: a reset output during power-up, power-down, and brownout conditions; a watchdog timer whose output goes low if its input is not toggled within 1.6 seconds; a 1.25V threshold detector for power-fail warning and low-battery detection; and an active low manual-reset input. In 8-pin DIP and SO packages, $1.02 (25,000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 420**

Video ADC. The SP973T8 A/D converter features 8-bit flash performance and needs no S/H circuit. An 8-bit D-type latch ensures that the TTL/CMOS-compatible outputs are accurately registered. The ADC operates from a 5V supply and offers conversion rates of 30 MHz or greater. Input bandwidth is 70 MHz. An internal bandgap regulator ensures low dc drift over a wide temperature range. The ADC is available in an 18-pin surface-mount package. $8.31 (1000). **GEC Plessey Semiconductor,** Box 660017, Scotts Valley, CA 95067. Phone (408) 438-2900. **Circle No. 421**

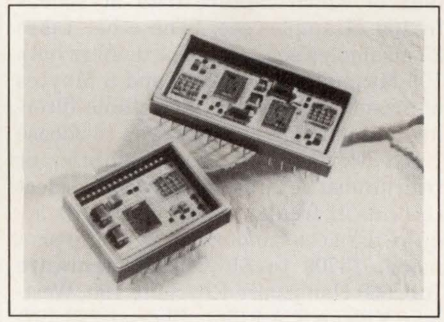
Linear active filters. The D70 series of fixed-frequency linear, active DIP filters combine small size and high performance. These lowpass filters are available in both Bessel and Butterworth configurations in 4-, 6-, and 8-pole models. Features include a 100-dB S/N ratio, −90-dB distortion, and user-specified corner frequencies between 500 Hz and 50 kHz. From $19 (4-pole filters) to $49 (8-pole filters) (10,000). **Frequency Devices,** 25 Locust St, Haverhill, MA 01830. Phone (508) 374-0761. FAX (508) 521-1839. **Circle No. 422**

Smart-power IC for car mirror. Designed for use with external rear-view mirrors, the L9946 IC drives the two motors used for orientation of a car mirror—the motor that "folds" the mirror for maneuvering and the defogging heating element. The chip contains four DMOS power stages: two 1A and two 4.75A half-bridge drivers plus a 4.75A high-side driver and control logic to achieve the desired motion. $3.50 (25,000). **SGS-Thomson,** 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290. **Circle No. 423**



Disk-drive read-channel IC. The AD899 incorporates all elements of a hard-disk-drive read channel into a single IC. It provides signal conditioning, data qualification and synchronization, RLL (1,7) data encoding/decoding, and write precompensation. To support constant-density recording, the 5V device includes a frequency synthesizer, a programmable filter, and a programmable center frequency for the data synchronizer. A servo demodulator enables embedded-servo applications. In 52-pin plastic quad flatpack, $10 (OEM qty). **Analog Devices,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-2210. **Circle No. 424**

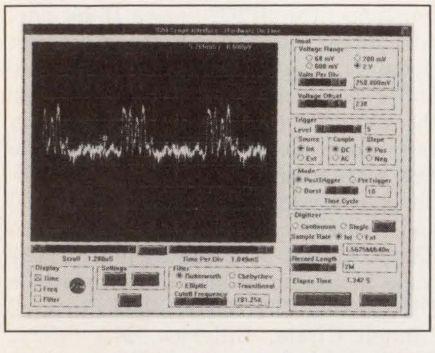
Dual 16-bit DACs. The SP9320 and SP9321 dual 16-bit DACs feature data readback for self-test and calibration functions. The SP9320 has a 16-bit parallel input; the SP9321 has a bidirectional 8-bit input. All inputs are double buffered. Each DAC has an input for the required reference voltage, which can range from −25 to +25V. The DACs are available in 14-, 15-, and 16-bit linearity grades, and in commercial and military temperature ranges. The 28-pin SP9320 and the 24-pin SP9321 come in plastic or side-brazed ceramic DIPs. From $32 (1000). **Sipex Corp,** 22 Linnell Circle, Billerica, MA 01821. Phone (508) 667-8700. FAX (508) 667-8310. **Circle No. 425**



16-bit synchro-to-digital converters. The SDC-14550 series of S/D converters feature programmable resolutions of 10, 12, 14, or 16 bits. They operate from a single 5V supply and comply with MIL-STD-1772 and MIL-STD-883C. Input-frequency ranges are either 47 Hz to 5 kHz or 360 Hz to 5 kHz. The parallel 16-bit digital outputs are TTL/CMOS compatible. They are available in a 1.5×0.78×0.21-in., 34-pin ceramic package. From $400 (1-9). **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 383. FAX (516) 567-7358. **Circle No. 426**

Wireless communications chips. The PMB2200 transmitter and PMB2400 receiver comply with the Cellular Telecommunication Industry Association IS-54 standard for digital wireless systems in the US and with the Groupe Speciale Mobile standard in Europe. The PMB2200 converts the baseband signal into modulated RF carrier frequencies in the 700-MHz to 1-GHz range. The PMB2400 includes a heterodyne receiver and demodulator that convert the received RF signal to the IF band. PMB2200 20-pin SOIC package, $7.85; PMB2400 24-pin SOIC package, $7.85 (1000). **Siemens Components Inc,** 2192 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4536. **Circle No. 427**

Test & Measurement Instruments



PC-based 100-Msample/sec DSO. The SWI-7100 series is a family of five 8-bit-resolution ISA bus DSO boards, four of which capture data at speeds to 100 Msamples/sec. (The other takes 25 Msamples/sec.) One board offers both 100-Msample/sec capture and 8 Mbytes of waveform memory. Selectable filtering of input signals allows you to choose Butterworth, Chebychev, elliptic, or transitional filters; you can also select the cut-off frequencies. The boards acquire data continuously or in single-shot mode. $5700 to $16,000. **Systemware Inc,** 660 Hampshire Rd, Suite 100, Westlake Village, CA 91361. Phone (805) 497-9603. FAX (805) 494-9719. **Circle No. 401**

Series systems for handling ICs. The Promaster 2000 programs, tests, and labels DIP ICs. The Promaster 3000 performs the same functions on both surface-mount and DIP ICs. The Promaster 7000 is similar to the 3000, but substitutes laser marking for labeling. Both the 3000 and 7000 are available in models for 44- and 88-pin surface-mount devices. $63,915 to $124,645. Delivery, eight weeks ARO. **Data I/O Corp,** Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 881-6856. **Circle No. 402**

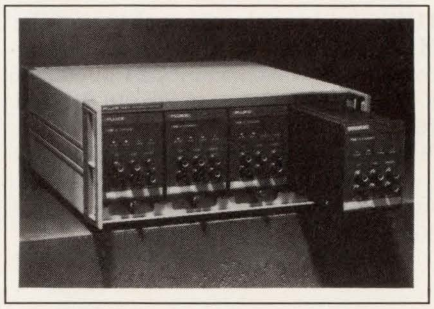
Probe arms for wafer analysis systems. The PPA-Series of probe arms allows the vendor's wafer-analysis systems to accommodate devices with nonplanar mounting surfaces. The arms allow a $\pm 5°$ adjustment. $950. **Cascade Microtech Inc,** 14255 SW Brigadoon Ct, Beaverton, OR 97005. Phone (503) 626-8245. **Circle No. 403**

Low-cost 1- and 2-GHz counters. The $330 B-1000 and the $425 B-2000 operate to 1 and 2 GHz, respectively. They include 8-digit LED displays, A- and B-channel inputs and outputs, selectable ac or dc coupling, and lowpass filters. Sensitivity is 0.25 mV; gate time is 0.01 to 10 sec; trigger level is less than 3.5 mV. Modes include A/B ratio, time interval, period A, and totalize. The timebase uses a temperature-compensated crystal. **Protek,** Box 59, Norwood, NJ 07648. Phone (201) 767-7242. FAX (201) 767-7343. **Circle No. 404**

Universal production-automation software. PC-based Tasklink control systems for handling and programming ICs, including automated device handlers and gang programmers. You establish files for each programming operation. The files specify such parameters as device type, labeling, and verification criteria. You can select devices from menus by manufacturer or type, and you can use wild-card characters when describing groups of devices. $1795; with one of the vendor's programmers, $1295. **Data I/O Corp,** Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 881-6856. **Circle No. 405**

2-channel, 2-Gsample/sec DSO. The 7200A modular unit accepts several types of plug-ins, including one that takes 1 Gsample/sec on two channels or 2 Gsamples/sec on one. By using two of these plug-ins, the scope can simultaneously sample two channels at 2 Gsamples/sec. You can order the plug-ins with 1-Msample waveform memories. The mainframe includes an 840×512-pixel color display. Mainframes, from $13,000; plug-ins, from $17,500. **LeCroy Corp,** 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 578-6011. FAX (914) 578-5985. **Circle No. 406**

Voltage-reference standard. The 734A consists of four mechanically and electrically independent plug-in standards in an enclosure that mounts in an equipment rack. Each standard provides 10 and 1.018V outputs that vary by no more than ±0.3 ppm/month and ±2 ppm/year. The standards include batteries that power them for 72 hours in the absence of ac power (144 hours optional). In normal operation, you establish a reference by comparison among three of the standards. You use



the fourth unit to transfer the standard reference value to other locations. $12,650. Delivery, 90 days ARO. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. **Circle No. 407**

Lowpass elliptic filter and amplifier. The 30A plugs into the vendor's 3905B and 3916B programmable filter-system chassis. As a filter, the board has tunable cutoff frequencies from 1 Hz to 99 kHz with a slope of 115 dB/octave. You can select a single-ended or differential input configuration, prefilter gains to 40 dB, and postfilter gains to 20 dB. As an amplifier, the bandwidth is 1 MHz with gains to 60 dB in 10-dB steps. $1345. **Krohn-Hite Corp,** 255 Bodwell St, Avon, MA 02322. Phone (508) 580-1660. FAX (508) 583-8989. **Circle No. 408**

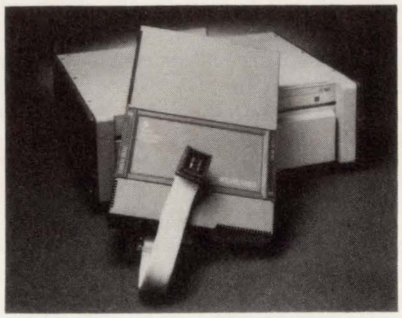
Gigabit error-rate test system. The Model 110/210 tests digital communications links from 10 Mbps to 1.1 Gbps. The system, which consists of two 15-lb units, produces three digital patterns, provides adjustment of clock and data phasing, permits insertion of errors, performs four error calculations, and includes an IEEE-488 interface. You can select sequence lengths of 2^7-1, $2^{15}-1$, and $2^{23}-1$. $29,500. **Broadband Communication Products Inc,** 17 E Hibiscus Blvd, Suite 210, Melbourne, FL 32901. Phone (407) 984-3671. FAX (407) 728-0487. **Circle No. 409**

3-axis elf milligauss meter. The Model 70 meter measures extra-low frequency (40 to 600 Hz; 2 kHz optional) magnetic fields from 0.1 to 1999 milligauss and provides a 3-axis vector-

magnitude display. It has a 3½-digit LCD and operates for 30 hours from a 9V alkaline battery. $450. **Teslatronics Inc,** 1 Progress Blvd #45, Alachua, FL 32615. Phone (904) 462-2010.
Circle No. 410

Mass-storage and data-logging system. The TD100 unit attaches to the top of the vendor's TDS 500, 600, and 800 series DSOs. It adds a 1.44-Mbyte, 3½-in. floppy-disk drive and a 50-Mbyte hard disk, both of which you control from menus displayed on the DSO screen. The unit lets you store dozens of complete scope front-panel setups and save displays in formats compatible with popular MS-DOS desktop publishing packages. It also lets you save waveform records in formats compatible with popular MS-DOS spreadsheets. $1995. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 411**

Emulators for MC68HC11K4. Coupled with the vendor's PC-hosted EMUL68-PC, the Pod-11KE and Pod-11KS enable in-circuit emulation of the MC68HC11K4, a 4-MHz microcontroller (μC) that includes 24 kbytes of EPROM, 640 bytes of EEPROM, and 768 bytes of RAM. The μC supports 1 Mbyte of external memory. Pods, $1100 to $1500. **Nohau Corp,** 51 E Campbell Ave, Campbell, CA 95008. Phone (408) 866-1820. FAX (408) 378-7869.
Circle No. 412

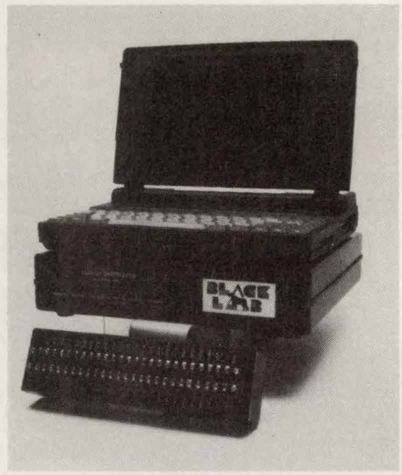


Development system for 80C186EB. The 80C186EB development system is based on the vendor's ES 1800 emulator. It supports transparent, nonintrusive emulation at the processor's full clock speed. Because the trace buffer stores every write and verify, memory locations of chip selects, timers, and DMA transfers survive target-system crashes. The system can include Genprobe II V3.0, a windowed source and assembly-level debugger. $11,100 to $17,500. **Applied Microsystems Corp,** Box 97002, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. FAX (206) 883-3049. TLX 185196.
Circle No. 413

Intelligent testing system for optical fibers. The FOT-900 series incorporates what the vendor calls a Fastest feature that permits a pair of units to measure the end-to-end attenuation of fibers at one of two wavelengths in less than 10 sec with a single key press. Using instruments equipped with appropriate options, back-reflection tests require 15 sec. The units, which receive power from ac, rechargeable batteries, or nonrechargeable batteries, operate at 850, 1300, and 1550 nm. $1550 to $12,000. **Exfo EO Engineering Inc,** 485 Godin, Vanier QC, G1N 3Y2, Canada. Phone (418) 683-0211. **Circle No. 414**

Jitter/wander analyzer. The SJ-300 is a portable instrument for testing networks that conform to the SONET (synchronous optical network) and SDH (synchronous digital hierarchy) standards. The unit continuously displays p-p and rms jitter. You can set the tester so that each time the phase error exceeds a threshold value that you specify, it records the date and time of the occurrence. The instrument also records the maximum time-interval error and $\sqrt{\text{time}}$ variation. From $27,950. Delivery, 30 to 60 days ARO. **Microwave Logic,** 20 Cummings Rd, Tyngsboro, MA 01879. Phone (508) 649-6099. FAX (508) 649-4722.
Circle No. 415

Software for testing "panelized" pc boards. HP Paneltest, which runs on the vendor's 3070 systems, overcomes difficulties that crop up when you test groups of small pc boards in panels. Partial panels and defective boards cause problems with software designed for testing large boards. Compared with more general packages, the specialized software reduces the time required for programming small-board tests. $15,000. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 416**



Notebook PC-based data-acquisition system. Black Lab measures 2.5×12×11 in., weighs 7 lb, and connects to the RS-232C port of any PC, including notebook computers. It takes 1000 samples/sec on each of 16 channels and permits other sampling rates from 1/minute to 20k/sec. The unit accepts ac power, and if appropriately equipped runs from internal or external 12V dc sources. AC-powered version, $1950. **Analog Interfaces Inc,** Box 3448, Alliance, OH 44601. Phone (216) 821-5800. FAX (216) 821-7625. **Circle No. 417**

160-channel analog logic analyzer. The S160 PC-hosted analog logic analyzer can have from 16 to 160 channels. It's a cross between a DSO and a logic analyzer. Like a DSO, it resolves signal levels other than just logic 1 and logic 0 (16 levels in single-shot mode; 64 levels for repetitive signals). Like a logic analyzer, it offers complex multilevel triggering. In single-shot mode, the system captures data at 200 Msamples/sec on all channels, 400 Msamples/sec on half the channels, or 800 Msamples/sec on a quarter of the channels. $19,950. Delivery, 90 days ARO. **Biomation** 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 934-2466; (408) 988-6800. FAX (408) 988-1647. **Circle No. 418**

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CIRCLE NO. 128

CAE & Software Development Tools

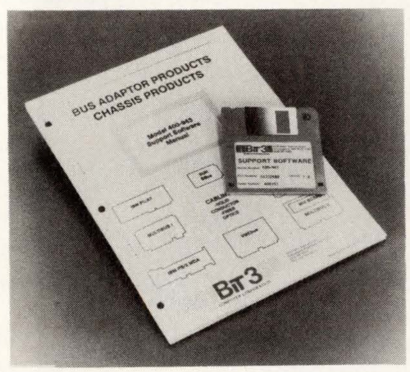
PC-board layout tools. Version 27 of the Scicards system for pc-board layout includes a gridless editor that provides push-shove of board traces and on-line design-rule checking. Another new feature is automatic testing of dense surface-mount and through-hole board designs. In addition to supporting other industry-standard computers, the software is now available for HP 700 series workstations. From $45,000. **Harris Corp,** Scientific Calculations Div, 7796 Victor-Mendon Rd, Box H, Fishers, NY 14453. Phone (716) 924-9303. **Circle No. 428**

Graphics library for C++. Object-graphics for C++ lets users develop hardware-independent graphics using Borland C++ and Application Frameworks or using Turbo C++ for Windows. Users can develop graphical applications via a simple set of graphic objects rather than using scores of primitive function calls. $195. Source code, $390. **The Whitewater Group,** 1800 Ridge Ave, Evanston, IL 60201. Phone (708) 328-3800. FAX (708) 328-9386. **Circle No. 429**

Hardware models for Xilinx FPGA. A model of the Xilinx XC3090 FPGA is available now to run on the LM-family of hardware modeling systems. A software utility lets designers program the FPGA model before a simulation run to reduce overall simulation time. $5000 **Logic Modeling Systems Inc,** 1520 McCandless Dr, Milpitas CA 95035. Phone (408) 957-5200. FAX (408) 945-9181. **Circle No. 430**

AutoCAD symbol library. Revision 4.0 of the Quikdraw symbol library contains 1700 blocked electronic symbols. Users can modify the library by creating new symbols or changing existing symbols. The library has parts for 500 pc-board symbols: physical parts, silk screens, a drill table, drill symbols, targets, and swage drawings. The library has approximately 9 Mbytes of data on 24 3½-in. disks and works with AutoCAD versions 2.5 to 10. $449. **Quantum Technologies Group Ltd,** 1575 Delucchi Lane, Suite 115, Reno, NV 89502. Phone (702) 827-3827. FAX (702) 827-0137. **Circle No. 431**

Design tool for mixed-signal ASICs. PPL Version 5.0 for mixed-signal ASICs provides physical context switching that lets users change rules, libraries, or constraints depending on area definitions. Users can design both analog and digital circuits with this tool. The Standard ASIC package includes tools for design entry, extraction, mixed-mode simulation, and layout and schematic generation. The package also has libraries for Mosis and Foresight shared silicon services. PC version, $14,500. **Bonneville Microelectronics Inc,** 1399 S 700 E, Suite 10, Salt Lake City, UT 84105. Phone/FAX (801) 467-4698. **Circle No. 432**



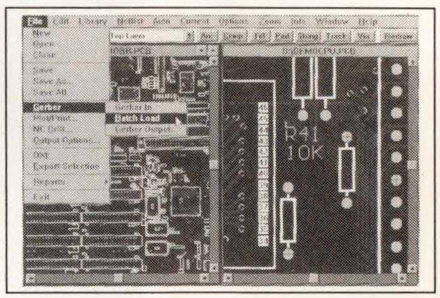
Software for SBus adapters. Model 400-943 Support Software lets users of the company's SBus adapters connect the buses of a SPARCstation and a Multibus system or Q22 bus system or VMEbus system with or without block-mode DMA features. The connection lets the workstation function as a single-board bus-master processor on the non-SPARCstation bus. Software license, $600. **Bit3 Computer Corp,** 8120 Penn Ave S, Minneapolis, MN 55431. Phone (612) 881-6955. FAX (612) 881-9674. **Circle No. 433**

Image-database software. PICS image-database software lets users attach multiple descriptive labels to individual images and retrieve images via Boolean searches. The software runs on a PC/AT or Sun computer and requires a Sony LVR-5000 series Laser Video Disc Recorder. From $6500. **High Sierra Technologies Inc,** Box 8296, 749 Kelly Dr, Incline Village, NV 89450. Phone (702) 832-0792. FAX (702) 832-0778. **Circle No. 434**

Backup for MS Windows. Central Point Backup 7.2 for Windows provides "drag and drop" file selection, backs up to tape drives, and does both background and unattended backup. The software works with all QIC 40/80-compatible and Irwin drives, which are available from many manufacturers. The software also detects 1000 viruses and can search files for viruses without doing a backup. The software runs on PC/AT, PS/2, or compatible computers running Windows 3.0 or 3.1. $129. **Central Point Software Inc,** 15220 NW Greenbrier Pkwy, No. 200, Beaverton, OR 97006. Phone (503) 690-2260. FAX (503) 690-8083. **Circle No. 435**

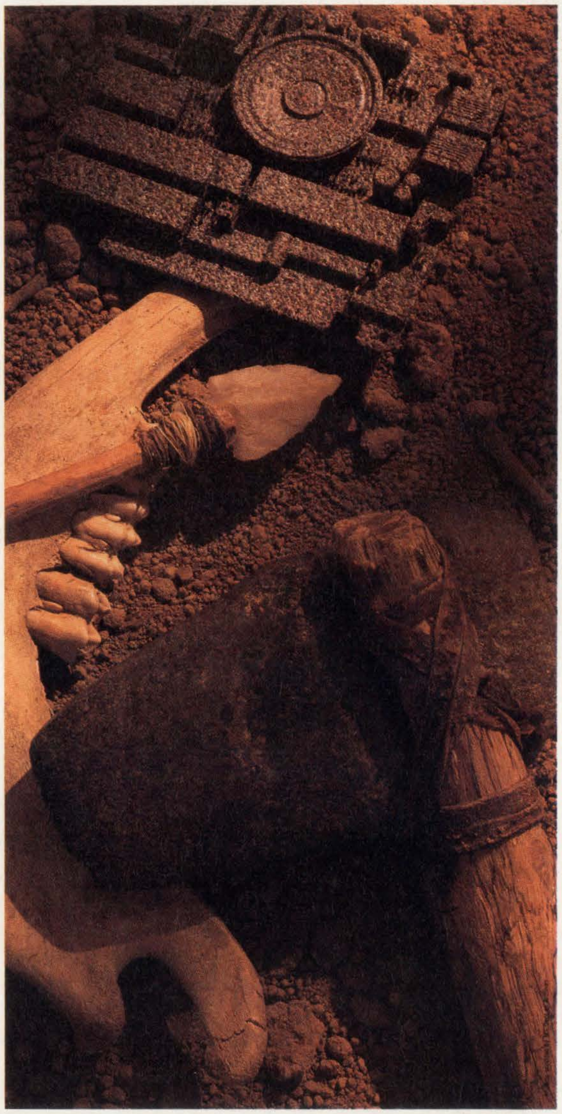
PC X server software. Release 3.0 of the HCL line of PC X server software supports both X11 Version 5 of the X-Window System and MS-Windows 3.1. The software lets a PC emulate an X terminal and connect to networks or mainframes running Unix. From $545. **Hummingbird Communications Ltd,** 2900 John St, Unit 4, Markham, Ontario, Canada. Phone (416) 470-1203. **Circle No. 436**

PC-board layout tools for Windows. The Advanced Pack from the Protel for Windows family of pc-board design tools now includes Advanced PCB, a layout tool; Advanced Place, an intelligent autoplacement tool; and Advanced Route, a 16-layer rip-up and re-



try autorouter. The tools run under MS-Windows 3.0. $2990. **Protel Technology Inc,** 151 Bernal Rd, San Jose, CA 95119. Phone (800) 544-4186. **Circle No. 437**

Virus protection for MS-Windows. Central Point Anti-Virus for Windows detects and removes 1000 viruses. The program also detects stealth viruses, both known and new. Additional features include scheduled scanning, automatic updating, and delete and wipe options for infected files. The software runs on PC/AT, PS/2, or compatible computers running MS-DOS 3.1 or higher and Windows 3.0 or higher. $129. **Central Point Software Inc,** 15220 NW Greenbrier Pkwy, No. 200, Beaverton, OR 97006. Phone (503) 690-2260. FAX (503) 690-8083. **Circle No. 438**



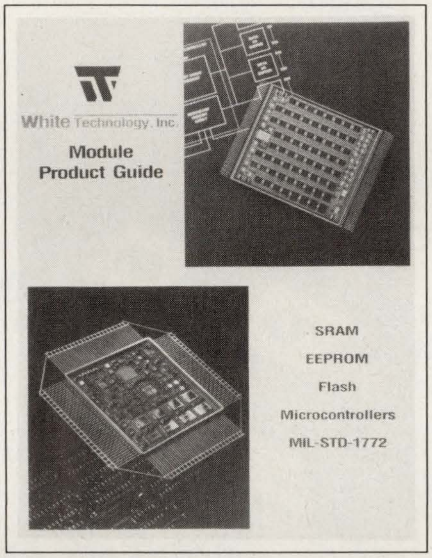
Booklet of SMT interconnect devices. The 28-pg Surface Mount Interconnect Handbook discusses designing insulators, contacts, leads, and terminals. It also provides specifications and

tolerances for materials and construction. **Samtec Inc,** Box 1147, New Albany, IN 47150. Phone (800) 726-8329; (812) 944-6733. FAX (812) 948-5047. TLX 333918. **Circle No. 351**

Three publications on Open Systems. The $1 paper, *Evolution of Open Systems,* discourses on what Open Systems are, their history, and an outlook on their future. The 140-pg Open Systems Reference Guide, *The World of Standards* (members, $3.25; nonmembers, $7), describes 78 standards, including ABI, ASCII, FDDI, IEEE Std 802, IRDS, MIL-D-28000, and X Windows. The listings of the 592-pg Sourcebook (members, $4.25; nonmembers, $8) provide a choice of numerous products that have been tested for shrink-wrap compatibility. **88open Consortium Ltd,** 100 Homeland Ct, Suite 800, San Jose, CA 95112. Phone (408) 436-6600. FAX (408) 436-0725. **INQUIRE DIRECT**

Disk/book set for System 7. *The System 7 Book/Disk Set* is a book on Apple's new operating software combined with two disks offering 7.0.1 utilities and fonts. The software comes on 800-kbyte floppy disks. $34.95. **Ventana Press,** Box 2468, Chapel Hill, NC 27515. Phone (919) 942-0220. FAX (919) 942-1140. **INQUIRE DIRECT**

Choosing a counter/timer. This 4-pg application guide helps you select a counter/timer. It provides an overview and explanation of counter/timer features. In addition, the publication compares the vendor's PM 6680 timer/counter with the HP 5334B and 5335A in categories such as price, frequency range and resolution, sensitivity, single-shot resolution, time average resolution, maximum reading rate, and memory. It also compares several measuring modes of three counters. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. TLX 185102. **Circle No. 352**
Philips Test and Measurement, Bldg TQ III-4, 5600 MD Eindhoven, The Netherlands. Phone local office. **Circle No. 353**

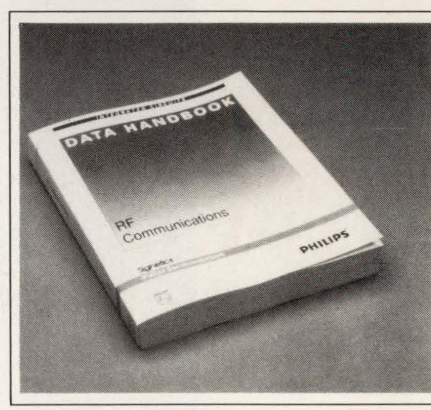


Product guide for computers. The *Modular Product Guide* describes 30 of the vendor's static RAMs, EEPROMs, flash PROMs, and microcontrollers. It lists product specifications, package configurations, and product features and options. **White Technology Inc,** 4246 E Wood St, Phoenix, AZ 85040. Phone (602) 437-1520. FAX (602) 437-9120. **Circle No. 354**

Report on fiber-optic test equipment. *Developments in the fiber-optic test-equipment market* (#1201) is a study and analysis of test equipment for fiber-optic devices. It divides the market into nine segments: telephone subscriber loop; data-communications local area network; aerospace/defense; academic research; test and measurement; industrial process control; computers; medical devices; and others. The report discusses the manufacturers' product lines and reviews competitive advantages of selected companies. It profiles more than 100 leading manufacturers of fiber-optic test equipment, and the appendix provides a directory of test-equipment manufacturers. $1295. **Corporate Strategic Intelligence,** Box 5204, Middlebush, NJ 08873. Phone (908) 545-8795. **INQUIRE DIRECT**

Guide to line of multiple DACs. *The Multiple Digital-to-Analog Converter Integrated Circuit Selection Guide* describes more than of 50 multiple DAC variations. A selection table sorts the DACs by resolution and number of DACs, as well as feature and block-diagram information. **Analog Devices,** Literature Center, 70 Shawmut Rd, Canton, MA 02021. FAX (617) 821-4273. **Circle No. 355**

Offering of self-maintenance services. The *Self Maintenance Services: Your Complete Support* catalog covers support programs to help you get the most from your in-house calibration and repair resources. The publication lets you look at prices and availability of factory-authorized spare-parts services, module exchange services, documentation aids, product-upgrade and service kits, training courses, and government-provisioning and metrology services for the company's instrumentation. Ask for literature no. J0365B. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853. **Circle No. 356**



Handbook of RF communications. This 870-pg handbook presents radio-frequency semiconductor products. It describes product families of amplifiers, compandors, FM IF systems, mixers, audio and data processors, frequency synthesizers, pagers and data receivers, and cellular-communications chip sets. The publication also includes a collection of application notes. **Signetics Co,** 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000. **Circle No. 357**

CIRCLE NO. 130

The quest for the corner office

Becoming a manager may be the most important career move you ever make. Don't rush into it.

JAY FRASER, Associate Editor

For many engineers, a management position is the Holy Grail. They seek it for years believing that when they finally have it in their grasp, their lives will be miraculously transformed. Unfortunately, the changes that accompany a move into management are often very different from what engineers expect.

It's true that becoming a manager can give you more power and prestige. It's also true that it can cause you con-

stant frustration and disappointment. Before you jump at the first management position that opens up, you should weigh its pro's and con's carefully, consider your own talents and goals, and decide whether it's a move you really want to make.

Some of the reasons for becoming a manager are obvious. First of all, you'll probably receive a larger salary, and you may be able to rise higher in the ranks of your company. Managers are also usually on a faster track for promotions and raises than engineers.

Another well-known benefit of becoming a manager is that you'll have more control over resources. You'll decide how money is spent. You'll also get the praise for the results of your decisions.

Dan Ganousis is a project manager at Solbourne Computer (Longmont, CO). He was a working engineer for 12 years for companies such as DEC and NCR before moving to Solbourne in 1989. He knows what it's like to finally have some power over his group's budget.

"It's similar to getting an allowance," he says, "and you decide where you're going to spend it to get the biggest bang. You get to go to management and say 'I want this money because it's going to help my productivity in this way.' Then you see your proposal implemented, and it actually does what you told them it was going to do. That's a great reward."

The added control you gain as a manager also extends to the way your group works. You may not set the final goals for your engineers, but you'll be able to decide to a large extent how they will accomplish them.

Mike Johnson spent eight years as an engineer for IBM and has been an engineering manager for Advanced Micro Devices (Austin, TX) for the past seven. "What I like best," he says, "is being able to leverage the skills that I have across many more people than I would as a hands-on contributor. There's a much better chance for one of my ideas to positively influence many people and have a much broader impact."

Added status and visibility

Managers generally have more status within their companies than engineers, and more visibility to outsiders. When you're a manager, your opinions carry more weight with your superiors, and when you have a voice in purchasing decisions, outside vendors pay more attention to you. Managers are often told of new products and developments in technology directly by managers of vendor companies, rather than having to glean information from sales representatives.

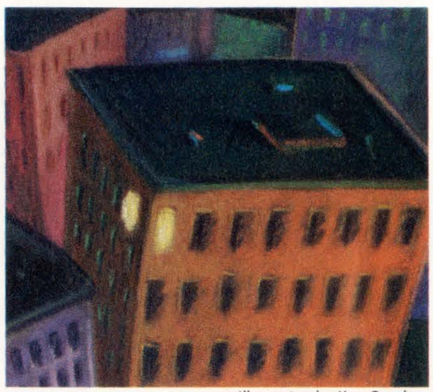


Illustration by Ken Condon

Another benefit is the opportunity to broaden your knowledge. Engineers often end up working in a very narrow niche. If you've become overly specialized, being a manager will enable you to stretch.

Counterbalancing these benefits are a number of aspects of managing that engineers usually find onerous, if not distinctly unpleasant. Primary among them is added responsibility.

"The responsibility weighed on me more than I thought it would," says Johnson. "Until you've had responsibility for people, your impression of how it's going to be is nothing like what it actually is. Suddenly you have people whose lives you can affect in a fairly major way. Your mistakes are potentially multiplied many times."

Another aspect of being a manager you may not be aware of is how much time and energy you'll have to spend dealing with the members of your group. "I was clueless about how draining it is physically and emotionally to manage personalities and conflicts," says Ganousis. "Once I got into this position, I was startled to find out how much was 'this person is saying bad things about me' or 'I'm worried about what my next project is going to be.' It really takes a lot out of you."

Paperwork is an inescapable chore for managers. Engineers have to deal with a certain amount of paperwork, of course, but managers have a much heavier burden. You'll probably have to fill out project schedules, progress reports, requisitions, and budget forms, as well as prepare presentations. You'll also have to write performance appraisals of the people who were once your coworkers, a task that many new managers find particularly difficult.

New demands on your time

Inevitably, all this additional work puts a new manager in a bind. You spend so much time on nontechnical matters that you have little left over for keeping up with new developments in technology. Lower-level managers may not have their hands on the work any more, but they're still expected to be up-to-date technically and understand all the aspects of the projects their engineers are working on.

Being caught in the middle is a typical predicament for new managers. You may, in some ways, have less autonomy than you did as an engineer. For example, strategic decisions about product develop-

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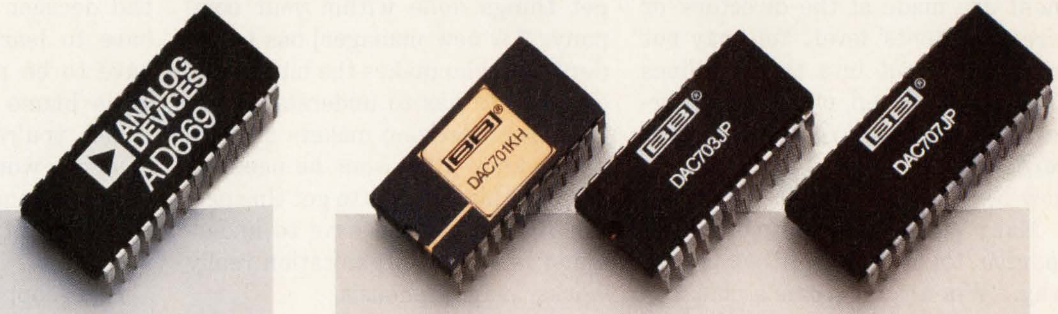

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CIRCLE NO. 132

ment are made at the directors' or vice presidents' level. You may not have any input into the deadlines that are imposed on you. Lower-level managers are largely concerned with specific projects and how to get them done on time.

Many new managers find it hard to give their engineers some leeway. "When you become a manager you have to trust the people who work for you to do the job," says Johnson. "You have to give them the flexibility to do it in a way that might not be the way you would have done it yourself. That can be difficult for some managers. They see people doing something the 'wrong' way, and they have a strong tendency to jump in and do the job themselves. Some managers develop a bad habit of doing other people's work for them."

One of the most important adjustments you'll have to make as a manager is changing your perspective. Engineers tend to focus on individual tasks, problems with clear-cut solutions, and details. Managers, on the other hand, have to see the larger picture. You'll have to understand not only all the technological aspects of the project at hand, but also how it fits into the company's business plans. No matter what level you're on as a manager, you'll be expected to know how your firm markets, sells, and services its products.

You'll also have to learn how to get things done within your company. "[A new manager] has to understand who makes the budget decisions. He has to understand who the power decision makers are. He has to know that when he needs to do something he has to get this person signed up. You have to understand how your organization really works," says Ganousis.

After you've weighed the pro's and con's of a move into management, you should also get some first-hand information. Talk to managers who were once engineers. Find out what they like and dislike about their jobs. Ask them what difficulties they faced making the transition and how they handled them. If they could make the decision again today, would they still choose to become managers.

You can get a good idea of what managers do on a day-to-day basis by observing your own manager. When he was working as an engineer, Dan Ganousis watched how his manager handled problems as they arose. "I asked myself what I would do if I were the manager. Would I do this? Would I do that? It turned out that I was generally making the right decisions. It helped me develop confidence in my ability to make decisions."

Making decisions is an inescapable part of a manager's job. Some people don't like to make decisions because they're afraid they'll make mistakes. But making an occasional bad decision is inevitable, and you have to learn to accept that. You have to be prepared to take some of the blame when things go wrong. When you're a manager you can delegate work, but you can't delegate responsibility. The ultimate responsibility will always remain with you.

If the opportunity arises, volunteer to be the leader of a project or to take on some other kind of short-term responsibility. In that way, you'll gain some actual managerial experience. You'll find out for yourself what it's like to make assignments, allocate resources, and deal with personality problems. There's no substitute for personal experience.

Making the great leap

If you do decide you want to move into management, don't grab the first postion that's offered. Make sure it's right for you. If your company has written job descriptions, read the one for the open position carefully. If any details aren't clear, ask questions. Find out how much authority you will have as a manager. Don't end up with an empty title.

Also find out about the group you may be managing. Suddenly having authority over people you've been working alongside for years can present some problems, but being made manager of a group you're unfamiliar with can create even more.

Should you become a manager?

Before you decide on a major career change, use the following questions to evaluate your potential for management.

- Will engineering or management utilize my personal strengths better?
- Do I have the ability or the desire to develop management skills?
- Will I be comfortable taking on more responsibility?
- Can I adjust to additional demands on my time?
- Am I willing to broaden my technical knowledge?
- Do I enjoy working with people?
- Am I willing to give others the latitude to work in their own way?
- Do I want to take on increased administrative duties?
- How much job security do managers in my company have?
- Which is more important to me, financial rewards or job satisfaction?

"It can really be difficult for somebody to start off with a group that has a history behind it, that has an existing grapevine and interpersonal relationships and so forth," says Johnson.

After you've evaluated the management position that's available, find out how much support your company is willing to give you. Does it have in-house training courses for new managers? Is it willing to send you to courses outside? What is the company going to expect from you? And how much independence will it give you to do your job?

You should also do some research on the economic condition and direction of your company—find out if your firm is growing or not. Ask about your company's plans for the future and see if your group fits into those plans. Find out how much job security managers have in your company. Take a look at the current job market. You may be better off remaining where you are and increasing your engineering knowledge and skills.

Finally, before you accept a management position, you should do what many people find extremely difficult—take a good look at yourself. Evaluate your potential to be a manager as objectively as possible. Try to determine your strengths and weaknesses and see how much they will help or hinder you. For example, as a manager you will have to deal with people every day, and most engineers have no training in how to do that. Ask yourself if you have the potential and the desire to develop your skills in managing people.

Many reasons for becoming a manager are important—money, power, prestige—but they're not as important as personal satisfaction. The final question you have to ask yourself is whether you will find more satisfaction as a manager or as an engineer. Only you can decide what you really want. EDN

Jay Fraser, Associate Editor, can be reached at (617) 558-4561, FAX (617) 558-4470.

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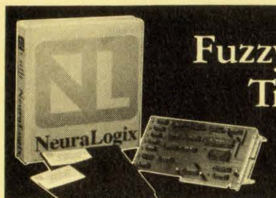

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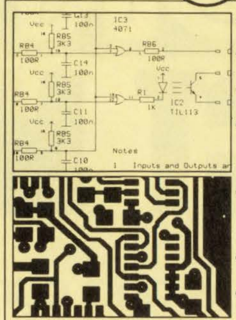

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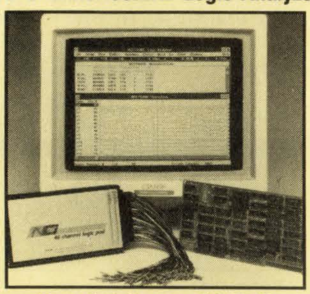

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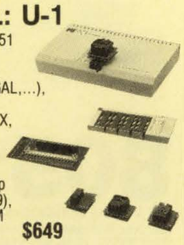

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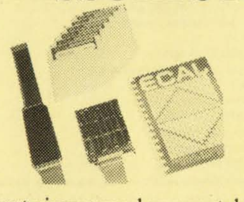

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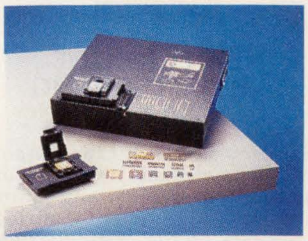

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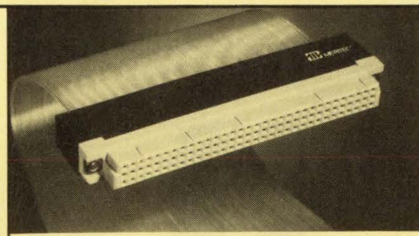

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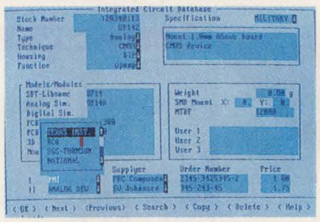

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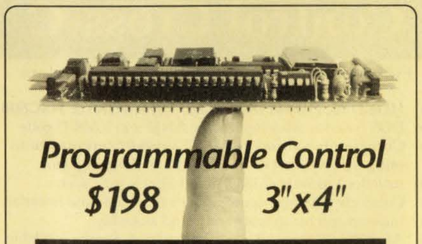

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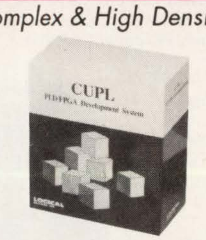

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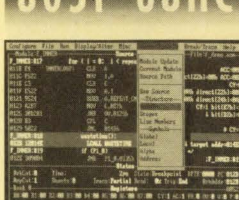

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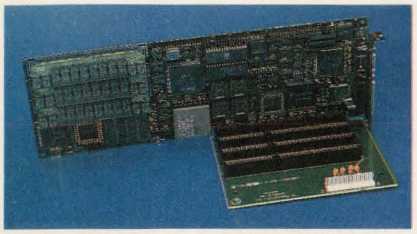

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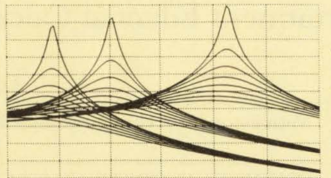

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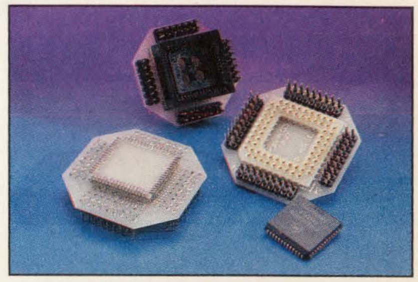

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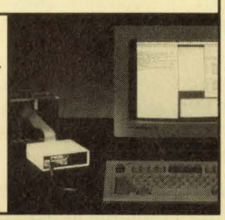

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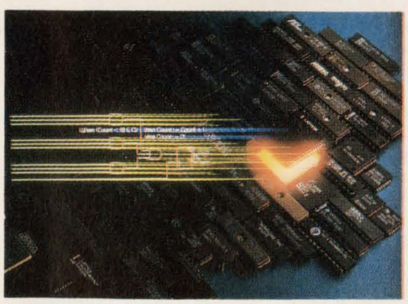

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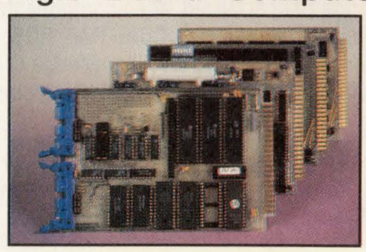

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EDN-ACRONYMS & ABBREVIATIONS

AGC—automatic gain control
ANSI—American National Standards Institute
BW—bandwidth
DOS—disk operating system
dpi—dots per inch
EDIF—electronic design-interchange format
FET—field-effect transistor
FPGA—field-programmable gate array
IC—integrated circuit
IEEE—Institute of Electrical and Electronics Engineers
I-to-V (converter)—a circuit that uses an op amp's near-infinite open-loop gain to accurately convert the current that flows into the summing junction's virtual ground into a proportional voltage
JFET—junction field-effect transistor
LED—light-emitting diode
MS-DOS—Microsoft Disk Operating System
NMOS—n-type metal-oxide semiconductor
NTSC—National Television System Committee
PAL—phase alternation line, European broadcast television standard
PC—personal computer
pc—printed circuit
PLD—programmable logic device
PMOS—p-type metal-oxide semiconductor
ppm—parts per million
PSRR—power-supply rejection ratio
RAM—random-access memory
RTD—resistive temperature detector
SECAM—sequentiel couleur à memorie, French broadcast television standard
Spice—Simulation Program with Integrated Circuit Emphasis, a public-domain general-purpose program from UC Berkeley that simulates ICs and system-level circuits
SRAM—static random-access memory
V/F—voltage/frequency

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