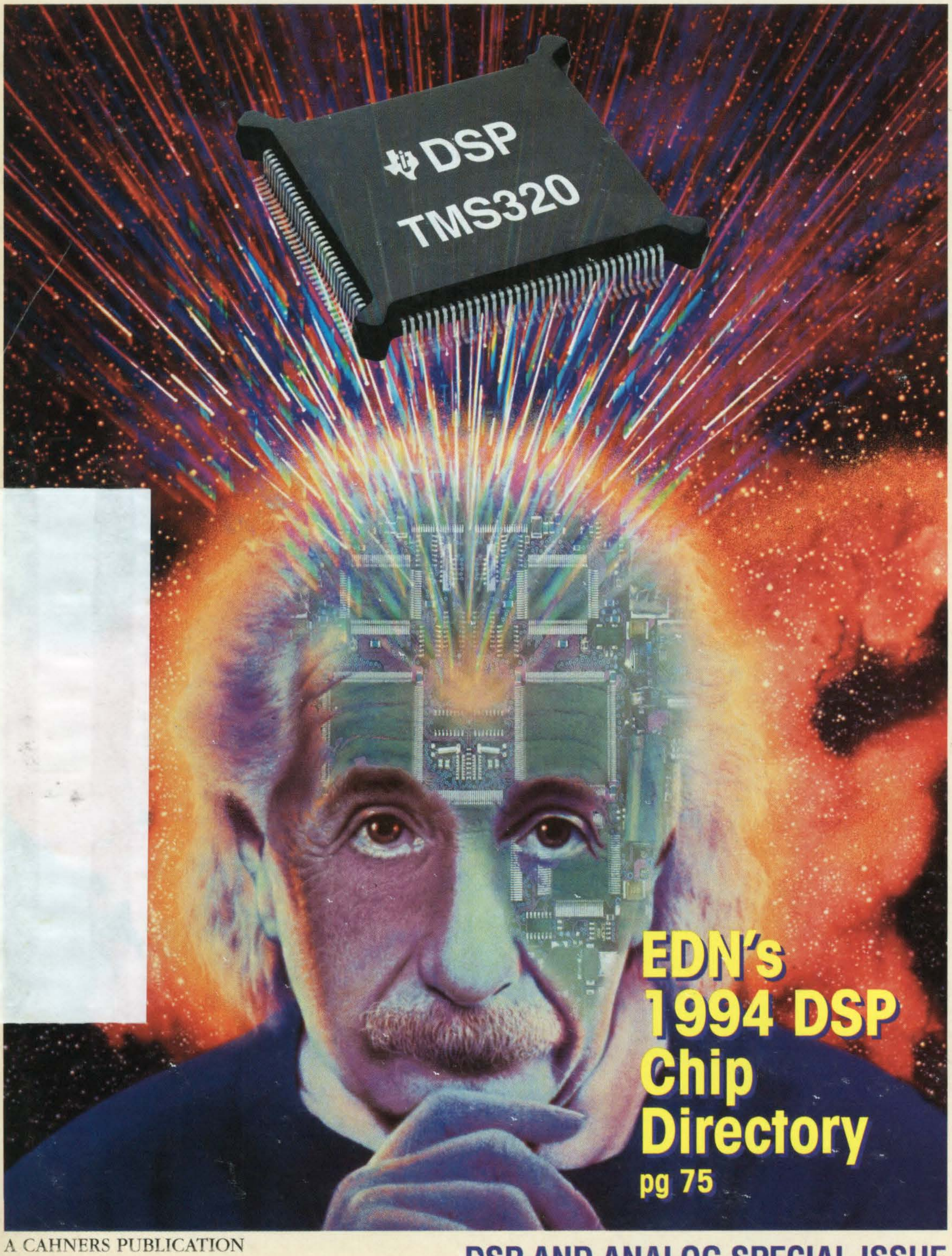
June 9, 1994

EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY



EDN's 1994 DSP Chip Directory
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NEW PRODUCT INTRO

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Ignore packaging effects at your peril
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Technique eases design of high-order PLLs
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Good design enables hot insertion of power supplies
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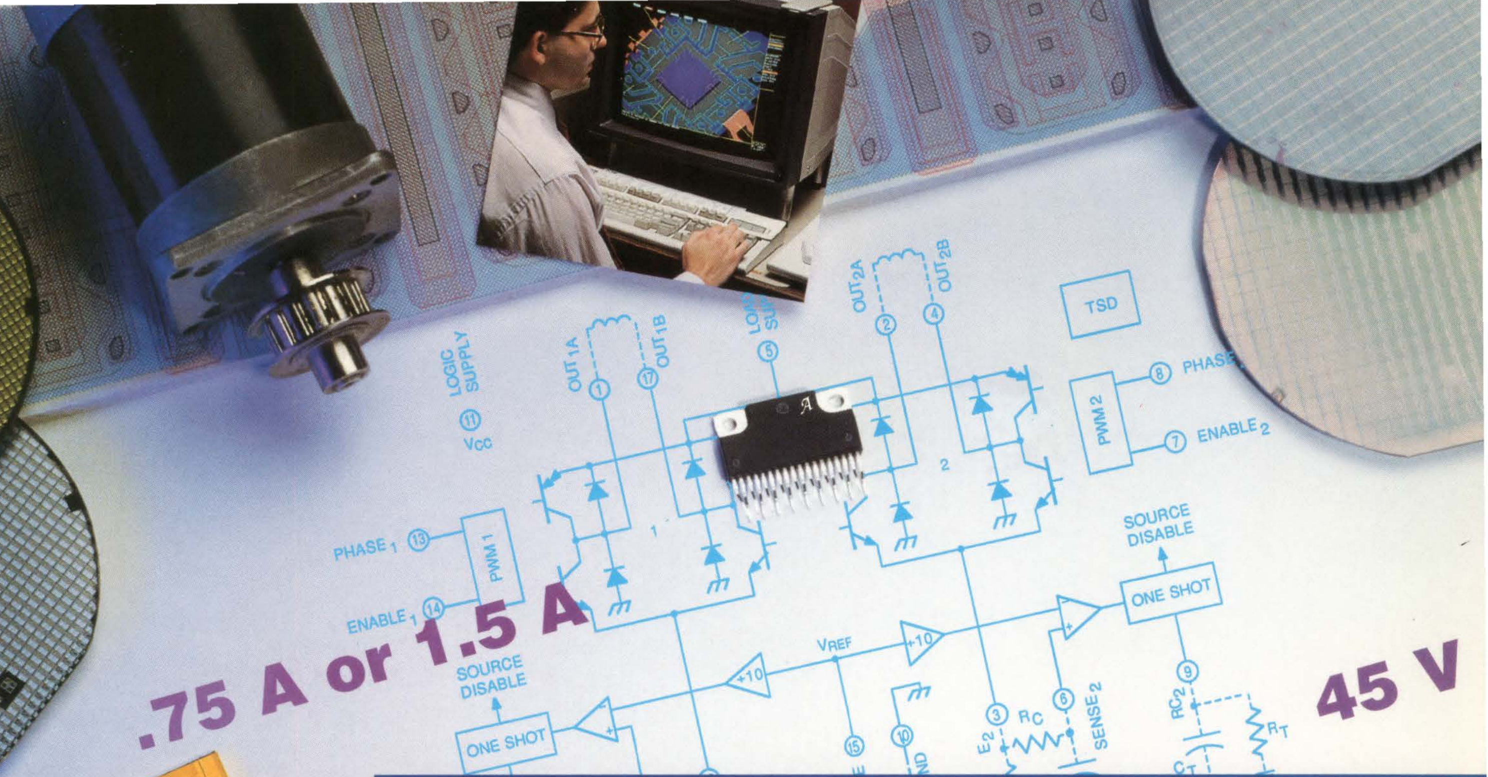
A CAHNERS PUBLICATION

DSP AND ANALOG SPECIAL ISSUE



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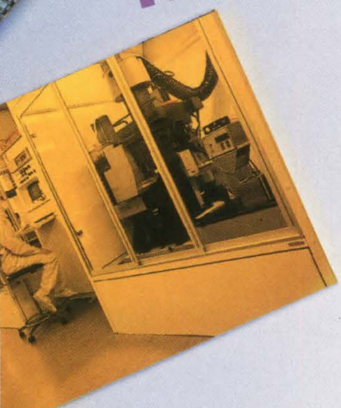

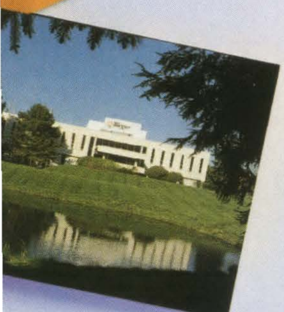

FEATURES

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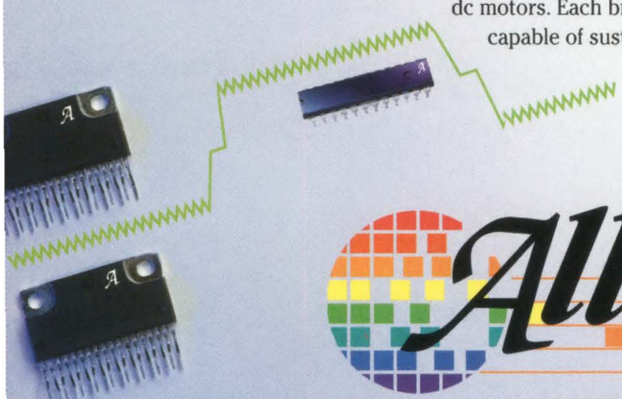

THE PACE QUICKENS

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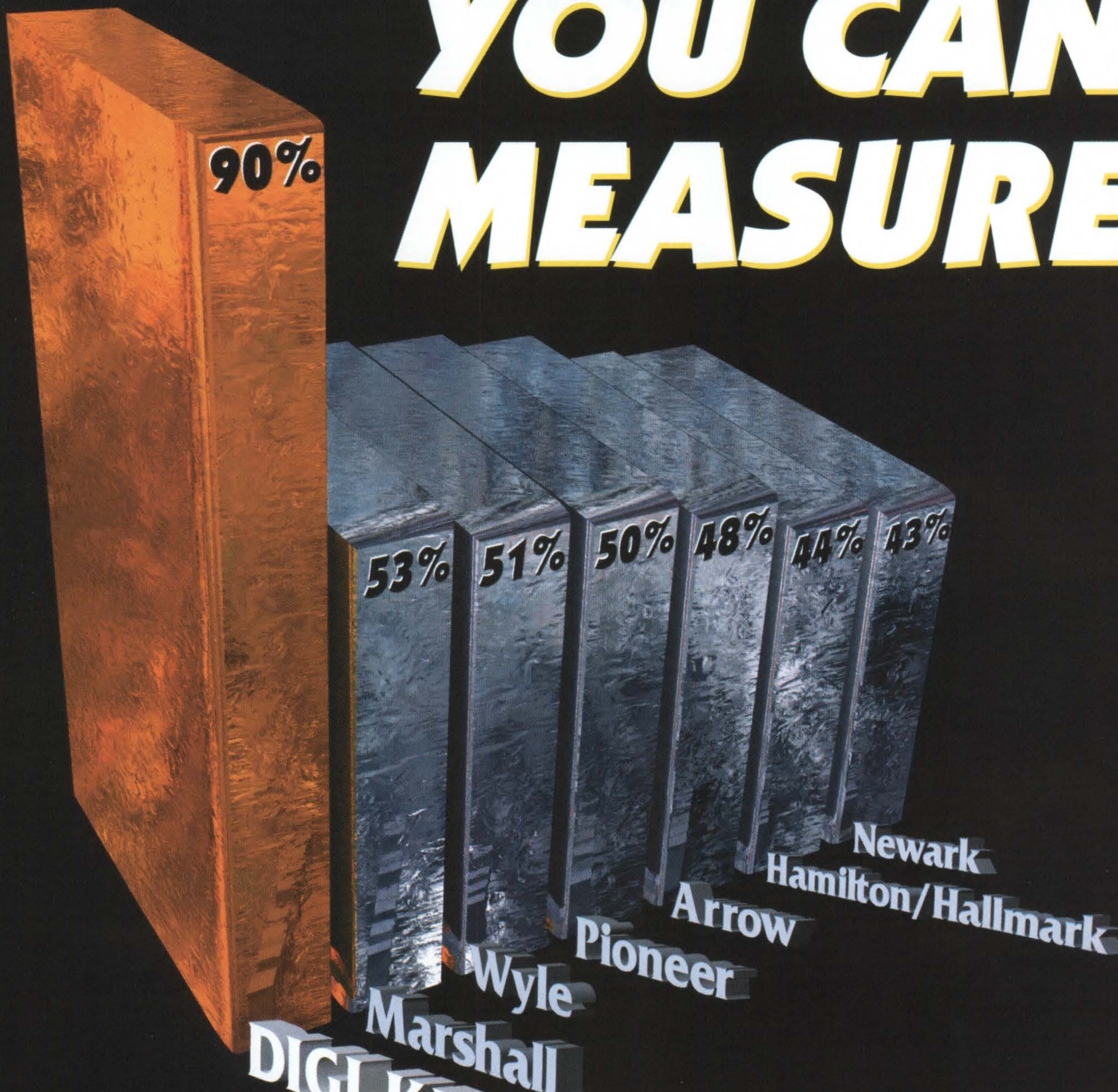

In a recent "Engineering & Distribution Survey" conducted by *Electronic Engineering Times*, engineering managers were asked to evaluate distributors they have done business with/are most familiar with on a wide range of criteria related to customer service and technical support. The bars above reflect the percentage of each distributor's customers that rated their distributor as excellent (6 & 5 responses) on a 6 point scale where 6=excellent and 1=poor in terms of OVERALL PERFORMANCE.

Note: Since the bases varied for each distributor, direct comparisons should not be made.

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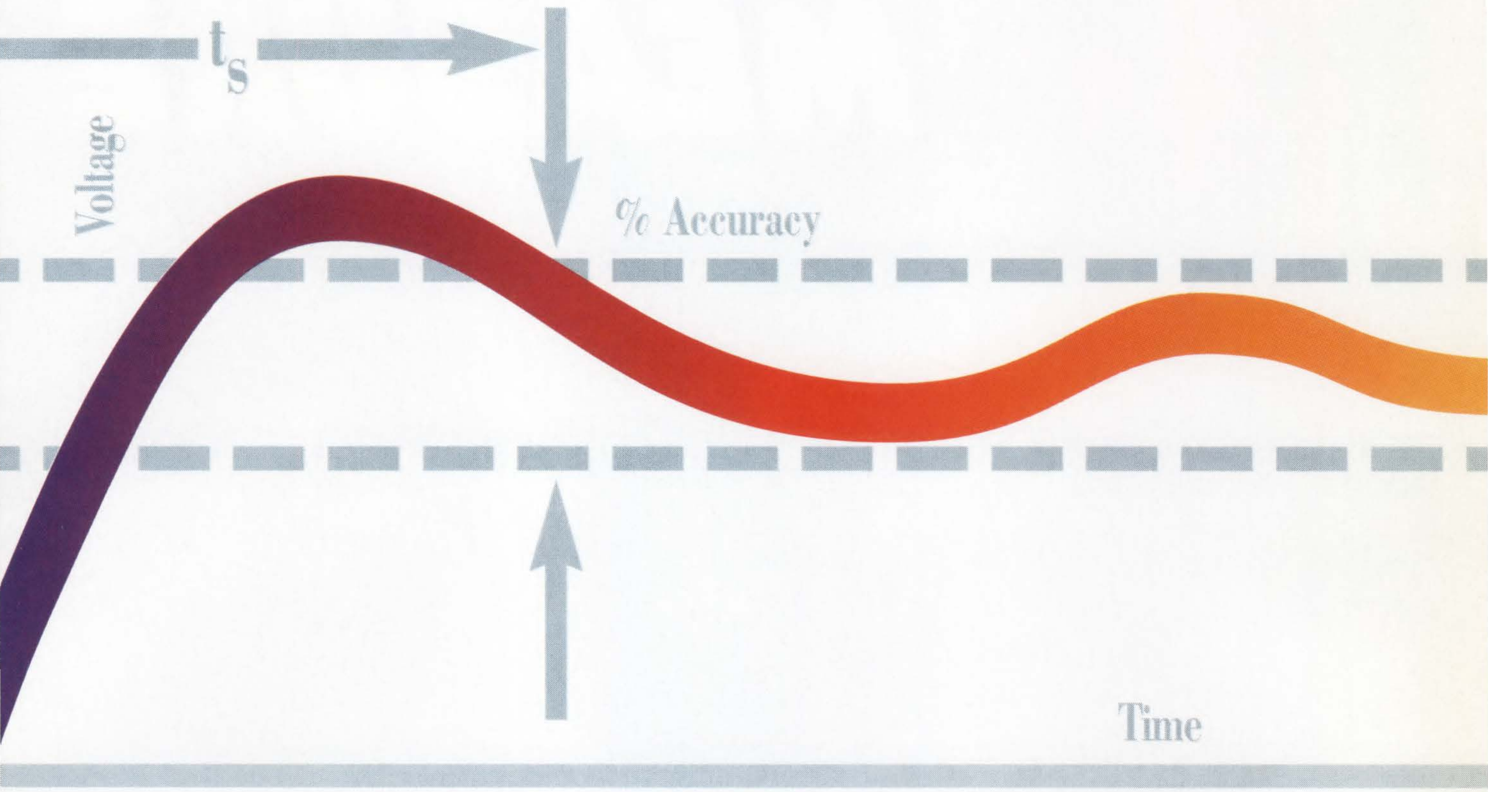

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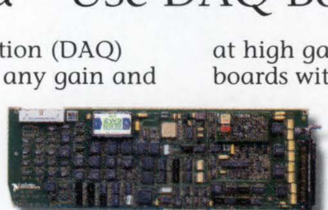

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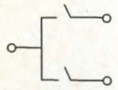

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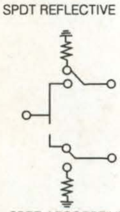

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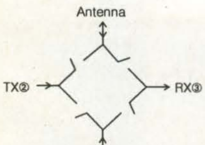

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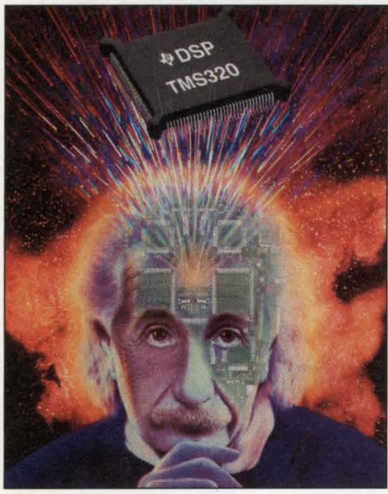

On the cover: If you're thinking about designing with DSPs, look no further. Our annual DSP directory, which begins on pg 75, gives you a head start on the evaluation process. (Cover photo courtesy Texas Instruments; design, Dennis Full; Albert Einstein photo courtesy The Roger Richman Agency Inc, Beverly Hill, CA, which is the licensing agency for The Hebrew University of Jerusalem, the beneficiary of the estate of Albert Einstein.)

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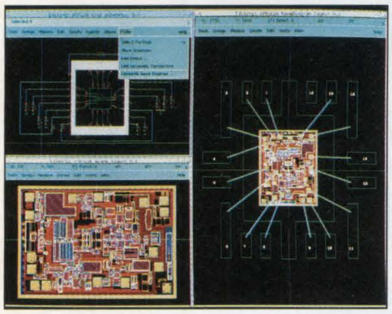

Design for packaging is not yet a standard part of CAD tools. Fortunately, vendors are developing the needed tools (pg 47).

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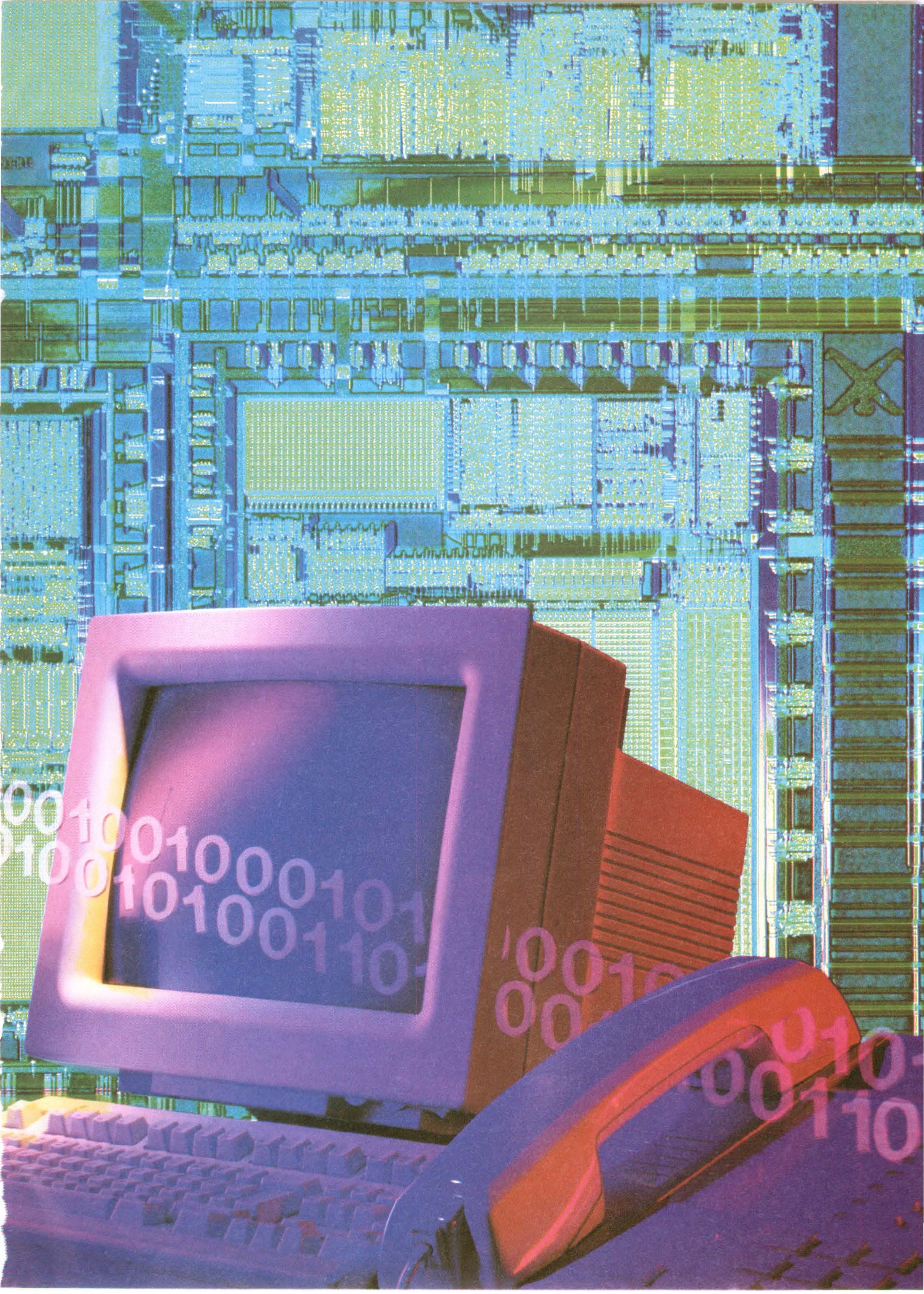
EDITORIAL

COLUMNIST

NEW PRODUCTS

DEPARTMENTS



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CIRCLE NO. 32

The DSP and Analog Special Issue

You've got a two ways to access the wealth of DSP and analog-related material that we've amassed for this special issue. Way #1: Read and keep this handy issue. Way #2: Log on to the free EDN bulletin-board system (BBS).

Start with our cover story—EDN's 1994 DSP Chip Directory (pg 75). You'll find all you need to know about 22 digital signal processors and their families: detailed architectural and performance data and pricing information on everything from 16-bit fixed-point chips to 32-bit floating-point devices. In addition, Technical Editors Charles Small and Anne Swager gathered DSP- and analog-specific Design Ideas for this issue. See that special section beginning on pg 139.

Our coverage of the DSP^X show will benefit new and experienced DSP users alike. Read about the design-oriented sessions and introductions of innovative products beginning on pg 58.

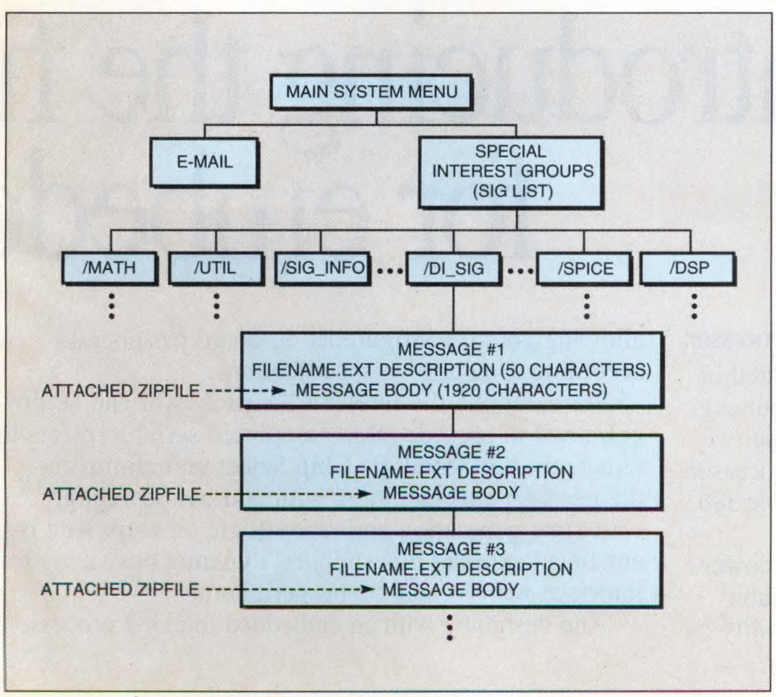
If you haven't had a chance to check out our free BBS, now would be the perfect time. It contains quite a bit of freeware and shareware for DSP and Spice, in addition to related material, on three subsections of the BBS under the Main System Menu.

The first place to look is the BBS's repository for Design Ideas, the /DI_SIG Special Interest Group. All of the postings on the /DI_SIG are freeware, available for only the price of a phone call. Among the 220 Design Ideas posted on this SIG you will find 20 related to DSP and 37 related to Spice.

Next visit the /DSP Special Interest Group. Of the 140 postings on the /DSP SIG, most are freeware. The posted files contain specialized math routines for many different DSP μPs as well as software for implementing functions such as a software modem. The /DSP SIG also contains development tools for DSP μPs such as monitors, simulators, assemblers, and linkers.

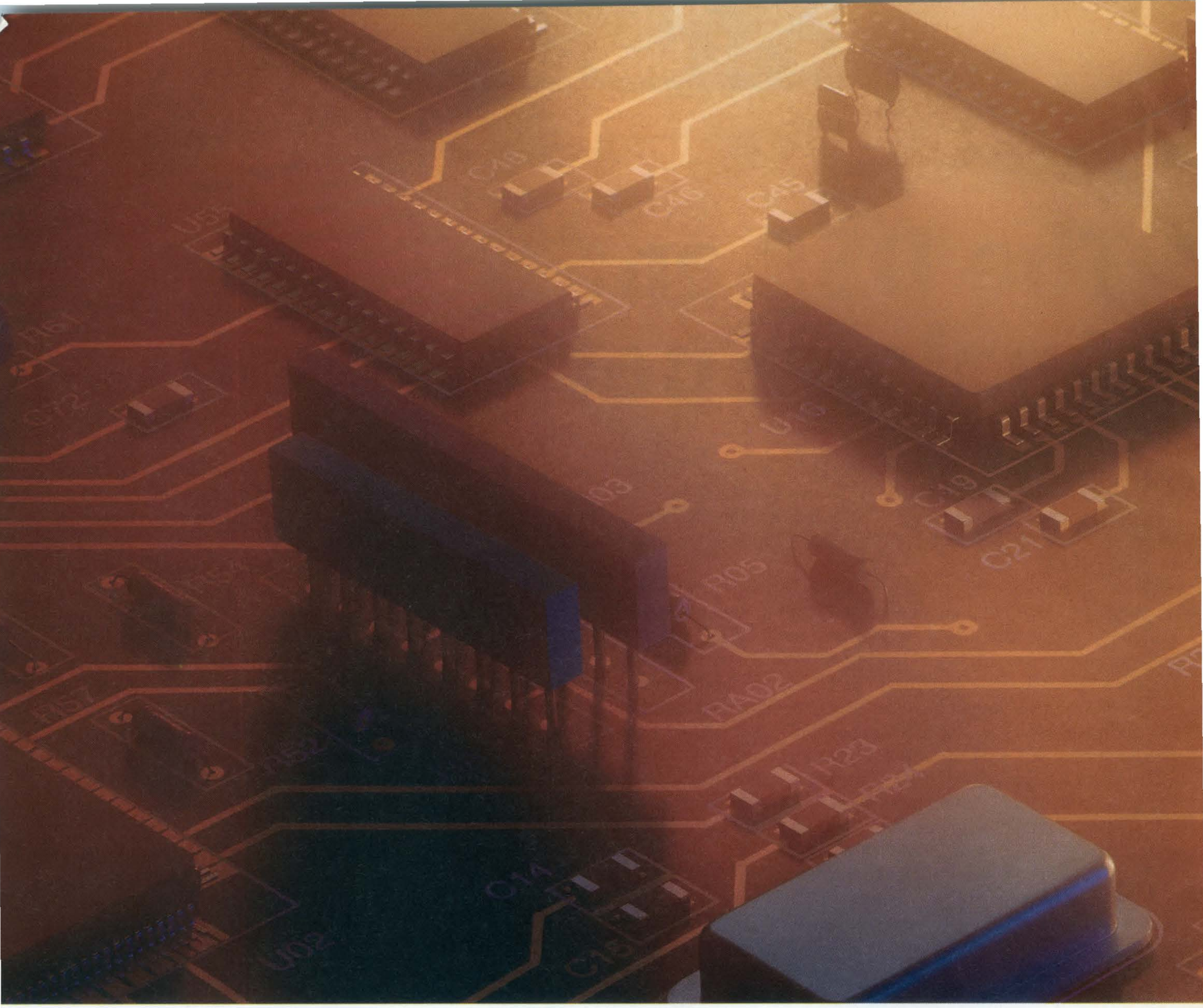
Analog engineers will be able to find Spice models for components ranging from the mundane (metal-oxide varistors) to the exotic (solar arrays). The /SPICE SIG also contains 16- and 32-bit versions of Spice compiled for operating systems such as OS/2, Windows 3.X, and Windows NT, among others. These versions of Spice are generally shareware programs. You may try out shareware programs for free, paying a modest "registration" fee only if you like the program.

To delve into the EDN Readers' BBS, first study its hierarchy. One layer down from Main System Menu are the Special Interest Groups. Attached to each SIG is a single chain of messages. Optionally, each message can have a single file attached to it. Generally these files are compressed ZIPfiles that may contain, in compressed, concatenated form, entire suites of files and their directories.



To log on and register, call (617) 558-4241, 1200/2400 8,N,1 (9600 baud, (617) 558-4580). To check out the Design Ideas SIG, for example, from the Main System Menu, enter *ss/DI_SIG*. Best bet: When you get to a SIG's main menu, turn on your communications program's screen-capture or log-file feature and then enter *rlb*. This command will give you a directory of everything posted on the SIG.

Or do a keyword search. To perform a keyword search for DSP-related Design Ideas on the /DI_SIG, for example, enter *rkdsp*. Again, having your screen-capture feature enabled during a search is a good idea. Once you find and read a message describing a file you want, the BBS will offer you the chance to download the attached file using one of a variety of common protocols. If you do not have PKware's outstanding example of shareware, PKUNZIP, with which to uncompress your downloaded file, you can pick up a copy from the BBS's /util SIG. Versions are available for PCs, MACs, and Unix computers. Happy hunting.



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And designing with an embedded Intel386 processor

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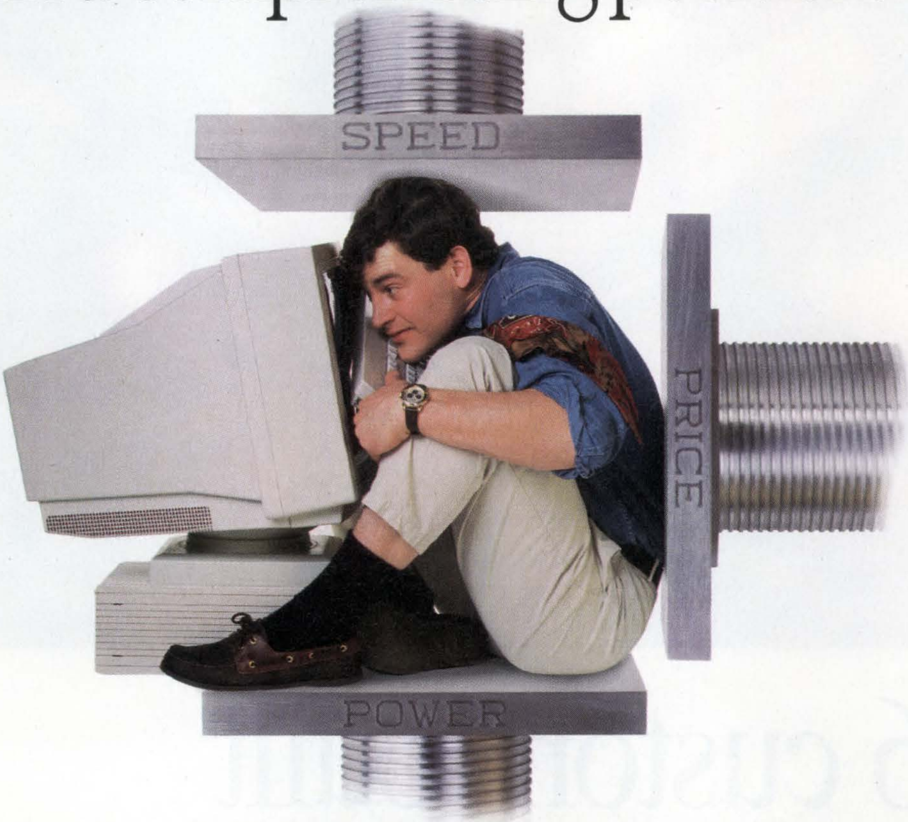

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Specification	AD8001	CLC406	HFA1105	OPA623
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Peaking, G=+2, (dB/MHz)	.1/100	.2/25	.12/75	.2/100
Slew Rate (V/μsec)	1200	1500	1100	2100
Diff Gain/Phase (%/°)	.01/.025	.02/.025	.02/.02	.12/.05
Supply Current (mA, Max)	5.5	6.7	6	4.5

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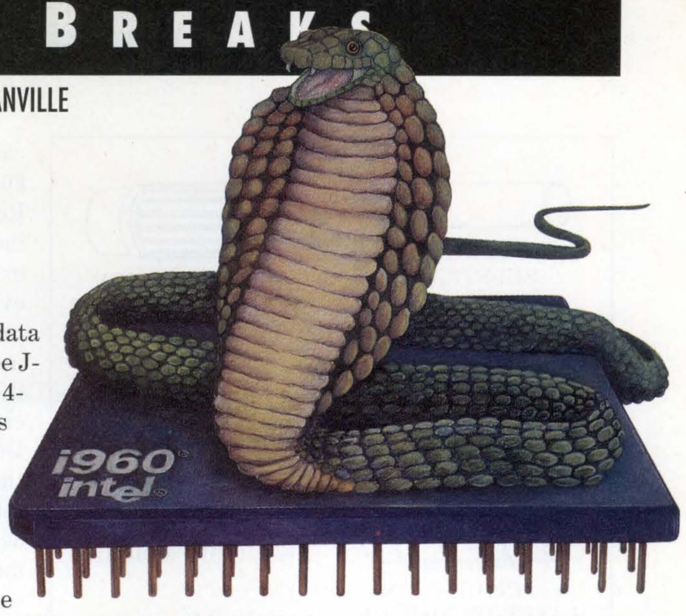


Cache and clock doubling boost i960 μP performance 2x

Intel has borrowed two speedup techniques from its immensely successful 386/486 μP family—clock doubling and on-chip cache—to more than double the performance of the company's third-generation i960 RISC μPs. Code-named the "Cobra" series and officially designated the "J" series, the new i960 μP family members retain pin-for-pin and code compatibility with earlier members of the family and provide substantially faster execution than the earlier units.

The Cobra series comprises the 80L960JA, 80L960JF, 80960JF, and 80960JD. Each μP is available in two or more speeds. The first two μPs, with the "L" designation in the part number, are 33-MHz, 3.3V processors. The 3.3V processors use 60% less power than the i960's "K" series processors. All processors in the "J" series have a low-power power-down mode and employ active power management, which switches off unused processor blocks on an instruction-by-instruction basis.

The 80L960JA has a 2-kbyte instruction cache and a 1-kbyte data cache, and the other three J-series processors have 4-kbyte instruction caches and 2-kbyte data caches. The midrange family member, the 80960JF, runs on 5V at 40 MHz, and the fastest of the Cobra series, the 80960JD, employs clock doubling to run at 50 MHz, while its external bus runs at 25 MHz. In addition, the Cobra i960 series employs a modular core that lends itself to custom versions. Intel will consider making custom parts based on the i960 core for key large-volume customers.

At the same time, Intel is introducing a 2-pass profiling compiler said to increase processor performance by an average of 25 to 30%. In the first pass, the profiling compiler puts timers and probes into code to identify the code segments that are consuming the most execution time. During the second pass, the compiler uses the first-pass timing information to optimize key code segments through optimization techniques such as code unrolling. Some early users of this approach have realized speed improvements of as much as 300%.

Samples of the 80960JF and 80L960JA will be available in September. Samples of the 80960JD will be available in December. Production volumes of all J-series μPs will be available in 1995. Prices are as follows: 80L960JA16: $16.60, 80960JF16: $24.90, 80L960JF16: $27.40, 80960JD32: $29.45.—by Steven H Leibson

Intel Corp, Chandler, AZ, (800) 628-8686. **Circle No. 471**

Experimental micromotor measures 1.4×15 mm

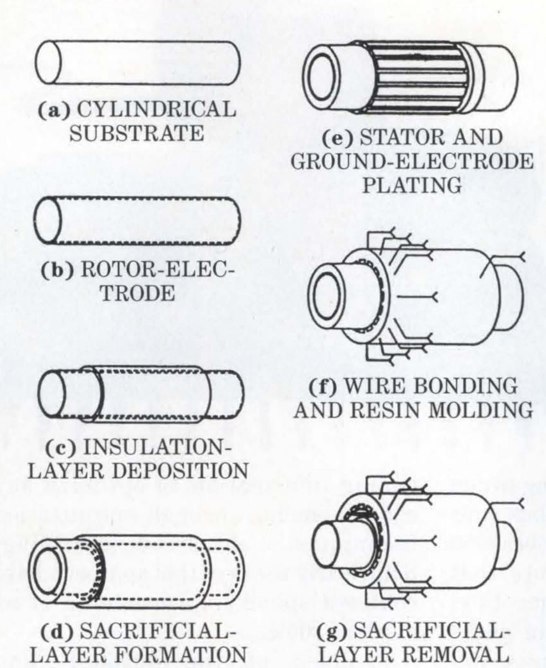
Matsushita Research Institute Tokyo Inc has successfully fabricated an experimental, electrostatic wobble motor using a concentric "buildup," or additive, process that more closely resembles pc-board or IC manufacturing than conventional motor assembly. Researchers elsewhere have developed wobble motors using silicon micromachining or conventional machining. Matsushita's experimental fabrication process creates a wobble motor whose size falls somewhere between motors built from these other processes. The completed micromotor is 15 mm long and 1.4 mm in diameter. It operates from 350V pulses and rotates as fast as 140 rpm with an applied excitation of 14k pulses/sec.

The fabrication process for the prototype motor starts with a machined ceramic rotor shaft (**a**). The hollow shaft has an outer diameter of 1 mm, an inner diameter of 0.12 mm, and is 15 mm long. RF magnetron sputtering adds a rotor electrode to the shaft (**b**). During sputtering, machinery in the sputtering chamber rotates the motor shaft to achieve a uniform electrode layer around the rotor shaft's circumference. In a similar manner, RF magnetron sputtering then adds a 0.004-mm $SiTiO_3$ insulating layer to electrically separate the motor's stator and rotor electrodes during the motor's operation (**c**).

Adding a polyimide sacrificial layer, the next step, (**d**), is the key to eliminating mechanical assembly steps. The dip-coated sacrificial layer provides a mechanical spacer that separates the motor's rotor and stator during manufacturing. Later, one of the final assembly steps dissolves the sacrificial layer leaving a 2-piece motor assembly. Researchers at Matsushita admit that achieving uniformity with the dip-coating process is tough and state that this manufacturing step requires more development.

A second dip-coating step then adds a layer of photoresist polymer to the rotor assembly. Special rotating imaging equipment patterns the ground and stator electrodes onto the photoresist, and conventional etching leaves patterns behind for the electrodes. Electroless plating forms the 1-μm-thick stator electrodes in depressions left in the photoresist layer after etching (**e**). The prototype motor has 16 stator poles.

After plating, the remaining photoresist is dissolved, and conventional wire bonding adds drive wires to each stator electrode (**f**). Then a resin coating fills in between the electrodes and a second coating, using a different resin, encompasses the overall stator. Finally, an ultrasonically assisted etching step completes the motor fabrication by dissolving the sacrificial layer and leaving behind an 11-μm gap be-



Steps in the wobble motor's fabrication

tween the motor's rotor and stator (g).

Although calculations predicted that the motor would rotate at 160 rpm with an excitation of 2k pulses/sec, the fabricated motor achieves only 30 rpm at that pulse rate. Rotation rate does seem to increase linearly with the excitation pulse rate, however. Researchers conjecture that residual stresses in the stator resin deformed the stator after the sacrificial layer was removed. Deformation would degrade the accuracy of the rotor-stator gap and could account for the drop in mechanical efficiency.

(Research on this wobble motor was performed under the management of Japan's Micromachine Center as part of the Research and Development of Micromachine Technology project supported by NEDO, the New Energy and Industrial Technology Development Organization.)

—by Steven H Leibson

Matsushita Electric Industrial Co, Tokyo, Japan, 81-3-3459-9736.

Circle No. 472

ATM ICs proliferate at telecomm trade shows

Components and products for asynchronous-transfer-mode (ATM) data links were a major component of two recent communications trade shows, SuperComm '94 (New Orleans) and Networld/Interop '94 (Las Vegas). The product announcements at these shows included a number of second-generation ATM ICs that reflect recent additions to the ATM specifications. Devices from AT&T Microelectronics, Fujitsu, LSI Logic, and PMC-Sierra head the list of new devices.

AT&T Microelectronics introduced its T7652 ATM Layer Interface (ALI) chip at Networld/Interop. The $35 (10,000) device handles ATM-layer functions, such as policing and virtual-channel translation for broadband switching equipment. Working with AT&T's T7650 self-routing switch, the ALI chip allows creation of ATM switches and hubs capable of handling 1000 virtual channels at sustained rates of 320 Mbps.

Fujitsu introduced its second-generation ATM chip set for network-interface cards. The set comprises the MB86680 switch-routing element ($86), the MB86686 adaptation-layer controller ($105), the MB86683 network-termination controller ($60), and the MB86689 address-translation controller ($47). The devices are pin-compatible with their first-generation counterparts but include enhancements reflecting additions to the ATM specifications. The enhancements include circuits to manage flow control, network congestion, and traffic-statistics gathering.

LSI Logic introduced the ATMizer-LX and -BX, both standard products based on the company's programmable ATM ASIC cores. The devices employ a RISC processor to handle segmentation-and-reassembly (SAR) and ATM-layer operations at data rates to 155 Mbps. The LX series ($79 to $129) devices serve the needs of network-interface cards for a variety of computer buses. The BX series ($175) devices are intended for backbone hub and router applications.

PMC-Sierra announced its STEL/AR chip set for broadband-transmission interfaces and switching subsystems. The devices work with PMC's earlier SUNI ATM physical-layer products and are aimed at Synchronous Optical Network (SONET) and STS-3/12 broadband line cards. Prices range from $121 to $336 (5000).

In addition to chip introductions, several manufacturers announced collaborative agreements to develop ICs for bringing ATM to desktop computers. Fujitsu is working with Olicom A/S (Denmark) and Cray Communications (UK) to develop ICs for ATM LANs and LAN-to-WAN (wide-area-network) links. LSI Logic will work with Integrated Telecom Technology (IgT) (Gaithersburg, MD) to combine the ATMizer with IgT's SONET framer in a single IC.—by Richard A Quinnell

AT&T Microelectronics, Allentown, PA, (800) 372-2447, Dept P21.
Circle No. 473

Fujitsu Microelectronics, San Jose, CA, (800) 642-7616. **Circle No. 474**

LSI Logic, Milpitas, CA, (800) 451-2742. **Circle No. 475**

PMC-Sierra, Burnaby, BC, Canada, (604) 668-7300. **Circle No. 476**

Build 0.8-μm gate arrays in a day

With its QYH500 family of laser-programmable gate arrays, Chip Express can provide packaged ASIC prototypes parts in one day. These laser-programmable devices combine the performance and density of traditional gate arrays with the fast turnaround of field-programmable gate arrays. The family offers 20,000 to 45,000 total gates, up to 300 programmable I/Os, 460-MHz toggle rates, and less-than-300-psec NAND gate delays. The fast turnaround results from the company's patented laser-based disconnect system and its QuICk place-and-route software. The software take inputs from industry-standard design tools and generates a cut list for a laser-based micromachine. With up to 10,000 bursts/sec, a 45,000-gate device that requires up to 15 million cuts takes approximately 2 hours to customize. The company ships packaged and tested units from the factory as quickly as one day after receipt of a customer's netlist.—by Anne Watson Swager

Chip Express, Santa Clara, CA, (408) 988-2445. **Circle No. 477**

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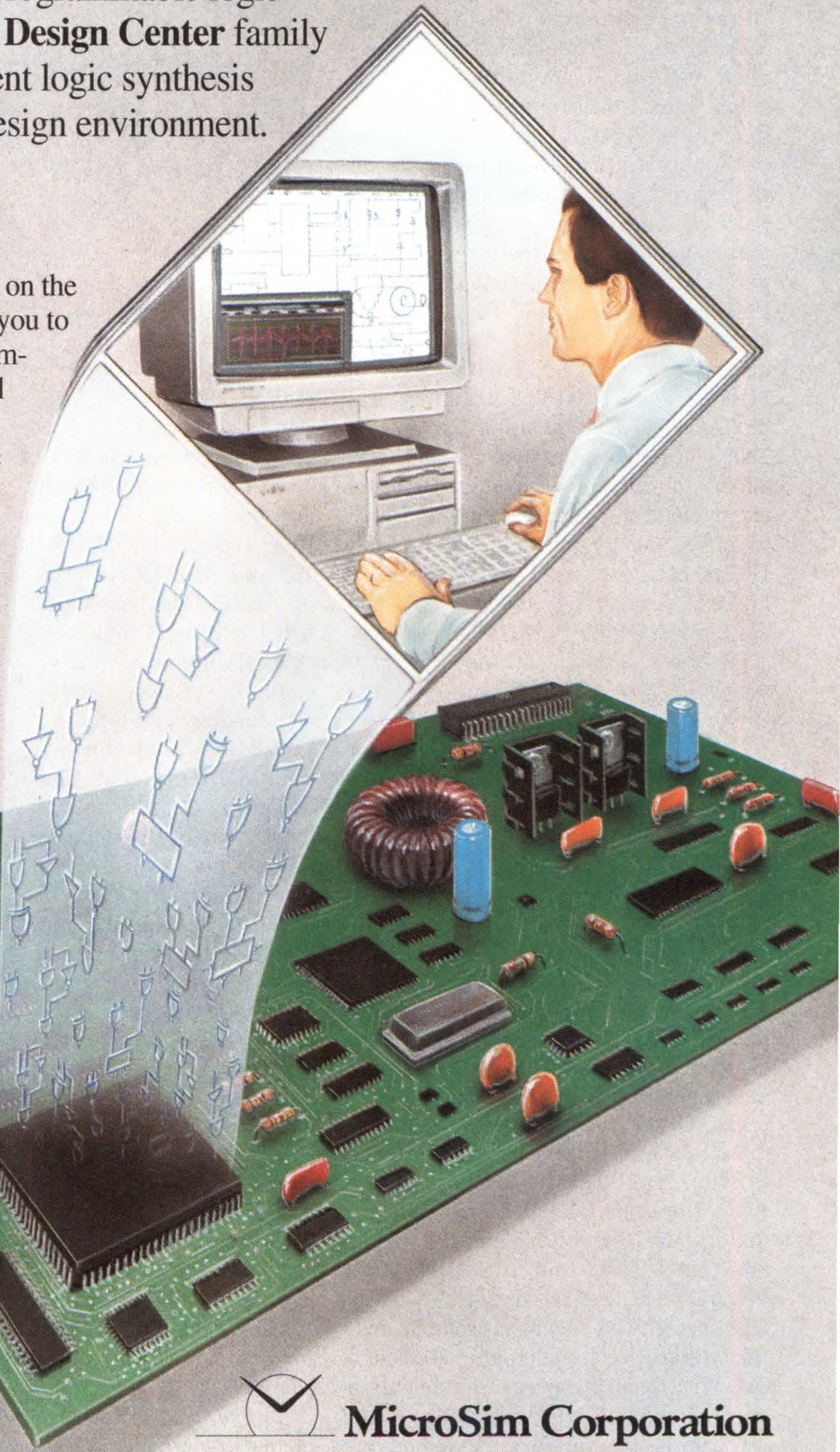

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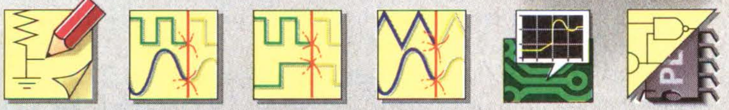

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ICs emulate fader potentiometers

Using dual current-feedback input stages that drive a pair of multipliers, Linear Technology's LT1251 and LT1256 provide for easy gain adjustment of signals from dc to 40 MHz. A single 0 to 2.5V-dc input voltage linearly fades the output signal between the two inputs. Internal control circuits set the gain of the multipliers and keeps the gain constant with temperature. The patent-pending architecture results in gain-control accuracy that's typically ±1% and a maximum of ±3%. The current-feedback architecture of the amplifiers results in a bandwidth of 40 MHz for gains from 1 to 10, and typical distortion of 0.001% when the gain is 100%. Other specifications include a low 2.5 mV of control feedthrough, 40 mA of output current, supply range of ±2.5V to ±15V, and 13 mA of supply current. Differential gain and phase are 0.1% and 0.1°, respectively. The 1251 has circuitry optimizing it for fader applications; the LT1256 is optimized for gain control. A 14-pin DIP version costs $5.76 (1000); SOICs, $6.06.

—by Anne Watson Swager

Linear Technology Corp, Milpitas, CA, (408) 432-1900. **Circle No. 478**

IF ICs aim for flexibility

A line of general-purpose intermediate-frequency (IF) ICs from AT&T Microelectronics are flexible, programmable, integrated alternatives to discrete components for digital-cellular and other digital-communications systems. The 5V ICs comprise a 150- to 450-MHz quadrature modulator (the W2009), a 100-MHz programmable AGC amplifier (the W1466), and two quadrature demodulators (the 45- to 86-MHz W1452 and 10- to 86-MHz W1575) with integrated AGC. The AGC amplifier in the receiver products feature digitally controlled gain steps of 3 dB. With accurate programmable gain up to 69 dB and total gain over 75 dB, you can use the quadrature-demodulator circuits for both the base station and the terminal. Wide (8-MHz) I/Q bandwidths suit narrowband-voice or wideband requirements using QPSK, GMSK, DQPSK, or QAM modulation. The ICs also feature a power-down capability. Prices range from $2.50 to $4.50.—by Anne Watson Swager

AT&T Microelectronics, Allentown, PA, (800) 372-2447. **Circle No. 479**

Isolated thermocouple-measurement system costs $64/point

Looking much like the vendor's DaqBook units that add data-acquisition capabilities to notebook PCs, the MultiScan/1200 makes isolated measurements on up to 744 type J, K, T, E, R, S, B, or N thermocouples at speeds as high as 147 channels/sec, with resolution as fine as 0.1°C, errors as low as ±0.5°C, and a cost as small as $64/point. The unit connects to both notebook and desktop PCs; it includes IEEE-488 and RS-232C/RS-422 interfaces. The base unit, which houses 24 channels, controls up to 15 daisy-chained expansion chassis, each accommodating two 24-channel, screw-terminal-input scanning boards.

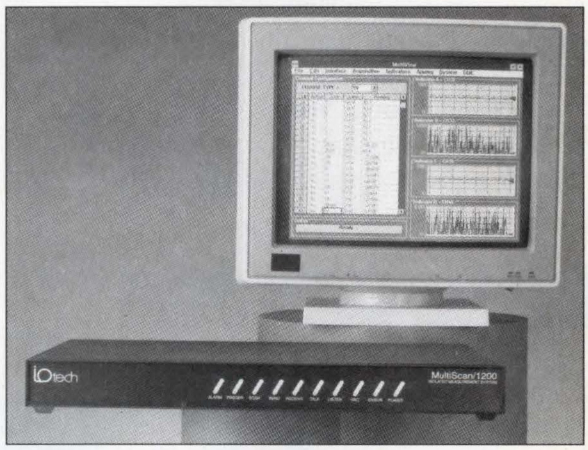
The unit's 16-bit, 20k-sample/sec successive-approximation ADC is ohmically isolated from ground. Relays whose rated life is 10^8 operations connect the signals to the ADC. The inputs withstand 250V peak between channels and from any channel to the output or ground. You can choose scanning boards of two types: One accepts the listed thermocouples and ac and dc voltages from ±100 mV to ±10V full scale. The other accepts ac and dc voltages between ±250 mV and 250V full scale. With either board, you can program gain individually on each channel.

There are three measurement modes. To reduce ac-line-related artifacts, the ADC spaces 32 readings over a line cycle. The unit can also integrate over 2, 4, 8, 16, or 32 line cycles. In the multichannel scanning mode, the ADC can take single readings on each channel (up to 147 channels/sec) or can remain connected to individual channels long enough to acquire and average 2 to 32 readings. In the high-speed burst mode, the ADC acquires single-channel data as fast as 20k samples/sec. The unit performs y=mx+b offset and gain scaling using separate coefficients for each channel. It can monitor inputs for alarm conditions. When it detects an out-of-limits input, it can report the alarm and increase its scanning rate. The unit, which includes a real-time clock, stores readings in 256 kbytes of RAM. You can expand the RAM to 8 Mbytes by plugging in SIMMs.

Two MS-Windows-based applications accompany the unit. One allows quick configuration of the operating parameters; the other permits a 32-channel display. Drivers are also available for several third-party data-acquisition packages. The base unit costs $1495. Both types of 24-channel scanning boards cost $995 each. Expansion chassis also cost $995 each. Thus, a 744-channel system costs $64/point, a 24-channel system costs $104/point, and additional points in any system that has an expansion chassis with an open slot cost $41 each. Delivery is four to six weeks ARO.

—by Dan Strassberg

IOtech Inc, Cleveland, OH, (216) 439-4091. **Circle No. 480**



A 16.75×12×1.75-in. unit houses a 24-channel version of IOtech's MultiScan/1200 isolated thermocouple data-acquisition subsystem, complete with screw-terminal inputs and cold-junction compensation. Expansion chassis of the same size house 48 channels. Up to 15 of them daisy-chain to the main unit.

Camera IC digitizes images on chip

The ASIS-1070 CMOS IC from VLSI Vision integrates a 160×160-pixel photodiode image-sensor array with enough active circuitry to produce an automatic-exposure camera. You can select video output in analog mode, complete with synchronization pulses, or in digital mode as 8-bit parallel or as serial data. The IC operates with a frame rate of 0.5 to 24 frames/sec. The effective image-array size is 1.68×1.68 mm, and you can select from four image formats of 120×120, 120×160, 160×120, or 160×160 pixels. You can also select between external, or on-chip automatic-exposure control. The auto-exposure control has a range of 2000:1, enabling the use of fixed-aperture lenses. Additional on-chip automatic black-level calibration maintains image stability without external components. The IC consumes less than 100 mW of power and comes in a 44-pin PQFP. Price is \$10 (10,000).—by Brian Kerridge

VLSI Vision Ltd, Edinburgh, UK. (31) 539-7111. **Circle No. 481**

Electronics/environment conference predicts product take-back

What to do about end-of-life electronic products and their effects on the environment was the topic of the IEEE-sponsored International Symposium on Electronics and the Environment, which took place on May 2 through 4 in San Francisco. Old computer and electronics equipment cause landfill problems not only because of their volume but also because of the hazardous nature of their content: About half of the 700 materials used in such equipment's manufacture are hazardous.

Draft legislation mandating that electronic manufacturers take back their end-of-life products is on the table in both Germany and the Netherlands. The European Union is also discussing the issue, and such legislation won't be far behind in the United States, according to one speaker at the symposium, Gerald Hane, staff member of the House of Representatives' Subcommittee on Technology, Environment, and Aviation.

US computer manufacturers with plants in Europe, such as Digital Equipment Corp, Hewlett-Packard, IBM, and Xerox, are already planning for such laws. For example, Lutz Kaiser of IBM Deutschland, outlined IBM's ecological product strategy, including extensive product recycling and possible "function leasing," in which a manufacturer must retain environmental stewardship of a product. Also setting the pace in the United States is AT&T, which offers Life Cycle Design Analysis, a program that stresses resource conservation. AT&T operates a materials-reclamation center with collection sites in 12 cities.

Another speaker, Kees Zoetman, deputy director general for environmental protection in the Netherlands, outlined waste- and pollution-cutting steps in the Netherlands, which targets materials recovery of 70 to 90%, except for 30% for polymers, by 2000. Zoetman also called for tax breaks for manufacturers meeting "eco-label" standards. To meet the standards, TVs would consume less than 5W of standby power, printed wiring boards would contain less than 0.1% of bromide chlorine, and the amount of allowable cadmium in a CRT would depend on the unit's weight.

Advocating industry-led recycling and "valorization" was Yvon Marty of Alcatel-Alshthom (France). "Valorization" refers to the means of getting at the value in end-of-life products after collection and sorting. Such means include parts recovery, recycling, and clean incineration with energy recovery. A "reverse-distribution" scheme would have users return products to the point of sale, which, in turn, would return the products to reprocessing plants. Manufacturers would also have to "embed" easy dismantling for recycling into product design, Marty said. France, which now dumps 1.3 million tons of electronic products/year aims at processing 2.1 million tons for value retrieval by 2004.

One problem remains, however: Who will pay for these recycling efforts? Patricia Dillon of Tufts University spoke on this topic, discussing how manufacturers, retailers, and municipalities will have to share the burden. Dillon expects to see the emergence of pool organizations and company-operated recycling facilities.

—by Jim Lippke, Contributing Editor

Comprehensive test package anticipates EMC Directive

A combination of software and two test instruments helps you identify tests required by Europe's electromagnetic-compatibility (EMC) directive relative to your product and to perform important parts of those tests in-house. The package from Seaward Electronics allows you to perform pre-compliance tests during product development or before formal test-house checks. It also lets you "self-certify" compliance, depending upon product category.

The Expert Consultant MS Windows software (£495) part of the package identifies routes to compliance and explains standards appropriate to your product. The software also helps you to compile EMC test plans, or "Technical Construction Files." The diagnostic section of the software details test-and-measurement methods and explains how to interpret test results. A section of the software covers EMC-problem countermeasures.

The Sceptre test instrument (£1980) is a spectrum analyzer with a built-in line-impedance-stabilizing network (LISN). Sceptre links to a PC via an IEEE-488 bus interface for control and for display and analysis of data. The analyzer has a 150-kHz to 450-MHz input frequency, and has preset bandwidth and detection settings in accordance with International Special Committee on Radio Interference (CISPR) requirements. The analyzer measures conducted emissions and makes relative radiated measurements using antennae or near-field probes.

The EMC directive also specifies EMI-susceptibility requirements. To meet those requirements, the company offers the Mace test instrument (£2980), which simulates line interference and produces ESD to test EMI. Mace performs programmable voltage-dip testing to prEN50093, fast transient testing to IEC 801-4, and ESD testing to IEC 801-2.

—by Brian Kerridge

Seaward Electronics Ltd, Peterlee, UK. (91) 586-3511. **Circle No. 482**

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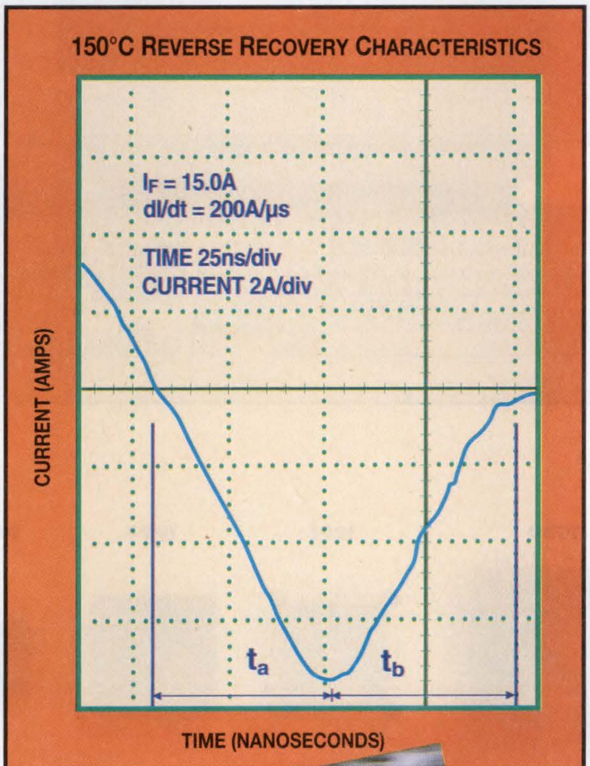

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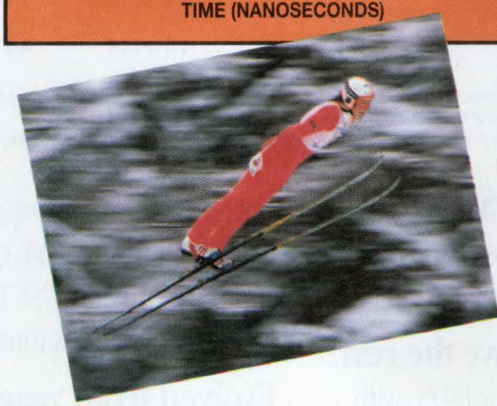

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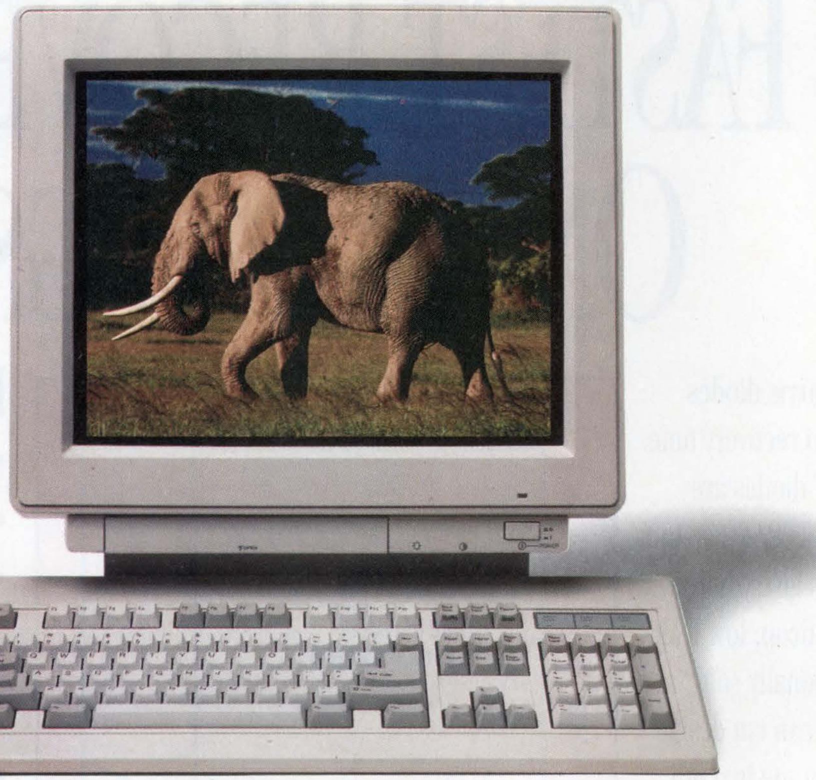

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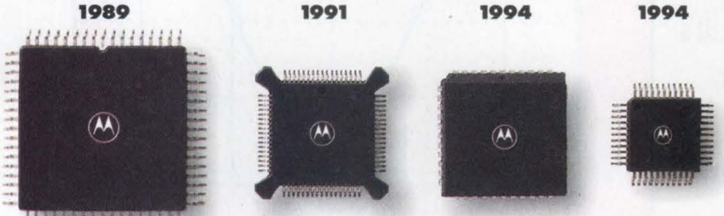

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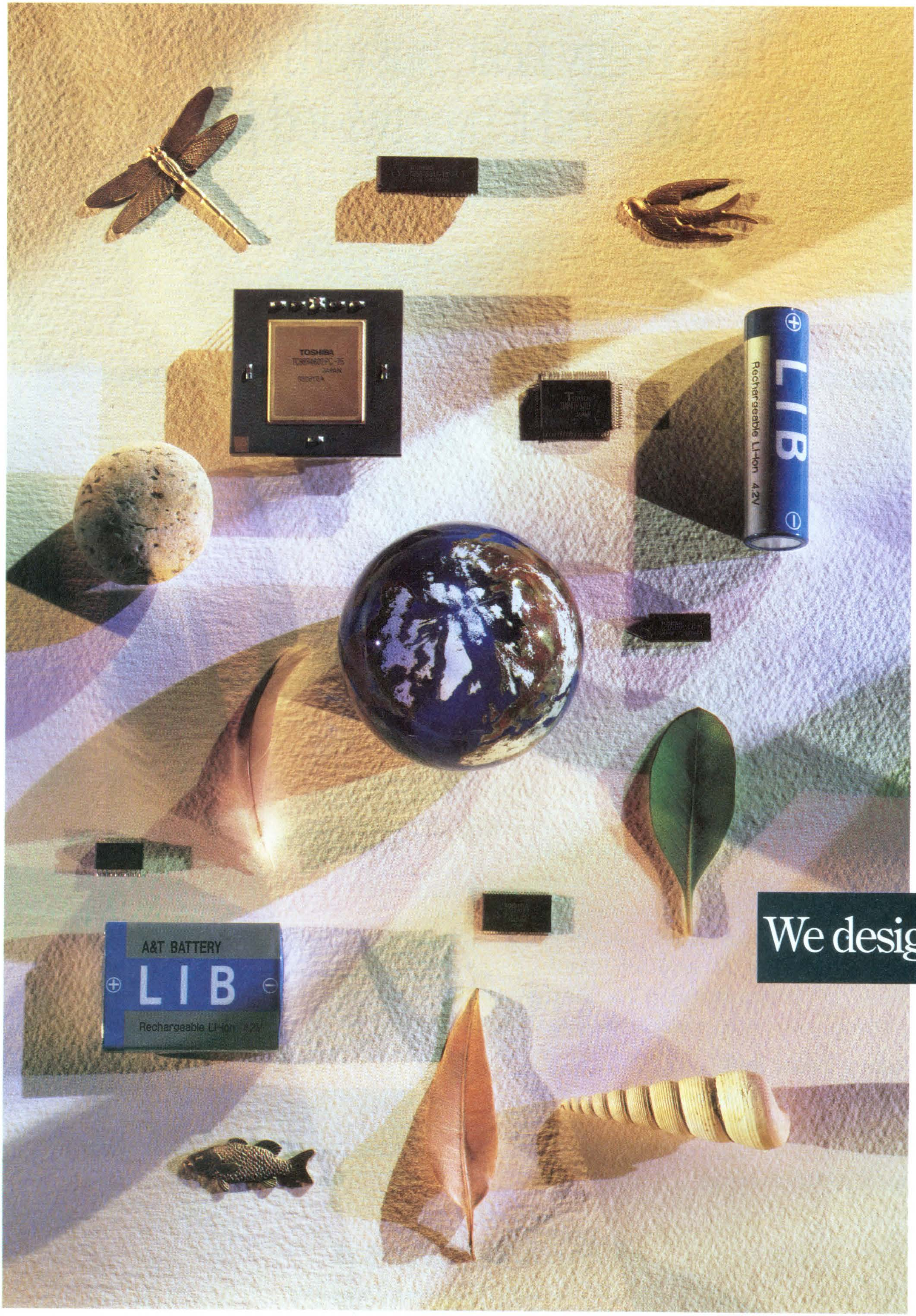
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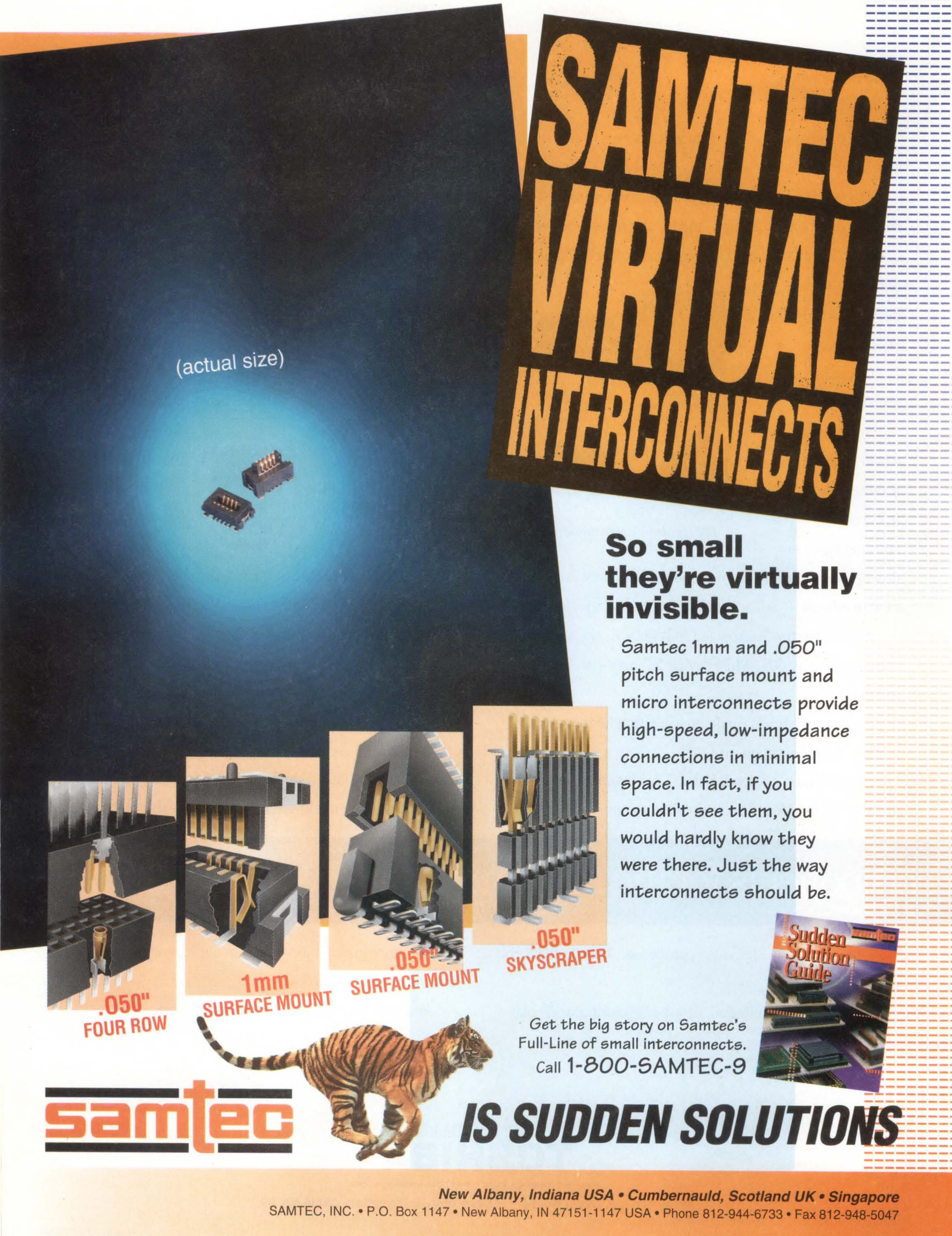
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CIRCLE NO. 27

Connecting physics, convergence, and EEs

I am not in a position to comment on "Step-by-step procedures help you solve Spice convergence problems" (EDN, March 3, 1994, pg 121), except that, in my experience, I've found convergence problems are often a warning that there may be a flaw in your approach to a problem.

Spice is a linearized program that frequently depends on the less stable of device parameters, which is something I (as physicist and electrical engineer) learned early on—but that engineers without a thorough physics background may not pick up. EEs must carefully classify parameters for elements of circuits or systems and must use an approach that avoids obvious pitfalls.

When Kirchhoff developed his laws he was aware that network properties must be developed in terms of both input and output parameters as well as two parameter types, which are now sometimes called across and through. Voltage, because it represents a difference (such as in height), can be called an across (or covariant) variable, whereas current, which is flow-variable, can be called a contravariant variable. Relations must be developed in these terms.

These ideas are key to what is called in physics "dimensional analysis," which is a subject electrical engineering typically neglects. When these principles are applied to the active devices used with Spice, it's immediately evident that the diode equation is of far greater importance than beta for bipolars or mu for triode tubes. When the linear simultaneous equations for a 2-port are rewritten in terms of the diode equations, a simpler and more meaningful approach results—and it just may be free of many convergence problems.

Keats A Pullen Jr
Kingsville, MD

Design needs warning label

The circuit in "Off-line power supply requires few parts" (Design Ideas, February 17, 1994, pg 55) provides no isolation from the ac line! It can seriously harm (or kill) unsuspecting users who may inadvertently bridge a number of points in the circuit (except ground) to the neutral of the ac line or any grounded point or surface.

This problem isn't new; it surfaces with surprising regularity. Because the circuit is low cost and unsophisticated, it's likely to be attractive to those with little knowledge of the hazards inherent in such a design. Similar circuits, using the reactance of a capacitor to drop the line voltage to low levels, are commonly used in low-cost battery-charging circuitry. They have the same isolation problems as the published circuit.

Safety agencies would only accept this type of circuitry if it were isolated from the user by high-reliability interlocks and the presence of barriers to prevent the user from coming into contact with any portion of the circuit. They consider all portions of such circuitry to be live.

Arthur E Michael, Editor
International Product Safety News
Middletown, CT

Senior Technical Editor Charles Small responds: This problem is common to any off-line switcher that is nonisolated, as most "cheapy" versions are. Note that *Design Ideas* are just ideas—not complete solutions that comply with UL, VDE, or CSA standards.

Just add a few resistors…and voilá

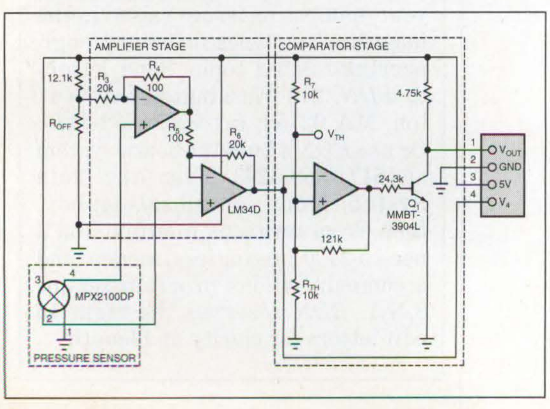


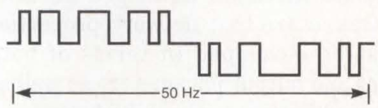
Fig 1 in "Simple pressure switches comprise transducers, comparators, and op amps" (EDN, April 14, 1994, pg 117) needs a few resistor names added. We neglected to label R_3, R_4, R_5, R_6, and R_7 in the schematic. Here is the correct version of **Fig 1**.

Ghost theorist offers harmonics insight

"The right μP simplifies using induction motors to propel electric cars" (EDN, March 31, 1994, pg 48) reminds me of an encounter I had in the late 1960s with a research team that designed a 50-Hz, 3-kW power supply using solid-state devices.

Back then, because of a power shortage, the power-line frequency drift was so great in mainland China that a television signal could not withstand it and therefore needed a stabilized power supply for TV-broadcasting equipment.

The design was based on a theory (unfortunately I cannot recall its author) that when a frequency synthesizer generates a series of pulses, the output waveform resembles the following:



With proper timing, number of pulses, and correct width, the theorist claimed that the highest harmonic is the 7th. Comparing this idea with the article in EDN, the older method has the advantage of a definable harmonic, which may reduce the risk of EMI and cause less iron loss in the motor (the filtering isn't free), and results in a greatly simplified circuit (clock and counters). Obviously the method is appropriate in different power and frequency applications.

Robert Shiyang Gao
Vicon Industries Inc
Melville, NY

Sound off

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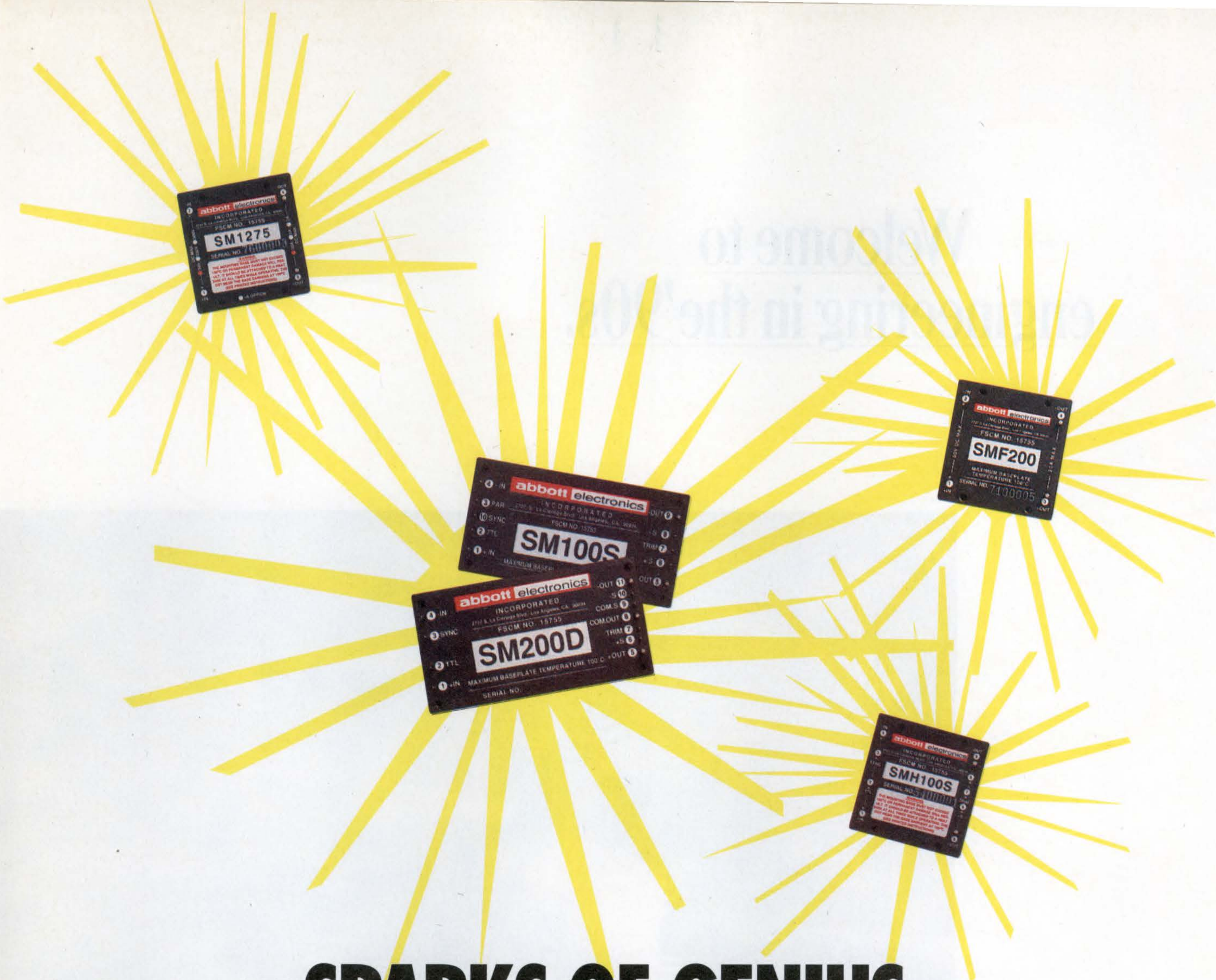

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PEAK POWER IN WATTS	100 / 280	50 / 100	100 / 200	375	300
INPUT VOLTAGE (VDC)	16-50 and 200-400				Mil-STD-1275A Mil-STD-704A
OUTPUT VOLTAGE (VDC)	2, 3.3, 5, 5.2,12, 15, 24, 28		±5, ±12, ±15	—	—

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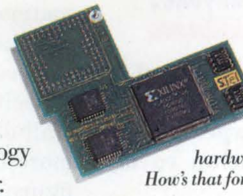

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CIRCLE NO. 194

EDITED BY JAMES P LEONARD

Creative design advice, anyone?

I am bumping up against my level of ignorance, but I hope that you can offer some technical expertise to point out an easy solution to my problem.

I need to be able to continuously determine the position of an object moving past a given point at a variable speed. The positioning of the object must be accurate to approximately 250 places per inch; any solution must be capable of being installed in a device 0.5 mm thick.

A slow 4-/8-bit microcontroller can be used to store data and perform calculations; any solution must be low-cost, easy-to-make and install, and reliable. I hope you or your readers can help.

Robert Daggar, President
Creative Associates Ltd
Reston, VA

Senior Technical Editor Charles Small responds: Without more specific information about this application, a recommendation would be tough. Possible choices include laser, LED, ultrasonic, capacitive, mechanical, magnetic, and Hall-effect sensors (and perhaps even more types I don't even know of). To figure the best type of sensor for your application, you'd need to list the medium through which the measurement is to be made, the material that the sensed object is made from, the distance between the sensor and the sensed object, and the size of the spot that is available for measurement. The requirement that the fixture be <0.2 in. thick is rather puzzling. To help solve your dilemma, write back with specific information when it becomes available.

Open forum for design advice

I am conducting an in-depth analysis of an LTC1043 application (reference Linear Technology's 1990 Linear Databook—LT1057/1058 Data Sheet (pgs 2-243, example "Analog Divider")), as I'd like to incorporate it into a middle-range production plan (hundreds of devices per year). The problem is that the linearity error of such a circuit is quite high (approximately ±0.6% FS and more), whereas its specular version (LTC1043 Data Sheet (pgs 11-23, example "Analog Multiplier")) exhibits a satisfactory error of <±0.04% FS worst case.

I unsuccessfully spent a lot of time trying to understand the reason for this. I've put a request in to Linear Tech for help, but before I give up on the idea of using such a divider, I'd also like to request the advice of *EDN* readers.

Paolo Zambusi
R&D Management
Società Italiana Controlli e Collaudi Srl
Selvazzana Dentro, Italia

EDN BBS user scans for PCI-chip info

An EDN reader logged-on to our electronic BBS (bulletin-board system) to request contact information for PLX Technology, which makes PCI chip sets, as well as references for other companies that make PCI chip sets for interfacing general-purpose hardware—specifically a general-purpose PCI interface chip in which the interface acts as a master as well as slave device on PCI.

Senior Technical Editor Gary Legg responds: You can reach PLX Technology (Mountain View, CA) at (415) 960-0448. PLX has a chip that provides an interface between the PCI bus and an i960 processor. For a more general-purpose interface chip, try Applied Micro Circuits Corp (San Diego, CA) at (619) 450-9333. AMCC has been working on a chip that will serve as an interface between the PCI bus and virtually any microprocessor; it will probably be available by the cover date of this issue.

Search for long-lost interface card

Years ago, my company purchased a μANALYST 2000 system from North West Instrument Systems Inc of Beaverton, OR. This system is a logic analyzer operating at 100-MHz timing and 10-MHz state. It comprises an electronics box having the usual connecting pods on one side and an interface to a PC for display and control on the other. The system initially worked well but was packed away for a while during a company move. We now wish to use the system again but find that the special interface card that fitted into a PC is missing. We are seeking a replacement for the missing interface card but have been unsuccessful in locating North West Instruments; we suspect that the company has moved or has ceased operating. Maybe your readers could help locate either the company or the interface card.

Roger A Munt
Senior Design Engineer
August Systems Ltd
Crawley, West Sussex, UK

Fruitless search for title in France

In *EDN Hands On!* (March 3, 1994, pg 173), Charles Small reviewed a book entitled *Microcontroller Technology, Data Acquisition and Process Control with the M68HC11 Microcontroller* by Frederick Driscoll, Robert Coughlin, and Robert Villanucci. I have searched—without success—to locate this book, which

Ask EDN

Macmillan Publishing Co publishes under the Merrill imprint. Any advice?
Guy Lemoine, Technical Director
ELBO Electronique
Ste Elbo, Courmangoux, France

Contact Macmillan's overseas distributor, which is located in the UK, and refer to ISBN 0-02-330555-X for the text and 0-02-330556-8 for the solution manual:
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Hemel, Hempstead
Herts HP2 7EZ, UK
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fax (44) 442-882277.

Seeking CCITT documentation

I am writing a C program in MS-DOS to convert a text file to a CCITT T.4 fax format file to send a fax with a fax/data modem.

Where can I find a copy of the CCITT T.4 standard? Also, where can I buy the C routines to convert a text file to CCITT T.4 fax standard or TIFF Group 3 for fax?
Keith Chow
Eliwell Spa
Pieve D'Alpago (BL), Italy

For CCITT information, contact the ITU:
International Telecommunications Union (ITU)
Place des Nations
CH-1211 Geneva 20
Switzerland.

New or used will do

For some time now, I've been searching for a copy of *The PLL Synthesizer Cookbook* by Harold Kinley (Tab Books, Blue Ridge Summit, PA). Perhaps an EDN reader would be willing to sell me a used copy.
Frank Lewon III
7614 Marion Ct
Saint Louis, MO 63143

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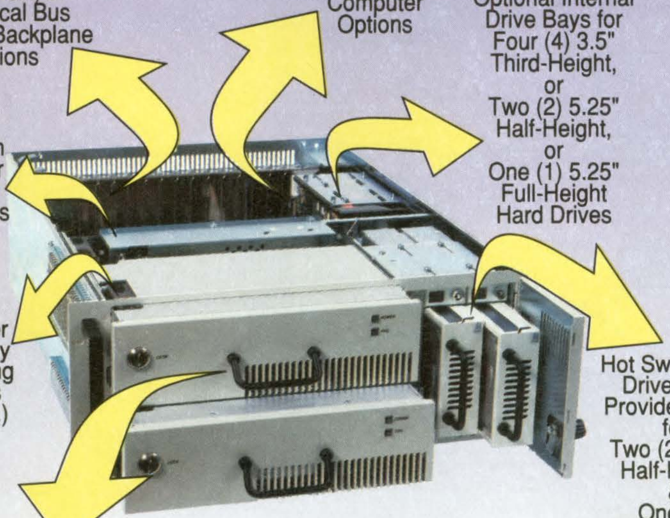
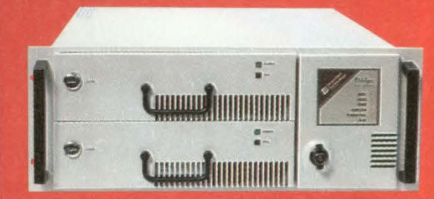


Modules shown are options for the FTS900 Fault Tolerant System



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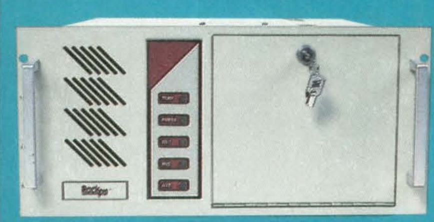
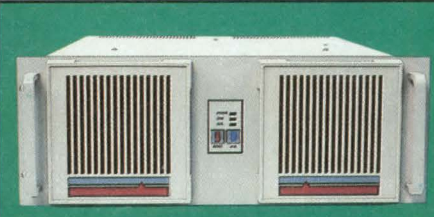
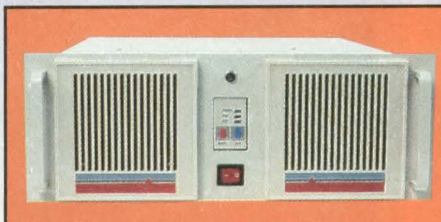


10,14,16 Slot - ISA, EISA or PCI Local Bus
CRM816

14 Slot ISA, EISA or PCI Local Bus
w/Built-In Monitor
CRM814



20 Slot ISA
CRM720



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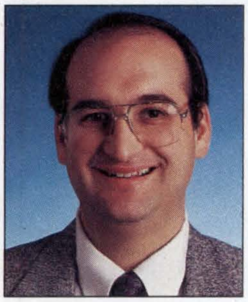
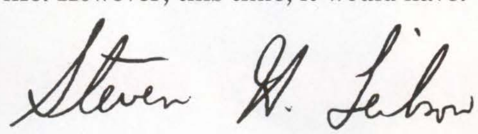


In my last editorial, I recounted an experience I'd had with an improperly issued parking ticket and suggested that bar-coded license plates and scanners might be a better way to track vehicles than handwritten paper tickets. This time, I want to finish this line of thought by recounting a story of an improper credit-card charge and making a case for smart cards.

I admit that I was unconvinced by the smart-card advocates until late last year. Then, I became a convert. I purchased some tires from a well-known retailer and charged them to my account. Two nearly equal charges appeared on my next credit-card bill. It took me two months to get this matter cleared up. The next month, the company billed me for interest on the unpaid fictitious charge. That charge took another month to clear up.

As with the undeserved parking ticket, it's almost impossible to prove you didn't charge something. You must force the credit provider to admit that it cannot produce a duly-authorized charge receipt. However, if this retailer used smart cards, it would be a simple matter to drop by the local retail store and pop my card into a reader to prove that the purchase never took place. Better yet, I could pop the card into a home reader and transmit the necessary information (encrypted, of course) to the company's billing office by phone.

Only when I can keep secure, duplicate records can I be safe from billing errors of this sort. Credit cards with magnetic stripes simply cannot store enough information to serve this need. The ever-rising spiral of technological advancement doesn't always simplify my life. However, this time, it would have.



Steven H Leibson
Editor-in-Chief

Note: This is the latest in a series of articles on C-Quad engineering. C-Quad (or C^4) stands for the ***convergence*** *of* ***computer, consumer,*** *and* ***communications*** *technologies.*

Jesse H. Neal
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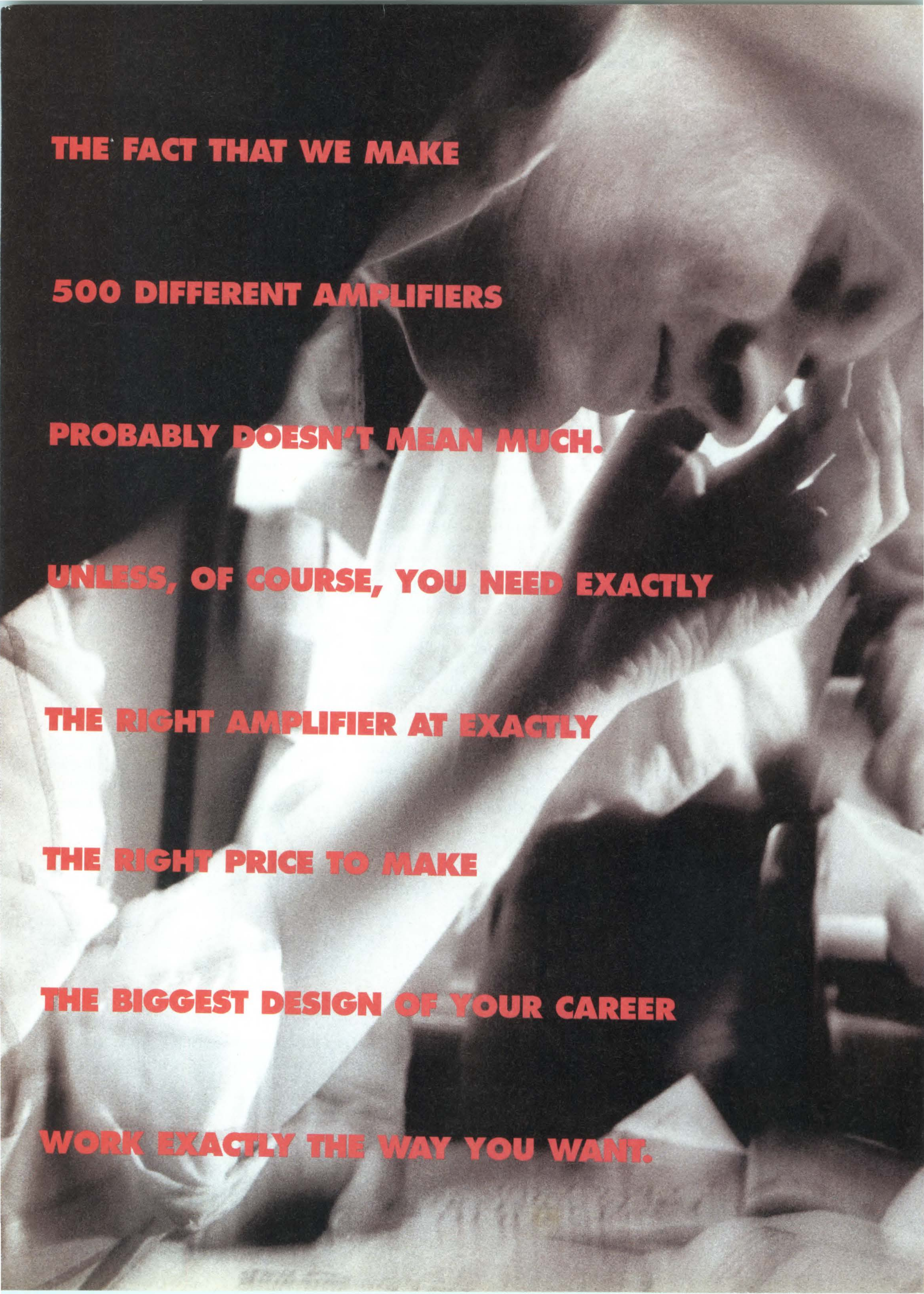
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Ignore packaging effects at your peril

RICHARD A QUINNELL, Technical Editor

Your high-speed ASIC design looked great in simulation and matched all its test vectors. So why didn't it work when you plugged it in a board? Maybe you didn't account for packaging effects.

There are hundreds of package types available for housing your IC design. Even though system or budget constraints eliminate some options, you have plenty of opportunity to make package-related decisions throughout the IC design process. You may need that flexibility. At today's signal rates, the electrical behavior of the packaging can undermine an otherwise-sound IC design unless you make those decisions carefully.

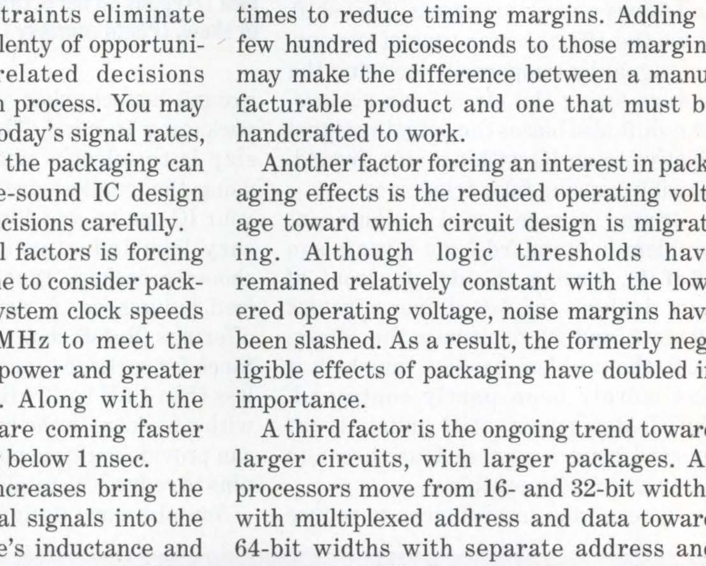
A confluence of several factors is forcing designers for the first time to consider packaging effects. For one, system clock speeds are pushing past 100 MHz to meet the demands for more CPU power and greater networking data rates. Along with the increased clock speeds are coming faster edge rates, now dropping below 1 nsec.

Together, these two increases bring the spectral content of digital signals into the realm where the package's inductance and parasitic capacitance can create a significant noise problem. Lead inductance translates into ground bounce. Mutual inductance and lead-to-lead capacitance provide paths for coupling signals into adjacent lines. Further, the impedance changes that occur at bond-wire junctions, along the lead frame, and at pin posts cause reflections. The reflections are internal to the package; you cannot observe or accommodate them during system debug. You must design for them.

These noise sources degrade system performance because they add to the time for a signal to stabilize before being clocked by the next stage. With ever-increasing clock frequencies, that additional delay combines with shrinking cycle times to reduce timing margins. Adding a few hundred picoseconds to those margins may make the difference between a manufacturable product and one that must be handcrafted to work.

Another factor forcing an interest in packaging effects is the reduced operating voltage toward which circuit design is migrating. Although logic thresholds have remained relatively constant with the lowered operating voltage, noise margins have been slashed. As a result, the formerly negligible effects of packaging have doubled in importance.

A third factor is the ongoing trend toward larger circuits, with larger packages. As processors move from 16- and 32-bit widths with multiplexed address and data toward 64-bit widths with separate address and data paths, I/O pin count has quadrupled. Hand in hand with the larger package styles



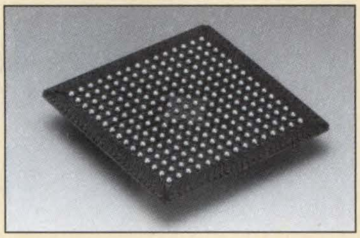
Design for packaging is not yet a standard part of CAD tools. Fortunately, vendors are developing the needed tools. The addition Harris Semiconductor is developing for its Fastrack CAD tool, for example, aids in package selection, assists in bond-wire placement, and automatically includes package Spice models in your simulations.

HIGH-PERFORMANCE PACKAGING

have come longer chip-to-pin leads and closer lead spacing. The longer leads add inductance and propagation delay. The tighter spacing increases the coupling between signal leads, increasing noise.

Many designers have run afoul of the most prominent packaging effect: ground bounce. In brief, ground bounce is the temporary shift in ground (and V_{cc}) an IC sees inside a package because of an L di/dt drop in the power lead caused when an output driver switches and draws a surge of current. That shift slows the effective rise time of the output signal by temporarily lowering the voltage swing the circuit can achieve. The shift also biases the outgoing signal relative to an IC with a stable ground, possibly causing false triggering.

(a)


(b)

The plastic ball grid array brings traces from the IC to vias on the substrate's top surface (a), then back to a solder-ball grid on the bottom (b). The trace pattern is such that two adjacent I/O pads on the IC can connect to traces differing by 0.5 in. in length, a potential source of skew. (Photo courtesy LSI Logic)

Ground bounce posed a significant problem in standard logic 5 years ago (**Ref 1**), forcing the development of new designs for I/O-driver circuits (**Refs 2** and **3**) to reduce the effect. Still, the problem has not vanished; it has merely been partly contained. ASIC designers still must treat ground bounce as a serious threat to their circuits' operation.

You can take several steps to reduce ground bounce when you design with packaging in mind. The most obvious step is to select a small package. By using the smallest package into which your IC can fit, you eliminate unnecessary lead inductance. You can also choose a package type that offers low lead inductance. A survey of package offerings (**Ref 4**) shows that lead inductance for package types can range from less than 1 nH to 12 nH. If you're stuck with a package in the higher range, you can provide multiple power and ground pins to reduce the total lead inductance.

You also have design options within the package. The method you use to attach the IC die to the lead frame affects the overall inductance that causes ground bounce. You can choose between a rim-connected IC and an array-connected IC. In an array-connected IC, the chip's I/O bond pads are scattered throughout the device. By bumping the pads and attaching the die to the lead frame in a flip-chip configuration, you minimize the inductance of the IC's metal-layer traces and can achieve short runs within the lead frame. A rim-attached device, with all I/O pads on the die's perimeter, is less costly, however, and may be a forced choice.

Even so, you have attachment choices. A bumped die with a rim-attached bonded lead frame, for example, produces a much lower inductance than does a traditional wire-bond attachment. If cost constrains you to use wire bonds anyway, you can reduce inductance on power and ground leads by using multiple bond wires in parallel from the lead frame to the die. To use this approach, though, you must remember to design-in extra bond pads on the die, even if the wires go to the same lead.

Don't think that, once you've addressed ground-bounce, you're done. Crosstalk, reflections, and skew are also becoming significant packaging effects in high-performance designs. Crosstalk, for example, increases with signal frequency. It stems from mutual inductance and parasitic lead-to-lead capacitance in the lead frame, both being aggravated by the trend toward larger packages and finer lead pitches.

Longer-lead packages also mean that

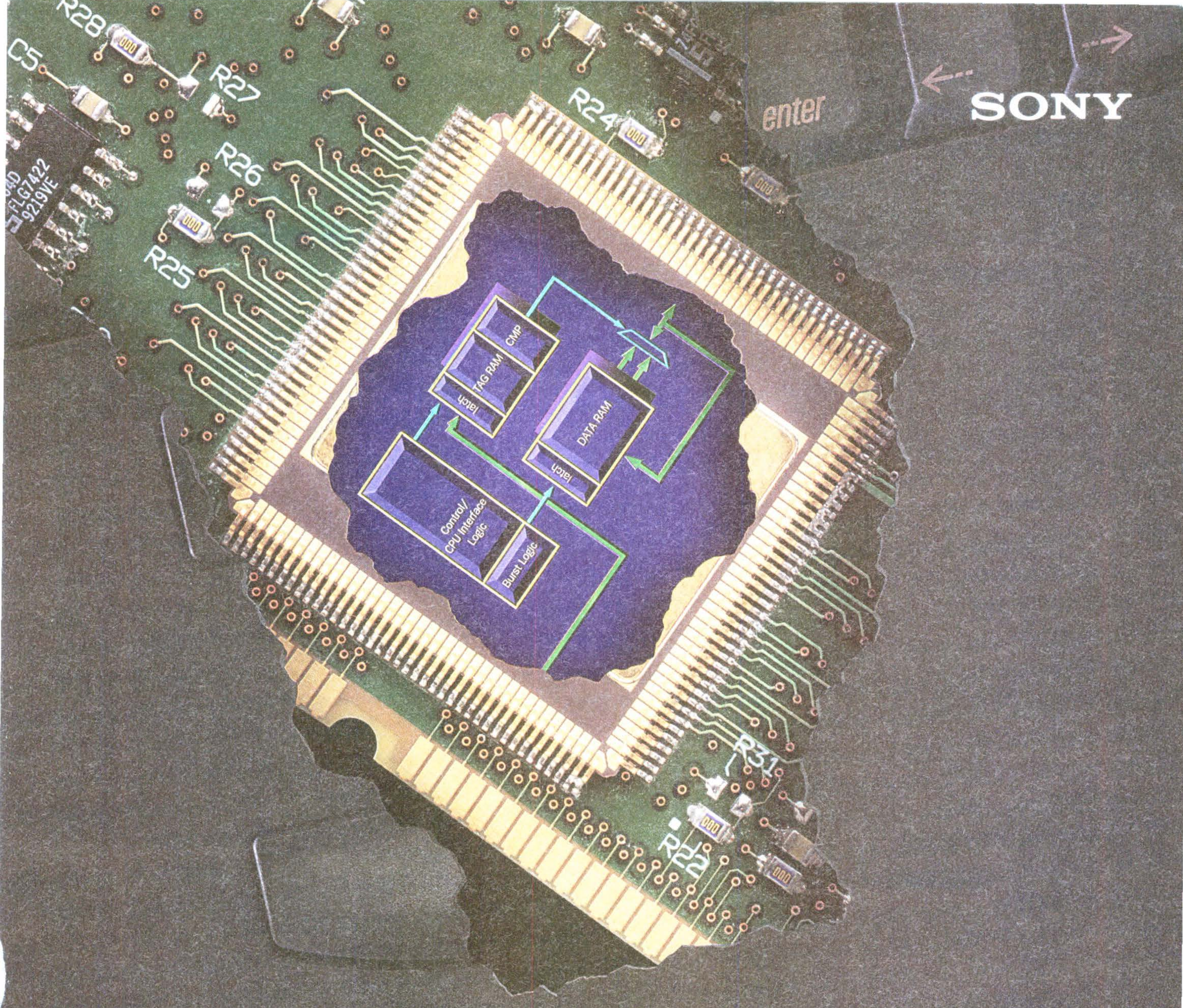
LOOKING AHEAD

The need to include packaging effects in IC design is only beginning to become widespread. As a result, few tools are available to automate the effort of including package effects in simulation. Awareness of packaging's importance is growing, however, and the CAD community is starting to respond.

One design-for-packaging tool under development comes from Harris Semiconductor. Faced with a need to account for packaging in its wireless communications-IC designs, Harris is modifying its Fastrack design software to incorporate packaging automatically. The enhancements provide designers with the characteristics of more than 400 packages. They allow quick initial estimates of packaging effects to facilitate package selection and to provide detailed models for final Spice simulations. The software carries the package characteristics throughout the design process, including preparation of bonding diagrams for final manufacture.

Another indication of packaging's growing importance is the creation of an IEEE Conference on Electrical Performance of Electronic Packaging. The conference, now in its third year, has grown tremendously in popularity, drawing both academic and industry experts in package design and circuit modeling. The 1994 conference will take place in Monterey, CA, November 2 to 4. Call (602) 621-3054 for information.

Although it will be painful for early adopters, accounting for package characteristics during design will slowly become a normal part of design. And, as with logic simulation, we'll come to wonder how we ever got anything to work without it.


SONY
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DATA RAM
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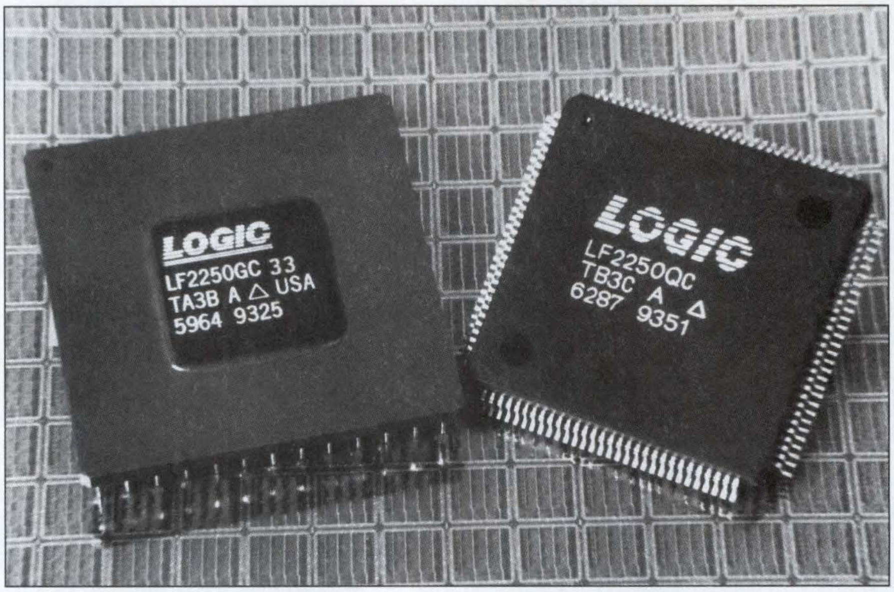
reflections, caused by impedance changes from lead frame to I/O pin, can return just as circuits with sub-nanosecond rise times are crossing the switching threshold. Further, the package elements can form an RLC circuit that can ring like a bell following a high-speed transition, increasing circuit settling time. A package choice that can reduce this problem is one that allows multiple lead-frame planes for creating transmission-line leads.

Lead length also affects the signal's propagation delay from die to board. Variations in path length through the lead frame can thus introduce skew that is invisible to pc-board-layout-based timing-simulation tools. That skew is not insignificant. A large pin-grid array, for example, can have as much as a 2-in. difference between its shortest and longest die-to-pin runs. With propagation speeds within the package running 6 to 8 in./nsec, that difference can result in a length-induced skew of more than 250 psec at each end of the signal run. With a cycle time of 10 nsec or less, that half-nanosecond may be fatal.



Packages exhibit vastly different electrical characteristics, so choose carefully. The pin-grid array, for instance, has wide pin-to-pin variations in on-chip delays. The QFP has more consistent lead lengths, but has a greater lead inductance. (Photo courtesy Logic Devices)

Design early for packaging

IC designers have traditionally ignored package-induced crosstalk, reflections, and skew effects, leaving them to packaging engineers. Yet, to catch and declaw these success-killers, your best opportunities occur during circuit design and simulation—the earlier in your design cycle, the better.

For example, when creating the initial floor plan for an IC's layout, you would typically arrange circuit elements to minimize on-chip timing delays. Your decisions, however, may place I/O signals where they might aggravate the package-induced delays. Remember, too, the effect that I/O assignments have on pc-board routing. If you don't pay attention, you could easily lose more in the packaging and board delays than you gain on the die.

You may also find that you're better off cutting your circuit in two. By placing critical signals in an IC with a small package and the rest of your design in the large package, you can reduce the packaging's impact on those critical signals. You may even be able to save money by replacing one high-cost package with two cheaper ones.

To determine the impact of all these packaging effects on your design, you need to know the package's electrical characteristics. Many package providers, unfortunately, give only typical values or upper limits for package inductance and capacitance. When ranges are available, they often refer equally to all package leads. Neither offering proves adequate for simulating critical signals. Ideally, your package supplier can provide lead inductance, capacitance, and die-to-board propagation-delay data for each pin or lead in the package. If the supplier doesn't have this information, however, you may have to char-

FOR FREE INFORMATION...

The following companies contributed their expertise in packaging technology to the creation of this article. For free information on their packaging capabilities, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

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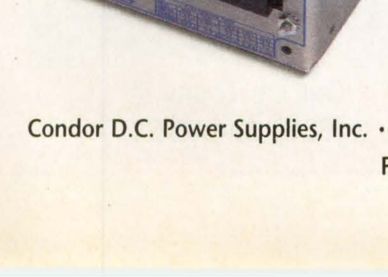

HIGH-PERFORMANCE PACKAGING

acterize the package yourself (**Ref 5**).

Armed with that information, you can begin to simulate the package's effect on your system. Typically, you know the timing of critical signals and the I/O structure you're using early in the design cycle. By using an I/O-cell model driving the LRC circuit representing the package, you can make a preliminary estimate of the package's impact on signal integrity. This provides you with the opportunity to make I/O-pin assignments that help protect critical signals.

Take care in simulations

Later in the design, you can run a full-chip simulation, including the packaging effects. Many IC simulators can't directly account for package effects, however, and you need to be careful in setting up the simulation. One common source of error is that simulators extract a circuit's parasitic capacitance to an ideal ground. To account for ground bounce, then, you must insert an inductor in the simulation model between the chip ground and node zero.

Another common error is to analyze signal integrity in the packaged IC using the fastest possible signals, yet set system timing constraints assuming the slowest possible signals. A simulation that fails under those conditions may prompt an unnecessary redesign. Make sure that your assumptions are consistent.

Admittedly, considering the package's electrical characteristics during IC design is more work. Worse, most design-automation tools force you to add manually the information needed to reflect those characteristics in your simulation, because electronic databases of package characteristics are almost nonexistent. And you may need to characterize your package yourself. Increasingly, though, it's worth the effort. With packaging effects accounted for, your final simulation should provide confidence that your IC design works not only alone, but also when plugged into a board. EDN

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You can reach Technical Editor Richard A Quinnell at (408) 685-0504, fax (408) 685-0504.*

Article Interest Quotient
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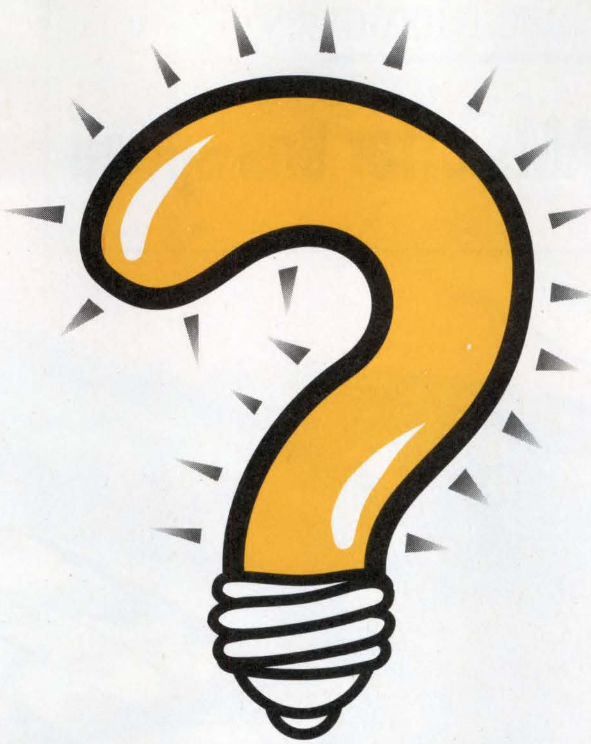
CIRCLE NO. 200

What's the brightest news in A/D price and performance in 1994?



TI's new TLC2543 12-bit A/D converter at $5.25*.

The TLC2543 from Texas Instruments sets a new price/performance point in the marketplace. Its power dissipation is only 5 mW typical. That's 50 percent lower than most 12-bit A/D converters, at about half the cost.

The right stuff. With the TLC2543 you get an on-board 14-channel multiplexer that offers 11 analog-input channels and three self-test channels. This 12-bit A/D converter has a 10-μs maximum conversion time and sample and hold. Plus a system clock and 8-bit control register. And an end of conversion flag makes it easy to interface with microprocessors and DSPs.

TLC2543 Features

- 12-bit resolution A/D converter
- 10-μs maximum conversion time
- Low power consumption — 5 mW (typ), 13 mW (max)
- Power-down mode — 125 μW
- Standard serial interface
- On-chip system clock
- 11 analog-input channels
- Available in 20-pin SOIC, DIP or PLCC packages

New Members of TI's A/D Family

Device	Supply Voltage	Input/ Output	Conversion Speed (Max)	Resolution
TLC2543	5.0 V	11 ch/serial	10 μs	12 bits
TLV1549	3.3 V	1 ch/serial	21 μs	10 bits
TLC1549	5.0 V	1 ch/serial	21 μs	10 bits
TLV1543	3.3 V	11 ch/serial	21 μs	10 bits
TLC1541/43	5.0 V	11 ch/serial	21 μs	10 bits
TLC1550	5.0 V	1 ch/parallel	6 μs	10 bits
TLC1225	5.0 V	1 ch/parallel	12 μs	12 + sign

The TLC2543 in 3.3-V and shrink small-outline versions is on the horizon.

Where you need it. Use the TLC2543 in automotive, instrumentation and a broad range of industrial applications, including motor control, robotics, numerically controlled machine tools and data logging.

Easy migration. Its pinout is compatible with the TLC543 8-bit and TLC1543 10-bit A/D converters from TI. So upgrades are easily achieved with only minor software adjustments.

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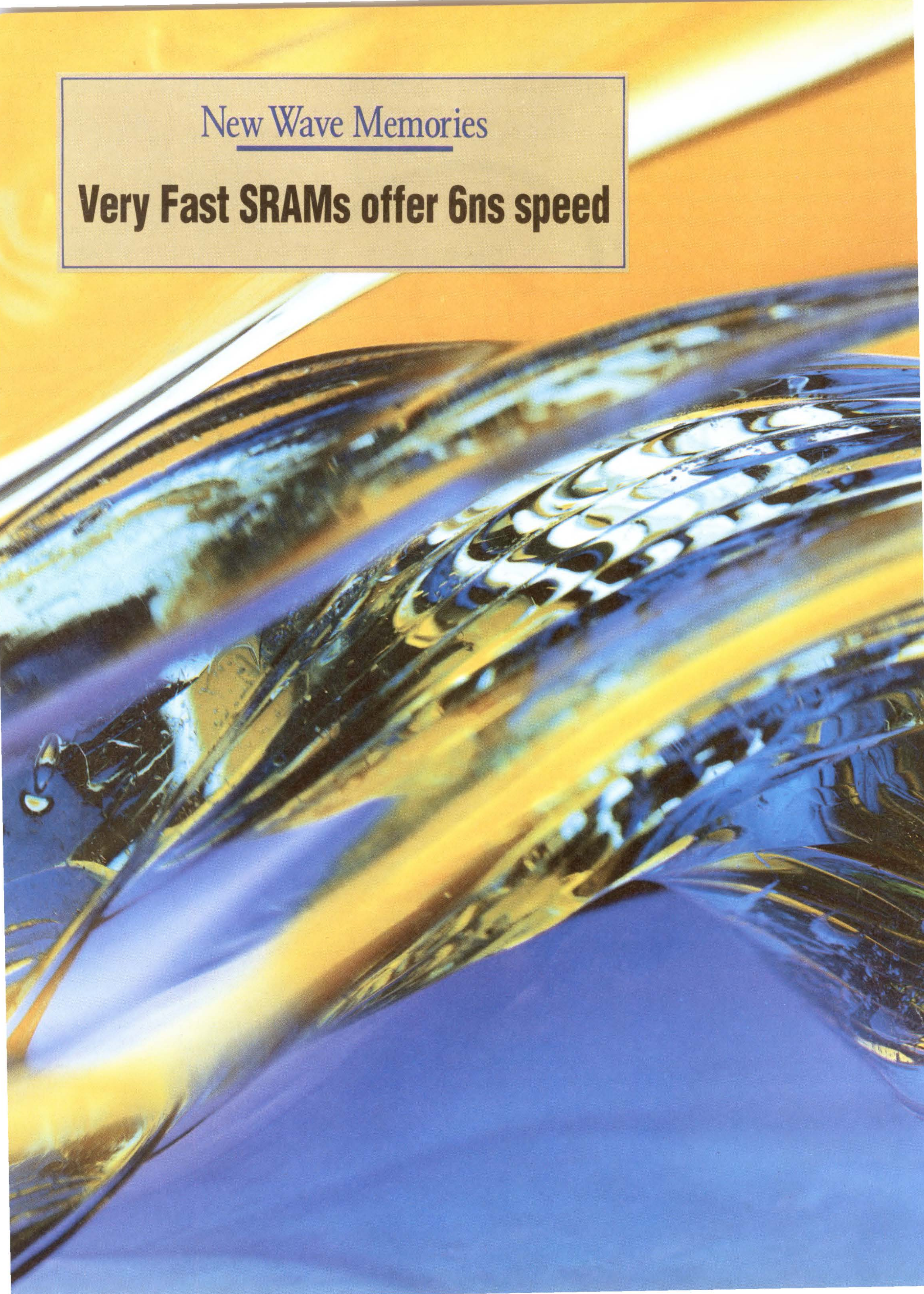

DSP^{x} 94 helps introduce DSP into your designs

Steven H Leibson, *Editor-in-Chief*

Reflecting the growing presence of DSP in all types of product design, this year's DSP^{x} conference delivers a broad range of design-oriented sessions. The sessions are split into three series (100, 200, and 300) to reflect the varying needs of the design and development community. Sessions from all three levels will occur each day of the conference.

The 100 series sessions are introductory and are designed to help the new DSP user. The 200 series sessions are moderated panels. Each panel contains four to eight company representatives who will compare and contrast their company's products in 10-minute presentations. Independent experts will moderate these panels. The 300 series sessions are for people looking for more advanced information. These sessions focus on technical applications of DSP and may include case studies or design examples. The **box**, "DSP^{x} '94 conference program" provides a complete list of the three sessions.

This year's DSP^{x} conference (Moscone Convention Center, San Francisco, June 13 to 15) divides sessions into three groups: tutorials, product presentations, and advanced applications sessions.

On Monday, June 13, companies will have the opportunity to introduce new DSP products in a special session focused just on products. In addition, more than 70 exhibitors will be displaying their latest DSP products in the DSP^{x} exposition. For a sampling of DSP-related products at DSP^{x}, turn to pg. 62 for product reviews. Because Moscone Center is in downtown San Francisco, parking may seem somewhat daunting. The map will help you find a place to park.

You might also consider taking Caltrain ((800) 660-4287 in California) to the San Francisco Terminal, which is only a few blocks from the Mocsone Center. EDN

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DSP^{x} '94 CONFERENCE PROGRAM

Monday, June 13		
8:30-10:3	101	Introduction to DSP
	203	Digital Cellular Solutions
10:15-11:45		New Product Introductions
11:45-1:15	102	Start-up and Algorithms
	206	System-Level Graphical Tools
2:15-3:45	205	Multimedia Platforms
	308	New and Emerging Speech Coding Standards
4:00-5:30	309	Audio Engineering Society Roundtable
Tuesday, June 14		
8:30-10:30	204	Video, Graphics, and Image Processing
	306	Speech Recognition/Synthesis
11:00-12:30	202	Mobile Communications
	302	Wireless
1:30-3:00	301	PC-Based Multimedia
	303	Speech Coding
3:30-5:30	103	DSP Case Studies
	201	Signal Analysis Software
Wednesday, June 15		
8:30-10:30	210	High-Level System Design
	304	Digital Telephony
11:00-12:30	104	Symbolic Computation
	208	Data Acquisition, A/D and D/A Converters
1:30-3:30	207	Parallel DSP Architectures
	305	Advanced Topics in Signal/ Spectral Analysis
4:00-5:30	209	Development Tools
	307	Embedded Control Systems

DSP^x '94 Exhibitor List (Partial)

3L Limited
AT&T Microelectronics
Adaptive Solutions Inc
Advanced Computing
Alacron Inc
Analog Devices Inc
Analogical Systems
Ariel Corp
Athena Group
Atlanta Signal Processors
Audio Engineering Society
Bittware Research Systems
Butterfly DSP
CADIS Software Ltd
CSPI
Comdisco Systems, A business unit of Cadence Design Systems Inc
Communication Automation & Control Inc
Computer Design
Domain Technology
DSP Group Inc
DSP Research
DSP Software Engineering
DSPnet
Datacube Inc
EDN Magazine
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Forward Concepts Co
Giga Operations
HNC Inc
Harris Semiconductor
Hyperception
IBM Mwave
IEEE Signal Processing Society
Ixthos
Image & Signal Processing Inc
Integrated Motions
Intelligent Systems International
Loughborough Sound Images Ltd
MW Media
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The Math Works Inc
Mentor Graphics
Mercury Computer Systems
Mizar Inc
Momentum Data Systems
Motorola, SPS
NEC Electronics Inc
National Instruments
Pentek Inc
Rational Software Corp
Scientific Computing & Automation
Signalogic
Signum Systems
Silicon Systems Inc
Sonitech International Inc
Spectron Micro Systems
Spectrum Signal Processing Inc
Star Semiconductor
Tartan Inc
Texas Instruments
Texas Memory Systems
Transtech Parallel Systems
Traquair Data Systems
Vocal Technologies Ltd
White Mountain DSP
Wintriss Corp
Wireless Design & Development
Wolfram Research
Zola Technologies

DSP^x CHIPS

SHARC (μP) attack. The ADSP-21060 SHARC DSP μP combines a 32-bit, 40-MIPS, floating-point ADSP-21020 DSP processor core with a dual-ported, 4-Mbit SRAM; a 10-channel, 40-MHz DMA controller; two 40-Mbps serial ports; and six 240-Mbyte/sec interprocessor link ports. The processor core incorporates an ALU, a multiplier, and a shifter and can perform 120 Mflops (peak) and sustain 80 Mflops. On-chip hooks allow "glueless" multiprocessor configurations. $296 (1000). **Analog Devices Inc**, Norwood, MA. (617) 329-4700. **Circle No. 438**

Wireless DSP μP runs on 2.7V. Designed with AT&T's DSP1600 core, the DSP1611 DSP μP provides as much as 54 MIPS of processing power and can run on supply voltages as low as 2.7V. On-chip memory comprises 12k words of dual-ported RAM and 2k words of ROM. You can download a program on the fly to the DSP's system RAM through its integral JTAG port. Three power-management modes drop the processor's power dissipation in stages down to less than 50 μA (in stop mode). The device is pin-compatible with the company's DSP1618 and DSP1617 μPs and includes on-chip, full-speed emulation hardware. A JTAG-based development system aids single-processor or multiprocessor software development. $85 (1000). **AT&T Microelectronics,** Allentown, PA. (800) 372-2447. **Circle No. 439**

"Pro-sumer" ADC. The AD1877, a 16-bit delta-sigma ADC, features a 92-dB signal-to-noise ratio (typ) and a 90-dB signal-to-(distortion plus noise) ratio (typ). The IC runs on 5V and draws only 100 μW in power-down mode. It has two single-ended analog inputs and a serial digital output. The input section employs autocalibration to correct any dc offsets. Because the ADC employs a delta-sigma modulator to digitize the analog input, the digitized output is inherently monotonic. Digitizing sample rates range from 235 Hz to 97.64 kHz. $10 (1000). **Analog Devices Inc,** Norwood, MA. (617) 329-4700. **Circle No. 440**

DSP μP powers down three ways. Designed for applications where power is at a premium, the 33-MIPS ADSP-2171 DSP μP features three power-down modes that can drop the chip's power requirements to ½ mW. For example, the μP requires only 28 mW and 3.3 MIPS to execute the GSM (European digital cellular) speech-coding algorithm. The ADSP-2171 is part of and is code-compatible with the 16-bit, fixed-point ADSP-21xx family, but it has an enhanced architecture including bit-manipulation instructions and an "Xop-squared" instruction. On-chip memory includes 2k words of 24-bit program/data memory, 2k words of 16-bit data memory, and an optional block of program ROM (8k 24-bit words). $25 (1000). **Analog Devices Inc,** Norwood, MA. (617) 329-4700. **Circle No. 441**

DSP^x SOFTWARE & DEVELOPMENT TOOLS

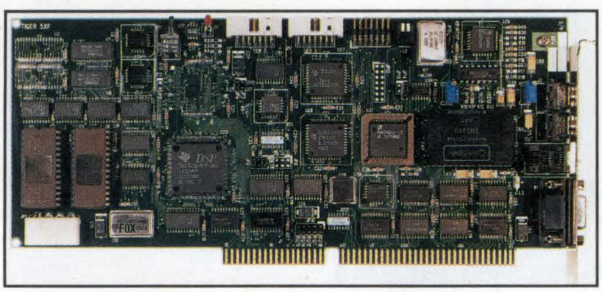
Signal processing and analysis for Unix. Vipre (visual processing environment) is a signal-acquisition and -analysis package for Unix workstations. Standard features include time-, amplitude-, and frequency-domain analysis during both real-time data acquisition and playback of previously recorded data. $7900. **Engineering, Scientific, and Industrial Computing,** Carlisle, MA. (508) 369-8499. **Circle No. 442**

RF library. This library of block functions adds RF circuits including nonlinear amplifiers, switches, couplers, A/D converters, and mixers to the company's Signal Processing WorkSystem. $5000. **Alta Group** (formerly Comdisco Systems), Foster City, CA. (415) 574-5800. **Circle No. 443**

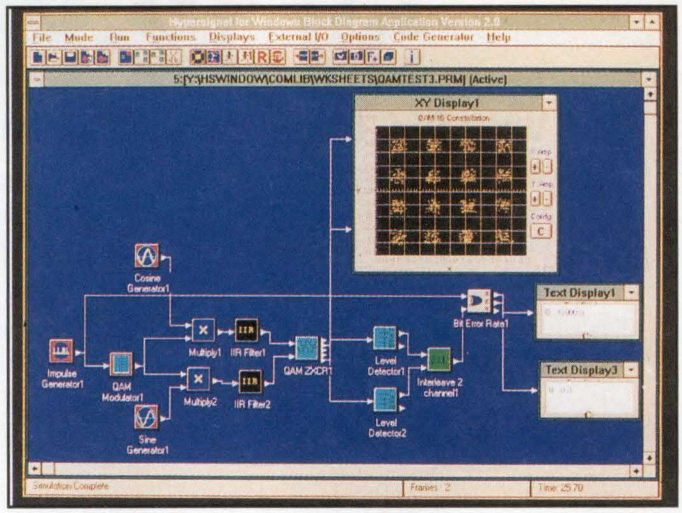
DSPx SOFTWARE & DEVELOPMENT TOOLS

Data acquisition and control for Windows. Labtech Notebook release 8.0 and Labtech Control release 5.0 are new versions of data-acquisition and -control software products that run under Microsoft Windows. Newly supported features include global parameter changes across an unlimited number of I/O channels, data streaming to 1 MHz under Windows DMA, hierarchical icon grouping, drill-down layer navigation, extensive on-line help, multimedia (plays .WAV files) and bit-map image support, and 4-level security. Labtech Notebook, $995; Labtech Control, $1995. **Laboratory Technologies Corp,** Wilmington, MA. (508) 657-5400. **Circle No. 444**

Generate and analyze signals in Windows. Siglab for Windows allows you to perform "what-if" experiments with simulated signals and systems. The software package runs under Microsoft Windows and includes more than 140 mathematical and system operations including Fourier transforms, window generation, phase and group delay, convolutions, arithmetic and complex arithmetic, statistical analysis, and program flow control. $199. **The Athena Group,** Gainesville, FL. (904) 371-2567. **Circle No. 446**



ICEs for TMS320C40 and 'C5x. The Tiger C40 emulator for Windows and the Tiger C5x emulator for DOS and Windows are scan-based emulators for systems based on the TMS320C40 and TMS320C5x DSP μPs, respectively. The target system runs at full execution speed during emulation. The 10-ft emulator cable allows considerable distance between target and host systems. You can debug in C source code, assembly language, or mixed modes. The Tiger C40 emulator supports debugging of multiprocessor systems. You can also get a complete TMS320C5x development system, the Tiger 5XF. Tiger C40 or Tiger C5x emulator, $3995; Tiger 5XF development system, $3995 to $6995. **DSP Research,** Sunnyvale, CA . (408) 773-1042. **Circle No. 448**



Block-diagram simulator for Windows. Hypersignal for Windows is a visually programmed simulation package running under Microsoft Windows. You can create and test various DSP algorithms by arranging and connecting prefabricated and custom-designed signal-processing blocks. The package's block-diagram editor supports hierarchical design; a block on one level can represent several blocks at a lower level in the hierarchical design. An optional C source-code generator emits code for selected DSP μPs. An advanced transmission library adds a comprehensive set of blocks for radio, wireline, and fiber-optic transmission systems. Hypersignal for Windows, $1495 to $7995; Advanced Transmission Library, $1495. **Hyperception,** Dallas, TX. (214) 343-8525. **Circle No. 445**

Turnkey development platform. The MX31 developer's kit is a turnkey package of hardware and software for embedded DSP development. The hardware system consists of an enclosure, power supply, and the company's TMS320C31-based motherboard, which accepts a variety of daughtercards. These daughter cards add memory, analog and digital I/O, and motion control. The software component of the development kit includes a C compiler and the Boss source-code debugger/development environment. $2495. **Integrated Motions Inc,** Berkeley, CA. (510) 527-5810. **Circle No. 447**

Remote Ethernet debugger for TMS320C40. You can remotely debug TMS320C40 programs over the Ethernet from a Sun workstation with the Remote Ethernet Debug System (REDS) for the company's CV line of 'C40-based VME boards. Implementation employs remote procedure calls in a client/server arrangement, allowing coexistence with other Ethernet communications. $8500. **Spectrum Signal Processing Inc,** Burnaby, BC, Canada. (604) 421-5422. **Circle No. 449**

DSPx SOFTWARE & DEVELOPMENT TOOLS

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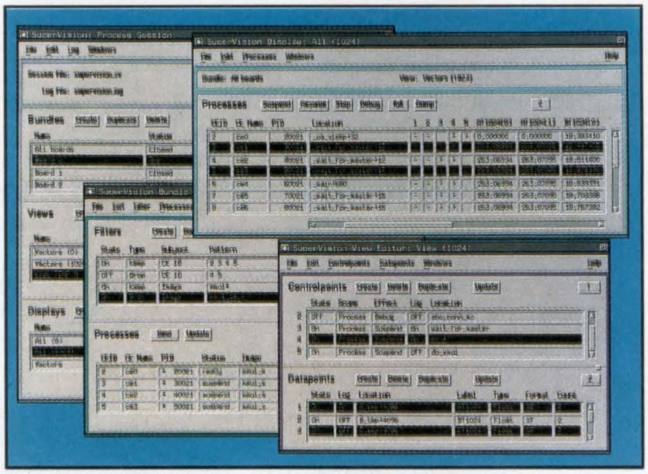
Fixed-point optimizer speeds hardware design. The Fixed-Point Optimizer works with the company's Hardware Design System to accelerate hardware design by automatically determining the optimum fixed-point attributes for a behavioral algorithm or architectural design. The optimizer works for any design including time-varying, multirate, and nonlinear systems. This tool allows you to start designing a system using floating-point blocks. It then automatically replaces floating-point blocks with fixed-point blocks where possible, thus reducing overall system cost while maximizing dynamic range and avoiding arithmetic overflow. $20,000. **Alta Group** (formerly Comdisco Systems), Foster City, CA. (415) 574-5800. **Circle No. 450**

Parallel C for the TMS320C40. This latest version (1.1) of the company's parallel C compiler for TMS320C40 systems adds access to low-level DMA, timer, interrupt, and CPU registers; global file services (any task on any processor has access to host I/O); flood filling of processor networks (topology independent); and a worm utility for exploiting 'C40 networks. $4500. **3L,** Edinburgh, Scotland. 44 31 662 4333. **Circle No. 451**

Fixed-point G.728 encoder/decoder for TMS320C5x. These real-time, fixed-point G.728 encoder/decoder C-callable routines for the TMS320C5x DSP µP are compatible with the company's floating-point G.728 encoder/decoder. The G.728 specification describes a process for compressing 128-kbps PCM speech into a 16-kbps bit stream. The average MIPS requirement for the encoder and decoder are 26.6 and 19.4, respectively, with a peak MIPS requirement below 38. For full-duplex operation, you'll need one 40-MHz 'C5x DSP µP or two slower processors. North American price, $75,000 plus royalties. **DSP Software Engineering,** Bedford, MA. (617) 275-3733. **Circle No. 452**



Debugger for real-time multicomputers. SuperVision is a system-level debugger for the company's Race series of real-time multicomputers. The package's monitoring capabilities give you multiwindowed views of the parallel processes executing in the system. The package runs under the X Window system and OSF/Motif through the company's MC/OS distributed, real-time operating system. $5500. **Mercury Computer Systems,** Chelmsford, MA. (508) 256-1300. **Circle No. 453**

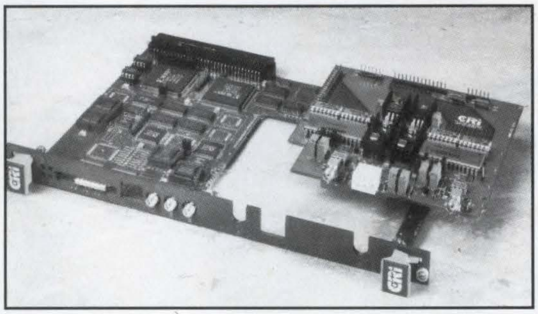
Development kit for Windows multimedia. Develop multimedia applications for 24-bit DSP56000 DSP µPs and Microsoft Windows including voice and data communications and high-quality audio with the PC Media system. The kit supports SPOX-based Windows API calls. SPOX is the DSP kernel from Spectron Microsystems (Goleta, CA). Initially, the kit's software library includes routines for audio synthesis, fax and data modems, a full-duplex speakerphone, MPEG audio, general MIDI, speech compression, text-to-speech conversion, and a telephone answering machine. The kit also includes a developer's board, reference design schematics, demo software, an assembler/linker, and a C compiler. $7500. **Motorola Inc,** Austin, TX. (800) 441-2447. **Circle No. 454**

Signal-processing routines for TMS-320C3x/C40. DSPLib is a library of signal-processing routines for the Texas Instruments TMS320C3x and 'C40 DSP µPs. You provide the glue in the form of C source code to link these callable routines into a DSP program. Functions in the library include FFTs; infinite- and finite-impulse-response filters; convolution; correlation; windowing; Gaussian white-noise generation; and matrix multiplication. The library can implement a 100-coefficient finite-impulse-response filter in 548 µsec on a 40-MHz 'C40 DSP µP. $750. **Spectrum Signal Processing Inc,** Burnaby, BC, Canada. (604) 421-5422. **Circle No. 455**

DSP^{X} SOFTWARE & DEVELOPMENT TOOLS

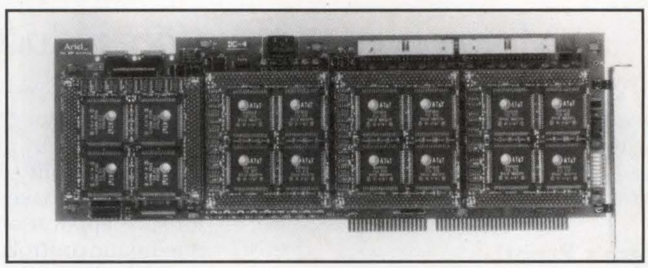
Design DSP data paths directly. DSP Blocks adds the ability to design custom DSP ASIC data paths for the company's DSP Station design environment. The package employs 22 parameterizable generators to create the data path using a graphic design approach. It also generates a behavioral data-flow language description, which allows fast fixed-point simulation of the design and structural VHDL code for VHDL simulation and logic synthesis. $15,000. **Mentor Graphics,** Wilsonville, OR. (503) 685-7000. **Circle No. 456**

DSP^{X} BOARDS



A/D card samples 14 bits at 40 MHz. The Nimble A/D board for VME and VSB bus systems offers one or two A/D channels with 10- to 14-bit resolution and sample maximum rates of 5 to 40 MHz. The board actually consists of a VME motherboard and five daughter-cards of varying ability. The mother board has image-processing capabilities including frame synchronization and pixel selection. The A/D cards offer single-ended or low-noise differential front ends. A 12-bit, 10M-sample/sec system costs $5700. **Catalina Research Inc,** Colorado Springs, CO. (719) 637-0880. **Circle No. 457**

Highly modular, parallel-processing DSP system. Mix four ADSP2101 DSP μPs, 4 Mbytes of RAM, and two FPGAs, place them on a 2.4×3.65-in. circuit board, and you have a powerful, reconfigurable DSP module capable of performing video-rate processing. Three carrier boards of varying speeds for the PC VASA bus each have four connectors. Each connector accommodates four stacked processing modules for a maximum of 16 modules per carrier and a total of 48 DSP μPs. DSPMOD processing modules, $500 to $2000; carrier cards and development software, $2000 to $3500. **Giga Operations Corp,** Berkeley, CA. (510) 528-8438. **Circle No. 458**



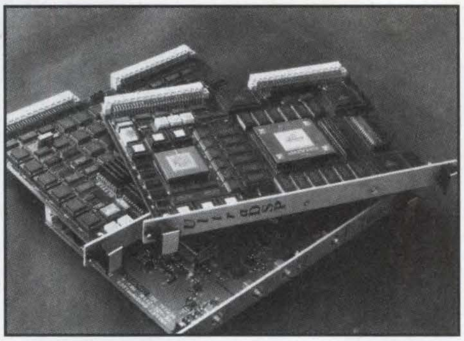
Floating-point DSP for PC/104 bus. Based on AT&T's 50-MHz DSP32C DSP μP, the PC5-DO board brings floating-point DSP to the PC/104 bus. The board also incorporates 512 kbytes of SRAM. In addition to the 8- or 16-bit PC/104 interface, the board has a 25-Mbps serial port for high-speed data transfers to and from the processor. A separate 32-bit, 100-Mbyte/sec mezzanine connector provides an expansion port for the DSP32C's address/data bus. $1395. **Communication Automation & Control Inc,** Allentown, PA. (215) 776-6669. **Circle No. 459**

ISA card mounts 16 DSP3210 DSP μPs. The TeraDON PC ISA bus card has four sites for 4-processor DON-4D daughter cards for a total of 16 processors. Each DON-4D incorporates four AT&T DSP3210 DSP μPs and as much as 256 Mbytes of DRAM. Software support for this system includes AT&T's VCOS real-time multitasking operating system and a set of multimedia and telephony software modules including fax, modem, text-to-speech conversion, speech recognition, MPEG/P*64 audio compression, and still image compression. A 4-processor version, $3995; 16-processor version, $9995. **Ariel Corp,** Highland Park, NJ. (908) 249-2900. **Circle No. 460**

Digital I/O board brings DSP to control applications. This 32-channel digital I/O board adapts DSP μPs for control applications. The DSP communicates with the board via the company's DSP-Link interface. $1045. **Spectrum Signal Processing Inc,** Burnaby, BC, Canada. (604) 421-1764. **Circle No. 461**

DSP^{X} BOARDS

DSP^{X} BOARDS



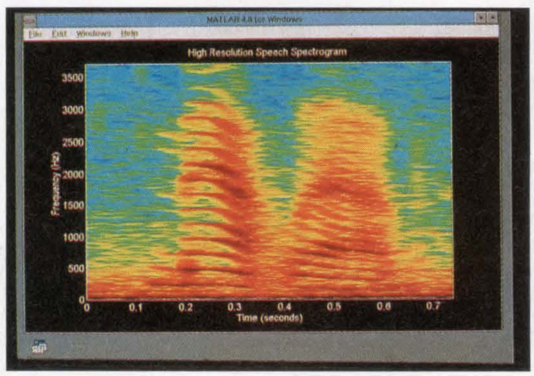
Ultra board series exploits 400-MIPS LH9124 DSP. The Ultra board family gives you three board-level building blocks to create systems based on the Sharp LH9124, a 24-bit, 400-MIPS DSP µP. This processor can perform a windowed, 1024-point FFT in 93 µsec, about the same speed as 20 TMS320C40s or 11 i860 processors. The DSP mounts on the UltraDSP, a VME processor board. An onboard DSP32C DSP µP acts as a supervisory controller. The UltraADC is a 10-bit, 40-MHz A/D-converter board that communicates with the UltraDSP through dedicated pins on the VMEbus' P2 connector. This board also incorporates a 12-bit D/A converter for waveform generation. The third member of the Ultra family, the UltraBUF, is a 24-bit×1M-word memory card that supports data-acquisition and waveform-generation rates to 40 Mbytes/sec. UltraDSP, $21,000; UltraADC, $5500; UltraBUF, $6500. **Valley Technologies Inc,** Tamaqua, PA. (717) 668-3737.
Circle No. 463

200-Mflops VME board carries five TMS320C31s. The AP65 DSP signal processor achieves 200 Mflops by ganging five 40-MHz TMS320C31 DSP µPs. The board also includes 16 Mbytes of global memory. The processors are arranged in a master/slave configuration, but all processors act as computational peers. The master processor controls the board's I/O ports, which include an 80-Mbyte/sec FIFO port, a 960-kbps serial port, an RS-232C port, and a 20-Mbyte/sec SCSI-2 port. $13,200. **Analogic Corp,** Peabody, MA. (508) 977-3000. **Circle No. 465**

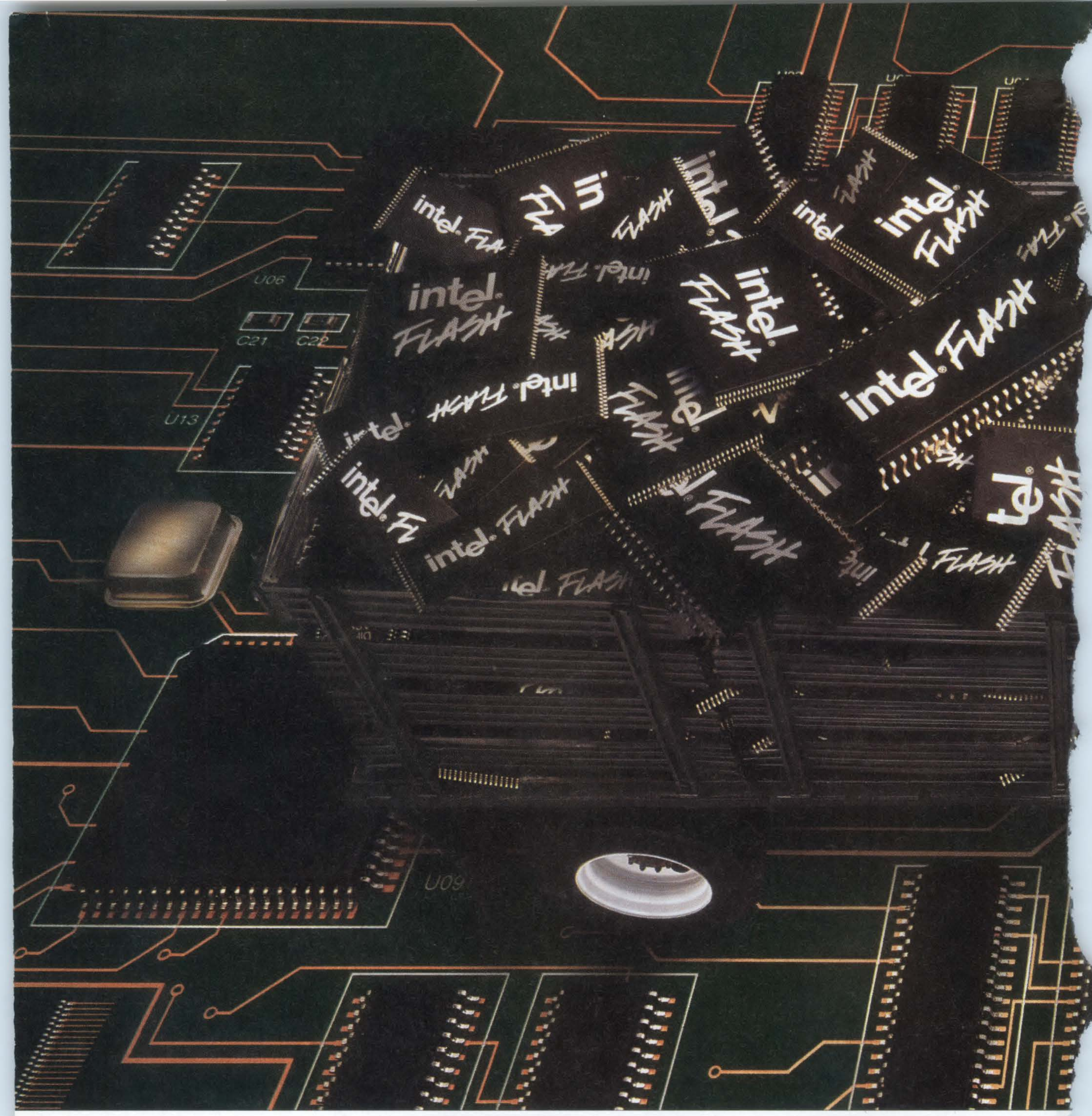
Put two or four 'C40s on VME. The Spirit-40 VME and Quad-40 VME place two or four 40- or 50-MHz TMS320C40 DSP µPs on a VME board, respectively. Both boards provide local memory for each processor and global memory for interprocessor communications. Both boards also accommodate as much as 4 Mbytes of local SRAM per processor and 4 Mbytes of global SRAM. Each board has six 20-Mbyte/sec ASM-C processor communications ports on the front panel for board-to-board communications and two 50-Mbyte/sec ASM-M ports for memory expansion. Spirit-40 VME, $8995; Quad-40 VME, $9995. **Sonitech International Inc,** Wellesley, MA. (617) 235-6824. **Circle No. 466**

VME multiprocessor card employs QuickRing. With eight Intel i860 µPs arranged in four processing pairs, the Supercard-4SLX delivers 640 MFLOPS. Multiple boards communicate via 182-Mbyte/sec QuickRing interfaces and reach an aggregate transfer rate of 1.28 Gbytes/sec when fully configured as a 16-board system. Each processing element can have as much as 16 Mbytes of local DRAM. A 5-port crossbar switch links the four processing elements on the board with the VMEbus. $29,000. **CSPI,** Billerica, MA. (508) 663-7598. **Circle No. 462**

Image processing for 'C40 systems. You can convert existing TMS320C40 DSP systems into image processing systems with the IPI-40 VME board. The board can capture frames from as many as four multiplexed NTSC or PAL video sources. It performs real-time 8×8, 2-dimensional convolution and RGB pseudocolor processing. The IPI-40 communicates with 'C40 systems via one of the 'C40's 20-Mbyte/sec comm ports. The HETVIO, a complete image-processing system that combines the features of the IPI-40 with a TMS320C40, a 1-Mbyte VRAM frame store, and 4 Mbytes of DRAM, is also available for ISA, VME, and SBus systems. IPI, $3850 ($5050 with convolution); HETVIO, $6750. **Traquair Data Systems,** Ithaca, NY. (607) 272-4417. **Circle No. 464**



Software for filter design and spectral analysis. Signal Processing Toolbox 3.0 software for signal analysis and DSP algorithm development includes an expanded, spectral-analysis suite and advanced design techniques for FIR and IIR filters. New features in the upgrade include parametric modeling routines for time-series analysis; graphical objects with automatic plotting; and specialized design and analysis functions for communications, multirate, speech-processing, and real-time embedded applications. **The MathWorks Inc,** Natick, MA. (508) 653-1415. **Circle No. 467**



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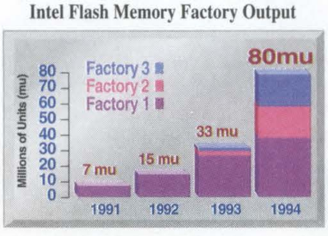
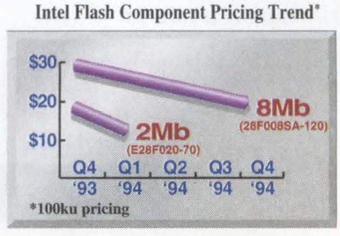
We're also growing the market by driving down flash prices, making Intel Flash

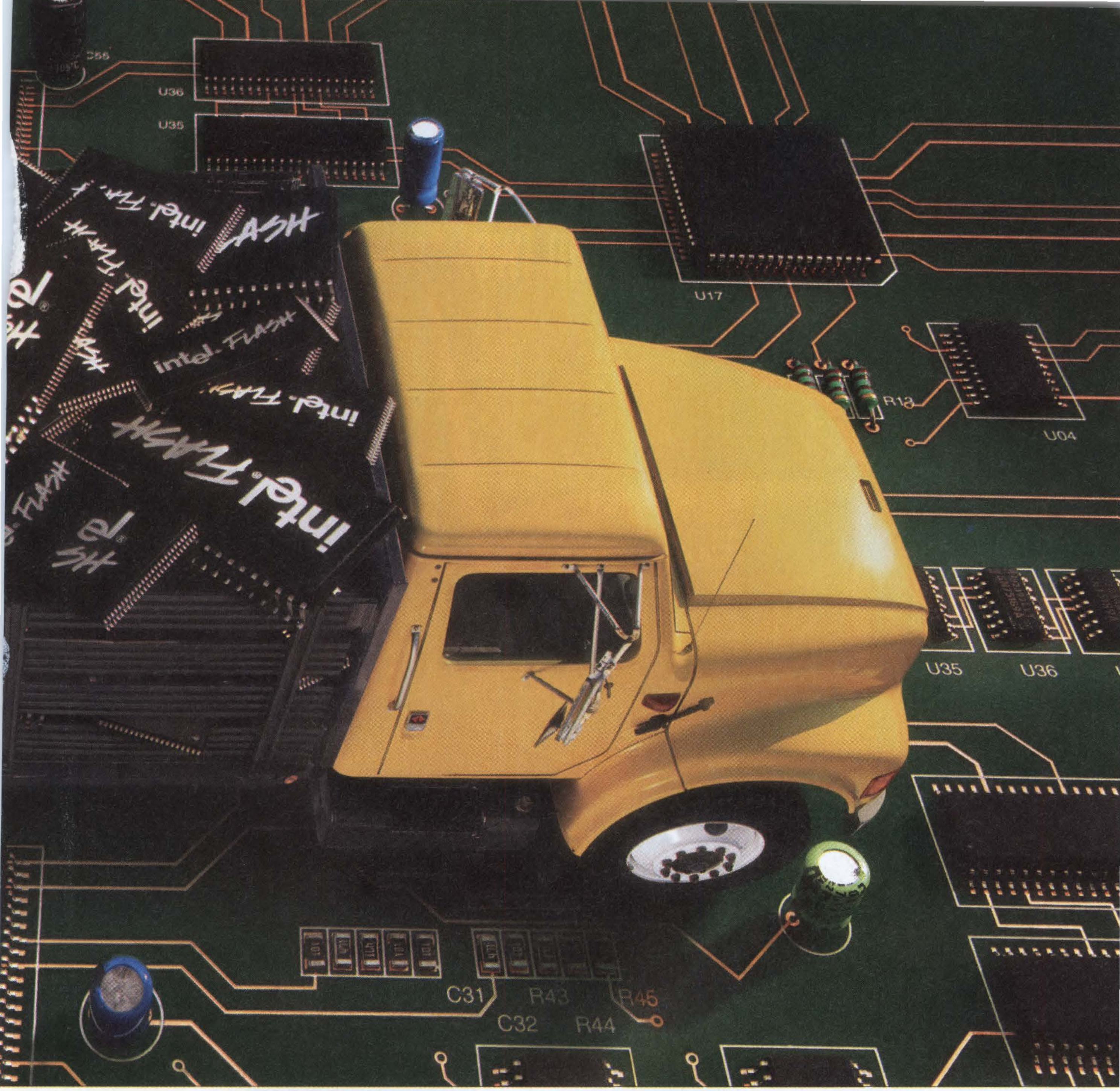
Intel Flash Memory Factory Output



Intel Flash Component Pricing Trend*



 [†]Based on 9/93 Dataquest forecast of total flash units to ship in 1994.



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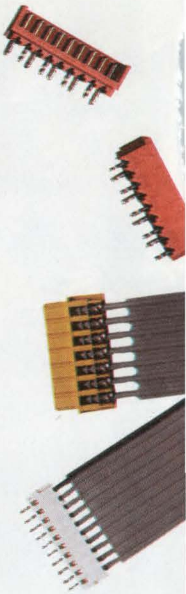
CIRCLE NO. 121

As a Rule, Four Points of Contact Are Better Than Two.



2,5mm

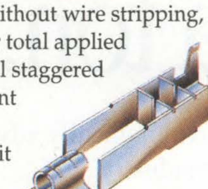
SPOX® IDT

System

Introducing the 2,5mm SPOX® IDT System, With Four Points of Contact, for Unmatched Reliability.

With 4 points of contact instead of the usual two, Molex's new 2,5mm SPOX (spring box) IDT terminals provide unmatched reliability in wire-to-board terminations.

The SPOX IDT system features a crimped metal strain relief for secure connections without secondary clamps. Insulation Displacement Technology (IDT) allows mass termination without wire stripping, lowering your total applied costs. Optional staggered PC tails prevent shorting and facilitate circuit tracing.



Environmentally tested (72 thermal cycles without failure), the UL-Recognized, CSA-Approved Molex 2,5mm system gives you superior reliability where miniaturization has restricted your design space for connectors.

Intermateable with the crimp SPOX system, the Molex design permits unique combinations to accommodate board space and height restrictions. Molex's SPOX also comes with four optional colors to help in production and field servicing.

The new 2,5mm SPOX lowers your applied costs, through Molex's semi-automated application tooling for high volume assembly. For maximum cost-effectiveness, a direct board-in version allows you to build an off-line harness that solders directly to the board, eliminating the need for a header.

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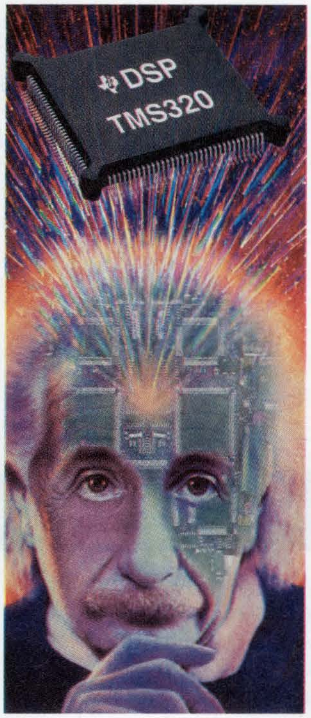
CIRCLE NO. 123

EDN's 1994 DSP-CHIP DIRECTORY

Compiled and edited by James P Leonard, Senior Associate Editor

The 1994 EDN DSP-Chip Directory is a keeper: Not only have we revised and updated last year's chip specs, but we've also added new entries, including Zoran's 16-bit fixed-point ZR38000, the Texas Instruments' 32-bit MVP, and Analog Devices' SHARC, a 32-bit floating-point DSP.



The 16-bit fixed-point devices continue to dominate low-cost applications. As new variations of each DSP μP hit the market, each family fills a greater variety of applications. The largest markets for these 16-bit speedsters include telecommunications, digital cellular telephones, and disk drives.

Floating-point DSPs are being designed in by the cluster. Often you'll see products that, instead of having just a couple of DSPs within, have many. For a number of years, designers generally thought floating-point DSPs would be used for prototyping fixed-point DSP-based products. Even though floating-point devices are easier to use, most developers aren't opting to use them as a crutch. As a result, floating-point devices end up in applications where the three most important design criteria are performance, performance, and performance.

Designing with DSPs continues to get easier. You can now buy world-class software-development tools. And in many cases, you don't even need to write the code—you can just buy the algorithms premade. For example, TI has created the TMS320 Software Cooperative, which offers a collection of algorithm data sheets. You select the algorithm you want by paging through the packet.

Getting a DSP-based board to work with Microsoft's Windows is also getting easier. In conjunction with DSP real-time operating-system (RTOS) vendors, Microsoft is busy creating a standard method for applications to call for DSP functions. Any DSP-based board that works within the guidelines of the standard can be plugged into the PC and used with any application.

Another year of above-average growth for DSPs hasn't been affected by a marketing myth that superfast CISC or RISC μPs will begin to replace DSPs. In many cases, the replacement trend is working the other way. The supremely fast DSP is using surplus cycles to replace slower microcontrollers.

As you flip through the following pages, you'll find a comprehensive listing of the major DSP chips, ranging from stripped-down, 16-bit, fixed-point processors to full-blown, 32-bit floating-point processors. Each chip family has its own page full of architectural information and a quick run-down of variations, peripherals, and price/packaging information. If your time's limited, check out the handy reference tables in the upper-right corner of each page—we've noted important feature and performance specs in an easy-to-read format. Keep a copy of the directory as a reference for your design work throughout the coming year. EDN

—Additional reporting by Contributing Editors Ray Weiss and David Shear

Article Interest Quotient (Circle One)
High 583 Medium 584 Low 585

Text continued on pg 76

DSP-Chip Directory Index

Key to abbreviations in schematics

AB—combined program-and-data address bus
ACC—accumulator
ADC/DAC—analog-to-digital and digital-to-analog converters
ADDR GEN—address generator
ALU—arithmetic logic unit
BIT MANIP—bit manipulation
BS—barrel shifter
CDB—control data bus
CM—cache memory
CPUB—CPU bus
DAB—data address bus
DB—combined program-and-data data bus
DDB—data data bus
DM—memory for data only
DMAAB—DMA address bus
DMADB—DMA data bus
DMAC—DMA controller
FP—floating point
FX—fixed point
GDB—global data bus
HOST INTER—host interface
IDB—instruction data bus
INT—external interrupt
MAC—multiply/accumulate
MULT—multiplier
PAB—program address bus
PDB—program data bus
P/DM—program and data memory
PIO—parallel I/O
PM—memory for program only
PPCP—parallel processor communications port
PRAB—peripheral address bus
PRDB—peripheral data bus
REG—register
REGB—register bus
SIO—serial I/O
TIM—timer
XAB—external address bus
XDB—external data bus
XDAB—external data address bus
XDDB—external data data bus
XIOAB—external I/O address bus
XIODB—external I/O data bus
XPAB—external program address bus
XPDB—external program data bus

Analog Devices ADSP-2100 Family

16-bit fixed-point DSP

☐ **OVERVIEW** The 2100 family combines 16-bit math processing with zero-overhead looping. The first chip, the DSP-2100, has no on-chip program or data memory. Instead, it has two external buses—one each for program and data—and an on-chip cache of 16 instruction words. Later chips, such as the ADSP-2171, add on-chip memory. The ADSP-2171 has 8k-word program ROM, 2k-word program RAM, and 2k-word data memory. Executing from this on-chip memory, the CPU can deliver single-cycle execution. It has two address generators (X, Y) and two buses: program and data. While executing out of on-chip cache, the two buses feed the X and Y data values for each MAC cycle. The program bus is free for MAC use when the CPU executes out of program ROM, which has a direct connection to the program sequencer and instruction decoder.

The later chips with on-chip memory have a single external, 24-bit bus for a simpler configuration and a larger address space. AD engineers also added peripherals to simplify processing and reduce chip counts. The peripherals include a 16-bit autoreloading timer, two serial ports, 8-/16-bit host/parallel port, and DMA controller, as well as a 16-bit sigma-delta ADC and a 16-bit DAC for audio-band applications.

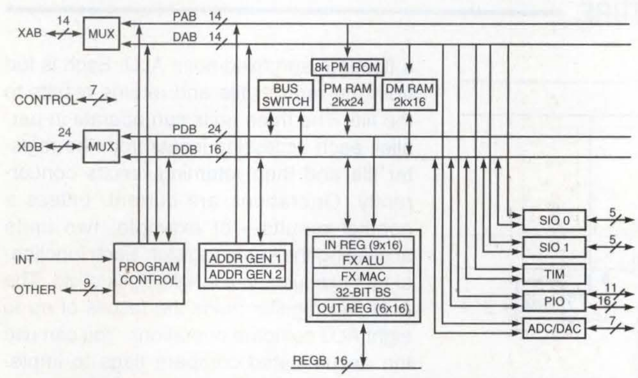
ADSP-2171

- 24-bit instruction word, 14-bit data word
- 2k×14-bit data RAM
- 4k×24-bit program RAM
- 8k×24-bit program ROM
- 8-/16-bit parallel/host interface
- 2 serial I/O ports
- 1 16-bit interval timer
- 3 external interrupts
- 8k PM ROM, 2k PM RAM, 2k DM RAM
- 3 power-down modes
- 33-MHz operation (16.67-MHz external clock)
- 30-nsec ADD, NOP, MPY, MAC
- 1-cycle external memory R/W
- Multiple wait states
- Register shadowing for fast context switch
- Zero-overhead instruction loops
- 3-cycle interrupt latency
- Serial I/O to 13-MHz rate
- Supports up to 8 simultaneous circular buffers

☐ **VENDOR CONTACTS**

Analog Devices Inc, Norwood, MA, (617) 329-4700. **Circle No. 484**
Application Hot Line: (617) 461-3672.
DSP BBS: (617) 461-4258 (N,8,1).

ARCHITECTURE



The ADSP-2100 family's CPU handles general processing needs and delivers single-cycle instruction execution when executing tight DSP algorithms from on-chip memory. Analog Devices designers opted for a wide 24-bit instruction word to minimize instruction decoding and speed execution, while utilizing complex instruction formats. Data words are 16 bits. The difference in code and data word sizes requires a Harvard architecture with two separate memory spaces. But Harvard architectures with separate memory spaces are typical for most DSPs; they enable instruction fetches to occur in parallel with single-cycle MAC operations. In the ADSP-2100's case, the different memory sizes can complicate external-memory design.

For DSP processing, the ADSP-2100 architecture treats both these spaces—program and data—as two data spaces: the X and Y memories supply variables and constants for a series expansion. Thus, program memory can be used as a data memory to hold constants for MAC processing. Code can execute multiple operations per clock cycle; the MAC, ALU, and barrel shifter are separate units and can execute in parallel.

When running at full speed, the DSP can execute an instruction per cycle out of on-chip memory. When doing a MAC operation, the X and Y data are accessed from the off-chip memory (ADSP-2100) or from on-chip program ROM and data RAM. A DO UNTIL command sets up a sequence of instructions for repeat operations. The hardware has built-in automatic loop control and addressing for MAC processing. The ADSP2100 delivers single-cycle MAC execution, executing from on-chip memory or from an on-chip cache in DSPs without on-chip memory.

The ADSP-2100 instruction set is surprisingly sophisticated for a stripped-down DSP processor. Most instructions, for example, are conditional: The hardware checks a specified condition first and then executes the core instruction if the condition is true. This tactic compacts code by eliminating the need for separate tests (branches) before doing specific work.

Address generators—Two address generators that access X and Y memory data. Zero-overhead looping: each generator supports up to four loops with three registers each, which define the end, length, and access address. Each generator handles modulo addressing (circular). One generator, DG1, provides bit-reversed addressing (for data only).

☐ **VARIATIONS**

ADSP-2100/A—A stripped-down version with no on-chip memory or peripherals. Accesses main memory through 14-bit addressing and 24-bit data/program buses. Has hardware wait states.

ADSP-2101/02—2k×24-bit programmable RAM/ROM; 1024×16-bit data RAM, timer, two serial I/Os.

ADSP-2103—3.3V part; has 2k×24-bit programmable RAM, 1024×16-bit data RAM, timer, two serial I/Os.

ADSP-2161/2—8k×24-bit programmable ROM, 0.5k×16-bit RAM, timer, two serial I/Os. 5 and 3V parts; 16.7- and 10-MHz clocks.

ADSP-2163/4—4k×24-bit programmable ROM, 0.5k×16-bit RAM, timer, two serial ports, 10 and 16.7-MHz, 3 and 5V parts.

ADSP-2165/6—12k×24-bit programmable ROM, 1k×24-bit programmable RAM, 4k×16-bit data RAM, timer, two serial I/Os. 10/13/16.67/20-MHz clocks.

ADSP-2171—8k×24-bit programmable ROM, 2k×16-bit programmable RAM, 2-kbyte data RAM, two serial I/O ports, 33 MIPS from ½ clock.

ADSP-2111—8k×24-bit programmable ROM, 2k×24-bit programmable RAM, 2-kbyte data RAM, two serial I/O ports, 20-MHz clock, host port.

ADSP-21mps51—2k×24-bit programmable ROM/RAM, 2k×24-bit programmable ROM, 1k×16-bit data RAM. Power-down modes, 16-bit timer, two serial I/Os, 13-MHz clock; 144-pin PGA, 100-pin PQFP.

Part No.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
ADSP-2105	13.8	Run	70	68-pin PLCC	$9.90
ADSP-2101	20	Run Idle	70 14.4	80-pin PQFP 68-pin PLCC	$31
ADSP-2103	10	Run Idle	13 4	68-pin PLCC	$31
ADSP-21msp5X	13	Run Idle	54 13.4	100-pin PQFP	$45
ADSP-2105	13.8	Run Idle	64 14	68-lead PLCC	$9.90
ADSP-2171	33	Run	N/S	128-lead TQFP/PQFP	$62

SUPPORT

☐ **HARDWARE** Evaluation boards are available for most ADSP processors. ICEs are available for hardware target debugging.

☐ **SOFTWARE** Analog Devices supplies an ANSI C compiler and an assembler, linker, and interactive simulator.

Analog Devices ADSP-21020 — 32-bit floating-point DSP

☐ **OVERVIEW** Introduced in 1990, the ADSP-21020 is the first member of Analog Devices' high-performance, floating-point DSP family. A descendent of the earlier ADSP-2100 processors, the ADSP-21020 has the processing throughput of 16-bit fixed-point DSPs while moving up to 32-bit floating-point processing. The ADSP-21020 meets IEEE-754 floating-point standards and, as with earlier AD chips, takes advantage of a large instruction word to encode multiple operations per instruction and speed hardware decoding.

Designed for high-speed DSP, CPU execution is optimized for executing instructions from an on-chip instruction cache. The chip features zero-overhead looping and automatic addressing for X and Y memories. It features a Harvard architecture with separate buses for code and data. The buses do not multiplex address information with data or code.

The ADSP-21020 and ADSP-2100 families use program memory as one of the data memories needed for series evaluation. The program bus and memory provide the X data-memory values, which combine with the Y data-memory values for MAC and ALU operations. Although they target high-throughput math processing, AD's DSP processors also have surprisingly sophisticated CPU features. For example, most instructions have conditional execution: They use a preliminary condition test and, if true, then execute the main instruction.

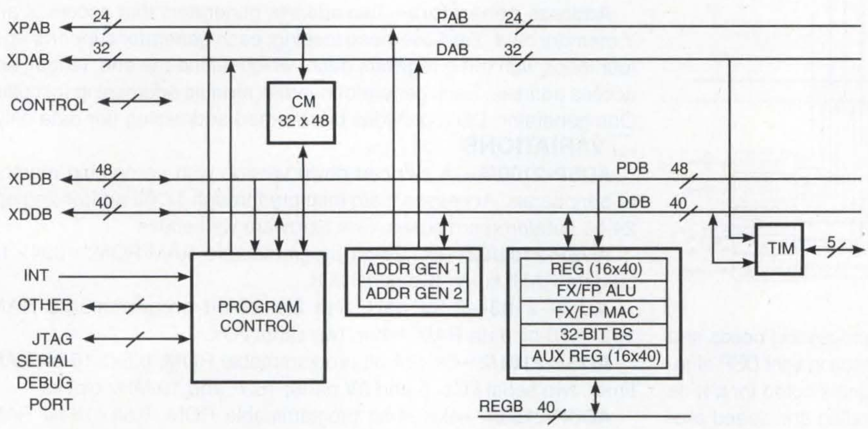
ADSP-21020

- 48-bit instruction, 32/40-bit data words
- 80-bit MAC accumulator
- 3-stage pipeline, 63 instructions
- 32×48-bit instruction cache
- 10-port, 32×40-bit register file (16 registers/set, 2 sets)
- 6-level loop stack
- 24-bit program, 32-bit data address spaces, memory buses
- Modulo, bit-reversed address
- 5 external interrupts
- 33-MHz clock
- 1 instruction/cycle (pipelined)
- 1-cycle MPY (32-bit floating or fixed point)
- 6-cycle DIV (32-bit FP)
- 2-cycle branch delay
- Zero-overhead loops
- 4-cycle max interrupt latency
- On-chip emulation via JTAG port

☐ **VENDOR CONTACTS**

Analog Devices Inc, Norwood, MA, (617) 329-4700. **Circle No. 485**
Application Hot Line: (617) 461-3672.
DSP BBS: (617) 461-4258 (N,8,1).

ARCHITECTURE



The ADSP-21020 delivers single-cycle, pipelined 80-bit MAC operations. It has a hybrid DSP organization. Like the earlier ADSP-2100 16-bit DSPs, the 21020 has no on-chip program or data memory. Instead, it has a 32-word cache memory to hold inner-loop instructions. The chip also has two external buses: one for instructions (48 bits) and one for data (32 bits). Like the 2100, the 32-bit 21020 achieves single-cycle MAC execution by executing the inner-loop instructions from its on-chip cache and bringing in the coefficients and data from external memory.

Unlike the early DSP designs, the ADSP-21020 is not a minimal-register, accumulator-based design. Operations center around a 32×40-bit, multiported register file that holds multiple accumulators and registers. For fast context switching, two 16-register segments shadow the file. The register file serves as the link between the two main buses and the three computational units. The buses pump data into the register file, which unloads to supply input data to the computational units. Ten ports link the computational units and the data and program buses to the register file.

The ADSP-21020's three computational units comprise a floating-point multiplier and fixed-point accumulator, a 32-bit barrel shifter, and a floating- and fixed-point ALU. Each is fed from the register file and returns results to the file. The three units can operate in parallel, each accessing inputs from the register file and then returning results concurrently. Operations are current, unless a conflict results—for example, two units accessing the same register. Each functional unit executes in a single clock cycle. The ALU flag register holds the results of up to eight ALU compare operations. You can use the accumulated compare flags to implement 2D and 3D graphical clipping operations.

Hardware automatically handles address generation for the X and Y data needed for each MAC cycle. The hardware has two address generators to access the X, Y memory data. Each address generator supports up to four loops with three registers each, which define the end, length, and access address. Each generator handles modulo addressing (circular). One generator, DAG1, provides bit-reversed addressing (data only) for FFT calculations.

Addressing modes—Direct and indirect addressing; must use indirect for off-chip memory access.

Fast context switching—Shadow registers for major registers enable fast context switching for interrupts. The PC stack is 20 levels deep. The program sequencer's count and loop stacks are six levels deep and support six levels of interrupt nesting.

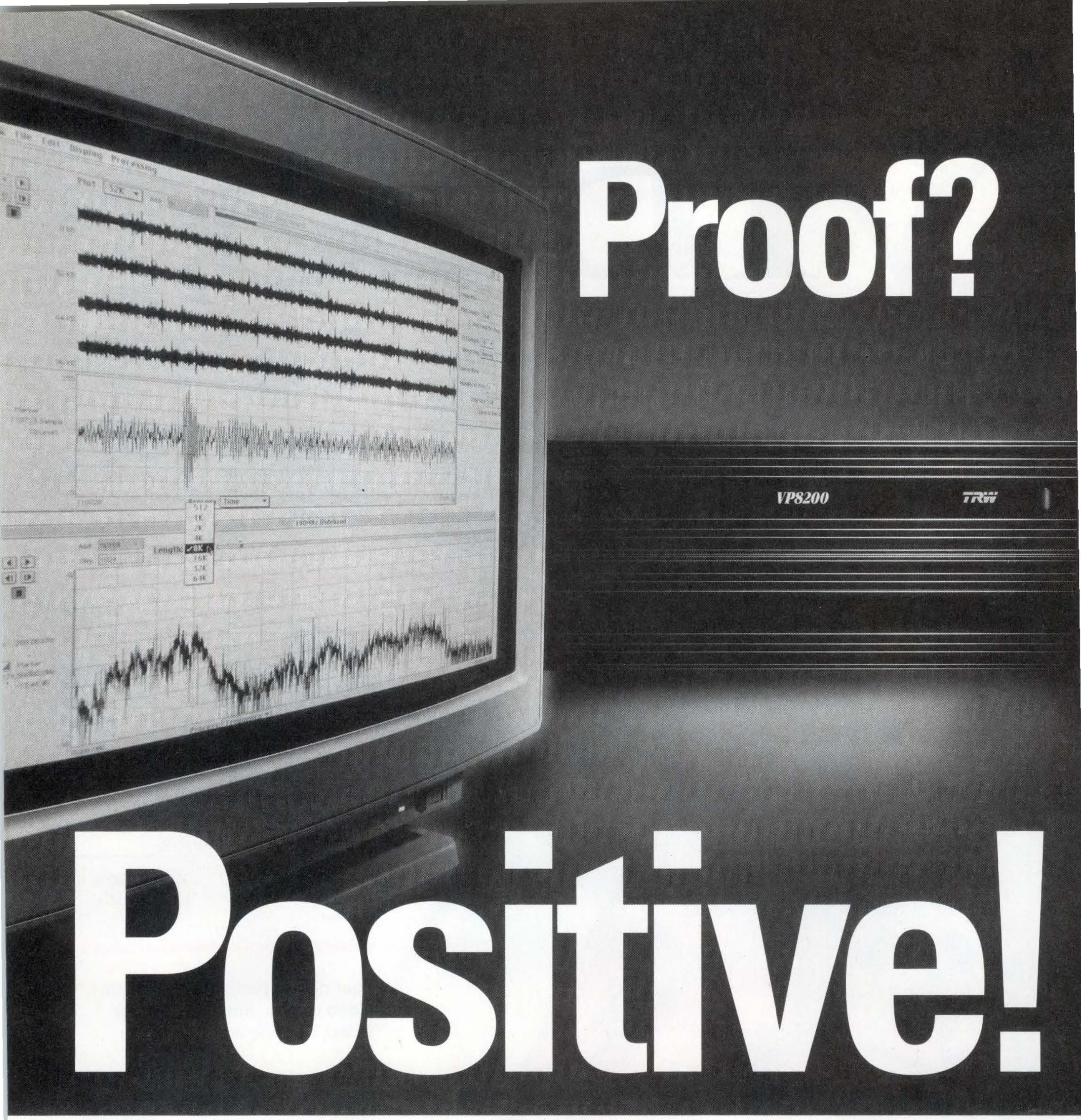
Numeric representations—IEEE-754 32-bit single-precision floating point (23-bit data, 8-bit exponent, and sign bit) and a 40-bit extended IEEE format for additional accuracy (32-bit data, 8-bit exponent, and sign bit). Can also use 32-bit fixed-point formats, fractional, and integer (2's-complement or unsigned).

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
ADSP-21020	33	Run Idle	500 150	223-pin PGA	$159

SUPPORT

☐ **HARDWARE** Analog Devices sells a full-speed ICE and an evaluation board. Third-party tools are also available; contact the company for references.

☐ **SOFTWARE** Analog Devices provides a tool set that includes an ANSI C compiler, C compiler with numerical C extensions for math and floating-point applications, source-level debugger, assembler/linker, simulator, application libraries, and PROM splitter. Third-party tools include the Spox real-time OS, filter-design packages, and a graphical application-development package.



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CIRCLE NO. 84

Analog Devices SHARC (ADSP-2106x)

32-bit floating-point DSP

☐ **OVERVIEW** Unlike other top-end DSP chips, the ADSP-2106x's CPU actually executes using only on-chip memory for a range of application code—it has 512-kbyte on-chip SRAM. Built on the ADSP-21020 32-bit DSP CPU, the ADSP-2106x integrates an I/O controller with the CPU to offload I/O. This DSP chip has six communication links, which enable designers to create DSP multiprocessor meshes; two high-speed serial ports and a host/parallel port that provides a direct interface to off-chip memory, peripherals, and a host processor; and bus arbitration for up to six ADSP-2106x chips in a multiprocessor cluster.

The core DSP CPU, the ADSP-21020 CPU, has a 48-bit instruction word and a 32-bit data word, although it handles double precision, 64-bit floating-point arithmetic. The wide instruction word minimizes instruction-decode overhead and speeds execution. Similar to Analog Devices' earlier 16-bit DSP processors, the 32-bit DSP core has a small, on-chip cache to hold the last x instructions for fast, inner-loop execution.

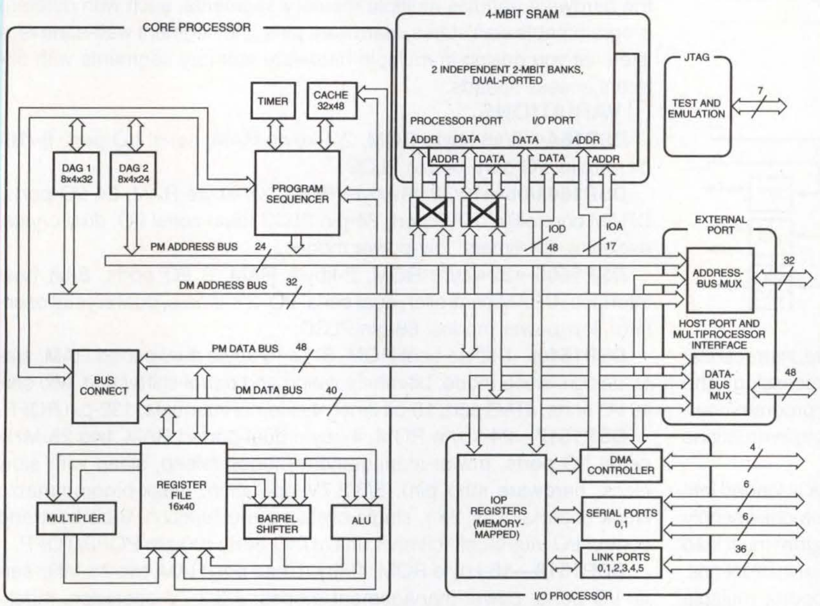
ADSP-2106x

- 48-bit instruction word
- 32/40-bit IEEE floating-point words
- 512-kbyte on-chip, dual-access memory
- I/O controller
- Host/parallel port
- Glueless, scalable, multiprocessing support
- 6 comm ports, 2 serial ports
- On-chip-emulation mode, JTAG support
- 33-, 40-MHz clock (25-nsec cycle)
- 120-Mflops peak performance
- Parallel ALU and MAC, 1-cycle execution
- 240-Mbyte/sec max comm port rate
- Max 40-Mbps serial I/O
- 3-cycle max interrupt latency
- 1k complex FFT in 0.46 msec
- 53M Whetstones/sec; 83k Drystones/sec

☐ **VENDOR CONTACTS**

Analog Devices Inc, Norwood, MA, (617) 329-4700; (800) 262-5643.
Applications Assistance Line, (617) 461-3672.
Computer Bulletin Board, (617) 461-4258.. **Circle No. 486**

ARCHITECTURE



SHARC is an advanced replay of the earlier ADSP-21020 32-bit DSP chip, but it moves 32-bit DSP processing to a new level of capability. SHARC fields a large 512-kbyte on-chip memory organized into two banks of dual-ported RAM. This on-chip RAM holds large chunks of critical code and delivers sustained single-cycle memory accesses. This large memory is fed, in turn, by an independent I/O controller that offloads reads and writes between off- and on-chip memory; the I/O controller executes in parallel with the chip's DSP core CPU, although delays are possible when they contend for the same data. The CPU, I/O controller, and peripherals interconnect through a multibus-crossbar-interconnection unit that allows flexible, nonintrusive transfers between these units. To reduce bottlenecks, the crossbar permits data and instruction fetches from external or internal memory, cache, and I/O from off- or on-chip peripherals all in a single cycle.

Following in the footsteps of the pioneering SGS-Thomson Transputer and TI's C40, the SHARC provides special communication links or ports. Fed through the I/O controller, these ports enable designers to create meshes of DSP processors (each processor in the mesh is defined by point-to-point connections between DSP ports). The on-chip I/O controller sets up, runs, and responds to these ports. Transfers pass through the I/O ports to and from internal memory. The I/O controller separates these transfers from mainstream DSP processing.

SHARC builds on the ADSP-21020 DSP CPU. The instruction set is upwardly compatible with the 21020s. The ADSP-2106x runs up to 40 MHz and can execute parallel floating-point ALU and multiplication computations in one 25-nsec cycle. The CPU has three arithmetic engines: an ALU, a multiplier, and a barrel shifter. Their operations center around a 10-port register file that transfers or receives operands from the computational units and memory in a single cycle. Arithmetic operations include y/x and $1/\sqrt{x}$. Two independent data-address generators support zero-overhead addressing (includes indirect), as well as modulo and bit-reverse address generation.

I/O controller—To maximize data movement, SHARC includes an I/O controller that executes I/O transfers in parallel with CPU execution. The controller manages 10 DMA channels, transferring data between internal memory and external peripheral devices and the host, serial, and link ports. All DMA controller operations are zero-overhead data transfers that generally do not interrupt or delay core thread execution. The synchronous serial ports can deliver transfer rates up to 40 Mbps; the six communication ports move data in 4-bit nibbles, transferring up to 1 byte/clock cycle. With six links operating simultaneously, there is a max throughput of 240 Mbytes/sec.

External interfaces—SHARC has a parallel port that serves as a direct interface to off-chip memory, peripherals, or a host processor. Up to six ADSP-2106x chips can share this bus with a common system-host processor; the bus implementation includes bus arbitration. The ADSP-2106x supports page-mode DRAM and fast SRAM external memory. It can access up to 4G words of external memory. For a 40-MHz clock, (25-nsec cycle) the chip requires a 15-nsec access time for zero-wait-state memory. The special host interface supports both 16- and 32-bit microprocessors, as well as system buses such as ISA and PCI. This host is treated like a memory-mapped device, with direct writes or read to internal memory.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, Package	Price
ADSP-21060 (512 kbytes)	33, 40	Run Idle	720 50	240-pin PQFP	$296
ADSP-21062 (256 kbytes)	33, 40	Run Idle	680 50	240-pin PQFP	$196

SUPPORT

☐ **HARDWARE** Analog Devices sells an ICE, which is a full-speed, nonintrusive, JTAG-based hardware tool that uses the ADSP-2106x built-in debugging capability. It runs under Microsoft Windows and supports debugging for multiple processor systems. Also available is the EZ-LAB Development System, a PC plug-in card for multiple 2106x processors.

☐ **SOFTWARE** Analog Devices supplies a C compiler that has full support for Numerical C, which extends C with vector- and matrix-processing capabilities for signal processing. Other tools include an assembler/linker, a simulator, application libraries, a PROM splitter, and a C source-level debugger.

AT&T DSP16xx

16-bit fixed-point DSP

☐ **OVERVIEW** The DSP16 has a core MAC unit, multiple on-chip memories, a small instruction cache, dual data-address generators, and multiple buses to move data in parallel. The DSP16 features a 16-bit external bus, three 16-bit internal buses, an 8-kbyte program/coefficient ROM block, a 1-kbyte data RAM block, and a small instruction cache. It loads 15 inner-loop instructions in the cache and then repeatedly executes them by pumping data and coefficients from the ROM and RAM blocks to the MAC execution unit. The chip also has a 16-bit host I/O port and a serial I/O port. Later versions add a bit-manipulation unit with a 16-bit barrel shifter, a second serial I/O port, and more peripherals; they also have a JTAG test/emulation port for chip test and in-circuit debugging.

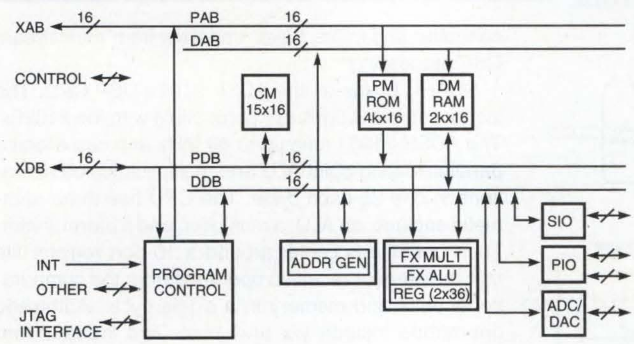
☐ **VENDOR CONTACTS**

AT&T Microelectronics, Allentown, PA, (800) 372-2447. **Circle No. 487**
BBS: (610) 712-4444, V.22bis, up to 2400 bps; (610) 712-1440, V.32bis, up to 14,400 bps (N,8,1).

DSP1617

- ▶ 8-stage pipeline, 46 instructions
- ▶ 4 36-bit accumulators; 4 alternate 16-bit regs
- ▶ 15-instruction cache
- ▶ 24-kbyte ROM (secure option)
- ▶ 3 buses: X, Y internal data
- ▶ 4-kbyte dual-ported RAM
- ▶ MAC unit with two 36-bit accumulators
- ▶ Bit-manipulation unit
- ▶ ROM, RAM address generators
- ▶ 2 64-kbyte address spaces
- ▶ 8-bit parallel I/O, two serial I/Os
- ▶ 2 external interrupts
- ▶ 38/40/50-MHz clock (1 cycle=1 clock), static design
- ▶ 5-cycle reg-to-mem ADD
- ▶ 1-cycle MPY, ACCUM (pipelined)
- ▶ No DIV instruction
- ▶ 2-cycle mem W; 1- to 2-cycle R
- ▶ Dual RAM access; 1-cycle penalty for accessing same bank
- ▶ Programmable wait states for each address-space segment
- ▶ 20/25-Mbps max for serial I/O
- ▶ 8-cycle interrupt latency
- ▶ ISRs and cache ops not interruptible; max cache-op latency is 1905 instr

ARCHITECTURE



The 16-bit DSP16 uses three internal buses to move instructions, coefficients, and data in parallel for high-throughput processing. The DSP CPU defines two 64k-word address spaces, one for program/coefficients and one for data. The X memory space holds both instructions and coefficients; the Y memory space holds data.

For fast inner-loop processing, an inner-loop code block is loaded into a 15-word instruction cache, and the on-chip X and Y memories supply the coefficients and data to drive MAC execution. The program must load the cache and execute the cached instructions via special instructions. The Y RAM is dual-ported, has eight banks, and supports multiple accesses. Accesses to the same bank, however, cause a 1-cycle delay. The DSP1610 and later versions have only one RAM block that holds both X coefficients and Y data, which can be accessed simultaneously.

The DSP has two address-generation units: the XAAU ROM address arithmetic unit and the YAAU RAM address arithmetic unit. These units have their own internal adders and registers to hold address values and offsets. The XAAU has a 12-bit adder, 12-bit static offset register, and four 16-bit pointer registers—the PC, program-return, program-interrupt, and table-pointer registers. The YAAU has eight static registers and an adder. In the original DSP16, the static registers were nine bits; in later processors, they are 16-bit registers. The XAAU and YAAU registers are accessible to programmers—you can use them for loading and storing.

The main execution unit is the DAU (data arithmetic unit), which has a 16×16-bit multiplier and a 36-bit adder with two accumulators. The multiplier and adder operate in parallel, and multiplier inputs and outputs are registered. A full MAC execution is pipelined. In the first stage, the registered inputs drive the multiplier, which outputs a 32-bit result into a holding register. The MAC can shift the multiply result before running it through the 36-bit ALU/shifter and into one of the accumulators. The DSP16 CPU uses fixed-point, 2's-complement arithmetic throughout. The bit-manipulation unit has a 36-bit barrel shifter, two 36-bit accumulators, and four general-purpose 16-bit registers.

The DSP CPU supports two memory spaces: a program/coefficient space and a data space. These address spaces are segmented, and the hardware handles multiple memory segments, each with different programmable wait states. Hardware pins and segment wait-state registers let you design-in multiple hardware memory segments with different access speeds.

☐ **VARIATIONS**

DSP16A—8/48-kbyte ROM, 2/4-kbyte RAM, serial I/O port, 8-/16-bit parallel I/O port, 84-pin PLCC.

DSP1604/06—16/32/48-kbyte ROM, 2/4-kbyte RAM, 24 I/O ports, DRAM controller, JTAG port, 84-pin PLCC, dual serial I/O, dual crystal oscillator, 2× timers, low-power modes.

DSP1605—32-kbyte ROM, 2-kbyte RAM, 8 I/O ports, 8-bit host interface, DRAM controller, dual serial I/O, 2× timers, dual crystal oscillator, low-power modes, 68-pin PLCC.

DSP1610—1-kbyte boot ROM, 8- or 16-kbyte dual-ported RAM, static design, sleep mode, bit-manipulation and barrel-shifter unit, two serial I/O ports, JTAG port, 16-bit timer, 4 external interrupts, 132-pin PQFP.

DSP1617—24-kbyte ROM, 4-kbyte dual-ported RAM, two 25-MHz serial I/O ports, power-management modes (sleep, sleep with slow clock, hardware stop pin), 5/3/2.7V operation, mask-programmable clock (internal 1 or 2×), single-cycle square function, 8-bit host and control I/O interfaces, bit/shift unit, JTAG port, 100-pin PQFP/TQFP.

DSP1618—16-kbyte ROM, 4-kbyte dual-port RAM, two 25-MHz serial I/O ports, power-management modes, 5/3/2.7V operation, mask-programmable clock (internal 1 or 2×), single-cycle square function, 8-bit host and control I/O interfaces, bit/shift unit, JTAG port, 100-pin PQFP/TQFP.

DSP1616X30—24-kbyte ROM, 4-kbyte dual-ported RAM, two 25-MHz serial I/O ports, power-management modes, 5/3/2.7V operation, mask-programmable clock (internal 1 or 2×), single-cycle square function, 8-bit host and control I/O interfaces, bit/shift unit, JTAG port, 100-pin PQFP/TQFP.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (10,000)
DSP1604/06	33	Run Sleep	100	84-pin PLCC	$15 to $20
DSP1605	33	Run Sleep	100	68-pin PLCC	$13.25
DSP1610	40	Run	130	132-pin PQFP	$63
DSP1617	50 30	Run Sleep SW stop	75 36 µA (2.7V) 28.6 µA (2.7V)	100-pin PQFP	$42.60
DSP1616X30	50	Run Sleep SW stop	50 (2.7V) 33 µA (2.7V) 28.6 µA (2.7V)	100-pin PQFP 100-pin TQFP	$27.40
DSP1618	50 30	Run Sleep SW stop	75 36 µA (2.7V) 26 µA (2.7V)	100-pin PQFP 100-pin PQFP 100-pin TQFP	$55

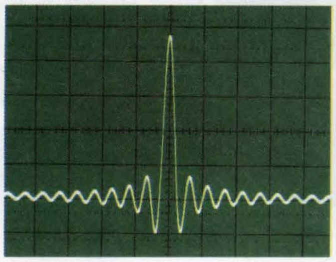
SUPPORT

☐ **HARDWARE** AT&T supplies a hardware-development system with an ICE pod. Evaluation and demo boards are also available.

☐ **SOFTWARE** AT&T sells software-development tools including a C compiler, assembler/linker, debugger, simulator, and application library.

Directory continued on pg 95

There are many areas where our function generator will surpass your expectations.



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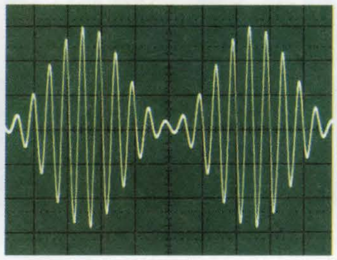
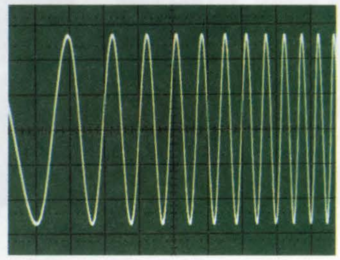


Internal AM, FM, FSK and burst modulation eliminate your need for a second modulation source.



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CIRCLE NO. 72

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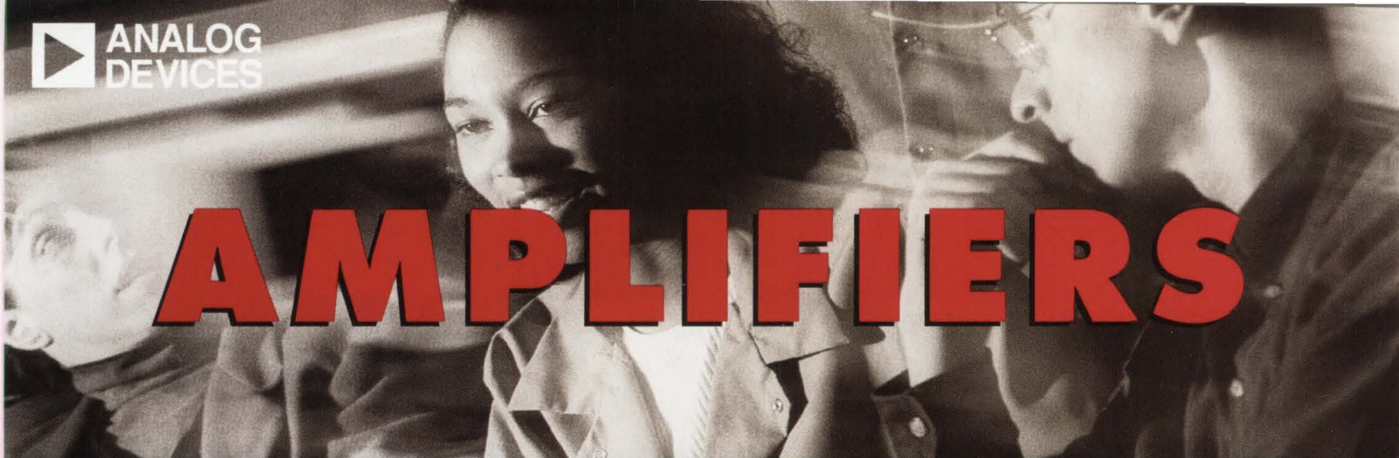
CIRCLE NO. 70

ANALOG DEVICES



NOBODY DOES AMPLIFIERS LIKE ANALOG DEVICES

IN THIS ISSUE

Whatever your application, ADI has the ideal amplifier for you. And they're available from national distributors and local sales offices nearby. In this issue you'll find our newest amplifiers, with performance and prices to meet the most demanding applications.

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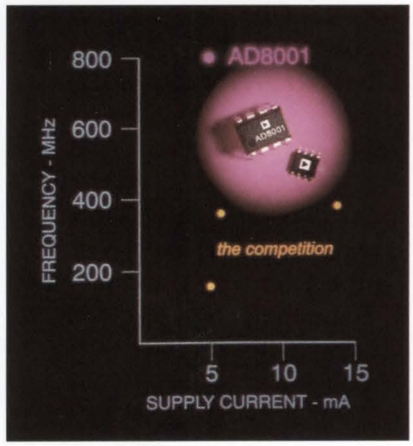
LEADERS IN HIGH SPEED

FASTEST AMP ON 50 mW

Introducing the industry's fastest op amp on 50 mW. The new AD8001 800-MHz unity-gain monolithic amplifier uses just 5 mA of supply current. It can process high-speed video signals in HDTV equipment, professional cameras and graphics workstations. Video-specific parameters include 0.1 dB gain flatness to 100 MHz, 0.01% differential gain, 0.025° differential phase (G = +2, R_L = 150 Ω).

Other specifications include 1,200 V/µs slew rate and 10 ns settling of 2 V steps to within 0.1%. A single AD8001 can provide 70 mA of output current and drive up to six back-terminated (75 Ω load) cable lines. Full power bandwidth is 125 MHz with 5 V p-p signal swings. The AD8001's worst harmonic component at 20 MHz is -60 dB, and voltage noise at 10 kHz is only 2 nV/$\sqrt{\text{Hz}}$.



The AD8001 is packaged in an 8-pin plastic DIP or SO-8 and operates from –40°C to +85°C. Military grades will be available with operation from –55°C to +125°C. Prices begin at $2.75 in 1,000s.

CIRCLE 1

LOW-POWER 110-MHz BUFFER RUNS COOL

The 110-MHz BUF04 slews at 3,000 V/µs and consumes only 6.9 mA. At ±5 V, you can reduce power to one-third with full ±15 V performance. Closed-loop design provides low offset and great gain accuracy, and ±10 V signals settle to within 0.1% in 60 ns. Best of all, the BUF04 is packaged in low-profile SO-8 and 8-pin DIPs.

Applications include a/d converter buffering, video cable driving, pulse detection, pro-audio d/a converters, and more. The BUF04 operates from ±5 V to ±15 V supplies over temperatures from –40°C to +125°C.

CIRCLE 2

BUF04 KEY SPECS

Parameter	Min	Typ	Max	Units
GBW		110		MHz
Slew Rate	2,000	3,000		V/µs
Supply Current		6.9	8.5	mA
Voltage Noise Density		4		nV/$\sqrt{\text{Hz}}$
Offset Voltage		0.3	1	mV
Gain Linearity		0.005		%

Prices, from $3.71 in 1,000s.

1 Specifications with ±15 V supply operation

WIDE BAND OP AMPS FOR VIDEO, IMAGING, AND COMMUNICATIONS

These new high-speed op amps provide optimal price/performance in a wide range of video-speed applications. They excel at driving heavy capacitive loads. Some are specified for operation on single +3 V to +5 V supplies, others use common ±5 V and ±15 V dual supplies.

AMPS WITH LOW ΔG/ΔØ

If you need high output drive, try the AD811. It's a high-performance video amplifier with superb video specs to preserve signal fidelity in high-definition TV systems. The AD811 delivers high output drive of 100 mA for efficient line driving. It's specified over a wide power supply range of ±4.5 V to ±18 V and uses just 16.5 mA of power supply current.

Other family members include the AD810 and AD812, ideal for broadcast-quality applications. The AD810 is a low-power version that consumes just 6.8 mA in normal mode, while a DISABLE feature further reduces power to only 2.1 mA. The versatile and low-cost dual AD812, runs on a single +3 V or +5 V supply, or from ±5 V or ±15 V supplies. Package options include 8-pin plastic DIPs, 16- and 20-pin SOICs, 8-pin Cerdips, or 20-pin LCCs.

CIRCLE 3

TRIPLE VIDEO AMP WITH FAST DISABLE

The triple AD813 packs three current-feedback op amps, each with its own independent 80 ns disable function. It offers unprecedented gain flatness for high-quality computer video and broadcast video gear. Operation is from either single +3 V to +5 V, or ±5 V to ±15 V supplies. Supply current is a low 3.5 mA (+3 V) and it delivers 100 MHz of unity gain (–3 dB) bandwidth.

For video muxing, CCD-based equipment, and RGB line driver applications, nothing matches the AD813. It operates from –40°C to +85°C and comes in small 14-pin DIP or narrow body SOIC packages.

CIRCLE 4

LOW-COST, GENERAL-PURPOSE AMPLIFIERS

The AD817 is optimized for applications that require unity-gain stable operation. Its counterpart, the AD818 is tailored for gains of magnitude equal to or greater than +2 or –1. The AD818, with low differential phase and gain errors, is great for video cameras and pro video equipment. As an ADC buffer or line driver, the AD817 excels with its combination of high output current and unlimited capacitive load drive.

CIRCLE 5

HIGH-SPEED FET-INPUT

The AD843 and AD845 FET-input op amps combine excellent ac and dc performance with low power consumption. The dc performance of these unity-gain stable op amps is perfect for high-speed data acquisition systems. Their low input bias current and offset voltage can reduce errors in high-speed active filters, integrators, peak detectors, and current-to-voltage converter circuits.

Dynamic performance is equally impressive. They have low total harmonic distortion for high-speed sample/hold circuits, ADCs, and DSP front-end circuits. They also have industry-standard pinouts and can upgrade system performance. Both op amps operate from ±15 volt supplies with five performance grades specified over commercial, extended, and military temperature ranges.

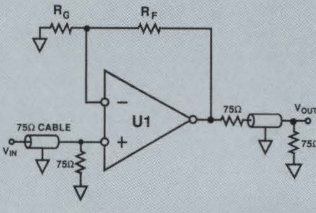
CIRCLE 6

VIDEO LINE DRIVING MADE EASIER

The figure below depicts a video line driver circuit and provides a list of recommended products with associated resistor values. When using a current feedback op amp for U1, closed-loop bandwidth largely depends on the value of the feedback resistor R_F.

Attenuation of the circuit's open-loop response, especially when driving a load value <250 Ω, will also affect its bandwidth. Gain resistance (R_G) is typically set for stable operation at G = 2. Low values of R_G and R_F will minimize the circuit's feedback time constant and nonlinear behavior. The use of 1% metal-film resistors ensures the widest possible 0.1 dB bandwidth. To achieve even wider bandwidths, you can reduce the magnitude of R_F, but you run the risk of increasing signal peaking. Use maximum supply voltages and limit amplifier loads to minimize signal distortion.

With the exception of the AD8001, which operates from ±5 V supplies, the products in the chart below are characterized with ±15 V supplies. Bandwidth is a measure of gain flatness at 0.1 dB.



MODEL	0.1dB BW (MHz)	ΔG (%)	Δφ (°)	RF/RG (Ω)
AD8001	110	0.01	0.025	750
AD811	35	0.01	0.01	649
AD812	40	0.05	0.02	715
AD813	50	0.03	0.06	681
AD818	55	0.005	0.045	1,000

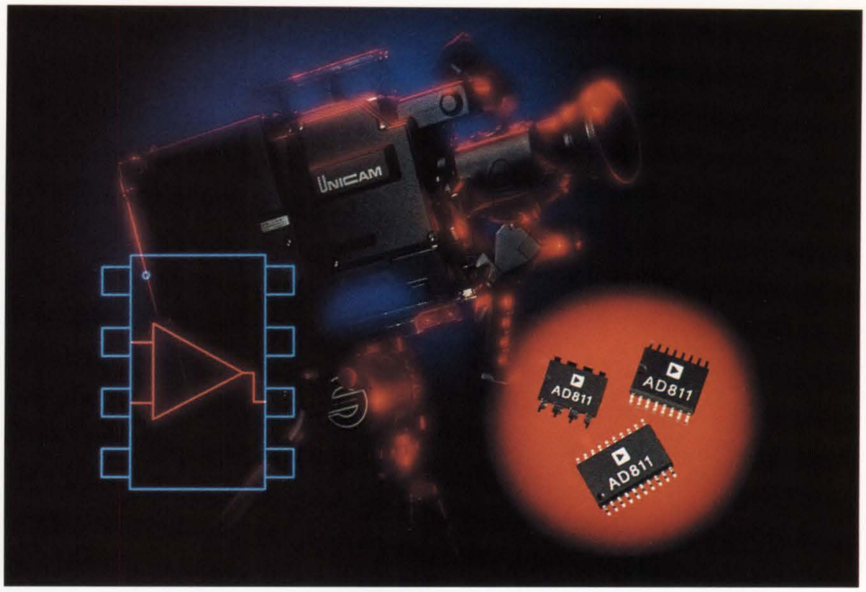
HIGH SPEED QUAD WITH PRECISION

The OP467, with four fast op amps in one package, has the fastest slew rate (170 V/µs) and settling time (≤200 ns to 0.01%) among quads. In multichannel systems, it can save space, reduce power and cost, and increase reliability. It's unity-gain stable and can drive high-capacitance loads up to 1,600 pF.

Besides its speed, it offers a low 200 µV offset. Use the OP467 in high-speed instrumentation and test equipment, high-speed detectors, laser scanners, sonar arrays, and other applications that need speed, accuracy, and a wide ±5 to ±15 V operating range. It's housed in 14-pin plastic DIP, cerdip, 16-lead SOL, and 20-contact LCC surface-mount packages. CIRCLE 7

IMPROVED EL2020

The ADEL2020, a superior second source, will improve performance with less power drain and lower cost. Low differential gain and phase errors make it ideal for low-power video applications. The ADEL2020 is available in either plastic DIP or SOIC packages specified over the -40°C to +85°C industrial temperature range. CIRCLE 8

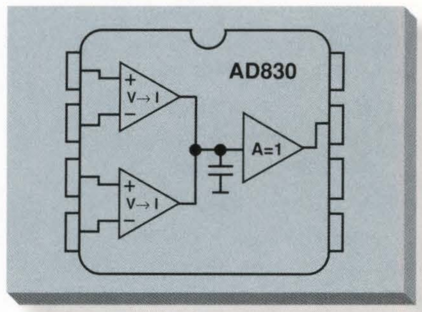


AN AMPLIFIER WITH A DIFFERENCE

The AD830 wideband amplifier rejects high-frequency common-mode voltage noise in differential line receiver applications. It handles differential signals, system grounds, and low-distortion high-frequency amplification. With >±50 mA full-output-current drive, it's useful for driving heavy loads. And its output clamping is great for driving ADCs.

Other benefits include balanced impedance inputs, symmetrical circuit behavior for gain of either +1 or –1, and low sensitivity to source resistance.

The AD830 uses ±15 V and ±5 V supplies, but its special offsetting capability allows it to perform with single supplies from +10 to +30 V. Packages include 8-pin plastic miniDIP, cerdip, and SOIC. CIRCLE 9



MODEL	AD810	AD811	AD812	AD813	AD817	AD818	AD843	AD845	OP467	AD830	UNITS
Channels	Single	Single	Dual	Triple	Single	Single	Single	Single	Quad	Single	
Supply Voltages	±5, ±15	±5, ±15	+3 to ±15	+3 to ±15	+5 to ±15	+5 to ±15	±15	±15	±5, ±15	±5, ±15	Volts
Feedback	Current	Current	Current	Current	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	
BW, 0.1 dB (G=+2)	30	35	40	50	16	55	—	—	—	15	MHz
BW, –3 dB (G=+1)	80	140	145	125	50	130 (+2)	34	16	28	100	MHz
Slew Rate	1,000	2,500	1,600	450	350	500	250	100	170	530	V/µs
Settling Time (0.01%)	125	65	40 (0.1%)	40 (0.1%)	70	80	135	350	200	35 (0.1%)	ns
ΔGain Error	0.02	0.01	0.02	0.03	0.04	0.005	0.025	0.04	—	0.05	%
ΔPhase Error	0.04	0.01	0.02	0.06	0.08	0.045	0.025	0.02	—	0.08	°
V_n (10 kHz)	2.9 (1 kHz)	1.9 (1 kHz)	3.5	3.5	15	10	19	18	6 (1 kHz)	27	nV/$\sqrt{Hz}$
Max V_{OS}	6	3	5	5	2	2	2	1.5	0.5	±3	mV
Min Output Current	40	100 (typ)	40	50	50	50	50	50 (typ)	50 (typ)	±50	mA
Max Supply Current	8	18	5.5	5.5	7.5	7.5	13	12	10	14.5	mA
Prices in 1,000s	$2.08	$2.85	$2.48	$3.74	$1.52	$1.69	$3.70	$2.76	$4.86	$2.42	USD
	CIRCLE 3	CIRCLE 3	CIRCLE 3	CIRCLE 4	CIRCLE 5	CIRCLE 5	CIRCLE 6	CIRCLE 6	CIRCLE 7	CIRCLE 9	

1.800.262.5643

LOW-POWER PRECISION FAMILY

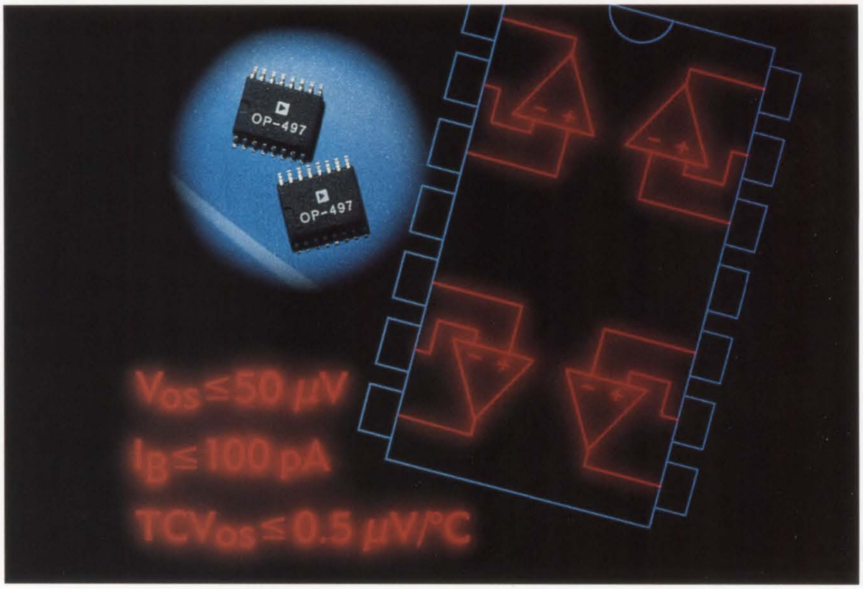
When your design demands precision and low power, nothing beats the OP97 family. The OP97 (single) OP297 (dual) and OP497 (quad) are great for designs that need very low bias currents.

The OP97 family is ideal for sample-and-hold circuits, peak detectors, and logarithmic amplifier designs that exhibit low leakage current. Thermocouples, strain gages and other industrial equipment need the OP97's accuracy over wide temperature ranges. Unlike conventional FET-input op amps, these ICs use a unique current cancellation circuit to keep bias current low over the entire temperature range.

The family combines low power consumption with guaranteed accuracy. Maximum voltage offset at 25°C is only 50 µV (with only 0.5 µV/°C drift) and bias current is 100 pA. Minimum open-loop gain is 2 kV/mV. Combined, these specs can eliminate the need for offset trims and additional gain stages.

Battery and low-powered systems will benefit from the OP97 family's low supply current: 625 µA (max) per channel. Wide supply voltages range from ±2 V to ±20 V. Packaging options include 8- and 14-pin DIPs and cerdips, 8- and 16-pin SOICs, and 20-contact LCCs.

CIRCLE 10



WHAT'S BETTER THAN THE OP-07?

The OP177 is today's industry standard for ultrahigh precision. Maximum offset voltage is only 10 µV, with less than 0.1 µV/°C V_{OS} drift, eliminating external V_{OS} trimming and increasing system accuracy over temperature. Other guaranteed specifications include minimum 130 dB CMRR and 120 dB PSRR.

This low-noise, bipolar-input op amp is a good alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without high noise, low frequency chopper spikes, external capacitors, and limiting common-mode input voltage range. The OP177 is available in 8-pin plastic, cerdip and SO-8 packages. Cerdip and 20-lead LCC devices are guaranteed over extended and military temperature ranges.

CIRCLE 11

DUALS AND QUADS TOO

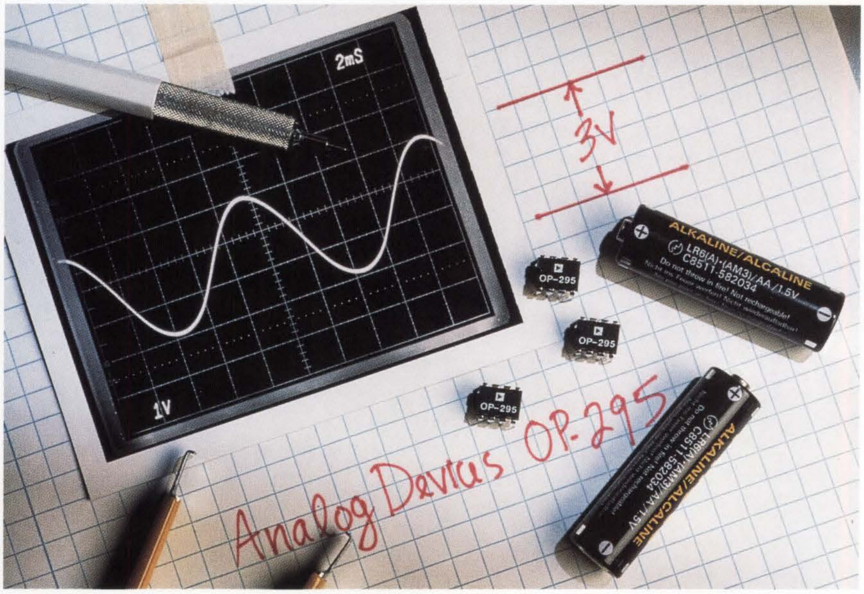
The dual OP200 and quad OP400 offer great performance over temperature and use very little power. For example, the OP200's input offset voltage is typically 25 µV with only 0.2 µV/°C drift from –55°C to +125°C. Its supply current (per amplifier) is a scant 570 µA. Industry standard DIP, SOL and LCC packages are available.

CIRCLE 12

MODEL	OP97	OP297	OP497	OP177	OP200	OP400	UNITS
Channels	Single	Dual	Quad	Single	Dual	Quad	
Offset Voltage (V_{OS})	25	50	50	10	75	150	µV, max
V_{OS} Drift	0.6	0.6	0.5	0.1	0.5	1.2	µV/°C, max
Offset Current (I_{OS})	0.1	0.1	0.1	1	1	1	nA, max
Input Bias Current	±0.1	±0.1	0.1	1.5	2	3	nA, max
Voltage Noise @ 1kHz	14	17	15	(118)	11	18	nV/√Hz (nV $_{RMS}$)
Current Noise	20	20	20	(8)	400	600	fA/√Hz (pA $_{RMS}$)
CMRR	132	120	120	130	120	120	dB, min
PSRR	132	120	120	120	-	-	dB, min
Input Voltage Range	±14	±14	±14	±13.5	±13	±13	V
Bandwidth (G=+1)	900	500	500	600	500	500	kHz
Supply Current	600	625	625	2,000	725	725	µA, max
Prices in 1,000s	$1.00	$2.50	$4.04	$0.95	$2.48	$4.50	USD
	CIRCLE 10	CIRCLE 10	CIRCLE 10	CIRCLE 11	CIRCLE 12	CIRCLE 12	

SINGLE-SUPPLY AMPLIFIERS DELIVER TOP PERFORMANCE AT LOW COST. INDUSTRY'S BROADEST PRODUCT LINE

Nobody has a broader product portfolio of single-supply amplifiers for low-power and battery-powered gear. These are just a few of the products we've recently introduced.



LOW-COST DUALS AND QUADS OUTPERFORM CMOS AMPS

The dual OP292 and quad OP492 single-supply op amps are low in cost and outperform comparably priced CMOS devices. These 4 MHz, 4 V/µs amplifiers combine the qualities of complementary bipolar—low noise, precision and output drive capability—with the low cost of CMOS devices. With +5 V supplies, the OP292 guarantees 2.4 mV maximum (500 µV typ) offset over our new HOT temperature range (–40°C to +125°C), at no additional cost.

Unlike competitive ICs, the inputs of these amplifiers can swing well below ground with output swings to ground. The OP292 and OP492 draw less than 1.4 mA per channel, excellent for multichannel battery-powered applications. Both amps feature low voltage and current noise: 15 nV/$\sqrt{Hz}$ and 0.7 pA/$\sqrt{Hz}$, and channel separation (at 1 kHz) is 100 dB.

Applications that can take advantage of the OP292 and OP492 include disk drives, mobile phones, multichannel industrial and servo control systems, modems, fax machines, pagers, and power supply monitoring circuits. Packaging options include 8- and 14-pin plastic DIPs or surface-mount narrow-body SOICs. USD prices for the OP292 and OP492 start at $1.32 and $2.16, respectively.

CIRCLE 13

3-V TO 30-V RAIL-TO-RAIL

The dual OP295 and quad OP495 3-V single-supply op amps are the industry's highest accuracy, lowest power true rail-to-rail amplifiers. Their low 30 µV offset, combined with a high gain of 1,000 V/mV, makes them ideal for portable instrumentation. On a 3 V supply, they drive a 10 kΩ load from 2.90 V to within only 2 mV of ground—perfect for process and motor control circuitry.

For driving coax cable, large FETs, or other capacitive loads, the OP295 and OP495 offer stability with loads up to 300 pF. They can supply over ±25 mA to the load on ±15V supplies (±18 mA at +5 V), with a typical gain-bandwidth product of 75 kHz.

The OP295 uses less power than CMOS chips, gives exceptionally low voltage offset drift (typically 1 µV/°C), and requires only 50% of the quiescent current of the closest competitive product.

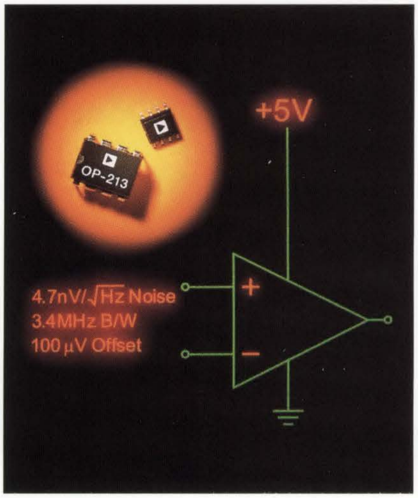
The OP295 and OP495 are specified from -40°C to +125°C and packaged in plastic DIPs and SOICs. Die are also available. USD prices in 1,000s begin at $1.98 and $3.56, respectively.

CIRCLE 14

HIGH PRECISION AT +5 V

The OP113, OP213 and OP413 are single, dual and quad single-supply precision amplifiers. Operating from +5 V to ±15 V, these op amps feature low noise (4.7 nV$\sqrt{Hz}$),3.5 MHz bandwidth, 75 µV offset voltage, and drift of just 0.2 µV/°C. Applications include automotive, process control, portable instruments, and pressure/strain gages. Packaging options range from 8-lead SOIC and plastic DIP to 16-lead SOL packages. USD prices in 1,000s begin at $1.47 (single), $2.21 (dual) and $4.92 (quad).

CIRCLE 15

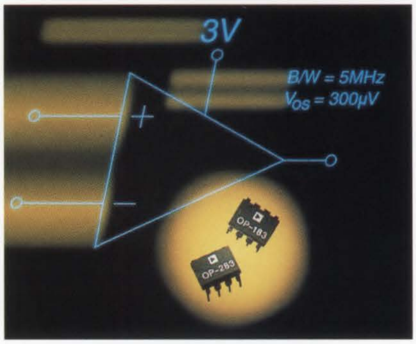


SINGLE-SUPPLY FET

The AD820 (single) and AD822 (dual) are precision, low-power, FET-input op amps that operate from a single +3 to +36 V range, or with dual supplies from ±1.5 to ±18 V. Their outputs swing from rail to rail (within 10 mV) and their inputs can swing 0.2 V below ground. The JFET input stage maintains low bias current (≤10 pA at 25°C, B grade), with offsets as low as 900 µV max over temperature (–40°C to +85°C) and 25 nV/$\sqrt{Hz}$ noise at 10 Hz.

Though the quiescent current drain is only 620 µA, both the AD820 and AD822 will drive loads of up to 15 mA and 350 pF. They both have a unity gain bandwidth of 1.8 MHz and 3 V/µs slew rate. A 3-volt version is optimized for low-power operation from –40°C to +85°C at no extra cost. The AD820 and AD822 are available in 8-pin plastic DIPs and SOICs.

CIRCLE 16



INDUSTRY'S FASTEST 3 V SINGLE-SUPPLY AMP

If your 3 V system needs a gain bandwidth product greater than 1 MHz, select the OP183 or OP283. They combine 5 MHz bandwidth with low noise for use in low voltage applications, such as ADC buffering, filtering, servo control and audio for portable computers.

These two amps are thoroughly specified for +3 V, +5 V and ±15 V supply operation. Unlike competing 3 V devices that specify only typical performance characteristics, the OP183 and OP283 guarantee low offset, high gain, and input and output ranges that include ground. Noise is typically a low 10 nV/$\sqrt{Hz}$, and both amplifiers can sink and source 25 mA—even with a 3 V supply.

Both devices are specified from –40°C to +85°C and are available in 8-lead plastic DIPs and SO-8 packages. Prices for the OP183 and OP283 (in 1,000s): $1.42 and $2.15, respectively.

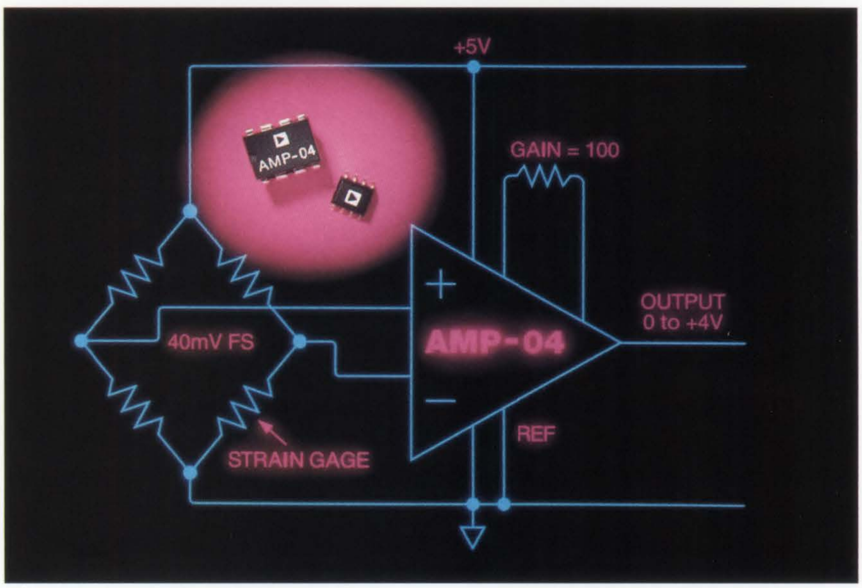
CIRCLE 17

SINGLE-SUPPLY INSTRUMENTATION AMPLIFIERS FEATURE SINGLE-SUPPLY, HIGH ACCURACY, LOW COST

When accuracy, space and cost are your concern, one of these three in-amps will provide the lowest cost solution—especially when compared with the time to design and implement an equivalent circuit.

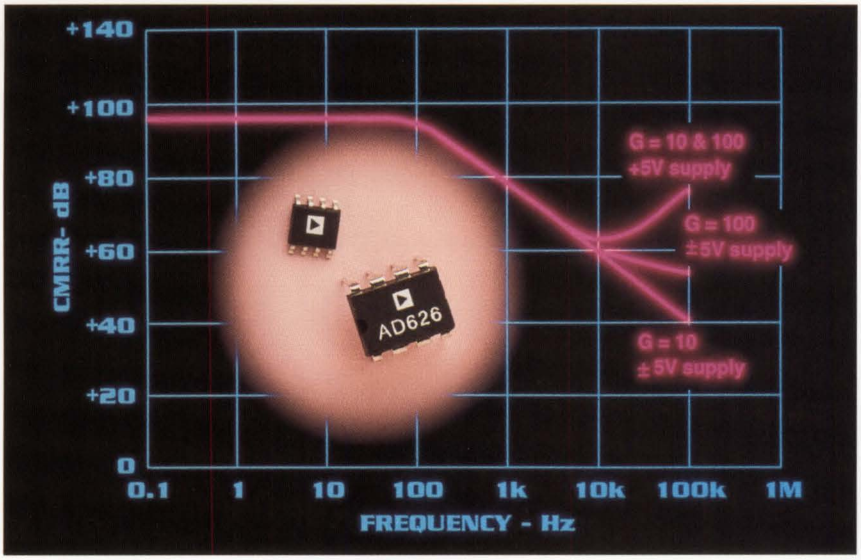
SINGLE SUPPLY IN-AMP

Specified for operation from +5 to ±15 volts, the AMP04 precision in-amp packs accuracy in a small SO-8 footprint for those difficult single-supply designs. The AMP04 can eliminate the need for a separate gain stage to isolate low-level differential signals from high-level common-mode signals. Gain is easily programmable from 1 to 1,000 with a single resistor.



The AMP04 has an input offset current of 1 nA for direct connection to strain gages and high-impedance transducers. Guaranteed max specs include 3 µV/°C offset drift, 150 µV offset voltage, and 0.005% gain nonlinearity, while requiring only 700 µA of supply current. A unique feature of the AMP04 is that it doesn't exhibit common-mode swing limiting at high gain, unlike "triple-amp" designs (see sidebar).

The AMP04 precision in-amp is specified for operation from -40°C to +85°C. Package options include an 8-pin plastic DIP, 8-pin SOIC, or 8-pin cerdip. USD prices (in 1,000s) begin at $4.55. CIRCLE 18



LOW-COST IN-AMP REPLACES DISCRETE DESIGNS

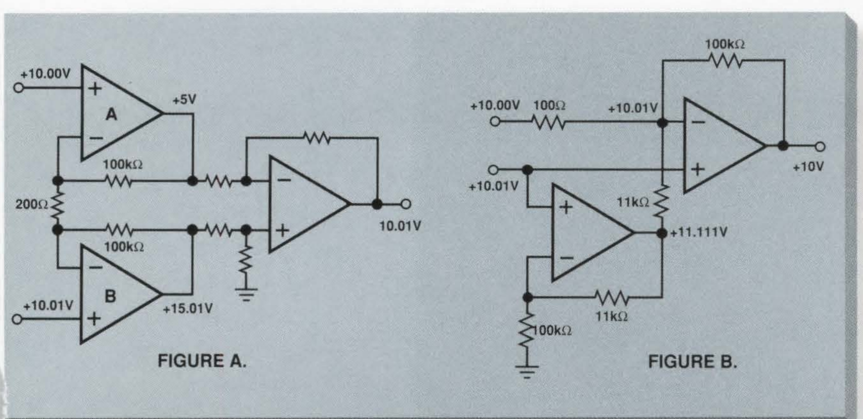
The AD620 high-accuracy in-amp replaces discrete designs with less overall error, lower power use, and reduced board space. It allows for gains from 1 to 1,000 set by a single external resistor. Noise is low (0.28 µV p-p, 0.1 to 10 Hz and 9 nV/√Hz at 1 kHz); bandwidth is 120 kHz (G = 100). With guaranteed-maximum 50 µV voltage offset, 0.6 µV/°C drift, 1 nA input bias current, and 40 ppm nonlinearity—and minimum 93 dB CMR (G = 10)—it's ideal for weigh scales, transducer interfaces and ECG circuits. The supply range is a wide ±2.3 V to ±18 V, at 1.3 mA (maximum). Prices in 1,000s begin at $3.27 USD.

CIRCLE 19

SINGLE-SUPPLY DIFFERENTIAL AMP

The AD626 is a single-supply, low-power differential amplifier with on-chip gains of 10 and 100 V/V (externally set). Its supply range is +2.4 to +10 V single, ±1.2 to ±6 V dual, drawing less than 290 µA of current. Uses include current sensing and sensor interfacing, especially in battery and portable applications. Its common mode range, 6 (V_S – 1 V), exceeds the supply; for +5 volt supply, CMR = 90 dB and the output range is +30 V to +4.7 V (minimum). Its inputs are overload protected (50 V continuous), and the internal attenuation network includes RFI filters. Prices (1,000s) start at $2.85 USD.

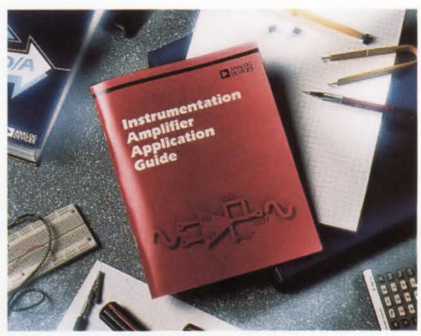
CIRCLE 20



EXTEND COMMON-MODE SWING LIMITATIONS AT HIGH GAIN

In traditional three op amp in-amp designs, common-mode voltage (CMV) range is limited at high gain. For example, the in-amp circuit below (Figure A) is designed for a gain of 1001 with a CMV of 10 volts, but there's a problem. Amplifier B must swing to 15.01 volts in order for the circuit's output to swing to 10.01 volts. Operating from a +15 V supply, an op amp cannot handle this swing range. The output will saturate before reaching the supply rails.

The single-chip AMP04 in Figure B, operating at the same common-mode conditions, does not exhibit this limitation. None of its internal nodes reach signal levels that are high enough to cause amplifier saturation. In addition, the AMP04 maintains a gain accuracy of 0.5%, provides high input impedance (4 x 10^9), and features 105 dB of CMRR at a gain of 1,000.



Instrumentation Amplifier Guide

CIRCLE 21

1.800.262.5643

The AD797 features the industry's lowest voltage noise and distortion. It's an excellent choice for use in audio preamplifiers, FFT and spectrum analyzers, and IR and ultrasound imaging: $V_n = 0.9\ nV/\sqrt{Hz}$ and remains flat over the full 8 MHz bandwidth (Gain = 10) at 1 kHz. Total harmonic distortion is -120 dB at 20 kHz. Settling time is 800 ns to 16-bit accuracy.

Many dc specifications are guaranteed, including a maximum 60 µV voltage offset with 0.6 µV/°C drift, 300 nA (200 nA typical) input offset current, and 2 µA input bias current. The AD797 features a fast 20 V/µs slew rate and a gain-bandwidth product of 110 MHz (Gain = 1,000). Full-power bandwidth is 280 kHz at 20 Vp-p. Output current drive is typically 50 mA, permitting the use of low-value gain-setting resistors to curb resistor noise.

AD797 operates from ±5 to ±15 V supplies over the -40°C to +85°C industrial and -55°C to +125°C military temperature ranges. Packages include 8-pin plastic DIP, SOIC and cerdip. Prices start at $3.36 (1,000s).

CIRCLE 22

LOW-POWER AUDIO AMPS COMBINE ADVANTAGES OF JFET & BIPOLAR CHIPS

The single OP176 and dual OP275 op amps feature a patented input circuit (combining both JFET and bipolar technologies) that offers new levels of performance to audio, instrumentation and consumer applications. The result is an op amp that offers the traditional benefits of bipolar amps (low distortion and voltage noise) with the advantages of JFETs (high slew rates, and wide dynamic range) at one third the power of the NE5532.

The OP275 features 0.0006% total harmonic distortion plus noise and 6 $nV/\sqrt{Hz}$ voltage noise density. Input offset voltage is guaranteed at <1 mV allowing the OP275 to be used in dc coupled or summing applications without adding noisy offset adjustment circuitry. Dynamic characteristics include 22 V/µs slew rate and 9 MHz gain-bandwidth product. In addition, the OP275 uses less than 5 mA of supply current, even with ±22 volt supplies.

For professional audio console designs, the small SO-8 package combined with the low power can save many square inches of board space and many watts of power, resulting in cooler operation and greater density.

Its companion, the OP176 has the same attributes with greater output swing and output short-circuit protection, at much lower power than NE5534, plus it's stable at unity gain.

Both the OP176 and OP275 are specified over the -40°C to +85°C extended industrial temperature range and are available in 8-pin plastic DIP or SOIC packages. The SOIC package is offered in 2,500 piece spools for high volume handling. Prices for the OP176 and OP275 begin at $.88 and $1.08, respectively in 1,000s.

CIRCLE 23

FREE SPICE DISK CONTAINS OVER 350 MODELS

ADSpice puts the power to predict amplifier behavior in your PC. This free disk contains the most innovative and comprehensive library of SPICE models ever. It contains over 350 complete models, including hundreds of high-speed and precision op amps, CMOS analog switches, variable-gain amplifiers, and video-difference amplifiers.

This valuable tool uncovers design problems before you breadboard by simulating real-world transient and ac electrical conditions. Critical performance models such as noise, bandwidth, and phase response are included. Don't miss this free offer, available on either 3-1/2" or 5-1/4" IBM PC-compatible disks.

Circle 24 (3-1/2")
Circle 25 (5-1/4")

MODEL	AD797	OP176	OP275	Units
Channels	Single	Single	Dual	
GBW	110	10	9	MHz
Slew Rate	20	25	22	V/µs
Supply Current	10.5	2.5	5	mA, max
THD + N	(98)	0.001	0.0006	(dB) %
Offset Voltage	0.8	1	1	mV, max
V_{OUT} Swing	±13	±13.5	±13.5	V
Price in 1,000s	$3.36	$0.88	$1.08	USD
	CIRCLE 22	CIRCLE 23	CIRCLE 23	

WORLDWIDE HEADQUARTERS

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ANALOG DEVICES

‹T&T DSP32C/3210 — 32-bit floating-point DSP

DSP3210	
► 68 instruction, 3-stage pipeline ► Two 4-kbyte RAM blocks ► 1-kbyte boot ROM ► 32-bit barrel shifter ► 32-bit address space; big/little-endian addressing ► External memory bus: 32-bit addr, 32-bit data; bus adapted to 680x0 and 80x86 bus systems ► Serial I/O port, 2 DMA channels ► 32-bit timer ► 2 ext intr	► 55/66.7-MHz clock (2 clocks/cycle) ► 4 X clocks per cycle ► Multiple operations/cycle using phased X clocks ► 1-cycle MAC, ADD (pipelined) ► 660-nsec floating-point DIV ► Up to 2 external memory R/W accesses/cycle ► 4-word external-memory burst ► Wait states=cycle/4 ► 180-nsec intr latency (3 cycles)

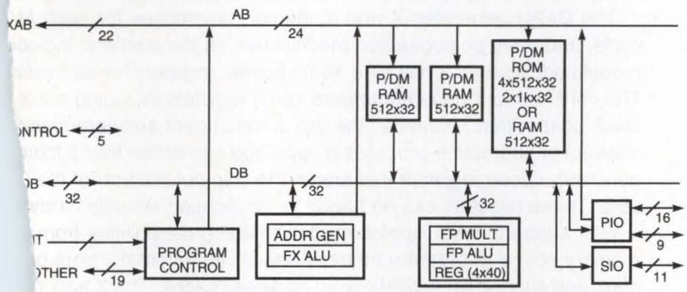
] **OVERVIEW** Introduced in 1984, AT&T's DSP32 was one of the ;st general-purpose 32-bit floating-point DSP processors. It has a fair- straightforward, microprocessor-like architecture. It delivers peak ngle-cycle (pipelined) instruction execution and has a 1-cycle MAC ıit. The DSP32 was later upgraded to CMOS, called the DSP32C, ıich was then followed by the DSP3210, a cost-reduced DSP32C for ecommunications and multimedia applications.

The DSP32C features a main bus, program ROM, three RAM blocks, ıd three functional units. These functional units are the data arithmetic ıit with 32-bit floating-point multiplier and adder; a control arithmetic unit th a 16-/24-bit ALU; and a serial I/O peripheral. The DSP32 architecture ɜts its speed from the use of high-speed on-chip memories that enable ıe CPU to perform multiple sequential accesses within a single cycle. The ;PU has three pipeline stages. Each stage takes two external clocks but ɪs four sequential time-slot clocks for multiple sequential operations in a ven cycle. Thus the CPU can handle up to four memory accesses per ʼcle: an instruction fetch, two operand (X,Y) fetches, and a memory write.

The later DSP3210 reduces motherboard design-in costs by direct- supporting standard µP buses such as the 680x0 and 80x86 buses. also has an on-chip DRAM controller. The DSP3210 has two on-chip AM blocks, which can hold data or code, and a small boot ROM. AT&T designed the VCOS Visible Cache Operating System in conjunction with the DSP3210. The operating system helps cut costs by letting the DSP3210 use motherboard main memory for caching instructions and data and for external storage instead of having the DSP rely on more-expensive on-chip RAM/ROM or external SRAM.

☐ **VENDOR CONTACTS** **AT&T Microelectronics,** Allentown, PA, (800) 372-2447. **BBS:** (610) 712-4444, V.22bis, up to 2400 bps; and (610) 712-1440, V.32bis, up to 14,400 bps (N,8,1). **Circle No. 488**

ARCHITECTURE



ne of the first 32-bit floating-point DSPs, the DSP32 has a register- ıted architecture that centers on a set of general-purpose registers. ;o has a dedicated MAC unit with four built-in 40-bit accumulators does a MAC operation in a single instruction cycle. The DSP32 has ıple architecture: Rather than use multiple buses to move the ıctions and data needed for a single cycle, it has a single internal hat can handle up to four sequential operations per cycle. The can access three 2-kbyte RAM blocks (or two RAM blocks and 4 s of ROM) and drives two core functional units. The first functional ; the data arithmetic unit (DAU), which has the floating-point mul- r and adder and four 40-bit accumulators. The second unit is the ol arithmetic unit (CAU), which has an integer ALU and 22 24-bit essing registers that handle both program and data addressing. SP32 family members have a high-speed internal bus that can handle four operations/instruction cycle. The CAU can generate up to four esses/cycle, one for each phase or state of an instruction cycle. The is pipelined; it has a 4-stage pipeline for a MAC cycle. Thus, the results a MAC cycle initiated by instruction 1 will be available when instruc- ; starts its first cycle; that is, the fifth cycle from the start of the MAC ıction. The CAU runs in parallel with the DAU; it executes addressing ıtions as well as control, data-move, and integer ALU operations.

ɜ latest DSP32 version, the DSP3210, is a cost-reduced DSP32C.)SP3210's on-chip RAM has been reduced to two 4-kbyte RAM ; supplemented by a 1-kbyte boot ROM. The DSP32C's DMA ller has been eliminated and replaced by a serial DMA controller -CPU data moves. The DSP3210 also has full 32-bit external- y addressing: The external bus has a 32-bit address, and the ıs 32-bit—rather than 24-bit—address registers. For low-power ɔn, both the DSP3210 and the DSP3207 run at 3.0V.

The DSP3210 is tailored for multimedia, telecommunications, and graphics applications. Instead of relying on on-chip memory, the DSP3210 can use low-cost, external DRAM to hold code and data. It can share the motherboard's system memory instead of requiring its own expensive SRAM. AT&T's VCOS operating system has been designed for DSP3210 applications. A minimal OS, the kernel is only 400 bytes. The VCOS kernel resides in on-chip memory along with critical instructions and data. The OS uses external system memory to cache pending code and data. The DSP3210 interfaces directly to standard ISA and MCA buses without external logic.

Addressing modes—Immediate, memory direct, register direct, register indirect, bit reversed (special case of register indirect), PC relative. Indexing is available as are postincrement and decrement options for register-indirect addressing.

Special instructions—DO next *k* instructions; DO LOCK, signals interlocked bus, DO BLOCK, signals quad word transfer; conditional increment/decrement; conditional ALU operations; compare; conversion to IEEE format; go-to loop with counter, and create a seed (reciprocal of Y).

DMA controller—Supplies two DMA channels (input and output) for moving data between memory and the serial I/O buffer. The DMA controller can access internal and external memory. It uses cycle stealing to move data and does not disturb the CPU's execution thread. The controller has its own set of control registers and can move single or multiple data frames. The controller can be restricted to request DMA cycles only when the DSP processor has ownership of the shared external bus. This strategy ensures that DMA operations won't incur the overhead of bus-master requests.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (10,000)
DSP32C	40	Run	180	133-pin PGA	$70
	50	Run	225	164-pin PQFP	$57
DSP3210	55	Run	220	132-pin PQFP	$44
		Wait	86		
	66	Run	285		$62
		Wait	103		
DSP3207	40	Run	150 (3V)	132-pin PQFP	N/S
		Wait	6 (3V)		
		Gated-clock	0.6 (3V)		
	66/55	Run	282/220		N/S
		Wait	26/22		

SUPPORT

ꟷ **RDWARE** AT&T supplies a development board and an ICE. rty-vendor tools include an HP ICE. Contact AT&T for refer-

☐ **SOFTWARE** AT&T sells development tools including a C compiler, assembler/linker, simulator, the VCOS operating system, and a library of multimedia functions.

DSP Group Oak/Pine

16-bit fixed-point DSP ASIC cor

☐ **OVERVIEW** DSP Group developed its own 16-bit DSP core architecture, called the Oak/Pine DSP, and licenses it to developers. Using one of the cores as a base, you can tailor your own DSP ASIC. Oak is DSP Group's second-generation 16-bit DSP core, following the Pine DSP core currently available at a number of ASIC vendors. Oak/Pine DSP processors are standard cells that are available in the ASIC libraries from many vendors. The cores use double-metal CMOS technology. Pine is available in 1.0-, 0.8-, and 0.6-μm processes; Oak is available in a 0.6-μm process. Pine and Oak both have built-in power-management features to cut power dissipation, including 3V parts to reduce power consumption further.

In high volume, Oak/Pine-based ASICs can cost less than $10 each. Both DSPs have been designed for ASIC development. They have an inner-core architecture and an expandable outer layer. Thus, engineers can make do with the minimal core or expand the architecture for higher processing efficiencies by adding more memory, peripherals, interrupt logic, and custom logic sections. Pine has two data buses and one program bus, two RAM data blocks for X, Y memory, an address generator, and a MAC unit. Oak expands on Pine by adding a barrel shifter, a bit-manipulation unit, two more accumulators, software stack, downloadab architecture, on-chip emulation, and an expanded instruction set.

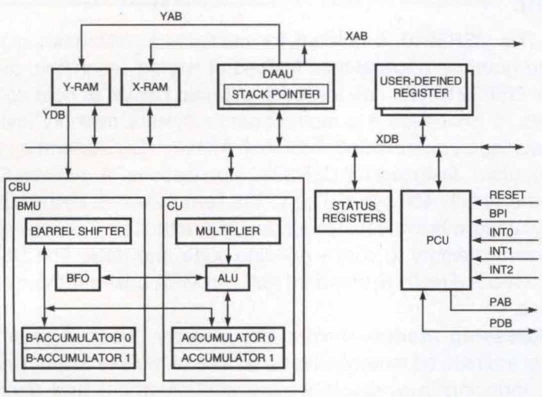
OAK DSP CORE

- 4-stage pipeline, 70 instructions
- 4 36-bit accumulators
- 9 16-bit general-purpose regs (4 optional user-defined regs)
- 2 2k data-RAM blocks, expandable to 64k
- ROM expandable to 64k
- 16×16-bit MPY, to 36-bit ALU
- 64k-word data, prog addr spaces
- Bit field operations
- Shadow reg/context switching
- 36-bit barrel shifter
- Viterbi accelerator
- On-chip emulation
- 4 external interrupts
- 80-MHz clock (2 per cycle)
- Static design, 3V operation
- Single-cycle MAC instruction
- Exponent evaluation in 1 cycl
- Divide step instruction
- Zero-overhead data addressin
- Program looping (4-level block repeat)
- Instruction repeat
- Software stack
- Wait-state support
- 2-cycle max interrupt latency
- Double-precision support

☐ **VENDOR CONTACT**

DSP Group Inc, Santa Clara, CA, (408) 986-4315. **Circle No. 4**

ARCHITECTURE



Oak has a double-level architecture: system and core. At the system level, the chip consists of a 16-bit Oak DSP core with links to on-chip program ROM, data RAM, and a bus-interface unit. At the core level, Oak is a compact DSP design with an X, Y data RAM block, data-arithmetic-address-generation unit (DAAU), a computational unit (CU) comprising a MAC unit, ALU with two 36-bit accumulators, and a bit-manipulation unit (BMU). The BMU adds a 36-bit barrel shifter and two additional 36-bit accumulators. The core also includes a software stack, program-control unit, four optional general-purpose registers, six interrupts, and a special on-chip-emulation module (OCEM), which provides trace and breakpoint capabilities for real-time debugging.

Oak's MAC unit has two 16-bit input registers; it takes in two 16-bit numbers, signed or unsigned, and delivers a 32-bit 2's-complement product in one cycle. The product is then sign-extended to 36 bits through a 4-bit extension nibble. The ALU performs arithmetic/logical operations on the data operands and functions such as normalization, step division, and rounding. The Oak's BMU has a 36-bit barrel shifter, a bit-field-operations unit (BFO), and two additional 36-bit accumulators with access to the accumulators of the CU. The accumulators can rapidly switch context between the two sets of accumulators, including the shadow registers. The accumulators can also evaluate 36-bit exponents.

Three main buses feed the DSP. At each cycle, they move X and Y memory data to the MAC unit from core X and Y data RAMs; the PCU fetches a new instruction from on-chip, external program ROM or RAM. The X data bus also serves as the main CPU data bus by linking the two data RAMs, status register, program-control unit, and a set of general-purpose registe

The DAAU generates X and Y memory addresses for each MA cycle, and does postoperation modification on the pointers, includi modulo addressing. It has nine 16-bit pointer registers for addressir The core has four general-purpose 16-bit registers including a top-stack pointer that references the top of the current software stack interrupt or subroutine-processing calls. You can define four additic general-purpose registers that are on the chip but not part of the D core. These registers can be handy for application-specific hardw

Oak supports DMA operation, downloading capabilities from memory space to program memory space, an automatic boot p dure, and support for two 64k-word address spaces: The X and Y space and the program space. The X RAM space can be in both i nal and external memory; the Y RAM space is in core internal me ry only. The X and Y memories can be expanded internally in the to 2k words, and the X memory expands externally to 62k words off-core program memory can expand to 64k words. Oak has a b 16-bit loop counter, which can repeat an instruction or block of ins tions up to 64k times. A repeat instruction can be nested in a loop with up to four levels of block nesting. Pine is a subset of Oak an all the architectural features of Oak except for the BMU. A harc stack replaces the software stack; the optional general-purpose ters expand to 8. Pine's instruction set is also a subset of Oak's.

Addressing modes—direct, register indirect, relative, and inc

Special instructions—conditional subroutine call/return fr subroutine, repeat next/block instructions, division step, com square, accumulate/subtract previous product, move data/pro memory, modify accumulator conditionally, support for double-p sion calculations, bit-field operations, exponent evaluation, co switching, min/max calculation, and automatic boot.

Part	Clock (MHz)	Mode	Max power (mA) at 5V	Price
Oak Core	80	Run Slow Stop	16 (3.3V) 1 (3.3V) 10 fA	N/S
Pine Core	50	Run Slow Stop	30 (5V) 5 (5V) 10 fA	N/S
	33	Run Slow Stop	14 (3.3V) 1 (3.3V) 10 fA	N/S

SUPPORT

☐ **HARDWARE** DSP Group supplies an ICE board and evaluation/development board and on-chip-emulation capabilities; the company also sells a bond-out chip for emulation and debugging.

☐ **SOFTWARE** Software tools for Oak include an assemb er, loader, simulator and debugger, a C compiler, and the ASS ulator, which enables users to map their customized logic into t All tools run under MS-Windows.

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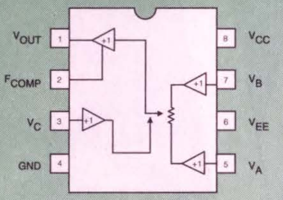

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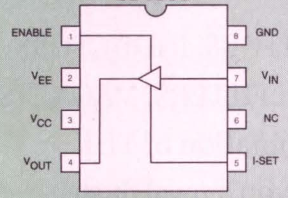

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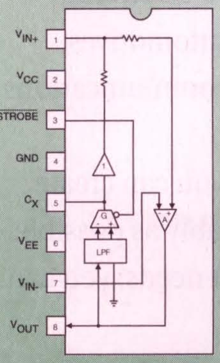

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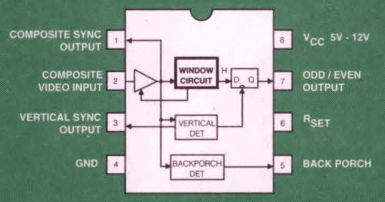

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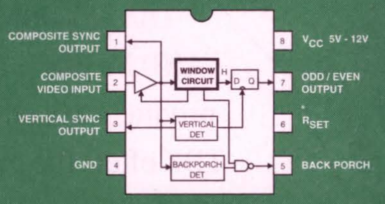

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- Replaces LM1881 For New Designs
- Industrial Temperature Range Available
- $2.50 in 100 unit quantities

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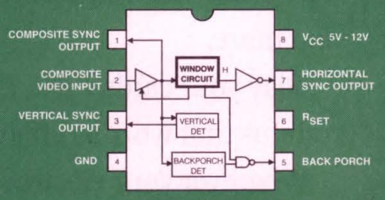

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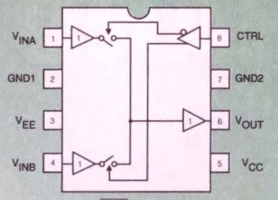

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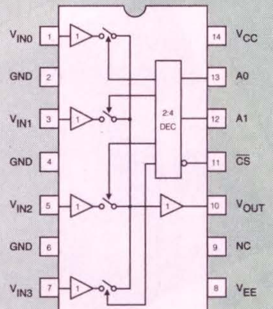

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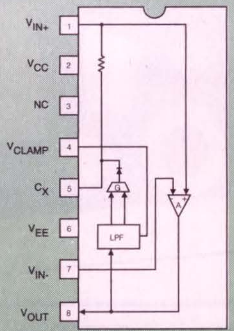

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CIRCLE NO. 47

Motorola DSP56100 Family

16-bit fixed-point DSP

☐ **OVERVIEW** Targeting digital-cellular and communications applications, Motorola engineers created the 16-bit DSP56100 family of DSP chips, which are downsized versions of the 24-bit fixed-point DSP56000. The DSP56100 builds on the basic DSP56000 architecture, adding a codec for D/A and A/D voice conversions for digital-cellular and voice communications. The DSP56156 suits the European cellular standards; the DSP56166 suits the emerging American and Japanese VSELP standards. To reduce silicon, the DSP56100 has two on-chip RAMs: 4 kbytes of program RAM and 4 kbytes of X memory SRAM. A program bus and X data memory bus serve these memories; each has an address and a data bus. Another bus, the global data bus, links the address-generator registers to external memory, peripherals, and a bit-manipulation functional unit. The chip's external bus is 16 bits.

A single-cycle (2-clock) MAC unit serves as the core for DSP processing. It has four 16-bit registers that hold MAC inputs and two 40-bit registers for accumulating results. You can repeat instructions or blocks of code for inner-loop processing. X values can be supplied from an on-chip X memory. The CPU can access memory with no penalty but requires fast SRAM. The DSP56100's address generator can deliver two addresses per instruction cycle. The address generator supports linear, modulo, and bit-reversed carry addressing. It has three sets of four registers that serve as address, offset, and ALU modification registers.

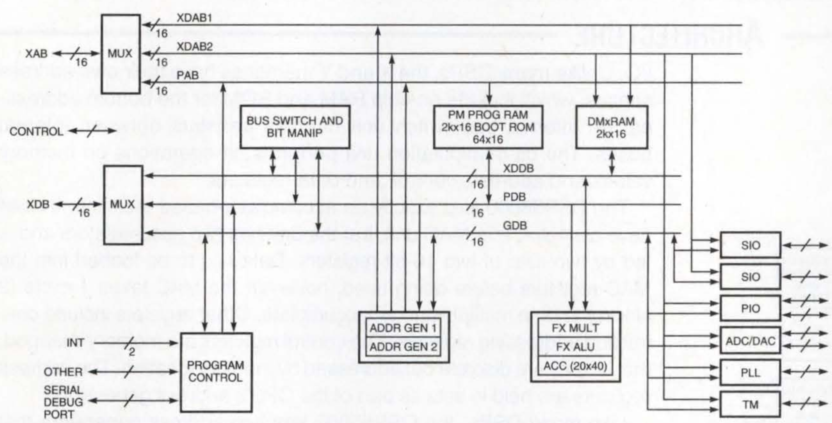
DSP56156

- 3-stage pipeline, 89 instructions
- 4-kbyte program RAM or 24-kbyte program ROM and 4-kbyte RAM
- 2 128-kbyte address spaces
- External bus: 16-bit address, data MAC: 4 16-bit input regs, 2 40-bit accumulators
- 1 address generator with 12 address regs
- Register-bit manipulation
- 14-bit sigma-delta codec
- 2 serial I/O ports
- On-chip ICE support (4 pins)
- 4 external interrupts, 8-bit host port
- 40/60 MHz (2 clocks/cycle), PLL
- 1-cycle most instr, NOP (pipelined)
- 1-cycle MAC (no pipeline)
- Address generator calculates 2 addr/cycle
- 21.6-μsec A/D conversion
- 1-cycle ext-mem R/W
- 2- to 3-cycle branch penalty
- Zero-overhead loops (DO, repeat)
- Indirect, modulo, bit-reversed addressing
- Stop instruction halts clock
- 161-nsec max interrupt latency

☐ **VENDOR CONTACTS**

Motorola Inc, DSP Div, Austin, TX, (512) 891-2030. **Circle No. 490**
DSP Helpline: (512) 891-3230. **BBS:** (512) 891-3771, 9600 (N,8,1).

ARCHITECTURE



Motorola's DSP56100 DSP processors are true 16-bit machines derived from the earlier DSP56000 family of 24-bit DSP chips. Designed for embedded-telecommunications applications, the DSP56100 delivers single-cycle MAC operation and offers hardware support for sum of products and vector processing. Like the DSP56000, the 56156/166 is partly an accumulator-based architecture and partly a register-based machine. The core MAC unit is accumulator-based (with two sets of two 16-bit input registers to hold incoming variables and coefficients) and two 40-bit accumulators to accumulate results. However, the address generator has 12 16-bit registers for sophisticated addressing and holding interim data values.

The 16-bit DSP architecture has three internal buses: a program address and data bus set, an X address and data bus set, and a global data bus. Processing centers around on-chip RAM and ROM. The DSP56156 has 4-kbyte program RAM and 4-kbyte X-memory data RAM as well as a 128-byte boot ROM. The 56166 has 4-kbyte program RAM, 8-kbyte X-memory data RAM, and a 128-byte boot ROM. For inner-loop MAC-type processing, first the code must be loaded into the program RAM. The X and Y data are fetched each cycle from X memory and external memory. Single-cycle inner-loop execution is possible as long as the code stays in the cache while external memory and the X-memory RAM furnish the MAC coefficients and variables for each cycle.

With a 60-MHz external clock and a 30-MHz basic pipeline cycle, a CPU memory fetch must take <33 nsec for single-cycle execution. The MAC unit has four input registers; these registers must be loaded on a previous cycle for the current MAC execution to complete in a single cycle. You can load a MAC input register in a MAC cycle that uses other registers.

The 16-bit external bus addresses two 64-kbyte address spaces—program and X memory. For MAC processing, portions of the X-memory space furnish the Y-memory values. The DSP56100 has two data-memory address buses—the XAB1 and XAB2—that fetch data from the X-memory RAM and from the external memory for Y-memory values. The processor also has an 8-bit host interface to link to a host processor and up to 25 I/O pins.

The DSP56100 DSPs have a stripped-down DSP56000 address generator with 16-bit (rather than 24-bit) paths and registers. Instead of the two address generators of the DSP56000 with two sets of ALUs and registers, the 16-bit DSP has only one address generator. However, the generator logic is fast enough to handle two address calculations per pipeline cycle. The address generator follows the DSP56000 family architecture and has address, offset, and modification registers that can be used for addressing as well as holding interim data. The address-generator registers are accessible via the global data bus.

Addressing modes—Register direct, address-register indirect (postincrement/decrement by 1 or offset indexed by offset). Special: immediate, short jump, absolute or I/O short address, implicit.

Debugging—The on-chip emulator port lets external hardware set breakpoints, single-step the CPU, and read/modify memory or registers. You can configure the chip to run with external RAM for development.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
DSP56156	60/40	Run Stop Wait	N/S N/S N/S	112-pin CQFP	\$46.10/ \$44.30
DSP56166	60	Run Stop Wait	100 11 0.4	112-pin CQFP	\$51.21

SUPPORT

☐ **HARDWARE** Motorola fields the Application Development System with ICE operation using the DSP's on-chip emulation features. Third-party tools are also available; contact Motorola for references.

☐ **SOFTWARE** Motorola supplies a Gnu C compiler and debugger, assembler/linker, and simulator. Third-party vendors supply data-acquisition and filter-design packages as well as operating-systems software. Contact Motorola for references.

Motorola DSP56000 Family

24-bit fixed-point DSP

☐ **OVERVIEW** Motorola came late to the DSP world; but instead of entering with just another 16-bit, fixed-point DSP, the company developed a 24-bit fixed-point DSP. Targeting audio and other applications that can take advantage of the larger data size, the DSP56000 filled a niche that has expanded with other vendors' 24-bit DSPs. The DSP56000 also takes advantage of Motorola's strengths as a leading µC and µP vendor. It melds a DSP processing core and multiple on-chip memories with a microprocessor central architecture and an external bus. The 56000 can access external memory each cycle without any penalties.

For peak performance, the CPU runs code from external memory and accesses on-chip X and Y data memories for MAC cycles. The DSP56000 family has multiple on-chip X and Y memories, a single-cycle MAC unit, and two address generators for zero-overhead X, Y addressing. It also has three independent execution units: a data-arithmetic unit, address-generation unit, and program controller. The MAC unit has dual 56-bit accumulators and four input-holding registers (two sets of two). The address generators each have three sets of eight registers for indirect addressing, address offset (add to address), and address modification.

Motorola has modified the DSP56000 for specific applications. These variations include a DSP with built-in ROM compending and sine tables (56001), a small-pin-out, cascadable chip (DSP56200), and a low-power chip for automotive audio (DSP56004). All DSP56000 chips (except the 56001) have on-chip emulation and a PLL. Motorola also sells a less-expensive, 16-bit DSP56100 family, the DSP56156/166, for lower-end applications.

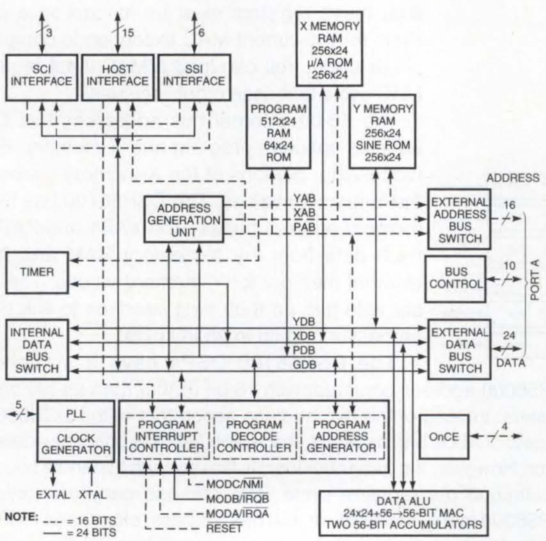
DSP56001

- 24-bit data, instr; 16-bit addr
- 62 instr, 3-stage pipeline
- 24×24-bit MPY, 56-bit accum
- 2 addr spaces: 192-kbyte prog, 304-kbyte data
- 2 addr generators, each has 3 sets of 8 addr regs
- Bit-manipulation unit operates on regs, memory
- External bus: 16-bit addr, 24-bit data
- 2 serial I/O ports
- 8-bit host-interface port
- On-chip emulation support
- 4 external interrupts
- 83/40-MHz clock (2 clocks/cycle)
- 15-level system stack
- 1-cycle MAC (not pipelined)
- 1-cycle instr execution (pipelined)
- 2- to 3-cycle branch/jump, branch penalty
- DO LOOP instr (repeat blocks); STOP instr halts clock
- 1-cycle external-memory R/W
- Indirect, modulo, bit-reversed addressing
- 112.5-nsec max interrupt latency

☐ **VENDOR CONTACTS**

Motorola Inc, DSP Div, Austin, TX, (512) 891-2030. **Circle No. 491**
DSP BBS: (512) 891-3771, 8N1, to 9600 bps.

ARCHITECTURE



Introduced in 1986, the 24-bit fixed-point DSP56000 had the luxury of smaller silicon processes and increased silicon budgets. The Motorola engineers who designed the processor integrated µC buses and architectural concepts with a DSP MAC core and X and Y memory blocks. Thus, unlike many early fixed-point DSPs, the DSP56000 has a versatile external memory bus, standard bit-manipulation capabilities, and the ability to execute directly from external memory with single-cycle accesses. The chip has no on-chip program ROM, except for a small boot ROM on some versions.

The processor combines 16-bit addressing with 24-bit words. It has three internal address/data bus pairs: X, Y, and program. A fourth bus—the global data bus—is a simple 24-bit logic bus. Any of the internal address and data buses can be switched into the external 16-bit address and 24-bit data bus; external devices can access internal memory via a bus request. The DSP56000 supports four 64-kbyte address spaces—one each for X memory, Y memory, program, and I/O. Unlike many DSPs, the X and Y memories have their own address spaces, which include on-chip RAM and ROM for the bottom addresses. An internal bus-switch unit handles transfers between internal buses. The bit-manipulation unit performs bit operations on memory values and address, control, and data registers.

The DSP56000 isn't exactly an accumulator-based machine. It does have a single-cycle MAC unit, but the unit has two accumulators and is fed by two sets of two 16-bit registers. Data has to be loaded into the MAC registers before being used; however, the MAC takes 1 cycle (2 clocks) to do a multiply and an accumulate. Other registers include control and addressing registers. The control registers are memory-mapped; that is, they are discrete but addressed by memory location. The address registers are held in sets as part of the CPU's address generators.

Like many DSPs, the DSP56000 has two address generators that automatically access the X and Y memories for MAC cycles. Each hardware generator has an ALU and three sets of four registers: one set for base address registers, one set of offset registers, and one set of modifier registers. The modifier registers can specify the type of address-register arithmetic operation or they can hold data. These register sets and the ALUs let you do complex addressing, including register indirect and postincrement/decrement indexes.

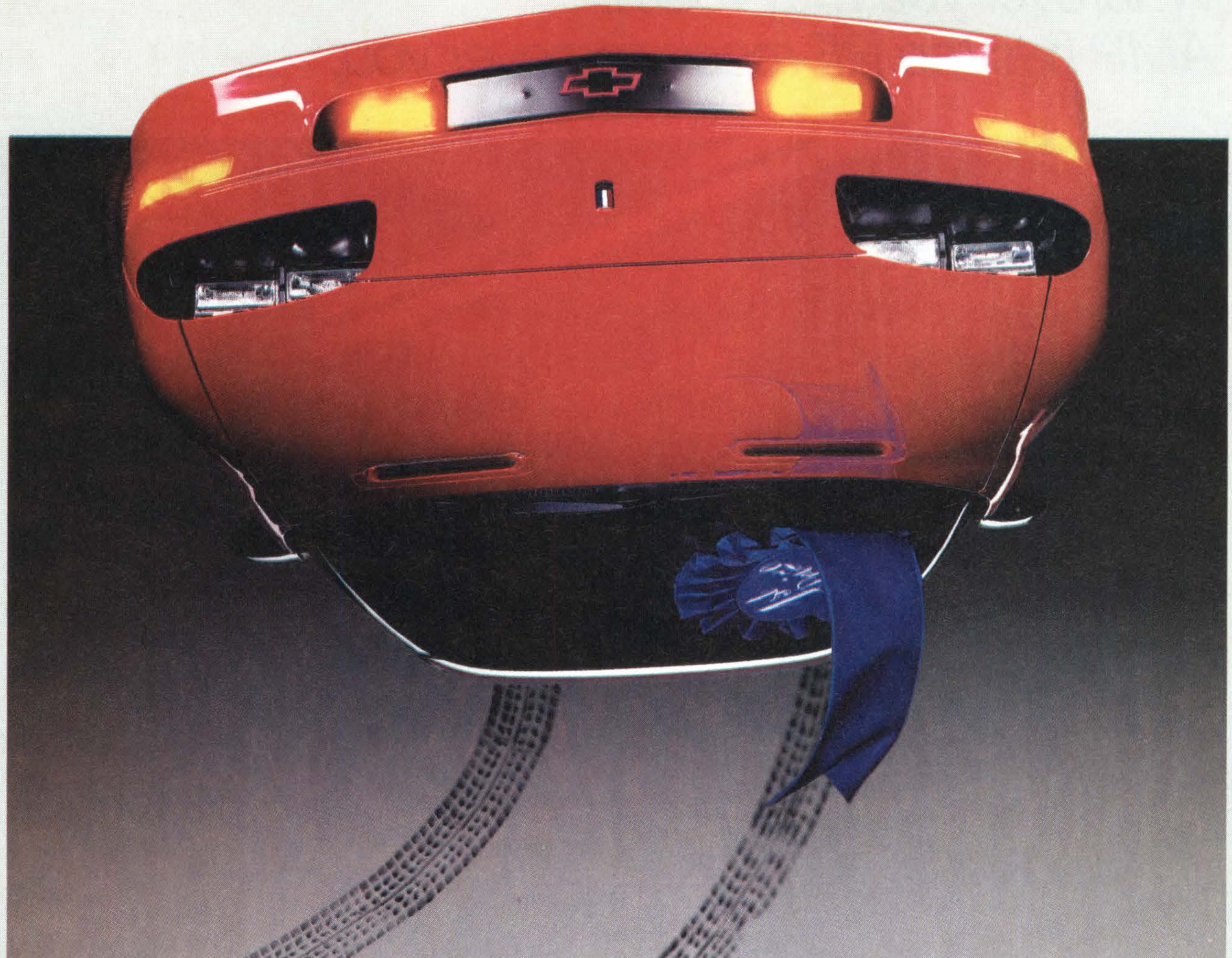
Special instructions—DO/EndDO, repeat, bit test and change, compare, divide iteration, jump if bit clear/set, jump to subroutine conditionally, move program memory.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
DSP56001	33/27	Run Stop Wait	185 2 25	132-pin PQFP	$30/$25
DSP56002	40/66	Run Stop Wait	95 (typ) 2 (typ) 10 (typ)	132-pin PQFP	$39.80/ $43.80
DSP56004	40	Run Stop Wait	95 (typ) 2 (typ) 15 (typ)	80-pin PQFP	$36.60
DSP56L002	40	Run Stop Wait	50 (3.3V) 2.2 (3.3V) 4.4 (3.3V)	132-pin PQFP	$46.20

SUPPORT

☐ **HARDWARE** Motorola's Application Development System offers a 20.48-MHz clock and ICE operation using the 56000's on-chip emulation features. Third-party hardware tools are available; contact Motorola for references.

☐ **SOFTWARE** Motorola supplies a Gnu C compiler and debugger, assembler/linker, and a simulator. Third-party vendors supply data-acquisition and filter-design packages as well as operating-system software. Contact Motorola for references.



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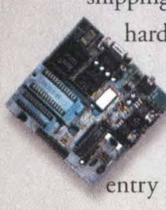

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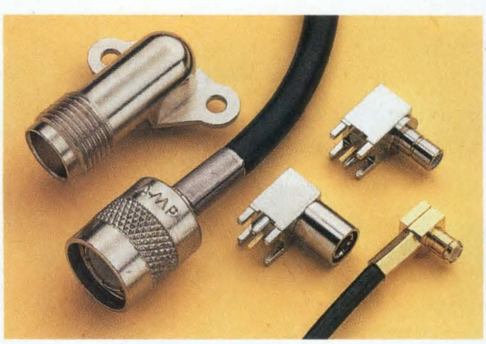

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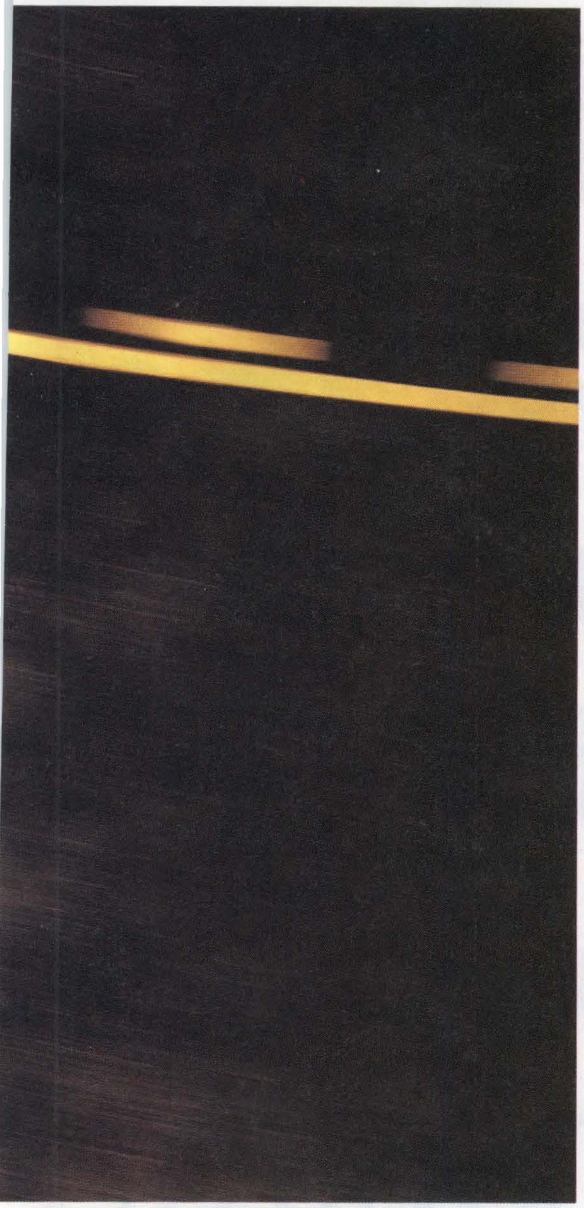


Motorola DSP96002

32-bit floating-point DSP

☐ **OVERVIEW** Motorola's 32-bit DSP96002 has found a home in high-end DSP and military sockets. Its external buses allow designers to cobble together multiprocessor systems. Basically a 32-bit floating-point extension of the 24-bit fixed-point DSP56000, the DSP96002 has five major internal buses to speed multiple-operation processing. These buses include the DSP56000's program, X-memory, and Y-memory bus sets and the global data bus. The DSP96002 has a DMA bus that supports two DMA channels. An on-chip DMA controller moves data without CPU assistance. The DSP96002 also has two 32-bit external bus systems. These buses can access or share external memory or link multiple DSP96002s in a multiprocessor configuration.

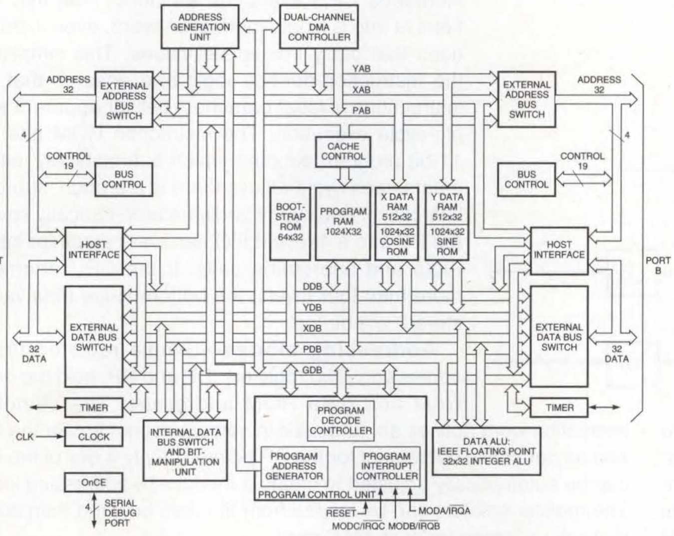
The floating-point processor presents a programming model nearly identical to that of the earlier 24-bit DSP56000 fixed-point processor. Motorola engineers extended the instruction set with floating-point instructions and extended the registers (including addressing registers) from 16 to 32 bits. The DSP floating-point data unit is built around a register file of 10 96-bit registers. The data ALU includes a separate floating-point/integer adder; format-converter logic for front-ending the register fills; and cascaded logic, divide, and square root/multiplier units. These units support integer operations as well as floating-point operations with 11-bit exponents and 32-bit mantissas. The DSP96002 meets the IEEE standards for single- and double-precision floating-point representations.

DSP96002

- ▶ 9-stage pipeline, 133 instructions
- ▶ Reg file: 10 96-bit regs, 24 32-bit address registers
- ▶ 96-bit accumulator, IEEE 754
- ▶ 2 2-kbyte RAM blocks
- ▶ 4-kbyte programmable RAM
- ▶ 2 preprogrammed data ROMs
- ▶ 5 internal 32-bit buses
- ▶ 2 external 32-bit memory buses
- ▶ 1 to 3 selectable address spaces
- ▶ 2 DMA channels, 1 serial port
- ▶ On-chip ICE support
- ▶ 3 external interrupts
- ▶ 33/40-MHz clock (2 clocks/cycle)
- ▶ Address generator calculates 2 addr/cycle
- ▶ 1-cycle MAC, instruction execution
- ▶ 200-nsec FP DIV (60 MHz)
- ▶ Parallel ALU, bit-logic, MAC ops
- ▶ Zero-overhead loops
- ▶ 1- to 3-cycle branch penalty
- ▶ Indirect, modulo, bit-reversed addressing
- ▶ 1-cycle off-chip fetch
- ▶ STOP instr halts clock
- ▶ 6-instruction max interrupt latency

☐ **VENDOR CONTACT** **Motorola Inc**, DSP Div, Austin, TX, (512) 891-2030. **DSP BBS:** (512) 891-3771, 8N1, to 9600 bps. **Circle No. 492**

ARCHITECTURE



The DSP96002 is a third-generation, 32-bit floating-point DSP processor. It has a complex, performance-oriented architecture. Features include on-chip program, X, and Y memories; five internal buses for concurrent processing; and a register-based (rather than accumulator-based) architecture. Additionally, the DSP96002 has two 32-bit external-memory interfaces with separate address and data buses. These external interfaces have built-in multimaster capability. Another DSP96002 or a host processor can use a bus request to take over the bus and use it to access shared external memory or the DSP96002's internal memory.

The DSP96002 is a 32-bit floating-point extension of the 24-bit fixed-point DSP56000 architecture. It has the same internal bus sets: address and data buses for program, X memory, and Y memory. It also has two logical buses: the global data bus (from the DSP56000) for transferring address and local data, and the DMA bus for moving data without disrupting the DSP CPU's instruction thread. The DSP96002 has a 3-stage pipeline.

Unlike the DSP56000, the DSP96002 has on-chip program memory—4 kbytes of static RAM. It also has a boot ROM. Like the DSP56000, it has X and Y RAM and ROM blocks to supply the coefficients and variables for sum-of-product MAC calculations. MAC operations take input data from a 10-register (96-bit-wide), multiported register file. So although MAC operations are not pipelined, the X, Y data accesses must be pipelined to pump data into the register file before the downstream MAC operation uses the data. The data ALU block includes multiply, adder, logic, divide, and square-root units. The adder unit can operate in parallel with the logic, divide, square-root, and multiplier units. The adder has a parallel adder and subtracter (handles both add and subtract for FFT calculations) and a barrel shifter and normalizer. It produces a 32-bit value or an IEEE single-precision (24-bit mantissa) value.

The DSP96002 has basically the same address-generation unit as the earlier DSP56000. This unit consists of two address generators that can operate concurrently. The generators each have three sets of four 32-bit registers: address (address pointers), offset (offset values), and modify registers. These registers are loaded and accessed via the global data bus. The DSP96002 has a flexible architecture; many typically hard-wired features are available as programmable options that you can set up via control registers. For example, the DSP chip supports a mix of address spaces ranging from a single unified address space to one that has separate 32-bit spaces for X, Y, and program memory.

Addressing modes—Register direct, address-register indirect (postincrement/decrement by 1 or offset, indexed by offset). Special modes: immediate, short jump, absolute/I/O short address, implicit.

Debugging—The on-chip emulator port lets external hardware set breakpoints, single-step the CPU, and read/modify memory or registers. You can configure the chip to run with external RAM for development.

Special instructions—DO/End DO, repeat, bit test and change, compare, graphics compare, divide iteration, jump if bit clear/set, jump to subroutine conditionally, conditional ALU operation, move program memory.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
DSP96002	33.3/40	Run Wait Stop	300 (typ) 10 (typ) 0.1 (typ)	223-pin PGA	$143.90/ $172.70

SUPPORT

☐ **HARDWARE** Motorola sells the Applications Development Module for evaluating and debugging the DSP96002. The module uses the processor's on-chip emulation support for ICE-like debugging. Some third-party tools are available; contact Motorola for references.

☐ **SOFTWARE** Motorola supplies a Gnu C compiler and tools and an assembler/linker, librarian, application library, and behavioral simulator. Third-party tools include C and Ada compilers, graphical development systems, filter-design software, and real-time operating systems. Contact Motorola for references.

NEC µPD77C25

16-bit fixed-point DSP

☐ **OVERVIEW** The µPD77C25 is NEC's second 16-bit fixed-point DSP chip, following the µPD7720. The C25 is a CMOS part that doubles performance but is pin- and upward-code-compatible with the older chip. Both DSPs have an accumulator-based architecture and run from on-chip program and data memory. The C25 has 2048 24-bit instruction words and two data blocks to hold MAC inputs—512 bytes of data RAM and 2048 bytes of data ROM. Program and data ROM are also available as EPROM or OTP memory. The µPD77C25 handles pipelined, single-cycle MAC operations with a 16×16-bit multiply and a 16-bit accumulate.

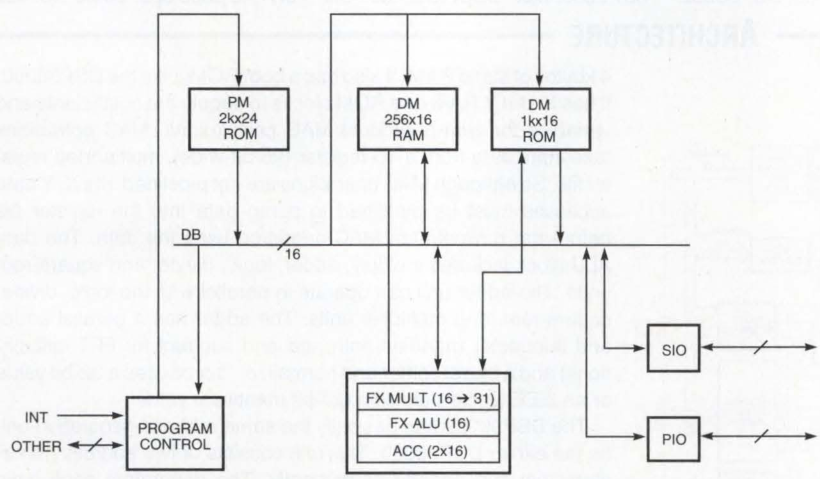
The µPD77C25 can run in stand-alone mode or in conjunction with a host processor. It has an 8-bit parallel I/O host port for exchanging data or DSP status with a host processor. This port can interface with standard µC buses such as the 8080, 8085, and 8086 and can handle 8-bit or double-buffered 16-bit data transfers. The µP77C25 also has two serial ports, which can interface to serial peripherals such as ADCs, DACs, codecs, and other µPD77C25 DSPs. You can configure the serial ports for single- or double-byte transfers.

µPD77C25

- 24-bit instruction, 16-bit data
- 4 instruction types, 98 instructions
- 2 16-bit accumulators
- 2k×24-bit program ROM/EPROM/OTP
- 2-kbyte data ROM/EPROM/OTP
- 512-byte data RAM
- 16-bit ALU/accumulator
- 2 internal data buses
- 4-level hardware stack
- 2 serial 8-bit I/O ports
- 2 I/O pins, 1 external interrupt
- 8/10-MHz clock
- All instructions 1 word
- 1-cycle MAC, MPY-SUB (pipelined)
- 16×16-bit MPY, 31-bit result
- 122-nsec ADD; 100-nsec NOP
- Auto increment/decrement for data-RAM pointer
- Auto increment for data-ROM pointer
- DMA support for 8-bit parallel I/O port
- 4-MHz serial I/O
- 2-cycle max interrupt latency

☐ **VENDOR CONTACT**
NEC Electronics Inc, Mountain View, CA, (800) 366-9782.
Circle No. 493

ARCHITECTURE



The µPD77C25 is a classical accumulator-based architecture built around a pipelined MAC core. It has three on-chip memories: one program and one data ROM/EPROM/OTP-memory block and a data-RAM block. The CPU can fetch two values per cycle to fill the multiplier input registers while getting the next instruction. The DSP has one 16-bit data bus that links to all memories and peripherals. For MAC data fetches, the RAM bypasses the data bus and directly feeds one of the MAC inputs. The data bus feeds the other MAC input, which passes data from the data ROM/EPROM/OTP-memory block.

The MAC unit is pipelined; the multiplier and accumulator-adder run in parallel. A multiply-accumulate takes two clock cycles: one for the 16-bit multiply and another for the product to be added to the accumulated result. The multiplier produces a 31-bit signed word, which is held in two 16-bit registers. The 16-bit-wide adder circuit has two 16-bit accumulators; you can keep two 16-bit running sums or a 32-bit sum that takes two passes through the adder. The multiplier is registered; each input is loaded into a register before passing though the unit's Booth multiplier. The resulting products are also registered. The accumulator ALU has two accumulators; an input from one accumulator can shift on its way to the ALU.

The µPD77C25 has a 24-bit instruction word and a 16-bit data word. The wider instruction word increases CPU execution efficiency—all instructions fit into a single instruction word, even instructions that carry immediate values. This simplifies the instruction-decode logic and ensures that all instructions (except branches) deliver apparent single-cycle execution. The instruction ROM has an 11-bit program counter, which automatically increments each cycle unless there is a branch, subroutine call, or interrupt. Hardware automatically saves the PC into a 4-level LIFO hardware stack for interrupts and subroutine calls. If the CPU attempts more than four levels, the bottom value (first value stored) will be lost.

Addressing modes—Simple register-direct addressing. Two registers, DP and RP, hold the data RAM and data ROM addresses. The complex instruction word defines an automatic increment/decrement for the DP and an automatic decrement for the RP pointers. Only 4 bits of the DP can be automatically adjusted to create a modulo-16 addressing loop. The register pointers can be loaded from the data bus and then automatically adjusted for each MAC cycle.

Numeric representations—The multiplier multiplies the 2's-complement of two 16-bit data words. The result is 30 bits of data and 1 sign bit and is left justified with a 0 LSB. The 16-bit accumulators require two passes for a 31-bit accumulate.

Special instructions—Accumulator decrement/increment, 8-bit exchange, 1's-complement the accumulator (no divide instruction).

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (10,000)
µPD77C25	8	50	44-lead PLCC	$12.90
	8	50	28-pin PDIP	$8.70
	8	50	28-pin SOP	$12.00
	10	50	28-pin DIP	$10.20
µPD77C25	8	60	28-pin PDIP (OTP version)	$56.20
	8	60	28-pin PDIP (EPROM version)	$101.55

SUPPORT

☐ **HARDWARE** An evaluation board, EVAKIT-77C25, is available from NEC. It can also function as a limited ICE by plugging directly into the target-system DSP socket. The evaluation board with an adapter also plugs into standard PROM burners to program versions with EPROM or OTP memory.

☐ **SOFTWARE** No C compiler is available for the 77C20. NEC supplies an assembler-linker-loader package, and a third-party simulator is also available.

NEC μPD77017

16-bit fixed-point DSP

☐ **OVERVIEW** Introduced this year, NEC's μPD77017 targets 16-bit digital-cellular, voice, and fax-modem applications. The 16-bit fixed-point processor is the most recent of the NEC DSP offerings. It has many of the features of third-generation DSP architectures such as separate on-chip X and Y data RAMs, each with its own address generator and two sets of four address-pointer and index registers. The core execution unit consists of three 40-bit functional units—a multiplier, ALU, and barrel shifter. The μPD77017 has a set of eight 40-bit, general-purpose register/accumulators and three internal buses to minimize conflicts when moving multiple data in a single cycle. The DSP delivers apparent single-cycle (pipelined) instruction execution. The MAC unit is pipelined as well and takes one cycle.

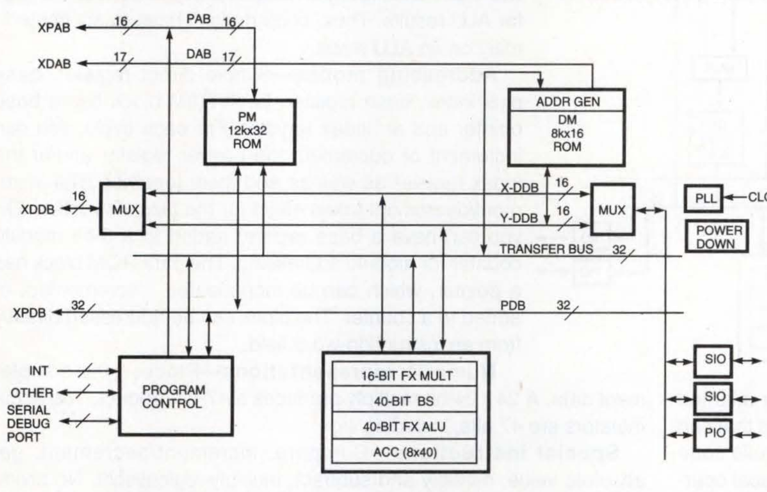
The μPD77017 has 16-bit data words, 32-bit instruction words, and 12k words in on-chip code ROM and 256 words of on-chip code RAM. It has dual external-memory ports—one for 16-bit data and one for 32-bit programs—with two distinct 16k-word address spaces for data. Memory read/write accesses can take a single cycle, although instruction pipelining may require an extra cycle for some instructions. An on-chip wait-state generator lets the processor run with slower, less-expensive memory. Like many of NEC's DSPs, the 77017 has an 8-bit host I/O port, which enables a host μP to exchange data with the DSP.

μPD77017

- 3V operation
- 32-bit instruction, 16-bit data
- 3-stage pipeline, 81 instructions
- 8 40-bit reg/accumulators
- 40-bit MPY, ALU, barrel shifter
- 2 2-kbyte data-RAM blocks
- 12k×32-bit program ROM
- 256×32-bit program RAM
- 3 internal buses
- 1 external-memory bus
- 15-level hardware stack
- 2 serial I/O ports
- 8-bit host I/O port with DMA
- 4 external interrupts, 5-pin JTAG
- 33/16.5/8.25/4.125-MHz clock (2 clocks/cycle)
- 1-cycle pipelined execution
- 1-cycle MAC
- Zero-overhead nested looping; program-loop control, data address generators
- Data: modulo, bit-reversed addressing; auto increment /decrement
- 4-level loop stack
- 2-cycle interrupt latency; repeat takes 2+n cycles
- DC to 16-Mbps serial I/O
- Power-down mode
- Built-in PLL

☐ **VENDOR CONTACT**
NEC Electronics Inc, Mountain View, CA, (800) 366-9782.
Circle No. 494

ARCHITECTURE



A third-generation DSP processor, the 16-bit fixed-point μPD77017 combines a number of architectural features to ensure fast, single-cycle MAC execution. These features include three internal buses for X data, Y data, and transfer buses; separate X and Y memories, each with its own dedicated address generator; a MAC unit; and eight general-purpose 40-bit register/accumulators. The 77017 is a 16-bit processor with a wider 32-bit instruction word to minimize instruction-decoding logic and increase code efficiency.

The 77017 neatly partitions into two major processor sections and a peripheral set. The main sections are the data unit and the program unit. The data unit contains the X and Y memory units, each of which has an address unit, register file, and MAC-execution unit. The program unit contains the instruction-address unit with built-in loop control, interrupt-control logic, 12k words of program memory, and instruction-decode/control logic. A main bus, the transfer bus, links the two main units. Each main unit connects to an external data-memory interface: 14-bit addresses and data for the data unit.

The data unit's MAC has three 40-bit parallel subunits: a multiplier/ALU, an ALU, and a barrel shifter. Unlike many DSP implementations, the MAC subunits do not have dedicated input and output registers. Instead, the MAC is tightly integrated with a set of eight general-purpose registers. The X, Y, and transfer buses push data into the general register set; the general register set provides the data to drive the individual MAC subunits, which can execute concurrently. In effect, the general register set, which is basically a multiport register file, serves as the interchange that links the data side of the processor to the execution side. The basic MAC operation executes in a single clock cycle.

Two 2-kbyte ROM data-memory banks supply the X and Y data components for each MAC cycle. Each bank has its own address generator with a set of four address-pointer registers, supplemented by four index registers and a modulo register. A special bit-reverse circuit handles bit-reversed addressing for each bank. On the program side, the DSP has a 12k-word (32-bit) instruction ROM and 256-word instruction RAM. The RAM has to be directly loaded under program control. To speed instruction execution, the DSP has a 15-level hardware PC stack that pushes and pops the PC for interrupts and subroutine calls and returns. Additionally, the DSP hardware supports automatic looping with a 4-level loop stack that lets code nest so it can loop under hardware control.

The X and Y address units each have two sets of four 16-bit registers, which serve as address pointers and modification registers. Each unit also has an index-register link to the main data bus. Through this bus, code can load and modify the pointer and modification registers. Each unit also has a modulo register for modulo index addressing.

Addressing modes—Direct, register, addressing, immediate. Hardware supports modulo and bit-reversed addressing for each data memory.

Special instructions—Conditional operations (minimize jumps), multiply-subtract, 1-bit shift-multiply-add, 16-bit multiply-add, increment/decrement, clip, exponent, absolute value, register-indirect subroutine call, register-indirect jump, loop, repeat, loop pop.

Part no.	Clock (MHz)	Mode	Max power (mA at 3V)	Pins, package	Price (10,000)
μPD77017	33	Run	170	100-pin TQFP	$32

SUPPORT

☐ **HARDWARE** NEC supplies a PC-based plug-in development board that offers in-circuit emulation using the 77017's on-chip emulation features. The board plugs into the PC/AT bus and links to the target board via a 6-pin connector that connects to the 77017's on-chip ICE logic.

☐ **SOFTWARE** NEC has MS-Windows-based development tools that include a simulator, relocatable assembler, librarian, linker, and a viewer for displaying error and assembly listings. (A C compiler will be available soon.)

NEC μPD77220

24-bit fixed-point DSP

☐ **OVERVIEW** Introduced in 1986, the 24-bit fixed-point DSP μPD77220 fits between NEC's 16- and 32-bit architectures. It is a second cousin to the 16-bit DSPs and a reduced version of the 32-bit μPD77240. The instruction set and coding resemble that of the 16-bit DSPs; the register-based architecture reflects that of the later 32-bit DSP. And like its older 32-bit brother, the 77220 has provisions for a close coupling with a host processor as well as the capability to use external memory for both data and code.

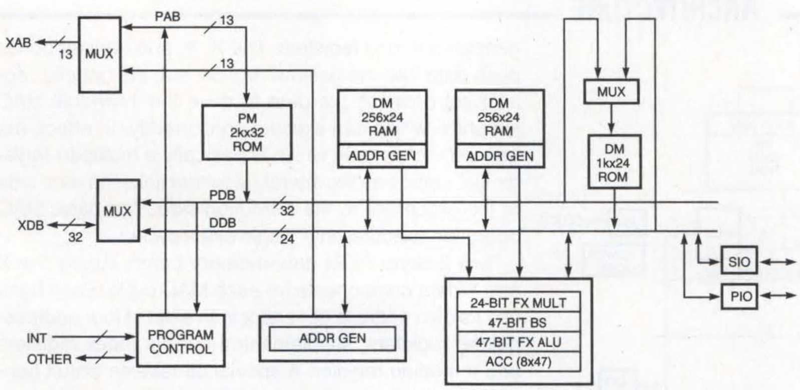
The μPD77220 has a complex architecture. In the NEC tradition, it uses an instruction word that is wider than its data word—32-bit instructions and 24-bit data. It has a single, 24-bit main data bus with hardware bypasses to ensure parallel data accesses for feeding the core MAC unit. The MAC unit has a parallel 47-bit multiplier and 47-bit ALU. The ALU has eight general-purpose register/accumulators. These registers can be used to accumulate results or as holders for interim program values. The data RAM and ROM blocks have their own built-in address generators and pointer registers to speed processing. An 8-level hardware stack automatically holds PC values for interrupts and subroutine calls. The hardware has two PSWs (program status words), which can be dynamically selected by a bit in each instruction.

μPD77220

- 32-bit instruction, 24-bit data
- 3-stage pipeline, 51 instructions
- 8 47-bit accumulators
- 2k×24-bit program ROM/EPROM
- 2 768-byte data RAM blocks
- 3-kbyte data ROM block
- 16-bit host port (slave mode)
- External-memory interface: 13-bit address, 32-bit data
- 4 I/O pins, 2 external interrupts
- 8/10-MHz clock (2 clocks/cycle)
- All instructions 32-bit words
- 100-nsec ADD, NOP (10 MHz)
- 1-cycle MAC, MPY-SUB (pipelined)
- 10-bit loop counter
- Data pointers: autoincrement/decrement, base+pointer, modulo addressing
- 8-level hardware stack
- 4-MHz max serial I/O
- 3-cycle max interrupt latency

☐ **VENDOR CONTACT**
NEC Electronics Inc, Mountain View, CA, (800) 366-9782.
Circle No. 495

ARCHITECTURE



NEC's 24-bit, fixed-point μPD77220 DSP has a register-oriented architecture with eight general-purpose register/accumulators that can hold values or accumulate results. Complex instructions enable code to operate on these registers for addressing or arithmetic/logical operations. The core of the processor consists of three RAM and ROM data blocks that feed a registered multiplier and ALU units each cycle. A MAC operation takes two cycles—one for the multiply and one for accumulating the multiplication result.

The 77220 takes a hard-wired approach to accessing and moving data to the DSP multiplier and ALU. It has a single 24-bit data bus that links all the major elements together. For fast MAC processing, the bus is bypassed with hard-wired paths to move data in parallel. Each of the data RAM and ROM blocks has its own attached address-generator logic. The two 768-byte data RAMs have a base pointer and index register that are directed by fields in each instruction word. The data ROM has an address register and a modulo counter; it can also be addressed directly from the instruction word.

The 77220 has a built-in 10-bit loop counter, which can be loaded, read, and decremented. When the counter decrements past 0, it generates a borrow, which causes the hardware to substitute a NOP for the next instruction. A decrement that passes through 0 will skip the jump instruction, typically a jump that loops back to the top of the block; this skip will fall through and terminate the loop.

The DSP has an 8-level hardware stack that pushes the PC on a LIFO basis for interrupts and subroutine calls. On returns, the PC values are popped off the stack into the PC. The hardware also maintains two 4-bit PSWs (program status words) that hold the flags for ALU results. Thus, code doesn't have to act immediately on an ALU result.

Addressing modes—Simple direct register, base plus index, base register. Each RAM block has a base pointer and an index register. For each cycle, you can increment or decrement the pointer register and/or the index register as well as add them together. The increment/decrement takes effect for the next instruction. Or, you can have a base register added to a 9-bit modulo counter for modulo addressing. The data ROM block has a pointer, which can be incremented, decremented, or added to a counter. The block can be addressed directly from an instruction-word field.

Numeric representations—Process 2's-complement data. A 24×24-bit multiply produces a 47-bit product. The accumulators are 47 bits, including sign.

Special instructions—Compare, increment/decrement, get absolute value, multiply and subtract, multiply-logical/shift. No divide instruction.

☐ **PERIPHERALS**

Slave mode—The 77220 has two hard-wired modes: slave mode and master mode. In slave mode, the DSP is slaved to a host processor. This mode maintains a 16-bit data port through an internal register. The host can write to this register or read from it. The DSP can transfer data between this register and RAM or any internal register. The host processor cannot take command of the slaved DSP CPU; it can only send or receive data through the port. In slave mode, the DSP can drive a general-purpose set of I/O pins and a limited external memory. The I/O pins comprise two output pins and two input pins. The 8-bit external-memory interface has a 13-bit address bus. Up to 8 kbytes of external memory can be used for data storage.

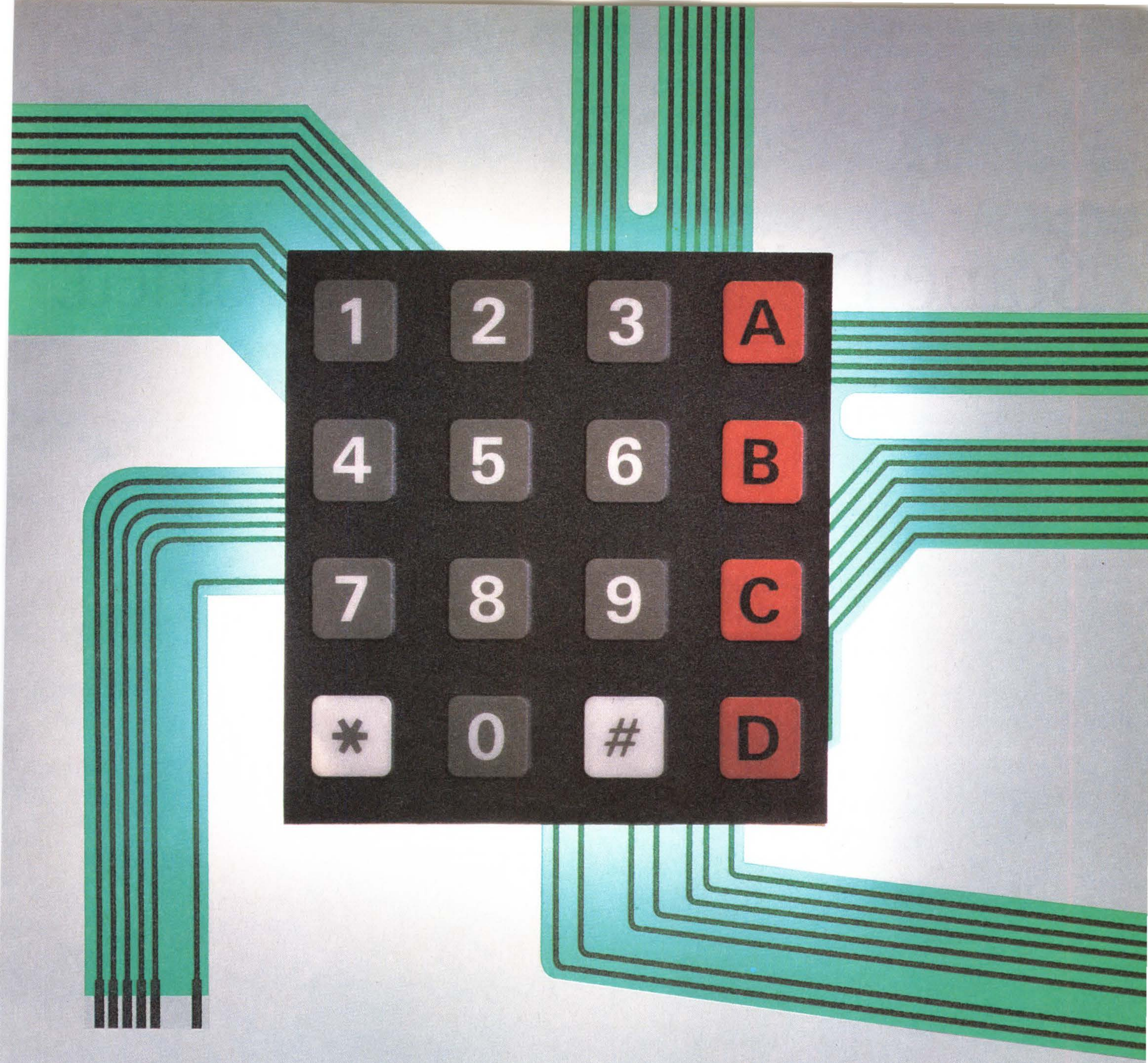
Master mode—In master mode, the DSP has no provision for direct interfacing to a host processor. Instead, the CPU supports up to 8 kbytes of 32-bit-wide external memory; 4 kbytes can be data, 4 kbytes code.

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (10,000)
μPD77220L	8 10	200 200	68-lead PLCC	\$32 \$38
μPD77220R	8 10	200 200	68-pin PGA	\$52 \$55

SUPPORT

☐ **HARDWARE** NEC supplies an evaluation board with 8-kbyte external program memory, 8-kbyte external data memory, and an 8-kHz analog front end. A stand-alone emulator is also available.

☐ **SOFTWARE** NEC has a relocatable assembler/linker/loader package for the 77220. It also has a window-oriented simulator for analyzing code and timing.



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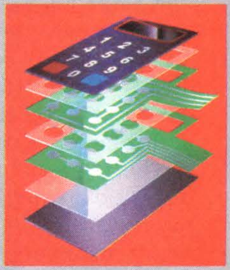

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CIRCLE NO. 110

SGS-Thomson ST18 Family

16-bit fixed-point DSP

☐ OVERVIEW The ST18950 is a general-purpose, programmable 16-bit, fixed-point DSP core. The ST18950 can be embedded as a megafunction in a gate array or cell-based device that has a 0.5-µm library containing RAM, ROM, and PLAs. By simply adding optional peripherals (IT controller, DMA controller, bus-switch control unit, etc) and memory for data and instruction, you can customize a powerful application-specific digital-signal processor (ASDSP) around the ST18950 DSP core. A key to the ST18950's performance is its high degree of parallelism, which allows the ST18950 to simultaneously perform multicycle functions along with other processors.

The ST18950's built-in 0.5-µm, triple-level-metal CMOS technology includes an arithmetic data-calculation unit (DCU), a program-control unit (PCU), and an address-calculation unit (ACU). The chip has up to 64k×16-bit (program) and 128k×16-bit (data) memory. An emulation and test unit (ETU) helps you implement and test ASDSPs built around the ST18950.

☐ VENDOR CONTACT

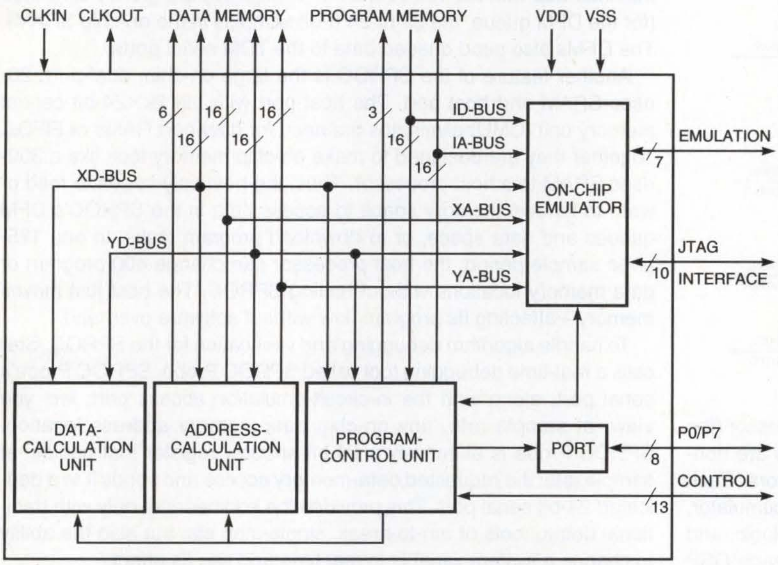
SGS-Thomson Microelectronics Inc, Phoenix, AZ, (602) 867-6100.

Circle No. 496

ST18950

- ► 40 MIPS/25-nsec instruction-cycle time
- ► Harvard architecture
- ► 2 64k×16-bit data memories
- ► 64k×16-bit program memory
- ► 16×16-bit parallel multiplier
- ► 40-bit barrel shifter unit
- ► 40-bit ALU (40-bit math operations)
- ► 2 40-bit extended precision accumulators
- ► Fractional and integer arithmetic (for floating-point)
- ► Bit manipulation
- ► Immediate and computed branches and subroutines
- ► No overhead nested hardware loops
- ► 1 interrupt pin and interface to interrupt-controller peripheral
- ► Bootstrap loading
- ► Stack in data memory
- ► 2 address-calculation units with modulo and bit-reverse capability
- ► General-purpose 8-bit I/O port
- ► Dedicated hardware for emulation and test; IEEE 1149.1 (JTAG) compatible
- ► Coprocessor interface and coprocessor-dedicated instructions
- ► Operation to dc
- ► Single 3.3V power supply
- ► Low-power standby mode

ARCHITECTURE



The SGS-Thomson ST18950 DSP architecture has four main components: a data-calculation unit (DCU), address-calculation unit (ACU), program-control unit (PCU), and emulation-and-test unit (ETU). These units are organized in a Harvard architecture around three bidirectional 16-bit buses—two for data (XD/YD) and one for instruction (ID); each bus is dedicated to a unidirectional 16-bit address bus (XA/YA/IA). Data memory (RAM and ROM) and registers map on to the external data buses (XD/YD and XA/YA). Access to program RAM and ROM is via the instruction bus (ID/IA); data and instruction buses share the same bus-control interface (RD/WR/BS).

Depending on the calculation mode, the ST18950 DCU computes operands, which can be 16- or 32-bit, signed or unsigned. The chip includes a 16×16-bit parallel multiplier to implement MAC-based functions (1 cycle/MAC). A 40-bit arithmetic-and-logic unit (ALU) implements a range of functions, with an 8-bit extension for arithmetic operations. The ST18950 has a 40-bit barrel-shifter unit and a bit-manipulation unit that handles MCU (master-controller-unit) processing through bit operations. Both 16/32-bit fractional (signed/unsigned) and 16/32-bit integer (signed/unsigned) word formats are available.

The ST18950 ACU generates an address for each of the two identical data memories and updates them at each instruction, allowing execution of instructions and performing up to two register-to-memory moves in one cycle. The ST18950 implements various addressing modes: direct, indirect-linear, indirect-modulo, indirect-bit-reverse (all with postincrement), indirect-indexed, and immediate.

The ST18950 PCU updates the program counter (PC) according to the current instruction and/or internal and external events. It performs program-address generation, instruction fetch and decoding, exception processing, and hardware loop control. By default, the PC increments by 1.

The chip's ETU contains three independent parts that share the same external interface: an emulation part, core-scan registers (CSR), and a test part (for production-test purposes). Access to these units is via dedicated I/O pins, which allow the ETU to interface with an outside JTAG TAP controller or function as primary access to the final ASDSP chip—according to the IEEE 1149.1 JTAG standard.

An 8-bit general-purpose parallel port (P0 to P7) can be configured (input or output). A test condition is attached to each bit to test external events; chip control is via interface pins related to interrupt, low-power mode, reset, and miscellaneous functions.

☐ VARIATIONS

ST18932—40-MHz DSP-core megacell for application-specific processors. Includes 384-byte X RAM, 256-byte Y RAM, no program ROM, MAC unit, 10/13-MHz clock, boundary-scan on-chip emulation.

ST18933—40-MHz, ST18 DSP with 8-kbyte data RAM, 16-kbyte data ROM, 64-kbyte program ROM, 3 serial I/Os, 8-bit host port, 160-pin PQFP.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price
ST18933	40	Run	80	150-pin PQFP	$26(10,000)

SUPPORT

☐ HARDWARE SGS Thomson offers a JTAG pc board with a graphic windowed high-level source debugger for ASDSP emulation.

☐ SOFTWARE A C compiler, a simulator, and an assembler/linker that run on PC/Sun systems are available, as well as a Synopsys VHDL model.

Star Semiconductor SPROC-1x00 Family

24-bit multiprocessor DSP

☐ **OVERVIEW** Star Semiconductor's SPROC-1400 has a unique architecture, with up to four 24-bit general signal processors (GSPs) that work independently or in unison. The GSPs deliver a sustained 40-MIPS throughput. The SPROC has four data-flow managers (DFMs), on-chip DMA units, and 2k×24-bit 20-nsec SRAM for program and data. SPROC also has an in-circuit emulation access port with real-time probe capabilities. An extensive family of macros provides an easy-to-use software-development environment. Developers can currently work in Assembly language and, in the future, XDL.

SPROC-1400

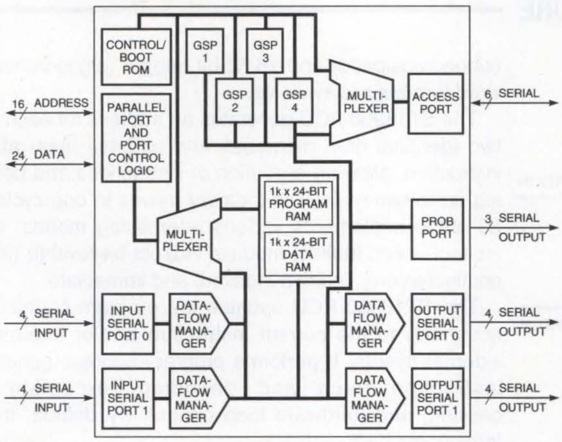
- 4 24-bit processors/chip
- CPUs time-share memory, buses
- 5 time slots/cycle, 61 instructions
- CPUs execute from same program memory
- Break/loader program ROM
- 2 3-kbyte RAM blocks; data, prog
- 24-bit instr, data, trigger buses
- 24-bit MPY; 56-bit result
- 8/16/24-bit parallel port with watchdog timer
- Serial I/O; 2 inputs, 2 outputs
- Access and probe ports
- 35/50-MHz clock (5 clocks/cycle
- Static CMOS design
- Each CPU uses different time slots to access memory
- Most instructions: 1 cycle
- 3-cycle MAC; other operations in parallel with MAC
- Data-address generator
- Parallel MAC unit, ALU in CPU
- Slave and master modes (pin-settable)
- Hardware/software wait states for external memory
- I/O takes fifth slot in data access

☐ **VENDOR CONTACTS**

Star Semiconductor Corp, San Jose, CA, (408) 526-2160; fax (408) 526-2165 **Circle No. 497**

BBS (408) 526-2180, 1200 to 2400 bps; (408) 526-2179, 4800 to 14,400 bps (N,8,1).

ARCHITECTURE



The SPROC architecture has up to four GSPs on one processor (the -1400 has four GSPs; the -1200 has two). SPROC's GSPs are non-pipelined, register-to-register, Harvard-architecture processors. Each GSP has its own 24-bit ALU, 24-bit MAC unit with 56-bit accumulator, data/program address-generation logic, instruction decode logic, and status flag register. To avoid memory or bus contention, each GSP works within a fixed time slot or state. The five states include fetch, decode, read, execute and flag-update. GSP memory or external bus access occurs only during the fetch (program op-code fetch) and read (data memory read/write) states. The SPROC has four GSPs and an I/O that request access to memory every five states. Therefore, GSP1 fetches while GSP2 is in decode state, and GSP3 is reading or writing to data memory. In addition, each GSP is autonomous from the next, allowing processing of four data types at four sample rates, concurrently and without software overhead.

SPROC/2: The data-flow managers work with time-division-multiplex (TDM) serial ports to maintain and queue input and output sampled data. These on-chip data queues can be any length (to 255 samples deep). For example, to eliminate interrupt overhead, applications that interface with the Telecom E1 or T1 highway are greatly simplified (for the DFM queue, the 32 or 24 8-bit samples in the on-chip SRAM). The DFMs also send queued data to the TDM serial ports.

Another feature of the SPROC is the large on-chip, dual-port, 20-nsec SRAM and host port. The host port with the 2k×24-bit central memory unit (CMU) eliminates the need for dual-port RAMs or FIFOs. Together they are designed to make on-chip memory look like a 300-nsec SRAM to a host processor. Thus, the host only needs to read or write to its own memory space to access data in the SPROC's DFM queues and data space, or to download program tasks. In one 125-μsec sample period, the host processor can change 400 program or data memory locations without halting SPROC. The host just moves memory—affecting its program flow without software overhead.

To handle algorithm debugging and verification for the SPROC, Star sells a real-time debugging tool called SPROC Probe. SPROC Probe's serial port, along with the in-circuit-emulation access port, lets you view, at sample rate, any on-chip data-memory address location. SPROC Probe is effectively a 24-bit shadow register that copies, at sample rate, the requested data-memory access and sends it to a dedicated 24-bit serial port. This provides the engineer not only with traditional debug tools of run-to-break, single-step etc, but also the ability to change a system variable in real time and see its effect.

Addressing modes—direct, register, indexed.

Numeric representation—24-bit integer, 24-bit Q22 fixed-point.

Memory access—10-bit program-address bus, 16-bit data-address bus.

Special instructions—multiply-accumulate, load parallel-port register from external address (master mode only).

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (500)
SPROC-1400	50 35	480 340	144-pin MQFP 144-pin PQFP	$96.29 $84.44
SPROC-1200	50	300	84-lead PLCC	$45.33
SPROC-1210	50	300	84-lead PLCC	$50.37

SUPPORT

☐ **HARDWARE** Star Semiconductor's development system is PC-based and communicates through a serial port to the SPROCbox interface unit. SPROCbox connects to a low-cost SPROC development evaluation board with I/O plug-and-go functions, such as an 80C51 host microcontroller card and a 48-kHz stereo A/D and D/A converter. The SPROC development system and the development-evaluation board use the SPROCbox to interface to the access port on the SPROC DSP, which provides ICE-like debug and run-time emulation capabilities. A PC/AT plug-in board is available from a third-party supplier.

☐ **SOFTWARE** Star Semiconductor sells a complete development environment for writing and debugging assembly-language routines as well as an extensive library of turnkey macros. The macros can be linked with user-generated code in text-editor or graphical-schematic packages. Also included in the development software is a scheduler and the tools required to link and schedule a DSP design. SPROC Micro Interface, another utility, takes advantage of SPROC's memory-mapping capability; it provides all the software hooks for the host to download and read any variable within the SPROC environment using C syntax (.H file structure).

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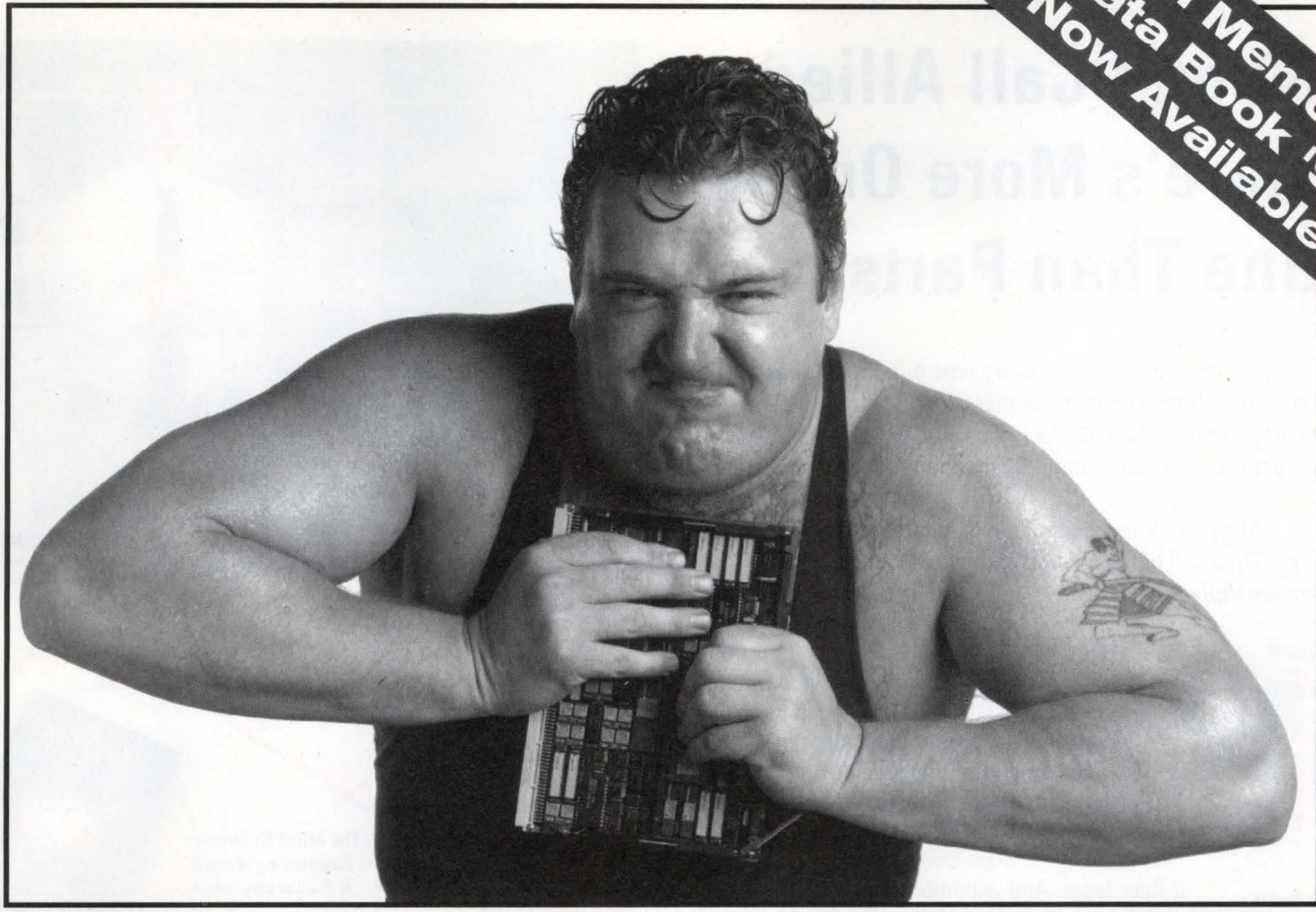

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256Kx32	EDI8F32256C*	12	64 pin ZIP/SIMM
256Kx32	EDI8F32257C*	17	64 pin ZIP
32Kx24	EDI8F2432C	15	56 pin ZIP
64Kx24	EDI8F2464C	15	56 pin ZIP
128Kx24	EDI8F24128C	20	60 pin ZIP

Surface Mount Package Styles

Organization	Part No.	Speed (ns)	Package Style
256Kx8	EDI8F8257C*	70	32 pin SOIC
2x512Kx8	EDI9F81025C	55	36 pin SOIC

*JEDEC Pinout

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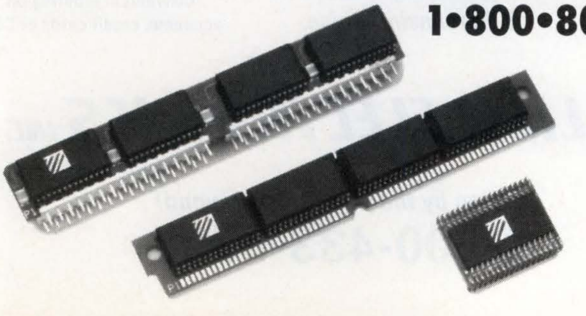

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CIRCLE NO. 158

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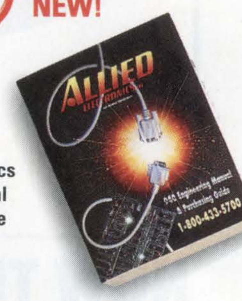

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CIRCLE NO. 30

Texas Instruments TMS320C1x Family

16-bit fixed-point DSP

☐ **OVERVIEW** Introduced in 1982, TI's TMS320C10 has some limitations, but they reflect the constraints of many early μCs and μPs: The CPU is accumulator-based, and the architecture relies on shared resources, such as buses and memories, rather than implementing multiple sets to speed processing. The modified Harvard architecture separates program and data accesses, yet allows transfers between code and data spaces to share resources. Initially, on-chip memories were small, and the C10 had a limited off-chip addressing range (12 bits).

The TMS320C10 incorporates a single-cycle multiplier, 16-bit barrel shifter, DSP-specific instruction set, and 4-level hardware stack. The C10 now has a large base of experienced designers, a large collection of application code, and a range of applications. The chip requires careful assembly-language programming, but costs have dropped to the point that C10s are competitive with many μP and μCs. In volume, C10s cost <$3 a piece.

TI has expanded the C10 family with object-code-compatible DSPs with expanded memory and peripheral sets. Memory for the later chips has ballooned—512-byte RAM and 8-kbyte ROM from the C10's 288-byte RAM and 3-kbyte ROM. Some versions provide OTP memory for development and prototyping.

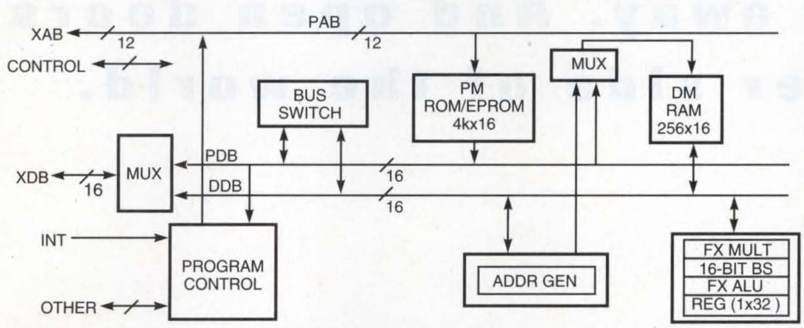
TMS320C14

- 16-bit instruction, data
- 59-instruction, 3-stage pipeline
- 2 16-bit registers, 32-bit accumulator
- 512-byte RAM
- 4-kbyte ROM/EPROM/OTP
- 2 sets 16-bit internal buses
- 4k-word address space
- 16-bit (L) barrel shifter
- 3 capture/compare timers
- 1 serial I/O port, 16 I/O pins
- 2 external interrupts
- 20/25/35-MHz clock
- 4-cycle instruction; 114-nsec cycles at 35 MHz
- Combined shift/ALU cycle
- 1-cycle multiplier
- 8-cycle MAC instruction
- 4-cycle instruction with memory R/W
- Watchdog timer
- 7-cycle max interrupt latency
- 4-level instruction stack

☐ **VENDOR CONTACTS**

Texas Instruments Inc, Dallas, TX, (800) 336-5236. **Circle No. 498**
TMS320 Technical Hot Line: (713) 274-2320.
TMS320 BBS: (713) 274-2323 (N,8,1).
Microchip Technology Inc, Chandler, AZ, (602) 786-7200 (second source for the TMS320C10, C14, and E14). **Circle No. 499**

ARCHITECTURE



A basic DSP engine, TI's TMS320C10's Harvard architecture separates program and data—each has its own bus and memory. Like many early μCs, the C10 is accumulator-based; the accumulator, however, is 32 bits wide for double-precision, 2's-complement arithmetic. A fast, single-cycle multiplier or 16-bit barrel shifter in parallel with the multiplier feeds the accumulator. A MAC operation takes two cycles and two instructions—first the multiply and then the add instruction. Addressing for the MAC data values is not automatic; a basic MAC pass requires code to specifically address, fetch, and operate on each set of X, Y data values.

The TMS320C10 has a single data bus. For each MAC operation, code must load the multiplier's T register with one data value, then move the second data value to the multiplier before starting the multiply. The DSP chip has two 16-bit auxiliary registers to hold temporary values and has one 32-bit accumulator.

The MAC's 16-bit shifter in parallel with the 16-bit multiplier feed into a 32-bit ALU that handles both 16- and 32-bit operations. The accumulator feeds back to the ALU to keep a running accumulation. Going forward, the accumulator feeds a simple shifter (shifts 0, 1, or 4 bits over) that, in turn, links to the data bus.

Code fetch and decoding is handled in a logic section that has its own program bus and memory. This section has a 4-deep stack that holds PC values for interrupts or subroutine branches. Data in the program ROM or EPROM can be transferred to the data RAM and used as constants for MAC series expansion.

Addressing modes—Direct addressing: 7 bits in instruction concatenate with 1-bit data-page pointer for accessing data RAM (128 words each page). Indirect addressing: Uses 8 bits from one of two auxiliary registers to address data RAM. Immediate addressing: Uses data in instruction.

Parallel I/O ports—You can use the 16-bit external data bus as an I/O port to connect external peripherals such as A/D or D/A converters. Separate I/O select signals let you use up to eight separate I/O ports on the bus.

Event manager—The C14 event manager adds a compare and capture subsystem to supplement the C14's two 16-bit timer/counters. The subsystem has six 16-bit compare and six 16-bit capture registers. Compare-register values are compared with the running timers; on a match, the subsystem generates an interrupt or an external signal. A high-precision PWM mode adds 2 bits of additional resolution for PWM outputs (resolution is 40 nsec at 25.6 MHz). The subsystem can capture events; changes in one of six input lines trigger logic to set the timer/counter value into a capture register. The subsystem has a FIFO stack that can buffer up to four capture values for four capture registers.

Companding hardware—On the C17, this hardware compands (compresses and expands) data for serial or parallel mode. It handles both the A and μ-Law forms, which meet American, Japanese, or European standards.

☐ **VARIATIONS**

TMS320C10—288-byte RAM, 3-kbyte ROM, 16-bit parallel I/O port, 40-pin DIP, 44-pin PLCC.

TMS320C14—512-byte RAM, 8-kbyte ROM/EPROM, 16 I/O lines, 1 serial I/O port, 2 timers, 16-bit watchdog timer, 1 baud-rate-generation timer, 68-pin PLCC.

TMS320C15—512-byte RAM, 8-kbyte ROM/EPROM; 40-pin DIP, 44-pin PLCC, 44-pin ceramic leaded chip carrier.

TMS320C16—512-byte RAM, 16-kbyte ROM, 64-pin PQFP.

TMS320C17—512-byte RAM, 8-kbyte ROM/EPROM/OTP, 2 serial I/O ports, 1 timer, 8/16-bit asynchronous coprocessor port; 40-pin DIP, 44-pin PLCC. 5 and 3V parts.

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (1000)
TMS320C10	25.6	94.4	68-pin PLCC	$4
TMS320C14	25.6	50	44-pin PLCC	$8.40
TMS320C15	25.6 14.4	85 50 (3.3V)	68-pin PLCC 68-pin PLCC	$5.80 $5.30
TMS320C16	35 25.6	100 65 (3.3V)	64-pin QFP 64-pin QFP	$6.30 $6.30
TMS320C17	20 14.4	300 22.7 (3.3V)	44-pin CLCC 44-pin PLCC	$5.30 (10,000) $5.30 (10,000)

SUPPORT

☐ **HARDWARE** An ICE and evaluation modules are available from TI. Many third-party vendors sell hardware development tools for the C1x; contact TI for references.

☐ **SOFTWARE** TI furnishes a development tool kit with an assembler/linker, simulator, and application library. Many third-party tools are also available; contact TI for references.

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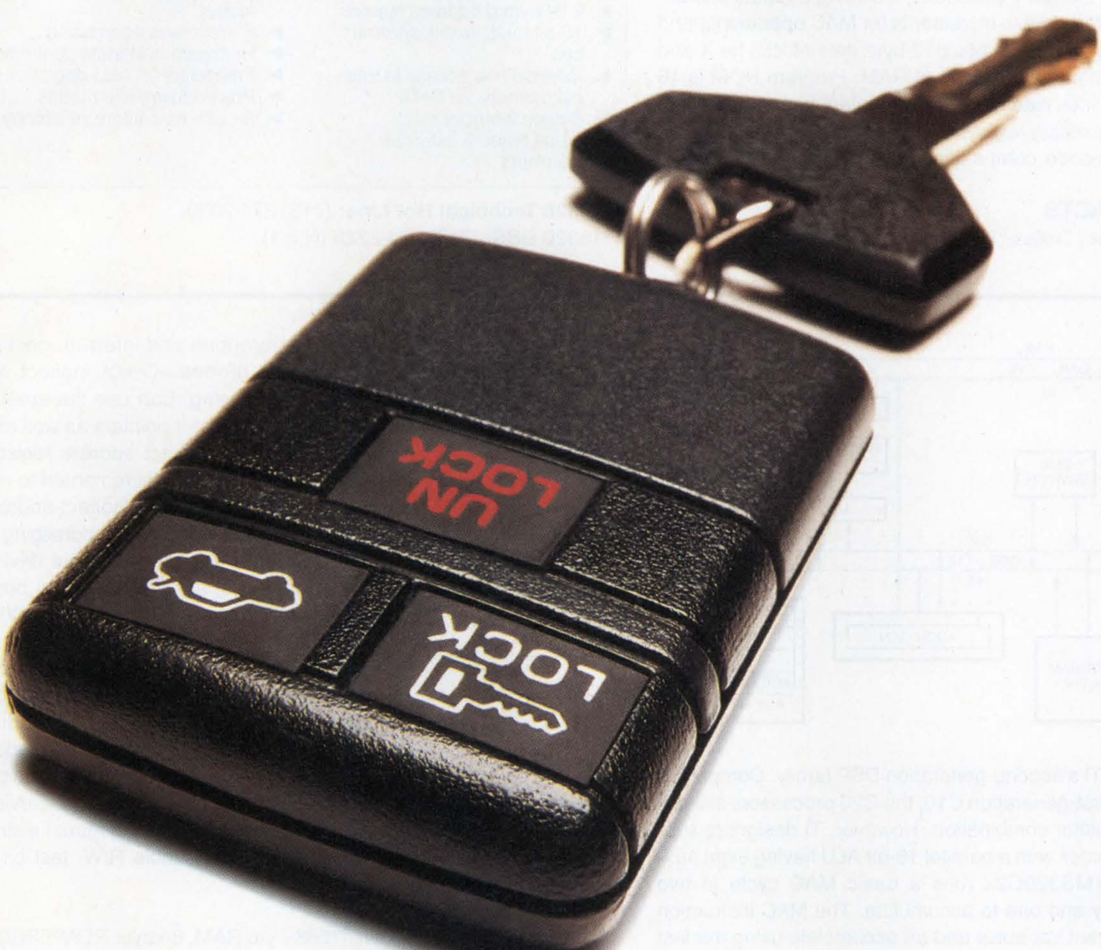


UN LOCK
LOCK

Texas Instruments TMS320C2x Family

16-bit fixed-point DSP

☐ **OVERVIEW** Introduced in 1986, the TMS320C2x is TI's second-generation 16-bit, fixed-point DSP. The C2x follows the C1x's accumulator-based architecture, but TI used increasing silicon densities to raise processor performance and make the chip easier to program and design in. TI engineers worked out the earlier C10's limitations: External memory addressing is 16 bits (64k words each for data and code); they added 24 new instructions, including a repeat instruction (with automatic data-address increments for MAC operations) and expanded on-chip RAM to include two 512-byte data blocks for X and Y memories supplemented by 64 bytes of RAM. Program ROM is 16 kbytes, and DMA simplifies external access to internal memory. A 16-bit ALU with a set of 8 auxiliary registers parallels MAC operations. The TMS320C2x is source-code compatible with the earlier 16-bit fixed-point C1x DSPs.

☐ **VENDOR CONTACTS**

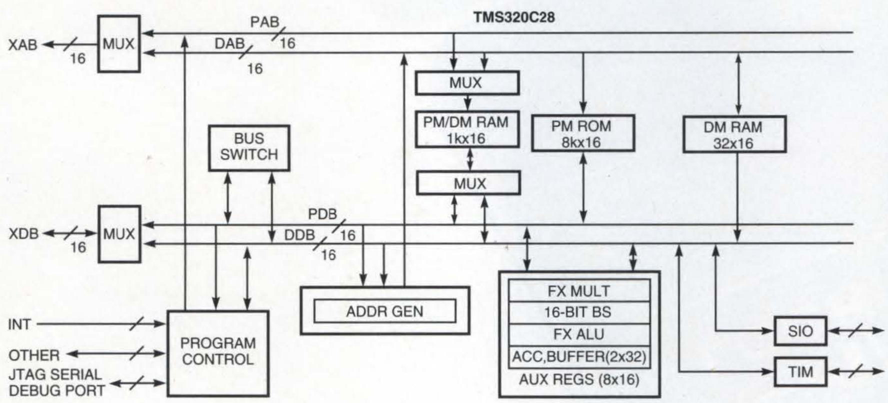
Texas Instruments Inc, Dallas, TX, (800) 336-5236. **Circle No. 500**

TMS320C28

- 133 instructions, 3-stage pipeline
- 8 auxiliary regs
- 2 544-byte data RAM blocks
- 64-byte data RAM
- 16-kbyte program ROM
- 2 64k-word address spaces
- 16-bit multiplexed external bus
- External bus access to internal memory via DMA
- 8-deep interrupt stack
- 16-bit timer, 3 external interrupts
- 50-MHz clock (cycle=clock/4)
- 1-cycle instruction execution (pipelined)
- 1-cycle MPY, MAC (pipelined)
- Data block move
- Zero-overhead instruction repeat
- Bit-reversed addressing
- Hardware wait-state generator
- Parallel MPY, ALU operations
- Power-down, idle modes
- 8-cycle max interrupt latency

TMS320 Technical Hot Line: (713) 274-2320.
TMS320 BBS: (713) 274-2323 (N,8,1).

ARCHITECTURE



The TMS320C2x is TI's second-generation DSP family. Compatible (to a degree) with the first-generation C10, the C20 processors still rely on a multiplier-accumulator combination. However, TI designers supplemented those resources with a parallel 16-bit ALU having eight auxiliary registers. The TMS320C2x runs a basic MAC cycle in two cycles—one to multiply and one to accumulate. The MAC instruction does a multiply on current variables and an accumulate using the last cycle's accumulated value. The chip can access two data (or program) RAMs in a single cycle to feed the multiply for a MAC cycle. However, unlike later DSPs, C2x code must explicitly handle data addressing for the next MAC cycle unless the MAC instruction is a repeated instruction. In that case, the data and program/data block addresses are automatically incremented.

The C2x has a modified Harvard architecture and maintains two separate memory and bus systems, one each for data and program code. On-chip program accesses do not interfere with DSP data manipulation. Code and data share a common external memory bus; each has its own 64k-word address space. A C2x can address up to 128k words of external memory, with a pin differentiating between the data and program address spaces. With a fast enough external memory, a C2x delivers single-cycle (pipelined) instruction execution by accessing instructions or one of the data values from external memory. However, you can use slower memory to cut costs; the C2x hardware generates memory wait states to stretch out access times.

With the C2x, you don't have to write code loops to repeat key instructions. TI added a repeat-instruction capability, and you can repeat an instruction up to 255×. Also, the 8-level hardware stack automatically extends into memory, thus enabling code to deal with deep subroutine and interrupt nesting.

Addressing modes—Direct, indirect, and immediate addressing. Can use the auxiliary registers to hold indirect pointers as well as to index the address. Indirect address registers can be postincremented/decremented to minimize addressing overhead. Indirect-addressing options include bit-reversal addressing.

External DMA access—External devices can take control of the C2x's internal buses and read/write the on-chip memories. When the HOLDA signal pulls down, the C2x processor halts, opening memory to external access.

Special instructions—Load T (multiply) register and accumulate previous product; load T register, accumulate previous product, and move data; multiply and accumulate; multiply and accumulate previous product; square and accumulate; square and subtract previous product; call subroutine indirect; block move (used with repeat instruction, program to data, data to data memory); table R/W; test bit (in memory); repeat.

☐ **VARIATIONS**

TMS320C25—40/50-MHz, 1088-byte RAM, 8-kbyte ROM/EPROM, serial I/O port, 68-pin PGA/PLCC.

TMS320C26—50-MHz, three 1-kbyte data/program RAM blocks, 64-byte data RAM, 512-byte boot ROM, timer, serial I/O port, 68-pin PLCC. Multiprocessor support.

TMS320C28—40-MHz, 512-byte data RAM, 512-byte data/program RAM, 64-byte data RAM, 16-kbyte ROM, timer, serial I/O port, 68-pin PLCC or 80-pin PQFP. Power-down mode.

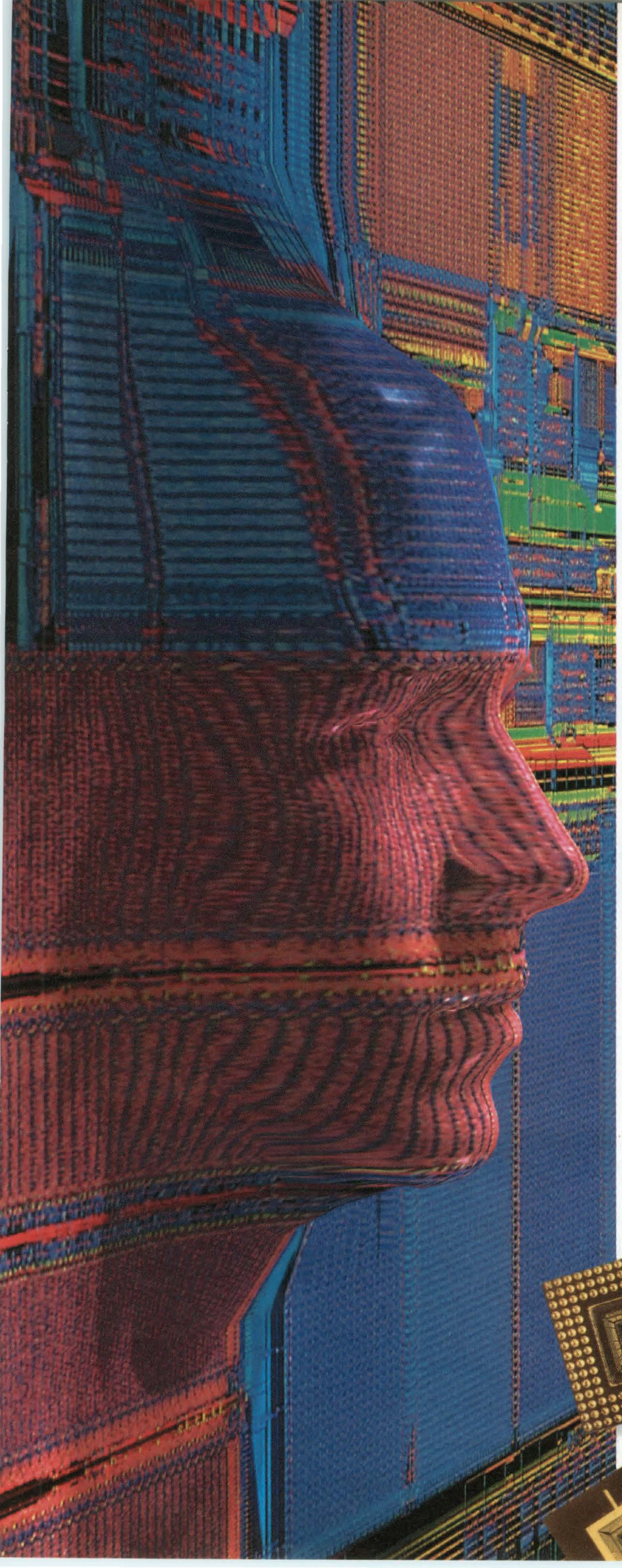
TEC320C25A—60-MHz application-specific processor (ASP) that combines a C25 and a gate array with 15k usable gates, 8-kbyte program ROM, 1088-byte data RAM, and 1-kbyte RAM. 100/144-pin SQFP.

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price (1000)
TMS320C25	50	Run Idle	185 100	68-pin PLCC	$11.60
TMS320C26	50	Run Idle	220 100	68-pin PLCC	$10.50
TMS320C28	40	Run Power-down	185 100	80-pin QFP 68-pin PLCC	$12.60

SUPPORT

☐ **HARDWARE** TI provides a software development board and evaluation boards that use the built-in emulation logic in the C2x. Third-party tools are also available; contact TI for information.

☐ **SOFTWARE** TI supplies a C compiler, source-level debugger, assembler/linker, simulator, and application library. Third-party tools are also available.



Texas Instruments TMS320C3x Family — 32-bit floating-point DSP

OVERVIEW TI's third-generation DSP, the TMS320C3x, is a 32-bit processor that integrates a Von Neumann microprocessor architecture with a high-performance, 32-bit, floating-point DSP MAC core. On the microprocessor side, the C3x supports a single 24-bit address space. On the DSP side, the C3x processor performs single-cycle MAC processing; the processor gets the next instruction while accessing two data values for the current instruction's MAC cycle. Two address generators automatically update X, Y memory addresses for inner-loop processing.

The C3x architecture uses multiple memories and bus paths for parallel data and instruction accessing as well as processing. The C3x supports two complete external memory or I/O buses; has three bus sets—program, data1, and data2—and a DMA bus to provide access to on-chip memories; and holds four memories—a 64-word cache, two 1k-word RAM blocks, and one 4k-word ROM block. The inner-core CPU is a complex of five sub-buses interconnecting a multiplier, 32-bit barrel shifter and ALU, and multiple accumulators. Instead of confining MAC operations to an accumulator-based structure, the C3x relies on a multiported register file, which holds 8 extended-precision registers, 8 auxiliary registers, 2 index and 12 control registers.

TMS320C31/LC31

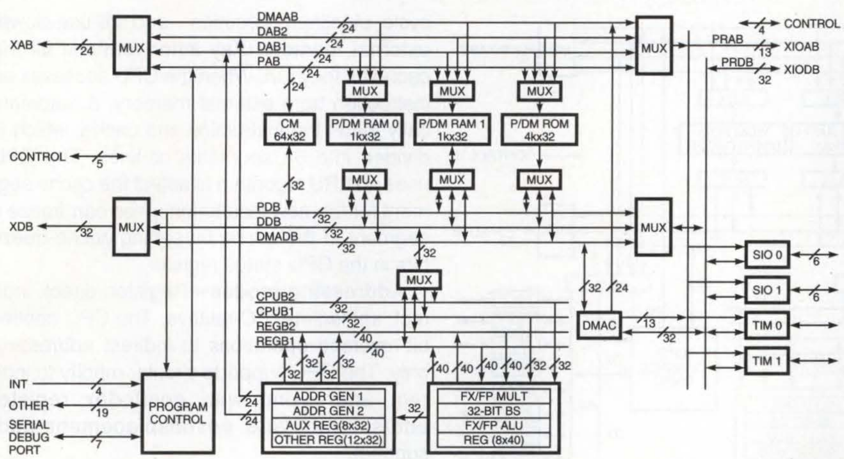
- 32-bit data, instruction
- 4-stage pipeline, 113 instructions
- Multiport reg file: 8 40-bit extended-precision regs, 2 index, 8 indirect address regs
- 32-bit barrel shifter/ALU
- 256-byte program cache, 16-kbyte ROM
- 2 4-kbyte data RAM blocks
- Floating-point/integer multiplier, ALU
- 32-bit barrel shifter
- Two address generators
- 3 address/data bus sets: program, data1, data2
- 24-bit address space
- 2 16-bit timers, serial I/O
- 4 external interrupts
- 27/33/40-MHz clock (2 clocks=1 cycle)
- Zero-overhead looping
- Single-cycle branches
- 2- and 3-operand instructions
- 1-cycle MPY, ALU operations
- 24-bit integer operations; 32-bit floating-point operations
- 40-bit floating-point MPY
- Code-block-repeat instruction
- DMA controller
- 200-μsec max interrupt response
- Serial scan, test/debug interface
- LC31: 2 user-programmable power-down modes

VENDOR CONTACTS

Texas Instruments Inc, Dallas, TX, (800) 336-5236. **Circle No. 501**

TMS320 Technical Hot Line: (713) 274-2320.
TMS320 BBS: (713) 274-2323 (N,8,1).

ARCHITECTURE



The 32-bit floating-point TMS320C3x is a complex DSP processor; it relies heavily on multiple buses, multiple memories, and register files to deliver parallel, high-throughput processing. It supports a single 16-Mbyte address space and has two external bus systems, a primary bus and expansion bus. (The C31 has only the primary bus.)

Three subsystems make up the TMS320C3x DSP: the memory/access, central core, and I/O subsystems. The memory/access subsystem builds around four major buses that link the central core and I/O subsystems and multiplex into the two external buses. The four buses—the program address/data buses, two data address/data1+data2, and DMA address/data buses—enable programs to access the next instruction and two data values simultaneously and transfer data to or from the I/O subsystem in one cycle. The data buses share a single address bus; they make two sequential RAM accesses in a single cycle. An on-chip cache automatically loads as instructions are accessed and holds up to 64 instructions. The two 4-kbyte RAM blocks hold parameters and constants for sum-of-products MAC processing, and a large ROM can hold code or coefficients for MAC processing.

The two data buses, which a single data-address bus serves, feed the C3x central-core subsystem. A minisystem in its own right, the central core has its own set of buses to move data and results; two CPU buses move data to and from the memory and access the subsystem and two register buses that move data between internal core registers. These registers and access data feed into an integer/floating-point multiplier and a parallel 32-bit barrel shifter/ALU. Results are stored in extended-precision or auxiliary registers that hold the values. Two address generators in the subsystem generate the addresses to access the memory/access subsystem's data memories. The major core registers—extended-precision registers (40 bits), auxiliary registers, and key-control registers—are held in a central multiported register file.

The third C3x subsystem, the I/O subsystem, comprises a single-channel DMA controller and a collection of peripherals interlinked with the peripheral address and data bus set. The DMA controller uses the memory/access subsystem's DMA bus to access on-chip memory. The memory/access subsystem buses pass through a multiplexer and link to the peripheral bus, which serves the DMA controller and peripherals. The peripheral bus links to the second external bus with a 13-bit address bus and 32-bit data bus.

Addressing modes—Register, direct, indirect, short immediate, long immediate, PC relative, pre- and postindex add/subtract, automatic circular, and bit-reversed addressing. The hardware has a memory-based stack.

Special instructions—Repeat code block, repeat an instruction, standard/delayed branches (standard empties pipe; delayed waits 3 cycles before changing PC), interlocked access instructions for multiprocessing (load/store integer or FP value and signal interlocked), computed GOTOs (dynamic subroutine calls). You can specify instructions to execute in parallel.

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (10,000)
TMS320C30	27	500	181-pin PGA (3V, 208-pin PQFP)	$126 (3V, $53.20)
	33	600		$135 (3V, $57)
	40	730		$155.70 (3V, $65.60)
TMS320C31 (TMS320LC31)	27	260	132-pin PQFP	$33.30
	33	325		$38
	40	390		$41.80

SUPPORT

HARDWARE TI supplies a full-speed ICE and an evaluation module. Third-party vendors have hardware tools for the C3x; contact TI for references. HP has an ICE for the C30.

SOFTWARE TI sells a tool set that includes a C and C++ compiler, assembler/linker, source-level debugger, code profiler, simulator, and application library. Third-party tools: C and Ada compilers, an OS (Spox), filter-design packages, and advanced graphical design tools.

Texas Instruments TMS320C4x Family

32-bit floating-point DSP

☐ **OVERVIEW** The TMS320C40 is the top TI floating-point DSP. As a DSP engine, the C40 has enough internal buses and on-chip memories to deliver single-cycle execution while walking through X, Y memories for a series of MAC operations. A cache speeds inner-loop processing using slower, cheaper external memories.

The C40 is more than just a fast, floating-point DSP chip—it provides a new level of parallel processing. TI engineers added six independent communications ports for point-to-point links to other C40 processors. The ports are backed with a sophisticated DMA subsystem that has its own internal buses. The C40 is popular for multiprocessor applications and is making a dent in the multiprocessing market previously dominated by the SGS-Thomson Transputer, which has point-to-point serial communications links.

TI engineers also added on-chip, scan-based emulation-control capability accessible via a JTAG test port. External hardware can use the JTAG port to control the processor as well as to set and to monitor registers or memory. You can also string multiple C40s on a JTAG circuit for parallel debugging. One processor breakpoint can halt execution in an array of C40s, and you can single-step them all in lock step.

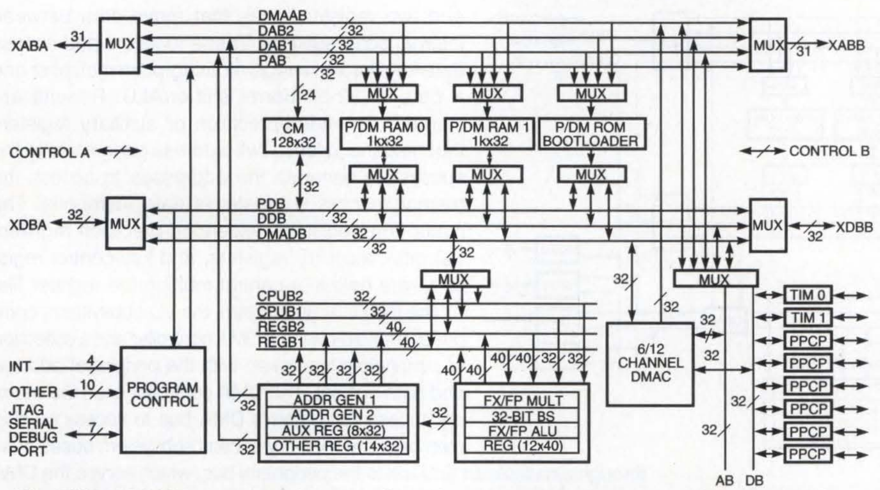
TMS320C40

- Multiport reg file: 12 40-bit, 8 auxiliary, and 12 control regs
- 4-stage pipeline, 135 instructions
- 512-byte program cache
- 2 4-kbyte dual-access RAM blocks
- Boot-loader ROM
- 2 external buses: 31-bit address, 32-bit data
- 6/12-channel DMA controller
- 6 8-bit comm ports
- 2 timers, 4 external interrupts
- JTAG test/debug interface
- 80/60/50/40-MHz clock (2 clocks=1 cycle)
- 1-cycle pipelined execution for most instructions
- 1-cycle IEEE floating-point conversion, branch, calls, returns
- 6 operations/cycle: 2 accesses, FP MPY, FP ALU, branch, DMA
- External bus: 160 Mbytes/sec max
- 29 Mbyte/sec max per comm port
- Circular, bit-reversal addressing
- Automatic loop and DMA addressing
- 12-cycle max interrupt latency

☐ **VENDOR CONTACTS**

Texas Instruments Inc, Dallas, TX, (800) 336-5236. **Circle No. 502**
TMS320 Technical Hot Line: (713) 274-2320.
TMS320 BBS: (713) 274-2323 (N,8,1).

ARCHITECTURE



The TMS320C40 has come a long way from the accumulator-based TMS320C10 that TI introduced in 1982. The C40, introduced in 1991, is built around a 5-port register file; and rather than time-sharing a single bus system, it features separate buses for program and two data fetches. Additionally, the C40 has three separate functional units: the FPU multiplier, ALU, and barrel shifter for parallel operations.

To maintain high throughput for math-intensive processing, the C40 has two independent bus systems for accessing separate external memories. These buses can be linked to the internal program and data buses. A small, 128-word cache holds inner-loop code for fast processing. To minimize instruction-fetch overhead, instructions and code blocks in the cache can be repeated with the help of automatic code control and X, Y data addressing.

TI engineers equipped the C40 with six independent communications ports for point-to-point communications with networks of C40s and peripherals. These ports free the external memory buses for program or data accesses. A sophisticated DMA subsystem with its own address and data buses moves data between the communication ports and memory without altering the CPU's sequential threads. Such data movements do not load down the DSP processor with servicing overhead, although some data contention for memory may slow CPU execution.

The C40's 128-word cache enables the processor to deliver single-cycle, pipelined execution—and still use slower external memory. Key inner routines fill the cache as they run. When the CPU accesses an instruction from external memory, it automatically loads the instruction into cache, which is divided into 32 segments or lines. The CPU uses an LRU algorithm to select the cache segment for the new instructions. You can freeze a segment in the cache by setting cache-freeze bits in the CPU status register.

Addressing modes—Register, direct, indirect, immediate, PC-relative. The CPU applies bit-reversed operations to indirect addressing only. The CPU supports circular modify to indirect addressing with postindex register add/subtract and postdisplacement add/subtract.

Memory maps—The C40 has a 4G-word address space for program and data. External memory for program and data are accessed via the local or global external buses. Bus usage is not fixed, but assigned by the application. Local and global buses have different memory-block assignments within each memory space. I/O can also use the external buses.

Numeric representation—The C40 supports TI's 40-bit extended floating-point format. However, TI built in a 1-cycle instruction that extends the TI format to the IEEE format. The C40 supports

- 16-bit short signed and unsigned integer
- 32-bit signed and unsigned integer
- short floating point: 4-bit exponent, sign bit, 11-bit fraction
- single-precision floating point: 8-bit exponent, sign bit, 23-bit fraction
- extended precision floating point: 8-bit exponent, sign bit, 31-bit fraction.

Repeat modes—The C40 can repeat a single instruction or a block of code with zero-overhead looping control. Launching a block repeat requires 4-cycle overhead; block repeats are nestable.

Part no.	Clock (MHz)	Max power (mA at 5V)	Pins, package	Price (10,000)
TMS320C40	40	680	325-pin PGA	$178.20
	50	850		$198
	60	1020		Sampling
	80	1360		this quarter

SUPPORT

☐ **HARDWARE** Development system includes scan-based emulation via the C40's JTAG test port. TI sells a C40 evaluation board with four processors that works with a number of host platforms. Third-party tools are also available; contact TI for a list of vendors.

☐ **SOFTWARE** Tools include a C compiler, Ada and C++ compilers, source-level debugger for parallel debugging, assembler/linker, and simulator. TI also has an application library. Third-party support includes the Spox, Parallel C, Virtuoso, and Helios operating systems.

Texas Instruments TMS320C5x Family

16-bit fixed-point DSP

☐ **OVERVIEW** Introduced in 1989, the TMS320C5x is TI's highest performance 16-bit fixed-point DSP. TI designers enhanced the C2x for more efficient operation, higher-throughput processing, and embedded applications. A static CMOS design, the C5x runs at up to 80 MHz for the 5V version and to 50 MHz for the 3.3V device. Processor throughput is double that of the earlier TMS320C2x; the instruction cycle is 25 nsec for pipelined execution. The C5x has gained instructions for controller applications, major registers have shadow registers for fast context switching, and an added logic unit handles logical bit operations. Depending on the device version, C5x features include up to 20-kbyte program/data RAM, up to 32-kbyte ROM, a standard serial port, a time-division-multiplexed (TDM) serial port, and a 16-bit timer. The C5x has two indirectly addressed circular buffers for DSP applications. The C5x also has a JTAG serial scan port for chip text and ICE-like debug control and monitoring.

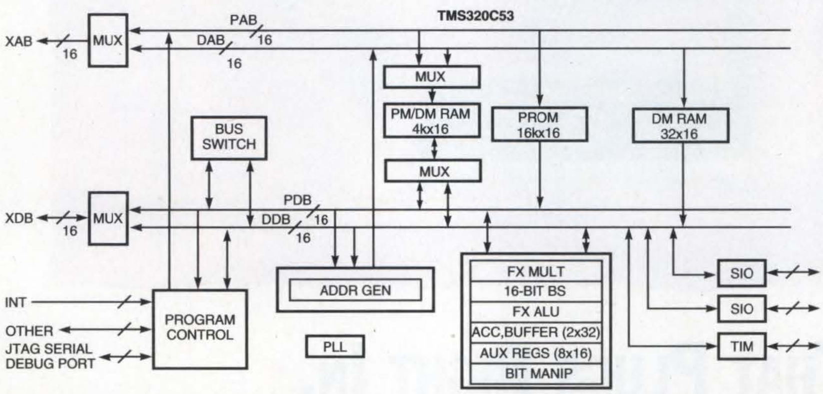
The TMS320C52 DSP CPU is also offered as an application-specific-processor (ASP) core for a TI gate array, the TEC320C52. It combines 10k usable gates for special logic, 8k words of ROM, and 2k words of RAM. The gate array runs at 57.1 or 80 MHz.

TMS320C53

- 3 MPY regs, 8 aux regs, 11 shadow regs
- 32-bit accumulator, buffer
- 2 1-kbyte data/prog RAM blocks, 64-byte data RAM, 6-kbyte data/prog RAM
- 32-kbyte program ROM
- 16-bit external bus
- 3 128-kbyte spaces for data, program, I/O
- 8-level PC stack
- 16-bit timer, 4 ext intr
- 2 serial I/O ports (1 TDM)
- JTAG-port emulator control
- 40/57/80-MHz clock (div-by-1 PLL)
- 1-cycle instr execution (pipelined)
- Single-cycle MPY
- Parallel ALU, MPY, logic operations
- Parallel op-code and 2-data fetch
- 1-/2-cycle read/write to ext memory
- 32-bit accum buffer for comparisons, 64-bit shifts
- Software wait-state generator for memory; up to 7 states
- Serial I/O up to 20 bps
- 5, 3.3V parts

☐ **VENDOR CONTACTS**
Texas Instruments Inc, Dallas, TX, (800) 336-5236. **Circle No. 503**
TMS320 Technical Hot Line: (713) 274-2320.
TMS320 BBS: (713) 274-2323 (N,8,1).

ARCHITECTURE



The TMS320C5x is both an accumulator-based, 16-bit fixed-point DSP and a register-based processor. It has a fixed MAC circuit with a registered, 16×16-bit multiplier loading a 32-bit product register. The product register, in turn, feeds a 32-bit accumulator. The C5x also has two parallel functional units feeding off the data bus: an independent ALU with a register file of eight auxiliary registers and a bit-logic processing unit. A multiply takes one cycle, as does an accumulate. The basic MAC cycle involves setting a value into a temporary register, fetching a second value, multiplying into a holder register, and accumulating the result in the next cycle. Like most DSPs, the C5x has a Harvard architecture with separate program and memory buses.

To improve C25 performance, TI engineers streamlined the hardware implementation, extended the instruction set, and moved to a smaller CMOS process. The C5x delivers double the performance of the earlier C2x. Additionally, the C5x has larger on-chip memories: up to 32 kbytes of program ROM, a 2112-byte data RAM that can also store code, and up to 18 kbytes of RAM for storing data or code. The CPU can read the 2112-byte data RAM to retrieve two values for the next MAC cycle. Data in the multiplier register can be prescaled before passing into the 32-bit ALU for the accumulator cycle.

For embedded applications, TI engineers added fast context switching and bit-level operations. To minimize the overhead for saving the CPU state or context on an interrupt, the C5x has a 1-deep shadow register stack for the major registers (accumulator, accumulator buffer, product reg, status regs, three temporary regs, index reg, and auxiliary compare reg). For control applications that need bit manipulation, TI engineers added a parallel logic unit (PLU) that runs in parallel with the MAC and ALU circuits. The PLU operations can set, clear, test, or toggle multiple bits in a control/status register or data-memory location.

Power-down mode—Minimizes power by shutting down the CPU (IDLE1 instr) or the CPU and the peripherals (IDLE2). Pulling down an external pin (HOLD') can also force the chip into power-down mode. An interrupt brings the chip up to normal run conditions.

Addressing modes—Direct, indirect, immediate, dedicated register, memory-mapped register. The processor supports automatic circular buffer addressing for two buffers.

Special instructions—Block repeat, load T (multiply) register and accumulate previous product; load T register, accumulate previous product, and move data; multiply and accumulate; multiply and accumulate previous product; square and accumulate; square and subtract previous product; call subroutine indirect; block move (use with repeat instr and prog to data, data to data memory); table R/W; test bit in memory; repeat.

☐ **VARIATIONS**

TMS320C50—20-kbyte prog/data RAM, 4-kbyte ROM, 2 serial ports, 1 timer, 132-pin PQFP.

TMS320C51—4-kbyte prog/data RAM, 16-kbyte ROM, 2 serial ports, 1 timer, 132-pin PQFP/100-pin TQFP.

TMS320C52—2-kbyte prog/data RAM, 8-kbyte ROM, 1 serial port, 1 timer, 100-pin PQFP/TQFP.

TMS320C53—8-kbyte prog/data RAM, 32-kbyte ROM, 2 serial ports, 1 timer, 132-pin PQFP/100-pin TQFP.

	Clock	Max power (mA at 5V and 40 MHz)			Price		
Part no.	(MHz)	Run	Idle-1	Idle-2	40-MHz	57-MHz	80-MHz
TMS320C50	40/57/80	100	10	0.005	$55	$60	$66
TMS320C51	40/57/80	100	10	0.005	$24	$27	$33
TMS320C52	40/57/80	100	10	0.005	$16	$19	$23
TMS320C53	40/57/80	100	10	0.005	$37	$42	$51

SUPPORT

☐ **HARDWARE** TI supplies a DSP starter kit, an evaluation module and an emulator based on the C5x's built-in emulation logic. Third-party tools are also available.

☐ **SOFTWARE** TI supplies a C compiler, source-level C/assembler debugger, assembler/linker, simulator, profiler, and application library. Third-party tools are also available.

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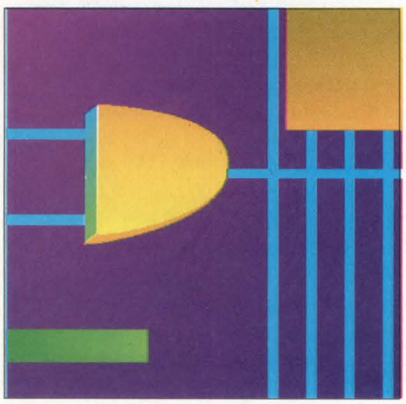

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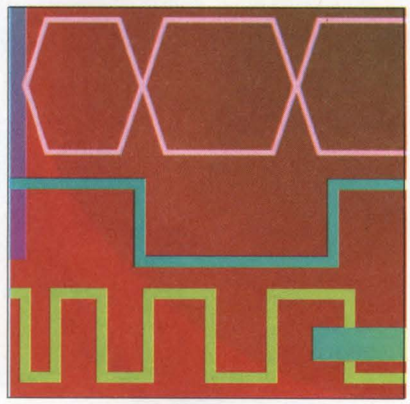

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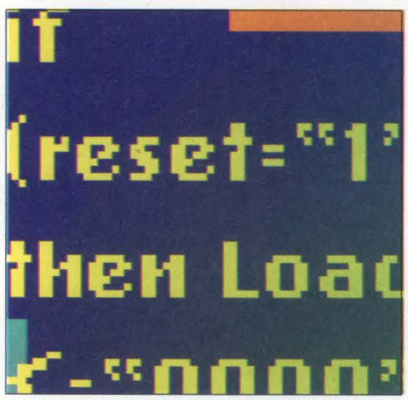

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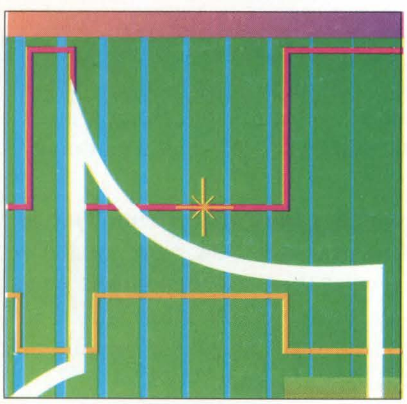

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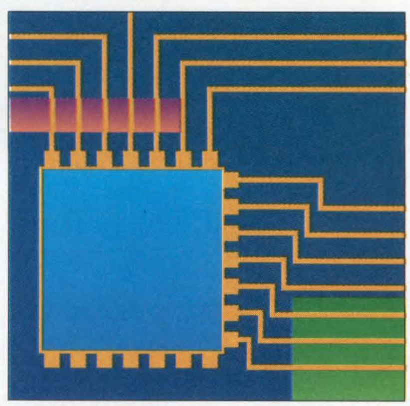

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Texas Instruments TMS320C80 — 32-bit multiprocessor DSP

☐ **OVERVIEW** The TI Multimedia Video Processor (MVP) delivers 2-BOPS (billion-operations/sec) performance and integrates four DSP CPUs and a 32-bit RISC CPU with a fast crossbar memory (50 kbytes), supplemented with I/O and video controllers. MVP's processing suits a range of real-time applications, such as video compression/decompression, telecommunications, image recognition, multimedia presentation, and audio. With the MVP, system designers no longer have to gang multiple DSPs to achieve billion-operation performance. And MVP is cost-effective: its four DSPs and 32-bit RISC fit on a single chip. Each processor has its own memory but can access the others' memories.

Following the TMS340, its graphics-processor predecessor, MVP handles bit/pixel addressing and processing. MVP has a video controller (VC) that supports two video channels and an on-chip I/O controller; its transfer controller accesses ROM, SRAM, VRAM, and DRAM. MVP does have processing limitations, however, such as per-processor memory resources and a 400-Mbyte/sec external bus bandwidth.

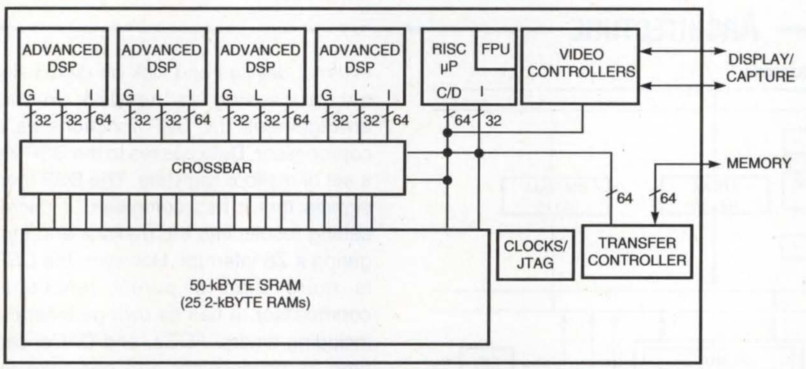
TMS320C80

- 4 million transistors, 0.6-µm CMOS
- 4 32-bit DSP CPUs: 64-bit instruction word, 2-kbyte instruction cache (CBM)
- 32-bit RISC CPU: 4-kbyte instruction cache (CBM), 4-kbyte data cache (CBM), 64-bit FPU (IEEE 754)
- On-chip crossbar memory (CBM): 25 2-kbyte RAM blocks with 5 2-kbyte blocks/CPU
- Transfer controller: 32-bit address, 64-bit data external buses with DRAM address multiplexing
- Video controller
- 42-, 50-MHz cycle rate (84/100-MHz crystal input)
- 2 billion operations/sec (BOPS)
- 4 DSP CPUs (1-cycle MAC)
- 1-cycle RISC CPU execution
- CBM: 4.2-Gbyte/sec peak rate, to 15 accesses/cycle, to 3 accesses/cycle/DSP, round-robin access priority, pipelined
- 400-Mbyte/sec peak off-chip transfer rate (50-MHz cycle rate)
- Big- or little-endian operation

☐ **VENDOR CONTACT** **Texas Instruments Inc,** Semiconductor Group, Houston, TX. (800) 477-8924, ext 4500. **Circle No. 504**

ARCHITECTURE

TMS320C80 MVP



MVP integrates, on a single chip, four DSP CPUs and a 32-bit RISC CPU with a fast crossbar memory (50 kbytes) and memory and video controllers. MVP processes multiple tasks in parallel (each assigned to a specific processor), collectively delivering high processing throughput.

MVP's five processors (four parallel DSP chips and a 32-bit RISC chip with its own FPU) execute independently and concurrently. A high-speed, on-chip crossbar connects the CPUs with 25 2-kbyte blocks of dedicated SRAM, which provides cache and RAM for each CPU. Any processor can access any of 16 SRAM blocks, although 5 blocks are dedicated to each CPU. The crossbar handles up to 15 simultaneous RAM accesses/clock cycle: 3 per DSP processor; 2 for the 32-bit RISC master processor; and 1 for the transfer controller. Peak crossbar bandwidth is 4.2 Gbytes/sec. Memory-mapped control registers handle both transfer and video controllers; the chip has a separate 32-bit data path between the MP (master processor), TC (transfer controller), and VC (video controller), which enables the MP to set register values.

The MVP has high processor throughput: each CPU can execute from its own crossbar-memory instruction cache—2 kbytes for the DSPs and 4 kbytes for the RISC CPU. The RISC CPU also has 4 kbytes of crossbar-memory data cache. The DSP processors access data from their dedicated SRAM blocks through the crossbar memory. Executing from crossbar instruction caches, the CPUs achieve apparent single-cycle execution.

The DSP CPUs have a 64-bit instruction word with three major subfields for controlling the data unit (with a 32-bit ALU and 16-bit multiplier) and each of two independent address units in each single-cycle instruction. Each address unit has a 32-bit data path to the crossbar. Three zero-overhead loop controllers support nested looping. The 32-bit ALU can split into two 16-bit ALUs or four 8-bit ALUs; the multiplier performs one 16×16 multiply or two 8×8 multiplies. Additional hardware supports bit field and pixel processing.

The 32-bit RISC CPU has an integrated 64-bit floating-point unit (FPU) that shares a common 31×32-bit register file with integer processing. A register scoreboard flags registers that are waiting on loads from memory or from the FPU to keep operations in order without unnecessary waiting.

The MP FPU incorporates a single-precision FP multiplier and a double-precision FP adder. It also supports vector processing with built-in vector operations and four accumulators to hold interim vector results. Both the CPU main integer path and the FPU units are pipelined. The CPU has a 3-stage pipeline. A single-precision multiply or double-precision addition normally takes four cycles to complete but are pipelined, so they can start every cycle. Divides, square root, and double-precision multiplies cycle to complete. The integer unit triggers FPU operations, which then proceed independently. Vector instructions can start a multiply, add, and load or store every cycle, yielding a peak performance of 100 Mflops.

The MVP is more than just a collection of CPUs and memory; it has its own on-chip I/O and memory controller, the TC, which provides an adaptive memory interface with automatic byte alignment, as well as both linear and X, Y (frame buffer) addressing. It supports DRAM, VRAM, and SRAM and also has a video controller to minimize design for video applications. This controller supports two video frames (all video timing signals). It also has a special serial-register-transfer (SRT) controller for controlling VRAM frame memories by the TC.

Part no.	Clock	Max power	Package	Price
TMS320C80	50 MHz	7.5W	305-pin CPGA	$400 (10,000)

SUPPORT

☐ **HARDWARE** MVP supports multiple processor breakpoints: one CPU can breakpoint and halt execution of all CPUs on the chip. TI sells a parallel-processing ICE (XDS5210) that handles debugging of multiple MVP chips. Loughborough Sound Images Ltd (Loughborough, Leicestershire, UK) sells a MVP hardware-development system.

☐ **SOFTWARE** TI sells a tool set that includes an assembler/linker, a C compiler, a simulator, a parallel debugger, and an application library. The debugger includes the Master Processor Debugger and multiple DSP debuggers. The Parallel Debug Manager handles and coordinates the individual CPU debuggers. TI fields a multitasking executive that runs on the RISC CPU, interfaces to a host CPU, and issues commands to MVP's DSP CPUs.

Zilog Z89C00 Family

16-bit fixed-point DSP

☐ **OVERVIEW** Zilog, a μP pioneer, added DSP chips and DSP-enhanced μCs to its line to handle math-intensive processing for voice, video, and disk-control applications. Starting with the Z89C00, Zilog offers a 10-MIPS, 16-bit, fixed-point DSP. The Z89C00 is an accumulator-based processor built around a MAC core, which includes a 16×16-bit multiplier, 24-bit product register, and 24-bit accumulator. The Z89C00 executes MACs in one cycle. Two on-chip RAM blocks hold X and Y data; two internal buses for program and data speed processing. The MAC core can access two operands/cycle because the two RAM blocks can directly load the MAC input-holding register each cycle.

Zilog uses the Z89C00 DSP as a core engine for embedded applications; Zilog engineers integrated the DSP with a standard Z8 8-bit μC. The two processors run concurrently and use a mailbox to pass data back and forth. Typically, the Z8 drives processing; it acts as an application host and initiates DSP processing as needed. When the DSP engine finishes a processing function, it can trigger a Z8 interrupt to notify the controller of pending processing. The Z8/DSP combination has been tailored for applications including disk-drive control and tapeless answering machines. Zilog has also expanded the Z89C00 engine with a variety of peripherals. A low-cost version, the Z89321, has an on-chip codec interface for voice, audio, and digital-cellular applications.

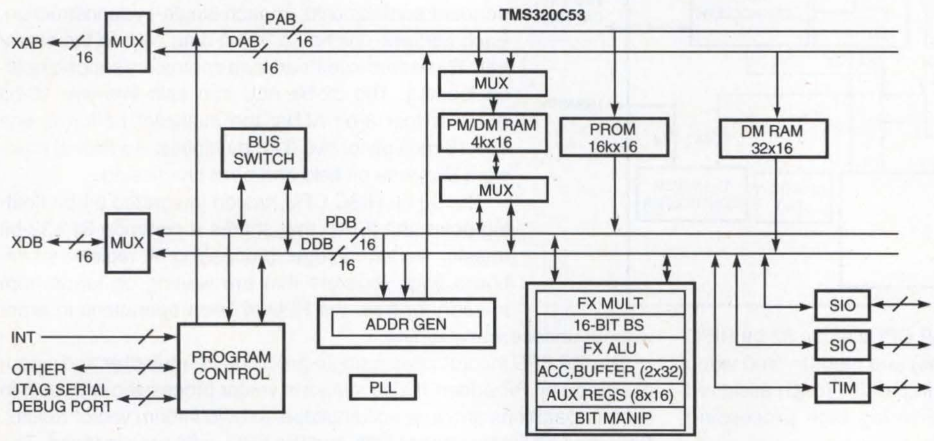
Z89C00

- ▶ 2-stage pipeline, 30 instructions
- ▶ 16-bit program, data buses
- ▶ 24-bit MPY/ACCUM, accumulate register
- ▶ 8-kbyte ROM; 2 512-byte RAM blocks
- ▶ 16-bit external memory bus, I/O bus
- ▶ 64k-word external address space
- ▶ 6-level hardware stack
- ▶ 2 output, 2 input pins
- ▶ 3 external interrupts
- ▶ 10-MHz clock, static design
- ▶ 1-cycle MAC, MPY, ACCUM
- ▶ 15-cycle DIV
- ▶ 1-cycle external-memory R/W (adds cycle to instruction execution)
- ▶ Zero-overhead looping for MAC addressing; auto-increment
- ▶ 2 to 256 modulo addressing
- ▶ 2 input pins for conditional branch test
- ▶ 8-cycle max interrupt latency

☐ **VENDOR CONTACTS**

Zilog Inc, Campbell, CA, (408) 370-8000. **Circle No. 505**
Product Support BBS: (408) 437-8024 (N,8,1).

ARCHITECTURE



The Z89C00 has a compact, accumulator-based DSP architecture and a single-cycle MAC unit. Two RAM blocks hold program coefficients and data, which feed into the MAC's input registers each cycle. Results land in a product register and 24-bit accumulator each cycle.

The DSP processor runs from an 8-kbyte program ROM, which external program memory supplements. Two internal bus sets—a program address/data bus set and a data address/data set—prevent program thread execution from interfering with cycle-by-cycle MAC processing. The RAM blocks feed directly into the MAC input registers, thus eliminating the need for a second data-bus set. RAM block addressing automatically increments or decrements the address, which eliminates the need for data-address-generation code for each MAC cycle. Modulo addressing options include modulo 2 to 256 processing loops.

The basic DSP chip has two external buses: an external program bus and an I/O bus; external data must come in on the I/O bus. An external-memory R/W takes one cycle. Running code from external memory takes one additional cycle for each instruction—the data is read in one cycle but is not available for processing until the next instruction cycle.

Zilog designers integrated the DSP engine with a Z8 μC and added peripherals for both processors so that the Z8 can control and monitor external devices and kick off digital signal processing as needed. In this arrangement, the DSP functions as a coprocessor. Data passes to the DSP via a set of mailbox registers. The DSP then signals that it has completed a chore, setting results into the mailbox and triggering a Z8 interrupt. However, the DSP is more than a purely functional coprocessor. It has its own peripherals, including timers, ADCs, and DACs; can time its processing; and can take in, process, and return analog data.

Halt pin—If pulled high with the clock, the halt pin will stop DSP CPU trace and start executing NOPs. Halts CPU until it gets an interrupt.

Addressing modes—Direct (to 512 RAM words), indirect (to RAM or ROM with pointer regs), immediate, short-form direct (uses 16-bit data registers in RAM), external peripheral addressing (1 cycle, treats peripheral as a reg).

Special instructions—Absolute value of accumulator, increment/decrement accumulator, compare register to accumulator, multiply and add, multiply and subtract, push and pop system stack.

☐ **VARIATIONS**

Z89C00—10-MHz DSP core with two 512-byte RAM blocks, 8-kbyte ROM.

Z89320—Low-cost version; has one 16-bit external bus, 10-MHz clock; 40-pin DIP, 44-lead PLCC.

Z89321—320 with a codec interface (20 MIPS).

Part no.	Clock (MHz)	Mode	Max power (mA at 5V)	Pins, package	Price
Z89C00	10	Run Standby	60 5.5	68-pin PLCC	$5 (50,000)
Z89320	10	Run Standby	60 5.5	40-pin DIP 44-pin PLCC	$2.50 (100,000)

SUPPORT

☐ **HARDWARE** Zilog sells an evaluation board and ICE for the Z89C00, as well as for the combined Z8/Z89 chips.

☐ **SOFTWARE** Zilog fields a C compiler, assembler/linker, simulator, source-level debugger, and application libraries. It also has a TMS320-to-Z89C00 assembly-code translator.

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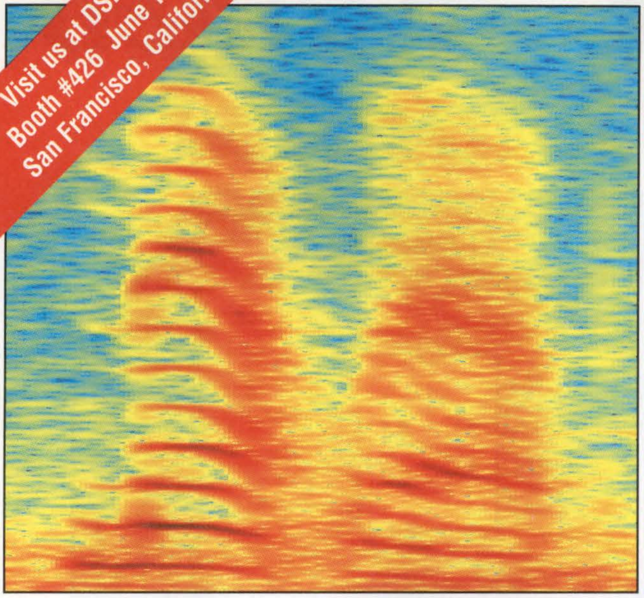
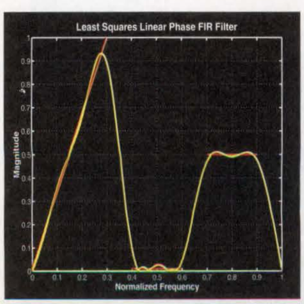


MATLAB simplifies analysis and algorithm development with integrated modeling, design and graphical tools. This spectrogram shows how a speech signal varies with time and frequency.

Speak the language of signal processing with MATLAB®

The MATLAB Signal Processing Toolbox is a powerful interactive environment for signal analysis, algorithm development, and DSP design.



Leading-edge filter design tools make it easy to design filters to fit any specification.

Because its matrix language is ideal for vector processing and data analysis, MATLAB helps you solve the widest range of signal processing problems.

Signal processing power

The Signal Processing Toolbox gives you an unrivaled ability to filter, model, and analyze signals and time-series data. Powerful functions let you perform FFTs, spectral estimation, and filter design in a single step, and display the results automatically.

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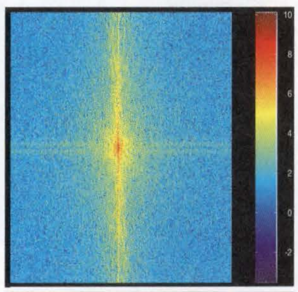

Visualization of a 2-D FFT. Efficient FFT algorithms form the basis for powerful spectral analysis and estimation functions.

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CIRCLE NO. 9

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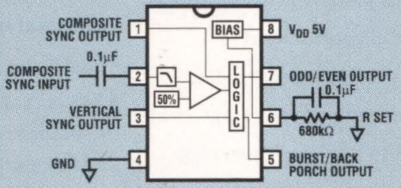
EL4581C
Video Sync Separator



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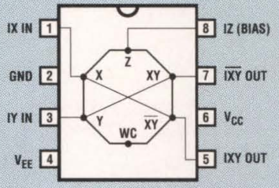
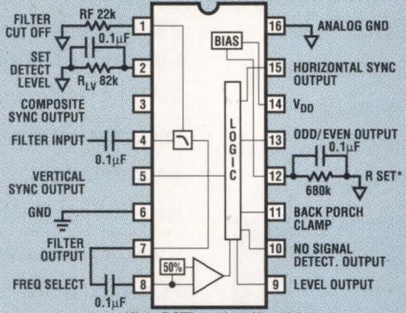
- Low Power CMOS (1.5 mA Max)
- $2.67 in 1,000's P-DIP

EL4083C
Current Mode 4-Quadrant Multiplier



- 200 MHz Bandwidth
- THD < 0.1% @ 10 MHz
- $6.90 in 1,000's P-DIP

EL4583C Video Sync Separator



*Note: R SET must be a 1% resistor

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- Precision 50% Slicing
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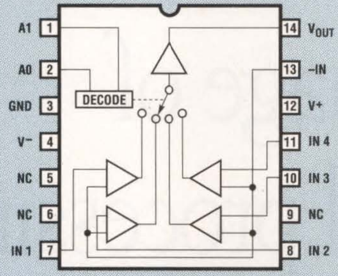
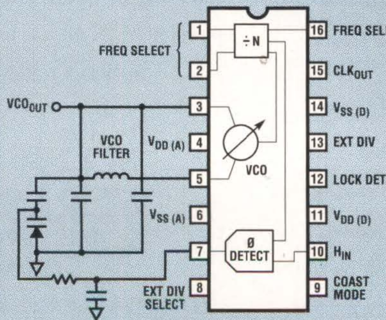


- 8 ns Switching Time
- 0.02%/0.02° Diff Gain/Phase
- $4.71 in 1,000's P-DIP

EL4584 Genlock



- Selectable 8-Preset Frequencies
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- $4.71 in 1,000's P-DIP

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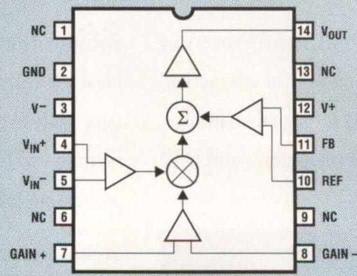

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CIRCLE NO. 124

Zoran ZR38000

16-bit fixed-point DSP

☐ **OVERVIEW** Zoran's ZR38000 is one of the few DSP-chip architectures developed for a specific application class and in tandem with a technology user, Dolby Laboratories. The ZR38000 is aimed at applications in multimedia audio and video, but the company is developing multiple application-specific DSP chips (ASDSPs) based on the original ZR38000. These variations include 6- and 2-channel Dolby AC-3 audio decoders and a 2-channel MPEG-1 audio decoder. A reduced-ROM ZR38000 variation substitutes 1k×32-bit code RAM and 1.5k×20-bit coefficient ROM.

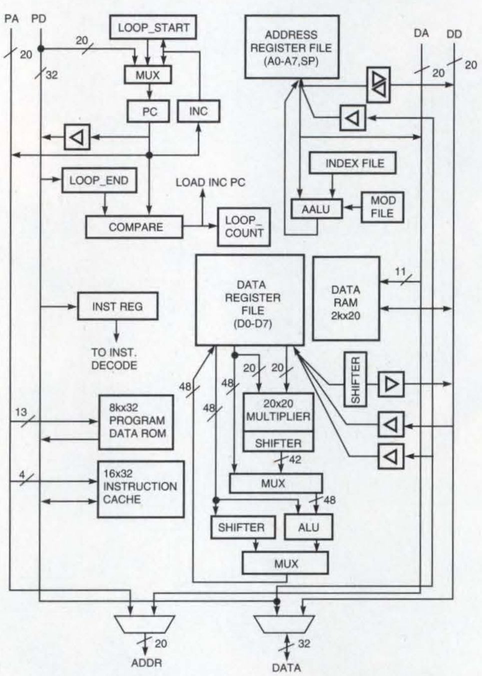
The ZR38000 borrows heavily from RISC technology but simultaneously incorporates a number of standard DSP features. Zoran takes advantage of a 32-bit wide-word instruction to streamline processing but relies on a 20-bit data word for better-than-16-bit resolution. Like RISC and other processors, the ZR38000 is a load/store, register-oriented architecture that lends itself to straightforward coding. The ZR38000 incorporates 8k words of 32-bit program ROM with 2k 20-bit data RAM for data. It delivers a 40-nsec MAC, a 0.88-msec 1024-point complex FFT, 160-nsec Radix-2 FFT Butterfly.

ZR38000

- 32-bit instruction, 20-bit data words, 34 instruction
- 3-stage pipeline
- 16-bit instruction cache
- 8k×32-bit code ROM
- 2k×20-bit data RAM
- 20×20-bit multiplier
- 48-bit ALU
- 8 20-bit data register file (3 reads, 2 writes/cycle)
- 25 20-bit address register file
- 48-bit barrel shifter
- 20-bit (1M-word) address space
- 25-MHz crystal oscillator
- PLL, 2× internal clock (50 MHz)
- 25 MIPS peak
- 4-cycle Radix-2 Butterfly inner loop
- 877-μsec 1024-point, Radix-3 complex FFT
- 20-bit precision (120-dB range)
- 2-cycle, 20-bit normalization
- Modulo, FFT bit-reversal addressing
- 2 data address generators
- Zero-overhead looping

☐ **VENDOR CONTACT**
Zoran Corp, Santa Clara, CA. (408) 986-1314. **Circle No. 506**

ARCHITECTURE



Zoran's ZR38000 integrates high-speed RISC design techniques with DSP-specific hardware features. To minimize decoding and instruction overhead, Zoran relies on a 32-bit instruction word. However, to minimize costs and provide sufficient math resolution, the ZR38000 has a 20-bit data word with a 1M-word address space. The DSP chip can hold up to 8k 32-bit instruction words and 32 kbytes of code in ROM (or RAM in some versions); it also has a 2k×20-bit data RAM.

Similar to Analog Devices DSPs, the ZR38000 has a small, on-chip instruction cache. Its 16×32-bit cache holds the last sixteen instruction words executed. Running from the cache, the CPU can start an instruction every cycle; it has a short, 3-stage pipeline, with instruction fetch, instruction decode, and execute stages. The hardware uses a RISC-like delayed branch: the delayed-branch instruction will execute the next two instructions before it takes a branch.

Similar to most DSPs, the ZR38000 architecture supports multiple operations per instruction cycle. For MAC class cycles, it can generate two data addresses per cycle, as well as fetch the next instruction. For dual data addressing, the chip has two data address generators and has an 8×80-bit address register file. Using a basic 50-MHz internal clock (up from 25 MHz), the hardware can access its on-chip RAM twice during a single, 40-nsec cycle. Thus, the processor can make do with a single data RAM, even for dual-access MAC operations. The hardware supports FFT bit reversal and modulo addressing for DSP processing. It incorporates zero-overhead looping, with up to four stacked loops (as long as they have separate end addresses).

An address register file (ARF) expands addressing capabilities: It incorporates a 20-bit stack pointer and eight address sets. Each address set consists of three registers: a 20-bit address, a 20-bit index, and a 20-bit modulus register. The hardware supplies a range of addressing options, including direct and indirect addressing (both with increment/decrement), indexed, bit-reversed, or circular modulus options. For table walking, you can postincrement/decrement by one or by an index value. You can also use the ARF registers as general registers or for I/O.

Arithmetic operations center on a multiport register file. This file can handle up to three reads and two writes per cycle, enabling the hardware to read data for the next operation while returning results for the current operation. The register file has eight 20-bit registers. Two of the registers are extended to 48 bits to support 48-bit accumulation (40-bit data, 8-bit overflow). The hardware incorporates a 48-bit ALU, a 20×20-bit multiplier, and step division. Some instructions integrate multiple operations to perform common DSP functions.

The ZR38000 supports a 20-bit, 1M-word, unified program/data address space. The chip has 20-bit external address bus and a 32-bit external data bus. Internally, the chip builds on a dual bus system with a 20-bit data address bus and data bus set, and a 20-bit program address bus and 32-bit data bus set. The hardware feeds the external address bus by multiplexing the internal program and data address buses. Similarly, the external data bus links through a bidirectional multiplexer to the 32-bit program data bus and 20-bit data bus. The ZR38000 supplies six serial I/O ports that suit multimedia applications.

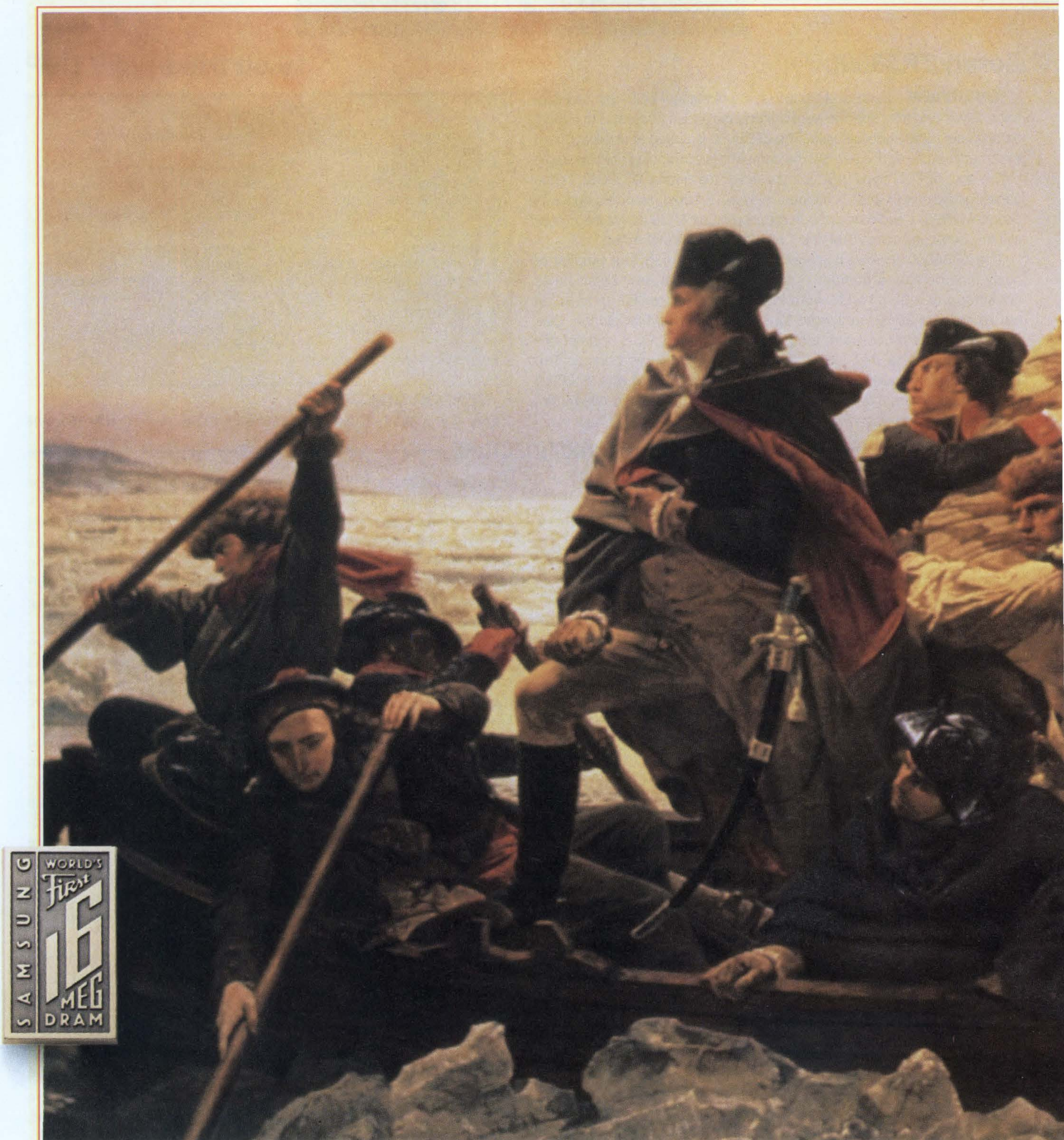
Special instructions—Absolute Value, Butterfly Primitive (multiplies 2 registers, stores registers, and intermediate sum), Compare, Compare Absolute, Delayed Branch (executes next two instructions before branch), Increment/Decrement, Divide Iteration (bit step), Loop, Multiply-and-Add/Sub, Move Max/Min (moves max/min value from array), Normalize (also for max mantissa), and Repeat Instruction.

Part no.	Clock	Max power (5V)	Package	Price
ZR38000	25 MHz	300 mA	128-pin PQFP	$42 (1000)

SUPPORT

☐ **HARDWARE** Zoran sells a ZR38000 development board. PC-AT ISA-bus compatible, the board can be dropped into a standard PC-AT (and above). It comes with 128k×32-bit, 24.5-MHz, zero-wait-state external memory. It has an interface to external analog systems.

☐ **SOFTWARE** Zoran supplies a software-development tool set, which runs on MS-Windows 3.1 on a 386- or 486-based PC. The tools include an assembler/linker, a simulator, and a debugger. Zoran has developed MPEG-1 utilities for decompression/compression (32-, 44.1-, 48-kHz sampling rates; 32- to 48-kbps compressed bit rates).


SAMSUNG
WORLD'S
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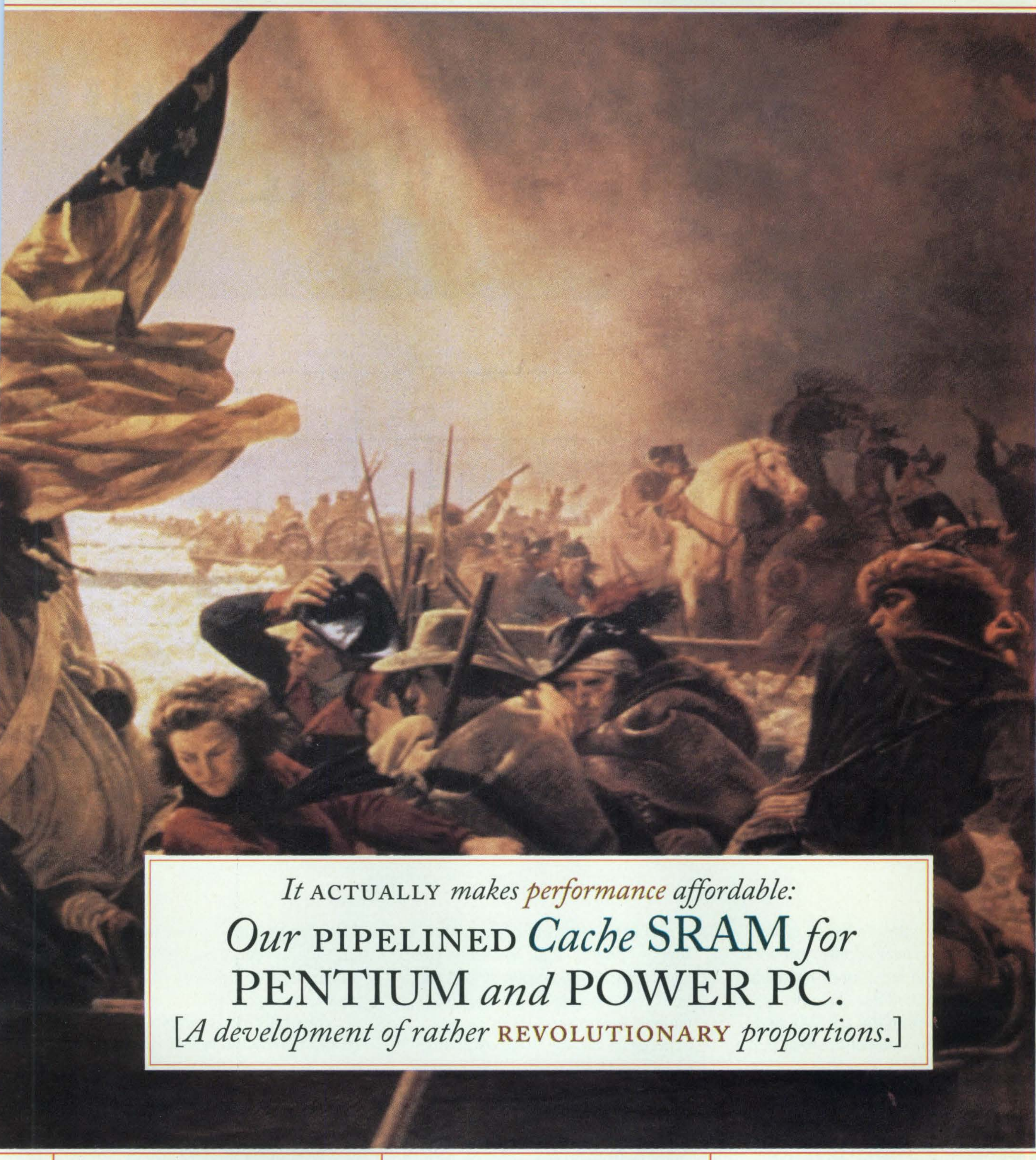
16
MEG
DRAM



This revolutionary design was developed collaboratively with major systems developers. It has already met with wide acclaim throughout the industry, and is second-sourced. It will support 3.3 volt systems up to 75 MHz, and is available in speeds of 7, 8, and 9ns.

For Samsung, the pipelined burst cache SRAM is just one of many notable achievements in memory—in a program that sails forward with remarkable success.

For information on designing it in, please call 1-800-446-2760 or 408-954-7229 today. Or write to SRAM Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, CA 95134.

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CIRCLE NO. 102

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

PC and DSP μP interrupt each other

Jerzy R Chrzaszcz, Institute of Computer Science, Warsaw, Poland

BBS

Efficient synchronization and communication between a PC bus and an add-on board is important for virtually all applications—but is essential to DSP boards such as those that use the TMS320C25. A bidirectional register mapped in I/O space at the DSP side and decoded in I/O channels at the PC side provides this efficiency and is simple and flexible. **Listing 1** describes control logic for such a register encapsulated in a low-cost GAL20V8 that allows for polled and interrupt-driven service. When enabled, the register generates DSP-to-PC or PC-to-DSP interrupts on data reads or writes. Jumpers or the control register can set four interrupt enables. To allow for polled service at the PC side, additional flags indicate register reads and writes executed by the DSP μP.

The design's interface to the PC bus requires eight locations. (This design doesn't include the decoding functions.) Because a 320C25 distinguishes only 16 I/O ports, the design uses four address lines for decoding at the DSP side. Separate flags are set when the DSP μP writes and reads data to and from the register. The flags clear when the PC resets and whenever the PC reads data from an I/O location designated as the status register. You can easily modify addresses by editing the "refine" statements in the source file. (You also have to make the appropriate changes in the simulation input file to generate valid test vectors.) For ISA compatibility, the "irq86" interrupt-request line needs an open-collector buffer. The **listing** posted on the *EDN* bulletin-board system includes a simulation file. (DI #1439) EDN

To Vote For This Design, Circle No. 340

Listing 1—GAL20V8 interrupt controller for ISA add-on board with 320C25

```
Pin 1         =  a0       ;  /* 320C25 address lines                   */
Pin 2         =  a1       ;  /* .                                      */
Pin 3         =  a2       ;  /* .                                      */
Pin 4         =  a3       ;  /* .                                      */
Pin 5         = !is       ;  /* 320C25 i/o space select                */
Pin 6         = !we       ;  /* 320C25 write enable                    */
Pin 7         = !strb     ;  /* 320C25 strobe                          */

Pin 8         = !rd86     ;  /* enable 80x86 interrupt on read         */
Pin 9         = !wr86     ;  /* enable 80x86 interrupt on write        */
Pin 10        = !rd25     ;  /* enable 320C25 interrupt on read        */
Pin 11        = !wr25     ;  /* enable 320C25 interrupt on write       */
Pin 23        =  reset    ;  /* reset from bus connector               */

Pin 18        =  sa0      ;  /* host system address lines              */
Pin 19        =  sa1      ;  /* .                                      */
Pin 20        =  sa2      ;  /* .                                      */
Pin 21        = !hit      ;  /* base address decoded on [sa9..sa3] */
Pin 13        = !ior      ;  /* data read strobe                       */
Pin 14        = !iow      ;  /* data write strobe                      */

Pin 22        = !irq25    ;  /* 320C25 interrupt request               */
Pin 15        =  irq86    ;  /* 80x86 interrupt request                */
Pin 16        =  rdflag   ;  /* data read flag for 80x86               */
Pin 17        =  wrflag   ;  /* data write flag for 80x86              */

$define ISA_DATA 0
$define ISA_STAT 2
$define DSP_DATA 0

field   isa_adr = [sa2..sa0];
isa_hit = hit & isa_adr: 0;
isa_rd  = isa_hit & ior;
isa_wr  = isa_hit & iow;
statrd  = hit & isa_adr: 2 & ior;

field   dsp_adr = [a3..a0];
dsp_hit = dsp_adr: 0;
dsp_rd  = dsp_hit & strb & is & !we;
dsp_wr  = dsp_hit & strb & is & we;

rdflag  = dsp_rd # rdflag & !reset & !statrd;
wrflag  = dsp_wr # wrflag & !reset & !statrd;
irq86   = rd86 & rdflag # wr86 & wrflag;
irq25   = rd25 & isa_rd # wr25 & isa_wr;
```

Autocalibrator nulls dc offsets

Doug Mercer and Steve Ruscak, Analog Devices, Wilmington, MA

Three inexpensive ICs in **Fig 1**'s autocalibration circuit correct for both the ADC's offset errors and systematic dc offsets that accumulate before the converter input. An RS flip-flop, a counter, and a low-cost DAC combine to provide the requisite offset correction voltage. When configured in unipolar mode, IC_1, a 12-bit 1.25-Msamples/sec ADC, has a maximum dc offset of ±9 LSBs, which this autocalibration circuit can reduce to less than ½ LSB.

IC_1 provides an out-of-range (OTR) signal that indicates when the analog input has exceeded positive or negative full scale. This OTR output drives the reset input of IC_{2B}. IC_{2B} and IC_{2C} form an RS flip-flop. The set input to the flip-flop is an external pulse, STRT_CAL, which initiates the calibration sequence. The width of this pulse must exceed one conversion period for proper circuit operation.

When you apply a STRT_CAL to the circuit, a 74HC393 configured as an 8-bit counter (IC_3) resets to zero. Simultaneously, the Q output of the RS flip-flop goes low, allowing an inverted copy of the ADC's sample clock (ENCODE) to gate through IC_{2A}. IC_{2D} inverts the ENCODE pulse such that the counter clocks at the same time as the beginning of conversion. At this point, the analog input of IC_1, AIN1, must be at its zero-level or negative full scale. The current at the IOUTA′ node is equal to

$$\text{I OUT A}' = -\left(\frac{D}{256}\right) * \left(\frac{\text{REF\_OUT}}{R_1}\right) + \approx \left(\frac{\text{REF\_OUT}}{R_2}\right),$$

where D is the digital input code to IC_4's DAC. When D equals 0, the current at IOUTA′ equals approximately 0.5 mA. The resultant correction voltage that the circuit applies to the AIN2 input of IC_1 approximately equals IOUTA′×R_3, or approximately 25 mV. As the ADC performs subsequent conversions, the counter increments by one count, which in turn decreases the voltage at AIN2. Conversions continue until the OTR pin toggles high, indicating that the AIN1 voltage has been level-shifted ½ LSB below negative full scale. Simultaneously, the Q output of the RS flip-flop goes high, which prevents further ENCODE pulses from incrementing the counter. At the maximum count of 255, the voltage at AIN2 is approximately equal to –25 mV. With IC_1's full-scale input range of 5V p-p, each LSB equals 1.22 mV, which corresponds to a maximum correction range of ±20 LSBs. (DI #1444) EDN

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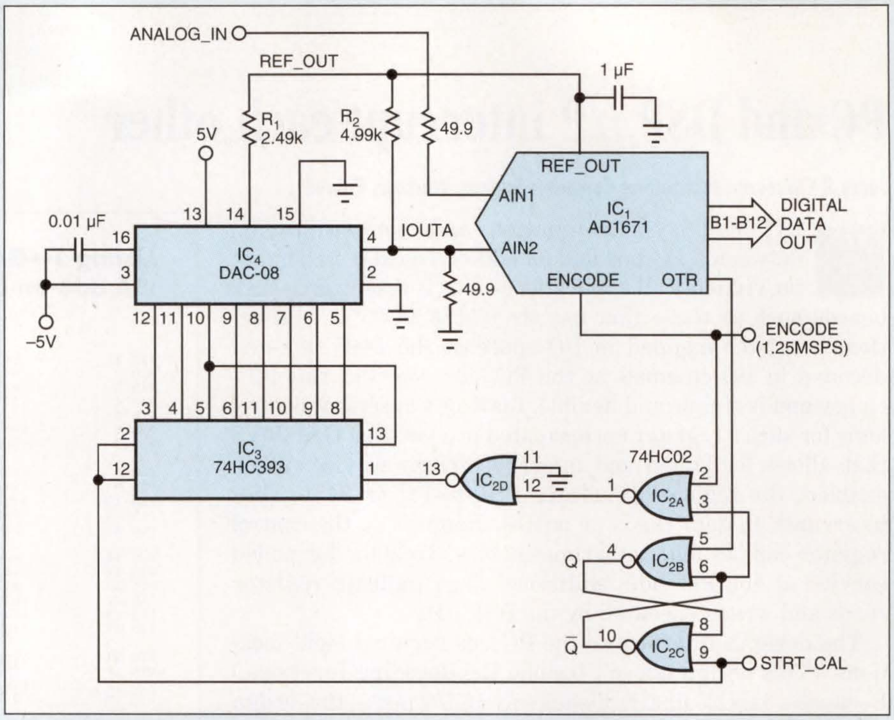

Fig 1—Three inexpensive ICs—an RS flip-flop, a counter, and a low-cost DAC—combine to provide an offset correction voltage for IC_1's ADC, which reduces the uncalibrated offset error from ±9 LSBs to less than ½ LSB.

Low-cost MOSFET quashes power resistor

Christophe Basso, European Synchrotron Radiation Facility, Grenoble, France

At power-on, off-line power supplies use a resistor to provide start-up current for the PWM IC, current that is necessary to start driving the power switch. After a few periods, an auxiliary winding delivers a sufficient voltage to power the IC. Unfortunately, the start-up resistor dissipates heat and raises the power supply's overall temperature. Manufacturers have recently introduced high-voltage MOSFETs to replace the power resistors. Wired as current sources, these

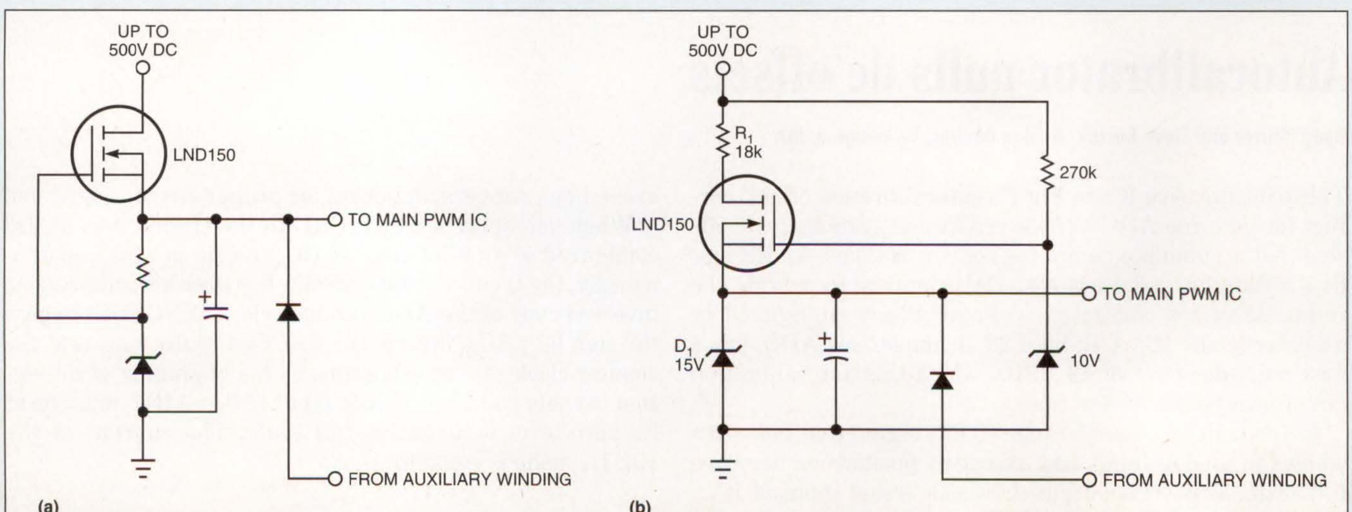

Fig 1—Built-in current sources allow some new MOSFETs to supply a few hundred microamps of start-up current (a). Some minor modifications to the circuit (b) provide much higher start-up currents of a few milliamps.

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UWR-12/1650-D12	9 - 36	12	1650	100	81%	C4	$76
UWR-15/1300-D12	9 - 36	15	1300	100	82%	C4	$76
UWR-5/500-D48	18 - 72	5	500	120	75%	C1	$45
UWR-12/250-D48	18 - 72	12	250	150	76%	C1	$45
UWR-15/200-D48	18 - 72	15	200	150	76%	C1	$45
UWR-3.3/1800-D48	18 - 72	3.3	1800	75	72%	C2	$66
UWR-5/1800-D48	18 - 72	5	1800	75	77%	C2	$66
UWR-12/750-D48	18 - 72	12	750	75	80%	C2	$66
UWR-15/600-D48	18 - 72	15	600	75	80%	C2	$66
UWR-3.3/4850-D48	18 - 72	3.3	4850	100	78%	C4	$76
UWR-5/4000-D48	18 - 72	5	4000	100	80%	C4	$76
UWR-12/1650-D48	18 - 72	12	1650	100	81%	C4	$76
UWR-15/1300-D48	18 - 72	15	1300	100	82%	C4	$76

Case Dimensions: C1 - 1.25" L x 0.80" W x 0.43" H C2 - 2.00" L x 1.00" W x 0.375" H
C4 - 2.00" L x 2.00" W x 0.45" H

Bipolar Models	V_{IN} Range (Volts)	V_{OUT} (Volts)	I_{OUT} (mA)	R/N (mV, p-p)	Efficiency (Min.)	Case	Price (100's)
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BWR-12/830-D12	9 - 36	±12	± 830	100	81%	C4	$76
BWR-15/670-D12	9 - 36	±15	± 670	100	81%	C4	$76
BWR-5/250-D48	18 - 72	±5	± 250	120	73%	C1	$45
BWR-12/125-D48	18 - 72	±12	± 125	150	80%	C1	$45
BWR-15/100-D48	18 - 72	±15	± 100	150	80%	C1	$45
BWR-5/700-D48	18 - 72	±5	± 700	100	76%	C2	$66
BWR-12/415-D48	18 - 72	±12	± 415	75	79%	C2	$66
BWR-15/330-D48	18 - 72	±15	± 330	75	79%	C2	$66
BWR-5/1700-D48	18 - 72	±5	±1700	100	81%	C4	$76
BWR-12/830-D48	18 - 72	±12	± 830	85	81%	C4	$76
BWR-15/670-D48	18 - 72	±15	± 670	85	82%	C4	$76
Triple Models							
TWR-5/1200-12/250-D48	18 - 72	5/±12	1200/250	75/175	81%	C4	$76
TWR-5/1500-12/250-D48	18 - 72	5/±12	1500/250	75/175	79%	C4	$76
TWR-5/1800-12/200-D48	18 - 72	5/±12	1800/200	75/175	81%	C4	$76
TWR-5/1000-15/250-D48	18 - 72	5/±15	1000/250	75/175	79%	C4	$76
TWR-5/1500-15/250-D48	18 - 72	5/±15	1500/250	75/175	81%	C4	$76
TWR-5/1800-15/150-D48	18 - 72	5/±15	1800/150	75/175	80%	C4	$76

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CIRCLE NO. 49

MOSFETs provide the few hundred microamps necessary to start the IC. **Fig 1a** shows a circuit based on the new Supertex (Sunnyvale, CA) LND150. Unfortunately, this configuration isn't sufficient for a main IC that requires start-up current of a few milliamps. For example, this current source cannot start a half-bridge power MOSFET driven by an International Rectifier (El Segundo, CA) IR2110 in off-line fluorescent ballast applications.

A circuit that provides higher current (**Fig 1b**) still uses the LND150, but this time as a high-voltage switch. At power-on, the LND150's positive V_{GS} allows the current to flow through R_1. The source potential starts to rise, authorizing the PWM IC to oscillate. The auxiliary winding begins to deliver voltage and forces the MOSFET's source voltage to rise until D_1 reaches its voltage limit. When the dc rail exceeds the 10V gate voltage, the V_{GS} becomes negative and soon stops MOSFET conduction, thus freeing R_1 from dissipating any heat. The heat dissipated by the resistor thus falls to zero, avoiding all the nuisance caused by excessive heat in the circuit and leading to better overall efficiency. A further enhancement to this circuit would be to lock the MOSFET gate to ground, thus inhibiting all oscillations when the auxiliary power supply disappears, such as when the tube is broken in ballast applications. (DI #1442) EDN

To Vote For This Design, Circle No. 342

Spice plots noise figure

Michael A Wyatt, SSAVD Honeywell Inc, Clearwater, FL

The waveform-manipulation capabilities of modern Spice-based simulators, such as MicroSim Corp's PSpice, make it easy to plot complex functions, such as noise figure. The traditional definition of "noise figure" is "the amount of signal-to-noise degradation a circuit causes." Another definition is "the total-output-noise power divided by the output-noise power due to the source impedance, expressed in decibels." Spice computes the total-output-noise voltage, e_{onoise}, as the root-sum-square voltage of all network noise sources referenced to the output, which corresponds to the equation

$$e_{onoise}=\sqrt{\sum_{1}^{k}\left[(e_{n1}\cdot G_1)^2+(e_{n2}\cdot G_2)^2+\cdots+(e_{nk}\cdot G_k)^2\right]} \quad (1)$$

where e_{nk} is the kth noise contributor and G_k is the associated kth gain. Spice also computes the equivalent input noise e_{inoise}, which would produce the same output noise voltage with a noise-free amplifier as

$$e_{inoise}=e_{onoise}/G_{amp} \quad (2)$$

where G_{amp} is the amplifier gain. Because noise power is proportional to noise voltage squared, you can replace e_{onoise} with $e_{inoise}\times G_{amp}$ to compute noise figure for equal input and output impedances as

$$\text{Noise Figure}=10\cdot\log\left[(e_{inoise})^2/4kTR_{source}\right] \quad (3)$$

where k is Boltzmann's constant (1.38×10^{-23} J/K) and T is temperature in Kelvin (298K at room temperature).

Consider the RF amplifier in **Fig 1a**. Spice computes the total root-sum-square output noise voltage and references it to the input source V_{in}. Spice can then use this noise voltage V_{inoise} with **Eq 3** to display noise figure. For example, entering the equation into PSpice's Probe feature produces **Fig 1b**, a graph of the RF amplifier's noise figure vs frequency. This convenient display is typical of RF semiconductor manufacturers' data sheets, and you can use it to investigate circuit, bias point, and component influences on noise figure. (DI #1440) EDN

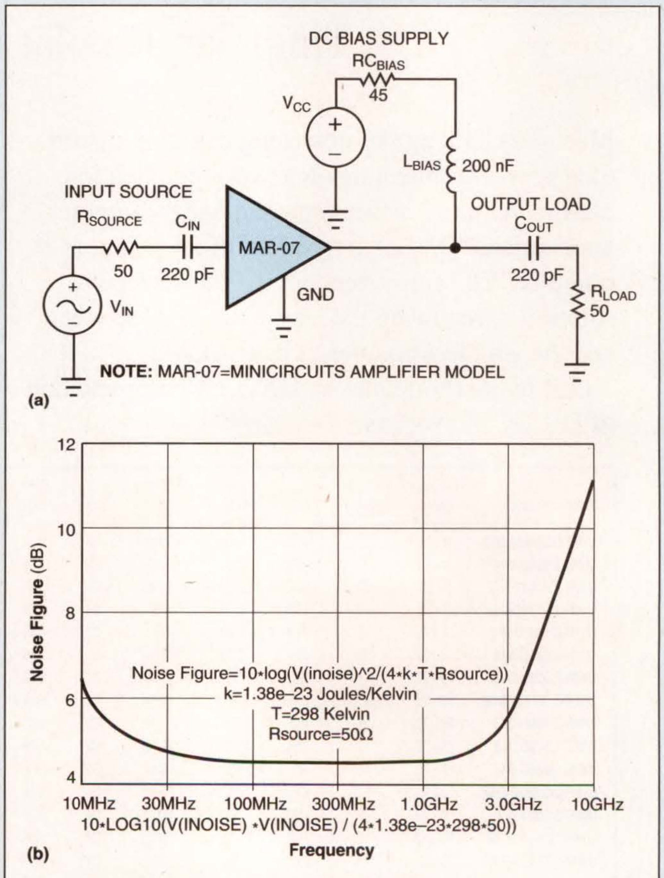

Fig 1—Equations for noise figure and PSpice's Probe feature can plot an RF amplifier's noise figure (a) vs frequency (b).

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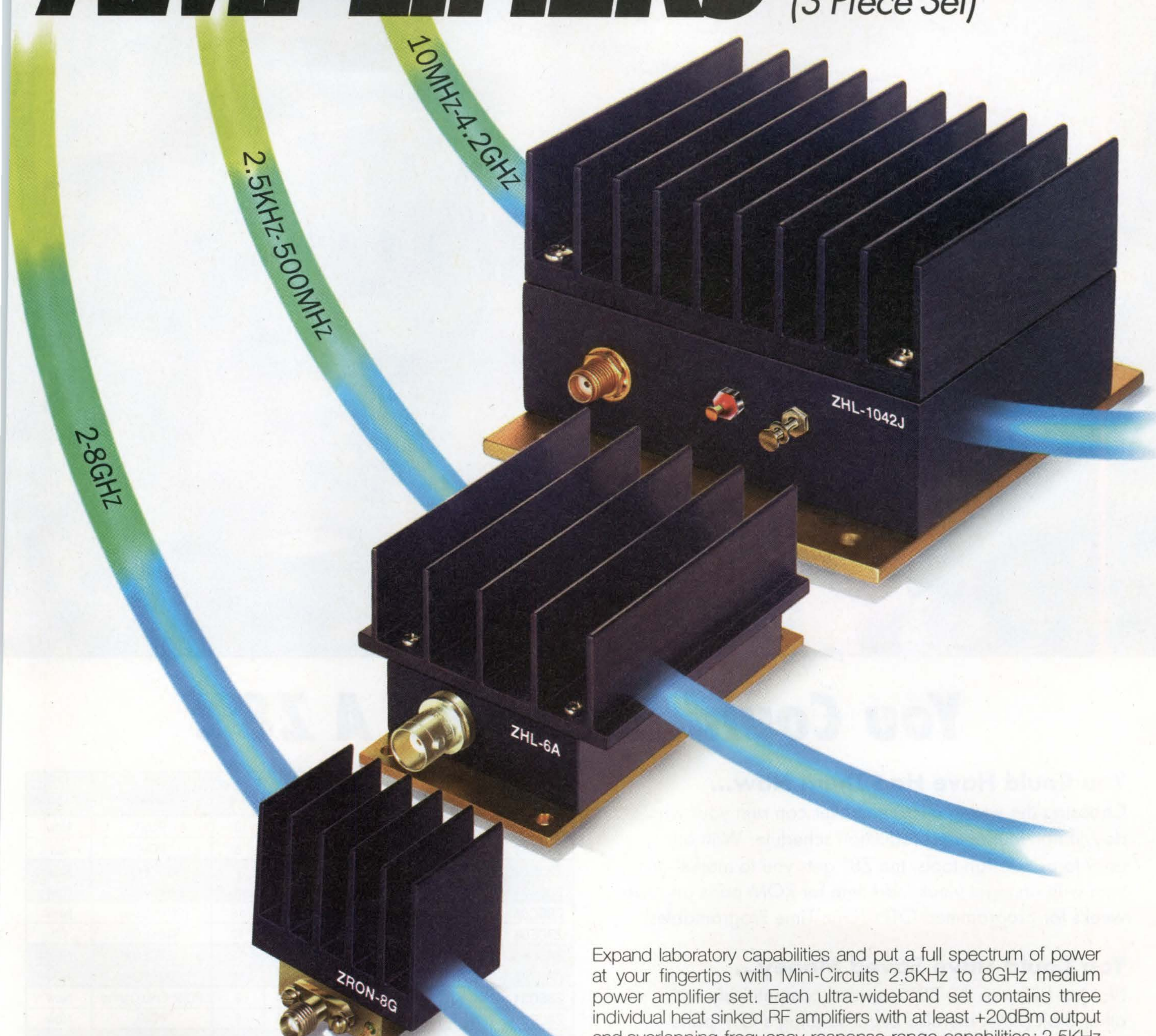

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Z86C04	Masked	18	1K	144	14	8	PDIP, SOIC	Now
Z86E04	OTP	18	1K	144	14	8	PDIP, SOIC	Now
Z86C06	Masked	18	1K	144	14	12	PDIP, SOIC	Now
Z86E06	OTP	18	1K	144	14	12	PDIP, SOIC	Q3
Z86C08	Masked	18	2K	144	14	12	PDIP, SOIC	Now
Z86E08	OTP	18	2K	144	14	12	PDIP, SOIC	Now
Z86C31	Masked	28	2K	256	24	8	PDIP, Chip Carrier	Now
Z86E31	OTP	28	2K	256	24	8	PDIP	Now
Z86C30	Masked	28	4K	256	24	12	PDIP	Now
Z86E30	OTP	28	4K	256	24	12	PDIP	Now
Z86C40	Masked	40/44	4K	256	32	12	PDIP, PLCC, QFP	Now
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CIRCLE NO. 162

DESIGN NOTES

C-Load™ Op Amps Tame Instabilities – Design Note 83

Richard Markell, George Feliz and William Jett

Introduction

By taking advantage of advances in process technology and innovative circuit design, Linear Technology Corporation has developed a series of C-Load op amps which are tolerant of capacitive loading, including the ultimate, amplifiers which are stable with any capacitive load. These amplifiers span a range of bandwidths from 1MHz to 140MHz. They are suited for a wide range of applications from coaxial cable drivers to capacitive transducer exciters.

The Problem

The cause of the capacitive load stability problem in most amplifiers is the pole formed by the load capacitance and the open-loop output impedance of the amplifier. This output pole increases the phase lag around the loop which reduces the phase margin of the amplifier. If the phase lag is great enough the amplifier will oscillate.

External networks can be used to improve the amplifier's stability with a capacitive load but have serious drawbacks. For instance, most designers are familiar with the use of a series resistor R_S between the load and the amplifier output. The optimum value of R_S depends on the load capacitance, so this approach isn't useful for ill-defined loads. Further disadvantages of the external approach include reduced output swing and drive current, and increased component count.

An Example

Figure 1 shows an example of a competitor's medium speed device which is sensitive to capacitive loading. When 50pF is paralleled with a 5kΩ load, the response exhibits considerable ringing. With a 75pF load the device oscillates. By comparison, the transient responses of the 50MHz LT1360 voltage feedback amplifier (Figure 2) shows the improvement in stability achieved in the latest generation of C-Load op amps. In fact the LT1360 maintains a stable transient response for any capacitive load.

C-Load is a trademark of Linear Technology Corporation

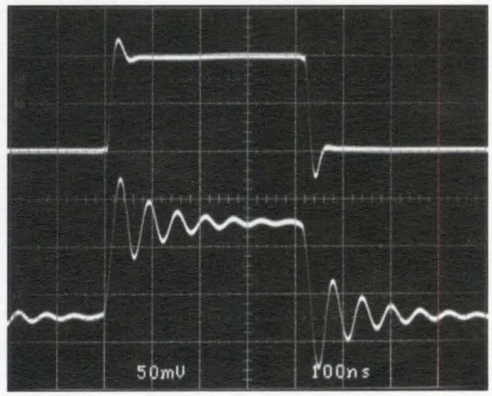

Figure 1. Medium Speed Non-LTC Op Amps

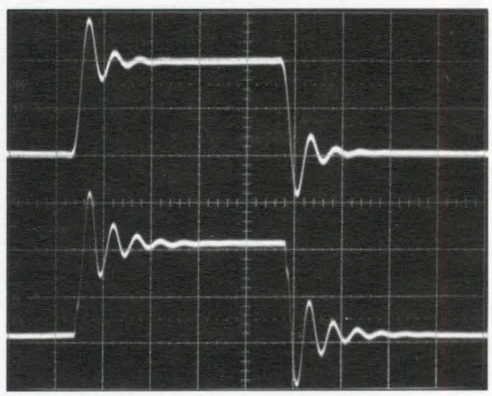

Figure 2. LT1360

The Solution

LTC's new family of voltage feedback amplifiers adjusts the frequency response of the op amp to maintain adequate phase margin regardless of the capacitive load thus, the amplifiers cannot oscillate. These C-Load amplifiers are great in systems where the load is not fixed or is ill-defined. Examples include driving coaxial cables that may or may not be terminated, driving twisted-pair transmission lines, and buffering the inputs of sampling A/D converters that present time varying impedances.

Table 1 lists LTC's *unconditionally stable* voltage feedback C-Load amplifiers. Table 2 lists other voltage feedback C-Load amplifiers that are stable with loads up to 10,000pF. Figure 3 shows overshoot as a function of capacitive load being driven for a wide variety of LTC op amps. Note that the unconditionally stable amplifiers (LT1355, LT1358 and LT1363) have the greatest overshoot for C_L = 10nF. Overshoot actually declines as C_L is increased beyond 10nF.

Table 1. Unity-Gain Stable C-Load Amplifiers Stable with All Capacitive Loads

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1200	LT1201	LT1202	11	1
LT1220	—	—	45	8
LT1224	LT1208	LT1209	45	7
LT1354	LT1355	LT1356	12	1
LT1357	LT1358	LT1359	25	2
LT1360	LT1361	LT1362	50	4
LT1363	LT1364	LT1365	70	6

Table 2. Unity-Gain Stable C-Load Amplifiers Stable with $C_L \le$ 10,000pF

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1012	—	—	0.6	0.4
—	LT1112	LT1114	0.65	0.32
LT1097	—	—	0.7	0.35
—	LT1457	—	2	1.6

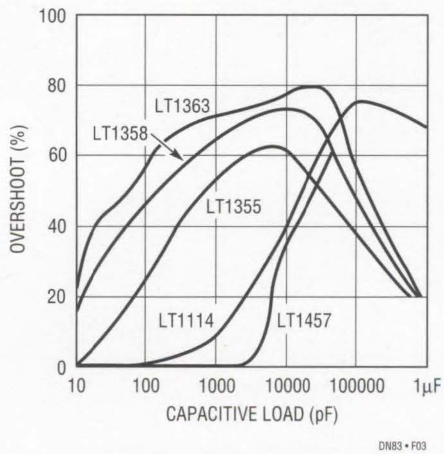

Figure 3. Overshoot vs Capacitive Load

All LTC op amps with adjustable bandwidth can be stabilized for a range of capacitive loads. The bandwidth of current feedback amplifiers is set by the external feedback resistor. Graphs which allow selection of the proper feedback resistor for C_L values to 10,000pF appear in the data sheets of most LTC current feedback amplifiers. As an example, Figure 4 shows the LT1206, a 60MHz current feedback amplifier with 250mA output current, driving loads of 1000pF and 10,000pF while remaining stable.

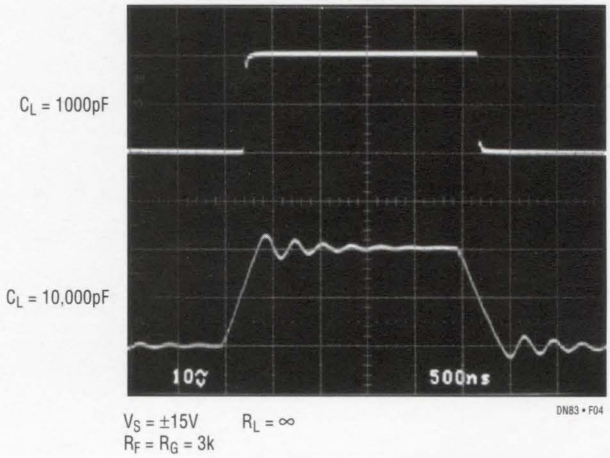

Figure 4. LT1206

Conclusions

Linear Technology has developed families of medium and high speed amplifiers which are much easier to apply than their predecessors. Stable operation with capacitive loads can be achieved without critical external components or loss of output drive. Amplifiers which are stable with any capacitive load are ideal for applications where the load is not well defined. These amplifiers can simplify even low frequency designs by insuring stability under all conditions of loading. For more information on C-Load op amps see the February 1994 issue of *Linear Technology* Magazine.

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Passive components cancel phase errors

Stan Bleszynski, Applied Micro Electronics Ltd, Dublin, Ireland

The circuit in **Fig 1** aims to achieve a constant, frequency-independent delay filter with a very flat amplitude characteristic that is insensitive to input impedance and load resistance. The addition of C_1 and L_1 cancels the nonlinear, third-order term in the formula relating the output phase angle (ϕ) to the frequency (f):

$$\phi = 2 \cdot a\tan\left[\frac{f/f_0}{1-(f/f_1)^2}\right]. \quad (1)$$

First choose R, L, and C such that

$$f_0 = \frac{R}{2\pi L} = \frac{1}{2\pi RC}, \quad (2)$$

where R is the effective resistance and equal to

$$R = \frac{r \cdot R_0}{r + 2 \cdot R_0}. \quad (3)$$

By choosing C_1 and L_1 such that

$$f_1 = \frac{1}{2\pi\sqrt{LC_1}} = \frac{1}{2\pi\sqrt{CL_1}} = f_0\sqrt{3}, \quad (4)$$

$$C_1 = \frac{L}{3R^2}, \quad (5)$$

and

$$L_1 = \frac{R^2C}{3}. \quad (6)$$

the third-order term in the expansion series of **Eq 1** vanishes, leaving only the first-order (linear) term and the fifth- and high-order terms such that

$$\phi = 2(f/f_0) + 0(f/f_0)^5. \quad (7)$$

The time delay (t) between the input and the output is, therefore, expressed by the approximate formula

$$2\pi t = d\phi/df = 2/f_0 = \frac{2L}{R} = \text{constant}, \quad (8)$$

which has an error on the order of 1%, even at frequencies as high as $F_0/2$. Of course, it's normal first to choose R, L, and C to get the required t and then calculate proper values for C_1 and L_1

Two more things worth noting about this circuit are

a. The filter exhibits frequency-independent delay and gain, regardless of the load resistance (r). The load resistance affects the attenuation factor (k) as follows:

$$k = \frac{r}{r + R_0}. \quad (9)$$

b. Input impedance is purely resistive and equal to

$$R_0(r + R_0)/(r + 2R_0), \quad (10)$$

which facilitates cascading the filter.

The following values produce a time delay of 50 nsec: R_0=150Ω, L=3.3 μH, L_1=1 μH, C=150 pF, C_1=47 pF, r=3 kΩ, f_0=7.2 MHz. As **Fig 1** shows, you can connect the output of the filter to a differential amplifier with the gain of 1.05 (1/k) to compensate for the attenuation factor k. (DI #1441)

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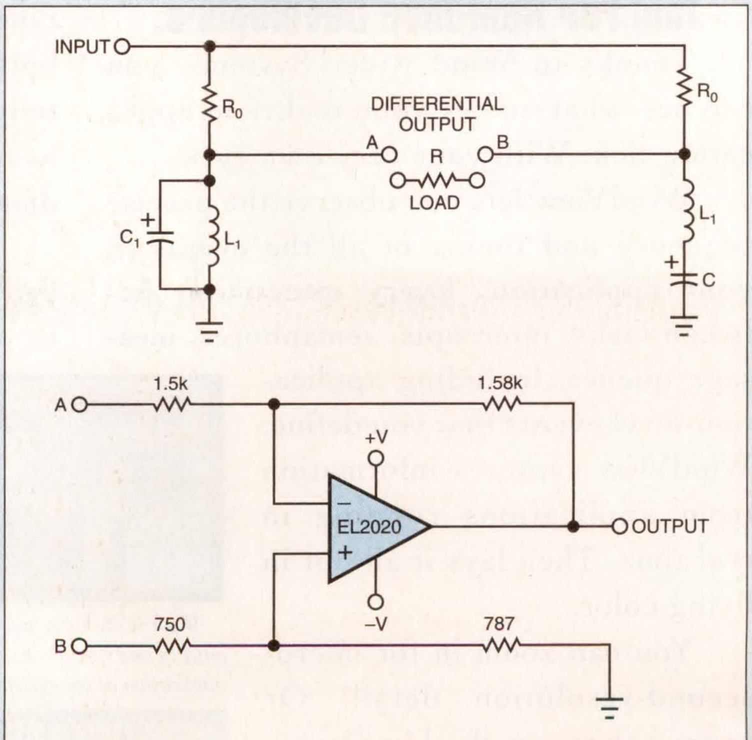

Fig 1—The addition of C_1 and L_1 to this delay filter cancels nonlinear phase-error terms.

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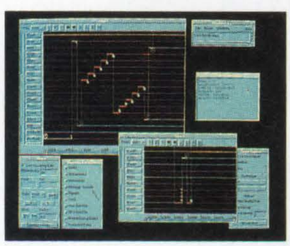

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CIRCLE NO. 114

PLDs substitute for obsolete latches

John R Stauber, Picker International Inc, Highland Heights, OH

The 22V10 series of PLDs in 24DIP300 or 28PLCC packages can substitute both physically and functionally for the now-discontinued 74ALS844 and 74ALS880 latches. Beware, however, that some early PLCC versions of the 22V10 *do not* have compatible pinouts. **Listings 1** and **2** contain the PLDASM source code for 22V10s that emulate the 74AS/ALS844 and 74AS/ALS880, respectively.

Determine whether your application can tolerate the performance differences between the PLDs and the AS/ALS originals. Pay particular attention to the I_{OH} source and I_{OL} sink capability your application requires. 22V10s source and sink only –3.2 and +16 mA compared with the ALS873/880's –2.6 and +24 mA and the AS873/880's –15 and +48 mA. Thus, these PLDs may not be a viable solution if your application drives a bus or a heavy load. Also, select the appropriate speed grade of the PLD, again depending on your application's requirements. The ZIPfile attached to **EDN BBS /DI_SIG #1430** contains the writeup and listings—including simulation specifications. (DI #1430) EDN

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Listing 1—74AS/ALS844 PLD emulation

```
TITLE     74AS/ALS844 Emulator
PATTERN   ???
REVISION  A
AUTHOR    Stauber
COMPANY   Picker International
DATE      02/28/94

CHIP  _74ALS844  PAL22V10

PIN  1      /OC                                        ; INPUT
PIN  2      /D1                                        ; INPUT
PIN  3      /D2                                        ; INPUT
PIN  4      /D3                                        ; INPUT
PIN  5      /D4                                        ; INPUT
PIN  6      /D5                                        ; INPUT
PIN  7      /D6                                        ; INPUT
PIN  8      /D7                                        ; INPUT
PIN  9      /D8                                        ; INPUT
PIN  10     /D9                                        ; INPUT
PIN  11     /CLR                                       ; INPUT
PIN  12     GND                                        ;
PIN  13     C                                          ; INPUT
PIN  14     /PRE                                       ; INPUT
PIN  15     Q9                          COMBINATORIAL ; OUTPUT
PIN  16     Q8                          COMBINATORIAL ; OUTPUT
PIN  17     Q7                          COMBINATORIAL ; OUTPUT
PIN  18     Q6                          COMBINATORIAL ; OUTPUT
PIN  19     Q5                          COMBINATORIAL ; OUTPUT
PIN  20     Q4                          COMBINATORIAL ; OUTPUT
PIN  21     Q3                          COMBINATORIAL ; OUTPUT
PIN  22     Q2                          COMBINATORIAL ; OUTPUT
PIN  23     Q1                          COMBINATORIAL ; OUTPUT
PIN  24     VCC

EQUATIONS

MINIMIZE_OFF

Q1      =  D1       *  C       * /CLR ; Transparent when C high.
        +       Q1 * /C        * /CLR ; Latch data when C low.
        +  D1 *  Q1          * /CLR ; Overlap pterm to prevent glitch.
        +            PRE          ; Output forced high when /PRE low.
Q1.TRST =  OC                   ; Output three-stated when /OC high.

Q2      =  D2       *  C       * /CLR ;
        +       Q2 * /C        * /CLR ;
        +  D2 *  Q2          * /CLR ;
        +            PRE          ;
Q2.TRST =  OC                   ;

Q3      =  D3       *  C       * /CLR ;
        +       Q3 * /C        * /CLR ;
        +  D3 *  Q3          * /CLR ;
        +            PRE          ;
Q3.TRST =  OC                   ;

Q4      =  D4       *  C       * /CLR ;
        +       Q4 * /C        * /CLR ;
        +  D4 *  Q4          * /CLR ;
        +            PRE          ;
Q4.TRST =  OC                   ;

Q5      =  D5       *  C       * /CLR ;
        +       Q5 * /C        * /CLR ;
        +  D5 *  Q5          * /CLR ;
        +            PRE          ;
Q5.TRST =  OC                   ;

Q6      =  D6       *  C       * /CLR ;
        +       Q6 * /C        * /CLR ;
        +  D6 *  Q6          * /CLR ;
        +            PRE          ;
Q6.TRST =  OC                   ;

Q7      =  D7       *  C       * /CLR ;
        +       Q7 * /C        * /CLR ;
        +  D7 *  Q7          * /CLR ;
        +            PRE          ;
Q7.TRST =  OC                   ;

Q8      =  D8       *  C       * /CLR ;
        +       Q8 * /C        * /CLR ;
        +  D8 *  Q8          * /CLR ;
        +            PRE          ;
Q8.TRST =  OC                   ;

Q9      =  D9       *  C       * /CLR ;
        +       Q9 * /C        * /CLR ;
        +  D9 *  Q9          * /CLR ;
        +            PRE          ;
Q9.TRST =  OC                   ;
```

Listing 2—74AS/ALS880 PLD emulation

```
TITLE     74AS/ALS880 Emulator
PATTERN   ???
REVISION  A
AUTHOR    Stauber
COMPANY   Picker International
DATE      02/28/94

CHIP  _74ALS880  PAL22V10

PIN  1      /PRE1                          ; INPUT
PIN  2      /OC1                           ; INPUT
PIN  3      D11                            ; INPUT
PIN  4      D21                            ; INPUT
PIN  5      D31                            ; INPUT
PIN  6      D41                            ; INPUT
PIN  7      D12                            ; INPUT
PIN  8      D22                            ; INPUT
PIN  9      D32                            ; INPUT
PIN  10     D42                            ; INPUT
PIN  11     /OC2                           ; INPUT
PIN  12     GND                            ;
PIN  13     /PRE2                          ; INPUT
PIN  14     C2                             ; INPUT
PIN  15     /Q42                COMBINATORIAL ; OUTPUT
PIN  16     /Q32                COMBINATORIAL ; OUTPUT
PIN  17     /Q22                COMBINATORIAL ; OUTPUT
PIN  18     /Q12                COMBINATORIAL ; OUTPUT
PIN  19     /Q41                COMBINATORIAL ; OUTPUT
PIN  20     /Q31                COMBINATORIAL ; OUTPUT
PIN  21     /Q21                COMBINATORIAL ; OUTPUT
PIN  22     /Q11                COMBINATORIAL ; OUTPUT
PIN  23     C1                             ; INPUT
PIN  24     VCC

EQUATIONS

MINIMIZE_OFF

Q11      =  D11        *  C1 * /PRE1  ; Transparent when C1 high.
         +       Q11 * /C1 * /PRE1  ; Latch data when C1 low.
         +  D11 *  Q11        * /PRE1  ; Overlap pterm to prevent glitch.
         +                PRE1  ; Output forced low when /PRE1 low.
Q11.TRST =  OC1                 ; Output three-stated when /OC1 high.

Q21      =  D21        *  C1 * /PRE1  ;
         +       Q21 * /C1 * /PRE1  ;
         +  D21 *  Q21        * /PRE1  ;
         +                PRE1  ;
Q21.TRST =  OC1                 ;

Q31      =  D31        *  C1 * /PRE1  ;
         +       Q31 * /C1 * /PRE1  ;
         +  D31 *  Q31        * /PRE1  ;
         +                PRE1  ;
Q31.TRST =  OC1                 ;

Q41      =  D41        *  C1 * /PRE1  ;
         +       Q41 * /C1 * /PRE1  ;
         +  D41 *  Q41        * /PRE1  ;
         +                PRE1  ;
Q41.TRST =  OC1                 ;

Q12      =  D12        *  C2 * /PRE2  ; Transparent when C2 high.
         +       Q12 * /C2 * /PRE2  ; Latch data when C2 low.
         +  D12 *  Q12        * /PRE2  ; Overlap pterm to prevent glitch.
         +                PRE2  ; Output forced low when /PRE2 low.
Q12.TRST =  OC2                 ; Output is three-stated when /OC2 high.

Q22      =  D22        *  C2 * /PRE2  ;
         +       Q22 * /C2 * /PRE2  ;
         +  D22 *  Q22        * /PRE2  ;
         +                PRE2  ;
Q22.TRST =  OC2                 ;

Q32      =  D32        *  C2 * /PRE2  ;
         +       Q32 * /C2 * /PRE2  ;
         +  D32 *  Q32        * /PRE2  ;
         +                PRE2  ;
Q32.TRST =  OC2                 ;

Q42      =  D42        *  C2 * /PRE2  ;
         +       Q42 * /C2 * /PRE2  ;
         +  D42 *  Q42        * /PRE2  ;
         +                PRE2  ;
Q42.TRST =  OC2                 ;
```

PC printer port controls frequency divider

Bogdan Manolescu, Microelectronica, Bucharest, Romania

In **Fig 1**'s circuit, two cascaded synchronous presetable binary counters, IC_1 and IC_2, can derive signals having a frequency of f_{CLK}/N. In the circuit, a simple oscillator generates f_{CLK}; however, you can substitute any triggerable source.

An IBM PC supplies the binary-coded integer divisor N (N=255 max) via eight pins of its printer port. Two additional control lines (pins 1 and 14 of the printer port) provide start and reset functions. The signal that starts the oscillator (COM=0) also enables the first counter, IC_1.

The counters, wired to count down, activate the overflow output of IC_2 when the counters reach zero. The overflow signal then enables the counters' parallel loading of the integer divisor N. The Turbo C++ program in **Listing 1** controls the frequency dividers' operation.
(DI #1431)

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Listing 1—Frequency-divider control program

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>
#include <ctype.h>

#define      OUT_PORT  0x378  /* printer output  port address */
#define      CTRL_PORT 0x37A  /* printer control port address */

int main(void)
{
  int n; char c;
  for (;;)  {
    clrscr();
    printf("Input the divisor (between 1 and 255): ");
    scanf("%d", &n);
    printf("\nStart ? (y/n)");
    if(tolower(getch()=='y')) {
      outportb(OUT_PORT,n);        //send out divisor
      outportb(CTRL_PORT,0x02);   //start oscillator and enable counter1
      printf("\n\n\tStop with any key...\
        \n\tESC to exit...");
      c=getch();
      if(c==0x1b) break;
      outportb(CTRL_PORT,0x01);   //reset the counters
      delay(1);
      outportb(CTRL_PORT,0x03);
      delay(1);
    }
  }
  return 0;
}
```

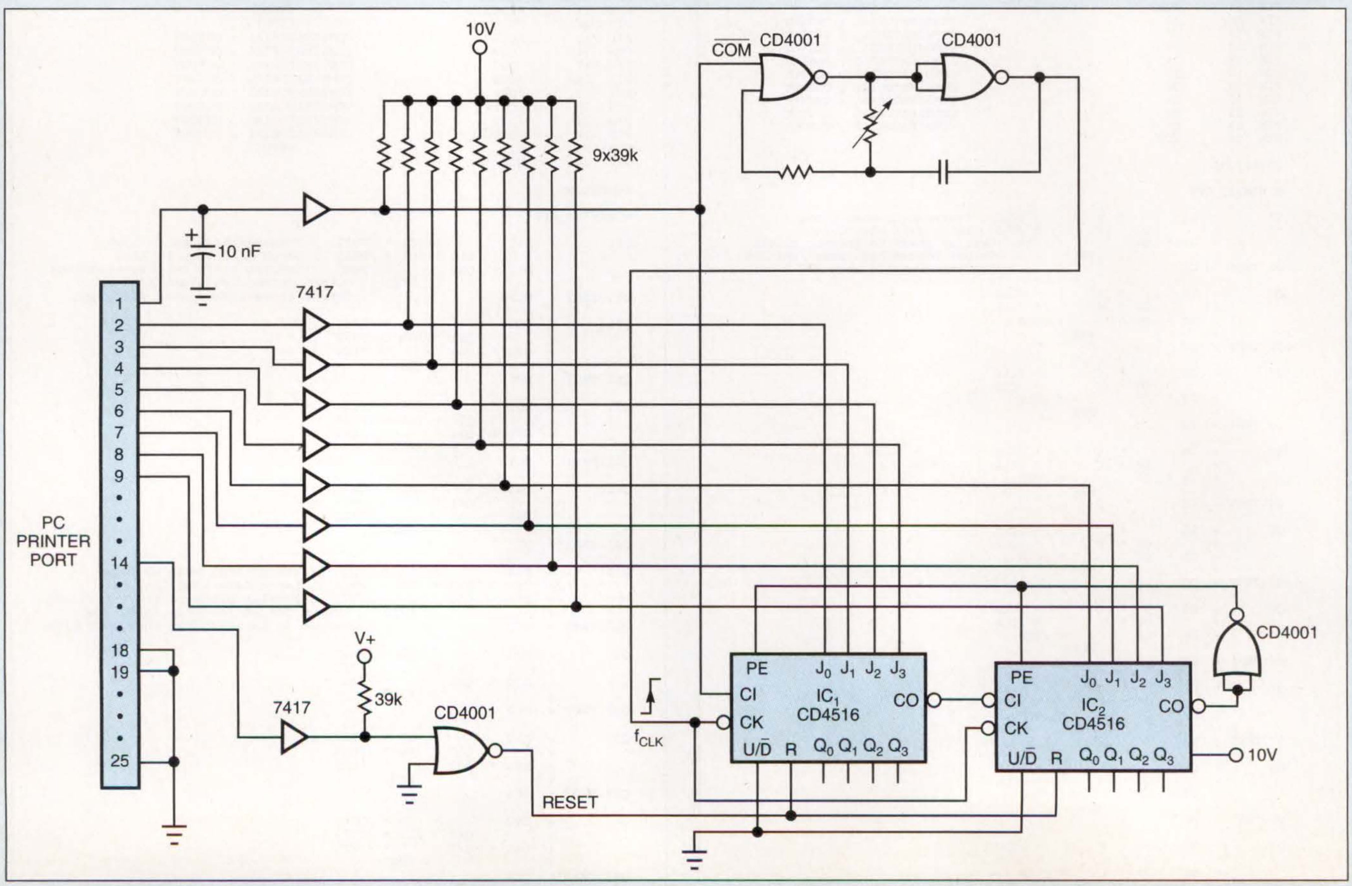

Fig 1—An IBM PC supplies a binary-coded integer divisor circuit to this circuit's pair of synchronous, presettable binary counters.

Printer-port data appears as bar on PC screen

Yongping Xia, EBT Inc, Torrance, CA

BBS Using the circuit in **Fig 1**, a PC's printer port can accept 8-bit parallel data. The 74HC241 in the circuit is a data buffer as well as a high/low nibble selector. The Borland C program in **Listing 1** reads the high and low nibbles, reforming the 8-bit data and converting them to a vertical bar on the PC's screen. Moreover, the program can compare the input data with preset high and low limits, sending the results of this comparison back out through the printer port. You can obtain a copy of the **listing** from **EDN BBS /DI_SIG #1432**. Because the printer port powers the IC, the circuit requires no external power. (DI #1432) EDN

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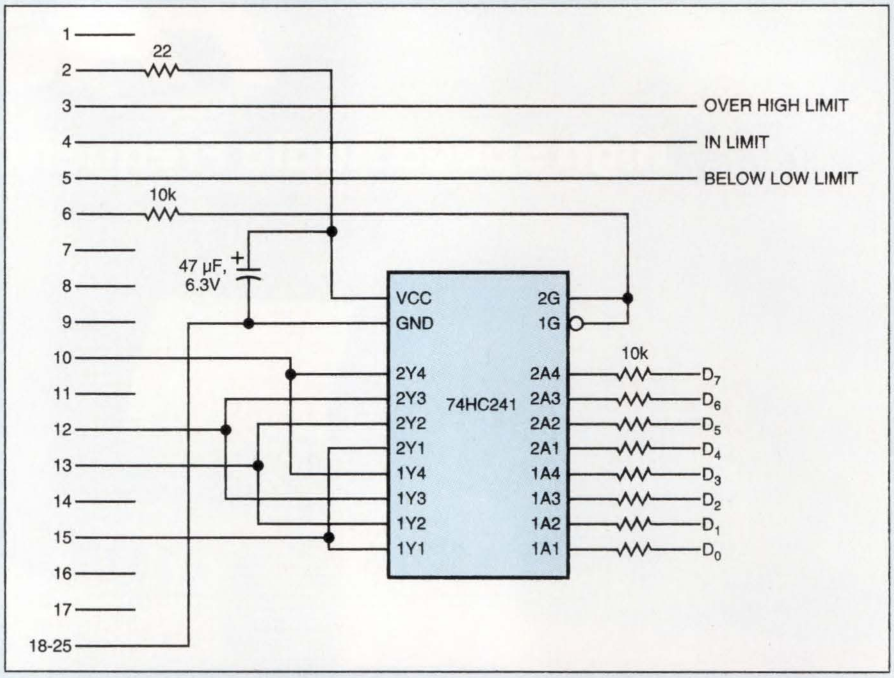

Fig 1—This simple buffer breaks up 8-bit data into a pair of nibbles.

Listing—Command-and-display program for printer-port data buffer

```c
#include <graphics.h>
#include <stdlib.h>
#include <stdio.h>
#include <conio.h>
#include <dos.h>
#include <bios.h>

#define POWER_ON      0x01
#define LOW_4BIT      0xef
#define HIGH_4BIT     0x10
#define CLEAN_OUT     0xf1
#define OVER_LIMIT    0x02
#define IN_LIMIT      0x04
#define BELOW_LIMIT   0x08
#define HIGH          0x90                     /* high limit                  */
#define LOW           0x70                     /* low limit                   */

typedef unsigned int WORD;

int  data, out_port, in_port, out=0;
char msg[80];

main()
{
  find_port();
  init_graph();
  init_screen();
  do {
       out &= LOW_4BIT;
       outportb(out_port, out);             /* set port to read low nibble  */
       data=(inport(in_port)/8)&0x0f;       /* read low nibble              */
       out |= HIGH_4BIT;
       outportb(out_port, out);             /* set port to read high nibble */
       data+=(inport(in_port)*2)&0xf0;      /* combine high and low nibbles */
       out &= CLEAN_OUT;
       outportb(out_port, out);             /* clean comparason output      */
       if (data>HIGH)
   {
    out|=OVER_LIMIT;
    outportb(out_port, out);                /* send out over-limit output   */
   }
       else if (data<LOW)
   {
    out |= BELOW_LIMIT;
    outportb(out_port, out);                /* send out below-limit output  */
   }
       else
  {
   out |= IN_LIMIT;
   outportb(out_port, out);                 /* send out in-limit output     */
  }
      setviewport(0, 0, 639, 479, 1);
      setfillstyle(1, RED);
      bar(70, 30, 85, 286-HIGH);            /* display over-limit bar       */
      setfillstyle(1, GREEN);
      bar(70, 286-HIGH, 85, 286-LOW);       /* display in-limit bar         */
      setfillstyle(1, RED);
      bar(70, 286-LOW, 85, 286);            /* display below-limit bar      */
      line(70, 286-data, 85, 286-data);
      line(70, 285-data, 85, 285-data);     /* display data mark            */
       setviewport(68, 320, 95, 340, 1);
       clearviewport();
       sprintf(msg, "%d",data);
       outtext(msg);                        /* show data on screen          */
       delay(100);
     } while (!kbhit());                    /* quit if any key hit          */
  clean_up();
  return 0;
}

init_screen()                               /* initialize display screen    */
{
  setbkcolor(BLUE);
  setcolor(WHITE);
  line(2,2,637,2);
  line(5,4,634,4);
  line(2,2,2,477);
  line(5,4,5,475);
  line(5,475,634,475);
  line(2,477,637,477);
  line(634,5,634,475);
  line(637,2,637,477);
  line(5,350,634,350);
  setviewport(450, 440, 630, 460, 1);
  sprintf(msg, "press any key to quit");
  outtext(msg);
  setviewport(0, 0, 639, 479, 1);
  return 0;
}

init_graph()                                /* initialize graphic mode      */
{
   int gdriver = DETECT, gmode, errorcode;
   initgraph(&gdriver, &gmode, "");
   errorcode = graphresult();
   if (errorcode != grOk)
    {
      printf("Graphics error: %s\n", grapherrormsg(errorcode));
      printf("Press any key to halt:");
      getch();
      exit(1);
    }
   return 0;
}

find_port()                                 /* find printer port's address  */
{
   out_port=*(WORD far *)MK_FP(0x0040,8);
   in_port=out_port+1;
   out|=POWER_ON;
   outportb(out_port, out);                 /* power on                     */
   delay(1000);
   return 0;
}

clean_up()                                  /* close graphic mode           */
{
   closegraph();
   return 0;
}
```

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CIRCLE NO. 113

Simple ADC is surprisingly accurate

Mike Walne, Farnell Instruments, Wetherby, West Yorkshire, UK

The reference voltage in **Fig 1a**'s simple rail-to-rail PWM ADC is the only critical component. The input-voltage range extends from ground to the power rail which also acts as the reference. The circuit is essentially a variation on the classic dual-slope integrator, the slopes being proportional to V_{IN} and $V_{REF}-V_{IN}$. The circuit works well in µP-based systems that have the spare capacity to perform the mark/space measurement and the necessary calculations.

Assuming that there is no loading, the output voltage is a square wave with amplitude equal to V_{REF} and a mean equal to V_{IN}. Provided that the period is much greater than the digital transition times, the principal source of error is the input offset voltage of the op amp. The accuracy is at least 9 bits (and more likely 12) over the full operating-input and supply-voltage range with no trims. Working with a higher supply rail yields better accuracy. You can increase resolution by lengthening the time for the mark and period.

You can also use the circuit to measure the ratio of two resistors R_U and R_L as in **Fig 1b.** The mark/space ratio is then independent of V_{REF} and equal to R_L/R_U. (DI #1443)

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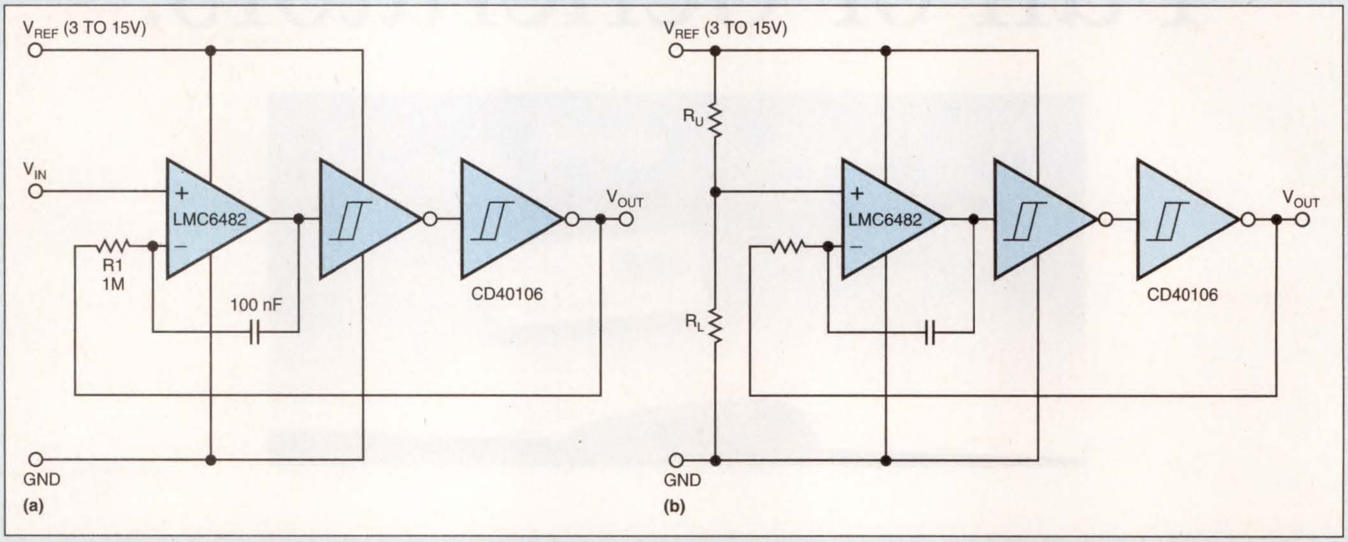


Fig 1—This simple ADC's output (a) is a PWM signal with a mark/period ratio equal to V_{REF}/V_{IN}. The circuit variation in (b) measures the ratio of R_L and R_U.

Precision clamp recovers in nanoseconds

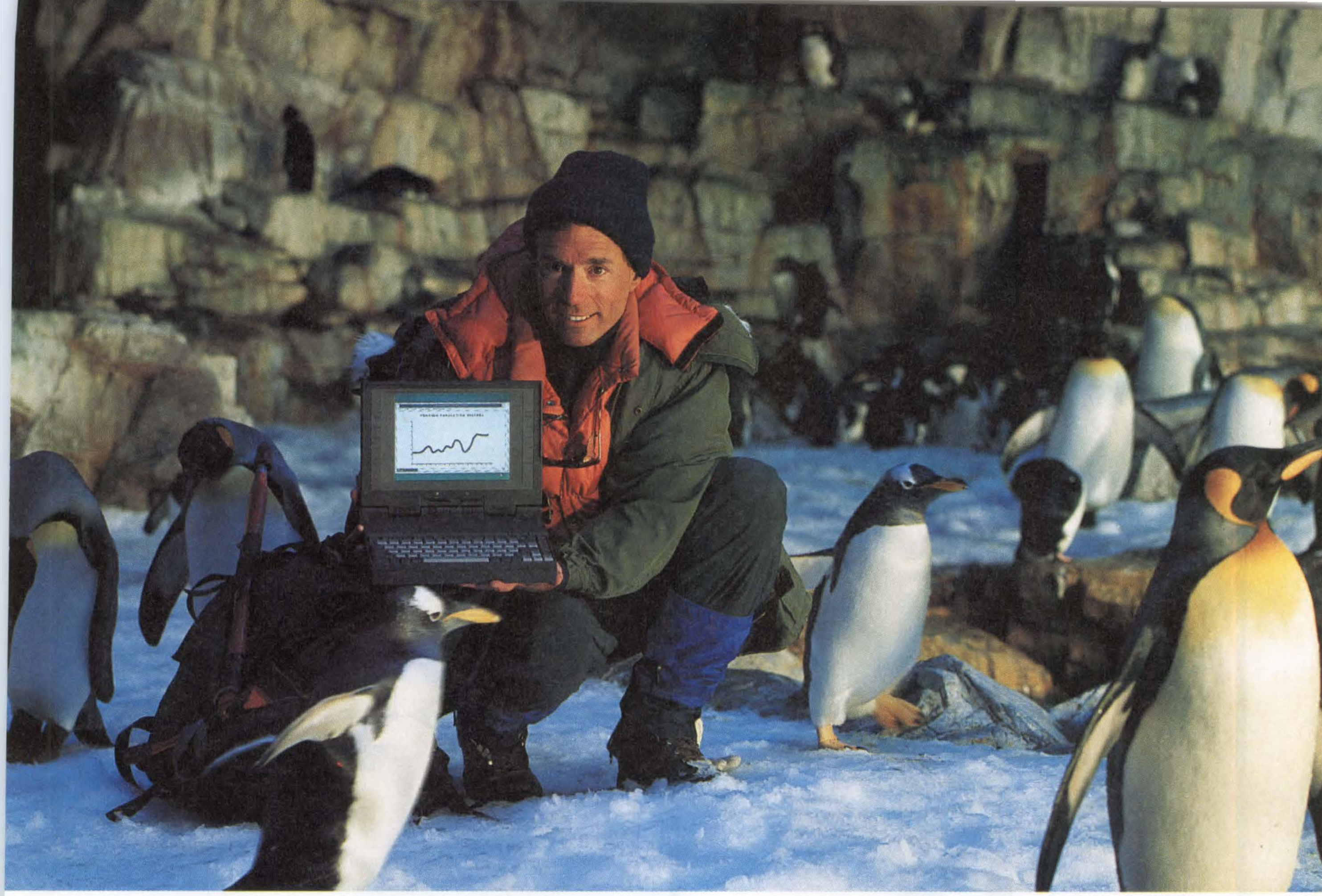
Steven D Roach, Kaman Instrumentation, Colorado Springs, CO

High-speed ADCs sometimes place very strict limits on their allowable input-voltage range, limits that generally require the use of input clamps. Some applications require very temperature-stable clamps that don't interfere with the speed of a 50-MHz amplifier. **Fig 1** shows one such circuit that clamps positive-going voltages to 1.25V at 10 mA, and you can easily adapt it for negative-going voltages and different voltage and current levels. Recovery from the clamped state occurs in about 1 nsec.

This circuit improves on the conventional diode clamp in three major areas. First, the clamping voltage drifts at only a fraction of the –2 mV/C figure of a simple diode clamp. For even lower drift, you can replace the transistors with a monolithic matched pair. Second, by using the emitter of a transistor as the clamping element, the circuit easily obtains a low clamping impedance over a very wide range of frequencies. Third, Q_1 recovers from the clamped state much faster than does a PN junction diode because there is no excess charge storage.

The op amp in the reference-circuit servo controls Q_2 to establish 1.25V at the emitter while carrying exactly 10 mA. The circuit also applies the base voltage of Q_2 to Q_1. Assuming reasonable matching of the transistors, Q_1 clamps V_{OUT} at exactly 1.25V when the clamp reaches 10 mA. This occurs when V_{IN} reaches 2V. (Transistor base currents are assumed negligible in this analysis.) The 47-pF capacitors reduce the clamping impedance of Q_1 at high frequencies.

You can easily modify the clamping voltage and current by changing V_{CLAMP} and R_{BIAS}. The circuit can clamp negative-going voltages using NPN transistors in place of Q_1 and Q_2 and changing the supply-voltage polarity. You can combine NPN- and PNP-based clamping circuits for precision clamp-



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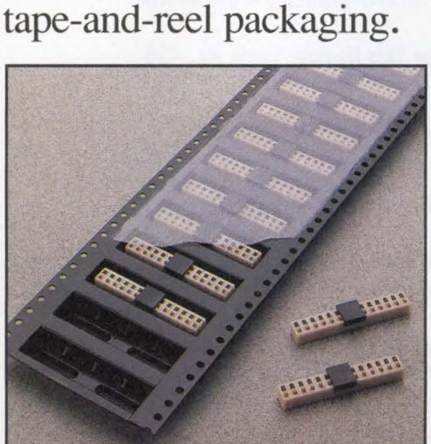

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ing in both directions. When using this circuit, be sure to consider the emitter breakdown voltage of Q_1. (DI #1445) EDN

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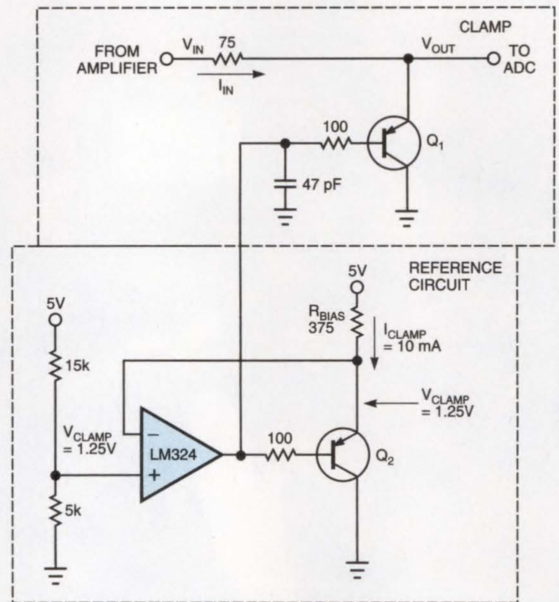

NOTE: $Q_1 = Q_2$ = MMBTH81 RF TRANSISTOR

Fig 1—Compared with conventional diode clamps, this precision clamp circuit has lower drift, provides lower impedance over a wide range of frequencies, and, most important, recovers in nanoseconds.

SOFTWARE SHORTS

Switches simulate chopper

Brian A Freese, Storage Technology Corp
Louisville, CO

Just two switches in the pSpice subcircuit in **EDN BBS /DI_SIG #1409** simulate a chopper circuit. You can modulate positive, negative, or mixed-polarity waveforms.

To Vote For This Design, Circle No. 436

C routine straightens out PC printer-port inputs

William Grill, Riverhead Systems, Littleton, CO

The C routine in **EDN BBS /DI_SIG #1411** allows you to take advantage of the speed of your PC's parallel printer port to input data.

To Vote For This Design, Circle No. 437

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on *EDN*'s bulletin-board system: (617) 558-4241, 310/1210/2410 8,N,1. From Main Menu, enter ss/DI_SIG, then rknnnn, where nnnn is the file referenced above.

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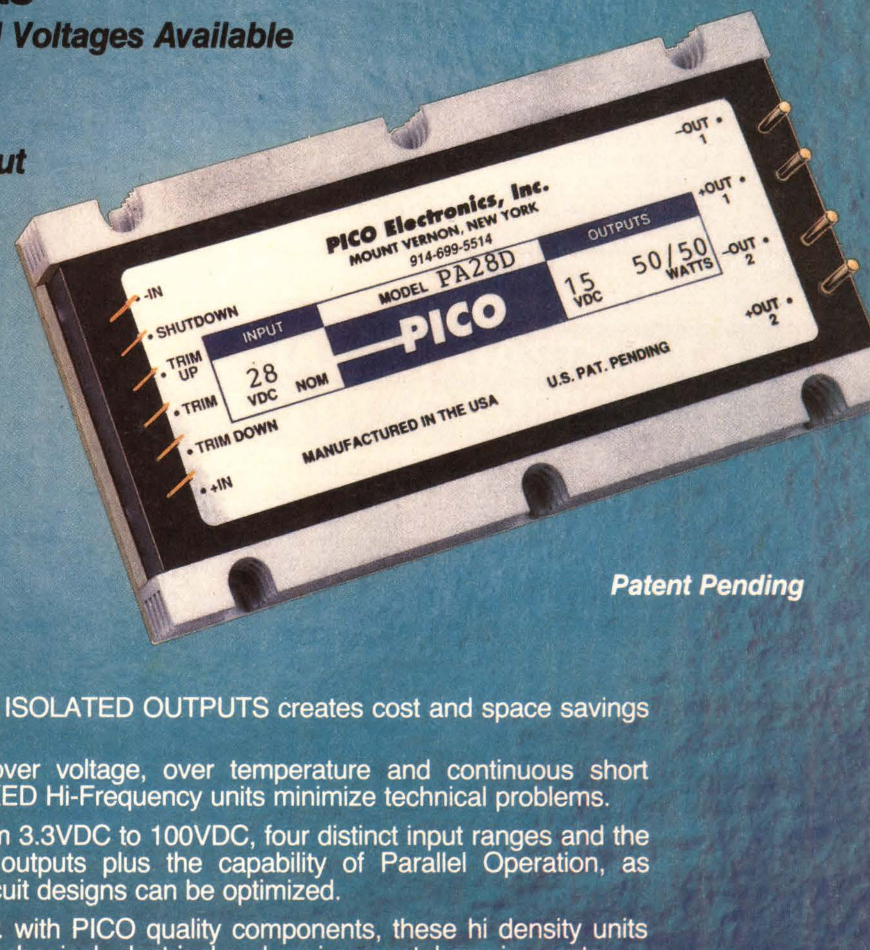

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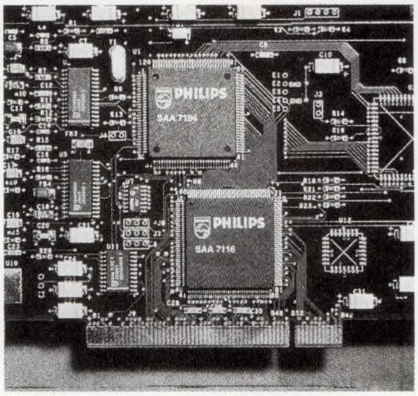
New DTV chip links video input to PCI bus

A new video capture IC serves as an interface between Philips' video capture chipset and the PCI bus. Designed in partnership with Intel, the SAA7116 permits instantaneous live video display from any analog video source directly onto the graphics monitor.

The new IC interfaces directly with Philips' extensive family of digital PAL, NTSC and SECAM video decoder devices including the SAA7196, SAA7110 and SAA7151B. By combining it with the SAA7196, a video image can be scaled to any size on the screen, stored in a hard drive or sent to the CPU for compression, manipulation or processing before storage.

The digitized video, which can be filtered, scaled and translated by the SAA7196, is presented to the SAA7116 in a number of formats, including RGB 5:5:5, YUV 4:2:2 and RGB 8:8:8. The SAA7116 is both a PCI bus master and slave. It operates in master mode to transfer data across the PCI bus and in slave mode to program local registers. The IC generates I^2C control for the rest of the Philips video chipset.

First generation TV-on-PC products kept the video on the add-in board because of the bandwidth limitations of the ISA bus. With the SAA7116 and the throughput capacity of the PCI, video can now stream onto the motherboard. Future applications for the SAA7116 include the possibility of sending video straight from the PCI bus onto a local area network for training, education or general information at the workplace, and the ability to create, manipulate and distribute video images in real time to a number of different nodes on a network.



The SAA7116 video capture IC, designed in partnership with Intel, links video input to PCI bus.

The SAA7116 is an impressive step towards providing speed and facility in manipulating video files on Windows and other platforms.

Call 1-800-447-1500 Ext 1126

For more information on any of these subjects: call 1-800-447-1500 and request appropriate extension number.

All Philips Semiconductors plants worldwide are ISO 9000 certified

Horizontal deflection transistors enhance CRT monitor reliability

The short switching times and low power losses achieved by Philips Semiconductors' two high-speed high-voltage npn power transistors significantly reduce power dissipation in the horizontal deflection circuits of CRT monitors. A narrow gain spread between transistors, resulting from carefully controlled diffusion processes, together with 100% testing of their RBSOA (reverse bias safe operating area) simplify the analysis of worst-case operating and fault conditions, allowing maximum circuit reliability to be designed-in. The BU2522AF and BU2527AF are targeted for use in 14- to 17-inch high-resolution monitors operating at horizontal scan rates up to 64 kHz.

The transistors are 1500 V devices designed to operate at mean collector currents between 5 and 7 A. Their DC maximum and peak collector current ratings are 10 A and 25 A respectively for the BU2522AF and 12 A and 30 A for the BU2527AF. When switching a mean current of 6 A in a 64 kHz horizontal deflection circuit, both transistors show a maximum charge storage time of only 2.0 μs, and maximum collector turn-off fall times are 0.25 μs for the BU2522AF and 0.20 μs for the BU2527AF. These very short switching times are major contributors to the low power dissipation and high reliability achievable.

The transistors are housed in SOT199 plastic power packages with electrically-isolated seating planes which eliminate the need for thermally-conductive washers between transistor and heat sink.

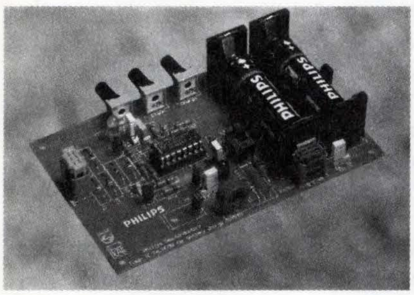
Call 1-800-447-1500 Ext 5015

Philips Semiconductors

First low-voltage IC for economic NiCd and NiMH battery management

A new low-cost LV-HCMOS battery management IC, the 74LV4799, is the first of its kind to be designed for operation from supply voltages between 0.9 and 6 V so that it can be used with one to four rechargeable NiCd or NiMH cells. Intended for 'intelligent' batteries and applications with integrated batteries, the low-power device is ideal for use in domestic appliances, personal care products, cordless tools, personal communications, data handling and many other consumer applications.

An on-chip oscillator, driver and up/down counter maintain a highly accurate log of the battery status and the charge, self-discharge and discharge times. The IC features automatic switchover to trickle charge at the end of the charge time, and can be adjusted to support



A demonstration board is available for evaluating the 74LV4799's performance in various battery charging applications and with different battery types.

virtually all types of rechargeable batteries. Typical charging time is between four and 16 hours.

Battery status indication includes an LED output for charge/battery full indication and a 'nearly empty' output for driving an LED or buzzer. The energy remaining can be detected by using the serial scan output, which represents the status of the internal counter. Built-in power-on reset initiates the IC when the battery is used for the first time or if it is disconnected. For maximum flexibility, the power-on sense input accepts input frequencies from DC to 100 kHz and voltages up to 10 V. The 74LV4799 is supplied in a 16-pin DIL package or in an SO minipack for surface mounting.

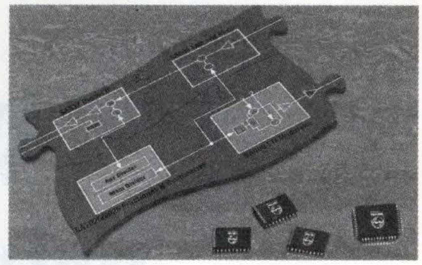
Call 1-800-447-1500 Ext 1127

Low power IS-54 chipset speeds time-to-market

Philips Semiconductors has introduced a low power, highly integrated chipset that meets the IS-54 TDMA (Time Division Multiple Access) North American digital cellular standard. The four-chip set provides designers with a complete radio solution for portable cellular handsets.

The dramatic growth in cellular phone usage has led service providers to convert a portion of their analog channels to a digital format. TDMA allows multiple users to share one channel at the same time, and the IS-54 digital standard provides for an analog link to satisfy those areas that do not endorse the TDMA standard. Dual mode operation requires higher integration and performance than other standards, and the new integrated chipset meets the challenges.

Incoming and outgoing signals are routed from chip to chip with minimum use of power while optimizing connectivity. The four chips are the SA601 RF front end, the SA637 digital IF receiver, the SA7025 dual



The new Philips chipset simplifies the design and implementation of the IS-54 standard.

frequency fractional-N synthesizer and the SA900 I/Q transmit modulator.

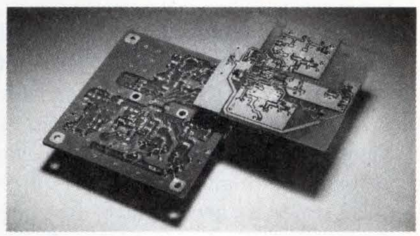
The new chipset offers a number of advantages to the cellular phone manufacturer. By using a low power chipset, designed from the start to work together, engineers can quickly create a phone that will be less expensive, offer longer talk time with fewer batteries, and still meet the exacting requirements of the IS-54 standard.

Call 1-800-447-1500 Ext 1125

Low-voltage low-power frequency synthesizers for mobile communication systems

Three new dual-frequency synthesizer ICs offer the lowest power dissipations per synthesizer currently available, offering operation at supply voltages as low as 2.7 V. Between them, these devices cover the frequency range 50 MHz to over 2 GHz, with each device being optimized for use in particular mobile phone systems. The UMA1015M serves CT1/CT1+ cordless and AMPS/(E)TACS/NMT analog cellular systems, the UMA1018M serves GSM and the UMA1020M DCS1800 and DECT systems. The UMA1020M is the only dual synthesizer in the world to offer over 2 GHz synthesis from a 2.7 V supply. All three synthesizers are also suitable for a wide range of other RF frequency synthesis applications.

All the synthesizers feature two independent frequency synthesis loops, direct drive to a voltage-controlled oscillator, and auxiliary output ports for control of other handset functions. With current consumption of



New dual-frequency synthesizer ICs mean that Philips now provides low-voltage low-power solutions to RF frequency synthesis in handsets for all the latest mobile phone systems.

typically only 10 mA, power-down modes which reduce standby power consumption to just 20 μA, plus high-speed on/off switching capabilities, these ICs can effectively increase time between battery charges in hand-portable telephones.

The synthesizers are programmed via a high-speed, serial interface, allowing the user to control the main and reference dividers, charge-pump operating mode, auxiliary control outputs and power-down modes. The devices are fabricated in Philips' QUBiC BiCMOS process to achieve the necessary combination of high speed and low power consumption.

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Windows NT brings uniformity and low cost to EDA

Bill Fuchs, Simucad

The Windows NT operating environment is a major advancement in the continuing evolution of operating systems and their associated graphical user interfaces.

Windows NT provides a level of integration between operating systems (OSs) and graphical user interfaces (GUIs) the computer industry has never seen before in high-performance systems. Although Apple's Macintosh operating system includes many powerful user-interface features, it lacks the performance high-end users require. Windows NT and NT-based products are about to revolutionize the computer industry, especially engineering software.

The reason for this revolution is simple: Windows NT is very much like Unix—but without most of Unix's problems. Until now, engineers have had to use Unix for high-level design tasks. But, although Unix is available for most high-performance computers, Unix versions are usually unique to each computer. Versions of Unix include Apple Computer's AUX, Digital Equipment's Ultrix, Hewlett-Packard's HP-UX, IBM's AIX, and Sun Microsystems' SUN-OS and Solaris. Xenix and numerous other System V-based Unix variants are available for X86-based PCs. Unix proponents once touted the variety of Unix offerings as its greatest strength. But today, the multitude of versions is one of Unix's most significant handicaps. This situation is particularly true for software developers—especially those software developers who support multiple computer brands.

A clear example of Unix's weaknesses occurred a few years ago when Mentor Graphics decided to support additional workstations along with the Apollo, upon which the company's original Idea system ran. After a lengthy decision, Mentor took a few years to port its products to Sun workstations. Furthermore, Mentor delayed introducing many of its more powerful software products on Sun workstations for more than another year. The result was devastating for Mentor, its shareholders, its stock value, and most important, its loyal customers. It is impossible to determine whether the differences between the Unix OSs and their associated GUIs were the sole cause of the problems at Mentor. Nonetheless, assuming that these differences were responsible for some of the difficulties is reasonable.

For developers who support many computer brands, the nightmare consists of having to maintain a workstation and all of the related, specialized peripherals required to support software development for each hardware system. The following equipment is required to construct a complete software-development environment for a single software developer using a workstation:

- A computer with adequate performance

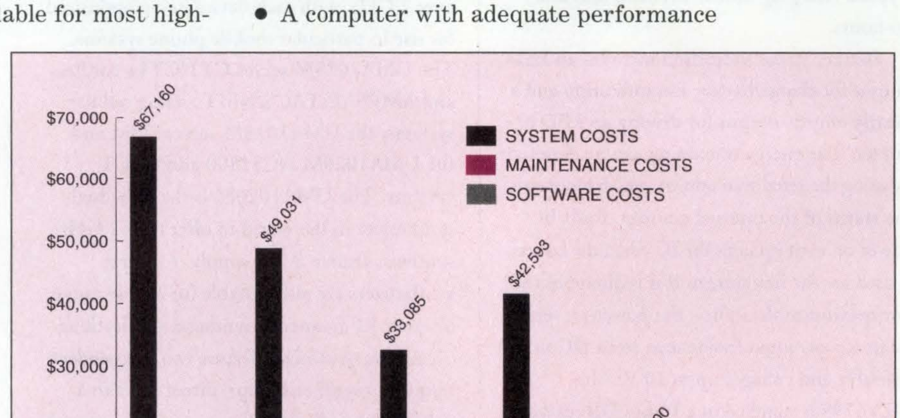

Fig 1—The real cost of a software-development environment includes hardware-system costs, maintenance costs, and software costs.

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- Enough hard-disk capacity for Unix, X (the X Window System), Motif, the system development kit (SDK), and other related development tools and quality-assurance tests
- A CD-ROM drive to load the OS, X, and Motif
- A high-density tape drive to load and offload applications and files
- DAT to handle system backups
- Additional network utilities and system memory to test large-design capacity (required for simulator development)
- Assorted application software such as the Motif SDK, editors, debugging tools, and networking software.

The price for a typical Sun Sparcstation 10 that can handle a task of this scope is about $40,000, not including the application software. The problem is that software developers need a complete configuration for each computer they target for development. If developers choose to support DEC, HP, IBM, and Sun, their development environment could easily cost several hundred thousand dollars, considering the cost of hardware, software, and annual maintenance fees associated with workstations. However, these costs are *not* the most significant limitation to developing under Unix.

Unix's real costs

The real costs associated with developing Unix applications are the time and resources to port software—particularly graphical software—to each architecture's version of Motif, Unix, and X. In addition, whenever you upgrade one of these software modules to a new version, it may create compatibility problems with previous versions (**Fig 1**). The time and resources to coordinate the elements of this development environment directly translate into the extremely high purchase price of Unix-based applications (especially the price of electronic-design-automation (EDA) software). This effort also directly relates to the delay in getting new products, new releases, and updates to market on time.

This problem does not exist with Windows NT running X86 PCs. All PCs run the same version of Windows NT, just as they do DOS and Windows. This similarity means that developers require only one X86 system and its related peripherals to develop under Windows NT. The completed programs run on every X86 PC without recompiling for each brand of hardware. This attribute is an extremely important one of Windows NT, not only from the software developers' perspective, but also from the users' perspective. With a common OS and GUI, users no longer are limited to a specific brand of hardware to obtain the software tools they want.

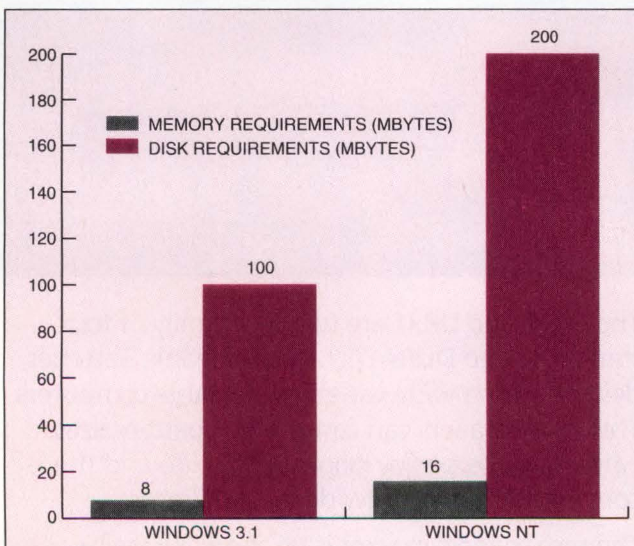

Fig 2—Windows NT turns out not to be the memory hog that some predicted.

The workstations that run Windows NT, such as DEC's Alpha and MIPS R4000/4400, require recompilation of each application's source code. This recompilation occurs because the architectures of the workstations are different from those of the X86-based systems. Although recompilation is necessary, changes to the source code will probably be insignificant, provided that the workstation designers learn from their experiences with Unix and design their hardware to run the standard version of Windows NT.

A clear example of Unix's limitation in this area occurred when Simucad engineers tried to bring up Sun's new Solaris OS on a Sparc 10. Simucad has hundreds of man-years of experience working with various OSs and hardware configurations, but nothing prepared them for this experience.

When Simucad upgraded its Sparc 10, Sun notified Simucad that it had to install Solaris, and that Solaris was compatible with SUN-OS. Simucad's unique development environment, itself built under SUN-OS, should have been easy to port to Solaris. The company has significant in-house expertise and a great deal of knowledge about Sun's products.

Despite that expertise, bringing the development environment up to operational speed took more than five weeks. Sun provided very little assistance, and nobody knew how great a level of incompatibility exists between the two OSs. An even more obvious indication of the software problem was that Simucad engineers were working on the same computer as they had previously worked on. They anticipated having a working version of the company's product under Solaris in approximately four months.

In contrast, using Windows NT provided significant timesaving. Because NT is so new, Simucad had only around four man-years of experience with it vs 30 man-years with Windows and DOS. However, working with a new DEC Alpha system and a MIPS R4000, engineers not only brought up the development environment, but also built a working version of the product—in one day. The product port took 3 hours for the R4000 and 2 hours for the Alpha.

Designing high-performance software to operate in a computer-independent way presents many difficulties. Windows NT will help eliminate most of these concerns. When Simucad embarked on porting the Silos III simulation environment to Microsoft Windows 3.0, Simucad expected to encounter a great deal of difficulty in maintaining the performance advantages it had gained over the last few years.

About three months into the development, a working pre-alpha version of the product, although primitive, was functioning. Simucad's development engineer followed Microsoft's development guidelines for Windows and used the appropriate Windows calls and system tasks, assuring a smooth-running, easily upgradable program.

One of the most interesting results of the initial development effort was an overall improvement in performance over DOS. But, perhaps more important, the final product is much easier to learn and to use than previous versions. Simucad focused on building not only a menu-based system but also a highly intuitive GUI. This interface entailed designing and implementing a system that goes beyond menus, scroll bars, dialog boxes, and mice. It required developing a common-sense GUI—a difficult task for a complex simulation environment.

Most GUIs for complex simulators require the user to memorize many abstract command strings, particularly for some of the more advanced debugging features. In addition, popular simulators, such as Verilog, also require programming knowledge for the more sophisticated aspects. Simucad engineers incorporated these features while staying within the programming guidelines for Windows.

Simucad tested its methods by distributing 100 beta-test versions of a new simulation environment without a single piece of supporting documentation. The results were astonishing. Every one of the 100 beta-test sites was able to use the simulator without difficulty by using their experience with other Windows-based tools. The only questions users asked were how to use the product's advanced debugging features. Simucad then included an on-line, context-sensitive help system, answering many of the users' questions. The Windows SDK supports adapting an intuitive GUI under Windows and Windows NT.

By following the structure of Microsoft's portable coding guidelines, the port from Windows 3.0 to Windows 3.1 was virtually effortless, and Simucad completed the development effort to port to the beta version of Windows NT in less than two months.

Developing under Windows NT offered many similarities to developing under Windows 3.0 and 3.1, but it also required many of the unique development strategies necessary when developing under Unix. Windows NT provides true preemptive multitasking, much as Unix does.

This multitasking requires a developer to consider how multiple versions of the application software can run and display results concurrently. This concurrency is of particular concern when a developer is building a simulation environment that must contend with many files of varying length and complexity from the execution of a process or multiple processes. In a multitasking environment, the developer must contend with numerous files directly related to each other for each simulation process and the potential for multiple simulation processes to execute concurrently. Only a sophisticated OS can handle this problem, and Windows NT proved capable of the task.

The development under Windows NT was similar in many ways to the development under Windows 3.0. Other developers told Simucad's developers that they would pay a severe performance penalty because Windows NT is slow, that painting and graphical refresh speeds are slower than those of Windows 3.1, and that Windows NT requires even more memory and disk space than does Windows 3.1, which some regard as a memory hog (**Fig 2**). Developers also warned Simucad that the beta version of Windows NT is replete with bugs.

As with any software under development, Windows NT had bugs. However, Microsoft responded promptly with fixes and work-arounds. In one case, the development engineer reported a problem to Microsoft on Friday afternoon and received a Federal Express package with a new floppy disk containing the bug fix on Monday morning.

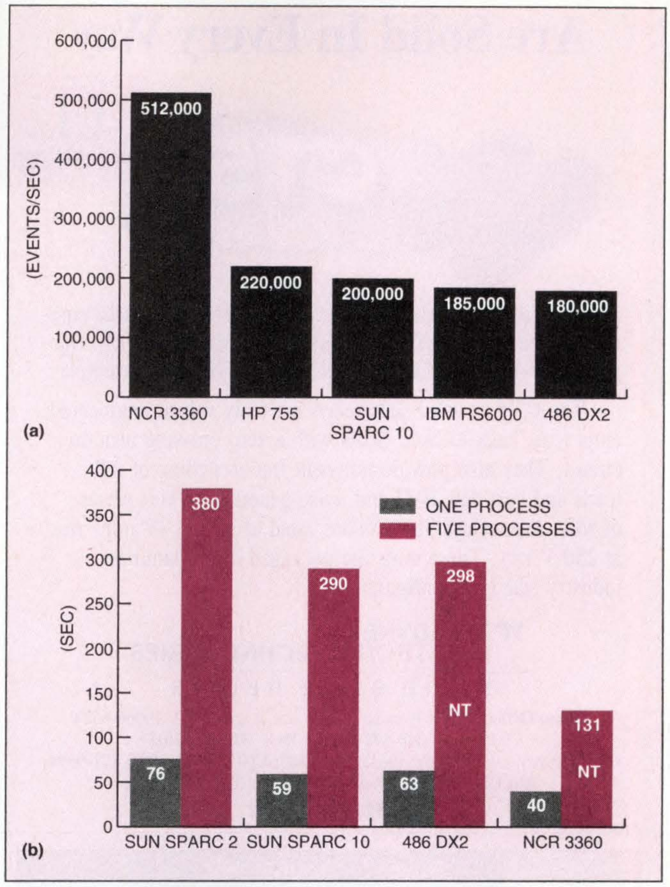

Fig 3—These software-performance results (a) and the multitasking-performance results (b) are early indicators of the performance you can expect from high-performance Pentium-based PCs.

The prediction of performance penalties under Windows NT was pure fiction. In fact, using Microsoft's C compiler (which is currently a beta version and which the Windows NT SDK includes), Simucad's Silos III simulator running under Windows NT realized a 15% performance improvement over the Windows 3.1 version running on the same computer. The company expects that with a final version of the C compiler and with some custom optimization of critical routines, the improvement could be around 35%.

When users consider such features as preemptive multitasking, multithreading, and true networking, along with this type of performance improvement, Windows NT seems a clear upgrade path. However, when you combine Windows NT with a high-performance PC, such as an NCR 3360 (dual 60-MHz Pentium μPs) and sufficient system memory and storage, you can have a system equal to or better in performance than any workstation.

To validate Windows NT's potential, Simucad uses its own hardware-performance test to determine system performance. The test comprises a string of devices in a chain that, when simulated with Silos III, provides a consistent measure

WINDOWS NT SOFTWARE DEVELOPMENT

in events/second. This measurement is useful because it provides an accurate benchmark of raw hardware performance. The best rating previously generated was 220,000 events/sec on an HP PA-RISC series 755 tested in HP's porting lab. In contrast, the NCR 3360 delivered a rating of 512,000 events/sec, more than twice that of the highest rated workstation—and that was with a program compiled without full optimization (**Fig 3**).

One of the more significant benefits of Windows NT is that it does not require a systems expert to install and maintain. On the other hand, Unix's complexity dictates that an expert in Motif, Unix, and X install and maintain the utilities and assures that system upgrades (new releases) are compatible with existing utilities and application software. Windows NT's consistency and guaranteed compatibility between the OS and the GUI ensure relatively easy installation and smooth operation of Windows NT-based software.

Another benefit of Windows NT is that, like Windows, it provides device independence. Microsoft and hardware vendors support peripherals, such as hard drives, tape drives, modems, networking hardware, multimedia systems, and printers. If you have ever tried to get a nonstandard printer or peripheral to run under Unix, you know the value of this often overlooked benefit.

Windows NT has the necessary OS attributes for superior EDA-application performance. It provides all the benefits that make Unix so popular but differs from Unix in one key area: It combines the GUI with the OS without variance and without compromise. This benefit, although arguable, provides the finest level of compatibility and consistency available. In short, Windows NT is an operating environment, and Unix is an OS.

The combination of Windows NT and Pentium create a highly desirable paradigm for high-performance EDA. Because developing software under Windows NT is far less complex, less resource-restrictive, and less costly than it is to develop under Unix, the price of EDA software for Windows NT should be less than the equivalent software for Unix. Furthermore, the X86-based PC's ever-increasing capacity and performance continue to make it an even more attractive computer for which to target EDA tools. This attraction is true for both software developers and users alike.

The X86 PC requires much less overhead and maintenance than its Unix-based workstation counterparts and benefits from reduced start-up costs. Nonetheless, users will move to Windows NT in large numbers only when qualified EDA software products are available at reasonable prices. Therefore, users must demand high-quality, price-sensitive Windows NT-based EDA software from their EDA tool suppliers. EDN

Author's biography

Bill Fuchs is president and CEO of Simucad in Union City, CA. Bill has been with Simucad for six years. His job includes "everything but writing the code," he says. Fuchs enjoys playing basketball and restoring automobiles in his spare time.

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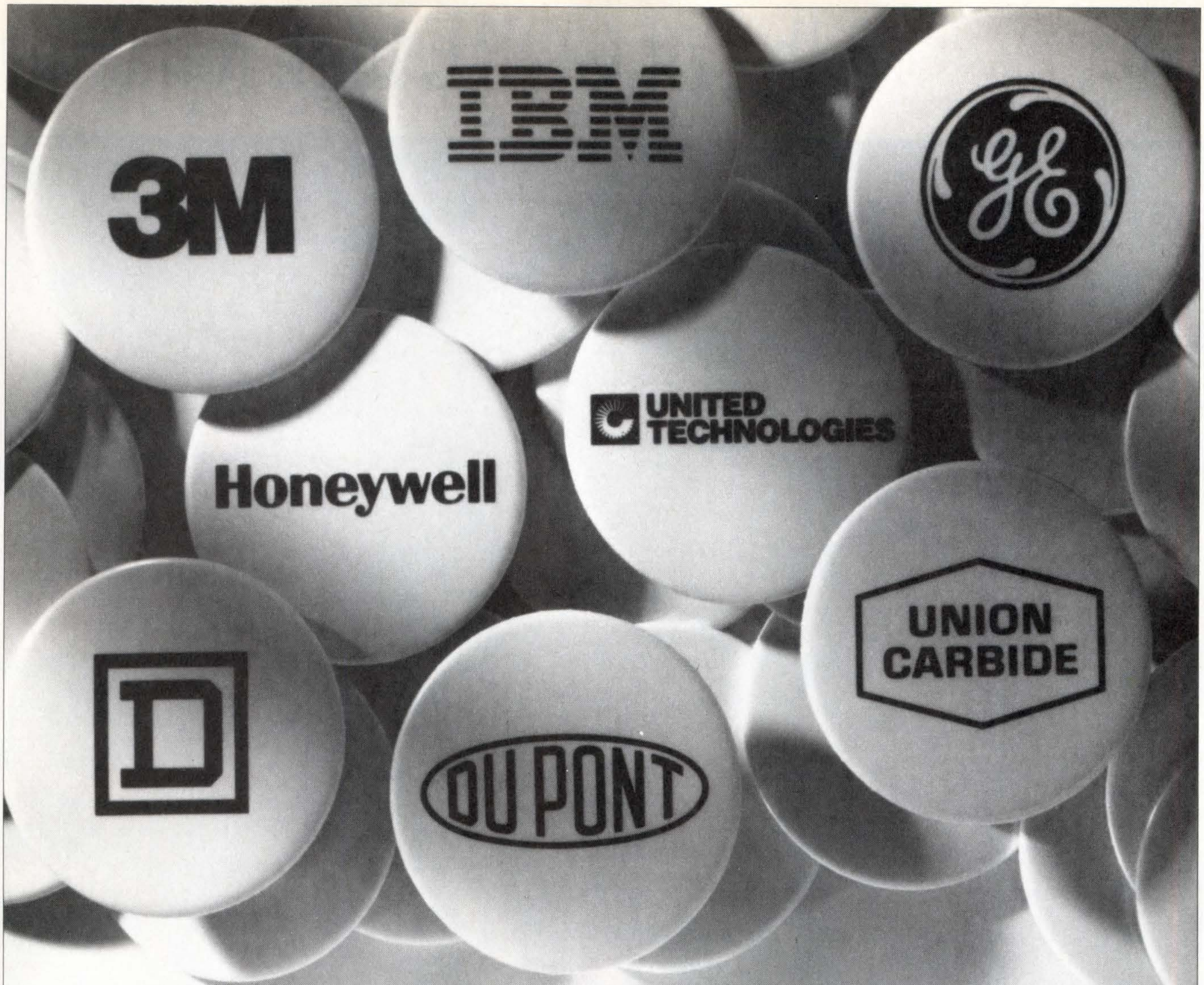

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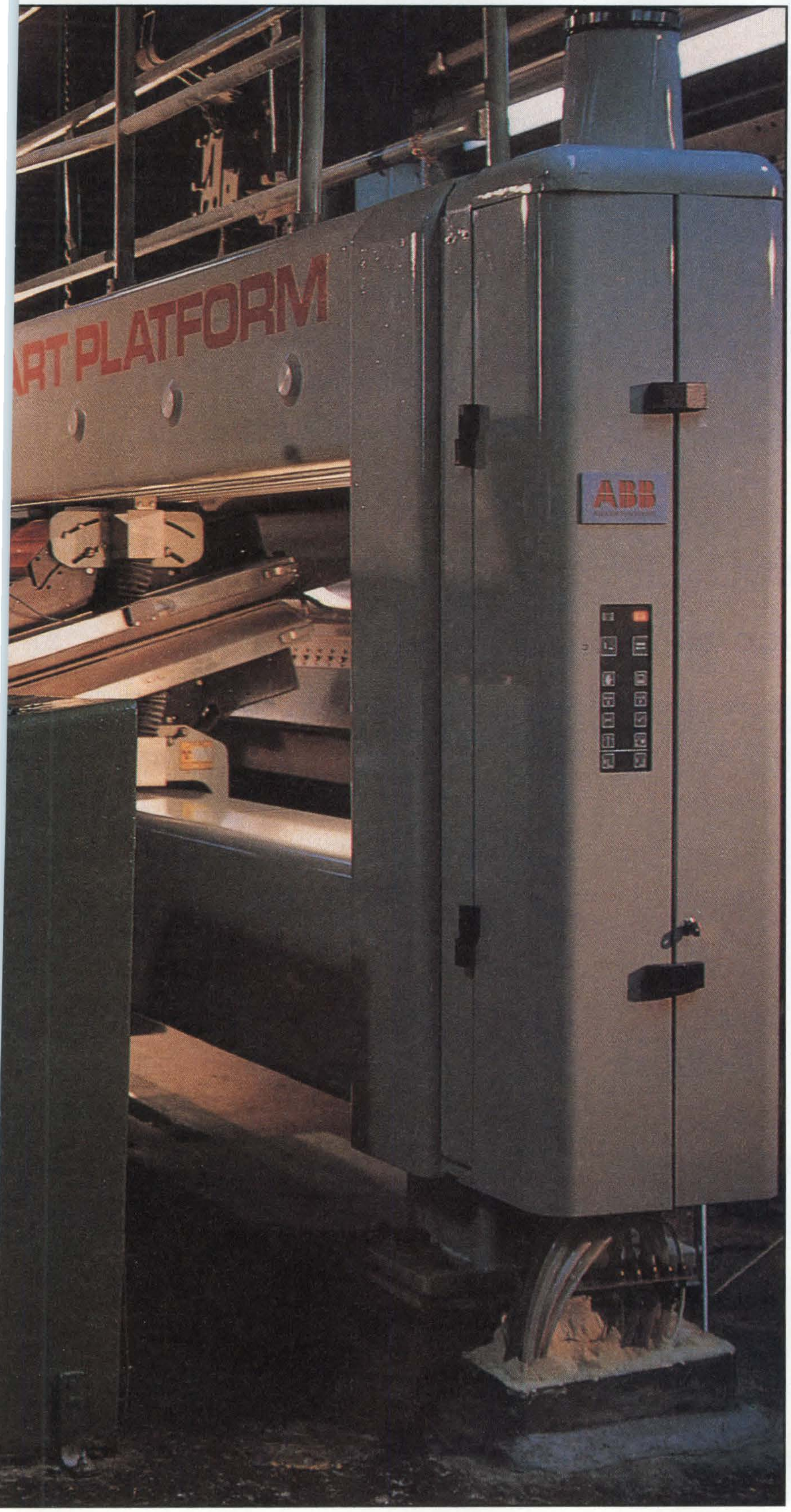

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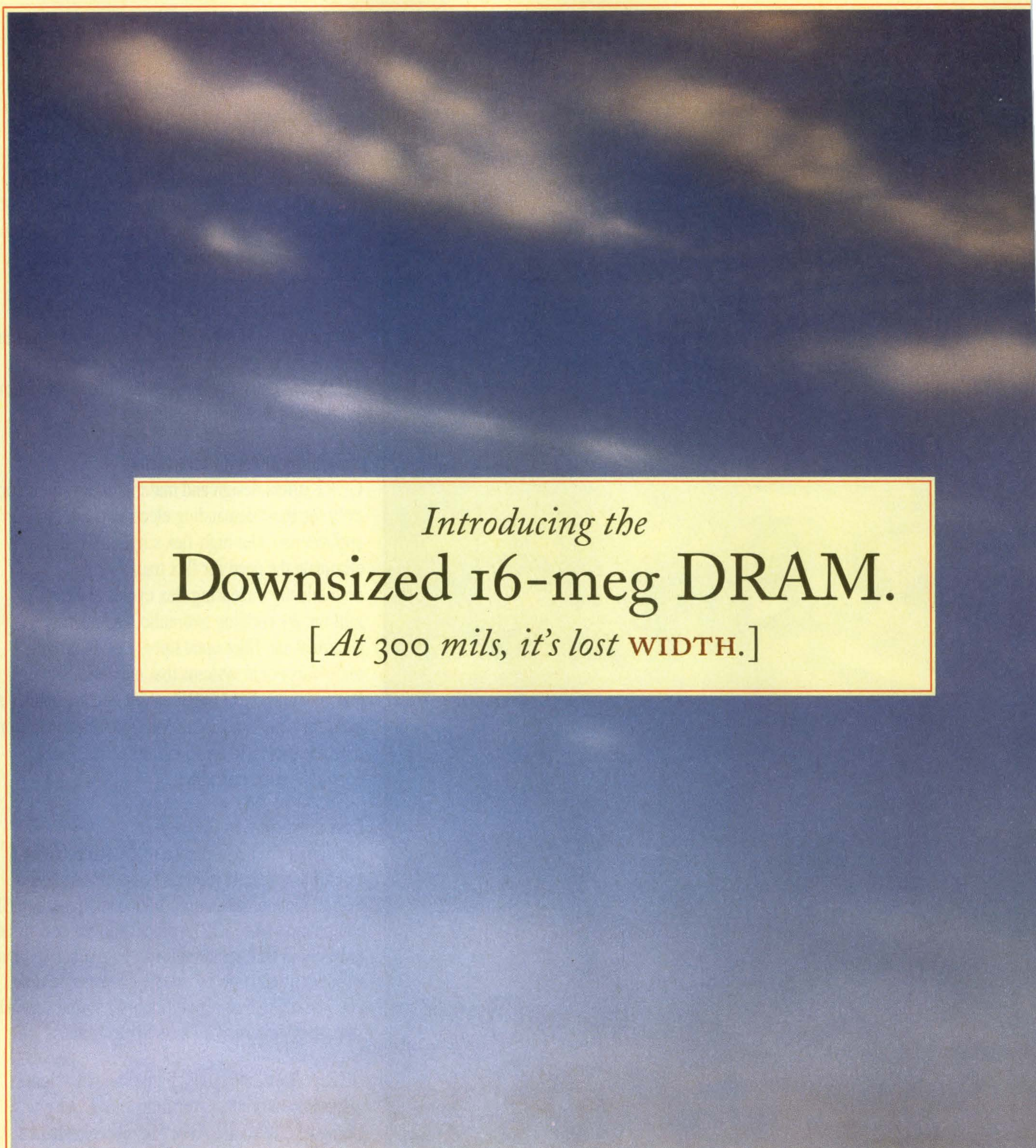

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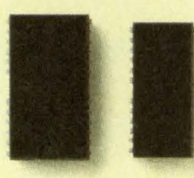

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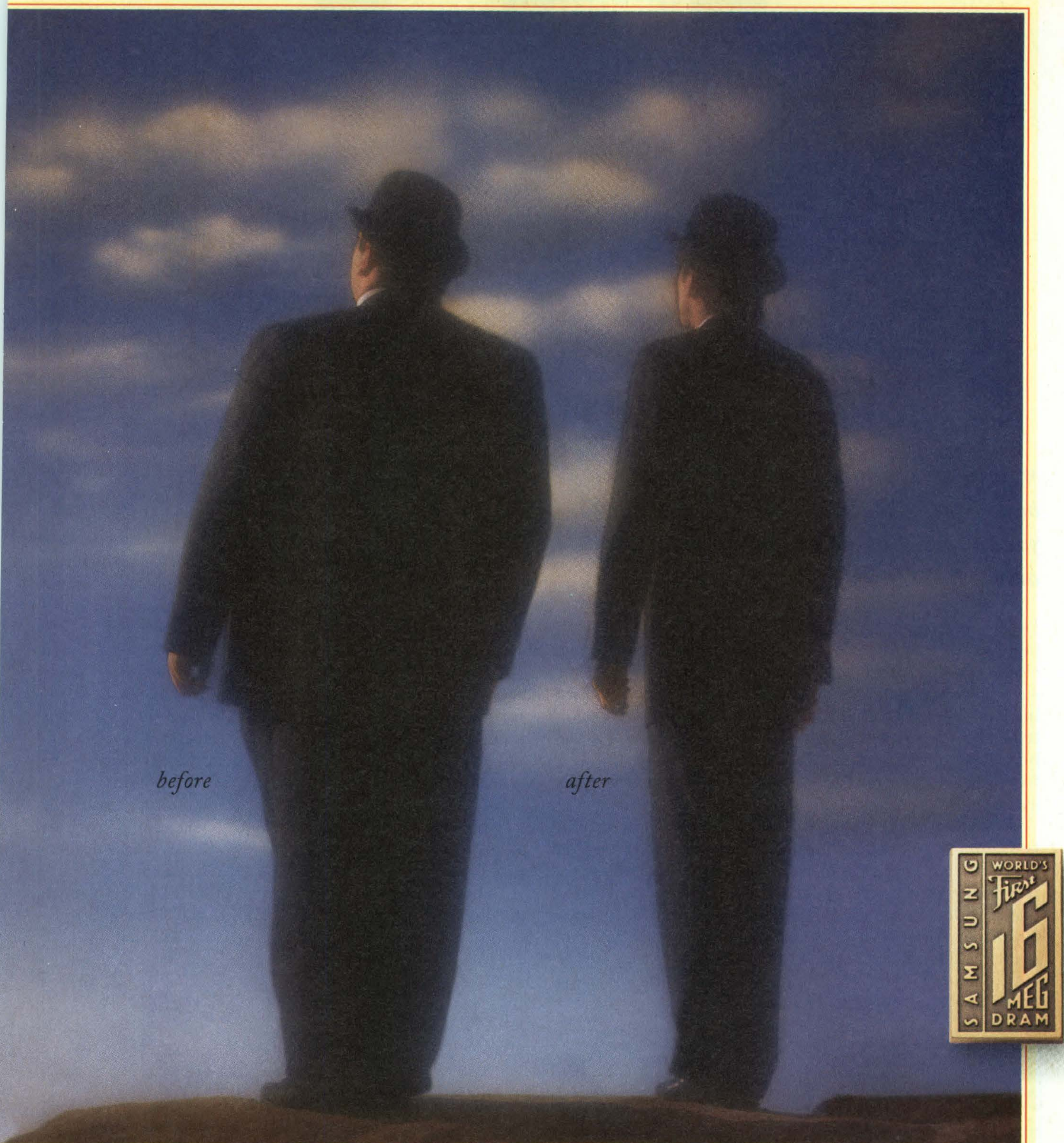
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Technique eases design of high-order PLLs

Fred Salvatti, White Sands Missile Range

Maintaining stability in high-order PLLs can be a chore. Two design programs can assist you in designing stable types 2 and 3, third-order PLLs.

Designers are using PLLs in a variety of applications, including clock distribution. Because distributing high-frequency clocks (above 33 MHz) on a pc board can cause RF problems, such as clock skew and crosstalk, designers are instead placing PLLs wherever a high-frequency clock is needed and distributing a low-frequency clock to the PLLs on the motherboard. The PLLs multiply the frequency of the low-frequency clock to generate localized high-frequency clocks, avoiding the problems of high-frequency distribution.

To determine the stability of a PLL, you can use a stability-factor (SF) parameter (**Ref 5**). The SF replaces tables and charts with an intuitive measure of stability and simplifies the design of a second-order PLL. SF is a dimensionless quantity that equals the number of damped natural-frequency cycles/system time constant. The more cycles/time constant, the longer time required for the PLL to reach a steady-state value. SF applies to higher-order systems, such as types 2 and 3, third-order PLLs.

BBS The software listings in this article are available on *EDN*'s computer bulletin-board system. Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #681."

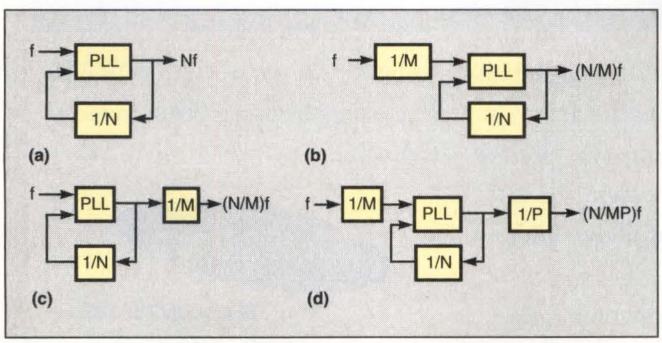


Fig 1—You can accomplish frequency multiplication by means of a PLL using one of four popular methods.

Fig 1 shows the basic methods for synthesizing a high-frequency clock from a low-frequency clock. **Fig 1a** shows the simplest method for multiplying by an integer. To multiply a frequency by a rational number, you must use the methods in **Fig 1b** or **c**. Because the bandwidth of the PLL should be smaller than the PLL's reference-input frequency to obtain good noise filtering and sideband suppression, designers prefer the method in **Fig 1c**. In cases in which method **Fig 1c** is not practical due to VCO range limits, the method in **Fig 1d** provides an alternative by lowering the input-reference frequency by 1/M.

High-order PLLs often find use in frequency-synthesis applications. The number of poles at the origin in the open-loop transfer function determines the type of the loop. The type also determines the steady-state tracking error. Because phase is the time integral of frequency, a frequency step produces a phase ramp, and a frequency ramp produces a constant phase acceleration. A Type 2 PLL tracks a reference frequency ramp with a constant phase error.

You can convert a Type 2, second-order PLL to a Type 2, third-order PLL by adding a single-pole RC filter to the out-

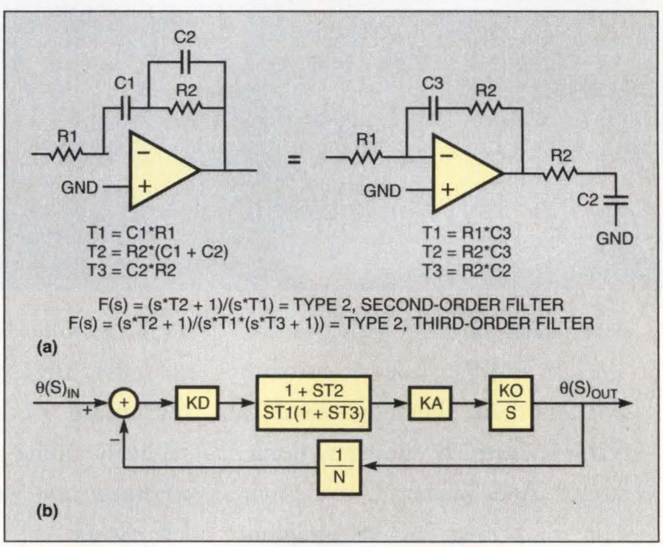
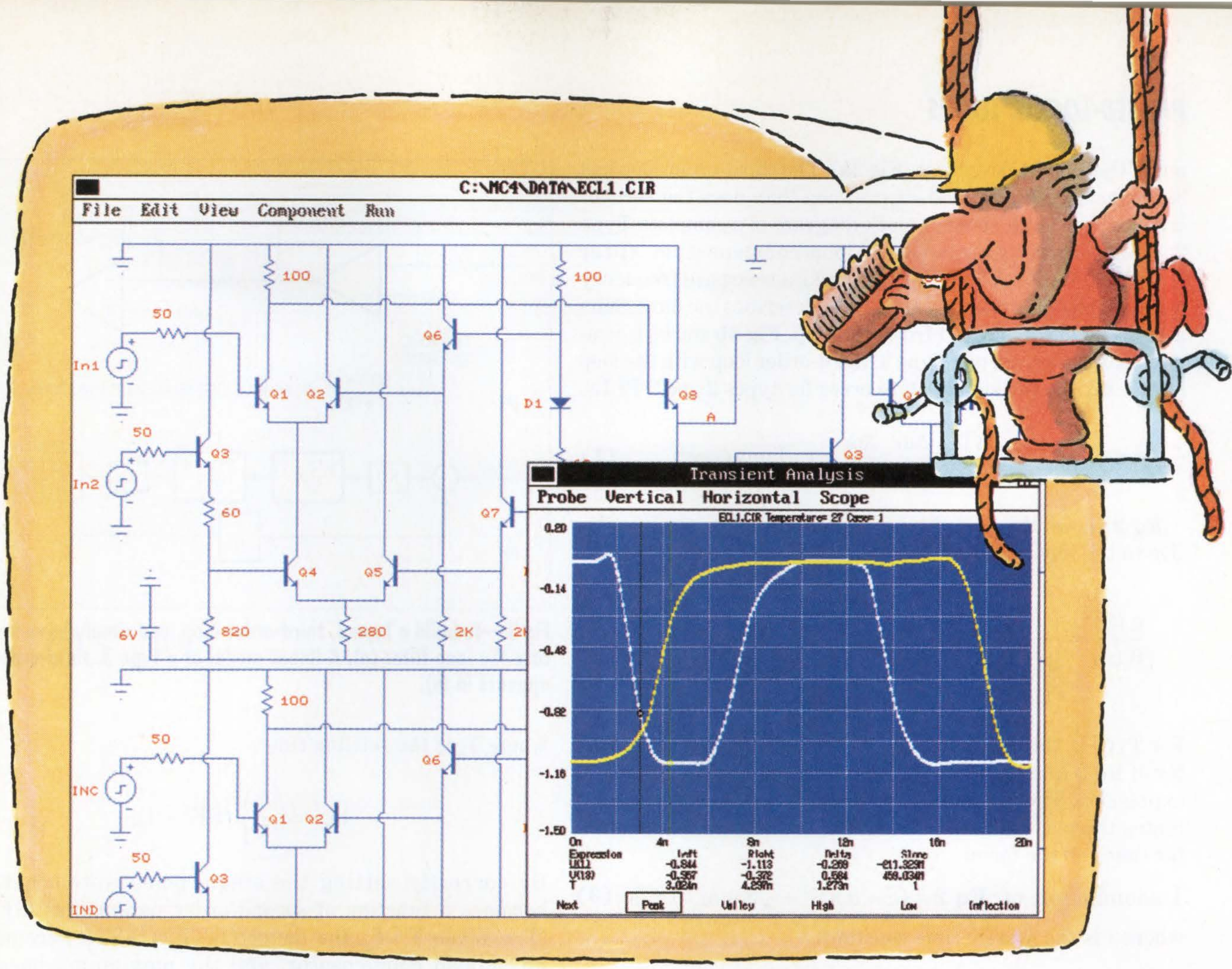


Fig 2—To convert a Type 2, second-order loop to a Type 2, third-order loop, you add another pole to the loop filter. (a) shows two methods of building the loop filter; (b) shows a block diagram of the linear model.



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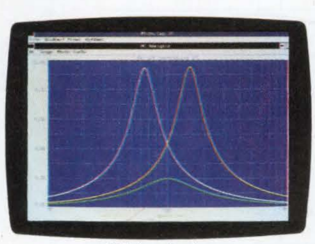

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put of the loop's active filter (**Fig 2a**). The third-order loop has better noise and sideband suppression than does the second-order loop. **Fig 2b** shows a block diagram of a complete Type 2, third-order loop with a loop-compensation filter (1+ST2)/(1+ST3). A Type 3 PLL tracks a reference frequency ramp without any phase error. **Fig 3a** describes the filter characteristics of a Type 3, third-order loop. **Fig 3b** shows a complete block diagram of a Type 3, third-order loop with the loop filters. **Eq 1** is the steady-state error for types 2 and 3 PLLs.

$$e_{ss}(t) = \frac{\Delta\omega/\Delta T}{K_a} + \frac{\Delta\omega}{K_v}; \frac{\Delta\omega}{\Delta T} = \text{radians}/\text{sec}^2. \quad (1)$$

Eq 2 shows the transfer function of the phase error relative to the input phase:

$$\frac{\epsilon(S)}{\theta_i(s)} = \frac{S^3 + S^2\dfrac{1}{T_3}}{S^3 + S^2\dfrac{1}{T_3} + S\dfrac{K_D K_A K_O T_2}{NT_1T_3} + \dfrac{K_D K_A K_O}{NT_1T_3}}. \quad (2)$$

For Type 2, third-order PLLs, you can factor the denominator of **Eq 2** into the products of a single pole and a quadratic expression. The complex pole-pair closest to the origin dominates the performance of the loop. The factored denominator takes on the form:

$$\text{Denominator of } \mathbf{Eq\ 2} = (S+\alpha)(S^2 + \frac{2}{\tau}S + \omega_n{}^2) = 0, \quad (3)$$

where τ is the system time constant.

$$T_S = 2\pi\tau, \quad (4)$$

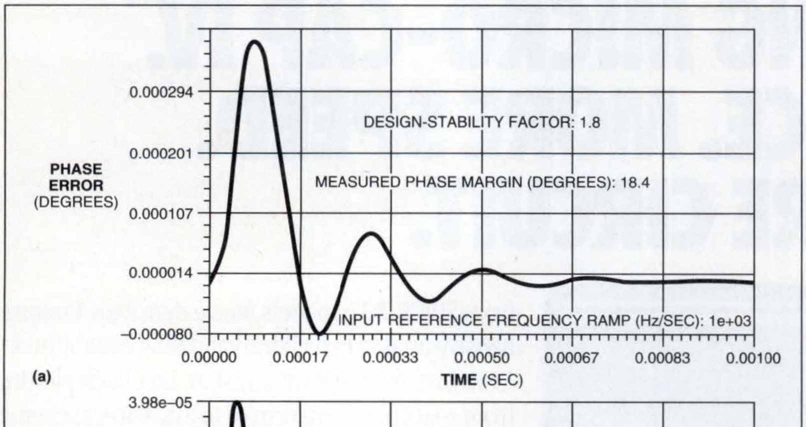

Fig 4—a shows the constant acceleration transient response of a Type 3, third-order PLL having a stability factor (SF) of 1.8. b shows the same response for a Type 2, third-order PLL having an SF of 6.1.

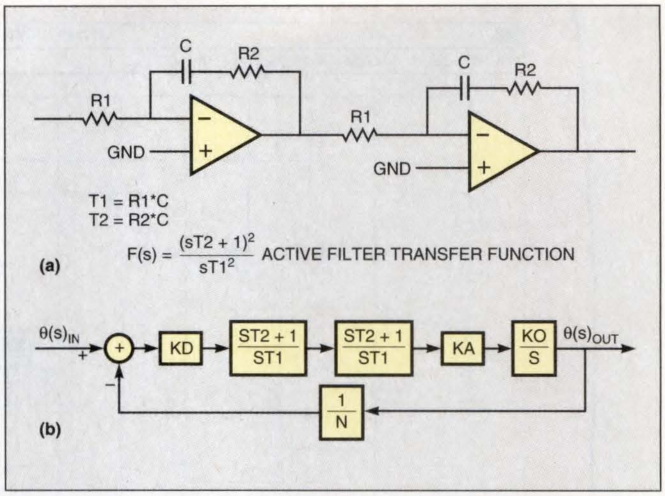

Fig 3—To build a Type 3, third-order loop, you simply have to duplicate the loop filter (a). A linear model of a Type 3, third-order loop appears in (b).

where T_s is the settling time.

$$\omega_n{}^2 = \left(\frac{1}{\tau}\right)^2 (SF^2 + 1). \quad (5)$$

By correctly setting the single pole, system behavior becomes a function of second-order parameters (SF) and (T_s). When $T_2 > T_3$, the factor $(1+sT_2)/(1+ST_3)$ becomes a a phase-lead compensator, and the maximum phase lead occurs at

$$\omega_{0db} = \sqrt{\frac{1}{T_2T_3}}. \quad (6a)$$

The design goal is to make the 0-dB crossover frequency of the open-loop Type 2, third-order transfer function identical to the frequency in **Eq 6a**. To ensure second-order dominance, impose the following restriction:

$$\alpha = 5 \times \omega_n. \quad (6b)$$

Equating coefficients in **Eq 3** and substituting **Eq 4** and **Eq 5**, you can arrange **Eq 6a** to be:

$$\omega_{0db} = 5\frac{\sqrt{(SF^2+1)}}{T_S\sqrt{\dfrac{T_2}{T_3}}}. \quad (7)$$

You can determine the stability of higher-order systems by examining the phase margin. **Eq 8** from **Refs 1** and **2** gives the phase margin, given a phase-lead compensator of $(1+sT_2)/(1+sT_3)$.

$$\frac{T_2}{T_3} = \left[\frac{\cos\Phi}{(1-\sin\Phi)}\right]^2, \quad (8)$$

where Φ=phase margin.

In addition, **Eq 9** relates the SF and the damping factor.

$$SF = \sqrt{\frac{1}{\zeta^2} - 1}, \quad (9)$$

where ζ is the second-order system-damping factor.

For second-order systems, **Eq 10** shows that the phase margin is a function of the damping factor or SF (**Ref 3**).

$$\Phi = \frac{\pi}{2} - \arctan\sqrt{\frac{1}{2}\sqrt{\left(1+\frac{(SF^2+1)^2}{4}\right)} - \frac{1}{2}} \quad (10)$$

Using the relationships from **Eq 3** to **10**, you can solve for T_1, T_2, and T_3 for any given SF and T_s. A design program is available that accepts SF, T_s, and other PLL parameters as inputs. (See **box**, "How to get a copy of the programs.") The program then selects the required values for resistors and capacitors that produce PLL performance corresponding to SF and T_s.

The transfer function of the phase error relative to the input phase in **Fig 3b** is:

$$\frac{\epsilon(S)}{\theta_i(s)} = \frac{S^3}{S^3 + S^2\frac{T_2^2K_DK_AK_O}{NT_1^2} + S\frac{K_DK_AK_O2T_2}{NT_1^2} + \frac{K_DK_AK_O}{NT_1^2}}. \quad (11)$$

Again, factoring the denominator into the product of a single- and complex-pole pair yields:

$$\text{Denominator of } \mathbf{Eq\ 11} = (S+\alpha)(S^2 + \frac{2}{\tau}S + \omega_n{}^2) = 0. \quad (12)$$

Ref 4 shows that the open-loop, 0-dB crossover frequency is:

$$w_{0db} = \frac{K_DK_AK_OT_2^2}{NT_1^2}. \quad (13)$$

To solve for T_1 and T_2, set the single-pole frequency to five times the value of the second-order natural frequency. Then, equate coefficients in **Eq 12** and substitute **Eqs 4** and **5**. A program is available to design a Type 3, third-order PLL using SF, T_s, and other PLL parameters.

Stability differs for PLLs

Generally, a Type 3 system is less stable than a Type 2 system because Type 3 PLLs have three integrators in the loop and Type 2 PLLs have only two. **Figs 4** and **5** show how the stability factor and phase margin affect Type 2 and Type 3 PLL behavior in the time domain. **Fig 4a** shows the time response for a Type 3, third-order filter, where SF=1.8 and the phase margin=18.4°. The loop is stable, but it takes an SF=6 to produce the same phase margin in a Type 2, third-order loop. **Fig 4b** shows the same time response for a Type 2, third-order loop under the same conditions.

Fig 5 shows that the Type 3, third-order loop is less stable than the Type 2, third-order loop.

HOW TO GET A COPY OF THE PROGRAMS

You can obtain a copy of the PLL programs mentioned in this article. A DOS PLL program on a 5¼-in., 1.2-Mbyte floppy disk contains the design of a Type 2, third-order PLL and costs $29.95. Another 5¼-in., 1.2-Mbyte floppy disk contains a DOS program to design a Type 3, third-order PLL and costs $39.95, plus shipping and handling. Send your orders to Fred Salvatti, 4644 Larkspur Court, El Paso, TX 79924 or phone (505) 676-5889. You must include payment with your purchase order. A demonstration program is available on *EDN*'s bulletin board posted at MS681Z.ZIP on the /freeware Special Interest Group.

In **Fig 5a**, the Type 3, third-order loop becomes unstable when SF=2.7. The phase margin is 206°. **Fig 5b** shows that a Type 2, third-order loop is stable for the same SF and has a phase margin of 38°.

Tune the loop for the desired bandwidth

Recall that SF is the number of cycles/system time constant and T_s in **Eq 4** is a function of the system time constant. If you keep T_s constant and increase the number of cycles/time constant, you increase system bandwidth. Similarly, if you keep SF constant and increase T_s, then you decrease the system bandwidth.

Figs 6 and **7** show how you can decrease the rise time without increasing the bandwidth. Figure **6b** shows the open-loop performance when SF=2 and T_s=0.0028 sec. **Fig 6a** shows the corresponding rise time of approximately 0.00047 sec. **Figs 7a** and **b** show that by increasing SF to 2.7 and increasing T_s

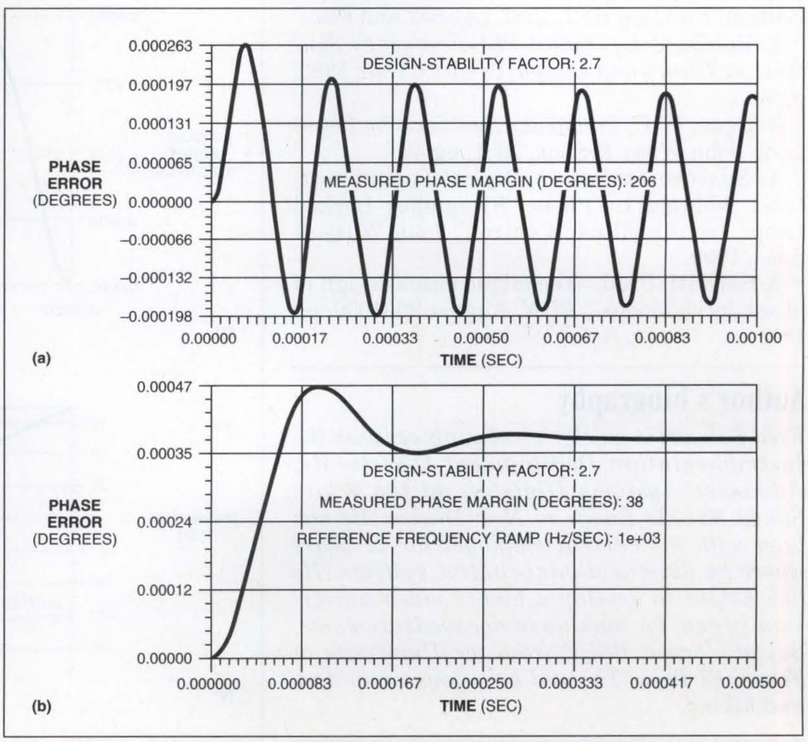

Fig 5—For a 2.7 SF, a Type 3, third-order PLL (a) is less stable (phase margin=206°) than a Type 2, third-order PLL (b) (phase margin=38°).

to 0.0045 sec, the rise time decreases to approximately 0.00037 sec. The bandwidth remains constant at 1.56 kHz. The figures also show that the damped oscillations die out after 0.00187 sec in both cases. The SF and T_s design parameters only approximate system performance; actual behavior may not be the same. However, using the design programs, SF and T_s let you quickly adjust to the desired performance.

Type 3 PLLs can be more difficult to design than Type 2 PLLs because they tend to be more unstable. However, the Type 3, third-order design program simplifies the design task. Using the program, you enter known or measured loop parameters, and the program computes and displays the component values to meet your requirements. Actual components, whose values only approximate the computed values, may cause the PLL to behave slightly different from what you expect. The program allows you to enter actual values, so that you can observe the transient and frequency response under actual conditions. Using this feature, you can observe the effects of component tolerances on loop stability. In addition, you can design even higher-order PLLs, such as fifth- and seventh-order loops, using the design program. EDN

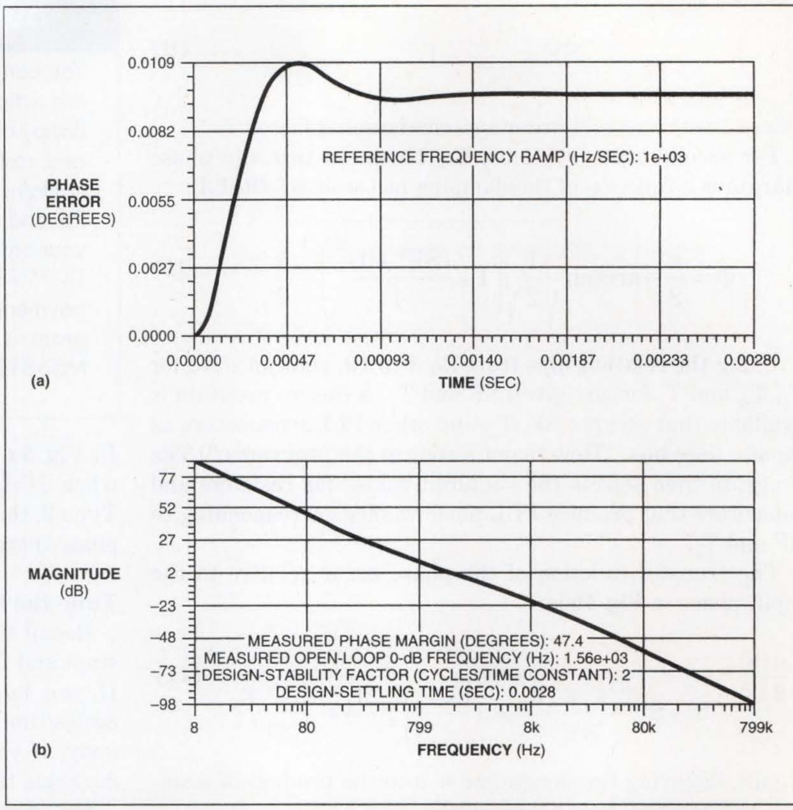

Fig 6—This design of a Type 2, third-order PLL employs an SF of 2 and a settling time (T_s) of 0.0028. The rise time is 0.00047 sec (a), and the open-loop 0-dB frequency is 1.56 kHz (b).

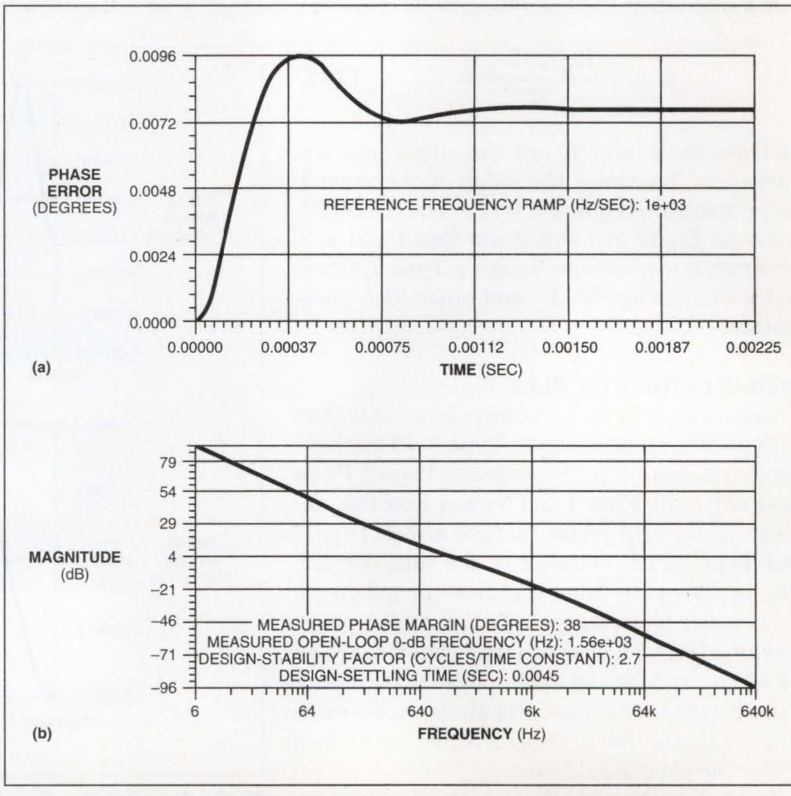

Fig 7—By changing the SF to 2.7 and the settling time (T_s) to 0.0045 sec, you can maintain the same bandwidth as Fig 6 and decrease the rise time to 0.00037 sec.

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Author's biography

Fred Salvatti is an electrical engineer with the Instrumentation Development Directorate, Advanced Systems Division, at the White Sands Missile Range in New Mexico. He has been with his current employer for 28 years where he designs digital-control systems. He has helped to develop a film-to-video conversion system for making image measurements. Salvatti has a BSEE from the University of Texas, El Paso, TX, and he enjoys computers and hiking.

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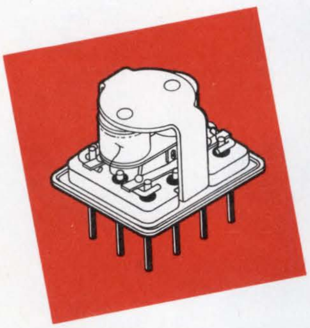

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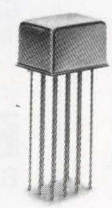

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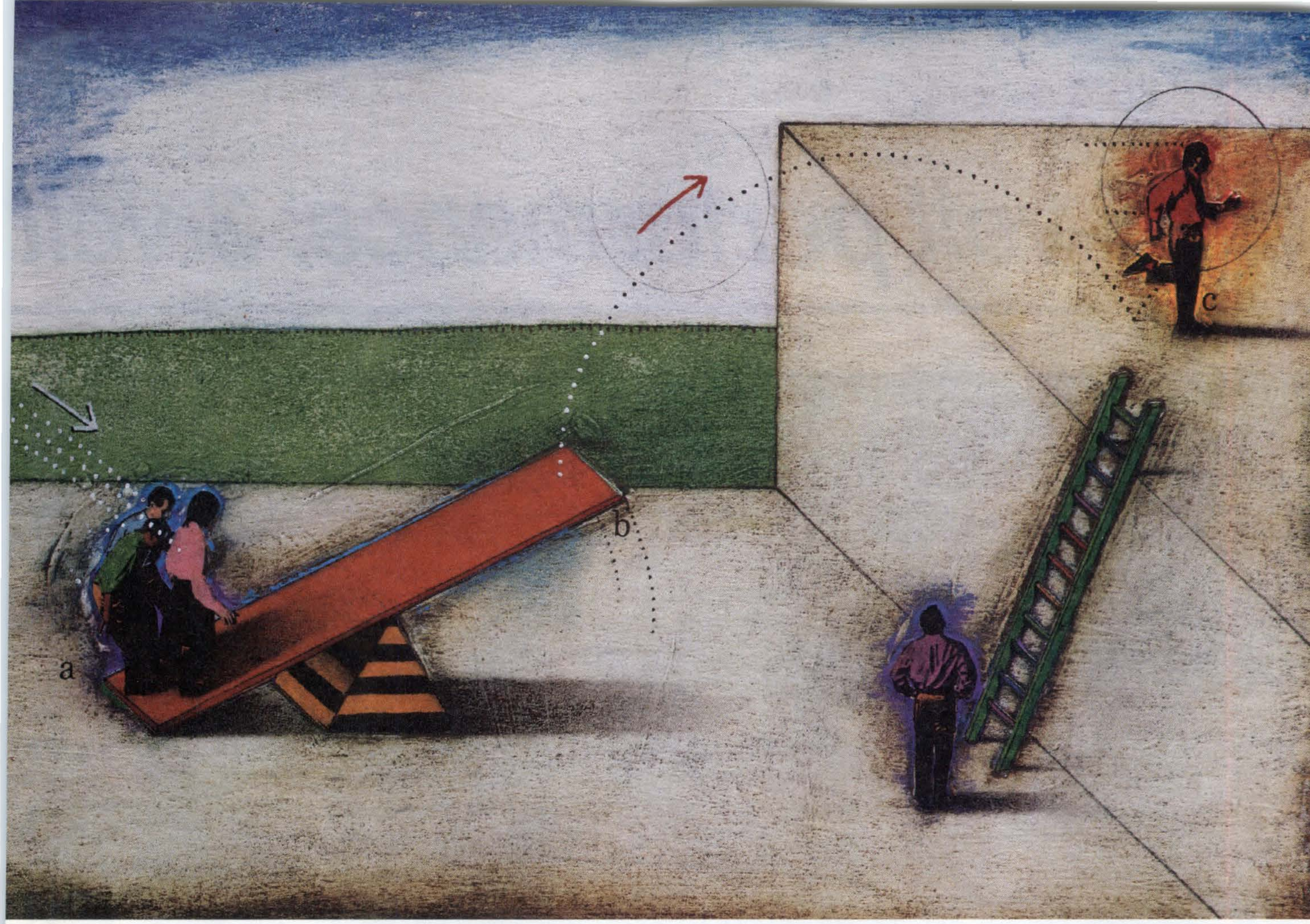

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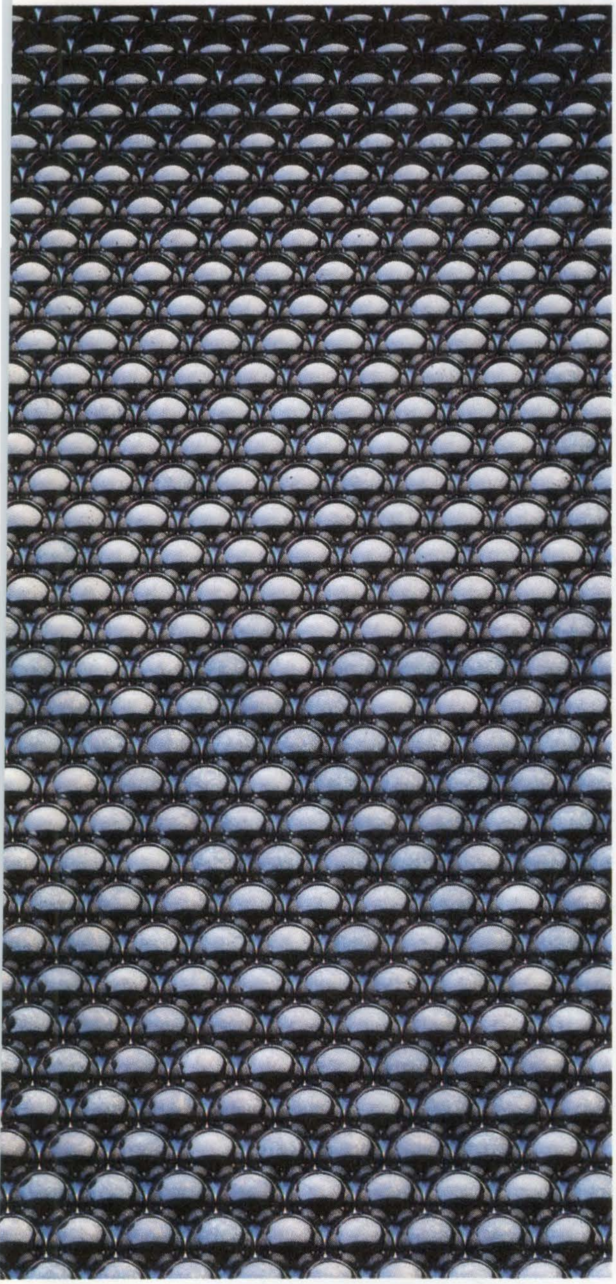

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Good design enables hot insertion of power supplies

Mikhail Grabois, Ascom Timeplex Inc

Hot insertion of power supplies offers many advantages, but it can cause lots of problems unless you prepare for it in your design.

By providing for "hot," or "live," insertion of power supplies, you can improve system serviceability, reliability, and availability. But these improvements don't come without a price; they require extra design effort to select the right connectors, prevent contact damage, avoid system-bus glitches, and balance power distribution.

Start with the connector

One of the first things to consider is the power-supply connector, which you can attach to the supply in one of three ways—with cables, with short wires, or directly to the supply's pc board. Each approach has its advantages and disadvantages.

If you use cables to attach connectors to a power supply and its load, you can remove the supply with part of the cabling in case the supply needs to be replaced. This approach somewhat improves serviceability but lowers overall reliability.

In the second approach, you can attach connectors to the power supply terminals by a set of short wires and then mechanically attach the body of the connector to the supply. Then it's possible simply to insert the power supply into the system rack and engage a connector on the backplane. A set of wires on the backplane runs from the connectors to the load. Because "connectorized" versions of power supplies are uncommon, this approach offers the advantage of using an off-the-shelf power supply with minor modifications. Disadvantages include the need for additional space and the increased cost of repackaging.

In a custom design, you can attach connectors directly to a power supply's pc board. This approach provides the most compact design and the highest reliability. If you select the correct connectors, this way provides the lowest cost for adding connectors. Note, though, that pc-board connectors cannot handle a significant amount of current, so you have to take special precautions in your design.

Don't neglect path resistance

When you use power connectors with only a few contacts, it's not difficult to select the rating and the number of contacts to accommodate any deviation in current-path resistance. However, if large numbers of pins have low current capacity, as is the case with board-mounted connectors, then path resistances become a real concern.

The current in each connector pin or contact is inversely proportional to the resistance of the path (and not the contact itself). In a way, that's good news, because contact resis-

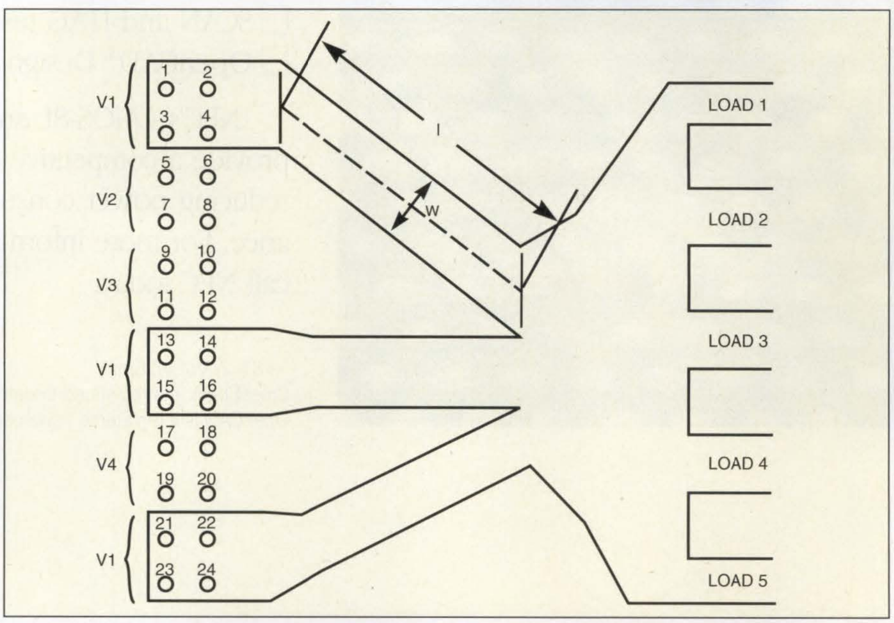

Fig 1—If contact resistances on a power supply's connector pins differ only a little, you can equalize path resistances by ensuring that pc-board traces have a significantly higher resistance and that all traces have the same length-to-width ratio.

tance is harder to control than any other part of the circuit. Some connectors—for example, the multirow pin-and-socket type—have distinct resistance differences that result from contact-length differences. You can control the resistances of individual contact circuits by providing separate runs, with individual wires or traces, that connect to a common bus. If differences in contact resistances aren't very obvious, it is sufficient to equalize all path resistances (using traces with the same length and the same width) and to make those resistances sufficiently higher than the contact resistance (**Fig 1**).

Often, pc boards have copper layers or fields for power distribution. In such cases, the currents from connector contacts take the shortest paths to the load, and these paths may be different for different contacts and may differ from the geometrical shape of the conductor. Therefore, it may be necessary to isolate the paths for individual pins or groups of pins (**Fig 2**).

An engineer who generates the design specification for a power supply must also address current distribution over connector contacts. The current source in a power supply is usually a single point (a device lead), so it is important to minimize or compensate for resistance difference between the source point and the connector contacts.

Guard against contact arcing

The issue of contact arcing is always a concern in live-circuit replacement, but it is much more critical for pc-board connectors with small contacts. Arcing results either from high voltage breaking the air gap between contacts during contact engagement or disengagement or from an interruption of the high current in low-voltage circuits. You should try to minimize the effects of both factors.

Limiting the available current minimizes the effect of high voltage, which is present on the contacts carrying the input ac power to the power supply. During contact engagement, the input current—called "inrush current" in this situation—results from the charging of the power supply's input capacitance. The duration of charging is usually less than 30 to 50 msec, and after this transitional period, any input-current increase is not critical because the contacts are fully engaged and do not produce arcing. The power supply's specified maximum inrush current should not exceed 10A. During contact disengagement, the fully charged input capacitance limits the input current.

Limiting the current can also minimize the effect of high current at low voltage—the usual output of the power supply. The power supply's output current should be significantly lower by the time contact disengagement occurs. To achieve this, you can disable the outputs in advance by the manual switch or, better, by an early disengagement of a connector pin that is shorter than the power-output pins.

Avoid power-bus disturbances

A design aspect that is critical to live power-supply insertion or removal involves the conditions on the common output bus during the transitional period. The common bus should not experience any disturbances that could affect system performance. Two aspects to consider are output capacitance and transient response.

If the power supply's output capacitance comes in contact with the common bus before it gets charged, sagging of the bus is inevitable. You can prevent this by precharging the output capacitance via dedicated pins or by isolating the capacitance with diodes. The isolating diodes may also prevent total system failure if one supply in a multiple-supply system gets a short circuit on its output.

Another source of disturbance on the common bus is a current transient that results from a change in the number of power supplies on the bus. To avoid this kind of disturbance, which may affect system operation, specify and design power supplies with a transient response adequate for the worst-case current-amplitude change and the maximum speed of the change.

In one situation, however, proper transient response is inadequate. If you yank an on-line power supply from a live system, no power supply can compensate for the change. Only the disabling of the output before removing the unit can do the job. EDN

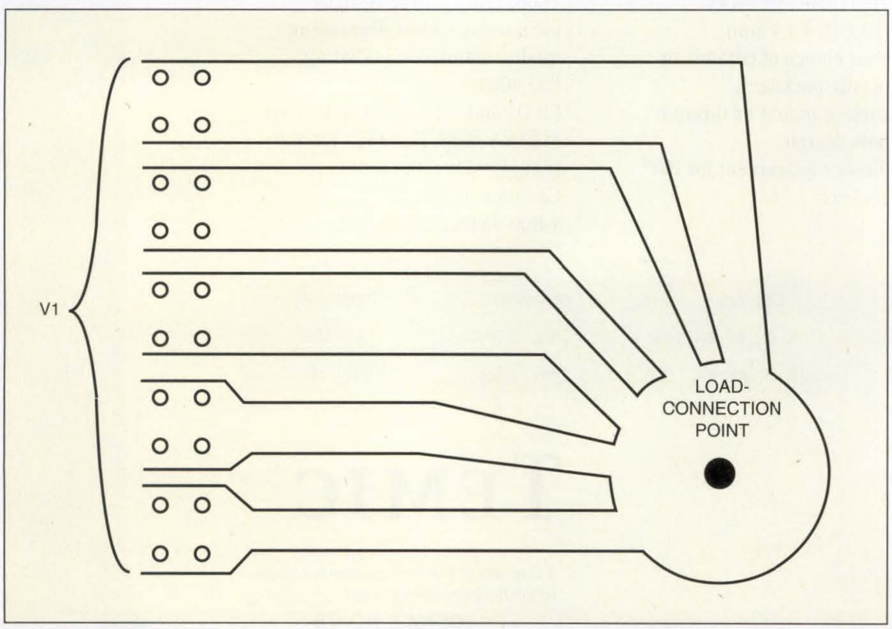

Fig 2—For proper power distribution when the same voltage appears on multiple connector pins, isolate and equalize current paths. Otherwise, current from the contacts takes the shortest paths to the load.

Author's biography

Mikhail ("Mike") Grabois is a staff engineer at Ascom Timeplex Inc, Woodcliff Lake, NJ, where he is responsible for the design of power systems and high-speed backplanes and also addresses thermal and electromagnetic-compatibility performance issues. He has a BSEE from the Moscow Institute of Railway Engineering and an MSEE from New York University, New York. His leisure activities include theater, music, soccer, and skiing.

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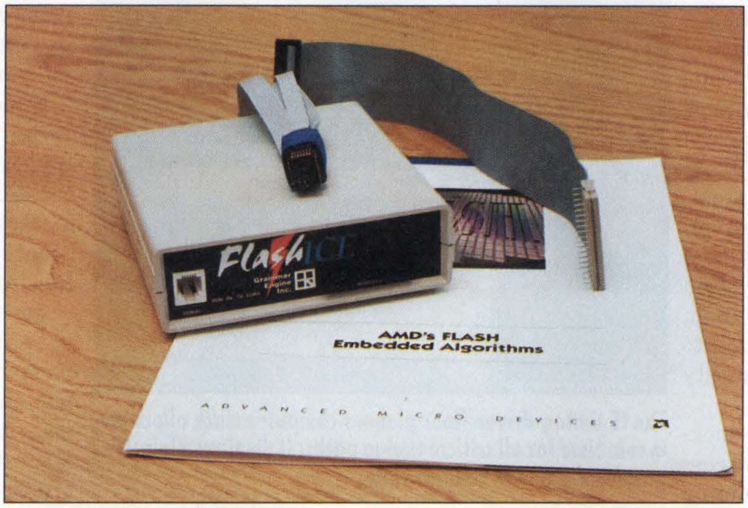
Emulator verifies code that controls flash memory



You can verify your flash-memory control code with Grammar Engine's FlashICE flash-memory emulator.

With its ability to accept and retain data without power, flash memory is ideal for many embedded systems and is finding use in many applications. But flash memory is not without its troubles. You must ensure that your code controls flash memory properly, and flash memory can perform only a limited number of write cycles.

Until now, it was difficult to verify that your code was indeed using the flash memory correctly. FlashICE from Grammar Engine aims at alleviating the problems of using flash memory. It emulates the operation of the Advanced Micro Devices Am29Fxxx family of 5V flash memories. FlashICE helps you with three main types of tests. First, it allows you to verify that you are correctly controlling the flash memory. The FlashICE works only with flash memory that uses an embedded algorithm. Your software must send the appropriate series of bytes to the flash memory, and then the memory takes over to perform the actual operation. The FlashICE verifies that you are sending the correct series of bytes.

The second test profiles sector write and erase cycles. Some applications require you to level the wear on the flash memory because logging data to the same memory location quickly wears out flash memory. But, storing data throughout the flash memory lengthens the memory's life. The FlashICE logs write/erase cycles to ensure that your wear-leveling algorithm is accessing all sectors equally.

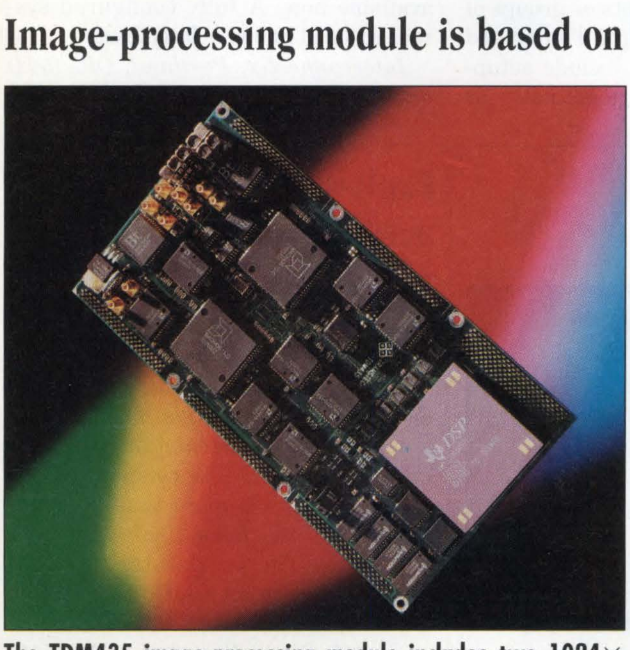
The third test is a simulation of errors. You can force a flash-memory error and then verify that your software properly handles the error.

The FlashICE flash-memory emulator connects to a target, much as a ROM emulator does. Functionally, the emulator looks just like the flash memory, and you can use it like any ROM emulator for code development. $2995.

—David Shear

Grammar Engine Inc, Westerville, OH. (614) 899-7878. **Circle No. 304**

Image-processing module is based on TMS320C40 DSP



The TDM435 image-processing module includes two 1024× 1024-pixel frame buffers.

The TDM435 image-processing module incorporates a programmable-resolution 8-bit monochrome frame grabber with two 1024×1024-bit video-RAM (VRAM) frame buffers, 4 Mbytes of zero-wait-state local memory, and a programmable-resolution RGB graphics-display section with a 4-bit overlay plane.

The high-resolution, TMS320C40-based module captures full-frame CCIR- and RS170-standard video, as well as high-resolution-camera video. Its architecture allows for simultaneous capture, display, and access by the C40 to the same block of VRAM.

The TDM435 comes with a graphics and capture-control library that facilitates display setup, window management, draw and fill operations, look-up-table control, and image-acquisition control, including live capture to a window.

The module is based on the TIM-40 specification and connects to global memory on a mother board, such as the TDMB410 PC, which can accept up to four TIM-40 modules. The TDM435 costs $7000.—**David Shear**

Transtech, Ithaca, NY. (607) 257-6502. **Circle No. 305**

Board-level design moves beyond place and route

Not that long ago, pc-board design was mostly a matter of finding a placement that let you efficiently route a design. As circuit speeds increased, clock-distribution lines and other critical signals started needing special attention during layout to meet timing and signal-integrity requirements. The typical practice was to start with a placement you hoped would avoid signal-integrity problems; then, after routing signals, you tried to mop up whatever signal-integrity problems were left.

The IS timing-driven floor planner computes slack allocation in real time for all critical timing paths. It displays violations graphically and in tabular form.

Today, circuit speeds are moving even higher, and the interconnection problem is mushrooming to include not just a few but many of the signals on high-speed pc boards and multichip modules.

To work with demanding high-speed board designs, Interconnectix is launching its interconnection-synthesis technology product, IS. The tool takes the interconnection requirements, including netlist, timing, and signal purity, and synthesizes a physical implementation to meet those requirements. Instead of iteratively modifying a physical design to meet timing and signal-integrity requirements, the tool attempts to find a workable design before going into layout.

The tool comprises four major modules: a hierarchical timing and thermal-driven floor planner, a physical-analysis engine, a spreadsheet-based rules engine, and a synthesizer with an intelligent router.

You start by capturing your design either in schematic or hardware-description-language form and then compiling the design into a netlist. The tool accepts netlists in a variety of standard formats and accepts timing constraints in the Standard Delay Format (SDF) file. Next, you specify rules using a spreadsheet for elements or groups of elements within the design. Timing and signal-purity rules can include setup-and-hold-time specifications; path- or net-based time delay; skew management; and maximum allowable crosstalk, overshoot, undershoot, and ringback constraints.

Once you provide a netlist, design constraints, and models, you are ready to develop a physical design. The timing-driven hierarchical floor planner lets you create and physically arrange functional groups. It automatically generates net topology, termination strategy, and power-density management to simplify floor planning. As you develop a floor plan, timing-path estimates and slack-time allocation help you track interconnection timing problems and whether the floor plan works.

After you develop a workable floor plan, you can put the intelligent router to work. The synthesis-and-router module makes routing decisions based on manufacturing-design rules and on the electrical constraints you specify. Synthesis continues until the tool creates an implementable physical representation that satisfies the electrical description.

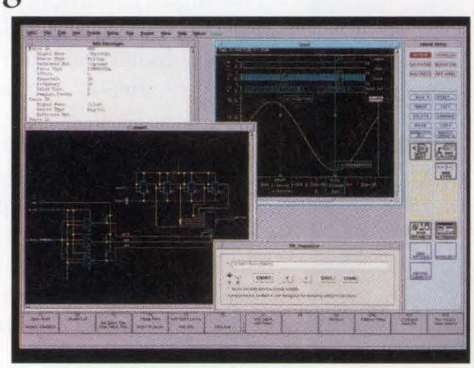
IS runs on Unix workstations and is available now. A fully configured system costs $170,000.—**Doug Conner**

Interconnectix, Portland, OR. (503) 684-6641. **Circle No. 306**

Mixed-signal simulator accepts analog behavioral language

The Continuum mixed-signal-simulation tool ties the QuickSim II digital simulator with the AccuSim II analog simulator using a simulation-backplane approach. AccuSim II integrates Anacad's Eldo simulator with Mentor Graphics' Spice simulator. The simulator accepts HDL-A, Anacad's proprietary VHDL-based analog behavioral language. Continuum will be available in July and costs $65,000.

Mentor Graphics, Wilsonville, OR. (503) 685-8000. **Circle No. 307**



The Continuum mixed-signal simulator accepts analog behavioral language.

Fault-simulation accelerator offers interactive fault tracing

The Paradigm Super Fault XP includes an interactive fault tracer that lets you view the path of a fault through a design during simulation. The information is useful in determining where a fault was blocked. The company claims the accelerator is more than 20 times faster than the fastest software fault simulator. The accelerator provides fault simulation for 64,000 to 4 million gates. Prices start at $79,900.

Zycad Corp, Fremont, CA. (510) 623-4400. **Circle No. 308**

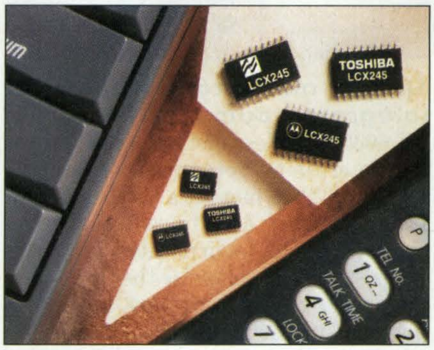
 CIRCLE NO. 189

CMOS logic series lets you mix 3 and 5V devices

The Crossvolt logic series from National Semiconductor comprises five CMOS families, which enable designers to mix 3 and 5V devices in a system. The families provide standard bus interfaces, which address the need for 3V devices to operate with 5V devices.

The LVX-X dual-supply translating transceivers operate from 3.3 and 5V supplies. The family suits 3V CPUs, which must interface to 5V buses and traditional 5V components. Two of the LVX-X devices offer configurable I/O translation on the fly for PCMCIA (Personal Computer Memory Card International Association) PC card slots. The devices enable a laptop computer to support a 3.3 or a 5V PCMCIA card. The translating receivers in a QSOP cost $2 (1000).

The LCX low-voltage octal and 16-bit buffers and transceivers provide 5V-tolerant inputs and outputs. The $2 (1000) devices enable complete 3V or both 3 and 5V operation in one design. The LCX family is the result of National Semiconductor's joint-development partnership with Toshiba and Motorola.



A joint agreement involving Toshiba, National Semiconductor, and Motorola has produced a family of 3V CMOS buffers and transceivers with 5V-tolerant inputs and outputs.

The LVX 10-bit low-impedance bus switches provide a high-speed bidirectional interface between buses with mixed voltages, 3V CPUs, and low-cost 5V dynamic RAMs. The 250-psec bus switches feature a current drain of 3 μA. Price is $2 in a QSOP (1000).

The LVX low-voltage gates, multiplexers, and octal transceivers have 5V tolerant inputs. The devices feature low power and noise for portable laptop or personal-digital-assistant applications. Toshiba provides an alternate source for the devices. Prices for the LVX family range from $0.92 for a flip-flop to $1.62 for an octal transceiver (1000).

Introduced last year, the LVQ Quiet devices suit only 3.3V applications that do not require interfacing with 5V devices. An LVQ device in a QSOP costs $1.25 (1000).—**John Gallant**

National Semiconductor, Santa Clara, CA. (800) 272-9959.

Circle No. 309

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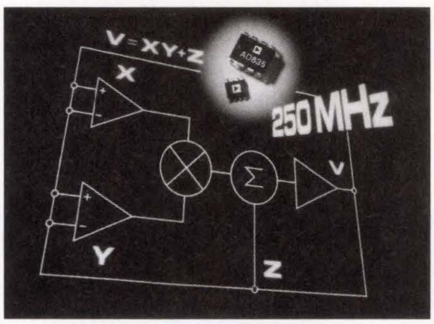
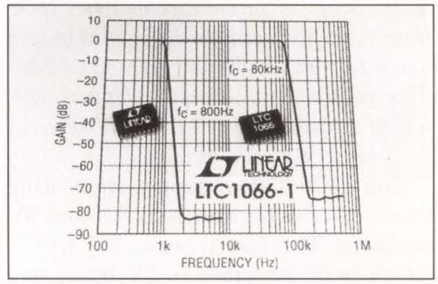
Spindle motor controller/driver integrates output drivers. The ML6035 brushless motor controller uses a zero-crossing rotor-position sensing technique that monitors the back EMF from the motor coils to control commutation. The IC incorporates six drive transistors that comprise the three complementary output drivers needed to power 3-phase brushless dc motors' windings. Each output can drive 1A at 1Ω. The 5V IC draws 6 mA, and a serial bus minimizes the number of external control pins. In a 32-pin thin QFP, $6.95 (1000). **Micro Linear Corp**, San Jose, CA. (408) 433-5200. **Circle No. 375**



Four-quadrant multiplier has 250-MHz bandwidth. The dc-coupled, voltage-output AD835 has a small-signal rise time of 1 nsec; full-scale ±1V rise and fall times are 2.5 nsec with 150Ω loads. Settling time to within 0.1% of full scale is typically 17 nsec. Typical noise is 44 nV/√Hz. The IC requires few external components; its X and Y differential multiplication and Z summing inputs are high-impedance nodes that don't require signal conditioning. The low-impedance outputs don't need additional buffering to drive ±2.5V into 50Ω loads. With ±5V supplies, the multiplier operates from –40 to +85°C. In 8-pin DIPs and SOICs, $7.95 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428. **Circle No. 376**

RS-485 transceiver consumes 300μA max. The low-power SP485 half-duplex transceiver, the first in a family of RS-485 devices, uses BiCMOS technology and meets the standard's requirements up to 5 Mbps. A half-duplex arrangement and a wide common-mode input range allow you to use the part in multipoint data-transmission networks. In 8-pin DIPs and SOICs, $1.10 (1000). **Sipex Corp**, Billerica, MA. (508) 667-8700. **Circle No. 377**



Lowpass filter has 14-bit dc-gain linearity. The LTC1066-1 is an 8th-order, pin-selectable elliptic or linear-phase filter with a clock-tunable cutoff frequency of 10 Hz to 100 kHz. An internal servo loop and precision op amp produce dc performance of 14-bit gain linearity and 1.5-mV offset over temperature. The filter IC's S/N ratio is 92 dB. Passband ripple is ±0.15 dB, and an 80-dB stopband attenuation occurs at 2.3× the cutoff frequency. $16.94 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 378**

Linear regulators each provide two voltage levels. The CS-8167, -8147, and -8157 feature an array of logic-control functions, low-quiescent sleep modes, and output voltage levels of 9, 10, and 12V, respectively. The tolerance on these primary outputs is ±2.5%, and output current is 500 mA. Each device also has a 5V ±5% secondary output that can source 70 mA. A CMOS enable pin puts the regulators into sleep mode, which reduces quiescent current to 70 μA. The devices can survive load dumps of 60V and reverse-polarity transients of –50V minimum. They feature short-circuit and thermal-runaway protection. In 5-lead TO-200 packages, $1.10 (10,000). **Cherry Semiconductor Corp**, East Greenwich, RI. (401) 885-3600. **Circle No. 379**

Read-channel IC set handles 64-Mbps data. The 2-chip Disk Reader set includes the PCA1151 pulse qualifier and equalizer and the PCA1161 data separator in 44- and 52-pin packages. The pair provides servo burst capture, 64-region zone switching, write compensation, and a 1.7 ENDEC for data rates as fast as 64 Mbps. The set offers five power-down modes and shifts from sleep to full-power mode in 2 μsec. Evaluation set, $25. **GEC Plessey Semiconductors**, Scotts Valley, CA. (408) 438-2900. **Circle No. 380**

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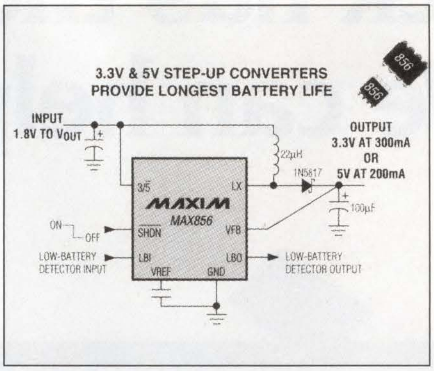
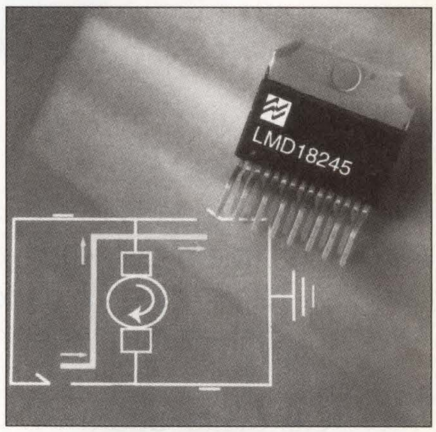


Converters boost two cells to 3.3 or 5V. The MAX856 to 859 family current-limited, step-up dc/dc converters combine efficiency, low-quiescent current, and very low shutdown current. For example, the MAX856 draws 25 µA, and its efficiency exceeds 85% when delivering 5V at 50 mA from a 2.5V input. Shutdown current is 1 µA maximum. The 856 and 857 deliver 100 mA at 5V; the 858 and 859 deliver 25 mA. The 856 and 858 have a pin-selectable 3.3 or 5V output. Two resistors fix the adjustable output of the 857 and 859 from 2.7 to 6V. A low-battery detector is built in. In 8-pin packages, from $1.60 (1000). **Maxim Integrated Products,** Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 381**

Devices implement SONET/SDH standard. Three new devices for implementing SONET are the Level 3 Mapper, which maps DS-3 or E-3 line signals into the SONET/SDH format; the advanced DS-3/STS-1 receiver/transmitter, which provides a single-chip line interface for DS-3 and STS-1; and the M13E, which multiplexes and demultiplexes 28 DS-1 signals into a DS-3 signal. Level 3 Mapper provides SONET or SDH mapping for both North American DS-3 lines at 45 Mbps and European E-3 lines at 34 Mbps. The receiver/transmitter performs the transmit and receive line-interface function required for STS-1 and DS-3 signal transmission. Level 3 Mapper, $182; receiver/transmitter, $45; M13E, $211 (1000). **Transwitch Corp,** Shelton, CT. (203) 929-8810. **Circle No. 382**

Frequency synthesizers integrate fractional-N division. The SA7025 and SA8025 integrate a high-frequency prescaler with a fractional-N, phase-locked-loop synthesizer on a single chip. The devices meet the fast switching requirements of IS-54 cellular and Japanese digital-cellular and cordless standards. The SA7025 provides coverage to 1 GHz; the SA8025 handles coverage to 2 GHz. A high-speed, 3-wire serial interface handles programming and channel selection. An adaptive filter with a programmable speed-up mode uses two filter designs with different charge-pump currents. In 20-pin SSOPs, SA7025, $6.50; SA8025, $8 (1000). **Philips Semiconductors,** Sunnyvale, CA. (800) 447-1500, ext 3012. **Circle No. 383**

Instrumentation amp consumes 350 µA. The INA118 operates with dual power supplies from ±1.35 to ±18V and single supplies down to 2.7V. The 3-op-amp, current-feedback architecture provides wide bandwidth at gains to 10,000. For example, the bandwidth is 500 kHz at a gain of 10. A single resistor sets the gain from 1 to 10,000. The IC protects its inputs up to ±40V with or without power applied. Other key specs include 50-µV offset voltage and 0.5 µV/°C offset drift, 5-nA input bias current (all maximum), and 110-dB minimum CMRR. Operating temperature range for the 8-pin DIPs or SOICs is –40 to +85°C. $3.25 (1000). **Burr-Brown Corp,** Tucson, AZ. (800) 548-6132. **Circle No. 384**



3A motor driver uses PWM. The LMD18245 55V H-bridge driver controls motor velocity directly through a pulse-width modulator, unlike linear controllers, which require two external power amps. The IC also features a 4-bit DAC for digital current control. In response to logic-level signals at the DAC's input, the IC uses a fixed off-time control scheme to regulate motor velocity; it does so by switching the bridge on and off at a variable high frequency, which controls the current to the motor. $R_{DS(ON)}$ per switch is 0.3Ω. Protection features include thermal shutdown, current limit, and undervoltage lockout. $8.45

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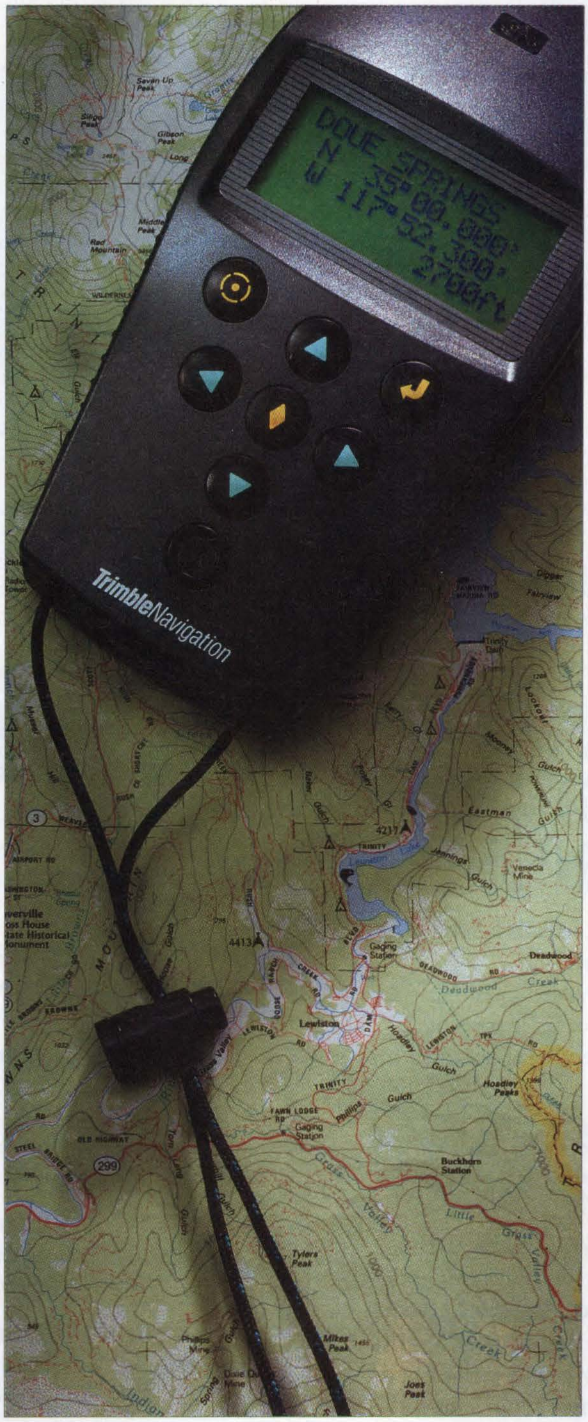

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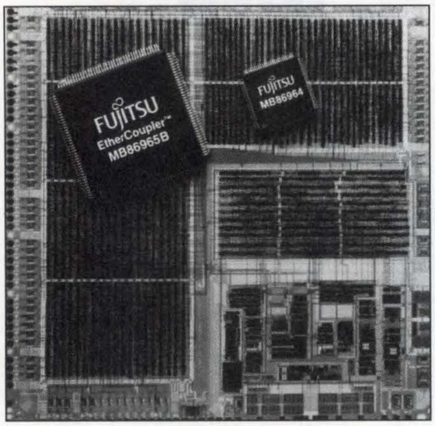
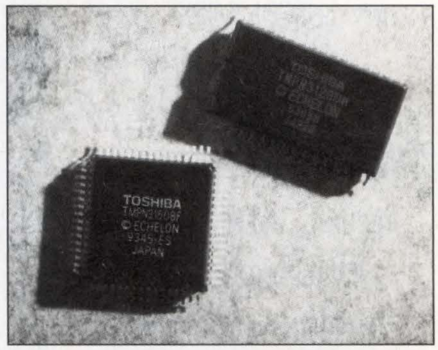
(1000) in 15-lead TO-220 packages. **National Semiconductor**, Santa Clara, CA. (408) 721-6937. **Circle No. 385**



Ethernet controllers match diverse system needs. The MB86964 and MB86965B Ethernet controller ICs include onboard 10BaseT transceivers, Manchester codecs, and transmit/receive filters. The MB86964 comes in a 100-pin shrink quad flat pack and offers a generic interface, suiting it for embedded applications. The 160-pin MB86965B offers an ISA interface and includes a full-duplex Ethernet interface. It suits add-in-card applications. MB86964, $15.25; MB86965B, $16.65 (10,000). **Fujitsu Microelectronics Inc**, San Jose, CA. (800) 642-7616. **Circle No. 386**

Logic devices operate at 3V. PEEL18CV8L is a 3V programmable electrically erasable logic (PEEL) device. The devices typically draw 5 mA from a 3V supply. PEELs provide 1/8 to 1/10 the power of traditional bipolar devices. Compared with a GAL device's five macrocells, the PEELs provide seven additional macrocell configurations, for a total of 12. $1 (10,000). **American Microsystems Inc**, Pocatello, ID. (208) 234-6668. **Circle No. 387**

RAMDAC operates at 135 MHz. The W30C491 is a RAMDAC that can operate at 135 MHz. It supports multiwindow displays and independent access to 16.8 million colors for each window. The RAMDAC can be used in XGA, Microsoft Windows, Targa, and Hi-Color GUIs. The chip offers eight software-selectable true-color modes of 15, 16, 18, or 24 bits. It also offers true-color bypass for direct D/A input access and an 8-bit pseudo-color mode. Integrated on the device are three 256×8-bit color lookup tables and three 8-bit D/A converters. 135-MHz version, $15.97. **IC Works Inc**, San Jose, CA. (408) 922-0202. **Circle No. 388**



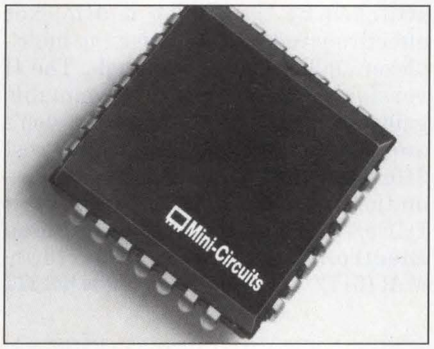
Neuron chips use Lontalk protocol. The TMPN3150BF and TMPN-3120BM are second-generation Neuron chips for use in Echelon Corp's Lonworks control network. The VLSI devices communicate with each other using the Lontalk protocol. Both chips contain 512 bytes of EEPROM for node

INTEGRATED CIRCUITS

addressing and configuration data. Each chip contains a unique 48-bit serial identification number that the application program can read for network configuration or product serialization. The chips have an operating current of 16 mA and a sleep mode of 15 μA. Either device, $5 (10,000). **Toshiba America Electronic Components Inc**, Irvine, CA. (714) 455-2000.
Circle No. 389

Cache SRAMs feature 7-nsec access time. Five application-specific cache SRAM modules are available for the Intel Pentium μP and the IBM/Motorola PowerPC μP. The MCMs (multichip modules) feature clock to level-two cache array access times as fast as 7 nsec. Three of the new modules are customer-configurable as 64k×72, 128k×36, or 256×18 bits. Two additional SRAMs are available in fixed 32k×72-bit configurations. The MCM SRAMs are designed for small skew and low noise, and a small form factor reduces line lengths. All of the MCMs run from a 5V supply. $400 for a 4-Mbit device. **Micromodule Systems** Cupertino, CA. (408) 864-7437. **Circle No. 390**

GaAs SP4T switch has wide bandwidth. The GSWA-4-30DR GaAs SP4T switch has a dc to 3000-MHz bandwidth. The device comes in a 28-pin PLCC package that has strain-relief J-leads. Other features include 25-nsec



switching time; 0.9-dB insertion loss; 30- to 40-dB isolation; and 50Ω RF ports. The switch can be used as an antenna switch in a 2-way radio receiver or as a filter or local oscillator selector. $19.95. **Mini-Circuits**, Brooklyn, NY. (718) 934-4500. **Circle No. 391**

PLD pair offers low power. Two complex programmable logic devices are available in 44-pin PLCCs, ceramic leadless chip carriers, or ceramic leaded chip carrier packages. The ATV2500B offers a propagation delay of 12 nsec and typical pin-to-pin delays of 10 nsec. The low-power ATV2500BL offers 2-mA standby current. The devices contain 24 flexible macrocells that each have 17 product terms, which are globally connected by a single AND/OR matrix. Each macrocell has two flip-flops that can be configured as either D- or T-types. $19.75 (100). **Atmel Corp**, San Jose, CA. (408) 441-0311. **Circle No. 392**

Logic device combines CMOS and EPROMs. The PEEL22CV8 is a 24-pin replacement for the GAL20V8. The programmable electrically erasable logic (PEEL) device combines CMOS and EEPROM technologies. CMOS PLDs replace bipolar devices and the erasability provides an alternative to conventional PLDs and GALs. The PEELs also have a faster erase time than GALs by a factor of 10. The device provides independent output enables and two additional input pins. $0.60 to $3. **American Microsystems Inc**, Pocatello, ID. (208) 234-6668. **Circle No. 393**

Graphical tool builds custom data-acquisition applications. With Visual Designer V2.0, function blocks selected from a menu appear on the screen as icons that you link to establish data flow. The latest version ($595 until July 31) adds 14 blocks, including one for serial-communication, which extends control to RS-232C/422/485 devices; the tool previously supported only ISA-bus boards. Other new blocks include a DDE client block that lets the software receive data from other Windows applications (the earlier version allowed sending of data only), an X-Y plot block, and a load block that lets you run other Windows programs without leaving Visual Designer. **Intelligent Instrumentation**, Tucson, AZ. (602) 623-9801. **Circle No. 320**

Digital IC-test systems suit evaluation and production testing. The HP 83000 F240i and F330i (240 and 330 MHz, external test head, from $3300/pin) are for prototype evaluation and analysis of defective ICs (complex RISC and CISC μPs, peripheral and support chips, and telecommunications devices, for example). The F80t and F120t (80 and 120 MHz, integral test head, from $4100/pin) are for high-volume production testing. The systems, which can change waveforms and timing on the fly, accommodate as many as 512 pins now and can expand to as many as 1024 in the future. Pattern memory stores 4M vectors. The 80- and 120-MHz systems' overall timing accuracy is ±300 psec. Shipments will begin this fall. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 321**

1M-sample/sec ADC boards have an amplifier per channel. The WIN-30PGH and PGL boards operate even faster than 1M-sample/sec ADC boards whose several channels share a programmable-gain amplifier. Using an amplifier per channel does away with the need to wait for amplifier settling. Moreover, the higher level of the signals

switched by the analog multiplexer effectively reduces the noise the multiplexer adds to low-level signals. The H version's software-programmable gains are 1, 2, 4, and 8; the L version's are 1, 10, 100, and 1000. The boards cost $1625 each, and both provide 12-bit resolution, two 12-bit DACs, two 16-bit DACs, and 24 digital I/O lines. **United Electronic Industries**, Watertown, MA. (617) 24-1155. **Circle No. 322**

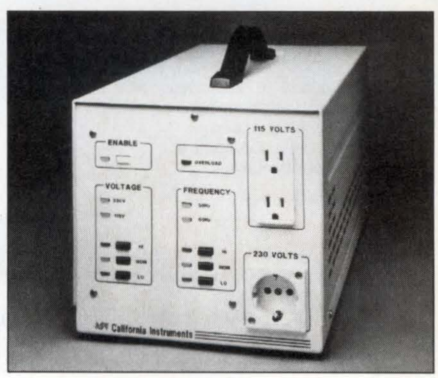
100M-sample/sec, 4-channel DSO boasts 2M-sample/channel memory. The VC-7124 offers a bandwidth of 150 MHz. It acquires data in both real-time and random-repetitive-sampling modes. At its fastest real-time sampling rate, it can acquire 20-msec records. You can also partition the acquisition memories to store many shorter records in quick succession (2000 1k-sample records, for example). In addition to the deep internal memories, the scope accepts PCMCIA cards that store as much as 4 Mbytes. The scope, which performs Go/No-Go testing, includes a built-in printer, an RS-232C port, and an IEEE-488 port. $12,500. **Hitachi Denshi America Ltd**, Torrance, CA. (310) 328-6116. **Circle No. 323**

Economical DSOs bring back the advantages of analog-scope displays without the drawbacks. The 54600B series of benchtop DSOs incorporate a second-generation custom waveform-processor IC that produces vector-enhanced displays, which indicate slew rate the way analog-scope displays do: Brighter traces denote more slowly changing signals; dimmer traces indicate signals that are changing more rapidly. The scopes' 1.5M-pixel/sec display rate allows refreshing the display 60 times/sec, even when 12 waveforms are on the screen. The 54600B series includes 2- and 4-channel units whose bandwidths range from 100 to 500 MHz and whose prices range from $2495 to $4995. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 324**

Electronic books provide on-line reference on thermodynamics, circuits, and differential equations. A series of electronic books works with the vendor's MathCad technical calculation software. Each book provides examples of problems, taking you through the process of breaking down the equation and interpreting the results. You can change numbers and watch the effect on solutions. The circuits and thermodynamics books cost $49 each; the differential-equation book costs $99. **Mathsoft Inc**, Cambridge MA. (617) 577-1017. **Circle No. 325**

Extender simplifies troubleshooting of PCMCIA cards. Model EXT-6800 plugs into PCMCIA sockets and accepts Type I and II PCMCIA cards. A right-angle socket on the extender provides access to both sides of the card under test. In addition, the extender provides access to all bus signals. A jumper on the extender lets you monitor the current drawn by the card under test from the 5V supply. $190. **Advanced Electronic Systems**, Lake Forest, CA. (714) 855-7271. **Circle No. 326**

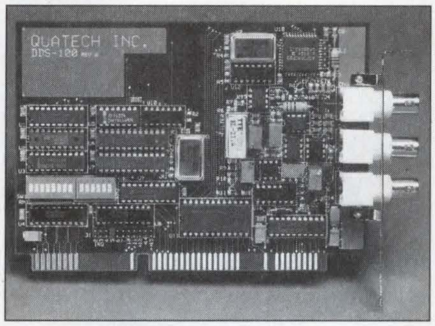
Software tailors HP 48 calculators for EEs' use. Even if you aren't familiar with the HP 48, you can use EE·Pro the first time you try it. The package includes on-line text help, a menu-navigation system with which you can quickly reach routines or reference data, and a key for setting the menu-scrolling speed. The package, which requires 5 kbytes of free calculator memory, comes on a plug-in expansion card for the 48GX and is fully compatible with the 48SX. $109.95, including a 330-pg user guide. **Sparcom Corp**, Corvallis, OR. (503) 757-8416. **Circle No. 327**



Portable unit supplies 1.3 kVA continuously at 50 and 60 Hz and five voltages for product testing. The fully isolated 1251WP produces 100, 115, 220, 230, or 240V ac with low distortion. It reliably starts loads whose inrush current is as much as 100A peak. You can select any voltage-frequency combination. Two of the 29-lb. units mount side-by-side in an 8.75-in. space in an EIA rack. From $2850. **California Instruments Corp**, San Diego, CA. (619) 279-8620. **Circle No. 328**

Software uses graphics to simplify data-acquisition-system setup. Fast-Daq uses National Instruments' LabView graphical instrumentation software and AT-MIO-16 series or Lab-PC+ data-acquisition boards. The $849 package helps you install boards, set switches, connect signals, and select sampling rates. Once the equipment is set up, the package automatically collects, stores, and displays the data. It lets you customize the displays or recall and display data recorded earlier. **Fast-Daq Engineering**, Maitland, FL. (800) 732-7832. **Circle No. 329**

Vendor bundles instrument-control library software with ISA-bus IEEE-488.2 interface card. With the 82335B, you can use routines from a standard I/O library or the vendor's SICL (Standard Instrument Control Library). SICL works with any Windows or DOS PC and with C, C++, Basic (including Visual Basic), and Pascal. Both libraries accompany the board, which, until September 30, costs $295. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 330**



ISA-bus board uses 32-bit direct-digital synthesis to create 20-Hz to 20-MHz sine waves. The DDS-100 produces TTL-compatible square waves at the same frequency as its sine waves. With appropriate software, such as the Windows application packaged with it, the board can produce FSK, AM, QAM, and phase-modulated outputs and output bursts. It can also do frequency hopping and create frequency sweeps. A phase-modulation register lets you use software to control the output phase. $495. **Quatech Inc**, Akron, OH. (216) 434-3154. **Circle No. 331**

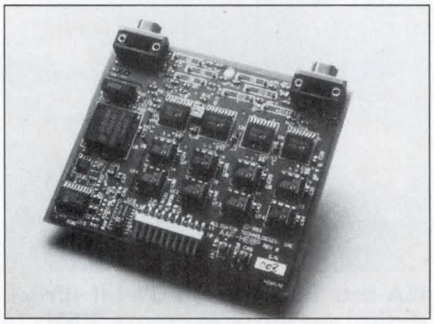
Memory of 4-channel, 60-MHz analog/digital scope expands to 128k samples/channel. The 2216's standard memory depth is 16k samples/channel, but you can expand it to 128k. The scope, which offers a parallel printer port and is fully programmable via RS-232C and IEEE-488 ports, also functions as an analog instrument. The maximum real-time acquisition rate in DSO mode is 20M samples/sec. In the random repetitive sampling mode, the scope allows pretrigger viewing to 100% of its memory depth. The unit makes 15 types of automated measurements and permits cursor measurements of voltage, time, and frequency. $3995; expanded memory, $1290. **Tektronix Inc**, Beaverton, OR. (800) 426-2200. **Circle No. 332**

Handheld DMMs tailor features and prices to user needs. Depending on which model you select, the

971A, 972A, 973A, and 974A offer 3½- or 4½-digit resolution. All models measure ac and dc voltage, current, frequency, and resistance and perform diode and continuity tests. Two models have true rms ac and ac+dc ranges. Two models measure capacitance and provide dual digital readouts. $195 to $370. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 333**

$495 data-acquisition package runs under Macintosh System 7. Igor Pro V2.0 can acquire and display data in real time. User-defined buttons and displays let you use the "System 7 savvy" application to build custom control panels. The package, which you can operate interactively by pointing and clicking or by issuing commands, can also execute programs that you create. Upgrades from earlier versions cost $200. **Wavemetrics Inc**, Lake Oswego, OR. (503) 620-3001. **Circle No. 334**

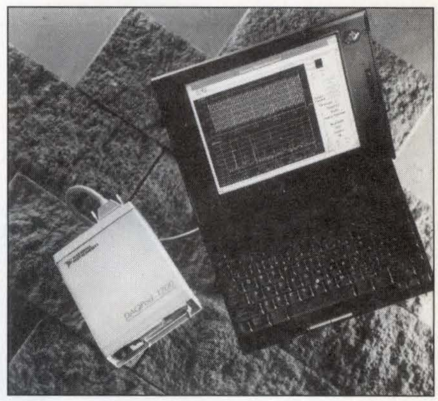
Test probes with switchable 10× attenuators add functions to Fluke ScopeMeters. The fully insulated 6033, a $125 kit of two probes (a red one and a gray one), and the 6035, a $95 individual probe, offer switchable ×1 and ×10 attenuation. The probes, which withstand 360V rms and are rated to operate to 200 MHz, terminate in insulated BNC connectors. **ITT Pomona Electronics**, Pomona, CA. (909) 469-2900. **Circle No. 335**



8-channel antialiasing filter programs from 1 Hz to 50 kHz via RS-232C. Unlike other switched-capacitor active filter boards, the $3995 AAF-HE8P does not plug into a standard bus. You can, however, daisy-chain 16 of the boards and control them from one RS-232C port. The boards have 5-pole Butterworth response with ±0.2-dB typ passband ripple to 0.8 f_C. Channels are phase-matched within ±0.5° typ. The boards require 7.5V at 175 mA, –7.5V at 185 mA, and 5V at 40 mA. **Alligator Technologies**, Costa Mesa, CA. (714) 850-9984. **Circle No. 336**

$79.95 handheld tester checks Ethernet cabling. The DXB65 separates into remote and master sections that you can use independently to test installed wiring or rejoin for bench testing of patch cords. **L-com Inc**, North Andover, MA. (508) 682-6936. **Circle No. 337**

VXIbus ARB now accommodates 512k-point memory. With a $595 128k-point memory option or a $1995 512k-point option, the $4995 SCPI-compatible model 1395 can store long waveforms or multiple shorter ones. (Segments can be as short as five points.) With these options, the vendor has redesigned the waveform-management system to keep programming tasks from proliferating. **Wavetek Corp**, San Diego, CA. (619) 279-2200. **Circle No. 338**



$995 5.7538.37531.5-in., 1.7-lb unit adds data acquisition to notebook PCs. The DAQPad-1200 works with any PC that has a parallel printer port; it transfers data faster when connected to an enhanced parallel port (EPP). The unit receives power from an ac adapter or from a $295 battery pack from which it operates for nine to 12 hours. There are eight single-ended analog inputs (four channels differential), two 12-bit DACs, 24 lines of TTL I/O, and three 16-bit counter timers. Speed of the 12-bit ADC is 100k samples/sec; the unit includes a 2k-sample FIFO ADC buffer. A programmable-gain amplifier boosts signal levels from one to 100 times in seven steps. **National Instruments Corp**, Austin, TX. (512) 794-0100. **Circle No. 339**

PCMCIA disk drives compete for storage-capacity championship

The PCMCIA disk drive with the highest storage capacity is
a. Intégral's 170-Mbyte Viper
b. Maxtor's 131-Mbyte MobileMax
c. MiniStor's 260-Mbyte More MB
d. All of the above.

The correct answer could be "d," but it's hard to tell for sure. All three companies have laid claim to "highest capacity" honors, and each claim may actually be valid. Qualifiers attached to the claims explain the apparent contradictions.

First, Intégral announced shipment of its 170-Mbyte Viper drive. Then, MiniStor announced availability of its 130-Mbyte More MB drive with an onboard compression utility that doubles capacity to 260 Mbytes. (You can disable compression if you wish.) Finally, Maxtor claimed its 131-Mbyte MobileMax is the highest capacity PCMCIA disk drive in volume production. So, depending on how many drives you need (and when) and how you feel about data compression, any one of the drives might be the most capacious available to suit your needs.

Shock tolerance also figures in the marketers' claims. Intégral says its drives can withstand a 750g nonoperating shock, MiniStor claims 900g shock tolerance, and Maxtor claims 600g tolerance. MiniStor also provides a storage and transport pouch, called the Pocket Socket, that boosts shock tolerance to 1200g. Operating shock tolerance for the drives ranges from 80g (Maxtor MobileMax, z axis) to 100g (Integral Viper, 2-msec linear pulse) to 120g (MobileMax, x and y axes) to 200g (MiniStor More MB, measurement method unspecified). Unfortunately, no standard exists for measuring disk drives' shock tolerance (see "Small rugged disk drives take (fairly) hard knocks," *EDN*, November 11, 1993, pg 41).

Other manufacturer-supplied specifications reveal few major differences in the disk drives. Power consumption varies the most, with MiniStor and Maxtor having an advantage during operation and with Integral edging out MiniStor during standby and sleep. Some of the best specs for typical power consumption are

- Active—0.6W, Maxtor
- Read/write/seek—1.25W, MiniStor
- Standby—45 mW, Intégral and Ministor
- Sleep—25mW, Intégral.

Average seek time is 15 msec for the Intégral and MiniStor drives, 19 msec for the Maxtor drive. Start-up time, important in portable devices that power-down disk drives that aren't being accessed, is 1.5 sec for Intégral and Maxtor, 2.5 sec for MiniStor.

Prices for the small disk drives are remarkably similar: $499 each.

—Gary Legg

Intégral Peripherals, Boulder, CO. (303) 449-8009. **Circle No. 301**

Maxtor Corp, San Jose, CA. (408) 432-1700. **Circle No. 302**

MiniStor Peripherals Corp, San Jose, CA. (408) 943-0165. **Circle No. 303**

PCMCIA disk drives are increasing their storage capacity. With built-in data compression, the More MB drive from MiniStor can hold 260 Mbytes.

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Video moves to HP workstations. The PowerVideo 700 series of EISA-bus cards puts full-size, full-motion, true-color video on Hewlett-Packard 9000 Series 700 workstations. The cards let you display, digitize, compress, and store video and take advantage of optional analog input. Optional software tools, which work with HP's Mpower 2.0 collaborative multimedia software product, help you develop video-enabled applications. Prices for the cards, with various options and configurations, range from $2995 to $4995. **Parallax Graphics Inc**, Santa Clara, CA. (408) 727-2220. **Circle No. 418**

ISA-bus DSP card targets multimedia and telephony. TeraDON, an ISA-bus card, uses as many as 16 AT&T DSP3210 floating-point signal processors to provide peak performance of 533 MFLOPS. Available software for the card includes ready-to-run multimedia and telephony modules for incorporating fax capabilities, modems, text-to-speech conversion, speech recognition, audio compression, and still-image compression. The card runs AT&T's VCOS multimedia operating system. With four processors, $3995; with 16 processors, $9995. **Ariel Corp**, Highland Park, NJ. (908) 249-2900. **Circle No. 419**

Removable-cartridge disk drive stores 270 Mbytes. The SyDOS 270MB series of removable-cartridge disk drives stores 270 Mbytes and provides 13.5-msec average seek times. The 3.5-in. drives are also compatible with 105-Mbyte cartridges. $500 to $700; cartridges, <$100. **SyDOS**, Boca Raton, FL. (407) 998-5400. **Circle No. 420**

200-Mbyte drive accommodates earlier SyQuest cartridges. The 5.25-in. SQ5200C removable-cartridge disk drive stores 200 Mbytes and is compatible with earlier 44- and 88-Mbyte SyQuest cartridges. The drive has a SCSI II interface and an average access time of 18 msec. MTBF is 100,000 hours. Drive and cartridge, from $599; cartridge only, $99 to $109. **SyQuest Technology**, Fremont, CA. (510) 226-4000. **Circle No. 421**

Flat-panel computer has 14-in. color LCD. The DisplayPac-Vista combines a 14-in., 262,000-color TFT LCD with a 486DX-based computer and a resistive touchscreen. The package fits in a 12.5×15.5×4.5-in. metal, open-frame panel mount, and a 19-in. rack-mount version is also available. From $7435 (OEM). **Computer Dynamics**, Greer, SC. (803) 877-8700. **Circle No. 422**

Workstation features 70-MHz MicroSPARC II. The micro COMPstation, based on a 70-MHz MicroSPARC II processor, provides performance estimated at 50 SPECint92 and 43 SPECfp92. It's available with 16 to 256 Mbytes of memory, three SBus slots, and Solaris 1.1.1B software. Available color monitors range from 14- to 20-in. versions. From $5000. **Tatung Science & Technology Inc**, Milpitas, CA. (800) 659-5902. **Circle No. 423**

Cursor controller works in harsh environments. DuraPoint, a ruggedized cursor controller, works in harsh environments, including wet areas and outdoor installations. The device is environmentally sealed and completely immersible. It's also resistant to shock, vibration, and most cleaning solutions. The controller is available in stand-alone and panel versions. $279. **Interlink Electronics**, Camarillo, CA. (805) 484-8855. **Circle No. 424**

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PKC series 15-18 watt DC/DC converters with up to three regulated outputs. 10.5mm height

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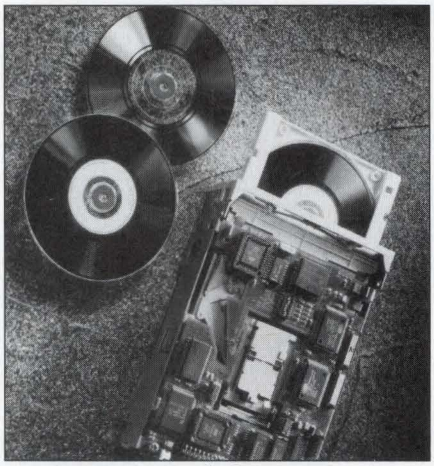
United States:	Richardson, TX, Tel: +1-214-997-6561 Fax: +1-214-680-1059

ERICSSON

CIRCLE NO. 185

Quad-speed CD-ROM drive has fast access. The Teac Super Quad, a quad-speed CD-ROM drive, provides data transfers of 600 kbytes/sec and an access time of 195 msec. The drive supports CD-ROM XA (extended architecture), has multisession photo-CD capability, and complies with MPC Level II. It has a 5.25×1-in. form factor. $399. **Teac America Inc**, Montebello, CA. (213) 726-0303. **Circle No. 425**

Color flat-panel display serves SPARCstations. A flat-panel display subsystem, comprising of the C5020 color active-matrix TFT display and the S20VGA frame buffer, makes a compact monitor for Sun workstations. The 9.4-in. (diagonal), 640×480-pixel screen displays 256 colors from a palette of 16.8 million; refresh rate is 60 Hz. The S20VGA is register-compatible with Sun's CG3 driver. $4295. **Integrix Inc**, Newbury Park, CA. (800) 300-8288. **Circle No. 426**



Magneto-optical drive stores 230 Mbytes. The LB3230 magneto-optical disk drive stores 230 Mbytes on a 3.5-in. mageneto-optical cartridge and has an average seek time of 28 msec. It also handles erasable optical-read-only-memory (OROM) and partial-ROM media and is compatible with 128-Mbyte cartridges. Burst-transfer rates are 4 Mbytes/sec; streaming data-transfer rates range from 920 kbytes/sec (zone 0) to 1.47 Mbytes/sec (zone 9). $800. **LaserByte Corp**, Sunnyvale, CA. (408) 734-9200. **Circle No. 427**

Graphics accelerators work on PCI bus. The GE 64 PCI and the Prostar 64 PCI graphics-accelerator cards provide a choice of performance levels for the PCI bus. Each card has 64-bit bandwidth and 32-bit bus transfers; the GE 64 delivers 16.8 million colors to 1024×768-pixel displays, and the Prostar 64 provides 65,536 colors at that resolution. The $229 GE 64 uses S3 Vision 864 accelerator chip; the $189 Prostar 64 uses Cirrus Logic's 5434 chip. **Actix Systems Inc**, Santa Clara, CA. (408) 986-1625. **Circle No. 428**

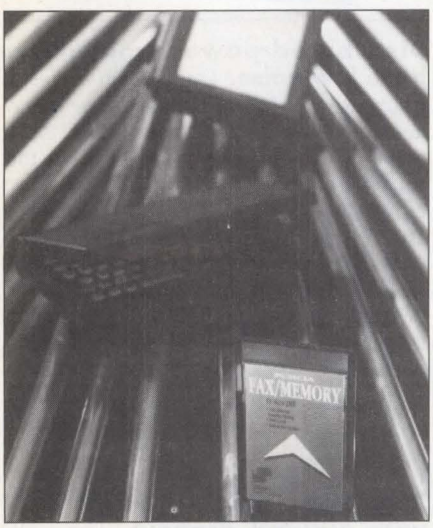
MPEG compression software runs on Windows. XingCD software provides full-screen MPEG-I compression

COMPUTERS & PERIPHERALS

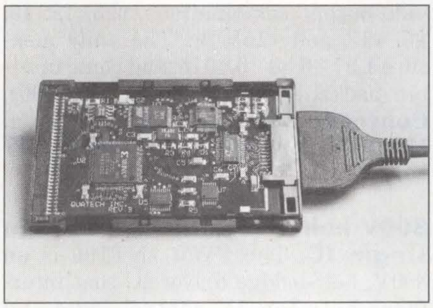
for Windows applications without MPEG hardware. It produces MPEG video streams from TGA, AVI, or BMP formats; it handles 352×240-, 320×240-, and 160×120-pixel images. $995. **Xing Technology Inc**, San Jose, CA. (800) 294-6448. **Circle No. 429**

Large color display suits demanding applications. The PrecisionColor Display/21 monitor puts 16.7 million colors in sharp edge-to-edge focus on a 21-in. screen. Its multiple-frequency capability allows configuration from 1024×768 to 1360×1024 pixels. Dot pitch is 0.28 mm. $2499. **Radius Inc**, San Jose, CA. (800) 227-2795. **Circle No. 430**

SCSI kits handle multimedia. Six new 16-bit SCSI host-adapter kits offer a variety of hardware and software options for multimedia CD-ROM applications. Versions are available with and without a floppy-disk controller; with and without CorelSCSI software; and with and without drivers for Windows NT, OS/2, Novell NetWare, and SCO Unix. From $140 (100). **Rancho Technology Inc**, Rancho Cucamonga, CA. (909) 987-3966. **Circle No. 431**



PCMCIA card combines fax and memory. A Type II PCMCIA card combining memory and a fax helps overcome the limitations of low-memory, single-slot, portable computers. The Hayes-compatible modem has full-duplex communication at 2400 bps plus fax operation at 9600 bps. The card is available with 2 Mbytes of flash memory for $349 or with 4 Mbytes for $449. **Smart Modular Technologies**, Fremont, CA. (510) 623-1231. **Circle No. 432**



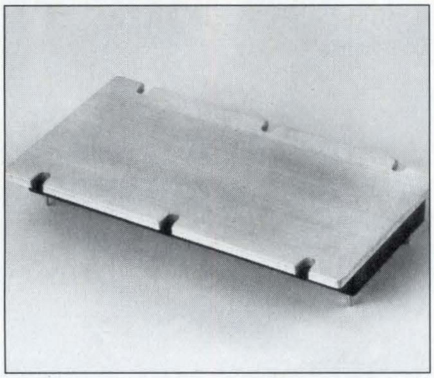
PCMCIA card holds RS-232C adapter. The SSP-100 packs a single-channel RS-232C asynchronous serial adapter in a PCMCIA card. The Type II card includes a 16550 UART and complies with release 2.1 of the PCMCIA standard. You can assign any COM port, interrupt level, and I/O address. $229. **Quatech Inc**, Akron, OH. (216) 434-3154. **Circle No. 433**

PCI local bus gets Ethernet controller. A new Ethernet adapter for the PCI bus has an independent 10-MHz serial clock and a PCI system clock that operates at speeds up to 33 MHz with no wait states. The card provides full support for 10BaseT, 10Base2, and 10Base5 connection in all popular network operating systems and supports IEEE 802.3, ANSI 8802-3, and Ethernet standards. A sleep mode reduces power consumption for battery-powered applications. $399. **CNet Technology Inc**, San Jose, CA. (408) 954-8000. **Circle No. 434**

Graphics card has PCI and VL versions. The WindowsVGA 64 graphics card, available in versions for the PCI and VL buses, provides 16.8 million colors on 1024×768-pixel displays. The DRAM-based card is based on Cirrus Logic's CL-GD5434 graphical-user-interface chip and has a 64-bit memory interface. The card is available with 1 Mbyte of memory (upgradable, via sockets, to 2 Mbytes) or with 2 Mbytes (upgradable to 4 Mbytes). 1-Mbyte version, $199; 2-Mbyte version, $289. **Genoa Systems Corp**, San Jose, CA. (408) 432-9090. **Circle No. 435**

POWER SOURCES

Switching power supplies meet military specifications. A line of MIL-SPEC universal-input switching supplies includes input filtering that meets MIL-STD-461C. The units comply with MIL-STD-454 and MIL-STD-2000. Units are available from 25W to 300W in single-, dual-, triple-, and quad-output versions. The units have a 3-year warranty. $845 to $2100 in small quantities. **Logitek Inc**, Ronkonkonkoma, NY. (516) 467-4200. **Circle No. 310**



Current sources supply constant current from batteries. The BatMod current-source modules run off batteries and deliver a programmable output current. The units measure 4.6×2.4×0.5 in. and handle currents up to 40A at 100V dc. One analog port controls the output-current level, and another controls the point at which the module switches from constant-current to constant-voltage mode. You can arrange the modules in series to handle voltages up to 500V dc. $150 (OEM qty). Delivery, 10 to 12 weeks. **Vicor Corp**, Andover, MA. (508) 470-2900. **Circle No. 311**

"Prismatic" NiMH cell stores 760 mAhr. The model HHF80T rectangular ("prismatic") nickel metal-hydride (NiMH) cell measures 0.67×0.24×2.64 in. and weighs 0.88 oz. You can recharge the cell in 1 hour. $8. **Panasonic Industrial Co**, Secaucus, NJ. (800) 848-3979. **Circle No. 312**

DIP-sized converter has ultra-high 8000V pk isolation. The 100VFI series of DIP-sized single- and dual-output 1.5W dc/dc converters feature 8000V pk (4000V steady-state) input-to-output isolation. Eighteen models operate from 5, 12, or 15V dc and provide output combinations of 5, 12, 15, ±5, ±12, and ±15V dc. The units measure 1.27×0.80×0.40 in. and come in 24-pin packages. $25.90 to $27.30 (100). **Conversion Devices Inc**, Brockton, MA. (508) 559-0880. **Circle No. 313**

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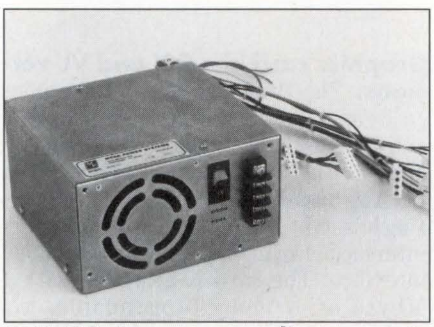
800V half-bridge driver comes in single IC. The PWR-INT100 is an 800V, half-bridge driver IC that interfaces between 5V control logic and MOSFETs driving high-voltage, 2-hp, brushless dc motors at rates up to 50 kHz. The IC incorporates a lockout for full-bridge implementations that prevents both high- and low-side transistors from turning on simultaneously. The drivers sink 300 mA and source 150 mA. $1.76 (1000). **Power Integrations Inc**, Mountain View, CA. (415) 960-3572. **Circle No. 314**

Hybrid converters meet military specifications. The 2680 series of 30W hybrid dc/dc converters operates from 28V-dc sources. The units exhibit MIS-STD-704 or -1275 surge characteristics and have MIL-STD-461 EMI filtering. The converters come in single-, double-, and triple-output models. They measure 0.495×1.34×2.12 in. Operating temperatures are from –55 to +115°C. $1014 (10). **Modular Devices Inc**, Shirley, NY. (516) 345-3100. **Circle No. 315**



IBM PC AT-type supplies operate from 12, 24, or 48V dc. A line of IBM PC AT-type supplies operates from 12, 24, or 48V dc inputs and handles 100, 125, or 240W, respectively. Input-output isolation is 500V dc. The supplies have short-circuit protection with automatic recovery. Operating temperature is 0 to 50°C. $187 (1000); delivery from stock. **Mesa Power Systems**, Escondido, CA. (619) 489-8162. **Circle No. 316**

SIP regulator lowers 5 to 3.3V dc. The PT6305N 5 to 3.3V regulator comes in a 12-pin SIP. The IC handles 3A at 85% efficiency max. It tolerates a 4.5 to 10.0V input-voltage range and has over-temperature and short-circuit protection. The unit measures 0.36×2×0.60 in. $19.90 (100); delivery, two to four weeks. **Power Trends Inc**, Batavia, IL. (800) 531-5782. **Circle No. 317**

Distributed-power converters have low noise. The PM900 series of ultra-low-noise, high-accuracy 5W dc/dc converters operate from 5, 12, 24, and 48V dc. The single- and dual-output units measure 2×2×0.42 in. Output ripple for single-ended units measures 10 mV p-p max, 6 mV p-p max for dual-ended. The units meet VDE 0871 Level B EMI requirements. Line and load regulation spec ±0.02%, and transient response is 20 μsec for 100% load steps. $50 (OEM qty). **Computer Products Inc**, South Boston, MA. (617) 464-6656. **Circle No. 318**

Regulators supply 7.5A at 3.3V with 600-mV dropout. The LDO family of 3-terminal regulators handles 1.5, 3, 5, and 7.5A. The regulators come in fixed (3-pin) and adjustable (5-pin) 3.3, 5, and 12V versions. Dropout voltage is 600 mA max. 3-pin models, $1.93 to $4.40 (100); 5-pin models, $2.14 to $5 (100). **Micrel Semiconductor**, San Jose, CA. (408) 944-0800. **Circle No. 319**

Interpoint's MIL-STD-883 dc-dc converters: Recognized for outstanding performance.

On Space Station Freedom, the Patriot Missile, European Fighter Aircraft and thousands of critical applications, Interpoint dc-dc converters are the ones designers choose first. However you measure performance, Interpoint commands the field.

HI-REL DC-DC Converters for Every Power Level

Series	V in	V out	Outputs	Power
MSA	16 to 40	5,12,15	1 or 2	5 W
MHF+	16 to 40	5,12,15	1 or 2	15 W
MTR	16 to 40	5,12,15	1, 2, or 3	30 W
MFL	16 to 40 80 to 160 160 to 400	5,12,15,28	1 or 2	65 W*
MFLHP	19 to 40	5,12,15	1 or 2	100 W*

** Multiple units current share*

Interpoint is recognized for broadest selection. From fully qualified SMD parts to low-cost solutions, from 5 to 285 watts. Interpoint has a solution for almost every power need.

Interpoint is recognized for innovation. Our 20-year history of breakthroughs includes the first 70 W/in^3 board-mountable dc-dc converters.

Interpoint is recognized for reliability. Our power supplies have logged more than 1,000,000 field hours per failure.

Our new, fully compliant MSA Series offers 5 watts of power in a case just 0.27" high. The MSA also meets MIL-STD-704A input voltages (up to 80V surges) with 5, 12, and 15 Vdc outputs.

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CIRCLE NO. 67

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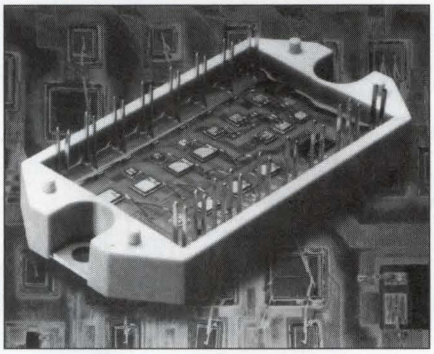
Manual volume control stifles Mallory Sonalerts. You can fit a manual volume control in the field to classic Mallory screw-neck Sonalerts. The control provides 14-dB attenuation of the Sonalert's ear-piercing, high-frequency shriek. Once you adjust the control, you can lock its setting in place. The control adds ¼ in. to the height of the Sonalert. $0.59 (100). **North American Capacitor Co**, Arlington Heights, IL. (708) 577-8505. **Circle No. 350**



Inverter stage integrates all power components for 1-hp motor drive. The MHPM7A15A60 hybrid power module integrates a 3-phase input rectifier bridge, a 3-phase output inverter, a brake transistor-diode, an optional current-sense resistor, and a temperature sensor on its insulated metal substrate (IMS). The 600V, 15A module drives 1-hp (750W) or smaller motors to bring intelligent motor control down to office equipment and household appliances. The output inverter uses matched IGBTs and free-wheel diodes. Other features include access to both positive and negative dc bus and a single-phase ac-input option. $50 (100). **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 244-3103. **Circle No. 351**

PIN diode switches 1 kW at low frequencies. Normally confined to very high frequencies, the UM2100 series of PIN diodes can switch 1 kW at frequencies as low as 500 kHz. The diodes' capacitance and series resistance are flat enough so that you can use the diodes as switching elements in the 2- to 30-MHz band. A forward bias of 50 mA max obtains an IP3 of 60 dBm at 300 kHz with 1W per tone. Voltage range of the devices is 0 to 1000V max. $18 to $46. **Microsemi Corp**, Watertown, MA. (617) 926-0404. **Circle No. 352**

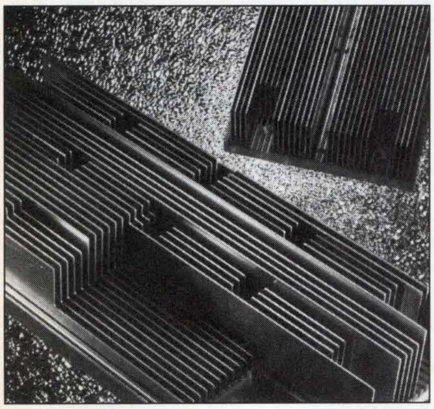
Gilbert Cell transistor-array IC suits double-balanced RF-mixer and amplifier applications up to 2.5 GHz. The HFA3101 Gilbert Cell transistor array replaces discrete, expensive GaAs ICs and is a pin-for-pin replacement for the NEC UPA101. The IC's f_T is 10 GHz, and collector-cutoff current, I_{CBO}, specs 10 nA. The device's gain-bandwidth product is 5 GHz, and its noise figure is 2.5 dB. Spice models and RF scattering parameters are available. $2.66 (1000). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7223. **Circle No. 353**

Liquid-cooled thermal planes suck heat out of closed chassis. Liquid-cooled thermal planes come in standard configurations for SEM or VME systems or as custom units. The thermal planes can be as thin as 0.070 in. Each side of the plane has a 0.09°C/W thermal resistance. The planes feature brazed cooling fins and a 150-psi working pressure. $500 to $1000, depending on design and volume. **Lytron Inc**, Woburn, MA. (617) 933-7300. **Circle No. 354**

Low-value, surface-mount chip resistors incorporate solid metal strips. The WSL series of low-value, surface-mount chip resistors have resistance values from 0.01 to 1Ω. These 2512-size units dissipate 1W max. Resistance tolerance is ±1%, and temperature coefficient is ±75 ppm/°C. $0.38 (10,000); delivery, six weeks. **Dale Electronics Inc**, Columbus, NE. (402) 563-6506. **Circle No. 355**

NTC thermistor-probe assemblies suit medical applications. A line of medical thermistor-probe assemblies include digital thermometers that feature tight tolerances over the medical temperature range of 32 to 43°C. Respiratory probes sense airflow through respirators; kidney-dialysis probes monitor blood flow through dialysis machines. Esophageal probes measure fluid flow in the body, and thermal-dilution probes go into heart catheters. Blood-flow-analysis probes suit intravenous use. $1 for disposable units, $5 for reusable units. **Fenwal Electronics Inc**, Milford, MA. (508) 478-6000. **Circle No. 356**

LED assemblies directly replace wedge-based incandescent lamps. An LED assembly consisting of a cluster of emitters, a lens, a protection diode, a limiting resistor, and a wedge-type base can directly replace common wedge-based incandescent lamps. The LED assemblies last 10 times longer than do the lamps they replace and consume 50% of the lamps' power. Versions of the assemblies accept power from 5 to 120V ac or dc, 50 to 400 Hz. Viewing angle is 160° (spherical). Eight colors are standard. A 28V-dc, red assembly costs $2.89 (1000). Samples are available. **Ledtronics Inc**, Torrance, CA. (310) 534-1505. **Circle No. 357**



Heat sinks's bonded fins remove heat two to three times faster than extruded fins do. The Series 4200 heat sinks feature cooling fins bonded to an aluminum heat spreader. This construction method permits 300% more cooling area than do extruding fins. The series comes in 24 variations of width and fin spacing. Widths range from 1.25 to 17 in. The highest fin count is 66 fins. A 2.4×2.4×2.5-in. heat sink having 16 bonded fins costs $10.20 (100); delivery is three to four weeks ARO. **Aavid Engineering Inc**, Laconia, NH. (603) 528-3400. **Circle No. 358**

Surface-mount coupler measures 0.31×0.31×0.2 in. The LRDC-10-1 broadband coupler's insertion loss measures 1 dB typ. Its directivity is 30 dB typ, and VSWR is 1.2 typ. The insertion loss has 4.5σ repeatability. Standard operating temperature range is –55 to +100°C. $15.95. **Mini-Circuits**, Brooklyn, NY. (718) 934-4500. **Circle No. 359**

Keyboard switches migrate into other applications. The FSM J series of pushbutton switches began life as "tactile" switches mass-produced for low-cost keyboards. But they are now available for other consumer application that require a positive feel from less than 0.02 in. of actuation travel. The switches use a silver-plated dome-shaped spring contact rated at 100,000 cycles/minute. $0.235 (5000). **Augat Inc**, Attleboro Falls, MA. (508) 699-7646. **Circle No. 360**

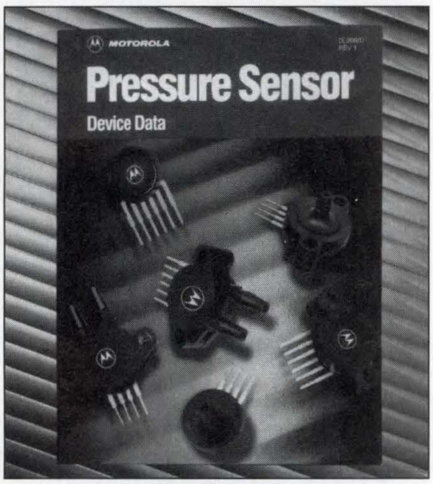
Curly plastic pigtail bundles cables. Kurly-tie brand cable wraps contract into a tight curl—somewhat smaller than a conventional phone cord—when not in use. Their inherent curl allows you to secure large or small cable bundles permanently during assembly or temporarily during test. The cable wraps come in 16 colors. The wraps are rubbery and do not slip. $1.49 to $12.95. Trial pack of all 16 colors, $8.50 (plus $2 shipping); sample, $1. **SuperVid Supply**, Stone Mountain, GA. (404) 413-8624. **Circle No. 361**

Tiny black-and-white TV camera comes on a single chip. The V-007's camera IC measures 0.55×0.42 in. A complete camera assembly in an aluminum case and bearing a 4-mm lens measures 1.37 in. square. The IC has a 312×287-pixel image-sensor array. Pixel size is 19.6×16 μm. Automatic exposure range is 40,000:1, and AGC is adjustable to –10 dB. The camera is sensitive into the infrared. A demo unit operates from a 9V battery and plugs directly into any type of monitor. $249. **Marshall Electronics Inc**, Culver City, CA. (310) 390-6608. **Circle No. 362**

Tiny surface-mount bead quashes EMI/RFI. The ICB-0603's inductance measures 120Ω at 100 MHz. The EMI/RFI-suppressing device measures 0.8×1.6 mm and carries 200 mA max. Devices come in 2000-item reels. $0.108 (100,000); delivery, eight weeks. **Associated Components Technology**, Garden Grove, CA. (714) 636-2645. **Circle No. 363**

LITERATURE

Handbook on compliance labeling. *The Essential, No Nonsense Guide to Compliance Labeling: Compliance Labeling for the Electronics and Telecommunications Industries* explains how to install label printing systems to meet industry-specific or customer-mandated bar-code label specifications. This 14-pg pamphlet discusses why labeling standards are necessary and how you design and implement a successful labeling program. **Zebra Technologies Corp,** Vernon Hills, IL. **Circle No. 394**



Data book details silicon pressure sensors. The *Pressure sensor device data book* offers extensive information on Motorola's integrated µP-compatible pressure sensors. The book covers specifications for individual devices, descriptions of interface circuitry, package outline drawings, and information for handling and mounting the devices. **Motorola Inc,** Phoenix, AZ. **Circle No. 395**

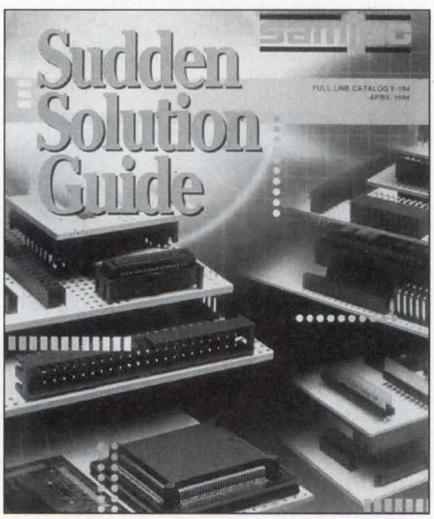
Data on cables. A 4-color, 2-pg data sheet features the Super CAT line of cables, which is designed for higher-performance systems such as ATM. **Helix/HiTemp Cables Inc,** Franklin, MA. **Circle No. 396**

Supplier directory for the fiber-optics industry. The *Worldwide Fiberoptic Suppliers Directory for 1994-1995* lists companies, products, and contacts for the fiber-optics industry. The directory also lists more than 1300 suppliers in over 36 countries and includes contacts and products manufactured. $60 plus $5 if shipped outside the US. **KMI Corp,** Newport, RI. **Circle No. 397**

Paper addresses dangers in electronic equipment. *Powerline Disturbances and Electronic Systems* presents an analysis of powerline disturbances and describes unexpected dangers to electronic equipment that conventional surge-control devices can't handle. **Zero Surge Inc,** Frenchtown, NJ. **Circle No. 398**

Free Spice newsletter. *Intusoft Newsletter* covers topics related to the Spice circuit-simulation program. The newsletter includes regular features, such as the Intusoft Modeling Corner, a column about Spice modeling. **Intusoft** San Pedro, CA. **Circle No. 399**

Book explains obstacles of circuit simulation. *Inside SPICE: Overcoming the Obstacles of Circuit Simulation* demonstrates how to get accurate, high-quality simulation results by learning to overcome common causes of error and simulation failures. The 208-pg book addresses the problems that engineers most commonly encounter while using Spice or any Spice-like simulator program. Topics covered include: the stumbling blocks of nonconvergence, numeric integration instabilities, and time-step control errors. $50. **RCG Research Inc,** Indianapolis, IN. **Circle No. 400**



Catalog of connectors. Catalog F-194 details 0.100-in.-pitch board-to-board interconnects, micro and surface-mount connectors, IC-to-board sockets and adapters, and IDC cable assemblies. An applications section gives information on the design of sockets and adapters for advanced IC packages. **Samtec Inc,** New Albany, IN. **Circle No. 401**

Catalog describes switching power supplies and converters. In 64 pgs, this catalog covers ac/dc switching power supplies from 15 to 650W and dc/dc converters from 1 to 650W. New products include surface-mount, wide-input-range, and high-isolation dc/dc converters. The catalog also contains detailed specifications, features, and performance graphs. **International Power Sources Inc,** Ashland, MA. **Circle No. 402**

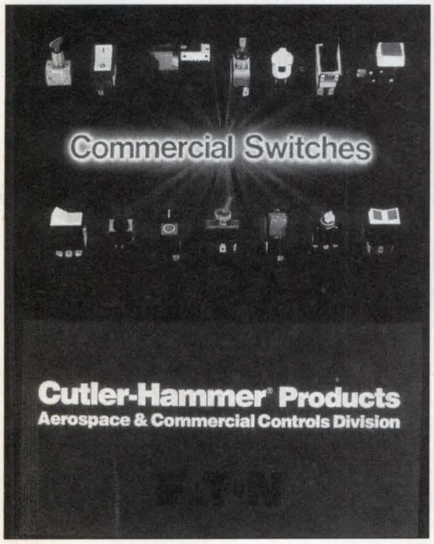
Paper describes voice-over-data technologies. This 5-pg paper details the features of the MultiModem PCS, including the voice-and-data mode that enables you to talk to the person on the other end of the modem link when sending data. The paper also compares the various voice-over-data technologies on the market. **Multi-Tech Systems Inc,** Mounds View, MN. **Circle No. 403**

Guide to selectors. The *RF Selector Guide and Cross Reference for 1994* outlines RF product offerings and incorporates new categories such as RF integrated circuits. The guide also includes package outline information and a listing of application literature. **Motorola,** Phoenix, AZ. **Circle No. 404**

Brochure describes stainless-steel enclosures. This brochure and selection guide assist enclosure specifiers

LITERATURE

who require stainless steel for their applications. The brochure explains new programs designed to cut lead times for modified enclosures. **Hoffman Engineering Co,** Anoka, MN.
Circle No. 405



Commercial switches catalog. Catalog No. NC-168 details switches for commercial and industrial applications. Each product section includes a brief description and a selection table to simplify the search and selection process. **Eaton Corp,** Milwaukee, WI.
Circle No. 406

Brochure features datacomm/telecomm products. This free brochure describes cabinet racks, open relay racks, and a broad selection of compatible accessories for the datacomm/telecomm markets. **Bud Industries Inc,** Willoughby, OH
Circle No. 407

Catalog features membrane switches for custom applications. This 4-color, 8-pg catalog contains photos, features, mounting dimensions, technical information, specifications, options, and components of membrane switching systems for custom applications. **EAO Switch Corp,** Milford, CT.
Circle No. 408

List of CD-ROM programs. This 2-pg sheet describes the various CD-ROMs available from PC-SIG. The list includes the *PC-SIG Library CD-ROM, 13th ed,* which contains thousands of fully functional shareware programs as well as spreadsheets, databases, word processors, and graphics programs. *The PC-SIG World of Windows CD-ROM* contains over 350 of the best Windows shareware programs available. **PC-SIG,** Sunnyvale, CA. **Circle No. 409**

Catalog details family of plug-in integrated switching regulators. Providing specifications, photos, and schematics on each power module, this 32-pg catalog covers a line of integrated switching regulators and converters. A section on product operation, applications, and special considerations is also included. **Power Trends,** Batavia, IL. **Circle No. 410**

Specs on RF and microwave components. This 93-pg catalog incorporates detailed specifications and outline drawings on a variety of passive components in the dc to 18-GHz frequency range. Commercial, industrial, and military components such as fixed and tunable filters, attenuators, switches, and switching and control subsystems are also covered. **Trilithic,** Indianapolis, IN. **Circle No. 411**

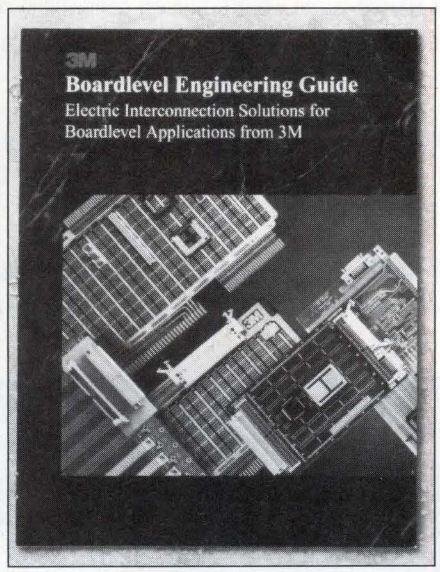
Hardware and Windows packages covered in handbook. This free 320-pg catalog highlights lines of data-acquisition and imaging products and programming tools. It details the DT VEE visual-programming language for data acquisition; the Global Lab Image family of imaging software tools; VB-EZ data-acquisition and high-speed plotting custom controls for Visual Basic; DataAcq-EZ and Vision-EZ low-cost data-acquisition and imaging packages; and the Fidelity series of high-accuracy frame grabbers. The handbook provides technical tutorials and examples of products to use as aids in choosing a product. **Data Translation,** Marlboro, MA. **Circle No. 412**

Features of fiber-optic connectors and adapters. This 132-pg catalog describes a line of fiber-optic connectors and adapters in addition to cable assemblies, termination tooling, fiber-optic switches, and premise-wiring products. It also provides a glossary and a section describing connector-termination procedures and the tooling required. **Molex Inc,** Lisle, IL.
Circle No. 413

Catalog details EMI/RFI services and products. "Solving Fabrication Problems" is a 100-pg catalog providing technical data materials from suppliers of electrical insulation, pressure-sensitive tapes, gasket materials, and EMI/RFI shielding. **Fabrico Div, Electrical Insulation Suppliers Inc,** Atlanta, GA. **Circle No. 414**

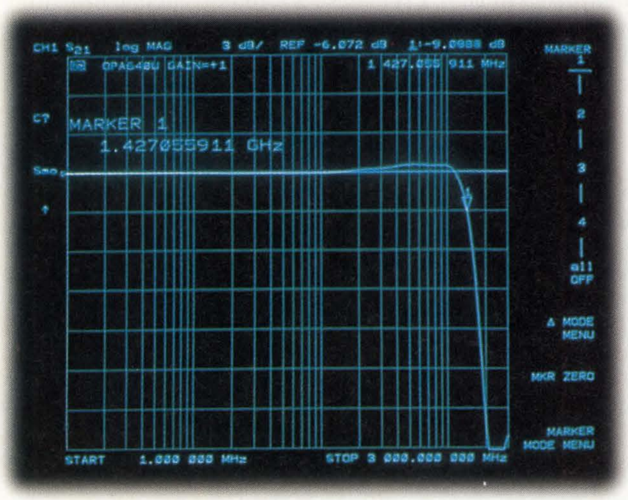
Hardware catalog. A 200-pg catalog describes a line of electronic hardware and includes specifications for circuit-board spacers, captive panel screws and retainers, standoffs, chassis and cabinet handles, shoulder screws, and many other items. **RAF Electronic Hardware,** Seymour, CT. **Circle No. 415**

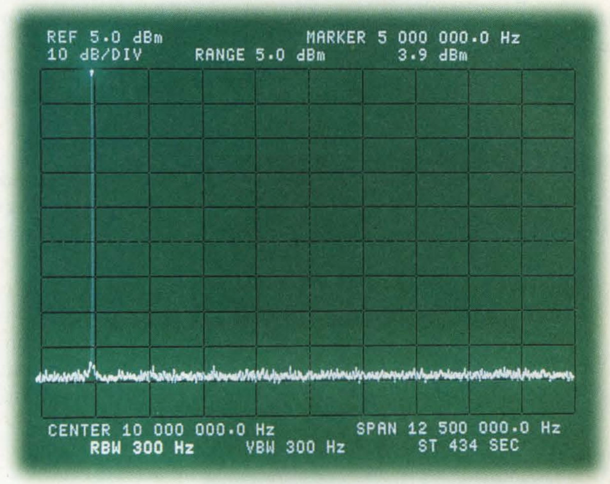
Application selector guide for wire-tacking adhesives. This guide highlights an extensive line of high-performance adhesive compounds for tacking wires and attaching components to printed wiring boards. **Master Bond Inc,** Hackensack, NJ. **Circle No. 416**



Guide available for interconnect products. This 8-pg brochure helps designers select the appropriate board-level interconnect product for I/O board stacking, IC socketing, and board-to-backplane applications. It includes photographs and specs on a line of sockets, headers, and high-density stacking connectors. Tables help you match the header and socket based on board-spacing requirements, pin or lead counts, contact quantities, and pitch. **3M** Austin, TX. **Circle No. 417**

SpeedPLUS Op Amps...
More Than High Speed!





Six wideband op amps give you the speed you'll need for tomorrow's faster designs, *PLUS* key specs to optimize your most demanding applications. Our new ***SpeedPlus*** op amps make your future faster.

FREE SAMPLES! Speed into the future...now! For a few samples, call **1-800-548-6132**. And, ask for a free copy of our *Operational Amplifiers* guide. Or, contact your local sales representative for immediate assistance.

OPA640 is the world's highest bandwidth op amp. Its speed and dynamic performance make it your best choice for critical communications and test equipment applications.

OPA641 is stable in gains of two or greater and features a fully symmetrical differential input and fast 12-bit settling. Try it for RF and imaging designs.

OPA642 gives you high speed with very low distortion and noise, the right combination for high resolution imaging and preamp applications.

OPA643 is stable in gains of five or greater and delivers high slew rate and low noise. It's purely perfect for all preamp applications.

OPA644's current feedback design gives you very high open loop transimpedance with high slew rate and superior differential gain/phase performance.

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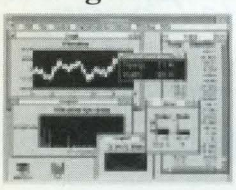

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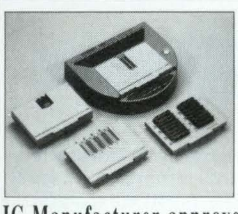

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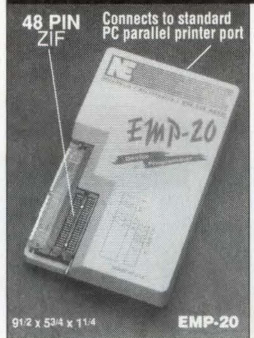

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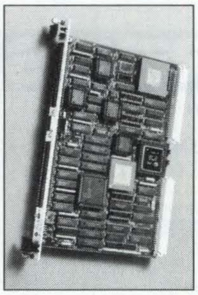

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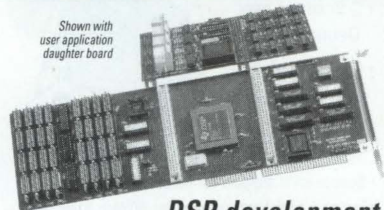

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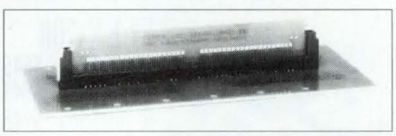

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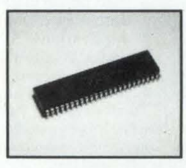

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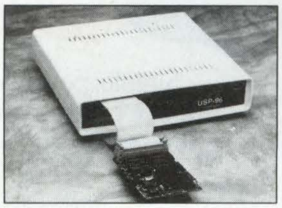

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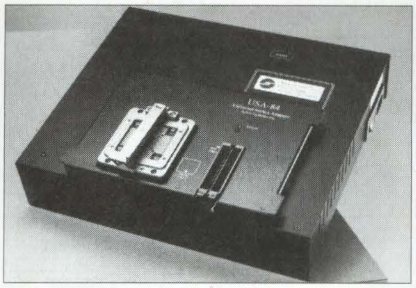

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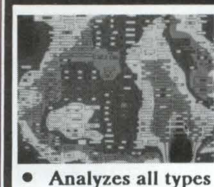

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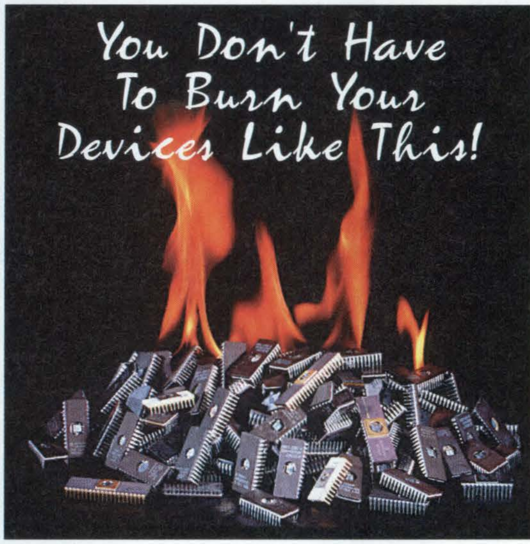

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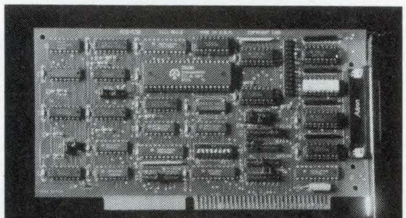

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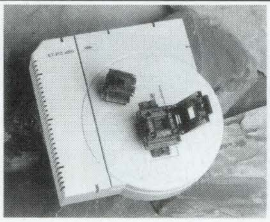

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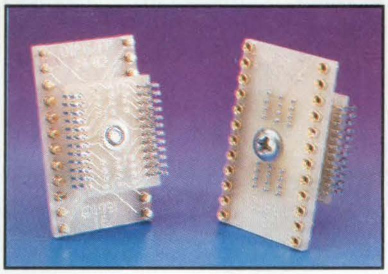

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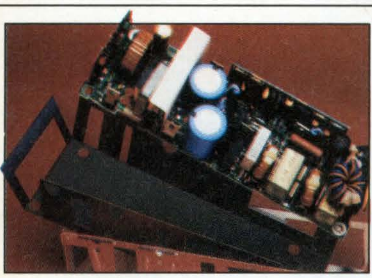

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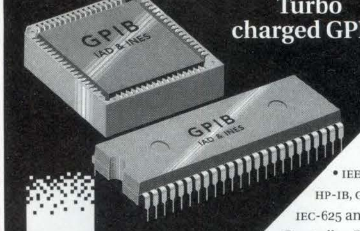

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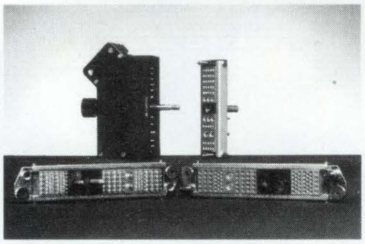

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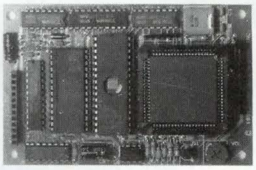

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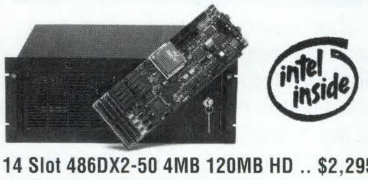

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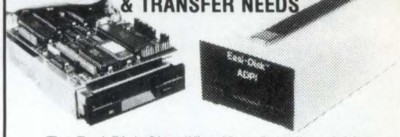

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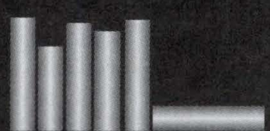
User-interface design book tells all

The response to my article on prototyping user interfaces (**Ref 1**) shows that a great many *EDN* readers really care about how users interact with their products. As a visit to a suitable technical library will quickly reveal, there is much you can read about human-factors engineering and interaction between people and computers. These subjects are controversial, too, so no single book or article provides a comprehensive view of the field. That said, if your human-factors library allows room for only one volume, you should seriously consider making it *Developing User Interfaces* by Deborah Hix and H Rex Hartson (ISBN 0-471-57813-4), a 391-pg trade paperback priced at $34.95.

If your library allows room for only one book on user interfaces, buy this one.



For the most part, this eminently readable book succeeds in remaining objective. It covers such topics as styles of interaction and the iterative process of developing, evaluating, and refining a user interface. Each chapter provides a reference list. Most chapters also include exercises for the reader and possible solutions. The chapter on development tools avoids presenting a long list of products; it focuses instead on how to evaluate and select tools. Considering how rapidly new and revised tools emerge and that books continue to be available for long periods, this approach is probably the only sensible one.

I did find several chapters to be downright depressing, though. These are the ones on user-action notation (UAN). As an alternative to using vague and verbose prose to describe the operation of user interfaces, especially graphical ones, the authors offer us the UAN shorthand. As an example, in UAN the tilde (~) character denotes a mouse movement. Being able to communicate easily how a graphical interface works has undeniable advantages, and using text-based notation to convey such information unambiguously seems like a good idea—at first. But a few minutes of reading about UAN made me wonder whether a problem so complex might be too tricky to even try solving.

Yes, it's worth knowing whether a function name will be highlighted as soon as I push down on a mouse button or whether the highlighting won't come on until I lift my finger off the button. And, yes, a text-based description of the interface operation might fail to differentiate between the two conditions. Nevertheless, I can't help thinking that the authors' cure is worse than the disease.

My feelings of frustration were heightened when I realized that the notation, which is supposedly based on the ubiquitous ASCII character set, uses several unique non-ASCII characters—an upside-down capital A and a double solid line that ends in arrows—in addition to superscripts and subscripts. These special characters make it impossible to use a standard text printer to reproduce UAN files. Moreover, if human-factors specialists can devise such an arcane and inscrutable notation, you have to wonder whether they believe that human factors are important to everybody *except* people who do human-factors work.

Nevertheless, the book is comprehensive, and most of it is informative and useful. It should prove worthwhile to any engineer seriously interested in creating products that real people can use. No book is perfect, and the UAN chapters should not deter you from purchasing this one.—**Dan Strassberg**

John Wiley & Sons Inc, New York, NY. (908) 469-4400. **Circle No. 469**

Reference

1. Strassberg, Dan, "User-interface prototypes help you design products real people can operate," *EDN*, March 3, 1994, pg 51.

New version improves CubiCalc's fuzzy-development features

Late last year, HyperLogic released CubiCalc Version 2.0, although I had been working with a beta version since midsummer. I reviewed CubiCalc 1.2 in the March/April 1992 issue of *PCAI* and expanded on that review in the March 1992 issue of the *Huntington Technical Brief.* This article discusses only version 2.0 features and only those I consider to be key to how I use fuzzy logic.

The addition for which I am most grateful is the support of matrices. The matrices are currently constrained to three dimensions with a maximum dimension size of 4000. The program provides a collection of operations, including matrix addition, subtraction, copying, inversion, transposition, and scaling, as well as diagonal-matrix initialization and several more that are a bit esoteric. The on-line help and readme file document all these matrices, although the current manual does not.

HyperLogic also has continued to strengthen the expression language, which processes data applied to and received from the rule base and simulates a controlled system in a feedback simulation. In some ways, the expression language is looking increasingly C-like. For example, the new version adds the C short-form operations +=, –=, *=, and /=. The software also now supports looping, using *while* as the keyword, and it supports random access to binary input files (with data in IEEE-standard, floating-point, 32- or 64-bit format).

HyperLogic has also improved the setting of fuzzy-variable values and added a terse-rule syntax for rules with antecedents connected with AND operators. For example, you can represent the rule with a traditional syntax

```
if E_X is SM_POS and
    DELTA_X is LRG_NEG then
    DRIVE is MED_POS;
```

as:

```
E_X SM_POS, DELTA_X LRG_NEG:
    DRIVE MED_POS;
```

The software supports multiple rule consequences; one rule can now specify actions for more than one output. CubiCalc includes two new fuzzy-related functions. **active_rules(...)** and **membership(...).active_rules** return the number of rules governing a specified output function that has fired.

The **membership** function is more interesting to me. It is called in the form:

```
var = membership(
    variable_name,
    adjective_name,
    crisp_input);
```

Given a fuzzy variable **variable_name**, one of its adjectives **adjective_name**, and a crisp-input value **crisp_input** returns the degree to which **adjective_name** contains **crisp_input**. You can use this feature, for example, to perform specialized fuzzy inference not using the provided defuzzification, as when combining the strengths of rule firings using a weighted average.

Version 2.0 also provides several new inference methods (and I am glad to see that the documentation separates combination and defuzzification of operations). As in earlier versions, you can choose between "scale via product" (often called "max-dot") and "scale via maximum" (often called "max-min"). In addition, you can now combine data via maximum or via sum. Both are forms of output-function combinations: The maximum method creates a resultant function by taking the pointwise maximum value of the functions being combined, and the sum method takes the pointwise sum.

The software also allows for a consequence indicated by multiple rule triggers to be counted only once or the number of times it was triggered. Two defuzzification options, centroid and maximum, are available, and the manual provides a good discussion of all inference methods.

HyperLogic has also provided three new plots: activation, resultant, and decision surface. The activation plot shows the degree to which each of the adjectives for a given variable is active. The resultant plot shows the output fuzzy-set waveform with a marker indicating the defuzzified output. The decision-surface plot is the only one that CubiCalc does not generate at runtime. It plots three variables in an X, Y, Z coordinate system. Although, typically, these variables are fuzzy, X and Y are inputs, and Z is an output, CubiCalc does not require this restriction: Any of the three can be fuzzy or crisp and can be inputs, outputs, or internal variables. To control viewing angle, the decision-surface window has three graphic thumbwheels to rotate the plot about the three possible axes. An optional but valuable feature of the decision-surface plot is the display of orthogonal slices at a specified coordinate pair through the X and Y input spaces.

The software also provides for color plots, making it easier to distinguish between the traces in the x-y scatter plot, available in this and earlier versions. In addition, this version supports execution tracing. Running a simulation with tracing enabled causes the status bar to show the phase and line number of each instruction as it executes. Further, if the editor window containing the currently executing expression is open, CubiCalc highlights each executable line as it is processed.

I am also grateful for CubiCalc's adherence to the part of the Windows specification that designates Ctrl-x, Ctrl-c, and Ctrl-v for Cut, Copy, and Paste, respectively. This feature facilitates projects with a lot of cuts and pastes and makes the keyboard version of these operations both more convenient and more Macintosh-like.

The runtime-compile (RTC) option continues to be available in Version 2.0. RTC allows you to compile a designed fuzzy system as a number of library functions that you can then link with Borland or Microsoft C for execution on a PC. The RTC fuzzy engine is also available as C source code that you can compile for non-PC targets.

Given all these improvements to CubiCalc, I list the following not as shortcomings of the current version (as I did the lack of matrices in Version 1.2), but as improvements worthy of a next generation.

First, the terse-command entry is an improvement, but I would also like to see a graphical-matrix-rule entry and presentation.

Second, I would like to see HyperLogic continue to strengthen CubiCalc's expression language, including the addition of user-generated functions and a textual in-line means of declaring variables, especially nonfuzzy variables.

Third, I would also very much like to see CubiCalc treat the characteristics of fuzzy values (CubiCalc's "adjectives") as variables available to the expression language, thus allowing such functional control as shifting, scaling, and hedging. Such capability is necessary in the design of adaptive and self-organizing systems, of which we shall see an increasing number.

Fourth, I would enjoy seeing CubiCalc support Sugeno inference, which replaces output fuzzy sets with functions of inputs.

A final "would-be-nice" feature is the ability to have multiple rule bases defined within a single simulation. CubiCalc can currently do this with multiple instantiations communicating through Windows, but a self-contained solution is preferable.

But, in general, Version 2.0 is a positive and significant refinement of an already-good fuzzy-simulation tool. It is apparent that HyperLogic developers put much thought into which features to add. The tool is easy to use and has considerable power. I often "throw together" a simulation on CubiCalc just to test the concept and feasibility of a new system.

In most ways, I consider CubiCalc to be not merely a contender but the front-runner in the fuzzy-development-tool market. It is also satisfying to know that while other fuzzy-tool vendors are struggling, HyperLogic remains strong.

CubiCalc runs under Windows 3.1. Its base price is $495 and $795 with the RTC option. Source code for the RTC engine is $995.

Bottom line: This is an excellent fuzzy-development tool—the one I most often use and recommend.—**David I Brubaker**

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David I Brubaker is president of Huntington Advanced Technology (Menlo Park, CA) and a frequent contributor to EDN.

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Whoa!

The Verilog / VHDL wars are ending!

Toward the end of the movie "The Wizard of Oz," a scene shows Dorothy finally getting to meet what she believes is the Wizard of Oz. What she sees is an incredibly large human head floating between two columns of fire and smoke. As she meekly converses with this angry apparition, her dog, Toto, manages to expose a man standing behind a nearby curtain. The man appears to be operating some sort of control room. When Dorothy notices this man, he tells her, "Pay no attention to that man behind the curtain!"

Real-life elements similar to Dorothy's experience dramatically unfolded at the Open Verilog International '94 (OVI) conference in March. Among all the usual technical discussions—such as what to include in the IEEE 1364 push, EDA-vendor announcements (such as that Cadence had just sold its 10,000th copy of Verilog-XL), and the hubbub of a very busy exhibit hall with lots of curious customers—a watershed event in the ASIC/EDA/field-programmable gate-array industry was taking place.

It was neither the fact that this year's OVI had 35 exhibitors compared with last year's 24 nor the fact that this year's OVI had 493 attendees compared with last year's 390; it was what was happening behind the scenes that was of real interest.

The hot gossip at OVI was that two EDA companies, Synopsys and ViewLogic, which had until the conference been very adamant—almost militant—VHDL proponents, were in a bidding war for Chronologics, a company that specializes in high-speed Verilog simulation. When asked about the rumor, all three EDA vendors gave the usual reply: "Pay no attention to that man behind the curtain!"

To muddy the waters further, in the middle of the "8 CEOs and Two Other Bigwigs" panel (on how many ways one can use the word "paradigm" in a sleepy discussion on 1-million-gate ASICs), Alain Hanover, CEO of ViewLogic, quoted "purchased" market research indicating that VHDL would soon kick Verilog's derrière. (ViewLogic eventually won the bidding war for Chronologics. When asked later why he quoted such "statistics" in the middle of a Verilog conference, Hanover said, "We knew that the rumor had gotten out, but we didn't want to tip our hand.")

Why is this such a watershed event? Big companies buy little companies all the time, you say. But it's not which company won the bid for Chronologics that's important; it's which companies were doing the bidding. What their actions signify is that the disastrous Verilog/VHDL wars are ending! The additional fact that Mentor dropped a pretty piece of change buying a pricey lunch for all the OVI attendees and was quite active in the technical forum also backs this assertion. The ever-demure CEO of Cadence, Joe Costello, says of this development, "Hell, we thought it was a bankrupt strategy to take sides in the Verilog/VHDL wars five years ago. Sell the customer the HDL [hardware-description language] he asks for, and you have a happy customer. Force him to go to an HDL he doesn't want, and you get an unhappy customer."

In this case, Costello couldn't have said it better. Now that ViewLogic has joined the "language-neutral" club by offering *both* Verilog and VHDL, it's only a matter of time before Synopsys and Mentor do the same.

John Cooley, an EDA consumer advocate and founder of the outlaw E-mail Synopsys Users Group (ESNUG), lives on the Holliston Poor Farm in Massachusetts. He raises sheep and is an EDA- and ASIC-design instructor and project-in-crisis consultant. He can be reached at "jcooley@world.std.com" or at (508) 429-4357.

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