Vintage machine produces memories

The Jacquard loom, dating from 1804, can be used to assemble modern read-only braid memories; the simplicity and low cost of the method widens the field of possible applications for the transformer stores

By Ramon L. Alonso

Instrumentation Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

Space-age read-only memories can be built with a machine rooted in the 18th Century and perfected in the early 19th Century. The technique promises to be substantially cheaper to use than conventional methods, both in the wiring of the memory itself and in the simpler circuits that can be used with it. The low cost, in turn, makes these memories much more attractive in many applications, and suggests some new uses for read-only memories.

The machine is a Jacquard loom, one of the first devices designed to be controlled by a punched card. The loom has been modified to control the placement of wires in a braid to make a braid memory—a kind of transformer read-only memory. The technique, developed at the Instrumentation Laboratory of the Massachusetts Institute of Technology, has been used to build a number of different feasibility models,[1, 2] and most recently to build a complete, self-contained memory containing about half a million bits in the form of 32,768 sixteen-bit words. The memory has only 256 U-shaped cores; it stores data by routing 2,048 wires through or around the cores.

Two cents a bit

Compared to standard memories, the braid unit's electronics are simpler, requiring monopolar currents rather than bipolar; furthermore, braid word-line currents, at 140 milliamperes, are about a third the 400-to-600-ma. currents needed for conventional core memories. Versions that use only one-tenth as much current are quite feasible. Sensing is also simpler in braid memories, but integrated sense amplifiers for core memories diminish the importance of this advantage.

Most of the cost of conventional core memories lies in the cores themselves, the plane threading, and the number of diodes. On these counts, wired memories should be one-third to one-tenth the cost of conventional read-write units. One report[2] estimated that the electronics of a braid system could be sold at about 2 cents per bit, and the braid itself replaced at about 0.6 cent per bit. These estimates, though speculative, do indicate market potential.

Wired memories are attractive wherever a large body of data isn't changed often and where random access is required. An interesting question here is the relative price at which additional memory in braid-like form would be more attractive than core for a commercial computer. If an installation has millions of words of operational programs, a large portion could reasonably be left unchanged. In a time-sharing environment, well-established programs should definitely be available on a random-access basis to avoid time-consuming swaps between core and drum, disk and tape. Balanced against this is the fact that, should a change be required, a whole braid might have to be replaced. A possible solution would be to combine an associative memory with the braid to detect the addressing of an obsolete location and provide the correct contents.

Wired memories are clearly desirable in control computers. There permanence is a virtue, especially if the computer operates unattended or isolated.

The author

Ramon L. Alonso, a native of Buenos Aires, is an assistant director of MIT's Instrumentation Laboratory, where he has worked since 1957. He is also a lecturer in the Department of Aeronautics and Astronautics at MIT. His present interests are multiprocessor organization and logic-circuit simulation.

In certain specialty devices, such as cathode-ray displays or tables for fast table-lookup operation of a control device, the wired memory has a strong appeal.

Wired-in data

A transformer memory is a fixed, read-only memory in which information is stored as a wiring pattern that is not electrically alterable. It offers high density, random access, permanent storage, and low power consumption, all of which make it attractive in special applications. One such unit is used, for example, as the program memory for the Apollo guidance computer;[3] others are being used as code converters in commercial printers and as instruction-interpreting sequence generators in some commercial computers.

In one transformer memory design, each wire either threads or does not thread a series of toroids; in another design, each wire passes either to the right or the left of each post in a series of posts. Information is permanently stored according to the routing of the wires, a fundamentally simple system.

The diagram at top right depicts three cores threaded by four wires. In symbolic form, the presence of a slash mark indicates a wire passing through the core, and the angle of the slash shows the direction of the wire. This convention is followed in other diagrams in this article.

Transformer memories can be arranged in two forms; conceptually, one form can be switched to the other by an interchange of cores and wires. The braid memory is arranged in the "word-per-line" form—each word is represented by a single wire, carrying a current pulse, that threads through certain toroidal cores and bypasses others. One sense wire is threaded through each core, and a voltage pulse is generated in the sense wire when any word wire through that core is pulsed. The memory basically contains as many cores as there are bits in each word. Early versions of these memories resembled braids, hence their name.

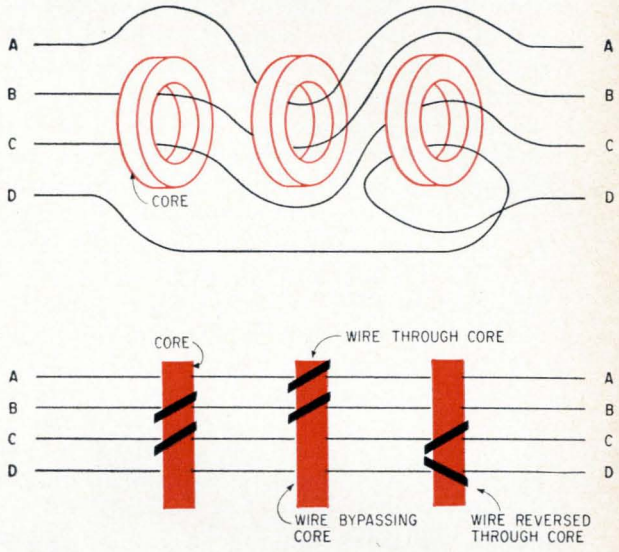
Although the word-per-line form of memory organization dates back more than 16 years,[4] interest in it has been revived recently in the context of transformer memories.[5, 6, 7]

The wires for a braid memory can be preformed into a harness that is laid over a set of U-shaped cores. The magnetic path is then completed through ferrite bars laid across the tops of the U's. Both the U-cores and the bars, which make up split cores, should be made of magnetically linear material for which the hysteresis loop is narrow and in which the degree of magnetization is nearly proportional to the magnetizing current.

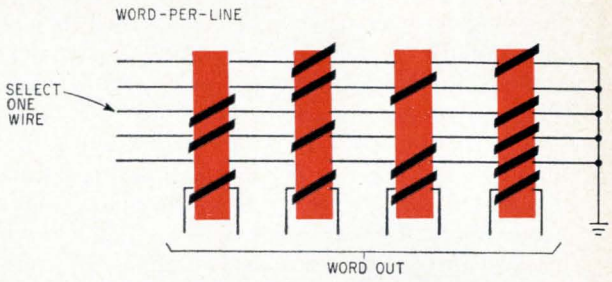
No loom for a rope

In the other form of transformer memory, the word-per-core, a single toroidal core made of magnetically nonlinear material for which the hysteresis loop is nearly square, is made to switch its direction of magnetization by a current pulse on a word wire threaded through it. Its switching generates pulses in sense wires that thread it, but not in those wires that bypass it. The memory in its basic form contains a separate core for each word and as many wires as there are bits in each word. This form is often called a "rope" memory because of the physical appearance of early versions.[8] Ropes have a long history of applications

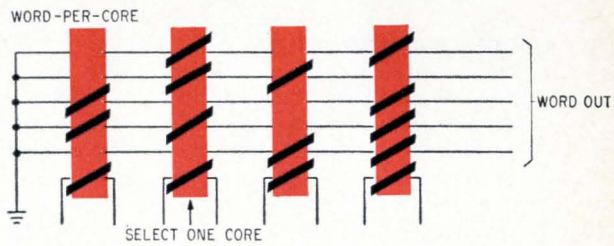
Transformers, ropes and braids



Transformer memory contains, in most cases, a series of cores plus wires that either thread or do not thread each core. In the symbolic diagram at the bottom, a slash mark indicates both the presence and the direction of a wire passing through a core.



Word-per-line organization is basis of braid memory. The wires making up the braid are word lines. They couple a signal to sense lines by way of the cores.



Word-per-core organization is basis of rope memory. The wires making up the rope are sense wires on which a word appears when a single core is switched.

as memories,[9] code converters,[10] and decoders.[11]

Rope memories cannot be made with looms or similar machines; for reasons related to the nature of the square-loop ferrite material of which the cores are made, the wires must be individually threaded through the cores, without first being woven into harnesses.

All the cores except one are kept below their switching threshold by a set of inhibiting currents. This permits a single common drive current passing through all the cores to switch only the selected core. The core's square-loop properties are instilled by annealing the previously shaped core at 1,100° to 1,400°C, a temperature range high enough to melt copper wire. The core can't tolerate an air gap, nor can it be assembled from semicircular pieces after annealing, as either would produce a reluctance much higher than that of a single continuous piece of material, causing the loss of nonlinearity. The wires must be individually threaded.

Because braid memories can be made with linear material, the cores can tolerate an air gap or a discontinuity where the U-core and the crosspiece meet. Indeed, some versions of braid memories don't have closed flux paths at all; they rely on a straight ferrite rod inserted in the holes in the harness.[5, 6]

Another advantage of braids over ropes is that the single sense winding on each core in a braid unit can be multiturn, generating a signal large enough to drive transistor logic circuits directly. This advantage is partly offset by the fact that more circuits are required to select one out of N lines ($2\sqrt{N}$ switches driving a diode matrix) than one of N cores ($2 \log_2 N$ inhibit lines plus one drive line). For example, if $N = 256$, the diode matrix must be driven by 32 switches, but only 16 inhibit lines plus a drive line are required for the rope form.

Various proposals for forming the wire harness call for an x-y table to control the routing, or for ladder-like conductive patterns deposited on plastic films.[6, 7] The latter approach was considered at the beginning of MIT's braid memory project, but discarded for reasons of cost and density. The cost was estimated to be close to 20 cents per bit, considerably more expensive than the loom technique; the plated-through holes accounted for the extra expense. Furthermore, the density appeared to be limited to about 625 bits per cubic inch. It is, however, a perfectly sound and rational approach that could very well become preferable when the manufacturing techniques improve. If the thickness of the laminates, including insulation between layers and air space, can be dropped below 10 mils, the density would be about 2,500 bits per cubic inch, which begins to look attractive. Because the loom technique can use wires less than 3 mils in diameter, its potential density is 10,000 to 20,000 bits per cubic inch. At present, the braid density is approximately 5,000 bits per cubic inch.

Weaving a memory

The technique developed at MIT involves a modified Jacquard loom[1] similar to the machines used for weaving complex patterns into fabrics for figured neckties or upholstery. The loom separates all the wires at once into two groups: ones and zeroes. [See "Looms and computers," below]. A temporary separator preserves the grouping at each step in the manufacturing process, and permanent separation is later achieved by lacing or encapsulation.

The loom is controlled in textile weaving by a punched card; the holes determine whether a particular thread is raised or not. A large number of these cards (which are large cardboard patterns, not the familiar paperboard cards used in

Looms and computers

Looms are probably the first devices to make use of the punched card. The earliest such application dates back to about 1736, when Jacques de Vaucanson used a form of punched card to determine which threads were to remain above and which below the shuttle. Vaucanson later became famous for making various automata, in particular a mechanical duck that performed so well that it became renowned throughout Europe; he also made a mechanical flutist that could play 12 different tunes.

Joseph-Marie Charles Jacquard perfected the card-controlled loom in 1804; it was an instant success, with thousands in operation in a few years. The Jacquard loom hasn't changed appreciably since then.[12]

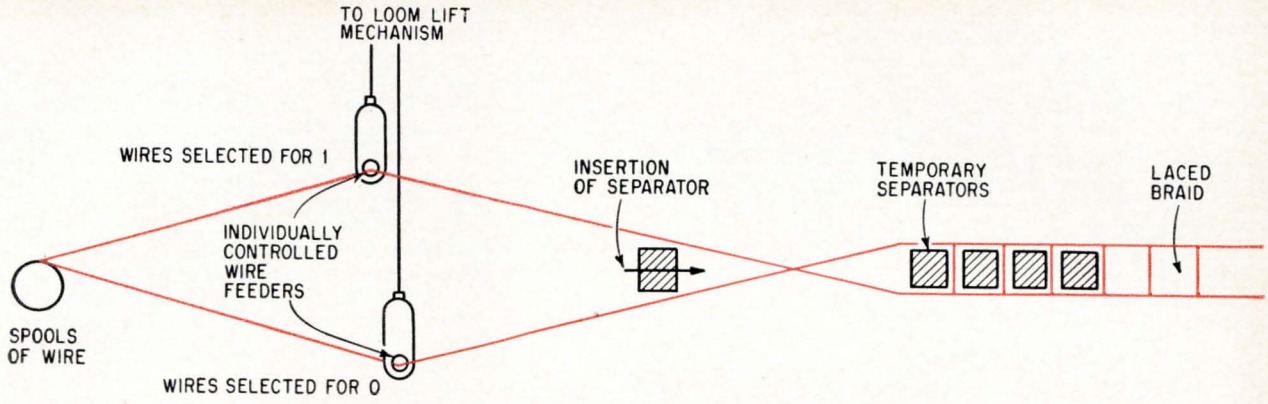
When weaving cloth, the simple loom lifts some threads above a shuttle plane, leaving others below it. A shuttle then carries a thread between the upper and lower threads. When the threads are reversed relative to the shuttle plane, the shuttle returns.

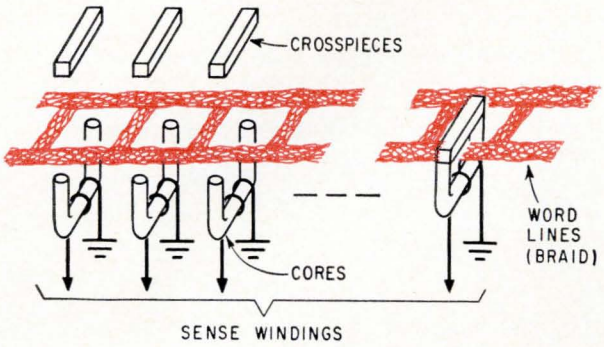
The Jacquard loom permits a completely arbitrary choice of which threads are to be placed above or below the shuttle plane at each step, with the punched card controlling the choice. The absence of a hole causes the push-rod to push the hook (see diagram, p. 92); the hole causes the push rod to remain stationary as the block moves forward. Jacquard cards have about 1,300 hole positions.

The loom lift mechanism MIT is now using isn't substantially different from either the Jacquard or the Vaucanson looms. However, the punched card has been replaced at MIT by a more versatile electrically alterable equivalent.

Braid memory characteristics

Capacity	32,768 words
Word length	16 bits
Cycle time	2 μsec
Access time	1 μsec
Power	10 watts
Input	16-bit address
Output	16-bit word
Number of cores	256
Number of word lines	2,048
Dimensions	11¼ x 12⅞ x 1⅞ in.





Wires are individually separated into ones and zeroes by the loom lift mechanism. This produces a ladder-like harness the shape of which is maintained by temporary separators until the braid is completely assembled and encapsulated. U-shaped cores are then placed in the openings in the harness and capped with ferrite cross-pieces. Addressing and sensing electronic circuits complete the memory assembly.

computers) are connected edge to edge to make a wide belt. The belt is advanced one card at a time for each step in the weaving process.

At MIT, the belt of punched cards has been replaced by a system of free pins and slides controlled by a punched paper tape [see diagrams and photographs on pages 92-96].

To make a braid, 256 wires are threaded through the loom and each one is connected to a separate diode card. During this stage, the loom selects the wires one at a time to identify them. After all the diode connections are made, the loom establishes the separation of ones and zeroes for each bit position. After one braid has been made, the wires are again selected in groups of 16 for termination at the other end. Eight braids make up a single memory, and the entire assembly is encapsulated after all are in place. After the encapsulating process, the temporary separators are replaced by the U-cores.

For each 256-strand braid, the terminations currently take about two hours and the weaving action, or separation, about one hour.

Switches that sense the separation made by the loom feed back this information to the paper-tape reader, where it is compared with the original separation instructions. If an error is detected, the controller tries again, up to four times. Such an error could be caused by a blockage in one of the air lines, a stuck slide or pin in the tape-controlled block, or a bent hook in the lift mechanism [see diagrams on page 92].

Also, the operator can miss or lose a wire when he inserts the temporary separator or when he transfers the separated bundle to Teflon-covered nails [see top photo page 95]. To date, the error rate has been about four bits per million. Corrections can be made before encapsulation by cutting erroneous wires from their diodes and connecting new lines in their place.

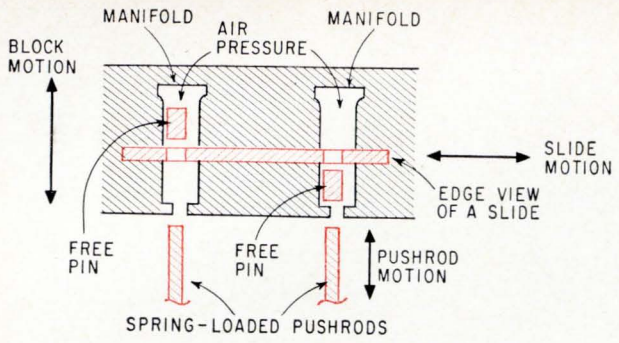
Self-contained unit

Various braid memories have been made at MIT over the last three years. The models made with the Jacquard loom represent a step beyond the feasibility "breadboards" described in earlier reports.[1, 2] The latest system was designed as a complete unit, self-contained in all aspects except power supplies. The model was intended to test not only the manufacturing process but the design and operation of the resulting braid memory system as well.

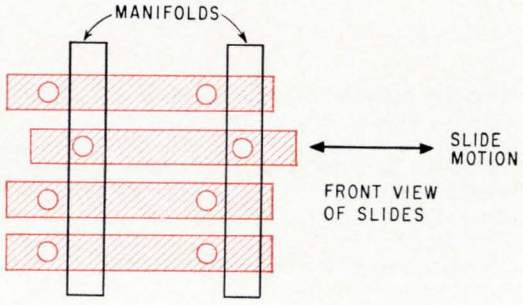
The total package, whose volume is approximately 270 cubic inches, houses about 500,000 bits. A 16-bit input address generates a 16-bit output word. A photograph of a partly assembled system is on page 98, and statistics are listed in the table on the facing page.

The system consists of the braid, the sense board, and the drive circuit board. The drive section, sense board, and cores can be reused if a change in the braid contents becomes necessary. The braid, of course, must be discarded.

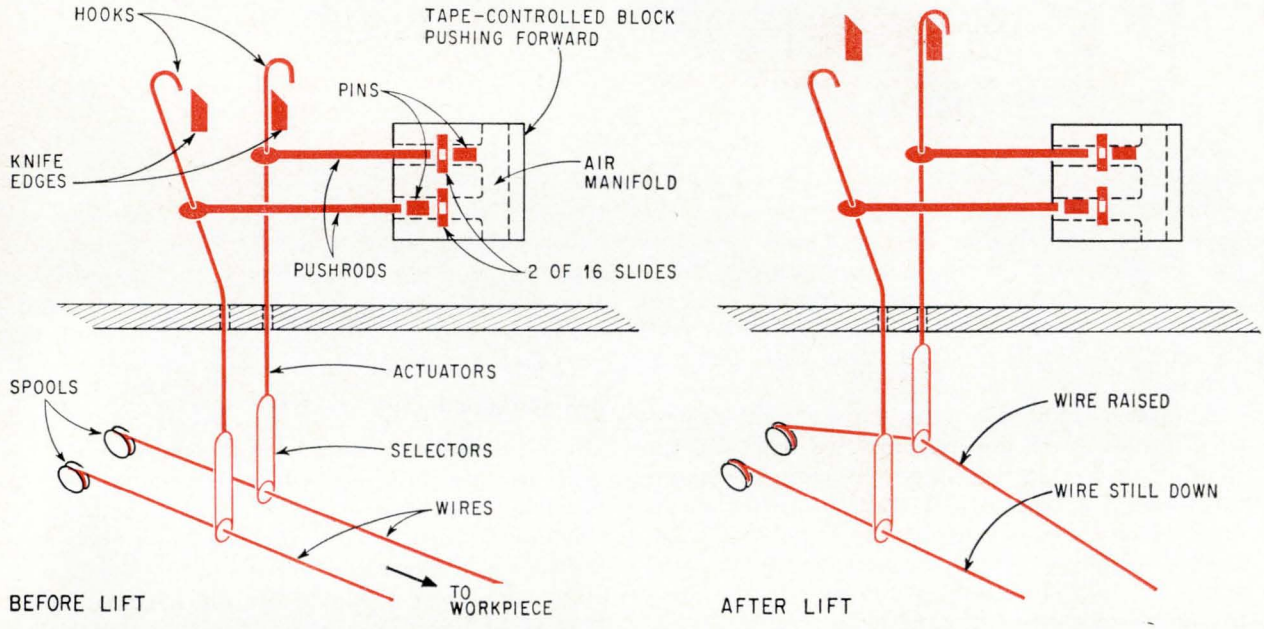
The sense board contains the sense windings, the sensing electronics, and the circuitry for selecting one particular subgroup of 16 bits out of the 256 outputs. The board has holes that exactly match the holes in the braid previously occupied by the



Modified Jacquard loom separates wires for braid memory. The Jacquard lift mechanism is the large green object on the platform; the tape-controlled block, which establishes the combination of wires that are separated with each motion of the lift, is on the right of the lift, behind the plastic air hoses. The copper-colored lines in the lift are actuators. They converge below to link with the wire selectors. The wires from which the braid is made converge into the workpiece in the foreground, into which the light-green Teflon-covered nails are inserted. The nails hold the temporary separators while the braid is being woven. The entire process is controlled by the paper tape reader at lower right.



In the loom, each of sixteen slides moves in turn so that its holes line up with the 16 pins behind it. Some combination of the 16 pins is blown by air pressure through the holes, and the slide then returns to its neutral position, locking the pins in the forward position. For simplicity, this drawing shows only four slides, each controlling two pins.



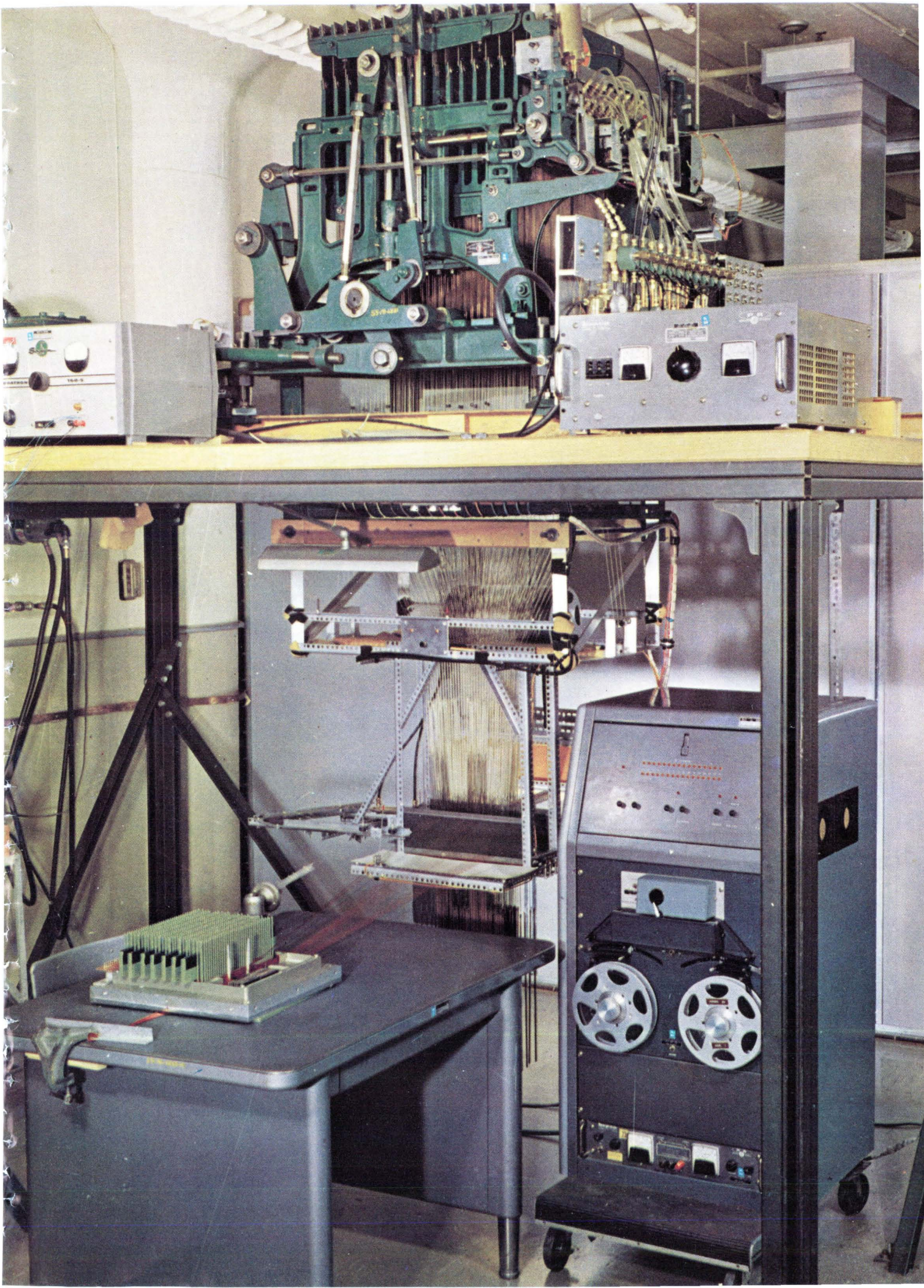
After the pins have been set, the block moves forward against a set of push rods. Where a pin is locked in front of a slide, the push rod pushes a hook connected to an actuator; where the pin is behind the slide, the push rod isn't moved and the hook remains in its vertical position. With the block in its forward position, a set of knife edges moves upward, catching the hooks that haven't been pushed out of the way. The hooks, through the actuators and wire selectors, lift the wires corresponding to a "one" in that position of the braid memory. When hooks are pushed aside, wires corresponding to a "zero" remain in the lower position.

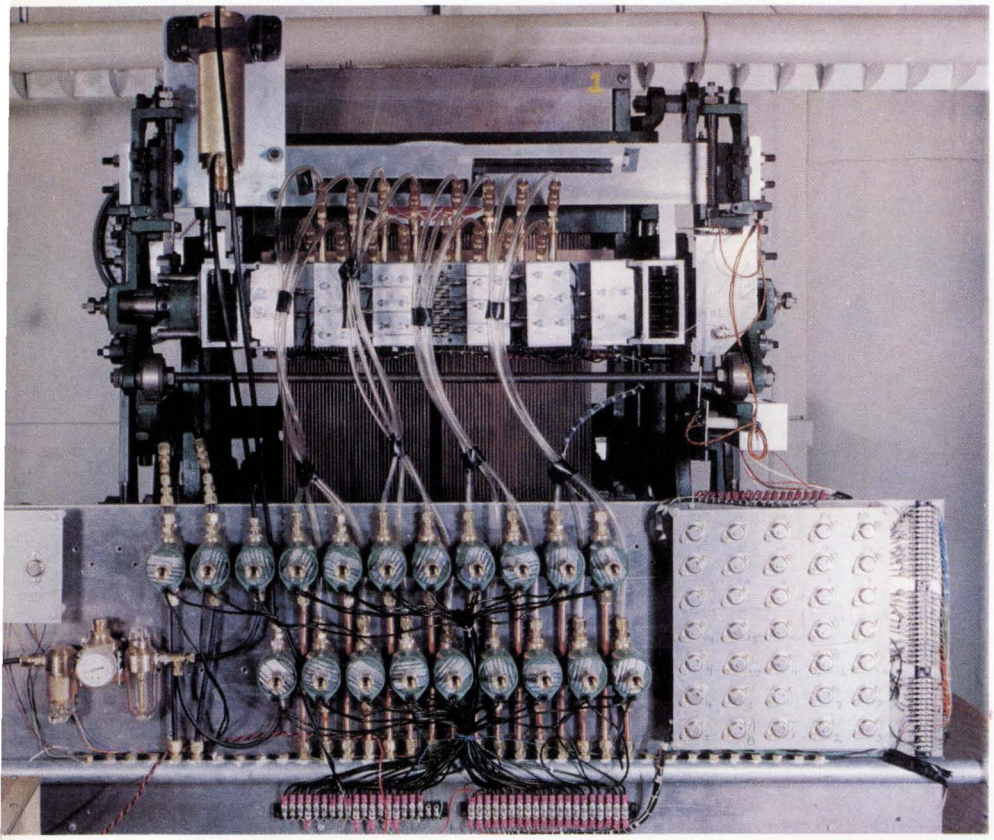
separators. In the detail view, bottom, page 96, the sense board is already mounted on the braid, with some cores in place. Around the holes are 30-turn sense windings, with the turns a part of the wiring in the multilayer board.

The sense windings are connected to low-power NOR gates that serve as sense amplifiers. The output voltages, which exceed 1.2 volts, are sufficient to drive the gates directly, without preamplification.

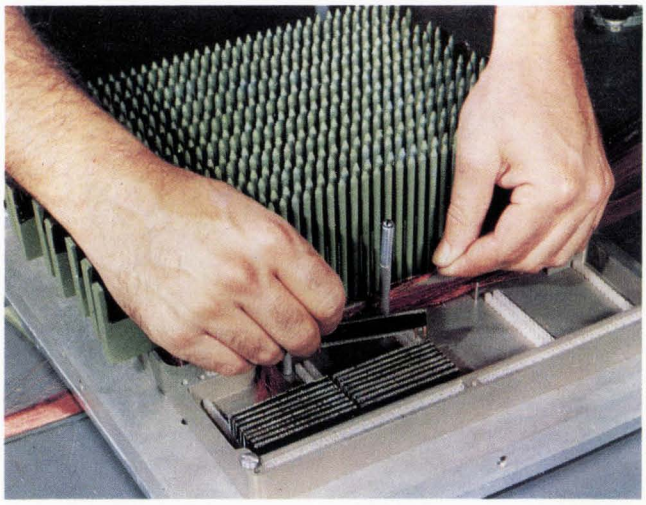
Each sensing winding is connected to an input of a NOR gate (the sensing gate) and to the output of an inhibiting gate, which, when turned on, effectively short-circuits the winding. This is how one subset of 16 bits is selected out of the 256 possible outputs. The sensing gates are combined into 16 sets, each set being in effect a 16-input NOR gate. The outputs of the 16 sets form the 16-bit output word from the memory system. Fifteen of the 16 inputs are always inhibited; only one input is left free to show a zero or a one output from the core. Some 220 dual three-input NOR gate packages are used, including some auxiliary decoding.

The final system element, the drive board, de-



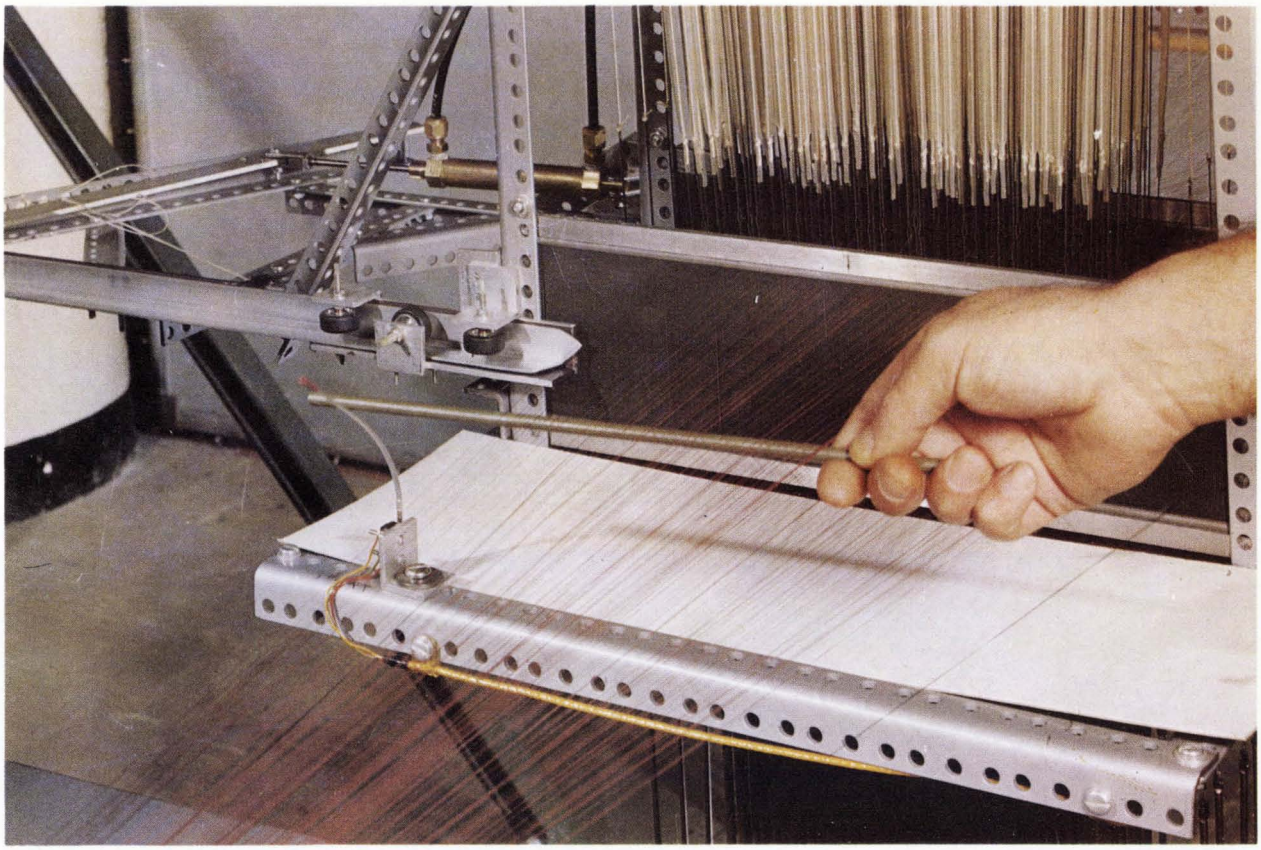


Tape-controlled block, at the upper end of the clear plastic hoses, contains free pins which, with the block lowered, fall to the rear of the block. When the block is in its raised position, shown here, air jets set the pins to establish the combination of wires to be separated during the lift's next move, following immediately.



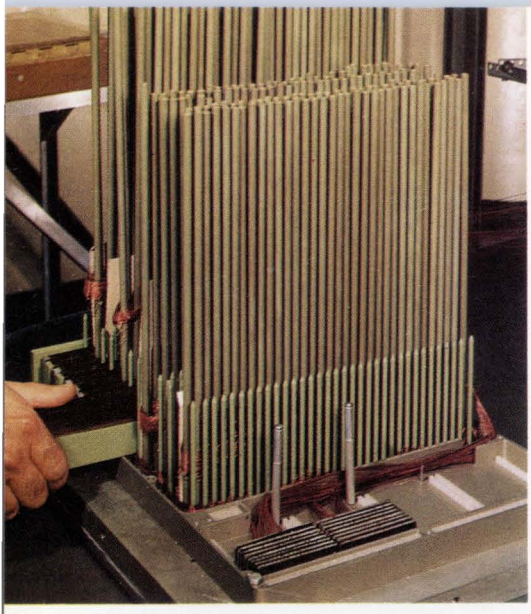
As the second of eight braids is started, the wires are individually soldered to diodes on the black terminal boards. The green Teflon-covered nails will hold the braid separators until encapsulation.

Feedback switches detect any faulty operation of the selection or lift mechanism. The actuators are at the top, with the selectors hanging down below them. The black bead on each selector operates one of the small snap-action switches if that selector is raised. At the completion of the lift motion, the switch settings are compared with the instructions from the paper tape reader. If they don't match, the selection operation is repeated. A few of the beads are just visible peeping over the edge of the platform in the photograph on page 93.



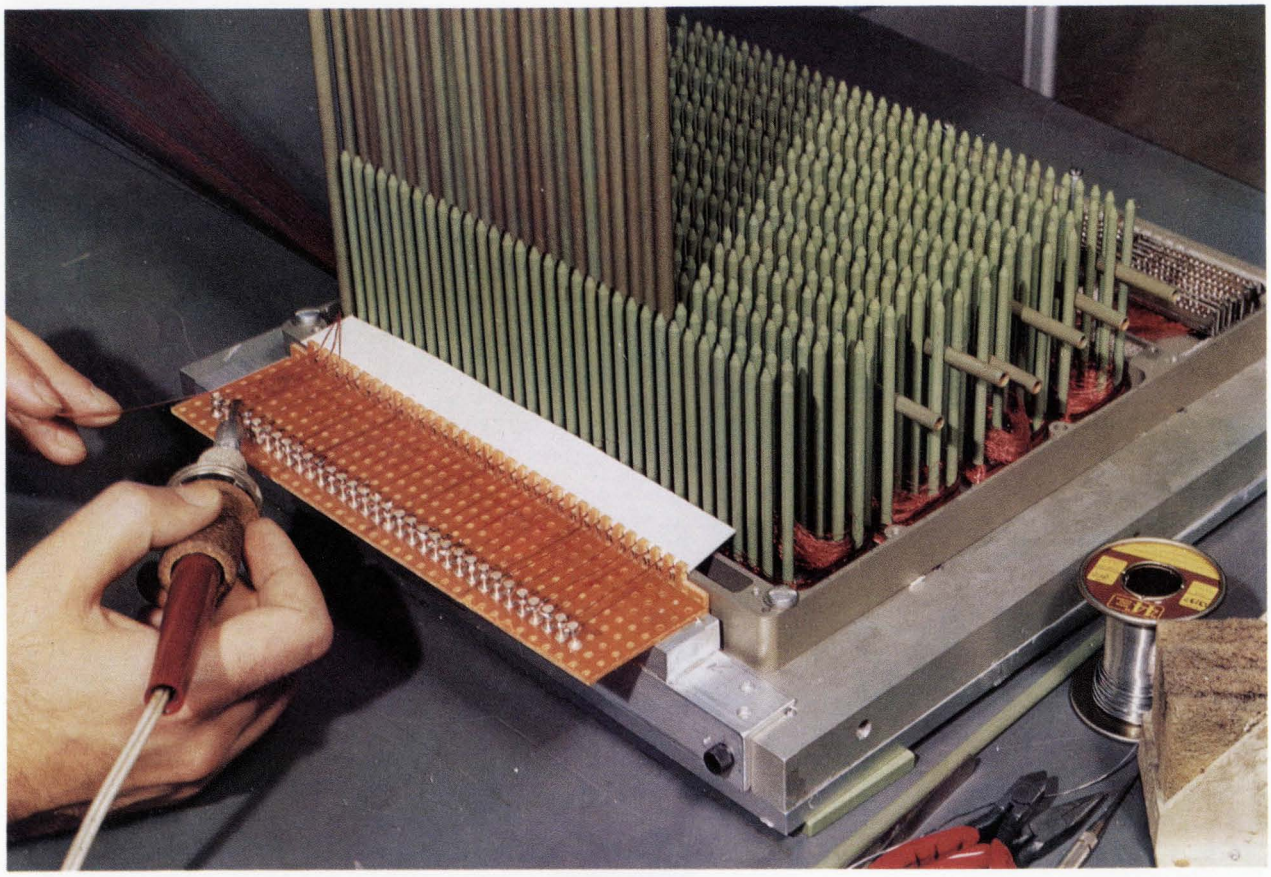
The operator inserts a separator between the upper and lower sets of wires. As he moves the separator toward the workpiece, he trips a switch — the red-topped bar — that initiates the next lift. In this photo, the setting of the pins for the next lift has already begun, with a characteristic "pst-pst-pst" sound. When the lift is complete, the metal angle bar seen just beyond the separator moves forward between the two sets of wires; the operator slides the separator along it to insure that he doesn't inadvertently snag a wire and separate it into the wrong group. The loom will hold the separation indefinitely, until the operator trips the switch with the separator.

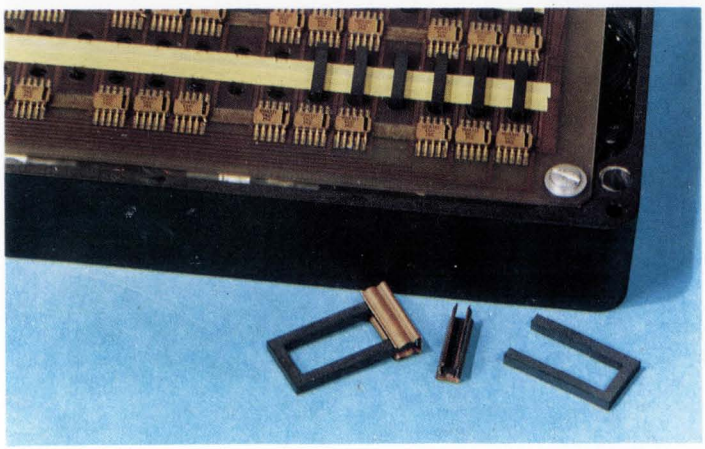
As the separator is moved toward the workpiece, the operator twists it into a vertical position. He must be careful not to lose the separation of the wires during this step. He then sets the separator — a hollow tube— onto one of the Teflon-covered nails at the workpiece.



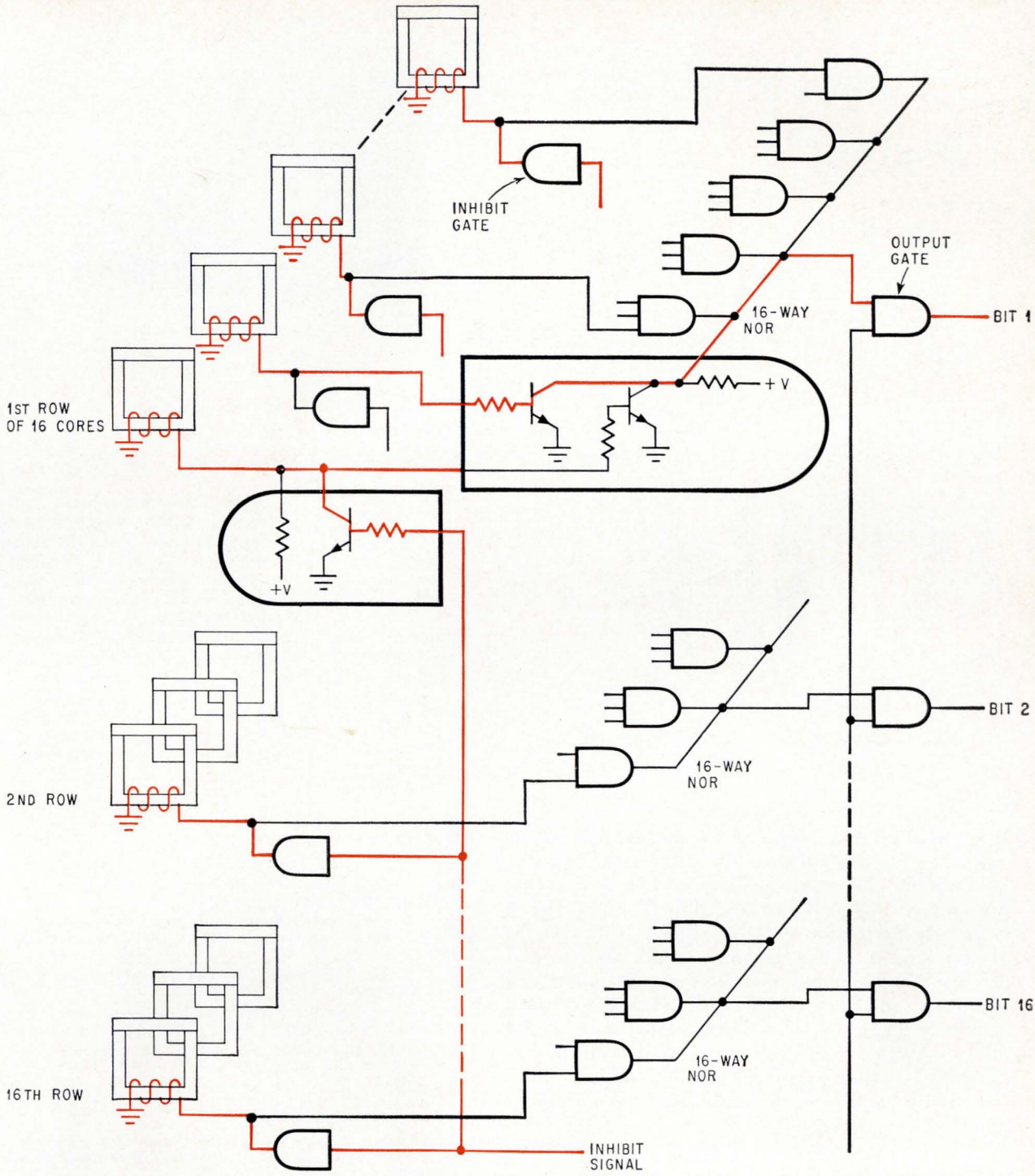
The completed braid is transferred from the temporary separators onto the nails. When the vertical slide is pulled out, the separators and braid drop into the frame. After the separators are removed, the nails retain the braid separations. Replacing the slide holds the braid down so that a new braid can be woven on top of the previous ones.

With the braid in the frame, the wires are soldered to terminals in groups of eight. The loom separates the wires for this operation just as it did in the assembly of the braid itself. As each group is soldered, the wires are cut from the loom. Successive braids in the memory are soldered to the same lugs. When all eight braids are complete, the wires are disconnected from the terminals and the braids are encapsulated. A current-return wire is included in each braid.





The sense board, with some cores in place, is mounted on the braid. Multiturn sense windings are part of the multilayer board. Two U-cores and their cross-pieces are at the bottom.

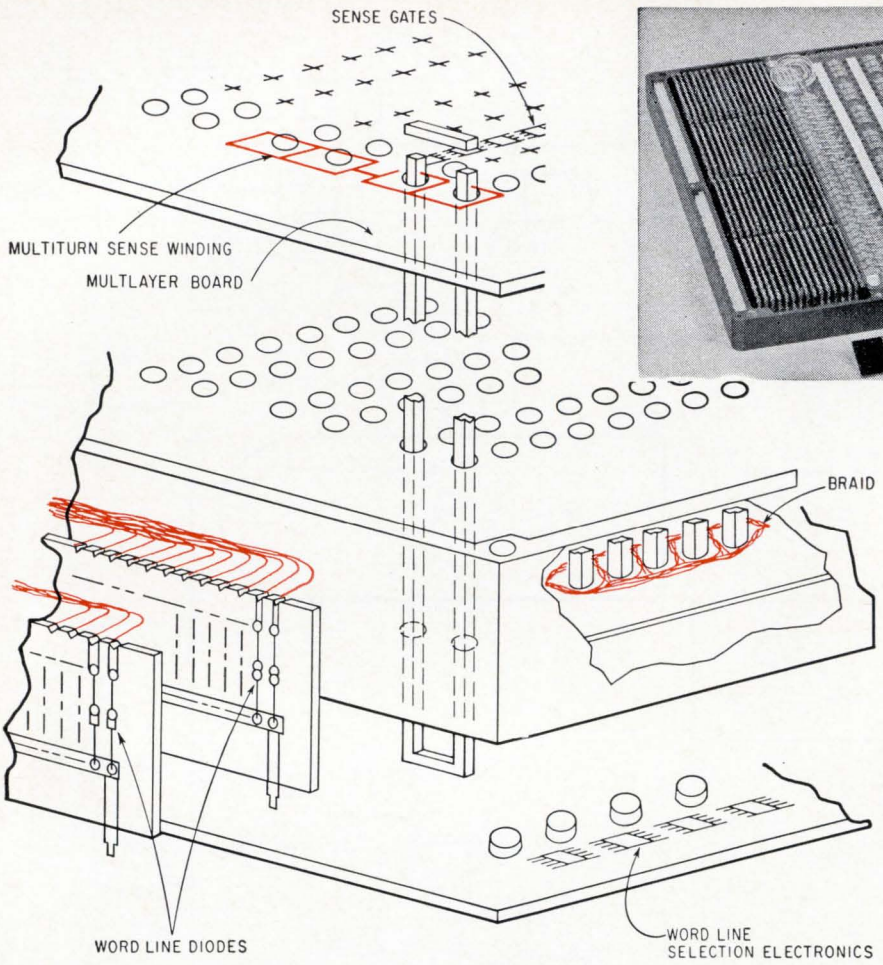


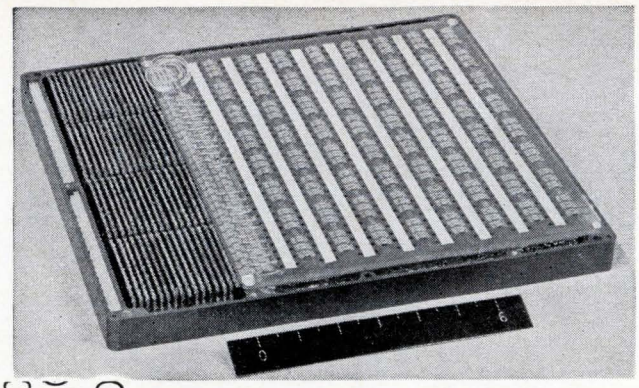
Each word line in the MIT braid memory links 256 cores. A single inhibit signal short-circuits the sense lines from a column of 16 cores; 15 inhibit signals short-circuit 240 cores. In any single row of 16 cores feeding a 16-way NOR gate, 15 are inhibited and one is active. The 16 active cores deliver one 16-bit word to the output gates.

codes 12 of the 16 address bits and generates the current to be sent down a word-line. The other four address bits go to the sense board. The line-selection method is of the conventional diode-steering or diode-matrix type.

Speed vs. size

Wired memories that have very short cycle times can be made at the expense of density, braid length, and complexity of electronics. Cycle times can be in the neighborhood of 300 nanoseconds. These memories are most useful as microprogram stores of about 100,000 bits. At the other end of the scale, a single braid unit is probably limited to somewhere between 1 million and 10 million bits. Performance deteriorates with length, or number of cores; with present wire dimensions, the practical limit is about 1,000 cores. The braiding of





In partly assembled braid memory, above, a large printed-circuit board carrying the sense circuits in flatpacks is installed on top of the braid. The U-shaped cores will be inserted through holes in the p-c board. Adding the drive circuits increases the thickness shown here by about 50%. Complete assembly of braid memory in exploded form, at left, shows drive circuits on the bottom, cores and braid in the middle, and sense circuits on top.

10 million bits on 1,000 cores would require 10,000 wires and 10,000 diodes. For maximum capacity and minimum cost, all numbers should be rounded to the next higher power of 2. For example, 10,000 wires would require a 14-bit address and a 14-bit decoding circuit. But the same length address and a very small amount of additional decoding can handle up to 16,384 wires, which, with 1,024 cores, can store 16,777,216 bits. These large braids would be quite slow, with cycle times of 5 to 10 microseconds. Obviously, a multiple-unit braid system is possible, and even desirable, if the replacement problem can be solved.

Wired memories face competition from large-scale integrated-circuit memories and from photographic storage units. For small amounts of storage, LSI units will soon be reasonable alternatives to the braid—probably as soon as a 1,000-bit chip with its own address decoding becomes available. For very large memories, photographic storage techniques are clearly superior, though they must be read out serially, bit by bit. The relatively large initial investment necessary for even small photographic permanent memories makes them impractical for systems of a few million bits.

The future of wired memories, then, lies in the range of 100,000 to 10 million bits. Within this range, they should be a useful addition to the choices available to system designers.

References

1. R.L. Alonso and W.H. Aldrich, "The Braid Transformer Memory," Report R-498, MIT Instrumentation Laboratory, Cambridge, Mass., September 1965.

2. W.H. Aldrich and R.L. Alonso, "The Braid Transformer Memory," IEEE Transactions on Electronic Computers, August 1966, p. 502.

3. A.L. Hopkins, "Electronic navigation charts man's path to the moon," Electronics, Jan. 9, 1967, p. 109.

4. T.L. Dimond, "No. 5 Crossbar AMA Translator," Bell Laboratories Record, February 1951, p 62.

5. I.R. Butcher, "A Prewired Storage Unit," IEEE Transactions on Electronic Computers, April 1964, p. 106.

6. G.G. Pick, S.B. Gray, and D.B. Brick, "The Solenoid Array: a New Computer Element," IEEE Transactions on Electronic Computers, February 1964, p. 27.

7. B.W. Kington and D.M. Taub, "The Design of Transformer (Dimond Ring) Read-only Stores," IBM Journal of Research and Development, September 1964, p. 443.

8. P. Kuttner, "The Rope Memory, a Permanent Storage Device," American Federation of Information Processing Societies, Conference Proceedings, Vol. 24, October 1963, p. 45.

9. R.L. Alonso and J.H. Laning Jr., "Design Principles for a General Control Computer," Institute of Aeronautical Sciences, New York; Fairchild Publication Fund Paper FF-29, April 1960.

10. J.A. Rajchman, "Static Magnetic Matrix Memory and Switching Circuits," RCA Review, Vol. 13, June 1952.

11. K. Olsen, "A Magnetic Core Matrix and its Application to a Coincident-Current Memory," Master of Science thesis, Massachusetts Institute of Technology, 1952.

12. U. Ecco and G.B. Zorzoli, "The Picture History of Inventions," Macmillan, 1963.

Acknowledgment

Development of the braid memory was financed by the National Aeronautics and Space Administration under Contract NAS-4065.