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INSTRUCTION MANUAL

FOR

ADAC CORPORATION

MODEL 1030

DATA ACQUISITION

AND

CONTROL SYSTEM

IM-678
A2-10019, Rev. 6

PREFACE

ORDERING CODE

The ordering code for the Model 1030 is as follows:

1030-□-□-□-□-□-□

Mux	A/D Range	A/D Type & Speed	No. of DACs	DAC Range	DC/DC Converter
8DI	A: +10V	1: 100KHz	0	0: None	O: Omit
16SE	B: $\overline{0}$ - 10V	3: 35KHz	1	A: +10V	P: Include
16PD	C: +5V	1PGA: 100KHz	2	B: $\overline{0}$ to 10V	
16DI	*D: $\overline{0}$ - 5V	PG=1,2,5,10		C: +5V	
32SE		1PGB: 100KHz		D: $\overline{0}$ to 5V	
32PD		PG=1,2,4,8			
32DI		3PGA: 35KHz			
64SE		PG=1,2,5,10			
64PD		3PGB: 35KHz			
		PG=1,2,4,8			

* Not available with 100 KHz module.

ADAM 12 module used for 35 KHz option.
ADAM 100 module used for 100 KHz option.

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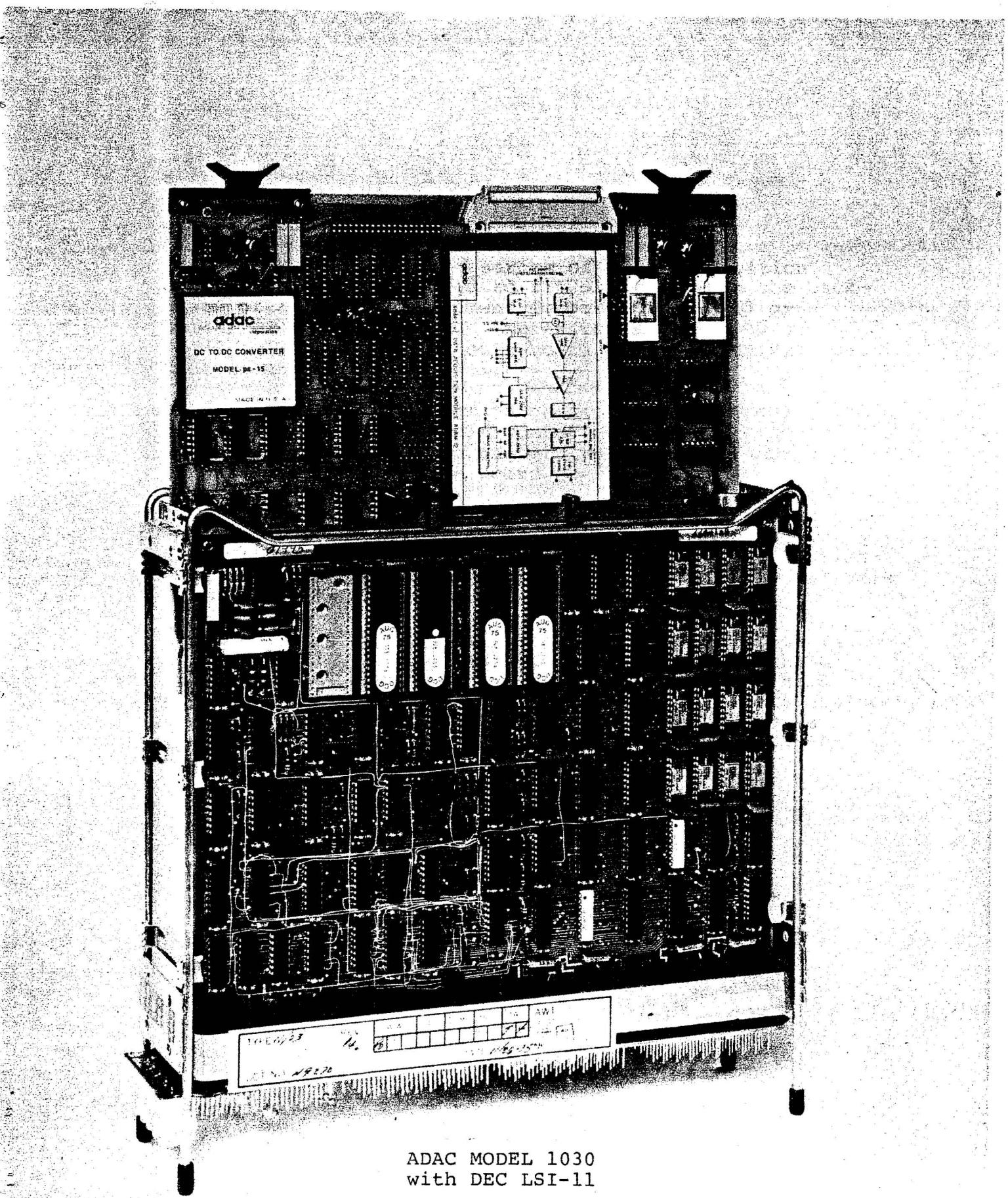


ADAC MODEL 1030
with DEC LSI-11

1. GENERAL DESCRIPTION

The ADAC Model 1030 is a series of data acquisition systems that are designed to fit directly into the backplane of a Digital Equipment Corporation LSI-11 or LSI-11/03 microcomputer. The system is built on an 8 1/2" x 10" printed circuit board and occupies but one slot in any of the chassis.

It uses the +5 volts from the backplane to power its logic as well as to power a self-contained DC to DC converter which supplies +15 volts and -15 volts to the analog circuitry mounted on the board.

A flat shielded ribbon cable assembly is attached to the end of the board opposite the I/O bus connector to bring the analog signals into and out of the computer. Mating connectors and cable clamps are supplied to allow reliable cable to cable connections.

Contained on the board is a multiplexer of up to 64 analog input channels, a programmable gain amplifier with automatic zeroing, a differential input amplifier, a high speed sample and hold amplifier, and a high speed 12 bit analog to digital converter. A program interrupt scheme is included to connect the output of the analog to digital converter to the computer bus.

In addition, provision is made for up to two digital to analog converters with interface to the bus.

II. HANDLING PRECAUTIONS

The system, protected with bubble pack and styrofoam, is shipped in a 15 3/4 x 9 1/2" x 3" cardboard container. Should the system have to be sent back to the factory for any reason, wrap the board in bubble pack, taking care to separately wrap the connector so that it is cushioned on all sides. Pack the unit in its original shipping container.

III. INSTALLATION INSTRUCTIONS

A. General

The critical analog circuitry of the Model 1030 is encased in grounded steel modules to minimize both EMI and RFI pickup. The analog inputs and outputs are connected via shielded ribbon cable and are not run through the I/O connector because of the high frequency digital signals that exist there.

However, care should be taken both in the choice of slot to be used in the computer as well as how the source returns are connected to the system, in order to prevent degradation of system performance.

B. Mounting

The ADAC Model 1030 is designed to work with the DEC LSI-11 or PDP-11/03 series of microcomputers. The board measures 10.4" x 8.5" x .75" and plugs directly into the DEC H9270 backplane or any other backplane designed to the LSI-11 I/O bus pinning. The H9270 backplane consists of a group of connectors four slots wide (A, B, C, & D) and four slots deep (1, 2, 3 & 4). Each slot contains 36 lines (18 each on component and solder side of the circuit board). The LSI I/O bus is contained within two slots (A & B or C & D). The Model 1030 occupies four slots (A, B, C, & D) of one row and can be used in any of the four slots. The "A" connector is the one furthest to the right when viewing the board from the component side, fingers down.

CAUTION: The board should be inserted or withdrawn only with power off. Damage can result if the board is plugged in backwards.

C. Bus Grant Capacity

Control signals provided by the LSI-11 CPU card include two daisy-chained grant signals which provide a priority structured I/O system. These signals are BIAKO/BIAKI (for interrupts) and BDMGO/BDMGI (for DMA grant). These signals, generated on the CPU board, normally propagate through the H9270 backplane until they reach the requesting device. Generally, the CPU is mounted in slot 1. The grant signals are first passed to slots 2-CD, and then to slots 2-AB, 3-AB, 3-CD, 4-CD and then to 4-AB. Any cards mounted between the CPU and the Model 1030 must pass the grant signals along, If any of the intervening double slots are not used, then the grant signals must be jumpered on the H9270 backplane in order to maintain the daisy-chained signal continuity.

For each unused slot, AN2 must be jumpered to AM2, and CN2 must be jumpered to CM2 for interrupt continuity. For DMA grant continuity, AS2 must be jumpered to AR2 and CS2 jumpered to CR2.

On the Model 1030, the interrupt acknowledge circuitry inputs on Pin CM2 and exits on Pin CN2.

The following internal jumpers are supplied to provice continuity: AM2 to AN2, AR2 to AS2 and CR2 to CS2.

D. Cabling

A shielded flexible ribbon cable assembly is supplied to carry the analog input and output signals to the Model 1030. In a fully loaded system, two cables are used. The first cable contains the first 32 analog input channels as well as the two DAC outputs. The second cable contains the second group of 32 analog input channels. The cables plug into right angle headers mounted on the board opposite to the bus.

The cable is supplied with a dual cable clamp assembly to allow a reliable cable to cable connection to be made. The shield of the cable is connected to Pin 49 of each connector.

E. Grounding Considerations

To maintain good 12 bit performance, proper grounding of the sources to the data acquisition system is required.

Several different ground points are brought out to the connector. On the board, the analog and digital grounds are run separately, and are tied together at one point only to eliminate possible ground loops. The common point is physically close to the analog return of the analog to digital converter. This point is brought out to J1 connector Pin 48 and should be used as the source return in single-ended systems.

In fully differential systems, both sides of each source are switched in the multiplexer and no direct connection is made to analog return. However, there is a system constraint that the signal plus common mode voltage cannot exceed 10.24 volts. If the source is truly floating (e.g. a non-grounded battery) then a resistor must be connected from the low side of the source to analog return. This is necessary, since, although the multiplexer presents a very high input impedance (over 100 megohms) there is still some finite leakage current that flows (1 nanoampere @ 25°C, 20 nanoamperes @ 60°C). Since two input switches are connected to the source a resistive path must be supplied to analog return for 40 nanoamperes of current.

If the source voltage is a maximum of 10 volts, then a maximum of 6.2 megohm resistor must be connected between the source low terminal and analog return to stay within the system constraint of 10.24 volts maximum of signal plus common mode. If a maximum full scale of 5 volts is used, then the resistor can be about twenty times larger and still maintain proper operation.

A pseudo-differential mode is provided as standard on all models. A fully differential amplifier is included between the multiplexer and the sample and hold amplifier. The output of the multiplexer is internally connected to the high side of the differential amplifier. The low side of the differential amplifier is brought out to connector J1 Pin 50. For single-ended operation, Pin 50 must be jumpered to J1 Pin 48 (analog return). However, if all the sources connected to the multiplexer have a common return, then the common return can be connected to the differential amplifier low terminal (Pin 50) rather than to analog return

(Pin 48). In this mode, there is excellent high impedance isolation between the source return and the data acquisition ground, eliminating potential ground loops and noise problems without sacrificing the number of multiplexer channels that can be fully employed. (Sixteen multiplexer switches can scan 16 sources rather than 8 as in fully differential mode). The same constraints on keeping the common mode as exists for the fully differential mode.

F. Case and Power Grounds

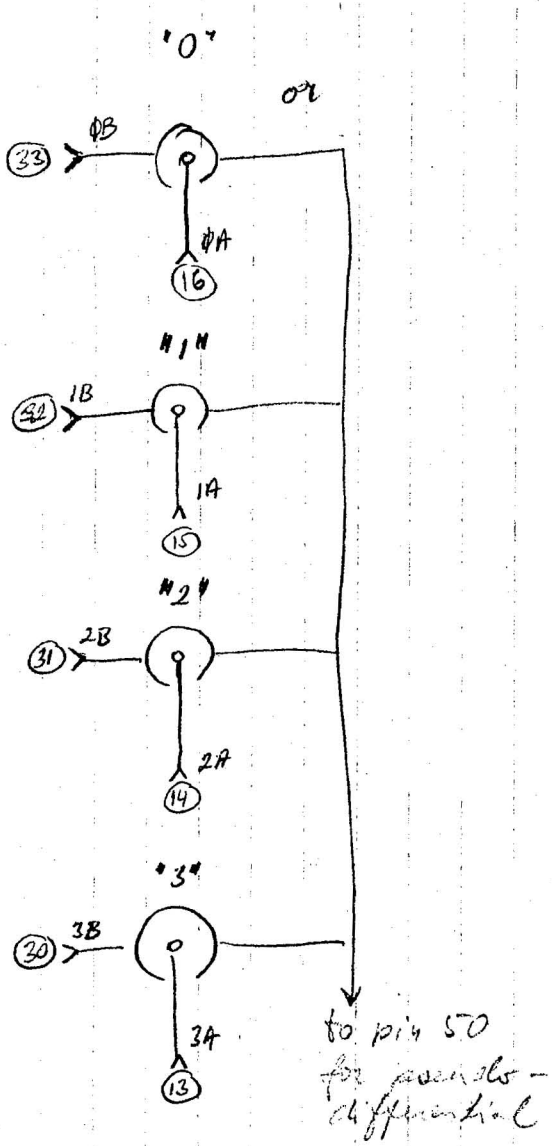
In order to minimize the amount of 60 Hz signal that flows in the input return (Pin 48), the case or power ground for the sources (or the shield of the input cable) must not be connected to analog ground (Pin 48) since this would allow power currents to flow through the input return lead and cause a 60 Hz normal mode signal to be in series with actual signal to be measured.

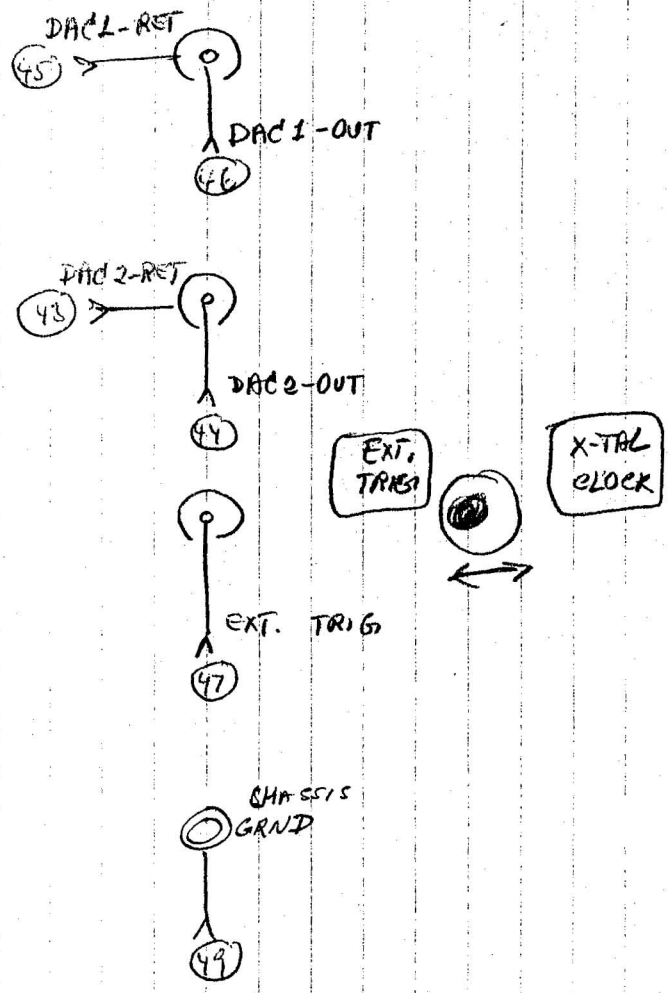
The input shield should be connected to the source case (or power) ground, and be left unconnected at the data acquisition end. A separate wire should be run to connect the source case (or power) ground to a terminal provided on connector J1 Pin 49.

G. DAC Returns

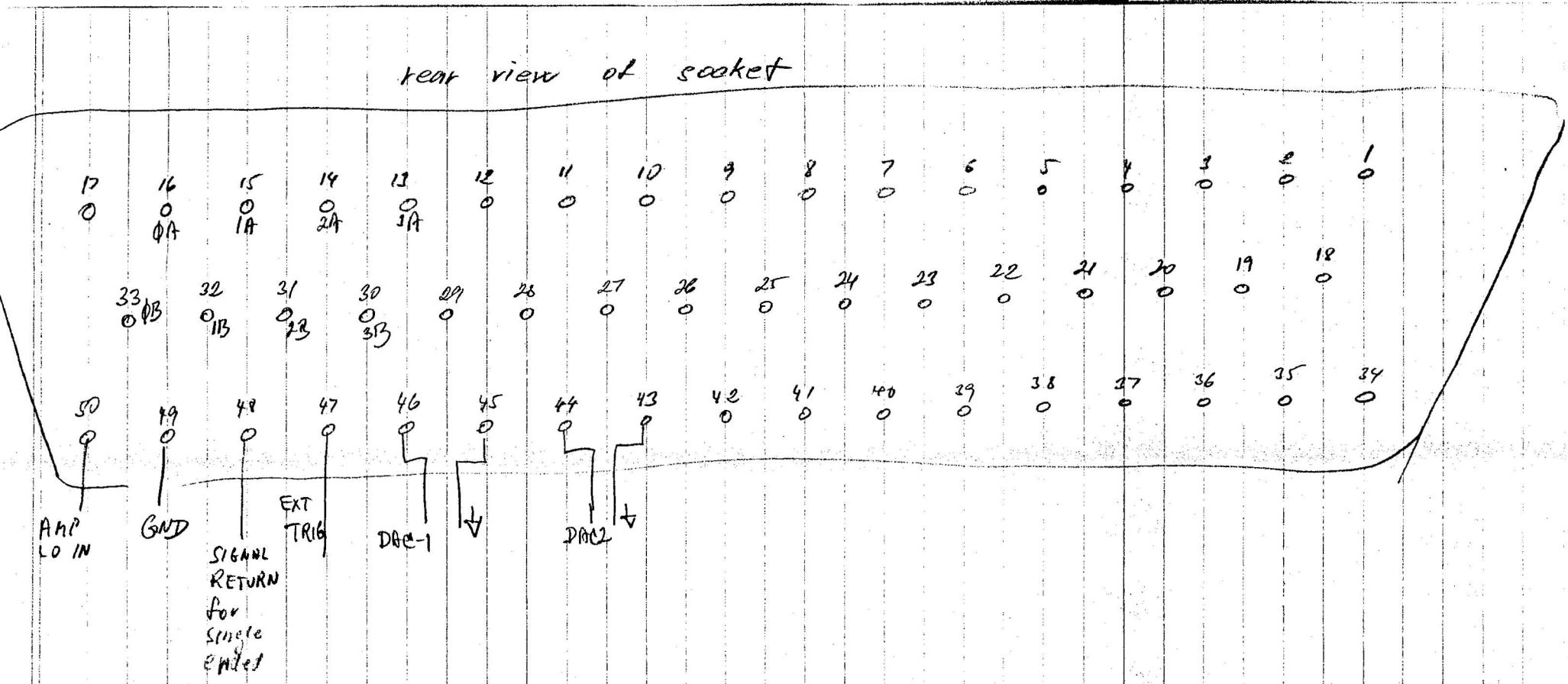
Although all the grounds for each digital to analog converter are connected together on the board, two wires are brought out from each DAC to connector J1, the DAC output and the DAC return. In this fashion, crosstalk between DACs is minimized since the output currents for each DAC are separately returned to the appropriate points in the system. It is good practice to follow through with the separation of returns external to the Model 1030 to the DAC loads.

ADAC1 – model 1030 for LSI-11 w. disk 11-8-78





Pin No.



For pseudo-differential disconnect 0B, 1B, 2B, 3B and tie them to pin 50.

IV. CONNECTOR TERMINATIONS

CONNECTOR J1

(At End of Cable)

Pin No.		Pin No.		Pin No.	
1	CH. 16-8A IN	18	CH. 24-8B IN	34	
2	17-9A	19	25-9B	35	
3	18-10A	20	26-10B	36	
4	19-11A	21	27-11B	37	
5	20-12A	22	28-12B	38	
6	21-13A	23	29-13B	39	
7	22-14A	24	30-14B	40	
8	23-15A	25	31-15B	41	
9	7-7A	26	15-7B	42	
10	6-6A	27	14-6B	43	DAC 2 RETURN
11	5-5A	28	13-5B	44	DAC 2 OUTPUT
12	4-4A	29	12-4B	45	DAC 1 RETURN
13	3-3A	30	11-3B	46	DAC 1 OUTPUT
14	2-2A	31	10-2B	47	EXTERNAL TRIGGER
15	1-1A	32	9-1B	48	SIGNAL RETURN
16	0-0A	33	8-0B	49	POWER RETURN
17				50	AMP LO INPUT

NOTES:

1. Ribbon cable mounted connector: Cannon DD50S
   Mating connector: Cannon DD50P

2. A and B designations for differential inputs. Connect high side of inputs to A pins and low side of inputs to B pins.

3. For single-ended operation, connect Pin 50 to Pin 48. Also connect source return to Pin 48.

4. For pseudo-differential operation, connect source return to Pin 50. Refer to Section III F for constraints.

5. Connect earth or case ground of sources to Pin 49.

6. Run DAC returns separately to their respective loads.

IV. CONNECTOR TERMINATIONS

CONNECTOR J2

(At End of Cable)

Pin No.		Pin No.		Pin No.	
1	CH. 48-24A IN	18	CH. 56-24B IN	34	
2	49-25A	19	57-25B	35	
3	50-26A	20	58-26B	36	
4	51-27A	21	59-27B	37	
5	52-28A	22	60-28B	38	
6	53-29A	23	61-29B	39	
7	54-30A	24	62-30B	40	
8	55-31A	25	63-31B	41	
9	32-16A	26	40-16B	42	
10	33-17A	27	41-17B	43	
11	34-18A	28	42-18B	44	
12	35-19A	29	43-19B	45	
13	36-20A	30	44-20B	46	
14	37-21A	31	45-21B	47	
15	38-22A	32	46-22B	48	SIGNAL RETURN
16	39-23A	33	47-23B	49	POWER RETURN
17				50	AMP LO IN

NOTE: 1. Ribbon cable mounted connector: Cannon DD50S
Mating connector: Cannon DD50P

IV. CONNECTOR TERMINATIONS

CONNECTOR C1

(Connector on PC Board)

1	CH 16-8A IN	2	CH 24-8B IN
3	CH 17-9A IN	4	CH 25-9B IN
5	CH 18-10A IN	6	CH 26-10B IN
7	CH 19-11A IN	8	CH 27-11B IN
9	CH 20-12A IN	10	CH 28-12B IN
11	CH 21-13A IN	12	CH 29-13B IN
13	CH 22-14A IN	14	CH 30-14B IN
15	CH 23-15A IN	16	CH 31-15B IN
17	CH 7-7A IN	18	CH 15-7B IN
19	CH 6-6A IN	20	CH 14-6B IN
21	CH 5-5A IN	22	CH 13-5B IN
23	CH 4-4A IN	24	CH 12-4B IN
25	CH 3-3A IN	26	CH 11-3B IN
27	CH 2-2A IN	28	CH 10-2B IN
29	CH 1-1A IN	30	CH 9-1B IN
31	CH 0-0A IN	32	CH 8-0B IN
33	AMP IN LO	34	POWER RETURN
35	SIGNAL RETURN	36	EXTERNAL TRIGGER
37	DAC 1 OUT	38	DAC 1 RETURN
39	DAC 2 OUT	40	DAC 2 RETURN

NOTES:

1. Connector 1 is a 40 pin header, 3M-3432/1002 mating connector: 3417/3000.
2. A and B are designations for differential inputs. Connect high side of inputs to A pins and low side of inputs to B pins.
3. For single-ended operation, connect Pin 33 to Pin 35. Also connect source return to Pin 35.
4. For pseudo-differential operation, connect source return to Pin 33. Refer to Section III F for constraints.
5. Connect earth or case ground of sources to Pin 34.
6. Connect input shield to Pin 34.
7. Run DAC returns separately to their respective loads.

IV. CONNECTOR TERMINATIONS

CONNECTOR C2

(Connector on PC Board)

1	CH 48-24A	IN	2	CH 56-24B	IN
3	CH 49-25A	IN	4	CH 57-25B	IN
5	CH 50-26A	IN	6	CH 58-26B	IN
7	CH 51-27A	IN	8	CH 59-27B	IN
9	CH 52-28A	IN	10	CH 60-28B	IN
11	CH 53-29A	IN	12	CH 61-29B	IN
13	CH 54-30A	IN	14	CH 62-30B	IN
15	CH 55-31A	IN	16	CH 63-31B	IN
17	CH 32-16A	IN	18	CH 40-16B	IN
19	CH 33-17A	IN	20	CH 41-17B	IN
21	CH 34-18A	IN	22	CH 42-18B	IN
23	CH 35-19A	IN	24	CH 43-19B	IN
25	CH 36-20A	IN	26	CH 44-20B	IN
27	CH 37-21A	IN	28	CH 45-21B	IN
29	CH 38-22A	IN	30	CH 46-22B	IN
31	CH 39-23A	IN	32	CH 47-23B	IN
33	AMP IN LO		34	POWER RETURN	
35	SIGNAL RETURN		36		
37			38		
39			40		

NOTE: Connector C2 is a 40 pin header, 3M-3432/1002.
Mating connector: 3M-3417/3000.

V. SPECIFICATIONS

A. ANALOG INPUTS

Number of inputs to multiplexer	64 single ended 32 true differential 64 pseudo-differential
Input Voltage Range (full scale range)	
1030-X-X-3-X-X-X (35 KHz)	-10V to +10V, 0 to +10V - 5V to + 5V, 0 to + 5V
1030-X-X-1-X-X-X (100 KHz)	-10V to +10V, 0 to +10V - 5V to + 5V
With Programmable Gain	Standard ranges, preceded by Gains of 1, 2, 5 & 10 or 1, 2, 4, & 8
Maximum Input Voltage for Proper Operation (signal plus common mode)	-10.24V to +10.24V
Maximum Input Voltage (no damage)	-15V to +15V
Input Resistance	Greater than 100 megohms
Resolution	12 bits
Relative Accuracy	±0.025% of FSR w/o prog. amp. ±0.035% of FSR, ± 100 µV with respect to input, w/prog. gain
Inherent Quantizing Error	± 1/2 LSB
Tempco of Linearity	Less than 3 ppm FSR/°C
Tempco of Range	Less than 30 ppm FSR/°C
Tempco of Offset	0.001% FSR/°C
Maximum Throughput Rate (12 bits)	
1030-X-X-3-X-X-X	35,000 channels/sec.
1030-X-X-1-X-X-X	100,000 channels/sec.
Sample & Hold Aperture Uncertainty	20 nanoseconds
Crosstalk	80dB down at 1 KHz, "off" channels to "on" channels

Differential Amp CMRR	70 dB (DC to 1 kHz)
Sample & Hold Feedthrough	80 dB down at 1 kHz
Maximum Error for FS to FS Transition Between Channels	1 LSB

B. ANALOG OUTPUTS

Number of Outputs	0, 1 or 2
Full Scale Range	-10V to +10V, 0V to +10V - 5V to + 5V, 0V to + 5V
Impedance	Less than 0.1 ohms @ DC
Load Current	5 ma, maximum
Load Capacitance	1000 pf max. for specified settling time
Resolution	12 bits
Relative Accuracy	$\pm$ 0.012% FSR
Total Output Drift at Zero Volts Output	20 ppm FSR/^{o}C, max.
Total Output Drift at Full Scale (includes offset, range, linearity and reference drift)	40 ppm FSR/^{o}C, max.
Settling Time to 1/2 LSB	5 microsec., typical 10 microsec., maximum
Slew Rate	10 V/microsecond

C. ENVIRONMENTAL & PHYSICAL

Operating Temperature	0^{o}C to 55^{o}C
Storage Temperature	-25^{o}C to 85^{o}C
Size	8 1/2" x 10" x 0.375"
Power, with DC/DC Converter	+5V, $\pm$5% @ 2.5 amps
without DC/DC Converter	+5V, $\pm$5% @ 1.2 amps
	$\pm$15V @ 150 ma

VI. THEORY OF OPERATION

A. General

In its maximum configuration, the ADAC Model 1030 contains a 64 channel multiplexer, a programmable gain amplifier, a high speed sample and hold amplifier, and a high speed 12 bit analog to digital converter. A complete program interrupt interface with a flexible addressing scheme is always included to connect the ADC to the bus. An optional internal clock and/or external trigger is included to allow synchronization of the ADC start pulses to a fixed time base.

Provision is also made for two 12 bit digital to analog converters. A DC/DC converter, which derives its input power from the computer +5 volt supply, supplies a clean +15 volt and -15 volt power to the analog circuitry.

1. Multiplexer

The multiplexer used on the Model 1030 is of MOS FET design with guaranteed break before make switching action. In conjunction with the differential amplifier that follows it, the multiplexer presents a very high input impedance (greater than 100 megohms) to the sources being scanned. The first 16 channels of the multiplexer are included within the same module that contains the differential amplifier, sample and hold and analog to digital converter. An additional 48 channels are supplied optionally on the printed circuit board.

By means of jumper selections, the multiplexer has three modes of operation: single-ended, pseudo-differential and fully differential.

In the single-ended mode, the common return of all sources are connected together to the analog return of the system. Up to 64 separate inputs may be scanned.

In the pseudo-differential mode, the common return of all sources are connected together to the low input side of the differential amplifier. This provides for a high degree of isolation between the source return and the data acquisition ground, allowing greatly improved system performance for situations in which the sources are physically located close to one another but distant from the

data acquisition system. Greater than 70 dB of common mode rejection can be obtained of unwanted noise voltage that may appear between the two grounds. In this mode, up to 64 separate inputs may also be scanned.

In the fully differential mode, both sides of each source are separately switched into the two sides of the differential amplifier simultaneously. This mode allows the returns for each source to be different in potential from one another as well as the data acquisition system. This mode is useful for applications where the sources are physically remote from one another as well as the system, and especially useful in noisy electrical environments. In this mode, up to 32 different sources may be scanned.

2. Programmable Gain Amplifier

The programmable gain amplifier option is very useful in applications where a dynamic range of greater than 4096 as supplied with a 12 bit converter is needed. There are four gain settings that are supplied: gains of 1, 2, 5 and 10. With a gain of 10, a dynamic range of over 40,000 to 1 is provided. Other gain ranges, such as 1, 2, 4 and 8 can also be provided, if desired.

An extremely useful feature that is provided with the programmable gain option is automatic zeroing. With this feature, when the ADC is not in a conversion cycle, the offsets of the multiplexer, programmable gain amplifier and the differential amplifier are measured and stored on an integrating capacitor. When the command is given to start the ADC, the zero loop is broken, and a compensating offset is applied to the differential amplifier to cancel out any drifts that may have occurred with time or temperature. Because of this feature, the zero position of the system is held solidly, regardless of gain setting.

The programmable gain option can be supplied with all full scale ranges. The following table gives the truth table for the bus data bits BDAØ4 and BDAØ3 which are used for establishing the gain.

GAIN	E FS	BDAØ4	BDAØ3
10	1V	0	0
5	2V	0	1
2	5V	1	0
1	10V	1	1

17-8-78

Sample & Hold

L1 $e_p = A \cdot 2\pi \cdot f \cdot T_a$

L2 $f = \frac{e_p}{2\pi \cdot A \cdot T_a}$

A = full scale signal amplitude
T_a = effective aperture time

R_1	R_2	R_3	R_4
e_p	f	A	T_a
L1	L2		

```
01 *LBL1
02  GSB3
03  RCL2
04    X
05  PRTX
06  STO1
07  RTN

08 *LBL2
09  RCL1
10  GSB3
11    ÷
12  PRTX
13  STO2
14  RTN

15 *LBL3   2π·A·Ta
16    2
17   PI
18    X
19  RCL3
20    X
21  RCL4
22    X
23  RTN
```

```
     0.50 STO1
    20.00 STO3
  24.-06 STO4
          GSB2
   165.79 ***
    20.00 ENT↑
  1024.00  ÷
 19.53-03 ***
          STO1
          GSB2
6.476+00 ***
  20.-09 STO4
  10.-03 STO1
          GSB2
3.979+03 ***
```

3. Sample and Hold

A high speed sample and hold amplifier is always included between the multiplexer differential amplifier and the analog to digital converter. Its primary function is to reduce the effective aperture time or "window" during which the ADC is connected actively to the source. With no sample and hold, the source would be actively connected to the ADC for the full 24 microseconds it takes to convert. Depending upon the highest frequency components present in the signal being measured, significant peak errors could occur because of the input signal changing during a conversion. The sample and hold amplifier reduces the effective aperture time from 24 microseconds to 20 nanoseconds.

The peak error caused by the effect of finite sampling interval can be calculated from:

$$e_p = A\, 2\pi f\, T_a$$

where: e_p = peak error voltage

A = full scale signal amplitude

f = highest frequency component in signal

T_a = effective aperture time

If a maximum of one-half of a least significant bit is desired for this error source, then the maximum frequency content of the source must be:

$$f_{max} = \frac{e_p}{2\pi A\, T_a}$$

With no sample and hold: $f_{max} = 1.5$ Hz

With the sample and hold: $f_{max} = 1900$ Hz

4. Analog to Digital Converter

A high speed 12 bit analog to digital converter is included with each system. The converter employs the successive approximation technique and utilizes monolithic quad current switches to obtain stable, precise current sources that can be switched at high speeds. The reference is a premium grade zener diode having a very low temperature coefficient. The reference current is slaved to the junction temperature of the most significant quad chip so that even small temperature changes of the chip caused by the switching action are compensated for as well as larger temperature changes caused by changes in ambient conditions.

A large number of full scale ranges are provided by merely changing a jumper on the master printed circuit assembly. Potentiometers are mounted on the edge of the board to facilitate calibration.

5. Converter Timing

The converter timing is such that a 5 microsecond delay follows the trigger pulse. This allows the multiplexer and amplifiers which follow, to settle before conversion. At the end of the delay, the successive approximation conversion takes 24 microseconds for the ADAM 12 module and 5 microseconds for the ADAM 100 module. This allows a sampling rate of 35 KHz for the ADAM 12 and 100 KHz for the ADAM 100, exclusive of computer instruction time.

If the programmable gain and auto zero option is used, the timing is identical to the above. In addition, there are a set of MOS FET switches which disconnect the multiplexer and short the differential amplifier inputs. These inputs are shorted at all times except during the 5 microsecond settling time. While they are shorted, an auto zero integrator is employed to compensate for any offsets in the amplifiers. This timing sequence allows the auto zero function to be transparent to the system timing and allows the system to maintain its normal conversion time.

Because auto zeroing is done during a previous cycle, a conversion should not be started with the same instruction that changes gain. It is preferable to change gain by loading the control register, then start conversion by loading the multiplexer register.

Suggestion:

To limit 100KHz, 10KHz, 1KHz

external X-TAL clock for accurate sample rate.

4-AUG-78 L. Pek

6. ADC Triggering

A conversion cycle can be initiated in one of four ways:

a) Loading the multiplexer channel address register

When the higher order byte of the status register is addressed to load the desired mux channel, a "conversion start" pulse is generated.

b) Loading the lower order byte

When the lower order byte of the status register is addressed and bit BDAØØ is a ONE, a "conversion start" pulse is generated. The lower order byte is also used to load the desired gain code if the programmable gain amplifier option is used.

c) Internal Clock (optional)

If bit BDAØ1 of the status register is loaded with a ONE, it enables the internal clock mounted on the board. The clock is a free running multivibrator whose rate is controlled over a 5 to 1 range by a potentiometer located on the top edge of the board. The nominal range is 20 kHz to 4 kHz. If desired, the range can be displaced by changing one resistor. When the internal clock is software enabled, triggering modes a) and b) listed above are disabled.

d) External Trigger

A jumper arrangement on the board allows hard-wire selection of an external trigger, which enters the system through connector J1, rather than the internal clock. When using the external trigger, modes a) and b) can be disabled as in c) by loading a ONE in bit BDAØ1 of the status register. The ADC will be triggered each and every time there is a low to high transition on the external trigger line if bit BDAØ1 is a ONE.

7. Digital to Analog Converters

Provision is made on the board for two 12 bit digital to analog converters. Each DAC has its own 12

bit register to store the data word transferred from the computer and has the capability to settle to its programmed output from any other output in 10 microseconds or less. A jumper arrangement is provided for each DAC to allow hardwire selection of one of four output ranges. Offset and range potentiometers are supplied on the top edge of the board to allow ease of calibration.

Two wires are brought to connector J1 for each DAC - the output lead and the return lead. Although the return leads of each DAC are connected to the analog return on the board, separation of the return leads all the way to the loads minimizes the possibility of interaction and crosstalk between the DACs.

8. Address Selection

The LSI-11 uses one set of 16 lines to pass the address of the selected device and the data. Address selection circuitry is provided on the 600-LSI-11 to decode and store the information on the bus during the address time. It also supplies appropriate pulses, synchronized to the bus, to communicate with the various registers on the 600-LSI-11. Four decoded outputs are provided and are tagged "status", "data", "DAC 1", and "DAC 2". The "status" line allows information to be read into and out of the status register. The "data" line allows the digitized data to be read from the ADC into the computer. The "DAC 1" line allows data to be transferred from the computer to load DAC 1 register. Likewise, the "DAC 2" line allows data to be transferred from the computer to load the DAC 2 register.

An etched jumper pattern allows flexibility in the choice of addresses for the four registers. The addresses that are provided are $1767xy_8$. The four most significant octal digits are fixed at 1767. The next most significant digit, x, is selectable as is the least significant digit, y. Unless otherwise specified, each system is delivered with the following addresses pre-wired:

176770:	STATUS
176772:	DATA
176760:	DAC 1
176762:	DAC 2

The user can easily change from the above by cutting the etch jumpers and re-jumpering.

In the logic implementation, the address lines set up which register is to be communicated with, the control lines, BDOUT and BDIN, determine whether information is to be read out of or into the computer, and the master sync line, BSYNC, causes the action to occur.

9. Status Register

The status register is used to store various bits of data needed to operate the ADC equipment as well as to store various commands. The portion of the register that is under control is read-write in nature, while the portion that is under control of the ADC is read only. The following table lists the bit positions used in the status register. (See Page 19)

MODEL 1030 STATUS REGISTER

Address 176770

Bit	Signal	Description
D15	Error	Set if ADC trigger occurs and previous conversion is not complete. Interrupt is produced when interrupt bit (D6) is enabled.
D14	Self-test	Used for maintenance purposes only.
D13	Mux-channel 2^5	Loads multiplexer address to select one of 64 channels and initiates a conversion (if EXT Enable, D1, is a zero)
D12	Mux-channel 2^4	
D11	Mux-channel 2^3	
D10	Mux-channel 2^2	
D9	Mux-channel 2^1	
D8	Mux-channel 2^0	
D7	Done	Set by completion of conversion and reset upon reading data register or initialize.
D6	Int. Enable	Program selectable interrupt mode. Interrupt produced by ADC Done (D7) or Error (D15) when selected.
D5	Reserved	Used for special applications only.
D4	Gain 2^1	Sets gain of programmable gain amplifier option. 11 sets lowest gain and 00 sets highest gain.
D3	Gain 2^0	
D2	Seq/Rand	Zero selects random mode for multiplexer. One selects sequential mode for multiplexer. In sequential mode, multiplexer register is automatically incremented at end of each conversion. Triggering of ADC is same as in random mode (See Section VI. A. 6.)
D1	Ext. Enable	Enables clock source to trigger ADC. Jumpers select on-board multivibrator or external trigger.
D0	Start	Triggers ADC, if Ext. Enable, D1 is a zero.

10. Data Transfer Bus Transactions

All bus activity is asynchronous and depends on interlocking of control signals. In every case, a signal from the Model 1030 is generated in response to a signal from the CPU.

Bus Data Transfer Transaction

Name	Mnemonic	Function
Data In	DAT I	Data from
Data Out	DAT 0	Data from CPU to 600-LSI-11
Data Out, Byte	DATO B	Transfers data from CPU to single byte in 600-LSI-11. Data transmitted on: BDA (15:08) for BDAØØ = 1 BDA (07:00) for BDAØØ = 0

The DAT I transaction requests transfer of data from the Model 1030. It is used for monitoring the status register as well as to transfer the ADC digitized data to the CPU. The register to be read is determined by the address transmitted. Address 176770 selects the ADC data. The places the data on lines BDA (15:00).

The DAT 0 and DATO B operations transfer data from the CPU to the Model 1030. They are used for establishing conditions on the status register, such as mux channel, gain, clock operation, ADC start, etc., as well as to transfer data to the digital to analog converters.

The register to be updated is determined by the address transmitted. Address 176770 selects the status register, 176760 selects the first DAC and 176762 selects the second DAC. DATO B can be used to transfer the mux channel only, if BDAØØ = ONE, without changing the gain of the system, since the gain register is located in the lower order byte of the status register.

11. Priority Transfer Transactions

Transfer of bus control from one device to another is determined by priority arbitration logic in the CPU. Requests for the bus can be made at any time (asynchronously) on the bus request (BIRQ) line. During each bus cycle, the arbitration logic first checks for a DMA request and services these first.

If no DMA is present, the priority arbitration logic checks the bus request lines. If the ADC issues a bus request (at the end of conversion) the priority logic issues a grant on the bus grant (BIACK) line. The Model 1030, in turn, issues a bus reply (BRPLY) signal in return.

12. Interrupt Transaction

The Model 1030 causes the interrupt operation to occur if the interrupt enable bit of the status register (D6) is a ONE and an error occurs or the DONE flip-flop is set. When bus grant (BIACK) is asserted, the Model 1030 is selected as bus master and asserts BRPLY and a vector address (130_8) on the BDA lines.

When the data is read from the ADC, the DONE flip-flop is reset. This clears the interrupt request (BIRQ) line and constitutes active release of the bus to the processor.

13. Priority Chaining

The LSI-11 uses physical daisy-chaining of the interrupt acknowledge signal (BIACK) to the various I/O devices in order to establish interrupt priority levels. The highest priority position is 2-CD (if the CPU is located in slot 1). Then, in order, the priority is passed to 2-AB, 3-AB, 3-CD, 4-CD and 4-AB.

The interrupt acknowledge line (IACK) passes through circuitry on the Model 1030 which causes a slight delay before being passed on to other controllers. IACK is blocked to other devices if the 600-LSI-11 is requesting an interrupt. Otherwise, the signal passes through unaltered with the exception of a slight delay.

VECTOR FIGURES

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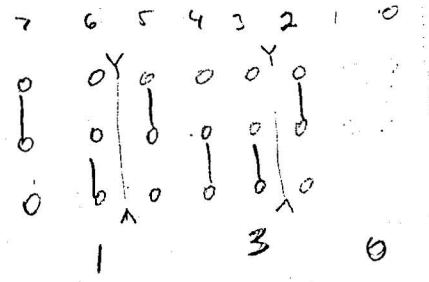

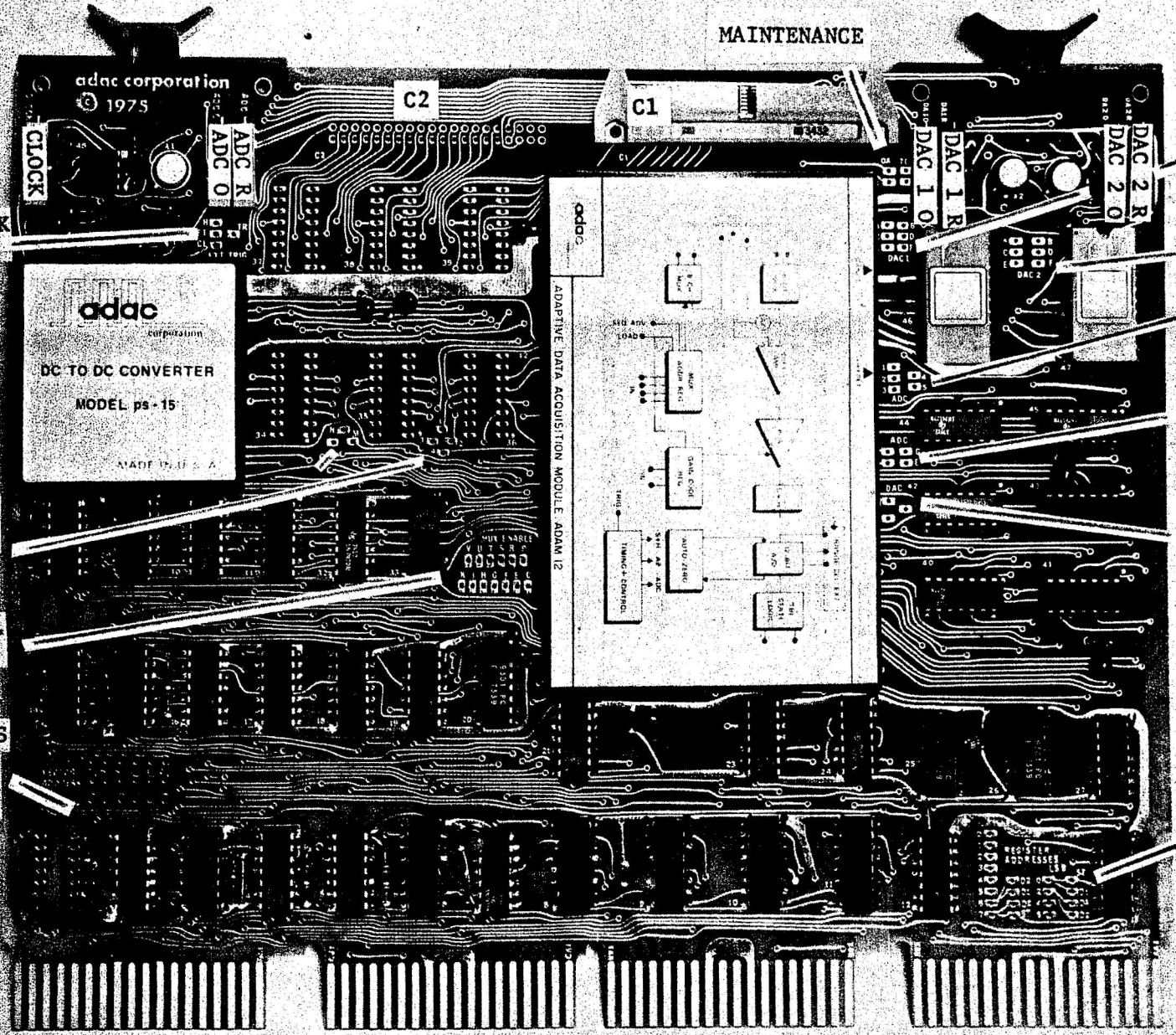

1030
JUMPER LOCATIONS

B. Jumper Options

The system has been configured to allow a maximum of flexibility with a jumper arrangement on the board. Jumpers control the input range of the ADC (including sign extension of the most significant bit), the operating mode of the multiplexer (single-ended, pseudo-differential, and fully differential), use of the internal clock, and the output range of the DACs.

1. ADC Input Range

The following table gives the jumper connections to establish the desired full scale range of the ADC.

Range	Jumpers	
A: -10 to +10V	4-1, 5-3, B-G, E-U	
B: 0 to +10V	4-2, U-G, E-G, 3-G	
C: - 5 to + 5V	4-2, 5-3, B-G, E-U	
D: 0 to + 5V	4-3, U-G, E-G, 2-G	(ADAM 12 Version Only)

2. Multiplexer Channel Capacity (beyond 16 channels)

Number	Type	Jumpers
32	SE	P-E, R-F
32	PD	P-E, R-F
16	DI	P-R-C
64	SE	P-E, R-F, S-G T-H, U-J, V-K
64	PD	P-E, R-F, S-G T-H, U-J, V-K
32	DI	P-R-C, S-T-E, U-V-F

3. Multiplexer Input Configuration

Type	Jumpers
Single-ended	1-2, 3-4, D-N
Pseudo-differential	1-2, D-N, .01 μf from 3 to 4
Differential	1-3, N-M, 1 meg from 1 to 4

4. DAC Full Scale Range

Range	Jumpers
A: -10 to +10V	A-B, E-F, M-B
B: 0 to +10V	B-C, M-U
C: - 5 to + 5V	B-C, E-F, M-B
D: 0 to + 5V	B-C, A-D, M-U

5. External Clock and Trigger Option

In addition to providing ADC start pulses from the status register bit DØ, the Model 1030 is capable of being triggered by an on-board clock or an external trigger. A jumper arrangement is provided to select either the clock or the external trigger. In both cases, the trigger is gated with EXT. ENABLE, which is bit D1 of the status register. If Ext. Enable is set, the selected clock triggers the ADC and the other modes of triggering, such as DØ of the status register and mux. channel transfer, are blocked.

To select the on-board clock, jumper TR-CL. To select the external trigger connect TR-EX. The clock repetition rate is controlled by potentiometer P3. The nominal range of the clock is 50 microseconds to 250 microseconds. The external trigger polarity should be a normally low level, going to a high level to trigger the ADC.

C. Calibration Procedure

The ADC and DACs are precision instruments that were factory calibrated against standards that are traceable to the National Bureau of Standards. The long term stability is excellent, allowing re-calibration intervals of at least six months. Sometimes, however, it may be necessary to adjust range and offset against system conditions that exist rather than against absolute standards. For this reason, some amount of adjustment is provided for the offset and range of the ADC and DACs.

1. ADC Adjustments

To properly make calibration adjustments on the ADC, it is desirable to use a secondary voltage standard that has been calibrated against a primary standard. A number of companies make such standards, such as Analogic, EDC and Fluke

In the use of a standard for calibration, the grounding considerations expounded upon in Section III E & F should be followed. The Analogic Model AN3100 has been found to exhibit the least amount of 60 Hz noise injected into the signal leads.

In calibration of the converter, the output code can be determined by examining the appropriate register in the computer or by having the computer print out the results.

a) ADC Offset

To recalibrate the offset, apply the input voltage shown in the accompanying table, and adjust the offset control so that the LSB alternates equally between "1" and "0". Offset should be readjusted whenever the jumpers are changed to select a range.

Range	Input	Code
-10V to +10V	-9.9976V	
0V to +10V	+0.0012V	000000/1 UNIPOLAR
- 5V to + 5V	-4.9988V	174000/1 BIPOLAR
0V to + 5V	+0.0006V	

b) ADC Range

The offset should be trimmed before adjusting range. To recalibrate range, apply the input shown in the accompanying table, and adjust the range control so that the LSB of the output code alternates equally between "1" and "0". Range should be readjusted whenever the the selected range is changed.

Range	Input	Code
-10V to +10V	+9.9927V	
0V to +10V	+9.9963V	7776/7 UNIPOLAR
- 5V to + 5V	+4.9963V	3776/7 BIPOLAR
0V to + 5V	+4.9982V	

2. DAC Adjustments

A precision calibrated digital voltmeter should be used to monitor the output of each DAC at connector J1, measuring between the DAC output and the return for that DAC.

a) DAC Offset

To recalibrate the offset, apply an input code of 174000 for bipolar or 0000 for unipolar and check that the output of the DAC agrees with the accompanying table.

Range	Input
-10V to +10V	-10.0000V
0V to +10V	0.0000V
- 5V to + 5V	- 5.0000V
0V to + 5V	0.0000V

ADCSR = 176770
ADCBR = 176772

b) DAC Range

The offset should be checked before readjusting the range control. To readjust the range, apply the appropriate input code and set the output to agree with the following table.

Range	Input	Output
-10V to +10V	3777	+9.9952V
0V to +10V	7777	+9.9976V
- 5V to + 5V	3777	+4.9976V
0V to + 5V	7777	+4.9988V

DAC1 : 176760
DAC2 : 176762

D. Diagnostic Program ADACØ5 (12-JUN-78)

Introduction

This program tests the control logic and operation of the ADAC Model 1030 Data Acquisition System. It requests the number of A/D channels available; determines the number of D/A channels; and asks which test is to be performed. Upon receiving a test code followed by CR, it proceeds to perform that test. Control is returned to the monitor when keyboard input is unacceptable, when a test is completed or when the operator types CTL-C. Some tests loop indefinitely, and can be stopped only by CTL-C.

The tests may be performed in any order; however, the LOGIC test (A) should be performed first.

If any DAC test is called and no DACs are present on the board, the program will halt due to a bus time out. If this occurs, the program may be either restarted at 3350 to do all initialization or at 1462 to short cut the test.

The program is supplied with all units as an absolute loader format paper tape. Optionally, it may be purchased on floppy diskette and will have the file name ADACØ5. The files provided are .MAC, .OBJ and .SAV, and an assembled object listing is provided.

Required Equipment

1. LSI-11 computer with at least 4K memory.
2. ADAC 1030 card with up to 64 A/D channels and 0, 1 or 2 D/A channels.
3. Console terminal.
4. Voltmeter or oscilloscope.
5. Signal source.

Detailed Description

1. Operating Procedure

The binary paper tape should be loaded with the Absolute Binary Loader. If floppy is used under RT-11, simply RUN DX1:ADACØ5. In either case, the line time clock must b turned off before loading program. The program is self-starting. It prints the title, asks for the number of

A/D channels (maximum of 64), determines the number of D/A channels (0, 1 or 2), and asks for a test code from A-G as follows:

"A" - Logic check
"B" - Rapid channel scan and printout
"C" - Conversion and printout (one channel)
"D" - D/A conversion of software switch register
"E" - Programmable gain test
"F" - Feed D/A converters from one A/D channel
"G" - Ramp to both D/A.

If an error is made typing the test code, pressing the RUBOUT or DELETE key will erase the letter, and a different one can be inserted. When inputing a number, RUBOUT clears all digits previously inserted, and the whole number must be retyped. All operator inputs must be followed by CR (carriage return).

The bus addresses of the ADAC Model 1030 and the console terminal are in locations 1000-1032 and can be easily changed.

Location	Contents	Explanation
1000	177560	Console terminal keyboard status
1002	177562	Console terminal keyboard buffer
1004	177564	Console terminal printer status
1006	177566	Console terminal printer buffer
1010	6000	Software siwtch register
1012	176770	A/D control and status
1014	176771	High byte of A/D control and status
1016	176772	A/D data buffer
1020	176760	D/A channel 0 data buffer
1022	176762	D/A channel 1 data buffer

Interrupt Vector Addresses:

Location	Contents	Explanation
1026	24	Power fail vector
1030	60	Console keyboard interrupt
1032	130	A/D interrupt vector

Changing any of the above locations effectively changes the constant for the whole program. The restart address is 3350.

2. Tests

A routine called the keyboard monitor waits for the operator to select the next test. Control is returned to the keyboard monitor at the end of the non-looping tests or whenever CTL-C is typed. (Hold the control key and press "C").

Test A: Logic Check

Tests all read/write bits for ability to set and clear. Checks that the DONE and ERR bits are set and cleared at appropriate times, and that conversion time is within preset limits. The interrupt logic is tested to see that interrupts occur properly.

Type "A" followed by CR to initiate logic test. Program will proceed until all logic tests have been executed. Control then returns to the keyboard monitor. Errors (if any) will be printed on the keyboard. Units without the programmable gain option will find errors in clearing bits 3 and 4 of the status register since these bits are not connected unless the option is included.

Test B: Rapid Channel Scan

Scans all available channels using a gain code of 0 and prints the sampled value in octal in a tabular format beginning with channel Ø and proceeding sequentially.

Type "B" followed by CR to start SCAN. Program will convert each channel and print its value. Upon completion, control is returned to the keyboard monitor.

Test C: Conversion and Printout of One Channel

Converts a single A/D channel using a gain code of 3, prints the value in octal and decimal, and loops until a non-existent channel is requested.

Type "C" to perform this test. Program will request a channel number, then perform the conversion. If the operator asks for a non-existent channel, control is returned to the keyboard monitor.

Test D: Digital to Analog Conversion

Converts memory location 6000 to a voltage (according to the convention in Section 3) by sending it to all D/A converters continuously until CTL-C is typed.

Type "D" to start D/A conversion. An error message will be printed if it has been determined that no DACs are present in the system. Control is then returned to the keyboard monitor. Otherwise, all DACs are continuously updated from location 6000 until stopped by CTL-C.

Test E: Programmable Gain Check

The program requests the gain code and the channel to be converted then performs the conversion and prints the value in both octal and decimal (see Section 3).

Type "E" to begin this test. Program will respond by asking for a gain from 0-3 and channel number. When conversion and printout are completed, the program loops to the gain code request and proceeds until an illegal gain code or channel number is inserted, at which time control is returned to the keyboard monitor.

Test F: Feed D/As From A/D

Test continuously updates all D/A converters from the specified A/D converter using a gain code of 3 until stopped by CTL-C.

Type "F" to perform this test. Program will ask for the desired A/D channel number, and proceed to loop through the conversion until CTL-C is typed on the keyboard. If no DACs are present, a message will be printed, and control returned to the keyboard monitor.

Test G: Ramp to D/As

Sends a continuous full scale triangle waveform to both DACs until terminated by typing a "control C".

3. Converting Values to Voltages

The program does not convert A/D readings to voltages. To determine the accuracy of the system, therefore, a conversion must be made. Three things must be considered in doing this conversion:

1) The range of the system.
2) Whether negative voltages are measured.
3) The gain used in the conversion.

The table included with this description gives the possible ranges of the system, and the corresponding mV/bit. Use these conversion factors with the decimal value to determine the measured voltage. If the range includes negative numbers, their value will be printed as a number between 2048 and 4095.

This can be converted to the absolute value by the following formula:

(4095 - value) + 1 where value is the decimal output.

Example: value = 3000

```
 4095
-3000
 1095 + 1 = 1096
```

The number represented by 3000 is -1096. This number can be used with the conversion factory to find the measured voltage.

To find voltage, take the printed decimal value (converted to negative if required) and multiply by the conversion factor from the table.

Example:

gain code:	3
range:	0 to 10
value	2000
conversion factor:	2.44 mV/bit
voltage:	4.88V

Example:

gain code:	2
range:	-10.24 to +10.24
value:	3000
converted to negative:	-1096
conversion factor:	2.5 mV/bit
voltage:	-2.64V

Conversion from Decimal Value to Voltage
(Millivolts Per Bit)

Range	Gain Code 0	1	2	3
0 to 10	.244	.488	1.22	2.44
-10 to 10	.488	.976	2.44	4.88
0 to 5	1.221	1.221	1.22	1.22
- 5 to 5	2.442	2.442	2.44	2.44

ADAC CORPORATION

ADAM 100 PGB-G- 1,2,4,8

MODEL 1030-16SE-A-1PGB-2-A-P

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