
Amdahl 580 Series

**580 / Multiple
Domain Feature
Overview**



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Edition Notice

This is the first edition.

Abstract

The purpose of this manual is to provide a general overview and basic planning information for the 580/Multiple Domain Feature (580/MDF).

This publication assumes the reader is familiar with information contained in:

- *IBM System/370 Principles of Operation* (GA22-7000).
- *IBM System/370 Extended Architecture Principles of Operation* (SA22-7085).

Additional information relating to the specification and operation of 580/MDF is available in the following Amdahl publications:

- *Amdahl 580 Computing Systems Computer Operator's Manual* (MC-108335).
- *Amdahl 580 MACROCODE Reference Manual* (MC-119324).

Reader Comments

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The 580/Multiple Domain Feature (580/MDF) is an innovative way for 580 users to manage and control their processing resources. 580/MDF, like the 580/ACCELERATOR, is another example of Amdahl's commitment to providing unique but compatible solutions to meet the needs of the large-systems user.

580/MDF gives the 580 user the ability to consolidate multiple computer systems into a single processing complex; in addition, when operating multiple system control programs (SCPs) on a single processor, the need to run VM is eliminated. (VM continues to be supported on all 580 Series processors.) In addition, this 580 Series hardware feature eliminates the need for independent production environments and separate test or conversion systems. Isolated, highly secure operation of multiple SCPs is available to the user without incurring the costs or limitations of owning and operating multiple processing complexes. 580/MDF provides multiple, independent operating environments, called domains, which are active concurrently on one 580 Series processor.

580/MDF also provides the Amdahl 580 Series with increased flexibility. A unique combination of hardware, microcode, and MACROCODE is used to support the definition, activation, and operation of multiple operating environments in a single processor.

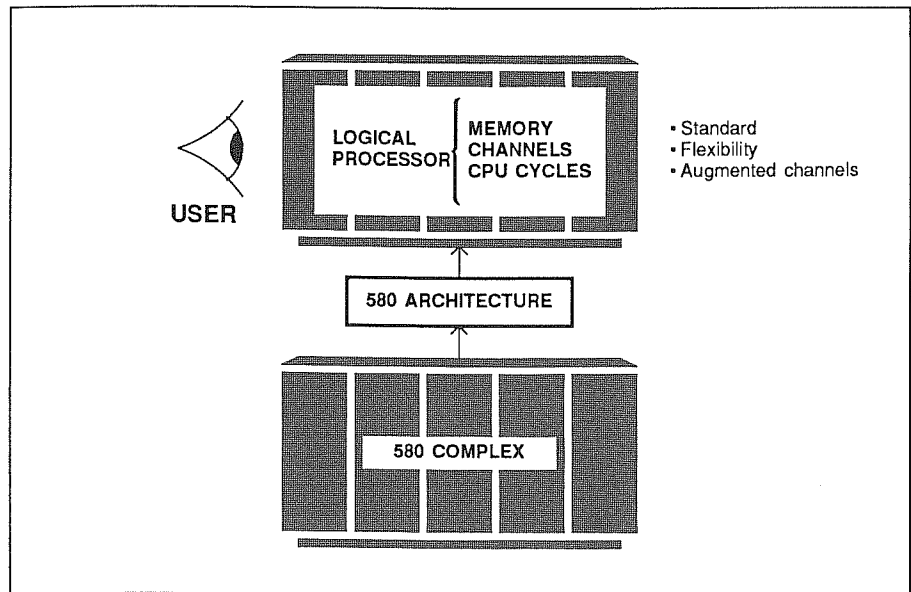


FIGURE 1 A Single Domain

Why was 580/MDF developed?

580/MDF was developed to provide the large-systems user the ability to operate more than one logical system on a single processor. The following 580/MDF features help achieve this:

- Concurrent native support of System 370 (S/370) and 370 extended architecture (370-XA) modes
- No additional system control program (SCP) or other software required
- No required software modifications
- Redundant IBM software licenses may be eliminated
- Performance at least 95% of native mode
- Hardware isolation and protection for each domain
- Dynamic allocation and redistribution of CPU time
- Flexible allocation of main storage and channels from a pool of resources
- Operational characteristics of two physically separate computer systems

What is a domain?

An Amdahl 580 processor creates and maintains a processing environment for the SCP. This environment consists of all the resources required to operate the SCP and is called a domain.

The attributes of a domain include:

- architectural mode
- main storage size
- channel configuration
- operator facilities
- logical processor[†]

[†]A logical processor is functionally equivalent to a physical CPU.

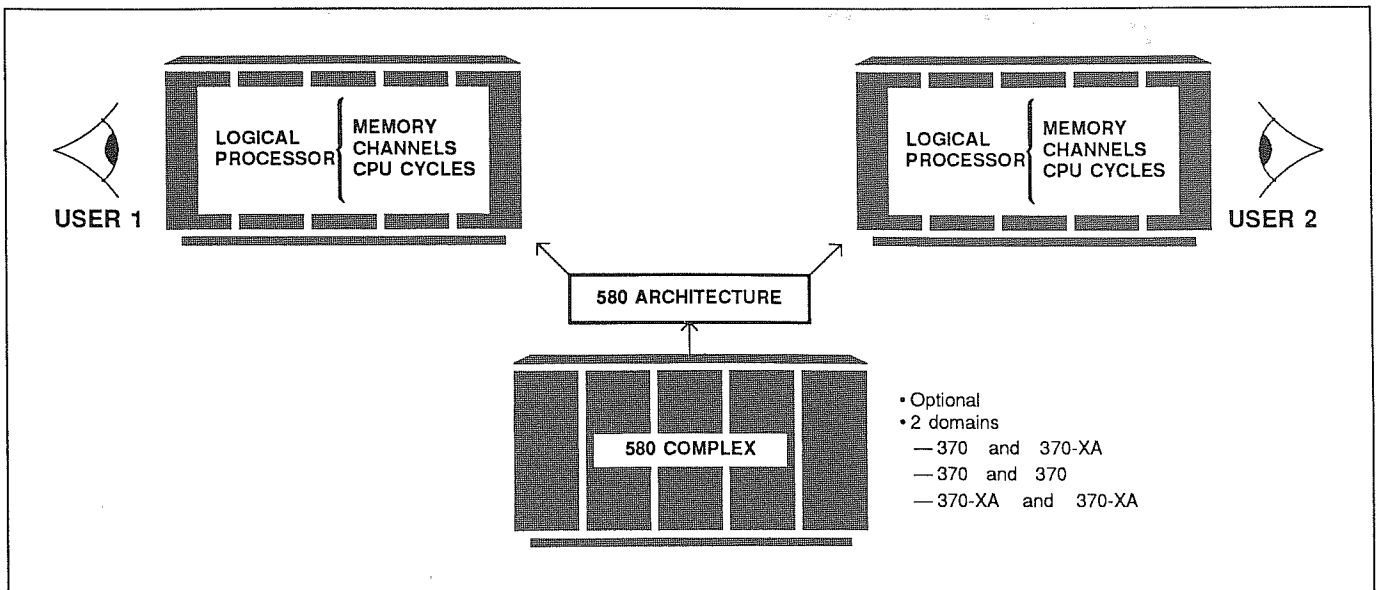


FIGURE 2 Multiple Domains

What is 580/MDF?

580/MDF extends the domain concept one level further. It allows the user to define and operate multiple domains concurrently on a single 580 processor. Each domain may be defined to operate in either S/370 or 370-XA mode, and represents a complete operating environment to the SCP.

Operator Interface

580/MDF offers an easy-to-understand, easy-to-use operator interface. All domain definition and activation is menu driven and provides clear, explicit parameters to be entered at the 580/MDF master console. Generally, domain definition is assigned to the 580 main operator console (MOC). A domain console is specified for each domain definition. Although the functions of a domain console are a subset of the functions of the master console, Amdahl recommends that a 580 remote operator console (ROC) be designated as the domain console.

The logical processor is controlled at the domain console. The operator may start and stop the logical proces-

sor, and inspect and alter registers or the program status word (PSW), while the logical processor in another domain is executing. The *stop key* on the console would, of course, stop the whole processor complex. The *stop command* at the domain console affects only the logical processor in that domain. IPL of the system control program is also performed at the domain console. Operation of an SCP, after it has been IPLed, remains unchanged in a 580/MDF environment.

Resource Allocation

Using an adjustable time-slicing technique, 580/MDF gives control of the 580 processor complex alternately to each one of the domains. In Figure 3, one domain is allocated 75 percent of the available CPU power. Each domain owns a portion of main storage and has exclusive access to a number of channels. CPU time can be dynamically redistributed either by the user or automatically by 580/MDF. Main storage is allocated to each domain in 64K-byte units and must be contiguous. Individual channels are allocated to each domain and need not be contiguous. The 580 design allows each domain to remain absolutely secure. And, since domains cannot share main storage, a software error in one domain cannot affect another domain.

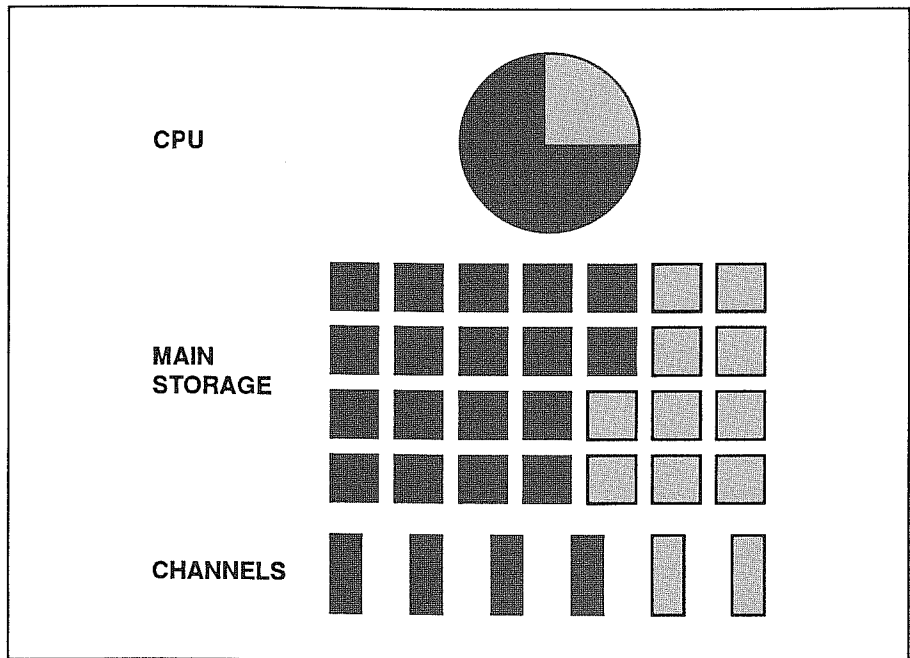


FIGURE 3 Resource Allocation

Storage Fencing

Each domain is allocated storage from the total amount of main storage installed on the processor. A domain can access only its portion of main storage. There are no existing paths that allow a program in one domain to look into another domain's storage. The address range in each domain starts at zero. The domain addresses are mapped using a technique which ensures data integrity in all domains. Whenever data are accessed in a domain, the real address is accompanied by a domain identification (ID). This ID serves as a pointer into an array of base and bound registers. If the sum of the real address and the contents of the base register is below the contents of the bound register, then access is granted. Unlike segment and page tables, the base and bound registers are in an area of main storage which is inaccessible from a domain.

Channels access data in main storage and therefore carry a domain ID to ensure that they can only read from and write to the proper domain's storage.

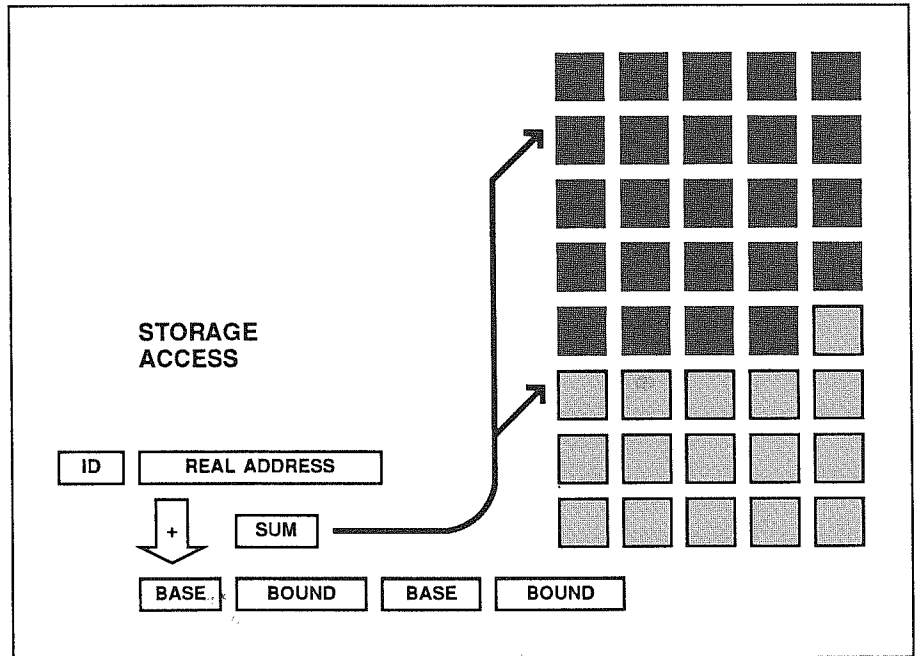


FIGURE 4 Storage Fencing

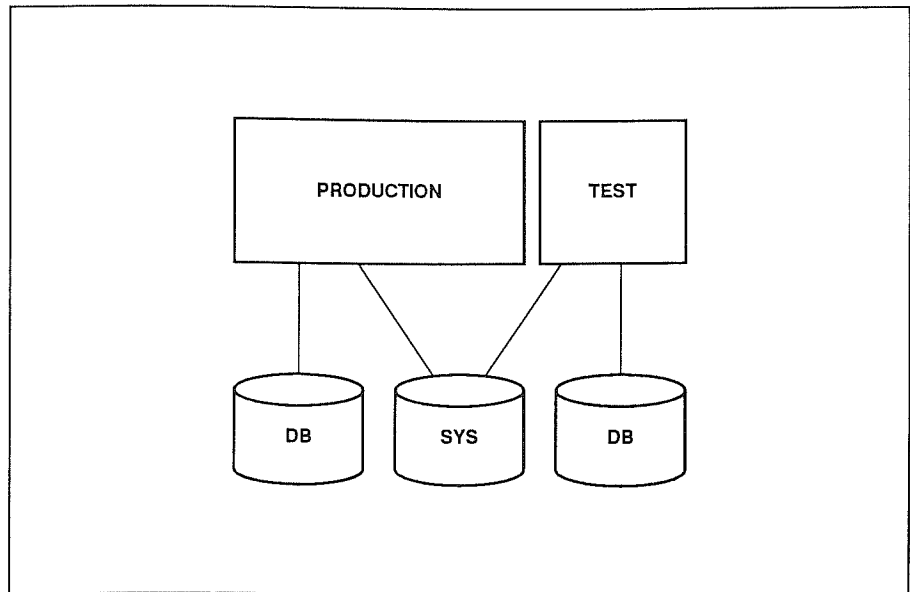


FIGURE 5 Production and Test Domains

Asynchronous Interrupts

Some events occur asynchronously to CPU operations such as I/O and external interrupts. Both are logically associated with a certain domain and they must not interrupt a different domain.

Therefore all I/O and certain external interrupts, such as timer interrupts, are associated with a domain ID. Both the I/O processor (IOP) and the memory bus controller (MBC), where the 580 interrupt routing facilities are located, are aware of which domain is currently in control. Any interrupt not matching the active domain's ID is kept pending in the hardware.

How can 580/MDF be used?

580/MDF provides the user with a flexible tool to address a variety of operational requirements such as:

- testing
- operational consolidation
- conversions
- backup strategies

Testing

580/MDF provides the user the ability to test SCPs, subsystems, and applications during prime shift without requiring standalone processors. It also provides the user with the opportunity to conduct installation verification tests on new peripheral equipment in a timely and fail-safe fashion. SCPs and their subsystems, such as JES and VTAM, are difficult to test because they are fundamental to the operation—generally, testing must be conducted during off-shift hours on a standalone processor. With 580/MDF, the user can establish test environments to conduct this critical testing during prime time. Domain isolation ensures that SCP and subsystem failures are not propagated throughout the processing complex.

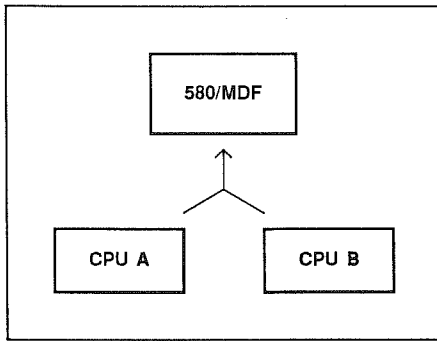


FIGURE 6 Two CPUs into One

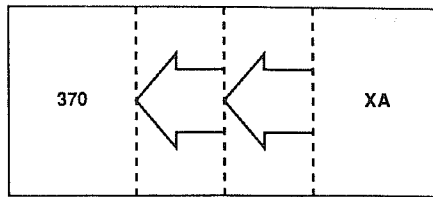


FIGURE 7 XA Conversion

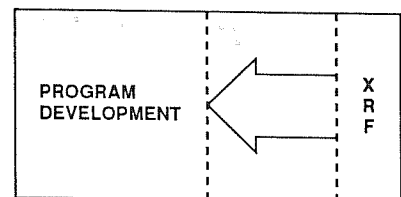


FIGURE 8 A Backup Domain

Operational Consolidation

580/MDF allows data center management to combine several different processing requirements that are now operating on multiple computers to operate on one processor. When using multiple domains, the user may experience reduced operating costs, reduced software costs, and more efficient use of data processing resources.

Conversions

Most data processing installations face the ongoing requirement of conversions. Whether they are architectural, SCP, subsystem, or application conversions, 580/MDF offers an efficient facility for supporting the conversion process while continuing to run production workloads on the same processor without compromising the integrity of the production environment.


Since the Amdahl 580 is capable of operating in either S/370 or 370/XA mode, 580/MDF allows each domain to operate in either mode without simulation. When migrating from MVS/370 to MVS/XA, for example, the XA domain may be allocated initially, e.g., 8MB of main storage, 8 channels, and 20 percent of CPU time. As the migration proceeds, and workloads shift to MVS/XA, more and more resources may be taken from the 370 domain and given to the XA domain.

Backup

An idle replica of a critical production system is operationally ideal, yet it is difficult to justify financially. While computer hardware is much more reliable today than a decade ago, networks have grown and there are many more potential single points of failure.

An important enhancement to IMS is the Extended Recovery Facility (XRF). It is intended to improve availability "by using additional resources to lessen the impact of certain events that disrupt service to the end users" (IBM announcement dated February 12, 1985). Access to multiple domains provides the user the ability to use a dormant domain to accommodate any recovery requirements. When XRF successfully recovers, the dormant domain's share of the CPU resource is automatically increased.

Functional Summary



This chapter discusses domain definition, activation, and operation. Domain definition consists of specifying domain characteristics and saving the configuration for later use. Domain definition can be done at any time prior to activation. Domain activation is the process used to enable a domain for operation. It consists of reading, or loading, the saved configuration into the System Storage Area (SSA) and activating the domain. During domain activation each domain is allocated a subset of the total resources installed on the processor. Domain operation provides the basic operator facilities as defined in the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation*.

Domain Definition

During domain definition, the user specifies the characteristics of the domain. As stated before, these characteristics include:

- architectural mode
- main storage size
- channel configurations
- operator facilities
- logical processor

The user may save the domain definition for later recall and use. Specific information about the use of MACROCODE and the command frames can be found in the *Amdahl 580 MACROCODE Reference Manual*.

Architectural Mode

To set the mode of a domain, specify either 370 or XA on the configuration attributes (CA) frame.

ACS 15.6L	CPU: process	CHK: normal	Amdahl 5860
DS3 SYS	CLK: on		
	RATE: proc		7e02 692

COMMAND OR OPTION ==> CA - CONFIGURATION ATTRIBUTES

S - SET DOMAIN CHARACTERISTICS D - DELETE A DOMAIN FACILITY
A - ADD A DOMAIN FACILITY

ARCHITECTURE MODE	==> 370	(IF S: 370 OR XA)
STORAGE SIZE	==> 32M	(IF S: ALL OR K OR M)
STORAGE LOCATION	==> 000D0000	(IF S: ANY OR HEX ADDRESS)
NUMBER OF LP'S	==> 1	(IF S)
CONSOLE ADDRESS	==> DS3A	(IF S: NONE OR DISPLAY STATION)
TARGET CPU PERCENTAGE	==> 001	(IF S: 1-100)
MAXIMUM CPU PERCENTAGE	==> 100	(IF S: 1-100)
DOMAIN FACILITY	==>	(IF A OR D)

DOMAIN FACILITIES: EK - EXTENDED KEY PF - PAGE FAULT
* = ASSIGNED SQ - SUBCHAN QUEUE

MASTER DS3A CSG370D1 0 078D0000 0014641E 370

FIGURE 9 Configuration Attributes Frame

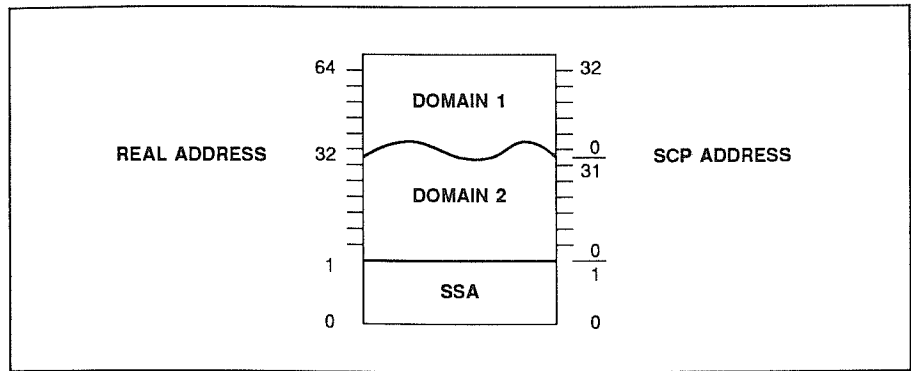


FIGURE 10 Main Storage Allocation

Main Storage Size

Main storage is allocated to a domain by specifying the domain's main storage size on the CA frame. MACROCODE requires 768K bytes of main storage with or without 580/MDF installed. (For detailed information on 580 main storage, refer to the *580 MACROCODE Reference Manual*.)

Domain Console Address

The configuration I/O (CI) frame specifies the logical address of the 580 console to be used as the domain console. The domain console must be a MOC or a ROC. It is used for all domain specific control functions such as START, STOP, and LOAD (IPL).

```

ACS 15.6L          CPU: process   CHK: normal          Arndahl 5860
DS3 SYS           CLK: on          RATE: proc
                                                    7802
                                                    692
-----
IN - INDEX FOR MACROCODE RELEASE 14X-020
COMMAND OR OPTION ==> █
IN - INDEX                CL - CONSOLE LOG
OP - OPERATOR FUNCTIONS  SL - SYSTEM LOG
OE - OPERATOR EXTENDED   PF - PROGRAM FUNCTION KEYS
AD - ALTER/DISPLAY       FC - FUNCTION LIST CONTROL
DE - DOMAIN DEBUGGING    DD - DOMAIN I/O DISPLAY
DI - DOMAIN I/O          SD - SYSTEM DEVICES
CC - CONFIGURATION CONTROL SI - SYSTEM I/O
CA - CONFIGURATION ATTRIBUTES SR - SYSTEM RESOURCES
CD - CONFIGURATION I/O DISPLAY SS - SYSTEM SCHEDULING
CI - CONFIGURATION I/O    MI - MISCELLANEOUS
TO DISPLAY A FRAME, ENTER 2 LETTER FRAME NAME ON COMMAND/OPTION LINE

NON-FRAME COMMANDS:
FORWARD          SETLP          WAITCONS
BACKWARD         SETPF          SWAPIOGDS
                 SETNAME

MASTER_DS3A_OSG370D1_0_078D0000_0014641E          370

```

FIGURE 11 Index Frame

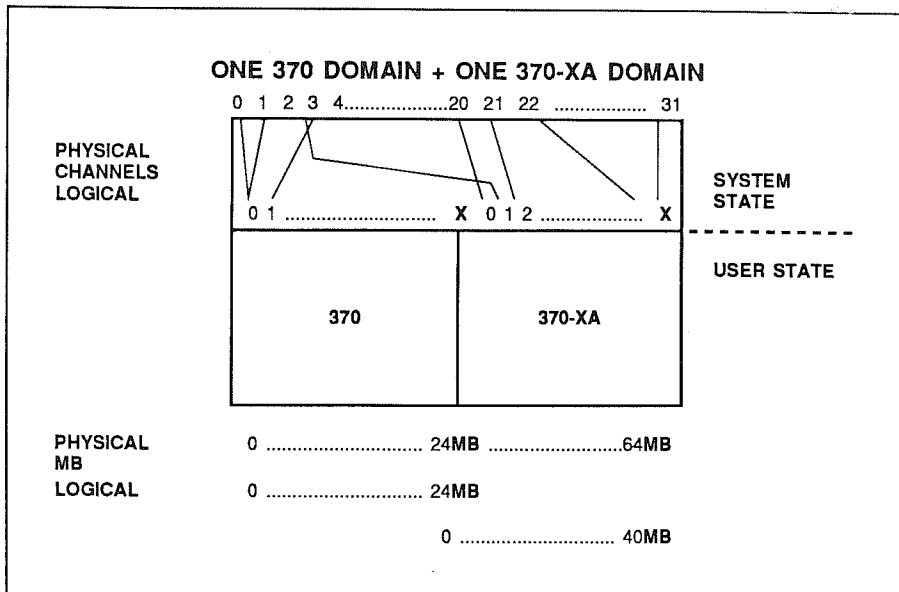


FIGURE 12 Channel Configuration

Channel Allocation

580 system channels are allocated to a domain, and their logical addresses are established through information supplied on the CI frame or, if one or more 370-XA domains are to be activated, in the input output control data set (IOCDs). Devices can be shared in the same way they are shared between separate physical processors.

CPU Time Allocation

580/MDF's flexible time-slicing technique is also used to make CPU time available to each domain. For each domain, the operator specifies two parameters: the target value (this is the percentage of CPU time the domain should receive) and the maximum value (MAX-value). The MAX-value establishes an upper limit on the percentage of CPU time the domain may use. In figure 13, a target value of 80 percent is specified for the production domain and a target value of 20 percent for the test domain.

If the test domain does not use its allotted CPU time, the production domain is allowed to use all available CPU time. In this case, the production domain has its MAX-value specified at 100 percent. On the other hand, if the production domain is less active, then the test domain is limited to 50 percent of the available CPU time. Such a setup would guarantee that important users, even if they are temporarily idle, always have sufficient CPU time allotted to access the system.

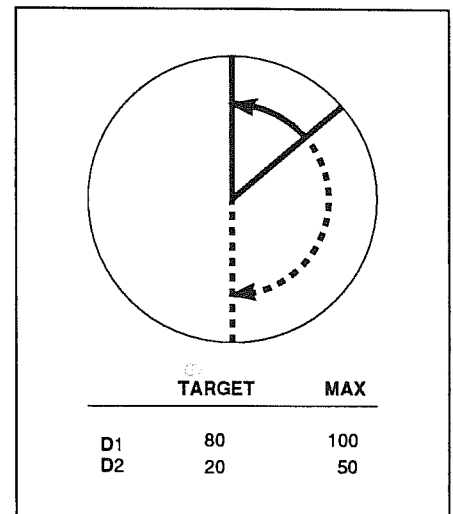


FIGURE 13 CPU Target and MAX-Values

The CPU resource allocation objectives are specified on the system scheduling (SS) frame. Since response time interacts with throughput time, the user may control overall performance through the scheduling parameter. This parameter determines the frequency of each domain receiving control (for a full description, refer to "System Programming Considerations" in this document). The user can select the value which best meets the installation's requirements. The value can be dynamically changed.

```

ACS 15.6L          CPU: process   CHK: normal          Amdahl 5860
DS3 SYS           CLK: on          RATE: proc          7e02
                                                           692
-----
COMMAND OR OPTION ==>  SS - SYSTEM SCHEDULING
S - SET DOMAIN CPU PERCENTAGES          P - SET SCHEDULING PARAMETER
TARGET CPU PERCENTAGE ==> 050          (IF S: 1-100)
MAXIMUM CPU PERCENTAGE ==> 100        (IF S: 1-100)
SCHEDULING PARAMETER ==> 3           (IF P: 1-5)
          DOMAIN          CPU-UTILIZATION
          NAME            TARG  MAX  NORVM
          OSGXADO         50   100  50
          OSG370D1        50   100  50
-----
MASTER_DS3A_OSG370D1_0_078D0000_0014641E          370

```

FIGURE 14 System Scheduling Frame

Saving the Configuration

The configuration created during domain definition can be saved for later recall and use. The configuration is saved by selecting the configuration control (CC) frame, naming the domain, and selecting the "S" option.

```

ACS 15.6L          GPU: process   CHK: normal          Amdahl 5860
DS3 SYS           CLK: on         RATE: proc          7e02
                                                           692
-----
COMMAND OR OPTION ==> | CC - CONFIGURATION CONTROL
L - LOCK DOMAIN      U - UNLOCK DOMAIN
M - SAVE DOMAIN      S - SAVE CONFIGURATION
R - READ CONFIGURATION E - ERASE CONFIGURATION
A - ACTIVATE CONFIGURATION D - DEACTIVATE DOMAIN

NAME                ==>
SIDE (FOR MP, A OR B) ==>
CURRENT ACS CONFIG: CONF2.0A      (F, R, S, E, OR M)
ACS CONFIG READ: CONF2.03

ACTIVE DOMAIN (* = LOCKED)      SAVED CONFIGURATIONS
#OSGXAD0  OSG370D1      ADAM      AFD      AUGTEST      CA
D          DOXA      D1370      EREP
GARY      IOCPGEN      IVP      LPTEST
MVXADM0   MVXADM1   MVXAMDF   OSGMDFX
OSGMDF3   OSGXAD0   OSGXAD1   OSG370D0
OSG370D1  OSG3701   QAXAD0    QAXAD1
QA370D0   QA370D1   RASTEST   SQAEREP
VMA       VMPESIOF

MASTER_DS3A_OSG370D1_0_078D0000_00146420          370

```

FIGURE 15 Configuration Control Frame

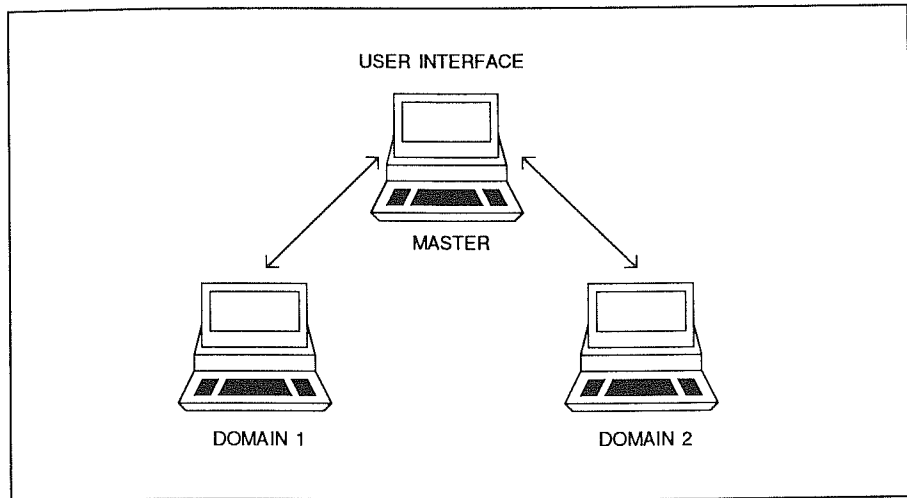


FIGURE 16 Domain Consoles

Domain Activation

Domain activation is the process by which resources are allocated to the domain according to the domain configuration specifications. The domain configuration is read and loaded into the system storage area (SSA) by selecting the CC frame, entering the name of the domain or configuration, and using the “R” option. The domain may then be activated by specifying the “A” option on the CC frame.

Modifying the Configuration

The domain configuration may be modified during the definition, activation, and operation phases. The CPU resource allocation objectives can be changed on any domain without interrupting operation.

Channels may be dynamically reallocated from one domain to another provided both domains are operating in the same architectural mode. It is the user’s responsibility to ensure that the channels affected are varied offline and that they are inactive before they are reallocated.

Reconfiguration of domain storage, or changing the architectural mode of a domain, requires deactivation of the domain, redefinition of the storage size or architectural mode, reactivation of the domain, and re-IPLing the SCPs.

Domain Operation

The primary interface between the user and 580/MDF is the domain console.

In case of a console failure, the system automatically initiates a console switch. The SCP is IPLed from a domain console and operation proceeds in the usual manner from any available SCP console.

Planning Information

System Control Program Support

580/MDF supports the following SCP environments:

- MVS/SP Version 1, Release 3 (MVS/370)
- MVS/SP Version 2, Release 1 (MVS/XA)
- VM/SP High Performance Option (VM/SP HPO) Releases 3.2 and 3.4

For support of later versions and releases of these SCPs, please refer to the current Amdahl Software Support announcement.

SCP Consoles

Any terminal which is supported by the SCP may be used as an SCP master console. It is also possible to use a 580 MOC or ROC as an SCP console, but this option may be chosen for no more than one active domain.

Trace and Debug

The trace facilities provided by the SCPs are available for use with 580/MDF.

Debugging facilities provided by the 580 Series processors are available at the domain console or the 580/MDF master console. All of these facilities affect only one domain. Available facilities include:

- ALTER/DISPLAY of domain storage
- ALTER/DISPLAY of program status word
- ALTER/DISPLAY of control registers
- ALTER/DISPLAY of general purpose registers
- ALTER/DISPLAY of floating point registers
- set address compare
- START/STOP
- instruction step
- store status

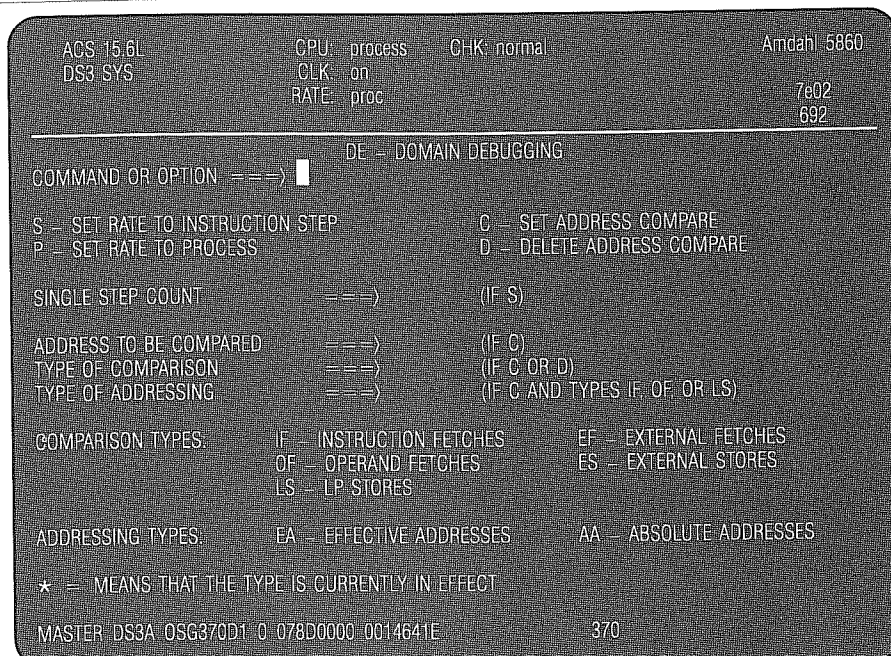


FIGURE 17 Domain Debugging Frame

System Programming Considerations

Performance Aspects

580/MDF has flexible tuning parameters to give the user maximum control over the performance of each domain. The user can explicitly define the amount of CPU time that can be used by each domain by specifying the same percentages as the target and MAX-values established during domain definition (see "CPU Time Allocation" section of this document for more information).

Performance of a domain in a 580/MDF environment is expected to be near that experienced in a single domain environment with the same resources. When a domain is given control, it has exclusive control of the processor and the resources allocated to it. Given the same resources, multiple domains typically provide at least 95 percent of the performance experienced with 580/MDF installed. Performance experienced when

operating only one domain with 580/MDF installed is equivalent to that experienced without 580/MDF installed.

The time-slicing technique is used to allocate the CPU resource to the domains. The scheduling parameter determines the duration of the time slice. This parameter influences the number of domain switches. The scheduling parameter is specified on the SS frame as an integer between 1 and 5 (default = 3). When a higher number is specified, the frequency of each domain receiving control is raised, favoring response-time-oriented work. When a lower number is specified, each domain stays in control for a longer period of time, and unnecessary domain switches are avoided. Thus, the user can balance performance of the system to achieve optimum throughput and responsiveness.

Performance, throughput, and transaction rates depend on configuration, applications, operating characteristics, and the CPU resource objectives specified during domain definition. Individual user environments should be carefully evaluated before making any performance estimates.

Timing Considerations

All timing facilities described in the *System/370 Principles of Operations* and the *System/370 Extended Architecture Principles of Operations* are available in each domain. Both the time-of-day (TOD) clock and the clock comparator are based on elapsed (wallclock) time. Both time facilities are provided for each domain independently. The TOD clock continues to run when the domain is not in control. Therefore, the TOD clock should be used with caution when monitoring an individual domain.

There is a CPU timer facility for each domain. This timer is only active when the domain is in control. In an MVS system, all TCB and SRB times, as well as the accumulated wait times in RMF, are collected by the dispatcher using the CPU timer. All TCB, SRB, and Wait times shown in the RMF reports as seen by that domain are correct.

All percentages reported by a monitor in one domain relate to the proportion of the CPU time that domain has been using—not to the whole processor. When two domains report 70 percent and 80 percent CPU busy respectively, this does not mean that the Amdahl 580 processor was 150 percent busy. To calculate the percent of the time the total CPU was busy:

$$\text{Total CPU busy} = \frac{\text{elapsed time} - (\text{domain1 wait time} + \text{domain2 wait time})}{\text{elapsed time}}$$

I/O Statistics

All I/O counts are correct. Once an I/O operation is started, it executes asynchronously and it may end when the initiating domain is not in control. In this case the interrupt is kept pending until the domain is in control again. The time between these events (Start I/O and interrupt) is reported as the device response time. Even if the interrupt is held pending, the I/O operation completes in its usual amount of time. However, in 370-mode, I/O completion is detected only when the interrupt is taken, so the reported device response time

may seem to be higher. In XA-mode, all I/O statistics are collected in the I/O processor, regardless of the domain in control. The time the MVS/XA system spends in interrupt handling is not included in the device response time, as is the case when operating in MVS/370 mode.

Sharing Data Sets

All of the provisions that are required to ensure data integrity when sharing data sets among multiple processors must also be taken when sharing data sets among multiple domains. These provisions include that the devices to be shared are properly declared in the system generation.

CPU ID

The CPU ID is returned by the STIDP instruction. It contains information identifying the domain number. Refer to the Appendix for complete information on the layout and content of this data area.

IOCDS Considerations

Only one IOCDS is necessary when operating multiple 370-XA domains. The IOCDS should include devices that are currently installed as well as those planned for the complex. This reduces the frequency of input output control program (IOCP) generations. During domain activation, the configuration described in the IOCDS is used as a resource pool for allocation to the domains.

EREP Reports

History data on systemwide errors are centrally maintained in the console subsystem and stored in the MOC. In multiprocessor systems, each MOC stores the data pertinent to that side of the processor complex to which the MOC is attached. The Amdahl-supplied Environmental Recording, Editing, and Printing Program (AMDEREP) obtains these data by accessing an OSI device (for a full description refer to the *Amdahl 580 Computing Systems Computer Operator's Manual*). Therefore, AMDEREP should be run in the domain that has the OSI devices attached to it.

Inter-Domain Communication

Inter-domain communication supports the same facilities currently available for connecting two physical processors. These include: shared DASD, channel-to-channel adapters, and teleprocessing links.

Feature Support

580/ACCELERATOR

The 580/ACCELERATOR feature provides the capability to increase the performance level of an Amdahl 5840 or 5850 processor. The 580/ACCELERATOR feature is supported by 580/MDF. All domains are accelerated equally when the 580/ACCELERATOR feature is active.

System Activity Monitor (SAM)

SAM is a standard feature on all 580 Series processors. It collects and graphically displays system utilization data. It is supported with 580/MDF installed and provides information for individual domains as well as the entire processor.

Hardware Monitor Attachment Feature (HMAF)

HMAF provides for attachment of customer-owned hardware performance monitoring equipment to a 580 Series processor. HMAF is supported with 580/MDF installed and provides information for individual domains as well as the entire processor.

High Speed Floating Point (HSFP) Feature

The HSFP feature provides additional computing capacity for applications which use the floating point arithmetic instruction set. The HSFP feature is supported with 580/MDF installed.

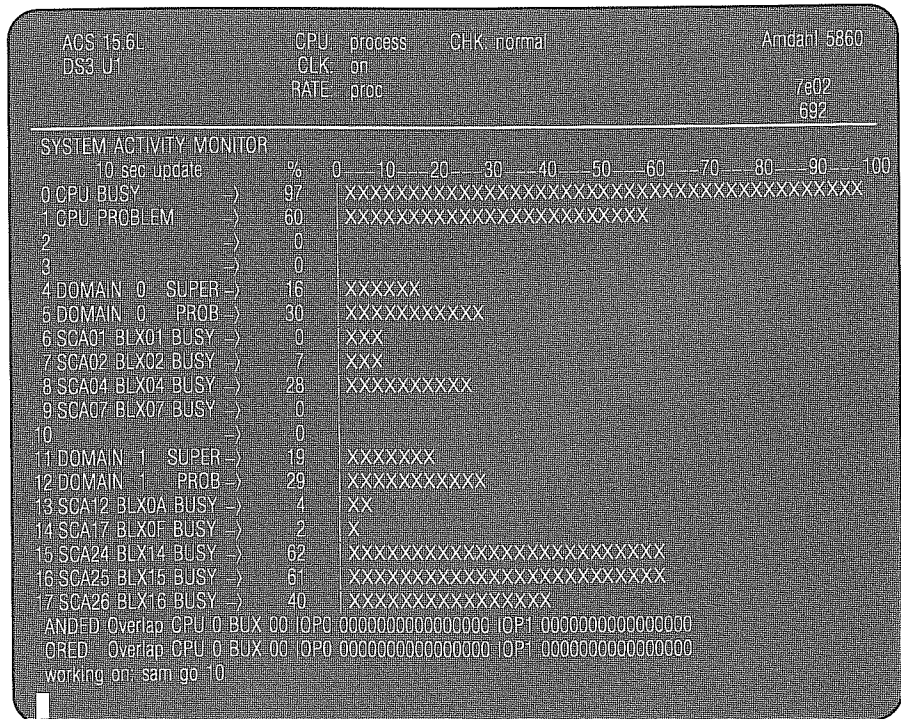



FIGURE 18 System Activity Monitor



The CPU ID that is stored for an individual domain is a double word containing five fields of information. The first byte of the first word is the environment/version code. Bits 0 through 3 are used to indicate the operating environment of the processor and the presence of features. Bits 4 through 7 contain the encoded model number. Bits 8 through 11 pertain to multiprocessors and domains. Bits 12 through 15 provide the CPU ID from the first two digits of the processor complex's serial number. Bits 16 through 31 are the low order four digits of the serial number. The second word contains two constants: the machine series (X'0580'), bits 32 through 47, and the Machine Check Extended Logout length (X'0000'), bits 48 through 63.

The contents of the double word returned by the STIDP instruction are outlined below.

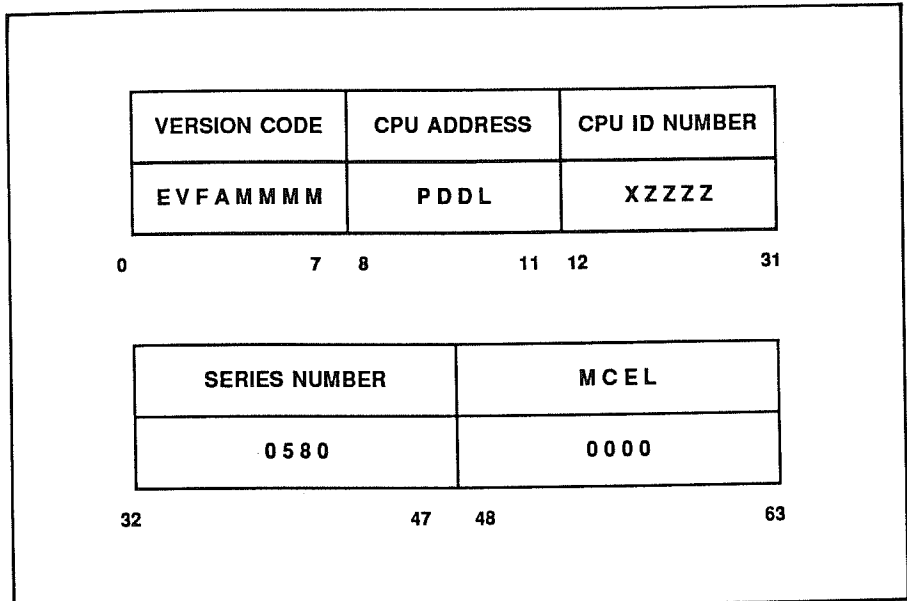


FIGURE 19 Results of STDP Instruction

LEGEND FOR FIGURE 19 (ABOVE):

Version Code (EVFA)

Bit 0	(E) — B'1'	MACROCODE installed
Bit 1	(V) — B'1'	Running under VM
Bit 2	(F) — B'1'	HSFP feature installed
Bit 3	(A) — B'1'	580/ACCELERATOR feature installed

Model Number of Complex (MMMM)

Bits 4–7		
B'0101'	— X'5'	5840
B'0110'	— X'6'	5850
B'0010'	— X'2'	5860
B'0111'	— X'7'	5867
B'1000'	— X'8'	5868
B'0011'	— X'3'	5870
B'0100'	— X'4'	5880

CPU Address (PDDL)

Bit 8	(P) — B'1'	Side B of partitioned multiprocessor
Bits 9–10	(DD)	Domain number
	— B'00'	Domain 0
	— B'01'	Domain 1
Bit 11	(L) —	Logical processor number
	— B'0'	LP 0
	— B'1'	LP 1

CPU Identification Number (XZZZZ)

Bits 12–15	(X) — X'0'	High order digit of the processor complex serial number.
Bits 16–31	(ZZZZ) — X'0000'	The low order 4 digits of the processor complex serial number.

