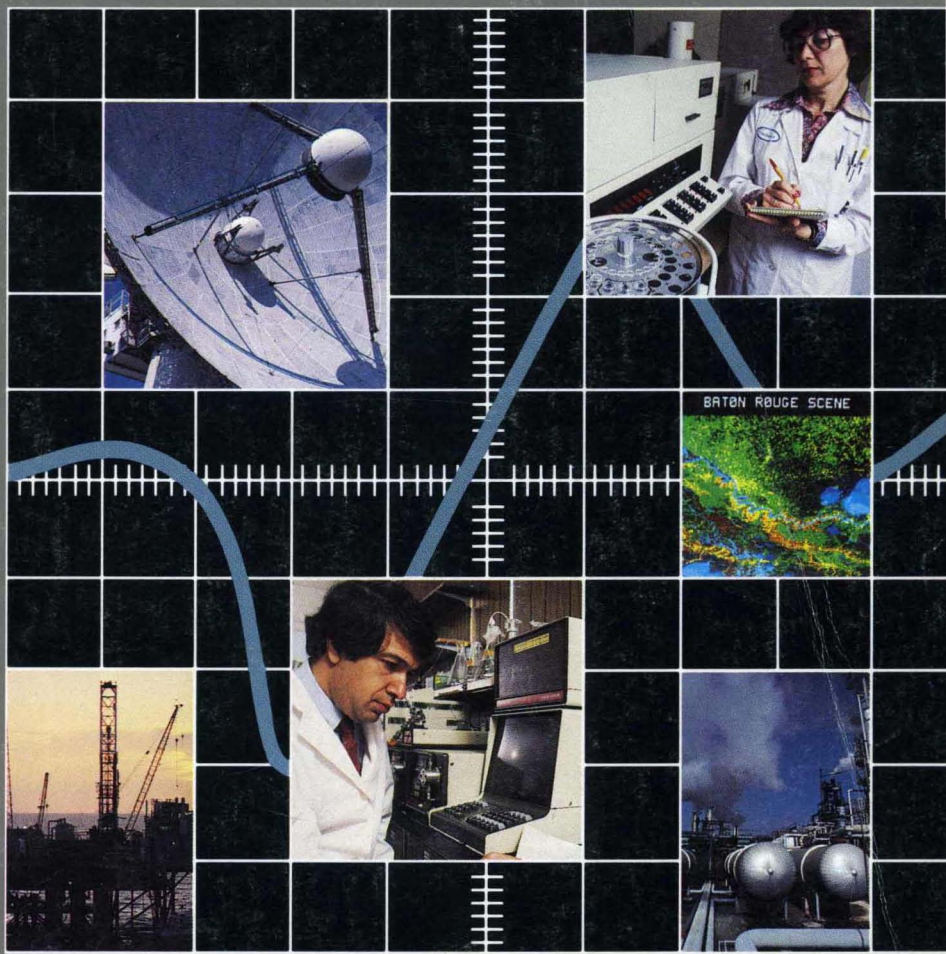
Data Conversion PRODUCTS CATALOG

ANALOGIC

1985



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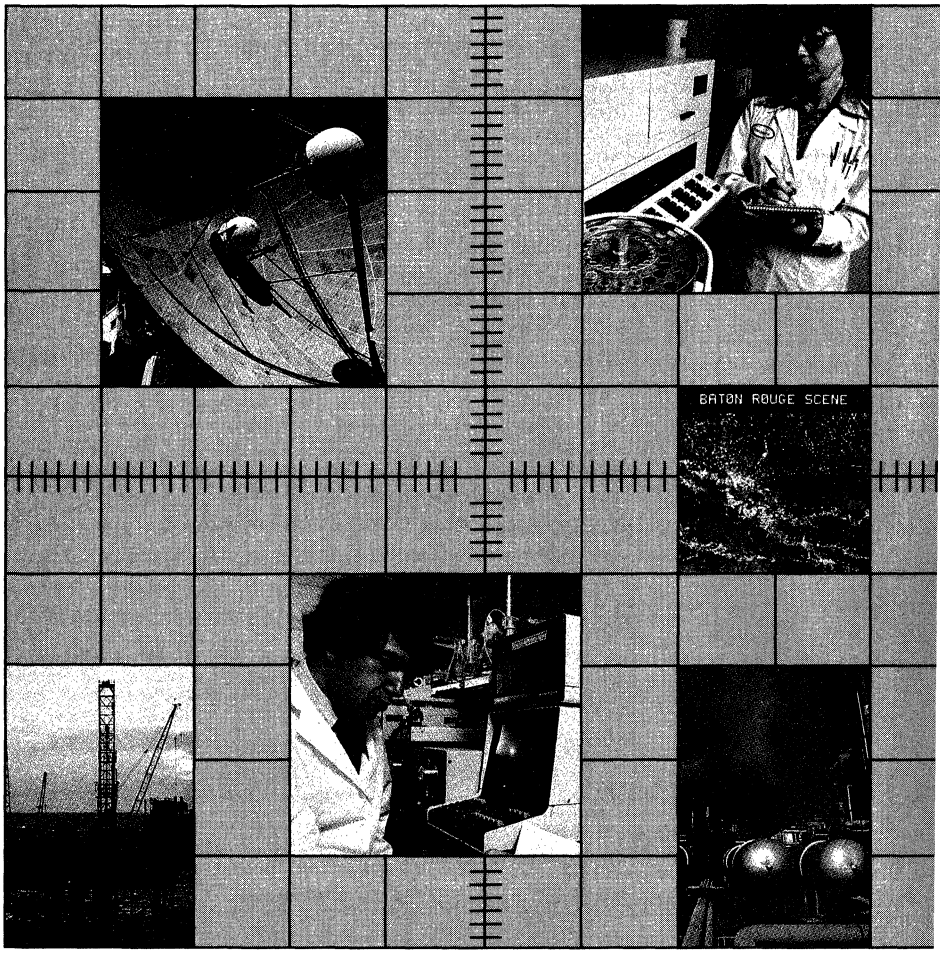

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SECTION 1

General Information

INTRODUCTION

The purpose of this Catalog is to provide you, the system designer, with an easy to use reference on data conversion technology as well as a selection guide for Analogic's Data Conversion Products. Complete technical data is provided for all of our standard product line. Similar products are grouped according to function, i.e. all amplifiers are in one section, all sample-and-hold amplifiers are in another section, A/D converters in another, etc. Selection guides are provided to assist in the selection of the appropriate product with respect to the most critical parameters for a given application. If information on a specific product is required, an alphanumeric index of all products is also provided.

Special modifications to standard products are easily accomplished; please consult the factory for details.

PLACING AN ORDER

Orders may be placed via mail, telephone, or Telex with any Regional Sales Office, sales representative, or our headquarters in Wakefield, Massachusetts. Our offices are listed on the inside back cover of the catalog. When placing your order, please provide complete information, including Analogic Model Number with all option designations, your Part Number (if required), product description or name, quantity required, and ship-to and bill-to addresses

DATA SHEETS/LITERATURE

Product data sheets on new products not found in this Catalog, or containing more recent revisions, are available from your local sales representative or Analogic sales office.

PRICING AND TERMS

Pricing on Analogic data conversion products is available from any of our Sales Offices, Subsidiaries, International Distributors and Sales Representatives, or direct from the factory.

All prices are FOB Wakefield, Massachusetts, USA, in US dollars unless otherwise noted. Applicable federal, state, and local taxes are extra. Terms are net 30 days.

QUOTATIONS

Price quotations made by Analogic or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time the order is placed.

RETURNS AND WARRANTY SERVICE

When returning products for any reason, it is necessary to contact Analogic, prior to shipping, for authorization and shipping instructions. In the U.S., contact our Customer Service Department at the factory in Wakefield, MA at (617) 246-0300 or 1-800-237-2200. In other countries, contact your nearest Analogic sales office or representative.

APPLICATIONS ASSISTANCE

If you need technical assistance regarding any aspect of the standard Data Conversion Products offered in this catalog, or, if you require a modification to a standard product to meet your requirements, or, if you would like to discuss your application and the use of Analogic's extensive expertise in the signal conditioning and data conversion areas to design and manufacture a subsystem or component to meet your specific requirements, please call our Applications Engineering Group at (617) 246-0300 Ext. 2368 or 2168.

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SECTION 2

Amplifiers

SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
Signal Conditioning	Differential Input	High Isolation Voltage	MP227A	2-17
	Single-Ended Input	Low Noise Low Bandwidth	MP221	2-11
DAC Deglitching Professional Audio	Low Harmonic Distortion	Single-Channel	AH201-1	2-5
		Dual-Channel	AH201-2	2-5

GLOSSARY OF TERMS

AMPLIFIERS

FULL POWER BANDWIDTH The highest frequency at which an amplifier, loaded to maximum rated output, will track a sinusoidal signal large enough to drive the output to its rated full-scale value at peak input. The nominal relationship between full power bandwidth and the slew rate is:

$$f = \text{Slew Rate} / 2\pi e_{fs}$$

where: f = Full Power Bandwidth e

e_{fs} = rated full scale output.

GAIN ACCURACY The maximum amount that the actual voltage gain deviates from the nominal value expressed as a percentage of that nominal value. This takes into account the effects of temperature variations, power supply variations, and drift with time, if significant.

ISOLATION AMPLIFIER A circuit that typically accepts a low level signal, often in the presence of a high level common mode voltage, from a transducer, and amplifies it to produce a clean, accurate output signal. Figure 1 shows a simplified functional diagram.

OVERLOAD RECOVERY TIME The time required for the circuit to return to linear operation, within a stated tolerance, after removal of a sustained input that was large enough to drive the circuit into complete saturation (i.e., a condition in which further increase in the input did not significantly increase the output).

SETTLING TIME The maximum time required for the output to track the input to within the specified accuracy after a full range step change.

SLEW RATE The maximum slew rate is the fastest rate of change of the output of the amplifier. This is normally obtained by a step input signal that drives the output from end to end of its range.

SMALL SIGNAL BANDWIDTH The maximum small signal bandwidth is the highest frequency at which an amplifier will track, to within 3 db of the low frequency response, a sinusoidal signal having an amplitude below that for which the slew rate limitation is significant.

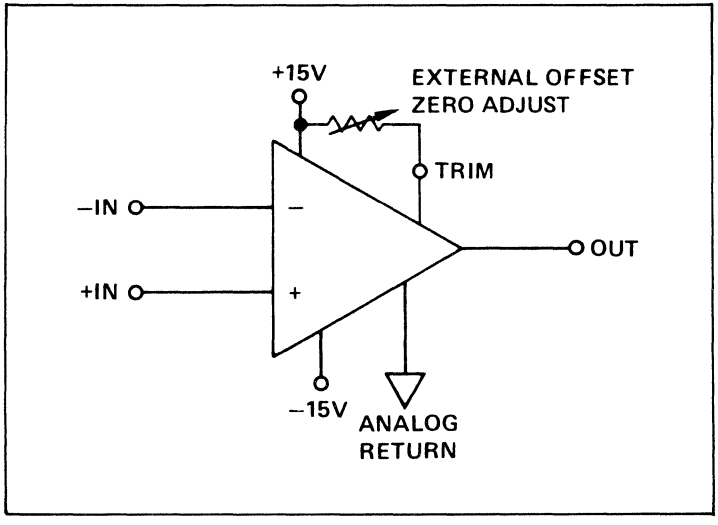
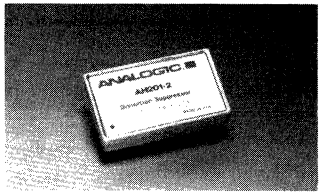


Figure 1. Simplified Functional Diagram.



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AH201

Distortion Suppressor

Description

The AH201 is a low-cost distortion suppressor, used to reduce the total distortion generated by unmatched bit switching in the decoder digital-to-analog (D/A) converter section of a digital audio or communications system. The AH201 features exceptionally low noise (−115 dB), and a time-constant limited response that eliminates slew-rate limiting problems, yet is short enough (3.4 μs) to ensure no significant attenuation of signals up to 20 kHz. These features, combined with a typical feedthrough rejection of 100 dB, provide a significant improvement in the performance of any digital audio decoder. Optimum performance is obtained by using the AH201 in combination with a true 16-bit D/A converter such as the ANALOGIC MP1926A.

All D/A converters generate some dynamic distortion each time they perform a conversion. This distortion results from code-dependent switching glitches or from slew-rate limiting of the D/A's output amplifier. Conventional sample-and-hold (S/H) amplifiers used at the D/A output do not suppress this distortion adequately for high performance, professional audio applications due to slew-rate limiting when changing modes. The AH201, however, can reduce the distortion from these nonlinearities by up to 40 dB or more, depending upon the decoder with which it is used. (Refer to Figure 2 for example).

The AH201 is a direct result of ANALOGIC's considerable experience in digital audio including professional audio recording, studio links, and telecommunications. Designed for ease of interconnection and maximum flexibility, the distortion suppressor requires a single control line per channel to provide all necessary control. The AH201 accepts a ± 10V input and can drive up to ± 16 mA into a 600-ohm load. The distortion suppressor is offered as a single or dual device, packaged in a 24-pin, double-width DIP, fully shielded metal can. Its small size, low noise, low cost and exceptional performance qualify the AH201 for use in any digital-audio system.

Features

- **Low Harmonic Distortion** 0.003% (−90 dB), maximum
- **Ultra-low Noise** — −115 dB
- **Single-Channel (AH201-1) or Dual-Channel (AH201-2) Versions**
- **Time-Constant Limited Response** Eliminates distortion due to slew-rate limiting
- **Small Size** — 24-pin DIP
- **Single Control Line/Channel**
- **Optimized for D/A Deglitching**

Applications

- **Professional Digital Recording Systems**
- **Satellite Downlinks**
- **Video Disc Audio**
- **Signal-Processing Systems**
- **Compact-Disc Systems**

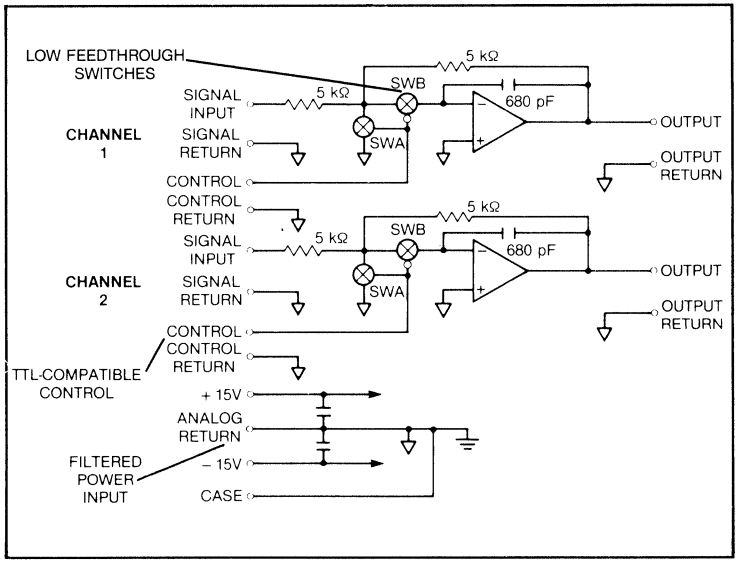


Figure 1. AH201 -2 Functional Block Diagram

SPECIFICATIONS

(All Specifications are guaranteed at 25°C unless otherwise noted)

INPUT

Input Voltage Range:
± 10V

Input Voltage Without Damage:
± 15V

Input Impedance:
5 kohms, ± 2%

OUTPUT

Output Voltage:
± 10V

Load:
600 ohms, minimum

Protection:
Short circuit to ground

Output Impedance @ dc:
0.1 ohm, maximum

TRANSFER CHARACTERISTICS

Frequency Response dc to 20 kHz:
0 dB, ± 0.3 dB maximum

Time Constant[1]:
3.4 μs, nominal

Settling Time:
Determined by time constant

Bandwidth (SAMPLE Mode):
46 kHz (Time-constant limited)

Gain[2]:
− 1, ± 0.02, maximum

ACCURACY (AT 25°C)

Integral Nonlinearity:
± 0.002% FSR, maximum

Noise (20 kHz Bandwidth)[3]:
10 μV rms, maximum

Total Distortion:
Down by at least 90 dB for frequencies up to 20 kHz (including harmonic distortion)

Peak Line Harmonic Distortion:
Down by at least 96 dB for frequencies up to 20 kHz

Output Offset Voltage (SAMPLE Mode)[2]:
± 12 mV, maximum

Feedthrough (HOLD Mode)[5]:
Down by 96 dB minimum, 100 dB typical for ± 10V sinewave up to 20 kHz

Power Supply Sensitivity Gain:
20 ppm FSR/V, maximum

Offset:
20 μV/V, maximum

Channel-to-Channel Crosstalk[4]:
Down by at least 100 dB

DIGITAL CONTROL INPUT

Logic Levels:
TTL compatible

SAMPLE Mode (Output Connected to Input):
Logic 0; 0V to 0.4V, maximum

HOLD Mode (Output Disconnected from Input):
Logic 1; + 2.4V, minimum to + 5V

POWER REQUIREMENTS (Exclusive of load)

+ 15V, ± 3%:
10 mA, maximum
(single channel, − 1)
20 mA, maximum
(dual channel, − 2)

− 15V, ± 3%:
10 mA, maximum
(single channel, − 1)
20 mA, maximum
(dual channel, − 2)

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range:
0°C to 70°C

Storage Temperature Range:
− 25°C to + 85°C

Relative Humidity:
0 to 85%, noncondensing to 40°C

Dimensions (Single or Dual Channel)
1.305" x 0.775" x 0.3", maximum
(20.07 x 33.14 x 7.62 mm)
24-pin double-width DIP

Pin Spacing:
0.6" x 0.1"

Packaging:
Metal can

Shielding:
Electromagnetic—6 sides
Electrostatic—6 sides

Note 1: Other time constants also available. Consult factory.

Note 2: From 0°C to + 70°C.

Note 3: Measured at 50% duty cycle. 10 μV rms equals − 115 dB referenced to rms full scale.

Note 4: Measured on one channel with its input grounded, with a ± 10V sinewave of frequency up to 20 kHz applied to the input of the other channel; applies to dual-channel AH201-2 version only.

Note 5: Feedthrough specification given is for standard 3.4 μs time constant. Feedthrough performance will be different for time constants other than 3.4 μs. Please consult factory.

Theory of Operation

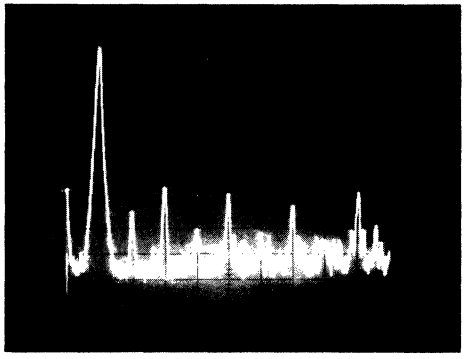
The operation of a single-channel AH201-1 is described. Each channel of the AH202-2 operates in a similar manner.

The AH201-1 consists of an inverting amplifier, a hold capacitor, and a pair of specially selected analog switches controlled by an external mode command. As shown in Figure 3, the mode is switched to minimize the effects of DAC nonlinearities on the output of the recovery system.

When the D/A output has settled to the value corresponding to the digital code at its input, the AH201 is commanded to the SAMPLE mode; shunt switch "A" opens and series switch "B" closes, connecting the settled D/A output to the output of the AH201. In this mode, the AH201's output response is exponential with the 3.4-μs time constant.

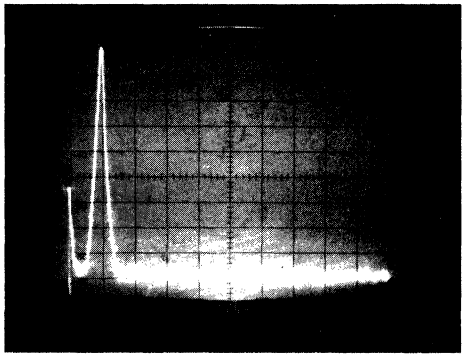
The AH201 remains in the SAMPLE mode until just prior to the time when the D/A is updated to a new value, when it is commanded into the HOLD mode. The switch positions reverse, shunting the changing D/A output signal to ground. The previous output level, now stored on the capacitor, is maintained as the output of the AH201. The 96-dB, minimum, feedthrough rejection of the AH201 effectively isolates the output from the transients and other nonlinear settling characteristics of the D/A converter.

When the distortion suppressor is switched between its two modes, it passes signals up to 20 kHz without introducing significant distortion. For example, with the AH201 switching at 50 kHz, the peak line distortion for a full amplitude sinewave at 20 kHz is 96 dB down with respect to the full-scale level.



D/A OUTPUT

Scale: 2 kHz per division
10 dB per division
100-Hz bandwidth
Fundamental: 2 kHz, 7V rms



AH201 OUTPUT

Figure 2. System Improvement with AH201

USING THE AH201

Grounding

The power return, analog input and output returns, and control return are all tied together internally and to the case. For convenience in pc-board layout, return pins for each function are located adjacent to the corresponding signal pins. To avoid ground loops, no connection should be made to the case ground pins 1, 12, and 15.

When using the AH201-1 single-channel version, it is necessary to connect pins 2 to 3 and 5 to 4. In addition, no connection should be made to pin 20. In both the single-channel AH201-1 and dual-channel AH201-2 versions, no connection should be made to pins 6, 7, 13, 14, 18, 19, or the case ground pins 1, 12, and 15.

Control

One control line is provided for each channel of the AH201. A logic 0 selects the SAMPLE mode, connecting the output to the input; a logic 1 selects the HOLD mode, isolates the output from the input. Please refer to Figure 3 for typical timing information.

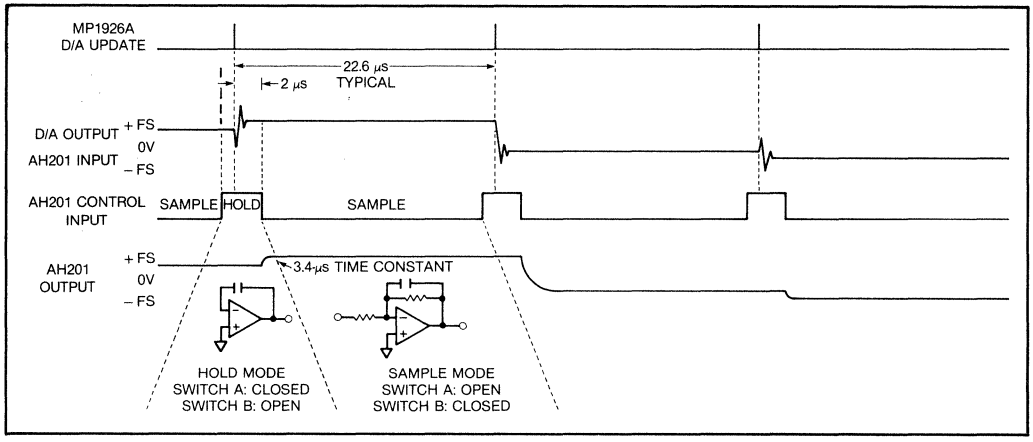


Figure 3. Typical Timing for a Single Channel System (44.1 kHz Sample Rate)

A time-constant limited response affects all input-voltage changes in the same proportion as long as the settling time allowed is constant. For this example, the on (SAMPLE) time of 17 μs (5 time constants) results in a gain error of 0.1 dB. If required, this gain reduction can be corrected by the system gain adjustment.

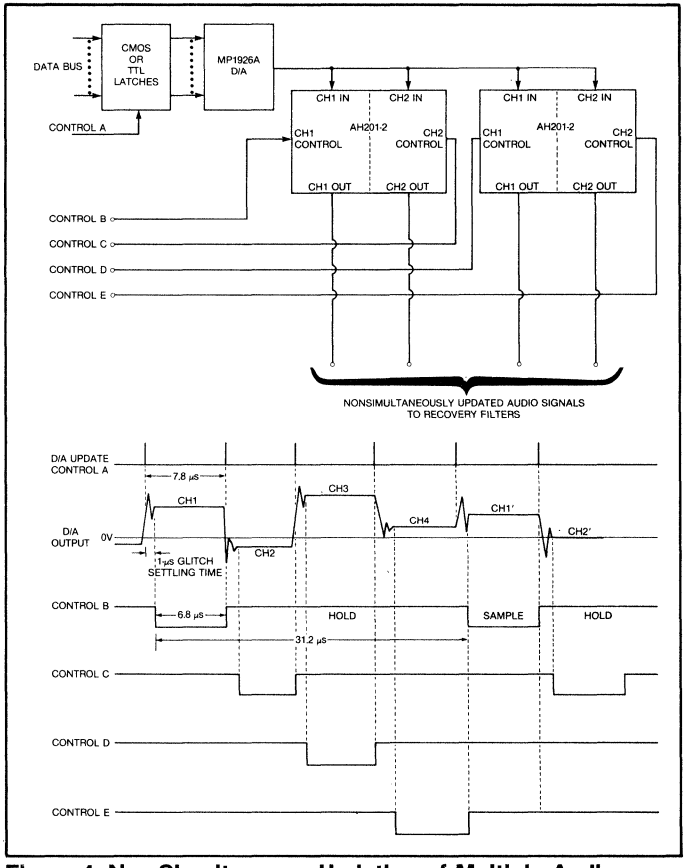
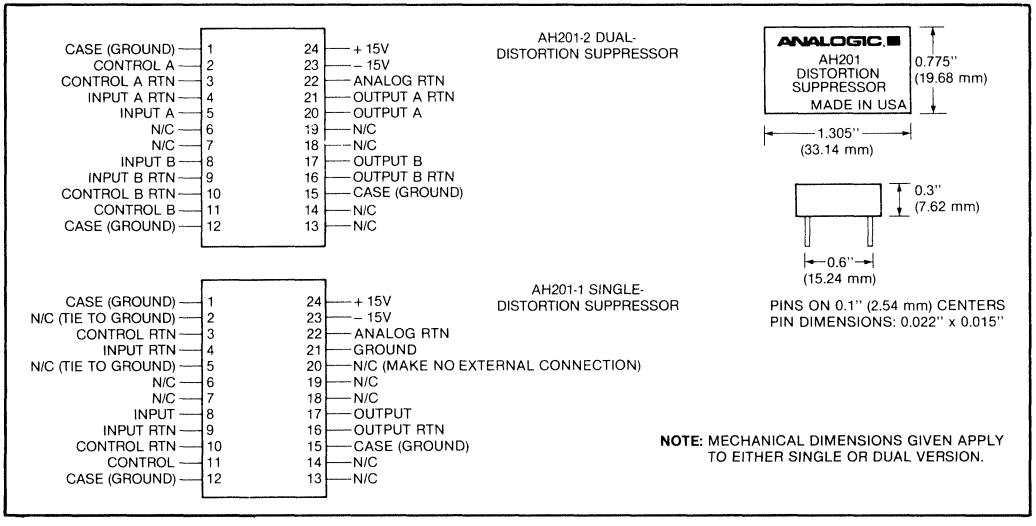


Figure 4. Non-Simultaneous Updating of Multiple Audio Channels (15 kHz bandwidth per channel, 16-bit resolution, 32 kHz sampling rate).

TYPICAL APPLICATIONS

Satellite Downlink Program Distribution

Multiple channels may be sequentially updated using one high-speed, high-accuracy D/A converter (such as the ANALOGIC MP1926A 16-bit Sign/Magnitude D/A) and multiple AH201s (−1 or −2). For example, a satellite ground station used in a program-channel distribution system would be required to update multiple audio outputs, but not necessarily simultaneously. Figure 4 illustrates one possible implementation using a single D/A converter to sequentially update four, 15-kHz bandwidth, audio channels. A nominal 32-kHz sample rate per channel is assumed. This means that the D/A converter must update four channels every 31.2 μs or one channel every 7.8 μs, which is well within the settling capability of the MP1926A. The AH201 circuit in each channel is simply turned on (SAMPLE mode) for the last 6.8 μs of the corresponding MP1926A update period.



Mechanical & Pinout

ORDERING GUIDE

Single-Channel Distortion Suppressor...Specify **AH201-1**
Dual-Channel Distortion Suppressor...Specify **AH201-2**

Stereo Program Distribution

Figure 5 illustrates the highest performance yet lowest cost method available for simultaneously updating stereo analog outputs, at rates up to 55 kHz from 16-bit resolution data (98 dB dynamic range). Conventional implementation requires two D/A converters plus digital double buffering to achieve simultaneous updating. The ANALOGIC MP1926A, with a voltage settling time of only 5 μs to 1 LSB for a 5V step, allows both channels to be updated from a single D/A converter within the 18 μs available. The only buffering required for simultaneous updating can be provided by an additonal AH201-2 configured as shown in Figure 5.

The timing diagram shows that the AH201 (Z1 in the Figure) samples the D/A output during a time slot assigned to Channel 1. It then holds this new Channel 1 level while the D/A output settles to a new Channel 2 value. As a result of the AH201's 96 dB feedthrough rejection in the HOLD mode, the Channel 2 information signal has a negligible effect on Channel 1. When the inputs to the AH201-2 (Z2 in the Figure) have settled to the new levels, both channels are switched into the SAMPLE mode simultaneously, causing both channel outputs to be updated. It should be noted that the two channels will be 180 degrees out of phase due to the double inversion in Channel 1. To bring both channels in-phase, an AH201-2 can be substituted for the AH201-1 (Z1), and the control for its second channel can be hardwired in the SAMPLE mode, as shown in the inset of Figure 4; alternatively, the sign of the data for one of the channels can be inverted prior to being presented to the DAC inputs.

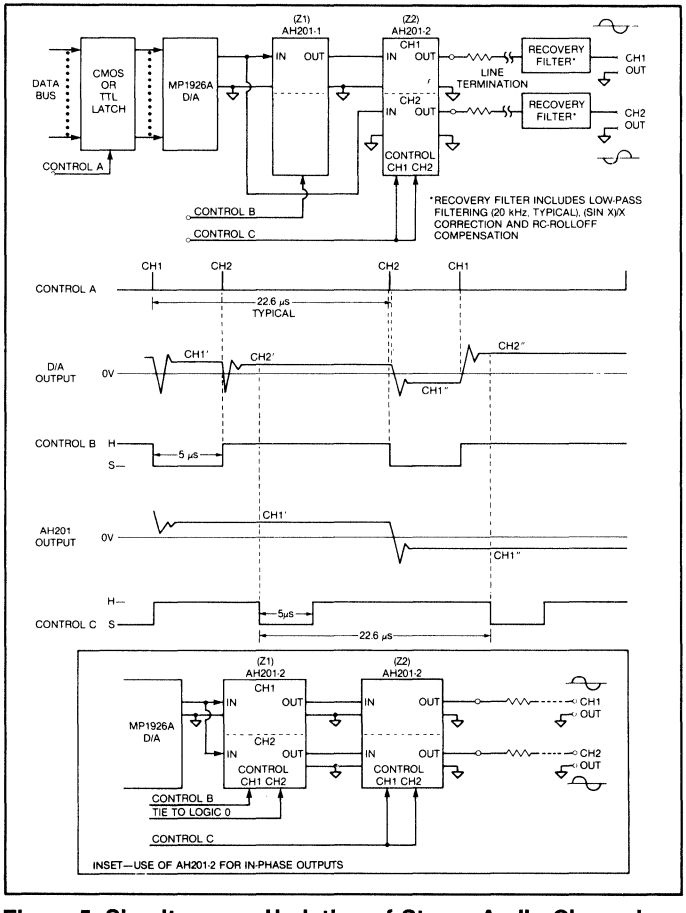
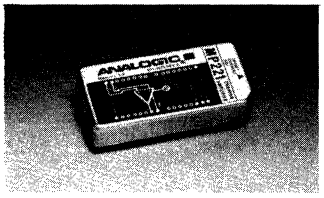


Figure 5. Simultaneous Updating of Stereo Audio Channels.



ANALOGIC®

MP221

Low Noise, Low Level Chopper Amplifier

Description

The Analogic MP221 Chopper Amplifier provides unprecedented low level signal amplification for instrument and industrial applications in the microvolt-to-millivolt region. The MP221 design generates less than 0.1 μV p-p noise from dc to 1 Hz, less than 0.3 μV p-p from dc to 10 Hz, less than 1 μV p-p from dc to 100 Hz, and less than 3 pA noise current from dc to 1 Hz. These superior specifications include flicker noise and Johnson noise components as well (See Figure 1). Moreover, the MP221 is virtually drift free with a maximum voltage drift of 0.05 μV/°C, a maximum current drift of 2 pA/°C, and a long term drift of 1 μV/month or 2 μV/year.

Implementation

Optimized for non-inverting signal applications, the MP221 amplifier is normally soldered to a user's PC board. Gold-plated pins enhance solderability and conductivity. Amplifier gain is determined by selecting and connecting two resistors and a capacitor external to the MP221 as shown in Figure 1. Both resistors must possess an operational stability of 10 ppm/°C or better to maintain the performance capability inherent in the MP221 advanced design. Thermal effects at the amplifier input terminals can be minimized by using low thermal solder and utilizing the installation precautions customary for low level signal circuits.

Current offset of the MP221 can be trimmed to zero by adjusting a built-in potentiometer. An external offset voltage adjustment may be incorprated as shown in Figure 4. When the MP221 is used in the non-inverting mode, the offset voltage can be buffered from the input by using a voltage follower to avoid interaction with the gain components.

Features

- **Low Noise**
  <0.1 μV p-p
  <3 pA p-p
- **Low Drift**
  <0.03 μV/°C
  <2 pA/°C
- **Gain Linearity**
  within ±0.002%
- **High Input Impedance**
  $10^9\Omega$
- **Short-Circuit Protected**

Applications

- **Instrumentation, Load Cells, Thermocouples, Strain Gauges**
- **Measurement Preamplifiers**
- **Low Level Buffers**

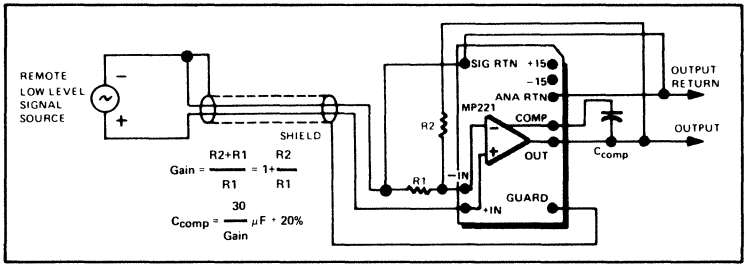


Figure 1. MP221 Non-Inverting Pin Connections and Gain Resistor/Capacitor Calculations.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)
(Note: All performance at dc power of ±15V, gain = 100, R_1 = 100Ω, R_2 = 10 kΩ, and C_{COMP} = 0.27 μF.)

ANALOG INPUT

Noise Current (0 to 1 Hz)
3 pA p-p

Offset Voltage
±2 μV typ., ±5 μV max. (ext. trim, Figure 4)

Bias Current (Non-Inverting)
±20 pA max. (trimmable to zero, Figure 3)

Bias Current (Inverting Mode)
±2 nA max.

Input Impedance
10^9Ω

Common Mode Voltage
±0.5V

Commom Mode Rejection Ratio
140 dB

Maximum Input Without Damage
±20V

ANALOG OUTPUT

Voltage Range
±10V

Current
±3 mA

Impedance at dc
±0.01Ω

Load
3 kΩ in parallel with 0.1 μF max.

Short-Circuit Protection
Output short-circuit protected ground

GAIN CHARACTERISTICS

Linearity
±0.002%

Gain Range
10 to 10,000*

Open Loop Gain
160 dB

NOISE BANDWIDTH

dc to 1Hz
<0.1 μV p-p

dc to 10Hz
<0.3 μV p-p

dc to 100 Hz
<1 μV p-p

STABILITY

Tempco of Offset Voltage
0.03 μV/°C typ., 0.05 μV/°C max.

Tempco of Bias Current
2 pA/°C max.

Power Supply Sensitivity
0.01 μV/1% power supply change

Warmup Drift
To within 2 μV of final value in 2 minutes

Long Term Drift
1 μV/month, 2 μV/year

Thermal Step Offset Recovery
5 minutes for 25°C step

Offset Resulting from ac Input
1 μV for 4 mV p-p 60 Hz

Overlaod Recovery Time
200 ms to within 2 μV for 10 x FSR input

FREQUENCY RESPONSE

Bandwidth
−3 dB at 100 Hz

Settling Time to 0.002% FS
(50 + 8Vsw)ms; Vsw = Output voltage swing

Slew Rate
130 V/s

POWER REQUIREMENTS

±15V
2.5 mA plus load current

ENVIRONMENTAL & MECHANICAL

OPERATING TEMPERATURE
0°C to +70°C

Non-Operating Temperature
−25°C to +85°C

Relative Humidity
0 to 95%, non-condensing

Shielding Protection
RFI 6 sides; EMI 5 sides

Dimensions
2 x 1 x 0.39" Modupac™ (50.8 x 25.4 x 9.91 mm)

*Note: At Gain <20, inputs must be < ±0.5V.

Application Information

The Analogic MP221 Low Level Chopper Amplifier is designed to perform in the microvolt-to-millivolt signal range for instrument and industrial applications. This amplifier has been optimized for operation in the non-inverting mode so that gains from 10 to 10,000 can be achieved with minimum loading of the signal source. Because of its unique features, which include low noise, low thermal offset drift, and low bias current, the MP221 is ideally suited for use as a preamplifier with load cells, thermocouples, and other low level transducers. However, to obtain a level of performance consistent with the superior specifications of the MP221, some usage guidelines must be exercised. This application note provides several recommended techniques for operating the MP221 with low level input signals.

Amplifier Operation

The MP221 amplifier has a chopper input that effectively samples the voltage difference between its plus (+) and minus (−) inputs. A circuit employing this amplifier should be considered a "sampled data" system, and proper attention must be paid to the generated errors. The most important error is unwanted signals or noise appearing at the amplifier output, which can be attributed to aliasing or intermodulation distortion. These effects can be reduced by filtering the amplifier input and by choosing an optimum chopper frequency. Since most systems are subject to noise pickup at the line frequency and its harmonics, the MP221 has been set to sample at 925 Hz, which is 25 Hz removed from the nearest 60 Hz or 50 Hz harmonic. These harmonic components at the amplifier input are translated to 25 Hz at the output. Because most A/D converters can respond at this speed, post filtering is often necessary.

Low Noise Techniques

For low noise operation, it is recommended that low-pass filtering be used before and after the amplifier. (See Figure 2). Because most active-type filters generate noise within the amplifier bandwidth, the pre-filter should be composed of passive components. Noise injected after the amplifier is less critical, and for that reason, a three-pole active-type low pass filter can be used as a post-filter. The component values shown in Figure 2 are effective for 2 Hz filtering.

Another consideration is to limit the bandwidth of the MP221 to that required in the system. Because the output noise generated by the amplifier varies as the square root of the bandwidth, there is 10 times more noise at a 100 Hz bandwidth than at 1.0 Hz bandwidth. The output capacitor (C_{comp}) shown in Figure 2 sets the bandwidth for a given gain. The C_{comp}

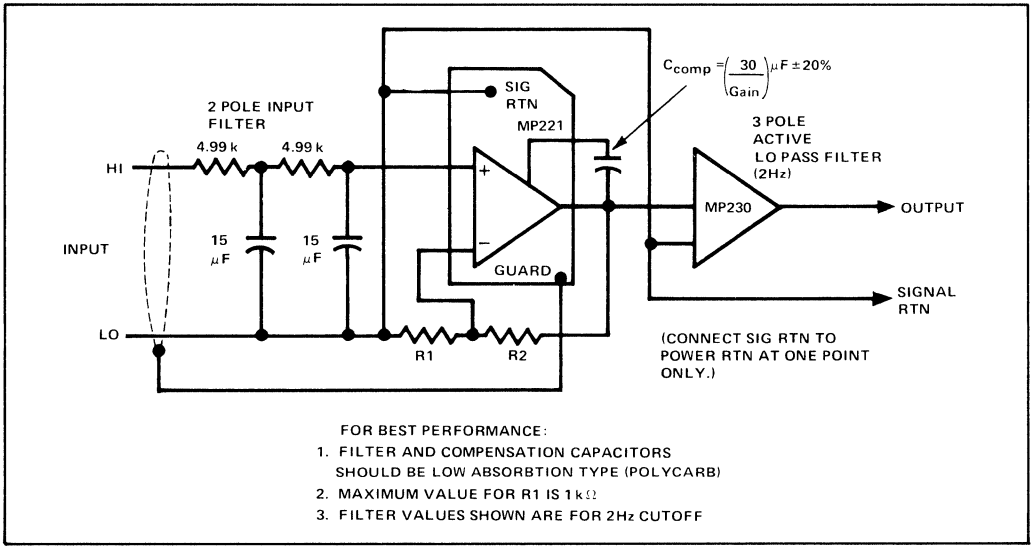


Figure 2. Recommended Filtering of MP221.

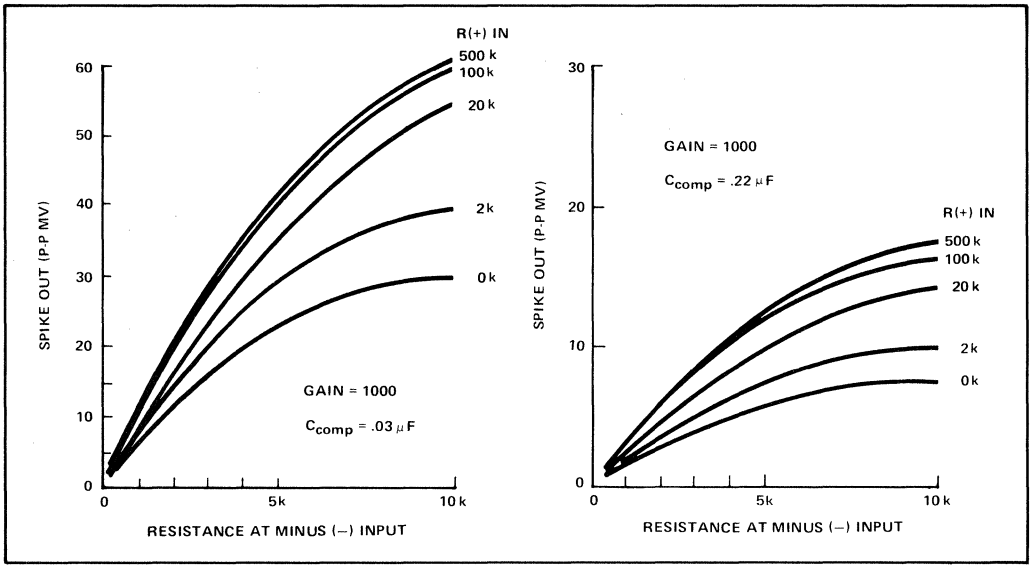


Figure 3. Switching Spikes vs. Input Source Impedance.

recommended value of (30/Gain) μF is for a 100 Hz bandwidth and bandwidth decreases proportionally as C_{comp} is increased. For example, at a gain of 100, a 3 μF C_{comp} sets a bandwidth of 10 Hz. The parameters of the pre- and post-filters should also be set to obtain only the needed bandwidth. An additional source of noise appearing at the amplifier output is due to internal chopper switching transients. The magnitude of this noise depends upon the input resistances, primarily that between the minus (–) terminal and common. Figure 3 illustrates this dependence and also shows the reduction of this noise as C_{comp} is increased. Reduction of this noise is another reason why a post-filter is recommended.

For the stated reasons and because of the unavoidable Johnson noise effects, the resistors associated with the MP221 amplifier should be as low in magnitude as practical (a limitation being the current available to generate the output voltage levels). A maximum of 1 kΩ from the minus (–) input to ground is recommended. Because carbon composition and some film resistors generate noise in excess of Johnson noise, only stable wirewound resistors or known low noise film resistors should be used.

The signal input wiring should be shielded to reduce pickup; a shielded-twisted pair is recommended.

The amplifier power supply inputs are decoupled internally, so that in most applications, external capacitors are not required.

Thermal Offset Techniques

If noise could be reduced to that of the source (theoretical minimum), thermal offset voltages would still appear when amplifying microvolt input signals. These thermal offsets are caused by joining dissimilar metals and by existing temperature gradients across the input circuit. For example, a thermocouple of copper and lead/tin solder can generate an offset voltage of 0.3 μV for 0.1°C temperature difference between the metals. Since this temperature gradient varies with time, the thermal offset appears similar to low frequency noise or "wandering". The techniques used to minimize these thermal offsets are: (1) keep signal high and low input connections physically close to reduce temperature differences, (2) shield connections from all convection air currents (breezes), (3) heat sink the input connections tightly, and (4) only join similar metals (copper) using low thermal solder (cadmium/tin). When operating at the microvolt (or below) level, all four techniques may be required. If all copper connections are made at the MP221 input terminals using low thermal solder and the amplifier is wrapped in polyurethane foam, then the total thermal offset wandering should be less than 0.1 μV.

Bias Current Adjustment

Another low level error is caused by bias current flowing through the external source resistance, thereby generating offset voltages. These voltages can be balanced externally but they are temperature dependent. An adjustment is provided on the MP221 so that the bias current at either input can be set to zero. However, since the currents at the inputs are not equal, only one input can be compensated, leaving a residual bias current at the other input.

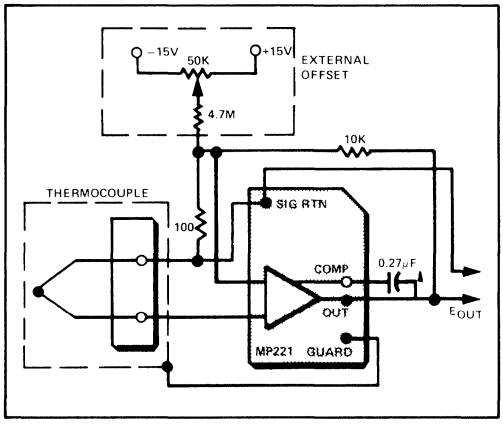


Figure 4. MP221 Amplification of the Thermocouple Low Level Output and Illustrating External Offset.

When an MP221 is used in the recommended positive gain configuration, the positive input bias current can be adjusted to zero with the negative input bias current remaining less than ±2 nA. If the resistor connected to the negative input is less than 1 kΩ (R1, Figure 2), the offset voltage due to the ±2 nA should be only ±2 μV (referred to the input). This value is much less than the offset voltage specification of the amplifier (±5 μV maximum).

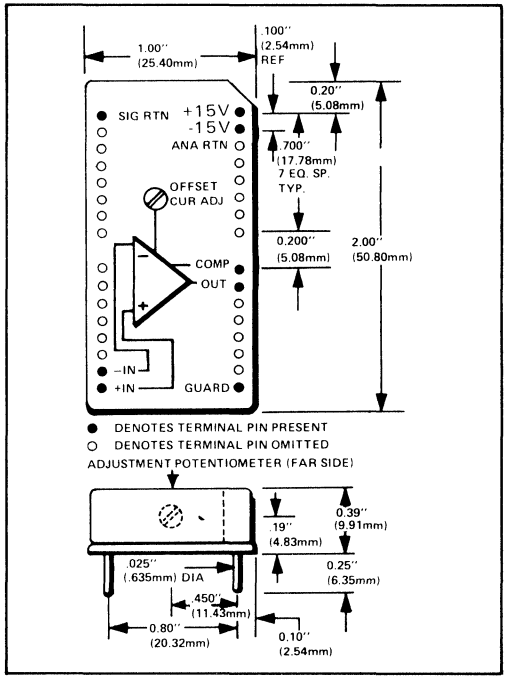


Figure 6. Mechanical & Pinout.

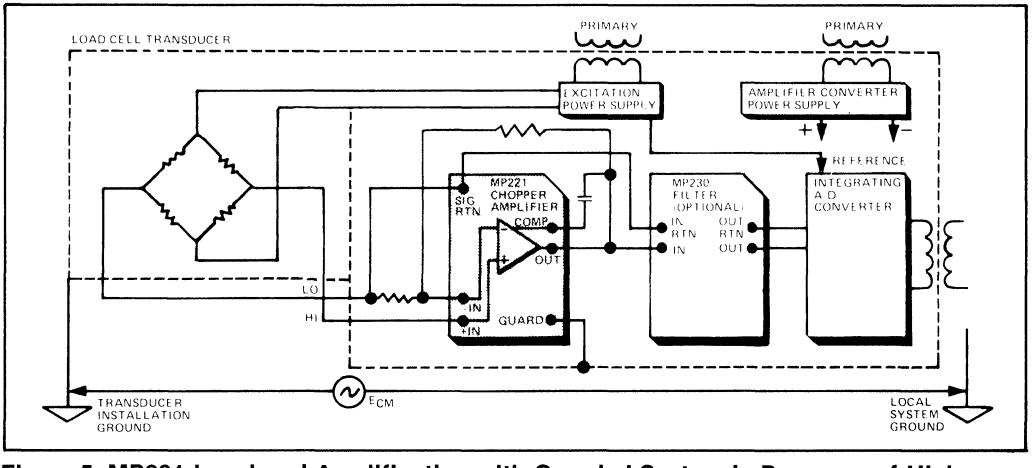
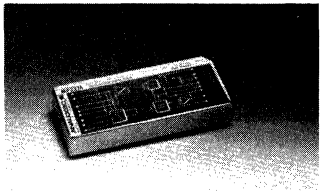


Figure 5. MP221 Low Level Amplification with Guarded System in Presence of High Common Mode Voltage.

ORDERING GUIDE

Low Noise, Low Level Chopper Amplifier

Specify **MP221.**



ANALOGIC®

MP227A

Isolation Amplifier

Description

The Analogic **MP227A** is a precision isolation amplifier that provides an unparalleled combination of linearity, stability, isolation, and very low cost. It is designed primarily to replace relays and filter elements in multichannel data acquisition systems. However, its unique features make it attractive wherever low-level, low frequency signals must be amplified in the presence of severe common mode interference.

The **MP227A** offers user-selectable gains from 10 to 1000, input full-scale voltage ranges from ± 10 mV to ± 1V, 3-pole (60 dB/decade) filtering from 5 Hz, extremely good linearity, superb common-mode rejection, and very low drift. All parameters are commensurate with A/D conversion at levels up to 13 bits.

The **MP227A** includes an internal power oscillator and isolated supply so that no external drivers are needed. The isolated power (± 4V nominal) can be used for open thermocouple indication or offsetting strain gauge inputs.

Features

- **High Common Mode Rejection** 170 dB
- **Excellent Linearity** 0.0075%
- **Selectable Input Range** ± 10 mV FS to ± 1V FS
- **Low Noise** <0.5 μV rms
- **Low Drift** 3.0 μV RTI per month
- **Built-in 3-pole Filtering**
- **Built-in Oscillator/Driver**

Applications

- **Thermocouple Temperature Measurement**
- **Weighing Systems**
- **Strain Gauge Measurements**
- **Remote Data Acquisition and Precision Telemetry Systems**
- **Microvolt and Millivolt Level Measurements**
- **Replacement for Classical Instrumentation Amplifier**

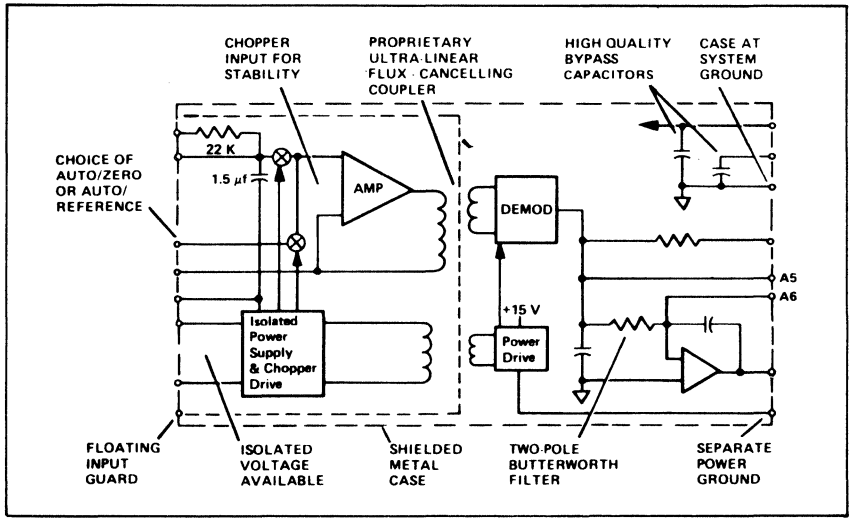


Figure 1. MP227A Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Gain Range
10 to 1000, non-inverting, resistor programmable; optimized for gains of 50 to 500

Non-linearity
±0.0075% FSR maximum at G = 50 to 500;
±0.01% FSR maximum at G = 1000;
±0.05% FSR maximum at G = 10

Input Amplifier Type
Isolated Chopper

Linear Differential Input Voltage Range
±10 mV to ±1V full scale

Maximum Safe Differential Input Voltage
16V rms continuous, without damage

Common Mode Isolation Voltage
1000 Vdc, 750V rms, maximum

Common Mode Rejection Ratio
At dc, with G = 100 and 1000, 166 dB minimum; 1 kΩ source unbalance
At 60 Hz, with G = 100 and 1000, 176 dB typical, 160 dB minimum; 1 kΩ source unbalance

Common Mode Impedance
10,000 MΩ / / 80 pF

Differential Input Impedance
At dc, 12 MΩ; at ac, low-pass filter of 22 kΩ and 1.5 μF

Overload Input Impedance
22 kΩ, at 50/60 Hz

Input Bias Current
0.5 nA typical, 3.0 nA maximum; bias current increases if open input indicator circuit is used

Offset Voltage
At G = 10, ±1 mV typical, ±5 mV maximum; at G = 1000, ±150 μV maximum; all referred to input (RTI); offset voltage may be determined by interpolation for other gain values

Voltage Noise (0.01 to 5 Hz)
At G = 10, 1.5 μV rms maximum; at G = 100 and 1000, 0.5 μV rms maximum; RTI

Bandwidth (See Note 1)
dc to 5 Hz nominal; 6 dB down at 5 Hz

Overall Filtering (See Note 2)
3-pole, 60 dB/decade roll-off (−60 dB at 50 Hz)

Input Filter
1-pole RC, 3 dB cut-off at 5 Hz

Output Filter
2-pole Butterworth, 3 dB cut-off at 5 Hz

ANALOG OUTPUT

Voltage Range
±10V full scale

Output Impedance at dc
0.1Ω

Maximum Load
±5 mA and 500 pF

Output Protection
Continuous short circuit to ground

Output Chopper Noise (1 MHz BW)
±1 mV p-p spike at approximately 10 kHz (See Note 3)

STABILITY

Gain Tempco
At G = 10 and 100, ±25 ppm FSR/°C maximum; at G = 1000, ±35 ppm FSR/°C maximum; exclusive of external gain setting resistor

Offset Voltage Tempco
At G = 10, ±5.0 μV/°C maximum;
At G = 100, ±1.7 μV/°C maximum;
At G = 1000, ±0.5 μV/°C maximum;
all RTI

Bias Current Tempco
100 pA/°C maximum, at 25°C; doubles every 10°C (maximum)

Power Supply Sensitivity
At G = 1000, ±2.0 μV/%; at G = 10, ±10 μV/% maximum; RTI

Warm up Drift (5 Minutes)
Within 2 μV RTI typical at G = 1000

Long Term Drift
3.0 μV RTI/month typical

ISOLATED POWER SUPPLY OUTPUT

Voltage
±4 Vdc nominal, with respect to INPUT LO

Current
±3 mA full load

Regulation
12%, no load to full load

Ripple
60 mV p-p at 10 kHz

INPUT POWER SUPPLY REQUIREMENTS

+15V, ±3%
3 mA, no load

−15V, ±3%
5 mA, no load

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature Range
−55°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Dimensions
1.2" x 2.8" x 0.5" (30 x 70 x 12 mm)

Shielding
RFI: 6 sides; EMI: 5 sides

NOTES:

1. Modifications for bandwidths from dc to 100 Hz, or optimized for specific settling times are available on special order. Please contact factory.
2. Filter nodes are externally accessible to allow modification of characteristics.
3. Output Chopper noise can be reduced to negligible level by suggested output multiplexer circuit.

OPERATION DATA

Application

The **MP227A** was designed as an economically competitive and functionally superior alternative to the relay multiplexing circuits traditionally used in multichannel data acquisition systems. In a typical thermocouple system, the **MP227A** replaces two functional blocks for each channel — the input filter and a dual relay, as well as the common channel high gain amplifier — and permits high-level, solid-state multiplexing to be used for low cost and high reliability.

The **MP227A** provides significantly better isolation and common-mode rejection than low-level relays and it puts the gain at a point in the system where the bandwidth is lowest (prior to multiplexing), thereby reducing total system noise. Even where multiplexing is not used, the unusual combination of performance and price makes the **MP227A** attractive for a wide variety of industrial applications.

When many **MP227A's** are used in a system, a high speed, high level analog multiplexer switches the **MP227A** outputs to a common analog output bus for subsequent A/D conversion. Any high precision isolation amplifier/filter used in such a configuration has an inherent error source of sizable magnitude that is often overlooked, ignored or simply unknown, that is, dumped charge effects. This Application Note discusses the problem, the solution, and the fringe benefits.

Dumped Charge

Figure 2 shows the apparently straightforward connection of multiple amplifiers/filters and multiplexer to a common A/D converter.

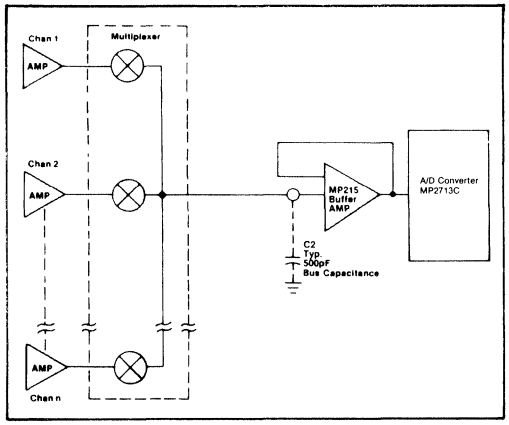


Figure 2. Multiplexing Amplifier Outputs.

Each time the multiplexer in Figure 2 switches channels, for instance, from Channel 1 to Channel 2, the Channel 1 output appears across C2, the capacitance of the output bus. The output stage of Channel 2 must absorb that dumped charge before it can reach a true final value dependent only on its input. The exact magnitude of the dumped charge is not important: what is significant is that the Channel 2 amplifier may be forced to deliver a peak instantaneous current beyond its design specifications.

The dumped charge (Q) is defined as, $Q = \int i\,dt$,

where $i = C\,dv/dt$

In a typical example, the outputs of the two channels could be at the extreme ends of the range.

Channel 1 output = + 10V.

Channel 2 output = − 10V.

This makes the voltage difference (dv).

dv = 20 volts.

Assume that the capacitance of the output bus C2 is about 500 pF, and a reasonable turn-on time for an analog switch is 100 ns, or,

$C = 500\ (10^{12})$

$dt = 100\ (10^{9})$

Solving first for the current and then the dumped charge, gives:

$$i = C\,(dv/dt) = \frac{500\ (10^{12})}{100\ (10^{9})}\ 20 = 100\ \text{mA}$$

$$Q = \int i\,dt = (100)(10^{3})(100)(10^{9}) = 10{,}000$$

pico Coulomb

Under these conditions, IC op amps, such as the popular 741, have been found to have full-scale current excursion lasting as long as a microsecond.

If the design factors allow a conventional IC output stage to drive the multiplexer instead of a high precision amplifier with an output/filter stage, no real harm is done by the dumped charge. The amplifier eventually recovers and C2 charges to the new value. The recovery time constant is the ON resistance of the multiplexer switch and C2

for R on = 300Ω

C2 = 500 pF

$T = (300)(500)\ 10^{12} = 0.15\ \mu s$

In high resolution systems, 10 time constants should be allowed to reach a voltage within 0.005% of final value. Therefore, the actual time should be 1.5 μs.

The 1.5 μs settling time required in this example is usually less than the settling time of the conventional buffer amplifier at the multiplexer output and the dumped charge effect can be safely ignored. The dumped charge cannot be ignored, however, when high precision amplifiers employing output filters are required.

The Problem

Many isolation and/or instrumentation amplifiers do not include an output filter. On the other hand, the **MP227A** has an integral two-pole Butterworth filter in the output stage. The feedback element of the **MP227A** is a capacitor and a sudden voltage step at the amplifier output, such as the dumped charge, presents a problem.

The dumped charge demands excessive current in too short a time and causes the amplifier to momentarily open-loop. The summing node changes to a large voltage, inducing current flow in the input resistor and causing an extraneous charge on the feedback capacitor.

This error source has produced observed errors as large as 0.05% in typical applications.

The Solution

Figure 4 shows the addition of a single-pole filter (R1, C1) at the output of each **MP227A** and ahead of the multiplexer. C1 of the succeeding channel, now absorbs the charge accumulated on C2 from the preceding channel. The **MP227A** no longer sees a step but a well controlled exponential change, well within its capabilities. Hence, the output stage in the **MP227A** does not open-loop, and no spurious charge is placed on the feedback capacitor.

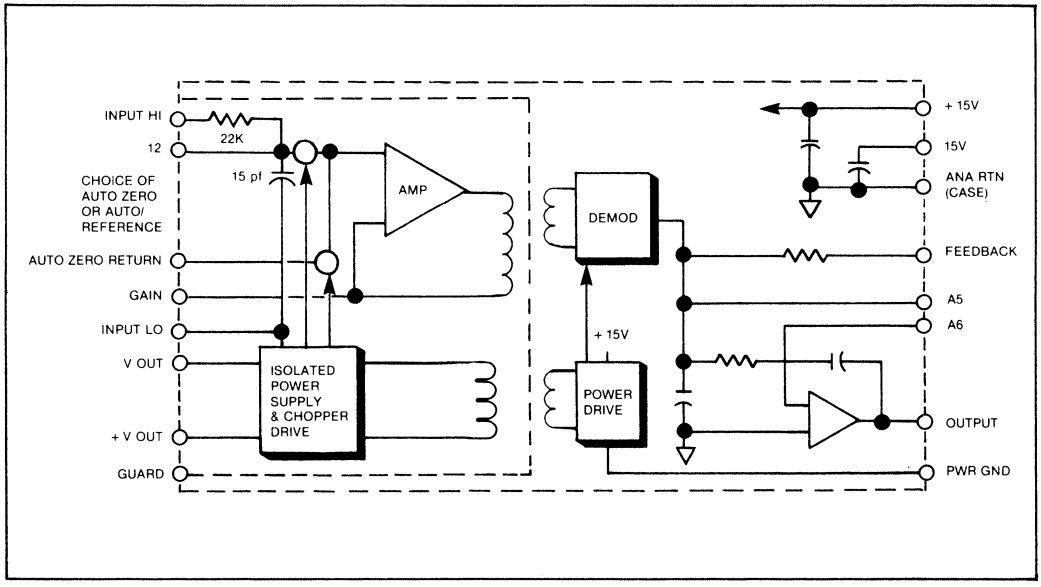


Figure 3. MP227A Isolation Amplifier Functional Block Diagram.

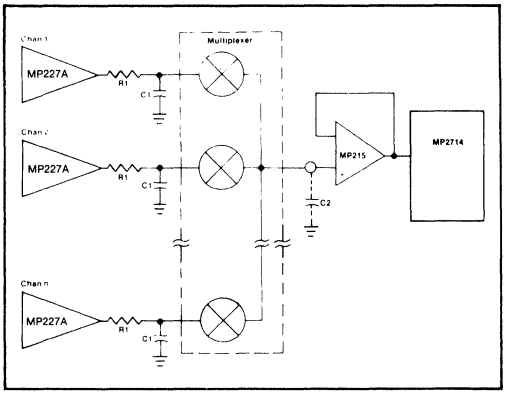


Figure 4. MP227A with Output Filters Added.

The best results are obtained with a time constant between 0.25 and 0.5 μs. This must be short for two reasons: 1) a settling time of up to 10RC does not significantly add to multiplexer settling time and 2) the recovery time is sufficiently short for final values that are independent of the duty cycle involved in reading a channel.

R1 should be between 50 and 270Ω: this value is kept intentionally low to reduce voltage divider error (R1 + R_{on} relative to R_{in} of the follower at the mulitiplexer output) to an insignificant level. These values of R1 yield values for C1 between 10,000 pF and 1,000 pF which is an acceptable range for C1. In the capacitive voltage divider, formed by C1 and the bus capacitance C2, as C1 decreases in size relative to C2, the initial voltage transferred to C1 by a succeeding channel approaches its final value and leaves a smaller exponential rise portion.

R1, C1 MUST BE INCLUDED FOR ALL HIGH RESOLUTION (>12 BITS) APPLICATIONS OF THE MP227A.

Fringe Benefits

Noise spikes inherent in the design of high performance isolation amplifiers are attenuated by 10 dB or more by the R1 C1 output filter.

The superior isolation of the **MP227A** is provided by transformer coupling. A modulator/demodulator is used in the analog signal path and is driven by an integral chopper/power driver. It is impossible to avoid some stray capacitance between the driver circuitry and the output. Careful design and layout of the **MP227A** has reduced the resulting output noise spikes caused by stray capacitance to 1 mVp-p, which is 0.01% relative to 10V F.S., when measured over a bandwidth of 1 MHz. The noise spikes repeat at 20 kHz, or twice the nominal 10 kHz frequency of the **MP227A** chopper driver.

If the output filter time constant (R1 C1) is equal to 0.5 μs, then

$fc = \frac{1}{2\pi RC}$

$= 333$ kHz

This low cut-off frequency ensures that the output spikes, over an effective bandwidth in excess of 1 MHz, are attenuated 10 dB or more, which is enough to reduce this error source from .01% to a negligible level.

USING THE MP277A

Offset Adjustment

Provision is made for external offset adjustment on the **MP227A** Precision Isolation Amplifier by connecting a 25k or 50 kΩ (100 ppm/°C or better) multi-turn potentiometer (R2) with a 1 MΩ resistor as shown in Figure 2. To adjust, momentarily short INPUT HI, INPUT LO, and AZ RTN to the output ANA RTN and set the offset potentiometer for zero output at the OUTPUT terminal.

Setting the MP227A Gain

The gain of the **MP227A** may be set to any value from 10 to 1000 by connecting an external resistor (R_G) between the GAIN and INPUT LO terminals as shown in Figure 2. Gain is equal to:

$$\text{Gain} = \frac{10.27 \times 10^3}{R_G\Omega}$$

An RN55E or better resistor is recommended for temperature stability. Untrimmed, the absolute gain will be within +2% and −3% of the calculated value.

Gain Trimming

The gain may be deliberately fine-trimmed, if desired, by connecting a 500Ω (100 ppm/°C or better) potentiometer (R1) between the FEEDBACK and OUTPUT terminals as shown in Figure 2. R1 compensates for the tolerance of R_G plus the unit-to-unit gain variability (3%) between multiple **MP227As.** This also allows standardization of the outputs of multiple **MP227As** to a common full-scale range. For volume production where cost is a factor, the trimpot may be replaced with a fixed resistor selected during final testing.

Auto-Zero Return

The signal that is amplified by the **MP227A** is actually the difference between the INPUT LO and the Auto-Zero (AZ) voltages. For normal operation, tie the AZ terminal directly to the INPUT LO terminal. In some applications, it may be convenient to offset the input deliberately by an amount that exceeds the range of the OFFSET trimpot (for example, to obtain expanded scale operation or to cancel out the initial or "tare" output of a load cell). To do this, connect the AZ terminal to a source of voltage equal to the desired offset, with noise performance and stability at least as good as the signal source.

Observe that both the INPUT HI signal and the AZ signal (if any) are measured with respect to the INPUT LO terminal. For best linearity, each signal must be within ± 1V of INPUT LO.

Open Input Indication

The user-accessible isolated power supply voltages make it possible to use a simple open input indication network. Connect a resistor on the order of 180 MΩ to the INPUT HI and either the + 4V or − 4V isolated power output terminal. This network produces a bleeder current of approximately 20 nA through the input source circuitry. If the source should open, this bleeder current will drive the **MP227A** output into a saturated state. The speed of this response is a function of the **MP227A** gain setting and input time constant.

Multiplexing MP227As

The outputs of multiple **MP227As** may be multiplexed to a common analog line as indicated in Figure 4. A single RC filter ahead of each MUX input is suggested.

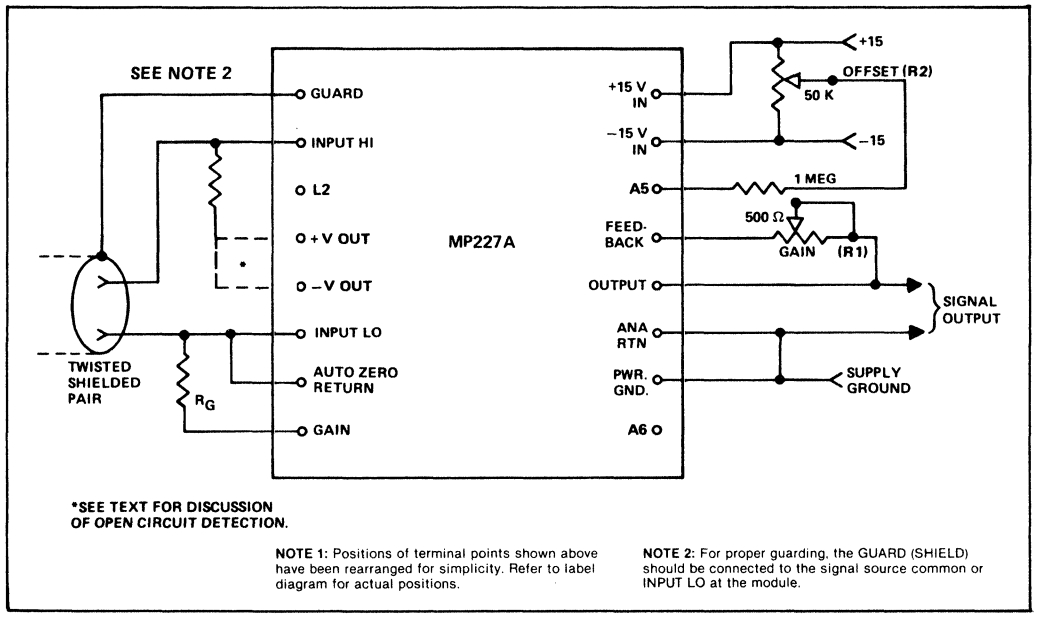


Figure 5. Typical External Connections—MP227A.

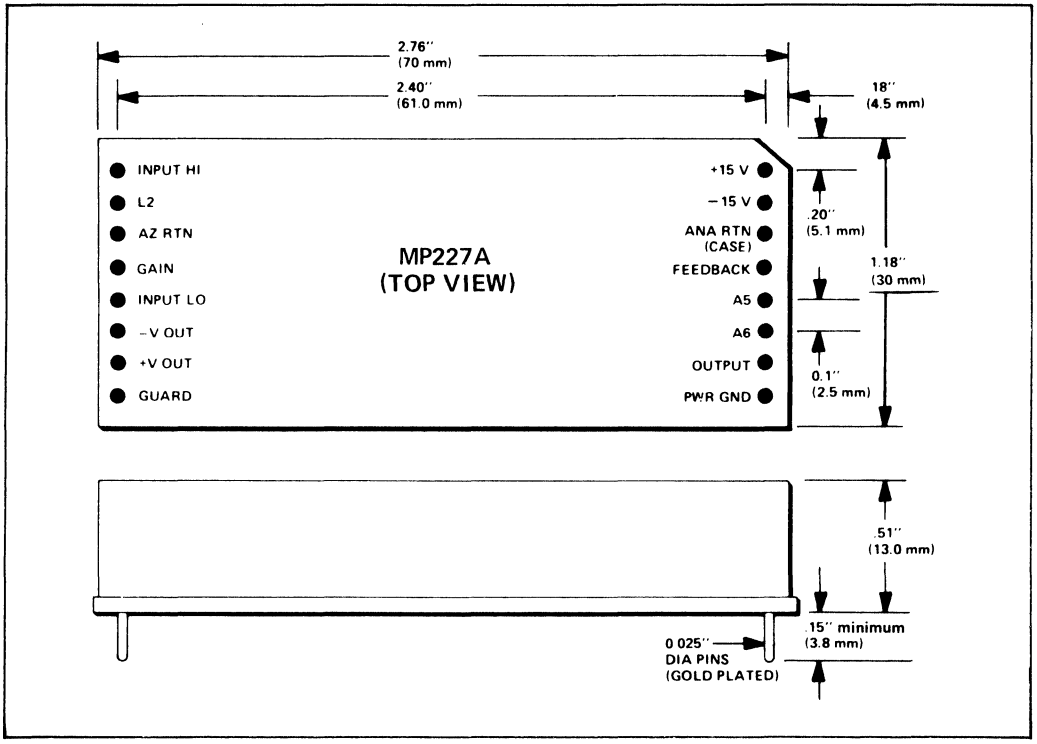


Figure 6. MP227A Mechanical & Pinout.

ORDERING GUIDE

Specify **MP227A**

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ANALOGIC®

SECTION 3

Sample-and-Hold Amplifiers

SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
Simultaneous Multi-Channel Sampling	Droop Rate	Acquisition Time	MP260	3-5
		—	MP261	3-5
Multiple, Multiplexed Inputs/Single S/H	Acquisition Time	High Linearity	MP270	3-11
		Linearity	MP271	3-15
	Acquisition Time	Medium Linearity	MP272	3-27

SAMPLE AND HOLD AMPLIFIERS

ACQUISITION TIME The time it takes the S/H amplifier to start tracking the input signal. It is measured as the maximum elapse time between application of the sample command and the point at which the output starts to track the input within a specified accuracy regardless of the previous state of the output or the magnitude or polarity of the input. See Figure 1.

APERTURE DELAY TIME The time delay between the HOLD command and the actual start of the HOLD mode. In reference to the SAMPLE mode this is called the turn-off time. See Figure 1.

APERTURE UNCERTAINTY A specification indicating how much the aperture delay time varies. It is measured as the difference between the maximum turn-off time and the minimum turn-off time. See Figure 1.

$$\triangle E = E_s \; K \log_{10}\left(\frac{t_s + t_h}{t_s}\right)$$

where:

$\triangle E$ = Output voltage error
E_s = Capacitor voltage change
K = Empirical constant for Hold capacitor dielectric ($K = 1.5 \times 10^4$ for polystyrene capacitor in MP270)
t_s = Sample time; t_h = Hold time

Example: For a 20V step, a Sample time of 2 μs, and a Hold time of 5 μs, $\triangle E$ = 1.5 mV.

DIGITAL CONTROL SPECIFICATIONS These are specifications for interfacing the digital control signals to the S/H and include: the logic type, e.g., TTL; the sense of the logic, e.g., 1 = SAMPLE, 0 = HOLD; and the required speed of the rise or fall time between SAMPLE and HOLD modes.

DISTORTION Unwanted output signals generated as a result of non-linearities in the sample and hold.

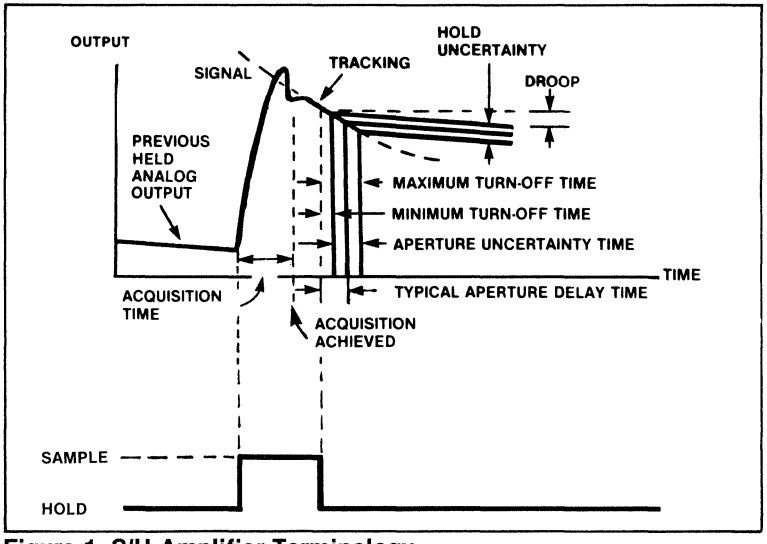


Figure 1. S/H Amplifier Terminology.

DIELECTRIC ABSORPTION ERROR Dielectric absorption error is the decaying of the HOLD voltage on the HOLD capacitor due to the charge redistribution within the capacitor dielectric. This error occurs as a result of rapidly charging the HOLD capacitor and then disconnecting the charging source. The output voltage will decay according to the following relationship:

DROOP RATE The maximum rate of change of the output voltage in the HOLD mode.

FEEDTHROUGH REJECTION The ratio, in db, of a specified input signal to the resultant output signal, during HOLD, over a stated frequency range.

FULL POWER BANDWIDTH The highest frequency at which an analog circuit will track a sinusoidal signal large enough to drive

the output to its rated full-scale value at its maximum rated power. The equation is as follows:

$$f = \text{Slew Rate} / 2\pi e_{fs}$$

where f = Full Power Bandwidth and e_{fs} = rated full scale output.

GAIN ACCURACY The maximum amount that the actual voltage gain deviates from the nominal value expressed as a percentage of that nominal value. This takes into account the effects of temperature variations, power supply variations, and drift with time, if significant.

INPUT IMPEDANCE Specified as a nominal resistance in parallel with a capacitance value, given for the SAMPLE mode. If the HOLD mode impedance is significantly different it will also be given. Input impedance is given at maximum rated input voltage.

INPUT SIGNAL RANGE The acceptable input signal levels, over the full power bandwidth, for which the S/H will maintain rated linearity.

LINEARITY In the sample mode, linearity is a measure of how accurately the output tracks the analog input signal. In the hold mode, it refers to the pedestal offset which varies over the input signal range.

OFFSET DRIFT The worst case variation in output offset voltage due to changes in ambient temperature, power supply voltage, and drift with time.

OUTPUT OFFSET VOLTAGE The maximum value of output voltage observed when sampling zero input at a stated temperature and power supply voltage.

OUTPUT VOLTAGE SWING The rated nominal output voltage range into a specified minimum load impedance.

OVERLOAD RECOVERY TIME The time required for the circuit to return to linear operation, within a stated tolerance, after removal of a sustained input that was large enough to drive the circuit into complete saturation (i.e., a condition in which further increase in the input did not significantly increase the output).

PEDESTAL OFFSET ERROR An offset error caused by switching to the HOLD mode. It is affected by a number of parameters including the capacitance of the mode control switch, the HOLD mode command signal level, the analog input signal level and the sample rate. The pedestal offset error may be nonlinear.

SAMPLE AND HOLD AMPLIFIER Sometimes called a track and hold amplifier, this is a circuit used to monitor a rapidly changing analog signal and, upon command, hold that signal level for processing by another circuit, typically an ADC. The S/H operates in two sequential modes, SAMPLE and HOLD, as determined by the state of a switch at the input to the amplifier which is controlled by an external digital control signal. In the SAMPLE mode the switch is closed, the input signal is connected to the amplifier and the output tracks it very closely. In the HOLD mode the switch is open, the input is disconnected from the amplifier and its level at the time of disconnect is maintained by a capacitor across the input. See Figure 2.

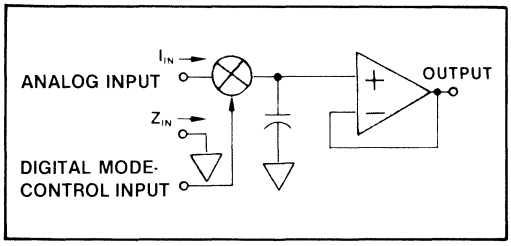


Figure 2. S/H Amplifier Block Diagram.

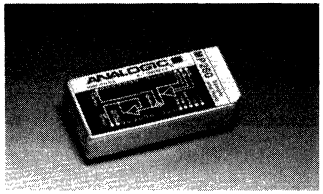
SETTLING TIME The maximum time required for the output to track the input to within the specified accuracy after a full range step change while in the SAMPLE mode.

SLEW RATE The maximum slew rate is the fastest rate of change of the output of the amplifier in the SAMPLE mode. The output changes most rapidly when a step change is applied at the input sufficient to drive the output from one end of its range to the other.

SMALL SIGNAL BANDWIDTH The maximum small signal bandwidth is the highest frequency at which an amplifier will track, to within 3 db of the low frequency response, a sinusoidal signal of less than the slew rate limited amplitude.

TURN OFF TIME See aperture delay time.

VOLTAGE GAIN The nominal ratio of output to input.



ANALOGIC

MP260/MP261

Low Cost High Speed High Accuracy Sample & Hold Amplifiers

Description

The Analogic MP260 and MP261 are low cost, highly accurate Sample-and-Hold (S/H) Amplifiers that sustain precise over-all system performance in applications requiring resolutions of up to 16-bits. The MP260 design is optimized for a time-shared S/H function at the input of a high speed (50 μs or faster conversion time) analog-to-digital converter. Its fast acquisition time of 5 μs and excellent linearity of 0.002% are representative of its superior performance. The MP261, with its extremely low droop rate of only 20 μV/ms, is ideal for simultaneous sample-and-hold applications. For example, as many as 500 channels may be held and sequentially sampled (at 16-bit resolution, 30 μs/sample, ± 10V full scale) before the last channel has drooped by only one significant bit (300 μV)! The rated performance of these units is maintained in the presence of harsh electromagnetic and electrostatic interference by shielding all components, including the low dielectric absorption hold capacitor, within a 1" x 2" Modupac™ metal case.

Features

MP260/MP261

- **Excellent Linearity**
  ± 0.002% FSR maximum
- **Negligible Feedthrough**
  100 dB Rejection (0.001%)
- **Low Aperture Uncertainty**
  1 nanosecond
- **Complete Small Size Module**
  1" x 2" Modupac™ Case
- **User-Selectable Input Configurations**
  Buffer or Inverter
- **Very Low Cost**

MP260

Optimized for Time-Shared S/H Applications

- **Fast Acquisition time**
  5 μs to ± 0.003% Full Scale Step
- **Low Pedestal Non-Linearity**
  ± 0.003% max.

MP261

Optimized for Simultaneous S/H Applications

- **Very Low Droop rate**
  20 μV/rms max.
- **Very Low Pedestal Non-Linearity**
  ± 0.002% max.

Applications

- **Low-Cost Simultaneous Sample & Hold Systems**
- **Automatic Test Equipment Systems**
- **Multi-Channel, Multi-Input-Level, 12- to 16-bit Data Acquisition Systems**
- **High Resolution, High Speed Data Acquisition Systems**
- **Audio Digitizing Systems.**

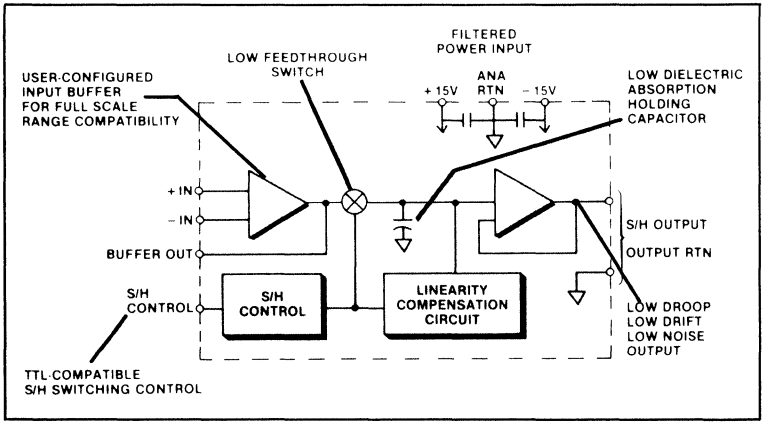


Figure 1. MP260/MP261 Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

SAMPLE MODE
(Input configured for Unity Gain Buffer)

Full Scale Linear Input Voltage Range (FSR)
±10V

Without Damage
±15V

Input Impedance
$10^9\Omega$ || 10 pF

Full Power Bandwidth
80 kHz, (MP261 — 20 kHz)

Small Signal Bandwidth
1 MHz, (MP261 — 150 kHz)

Slew Rate
10 V/μs, (MP261 — 2 V/μs)

Non-Linearity
±0.002% (max.)

Noise (300 kHz bandwidth)
40 μV rms

Gain
1 ±0.02%

Total Harmonic Distortion (20-20 kHz sinusoid input)
0.002% max.

SAMPLE-TO-HOLD TRANSITION

Aperture Delay Time
50 ns

Aperture Uncertainty
1 ns

Switching Transient Decay Time to 0.003%
0.5 μs typ., 1 μs max.

HOLD MODE

Voltage Swing into 2K Ω || 500 pF load)
±10V min.

Impedance
<1Ω @ dc

Hold Offset Pedestal
10 mV max; Proportional to input, (MP261 — 5 mV max; Constant for all input signals

Offset Pedestal Non-Linearity (±5V FSR)
±0.001% max.

Offset Pedestal Non-Linearity (±10V FSR)
±0.003% max., (MP261 — ±0.002% max.)

Offset @ 25°C (Externally Adjustable to Zero)
10 mV max., (MP261 — 5 mV max.)

Offset Tempco
(20 typ., 0.2 max. μV/μs, (MP261 — (5 typ., 15 max.) μV/°C

Voltage Feedthrough Attenuation (20V p-p 100 kHz input)
100 dB typ., 96 dB min.

Droop Rate @ 25°C (typically doubles every 14°C)
0.02 typ., 0.2 max. μV/μs, (MP261 — 1 typ., 20 max. μV/ms)

Noise (300 kHz bandwidth)
50 μV rms

Dielectric Absorption Error[1]
±0.003% of input voltage change typ.

HOLD-TO-SAMPLE TRANSITION

Acquisition Time
(Measured with 5K Ω || 500 pF load)

To within ±0.01% of 10V Step
3.5 μs max.

To within 0.003% of 10V Step
4.0 μs max., (MP261 — 10 μs max.)

To within 0.01% of 20V Step
4.5 μs max.

To within 0.003% of 20V Step
5.0 μs max., (MP261 — 15 μs max.)

DIGITAL CONTROL INPUT

Logic Type
TTL Compatible

Sample
Logic "1" (+3V min.)

Hold
Logic "0" (0.4V max.)

Required Fall Time
10 ns max.

POWER, MECHANICAL, ENVIRONMENTAL

Power Supply
±15V ±3% @ 12 mA nom. (Plus load current), (MP261 — ±15 ±3% @ 6 mA nom. (Plus load current)

Operating Temperature
0°C to 70°C

Relative Humidity (Up to 40°C) non-condensing
0 to 95%

Modupac™ Dimensions
1" x 2" x 0.44"
(25.4 x 50.8 x 11.2 mm)

Shielding
RFI 6 sides; EMI 5 sides

[1]At Hold Time = Twice Sample Time
**Unless otherwise stated, percentage values apply to FSR of 20V.

The high speed Input Buffer Amplifier feedback path is completed at the S/H pin terminals. This provides user capability for gain programming (Figure 1), or for replacing the amplifier stage in typical D/A converters. Performance specifications of the uncommited amplifier are furnished below.

Input Offset Voltage
<6.0 mV, (MP261 — <2.0 mV)

Input Offset Current
<5 nA, (MP261 — <1 nA)

Input Bias Current
<10 nA, (MP261 — < 2 nA)

Input Impedance
$10^9\Omega$ || 10 pF

Gain Bandwidth Product
3 MHz

Output Voltage Swing
± 10.5V min. (R_L ≥5 kΩ)

Common Mode Rejection Ration (CMRR)
85 dB min.

Design Features

The MP260 and MP261 support error budgets for system accuracy of 14 to 16-bits with a tracking linearity of 0.002%, low noise of 50 μV rms and a pedestal offset uncertainty of only 0.001%. System throughput speeds may actually be increased with these units by allowing input multiplexer switching to occur during A/D conversion (the Hold mode rejection is typically 100 dB or 0.001%), without a significant reduction in accuracy.

Each S/H is a complete flexible unit as shown in Figure 1. The non-commited input amplifier may be used as a high impedance buffer (following a multiplexer) or as a high speed output amplifier (following a current output digital-to-analog converter) or providing gain to match a wide range of signal inputs.

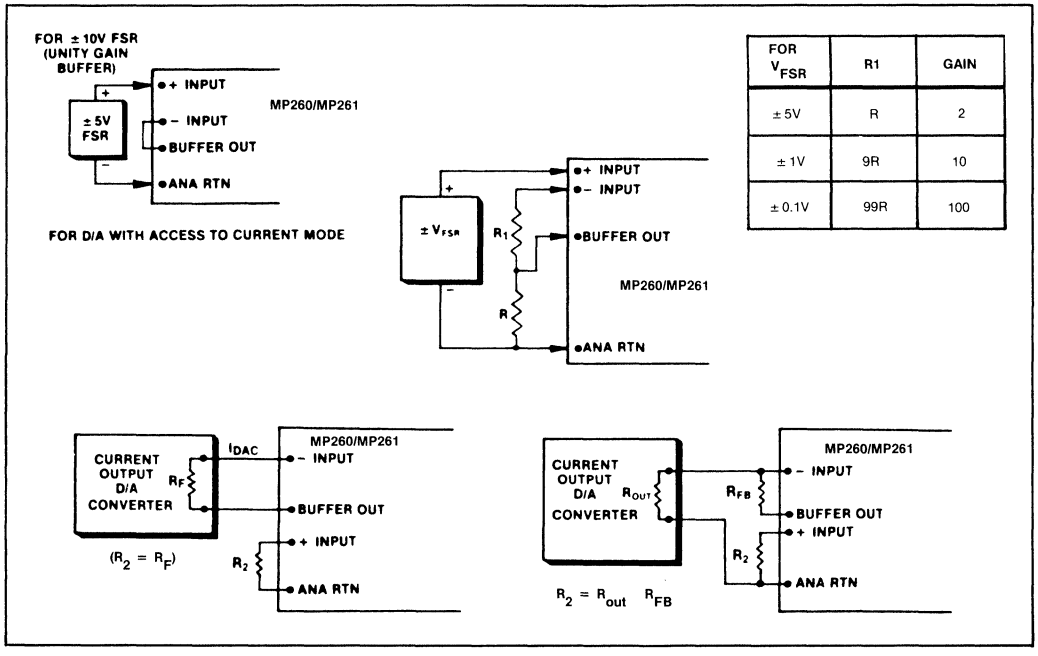
Unlike IC S/H circuits, these modular units are thoroughly specified for all critical performance parameters, many of which aren't even mentioned on IC S/H specification sheets. Note also that these modular units occupy less PC-board "real estate" than many IC S/H designs with their requisite external discrete components.

USING THE MP260/MP261

Input Buffer Configurations

Figure 2 illustrates how the input buffer amplifier may be configured to provide gains of one through ten so that the S/H output will have a ± 10V FSR swing.

The illustration also includes sample configurations of the input buffer when used to replace the current-to-voltage amplifiers of D/A converters in which the current outputs are usually available.



FOR V_{FSR}	R1	GAIN
±5V	R	2
±1V	9R	10
±0.1V	99R	100

Figure 2. Input Configuration Connections for MP260/MP261, Including Use As Replacement for D/A Output Amplifiers.

MP260/MP261 Trim Adjustments

As shown in Figure 3, the S/H MP260/MP261 may be adjusted to compensate for any S/H offset and for system offsets common to all channels sampled through the installed S/H unit.

(1) Connect a potentiometer of indicated resistance to the S/H trim terminals and the wiper to the + 15V supply.
(2) Sample a channel with desired zero voltage signal.
(3) Issue a train of SAMPLE and HOLD commands to obtain a stable output value.
(4) Adjust the trim potentiometer for zero voltage at the S/H output.

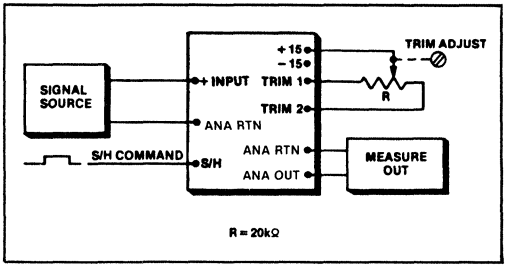


Figure 3. Trimming MP260/MP261 for Zero Offset.

Simultaneous S/H Application

Figure 4 illustrates the use of MP261 as simultaneous S/H units in a multi-channel data acquisition system. As shwon, each S/H may be independently configured at the input for an appropriate gain, while the oututs are connected as differential inputs to an 8-channel analog multiplexer.

In a typical seismic exploration application, for example, the control logic causes all inputs to be sampled and the tracked inputs to be "held" at the same time. With only 1 ns aperture uncertainty, the S/H output signal is accurate to within ½ bit for signals are then converted sequentially in the MP8016 and eight parallel 16-bit values are placed on the data bus of a minicomputer/microprocessor control system.

Figure 5 illustrates the use of high accuracy MP261 S/H units in an Automatic Test Equipment (ATE) application. A high quality 16-bit D/A converter, such as the Analogic MP1916TC, or 14-bit D/A converter MP1914TC), is programmed to supply accurate analog signals as stimuli for the unit under test (UUT). Each analog voltage is held at the output of a S/H unit and connected to an appropriate analog stimulus node of the UUT.

Under program control, the recorded results are compared with the specified performance for the computer controlled profile of analog stimuli. The low cost per channel of the MP261 makes this application particularly cost effective for very high quality performance. The illustrated instrumentation is far less costly than the usual D/A-per-channel approach.

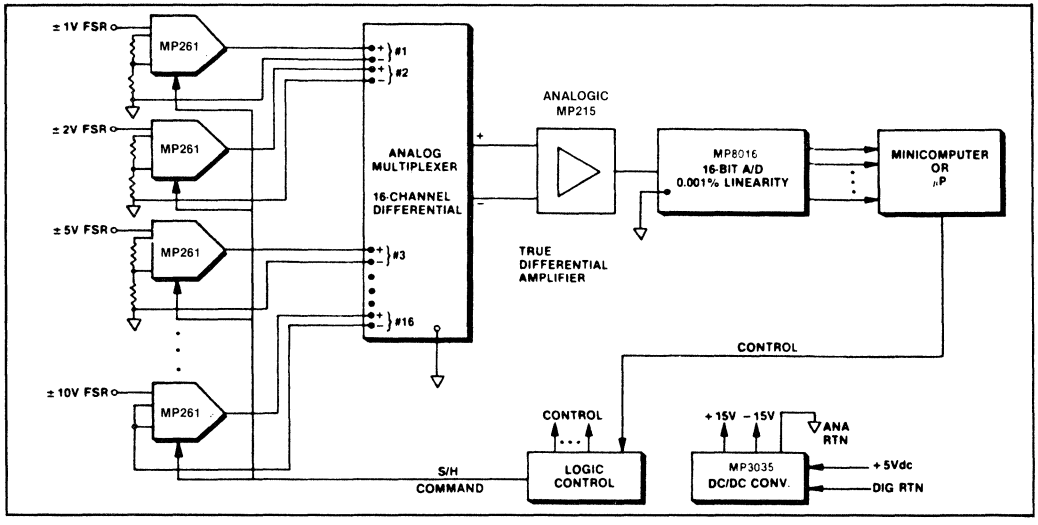


Figure 4. MP261 in a Simultaneous S/H Application, Showing Independent Gain Setup for Each Output Channel.

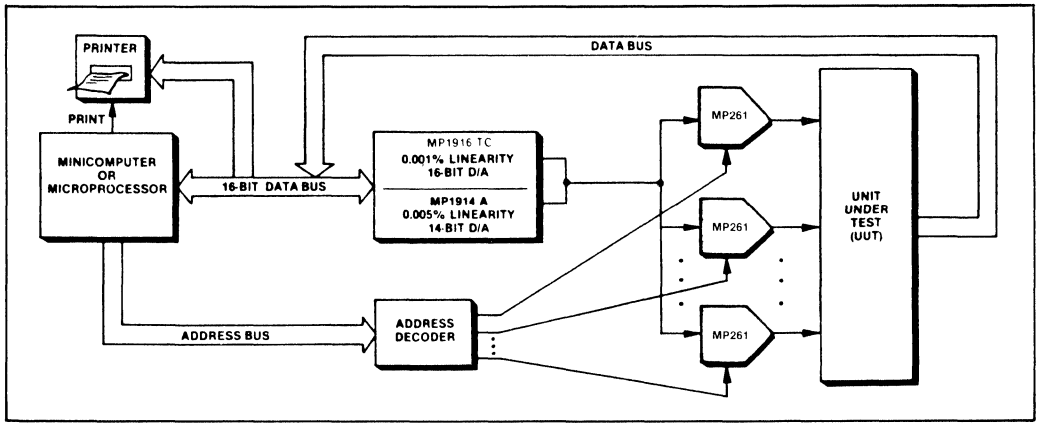


Figure 5. Time-Sharing a Precise D/A Converter with a S/H per channel for High Precision Analog Signal Stimulus in ATE Systems.

MP260 Time-Shared Application

Figure 6 illustrates a typical application of the MP260. It provides the input to a 14-bit A/D converter (MP2734) from multiplexed analog channels with the same full scale range specifications. The excellent feedthrough rejection of the MP260 inputs may be switched from one full scale limit to the opposite polarity full scale limit.

For a 20-volt step, the 100 dB rejection ratio means only 200 microvolts into the "held" channel (0.001% error). Thus, there is no significant penalty incurred by switching inputs during the conversion cycle. The S/H performance allows the multiplexer circuits to stabilize for the next channel while the current channel is still being converted.

As shown in Figure 7, the sample/hold control timing sequence, that takes advantage of this "overlapping" of channel addressing and channel conversion, increases system throughput. The example in Figure 7 allows the MUX and amplifier circuits to stabilize before the value is switched to the S/H input. For competitive S/H units with poorer feedthrough rejection, the S/H inpuyt must remain connected to the "held" channel until conversion is completed. Otherwise, an error will be introduced into the currently converted signal.

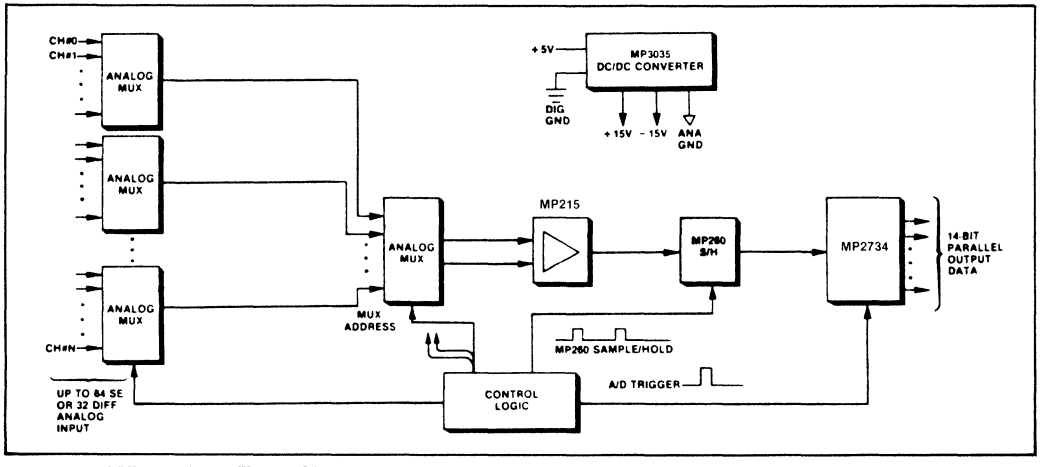


Figure 6. MP260 in a Time-Shared Application Block Diagram.

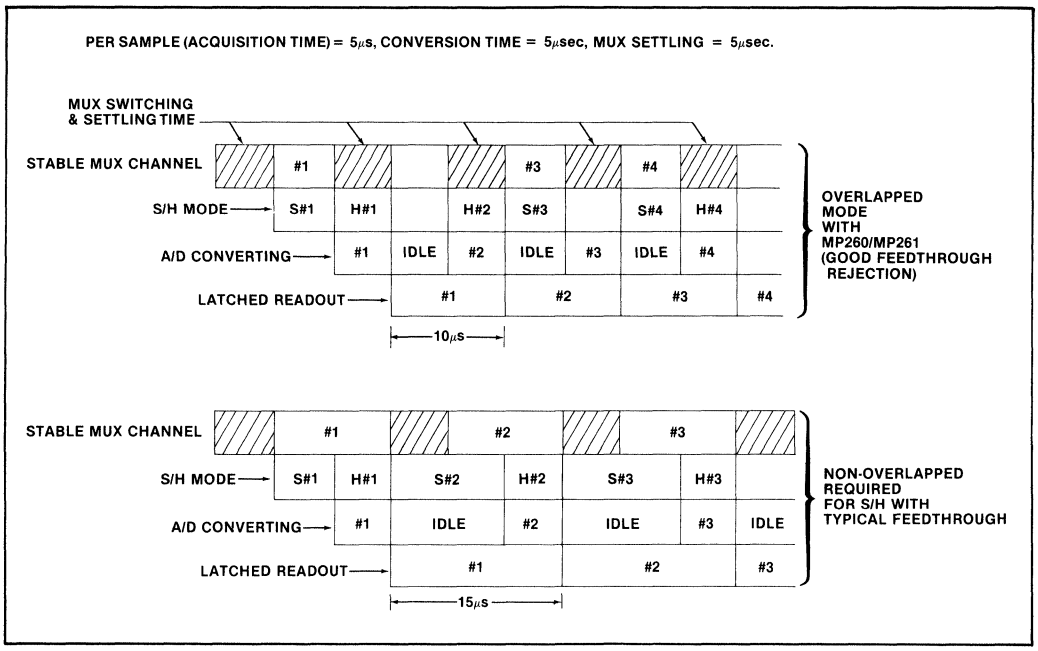


Figure 7. Timing S/H Waveforms, Showing Overlapped Switching and Converting Intervals for MP260 Instrumentation.

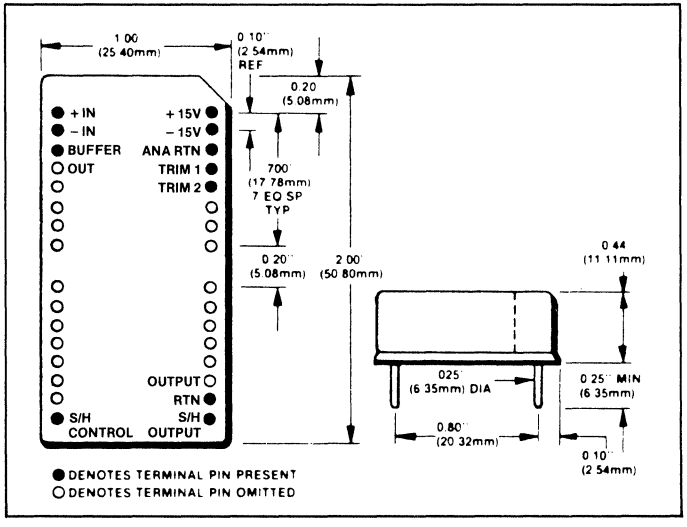
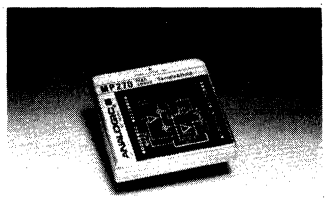


Figure 8. MP260/261 Mechanical & Pinout.

ORDERING GUIDE

Specify **MP260** or **MP261**



ANALOGIC®

MP270

Very High Speed Sample & Hold Amplifier

Description

The Analogic MP270 is a high speed, high accuracy sample and hold amplifier, featuring a low acquisition time of 1 μs aperture uncertainty time of less than 0.2 ns, and wide bandwidth, assuring compatibility with data acquisition systems having throughput rates up to 300 kHz. The high input impedance of the MP270 combined with its low noise and low feedthrough characteristics assure accuracies of 0.01% at these throughput rates.

Performance

The 1 μs maximum acquisition time and the 0.01% accuracy of the MP270 are attained by placing a feedback loop around the switching circuit. This design technique provides compensation for any switching and non-linearity errors within the loop while forcing the output to follow the input. The introduction of very fast switching circuits limits the aperture uncertainty time to within 0.2 ns and virtually guarantees measurement repeatability. The 100Ω input impedance of the MP270 assures minimal source loading without additional external buffering, and the low hold mode decay rate of 2 μV/μs assures highly accurate digitization even at slower conversion rates.

Using the MP270

Because of the exceptionally high accuracy-with-speed performance of the MP270 and its low noise and wide bandwidth characteristics, care must be taken to minimize noise pickup on the signal input leads. All input and control pulse leads should be short and shielded, and a remotely generated control signal should be buffered close to the MP270 to prevent ringing.

Features

- **1 μs Maximum Acquisition Time with 0.01% Accuracy**
- **Wide Bandwidth:** 500 kHz for Full Power
- **High Input Impedance:** $10^8\Omega$
- **Low Aperture Uncertainty of 0.2 ns Guarantees Accurate Digitization**
- **Low Droop Rate:** 2 μV/μs

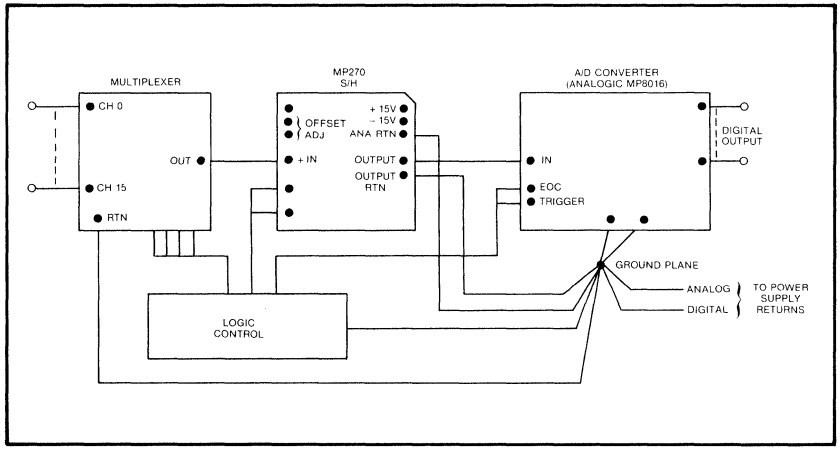


Figure 1. MP270 Sample and Hold Amplifier with MP2912A Analog-to-Digital Converter and AN4716 Multiplexer Guarantees a Throughput Rate of Up to 140 kHz for a 12-Bit Data Acquisition Application.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

SAMPLE MODE

Input Voltage Range
± 10V max. useful signal, ± 15V max. without damage

Gain
+ 1.000 ± 0.005%

Small Signal Bandwidth
10 MHz min.

Full Power Bandwidth
500 kHz min.

Slew Rate
50 V/μs min.

Input Impedance
$10^8\Omega$ in parallel with 10 pF

Linearity
0.005% max.

Settling Time
To 0.01% of 20V Input Step
700 ns typ., 900 ns max.

To 0.05% of 10V Input
450 ns typ., 600 ns max.

Input Bias Current
< 100 pA

Input Offset Voltage
± 20 mV max., adjustable to zero (see Fig. 4)

Offset Tempco
± 50 μV/°C typ.

Offset vs. Supply
± 0.0015% FS voltage change typ.

Noise
300 μV p-p max.

SAMPLE-TO-HOLD SWITCHING

Switching Transient Settling Time (to 0.01% of FS)
150 ns typ., 400 ns max.

Aperture Time
10 ns typ.

Aperture Uncertainty Time
± 0.2 ns typ.

HOLD MODE

Output Voltage
± 10V max.

Maximum Load
500Ω in parallel with 200 pF (short circuit protected)

Output Impedance
0.1Ω

Droop Rate
2 μV/μs max.

***Dielectric Absorption**
Approx. 0.0075% @ 2 μs sample time, 5 μs hold time

Voltage Feedthrough (20V p-p 500 kHz Sinusoidal on Input)
− 80 dB max.

Hold Offset (pedestal)
± 10 mV adjustable to zero with externally accessible internal adjustment

Hold Offset Tempco
± 30 μV/°C typ.

Hold Offset Non-Linearity (Pedestal Variation over Input Signal Range)
± 0.005% max.

Output Voltage Variation due to Control Pulse Variation
1 mV per volt of change in control signal typ.

Noise
0.5 mV p-p max.

HOLD-TO-SAMPLE SWITCHING

Acquisition Time
To 0.01% of 20V Step Input
800 ns typ., 1 μs max.

To 0.05% of 10V Step Input
550 ns typ., 700 ns max.

DIGITAL CONTROL INPUT

Compatibility
TTL compatible, 2 logic loads

Input Impedance
1 kΩ in parallel with 33 pF (3 mA sink current)

Sample
Logic "0" (+ 0.4V max.)

Hold
Logic "1" (+ 3.0V min.)

Required Rise Time
10 ns max. to obtain minimum aperture time

POWER SUPPLY

+ 15V ± 3%
60 mA max. + load current

− 15V ± 3%
40 mA max. + load current

ENVIRONMENTAL & PACKAGING

Operating Temperature Range
0°C to 70°C

Storage Temperature Range
− 25°C to + 85°C

Relative Humidity
0 to 95%, non-condensing

Modupac™ Dimensions
2" x 2" x 0.39" (50.8 x 50.8 x 9.9 mm)

Electrical Shielding
RFI 6 sides; EMI 5 sides

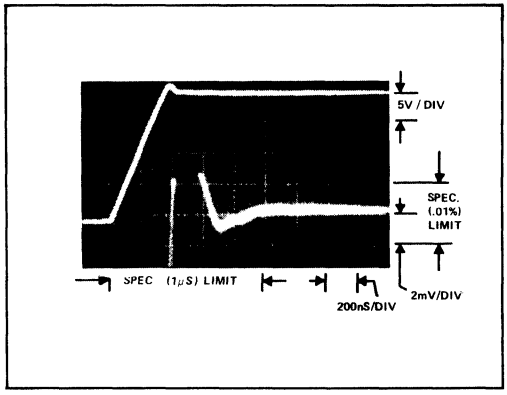


Figure 2. MP270 Output Characteristics Showing Acquisition Time. Upper Waveform Shows Response of MP270 to a 20V Step Input Signal. Lower Waveform is a 2500:1 Amplification of the Upper Trace and Shows Settling Characteristics of the MP270.

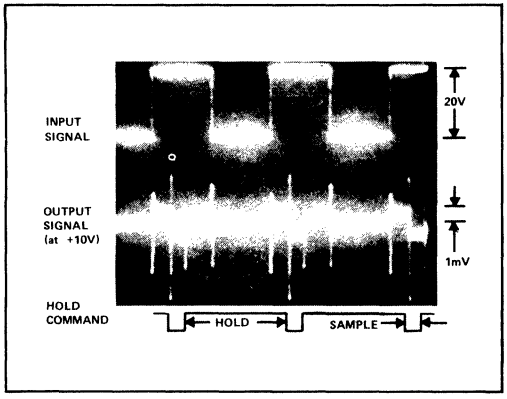


Figure 3. MP270 Output Characteristics Showing Hold Pedestal and Feedthrough Rejection Characteristics. The MP270 Samples the Input Signal Only While it is at +10V. When the Input Signal Goes to −10V, the MP270 Hold Voltage Changes by Less Than 1 mV.

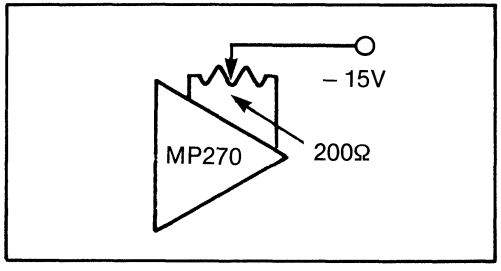


Figure 4. MP270 Input Offset Adjustment.

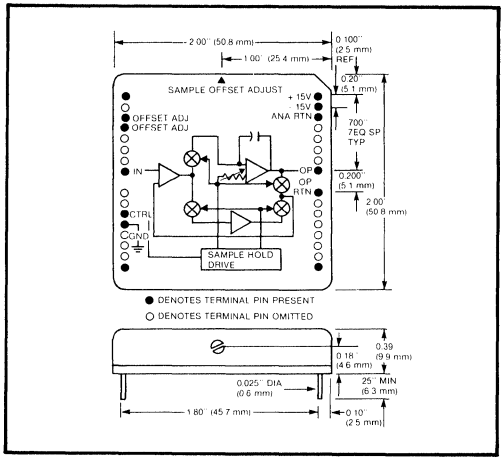


Figure 5. MP270 Outline Drawing.

Input Voltage offset compensation is accomplished by connecting a potentiometer between the two OFFSET ADJ. terminals. The variable output of the potentiometer is adjusted until the offset is reduced to an acceptable level.

*Dielectric Absorption

Dielectric absorption is the decaying of the Hold voltage (on the Hold capacitor) due to the charge redistribution within the capacitor dielectric. This error is a resultant of rapidly charging the Hold capacitor and disconnecting the charging source. The output voltage will decay according to the following relationship:

$$\Delta E = E_S K \log 10 \left(\frac{t_s + t_h}{t_s} \right)$$

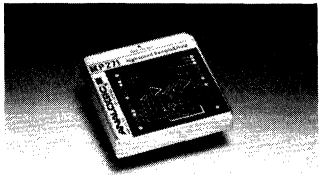
where:

ΔE = Output voltage error
E_s = Capacitor voltage change
K = Empirical constant for Hold capacitor dielectric (K = 1.5 x 10^4 for polystyrene capacitor in MP270)
t_s = Sample time;
t_h = Hold time

Example: For a 20V step, a Sample time of 2 μs, and a Hold time of 5 μs, ΔE = 1.5 mV.

ORDERING GUIDE

Specify **MP270**



ANALOGIC®

MP271

High Speed-Precision Sample & Hold Amplifier

Description

The MP271 (see Fig. 1) is one of the highest performance sample-and-hold amplifiers currently available and provides an exceptional combination of very high speed with precision. Performance is optimized for use in data acquisition systems which have sampling rates of up to 300 kHz and resolutions of up to 16 bits. The very high speed performance of the MP271 is evidenced by the acquisition time of 1.0 μs, the aperture uncertainty of 0.2 ns, and the full power bandwidth of 600 kHz. The capability of the MP271, in high resolution systems of up to 16 bits, is demonstrated by its excellent linearity and feedthrough specifications. It has a non-linearity of 0.003% maximum while sampling, a sample-to-hold offset non-linearity of 0.002% maximum, and a high frequency feedthrough of typically 0.001% at 500 kHz.

No other sample-and-hold amplifier matches the overall performance of the MP271. It surpasses the previously best available modular unit (the Analogic MP270). In comparison with integrated circuit (IC) units, it is an order of magnitude better in specific features such as feedthrough, aperture jitter, linearity and pedestal non-linearity.

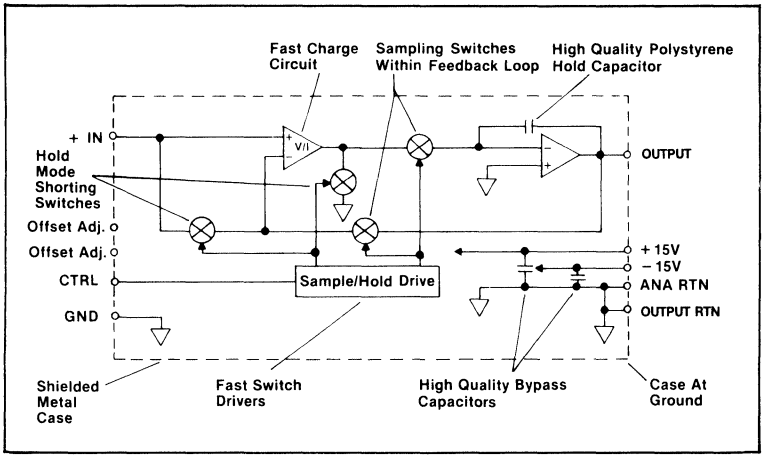


Figure 1. MP271 Sample & Hold Amplifier Functional Block Diagram.

Features

- **Excellent Linearity:** ± 0.003% max.
- **Extremely Low Feedthrough:** − 100 dB (0.001%)
- **Very Low Pedestal Variation:** ± 0.002% max.
- **Fast Acquisition:** 1.0 μs to 0.005%
- **Low Aperture Uncertainty:** 0.2 ns
- **Wide Bandwidth:** 500 kHz full power
- **High Input Impedance:** 100 MΩ
- **Low Droop:** 2 μV/μs

Applications

- **Wideband Data Acquisition Systems**
- **Telecommunications Digitizing**
- **Industrial Process Control Systems**
- **Medical Scanning Systems**
- **Nuclear Research**

Using the MP271

The performance of the MP271 is optimized for use in multiplexed, high speed, high resolution, data acquisition systems. The *very low hold mode feedthrough MP271* significantly increases system throughput rates by allowing the A/D conversion time to overlap the multiplexer switching time without degrading system accuracy.

Maximum throughput is achieved by switching the multiplexer to the next channel while the S/H holds the previous channel value. The multiplexer settles fully to the new value while the A/D conversion is completed on the previous channel value. At the end of the conversion, the MP271 switches to the sample mode; it acquires the new input and the new conversion is triggered.

(continued)

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

SAMPLE MODE

Input Voltage Range
±10V (±15V without damage)

Gain
+1 ±0.01% max., +1 ±0.003% typ.

Small Signal Bandwidth
10 MHz min.

Full Power Bandwidth
500 kHz min.

Slew Rate
50 V/μs min.

Input Impedance
$10^8\Omega$ in parallel with 10 pF

Nonlinearity (for 20V input)
±0.003% max.

Settling Time
To within ±0.005% of 20V Input Step
850 ns typ., 1.0 μs max.

To within ±0.010% of 20V Input Step
700 ns typ., 900 ns max.

To within ±0.050% of 10V Input Step
450 ns typ., 600 ns max.

Input Bias Current
100 pA max.

Input Offset Voltage
±20 mV max., adjustable to zero

Offset Tempco
±50 μV/°C typ.

Offset vs. Supply
±0.0015% FS per % supply voltage change typ.

Noise (10 MHz bandwidth)
300 μV p-p (≈ 50 μV rms) max.

SAMPLE-TO-HOLD SWITCHING

Switching Transient Settling Time (to ±0.01% of FS)
150 ns typ., 400 ns max.

Aperture Time
10 ns typ.

Aperture Uncertainty
±0.2 ns typ.

HOLD MODE

Output Voltage Range
±10V min.

Maximum Load
500Ω in parallel with 200 pF, short circuit protected (tested with 100 pF load)

Output Impedance (dc)
0.1Ω

Droop Rate (@ 25°C)
2 μV/μs max.

Dielectric Absorption
0.0075% @ 2 μs sample time, 5 μs hold time

Voltage Feedthrough (20V p-p 500 kHz sinusoidal input)
−100 dB typ., −94 dB max.

Hold Offset (pedestal)
±10 mV unadjusted. Adjustable to zero with externally accessible internal adjustment

Hold Offset (pedestal) Tempco
±30 μV/°C typ.

Hold Offset Nonlinearity (pedestal variation over input signal range)
±0.002% max.

Output Voltage Variation due to Control Pulse Variation
1 mV per volt of change in control signal typ.

Noise (10 MHz bandwidth)
0.5 mV p-p typ., 1 mV p-p max. (≈150 μV rms)

HOLD-TO-SAMPLE SWITCHING

Acquisition Time
To within ±0.005% of 20V Input Step
1.0 μs typ., 1.1 μs max.

To within ±0.01% of 20V Input Step
800 ns typ., 1.0 μs max.

To within ±0.05 % of 10V Input Step
550 ns typ., 700 ns max.

DIGITAL CONTROL INPUT

Logic Type
TTL compatible, 1 logic load (1 μA load)

Sample
Logic "0" (+0.4V max.)

Hold
Logic "1" (+3V min.)

Required Rise Time
5 ns max. to obtain min. aperture time

POWER SUPPLY

+15V ±3%
50 mA max. + load current

−15V ±3%
45 mA max. + load current

ENVIRONMENTAL & MECHANICAL

Operating Temperature Range
0°C to 70°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Modupac™ Dimensions
2" x 2" x 0.39" (50.8 x 50.8 x 9.9 mm)

Electrical Shielding
Electrostatic 6 sides; Electromagnetic 5 sides

Using the MP271 (cont.)

High frequency components may be present at the S/H input from two sources: ultra fast multiplexer switching of full scale step inputs and high frequency data. The superior feedthrough characteristics of the MP271 result in the hold mode output voltage changing by only 0.001% (– 100 dB) with a 20V p-p 500 kHz sinusoidal input applied.

Fig. 2 shows an application in which system speed and accuracy are optimized with the MP271. The MP2734 conversion time is only 6.8 μs to 14 bits and the differential linearity is ± ½ LSB (± 0.003%). The low feedthrough of the MP271 (0.001%) complements system performance. The multiplexer is switched during the hold mode and its settling time overlaps the conversion time. The system throughput rate is determined solely by the 6.8 μs conversion time plus the 1.1 μs maximum acquisition time (to ± 0.005%) of the MP271. This yields a system throughput rate of 125 kHz to 14 bits.

System Considerations

A sample-and-hold amplifier is used to reduce the time uncertainty (and resultant amplitude error) in practical systems which have inherent finite sampling apertures. The MP271 reduces this time to only 0.2 ns... the aperture uncertainty time. In a system without a sample-and-hold, the time uncertainty is the conversion time of the A/D converter, generally measured in microseconds. See the Analogic Data-Conversion System Digest, for a complete treatment of this subject.

The time uncertainty used in calculating the error vs. information frequency, is the *system* time uncertainty. The system time uncertainty is the MP271 aperture time uncertainty, plus any jitter in generating the control input to the MP271. Control input jitter is frequently caused by triggering the A/D with the system clock and then using the end-of-conversion output of the A/D as the control input to the sample-and-hold amplifier. This source of jitter is eliminated when the system clock directly initiates the sample-to-hold control (see Fig. 2). Buffering (immediately adjacent to the MP271) is suggested to provide the very fast rise time (5 ns) required by the control input.

The high impedance ($10^8\ \Omega$ in parallel with 10 pF) of the MP271 make it ideal as a buffer for the output of CMOS or FET analog multiplexers. Voltage divider error, caused by multiplexer switch ON resistance in series with the input impedance, is negligible.

The low droop rate (2 μV/μs) of the MP271 holds its output constant, even with 16-bit converters. On a 10V full scale range, a 16-bit ADC such as the Analogic MP8016, has an LSB of 153 μV. For the MP271 to discharge less than ½ LSB (at 2 μV/μs) the conversion must be completed in less than 39 μs, which is well within the limits of the MP8016.

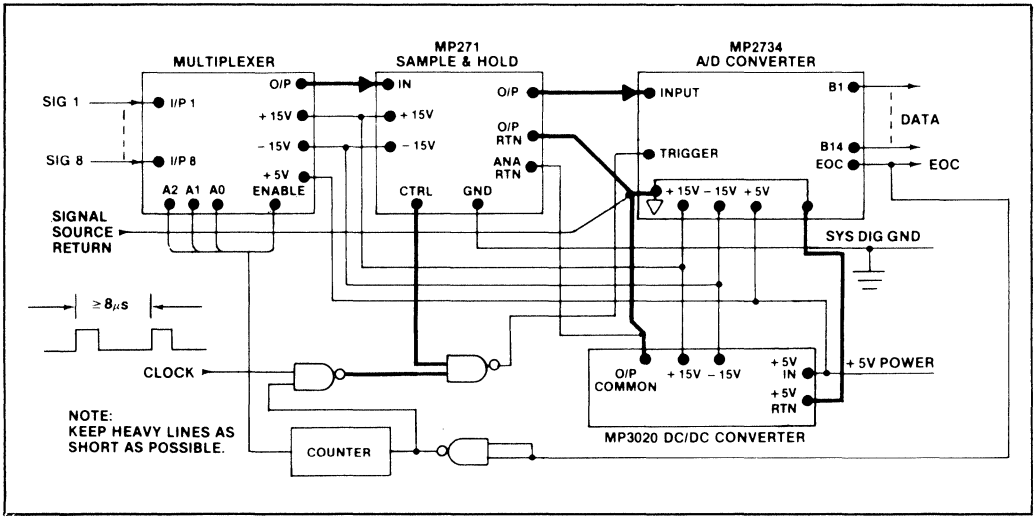


Figure 2. High Accuracy, High Resolution, 125 kHz 14-Bit Data Acquisition System Using the MP271.

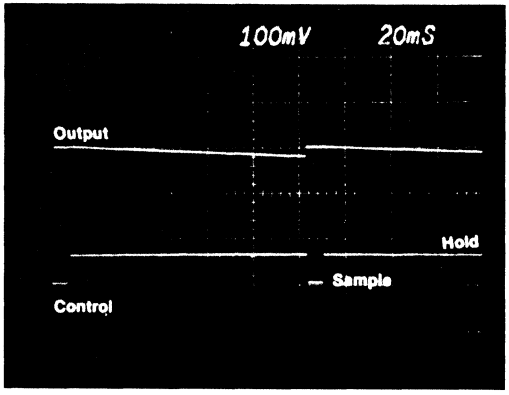


Figure 3. MP271 Output Showing Sample-to-Hold Switching Illustrating Low Droop Rate. Performance Limit is Two Divisions Vertically On Upper Trace (200 mV/100 ms).

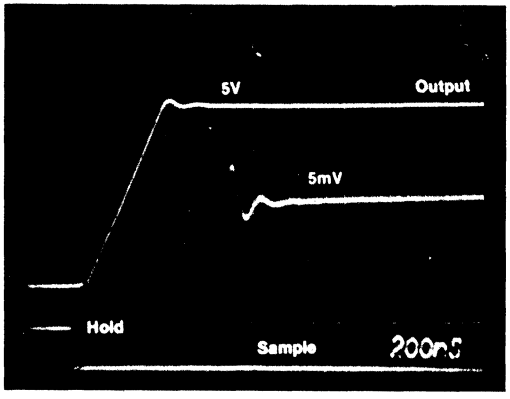


Figure 4. MP271 Output Acquiring 20V Step Input. Upper Trace Shows Slew Rate of 50 V/μs at 5V/Division. Lower Trace Shows Acquisition Time of 800 ns to 0.01% at 5 mV/Division.

Theory of Operation

The exceptional performance of the MP271 results directly from its unique combination of design features. As shown in the simplified block diagram of Fig. 5, the MP271 is basically, three circuits: 1) a voltage-to-current (V/I) source amplifier, 2) an output amplifier/integrator, and 3) a switching circuit.

When the MP271 is in the sample mode (switches S1 and S3 are open, S2 and S4 are closed, and control is at logic "0") the circuit functions as a unity gain follower with the voltage across the holding capacitor (C1) forced to equal the input voltage. The maximum acquisition time of only 1 μs (to 0.01% of final value) results from using a small value of C1, high speed amplifiers, and very fast switch drivers in addition to the high-power current source amplifier (V/I). Switching and non-linearity errors are held to a minimum by placing the switching circuits and the current source within the over-all feedback loop.

In the hold mode (switches S1 and S3 closed, S2 and S4 open, and control at logic "1") the holding capacitor (C1) is part of the low leakage integrator. The discharge rate is slow enough to limit the droop to less than ½ LSB. High input/output isolation is guaranteed by opening the input to C1 with S4; opening the feedback loop with S2; and at the same time shorting the V/I inputs through S1 and grounding its output with S3. A 20V p-p, 500 kHz sinusoidal input to the MP271 is typically attenuated by 100 dB.

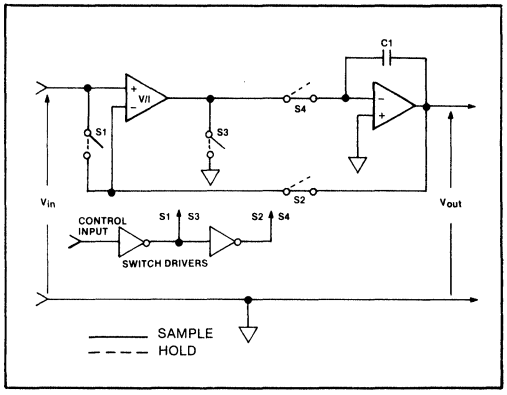


Figure 5. MP271 Simplified Block Diagram.

Adjustments

Provision is made to adjust the input offset voltage of the MP271 to zero externally by connecting a 200Ω potentiometer as shown in Fig. 6. To adjust, short the input to analog return, connect the control input to ground (placing the MP271 in the sample mode), and set the offset potentiometer for zero output from the MP271.

It is virtually impossible to avoid capacitance coupling between the switch drivers and the hold capacitor (C1), which results in a small charge being dumped onto C1 when switching from sample to hold. This produces an offset, or pedestal, at the output which is mode

dependant. The MP271 includes an internal pedestal offset adjustment control. To adjust, short the input to analog return, switch the control input between sample and hold (a 50% duty cycle at 200 kHz is convenient), and set the pedestal control for zero output during the hold mode period.

The gain of the MP271 is typically within ±300 μV of nominal ±10V output. Provision for gain adjustment is not included. The small gain error of the MP271 may be compensated via the gain adjustment potentiometer on the ADC following the sample-and-hold amplifier.

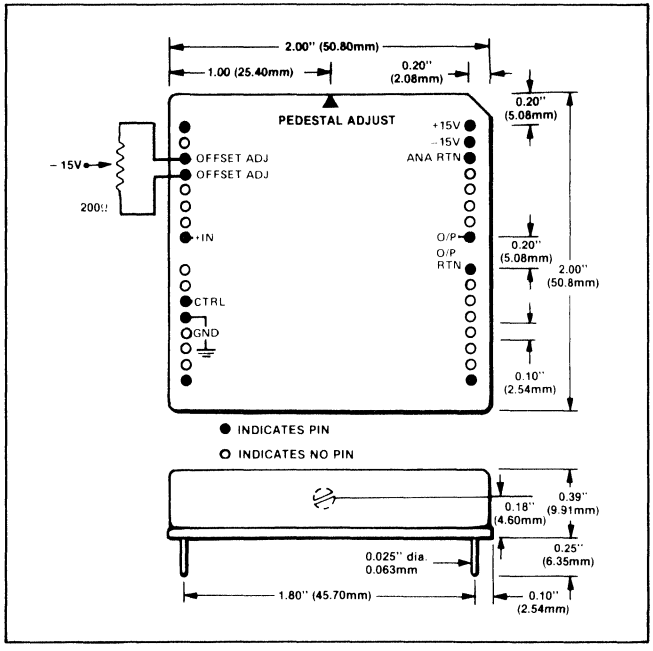
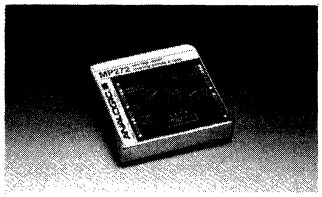


Figure 6. MP271 Mechanical Outline and Offset Adjustment.

ORDERING GUIDE

Specify **MP271**



ANALOGIC®

MP272

Very High Speed High Accuracy Inverting Sample-and-Hold

Description

The Model MP272 is an inverting sample-and-hold (S/H) amplifier module with an unprecedented combination of high speed and high accuracy at low cost. Its maximum time for acquiring a 10V input step to ±0.01%, including the settling time of its input buffer, is only 300 ns (350 ns max. for a 20V step). This is faster than the "typical" acquisition time specified by many other manufacturers who frequently neglect the input buffer amplifier settling time.

The aperture uncertainty time of the MP272 is only 50 ps and its hold mode droop rate is 5 μV/μs max.; each of these values is one-half to one-fifth of the corresponding specifications published for a variety of other high-speed models. These specifications translate directly into correspondingly greater overall system accuracy. Available at prices equal to or lower than those of less accurate models, the MP272 delivers the optimum S/H performance for transient analyzers, digital oscilloscopes, and other high-speed systems requiring up to 12-bit resolution.

The Model MP272 includes a unity-gain input buffer amplifier with 100 MΩ input impedance and a low 150 pA bias current. This stage is followed by a low output impedance, switch-controlled stage that acts as

(continued)

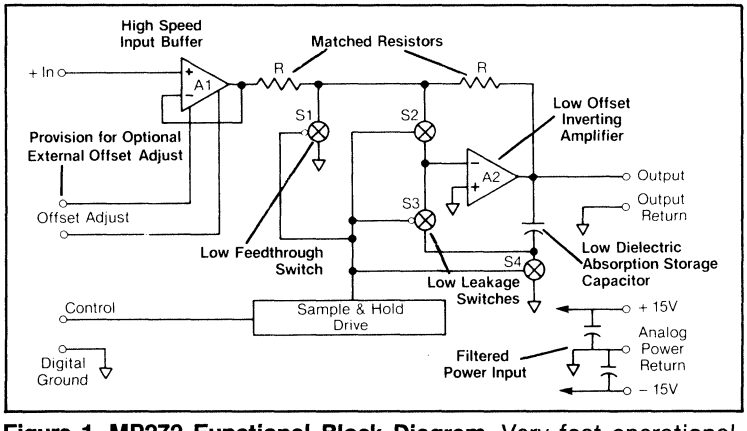


Figure 1. MP272 Functional Block Diagram. Very fast operational amplifiers provide a 200 ns typical acquisition time to 0.01% for a 10V step.

Features

- **High Speed**
  200 ns typ. acquisition time for a 10V step *(including input buffer settling time)*
  5 ns aperture time, typ.
- **High Sampling Accuracy**
  ±0.005% FSR non-linearity, max. 50 ps aperture uncertainty upon transition to HOLD, typ.
- **Exceptionally Low Bias Current**
  150 pA max. @ 25°C
- **High Holding Accuracy**
  5 μV/μs droop rate, max. @ 25°C
  ±0.005% FSR offset non-linearity, max.
- **Low Dielectric Absorption**
  0.005% of voltage change per microsecond of hold time
- **Wide Bandwidth**
  (in sample mode)
  15 MHz small signal bandwidth (–3 dB)
  3 MHz full power bandwidth
- **Low Noise**
  200 μV rms (10 MHz) max., in both SAMPLE and HOLD
- **System Oriented**
  Drives large capacitive load
  Consumes only 1.5 Watts
  Includes holding capacitor and provisions for optional external offset adjust
- **Offers superior performance at low cost**

Applications

- **Digital Oscilloscopes**
- **Transient Analyzers**
- **Automatic Test Equipment**
- **High Speed Data Acquisition Systems**
- **Digital Signal Processors**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

SAMPLE MODE

Input Voltage Range (FSR)
±10V (±V_{supply} without damage)

Gain
−1

Gain Accuracy
±0.01% max. @ 25°C (10 ppm/°C max. tempco)

Non-linearity
±0.005% FSR max.

Settling Time:
to within ±0.01% of 10V input step—
200 ns typ., 300 ns max.
to within ±0.01% of 20V input step—
250 ns typ., 350 ns max.

Small Signal Bandwidth (−3 dB)
15 MHz typ.

Full Power Bandwidth
3 MHz typ.

Slew Rate
200 V/μs, min.

Input Impedance
100 MΩ||5 pF typ.

Input Bias Current (@25°C)*
150 pA max.

Input Offset Voltage (@25°C)
±10 mV max.

Offset Tempco
±100 μV/°C max.

Offset vs. Supply
200 μV per 1% change in supply voltage, max.

Noise (10 MHz bandwidth)
200 μV rms max.

SAMPLE-TO-HOLD SWITCHING

Aperture Time
5 ns typ.

Aperture Uncertainty
50 ps typ.

Switching Transient Settling Time (to ±0.01% of FSR)
150 ns max.

HOLD MODE

Output Voltage Range
±10V

Maximum Load
2 kΩ||50 pF

Droop Rate (@25°C)*
5 μV/μs max.

Dielectric Absorption
0.005% of voltage change @ 0.3 μs sample time, 1 μs hold time typ.

Hold Offset (Pedestal) @ 25°C
±0.5 mV typ., ±2 mV max. (optionally adjustable to zero)

Hold Offset (Pedestal) Tempco
±40 μV/°C max.

Hold Offset Non-linearity
±0.005% FSR max.

Voltage Feedthrough Rejection Ratio (10V Input Step)
84 dB typ., 78 dB min.

Output Voltage Variation due to Control Pulse Variation
1 mV per volt of change in control signal max.

Noise (10 MHz Bandwidth)
200 μV rms max.

HOLD-TO-SAMPLE SWITCHING

Acquisition Time:
to within ±0.01% of 10V input step—
200 ns typ., 300 ns max.
to within ±0.01% of 20V input step—
250 ns typ., 350 ns max.

DIGITAL CONTROL INPUT

Logic Type
TTL compatible, 1 unit load

Sample
Logic "0" (+0.4V max.)

Hold
Logic "1" (+3V min.)

Required Rise Time
5 ns max. to obtain min. aperture time

POWER SUPPLY (Exclusive of Load)

+15V ±3%
50 mA typ.

−15V ±3%
50 mA typ.

ENVIRONMENTAL & MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Modupac™ Dimensions
2" x 2" x 0.44" (50.8 x 50.8 x 11.2 mm)

Electrical Shielding
Electrostatic 6 sides; electromagnetic 5 sides

* Doubles approximately every 10°C

Description (cont.)

a unity gain inverting amplifier in the sample or follow mode, and as a memory circuit in the hold mode. The low 5 μV/μs droop rate in the hold mode ensures high measurement accuracy, even when used with a relatively slow analog-to-digital converter.

The module accepts a full scale input voltage of ±10V. Output gain accuracy is ±0.01% with a maximum non-linearity over the full range of less than ±0.005%. Noise level is maintained at less than 200 μV rms over a 10 MHz bandwidth. The hold mode offset is typically less than ±0.5 mV and is externally adjustable to zero. A combination of precision matched resistors and low temperature coefficient circuit components limits offset temperature coefficient to less than ±40 μV/°C.

Dielectric absorption error, commonly neglected or not even recognized by other manufacturers, is minimized in the MP272 by the use of an extremely high quality "hold" capacitor. As a result, the error, assuming 0.3 μs sample and 1 μs hold times, is typically 0.005% of voltage change, by actual measurement!

Even under worst case conditions, aperture time of 5 ns aperture uncertainty of 50 ps and switch settling time of 100 ns, the MP272 still allows up to 700,00 samples per second using a 1 μs A/D converter. Figure 2 shows acquisition time of a typical unit when a 20V step is applied. The 140 ns acquisition time obtained is well within the 250 ns typical specification.

This compact module is enclosed in a metal case, 2" x 2" x 0.39" (50.8 x 50.8 x 9.9 mm), that provides electrostatic shielding on all six sides and electromagnetic shielding on five. Its power consumption of 1.5W is approximately half that of some earlier S/H models, resulting in significantly lower internal operating temperatures, thereby improving reliability. Delivering the rated performance over a 0°C to 60°C temperature span, with a relative humidity up to 85%, the Model MP272 provides the highest speed-with-accuracy performance available for a wide variety of applications.

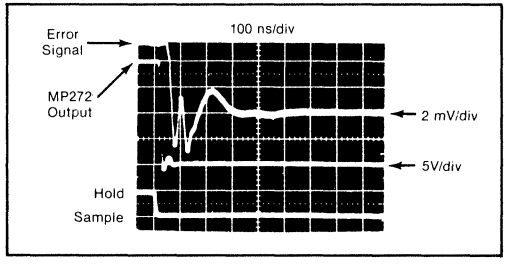


Figure 2. MP272 Acquisition of a 20V Input Step. The middle trace shows a slew rate of 1000 V/μs. The upper trace shows acquisition, to within 2 mV (0.01% of final value), in 140 ns. Thus, this typical unit's speed is appreciably better than the specified value.

TYPICAL TIMING AND APPLICATION

General Timing Usage

Figure 3 shows a typical timing diagram for controlling the MP272 in multiplexed systems. The conversion time of the analog-to-digital converter used may be inserted in the time line shown, yielding the sampling period for a specific application. Note that in addition to the MP272's fast acquisition time, its low settling time upon switching from SAMPLE to HOLD contributes to its high throughput rate capability.

Typical High Speed Multiplexed Data Acquisition System

The Model MP272's speed and accuracy provide several system advantages, even in applications not usually considered as "high speed". For example, a typical industrial process control system may be required to monitor numerous process parameters, most of which do not ordinarily change rapidly. Nevertheless, consideration of overall system throughput rate and processor utilization may dictate a need for high speed sampling, possibly in bursts. In addition, the higher the accuracy of each measurement made, the more precisely, and therefore economically, is the process controlled.

Figure 4 shows how the speed and accuracy of such a process control application are optimized with the Model MP272 Sample-and-Hold. The grounding and power distribution method shown is appropriate to nearly all high precision applications.

Use of a 12-bit analog-to-digital converter with differential non-linearity of ± ½ LSB max. is recommended. To maximize throughput rate, a multiplexer is switched to each succeeding channel simultaneously with selection of the HOLD mode for the current channel (Figure 3). This allows time for multiplexing transients

to settle prior to the converter's first bit decision. When the system is ready to convert the next channel, no "waiting" time is expended for channel switching. The next channel, already connected to the MP272, can be acquired to 0.01% in 300 ns max. (10V step).

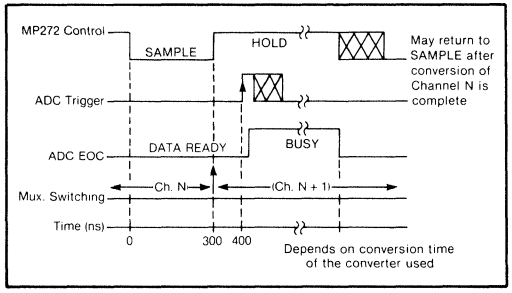


Figure 3. Typical Timing For A High Speed Multiplexed Data Acquisition Subsystem Using the MP272 S/H.

Aperture Uncertainty Effects

For any sampled data process, uncertainty in the time of taking a sample results in an equivalent amplitude error for a signal of frequency f. The uncertainty, ΔT, includes system clock jitter and S/H aperture uncertainty. The error due to ΔT may be stated as rms %FSR error = 222 x f(Hz) x ΔT(s). With ΔT = 50 ps for the MP272, assuming use of a jitter-free CONTROL input and a sufficiently fast analog-to-digital converter, signals having frequency content approaching 1 MHz may be measured with less than ±0.012% FSR rms aperture uncertainty error.

For applications requiring the maximum system accuracy, it is recommended that a crystal-controlled oscillator and fast rise time logic (5 ns max.) be used to generate a jitter-free CONTROL input. The end of conversion (EOC) output from the analog-to-digital converter used may have significant jitter relative to 50 ps. For this reason, in many applications, it should not be fed back directly as the MP272 CONTROL input. Rather, it is recommended that the EOC signal be used to gate the jitter-free clock to the MP272.

Offset Adjustment

As shown in Figure 5, the MP272 may be adjusted to compensate for any S/H offset and for system offsets common to all channels that are sampled through the installed S/H unit.

1. Connect a 20 kΩ potentiometer to the S/H trim terminals and its wiper to the −15V supply.
2. Sample a channel with a zero voltage input.
3. Issue a train of SAMPLE and HOLD commands per the system usage timing, via the CONTROL input.
4. Adjust the trim potentiometer for zero voltage, during the HOLD mode, at the S/H output.

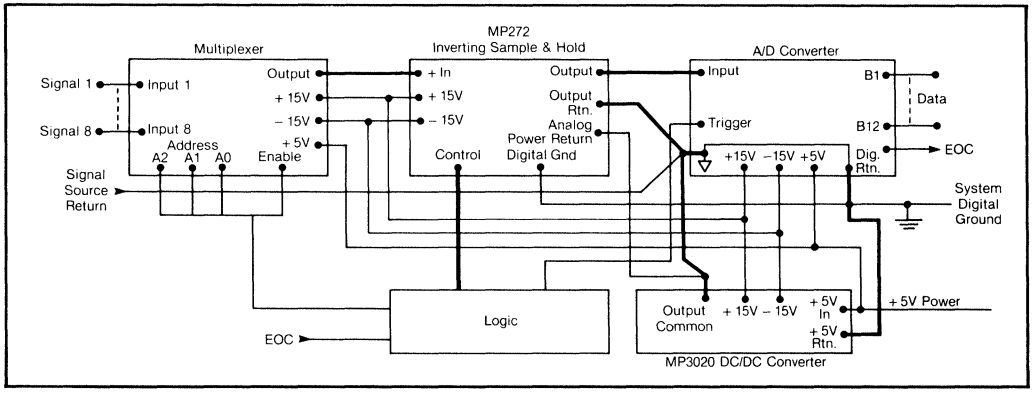
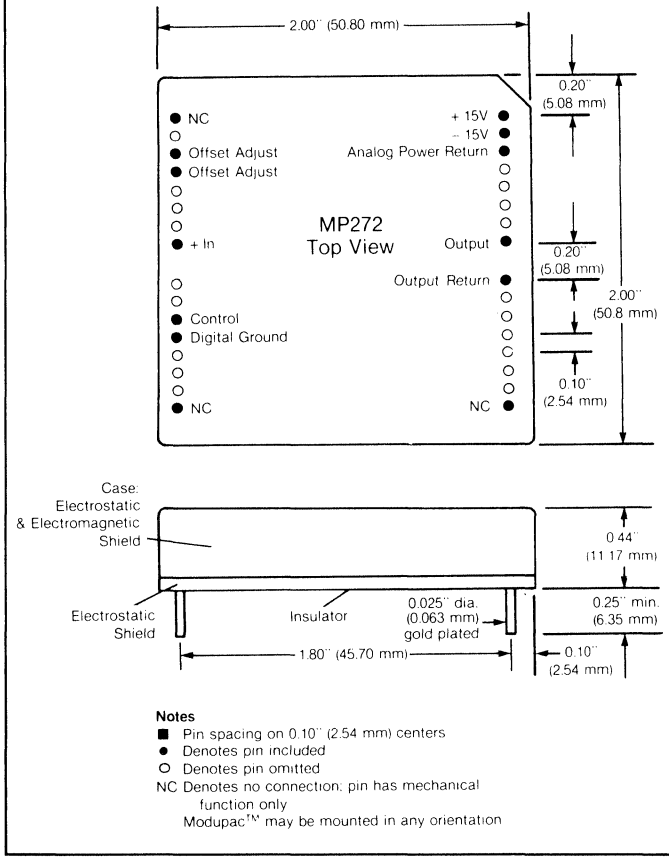


Figure 4. Typical High Accuracy, 12-bit Data Acquisition System. The grounding, control, and power distribution layout shown minimizes ground loop and other error effects. Keeping interconnections shown in heavy line as short as possible will help ensure system accuracies that are fully consistent with the MP272's high precision.

MOUNTING DIMENSIONS & PINOUTS



Notes
- ■ Pin spacing on 0.10" (2.54 mm) centers
- ● Denotes pin included
- ○ Denotes pin omitted

NC Denotes no connection; pin has mechanical function only

Modupac™ may be mounted in any orientation

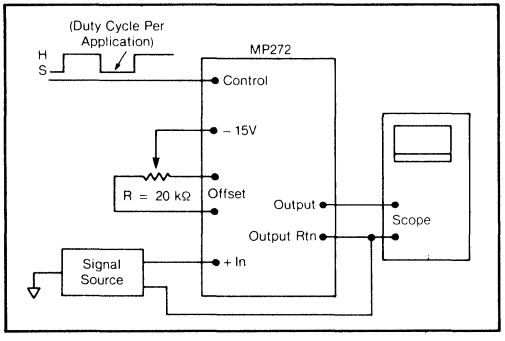
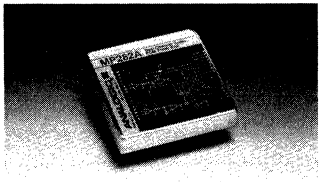


Figure 5. Optional External Offset Adjustment Set-Up.

ORDERING GUIDE

Specify ☐ **MP272**



ANALOGIC®

MP282A

Dual-Channel Audio PCM Front End

Description

The Analogic MP282A is a high-speed dual-channel sample-and-hold module with built-in multiplexer and automatic gain-ranging amplifier. Optimized for professional audio recording and designed specifically to increase the dynamic range and improve the performance of audio bandwidth analog-to-digital conversion, it also offers a low priced alternative to previously available equipment for converting audio bandwidth signals to digital words for such wide-dynamic range applications as vibration analysis, spectrum analysis, seismic exploration and sonar systems.

To achieve the high performance standards required for high fidelity audio recording, signal conversion equipment must yield 16 bits of dynamic range and low harmonic distortion at high sampling rates. The MP282A, when connected to a 15-bit analog-to-digital converter (ADC), such as Analogic's MP2735-2, meets all the analog function requirements of professional audio recording at relatively low cost. Its one bit of automatic gain ranging (see Figure1) allows a 15-bit ADC to give a total of 16 bits of dynamic range (98 dB), eliminating the need for high-cost 16-bit ADCs. Figure 2

(continued)

Features

- **Automatic 1-bit Gain Ranging**
- **Dual or Single-Channel Sampling**
- **High-Speed Sampling**
  (with MP2735)
  111 kHz single channel
  55 kHz dual channel
- **Built-in Multiplexer**
- **Wide Dynamic Range**
  98 dB (with 15-bit A/D converter)
- **Low Harmonic Distortion**
  – 86 dB
- **Low Crosstalk** – 86 dB
- **Low Noise**
  – 98 dB at 20 kHz bandwidth
- **Low Aperture Uncertainty**
  less than 0.4 ns

Applications

- **Multitrack PCM for professional audio recording**
- **Self-contained Record and Playback**
  (PCM adaptors for video cassette recording)
- **Vibration Analysis**
- **Spectrum Analysis**
- **Seismic Exploration**
- **Sonar Systems**
- **Spectroscopy**

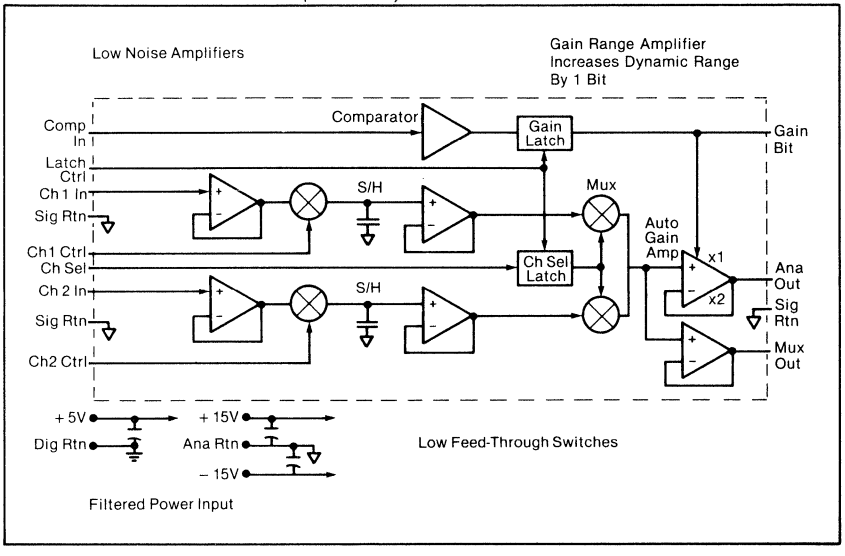


Figure 1. MP282A Functional Block Diagram.

SPECIFICATIONS

ANALOG INPUTS

Number of Inputs
2 channels

Full Scale Linear Range
($\pm 5V$ $\pm V_{supply}$ without damage)

Input Impedance
10 MΩ//10 pF with input connected as voltage follower

Input Bias Current
0.5 μA typ.

Comparator Input Impedance
12 kΩ

ANALOG OUTPUT

Number of Outputs
1 channel

Full Scale Linear Voltage Range
±5V

Output Impedance @ dc
0.1Ω

Load
2 kΩ min. & 100 pF max.

Protection
Short circuit to ground

Multiplexer Out[1]
Same characteristics as above

TRANSFER CHARACTERISTICS[5]

Full Power Bandwidth (sample mode)
150 kHz typ.

Slew Rate (sample mode)
6 V/μs typ.

Crosstalk[2]
−86 dB max.

Gain, Referred to Input (RTI)
+1 or +2

Sample and Hold Acquisition Time[3]
3.5 μs max.

Aperture Delay Time
50 ns typ.

Aperture Uncertainty
0.4 ns typ.

Channel Select Multiplexer Settling Time[3]
2.0 μs max.

Auto Range Amplifier Settling Time[4]
1.5 μs max.

Sampling Rates (with MP2735-2 ADC)
2 Channels
57 kHz max.

1 Channel
105 kHz max.

ACCURACY AND STABILITY[5]

Harmonic Distortion
−86 dB max. (see Fig. 2)

Gain Accuracy (0°C to 60°C)
±0.1% max.

Offset Voltage (0°C to 60°C)
20 mV max. RTI

Noise (shorted input, 20 kHz bandwidth)
−98 dB RTI referred to rms full scale

Droop Rate at 25°C (doubles every 10°C)
0.05 μV/μs, typ.; 0.4 μV/μs, max.

Linearity
±0.002% FSR, max.

DIGITAL INPUTS

Logic Type
TTL

Control Channel 1 and Channel 2
2 lines

Sample Mode
TTL Low

Hold Mode
TTL High

Required Rise Time
10 ns max.

Channel Select
1 line

Channel 1
TTL High

Channel 2
TTL Low

Latch Control
1 line

Transparent
TTL High

Latches
High to low transition

Latch Control Simultaneously Affects Channel Select and Gain Output

DIGITAL OUTPUT

Gain Output (controlled by latch)
1 line

Gain @ +1
TTL Low

Gain @ +2
TTL High

POWER, MECHANICAL, ENVIRONMENTAL

Analog Power Supplies[6]
±12V to ±15V @ 35 mA, typ. tracking @ ±1%

Digital Power Supply[6]
+5V ±5% @ 10 mA, typ.

Operating Temperature Range
0°C to 60°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
0 to 85%, non-condensing to 40°C

Modupac™ Dimensions
2" X 2" X 0.44" (50.8 X 50.8 X 11.2 mm)

Electrostatic Shielding
6 sides

Electromagnetic Shielding
5 sides

Case Potential
Ground

Notes:
1. User must connect comparator input with multiplexer output to enable gain ranger.
2. Over the frequency range of 20 kHz and inputs at 0 dB (FS) to −15 dB measured as the peak line by a spectrum analyzer with 100 Hz bandwidth.
3. To ±0.005% final value.
4. Measured from high-to-low transition of latch control input.
5. Unless otherwise specified, these specifications apply at 25°C and with each input amplifier connected as a voltage follower.
6. Analog Power return, digital return and signal return are not internally connected.

Description (cont.)

shows the broad signal range over which the MP282A, with Analogic's MP2735-2 ADC, maintains low harmonic distortion.

The MP282A's sampling versatility makes it suitable for several applications. Its low crosstalk (−86 dB) multiplexer enables one ADC to accept data from two channels (for a stereo system). Samples from each channel can be taken simultaneously (at 55 kHz sampling frequency), essential for multitrack pulse code modulation (PCM) recording. The dual channel capability halves the number of ADCs necessary for multitrack recording, substantially reducing total analog function costs. Where higher speed sampling from a single channel (such as for vibration analysis) is required, sampling rate can reach 111 kHz.

Furthermore, the MP282A S/H features low noise (−98 db) and low jitter or aperture uncertainty (less than 0.4 ns), critical parameters in S/H circuits for audio applications. The low cost MP282A audio PCM front end thus features the wide dynamic range, low noise, low sampling uncertainty and low harmonic distortion at high sampling rates, required for professional quality audio recording and other similar applications.

PRINCIPLES OF OPERATION

Automatic Gain Ranging

The MP282A's automatic gain ranging amplifier increases the dynamic range of an associated ADC by one bit, boosting the output of a 15-bit converter to 16 bits (98 dB dynamic range). The following equation* gives dynamic range as a function of bits:

where n = number of bits,

$$\text{dynamic range} \approx 1.76 + 6.02\ \text{ndB}$$
$$= 1.76 + 6.02(16)\ \text{dB}$$
$$= 98.08\ \text{dB}$$

The MP282A accomplishes this gain ranging by sensing the magnitude of the signal passing from the multiplexer to the ADC (refer to Figure 1). When the input is equal to or greater than approximately ½ full scale, the signal is amplified by a gain of 1. When the input is less than approximately ½ full scale, the MP282A applies a gain of 2. The state of the gain range bit appears as a digital signal or binary exponent for shifting the ADC output word.

The latch control holds a particular gain setting constant for the duration of the conversion time. (The same latch input is also used to control the channel select for sequential sampling.)

S/H Mode Control Lines

Each of the two S/H circuits of the MP282A is controlled by an external command, permitting simultaneous or consecutive dual-channel sampling, or single-channel sampling. For simultaneous sampling, the signal from one channel remains in the hold mode, while the other passes through the multiplexer, gain-ranger and converter. When conversion of one signal is complete, the other is multiplexed, gain-ranged and converted.

*For further discussion, please refer to *The Analogic Data-Conversion Systems Digest*, "Some Considerations in the Design of Wide Dynamic Range Audio Digitizing Systems," by Robert Talambiras.

Channel Select Line

The multiplexer used in the MP282A allows a single ADC to time-share samples from two S/H circuits, enabling simultaneous recording for a stereo system. The multiplexer control line, which determines whether channel 1 or 2 will be applied to the gain range amplifier, is enabled when the latch input is high and is latched on the high-to-low transition of the latch input.

Gain Output

The logic which triggers the gain bit in the MP282A relies on a comparator (refer to Figure 1); an unknown input is compared with a locally generated reference which marks nominal 1/2 full scale, acting as a trip point. An internal Zener diode regulates the trip point for symmetrical power supply voltages from ± 12V to ± 15V. The trip point has been set nominally lower than ½ full scale so that scaling action never takes place at a critical point, even when normal tolerances are taken into account.

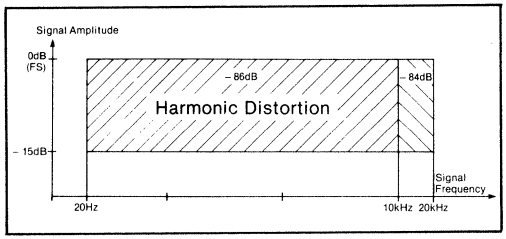


Figure 2. Harmonic Distortion of MP282A and 15-bit A/D Converter: no more than – 84 dB below signal for sampling frequencies of 50 kHz, within signal magnitude/frequency range shown.

Applications of the MP282A in Tandem with a High-Speed A/D Converter

The MP282A's sampling versatility makes it suitable for a wide range of applications, from multitrack audio PCM systems, to self-contained record and playback systems, to high-speed vibration analysis systems. Analogic's SHAD-2 card (see Figure 3) is especially designed to meet the 16-bit dynamic range, high speed, low distortion requirements of these audio applications. The SHAD-2 combines the MP282A and the MP2735-2 15-bit ADC with the logic for automatically shifting the mantissa and achieving 16-bit dynamic range (please refer to SHAD-2 and MP2735 data sheets, available from Analogic Corporation).

For Multitrack Audio PCM

Because professional audio studios perform multitrack recording, taking signals from separate microphones, adjusting them according to desired tonal quality and mixing them for the final product, signal sampling must occur at precisely the same time for each channel. The MP282A, with a high-speed ADC such as the MP2735-2, allows for simultaneous dual-channel sampling at high speed (57 kHz, see Figure 4). This is enabled by short acquisition time (3.5 μs), short multiplexer settling time (2 μs), fast auto range amplifier settling time (1.5 μs) and short ADC conversion time (5.5 μs).

For Single-Channel Sampling

Where single-channel sampling is required, the MP282, in tandem with a high-speed ADC, offers high-speed sampling at 105 kHz (see Figure 5) suitable for vibration and spectrum analysis.

The MP282A dual-channel audio PCM front end and MP2735-2 ADC combine with Analogic's MP1926A 16-bit digital-to-analog converter and MP201A audio distortion suppressor to form a complete data conversion system, offering the exceptional end-to-end accuracy required by the audio engineer at relatively low cost. For more information, please send for data sheets on each of these products.

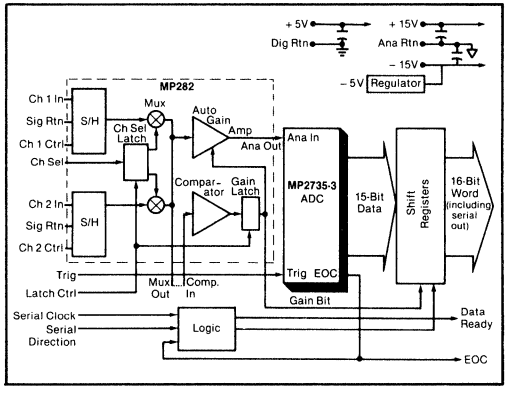


Figure 3. MP282A Application on SHAD-2 Card.

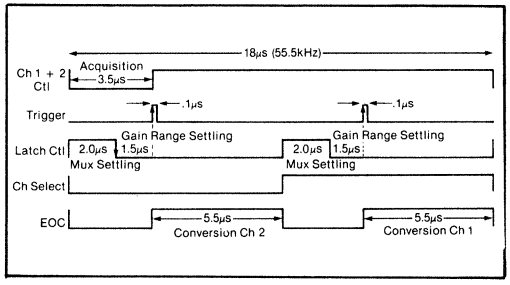


Figure 4. Timing Diagram for Simultaneous Sampling.

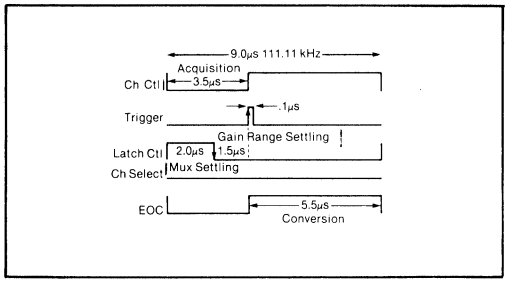
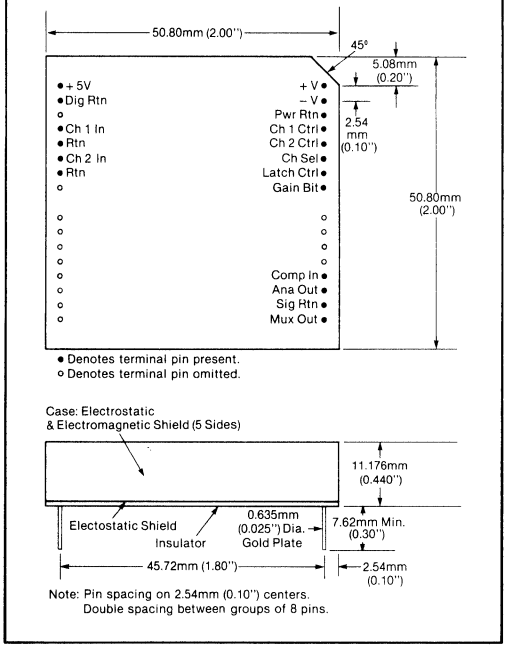


Figure 5. Timing Diagram for Single Channel Sampling.

MOUNTING DIMENSIONS & PINOUTS



ORDERING GUIDE

Specify **MP282A.**

ANALOGIC®

SECTION 4

Analog-to-Digital Converters

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SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
High Accuracy (±0.00075% to ±0.006% FSR)	High Speed	Stability, Diff. Input Amp. (internal-optional)	MP8016 MP8015 MP8014	4-43 4-43 4-43
		Low Harmonic Distortion Wide Dynamic Range	MP2735-2 MP2735-1	4-37 4-37
		Good Overall Performance	MP2734 MP2714C	4-31 4-25
	Low Speed	External Accuracy, Integrating	MP8037	4-49
		Fully Isolated, Floating, Integrating, High CMRR Programmable Gain	MP2316	4-11
Moderate Accuracy (±0.01% to ±0.1% FSR) Moderate Resolution (8- to 13-Bits)	High Speed	Good Overall Performance	MP2713C MP2712D	4-25 4-25
	Low Speed	High CMRR, Binary Output	MP2321	4-21
		High CMRR, BCD Output	MP2322	4-21

ANALOG TO DIGITAL CONVERTERS

ABSOLUTE ACCURACY A measure of the the largest static difference between the actual output code and that predicted by the ideal transfer function, expressed as a percentage of full scale. In the case of a bipolar input range, e.g., −10V to +10V, the absolute accuracy is computed as a percentage of the the full range, or 20V. Absolute accuracy measurements must reference a voltage standard traceable to the NBS with at least an order of magnitude lower uncertainty than the difference represented by one LSB.

A/D or ADC An Analog to Digital Converter is a device that accepts an analog input signal and generates the corresponding digital output code determined by its transfer function. The ideal output is accurate to ±0.5 LSB as shown by the quantizing error curve in Figure 1. A black-box representation of an ADC is shown in Figure 2. There are a number of different ADC architectures in use. Two of the most popular are the successive approximation ADC and the integrating ADC. Speed is an inherent advantage of the successive approximation ADC. In other respects, including cost and reliability, the integrating ADC is generally superior.

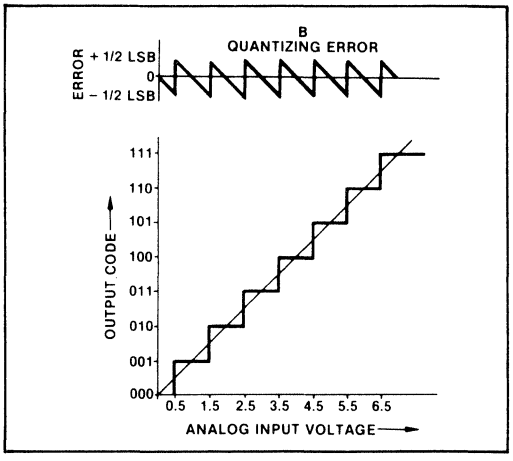


Figure 1. Theoretical Transfer Function of an ADC (first three LSBs only).

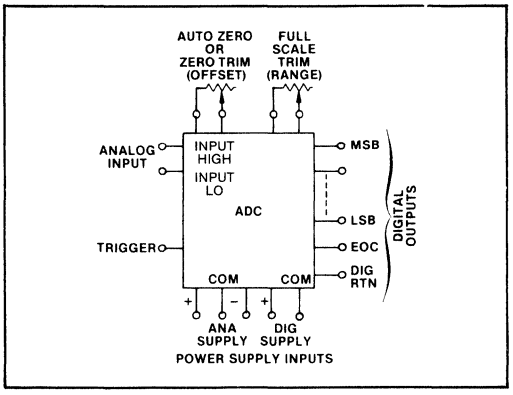


Figure 2. "Black Box" Representation of an ADC.

CMRR The Common-Mode Rejection Ratio is a measure of the ability of an ADC with a balanced differential input to attenuate signals common to both the INPUT HI and the INPUT LO lines. See Figure 3 for configuration and formulae used to calculate CMRR.

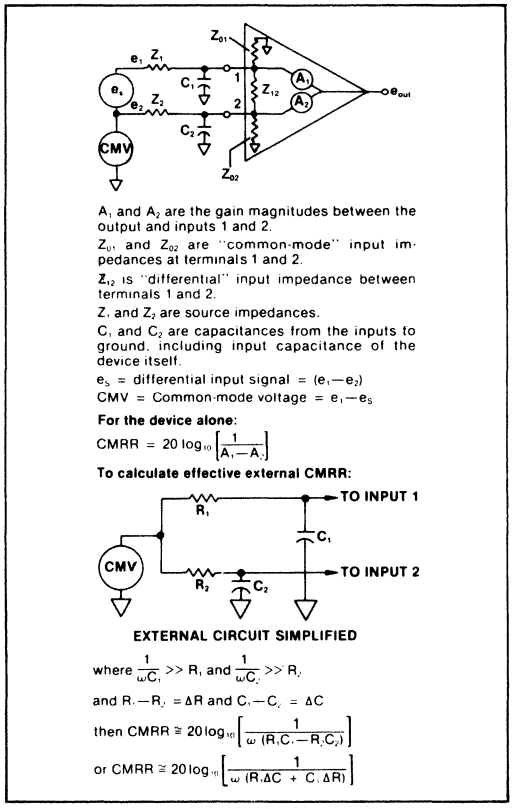


Figure 3. Common-Mode Rejection Configurations and Basic Formulae.

CONVERSION TIME The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant.

DIFFERENTIAL LINEARITY A parameter that measures the difference between the theoretically uniform voltage bandwidth corresponding to a given code and the worst case actual voltage bandwidth for a given code. It is expressed either as a percentage of the ideal voltage bandwidth or as a fraction of an LSB. Figure 4 demonstrates differential linearity.

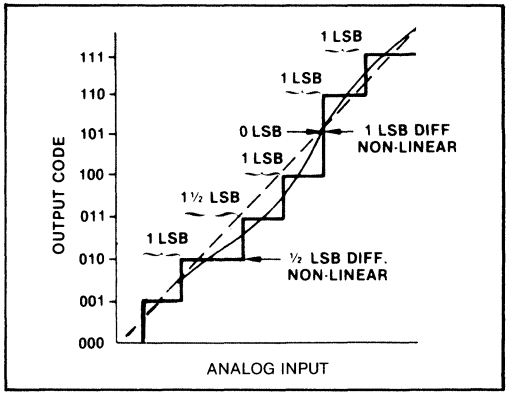


Figure 4. Differential Linearity.

GAIN The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

INTEGRAL LINEARITY A measure of how closely the actual transfer function of the ADC adheres to the ideal (straight line) transfer function.

INTEGRATING ADC The integrating ADC uses a converter architecture with inherent advantages over successive-approximation including: lower cost for a given resolution, accuracy, linearity and stability; inherent monotonicity; high NMRR; true averaging of the signal during conversion; and the ability to autozero before every conversion cycle. The only real disadvantage is speed.

As Figure 5 shows, the conversion is accomplished in two integration phases. Because of this it is often called a "dual slope" integrating converter. Operation is as follows:

1) In the first phase of the conversion a clock pulse generator is started and the unknown analog input signal, E_{in} charges the integrator for a fixed time interval, N_s. At the end of the time interval the charge on the integrator is proportional to E_{in}.

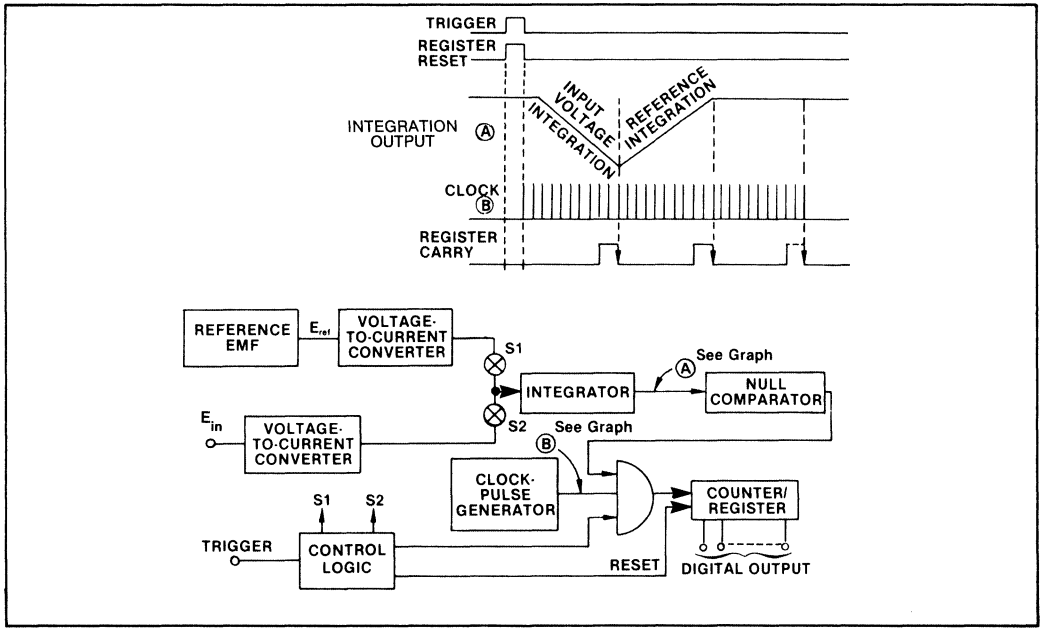


Figure 5. Fundamental Block and Timing Diagrams of Dual-Slope Integrating A/D Converter.

2) In the second phase the clock is reset and an internal standard reference voltage of opposite polarity, E_{ref}, is substituted for the input signal. This discharges the integrator, at a known rate, to zero. The time it takes to discharge the integrator, N_R, is proportional to the input signal: $N_R = (E_{in} / E_{ref}) \times N_s$

Since E_{ref} and N_s are fixed by the design, N_R will be linearly proportional to E_{in} and can be easily scaled to read directly.

As long as the components of the integrator and the clock-counter have good short-term stability, changes in their values do not decrease accuracy because both charging and discharging are affected to the same degree.

Integrating converters have a zero offset error which can be corrected by an autozeroing function. This is done by shorting the input electronically between conversions and storing the resultant integrator output on a capacitor. This stored voltage is fed back during conversion. A dual-slope integrating converter with autozeroing is called a "three-phase" or "three- step" converter: 1) autozero; 2) ramp up; 3) ramp down.

ITERATIVE ADC This uses an architecture that achieves high speed throughput approaching that of a flash converter with high (14 to 16 bit) resolution and relatively lower cost.

Figure 6 shows a very high speed, 15-bit resolution iterative converter. It uses a very fast, ultra-stable, 8-bit successive approximation ADC; the first 8 MSB's of an ultralinear, high speed 16-bit DAC; and some switch-control logic. The sequence of operation is as follows:

1) The input signal is first converted to an 8-bit digital code by the ADC.

2) The output of the ADC provides the high-order 8 bits. The output is also fed into the first 8 MSB's of the DAC where it is converted back to analog.

3) The output of the DAC is subtracted from the the input to the ADC.

4) The ADC performs a conversion on the difference to provide the low-order 8 bits.

5) The result of the first conversion is moved to the first 8 MSB's of the output register.

6) The result of the second conversion is moved to the 8 LSB's of the overlapping adder. The output register now contains the 15-bit converted result.

MONOTONICITY Is a characteristic that describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

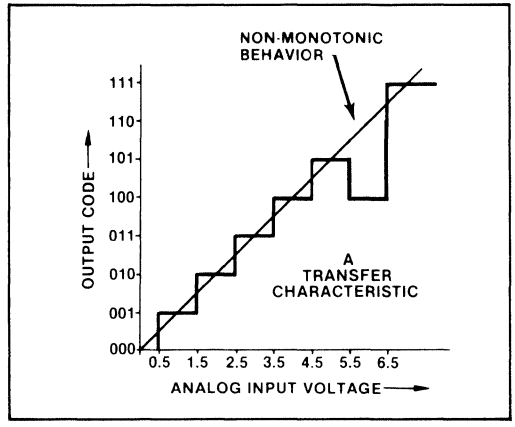


Figure 7. Non-Monotonic Behavior.

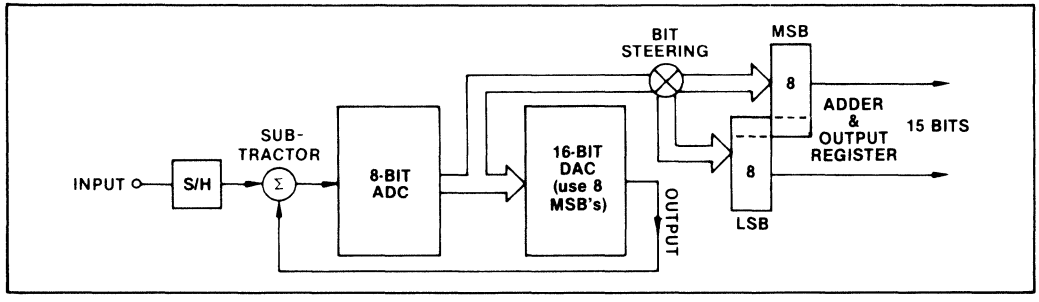


Figure 6. Iterative A/D Converter Architecture.

MULTI-SPEED INTEGRATING ADC This is an integrating ADC that uses two or more integration speeds to: 1) increase the overall throughput rate; or 2) increase the resolution achievable at a dynamically limited conversion rate; or both. A converter of this type with two integration speeds is designated a "two speed, triple slope" converter.

Figure 8 demonstrates the sequence of operation of a multi-speed integrating converter. The first two ramps are much steeper than they would be in a dual-slope (single-speed) ADC. The first ramp "acquires" the input signal very quickly. The second ramp integrates the reference voltage at the same rapid pace converting the integrator output to the MSB's, until the integrator output approaches a small percentage of full scale, typically 1%. At that point the internal control logic reduces the reference voltage to 1% of its previous value and shifts the counter outputs to the LSB's. This effectively adds a vernier mode to the reference integration phase to provide greater precision at a faster rate.

The auto-zero function has been left out for clarity.

NMRR Abbreviation for Normal Mode Rejection Ratio. NMRR is a measure of the ability of a converter to attenuate unwanted signals, particularly noise at line frequency and its harmonics. As it pertains to an ADC it is the ratio of the transfer function of the signal component of interest to the transfer function of unwanted signal components (noise, line frequency pickup, etc.) as a function of frequency. It is is expressed in decibels as follows:

$$NMRR = 20 \log_{10} (K(f_0) / K(f))$$

where $K(f_0)$ is the transfer function e_{out} / e_{in} at the frequency of the signal component of interest; f_0 is usually either 0 (dc) or a frequency consistent with the highest rate of change of the sampled input signal; and K(f) is the transfer function for the frequency at which NMRR is calculated — typically an integral multiple of the line frequency. Figure 9 shows NMRR as a function of frequency for a typical A/D converter.

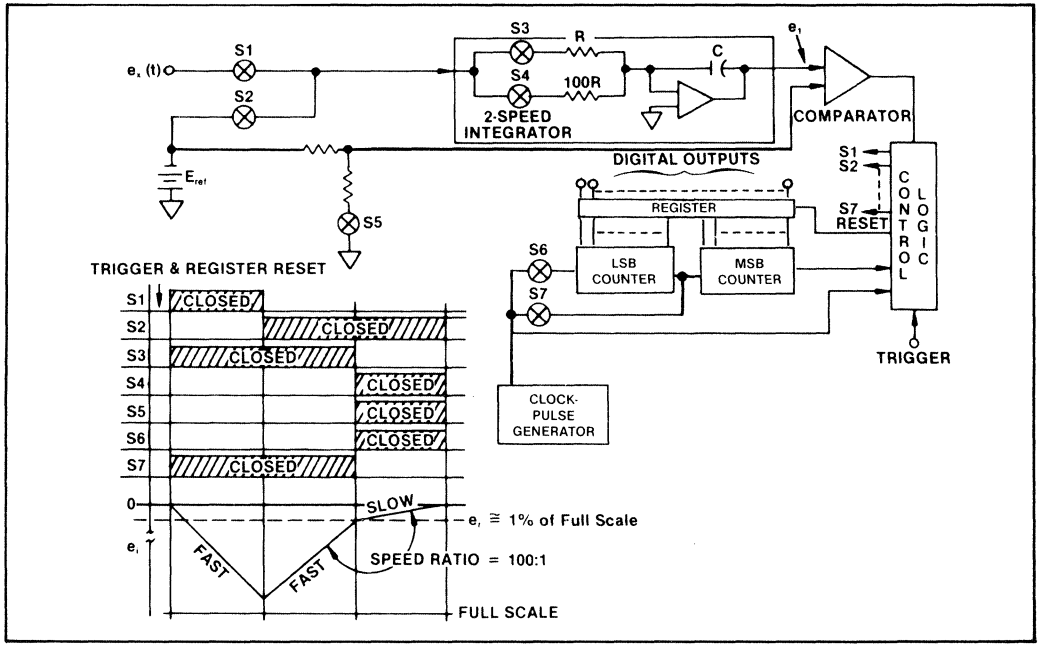


Figure 8. Block and Timing Diagrams of a Triple-Slope Integrating A/D Converter.

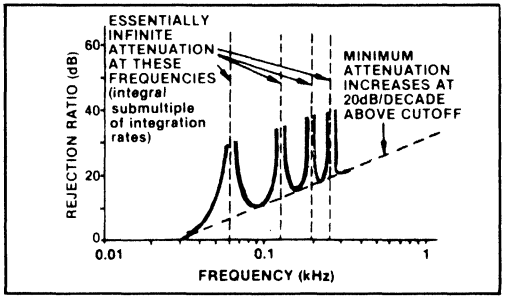


Figure 9. NMRR vs. Frequency of a Typical Integrating ADC.

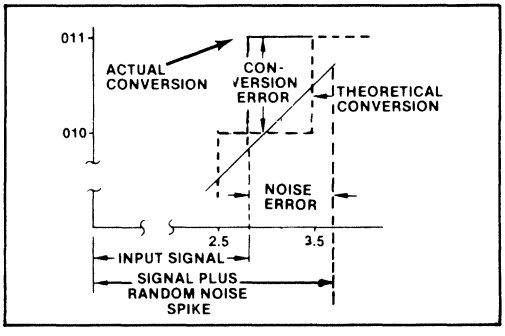


Figure 10. Effect of Noise on Conversion Accuracy.

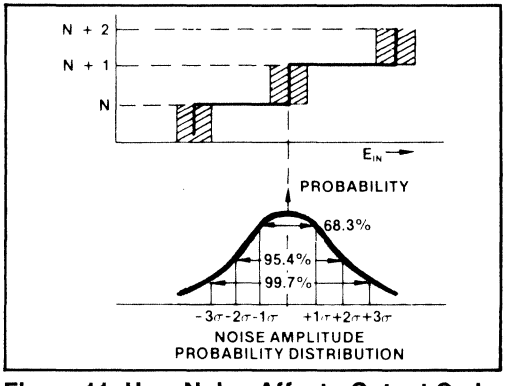


Figure 11. How Noise Affects Output-Code Transitions.

NOISE ERRORS These are errors in the output code caused by the presence of signals other than those one is trying to measure (see Figure 10). There are four main types of noise: 1) power line frequency (common mode); 2) electrical interference on the input lines (normal mode); 3) noise generated by the signal conditioning circuitry; and 4) noise generated by the ADC during the conversion process. Common mode noise can be filtered out by the integrator or by signal conditioners in the front end. Normal mode noise can usually be reduced by low pass filtering. Internally generated noise is inherent to the converter and tends to be random in nature.

The characteristics of random noise can be described by statistical measures using the Gaussian distribution function and the dispersion value (sigma). See Figure 11. Noise generated by the ADC is specified over $\pm 3\sigma$ in μV RMS. This number can be used to calculate the percentage of time during which the noise level will exceed the 1-bit threshold and cause an incorrect output code. The table in Figure 12 shows that if the 1-bit threshold is greater than the $\pm 3\sigma$ noise level (p-p threshold = 6 x RMS noise level), a 1-bit or greater code error of either polarity will occur less than 0.3% of the time; a unipolar error will occur less than 0.15% of the time.

NOMINAL DIGITAL LEVELS Digital output signal level convention. This is typically binary or tristate, standard TTL, ECL, etc., or two specific voltage ranges.

OUTPUT CODE The output of an ADC may be one of a number of binary codes. The various codes include: unipolar binary, offset binary, one's complement and two's complement. Examples of these codes are shown in Figure 13, for a 12-bit device.

PERCENT OF TIME RMS NOISE LEVEL IS EXCEEDED IN EITHER DIRECTION	PERCENT OF TIME RMS NOISE LEVEL IS EXCEEDED IN ONE DIRECTION	PEAK-TO-PEAK NOISE LEVEL
31.8%	15.9%	$\pm 1\ \sigma$ (2 x RMS)
20%	10%	$\pm 1.64\ \sigma$ (3.3 x RMS)
4.6%	2.3%	$\pm 2\ \sigma$ (4 x RMS)
0.3%	0.15%	$\pm 3\ \sigma$ (6 x RMS)
0.02%	0.01%	$\pm 3.89\ \sigma$ (7.8 x RMS)

Figure 12. Probability Table for Figure 11.

Unipolar Binary:
For a device with a nominal FSR of 0 to 10V,

V_{max} = 111 111 111 111 = +9.9976V,
V_{min} = 000 000 000 000 = 0.0000V.

Offset Binary:
For a device with a nominal FSR of −10V to +10V,

$V_{max\ pos.}$ = 111 111 111 111 = +9.9951V,
$V_{midrange}$ = 100 000 000 000 = 0.0000V,
$V_{max\ neg.}$ = 100 000 000 000 = −10.0000V.

One's Complement:
For a device with a nominal FSR of −10V to +10V,

$V_{max\ pos}$ = 011 111 111 111 = +9.9951V,
$V_{midrange}$ = {000 000 000 000 / 111 111 111 111} = 0.0000V,
$V_{max\ neg}$ = 100 000 000 000 = −9.9951V.

Two's Complement:
For a device with a nominal FSR of −10V to +10V,

$V_{max\ pos}$ = 011 111 111 111 = +9.9951V,
$V_{midrange}$ = 000 000 000 000 = 0.0000V,
$V_{max\ neg}$ = 100 000 000 000 = −10.0000V.

Figure 13. Most Common Binary Codes.

PARALLEL THRESHOLD (FLASH) ADC The flash converter uses an architecture that achieves very fast conversions. The input signal is simultaneously applied to a large number of comparators each of which represents a successively higher LSB step. The output of the comparators is decoded to a binary value representing the highest step level attained. A block diagram of a 4-bit flash converter is shown in Figure 14.

Because the number of components rises exponentially as the number of bits of resolution increases, the practical implementation of this architecture is limited to 8-bits. Resolution can be significantly increased, without an exponential increase in the circuitry, by performing a sequencing operation: flash encode the signal to yield outputs for the MSB's; convert the MSB's to an analog value and subtract that from the original input; flash encode the new input through a similar circuit to yield outputs for the LSB's.

POWER SUPPLY COEFFICIENTS Also stated as power supply sensitivity, these specifications indicate how the power supply voltage affects various parameters of

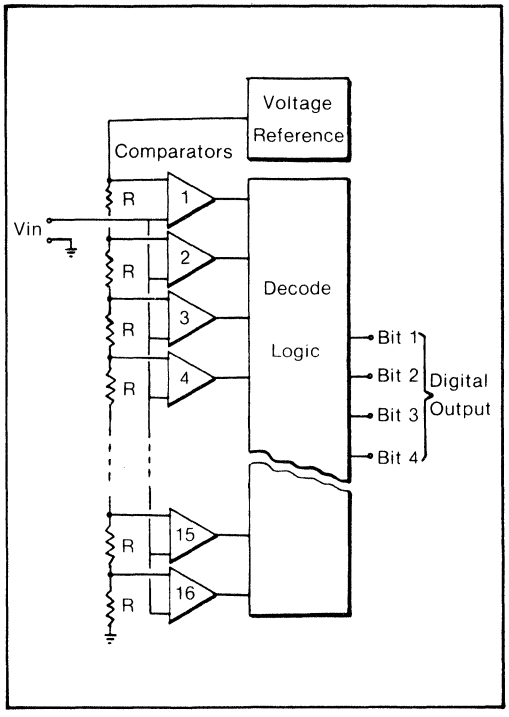


Figure 14. "Flash" A/D.

the ADC, e.g., ±0.001% per 1% change in power supply voltage.

QUANTIZING ERROR The conversion error equal to the smallest quantization level of the converter, ±0.5 LSB. This error is demonstrated in Figure 1.

RELATIVE ACCURACY This is a measure of the largest deviation of the converter's actual transfer function from the best straight line approximation of the actual transfer function, expressed as a percentage of full scale range. It comprises errors due to linearity, drift and circuit component tolerances:

e.g., ±0.005% of FSR.

RESOLUTION — ACTUAL VS. AVAILABLE The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes. Excessive internal noise and/or component drift can exclude the possibility of obtaining some output codes, reducing the actual resolution.

SUCCESSIVE APPROXIMATION ADC The successive approximation converter uses an architecture with inherently high throughput rates which converts high fre-

quency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

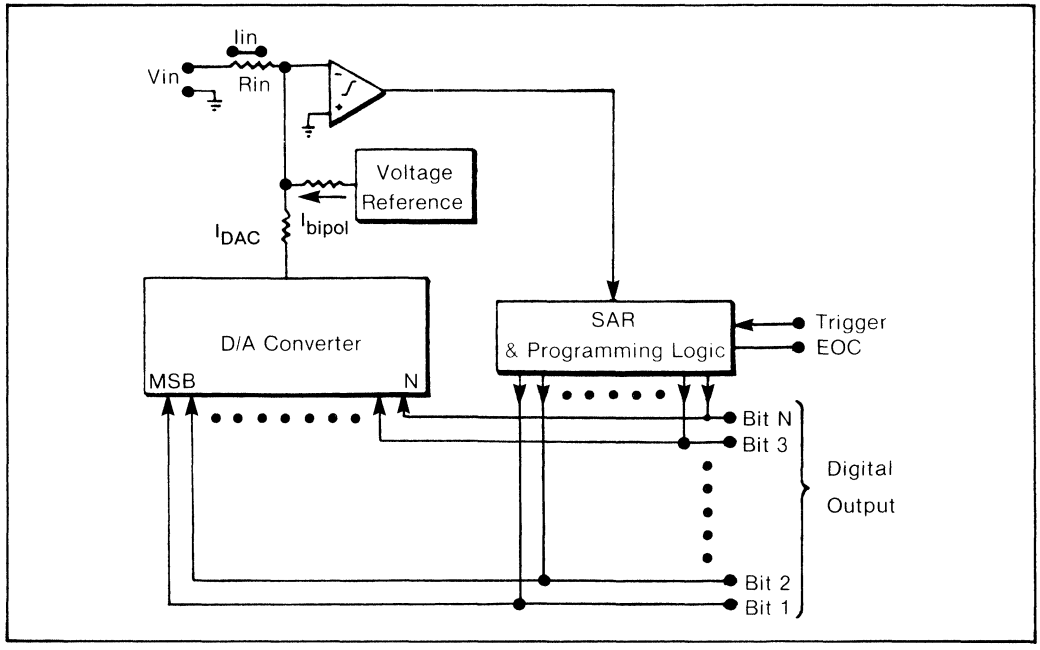
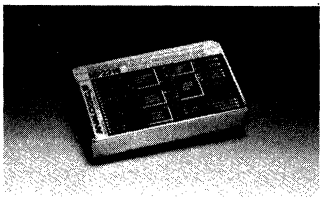


Figure 15. Block Diagram of a Successive Approximation A/D.

TEMPERATURE COEFFICIENTS Changes in the operating temperature can affect a number of parameters including zero offset, gain and differential linearity. The temperature coefficient, or tempco, of one of these parameters is computed as the change in that parameter over a specified temperature range divided by the number of degrees in that temperature range. This yields an average tempco over the temperature range, not the worst case. Analogic tempco specifications are conservative and generally may be considered worst case values.

THROUGHPUT Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

ZERO OFFSET The input voltage required to yield an output code corresponding to zero. Provision is normally made to allow the user to adjust the zero offset.



ANALOGIC®

MP2316

16-Bit Floating Input Programmable Gain Analog Processor

Description

The **MP2316** is a floating input, self-powered, programmable gain analog converter-processor front-end that provides very high isolation between high resolution digital systems and large numbers of multiplexed analog input signals, especially in high common-mode voltage industrial environments such as process control, data acquisition systems and HVAC systems.

The **MP2316** consists of an input stage, a 13-gain programmable gain amplifier, a buffered dual-slope integrating A/D, a precision reference, an isolated dc/dc converter, and all of the circuits required to complete the analog portion of a precision, 16-bit data acquisition system. The entire interface to the digital host system is through three transformer-isolated lines, two inputs for control and one output line for conversion results, which are in the form of an elapsed time between a pulse on one control line and the End-of-Conversion (EOC) signal from the converter.

The high isolation of the analog inputs from the digital output is achieved by an intrinsic CMRR of 90 dB due to high-quality magnetic isolators, an overall CMRR of 150 dB, a 60 dB line frequency normal mode rejection ratio, and up to ± 500V (ac peak and dc) of common mode isolation. *(continued)*

Features

- **Programmable Gain Amplifier**
  Provides 13 switch selectable full scale ranges from ± 10 mV to ± 50V
- **Floating Isolated Input**
  Provides 500V isolation from signal common to output common
- **150 dB Common Mode Rejection Ratio**
- **Guarded Input**
  Allows multiplexing of input lead shields
- **Time interval output proportional to input voltage**
- **± 0.001% FSR Linearity**
  Consistent performance with 16-bit resolution
- **Isolated Output Voltages**
  Provides power for sensors
- **High Stability**
  0.3 μV/°C offset
  12 ppm/°C range
- **Wide Power Supply Requirement**
  + 12V to + 15V
- **Small Size**
  2" x 3" x 0.51"

Applications

- **Industrial Process Control**
- **Heating, Ventilating and Air Conditioning (HVAC)**
- **Thermocouple Measurement**
- **Bridge Measurement**
- **Data Acquisition Systems**

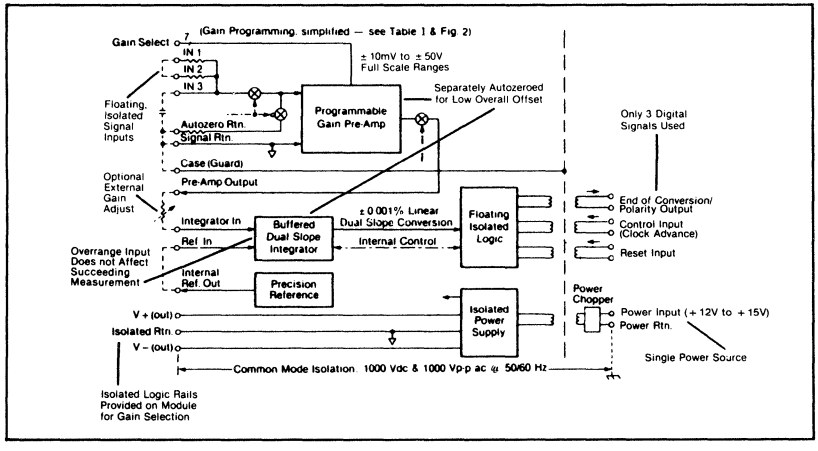


Figure 1. MP2316 Functional Block Diagram.

SPECIFICATIONS (Note 1.)

(All specifications guaranteed at 25°C unless otherwise noted.)

ANALOG INPUT

Configuration
Floating, isolated, three wire

Full Scale Range (FSR)
Selectable ranges from ± 10 mV to ± 50V (See Table 1)

Maximum Common Mode Voltage
± 500 Vdc or ac peak, minimum; (SIGNAL RETURN to POWER RETURN) (see Note 2.)

Common Mode Rejection Ratio
150 dB minimum at 50 or 60 Hz, with integration period within ± 0.05% of the power line frequency

Input Impedance
FSR ≤ ± 5V
100 MΩ minimum
FSR > ± 5V
1 MΩ nominal

Bias Current
300 pA, typical (see Note 3.)

Maximum Input
264 Vac rms continuous without damage (See Notes 2, and 4.)

ISOLATED VOLTAGE OUTPUTS

Output Voltage
+ 8V nominal (V+);
− 10V nominal (V−);
the amount of current drawn from V+ must never exceed that drawn from V− by more than 3 mA; the total current drawn from both outputs must not exceed 6 mA

ACCURACY

Output Coding
Time interval proportional to the magnitude of the input voltage, plus sign decision based on polarity of input

Resolution
Depends on count rate of external counter; up to 16 bits (15 magnitude bits plus sign bit) achievable with appropriate external logic

Transfer Accuracy
Consistent with 15-bit resolution, with external calibration adjustment

Differential Non-linearity
± 0.001% FSR, typical

Integral Non-linearity
± 0.006% FSR, typical

Offset
RTI
Externally adjustable to zero (see Note 5.)
RTO
± 15 ppm FSR, maximum (see Note 6.)

Noise
3 μV rms or 10 ppm FSR rms maximum, whichever is greater; assumes a 1.5 μF capacitor (Cx) across IN3 and SIGNAL RETURN per Figure 1

STABILITY

Range Tempco (0°C to 70°C)
FSR ≤ ± 5V
± 12 ppm FSR/°C typical,
± 25 ppm FSR/°C maximum
FSR > ± 5V
± 20 ppm FSR/°C typical,
± 30 ppm FSR/°C maximum

RTI Offset Tempco (0°C to 70°C)
± 0.3 μV/°C typical

Power Supply Rejection Ratio
± 0.002% FSR/percent power supply change

Recommended Recalibration Intervals
6 months

DYNAMIC PERFORMANCE

Input Integration Time (Phase 1)
1/60 second ± 0.05% when synchronized to 60 Hz power line; 1/50 second ± 0.05% when synchronized to 50 Hz power line (see Note 7.)

Full Scale Reference Integration Time (Phase 2)
One-half the input integration time, nominal

Integrator Autozero Time (Phase 3)
1.9 μs, minimum, no maximum limit

Time to recover from Overrange Input
1.9 μs (see Note 8.)

Overall Throughput Rate
Up to 37 measurements/second when synchronized to 60 Hz line; Up to 31 measurements/second when synchronized to 50 Hz line

DIGITAL INPUT/OUTPUT (see Figure 3)

Input Lines
12V CMOS compatible; negative pulses

Reset Line
A negative pulse on this line initiates the autozero phase; low level is active; 200 ns pulse width minimum, 3 μs maximum (see Note 9.)

Clock Advance Line (see Figure 6)
Negative-going (leading) edge is active; each pulse must be low for 100 ns minimum

First Pulse (Φ1)
Initiates input integration

Second Pulse (Φ2)
Strobes out the Polarity (decision) Pulse

Third Pulse (Φ3)
Initiates reference integration

Output Line
12V CMOS compatible, positive pulses; positive-going (leading) edge is active; 100 ns minimum pulse width, 4 μs maximum; 100 ns rise and fall times, typical

Polarity Pulse
Occurrence of an output pulse upon receipt of the polarity strobe (Φ2) indicates that the input signal has a negative polarity; absence of a pulse at this time indicates positive polarity

End-of-Conversion (EOC) Pulse
The elapsed time from the start of reference integration until EOC occurs is directly proportional to the magnitude of the input signal plus a constant 1 μs, nominal, delay

POWER SUPPLY REQUIREMENTS

+12V to +15V
80 mA typical
125 mA maximum

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
0 to 80%, non-condensing to 40°C

Dimensions
2.0" x 3.0" x 0.51"
(50.8 x 76.2 x 12.9 mm)

Shielding
Electrostatic 6 sides
Electromagnetic 5 sides

Case Potential
At the GUARD potential (equals common mode potential referenced to POWER RETURN)

Notes:
1. Assumes a 1 kΩ gain adjust potentiometer is connected per Figure 1.
2. With Cx = 1.5 μF installed between AUTOZERO RETURN and IN3, or with external diode input protection circuit per Figure.
3. 500 pA maximum at 40°C; doubles every 10°C above 40°C.
4. Input 1 to SIGNAL RETURN; INPUT 2 to SIGNAL RETURN.
5. ±50 μV maximum, externally adjustable to zero via AUTOZERO RETURN (See Autozero Connection Section).
6. Externally adjustable via 1 μs nominal delay between Clock Advance Φ3 and start of user's counter.
7. Sign decision is made immediately prior to completion of the input integration phase.
8. Assumes that Reset is issued whenever EOC does not occur within the nominal full scale integration time.
9. Measured between 50% points.

Description (cont.)

The programmable gain amplifier (PGA) provides a simple and flexible scheme for selecting a ±10 mV to ±50V full scale range while maintaining full isolation. Gain may be changed by applying the **MP2316's** own isolated auxiliary voltage outputs, via switches, to the gain programming pins (see GAIN PROGRAMMING). An auto-zero return from the PGA allows long-term system offset drifts to be essentially eliminated. Both the PGA and the integrator are auto-zeroed between conversions, so that dc offset is less than 50 μV RTI (adjustable to zero).

By fully implementing the most difficult (analog) functions, the **MP2316** is an ideal starting point for designing a wide variety of low speed, precision data acquisition systems. By parallel connection of multiple units, higher throughputs can be achieved.

USING THE MP2316

Gain Programming

The three gain stages shown in Figure 2 allow selecting any of the 13 gains from 0.05 to 250 inclusive, providing full scale ranges from ±50V to ±10 mV. The external potentiometer connections shown allow fine adjustment of any selected range. For example, a 1 kΩ pot provides a ±4.5% adjustment, more than adequate for obtaining either a ±1.000V FSR or a ±1.024V FSR with one basic gain selection.

Each of the gain stages may be externally configured using either switches, relays, opto-isolators, or by any other convenient means available in the host system. The module's own floating output voltages may be used for controlling the **MP2316's** internal solid-state switches, A through H, per the inset of Figure 2.

External gain and offset adjustment potentiometers, if used, can be switched similarly. It is possible, then, to configure and trim the **MP2316** to provide nearly any desired full scale range(s) and/or any desired range-to-range absolute accuracy, while maintaining full isolation. When the maximum obtainable accuracy is required, it is recommended that each range be calibrated individually.

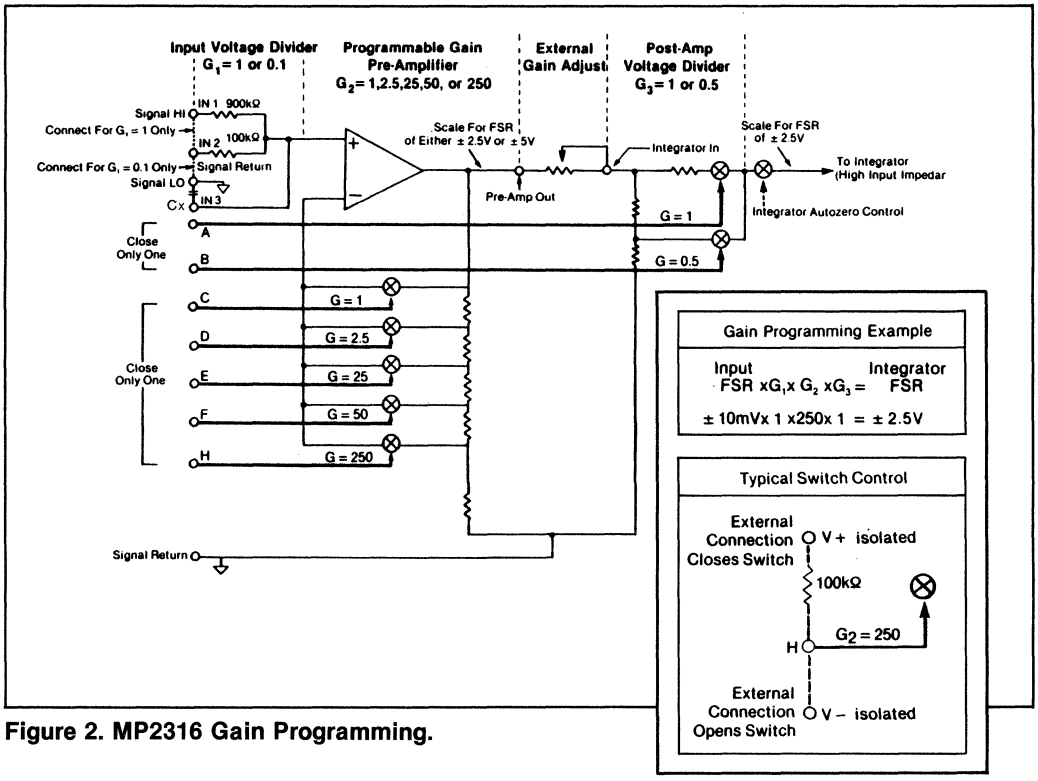


Figure 2. MP2316 Gain Programming.

FSR[1]	Gain Select Pin Connections[2] A	B	C	D	E	F	H	G_1[3]
± 10mV	1	0	0	0	0	0	1	1
± 20mV	0	1	0	0	0	0	1	1
± 50mV	1	0	0	0	0	1	0	1
± 100mV	1	0	0	0	1	0	0	1
± 200mV	0	1	0	0	1	0	0	1
± 1V	1	0	0	1	0	0	0	1
± 2V	0	1	0	1	0	0	0	1
± 2.5V	1	0	1	0	0	0	0	1
± 5V	0	1	1	0	0	0	0	1
± 10V	1	0	0	1	0	0	0	0.1
± 20V	0	1	0	1	0	0	0	0.1
± 25V	1	0	1	0	0	0	0	0.1
± 50V	0	1	1	0	0	0	0	0.1

Table I. MP2316 Range Programming

NOTES TO TABLE I

1. Full scale ranges (FSR's) specified with 500Ω nominal between gain adjust terminals @ 25°C ± 5°C. A resistance change of 0 to 1kΩ between gain adjust terminals results in a nominal gain change of 9%

2. "0" denotes this pin connected to the V− isolated output.
   "1" denotes this pin connected to the V+ isolated output through a resistor.

3. Input Gain; see Figure 2 and **Input Connections.**

INPUT CONSIDERATIONS

Input Connections

For full scale ranges larger than ± 5V, the analog input signal is connected to IN1, and IN2 is externally connected to SIGNAL RETURN. In this configuration, the input stage's gain of 0.1 allows use with input signals having full scale ranges up to ± 50V.

For full scale ranges nominally ≤ ± 5V, the analog input signal is connected to IN2, which provides unity gain. IN1 should be tied to IN2 to prevent noise pick-up. By connecting a 1.5 μF capacitor between IN3 and ground, high frequency noise filtering on any range can be accomplished. The low-pass filter thus formed (RC = 900 kΩ/1.5 μF for IN1 and RC = 100 kΩ/1.5 μF for IN2) will reduce the usable input signal bandwidth.

Case Potential

The Case (GUARD) pin may be tied to SIGNAL RETURN as shown in Figure 1, and/or to the lead shield, if one is used. If

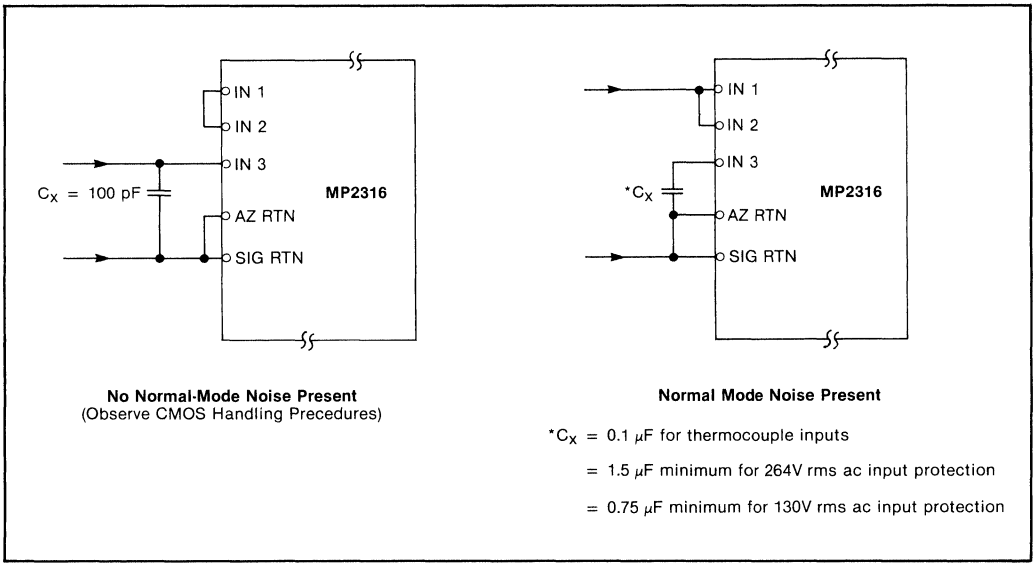


Figure 3. Input Configurations.

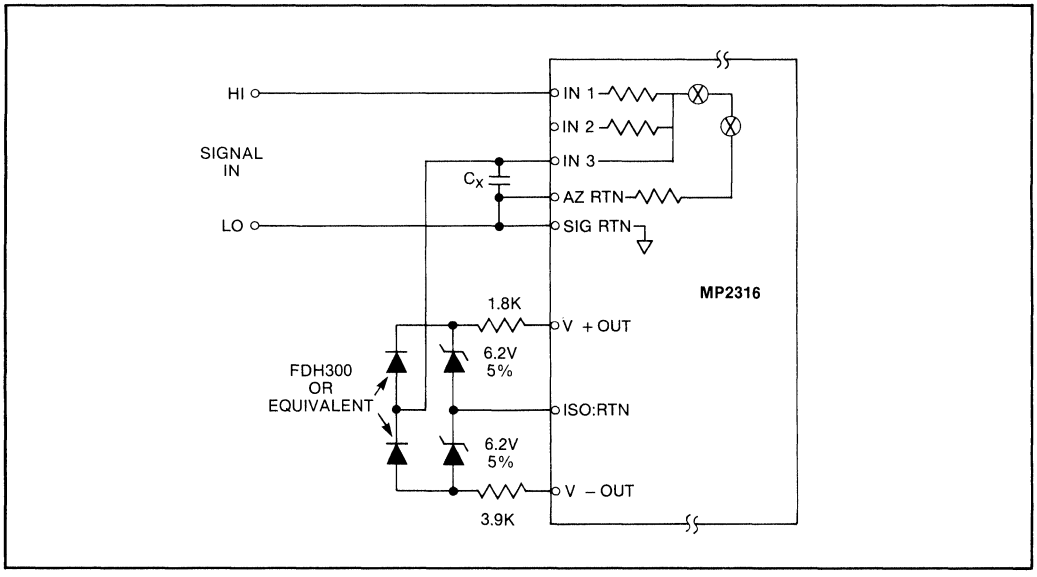


Figure 4. Diode Input Protection Circuit.

lead shields for different channels carry different potentials in the system, and the shields, are *not multiplexed to the Case pin,* it is recommended that each shield be tied to local earth at its sensor, while the Case pin is tied to SIGNAL RETURN. Optimum system performance will generally be obtained by using twisted shielded pair for each channel.

Input Overvoltage

The Specifications call out a maximum continuous input without damage of 264 Vac rms. This assumes a value for Cx of 1.5 μF connected between the IN3 and SIGNAL LO pins as shown in Figure 2. Failure to use this capacitor will result in damage to the unit under the specified input conditions. It should be noted that this capacitor will

form a low-pass filter on the input (RC = 900 kΩ/1.5 μF for INPUT 1 and RC = 100 kΩ/1.5 μF for INPUT 2). This will reduce the usable signal bandwidth at the input to the A/D.

Noise

The Specification for noise performance assumes a value of 1.5 μF for Cx. If the capacitor is not used to low-pass filter the input, noise in excess of the specification can occur.

The input configuration can be modified depending on whether or not normal mode noise is present. See Figure 3.

Thermocouple Inputs

When used with thermocouple inputs, the value of Cx between IN3 and SIGNAL LO should be ≥0.1 μF to limit the input response to approximately 12 Hz.

Input Protection

It is recommended that the diode input protection circuit in Figure 4 be used to protect the **MP2316** from large common mode and normal mode spikes, such as those that occur when relay contacts are switching signal sources to the **MP2316** input.

Autozero Connection

Using the AUTOZERO RETURN, offsets that may occur between the SIGNAL RETURN and the common of the sensor subsystem (see Figure 5) can essentially be eliminated. The maximum offset that can be eliminated is 20% of the selected full scale range if the input voltage divider gain is set at unity. For larger full scale ranges where the input divider is set at 0.1, the maximum offset eliminated is 2% of the full scale range. A small signal potentiometer installed between SIGNAL RETURN and AUTOZERO RETURN can be used to zero the **MP2316's** small (±50 μV RTI maximum) offset, per Figure 5.

Isolated Output Voltages

The **MP2316** is provided with isolated voltage outputs of +8V and −10V nominal. These can be used to power strain gauges, or other sensors. It is important to limit the total current drawn from both outputs to 6 mA or less, and to ensure that the amount of current drawn from the V+ output never exceeds that drawn from the V− output by more than 3 mA.

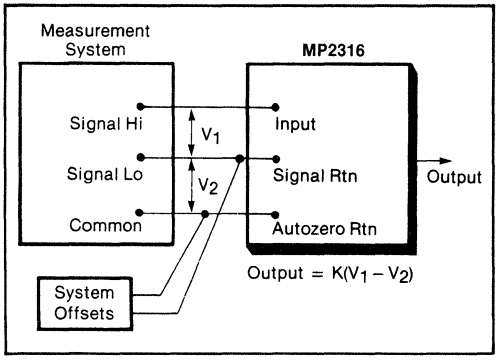


Figure 5. The MP2316's Three-Wire Input Configuration. *Essentially Eliminates Long Term Sensor System Offsets.*

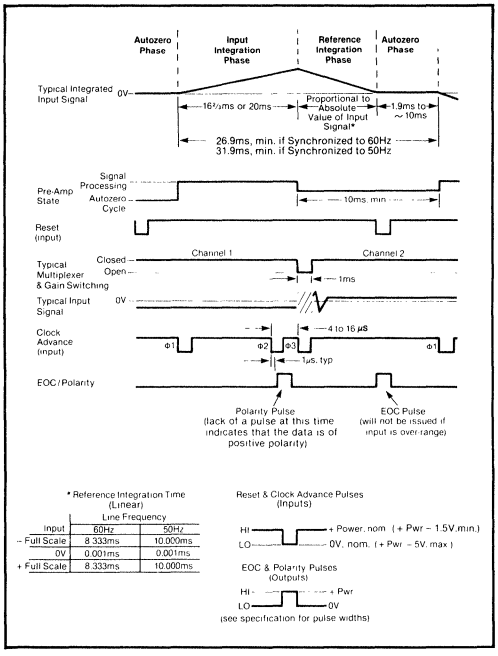


Figure 6. MP2316 Timing Diagram.

Reference Connections

The **MP2316** contains its own isolated precision reference source (−4.75V). This reference is brought out as a test point (INTERNAL REFERENCE OUT), and should be jumpered to REFERENCE IN for most applications.

For true ratiometric applications, a floating external supply that excites the system's sensors may also be applied, via a buffer, to REFERENCE IN (while INTERNAL REFERENCE OUT floats). If used, such a reference should be −4.75V ±10%.

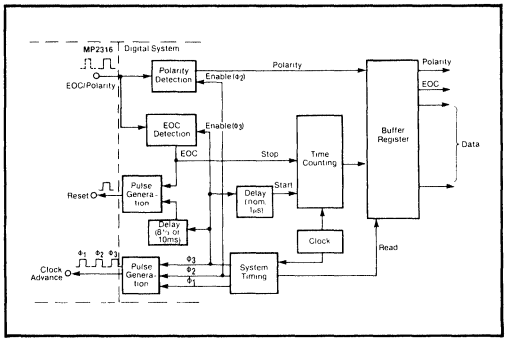
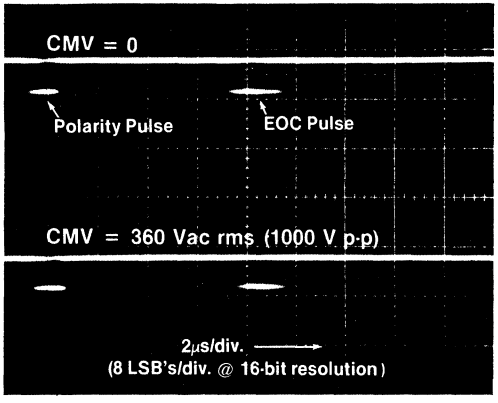


Figure 7. Application Diagram — *Functional Block Diagram of MP2316 External Control Logic, Implementable in either Hardware/Software.*



(Note: pulse polarity inverted for display only)

Figure 8. MP2316 Common Mode Rejection Ratio Test *(360V rms CMV, 37 Hz measurement rate, ± 50 mV FSR).* The upper trace shows the Polarity and EOC pulses for a zero volt input with no common mode voltage present. The lower trace shows the same pulses when 360V rms of CMV is present, also with a zero volt input signal. A time exposure is used to display both conversion results. In the lower trace, EOC occurs 0.5 μs later than in the upper trace. At 16-bit resolution, this shift is equivalent to 2 LSB's, or only 3 μV common mode error — on a full scale range of ± 50 mV — resulting from 360V rms CMV. Thus the CMRR measured is greater than 160 dB, 10 dB better than the MP2316 specification!

Timing and Control

The Timing Diagram (see Figure 6) shows the operation of a multiplexed data acquisition system that uses the **MP2316;** the Applications Diagram (Figure 7) indicates the corresponding external logic functions. These functions can be implemented via either hardware or software, depending on the economics of the host digital system. The operational timing contains three phases summarized as follows:

1. Integrate the input signal;
2. Integrate the precision reference for a maximum of one-half of the input integration time;
3. Autozero the integrator.

Operation during each of these phases is described below, starting with the autozero phase.

Autozero Phase

Each measurement cycle begins with a pulse on the RESET line, which initiates autozeroing of the precision integrator. A minimum of 1.9 ms should be allowed for autozeroing. If the **MP2316** input is overranged, the autozero circuit will ensure recovery within this time.

Input Integration Phase

When the first pulse (Φ1) is received on the CLOCK ADVANCE line, the autozero cycle terminates and integration of the input signal begins.

The second pulse on the CLOCK ADVANCE line (Φ2) strobes out the results of a polarity test which the module performs on the input signal during the integration. This second pulse should occur from 10 μs before the end of this signal integration period. If the input signal is negative, the **MP2316** issues a pulse on the EOC/POLARITY line nominally within 1 μs of receipt of the Φ2 pulse. If the input signal is positive, the **MP2316** issues no pulse on the EOC/POLARITY line at this time.

Reference Integration Phase

The third pulse is applied to the CLOCK ADVANCE (Φ3) from 4-16 μs after the Φ2 pulse, at which time the module automatically switches the integrator's input to the precision reference, and the pre-amplifier's input to the AUTOZERO RETURN line. Because the preamplifier is disconnected from the integrator, any gain and/or multiplexer switching needed for the next measurement may be made during this phase without affecting the accuracy of the reference integration.

Within nominally 1 μs after receiving Φ3, the **MP2316** begins discharging the integration capacitor via a precision reference of opposite polarity from that of the input signal. If the magnitude of the integrated signal is within the integrator's full scale range, the capacitor will be fully discharged during this phase, causing a pulse to appear on the EOC/POLARITY line. The table in Figure 8 shows the linear relationship between (1) the integrated input signal, and (2) the elapsed time between the Φ3 and EOC pulses.

If the magnitude of the integrated signal exceeds the integrator's full scale range, EOC will not be issued. In such a case, a pulse must be issued on the RESET line after the maximum reference integration time has elapsed; this will cause the overrange condition to be cleared by the autozero circuit.

Timing Resolution and Code Conversion

The resolution of the analog-to-digital conversion may be established at any desired level continuously up to 16 binary bits or 4 full BCD digits plus sign. Linearity will be 0.001% FSR regardless of the resolution selected. Selection of resolution is accomplished by specifying the external counter's clock rate in accordance with the following relationship:

$$F_{clock} = \frac{B^{(n-1)} \text{ (the maximum counts at } \pm \text{ full scale)}}{T}$$

where n is the desired resolution (including the sign bit), B is the counting base (normally 2 or binary) and T is the maximum reference integration time. As an example, for 15-bit binary resolution with 60 Hz power line:

$$F_{clock} = \frac{2^{(15-1)}}{8.33 \text{ ms}} = 1.966 \text{ MHz}$$

A 2 MHz clock may be used for convenience in this case, which will slightly increase the resolution with no change in linearity. As a second example, for a full 4 digit BCD display plus sign with 50 Hz power line:

$$F_{clock} = \frac{10^{(5-1)}}{10.0 \text{ ms}} = 1.00 \text{ MHz}$$

Other coding, such as two's complement, can be established by simple logic at the counter's output.

Calibration

The **MP2316** is inherently stable, and in most applications, will not require recalibration more often than every six months. When recalibrating the system, adjust offset before adjusting range.

Offset Adjustment

RTI offset may be adjusted to zero via external potentiometer installed between AUTOZERO RETURN and the SIGNAL RETURN (see Figure 9); RTO offset may be adjusted via a time delay between Φ3 and the start of the external software or hardware counter. With a 0V input signal, adjust the offset signal via the selected method(s) so that the reference integration time is within the desired tolerance (e.g., within one or two clock periods of the counter start.)

Range Adjustment

Range may be adjusted via a potentiometer installed between the PGA OUTPUT pin and the INTEGRATOR INPUT pin (see section on gain programming). It is recommended that an input voltage of roughly 10% less than full scale be used during this adjustment procedure to avoid overrange conditions during adjustment. Adjust the range so that the dual-slope-derived reference integration time, as shown by an external counter, is proportional to the input voltage to within the desired tolerance.

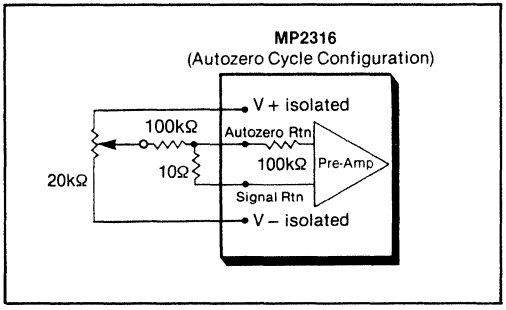


Figure 9. Optional RTI Offset Compensation.

ORDERING GUIDE

Specify **MP2316**

Notice: The Analogic MP2316 is protected under one or more of the following U.S. patents and others pending: 3,051,939; 3,054,910; 3,316,547; 3,649,924; 3,750,146.

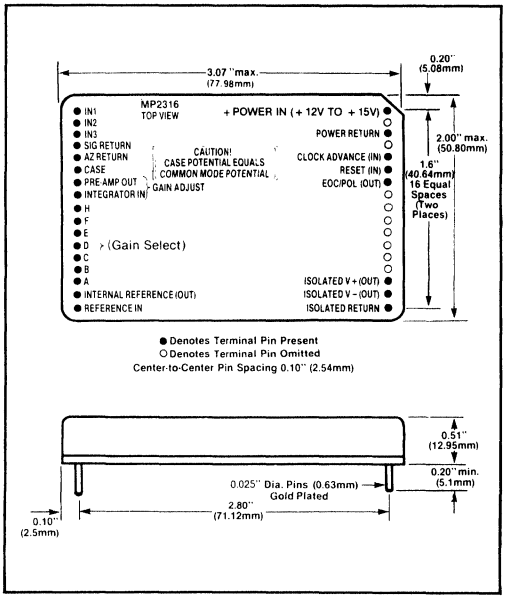
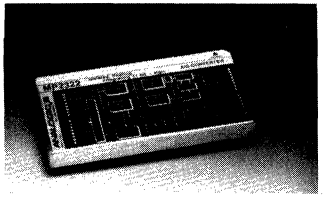


Figure 10. Mechanical & Pinout.



ANALOGIC®

MP2321/2322

Isolated, Floating 3½-Digit BCD or 12-Bit Binary Integrating A/D Converters

Description

Analogic's MP2321 and MP2322 are high performance, low cost extremely versatile integrating analog-to-digital converters that feature well isolated, floating, guarded, bipolar analog inputs. They are designed for use by OEM's in a broad range of recording, analytical and industrial control instrumentation systems. These converters reject high common mode levels of ±300V with respect to system ground, are accurate to 0.05%, exhibit an accuracy tempco that is less than 50 ppm/°C of reading, and require but a single 5V supply. They therefore allow economical, extremely accurate and highly stable 3½ BCD digit or 12-bit (sign and magnitude) data transformation in severe common mode environments, a capability frequently required in process control instrumentation and single current loop remote indicator systems. The DTL/TTL compatible output and control lines provided by these digitizers permit easy automatic examination of the data by local and remote displays and printers, and facilitate control of the data acquisition by computer-oriented hardware.

The MP2321 and MP2322 are particularly qualified as the nuclei of measurement systems. The isolated floating front end allows digital conversion of remote signals which may not be referred to ground; and the computer-compatible control and status connections permit easy interfacing to ancillary equipment. Additionally, these converters are easily customized for use in a gamut of OEM applications simply by selecting the proper pins for the following operations: Ratiometric A/D conversion, useful for automatic compensation of transducer excitation supply drift, or standard digitization (see Figs. 4 and 6); control of the conversion rate — up to 100 readings per second (see Figs. 3 and 5), or conversion initiation by external command (see Figs. 5 and 7) so that digitizations occur exactly when required, and for the MP2322, a choice of output binary codes (see Fig. 9).

Features

- **True Floating Isolated Inputs**
- **2 Versions**
  BCD Outputs — MP2321
  Binary Outputs — MP2322
- **600V p-p Common Mode Voltage**
- **Automatic Zero**
  Negligible Offset
- **Ratiometric Conversion Available**
- **Only Single 5 Vdc Power Supply Required**
  Floating Supply Built-in
- **Up to 100 Conversions/second**
- **Low Cost**
- **Shielded Metal DIP Case**
  2" x 4" x 0.49"

Applications

- **Medical Instrumentation Systems**
- **Industrial Transducer Digitization**
- **Analytical Instruments**
- **Industrial Process Control**

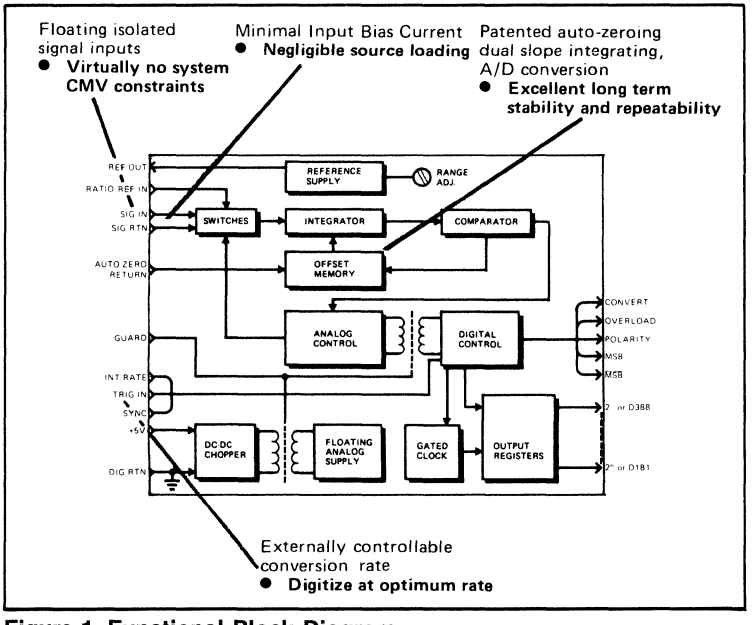


Figure 1. Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Configuration
Bipolar, floating, isolated, guarded and shielded

Full Scale Range
MP2321: ± 1.999V or ± 199.9 mV standard, + 1V or + 100 mV Ratiometric
MP2322: ± 2V or ± 1V or ± 200 mV or ± 100 mV depending on output code (see Fig. 9) standard; + 1V or 100 mV ratiometric

Input Impedance
500 MΩ nom.

Bias Current
1 nA nom.

Common Mode Voltage (Between SIG RTN and DIG RTN)
± 300 Vdc, 600 Vac p-p

Common Mode Rejection (With 1 KΩ Unbalance)
120 dB min. @ dc, 100 dB min. @ 60 Hz, 60 dB min. @ 1 kHz

ACCURACY

Resolution
MP2321: 1 part in 2000 counts, 3½ BCD digits plus sign
MP2322: 1 part in 2048 counts, 11 bits plus sign

Relative Accuracy (Linearity)
0.05% rdg ± 1 count

Offset
50 μV typ., 75 μV max.

Monotonicity
Guaranteed

STABILITY

Range Tempco
50 ppm rdg/°C max. for 1V or 2V FSR
75 ppm rdg/°C max. for 100 mV or 200 mV FSR

Offset Tempco
1 μV/°C max.

CONVERSION

Technique
Dual slope bipolar integration with auto-zero; complete conversion in each cycle

First Integration Time
2 ms nom. See timing diagram

Auto-zero Time
3 ms min. See timing diagram

Reading Rate
Internal trigger: 4/s nom.
External trigger: 100/s max. See Fig. 5

CONTROL INPUTS

External Trigger
TTL/DTL compatible
Negative pulse 1.5 μs min., 1.8 ms max.
See Fig. 5

Hold
Conversion held by connecting a 47 kΩ resistor between INT RATE and DIG RTN. See Fig. 7

Line Frequency Sync
Connecting 10 Vac p-p max. at power line frequency to sync input will minimize effect of normal mode noise

DIGITAL OUTPUTS

Compatibility
TTL/DTL compatibility, sinks 5 mA max. (3 loads)

Output Data Codes
MP2321: Bipolar BCD (sign and magnitude)
MP2322: Bipolar binary (sign and magnitude) offset binary, and 2's complement. Pin selectable. See Fig. 9

Polarity
High (logic "1") level indicates positive input signal

Overload
High (logic "1") level indicates input signal amplitude greater than FSR

Convert
High level indicates conversion in process. Negative going transition signifies end of conversion. See timing diagram. Note: Internal clock is available; consult factory.

POWER SUPPLY

+ 5 Vdc ± 5%
300 mA

ENVIRONMENTAL & PHYSICAL

Operating Temperature
– 10°C to + 70°C

Storage Temperature
– 15°C to + 85°C

Relative Humidity
0 to 95% non-condensing

Electrical Shielding
RFI 6 sides; EMI 5 sides

Overvoltage Protection (Between SIG IN and SIG RTN)
± 15V maximum input without damage

Packaging MP232X
2" x 4" x 0.49" (50.8 x 101.6 x 12.45 mm) see Fig. 10

CALIBRATION AND OPERATION

Calibration

The Models MP2321 and MP2322 self-zeroing A/D converters require only a single adjustment for complete calibration to specified accuracy. RANGE is calibrated by applying a voltage level such as + 1.9985V or + 0.9985V, or + 199.85 mV or + 99.85 mV (depending on output code and model, see Fig. 9) to the input, and trimming the RANGE control so that the LSB only of the output code alternates equally between "1" and "0".

Internal Triggering Control

Adjustment of the built-in triggering rate (4 conversions/s) may be implemented by the circuitry described in Fig. 3. The sampling rate is approximately $1.44/R_TC_T$, where R_T is R_1 in parallel with the internal 82 kΩ and C_T is C_1 in parallel with the internal 3.3 μF.

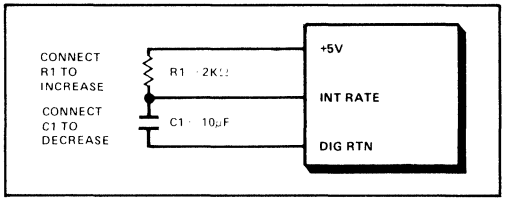


Figure 3. Connections for Adjusting Internal Triggering Rate.

Hold or Convert on Command

Holding or continuously converting the analog input can be selected by means of the circuitry presented in Figure 7. When the CONVERT/HOLD switch is in the HOLD position, the last conversion will be "held" indefinitely; in the CONVERT position, the analog input will be digitized at the rate selected by the methods shown in Figures 3 and 5.

External Triggering

Triggering the conversion cycle externally is implemented by means of the external circuitry shown in Figure 5, and applying a negative pulse (logic "1" to logic "0") 1.5 μs min. and 1.8 ms max. duration. The negative going transition initiates the conversion cycle. The maximum conversion rate to specified accuracy is 100/s.

Conversion Operation Selection

The MP2321 and MP2322 can perform standard or ratiometric A/D conversions by implementing the connections described below.

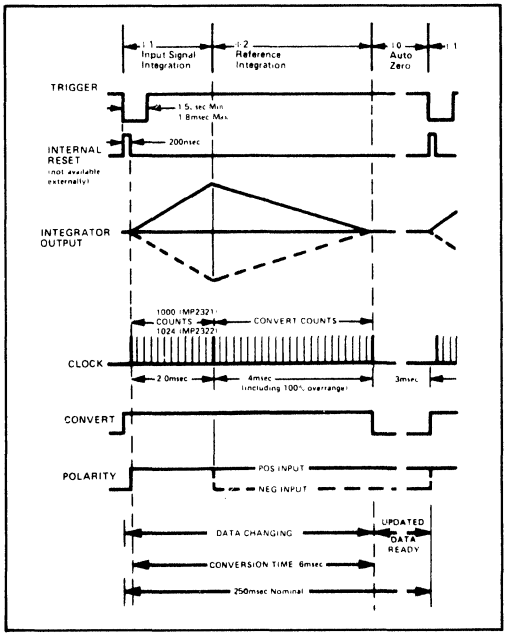


Figure 2. MP2321 and MP2322 Timing Diagram.

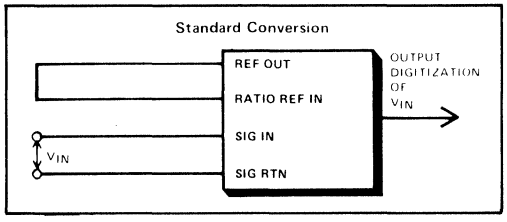


Figure 4. Connections for Standard A/D Conversions.

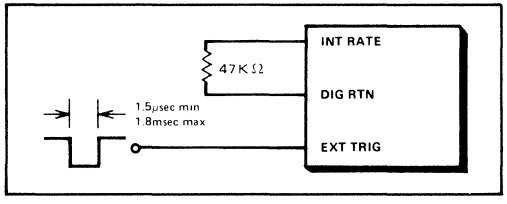


Figure 5. Connections for External Triggering.

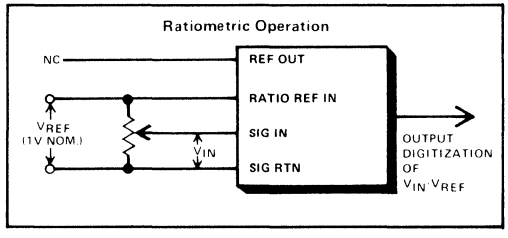


Figure 6. Connections for Ratiometric A/D Conversion.

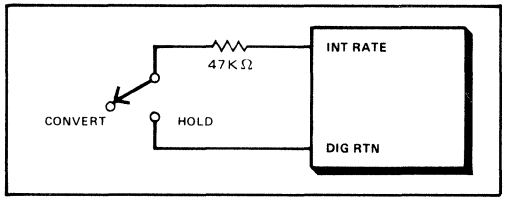


Figure 7. Connections for Commanding Hold or Continuous Conversion.

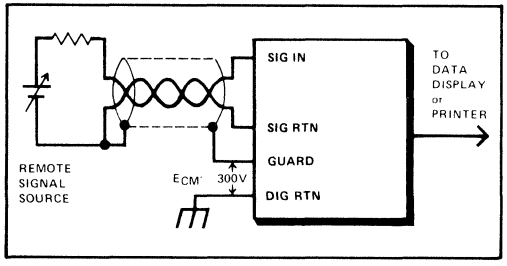


Figure 8. Typical Connections Showing Use of MP2321 GUARD to Minimize Pick-Up Noise.

Typical Hook-Up Connections

In a typical application the GUARD may be used to minimize stray pick-up noise and enhance common mode rejection by wiring it to the shield of the signal source leads.

Output Code Selection

The output code for Model MP2321 is 3½ digits BCD plus sign. The output code for Model MP2322 is pin selectable. Figure 9 presents the appropriate connections and full scale values for the available codes.

Converter Model	**Full Scale Input Voltage	Output Code	Jumper Connections
Bipolar BCD 3½ BCD Digits + Sign (MP2321)	+1.999 0.000 0.000 −1.999	1 1 1001 1001 1001 1 0 0000 0000 0000 0 0 0000 0000 0000 0 1 1001 1001 1001 *P, D4B1, D3B8,...D1B1	None
Bipolar Binary 11 Bits + Sign (MP2322)	+1.999 0.000 0.000 −1.999	1 1 111 111 1111 1 0 000 000 0000 0 0 000 000 0000 0 1 111 111 1111 *P, MSB, 2^9....2^0	Connect AUTO ZERO RET to SIG RTN
†Offset Binary − 11 bits (MP2322)	−0.999 0.000 +1.000	1 111 111 1111 1 000 000 0000 0 000 000 0000 *MSB, 2^9....2^0	Connect AUTO ZERO RET to RATIO REF IN
†Two's Complement − 11 bits (MP2322)	−0.999 0.000 +1.000	0 111 111 1111 0 000 000 0000 1 000 000 0000 *MSB, 2^9... 2^0	Connect AUTO ZERO RET to RATIO REF IN

Figure 9. Table Showing Available Full Scale Value and Jumper Connection Required for Selected Output Code.

** For 100 mV or 200 mV units divide input voltage by 10

* P: polarity (or sign) bit; D4B1: fist bit of the fourth digit; NSB: most significant bit

† Reverse signal input leads to obtain true 2's complement or offset binary output

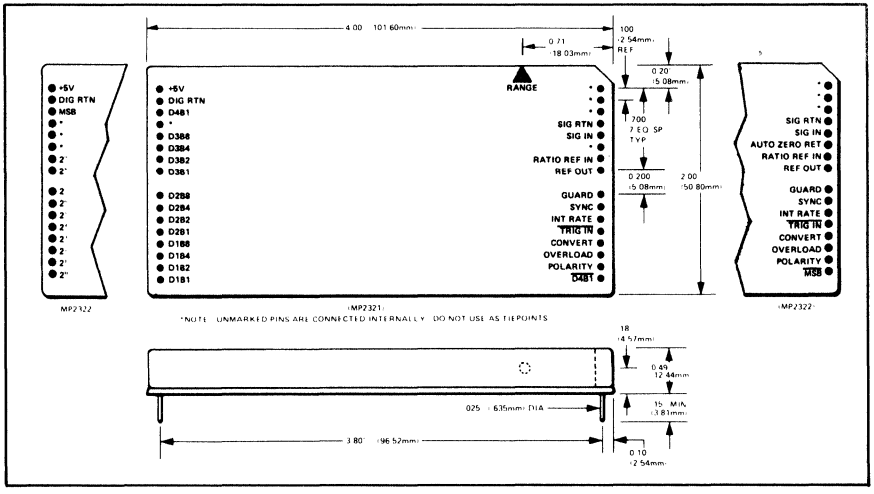
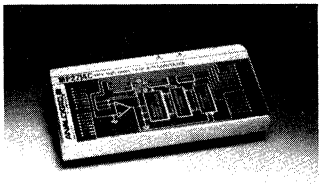


Figure 10. MP2321 and MP2322 Outline Drawing.

ORDERING GUIDE

For	Specify	
3½ Digit BCD Output	**MP2321***	*For 1V and 2V units. To specify 100 mV and 199.9 mV FSR, add "−01" to ordering code. For example a "MP2321-01" converts 199.9 mV FSR to BCD.
Sign11 Bit Binary + Output	**MP2322***	



ANALOGIC®

MP2700 SERIES

A/D Converters

Description

The MP2700 Series are general purpose A/D converters offering high speed, accuracy and stability, with resolutions of 12, 13 and 14 bits. All of the converters in the Series feature both parallel or serial (NRZ) data outputs, internal offset and gain adjustment potentiometers, and pin-selectable input voltage ranges.

Each model in the MP2700 Series is packaged in a 2" x 4" metal can that provides RFI shielding on six sides, and EMI shielding on five.

Features

- **Pin-selectable Input Ranges** 0V to +10V, ±5V, ±10V and 0V to +5V.
- **Parallel and Serial Data Outputs**
- **Can be short-cycled for increased throughput**
- **Buffered outputs**
- **Internal Offset and Range Adjustment Potentiometers**

Applications

- **General Purpose Analog Computer Interface**
- **Multi-channel Process Control**
- **Analytical Instrumentation**
- **Telemetry**

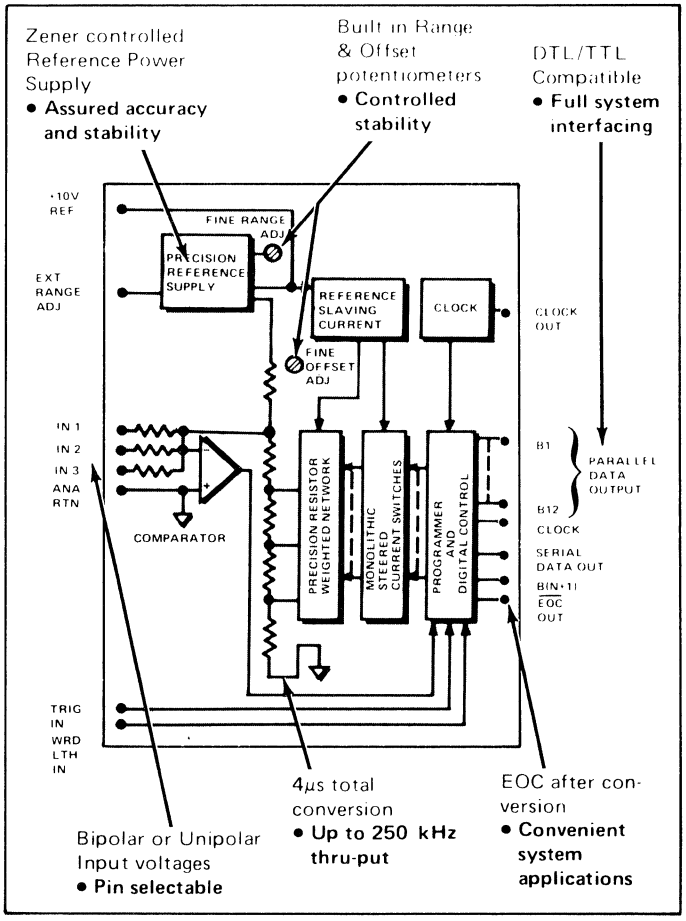


Figure 1. MP2712D Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Input Voltage (Full Scale Range)
0 to +10V, ±5V, ±10V, or 0 to +5V

Input Impedance
125Ω/V of FSR

ACCURACY

Absolute Accuracy (Traceable to NBS Standards)
Calibrated to:
0.015% max. (MP2712D),
0.009% max. (MP2713C),
0.007% max. (MP2714C)

Relative Accuracy
±0.012% max. (MP2712D),
±0.006% max. (MP2713C & MP2714C)

Differential Linearity
±0.012% FSR max. (MP2712D),
±0.006% FSR max. (MP2713C & MP2714C)

3σNoise (Includes Reference Noise)
0.01% FSR p-p, max. referred to input (MP2712D),
0.005% p-p, max. referred to input (MP2713C & MP2714C)

Monotonicity
Guaranteed

STABILITY

Tempco of Differential Linearity
< ±3 ppm/°C FSR max.

Tempco of Gain
< ±12 ppm/°C max. (MP2712D),
< ±10 ppm/°C max. (MP2713C),
< ±8 ppm/°C max. (MP2714C)

Tempco of Offset
< ±12 ppm/°C FSR max.

Clock Stability
±0.1%/°C

Power Supply Sensitivity
±0.0012%/% max. change in supply voltage

Recommended Recalibration Interval
6 months

Repeatability
Defined by Noise and Accuracy

CONVERSION TIME

Total Conversion
5 μs max. (MP2712D),
10 μs max. (MP2713C & MP2714C)

DIGITAL SIGNALS

Parallel Output (see Timing Diagram)
Binary $\overline{B1}$, B1 to B12 (MP2712D),
Binary $\overline{B1}$, B1 to B13 (MP2713C),
Binary $\overline{B1}$, B1 to B14 (MP2714C)
Standard TTL, 2 unit load/line

Serial Output (see Timing Diagram)
Negative pulses simultaneous with clock pulse for "0". Max. load 30 pF

Coding
Pin selectable

Trigger Input
3.5V ±1V pulse. See Timing Diagram

Trigger Input Transition
≤200 ns (90% to 10%)

End of Conversion, EOC
"1" to "0" level transition, nominally 100 ns after LSB data pulse. TTL compatible, 9 loads. (See Timing Diagram)

EOC Transition
≤20 ns (10% to 90%)

Clock Output
TTL compatible (See Timing Diagram)

Clock Output External Capacitance
30 pF maximum allowable

Selectable Word Length
2 to 12 bits (MP2712D),
2 to 13 bits (MP2713C),
2 to 14 bits (MP2714C)

POWER SUPPLY

+15V ±3%
60 mA, max.

−15V ±3%
60 mA, max.

+5V ±5%
300 mA, max.

ENVIRONMENTAL, PHYSICAL, & RELIABILITY

Maximum Input Without Damage
±200% of Full Scale Range

Missing Codes
None

Warm-up Time to Stated Accuracy
<5 minutes

Operating Temperature
0°C to +60°C

Storage Temperature
−25°C to +85°C

Electrical Shielding
RFI 6 sides; EMI 5 sides

Packaging MP27xx
2" x 4" x 0.44" Metal Case
(51 X 102 X 11.3 mm)

USING THE MP2700 SERIES

Input Voltage Range Selection

Three input pins are provided to allow user selection of one of four standard input voltage ranges. "IN 1", "IN 2", and "IN 3" must be connected in accordance with the following tables and illustrations to select the desired full-scale range.

Output Word Length Selection

The number of bits in the output word is pin selectable. To operate the ADC at its full capacity, B (N + 1) must be connected to WRD LTH IN. To operate the converter at less than its full digital output capacity, WRD LTH IN must be connected only to the terminal identified as one bit more than the desired number of bits out. EXAMPLE: When the ADC is operated as an 8-bit converter, connect WRD LTH IN to B9 only. Refer to the accompanying chart for the binary output coding.

CALIBRATION

Zero Offset Calibration

To recalibrate the OFFSET:
1. Apply input voltage shown in accompanying table and,
2. Adjust the OFFSET control so that the LSB of the output code 100...00/1 for bipolar units and 00...00/1 for unipolar units alternates equally between "1" and "0". Offset should be readjusted whenever the selected full scale range is changed.

Zero Offset should be calibrated before recalibrating RANGE.

Range Calibration.

Internal: A built-in 0.1% adjustment of the full scale voltage is provided. To recalibrate the RANGE:
1. Apply input voltage shown in the accompanying table and,
2. Adjust the RANGE control so that the LSB of the output code, 111...110/1 (B1,...B(N)), alternates equally between "1" and "0". RANGE should be readjusted whenever the selected full scale range is changed.

External Connection

A wider range adjustment may be implemented by connecting a 20 kΩ potentiometer between "+10V REF" and "ANA RTN"; and connecting a resistor, R, between the wiper arm of the 20 kΩ potentiometer and "RANGE ADJ". The adjustment range will be +5% to −0.3% for R = 470 kΩ and +5% to −2.8% for R = 47 kΩ. This latter value permits the calibration of a unit to be set for the so-called binary adjusted scale factors of 10.24V or 5.12V.

Typical Application

An MP2712D Analog-to-Digital Converter is shown connected to a high speed-high resolution multiplexed data conversion subsystem. The subsystem provides 12-bit data conversion at thru-put rates up to 200,000 conversions per second.

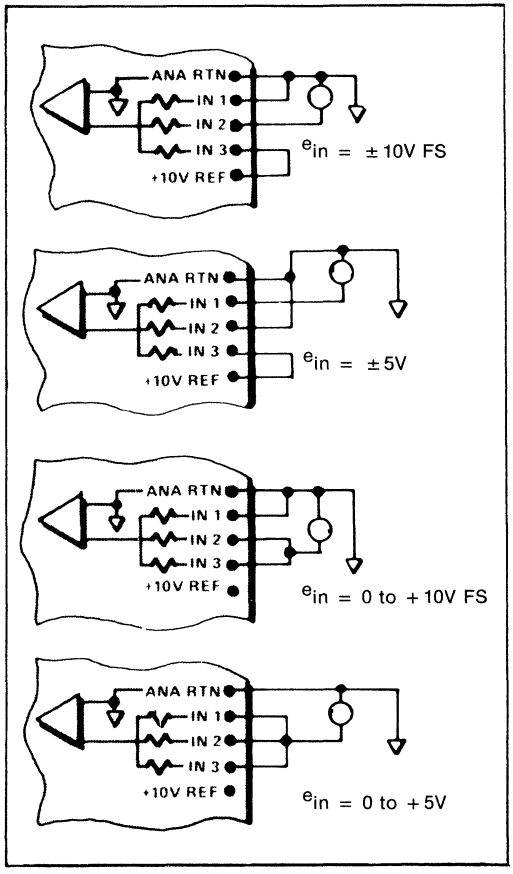


Figure 2. Jumper Connections for Input Voltage Range Selection.

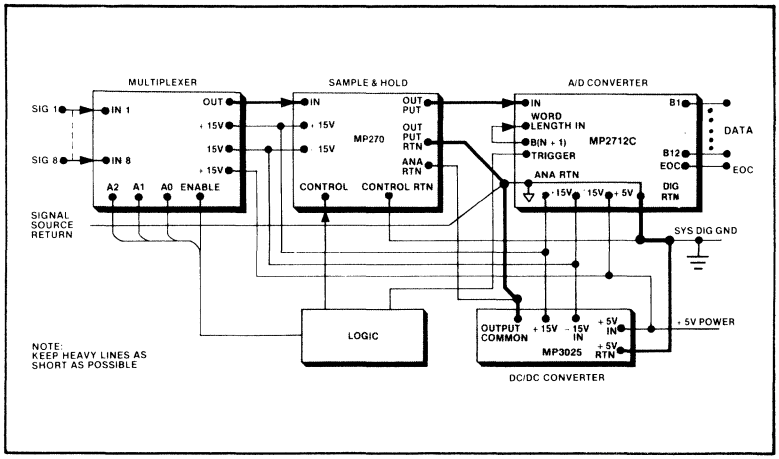


Figure 3. Typical Application of MP2712D A/D Converter.

INPUT RANGE CONNECTION TABLE			
Nominal Full Scale Range	**MP2710D, MP2712C, MP2713C, MP2714C**		
	IN 1	**IN 2**	**IN 3**
− 10V to + 10V	to ANA RTN	to ANA INPUT	to + 10V REF
0V to + 10V	to ANA RTN	to ANA INPUT	to ANA INPUT
− 5V to + 5V	to ANA INPUT	to ANA RTN	to + 10V REF
0V to + 5V	to ANA INPUT	to ANA INPUT	to ANA INPUT

INPUT VOLTAGES FOR CALIBRATION						
Nominal Full Scale Range	**MP2712D For**		**MP2713C For**		**MP2714C For**	
	Zero Cal.	**Range Cal.**	**Zero Cal.**	**Range Cal.**	**Zero Cal.**	**Range Cal.**
− 10V to + 10V	+ 0.0024V	+ 9.9927V	+ 0.0012V	+ 9.9963V	+ 0.00061V	+ 9.9982V
0V to + 10V	+ 0.0012V	+ 9.9963V	+ 0.0006V	+ 9.9982V	+ 0.00031V	+ 9.9991V
− 5V to + 5V	+ 0.0012V	+ 4.9963V	+ 0.0006V	+ 4.9982V	+ 0.00031V	+ 4.9991V
0V to + 5V	+ 0.0006V	+ 4.9982V	+ 0.0003V	+ 4.9991V	+ 0.00015V	+ 4.9995V

12 BIT RESOLUTION	13 BIT RESOLUTION	14 BIT RESOLUTION
Unipolar binary: +9.9976V = 111 111 111 111 0.0000V = 000 000 000 000 Pin Label = B1, B2.....B12	**Unipolar binary:** +9.9988V = 1 111 111 111 111 0.0000V = 0 000 000 000 000 Pin Label = B1, B2.....B13	**Unipolar binary:** +9.9994V = 11 111 111 111 111 0.0000V = 00 000 000 000 000 Pin Label = B1, B2.....B14
Two's complement:** +9.9951V = 011 111 111 111 0.0000V = 000 000 000 000 −10.0000V = 100 000 000 000 Pin Label = $\overline{B1}$, B2.....B12	**Two's complement**:** +9.9976V = 0 111 111 111 111 0.0000V = 0 000 000 000 000 −10.0000V = 1 000 000 000 000 Pin Label = $\overline{B1}$, B2.....B13	**Two's complement**:** +9.9988V = 01 111 111 111 111 0.0000V = 00 000 000 000 000 −10.0000V = 10 000 000 000 000 Pin Label = $\overline{B1}$, B2.....B14

**To change to offset binary, use B1 instead of $\overline{B1}$. For 5V units, divide input voltage by 2.

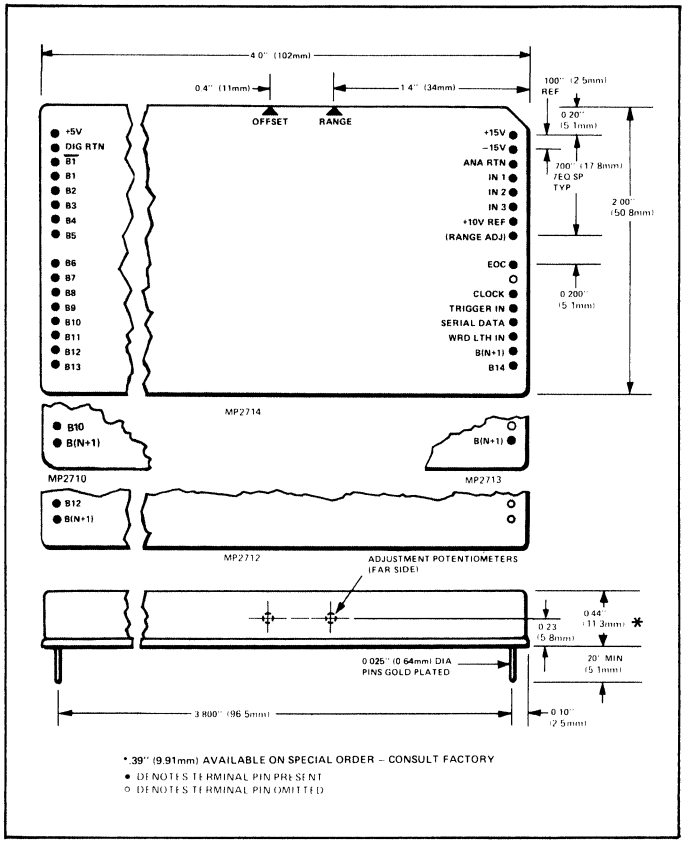


Figure 5. Outline Drawing.

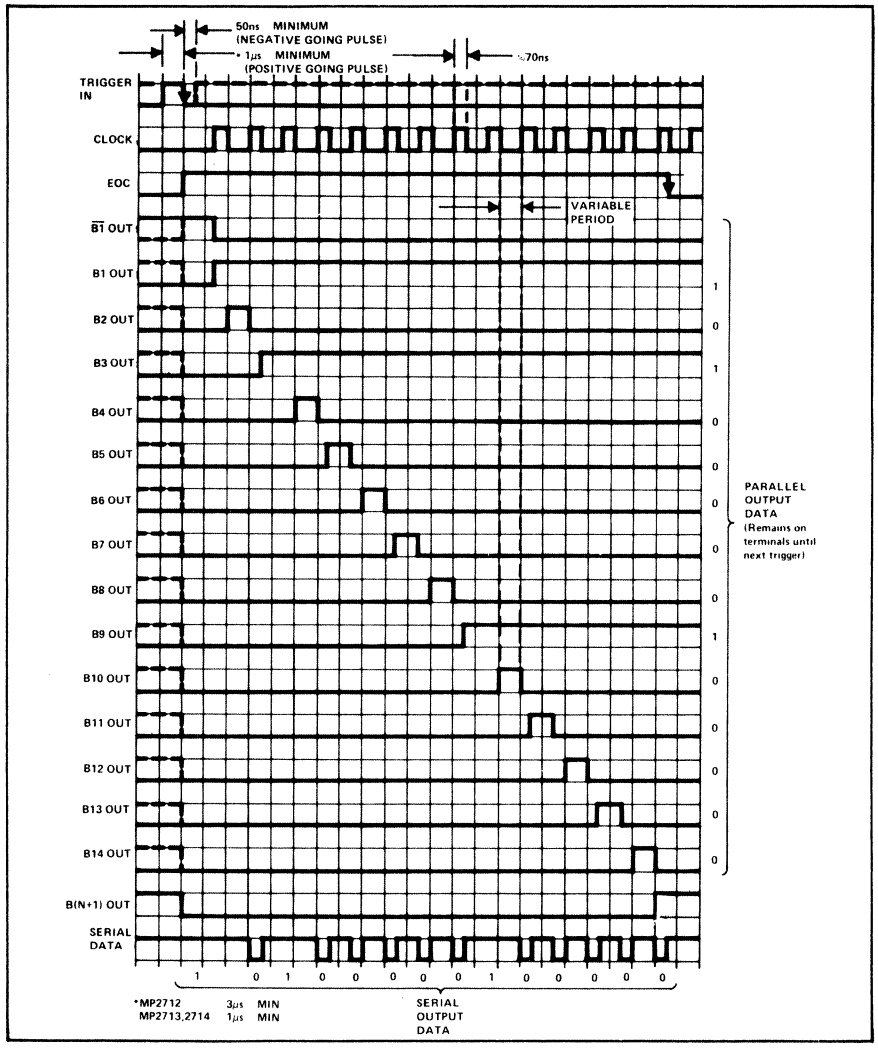


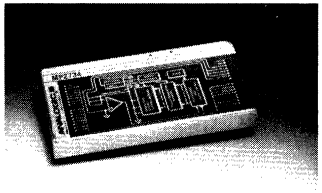
Figure 6. Timing Diagram for MP2714C

ORDERING GUIDE

Specify ——— [ ][ ] ———

Enter
MP27

For Resolution Of:	*Enter*
12 Bits	12D
13 Bits	13C
14 Bits	14C



ANALOGIC®

MP2734

Very High Speed Low Cost 14-Bit A/D Converter

Description

The MP2734, an economical, high speed 14-bit successive approximation analog-to-digital converter, features not only a 7 μs conversion time, but also a superb differential linearity of ±0.5 LSB, a relative accuracy of +0.006%, very low noise, and an exceptionally low differential non-linearity tempco of ±1 ppm. Such stability not only assures unusually uniform code widths, but also provides accurate, reliable performance for critical high speed, high accuracy applications, such as precision data acquisition and medical imaging systems.

Its superior performance is augmented by its interfacing flexibility and versatility. With four pin-programmable full-scale ranges, 0 to +5V, 0 to +10V, ±5V, ±10V, the MP2734 accepts all standard signal input ranges. The latched tri-state outputs allow high system throughput by holding the digital data for a full conversion period. In addition, the Modupac™ construction preserves the MP2734's performance in the presence of harsh electrostatic and electromagnetic interference. Finally, since the unit is pin-compatible with the industrial standard MP2714, for most applications, existing systems can be easily upgraded with the MP2734.

Built-in gain and offset adjustments eliminate the need for external adjustments since the adjustments are driven from an internal precision reference supply rather than from external potentiometers driven by raw ±15V power supplies. Furthermore, each individual MP2734 undergoes an exhaustive computer-programmed test, traceable to NBS standards; and the results are printed out and shipped with each unit. Thus, it is assured that the MP2734 will offer state-of-the-art, high speed, 14-bit performance under worst-case conditions.

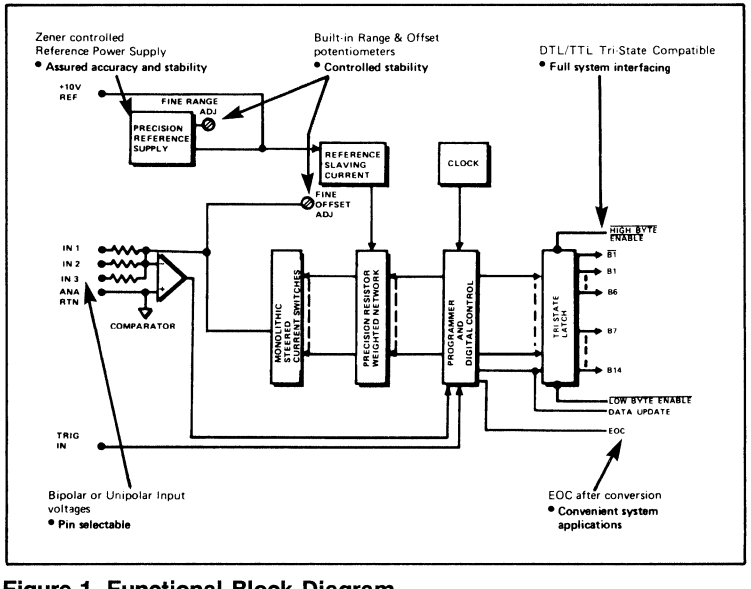


Figure 1. Functional Block Diagram.

Features

- **14-bit Resolution**
- **7 μs Conversion Time**
- **Low Cost**
- **Latched, Tri-State Output Buffers**
- **Pin Compatible with Industrial Standard MP2714**
- **±0.5 LSB Differential Linearity**
- **±1ppm FSR/°C Differential Non-Linearity Tempco**
- **0.005% p-p Noise**
- **Built-in Gain and Offset Adjustments**
- **Pin Programmable Input Ranging**
  Four full-scale ranges provide a 4 to 1 sensitivity range (choose range best matched to data system).

Applications

- **High Speed Computer Interfacing**
- **Wide Band Data Digitizing**
- **Multi-Channel Process Control**
- **Audio Digitizing**
- **Mass Spectroscopy**
- **Biomedical Instrumentation**
- **Seismic Array Digitizing**
- **Telemetry**
- **Research Instrumentation**

SPECIFICATIONS

(All Specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Full Scale Range (FSR)
0 to +5V, 0 to +10V,
±5V, ±10V (See Table 3)

Impedance
250 Ω/V of FSR

Maximum Voltage Without Damage
±200% of FSR

Offset
Adjustable to Zero

ACCURACY

Resolution
14-bits binary

Relative Accuracy @ 142 kHz
±0.006% FSR max.

Absolute Accuracy[1]
±0.007% FSR max.

Differential Non-linearity
±0.5 LSB typ., ±0.7 LSB max.

Noise on 0 to +10V FSR
83 μV rms

Monotonicity
Guaranteed

DYNAMIC PERFORMANCE

Throughput Rate
142 kHz, min.

A/D Conversion Time
7.0 μs max.

STABILITY

Differential Non-linearity Tempco
±1 ppm FSR/°C[5] typ.

Gain Tempco
±8 ppm FSR/°C typ.

Offset Tempco
±3 ppm FSR/°C typ.

Warm-up Time[2]
10 minutes

Recommended Calibration Interval
6 months

Power Supply Sensitivity
(per 1% change in supply voltages)
±12 ppm FSR

POWER REQUIREMENTS

Typical Power
2 watts

+15V ±3%
40 mA max.

−15V ±3%
50 mA max.

+5V ±5%
300 mA max.

ENVIRONMENTAL & MECHANICAL

Operating Temperature
0°C to +70°C

Storage Temperature
−25°C to +85°C

Relative Humidity
5% to 85%, non-condensing up to 40°C

Shielding
Electrostatic and Electromagnetic

Package Size
2" x 4" x 0.44" (50.8 X 101.6 X 11.2 mm)

SIGNAL	FAN IN (unit loads)	HIGH STATE = "1"	LOW STATE = "0"	COMMENTS
A/D Trigger	0.25	0.1 μs, min.	0.2 μs, min.	Negative edge starts conversion
High Byte Enable	0.25	Outputs at high impedance.	$\overline{B1}$, B1 through B6 active	
Low Byte Enable	0.25	Outputs at high impedance.	B7 through B14 active	

Table 1. Digital Control Inputs[3,4]

SIGNAL	FAN OUT[2] (unit loads)	TIMING	COMMENTS
$\overline{B1}$ and B1 through B14	2	Updated during the time that EOC is high and B15 is low.	Parallel data from tri-state latches.
End-of-Conversion (EOC)	2	Goes high 0.1 μs (typical) after A/D trigger falls. Goes low at end of conversion.	$\overline{B1}$ and B1 through B14 are updated 0.3 μs before "1-to-0" transition of EOC.
Data Update B15	2	"1-to-0" transition signals that B1 and B1 through B14 will update nominally 0.1 μs later.	Will arbitrarily be a "1" or "0" between conversions.

Table 2. Digital Outputs [3,4]

NOTES

1. Calibrated on ± 10V FSR. The gain potentiometer can be adjusted for zero error.
2. To specified accuracy.
3. Digital inputs and outputs are 74LS TTL with all input loads less than 0.4 mA.
4. See Timing Diagram.
5. Typical.

Using the MP2734

Four full-scale ranges, 0 to +5V, 0 to +10V, ±5V, or ±10V, offer a 4 to 1 sensitivity range. By connecting "IN 1," "IN 2," and "IN 3" in accordance with Figure 3 and Table 3, the operating range best matched to the data system can be selected. The latched tri-state outputs (DTL/TTL compatible) allow full system interfacing to either 8 or 16 bit data busses.

CALIBRATIONS

Zero Offset Calibration

To recalibrate the OFFSET:

1. Apply the input voltage shown in Table 4.
2. Adjust the OFFSET control so that the LSB of the output code 100...00/1 for bipolar units and 000...00/1 for unipolar units alternates equally between "1" and "0". The offset should be readjusted whenever the selected full scale range is changed.

Zero offset should be calibrated before recalibrating the RANGE.

Range Calibration

Internal: A built-in adjustment range of 0.1% of the full scale voltage is provided. To recalibrate the RANGE:

1. Apply the input voltage shown in Table 4.
2. Adjust the RANGE control so that the LSB of the output code 111...110/1 (B1...B14) alternates equally between "1" and "0". The RANGE should be readjusted whenever the selected full scale range is changed.

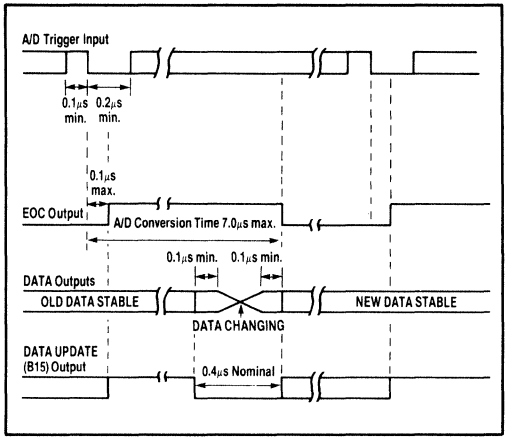


Figure 2. Timing Diagram.

Nominal Full Scale Range	IN 1	IN 2	IN 3
−10V to + 10V	to ANA RTN	to ANA INPUT	to + 10V REF
0V to + 10V	to ANA RTN	to ANA INPUT	to ANA INPUT
−5V to + 5V	to ANA INPUT	to ANA RTN	to + 10V REF
0V to + 5V	to ANA INPUT	to ANA INPUT	to ANA INPUT

Table 3. Input Range Connections.

Nominal Full Scale Range	Zero Cal.	Range Cal.
−10V to + 10V	+0.00061V	+9.9982V
0 to + 10V	+0.00031V	+9.9991V
−5V to + 5V	+0.00031V	+4.9991V
0 to + 5V	+0.00015V	+4.9995V

Table 4. Input Voltages for Calibration.

Unipolar binary

+9.9994V = 11 111 111 111 111
0.0000V = 00 000 000 000 000
Pin Label = B1, B2.....B14

Two's complement**

+9.9988V = 01 111 111 111 111
0.0000V = 00 000 000 000 000
−10.0000V = 10 000 000 000 000
Pin Label = $\overline{B1}$, B2.....B14

Table 5. Binary Output Coding

**To change to offset binary, use B1 instead of $\overline{B1}$.
For 5V units, divide input voltage by 2.

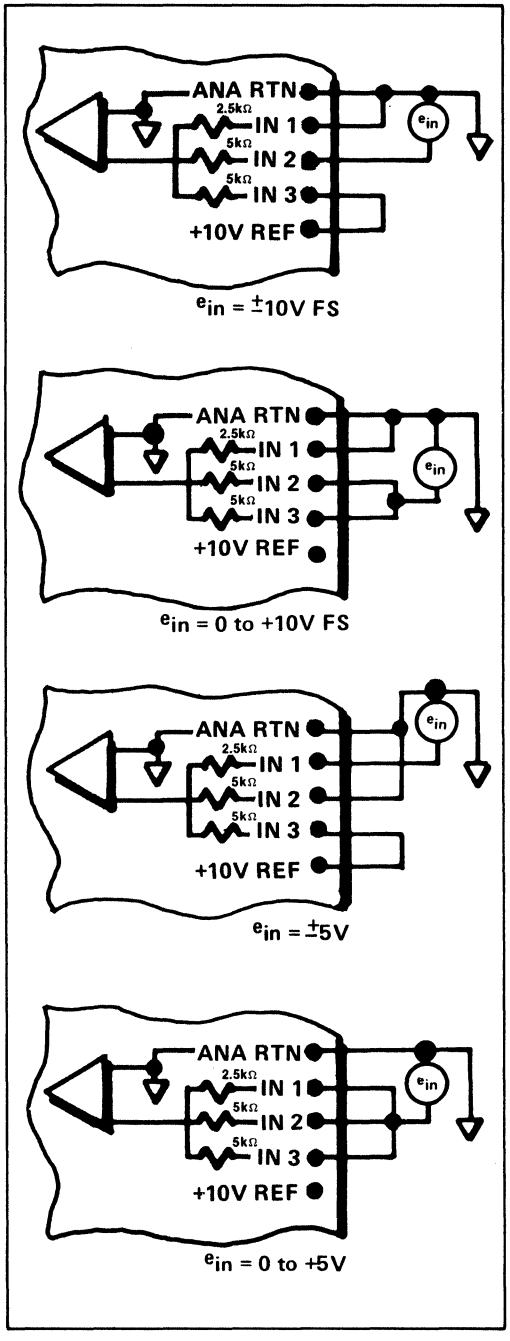


Figure 3. Jumper Connections for Input Voltage Range Selection.

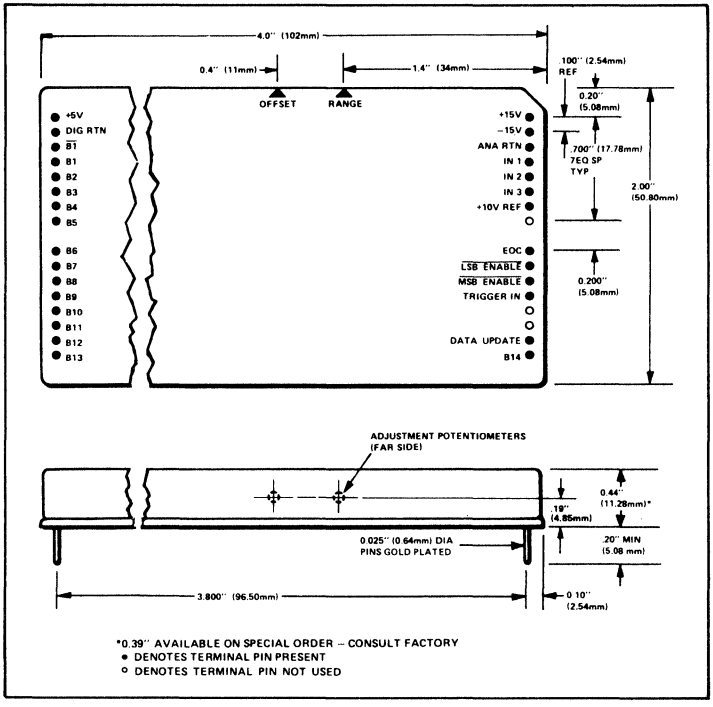


Figure 4. Mounting Dimensions.

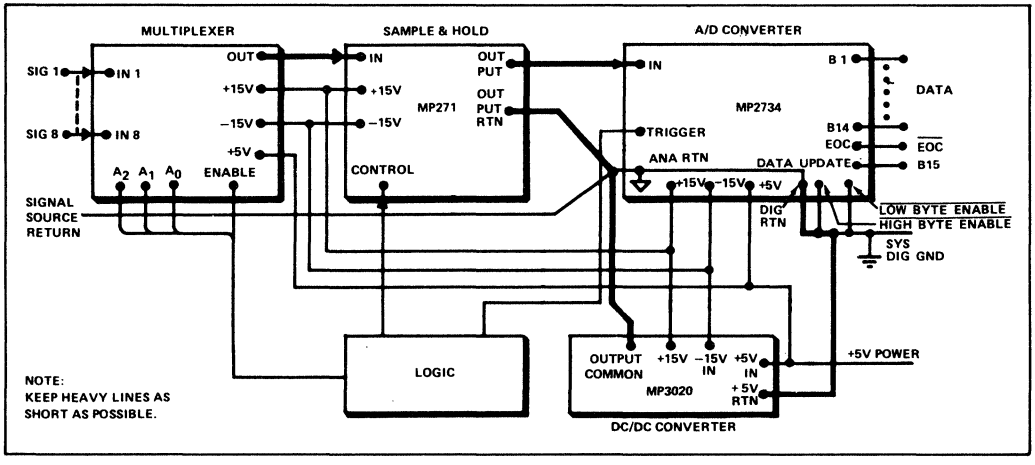
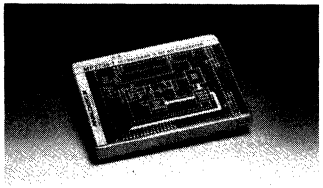


Figure 5. Typical 8 μs Conversion Application.

ORDERING GUIDE

Specify **MP2734**



ANALOGIC®

MP2735

Low Distortion, High Speed, 15-Bit Sampling A/D Converter

Description

The MP2735, a high speed, 15-bit sampling analog-to-digital converter, features zero crossover linearity and a differential linearity about mid-range that is actually better than that of most 16-bit converters. It is designed specifically to digitize dynamic complex waveforms, particularly audio or acoustic signals that have a substantial amount of information content around "zero volts" (mid-range). With a 5 μs conversion time, a low harmonic distortion of $\pm 0.005\%$ (-86 dB of peak full scale), a noise power ratio (NPR) of 65 dB, low idle noise (within 3 dB of the theoretical level), and wide dynamic range (90 dB), the MP2735 is suitably designed for professional audio applications.

The MP2735 exhibits excellent stability and reliability over temperature and time because its internal DAC has a sign/magnitude architecture, which is relatively insensitive to resistor instabilities especially around mid-range. In fact, because of this architecture, the MP2735 provides a monotonic and continuous transfer function through zero volts and is sig-

Features

- **Low Harmonic Distortion** $\pm 0.005\%$
- **Ultra-low Idle Noise** within 3 dB of theoretical level
- **High Noise Power Ratio** 65 dB for FDM/PCM Telecommunications
- **Wide Dynamic Range** 90 dB
- **Low Cost**
- **Low Power** 1.5 watts
- **High Speed** 5 μs
- **Built-in Sample-and-Hold**
- **Stable and Reliable Performance over Time and Temperature**

Applications

- **Professional Audio Systems**
- **FDM/PCM Telecommunications**
- **Seismic Data Acquisition**
- **High Frequency Communications**
- **Satellite Communications**
- **High Speed Data Acquisition**
- **Imaging Data Acquisition**
- **High Speed Automatic Test Equipment**

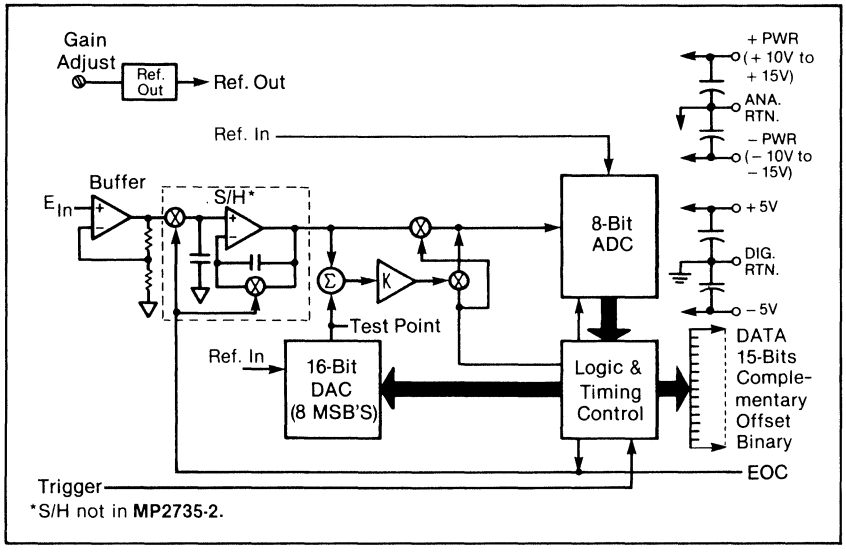


Figure 1. Functional Block Diagram.

SPECIFICATIONS

ANALOG INPUT

Full Scale Range (FSR)
± 5V

Input Impedance
100 MΩ||10 pf

Reference Input Voltage
– 6.4V

Reference Input Impedance
2.7 kΩ

ACCURACY

Resolution
15-bits

Quantization Error
± 0.5 LSB

Relative Accuracy of ADC @ 200 kHz Conversion Rate
± 0.005% FSR

FSR Factory Calibrated to
± 0.01%[1]

Offset Factory Adjusted to
± 1 mV[1]

Differential Linearity
± 0.5 LSB max., 0.25 LSB typical at ≤ 0.25 FSR
± 1 LSB max., ± 0.25 LSB typical at ≥ 0.25 FSR

Monotonicity
Guaranteed

Noise (10 Hz to 100 kHz)
25 μV rms

Zero Code 0° to 60°C
Continuous and monotonic through zero

STABILITY

Tempco of Differential Linearity

For Mid-Range Outputs Centered About Zero Volts (± 0.125 FSR)
± 0.5 ppm FSR/°C, max.

Over the Full Scale Range
± 1 ppm FSR/°C, max.

Tempco of Gain
± 10 ppm FSR/°C[4]

Tempco of Offset
± 10 ppm FSR/°C, max.

Power Supply Sensitivity
Gain
± 0.001% of FSR/% change in power supply

Offset
15 ppm of FSR/volt change in power supply

Warm-up Time
5 minutes

SIGNAL DYNAMICS

A/D Conversion Rate
MP2735-1
125 kHz, min. [2]

MP2735-2
200 kHz, min.

A/D Conversion Time
MP2735-1
5 μs, max.

MP2735-2
5 μs, max.

S/H Acquisition Time
3 μs

Slew Rate
10 V/μs

Aperture Delay
30 ns, typical

Aperture Uncertainty
± 0.4 ns, typical

Sample & Hold Feedthrough
– 86 dB

Harmonic Distortion up to 108 kHz
± 0.005%

DIGITAL INPUT CONTROLS

Code Compatibility
TTL Logic Levels

Trigger (positive transition)
Fan In
1 TTL Unit Load

Width
500 ns min.

DIGITAL OUTPUTS

Parallel Data
Fan Out
2 TTL Unit Loads/Line

Coding
Complementary Offset Binary [3]

End of Conversion (EOC)
High During Conversion

Fan Out
2 TTL Unit Loads

POWER SUPPLY [4]

+ 15V (+ 10V)
35 mA

– 15V (– 10V)
35 mA

+ 5V
90 mA

– 5V
50 mA

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 60°C

Storage
– 25°C to 85°C

Relative Humidity
0 to 85% non-condensing up to 40°C

Packaging Dimensions
3" x 4" x 0.44"

Shielding
Electromagnetic 5 sides
Electrostatic 6 sides

Case Potential
Ground

Notes

[1]Internal pots allow field calibration.

[2]Including internal S/H.

[3]Refer to "Calibration Procedures."

[4]Typical Values are shown.

Description (cont.)

nificantly more stable over temperature and time than a conventional 16-bit converter with an offset binary architecture. The MP2735 attains a differential linearity of ±0.5 LSB maximum and ±0.25 LSB typical at less than 0.25 full scale range, and it has no missing codes.

Furthermore, the unit's high speed conversion time of 5 μs allows two channels to be multiplexed and sampled at 55 kHz each and provides an ideal design for digitizing telephone group set FDM (frequency division multiplexed) analog data with a frequency band from 60 kHz to 108 kHz and a data update rate of 112 kHz, for multiplexed audio applications with a typical sampling rate from 32 kHz to 55 kHz, and for seismic data acquisition with a typical sampling rate of 32 kHz to 110 kHz.

The MP2735 is available in two versions: the MP2735-1 has a built-in sample-and-hold and features a conversion time of 5.0 μs for the A/D converter and a total conversion time of 8.0 μs; the MP2735-2, without a sample-and-hold, has a conversion time of 5.0 μs. The MP2735-2, which is designed specifically to be used with the dual channel MP282 Sample-and-Hold on one PC card, available as the Analogic SHAD2, features an increased dynamic range of 98 dB.

The MP2735, with the benefits of low power (only 1.5 watts), low cost, a wide analog power supply range of ± (10 to 15 volts), and excellent crossover linearity near zero volts, is the ideal choice for even the most demanding applications.

PRINCIPLES OF OPERATION

The MP2735 uses a two-step successive approximation (iterative) technique to attain a 15-bit analog-to-digital conversion in 5 μs. (Refer to the Functional Block Diagram of Figure 1 and the Timing Diagram of Figure 2). It has a unique internal architecture consisting of a buffer amplifier, an 8-bit ADC, an 8-bit DAC with 16-bit accuracy, associated timing and logic control with an internal reference and clock, parallel outputs, and an optional sample-and-hold amplifier that provides convenience and simplification of system integration problems.

If the optional sample-and-hold is not used (MP2735-2), the buffered analog input signal is presented directly to the ADC; if the sample-and-hold is used (MP2735-1), the signal is stored within the S&H capacitor. The ADC then converts the input signal to an 8-bit word accurate to within 0.5 LSB, and this digital output is stored in a holding register in the logic control.

The 8-bit DAC, with 16-bit accuracy, converts this digital output to an analog signal. An error amplifier expands the difference between this signal and the original analog input signal. That value is recirculated through the ADC, and the resulting 8 LSB's of the final 15-bit digital code are presented to the parallel output data bits. This second decision may change the 8 MSB's stored in the holding register from the first conversion since the MSB of the 8 LSB's and the LSB of the 8 MSB's overlap. These final 8 MSB's then enter the parallel output data bits, thus producing a 15-bit digital code of the original analog input.

The low harmonic distortion — 0.005% (−86 dB!) — is principally due to the sign/magnitude architecture of the 8-bit DAC. As opposed to conventional offset binary, the sign/magnitude architecture of the DAC provides excellent differential linearity; and to maintain that high differential linearity near zero volts, there is an internal 0.5 LSB offset of the DAC's output, thereby avoiding the "+0V" and "−0V" implicit in the sign/magnitude architecture.

This DAC also provides excellent stability and reliability over time and temperature. In offset binary converters resistor drifts fre-

quently cause significant linearity drift for signals near zero volts; for example, most resistors, except for laboratory standard wire-wound types, have tracking ratios greater than 15 ppm/year. However, converters with sign/magnitude architecture are four to five times less sensitive to resistor drift.

Thus, the MP2735, with its high noise power ratio, low power consumption, high speed, excellent stability and reliability, superb differential linearity, and exceptionally low harmonic distortion, offers superior, state-of-the-art performance.

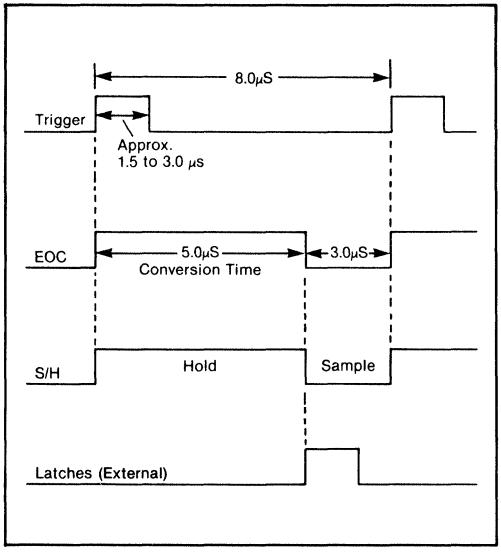


Figure 2. Timing Diagram of MP2735-1.

APPLICATIONS

Professional Audio Digitizing

The MP2735, with its wide dynamic range, low harmonic distortion, and ultra-low idle noise, is designed to meet the demands of professional audio applications, such as multi-track audio PCM systems or self-contained record and playback systems. With conversion rates of 125 kHz and 200 kHz for the MP2735-1 and MP2735-2, respectively, the frequency of this converter is more than adequate for high fidelity audio signals.

Since professional audio studios perform multi-track recording, processing signals from separate microphones, adjusting them according to desired tonal quality, and mixing them to attain the final product, signal sampling must occur at precisely the same time for each channel. When the MP2735-2 is used with the dual channel MP282A sample-and-hold, a pair of stereo channels can be sampled simultaneously at 55 kHz with 16-bit dynamic range.

A typical application is illustrated in Figure 3. Two inputs from separate microphones pass through anti-aliasing filters and are sampled simultaneously, or separately, by the MP282A, where they are multiplexed. Then the MP2735-2 converts each input to 15-bit digital data, which is combined with the gain ranging bit of the MP282A to provide 16-bit data for storage, processing, or mixing. The MP1926 converts the processed digital data back to an analog signal,

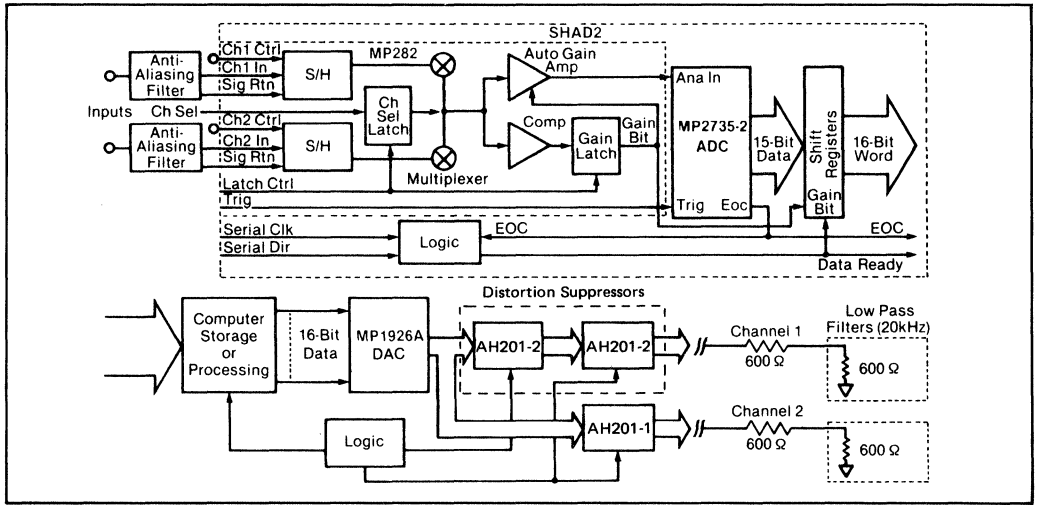


Figure 3. Professional Audio Application.

which, after being multiplexed, passes through a sample-and-hold, two deglitch amplifiers, and two low pass filters that include (sin x)/x compensation. The low harmonic distortion achieved with the MP2735 in a similar application is demonstrated in the spectral analysis shown in Figure 4.

The MP2735 is also applicable for a self-contained record and playback system, which does not require simultaneous sampling because incoming signals, although dual channeled, are not separated, manipulated, and mixed, but are played back immediately. The high speed MP2735 allows overlapping between signal acquisition from one channel and signal conversion from another.

Furthermore, for a single channel audio application, the 125 kHz conversion rate of the MP2735 is more than adequate for the 32 kHz sampling rate required for broadcast applications.

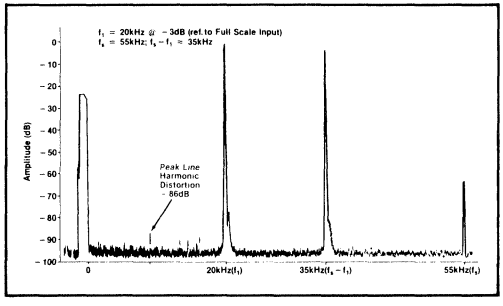


Figure 4. Photo of Spectral Analysis Showing Low Harmonic Distortion.

CALIBRATION

Although not usually required in practice, gain and offset may be adjusted through the top edge of the board. The offset should be adjusted until the least significant bit (LSB) of the output code, 100...00/1, alternates equally between "0" and "1" when the measured potential across pins A14 and A15 is – 0.000153V. The gain should be adjusted until the LSB of the output code, 111...10/1, alternates equally between "0" and "1" when the measured potential across pins A14 and A15 of the MP2735 is – 4.99954V.

TELECOMMUNICATIONS DIGITIZING

In a telecommunications application (refer to Figure 5) the MP2735-1 digitizes Frequency Division Multiplexing (FDM) group band signals for Digital Signal Processing. The frequencies of interest are in the band from 60 kHz to 108 kHz, thus a sampling frequency of 112 kHz is chosen.

All system measurements are specified with input and output filters in the system. The input filter limits the input signal to the frequency band of 60 kHz to 108 kHz, and the output filter has a passband of 60 kHz to 108 kHz. The composite D/A and filter will have a flat response over the 60 kHz to 108 kHz frequency range. The D/A output is gated with a deglitch amplifier to reduce the amount of (sin x)/x compensation and eliminate D/A glitches.

The MP2735 achieves a high NPR of 65 dB because of its low distortion and low idle noise. NPR is the measured decibel ratio between the noise level in one of the 12 channels with the baseband (60 — 108 kHz) fully noise loaded (typically at – 18 dB of full scale range) and the level in that channel with all the baseband noise loaded except in that channel.

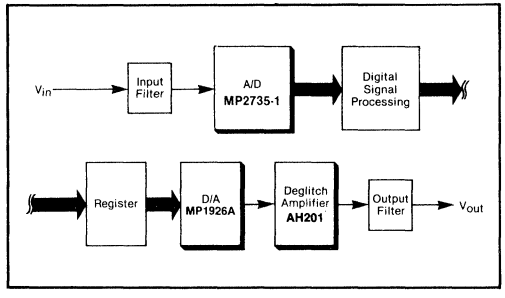


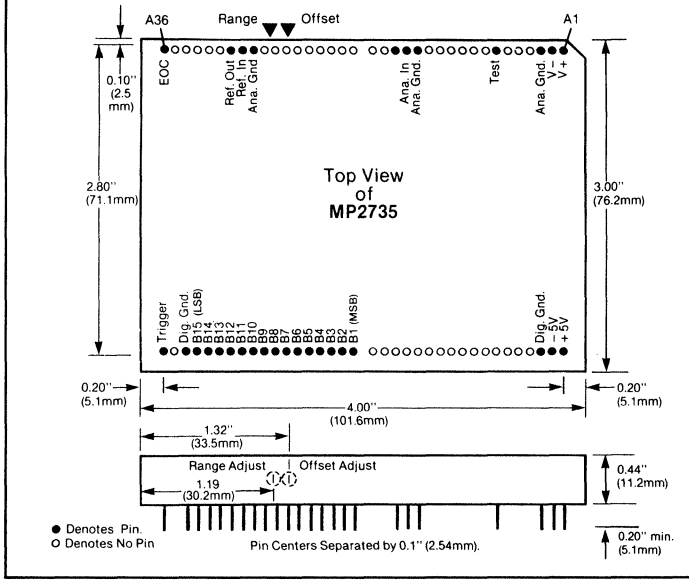
Figure 5. Telecommunications.

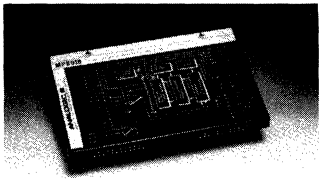
ORDERING GUIDE

For A/D Converter and Optional S/H:
Specify **MP2735-1**

For A/D Converter only:
Specify **MP2735-2**

MOUNTING DIMENSIONS AND PINOUTS





ANALOGIC®

MP8000 Series

14, 15 and 16-Bit A/D Converters

Description

The MP8000 Series of A/D converters offers the system designer a wide choice of resolution, conversion rate, analog input and digital output configuration, while providing high accuracy and long-term time and temperature stability. Resolutions of 14-, 15-, and 16-bits, at conversion rates externally adjustable from 0.6 — 2.5 μs/bit are accommodated. Input full scale ranges of 0V to +10V unipolar, or ±10V bipolar are pin-selectable, as is an input configuration of either low impedance single-ended, or very high impedance true differential (using an internal buffer amplifier). The digital output code may be pin-selected to provide either unipolar binary, offset binary or two's complement parallel data, or NRZ serial data formats, and the converters can be short-cycled to increase throughput if required.

The relative accuracy of each model in the MP8000 Series is appropriate for its resolution, ranging from 0.0015% to 0.006% FSR (16-bits to 14-bits respectively), while absolute accuracy (NBS traceable) is guaranteed from 0.003% to 0.006% FSR. Temperature stability is equally good, with tempcos for gain and offset of 5 ppm/°C and 2 ppm/°C. The Differential Linearity tempco is 1 ppm/°C, monotonicity is guaranteed and there are no missing codes over a 0°C to 60°C temperature range.

The MP8000 Series of A/D converters is packaged in a fully shielded 3" x 4.6" metal can. Pin locations and functions on all three MP8000 Series converters are identical and can be plugged into two standard 24-pin connectors for rapid insertion/removal. Internal potentiometers are provided for adjusting gain and offset.

Features

- **14-, 15-, and 16-bit Resolution**
- **High Accuracy**
  Relative Accuracy of 0.0015% to 0.006% FSR
- **Absolute Accuracy NBS Traceable**
  0.003% to 0.006% FSR
- **Single-ended or true differential input**
- **Parallel or NRZ Serial Output Data Format**
- **Short-cycle capability**
- **Excellent Stability**
  Gain Tempco 5 ppm/°C Offset Tempco 2 ppm/°C

Applications

- **Data Acquisition Systems**
- **Medical Electronics**
- **Automated Test Equipment**
- **Digital Audio**

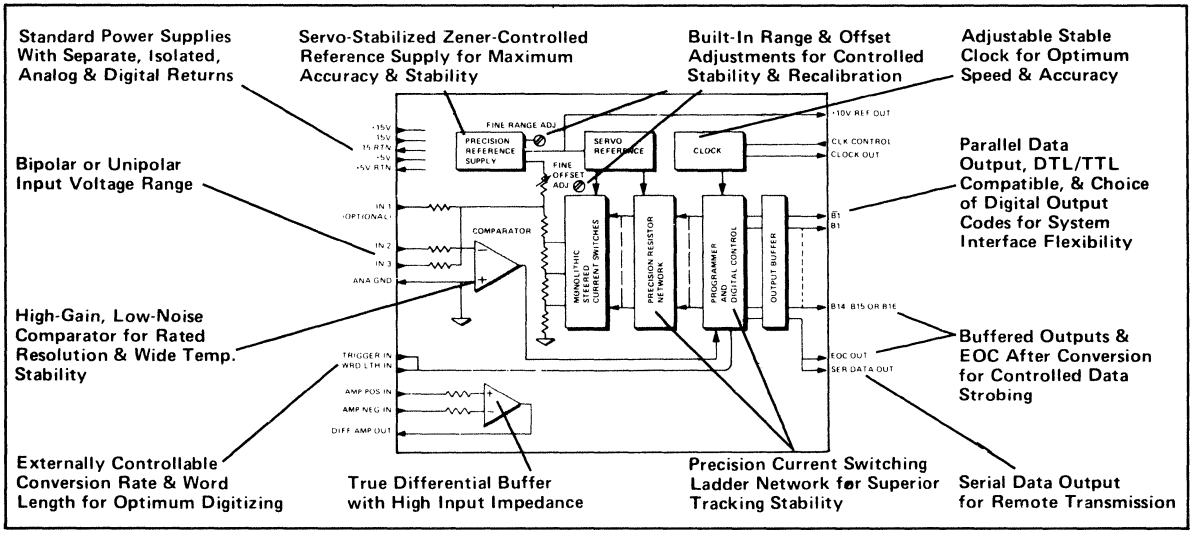


Figure 1. Functional Block Diagram for MP8000 Series.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Input Voltage (Full Scale Range)
0 to +10V unipolar; −10V to +10V bipolar

Input Configuration
Differential or direct, pin selectable

Input Impedance Differential
$10^9\Omega$

Direct, 0 to +10V FSR
2.5 kΩ

Direct, −10V to +10V FSR
5.0 kΩ

Common Mode Voltage Plus Signal
+11V max.

Common Mode Rejection Ratio
>75 dB

ACCURACY

Resolution (With Short Cycle Capability)
16 bits (MP8016), 15 bits (MP8015),
14 bits (MP8014)

Relative Accuracy
±0.0015% FSR max. @ 2 μs/bit (MP8016)
±0.003% FSR max. @ 1 μs/bit (MP8015)
±0.006% FSR max. @ .72 μs/bit (MP8014)

Absolute Accuracy (NBS Traceable)
±0.003% FSR max. @ 2 μs/bit (MP8016)
±0.006% FSR max. @ 1 μs/bit (MP8015)
±0.006% FSR max. @ .72 μs/bit (MP8014)

Quantizing Error
± ½ LSB @ 2 μs/bit (MP8016)
± ½ LSB @ 1 μs/bit (MP8015)
± ½ LSB @ .72 μs/bit (MP8014)

Monotonicity
Guaranteed @ 2 μs/bit (MP8016)
Guaranteed @ 1 μs/bit (MP8015)
Guaranteed @ .72 μs/bit (MP8014)

3σ Noise (Including Ref.)
300 μVp-p

STABILITY

Tempco of Differential Linearity
1 ppm/°C FSR max.

Tempco of Gain
5 ppm/°C FSR typ.; 10 ppm/°C FSR max.

Tempco of Offset
5 ppm/°C FSR max.

Clock Stability
0.1%/°C

Power Supply Sensitivity (per 1% Change in Power Supply Voltage)
0.0005%

Recommended Calibration Interval
6 months

Warmup Time to Spec. Accuracy
10 minutes

CONVERSION TIME

Clock Rate (Externally Adjustable)
1.0 to 2.5 μs/bit (MP8016)
0.8 to 2.0 μs/bit (MP8015)
0.6 to 1.5 μs/bit (MP8014)

LOGIC SIGNALS

Digital Output Codes
Unipolar: binary; bipolar: offset binary or 2's complement

Compatibility
Standards DTL/TTL logic levels, positive true B1 through Bn and $\overline{B1}$. Data available 100 ns (nominal) after EOC and remains at output register terminals until new TRIGGER occurs. Capable of driving 8 TTL Loads

Serial Data Outputs
After a complete conversion, SERIAL OUT remains in condition of last bit until new TRIGGER occurs

Trigger (Start Convert)
Conversion initiated by negative-going edge of positive or negative +3.5 ±1V pulse having 100 ns maximum transition time. Positive pulse width: 3 μs minimum; negative pulse width: 800 ns minimum
1 TTL Load

EOC (End-of-Converstion)
Negative-going signal with ≤20 ns transition time occurs @ leading edge of last clock pulse (100 ns before TRIGGER occurs). Capable of driving 10 TTL Loads

Clock (Internal) Output (see Fig. 3)
Negative-going pulse of 200 ns width. Maximum allowable external capacitance: 30 pF. Capable of driving 10 TTL Loads

Short Cycle Capability
8 to 15 bits (MP8016)
8 to 14 bits (MP8015)
8 to 13 bits (MP8014)

POWER SUPPLY

±15 ±0.5 Vdc
40 mA max.

−15 ±0.5 Vdc
65 mA max.

+5 ±0.25 Vdc
300 mA max.

ENVIRONMENTAL & PHYSICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
5% to 95%, noncondensing

Electrical Shielding
RFI 6 sides; EMI 5 sides

Dimensions
4 X 3 X 0.375 inches
(101.6 X 76.2 X 12.7 mm)

Right-Angle Connectors
15-300014, 2 each, supplied

USING THE MP8000 SERIES A/D CONVERTERS

Data Output

Both parallel and serial data output formats are available at the converter pins, plus an EOC (End-of-Conversion) indication at the end of the data output. (See timing diagram). The MP8000 Series provides for the control of the digital output word length so that the user can preselect any number of bits from 8 to either 14, 15, or 16. To operate this MP8016 converter at its full digital output capacity, externally connect the WRD LTH IN terminal (Pin 35B) to the B16 terminal (Pin 25T). To operate this converter at less than full capacity, thereby decreasing the total conversion time, connect Pin 35B to the desired bit output terminal (B8 to B15). For example, for 10-bit operation, connect Pin 35B to Pin 28T (B10).

Binary output coding is used for unipolar operation, while for bipolar operation, the parallel output data can be either offset binary or 2's complement, as pin selected by the user.

Timing

As shown in Figure 2 for the MP8014 converter, the negative-going edge ("1" to "0" transition) of the TRIGGER pulse enables: (1) EOC to high, (2) B1 to High (B1 to Low), (3) all other bit outputs (B2 to B14) to Low and (4) CLOCK pulse train. Conversion begins when the negative-going edge of the first clock pulse goes to Low. The bit decisions are made on successive negative-going pulse transitions with the MSB bit occurring at the second clock pulse.

Conversion is completed when EOC goes to Low on the negative-going edge of the last clock pulse. EOC remains at Low until the next TRIGGER pulse is initiated. Parallel data is available 100 ns after EOC goes to Low and remains valid at the output register terminals until the next TRIGGER pulse.

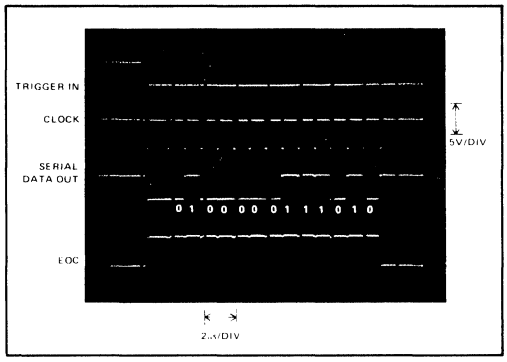


Figure 2. Typical Timing Diagram. (MP8014 shown)

The conversion rate can be user-controlled by connecting pin 12T (CLOCK CONTROL) through a 25 kΩ potentiometer to +5V as shown. Direct connection to +5V results in a minimum conversion rate. Pin 12T **must** be terminated as above for proper operation of the module; clock will not operate with 12T floating.

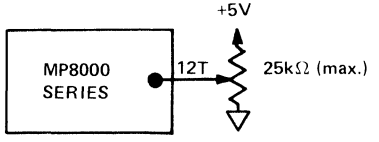


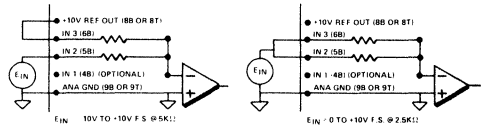
Figure 3. Conversion Rate Adjustment.

The 200 ns wide clock pulses are used to synchronize the transmission of serial data. After B1 is set to "1" by the TRIGGER pulse, the MSB decision is made one clock period later. Thereafter, each bit is set to "1" or "0" according to each successive decision, coincident with the negative-going edge of the clock pulses. After a complete conversion, NRZ SERIAL OUT remains in the condition of the last bit transmitted until a new TRIGGER pulse occurs. Pin 12T, connected in accordance with Figure 3, enables the internal clock.

Input Configuration

Figure 4 illustrates how the internal buffer amplifier may be configured for either a single-ended or differential input to the A/D converter.

For Standard (Direct Input) Impedance. The three input pins (IN 1, IN 2, & IN 3) permit user selection of the two input voltage ranges (+10V & ±10V) at low impedance (2.5 to 5 kΩ). Make the connections shown below.



For High (Differential Input) Impedance. The differential amplifier allows user selection of the two input voltage ranges (+10V & ±10V) at high impedance ($10^9\Omega$). Make the connections below.

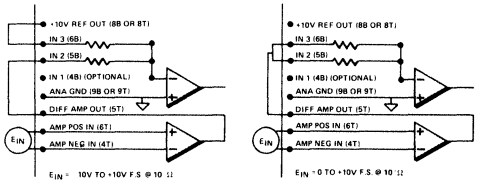


Figure 4. Input Configuration.

Calibration

Linearity and relative accuracy of the MP8000 Series converters are built-in. Absolute accuracy is established by factory calibration to NBS Standards. After extended periods of time, recalibration using the built-in offset and range controls can be accomplished as described below.

Zero Offset Calibration

Apply the low input voltage listed in Table 1. Adjust the OFFSET control so that the LSB of the appropriate output code alternates equally between "1" and "0". The OFFSET control should be readjusted whenever the selected full scale range is changed.

Range Calibration

Offset Should Be Calibrated Before Adjusting Range

Apply the high input voltage as listed in Table 2. Adjust the RANGE control so that the LSB of the appropriate output code alternates equally between "1" and "0". The RANGE control should be readjusted whenever the full scale range is changed.

Table 1. Offset Calibration Chart

Full Scale Range	Input Voltage		
	8014	8015	8016
0 to +10V	+305.2μV	+152.6μV	+76.3μV
−10V to +10V	+610.4μV	+305.2μV	+152.6μV

Table 2. Range Calibration Chart

Full Scale Range	Input Voltage		
	8014	8015	8016
0 to +10V	+9.99908V	+9.99955V	+9.99977V
−10V to +10V	+9.99817V	+9.99908V	+9.99955V

INPUT/OUTPUT DIGITAL CODING

14 BIT RESOLUTION	15 BIT RESOLUTION	16 BIT RESOLUTION
Unipolar Binary 11 111 111 111 111 = +9.99939V 00 000 000 000 000 = 0.0000V B1, B2 . . . . . B14 = Pin Label	**Unipolar Binary** 111 111 111 111 111 = +9.99970V 000 000 000 000 000 = 0.0000V B1, B2 . . . . . B15 = Pin Label	**Unipolar Binary** 1 111 111 111 111 111 = +9.99985V 0 000 000 000 000 000 = 0.0000V B1, B2 . . . . . B16 = Pin Label
Offset Binary 11 111 111 111 111 = +9.99878V 10 000 000 000 000 = 0.0000V 00 000 000 000 000 = -10.0000V B1, B2 . . . . . B14 = Pin Label	**Offset Binary** 111 111 111 111 111 = +9.99939V 100 000 000 000 000 = 0.0000V 000 000 000 000 000 = -10.0000V B1, B2 . . . . . B15 = Pin Label	**Offset Binary** 1 111 111 111 111 111 = +9.99970V 1 000 000 000 000 000 = 0.0000V 0 000 000 000 000 000 = -10.0000V B1, B2 . . . . . B16 = Pin Label
2's Complement* 01 111 111 111 111 = +9.99878V 00 000 000 000 000 = 0.0000V 10 000 000 000 000 = -10.0000V $\overline{B1}$, B2 . . . . . B14 = Pin Label	**2's Complement*** 011 111 111 111 111 = +9.99939V 000 000 000 000 000 = 0.0000V 100 000 000 000 000 = -10.0000V $\overline{B1}$, B2 . . . . . B15 = Pin Label	**2's Complement*** 0 111 111 111 111 111 = +9.99970V 0 000 000 000 000 000 = 0.0000V 1 000 000 000 000 000 = -10.0000V $\overline{B1}$, B2 . . . . . B16 = Pin Label

*To change to Offset Binary, use B1 instead of $\overline{B1}$.

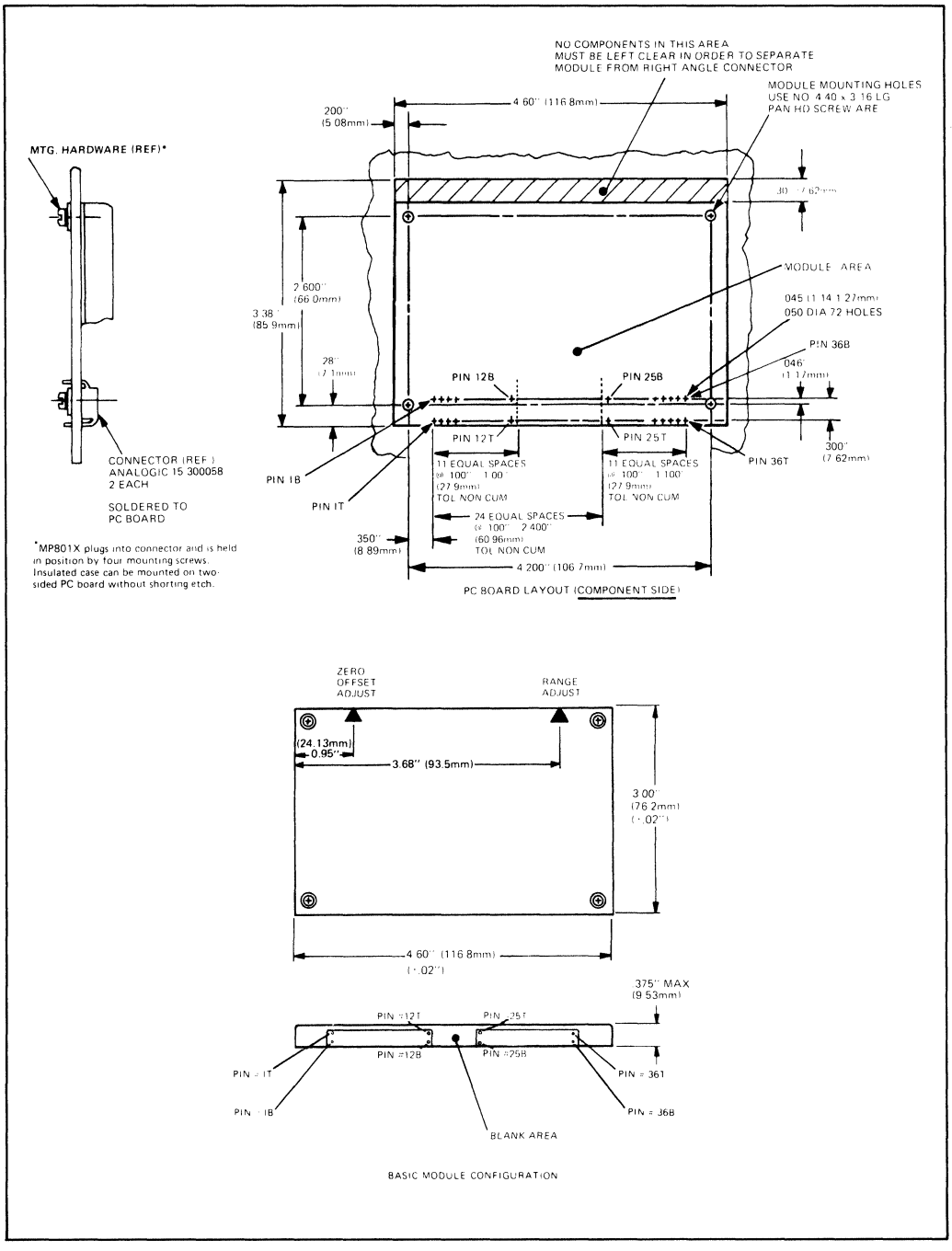


Figure 5. Mechanical.

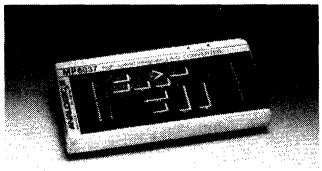
MP8000 SERIES PIN DESIGNATIONS

±15V RTN	**1B**	**1T**	±15V RTN
−15V	**2B**	**2T**	−15V
+15V	**3B**	**3T**	+15V
(OPTIONAL) IN 1	**4B**	**4T**	AMP NEG IN
IN 2	**5B**	**5T**	DIFF AMP OUT
IN 3	**6B**	**6T**	AMP POS IN
	7B	**7T**	
+10V REF OUT	**8B**	**8T**	+10V REF OUT
ANA GND	**9B**	**9T**	ANA GND
	10B	**10T**	
	11B	**11T**	
	12B	**12T**	CLOCK CONTROL

B15	**25B**	**25T**	B16
B13	**26B**	**26T**	B14
B11	**27B**	**27T**	B12
B9	**28B**	**28T**	B10
B7	**29B**	**29T**	B8
B5	**30B**	**30T**	B6
B3	**31B**	**31T**	B4
B1	**32B**	**32T**	B2
SER DATA OUT	**33B**	**33T**	$\overline{B1}$
EOC OUT	**34B**	**34T**	CLOCK OUT
WRD LTH IN	**35B**	**35T**	TRIGGER IN
+5V RTN	**36B**	**36T**	+5V

ORDERING GUIDE

For	Specify
14-Bit Modupac™	**MP8014**
15-Bit Modupac™	**MP8015**
16-Bit Modupac™	**MP8016**



ANALOGIC®

MP8037

17-Bit, Moderate Speed Triple-Slope Integrating A/D Converter

Description

Analogic's MP8037 is a ultra-high resolution, integrating A/D converter that provides exceptional performance in a smaller size and at a lower cost than previously available. The MP8037 is the first integrating converter to offer true 17-bit resolution. Its conversion speed of 250 conversions per second and TTL compatibility make it ideal for universal interfacing with the high precision data acquisition and control systems used in industrial, analytical and environments.

Performance Features

The MP8037 features an innovative quadraphasic triple-slope integrating conversion design that completes the 17-bit conversion, including autozero, in 4.0 ms maximum. The MP8037 automatically autozeros whenever it is in the standby mode, guaranteeing accurate conversions each and every time by effectively eliminating internal drifts. MP8037 relative accuracy (linearity), stability, and differential linearity are consistent with the unit's high 0.00075% FSR resolution. Absolute accuracy traceable to NBS standards is factory set to ±0.005% FSR and is adjustable to within ±0.002% FSR. Integral linearity within ±0.00075% FSR, differential linearity of ±0.00025% FSR, which guarantees monotonicity, assure meaningful 17-bit information.

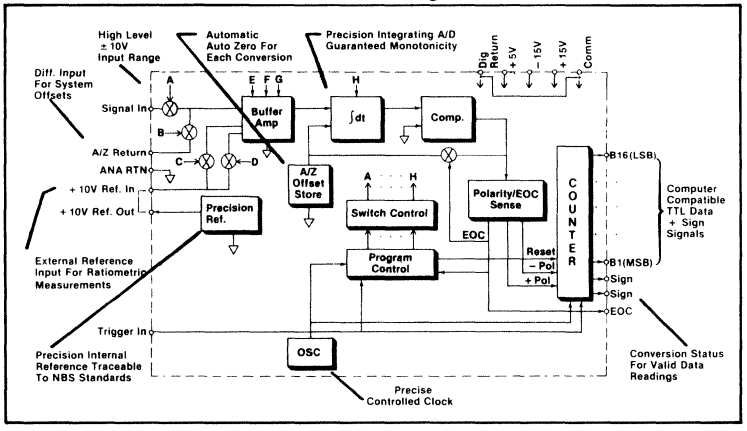


Figure 1. MP8037 Block Diagram.

Features

- **Ultra-high Resolution**
  17 bits (16 data, 1 polarity)
- **High Speed**
  Up to 250 conversions/second
  External trigger control
- **Small Size**
  Standard 2 x 4" Modupac™
- **High Accuracy & Stability**
  Linearity error <7.5 ppm FSR
  Auto-stabilized Zero
- **High Differential Linearity**
  ±2.5 ppm FSR
- **Guaranteed Monotonicity**
- **True Ratio Measurements**
  Pin-programmable precision internal reference
  Or user supplied external reference
- **Low Input Current**
  50 nA @ 100 conversions/second
- **High Input Impedance**
  1000 MΩ, minimum
  50 pF, maximum
- **Universal Data Systems Compatibility**
  Data fanout for 2 TTL loads

Applications

- **Precision Chemical Process Control Systems**
- **Digital Signal Processing Systems**
- **High Resolution Monitoring and Control Systems**
- **Precision Pharmaceutical Mixing & Grading Systems**
- **High Resolution Laboratory and R & D Systems**
- **Gas Chromatography**
- **Analytical Instrumentation**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG

Input Configuration
Differential (See Figure 4)

Input Range (Operating)
± 10V max.*

Input Range (Without Damage)
± 15V max.

Input Impedance
1000 MΩ min., 50 pF max.

Input Current
50 nA @ 100 conversions/second

Input Integration Time
640 μs*

ACCURACY (@ 25°C ± 5°C)

Relative Accuracy
± 7.5 ppm FSR max.

Differential Linearity
± 2.5 ppm FSR max.

Resolution
16 bits and sign

Noise
15 μV rms

Absolute Accuracy
± 0.005% FSR, without adjustment; ± 0.0027 FSR, adjusted

STABILITY

Zero Tempco
± 6 μV/°C max.

Gain Tempco
± 10 ppm/°C max.

CONVERSION

Technique
4-phase, triple slope integrating analog-to-digital conversion, autozeroed before each conversion

Rate
250 conversions per second, max., controlled by external command

SYSTEM INPUTS

External Trigger
0.1 μs min., negative pulse, TTL compatible, must drive 6 loads; 3 CMOS and 3 low-powered Schotky. Conversion starts on positive transition. See Figure 2

*Other values of Input Full Scale Range, Conversion Rate, or Integration Time are available on special order. Consult Factory.

DIGITAL OUTPUTS

Data Output
16 data bits, SIGN, and SIGN

EOC
High level indicates conversion is in process; low level indicates outputs are valid.
Allow 10 ns delay from EOC high to low transition before reading data

Compatibility
1 LS load each for 16 data bits; 2 TTL loads each for SIGN, SIGN, and EOC

Code Format
Sign and absolute value

POWER SUPPLY

± 5 Vdc ± 5%
200 mA, typ.

+ 15 Vdc ± 3%
20 mA, typ.

− 15 Vdc ± 3%
16 mA, typ.

ENVIRONMENTAL & MECHANICAL

Operating Temperature
0°C to 70°C

Storage Temperature
− 25°C to + 85°C

Relative Humidity
0 to 95%, non-condensing

Modupac™ Dimensions
2 x 4 x 0.440 in., (50.8 x 101.6 x 111.8 mm) (See Figure 7)

Shielding
RFI 6 sides; EMI 5 sides

SPECIAL FEATURES

Ratiometric Measurements
+ 10V ± 0% external reference may be used in place of internal reference. Connect to REF IN

External System Offset Compensation
± 50 mV max. may be compensated. Connect to A/Z RTN

Performance Features

The guaranteed differential linearity of the MP8037 makes it adaptable for use in computer-based data acquisition systems to accomplish statistical processing and achieve an effective resolution up to 20-bits.

Simple pin programming achieves true ratiometric measurements with 17-bit resolution by connecting an external in place of the precision internal reference.

The high quality performance of the MP8037 is confirmed by comprehensive computer-controlled factory acceptance tests, whose results are shipped with each module. Reliable performance is further supported by the Analogic standard QC procedure, including vendor qualification, rigid incoming inspection, and 100% burn-in cycling under power of all critical components.

Principles of Operation

The innovative quadraphasic design of the MP8037 completes a conversion in 4 phases, the operation of which may be best understood with reference to Figures 1 and 2. The four phases are: the autozeroing phase (AZ), the signal integration phase ($\int$ x), integration of ref high ($\int$ ref hi), and integration of ref low ($\int$ ref lo). Timing signals for each of the phases is developed in programmed read-only memory (PROM's) in response to input signal magnitude and polarity. When not in a conversion mode, the converter is placed automatically into its auto zero phase. The unit need only remain in this phase for a minimum of 600 μs to assure that the charge on the integrating capacitor is reduced to reference zero level. It also assures that the memory capacitor is charged to balance out any internal drifts as well as compensate for any external offsets introduced at the module pin connections.

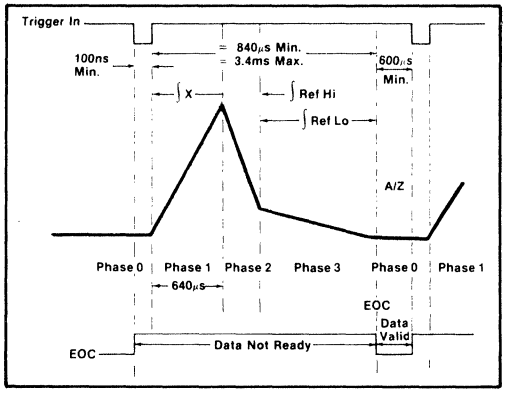


Figure 2. Quadraphasic Timing Waveforms.

When the trigger pulse is received, the low level transition causes the counters to be reset to zero. The rising edge generated by the return of the pulse to a positive level triggers the converter, and phase 1 begins. The input signal (and any stored AZ offset) is integrated for a period of 640 μs. Program control shifts the unit into phase 2, where the input signal is replaced by a high current, opposite polarity reference. This discharges the integrating capacitor at a high rate as shown in Figure 2. During this phase, the counters are incremented beginning with B9 counting up to B1 (MSB).

When the integrating capacitor has been discharged to a preset level, the program control begins phase 3. The high current reference is then replaced by a low current reference, and the low bit counters beginning with B16 (LSB) are incremented. This phase continues until the integrating capacitor is discharged to its initial value, when an end of conversion signal (EOC) is generated. At this time, the output data is valid, and program control is returned to the AZ phase. Suitable pauses are introduced between phases to eliminate conversion errors which could result from the settling of the program-switching circuits. The result is true 17-bit performance.

Initial Installation

As shown in Figure 3, the MP8037 is connected to the signal source, a trigger command, two sources of power (5 Vdc and ± 15 Vdc), and an optional external reference. The second signal input may be used to remove common mode voltages that may exist between signal and MP8037 grounds, or to introduce corrections to the input signal resulting from other system considerations.

The external reference, if used, should be within ±10% of the internal value of 10 Vdc. If an external reference is not used, then the REF OUT and REF IN pin terminals must be jumpered.

Be sure the MP8037 completes a conversion before applying a new trigger.

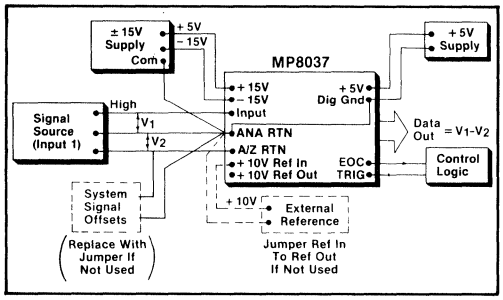


Figure 3. Connecting Power & signals to MP8037.

Calibrating The MP8037

The MP8037 is calibrated at the factory traceable to NBS Standards and is ready for immediate use. For special system applications, the 3-wire input capability of the MP8037 provides for high accuracy systems recalibration of the module to achieve true 17-bit system converter performance. As shown in Figure 4, connecting the system calibrating voltage source COM to the MP8037 A/Z RTN effectively removes up to ±50 mV of CMV between the two units.

Procedure:

Set the input for a value of +9.999977 Vdc Trigger the MP8037; read the binary data output.

Adjust the **+RANGE control for a positive full scale binary output** (1 1111111111111111), where the positive true **SIGN** bit is sensed, and set the control just past the transition of the LSB.

Reverse the input leads.

Adjust the **−RANGE control for a negative full scale binary output** (0 1111111111111111), where the positive true **SIGN** bit is sensed, and set the control just past the transistion of the LSB.

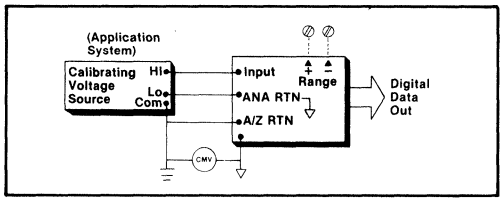


Figure 4. MP8037 Calibration Setup.

Input Connections to MP8037

Input Signals: The MP8037 encodes the difference between two input signals (Figure 5), thereby providing a differential input for systems applications. Small system ground-loop voltages, (up to 50 mV) common mode voltages, and minor system offsets are almost completely removed by using this 3-terminal input configuration as shown in the illustration.

Reference: True Ratiometric Measurements may be made with the MP8037 by replacing the internal reference with an external reference. Simply remove the jumper between pin terminals REF OUT and REF IN, and connect +10 Vdc ±10% between REF IN and ANA RTN.

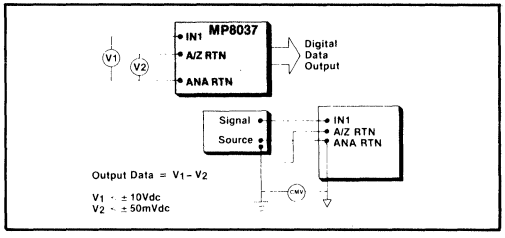


Figure 5. Connecting Input Signals to Remove CMV.

Typical Application

The MP8037 can be used to provide very wide dynamic range when connected as shown in Figure 6. Here the output of the Gas Chromatagraph is connected to a programmable gain amplifier (PGA). The output of the PGa is fed to the MP8037 and the selected gain is indicated by 3 output bits.

Once the gain has been properly set and sufficient time has been allotted after EOC for autozero, the Control Logic issues a convert command to the MP8037. When the EOC signal is obtained, valid 20-bit data digitizing a 21-bit input dynamic range is available at the output. In this system, the MP8037 A/Z RTN is jumpered to ANA RTN, and any CMV between source, system and measuring system grounds is rejected in the PGA.

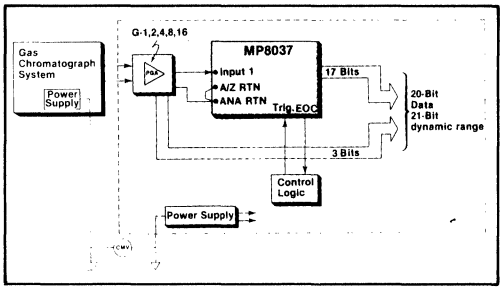


Figure 6. Using MP8037 for 20-bit Data Gas Chromatograph Instrumentation.

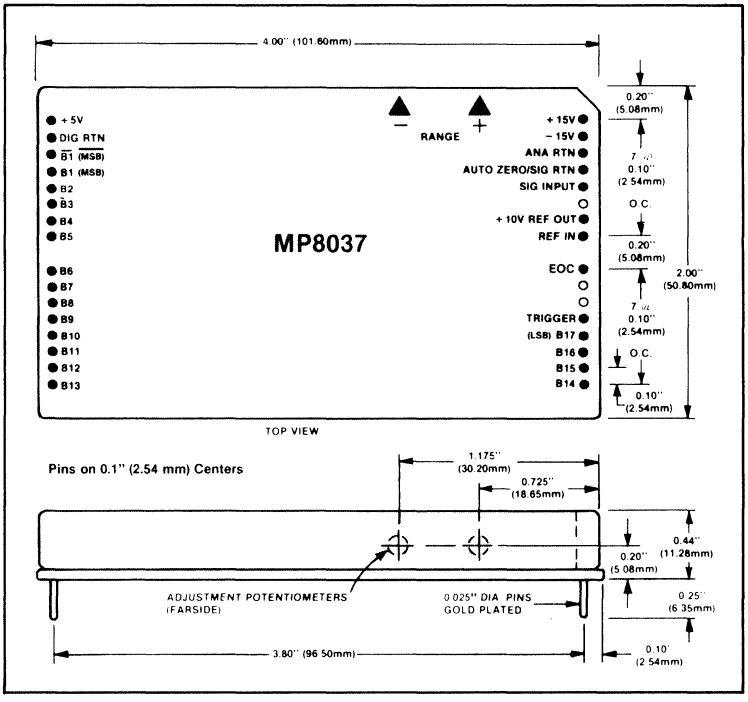


Figure 7. MP8037 Outline & Mounting Dimensions.

ORDERING GUIDE

Specify **MP8037.**

For Full Scale Ranges other than ± 10V, or for Signal Integration times other than 640 μs, or for Conversion Rates greater than 250 per second, Consult Factory.

ANALOGIC®

SECTION 5
Data Acquisition Systems

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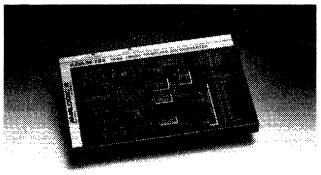
SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
Sampling Time or Phase Related Signals	Simultaneity	26 kHz Sampling Rate	ADAM-822	5-17
		51 kHz Sampling Rate	ADAM-812	5-13
High Speed Data Acquisition	14-Bit Resolution	Programmable Gain	ADAM-724	5-3
	16-Bit	Internal Sample & Hold (2.3 μs)	ADAM-826-1	5-33
		Buffered A/D (2.0 μs)	ADAM-826-2	5-37
		Unbuffered A/D (1.5 μs)	ADAM-826-3	5-41
Stereo Audio Digitizing	Low Distortion	Complete PCM Front-End	SHAD2A	5-53
Integral S/H and A/D, 20 kHz Throughput	Low Power	14-Bit Accuracy	ADAM-834A	5-45
		15-Bit Accuracy	ADAM-835A	5-45
	Stability	14-Bit Accuracy	ADAM-824A	5-23
		15-Bit Accuracy	ADAM-825A	5-23
Nuclear Event Monitoring	Ultra-High Differential Linearity	High Speed	MP8008R	5-49



ANALOGIC®

A/D/A/M-724

Very High-Speed 14-bit, Multifunction Sampling A/D Converter

Description

In a single low-profile module (0.375" high), the ADAM-724 provides a 6.8 μs, 14-bit, analog-to-digital converter plus three other user-accessible circuits — a sample-and-hold, a programmable gain differential amplifier, and a buffer amplifier. With this very high speed converter the ADAM-724 offers end-to-end throughput rates (including all four functions) that exceed 100,000 measurements/second. When used alone the converter provides throughput rates approaching 150 kHz. High accuracy has been maintained at these very high speeds; for example, end-to-end differential non-linearity is a superb ±0.003% FSR **max.** (± ½ LSB), with a tempco of only ± 3 ppm FSR/°C, **max.** A metal case preserves the module's performance in the presence of harsh electromagnetic and electrostatic interference. Moreover, using the ADAM-724 **costs less than combining separate circuits that offer lesser performance.**

The A/D/A/M-series of Analog Data Acquisition Modules was introduced to simplify the integration of high accuracy systems. Accordingly, the ADAM-724 offers *flexibility* and

(continued)

Features

- **Combined S/H, A/D, and Signal Conditioning in One Module**
- **Lower Cost than Separate A/D and S/H**
- **Latched, Tri-State Outputs,** Byte Selectable
- **Complete in Low Profile** 0.375" (0.95 cm) High, Shielded Case
- **User Accessible** 6.8 μs, 14-bit A/D
- **Input Flexibility**
  - Differential input
  - Low feedthrough S/H
  - Pin programmable input ranges to 50V
- **End-to-End Performance Better than Separate Modules**
  - ± ½ LSB, max., differential non-linearity
  - ± 3 ppm/°C FSR, max., non-linearity tempco

Applications

- **Precision Data Acquisition Systems**
- **Medical Imaging**
- **Telecommunications**
- **Automatic Test Equipment**
- **Industrial Process Control Systems**
  - High Speed Burst Sampling
- **Nuclear Instrumentation**

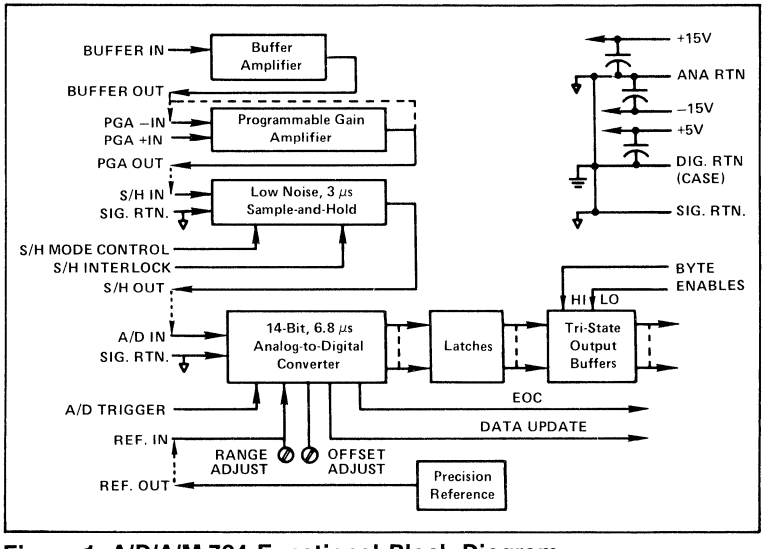


Figure 1. A/D/A/M-724 Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT[1]

Full Scale Range (FSR)
0 to +5V, 0 to +10V, ±5V, ±10V (See Table 3)

Impedance
10^9 Ω|| 10 pF

Bias Current
10 nA max.

Maximum Voltage[2] (signal plus common mode)
±11V

Offset
Adjustable to zero

ACCURACY @ 25°C[1]

Resolution
14 bits binary

Relative Accuracy @ 100 kHz[3] (combined performance of buffer amp, PGA, S/H & A/D)
±0.006% FSR max.

Absolute Accuracy[4]
±0.01% FSR max.

Differential Non-Linearity
± ½ LSB max.

Quantizing Error
± ½ LSB

±3σ Noise on 0 to +10V FSR
83 μV rms

Monotonicity
Guaranteed

DYNAMIC PERFORMANCE[1]

Throughput Rate
100 kHz min.

A/D Conversion Time
6.8 μs max.

S/H Acquisition Time
3.0 μs max.

S/H Aperture Delay Time
30 ns

S/H Aperture Uncertainty[5]
±0.4 ns

S/H Hold Mode Feedthrough
−86 dB min.

TEMPERATURE COEFFICIENTS

Differential Non-Linearity
±3 ppm/°C FSR/°C typ.
±8 ppm FSR/°C typ.

Gain
±8 ppm/°C typ.

Offset
±12 ppm FSR/°C typ.

Offset (A/D Only)
±3 ppm FSR/°C typ.

STABILITY

Warm-Up Time[2]
10 minutes

Recommended Calibration Interval
6 months

Power Supply Sensitivity (per 1% change in supply voltage)
±12 ppm FSR max.

POWER REQUIREMENTS

+15V ±3%
50 mA

−15V ±3%
50 mA

+5V ±5%
300 mA

ENVIRONMENTAL & MECHANICAL

Operating Temperature
0°C to +70°C

Storage Temperature
−25°C to +85°C

Relative Humidity
5% to 85% non-condensing to 40°C

Shielding
Electrostatic and electromagnetic

Package Size
4.6" x 3.9" x 0.375" (116.8 x 76.2 x 9.7 mm)

Digital Control Inputs[6,7] Table 1.

Signal	Fan In (unit loads)	High State = "1"	Low State = "0"	Comments
S/H MODE CONTROL	2	SAMPLE Mode (3 μs min) "1" = +3V min.	HOLD Mode (During conversion) "0" = 0.4V max.	10 ns max fall time
INTERLOCK	1	Inhibits SAMPLE Mode	No Effect	Normally tied to EOC
A/D TRIGGER	1/4	0.1 μs min.	0.2 μs min.	Negative edge starts conversion
HIGH BYTE ENABLE	1/4	Outputs at High Impedance	B1, B1 thru B6 active	—
LOW BYTE ENABLE	1/4	Outputs at High Impedance	B7 thru B14 active	—

Digital Outputs[6,7] Table 2.

Signal	Fan Out (unit loads)	Timing	Comments
B1 and B1 thru B14	2	Updated during the time that EOC is high **and** B15 is low	Parallel data from tri-state latches
End-of-Conversion (EOC)	2	Goes high 0.1 μs (typ.) after A/D TRIGGER fall. Goes low at end of conversion	B1 and B1 thru B14 are updated 0.1 μs before "1-to-0" transition of EOC
DATA UPDATE (B15)	2	"1-to-0" transition signals that B1and B1 thru B14 will update nominally 0.1 μs later	Will arbitrarily be a "1" or "0" between conversions

The A/D/A/M-724 is normally operated using its built-in precision reference (REF IN tied to REF OUT). For ratiometric operation see Table 5.

NOTES
1. **Digital inputs and outputs are TTL compatible.**
2. **See timing diagram.**

Description (cont.)

control simplicity. Thus system designers can easily exploit its speed in numerous high accuracy applications such as precision data acquisition systems and medical imaging systems. *Analog* flexibility is provided by the module's differential input amplifier, by user access to the 6.8 μs A/D converter (147 kHz throughput rate), and by a capability for ratiometric measurements. *Digital* flexibility is provided by latched, tri-state, byte selectable output buffers that will directly drive a computer system data bus. *Control* is simplified by a unique interlock on the S/H which allows a single, easy to generate, input signal to control both the A/D and S/H.

Further, as a part of the A/D/A/M-series, the module offers *overall* performance that has been optimized through use of a **rigorous** error budget. Systems using this module are not subject to the surprises that commonly occur when separate amplifier, S/H and A/D circuits are interfaced. The ADAM-724's **end-to-end accuracy is guaranteed** and is actually **better than that of many S/H circuits alone.**

USING THE ADAM-724

Accuracy

Interface problems commonly restrict accuracy in high speed systems that incorporate separate S/H and A/D units — problems such as ground loops, crosstalk, impedance mismatch, and radiated interference. Using the ADAM-724 totally avoids such problems. The module performs the functions of buffering, amplification, sampling, and conversion with its inputs and outputs interconnected per Figure 2. Figure 3 shows that *end-to-end accuracy of these four functions is exceptional, well within the specified ± ½ LSB differential non-linearity.*

Ease of Control

Using the ADAM-724 requires a minimum of control curcuitry. Conversions may be obtained via one control signal supplied in parallel to both the S/H MODE CONTROL input and the A/D TRIGGER (Figure 2). *This signal may be simply a 50% duty cycle square wave pulse train of frequency equal to the required conversion rate.* This duty cycle need not be carefully controlled, because connecting the EOC output to the S/H INTERLOCK input as shown automatically keeps the S/H in the HOLD mode during a conversion and returns it to SAMPLE when the conversion is complete.

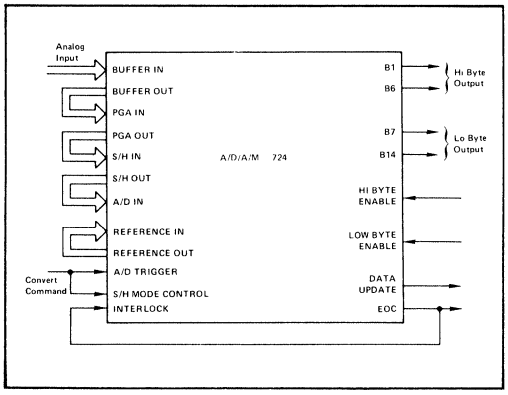


Figure 2. Typical Interconnection.

Interface Flexibility

The module's flexibility makes its accuracy and control simplicity available for use with a wide variety of analog front ends and digital processing/display subsystems.

Analog Interface Flexibility: A programmable gain amplifier allows pin-programming of bipolar and unipolar inputs, with ranges from 2V to 50V. The S/H reduces aperture uncertainty to ± 0.4 ns, allowing acquisition of high frequency inputs.

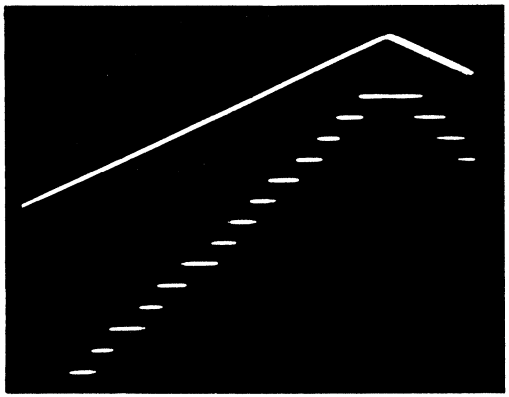
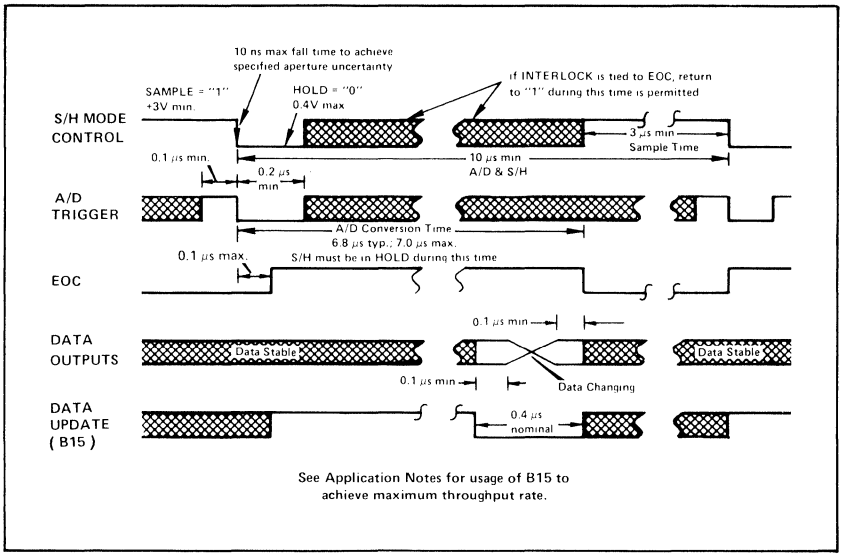


Figure 3. ADAM-724 Crossplot shows highly linear end-to-end performance.

Digital Interface Flexibility: The 14 parallel output data lines are tri-state buffered and may be enabled in two bytes for interfacing with an 8-bit wide data bus, or in one byte. The output of the ADAM-724 is statically available most of the time. Data from each measurement is latched at the end of the conversion (EOC) and then remains available during sampling and conversion of the next measurement. The data invalid time is the period between DATA UPDATE and EOC (nominally 0.4 μs; see SYSTEM TIMING). This latching architecture simplifies processor software by allowing nearly a full measurement period for reading the results of a conversion. For example, a system may trigger several ADAM-724 modules simultaneously and then sequentially strobe their outputs onto a common data bus.

BUFFER AMPLIFIER: This circuit's ultra-high input impedance minimizes source loading errors (especially useful when interfacing to an analog input multiplexer).

PROGRAMMABLE GAIN AMPLIFIER: The PGA is a differential amplifier used to provide scaling, offsetting, and inversion as detailed under RANGE PROGRAMMING. It accepts unipolar and bipolar inputs, and may be connected to provide gains from 0.2 to 5. Because the PGA is differential, it may also be connected to reject common mode voltage as shown under APPLICATIONS.



System Timing

SAMPLE-AND-HOLD: The Sample-and-Hold is a fast circuit with an acquisition time of 3 μs. Its low aperture uncertainty (Δt = 0.8 ns) reduces rms aperture error to ~1 LSB even at 50 kHz, the maximum information frequency of data that can be properly digitized without aliasing at the module's 100 kHz sampling rate (single channel application). This may be seen from the relationship:

rms error (%FSR) = 222 X f(Hz) X Δt(sec).

For multiple-channel applications, excellent feedthrough performance is obtained by switching the multiplexer channels coincident with the S/H switching to either mode.

The INTERLOCK input may be used to prevent switching of the S/H during a conversion. When the INTERLOCK signal is low, it has no effect. When INTERLOCK goes high, it inhibits the S/H from taking a new sample. (Suggested usage is to connect the EOC output, which is high during a conversion, to the INTERLOCK input. This allows the S/H MODE CONTROL to return to the SAMPLE state prior to the end of a conversion, yet keeps the S/H in the HOLD mode. At the end of the conversion EOC goes low and the S/H automatically switches to the SAMPLE mode.)

For arbitrary signal processing, you may connect directly to the S/H (see APPLICATION). Its input range is 0 to + 10V.

ANALOG-TO-DIGITAL CONVERTER: The A/D is a fast, current-steering successive approximation converter with low offset drift. It is user-accessible, providing up to a 128 kHz throughput rate when used with an external sample-and-hold such as the 1 μs MP271, or a 147 kHz throughput rate when used with no sample-and-hold. Its reference input allows true ratiometric measurements as shown under APPLICATIONS.

The A/D's outputs are from tri-state buffers which drive up to 2 standard TTL loads. The output devices are 74LS374 IC's.

For arbitrary signal processing, you may connect directly to the A/D. Its input impedance is 2.5 kΩ and its input range is 0 to + 10V. When using the A/D converter by itself, it is important to note that **THE LOGIC SENSE OF THE A/D OUTPUT, REFERENCED TO THE A/D INPUT, IS OPPOSITE THAT OF COMMON PRACTICE.** For a nominal + 10V input to the A/D, its output is all zeros; for a 0V input, its output is all ones. **THIS IS INVISIBLE TO THE MODULE USER WHO CONNECTS THE PGA PER RECOMMENDATIONS AS AN INVERTER WITH OFFSET.** (see RANGE PROGRAMMING for recommendations. Information published in this data sheet is based on the use of these recommendations.

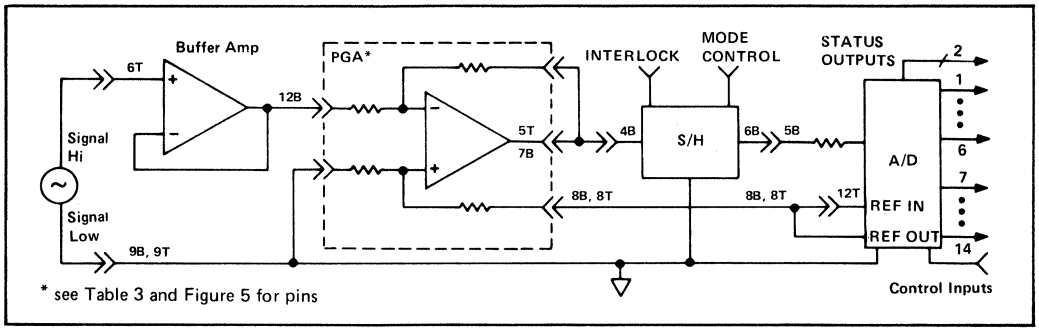


Figure 4. ADAM-724 Simplified Schematic.

RANGE PROGRAMMING

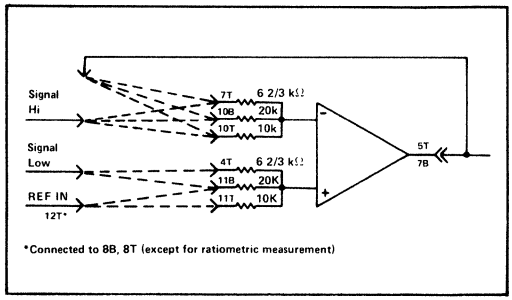


Figure 5. Programmable Gain Amplifier provides gains from 0.2 to 5 (to produce 0 to 10V output) and accepts differential inputs.

Nominal Full Scale Range	Signal High To	Signal Low[2] To	REF. IN To	PGA OUT To
+5V	7T & 10B	4T & 11B	11T	10T
+10V	10T & 10B	4T	11T & 11B	7T
±5V	10T & 10B	4T	11B	7T
±10V	10T	4T & 11B	11T	7T & 10B
± 10V Diff.				

Notes

1. For ±5V input range, pin 11T is not connected.
2. For single-ended operation also connect Signal Low to SIG RTN (pins 9B or 9T).

Table 3. Recommended PGA Connections.

Unipolar Binary

BA Input		B1, B2, ..., B13, B14
+9.99939V	=	11 111 111 111 111
0.00000V	=	00 000 000 000 000

Offset Binary

BA Input		B1, B2, ..., B13, B14
+9.99878V	=	11 111 111 111 111
0.00000V	=	10 000 000 000 000
−10.00000V	=	00 000 000 000 000

Two's Complement

BA Input		$\overline{B1}$, B2, ..., B13, B14
+9.99878V	=	01 111 111 111 111
0.00000V	=	00 000 000 000 000
−10.00000V	=	10 000 000 000 000

Comments:

1. BA = Buffer Amplifier.
2. For nominal +5V and ±5V ranges divide above input voltages by 2
3. Offset binary and two's complement differ only in using $\overline{B1}$ or B1 respectively as the MSB
4. Assumes PGA connected per Table 3.

Output Coding

APPLICATIONS

Direct Wiring to Data Bus

Figure 6 illustrates the easy connection of multiple ADAM-724 modules to a micro or mini-computer data bus. In applications such as multi-channel scanning systems several A/D converters may present data to a single bus-oriented computer system. The ADAM-724 data outputs may be connected directly to the bus lines and will drive them without the need for separate interface or pull-up components. The tri-state output devices allow direct wire "OR" connection. Because the outputs are latched, data may be transferred at any time, even during a conversion, except for a very short interval (nominally 0.4 μs). The 14-bit data word may be taken as two successive 8-bit bytes or as one 14-bit byte. Figure 6 shows right justification onto an 8-bit bus, with two diodes used to "zero-fill" the two MSB's of the High Byte.

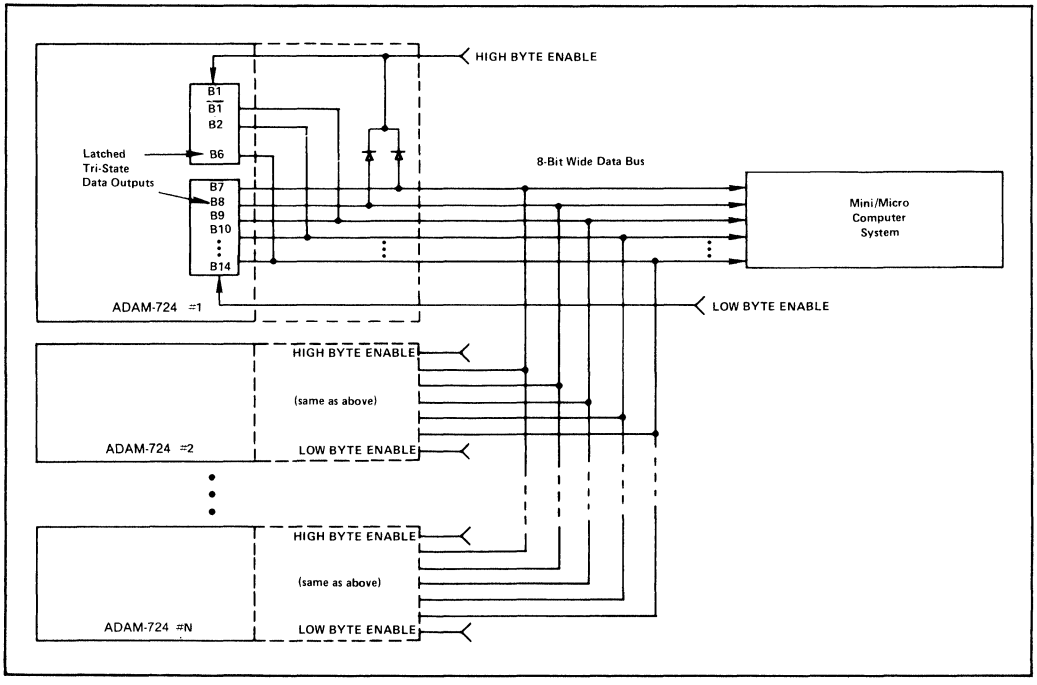


Figure 6. Connecting Several A/D/A/M-724's to a Data Bus is made simple by latched, two byte, tri-state outputs.

Rejection of Common Mode Voltage

Figure 7 illustrates the flexibility inherent in the ADAM-724. The internal buffer amplifier and the PGA, plus a single external buffer amplifier connected at the signal low input, form a high input impedance differential amplifier. This arrangement buffers the outputs of the multiplexer to provide full differential multiplexing. Common mode voltages of up to ±6V, for example due to the ground potential differences between the signal sources and the converter common, are rejected by this arrangement.

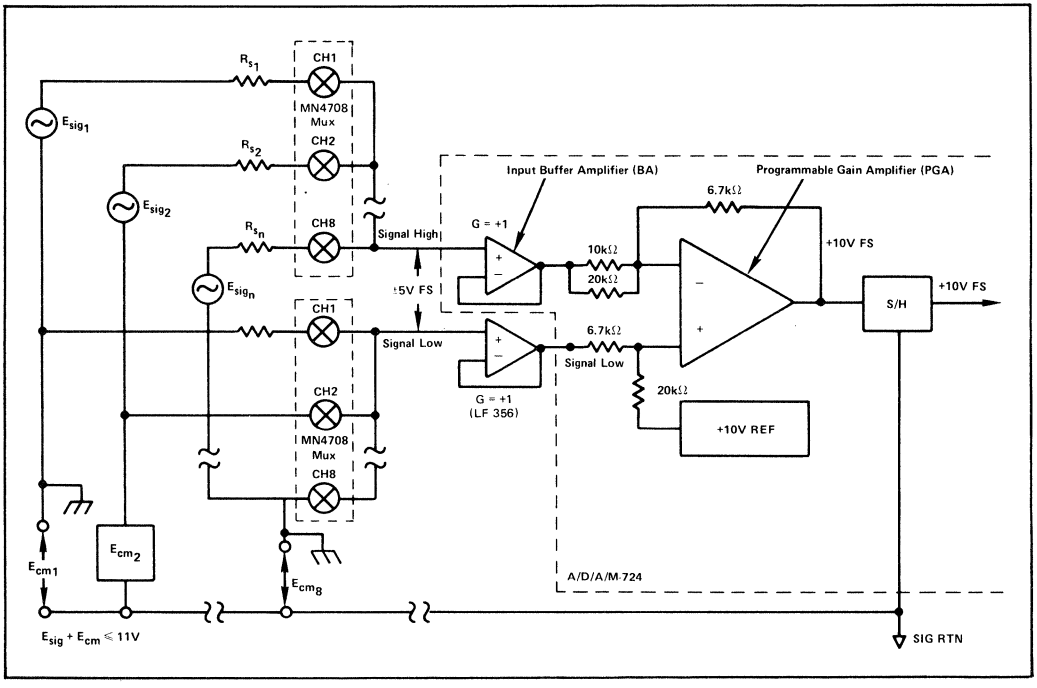


Figure 7. Rejection of Common Mode Voltages using the differential input capability of the A/D/A/M-724.

Automation Compensation

Figure 8 illustrates yet another advantage of the ADAM-724 — ratiometric operation. The output of the strain gauge, for example, is meaningful only with respect to its excitation voltage, *i.e.,* it is their ratio which conveys information. A common practice is to digitize both the strain gauge output and its excitation voltage, and then digitally compute the true reading. The ADAM-724 module allows the excitation voltage to be used in place of its internal precision reference. Slow variations of E_{ex} with time and temperature would then be compensated automatically, and there would be a corresponding reduction in computer loading.

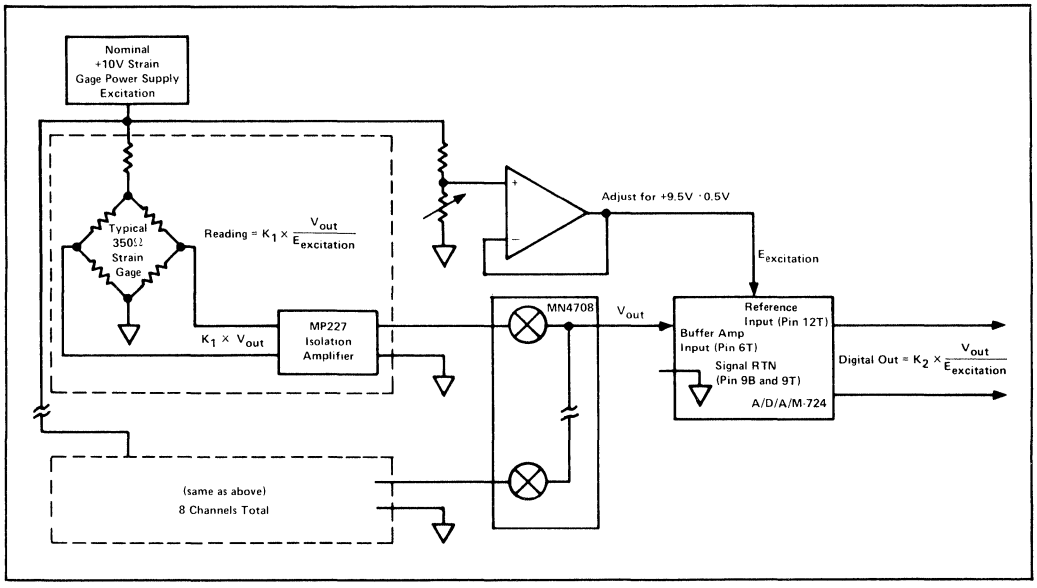


Figure 8. Automatic Compensation of strain gauge excitation voltage drift using the ratiometric capability of the A/D/A/M-724.

CALIBRATION

Due to its excellent long-term stability, the **ADAM-724** will rarely require recalibration. However, it should be recalibrated whenever the full scale range is changed.

Comments

1. Readjust the ZERO OFFSET control before readjusting the RANGE control.
2. The voltages in the Zero Adjust column of Table 4 are 1 1/2 LSB's below nominal FSR; those in the Range Adjust column are 1/2 LSB above the most negative point of the input range.
3. The span of each adjustment is ±0.1% FSR.

Zero Offset Adjustment Procedure

1. Apply the input voltage shown in Table 4.
2. Adjust the ZERO OFFSET control so that the LSB of the output code, 111 . . . 110/1 (B_1, . . .,B_{14}), alternates equally between "1" and "0".

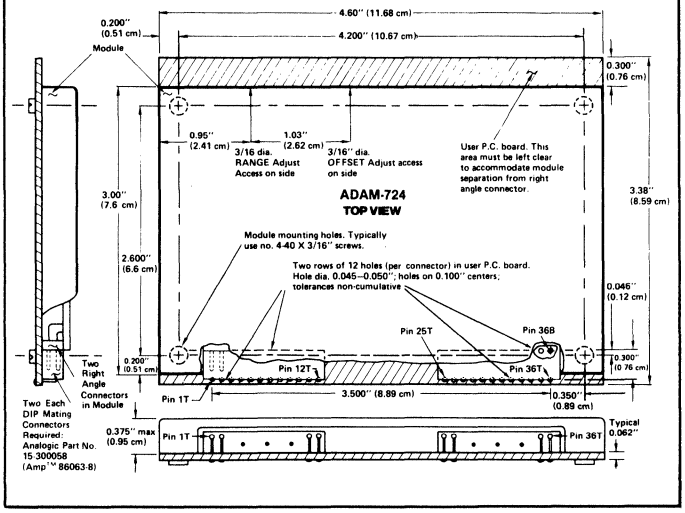
Range Adjustment Procedure

1. Apply the input voltage shown in Table 4.
2. Adjust the RANGE control so that the LSB of the output code, 000 . . . 000/1, alternates equally between "1" and "0".

Table 4. Buffer Amp Input Voltages for Module Calibration*

Nominal FSR	Zero Adj.	Range Adj.	LSB Size
0V to +5V	+4.99954V	+0.00015V	305 μV
0V to +10V	+9.99909V	+0.00031V	610 μV
−5V to +5V	+4.99909V	−4.99969V	610 μV
−10V to +10V	+9.99817V	−9.99939V	1221 μV

MOUNTING DIMENSIONS



Signal	Pin	Pin	Signal
ANA RTN*	1B	1T	ANA RTN*
−15V	2B	2T	−15V
+15V	3B	3T	+15V
S/H Input	4B	4T	6 2/3 kΩ PGA IN (+)
A/D Input	5B	5T	PGA Output
S/H Output	6B	6T	BUFFER Input
PGA Output	7B	7T	6 2/3 kΩ PGA IN (−)
REF Output	8B	8T	REF Output
SIG RTN*	9B	9T	SIG RTN*
20 kΩ PGA IN (−)	10B	10T	10 kΩ PGA IN (−)
20 kΩ PGA IN (+)	11B	11T	10 kΩ PGA IN (+)
BUFFER OUTPUT	12B	12T	REF Input
DATA UPDATE (B15)	25B	25T	INTERLOCK
B13	26B	26T	B14 (LSB of Low Byte)
B11	27B	27T	B12
B9	28B	28T	B10
(MSB of Low Byte) B7	29B	29T	B8
B5	30B	30T	B6 (LSB of High Byte)
B3	31B	31T	B4
(MSB of High Byte) B1	32B	32T	B2
HIGH BYTE ENABLE	33B	33T	$\overline{B1}$ ($\overline{MSB}$ of High Byte)
EOC	34B	34T	S/H MODE CONTROL
LOW BYTE ENABLE	35B	35T	A/D TRIGGER
DIG RTN*	36B	36T	+5V

Pins positions 13 through 24 not used.
— = Same signal available in two pins
*ANA RTN, DIG RTN, and SIG RTN are tied together internally.

Pin Designations

REFERENCE SPECIFICATIONS

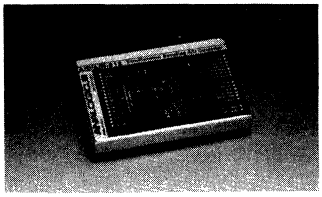
REFERENCE OUTPUT*		REFERENCE INPUT	
Voltage	+10V ±0.005V	Voltage	+10V nominal for full accuracy
Impedance	0.1 Ω	Range	5V to 10V
Current	1 mA	Bias Current	1 μA

*Independent of Range Pot Setting

Table 5

ORDERING GUIDE

Specify **ADAM-724**



ANALOGIC®

AIDIAIM-812

Dual Channel Simultaneously Sampling 51 KHz 12-Bit A/D Converter

Description

The ADAM-812 is a two-channel data acquisition system consisting of two simultaneously operating Sample-and-Hold Amplifiers (S/H) and a 12-bit Analog-to-Digital Converter (ADC). The dual S/H's allow near simultaneous (within 5 ns) sampling of time- or phase-related signals, thereby reducing the complexity of expensive hardware and/or software time-skew correction in systems such as quadrature demodulated signal processing front-ends, component transfer function testers, and colorimeters.

In systems using time-shared S/H's or dedicated S/H's controlled with insufficient simultaneity, the information contained within the time or phase interrelationship can be lost. Sequential sampling of these signals may require costly correcting of errors induced by the sampling process; these correction methods are of use only if the delay between the samples is known precisely. By sampling the input pair within 5 ns of one another, the ADAM-812 significantly reduces these sources of error.

The ADAM-812 provides a two-channel throughput rate of 51 kHz (single channel throughput of 91 kHz). ADAM-812 specifications are based on an end-to-end error budget that accounts for all internal error sources, including S/H droop at a 51 kHz sampling rate, errors due to aperture uncertainty for bandlimited signals up to 25 kHz, S/H pedestal non-linearities, and A/D non-linearities. The design of the ADAM-812 takes maximum advantage of the temperature and time stability of discrete components, and offers an end-to-end accuracy of ±1 LSB maximum; this is in direct contrast to monolithic S/H's which commonly exhibit more than 1 LSB equivalent error at the 12-bit level by themselves.

The fully integrated ADAM-812 is tested as a subsystem by ANALOGIC, which frees the system designer from performing a myriad of time-consuming design and testing tasks, and minimizes system production and test efforts. A fully tested and shielded subsystem, the ADAM-812 offers superior performance, ease of use and integration, at a lower cost than the parts alone for a custom design.

Features

- **Guaranteed Overall Transfer Accuracy**
  ±0.025% FSR, maximum
- **High Throughput Rate**
  51,000 two-channel samples per second
  91,000 single-channel samples per second
- **Low Aperture Uncertainty Time**
  5 ns—minimizes phase error between simultaneously sampled channels
- **Universal Data Systems Compatibility**
  Standard TTL digital inputs/outputs
- **Low Noise**
  165 μV rms
- **Separate Reference Input and Output**
  Allows ratiometric operation
- **Small Size**
  2" x 3" x 0.375"
- **RFI and EMI Shielded**

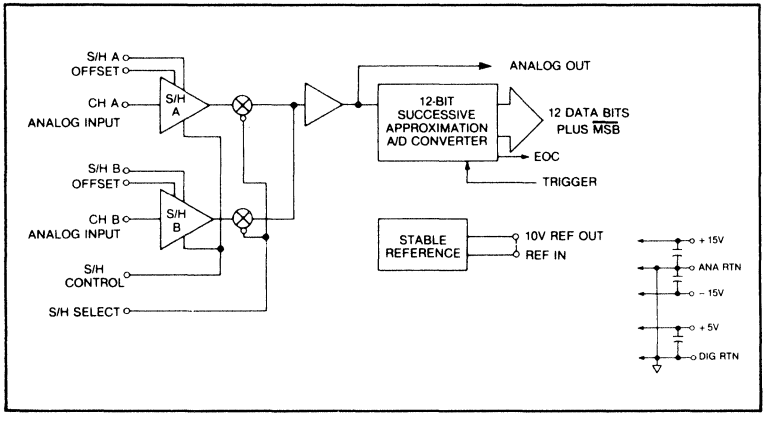


Figure 1. ADAM-812 Functional Block Diagram.

SPECIFICATIONS

(All Specifications guaranteed at 25°C unless otherwise noted.)

ANALOG INPUTS

Number of Channels:
2

Configuration:
Voltage Follower Input

Full Scale Range (FSR):
0 to +10V, ±5V, or ±10V; Factory configured

Maximum Input Without Damage:
±15V

Input Impedance:
>100 Megohms

Input Bias Current[1]:
<1 nA (at 25°C)

ACCURACY

(at 51 kHz Sampling Rate, at 25°C, nominal)

Relative Accuracy[2]:
±0.025% FSR, maximum

Differential Non-linearity:
±1/2 LSB, maximum

Noise:
165 μV rms maximum for 10V FSR; 320 μV rms maximum for 20V FSR; referred to input; measured over dc to 1 MHz bandwidth

Monotonicity:
Guaranteed; No missing codes

S/H Hold Mode Feedthrough Rejection Ratio[3]:
−82 dB minimim; measured with 1 kHz squarewave, full scale

Channel-to-Channel Crosstalk[4]:
−110 dB at 10 kHz

Total Offset Error (Untrimmed, including pedestal Error)[5]:
25 mV maximum; adjustable to zero

Gain Error[5, 6]:
±0.025% FSR, maximum

Gain Accuracy Between Channels:
±7.5 mV, maximum

DYNAMIC PERFORMANCE

Maximum Dual Channel Sampling Rate[7]:
2 samples/19.5 μs (51 kHz)

Maximum Single Channel Sampling Rate[7]:
1 sample/11.0 μs (91 kHz)

S/H Acquisition Time to 1/2 LSB:
4.5 μs maximum

S/H Droop Rate (at 25°C)[1]:
0.02 μV/μs, typical, 0.2μV/μs, maximum

S/H Multiplexer Settling Time to ±1/2 LSB:
Refer to Timing Diagram

S/H Aperture Delay Time:
50 ns typical

S/H Aperture Uncertainty Time:
5 ns typical

STABILITY

Differential Non-linearity Temperature Coefficient:
±3 ppm/°C FSR maximum

Offset Temperature Coefficient Unipolar:
±10 ppm/°C FSR Maximum

Bipolar:
±15 ppm/°C FSR maximum

Gain Temperature Coefficient:
±20 ppm/°C FSR maximum

Power Supply Sensitivity:
0.003% FSR per percent change in Supply Voltage

Warm-up Time to Specified Accuracy:
5 Minutes

DIGITAL INPUT/OUTPUT

General:
Inputs: 1 TTL LS Load, each; Outputs: 2 TTL Load Fanout, each

TTL positive true is Logic "1"

Logic "0" = 0.4V maximum for output; 0.8V maximum for input

Logic "1" = 2.4V minimum for output; 2.0V minimum for input

S/H Select:
Logic "0" selects S/H A,
logic "1" selects S/H B

S/H Mode Control:
Logic "0" selects HOLD mode, logic "1" selects SAMPLE mode for both channels

A/D Trigger:
Positive pulse, trailing edge triggered; 100 ns minimum pulse width

Data:
12 data bits plus MSB; binary, offset binary, or two's complement coding

EOC:
Logic "1" during conversion; "1" to "0" transition indicates data available

POWER REQUIREMENT[8]

+15V, ±3%
60mA maximum

−15V, ±3%
70mA maximum

+5V, ±3%
65mA maximum

ENVIRONMENTAL AND MECHANICAL

Operating Temperature:
0°C to +70°C

Storage Temperature:
−25°C to +85°C

Relative Humidity:
Up to 95%, non-condensing

Dimensions:
2:00" x 3.00" x 0.375"
(50.8 x 76.2 x 9.53 mm)

Shielding:
Electromagnetic 5 sides
Electrostatic 6 sides

NOTES:

1. Doubles every 10°C
2. Includes effects of input switching, buffer amplifier, S/H amplifier and ADC
3. Measured on S/H output, in HOLD mode with input signal as stated
4. Measured on Channel A S/H output with input grounded. Input signal applied to Channel B input. Both channels in SAMPLE mode
5. Offset and gain errors are externally adjustable to zero
6. With 50 ohm, 1% fixed resistor installed in series with Reference input
7. On ± 10V FSR
8. Digital ground, analog ground and case are tied internally

Typical Timing

Figure 2 depicts a typical timing relationship among the various control signals required by the ADAM-812. Channel A and B are simultaneously sampled, then sequentially converted to digital data.

The S/H amplifiers require 4.5 μs to simultaneously acquire the signals on both input channels (to within 1/2 LSB for a worst case full-scale input step). Once the signal pair is acquired, the S/H Control can be switched into the HOLD mode. If the application warrants, the S/H Control input can also be used as the A/D Trigger input.

The diagram indicates that the output data from the A/D converter is valid after a 10 ns delay from the logic "1" to "0" transition of EOC. The output data can be read at this time or at any time up to the next A/D trigger, since the last bit (LSB) decision is made, and the result settled prior to the EOC transition. The S/H Control can be switched to SAMPLE while the second data word is being read, with no effect on the data.

Offset

A separate, external 20 kohm multi-turn potentiometer for each S/H amplifier is recommended, per Figure 3. The +15V source used to power the ADAM-812 should be used for the offset circuit as well.

With S/H A selected and the S/H Control line at logic "1" (SAMPLE), supply the input indicated in the Calibration Voltages table to input A. Adjust the S/H A offset pot until the LSB of the output data word varies equally between 0 and 1. Repeat the above procedure for S/H B.

Gain

If gain trimming is required by the application, a 100 ohm, multi-turn potentiometer connected between the 10V REF OUT and REF IN pins per Figure 3 will provide an approximate ±0.25% FSR adjustment in gain. For many applications, a fixed 50 ohm, 1% resistor may be used in place of the trimpot.

Gain will rarely require recalibration in most applications. If gain is to be adjusted, follow the procedure below, after performing the offset procedure for both S/H's.

Select either the A or B S/H, and supply a logic "1" to the S/H Control line (SAMPLE). Supply the input indicated in the Calibration Voltages table to the selected input. Adjust the optional 100 ohm trimpot until the LSB of the data word varies equally between 0 and 1.

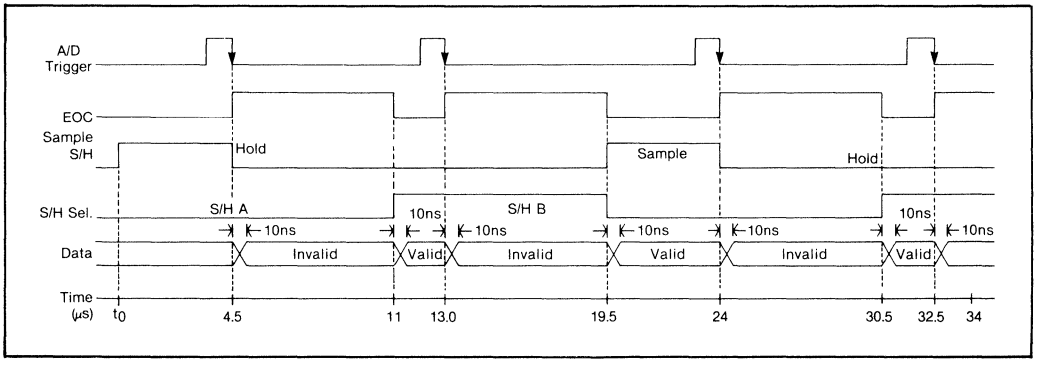
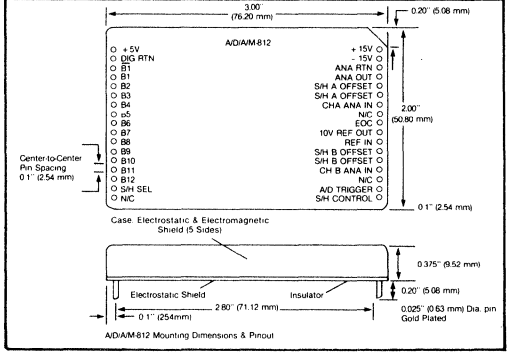


Figure 2. ADAM-812 Typical Timing Diagram for Single-Channel or Dual-Channel Simultaneous Sampling, ± 10V FSR.

Unipolar Binary												
Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9976V	1	1	1	1	1	1	1	1	1	1	1	1
0.0000V	0	0	0	0	0	0	0	0	0	0	0	0
Offset Binary*												
Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9951V	1	1	1	1	1	1	1	1	1	1	1	1
0.0000V	1	0	0	0	0	0	0	0	0	0	0	0
−10.0000V	0	0	0	0	0	0	0	0	0	0	0	0
Two's Complement*												
Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9951V	0	1	1	1	1	1	1	1	1	1	1	1
0.0000V	0	0	0	0	0	0	0	0	0	0	0	0
−10.0000V	1	0	0	0	0	0	0	0	0	0	0	0

Output Coding. *For ±5V Full Scale Range, divide voltages by 2

MOUNTING DIMENSIONS & PINOUTS



A/D/A/M-812 Mounting Dimensions & Pinout

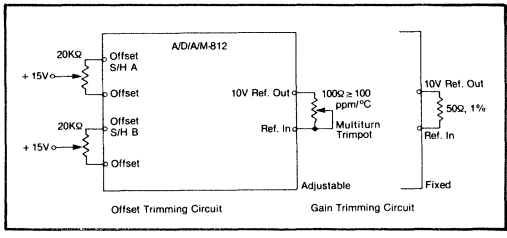
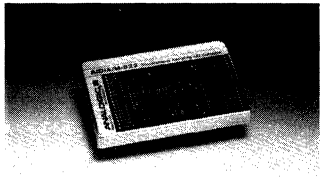


Figure 3. Gain and Offset Trimming of ADAM-812

Calibration Voltages			
Adjustment Procedure	**Input Full Scale Range**		
	0 to +10V	±10V	±5V
Offset	+0.0012V	+0.0024V	+0.0012V
Gain	+9.9976V	+9.9951V	+4.9975

ORDERING GUIDE

For an input voltage range of:	Specify:
0V to +10V FSR	☐ **ADAM-812-1**
±10V FSR	☐ **ADAM-812-2**
±5V FSR	☐ **ADAM-812-3**



ANALOGIC®

ADAM-822

Simultaneously Sampling Low Cost 12-Bit Analog-to-Digital Converter

Description

The ADAM-822 is a self-contained, two channel, analog-to-digital conversion module complete with two simultaneously operating sample-and-hold (S/H) amplifiers, a stable reference, and a 12-bit successive approximation A/D converter. An added feature is the fact that this unit includes four input channels that can be chosen in two groups of two each. This module has been designed to simplify the hardware and software of systems that utilize two or more phase- or time-related signal channels or cross-channel measurements such as quadrature demodulated signal processor front-ends, component transfer function testers, and colorimeters. By adding a multiplexer to each of the four inputs of the ADAM-822, a mini-DAS (Data Acquisition System) can be configured at a very modest cost.

In many systems, information of interest is often carried by the time-or phase-interrelationship among signal channels. Such information may be lost when time-shared S/H's are used or when dedicated S/H's are triggered with insufficient simultaneity. Sequential sampling of the related signals may require costly software correction of errors induced by the sampling process; such correction methods are generally useful only if the delay between samples is known precisely. The

(continued)

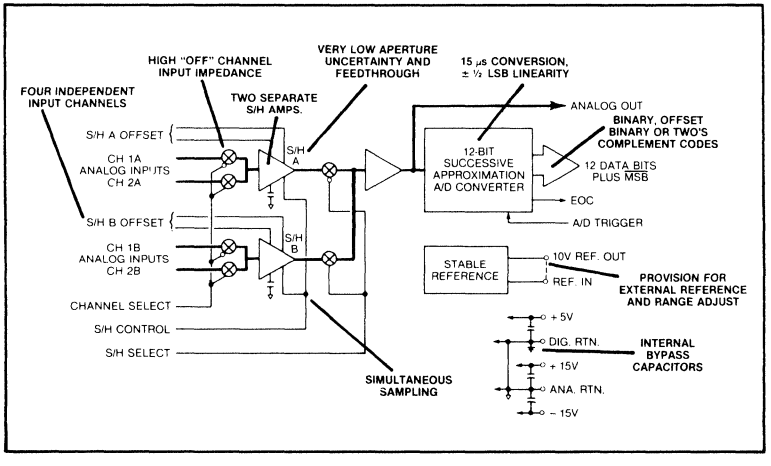


Figure 1. ADAM-822 Functional Block Diagram. High precision sample & holds ensure low aperture uncertainty and high measurement accuracy.

Features

- **Guaranteed Overall Transfer Accuracy**
  ±0.025% FSR, maximum
- **High Throughput Rate at Low Cost**
  Two Channels at 26,000 samples per second each
  Single Channel at 52,600 samples per second
- **Low Aperture Uncertainty Time—5 ns**
  Minimizes phase error between simultaneously sampled channels
- **Universal Data Systems Compatibility**
  Standard TTL digital inputs/outputs
- **Low Power**
  1.25W, typ.
- **Low Noise**
  0.01% FSR
- **Flexibility**
  Independently selectable input channel pairs
  Multiple units can be driven by single TTL line driver for multiple simultaneously sampled channels
- **Ratiometric Operation**
- **Superior Performance**
  Lower cost and higher overall accuracy when compared to functionally equivalent designs based on integrated circuits
- **Small Size**
  2" X 3" X 0.375"
  (50.8 X 76.2 X 9.53 mm)
- **RFI & EMI Shielding**

SPECIFICATIONS

ANALOG INPUTS

Number of Channels
4 (2 pair)

Configuration
Voltage follower input

Full Scale Range (FSR)
0 to +0V, ±5V, ±10V (see Ordering Guide)

Maximum Input Without Damage
±15V

Input Impedance
>100 MΩ

Input Bias Current
≤1 nA (at 25°C)

ACCURACY (at 26 kHz sampling rate and 25°C, nominal)

Relative accuracy[2]
±0.025% FSR max.

Differential Non-Linearity
± ½ LSB max.

±3σ Noise (Shorted input, measured over dc to 1 MHz Bandwidth)
0.01% FSR, p-p Referenced to input, max.

Monotonicity
Guaranteed; No missing codes

S/H Hold Mode Feedthrough Rejection Ratio[3]
−82 dB; 1 kHz square wave, full scale

Channel-to-Channel Crosstalk[4]
−110 dB @ 10 kHz

Offset Error (Untrimmed)[5]
25 mV, max.; adjustable to zero

Gain Error (Untrimmed)[5] [6]
±0.25% FSR max.

Gain Accuracy Between Channels
±7.5 mV max.

DYNAMIC PEFORMANCE

Maximum Dual Channel Sampling Rate[7]
26 kHz (2 samples/39 μs)

Maximum Single Channel Sampling Rate[8]
52.6 kHz

S/H Acquisition Time to ½ LSB
5 μs max.

S/H Aperture Delay Time
50 ns typ.

S/H Aperture Uncertainty Time
5 ns typ.

S/H Droop Rate (at 25°C)[1]
0.02 μV/μs typ., 0.2 μV/μs max.

Input Switching and S/H Multiplexer Settling Time to ± ½ LSB
Refer to timing diagram (Figure 2)

STABILITY

Tempco of Differential Non-Linearity
±3 ppm/°C FSR max.

Tempco of Offset — Unipolar
±10 ppm/°C, FSR max.

Tempco of Offset — Bipolar
±15 ppm/°C, FSR max.

Tempco of Gain
±20 ppm/°C, FSR max.

Power Supply Sensitivity
0.003% FSR/% change in V_{supply}

Recommended Recalibration Interval
6 months

Warm-Up Time to Specified Accuracy
5 minutes

DIGITAL INTERFACES

General
Inputs: 1 TTL LS Load, each; Outputs: 2 TTL load fanout, each

TTL positive true is logic "1"
Logic "0": 0.4V max. for outputs; 0.8V max. for inputs
Logic "1": 2.4V min. for outputs; 2.0V min. for inputs

Inputs

Input Channel Select
Logic "0" selects channel 1;
logic "1" selects channel 2

S/H Select
Logic "0" selects S/H A; logic "1" selects S/H B

S/H (Mode) Control
Logic "0" selects HOLD mode; logic "1" selects SAMPLE

A/D Trigger
Positive Pulse, trailing edge triggered; 0.1 μs pulse width minimum

Outputs

Data
12 data bits in Binary, 2's Complement, or Offset Binary (see Coding Table for format)

EOC
Logic "1" during conversion

POWER & ENVIRONMENTAL

Analog Power Requirements[9]
+15V ±3% @ 35 mA, typ. & −15V @ 35 mA, typ.

Digital Power Requirement[9]
+5V, ±3% 40 mA, typ.

Operating Temperature
0°C to 70°C

Storage Temperature
−25°C to +85°C

Relative Humidity
Up to 95%, non-condensing

Modupac™ Dimensions
2" x 3" x 0.375"
(50.8 x 76.2 x 9.53 mm)

Electromagnetic Shielding
5 sides

Electrostatic Shielding
6 sides

NOTES:

1. Doubles every 10°C.
2. Includes effects of input switching, buffer, amplifiers, S/H Amp and ADC.
3. Measured on S/H output, in HOLD mode with input signal as stated.
4. Measured on Channel A S/H output with input grounded. Input signal applied to Channel B input. Both channels in SAMPLE mode.
5. Offset and gain errors are extremely adjustable — see Figures 3 and 4.
6. With 50Ω, 1% fixed resistor installed per Figure 4.
7. On ±10V FSR.
8. On ±5V FSR; 50 kHz on ±10V FSR.
9. Digital Ground, Analog Ground, and case are tied internally.

Description (cont.)

ADAM-822 eliminates these sources of error and additional system cost by providing simultaneous sampling of either channel pair — within 5 ns of each other. For an equivalent system configuration, only half of the number of A/D converters need be used, further reducing overall system costs.

The specification for the ADAM-822 is based on an end-to-end error budget that accounts for all internal error sources, including S/H droop at a 26 kHz sampling rate, error due to aperture uncertainty for band limited signals up to 12.5 kHz, S/H pedestal non-linearities, input switching crosstalk, and A/D non-linearities. With a throughput time for two digitized samples of less than 40 μs, it provides 12-bit (±1 LSB) overall accuracy. The use of discrete component S/H amplifiers contributes greatly to the overall accuracy of the ADAM-822 — by contrast functionally comparable monolithic S/H's commonly exhibit more than 1 LSB equivalent error at the 12-bit level by themselves.

As a member of the ADAM Series of analog data acquisition modules, the ADAM-822 is fully integrated and tested as a subsystem. This frees the system engineer from performing a myriad of time-consuming design tasks and minimizes system production and test efforts. With no need to design a printed circuit layout for critical analog components, users avoid potential costly PC design iterations, which are commonly required to eliminate ground loops and other noise and error sources. A fully tested and shielded subsystem, the ADAM-822 offers superior performance, ease of use, and integration, at a lower cost than the parts alone for a comparable custom design.

Typical Timing

Figure 2 shows the typical timing relationship among the various control signals required by the ADAM-822. In this example, channels 2A and 2B are selected first. Their input signals are sampled simultaneously, then the samples are sequentially converted to digital data. Subsequently, the process is repeated for channels 1A and 1B.

The S/H amplifiers require 5 μs to simultaneously acquire the signals on both input channels (to within ½ LSB for a worst case full-scale input step). Once the signal pair is acquired, the S/H Control can be switched to the HOLD mode. Because the sample-to-hold mode settling time (input switch settling time) is less than the A/D Trigger's internal propagation delay, the S/H Control input can be used as the A/D Trigger input, if the application warrants.

The diagram shows input switch settling time and S/H Select settling time to be 2 μs each. These are the maximum times; typical values are 1 μs each. The diagram also shows that the output data from the A/D converter is valid at the instant of the EOC falling edge transition. The output data can be read at this instant or at any time up to the next A/D Trigger, since the last bit (LSB) decision is made, and the result settled, prior to the EOC transition. The S/H Control can be switched to SAMPLE while the data is being read, with no effect on the data.

ADJUSTMENTS & CALIBRATION

Offset

A separate, external 20 kΩ multi-turn potentiometer for each S/H amplifier is recommended, per Figure 3. The +15V source used to power the ADAM-822 may be used for the offset circuit as well.

With S/H A selected and the S/H Control line at logic "1" (Sample), supply the input indicated in the Calibration Voltages table to either Ch. 1 or Ch. 2. Adjust the S/H A offset pot until the LSB of the output data word varies equally between 0 and 1. Repeat the above procedure for S/H B.

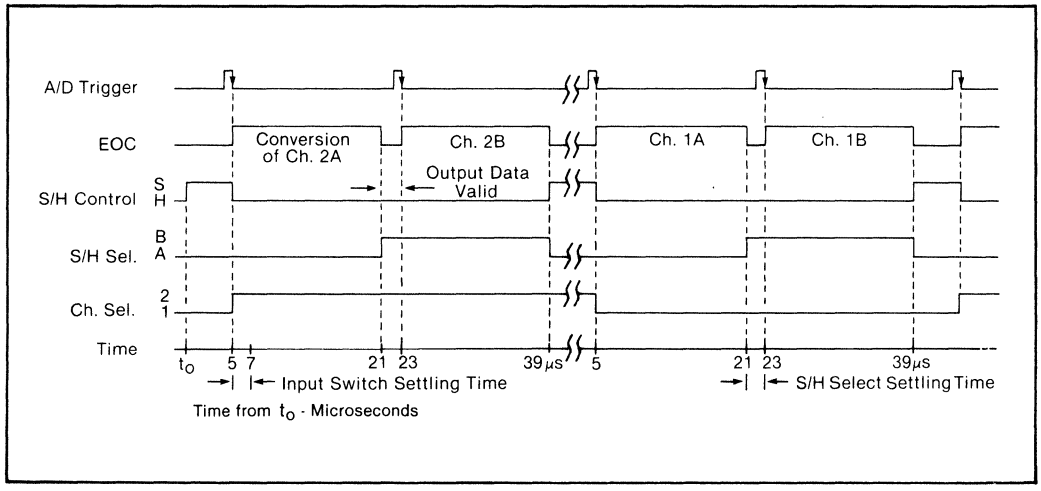


Figure 2. ADAM-822 Typical Timing Diagram for Dual-Channel Simultaneous Sampling, ± 10V FSR.

Gain

If gain trimming is required by the application, a 100Ω, multi-turn potentiometer connected between the 10V Ref Out and Ref In pins per Figure 4 will provide an approximate ± 0.25% FSR adjustment in gain. For many applications, a fixed 50Ω 1% resistor may be used in place of the trimpot.

Gain will rarely require recalibration in most applications. If gain is to be adjusted, follow the procedure below, after performing the offset adjust procedure for both S/H's.

Select any channel by providing the appropriate logic levels to the Channel Select, S/H Select, and S/H Control lines (S/H Control should be in the SAMPLE mode—logic "1"). Supply the input indicated in the Calibration Voltages table to the selected channel. Adjust the optional 100Ω trimpot until the LSB of the data word varies equally between 0 and 1.

Offset Binary*

Input	B1, B2, ..., B12
+ 9.9951V	111 111 111 111
0.0000V	100 000 000 000
− 10.0000V	000 000 000 000

Two's Complement*

Input	$\overline{B1}$, B2, ..., B12
+ 9.9951V	011 111 111 111
0.0000V	000 000 000 000
− 10.0000V	100 000 000 000

Unipolar Binary

Input	B1, B2, ..., B12
+ 9.9976V	111 111 111 111
0.0000V	000 000 000 000

*For ± 5V Full Scale Range, divide voltages by 2

Output Coding

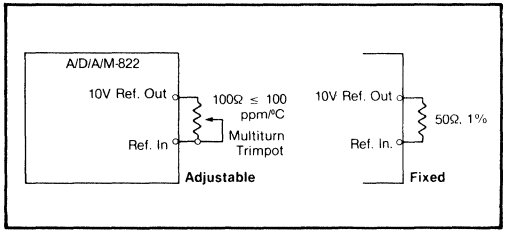


Figure 4. Gain Trimming Circuit.

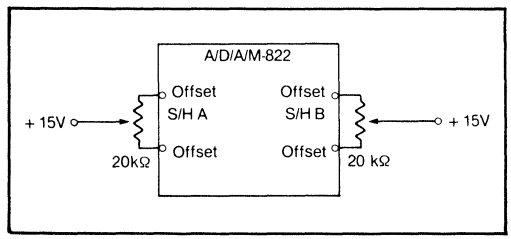
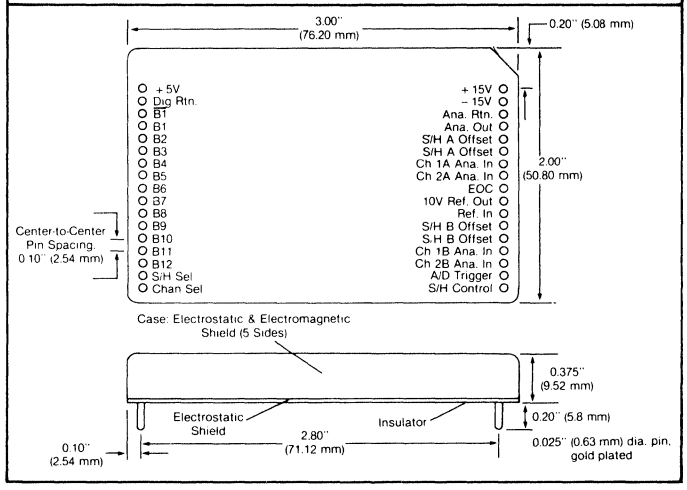


Figure 3. Offset Trimming Circuit.

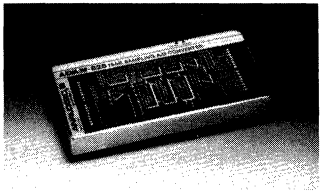
Calibration Voltages			
Adjustment Procedure	**Input Full Scale Range**		
	0 to + 10V	± 10V	± 5V
Offset	+ 0.0012V	+ 0.0024V	+ 0.0012V
Gain	+ 9.9976V	+ 9.9951V	+ 4.9975

MOUNTING DIMENSIONS & PINOUTS



ORDERING GUIDE

For an input voltage range of:	Specify:
0 to +10V FSR	☐ **A/D/A/M 822-1**
±10V FSR	☐ **A/D/A/M 822-2**
±5V FSR	☐ **A/D/A/M 822-3**



ANALOGIC®

ADAM-824A/ 825A

14- and 15-Bit Highly Stable, Low Power Sampling A/D Converters

Description

The **ADAM-824A** and **-825A** analog-to-digital converters (ADCs), with their integral sample-and-hold amplifiers, are complete data acquisition subsystems that provide overall accuracies better than many ADCs alone. This high level of accuracy is accompanied by improved stability and reduced power dissipation over previous converters of similar architecture. For example, with a differential linearity tempco of ±3 ppm, the 14-bit accuracy of the **ADAM-824A** is maintained over a full 20°C temperature rise! Due to the integral sample-and-hold (S/H) circuits, the **ADAM-824A** and **-825A** give the system designer optimized system performance and eliminate the potential difficulties in integrating the S/H and A/D of precision data acquisition systems.

Both the **ADAM-824A** and **825A** provide guaranteed end-to-end performance in a small 2" x 4" modular package. Their accuracy, along with features such as tri-state output, low power dissipation, and low cost, make them an excellent choice for a variety of data acquisition systems, automatic test equipment, and analytical instrumentation.

Features

- **Combined S/H and A/D in a 2" x 4" x 0.44" Module**
- **High Throughput Rate**
  20 kHz (Includes both sampling and conversion time)
- **Low Power**
  0.9W
- **Precision S/H**
  True 14-bit performance
- **Low Differential Nonlinearity**
  ±1/2 LSB maximum (824A)
- **Low Tempco**
  Differential nonlinearity ±2 ppm/°C FSR maximum (825A)
- **Low Noise**
  50 μV rms (ADC)
- **Byte-Selectable Tri-State Buffered Outputs**
- **Pin-Programmable Input Voltage Range**
  0V to +5V, 0V to +10V, ±5V, ±10V

Applications

- **Automatic Test Equipment**
- **Analytical Instrumentation**
- **Precision Data Acquisition Systems**
- **Materials Testing**

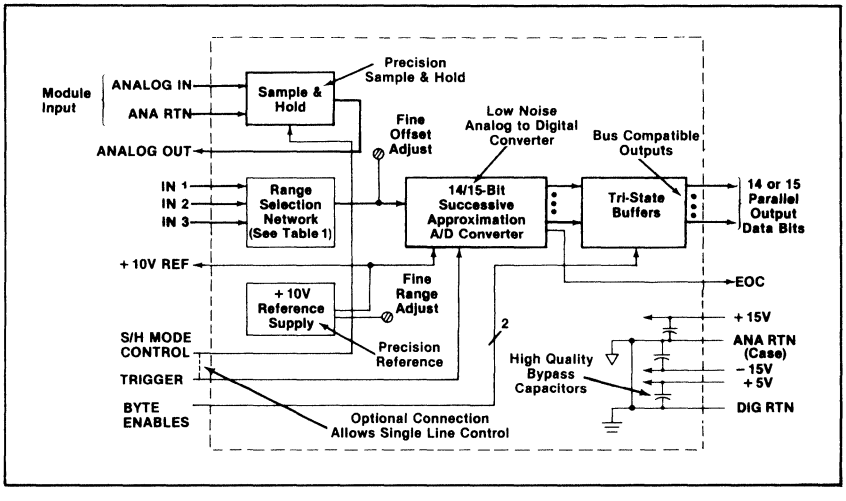


Figure 1. ADAM-824A/5A Functional Block Diagram.

SPECIFICATIONS

(Includes combined S/H and A/D performance, and applies to both ADAM-824A and ADAM-825A except where noted)
(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Full Scale Range (FSR)
0V to +5V, 0V to +10V, ±5V, ±10V

Maximum Input Without Damage
15V

Impedance
100 Megohm || 5 pF

Bias Current[1]
1 nA maximum

ACCURACY

Absolute Accuracy[2]
Calibrated to ±0.006% FSR

Relative Accuracy[3]
±0.005% FSR maximum (ADAM-824A),
±0.003% FSR maximum (ADAM-825A)

Differential Nonlinearity
±0.003% FSR maximum (ADAM-824A),
±0.002% FSR maximum (ADAM-825A)

Quantizing Error
±1/2 LSB

Noise (S/H plus A/D)
75 μV rms

Noise (A/D only)
50 μV rms

Monotonicity
Guaranteed

STABILITY

Differential Nonlinearity Tempco
±3 ppm/°C FSR maximum (ADAM-824A),
±2 ppm/°C FSR maximum (ADAM-825A)

Gain Tempco
±8 ppm/°C FSR maximum

Offset Tempco
±30 μV/°C typical, ±80 μV/°C maximum

Clock Stability
±0.03%/°C

Power Supply Sensitivity
±0.001% per 1% change in supply voltage

Warm-up Time to Specified Accuracy
5 minutes

Recommended Recalibration Interval
6 months

DYNAMIC PERFORMANCE

Maximum Throughput Rate[4]
20,000 measurement/seconds (ADAM-824A)
17,800 measurement/seconds (ADAM-825A)

S/H Aperture Delay
50 ns

S/H Aperture Uncertainty
1 ns

S/H Hold Mode Feedthrough Rejection
90 dB, measured with 20V p-p
10 kHz sinewave input

S/H Droop Rate[1]
0.2 μV/μs

S/H Dielectric Absorption Error[5]
±0.005% of input voltage change

DIGITAL OUTPUTS

General
Tri-state CMOS

Parallel Data
Positive true; unipolar binary, offset binary, or two's complement (see Table 1)

End of Conversion (EOC)
Positive true

DIGITAL INPUTS

General
Standard TTL compatible, one unit load/line

S/H Mode Control
Logic 1 = SAMPLE (6 μs minimum)
Logic 0 = HOLD (conversion time minimum);
logic 1 to logic 0 transition time 10 ns maximum

A/D Trigger
Negative-going edge; logic 1 to
logic 0 transition 50 ns maximum

Low/High Byte Enable
Logic 0 = enable

POWER REQUIREMENTS

±15V, ±3%
37 mA maximum

−15V, ±3%
29 mA maximum

+5V, ±5%
9 mA maximum

Power Dissipation
0.9W

ENVIRONMENTAL AND MECHANICAL

Operating Temperature
0°C to +70°C

Storage Temperature
−25°C to +85°C

Relative Humidity
5% to 95% noncondensing to 40°C

Shielding
Electrostatic (RFI) 6 sides;
Electrostatic (EMI) 5 sides

Package Size
2.0" x 4.0" x 0.44"
(50.8 x 101.6 x 11.18 mm)

Shielding
Electrostatic (RFI) 6 sides;
Electrostatic (EMI) 5 sides

Package Size
2.0" x 4.0" x 0.44"
(50.8 x 101.6 x 11.18 mm)

Notes:
1. Doubles every 10°C.
2. Traceable to NBS, calibrated on ± 10V range.
3. Worst-case summation of S/H and A/D nonlinearity errors.
4. Includes 6 μs maximum for S/H acquisition and 44 μs maximum for 824A A/D, 50 μs maximum for 825A A/D.
5. At maximum throughput rate. The error decreases as sampling time is decreased.

Operation

The **ADAM-824A** and **-825A** interface directly to most commonly available input devices (multiplexers, amplifiers, etc.). The high impedance of the fast, fully buffered, unity gain S/H input amplifier minimizes source loading errors. Excellent hold-mode feedthrough performance is provided even at 10 kHz—the maximum information frequency of data that can be digitized at the module's 20 kHz sampling rate (single-channel application). For multichannel inputs, excellent feedthrough rejection is maintained by switching the multiplexer channels coincident with either edge of the S/H mode control.

Parallel data bits are driven by tri-state buffers and may be enabled in one or two bytes. (If the tri-state feature is not needed, normal binary outputs can be obtained by connecting the enable pins to ground.) To obtain two's complement, use B1 instead of B1 (the MSB). Maximum system throughput rate is attained by reading the output of an A/D conversion while the S/H is acquiring the next sample.

To operate with a single control pulse, connect the S/H mode control input to the A/D trigger, and observe the timing requirements for the S/H mode control (Figure 2).

Operating range is established by connecting the S/H output to the appropriate A/D input pins (see Table 1). These pins provide access to the S/H output (a low-impedance buffer amp) for arbitrary signal processing prior to A/D conversion. The S/H can be bypassed for applications requiring direct input to a low noise A/D converter.

Performance Features

In most high accuracy applications the S/H, A/D, and related interfaces constitute the key subsystem of the data conversion process. By using an ADAM-series module that has been "worst-case" designed, the system engineer avoids the problems that commonly occur when transforming a 14-bit breadboard into a finished product.

End-to-end performance is not subject to the surprises that usually result from S/H output spikes, ground loops, timing problems, and so on. Offset is specified (and trimmed) as a single characteristic. The signal path from the S/H to the A/D is very short, minimizing noise pick-up, cross-talk, etc.; trim potentiometers and the bypass capacitors that filter power supply noise are in the module, not on the PC board. The module is EMI/RFI shielded.

The integral S/H is a precision circuit similar to Analogic's model MP260, so the total S/H error is very small. Due to the module's low power dissipation, errors induced by self-heating of the module are negligible. Internal temperature rise is only 12.5°C above external ambient, much less than in many other A/D converters.

The resulting performance is exceptional. Figure 3 shows a dynamic crossplot taken for the ***ADAM-824A*** *with worst-case inputs (small signals). This crossplot allows visual detection of very small errors (approaching 1/8 LSB). The unit displays differential nonlinearity that is well within the specified ± 1/2 LSB.*

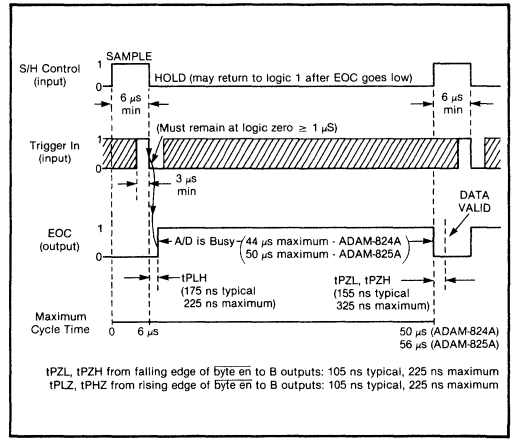


Figure 2. ADAM-824A/5A Timing.

A/D Input Connections

Full Scale Range	Connect IN 1 to	Connect IN 2 to	Connect IN 3 to	Input Impedance
0 to +5V	S/H ANA OUT	S/H ANA OUT	S/H ANA OUT	1.25kΩ
0 to +10V	ANA RTN	S/H ANA OUT	S/H ANA OUT	2.5kΩ
−5V to +5V	S/H ANA OUT	+10V REF	ANA RTN	2.5kΩ
−10V to +10V	ANA RTN	+10V REF	S/H ANA OUT	5.0kΩ

Output Codes

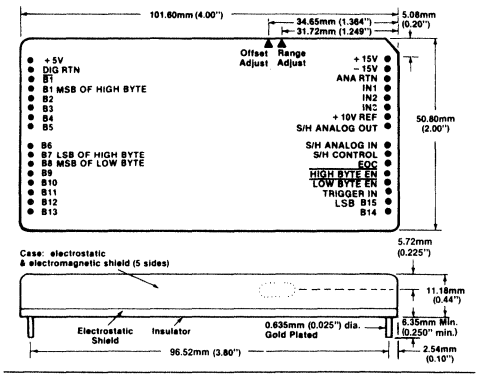
A/D/A/M-824A (14 bits)		A/D/A/M-825A (15 bits)	
Unipolar Binary			
11 111 111 111 111	= +9.99939V*	111 111 111 111 111	= +9.99969V*
00 000 000 000 000	= 0.00000V	000 000 000 000 000	= 0.00000V
Offset Binary			
11 111 111 111 111	= +9.99878V†	111 111 111 111 111	= +9.99939V†
10 000 000 000 000	= 0.00000V	100 000 000 000 000	= 0.00000V
00 000 000 000 000	= −10.00000V	000 000 000 000 000	= −10.00000V
Two's Complement			
01 111 111 111 111	= +9.99878V†	011 111 111 111 111	= +9.99939V†
00 000 000 000 000	= 0.00000V	000 000 000 000 000	= 0.00000V
10 000 000 000 000	= −10.00000V	100 000 000 000 000	= −10.00000V

*For +5V FSR, divide voltage by two

†For ±5V FSR, divide voltage by two

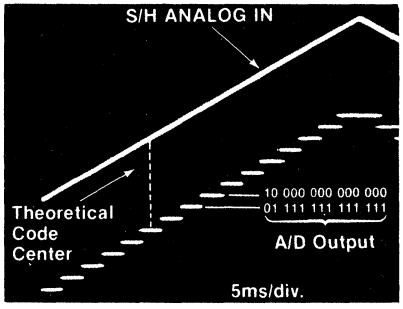
Table 1. Range Programming and Output Coding

MOUNTING DIMENSIONS & PINOUTS



Notes

- Pin spacing on 2.54 mm (0.10") centers. Double spacing between pins 8 & 9 as shown.
- ADAM-824A and -825A identical except B15 not used on ADAM-824A.
- Modupac™ may be mounted in any orientation.



The upper trace shows an input that ramps repetitively from −9.77mV to +9.77mV and back very slowly in relation to the module's 20kHz sampling rate. The module output is used to drive a digital-to-analog converter, whose output is then shown on the lower trace. Thus each level on the staircase corresponds to a set of conversions made around a code center voltage, and the transitions show when the module toggles its LSB. This type of plot may be used to measure differential nonlinearity (the most significant A/D performance parameter for most applications) and to determine by inspection the existence of errors such as wide code, narrow code, missing code, non-monotonicity, etc. Because the input is dynamically changing, this type of test simulates actual operation very well.

Figure 3. ADAM-824A/5A Crossplot Shows Highly Linear Performance.

CALIBRATION

Due to excellent long-term stability, these modules will rarely require re-calibration. They should, however, be re-adjusted when the selected FSR is changed. Offset should be zeroed prior to trimming the range.

Offset Zeroing Procedure

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Offset pot until the module output code corresponds to 0V, with the LSB alternating equally between 0 and 1.

Range Trimming Procedure (Gain Adjust)

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Gain pot until the module output code is all 1's, with the LSB alternating equally between 0 and 1.

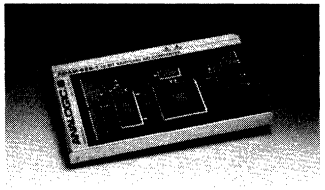
Input Voltages For Calibration

	ADAM-824A		ADAM-825A	
Nominal FSR	Offset	Range	Offset	Range
0 to +5V	153μV	+4.99954V	76μV	+4.99977V
0 to +10V	305μV	+9.99909V	153μV	+9.99954V
-5 to +5V	305μV	+4.99909V	153μV	+4.99954V
-10 to +10V	610μV	+9.99817V	305μV	+9.99909V

ORDERING GUIDE

Simply Specify

☐ **ADAM-824A**	**14-bit Resolution**
☐ **ADAM-825A**	**15-bit Resolution**



ANALOGIC®

A/D/A/M-826

High Performance, 16-Bit, 500 kHz A/D Converter Family

Description

The ADAM-826 is a 16-bit, 1.5 μs analog-to-digital converter (ADC) available with or without input buffer or Sample-and-Hold Amplifier. In any of its three input configurations, the ADAM-826 represents the ultimate combination of conversion rate, accuracy, flexibility, package size, and power dissipation.

The ADAM-826 converters have been designed to operate effectively in applications which involve either a single input channel or multiplexed signal sources, system configurations which often place different demands on the functions of the analog-to-digital converter (ADC) and sample-and-hold amplifier (S/H). The ADAM-826 is therefore an appropriate choice for Automatic Test Equipment, waveform analyzers, NMR and other applications requiring conversion rates to 500 kHz.

In many applications, differential linearity is of primary importance. All configurations of the ADAM-826 provide ± 1/4 LSB typical code differential linearity error and all are guaranteed to have NO MISSING CODES. Furthermore, the differential linearity is extremely stable over temperature, having a temperature coefficient of better than ± 1 ppm/°C.

Power dissipation is quite low, ranging from 2.75 watts (maximum) for the ADAM-826-3 to 3.5 watts (maximum) for the ADAM-826-1. All versions are available in two mechanical packages — the low profile Modupac® measuring 3"x 5"x 0.44", or an optional package with

(continued)

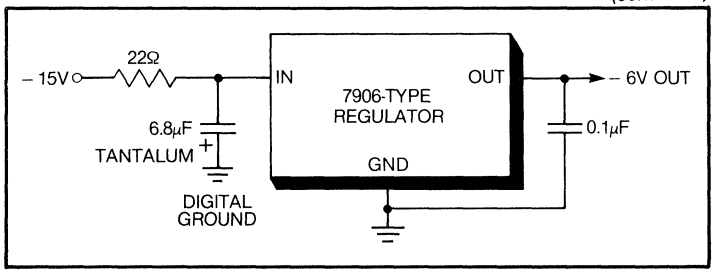


Figure 1. Deriving – 6V from – 15V Power Supply.

Features

- **16-bit Resolution**
- **Superb Differential Linearity**
  ± ¼ LSB typical code
  ± ¾ LSB maximum code
- **Excellent Stability**
  ± 1 ppm/°C max. differential non-linearity tempco
- **Flexible Configuration Capability**
  A/D Converter (**ADAM-826-3**)
  Highest Conversion Rate — 1.5 μs
  Buffered ADC (**ADAM-826-2**)
  100 MΩ Input Impedance
  2.0 μs Conversion Rate
  Sampling ADC (**ADAM-826-1**) — Guaranteed end-to-end specifications
  2.3 μs Sampling/Conversion Rate
  including S/H function
- **Unipolar/Bipolar Input** (Factory configured; specified on order)
- **Low Power**
  3.25 watts maximum for the ADC alone
  4.5 watts maximum for the ADC with S/H
- **Tri-state Data Output**
  Bus Compatibility
  Code Flexibility
- **Two Packaging Options Available**
  Pin solderable for lowest profile — Modupac®
  Plug-in socket mounted for ease of removal

Applications

- **Nuclear Magnetic Resonance**
- **Automatic Test Equipment**
- **Analytical Instrumentation**
- **Data Acquisition Systems**
- **Digital Audio/Communications**
- **Spectroscopy**
- **Signal Analysis**

Description (cont.)

connectors and mating pc board-mounted sockets (included) which allow the module to be easily removed from the board. (Available October, 1985).

Often it is impractical for users to adequately test 16-bit high speed ADCs, except by measuring overall performance in the completed system. Under these conditions, tracing an anomaly back to its source may prove exceedingly difficult. Therefore, Analogic recognizes its responsibility to provide units fully tested to meet guaranteed maximum and minimum specifications. Every ADAM-826 is subjected to extensive, automated testing and temperature cycling, followed by a final re-test, and is delivered to the customer with documented test data.

The ADAM-826 is offered in three configurations each of which is described more fully on the following pages:

The ADAM-826-1 — combines the ADAM-826 A/D with an extremely fast and accurate Sample-and-Hold Amplifier (S/H) (better than ±0.0015% in less than 800 ns for a full 20V step) to produce a complete acquisition and conversion in 2.3 μs.

The **ADAM-826-2** — provides a 100 MΩ input impedance buffer amplifier with full scale settling in less than 400 ns to yield an overall conversion rate of 500 kHz.

The **ADAM-826-3** — offers the designer the opportunity to take maximum advantage of the A/D's 1.5 μs conversion time by eliminating both the input buffer and S/H where the application or system architecture will allow.

We invite systems designers to take advantage of Analogic's considerable experience in implementing systems accurate to 16 bits and beyond. The suggestions given in the sections on PC Board Layout, Power Supplies and Timing in this Data Sheet will help eliminate a number of potential problem areas. If the need arises, we will be happy to provide personal assistance; please call on us directly.

USING THE ADAM-826

P.C. Board Layout

The analog input lead lengths should be as short as possible, preferably surrounded on both sides by an analog ground plane. The module has been carefully laid out internally to separate the analog input from the digital output and control lines. This practice should be extended to the pc board as much as possible. Figure 2 depicts a typical pc board layout illustrating the recommended routing, etch width and length, and grounding scheme.

Analog and digital ground should be totally separated in the system, except for the connection internal to the ADAM-826. If multiple ground connections in the system cannot be avoided, then the use of one, massive ground plane on the pc board is strongly recommended, with all ground connections made to this groundplane. This precaution will minimize both the effects of ground loops and the possibility of digital noise coupling into the analog circuitry.

Mechanical Packaging

The flexibility of the performance of the ADAM-826 is extended to its packaging options as well. The ADAM-826 is available in our standard Modupac, measuring 3" x 5", which when soldered into the pc board, will provide the lowest profile. Where board spacing is not a problem, and/or where ease of removal for recalibration is required, all versions of the ADAM-826 are offered with edge connectors and mating sockets (included) (available October, 1985). Both packaging options are illustrated in the Figures "MECHANICAL & PINOUT" for each version of the ADAM-826.

Power Supplies

In order to take advantage of the full 16-bit accuracy of the ADAM-826, it is recommended that well-regulated linear power supplies be used for the ± 15V required by the ADAM-826; these supplies must have no more than 5 mV p-p ripple. A switching supply must not be used for the ± 15V supplies. A linear +5V supply is recommended, although a switching type can be used since the ADAM-826 is well bypassed internally.

The required −6V may pose a problem for some designers whose systems do not have a −6V supply readily available. The −6V can be generated by using the circuit shown in Figure 1. The three terminal regulator can be any type of negative voltage regulator that can provide the 125 mA required by the ADAM-826. When this circuit is used, it is imperative that the ANALOG and DIGITAL RETURNS be tied together by a massive ground connection (plane) at the module.

Timing

Figures 5, 8, and 10 depict the typical timing of control signals and data output for each

version of the ADAM-826. All versions of the converter are triggered on the falling edge of the Trigger pulse applied to the TRIGGER INPUT pin. The minimum and recommended pulse width is 50 ns, with a maximum width of no more than 200 ns.

The TRANSFER (XFER) line is normally high. Approximately 225 ns prior to the time when valid data is available at the converter's outputs, XFER goes low, and remains so for 175 ns. At the end of this time, XFER again goes high. This rising edge loads the data for the just completed conversion into the tri-state output latches. After a delay of 50 ns from this rising edge, the data is valid. Therefore the actual conversion is completed when XFER goes low.

Data Outputs

The 16-bit data available in the tri-state output latches at the end of a conversion can be formatted in any of three ways. For a 0V to +10V FS input signal, the output data is unipolar binary; for bipolar ±10V FS inputs, using B1 (MSB) as the sign bit provides offset binary data; $\overline{B1}$ ($\overline{MSB}$) provides two's complement data.

Unipolar Binary		
MSB		LSB
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99985V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.00000V
B1,B2, ... B16	=	Pin Label
Offset Binary		
MSB		LSB
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99970V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.0000V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	−10.0000V
B1,B2, ... B16	=	Pin Label
2's Complement		
MSB		LSB
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99970V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.0000V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	−10.0000V
B1,B2, ... B16	=	Pin Label

Table 1. Output Coding for ADAM-826 Family.

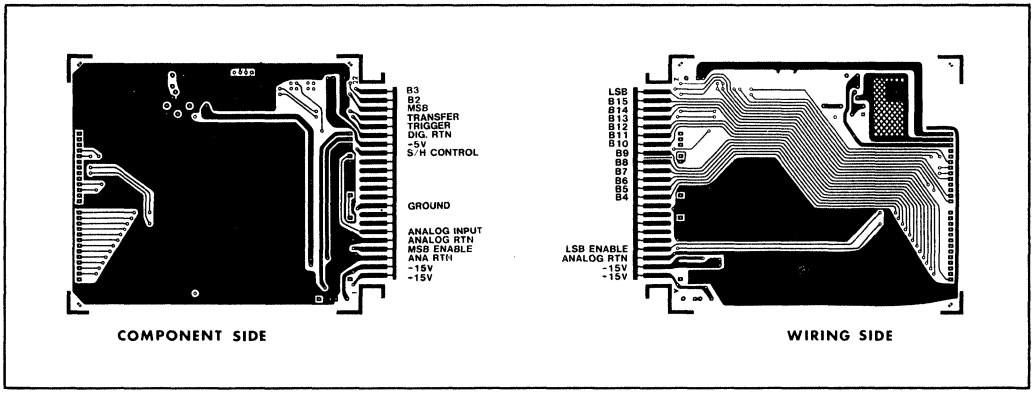


Figure 2. Typical PC Board Layout.

If the −6V power supply voltage is derived from the −15V supply on the pc board, then an additional heavy ground connection between power supply returns back at the supplies themselves is suggested. This will provide a "path of least resistance" for the −6V return current back to the −15V supply (see "Correct Method" in Figure 3). If this path is not provided, the IR drop between the DIGITAL and ANALOG RETURN's can become significant relative to 1 LSB at the 16-bit level (see "Incorrect Method" in Figure 3). If the −6V is NOT derived in this manner, this connection is not necessary.

LC filtering on the power supply inputs should be used right at the **ADAM-826** module. A 100 μH inductor and a 15 μF capacitor are recommended. If the −6V regulator is used, then an RC low-pass filter of 22Ω (1 watt) and 6.8 μF (20V) at the input of the regulator is required. The LC filter above should be used at the −6V input to the **ADAM-826.**

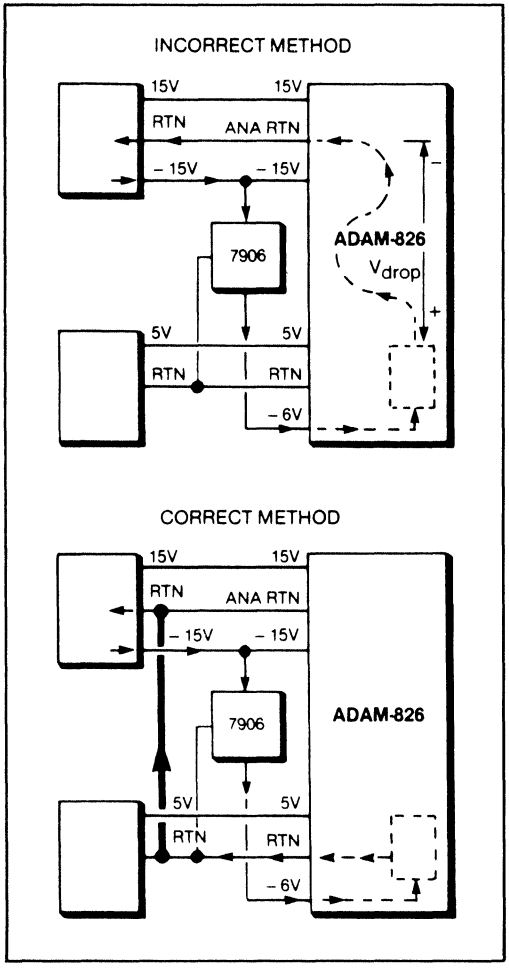


Figure 3. Ground Return Connections.

Grounding

The pc board that the **ADAM-826** is mounted on should make use of a single, massive ground plane for both analog and digital ground. This ground plane should cover as much of at least one side, and preferably both sides of the pc board as possible. If an extensive ground plane can be utilized on both sides of the board, then many feedthroughs should be used to connect the two sides together. You can't use to many feedthroughs (except to endanger the mechanical integrity of the board).

Separate ground return lines back to the +5V and ±15V power supplies is very important, as is a separate analog input return back to the signal source. All of these grounds are connected to the ground plane at the pc board.

If the **ADAM-826** is mounted on a pc board plugged into a card cage, use any free pins to carry ground to the pc board ground plane. Extend the ground plane concept as much as possible in the design.

CALIBRATION SUGGESTIONS

Recalibration of the ADAM-826 for absolute accuracy (gain & offset) is normally required every six months. However, the application will determine how frequently recalibration needs to be performed. Please remember that the very high-speed ADAM-826 performance specifications approach laboratory standard parameters. In applications where temperature fluctuates more than several degrees Celsius and power is cycled on and off frequently, recalibration may be performed more frequently. Where offset and/or gain calibration are performed digitally, hardware calibration may not need to be performed at all. In any case, recalibration of the offset and range potentiometers should be performed as described below in accordance with the system performance needs.

Offset Calibration

Apply the input voltage specified in the Table for the input full scale range in use. Adjust the OFFSET potentiometer so that the LSB of the appropriate output code alternates equally between "0" and "1". The OFFSET pot should be readjusted whenever the selected full scale range is changed.

Range Calibration

Offset should be calibrated before adjusting range. Apply the input voltage specified in the Table for the input full scale range in use. Adjust the RANGE potentiometer such that the LSB of the appropriate output code alternates equally between "0" and "1".

	Input Voltage	
Full Scale Range	**Offset**	**Range**
0V to +10V	+76.3V	+9.99977V
−10V to +10V	+152.6V	+9.99955V

Your Assurance of Quality

The ADAM-826 family represents a major design achievement as reflected in these specifications. In order to guarantee that all of the design capabilities are present in the delivered product, every step of the manufacturing cycle must be meticulously controlled. Critical components are burned-in and screened to exacting standards prior to assembly. In-process inspection and testing is conducted on every unit at several stages of construction, and is followed by a powered-up temperature cycling of the completed unit.

An exhaustive final test of all guaranteed specifications is then conducted on every unit at ambient and at the extremes of the operating temperature range using specially designed automatic test equipment. As an example, Differential Linearity is measured to better than 0.1 LSB **for every single code over the entire transfer curve** under both sequential dynamic and psudo-random dynamic conditions, in each case making over 65,000,000 conversions.

A histogram is printed out showing the distribution of errors as part of the Test Report, a copy of which is shipped with the unit (see Figure 3.) This Test Report, along with your knowledge of the care exercised in its construction, is your assurance that the ADAM-826 delivered to you is the finest converter of its type available.

```
ADAM 826 TEST REPORT
OPERATOR INITIALS:  ____  DATE: ____

TEST CONDITIONS:
Unit type       : unipolar,826-1 sampling A/D
Temperature     : 25 deg. C
Input           : sequential dynamic
Conversion rate: 2.3 microseconds

SERIAL NUMBER-- 84141466

          CODES OUT OF SEQUENCE
CODE(hex)                    OCCURENCES
---------                    ----------
none                         none

     MISSING OR OUT-OF-SPECIFICATION CODES
        (specification=0.75 lsb's max)
     (average conversions per code = 1109)

CODE(hex)                    ERROR(lsb's)
---------                    ------------
none                         none

maximum positive error = 0.454 lsb's
maximum negative error = -0.474 lsb's

          ERROR HISTOGRAM
     (deviation from ideal code width)
RANGE (lsb's)                # OF CODES
-------------                ----------
  -1.0 to -0.9                        0
  -0.9 to -0.8                        0
  -0.8 to -0.7                        0
  -0.7 to -0.6                        0
  -0.6 to -0.5                        0
  -0.5 to -0.4                       35
  -0.4 to -0.3                      272
  -0.3 to -0.2                     1247
  -0.2 to -0.1                     5345
  -0.1 to -0.0                    23260
   0.0 to  0.1                    29636
   0.1 to  0.2                     5035
   0.2 to  0.3                      647
   0.3 to  0.4                       43
   0.4 to  0.5                       12
   0.5 to  0.6                        0
   0.6 to  0.7                        0
   0.7 to  0.8                        0
   0.8 to  0.9                        0
   0.9 to  1.0                        0

Differential linearity tests pass
```

Figure 4. Sample ADAM-826 Final Test Report.

ORDERING GUIDE

Specify..... **ADAM-826-□-□-□**

Basic Configuration

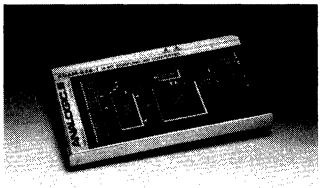
- 2.3 μs Sampling A/D Converter —1
- 2.0 μs Buffered A/D Converter —2
- 1.5 μs A/D Converter alone —3

Input Full Scale Range

- 0V to +10V Unipolar —1
- −10V to +10V Bipolar —2

Connection Option

- Standard Modupac pins for minimum board spacing —0
- Connector —1
  (Check with factory for availability)



ANALOGIC®

ADAM-826-1

16-Bit, 2.3 μs A/D Converter with Integral Sample-and-Hold

Description

Superior performance and relative ease of system implementation make the ADAM-826-1 the ideal solution for those applications requiring a sample-and-hold amplifier (S/H) directly at the input to the A/D Converter. The unit can be ordered with either a ±10V bipolar or 0-10V unipolar input and provides 16-bit two's complement or offset binary output data in 2.3 μs, including acquisition time. The differential linearity error of the ADAM-826-1 is typically less than ±1/4 LSB with a worst case maximum of less than ±3/4 LSB. The internal S/H represents a significant technical achievement in its own right, with an acquisition time of less than 800 ns for full scale input step change — extremely fast for an amplifier whose linearity is better than ±0.001%!

The selection of the ADAM-826-1, with its integral S/H, benefits overall system performance in at least two ways. First, the S/H has been designed specifically to match the requirements of the A/D Converter. For example, great care has been exercised in the internal timing to avoid overlap of critical functions which might impair system performance. Furthermore, S/H performance criteria such as acquisition time, hold mode settling, droop rate, and the like, have been optimized for the A/D Converter, resulting in exceptional combined overall performance as reflected in its specifications. The second benefit to the designer is that by selecting the ADAM-826-1, he can sidestep the sometimes costly iterations of printed circuit board layout often necessary to avoid degradation of 16-bit system performance due to ground loops, signal coupling, and digital noise introduced when separate S/H and A/D Converters are interconnected. To our knowledge at the time of writing, separately or together, there are no better commercially available 16-bit, 500 kHz Sample-and-Holds or Analog-to-Digital Converters, than those contained in the ADAM-826.

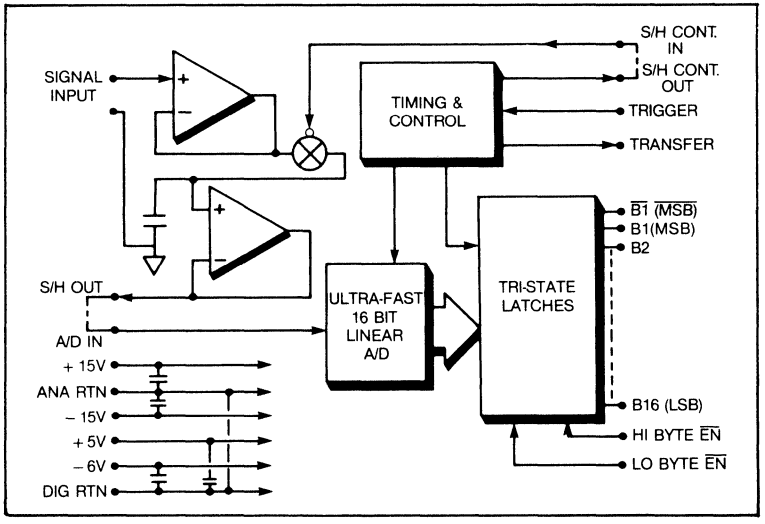


Figure 4. ADAM-826-1 Block Diagram

Using the ADAM-826-1

In most cases, the ADAM-826-1 will be connected as shown in the Block Diagram of Figure 4, in which case, a single trigger/start convert command will cause the S/H to go into the hold mode. Under control of the internal timing logic, the A/D Converter will then begin the conversion while hold mode settling takes place. At the completion of the conversion process, the S/H will automatically be returned to the sample mode to await the next trigger/start convert command. Please refer to the Timing Diagram of Figure 5 and to the section on Timing. It is important to note that the connection to the TRANSFER line must be kept as short as possible, or alternatively, buffered prior to connection to external circuitry.

If external system considerations so dictate, control of the S/H and A/D Converter may be accomplished independently through external logic provided by the user. This is achieved by disconnecting the S/H CONTROL OUT pin from the S/H CONTROL IN pin, as shown in the Block

(continued)

SPECIFICATIONS

(All specifications guaranteed at 25°C and nominal power supply voltages unless otherwise noted)

COMBINED S/H AND A/D CONVERTER PERFORMANCE (ADAM-826-1) (See Note 1.)

Note: These specifications represent the total error of all sources, including both the S/H and A/D Converter errors. As tabulated in subsequent sections, the specifications for the S/H and A/D by themselves are even better.

INPUT

Input Voltage Range
0V to +10V unipolar (See Note 2.) −10V to +10V bipolar

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum (doubles every 10°C)

Initial Offset Voltage
±5 mV maximum, adjustable to zero

THROUGHPUT

Conversion Time
2.3 μs, maximum

Maximum Conversion Rate
435,000 samples per second

ACCURACY

Resolution
16 bits

Differential Non-Linearity
±1/4 LSB typical, ±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR typical (See Note 3.) ±0.003% FSR maximum (See Note 3.)

Absolute Accuracy (Includes Reference Accuracy)
±0.005% FSR maximum (See Note 4.) The Internal Reference (and offset) may be adjusted against a standard source traceable to the National Bureau of Standards for even better Absolute Accuracy

Noise
Unipolar: 60 μV rms maximum, Bipolar: 80 μV rms maximum

STABILITY

Differential Non-Linearity Tempco
±1 ppm FSR/°C maximum

Total Offset Tempco (including Pedestal)
±5 ppm FSR/°C maximum

Gain Tempco
±5 ppm FSR/°C maximum

Warmup Time
10 minutes to specified accuracy (See Note 5.)

Power Supply Sensitivity Gain
±10 ppm/Δ1% each supply, maximum

Offset
±10 ppm/Δ1% each supply, maximum

Recommended Recalibration Interval
6 months

DIGITAL INPUTS/OUTPUTS INPUTS

Trigger
Negative edge triggered; 1 LSTTL load; 50 ns pulse width minimum, 200 ns maximum; (See Note 9.) CMOS and 74LSTTL Compatible

S/H Mode Control
Logic 1 is HOLD mode, logic 0 is SAMPLE, Logic 1 must be +5V, drive with CMOS gate or TTL gate with <470Ω pullup

Tri-state Control
HI Byte Enable
Logic 1 produces high impedance

LO Byte Enable
Logic 1 produces high impedance, CMOS and 74LSTTL Compatible

OUTPUTS

Data
16 bits data plus $\overline{B1}$; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

Data Output Loading Transfer (XFER)
1 LSTTL load, positive edge loads output data latches; data ready after 50 ns delay

Transfer (XFER) Loading
1 LSTTL Load

POWER REQUIREMENTS

+15V ±0.5V
85 mA, typical

−15V ±0.5V
95 mA, typical

+5V ±0.25V
65 mA, typical

−6V ±0.25V
150 mA, typical (See Note 8.)

Note: At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

Note: The ±15V power supplies must have no more than 5 mV p-p ripple.

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +70°C

Relative Humidity
0 to 85%, non condensing

Dimensions and Shielding
Modupac
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

Socket Mount Option
3.45" x 5.00" x 0.55" (87.63 x 127.00 x 13.97 mm)
RFI 6 sides, EMI 6 sides

SAMPLE-AND-HOLD AMPLIFIER ONLY

INPUT

Input Voltage Range
± 10V, (See Note 2.)

Maximum Input Without Damage
± Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
± 100 pA maximum (doubles every 10°C)

Initial Offset Voltage
± 5 mV maximum, adjustable to zero

SAMPLE MODE

Gain
+ 1

Small Signal Bandwidth
5 MHz typical

Full Power Bandwidth
250 kHz

Acquisition Time
800 ns maximum to 0.0015% for 20V full scale step. Acquisition time for smaller steps will be less.

Non-Linearity
± 0.001% (20V input)

Noise
40μV rms typ., 50V rms max. Unipolar or Bipolar

SAMPLE-TO-HOLD SWITCHING

Aperture Uncertainty
150 ps typical

Aperture Time
15 ns typical

Switching Transient Settling Time
150 ns maximum (See Note 6.) to ± 0.0015% FSR

HOLD MODE

Output Drive Capability
1 kΩ // 50 pF Short-circuit protected

Droop Rate
5 μV/μs maximum (See Note 7.)

Dielectric Absorption
± 0.001% of voltage change, typical (800 ns Sample, 1.5 μs Hold)

Pedestal Non-Linearity
± 0.0015% FSR maximum

A/D CONVERTER ONLY

Input Voltage
0V to + 10V unipolar; − 10V to + 10V bipolar, Factory configured

Input Impedance
1.4 kΩ unipolar, 2.8 kΩ bipolar

ACCURACY

Resolution
16 bits

Differential Non-Linearity
± 1/4 LSB typical, ± 3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
± 1/2 LSB

Relative Accuracy
± 0.0015% FSR maximum

Absolute Accuracy
± 0.003% FSR maximum

Noise (Including Ref.)
Unipolar: 30 μV rms, maximum, Bipolar: 60 μV rms, maximum

STABILITY

Differential Non-Linearity
± 1 ppm/°C maximum

Tempco
± 5 ppm/°C maximum

Gain Tempco
Unipolar: ± 1.5 ppm/°C maximum,
Bipolar: ± 4.5 ppm/°C maximum

Warmup Time
10 minutes to specified accuracy

Recommended Recalibration Interval
6 months

THROUGHPUT

Conversion Time
1.5 μs maximum

Note 1: Specifications apply when S/H control is internally generated. See text and Figure 4.
Note 2: Input voltage range is determined by the A/D Converter. The S/H is a unity gain device.
Note 3: Specified as the maximum deviation from a best fit line. Maximum deviation from straight line drawn through full scale end points is 0.004%.
Note 4: Absolute Accuracy is the worst case summation of all error sources for both the Analog-to-Digital Converter and the Sample-and-Hold Amplifier.
Note 5: Time required for internal reference heater to stabilize.
Note 6: Specified for completeness only — this settling time is overlapped by the A/D conversion time and does not affect throughput.
Note 7: Specified for completeness only — droop rate does not affect the accuracy of the 1.5 μs conversion process.
Note 8: − 6V may be readily derived from the − 15V power supply using a 7906-type three-terminal regulator. See Figure 1.
Note 9: The 50 ns pulse width is recommended where possible.

Using the ADAM-826-1 (cont.)

Diagram of Figure 4, and supplying an external S/H mode control signal to the S/H CONTROL IN pin. This signal should be provided by a HCMOS driver so that the logic "1" (HOLD mode) is a solid +5V.

In some system architectures, it may be desirable to introduce a signal, such as a digitally controlled overall system offset correction, between the S/H output and the A/D Converter input. A provision for this is made in the ADAM-826-1 allowing the user to add appropriate circuitry between the S/H OUT and A/D IN pins. If this offset correction signal is changed when the ADAM-826-1 is in the sample mode, then the timing as shown in Figure 4 will not be affected, provided the D/A converter supplying the correction voltage is completely settled prior to the next trigger/start convert command. The connection to the S/H OUT-A/D IN pins from the D/A must be as short as possible; refer to the sections on pc board layout, and the text on the ADAM-826-3.

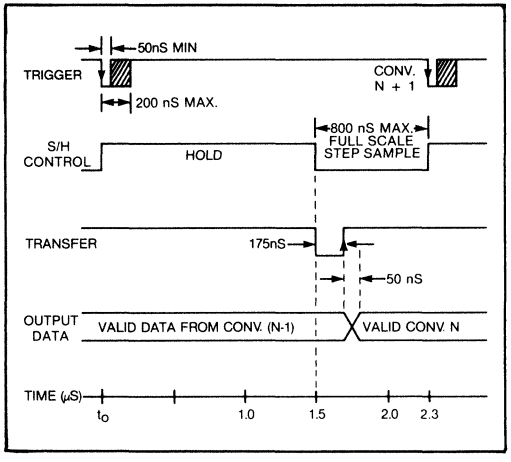


Figure 5. Typical Timing - ADAM-826-1

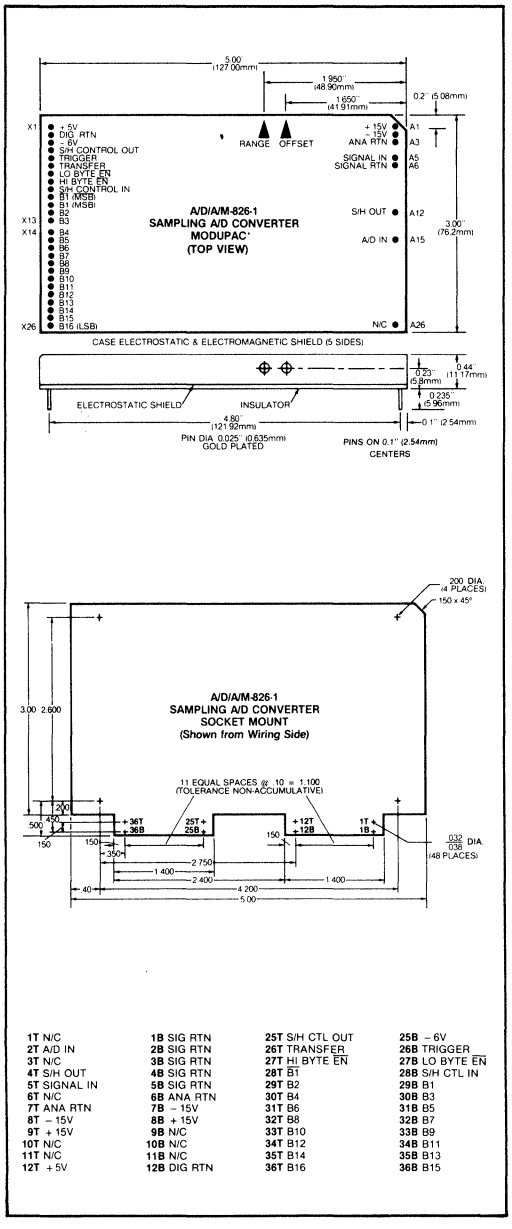
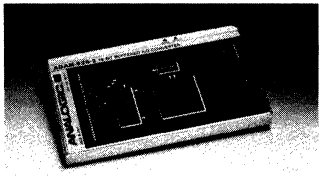


Figure 6. ADAM-826-1 Mechanical & Pinout



ANALOGIC®

ADAM-826-2

16-Bit, 2.0 μs A/D Converter with Input Buffer Amplifier

Description

In systems that simultaneously sample multiple channels prior to multiplexing the analog signal, a sample-and-hold (S/H) directly at the input to the A/D Converter is not required. In other multi-channel systems, the analog inputs will be essentially low frequency and stable during conversion. In either case, the high conversion rate of the ADAM-826-2 may be desirable in order to minimize the time required to input the data and clear the input channel to the computer. The unit includes a high input impedance (100 MΩ) buffer with settling time of less than 400 ns resulting in an overall conversion time of 2.0 μs. Input full scale ranges of ±10V bipolar or 0V to +10V unipolar can be accommodated. To make the ADAM-826-2 even more flexible, the output of the buffer amplifier and the input to the A/D Converter are brought out to separate pins. Normally, these two pins would be connected together as shown in the Block Diagram in Figure 7; however, this connection may be broken, or signals may be injected at this point. This should be done only when absolutely required by external system considerations as the output of the buffer amplifier is not short-circuit protected. Refer also to the sections on the ADAM-826-3 and PC BOARD LAYOUT.

In order to determine whether an error will occur due to the changing signal without using a S/H, the system designer need only consider the first 1.5 μs of the conversion process. Any change in input signal thereafter will not affect the result as this remaining time is used to complete the conversion and to transfer the resulting data word to the internal output data register. This timing relationship is depicted in the Typical Timing Diagram of Figure 8.

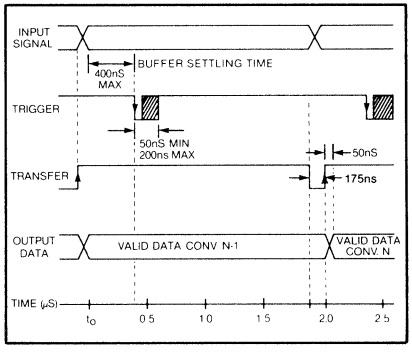


Figure 8. Typical Timing — ADAM-826-2.

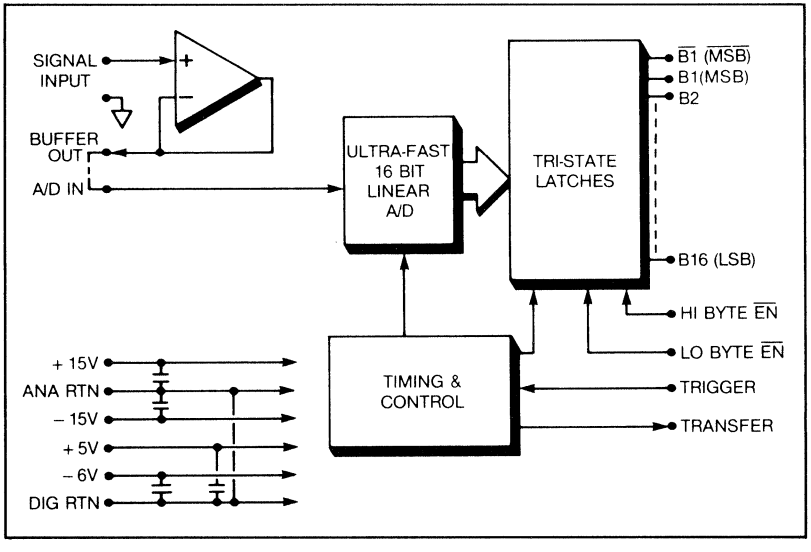


Figure 7. Block Diagram — ADAM-826-2.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

COMBINED BUFFER AMPLIFIER AND A/D PERFORMANCE

Note: These specifications represent the total error of all sources including both the Buffer Amplifier and A/D converter errors. As tabulated in subsequent sections, the specifications for the Buffer Amplifier and A/D by themselves are even better.

INPUT

Input Voltage Range
0V to +10V Unipolar
(See Note 1.)
±10V Bipolar
Factory configured

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum

THROUGHPUT

Conversion Time
2.0 μs maximum

Conversion Rate
500,000 samples per second

ACCURACY

Resolution
16-bits

Differential Non-linearity
±1/4 LSB typical,
±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR typical (See Note 2.)
±0.0025% FSR maximum (See Note 2.)

Absolute Accuracy (Includes Reference Accuracy)
±0.004% FSR maximum. The Internal Reference (and offset) may be adjusted against a standard source traceable to the National Bureau of Standards for even better Absolute Accuracy

Noise
Unipolar: 45 μV rms maximum
Bipolar: 70 μV rms maximum

STABILITY

Differential Non-linearity Tempco
±1 ppm/°C FSR maximum

Offset Tempco
Unipolar: ±3 ppm/°C maximum
Bipolar: ±5 ppm/°C maximum

Gain Tempco
±5 ppm FSR/°C maximum

Power Supply Sensitivity Gain
±10 ppm/Δ1% each supply, maximum

Offset
±10 ppm/Δ1% each supply, maximum

Warmup Time to Specified Accuracy
10 minutes (See Note 3.)

Recommended Recalibration Interval
6 months

DIGITAL INPUTS/OUTPUTS

INPUTS

Trigger
Negative edge triggered; 1 LSTTL load; 50 ns pulse width minimum, 200 ns maximum; CMOS and 74 LSTTL Compatible (See Note 5.)

Tri-state Control
HI Byte Enable
Logic 1 produces high impedance

LO Byte Enable
Logic 1 produces high impedance CMOS and 74 LSTTL Compatible

OUTPUTS

Data
16 bits data plus B1; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

Data Output Loading
1 LSTTL load

Transfer (XFER)
Positive edge loads output data latches; data ready after 50 ns delay

Transfer (XFER) Loading
1 LSTTL Load

POWER REQUIREMENTS

+15V ±0.5V
55 mA, typical

−15V ±0.5V
80 mA, typical

+5V ±0.25V
65 mA, typical

−6V ±0.25V
150 mA, typical (See Note 4.)

Note:
At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

Note:
The ±15V power supplies must have no more than 5 mV p-p ripple.

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +70°C

Relative Humidity
0 to 85%, non condensing

Dimensions and Shielding Modupac®
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

Socket Mount Option
3.45" x 5.00" x 0.55"
(87.63 x 127.00 x 13.97 mm)
RFI 6 sides, EMI 6 sides

INPUT BUFFER AMPLIFIER ONLY

INPUT

Input Voltage Range
0V to +10V Unipolar
±10V Bipolar
Factory configured

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum

AC PERFORMANCE

Small Signal Bandwidth
5 MHz typical

Full Power Bandwidth
250 kHz

Non-linearity
±0.001% FSR maximum

Buffer Settling Time
400 ns to ±0.0015% of Full Scale step

Noise
25 μV rms typical,
35 μV rms maximum

Output Drive Capability
1 kΩ // 50 pF; This output is NOT short circuit protected

A/D CONVERTER ONLY

ANALOG INPUT

Input Voltage
0V to +10V unipolar
−10V to +10V bipolar
Factory configured

Input Impedance
1.4 kΩ unipolar
2.8 kΩ bipolar

ACCURACY

Resolution
16 bits

Differential Non-linearity
±1/4 LSB typical,
±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR maximum

Absolute Accuracy
±0.003% FSR maximum

Noise (Including Ref.)
Unipolar: 30 μV rms, maximum
Bipolar: 60 μV rms, maximum

STABILITY

Differential Non-Linearity Tempco
±1 ppm/°C maximum

Offset Tempco
Unipolar: ±1.5 ppm/°C max.
Bipolar: ±4.5 ppm/°C max.

Gain Tempco
±5 ppm/°C maximum

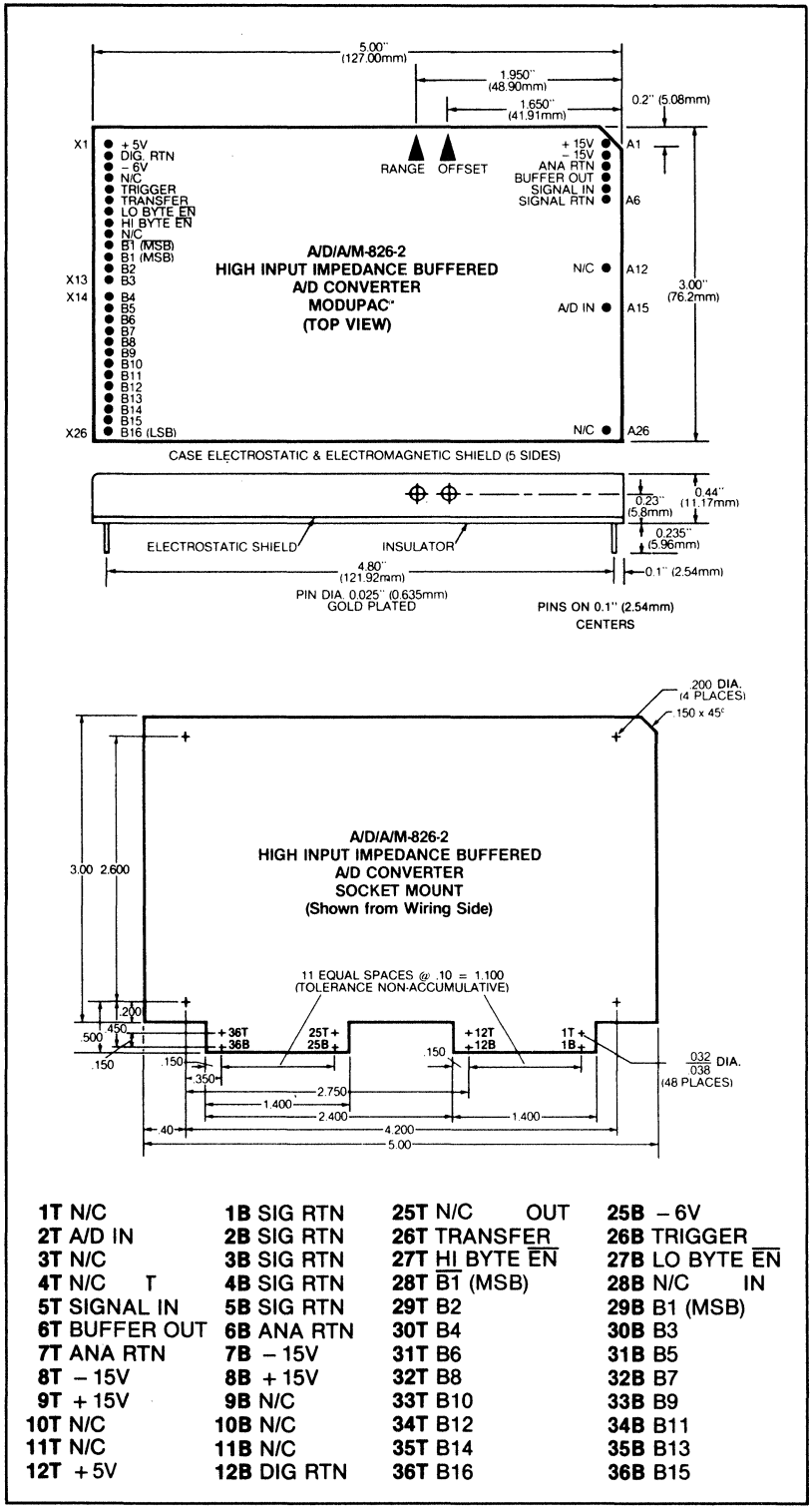
Warmup Time
10 minutes to specified accuracy

Recommended Recalibration Interval
6 months

THROUGHPUT

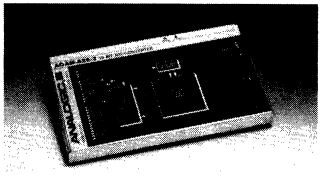
Conversion Time
1.5 μs maximum

Note 1: Input Voltage range is determined by the A/D Converter. The Buffer Amplifier is a unity gain device.
Note 2: Specified as the maximum deviation from a best fit line. Maximum deviation from a straight line drawn through the full scale end points is ±0.0035%.
Note 3: Time required for internal reference heater to stabilize.
Note 4: −6V may be readily derived from the −15V power supply using a 7906-type three-terminal regulator. See Figure 5.
Note 5: The 50 ns pulse width is recommended where possible.



1T N/C	**1B** SIG RTN	**25T** N/C OUT	**25B** – 6V
2T A/D IN	**2B** SIG RTN	**26T** TRANSFER	**26B** TRIGGER
3T N/C	**3B** SIG RTN	**27T** HI BYTE EN	**27B** LO BYTE EN
4T N/C T	**4B** SIG RTN	**28T** B1 (MSB)	**28B** N/C IN
5T SIGNAL IN	**5B** SIG RTN	**29T** B2	**29B** B1 (MSB)
6T BUFFER OUT	**6B** ANA RTN	**30T** B4	**30B** B3
7T ANA RTN	**7B** – 15V	**31T** B6	**31B** B5
8T – 15V	**8B** + 15V	**32T** B8	**32B** B7
9T + 15V	**9B** N/C	**33T** B10	**33B** B9
10T N/C	**10B** N/C	**34T** B12	**34B** B11
11T N/C	**11B** N/C	**35T** B14	**35B** B13
12T + 5V	**12B** DIG RTN	**36T** B16	**36B** B15

Figure 9. ADAM-826-2 Mechanical & Pinout.



ANALOGIC®

ADAM-826-3

16-Bit, 1.5 μs Unbuffered A/D Converter

Description

The 1.5 μs A/D Converter itself is available for those applications where the signal has already been conditioned and only the A/D conversion function is required. In this configuration, as depicted in the Block Diagram of Figure 10, the duplication of circuitry and errors associated with an internal buffer amplifier or S/H are eliminated.

To preserve the full performance capability inherent in the A/D, whether configured for ± 10V bipolar or 0V to + 10V unipolar signals, care must be exercised in its implementation in the system. The input impedance of the unbuffered A/D is 1.4 kΩ unipolar or 2.8 kΩ bipolar. The pc etch that connects the A/D input to the signal source(s) must be carefully routed to avoid other etches carrying digital signals to prevent coupling of digital noise into the analog input. In addition, the physical dimensions (length and width) of this etch must be controlled to reduce the effects of temperature on the overall gain specification of the ADAM-826-3. For example, for 2 ounce copper-clad pc board, and a etch width of 0.025", the etch will have a dc resistance of 0.010Ω per inch. If we assume a six inch etch length, the total dc resistance of this etch is 0.060Ω. This etch, which forms a resistive divider with the A/D Converter input impedance, has a temperature coefficient of 0.39%/°C. For a temperature rise of 35°C from 25°C to 60°C, the etch resistance will change by a sufficient amount to cause the gain to change by 0.4 LSB at the 16-bit level. This example illustrates the effects on conversion accuracy of typical pc etch dimensions found in many data acquisition systems. Wherever possible pc etch lengths should be kept as short as absolutely necessary to reduce these errors.

The maximum frequency of the signal at the input to the ADAM-826-3 can be determined by the timing relationships as shown in the Typical Timing Diagram of Figure 11. As shown, the actual conversion requires only 1.5 μs while the last 225 ns is used to complete the internal conversion process and to transfer the resulting data word into the internal data register. As long as the signal does not change during the first 1.5 μs of the conversion cycle, no errors will be introduced from this source.

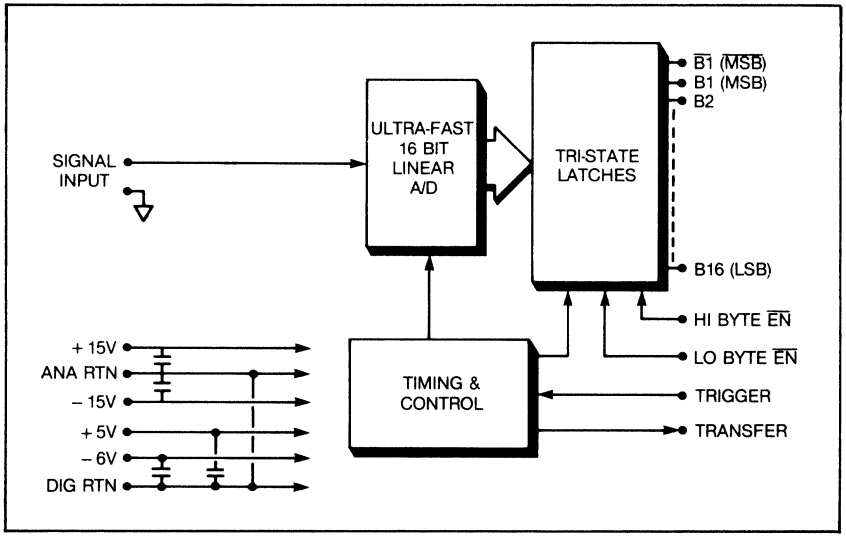


Figure 10. Block Diagram — ADAM-826-3.

SPECIFICATIONS

(All Specifications are guaranteed at 25°C and nominal power supply voltages unless otherwise noted)

ANALOG INPUT

Input Voltage
0V to +10V Unipolar
−10V to +10V Bipolar
Factory configured

Input Impedance
1.4 kΩ Unipolar
2.8 kΩ Bipolar

ACCURACY

Resolution
16-bits

Differential Non-linearity
±1/4 LSB typical,
±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR maximum

Absolute Accuracy
±0.003% FSR maximum

Noise (Including Ref.)
Unipolar: 30 μV rms, maximum
Bipolar: 60 μV rms, maximum

STABILITY

Differential Non-linearity Tempco
±1 ppm/°C maximum

Offset Tempco
Unipolar: ±1.5 ppm/°C maximum
Bipolar: ±4.5 ppm/°C maximum

Gain Tempco
±5 ppm FSR/°C maximum

Power Supply Sensitivity Gain
±10 ppm/Δ1% each supply, maximum

Offset
±10 ppm/Δ1% each supply, maximum

Warmup Time
10 minutes to specified accuracy

Recommended Recalibration Interval
6 months

THROUGHPUT

Conversion Time
1.5 μs maximum

DIGITAL INPUTS/OUTPUTS

INPUTS

Please refer to ADAM-826-2

Trigger
Negative edge triggered; 1 LSTTL load; 50 ns pulse width minimum, 200 ns maximum; CMOS and 74 LSTTL Compatible

Tri-state Control
HI Byte Enable
Logic 1 produces high impedance

LO Byte Enable
Logic 1 produces high impedance CMOS and 74LSTTL Compatible

OUTPUTS

Data
16 bits data plus $\overline{B1}$; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

Data Output Loading
1 LSTTL load

Transfer (XFER)
Positive edge loads output data latches; data ready after 50 ns delay

Transfer (XFER) Loading
1 LSTTL Load

POWER REQUIREMENTS

+15V ±0.5V
40 mA, typical

−15V ±0.5V
65 mA, typical

+5V ±0.25V
65 mA, typical

−6V ±0.25V
150 mA, typical (See Note 2.)

Note:
At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

Note:
The ±15V power supplies must have no more than 5 mV p-p ripple.

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +60°C

Relative Humidity
0 to 85%, non condensing

Dimensions and Shielding Modupac®
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

Socket Mount Option
3.45" x 5.00" x 0.55"
(57.63 x 127.0 x 13.97 mm)
RFI 6 sides, EMI 6 sides

Note 1: Time for internal reference heater to stabilize.

Note 2: – 6V may be readily derived from the – 15V power supply using a 7906-type three-terminal regulator. See Figure 1.

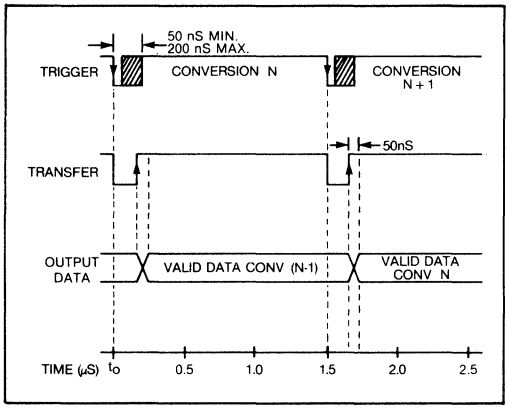


Figure 11. Typical Timing — ADAM-826-3.

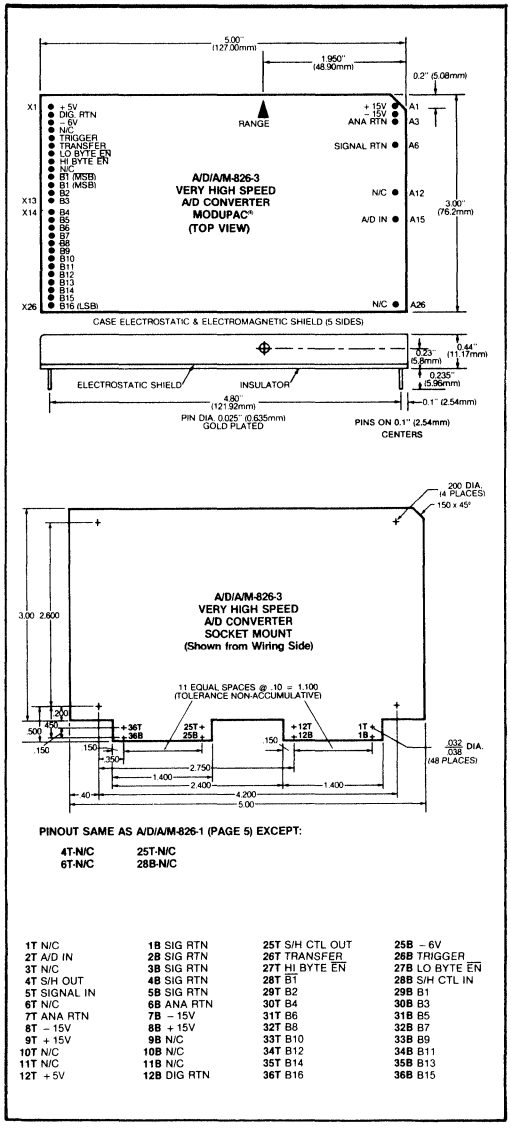
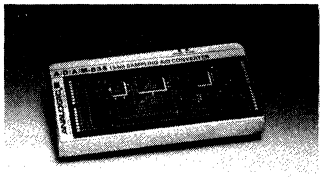


Figure 12. ADAM-826-3 Mechanical & Pinout.



ANALOGIC®

A/D/A/M-834A/835A

14- and 15-Bit Extended Temperature Range Sampling A/D Converters

Description

Analogic's ADAM-834A and 835A are 14- and 15-bit analog-to-digital converters (ADCs) with integral sample-and-hold amplifiers (S/H) that offer significantly improved stability and reduced power dissipation over previous converters of similar architecture. Their low noise, low power dissipation, and guaranteed end-to-end S/H plus A/D performance over a wide temperature range make them ideal for applications requiring high precision in severe environments, such as seismic exploration and field testing. Both combine a precision S/H circuit and a high accuracy A/D converter with tri-state output buffers in a single module, eliminating the interface problems that often accompany the integration of individual modules. (See Figure 1).

The ADAM-834A and 835A feature exceptional accuracy and stability over temperature, including a maximum Differential Nonlinearity Tempco of ±1 ppm/°C, clock stability of ±0.03%/°C maximum, and rapid stabilization at power up. Offering guaranteed performance over the temperature range of −25°C to +85°C, the ADAM-834A and 835A satisfy the most stringent industrial and geophysical data acquisition requirements. Low power dissipation (0.9W), very low noise (75 μV rms), and wide dynamic range (15 bits) allow the user to perform sophisticated measurements with a much higher level of confidence in the results than would otherwise be possible in these severe environments.

The ADAM-834A and 835A are fully shielded in 2" x 4" x 0.37" metal packages. Each is fully tested and supplied with its documented test data.

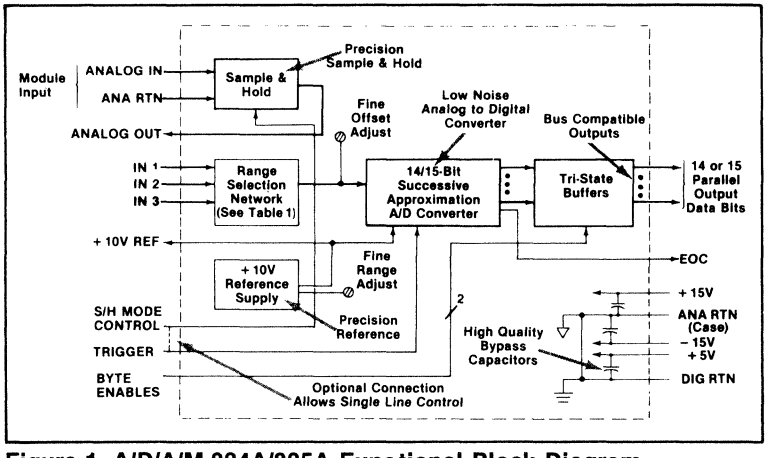


Figure 1. A/D/A/M-834A/835A Functional Block Diagram.

Features

- **Guaranteed performance over extended temperature range** (−25°C to +85°C)
- **Low Noise** 50 μV (ADC)
- **Low differential nonlinearity** ±0.0015% FSR maximum (835A)
- **Low Drift** ±1 pm/°C differential nonlinearity tempco (835A)
- **Low Power** 0.9W
- **Byte-selectable CMOS tri-state buffered outputs**
- **High Throughput Rate** 16.6 kHz
- **Pin-programmable input voltage range** 0V to +5V, 0V to +10V, ±5V, ±10V

Applications

For severe temperature environments including:

- **Seismic Data Acquisition**
- **Portable Field-Test Equipment**
- **Automatic Test Equipment**
- **Materials Testing**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)
(includes combined S/H and A/D performance, and applies to both ADAM -834A and ADAM-835A except where noted)

ANALOG INPUTS

Full Scale Range (FSR)
0V to +5V, 0V to +10V, ±5V, ±10V (see Table 1)

Maximum Input Without Damage
±15V

Impedance
100 MΩ//5 pF

Bias Current
1 nA maximum

ACCURACY

Absolute Accuracy (Traceable to NBS)
Calibrated to ±0.006% FSR

Relative Accuracy
±0.005% FSR maximum (ADAM-834A)
±0.003% FSR maximum (ADAM-835A)

Differential Nonlinearity
±0.003% FSR maximum (ADAM-834A)
±0.0015% FSR maximum (ADAM-835A)

Quantizing Error
± ½ LSB

Noise (S/H plus A/D)
75 μV rms, ±10V range

Noise (A/D only)
50 μV rms, ±10V range

Monotonicity
Guaranteed

STABILITY

Tempco of Differential Nonlinearity
±3 ppm/°C FSR maximum (ADAM-834A)
±1 ppm/°C FSR maximum (ADAM-835A)

Gain Tempco
±8 ppm/°C FSR maximum

Offset Tempco
±30 μV/°C typical, ±40 μV/°C maximum

Clock Stability
±0.03%/°C maximum

Power Supply Sensitivity
±0.001% per 1% change in supply voltage

Warm-up Time to Specified Accuracy
1 minute

Recommended Recalibration Interval
6 months

DYNAMIC PERFORMANCE

Maximum Throughput Rate
16,600 measurements/second

S/H Aperture Delay
50 ns

S/H Aperture Uncertainty
1 ns

S/H Hold Mode Feedthrough Rejection
90 dB minimum, measured with 20V p-p, 10 kHz sine wave input

S/H Droop Rate
0.2 μV/μs at 25°C, doubles every 10°C

S/H Dielectric Absorption Error
±0.005% of input voltage change at maximum throughput rate. Error decreases as sampling time is decreased

DIGITAL OUTPUTS

General
Tri-state CMOS

End of Conversion (EOC)
Positive true, 2 unit loads/line, (see Figure 3 for timing) CMOS

Parallel Data Codes
Positive true, tri-state buffered CMOS; unipolar binary, offset binary, or two's complement (see Table 1)

DIGITAL INPUTS

General
Standard TTL, one unit load/line

S/H Mode Control
Sample = Logic 1 (10 μs minimum)
Hold = Logic 0 (minimum = conversion time)
Logic 1 to logic 0 transition time 10 ns maximum

A/D Trigger
Negative-going edge; logic 1 to logic 0 transition 50 ns maximum

Low/High Byte Enable
Logic 0 = enable
Logic 1 = 3.5V minimum @ 1 μA, CMOS
Logic 0 – 1.5V maximum @ 1 μA, CMOS

POWER REQUIREMENTS

+15V, ±3%
37 mA maximum

–15V, ±3%
29 mA maximum

+5V, ±5%
9 mA maximum

Power Dissipation
0.9W

ENVIRONMENTAL & MECHANICAL

Operating Temperature
–25°C to +85°C

Storage Temperature
–25°C to +85°C

Relative Humidity
5% to 95% non-condensing to 40°C

Shielding
Electrostatic (RFI) 6 sides; Electromagnetic (EMI) 5 sides

Package Size
2.00 x 4.0 x 0.375" (50.8 x 101.6 x 9.53 mm)

Operation

The ADAM-834A and 835A interface directly to most commonly available input devices (multiplexers, amplifiers, etc.). The high input impedance of the fast, fully-buffered unity gain S/H amplifier minimizes source loading errors; the hold mode feedthrough rejection and droop rate allow optimum performance in multichannel systems.

The parallel binary data information is CMOS tri-state buffered allowing access as either two 8-bit bytes or as a single 16-bit (including $\overline{B1}$) data word. (If the tri-state feature is not needed, normal binary outputs can be obtained by connecting the byte enable pins to ground.) For two's complement operation, use $\overline{B1}$ instead of B1 (the MSB).

For operation with a single external control pulse, the S/H mode control input may be connected to the A/D trigger. Figure 3 shows the timing requirements for the digital control signals.

Input voltage range is established by connecting the S/H output to the appropriate A/D input pins (see Table 1). These pins provide access to the S/H output for arbitrary signal processing prior to analog-to-digital conversion. In addition, the S/H may be bypassed for applications requiring direct input to the A/D converter.

RANGE PROGRAMMING AND OUTPUT CODING

A/D Input Connections

Full Scale Range	Connect IN 1 to	Connect IN 2 to	Connect IN 3 to	Input Impedance
0 to +5V	S/H ANA OUT	S/H ANA OUT	S/H ANA OUT	1.25kΩ
0 to +10V	ANA RTN	S/H ANA OUT	S/H ANA OUT	2.5kΩ
−5V to +5V	S/H ANA OUT	+10V REF	ANA RTN	2.5kΩ
−10V to +10V	ANA RTN	+10V REF	S/H ANA OUT	5.0kΩ

Output Codes

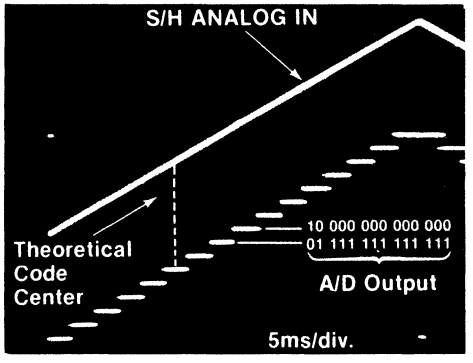
A/D/A/M-834 (14 Bits)		A/D/A/M-835 (15 Bits)	
Unipolar Binary			
11 111 111 111 111	= +9.99939V*	111 111 111 111 111	= +9.99969V*
00 000 000 000 000	= 0.00000V	000 000 000 000 000	= 0.00000V
Offset Binary			
11 111 111 111 111	= +9.99878V†	111 111 111 111 111	= +9.99939V†
10 000 000 000 000	= 0.00000V	100 000 000 000 000	= 0.00000V
00 000 000 000 000	= −10.00000V	000 000 000 000 000	= −10.00000V
Two's Complement			
01 111 111 111 111	= +9.99878V†	011 111 111 111 111	= +9.99939V†
00 000 000 000 000	= 0.00000V	000 000 000 000 000	= 0.00000V
10 000 000 000 000	= −10.00000V	100 000 000 000 000	= −10.00000V

*For +5 volts FSR, divide voltage by two
†For ±5 volts FSR, divide voltage by two

Table 1

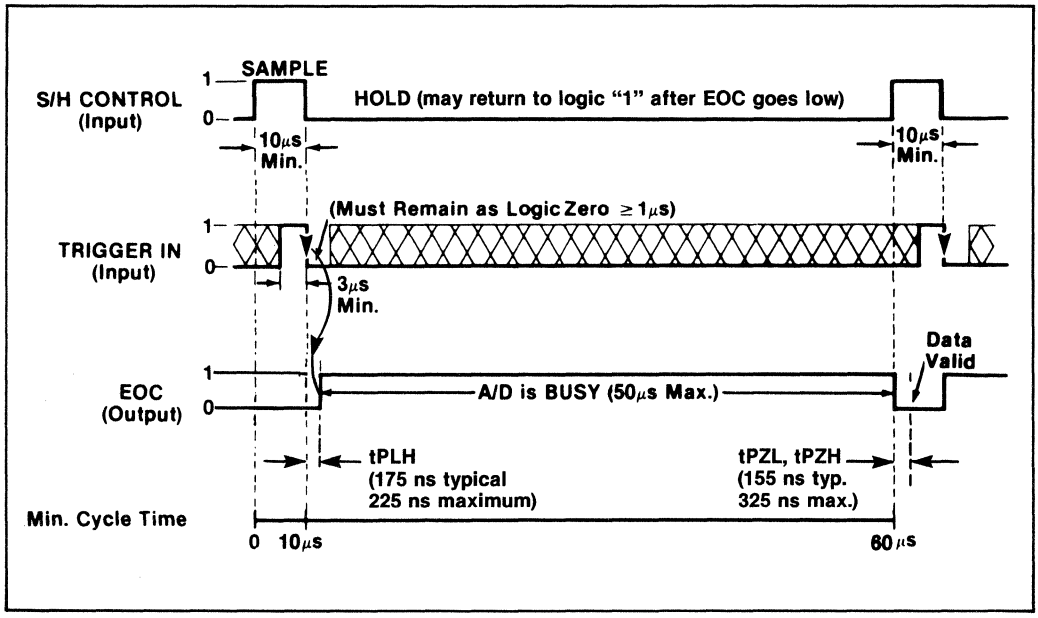
Applications

Designed to operate within the −25°C to +85°C temperature range with high accuracy and low drift, the ADAM-834A and 835A can serve a variety of applications, including field testing, such as portable multichannel seismic data acquisition systems to provide rapid, highly-linear, and stable A/D conversion. In these systems, geophones receive artificially induced shock wave reflected off the different subsurface strata at various angles and velocities. The weakest signals may travel up to 5 miles through the lithosphere, and are difficult to distinguish from the noise and interference caused by ground roll. After appropriate front-end preamplification and filtering, the analog signals are converted to digital form and stored for processing. The ADAM-834A and 835A provide the low noise and required throughput to digitize data from 16 channels, while maintaining a 1 kHZ-per-Channel sampling rate.



The upper race shows an input that ramps repetitively from −4.88 mV to +4.88 mV and back very slowly in relation to the module's 16.6 kHz sampling rate. The module output is used to drive a digital-to-analog converter, whose output is then shown on the lower trace. Thus each level on the staircase corresponds to a set of conversions made around a code center voltage, and the transitions show when the module toggles its LSB. This type of plot may be used to measure differential nonlinearity (the most significant A/D performancce parameter for most applications) and to determine by inspection the existence of errors such as wide code, narrow code, missing code, non-monotonicity, etc. Because the input is dynamically changing, this type of test simulates actual operation very well.

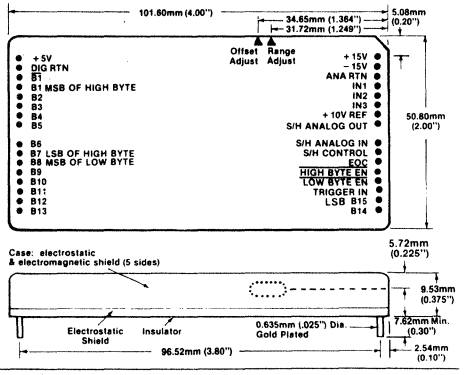
Figure 2. A/D/A/M-835A Crossplot Shows Highly Linear Performance.



Output data registers are National Semiconductor MM74C373,
tPZL, tPZH from falling edge of byte en to B outputs: 105 ns typical, 225 ns Maximum
tPLZ, tPHZ from rising edge of byte en to B outputs: 105 ns typical, 225 ns Maximum

Figure 3. ADAM-834A/835A Timing.

MOUNTING DIMENSIONS & PINOUTS



Notes

- Pin spacing on 2.54mm (0.10") centers. Double spacing between pins 8 & 9, as shown.
- A/D/A/M-834 and -835 identical except B15 not used on A/D/A/M-834
- Modupac™ may be mounted in any orientation.

CALIBRATION

Due to excellent long-term stability, these modules will rarely require re-calibration. They should, however, be re-adjusted when the selected FSR is changed. Offset should be zeroed prior to trimming the range.

Offset Zeroing Procedure

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Offset pot until the module output code corresponds to 0V, with the LSB alternating equally between 0 and 1.

Range Trimming Procedure (Gain Adjust)

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Gain pot until the module output code is all 1's, with the LSB alternating equally between 0 and 1.

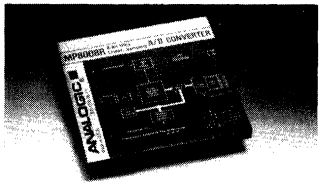
Input Voltages For Calibration

	ADAM-834A.		ADAM-835A.	
Nominal FSR	Offset	Range	Offset	Range
0 to +5V	153μV	+4.99954V	76μV	+4.99977V
0 to +10V	305μV	+9.99909V	153μV	+9.99954V
-5 to +5V	305μV	+4.99909V	153μV	+4.99954V
-10 to +10V	610μV	+9.99817V	305μV	+9.99909V

ORDERING GUIDE

Specify

ADAM-834A. 14-bit Resolution
ADAM-835A. 15-bit Resolution



ANALOGIC®

MP8008R

8-Bit, 3.0 μs Ultra-High, Differential-Linearity, Sampling A/D Converter

Description

The MP8008R, a high speed, 8-bit, sampling analog-to-digital converter (a form of randomizing converter) is designed especially for imaging applications that are based on statistical principles, such as nuclear pulse height analysis. In critical applications, such as nuclear medical diagnostic imaging, where it is imperative to reduce artifacts in the displayed data, high differential-linearity must be attained. The MP8008R provides a basic single-measurement ultra-high differential-linearity of 0.02% and provides an even superior differential-linearity of approximately 0.004% when the dithered offset or randomizing mode of operation is utilized for multiple measurements. This is equivalent to the statistical performance consistent with the near perfect measurement of approximately 10^{11} samples of nuclear events of a random amplitude distribution.

The unit employs a unique architecture consisting of a sample-and-hold, an A/D converter, two D/A converters, a random number generator, and associated control and output logic. However, unlike previously available averaging-type A/D converters, which typically

(continued)

Features

- **Ultra-High Differential Linearity**
  Enhanced differential linearity for large samples (1% of one LSB differential linearity consistent with nuclear even sample quantitites of 10^4/channel code)
- **Low Cost**
- **Very High Speed**
  3.0 μs Overall Sampling and Conversion Time
- **8-Bit Precision Resolution**
- **Averaging Scheme Reduces Artifacts**
- **Low Power**
  3.3W, typical
- **Versatile Input/Output Interfacing**
  TTL Commpatible
  Latched, Tri-State Outputs
- **Excellent Stability Over Time and Temperature**
  (0°C to 60°C)

Applications

- **Nuclear Medical Diagnostic Imaging**
- **Nuclear Pulse Height Analysis**
- **General Scientific Research**

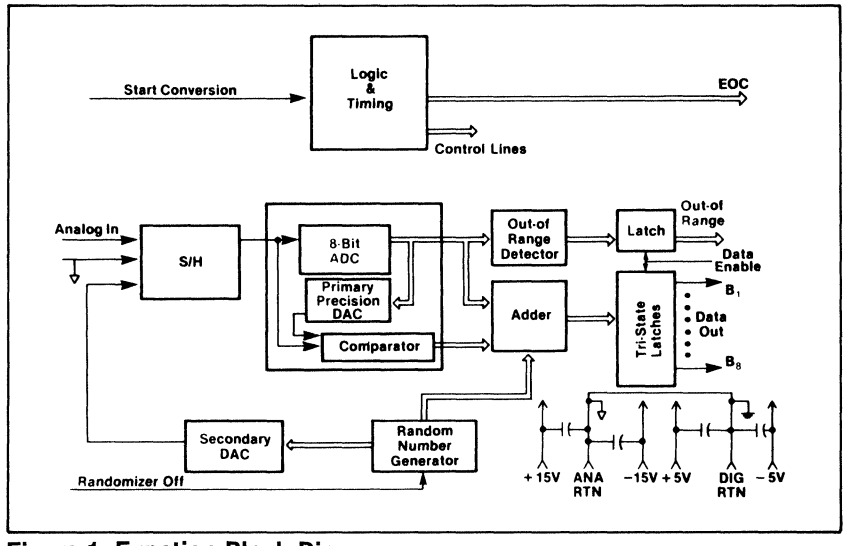


Figure 1. Function Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Full Scale Range (FSR)
±5V

Impedance
1.7 kΩ||10 pF

ACCURACY

Resolution
8-bits binary

Differential Non-Linearity
Randomizer on[1]
1% of an LSB, max.

Randomizer off[2]
0.003% FSR typ., 0.005% FSR max.

Noise
Randomizer on
25• of an LSB p-p

Randomizer off
1% of an LSB p-p

Absolute Accuracy
±0.1% FSR

DYNAMIC PERFORMANCE

Throughput Rate
33 kHz, min.

S & H Acquisition Time
1.0 μs, max.

Conversion Time
2.0 μs, max.

Overload Recovery Time[3]
1 μs, max.

STABILITY

Differential Non-Linearity (for 1 year from 0°C to +60°C, with ±3% power supply variations)
Randomizer on[1]
1% of an LSB, max.

Randomizer off[2]
0.02% FSR, max.

Gain 0°C o +60°C
±0.1% FSR, max.

Offset 0°C to +60°C
±0.1% FSR, max.

Warm-Up Time[4]
5 minutes

POWER SUPPLY

+15V ±3%
75 mA

−15V ±3%
90 mA

+5V ±5%
160 mA

−5V ±3%
70 mA

Typical Power Dissipation
3.3W

DIGITAL CONTROL INPUTS[5]

Start Conversion
Fan In
2 TTL loads

Pulse Width
100 ns, min.

Randomizer Control
0: Randomizer off
1: Randomizer on

DIGITAL OUTPUTS[5]

Data
Resolution
8-bits, overrange

Fan Out
2 TTL, Tri-state Driver

Format
Offset Binary

Data Enable
Low activates data outputs

End of Conversion (EOC)
Fan Out
2 TTL

Busy
Logic "1"

ENVIRONMENTAL & MECHANICAL

Operating Temperature
0°C to 60°C

Storage Temperature −25°C to +85°C

Relative Humidity
5% to 85%, non-condensing to 40°C

Shielding
Electromagnetic 6 sides, Electrostatic 6 sides

Case Potential
Ground

Dimensions
4.60 x 4.60 x 0.375" max. (116.8 x 116.8 x 9.7 mm)

Notes
1. Consistent with nuclear event large sample quantities per channel.
2. Per individual measurement.
3. From 100% overload (typical range of zoom amplifier.
4. To specified accuracy.
5. TTL compatible.

Description (cont.)

have depended solely on the random number generator to correct for the relatively low differential-linearity characterisitic of high speed converters, the MP8008R has a superior design, highlighted by an 8-bit A/D converter whose components are physically compatible with a true 15-bit connverter and that can attain an ultra-high differential-linearity even with the random number generator turned off. The random number generator, which further minimizes any code width errors by averaging them across a range of N codes, thereby creating virtually equal adjacent code widths, is added to the high-quality basic architecture to assure stability and ultra-high differential-linearity over time and temperature.

With a high speed conversion time of 2.0 μs, the MP8008R provides ultimate 8-bit resolution, utilizing a two-step successive approximation technique of the input signal: an 8-bit approximation of the signal occurs in about 0.5 μs with ½ LSB accuracy; this value is then compared to the analog input signal, and, if necessary, a correction is made to the digital output. This second step takes approximately 1 μs. This technique, therefore, requires only one "slower" major decision, not eight faster decisions as with a conventional 8-bit successive approximation technique.

The MP8008R not only provides ultra-high differential-linearity at a low cost, but with extraordinary versatility. It can easily directly interface with most gamma cameras and data systems now available. It provides reliable performance over a wide temperature range, from 0° to 60°C. Including its built-in sample-and-hold function, it occupies only 8 cubic inches and typically requires only 3.3 watts. It performs with excellent stability and performance over extended periods of time. The MP8008R is thus a state-of-the-art economical averaging A/D converter.

Principles of Operation

The operation of the MP8008R may be best understood by referring to the Functional Block Diagram and the Timing Diagram in Figures 1 and 3.

In a typical imaging application the MP8008R interfaces with two external systems, a gamma camera and a data system, to produce a digitized image of a nuclear event. The gamma camera

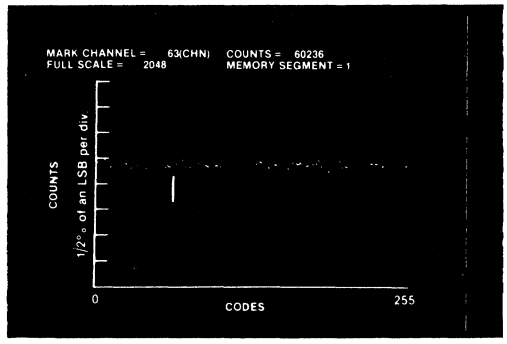


Figure 2. Graph of Differential Linearity.

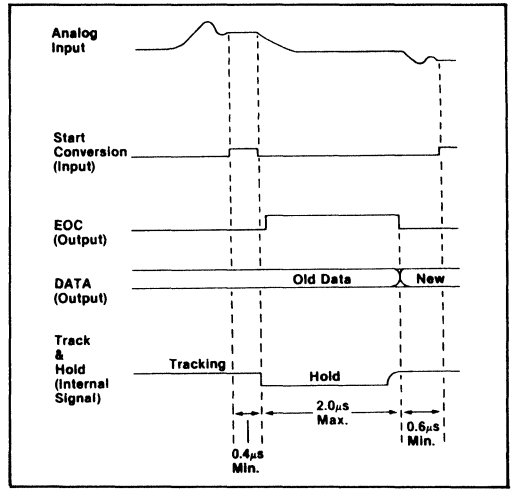


Figure 3. Timing Diagram.

translates each nuclear event into two voltage signals, the amplitude of each signal corresponding to the "X" or "Y" coordinate of the event's position. Each of these signals enters its respective "X" or "Y" MP8008R unit, which converts the amplitude of the analog signal to a digital code. Finally, the digital codes from the "X" and "Y" MP8008R are processed by an external data system that creates a histogram, or image of the nuclear event. The versatile input and output interfacing of the MP8008R allows it to connect easily to most gamma cameras and data systems now available.

The following discussion is limited to the operational analysis of one of the two MP8008R units used in the above process; it should be kept in mind, however, that the "X" and "Y" units function simultaneously and identically.

When a nuclear event occurs, the gamma camera presents an analog voltage signal, ranging from −5V to +5V, to the MP80008R. A random digital output from the random number generator is converted to an analog output by the secondary D/A conveter. This analog output is added to the input signal from the gamma camera, and the "sum" is stored across the sample and hold capacitor.

When the exernally presented start conversion signal occurs, the capacitor voltage is frozen and the ADC converts this voltage "sum" to an 8-bit digital code in 0.5 μs. This code is stored in a register in the A/D converter. The primary precision D/A converter then converts this digital code to an analog output which, in 1 μs, is compared to the previous voltage "sum" by a comparator. The digital output from the register enters the adder, where any changes to the digital code required by the comparator occur and where the random number is then subtracted. The final 8-bit digital code of the analog input signal is presented to the latched, tri-state outputs.

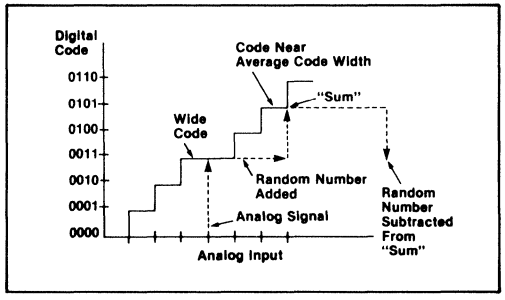


Figure 4. Effect of Randomizing Technique on Differential Linearity. (See text).

By adding a random number to the analog input signal and then subtracting that number from the digital output, all code width errors are averaged over a range of N codes (see Figure 4). Without this averaging scheme a systematic error would result in wide and narrow codes whenever an analog input signal is equal to a point at which the DAC has an error. This method, therefore, substantially reduces these systematic errors by converting the "sum" of a particular analog input signal and a random number at a different, randomly determined code for each measurement, thus averaging differences between adjacent codes over a range of N codes, and thereby achieving virtually equal code widths and an effective differential-linearity of approximately 1% of one LSB for large sample quantities per channel. Ultimately, the result is a substantial reduction of artifacts in the displayed data.

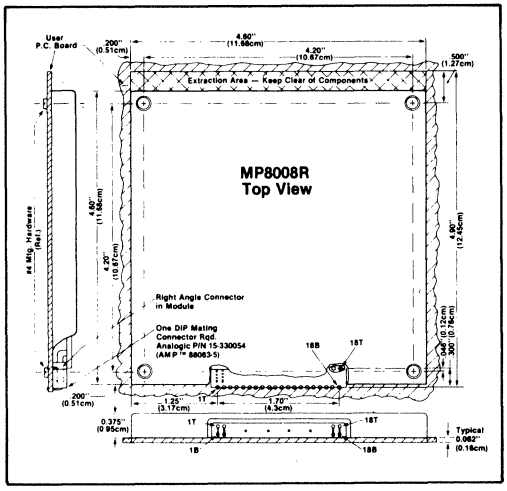
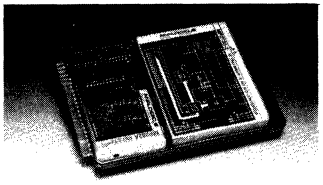


Figure 5. MP8008R Mounting Dimensions.

Signal	Pin	Pin	Signal
+15V	1T	1B	+15V
Analog Return	2T	2B	Analog Return
−15V	3T	3B	−15V
Analog Return	4T	4B	Analog Return
Analog In	5T	5B	Analog Return
Analog Return	6T	6B	Analog Return
−5V	7T	7B	−5V
Out of Range	8T	8B	Data Enable
Randomizer Off	9T	9B	No Connection
Start Conversion	10T	10B	End of Conversion
B1 (MSB)	11T	11B	B2
B3	12T	12B	B4
B5	13T	13B	B6
B7	14T	14B	B8 (LSB)
No Connection	15T	15B	No Connection
No Connection	16T	16B	No Connection
Digital Return	17T	17B	Digital Return
+5V	18T	18B	+5V

ORDERING GUIDE

Specify: **MP8008R.**



ANALOGIC

SHAD-2

Low Distortion, Stereo Pair, Audio Digitizing Subsystem

Description

Analogic's SHAD-2 card with two sample-and-holds, 1-bit auto gain ranger and 15-bit analog-to-digital converter is, we believe, the optimal cost/performance solution to professional audio digitizing. Its 16-bit dynamic range, high-speed, dual-channel sampling capability (up to 57 kHz simultaneous sampling, to 105 kHz single-channel sampling), low harmonic distortion (−86 dB) and exceptionally high linearity (±0.25 LSB) near zero volts ensure that the SHAD-2 satisfies the stringent requirements of audio pulse-code-modulation (PCM) systems and other high precision audio bandwidth applications. Because the SHAD-2 performs simultaneous dual-channel sampling with a single analog-to-digital converter (ADC) and because its one bit of gain ranging combines with a 15-bit ADC to give 16-bit dynamic range, eliminating the need for an expensive 16-bit ADC, the SHAD-2 reduces the cost of audio digitizing by approximately one-half without sacrificing accuracy or speed.

Operation

SHAD-2 operation can be adjusted to meet the requirements of the user. For example, sampling flexibility is provided through separate sample controls in the MP282A which allow simultaneous dual or single-channel sampling. The unit can also be set for parallel or serial data output. For parallel output, the serial clock input should be tied to ground. Serial data is strobed by the falling edge of the clock with the first bit valid after the falling edge of the data ready output (see Figure 2).

Although not usually required in practice, gain and offset may be adjusted through the top edge of the card. To obtain minimum distortion, the potentiometer adjustments should be done with one input connected to a low distortion sine wave with an amplitude just below full scale at a frequency of less than 5 kHz. The MP2735A's offset potentiometer should be adjusted to null the even harmonics, and the

(continued)

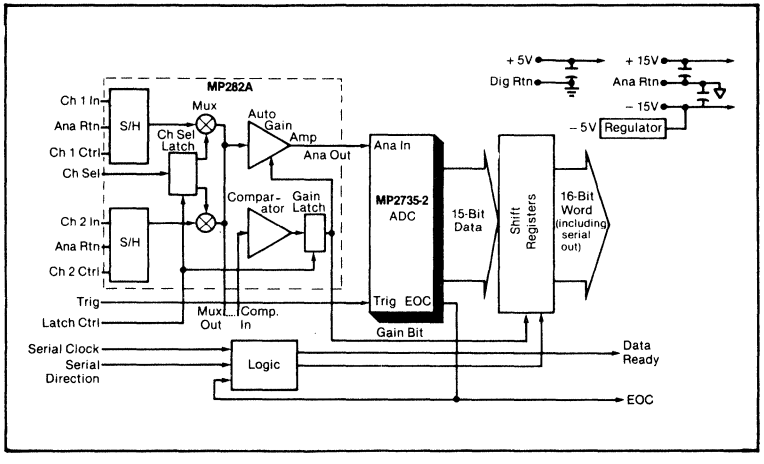


Figure 1. SHAD-2 Functional Block Diagram.

Features

- **Low Harmonic Distortion**
  −86 dB
- **Wide Dynamic Range**
  98 dB
- **High-Speed Sampling**
  105 kHz single channel
  57 kHz dual channel
- **Low Noise**
  −92 dB at 20 kHz bandwidth
- **Low Cost**
- **Automatic 1-Bit Gain Ranging**
- **Low Crosstalk**
  −86 dB
- **Low Aperture Uncertainty**
  less than 0.4 ns
- **High Stability Over Time and Temperature**

Applications

- **Multitrack PCM for Professional Audio Recording**
- **Self-Contained Record and Playback**
- **Vibration Analysis**
- **Spectrum Analysis**
- **Seismic Exploration**
- **Sonar Systems**
- **Instrumentation**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUTS

Number of Inputs
2 channels

Full Scale Linear Voltage
± 5V

Voltage, damage limit
± 15V

Impedance
47 kΩ/ /10 pF[1]

TRANSFER CHARACTERISTICS

Full Power Bandwidth (Sample Mode)
150 kHz typ.

Slew Rate (Sample Mode)
6 V/μs typ.

Crosstalk[2]
– 86 dB

Gain, Referred to Input (RTI)
+ 1 or + 2

Sample and Hold Acquisition Time[3]
3.0 μs max.

Aperture Delay Time
50 ns

Aperture Uncertainty
0.4 ns

Channel Select Multiplexer Settling Time[3]
2.0 μs max.

Auto Range Amplifier Settling Time[4]
1.0 μs max.

Sampling Rates
Single-Channel
105 kHz

Dual-Channel
57 kHz

ACCURACY AND STABILITY

Harmonic Distortion
20 Hz to 10 kHz
– 86 dB max.

10 kHz to 20 kHz
– 84 dB max.

Gain Accuracy (0°C to 60°C)
± 0.1 dB max.

Noise (shorted input; 20 kHz bandwidth)
– 92 dB, Referred to rms full scale

Gain Change Trip Point (RTI)
± 2.35V nominal

at 25°C from 0° to 60°C
≤2.47V

Differential Nonlinearity
± 0.5 LSB max., 0.25 LSB typ. at ± 0.25 FSR
± 1.0 LSB max., 0.25 LSB typ. at ≥0.25 FSR

Tempco of Gain
± 15 ppm FSR/°C[7]

Tempco of Offset
± 15 ppm FSR/°C[7]

DIGITAL INPUTS

Logic Type
TTL

Control Channel 1 or Channel 2
2 lines

Sample Mode
TTL Low

Hold Mode
TTL High

Required Rise Time
10 ns max.

Channel Select
1 line

Channel 1
TTL High

Channel 2
TTL Low

Latch Control
1 line

Transparent
TTL High

Latches
High-to-low transition
Latch Control Simultaneously Effects Channel Select and Gain Output

Trigger Load
2 TTL

Width
100 ns min.
5 μs max.

Conversion Starts
On low-to-high transition

Serial Clock Load
2 TTL

Rate
5 MHz max.

Timing
High-to-low transition shifts data

Serial Direction
High, MSB first out at MSB, low LSB first out at LSB

Load
2 TTL

DIGITAL OUTPUT

Digital Word Length
16 bits

Coding
Complementary offset binary

Dynamic Range
16 bits total; 1 bit multiplier plus 15 bits mantissa, including sign

Internal Architecture
1 sign bit plus 1 gain bit plus 14 magnitude bits

Multiplier (Gain)
1 or 2

Parallel Data
TTL positive true 5 unit loads/line, 16 lines

Serial Data
Complementary offset binary out of MSB or LSB output lines

DIGITAL OUTPUT

End of Conversion (EOC, A/D ready↓)
High during conversion; 2 TTL unit loads

Data ready (SHAD-2 ready↓)
Falling edge

POWER, MECHANICAL, ENVIRONMENTAL

Power Supplies[5]
+10V to +15V @ 80mA typ.
−10V to −15V @ 125mA typ.
+5V ±5% @ 200mA typ.

SHAD-2 Printed Circuit Card
(4.62" x 5.78" x 0.55")[6]
(117 x 147 x14mm)

NOTES

1. If other values are required, please consult factory.
2. Over the frequency range of 20 kHz and inputs at 0 dB (FS) to −15 dB measured as the peak line by a spectrum analyzer with 100 Hz bandwidth.
3. To ±0.005% final value.
4. Measured from high-to-low transition of latch control input.
5. Separate analog, digital and signal returns all internally connected.
6. From surface of board to top of modules (please see mounting diagram).
7. Typical values.

Operation (cont.)

MP282A's gain potentiometer (controlling the gain ranging amplifier) should be adjusted to null the odd harmonics. For instrumentation applications, the offset potentiometer on the SHAD-2 board should be adjusted until the least significant bit (LSB) of the output code, 100...00/1 alternates equally between "0" and "1" when the measured potential across pins X and W of the SHAD-2 is −150 μVdc. The gain potentiometer of the MP2735-2 should be adjusted until the LSB of the output code 111...10/1 alternates equally between "0" and "1" when the same input potential of the SHAD-2 is −4.99954 Vdc.

Application

The SHAD-2, with its wide dynamic range, low harmonic distortion, dual channel sampling and ultra-low idle noise, is designed to meet the demands of professional audio applications and digital transmission systems. Placed back-to-back with the MP1926A or MP1936 digital-to-analog converters, and the MP201A or AH201 distortion suppressors, the SHAD-2 becomes part of a total audio system* offering exceptional performance at remarkably low cost.

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* For more information on Analogic's audio system, please send for data sheets on the MP282A, MP2735, MP1926A, MP1936, MP201A and AH201.

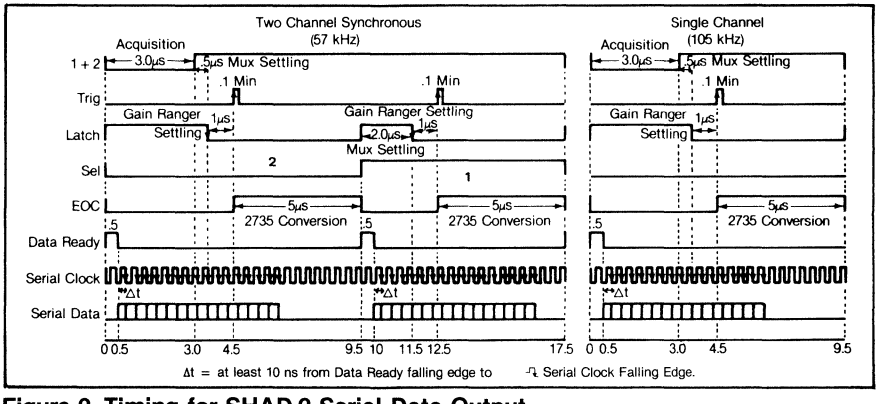
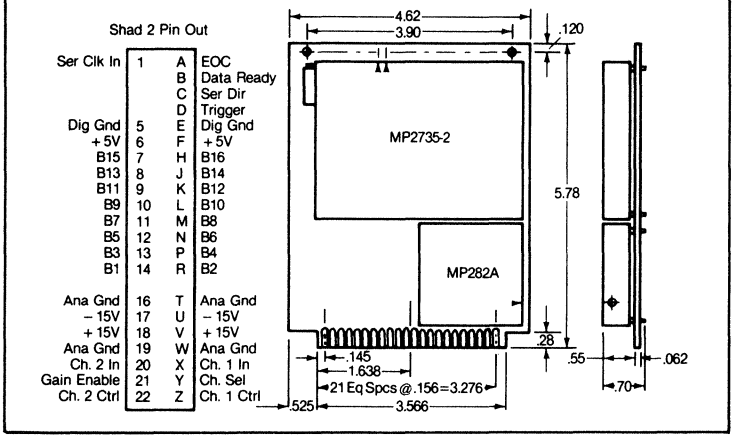


Figure 2. Timing for SHAD-2 Serial Data Output.

MOUNTING DIMENSIONS & PINOUTS



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Specify **SHAD-2**

ANALOGIC®

SECTION 6

Digital-to-Analog Converters

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SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
Repeatability	High Stability	13-Bit Accuracy	MP1913A	6-47
		14-Bit Accuracy	MP1914A	6-47
		15-Bit Accuracy	MP1915A	6-47
		16-Bit Accuracy	MP1916A	6-47
	High Stability Temperature Compensated	14-Bit Accuracy	MP1914TC	6-51
		15-Bit Accuracy	MP1915TC	6-51
		16-Bit Accuracy	MP1916TC	6-51
Extreme Repeatability	Extreme Stability High Absolute Acc.	16-Bit Accuracy	MP8116	6-73
Digital Audio Reproduction	Low Harmonic Distortion, High Throughput & Stability	Low Drift	MP1926A	6-55
		Low Drift Integral Distortion Suppressor	MP1936	6-63
High Stability	Long-Term Drift	Moderate Settling Time	MP1926S	6-55
Process Control	4-20 mA Current Loop Output	12-Bit Binary or 3 Digit BCD Input	MP1480S	6-37
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Monochrome Composite Video	8-Bit TTL	40 MHz Pixel Rate	MP8308 TTL	6-79
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GLOSSARY OF TERMS

DIGITAL TO ANALOG CONVERTERS

ABSOLUTE ACCURACY A measure of the largest static difference between the actual output and that predicted by the ideal transfer function, expressed as a percentage of full-scale output. In the case of a bipolar output range, e.g., −10V to +10V, the absolute accuracy is computed as a percentage of the the full range, or 20V. Absolute accuracy measurements must reference a voltage standard traceable to the NBS with at least an order of magnitude lower uncertainty than the difference represented by one LSB.

DAC A Digital to Analog Converter is a device that accepts signals in the form of a binary code at its input terminals and generates a corresponding analog output. Figure 1 shows the black box representation of a DAC. The ideal transfer function for a three bit, unipolar binary DAC is shown in Figure 2.

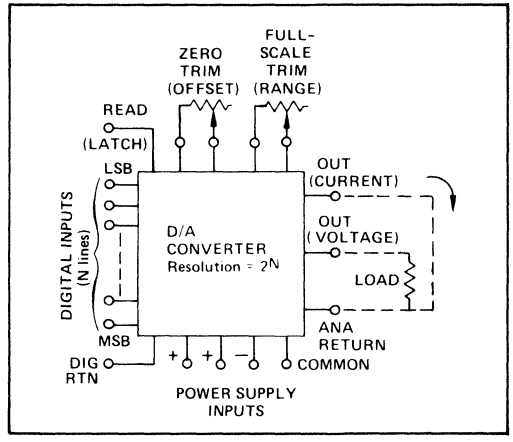


Figure 1. "Black Box" Representation of a DAC.

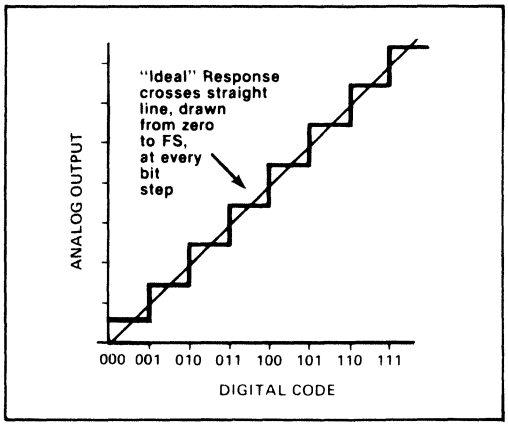


Figure 2. Theoretical Transfer Function of a DAC (first three LSBs only).

DIFFERENTIAL LINEARITY A parameter that measures the actual change in output voltage between adjacent codes compared to the ideal voltage change for adjacent codes. It is expressed as a percentage of the ideal voltage bandwidth or as a fraction of an LSB. Figure 3 demonstrates differential linearity.

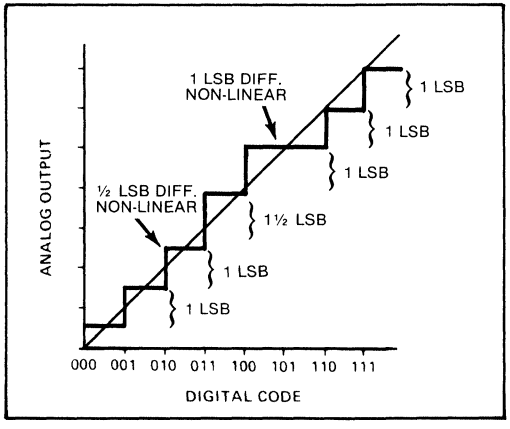


Figure 3. Differential Linearity.

DRIFT WITH TIME Drift with time is a change in parameters as a result of component aging. The parameters most affected are offset and gain. Linearity and the tempco's may also be slightly affected. Burn-in at the factory significantly decreases the long term drift. Provision is generally made for recalibration after a specified time period to maintain the rated accuracy.

GAIN The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift. See Figure 4.

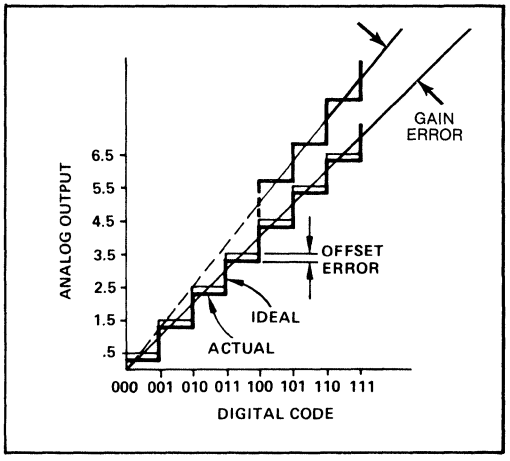


Figure 4. Gain and Offset.

GLITCH A noise spike at the output of a DAC caused by unequal propagation delays through the input registers and the equidelay current switches. Glitches typically occur at major carry points when running at high update rates.

GLITCH AREA The energy content of a glitch, measured in volt-seconds. It is the area under the curve in Figure 5.

GLITCH SETTLING TIME A measure of the duration of a glitch as a result of a worst case transition. It is specified as the length of time that its level exceeds 1 LSB.

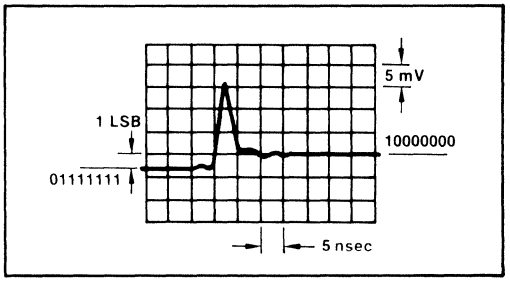


Figure 5. Typical Glitch at Major Carry (worst-case transition). Glitch is Approximately 40 mV-ns.

INPUT CODE The binary code for the input of a particular DAC. The various codes include: unipolar binary, offset binary, one's complement and two's complement, as shown in Figure 6. Another popular code is BCD, not shown.

Unipolar Binary

$$V_{out} = V_{FS}\left[\sum_{n=1}^{n=N}\left(\frac{a_n}{2^n}\right)\right] \quad \text{where } a_n = 1 \text{ or } 0.$$

This expression relates the actual output voltage (V_{out}) to the *nominal* full-scale voltage (V_{FS}), for a finite bit-length (N). Note that, for N = ∞, and all ONES (all a_n's set at 1), $V_{out} = V_{FS}$. For a *finite* number of bits (finite N), the maximum output (V_{max}) is less than V_{FS}, and is given by:

$$V_{max} = V_{FS}\left[1 - \frac{1}{2^N}\right]$$

Example: for a 12-bit unipolar binary device with a 0 to +10 Volt nominal full-scale range,

V_{max} = 111 111 111 111 = +9.9976 Volts V_{min} = 000 000 000 000 = 0.0000 Volts

Offset Binary Using the same nomenclature as above,

$$V_{out} = V_{FS}\left[\sum_{n=1}^{n=N}\left(\frac{a_n}{2^{(n-1)}} - 1\right)\right]$$

$$\text{and } V_{max}\text{ (positive)} = V_{FS}\left[1 - \frac{1}{2^{(N-1)}}\right] \quad \text{and } V_{max}\text{ (negative)} = V_{FS}$$

Example: for a 12-bit offset-binary device with a −10 Volt to +10 Volt nominal full-scale range,

V_{max} (positive) = 111 111 111 111 = +9.9951 Volts
V (mid scale) = 100 000 000 000 = 0.0000 Volts
V_{max} (negative) = 000 000 000 000 = −10.0000 Volts

One's Complement

$$V_{out} = V_{FS}\left[\sum_{n=2}^{n=N}\left(\frac{a_n}{2^{(n-1)}}\right) - a_1 + \frac{a_1}{2^{(N-1)}}\right]$$

$$V_{max}\text{ (positive)} = V_{FS}\left[1 - \frac{1}{2^{(N-1)}}\right] \quad \text{and } V_{max}\text{ (negative)} = -V_{FS}\left[1 - \frac{1}{2^{(N-1)}}\right]$$

Example: for a 12-bit device with one's complement coding, and a nominal full-scale range of −10 Volts to +10 Volts, V_{max} (positive) = 011 111 111 111 = +9.9951 Volts

V (mid scale) = {000 000 000 000 / 111 111 111 111} = 0.0000 Volts

V_{max} (negative) = 100 000 000 000 = −9.9951 Volts

Two's Complement

$$V_{out} = V_{FS}\left[\sum_{n=2}^{n=N}\left(\frac{a_n}{2^{(n-1)}}\right) - a_1\right] \quad \text{and } V_{max} = V_{FS}\left[1 - \frac{1}{2^{(N-1)}}\right]$$

Example: for a 12-bit device with two's complement coding and a nominal full-scale range of −10 Volts to +10 Volts,

V_{max} (positive) = 011 111 111 111 = +9.9951 Volts
V (mid scale) = 000 000 000 000 = 0.0000 Volts
V_{max} (negative) = 100 000 000 000 = −10.0000 Volts

Figure 6. Most Common Binary Codes.

MONOTONICITY Is a characteristic that describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output voltage (current) continuously increases as the input code increases, and if the output voltage (current) continuously decreases as the input code decreases. Figure 7 demonstrates non-monotonic behavior.

NOMINAL DIGITAL LEVELS Digital input signal level convention. This is typically TTL, ECL, etc., or two specific voltage ranges.

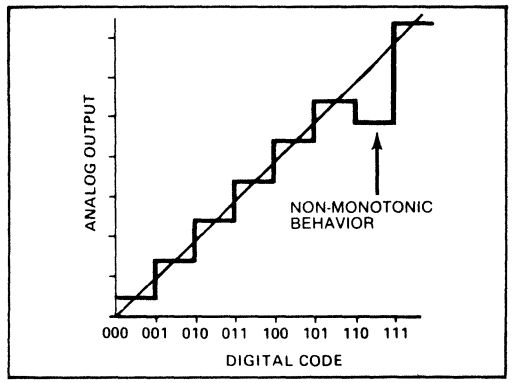


Figure 7. Non-Monotonic Behavior.

OUTPUT RANGE The polarity, magnitude and unit of measure of the analog output corresponding to minimum and maximum input codes. Unipolar outputs range from 0 to full scale. Bipolar outputs range from negative full scale to positive full scale. The unit of measure is specified as either voltage or current.

POWER SUPPLY COEFFICIENTS Also stated as power supply sensitivity, this specification indicates how the output of the DAC is affected by changes in the power supply voltage. e.g., 5 ppm FSR/% change in dc voltage.

RELATIVE ACCURACY This is a measure of the largest deviation of the DAC's actual transfer function from the best straight line approximation of the actual transfer function, expressed as a percentage of full scale range. It comprises errors due to linearity, drift and circuit component tolerances. e.g., ± 0.005% of FSR.

RESOLUTION The number of unique codes the converter will accept at the input data lines. The resolution of an N-bit converter is 2^N.

SETTLING TIME The time it takes for the output of a device to stabilize after an instantaneous code change at the input. It is measured as shown in Figure 8 starting from the leading edge of the input to the point where it enters a defined equilibrium band, typically ± 0.5 LSB.

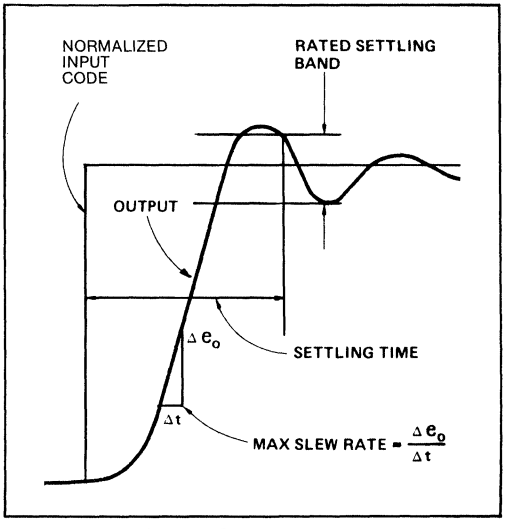


Figure 8. Defining Slew Rate and Settling Time.

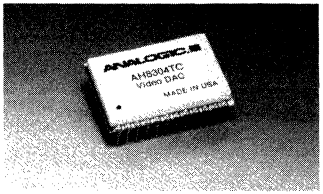
SLEW RATE The maximum slew rate is the fastest rate of change of the output of the DAC as shown in Figure 8. It limits the highest frequency of large-signal sine wave output that can be obtained from the circuit.

TEMPERATURE COEFFICIENTS Changes in the operating temperature can affect a number of parameters including zero offset, gain and differential linearity. The temperature coefficient, or tempco, of one of these parameters is computed as the change in that parameter over a specified temperature range divided by the number of degrees in that temperature range. This yields an average tempco over the temperature range, not the worst case. Analogic tempco specifications are conservative and generally may be considered worst case values.

THROUGHPUT The maximum throughput rate is the greatest number of D/A conversions per second at which a DAC will deliver its full rated static performance regardless of the rate at which the output changes.

VIDEO DAC Video DAC's are specialized digital to analog converters designed specifically for use in video or graphics display systems, where low resolution and high speed are the dominant requirements. Digital inputs include the video data and lines for strobe, sync, blanking, etc. The inputs are converted to a composite video output signal, compatible with RS170, RS330 and/or RS343, for driving a video monitor.

ZERO OFFSET The actual DAC output obtained by applying the input code corresponding to theoretical zero output. Provision is normally made to allow the user to adjust the zero offset to compensate for temperature, power supply voltage, drift with time, etc. See Figure 4.



ANALOGIC®

AH8304TM/TC

RGB 4-Bit Composite Video D/A Converters

Description

The **AH8304** video D/A converters are third generation hybrid devices that provide designers of low- to medium-cost color display systems with a complete, self-contained, TTL compatible, composite video subsystem in a 24 pin DIP. Offered as both an RGB 4-bit D/A only, or with integral color look-up table memory, the **AH8304** features advanced single-chip design that provides low power, high reliability, small size and low cost.

The **AH8304TM** color-mapped video D/A converter is designed for the color graphic system where space is at a premium. Both the functions of triple (RGB) video D/A converter **and** color look-up table memory are provided within a single 24-pin package. Data can be written into the internal 32 word RAM (one for each color channel) such that 32 colors can be defined out of a possible 4096 at any given time. During the display (Read) interval, any of these 32 colors can be addressed from a 5-bit bus. Separate Sync, Blanking and D/A Strobe control inputs are provided.

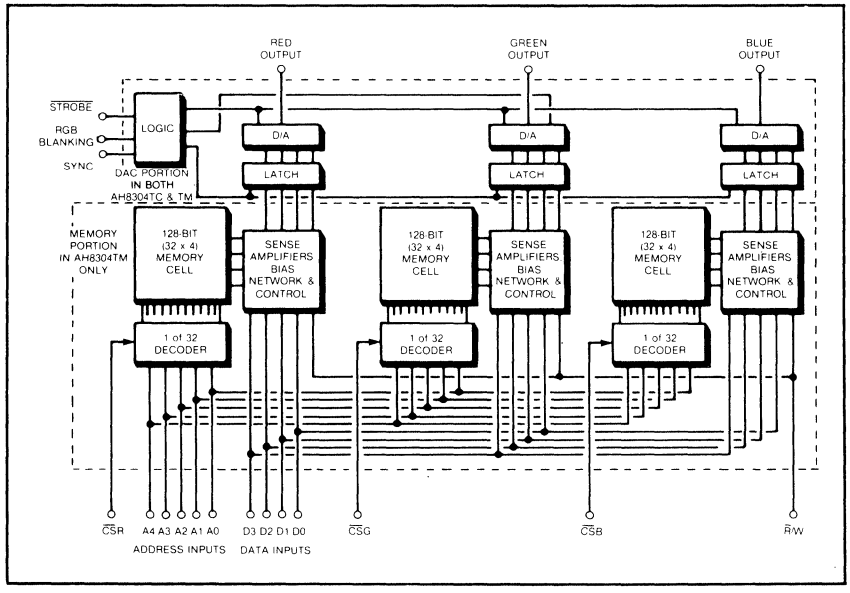
The **AH8304TC** D/A converter only is offered for those systems where a different configuration of look-up table memory is required. The D/A accepts 4-bit TTL data at an update rate of up to 100 MHz for each D/A. Common Blanking, Strobe and Sync (Green Channel only) controls are provided. The output of each channel is RS170/RS330/RS343 compatible, providing a 75Ω source impedance and 1 Vp-p output signal.

Features

- **Available with and without color look-up table**
  AH8304TC 100 MHz D/A
  AH8304TM 20 MHz D/A with 32 word memory
- **TTL compatible**
- **Synchronous Blanking**
- **4096 color palette**
- **RS170/RS330/RS343 composite video output**
- **Low Power Dissipation**
  2.0W maximum for D/A and memory
  1.75W maximum for D/A only
- **24-pin DIP**

Applications

- **Color graphic workstations**
- **Personal Computers**
- **Low-end CAD/CAM Systems**



AH8304TM/TC Block Diagram

SPECIFICATIONS

(All specifications are guaranteed at 25°C unless otherwise noted)
(All specifications applied to both AH8304TC and AH8304TM unless otherwise noted)

OUTPUT CHARACTERISTICS (Each Channel)

Gray Scale Output
0.000V to −0.643V, ±3% of Gray Scale; assumes load of 75Ω ±0.5% and −5.0V power supply

Recommended Load Impedance
75Ω, ±5%; dc to 50 MHz

Source (Thevenin) Impedance
75Ω, ±3%; dc to 50 MHz

LSB Size
42.9 mV, nominal

Full Scale Step Settling Time
5 ns typical, 7 ns maximum to 1 LSB after propagation delay

Glitch
Total Glitch Energy less than 250 pV-s for major code transition (0111 to 1000 or vice versa)

Cable Drive Capability
75Ω characteristic impedance; to avoid appreciable signal loss, total length should have no more than 7.5Ω dc resistance

RGB Blanking Level
−0.714V, with 71 mV (10 IRE Unit) setup; offset is 2 mV maximum, from 0°C to +55°C

Sync Level (Green Channel Only)
−1.000V; −0.286V (−40 IRE Units) with respect to Blanking level

TRANSFER CHARACTERISTICS (Each Channel)

Resolution
4-bits, 16 Gray Scale levels; 42.9 mV per step nominal

Reference White Level
1111 produces 0.000V absolute; 100 IRE Units relative to Blanking level

Reference Black Level
0000 produces −0.643V absolute, 10 IRE relative to Blanking level

Blanking Level
Active BLANKING control reset all DACs to 0000 and drives all outputs to −0.714V

Differential Non-linearity
±1/2 LSB, maximum

Monotonicity
Guaranteed

Transfer Gain (Slope) Tempco
±0.1% FSR/°C

RGB Blanking Input Delay
7 ns typical to 10% of final value after STROBE goes low

INPUT CHARACTERISTICS

Logic Levels (all inputs)
Standard TTL levels
Logic 1 >2.4V
Logic 0 <0.4V
No input to go below −0.3V
(CMOS limits)

Loading —
Data, Address, and Strobe
2 Unit Load
Control Inputs
2 Unit Load

Coding —
Data and Address
Binary

Data Update Rate
100 MHz maximum (AH8304TC); 20 MHz maximum (AH8304TM)

Memory Size
32 word by 4-bit (each RAM/channel) (AH8304TM only)

Control Inputs —
DAC $\overline{\text{Strobe}}$
Input data entered into all three DAC channels simultaneously on negative-going edge

Rise and Fall Time
<10 ns (10% to 90%)

DAC Propagation Delay
7 ns typical, $\overline{\text{STROBE}}$ to output, 50% points

Blanking Rise and Fall Time
<10 ns (10% to 90%)

RGB Blanking
Logic 1 on RGB Blanking input resets all DAC inputs to 0000 and drives all DAC outputs to −0.714V; RGB Blanking is synchronous with $\overline{\text{STROBE}}$; next $\overline{\text{STROBE}}$ after Blanking released loads input data

Sync
Logic 1 on RGB Blanking and Sync inputs resets all DAC inputs to 0000 drives Red and Blue outputs to −0.714V, and Green output to −1.000V absolute, −0.286V (−40 IRE Units) relative to Blanking level

Sync Rise and Fall Time
<10 ns (10% to 90%)

Read/Write
(AH8304TM only)
Logic 0 select Read operation; logic 1 selects Write operation; DAC outputs will retain previous Read value until STROBE input is applied; STROBE applied during Write operation causes Reference Black output level from all DACs

Address — 5-bits (A0 to A4)
(AH8304TM only)
Determines location in memory for Read or Write operation; used as Address input to load RAM arrays in Write mode and as look up table inputs in Read (Display) mode

Chip Select — CSR, CSG, CSB
(AH8304TM only)
CHIP SELECT for each channel (RED, GREEN, BLUE); logic 0 selects RAM channel for Read or Write operation; when deselected, RAM data output is all 0's to DAC inputs; DAC output of

deselected channels will retain last Read level if no STROBE applied, otherwise output will fall to Reference Black level; normally only one input at a time is enabled (selected) to write data to its corresponding RAM; all inputs are enabled to read data during display; these may be held at logic 0 throughout the read cycle

Data
16 Valid levels per channel;
D0-D3 (AH8304TC only)
R0-R3 (Red) (AH8304TM only)
G0-G3 (Green) (AH8304TM only)
B0-B3 (Blue) (AH8304TM only)

DYNAMIC CHARACTERISTICS

Width of Write Pulse
25 ns minimum (AH8304TM only)

Data and Address Before Write
30 ns minimum (AH8304TM only)

Data and Address Hold Time
20 ns minimum (AH8304TM only)

Data Setup Time
2 ns minimum (AH8304TC only)

Data Hold Time
1.5 ns minimum (AH8304TC only)

Address Access Time (after valid address)
48 ns maximum (AH8304TM only)

Chip Select Access
40 ns minimum (AH8304TM only)

Chip Select Disable
35 ns maximum (AH8304TM only)

POWER REQUIREMENTS

+5.0V, ±5%
50 mA maximum; 50 mVp-p ripple maximum (AH8304TC)
100 mA maximum; 50 mVp-p ripple maximum (AH8304TM)

−5.0V
200 mA maximum; 30 mVp-p ripple maximum (−4.75V to −5.5V operating range)

Power Dissipation
1.25W typical, 1.75W maximum (AH8304TC)
1.50W typical, 1.56W maximum (AH8304TM)

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Dimensions
1.00" x 1.30" x 0.3" maximum
(25.4 x 33.14 x 7.62 mm)
24-pin triple width DIP

SPECIAL TESTING

Burn-in
24 Hours at +125°C to be performed prior to final test

Operation

The **AH8304TM** consists of two major functional blocks: (1) a memory organized as three 32-word by 4-bit blocks, one for each color channel, with common data, Read/Write control, and address inputs, separate chip select inputs and data outputs, and (2) a triple 4-bit D/A converter with common Sync, Blanking and Strobe control inputs. Data flow is always from the output of the memory to the input of the D/A converter.

During a Write operation, data to be loaded into the look-up table RAM is presented to the DATA inputs. The CHIP SELECT line for the color channel RAM that is to receive the data is brought low to enable it. The READ/WRITE line is pulsed, causing the data to be written into the RAM location corresponding to the address that is presented to the five ADDRESS inputs. The CHIP SELECT line is then brought high to disable that channel. The process can then be repeated for other addresses and/or color channels.

During a Read (display) cycle, all three CHIP SELECT lines are brought low to enable all channels, and the RAM address for the color to be displayed is presented to the ADDRESS inputs. After a propagation delay through the memory of 48 ns maximum, the data from the addressed RAM location appears at the output of the memory. The D/A STROBE line is then pulsed to latch the data into the D/A converter input register. After a propagation delay through the D/A converter, the corresponding analog output voltages appear at the three D/A outputs.

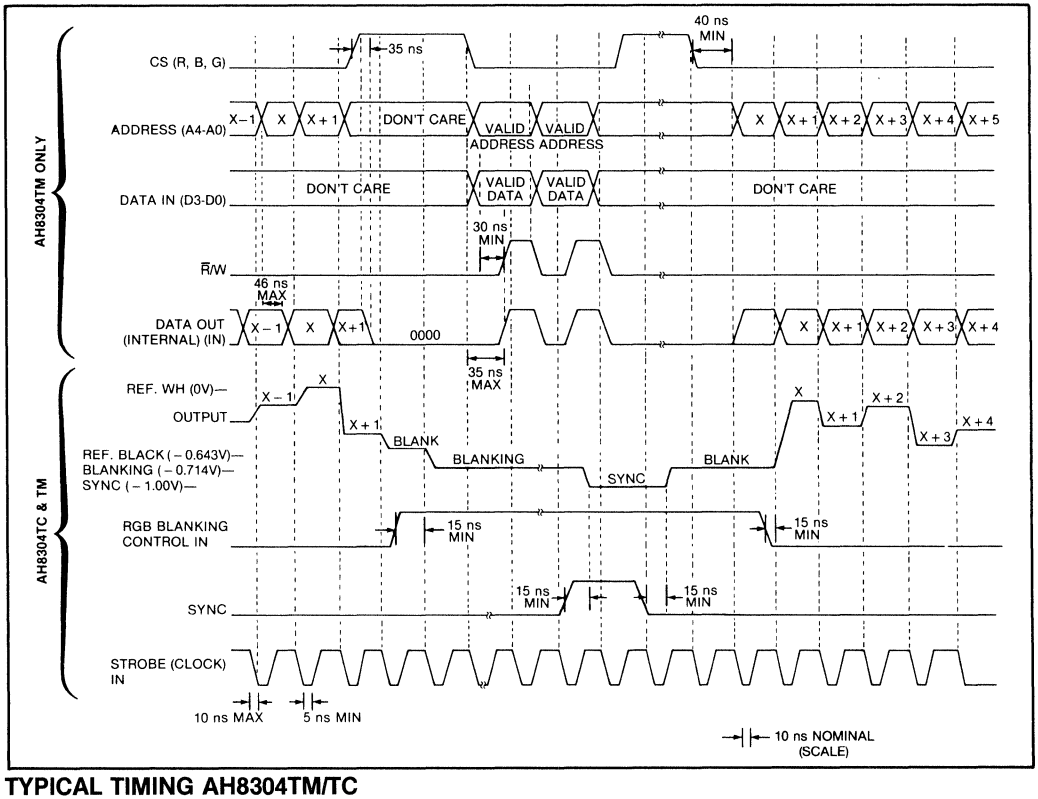
The **AH8304TC** D/A only (and the D/A portion of the **AH8304TM**) accepts a 4-bit data word for each of the three video channels (Red, Green, and Blue). The data is presented to the DATA inputs and held for the duration of the setup time, and the STROBE is pulsed to load the data into the three D/As. During the blanking interval, the BLANKING control line is activated by a logic 1. At the next STROBE pulse, this resets the three input registers to 0000 and drives the D/A outputs to the blanking level. When the SYNC line is activated, the output of the Green channel is driven to the sync level. At the end of the blanking/sync in-

terval, the SYNC and BLANKING controls are released (i.e. returned to a logic 0). At the next STROBE to the D/A, the data present at the DATA inputs to the D/A is loaded into the input registers, and will subsequently appear at the D/A outputs after the D/A propagation delay.

INPUTS							
DATA D3-D0	ADDRESS A4-A0	$\overline{CS}$	$\overline{R/W}$	BLANKING	SYNC	$\overline{STROBE}$	FUNCTION
X	VALID	L	L	L	L	H→L	RAM Data Loaded into DAC
X	X	L	L	H	L	H	Previous Data Value From RAM at DAC Output
X	X	L	L	H	L	H→L	DAC Output at Blanking Level
X	X	L	L	H	H	X	DAC Output at SYNC Level
X	X	H	L	L	L	H→L	DAC Output at Ref. Black Level
X	X	H	L	H	L	L	Last Data Value at DAC Output
VALID	VALID	L	H	H	L	H→L, then X	Data Loaded into RAM, DAC Out at Blanking Level
VALID	VALID	L	H	L	L	H→L	DAC Output at Reference Black

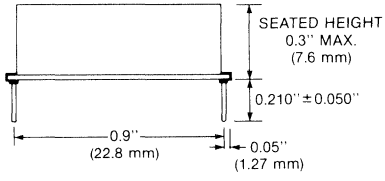
Truth Table — AH8304TM

X = don't care



TYPICAL TIMING AH8304TM/TC

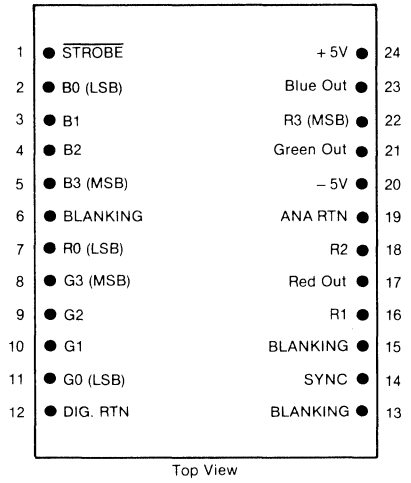
MECHANICAL



PINS ON 0.1" (2.5 mm) CENTERS

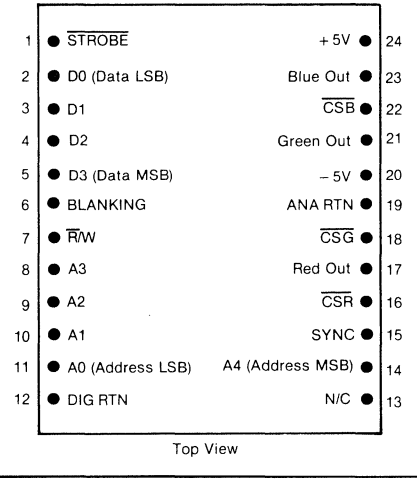
PINOUT

AH8304TC



Top View

AH8304TM

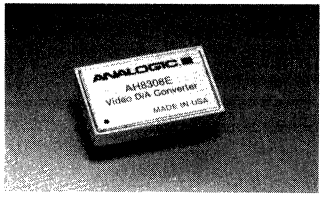


Top View

ORDERING GUIDE

20 MHz, RGB 4-bit D/A with 32 word lookup table memory.....Specify **AH8304TM**

100 MHz, RGB 4-bit D/A.....Specify **AH8304TC**



ANALOGIC®

AH8308E

8-Bit Composite Video D/A Converter

Description

The AH8308E is an optimally designed, low power, minimum glitch, high-speed 8-bit composite video D/A converter intended for use in both color and monochromatic Digital Display Systems. It accepts 8-bit digital video data plus sync and blanking commands from an ECL source and produces a composite video output to directly drive a 75Ω load at an update rate as high as 150 MHz.* The 150 MHz update rate, uncontested by competing units, makes this device compatible with the highest resolution monitors available.

A second generation unit drawing on the success of the current industry standard MP8308, the AH8308E represents a completely new design utilizing an optimum combination of hybrid techniques and the successful marriage of both analog and digital circuits on a single custom monolithic VLSI chip. This combination is a significant advance over competing units which are either discrete component devices (modules) or "hybridized" versions of discrete designs. Of particular importance is that the AH8308E achieves its remarkable 150 MHz data update rate at a power dissipation level 25% lower than that of the earlier generation MP8308 or of the other competing modular or hybrid devices patterned after it. All of this has been accomplished without

*A TTL version is also available from Analogic. Please consult the factory for information and applications assistance.

(continued)

Features

- **Up to 150 MHz Update Rate**
  Extends display system capabilities
- **Direct Drive to 75Ω Coaxial Cable/TV Monitor**
  Requires no additional circuitry
- **"Glitch-free" performance**
  Simplifies display system design
- **Single −5V Supply**
  Reduces power requirements
- **Composite Sync and Blanking Control Inputs**
  Eliminates need for additional logic or amplifiers
- **10% Overbright Control Input**
  Provides Simple Cursor Generation
- **3 ns Rise and Fall Time**
  Provides accurate, high-speed data update
- **RS170A/RS343A Compatible Output**
  Directly drives monitor
- **Standard 0.790" X 1.305" X 0.295" Package Size**
  Reduces pc board area requirements
- **Pin Compatible with Hybrid Reproductions of Our Earlier Generation MP8308**

Applications

- **CAD/CAM Display Systems**
- **Medical Imaging Systems**
- **"Quick Look" Display Systems**
- **Image Processing Systems**
- **Workstations**
- **Monochrome or Color Display Systems**

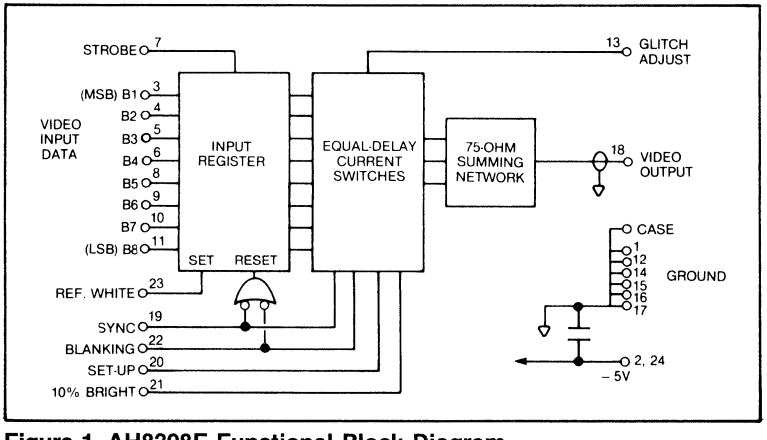


Figure 1. AH8308E Functional Block Diagram.

SPECIFICATIONS

(All specification guaranteed at 25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

Output Voltage Range

Composite Video
0V to −1.064V; ±3% into 75Ω termination

Gray Scale
−0.064V to −0.707V; ±3% into 75Ω termination

Output Current (Gray Scale)
−17 mA

Recommended Load Impedance
75Ω ±5%, dc to 50 MHz

Source (Thevenin) Impedance
75Ω ±5%, dc to 50 MHz

LSB Size
2.5 mV, nominal

Rise and Fall Time
3 ns, typical, 4 ns maximum (10% to 90%)

Full Step Settling Time
8 ns typical to 1 LSB (0.4%)

Glitch Settling Time
5 ns to <1 LSB for worst MSB transition

Glitch Area
50 pV-s typical, 70 pV-s max.

Compliance Voltage
+1.1V to −1.1V typical

Cable Drive Capacity
75Ω characteristic impedance. Total length to have 7.5Ω dc resistance maximum.

Composite Sync Level
−1.064V with Standard Setup
−0.286V (−40 IRE Units) with respect to blanking level (back porch)

Composite Blanking Level
−0.778V, with Standard Setup

10% Overbright Level
0V

TRANSFER CHARACTERISTICS

Resolution
8 Bits, 256 Gray Scale Levels
2.5 mV per step, nominal

Coding
Binary

Reference White Level
11111111 produces −0.064V absolute, +0.714V (100 IRE Units) relative to blanking level with Standard Set-up; +0.643V relative to Reference Black

Reference Black
00000000 produces −0.707V absolute, +0.071V (10 IRE Units) relative to blanking level with Standard Set-up

Differential Linearity
± ½ LSB maximum

Monotonicity
Guaranteed

Offset (dc output with 10% Overbright Actuated)
± ½ LSB maximum, 0°C to +55°C

Transfer Gain (Slope) Tempco
±0.1% FSR/°C maximum

Propagation Delay
5 ns typical, strobe to output, 50% points

Control Input Speed (Sync, Blanking, Ref. White and 10% Overbright)
8 ns typical to settle to 10% of final value

INPUT CHARACTERISTICS

Logic Levels (all inputs)
10,000 Series ECL
Logic 0 = −1.75V
Logic 1 = −0.9V

Loading (all inputs)
5 pF; open transistor base;
open input is logic "0"

Data
8 ECL compatible inputs

Validity
Data must be valid 2.0 ns min., prior to Strobe and remain valid for 1.5 ns after data Strobed

Update Rate
150 MHz maximum

Strobe Input
Data entered on positive-going edge (Timing Reference)

Pulse width
3 ns minimum

Setup (Reference Black to Blanking)
Input open: Standard 71 mV (10 IRE Units)
Input to −5.0V: 142 mV (20 IRE Units)
Input to Ground: 0 mV (0 IRE Units)

Composite Sync Level
Logic "0" on Sync and Blanking inputs simultaneously resets the input register to 00000000 and drives the output to −1.0643V

Composite Blanking Level
Logic "0" on Blanking input simultaneously resets the input register and drives the output to −0.778V

Reference White Level
Logic "0" on Ref. White input simultaneously sets input register to 11111111 and drives output to −0.064V

10% Overbright Level
Logic "0" on input raises output level by 0.064V. Logic "0" on Ref. White and 10% Overbright drives output to 0V

Rise and Fall Time (all inputs)
<10 ns (10% to 90%)

Glitch Adjust

Control Port Input Impedance
7.5 kΩ

Control Sensitivity
50 pV-s per volt applied to Glitch Adjust pin

POWER SUPPLY REQUIREMENTS

Power Dissipation
0.875 watt typical, 1.0 watt maximum

Power Supply Required Regulation
−5.0V @ 200 mA maximum 5 mV p-p ripple
−4.75V to −5.5V operating range

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range (Ambient)
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to +40°C

Mechanical Dimensions
0.790" X 1.305" X 0.295"
(20.07 X 33.14 X 7.49 mm)
24-pin DIP

Shielding
Steel foil

Description (cont.)

sacrifice of the trend-setting features of its discrete predecessor such as composite video 75Ω output and "glitch free" performance.

Because of its single chip design, the unit has fewer internal wire bonds than other presently available devices and should therefore prove to be considerably more reliable over the life of the system in which it is used. Reliability is further enhanced by its reduced power consumption and lower resultant operating temperature rise.

The very fast (3 ns) rise time analog output directly drives a 75Ω coaxial cable and monitor with a 1 Vp-p signal. No additional amplifiers are required. Output transitions exhibit sufficiently low glitch that no further processing is required. Separate digital inputs for sync and blanking allow the AH8308E to produce EIA Standard RS170A and RS343A compatible composite video; these plus additional inputs for Reference White and 10% Overbright combine to provide a complete, highly flexible, improved performance video D/A converter subsystem in a 0.790" x 1.305" 24 pin dual-in-line package.

Theory of Operation

Eight bit digital data presented to the AH8308E on the data inputs is latched into the D flip-flops at the rising edge of the STROBE pulse applied to the STROBE control input. The outputs of the flip-flops, drive high speed switches that steer current into a summing network with an output impedance of 75Ω, developing a 1 Vp-p signal directly. Due to the extremely small differential delay among the eight data channels, the code switching output glitches are invisible even on the best video monitor.

Digital control inputs for REFERENCE WHITE, SYNC, BLANKING and 10% OVERBRIGHT are provided. A logic 0 on the REF. WHITE input sets the flip-flops and drives the output to −0.064V. Logic 0 on 10% OVERBRIGHT increases the output by 0.064V. Used in conjunction with REF. WHITE, the flip-flops are set and the output is driven to 0V. Logic 0 on the BLANKING and SYNC inputs resets the flip-flops and drives the output to −0.778V and −1.064V respectively. Combinations of BLANKING/SYNC and REF. WHITE/10% OVERBRIGHT should be avoided. While no damage will result, active levels on both the SET and RESET inputs of the D flip-flops will cause an indeterminate output. The condition of the SETUP line determines the relative levels between Reference Black and the Blanking level—left open, the standard 71 mV (10 IRE units) is produced; tied to −5.0V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units) is produced. (See Chart on last page).

Please refer to the Timing Diagram, Applications Considerations and Video System Display Application sections for examples of operation.

ENGINEER'S NOTEBOOK

Power Supply Requirements

The AH8308E is capable of operating from a single supply voltage between −4.75V and −5.5V. The output amplitudes specified are nominal values based on a −5.0V supply and will change in direct proportion to the supply voltage.

The unit can be powered from a +5.0V positive supply voltage if +5.0V is connected to the GROUND pin(s) and digital return is connected to the −5.0V pin. Under these conditions, the composite video signal will vary from +3.935V to +5.0V, and THE CASE WILL BE AT A +5.0V POTENTIAL.

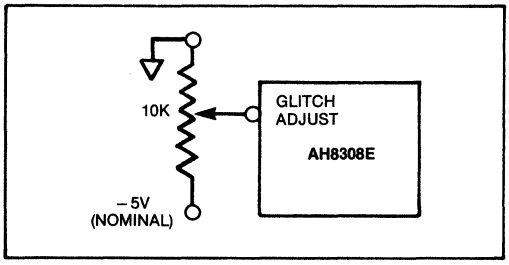


Figure 2. Glitch Adjust

The glitch area will vary as a function of the supply voltage. The factory trim is normally carried out at –5.0V, and may be done at another voltage if specified when ordering.

If other than –5.0V is used with a unit trimmed for –5.0V operation, provisions should be made on the PC board for a 10 kΩ potentiometer connected to the GLITCH ADJUST terminal as shown (in Figure 2). The pot should be adjusted to reduce the glitch area to a minimum.

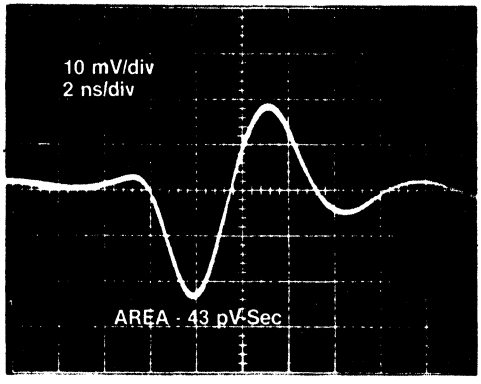


Figure 3. Glitch Area at Major Code Transition.

Grounding

There are six ground pins all tied together internally and to the case of the AH8308E.

ECL Terminators

ECL terminators are not included in the AH8308E. If the source of the video data and control inputs is more than a few inches away from these units, ECL terminators should be connected in close proximity to the inputs of the DAC.

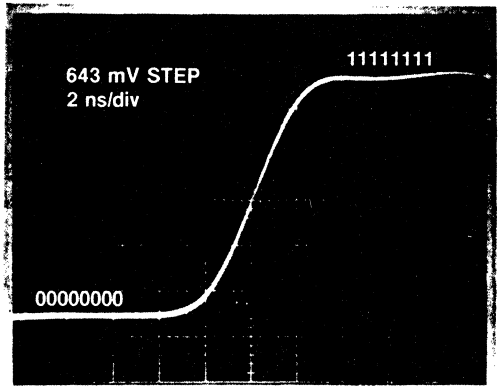


Figure 4. Full Scale Step Rise Time.

Current Output

The AH8308E can be used as a current output device by connecting the inverting input of an op-amp to the AH8308E output and then selecting the appropriate op amp feedback resistor for the required voltage output.

Timing

Figure 5 shows a detailed diagram depicting the timing required to generate composite video for the case of a full-scale (black to white) transition. 10% OVERBRIGHT, BLANKING PEDESTAL and SYNC are generated after the transition to illustrate their timing.

Cursor

To produce a cursor on a display, both 10% OVERBRIGHT and REF. WHITE should be brought to a logic "0" which will drive the output to 0V. If 10% OVERBRIGHT only is brought to logic "0", the output of the AH8308E will increase +0.064V above its prior output.

APPLICATION CONSIDERATIONS

Color Graphic Systems

The AH8308E is ideally suited for both monochrome composite video and RGB color applications. Normally only one channel (the green) carries the SYNC signal. For use in the other channels of such systems, the SYNC and BLANKING lines of the AH8308E can be disabled by tying them to logic "1".

While using a 4- or 5-bit DAC on each color channel may give the display system designer an acceptable color palette, the low resolution of these DACs may not be sufficient to allow anti-aliasing techniques to be employed successfully. One advantage to using an 8-bit DAC may not be readily apparent — one that is especially important in CAD/CAM type applications where single lines are drawn on the display. When a diagonal line is drawn on the screen, "bunching" of the pixels causes a stair-stepping effect as opposed to a smooth, straight line. Increased display resolution helps to reduce the size of the "jaggies" and smooth out the line, but cannot eliminate them. Various digital-differential analysis (DDA) procedures have been used to attempt to solve this problem and minimize its effect. By using a higher Z-axis resolution (8 bits versus 4 or 5), further improvements in the smoothing process are realized with these DDA procedures due to the increased control over the line intensity.

Broadcast Usage

The AH3808E is normally used in Digital Display applications. It can, however, be used for broadcast applications in which case additional circuitry is required in order to achieve full compliance with EIA Industrial Electronics Tentative Standard No. 1 (part of RS170A). This Standard details the exact waveform and timing characteristics of the broadcast composite video signal. The additional circuitry would, at a minimum, provide sinx/x correction and bandwidth filtering. In addition, the set-up on the AH8308E should be changed to 7.5 IRE units by placing a nominal 560Ω resistor between the SETUP terminal and ground.

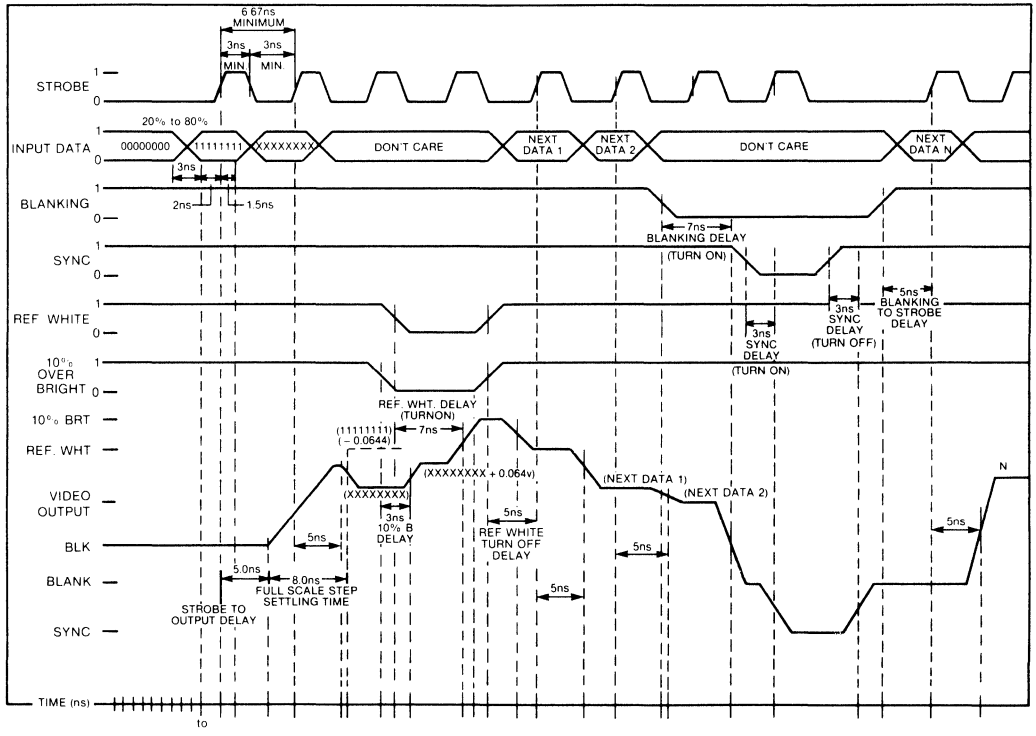


Figure 5. Typical Timing Diagram.

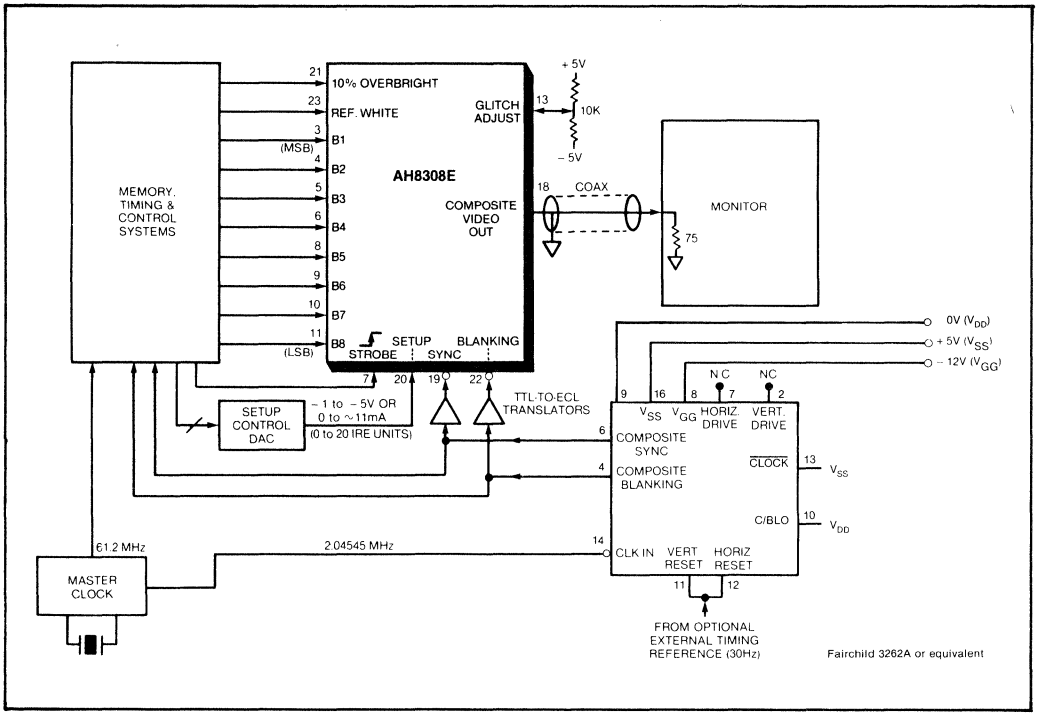


Figure 6. Typical AH8308E Application.

Video Display System Application

An example of a video display subsystem using the AH8308E is shown in block diagram form in Figure 6. Only the portion of the subsystem directly involving the AH8308E is shown. The memory and monitor circuits are not discussed in any detail, since system requirements vary. It is assumed that eight bits of digital data are available from some source for use by the AH8308E and that a monitor and/or sinx/x filter is being driven by the AH8308E. If fewer than eight bits are used, tie the unused LSBs to logic 0. Any AH8308E control signals not required in a particular system application should be tied to logic 1 to prevent erroneous operation. The timing relationships of the various signals are shown in Figure 5.

Timing for the overall display subsystem is derived from the system Master Clock. Through a suitable divider chain, a frequency of either 2.04 MHz is generated and applied to the clock input of the 3262A Sync Generator IC or equivalent (see Note*). From this clock signal, the 3262A generates the Sync and Blanking signals. The Composite Sync and Blanking Signals are applied to the corresponding control inputs on the AH8308E after first passing through TTL to ECL translators (all 3262A outputs are TTL). The Sync and Blanking signals are also sent to the Memory System for use by the Memory Address logic if required. The 3262A also produces a timing signal which is valid during the Vertical Interval at the start of the odd Field for interlaced systems. This signal may be used to control Memory addressing.

In most systems the "setup" level is left at one particular value such as the Standard 71 mV. In rare cases where the application requires, the setup level can be controlled digitally by means of a DAC with either a current or voltage output. If the SETUP pin is driven as a voltage point, values from −1 to −5V will produce 0 to 20 IRE units respectively. If a current is injected into the SETUP pin, approximately 11 mA is needed to produce 0 IRE units.

The composite video output from the AH8308E is connected directly to the (75Ω-terminated) video input of the monitor by a length of coax cable. The length of the cable should be limited to prevent the dc resistance of the cable run from exceeding 7.5Ω. If an amplifier is used between the AH8308E output and the monitor, longer lengths of cable can be allowed.

***PLEASE NOTE**

Comparable IC's providing similar functions to the 3262A are available from several manufacturers. The Fairchild part number 3262A is used by way of example, and no endorsement by Analogic of this part is intended or implied. Also, Analogic is not responsible for the accuracy of technical information supplied by other manufacturers.

The Video Signal

The EIA Standards RS170 and RS343 define the video signal in detail and refer to the IRE units for measuring the various components of the signal. The total peak amplitude of the standard video signal, from the maximum white level to the sync level is 140 IRE units. The standards further define the video signal as 1 Vp-p; therefore, 1 IRE unit is 7.14 mV. The maximum white level is the most positive amplitude of the video signal, and sync the most negative; this is referred to as a black-negative (as opposed to a black-positive) video signal. The illustration in Figure 7 depicts the composite video signal produced by the AH8308E.

The AH8308E provides a 10% Overbright feature which causes a negative shift in all of the various levels (i.e. Reference White, Reference Black, Blanking and Sync) by approximately 9 IRE units. The relative number of IRE units between each of these levels is compatible with the EIA Standards. As the definitions are given for the various levels in the AH8308E composite signal, it should be remembered that they differ from the standard RS170/RS343 absolute levels by 9 IRE units (0.064V).

The most positive amplitude level is the 10% Overbright. As its name implies, this level is higher than the whitest level of the picture information by 10% of the signal or 0.064V (10% of 0.643V). This level is most often used to define a cursor on a display screen. By making the cursor 10% brighter than the remainder of the picture, it can be located easily. REFERENCE WHITE is the most positive amplitude of the normal picture information, while REFERENCE BLACK is the most negative. The span of signal from REFERENCE WHITE to REFERENCE BLACK is 90 IRE units or 0.643V. This span is divided into 256 discrete levels (gray scale) because of the 8-bit resolution of the AH8308E.

The BLANKING LEVEL is 10 IRE units below REFERENCE BLACK in a standard video signal and is the voltage level that will completely cut off the display screen. The AH8308E provides a means of varying the relative distance between the REFERENCE BLACK and BLANKING LEVEL, referred to as the setup. The SETUP pin on the AH8308E can be programmed to provide a set-up of 0 mV., 71 mV or 142 mV (0 IRE, 10 IRE or 20 IRE units). Left open, the standard setup of 71 mV (10 IRE units) is produced. Tied to – 5V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units) is produced. The BLANKING LEVEL is also referred to as the PEDESTAL, BACK PORCH or FRONT PORCH.

(continued)

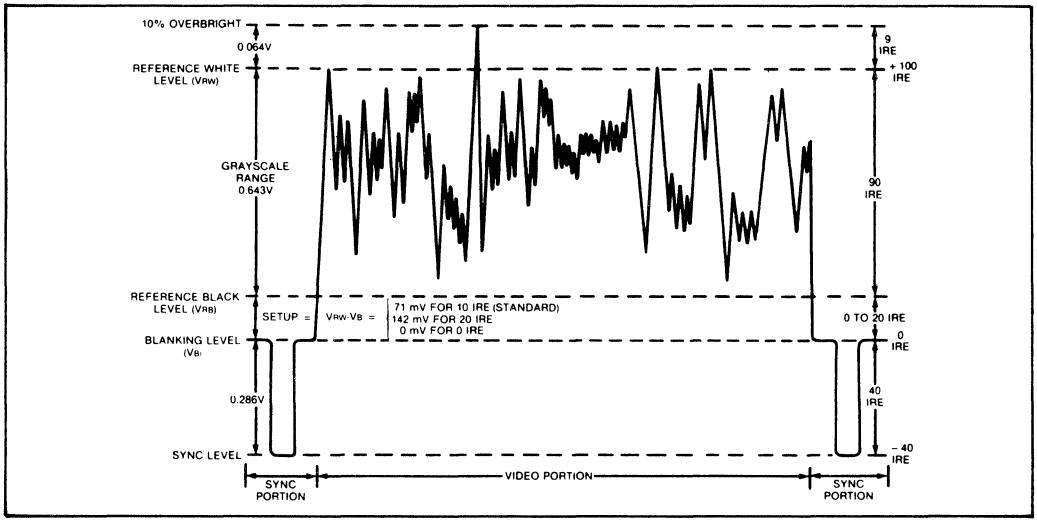


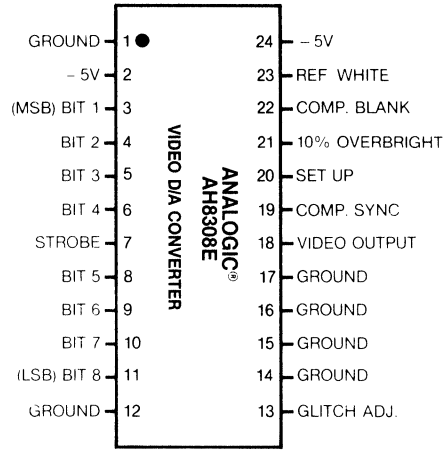
Figure 7. The Composite Video Signal (Not to Scale).

The Video Signal (cont.)

The most negative amplitude of video signal is the SYNC LEVEL at −40 IRE (0.286V) below the BLANKING LEVEL. Relative to 10% OVERBRIGHT, this level is −1.064V. The SYNC level is used to synchronize the scanning circuits in the display system. It is this sync level (along with BLANKING) produced directly by the AH8308E that provides the composite video signal.

All of the above definitions apply to both monochrome and color (RED/BLUE/GREEN) display systems. In color systems, the composite signal is produced on only one channel (usually the green). The other two DACs producing the Red and Blue video have the Sync and Blanking levels disabled by tying them to logic 1.

PINOUT

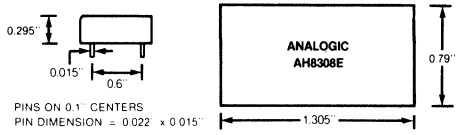


(TOP VIEW)

Available Options

The AH8308E is normally supplied with eight DATA INPUTS, STROBE, REFERENCE WHITE, 10% OVERBRIGHT, BLANKING and SYNC control inputs, capable of driving a 75 ohm terminated monitor. We invite inquiries on modifications such as dual monitor capability, REFERENCE BLACK CONTROL and other custom requirements.

MECHANICAL



CONTROL SIGNALS

SIGNAL	ACTIVE LOGIC LEVEL	RESULTANT OUTPUT
DATA, BIT 1—BIT 8	000 000 00	−0.707V (REF. BLK)
	111 111 11	−0.064V (REF. WHT)
STROBE	↓	DATA LOADED
REF. WHITE	0	−0.064V
COMP. BLANK	0	−0.778V
10% OVERBRIGHT	0	0V
COMP. SYNC	0	−1.064V
SETUP	OPEN	71 mV (10 IRE)
	−5.0V	−142 mV (20 IRE)
	GND	0 mV (0 IRE)

ORDERING GUIDE

150 MHz 8-Bit ECL Video DAC...

Specify **AH8308E**

ANALOGIC

AH8308T

8-Bit Composite Video D/A Converter

Description

The AH8308T is a complete 8-bit composite video D/A converter subsystem intended for use in monochromatic and color Digital Display Systems. Unlike other devices which require external power-hungry TTL to ECL level translators, the AH8308T accepts 8-bit digital video data plus sync and blanking commands directly from a TTL source and produces a composite video output that drives into a 75Ω load at an update rate as high as 65 MHz*.

The 1.15 watt maximum power dissipation of the AH8308T is significantly lower than its competition; other devices typically require as much as 1.7 watts just for the video DAC (plus another 300 plus milliwatts for the external level translators for a total of over 2.0 watts!).

The single chip design of the AH8308T means far fewer internal wire bonds than other presently available devices and a considerable improvement in reliability over the life of the system in which it is used. Reliability is further enhanced by its reduced power dissipation and lower resultant operating temperature rise.

The analog output, which has a typical full scale settling time of 7.5 ns, will directly drive a 75Ω coaxial cable and monitor with a 1 Vp-p signal. No additional amplifiers are required. Output transitions exhibit sufficiently low glitch that no further processing is required. Because these parts, as well as TTL to ECL level translators are not required, the AH8308T provides savings in PC board area, parts count and product cost.

Separate inputs for sync and blanking allow the AH8308T to produce EIA standards RS170A and RS343A compatible composite video; these plus additional inputs for Reference White and 10% Overbright combine to provide a complete, highly flexible, low power, improved performance video D/A converter subsystem in a 0.78″ x 1.30″ x 0.3″, 24 pin dual-in-line package.

*A 150 MHz ECL video D/A Converter, the AH8308E, is also available. Please consult the factory for technical/applications information.

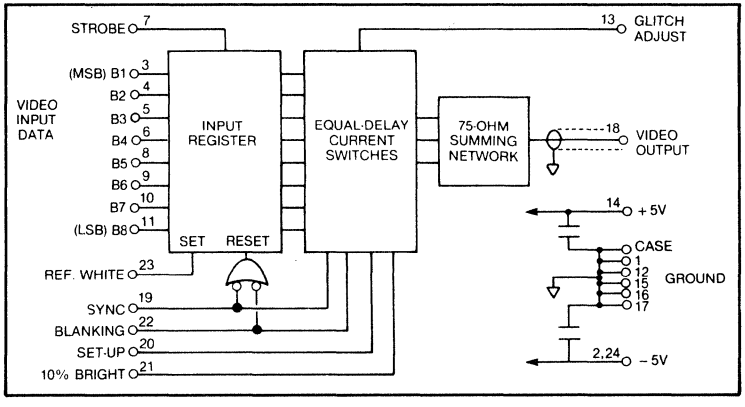


Figure 1. AH8308T Functional Block Diagram.

Features

- **Lower Power - 1.15 watt maximum**
  Extends reliability over other devices
- **Complete TTL input Video D/A Subsystem**
  Requires no external level translators
- **Up to 65 MHz Update Rate**
  Extends display system capabilities
- **"Glitch-free" Performance**
  Simplifies display system design
- **Direct Drive to 75Ω Coaxial Cable/Monitor**
  Requires no additional circuitry
- **Composite Sync and Blanking Control Inputs**
  Directly produces RS170A/RS343A compatible output
- **10% Overbright Control Input**
  Provides simple cursor generation
- **Standard 0.78″ x 1.305″ x 0.3″ Package Size**
  Reduces pc board area requirements

Applications

- **CAD/CAM Display Systems**
- **Medical Imaging Systems**
- **"Quick Look" Display Systems**
- **Image Processing Systems**
- **Workstations**
- **Monochrome or Color Display Systems**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

Output Voltage Range Composite
0V to −1.064V; ±3% of Full Scale into 75Ω termination

Gray Scale
−0.064V to −0.707V; ±3% of Gray Scale into 75Ω termination

Recommended Load Impedance
75Ω ±5%, dc to 50 MHz

Source (Thevenin) Impedance
75Ω ±5%, dc to 50 MHz

LSB Size
2.5 mV, nominal

Rise and Fall Time
3 ns, typical, 4 ns maximum (10% to 90%)

Full Step Settling Time
7.5 ns typical to 1 LSB (0.4%)

Glitch Settling Time
3 ns to <1 LSB for worst MSB transition

Glitch Area
35 pV-s typical, 70 pV-s max.

Compliance Voltage
+1.1V to −1.1V typical

Cable Drive Capacity
75Ω characteristic impedance

To avoid appreciable signal loss, total length should have no more than 7.5Ω dc resistance

Composite Sync Level
−1.064V with Standard Setup
−0.286V (−40 IRE Units) with respect to blanking level (back porch)

Composite Blanking Level
−0.778V, with Standard Setup

10% Overbright Level
0V

TRANSFER CHARACTERISTICS

Resolution
8 Bits, 256 Gray Scale Levels
2.5 mV per step, nominal

Coding
Binary

Reference White Level
11111111 produces −0.064V absolute; +0.714V (100 IRE Units) relative to blanking level with Standard Set-up; +0.643V relative to Reference Black

Reference Black Level
00000000 produces −0.707V absolute; +0.071V (10 IRE Units) relative to blanking level with Standard Set-up

Differential Linearity
± ½ LSB maximum

Monotonicity
Guaranteed

Offset (dc output with 10% Overbright Actuated)
± ½ LSB maximum, 0°C to +55°C

Transfer Gain (Slope) Tempco
±0.1% FSR/°C maximum

Propagation Delay
7 ns Typical, Strobe to output 50% points

Control Input Speed
(Sync, Blanking, Ref. White and 10% Overbright)
10 ns Typical to settle to 10% of final value (Refer to Timing Diagram)

INPUT CHARACTERISTICS

Logic Levels (all inputs)
Standard TTL Levels
LOGIC 1 ≥ 2.4V
LOGIC 2 ≤ 0.4V

Loading
Data and Strobe
2 unit load

Control Inputs
<2 unit load

Data
8 TTL compatible inputs

Validity
Data must be valid 2.0 ns min., prior to Strobe and remain valid for 1.5 ns after data Strobed

Update Rate
65 MHz maximum

Strobe Input
Data entered on positive-going edge (Timing Reference)

Pulse width
5 ns minimum

Rise and Fall Time (all inputs)
≤10 ns (10% to 90%)

Setup (Reference Black to Blanking)
Input open: Standard 71 mV (10 IRE Units)
Input to −5.0V: 142 mV (20 IRE Units)
Input to Ground: 0 mV (0 IRE Units)

Composite Sync Level
Logic "0" on Sync (and Blanking) input simultaneously resets input register to 00000000 and drives output to −1.064V

Composite Blanking Level
Logic "0" on Blanking input simultaneously resets input register and drives the output to −0.778V

Reference White Level
Logic "0" on Ref. White input simultaneously sets input register to 11111111 and drives output to −0.064V

10% Overbright Level
Logic "0" on input raises output level by 0.064V. Logic "0" on Ref. White and 10% Overbright drives output to 0V.

Glitch Adjust
Input Impedance
7.5 KΩ

Control Characteristics
50 pV-s/V applied to Glitch Adjust pin

POWER SUPPLY REQUIREMENTS

Power Dissipation
0.95 watts typical, 1.15 watt maximum

Power Supply Required
+5.0V, +5% @ 30 mA max. 50 mV p-p ripple max.
−5.0 V @ 200 mA maximum 5 mV p-p ripple max.
(−4.75 V to −5.5V operating range)

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range (Ambient)
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to +40°C

Mechanical Dimensions
0.78" X 1.30" X 0.3"
(20.07 X 33.14 X 7.82 mm)

24-pin double DIP

Shielding
Steel foil

Theory of Operation

Eight bit TTL digital data presented to the AH8308T on the data inputs is latched into the input register at the rising edge of the STROBE pulse applied to the STROBE control input. The outputs of the register drive high speed switches that steer current into a summing network with an output impedance of 75Ω, developing a 1 Vp-p signal directly. Due to the extremely small differential delay among the eight data channels, the code switching output glitches are invisible even on the best video monitor.

Digital control inputs for REFERENCE WHITE, SYNC, BLANKING and 10% OVERBRIGHT are provided. A logic 0 on the REF. WHITE inputs sets the registers and drives the output to −0.064V. Logic 0 on 10% OVERBRIGHT increases the output by 0.064V. Used in conjunction with REF. WHITE, all registers are set and the output is driven to 0V. Logic 0 on the BLANKING and SYNC (plus BLANKING) inputs resets the registers and drives the output to −0.778V and −1.064V respectively. Combinations of BLANKING/SYNC and REF. WHITE/10% OVERBRIGHT should be avoided. While no damage will result, active levels on both control lines may cause an indeterminate output.

The condition of the SETUP line determines the relative levels between Reference Black and the Blanking level — left open, the standard 71 mV (10 IRE units) is produced; tied to −5.0V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units) is produced. (See Chart on last page).

Please refer to the Timing Diagram, Applications Considerations and Video System Display Application sections for examples of operation.

ENGINEER'S NOTEBOOK

Power Supply Requirements

The AH8308T requires both +5V ±5% and −5V (−4.75V to −5.5V operating range) power supplies. The output amplitudes specified are nominal values based on a −5.0V supply and will change in direct proportion to the −5V supply voltage.

The glitch area will also vary as a function of the −5V supply voltage. The factory trim is normally carried out at −5.0V and may be done at another voltage if specified when ordering.

If other than −5.0V is used with a unit trimmed for −5.0V operation, provisions should be made on the PC board for a 10 KΩ potentiometer connected to the GLITCH ADJUST terminal as shown (in Figure 2). The pot should be adjusted to reduce the glitch area to a minimum.

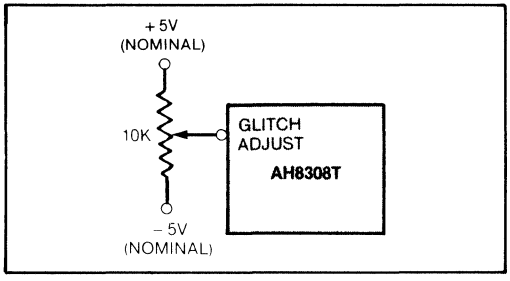


Figure 2. Glitch Adjust.

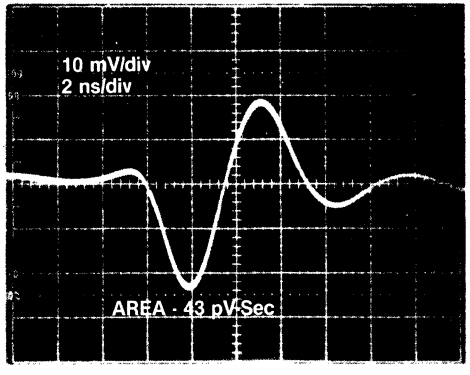


Figure 3. Glitch Area at Major Code Transition.

Grounding

There are five ground pins all tied together internally and to the case of the AH8308T.

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The AH8308T can be used as a current output device by connecting the inverting input of an op-amp to the AH8308T output and then selecting the appropriate op-amp feedback resistor for the voltage output required by the application.

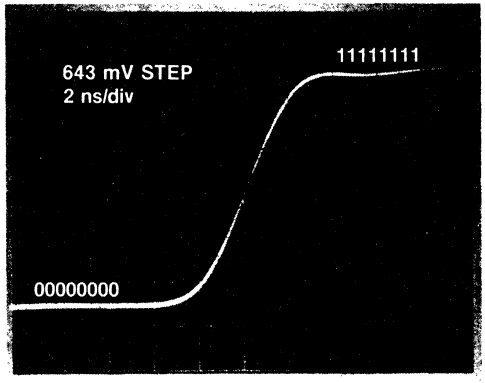

Figure 4. Full Scale Step Rise Time.

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Cursor

To produce a cursor on a display, both 10% OVERBRIGHT and REF. WHITE should be brought to a logic "0" which will drive the output to 0V. If 10% OVERBRIGHT only is brought to logic "0", the output of the AH8308T will increase +0.064V above its prior output.

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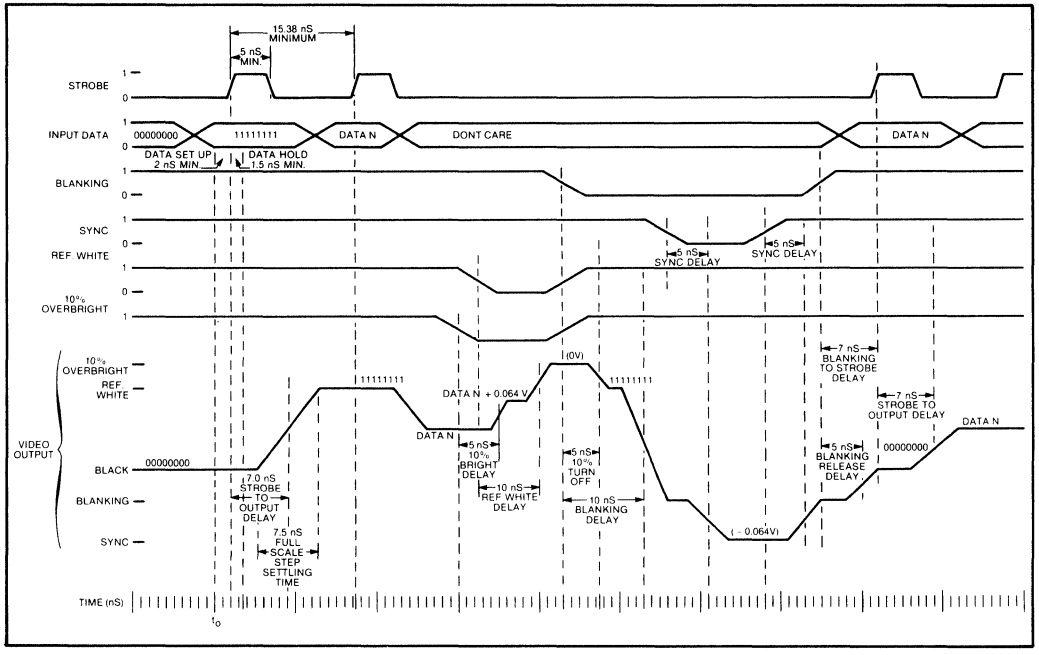

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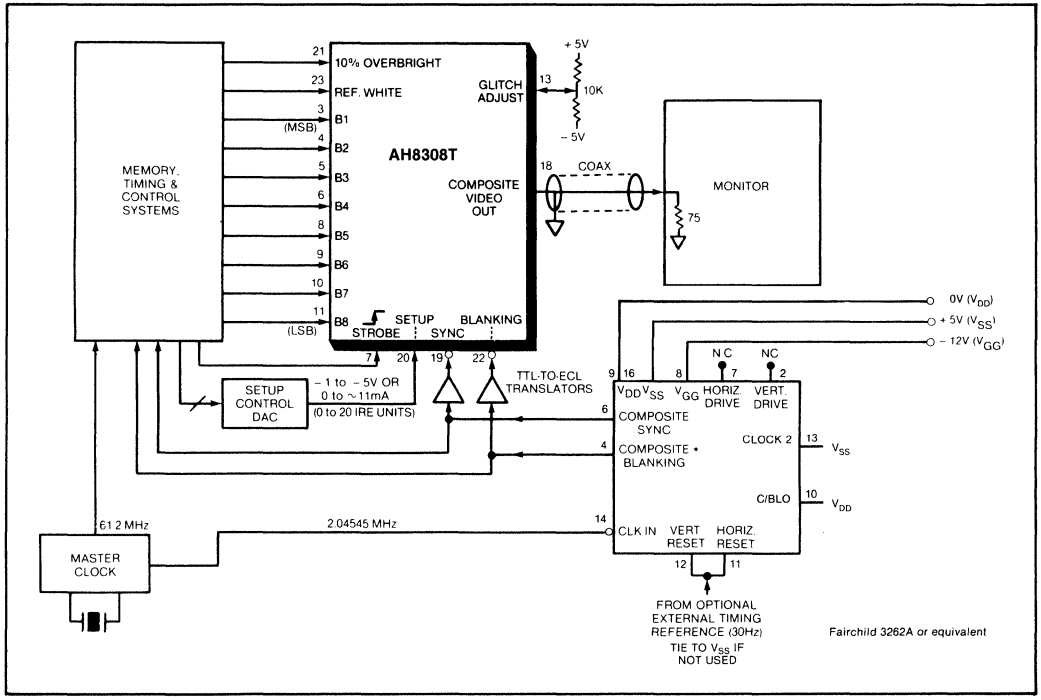

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***PLEASE NOTE**

Comparable IC's providing similar functions to the 3262A are available from several manufacturers. The Fairchild part number 3262A is used by way of example, and no endorsement by Analogic of this part is intended or implied. Also, Analogic is not responsible for the accuracy of technical information supplied by other manufacturers.

The composite video output from the AH8308T is connected directly to the (75 Ω-terminated) video input of the monitor by a length of a coax cable. The length of the cable should be limited to prevent the dc resistance of the cable run from exceeding 7.5Ω. This is necessary to limit the amount the signal is attenuated by the cable to approximately 10% or less. If an amplifier is used between the AH8308T output and the monitor, longer lengths of cable can be allowed.

The Video Signal

The EIA Standards RS170A and RS343A define the video signal in detail and refer to the IRE units for measuring the various components of the signal. The total peak amplitude of the standard video signal, from the maximum white level to the sync level is 140 IRE units. The standards further define the video signal as 1 Vp-p; therefore, 1 IRE unit is 7.14 mV. The maximum white level is the most positive amplitude of the video signal, the sync the most negative; this is referred to as a black-negative (as opposed to a black-positive) video signal. The illustration in Figure 7 depicts the composite video signal produced by the AH8308T.

Because the output of the AH8308T must accommodate 10% Overbright control, Reference White, Reference Black, Blanking and Sync are shifted from their standard absolute levels by approximately -9 IRE units. The relative number of IRE units between each of these levels is compatible with the EIA Standards. As the definitions are given for the various levels in the AH8308T composite signal, it should be remembered that they differ from the standard RS170/RS343 absolute levels by 9 IRE units (0.064V).

The most positive amplitude level is the 10% Overbright. As the name applies, this level is higher than the whitest level of the picture information by 10% of the gray scale or 0.064V (10% of 0.643V). This level is most often used to define a cursor on a display screen. By making the cursor 10% brighter than the remainder of the picture, it can be located easily. REFERENCE WHITE is the most positive amplitude of the normal picture information, while REFERENCE BLACK is the most negative. The span of signal from REFERENCE WHITE to REFERENCE BLACK is 90 IRE units of

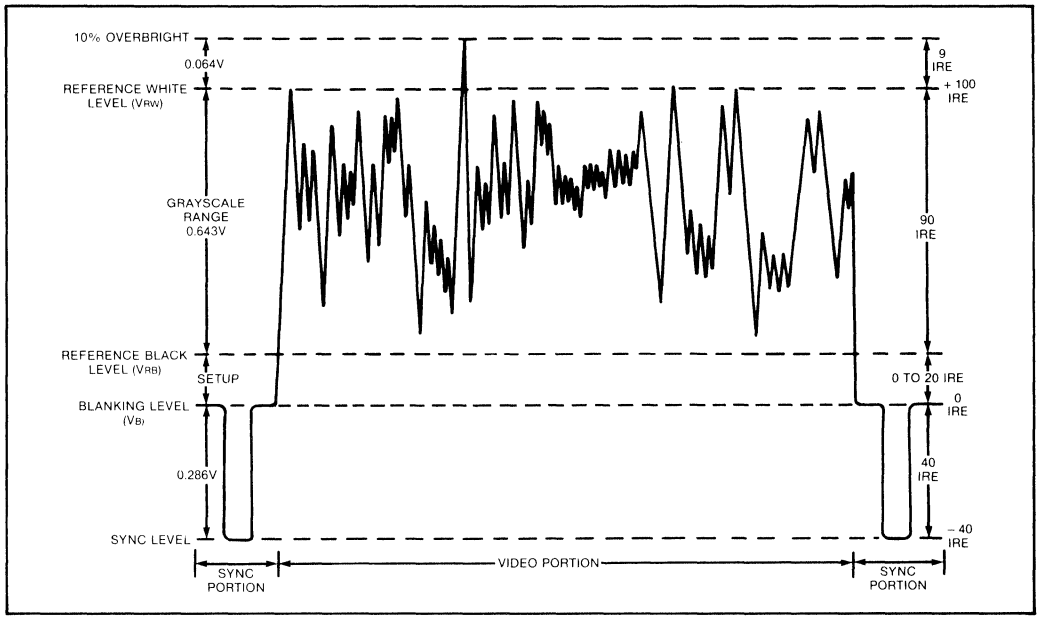


Figure 7. The Composite Video Signal (Not to Scale).

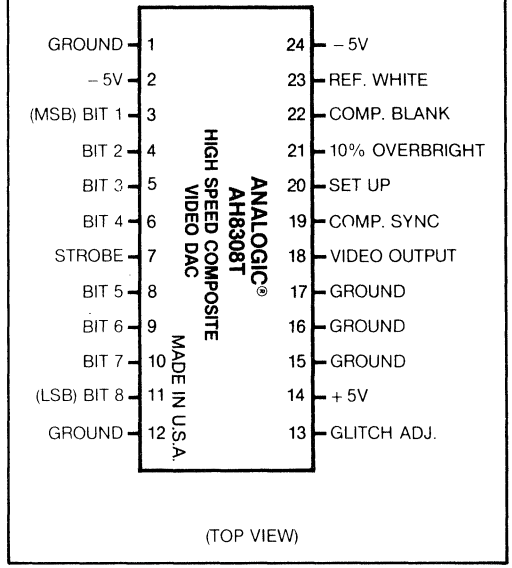
0.643V. This span is divided into 256 discrete levels (gray scale) due to the 8-bit resolution of the AH8308T.

The BLANKING LEVEL is 10 IRE units below REFERENCE BLACK in a standard video signal and is the voltage level that will completely cut off the display screen. The AH8308T provides a means of varying the relative distance between the REFERENCE BLACK and BLANKING LEVEL, referred to as the setup. The SETUP pin on the AH8308T can be programmed to provide a set-up of 0 mV., 71 mV or 142 mV (0 IRE, 10 IRE or 20 IRE units). Left open, the standard setup of 71 mV (10 IRE units) is produced; tied to – 5V, 142 mV (20 IRE units) is produced; tied to ground, 0 mV (0 IRE units is produced. The BLANKING LEVEL is also referred to as the PEDESTAL, BACK PORCH or FRONT PORCH.

The most negative amplitude of video signal is the SYNC level at – 40 IRE (0.286V) below the BLANKING LEVEL. Relative to 10% OVERBRIGHT, this level is – 1.064V. The SYNC level is used to synchronize the scanning circuits in the display system. It is this SYNC level (along with BLANKING) produced directly by the AH8308T that provides the composite video signal.

All of the above definitions apply to both monochrome and color (RED/GREEN/BLUE) display systems. In color systems, the composite signal is produced on only one channel (usually the green). The other two DACs producing Red and Blue video have the SYNC and BLANKING lines disabled by tying them to logic 1.

PINOUT

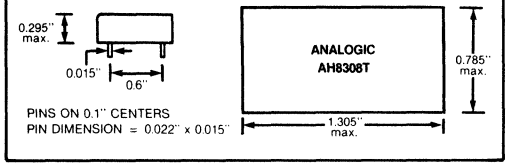


(TOP VIEW)

Available Options

The AH8308T is normally supplied with eight DATA INPUTS, STROBE, REFERENCE WHITE, 10% OVERBRIGHT, BLANKING and SYNC control inputs, capable of driving a 75Ω terminated monitor. We invite inquiries on modifications such as dual monitor capability, REFERENCE BLACK CONTROL and other custom requirements.

MECHANICAL



CONTROL SIGNALS

SIGNAL	ACTIVE LOGIC LEVEL	RESULTANT OUTPUT
DATA, BIT 1—BIT 8	000 000 00 111 111 11	– 0.707V (REF. BLK) – 0.064V (REF. WHT)
STROBE	↓	DATA LOADED
REF. WHITE	0	– 0.064V
COMP. BLANK	0	– 0.778V
10% OVERBRIGHT	0	Vout + 0.064V
10% + REF. WHITE	0	0V
COMP. SYNC	0	– 1.064V
SETUP	OPEN – 5.0V GND	71 mV (10 IRE) – 142 mV (20 IRE) 0 mV (0 IRE)

ORDERING GUIDE

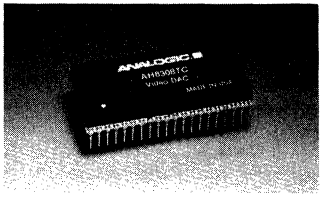
65 MHz 8-Bit TTL Video DAC...

Specify **AH8308T**

150 MHz 8-Bit ECL Video DAC

(Please consult factory or representative for Data Sheet)

Specify **AH3808E**



ANALOGIC

AH8308TC

8-Bit RGB Video D/A Converter

Description

The **AH8308TC** is a third generation triple (RGB) 8-bit video DAC that provides designers of color display systems with a complete, self-contained, TTL-compatible RGB composite video subsystem in a 40-pin DIP. The **AH8308TC** features an advanced design that provides low power (3.0W maximum), high reliability, and low cost. The small size of the **AH8308TC** reduces the PC board area by 30% or more, and the power dissipation by up to 25% over the equivalent function implemented with single channel DACs.

Each of three video DACs within the **AH8308TC** accepts independent 8-bit TTL data at an update rate of up to 100 MHz. Controls are provided for common Blanking and Strobe, and Sync (GREEN channel only). Blanking is synchronous with Strobe when activated, and asynchronous when deactivated. The video output of each channel is RS330/343 compatible, providing a 75Ω source impedance and a 1V p-p output signal.

The **AH8308TC** is a cost-effective solution to the requirement for a triple 8-bit composite video DAC in applications ranging from engineering workstations to CAD/CAM systems, medical imaging, and other high-end graphics systems.

Features

- **Three 8-bit Video DACs in one 40-pin DIP**
- **100 MHz Data Update Rate**
- **TTL Compatible**
- **Synchronous Blanking**
- **RS330/RS343 Composite Video Output Compatible**
- **Low Power Dissipation 2.5W**

Applications

- **Color Graphic Workstations**
- **CAD/CAM Systems**
- **Medical Imaging Systems**
- **"Quick Look" Display Systems**
- **Image Processing Systems**

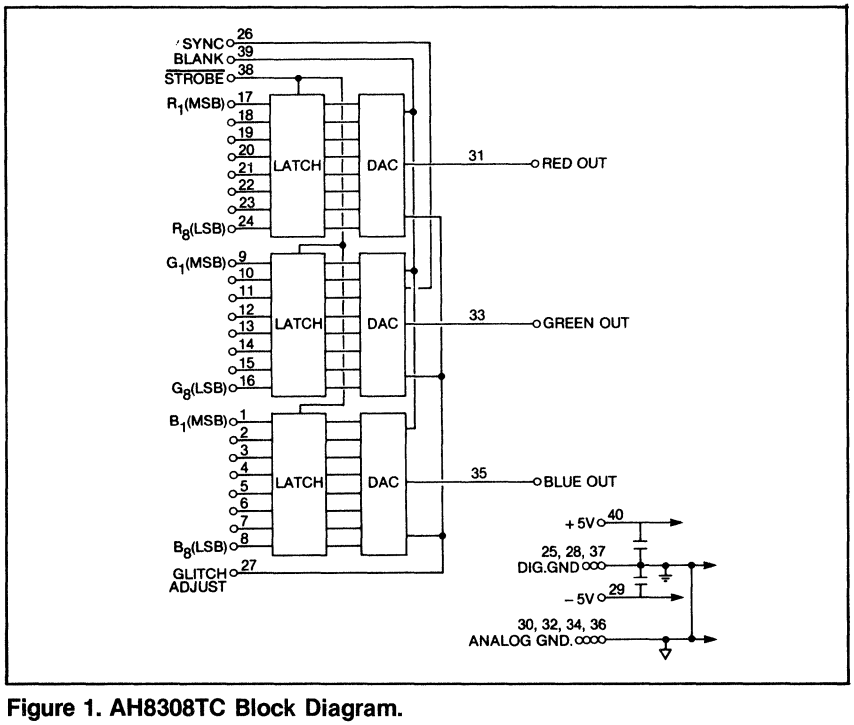


Figure 1. AH8308TC Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted.)

OUTPUT CHARACTERISTICS (Each Channel)

Composite Output (GREEN Channel only)
0V to −1.00V, ±3% of full scale into 75Ω termination

Gray Scale Output (all Channels)
0V to −0.643V, ±3% of Gray Scale into 75Ω termination

Recommended Load Impedance
75Ω, ±5%; dc to 50 MHz

Source (Thevenin) Impedance
75Ω, ±5%; dc to 50 MHz

LSB Size
2.5 mV, nominal

Rise and Fall Time
3 ns typical, 4 ns maximum; 10% to 90%

Full Step Settling Time
7.5 ns typical to 1 LSB (0.4%)

Glitch Settling Time
5 ns to <1 LSB for worst-case transition

Glitch Area
80 pV • s typical

Cable Drive Capacity
75Ω characteristic impedance; to avoid appreciable signal loss total length should have no more than 7.5Ω dc resistance

Composite Sync Level (GREEN Channel only)
−1.00V absolute, −0.286V (−40 IRE Units) relative to Blanking level

Composite Blanking Level
−0.714V

TRANSFER CHARACTERISTICS (Each Channel)

Resolution
8 bits, 256 Gray Scale levels; 2.5 mV per step, nominal

Coding
Binary

Reference White Level
1111 1111 produces 0V absolute; +0.714V (100 IRE Units) relative to Blanking level

Reference Black Level
0000 0000 produces −0.643V absolute; +0.071V (10 IRE Units) relative to Blanking level

Differential Linearity
± ½ LSB maximum

Monotonicity
Guaranteed

Offset (Output with 1111 1111 Input)
± ½ LSB maximum, 0°C to +55°C

Propagation Delay
7 ns typical, strobe to output; 50% points

BLANKING Input Speed
7 ns typical, 10 ns maximum to settle to 10% of final value after strobe high-to-low transition

SYNC Input Speed
7 ns typical, 10 ns maximum to settle to 10% of final value

Channel-to-Channel Crosstalk
½ LSB maximum, dc component
100 pV • s maximum, ac component

INPUT CHARACTERISTICS (Each Channel)

Logic Levels (all inputs)
Standard TTL levels
Logic 0 = 0V to 0.4V
Logic 1 = 2.4V to 5.0V

Loading:
Data and Strobe
2 unit load
Control Inputs
<2 unit load

Data:
Validity
Data must be valid 2.0 ns prior to Strobe and remain valid for 1.5 ns after data Strobe

Update Rate
100 MHz maximum

COMMON CONTROL INPUTS

Strobe Input
Data entered on negative-going edge (Timing Reference) simultaneously on all three channels

Skew
5 ns maximum variation between channels for data latched into input registers

Pulse Width
5.0 ns minimum

Rise and Fall Time
<10 ns (10% to 90%)

Composite Blanking
Logic 1 on Blanking input simultaneously resets all input registers to 0000 0000 and drives all channel outputs to −0.714V. Blanking is synchronous with falling edge of next STROBE pulse; after logic 1 to 0 transition, all channel outputs remain at the Blanking level until the next STROBE pulse, at which time data present at DAC inputs is loaded into the DAC.

Composite Sync
Logic 1 on SYNC input (after BLANKING is activated) drives the GREEN channel output further negative to −1.00V. SYNC must not be activated without BLANKING first being active. When SYNC is released (returned to logic 0), all channel outputs remain at the Blanking level until the next STROBE pulse, at which time data present at DAC inputs is loaded into the DACs (assuming BLANKING control is inactive).

Glitch Adjust:
Input Impedance
7.5 kΩ
Control Characteristics
75 pV • s/V applied to Glitch Adjust pin

POWER SUPPLY REQUIREMENTS

+5V, ±5%
100 mA maximum; 50 mV p-p ripple maximum
−5.0V
500 mA maximum; 5 mV p-p ripple maximum
(−4.75V to −5.5V operating range)
Power Dissipation
2.5W typical, 3.0W maximum

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C
Storage Temperature
−25°C to +100°C
Relative Humidity
0 to 85%, noncondensing up to +40°C
Mechanical Dimensions
2.0" x 1.0" x 0.3"; 40-pin triple width DIP

OPERATION

Each of the three DAC inputs is presented with an 8-bit data word corresponding to the intensity required for each CRT electron gun. After allowing for the data setup time, a high-to-low transition on the STROBE input causes the three 8-bit data words to be latched into the DACs. After the DAC propagation delay, each video output produces a voltage corresponding to the data loaded in its DAC.

During the blanking interval, the BLANKING control line is activated by a logic 1. At the next STROBE pulse, the three DAC input registers are reset to 0000 0000 and the DAC outputs are driven to the blanking level.

When BLANKING (and SYNC) are deactivated at the end of the retrace interval, all three DAC outputs remain at the blanking level until the next STROBE pulse. Then data at the DAC inputs are latched into their respective input registers and subsequently appear at the DAC outputs after the DAC propagation delay.

USING THE AH8308TC

Power Supply Requirements

The **AH8308TC** requires both +5V and −5V power supplies. The specified output amplitudes are nominal values based on a −5.0V supply and change in direct proportion to the −5.0V supply voltage.

The glitch area also varies as a function of the −5V supply voltage. The factory trim is normally carried out at −5.0V and may be done at another voltage if specified when ordering.

If other than −5.0V is used with a unit (measured directly at pin 29) trimmed for −5.0V operation, provisions should be made on the PC board for a 10 kΩ potentiometer connected to the GLITCH ADJUST pin (pin 27) as shown in Figure 2. The pot should be adjusted to reduce the glitch area to a minimum.

Grounding

There are seven (7) ground pins tied together internally via the ground plane. To reduce ground loops, each ground pin should be used for the function for which it is labelled.

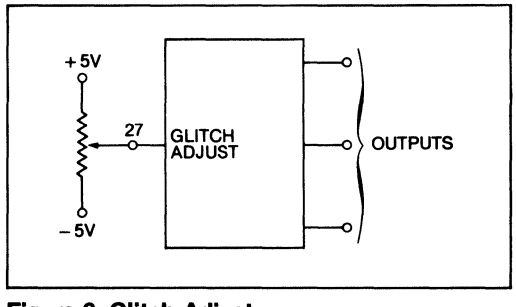
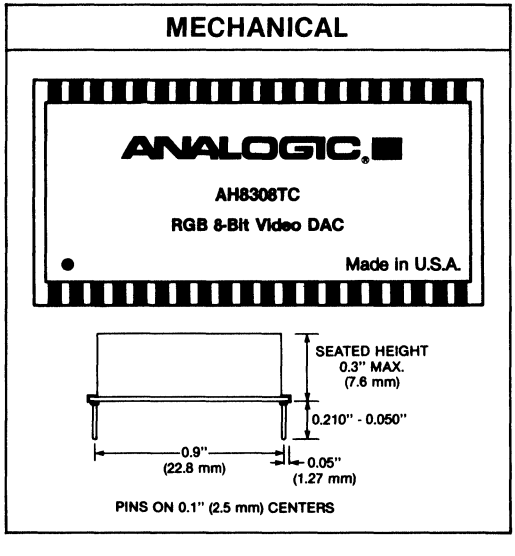


Figure 2. Glitch Adjust



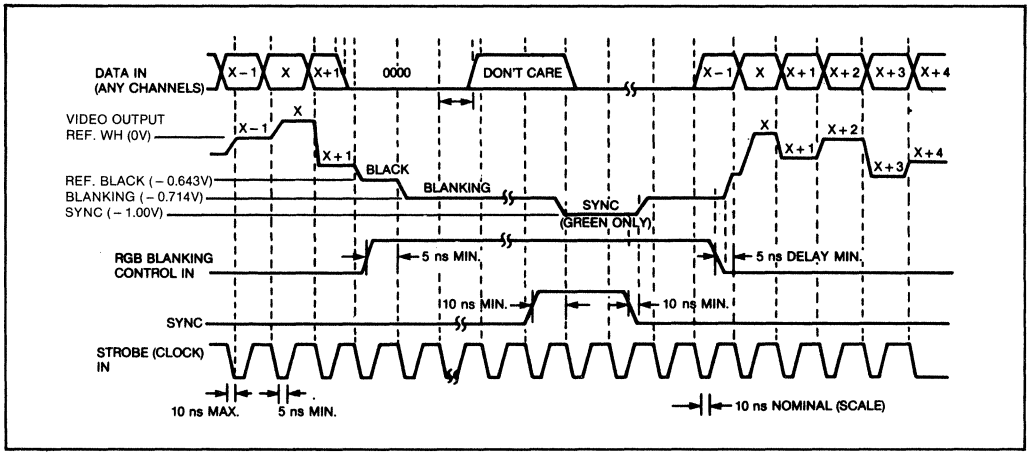


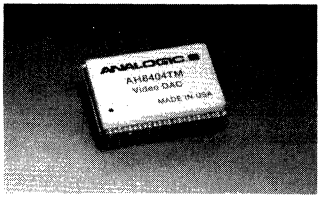
Figure 3. AH8308TC Typical Timing Diagram.

PINOUT

B1 (MSB)	1	40	+5V
B2	2	39	Blanking
B3	3	38	$\overline{\text{Strobe}}$
B4	4	37	Digital Ground
B5	5	36	Analog Ground (Blue)
B6	6	35	Blue Ana Output
B7	7	34	Analog Ground (Green)
B8	8	33	Green Ana Output
G1 (MSB)	9	32	Analog Ground (Red)
G2	10	31	Red Ana Output
G3	11	30	Analog Ground
G4	12	29	-5V
G5	13	28	Digital Ground
G6	14	27	Glitch Adjust
G7	15	26	Sync
G8	16	25	Digital Ground
R1 (MSB)	17	24	R8(LSB)
R2	18	23	R7
R3	19	22	R6
R4	20	21	R5

ORDERING GUIDE

100 MHz, RGB 8-bit video DAC
Specify **AH8308TC**



ANALOGIC®

AH8404TM/TC

Triple 4-Bit Video D/A Converter

Description

The **AH8404s** are a significant advance in video D/A converters that provide designers of low-to-medium-cost personal computer-based color display systems with a complete, self-contained, TTL compatible, composite video subsystem in a 24-pin DIP. The advanced design of the **AH8404s** provides low, 0.8W power dissipation from a single +5V supply, including color look-up table memory! Offered as either an RGB 4-bit D/A only, or with the integral color look-up table memory, both configurations of the **AH8404s** provide high reliability, small size, and low cost.

The **AH8404TM** color-mapped video D/A converter is designed for the color graphic system where space is at a premium. Both the functions of triple (RGB) video D/A converter and color look-up table memory are provided within a single package. Data can be written into the internal 32 word RAM (one for each color channel) such that 32 colors can be defined out of a possible 4096 at any given time. During the display (Read) interval, any of these 32 colors can be addressed from a 5-bit bus. Separate Sync, Blanking (synchronous) and D/A Strobe control inputs are provided.

The **AH8404TC** D/A converter only is offered for those systems where a different configuration of look-up table memory is required. The D/A accepts 4-bit TTL data at an update rate of up to 25 MHz for each D/A. Common synchronous Blanking, Strobe, and Sync (Green Channel only) controls are provided. The output of each channel is RS330/343 compatible, providing a 75Ω source impedance and 1 Vp-p output signal.

Features

- **Available with and without color look-up table**
  AH8404TC 25 MHz D/A
  AH8404TM 20 MHz D/A with 32 word memory
- **TTL compatible**
- **Synchronous Blanking**
- **4096 color palette**
- **RS330/RS343 compatible composite video output**
- **Low Power Dissipation**
  0.8W maximum for D/A and memory
  0.6W maximum for D/A only
- **24-pin DIP**

Applications

- **Color graphic workstations**
- **Personal Computers**
- **Low-end CAD/CAM Systems**

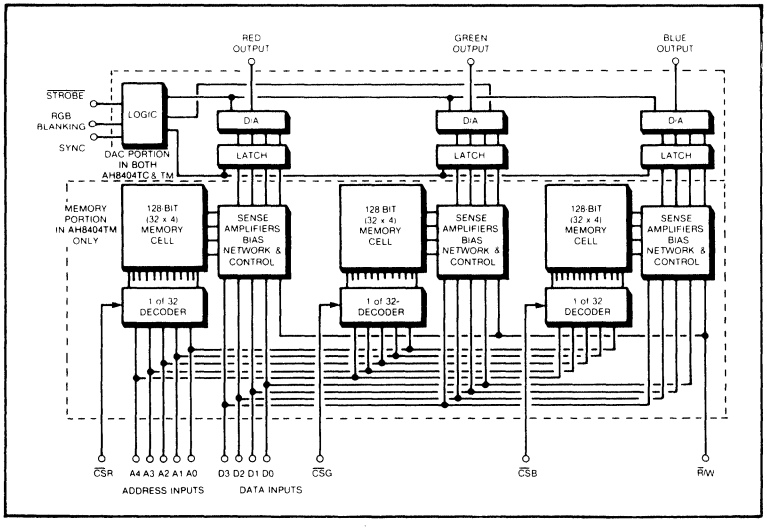


Figure 1. AH8404TM/TC Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

OUTPUT CHARACTERISTICS (Each Channel)

Composite Output (Green Channel Only)
0.00V to 1.000V, ±3% of Full Scale (assumes load is 75Ω, ±5% and +5.0V power supply voltage; measured at load)

Gray Scale Output
0.357V to 1.000V, ±3% of Full Scale (assumes load is 75Ω ±0.5%, and +5.0V power supply voltage; measured at load)

Recommended Load Impedance
75Ω, ±5%; dc to 25 MHz

Source (Thevenin) Impedance
75Ω, ±3%; dc to 25 MHz

LSB Size
42.9 mV nominal

Full Scale Step Settling Time
20 ns typical, 30 ns maximum to 1/2 LSB after propagation delay

Glitch
Total Glitch Energy less than 300 pV•s at major code transition (0111 to 1000 or vice versa)

Cable Drive Capability
75Ω characteristic impedance; to avoid appreciable signal losses total length should have no more than 7.5Ω dc resistance

RGB Blanking Level
0.286V with 71 mV (10 IRE Unit) set-up

Sync Level
0.000V; offset is 2 mV maximum, from 0°C to +55°C

TRANSFER CHARACTERISTICS (Each Channel)

Resolution
4 bits, 16 Gray Scale levels; 42.9 mV per step

Reference White Level
1111 produces 1.000V, 100 IRE Units relative to Blanking level

Reference Black Level
0000 produces 0.357V, 10 IRE Units relative to Blanking level

Differential Nonlinearity
±1/2 LSB, maximum

Monotonicity
Guaranteed

Transfer Gain (Slope) Tempco
±0.1% FSR/°C

RGB Blanking Input Delay
60 ns typical to 10% of final value.

Sync Input Delay
60 ns typical to 10% of final value

INPUT CHARACTERISTICS

Logic Levels (all inputs)
Standard TTL levels
Logic 1 >2.4V
Logic 0 <0.4V

Loading:
Data and Strobe
2 Unit Load
Control Inputs
2 Unit Load
Address (TM Only)
2 Unit Load

Coding
Binary
Address Coding (TM Only)
Binary

Data Update Rate
25.0 MHz maximum (TC), 20.0 MHz maximum (TM)

Memory Size (TM Only)
32 word by 4-bit (each RAM/channel)

Control Inputs

DAC Strobe
Data entered into all three DAC channels simultaneously on negative-going edge

Rise and Fall Time
<10 ns (10% to 90%)

DAC Propagation Delay
60 ns maximum, STROBE to output 10% point

Blanking Rise and Fall Time
<10 ns (10% to 90%)

RGB Blanking
Logic 1 on RGB Blanking input resets all DACs to 0000 at next STROBE pulse and drives the outputs of all channels to 0.286V

Sync
Logic 1 on RGB Blanking and Sync inputs resets all DAC inputs to 0000, drives the RED and BLUE outputs to 0.286V and GREEN output to 0.000V, −0.286V (−40 IRE Units) relative to Blanking level

LOOK-UP TABLE MEMORY CONTROL (AH8404TM)

Read/Write
Logic 0 selects Read operation; logic 1 selects Write operation. DAC outputs retain previous Read value until STROBE input is applied; STROBE applied during Write operation causes Reference Black output level from all DACs

Address — 5 bits (A0 to A4)
Determines location in memory for Read or Write operation; used as Address input to load RAM arrays in Write mode and as Look-up inputs in Read (Display) mode

Data — 4 bits (D0 to D3)
Data to be loaded into RAM array(s) by CHIP SELECT input(s) during Write operation

Chip Select — CSR, CSG, CSB
CHIP SELECT for each channel (RED, GREEN, and BLUE); logic 0 selects RAM channel for Read or Write operation; when disabled, RAM data output is all 0's to DAC inputs. DAC output of deselected channels retain last Read level if no

STROBE is applied; otherwise output falls to Reference Black level. Normally only one input at a time is enabled (selected) to write data to its corresponding RAM. All inputs are enabled to read data during display. These may be held at logic 0 throughout the read cycle

DYNAMIC CHARACTERISTICS

Data Setup Time
30 ns minimum (TM), 0 ns min. (TC)

Data Hold Time
20 ns minimum (TM), 30 ns min. (TC)

Width of Write Pulse
25 ns minimum

Address Before Write
30 ns minimum

Address Hold Time
20 ns minimum

Address Access Time (after valid address)
48 ns maximum

Chip Select Access
40 ns maximum

Chip Select Disable
35 ns maximum

POWER REQUIREMENTS

+5.0V, ±5%
120 mA maximum (TC); 160 mA maximum (TM), 50 mV p-p ripple maximum

Power Dissipation
0.5W typical; 0.6W maximum (TC)
0.6W typical; 0.8W maximum (TM)

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C ambient

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, noncondensing up to 40°C

Dimensions
1.00" x 1.30" x 0.3"maximum
(25 x 33 x 7 mm)
24-pin triple width DIP

Packaging
Ceramic lid epoxied to substrate

Handling
CMOS precautions required

Operation

The **AH8404TM** consists of two major functional blocks (1) a memory organized as three 32-word by 4-bit blocks, one for each color channel, with common data, Read/Write control and address inputs, separate chip select inputs and data outputs, and (2) a triple 4-bit D/A converter with common Sync, Blanking, and Strobe control inputs. Data flow is always from the output of the memory to the input of the D/A converter.

During a Write operation, data for the look-up table RAM is presented to the DATA inputs. The CHIP SELECT line is brought low to enable the color channel RAM that is to receive the data. The READ/WRITE line is pulsed, and the data is written into the RAM location defined by the five ADDRESS inputs. The CHIP SELECT line is then brought high to disable that channel. The process can be repeated for other addresses and/or color channels.

During a Read (display) cycle, all three CHIP SELECT lines are brought low to enable all channels, and the RAM address for the color to be displayed is presented to the ADDRESS inputs. After a 48 ns maximum propagation delay through the memory, the data from the addressed RAM location appears at the output of the memory. The D/A STROBE line is then pulsed to latch the data into the D/A input register. After a propagation delay through the D/A converter, the corresponding analog output voltages appear at the three D/A outputs.

The **AH8404TC** D/A only (and the D/A portion of the **AH8404TM**) accepts a 4-bit data word for each of the three video channels (RED, GREEN, and BLUE). The data is presented to the DATA inputs and held for the duration of the setup time. The STROBE is then pulsed to load the data into the three DAC registers. During the blanking interval, the BLANKING control line is activated by a logic 1. The next STROBE pulse resets the three input registers to 0000 and drives the D/A outputs to the blanking level. When the SYNC line is activated, the next STROBE pulse drives the GREEN channel output to the sync level. At the end of the blanking/sync interval, the SYNC and BLANKING controls are released (returned to a logic 0). At the next STROBE to the D/A, the data at the DATA inputs to the D/A are loaded into the input registers and subsequently appear at the D/A outputs after the D/A propagation delay.

ORDERING GUIDE

20 MHz, RGB 4-bit D/A with 32-word look-up table memory.....Specify **AH8404TM**

25 MHz, RGB 4-bit D/A.....Specify **AH8404TC**

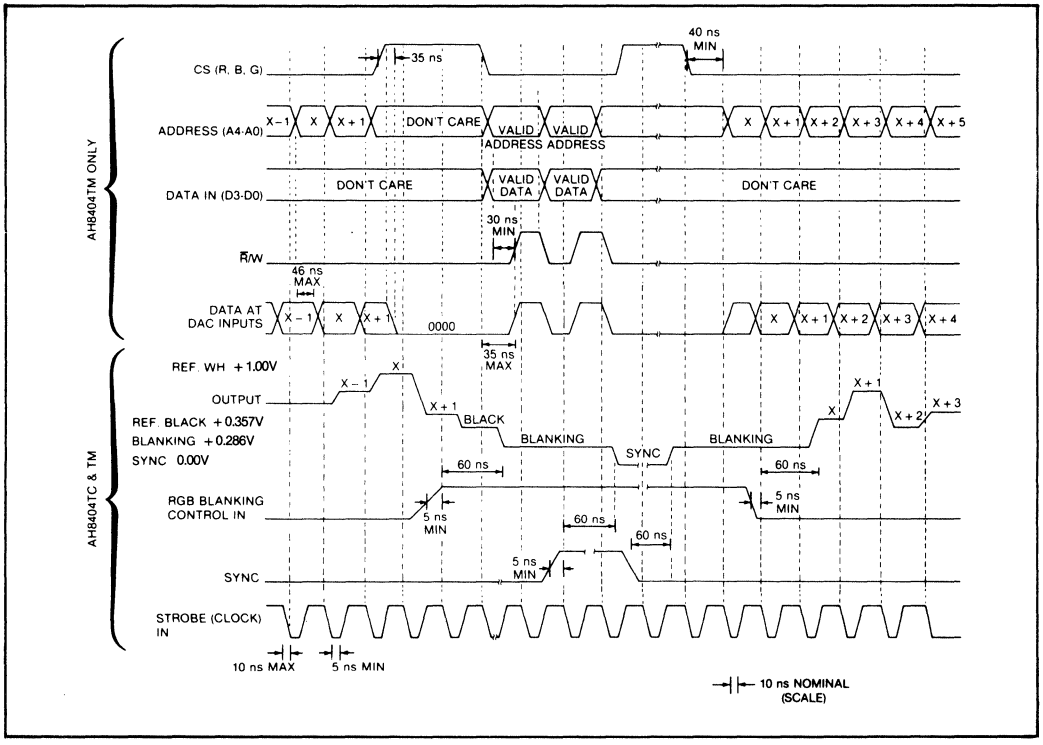
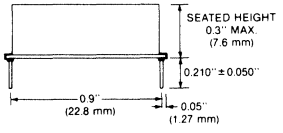


Figure 2. Typical Timing AH8404TM/TC.

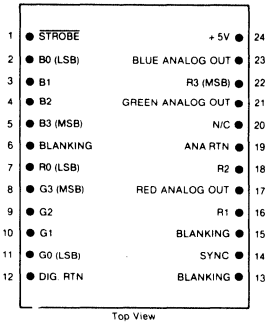
MECHANICAL



PINS ON 0.1" (2.5 mm) CENTERS

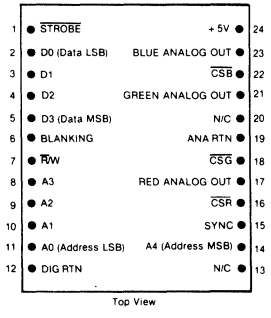
PINOUT

AH8404TC

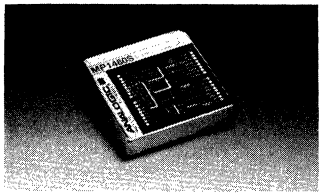


Top View

AH8404TM



Top View



ANALOGIC®

MP1480S

High Performance, 12-Bit, Current Loop D/A Converter

Description

The Analogic MP1480S is a unique 12-bit digital-to-analog current loop converter incorporating a proprietary Analogic current valve. It consists of an input register, a high-accuracy digital-to-analog converter (DAC), followed by a voltage-to-current loop conversion circuit (Fig. 1). Together, these building blocks act as a digitally-controlled current valve, for standard 4 to 20 mA or other customer-selectable current ranges. For maximum flexibility, the MP1480S offers a choice of computer-compatible CMOS or low-power Schottky input registers and the option of voltage output. This high speed, accurate and versatile current transmitter has been specifically designed for application in industrial process control systems and satisfies the Instrument Society of American Standard ISA-S50.1, "Compatibility of Analog Signals for Industrial Process Control".

Features

- User-Selectable Current Loop or Voltage Output
- Current Range: 4 to 20 mA Standard; ranges from 0 to 50 mA available
- ISA Type 4 Transmitter, Class L and Class U Operation
- Built-in Digital Latching Register
- Overvoltage and Open-Circuit Protection in Current Loop
- Short-Circuit Protection in Voltage Output
- 12-Bit Resolution
- Multiplying Capability in Two Quadrants
- High Accuracy and Linearity: 0.021% FSR
- Settling Time: 10 μs to ½ LSB
- Choice of LS TTL or CMOS Inputs
- Choice of BINARY or BCD coding
- Low Profile: Metal Case

Applications

- Industrial Control Systems
- Remote Data Acquisition Systems
- Instrumentation Systems
- Computer-Controlled Current Sources
- Automatic Relay Testing

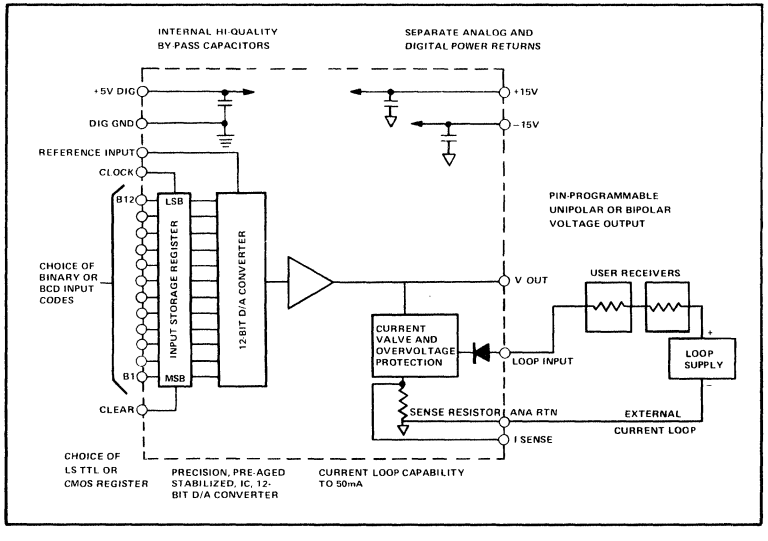


Figure 1. MP1480S Current Loop D/A Converter Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG OUTPUTS

Current loop or voltage — programmable by customer.
Current Mode — ISA type 4, non-isolated transmitter, Class L operation with > + 12 Vdc loop supply; Class U operation with > + 20 Vdc loop supply. See Note 1
Voltage Mode — Unipolar; 0 to + 5V or 0 to + 10V; Bipolar: ± 5V or ± 10V; programmable by customer. See Note 2.

ACCURACY (@ + 25°C)

Resolution
12 bits

Relative Accuracy
0.012% FSR (0.05% for BCD)

Noise (10 Hz to 100 kHz)
Current Mode — <2 μA rms
Voltage Mode — <0.01% FSR rms

OUTPUT CHARACTERISTICS

Output Impedance
Current Mode — Current Source
Voltage Mode — <0.3Ω @ dc

Load Current
Current Mode - See Note 1
Voltage Mode — 5 mA.
Short circuit Ilmit = 20 mA

Receiver Voltage
Current Mode — 6V min., 33V max. See Note 1

Output Protection
Current Mode — Protected against 120 Vac @ 60 Hz. Open-circuit protected

STABILITY

Offset Drift
Current Mode — 0.6 μA/°C
Voltage Mode — 10 ppm//°C max.

Gain Drift
Current Mode — 1.0 μA/°C
Voltage Mode — 20 ppm/°C max.

Supply Sensitivity
10 ppm FSR/% change in supply voltage

DIGITAL INPUTS

Logic Compatibility
Standard CMOS logic levels (C Version)
Low Power Schottky TTL (T Version)

Data Set-up Time
10 ns, minimum

Clock
Positive-edge triggered

Clear
Active low, asynchronous with clock

SPEED

Settling time to ½ LSB
10 μs, max. to ½ LSB; 0.5 μs to 10%

Slew Rate
Current Mode — 2 mA/μs, min.
Voltage Mode — 2V/μs, min.

REFERENCE VOLTAGE INPUT

Input Impedance
20 kΩ ± 10% and 0.01 μF

Voltage
Current Mode — + 2.5V and − 1.25V See Note 3
Voltage Mode — + 10V

MULTIPLYING MODE PERFORMANCE

Quadrants
2

Accuracy V.REF (+ 1 to + 10V)
0.1%

Reference Feedthrough at 1 kHz
< ½ LSB

Output Slew Rate Referred to Reference
Current Mode — 1 mA/μs
Voltage Mode — 2V/μs

Output Settling Time from Reference
10 μs to stated accuracy

MONOTONICITY

Guaranteed over full range

POWER SUPPLY REQUIREMENT

± 15 Vdc ± 3%
25 mA

+ 5 Vdc ± 5%
25 mA

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to + 70°C

Storage Temperature
− 55° to + 150°C

Mechanical Dimensions
2 x 2 x 0.39 inches (50.8 x 50.8 x 9.9 mm)

Shielding
EMI: 5 sides, RFI: 6 sides

PURCHASE OPTIONS

Input Register
Low Power Schottky or CMOS

Input Code
Binary or 3-decade BCD

Note 1: The MP1480A output does not "generate" current, but acts as a valve for an externally applied series voltage and "receiver" load. A standard 4-20 mA current is thus accepted independent of supply variation, transmission line resistance or induced noise. Inputs to the unit, at the current loop terminals, must be within the 6-33V range. These terminals are protected against voltages in excess of 33V by an HV Protect circuit.

Note 2: Voltage mode and current mode cannot be used simultaneously.

Note 3: In the current mode, the +9.95V reference sets the span of current at 16 mA and the −4.975V sets the baseline at 4 mA, giving a range of 4 to 20 mA. The range may be modified slightly by adjusting the reference voltage values. To alter the span, the value of the sense resistor must be changed.

Applications Concepts

When analog signals are sent over lines characterized by unpredictable impedance and induced noise, controlled current sources often provide the most reliable transmission. The MP1480S acts as a digitally controlled valve operating in series with the customer's remote current receiver and voltage source. The unit accepts a level of current determined solely by the 12-bit digital input command and thus enables microprocessors or other digital sources to communicate with standard analog loops, including the popular 4 to 20 mA type.

OPERATION

Current Loop Mode

The standard current range available in the MP1480S is 4-20 mA. Apply supply voltages and the +9.95V and −4.975V reference voltages to obtain the desired control current. A 3-terminal voltage reference and op amp circuit are recommended for the reference voltages. Make jumper connections as shown in Fig. 2. Select a current loop supply voltage, V_S, such that the difference between V_S and the voltage drop across the external loop resistance, R_L, lies in the range 6-32V. The relationship between V_S and R_L is given by,

$$(20R_L + 6) \leq V_S \leq (4R_L + 32)$$

where, R_L is in K-ohms.

It can be seen from this relationship that the maximum permitted theoretical value of R_L is 1.625 kΩ. The MP1480S is protected against output terminal voltages up to 120 Vac. Operation outside the 6 to 32V range will not be within specifications. See Note 3, under Specifications, for other current ranges.

Unipolar and Bipolar Output Voltage Modes

Determine output range required. Apply supply voltages and +10V reference voltage and make jumper connections(s) as shown in Fig. 3.

CMOS Operation (MP1480S-C)

Make jumper connection between the TTL/CMOS control pin and +V.DIG. terminal and connect +V.DIG. to the CMOS supply voltage (+5V to +15V).

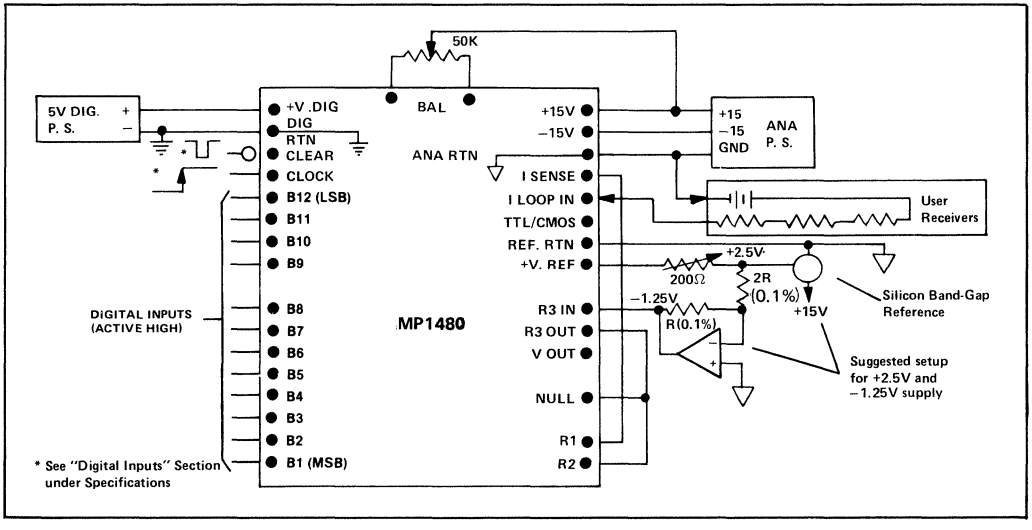


Figure 2. MP1480S Current Output Connections and Zero and Gain Adjustments.

TTL Operation (MP1480S-T)

No external connection is required at the TTL/CMOS terminal for this mode of operation.

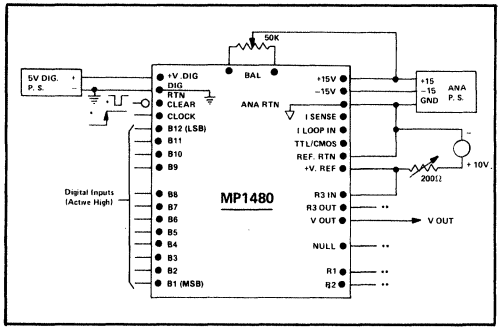


Figure 3. MP1480S Voltage Output Connections and Zero and Gain Adjustments.

NOTES ON VOLTAGE OUTPUT CONNECTIONS:

1. For Bipolar outputs, connect R3 OUT to NULL.
2. For 0 to +5V, connect R2 to NULL.
3. For 0 to +5V, 0 to +10V and ±5V ranges, connect R1 to V.OUT
4. For ±10V, connect R2 to V.OUT

* See "Digital Inputs" Section under Specifications

** See Notes on Voltage Output Connections

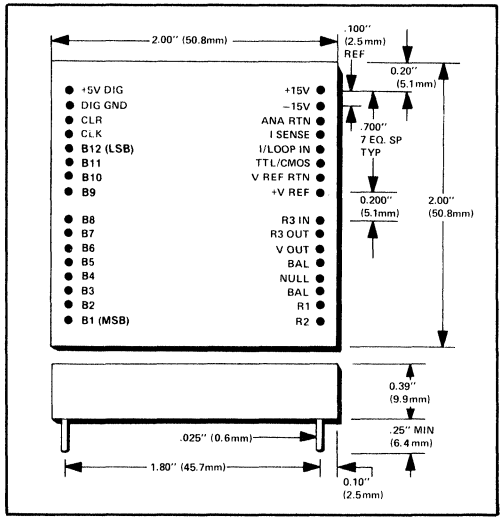


Figure 4. MP1480S Outline Drawing, Mounting Dimensions and Terminal Identifications.

CALIBRATION

Current Loop Mode

Make the connections shown in Fig. 2. Connect an external supply with a voltage on the order of +15V to the current loop terminals in series with a current-limiting resistor of 47 to 100Ω and a milliammeter. Set the digital input code to zero (grounding the CLEAR terminal will accomplish this) and adjust the 50 kΩ trimpot for a reading of 4 mA. Set the input code to maximum as listed in Table 1 (all 1's for binary or the code corresponding to 999 for BCD) and adjust the 200Ω trimpot for a reading of 20 mA. See Note 3, under Speccifications, for other current ranges.

Unipolar Voltage Mode

The MP1480S provides the system user with the capability of adjusting the converter to compensate for system zero offsets. Determine output range required. Make the connections shown in Fig. 3, including the desired Unipolar output connections listed under the Figure. Apply a "ZERO" input digital code (see Table 1) and adjust the 50 kΩ potentiometer for a zero voltage reading at V OUT. Set input code for maximum reading and adjust the 200Ω potentiometer for the proper output, as listed in Table 1.

Bipolar Voltage Mode

Determine output range required. Make the connections shown in Fig. 3, including the desired Bipolar output connections listed under the Figure. Apply a "ZERO" input code and adjust the 50 kΩ potentiometer for full negative value at V OUT. Apply a midscale input code, as listed in Table 1. Adjust 200Ω potentiometer for zero output at V OUT.

Output Current	Code	Digital Input	Full Scale Output Range 0-5V or ±5V	Full Scale Output Range 0-10V or ±10V
20 mA	Unipolar Binary	1111 1111 1111	+4.9988	+9.9976
4 mA	Unipolar Binary	0000 0000 0000	0.0000	0.0000
Not Used	Bipolar Offset Binary	1111 1111 1111	+4.9976	+9.9951
		1000 0000 0000	0.0000	0.0000
		0000 0000 0000	−5.0000	−10.0000
20 mA	Unipolar BCD	1001 1001 1001	+4.995	+9.990
4 mA	Unipolar BCD	0000 0000 0000	0.000	0.000
Not Used	Bipolar Offset BCD	1001 1001 1001	+4.990	+9.980
		0101 0000 0000	0.000	0.000
		0000 0000 0000	−5.000	−10.000

NOTE: Input of all zeros may be forced by grounding the CLEAR input terminal.

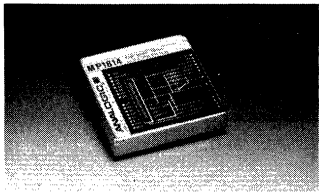
Table 1. MP1480S Digital Input Coding for Binary and BCD Inputs.

ORDERING GUIDE

Specify **MP1480S** — □ — □

Input Logic
- LS TTL — T
- CMOS — C

Input Code
- Binary — BIN
- BCD — BCD



ANALOGIC®

MP1814

High Performance General Purpose 14-Bit D/A Converter

Description

The Analogic MP1814 is a premium quality digital-to-analog converter which provides genuine 14-bit resolution, linearity, and stability. Every contributing element to the MP1814 Error Budget has been designed and engineered to provide a converter that meets the requirements for economical, high-speed, accurate, and stable 14-bit resolution in high-precision, wide-dynamic-range applications.

Performance Achievements

The MP1814 incorporates high-speed, thermal tracking, monolithic voltage switches; precise, ultra-stable, network resistors; and a reference source servoed to an aged, temperature-compensated precision reference Zener for accurate, stable operation over wide temperature ranges. The MP1814 also includes a high speed voltage amplifier that slews at 10V/μs and supports the throughput settling time of less than 15 μs for conversion to within $\pm$0.005% of a full 20V step.

The versatile MP1814 provides the user with pin-selectable full scale ranges of $\pm$10V, $\pm$5V, +10V and +5V analog outputs for computer-compatible binary or offset binary input data codes.

The MP1814 small size (2" x 2"), low profile (0.375"), metal case provides RFI and EMI shielding, and encloses a repairable assembly that includes high-quality power supply by-pass capacitors to prevent power supply transients from interfering with conversion performance.

Features

- **True 14-bit Accuracy and Linearity**
- **Maximum Interface Compatibility**
  Selectable $\pm$10V, $\pm$5V, +5V, +10V Output Voltage
  Positive True Logic Input Coding (TTL Compatible)
- **High Speed**
  15 μs max. to 0.005% of 20V step
- **Separate Digital and Analog Grounds**
  Up to 250 mV potential difference
- **Guaranteed Monotonicity**
  Differential Linearity with 0.003%
  Tempco of Differential Linearity 1 ppm/°C typ.
- **Low Profile**
  0.375" high metal shielding case

Applications

- **Wide Dynamic Range, Computer Controlled, Industrial Processes**
- **High Precision CRT Display Systems**
- **Automated Test Instrumentation**
- **Waveform Synthesis and Recovery**
- **High Resolution Information Translation Systems**
- **Programmable Control Instrumentation (Gain, Offset, etc.)**
- **High Resolution Oscillographic Recordings**

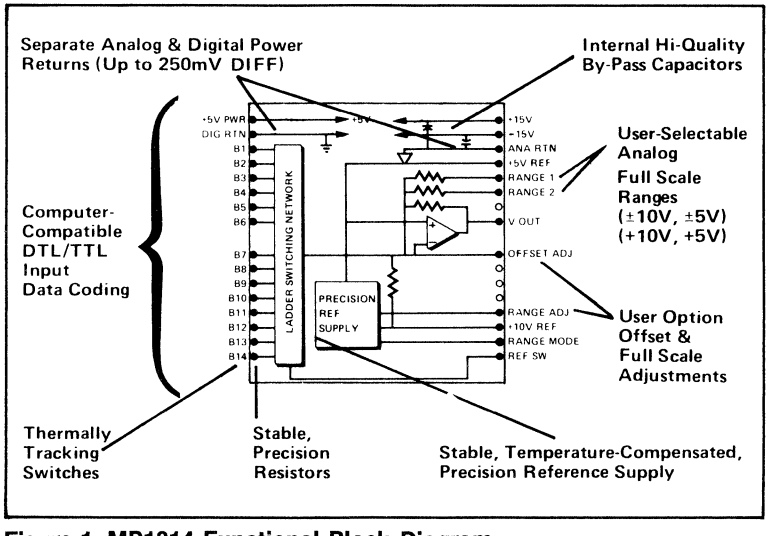


Figure 1. MP1814 Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

DIGITAL INPUTS

Number of Bits
14

Coding
Binary, Offset Binary Positive "TRUE" Logic

Compatibility
1 TTL/Bits 2-14; 2 TTL/MSB-1

ANALOG OUTPUT

Full Scale Ranges
±5V, ±10V, +5V, +10V

Impedance
<0.1Ω (dc)

Maximum Load
2 KΩ 1000 pF for rated settling time

INPUT REFERENCE OUTPUT

Voltage
+10V, +5V

Impedance
<0.1Ω

SPEED

Settling Time
10 μs typ., 15 μs max. for 20V step to 0.005%

Slew Rate
10 V/μs

ACCURACY

Absolute Accuracy
±0.006% FSR*

Linearity
± ½ LSB (±0.003% FSR)

Differential Linearity
± ½ LSB (±0.003% FSR)

Zero Offset
Adjustable to Zero

*Adjustable to ±0.003% with proper adjustment of external trim pots.

STABILITY

Diff. Linearity Tempco
1 ppm/°C typ., 3.0 ppm/°C max.

Range (Gain) Tempco
7 ppm/°C typ., 10 ppm/°C max.

Zero Offset Tempco
Unipolar
5 ppm/°C typ., 7.5 ppm/°C max.

Bipolar
7 ppm/°C typ., 10 ppm/°C max.

Noise
±0.005% FSR p-p (3σ)

Power Supply Sensitivity
±0.0005%/% P.S. Change, nominal

Warm Up Time
5 minutes

POWER SUPPLY GROUNDS

Separate Analog and digital Grounds; 250 mV max. allowable difference of potential

POWER REQUIREMENTS

+15V ±3%
34 mA max. + Load

−15V ±3%
30 mA max. + Load

+5V ±5%
35 mA max. + Load

ENVIRONMENTAL AND PACKAGING

Operating Temperature
0° to 70°C

Relative Humidity (Non-Condensing)
5% to 95%

Size
2" x 2" x 0.375"

Shielding
RFI 6 sides, EMI 5 sides

Storage Temp.
−25°C to +85°C

APPLICATION DATA

Calibration

Linearity and relative accuracy for 14-bit performance are designed in. Absolute accuracy calibration may be set externally as shown in Figure 2 and described below.

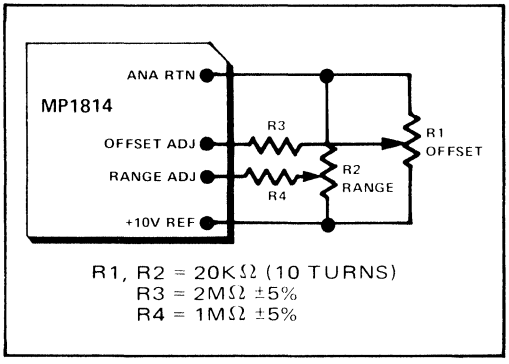


Figure 2. Connecting External Adjustments Potentiometers for MP1814 OFFSET and RANGE.

Offset Adjustment

The analog output is adjusted for zero, or other desired offset, by connecting R1 (10-turn 20 kΩ potentiometer) and R3 (2 MΩ) as shown in Figure 2. Use thermally stable components of 50 ppm/°C or better, and keep the connection leads as short as possible to maintain the MP1814 performance.

After making the required connections, (Table 1) apply the appropriate "ZERO" code (See Table 2), and adjust R1 for 0.0000 volts output.

FOR FSR ↓	CONNECT		
	RANGE MODE TO ↓	RANGE 1 TO ↓	RANGE 2 TO ↓
±10V	REF SW	+5V REF	ANA RTN
±5V	REF SW	+5V REF	V_{OUT}
+10V	ANA RTN	ANA RTN	V_{OUT}
+5V	ANA RTN	V_{OUT}	V_{OUT}

Table 1. Connection Matrix for Full Scale Outputs.

ORDERING GUIDE

Specify **MP1814**

Range Adjustment

The MP1814 analog output may be calibrated for the desired full scale range by connecting R2 (10-turn 20 kΩ potentiometer) and R4 (1 MΩ) as shown in Figure 2. (See stability and lead length requirements described above.) Apply the full scale code as indicated in Table 1, and adjust R2 for the appropriate full scale voltage output.

CODE	UNIPOLAR (Binary)		BIPOLAR (Offset Binary)	
	0 to +10V	0 to +5V	±10V	±5V
111 111 111 111 11	9.9994	4.9997	9.9988	4.9994
100 000 000 000 00	5.0000	2.5000	0.0000	0.0000
000 000 000 000 01	0.0006	0.0003	−9.9988	−4.9994
000 000 000 000 00	0.0000	0.0000	−10.0000	−5.0000

Table 2. MP1814 Coding Translation Table.

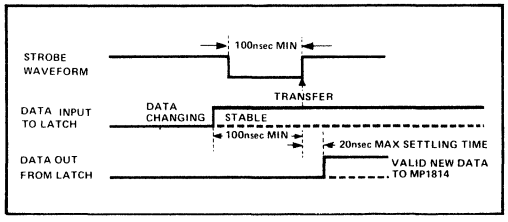


Figure 3. Strobe and Data Input Timing.

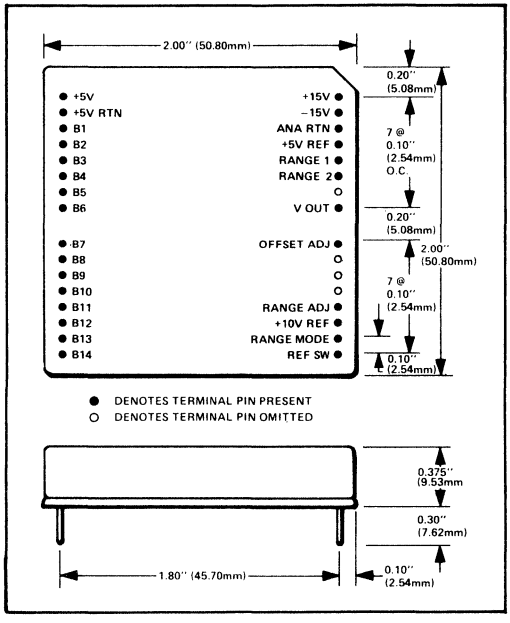
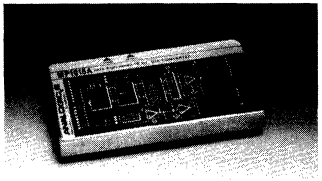


Figure 4. MP1814 Outline Dimensions.



ANALOGIC®

MP1900A SERIES

High Speed, High Stability
13, 14, 15 and 16-Bit D/A Converters

Description

The MP1900A Series are thermally stabilized, precision digital-to-analog (D/A) converters that provide exceptional linearity, and stability over both time and temperature. Employing unique offset and gain stabilizing circuitry, each model in the Series offers true accuracy commensurate with its resolution at throughput rates in excess of 100 kHz. Linearity of 0.001% FSR, absolute accuracy of 0.002% FSR, and a differential linearity tempco of 1 ppm/°C are achieved to meet the most demanding industrial and instrumentation requirements, where stability over time and temperature and high reliability are critical.

Both unipolar and bipolar current and voltage output modes are provided to allow maximum flexibility in implementing a design using the MP1900A Series. Settling times to within 1 LSB of a full scale input step of 1.5 μs in the current mode, or 10 μs in the voltage mode (using the internal output amplifier) are obtainable. Additional features such as data input latches, internal gain and offset adjustment potentiometers, internal reference supply and pin-selectable operating mode, combine to make system integration of the MP1900A Series of high accuracy, high stability D/A converters very straight-forward.

Completely self-contained, each model in the MP1900A Series is packaged in a fully shielded 2 x 4 x 0.375" metal can. The locations of the various functional pins is standardized, allowing or direct interchangeability among the four converters in the Series.

Features

- **Up to 16-bit Resolution**
- **0.001% FSR Integral Linearity**
- **0.002% FSR Absolute Accuracy**
- **Settling Times to 1.5 μs**
- **Pin-Selectable Output Mode**
  Unipolar or bipolar
  Current or voltage
- **Thermally Stabilized Gain and Offset**

Applications

- **Precision Incremental CRT Displays**
- **Digital Control of Power Supplies**
- **Automated Component Testing**
- **Waveform Synthesis**
- **Automated Phototypesetting**

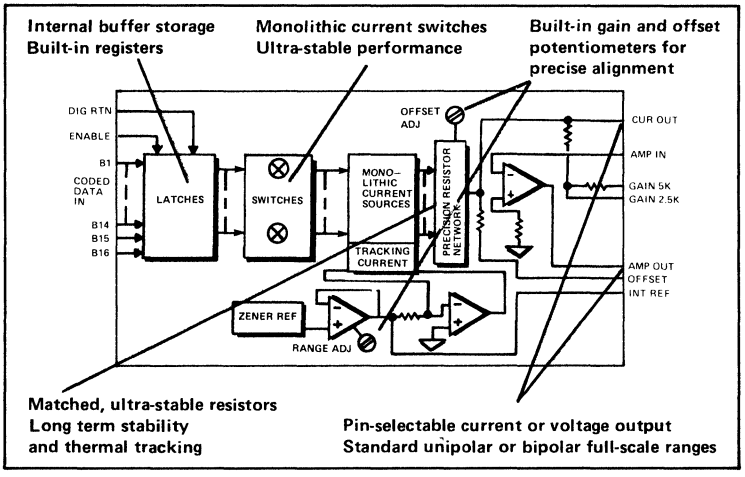


Figure 1. MP1916A Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

PARAMETER

DIGITAL INPUT

Enable
32 loads

DTL/TTL Compatible
2 loads

Resolution
16 — MP1916A, 15 — MP1915A, 14 — MP1914A, 13 — MP1913A

Input Codes
Binary, 2's complement (pin selectable)

ANALOG OUTPUT

Current Mode

Full Scale Range
−2 mA to +2 mA, bipolar, 0 to −4 mA, unipolar

Impedance
1.25 kΩ, bipolar, 2 kΩ, unipolar

Voltage Compliance
± 1V max.

Voltage Mode
Full Scale Range
± 10V, ± 5V, 0 to +10V, 0 to +5V (pin selectable)

Impedance
0.1Ω @ dc

Load Current
± 5 mA (includes feedback current)

INTERNAL REFERENCE OUTPUT

Voltage
6.5V ± 0.3% (proportional to range control)

Output Impedance
0.1Ω

Current Load
1 mA max.

SPEED

Current Mode

Settling Time to 1 LSB
1.0 μs typ. — MP1916A, 0.8 μs typ. — MP1915A, 0.6 μs typ. — MP1914A & MP1913A

(Full Scale Step)
1.5 μs max. — MP1916A, 1.2 μs max. — MP1915A, 1.0 μs max. — MP1914A & MP1913A

Voltage Mode (Internal Amp) Settling Time to 1 LSB
10 μs typ., 20 μs max. — MP1916A
10 μs typ., 17 μs max. — MP1915A
10 μs typ., 15 μs max. — MP1914A & MP1913A

Slew Rate
2 V/μs

ACCURACY

Linearity
0.001% FSR — MP1916A, 0.0015% FSR — MP1915A, 0.003% FSR — MP1914A, 0.006% FSR — MP1913A

Absolute Accuracy
0.002% FSR — MP1916A, 0.004% FSR — MP1915A, 0.006% FSR — MP1914A, 0.01% FSR — MP1913A

STABILITY

Current and Voltage Modes

Tempco of Reference
2 ppm/°C typ., 3 ppm/°C max. — MP1916A, MP1915A & MP1914A
3 ppm/°C typ., 5 ppm/°C max. — MP1913A

Tempco of Linearity
1 ppm/°C typ., 2 ppm/°C max.

Tempco of Gain
2 ppm/°C typ., 3 ppm/°C max. — MP1916A, MP1915A & MP1914A
3 ppm/°C typ., 6 ppm/°C max. — MP1913A

Power Supply Sensitivity
5 ppm FSR/% change in dc voltage

Current Mode

Tempco of Offset
1 ppm/°C max., unipolar; 2 ppm/°C max., bipolar — MP1916A, MP1915A & MP1914A
1 ppm/°C max., unipolar; 3 ppm/°C max., bipolar — MP1913A

Voltage Mode
Tempco of Offset
2 ppm/°C max., unipolar — MP1916A, MP1915A & MP1914A
6 ppm/°C max., unipolar — MP1913A

NOISE (3σ)

dc to 1 MHz
0.0015% FSR p-p — MP1916A, MP1915A & MP1914A
0.0030% FSR p-p — MP1913A

dc to 60 Hz
50 μV p-p (0.00025% FSR)

DIGITAL CONTROL*

Enable Input
TTL compatible (high = enable)

Loading
32 loads

*See Timing Diagram

POWER SUPPLY

+15V ±3%
35 mA typ. + load current

−15V ±3%
35 mA typ. + load current

+5V ±5%
180 mA typ.

ENVIRONMENTAL & PACKAGING

Storage & Operating Temperature
0°C to +60°C

Relative Humidity
5% to 95%, non-condensing

Warmup Time
5 min. to spec. accuracy

Fault Protection
Output may be shorted to ground indefinitely without damage

Size
4 x 2 x 0.375" (101.6 x 50.8 x 9.5 mm)

Shielding
RFI 6 sides; EMI 5 sides

Using the MP1900A Series

The 1900A Series of 13- to 16-bit D/A Converters is factory equipped to permit user selection of any of the standard performance options. These selections are accomplished by making appropriate pin connections externally at the module pins.

Operation for binary, offset binary, or two's complement input code, voltage or current output mode, and the full-scale output range are determined by making the pin connections specified in Figure 2.

When using the current output mode, the built-in voltage amplifier is available for other system applications. However, if not used, the amplifier voltage output should be conected to AMP IN, to prevent possible no-load amplifier oscillations from coupling to the current output signal.

OUTPUT AND CODING REQUIRED		JUMPERS PIN JUMPERS ON MODULE
0 TO 4mA		
−2mA TO +2mA		OFFSET TO INT REF
±10V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 5K TO AMP OUT OFFSET TO INT REF
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 5K TO OUTPUT* OFFSET TO INT REF
±5V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT OFFSET TO INT REF
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT* OFFSET TO INT REF
+10V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT*
+5V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT GAIN 5K TO CUR OUT
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT* GAIN 5K TO CUR OUT
UNIPOLAR BINARY OR OFFSET BINARY		N1 TO N2
TWO'S COMPLEMENT		N3 TO N2

NOTE: The +IN* terminal of the external op amp should be connected to the ANA RTN Pin of the MP1916 via a resistor (1.2KΩ).
*Connection on external op. amp.

Figure 2. Mode and Full-Scale Range Jumper Connections.

Adjustments

Built-in potentiometers may be adjusted to customize the MP1900TC Series D/A converters to system aplications requiring trimming of Range (Gain) and/or Offset (Zero). The RANGE and OFFSET potentiometers are identified and located on the label, and access to them is made at the top of the Modupac.

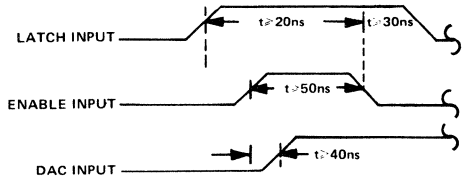
MP1916A DIGITAL INPUT DATA CODING

FORMAT	INPUT CODE MSB (for 16 bits)** LSB	I_{OUT} Milliamperes* 1913	1914	1915	1916
Unipolar Binary	1111 1111 1111 1111	−3.99950	−3.99975	−3.99988	−3.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
Offset Binary	1111 1111 1111 1111	−1.99950	−1.99975	−1.99988	−1.99994
	1000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
	0000 0000 0000 0000	+2.00000	+2.00000	+2.00000	+2.00000
Two's Complement	0111 1111 1111 1111	−1.99950	−1.99975	−1.99988	−1.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
	1000 0000 0000 0000	+2.00000	+2.00000	+2.00000	+2.00000

*For Voltage Amplifier, V_{OUT} is defined by Selected Feedback Resistor, R_{FB}; $V_{OUT} = -I_{OUT} \times R_{FB}$.
**For lesser bits, delete less significant bits.

To trim any offsets to zero, apply the coded input for zero signal, and trim OFFSET for a zero analog current or voltage output.

To adjust the range, apply a full-scale coded input and trim RANGE for the correct analog current or voltage output.



Typical Timing Diagram For Any Bit.

Data present at the latch input is transferred to the DAC input when the enable line goes high, and follows the data as long as the enable line remains high. When the enable goes low, the information that was present just prior to the time the transition occurred is retained.

Figure 3. Typical Timing, MP1900A Series.

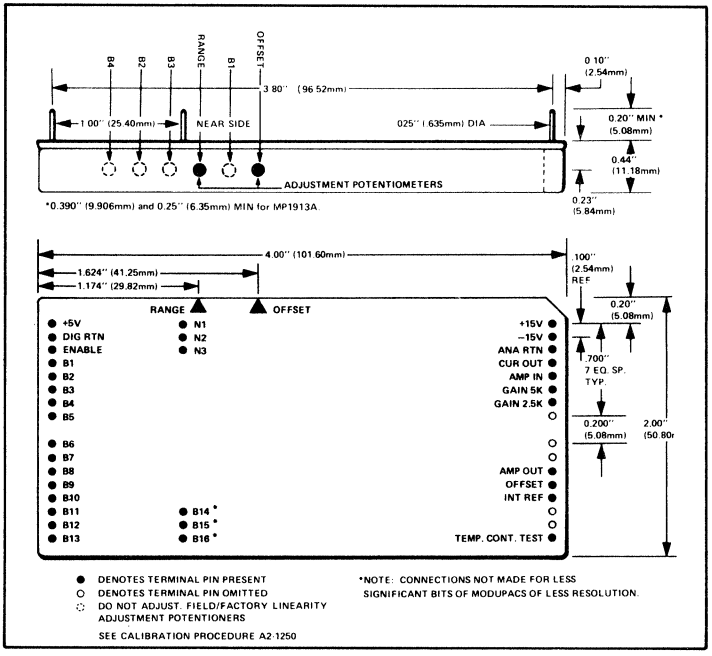
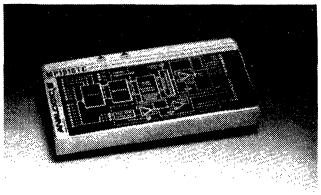


Figure 4. MP19XXA Outline Drawing and Pin Locations.

ORDERING GUIDE

For	Specify
13-Bit D/A	**MP1913A**
14-Bit D/A	**MP1914A**
15-Bit D/A	**MP1915A**
16-Bit D/A	**MP1916A**



ANALOGIC®

MP1900TC SERIES

High Speed, Ultra-Stable 14-, 15-, and 16-Bit D/A Converters

Description

The MP1900TC Series are thermally stabilized, precision digital-to-analog (D/A) converters that provide exceptional linearity and stability over both time and temperature. Employing unique temperature stabilizing circuitry, each model in the Series offers true accuracy commensurate with its resolution at throughput rates in excess of 100 kHz. Linearity of 0.001% FSR, absolute accuracy of 0.002% FSR, and combined Reference, Gain, Linearity and Offset tempco of 1 ppm/°C are achieved to meet the most demanding industrial and instrumentation requirements, where stability over time and temperature and high reliability are critical.

Both unipolar and bipolar current and voltage output modes are provided to allow maximum flexibility in implementing a design using the MP1900TC Series. Settling times to within 1 LSB of a full scale input step of 1.5 μs in the current mode, or 10 μs in the voltage mode (using the internal output amplifier) are obtainable. Additional features such as data input latches, internal gain and offset adjustment potentiometers, internal reference supply and pin-selectable operating mode, combine to make system integration of the MP1900TC Series of high accuracy, high stability D/A converters very straight-forward.

Completely self-contained, each model in the MP1900TC Series is packaged in a fully shielded 2 x 4 x 0.44" metal can. The locations of the various functional pins is standardized, allowing for direct interchangeability among the four converters in the Series.

Features

- **Up to 16-bit Resolution**
- **0.001% FSR Integral Linearity**
- **0.002% FSR Absolute Accuracy**
- **Settling Times to 1.5 μs**
- **Pin-Selectable Output Mode**
  Unipolar of bipolar
  Current or voltage
- **Thermally Stabilized**

Applications

- **Precision Incremental CRT Displays**
- **Digital Control of Power Supplies**
- **Automated Component Testing**
- **Waveform Synthesis**
- **Automated Phototypesetting**

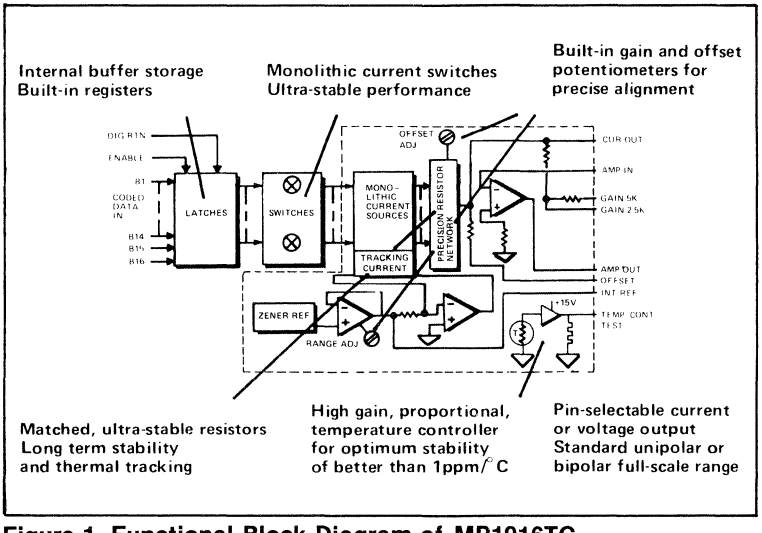


Figure 1. Functional Block Diagram of MP1916TC.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

PARAMETER

ANALOG OUTPUT

Current Mode

Full Scale Range
−2 mA to +2 mA, bipolar; 0 to −4 mA, unipolar

Impedance
1.25 kΩ, bipolar; 2 kΩ, unipolar

Voltage Compliance
±1V maximum

Voltage Mode

Full Scale Range
±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)

Impedance
<0.1Ω @ dc

Load Current
±5 mA max. (includes feedback current)

DIGITAL INPUT

DTL/TTL Compatible
2 loads

Number of Bits
16 — MP1916TC, 15 — MP1915TC, 14 — MP1914TC

Input Codes
Binary, 2's complement (pin selectable)

Enable
32 TTL Loads

INTERNAL REFERENCE OUTPUT

Voltage
6.5V ±0.15% (proportional to range control)

Output Impedance
<0.1Ω

Current Load
1 mA maximum

SPEED

Current Mode

Settling Time to 1 LSB
1 μs typ. — MP1916TC, 0.8 μs typ. — MP1915TC, 0.6 μs typ. — MP1914TC

(Full Scale Step)
1.5 μs max. — MP1916TC, 1.2 μs max. — MP1915TC, 1.0 μs max. — MP1914TC

Voltage Mode (Internal Amp)
Settling Time to 1 LSB
10 μs typ., 20 μs max. — MP1916TC
10 μs typ., 17 μs max. — MP1915TC
10 μs typ., 15 μs max. — MP1914TC

Slew Rate
2 V/μs

ACCURACY (@ +15°C to +35°C)

Relative Accuracy (Linearity)
0.001% FSR max. — MP1916TC, 0.0015% FSR max. — MP1915TC, 0.003% FSR — MP1914TC

Absolute Accuracy (NBS Traceability)
0.002% FSR max. — MP1916TC, 0.004% FSR max. — MP1915TC, 0.006% FSR — MP1914TC

STABILITY (@ +15°C to +35°C)

Current and Voltage Modes

Total Combined Tempco's of Reference, Linearity, Gain and Offset
1 ppm/°C max.

For 0 to +15°C and +35°C to +60°C without Temperature Control
5 ppm/°C max.

Power Supply Sensitivity
5 ppm FS/% change in dc voltage

POWER REQUIREMENTS

+15 ±0.5 Vdc
DAC: 35 mA typ. + load current
Temperature Controller: 150 mA initial, 60 mA typ. after warmup @ 25°C

−15 ±0.5 Vdc
35 mA typ. + load current

+5 ±0.25 Vdc
180 mA typ.

ENVIRONMENTAL & MECHANICAL

Controlled Operating Temperature Range[2]
+15°C to +35°C

Storage Temperature Range
−25°C to +85°C

Relative Humidity
5% to 95%, non-condensing

Warmup Time
10 min. to spec. accuracy

Fault Protection
Output may be shorted to ground indefinitely without damage

Dimensions
4 x 2 x 0.44" (101.6 x 50.8 x 11.2 mm)

Shielding
RFI 6 sides, EMI 5 sides

1. Stabilities and temperatures given are for a normally specified DAC operation of +15°C to +35°C. For other temperature ranges, data may be shifted accordingly. See Note 2.
2. Any 20°C span between 0°C and +60°C may be user-specified.

Principles of Operation

As shown in Figure 1, binary data is loaded in parallel into the internal latches by a high logic level at the ENABLE input. The latched outputs of the eight more significant bits drive quad switches that steer precision current sources either to the CURRENT OUTPUT or to ground. Exact current values are determined by the binary-weighted, precision, thermally tracking resistor network. This network converts the precision internal reference voltage into 16 precision currents which are gated to the output by the current steering switches. The eight less significant bits are provided by a monolithic digital-to-analog converter.

The entire package described above plus the gain-setting resistors associated with the output voltage amplifier are enclosed in a proportional temperature controller which, in turn, includes a thermistor, an operational amplifier, and a heating element. Temperature determines the thermistor output. When the exterior temperature ambient drops, the thermistor resistance increases. This action causes an increased amplifier output that forces more current through the heating element. Conversely, when the exterior temperature rises, less current flows through the heating element. Thus, a constant temperature, well within 1°C, is maintained for an exterior 20°C ambient span. Wider temperature ranges or different ambient spans can be specified at time of ordering.

Using the MP1900TC Series

The MP1900TC 14- to 16-bit D/A Converters are factory equipped to permit users to select any of the standard performance options. These selections are accomplished by making appropriate connections externally at the module pins.

Operation for binary, offset binary, or two's complement input code, voltage or current output mode, and the full-scale output range are determined by making the pin connections specified in Figure 2.

When using the current output mode, the built-in voltage amplifier is available for other system applications. However, if not used, the amplifier voltage output should be connected to AMP IN to prevent possible no-load amplifier oscillations from feedback coupling to the current output signal.

OUTPUT AND CODING REQUIRED		JUMPERS PIN JUMPERS ON MODULE
	0 TO 4mA	
	−2mA TO +2mA	OFFSET TO INT REF
±10V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 5K TO AMP OUT OFFSET TO INT REF
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 5K TO OUTPUT* OFFSET TO INT REF
±5V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT OFFSET TO INT REF
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT* OFFSET TO INT REF
+10V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT*
+5V	INTERNAL AMP	CUR OUT TO AMP IN GAIN 2.5K TO AMP OUT GAIN 5K TO CUR OUT
	EXTERNAL AMP	CUR OUT TO − IN* GAIN 2.5K TO OUTPUT* GAIN 5K TO CUR OUT
UNIPOLAR BINARY OR OFFSET BINARY		N1 TO N2
TWO'S COMPLEMENT		N3 TO N2

NOTE: The + IN* terminal of the external op. amp should be connected to the ANA RTN Pin of the MP1916 via a resistor (1.2 kΩ).
*Connection on external op. Amp.

Figure 2. Mode and Full-Scale Range Jumper Connections.

Adjustments

Built-in potentiometers may be adjusted to customize the MP1900TC Series D/A converters to system aplications requiring trimming of Range (Gain) and/or Offset (Zero). The RANGE and OFFSET potentiometers are identified and located on the label, and access to them is made at the top of the Modupac.

To trim any offsets to zero, apply the coded input for zero signal, and trim OFFSET for a zero analog current or voltage output.

To adjust the range, apply a full-scale coded input, and trim RANGE for the correct analog current or voltage output.

DIGITAL INPUT DATA CODING				
FORMAT	INPUT CODE (MSB) (for 16 bits)** (LSB)	I_{OUT} Milliamperes* 1914TC	1915TC	1916TC
Unipolar Binary	1111 1111 1111 1111	−3.99975	−3.99988	−3.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000
Offset Binary	1111 1111 1111 1111	−1.99975	−1.99988	−1.99994
	1000 0000 0000 0000	0.00000	0.00000	0.00000
	0000 0000 0000 0000	+2.00000	+2.00000	+2.00000
Two's Complement	0111 1111 1111 1111	−1.99975	−1.99988	−1.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000
	1000 0000 0000 0000	+2.00000	+2.00000	+2.00000

*For Voltage Amplifier, V_{OUT} is defined by Selected Feedback Resistor, R_{FB}; $V_{OUT} = -I_{OUT} \times R_{FB}$.

**For fewer bits, delete less significant bits

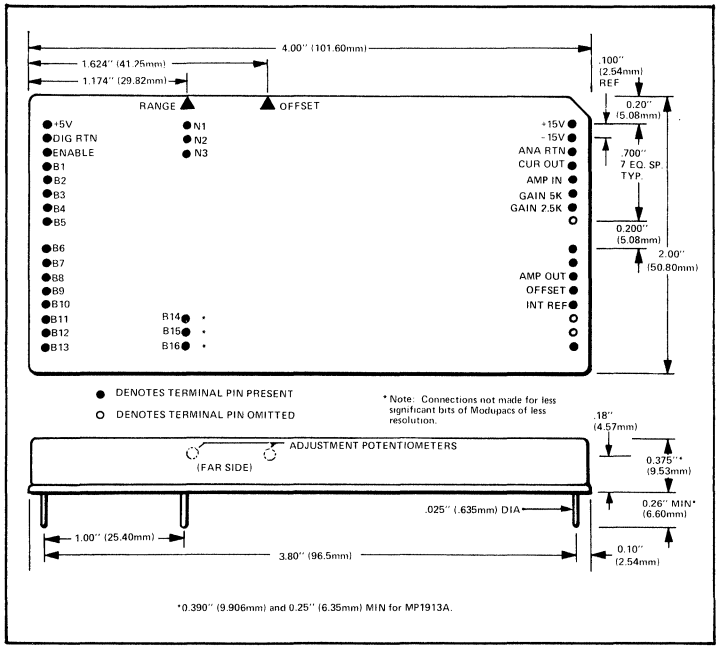


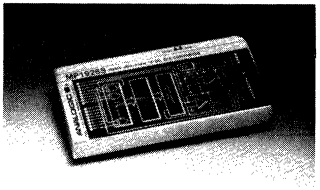
Figure 3. MP1900TC Outline Drawing and Pin Locations.

ORDERING GUIDE

Specify

14-Bit D/A Converter **MP1914TC**
15-Bit D/A Converter **MP1915TC**
16-Bit D/A Converter **MP1916TC**

If stabilization over 20°C span other than +15°C to +35°C is required, please specify temperature span when ordering.



ANALOGIC®

MP1926

Ultra-Linear, 200 kHz 16-Bit Sign/Magnitude D/A Converter

Description

The MP1926 is an ultra-linear, high speed, 16-bit digital-to-analog converter module designed specifically for reconstructing dynamic complex waveforms from digital data, particularly audio or acoustic signals, sonar, and other signals that have a substantial amount of the information content in the vicinity of "zero volts" (midrange). In such systems, power occasionally peaks well above the rms power level, as in speech or music. Thus, accurately recreating such information from digital data requires exceptional small signal performance to handle the information near zero level without crossover distortion, yet there must be a very large dynamic range to handle the bursts of higher amplitudes, together with the ability to handle the wide range of frequency interest.

The MP1926 meets these requirements with an internal sign/magnitude architecture that gives **18 bits of linearity for signals near zero volts and a 3 μs settling time** — at a price less than that of other, low speed, 16-bit DACs which typically offer, at best, 14-bit accuracy at midrange.

Accepting standard input binary codes, including offset binary and 2's complement. Analogic's proprietary (pat. pending) sign/magnitude internal architecture provides performance that actually improves as the signal approaches zero from either direction (error proportional to the signal's absolute value, or magnitude). With the commonly used "offset binary" architecture, which produces a bipolar output by offsetting an internal unipolar signal by one half full scale, even a small error in the

(continued)

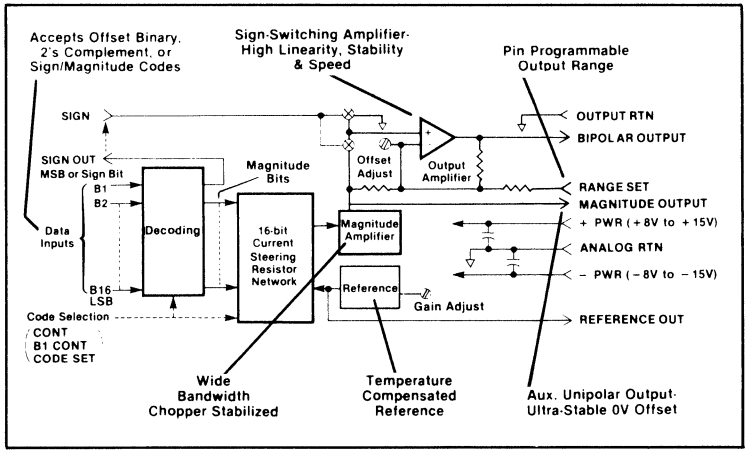


Figure 1. MP1926 Functional Block Diagram.

Features

- **Low Harmonic Distortion** 0.005% (0.0005 dB!)
- **Wide Dynamic Range 16 bits**
- **Ultra-High Linearity Over the Full Scale Range** ± ¼ LSB, max. mid-range non-linearity
- **High speed** settling time <3 μs (MP1926A)
- **Low Tempco's** total drift from all sources <1 ppm/°C (MP1926S)
- **Low Power** 250 mW
- **Built-In Code Conversion** uses standard codes
- **Low Cost**
- **Flexible**
  ± 8V to ± 15V power supply
  TTL or CMOS inputs
  Offset Binary, 2's Complement, or
  Sign/Magnitude codes
  Operates −25°C to +85°C

Applications

- **Professional Audio Systems — Low Total Harmonic Distortion**
- **Telecommunications Digitizing — High Noise Power Ratio**
- **High Resolution Information Translation Systems**
- **High Speed, High Precision, Automated Test Instrumentation**
- **Wide Dynamic Range, Computer Controlled, Industrial Processes**
- **Waveform Synthesis and Recovery**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

BIPOLAR OUTPUT

Full Scale Voltage Ranges (FSR)[1]
±5V or ±10V

dc Output Impedance
0.1Ω max.

Load Current
5 mA max.

ACCURACY @ 25°C — TOTAL NONLINEARITY

For Mid-Range Outputs Centered about Zero Volts (¼ FSR)[2]
±4 ppm FSR max.

Over the Full Scale Range[3]
±15 ppm FSR max.

Absolute Range Accuracy[4]
MP1926A — ±0.1% FSR
MP1926S — ±0.01% FSR

Offset Voltage[4]
MP1926A — ±1 mV
MP1926S — ±0.1 mV

Zero Code, 0° to 70°C
Continuous and monotonic through zero

STABILITY

Tempco of Differential Nonlinearity for Mid-Range Outputs Centered about Zero Volt (¼ FSR)
±0.25 typ., ±1 max. ppm FSR/°C

Over the FSR
±0.5 typ., ±2 max. ppm FSR/°C

Tempco of Gain (Includes Reference)[5]
MP1926A — ±10 ppm of READING/°C typ., ±30 ppm of READING/°C max.
MP1926S — ±2 ppm of READING/°C typ., ±5 ppm of READING/°C max.

Tempco of Offset Voltage[6]
MP1926A — ±5 ppm FSR/°C max.
MP1926S — ±0.5 ppm FSR/°C max.

Power Supply Sensitivity
Gain
20 ppm FSR/V

Offset
20 μV/V

Recommended Recalibration Interval
MP1926A — N/A
MP1926S — See Note 4

Warm Up Time to Specified Accuracy
5 minutes max.

Settling Time for 5V step
to 0.01%
MP1926A — 3 μs max.
MP1926S — 40 μs max.

to 1 LSB
MP1926A — 5 μs max.
MP1926S — 50 μs max.

Slew Rate
MP1926A — 7.5V/μs min.
MP1926S — 0.15V/μs min.

Noise (10 Hz to 100 kHz)
35 μV rms

Output Fault Protection
Indefinite short to ground

MAGNITUDE OUTPUT (Auxiliary Output)

Voltage Range
0 to −5V

Offset Voltage
20 μV typ.

Tempco of Offset Voltage
1 μV/°C max.

Output Fault Protection
Indefinite short to ground

INTERNAL REFERENCE OUTPUT

Nominal Voltage
+5V (proportional to Range Control)

dc Output Impedance
0.1Ω max.

Load Current
1 mA max.

DIGITAL INPUTS

Resolution
16 bits

Format (Pin Programmable)
See Tables 1 & 2

Logic Compatibility[7]
CMOS, TTL

Low (FALSE) Level/High (TRUE) Level
0.4V ±0.6V/4.6V ±0.6V

Input Impedance
1 MΩ min.

POWER REQUIREMENTS[8]

Nominal Voltage[1]
±8V to ±15V

Absolute Max.
±16V

Current, Exclusive of Load ±16 mA

Dissipation @ ±8V, exclusive of load
250 mW max.

Dissipation @ ±15V, exclusive of load
500 mW max.

ENVIRONMENT

Rated Performance
0°C to 70°C

Operating Temperature Range
−25°C to +85°C

Storage Temperature Range
−55°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

PACKAGING

Dimensions, inches (mm rounded)
2 x 4 x 0.44 inches (50.8 x 101.6 x 11.2 mm)

Electromagnetic Shielding
5 sides

Electrostatic Shielding
6 sides

Notes
1. FSR is pin programmable. 20V FSR requires ± 15V power supply.
2. Deviation from best straight line.
3. Deviation from best straight line.
4. Range accuracy (gain) and offset voltage each adjustable via externally accessible potentiometers. Specifications given are factory setting, using ± 8V supplied. Recommended recalibration interval is three months in an instrumentation application (MP1926S).
5. For bipolar signals, X ppm of READING is less than or equal to X/2 ppm of FSR, e.g., 2 ppm of READING ≤1 ppm FSR.
6. Total at 0V, not affected by reference drift.
7. Unit does not include pull-up resistors, which may be required for TTL.
8. Analog Return, Output Return, and case are tied internally.

Description (cont.)

offsetting resistor can frequently cause large output errors near zero volts. Therefore, the MP1926 is the only high speed, 16-bit digital-to-analog converter to offer linearity near zero volts *better than ± ¼ LSB (4 ppm)* and total full range harmonic distortion (measured with an output deglitch amplifier) *better than 0.005% (0.0005 dB!).*

Moreover, this performance is preserved over a wide temperature range. The MP1926S, a version optimized for use in reference-type applications, offers voltage offset, linearity, and gain drifts so low that the worst-case total (algebraic sum) of their effects for signals near zero volts is typically **less than 1 ppm/°C from 0°C to 70°C.** Even the very fast MP1926A version offers better stability than provided by many higher-priced 16-bit DACs. Both versions have an auxiliary unipolar output that is proportional to the magnitude of the bipolar output and which offers zero voltage offset stability of 1 μV/°C!

Besides offering such linear and stable performance, the MP1926 offers versatility. It directly accepts offset binary and two's complement codes as well as sign/magnitude codes, without added circuitry, from CMOS or TTL logic, so that it can be interfaced easily with most computer-based systems. It operates from a single bipolar power supply (no separate +5V supply is required), and its low power consumption of 250 mW and metal case qualify it for use in a variety of environments. Thus the benefits of exceptionally good small-signal performance, high speed, and very wide dynamic range, coupled with low cost, make the MP1926 the ideal choice for a large variety of applications.

Performance Features

An internal sign/magnitude architecture provides optimum bipolar performance, particularly when compared to the commonly used offset binary architectures. Several key features of the MP1926 make this dramatic improvement in performance easy to use in many applications. Those features include low gain, linearity, offset errors: onboard decoding of several popular digital codes (converting to the sign/magnitude code used internally; and hard-wired range selection.

Bipolar Performance

An internal sign/magnitude architecture provides optimum bipolar performance because step size error decreases as the signal magnitude decreases, rather than being proportional to major bit weight contributions as in an offset binary architecture. The MP1926 employs a unique internal implementation of the sign/magnitude algorithm. Figure 1 shows that the 15 LSBs of a decoded (code converted) digital word control a resistor network that provides a scaled current to a chopper stabilized Magnitude Amplifier, which in turn converts this current to a unipolar (0V to −5V) voltage. The bipolar output is generated by using the MSB to configure the Output Amplifier as either an inverter or a follower.

Figure 2 shows the resulting performance for a typical MP1926 — note that the error decreases as the output approaches zero from either direction, that the performance is symmetric above and below 0V, and that the output crosses through zero continuously.

As shown, *for midrange outputs the nonlinearity is typically much less than 4 ppm FSR.* Thus the MP1926 provides a full 96 dB of *useable* dynamic range (2^{16} voltage steps). Most other 16-bit converters have a much smaller effective dynamic range because they exhibit relatively large errors

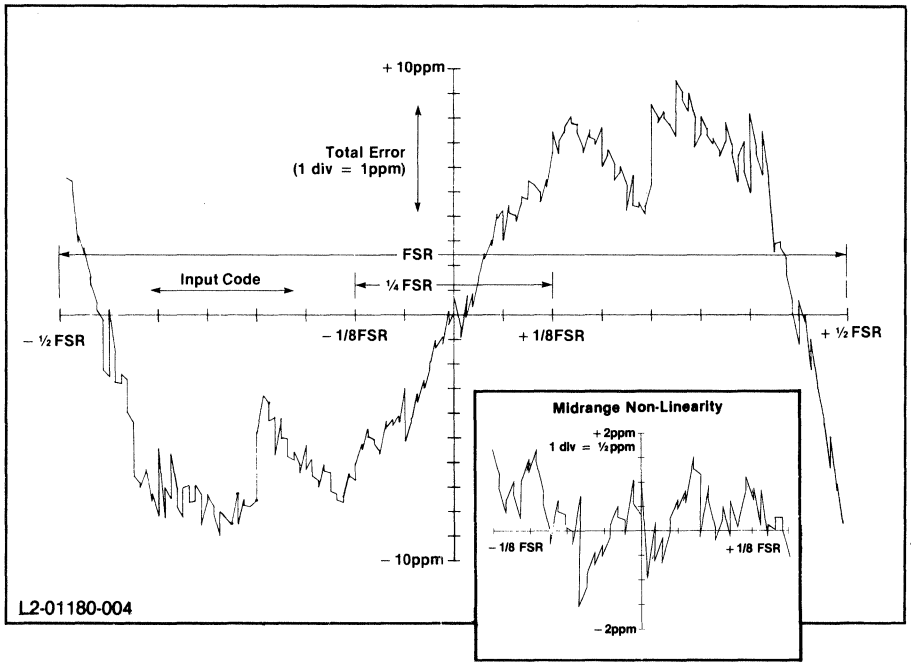


Figure 2. Error Plot of an MP1926. Error measured at zero volts and at 256 other points across the full scale range. These included the 128 most major bit transition points, plus a point 1 LSB away from each. Over the FSR the largest total error (non-linearity, gain and offset) is **less than 10 ppm.** Over the midrange centered around zero volts, the non-linearity error is **less than 2 ppm.**

for small output signals. The following paragraphs show why the MP1926 approach is superior to offset binary approaches and to earlier sign/magnitude approaches in most bipolar applications.

Figure 3 compares performance around zero of offset binary and sign/magnitude architectures, showing dramatically the lower gain error sensitivity of a sign/magnitude approach. Further, an offset binary converter requires a precise match (much better than ½ LSB) between the MSB resistor and the offsetting resistor. For outputs near 0V the MSB is switched on and all other bits are switched off (or MSB off, all other bits on), so small imbalances and drifts with time can easily cause a discontinuity at 0V which is proportional to the MSB weighting — i.e., an error proportional to one half of the full scale even for small signals.

On the other hand, in a converter using an internal sign/magnitude approach, the most significantly weighted resistors do not affect the current summing for outputs near 0V, so linearity is inherently superior when using the same quality resistors, both *initially* and *over time.* (Dynamic accuracy at zero is also superior because a zero crossing is not a major current switching point.)

Initial Linearity

For midrange outputs centered around 0V, the MP1926's linearity is better than ± ¼ LSB (4 ppm FSR). For outputs beyond midrange, the increment between codes equals the LSB step size of 15 ppm plus a differential nonlinearity of +13/–9 ppm FSR, *even at the major carries.* This ensures both monotonicity and no missing steps over the entire output range.

Long Term Stability

Most resistors, except for laboratory standard wire-wound types, exhibit tracking ratios worse than 15 ppm/year. In offset binary converters such resistor drift frequently results in significant linearity drift for signals near 0V; a converter using an internal sign/magnitude approach can be expected to be four or five times less sensitive to resistor drift. For signals centered around 0V (¼ FSR), *long-term linearity stability of the MP1926 is predicted to be much better than ½ LSB per year.*

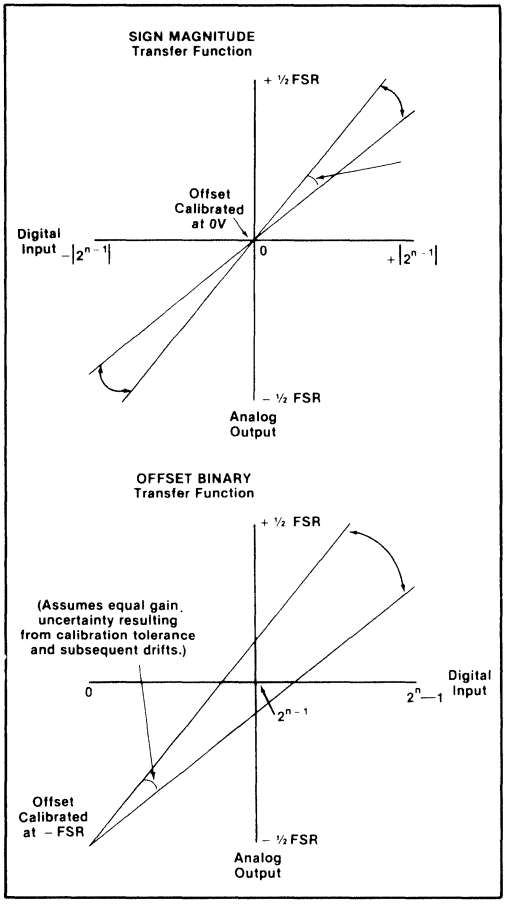


Figure 3. Comparison of Performance Near Zero. The transfer function of an offset binary converter originates at – FS (all current switches off). Thus 0V is usually ½ of FSR, and any gain drift will shift the 0V output as shown. With an internal sign/magnitude approach the transfer function originates at 0V (all current switches off), so the 0V output is not affected by gain drift.

The classical problem of attaining both low offset drift and high speed simultaneously when using a sign/magnitude approach has been solved by using the unique Magnitude Amplifier. (An offset error in the Magnitude signal would cause a discontinuity whenever the sign switches at a zero crossing, and would cause the output to be asymmetric about 0V). Earlier sign/magnitude approaches have met this low offset requirement by using slow amplifiers, limiting their applicability. The MP1926's Magnitude Amplifier is both chopper stabilized and fast. Its offset drift is an extremely low 1 μV/°C, yet the MP1926A settles to 1 LSB in only 5 μs. The converter has no offsetting resistor, so the only other contributor to offset drift is the output amplifier, resulting in less than 0.5 ppm/°C drift for the MP1926S. Therefore, the module's performance is symmetric about zero yet fast enough for a wide variety of applications.

In summary, the Analogic MP1926 sign/magnitude approach inherently provides better bipolar performance than would any offset binary approach using equal quality resistors and amplifiers. Furthermore, the precision chopper stabilized design of the MP1926 is the optimum internal implementation of the sign/magnitude approach. The resulting total improvement for a typical application (e.g., rms signal ±10% of the peak signal) can be on the order of 20 dB!

Input Decoding

The MP1926 may be connected to accept either of four input code types: offset binary, 2's complement, sign/magnitude, or modified sign/magnitude. Neither external decoding control nor an MSB input are required, because interconnecting the module per Table 1 automatically provides conversion to the sign/magnitude code used internally. Each code bit is supplied to one of 16 CMOS EXCLUSIVE OR gates. Each gate either follows or inverts the bit, depending on the state of the CONTrol signal connected to its second input.*

	MODULE CONNECTIONS			
CODE	SIGN to	CONT to	B1 CONT to	CODE SET to
Offset Binary	SIGN OUT	SIGN OUT	REF OUT	REF OUT
2's Complement	SIGN OUT	SIGN OUT	OUT RET	REF OUT
Sign/Magnitude*	SIGN OUT	OUT RTN	REF OUT	OUT RTN
Modified Sign/Magnitude*	SIGN OUT	OUT RTN	OUT RET	OUT RTN

*Sign Bit = B1

Table 1. Code Selection.

*For offset binary and two's complement operation, the CODE SET input connects a voltage available on the module to the 16th resistor in the network, offsetting the output by ½ LSB and thus avoiding the "+0V" and "–0V" codes implicit in sign/magnitude operation. The MP1926's offset control is factory adjusted to make this 17th bit offsetting transparent to the user who is supplying offset binary or 2's complement codes. To set up for sign/magnitude input coding, see the calibration procedure.

Output Range Selection

Outputs from the module have a low impedance and can drive up to 5 mA. The user may select the desired output voltage range by setting the gain of the Output Amplifier via the RANGE SET input. To select an output range of ±5V (10V FSR), connect RANGE SET to the bipolar OUTPUT. To select ±10V output range (20V FSR), connect RANGE SET to OUTPUT RETURN, and use ±15V power supplies.

Calibration

For audio and telecommunication applications, offset and range recalibration will rarely, if ever, be required. However, the module should be recalibrated whenever the full scale range is changed.

Comments

1. Interconnect the MP1926 per the application. Apply power and allow 5 minutes for warm-up.
2. Readjust the OFFSET control before readjusting the GAIN (range) control.
3. Refer to Table 2 for the corresponding codes and voltages.

Bipolar Zero Offset Adjustment Procedure

1. If supplying Offset Binary or 2's Complement input code, apply the code corresponding to zero while adjusting the OFFSET control so that the output is 0V ± the tolerance required for the application.
2. If supplying Sign/Magnitude or Modified Sign/Magnitude code:
a. Alternately apply the codes corresponding to +0V and −0V;
b. While so doing, adjust the OFFSET control so that the average value of these two outputs if 0V. (these two outputs will typically differ by less than 2 ppm.)

Range Adjustment Procedure

1. Apply a code corresponding to the largest voltage for which the absolute value is critical.
2. Adjust the GAIN control so that the output equals the corresponding voltage to within the application tolerance.

B1, B2, . . . , B15, B16	Bipolar Output
Offset Binary	
1 111 111 111 111 111	+4.999847V
1 000 000 000 000 000	0.000000V
0 000 000 000 000 000	−5.000000V
Two's Complement	
0 111 111 111 111 111	+4.999847V
0 000 000 000 000 000	0.000000V
1 000 000 000 000 000	−5.000000V
Sign/Magnitude	
1 111 111 111 111 111	+4.999847V
1 000 000 000 000 000	+0.000000V
0 000 000 000 000 000	−0.000000V
0 111 111 111 111 111	−4.999847V
Modified Sign/Magnitude	
0 111 111 111 111 111	+4.999847V
0 000 000 000 000 000	+0.000000V
1 000 000 000 000 000	−0.000000V
1 111 111 111 111 111	−4.999847V

Notes
For ±5V FSR, 1 LSB = 153μV
For ±10V FSR, multiply above voltages by 2.

Table 2. Input Coding.

TYPICAL APPLICATIONS

Professional Audio Systems

Figure 4 illustrates the highest performance, yet lowest cost solution available to the problem of simultaneously updating a stereo pair of analog outputs at rates up to 55 kHz from 16-bit resolution data. A conventional implementation would require two D/A converters, with digital double buffering for simultaneous update, feeding two output deglitch amplifiers. The MP1926A, with a voltage settling time of only 5 μs, allows two channels to be updated from a single D/A converter within the 18 μs available. The only buffering required for simultaneous updating can be provided by an AH201-1 Distortion Suppressor (Z1 in Figure 4.) The very low feedthrough (−100 dB) of the AH201-1 allows Channel 1 to be held while the MP1926A outputs Channel 2 data with negligible effect on Channel 1.

A deglitcher is always required at the output of D/A converter in audio aplications to minimize harmonic distortion. The AH201 is a deglitch amplifier designed specifically for use with the MP1926A in these applications. The Channel 2 AH201-2 deglitches by momentarily holding its output at ground during the time that the MP1926A is updating Channel 2. The Channel 1 AH201-2 holds its output at ground during the time that the AH201-1 is switching (see timing diagram). The response of the AH201 is time constant controlled (RC = 2 μs) to pass full power 20 kHz sine waves without output slew rate limiting (and subsequent distortion). The overall harmonic distortion of this configuration has been measured to be less than 0.005% (0.0005 dB!) over the frequency range of 20 Hz to 20 kHz.

For applications in which sequential updating of the outputs is acceptable, the AH201-1 shown in Figure 4 may be ommitted. Each half of the AH201-2 would be sequentially updated, coincident wih the D/A update of its channel data. Also, depending on the application, units may be driven from a single MP1926A.

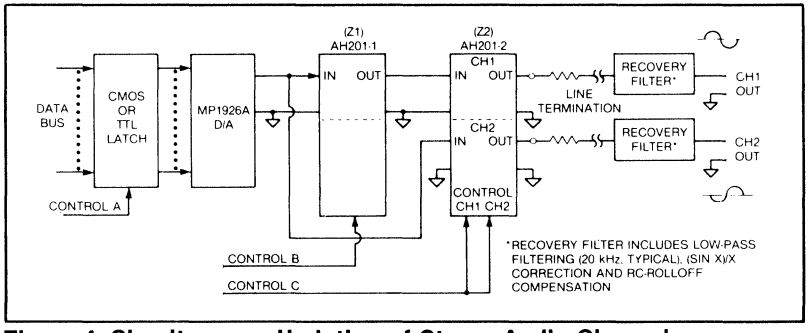


Figure 4. Simultaneous Updating of Stereo Audio Channels.

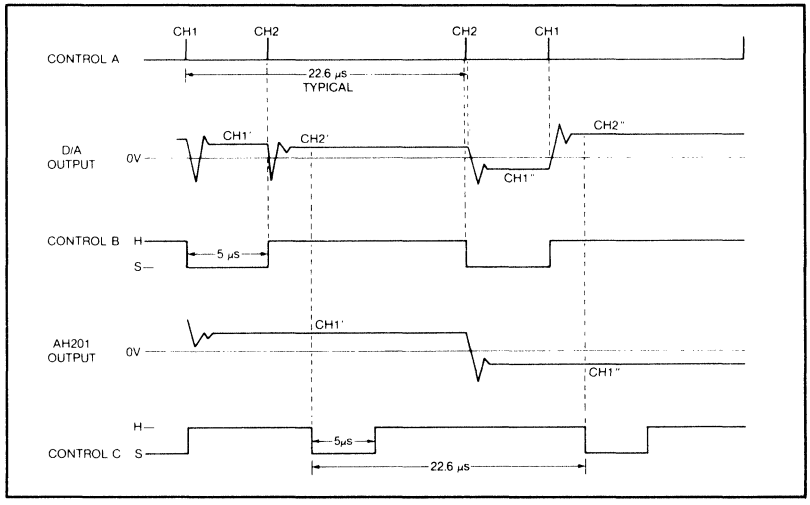
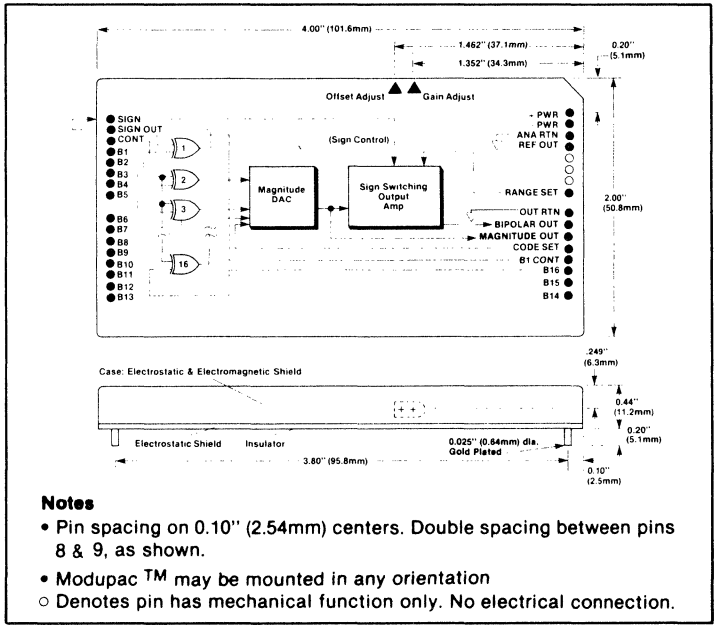


Figure 5. Typical Timing for Figure 4.



Notes

- Pin spacing on 0.10" (2.54mm) centers. Double spacing between pins 8 & 9, as shown.
- Modupac ™ may be mounted in any orientation

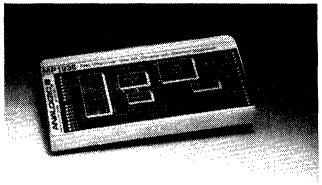
○ Denotes pin has mechanical function only. No electrical connection.

Figure 6. Mechanical & Pinout.

ORDERING GUIDE

For 3 μs settling time: Specify **MP1926A**

For 2 ppm of READING/°C gain stability: Specify **MP1926S**



ANALOGIC®

MP1936

Ultra-Low Harmonic Distortion
Multi-Year Stable, Low Cost
16-Bit D/A Converter with Distortion Suppressor

Description

The MP1936 combines an ultra-linear, bi-polar digital-to-analog conversion circuit with a controlled time constant distortion suppressor, providing in one low-cost module complete capability for restoring digitized signals to analog form with less than 0.005% harmonic distortion (less than −86 dB, worst case). A complete, fully-tested subsystem needing no external parts or adjustments, this module requires less total component and assembly expense, pc board area, and power than do subsystems based on integrated circuit DAC's. Nevertheless, it provides superior low-level performance essential to quality telecommunications, satellite program distribution, and other ac-coupled applications requiring wide dynamic range. As an example, for a 1 kHz tone at the commonly measured level of −41 dB down from full scale, peak line distortion is down by −50 dB (−91 dB relative to full scale)!

The D/A and distortion suppression circuits are based on the Analogic professional audio DAC and professional audio distortion suppressor (MP1926A* and MP201A*, respectively), but are optimized within a single shielded and tested module

(continued)

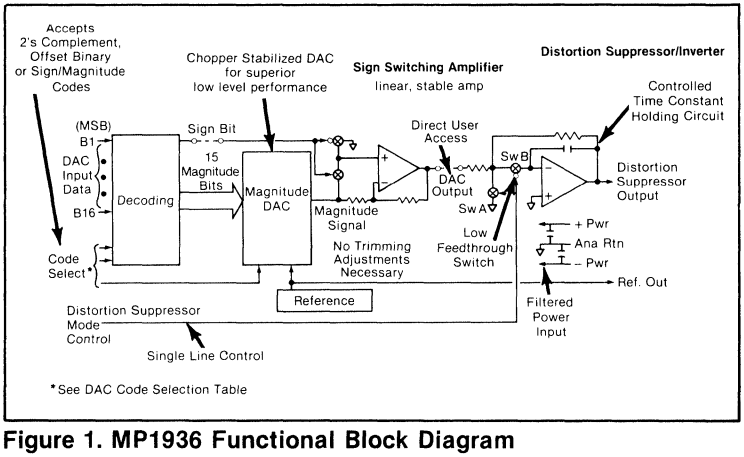


Figure 1. MP1936 Functional Block Diagram

Features

- **Ultra-Low Harmonic Distortion**
  For full scale signals:
  −86 dB worst case 20 Hz to 20 kHz
  For low level signals:
  −50 dB max. for a 1 kHz tone @ −41 dB below peak
- **High Speed**
  Up to 128,000 updates/sec Wide bandwidth for multiple high fidelity or voice grade channels
- **Ultra Low Noise**
  −110 dB (less than 1 LSB)
- **Low Cost**
  No external components
  Minimized board space
  Adjustment-free operation
- **Ultra Stable**
  3-year, no-adjustment differential linearity of ±25 ppm FSR, *better than the 3-month performance of higher-priced converters*
  Differential linearity tempco of ±0.25 ppm FSR/°C
- **Environmentally Rugged**
  128,700 hour MTBF (>14 years)
  Operates −25°C to +85°C EMI & RFI shielded
- **Low Power**
  <430 mW
- **Flexible**
  ±9V to ±15V power supply
  TTL or CMOS inputs
  Offset binary, 2's complement, or sign/magnitude input codes
- **Easy to Use**
  DAC updates upon code change
  Deglitcher controlled by single line
  Compatible with industry standard MP1926A professional audio DAC

Applications

- **Telecommunications Decoding**
  Satellite Earth Stations
  Terrestrial Channel Bank Equipment
  Studio Transmission Links (STL's)
  Terrestrial Audio PCM Systems
- **High Accuracy Bipolar Data Translating**
  Waveform Synthesizers
  Testers for Consumer Grade Digital Audio Systems

SPECIFICATIONS

BIPOLAR OUTPUT

Full Scale Voltage Range (FSR)
±5V nom.

Load Current
±5 mA max., (DAC w/Distortion Suppressor[1] — ±20 mA max.)

Output Impedance @ dc
0.1Ω max.

Output Fault Protection
Indefinite short to ground

ACCURACY @ 25°C, nom.

Peak Line Harmonic Distortion[2]

Fundamental @ ±5V; 20 Hz through 20 kHz
N/A, (DAC w/Distortion Suppressor[1] — Down from fundamental by at least −86 dB)

Fundamental −41 dB down @ 1 kHz
N/A, (DAC w/Distortion Suppressor[1] — Down from fundamental by at least −50 dB)

Total Non-Linearity[3]
For Midrange Outputs Centered About Zero Volts (¼ FSR):
Initially
±4 ppm FSR max., (±2 ppm FSR typ.)

After 3 years (calculated)
±25 ppm FSR max.

Over the Full Scale Range
±15 ppm FSR max., (DAC w/Distortion Suppressor[1] — ±25 ppm FSR max.)

Absolute Range (Gain) Accuracy
±0.01 dB (±0.1%), (DAC w/Distortion Suppressor[1] — ±0.2 dB (±2%)

Offset Voltage
±20 mV max., (DAC w/Distortion Suppressor[1] — ±30 mV max.)

Zero Code 0°C to 70°C
Continuous and monotonic through zero

Noise[4] (referenced to rms full scale)
−113 dB rms, (DAC w/Distortion Suppressor[1] — −110 dB rms)

STABILITY

Tempco of Differential Non-Linearity
For Midrange Outputs Centered About Zero Volts (¼ FSR)
±1 ppm FSR/°C max.
(±0.25 ppm FSR/°C typ.)

Over the Full Scale Range
±2 ppm FSR/°C max., (±0.5 ppm FSR/°C typ.)

Tempco of Gain (0°C to 70°C average; includes reference)[5]
±30 ppm of READING/°C max., (±10 ppm of READING/°C typ.), (DAC w/Distortion Suppressor[1] — ±50 ppm of READING/°C max., (±20 ppm of READING/°C typ.))

Tempco of Offset Voltage[6]
±5 ppm FSR/°C max., (DAC w/Distortion Suppressor[1] — ±7 ppm FSR/°C max.)

Power Supply Sensitivity
Range (Gain)
20 ppm FSR/V

Offset
35 μV/V

Time Stability
see Non-Linearity spec

Warm-Up Time to Specified Accuracy
3 minutes max.

TRANSFER CHARACTERISTICS

Frequency Response[7]
N/A, ((DAC w/Distortion Suppressor[1] — See Theory of Operation)

Settling Time for 5 Volt Step
To 0.01%
3.5 μs, (DAC w/Distortion Suppressor[1] — N/A)

To 1 LSB
6 μs, (DAC w/Distortion Suppressor[1] — N/A)

To Desired Gain Accuracy
N/A, (DAC w/Distortion Suppressor[1] — Determined by time constant (τ) and system timing (3.4 μs τ std.; consult factory for other τ's))

Slew Rate
7.5 V/μs min., (DAC w/Distortion Suppressor[1] — Time constant limited response)

INTERNAL REFERENCE

Nominal Voltage
+5 V

DC Output Impedance
0.1Ω max.

Load Current
1 mA max.

DIGITAL INPUTS

Definition
16 data bits per Decoding Table, (Distortion Suppressor — 1 Mode Control signal

Logic Compatibility
CMOS
5V only, (Distortion Suppressor — N/A)

TTL
With external pull-up to +5V supply, (Distortion Suppressor — TTL)

Low Level
0V to +1V (FALSE), (Distortion Suppressor — 0V to +0.5V (ON))

High Level
+4V to +5V (TRUE), (Distortion Suppressor — +3V to +5V (OFF))

Required Rise and Fall Time
N/A, (Distortion Suppressor — 5 ns max.)

POWER REQUIREMENT[8]

Nominal Voltage
±9V to ±15V

Absolute Max.
±16V

Current, Exclusive of Load
±23 mA typ.

Dissipation @ ±9V, Exclusive of Load
430 mW max.

Dissipation @ ±15V, Exclusive of Load
750 mW max.

ENVIRONMENT

Rated Performance
0°C to 70°C

Operating Temperature Range
−25°C to +85°

Storage Temperature Range
−55°C to +85°C

Relative Humidity
0 to 85%, non-condensing, up to 40°C

PACKAGING (Modupac™)

Dimensions, Inches (mm rounded)
2" X 4" x 0.44"
(50.8 mm x 101.6 mm x 11.2 mm)

Electromagnetic Shielding
5 sides

Electrostatic Shielding
6 sides

NOTES

1. These specifications apply when the distortion suppressor and the DAC are used in combination per Figure 1. For distortion suppressor-only specifications, consult factory.
2. Peak line harmonic distortion as measured by spectrum analyzer with 100 Hz bandwidth @ 25°C nominal; specification assumes that interconnections and timing for DAC and distortion suppressor are per recommendations.
3. Deviation from best straight line.
4. 20 kHz bandwidth, measured with a distortion suppressor duty cycle of 50% and 50 kHz sampling frequency. Noise in OFF mode is 3 dB greater than in ON mode.
5. For bipolar signals, X ppm of READING is less than or equal to X/2 ppm of FSR, *e.g.,* 2 ppm of READING ≤1 ppm FSR.
6. Total at 0V, not affected by reference drift.
7. For flat system frequency response, post filtering that follows the distortion suppressor should include a zero at 46 kHz to cancel the pole that exists at 46 kHz in the distortion suppressor. It should also compensate for the (sin x)/x attenuation that is introduced by any sampled data process. For related information, see the Analogic Data Conversion Systems Digest, Ed. 4, esp. pp. 160-162, 215-217, 223 and 224.
8. Analog Return, Output Return, and Case are tied internally.

Description (cont.)

for low cost systems that require long term stability exceeding several years. Accepting a variety of standard input codes, the DAC circuit employs a proprietary (pat. pending) internal sign/magnitude architecture that provides better than 18-bit linearity for signals in the critical zero crossover region (±⅛ full scale range), yet offers 3.5 μs settling time to 0.01% of a 5V step — a speed sufficient for multiple broadcast-grade channels. In this internal architecture, the most significant bit weighting resistances make no contribution to small signals. This contrasts dramatically with the commonly-used offset binary architecture, in which a heavily weighted resistor predominates at midrange, enabling even small resistor errors and drifts to degrade midrange linearity by the equivalent of several bits and to cause large zero crossover distortions. Low sensitivity to resistor error, combined with high-quality stabilized resistors, renders the differential linearity of the MP1936 for signals more than 18 dB down virtually immune to temperature changes (typically less than 1 LSB of drift over a 60°C span) and yields a three-year no adjustment differential linearity drift of *less than* ±25 ppm, meeting the critical long-term fidelity criteria and economic goals established for many unattended remote communication stations.

The distortion suppressor — used to sample the DAC's output value and then hold it while the DAC is being switched to a new value — suppresses the DAC's code-dependent switching glitches.* Its 3.4 μs output time constant prevents slew-rate-limiting output distortions, yet provides full power response for signals up to 46 kHz in the sampling mode. This unique amplifier has been specifically developed for low-distortion applications, because conventional sample and hold circuits commonly used as deglitchers have been found to distort high-frequency or high-amplitude signals.

High speed, low noise and low distortion over the dynamic range from peak power to studio quiet, ease of use including CMOS and TTL logic compatibility, and wide environmental latitude qualify the MP1936 for many of the most demanding digital communication applications.

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*In general, applications will incorporate a recovery filter to compensate for both the (sin x)/x attenuation introduced by the sampling process and the frequency-dependent attenuation (rolloff) introduced by the distortion suppressor's time constant limited response.

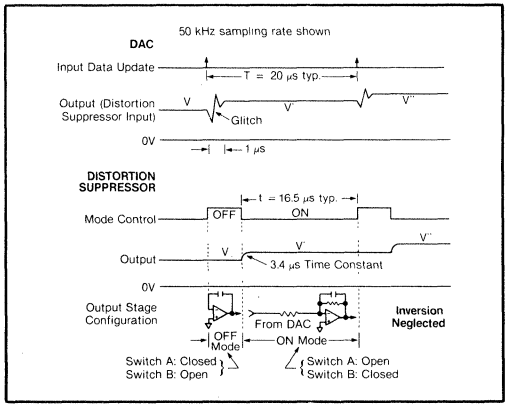
SYSTEM PERFORMANCE FEATURES

An internal sign/magnitude architecture provides accurate large signal performance and superior low level performance, particularly when compared to the commonly used offset binary internal architecture. A complete modular subsystem based on this approach, the MP1936 conserves pc board area, power, and design & production expense when compared to circuits based on offset binary IC converters, making it easy to use in many applications.

Optimized for Audio Applications

Analogic instrumentation grade converters have served the needs of digital audio system designers for over a decade. In the late 1970's, to meet their expressed needs for lower-cost, optimized converters, a high-speed sign/magnitude architecture was developed. This architecture is particularly suited to reconstructing dynamic complex waveforms, such as speech or music, that: 1) have a substantial amount of their information content in the vicinity of "zero volts" (midrange on a bipolar scale), and 2) may occasionally peak well above the rms level.

Differential linearity in the region near zero has been identified as the critical parameter for such signals. With the commonly used offset binary architecture, which produces a bipolar output by offsetting an internal unipolar signal by one half full scale, even a small error in the offsetting resistor can frequently cause relatively large differential linearity errors near zero volts. Further, for a zero crossing, all bit-weighting resistors are switched, further degrading differential linearity and increasing susceptibility to harmonic distortion, granularity noise, and similar audio artifacts. These effects are often magnified by the ±15 ppm/year to ±100 ppm/year tracking ratio drift of many commonly used bit-weighting resistors. Thus, *all offset binary converters are virtually useless in the critical audio region after a short time in the field.*



In contrast, with a sign/magnitude internal architecture, step size error decreases as the signal approaches zero volts from either direction, and no current-weighting resistors are switched for a zero crossing.* In the MP1936, the six most significant current-weighting resistors make no contribution to signals that are down by −41 dB or more from peak full scale, ensuring ultra-linear performance in the most critical audio range. This basic architectural advantage, coupled with over a decade of experience in the manufacture of precision data converters, makes this module optimum for high quality, low cost communication applications. Even for outputs larger than −18 dB, the increment between codes equals the LSB step size of 15 ppm FSR plus a differential nonlinearity of only +13/−9 ppm FSR, ensuring both monotonicity and no missing steps over the entire output range.

A Complete Modular Subsystem

Traditionally, designers and manufacturers of telecommunications systems have been required to select separate DAC and deglitch circuits, test each one, then mate them and test the combination. Further, most high resolution integrated circuit DAC's commonly available in the audio speed range require an external reference supply, multiple external operational amplifiers, power supply decoupling capacitors, and trimming potentiometers — consuming equal or more printed circuit board area than does the MP1936. In addition, they frequently require tedious and expensive offset zeroing operations via the external potentiometers, with questionable stability and reliability.

NOTE: A time-constant limited response affects all input voltage changes in the same proportion as long as the settling time allowed is constant. For this example, the ON time of 16.5 µs (approximately 5 time constants) results in a gain error of 0.1 dB. If required, this gain reduction can be corrected by the system's gain adjustment.

*For more details on the applicability of the sign/magnitude architecture to audio systems, consult your Analogic Representative.

The MP1936, on the other hand, requires no external potentiometers. Its stability obviates the need for routine linearity, gain, or offset adjustments, increasing reliability and decreasing field support cost. As a completely engineered subsystem, the MP1936 conserves user design time significantly; as a fully assembled and tested subsystem, it conserves production labor cost as well as component cost when compared to the total cost of an IC-based equivalent subsystem.

Using the MP1936

The MP1936 provides decoding and interconnect flexibility as well as control simplicity, facilitating use in a variety of applications.

Input Decoding The MP1936's digital-to-analog converter may be connected to accept any one of four input code types: offset binary, two's complement, sign/magnitude, or modified sign/magnitude. The input data is automatically converted, if necessary, to the sign/magnitude code used internally—the user need only interconnect the module per the Code Selection Table.

Note that the Input Decoding Table defines the transfer function of the DAC only; the distortion suppressor inverts the DAC's output. (The table is presented on a DAC-only basis for consistency among applications, independent of the number and type of post-DAC processing channels.)

Control Only the input data and one control line are needed to operate the MP1936. The DAC updates upon receipt of each new code word—no separate selection or enable signals are required. Per the Typical Timing Diagram, the control line is used to select the distortion suppressor's mode: a logical zero places this amplifier in the ON (input connected) mode; a logical one places it in the OFF (input disconnected) mode. Recommended switching rates are from 5 kHz to 128 kHz.

Interconnect Flexibility The DAC's output and the distortion suppressor's input are both available to the user on external pins, providing for special purpose processing and multiple-channel hookups (see Typical Applications). It is recommended that MP201A Distortion Suppressors be used to deglitch any additional channels that use the same DAC. The primary circuit in that module is essentially identical to the MP1936's distortion suppressor, ensuring identical performance in all channels.

Logic Compatibility The digital data may be supplied via either CMOS or TTL devices. However, if TTL is used, an external pull up resistor to +5V is needed on each data input line. The distortion suppressor's mode control input must be TTL.

Power Supply The MP1936 operates from a bipolar supply at any voltage from ±9V to ±15V. Thus the module may be isolated from the system's ±15V supplies via simple regulators.

Interchangeability The mechanical dimensions of the MP1936 are identical to those of the industry standard professional audio DAC, the MP1926A, and the pinouts are nearly identical. MP1926A users who wish to convert to the MP1936 may do so with a minimum of external jumpers. For related information, consult your Analogic Representative.

THEORY OF OPERATION

D/A Converter

Figure 2 shows the theoretical transfer function of a sign/magnitude digital-to-analog converter (DAC). Per Figure 1, this is implemented by first decoding the digital input word (converting it to the sign/magnitude code used internally), then: 1) applying the 15 LSB's to a magnitude DAC and 2) applying the MSB (sign bit) to configure an amplifier that either follows or inverts the magnitude signal.

The classical problem of attaining both low offset drift and high speed simultaneously from a sign/magnitude circuit has been solved by using a unique amplifier in the Magnitude DAC. (An offset error in the magnitude signal would cause a discontinuity whenever the sign switches at a zero crossing, and would cause the output to be asymmetric about 0V.) Earlier sign/magnitude approaches have met this low offset requirement by using slow amplifiers, limiting their applicability. The MP1936's magnitude amplifier is both chopper stabilized and fast. Offset drift of this amplifier is an extremely low 1 μV/°C, yet settling time to 1 LSB, including the sign switching amplifier, is only 6 μs. The MP1936's performance is, therefore, symmetric about zero yet fast enough for quality audio applications.

Distortion Suppressor

All digital-to-analog converters, including the MP1936's Magnitude DAC, generate some dynamic distortion while they are being updated from one "steady-state" value to

another. This distortion results primarily from code-dependent switching glitches associated with the DAC's current-weighting network. To reject these glitches, the distortion suppressor uses a holding capacitor and a pair of high-quality analog switches in addition to an inverting amplifier (Figure 1). The switches select one of two modes, as follows:

When the DAC output has settled to some desired value, the distortion suppressor is commanded to the ON mode: shunt switch "A" opens and series switch "B" closes, connecting the settled DAC output to the distortion suppressor's output. In this mode the distortion suppressor's output response is exponential, with the 3.4 μs time constant provided by the holding capacitor and feedback resistor being sufficient to avoid slew rate limiting effects for up to ±5V signals.*

When the DAC is updating to a new value, the distortion suppressor is commanded into the OFF mode: the switch positions reverse, shunting the changing DAC output signal to ground and allowing the previous DAC output level, now stored on the holding capacitor, to continue as the distortion suppressor's output. In this mode, its output is isolated from the DAC's transients. (Feedthrough of a ±5V sine wave injected at the distortion suppressor's input pin during this mode is typically down −90 dB!)

When the distortion suppressor is switched between its two modes, it will pass signals up to 20 kHz without introducing noticeable distortion. For example, the peak line distortion for a full amplitude sine wave at 20 kHz (switching rate = 50 kHz) is −86 dB with respect to the ±5V level! Clearly, the transfer function of this circuit is related to both the ON time (t_O) and the sampling period (T) chosen for operation. The theoretical relative frequency response can be obtained by taking the convolution of the transfer functions of the two circuit configurations shown at the bottom of the Typical Timing Diagram. At dc, the distortion suppressor's gain is −1. The transfer function is included in an application note available from your Analogic Representative.

*Other time constants available — consult factory.

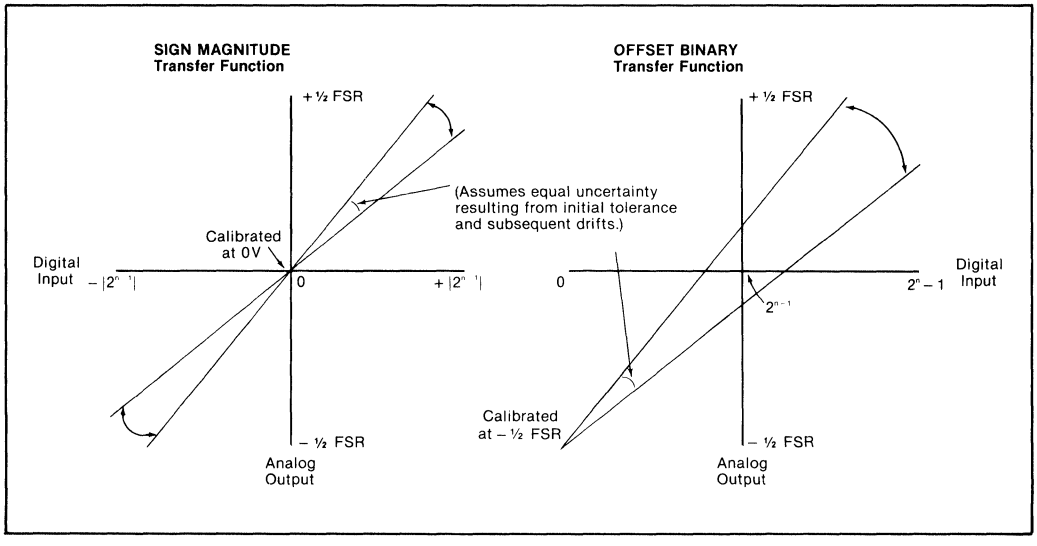


Figure 2. Comparison of Performance Near Zero The transfer function of a converter using an internal sign/magnitude approach originates at 0V (all current switches off), so the 0V output is not affected by linearity or gain drifts. With an offset binary approach, the transfer function originates at −½ FSR (all current switches off), and any linearity or gain drift will shift the 0V output as shown.

TYPICAL APPLICATIONS

Stereo Broadcast Link

Figure 3 illustrates a high performance, yet low cost method for simultaneously updating a stereo pair of analog outputs, at rates up to 55 kHz, from 16-bit resolution data (98 dB dynamic range). A conventional implementation would require two DAC's plus digital buffering to achieve simultaneous updating. The MP1936, with a voltage settling time of only 6 μs to 1 LSB for a large step, allows both channels to be updated from a single DAC within the 18 μs available. The only buffering required for simultaneous updating can be provided by an additional, external distortion suppressor such as the Analogic AH201-1.

The timing diagram shows that the S/H samples the DAC's output during a time slot assigned to Channel 1. It then holds this new Channel 1 level while the DAC output settles to a new Channel 2 level. Due to the AH201's low feedthrough in the HOLD mode, the Channel 2 information and glitches will have negligible effect on Channel 1. When the inputs to the distortion suppressor and the first AH201 contain stable new data, both of these circuits are switched ON, causing both channels to be updated simultaneously.*

*For more complete implementation information, consult your Analogic Representative.

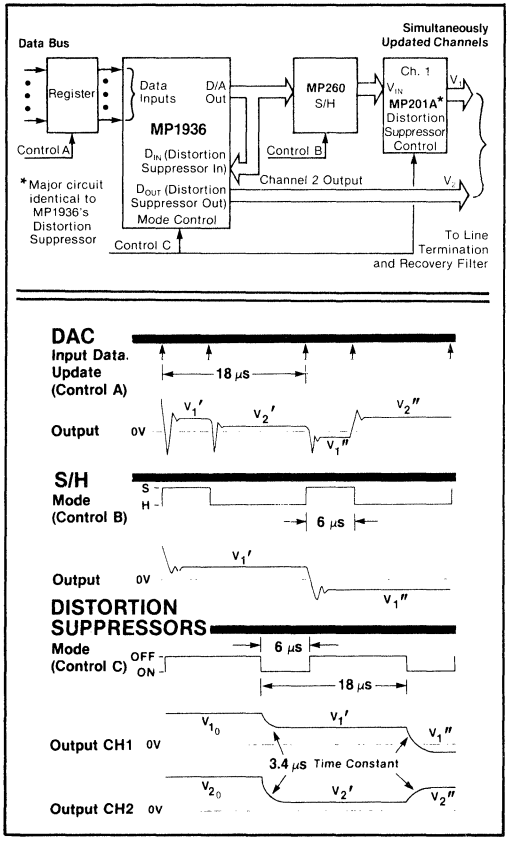


Figure 3. Simultaneous Updating of Stereo Audio Channels with a single D/A @ 55 kHz sampling rate per channel and 16-bit resolution.

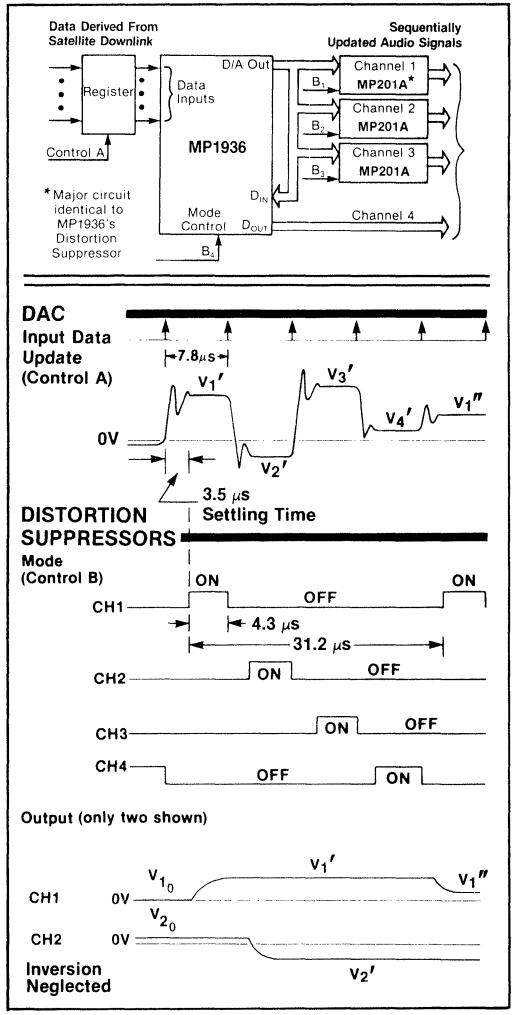


Figure 4. Non-Simultaneous Updating of Multiple Audio Channels *with a single D/A* @ 15 kHz bandwidth per channel (16-bits of resolution).

Satellite Downlink

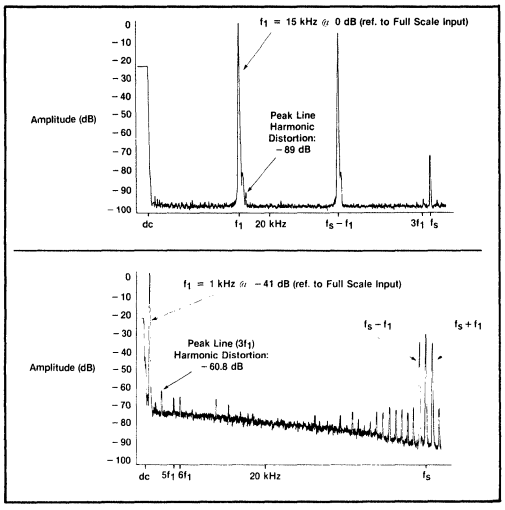
The MP1936 also provides an economical method for restoring channels sequentially. For example, a satellite ground station used in a program channel distribution service would be required to update multiple audio outputs, but not necessarily simultaneously. Figure 4 illustrates one possible implementation using a single DAC to sequentially update four, 15 kHz bandwidth, audio channels. A nominal 32 kHz sampling rate per channel is assumed. This means that the DAC must update four channels every 31.2 μs or one channel every 7.8 μs, which is well within the settling capability of the MP1936. The distortion suppressor in each channel is simply turned on for the last 4.3 μs of the corresponding MP1936 update period.

Performance In An Audio Sampled Data System

A complete digital audio system — using an Analogic SHAD-2 A/D conversionsystem* for digitally encoding analog input signals and an MP1936 for decoding the digital data to recover them — has been evaluated. The spectral analyses presented here indicate that end-to-end performance of the total system is well within the fidelity criteria of studio transmission links for both low level and high level signals.

The peak harmonic distortion measured for high frequency, full scale signal was only −89 dB (−101 dB referenced to full scale). These measurements show the accumulated effects of distortion produced by all of the components in the audio sampled data system as well as by the input signal generator used. Thus it is reasonable to conclude that the performance of the MP1936 alone during these test runs was signficantly better than the −89 dB and −60 dB measured for the total system!

On the basis of these tests, MP1936 performance exceeded the specifications (−86 dB and −50 dB) notably, a characteristic not uncommon with Analogic products. The unit tested was selected from a production prototype lot. As the MP1936 has no external adjustments, no special tweaking was performed for these tests; the results shown here may be considered representative of typical, adjustment-free audio fidelity.



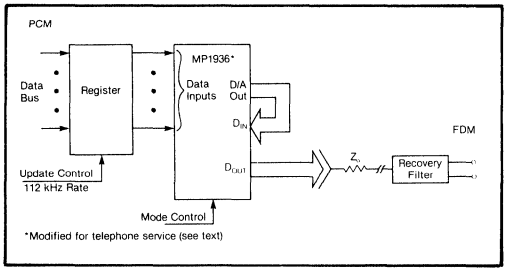
Spectrum Analyzer Recordings (100 Hz bandwidth) for Reconstructed Sine Wave Signals. For a high frequency, full scale test tone, the largest harmonic measured in the 20 Hz to 20 kHz band was −89.0 dB; for a low-level tone, the largest harmonic in this band was −60.8 dB. Filtering was not used in this test. In most applications, output filtering would remove the components above 20 kHz, including those which result from foldback on the sampling frequency, f_S.

*The SHAD-2 provides 98 dB (16-bit) dynamic range at low cost via an MP282A Dual Channel Sample and Hold (with 1-bit automatic gain ranging) and an MP2735-2 Low Distortion 15-Bit Analog-to-Digital Converter. It incorporates these two modules, plus control logic for simultaneously updating two channels, within a compact 4.62" x 5.78" (117 mm x 147 mm) printed circuit board. For more information on Analogic audio PCM products, consult your Analogic Representative; for a detailed summary of end-to-end system tests that used the MP1936's decoding architecture, ask for a reprint of "A New, Ultra Linear 16-Bit Digital-to-Analog Conversion System for Professional Audio," by Albert A. Sanchez.

Telephone Group Set PCM/FDM Conversion

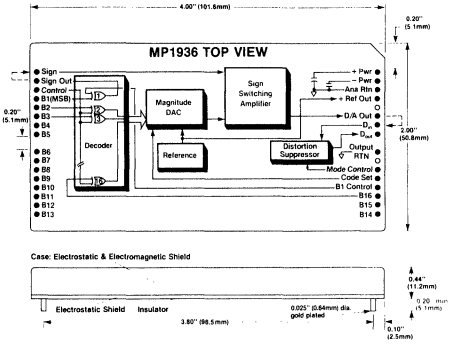
The output frequency band in a pulse code modulation (PCM)/frequency division multiplexed (FDM) telephone baseband group is 60 kHz to 108 kHz, with a data update rate of 112 kHz. To minimize the amount of (sin x)/x correction required and to reduce the energy present at the sampling frequency, the distortion suppressor may be modified (consult the factory) to switch its input between ground and the newly settled DAC output, rather than between a stored level and the newly settled DAC output. Switching to ground is coincident with the update of the DAC; typically t_o

may be ¼ to ½ of T. The large dynamic range and low distortion of the MP1936 result in negligibly low crosstalk. Measured under standard telephone conditions, the noise power ratio (NPR) is better than 64 dB when tested in a loop back system.



PCM/FDM Telephone Application

MOUNTING DIMENSIONS & PINOUTS



Notes

- Pin spacing on 0.10" (2.54 mm) centers.
- Modupac™ may be mounted in any orientation

○ Denotes pin has mechanical function only. No electrical connection.

Offset Binary	
B1, B2, ..., B15, B16	Bipolar Output
1 111 111 111 111 111	+ 4.999847 V
1 000 000 000 000 000	0.000000 V
0 000 000 000 000 000	– 5.000000 V

Two's Complement	
B1, B2, ..., B15, B16	Bipolar Output
0 111 111 111 111 111	+ 4.999847 V
0 000 000 000 000 000	0.000000 V
1 000 000 000 000 000	– 5.000000 V

Sign/Magnitude	
B1, B2, ..., B15, B16	Bipolar Output
1 111 111 111 111 111	+ 4.999847 V
1 000 000 000 000 000	+ 0.000000 V
0 000 000 000 000 000	– 0.000000 V
0 111 111 111 111 111	– 4.999847 V

Modified Sign/Magnitude	
B1, B2, ..., B15, B16	Bipolar Output
0 111 111 111 111 111	+ 4.999847 V
0 000 000 000 000 000	+ 0.000000 V
1 000 000 000 000 000	– 0.000000 V
1 111 111 111 111 111	– 4.999847 V

D/A Converter Input Decoding*

*This table defines the transfer function of the sign/magnitude D/A conversion circuit only. Note that the distortion suppressor circuit inverts the polarity of the D/A OUT signal.

	MODULE CONNECTIONS			
CODE	SIGN to	CONTROL to	B1 CONTROL to	CODE SET to
Offset Binary	SIGN OUT	SIGN OUT	REF OUT	REF OUT
2's Complement	SIGN OUT	SIGN OUT	OUT RET	REF OUT
Sign/Magnitude*	SIGN OUT	OUT RTN	REF OUT	OUT RTN
Modified Sign/Magnitude*	SIGN OUT	OUT RTN	OUT RET	OUT RTN

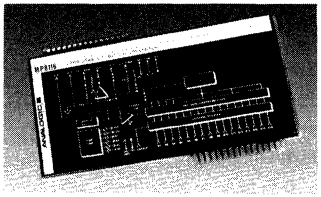
*Sign Bit = B1

DAC Code Selection Table

ORDERING GUIDE

For digital-to-analog decoding with low distortion over a 98 dB dynamic range, Specify □ **MP1936**

For a complete family of digital audio data conversion/ translation building blocks, consult your Analogic representative.



ANALOGIC®

MP8116

16-Bit D/A Converter

Description

The MP8116 is the ultimate in precision, high stability, 16-bit digital-to-analog converters. Originally developed for nuclear physics experimentation applications, the MP8116 is ideally suited for any application where differential linearity, accuracy and stability over time and temperature are critical.

The MP8116 features both Relative Accuracy and Differential Non-Linearity of better than 0.25 LSB. Tempco of Differential Non-Linearity is an outstanding 0.25 ppm/°C maximum, giving the MP8116 solid 16-bit accuracy over a full 30°C temperature range. All other parameters are commensurate with this level of performance, thus making the MP8116 the ultimate in precision and stability.

Features

- True 16-bit accuracy
  ±0.25 LSB maximum Relative Accuracy
  ±0.25 LSB maximum Differential Non-Linearity
- Exceptional Temperature Stability
  0.25 ppm/°C Differential Non-Linearity Tempco
- Separate Analog and Digital Grounds
- Dual-Feedback Load Sensing
- Low Power Dissipation

Applications

- Automatic Test Equipment
- Calibration Standards
- Laser-trimming and Scribing Systems
- Profilers
- Phototypesetting
- Digitally controlled Power Supplies
- Precision Function Generation

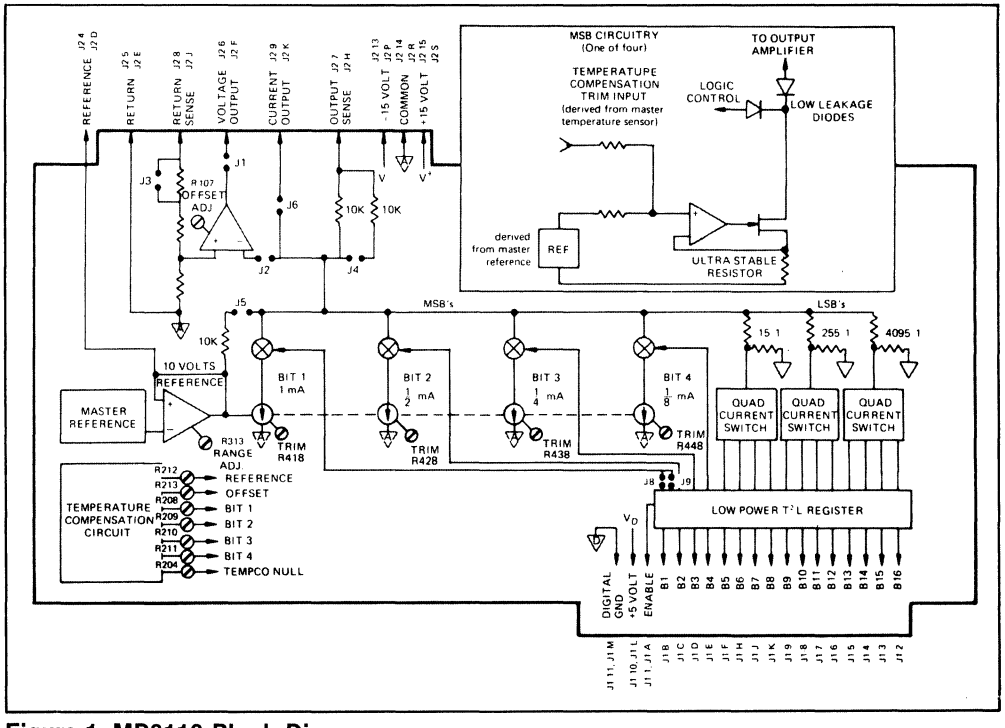


Figure 1. MP8116 Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG OUTPUTS

Fault Protection
Outputs may be short-circuited to ground indefinitely

VOLTAGE MODE

Full-Scale Ranges
±10.00000V, ±5.00000V and 0V to +10.00000V; determined at time of order

Output Impedance
<0.1Ω at dc

Output Configuration
Balanced 4-wire for remote sensing

Load Current
2 mA maximum

Settling Time
25 μs maximum to ½ LSB for full scale step

Slew Rate
18 V/μs minimum

CURRENT MODE

Full Scale Range
−1.00000 mA to +1.00000 mA (Bipolar); 0.00000 mA to −2.0000 mA (Unipolar)

Output Impedance
3.33 kΩ bipolar
5 kΩ unipolar

Voltage Compliance
±0.5V maximum

Settling Time
10 μs maximum to ½ LSB for full scale step

INTERNAL REFERENCE

Voltage Output
+10V nominal

Output Impedance
0.1Ω nominal

Output Load Current
1 mA maximum

ACCURACY

Absolute Accuracy
Relative Accuracy ±2 ppm NBS traceable

Relative Accuracy
±0.00022% FSR typical,
±0.00037% FSR maximum

Differential Non-Linearity
±0.00012% FSR typical,
±0.00037% FSR maximum

Noise
<1.5 ppm FSR rms typical, 3 ppm FSR rms maximum over 20 Hz to 100 kHz;

<1 ppm FSR, p-p typical, 2 ppm FSR p-p maximum from dc to 100 Hz

STABILITY (Tempco)

Differential Nonlinearity
±0.07 ppm/°C typical,
±0.25 ppm/°C maximum

Gain
±0.23 ppm/°C typical
±0.44 ppm/°C maximum

Offset
±2.3 μV/°C typical,
±5.6 μV/°C maximum

Power Supply Sensitivity
Offset
20 μV/V maximum

Gain
20 ppm/V maximum

Recommended Recalibration Interval
3 months

DIGITAL INPUTS

General
TTL compatible, one unit load Positive true

Coding
Binary or two's complement (specify when ordering)

ENABLE
Logic "1", output follows input data; logic "1" to "0" transition latches input data into registers

POWER REQUIREMENTS

+15V, ±3%
20 mA maximum

−15V, ±3%
50 mA maximum

+5V, ±5%
75 mA maximum

ENVIRONMENTAL AND MECHANICAL

Storage Temperature
−10°C to +85°C

Operating Temperature
+5°C to +70°C

Temperature Range for Rated Temperature Coefficients
+20°C to +35°C

Relative Humidity
5% to 90% non-condensing

Warm-up Time to Specified Performance
20 minutes

Dimensions
3.875" x 7.09" x 0.5" nominal
(98.4 x 180.2 x 12.7 mm)

Mating Connector
30 pin, 0.156" spacing;
Viking 2V K 15D/1-2 or equivalent
Two Analogic 15-300004 supplied

USING THE MP8116

General

Integration of the MP8116 in a system is relatively straight-forward. The separation of analog and digital grounds, the fourwire output load sensing, and both current and voltage output modes combine to allow maximum flexibility in implementation.

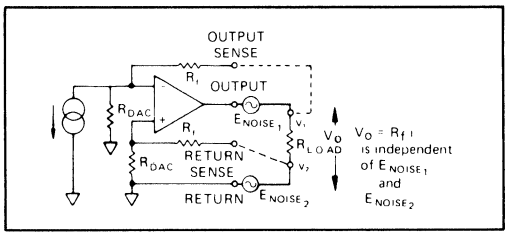


Figure 2. Voltage Output Circuit.

Digital Control

The digital input latches are 74L75 registers. When the ENABLE line is high, the output of the MP8116 will follow the data present at the inputs. When the ENABLE line is brought low, the data present at the inputs at the transition will be latched into the registers.

Digital Data

The coding of the digital data is selected at the time of ordering and cannot be changed by the user. Binary and two's complement coding can be accommodated.

Grounding

The Analog and Digital grounds in the MP8116 are totally separate. Depending on the application, the grounds can be maintained separated, or can be tied together at the MP8116 connector.

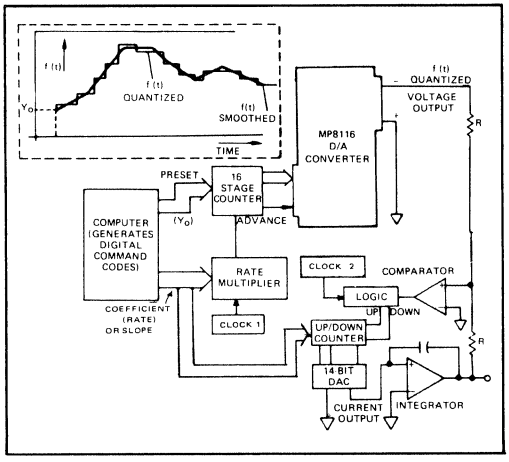


Figure 3. Function Generation.

Current Output

The current output full scale range is determined at the time of manufacture and is not user selectable. The MP8116 can be used in the current mode, even if a voltage mode version has been ordered. In this case, the current range will correspond to the voltage range, i.e. a unipolar current with a unipolar voltage range model, and a bipolar current output with a bipolar voltage range model.

Voltage Output

The voltage output full scale range must be determined at the time of ordering and is not user selectable. Full scale output ranges of 0V to +10V, ±10V and ±5V are accommodated.

Remote sensing capability of the load voltage is provided. Connect the load as shown in Figure 2.

TYPICAL APPLICATIONS

Figure 3 shows the MP8116 used as part of a function generator, the application for which it was originally developed. In this application, the DAC is used to program the current in the magnets of a particle accelerator. Open-loop programming of the DAC would cause small but intolerable "steps" in the generated current-time function, f(t), as shown in the insert. The circuit shown* achieves virtually perfect smoothing of the function, at high speeds, without introducing significant error.

In operation, the computer presets a 16-stage counter to the Y_0 intercept of the desired function, and also programs a rate multiplier to control the clock pulses that advance the counter. The counter state is the input code to the MP8116, so that the rate-multiplier coefficient actually establishes the slope of the function at any time. The output of the MP8116 is, then, the quantized value of f(t). A comparator then compares this quantized value with the smoothed value, which is derived from the output of an integrator. The input of the integrator is the output of the same MP8116 DAC, whose input code is generated

*This function generating technique is due to Dr. J. Bosser, (at CERN Geneva) whose cooperation we wish to acknowledge.

by the state of a presettable up-down counter. This up-down counter stores counts generated by logic driven by the output of the comparator. Thus, if the sensitivity of the comparator is of the order of ½ LSB (8 ppm of full scale), the integrator output will not be more than 1 LSB different from the quantized f(t), but the output f(t) is smoothed by the integration.

Testing Converters and Precision DVM's (Figure 4)

The MP8116 is the ideal device for testing and calibrating high-resolution D/A converters, A/D converters, and DVM's up to 5½ decimal digits, because of its high absolute accuracy and linearity. In figure 4 we show a digital programming source that might be anything from a set of 16 switches (for manual testing) to a digital computer, including test-program RAM, ROM, digital controllers, etc. The analog output of the MP8116 is then used as the input to the A/D Converter or DVM under test, and its output is then compared with the programmed input to the MP8116. (To test D/A converters, the digital code is fed to *both* the MP8116 and the DAC under test, and their analog outputs are compared in a null detector of adequate sensitivity.)

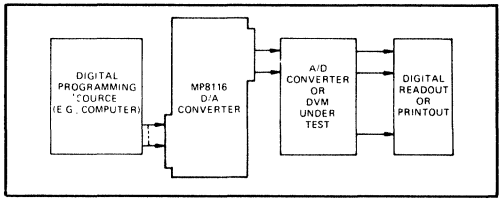


Figure 4. Testing Converters or DVM's.

Computer-Programmable Voltage/Current Source for Precision ATE Systems (Figure 5)

In Figure 5, we see one of the most important applications of the MP8116: its use as a computer-programmable voltage or current source in high-speed automatic test equipment (ATE). Here again, the high accuracy and linearity of the MP8116, and its relatively fast settling time, provide measurement capability and confidence levels not previously available for less than 3-5 times the cost of the MP8116. Note the use of optical couplers at the digital input, for full floating analog output, and the use of load-sensing in the voltage mode. The low-cost Analogic MP3020 dc/dc converter power supply shown will preserve the isolation of the output, and eliminate consideration of common-mode noise errors.

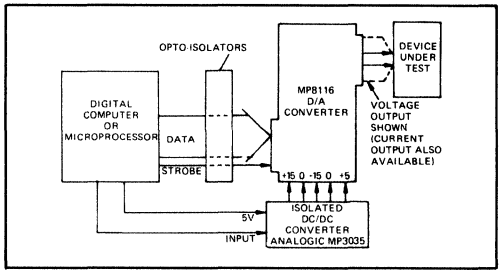
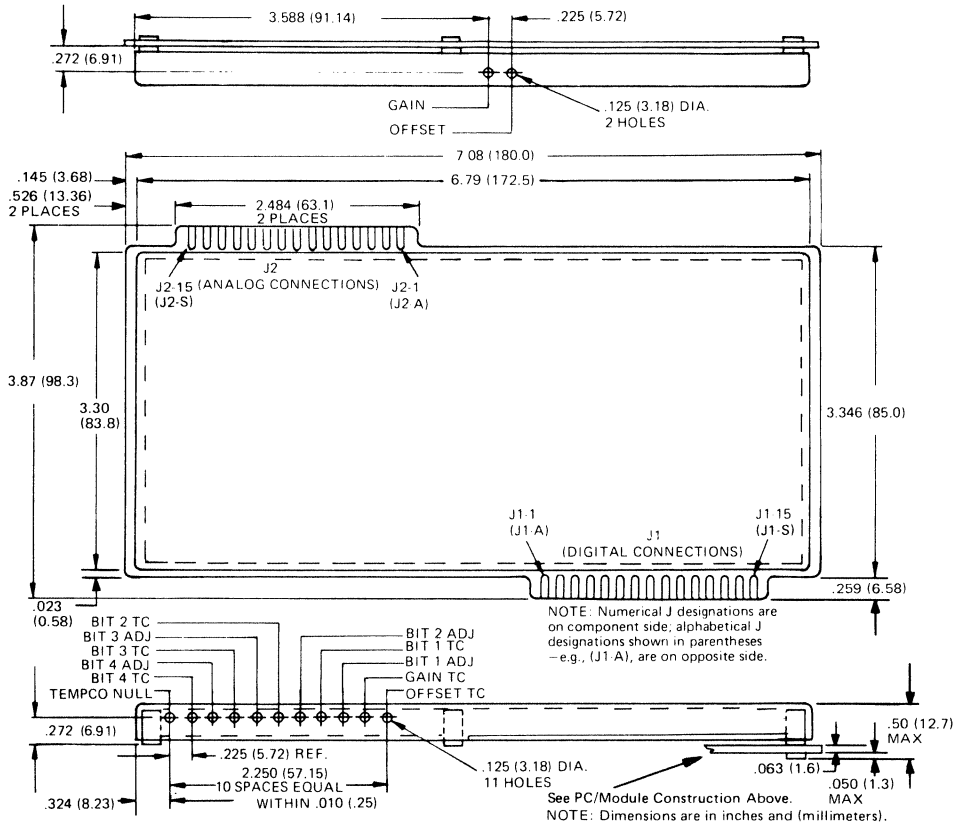


Figure 5. Precision ATE Voltage/Current Source.

FORMAT	INPUT CODE	OUTPUT
Monopolar	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 Volts
10V Span	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9.999847 Volts
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	– 5.000000 Volts
10V Span	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 Volts
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4.999847 Volts
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	– 10.000000 Volts
20V Span	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 Volts
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9.999695 Volts
Two's	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	– 10.000000 Volts
Complement	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 Volts
20V Span	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9.999695 Volts
Monopolar	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 mA
Current	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	– 1.999969 mA
2 mA Span		
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1.000000 mA
Current	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000 mA
2 mA Span	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	– .999969 mA

Table 1 Digital Input Data Coding

MECHANICAL & PINOUT



J1
DIGITAL

ENABLE	1	A	ENABLE
B16	2	B	B1
B15	3	C	B2
B14	4	D	B3
B13	5	E	B4
B12	6	F	B5
B11	7	H	B6
B10	8	J	B7
B 9	9	K	B8
+5V	10	L	+5V
DIG RTN	11	M	DIG RTN
	12	N	
	13	P	
	14	R	
	15	S	

J2
ANALOG

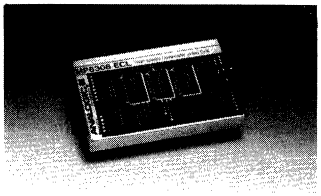
	1	A	
	2	B	
	3	C	
+10V ref	4	D	+10V ref
Return	5	E	Return
Voltage Output	6	F	Voltage Output
Sense Output	7	H	Sense Output
Sense Return	8	J	Sense Return
Output Current	9	K	Output Current
	10	L	
	11	M	
	12	N	
−15V	13	P	−15V
COMMON	14	R	COMMON
+15V	15	S	+15V

ORDERING GUIDE

Order..... **MP8116** ☐ ☐

For Input Full Scale Range
- 0V to 10V..... 1
- ± 10..... 2
- ± 5V..... 3

For Digital Input Coding
- Binary.....A
- Two's Complement.....D



ANALOGIC®

MP8308/8318

Ultra-Fast 8-Bit Video D/A Converters

Description

The Analogic MP8308 and MP8318 are fast, low cost, functionally complete digital-to-analog converter subsystems designed for video and graphic display applications.

The MP8318 accepts 8 data bits, at rates up to 100 MHz, into a set of strobed latches and converts the data into a very fast rise time (3 ns) analog output. The output drives a terminated 75Ω coaxial cable directly, producing a 1V output. This module provides output steps so clean that deglitching is not required (see oscillo-photos). If the 8-bit video input represents a digitized composite video signal, the MP8318 will produce a composite video output.

The MP8308 retains all of the features offered by the MP8318 and produces a composite video output signal with 256 gray levels, including setup, blanking and sync, all derived from separate digital inputs. The output is in general conformance with EIA Standards RS170 and RS343A, and will directly drive the composite video input of high-resolution TV monitors. Both units are available with TTL or ECL logic interfaces, and operate from +5V and −5V (or −5.2V) supplies. They are packaged in fully shielded 2 x 3 x 0.35-inch metal cases, thus allowing ½-inch board spacing.

Features

- **100 MHz Update Rate, ECL**
- **40 MHz Update Rate, TTL**
- **<3 ns Rise and Fall Times**
- **Direct Drive to 75Ω Coaxial Cable or TV Monitor**
- **No Deglitching Required**
- **Strobed Input Data Register**
- **Low Cost**
- **+5V, −5V Supplies**
- **Low Profile, 9 mm (.350") Shielded Case**

MP8308 ONLY

- **RS343A Compatible Signal**
- **Composite Blanking**
- **Composite Sync**
- **Adjustable Setup**
- **8-Bit Gray Scale/256 Levels**

Applications

- **Raster-Scan High Resolution Monochrome Video**
- **Raster-Scan High Resolution Color Video**
- **Graphic Display Systems**
- **Function Generation**
- **Time Base Correction**

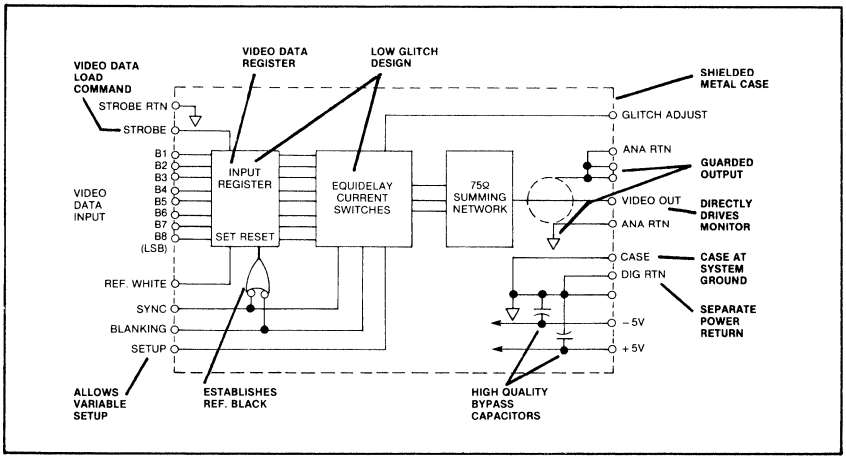


Figure 1. MP8308 Functional Block Diagram.

SPECIFICATIONS

OUTPUT CHARACTERISTICS

Output Voltage Range
0V to −1V ±5% into 75Ω termination

Output Current
−13.3 mA

Recommended Load Impedance
75Ω ±5%, dc to >10 MHz

Source (Thevenin) Impedance
75Ω ±5%, dc to 50 MHz

Output Bandwidth
>100 MHz @ −3 dB

LSB Size
3.9 mV nominal, MP8318
2.5 mV nominal, MP8308

Rise and Fall Time
3 ns typ., 4 ns max. (10% to 90%)

Full Step Settling Time
7.5 ns typ. to 1 LSB (0.4%)

Glitch Settling Time
5 ns to <1 LSB, for worst (MSB) transition

Glitch Area
Equivalent to 1 LSB step @ 50 MHz update rate, typical
For MP8308, worst case area = 70 pV/s max., 50 pV/s typ.

TRANSFER CHARACTERISTICS

Resolution
8 bits, 256 levels

Coding
Binary. An input code of 11111111 (All High) produces 0V out. Input = 00000000 produces −1V out, (MP8318), or −0.643V out, (MP8308)
See "Video Characteristics"

Differential Linearity
±1/2 LSB max. @ 25°C

Monotonicity
Guaranteed, 10°C to 40°C

Offset (dc output with 11111111 input)
±1/2 LSB max., 0°C to 55°C

Transfer Gain (Slope) Tempco
±0.02%/°C max.

Propagation Delay
ECL Version: 7 ns, typ., strobe to output, 50% points
TTL Version: 10 ns, typ., strobe to output, 50% points

INPUT CHARACTERISTICS

Update Rate
ECL: 100 MHz
TTL: 40 MHz

Input Register
8 ECL Type D Flip-Flops in all versions. TTL version also includes built-in TTL to ECL translators in data input lines and strobe

Strobe Input
Data entered on positive-going edge (timing reference)

Setup
ECL: 2.5 ns min. before strobe
TTL: 7.0 ns min. before strobe

Hold
ECL: 1.5 ns min.
TTL: 6.0 ns min.

Logic Levels
TTL version: standard 7400 TTL Levels
ECL version: 10,000 series ECL on Data and Strobe inputs only; TTL levels on control logic

Data Input Loading
ECL: 5 pF and 50 kΩ (to −5V)

(Each of 8 Inputs)
TTL: two-unit load

Strobe Input Loading
ECL: 40 pF and 6 kΩ (to −5V)
TTL: two-unit load

Control Input Loading (MP8308: Blanking, Sync, and Ref. White, MP8318: Set and Reset)
All versions, TTL levels; <2 units each line

POWER SUPPLY REQUIREMENTS

Supply Volgage
Two supplies for all units, +5V and −5V, nominal

Positive Supply
5.0V ±5% @ 25 mA for MP83XX ECL; @ 50 mA for MP83XX TTL

Negative Supply
−4.75V to −5.5V @ 340 mA for MP83XX ECL; at 450 mA for MP83XX

Supply Regulation
Negative supply should not have more than 5 mV p-p ripple

Supply Common
Digital Return is the common for the +5V and −5V supplies

ENVIRONMENTAL AND PACKAGING

Operating Temperature Range
0°C to +55°C

Storage Temperature
−25°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

Mechanical Dimensions
2" x 3" x 0.35"
(50 x 75 x 9 mm)

Shielding
Steel case with electromagnetic shielding 5 sides, electrostatic shielding 6 sides

System Performance

The MP8308 provides three circuit functions: an input data register, eight equi-delay switches, and a high-speed summation network. The register flip-flops are ultra-high speed ECL units that are selected for minimum differential delay. The flip-flops drive high-speed switches that steer current into a summing network.The network has a Thevenin impedance of 75Ω; the input current develops a 1 Vp-p signal directly into a 75Ω load. Due to the unusually small differential delay among the eight data channels, the glitches introduced by code switching are invisible, even on the best monitors. In addition, because the network directly generates the required output voltage, no amplifier or buffer is needed, which results in an unusually clean transition at the output with an extremely fast rise time.

The MP8308 Composite Video DAC

The MP8308 has two additional current switches in the equi-delay bank: one to inject the Blanking level and one for the Sync level, as required to generate a composite video signal. The MP8308 therefore provides higher resolution than other video DAC designs, since none of the 8-bit video gray scale levels are used in generating the Sync signal levels. In addition to preserving full resolution, this approach permits direct control of the amount of Setup. In critical applications, such as computerized tomography (CT), varying the picture brightness is helpful in delineating suspected areas. Heretofore, this was accomplished by manually adjusting the brightness control on the TV monitor. The problem, however, is to restore the picture to its original brightness; this is especially important in the case of color.

The Setup control provides a means for varying brightness in reproducible steps. TV monitors cut off the picture tube in response to the Blanking level, producing the blackest possible visual picture. The Setup control varies the offset between Reference Black level and Blanking level which produces an apparent shift in the "brightness" of Reference Black.

The MP8308 has additional user flexibility, achieved by the addition of a Reference White control. Assertion of this input drives the output to its most positive voltage; the Reference White level. Reference White sets the input register, which turns OFF the eight gray scale current switches. The Sync or Blanking inputs reset the input register, producing full scale output from the gray scale current switches; the output of the Sync or Blanking current switches is added to the full scale output. Obviously Reference White should not be activated during the Sync or Blanking intervals.

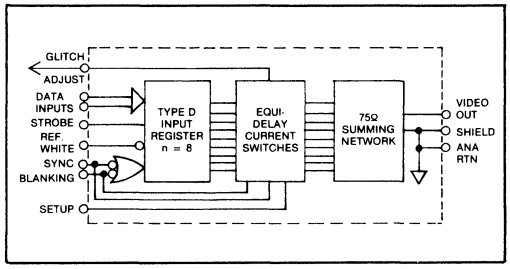


Figure 2. MP8308 Block Diagram.

The MP8318 High Speed DAC

The MP8318 scale output of 1V peak is fully controlled by the 8-bit data word. The MP8318 may be connected to the output of a video ADC, to regenerate a TV image on a monitor. In this example, it is assumed that the input digital data of 8-bits includes the Sync tips.

The Set and Reset inputs of the input register are available on terminals, as shown in Fig. 3; they produce zero or full-scale outputs, respectively, when activated.

The MP8318 is ideally suited for time base correction and function generation applications.

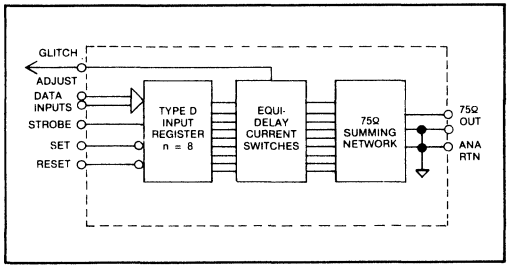


Figure 3. MP8318 Block Diagram.

Operation with other than −5.0V supply

The MP8308 and MP8318 series are capable of operation from a negative supply voltage between −4.75V to −5.5V. The output amplitudes specified are nominal values based upon a −5.0V supply, and will change in direct proportion to the negative supply voltage.

Additionally, the glitch area will vary as a function of the negative supply voltage. The factory trim is carried out at −5.0V. If other than −5.0V is used, connect a 10 kΩ potentiometer as shown, to the Glitch Adjust Terminal. Adjust this pot for minimum glitch area at the major carry transition. If −5.0V is used, this pot may be omitted and the Glitch Adjust Terminal left open.

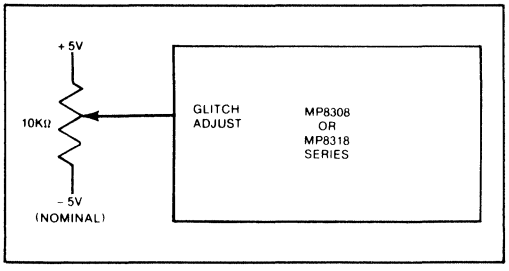


Figure 4. Glitch Adjustment.

Broadcast Usage

EIA Industrial Electronics Tentative Standard No. 1 which will, in the future, become a part of RS170-A, details the exact waveform and timing characteristics of the composite video signal at the output of a color television studio.

The products described in this data sheet are in general conformance with such needs. Exact compliance requires additional circuitry which would, at a minimum, provide Sin X/X correction and bandwidth filtering. In addition, the Setup on the MP8308 should be changed to 7.5 IRE units, by placing a resistor of about 560Ω between the Setup terminal and ground.

APPLICATION INFORMATION

Bandwidth

The output bandwidth may be reduced, if desired, by adding a small capacitor across the DAC output. This will result in slower rise times. The absolute glitch amplitude will decrease, but the energy (or net area) of the glitch will be unchanged.

ECL Terminators

The MP8308ECL and MP8318ECL units do not include ECL terminating resistors. If the source of the video data and strobe is more than a few inches away from these units, ECL terminators should be connected in close proximity to the inputs of the DACs.

Grounds

The DIG RTN, ANA RTN and STROBE RTN terminals are all tied together internally. The +5V and −5V supply common should be connected to DIG RTN. If a long printed circuit wiring connection is required for integration of the DAC into a video system, stripline wiring techniques may be implemented by taking advantage of the physical arrangement of the output terminals i.e., the ANA RTN terminals are located on each side of the VIDEO OUT terminal. ANA RTN normally connects to the shield of an external 75Ω coaxial cable. STROBE RTN is included as a convenience and may be used optionally to facilitate connection.

3262A TV Timing Generator

The sync and blanking outputs of this device may not be capable of driving the MP8308 series, under worst case conditions, without the use of a logic driver.

Data Input Timing

All timing is referenced to the positive edge of the strobe. On ECL units, a Setup of 2.5 ns minimum and a Hold of 1.5 ns minimum, from strobe, are required. On TTL units, 7.0 ns and 6.0 ns are required, respectively, for Setup and Hold.

This example underscores the simplicity achieved when using the MP8308 in a display system. Digital video data, digital sync and digital blanking are converted directly to a composite monitor input. Analog mixing and/or generation of the sync/blanking is not required, nor is a separate high power driver amplifier required ahead of the monitor. Input video data need not be "aligned" to achieve low glitch performance. In fact, a "deglitcher" is not needed, or even built into the MP8308/MP8318 series; the design is inherently low glitch.

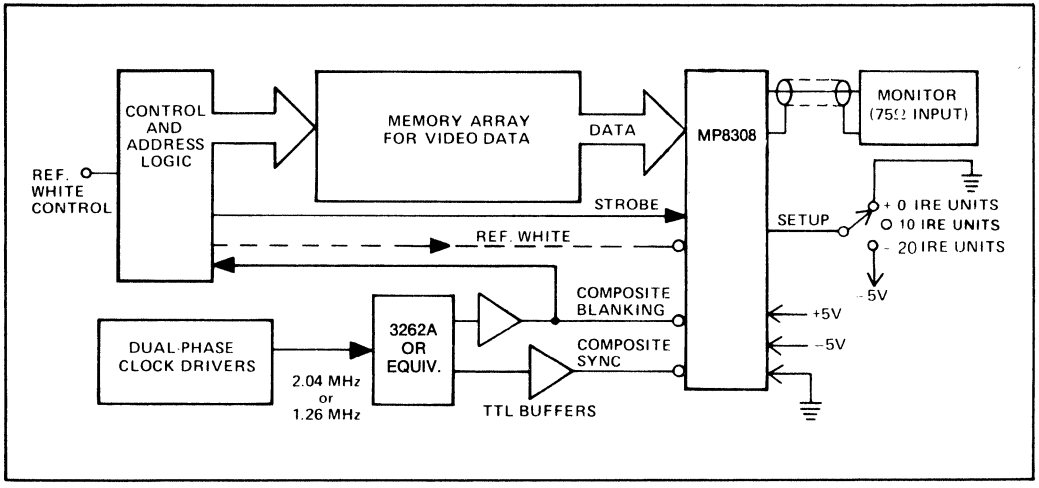


Figure 5. Typical Application of MP8308 in Small Display System.

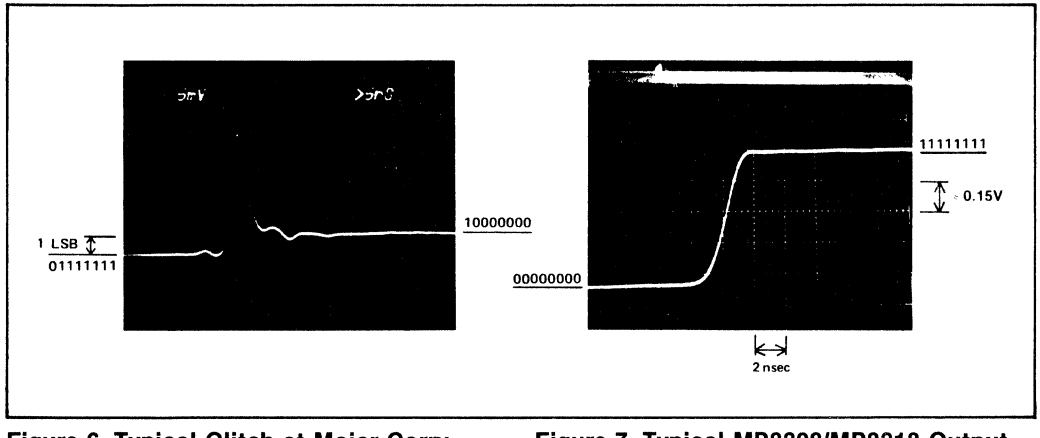


Figure 6. Typical Glitch at Major Carry (worst case transition). Glitch is approximately 40 mV-ns.

Figure 7. Typical MP8308/MP8318 Output for Full Scale Step.

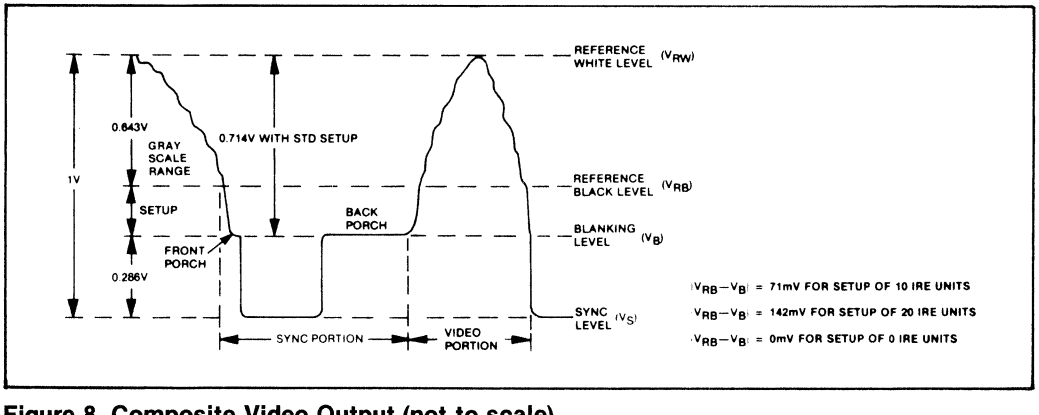


Figure 8. Composite Video Output (not to scale).

VIDEO CHARACTERISTICS (MP8308 ONLY)

Composite Video Signal
Consists of 256 gray levels plus blanking level and sync level

Gray Scale Range
0.643 Vp-p

Step Size
2.5 mV step

Reference White Level
0V, absolute; +0.714V (100 IRE Units) relative to blanking level with standard Setup; +0.643V relative to Reference Black

Input Code for White Level
11111111

Reference White Control
Logic "0" (TTL) on Ref. White line overrides video input data and drives the output to 0V

Reference Black Level
−0.643V, absolute; +71 mV (10 IRE Units) relative to blanking level with standard Setup

Input Code for Reference Black Level
0000000

Composite Blanking Level
−0.714V, absolute, with standard Setup

Input Command for Blanking/Pedestal Level
Logic "0" (TTL) on "Blanking" line simultaneously resets input register to 00000000

Composite Sync Level
−1.0V absolute with standard Setup; −0.286V (−40 IRE Units) with respect to blanking level (back porch)

Input Command for Sync Level
Logic "0" (TTL) on "Sync" line simultaneously resets input register to 00000000

Sync and Blanking Rise and Fall Times
<100 ns

Sync and Blanking Overshoot
<2%

Setup (Reference Black-to-Blanking)
Externally programmable from 0 mV (0 IRE Units) to 142 mV (20 IRE Units)

Setup Control Line
Input Open: Standard 71 mV (10 IRE Units) Setup. Input tied to −5V: 142 mV (20 IRE Units). Input tied to gnd: 0 mV (0 IRE Units)

GLOSSARY OF VIDEO TERMS

Composite Video Signal
The combined video signal, with or without Setup, plus the Sync signal.

Video Signal
The visually perceived portion of the composite video signal which varies in gray scale levels from Reference White to Reference Black. Also known as the picture signal.

Sync or Composite Sync Signal
That portion of the composite video signal which synchronizes the scanning process.

Sync Level
The level of the peak of the Sync signal.

Setup
The difference in level between the Reference Black level and the Blanking level. Not to be confused with setup as used in conjunction with digital logic.

Blanking Level
The level which separates the Sync portion from the video signal, with or without Setup. This level is sometimes also called the pedestal, back porch or front porch. It usually refers to the level which will cut off the TV tube, producing the blackest possible visual picture.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Gray Scale
The discrete levels of the video signal between Reference White and Reference Black levels.

Raster-Scan
The basic method of sweeping across a CRT, a line at a time, to generate and display pictures such as used in commercial TV in the USA.

Monochrome Video
Conventional black-and-white television video in which the Z-axis, or intensity, of the beam is modified during scanning to shade and/or outline images.

Color Video (RGB)
As used herein, this refers to the method of generating color images by combining the three primary colors of red-green-blue (RGB). The associated monitor would be identified as an "RGB" monitor. Three MP8308 series D/A converters are required to drive such a monitor, one each for red, green and blue.

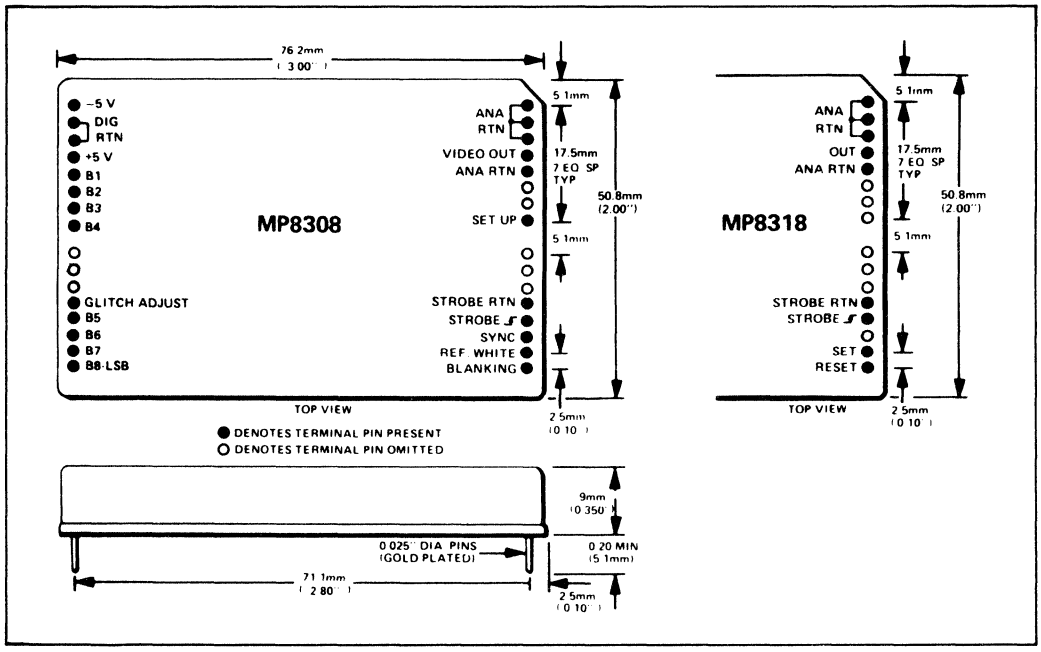


Figure 9. MP8308/MP8318 Outline Dimensions.

ORDERING GUIDE

For 100 MHz ECL Input 8-bit D/A: Specify **MP8318 ECL.**
For 40 MHz TTL Input 8-bit D/A: Specify **MP8318.**
For 100 MHz ECL Composite Video D/A: Specify **MP8308 ECL.**
For 40 MHz TTL Composite Video D/A: Specify **MP8308.**

NOTES

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ANALOGIC®

SECTION 7
DC/DC Converters

SELECTION GUIDE

MAJOR CHARACTERISTIC OR APPLICATION REQ'MT	PRIMARY PARAMETER	SECONDARY PARAMETER	RECOMMENDED MODEL NO.	DATA SHEET ON PAGE
± 15V Output @ 75 mA	Load Regulation ± 0.75% for NL-FL	Line Regulation ± 1% for ± 5% change	MP3024	7-13
± 15V Output @ 100 mA	Load Regulation ± 0.01% for 10 mA change	Line Regulation 0.1% for 4.5-5.5V change	MP3015	7-5
± 15V Output @ 150 mA	Load Regulation ± 0.1% for NL-FL	Line Regulation ± 0.1% for ± 5% input change	MP3020	7-9
	Load Regulation ± 0.2% for NL-FL	Line Regulation ± 0.2% max. ± 5% change	MP3026	7-13
± 15V Output @ 165 mA ± 5V Output @ 750 mA	Load Regulation 0.1% max. (± 15V) 1% max. NL-FL (5V)	Line Regulation 0.1% max. (± 15V) 1% max. for 4.5-5.5V	MP3035	7-17

GLOSSARY OF TERMS

DC-TO-DC CONVERTERS

DC-TO-DC CONVERTER A circuit that converts +5V power to highly stable, highly regulated ±15V power for bipolar analog circuitry. In addition to stability and regulation, DC-to-DC converter requirements include higher isolation, higher efficiency, EMI and RFI shielding, and short circuit protection. See Figure 1.

EFFICIENCY A ratio, expressed in percentage, of output power at full load divided by input power.

ISOLATION Breakdown voltage between the input and the output.

KICKBACK Noise fed back to the input of the converter as a result of inductive switching.

LINE REGULATION A measure of the ability of the converter to maintain its output voltage when the input voltage changes, e.g., ±0.1% for ±5% input change.

LOAD REGULTATION A measure of the ability of the converter to maintain its output voltage when the load changes, e.g., ±0.1% for no load to full load.

LOAD TRANSIENT RECOVERY The time it takes the output to settle to its rated value after a specified step change in the load, e.g., 100 μs to settle to rated output with change from 1/2 load to full load.

PEAK TRANSIENT The maximum noise level, in a given bandwidth, at the output of a converter, as a result of a specified step change in the load, e.g., 50 mV typical for full load change.

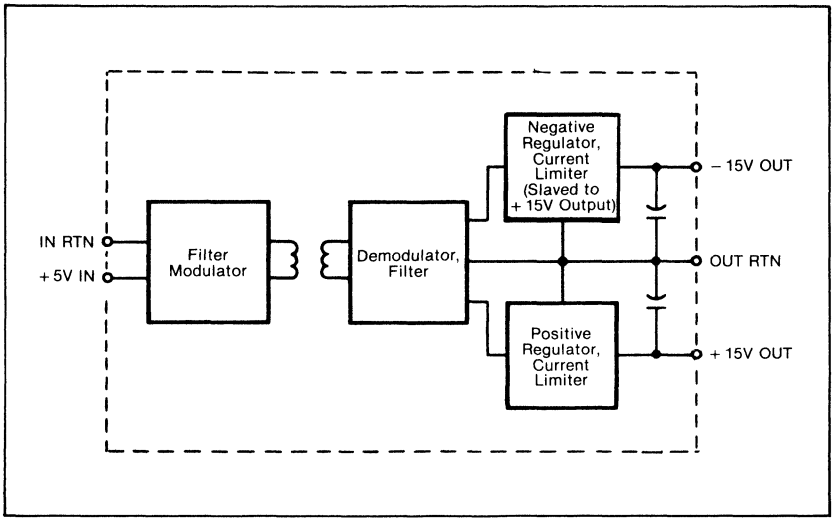
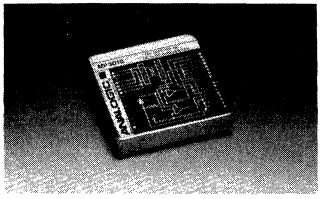


Figure 1. Functional Block Diagram of a DC- to-DC Converter.



ANALOGIC®

MP3015

Stable, Dual Output ±15V out/+5V in dc/dc Converter

Description

The MP3015 is a highly regulated, dual-tracking and very stable dc-to-dc converter, operating from a +5V supply. It provides an output current of 200 mA maximum from both +15V and −15V outputs, with each output limited to 100 mA. It has the ability to sense and correct output voltages at local or remote loads.

Without remote sensing, the load regulation provided by the MP3015 is ±0.1% maximum, for a ±10% change in load. When the 3-wire remote sensing capability is utilized, load regulation improves to 0.01% for the same change in load.

The excellent line regulation of the MP3015 maintains the ±15V output to ±0.1% with variations up to 10% in the +5V input supply voltage.

Short circuit protection is provided by fold-back-type output current limiting. In addition, the +5V supply input is protected from transient loading by an integral LC filter network. Typical output noise is below 1 mV rms, or 20 mV peak, in a 10 MHz bandwidth.

Low current density connections to the MP3015 have been realized through the use of multiple parallel-wired pins for each input and output terminal. The unit is packaged in a 2 x 2 x 0.44 inch module. Gold-plated 0.025 in. diameter pins, with standard 0.1 in. spacing, allow mounting of the module on standard circuit boards designed for 16-pin IC packages.

The use of a metal case guarantees stable operation under all ambient electrostatic and electromagnetic conditions and permits freedom of physical positioning without any risk of mutual interference.

Features

- **±15V Output @ up to 200 mA Total Current**
- **Operates from +5V Source**
- **Voltage Correction with Remote Sensing Feature**
- **±0.01% Line Regulation**
- **Output Impedance Less Than 0.1Ω**
- **1 mV rms Maximum Noise**
- **Short Circuit Protected**
- **Fast Load Transient Recovery**
- **Metal Construction**
  Combines Heat Sink with Superior Shielding
- **Compact:**
  2.0" x 2.0" x 0.44"
  (51 x 51 x 11 mm)

Applications

- **Circuits requiring monitoring of load voltages, for critical ±15V stability and correction**
- **Circuits requiring good load regulation for large changes in load**

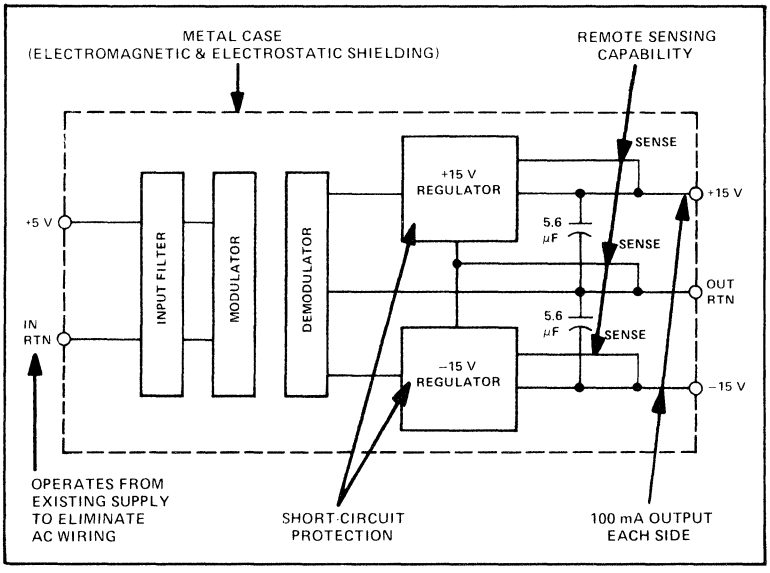


Figure 1. MP3015 Functional Block Diagram.

DC/DC CONVERTERS

SPECIFICATIONS

ELECTRICAL PERFORMANCE

Temperature Coefficient
200 ppm/°C

Noise
Less than 1 mV rms (20 mV peak) with 10 MHz bandwidth

Line Regulation
±0.1% max. change in output voltage for ±10% change in input supply voltage

Load Voltage Sensing Capability
Local or Remote

Load Regulation
Without remote sensing: ±0.1% change in output voltage from 10% change in load.
Remote sensing: ≈±0.01% change in output voltage for 10% change in load

Transient Recovery
100 μs to settle to rated output with change from ½ load to full load

Warm-Up Time
Essentially zero

Shielding
Electrostatic all sides; electromagnetic all sides except bottom

Output Short Circuit Protection
Either side to ground: indefinitely. Both sides to ground: 5 min. max. Short circuit (foldback current: 40 mA max.

ELECTRICAL INTERFACE

Output Voltage
+15V and −15V ±0.7%

Output Current
@ 0°C to +35°C: 200 mA max. Total from both +15V and −15V outputs, but not more than 100 mA from either output
@ +35°C to +70°C: 150 mA max. total from both +15V and −15V outputs, but not more than 100 mA from either output

dc Output Impedance
<0.1Ω

Maximum Voltage Between Input and Output Returns
50V

External Load Capacitance
No maximum

Input Power Requirements
+5 Vdc ±10% @ 1.1 amp, full load; no-load input current = 180 mA

PHYSICAL

Size
2.0 x 2.0 x 044"
(51 x 51 x 11 mm)
Metal encased module

Pin Configuration
0.025 inch diameter gold-plated pins arranged for 16 pin DIP sockets or P.C. mounting

Repairability
Factory repairable

ENVIRONMENTAL

Temperature Range
Operating: 0°C to 70°C. Non-operating −25°C to +85°C

Case Temperature
25°C max. above ambient (case may be connected to heat sink if desired)

Application Data

Remote Sensing:

To utilize the remote sensing capability of the MP3015, sever the three printed circuit foil connections between the three pairs of adjacent pins, as indicated by the asterisks in Figure 3, and connect separate sensing lines between the +15V, −15V, and OUT RTN terminals of the load circuit and the corresponding sense terminals of the Converter. In Figure 3, the supply buses are indicated by bold lines, with sensing lines shown lighter.

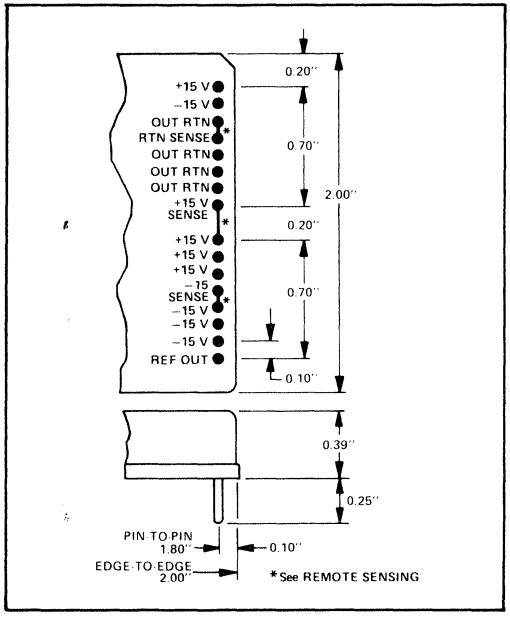


Figure 2. Outline and Mounting Dimensions.

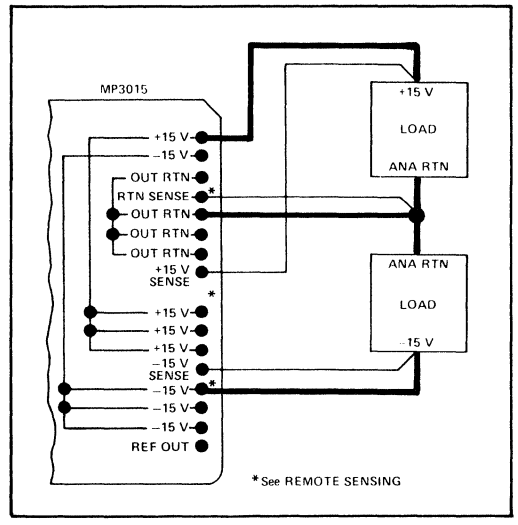
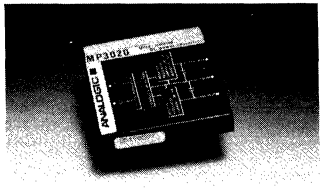


Figure 3. Connections for Remote Sensing.

ORDERING GUIDE

Specify **MP3015.**



ANALOGIC®

MP3020

Ultra-Isolated
+5V In/±15V Out
dc Power Converter

Description

The MP3020 is a tightly regulated, highly isolated, and very stable dc-to-dc converter. It is ideal for driving analog circuitry from digital logic power sources where exceptional efficiency and an extra margin of power are needed. Excellent regulation circuits end spiking problems and limit output voltage variations to 0.1 percent with either an input voltage change of 10 percent or an output change from no load to full load. Typical noise is 700 μV rms or 11 mV p-p across a 20 MHz bandwidth. Positive and negative output circuits can deliver 150 mA individually or 300 mA combined. At maximum load (4.5W), this converter is 65 percent efficient. It draws only 1.4A from a 5V supply, minimizing heat dissipation, and it requires no added heat sinking, as do many other converters, to operate without derating. Noise coupling, either back to the digital supply source or forward to the analog circuitry, is minimized, making the MP3020 ideal for noise-sensitive computer-converter environments.

Sophisticated multiple shielding minimizes the threat of interference, enabling the designer to position this converter in nearly any desired location. A phenolic board protecting the base prevents the possibility of etch run shorts.

Internal limiting of the individual output current to 225 mA protects the MP3020 against short circuits, and an integral filter network protects input circuitry against transients on the source lines.

Features

- **Offers unmatched isolation:** 80 pF, $10^{12}\Omega$, 1000V
- **Delivers 4.5 watts of usable power at 65 percent efficiency**
- **Operates reliably without heat-sinking over full load and temperature ranges**
- **Only 0.375 inches high for plug-in or PC mounting with 0.5-inch card cage spacing**
- **Recovers from full-load transients in 25 μs**

Applications

- **Driving floating front ends in A/D and D/A conversion systems**
- **Driving floating operational amplifier, permitting it to operate with high common mode voltages**
- **Driving strain gauges and load cells**

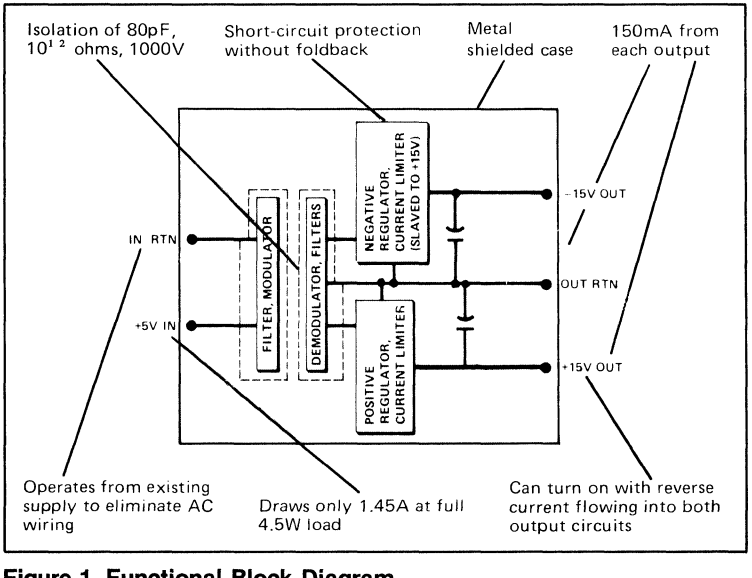


Figure 1. Functional Block Diagram.

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG OUTPUTS

Voltage
+15 Vdc and −15 Vdc, ±0.5% max. (tracking)

Current
150 mA max. each side, 300 mA max. total

Current Limit (Internal)
225 ±50 mA at 25°C

Output Capacitance
10 μF

Load Capacitance
Virtually no limit

Load Regulation
±0.1% max. for no-load to full-load change

Line Regulation
±0.1% max. for a +5 to −5% change or a −5 to +5% change in the input voltage

Load Transient Recovery
20 μs typical, 50 μs max. to 0.1% after a full-load change

Peak Transient
50 mV typical for full-load change, 25 mV typical for a half-load change, both at 10 MHz bandwidth

Temperature Coefficient
±50 ppm/°C typ., ±100 ppm/°C max.

Noise
1 mV rms typ., 40 mV p-p max., both at 20 MHz bandwidth

Short-Circuit Protection
Current limited on both sides, without foldback, to 225 ±50 mA

ANALOG INPUTS

Voltage
5.0 ±0.25V

Current
1.75 mA typ., 200 mA max. at no load, 1.45 amp. max. at full load

Reflected Input Ripple Current
25 mA p-p typ., 50 mA p-p max., with full load change

CHOPPER FREQUENCY

25 kHz nominal

EFFICIENCY

65% typical at 5.0V input voltage and full load

ISOLATION

Resistive Coupling
$10^{12}\Omega$ typical, 10^{10} minimum

Capacitive Coupling
80 pF typical, 100 pF maximum

Breakdown Voltage
1000V typical, 500V minimum

Shielding
Electromagnetic, 5 sides

PHYSICAL

Size
2.0 x 2.0 x 0.375 inches (50.8 x 50.8 x 9.6 mm)

Weight
3.5 oz. max. (99.23g)

Pin Size
0.040 by 0.35 inches (1.0 X 8.9 mm), hardened brass

ENVIRONMENTAL

Operating
−25°C to +70°C

Non-Operating
−40°C to +150°C

Case Temperature Rise
31°C max. (after 30 minutes), 10°C/watt dissipated in package (i.e., at full load, 3.5 watts are dissipated in package)

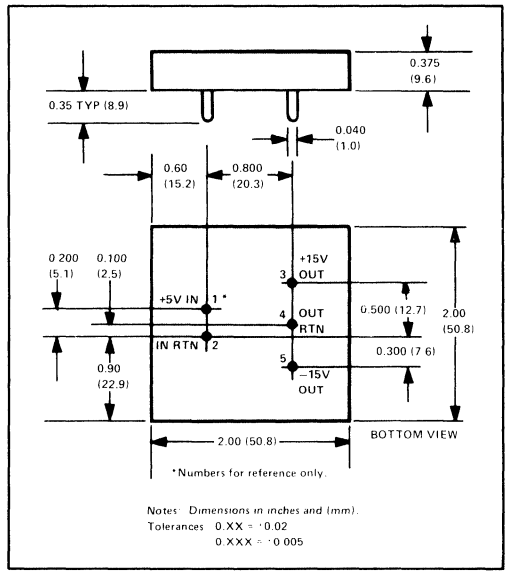


Figure 2. Outline and Mounting Dimensions.

ORDERING GUIDE

Specify: **MP3020**

ANALOGIC®

MP3024/3026

High Isolation, Low Kickback
+5V IN/±15V Out
dc to dc Converters

Description

The MP3024 and MP3026 are dc/dc converters specifically designed for powering and floating analog circuits from +5V logic-level power supplied without inducing "kickback" errors onto the logic circuits that share the same +5V source. Two mdoels are available, each providing a +15V output and a slaved −15V output; the MP3024 provides a total of 2.25W of output power, and the MP3026 provides 4.5W for higher power applications.

Besides a high efficiency of approximately 60% and good regulation, both supplies offer other electrical and mechanical features making them suited to numerous real-world applications. Up to 500V of isolation is provided between the input and the outputs, so that analog circuits powered by these supplies reject the error effects of high common mode voltages arising in many real-world environments. This isolation also prevents such voltages from being coupled back to, and damaging, the host digital system.

As a result of the high efficiency design, very little heat is dissipated so that rated performance may be

(continued)

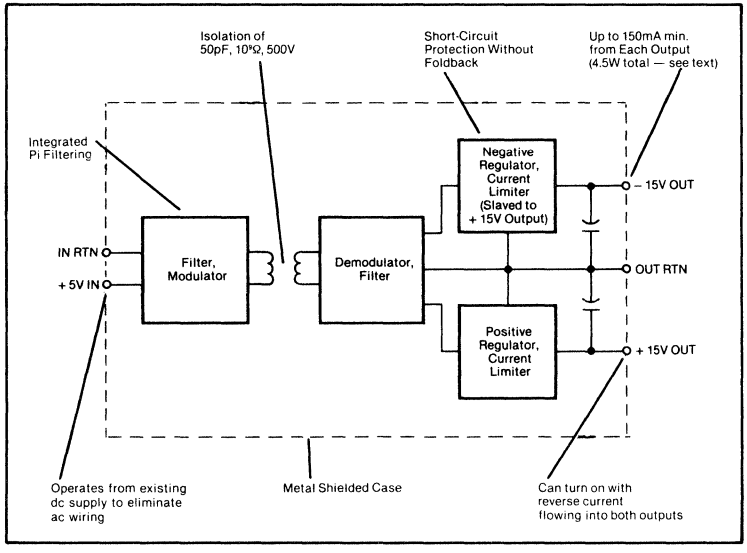


Figure 1. MP3024/MP3026 Functional Block Diagram.

Features

- **Low Cost**
- **High Isolation**
  500 Vdc min. breakdown voltage
- **Choice of Power Ratings**
  Up to 75 mA min. output at +15V and at −15V (150 mA min. total, MP3024)
  Up to 150 mA, min. output at +15V and at −15V (300 mA min. total, MP3026)
- **Integral Pi Filtering**
  Low kickback without external circuitry — less than 50 mA p-p @ 35 kHz (MP3024)
- **High Efficiency**
  60% full load efficiency (MP3024)
  Operation without heat-sinking
- **Good Regulation**
  0.2% load regulation
  200 mV p-p load transient response
  0.2% line regulation (MP3026)
- **Low Profile Metal Case**
  0.375" height — compatible with 0.5" — centers (12.70 cm) board mounting
  Electromagnetic and electrostatic sheilding
- **High Temperature Operation**
  Up to 70°C without derating (MP3026)
- **Fully Specified Performance**
  Fully tested and burned-in (with temperature/load cycling) to ensure dependability

Applications

- **Powering bipolar analog circuits from a +5V supply**
- **Powering floating operational amplifiers in high common-mode-voltage environments**
- **Powering floating front ends in A/D and D/A conversion systems**
- **Exciting strain gauges and load cells**
- **Powering simultaneously-sampling medical instrumentation front-ends**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

OUTPUTS

Voltage
+15 Vdc and −15 Vdc ±5% max.

Current
MP3024 — 75 mA min. at +15 Vdc and 75 mA min. at −15 Vdc (150 mA min. total)
MP3026 — 150 mA min. at +15 Vdc and 150 mA min. at −15 Vdc (300 mA min. total)

Power
MP3024 — 2.25W, min.
MP3026 — 4.5W, min.

Output Capacitance
6.8 μF nom.

Load Capacitance
Unlimited

Line Regulation
MP3024 — ±1.0% max. (±0.5% typ.) for a ±5.0% change in the input voltage
MP3026 — ±0.2% max. for a ±5.0% change in the input voltage

Load Regulation
MP3024 — ±0.75% max. (±0.2% typ.) for no-load to full load change
MP3026 — ±0.2% max. for no-load to full-load change

Temperature Coefficient
±0.03%/°C max.

Transient Response
(for an instantaneous change from 50% load to full load on either or both outputs)
200 mV p-p output transient, max. (10 MHz bandwidth), settling to within specified load regulation tolerance in 50 μs

Noise & Ripple
75 mV p-p and 3 mV rms max. (10 MHz bandwidth)

Short Circuit Protection without damage
Both outputs to each other, or either output to ground

Current Limit (internal)
MP3024 — 300 mA max. at +15 Vdc; 300 mA max. at −15 Vdc
MP3026 — 600 mA max. at +15 Vdc; 600 mA max. at −15 Vdc

INPUT

Voltage
+5.00V ±0.25V

Current
MP3024 — 0.75A, max., @ full load & nominal voltage
MP3026 — 1.55A, max., @ full load & nominal voltage

Power
MP3024 — 3.75W
MP3026 — 7.25W

Reflected Input Ripple Current
MP3024 — 50 mA p-p max., at 35 kHz
MP3026 — 75 mA p-p max., at 35 kHz

Input Protection
Reverse polarity, indefinite without damage

CONVERSION & ISOLATION

Efficiency
MP3024 — 60% min., at nominal +5V input and 150 mA output
MP3026 — 58% min., at nominal +5V input and 300 mA output

Resistive Coupling (input to output)
$10^9\Omega$ typ.

Capacitive Coupling (input to output)
50 pF typ.

Breakdown Voltage (input to output)
500 Vdc min.

Shielding
Electromagnetic, 5 sides; Electrostatic, 6 sides

Chopper Frequency
35 kHz

ENVIRONMENTAL & MECHANICAL

Operating Temperature
MP3024 — 0°C to 50°C in free air (derated to ±50 mA output at 70°C)
MP3026 — 0°C to 70°C in free air (no derating)

Case Temperature Rise
MP3024 — 30°C max. above ambient
MP3026 — 35°C max. above ambient

Non-Operating Temperature
−25°C to +85°C

Relative Humidity
5% to 95%, non-condensing, to +40°C

Size
MP3024 — 1.000 x 2.000 x 0.375" (25.4 x 50.8 x 9.5 mm)
MP3026 — 2.000 x 2.000 x 0.375" (50.8 x 50.8 x 9.5 mm)

Weight
MP3024 — 1 oz. max. (28.4 gm)
MP3026 — 2 oz. max. (56.7 gm)

Case Potential
Tied to Output Return

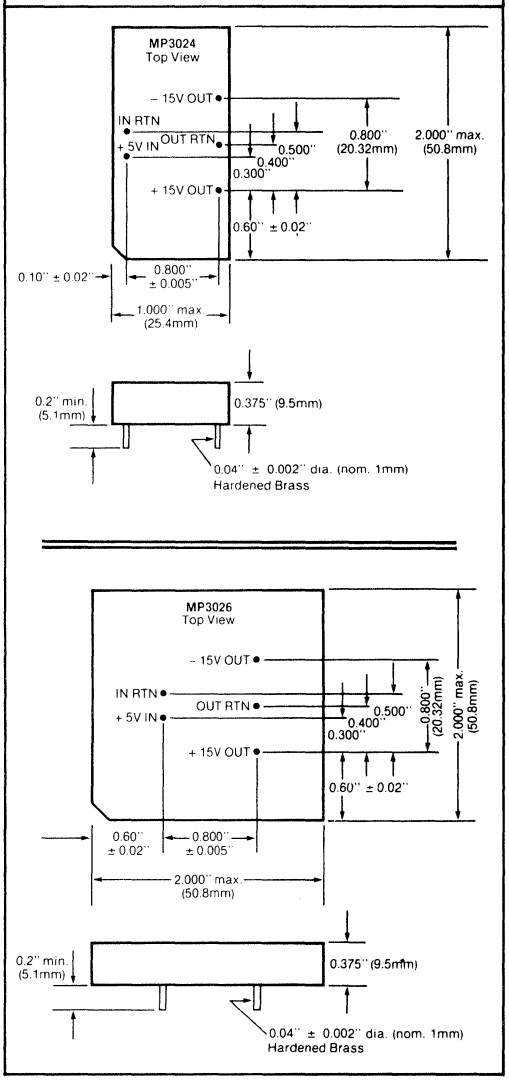
Description (cont.)

obtained without heat-sinking. A metal case is standard, providing RFI shielding on six sides, and EMI shielding on five. The case's low profile (0.375") allows printed circuit board spacing of only 0.5" (12.70 mm) on centers.

These supplies are reliable in a variety of usage situations, incorporating protection for both the inputs and the outputs. Each unit is exhaustively tested and burned-in with on/off cycling, load variations, and temperature cycling to ensure reliable operation under all operating conditions. Further, the MP3026 affords operation up to 70°C without derating.

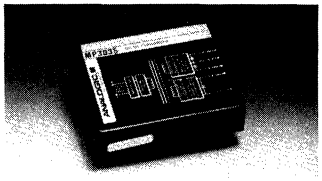
The reliability, high performance, and low cost of these converters qualify them for driving operational amplifiers, strain gauges, and many other circuits for which precision and dependability must be achieved at low cost.

MOUNTING DIMENSIONS & PINOUTS



ORDERING GUIDE

For	Specify
2.25W output	**MP3024**
4.5W output	**MP3026**



ANALOGIC®

MP3035

+5V In
Isolated +5V Out
& Isolated ±15V Out
DC Power Converter

Description

Analogic's MP3035 is a compact dc-to-dc power converter that provides exceptionally high levels of efficiency, isolation, and reliability, with a full 9 watts of output... enough to power a complete A/D or D/A data system. It provides a very high degree of isolation, both from input to output and between the analog (±15V) and digital (5V) grounds. Noise, ripple, and heat dissipation are all minimized in this system-oriented design.

The positive and negative analog outputs can deliver 165 mA each, and the +5V output is rated at 750 mA. Load and line regulation are typically 0.02% on the ±15V outputs and 0.1% and 0.01% on the +5V output.

The isolated grounds suppress digital interference in the analog section, and eliminate system ground-loop problems. Common-mode voltages may be as high as 500V.

In addition to positive, non-foldback constant-current limiting of all three outputs, each is provided with a thermal-shutdown feature that protects semiconductor junctions. In the Fault Mode, any output shorted to its respective common will survive eight hours, at a T_A of +71°C — a period generally adequate to locate a system short.

Only derated computer-grade components are used in the MP3035, and each unit is subjected to **100-hour burn-in** after assembly, to assure the highest reliability. Thermal resis-

(continued)

Features

- **Excellent Isolation** — 75 pF, $10^9\Omega$, 500V. Separate analog and digital grounds
- **Complete EMI/RFI Shielding** — continuous six-sided package shield, π-type input filter, multiple transformer shielding
- **Double Protection** — special constant-current limiting (no latchdown); thermal shutdown for long-term fault protection
- **Low surface temperature rise** — 5°C per package watt dissipated
- **High reliability** — 100% burn-in, components derated, operates without heat sinking over full load and temperature range
- **Fast full-load transient-recovery time** — 25 μs maximum
- **Separate Analog and Digital Grounds** — System ground loops eliminated, low digital noise interference
- **Low Noise** — Minimizes open-board noise and shielding problems

Applications

- **A/D & D/A Converters and Data Acquisition Systems** — linear, digital circuitry, CMOS, DTL/TTL, Function Modules, LSI Memory Standby Power Source (from batteries)
- **Portable Data Systems** — mobile instrumentation
- **Transducer Excitation** — driving strain gauges and load cells

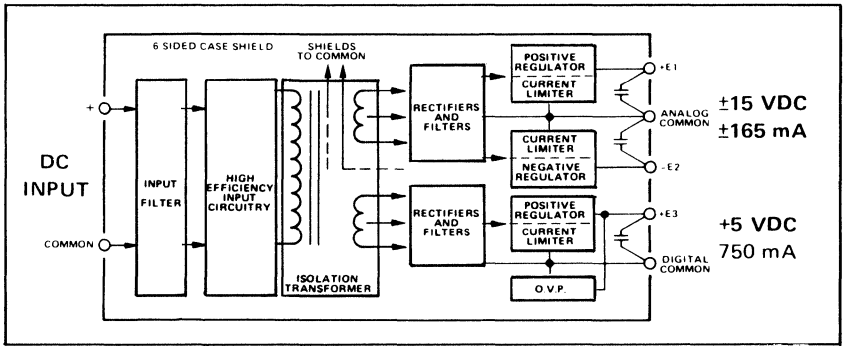


Figure 1. MP3035 Functional Schematic Diagram.

OUTPUTS

Voltage, E1 & E2
+15 Vdc and −15 Vdc, ±0.2% typ. ±1% max. (tracking)

E3
+5 Vdc ±4% max.

Voltage Balance, E1 to E2
±0.5% ±1% max.

Rated Current
E1 & E2
±165 mA

E3
±750 mA
(all three outputs may be fully loaded simultaneously)

Constant Current Limiting, E1 & E2
I thresh = 250 mA; Issg = 300 mA

E3
I peak = 2.2A; Issg = 750 mA

Voltage Limiting (O.V.P.), E3
6.8V

Load Regulation (NL-FL), E1 & E2
±0.02% typ., ±0.1% max.

E3
±0.1% typ., ±1% max.

Line Regulation (full range), E1 & E2
±0.02% typ., ±0.1% max.

E3
±0.1% typ., ±1% max.

Average Voltage Temperature Coefficient, E1 & E2
±0.003% typ., ±0.015% max.

E3
±0.02% typ., ±0.05% max.

Voltage Stability after Initial Warmup, E1 & E2
±0.01% max./1 hr. ±0.05%/24 hr.

E3
±0.05% max./1 hr. ±0.2%/24 hr.

Initial Voltage Warmup Drift, E1 & E2
±20 mV typ., ±90 mV max.

E3
±40 mV typ., ±90 mV max.

Initial Warmup Time (±FL)
60 minutes

Load Transient Recovery (NL-FL; error band ±0.1%)
25 μs typ., 50 μs max.

Noise, Bandwidth = 20 MHz (±FL), E1 & E2
1 mV max. rms, 15 mV p-p typ., 40 mV p-p max.

E3
1.2 mV max. rms, 20 mV p-p typ., 40 mV p-p max.

Short Protection
Any output to its respective common will survive 8 hr. at T_A of +71°C

Output Power
8.7 watts

INPUTS

Voltage Range
±5.00 Vdc ±0.500 Vdc

Current
3.48A (FL), 0.50A (NL)

Power Interruption
Restarts in Fault Mode. Restarts with reverse current injected into output.

Converter Start-up
E_{IN} <1 Vdc

Converter Switching Frequency
>20 kHz (inaudible)

Power Efficiency
50%

Reflected Input Ripple Current
2%, 3.5% p-p max. of I_{IN}

(Bandwidth = 20 MHz, ±FL, R_S = 0.25 terminated)
70 mA p-p

Input Fault Mode Current
7A (worst case)

ISOLATION

Input to Output
Effective "C", E1 & E2
150 pF

E3
75 pF

Effective "R"
$10^9\Omega$ min.

E1, E2 to E3 Output
Effective "C"
110 pF

Effective "R"
$10^9\Omega$ min.

Breakdown Voltages
500 Vdc min.

COMMON MODE NOISE CURRENT

(CM_{IN}) Bandwidth = 20 MHz (±FL), RS = 50Ω E1 & E2
500 μA p-p

E3
700 μA p-p

EMI/RFI SHIELDING

Transformer
Mulitple Shielding

Internal Input Filter
π-type

Package
6 sides, continuous

PHYSICAL

Size
3.00" x 2.56" x 0.75"
(76.2 x 65.0 x 19.1 mm)

Weight
12 oz. (340.2g)

Pin Size
0.040" dia. x 0.25"
(1.02 dia. x 6.35 mm)

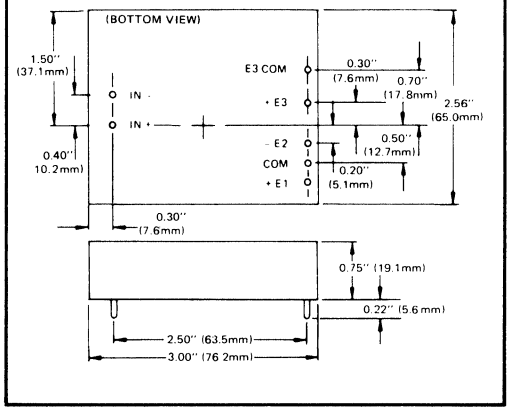
ENVIRONMENTAL

Operating Temperature Range
– 25°C to + 71°C

Storage Temperature Range
– 40°C to + 125°C

Case Temperature Rise
5°C/Package watt dissipated

DIMENSIONS & PIN CONNECTIONS



Description (cont.)

tance paths (θ_{J-C}) are of the order of 50% less than in comparable power-supply modules. Surface temperature rise is only 5°C per package watt dissipated and, at maximum load, the MP3035 is 50% efficient.

Sophisticated multiple shielding of transformer and case, including an internal π-type input filter, effectively minimizes interference. The converter may thus be positioned in nearly any desired location.

NOTES

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