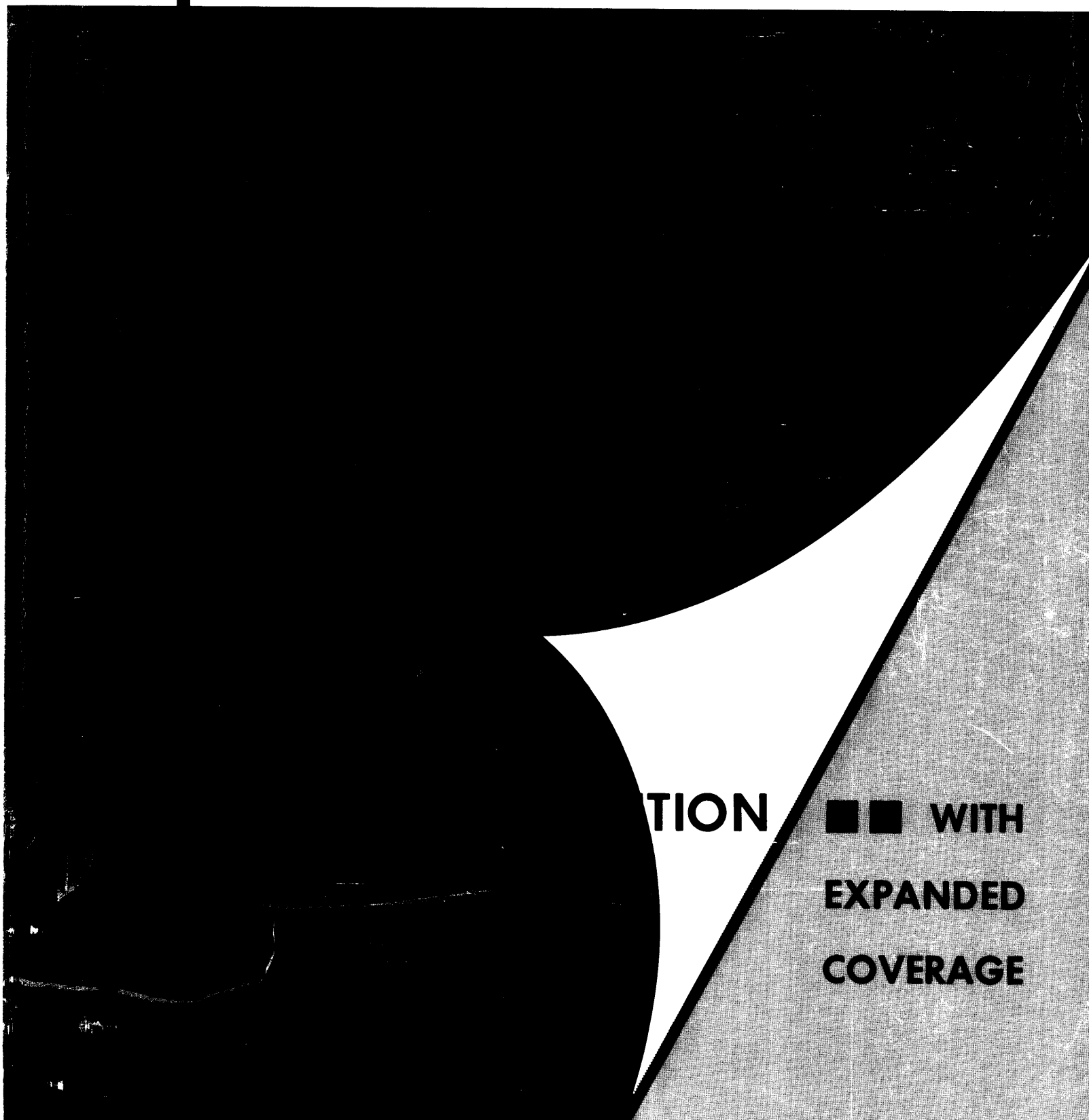
AUERBACH Guide to



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AUERBACH

Guide to Minicomputers

The material contained in this publication will be included in *AUERBACH Computer Technology Reports*, an analytic reference service that provides comprehensive coverage of the information processing industry.

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PREFACE

Although "dispersal of computer power" is currently a popular phrase, minicomputers have been dispersing computer power for more than 8 years. Sophisticated users were quick to find the minicomputer an attractive alternative to waiting in line for a batch processing system. Minicomputers are not only cheaper and faster than their general-purpose cousins, but also technologically more advanced. New technology adds more power, lowers costs, and increases markets. Because they were first used in process control applications, in laboratories, and for communications, minicomputers are real-time and on-line oriented. After 8 years, the marginal manufacturers have been shaken out; only well-managed companies that produce substantial products remain.

This **AUERBACH Guide to Minicomputers** presents an introduction to minicomputers and a system overview of the major minicomputers on the market today. Some manufacturers, such as Digital Equipment, produce two or three lines of minis. Others produce only one broad line. Generally the minicomputer manufacturers call themselves "toolmakers." They produce the hardware and software tools that others use to solve problems in a particular application.

The **AUERBACH Guide to Minicomputers** presents information in several levels of detail. Special individual reports devoted to general-purpose minicomputers, microcomputers, and microprocessors and process control systems explain how to evaluate and select your own system. Each major minicomputer and some minor ones are covered in a separate analytical report.

You can look through the Table of Contents for a system which interests you. If you want a quick view of the minicomputers available on today's market, check the search chart. For more detailed information on a particular manufacturer's components, go to the individual product reports. A price list is included as part of each report. When you have evaluated the minicomputers and selected the ones that seem most likely to fulfill your needs, consult the list of suppliers for addresses and phone numbers.

This selection guide presents the following information:

- Device Reports
  - — Text: describes characteristics of various minicomputer systems. Each product report begins with a summary and then discusses configuration, software, design features, performance, maintenance and company history.
  - — Product Specifications: a chart that summarizes information on the components' performance, capacity and design.
  - — Price Data: price list of equipment supplied.
- Search Chart — provides a quick way to compare the minicomputers covered in the product reports. Lists major processor features, peripheral devices and programming languages for all minicomputers available on the market. The reports are a selection of this material.
- Suppliers: — an alphabetical directory of vendors.

PREFACE (Cont.)

To use the guide effectively, it is important to know what information is contained in each product report. Separate sections discuss a device's advantages and marketing, configuration possibilities, facilities requirements, performance characteristics, and service. The company's background is also covered.

The Summary or Overview gives the name of the company marketing the system, its special capabilities or unique features, and their significance to the user, as well as the user group most likely to benefit from a particular minicomputer. The Performance section evaluates the system's competitive position, performance capabilities, special strengths and weaknesses, and its impact on other systems in the marketplace. Users are interviewed to show how effective the system is in operation. The company history is also included, telling the date the firm was established and its major business, and noting the growth of its minicomputer line.

The Configuration Guide identifies the major system components, states their performance and interface requirements, and lists available options. This section also gives information on capacities of main and auxiliary storage, data structure and speeds of input/output devices.

The Software section identifies the major software available to the SBC under consideration. This includes discussions of the applications software offered by the vendor.

Since maintenance is another important aspect in selecting an SBC, a section of each report specifies the company providing maintenance and its experience.

For selected major minicomputer systems, the **Guide to Minicomputers** includes the Detail Report that also appears in the General-Purpose Minicomputers segment of the updated **AUERBACH Computer Technology Reports** library service. The Detail Report provides expanded information in the following areas: mainframe, memory, input/output control, peripherals, data communications and software.

SEARCH CHART

Minicomputers

MFR AND MODEL NUMBER	First Delivery	COVERAGE			WORD LENGTH (Bits)				MAX MEM (Bytes)			PERIPHERALS			SOFTWARE		MAJOR MARKETS					
		Small Business	Minis	Intel Term	8	12	16/18	24/32	< 32K	32-64K	> 64K	Disc/Drum	Mag Tape	Data Comm	Oper Sys	Fortran/Algol	Germany	France	Italy	U.K.	U.S.A.	Other
ACEC-92	68						X				X	X			X	X						X
AEG 60-07	72		X		X				X								X					
60-10	69		X			X				X		X	X		X		X					X
60-50	68		X					X			X	X			X	X	X					X
TR 86			X					X			X						X					X
Ai-Denshi Sokki																						
Aicom-C4	70						X			X		X	X			X						X
C4P	71						X			X		X	X			X						X
C5	72						X			X		X	X	X		X						X
Arcturus 18C	71						X				X	X	X	X						X		
18D	73		X				X			X		X	X	X						X		
Brown-Boveri																						
DP 100	69						X					X	X	X	X	X	X					
DP 1000	72						X			X					X		X					
Burnt Hill																						
Electronics 204	70						X			X										X		
Canon-Jimuki																						
Canon BP-1000	71							X	X							X						X
Pasca 2500	72							X	X			X										X
Chuo-Denshi																						
CEC 555	68						X			X		X				X						X
CEC 5555	69						X		X			X	X	X		X						X
CEC 5557	70						X		X			X	X	X		X						X
CEC 555M	71						X				X					X						X
CEC 555H	71						X				X					X						X
CDC System 17	73		X				X				X	X	X	X	X	X					X	
SC1700	69		X				X			X		X	X	X	X	X	X	X	X	X	X	X
1704	66		X				X			X		X	X	X	X	X	X	X	X	X	X	X
1714	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
CII 10010					X					X		X		X	X	X	X	X		X		X
10020							X				X	X	X	X	X	X	X	X				
Mitra 15/20			X				X		X			X		X	X	X	X	X		X		X
Mitra 15/21			X				X			X		X		X	X	X	X	X		X		X
Mitra 15/30			X				X			X		X		X	X	X	X	X		X		X
Cincinnati Milacron																						
CIP/2200	72		X				X			X		X	X	X	X						X	
Computer Automation Naked Mini																						
LSI-2	73		X				X			X		X	X	X	X	X	X	X		X	X	X
LSI-3/05	75		X				X		X	X		X			X	X	X	X		X	X	X
Alpha/LSI	73		X				X			X		X	X	X	X	X	X	X		X	X	X
MegaByter	75		X				X				X	X	X	X	X	X	X	X		X	X	X

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Computer Signal Processors																						
CSP-30	70		X				X				X	X	X								X	
CSP-125	73		X				X				X	X	X								X	X
Computer Technology																						
MiniMod	73		X				X				X	X	X	X	X	X		X		X		
Modular One	68		X				X				X	X	X	X	X	X		X		X	X	
Datacraft																						
DC-6024/1	69		X					X			X	X	X	X	X	X					X	
DC-6024/3	72		X					X			X	X	X	X	X	X					X	
DC-6024/4	73		X					X			X	X	X	X	X	X					X	
DC-6024/5	72		X					X			X	X	X	X	X	X					X	
DC-6024/5R	73		X					X			X	X	X	X	X	X					X	
Data General																						
ECLIPSE	75		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Nova 2/4, 2/10	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Nova 800	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Nova 820	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Nova 830	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X	X
Nova 840	73		X				X				X	X	X	X	X	X	X	X	X	X	X	X	X
Nova 1200	70		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Nova 1210	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Nova 1220	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Supernova	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Supernova SC	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Datamate Computer DM-16	69		X				X			X		X	X	X		X					X		
DM-70	70		X				X			X		X	X	X		X					X		
Datasaab D5	70	X	X				X				X	X	X	X	X	X	X					X	X
D21	65							X			X	X	X	X	X	X	X						X
Dietz Mincal 513	69		X				X		X								X						
523	69		X				X			X		X	X		X	X	X						X
621	71		X		X						X	X	X	X	X	X	X	(1)	(1)				X
1600	73						X			X		X	X	X	X	X	X						X
Digico Micro 16	68		X				X			X					X	X	X				X		
16-P	70		X				X				X	X	X	X	X	X	X				X		
16V	72		X				X				X	X	X	X	X	X	X				X		
Digital Computer Controls D-112			X			X				X		X	X	X	–	–					X		
D-112H/SC			X			X				X		X	X	X	–	–					X		
D-116			X				X			X		X	X	X	–	–					X		
DEC MPS Series	74		X		X				X								X	X	X	X	X	X
PDP-8/A	74		X			X				X					X	X	X	X	X	X	X	X

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PDP-8/E	70		X			X				X	X	X	X	X	X	X	X	X	X	X	X	X
PDP-8/F	72		X			X			X	C		X	X	X	X	X	X	X	X	X	X	X
PDP-8/M	71		X			X				X		X	X	X	X	X	X	X	X	X	X	X
LSI-11	75		X				X			X		X	X	X			X	X	X	X	X	X
PDP-11/04	75		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/05	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/10	72		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11E/10	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/15	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/20	70		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/R20	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/35	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-11/40	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-11/45	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-11/50	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X
PDP-11/70	75		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-12	70		X			X				X		X	X	X	X	X	X	X	X	X	X	X
PDP-15/10	70		X				X		X								X	X	X	X	X	X
PDP-15/20	70		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/30	70		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/35	70		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/40	70		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/50	71		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/70	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/76	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
PDP-15/78	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Digital Scientific META 4	70		X				X				X	X	X		X	X					X	
Elbit 100						X			X			X					X	X				X
Electronic Associates EAI PACER 100	72		X				X			X		X	X	X	X	X	X	X	X	X	X	X
Electronic Processors																						
EPI-118	70		X				X				X	X	X	X	X	X					X	
EPI-218	72		X				X				X	X	X	X	X	X					X	
Ericsson																	X					X
Ferranti Argus 400								X			X	X		X	X	X	X	X		X		X
500	68		X					X			X	X		X	X	X	X	X		X		X
600	70		X		X				X			X		X	X	X	X	X		X		X
700E	74		X				X				X	X	X	X	X	X	X	X		X		
700S	73		X				X				X	X	X	X	X	X	X	X		X		
700T1	74		X				X			X		X	X	X	X	X	X	X		X		
700T2	74		X				X			X		X	X	X	X	X	X	X		X		
Foxboro FOX 1	71							X			X	X			X	X	X	X	X	X	X	X
FOX 2/10	72						X			X					X	X	X	X	X	X	X	X
FOX 2/30	72						X			X		X			X	X	X	X	X	X	X	X

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Fujitsu Facom R	69						X				X	X	X	X		X					X	X
Facom R/R-E	70						X				X	X	X	X		X					X	X
Facom Mate II	73		X				X			X		X	X		X	X						X
GEC 903	66						X				X		X		X	X	X	X		X		X
905	69		X				X				X	X	X	X	X	X	X	X		X		X
2050	72		X		X					X		X		X			X	X		X		X
M.2140	69						X				X	X	X	X	X	X				X		
4080	72		X		X						X	X	X	X	X	X	X	X		X		X
Myriad	65							X			X	X		X						X		
LSI 12/16	74		X		X					X		X	X	X	X		X	X	X	X	X	X
General Automation																						
SPC-12	68		X		X				X					X	X		X	X	X	X	X	X
SPC-12/10	71		X		X				X			X	X	X	X		X	X	X	X	X	X
SPC-12/15	71		X		X				X			X	X	X	X		X	X	X	X	X	X
SPC-12/20	71		X		X				X			X	X	X	X		X	X	X	X	X	X
SPC-16	70		X				X				X	X	X	X	X	X	X	X	X	X	X	X
SPC-16/40	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
SPC-16/45	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
SPC-16/60	71		X				X			X		X	X	X	X	X					X	
SPC-16/65	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
SPC-16/80	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
SPC-16/85	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
GA 18/30	69		X				X			X		X	X	X	X	X	X	X	X	X	X	X
General Electric																						
GE/PAC 3010/2	72		X				X			X		X	X	X	X	X					X	
GE/PAC 4010	70		X					X			X	X		X	X	X		X		X	X	
GE/PAC 4020	67		X					X			X	X			X	X		X		X	X	
GRI Computer																						
GRI-99, Model 10	72		X				X			X			X		X	X	X	X		X	X	
GRI-99, Model 30	72		X				X			X			X		X		X	X		X	X	
GRI-99, Model 40	72		X				X			X			X		X		X	X		X	X	
GRI-99 Model 50	74		X				X			X		X	X	X	X	X	X	X		X	X	
Harris																						
Slash 1	69		X					X			X	X	X	X	X	X					X	
Slash 3	72		X					X			X	X	X	X	X	X					X	
Slash 4	73		X					X			X	X	X	X	X	X					X	
Slash 4VMS	74		X					X			X	X	X	X	X	X					X	
Slash 5	72		X					X			X	X	X	X	X	X					X	
Slash 5R	73		X					X			X	X	X	X	X	X					X	
Hewlett-Packard	72		X				X				X	X	X	X	X	X	X	X	X	X	X	X
HP 2100A	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
HP 2100S	72		X				X			X		X	X	X	X	X	X	X	X	X	X	X
HP 3000CX	74		X																			
HP 21MX	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Model 50CX	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Model 100CX	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Model 200CX	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X

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Model 300CX	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
HP 9600	70		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
9700	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Hitachi Hitac 10	69						X			X		X	X	X		X					X	
Hitac Mini	71						X		X							X					X	X
Hokushin Hoc 700E	71						X				X	X			X	X						X
Honeywell																						
H112	69		X			X			X					X			X	X	X	X	X	X	X
H316	69		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
DDP-516	67		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
GE/PAC 4010	70		X					X			X	X		X	X	X		X		X	X		
GE/PAC 4020	67		X					X			X	X			X	X		X		X	X		
4400			X					X			X	X	X	X	X	X		X		X	X		
System 700	72		X				X		X		X	X	X	X	X	X	X	X	X	X	X	X	X
System 725-G, S, M	74		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
System 735-G, S	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X	X
Honeywell																							
1640 Series			X				X			X		X	X	X	X	X						X	
1648A			X				X			X		X	X	X	X	X						X	
IBM 1130	65		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
1800	66		X				X			X	C	X	X	X	X	X	X	X	X	X	X	X	X
System/7	71		X				X				X	X		X			X	X	X	X	X	X	X
ICS Multum	72		X				X				X	X	X	X	X	X				X			
Informatek																							
Matek 1026	72						X				X	X	X	X	X	X		X					
Interdata Model 1	70		X		X				X			X	X	X			X	X	X	X	X	X	X
Model 70	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X	X
Model 74	73		X				X			X		X	X	X	X	X	X			X	X	X	X
Model 80	71		X				X			X		X	X	X	X	X	X			X	X	X	X
Model 85	73		X				X			X		X	X	X	X	X	X			X	X	X	X
RD-800	75		X				X			X		X	X	X	X	X	X			X	X	X	X
RD-850	75		X				X			X		X	X	X	X	X	X			X	X	X	X
System 7/16	74		X				X			X		X	X	X	X	X	X			X	X	X	X
System 7/32	74		X				X				X	X	X	X	X	X	X			X	X	X	X
System 8/32	75		X					X			X	X	X	X	X	X	X			X	X	X	X
Intertechnique																							
Multi-4	73		X		X				X								X	X	X	X		X
Multi-4/01	74		X				X		X			X	X		X	X	X	X	X	X		X
Multi-4/02	74		X				X		X			X	X		X	X	X	X	X	X		X
Multi-4/05	74		X				X		X			X	X	X	X	X	X	X	X	X		X
Multi-4/M.301	74						X		X			X	X		X		X	X	X	X		X

SEARCH CHART—MINICOMPUTERS

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Multi-4/M.302	74						X		X			X	X		X		X	X	X	X		X
Multi-4/M.305	74						X		X			X	X	X	X		X	X	X	X		X
Multi-8	69		X		X					X							X	X	X	X		X
Multi-8M.301	70		X				X			X		X	X		X	X	X	X	X	X		X
Multi-8M.302	70		X				X			X		X	X		X	X	X	X	X	X		X
Multi-8M.304	70		X				X			X		X	X	X	X	X	X	X	X	X		X
Multi-8M.350	71		X				X			X		X	X		X	X	X	X	X	X		X
Multi-20	72		X		X						X						X	X	X	X		X
Multi-20/01	72		X				X				X	X	X		X	X	X	X	X	X		X
Multi-20/05	72		X				X				X	X	X		X	X	X	X	X	X		X
Multi-20/06	72		X				X				X	X	X	X	X	X	X	X	X	X		X
ITT System 310																		X	X			X
Krantz Elektronik MULBY			X		X					X							X					X
MULBY 3/30, 3/35	73				X					X		X	X	X	X	X	X					
Krupp EPR 1100	73					X					X	X	X		X		X					
Laben 70							X			X		X	X		X	X			X			X
701	73					X				X		X	X		X	X			X			
Leeds & Northrup LN 5400	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Lockheed Electronics MAC 16	69		X				X				X	X	X	X	X	X	X			X	X	
MAC Jr	70		X				X				X	X	X	X	X	X	X			X	X	
SUE 1110	71		X				X			X		X	X	X							X	
SUE 1111 (System III)	72		X				X			X		X	X	X							X	
SUE 1112	72		X				X			X		X	X	X							X	
Marme GMG 5000	72						X			X		X	X					X				
Matsushita-Tshushin MACC-7/S	70						X		X			X	X	X		X						X
MACC-7/F	71						X		X			X	X	X		X						X
MB Metals K-202	72				X						X	X	X	X	X	X				X		X
Micro Computer Systems MINIC	71		X		X						X	X	X	X						X		
Micro Consultants 1601	71		X				X			X		X								X		
Microdata																						
MICRO-ONE	74		X		X					X											X	

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MICRO 400	70		X		X						X	X	X	X							X	
MICRO 800 Series	69		X		X					X		X	X	X							X	
MICRO 1600 Series	71		X		X					X		X	X	X							X	
MICRO 3200	73		X				X				X	X	X	X	X						X	
MICRO 3230	73		X				X				X	X	X	X							X	
MICRO 32/S	74		X				X				X	X	X	X							X	
Mitsubishi Denki																						
MELCOM 70	71						X				X	X	X	X	X	X						X
MELCOM 83	69	X						X	X			X	X	X								X
Modular Computer																						
MODCOMP I/5	71		X				X			X		X	X	X	X	X	X	X		X	X	
MODCOMP I/15	71		X				X			X		X	X	X	X	X	X	X		X	X	
MODCOMP II/5	72		X				X			X		X	X	X	X	X	X	X		X	X	
MODCOMP II/10	72		X				X			X		X	X	X	X	X	X	X		X	X	
MODCOMP II/12	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP II/20	72		X				X				X	X	X	X	X	X	X	X		X	X	
MODCOMP II/25	72		X				X				X	X	X	X	X	X	X	X		X	X	
MODCOMP II/26	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP II/26 CP	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP II/201	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP II/221	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP II/231	74		X				X				X	X	X	X	X	X	X	X		X	X	X
MODCOMP III/5	72		X				X				X	X	X	X	X	X	X	X		X	X	
MODCOMP IV/10	73		X				X				X	X	X	X	X	X	X	X		X	X	
MODCOMP IV/25	73		X				X				X	X	X	X	X	X	X	X		X	X	
Nihon-Denki																						
NEAC M4	69							X		X		X				X						X
NEAC 3200 M30	71						X		X			X		X		X						X
NEAC 3200 M50	71						X			X		X		X		X						X
JEC 5							X		X							X						X
Nihon Minicon (Nova) N-Model 01							X			X		X	X	X		X						X
(Nova) N-Model 02							X			X		X	X	X		X						X
(Nova) N-Model 03/SC							X			X		X	X	X		X						X
Nihon Musen JAC 120M-520	70							X		X		X	X	X		X						X
Nord 1	69						X				X	X	X	X	X	X	X			X		X
5, 10, 20	73		X				X				X	X	X	X	X	X						X
Nuclear Data ND 812	70		X			X			X			X	X								X	

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Oki-Denki																						
OKITAC 4300S	69						X			X		X	X	X	X	X						X
OKITAC 4300E	69						X			X		X	X	X	X	X						X
OKITAC 4500	70						X				X	X	X	X	X	X						X
OKITAC 4000	71						X				X	X	X	X	X	X						X
Ordoprocesseurs																						
Ordo 16A	71		X				X		X					X				X				
MF 300	71						X		X				X	X	X			X				
Philips Electrologica																						
P850	71		X				X		X								X	X	X	X	X	X
P850M	73		X				X		X								X	X	X	X	X	X
P855M	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X
P860M	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X
P880	71		X				X				X	X	X		X	X	X	X	X	X	X	X
P/9200	69						X				X	X	X	X	X	X	X	X	X			X
PRIME Computer																						
PRIME 100	72		X				X			X		X	X	X	X	X				X	X	
PRIME 200	72		X				X			X		X	X	X	X	X				X	X	
PRIME 300	73		X				X				X	X	X	X	X	X				X	X	
R2E MICRAL	73		X		X					X		X	X	X	X			X				
Raytheon RDS-500	73						X			X		X	X	X	X	X					X	
704	70		X				X			X		X	X	X	X	X	X	X		X	X	
706	69						X			X		X	X	X	X	X	X	X		X	X	
707	72		X				X			X		X	X	X	X	X					X	
Regnecentralen																						
RC 7001	71						X				X	X	X	X	X	X						X
RC 7002	72						X				X	X	X	X	X	X						X
RC 7003	72						X				X	X	X	X	X	X						X
RC 7004	71						X				X	X	X	X	X	X						X
RC 7004SC	71						X				X	X	X	X	X	X						X
Ricoh RICOM-8	71							X	X			X				X						X
Selenia GP-16	70						X			X				X		X			X			
GP-160	73		X				X			X		X	X	X	X	X			X			
Siemens 101	68						X				X						X	X	X	X		X
301	69		X					X		X				X	X		X	X	X	X	X	X
302	67		X					X		X				X	X		X	X	X	X	X	X
303	65		X					X			X			X	X		X	X	X	X	X	X
304	67		X					X			X	X	X	X	X		X	X	X	X	X	X
305	67		X					X			X	X	X	X	X	X	X	X	X	X	X	X
306	70		X					X			X	X	X	X	X	X	X	X	X	X	X	X
320	72		X				X				X						X	X	X	X	X	X
404/3	70	X	X				X				X	X	X		X		X	X	X			X
404/6	70		X				X				X	X	X	X	X		X	X	X			X
PR 330	73		X				X				X	X	X		X	X	X	X	X	X		X
Spiras Systems																						
SPIRAS-65	69		X				X				X	X	X	X		X					X	

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Systems Engineering Labs SEL 71	72		X				X				X		X	X	X	X	X	X		X	X	
SEL 32	75	X					X			X	X	X	X	X	X	X	X		X	X		
Takachiho TK-70	70						X		X			X	X	X		X						X
TK-7100	71						X		X			X	X	X		X						X
Teac TEAC-16	70						X		X				X	X	X	X						X
Telefunken TR 86	68							X			X	X	X	X	X	X	X					X
Telemecanique T621	73				X				X			X	X	X	X	X		X	X			
T1000	71		X				X			X		X	X		X	X	X	X	X	X		X
T1600	72		X				X			X		X	X	X	X	X	(2)	X	X	X		X
T2000	69		X				X				X	X	X		X	X	X	X	X	X		X
T2000/10	72		X				X			X		X	X		X	X	X	X	X	X		X
T2000/20	72		X				X				X	X	X		X	X	X	X	X	X		X
Texas Instruments TI 960A	71		X				X				X	X	X	X	X	X	X	X	X	X	X	
TI 960B	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
TI 980A	72		X				X				X	X	X	X	X	X	X	X	X	X	X	
TI 980B	74		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Toshiba TOSBAC 40A	70						X				X	X	X	X		X						X
TOSBAC 40B	71						X					X	X	X		X						X
TOSBAC 10	71					X			X			X	X	X		X						X
TOSBAC 10E	71					X						X	X	X		X						X
Varian Data 520/i	68		X		X					X		X	X	X	X		X	X	X	X	X	X
620/f	70		X		X		X			X		X	X	X	X	X	X	X	X	X	X	X
620/f-100	72		X				X			X		X	X	X	X	X	X	X	X	X	X	X
620/i	67						X			X		X	X	X	X	X	X	X	X	X	X	X
620/L	71		X				X			X		X	X	X	X	X	X	X	X	X	X	X
620/L-100	72		X				X			X		X	X	X	X	X	X	X	X	X	X	X
622/i	68						X			X		X	X	X	X	X	X	X	X	X	X	X
V71	74		X				X			X		X	X	X	X	X	X	X	X	X	X	X
V72			X				X			X		X	X	X	X	X	X	X	X	X	X	X
V73	73		X				X			X		X	X	X	X	X	X	X	X	X	X	X
V74	73		X				X				X	X	X	X	X	X	X	X	X	X	X	X
Varisystems PAC-16			X				X					X									X	
P2000	69		X				X				X	X			X	X	X	X	X	X	X	X
Westinghouse 2500	71		X				X				X	X	X	X	X	X					X	
2550	72		X				X				X	X	X	X	X	X					X	
Xerox Sigma 3	70		X				X				X	X	X	X	X	X	X	X		X	X	X
530	73		X				X				X	X	X	X	X	X	X	X		X	X	X
Yasukawa-Denki MEMOCON-16	70						X		X			X		X		X						X

SEARCH CHART—MINICOMPUTERS

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Zuse Z.43	69						x					x	x	x	x	x	x					x

Notes:
(1) Dietz Mincal 621 is marketed in France and Italy under the label Telemecanique T621.
(2) Telemecanique T1600 is marketed in West Germany, Netherlands, Scandinavia, and Eastern Europe under the label Dietz Mincal 1600.

INTRODUCTION TO MINICOMPUTERS

OVERVIEW

The revolution is over. Long live the revolution. The impact of the minicomputer has indeed been revolutionary. As problem-solving tools, their impact has been dramatic. But the torrent has matured to a broad, sweeping river. Indeed, so varied are the options facing the designer today that the very term "minicomputer" is in danger of losing its meaning.

While the range of solutions now spans a complete spectrum — from smallest microprocessor to the grandest minicomputer facility, the fundamental truth remains. The minicomputer represents the fruitful, joyful conjunction of technician and user. The technician can achieve perceptible goals within perceptible time; the user acquires a viable mechanism at reasonable cost.

This paper describes the early days, the frenetic growth, coming finally to a review of present technology. It describes applications that are well suited to this technology, and, by example, the advantages and disadvantages of using a particular technology. Some notes and methodology are presented to help the potential user survive the hazards of selecting a vendor. In applying technology, the problem is to choose from gradations of performance and variations in types of technology delivery: service bureau vs system supplier vs computer vendor.

Finally, in the last section, the broad trends that have influenced small-machine development in the past are cataloged and extrapolated into the future.

The word "minicomputer" became popular in 1968, to categorize a growing number of small, general-purpose computers. These machines were introduced initially to bring software solutions for the limited processing tasks of data acquisition and communications. These vintage machines, many from new vendors, generally conformed to the following descriptions:[1]

- Basic system configurations cost $25,000 or less.
- 4,096- or 8,192-word core memory.
- Programmed in Assembly language (and less often in FORTRAN).
- Computer peripherals often restricted to Teletype and paper tape.
- Usually supported customer hardware (sensors, communications lines, and control lines).

The scope of this report, however, is more than just "those processors that cost less than $25,000." Today, minicomputer is less a description of a black box than a philosophic approach to problem solving:

> "Give me just the right amount of hardware and software to solve my problem."

The technology today is broad. It is bounded by the $1,500 "system" based on the Intel computer-on-a-chip (or three chips), and a vast PDP 11/45 network from Digital worth a quarter million dollars including terminals, peripherals, and discs. With such scope it is clear why the application environment is boundless.

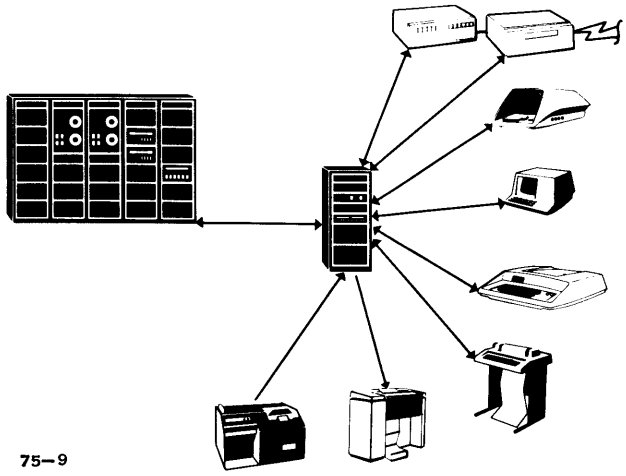

Figure A. Digital Equipment TC/D (Terminal Control Enhancement): up to 80 devices can connect to four such secondary TC/D processors; the secondary connects to the host processor at left

HISTORY

The computer industry dates from about 1954. Only then did the number of machines extant warrant the name "industry." In the first decade the trade boomed. Initially, reliability was obtained only at great expense, but transistor logic solved the problem of costs. As business organizations became acquainted with computing, configuration sizes grew, and the process was still very expensive. Operating systems were invented to harness the larger number of hardware units, and languages were put in the field to speed problem solution. Both caused operation inefficiencies, so faster, larger machines were required. The computing resource became centralized and vital to the organization, so time had to be scheduled. Batch operations were the standard, and closed shops the rule. If a task could not be made to conform to this mold, only two alternatives were available: do the job manually or design special hardware to do it.

Upon this scene, in 1962, came Computer Control Corporation[2] and Digital Equipment Corporation with small machines for laboratory applications. Digital opted for a 12-bit word machine that balanced the high cost of memory (a function of word size) against popular transducer resolution (1 part in 1,000, sometimes with a sign). Digital has prospered from that time to now, but development of this avenue of computing has always been servant to hardware advances. The introduction of transistor logic in the early 60's made small computers possible, but the use of integrated circuits in 1968 opened the flood gates of small machine activity.

The hands-on scientist with ill-conditioned data, the small user with limited budget, the executive with untimely reports, all found a new alternative for centralized

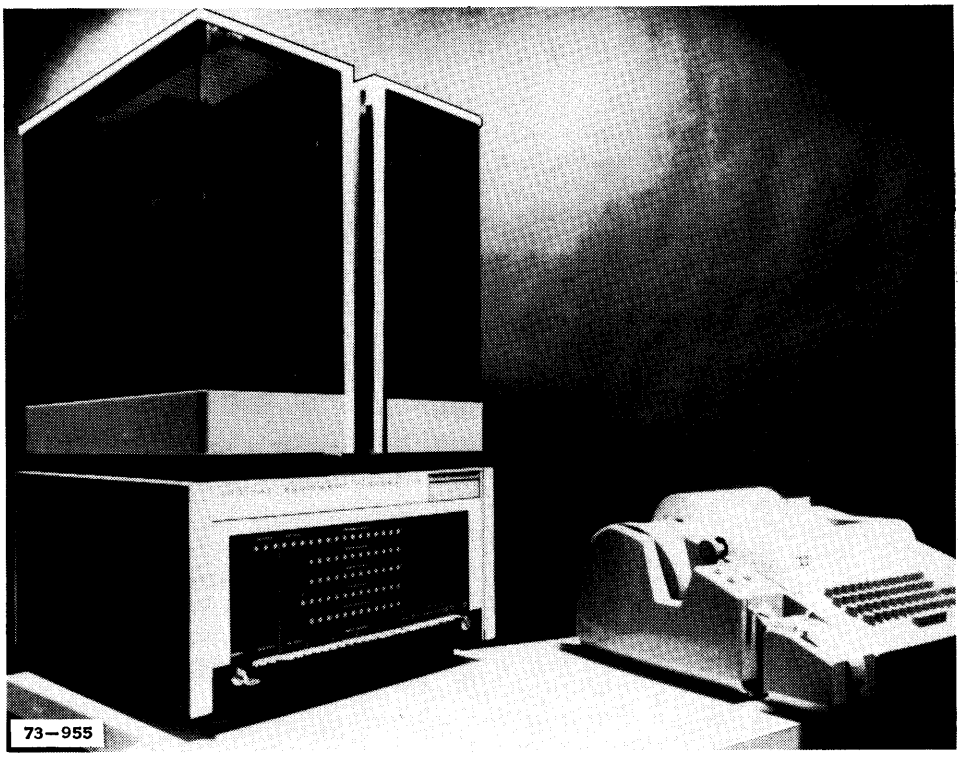

Figure B. First Tabletop Digital PDP-8 Computer System

computing. New minicomputer manufacturers entered the lists monthly until 1970, when the number of vendors stabilized to between 40 and 50 and new product emphasis shifted to low-cost, modest-performance peripherals. Also during this period a large number of small systems houses sprang up. They took the very modular, low-cost components and welded them into systems with software. It took only a modest bankroll to become a minicomputer manufacturer and even less to become a hardware-software shop providing turnkey service.[3]

More recently, other developments have accelerated the production and use of small computers:

- Availability of economical peripherals.
- Large-Scale Integration (LSI) of logic functions.
- Dramatic decline in memory costs (1973-74).
- Accumulation of system software.
- Advances in packaging techniques.

The improved hardware and software have significantly increased speed and reliability. The net effect is a better product at a lower price. With each quantum step of improvement, "minis" have gained wider acceptance and a broader range of applications.

The following table shows how two models of the Nova minicomputer from Data General Corporation compare with Univac 1[4] ,the first electronic commercial processor.

Date	CPU	Add Time (μ sec)	Memory (words x bits)	Cost
1952	Univac 1	4	1,000x48	$750,000
1972	Nova 1200	1.2	4,096x16	$5,200
1975	Nova 2/10	0.8	4,096x16	$3,800

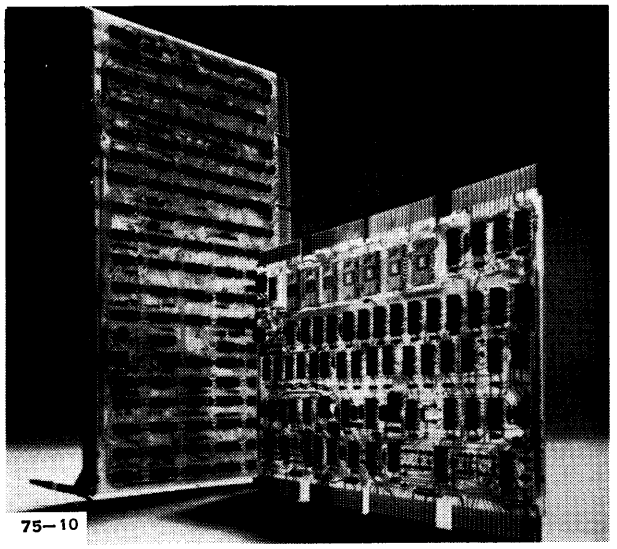

Figure C. The PDP-8/A, Digital's Smallest PDP-8: made up of two modules

Figure D. Alpha/LSI and Naked Mini/LSI

In the early 70's, the path of development was to extend the market upward by offering "bundled" operating systems and language processors. FORTRAN was available from practically all vendors. ALGOL and COBOL derivatives came later — but they came. Disc-based operating system software was so pervasive by 1974 that Computer Automation — ever an OEM supplier — provided one. Entering the last half of the decade, vendors were supplying machines that spoke ENGLISH[5] and employed some of the optimizing features of the very large systems:

- From IBM 360/85, circa 1968, comes the "cache" memory now on the Data General ECLIPSE.
- From the B5000, circa 1962, comes the "stack" architecture of the HP3000.
- From the IBM-360, circa 1963, comes the "dynamic control store" of the Varian V70 Series and Hewlett Packard 2100MX.

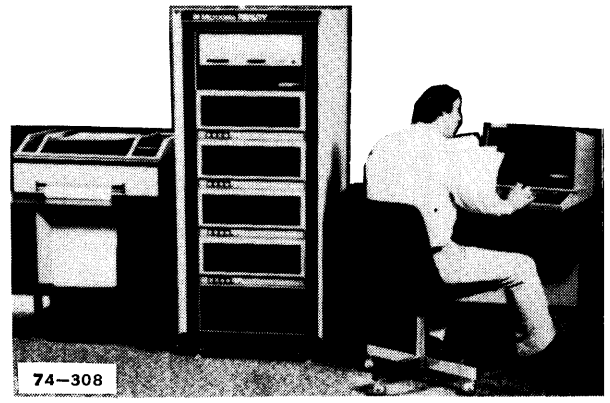

Figure E. Reality Speaks ENGLISH

At the other end of the scale, LSI allows a computer (with reasonable performance) to be built on very few chips for $500 and yet have a mean time between failures (MTBF) approaching 50,000 hours. Thus, today's minicomputer range is so broad that equipped with a variety of peripherals, it can be fitted for applications with budgets ranging from $10,000 to several millions of dollars. The unifying notions are no longer size or price. The term "minicomputer" now denotes modular construction and task-oriented system design.

MINICOMPUTER TECHNOLOGY

The "mini" in minicomputer acknowledges that these units have generally been associated with limited size, limited price, limited performance, and limited support from the manufacturer. Manufacturers are removing the "limitations" previously associated with minicomputers as fast as they can; superior performance and software are now available — at a price. Discussion will be anchored on middle-line minis, while the extremes of micros computers and mini-facility configurations are spotlighted.

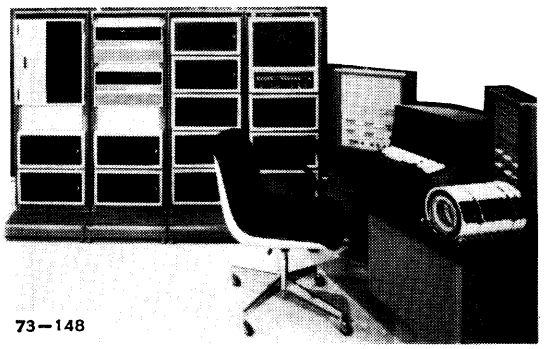

Figure F. Hewlett-Packard HP 3000

Design Philosophy

Minicomputers are designed as general-purpose computers with a mix of logical, arithmetic, and input/output (I/O) functions. These features are complemented with packaging that permits easy build-up from small configurations. Processor options, memory, and peripherals can, in general, be added by plugging-in circuit boards to prewired spare connectors in the computer chassis.

Minicomputer chassis are usually made of light sheet metal, which is satisfactory for practically all commercial installations. If the computer will be moved frequently, a specially ruggedized model might be selected. Recent packaging trends have been toward large circuit boards, which reduce the number of mechanical connections and make the units more reliable. For example, the entire Nova computer is contained on a single 15-inch-square circuit board; the Interdata 7/32 on two 15-inch boards.

Manufacturing economies are often effected by using power supplies of questionable merit. More than one manufacturer has had greater difficulty with the system's power supply design than with the processor.

The computer design can be shaded towards a broad applications market. A manufacturer can include many features as standard if the intended market requires those options. Machines intended for word-processing or accounting applications generally use shorter word lengths with multiple word instructions, and they implement hardware decimal arithmetic. Machines intended for scientific calculation or process control applications generally use long word lengths and frequently hardware for floating-point arithmetic.

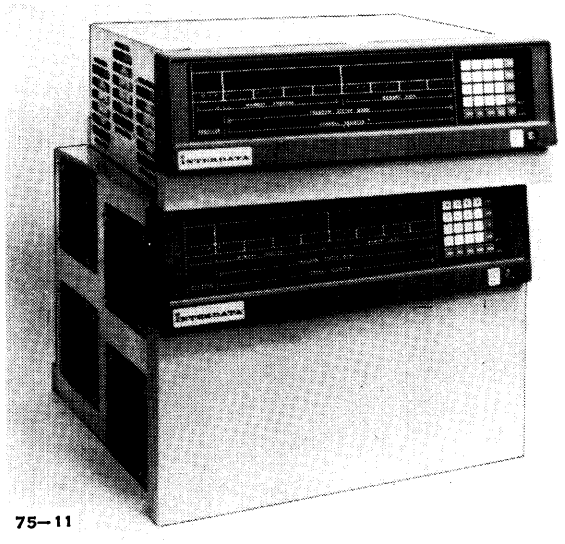

Figure G. Interdata Models 7/16 and 7/32

Table 1 summarizes the general characteristics of minicomputers. The "average" column presents a picture of the middle-of-the-line mini. Minimum and maximum columns indicate the range from very small, single task computers to very large, facility-oriented machines. A "maximum" mini would be supported with many peripherals, an operating system, and, probably, a large staff.

Table 1. Minicomputer Characteristics

	Minicomputer Size		
Characteristics	**Minimum**	**Average**	**Maximum**
Memory			
Word length (bits)	8	16	32
Type	Core or semiconductor	Core	Mixed
Size (bits)	256-4,096	To 65,536	To 262,000
Increment size (words)	256	8,192, 16,384	16,384, 32,768
Cycle time (μsec)	8	0.75-1.75	0.64 to .3
Parity check	No	Opt	Std
Memory protect	No	Opt	Std
Direct addressing (words)	±128	512-4,096	All of memory
Indirect addressing	No	Yes	Multilevel
Sub-word addressing	No	Byte, half-word	Byte, bit
Central Processor			
General-purpose registers	1, 2	2-4	To 64
Index registers	0	1-4	15
Hardware multiply/divide	Opt	Std	Std
Floating-point hardware	No	Opt	Std
Double-word instructions	No	Opt	Std
Input/Output			
Programmed I/O channel	Yes	Yes	Yes
I/O word size (bits)	8	8/16	8/16
Priority interrupt lines	1	1 std, up to 64	4 std, up to 256
Direct memory access	Opt	Std	Std
I/O maximum transfer rate, DMA (words/sec)	125,000	To/Million	To 5.0 x 10^6
Other Features			
Real-time clock	Opt	Yes	Yes
Power fail/restart	Opt	Yes	Yes
Largest disc (megawords)	4.8	9	85
Assembler	Yes (not macro)	Yes	Yes (macro)
Compiler	BASIC, FORTRAN	BASIC, FORTRAN, COBOL subset	BASIC, FORTRAN, COBOL, ALGOL
Operating system	Yes: cassette or core-based cassette	Yes: disc, tape, or core-based	Real-time, foreground/background, time sharing
Percentage of Units Installed	38	60	2
Purchase Price*	$1,000	$8,000	$22,000
Est. Annual Growth	+100%	+30%	+200%

*Purchase price is for the average computer in its class without peripherals.

Central Processor Unit (CPU)

The central processors are usually single-address, binary units with negative numbers expressed in two's complement form. Central processors vary most in the number of accessible registers, instruction sets implemented, instruction decoding technique, interrupt handling capability, and I/O facilities.

Arithmetic and logical operations are performed on data brought to the CPU from memory. The data is held and transferred between registers during these operations. A register is merely an assemblage of electronic components (flip-flops) that contain the data word while it is being processed. Some registers are accumulators (of data).

The elements of the computer are connected by buses over which data and instructions move. Generally two buses are used: one for transfers between memory and CPU and another for transfers between the CPU and its peripherals (the outside world).

Most processors use one-word instructions with the following format: 4 to 6 bits for operation code, 2 to 4 bits for modification field, and 8 or 9 bits for the address field. Most of the operation codes are used for memory referencing instructions. Non-memory referencing instructions use additional bits of the instruction word to define the operation code; thus, the number of instructions can be quite large. Most have an instruction set of 64 to 100 instructions; some have many more, over 200. The modification field further defines the instruction, usually specifying an addressing mode (indexing, indirect addressing, or both) and a literal (immediate) address; or specifying a two-word instruction. The address field provides an address increment or a literal. The effective address is calculated in accordance with the address mode; usually the contents of the program counter specify the base address and the address field specifies an increment or the core address within a page. Some minis have page registers that can be loaded with the page number of the core area from which operands are being extracted. Two-word instructions allow direct addressing of large memories — a common method of extending the addressing capability for large minis. The Interdata 7/32, for example, can address 1 million bytes of memory.

The basic instruction set usually includes the arithmetic operations of fixed-point add and subtract; multiply and divide are implemented by subroutine but usually are available with optional hardware.

Double-precision operations are sometimes provided. Most larger minis offer floating-point hardware as an option, but this feature is usually expensive. All offer some form of logical, compare, and shift operations. Many also offer byte and bit manipulation instructions. The I/O instruction is usually very general. It transfers control, status, and data words between the peripheral devices and the processor's accumulator. Commonly, the I/O instruction also provides control of optional features. They are addressed as external devices.

Classical CPU design includes a program counter, an accumulator, an accumulator extension register, and one or more index registers. Newer designs provide a number of general registers that can be used as accumulators or index registers. Sometimes a condition register keeps track of processor status with respect to overflow, operation mode, or the result of a comparison.

Some newer systems, such as the Digital PDP-11, feature two-address instructions that specify source and destination addresses calculated using the contents of general registers. This architecture lends itself to real-time processing and multiprogramming because the general registers can operate as stack pointers for stack manipulation and context switching.

Unfortunately, many manufacturers are stuck with old processor designs because of the large investment in software. Microcoding, however, has allowed some freedom; the processor can utilize modern design but emulate older systems in microcode for software compatibility. This need for compatibility places many restrictions on system design, but it does protect the users' investment in software.

Memory

Memory technology has advanced rapidly. In the early seventies, many people predicted that ferrite cores as CPU local memory would be replaced with solid-state memory. The decline in the cost of core, however, has kept core the standard for minicomputer memory. Semiconductor memory is faster, but it forgets when power is removed. A third type is Read Only Memory (ROM). As its name implies, it can only be read, not written. This restriction has two attributes: it is nominally twice as fast as a read/write memory having the same clock rate, and it is secure from inadvertent modification. Therefore, fixed, unchanging data or code can be located in ROM. Often all three types are offered by a manufacturer and can be mixed on a system.

Computer memory can be functionally divided into program storage and data storage. The CPU accesses a program instruction and then, based upon the instruction, recovers or replaces data. Besides communicating with the CPU, memory usually can communicate with I/O devices via direct-memory access (DMA) facilities. Thus, both the CPU and I/O devices share the memory bus.

Memory size can range from a few words for a small, fixed process to hundreds of thousands of words for a time-constrained major activity.[6] The addressing techniques used by the instruction set are often supplemented by special memory "mapping" hardware for very large memories. The mapping hardware provides selection of a particular block of physical memory. Memory is usually subdivided into modules of 4K, 8K, or 16K words; some vendors, such as Modular Computer and PRIME Computer, have 32K-word boards. More elegant memories have multiple ports of entry so that a module can be shared by two or more CPUs, or by a CPU and a DMA device. Multiple ports can double or triple throughput if data in one memory module can be processed while data is transfered between other memory modules and peripheral devices.

Memory word size can be extended to include provision for error recognition and correction. Simple detection is afforded by adding a parity bit. If several more bits are added to each word, special hardware can not only recognize errors but also correct them.

Memory protection can be accomplished word-by-word by adding a protect bit to each word. Area protection, using separate logic that establishes upper and lower bounds for protected memory, is much more common.

Core memory construction is very much a manual process; fine wires must be strung through the ferrite doughnuts. Consequently, memories are made in places

where labor costs are low — generally outside the United States. This construction method also makes it very expensive to thread tiny ferrite cores, and faster memory speeds are obtained by making the cores smaller. Thus, there is a natural price break for core memory with a cycle time of about 1 microsecond.

Instruction Set

The computer's instruction set defines the most primitive functions that are available to the programmer. When these operations are given mnemonic names (such as ADD for addition operator, BEQ for branch if registers equal) and combined with the rules for instruction use, the result is the machine's Assembly language.

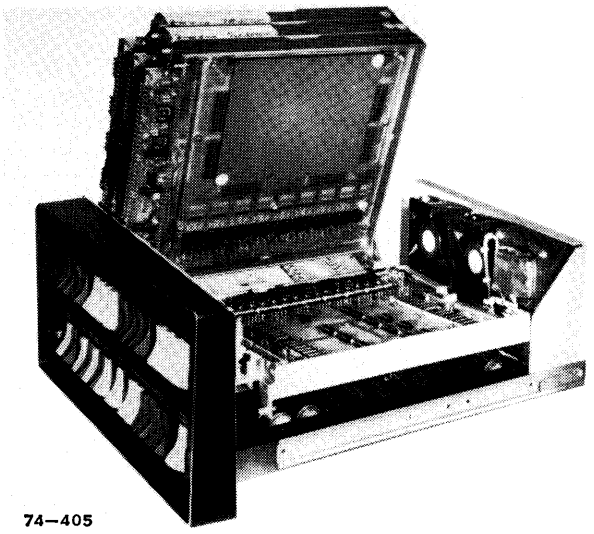

Figure H. MODCOMP II/12 with Two 32K-Word Memory Boards

A minicomputer's vocabulary usually consists of from 70 to 200 different operations, including memory reference, logical register manipulations, comparisons, and transfer instructions. The computer word has fields committed to define an operator, a memory address, and modifications to operator or address fields. Modifications to instructions may specify variations on a basic operator; modification of addresses defines indirect or indexing functions.

The computer's instruction set is usually determined by fixed wiring of electronic components within the machine. Most recent designs however, employ a concept first advanced by M. V. Wilkes in 1951.[7] Wilkes proposed that a program, that is, a sequentially executed procedure, could be brought inside the CPU and used to define the instruction set of the machine. An ADD instruction, a single operation as seen by the programmer, would actually be effected inside the CPU by a subroutine of microinstructions. Each microstep would deal with intrinsic computer operations that are more primitive than the Assembly language.

This approach, called firmware or microcode, provides a means of making changes in a computer's instruction set without scrapping the hardware design. This facility is of limited value to the user except for special circumstances, such as emulation or specialized, time critical instructions. It does permit the manufacturer, however, to extend or purify the computer's design with minimum pain. Firmware is of negative value if this approach reduces computer throughput. Within the past few years, the increased speed of logic circuits has made the technique practical. Early Interdata machines, for example the Model 3, used firmware but were slower than comparable hard-wired machines. ROM was used for its speed and security. Today, a number of manufacturers — Varian, Hewlett Packard, Prime — have

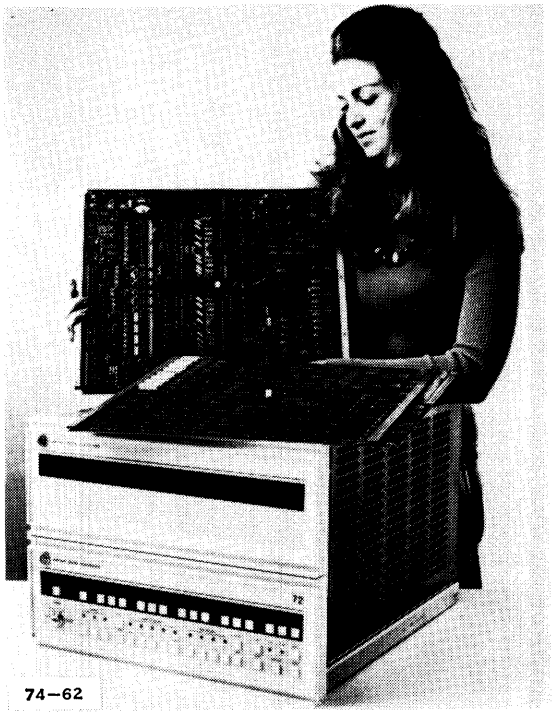

Figure I. Varian Data Machines V-72, Second in V70 Series

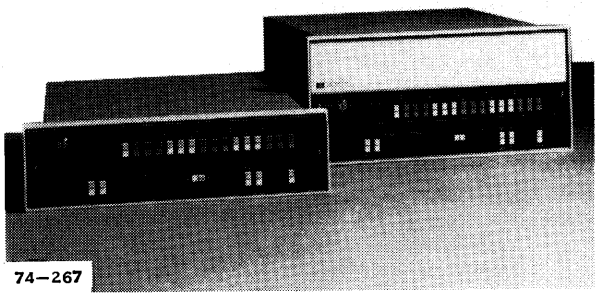

Figure J. Hewlett-Packard 21MX Computers

relaxed the read-only constraint and provide writable control store (WCS) for their systems. The speed of solid-state memory makes WCS practical. Now, for some systems, the instruction set can be modified or extended dynamically while the machine is operating.

Input/Output

Two basic means of I/O are available: programmed and automatic. The processor's data channel (or bus) is generally one word wide (16 bits for a 16-bit word processor). The channel transfers control and status information as well as data. For programmed I/O, all information is passed as a result of executing programmed instructions. For automatic I/O, control information is passed to a device controller specifying the mode of operation, the memory area involved in the transfer, and the amount of data to be passed. Once the transfer operation begins, it proceeds to completion using the DMA facility without further intervention by the program. Often, the completion of a block transfer causes an interrupt from the device controller to signal that the device is available for another transfer.

Fast devices such as tapes, discs, and drums require automatic block I/O. Slower devices can operate under either regime. Since hardware controllers for doing block I/O are relatively expensive, control information governing automatic block transfers can reside in special memory locations associated with one or more data channels, or it can reside in the device controllers.

Most minicomputer vendors provide controllers for industry standard I/O devices: high-speed paper tape units, punched card readers and punches, line printers, magnetic tape transports, plotters, displays, and Teletype units. Almost all manufacturers provide mass storage devices such as disc, drum, or tape for their products. Magnetic tape cassettes and floppy discs are among the latest offerings from the vendors. In addition, a number of independent firms offer peripherals with controllers and controller software for the popular minicomputers.[8]

Interrupt Function

The interrupt facility allows the computer to recognize the occurrence of an asynchronous external event. Then, the CPU pauses in its processing to service that event. Software analysis of the interrupt is required on the simpler minis to identify what to do. More sophisticated schemes provide a transfer vector and interrupt priorities or levels.

Interrupts include both external — outside world events — and internal — machine-generated events. Internal interrupts, sometimes called traps, include power failure sensing, illegal instructions, memory parity, memory protect, and real-time clock events.

When an interrupt is recognized, processor control is transferred to an interrupt processing routine. At this point, it is usually necessary to save the current status of all registers that will be used by the interrupt processor so they can be restored when the interrupt routine is finished. This status-saving/restoring is done automatically on a number of computers.

External interrupts are under program control and can usually be individually disabled or inhibited. A disabled interrupt level ignores an interrupt signal. An inhibited interrupt level stores the signal but does not cause an interrupt until the inhibition has been removed.

A hardware provision blocks out all interrupts until the interrupt servicing subroutine has stored the status of the processor: the contents of the accumulators, index registers, program counter, and overflow. In addition, hardware also blocks out all interrupt levels of an equal or lower priority than the one currently being serviced.

When each interrupt condition is connected to a unique interrupt level, the source is identified immediately. When several interrupt conditions are connected to a single interrupt level, additional processing is required. Some systems have a hardware provision for reading the address of the highest-priority device with a single I/O instruction. Others require a separate I/O instruction to test each device status flag. Most minis provide multiple interrupt levels; thus devices that require a fast response time can connect to unique interrupt levels, while several devices that can tolerate a longer response time are multiplexed into a lower-priority interrupt level. Some interrupt systems automatically inhibit the interrupt system from the time an interrupt is granted until the system is released by instruction. Others have hold-and-release interrupt instructions.

The efficiency of an interrupt system is determined by the time required for the overhead functions: to identify the interrupt source, to inhibit further interrupts until preliminary servicing is finished, and to initiate the interrupt service routine. These operations can be performed by hardware, software, or a combination of the two.

Software

All manufacturers supply "system software" to assist the user in developing applications programs. The minimum level of support includes a text editor, assembler, loader, and utility subroutine package. Most vendors also supply FORTRAN and BASIC language processors together with an operating system that permits their use. Such systems generally require at least 16,000 words of local memory and some form of high-speed data entry (disc, magnetic tape, or fast paper tape).

More elaborate operating systems supporting time-sharing and real-time operations are available from most

vendors. ALGOL, COBOL, and subsets of these languages are also available for some systems. At this level, diagnostics, debugging aids, and useful subroutine libraries are common.

Training

The major vendors conduct maintenance and programming courses for their customers. Typically an arrangement is made with the salesman when a customer wants to attend these sessions. Detailed reference material defining hardware and software products is generally available free from all manufacturers.

Successful minicomputer user groups that share software and product expertise are a rarity. [DECUS (Digital Equipment User's Society) is a notable exception.] Because machines are often dedicated to a single task, there has been no great pressure from users to maintain communication with each other. The impetus for such activity has been an off-again, on-again interest of the manufacturers. The trend to facility-oriented, big minis may change this situation.

APPLICATIONS

Appropriate applications for minicomputers are as numerous as leaves on a tree. The key attributes of a task to make it a candidate for solution with today's small computer technology are as follows:

- It requires computation or logical testing.
- Process is repetitive — frequently or cyclically performed.
- Manual method is either too slow or too inaccurate.
- Requirements change with time.
- Expenditure must be modest.
- Process must operate unattended.

Application areas for which minicomputers are used are so broad that whole fields of specialization develop within them. Process control applications, for example, can range from the control of a small, simple laboratory experiment to the control of a large oil refinery or chemical plant. Automating the laboratory process affects little outside the laboratory involved. Automating an oil refinery or chemical plant, however, has ramifications far beyond the computer site and can affect hundreds of people and pieces of equipment. In fact, the personnel problems in setting up a large process control center are so great that most books on the subject devote large portions of the text to ways of handling them.

Small computer applications can be divided into five broad categories, as shown in Table 2. For each application, special equipment and software have been developed and applied, depending on the size of the task in hand. Each satisfies one or more of the attributes identified previously. For further reference, the bibliography has been organized to reflect the breakdown shown in Table 2. Regardless of the nature of the task, the preeminent requirements for successful computer application are that management understand the task and make a solid commitment to the computer-based solution.

Table 2. Applications of Minicomputers

Computation	
	Accounting Functions
	Sales Analysis
	Order Entry
	Inventory
	Production Scheduling
	Bill of Materials
	Engineering, Scientific Computation
	Time Sharing
Word Processing	
	Key to Disc, Tape
	Text Editing
	Typesetting, Photo Composition
	Computer-Aided Design
	Computer-Aided Instruction
Communications	
	Remote Batch Terminal
	Line Concentrator
	Front-End Processor
	Message Switching
Data Acquisition	
	Telemetry Decommutation
	Data Reduction
	Data Conversion
	Laboratory Experiment Control
	Medical Test Analysis
Process Control	
	Automatic Testing
	Numerical Tool Control
	Traffic Management

Because of their low cost, minicomputers tend to be located close to the hands of the user. Thus, minicomputer systems design must be very attentive to the human engineering of hardware and software.

Rather than look at the uses of a minicomputer from the point of view of a specific application, or vertical industry, one can look at the different ways the computer is used regardless of application. Viewed thus, minicomputers are used in the following ways:

- As stand-alone computer systems.
- As dedicated computers performing the same operation day after day.
- As modules in a hierarchical system.

As a stand-alone processing system, the computer performs a variety of functions depending on its programs. The stand-alone system can be a simple one, with small memory and a single typewriter station with slow paper tape for I/O. Software can include an assembler; a loader; I/O handlers; editing, debugging, and diagnostic routines; and some math subroutines.

On the other hand, the stand-alone system can be large and comprehensive. It could include a large internal

memory, a disc for external storage, and multiple I/O devices, such as key-entry stations, paper tape, magnetic tape, and printers. Software can include a disc operating system with control for several real-time processes in the foreground, and priority-selected batch processing facilities for programs written in an Assembler language, FORTRAN, or ALGOL in the background.

Dedicated processors can be used as an extension of the operator, who can do the job better, as in product or environmental testing, process monitoring, and data acquisition.[9] The computer interfaces directly to control or monitoring equipment and is programmed for interaction with the operator. Parameters for the function performed can be provided by the operator or by sensors. The computer acquires data, analyzes it in relationship to the parameters, and communicates the results to the operator or to equipment that it controls. In addition, the computer can prepare and maintain statistical records on data received.

A minicomputer can also function as one module in a large computer system, preprocessing data for the larger computer, handling communications among many terminals, or performing most functions on its own and calling on the large computer only when problems are too large or too complex for it to handle. These systems can be very efficient with each component performing those functions for which it is best suited.

There is a trend to decentralized systems that operate both as stand-alone computer centers and as terminals to a central facility. In this situation, a minicomputer (or smaller microprocessor) may be located at the remote sites while a larger minicomputer or maxi time-sharing system operates as the parent at the central site. This configuration is attractive to organizations with many remote offices. Large central files need to be maintained, and they are updated from the field offices periodically. Computation needs of both central and remote offices are performed by the on-site processors.

ADVANTAGES AND DISADVANTAGES OF MINICOMPUTERS

The greatest advantage of the minicomputer, in comparison to large computer systems, is that a user can buy the specific amount of computer power required for a job. The minicomputer is general-purpose and can be used to perform any function, within its size limitation, for which a program has been written. Because the overall cost is low, the minicomputer tends to be located at the problem site rather than in a computer center, and users can interact with it directly. It can be dedicated to a single problem or related set of problems. It can be fine-tuned to solve a problem as the problem should be solved. A general solution need not be adopted; a task-efficient approach is acceptable.

Generally, minicomputers are compact and rugged and do not require specialized environments. In addition, most minicomputers are as fast as, in some cases even faster than, their larger counterparts and can provide instantaneous response to an external request for service. Because a minicomputer is used by a smaller group of people, the effect of a computer malfunction is not as catastrophic as it is in a larger system. Indeed, hardware redundancy can be structured at moderate cost.

The greatest disadvantage of minicomputers to date has been the difficulty of programming because of the limited amount of software supplied with a system. This difficulty is gradually being overcome, especially for older designs. Vendors are commonly supplying operating systems that allow program development concurrent with on-line tasks.[8] Various manufacturers now supply ALGOL, FORTRAN, BASIC, and COBOL-subset language processors.

The other major disadvantage is the availability of field engineering and spare parts. This problem is endemic and not necessarily confined to new or small manufacturers. As the industry matures, more systems are being based on vendor-supplied operating systems and languages, and system software support is an important factor.

The very reliability occasioned by the move to large boards and wire-free packaging has created a spares problem. When the PDP-8 had 60 circuit boards of nine types, a spares kit could be obtained for a reasonable price. However, a spare for the Nova CPU is another complete CPU.

Other disadvantages relate to manufacturers' attempts to reduce costs. These items tend to be irritating rather than serious: switch toggles that break, lamp sockets poorly made, or inaccessible fuses and lamps. These problems tend to vary from manufacturer to manufacturer.

SELECTING A MINICOMPUTER

There is no best computer on the market, no computer has the lowest overall price/performance ratio, and no one can guarantee which computer is the best for a particular user application. On the other hand, many good computers are available, many computers have good price/performance ratios, and several computers can probably do a particular job well. The problem is to identify those computers.

Unfortunately, selecting a computer for a specific job is not easy. Still, if done without panic and without rush, the rewards of the search can include raising the staff's technical competence, understanding the individual application better, and building a firm foundation for the decision-making that will accompany future developments within the application.

The wise selection of a computer depends on the selector(s) fully understanding the application. A number

of people can be involved, but cooperation among the ultimate users is essential. The group of end users must develop a set of criteria for selecting a suitable computer; and these criteria must reflect the needs of each user's application area. Expressing these criteria in computer terms is a non-trivial task that must be accomplished, and should involve someone with a computer background. Because it is human nature for each to consider his personal needs most important, some member of the selecting group must have responsibility for leading the group toward satisfactory compromises. Such compromises might be expressed as weights applied to the selection criteria.

Developing the weighted selection criteria is an educational process and is the hardest part of the selection procedure. Application areas must be viewed in terms of what is now done, what can be done better by computers, and what can be expected in the future. Each person in the group must appreciate what computers can do from the functional point of view; each must discern that computers vary in architecture and capability; and each must understand that, whatever the hardware capability, the viability of the system is dependent on successful software.

The goal in any selection procedure is to choose a vendor or vendors that present the best combination of technical solution and system cost. Depending on the size of the project, the procedure for selection will be quite detailed or accomplished in an afternoon (with the back of an envelope for notes).

This procedure can be adjusted as necessary to suit large or small projects. The following algorithm is appropriate for selection:

- Establish minimum performance and maximum cost standards.
- Determine performance criteria, note thresholds or minimum performance levels, for example band width and speed.
- Relate performance criteria to computer and peripheral characteristics.
- Determine vendor characteristics that are important to the project.
- Assign numerical values to the quantifiable hardware and vendor characteristics.
- Rank the various characteristics and weight them, if necessary.
- Determine total cost of proposed solution — cost of vendor proposal plus cost of internal engineering, management, and programming for the proposed solution.
- Map the performance and price data developed.
- Make a subjective decision based on the clear understanding of cost and performance trade-offs provided by the objective data.

Objectivity can be maintained by setting up important criteria in advance of evaluation. Ranking or weight assignment is done before seeking vendor proposals. Objectivity is guaranteed by using measurable, quantifiable characteristics.

Cost-effectiveness requires considering all elements of a project that contribute to its cost. These factors include training, supplies, and spare parts. Note that even the FORTRAN programmer must relearn the language and the new compiler control mechanisms when moving to new hardware. An inexpensive printer that uses expensive, treated paper may not be a bargain over the system's lifetime.

The final decision is based on solid information. Subjective considerations are restricted to evaluating the importance of adequate cost and performance margins, based on maximum cost and minimum performance initially established. Observe that selection cannot be based on the notion of an absolute performance/cost evaluation. Many criteria, such as personnel experience, are situation- and time-dependent.

The difficult step in this algorithm is the conversion from task specification to computer characteristics. The selection criteria must be expressed in computer terms, and the weight applied to each criterion reflects the importance of that parameter to the particular application.

The following elements of computer systems usually form the basis for selection criteria:

- Central processor.
- Memory.
- I/O structure and channels.
- Interrupt system.
- Standard peripheral devices.
- Software.
- Manufacturer.

Central Processor and Memory

The central processor and memory determine to a large extent the computing power of a computer system. Important memory characteristics are word length, cycle time, and size. Ideally, the word length should correspond to the data precision required by the application. The cycle time determines the speed of the computer, but the user must beware of considering cycle time alone. How efficient is the instruction set for the specific application? For example, fast instruction execution may not offset a communications interface that requires several instructions for each I/O operation.

The memory size determines the complexity and size of programs the computer can run and the type of software that can be supported. Additional memory features that are often important are memory parity and memory protection.

Important central processor characteristics are the instruction set, addressing capability, speed of instruction execution, number and kind of program accessible registers, number of internal interrupts, and optional features.

If the instruction set does not include a required function such as floating-point arithmetic, software routines must perform the operation. These routines occupy memory storage space. Execution time is longer than for a comparable hardware operation. Some minicomputers have control stores (either writable or read-only) that can implement new, specialized instructions. Additional, pluggable hardware can be added to perform the required function. Floating point and fast Fourier transform processors are examples.

Memory organization can have a profound effect on the way in which software is developed. For example, the most successful mini, the PDP-8, has memory allocated in 256-word pages. An instruction can directly reference only those addresses within its page (or a base page). When working in a higher level language, the programmer is masked from such considerations, but inefficient execution times may result if program size passes certain thresholds.

The speed of instruction execution is usually a function of memory cycle time. Each instruction must be fetched from memory, and many instructions require another memory operation for data.

The number, size, and arrangement of index registers and accumulators affect the time required to do a job and the memory space required by the program. Index registers save memory references to software index registers set up in memory and thus cut down on the number of indirect references made. They can make the programmer's job easier for loop control and linking to subroutines. The number of accumulators also determines the precision of arithmetic operations, the ease with which precision can be increased, and, generally, the efficiency of the processor.

The number of internal interrupts and number of optional features offered are factors in determining the flexibility of the processor for a particular application. The selection criteria should specify all optional features required.

I/O Structure

Small computers are often tied to sensor- or operator-based systems, and the I/O structure is a major factor in evaluation. The most common I/O facility for minicomputers is a programmed party-line channel to which peripheral device controllers interface for transferring data, status information, and commands. The number of devices the channel can support and the maximum allowable length of the bus vary from CPU to CPU. Channel performance is determined by the number and kind of I/O instructions and the facilities for determining which device requires service.

I/O transfer rates are affected by the memory addressing techniques, the instructions provided for controlling and testing counters, and other factors such as the elegance of the I/O instructions. Most minicomputers have a generalized I/O instruction that is used to transfer data control words or status words between the accumulator and a peripheral device controller. The instruction set should be examined to determine how easily the processor identifies a device requiring service.

Most minicomputer systems include a direct memory access (DMA) channel to allow high-speed data transfers between peripheral devices and memory, with the data transfers under control of the channel.

Processor time devoted to I/O operations is a function of the number of peripheral devices in the system, their frequency of use, and the execution time of the software I/O routines. Requirements for the application must be carefully analyzed and the criteria defined to eliminate from consideration all computer systems that do not have minimum performance. Vendor proposals should note the number and kind of I/O channels supplied and the costs for extending these.

Interrupt System

The function of an interrupt system is to signal the processor that an untimed (untimely) event has occurred. A priority interrupt system establishes a hierarchy of importance for the attention-getting signals.

A simple interrupt configuration includes one line to which all devices interface. Software analysis is required to determine which device has caused the interrupt and what action to take. The Nova and PDP-8 machines use this scheme. The order in which interrupt servicing routines test the status of devices that can cause the interrupt establishes the priority of the devices.

A true priority interrupt system provides a number of interrupt lines, with a memory location dedicated to each line to select the interrupt servicing routine appropriate to the interrupt signal. This setup significantly decreases the response time of the processor to interrupt signals.

The priority of interrupt lines can be hardwired and fixed, or controlled by bits set in one or more programmable interrupt control registers. Programmable registers make the interrupt system more flexible — important if the various peripheral devices assume different priorities from program to program.

Normally, the instruction set includes a provision for blocking out all interrupts so that crucial processing can proceed, such as a routine to load or store the interrupt control registers. In addition, the interrupt system can block out all interrupts except those of a higher priority until an interrupt servicing routine is finished. The instruction set also includes some means of restoring the interrupt system to its state prior to the beginning of the interrupt servicing routine.

When a program is interrupted, the volatile CPU registers must be saved. This overhead may be handled in hardware or software. The method should be noted in the evaluation.

Standard Peripheral Devices

Vendor-offered peripheral devices and their delivery times may eliminate many minicomputers from consideration by the selection group. Most minicomputer manufacturers do not make all of their own peripheral devices. Instead, they buy standard devices and provide the controllers for a particular computer. Generally, the cost for peripheral devices is relatively higher than that for a processor. Recently, many new products have entered the marketplace. Costs have been dropping for two principal reasons:

- Performance standards have been moderated.
- Large minicomputer sales have permitted volume sales of peripherals.

The alphanumeric CRT/display with keyboard is a good example of how prices have been reduced.

Year	Performance	Price (interfaced)	Vendor
1967	250,000 cps	$40,000	CDC
1972	1,000 cps	3,000	Hazeltine
1975	100 cps	1,800	Digilog

The dilemma faced by the minicomputer manufacturer is which of the many new products to offer with the computer. The dilemma faced by the buyer is how many different vendors to use.

Today, the CPU manufacturer generally offers a wide variety of peripherals, but not necessarily the latest or best. The manufacturer also tends to develop and produce some peripherals, such as Hewlett Packard cartridge discs, Digital DECtapes, Data General cassettes and fixed-head discs.

Meanwhile, the popular computers are supported by many independent vendors who can supply plug-compatible devices. Often, as with a disc, significant software comes from the vendor. These peripheral vendors often are credible though some are not. In the area of peripheral evaluation, much greater emphasis should be on the device's performance in a benchmark situation since only a few devices fit the particular needs of a given project.

Interfaces Available

A majority of minicomputer manufacturers provide interfaces to standard data communications devices, to analog/digital and digital/analog devices, and to sense and signal modules. Some manufacturers specialize in these applications and have extensive hardware options as well as the software to support the equipment.

If the application requires interfaces to special-purpose devices, the selection criteria should include interface requirements. The cost of designing special-purpose interfaces can become a significant fraction of the total project cost.

Software

One of the most important components of a new computer is its software. It is critical to performance and is the most frequently underestimated, misunderstood item in the system budget. Because the cost of minicomputers is small, many minicomputers do not have extensive system software. The selection criteria should include the required software, with weights applied to the desired features for future as well as current needs. In fact, the system software supplied by the vendor controls the ease and speed of applications program development.

If the manufacturer writes off software production costs in the hardware price, the system cost increases as more system software is included. On the other hand, if the user needs system software not produced by the manufacturer of the system he buys, the cost for its development must be added to the price of his computer. This cost will be much higher than if the manufacturer distributed the software charge over many computers. In other words, well-conceived system software that is needed for an individual application is much cheaper for the user to buy from the manufacturer than to develop, and the selection criteria should reflect this view.

The user must determine the software selection criteria. Because software needs are tied to an application area as closely as hardware needs, criteria can vary from application to application. Despite the previous disclaimers, certain general software characteristics should be included in the software criteria.

Generally, the cost per line of software developed is inversely proportional to the investment in hardware. In other words, the less expensive the hardware, the more expensive it is to program. It is uneconomical, for example, for the programmer to do clerical chores such as loading a succession of paper tapes or stepping through a compiler process. If the system does not support program development, then an alternative must be identified and its cost.

System software universally includes an editor and an assembler. A variety of conventional and special-purpose compilers are available — not all from the same vendor.

Manufacturers emphasize the following features of their assemblers and compilers:

- Number of passes of the source code.
- Memory required.
- Quality of syntax checking.
- Pseudo-operation codes.
- Absolute or relocatable output code.
- User-defined macros in the Assembly language.
- Library calls and in-line Assembly code provided.

The selection committee must consider the ease and speed with which applications programs can be coded, debugged, and run on the system. An initial decision is what language should serve as a basis for development. The fundamental considerations are as follows:

- Compiler languages are superior because programs can be developed faster, documentation is better, and larger pools of trained programmers are available.
- Assembler languages produce more efficient code.
- Some languages will not be available on otherwise superior equipment.
- Compilers require operating systems for support. Larger, more elegant languages often are not acceptable in the user environment until many months after their first release (caveat emptor).

Most assemblers require a minimum of two passes of the source code to produce an assembled program, and a so-called one-pass assembler either leaves many references to be resolved by a loader or is a two-pass assembler, which does not require the source code to be read from an input device twice. The first pass checks the source code for syntactic errors and builds the symbol table in memory. The second pass completes the assembly and tags unresolved references for the loader. The language compiler adds one translation pass at the front end of this process.

Utility routines should be supplied for arithmetic and data conversion and for source code debugging. I/O handlers should be provided. Loaders should be furnished for all software supplied with the system and all applications programs.

System software should include diagnostic routines for system maintenance. Tests should be provided to check the operation of every unit in the system and to diagnose malfunctions within those units supplied as spare parts. Many manufacturers provide software on a modular basis. Each module requires a specific minimum hardware configuration, number of memory locations, optional features, interrupt lines, mass storage, and peripheral devices.

Operating systems for minicomputers are becoming increasingly important, particularly for systems that include mass storage devices. Most operating systems are of the foreground/background type; one or more real-time programs can be executed in the foreground and one batch program can be executed in the background. Batch background programs are sometimes priority-oriented. Time-sharing operating systems for minicomputers are also available from major minicomputer manufacturers and some independent vendors.[10]

Foreground/background operating systems make minicomputers suitable for real-time control applications, and increase the efficiency of the overall computing system. Real-time programs are incorporated into the operating system and are executed in the foreground, while batch programs can be executed during leftover processor time in the background. The important feature of these systems for control applications is that new real-time programs can be debugged and prepared for incorporation in the operating system without closing down the system.

Time-sharing operating systems are a variation of the foreground/background operating systems. Instead of real-time control programs being executed in the foreground, all time-sharing users are in the foreground.

Operating systems vary in complexity, depending on the kinds of applications for which they were designed. Most manufacturers who include operating systems in their software packages offer modular systems with more features available as the hardware configuration increases in size. Operating systems handle the following functions:

- Communication between the operator and the system.
- I/O.
- Servicing of the interrupt system.
- File definition and manipulation.
- Processor status.
- Initiation of program execution.
- Core assignment.

User programs have access to the preceeding facilities only through the operating system to ensure against inadvertent destruction of the programs in core.

System generation permits tailoring the operating system to a particular hardware configuration. Only those modules required by the application are incorporated into the operating system for that application. For example, if the hardware configuration includes no magnetic tape units, no magnetic tape handler programs are loaded. System generation occurs only once for an installation unless new equipment is added.

Organization of the operating system depends on the type of system. Foreground/background real-time systems execute programs on a priority basis; the priority of each program application is assigned on the basis of the required response time. The execution time of real-time programs is usually short, and any long calculations are performed by background programs. Background programs can be executed in the order received by the operating system, or programs can be executed in accordance with an assigned priority that can be changed by the operator via the console or control cards.

Time-sharing systems can assume all users have equal priority and allocate a time slice to each one. Alternatively, the time-sharing system can assume that some users have higher priority than others; and the programs of high-priority users are permitted to run to completion.

Communication between the operator and the system can be via a Teletype keyboard/printer, card or tape reader and punch, and/or line printer. The operating

system includes an interpreter routine that decodes messages from and generates messages to the operator. The communications codes provided limit an operator's control over the system.

Operating systems handle all I/O for the system; users specify their I/O via logical unit numbers. The operating system maintains queues for the use of I/O devices and overlaps I/O operations with processing.

The manufacturer designing the operating system makes various assumptions on which to base the system. These assumptions or system parameters are based on the hardware and the application for which the hardware will be used; they include such factors as the average core storage required by a foreground or background problem, the maximum number of foreground problems, the maximum number of priority levels allowed, the type of programs that can be run in the foreground and background, and the system software a user can utilize. Thus, a particular operating system can be too big and complex, too small and simpleminded, or about right for a particular application, depending on the parameters used in the system design. The selection criteria must spell out the minimum facilities required of the operating system.

The structures of various files are based on the anticipated needs of the applications for which the system was designed. The means for addressing, changing, and adding to files should be examined in the light of the file use for an application.

The operating system allocates memory for all programs executed. Normally, the memory map includes three main areas; one area is assigned to the resident portion of the operating system, another area is assigned to the resident applications programs, and the third area is assigned for temporary use by all other executing programs — whether system or user. The amount of memory devoted to resident applications programs and to temporary programs determines the size of programs that can be run. If the temporary storage area is too small for applications programs or for the required systems programs, then more memory must be added.

Manufacturers also emphasize the system software packages that can run under the operating system, the ease of inserting programs into the batch stream, the protection safeguards for users files, and the facilities for segmenting large programs into a size that can be handled by the system.

In general, when considering operating systems, the judgement criteria are not very different from those used in evaluating operating systems of larger computers. Usually, the small computer system must respond to new requirements, however. Some insight into operating system organization or methods for making additions — specifically in the I/O area — is desirable.

Qualifications of the Manufacturer

The characteristics attributed to the manufacturer supplying the system are important in selecting a system because users require many services from this manufacturer. Consideration should also be given to the following factors:

- Reputation of the sales personnel.
- Delivery schedules and reputation for meeting them.
- Maintenance, distance of computer site from manufacturer or service center, and quality of the field engineering staff.
- Software support available for applications programming.
- Number of systems delivered.
- Quality of documentation on hardware and software.
- Training provided.
- General reputation of the hardware and software.
- Financial health of the vendor.

Settling on a System

At this point, the selection criteria should include only those features that are relevant to the application. Some criteria are critical; these must be identified, and all computers without the critical features should be ignored. From the selection criteria, the selection committee should make up a hardware list and, using AUERBACH reports or other computer surveys, select a group of manufacturers that can do the job.

The committee can calculate hardware costs from price lists or seek bids from the manufacturers of acceptable computers. Seeking bids is preferable if special equipment, special services, or a competitive bid is required.

The first step is to solicit the "long list," which describes the functional requirements and requests a response of qualification and interest in bidding. From this information the "short list" of three to six vendors will do; these are asked for a formal proposal.

Using the performance criteria described previously, the next step is to calculate the system performance for all acceptable computers:

$$P_c = \sum_{i=1}^{N} W_i \, S_i$$

where P = system performance
c = a particular computer system
i = a selection criterion for an application
N = the total number of selection criteria for that application
W = criterion weight
S = implementation scale factor. [11]

A unique performance number (P) can now be associated with each acceptable computer system.

When the proposals for the computer hardware are received, the selection committee can compute a total system price. This price includes the manufacturer's system price plus the estimated in-house costs for programming, hardware, and operations. Once the total system costs for all proposed systems are obtained, the price/performance ratios are calculated for each by dividing total system cost by the performance number.

Logically, using this method, the selection committee selects the computer with the lowest price/performance ratio (PPR). Other factors, however, can dictate selecting some other system. The total system cost in relationship to the computer budget, for example, might force the selection of a lower-priced computer with a higher price/performance ratio. If two computers are roughly equivalent, the committee might select one over the other because of delivery schedules. Having performed the analysis described in the preceding paragraphs, the selection committee can make decisions on a sound analytical basis, and that is the main advantage of this approach.

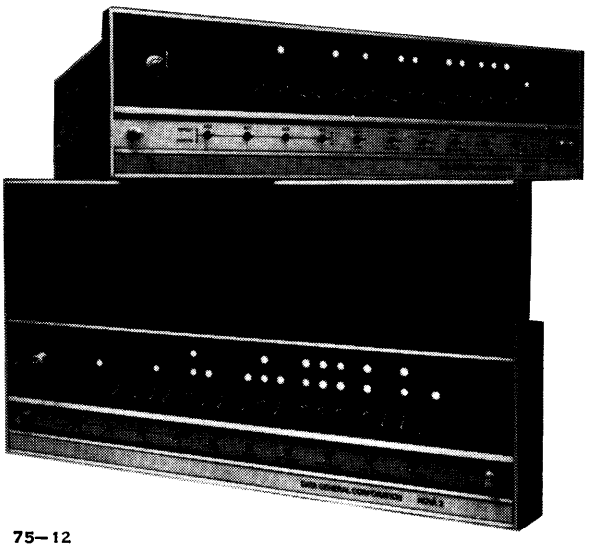

Figure K. Data General Nova 2/4 and 2/10

FUTURE DEVELOPMENTS

The rise of minicomputer technology has been explosive. The diversification of equipment and applications has been dramatic since 1968. Viewed from the standpoint of the problem to be solved, the history of computing technology can be described as follows:

Pre-history	Mechanical computing; abacus to Hollerith.
50's	Widespread computation, but unreliable and expensive.
60's	Centralized large computers with languages and operating systems: problems forced to conform to batch processing regimes.
70's	Decentralized task-oriented processing, using language and processors scaled to the task.
Beyond	Further melding of hardware and software techniques, with highly individual designs extending into the CPU itself.

It is a fact that minicomputer manufacturers are selling larger average systems. One minicomputer manufacturer spokesman notes that the average system now shipped is valued at $37,000. Four years ago it was only $14,000. More system software and more peripherals are available. The basic small computer is still very much the big seller; but it has larger cousins now. The genealogy can be observed by looking at Data General as an example of the industry trend maker: first the Nova, then the Supernova; the line was subsequently filled out with Nova 800 and Nova 1200, then the "hairy" (big) 840; all software compatible; followed by the tiny Nova 2/4 and 2/10; now the much grander ECLIPSE. Another example is Varian: first came the simple 620A, then the fast 620F, next the economical L100, and finally the V70 Series; all software upward compatible.

The glamour and promotion are concentrated on the maxi-mini and the new compilers, but this rising scale of grandeur is deceptive. At the other end of the spectrum, history is repeating itself. As the mini has challenged large computer designers, now the microprocessor challenges the established minicomputers. The burgeoning activity centers on a new set of suppliers — the computer-on-a-chip vendors who are producing scaled-down minicomputers. The decade ahead should see far greater emphasis on system engineering, task-oriented design than was ever true for minicomputer design. The fortunate user can now choose from an almost complete spectrum of solutions for a problem and truly find just the right amount of hardware and software to do the job.

Figure L. Data General ECLIPSE® Computer

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General Automation LSI 12/16 Processor Clip

INTRODUCTION

Change in the computer industry has always occurred at a high rate. Since the introduction of computers for commercial use, generation has followed generation in rapid succession. A change in basic circuit technology — always tending toward smaller size, higher speed, more reliability, and, especially, lower cost—produces changes in software architecture, data handling and storage methods, and even types of peripherals used, because the ultimate goal is to reduce the cost of the total system.

Changing the cost of one large system component alters the cost relationships among the other system components, leading to new types of system architecture. If memory is more expensive than labor, then programmers spend long hours devising ingenious algorithms to save the memory required by a program. If memory is cheap relative to manpower costs, then high-level languages are used to save programmers time at the expense of efficient utilization of memory. If memory becomes very, very cheap — who needs discs? Exit virtual storage.

Thus, a change in circuit technology quickly snowballs into a series of other changes and a new generation is born. The advent of large-scale integrated circuitry using semiconductor technology was the beginning of such a change. The miniature, high-density semiconductor "chips" of various kinds lent themselves to mass production; and they attacked existing computer technology on two fronts. On one hand, they could replace the magnetic cores used for working memory; on the other hand, they could replace the small and medium-scale integrated circuitry used in the CPU itself.

Success on both fronts is linked to three factors. First, larger and larger numbers of bits can be packed on a single chip, which increases total reliability (fewer interconnections to malfunction), reduces power consumption, and reduces total size. Second, mass production methods have been developed for high volume and low cost without sacrificing reliability. Third, the product has been marketed successfully.

Core memories were first impacted by semiconductor technologies; it is clear that the changeover from core to semiconductor memory is now well under way. The change-over in CPU circuitry is just beginning, slower in coming because CPU circuitry is complex and engineering the CPU functions onto semiconductor chips at their existing densities is difficult. As a result, the first semiconductor CPU chips, called microprocessors, were "simplified" in a number of ways that did not prevent them from becoming cost-effective in certain types of applications, with their most notable success as the basic component of calculators.

As technological and engineering problems were solved, a second generation of faster, denser CPU chips was born. These chips are called microcomputers because they can compete at the low end of the minicomputer market when memory, I/O circuitry, and programs are added. The ability to produce CPU chips equal in power to the fastest minicomputers and general-purpose computers is a matter of increasing speed and bit density to specifications, and that may well be within the range of these new semiconductor technologies. The semiconductor CPU's "third generation" (macro microcomputer?) is probably already on someone's drawing boards.

Meanwhile, what will the impact of these new microprocessors and microcomputers be on today's minicomputer markets? To answer this question, the successes and failures of microprocessors and the resulting developments in microcomputers must be examined. To understand some of the microprocessor's early problems, however, requires a brief examination of the semiconductor technologies currently used for microprocessor and microcomputer production.

SEMICONDUCTOR TECHNOLOGY

All existing semiconductor technologies base their circuitry on combinations of "solid solutions." The prevailing MOS (metal oxide semiconductor) technology uses silicon (valence of 4) as the "solvent" and another element with a valence of 3 (such as boron) or 5 (such as phosphorus) as the "solute" to yield semiconductor wafers with regular areas of either positive or negative charge, respectively. Typically, a thin insulating layer of silicon dioxide is grown over the substrate wafer, channels are etched through the insulation, and these channels are doped with the oppositely charged "solute"; i.e., phosphorus is used to create n-channels in a positively charged boron-silicon wafer or, conversely, boron is used to create p-channels in a negatively charged phosphorus-silicon wafer.

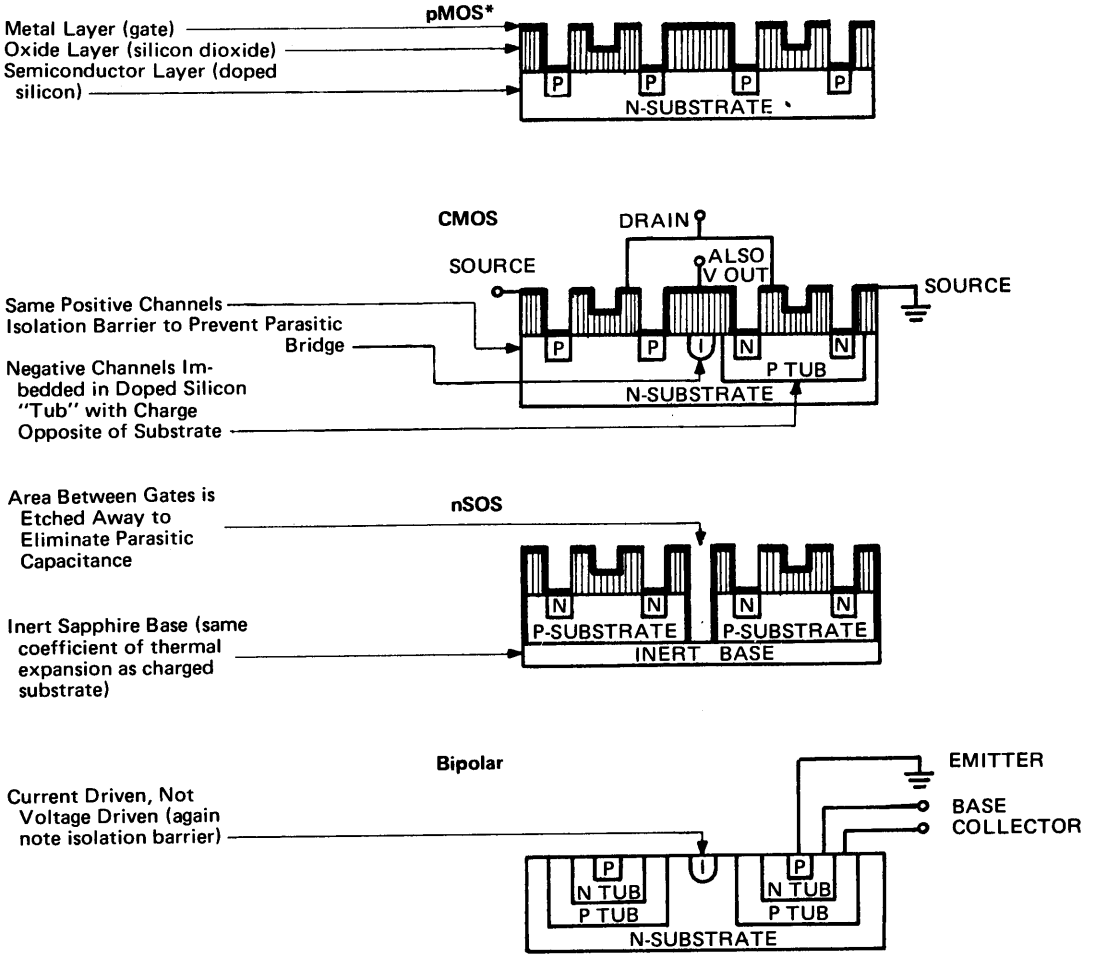
After several steps to build up the insulation layers and gates, while leaving the charged channels exposed, a metal is deposited over the entire surface. Gates and contacts are etched away; the surface is glassed in; and windows are

etched for external connections. The result is an n-channel or p-channel MOS chip, abbreviated nMOS and pMOS, respectively. (See Figure 1.)

Both pMOS and nMOS gate settling times are slowed by the parasitic capacitance presented by the thin insulating oxide layer sandwiched between two conducting layers. Some manufacturers have reduced this problem by developing CMOS (complementary MOS) wafers; Intersil and RCA, for example, are working on CMOS. Sets of p-channels are alternated with n-channels etched into an extra large p-channel called a "tub." This requires extra fabrication steps to make the p-tub and the n-channels within the p-tub; in addition, extra steps are usually required to create isolation barriers to prevent accidental "parasitic bridges" between the p-channels and the p-tubs. Again, see Figure 1 for an illustration.

Another method to make nMOS and pMOS faster is used by General Automation in conjunction with Rockwell, in their nSOS (sapphire on silicon) technology. In this technology, the whole MOS sandwich is superimposed on an inert sapphire substrate, and all surplus base material is etched away to cut down on parasitic incapacitance. The result is faster than CMOS. The manufacturers point out that nSOS is the low end of this technology, and that CSOS could achieve even higher performance. SOS could also be combined with bipolar circuitrv.

Bipolar devices are faster than even CMOS and SOS devices. Each bipolar channel can be conceptualized as a channel in two nested tubs (again separated from other channels by isolation barriers) as shown in Figure 1. This creates a current-driven not a voltage-driven device, however; and it dissipates more power because an input current must be continually applied to the metal gate to maintain its "on" state. Bipolar circuits, moreover, require many more fabrication steps; consequently, they are more expensive. Typically nMOS and pMOS circuits require five masking steps and one diffusion step; bipolar circuit fabrication requires 12 masking steps and four diffusion



**nMOS is not shown, because it has the same basic pattern as pMOS except the substrate is positive and the channel is negative. Silicon gates also not shown (these achieve higher speeds on both pMOS and nMOS).*

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Figure 1. Microprocessors and Microcomputers: Semiconductor Transistors

steps; CMOS and SOS circuits are intermediate, they require two or three more steps than nMOS.

MICROPROCESSOR ARCHITECTURE

As might be expected, the earliest successful microprocessors used pMOS and nMOS technologies, with their less elaborate fabrication processes. The first CPUs had to be cut down to their barest essentials in order to fit on a small number of MOS chips.

The first manufacturer to mass produce and market MOS microprocessors successfully was Intel, a company formed in 1968 by former employees of Fairchild Semiconductor. Before introducing the 4004 microprocessor, Intel had earned a name for itself with its semiconductor memories, capturing a dominant share of the market in competition with such memory makers as Texas Instruments, Fairchild, National Semiconductor, and Mostek.

The 4004 is a 4-bit machine; the data bus and data handling registers are four bits wide, but the instruction register is eight bits wide, the address register 12 bits wide. Like most full-blown minicomputers, the 4004 has an arithmetic logic unit (ALU) and a program counter, in addition to its address and instruction registers. It also has 16 index registers, which can be addressed individually or in pairs.

Addresses, data, and instructions are all transferred over the 4-bit wide bidirectional bus. This means that the three segments of the address and the two segments of the instruction must be transferred using five machine cycles before the instruction can be decoded and executed. Because the CPU chip has only 16 pins for transfer of data, addresses, and control bits to and from memory, ROM and RAM memories are masked to "recognize" the proper location in the broadcasted addresses and to respond with an input or output operation. ROM modules contain words of memory, while RAM contains 320 4-bit words; up to a total of 4K words of ROM and RAM can be added to a system. A 4004 CPU can control 64 to 128 I/O devices.

Price and size have dictated the 4004's spare CPU architecture, with its 4-bit wide multifunction bus, small number of pins, limited instruction set, few registers, and so on. Consequently, programming a 4004 (in machine or assembly language) involves a number of maneuvers required by the limitations of the machine. A simple 4-instruction minicomputer program (Load, Add, Store, Stop) for adding two numbers takes 20 instructions with the 4004, because a 5-instruction routine is needed to assemble the address and the instruction for the operation performed by the sixth instruction. Then, because the 4004 has no Halt instruction, a conditional jump dependent on the state of the external test line is used to stop the program.

The 4-bit Intel chip sets are extremely low in cost; and, in spite of limited capabilities in comparison with minicomputers, they have found a wide variety of applications in addition to their original calculator market. The 4-bit word is ideal for decimal-number handling, so the 4004 is useful for cash registers, weighing machines, credit and point-of-sale terminals, and simple billing and accounting machines, particularly when these devices are interactive with (slow) human beings. Besides these applications, a large number of machine control applications are amenable to 4-bit microprocessor control. In the automotive industry, for example, applications include control of engine parameters, instrument displays, automatic locks, alarms, safety procedures, and burglar alarms, to name only a few. Intel says the 4004 can be a cost-effective replacement for any board with 30 to 100 packages of TTL logic.

Intel's major competitor for the large, general-purpose, 4-bit microprocessor market is Rockwell International with its PPS-4. Fairchild's PPS-25 is also competitive, particularly for the calculator market. These two systems have architectures that differ from each other and from Intel; but, like the Intel machine, they are extremely low-cost systems and very small. Consequently, they require clever programming to get around architectural idiosyncrasies.

The Rockwell PPS-4 has a slower clock time than the Intel MCS-4, but it is faster. PPS-4 uses Rockwell's proprietary 42-pin package, so it can implement separate 12-bit address and 8-bit data buses, making memory references easy and fast. Also, it allows fetch and execute portions of instructions to overlap. The CPU, including six registers and two control flip-flops, is contained on one chip; a minimum system consists of a CPU chip plus a memory chip. The CPU chip can handle 16 I/O chips, 30 memory chips, or a total of 30 mixed memory and I/O chips. Although the PPS-4 is faster and more flexible than the 4004 for handling BCD arithmetic, the Intel machine can handle more I/O, giving it a competitive edge in control-type applications.

The Fairchild PPS-25 is less suited than the Rockwell and Intel machines for general-purpose applications; but it is well suited for calculator functions, as well as for similar devices requiring numeric calculations, such as navigation instruments. The standard RAM module is organized as three 25-digit registers, allowing numbers up to 25 digits long to be processed serially by the CPU using a 4-bit data bus like Intel's. Although the 62.5-microsecond cycle seems slow, it is broken up into 25 time slots (versus eight for Intel and eight for Rockwell), allowing an instruction, for instance, to send to memory for another instruction and to receive it back. Registers can also be masked so that part of a register can be operated on by an instruction. The PPS-25 can attach up to 6,656 bytes of memory.

It is clear that the processing, memory, and I/O limitations of these three devices present no threat to the established minicomputer market. Instead, they are finding an enormous market as replacements for hardwired logic,

simultaneously achieving lower costs and greater flexibility. Costs depend on quantity, of course, but prices average less than $50 for chip sets.

The biggest problem faced by the new user in evaluating the suitability of microprocessors for an application is estimating the cost of programming them. Although all three devices have cross assemblers, assemblers, instruction simulators, and prototype board software support available, the programming is still somewhat intricate, especially for engineers unused to programming. The resounding success of all three devices, however, points to the fact that while programming is a stumbling block, it does not prevent microprocessor-based devices from being highly cost effective.

The second big cost involved with microprocessors is that of adding I/O logic, timing and control circuitry, memory modules, and I/O drivers to the microprocessor; assembling them into a system; and interfacing them to the product. Intel and Rockwell sell board-level systems, with CPU and related components assembled into a circuit board(s) that has simpler interfacing problems, similar to those encountered with stripped down minicomputers. These standardized boards are easier to use but are more expensive. A full-blown, tabletop, minicomputer-type device costs under $2,000 in most cases; but a minimum chip set usually is less than $50. In moderate quantities, the Intel 4004 costs around $15.

The cost of external circuitry and design work in building a system is enough to allow several manufacturers to buy Intel microprocessors OEM and assemble their own systems. Prolog, for instance, sells systems aimed at design engineers. The new 2 x 2-inch Teledyne TDY-52A is an Intel-based system, as is the DEC MPS Series. The tiny Intel-based TDY-52A sells for approximately $1,500 with 4K words of memory, while the DEC MPS sells for around $476 (with 1K memory).

It has been estimated that the huge market for the extremely low-cost, 4-bit processors has hardly been tapped. It is interesting, therefore, that new companies don't want to compete for the low end of the market. One reason for this lack of activity may be the relationship between R&D cost outlays and the long recovery time. The R&D costs are very large; the time gap between anticipated and actual delivery has frequently been large. More than one industry observer has noted that the most important specification for a microprocessor is its availability.

The larger, more expensive 8-bit and 16-bit microprocessors, which can overlap the lower end of the minicomputer market in many cases, have an average of 8 to 10 memory modules (256 words each) associated with each CPU, whereas 4-bit system applications usually require very little memory. A number of Intel users feel that the 4004 (MCP-4) is impractical when more than four RAM chips are needed. The upshot is that it is much easier for a semiconductor manufacturer to recover the R&D costs for a larger processor of eight or more bits because it increases sales of existing memory products which do not have to be redesigned.

From Microprocessor to Microcomputer — The First Generation

It was not until the first rumblings of the 8-bit microprocessors were heard that minicomputer manufacturers started to worry about the threat of microprocessors to existing minicomputer markets. A glance at the specifications for the slow first-generation 8-bit pMOS systems was temporarily reassuring; but R&D developments toward faster systems and the increasing miniaturization with greater CPU power told the more farsighted mini manufacturers that the days for small- and medium-scale integrated circuits were numbered. General Automation, for instance, began serious design efforts to produce a microprocessor-based mini.

The first 8-bit pMOS processors were not really microcomputers although they packed the CPU on a single chip and managed standard bytes of data; the slow speed and architectural limitations imposed by the scarcity of chip "real estate" kept performance down. Intel 8008 CPU (MCS-8 system), for example, added only three instructions to the 4004 instruction set (one of these is Halt, reducing the addition program discussed earlier to 19 steps on the 8008), added two pins to the chip, and reduced the number of registers to eight. Cycle time was reduced to 7.5 microseconds; DMA and interrupt capability were added; but the maximum number of I/O devices that could be handled was reduced to 24. Memory capacity was increased to 16K words, as opposed to 4K on the 4-bit system. The composite data/instruction/address bus architecture is retained, and each chip requires about 20 external TTL packages to implement. Performance is improved, however, because the bus is eight bits wide, and only five steps are required per machine cycle.

Another first-generation 8-bit pMOS CPU, called IMP-8 is marketed by National Semiconductor. Actually the IMP-8 is created from two 4-bit, 40-pin chips, operating in parallel with a microprogrammed control ROM (CROM). National semiconductor also markets a 16-bit system (4-bit chips operating in parallel); actually the 4-bit chips are all 4-bit CPU slices, so a user could configure a 32-bit word computer if he liked. The chip sets require a number of SSI (small-scale integration) and MSI (medium-scale integration) circuits to implement, thus the price is pushed up along with the word size. The IMP-8 has a 16-bit address scheme and can address up to 64K words of memory or devices, or both.

Although Intel's 8008 has many constraints, its low price and availability have made it a highly successful system. The market for 8-bit systems includes all types of communications gear (which deals mostly in 8-bit EBCDIC and ASCII characters), the new word processor

market, and many types of control systems. Intel's strategy has been to hold down the processor price by sticking to an 18-pin chip, small enough for good processing yields.

Both National Semiconductor and Intel supply their systems at the board level as well as at the chip-set component level. A user can buy the chips and do all the control and interfacing logic himself, or he can buy a microcomputer-on-a-board, with many of the control and interfacing chores already done. If he wants card reader input, though, he may have to design the card reader interface because microcomputer boards still fall somewhat short of minicomputer boards as far as ease of use is concerned.

Software support has increased to include a PL/M compiler for a high-level language similar to PL/1.

An interesting system, using four of National Semiconductor's 4-bit CPU slices to create a 16-bit processor, has been developed by Teledyne of California. Instead of using TTL, SSI, and MSI circuitry for external logic, I/O interfacing, and so on, Teledyne uses LSI throughout on 41 chips. It is housed in a tiny 2 x 2-inch, 120-pin package. A separate 2 x 2-inch package houses 8K words of memory. Teledyne also produces an 8-bit system based on an Intel processor; it packs the CPU, all logic, and 4K bytes of memory (50 chips total) in one 2 x 2-inch package. Teledyne has begun deliveries; the first applications take advantage of the extremely small size and have been for noncommercial aviation and navigation fields.

The Second Generation — Microcomputers Arrive

Although the delivered first-generation systems proved successful, most manufacturers concentrated on technologies other than pMOS for microprocessors with performance closer to minicomputer speeds, without sacrificing much size. The nMOS technology, in spite of its similarity to pMOS, doubles the speed of pMOS; the carriers of the charge are the extra electrons in the silicon lattice (resulting in negative charge) rather than the positive lattice "holes" (missing electrons). Electron carrying speeds are twice as fast, while threshold voltages are lower. The n-channels also require less space, so output buffers can be smaller, allowing more buffers and more I/O devices per chip. Manufacturers also learned how to make registers more compact, so more of them can be fitted on one chip.

One of the biggest problems in chip real estate is the bus structure, which needs to be twice the data word width to be efficient. Each interconnecting wire for the bus channel is around 1 mil wide, for a total of 16 mils on an 8-bit system. Manufacturers contemplating 16-bit processors are faced with a 32-mil wide bus, which takes quite a chunk out of a 200-mil wide chip. Using doped silicon for interconnections in the silicon-on-sapphire process allows narrower bus channels, but bus size is still one of the big problems for manufacturers trying to fit powerful 16-bit systems on a single chip.

The recent rash of second-generation microcomputer announcements signifies the state of the art in semiconductor technology. Three basic technologies obtain performance benefits over pMOS systems: nMOS (Intel, General Instruments, Signetics), SOS (General Automation, Rockwell), and CMOS (RCA, Intersil). Only two of these new systems, the Intel 8080 and the General Automation LSI 12/16, have been delivered, however. New microprocessors take about two years to develop, and they are prone to unexpected design problems requiring several chip prototypes.

The successful entry of General Automation into the market is significant in a number of ways. It marks the first line of defense against the impending encroachment of microprocessor manufacturers on minicomputer markets — if you can't beat 'em, join 'em. The fact that DEC has rapidly designed the MPS Series microcomputers, using the Intel 8008 in order to get large volumes of the product on the market quickly, underscores the threat to minicomputers. The 8080, although delivered, is not yet in high-volume production.

Industry observers note that about 10% of installed minicomputers are underutilized. It is these types of installations, using stripped down minis like Computer Automation's erstwhile Naked Mini or older systems like the PDP-8, which will be captured by the microcomputers first. Minicomputer manufacturers that produce microcomputers compatible with minicomputer lines, such as Computer Automation and General Automation have done, will remain competitive because of the body of software to which the systems fall heir. Undoubtedly, minicomputer manufacturers competing at the low end of the market will either have to develop their own microprocessors or OEM them from a semiconductor manufacturer in order to remain competitive.

Intel has taken advantage of existing 8008 software in the development of the 8080. The 8080 instruction set is a superset of the 8008 (78 instructions as opposed to 46). Users adapting 8008 programs to the second-generation processor have had some problems, but often they find the increased power of the new microcomputer well worth the reprogramming efforts.

The 40-pin 8080 is more like a normal mini; it has a 16-bit address structure, 64K-word memory capacity, and 10 registers; and it can address up to 256 I/O devices. The processor cycle time is 8.2 microseconds, faster than that of the 8008 but not up to current minicomputer speeds. Nevertheless, the flexibility and power of the microprocessor as a whole has led many manufacturers of terminals, word processors, and the like to feel they can make microcomputer-based systems competitive with minicomputers; processing speeds do not have to be high for these applications.

Most manufacturers working on second-generation microcomputer systems are, predictably, semiconductor manufacturers, such as General Instruments, Motorola, Signetics, AMI, Intersil, and RCA. Some manufacturers, Texas Instruments, for example, make both semiconductors and minicomputers; they are logical candidates to make microprocessors. Burroughs has used microprocessors to control its own peripheral devices for years. Honeywell uses its own "Big Blue" internally. Anxious minicomputer manufacturers, perhaps already into the calculator as well as the minicomputer market, are experimenting with semiconductor technology.

The lead time from introduction to first deliveries to high-volume production of a new processor is at least as long as for any new class of computers. In view of the number of manufacturers experiencing difficulties with the new technologies, however, the marketing move by DEC, choosing a design based on a first-generation processor in high-volume production, seems like good strategy. DEC delivered the first MPS in the second quarter 1974, high-volume production should follow shortly thereafter. As a result it will have a sizable installed base by the time a large number of second-generation microcomputers are available—which DEC estimates to be at least two years hence. DEC also plans to utilize the 8080 in its line as well, when production volumes are high enough.

The Third Generation

The basic trends in microcomputer technology are clear — greater miniaturization and higher speeds in order to place the maximum amount of processing power on a single chip. Semiconductor technology is still young, but the solution to many space and speed problems already seems within reach of those experimenting with SOS. It appears that future generations of microcomputers will replace the CPU not only of minicomputers but also, eventually, of the larger general-purpose systems. Conceivably, even some of the CPU memory, control, and I/O logic now external to the microprocessor chip will be fitted on it, shrinking the computer-on-a-board as well as the full-blown enclosed computer system. Meanwhile, the smaller, slower, cheaper processor chips will be used as components for new applications not yet thought of. Given DEC's estimate of two years before second-generation chips begin to impact the minicomputer business seriously, it is reasonable to assume that the third-generation revolution will be under way by 1980.

THE CURRENT MARKET

What the current market has to offer in the way of microprocessors is summarized in the chart at the end of this report. The 4-bit, 8-bit, and 16-bit systems have all been covered together because their basic parameters are similar. As many as possible of the processors currently under development were included with those already delivered, although specifications in this field are particularly subject to change.

The earlier 4-bit systems are generally sold as chip sets with varying amounts of accompanying logic modules and supporting software. The 8-bit systems are sold as chip sets, as well as at the board level and in the fully enclosed versions familiar to minicomputer users.

Parameters relating to the engineering of basic chip sets into finished products are probably of more interest to logic designers and engineers than computer users; thus, information regarding chip engineering has been provided with an eye to indicating the level of sophistication in the CPU, while configuration guidelines refer to the systems at board and enclosure levels, the levels of most interest to the current minicomputer market.

INTERPRETING THE CHART

Engineering. Most chip manufacturers sell microprocessors as chips (or chip sets); board-level systems or fully enclosed systems may or may not be offered. An OEM manufacturer, using chips fabricated by another manufacturer, concentrates on the higher-level systems and often provides much better software support. Microprogramming, which takes advantage of the higher memory speeds relative to the CPU, is a growing trend in second-generation systems.

The width of the address bus and data bus can be indicative of system speeds; if a system has a 4-bit address bus and a 4K-word memory capacity (requiring at least 12 address bits), then addresses will have to be moved back and forth in segments, resulting in extra programming steps and lower speeds. The same thing holds true for the data bus. The number of chips refers to a basic functional system (including memory) as defined by the manufacturer. The number of chips and the number of pins per chip give a rough indication of I/O capability and the generation of the chip set; large numbers are generally preferable.

Processor and Memory. The parameters pointing to processor power and flexibility are similar to those for minicomputers, but microprocessor parameters are probably even more misleading. Some systems have multiple registers to get around basic architectural limitations. Others implement unlimited nesting of subroutines through software, so the processors may or may not have a stack. Double-precision operation and indirect addressing entries refer to the ability to perform the appropriate operation with a single basic instruction, not to the number of steps the CPU must perform to implement the operation.

Input/Output. The Maximum Devices entry refers to the highest number of discrete peripherals (such as card readers and printers) that the system could conceivably run.

Configuration. Some manufacturers have used microprocessors to create a computer-on-a-board; a single compact unit is beneficial for certain OEM

applications where space is a limitation. Other manufacturers provide several "cards," which can be quite small (3 x 5 inches). Many microprocessor manufacturers are starting to offer a standard Teletype-interface chip. Peripheral Offerings entry refers to interfaces and/or the actual peripherals the manufacturer provides other than the Teletype interface.

Software. Supporting software is a vital element of all computers, be they macro, mini, or micro. Many of the problems experienced by early microprocessor users resulted from the lack of a standing body of proven software, one of the cornerstones of most minicomputer manufacturers' reputations.

Delivery Status. As mentioned several times previously, availability is extremely important. Chart entries refer to first customer deliveries, not to the achievement of high-volume production, which usually lags by at least half a year.

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	AMI CK 114	AMI 7300	Computer Automation LSI Series	Control Logic L Series
ENGINEERING				
Chip Fabricator	AMI	AMI	NA	Control Logic
Chip Word Size (bits)	8	8	–	8
Microprogrammed	Yes	Yes	Yes	Yes
Technology Used	pMOS	pMOS	pMOS	CMOS
No. of Chips	7	2	7	3
Address Bus (bits)	8	16	16	–
Data Bus (bits)	4	8	16	8
Pins/Chip	16, 28, 40	40	–	–
PROCESSOR				
No. of Registers	17	49	8	–
Push/Pop Stacks	No	Yes	No	Yes
Nesting Levels	No	7	–	7
Instruction Length (bits)	12	8, 16	16	–
No. of Instructions	75	150	168	–
Double Precision	Yes	Yes	Yes	–
Decimal Arithmetic	Yes	No	No	No
Indirect Addressing	No	–	Yes	No
Cycle Time (μsec)	4	5/bit	1.6	–
MEMORY				
Types	ROM	ROM	RAM, ROM, PROM	PROM, RAM
Data Word (bits)	8 or any	8	16	8
Max Memory (bytes)	2K	64K	128K	16K
INPUT/OUTPUT				
Interrupts (no.)	No	4-level	Yes, 5-256	Yes
DMA	No	Yes	Yes	No
Max Devices	78/50	64K	248	–
CONFIGURATION				
Single Board (w x h, in.)	No	–	Yes, 8.5 x 14	No (3 cards)
Memory on CPU Board	No	–	4K	No
Enclosure	No	No	Yes	Yes
Peripheral Offerings	No	No	Yes	No
SOFTWARE				
Cross Assembler	Yes	Yes	Yes	No
Assembler	No	No	Yes	Yes
High-Level Languages	No	No	Yes	No
Text Editor	No	No	Yes	Yes
Operating System	No	No	Yes	No
DELIVERY STATUS	Delivered	–	4Q '74	–
COMMENTS	Serial processor, up to 17 digits/field	–	–	3 x 5" cards

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	DEC MPS	Fairchild PPS-25	General Automation LSI-12/16	General Automation LSI 16
ENGINEERING				
Chip Fabricator	Intel (8008)	Fairchild	Rockwell	Rockwell
Chip Word Size (bits)	8	4	–	–
Microprogrammed	Yes	Yes	Yes	Yes
Technology Used	pMOS	pMOS	nSOS	nSOS
No. of Chips	1	7	1	1
Address Bus (bits)	14	–	12	16
Data Bus (bits)	8	4	16	16
Pins/Chip	18	16, 18, 24, 40	–	–
PROCESSOR				
No. of Registers	7	7	7	16
Push/Pop Stacks	–	1	No	–
Nesting Levels	7	4	–	–
Instruction Length (bits)	–	12	8, 16	16
No. of Instructions	48	46-95	51	78-83
Double Precision	No	Yes	No	Yes
Decimal Arithmetic	No	Yes	No	No
Indirect Addressing	–	No	Yes	Yes
Cycle Time (μsec)	1.5	6.25(2.5/bit)	2.64	1.8
MEMORY				
Types	RAM, PROM	PROM	RAM, ROM, PROM	RAM, ROM, PROM
Data Word (bits)	8	25 digits	12	16
Max Memory (bytes)	16K	6,656	32K	32K
INPUT/OUTPUT				
Interrupts (no.)	Yes (9)	Yes	63	64
DMA	NO	No	Yes	Yes
Max Devices	–	–	63	64
CONFIGURATION				
Single Board (w x h, in.)	Yes	Yes	Yes, 7.75 x 11	Yes, 7.75 x 11
Memory on CPU Board	No	–	Yes, 2K	No
Enclosure	No	No	Yes	Yes
Peripheral Offerings	Yes (TTY & console)	No	Yes	Yes
SOFTWARE				
Cross Assembler	Yes (PDP 8)	Yes, 360/370	Yes (SPC-16)	Yes (SPC-16)
Assembler	Yes (PDP 8)	No	Yes	Yes
High-Level Languages	No	No	Yes	Yes
Text Editor	Yes	No	Yes	Yes
Operating System	No	No	Yes	Yes
DELIVERY STATUS	2Q '74	Delivered	–	–
COMMENTS	Includes full-duplex serial interface	25-digit registers	–	–

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	Intel MCS-4 (4004)	Intel MCS-8 (8008)	Intel 8080	Microdata Micro-one
ENGINEERING				
Chip Fabricator	Intel	Intel	Intel	NA
Chip Word Size (bits)	4	8	8	8
Microprogrammed	No	No	No	Yes
Technology Used	pMOS	pMOS	nMOS	MOS
No. of Chips	4	1	1	1
Address Bus (bits)	Use data bus	8	–	–
Data Bus (bits)	4	16	–	–
Pins/Chip	16	18	40	–
PROCESSOR				
No. of Registers	17	9	10	15
Push/Pop Stacks	4x12 bits	8x14 bits	–	–
Nesting Levels	3	7	7	–
Instruction Length (bits)	8	8	8	–
No. of Instructions	45	48	74	–
Double Precision	Yes	Yes	Yes	–
Decimal Arithmetic	No	No	No	–
Indirect Addressing	No	No	–	–
Cycle Time (μsec)	10.8	12.5 or 20	8.2	1.2
MEMORY				
Types	ROM, RAM	RAM, ROM, PROM	RAM, ROM, PROM	–
Data Word (bits)	4	8	8	–
Max Memory (bytes)	8K ROM, 180 RAM	16K	65K	–
INPUT/OUTPUT				
Interrupts (no.)	No	Yes	Yes	–
DMA	No	Yes	Yes	–
Max Devices	64-128	8-24	256	–
CONFIGURATION				
Single Board (w x h, in.)	Yes	–	–	Yes, 8.5x11
Memory on CPU Board	4K	–	–	–
Enclosure	No	No	No	Yes
Peripheral Offerings	No	No	No	Yes
SOFTWARE				
Cross Assembler	Yes	Yes	Yes	Yes
Assembler	Yes	Yes	Yes	Yes
High-Level Languages	No	Yes	Yes	Yes
Text Editor	Yes	Yes	Yes	Yes
Operating System	No	No	No	Yes
DELIVERY STATUS	–	Delivered	Delivered	–
COMMENTS	–	–	–	Microdata 800/1600 compatible

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	Micro International	Micro International	Motorola MC 6800	National Semiconductor IMP-8 Series
ENGINEERING				
Chip Fabricator	Micro	Micro	Motorola	National
Chip Word Size (bits)	8	8	8	4
Microprogrammed	No	No	No	No
Technology Used	pMOS	nMOS	nMOS	pMOS
No. of Chips	1	1	5	3
Address Bus (bits)	8	16	16	16
Data Bus (bits)	8	8	8	8
Pins/Chip	18	40	40, 24	40
PROCESSOR				
No. of Registers	9	10	9	9
Push/Pop Stacks	8x14 bits	–	Yes	16x8 bits
Nesting Levels	7	7	NA	NA
Instruction Length (bits)	8	8	8, 16	8 or 16
No. of Instructions	48	74	72	38
Double Precision	–	–	Yes	Yes
Decimal Arithmetic	–	–	Yes	No
Indirect Addressing	–	1	Yes	No
Cycle Time (μsec)	12.5 or 20	8.2	5	1.4
MEMORY				
Types	RAM, ROM, PROM	RAM, ROM, PROM	ROM, RAM	ROM, RAM, PROM
Data Word (bits)	8	8	8	8
Max Memory (bytes)	16K	64K	64K	64K
INPUT/OUTPUT				
Interrupts (no.)	Yes	Yes	Yes	Yes, 1-level
DMA	Yes	Yes	Yes	No
Max Devices	8-24	256	40	16
CONFIGURATION				
Single Board (w x h, in.)	–	–	No	Yes, 8.5x11
Memory on CPU Board	–	–	No	Yes
Enclosure	No	No	No	Yes
Peripheral Offerings	No	No	No	Yes
SOFTWARE				
Cross Assembler	Yes	Yes	Yes	Yes, 360/370
Assembler	Yes	Yes	Yes	Yes
High-Level Languages	Yes	No	No	Yes
Text Editor	No	Yes	Yes	Yes
Operating System	Yes	No	No	No
DELIVERY STATUS	Delivered	Delivered	4Q '74	Delivered
COMMENTS	Second source Intel 8008	Second source Intel 8080	Async communications interface chip	Composed of two 4-bit CPU "slices"

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	National Semiconductor IMP-16 Series	Prolog 400 Series	Prolog 800 Series	RCA COSMAC
ENGINEERING				
Chip Fabricator	National	Intel (4004)	Intel (8008)	RCA
Chip Word Size (bits)	4	4	8	8
Microprogrammed	Yes	No	No	No
Technology Used	pMOS	pMOS	pMOS	CMOS
No. of Chips	4	4	1	2
Address Bus (bits)	16	Use data bus	8	2
Data Bus (bits)	16	4	8	8
Pins/Chip	40	16	18	40,28
PROCESSOR				
No. of Registers	23	17	9	16
Push/Pop Stacks	16x16 bits	4x12 bits	8x14 bits	No
Nesting Levels	NA	3	7	Unlimited
Instruction Length (bits)	8,16,24	8	8	8
No. of Instructions	43-60	45	48	37
Double Precision	Yes	Yes	Yes	No
Decimal Arithmetic	No	No	No	No
Indirect Addressing	Yes	No	No	No
Cycle Time (μsec)	1.4	10.8	12.5 or 20	6
MEMORY				
Types	ROM, RAM, PROM	ROM, RAM	RAM, ROM, PROM	RAM, ROM, PROM
Data Word (bits)	16	4	8	8
Max Memory (bytes)	128K	8K ROM, 160 RAM	16K	64K
INPUT/OUTPUT				
Interrupts (no.)	Yes, 4-level	No	Yes	Yes
DMA	Yes	No	Yes	Yes
Max Devices	65K	64-128	8-24	256
CONFIGURATION				
Single Board (w x h, in.)	Yes, 8.5x11	No, several	No, several	No (3 cards)
Memory on CPU Board	Yes	No	No	No
Enclosure	Yes	No	No	Yes
Peripheral Offerings	Yes	No	No	No
SOFTWARE				
Cross Assembler	Yes, 360/370	No	No	Yes, 360/370
Assembler	Yes	No	No	Yes
High-Level Languages	Yes	No	No	No
Text Editor	Yes	No	No	Yes
Operating System	No	No	No	No
DELIVERY STATUS	Delivered	Delivered	Delivered	4Q '74
COMMENTS	Composed of four 4-bit CPU slices	For design engineers; system analyzer	For design engineers; system analyzer	Tymshare, Inc. software; 1-chip system due soon

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	Rockwell PPS-4	Signetics PIP	Teledyne TDY-52A	Teledyne TDY-52B
ENGINEERING				
Chip Fabricator	Rockwell	Signetics	Intel	National
Chip Word Size (bits)	4	8	8	16
Microprogrammed	Yes	No	Yes	Yes
Technology Used	pMOS	nMOS	MOS	MOS
No. of Chips	1	1	50	41
Address Bus (bits)	Use data bus	16	4	16
Data Bus (bits)	Dual 4-bit	8	8	16
Pins/Chip	42	40	120/Pkg	120/Pkg
PROCESSOR				
No. of Registers	6	4	8	4
Push/Pop Stacks	12x2 bits	8 deep	4x12 bits	16x16 bits
Nesting Levels	2	–	3	NA
Instruction Length (bits)	8, 16	8, 16	8	8, 16, 24
No. of Instructions	50	68	46	–
Double Precision	Yes	Yes	Yes	Yes
Decimal Arithmetic	–	No	No	No
Indirect Addressing	–	Yes	Yes	Yes
Cycle Time (μsec)	5/bit	5	10	1.4
MEMORY				
Types	ROM, RAM	–	ROM, RAM	ROM, RAM
Data Word (bits)	4	8	8	16
Max Memory (bytes)	16K ROM, 8K RAM	32K	32K	64K
INPUT/OUTPUT				
Interrupts (no.)	No	Yes	Yes	Yes
DMA	No	Yes	No	Yes
Max Devices	16	256	2	10
CONFIGURATION				
Single Board (w x h, in.)	Yes	No	2x2" pkg	2x2" pkg
Memory on CPU Board	–	No	4K words	No
Enclosure	Yes	No	–	–
Peripheral Offerings	No	No	No	No
SOFTWARE				
Cross Assembler	Yes	Yes	Yes; 360/370, PDP-8	Yes; 360/370, PDP-8
Assembler	Yes	No	Yes	Yes
High-Level Languages	No	No	No	No
Text Editor	No	No	Yes	Yes
Operating System	No	No	No	No
DELIVERY STATUS	Delivered	4Q '74	Delivered	Delivered
COMMENTS	Software by Tymshare Inc. Applied Computing Technology	–	2x2" pkg has entire CPU, control, I/O memory, etc.	2x2" pkg has control, I/O, logic; 2x2" memory pkg

CURRENT MICROPROCESSORS AND MICROCOMPUTERS

System	Texas Instruments 0117NC	Toshiba TLCS-12
ENGINEERING		
Chip Fabricator	TI	Toshiba
Chip Word Size (bits)	4	12
Microprogrammed	No	Yes
Technology Used	pMOS	pMOS
No. of Chips	1	1
Address Bus (bits)	–	Use data bus
Data Bus (bits)	–	12 bits
Pins/Chip	28	42
PROCESSOR		
No. of Registers	3	13
Push/Pop Stacks	No	NA
Nesting Levels	No	NA
Instruction Length (bits)	4, 8	12, 24
No. of Instructions	14	108
Double Precision	No	Yes
Decimal Arithmetic	No	Yes
Indirect Addressing	Yes	No
Cycle Time (μsec)	No	Yes
MEMORY	156	1.0
Types	PROM	ROM, RAM
Data Word (bits)	4	4, 8, 12
Max Memory (bytes)	NA	4K
INPUT/OUTPUT		
Interrupts (no.)	Yes, 1-level	8-level
DMA	No	Yes
Max Devices	3	NA
CONFIGURATION		
Single Board (w x h, in.)	No	Yes
Memory on CPU Board	No	NA
Enclosure	No	Yes
Peripheral Offerings	No	NA
SOFTWARE		
Cross Assembler	–	–
Assembler	–	–
High-Level Languages	–	–
Text Editor	–	–
Operating System	–	–
DELIVERY STATUS	Delivered	–
COMMENTS	–	–

PRODUCT CLASS REPORT
Process Control

OVERVIEW

Process control is the automatic handling of matter or energy, and its modification by chemical or physical means to yield the products or results desired at a profit. Process control computers are electronic digital computers functioning in a process control environment. (The term process control itself is somewhat redundant, inasmuch as process implies control; we therefore will speak of a control computer.)

Digital computers were first applied to the automatic control of industrial processes in 1958. Early applications included chemicals, steel, petroleum refining, paper, electric power, and cement. Current uses are in satellite control, missile launches, pipelines, intensive care hospital units, television networks, data acquisition-reduction systems, automatic testing, bridge and traffic control, food packaging, postal cancellation, and laboratory automation. In each instance, the introduction of the electronic digital computer began a trend away from older, more manual forms of control such as human resources, controllers, data loggers, and analog computers. As processes became more complex and instruments more numerous, human operators were inundated with information. Digital computers have had an enormous effect on such systems, primarily because they can handle large amounts of information with far greater speed, accuracy, and flexibility than has previously been possible.

Computers used in the control of industrial processes are similar to business and scientific computers in that they benefit from technological advances such as integrated circuits. Control computers differ from their siblings in that they are more compact, cost less, can accept input directly from the process, and must operate continuously in most adverse conditions. For example, a business computer usually lives in a temperature- and air-controlled, dust-free environment. A control computer must withstand extreme ranges of temperature and humidity and often must ignore vibrations caused by nearby heavy machinery.

Business and scientific computers differ from control computers in the thought and planning preceding their installation. Control computer installations depend on a great deal of advanced engineering and analysis of hardware and applications software for design, installation, and programming. In most cases, advanced mathematical models are made by system engineers to determine the exact configuration to explore the range of operations and to exploit potential operational improvements. Planning generally consumes more than two years prior to installation. Once installed, the control computer must function almost immediately in an error-free manner. Experience has shown that success in a given installation is directly proportional to the size of the user's planning team, not to the vendor's support.

Such thorough planning is not the norm in a business or scientific environment where debugging may take up to 6 months or even longer before efficient processing occurs. The primary reason for this vast difference in planning techniques is that rerun time doesn't exist for a process that is on-line 24 hours a day.

Control applications can be discrete, continuous, semi-continuous, or batch and can be serviced by a single computer or a myriad of computers linked in a plantwide system. Functions can include the allocation of tasks to and the control of lesser computers; raw material operations; inventory maintenance; materials scheduling; future orders; and utilization of equipment capacity.

The components of a control system are basically the same as those of a business or scientific computer system: a main memory unit to store programs and data; a control unit to direct computations and switching; an arithmetic unit to perform calculations; and input-output units to communicate with the computer. In business and scientific computers as well as control computers, the control unit plus the arithmetic unit is called the central processing unit.

Unlike a business or scientific computer system, however, a control computer system is connected directly to sensing devices which measure product qualities, raw material characteristics, temperatures, flows, pressures, and other process conditions. Various signal converters change the signals from these sensing devices into a digital form that is usable by the computer. The devices or positioners in the process receive signals from the computer relayed through analog controllers; or in some cases, analog controllers are omitted and the computer is connected directly to control devices or actuators for direct digital control (DDC). In a DDC system, the elimination of conventional instruments and control equipment offsets the cost of the computer equipment. A disadvantage is that manual control is harder to invoke in the event of computer malfunction.

Human intervention occurs through input-output equipment. An operator can communicate with the computer by using pushbuttons, switches, knobs, typewriter keyboards, video display screens, and punched paper tape or cards. The computer communicates with the operator through alarm buzzers, horns, lights, digital indicators, typewriter printouts, and video displays. Although the degree of difficulty varies, almost every control computer can be bypassed by the operator to take direct readings from sensors or to enter changes in the process through analog controllers or manual adjustment of control devices.

Figure 1 depicts a digital computer control system. Industrial process control developed before business and scientific computer control, and Figure 1 shows the similarities of concept in input and output. Not shown in Figure 1 are computer concepts once thought to have only commercial or scientific application that are now finding their way into process control technology. For example, information storage and retrieval methods have much to

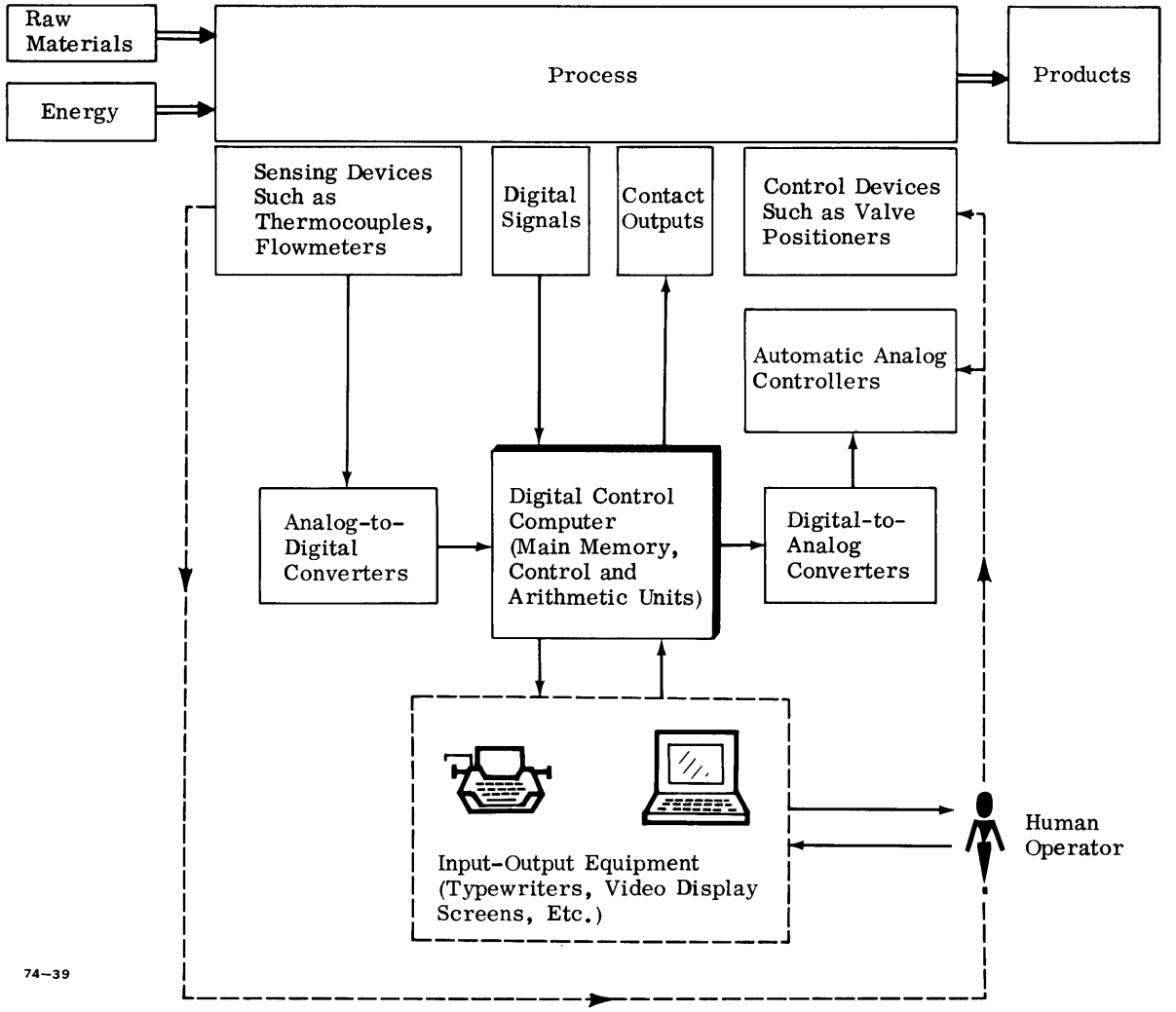


Figure 1. Digital Computer Control System

offer in the creation and maintenance of a system data base; time sharing has become commonplace; compilers, report generators, and batch processing techniques are all appearing in today's control computer systems.

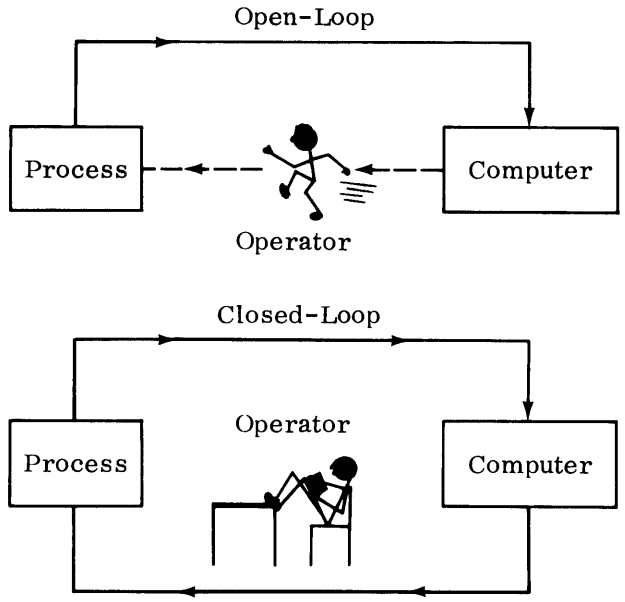
FORMS OF CONTROL

In the most elementary control applications, the computer is not connected to the process but functions as an extension of instrumentation to collect and record process data, which is entered manually and interpreted by the operator. In its more advanced functions, however, the control computer is connected directly to the process and is part of a total system of control. Advanced functions range from the output of explicit instructions for an operator to follow (open-loop system) to complete automatic control of the process (closed-loop system). The relationships in the open-loop and closed-loop system appear in Figure 2.

An advanced form of closed-loop control is optimized control. The objective of an optimized system is to achieve the best or most desirable operating conditions while also controlling ultimate goals such as production costs, yields, or efficiencies. The computer takes into consideration all significant variables, calculates the best process conditions, and applies the integrated control changes necessary to achieve the most desirable performance. This type of control is particularly appropriate for continuous processes in which many variables interact simultaneously. Optimized control, for example, can be used to achieve the most profitable product mix from a given input of raw materials.

CONTROL COMPUTER CONCEPTS

There are three main categories of tasks that a control computer can perform: supervisory functions, control



Note: Broken lines indicate manual handling of information; solid lines indicate automatic transmission.

74-40

Figure 2. Open and Closed-loop Control Systems

functions, and recording and reporting. In the supervisory role, the computer collects data and provides it in an accurate and timely form to the operators. In its control function, the computer calculates control action to be performed and either executes the control itself (closed-loop) or advises the operator of the action to be taken (open-loop). Recording and reporting is primarily used by management to promote closer control.

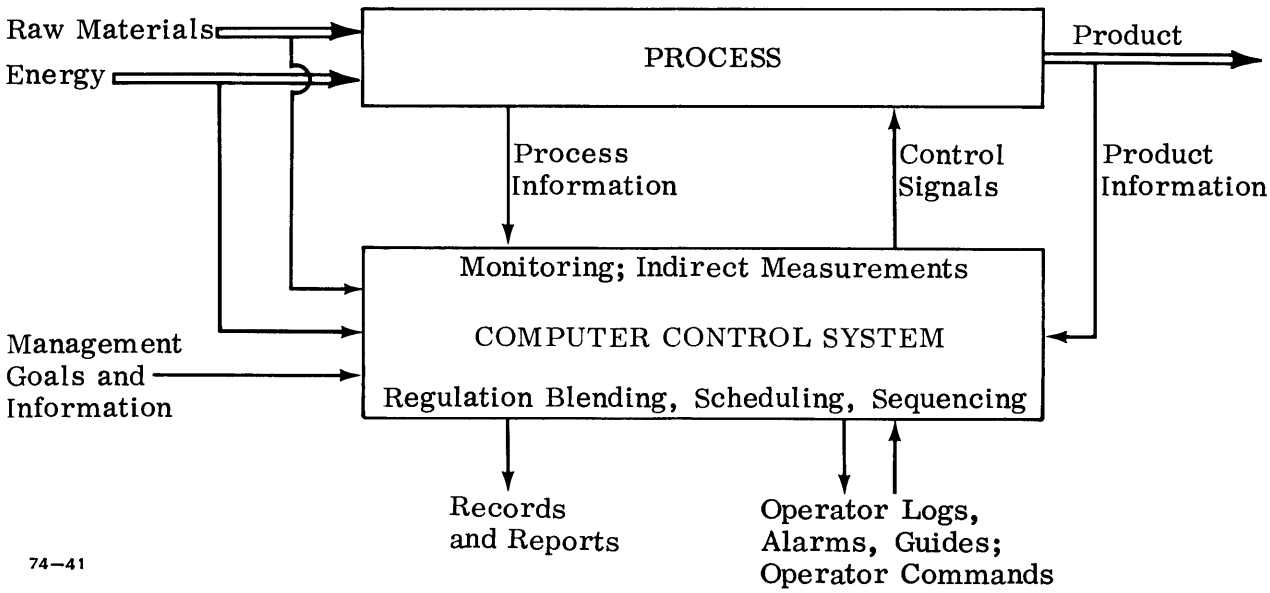
The tasks performed and the general information flow is depicted in Figure 3.

Supervisory Functions

Supervisory functions include process monitoring, indirect measurement, and logging and alarming.

Monitoring. Monitoring is necessary to define the conditions in the processing system. It is accomplished by determining the status of the instruments and process variables, the equipment, and the product. The status of the sensing instruments is determined by scanning on a fixed time schedule, by a signal from the process itself, or on demand either by the operator or by the control program. The frequency of scanning is commensurate with the use of the scanned data and the dynamic characteristics of the unique process. Scanning also involves the discernment of out-of-limit conditions. This can involve screening out wild or erratic readings by taking comparison readings from similar instruments in a different place.

Data from the process instruments is converted to digital form prior to its entry into the computer; the computer software is responsible for transforming the data



74-41

Figure 3. Information Flow in a Control Process

into meaningful units such as gallons per minute or degrees centigrade. Such conversions are accomplished either by conversion tables stored in main memory or by calculation through use of a suitable routine. Modification required by a change of instruments, instrument rescaling, or correction of various factors is accomplished by reprogramming rather than equipment modification of the control system. This versatility is a significant characteristic of the control computer.

Data from the process instruments can be further refined by data substitution, correction, calibration, compensation, smoothing, curve fitting, integration, and differentiation. Techniques such as these are generally performed by software routines.

The monitoring of equipment status prevents mistakes that could result in injury, severe equipment damage, or material losses by preventing (closed-loop) or guarding against (open-loop) forbidden combinations of valve settings, motor conditions, and so forth. Equipment monitoring of this type is standard in most control computer environments.

To determine the status of the products, the computer receives information on product quantity and quality either from the on-line process or from data entered manually by way of input devices such as the video display.

Indirect Measurement. Another major function of a control computer is to indirectly determine unmeasurable quantities by computation from other variables which are measured. Variables may be unmeasurable because the cost of sensing instruments is prohibitively high, relevant on-line sensing instruments are unavailable, the process noise at the desired measurement points is excessive, or the variable is a quantity that cannot be directly measured. Efficiency is an example of such a variable. Calculated variables are valuable as data for further calculations associated with the control functions of the computer and as necessary input to process-analysis studies.

Logging and alarming. The control computer can present information gathered through the monitoring and indirect measurement of the process through logging and alarming functions. (These are different from reporting and recording, which are discussed later.)

Logging is a data acquisition function that can be periodic (continuous analog signals) or non-periodic (chromatographs operating asynchronously with the control system). Information that is logged can be output on a fixed schedule, in a response to an operator inquiry, as an exception report, or as a result of an event in the process. The form and content of the report are established and modified by software. Generally logs are of two varieties: One presents information directly needed for the operation of the process whereas the other provides selected data for supervisory personnel. Averages or exceptions, for example, have meaning for planning but not for direct control of the process. Logged information is communicated by means of typewriters, video display units, and plotters.

An alarm system immediately communicates to an operator that an out-of-limit condition has occurred in either a process variable or a piece of equipment. An alarm can be a light, a typed red warning message, a buzzer, a horn, or a video display. Predetermined emergency situations can be immediately and automatically handled by corrective action by the control computer if it is configured with the appropriate devices.

Control Functions

Computer control can regulate process variables at a desired value, carry out a schedule or a sequence of predetermined process actions, and optimize processes.

Regulation. Regulatory control adjusts set points of local analog subsystems. The control can be feedback, feedforward, or multivariable. Feedback control can regulate an output variable that is measured indirectly. Feedforward control gathers information, anticipates, and counteracts possible upsets to the system. Multivariable control simultaneously manipulates several input variables to produce a desired output value without violating process limits. Raw material blending is an example of multivariable control.

Standard procedures for regulatory control include the solution of conversion equations for feedback control, validation for high-low limits on variables and outputs (including recognition of reverse reaction response), output status checks and dynamic adjustment features. The control computer does not handle all of these procedures; some are handled by sophisticated process equipment such as multi-variable controllers and other instrument units that include integrated computing circuits. The special purpose process equipment is not only generally less expensive but also less flexible than the control computer.

Scheduling and Sequence Control. Scheduling and sequencing control supervises the flow of materials through a plant and the events that operate on it. Successful operating conditions must be reproduced consistently and uniformly. Scheduling control is limited in its use because it assumes that other factors are always equal and that the same action produces the same results. Because of its limitations, scheduling control is often presented to an operator as an open-loop suggestion.

Sequencing control handles the coordination and serial-control problems of a process. It is used when a series of predetermined control actions must be carried out and considerable monitoring and checking must be done before proceeding from one step to the next in the sequence. An example of such control is the starting and stopping of a steam-boiler and turbine-generator unit.

Recording and Reporting

Documentation of process information is generally business-oriented and is part of a management information system. Reports include material usage, production, cost accounting, inventory management, lost-time analysis, maintenance required, equipment performance, quality control, process analysis, legal records, and information retrieval. The most traditionally business-oriented function is information retrieval, which requires a large data base usually stored on a magnetic disc.

Other business-related tasks that can be performed by a control computer include accounting and clerical jobs, production planning, and inventory control. These functions are normally executed in a batch environment although occasionally they are done in a time-shared environment.

CONTROL COMPUTER HARDWARE

Basic to determining the capabilities of a control system are the interrelationships and characteristics of its input and output, arithmetic and control units, main memory, and priority-interrupt features. Both process and non-process devices are relevant to a control computer.

Non-process devices such as magnetic disc, drum, tape, and operator's console are needed for operator communication and for storing and retrieving information. These devices can attach to the system through a direct memory access (DMA) channel or through a programmed I/O (PIO) channel; high speed devices (disc, drum) connect to DMA and slow-speed devices to PIO. The best results occur when all devices are buffered. Processor arithmetic speeds, storage access times, instruction execution times, and maximum data transfer rates are less relevant for control computers than for business and scientific computers. Although these characteristics are important, they do not indicate true on-line process control capabilities. Other factors such as reliability are far more important.

Central Processor

The processor, through programs stored internally in main memory, directs the operation of the entire system. A control system has one or more processors. Multiprocessor control systems generally function in a clearly defined hierarchy of control or one processor operates as a backup for the other in case of failure.

Important features of processor design include word-size, instruction set, addressing methods, information transfer rate, and priority interrupt system. These influence programming, effective computing speeds, and storage utilization.

Another important feature is the interval timer and clock. Because this circuitry is often handled by pulse-counting on input channels, the discussion of the timer appears later under DIGITAL INPUT CHANNELS.

Information Transfer. The rates for information transfers between the processor and main memory and between the input and output channels and devices are extremely important because they affect the performance of the overall control computer system. If input-output facilities are limited it is difficult to use a digital computer efficiently. Some older systems, for example, cannot perform parrallel computation with data transfers. Others do not have a DMA facility. These limitations are rare for newer systems, however.

There are three main ways to enter information into the system: programmed entry, buffered entry, and direct entry. Programmed entry in its pure implementation is the worse possible means of entering data into a control computer. Input and output cannot be overlapped with computations because every piece of information passed into or out of the processor's storage proceeds under direct control of program commands, which of course use processor cycles. Programmed entry is best used for non-critical data that can be relegated to a low priority.

Buffered entry is a step above programmed entry. Buffers are storage registers functioning as "way stations"; they hold information temporarily until the processor is ready to receive it or the peripheral devices and channels have time to operate on it. Buffers allow the processor to proceed with computations after initiating a command to peripheral units, which then complete the commands or actions independently of the processor.

The number and size of buffers vary, but the minimum requirement for a control system is a one-character or one-word data register plus an input-output addressing and control register. Buffer registers for each type of input-output (analog, digital, or logging) provide complete overlapping of processing, input, and output.

Direct entry is by far the most straightforward means of data entry because it allows essentially simultaneous computations and input-output functions. Direct entry has specific main memory locations associated with the input and output variables. Transducers or converters transform inputs to or outputs from digital form. These functions are performed independently of the control programs and require external control circuitry for switching and timing.

Information flow within the control computer in its optimum case is depicted in Figure 4.

Word Size. The word is the basic primary unit of data. Words are generally a sequentially numbered group of bits, data bits as well as check bits or parity bits.

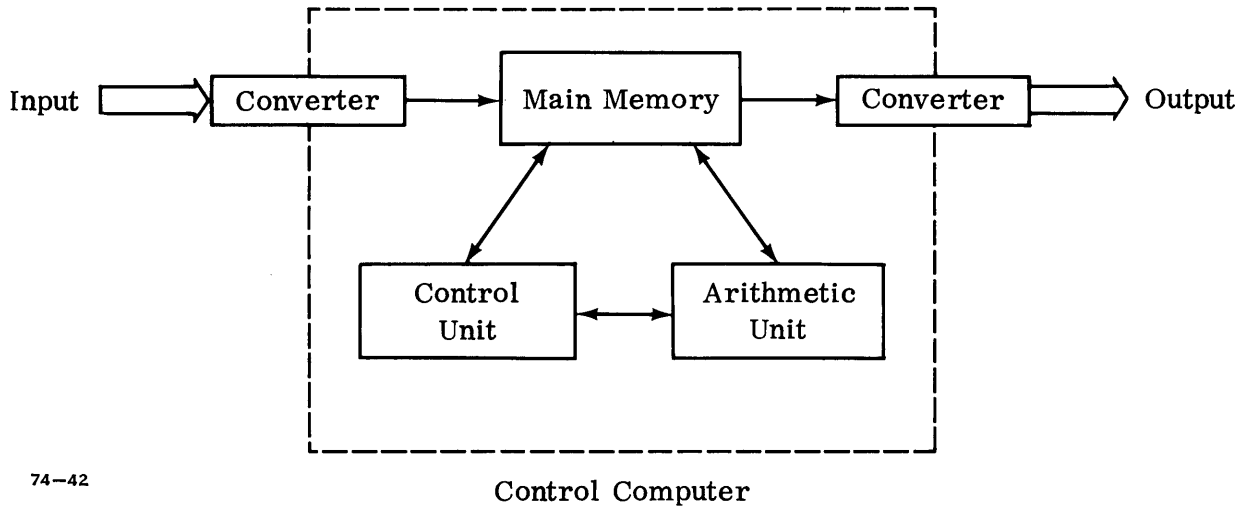


Figure 4. Optimum Information Flow in Control Computer

(Parity bits are not always used). Words can be fixed-length or variable-length. Variable-length words are the most flexible and offer the most efficient means for specifying adequate precision in calculations. Fixed-length words often require double word calculations for adequate precision.

Instruction Set. The control computer's instruction set can reduce the number of "housekeeping" functions necessary by providing the right kind of instructions. Instructions to transfer large variable length blocks of data between storage units or between memory locations should be provided. Instructions should perform more than one operation in a single command. They should allow direct, indirect, indexed, and immediate addressing. The most powerful and precise instruction sets for process control allow variable length word manipulation at any desired bit level. Such instructions, however, are usually bulky and time-consuming to code.

Priority Interrupt. The interrupt system is the primary vehicle for handling emergencies, accepting intermittent data, and interleaving diversified on-line and off-line tasks. It allows the processor, upon receipt of an interrupt signal, to suspend work on the program in progress, to transfer control to another program, and to return control to the original program automatically when the routine is finished. An example of an emergency interrupt is a power-failure interrupt. Important considerations in a power failure situation are safety to humans, equipment, and data.

Interrupt signals are caused by electrical impulses or by switches. Electrical impulses can come from either the computer system or external devices. Switches can be set manually or by alarm devices or process events.

In the complex control environment, interrupts must be serviced according to a clearly defined hierarchy of priority levels. This can be provided both by equipment and programming; most systems use a combination of hardware and software interrupt priority scheme.

Main Memory and Auxiliary Storage

Main memory stores the data, programs and results currently being used. The most important characteristics of main memory are its size, addressing capability, and sensitivity to power fluctuations. The size of main memory required for a system depends on the definition of the process and the tasks to be performed. Memory size is measured in terms of the smallest addressable unit, for example, 16K 16-bit words or 16K bytes.

Most main memory components used today (semiconductor, plated wire, core) are sensitive to power fluctuations. Power-failure protection is therefore provided by circuitry that prevents storage accesses when power-supply voltages are below safe limits.

Main memory protection is also essential in a control computer to prevent interference to the process while another program is being "debugged" or run. Protection at the hardware level is provided by logic circuits that inhibit the execution of any instructions that attempt to write in a protected portion of main memory. At the software level, protection is accomplished by the operating system's assignment of protection keys to individual program areas. A comparision of protection keys precedes a program's access of memory.

Auxiliary storage is usually a magnetic disc or drum; it stores data or programs not immediately required by the

control computer. Disc or drum access times are significantly slower than non-rotating memory access time; moving head discs are the slowest. Because it is too slow, magnetic tape is rarely used as auxiliary storage in a control environment.

Input and Output

Programmers and engineering personnel, the computer, and the process communicate with each other by way of input-output channels. Channels are characterized by their ability to operate simultaneously with processing, their transfer rate, and their transfer mode. Maximum flexibility of I/O structure is one of the strictest requirements in a control system; most systems can transfer data by way of programmed I/O, buffered I/O, and direct memory access.

The types of input/output devices, logging devices, and displays cover a wide range. Control computer systems offer input/output expansion in small increments: up to over 2000 analog and digital inputs, several hundred analog and digital outputs, and multiple logging and display devices. Furthermore the process environment dictates that the channels and devices can be added or deleted as required.

Input-output channels often perform some integrated computing and control functions such as "compare" and "add". This unburdens the processor of highly repetitive functions such as those involved in comparing a measurement with a standard value to detect random or out-of-limit events. Intelligent channels simplify programming, reduce interrupt operations, provide more efficient memory utilization, and improve the overall capabilities of the control computer system.

Types of Channels. Channels in a control environment are defined in terms of their functions and the equipment they service. Two basic types of channels handle analog input and output and digital input and output.

Analog input channels contain control registers and data registers that receive instructions from the processor. General functions the channel provides are termination points for process analog signals, the conditioning and normalization of the signals to required levels for amplifiers or analog-to-digital converters, analog-to-digital conversion, and data transfer to the processor's storage. Specific functions might be the selection of the exact process point to be read, the generation of proper timing signals, initialization of analog-to-digital conversion, and generation of an interrupt to the processor if necessary. A termination unit, signal conditioner, multiplexer, amplifier, ADC, limit comparator, or calibrator (including thermocouples) can be attached to an analog input channel.

Analog output channels are required for closed-loop systems and basically are a special form of the digital output channel that converts digital data to analog form. Outputs are voltage or current, pulse train, or pulse duration signals.

Digital input channels scan, assemble, and accumulate discrete digital inputs into a suitable input format such as bytes or words. Digital input channels may or may not be intelligent. Those unintelligent channels can seriously degrade processing throughput because they require program (processor) time to perform their process functions. Intelligent channels perform status sensing and pulse counting and can provide effective input rates of 100,000 to 1,000,000 bits per second without requiring any processor time.

For status sensing, digital inputs are scanned sequentially. Changes are sensed by comparing present-status with last-status values held in registers. If necessary, the channel generates an interrupt. In pulse counting, pulses generated by process devices are integrated or accumulated. Pulses represent a unit of measurement such as time, volume, length, and so forth. Time integration is an extremely important function of a pulse-counter because elapsed time and real time are required by the control computer to determine when to initiate control actions, logs or updates.

Digital output channels provide transfer paths for digital signals from the computer to the process or process operators. Output can be contact operate, pulse output, pulse duration, display drivers, or printer output.

Instrumentation

Instruments in a process can be divided into two broad classifications: measurement and control.

Measurement. Measuring instruments are sensing, indicating, or recording units. Ranges vary from 3 to 15 pounds per square inch for pneumatic instruments or 1 to 5 milliamperes, 4 to 20 milliamperes, 10 to 50 milliamperes, and −25 DC to +25 DC volts for signals.

Factors measured include temperature, pressure, flow and liquid level. Temperature is measured by thermocouples, resistance thermometers, and gas-filled or liquid-filled thermometers. Pressure is measured by pressure gauges; flow by flowmeters; and liquid level by a displacement-type level meter.

Measurements or factors in measurements can be further analyzed by instruments such as mass, infrared, ultraviolet, and nuclear magnetic resonance spectrometers, gas chromatographs, and infrared analyzers.

Control. Controllers generally control a single variable. Cascade and ratio control systems, however, relate two or more variables. Controllers sense and compare; they also correct in a closed-loop feedback control

system. Controllers can be of the on-off, floating, proportional, ratio, or cascade type. Controllers often contain analog computing elements that can multiply, divide, or take the square root. At most, they handle three variables.

RELIABILITY AND PERFORMANCE

Down time cannot exist in a process that is on-line 24 hours a day. Therefore, business and scientific computers' down times—which range from 5 to 15 percent—cannot be tolerated in a control computer.

Reliability

Reliability is a function of components, design, manufacturing, and overall system performance. Components must be long lived and have predictable characteristics, which can usually be determined by qualification tests. The most useful measure of reliability is the mean time between failures (MTBF).

MTBF is calculated either by actual experience or by combining the reliability of the component parts. Because there are so many components in a digital computer, the best design minimizes their number by organizing components to avoid duplication of function. (Duplication is used, however, for system backup.) Strict quality control in manufacturing components is a necessity.

Reliability is no guarantee of perfection so preventive maintenance is a critical factor. Possible equipment failures must be detected. This can be done by diagnostic programs, test points and indicators, and/or modularity of circuit design. Diagnostic tests and internal parity checking can detect and pinpoint marginal conditions and impending failures. Test points and indicators can be set to generate an interrupt if they are not reset after a specific time. Since modularity allows for substitution of defective parts, they can be repaired off-line.

Even more important than reliability and maintenance is making the system fail-safe — designing the system so that failures, if they occur, will not result in uneconomical or hazardous operation. System fail-safe measures can include an operator alarm system to warn of unsafe or out-of-limit events; a means to transfer control to completely manual operation; the establishment of predetermined set-points for all control devices in the event of system-failure; and the duplication of the control computer for backup.

The nature of a given application determines the method used for making the system fail-safe. System failures can also occur external to the control computer. For example, a measuring device can provide incorrect readings. Programmed checks aid in detecting and correcting such external failures.

Performance

Performance in a control computer environment is not necessarily determined by the sum of the performance of the parts; rather, it is determined by unique interrelationships between components, hardware, software, and so forth.

Primary considerations for determining the performance of a control computer include the following factors.

- The speed with which the system can scan input data (the number of inputs acceptable), convert it to machine language, check it for reliability, and store it in working storage for processing.
- The amount of processing time required to solve the control algorithm.
- The time the processor requires to execute control programs.
- The number of logs and printed records the system can produce while controlling the process.

A control computer that uses a relatively slow processor but extensive buffering and direct entry I/O channels may perform better than a high-speed processor that uses only programmed I/O and minimal buffering. Thus, a detailed analysis of each system must be performed before a system is selected for a particular application.

CONTROL COMPUTER SOFTWARE

The biggest difference between a control computer's software and that of a business or scientific machine is the way it implements the interrupt scheme. The control computer must operate on actual time (clock time) and must operate in relationship to other events external to the computer. A control computer also receives information directly from instruments and must respond instantly to priority signals from the process.

Throughout this report we have assumed the primary importance of process mostly because its failure can be hazardous and costly. There are environments, however, where the control of a process is a secondary application on a computer intended primarily for batch or time-shared processing. The power and complexity of the control routines required by a given application cover a wide spectrum. For example, an application can require a highly complicated executive and little or no time is available for time-sharing or batch processing operations. In other cases, the on-line process is relatively straightforward, but involved preparations are necessary in other areas.

Software for a control computer consists of two types: operating system software and application software. Both are indispensable to an efficient control environment.

Operating System

The operating system is the most essential part of a computer control system. Besides coordinating the on-line programs, which is its primary duty, it must also coordinate other processing activity such as time-shared applications and/or batch processing.

Time sharing is the primary means of compiling or assembling additional programs, running test data, analyzing plant data, and executing unrelated off-line work. The batch mode generally performs off-line reporting and runs non-process related programs such as accounting or inventory control.

Time sharing is a risky business in an on-line control computer; therefore, the executive must have means, usually storage protection, to protect the process application from unwitting destruction and to protect the executive itself against tampering with its interrupt scheme.

A control computer operating system must schedule the execution of the various process programs, coordinate the servicing of priority interrupts, supervise input-output, analyze and correct computer malfunctions, and handle large storage transfers.

The core program in a control computer's operating system is the monitor, executive, or supervisor. All other programs report to the executive, which schedules and controls all program execution. The following routines report to the executive.

- The system error monitor receives input from the error detection hardware and initiates the requests for error analysis and correction programs.
- The scan control monitor services the interface between the process instruments (the analog-digital equipment) and the computer system.
- The input-output monitor handles operator communications, logging typewriters, and programmed input-output requests.

Because the primary responsibility of a control computer is the process, all process interrupts or service requests must be handled before any other programs are executed. Only the idle or unused time can be allocated to time-sharing or batch operations, and, if necessary, these operations must be immediately interruptable by the process. The interrupt monitor is of equal importance with the executive, but it is usually subservient to it. The interrupt monitor responds to external interrupts from the process, timer interrupts, and internal interrupts from the processing programs (system interrupts). Timer interrupts are generally considered system interrupts.

Process interrupts can be initiated manually or automatically. They denote process conditions that require attention; they may also serve as an alarm. System interrupts promote efficiency of the control computer and prevent possible malfunctions. Clock interrupts indicate the passing of discrete periods of time and can be used to start a scheduled operation.

Interrupts are also described in terms of their relationship to the control computer. An interrupt system can be single or multilevel, and it can be priority- and/or nonpriority-oriented. An interrupt level denotes its degree of susceptibility to being interrupted. For example, there is always a non-interruptible level for critical processing. Additionally, there can be one or more interruptible levels. When there is more than one interrupt level, interrupts are assigned levels according to the interrupt function and its time constraints. The differences between single-level and multilevel priority interrupt systems appear in Figure 5. Figure 5 assumes three interrupt conditions with priorities in reverse order to the order of receipt of the interrupts. That is, interrupt

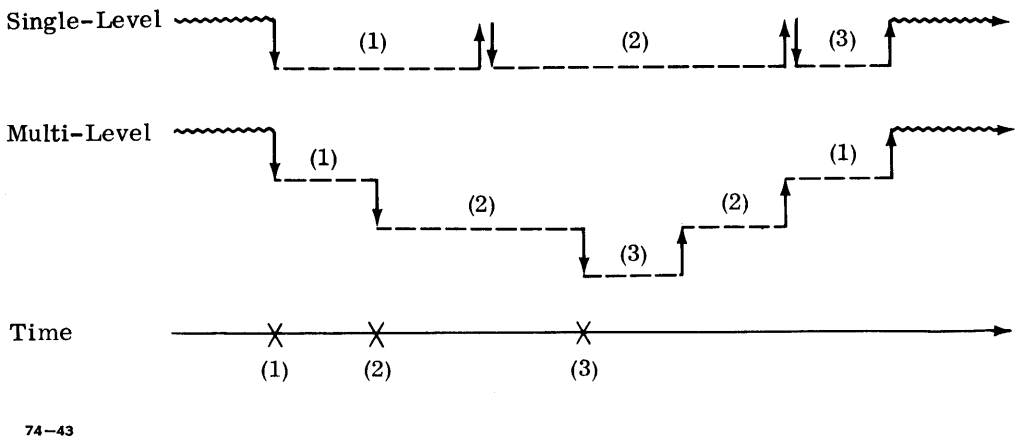


Figure 5. Single-level and Multilevel Priority Interrupt Systems

one has the lowest priority but is received first. The figure shows that multilevel priority interrupt systems are more efficient in responding to priority interrupts, but there is little or no saving in overall elapsed time.

Applications Programs

For business and scientific computers, applications are coded in computer programming languages, either higher level languages or assembly language. It is the same for control computers. Historically, higher level languages are easier to program; code is easier to document or it is self-documenting; software is easier to maintain; and the capability for extremely complex arithmetic and logical operations is provided. High level language compilers, however, run slower; use more system resources, particularly time and space; and do not provide the level of detail usually required in a control process.

Assembly languages are harder to program than higher level languages; codes are harder to modify; and programs are harder and more time consuming to document. Assembly languages are weak where higher level languages are strong. Also, assemblers run faster and provide a level of detail equivalent to the addressing level of the control computer. Assemblers are generally preferred for control applications; in particular they allow an application program to attain a very close relationship to the executive routines, notably the interrupt monitor.

A concept originally conceived for the scientific environment but heavily used for applications programs on control computers is code optimization. Depending on the needs of the application either time or space can be optimized. If the amount of information to be handled threatens to exceed the storage capacity of the computer, space must be optimized. On the other hand, if the time required to complete a calculation or processing phase exceeds the time prescribed, timing must be optimized.

Assembler programs are generally optimized by the programmer; higher level language programs are optimized either by the programmer or by an optimizing compiler. Optimizing compilers generally consume large amounts of resources but generally produce tighter, faster code.

CONTROL COMPUTER APPLICATIONS

Control computer installations are unique because the processes to which they are applied are as diverse as industry itself. Selected applications are presented here in order to give the reader an opportunity to relate typical applications to his own industry and his own problem.

Chemical Industry

The chemical industry processes ethylene, ammonia and methanol, and other chemicals.

Ethylene. The most valuable function of computer control in an ethylene plant is the optimization of operating profit, which is subject to all the process restraints and market limits that exist. In fact, the cracking furnace is generally the primary target of an optimizing program. The control computer also regulates the distillation portion of the plant to make products of specified purity and to carry out the specifications called for by the optimizer in terms of product splits and losses.

Typical plants can have five to 20 cracking furnaces with an assigned feed type. Although many feed types exist, most plants use either light hydrocarbons such as ethane or propane or heavier feeds generally described as napthas. Ethylene is the primary product, but other byproducts are also generated. All must be passed through compression and distillation equipment.

There are at least three independent variables for each cracking furnace: feed rate, diluent steam rate, and heat input. Each furnace can have a number of operating constraints, such as the cracking coil skin temperature, the furnace temperature, and independent variable limits.

Additional variables and constraints follow the cracking process, such as loading limits in the process gas compressors and each distillation column. The limits are a function of the products produced.

Ammonia and methanol plants. The primary function of computer control in ammonia and methanol plants is to increase throughput where market limits do not affect the production level. Neither process produces very useful byproducts. Because the equipment costs tend to discourage oversizing, the invariable bottleneck in any ammonia plant is in compression. Therefore, control computers are mainly concerned with getting as much synthesis gas through the compressors as possible at any given time. This throughput is dependent on ambient conditions and compressor availability. Maximum amount of conversion-per-pass at the synthesis converters is also important, and the conditions to achieve this target change as catalyst activity changes. There is an important tradeoff in this respect; conversion efficiency increases as pressure increases. Compressor throughputs must be restrained in order to increase compression ratios.

A control computer also regulates tasks. It maintains the proper hydrogen/nitrogen ratio at the shift converter, determines fuel to air ratios as well as outlet temperature control at the primary reformer, and regulates the methane content to the secondary reformer.

Rolling Mills

The production of steel was among the first applications of control computers because many parameters affect the product and decisions must be made very rapidly. Two important applications in the steel industry are hot-strip rolling and cold rolling.

Hot-Strip Rolling. The control computer allows improved productivity, more flexible scheduling, better gauge and width control, and less edge damage. Basically, the computer uses parameters such as slab temperature, composition, and dimensions to calculate and set side-guard positions, edger positions, edger speeds, table speeds, and main-roll screw positions. Constraints such as maximum allowable roll force, main-drive-motor load, and maximum roll bite are also taken into account. Because several slabs are usually handled at a time, the computer must keep track of all of them. When the slab is out of the roughing train, the computer determines the desired reduction schedule and optimizes the power distribution among the multiple finishing stands for maximum production. Supervisory functions include monitoring temperatures of the roll bearings and motor windings, voltage and current of each mill motor, strip tensions, and strip thickness. Other functions include automatic production reports and mill pacing to achieve maximum throughput.

Cold-rolling. Cold rolling is done with an incoming strip made from several hot-strip mill products welded together. The control computer calculates the reduction schedule that will minimize the number of passes. It also controls coil deceleration, mill reversing, and acceleration. It must also determine when the end of the roll is being reached. Thickness measurements allow the computer to preclude strip tension exceeding the yield point of the metal.

Cement Plants

The production of cement involves blending and grinding raw materials, which are fed into kilns to make cement clinker. The clinker is then ground to make cement.

An important consideration is the amount of free lime in the clinker because it cannot exceed a prescribed amount. Heat input is another variable which can be controlled in several ways varying in complexity. Most use an off-line model for optimization in conjunction with an on-line regulation scheme. Optimization is for either a market-limited or production-limited situation. Multivariable control loops are usually employed for regulation. Other control functions include detecting upset condition detection, automatic start-up and shutdown, and control of blending raw material to smooth out fluctuations in the feed.

Some variables are controlled in the cooler section: secondary air temperature, undergrate pressure, overgrate pressure differential, and exhaust fan temperature. Manipulated variables are cooler drive speeds and cooler fan throughputs.

Controlled variables in the kilns are: burning zone temperature, fuel to air ratio, before chains gas temperature, and before chains solids temperature. Manipulated variables in the kiln are fuel rate, exhaust fan speed, kiln speed, and kiln feed rate.

Petroleum Industry

Some functions of the control computer in the petroleum industry include oil refining (crude oil distillation, catalytic cracking) and pipeline and terminal operations.

Crude Oil Distillation. The primary function of a computer in a crude oil unit is regulation. Specifically, regulation involves computing the flows of all products to satisfy production requirements and still keep each product in specification. A model is required to predict cut-point temperatures as a function of draw rates. Adjustments in reflux and bottoms temperature must be made to compensate for effects of changes in product rates on tops and bottoms. Distillation usually requires a large-capacity control computer because there are many interactions and long dynamic lags in the various columns of a crude unit.

Fluid Catalytic Cracking. Fluid crackers, like crude units, are large and complex. The main goal of computer control is optimization of product yield, distribution, and throughput. Optimixation is on-line because a fluid catalytic cracker is never in a steady-state condition.

The chief controlled variables are recycle ratio, reactor temperature, and catalyst/oil ratio. Others are air rate, stripping stream to the reactor, fresh feed rate, and system pressure. Most of the variables are dependent.

Pipelining and Production. In both applications, the computer acts in a supervisory capacity. In pipelining, it handles automatic dispatching, inventory monitoring, batch tracking, and supervision of remote compressor and pumping stations. In production, it handles automatic well-testing and data acquisition for oil, water, and gas production; well start-up and shutdown; pump control; and inventory monitoring.

Oil field applications often use satellite data acquisition stations because there are many scattered, remote wells, and state requirements and multi-owner relations in unitized fields make frequent status evaluation necessary. Also, off-shore sites have peculiar problems such as automatic shut-in.

Pulp and Paper Industries

One critical area for a paper mill is raw material variation as determined by the pulp characteristics. Other operating variables are additive flows, temperature, head box level, slice position, wire speed, vacuum, press roll pressures, dryer environment, and intersection tension.

Many of the variables in the paper product industry, especially for the finished product, are not measurable on-line. Examples are basis weight, thickness, tensile strength, color, and moisture content. Feedback control is difficult because of the noise factor. Variables, therefore,

are measured either by beta-gauge measurements or occasionally by programmed histories. Often a statistical approach is used to reduce the standard deviation of the basis weight significantly.

Power Generation and Distribution

One of the primary considerations of computer control in this industry is the avoidance of catastrophes. Many computer installations are dedicated to monitoring and surveillance. Certainly, monitoring and alarming functions are performed in all power plant computer installations. Some are also fully automated including cold start and shutdown.

Direct digital control is often used because it is required by such operations as sequencing the start-up of a boiler-turbine-generator system. The computer supervises the feedwater, firing rate, and level controls, allowing the boiler to produce constant enthalpy steam. Steam supply initially is tightly regulated; later, the values are handled automatically. Start-up of a cold turbine requires coordination of high-pressure and low-pressure sections; initial check-out; acceleration to operating speed; synchronization with the electrical network; and finally, loading to the specified level. Metal thermal shock, excessive vibration, and over acceleration must be avoided.

Power dispatch is another area regulated and controlled by computers.

Nuclear power plants require approximately the same functions as conventional power installations. In place of a boiler fired by fossil fuel, the heat source is a nuclear reactor which is susceptible to rapid and wide-ranging transients that can cause catastrophic damage. Monitoring these transients and detecting deterioration of operation before a real hazard exists is an important role for a control computer.

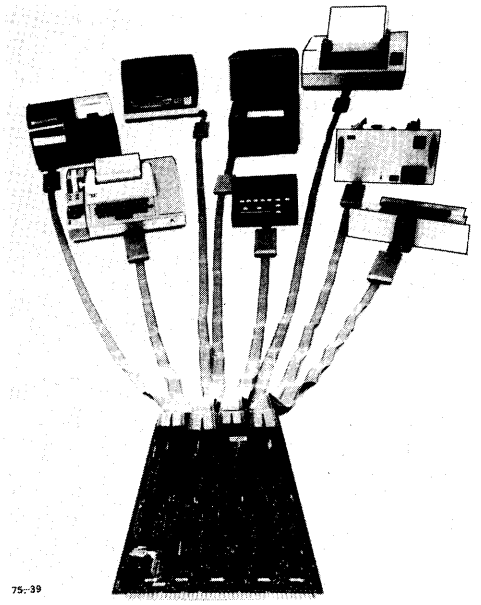
Food Industries

The computer's role in food industries usually is that of a high-level supervisor which examines the accuracy of each step of various subsystem operations and requests adjustment or signals an advancement to the next step. Food industries often use open-loop control system or mixtures of open-and closed-loop systems. Hundreds of variables are required for computer control. They include sensor measurements such as temperatures, humidities, flow, pressure, level, and quantity. Other functions include requesting and adjusting the liquid and dry ingredients added to batching equipment; monitoring bulk storage of ingredients; control of batch blending and mixing from stored recipes; monitoring time cycles, oven temperatures, and speeds; recording of production leaving the lines; direction of storage and retrieval of products in holding areas; and recording and outputting inventory and available-space data.

Another function in food industries (and others) is automatic warehousing. Stacker cranes must be used in the most efficient manner; plus a real-time inventory often must be maintained.

COMPUTER AUTOMATION

LSI-3/05 NAKED MILLI®



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OVERVIEW

Computer Automation announced the LSI-3/05 NAKED MILLI on January 16, 1975, as part of an overall expansion of its existing product line. The NAKED MILLI is a computer-on-a-board (7 by 15 inches), and competes with both microcomputers and small minicomputers for the OEM market. The NAKED MILLI is upward compatible with Computer Automation's LSI-2 line of minicomputers in that it can attach the same peripherals and interfaces as the larger systems. However, it approaches the cost of board-level microcomputers. In single-unit quantities, a processor costs $295 (without memory), while a system with 1 kilobyte of semiconductor RAM memory is priced at $695. Delivery is 30 days after receipt of order.

The NAKED MILLI LSI-3/05 uses the same basic architecture as the LSI-2 Series, but the processor cycle time is somewhat slower. The LSI-2 Series uses a faster processor and either 960-nanosecond or 1,200-nanosecond memory modules. Although LSI-3/05 uses the same 1,200-nanosecond memory as the 2/10, the processor slows instruction execution time. Thus, execution time for an Add or Subtract instruction is 6.0 microseconds on the LSI-3/05, 2.4 microseconds on the 2/10, and 2.06 microseconds on the 2/20 and 2/60.

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The LSI-3/05 is designed with bipolar MSI circuitry and TTL logic to produce a compact, low-cost system. It is a microprogrammed system organized around a Maxibus, with three major I/O subsystems: DMA, Direct Memory Channels, and Programmed I/O. The LSI-2 Series adds a fourth "Block Transfer I/O" capability not available to the NAKED MILLI. Memory for the LSI-3/05 can be MOS or core modules ranging from 1K to 64K bytes composed of 1K-, 2K-, 8K-, 16K-, or 32K-byte modules. Semiconductor RAM, ROM, and PROM memories are available as well as core. The register complement, priority interrupts, word or byte operations and eight modes of addressing are the same as for the LSI-2 Series. Table 1 lists system specifications.

The LSI-3/05 implements 93 instructions, which make up a subset of the LSI-2 Series instruction set. LSI-2/10 implements 162 instructions, LSI-2/20 implements 182 instructions, and LSI-2/60 implements 224 instructions. Table 2 lists typical instruction execution times for the LSI-3/05. Programs developed on LSI-2 systems can run on the LSI-3/05 by using subroutines for missing instructions.

Software for the LSI-3/05 includes the Real-Time Executive (RTX), including an I/O Executive (IOX), the OMEGA conversational assembler/editor, loader utilities, and a debug package. Table 3 lists available software. Programs developed under DOS on the LSI-2 can usually run on the LSI-3/05 without difficulty.

Peripherals for the LSI-3/05 are the same as those for all the other members of the LSI Series. These devices include discs, floppy discs, magnetic tape, punched cards, paper tape, printers CRTs, teletypewriters,

process I/O and communications interfaces. Table 4 lists the peripherals available for LSI-3/05.

The new I/O Distributor is an option that will enhance the entire LSI product line. By placing a microprogrammed PicoProcessor at the end of the cable that interfaces to a device, CAI can standardize cabling and provide a programmable interface that can translate unique peripheral interface characteristics into standardized three-state bus signals. The PicoProcessor also generates and checks parity. PicoProcessors are available in three versions; a parallel version for parallel TTL devices and two serial versions for current loop or EIA devices.

The I/O Distributor buffers and transfers data between the I/O bus and the PicoProcessor cables as well as providing interrupt priority control for two interrupts per cable. The standard I/O Distributor operates in DMA mode, with word/byte counts and addresses in memory instead of in controller hardware. The Serial Feature provides clocks for "strap selectable" baud rates from 75 to 19,200 baud, with each of the eight channels operating at a different rate if desired.

The I/O Distributor costs $380 in a single-unit quantity; intelligent cables cost $145 each. Discounts are available for volume orders. Delivery is 60 days after receipt of order.

Computer Automation was formed in August 1967 to manufacture and market minicomputers to the OEM market. Since its introduction of the Alpha and Naked Mini Series, and the later LSI versions, the company has shipped more than 5,500 systems. It also produces and markets the Capable Tester System; this computer-driven production line tester for digital logic modules was originally designed for its in-house production facility. Computer Automation has expanded steadily and now has 18 direct sales offices and service facilities in the United States. A number of distributors market this system in other parts of the world.

Table 1. CAI LSI-3/05: Mainframe Specifications

Identity	Characteristics
CENTRAL PROCESSOR	
Microprogrammed	Yes
General-Purpose Registers	8
Addressing	
Direct (words or bytes)	768
Indirect words	Multilevel
Indexed	Yes
Mapping	No
Instruction Set	
Number	93
Floating point	No
Priority Interrupt	
Levels (std; max)	5; 256
MAIN STORAGE	
Type	Core, semiconductor
Cycle Time (nsec)	1,200
Basic Addressable Unit	Word or byte
Min Capacity (bytes)	1,024
Max Capacity (bytes)	32,768
Increment Sizes (bytes)	8K, 16K, 32K (core); 1K, 2K, 4K, 8K (MOS)
Memory Parity	Option
Memory Protect	No
INPUT/OUTPUT	
Max Addressable I/O Devices	248
Conditional I/O	Std
DMA (no. of channels)	2-64

Addition of the NAKED MILLI and the MEGA-BYTER systems expands the market for the Naked Mini LSI/Alpha LSI line at both the top and the bottom. Naked Mini/LSI refers to Alpha/LSI systems without a chassis and interfacing hardware; conversely, Alpha LSI systems are packaged. The NAKED MILLI, as the name indicates, is offered in the "unpackaged" form only; the MEGABYTER is available both ways. The entire LSI line now consists of three processors: the LSI-1 (an MOS processor not yet delivered), the LSI-2 (Models 2/10, 2/20, and the Model 2/60 MEGABYTER), and the LSI-3/05 NAKED MILLI.

PERFORMANCE AND COMPETITIVE POSITION

The Computer Automation LSI-3/05 NAKED MILLI occupies an intermediate position in the computer market between microprocessors and minicomputers. Like microprocessors (the computers-on-a-chip), they are designed to be components. However, the NAKED MILLI carries this comparison further; even the power supply and console are priced separately. Like

Table 2. CAI LSI-3/05: Typical Instruction Execution Times

Instruction	Timing (SEC)
MEMORY REFERENCE	
Add; Subtract	6.0 (1),(2)
AND; Exclusive OR; Inclusive OR	6.25 (1)
Exchange A and Memory	5.25 (1)
Load A (or X)	7.5 (1)
BYTE IMMEDIATE	
Add to or Subtract from A (or X)	5.0 (2)
Compare to A (or X) Skip if Not Equal	4.5-5.0
CONDITIONAL JUMP	
Jump if OV Set	4.25-6.25
All Other conditional Jumps	4.0-5.0
SHIFT	
Logical, Left/Right, A/X	5.25 + 0.25/ shift count
Rotate Left/Right, A/X, with OV	5.25 + 0.25/ shift count
REGISTER CHANGE, CONTROL	
Disable/Enable Interrupts	7.0
Transfer A/X to A/X, Status Output from A/X	4.25
INPUT/OUTPUT	
Select and Present A; Output A/X	4.5
Input Word to A/X	5.25
DMA Input/Output Byte to Memory	17.0/15.25
DMA Input/Output Word to Memory	16.75/15.5

Notes:
(1) In byte operand mode, add 0.5.
(2) Add 1.0 if overflow is set.

minicomputers, the LSI-3/05 Series has systems software designed so the user can quickly implement applications.

Microprocessors range in size and capability from the Intel single chip to National Semiconductor's four-chips-on-a-board. Some manufacturers provide only chip sets, leaving the user to provide I/O, interface logic memory, and programs. Others provide board-level systems that may include memory and ease the I/O interfacing problems, but rarely provide standard interfaces to peripherals other than Teletypes.

The big advantage of the CAI minicomputer lies in its completeness: memory, peripherals, and software. For many applications the LSI-3/05 costs the same as or less than an in-house developed microcomputer, and implementation of the total system would be faster with the LSI-3/05. The Distributed I/O Subsystem option supports this concept of quick and easy interfacing. In addition, the user of an LSI-3/05 can move up to the compatible LSI-2 Series if requirements outstrip the LSI-3/05 processor capability.

The NAKED MILLI LSI-3/05 has several competitors from minicomputer makers also trying to extend market penetration downward. Digital has used the Intel microcomputer in its MPS system,which is not compatible with the PDP-8 or PDP-11 lines. Data General's Nova 2 is sold at the board level; Nova 2 is faster than the LSI-3/05 and also more expensive.

Although the projected LSI-1 system will be even more economical than the LSI-3/05, it will probably be accepted slowly because of widespread knowledge of CAI's design difficulties with the system. This possibility may be part of the rationale behind the LSI-3/05, which is intermediate in performance between LSI-1 and LSI-2, low in cost yet near the small size anticipated for LSI-1. The LSI-3/05 can carry the ball while LSI-1 is gaining acceptance.

Computer Automation has a competitive advantage over minicomputer manufacturers who sell both to end users and in the OEM market. Computer Automation sells only OEM, and system builders are not concerned about the company becoming a competitor. Also, Computer Automation stresses thorough testing of system components, as well as reliability in meeting production deadlines and living up to contractual obligations.

Although Computer Automation entered the field only 7 years ago, the

Table 3. CAI LSI-3/05: Peripherals

Model Numbers	Description
Discs	
18530-43	Moving-head disc subsystem, 1 fixed, 1 removable cartridge, 2.46M wds/drive, 4 drives/controller
NA	Floppy disc, 1.2M bytes, 4 drives/controller
Terminals	
22205-00	Teletype ASR 33-20/3JC, 10 cps
22230-00	A/N display, 1,920 char, 24x80 char, 64-char set, to 9,600 baud
Punched Cards	
18223-43	285-cpm reader
Paper Tape	
18223-12	300-cps reader
18223-61	300-cps reader, 75-cps punch
Printers	
18223-31	100-cps printer (60-150 lpm), 80 cols
Magnetic Tape	
18224-15	9-track, 800 bpi, 25 ips, 4 drives/controller
18240-01/02	Single/dual cassette drives, 520K bytes/cassette, 4 drives/controller
Process I/O	
13213-00	Digital I/O, 16-bit DTL/TTL-compatible
13214-00	Relay output module; 32-bit (1x32, 2x16, or 4x8)
13215-00	Relay input module; 32-bit (1x32, 2x16, or 4x8)
13216-00	Output module, 64-bit (1x64, 2x32, 4x16, or 8x8)
14223	Utility I/O, 8- or 12-bit parallel input or output
Communications	
14236	Single or dual interface for 1 or 2 EIA RS232-compatible CRTs or leased line modems
14535	Asynchronous programmable modem controller, 1 line to 9,600 baud
14512	Asynchronous programmable modem MUX, for 2 or 4 lines
14513S	Synchronous programmable modem controller, to 50K baud
14523	Automatic Calling Unit MUX for 1-4 ACUs

Table 4. CAI LSI-3/05: Software

Package	Description
Real-Time Executive (RTX)	Modular system consisting of multitasking executive (RTX nucleus), I/O Executive (IOX) subsystem, communications executive (COMX); RTX nucleus requires 650 wds of memory and console
BETA	Assembler
OMEGA Conversation	Adds on-line editing, updating, and conversational capabilities to BETA
IBM/360 Cross Assembler (XASM)	Written in IBM FORTRAN IV Level G; produces output identical to BETA and OMEGA
Utilities	Source tape preparation; loader, TTY/CRT utility, math packages, diagnostics

company grew rapidly until last year when its steady growth rate slowed somewhat due to the unfavorable economic climate. The expansion of its product line at both ends and the new I/O interfacing should provide other markets for CAI systems, and spur its return to previous growth levels.

MAINTENANCE

Since Computer Automation sells only to OEM manufacturers, it does not provide the type of on-site preventive and emergency maintenance contracts usually associated with end users. The company does offer a 1-year warranty. Components that break down are immediately replaced or repaired free of charge during the first 30 days. After that, parts are repaired at the factory; the user has access to "loaned" components (20 percent of purchase price) while repairs are made.

HEADQUARTERS

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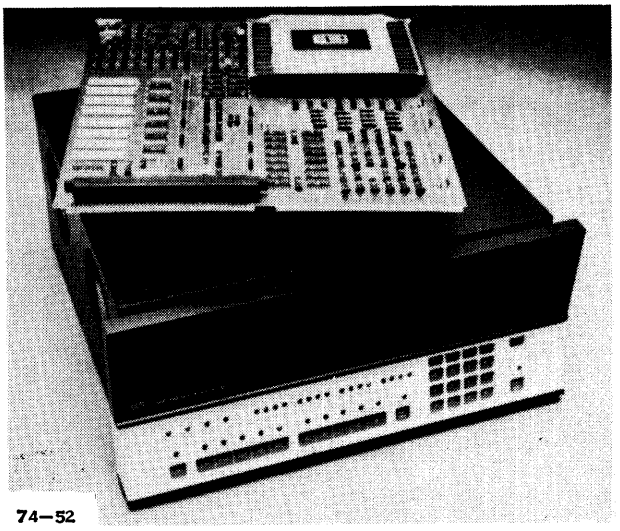

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OVERVIEW

The Computer Automation Inc. (CAI) Naked Mini/LSI and Alpha/LSI Series are low-cost, 16-bit, microprogrammed minicomputers aimed exclusively at the OEM market. Like their respective predecessors, the Naked Mini/16 and the Alpha/16, the Naked Mini/LSI is the bare hardware without chassis or power supply, while the Alpha Mini/LSI is the same hardware housed in a chassis with a pushbutton control console and power supply. The LSI (for Large Scale Integration) Series feature a full CPU and 4K words of memory for about 50% of the cost of their predecessors.

There are two basic LSI lines — the LSI-1, a MOS/LSI system, and the LSI-2, which uses a conventional ROM microcontrol unit and medium scale integration. LSI-2 is further subdivided into the 2-10 and the 2-20; both use 960 or 1200 nanosecond core modules, but the processor cycle time of the former is about half that of the latter.

LSI-1 was the first of the systems to be announced. Original specifications declared that the CPU and 8K words of memory would be fitted on one circuit board, for less than $1,000. It was the first of several similar announcements by other manufacturers extending the minicomputer market down to the edges of the microprocessor level. Computer Automation, like so very many manufacturers dealing with semiconductors, found their path beset by unexpected difficulties, so at the time of this writing the firm has not yet delivered LSI-1s in quantity.

The LSI-1 system was designed to implement both word- and byte-oriented processing using a 168-instruction set. Twenty instructions have been added to the LSI-2 processors to allow push-pop stack handling. The I/O structure is flexible, allowing five modes, and an asynchronous MAXIBUS that can attach up to 256K words of memory and peripherals. The first 2-20 system was delivered in September 1973. The slower 2-10 was introduced later, probably as a stop-gap measure to supply a slower, cheaper system while waiting for the LSI-1. Computer Automation's studies have indicated that the lower-speed, lower-price systems can satisfy 90 percent of the OEM market, while one-board systems can be used to computerize new applications.

Both systems can use the software and peripherals developed for their predecessors. Peripherals include discs, magnetic tape drives, cassettes, paper tape and card reader/punches, printers, displays, Teletype units, communications devices, and a number of general-purpose interfaces. Disc, tape, and cassette operating systems and a real-time executive as well as Assemblers and BASIC interpreters have been upgraded to handle the new, larger instruction set. A new Fortran IV compiler has been added.

Computer Automation was formed in August 1967 to manufacture and market minicomputers to the OEM market. Since the introduction of the Alpha and Naked Mini series, the company has shipped more than 4,500 systems. The company also produces and markets the "Capable" Tester System, a computer-driven production line tester for digital logic modules, that was originally designed for its in-house logic production facility. Computer Automation has expanded steadily and now has 18 direct sales offices and service facilities in the United States. A number of distributors market their systems in other parts of the world: D. C. Industries in Australia; the Metric companies in the Scandinavian countries (Scandia Metric AB in Sweden, Finn Metric oy in Finland, SC Metric A/S in Denmark, and Metric A.S. in Norway); Geveke Elektronica en Automatie nv in Belgium, Netherlands, Luxemburg and Germany; DataCare AG in Switzerland; Tranchant Electronique in France; Computer Advances in South Africa; Alfatronica in Spain; and Electro Marketing in Japan. Computer Automation has its own subsidiary, CAI Ltd. in England for sales to the United Kingdom and for support for certain parts of Europe.

Basic system specifications are presented in Table 1.

PERFORMANCE AND COMPETITIVE ANALYSIS

The Computer Automation LSI Series occupy an intermediate position in the computer market, between microprocessors and minicomputers. Like microprocessors (the computers-on-a-chip), they are designed to be low cost components; the Naked Mini carries this comparison further, since it is provided without power supply or console. Like minicomputers, the LSI Series have systems software designed to help the user program his application quickly. The higher-speed LSI-2, for example, is comparable with the lower to middle portion of Data General's Nova Series.

Table 1. CAI Naked Mini/Alpha LSI: Mainframe Characteristics

Characteristics	Alpha/LSI-1 and 2 Naked Mini/LSI-1 and 2
CENTRAL PROCESSOR	
General-Purpose Registers	8
Addressing	
Direct	768 words or bytes
Indirect	Multilevel, to 32K words or 64K bytes per level; 128K words max
Indexed	Yes
Instruction Set	
Number	162 (LSI-1); 182 (LSI-2)
Floating-point arithmetic	No
Priority	
Interrupt Levels (std; max)	5; 256
MAIN STORAGE	
Type	Semiconductor; core can be mixed
Cycle Time (μ sec)	0.96, 1.2
Basic Addressable Unit	Word or byte
Min Capacity (bytes)	2,048
Max Capacity (bytes)	524,288
Increment Sizes (bytes)	8K; 16K; 32K (core); 2K; 4K; 8K (MOS)
Memory Parity	Option
Memory Protect	No
ROM	Yes
RAM	Yes; can be mixed with core
I/O	
Transfer Rate	
DMA (wds or bytes/sec)	625,000 (1.25M with interleaved memory)
Block I/O (wds/sec)	131,579
Programmed I/O	34,247 via registers
Programmed (wds or bytes/sec)	24,631 direct to memory
Direct Memory Channels (wds or bytes/sec)	26,738
No. of DMA Channels (std; opt)	2; 64
Conditional I/O	Std
Max Addressable I/O Devices	248

The LSI-1 system, when it makes its appearance, will be particularly suited for the "gap-filling" role. General Automation looked like a formidable contender in this market earlier, because its SOS (silicon on sapphire) system was faster and more powerful, but it recently withdrew the SOS system, at least temporarily. Digital also produces a computer on a board based on the Intel microcomputer, but Digital's MPS is not upward compatible with its other lines. Many others have extended their lines downwards with low cost new models that use 16K-word boards and CPUs on a single board — Data General's Nova 2 line is a case in point.

Most minicomputer manufacturers market both to end users and various segments of the OEM market. Computer Automation's competitive advantage lies partly in its exclusive devotion to the OEM market. A manufacturer of data entry equipment, for example, might be interested in using the LSI-1 or 2 because Computer Automation as the supplier of his chief component will not suddenly enter the market in competition with him. As a supplier of OEM machines, Computer Automation stresses thorough testing of system components, as well as reliability in meeting production deadlines and living up to contractual obligations.

Of course, the comparative newness and small size of the company compared with giants like DEC and Data General have constituted some of its weaker points in the past. The continuing profitability and growth of the company have lessened the initial disadvantage, so the new LSI line should be received with even more interest—"success breeds success" as the saying goes.

The complementary design of the LSI-1 and LSI-2 is an added security to users who are apprehensive of using MOS because of the dependence on the MOS supplier. If the supplier withdraws his product the user's product collapses as well. Because CAI designs its own masks, it is not dependent on a single supplier but can switch suppliers if necessary. The LSI-2 Series, however, provides a back-up capability (at larger sizes and higher prices) for the MOS systems because the LSI-1 software and interfaces are upward compatible with the LSI-2.

User Reactions

A manufacturer of blood serum analyzers has bought around 200 CAI LSI units as a component, partly because of the price, but largely because the one-board CPU means simpler maintenance. The CAI computer is used for mathematical analysis of chemical reactions and for printing reports for doctors. The analyzer itself is controlled by another computer system. This user is very pleased with the performance of the system; CAI's support has been very good and response to service requests is prompt. The user made only one criticism; he feels that the programming manuals could be improved.

A second user is a prominent POS manufacturer using the system as a ROM simulator and a testing device for customized ROM units. The LSI-2 is programmed with the desired logic pattern and the pattern is then tested before it is fused into ROM firmware by another system. The resulting chips are then retested by the CAI unit. The company bought 15 of the LSI-2 systems and is now using some as field trial units. This manufacturer has found the mini to be an excellent machine with a very good capacity. He likened it to a Nova system, with capabilities somewhere between the DEC PDP-8 and PDP-11.

A department in a communication equipment manufacturing facility bought a single LSI-2 with an 8K-word memory and a Teletype for an in-house machine control application. The department chose the system over DEC and Hewlett-Packard systems partly because of price, partly because of the I/O structure, and partly because a neighboring department had one.

This user has had no problems whatsoever with his system so he was not able to offer any opinion on CAI's

service organization. When asked what he thought about the programming manuals, he said they are as good as anyone else's manuals; writers for all the manufacturers seem to leave something out as self-evident, when it is not self-evident to the user. This user's only annoyance was that he could not obtain logic diagrams and documentation on the memory board because it is proprietary. This user wanted to trace down trouble himself when it occurred.

CONFIGURATION GUIDE

There are two basic processor models in the LSI-2 Series; each has submodels, differentiated by the memory type and size packaged with the basic CPU. The original Alpha/Naked Mini 16 Series had "jumbo" as well as standard versions similarly broken out into submodels according to size and type of memory. Processor architecture is the same; LSI-10 operates at about half the speed of LSI-20 although both use the same memory.

All minimum Naked Minis, both old and new, consist of a processor with memory, but no power or control console. The Naked Mini 16s and LSI-2s also include a chassis and motherboard with a varying number of slots available, usually five or six. The minimum Naked Mini LSI-1s are to have no chassis and motherboard; the CPU and up to 8K words of memory are all contained on a single board. Naked Minis must be bought in quantities of at least five in the LSI Series and 10 in the older 16 Series.

All Alpha systems include the processor, memory, chassis, power supply, and control console; slots are available on the minimum system for attachment of additional memory and controller/interfaces.

Processor options for the LSI Series include Power Fail Restart (PFR); Teletype 33 ASR interface; Real-Time Clock (0.1, 1.0, and 10.0 kHz) with two interrupts; autoload ROM (programmed for paper tape reader, Teletype, cassette, magnetic tape, or disc); and an EIA RS232 CRT interface that can be added to the Teletype interface. In addition there is a Basic Variables option (a prerequisite for certain others) which includes offset of processor interrupts, enabling power fail interrupt, and sense register jumpering for operation without console. DMA is a standard feature. Processor options are mounted "piggy back" on the processor board instead of on a separate card, so they must be factory-installed.

The minimum LSI-2 processor is contained on one board with memory on another, leaving three slots for additions. Each expansion chassis adds five slots to the system. System size is limited by the maximum memory size (up to 256K words with the Memory Bank Control option), and by the maximum number of peripherals that can be addressed (up to 256 individual device controllers) and handled by the system software. Peripheral offerings are summarized in Table 2.

Table 2. CAI Peripherals

Model No.	Description
Discs	
18530-43	Moving Head Disc Subsystem, 1 fixed, 1 removable cartridge, 2.46M wds/drive, 4 drives/controller
18566	Floppy disc; 243K bytes/disc, dual drive, 2 dual drives/controller
Terminals	
22205-00	Teletype ASR 33-20/3JC, 10 cps
22230-00	A/N Display, 1920 chars, 24x80 char, 64-char set, to 9600 baud
Punched Cards	
18223-43	285-cpm reader
Paper Tape	
18223-12	300 cps reader
18223-61	300 cps reader, 75 cps punch
Printers	
18223-31	100 cps printer (60-150 lpm), 80 col
Magnetic Tape	
18224-15	9-track, 800 bpi, 25 ips, 4 drives/controller
18240-01/02	Single/Dual cassette drives, 520K bytes/cassette, 4 drives/controller
Process I/O	
13213-00	Digital I/O, 16-bit DTL/TTL-compatible
13214-00	Relay Output Module; 32-bit (1x32, 2x16 or 4x8)
13215-00	Relay Input Module; 32-bit (1x32, 2x16 or 4x8)
13216-00	Output Module, 64-bit (1x64, 2x32, 4x16 or 8x8)
14223	Utility I/O, 8- or 12-bit parallel input or output
Communications	
14236	Single or Dual Interface for 1 or 2 EIA RS232-compatible CRTs or leased line modems
14535	Async Programmable Modem Controller, 1 line to 9600 baud
14512	Async Programmable Modem MUX, for 2 or 4 lines
14513	Sync Programmable Modem Controller, to 50K baud
14523	Automatic Calling Unit MUX for 1-4 ACUs.

Computer Automation supplies four packaged Alpha LSI-2 configurations that are less expensive than the total of all components. These four configurations are available on short delivery.

- 30010-16 Standard DOS — CPU, 16K words of core memory, all processor options except RS232 interface, disc (2.46 million words), printer, paper tape reader/punch, Teletype ASR 33 expansion chassis and power supply, and DOS software.
- 30010-32 Expanded DOS — same as 30010-16 but with a total of 32K words of core memory.
- 30020-16 Standard MTOS — CPU, 16K words of core memory, and all processor options except RS232 interface; dual magnetic tape system (two 9-track drives); printer; Teletype ASR 33; paper tape reader/punch; and MTOS software.
- 30020-32 Expanded MTOS — same as 30030-16 but with 32K words of core memory, expansion chassis, and second power supply.

Minimum configurations required by the various software packages are summarized in Table 3.

Table 3. Naked Mini/Alpha LSI: Software

Package	Description
Real-Time Executive (RTX)	Modular system consisting of multitasking executive (RTX nucleus), I/O executive (IOX) subsystem; communications executive (COMX), RTX nucleus, requires 650 wds of memory, console
Disc Operating System (DOS)	For control of sequential job operations; with system secondary storage on disc; requires 16K wds of memory, disc, Teletype, real-time clock, printer, paper tape I/O
Magnetic Tape Operating System (MTOS)	Functionally equivalent to DOS, but with secondary storage on computer tape; requires 16K words of memory, Teletype, magnetic tape drive, real-time clock, printer, paper tape I/O
Cassette Operating System (COS)	Functionally equivalent to DOS, Teletype, cassette drive
BETA Assembler (2 versions)	Relocatable; one version requires 4K words of memory; another (8K) version supports unit record I/O with intermediate mass storage
OMEGA Conversation Assembler	Adds on-line editing, updating, conversational capabilities to BETA
360 Cross Assembler (XASM)	Written in IBM FORTRAN IV Level G; produces output identical to BETA and OMEGA
Advanced BASIC	Dartmouth BASIC with nested recursive subroutines, calculator mode, and other extensions; requires 4K words of memory
Extended BASIC	Advanced BASIC with string manipulation and matrix instructions; requires 8K words of memory
Extended Multiple User BASIC	Same as Extended BASIC, but for 8 users
FORTRAN	ANSI Basic FORTRAN, but with a number of added features; requires 4K words of memory
FORTRAN IV	ANSI FORTRAN IV, but with added features; stresses compact object code; requires 16K words to compile, 8K words to run
File Manager	Program storage and retrieval for small memories; 4K words of memory plus disc, magnetic tape, or cassette unit
Utilities	Source tape preparation; loader, TTY/CRT utility, math packages, diagnostics

COMPATIBILITY

The Alpha/Naked Mini computers are upward compatible, moving up from slow to fast series. The older 16 Series are the slowest, with a 1,600-nanosecond cycle and a set of 152 instructions. The LSI-1 Series is next in the hierarchy, with a 1,200-nanosecond processor cycle time and 168 instructions. The LSI-2 Series is the top of the line, with a 150-nanosecond processor cycle time and 188 instructions; this series is bound by its memory cycle time which can be 960, 1,200 or 1,600 nanoseconds. Each instruction set is a superset of the previous set, allowing complete upward compatibility. With the exception of the disc drives, peripherals can also be moved up.

MAINTENANCE

Computer Automation sells only to OEM manufacturers, and hence does not provide the type of on-site preventative and emergency maintenance contracts usually associated with end-users. The company has a 1-year warranty, however. Components that break down are immediately replaced or repaired free of charge during the first 30 days. After that, parts are repaired at the factory; while waiting the user has access to "loaned" components (20 percent of purchase price).

TYPICAL PRICES

Model Number	Description	Purchase $
30010-16	Standard Disc Operating System (DOS) includes ALPHA/LSI-2/20 Computer, 16K words (16 bits) core memory; Power Fail/Restart option; Basic Variable/ Real Time Clock/Teletype Interface/Autoload options; Disc system with 4.92 million bytes of storage; Line Printer system; High Speed Paper Tape Reader/Punch system; Teletype ASR 33; Expansion chassis; Second power supply; Matching enclosure (19 inch rack); DOS Disc Operating System software (includes paper tape library); DOS software supplied on Disc Cartridge	26,900
-32	Expanded DOS Standard DOS plus 16K words of core	29,100
30010-18	Extended DOS (A) 30010-16 plus Card Reader System	30,650
-34	Extended DOS (B) 30010-32 plus Card Reader System	32,850
	Processors	
	NAKED MINI LSI-2/20 includes 2 modules; chassis, motherboard and fans; CPU consists of a single module with options contained on a piggy-back unit; memory is on separate board. Does not include power supply or control console	
10440-08	With 8K 16-bit words of Core 1600 memory	2,595
10450-04	With 4K 16-bit words of Core 980 memory	2,300
-08	With 8K 16-bit words of Core 980 memory	2,695
10460-16	With 16K 16-bit words of Core 1200 memory	3,875
	The ALPHA LSI-2/20 T includes a processor; chassis; power supply; operator's console	
10540-28	With 8K 16-bit words of Core 1600 memory	3,060
10550-24	With 4K 16-bit words of Core 980 memory	2,765
-28	With 8K 16-bit words of Core 980 memory	3,160
10560-36	With 16K 16-bit words of Core 1200 memory	4,340
	ALPHA LSI-2/20G is same as LSI-2/20T except includes programmer's console	
10540-08	With 8K 16-bit words of Core 1600 memory	3,160
10550-04	With 4K 16-bit words of Core 980 memory	2,865
-08	With 8K 16-bit words of Core 980 memory	3,260
10560-16	With 16K 16-bit words of Core 1200 memory	4,440
	NAKED MINI LSI-2/10 same as 2/20 but does not include motherboard and power supply	
10640-04	With 4K 16-bit words of Core 980 memory (980 nsec)	1,750
-08	With 8K 16-bit words of Core memory (980 nsec)	2,120
10660-16	With 16K 16-bit words of Core memory (1,200 nsec)	3,300
	ALPHA LSI-2/10	
10740-24	With 4K 16-bit words of Core memory (980 nsec)	2,440
-28	With 8K 16-bit words of Core memory (980 nsec)	2,810
10760-36	With 16K 16-bit words of Core 1200 memory	3,990
	OSC ALPHA LSI-2/10T except includes programmer's console	
10740-04	With 4K 16-bit words of Core memory (980 nsec)	2,540
-08	With 8K 16-bit words of Core memory (980 nsec)	2,910
10760-16	With 16K 16-bit words of Core memory (1,200 nsec)	4,090
	NAKED MINI/LSI-1 (includes single module with options contained on a piggy-back unit)	
10110-01	With 1K 16-bit words of integral SC1600 memory	985
-02	With 2K 16-bit words of integral SC1600 memory	1,125
10120-04	With 4K 16-bit words of integral Core 1600 memory	1,650
-08	With 8K 16-bit words of integral Core 1600 memory	2,020
	The ALPHA/LSI-1 T includes processor; chassis w/power supply; operator's console	

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $
10210-21	With 1K 16-bit words of integral SC1600 memory	1,730
-22	With 2K 16-bit words of integral SC1600 memory	1,865
10220-24	With 4K 16-bit words of integral Core 1600 memory	2,390
-28	With 8K 16-bit words of integral Core 1600 memory	2,760
	The ALPHA/LSI-1G same as LSI-1T except includes programmer's console. The CPU contained on a single module; options contained on piggyback module	
10210-01	With 1K 16-bit words of integral SC1600 memory	1,830
-02	With 2K 16-bit words of integral SC1600 memory	1,965
10220-04	With 4K 16-bit words of integral Core 1600 memory	2,490
10220-08	With 8K 16-bit words of integral Core 1600 memory	2,860
	NAKED MINI LSI-2/10 consists of 2 modules only	
10690-50	With 1K RAM only	1,200
-60	With 2K RAM only	1,475
-52	With 1K RAM, 2K PROM	2,340
-54	With 1K RAM, 4K PROM	3,260
-62	With 2K RAM, 2K PROM	2,640
-64	With 2K RAM, 4K PROM	3,560
-56	With 1K RAM, 2K ROM	1,495
-57	With 1K RAM, 4K ROM	1,610
-58	With 1K RAM, 8K ROM	1,830
-66	With 2K RAM, 2K ROM	1,795
-67	With 2K RAM, 4K ROM	1,910
-68	With 2K RAM, 8K ROM	2,130
	Processor Options (no slots required)	
12500-00	Power Fail Restart (PFR)	250
12500-01	Automatic Start-up	150
12505-01	Basic Variables	95
-02	Teletype Interface (TTI) for modified ASR 33	100
-04	Real Time Clock (RTC)	225
-08	Autoload (AL) (uses bootstrap and binary loader)	175
12505-16	EIA RS232 Interface	75
-15	Basic Variables, TTY Interface, Real Time Clock, and Autoload	545
-31	BV/TTI/RTC/AL/EIA	620
	Memories	
	Add-on semiconductor memories operate at 1,600 nsec full cycle time, 16-bit words	
11530-50	SCM module, 1K RAM only	745
11530-60	2K RAM only	1,095
11530-52	SCM module, 1K RAM, 2K PROM	1,640
11530-54	1K RAM, 4K PROM	2,550
11530-62	SCM module, 2K RAM, 2K PROM	1,940
11530-64	2K RAM, 4K PROM	2,860
11530-56	SCM module, 1K RAM, 2K ROM	845
11530-57	1K RAM, 4K ROM	960
11530-58	1K RAM, 8K ROM	1,180
11530-66	SCM module, 2K RAM, 2K ROM	1,145
11530-67	2K RAM, 4K ROM	1,260
11530-68	2K RAM, 8K ROM	1,480
	Core Memories	
11540-08	Module 8K, 16-bit words, 1,600 ns cycle	1,800
11550-08	Module 8K, 16-bit words, 980 ns cycle	1,950
11560-16	Module 16K, 16-bit words, 1,200 ns cycle	3,050
12542-00	Memory Bank Control for memory larger than 32K (not available with SCM)	900
	Power Back-up for Memories	
12099-00	On-Card Data Retention Option	42
	MASS STORAGE	
	Moving Head Discs	
16530-43	Moving Head Disc System (includes single disc drive with 1 removable and 1 fixed disc)	13,200
22530-43	Additional Moving Head Disc Drive	11,085
	INPUT/OUTPUT	
	Teletype/CRT Terminals	
22205-00	Teletype (modified ASR 33)	1,650
22215-00	Modification Kit for Standard TTY	90
22230-00	Keyboard-Display Terminal	3,175
	Punched Card	
18223-43	Card Reader System	4,585
	Paper Tape	
18223-12	High-Speed Paper Tape Reader System	2,745
18223-61	High-Speed Paper Tape Reader/Punch System	6,610
	Line Printers	
18223-31	Line Printer System	6,525
	Magnetic Tapes	
18224-15	Magnetic Tape System (includes controller/interface for up to 4 mag tape transports)	8,275
22224-15	Additional 25 ips Magnetic Tape Transport	4,500
	Digital Cassettes	
18240-01	Single Digital Cassette System	2,850
-02	Dual Digital Cassette System	4,550
22240-02	Additional Dual Digital Cassette Drive	3,975
	General-Purpose I/O Interfaces	
	All interfaces include control and sense lines, and interrupts plus a mating connector and documentation	
13213-00	Digital I/O Module	500
13214-00	Relay Output Module	750
13215-00	Relay Input Module	750
13216-00	Output Module	500
13219-00	Input Module	500
13220-00	16-Channel Priority interrupt	500
13222-00	I/O Driver Module	500
14223-00	Utility I/O Interface	600
14511-00	I/O Terminator Board	125
	DATA COMMUNICATIONS	
	The x in model number designates the below:	
	x = 1, 110 baud	
	x = 2, 150 baud	
	x = 3, 300 baud	
	x = 4, 600 baud	
	x = 5, 1,200 baud	
	x = 6, 1,800 baud	
	x = 7, 2,400 baud	
	x = 8, 4,800 baud	
	x = 9, 9,600 baud	
	Prerequisite for all interfaces is 10xxx-xx	
14236-1x	Dual interface for 2 CRTs or leased line modems	575
-21	Dual Interface for 2 TTY ASR 33x	500
-5x	EIA RS232 Interface	600
14535-0x	Asynchronous Modem Controller (control and interface for 1 async line: point-to-point, multipoint, or direct dial	
-01	Async Modem Controller (with EIA interface; full data set controls)	600
-02	Async Modem Controller (with current loop interface; data only)	575
14512-xx	Async Modem Multiplexor (control and interface for 2 or 4 independent async lines)	
-21	Async Modem Multiplexor (for 2 EIA lines; full data set controls)	950
-22	Async Modem Multiplexor (for 2 current loop lines; data only)	850
-41	Async Modem Multiplexor (for 4 EIA lines; full data set controls)	1,400
-42	Async Modem Multiplexor (for 4 current loop lines; data only)	1,200
14513-00	Synchronous Modem Controller	1,200
-01	Sync Modem Controller with Internal Clock option	1,400
14523-0x	Automatic Calling Unit (ACU) Multiplexor (interface for up to 4 Model 801 (ACU) or equivalent)	
14523-02	ACU Multiplexor for 2 ACUs	800
-04	ACU Multiplexor for 4 ACUs	1,200

Notes:

(1) No systems are available for rent.

(2) Sold exclusively OEM. Minimum Naked Mini/LSI Processor order is five systems. Single Unit Alpha/LSI orders are taken. Quantity discounts are available for processors, options, memories, and other units designed and manufactured by Computer Automation, Inc. Two discount schedules are available, depending on volume. Discounts vary from 2.5% to 30% depending on production costs and volume. Discounts beyond 30% are for 200 or more units and require a home office quote. Peripheral devices are not discounted.

(3) Maintenance provided through the company selling the end-user product. CAI provides training for their maintenance personnel.

HEADQUARTERS

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COMPUTER AUTOMATION
LSI-2/60 MEGABYTER®

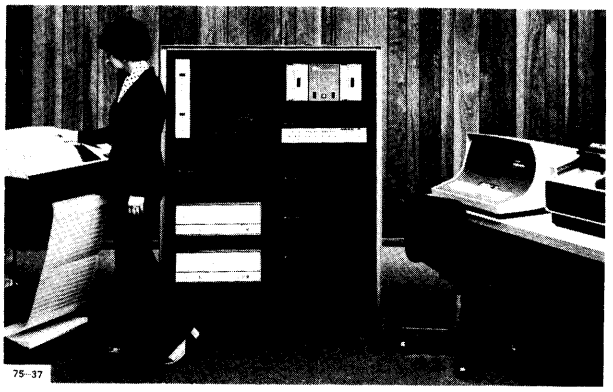

Figure 1. CAI LSI-2/60 Megabyter

OVERVIEW

Computer Automation announced the LSI-2/60 MEGABYTER on January 16, 1975, as part of an overall expansion of its existing product line. The MEGABYTER extends the capabilities of the LSI-2 line upward by adding instructions optimized for real-time, multiprogramming, communications, and business applications, and by expanding memory capacity to 1 million bytes in 32K-word memory banks. Since MEGABYTER uses the same architecture as the rest of the LSI-2 line, it can use all the peripherals and software developed for other members of the line. The MEGABYTER was announced along with two other offerings that enhance its capabilities:

- A new optimizing FORTRAN IV compiler that generates highly compact object code.
- A Distributed Input/Output System consisting of a half-board I/O Distributor that can handle eight "intelligent" cables controlled by PicoProcessors® ; these programmable interfaces let users simplify interfacing to any serial or parallel I/O device. The LSI-3/05 NAKED MILLI, a computer-on-a-board, was also announced; it extends the product line downward to compete with board-level microcomputers.

The LSI-2/60 MEGABYTER uses the same LSI-2 processor as the other members of the LSI-2 family: the 2/10 with 1,200-nanosecond memory and the 2/20 with 960-nanosecond memory. The register complement, interrupt and I/O schemes, word-or-byte modes of operation, and addressing modes are the same for all models. The LSI-2/60 implements the following facilities in addition to those available for the LSI-2/10 and 2/20:

- Expansion of the 2/20's stack processing capabilities.
- String instructions that can move up to 255 bytes at a time, can compare strings, and can move mismatched characters.
- Decimal arithmetic for adding and subtracting up to 31 digit strings.
- Bit manipulation; direct addressing to the bit level.

CRC character generation, hardware multiply/divide, and interleaved memory are standard features. Table 1 lists system specifications.

Software for the LSI-2/60 MEGABYTER includes DOS, COS, and MOS batch operating systems, BASIC, ALGOL, FORTRAN IV, and Assembly language processors. A Real-Time Executive (RTX) allows multiprogramming. An optimized version of the FORTRAN IV compiler, designed to produce more compact object code, was introduced at the same time as the MEGABYTER.

Peripherals include discs, diskette, magnetic tape, printers, card reader, paper tape reader and punch, process I/O, and communications. The new Distributed I/O Interface can support up to eight intelligent cables, which can connect to a variety of peripherals. Table 2 describes the MEGABYTER peripherals.

The I/O Distributor is an option for the entire LSI product line. It supports eight intelligent cables. A microprogrammed PicoProcessor at the end of each cable translates unique peripheral interface characteristics into standardized three-state bus signals. The PicoProcessor also generates and checks parity. Three PicoProcessors are available: one for parallel TTL devices and two for current loop or EIA serial interfaces.

The I/O Distributor buffers and transfers data between the I/O bus and the PicoProcessor cables, and provides interrupt priority control for two interrupts per cable. The standard I/O Distributor operates in DMA mode with word/byte count and current address counter in memory instead of in controller hardware. The Serial Feature provides clocks for "strap selectable"

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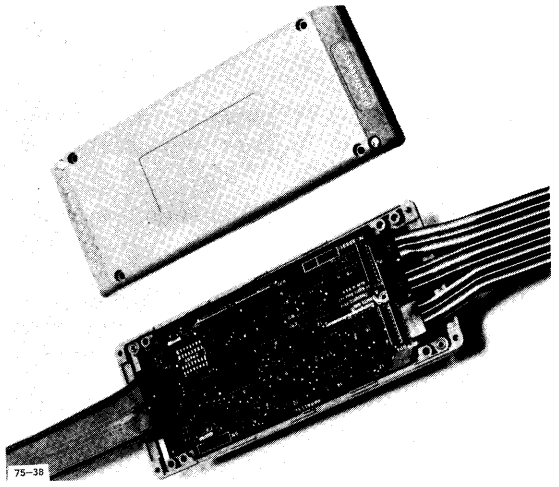

Figure 2. CAI Intelligent Cable

baud rates of from 75 to 19,200 baud; each of the eight channels can operate at a different rate if desired.

The MEGABYTER ranges in price from $9,600 for a basic 32K-byte configuration to around $110,000 for a million-byte version. Power fail/auto restart, auto load, and real-time clocks are options, as are special "jumbo" and expansion chassis. Volume discounts are available.

Computer Automation was formed in August 1967 to manufacture and market minicomputers to the OEM market. Since its introduction of the Alpha and Naked Mini Series, and the later LSI versions, the company has shipped more than 5,500 systems. It also produces and markets the Capable Tester System; this computer-driven production line tester for digital logic modules was originally designed for its in-house logic production facility. Computer Automation has expanded steadily and now has 18 direct sales offices and service facilities in the United States. A number of distributors market this system in other parts of the world; D. C. Industries in Australia; the Metric companies (Scandia Metric AB in Sweden, Finn Metric oy in Finland, SC Metric A/S in Denmark, and Metric A. S. in Norway) in the Scandinavian countries; Geveke Elektronica en Automatie nv in Belgium, Netherlands, Luxembourg, and Germany; Data Care AG in Switzerland; Tranchant Electronique in France; Computer Advances in South Africa; Alfatronica in Spain; and Electro Marketing in Japan. Computer Automation has its own subsidiary, CAI Ltd, in England for sales to the United Kingdom and for support in certain parts of Europe.

Addition of the NAKED MILLI and the MEGABYTER systems expands the market for the

Table 1. CAI LSI-2/60 MEGABYTER: Mainframe Specifications

Identity	Characteristics
CENTRAL PROCESSOR	
Microprogrammer	Yes
General-Purpose Registers	8
Addressing	
Direct (wds, bytes, or bits)	768
Indirect words	Multilevel
Indexed	Yes
Mapping	No
Instruction Set	
Number	224
Floating point	No
Priority Interrupt	
Levels (std; max)	5-256
MAIN STORAGE	
Type	Core, semiconductor
Cycle Time (nsec)	980, 1,200
Basic Addressable Unit	Word or byte
Min Capacity (bytes)	32,768
Max Capacity (bytes)	1,048,576
Increment Sizes (bytes)	8K, 16K, 32K (core); 1K, 2K, 4K, 8K (MOS)
Memory Parity	Option
Memory Protect	No
INPUT/OUTPUT	
Max Addressable I/O Devices	248
Conditional I/O	Std
DMA (no. of channels)	2-64
Max Transfer Rate	
DMA (wds or bytes/sec)	625,000
Block I/O (wds/sec)	131,579
Programmed (wds or bytes/sec)	34,247
Direct memory channels (wds or bytes/sec)	26,738

Naked Mini LSI/Alpha LSI line at both the top and the bottom. Naked Mini/LSI refers to Alpha/LSI systems without a chassis and interfacing hardware; conversely, Alpha LSI systems are packaged. The NAKED MILLI, as the name indicates, is offered in the "unpackaged" form only; the MEGABYTER is available both ways. The entire LSI line now consists of three processors: the LSI-1 (an MOS processor not yet delivered), the LSI-2 (Models 2/10, 2/20, and the Model 2/60), and the LSI-3/05 NAKED MILLI. The wide range of this compatible line should enhance all its members because OEM manufacturers can move up when they need to expand system capabilities.

PERFORMANCE AND COMPETITIVE POSITION

The LSI-2/60 MEGABYTER expands the LSI-2 line upwards; it provides an upward path for current customers and should also attract new customers on its own merit. The new instructions and the million-byte memory capacity make it suitable for large communications, data entry, real-time, or other multiprogramming systems

Table 2. CAI LSI-2/60 MEGABYTER: Peripherals

Model Numbers	Description
Discs	
18530-43	Moving-head disc subsystem, 1 fixed, 1 removable cartridge, 2.46M wds/drive, 4 drives/controller
NA	Floppy disc, 1.2 Mbytes, 4 drives/controller
Terminals	
22205-00	Teletype ASR 33-20/3JC, 10 cps
22230-00	A/N display, 1,920 char, 24 x 80 char, 64-char set, to 9,600 baud
Punched Cards	
18223-43	285-cpm reader
Paper Tape	
18223-12	300-cps reader
18223-61	300-cps reader, 75-cps punch
Printers	
18223-31	100-cps printer (60-150 lpm), 80 cols
Magnetic Tape	
18224-15	9-track, 800 bpi, 25 ips, 4 drives/controller
18240-01/02	Single/dual cassette drives, 520K bytes/cassette, 4 drives/controller
Process I/O	
13213-00	Digital I/O, 16-bit DTL/TTL-compatible
13214-00	Relay output module; 32-bit (1 x 32, 2 x 16, or 4 x 8)
13215-00	Relay input module; 32-bit (1x32, 2x16, or 4x8)
13216-00	Output module, 64-bit (1x64, 2x32, 4x16, or 8x8)
14223	Utility I/O, 8- or 12-bit parallel input or output
Communications	
14236	Single or dual interface for 1 or 2 EIA RS232-compatible CRTs or leased line modems
14535	Asynchronous programmable modem controller, 1 line, to 9,600 baud
14512	Asynchronous programmable modem MUX, for 2 or 4 lines
14513 S	Synchronous programmable modem controller, to 50K baud
14523	Automatic Calling Unit MUX for 1-4 ACUs

capable of considerable expansion. The range in the instruction set, I/O structure, and memory capacity allow it to compete with the Digital's PDP-11/45, Data General ECLIPSE and Interdata 7/32 and 8/32. These companies sell their systems in OEM as well as end-user versions.

The MEGABYTER does not perform memory mapping; instead, programs execute out of a 32K-word memory bank. An instruction is used to switch from one bank to another. Memory protect and hardware floating-point arithmetic are currently unavailable. The Universal Interface should save many OEM manufacturers considerable time and money in system building. The MEGABYTER is particularly suited to control multiterminal distributed processing systems for data entry, accounting, and text editing.

Computer Automation has a competitive advantage over minicomputer manufacturers who sell to end users and in the OEM market. A Computer Automation sells only OEM, and system builders are not concerned about the company becoming a competitor. Also, Computer Automation stresses thorough testing of system components, as well as reliability in meeting production deadlines and living up to contractual obligations.

Although Computer Automation entered the field only 7 years ago, the company grew rapidly until last year when its steady growth rate was slowed somewhat due to the unfavorable economic climate. Expansion of its product line at both ends and the new I/O interfacing should provide other markets for CAI systems, and spur its return to previous growth levels.

MAINTENANCE

Since Computer Automation sells only to OEM manufacturers, it does not provide the type of on-site preventive and emergency maintenance contracts usually associated with end users. The company does offer a 1-year warranty. Components that break down are immediately replaced or repaired free of charge during the first 30 days. After that, parts are repaired at the factory, while the user has access to "loaned" components (20 percent of purchase price) during the repair period.

HEADQUARTERS

Computer Automation, Inc.
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CONTROL DATA CORPORATION

System 17 Series

OVERVIEW

The CDC System 17 is a minicomputer which can be applied to many application areas including industrial control, data acquisition, hospital/medical, optical character recognition, digigraphics, communications, terminal, amusement and recreation, data entry, and supervisory control. Its primary orientation as a system is towards industry, however; the system was announced in Troy, Michigan, which is just outside of Detroit. CDC has been courting major automobile manufacturers for large orders of the minicomputers.

Three items are of significance to users considering the System 17. First, the system is based heavily upon the earlier CDC 1700 series of minicomputers; it is program-compatible with the 1700 but optional channel adapters are required to interface 1700 peripherals to System 17. Because of this heritage, applications program developed over the last eight years are immediately available to a prospective user. (Users feel that CDC has one of the largest software libraries available for minicomputers.) Second, the System 17 uses new technology consisting of a new processor, all MOS/LSI semiconductor memory, and new peripherals scaled to minicomputer dimensions. Most significant of all, the total System 17 package offers a better price/performance ratio than previously offered by the 1700 line.

An item of interest is CDC's 2-year old policy of offering user-oriented hardware/software applications packages. This policy is reflected in the extreme modularity of the System 17. The policy is company-wide for CDC computers: CDC's new general-purpose computers (the Cyber 170 Series) are also oriented towards applications and away from strictly hardware considerations.

The 1700 series upon which the System 17 is based represented CDC's early recognition of the need for a relatively small computer for real-time applications. The 1704 was first delivered in 1966. It was followed in 1969 by the less expensive, slower 1774. In 1972, the memory capacity of the line was extended from 32K to 64K words when the 1714 was first delivered. Over 750 installations of CDC 1700 systems are currently operating; CDC has made no push to move 1700 users over to the System 17. The 1700 line, however, went out of production in September 1973. The System 17 then can be viewed both as an extension of the long-lived 1700 line of minicomputers and as the beginning of a new System 17 line.

The first System 17s were delivered in the fourth quarter of 1973. There are currently more than 30 installations (November 1974), with around 200 orders backlogged. Originally, plans called for the System 17 to be manufactured exclusively in Israel, but unsettled conditions there caused CDC to begin manufacturing in the United States also. Although initial deliveries were delayed, CDC is now delivering 25 to 35 systems per month.

Two models of the System 17 are available; both use the same processor (1784) which features a 900-nanosecond memory cycle time for the 1784-1 and a 600-nanosecond memory cycle time for the 1784-2. Both models use MOS/LSI semiconductor memory and include an integral 4K-word memory module. Additional memory is available in 4K-word modules and varies in total size from 4K to 64K-words. Because memory is volatile, an optional standby battery can be mounted in the CPU mainframe to supply power to memory in case of main power supply failure.

System 17 uses an 18-bit word with 16 data bits (two bytes), one parity bit, and one memory protect bit. Parity checking is standard; other standard features include hardware multiply and divide, 16 priority interrupts and two data channels — programmed I/O and DMA, which CDC calls DSA, or "direct storage access."

The maximum I/O rate over DMA is 1.1 million words per second for the 1784-1 and 1.6 million words per second for the 1784-2.

Intercomputer couplers are available to allow the System 17 to communicate with and share peripherals with other System 17s or CDC 1700 systems; to operate as a front end for the CDC 3000, CDC 6000, Cyber 70 and Cyber 170 computer systems; and to interface as a remote processor. Table 1 summarizes mainframe characteristics.

The new peripherals introduced with the System 17 include cartridge disc and magnetic tape subsystems, two line printers, desktop card reader, conversational display terminal, and teletypewriter. Table 2 lists all the peripherals currently available with the system.

Software for the System 17 is the same as that developed over the years for the 1700 systems. Real-time

Table 1. CDC System 17: Mainframe Characteristics

Feature/Characteristic	
Central Processor	1784-1 1784-2
Microprogramming	No
Control Memory	None
No. of Internal Registers	2 accs; 2 index
Addressing	
Direct (no. of words)	256
Indirect	Yes
Indexed	Yes
Instruction Set	Hardware/subroutine
Number	196
Decimal Arithmetic	No
Floating-Point Arithmetic	Subroutine (std); hardware (opt)
User-Microprogramming	No
Priority Interrupt System Levels	16
Main Storage	
Type	MOS/LSI
Cycle Time (μsec)	0.900 (1784-1); 0.600 (1784-2)
Basic Addressable Unit	1 wd
Bytes/Access	2
Cache Memory	None
Min Capacity (bytes)	8,192 (std)
Increment Size (bytes)	8,192
Error Checks	Parity
Protection Method	Manual switches
ROM	No
I/O Channels	
Programmed I/O	Yes (called AQ)
A/Q Channel Expansion	1785-1
DMA Channels	Yes (called DSA) 1 std; 1 opt
DSA Channel Expansion	1785-2
Multiplexed I/O	No
1700 Channel Adapters	
1700 AQ Channel Adapter	1785-3
1700 DSA Channel Adapter	1785-4
Max Transfer Rate	
Within Memory	278K wds/sec (1784-1); 417K wds/sec (1784-2)
Over DMA (DSA)	1.1M wds/sec (1784-1); 1.6M wds/sec (1784-2)
Simultaneous Operations	Function of I/O control program technique & peak data rates of devices involved
Intercomputer Couplers	
Coupling Data Channel	1716
Satellite Coupler	1718

Table 2. CDC System 17: Peripherals

Class/Device	Performance Characteristics
Magnetic Discs	
853* Disc Storage Drive	1.5M wds/disc, 8 drives/cntrl
854* Disc Storage Drive	3.1M wds/disc, 8 drives/cntrl

Table 2. (cont.)

Cartridge Discs	
1739-1* Disc and Controller	1.1M wds fixed, 1.1M wds removable; 8 contrs/ch
856-2 Drive	1.1M wds fixed, 1.1M wds removable; 4 drives/cont requires 1733-2 control
856-4 Drive	Same as 856-2 but 2.2M wds/disc
Drums	
1752* Drum and Controller	196K to 1.5M wds; 8.7 msec avg access
Magnetic Tape	
608* Magnetic Tape Transport	7-trk, 200, 556, or 800 bpi; requires 1732 cntrl
609* Magnetic Tape Transport	9-trk, 800 bpi; requires 1732 cntrl
615-73 Magnetic Tape Transport	7-trk, 556 or 800 bpi
615-93 Magnetic Tape Transport	9-trk, 800 or 1,600 bpi
Punched Card	
405* Reader	1,200 cpm (80-col), 1,600 cpm (51-col); requires 1726-1 cntrl
1729-2* Reader	330 cpm (80-col); requires 1726-1 cntrl
1729-3 Reader	300 cpm (80-col); requires 1726-1 cntrl
415 Punch	250 cpm; requires 1728 cntrl
430* Reader/Punch	500 cpm read; 100 cpm punch (80 col); requires 1728 cntrl
Line Printer	
501 Printer	1,000 lpm; requires 1740 cntrl
1742 Printer	300 lpm
1742-30 Printer	300 lpm
1742-120 Printer	1,200 lpm
Paper Tape	
1721* Reader	400 cps
1723* Punch	120 cps
Paper Tape Reader/ Punches	
1777-1* Read/Punch	400 cps read, 150 cps punch
1777-2* Read/Punch	400 cps read, 150 cps punch
Teletype	
1711 35 KSR	10 cps
1713 35 ASR	10 cps, includes PT reader
CRT	
713-10 CRT Console	Display 10-x 8-in.; 16 lines & printer opt
274 Digigraphic Console	8 Control/ch; 22-in. screen
Communications	
1717-1 Single Line Data Set Controller	Duplex to 40,800 baud
1747 Single Line Data Set Controller	Half-duplex to 60,800 baud
364/45* Communications Multiplexors	

Note:
*CDC 1700 peripherals.

operating systems are available for paper tape, magnetic tape, or mass storage; FORTRAN, AUTRAN, Assemblers, DRAFT, and BASIC languages are available, as well as many applications packages for data acquisition, communications, data entry, engineering, graphics, process control, OCR, and scientific research. Table 3 outlines the System 17's software.

Table 3. CDC System 17: Software Systems

Characteristic	4K Assembly System	Utility System	Mass Storage Operating System
Assembler	Assembler	Assembler or Macro Assembler	Macro Assembler
Compiler	None	Tape FORTRAN	Mass Storage FORTRAN
Mass Storage Required	No	No	Yes
Minimum Configuration Required	4,096 wds	8,192 wds*	12,288 wds*
Core Storage Occupied by Resident Portion	750 wds	2,250 wds	8,673 wds (largest overlay)
Execute Batch Programs	Yes	Yes	Yes
Execute Control Programs	No	No	Yes
Multiprogramming	No	No	Yes
Program Library	No	Yes	Yes

Note:
*If the FORTRAN compiler is used, additional 4K words of core storage are required.

PERFORMANCE AND COMPETITIVE POSITION

The System 17 places CDC in the best position it has been in for several years in the minicomputer market. Although CDC early recognized the need for real-time small computers and produced the 1700 line for that market, the company never followed up by developing minicomputer-sized peripherals for the 1700 line. CDC interfaced a broad range of peripherals to the 1700, but they were generally the same peripherals CDC offered with its large computers and they were expensive. As minicomputer processor prices fell, it became apparent that minicomputers needed their own low-cost peripherals. Thus, the cost of peripherals for most minicomputer systems has dropped markedly in the past few years.

With the System 17, CDC has introduced minicomputer-sized peripherals: magnetic tape, cartridge disc, printers, conversational display, card reader, and teletypewriter. System 17 retains the really fine logic designed into the 1700 line, and it can run all the 1700 software developed over the last eight years. In addition, CDC has many years of experience in real-time processing and has an impressive number of systems operating for varied applications.

The System 17 will be competing with the DEC PDP-11/40 and /45, Data General Nova ECLIPSE line, Hewlett-Packard 21MX Series, Xerox System 530, and Honeywell System 700. System 17 can be a strong competitor if CDC takes its own claims seriously and does offer users service rather than hardware. Real-time systems tend to require tailoring to fit a specific application, and the strong competitors in this market must be prepared to perform applications engineering and programming for users. A large market exists for minicomputers like the System 17, and CDC should be able to produce a number of hardware/software System 17 application packages that will do well.

USER REACTIONS

Users contacted had previous experience with CDC systems, notably the 1700 Series. For them, the step to the 17 was a logical, orderly one; nevertheless, they first considered alternatives from other manufacturers.

Manufacturing

A manufacturer of chemicals and drugs obtained one of the first System 17s to use as a front end for its CDC 6400, with terminals connected to several real-time lab operations. This manufacturer already had a number of CDC 1700s in use in various capacities for process control. A competitive system closely examined was the DEC PDP-11. The System 17 was chosen because it had more software immediately useful to their purpose and it could be used to compile programs for the 1700s they already had. This manufacturer is now considering adding more System 17s for control applications.

The current front-end configuration includes a 1700 channel adapter, two tapes, two discs, CRT terminal, dot matrix printer, and 32K words of memory. The disc drives installed are 854 models; but this user is looking forward to CDC's new line of cartridge discs, which use an electronic seek mechanism that is more reliable than current electromechanical ones.

This user found no problems with program compatibility between the 1700 and System 17. As for maintenance, the 1700s have been quite reliable, and he expects the System 17 to be even easier to maintain. This user stressed the excellence of the 1700 operating system used also on the System 17. He noted that CDC has one of the largest software libraries for minicomputers.

Medical Systems

A medical systems house produces packages for admissions screening, intensive care, coronary care, operating

room functions, and the like. About five years ago, this company selected the 1700 as the basis for its medical hardware/software packages because it was one of the few proven systems with nationwide maintenance. Also, CDC had a good FORTRAN package to make programming easier.

Experience with the 1700 has borne out expectations. The evolution to the System 17 is a natural step because of the complete software compatibility, lower cost, and greater reliability of the new system.

CONFIGURATION GUIDE

A basic System 17 includes a processor (either 1784-1 or 1784-2) and 4K words of MOS/LSI semiconductor memory. Both processor submodels include 16 interrupts, two index registers, DSA, parity, memory protect, and hardware multiply/divide as standard features. The difference between the two models is in the memory cycle time: 900 nanoseconds for the 1784-1 and 600 nanoseconds for the 1784-2.

Two enclosures are available: the first is required and houses the CPU, 32K words of memory, the DSA and AQ channel, a memory hold battery (providing power for eight hours in case of main power failure), and AQ/DSA expansion. Each 4K-word memory module is mounted on one circuit board. Up to 36 circuit boards, plus power supply and cooling equipment, are also housed in the CPU enclosure. Optional features are integral controllers for magnetic tape transport, cartridge disc unit, line printer, card reader, teletypewriter, and conversational display terminal.

The second enclosure is required to add memory beyond 32K words. Full memory expansion to 64K words also requires a memory expansion module (1786-1).

Up to eight peripherals can connect to the DSA and AQ I/O channels. The 1785 channel expansion adapter is available in four models to expand the channel capacity.

- 1785-1 expands the AQ channel to handle up to eight additional devices.
- 1785-2 expands the DSA channel to handle up to eight additional devices.
- 1785-3 converts the AQ channel to the standard 1700 bus so the CDC 1700 programmed I/O devices can be connected to System 17.
- 1785-4 converts the DSA channel to the standard 1700 I/O bus so the CDC 1700 DSA devices can be connected to the System 17.

The System 17 can support all the peripherals designed specifically for it as well as peripherals available with the CDC 1700 line.

In addition, intercomputer couplers are available to interface it to the CDC 3000, CDC 6000, and Cyber 70 Series computers.

The System 17 is very modular and CDC offers dozens of application-oriented configurations.

COMPATIBILITY

The System 17 is program compatible with the CDC 1704, 1714, and 1774. An intercomputer adapter allows the System 17 to operate as a front end for the CDC 3000, CDC 6000, and Cyber 70 Series computers; to communicate with CDC 1700 systems; and to use the CDC 1700 peripherals. In addition, hybrid A/D configurations incorporate an EAI 680 analog computer as a system component.

MAINTENANCE AND SUPPORT

CDC provides 24-hour service centers in 42 metropolitan areas in the United States. Preventive maintenance is provided during primary maintenance period.

CDC provides training and education for customers at their Education Institutes. Other services include site planning, systems analysis, and consulting. FOCUS, the international Forum of Control Data Users formed in 1968, gives users opportunities to exchange ideas among themselves and CDC personnel. A special interest group has been formed for CDC 1700 users. A newsletter is published monthly to distribute information.

HEADQUARTERS

Control Data
P.O. Box 0
Minneapolis MN 55440

PRICE DATA

Model Number	Description	Monthly Rental $ 1-Yr	Monthly Rental $ 2/3 Yr	Purchase $	Monthly Maint. $
	CONTROL DATA SYSTEM 17				
	CENTRAL PROCESSORS AND WORKING STORAGE				
1784-1	Processor with 4K words of 18-bit MOS memory, 900 nsec	347	258	14,175	100
1784-2	Processor (same as 1784-1 except 600-nsec memory cycle time)	373	364	17,325	121
	Systems Options				
1785-1	AQ Channel Expansion	27	26	1,050	11
1785-2	DSA Channel Expansion	27	26	1,050	11
1785-3	1700 AQ Channel Adapter*	69	67	2,625	16
1785-4	1700 DSA Channel Adapter*	42	41	1,575	16
	Memory				
1782-1	Memory Module (900 nsec, 4,096 wds)	84	82	3,150	31
1782-2	Memory Module (600 nsec, 4,096 wds)	90	88	4,200	36
	MASS STORAGE				
	Cartridge Disc				
856-2	Cartridge Disc Drive (1.1M wds on fixed, 1.1M wds on removable discs)	200	195	9,450	57
856-4	Cartridge Disc Drive (same as 856-2 except has 2.2M wds/disc)	315	307	13,125	67
1733-2	Cartridge Disc Controller (single DMA channel connection; absolute cylinder addressing; daisy chain capability; controls up to 4 856-2 or 856-4 drives)	174	168	5,775	31
	INPUT/OUTPUT				
	Magnetic Tape				
615-73	Magnetic Tape Transport (7-track, NRZI; 556 or 800 bpi)	174	168	5,775	68
615-93	Magnetic Tape Transport (9-track, PE with 1,600 bpi or NRZI with 800 bpi)	189	184	7,350	79
	Punched Card				
1729-3	Card Reader and Controller (300 cpm)	179	171	6,300	78
	Line Printer				
1742-30	Line Printer and Controller (300 lpm; 64-char set)	389	378	17,850	200
1742-120	Line Printer and Controller (1,200 lpm; 48-char set)	1,533	1,495	52,500	300
	Terminals				
	TTY				
1711-4	33KSR	37	36	1,470	32
1711-5	35KSR	74	72	3,150	39
1713-4	33ASR	48	47	1,680	36
1713-5	35ASR	116	111	5,040	97
	CRT				
713-10	CRT Console	63	62	2,095	13
711-100	CRT Expanded Memory	11	–	336	11

**To connect CDC 1700 peripherals.*

DATA GENERAL

ECLIPSE®

OVERVIEW

The ECLIPSE® family of computers is Data General's most recent line of general-purpose minicomputers. ECLIPSE systems run the entire gamut of the Nova/Supernova line they replace, but they add a variety of features to increase speed and throughput; to enhance system reliability and error handling; and above all to expand system capabilities while maintaining compatibility with all Nova/Supernova models. With this line, Data General can compete more aggressively in its current markets and open up new ones. The extended processing power gives Data General's current customers a system to move up to.

The slower-speed (1 microsecond cycle) Nova 2 systems, announced in June 1973, overlapped all models of the Nova/Supernova line except the Nova 840 and the Supernova SC. The S/100 and S/200, the first two ECLIPSE computers, overlap these two systems as well as the rest of the Nova line. Nova 2s, however, are considerably cheaper for comparable configurations. Nova 2/4 is not available in single-unit quantities, however; it must be purchased in quantities of five units. The Nova 2/10 is available at the system level in single-unit quantities.

The ECLIPSE S/100 parallels the Nova 800, Nova 1200, and Supernova computer characteristics while the S/200 parallels the Nova 840 characteristics. Both the S/100 and S/200 outperform their predecessors and offer a superset of system enhancements: error checking and correcting (ERCC) memories composed of core or MOS semiconductor (SC) modules; 16-word bipolar cache memory on SC modules; up to 8-way interleaving of core memory modules, and up to 4-way interleaving of SC memory modules; superset of the Nova/Supernova instruction set to perform bit, byte, and word data manipulations and efficient context switching and stack operations; and optional Writeable Control Store for use-oriented microprogramming. The model 200 offers double user maps plus a data channel map in the mapping option to cut processor overhead in context switching. Table 1 summarizes system specifications.

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Table 1. Data General ECLIPSE: Mainframe Characteristics

MODELS	**S/100, S/200**
CENTRAL PROCESSOR	
Microprogrammed	Yes
Control Memory	ROM
No. of Registers	8 accs: 4 16-bit (2 also used as index regs) and 4 64-bit for fl. pt. arithmetic
Addressing No. of Wds	
Direct	To 64K bytes
Indirect	Multilevel
Indexed	Yes
Mapping	No (S/100; yes (S/200 to 256K bytes)
Overflow Entry	
Instruction Set	
Implementation	Firmware
Types	Single & doubleword
Number	86 std, 66 opt
Floating Point	Hardware option
Hardware Stack	Yes
Writable Control Store (256 56-bit words)	Opt, not software supported
Interrupts	
Levels	16 ext
Type	Hardware
MAIN STORAGE	
Type	MOS, core
Cycle Time, μsec	0.8 (core), 0.7 (MOS), 0.2 (cache)*
Basic Addressable Unit	Wd, byte
Bytes per Access	2
Cache Memory	MOS only
Capacity, bytes	
Min	16K (S/100), 32K (S/200)
Max	64K (S/100), 156K (S/200)
Increment Size, bytes	16K
Ports per Module	1
Error Checks	ERCC opt
Memory Protection	No (S/100); opt (S/200); dual user memory maps, 1 data channel mgs
Overflow Entry	
Memory Management	No (S/100); Yes (S/200)
Interleaving	Core; 8-way MOS 4-way
INPUT/OUTPUT	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate (MA2)	1,250K wds/sec

Note:

**Effective memory cycle time varies with type of memory and number of memory modules interleaved.*

Many of the ECLIPSE features enhance multiprogramming and multiprocessing in communications, text processing, and process control environments. Dual processors or up to 15 processors can attach to IBM systems while controlling 32 communication lines each; configurations are also available for front-end, message-switching, and network processing. Appropriate software support is provided for most options.

Initially, all software and peripherals for the ECLIPSE computers will be the same software and peripherals available for the Nova/Supernova. No new software has yet been developed to use the unique features of ECLIPSE to best advantage. Table 2 summarizes differences between ECLIPSE and Nova 2 Computers.

First deliveries of both the S/100 and S/200 are scheduled for February 1975.

COMPETITIVE POSITION

With its ECLIPSE Computer, Data General does not find itself in the same position vis-a-vis Digital Equipment's PDP-11 as it was in 1968 with its Nova vis-a-vis the PDP-8. At that time, Digital had no 16-bit computer. Data General capitalized on that fact and sold its 16-bit Nova aggressively and successfully in the OEM market against the 12-bit PDP-8. In 1970, Digital introduced the 16-bit PDP-11, which was new conceptually and architecturally. Digital "bit the bullet" on software because the PDP-11 was not compatible with any of its previous computers and all software had to be developed from scratch. In the meantime, Data General developed substantial system software for its Nova/Supernova line, added optional features, and developed the Nova 840, the true forerunner of the S/200. Until now, Data General has mostly sold the Nova/Supernova against the PDP-8, not the PDP-11. The PDP-11, however, has intruded more and more into PDP-8 territory. With the ECLIPSE, Data General is now tackling the PDP-11 as a competitor.

Two things are particularly significant about the ECLIPSE. First, it is upward compatible with the Nova/Supernova computers; thus the system has a substantial body of inherited software, and Data General is not faced with a massive system software development effort. Second, Data General has rejected the unified bus in favor of a distributed bus structure with the I/O bus separate from the memory bus. It appears Data General learned from Digital's experience. The PDP-11 suffered for a couple of years after its announcement because of its lack of software.

On another front, Data General has experienced some inroads into its own Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem, since the underestimating of demand meant that the company slipped behind schedule from

Table 2. Chief Differences Between ECLIPSE and Nova 2 Computers

COMPUTER MODEL	ECLIPSE S/100	ECLIPSE S/200	Nova 2 2/4	Nova 2 2/10
Packaging				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
MEMORY				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management				
Protect				
CAPABILITIES				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Std	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

Table 3. Comparison of Floating-Point Processor Execution Times in Microseconds

Operation	ECLIPSE (core memory 4-way interleaved)	PDP-11/45 (core memory)	PDP-11/50 (MOS memory)	IBM 370/158(1)
Load	2.8	4.8	3.4	–
Store	2.0	4.8	3.4	–
Add/Subtract	2.4	6.5	5.4	2.0
Multiply	3.9	8.2	7.1	2.0
Divide	4.6	9.9	8.8	8.6
Add/Subtract (long)	2.4	—	—	2.2
Multiply (long)	7.1	14.2	12.3	3.6
Divide (long)	7.8	17.5	15.4	23.2

Note:
(1) Times assume instruction is in buffer 90% of the time.

time to time, and impatient OEM customers bought from the smaller company. This threat was earlier counteracted by the Nova 2 line which is competitive in price and comparable in speed to the D-116.

Although Data General has compared their floating-point processor's instruction execution times with those of the IBM System/370 Model 158 (see Table 3), the real competition for the ECLIPSE system as a whole will be from systems supplied by the minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Interdata, MODCOMP, Varian Data Machines, Computer Automation, General Automation, and Microdata. All of these manufacturers except Computer Automation, which caters exclusively to the OEM market, produce a broad range of processing power in their computer lines. All have discovered gold in the midicomputer range, once sparsely populated and now getting congested, but none can supply the support required by a truly novice user. All supply system software, and the user must prepare the applications software.

The ECLIPSE extends the processing power of the Nova/Supernova line and gives Data General's customers a compatible system for upgrading. In addition, it retains the relatively new Nova 2 low end of the line for the OEM market. Initial comparison of the ECLIPSE floating-point processor execution times with those for the PDP-11/45 and 11/50 indicate the ECLIPSE is faster. (See Table 1.) The cache memory and interleaving of memory modules also increase throughput substantially. Context switching and multiprogramming on larger systems are facilitated by multiple user maps in the mapping unit, and extended operation macroinstructions that, for example, call a procedure and place relevant return information on the stack all in one instruction. These features are impressive and also necessary to make the ECLIPSE truly competitive with the PDP-11 because the PDP-11 is faster than it appears by looking at instruction execution times. The 2-address structure of the PDP-11 as well as the instruction set itself produce tight codes. Generally, fewer instructions are executed per task than on more conventional 1-address computers.

All in all, the ECLIPSE appears to be a well-conceived system from a company that has made few wrong moves in its short life. Also, the system's name "ECLIPSE" is refreshing (not a 3 in it anywhere) and perhaps prophetic. The system will certainly eclipse the Nova/Supernova and probably some competitors, but mostly it will win some and lose some to the PDP-11, HP 3000, MODCOMP I, II, IV, Varian 70, and Interdata 7/16 and 7/32.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes up to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, software subscription service for automatic timely updates of software and documentation, and summary of available software for users not needing revisions. The Data General User's Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time and materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

COMPATIBILITY

The ECLIPSE computer is generally program-compatible with the Nova/Supernova line, given comparable configurations, but there are some restrictions. ECLIPSE computers implement multiply/divide, hardware floating point, and memory management options differently than Nova/Supernova. For the first two, the difference is chiefly a matter of coding which is easy to

change, but memory management is a little more difficult to alter, because of functional differences, such as double user maps. ECLIPSE also uses the codes for "no-load" and "no-skip" Nova options in the standard instruction set, so Nova programs with these instructions are not compatible and must be altered. A compatible program cannot contain the data channel increment, add-to-memory feature, or execution and I/O time-dependent subroutines.

Both computers use the same type of I/O bus structure, and all Nova/Supernova peripherals can attach to ECLIPSE computers.

CONFIGURATION GUIDE

ECLIPSE S/100, the smallest model, has a memory capacity ranging from 8K to 32K words; core and semiconductor memory modules can be mixed. The CPU has space for seven standard circuit boards. The CPU occupies two boards, and each 8K-word memory module occupies one board. The remaining slots can be used for additional 8K-word memory modules, I/O subsystem controllers, and certain processor options. The S/100, which is designed for instrumentation or control applications with modest requirements, is housed in a small 5.25-inch high chassis but it can be expanded with another 16-slot chassis.

The S/200 system is a larger system designed for medium to large scale end-user applications. The 10.5-inch high chassis can hold 16 circuit boards, and it can be expanded to include another 16-slot chassis. Minimum systems include CPU, 16K words of memory and console. This can be directly expanded up to 32K words; the Memory Allocation and Protection (MAP) option allows memory to be further expanded to 128K words (256K bytes).

The MAP option available only on the S/200 model adds 12 instructions and occupies a full printed circuit board. Other processor options, such as automatic program load, power monitor/auto restart and a real-time clock are available for both systems. The extremely fast hardware floating point processor (FPP) Data General recently introduced is also available; FPP occupies one board and adds 54 instructions to the instruction set. Another important option is Writeable Control Store, which allows users to microprogram their own instructions.

Either system can attach any of the peripherals previously available to the Nova/Supernova line. These include the wide range of high-speed, low-speed, special-purpose, and communications devices listed in Table 4.

Adapters allow the ECLIPSE systems to be configured into multiprocessor configurations. The interprocessor bus allows dual computer/shared disc systems to be configured for front-end and message switching systems needing redundant CPU. An interprocessor bus allows networks of up to 15 Data General computers (Novas, Supernovas, Nova 2s, ECLIPSES) to be interconnected. An IBM 360/370 adapter allows the ECLIPSE to be interfaced directly to an IBM system.

The various operating systems have different minimum configuration requirements. RDOS and MRDOS are the standard ECLIPSE operating systems but RTOS and SOS subsets can be used as well. Table 5 summarizes software system and includes the configuration required for each major package.

Table 4. Data General ECLIPSE: Peripherals

DEVICE MODEL	DESCRIPTION
DISCS	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
Magnetic Tape	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm

Table 4. (Contd.)

DEVICE MODEL	DESCRIPTION
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
Displays	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
A/D, D/A Systems	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
Digital	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

Table 5. Data General ECLIPSE: System Software

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console

Table 5. (Contd.)

PACKAGE	DESCRIPTION
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

PRICE DATA

Model No.	Description	Purchase Price[1] $
S/100	Computer (microprogrammed CPU with capacity for 64K bytes of memory) with	
	16K Bytes Std Core	9,200
	16K Bytes ERCC Core	11,200
	32K Bytes Std Core	11,900
	16K Bytes Std SC	10,700
	16K Bytes ERCC SC	12,700
	32K Bytes SC	14,900
S/200	Computer (microprogrammed CPU with capacity for 256 bytes of memory) with	
	32K Bytes Std Core	16,300
	32K Bytes ERCC Core	19,300
	128K Bytes Std Core	32,500
	32K Bytes Std SC	19,300
	32K Bytes ERCC SC	22,300
	128K Bytes SC	44,500
	Memories*	
	16K-Byte Core	2,700
	16K-Byte ERCC Core	3,700
	16K-Byte SC Memory	4,200
	16K-Byte SC ERCC	5,200
	Representative Systems	
	Small Process Control System including: ECLIPSE S/100, 64K Bytes ERCC Memory, Fixed-Head Novadisc, A/D Subsystem, PT Reader, Display Terminal	46,600
	Remote Data Concentrator including: ECLIPSE S/100, 48K Bytes of Memory, Communications Interfaces	33,350
	Large Data Base Management System including: S/200 Computer, 256K Bytes of Memory, 2 3330-Type Disc Pack Drives, Line Printer, Card Reader, 13 Display Terminals	186,700
	Large Dual Processor System for message switching or front-end processing: 2 S/200 Computers each with 256K Bytes of Memory, 3330-Type Disc Pack, Fixed-Head Novadisc, 2 Magnetic Tape Transports, 2 Display Terminals	263,000
	FORTRAN 5 System in Computation Environment: S/200 Computers, 96K Bytes of Core Memory, 64K Bytes of SC Memory, Floating-Point Processor, Moving-Head Disc, Magnetic Tape Transport, Line Printer, Card Reader, Display Terminal	81,400

Notes:

* *ERCC = Error Checking and Correcting.*

(1) Quantity discounts range from 10% to 40%.

HEADQUARTERS

Data General Corporation
Southboro MA 01772

(See Report S379.011.050 for System Overview and Competitive Position)

MAINFRAME

The ECLIPSE® architecture allows the computers to operate in a variety of environments. The memory allocation and protection (MAP) unit, an optional feature on the Model S/200, allows hardware-protected dual program operation. Two user maps allow two programs to operate concurrently in completely different hardware-protected environments, although only one can be performing I/O functions at any given time because only one data channel map is provided. Multiprogramming operating systems allow up to 32 users to be serviced concurrently; one batch program can execute in a background mode. In addition, the standard DMA channel allows block I/O transfers to proceed independently of the CPU once the block transfer has been initiated.

The dual processor/shared disc system is built around two or three standard Data General computers, one moving-head or fixed-head disc, and real-time Disc Operating System (RDOS). Each processor has 64K bytes of memory and an interprocessor bus for communication between computers. High-level languages and utility software are included. Under RDOS, both computers have on-line access to programs and data files. Hardware multiplexed data paths allow access to the data base and programs by both processors. Each processor is independent, but all share the same disc data base. Combinations of fixed and moving-head discs can be used in configurations. Maximum disc storage is obtained with eight moving-head disc packs (200M bytes) and 8M bytes of fixed-head storage.

Communication between the two processors is handled via the interprocessor bus. The bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — Carries the data for intercomputer communication.
- Dual 1-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of 1 million bytes per second.

The main advantage of a dual-processor configuration is continual system availability, even when one processor is down. Also, programs and data-base files can be shared. The first processor can gather and reduce incoming data and monitor real-time operations. The second processor, used in the background mode, can develop new programs or carry out batch processing. Using MCA, processors can access each other through the I/O bus.

Where high throughput and continuity are prime considerations, the dual-processor system can handle many communication lines and data rates that peak at unpredictable times. The first processor stores or forwards messages to the second processor for peak times. The second processor shares the message load (doubling throughput), handles peak data rates, and controls the switching if the first processor is down. The second processor can also accumulate network statistics, compile management reports, and generate customer service charges.

In a time-sharing situation where common access to programs is needed yet file protection is required, each processor functions as an independent time-sharing system. All terminals can handle Extended BASIC.

Central Processor

The ECLIPSE S/100 and S/200 are microprogrammed systems with conventional bus structures and nearly identical architecture. The S/200 can include 16 circuit boards instead of the seven allowable on the S/100; the S/200 includes memory mapping allowing expansion to 128K words (256K bytes) as a standard feature instead of the 32K-word (64K-byte) maximum allowable on the S/100. Most other system differences stem from these two features. All peripherals, most processor options, and most of the software can be used on either system.

Important processor options include an extremely fast floating-point processor, writeable control store, and memory mapping (S/200 only).

Data Structure. The basic unit of data is the 16-bit word. Negative numbers are represented in two's complement form with the most significant bit representing the sign. Basic arithmetic instructions use 1-word operands. Single- and double-precision floating-point arithmetic are performed either by subroutines or by a hardware option, using 2- or 4-word operands: a 7-bit exponent, 1 sign bit, and a 24- or 56-bit fraction. Alphanumeric data is represented in ASCII code, two bytes per word.

Special Registers. The processor operates under control of a 15-bit program counter. Four 16-bit accumulators are provided, two can also serve as index registers. Core locations 0 and 1 serve as program interrupt pointers. Four 64-bit accumulators are provided for the floating-point arithmetic option.

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Additional addressing flexibility is furnished by 16 core locations that serve as autoincrement or autodecrement registers (eight locations each). The contents of these core locations are automatically incremented or decremented by 1 when indirectly addressed before the contents are used as an indirect address.

Instruction Set. The basic instruction set includes 87 instructions, some of which are capable of a variety of permutations. "Compare Limits," for instance, compares the contents of two specified accumulators and checks if the number is within specified bounds. The "Vector" instruction is affected by five modes. Eight of the arithmetic and logical instructions have more than 100 permutations implemented.

Basic instructions include 50 fixed-point arithmetic instructions, eight logical instructions, six shift instructions, seven bit manipulation instructions, two byte instructions, two block move instructions, 10 stack instructions, eight I/O instructions, and eight CPU instructions. In addition to the basic set (which is a superset of the basic Nova/Supernova instruction sets), 56 additional instructions are included with the hardware floating-point processor and 12 with the memory mapping option. Hardware multiply/divide and multiple precision arithmetic are standard ECLIPSE instructions. Basic instructions are one word long; 2-word formats specify extended addressing.

The ECLIPSE instructions unavailable for the Nova/Supernova provide block, byte, and bit manipulation, signed multiply/divide, immediate addressing, doubleword shifts, and stack facilities. Data General defines a stack as a series of variable-length temporary storage areas called frames. A single instruction allocates the frame, saves the entire machine state, and sets a pointer. A single instruction can push or pop registers on/off a stack. A single instruction can also push or pop all four floating-point registers as well as the floating-point status register; execution time is 8.4 microseconds for the push and 9.8 microseconds for the pop.

All arithmetic, logical, shift, and test operations are performed on operands located in the accumulators. The arrangement of the register-to-register instructions allows combining a logical or arithmetic operation on two operands with shifting the result left or right 1-bit position; specifying the carry as its current value, the complement of its current value, zero, or one; loading or not loading the result into an accumulator; and testing the result and/or carry for zero or nonzero. Thus, each instruction performs functions that require several instructions for some other small computers.

Input/output instructions provide for initiating all I/O transfers as well as for controlling the real-time clock, the multiply/divide option, and the interrupt system. Typical instruction execution times are shown in Table 1.

Table 1. Typical Instruction Execution Times

Type of Instruction	Typical Time, μsec(1)
Simple Add/Subtract/Logical Complement, Increment, Move	0.6
Extended Add/Subtract, Immediate	1.2
Compare Limits	1.6 – 2.6
Shift	1.8 – 3.0
Double Shift	2.4 – 4.2
Jumps	0.7
Extended Jumps	1.6
Skips	2.3
Skip On Test	1.0 – 2.8
Divide	9.6
Multiply	7.2
Indirect Reference	0.65
Auto Index	1.15
Floating Add/Subtract(2)	2.4
Floating Divide(2)	4.6
Floating Multiply(2)	3.9
Long Add/Subtract(2)	2.4

Notes:
(1) Times vary considerably depending on type of memory and interleaving; these times assume 4-way interleaved core memory.
(2) Using hardware option.

Addressing Facilities. The addressing scheme allows direct, indirect, indexed, and combined indexed and indirect addressing.

All memory reference instructions contain an 8-bit address field. The 8-bit address can be used either as an absolute address of the first 256 words of memory or as an increment relative to the contents of the program counter or either indexed register. For relative and indexed addressing, the 8-bit address field is used as a 7-bit signed number; thus the instruction can address core locations within the core area defined by the contents of the program counter or an index register -128 to +127.

A memory referencing instruction can specify indirect addressing, which is recursive. Indirect addressing can be combined with indexing, which precedes all indirect addressing. In addition, autoincrement and autodecrement registers are provided. These are memory locations that automatically increment or decrement by 1 when indirectly addressed; the incrementing or decrementing is done before the contents are used as the indirect address.

Indirect addressing adds one memory cycle time per level to the instruction execution time; and indexing adds a half cycle.

Interrupt Control. The interrupt system consists of one interrupt line and a 16-bit programmable mask register that establishes 16 levels of priority interrupt.

Device priority within an interrupt level is determined by the device's physical location on the I/O bus; the device nearest the processor has highest priority.

The processor grants an interrupt under the following conditions: the processor has completed an instruction or a data channel transfer; no device is requesting a data channel transfer; at least one device is requesting an interrupt; and interrupts are enabled.

When the processor grants an interrupt, it disables the interrupt system, stores the contents of the program counter in location zero, and generates an indirect jump to location 1, which must contain the address of the interrupt servicing routine. The servicing routine can selectively inhibit lower-priority interrupts and allow higher-priority interrupts by setting bits in the interrupt mask register.

MEMORY

Memory consists of either core of MOS semiconductor memory modules, 8K words each. Each memory word is 16 bits long. Memory can include an error checking and correcting (ERCC) feature, which adds five bits per word.

The algorithm allows not only checking for single and multiple errors but correcting of all single bit errors. The check bits are generated and stored as each word is written into memory. They are recalculated when the word is read from memory and compared to bits stored with the word. The bits that do not agree are used as a code to determine the bit in error. The error is then corrected and the correct word is dispatched. The ERCC circuitry requires no extra time for checking, but it requires 200 to 800 nanoseconds to correct an error.

MOS semiconductor memory includes a 16-word, bipolar cache memory on each 16K-byte memory module. When a memory location is addressed, the processor looks in cache memory to determine if the contents of that memory location are stored there. If so, the word is sent to the CPU in 200 nanoseconds. If not, the word is read from memory and sent to the CPU in 700 nanoseconds and the contents of the three adjacent memory locations are loaded into cache memory, replacing those words that have been unused for the longest time. Most programs access memory locations in sequence, thus the desired word will be in cache a good proportion of the time.

Memory modules are also interleaved: up to eight ways for core modules and up to four ways for MOS modules.

In addition, memory operations can be overlapped. A read from one module can be overlapped with a write to another module. Memory operations on three modules can be overlapped with CPU processing.

Memory size ranges from 8K to 32K words on the System S/100, and from 16K to 128K words on the S/200. The S/200 uses a hardware memory management option to address memories larger than 32K words.

Memory Allocation and Protection (MAP). Like the Memory Management and Protection Unit (MMPU) used with the Nova 840, MAP maps logical addresses into physical locations, establishes user and Executive modes and provides various protection functions related to multiprogramming. The MAP option allocates memory into up to 128 physical 2,048-byte blocks; up to 32 blocks are allocated to each user and up to 32 users can operate concurrently. MAP holds three address maps simultaneously: two are user maps and the third is a data channel map. The data channel map allows the data channel and the CPU to operate concurrently without map switching, and the two user maps speed context switching. For example, one user can be performing I/O while a second is executing programs with no CPU overhead for context switching between the two.

MAP provides five different types of protection:

- Validity — prevents a user from accessing physical memory allocated to another.
- Write — protects shared physical memory from alteration.
- Indirect — prevents endless indirect loops by limiting indirect addressing to 16 levels.
- I/O — prevents unauthorized access to an I/O device.
- Data channel — prevents data channel from altering unauthorized memory.

MAP is used with the MRDOS operating system to allow hardware-protected dual operations. Two programs can run concurrently and independently; the multiple mapping registers cut processor overhead for context switching to almost zero. The two user maps provide the chief difference between MAP and MMPU (used on Nova 840) which has only one user map.

MAP is addressed as an I/O device although it is located between the processor and memory and the data channel and memory.

I/O Control

ECLIPSE systems have two I/O channels: the programmed I/O channel and the direct memory access (DMA) channel.

All I/O channels operate over the I/O bus, and 59 devices can be distributed in any combination between programmed I/O and DMA.

Data words are transferred over the programmed I/O channel between an accumulator and a peripheral device; a separate I/O instruction is required for each data word transferred.

Once initiated by instructions, blocks of data words are transferred over the DMA between core memory and a peripheral device. The device controller controls the transfer of each data word. Processing is suspended as each data word is transferred. DMA channel transfer requests are serviced at the end of the current instruction.

The I/O instruction has a 6-bit device address field, but five device codes are used for various central processor features, leaving 59 for devices.

PERIPHERALS

Peripheral devices for the ECLIPSE line are the Nova/Supernova peripherals. They include conventional slow-speed devices and high-speed mass storage devices (such as magnetic tape and discs) as well as special-purpose equipment, all of which require interfaces or controllers.

Slow-Speed Peripherals. Slow-speed devices use the programmed I/O channel for the transfer of control information and for data transfers.

CONSOLE TYPEWRITERS A-E

4010 A-E Teletype Model ASR 33/KSR 33/ASR 35 (10 cps) — require 4010 Teletype I/O Interface and 4007 I/O Interface Subassembly; ASR units include paper tape reader/punch.

4023 A/B Teletype Model ASR 37/KSR (37.15 cps) — require 4010 Teletype I/O Interface, 4023 I/O Interface, and 4007 I/O Interface Subassembly; ASR includes paper tape reader/punch.

PAPER TAPE

4011B High-Speed Paper Tape Reader (300 cps) — requires 4011 Paper Tape Control and 4007 I/O Interface Subassembly.

6013 Paper Tape Reader (300 cps).

4012A High-Speed Paper Tape Punch (63.3 cps) — requires 4012 Paper Tape Punch Control and 4007 I/O Interface Subassembly.

PUNCHED CARDS

4016A-G Medium-Speed Card Readers (225/400/150/285/400/600/1,000 cpm) — require 4016 Card Reader Control and 4036 I/O Interface Subassembly.

PRINTERS

4034A Data Products Line Printer (80-col line; 64-char set; 356 lpm) — require 4034 Line Printer Control and 4014 I/O Interface Subassembly.

4034B Data Products Line Printer (132-col line; 64-char set; 235 lpm) — same requirements as for 4034A.

4034C, D Centronics Serial Matrix Printer (132 col/line; 165 cps) — same requirements as for 4034A; Model C uses 5 x 7 matrix, Model D, 7 x 9 matrix.

Data General designed, Data Products manufacture, 64-character set, 300 lpm; 94-character set, 240 lpm.

MARK SENSE

4016 H-L Mark Sense Card Readers (150/285/400/600/1,000 cpm) — same as 4016A.

High-Speed Peripherals. ECLIPSE computers support both magnetic tape (industry standard 7- or 9-channel and cassette tape drives) and disc storage peripherals: 7 low-capacity, fast-access fixed-head units; 2 moving-head, high-capacity units; and 2 removable cartridge units.

MAGNETIC TAPE

4030I Wang 1045 Magnetic Tape Transport (7-channel; 45 ips; 556/800 bpi; 25/36 kb/sec transfer rate) — requires 4030 Magnetic Tape Control; control connects to DMA and can control up to 8 transports.

4030J Wang 1045 Magnetic Tape Transport (9-channel; 45 ips; 800 bpi; 36 kb/sec transfer rate) — same requirements as for 4030I.

4030K Wang 812 Magnetic Tape Transport (7-channel; 12.5 ips; 556/800 bpi; 6.9/10 kb/sec transfer rate) — same requirements as for 4030I.

4030L Wang 812 Magnetic Tape Transport (9-channel; 12.5 ips; 800 bpi; 10 kb/sec transfer rate) — same requirements as for 4030I.

4030M Wang 1175 Magnetic Tape Transport (7-channel; 75 ips; 556/800 bpi; 41.7/60 kb/sec transfer rate) — same requirements as for 4030I.

4030N Wang 1175 Magnetic Tape Transport (9-channel; 75 ips; 800 bpi; 60 kb/sec transfer rate) — same requirements as for 4030I.

Data General, 7-/9-track, 75 ips, 556,800/800 bpi.

MAGNETIC TAPE CASSETTES

4080 Novacassette (1,600 bps; 3 drives, chassis, for ⅛-in. tape) — requires 4076 Controller, 4075 Interface.

4081 Novacassette single-drive version of 4080.

4084 Novacassette dual-drive version of 4080.

FIXED-HEAD DISCS

4019A Alpha Data Disc Unit (32 tracks on 1 surface; 65,536-wd storage capacity; 57,835-wd/sec transfer rate; 16.7-msec rotation time) — requires 4019 Disc Controller, which can operate up to eight 4019A, B, or C disc units in any combination; connected to system by DMA.

4019B Alpha Data Disc Unit (same specs as 4019A except 2 surfaces totaling 131,072 words).

4019C Alpha Data Disc Unit (64 tracks on 2 surfaces; 262,144-wd storage capacity) — other specs same as 4019A.
6001 Novadisc Drive (128K-wd storage capacity) — same requirements as for 4019A.
6002 Novadisc Drive (256K-wd storage capacity) — other specs same as 6001.
6003 Novadisc Drive (512K-wd storage capacity) — other specs same as 6001.
6004 Novadisc Drive (768K-wd storage capacity) — other specs same as 6001.

Data General Disc — 45.9m-word capacity, 403K word-per-second transfer rate, 30-msec positioning time.

MOVING-HEAD DISC PACK DRIVES
4048A Century 111 Drive (like IBM 2311) (200 tracks on each of 10 surfaces; 3,072,000-wd storage capacity; 80,000 wd/sec transfer rate; 25-msec rotation time; 75-msec average head positioning time) — requires 4046 Disc Control and 4048 Adapter, which can operate up to 4 disc units; connected to system by DMA.
4057A Century 114 Drive (like IBM 2314; same specs as 4048 except 20 surfaces totaling 12,288M wds) — uses 4057 adapter.

MOVING-HEAD DISC CARTRIDGE DRIVES
4047A Diablo 31 Single Cartridge Drive (203 tracks on each of 2 surfaces; 1.247M 16-bit-word storage capacity; 90,000 wd/sec transfer rate; 70-msec head positioning time; 40-msec rotation time, has 1 removable disc cartridge) — requires an adapter and a 4046 Disc Control and 4047 Adapter.
4047B Diablo 33 Drive (same specs as 4047A except 4 surfaces totaling 2.494M words; has 1 fixed disc and 1 removable disc cartridge) — requires an adapter and a 4046 Disc Control and 4047 Adapter.

Special-Purpose Devices. Special-purpose devices include analog/digital equipment, plotters, CRTs, a numerical control subsystem, clocks, and an interface board for a user's own device.

ANALOG/DIGITAL
4032 Basic A/D Interface — requires 4014 I/O Interface Subassembly; can accommodate 4033 A/D Interface Expansion.
4055 A-Q A/D Converters, Multiplexors, and Other Subsystem Components — converters for 8-15 bits; multiplexors; 2 enclosures, enclosure for 128 single-ended or 64 differential channels.
4037 D/A Converter Control (60 kHz, 10 bits) — has no interrupt facility; has 8-bit channel select register and a data register.
4056 A-H Converters, Timing, Enclosure, Converters for 8-14 bits — enclosure for 24 D/A converters.
4065 I/O Interface Subassembly, 16 input, 16 output lines — requires 4066 Digital I/O Interface and 4067 or 4068.
4067 External Interrupts; 8 interrupts.
4068 Programmable Interval Timer.
4085 Wide Range Analog Input System, for up to 512 input channels; various submodels for 13- or 15-bit A/D converters — sample rates up to 200 samples/sec.

PLOTTERS
4017 A/B CalComp 565 Incremental Drum Plotter (300 steps/sec at step sizes of 0.01 or 0.005 in. and 0.1 mm, 12-inch paper) — requires 4017 Incremental Plotter Control and 4014 I/O Interface Subassembly; B model is rack mountable.
4017C CalComp 563 Incremental Drum Plotter (200/300 steps/sec at step sizes of 0.01 or 0.005 in. and 0.1 mm, 30-inch paper) — same requirement as for 4017A.
4017D CalComp 502 Incremental Flatbed Plotter (300 steps/sec at step sizes of 0.01, 0.005, or 0.002 inch and 0.1 or 0.5 mm, 31- x 34-inch plot area) — same requirements as for 4017A.
4017E Houston Instruments DP-1 Incremental Plotter (300 steps/sec at step sizes of 0.01 or 0.005 in. and 0.25 or 0.10 mm), Z-fold paper 11 in. wide — same requirements as for 4017A.

CRT
6010/CPU Video Display, variable code structure baud rate (24-line, 80-char) — requires 4010, 4023, or 4060-63 Interfaces.
6012/CPU Video Display — same as 6010; also has local editing.
4010I/CPU Infoton Vista Video Display (variable code structure and baud rate; 20-line, 80-char) — requires 4010 Teletype I/O Interface or 4060-63 Multiplexor.

Numerical Control

Contour 1 System, a special subsystem designed for numerical control, utilizes a CPU, paper tape reader, special console and peripherals, and 8K words of memory to control two machine tools doing different jobs. Addition of 4K words of memory allows the system to control a total of four different tools simultaneously. Setup time (a significant element of the time required for short runs) is minimized because the parts programmer can alter programs on-line. Dataprep, a software package, allows preparation of the numerical control tapes.

OTHER PERIPHERALS
4008 Real-Time Clock (10-Hz, 100-Hz, 1,000-Hz line frequencies, 4 selectable frequencies) — includes an interrupt; requires 4007 I/O Interrupt Subassembly.
4079 Real-Time Clock — same as 4008 but uses 4075 interface.

4040 General-Purpose Interface Board — can accommodate a 4041 16-bit input register and 16-bit output register, and a 4042 Data Channel Connection.

DATA COMMUNICATIONS

Data General supplies four basic series of multiline data communications interfaces: three single-line interfaces, and a special interface for creating a multiprocessor network. The 4026 Sixteen-Line Teletype Multiplexor, the 4060 Series Asynchronous Multiplexor Adapters, the 4073/4074 Synchronous Multiplexors, and the 4100 Multiline Asynchronous Controller Subsystem (MAC) all employ a variety of methods to control multiple lines; in most cases, each controller is addressed as a single device.

The 4026 directly controls 16 lines, whereas the 4060 Series is made up of one to 16 subsystems, each of which can receive, transmit, and buffer characters on four lines. Both multiplexors operate, however, as a single I/O device. The 4074/4073 Synchronous Interfaces handle one and four lines, respectively, but up to 16 interfaces can be connected to a system.

The 4100 Multiline Asynchronous Controller Subsystem (MAC) can economically control from two to 1,024 asynchronous lines at programmable line speeds ranging from 50 to 9,600 baud. MAC can be used for message switching, for remote line concentrating, and for front-end communications processing.

The 4038 Multiprocessor Communications Adapter links up to 15 ECLIPSE computers into a multiprocessor communicating network.

4026 Sixteen-Line Teletype Multiplexor — connects to programmed I/O bus for data transfers; full-duplex; has internal clock; output to 4027 (TTY 33, 35) TTY or 4028 (TTY 37, Bell 103) EIA interface; EIA-level input only.

4023 Single-Channel Asynchronous Interface, full-duplex receiver transmitter — communicates between Bell 103, 202, or equivalent and computer; connects to I/O bus; requires 4010 Teletype I/O Interface and 4007 I/O Interface Subassembly.

4060, 4061, 4062, 4063 Hardware Asynchronous Multiplexor Adapters (transmission rate up to 9,600 baud) — allows computer to communicate with up to 64 full-duplex lines; Models represent EIA or Teletype interfaces wired for use with 4050 or 4051 interface panel.

4073, 4074 Synchronous Multiplexors — 4-line and single-line versions (64 lines/system max).

4100 Multiline Asynchronous Controller Subsystem (MAC) (programmable line speeds from 50-9,600 baud) — controls up to 1,024 async lines; basic interface cards are 2-line EIA/modem, 4-line local TTY, 4-line EIA; multiple CPUs can access common communication chassis.

4015 High-Speed Communications Controller (6,000-50,000 bps for high-speed, full- or half-duplex sync Bell 201, 301, or equivalent data sets) — up to 17 controllers can connect to 1 processor; connects to DMA or high-speed data channel for automatic block transfers; internal clock option.

4025 Interface to IBM Systems/360 and 370 (300 kc) — operates on multiplexor, block multiplexor, or selector channels.

4038 Multiprocessor Communications Adapter (500K wd/sec bus transfer rate) — up to 15 processors can be interconnected; one 4038 per processor.

SOFTWARE

ECLIPSE software is the same as the Nova/Supernova software: it includes utility routines; three sets of assemblers (one absolute, one relocatable, and one macro); ALGOL, BASIC, FORTRAN IV, and FORTRAN 5 compilers; Real-Time Operating System (RTOS); Stand-Alone Operating System (SOS); Real-Time Disc Operating System (RDOS), and Mapped Disc Operating System (MRDOS).

Operating Systems

RDOS. RDOS is a modular foreground/background real-time disc operating system with comprehensive file capabilities plus the flexibility of a multiprocessing, multiprogramming environment. Dual-processor, partitioned-disc software allows both processors to share discs completely under RDOS control. Up to 32K words (64K bytes) of memory can be dynamically allocated to a single program in either the foreground or the background on the S/200 which includes Memory Allocation and Protection (MAP). MAP allows core memory to be extended to 128K words (256K bytes) and provides protection for both user programs and the operating system.

Programs can operate in either protected or unprotected foreground/background modes. The multipartitioning system allows users to swap programs between memory and disc and to overlay program tasks within a user program; the operating system itself operates with a core-resident executive that calls on system overlay modules from disc as needed. A 256-level hierarchy determines the priority for CPU processing time for tasks in the foreground and the background programs that are running simultaneously. Foreground program tasks, which are expected to be real-time tasks interacting with external devices, can be stored in a foreground root program or in one of 128 core overlay areas, depending on response time needed. Nonresident foreground tasks are stored on disc in absolute main memory image form to reduce response time for loading and executing. Three

types of disc file organizations are available under RDOS: sequential, random, and contiguous. Background tasks, which are usually batch processing jobs, overwrite the Command Line Interpreter (CLI) and restore it as soon as the program is completed.

Simple program swapping for up to five program levels overwrites an entire resident core image with a disc file image of another program. In addition, tasks within a program can be overlayed or swapped to an unlimited number of sublevels. A root program remains core resident; it is followed by an overlay area, which begins at an address called the node point and extends up to an address high enough to accommodate the largest overlay within this overlay area that contains the changing tasks. The entire program including overlays is treated as a single program level.

A program can communicate with another program through the use of common files in memory or on disc. User overlays can be implemented with either reentrant or nonreentrant code in both single task and multitask environments. In a multitask environment, a conditional load request, which loads an overlay if it is not already memory resident, requires that the overlay be in reentrant code.

The user can communicate with RDOS with task commands as well as with system calls and CLI available for DOS. The task commands permit the creation or modification of tasks under program control and alterations to their priority and status. RDOS handles all I/O and interrupt conditions for the user and provides file system capability using fixed-head disc storage and movable-head disc cartridge or disc pack units. Specific hardware configurations required for running RDOS depend on the particular system supported.

Communication with the operating system is on two levels: direct program communication via system calls, and indirect communication via the command line interpreter (CLI). CLI is not part of the operating system; it is a system program that is called when the system is idle or when the user program is interrupted by the operator via the Teletype keyboard. The interpreter can perform the following functions:

- Direct the flow of program control.
- Create, delete, or rename files.
- Transfer a file to another file or to any output device.
- Transfer information to a file or to any output device.
- List all entries in the file directory.
- List all information concerning a file, including attributes and size.
- Create a saved file of the current memory state and a core image.

The user can access all files by name; the operating system provides file names for all peripheral devices. In addition, the user can reference files in a line, sequential, or random access mode. The random access mode accesses files by record number.

RDOS can support the following system software:

- Command line interpreter (CLI).
- Text editor.
- Library file editor.
- Relocatable assembler.
- Relocatable loader.
- Symbolic debugger.
- ALGOL compiler.
- FORTRAN IV and 5 compilers.
- Relocatable math library.

RDOS supports as many as 15 interconnected computers. The computers are connected through direct memory access (DMA) channels, which permit fast intercomputer communication of programs or data with minimum processor overhead. The computers are interfaced through Multiprocessor communication Adapters (MCA).

Full Batch processing capabilities are available to ECLIPSE users through the BATCH software package. Running under RDOS, BATCH can run jobs in Assembly language, FORTRAN IV, FORTRAN 5, and ALGOL. A user can specify with a single command which devices and files are to be used. Without operator interruption, BATCH can run programs from different input device types. BATCH can run alone or as part of a multiprogrammed system in the background mode. The basic configuration required to support BATCH is any ECLIPSE computer with at least 16K words of memory, a disc, and input and output devices. Data can be spooled onto a disc as intermediate storage instead of being transmitted directly to an output device. When the device becomes available, the data is transferred off disc to the output device.

The minimum configuration required by RDOS is 16K words of memory, S/100 or S/200 CPU, 2.5M words of disc storage, and console.

MRDOS. A special version of RDOS, called MRDOS (Mapped Real-Time Disk Operating System) is used when the Memory Allocation and Protection (MAP) option is included in an S/200 system. MRDOS in conjunction with MAP is designed to manage a tripartite environment; two user programs can execute simultaneously in independent environments, while system software is protected from both. MRDOS requires 24K words of memory, a 2.5M-word disc, S/200 CPU with MAP option and console. Like RDOS, MRDOS is compatible with RTOS and SOS.

RTOS. RTOS is a small basic real-time executive designed to handle a number of real-time tasks simultaneously. It provides I/O timing, inter-program communication, data buffering, priority handling, and task sequencing. The system is modular and it can reside in as

little as 1K words of memory. The minimum system configuration required to use RTOS must include 4K words of memory and a real-time clock. RTOS is a compatible subset of RDOS and MRDOS; it can support a wide range of conventional and real-time peripherals and can be used as a run-time system for programs developed under RDOS/MRDOS.

SOS. SOS is a compatible subset of RDOS allowing users to edit, assemble, or execute programs stored on magnetic tapes or cassettes. It provides buffered service of I/O peripherals on a device-independent basis, and it provides stand-alone facilities, structured to run programs in a nondisc environment. Programs for SOS can be developed under RDOS/MRDOS.

Languages

Data General supplies three compilers and two interpreters: FORTRAN IV, FORTRAN 5, and ALGOL compilers and two BASIC interpreters.

Nova/Supernova FORTRAN. The Nova/Supernova FORTRAN IV is an extended implementation of the Standard ANSI FORTRAN programming language. The following extensions are included:

- Multiple entry to subprograms.
- Abnormal returns via dummy variables.
- Mixed mode arithmetic.
- Unlimited array dimensions.
- Specification of lower subscript bound, including negative.

FORTRAN IV runs under RDOS and SOS; it requires at least 8K words of memory.

FORTRAN 5, which runs under RDOS, is a compatible superset of ANSI FORTRAN IV; it is compatible with IBM's Level H FORTRAN and FORTRAN and Univac's FORTRAN 5. Compiled programs written in FORTRAN 5 can be executed on any Eclipse computer with a floating-point processor and hardware multiply/divide. To compile FORTRAN 5 programs, a system must include an Eclipse computer with 28K words of memory, 512K words of disc storage, floating-point processor, hardware multiply/divide, magnetic tape or cassette transport, and console terminal. FORTRAN 5 adds the following extensions to Data General's FORTRAN IV.

- Full mixed-mode arithmetic.
- INCLUDE statement.
- Optimized DO loops.
- Static and dynamic storage allocation.
- Generic library functions.
- Subscript handling to allow a single computation of repeated subscripts.

Optimization is performed on the program as a whole during compilation rather than on individual statements only.

Algol. The ECLIPSE ALGOL is an extended implementation of the ALGOL 60 programming language with the following exceptions:

- No blanks within identifiers are permitted; an underscore can be used to separate logical parts of identifiers.
- Identifiers cannot contain more than 32 characters.
- Identifiers that are the same as ALGOL keywords cannot be redefined.

ALGOL includes the following extensions to ALGOL 60:

- Procedure blocks can be externally compiled.
- SHIFT, ROTATE, and ADDRESS functions are built in.
- Subscripted labels are allowed.
- Character string variables can have substrings.
- Octal literals are permitted.
- Base and pointer variables are allowed.
- Inclusive OR Boolean operator is permitted.
- Essentially infinite-precision arithmetic can be used.
- Declaration of array precision is optional.

ALGOL runs as a stand-alone program or under RDOS. It requires 12K words of main storage.

Basic. Data General supplies two versions of BASIC: Standard BASIC for a single user operating the ECLIPSE as a desk calculator and Timesharing BASIC for 16 users. Both versions are a full implementation of the BASIC language developed at Dartmouth College.

Assemblers

Data General provides three assemblers: standard, relocatable, and macro assembler. All have the same facilities except that the standard assembler produces absolute, binary output code and the relocatable and macro assemblers produce relocatable, binary output code. In addition, Data General provides cross assemblers for preparing programs on the Univac 1108, CDC 6600, and the IBM System/360 or 370.

Standard Assembler. The relocatable assembler language is a straightforward, machine-oriented programming language, designed for small systems with no mass storage devices. Source coding is written in a free form, but the listing of the source code can be formatted by the user. Some format is intrinsic to the language because the format characters are used as punctuation. For example, the source program is automatically formatted into lines because all statements, except label statements, must terminate by at least one carriage return before a new statement can begin.

To assemble a program, the assembler requires 2 passes of the source tape. The first pass checks the syntax and builds the symbol table; thus all symbols must be defined before they are used. In addition, the first pass must be able to evaluate all statements that indicate how integers are interpreted and all statements that alter the

normal location counter sequence. The second pass evaluates all other statements, punches an output tape, and produces a listing of the output code. The standard assembler can operate in a minimum 8,192-word configuration.

Relocatable Assemblers. The relocatable assemblers are extended versions of the standard assembler and provide the following extension features:

- Output code can be absolute or relocatable and can be loaded by the relocatable loader.
- Programs can reference data, instructions, or addresses that are defined in other programs.
- A simple procedure can be used to define double-precision, decimal, and floating-point constants and to specify bit boundary alignment.
- Whole programs or portions of programs can be assembled conditionally based on the evaluation of an absolute expression.

If the extended features of the relocatable assembler are not used, the output tape is compatible with the standard assembler output tape and can be loaded by the absolute binary loader. The relocatable assembler requires an 8K-word configuration for operation. It is packaged in several ways: for SOS, RDOS, MRDOS, in binary format, and others.

Macro Assembler. The macro assembler that runs under RDOS or MRDOS gives the user many features in addition to those offered by the relocatable assembler.

- Expanded expression syntax that provides for implicit as well as explicit precedence; includes all logical comparison operators.
- An assembly repeat feature to produce many lines of source from a simple repeat construct; with a repeat constant of zero, it also provides for conditional assembly; conditionals can be nested to any depth.
- An assembler variable replacement scheme to allow the programmer access to assembler variables using appropriate source line references.
- A powerful macro facility that allows complete recursion, nested macro calls, and an unlimited number of macro definitions.
- An extensive macro library for often-used operations such as shifts, byte operations, logical operations, and signed comparisons.
- Literal references with any memory reference instruction; optionally, the assembler will eliminate all address errors by literal indirect references through page zero; literals can be absolute numeric quantities or any legitimate expression.

The macro assembler is completely compatible with the relocatable assembler.

Applications Packages

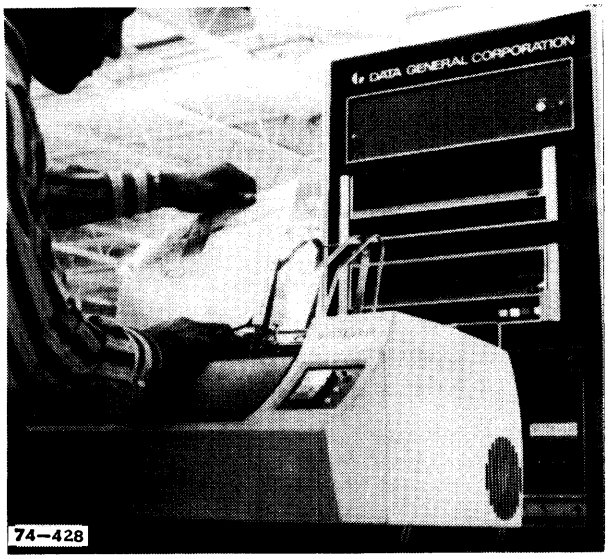
Data General supplies a Dataprep language and processor to allow a user to prepare parts programs for numeric control applications. The language consists of supervisory and editing commands and a number of geometric statements to define parts specifications. Input is from the Teletype keyboard or paper tape reader. Dataprep performs error checks on all input coordinates and geometric commands and prints an error message upon receipt of erroneous input.

Dataplot, another applications package, is designed for support of incremental plotters. It is a FORTRAN package including character generation, drawing lines, axes, and rotation of axes.

Other System Software

ECLIPSE utility software does not include any provisions for simulation of other computers, data sorting or merging, or report writing. A communications package provides for 2780 RJE emulation. A command "line" (language) interpreter operating under the RDOS or MRDOS provides, among other things, transfer of data from any input device to any output device, with the contents of the transferred records unchanged but properly formatted for the output device. Bootstrap loaders, which load the binary loader into core memory, are all ROM modules. The following routines are also available:

- Binary Loader — loads the output tapes from the standard assembler.
- Relocatable Loaders (several versions) — load the output tapes from the relocatable assembler.
- Editor (several versions) — edit source text and produce new output tape for the assembler.
- Symbolic Debugger — provides 31 commands to examine and alter user programs and to punch a new tape acceptable to the binary loader.
- Math Package — routines provide for single-precision multiply and divide for systems that do not have hardware multiply/divide, double-precision arithmetic operations, conversion routines, the floating-point interpreter, and floating-point subroutines.
- Diagnostic Routines, including Program Exerciser, Power Shut Down Tests (tests retention of memory data when power is shut down), Address Test (tests memory address selection logic), instruction Timer Test clock logic, Memory Checkboard II (tests worst-case memory noise), and Teletype Test II (tests functioning of the Teletype logic, interrupt system, and I/O bus logic). Diagnostics for discs, tapes, and communications equipment are also available.



OVERVIEW

Data General's Nova 2 line is a compact, low-cost replacement system for the Nova/Supernova line, chiefly in the OEM market. Nova 2 is functionally identical to the Nova/Supernova line architecture and compatible with all models except the Nova 840. The CPU has been redesigned to fit on a single circuit board; new low-cost core memory has been manufactured by Data General in 4K- and 8K-word modules that cycle at 800 nanoseconds and in a 16K-word module that cycles at 1,000 nanoseconds. Because Nova 2 is completely software and hardware compatible with the Nova/Supernova, it has a large body of tested facilities for support of many types of applications. Rock bottom prices, at least at this point in time, are possible because of the reduction in component size. This system unquestionably announces Data General's intention to continue vigorously competing in the OEM market, which in the past comprised around 50 percent of all installations.

Nova 2 has two submodels: the 2/4, a 4-slot system in a 5.25-inch high chassis weighing 50 pounds for a minimum system, and the 2/10, a 10-slot system in a 10.5-inch chassis weighing 110 pounds for a minimum system.

Nova 2 architecture, like the Nova/Supernova, is not microprogrammed, and it has a conventional bus arrangement. DMA and programmed I/O and a 16-level priority interrupt system are standard features. Up to 61 devices can be addressed but these can be multiplexed subsystems. Four accumulators, two of which are index registers, and 16 memory registers allow a variety of addressing modes. The instruction set allows a great many permutations of basic arithmetic and logical basic instructions so that several operations can be performed with one instruction. The memory bus is asynchronous, allowing different speed modules to be mixed on a system. In addition to manufacturing its own core, Data General has begun making a large number of its own peripherals, including discs, magnetic tape and cassette drives, printers, paper tape readers and CRTs. Table 1 summarizes system specifications.

Software for the Nova 2 includes a Real-Time Disk Operating System (RDOS), a Real-Time Operating System (RTOS), and a Stand-Alone Operating System (SOS); FORTRAN IV, FORTRAN 5 and ALGOL compilers; BASIC interpreters; three assemblers; cross assemblers for IBM 360/370, Univac 1100, and CDC 6000 systems; and a variety of utilities and applications.

Table 1. Data General Nova 2: Mainframe Characteristics

MODELS	
CENTRAL PROCESSOR	
Microprogrammed	No
No. of Registers	
Accumulators	4
Hardware Index	2
Memory	16
Addressing (wds)	
Direct	1,024
Indirect	32K
Indexed	Yes
Mapping	No
Instruction Set	
Implementation	Hardware
Number	202 (counting implemented sub-instructions)
Floating Point	Option
Hardware Stack	No
Writeable Control Store	No
Interrupts	
Levels	16
Type	Hardware
MAIN STORAGE	
Type	Core
Cycle Time, μsec	0.8, 1.0*
Basic Addressable Units	Word, byte
Capacity, bytes	
Min	8K
Max	64K
Increment Size (bytes)	8K, 16K, 32K
Ports per Module	1
Error Checks	Parity option
Memory Protection	No
Memory Management	No
Interleaving	Up to 8-way core, 4-way on MOS
INPUT/OUTPUT	
Max Devices Addressable	59
Programmed I/O	Yes
DMA	Std
DMA Transfer Rate	1,250K wds/sec

Note:
**Effective memory cycle time varies with type of members and number of memory modules interleaved.*

The Nova 2 systems were announced in June, 1973 and first delivered in 1973.

COMPETITIVE POSITION

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. The Digital Computer Controls (DCC) company has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line, because the expandability of the system allows memory sizes equal to the Nova 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically the popularity of the Nova/Supernova line has been part of Data General's problem; the company underestimated demand, slipped behind schedule from time to time, and as a result impatient OEM customers bought from the smaller companies. This competitive threat is counteracted by the Nova 2 line which is very competitive in price, comparable in speed, flexibility, and size.

The small size and reduced number of components work together to make the Nova 2 very competitive with one-board OEM minis and microcomputers from other manufacturers such as Computer Automation and General Automation. The 16K-word memory board allows the user more memory for a very small price increase over the minimum system and at prices lower than minimum systems of a year ago. This can save both OEM and end-user costs because of the ability to handle high-level languages in the larger memory, sometimes cutting programming time and costs by more than half.

The capabilities of the Nova 2 are expanded in Data General's compatible ECLIPSE® line. The ECLIPSE family of computers is Data General's most recent line of general-purpose minicomputers. The ECLIPSE systems run the gamut of the Nova/Supernova line that they replace, but with a variety of features added to increase speed and throughput; to add to system reliability and error handling; and above all to expand the flexibility of the system while maintaining compatibility with all Nova and Supernova models. With this line, Data General hopes to compete more aggressively in its former end-user markets while opening up new ones. The extended processing power gives Data General's current customers a system to move up to, and, as the line develops, they will undoubtedly find even more upward possibilities. OEM customers with greater speed, size, and checking requirements will be also interested in ECLIPSE. Table 2 highlights some of the chief differences between the Nova 2 and the ECLIPSE systems.

As the second largest minicomputer manufacturer, Data General has the worldwide service and support capabilities so important to many OEM manufacturers. These facilities are receiving increased emphasis, with two new software support services recently announced.

CONFIGURATION GUIDE

Data General introduced the Nova computers in 1973 as their OEM line. The minimum order for this equipment was five. To bring the price/performance advantages of the Nova 2 to the end user, Data General has announced end-user systems built around the Nova 2s, available in single quantities. These Nova 2 end-user systems now use the standard Data General operating systems.

The chief difference between the Nova 2/4 and 2/10 models is in packaging. The 2/4 is housed in 5.25-inch high chassis with four slots, while the 2/10 is housed in a 10.5-inch high chassis with 10 slots. The CPU in both cases is contained on a single circuit board, and single board modules are available for 4K words, 8K words,

Table 2. Chief Differences Between ECLIPSE and Nova 2 Computers

COMPUTER	ECLIPSE		Nova 2	
MODEL	S/100	S/200	2/4	2/10
Packaging				
No. of Slots	7	16	4	10
No. of CPU Boards	2	2	1	1
16K-wd Module	No	No	Yes	Yes
Chassis Height (in.)	5.25	10.5	5.25	10.5
MEMORY				
Types	Core; MOS	Core; MOS	Core	Core
Max Size (bytes)	64K	256K	64K	64K
Cycle Time	0.8 Core 0.7 MOS 0.2 Cache	0.8 Core 0.7 MOS 0.2 Cache	0.8 or 1.0	0.8 or 1.0
Memory Management				
Protect				
CAPABILITIES				
Stack Processing	Yes	Yes	No	No
Multiply/Divide	Std	Std	Opt	Opt
Microprogrammed	Yes	Yes	No	No
ERCC	Opt	Opt	No	No

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and 16K words of core. The 16K-word module is available only in the slower memory, 1.0 microsecond cycle time, however. Different speed memory modules can be mixed on one system. Options for Nova 2 systems include:

- Hardware multiply divide.
- Hardware floating-point arithmetic.
- Turnkey console.
- Power monitor/auto restart.
- Automatic program load.

Both can attach an expansion chassis adding 16 more slots.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, the Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in Paris, France; Frankfurt, West Germany; London, England; Hull, Canada; and East Hawthorne-Melbourne, Australia. Customer support includes up to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers to help users apply systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special ECLIPSE computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. A factory service contract allows equipment to be rapidly repaired at a repair depot for a monthly charge. On-call service contracts provide preventive maintenance checks and high-priority emergency service on the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

Minimum systems include 4K words of memory. These can be expanded up to 32K words of memory with console, peripherals, communication devices, and so on attached. Peripherals of all sorts are available, as noted in Table 3. Configuration requirements are basically determined by the operating system, language processors,

Table 3. Data General Nova 2: Peripherals

DEVICE MODEL	DESCRIPTION
DISCS	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K wds capacity
6000 Series	Nova discs (fixed-head), 128K, 256K, 512K, 768K wds capacity
4048A	Century 111, 3M wd capacity, IBM 2311 compatible
40578	Century 114, 12M wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M wds capacity
New	Data General, 45.9M-word capacity, like IBM 3330
Magnetic Tape	
4030 I-N	Wang Mag Tape Transports, 7/9-track, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-Drive versions
New	Data General Transports, 7-/9-track, 75 ips
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011B/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cpm
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps
New	Data General Printer, 240, 300 lpm
Displays	
6010/6012	24 lines, 80 char each; 6012 has local edit
4010	Infoton Vista, 20 lines, 80 char each
A/D, D/A Systems	
4032	Basic A/D interface, Models 4055 A/Q converters, 8 to 15 bits, multiplexors, 2 enclosures (128 single-ended channels, 64 differential)
4037	Basic D/A control, Models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters

Table 3. (Contd.)

DEVICE MODEL	DESCRIPTION
4085	Wide range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 Drum or Rack Mountable, 563 Drum, and 502 Flatbed Plotters
4017E	General Interface Board
Digital	
4065	I/O Interface Subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Read-time clocks, 10/100/1,000 Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed Controller 600-50,000 baud
4025	IBM 360/370 Interface
4038	Multiprocessor Communications Adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async, controller subsystem, up to 1,024 lines

and so forth which are used. Operating systems and their requirements are listed in Table 4.

Data General also offers a dual-processor shared-disc configuration using Nova 2/10s. Each processor has 32K words of memory, a real time clock, and a console terminal. The two CPUs are housed in a dual cabinet and connected by an interprocessor bus. They share a disc subsystem which can include anywhere from 2.5M to 200M words of storage.

The interprocessor bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — Carries the data for intercomputer communication.
- Dual one-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The Multiprocessor Communications Adapter (MCA) interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of one million bytes per second.

COMPATIBILITY

The Nova 2 Systems are software compatible, given comparable configurations, with all Nova/Supernova computers except the Nova 840. The line is also software

Table 4. Data General Nova 2: System Software

PACKAGE	DESCRIPTION
RDOS	Realtime Disc Operating System, foreground/background multiprocessing, multiprogramming; requires 16K wds memory, S/100 or S/200 CPU, 2.5M disc, console
MRDOS	Mapped Realtime Disc Operating System, requires 24K wds memory, S/200 with MAP, 2.5M disc, console
RTOS	Small basic, real-time, executive, requires 4K wds of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette or mag tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV, runs under RDOS, MRDOS and SOS, requires 8K wds of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV, runs under RDOS or MRDOS, requires 28K wds of memory, CPU, console
ALGOL	Extended ALGOL 60, runs under RDOS or MRDOS, or stand-alone, requires 12K wds of memory, CPU, console
BASIC	2 versions, of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions require 4K, 8K and 16K wds of memory, respectively; CPU, console
Utilities	Text editor, library, loaders, debuggers

compatible with the ECLIPSE line except for a few instructions relating to optional features, like signed hardware multiply divide.

Peripherals from all three lines are interchangeable.

PRICE DATA

Number	Description	Purchase $ (1)	Monthly Maint. $
	DATA GENERAL NOVA 2/4 & 2/10		
	CENTRAL PROCESSORS & WORKING STORAGE		
	Nova 2/4 Processors (4 accs; PIO bus; 17-level interrupt; DMA; 4 additional subassembly slots; rack mountable)		
8331	With 4K Words of Core Memory	3,500	40
8332	With 4K Words of Core Memory	4,000	52
8333	With 16K Words of Core Memory	5,600	64
8334	With 24K Words of Core Memory	7,600	96
8335	With 32K Words of Core Memory	9,100	108
	Nova 2/10 Processors (4 accs; PIO bus; 16-level interrupt; DMA; 10 additional subassembly slots; rack mountable)		
8351	With 4K Words of Core Memory	4,400	44
8352	With 8K Words of Core Memory	4,900	56
8353	With 16K Words of Core Memory	6,500	68
8354	With 24K Words of Core Memory	8,500	100
8355	With 32K Words of Core Memory	10,000	112
	Memories		
8300	Memory with (4K words)	2,000	20
8301	Memory with (8K words)	2,200	32
8302	Memory with (16K words)	3,500	44
	Processor Options		
8306	Power Monitor and Auto Restart	400	1
8307	Multiply/Divide	1,600	13
8308	Automatic Program Load	400	2
8020	Floating-Point Processor	4,000	32
	Packaged Systems		
	Nova 2/10 RTOS Systems		
	System A		
9001	Part 1 consists of 8358 Nova 2/10 Computer (with 16,384-word core memory in tabletop enclosure, 8306 power monitor and auto restart, 4007 I/O interface subassembly, 4010 Teletype/video display I/O interface and 4008 real-time clock)	9,150	102
900XA	Part 2 consists of a 4010A Teletype model 33ASR keyboard/printer (for 9001, 9002, 9003, 9004)	1,750	102
	Nova 2/10 SOS Systems		
	System A		
9005	Part 1 consists of 8353 Nova 2/10 Computer (with 16,384-word core memory and slides for rack mounting, 4007, 4010, 4011 paper tape reader control, 6013 high-speed paper tape reader and 4012 paper tape punch control)	11,000	135
	Part 2 consists of 4010A, 4012A High-speed Paper Tape Punch, and 1012F Single-Bay Rack Cabinet (for 9005, 9006)	5,100	135
	Nova 2/10 RDOS Systems		
	System A		

PRICE DATA (Contd.)

Model Number	Description	Purchase $ (1)	Monthly Maint. $
9011	Part 1 consists of 8355 Nova 2/10 Computer (with 4007, 4010, 4011, 6013, 4046 moving head disc control, 4047 moving head disc adapter and power supply, and 5 remaining slots in computer chassis)	19,450	237
90XXH	Part 2 consists of 4010A, 4047A Moving Head Disc Drive with 1.247 Million Words capacity; 4047C Disc Cartridge, and 1012F Single-Bay Rack Cabinet (for 9011, 9012)	7,900	257
	Dual Nova 2/10 System		
9022	Part 1 consists of 8355 Nova 2/10 Computer (with 8306, 8308, 4007, 4008, 4010, 4119, 4011, 6013, 4240 interprocessor bus, 4046, 4047, and 4 remaining slots in computer chassis)	22,600	510
9022A	Part 2 consists of 40101, 1065F Interprocessor Bus Cable, 4047B, 4047C and 1012G 2-Bay Rack Cabinet	13,400	510
9023	Part 3 consists of 8355 Nova 2/10 Computer 8306, 8308, 4007, 4008, 4010, 4240, 4046, and 4 remaining slots in computer chassis	18,850	510
9023A	Part 4 consists of 4010A, EC4047 Moving Head Disc Adapter and Power Supply Cable, and IC4011 Paper Tape Reader Control Cable	2,250	510

Notes
(1) Nova 2/4 is available only in minimum quantity orders of 5 systems.

HEADQUARTERS

Data General Corporation
Southboro MA 01772

DATA GENERAL

Nova and Supernova Series

OVERVIEW

Data General's Nova and Supernova product line includes 10 Nova systems (Nova, Nova 800, 800 Jumbo, 820, 830, 840, 1200, 1210, 1220, and 1230) and two Supernova systems. The Nova/Supernovas are small-scale, general-purpose, 16-bit computers, oriented toward control, scientific, laboratory, and time-sharing applications.

All of the systems currently marketed are upward compatible and differ mostly in memory speed, price, and packaging. All use the same mass storage units, peripheral devices, and software. The Novas utilize core memories in their basic configurations but can support both read-only memory (ROM) and core memory on a single system. The Supernovas utilize core or read/write semiconductor memory in basic system configurations (a Supernova system with semiconductor memory is called Supernova SC). In addition, each can support a combination of ROM, core, and read/write semiconductor memories.

Core memory cycle time is 800 nanoseconds for the Nova 800, Nova 800 Jumbo, Nova 820, Nova 840, and Supernova, 1.0 microseconds for the 830, and 1.2 microseconds for the Nova 1200, 1210, 1220, and 1230. The Supernova SC has the fastest cycle time: 300 nanoseconds. The first Nova, which is available but no longer marketed, has a cycle time of 2.6 microseconds.

The original members of the product line were the Nova and Supernova systems. As the 1200 Series, 800 Series and Supernova SC were added to the line one at a time, they had clearcut differences in performance. However, Data General has responded to the needs of its user community by adapting options originally aimed at the top of the line (as it was defined at a particular point in time). In this way, most users could benefit.

The high-speed data channel is a case in point. Originally it was an option available only for the two Supernovas. This fact, coupled with the Supernovas' greater memory speeds, made them clearly the top of the line. Now differences between the Nova 800 and Supernova processors have been considerably leveled. In fact, the high-speed data channel is standard for all Novas (still optional on Supernova). The Nova 830 and 840 (which are 800 Jumbos with memory management and protection) are the only models able to expand main memory to 128K words through the new memory management and protection unit.

The memory for the 1200 line (cycle time: 1,200 nanoseconds per word) is available in modules of 4K, 8K, and 16K words. Memories for the 800 line are available in modules of 4K and 8K words for the Nova 800 and 820. The 8K-word module is also available for the Nova 840. The 16K-word module for the Nova 830 has a 1.0-microsecond cycle time.

In addition to 2K, 4K, 8K, and 16K core increments, Novas can increment core with 1K-word modules but Supernova cannot; on the other hand, read/write semiconductor memory increments of 256, 512, and 1,024 words are available only for the Supernova.

There are still a few differences among the 800, 1200, and Supernova Series other than memory speeds, but these are not as distinctive as the capabilities that set the Nova "mapped" 830 and 840 apart from the rest of the line. The memory allocation and protection option, available to all of the Supernova and Nova 800 Series but not to the Nova 1200 Series, functions in a limited way like the 830/840 memory management and protection unit by mapping up to 32K words of memory for time sharing. Tables 1 and 2 list current similarities and differences between Nova and Supernova processors.

The Dual Nova computer system is a dual-processor/shared-disc system, built around two or three standard Data General computers (Nova 1200 Jumbo and Nova 830 or 840), one moving-head or fixed-head disc, and the Real-Time Disc Operating System (RDOS).

The advantages of a dual-processor configuration are continual system availability even when one processor is down, plus shared program and data-base files. The first processor can gather and reduce incoming data and monitor real-time operations. The second processor, used in the background mode, can develop new programs or carry out batch processing. Using the Multiprocessor Communications Adapter (MCA), processors can access each other through the I/O bus.

Where high throughput and continuity are prime considerations, the dual-processor system can handle many communication lines and data rates that peak at unpredictable times. The first processor stores or forwards messages to the second processor for peak times. The second processor shares the message load (doubling throughput), handles peak data rates, and controls the switching if the

Table 1. Data General Nova and Supernova: Common Characteristics

PROCESSOR	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Hardware Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Floating-Point Hardware	Opt
I/O	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
MEMORY	
Min ROM (wds)	256
Max ROM (wds)	31,744
Parity	No
ROM increments (wds)	256; 512; 1,024
SOFTWARE	
Assemblers	3
DOS, RDOS, SOS, RTOS	Yes
Compilers	
FORTRAN	Yes
ALGOL	Yes
Interpreter	
BASIC	Yes

first processor is down. The second processor can also accumulate network statistics, compile management reports, and generate customer service charges.

In a time-sharing situation where common access to programs is needed yet file protection is required, each processor functions as an independent time-sharing system. All terminals can handle Extended BASIC.

For customer service scheduling, the first processor controls the terminals and gathers the customer service requests. The second processor analyzes the data, bills the customers, and performs engineering calculations in batch mode. It also aids the first processor in peak times.

Data General states that the Dual Nova is well suited for supervisory control, front-end processing, data acquisition, point-of-sale systems, hospital patient monitoring, and data entry.

Along with processor development, Data General continues to fill out its line of available mass storage units and peripheral devices and to enhance its software support for the Nova and Supernova. Currently, the firm offers a variety of models and well-integrated hardware and software packages for its minicomputer systems. The company began manufacturing peripherals with the introduction of the Novadiscs, which are a series of fixed-head disc drives with capacities ranging from 128K to 768K words. To date, Data General has added a series of cassette drives, magnetic tape drives, 6013 high-speed paper tape reader, and two CRTs (the 6010 and 6012) to its roster of in-house peripherals. The company also manufactures its own cores.

Data General has developed comprehensive software that will run on both the Nova and Supernova under two types of disc operating systems that have file handling capability. Both disc operating systems, DOS and RDOS, control relocatable assemblers; loader math library; BASIC, ALGOL and FORTRAN compilers; text editor; symbolic debugger; and command line interpreter. DOS was previously the basic operating system. The newer RDOS, a real-time disc operating system, has all of the facilities of DOS as well as foreground/background processing plus multiprocessor and shared disc capabilities. RDOS is now the basic operating system. Subsets of RDOS, called SOS and RTOS, are also available for small stand-alone systems without disc. All of the operating systems will support one of two BASIC interpreters, one for a single user and one for up to 32 time-sharing users. ALGOL 60, and FORTRAN IV can run stand alone or

Table 2. Data General Nova and Supernova: Differences between Models

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830	Nova 840	Nova 1200, 1230	Nova 1210, 1220	Supernova	Supernova SC
PROCESSOR								
Auto Program Load	—	Opt	Opt	Opt	Opt	Opt	Std	Std
Total Subassembly Slots	7	7; 10; 17	17	17	7; 17	4; 10	7	11
MEMORY								
Capacity (K wds)	32	32	128	128	32	24; 32	32	32
Core Increments (wds)	1; 2; 4; or 8K	1; 2; 4; or 8K	16K	8K	1; 2; 4; or 8K	1; 2; 4 or 8K	2; 4; or 8K	2; 4; or 8K
Read/Write SC Memory Increments (wds)	—	—	—	—	—	—	—	256; 512; 1,024
Memory Protect	—	Opt	Opt	Std	—	—	Opt	Opt
Memory Management	—	—	Opt	Std	—	—	—	—
SPEED								
Core Cycle (μsec)	2.6	0.8	1.0	0.8	1.2	1.2	0.8	0.8
SC Cycle (μsec)	—	0.8	—	0.8	1.2	1.2	0.3	0.3
Interrupt Response Time (μsec)	40.0	11.0	—	11.0	17.8	17.8	9.8	9.8
Transfer Rates (K wds/sec)								
DMA	285	1,250	—	1,250	833.3	833.3	500	500
High-Speed Data Channel	—	1,250	—	1,250	—	—	1,250 (opt)	1,250 (opt)

under DOS or RDOS. RDOS also supports a macro assembler and Fortran 5 (a superset of ANSI FORTRAN, IBM Level H FORTRAN, and Univac FORTRAN V). FORTRAN 5 is designed to optimize a user's entire program so that its efficiency compares to a program written in assembly language.

Multiply/divide and floating point are options available to all processors either as hardware units or as software subroutines.

In addition, Data General provides three cross-assemblers to prepare Nova/Supernova programs on the IBM System 360/370, Univac 1108, and CDC 6600 computers. These assemblers are written in FORTRAN and are compatible with the Nova/Supernova extended assembler.

Data General announced the first Nova in September 1968 and the first Supernova in August 1969. Substantial price cuts for the Supernova were made in September 1970. In October 1970, Data General introduced the Nova 800 and 1200 and the Supernova SC memory modules. In May 1971, the Nova 800 and 1200 Jumbos (subsequently the designation for the 1200 Jumbo was changed to Model 1230) were announced. The Nova 820, 1210, and 1220 were announced on November 10, 1971. The Nova 840 was shown at the Fall Joint Computer Conference in December 1972. Recently, (fall 1974) Data General announced that the 830 combines new lower-cost memory modules in the 840 configuration.

COMPETITIVE POSITION

The Nova/Supernova line has been Data General's mainstay for the last few years. It has held its own against stiff competition from companies like Digital Equipment, Hewlett-Packard, General Automation, Honeywell, and Varian. Although the company introduced the microprogrammed Eclipse line in 1974 to replace the Nova/Supernova line and to extend the market upward for Data General computers, the company still plans to keep the Nova/Supernova line current for awhile. Thus Model 830 and a series of lower-cost memories have been introduced to reduce the cost of all systems.

In the development of its systems, Data General has consistently utilized the latest technology to improve the price/performance of its systems; all have the same basic logical design as the first Nova. Thus, all software developed for previous models is compatible with new models, even the new Nova 2 and Eclipse systems, which are compatible in most respects and thus can build on the Nova/Supernova software base. The firm steadily continues to develop system software, and the available software is substantial.

Data General has a large OEM and end-user customer base, which is necessary to support continued system development. An increasing number of small business computer manufacturers are using Nova/Supernova processors as the heart of their systems. In addition, the ROLM Corporation builds a Ruggednova for military applications, and licenses the Nova/Supernova software for it.

Data General claims to be number 2 in minicomputer sales and deliveries, having shipped more systems than any other manufacturer except Digital; the company has a firm grip on around 15 percent of the market. This sales record results from Data General's aggressive marketing combined with its ability to produce and deliver systems with attractive price/performance ratios. Data General markets its systems for all minicomputer applications.

A good mix of hardware/software is available for Nova and Supernova minicomputers. The peripherals equipment complement compares quite favorably to that of competitors (particularly noteworthy is the assortment of disc units, the communications subsystems, and the special peripherals associated with numerical control). The Novadisc was Data General's first peripheral; the company now also manufactures the 6013 High-Speed Paper Tape Reader, the 6010 and 6012 CRT Displays, magnetic tape drives, and the Novacassette.

Nova/Supernova's DOS and RDOS operating systems are versatile in their support of an assembler; BASIC, FORTRAN, and ALGOL compilers; and a command language interpreter. RDOS is noteworthy for its ability to handle dual processors combined with a shared-disc environment and multiprocessor networks.

Data General has experienced some inroads on its Nova/Supernova customer base from the minicomputer's equivalent of the plug-compatible independent. Digital Computer Controls has been marketing a Nova 1200-compatible system, the D-116, which competes indirectly with the rest of the line because the expandability of the system allows memory sizes equal to the Nova 830 and 840. DCC claims to be third in number of systems shipped per month; many of its customers are OEM. Ironically, the popularity of the Nova/Supernova line has been part of Data General's problem; underestimating demand caused the company to slip behind schedule from time to time in the past, and impatient OEM customers bought from the smaller company. This threat is really counteracted more by the Nova 2 (OEM) line, which is competitive in price and comparable in speed. Meanwhile, addition of the Eclipse line, extending into the upper end of the market, provides an attractive upward path for users who anticipate growing systems needs.

Thus, Data General's recent announcements at the upper and lower ends of the market, consistent with the continuing expansion of the Nova/Supernova hardware and software base, put the firm in an aggressive posture

across the entire range of the minicomputer market. Indications are that Data General can hold its own in the marketplace and gradually increase its share at the expense of the weaker, smaller minicomputer manufacturers.

User Reactions

The Data General users interviewed predictably exhibited a wide range of applications and systems sizes as well as a range of reactions to the system.

Installations included a software house with a number of accounting, inventory, order entry, and forecasting systems installed among its customers; a ship voyage accounting firm; a university physics laboratory; and an investment firm.

All users interviewed felt the system was very reliable. One OEM user, a software service bureau with a number of systems, remarked that he had "blown" only two 8K-word core boards in 2 years; other than that, he has had no downtime. Remarks about service showed more variety; several users of various size systems said it was fine; one user said it was excellent (2-hour response time during emergency), while another (small) user reported problems with slow response. The dissatisfied user remarked that several other small users in his area with down systems had occasionally come to "borrow" his system during off-hours. Although this added to his impression of slow service, he added that the system was very reliable and he had no complaints on that score.

User reactions to Data General software were generally positive. A user of RDOS Version III on three Nova 800s (32K words of core each) had previously used DOS 5 but switched operating systems because of the type of file-handling capabilities and the new editing commands; he was quite satisfied with the change. Other users had no complaints about the way Data General's software functioned. One small user, with a 12K-word Nova 1200 system without disc, mourned that Data General's software development appeared to be aimed at larger disc-based systems and nothing seemed to come in his direction. One user stayed with FORTRAN IV rather than buy the additional memory needed for FORTRAN 5; he said his application was I/O-bound not compute-bound, so he did not need optimized code.

CONFIGURATION GUIDE

A basic Nova/Supernova central processor includes four accumulators (two of which can be used as index registers); a single-line, 16-level priority interrupt system; a programmed I/O channel; and a direct memory access (DMA) channel. Supernova processors also include an automatic program load feature initiated from the console; automatic program load is an optional feature for the Nova 800 and 1200 Series. The basic processor includes only add and subtract arithmetic operations; hardware multiply/divide and floating point can be added as options. Each central processor unit is rack mountable or fits in a tabletop enclosure. Table 2 shows the differences in processor submodels.

Working storage for all the Nova/Supernova processors is provided by storage modules that can be added in any combination up to a maximum size of 32,768 words (131,072 words for the Nova 830 and the Nova 840 with a memory management and protection option). All use magnetic core memory except the Supernova SC, which uses semiconductor memory. In addition, read-only memory (ROM) modules are available in 256- to 1,024-word modules. ROM modules and core memory modules can be added in any combination, but total memory size cannot exceed 32,768 words without the memory management and protection option.

Up to 58 I/O devices can be connected to a Supernova and 61 to a Nova. All devices connect to the programmed I/O channel for the transfer of control information. Slow-speed devices such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel or via the high-speed data channel if included in the system. Table 3 lists the various models of peripheral devices available.

Table 3. Data General Nova and Supernova: Peripherals

Device Model	Description
Discs	
4019 A/B/C	Alpha Data (fixed-head), 64K/128K/256K-wd capacity
6000 Series	Nova Discs (fixed-head), 128K, 256K, 512K, 768K-wd capacity
4048A	Century 111, 3M-wd capacity, IBM 2311 compatible
40578	Century 114, 12M-wd capacity, IBM 2314 compatible
4047A/B	Diablo 31/33 (cartridge), 1.2/2.4M-wd capacity
Magnetic Tape	
4030 I-N	Wang magnetic tape transports, 7/9-trk, 12.5/45/75 ips
4000 Series	Nova cassettes, 1-, 2-, or 3-drive versions
6020 Series	7/9-trk dual-head, 75 ips, up to 8 drives/controller
4080 Series	Cassette subsystem, 50K wds/cassette, single/dual triple transports, 7 to 8 transports/controller
Consoles	
4010A-E	Teletype ASR/KSR 33, KSR 35
4023A/E	Teletype ASR/KSR 37
Paper Tape	
4011/6013	Reader, 300 cps
4012A	Punch, 63.3 cps
Punched Card	
4016A-G	Readers, 225/400/150/285/400/600/1,000 cps
4016H-L	Mark Sense Card Readers, 150/285/400/600/1,000 cpm
Printers	
4034A/B	Data Products 356/245 lpm, 80/132 cols
4034C/D	Centronics, 165 cps

Table 3. (Contd.)

Displays	
6010/6012	24 lines, 80 char each, local edit (6012)
4010	Infoton Vista, 20 lines, 80 characters each
A/D, D/A Systems	
4032	Basic A/D Interface, models 4055 A/Q converters, 8 to 15 bits; multiplexors, 2 enclosures (128-single-ended channels, 64 differential)
4037	Basic D/A control, models 4056 A-H, 8 to 14 bits, timing, enclosure for 24 converters
4085	Wide-range analog input, up to 512 channels, 13 to 15 bits
Plotters	
4017 A-D	CalComp 565 drum or rack mountable 563 drum, and 502 flatbed plotters
4017E	General Interface Board
Digital 4065	I/O interface subassembly, 16 input, 16 output lines
Contour 1	Controls 1 to 4 machine tools, 500-lpm feed
4008/4079	Real-time clocks, 10/100/1,000-Hz frequencies
4040	General Interface Board
Communications	
4015	High-speed controller, 600-50,000 baud
4025	IBM 360/370 interface
4038	Multiprocessor communications adapter
4026	TTY MUX, 15 lines
4023	Single channel async interface
4060-4063	Async multiplexors, up to 64 full-duplex lines
4073/4074	Sync multiplexors, 4-line and 1-line versions
4100	Multiline async controller subsystem, up to 1,024 lines

Dual Nova multiprocessor configurations are hardware and software supported. Each processor has 64K bytes of memory and an interprocessor bus for communication between computers. High-level languages and utility software are included. Under RDOS, both computers have on-line access to programs and data files. Hardware-multiplexed data paths allow access to the data base and programs by both processors. Each processor is independent, but both share the same disc data base.

Three types of disc storage available for the Dual Nova configuration are as follows:

- Fixed-head Novadiscs — 256K to 1,536K-byte capacity; up to 8 million bytes of Novadisc storage used for a Dual Nova configuration; provides fast access.
- Moving-head disc with cartridge drives — Removable cartridge model with 2.49 million-byte capacity; one fixed and one removable disc unit with 4.9 million-byte capacity; up to 20 million bytes shared in a Dual Nova configuration; convenient mass storage.
- Moving-head disc pack drives — 24.944 million-byte capacity; almost 200 million bytes accessible in a Dual Nova configuration.

Combinations of fixed and moving-head discs can be used in configurations. Maximum disc storage is obtained with eight moving-head disc packs (200 million bytes) and 8 million bytes of fixed-head storage.

Communication between the two processors is handled via the interprocessor bus. The bus consists of the following components:

- Buffer — Under control of the operating system, the buffer acts as an interlocked communication path between two processors. When the processors both request access to the data files simultaneously, the buffer resolves the conflict.
- Data path — This part carries the data for inter-computer communication.
- Dual 1-second timers — Each computer must restart its timer every second. If it fails to do so, the other computer generates an interrupt, allowing it to usurp total system workload.

The MCA interconnects up to 15 computers in a network through the I/O buses. Any computer can access any other computer, not just the adjacent computer. Data is transferred block-by-block at a rate of 1 million bytes per second. These types of multiprocessor network configurations are software supported under RDOS.

Software packages and the minimum configurations required are listed in Table 4.

COMPATIBILITY

All Nova/Supernova processors are compatible and use the same instruction set as well as the same peripheral and mass storage devices. All currently available software can run on all the Nova/Supernova computers, if the processor can support the required configuration. Software for mapped systems, for instance, must run on an 830 or 840. Cross-assemblers are available so that users with an IBM System/360 or 370, Univac 1108, or CDC 6600 can utilize their more powerful processing capabilities to assemble Nova/Supernova programs. Nova 2 processors are completely compatible with the small processors at the low end of the line.

The Eclipse computer is generally program-compatible with the Nova/Supernova line, given comparable configurations; there are only a few restrictions. Eclipse computers have implemented multiply/divide, hardware floating point, and memory management options differently. In the first two cases the difference is chiefly a matter of coding, which is easy to change. But, memory management is more difficult to alter. Eclipse also uses the codes for "no-load" and "no skip" Nova options for the standard set, so Nova programs with these instructions are not compatible. A compatible program cannot

Table 4. Data General Nova and Supernova: System Software

Package	Description
RDOS	Real-time disc operating system, foreground/background multiprocessing, multiprogramming; requires 16K words of memory, CPU, 2.5M disc, console
RTOS	Small basic, real-time, executive; requires 4K words of memory, real-time clock, CPU, console
SOS	Subset of RDOS for minimum stand-alone, non-disc systems, cassette, mag tape, card or paper tape I/O
FORTRAN IV	Extended ANSI FORTRAN IV; runs under RDOS and SOS; requires 8K words of memory, CPU, console
FORTRAN 5	Superset of FORTRAN IV; runs under RDOS; requires 28K words of memory, CPU, console
ALGOL	Extended ALGOL 60; runs under RDOS or is stand-alone; requires 12K words of memory, CPU, console
BASIC	2 versions of Dartmouth BASIC, 1 for single user calculator mode, 1 for 16 users
Assemblers	Standard, relocatable, and macro versions; require 4K, 8K, and 16K words of memory, respectively, CPU, console
Utilities	Text editor, library, loaders, debuggers

contain the data channel increment, add-to-memory feature, or execution- and I/O-time-dependent subroutines.

All three computer lines use the same type of I/O bus structure; thus all Nova/Supernova peripherals can attach to Eclipse and Nova 2 computers.

MAINTENANCE AND SUPPORT

Data General maintains 38 sales and service centers in 24 states of the United States; eight in Canada; three each in France, England, and Spain; five in West Germany; two in Australia; and one each in Austria, Netherlands, Finland, Denmark, Sweden, Switzerland, Scotland, Israel, Japan, Malaysia, Singapore, Hong Kong, Mexico, Puerto Rico, and Costa Rica. International headquarters are located in France (Paris), West Germany (Frankfurt), England (London), Canada (Hull), and Australia (East Hawthorne-Melbourne). Customer support includes 2 to 10 customer training courses offered at headquarters and selected field locations, the services of hardware/software applications engineers that help users apply their systems, a software subscription service for automatic timely updates of software and documentation, and a summary of available software for users not needing revisions. The Data General Users' Group maintains a library of user-written programs and sponsors informative meetings. The Custom Products Group will quote on design and fabrication of special Eclipse computer interfaces.

Data General provides several levels of hardware maintenance and support. Depot service can be done at reduced rates on a straight time-and-materials basis. For a monthly charge, a factory service contract allows equipment to be rapidly fixed at a repair depot. On-call service contracts provide preventive maintenance checks and high-priority emergency service to the user's site, again for a monthly charge. On-site service is available on a straight time-and-materials basis.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE		
4001	Nova Processor	3,950	34
	Nova Options		
4006	Power Monitor and Auto Restart	400	1
4022	External I/O Cable Connector	250	NC
4024	Expansion Chassis	1,850	10
4031	Multiply/Divide	2,000	16
	Nova Memories (16-bit words; 2.6-μsec cycle time)		
4003	4,096-Word Core Memory	3,650	28
4004	2,048-Word Core Memory	2,700	20
8016	8,192-Word Core Memory	4,100	32
	Nova 800 Processor		
8230	With 4K Words of Core Memory	6,600	53
8231	With 8K Words of Core Memory	8,000	64
8232	With 16K Words of Core Memory	11,200	99
8233	With 24K Words of Core Memory	14,400	134
8235	Jumbo, with 4K Words of Core Memory	7,450	60
8236	Jumbo, with 8K Words of Core Memory	8,850	71
8237	Jumbo with 16K Words of Core Memory	12,050	106
8238	Jumbo with 24K Words of Core Memory	15,250	141
8239	Jumbo with 32K Words of Core Memory	18,450	176
	Nova 820 Processors (with 7 additional subassembly slots)		
8253	With 4K Core Memory	6,100	63
8254	With 8K Core Memory	7,500	74
8264	With 16K Core Memory (2 8K modules)	10,700	109
8285	With 24K Core Memory (3 8K modules)	13,900	144
8286	With 32K Core Memory (4 8K modules)	17,100	179
	Nova 800/820 Processor Options		
8139	Turn-key Console	100	NC
8159	Turn-key Console	125	NC
8206	Power Monitor and Auto Restart	400	1
8207	Nova 800/820 Multiply/Divide	1,000	8
8208	Automatic Program Load	400	2
8209	Memory Protection and Allocation (for Nova 800 only)	3,500	28
8222	External I/O Cable Connector (for Nova 800 only)	250	NC
8224/5	Expansion Chassis	1,850	10
8281	Expansion Chassis (adds 10 I/O subassembly slots)	1,850	10
	Nova 800/820 Memories		
	Core Memory		
8268	4K Words	2,500	24
8269	8K Words	3,200	35
	Semiconductor Read-Only Memory		
8226/77	256 Words	900	9
8227/78	512 Words	1,450	13
8228/79	1,024 Words	1,950	20
	Nova 840 Processors		
8264	With 16K Words of Core Memory (expansion to 64K words)	16,530	134
8265	With 16K Words of Core Memory (expansion to 64K words; wiring only for memory management and protection; includes 2025 jumper card)	13,230	106
8290	With 24K Words of Core Memory (expansion to 64K words)	19,730	169
8291	With 32K Words of Core Memory (expansion to 64K words)	22,930	204
8292	With 40K Words of Core Memory (expansion to 64K words)	26,130	239
8293	With 48K Words of Core Memory (expansion to 64K words)	29,330	274
8294	With 64K Words of Core Memory (expansion to 80K words)	35,730	344
8295	With 80K Words of Core Memory (expansion to 128K words)	45,130	438
8296	With 96K Words of Core Memory (expansion to 128K words)	51,530	508
8297	With 128K Words of Core Memory	64,330	648
8298	With 24K Words of Core Memory (wired for memory management and protection only)	16,430	141
8299	With 32K Words of Core Memory (wired for memory management and protection only)	19,630	176
	Nova 840 Memories		
8269	Core Memory (8K words)	3,200	35
	Nova 840 Processor Options		
8206	Power Monitor and Auto Restart	400	1
8207	Multiply/Divide	1,000	8
8208	Automatic Program Load	400	2
8021	Memory Management and Protection Unit	3,500	28
8222	External I/O Cable Connector	250	NC
8224	Expansion Chassis (adds 7 I/O subassembly slots)	1,850	10
8283	Memory and I/O Expansion Chassis (provides 15 additional slots)	3,000	34
	Nova 830 with Memory Management and Protection Option		

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
8244	With 16K Words of Core Memory	12,650	NA
8245	With 32K Words of Core Memory	16,150	NA
--	With 64K Words of Core Memory	23,150	NA
--	With 16K-Word Memory Board (1.0-μsec cycle time)	3,500	
	NOVA 1200		
	Nova 1200 Processors		
8182	With 4K Words of Core Memory	5,100	40
8183	With 8K Words of Core Memory	5,950	52
8184	With 16K Words of Core Memory	7,550	64
8185	With 24K Words of Core Memory (1 16K module and 1 8K module)	9,550	96
8186	With 32K Words of Core Memory (2 16K modules)	11,050	108
8187	Jumbo with 4K Words of Core Memory	5,950	44
8188	Jumbo with 8K Words of Core Memory	6,800	56
8189	Jumbo with 16K Words of Core Memory	8,400	68
8190	Jumbo with 24K Words of Core Memory	10,400	100
8191	Jumbo with 32K Words of Core Memory	11,900	112
	Nova 1200/1210/1220 Memories		
8120	4K-Word Core Memory	1,800	20
8121	8K-Word Core Memory	2,000	32
8117	16K-Word Core Memory	3,500	44
	Nova 1210 Processors		
8133	With 4K-Word Core Memory	4,000	40
8134	With 8K-Word Core Memory	5,400	59
8140	With 16K-Word Core Memory	7,000	71
8141	With 24K-Word Core Memory	9,000	103
8142	With 32K-Word Core Memory	10,500	115
	Nova 1220 Processors		
8153	With 4K-Word Core Memory	4,900	44
8154	With 8K-Word Core Memory	6,300	56
8165	With 16K-Word Core Memory	7,900	68
8166	With 24K-Word Core Memory	9,900	100
8167	With 32K-Word Core Memory	11,400	112
	Nova 1200/1210/1220/1230 Processor Options		
8106	Power Monitor and Auto-Restart	400	1
8107	Nova 1200/1210/1220 Multiply/Divide	1,600	13
8108	Automatic Program Load	400	2
8122	External I/O Cable Connector	250	NC
8124/5	Expansion Chassis (adds 7 I/O subassembly slots)	1,850	10
8139	Turn-key Console (provides start, continue, reset, and program load functions; for 1200 or 1210 series with 5.25-in. chassis)	100	NC
8159	Turn-key Console (same as 8139 but is for 1210 and 1220 series with 10.5-in. chassis)	125	NC
8181	Expansion Chassis (adds 10 I/O subassembly slots)	1,850	10
	Nova 1200/1210/1220 Memories		
	Semiconductor Read-Only Memory		
8126/77	256 Words	750	8
8127/78	512 Words	1,250	12
8128/79	1,024 Words	1,750	18
8001	Supernova Processor	5,600	54
	Supernova Options		
8006	Power Monitor and Auto-Restart	400	1
8007	Multiply/Divide	1,600	13
8008	Memory Allocation and Protection	3,500	28
8009	High-Speed Data Channel	950	9
8022	External I/O Cable Connector	250	NC
8024	Expansion Chassis (adds 7 additional slots)	1,850	10
8025	Supernova SC Memory Expansion Chassis	1,850	10
8003	4K-Word Core Memory	3,650	30
8015	8K-Word Core Memory	4,900	40
8012	1,024-Word Semiconductor Read/Write Memory	2,800	28
8013	512-Word Semiconductor Read/Write Memory	2,200	22
8014	256-Word Semiconductor Read/Write Memory	1,500	15
8015	8,192-Word Core Memory	4,900	40
8077	256-Word Semiconductor ROM	1,000	10
8078	512-Word Semiconductor ROM	1,550	14
8079	1,024-Word Semiconductor	2,050	21
	Option for All Nova/Supernova Processors		
8020	Floating-Point Processor	4,000	32
	Dual Nova 840 System		
9028	Part 1 consists of 8291 rack-mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4119 precision crystal oscillator for 2,400 baud, 4011 paper tape reader control, 6013 high-speed paper tape reader, 4240 interprocessor bus, 4046 moving-head disc control, 4047 moving-head disc adapter and power supply, 4030 magnetic tape control, and 6 remaining slots in computer chassis)	36,550	784
9028A	Part 2 consists of 40101 20-Line, 80-Char Video Display, 1065F Interprocessor Bus Cable, 4047B Moving Head Disc Drive (with 2.494M-words capacity, 4047C disc cartridge, 4030J magnetic tape transport, and 1012G 2-bay rack cabinet)	19,300	784
9029	Part 3 consists of 8291 Rack-Mounted Nova 840 Computer (with 32,768-word core memory and memory management and protection unit, 8206 power monitor and auto restart, 8208 automatic program load, 4007 I/O interface subassembly, 4008 real-time clock, 4010 Teletype/video display I/O interface, 4240 interprocessor bus, 4046 moving head disc control, and 7 remaining slots in computer chassis)	28,700	784
9029A	Part 4 consists of 4010A Teletype Model 33 ASR Keyboard/Printer, EC4047 Moving-Head Disc Adapter and Power Supply Cable, IC4011 Paper Tape Reader Control Cable, IC4030 Magnetic Tape Control Cable and Major Portion of Supplied Software on Magnetic Tape	2,750	784

HEADQUARTERS

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DIGITAL COMPUTER CONTROLS

D-116 Series

OVERVIEW

The Digital Computer Controls D-116 Series is to the minicomputer market what plug-compatible devices are to the peripherals market. All are software-compatible with Data General's popular Nova 1200 line of minicomputers. The marketing stance for the D-116 line is similar in many respects to that found in the independent peripherals market: users are offered more compact packaging, the same or better speeds, the same or better overall flexibility, lower power requirements, and above all, lower prices. Comparable configurations cost about 15 percent less than Data General systems. The D-116 Series is program- and interface-compatible with the Data General Nova 1200 Series (Models 1200, 1210, and 1220).

The company's successful approach to the minicomputer market was demonstrated fairly quickly after they were formed in 1970. Their first product was the D-112, which was compatible with the Digital Equipment PDP-8. The D-112 was first delivered in August 1970. By the end of fiscal 1972 the company had delivered more than 400 D-112 systems, had begun production of the D-116, and had acquired several subsidiaries. Also, it had become distinctly profitable, in spite of the onset of litigation with Data General. To date, the company has delivered around 750 D-112 systems and 4,200 D-116s.

All of Digital Computer Control's (DCC's) current developmental efforts are centered around the D-116. Previously, the company had followed the simple expedient of purchasing Digital's PDP-8 software for their D-112 Series. However, for the D-116 it established its own software group and began to write systems software. The D-112 is no longer actively marketed although DCC continues to supply it to long-standing customers.

Many of the options that Data General provides for the Nova 800 and the Supernovas, but not the Nova 1200s, have been incorporated into DCC's replacement system: notably, a memory mapping and protection unit allowing attachment of as many as 128K words of core. Table 1 compares the Nova/Supernova Series (including the 1200 Series) with the D-116 systems offered by DCC, while Table 2 notes characteristics common to the computers of both companies' lines.

The D-116 Series uses medium- and large-scale integrated circuits to achieve a processor on a single circuit board. Core memory units are also extremely compact: the 1,200-nanosecond core memory for the D-116 includes a 16K-word module on a single board. The higher speed D-116H system, however, does not have a 16K-word board — the maximum 960-nanosecond single-board size is 8K words. The compactness of the DCC system may be of particular interest to users looking for an OEM minicomputer as a component.

The DCC peripherals closely parallel Data General's. Data General offers few items not available from DCC though software is not yet comparable. Data General has an extremely large body of software that is partly responsible for the popularity of the Nova/Supernova Series. DCC is working steadily to narrow the gap. Operating Systems include MSOS (Mass Storage Operating System), IRIS (Interactive Real-Time Information System) and RTX (Real Time Executive), while language processors include extended Fortran IV ("Fortran 74"), single-user

Table 1. Digital Computer Controls D-116 Series Compared with Data General Nova/Supernova

Characteristic	Nova	Nova 800, 820, 800 Jumbo	Nova 830, 840	Nova 1200, 1230	Nova 1210, 1220	Super-nova	Super-nova SC	DCC-116S	DCC-116H
PROCESSOR									
Auto Program Load	–	Opt	Opt	Opt	Opt	Std	Std	Opt	Opt
Total Subassembly Slots	7	7; 10; 17	17	7; 17	4; 10	7	11	4; 7; 10, or 17	4; 7; 10, or 17
Floating-Point Hardware	Opt	Opt	Opt	Opt	Opt	Opt	Opt	No	No
MEMORY									
Capacity (K wds)	32	65	128	65	24; 65	65	65	128	128
Core Increments (wds)	1,2,4	1,2,4	8K	1,2,4	1, 2, 4	2, 4, or 8K	2, 4, or 8K	4, 8, or 16K	4 or 8K
Read/Write SC Memory Increments (wds)	–	–	–	–	–	–	256;512; 1,024	–	–
Memory Protect	–	Opt	Std	–	–	Opt	Opt	Opt	Opt
Memory Management	–	–	Std	–	–	–	–	Opt	Opt
SPEED									
Core Cycle (μsec)	2.60	0.80	0.80	1.20	1.20	0.80	–	1.20	0.96
SC Cycle (msec)	–	0.80	0.80	1.20	1.20	0.30	0.30	–	–
Interrupt Response Time	40.00	11.00	11.00	17.80	17.80	9.80	9.80	–	–
Transfer Rates (K wds/sec)									
DMA	285	833	833	833.3	833.3	500	500	833.3	–
High-Speed Data Channel	–	1,250	1,250	–	–	1,250 (opt)	1,250 (opt)	No	No
Programmed I/O	Std	Std	Std	Std	Std	Std	Std	Std	Std

Table 2. Processor Characteristics Common to the D-116 Series and the Data General Nova/Supernova

PROCESSOR	
Power Monitor/Auto Restart	Opt
No. of Instructions	202
Hardware Registers	2
Memory Registers	16
Accumulators	4
Word Size (bits)	16
Decimal Arithmetic	No
Hardware Multiply/Divide	Opt
I/O	
Max Devices Addressable	62
Programmed I/O	Yes
DMA Channel	Yes
Interrupt Levels	16
MEMORY	
Min ROM (wds)	256
Max ROM (wds)	31,744
Parity	No
ROM increments (wds)	256; 512; 1,024
SOFTWARE	
Assembler(s)	Yes
Mass Storage Operating System or Systems	Yes
Real-Time Executive or Operating System	Yes
Basic Interpreter(s)	Yes

Basic, multiuser Basic and Assembly Language. The steady expansion of their software base means that DCC can gain an increasing proportion of their revenues from end users, instead of marketing only to OEM manufacturers. The software base has grown substantially since the company's inception, and now is at the point where the system is a serious contender for the minicomputer dollar on its own merit, and not just as a "replacement" for a Data General system.

DCC markets its systems directly through six sales and service centers in the United States and through a number of sales representatives in the United States, Canada, Mexico, Europe, and other parts of the world. U.S. sales representatives include Datatron, Barnhill, Inland Associates, A & D Devices, Computer Complements, Deerland Distributers, Randal Data Systems, Rush S. Drake Associates, and Aloha Associates (Hawaii). Transword Data Systems markets the system in England and France; Aheam & Soper in Canada; Techmation in the Benelux Countries; Teleprint in Germany, Austria, and Switzerland; Datatek oy in Finland; Control y Proceso Electronics in Israel, Greece, Turkey, and Iran.

In addition to the D-112 and D-116 Series, DCC makes a memory expansion unit (add-on memory) that allows the PDP-8L to be expanded from 4K to 32K words. The company also produces a POS register and several other minicomputer-controlled devices.

COMPETITIVE POSITION

The D-116 has, to judge from the rate of deliveries, become one of the most popular minicomputers on the market. DCC claims it ranks third in number of minicomputer systems shipped per month; only Digital Equipment and Data General ship more. A large number of DCC customers buy OEM and do not want to disclose the transaction, so the system has not received the attention from end users that would appear to correspond to its sales record.

In spite of its impressive growth rate, DCC feels it has not lived up to projections, largely because Data General instituted a $20 million lawsuit claiming that DCC "had stolen trade secrets." DCC's countersuits include unfair trade practices, fraud on the patent office, and $23 million dollars in damages — an estimate of the loss in growth caused by the unfavorable publicity of the suit. DCC contends the Data General lawsuit is largely without merit and is a form of harassment. The suit is scheduled for a hearing in February, 1975.

Ironically, one reason for the popularity of the DCC system is that Data General apparently underestimated the demand for its Nova/Supernova line, and as a result of the flood of orders, has had trouble meeting commitments on time. Because of its small size, DCC has been able to tool up to increase delivery rate and to respond to users requiring prompt delivery. The shortage of circuit boards, which has affected the whole industry, may also be part of Data General's problems.

The introduction of Data General's Eclipse line will probably not seriously impact DCC's markets. Eclipse is a more expensive, higher performance system, whereas the D-116 appeals to the user who wants economy and does not need greater speed. The D-116H is slightly slower than the Nova 830 and 840 while D-116S has the same cycle time as the 1200. Data General's Nova 2 is a horse of another color. This system is cheaper, and more compact than the Nova 1200 line, while maintaining compatibility, and Data General has taken pains to make the system attractive to OEMs. DCC will undoubtedly lose some business to the Nova 2, but the company's well-established customer base in the OEM market and gradual expansion of end user business means the company will probably continue to be a contender for the minicomputer dollar.

Although the D-116 is directly compatible only with the Nova 1200 Series, its memory mapping and protection option enables it to compete with the entire line indirectly.

User Reactions

One of the larger users of a D-116 is the manufacturer of a popular key/disc entry system. This user, who purchases around 600 systems a year, switched from Data General to DCC for a number of reasons. First, this manufacturer started making its own memories, and DCC would sell its processor without a memory, while Data General required some memory with its processor. In addition, the long lead time for the Data General systems was getting difficult to accept. Since this key/disc company wrote all its own software from scratch (one of its

strong points in the key/disc market), the amount of available software was of no consequence. The key/disc manufacturer is very pleased with the way the arrangement has worked out. The DCC-116 proved to be compatible mechanically and electrically, no software alterations were needed, service is good, and DCC's accounting department has been responsive to any problems that arose. In addition, this user feels that DCC is attuned to buyers' problems.

Another large user, a manufacturer of point-of-sale equipment, uses the DCC-116 in each store to control the local terminals directly, and at the central supervisory site to communicate with all the controllers in the branch stores. This user switched from Data General to DCC for two reasons: price and the D-116 power supplies, which this user feels are the best he has seen. A careful comparison of the reliability of the two systems in terms of number of man-hours spent to fix defects was made shortly after delivery; both manufacturers were rated good to very good. Data General had the edge over DCC, but the difference in the cost of the few extra man-hours on repair did not equal the amount saved on the DCC systems. This manufacturer found a slight incompatibility in the memory interfacing between his equipment and the DCC memory boards, but the adjustment was very minor. The CPU board, I/O board, interfacing and software were all completely compatible.

A supplier of turn-key graphics systems is using the D-116 as a controller that replaces the Nova used in earlier systems. This company has used six so far and has found no problems with the software originally developed for the Nova. Interestingly, this firm had written all its own software from scratch. The company turned to DCC as its supplier when Data General began having trouble meeting delivery commitments due to the unanticipated volume of business in Novas and Supernovas (the demand for the 800 is apparently particularly out of line with projections). DCC promises faster deliveries and has lived up to commitments. Most of the graphics systems use 32K words of core and an assortment of discs and other peripherals to support the displays. This user was quite happy both with the way the system performed and with service — his only complaint was that the racks for the tape drives bent because they were not sturdy enough for the weight they held.

CONFIGURATION GUIDE

A basic D-116 Series central processor includes four accumulators (two of which can be used as index registers), a single line, 16-level priority interrupt system, a programmed I/O channel, and a direct memory access (DMA) channel, with automatic program load as an optional feature. The basic processor includes only add and subtract arithmetic operations; hardware multiply/divide can be added as an option. Each central processor unit is rack mountable or can be housed in a table-top enclosure.

Working storage for all the D-116 processors is provided by storage modules that can be added in any combination up to a maximum size of 131,072 words with a Memory Management and Protection option. All use core memory, but the core cycle time for the D-116H is 960 nanoseconds as compared to the 1,200-nanosecond cycle time for the 116s. In addition, read-only memory (ROM) modules are available in 256- to 1,024-word modules. ROM modules and core memory modules can be added in any combination, but total memory size cannot exceed 32,768 words without the Memory Management and Protection option.

Up to 58 I/O devices can be connected to a D-116 Series computer. All devices connect to the programmed I/O channel for transfer to control information. Slow-speed devices such as console typewriters, punched card, paper tape, and line printers also use the programmed I/O channel for data transfers. High-speed devices, such as magnetic tape and disc, transfer data via the DMA channel. Table 3 lists individual peripheral devices supplied by DCC.

Table 3. Digital Computer Controls D-116: Peripherals

Model No.	Description
Terminals	
116410 Series	Teletypes, Models 33, 35, & 38 ASR & KSR
116424 A/B	A/N displays — 4,000/1,600 char (25 or 12 x 80) to 9,600 baud
Paper Tape	
116411B	300-cps reader
116412B	75-cps punch
116412D	Combination: 300-cps reader and 75-cps punch
Punch Cards	
116416 Series	150-, 300-, or 600-cpm readers
116416E	Mark-sense reader, 300 cpm
116435	150-cpm punch
Printers	
116434 Series	125-, 35-, 300-, 30-cps printers
116460	600-lpm printer
Plotters	
116417 A/B	Drum plotter — 300 steps/sec; 0.01/0.005-in., 0.1-mm steps
116417C	Drum plotter — 200 steps/sec; 0.005-in.; 0.1-mm steps
116417D	Flatbed plotter — 300 steps/sec; 0.01/0.005/0.002-in., 0.05/0.1-mm steps
116417E	Incremental plotter — 300 steps/sec; 0.01/005-in., 0.25/0.1-mm steps
Discs	
116418	Flexible disc — 128K wds/cartridge
116447 2315-type	Cartridge disc — 1.2M wds/cartridge
116447B/D	One fixed, one removable (2315-type) cartridge disc — 2.4/5M wds/cartridge
Magnetic Tape	
116430 series	NR2I tape drives — 7- or 9-trk; 12.5, 25, 45, or 75 ips
116430 series	PE tape drives — 9-trk; 1,600 bpi; 45 or 75 ips
116461	Cassette drive — up to 125K wds/cassette

Table 3. (Contd.)

Process I/O	
116455 Series	A/D and D/A subsystem — up to 64 single-ended (32 differential) inputs with 8/10/12/13/14/15 bits; or up to 16 single-ended together with 2D/A, or 8 D/A
116456 Series	D/A conversion subsystem — up to 24 D/A converters with 8/10/12/13/14 bits
116466	Digital I/O — 16 input, 16 output lines
116462/116415	Single line interfaces — async/sync
116425	IBM 360/370 programmable interface
116426	16-line async multiplexor
116427	4-line voltage interface — EIA RS2326
116428	4-line current interface — for local teletypewriter
116431	8-line asynchronous line unit — for either voltage or current interfaces
116438	Multiprocessor communications adapter — for up to 15 D-116s
116450	Teletypewriter junction panel — for up to 16 teletypewriters or displays
116451	Model junction panel — for up to 16 lines
116465	4-line synchronous unit
116472	Automatic calling unit — up to 4 dialer interfaces

The two basic processors, the D-116S and the 116H, come in four possible basic chassis having 4, 7, 10, or 17 slots and 4K, 8K, 16K, 24K, or 32K words of memory. All systems can add core modules, but require the Memory Management option to exceed 32K words.

The CPU is on one card (requires one slot). The 4K-, 8K- and 16K-word memory modules (1,200-nanosecond cycle time) fit on one card as well, so a maximum of three slots is used by a basic D-116 system with 24K or 32K words of memory. On the D-116H (960-nanosecond cycle time), however, only 4K- and 8K-word memory modules fit in one card, so a basic system using 32K words of memory takes up five slots. ROM is available for all processors in 256-, or 512-, or 1,024-word increments.

Each processor has a DMA channel as a standard feature, but memory parity checking is unavailable. Among the optional features are hardware multiply/divide, real-time clock, and power monitor with automatic restart. The hardware multiply/divide feature is an external device, but it uses the processor accumulators to hold the operands and the result. The Memory Management and Protection unit is also an external device. The power monitor and auto restart feature provides for orderly power-down and power-up sequences when the power supply is interrupted for any reason.

Especially important interfaces (aside from those for communications interfaces) include a multiprocessor adapter for up to 15 processors and an IBM 360/370 interface allowing the DDC to be adapted to front-end processing.

Software packages, of course, vary in the minimum configurations they require. Table 4 lists the important packages and indicates basic configuration requirements.

Compatibility

The DCC D-116 family is fully compatible with the Data General Nova 1200, 1210, and 1220 minicomputers, but is not completely compatible with the Nova

Table 4. Digital Computer Controls D-116: Basic System Software

Package	Description
Mass Storage Operating System (MSOS)	Combines real-time executive with file manager; requires 12K wds of core, 1 mass storage device (cartridge or floppy disc, magnetic tape), and ASR-33; supports Fortran IV, single-user Basic
Interactive Real-time Information System (IRIS)	Modular data base management system, requires 12K wds of memory, disc, paper tape I/O, real time clock, teletypewriter or keyboard/display.
Real-Time Executive (RTX)	Multi-task monitor, priority-oriented task scheduling; requires 4K wds of memory (resides in less than 2K), real-time clock, and teletypewriter or keyboard/display.
FORTRAN IV	Extension of ANSI Fortran X 3.9-1966 specifications; includes real-time extensions of ISA S61.1/1972 Industrial Computer System Fortran Procedures; core-resident version requires 8K wds of memory; MSOS version (disc resident) requires 8K wds also.
Single-User BASIC	Upward compatible with Dart-mouth BASIC; requires 8K wds of memory, Teletype control, and 1 teletypewriter
Multi-User BASIC	Same as Single-User but allows up to 5 users concurrently; requires 8K wds of memory, Teletype control, and 1 teletypewriter
Relocatable Assembler	Two-pass assembler with third optional verification pass; requires 8K words of memory, Teletype
Editor	Allows user to create, modify, list, and punch source files; requires 8K words of memory
Octal Debug	Relocatable: requires 4K wds of memory and Teletype
Extended Debug	Incorporates symbolic I/O, extensive tracing; requires 4K wds of memory and Teletype
D-116 Loader	Loads assembler or debug object tapes
1200 Series Absolute Loader	Used to load absolute object tapes generated by 1200 Assembler; requires Teletype or paper tape reader

800 or the Supernova. Software requirements for the D-116 Series are identical with those for the 1200 Series, and interchangeability is maintained even through the subassembly level. Finally, peripheral interfaces are also compatible.

MAINTENANCE

DCC provides three basic types of service contracts for purchased systems (DCC systems are not leased): on-call maintenance, an extension of the factory warranty, or the services of a dedicated on-site service engineer. The on-call contract provides for regular preventive maintenance plus on-site emergency repairs for a fixed monthly charge. The warranty extension contract provides for repairs at an authorized service center and for a fixed monthly charge that is approximately half that of the on-call contract. The third contract provides for the full-time services of a trained customer engineer during the prime shift. DCC also provides for non-contract service at the site or at a factory service center.

TYPICAL PRICES

Model Number	Description	Purchase $
	CENTRAL PROCESSORS AND WORKING STORAGE PROCESSORS	
D-116/4	CPU with 4K core memory and 4 slots	2,975
	With 8K	3,365
	With 16K	4,580
	With 24K	6,220
	With 32K	7,285
D-116/7	CPU with 4K core memory and 7 slots	3,640
	With 8K	4,055
	With 16K	5,255
	With 24K	6,890
	With 32K	7,950
D-116/10	CPU with 4K core memory and 10 slots	3,700
	With 8K	4,125
	With 16K	5,320
	With 24K	6,955
	With 32K	8,020
	With 48K	13,700
	With 64K	16,470
D-116/17	CPU with 4K core memory and 17 slots	5,410
	With 8K	6,130
	With 16K	7,330
	With 24K	8,960
	With 32K	10,020
	With 48K	15,770
	With 64K	18,470
	With 128K	29,270
	PROCESSOR OPTIONS	
116806	Power Monitor/Auto-Restart	325
116807	Multiply/Divide	1,430
116808	Automatic Program Load	325
116809	MEU Backplane	50
116810	High-Current Power Supply	150
116824	7-Slot Expansion Chassis	1,350
116825	15-Slot Expansion Chassis	1,650
116880	4-User MEU	3,500
	MEMORY	
116883/03	4K-Word Core Memory	1,800
116884/74	8K-Word Core Memory	2,000
116885/75	16K-Word Core Memory	3,180
116876	PROM Memory (1K wds)	1,575
116876-1	PROM Memory Module (1K words, add-on for 116876)	1,125
116877	RAM Memory. (1K words)	1,225
116877-1	RAM Memory Module (1K words, add-on for 116877-1)	400
	MASS STORAGE DISCS	
116476	I/O Interface Board	150
116418	Flexible Disc Control Interface	1,000
116418A	Flexible Disc Drive	1,350
116418B	Flexible Disc Cartridge	50
116418C	Flexible Disc Chassis Adapter with Power Supply	650
116422	Local Drive Electronics Kit	400
116446	Cartridge Disc Control	3,500
116447	Adapter and Power Supply (power for 2 116447A discs or 1 116447B disc)	1,375
116449	Adapter and Power Supply (same as above for 4)	2,175
116447A	Cartridge Disc Drive (1.2M-word)	5,000
116447B	Cartridge Disc Drive (2.4M-word)	8,000
116447D	Cartridge Disc Drive (5M-word)	6,450
116447C/E	Disc Cartridge	200
	INPUT/OUTPUT MAGNETIC TAPE	
116430	NRZI Magnetic Tape Control	3,500
116430-1	Phase-Encoded Magnetic Tape Control	4,200
116430C/D	Magnetic Tape Transport (7/9-track tapes, up to 45 ips)	5,500
116430E/F	Magnetic Tape Transport (7/9-tk, 12.5 ips, industry compatible)	4,000
116430G	Magnetic Tape Transport (45 ips; 1,600 bpi, PE)	6,750
116430H	Magnetic Tape Transport (75 ips; 1,600 bpi)	8,700
116430I	Magnetic Tape Transport (75 ips; 800 bpi)	8,500
116461	Cassette Loader II	1,850
116475	I/O Interface Board	150
116408	Real-Time Clock	325
116468	Programmable Interval Timer	600
116414/36/65	I/O Interface Board	200
	TELETYPEWRITERS	
116410	Teletypewriter (Current) Interface	150
116476	I/O Interface Board	150
116405	Teletypewriter (Current) Interface	150
116431	Asynchronous Line Unit	800
116431-2	Current Loop Interface	150
116410A	Teletype Model 33 ASR	1,700
116410B	Teletype Model 33 KSR	1,300
116410C	Teletype Model 35 KSR	3,400
116410D	Teletype Model 35 ASR	4,475
116410E	Teletype Model 33 ASR	1,850
116410F	Teletype Model 38 ASR	2,500
	DISPLAYS	
116459	Voltage Interface	50
116424A	Video Display (25-line, 80 char, CRT, EIA interface)	3,000
	PAPER TAPE	
116411	Paper Tape Reader Control Interface (for 116411B)	675
116411B	Paper Tape Reader (300 cps)	1,450
116412	Paper Tape Punch Control Interface	560
116412B	Paper Tape Punch (75 cps)	2,000
116412D	Combination Reader Punch	3,175
	CARD READER/PUNCH	
116416	Card Reader Interface	700
116416A	Card Reader (300 cpm)	2,950
116416B	Card Reader (300 cpm)	3,595
116416C	Card Reader (600 cpm)	4,100
116416D	Card Reader (150 cpm)	2,000
116416E	Mark-Sense Card Reader (300 cpm)	4,295
116435	Card Punch Control	850
116435A	Card Punch (100 cpm)	14,250
	PRINTER	
116436	I/O Interface Board	200
116434	Printer Control Interface	1,135
116434-1	Printer Control Interface	750
116434-2	Printer Control Interface	2,500
116460	Printer Control Board	950
116434B	Printer (125 lpm)	6,000
116434C	Printer (35 lpm)	3,600
116434D	Printer (300 lpm)	8,500
116434E	Character Printer (30 cps)	13,900
116460A	Printer, 600 lpm	2,725
	PLOTTERS	
116436	I/O Interface Board	200
116417	Plotter Control Interface	1,250
116417A	Drum Plotter (12-in. paper)	6,850
116417B	Drum Plotter (rack-mountable version of 116417A)	7,580
116417C	Drum Plotter (30-in. paper)	12,000
116417D	Flatbed Plotter	25,500
116417E	Incremental Plotter	5,000
	DATA COMMUNICATIONS	
	Communication Equipment and Computer Interfaces	
116462	Single Line Asynchronous Interface	350
116415	Single Line Synchronous Interface	1,800
116420	Internal Clock Option	140
116421	Parity Option	200
116425	IBM 360/370 Programmable Interface	4,200
116426	16-Line Asynchronous Multiplexor	800
116427	4-Line Voltage Interface	280
116428	4-Line Current Interface	240
116438	Multiprocessor Communications Adapter	1,900

HEADQUARTERS

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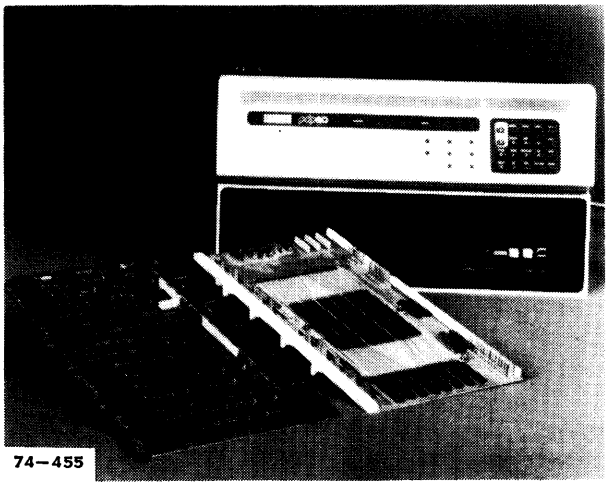
DIGITAL EQUIPMENT CORPORATION

PDP-8/A, 8/E, 8/F, and 8/M



OVERVIEW

The PDP-8 family of computers were the first computers on the market that combined the small size, processing power, and low cost now associated with the whole class of systems termed "minicomputers." Since Digital's original introduction of the PDP-8, the company has continued to develop this 12-bit line, adding new memories, new processors, new peripherals, and a programmable general-purpose register and changing from the positive external bus on earlier models to an internal OMNIBUS®. The OMNIBUS saves space and eliminates back-panel wiring by allowing all system modules (including memory and the CPU) to communicate over the same bus, with the result that any module can be located anywhere along the bus. Because the PDP-8 continues to be popular, a large body of all types of efficient software is being accumulated, resulting in even more user interest. As a result of this developmental cycle, there are more installed PDP-8s than all other minicomputers put together.

The current PDP-8 models, the 8/A, 8/E, 8/F, and 8/M, can all expand the basic memory to 32K words. The 8/E is the top of the line, with all options and peripherals available for expansion of the basic system. The 8/F is a physically smaller 8/E with lower initial power requirements and somewhat less internal expansion capability. The 8/M is basically an 8/F geared to the OEM market. The 8/A is a new MOS system with a compact 1-board CPU for even greater savings to OEM users.

The 8/E-8/F-8/M models use core modules with a 1.2/1.4-microsecond cycle, while the 8/A uses MOS modules with a 2.3/2.8-microsecond cycle. All can attach ROM and PROM modules; all can attach the same peripherals, use the same software, and perform the same functions.

® Registered trademark

Peripherals of every variety are provided for the PDP-8: conventional I/O units for cards and paper tape, including a mark-sense card reader; DECtape or cassette tape as mass storage for small systems, and industry-standard tape for larger storage requirements; fixed- and movable-head disc subsystems for larger systems; terminals, CRTs, and plotters; special-purpose subsystems to handle A/D, D/A, and digital I/O for data acquisition and control applications; and a fairly broad range of communication interfaces for data communication environments.

More than 700 programs are DEC-supported for the 8/A, 8/E, 8/F, and 8/M. Many of these programs were developed by DEC and many by users who also contribute programs to the DECUS (Digital Equipment Corporation Users' Society) software library. Available software includes general operating systems (CAPS — 8-cassette Operating System, RTS-8 Real-Time Operating System, OS-8), a variety of special-purpose operating systems (LAB-8/E, PHA-8, INDAC 8, EDUSYSTEMS, TS8/E time-sharing, COS 300 commercial, and others). Language facilities include BASIC, FORTRAN, ALGOL, FOCAL (a compact interactive language similar to BASIC), DIBOL (a commercial language similar to COBOL) and assemblers. Special application software is available for communication, typesetting, industrial data acquisition, numerical machine control, education, graphic displays, and a variety for scientific laboratory instrument control. The comprehensive OS/8 operating system is an excellent system for combining interactive processing and batch processing; resident core requirements can be as little as 256 words of memory.

History

In 1965, Digital Equipment Corporation (Digital) delivered the first member of its largest family of computers, which has grown to include Models PDP-8, 8/S, 8/L, 8/I, 8/E, 8/F, 8/M, and 8/A. Related members include the LINC-8 and PDP-12. Only the PDP-8/E, 8/F, 8/A, and 8/M and the PDP-12 are in production. All other family members are "traditional" products, that is, products Digital services and maintains but no longer produces. Generally, Digital retrofits new software and peripheral devices to the traditional products in the line. Returned machines are refurbished and sold at prices competitive with those for newer products.

The first PDP-8 went against the trend toward big, complex, expensive computer systems with massive software. It had a short word length (12 bits), modular memory of 4K to 32K words, a 1.5-microsecond cycle time, simple instruction set, flexible I/O structure, and an $18,000 price tag. The system lent itself to many scientific and control applications that did not require the power of the computers supplied by the large manufacturers. PDP-8 sold briskly; over 25,000 computers from the family have been installed to date. Its popularity proved there was a large market for this type of computers, now called minicomputers. In 1966, the PDP-8 was followed by the

PDP-8/S, a slower, smaller, cheaper version of the PDP-8 with a curtailed I/O capability. The 8/S was a highly successful system extending the market to users who did not need the PDP-8's speed. It cost about $9,000 less than the PDP-8.

The PDP-8/S was followed by the PDP-8/I and PDP-8/L in 1968. The PDP-8/I was a redesigned PDP-8 using TTL integrated circuit modules to duplicate the functional capabilities of the PDP-8. PDP-8/I was physically smaller and about $5,000 lower in price than the PDP-8. PDP-8/L was designed primarily for the OEM market. System expansion capability was removed from the PDP-8/L processor chassis, and expansion modules had to be added to the PDP-8/L system before additional core memory and I/O devices could be connected. Originally the PDP-8/L core memory capacity was limited to 8K words, subsequently raised to 12K words, and eventually increased to 32K words, the same as for the other PDP-8 processors. The basic PDP-8/L sold for about $5,000 less than the PDP-8/I.

PDP-8/E, first delivered in 1970, is a slightly faster, more compact, more modular, less expensive version of the PDP-8/I, but with more system configuration flexibility in the lower range where the processor can operate as a sophisticated controller. In addition, the PDP-8/E has features not available on previous PDP-8 models: ROM (read-only-memory) in 256-word modules, an OMNIBUS, additional instructions, and an improved EAE (Extended Arithmetic Element) option. A minimum configuration PDP-8/E can include a processor, a 4,096-word core memory, a minimum control console, and a power supply. The PDP-8/F and 8/M, first delivered in 1970, are smaller, less expensive versions of the 8/E. The 8/F is marketed as an end-user system, while the 8/M is directed toward the OEM market.

Because the 8/E is flexible in the lower ranges, price differences for basic systems of the three core-based models do not show the wide differences found among earlier models. The lowest-priced, minimum configuration 8/E costs little more than minimum configurations for 8/F and 8/M. Prices for the 8/E and 8/F include a programmer's console, while the 8/M price includes only an operator's console. Prices for PDP-8/Ms with PROM memory and operator's console, however, are considerably less. The PROM includes 256 words of read/write memory for each 1K words.

The new PDP-8/A, first delivered in December 1974, departs from the 8/E, 8/F, and 8/M in a number of ways, while essentially retaining both hardware and software compatibility. The PDP-8/A has a CPU with MSI circuitry engineered to fit on a single board, and it uses 1K-, 2K-, or 4K-word MOS memory modules. Both the CPU and memory have slower cycles than the 1.2-microsecond 8/E, 8/F, and 8/M: 1.5 microseconds for the PDP-8/A CPU, 2.0 or 2.3/2.8 microseconds for MOS RAM, 1.5 microseconds for core and ROM, and 3.4 microseconds for PROM. Moreover, the PDP-8/A does not yet have an option corresponding to the Extended Arithmetic Element (EAE), but it is currently under development. These differences may present compatibility problems with some time-dependent or EAE programs and interfaces but, generally speaking, all of the PDP-8 software is available to the 8/A, including the OS-8, RTE-8, and CAPS-8 operating systems. The PDP-8/A minimum prices are well under $1,000 for board only systems; for a CPU and 1K word RAM, unit prices are $895 for a single system and $537 for 100 or more; "boxed" systems with chassis, power, battery back-up for MOS modules and 1K-4K words of memory are in the $1,745 to $1,995 range.

COMPETITIVE POSITION

Despite the proliferation of different minicomputers on the market, the PDP-8 family remains a significant system in Digital's product line and in the entire minicomputer field. It is a dynamic system because Digital keeps the price competitive with new models that reflect current technology, such as the recent addition of the PDP-8/A with its 1-board CPU and MOS memory. Digital also continues to add extensive system and applications software, and interfaces to it almost all of the broad range of mass storage and peripheral devices the company produces. Probably the PDP-8's strongest points in the current market are its enormous body of available software and its wide variety of peripherals. Although other systems have faster cycle times and more efficient hardware architecture, the PDP-8's software is so highly developed that it has circumvented most hardware limitations. The user sees only a highly flexible system that has software on hand for the most diverse applications.

To some extent the low end of the PDP-11 line competes with the PDP-8 for the OEM, process control, communications, and data acquisition markets.

The PDP-11, of course, can be expanded to a powerful system that competes with some of the general-purpose commercial processors. The more extensive communication offerings on the PDP-11 partly reflect the convenience of the 16-bit word in communication networks using standard 8-bit bytes. On the other hand, the PDP-8's 12-bit word is handier for interfacing some types of analog/digital equipment that frequently has 10-bit precision.

Quite apart from inherent characteristics of the two systems, the fact remains that the PDP-8's proven software makes it competitive with many other systems, including the PDP-11, for applications requiring minicomputers of its size.

Its position is doubly unique in that it has the largest share of the market of any single system, and yet it is the only 12-bit system that still retains any sizeable share of the market at all. Other manufacturers have concentrated on 16-bit (or 8-bit or 32-bit) systems that compete more directly with the PDP-11.

At the very lowest end of the market, the PDP-8/A and Digital's MPS both compete for those users who want a 1-board CPU. This market has seen much activity recently due to the new compact memories using both core and semiconductor technologies and advances in microprocessor development. General Automation, Computer Automation, and Data General have all produced 1-board systems that are upward compatible with their major computer lines; consequently, these small systems can take advantage of a body of tested software. All of these are 16-bit systems. Although most of the competing systems have higher performance than the 8/A and some can even fit 1K or 4K words of memory on the CPU board, the 8/A still retains the advantage of its fabulous software base. For users who are not interested in the software, Digital offers the MPS based on the Intel-8 microprocessor, with processor and 1K memory on a board. The MPS has only a Teletype and console for peripherals, and it is not compatible with Digital's other systems, but a PDP-8 cross assembler provides for program development.

USER REACTIONS

We interviewed a number of PDP-8 users, representing several models and a variety of applications. Without exception, all quoted the reliability of the system as one of its strong points. One user waxed enthusiastic on this subject and then said he didn't want to sound like an advertisement, but he had only experienced 1.5 hours of downtime since he obtained the system a year ago. These users also agreed uniformly on the quality of Digital's service organization and the ease with which the system could be fixed. Response to emergency calls was always prompt.

One user, who is a Digital employee, bought a computer for his own use and chose the PDP-8/E partly because he could just remove a module and carry it to a parts depot instead of having an expensive maintenance call. He has not been able to take advantage of this feature yet, however, because in the 1.5 years he has had the system, the only thing he had to fix was a burned-out lamp on the console, which he replaced himself.

Remarks from several users illustrate the maxim that nothing succeeds like success ("to him who has, more will be given," and so forth). One newspaper installation that has been using three PDP-8s (two PDP-8/S computers and one PDP-8/I) since 1968 for classified section updates, justification, and interfacing to an offset printing press would still choose the PDP-8 because so many PDP-8 installations are successful in that industry.

The chemistry department of a university bought its first PDP-8 system to teach majors how to use the computer in research projects; the PDP-8 was chosen because the department was new to minicomputers and Digital could give them the support needed to develop the software and maintain the hardware. A manufacturer of spectrometers chose the PDP-8 as the control component for a number of reasons. Highest on his list was the size of Digital's sales and service organization, which allowed the spectrometer company to market its systems internationally without worrying about maintenance for the computer component.

The breadth of hardware offerings was a factor mentioned particularly among scientific users. The chemistry department mentioned earlier felt this was important because future expansion might take on unknown directions. An independent consulting service developing an inexpensive system for analysis of chromosomal aberrations needed the fully software-supported digitizer/writing tablet/spark pen combination. A PDP-8 at the center of a rapidly expanding system for monitoring pacemakers will have to handle up to 1,000 special terminals by next year. The department ordered a second PDP-8 with computer tape to process complete medical records instead of the abbreviated versions currently used.

Almost all users stressed the variety of software available as a powerful factor in selecting the PDP-8. The spectrometer manufacturer wanted a maximum number of routines to choose from so that he had a minimum amount of work to do himself. The Digital employee wanted an efficient high-level language on a 4K machine and was attracted by the FOCAL interpreter. The chemistry department wanted as much help as possible because of its inexperience.

A high school implementing a computer-related mathematics program needed an inexpensive system that could provide the BASIC language. Only the newspaper was not taking advantage of Digital's software; a software house developed the software six years ago, at the time of the initial acquisition.

Last, but hardly least, was the cost of the system. The PDP-8 has remained competitive in price and won the previously-mentioned high school math department contract by bidding to a set of specifications. Price was also an essential element to the laboratory programming for chromosomal aberrations. The big problem here was not how to detect, analyze, and interpret, but how to make the procedure cost-effective enough to become a widely available service. Competitive pricing was quoted as a factor of varying degrees of significance to each of the users.

CONFIGURATION GUIDE

All basic PDP-8/E, 8/F, and 8/M computers use the same KK8-E Central Processor, power supply, chassis, and OMNIBUS with 20 quad bus slots. Basic systems also include memory modules, mounting, and an operator interface (either an operator's or programmer's console) and TTY control combinations. The PDP-8/E has two sets of submodels with identical specifications: one set has an on-site warranty and one set has a factory warranty. In addition, all submodels on all processors can connect to 115- and 230-volt power sources.

Memory can expand in increments of 4,096 words for core and 256 words for ROM on the 8/E, 8/F, and 8/M.

ROM and core memory can be intermixed in any desired combination, but a memory extension control is necessary when total memory exceeds 4,096 words. Maximum memory on all current PDP-8 systems is 32,768 words.

A basic PDP-8/E, 8/F, or 8/M computer uses eight to 11 of the 20 standard OMNIBUS quad slots in the basic system: central processor, five slots; programmer's console (if included), one slot; 4K-word memory, three slots or 8K-word memory with extension control, four slots; and Teletype control (if included), one slot. The operator's panel on 8/M systems does not require an OMNIBUS slot.

All 8/E, 8/F, and 8/M processors can optionally attach an Extended Arithmetic Element (EAE) and a Floating-Point Processor (FPP). Both are high-speed asynchronous hardware modules that attach to the OMNIBUS like peripheral devices. EAE performs division, multiplication, and other mathematical functions, and FPP performs floating-point and double-precision arithmetic. Both EAE and FPP increase processor throughput indirectly, because OS/8 systems equipped with these modules greatly expedite FORTRAN IV compilations and runs.

A basic 8/E system can be expanded within the main chassis through the BE8A OMNIBUS expander, which adds 18 more usable slots. In addition, a BA8 System Expander Box allows the OMNIBUS to be expanded by 18 more slots outside the chassis. The BA8 itself can be expanded by 18 additional slots for a maximum of 76 slots per 8/E system. Because the 8/F and 8/M models have smaller chassis, the internal expansion option is not available to them, and these models can expand only up to 56 slots through an external BA8 expanded to full capacity.

The PDP-8/A fits on a single 15 by 8.5-inch "hex" size board, housed in an eight-slot chassis. It can attach its own version of almost all 8/E, 8/F, and 8/M options and all of the same peripherals, except the KE8-E Extended Arithmetic Element, the AD8-E Extended Arithmetic Element, the AD8-E Analog-to-Digital Converter and MUX control, and the AM8-EA MUX and preamplifiers. The slower memory cycle of the PDP-8/A CPU (1.5 microseconds) may affect certain time-dependent PDP-8/E interfaces. Autostart is a standard feature which must be switched off if the 8/A's own power-fail/auto restart option is included.

The PDP-8/A uses 1K-, 2K-, and 4K-word MOS memory modules with 2.0 or 2.3-microsecond read and 2.8-microsecond write cycles; each module requires one slot. A special 1.5-microsecond core board is also available for the 8/A. Like the 8/E, 8/F, and 8/M, the PDP-8/A requires the KM8-A extended option board to expand memory beyond 4K words. The KM8-A also includes the PDP-8/A's power fail/auto restart option, time share control to distinguish between user and monitor modes, and a bootstrap loader. ROM memory can be added in 1K-, 2K-, or 4K-word increments, and PROM is added in 1K-word increments. Both ROM and RAM can be included on a system.

The DKC8-AA option board adds a Serial Line Unit, a Parallel I/O interface, a 100-Hertz crystal-controlled real-time clock, and a programmer's console control. The KC8-AA programmer's console is newly designed for the 8/A, with a 5 by 4-inch key pad and LED octal readouts.

The PDP-8/A-100 is offered in three packaged models that differ in the type of memory used, slots available, and power supply. The 8/A-100 is a 10-slot system, with either a 20 amp, ± 5 volt power supply, or a 1 amp, ± 15 volt power supply, battery backup for the entire system for 1 to 7 minutes, operator's panel, and chassis. Memory can be the same ROM, RAM, and PROM modules discussed for the 1-board system.

The PDP-8/A-200 is a 12-slot system with the same power options as the 8/A-100, but it has a 1-hour battery backup for the memory only. All other basic system components are the same as the 8/A-100, except that the 8/A-200 has the option of attaching a 4K-word MOS board using 4K chips with a 2.0 microsecond cycle.

The 8/A-400 system is a 12-slot system like the 8/A-200, but with 25 Amp, ± 5 volt power, no battery backup and core memory. The core board, with a 1.5-microsecond cycle time, is not compatible with the 8/E, 8/F, and 8/M systems.

No bus extensions are allowed for any of the PDP-8/A systems. Mainframe specifications are given in Table 1.

A variety of standard peripherals can be attached to any PDP-8. These are summarized in Table 2. There are some limitations on the numbers of special interfaces that can be attached to any PDP-8. Only one KA8 external interface for positive I/O devices need be attached per system. This interface can handle all traditional positive I/O bus devices. A maximum of 12 Data Break (DMA) Interfaces are allowed, with one interface per device. Up to eight DB8 Interprocessor buffers or DR8 12-channel buffered digital I/O interfaces can be attached. The maximum number of KL8-E or J Serial Line Interfaces per system is 17.

Each DB8-E interprocessor buffer allows two or more PDP-8s to exchange data. The sending computer loads the buffer from the accumulator and sets a flag in a receiving computer. Transfers are one word at a time as the receiving computer senses the set flag.

Digital has a specially-priced prepackaged system for use with the OS/8 operating system. This includes a PDP-8/E with memory extension control and time-share option, 8K or 16K words of core memory, cassette bootstrap loader, dual drive cassette system, disc cartridge system, DECwriter data terminal with a parallel interface and freestanding cabinet.

Each major software package has minimum configuration requirements. Table 3 summarizes PDP-8's system software and the configuration requirements of the major packages.

COMPATIBILITY

Generally, the various members of the PDP-8 family are compatible with comparable configurations from one model to the next. In some cases, however, users' software must be reprogrammed for an improved optional feature, such as the PDP-8/E EAE (Extended Arithmetic Element), which differs significantly from previous EAE options. This option uses some of the instruction codes previously available for microcoding the Operate instructions.

The Positive I/O Bus Interface allows peripherals originally designed for the PDP-8/I, 8/L, and 8/S systems to be attached to the OMNIBUS on the PDP-8/E, 8/F, and 8/M. Because the PDP-8/A uses an OMNIBUS similar to the 8/E and it can attach the Positive I/O Bus, nearly all PDP-8 peripherals can attach to the 8/A. Exceptions are the A/D converter and its related MUX. The 8/A is slower than an 8/E, and also does not have an EAE like the 8/Es. These may create some compatibility problems with time-dependent programs and interfaces.

Table 1. Digital Equipment PDP-8: Mainframe Specifications

MODEL	8/E, 8/F, 8/M	8/A
CENTRAL PROCESSOR		
Microprogrammed	No	No
No. of CPU boards	5	1
No. of Registers	5	5
Addressing		
Direct	256	256
Indirect	1 level to 4K	1 level to 4K
Indexed	1 level "auto index"	1 level "auto index"
Instruction Set		
Number (std; opt)	56; 72	56
Extended Arithmetic	Yes, option	No
Decimal Arithmetic	No	No
Floating Point	Hardware option	Hardware option
Priority Interrupt Levels	1	1
MAIN STORAGE		
Type	Core	MOS; core
Cycle Time (μsec/wd)	1.2; 1.4 (2 accesses)	2.3 read, 2.8 read/write (MOS); 1.5 (core)
Basic Addressable Unit	12-bit wd	12-bit wd
Bytes/Access	2 (6-bit)	2 (6-bit)
Min Capacity (wds)	4K	1K
Max Capacity (wds)	32K	32K
Increment Size (wds)	4K; 8K	1K; 2K; 4K
Ports/Module	1	1
Parity	Option	Option
Protect	Software or ROM	Software or ROM
Memory Management	To 32K	To 32K
ROM		
Use	Program protection	Program protection
Capacity (wds/module)	256	1K-32K/system
PROM	1K-wd module	1K-wd module
INPUT/OUTPUT		
Programmed I/O	Yes	Yes
DMA Channels (no.)	1-12	1-12
Multiplexed I/O	No	No
Data Break (for positive I/O devices)	Option	Option
Max DMA Transfer Rate (wds/sec)	833,333	333,333 (MOS), 833,333 (core)

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks in the United States and worldwide, numbering more than 1,500 engineers.

Table 2. Digital Equipment PDP-8: Peripherals

MODEL NUMBER	DESCRIPTION
DISCS	
DF32/DS32	Fixed Disc, 32K wds/drive, 4 drives/controller
RF08/RS08	Fixed Disc, 262K wds/drive, 4 drives/controller
RK8/RK05	Disc Cartridge System, 1.6M wds/drive, 4 drives/controller
MAGNETIC TAPE	
TC08/TU56	DECtape, 8 drives/controller
TD8/TD8-E	Dual DEC cassette, 75K-byte capacity/cassette, 8/system
TM8/TU10	7- and 9-trk DEC MAGtape drives, 8 drives/controller
CARDS	
CM8	Optical Mark Card Reader, 300 cpm
CR8	Punch Card Reader, 300 cpm
PAPER TAPE	
PR8	Reader
PP8	Punch
PC8	Combination Reader/Punch
PRINTERS	
LS8	Dot Matrix Printer, 165 cps
LE8	Line Printers, 173-356 lpm
LS01	Printer for VT8 Display, 165 cps
TELETYPEWRITERS	
LT33/LT35	ASR & KSR Teletypes, 10 cps
LA30	DECwriter, 30 cps
DISPLAYS	
VT8	Alphanumeric and Graphics Display
VC8/VR14, VR20	Plot Display, Subsystem, B & W or 2-color display
VT05	A/N Terminal 1,440 Char (72 x 20)
PLOTTERS	
XY8 Series	CalComp 565, 563, and Houston Instruments DP-1, DP-10
TERMINALS	
RT01	Numeric Data Entry Terminal, 16-digit display
RT02	Alphanumeric Data Entry Terminal, 32-digit display
WRITING TABLETS	
VW01 Series	Tablets, 4 multiplexors/control
COMMUNICATIONS	
KL8 Series	Async Line Interface, 110-2,400 baud models
DP8	Sync Modem Interface
DC08	ACU and 10-channel Multiplexor
PROCESS I/O	
AD8	10-bit Subsystem, up to 16 chan
AD01	10-bit Subsystem, up to 32 chan
AF04A	Integrated Digital Voltmeter, to 128 chan
AFC8	Low-Level Differential Analog Input Subsystem, up to 128 chan
AA50	Digital-to-Analog Subsystem, up to 6 chan
UDC8	Digital I/O to 192 digital pts

Aside from 46 sales and service locations in the United States, Digital has five offices in Canada, six in Australia, five in Germany, six in the United Kingdom, three in Brazil and one or two each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, Netherlands, New Zealand, Norway, Phillipines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users, requiring considerably less software support and applications programming assistance than the large commercial system users, this picture is changing, as evidenced by Digital's recently-added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour shifts. An on-site engineer can be hired if requirements are critical, or a user can buy an on-call service or set up his own maintenance staff.

Table 3. Digital Equipment PDP-8: Software

PACKAGE	DESCRIPTION
OS-8	Standard PDP-8 operating system for batch and interactive processing, requires 8K-wd memory, cassette I/O and bootstrap, disc, and DECwriter terminal
RTS-8	Real-Time multiprogramming system
CAPS-8	For small cassette-based system, requires 4K-wd memory, 2 TU-60 cassette drives, teletypewriter
TS8/E	Time-sharing system for up to 17 users, requires 8K-wd memory, KM8-E Interface
COS-300	Commercial operating system, requires 8K-word memory, discs, console, printer; can operate in foreground/background mode
BASIC	9 different packages: EDU System 10, 20, 28, 30 versions using OS/8, CAPS-8, LAB 8/E, Industrial real-time BASIC, Dartmouth BASIC. Various requirements range from 4K-12K-wd memories, all require LT33-D or LA30-P terminals, some require PC8-E, others require RK8-E disc, TU56 tape, or DECtape
FOCAL	Interactive language for small computers, requires 4K-wd memory, LT33-D terminal
FORTRAN, FORTRAN IV	FORTRAN in stand-alone or OS/8 versions, FORTRAN IV for OS/8, all require 8K-wd memory, PC8-E, LT33-D or LA30-P terminals, OS/8 versions read disc
DIBOL	COBOL-like language for 8K-wd system under OS/8
ALGOL	From DECUS; ALGOL 60 subset of ALGOL-8
Assemblers	PAL III or PAL C/Macro-8 require 4K-wd memory, and LT33-D terminal; SABR stand-alone, OS/8, PAL-8, CAPS-8, PAL-C. and OS/8 SABR need 8K wds of memory
Utilities	4 Symbolic editors, 3 floating-pt package, libraries, editors, loaders, debuggers, diagnostics, many others
EduSystems	For hands-on classroom use with BASIC or FOCAL single-user to 8 users and batch versions (several versions)
Typeset-8	Several typesetting systems for justifying, hyphenating, etc.
COGO-8	For interactive graphics control, requires 16K-wd memory, OS/8, 2 DECtape drives, DECwriter
LAB-8	Signal Averaging System for 8/E with 10-bit A/D, 10-bit plot display controller, clock, lab panel, and ASR-33
Communications	Programs for concentration, message switching, data collection, remote batch

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	SYSTEMS		
STD8E CA/CB	Packaged Hardware/Software System RK8-E Cartridge Disk System TA8E DECcassette with dual drives PDP-8/E Central Processor (8K words) Decwriter MI8-EL Bootstrap for DECcassette H960-BC Cabinet OS/8 Operating System on Cassette	18,000	232
STD8E CC/CD	Same as STD8E-CA/CB Except with 16K Words of Memory	20,000	275
LAB8E-05	The LAB8E-05 PDP-8/E-PA Tabletop PDP-8/E (4K memory) H945-AA Laboratory Data Panel (tabletop) LT33-D ASR-33 Teletypewriter and Punch AD8-ES 10-Bit A/D Converter VC8-E 10-Bit Point Plot Display Controller DK8-ES Real-Time, Programmable Clock LAB8E Software Kit	9,760	117

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
LAB8E BA/BB	Laboratory System for General-Purpose Computing PDP-8/E-NE/NF Central Processor (8K-word core memory; terminal control) LT33-DC/DD ASR 33 Terminal AD8-EA A/D Converter AM8-EA 8-Channel MUX and Preamps AM8-EC Control Panel DK8-ES Programmable Clock, Schmitt Triggers, and Front Panel VC8-E Scope Controller H945-AB/CB Cab Mounting Panel H960-BB/CB Cabinet LAB8E Software Kit	13,470	151
OS/8-10	Complete Hardware/Software System PDP-8/E1AE Central Processor (8K-word core memory) DECwriter Terminal MR8-EC Bootstrap Loader TD8-EM Dual DECtape Drives H967-BA Cabinet H952-HA Table OS/8 System Software	14,400	161
LAB8E-15	System PDP-8/E-NE — Rack-Mountable PDP-8/E; 8K Memory less Teletype Control PC8-E — High-Speed Paper Tape Reader/Punch DECwriter — Terminal H945-AB — Laboratory Data Panel; Rack Mountable VC8-E — 10-Bit Point Plot Display Controller AD8-EA+AM8-EA+AM8-EC — 10-Bit A/D Converter; 8-Channel Multiplexor DK8-ES — Real-Time Programmable Clock VR14 — 7 x 9" Point-Plot CRT H960-BB — 19" Freestanding Cabinet QF060-AB — LAB8E Paper Tape Software Kit	20,000	202
LAB8E-25	System PDP-8/E-NE — Rack-Mountable PDP-8/E; 8K Memory less Teletype Control BE8-A — 20-Quad-Slot OMNIBUS Expander DECwriter — Terminal H945-AB — Laboratory Data Panel (rack mountable) VC8-E — 10-Bit Point-Plot Display Controller AD8-EA — 10-Bit A/D Converter; 8-Channel AM8-EA/EC — Multiplexor DK8-ES — Real-Time Programmable Clock VR14 — 7 x 9" Point-Plot CRT MR8-EC — 256-Word OS/8 Read-Only Memory TD8-EM — OMNIBUS DECtape Control and Dual DECtape Drive H952-HA — Programmer's Table H960-BB — 19" Freestanding Cabinet OS/8 Software Kit; OS/8 Extension Kit; OS/8 LAB-8/E Software Kit	22,600	218
	CENTRAL PROCESSORS AND WORKING STORAGE		
PDP-8/E-AA/AB*	Computer (4K-core memory and Teletype control; rack mountable; slides included) KK8-E Central Processor MM8-E 4K Core Memory KC8-EA Programmer's Console KL8-E Console Teletype Control Combination Power Supply, Chassis, and OMNIBUS with 20-Quad Bus Slots	4,490	53
PDP-8/E-AE/AF*	Same as PDP-8/E-AA (except MC8-EJ 8K core memory and memory extension control)	5,650	74
PDP-8E-AS	Same as PDP-8/E-AE (except with MM8-EJ 8K core memory added for total of 16K)	7,670	117
PDP-8E-AT			
PDP-8/F-AH/AJ	Same as PDP-8/E-AA (with KC8-EA replaced by KC8-FL programmer's console)	3,990	53
PDP-8/F-AK/AL	Same as PDP-8/F-AH (except with memory extension control and MM8-E core replaced by MC8-EJ 8K core memory)	5,150	74
PDP-8/F-AS/AT	Same as PDP-8/F-AS (with MM8-EJ 8K core memory module added for total of 16K)	6,870	117
	PROCESSOR OPTIONS		
KE8-E	Extended Arithmetic Element (EAE)	1,200	5
KP8-E	Power Fail Detector and Auto Restart	270	2
FPP12-AB	Floating-Point Processor (24 + 12 bits; supporting software requires min OS/8 configuration)	8,500	51
FPP12-AE	Double-Precision Option for FPP12-AB only (provides 60 + 12 bits capability)	2,700	16

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	MEMORY OPTIONS		
	CORE MEMORY		
MM8-EJ	8K-Core Memory Expansion	3,900	
MM8-E	4K-Core Memory Expansion	2,500	
KM8-E	Memory Extension & Time-Share Control	350	
	READ-ONLY MEMORY		
MI8-E	Hardware Bootstrap Loader	540	
MR8-EC	256-Word OS/8 ROM and Bootstrap for TD8-E Systems	860	
	MASS STORAGE		
	Discs		
DF32-DP/EP	Fixed-Head Disc File and Control; 32K Words; Controls up to 3 DS32-D Disc Expanders	7,000	32
DS32-D/E	Disc Expander (32K words)	4,000	16
RK8-EA/EB	Disc Cartridge System (controller and 1.6M-word drive; supports up to 3 additional RK05 drives)	7,900	74
RK05-AA/BB	Disc Cartridge Drive (1.6M wds)	5,100	64
RK05K-8	Disc Cartridge	99	—
	INPUT/OUTPUT		
	Interfaces		
KA8-E	External Interface for Positive I/O Devices (max 1/system)	270	3
KD8-E	Data Break Interface (max 12/system)	540	3
DR8-EA	Twelve-Channel Buffered I/O Interface	540	5
	CLOCKS		
DK8-EA	Fixed Interval Clock, Line Frequency	270	2
DK8-EC	Real-Time Clock (fixed interval; crystal frequency)	320	2
DK8-EP	Real-Time Clock (programmable)	700	3
DK8-ES	Programmable, Real-time Clock (with 3 Schmitt triggers and control panel)	1,350	5
	TERMINALS		
	All Terminals Require KL8-JA Interface		
LT33-CC/CD	KSR 33 Keyboard	1,400	32
LT33-DC/DD	ASR 33 Sync	1,850	37
LA36-CA/CB	DECwriter Data Terminal (300 cps; 132-col; 96-char uc/lc; 110, 150, & 300 baud)	1,850	
VT05B-AA/AD	A/N Display with Keybd	2,795	23
VT50-AA	DECscope Video Terminal	1,250	22
	CARD READERS		
CM8-FA/FB	Optical Mark Card Reader and Control (300 cpm)	5,290	53
CR8-FA/FB	Punched Card Reader and Control (300 cpm)	4,860	53
	PAPER TAPE		
PC8-E/EA	Combination Paper Tape Reader/Punch and Controls (rack mountable)	3,900	37
	LINE PRINTERS		
LS8-FA/FB	Line Printer and Controller	5,615	58
LV8-BA/BB	Electrostatic Printer/Plotter	11,770	53
LE8-VA/VD	Line Printer and Controller	9,900	72
LE8-WA/WD	Line Printer and Controller	11,900	72
	MAGNETIC TAPE		
TA8-AA/AB	DECcassette System	2,990	40
TD8-EH	OMNIBUS DECtape Control and Single DECtape Drive	4,000	32
TD8-EM	OMNIBUS DECtape Control and Dual DECtape Drive	5,500	42
TM8-EA/ED	DEC Magtape Drive and Controller (9-track)	10,745	101
TM8-FA/FD	DEC Magtape Drive and Controller (7-track)	12,500	101
	PLOTTERS		
XY8-E	Plotter Control Module Only	540	8
XY8-EK/EL	Incremental Flatbed Plotter and Control	3,995	23
XY8-EH/EJ	Incremental Flatbed Plotter and Control	3,995	23
	GRAPHIC DISPLAYS		
	DISPLAYS		
VC8-E	Point-plot Display Control	1,185	11
VR14	CRT Display (7 x 9" point-plot)	3,240	19

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	DATA COMMUNICATIONS		
KL8-JA	Async Serial Line Interface	425	11
KL8-M	Modem Control Interface (for Bell 103 and 202 modems)	400	5
H308	Null Modem Adapter (needed when a modem is not used)	65	—
DP8-EA	Sync Modem Interface (for Bell 201 modems)	1,620	11
DP8-EB	Sync Modem Interface (for Bell 300 modems)	2,000	11

— Not Applicable

HEADQUARTERS

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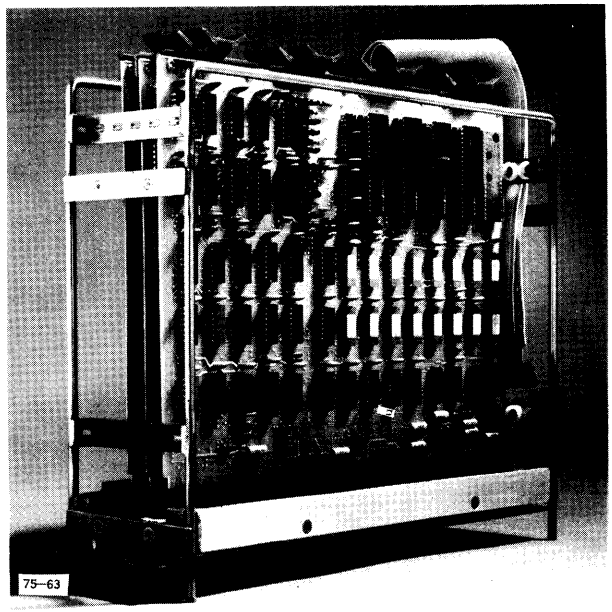
DIGITAL EQUIPMENT CORPORATION

LSI - 11



OVERVIEW

With the introduction of the LSI-11, Digital continues to reaffirm the company's policy of providing more computing power at less cost. This new entry in the popular PDP-11 product line (over 17,000 installed) occupies a unique position; it is a microcomputer that implements the PDP-11/40 instruction set and offers the performance of the PDP-11/05. In quantities of 100, an LSI-11 processor with I/O bus, 4K-word MOS random-access memory (RAM), real-time clock, single-level interrupt, and power fail/auto restart for stand-alone operation costs $684. All components are mounted on one 8.5 by 10-inch board. Table 1 lists mainframe characteristics.

The LSI-11 processor is contained on four silicon, N-channel metal oxide semiconductor (MOS) chips. The chip set includes one 40-pin control chip, one 40-pin data chip, and two 40-pin microcoded microms (microcoded read-only memories). A socket for an optional fifth chip to implement extended fixed-point and floating-point arithmetic is provided. Western Digital, a company that is in the calculator business and produces thousands a month, supplies the chips. The first LSI-11 deliveries have already been made, and volume deliveries should begin this summer.

The LSI-11 system is aimed at the OEM market and high-volume end users. It is designed for easy interfacing to machines, instruments, and terminals. Digital expects to penetrate markets in business, communications, education, health, industrial control, laboratory automation, process control, and transportation.

The microcomputer can support two I/O modules and four expansion memory serial interface modules. The I/O modules are the DLV11 serial module and the DRV11 parallel module.

The DLV11 provides for 20mA current loop or EIA interfaces. Jumper-selectable transmission rates (50 to 9,600 baud) and codes are available. The DLV11 is pin, signal, and software compatible with the DL-11C interface available on other PDP-11s.

The DRV11 is a general-purpose, 16-bit parallel interface between the LSI-11 bus and a peripheral device. The DRV11 is pin, signal, and software compatible with the DR11-C available for the other PDP-11s.

Basic memory is a 4K-word MOS RAM, but expansion memory modules are also available: 4K-word core memory, 1K-word static RAM, 4K-word dynamic RAM, and 4K-word programmable read-only memory (PROM/ROM) available in 256- and 512 word increments.

Software consists of a paper tape operating package resident as a basic utility. It includes an assembler, an editor to create and modify ASCII source files for input to system programs, loader, on-line debugging package, and I/O executive. Programs can also be developed on other PDP-11 systems via an Emulator package that runs on the PDP-11/35 and 40, which have instruction sets identical to the LSI-11. The configuration must include a PDP-11/35 or 11/40 processor with 16K-word memory,

Table 1. Digital Equipment Corporation LSI-11: Mainframe Characteristics

MODELS	
CENTRAL PROCESSOR	KD11-F
Microprogrammed	Yes
No. of Registers	6 general, 1 stack pointer, 1 program counter
Addressing (no. of wds)	
Direct	32K
Indirect	32K
Indexed	32K
Mapping	No
Instruction Set	Same as PDP-11/40
Implementation	Microcode
Types	Singleword
Number	400
Floating Point	Opt
Hardware Stack	Yes
Instruction Execution Times (μsec)	
Fixed Point	
Add	3.5 (reg to reg); 12.0 (memory to memory)
Multiply	24-64 (memory to reg)
Divide	78 (memory to reg)
Floating Point (1)	
Add/Subtract	42.0
Multiply	52-92
Divide	151
Writable Control Store	No
Interrupts	
Levels	1
Type	Hardware
MAIN STORAGE	
Type	RAM;core; PROM/ROM
Speed	350 nsec access time (RAM); 1.2 μsec cycle time (core); 70 to 80 nsec access time (PROM/ROM)
Basic Addressable Unit	Byte/word
Bytes/Access	2
Cache Memory Capacity (bytes)	No

Table 1. (Contd.)

MAIN STORAGE (Contd.)	
Min	8K (RAM); none (core); none (PROM/ROM)
Max	64K (RAM); 64K (core); 8K (PROM/ROM)
Increment Size (bytes)	2K/8K (RAM); 8K (core); 512K/1K (PROM/ROM)
Ports/Module	1
Error Checks	No
Memory Protection	No
Memory Management	No
Interleaving	No
INPUT/OUTPUT	
Max Devices Addressable	No practical limit (4,096)
Programmed I/O	Yes
DMA	Yes
DMA Transfer Rate	833K wds/sec
Price	$634 in quantities of 100

Note:
(1) Two-word operands.

memory management control option, disc storage, paper tape reader/punch or cassette tape, and printer or CRT terminal.

The LSI-11 I/O bus is not compatible with the UNIBUS although it is functionally similar in that I/O device registers are addressed as memory locations. Currently, only serial devices, such as a Teletype unit, can interface to the LSI-11 as a peripheral device. Special devices can connect to the parallel interface. Digital will provide more I/O interfaces in the future for other devices such as mass storage units.

Initially, the LSI-11 must be program loaded from ROM, from a host computer, or from a mass storage device supplied with a turnkey system.

COMPETITIVE POSITION

Although the LSI-11 uses the PDP-11/40 instruction set, it is a horse of another color.

The LSI-11 offers a challenge more to the microcomputer manufacturers, such as INTEL, than to minicomputer manufacturers. Only Computer Automation with its Naked Mini/Milli systems competes in this market. Thus, Digital has chosen to halt the microcomputer encroachment on the low end of the minicomputer market by expanding the processing power of the PDP-11 line downward. A microcomputer manufacturer would have to make a considerable investment to match the software available for the PDP-11.

The LSI-11 is slower than minicomputers and its I/O is rudimentary. It is ideal, however, for dedicated applications that require power but relatively low speed.

HEADQUARTERS

Digital Equipment Corp.
Components Group
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Marlborough MA 01752
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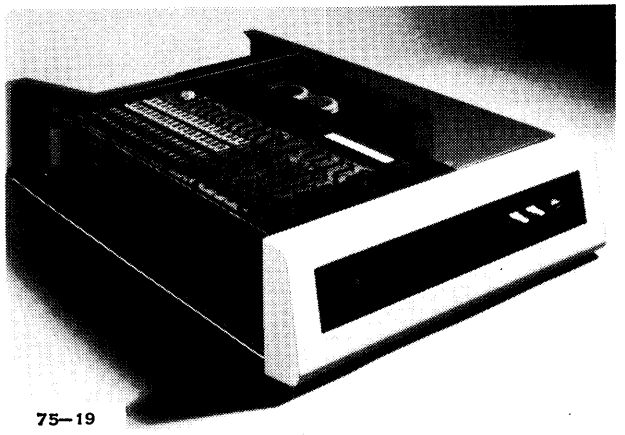
TYPICAL PRICES

Model Number	Description	Purchase $*
	Processors	
KD11-F	Microcomputer Module System (includes CPU; 4K x 16 random access memory; 16-bit I/O port; power fail/auto restart; real-time clock input; automatic priority interrupt arbitration; vectored interrupt handling; 8.5 x 10-in. board)	990
KD11-J	Same as KD11-F except with multiple board configuration of two 8.5 x 11-in. boards	1,536
	Memory	
MRV11-AA	PROM/ROM Memory Unit (includes 31 IC sockets; accepts 256 x 4 or 512 x 4 fusible link memory device; accepts masked ROM device; max capacity to 4K x 16)	175
MSVII-A	1K x 16 Random Access Memory (static RAM)	475
MSVII-B	4K x 16 Random Access Memory (dynamic RAM)	625
MMVII-A	4K x 16 Core Memory	625
	Processor Options	
H9270	Backplane Assembly	175
KEVII	Extended Arithmetic Chip	125
MRV11-AC	Fusible Link Unprogrammed PROM Chip (512 x 4 array size)	35
	Interfaces	
DRV11	Parallel Interface Unit	195
DLV11	Serial Interface Unit	235
	Software	
QJV10-AB	Paper Tape Software Package (includes editor, assembler, loader, debugging package (ODT); input/output exerciser (IOX))	100
QPV10-AE	Emulator Software Package (runs under RT11 on PDP-11/34/40 system; includes editor, assembler, linker, debugging program, load package, save package, execute package)	500

*Quantity discounts available.

DIGITAL EQUIPMENT CORPORATION

PDP-11



OVERVIEW

PDP-11, Digital's 16-bit minicomputer, was introduced in January 1970 with the announcement of the PDP-11/20. Since then, Digital has continued to expand the line at both the upper and lower ends until it covers most of the market up to a range of medium-scale general-purpose computers. Digital directs most systems to both the OEM and end-user markets.

A basic processor design frequently has two possible model numbers, a number ending in zero if it is an end-user system or a number ending in 5 if it is an OEM system. Thus, Models 11/05, 11/15, and 11/35 are the OEM equivalents of Models 11/10, 11/20, and 11/40, respectively. Although no OEM model numbers have been assigned, the 11/45 is available in both OEM and end-user versions. The PDP-11/50 is a PDP-11/45 that uses MOS semiconductor solid-state memory for main memory. The PDP-11/04 is an 11/05 that uses a 725-nanosecond MOS memory and MSI circuitry to achieve small size and low cost. In general, model numbers reflect processing power, with lower numbers for smaller, slower speed, less powerful systems and higher numbers for faster, larger, more powerful systems.

The PDP-11/40 and its companion model 11/35 were logically like the 11/20 and comparable in price, when introduced. The 11/40, however, has an expanded instruction set, one additional optional processor mode (two modes total), and a larger memory capacity than the 11/20, as well as optional hardware for floating-point arithmetic and memory management. Therefore, it has replaced the slower 11/20 as the backbone of the PDP-11 line because it offers higher performance at the same cost. Digital no longer actively markets the 11/20, or its OEM equivalent, the 11/15.

The PDP-11/45 and 11/50 are major upward expansions of the PDP-11 line and offer many features unavailable for the other models, including semiconductor bipolar or MOS memory and three processing modes. They are designed for applications requiring large memories, fast computation speeds, or multiprocessor configurations.

PDP-11/45 and 11/50 memory segmentation option is functionally similar to the 11/35 and 11/40 memory management option although it differs in some respects because of the larger number of registers and processing modes on the 11/45 and 11/50. Memory segmentation (memory management) provides virtual addressing for memories larger than 28K words; it also provides a means of memory protection for multiprogramming environments.

At the low end of the line, the 11/04, which is the newest member of the series, keeps the line competitive with very small low-cost OEM systems. These have been the first to benefit from the new MOS and microprocessor technologies and frequently have the CPU on a single board.

The PDP-11 line has three characteristics that distinguish it from other computers in its class: the UNIBUS, multiple general-purpose registers, and the manner of handling I/O operations. Like many of the newer systems on the market, later models are microprogrammed.

All PDP-11 models except the PDP-11/45 and 11/50 are organized around a single fast UNIBUS that connects all system components. The processor, memory, and peripheral devices operate as UNIBUS subsystems; the processor allocates UNIBUS time to system components, which communicate with each other in a master-slave relationship.

The distances between devices and the speeds of the connected devices are immaterial because of the master-slave communications technique. This arrangement means, for example, that memory modules with different speeds can be connected to a system.

A single UNIBUS inherently limits system speed to that of the UNIBUS because units in the system must time-share it. The PDP-11/45 and 11/50 overcome this limitation by using a second bus between solid-state memory and the CPU. Also solid-state memory has two ports of entry; one port can connect to one CPU and the other port to a second CPU. Thus, solid-state memory can be shared by two processors.

All PDP-11 processors have at least eight general-purpose registers, which can be used as accumulators, address or stack pointers, or index registers. Two registers have special functions as well: one is the program counter, and the other is a hardware stack pointer for interrupt handling. The PDP-11/35 and 11/40 have two stack pointers for interrupt handling, one for each of the two processing modes; thus, a program can use only the pointer associated with its processing mode. The general-purpose registers are versatile and are used to implement a powerful addressing scheme, which makes stack manipulation easy.

The PDP-11/45 and 11/50 have 16 general-purpose registers: 12 are dual sets of six registers used for accumulators, address or stack pointers, and index registers; three

are hardware stack pointers that handle interrupts for the three processor operating modes; and one register is the program counter. The 11/45 and 11/50, like the other PDP-11 processors, have only one program counter.

All PDP-11 processors address I/O device registers as memory locations; thus, the entire instruction set can be used to operate on data or control information held in those registers. Memory addresses 28,672 to 32,767 are reserved for I/O register addressing, so maximum main memory for a basic system cannot exceed 28,672 words. Memory to 124K words is available as an option on the 11/35, 11/40, 11/45, and 11/50 and by special order on the other systems.

Digital provides a comprehensive range of peripherals for its PDP-11 line: conventional paper tape and punched card I/O units including a mark sense card reader; DECtape as mass storage for small systems and industry-standard magnetic tape devices for larger storage requirements; fixed-head disc units and movable-head disc cartridges for larger systems; graphic subsystems; special-purpose subsystems to handle analog/digital and digital/analog and digital I/O for data acquisition and control applications; and a broad range of communication interfaces for data communications environments.

Software support for the PDP-11 is substantial. Software packages currently offered include a Paper Tape Software System and a Cassette Programming System (CAPS) for small configurations, Resource Time-Sharing System (RSTS), Disc Operating System (DOS), two Real-Time Multiprogramming Systems (RSX-11 M and D), and a smaller single-user real-time system (RT-11), a Communications-Oriented Multi-Task Executive (COMTEX-11), and others. Current languages supported are the PAL-11 and MACRO-11, assembly languages, FORTRAN IV, FOCAL, BASIC Plus, and COBOL. These packages support small stand-alone systems, time sharing, batch processing, real-time multiprogramming, communications applications (including 2780 and 2788 emulation for front-end and concentrator configurations), graphics, and laboratory applications.

Table 1 lists system specifications common to all models and Table 2 lists the chief differences among models.

Competitive Position

PDP-11 is a major minicomputer system from the leading minicomputer manufacturer—it is the system against which all other minicomputers are compared in the marketplace.

Digital was slow to enter the 16-bit minicomputer field, having a large investment in its popular 12-bit PDP-8 line and 18-bit PDP-9/15 line. By the time the PDP-11 was introduced, the design for most 16-bit minicomputers had stabilized and included a paging addressing scheme, priority interrupt system, programmed I/O, and direct memory access channel.

Table 1. Digital PDP-11: Characteristics Common to All PDP-11s

ADDRESSING	
Direct (no. of words)	None (always through internal registers)
Indirect	Yes
Indexed	Yes
INPUT/OUTPUT	
Programmed I/O	Yes
DMA Channels (no.)	1 (any no. of devices per channel)
Multiplexed I/O (no. of sub-channels)	None
MEMORY	
Parity	Option
Basic Addressable Unit	Byte or word
Bytes per Access	1 or 2
DECIMAL ARITHMETIC	No
MICROPROGRAMMED	All models except 11/15 and 11/20

PDP-11's design was radically different, incorporating features not provided in most other systems, such as the UNIBUS that connects all units in the system; multiple internal general-purpose registers used as accumulators, index registers, address and stack pointers and special-purpose registers (program counter and interrupt pointer); and I/O registers that operate like memory locations. Thus, Digital asserted itself as the trend-setter, leaving other manufacturers to follow its lead or to compete by using minicomputers with designs that could rapidly become obsolete.

To date, only a few minicomputer manufacturers have introduced systems similar to the PDP-11. The GRI-909 and the Lockheed SUE resemble PDP-11 somewhat, in that they have a universal bus comparable to the UNIBUS. The cost of developing totally new system software has probably prevented other manufacturers from departing from traditional designs. In addition, the single-bus architecture has some major drawbacks for real-time applications that require many I/O operations. Even for large configurations, a second bus is unavailable except for solid-state memory modules.

Major PDP-11 competitors are the Data General ECLIPSE; General Automation 16 Series; Honeywell System 700; Hewlett-Packard 21MX Series; Varian V70 Series; PRIME 100, 200, 300; MODCOMP I, II, and IV; Xerox 530; and Digital's own PDP-8. Hewlett-Packard's powerful HP 3000 competes directly with the PDP-11/45 and 11/50. Other systems compete in specific application areas where they provide strong system support.

The PDP-11 is a formidable competitor. Its members cover a broad range of processor power, with each larger system upward compatible with smaller systems in the line. The software support also covers a broad range, from small systems using the RT-11 operating system to large configurations with 124K words of memory and the

Table 2. Digital PDP-11: Differences Among PDP-11s

Model	PDP-11/04; 11/E05; 11/05; 11/10	PDP-11/15; 11/20; 11/R20	PDP-11/35, 11/35F; 11/40	PDP-11/45; 11/50
ARCHITECTURE				
CPU Models	KD11-B	KC11; KA11; KAR11	KD11-A	KB11
Microprogrammed	Yes	No	Yes	Yes
G-P Registers	8	8	9	16
Buses	UNIBUS	UNIBUS	UNIBUS	UNIBUS + semiconductor memory bus
Automatic Priority Interrupts	Multiline, multilevel	Single-line, multilevel	Multiline, multilevel	Multiline, multilevel + 7 software levels
Stack Size	Fixed	Fixed	Fixed std; variable opt	Variable
Floating Point	Software	Software	Hardware opt	Hardware opt
MEMORY				
Types	Core (11/05, 11/10); MOS (11/04)	Core	Core	Core/MOS/bipolar
Capacity (words)				
Min	4,096	4,096	8,192	16,384
Max	28,672	28,672	126,976	126,976
Increment Sizes (words)	8,192; 16,384;	8,192; 16,384	8,192; 16,384	1,024; 4,096; 8,192; 16,384
MEMORY				
Management Hardware	No	No	Yes, opt	Yes, opt
Memory Protect	No	No	Opt	Opt
Cycle Time (μsec)				
Core	0.90, 0.98	0.90	0.90, 0.98	0.90, 0.98
MOS	0.725 (11/04 only)	–	–	0.495
Bipolar	–	–	–	0.300
INSTRUCTIONS				
Overlapped	No	No	Yes	Yes
Extended Arithmetic	Opt	Opt	Opt	Std
Std Instruction	Basic	Basic	Basic + XOR, SOB, RTT, MARK, SXT	11/40 set + MUL, DIV, ASH, ASHC, SPL
No. (std; opt)	70; 4	70; 4	70; 10	83; 50

RSX-11D Operating System. User programs in a multiprogramming environment can use up to 32K words for program space and 32K words of data space. Also, the PDP-11 is a relatively new system from the largest minicomputer manufacturer; thus it is still in the growth period of its life cycle. Digital will continue to enhance the line with both software and hardware.

The one disadvantage that Digital has in relationship to the large computer manufacturers is that the company still does not lease its computers. This decision deters some potential users who do not wish to make the total commitment of buying a system. It also means Digital does not have a solid rental base for steady income. So far, this has not thwarted Digital's growth although it is difficult to believe that the market for minicomputers can continue to grow at its current rate. As the minicomputer manufacturers market to less sophisticated users and to smaller companies, leasing will become more of a competitive factor.

User Reactions

Interviews with several PDP-11 users to get sample responses to the systems produced information on a wide variety of applications since some users have several systems, each used for different purposes. A southern telephone company uses one PDP-11/45 with a 48K-word memory for I/O preprocessing and media conversion to magnetic tape. A second, disc-based (300M bytes total) 11/45 polls two computers, which in turn poll 500 terminals for sales and delivery data — also converted to magnetic tape that feeds into a CDC 3301. A large university laboratory has a disc-based PDP-11/45, a core-based 11/40, and a core-based 11/15, each running different instruments and experiments. The 11/45 is used for program development for the other two, and also to communicate with Brookhaven's CDC 6600. A large research institution also uses a PDP-11/40 with one disc to tie into Brookhaven's computer, as well as to run a graphics display. A steel company has two 11/20s and four 11/10s, all used

for automatic gauge control on rollers/reversers. A large oil company uses a PDP-11 with 16K words of memory to poll 48 terminals to obtain delivery and service information from all over the country.

Users seem to agree that the PDP-11 CPUs are reliable, and service is prompt. Promptness is variously defined, of course; one user, who is 600 miles from the nearest service center, feels that a 1- or 2-day response time is pretty good. Universally, the CPU is praised for reliability, but some users have found problems with various I/O components that must be adjusted. The steel company, for instance, had some trouble with a power supply that eventually had to be replaced. The steel company does its own maintenance, and complains that, under these circumstances, it does not receive news about field engineering changes, such as a new power supply. The company feels that the UDC (Universal Digital and Analog Subsystem Controller) interface could use some design work because the large circuit boards are unwieldy and difficult to change.

Users universally feel the system software is efficient and proves to have no unexpected bugs. One user at the university chemistry laboratory would like to see Digital develop a high-powered time-sharing system that would allow multiple interactive terminals for users to develop and execute programs in FORTRAN or a similar high-level language. A user at the university laboratory says that the 11/45 hardware could clearly support this type of a system but system software is needed. The user at the research institute is delighted that the system is considerably more powerful than expected, and has found that it can do more and more of its calculations at the satellite, instead of using the remote Brookhaven system as originally intended.

Configuration Guide

A PDP-11 system consists of a processor, UNIBUS, memory ranging in size from 4,096 to 28,762 words (126,976 on the 11/35, 11/40, and 11/45 and by special order on the other PDP-11 processors), programmer's or operator's console, and peripheral devices. Addresses of the top 4K from the 32K memory words of the basic system are reserved to address I/O device registers.

Minimum system configurations for each of the models are as follows:

- 11/04 — KD11-D CPU, 4K- or 8K-word MOS memory, operator's console, ASCII device control logic, power supply, bootstrap, ROM diagnostics, DMA, 4-level interrupt, 5-1/4-inch chassis with 14 or 9 slots.
- 11/05, and 11/E05 — KD11-B CPU, 4K- or 8K-word core memory, programmer's console, Teletype control, power fail/auto restart, power supply, line frequency clock, 4-level interrupt system; standard core (900-nanosecond cycle time); Model 11E05 uses 16K-word core board (980-nanosecond cycle time).
- 11/10 — KD11-B CPU, memory, console, power supply, real-time clock, terminal interface and 5-1/2-inch assembly for basic configuration: the same features with 16K-word memory, 10.5-inch assembly, DECwriter, RK11D disc, TA11 cassette and bootstrap loader for larger configurations.
- 11/35 and 11/35F — KD11-A CPU with 4-level interrupt and 32K-word memory, memory management unit, console, 21-inch chassis, power fail/auto restart, power, OEM diagnostics; prewired slots for clock, extended arithmetic, floating point, prog. stack; 11/35F is like 11/35 but with 32K words of 980-nanosecond-core modules.
- 11/40 — KD11-A CPU with 4-level interrupt and 8K- or 16K-word memory and console terminal; submodels differ depending on whether memory is 8K or 16K words, whether parity is included, and whether the console terminal is a Teletype, LA30 DECwriter, or VT05 display.
- 11/45 — KB11-A CPU with 4-level interrupt, 16K- or 32K-word core memory, console terminal; submodels differ depending on whether memory is 16K or 32K words, whether parity is included, and whether terminal is Teletype or LA30 DECwriter; DECwriter version includes clock and bootstrap.
- 11/50 — KB11-A CPU with 16K-word MOS memory and 16K-word core memory, both with parity, memory management, LA30 DECwriter, clock, and bootstrap.

All processors support all of the devices provided for the PDP-11 line, as listed in Table 3. The 11/04 includes a four-slot or nine-slot, 5-1/4-inch chassis. The 11/05 and 11/10 include either a 5-1/4 inch or a 10-1/2-inch chassis. Larger models use only the larger chassis. The 10-1/2-inch chassis has 20 slots, which can be expanded to 40 slots within the chassis. All PDP-11 systems can also attach one or two external 20-slot bus extensions. The 11/04 is designed as a MOS memory system, but core can be added to the system provided it is located in an external extension chassis.

Models 11/10 and below can expand memory to 28K words. The 11/35, 11/40, 11/45, and 11/50 have memory management options allowing memory up to 124K words to be addressed.

The 11/35 and 11/40 processors can support two processor modes with the memory management option and a floating-point arithmetic option, in addition to all the features of the 11/20. The memory management option, which is in most respects similar to the memory management option on the 11/45 and 11/50, allows addressing 124K words of core and provides for programmed memory protection.

PDP-11/45 and 11/50 use a processor that has all the features of the 11/40 plus three processing modes, more internal registers, an internal bus to semiconductor memory, and options for memory management and floating-point arithmetic. They are dual-bus systems. An internal

Table 3. Digital PDP-11: Peripherals

Model No.	Description
Discs	
RC11/RS64	Fixed-head discs – 64K wds/drive, 8 drives/controller
RF11/RS11	Fixed-head discs – 256K wds/drive; 8 drives/controller
RJ03/RJ04, RS03/RS04	Fixed-head discs – 256K/512K wds/drive; 8 drives/controller
RK11/RK05	Moving-head discs – 1.2M wds/pack; 8 drives/controller
RP11/RP03	Moving-head discs – 20M wds/pack; 8 drives/controller
RJP04	Moving-head discs – 3330-type, 44M wds/pack, 8 drives/subsystem
Magnetic Tape	
TC11/TU56	DECtape – 288K char/reel; 4 drives/controller
TM11/TU10	7 or 9-trk magnetic tape–45 ips; 8 drives/controller
TA11	Dual cassette transport and controller
TJU16	9-trk magnetic tape system – 800 bpi only or mixed 800 NRZI/1,600 PE, 8 drives/controller
Card	
CM11	Mark sense reader – 40 col, 200 cpm
CR11/CD11	Punched cards – 80 col, 300/1,000 or 1,200 cpm respectively
Paper Tape	
PC11	Reader/punch – 300 cps read, 50 cps punch
PR11	Reader – 300 cps
Printers	
LP11	Line printer series – 170 to 1,200 lpm, 80 to 132 cols, 64 or 96 char
LS11	Line printer – 60 lpm, 132 cols, 64 char
LV11	Electrostatic printer/plotter – 500 lpm, 120,000 dots/sec
CRT	
VT01/TR01	Tektronix 611/RM503, respectively
VR14	Point plot display – 7 x 9 inches
VT05	CRT displays – 1440 char (20 lines, 72 char/line)
Graphics	
GT40	PDP-11/10-based subsystem – 17-inch CRT, light pen
GT42	PDP-11/40-based subsystem – 17-inch CRT, light pen, disc
EG11	Engineering display subsystem – dot display, 71 x 43 A/N characters, controller
Teletypewriters	
Teletypes	LT33 & LT35 ASR and KSR units – 10 cps
LA30	DECwriter – 30 cps, local/remote
Communications	
DC11	Digital I/O subsystem – 50 to 1,800 baud units
DL11	Full-duplex single serial line interfaces – to 2,400 baud
DJ11	16-line multiplexor
DH11	Programmable asynchronous 16-line multiplexor
DP11	Synchronous line module set – full/half duplex models up to 40K baud
DU11	Synchronous interface – full/half duplex, 9600 baud
DQ11	Synchronous interface – full/half duplex, models up to 1.0M baud
DF11	TTL to 20 mA local TTY, or EIA/CCITT voltage
DN11	System unit for 4 Bell 801 ACUs
DC08	Telegraph line interface – up to 32 lines
Process I/O	
LPS	Laboratory peripheral system – for up to 48 channels of A/D and 8 channels of D/A
AD01	A/D conversion subsystem – up to 32 channels
AA11	D/A conversion subsystem – up to 4 channels

bus connects the central processor to semiconductor (MOS or bipolar) memory modules, and the UNIBUS connects the processor, core memory, and all other system units. All semiconductor memory modules have two ports of entry; thus, two processors can share semiconductor memory modules. A PDP-11/45 or 11/50 system can use a mixture of MOS, bipolar, and core memory up to the maximum total memory capacity of 126,976 words.

The 11/45 and 11/50 processors can support two solid-state memory controllers. Each controller can support only one type of memory: up to four 4K-word MOS modules or four 1K-word bipolar memory modules. Thus, a system can have a maximum of 32K words of MOS memory and 8K words of bipolar memory, or 16K words of MOS and 4K words of bipolar memory. The basic 11/45 configuration uses all core memory, while the 11/50 uses either all MOS or a mixture of MOS and core. Either model can be expanded to include both types as well as bipolar memory modules.

Memory for all PDP-11 models can be read/write or read only. Modules are available in increments of 1K (bipolar), 4K (MOS), 8K or 16K (core) words, with only core common to all models. All present core memory modules have a single port of entry while semiconductor modules for the 11/45 and 11/50 can have two ports. Although any PDP-11 system can support core memory modules with any cycle rate, the memory cycle rate considered standard for the different systems is 900 nanoseconds for 8K-word modules and 980 nanoseconds for 16K-word modules. Parity is optional on all models.

Software packages may require considerably more than the basic configurations. Table 4 lists configuration requirements for the major software packages.

In addition to general configurations, Digital offers hardware/software packages for special applications,

which provide savings over using systems configured from a components shopping list. Packages are offered for GT40 and GT42 graphics subsystems, laboratory systems, industrial systems, and communications systems.

Compatibility

PDP-11 computers are upward compatible, from the PDP-11/04 through the 11/10, 11/20, 11/40, to the 11/45 and 11/50, and their OEM equivalents. All can use the same peripheral devices and core memory modules, as well as the same instruction and data formats. All use the same basic instruction set; the 11/35, 11/40, 11/45, and the 11/50 use supersets of the basic instruction set.

PDP-11 is not compatible with any other computer system.

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks outside the large computer companies, both in the United States and worldwide. More than 1,500 engineers man its service staff.

Aside from 46 sales and service locations in the United States, Digital has offices in five Canadian cities, six Australian cities, five German cities, six U.K. cities, three Brazilian cities, and one or two cities each in Argentina, Austria, Belgium, Chile, Denmark, Finland, France, India, Israel, Italy, Japan, Mexico, the Netherlands, New Zealand, Norway, Philippines, Puerto Rico, Spain, Sweden, Switzerland, and Venezuela. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users and have thus provided considerably less software support and applications programming assistance than the large systems makers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical; on the other hand, a user can buy service on an individual call basis, or set up his own maintenance staff.

HEADQUARTERS

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Table 4. Digital PDP-11: Software

Package	Description
DOS	Disc operating system; batch package adds job stream processing; requires 8K-wd memory, TTY, disc, DECtape or high-speed paper tape device
RSTS	Time-sharing for up to 16 (RSTS-11) or 32 (RSTS-E) terminals; RSTS-11 requires 20K-wd memory, 256K-wd disc, 2 DECtapes, clock, terminal interfaces; RSTS-E requires 40K-wd memory with parity, larger disc
RT-11	Single user interactive real-time system for program development in scientific or research environment; requires 8K-wd memory, console terminal, and either dual DECtape or disc plus paper tape or cassette
MUMPS-11	Interpretive data management software system geared to interactive I/O; requires 8K-wd memory on any PDP-11, disc, tape, and console terminal
CAPS-11	Cassette programming system for 4K-wd memory, dual cassette drives, and console terminal
RSX-11	Real-time multiprogramming executive in 5 versions, 2 actively marketed; running from 8K-wd core-based or disc-based version with assembly language support, to full-blown disc-based foreground/background multiprogramming system supporting on-line FORTRAN and COBOL. Configurations vary widely; largest systems require memory management option
COMTEX-11	Modular reentrant package for servicing communications devices; SCIP monitor, and TAP table-oriented, terminal routines
BASIC	Extension of Dartmouth BASIC, language of RSTS and RT-11, also stand-alone version (desk calculator)
FOCAL	Interpreter for small systems in either stand-alone or DOS versions
FORTRAN IV	ANSI standard, batch versions for DOS or on-line version for RSX-11
COBOL	ANSI x • 3.23-1974, standard plus extensions; requires PDP-11/30 or larger system with 48K wds of memory, printer, card reader, keyboard/display, and RSX-11 (M or D)
Assemblers	Absolute and relocatable PAL-11, stand-alone and DOS, RSTS-11, COMTEX-11, RSX-11 versions
Utilities	Editor, debugger, linker, librarian, loader and so on.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	LABORATORY AND SCIENTIFIC SYSTEMS		
PDP-11E10-NE/NF*	Disc Operating System with PDP-11/10	24,000	285
DECLAB 11/10-A	LAB System with ASR-33 terminal	11,495	131
DECLAB 11/10-B	Lab System with DECwriter and 10-bit A/D	15,585	159
DECLAB 11/10-C	LAB System with DECwriter and 12-bit A/D	18,385	191
DECLAB 11/10-D	LAB System with DECwriter; uses Foreground/Background Operating System	26,750	265
DECLAB 11/10E	LAB System with 1.2M-wd disc cartridge drive and control	29,550	297
DECLAB 11/40-AA/AB*	Laboratory Computer System with PDP-11/40 CPU	37,500	494
RSX-11D System #1	Real-Time System Executive System with PDP-11/50	111,100	886
RSX-11D System #2	Real-Time Executive System with PDP-11/40	52,525	444
RSX-11D System #3	Same as System #2 except for RK05 disc cartridge drive instead of TM11 magtape unit	46,880	407
RT-11 System #4	Real-Time system with PDP-11/50	57,505	557
RT-11 System #5	Real-Time System (same as system #4 except for RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	51,860	520
RT-11 System #6	Real-Time System with PDP-11/45	49,505	401
RT-11 System #7	Real-Time System (same as System #6 except RK05-AA/BB* disc cartridge drive instead of TM11 magtape)	43,860	364
RT-11 System #8	Real-Time System with PDP-11/40 Recommended software: RT-11 monitor and system programs, Dartmouth BASIC, and ANSI Std FORTRAN IV	38,945	345
RT-11 System #9	Real-Time System (same as System #9 except BM792-YB disc/DECtape bootstrap loader and RK05AA/BB disc cartridge drive instead of TM11 magtape) DOS/BATCH Operating System and ANSI Std FORTRAN IV	33,050	306
DOS/BATCH System #4	DOS/Batch System with PDP-11/50	57,505	557
DOS/BATCH System #5	DOS/Batch System (same as System #4 except RK05-AA/BB* disc cartridge drive)	51,860	520
DOS/BATCH System #6	DOS/Batch System (same as System #4 except with 11/45-CU/CV*CPU)	49,505	401
DOS/BATCH System #7	DOS/Batch System (same as System #6 except RK05-AA/BB* disc cartridge drive)	43,860	364
DOS/BATCH System #8	DOS/Batch (same as RT-11 System #8 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	38,945	345
DOS/BATCH System #9	DOS/Batch System (same as RT-11 System #9 but with recommended software: DOS/BATCH operating system and ANSI Std FORTRAN IV)	330,050	306
CAPS-11 System #10	CASSETTE Programming System with PDP-11/10	12,335	147
CAPS-11 System #11	Cassette Programming System with PDP-11/40 Recommended software: Dartmouth BASIC/PTS	19,200	185
MUMPS-11 System #12	MUMPS-11 Software Package, with 11/45	80,195	580
MUMPS-11 System #13	MUMPS-11 Software Package with 11/40	45,145	386
PHA-11 System #14	Pulse Height Analysis System with PDP-11/40	52,920	456
PHA-11 System #15	Pulse Height Analysis System on PDP-11E10	32,500	330
GAMMA-11 BM11-HA/HB*	Nuclear Medicine System on PDP-11/40	56,500	442
11/45-RP/RR*	RSTS/E Timesharing Systems on PDP-11/45; with dual DECtape and cartridge disc storage; expandable	83,670	485
11/45-RS/RT*	Same as 11/45 RP/RR except industry std 9-track magnetic tape instead of DECtape unit	85,715	538
11/45 RU/RV*	Same as 11/45 RS/RT except with floating-point processor and 20M-wd disc pack unit	97,485	635
RSX-11D	Real-Time Operating System on PDP-11/45	64,315	433
11/45-NA/NB*			
11/45-NC/ND	Same as 11/45-NA/NB* except with additional 16K parity core memory and H960-D extension mounting cabinet with PDP-11/45 and simultaneous background batch processing	73,015	473
11/45-NE/NF		122,040	743
11/45-NH/NJ	Same as 11/45 NH/NJ except with RK05 DECpack disc drive and no mag tape unit	67,370	438
11/45-PS/PT	Batch Processing System on PDP-11/45	51,205	378
11/45 PU/PV	Same as 11/45 PS/PT except with RF11-A 262K fixed-head disc unit and TC11 DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	52,560	290

Model Number	Description	Purchase $	Monthly Maint. $
11/50-NA/NB	Batch Processing System on PDP-11/50	73,015	580
11/50-NC/ND	Same as 11/50-NA/NB* except additional 16K parity core memory	78,615	605
11/50-NE/NF*	High-Performance PDP-11/50-Based Real-Time System with simultaneous background batch processing	153,500	990
11/50 NH/NJ*	Same as 11/50 NC/ND* except 1.2M-word DECpack instead of mag tape unit	72,970	570
11/50-PS/PT*	Batch Processing System on PDP-11/50	59,205	525
11/50-PU/PV	Same as 11/50 PS/PT except RF11-A 262K fixed-head disc unit and TC11-G DECtape unit instead of RK11-D DECpack disc unit and TM11-E mag tape unit	60,560	437
11/50-PW/PY	Batch Processing System on PDP-11/50 with high-speed card reader and line printer, floating-point hardware, industry std mag tape and 20M-word disc pack storage	137,980	1,004
11/50 RP/RR	48K 11/50-Based Timesharing System on PDP-11/50 with dual DECtape and cartridge disc storage; expandable to 32 simultaneous users	92,370	632
11/50-RS/RT	Same as 11/50 RP/RR except TM11-E mag tape unit instead of TC11-G DECtape unit	94,415	685
11/50-RU/RV	Timesharing System on PDP-11/50 with 20 M-wd disc pack storage, hardware floating-point processing, industry std mag tape expandable to 32 users	106,185	782
	CENTRAL PROCESSOR AND WORKING STORAGE		
PDP-11/04	Computer System with processor, operator's console and bootstrap loader	2,475	NA
PDP-11/05	Computer System (OEM only) with KD11-B Central Processor		
KA/KB*	4K Core (space for 8K co and 4 peripheral controllers)	4,395	53
LA/LB*	Same as KA except 8K core (space for 4 peripheral controllers)	4,995	69
NC/ND*	8K Core (mounted in 10.5-inch box)	5,995	69
SC/SD*	16K Core	7,495	NA
PDP-11/05-SC/SD*	16K Core; 28K Chassis	7,495	74
	Processor Options		
MM11-K	4K Wd of 16-Bit Read/Write Core Memory (900-nsec cycle time)	2,700	20
PDP-11E05 NE/NF*	Computer System (OEM only) with KD11-B Central Processor and 16K core	24,000	269
PDP-11/10 AC/AD*	Computer System with KD11-B Central Processor and 8K core	6,995	69
KE11-A	Extended Arithmetic Hardware Element (multiply/divide; multiple shifts; normalize)	1,940	10
KG11-A	Communications Arithmetic Element	810	6
PDP-11/10 NC, ND	Same as 11/10-AC, D except in 10½-inch assembly	7,495	69
PDP-11/10 NE, NF	Basic PDP-11/10 with 16K core	24,000	285
11/10-SC/SD*	PDP-11/10 Computer in 10.5-Inch Assembly with 16K-word core memory, real-time clock, and console terminal control (for serial devices)	7,495	74
KG11-A	Communications Arithmetic Element (for calculation of cycle and longitudinal redundancy checks; calculation and test of block check char; required for sync communications)	900	6
PDP-11/35 FL/FM*	Computer System (OEM only) with KD11-A Central Processor and 32K Core	20,495	147
11/35-SC/SD*	Same as 11/35-FL/FM* except 16K MF11-U memory and 40K chassis	11,495	111
11/35-JE/JF*	Same as 11/35-FL/FM* except 8K ME11-L memory and 56K chassis	9,995	100
11/35-JC/JD*	Same as 11/35-FL/FM* except 8K MM11-S memory and 32K chassis	9,495	101
11/35-JA/JB*	Same as 11/35-FL/FM* except 8K MF11-L memory and 32K chassis	9,495	100
PSP-11/40 CA/CB*	Computer System with KD11-A Central Processor and 8K Core	12,995	143
PDP-11/40 BA/BB*	Same as 11/40-CA except 16K wds of core memory	15,500	138
PDP-11/40 BC/BD*	Same as 11/40-BA/BB except with Serial LA30 DECwriter and control instead of Teletype	16,250	133
PDP-11/40 BE/BF*	Same as 11/40-BC/BD except with VT05 display terminal and control instead of the LA30	16,250	124
PDP-11/40 BH/BJ*	Same as 11/40-BA/BB except core memory has parity	16,900	133
PDP-11/40 BK/BL*	Same as PDP-11/40-BC/BD except core memory has parity	17,650	127
PDP-11/40 BM/BN*	Same as PDP-11/40-BE/BF except core memory has parity	17,650	119
	Options for KD11-A Processor		
KE11-E	Signed Integer Multiply and Divide; extended instruction set (EIS) option	1,400	11
KE11-F	Floating-Point Processor (4 instructions: multiply, divide, subtract, add; requires KE11-E)	1,500	11
KJ11-A	Stack Limit Option (permits a soft stack limit violation)	400	5
KT11-D	Memory Management Option (permits access to 124K wds; includes KJ11-A)	2,480	21
PDP-11/45 BA/BB*	Computer System KB11-A Processor with 16K-wd core memory, ASR33 TTY terminal, and control cabinet	26,660	196
PDP-11/45-BH/BJ*	Same as 11/45 BA/BB except core memory has parity	27,670	191
PDP-11/45-CU/CV*	KB11-A Processor with 16K-wd parity core memory, serial LA30 DECwriter, and control	27,760	194
PDP-11/45 CW/CY*	Same as 11/45-CU/CV except with 32K-wd parity core memory	37,570	252

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
PDP-11/45-FK/FL	KB11-A Processor with 16K core memory, no parity (OEM)	23,900	191
PDP-11/45-FH/FJ	KB11-A Processor with 16K core memory, and parity (OEM)	25,300	186
PDP-11/45-FU/FV	KB11-A Processor with 32K core memory, no parity (OEM)	32,600	254
PDP-11/45-FS/FT	KB11-A Processor with 32K core memory and parity	35,100	244
PDP-11/50 CU/CV*	Same as 11/45-CU/CV except has 16K-wd MOS memory with parity	35,670	350
PDP-11/50 CW/CY*	KB11-A Processor with 16K MOS and 16K core	46,270	408
PDP 11/50-FK/FL	KB11-A Processor with 16K MOS memory, no parity (OEM)	32,000	341
PDP 11/50-FH/FS	KB11-A Processor with 16K MOS memory and parity (OEM)	33,000	341
PDP 11/50-FU/FV	KB11-A Processor with 16K MOS, 16 core, no parity (OEM)	39,900	405
PDP 11/50-FS/FT	KB11-A Processor with 16K MOS, 16 core, and parity (OEM)	42,500	400
	Options for KB11-A Processor		
FP11-B	Floating-Point Processor (operates on 32- and 64-bit nos.; integer to floating conversion)	5,290	45
KT11-C	Memory Management Unit	4,210	32
	Options for Any PDP-11 Processor		
KG11-A	Communications Arithmetic Element	900	6
KE11-A	Extended Arithmetic Hardware Element	1,940	11
	Memory for All PDP-11 Processors		
ME11LA/LB*	Memory System (16-bit read/write; 900-nsec core; rack mountable; power supply; first 8K increment)	5,200	37
MF11-L	8K Words of 16-bit Read/Write Core Memory (900-nsec cycle time; expandable to 24K in 8K or 12K increments)	4,700	37
MM11-L	8K-Word Expander for ME11-LA or MF11-LB	4,400	37
MM11-LK	12K Word Expander for MF11-L or ME11-L	7,100	58
MM11-S	8K-Word Core Memory and Control (900-nsec cycle time)	4,700	38
MF11-U	16K-Word Core Memory and Control with Expansion Capability to 32K (980-nsec cycle time)	4,900	32
MM11-U	16K-Word Expander Core Memory (980-nsec cycle time; MF11-U reqd)	4,500	32
MF11-UP	16K-Word Parity Core memory and Control with Expansion Capability to 32K (980-nsec cycle time)	6,300	27
MM11-UP	16K-Word Parity Core Memory Expander (980-nsec cycle time; MF11-UP reqd)	5,600	27
FM11-U	Conversion Kit (to add 16K memory capability)	1,000	–
	Memory for 11/40 and 11/45		
MF11-LP	8K-Word Parity Core Memory	5,700	32
MM11-LP	8K-Word Expander Parity Core Memory	5,400	32
	Semiconductor Memory for 11/45 and 11/50		
MS11-CC	Bipolar Memory Control	1,950	13
BC	First MOS Memory Control	1,950	13
BD	Second MOS Memory Control	1,500	13
MS11-CM	1K-Word Bipolar Memory (300-nsec cycle time)	1,950	16
CP	1K-Word Bipolar Memory (byte parity; 300-nsec cycle time)	2,500	16
BR	4K-Word MOS Memory (495-nsec cycle time)	3,000	42
BT	4-K-Word MOS Memory (byte parity; 495-nsec time)	3,400	42
	Graphic Systems		
GT40AA/AB*	Computer-based PDP-11/10 Graphic Terminal System	14,500	186
GT40AC/AD*	Same as GT40-AA/AB but ASR33 replaces keyboard	15,720	223
GT40AE/AF*	Same as GT40-AA/AB but LA30 DECwriter replaces keyboard	16,795	217
GT42AA/AB*	Computer-Based Graphic Terminal System	17,500	151
GT42 AC/AD*	Same as GT42-AA/AB but ASR33 replaces keyboard	18,720	181
GT44 AE/AF*	Same as GT42-AA/AB but LA30 DECwriter replaces keyboard	19,795	176
GT42 AA/AB*	Graphic Display Standard System	34,500	424
BM873-YA	Restart/Loader	400	1
MR11-DB	64-Word Bulk Storage Bootstrap Loader	700	5
	MASS STORAGE		
	Fixed-Head Discs		
RC11-A/B*	64K-Word Fixed-Head Disc Drive and Controller (for up to RS64 drives)	8,300	37
RS64-A/B*	64K-Word DECdisc Fixed-Head Drive (16 μsec/word transfer rate; 17-msec avg access time)	5,500	16
RF11 AA/BB*	256K-Word Disc Drive and Controller (for up to 8 RS11 discs; includes cabinet)	16,650	69
RS11/RS11-A*	256K-Word Fixed-Head Disc Drive (16 μsec/word transfer rate; 17-msec avg access time)	10,700	40
RJS03 BA/BD*	256K-Word Disc Drive and Controller (for up to 8 RS03 or RS04 drives; 4 or 8 μsec transfer rate; 8.5-msec avg access time; includes cabinet with space for 2 additional drives)	14,000	75
RJS04 BA/BD*	512K-Word Disc Drive and Controller (expands up to 8 RS03 or RS04 drives; includes cabinet with space for up to 2 additional drives)	18,000	85
RS03 AA/AD*	256K-Word Disc Drive (4 or 8 μsec/word transfer rate, 8.5-msec avg access time)	9,000	48
RS04	512K-Word Disc Drive (4 μsec/word transfer rate, 8.5-msec avg access time)	13,000	58
	Removable Discs		
RK11-DE/DJ*	1.2M-Word Disc Cartridge Drive (expandable to 8 RK05 DECpack disc drives; cabinet includes space for 3 additional RK05s)	11,000	106
RK05-AA/BB*	1.2M-Word DECpack Moving-Head Disc Cartridge drive (11.08 μsec/word transfer rate; 70-msec avg seek time)	5,100	64
RK05K-11	Cartridge for RK05	99	–
RP11 CE/CJ*	20-Word Disc Pack Drive and Controller (expandable to 8 RP03s)	31,880	233
RP03 AS/BB*	20M-Word Moving-Head Disc Drive (7.5 μsec/word transfer rate; 29-msec avg access time)	20,000	159
RP02-P	Disc pack for RP03 (20M wds)	295	–
	INPUT/OUTPUT		
KW11-L	Real-Time Clock (line frequency; causes interrupt every 16.6 msec [60 Hz] or 20 msec [50 Hz])	300	3
KW11-P	Programmable Real-Time Clock	700	6
LT33 DC/DD*	Teletype ASR 33 (with paper tape reader/punch; 10 cps)	1,850	37
CC/CD	Teletype KSR 33	1,400	32
LT35 DC/DD*	Teletype ASR 35 (with paper tape reader/punch; 10 cps)	4,860	32
CC/DD*	Teletype KSR 35	3,240	29
LC11-A	Controller for Data Terminal LA30-P	500	6
LA30 PA/PD*	DECwriter Data Terminal	2,795	32
CA/CD*	Same as LA30-PA except serial 20 ma current loop; switch selectable 110, 150, or 300 baud	3,195	32
EA/ED*	Serial DECwriter Word Copy Terminal	3,195	30
PC11,-A*	High-Speed Paper Tape Reader (300 cps) and Punch (50 cps) with Control	3,900	38
PR11	High-Speed Paper Tape Reader (300 cps) with Control	2,400	22
H-722	Transformer (required for 230 V operation of PC11, PR11)	100	–
CM11/CM11-A*	Mark-Sense Card Reader (40 col; 200 cpm)	5,290	50
CR11/CR11-A*	Card Reader (80 col; 300 cpm; tabletop model)	4,860	53
CD11-B/CD11-A*	Same as CR11 except 1,000 cpm; with DMA interface	10,800	74
CD11-EA/EB*	Card Reader (80 col; 1,200 cpm)	15,120	95
CM11-FA/FB*	Mark Sense and Punched Card Reader (285 cpm; includes control unit)	5,290	53
LP11	Line Printer (300 lpm; includes control logic)		
FA/FB*	(80-col, 64 char; 350 lpm)	12,000	60
HA/HB*	(80-col, 96 char; 250 lpm)	13,500	65
JA/JB*	(132-col, 64 char; 240 lpm)	17,500	75
KA/KB*	(132-col, 96 char; 170 lpm)	19,000	80
RA/RB*	Same as LP11-JA except 1,200 lpm; heavy duty	30,000	154
SA/SB*	Same as LP11-KA except 900 lpm; heavy duty	33,000	154
VA/VD*	132-Col, 64-Char Printer and Control Unit (300 lpm)	9,900	72
WA/WD*	132-Col, 96-Char Printer and Control Unit (230 lpm)	11,900	72
LS11-A,B*	132 Col, 64-Char (60 lpm)	5,615	48
LV11-BA/BB	Electrostatic Printer/Plotter and Controller; 132-col, 96 char; 500 lpm, 120,000 dots/sec	11,770	50
TC11-GA/GB*	DECtape Transport and Controller (for up to 4 TU56 transports; includes cabinet; 288K char/reel)	9,500	45
TU56	Dual DECtape Transport (288K char/reel)	5,100	32
TU10	Industry-Compatible Tape (½-in. tape; 800 bpi; 45 ips; 7-channel model has provision for program-selectable 556 and 200 bpi; up to 7 slave units can be added to each master and control; cabinet included)		
TM11-EA/ED*	9-Track Master (1st unit)	10,745	101
TU10-EE/EJ*	9-Track Slave	7,505	74
TM11-FA/FD*	7-Track Master (1st unit)	12,500	101
TU10-FE/FJ*	7-Track Slave	7,505	74
TA11-AA/BB*	Dual Cassette Transport and Controller	2,990	38
TU60-K	Cassette (150 ft.; 90,000 char)	7	
AA11-A	Control for VT01-A Scope (requires AA11-D and 2 BA614s)	645	2
B	Control for Scope (requires AA11-D and 2 BA614s)	645	2
C	Control for VR14 Scope (requires AA11-D and 2 BA614s)	645	2
VT01-A	Tektronix 611 Storage Tube Display	3,240	80
VR01-A	Tektronix RM503 Oscilloscope Display	1,080	15
VR14/VR14-A*	Point Plot Display (7 x 9 in.)	3,240	19
VT05B-AA/AD*	CRT Display (A/N; with keyboard; half/full-duplex; 64/96-char set; 20 lines, 72 char/line; TTY compatible; 110, 150 or 300 baud; requires DC11; no parity)	2,795	23
BA/BD*			
VT05B-CA/CB*	CRT Display (A/N; parity; 64/96-char keyboard; DF01-A or Bell 103 equivalent reqd; BC05-D cable reqd)	2,795	23
DA/DB*			
VT11-AA/AB*	Display Processor with 17-In. CRT and Light Pen	9,500	250
	DATA COMMUNICATIONS		
DC11-AA	Dual Asynchronous Serial Line System Unit and Clock (for mounting 2 DC11-DA modules; 110, 134.5, 150, or 300 bps; typical 103 modem speeds program selectable)	350	3
DC11-DA	Full Duplex Serial Module Set for DC11A (5-, 6-, 7-, or 8-bit codes; EIA/CCITT termination for direct use with 103 or 202 modem)	700	7
H312A	Asynchronous Null Modem (allows direct connection of peripherals with EIA 232 interface with a DC11)	85	2
DL-11A	Full Duplex Single Serial Line Interface (replaces KL11; customer specifies speed group 1 [110 baud] or 3 [50, 75, 150, 300, 600, 1,200, 1,800, and 2,400 baud]; for DEC-supplied TTY or VT05)	500	6

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
DJ11-AA	Asynchronous 16-Line Multiplexor for EIA/CCITT terminals or lines	3,400	32
DJ11-AB	Asynchronous 16-Line Multiplexor for use with external signal conditioning equipment	3,100	27
DJ11-AC	Asynchronous 16-Line Multiplexor for 20mA level conversion	3,200	32
DH11-AA/AC*	Programmable Asynchronous 16-Line Multiplexor and Mounting Panel with space for up to 4 DM11 line adapters (16 lines)	4,400	32
DH11-AB	Programmable Asynchronous 16-Line Multiplexor with data cable for connection to DC08 telegraph line interface	4,200	29
DM11-BB	Modem Control Multiplexor	1,295	19
DM11-DA	Line Adapter for 4 20mA terminals	170	5
DM11-DB	Line Adapter (4 EIA lines; includes four 25-ft modem cables)	485	5
DM11-DC	Line Conditioning	860	11
DP11-DA	Synchronous Line Module Set and System Unit	1,700	19
CA	Data/Sync Register Extender	400	3
KA	Internal Clock	300	3
DP11-DC	Same as DP11-DA, only suitable with direct use with 303 modems; includes 25-ft cable	2,100	19
DU11-DA	Full/Half-Duplex Synchronous Interface Data set control included	900	5
DQ11-DA	Full/Half-Duplex NPR Synchronous Interface with programmable transmission speeds up to 10,000 baud	2,800	24
DQ11-EA	Full/Half-Duplex Synchronous NPR Interface to Bell System 303 or equivalent modems	4,200	25
DQ11-KA	Crystal Clock Option	150	1
DC08-CS	Telegraph Line Interfaces (not for 11/45) Interface Panel (up to 16 DC08-CM dual-line adapters)	2,160	4
CM	1 Dual Telegraph Terminal and Receive Line Adapter	230	2
EB	Telegraph Line Current Adjustment Panel	2,160	2
D	Distribution Panel	1,080	2
793	Power Supply	540	7
893	Fuse Panel	1,080	–
H316-A,B*	Dual Telegraph Line Interface for 2 common carriers on private telegraph circuits	1,000	3
DR11-B	General-Purpose Direct Memory Access Interface	1,400	13

Notes:
* Starred submodel is 230V, 50/60 Hz version; unstarred submodel is 115V, 50/60 Hz version; some components are also available for 47 to 420 Hz.
(1) DEC does not rent equipment.
(2) Contact Digital in Maynard MA.
(3) Maximum total memory is 124K; system allowed max of 2 solid-state memory controllers. OEM models available for most equipment.
– Not Applicable NC No Charge NA – Not Available

A WISE System

(See Report 180.3451.100 for System Overview, Competitive Position, and Compatibility.)

MAINFRAME

The PDP-11 is a modular computer system designed to handle a broad range of problems. Model 11/40, the backbone of the line, is designed to operate in a multiprogramming environment, such as time-sharing, real-time control, data acquisition, or data communications applications. The 11/04, 11/05, and 11/10 are functionally slower than the 11/40. The PDP-11/45 can operate like a more powerful 11/40 with much higher throughput in a multiprogramming environment. It, like the 11/50, can be used in multiprocessor configurations, with dual-port MOS memory modules (see Figure 1). The 11/04 and 11/05 systems, on the other extreme, are small enough to be used in OEM applications and for single-device control. Hardware/software packages are offered in graphics, communications, industrial systems, laboratory systems, and many other areas.

Digital produces Unibus switches, data links, and communications devices to support multiple processor configurations for complete backup of critical processing facilities, for shared processing, and for processing networks.

Central Processors

Seven central processor models are available: the KD11-D (11/04), KD11-B (11/05 and 11/10), KC11 (11/15), KA11 (11/20), KAR11 (11/R20), KD11-A (11/35 and 11/40), and the KB11 (11/45 and 11/50). The 11/R20 is a ruggedized version of the 11/20.

KD11-B is a newer, smaller, microprogrammed version of the KA11. The KC11 implements only one external interrupt line and does not have a power fail/safe feature. It can be upgraded to a KA11 by adding three external interrupt lines and the power fail/safe option. The KC11 and the KA11 can be treated as if they were the same processor, since the KA11 is really a KC11 with its options incorporated as standard features. The KAR11 is a KA11 built to withstand harsh environments. The KB11 and KD11-A, also microprogrammed processors, have features unavailable for the other models: floating-point hardware, memory management, multiple processing modes, and memory to 124K words.

Data Structure. Each word consists of 16 bits divided into two 8-bit addressable bytes. Memory parity adds 1 bit per byte. Instructions are 1, 2, or 3 words long. Operands can be 1 word or 1 byte long.

Fixed-point arithmetic add and subtract use 1-word operands. Negative numbers are represented in two's complement form. Floating-point numbers use a 2- or 4-word format. They are represented by an 8-bit exponent (expressed in excess 128 notation) and a signed 24- or 56- bit fraction. The PDP-11/40 Floating-Point Processor (FPP) uses the 2-word floating-point format for operands; the 11/45 FPP uses both the 2-word and 4-word formats.

Special Registers

All PDP-11 processor models have a 16-bit processor status register (PS), and all except the 11/35, 11/40, 11/45, and 11/50 have eight general-purpose registers. The 11/35 and 11/40 have nine registers; the 11/45 and 11/50 have 16.

All addressing is done through the general-purpose registers. The instruction set operates on each of them in the same way and can use them as accumulators, address or stack pointers, or index registers. The addressing scheme provides a means to push items on or pop items off the stack pointed to by the specified register. Two registers also have special functions: one is a program counter (PC) and the other is a hardware stack pointer (SP) for interrupt handling. When an interrupt occurs, the hardware pushes the contents of PC and PS on the stack pointed to by the SP register.

The ability to operate on PC and SP in the same way as on the other registers adds some attractive features. Using PC as an address pointer or index register provides for immediate operands and relative addressing. Software routines can use the inherent stack manipulating capability with SP to gain access to the interrupt stack for processing.

The PDP-11/35 and 11/40 have two stack pointers, one for each processing mode — kernel and user. Only the stack pointer register corresponding to the current processor mode can be used by the program.

PDP-11/45 and 11/50 have duplicate sets of six general-purpose registers. A bit position in the processor status register selects the active set. One of the four other registers is the program counter. The three remaining registers are interrupt stack pointers, one for each of the three processor modes — kernel, supervisor, or user.

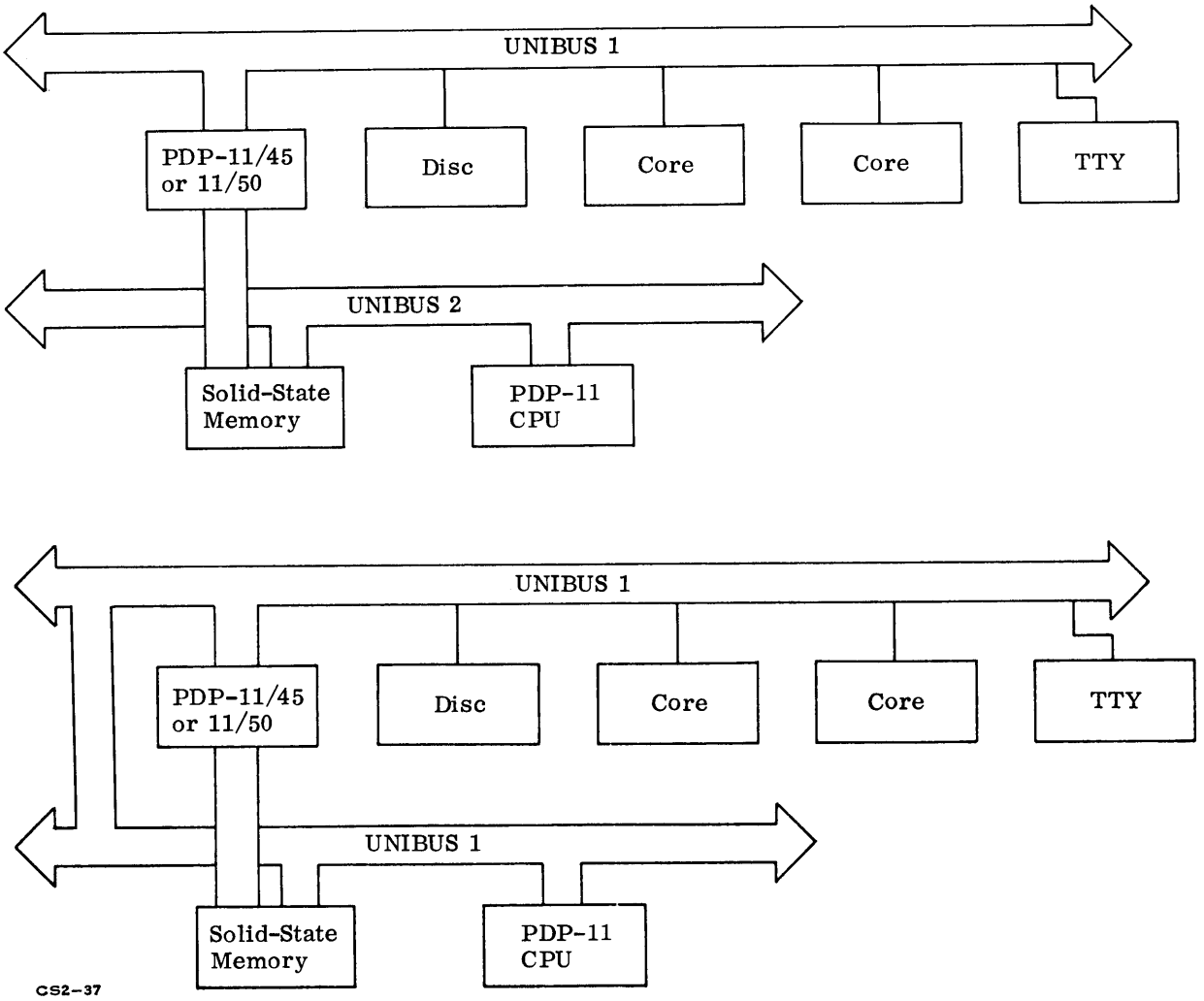

Figure 1. Digital PDP-11/45 and 11/15: Use of Multiple Ports to Solid-State Memory

The SP registers are used in conjunction with the memory management option to provide a fully protected multiprogramming environment.

The 16-bit processor status (PS) register controls and reflects processor status. PS stores a 3-bit processor priority code that operates as a mask for the interrupt system. It also stores a trap bit, which can be set or reset under program control to establish breakpoints for debugging programs and diagnostic routines, and a 4-bit condition code that reflects the outcome of the previous operation — negative, zero, overflow, or carry. Instructions are included to test condition code settings and to branch if the condition is met.

The 11/35 and 11/40 use 4 additional PS bits: 2 bits store the current processor mode; the other 2 bits store the previous processor mode. The 11/45 and 11/50 uses 1 PS bit in addition to those used by the 11/35 and 11/40 — this bit selects the internal general register set to be active. Figure 2 shows the PS register layout for all PDP-11 models.

Current processor mode for the four multimode models not only selects the appropriate SP register for storing PC and PS when an interrupt occurs but also selects the appropriate memory mapping registers in the memory management option for virtual addressing. The previous processor mode is used by the Return from Interrupt instruction to set the processor in the mode operating prior to the interrupt. The memory management option also uses it to pass data among user, supervisor (11/45 and 11/50), and kernel mode programs.

Processor mode bits are coded as follows:
- 00 — kernel (11/35, 11/40, 11/45, and 11/50).
- 01 — supervisor (11/45 and 11/50 only).
- 11 — user (11/35, 11/40, 11/45, and 11/50).

Processor Status (PS) Register

Use:	CPM	PPM	RS	U	P	T	CC			
							N	Z	V	C
Bits:	2	2	1	3	3	1	1	1	1	1

Notes:
CPM = current processor mode for PDP-11/35, 11/40, 11/45 and 11/50; unused for other models
PPM = previous processor mode for PDP-11/35, 11/40, 11/45, and 11/50; unused for other models
RS = register set active for PDP-11/45 and 11/50; unused for other models
U = unused
P = processor status
T = trap
CC = condition codes: N (negative), Z (zero), V (overflow), C (carry)

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Figure 2. Digital PDP-11: Processor Status Word Layout

Programs can set PS bits but cannot clear them; interrupts and traps always set PS with the bits in the interrupt or trap vector. The kernel can pass control outward to either supervisor or user mode programs by setting PS bits. Supervisor mode programs in turn can pass control outward to user mode programs but not inward to the kernel except via interrupts or traps. User mode programs cannot pass control back to either supervisor or kernel mode programs, except via the interrupt/trap system.

Certain instructions are privileged and can be executed in the kernel mode only. These are Halt, Reset, and Set Priority Level.

Floating-Point Arithmetic

The PDP-11/35 and 11/40 FPP is relatively simple. It provides four instructions for add, subtract, multiply, and divide and uses 2-word operands located in memory. The PDP-11/45 and 11/50 FPP, on the other hand, is more elegant; it includes its own set of six 64-bit accumulators, 16-bit status register, and program counter. Once the floating-point accumulators are loaded, the processor can continue processing while the floating-point operation is performed.

The FPP status register controls FPP and reflects the status of the result. If an error occurs, a floating error code (FEC) is stored and the FPP program counter points to the address of the instruction causing the error. All FPP interrupts are multiplexed into one interrupt vector; thus, the program must examine FEC to determine which error occurred.

Error codes are as follows:
0 — not used
2 — op-code error
4 — divide by zero
6 — integer conversion error
8 — overflow
10 — underflow
12 — undefined variable
14 — maintenance trap

Addressing Facilities. The PDP-11 has powerful addressing facilities. All addressing is done through the internal registers; therefore 16 bits are always available to address memory. Addressing is to the byte level, and up to 65,536 bytes can be addressed.

The upper 8,192 byte addresses, however, are reserved to address I/O device and other special-purpose registers, which means only 57,344 byte addresses (28,672 word addresses) can be used to address main memory. To address memory larger than 57,344 bytes, the processor requires the memory management option available only on the 11/35, 11/40, 11/45, and 11/50.

Instructions can address one or two operands, located anywhere in memory. This means memory-to-memory operations can be performed without using an accumulator. Each operand address field in the instruction word consists of 6 bits; 3 bits select the addressing mode, and the other 3 bits select the internal register used to calculate the address. Any general-purpose register — including the program counter and stack pointer — can be selected. The following eight addressing modes are provided:

- Register — operand is in an internal register.
- Register Deferred (indirect) — internal register contains the operand address.
- Auto Increment — internal register contains the operand address; register content is incremented by one for byte instructions, by two for word instructions, or by four or eight for floating-point instructions; provides for popping bytes or words off a stack (stacks are built downward in memory) or for stepping through memory; enables immediate addressing if PC is the internal register.
- Auto Increment Deferred (indirect) — this is the same as preceding except the addressed memory location contains the operand address; provides for popping addresses off stacks; enables absolute addressing if PC is the internal register.
- Auto Decrement — internal register content is decremented by one for byte instructions, by two for word instructions, or by four or eight for floating-point instructions; the new content is the operand

address; provides for putting bytes or words on a stack.
- Auto Decrement Deferred (indirect) — this is the same as preceding except the addressed memory location contains the operand address; provides for putting addresses on a stack.
- Indexed — internal register contains an index that is added to the content of the memory location following the instruction word to obtain the operand address; provides relative addressing if PC is the internal register.
- Indexed Deferred (indirect) — this is the same as preceding except the addressed memory location contains the operand address.

All PDP-11 processors use the same addressing scheme, but the 11/35, 11/40, 11/45, and 11/50 have additional memory management facilities.

Memory Management Facilities. The memory management facility for the PDP-11/35 and 11/40 is similar to that for the 11/45 and 11/50. The 11/45 and 11/50 facility is more complex chiefly because it has three processing modes while the 11/35 and 11/40 facility has two.

When the memory management option is incorporated in a PDP-11 system, calculated memory addresses are considered virtual addresses, which the option translates into physical addresses. Physical memory is divided into a maximum of 16 (11/35 and 11/40) or 48 (PDP-11/45 and 11/50) pages. The 16 pages for the 11/35 and 11/40 provide eight pages for each processor mode — kernel and user. The 48 pages of the 11/45 and 11/50 provide 16 pages (eight for instructions and eight for data) for each processor mode — kernel, supervisor, and user. Both data and instructions can reside in the eight instruction pages if data space is disabled.

Each page can contain from 32 to 4,096 words (1 to 128 blocks, 32 words each).

A 16-bit active page register (APR) that operates as a relocation register and a 16-bit page descriptor register (PDR) are associated with each memory page. A set of eight APRs and PDRs are associated with each processor mode's data (11/45 and 11/50 only) and instruction memory space. The three most significant bits of the virtual memory address select the current APR and PDR; the 13 least significant bits are a displacement address, which consists of a 7-bit block number (BN) and a 6-bit displacement in block (DIB).

The APR register contains four unused bits and a 12-bit page address field (PAF). The PAF and BN fields are combined to form a 12-bit physical block number (PBN). PBN is concatenated with DIB to form an 18-bit physical memory address. Figure 3 illustrates how the virtual address is converted to a physical address.

The active PDR contains status and control information for its associated memory page. PDR consists of an access control field (ACF), an expansion direction (ED) bit, 2 access information bits (A and W), and a 7-bit page length field (PLF).

ACF provides the following access modes:
- Nonresident — abort all accesses.
- Read/Write — memory management trap on completion of read or write (PDP-11/45 and 11/50 only).
- Read/Write — memory management trap on write (PDP-11/45 and 11/50 only).
- Read/Write — no system trap or abort action.
- Read Only — abort on write attempt; memory management trap on read or write (PDP-11/45 and 11/50 only).
- Read Only — abort on write attempt.

Besides the protection provided by ACF, the division of memory into I space and D space on the 11/45 and 11/50 provides execute-only protection for I space.

The ED bit determines whether blocks are added upward or downward in memory for page expansion. Changing the page length field (PLF) makes the page larger or smaller.

The A and W bits are used by the software. If any accesses to the page meet the trap condition specified by the ACF, A is set; W is set if the page is modified after APR is loaded. Both bits are reset if either APR or PDR is modified.

PLF stores the page length in blocks. A page length error occurs if BN of a virtual address is outside the range PLF specifies.

Four 16-bit program status registers (PSRs) are associated with the memory segmentation unit for the 11/45 and 11/50 and two for the 11/35 and 11/40. PSR 0, 1, and 2 are used to store error flags, the page number that caused the abort, virtual program counter (PC), and other status information needed by the software to recover from an error condition. PSR 3 enables or disables the use of the D (data) space APRs in user, supervisory, and kernel processor modes. When D space is disabled, all program addresses access the I space APRs for memory accesses. The 11/35 and 11/40 utilize only status registers 0 and 2.

All the memory management registers are located in upper memory in the 2K words below the space allocated to I/O device register addresses; thus, these registers can be manipulated in the same way as any memory location.

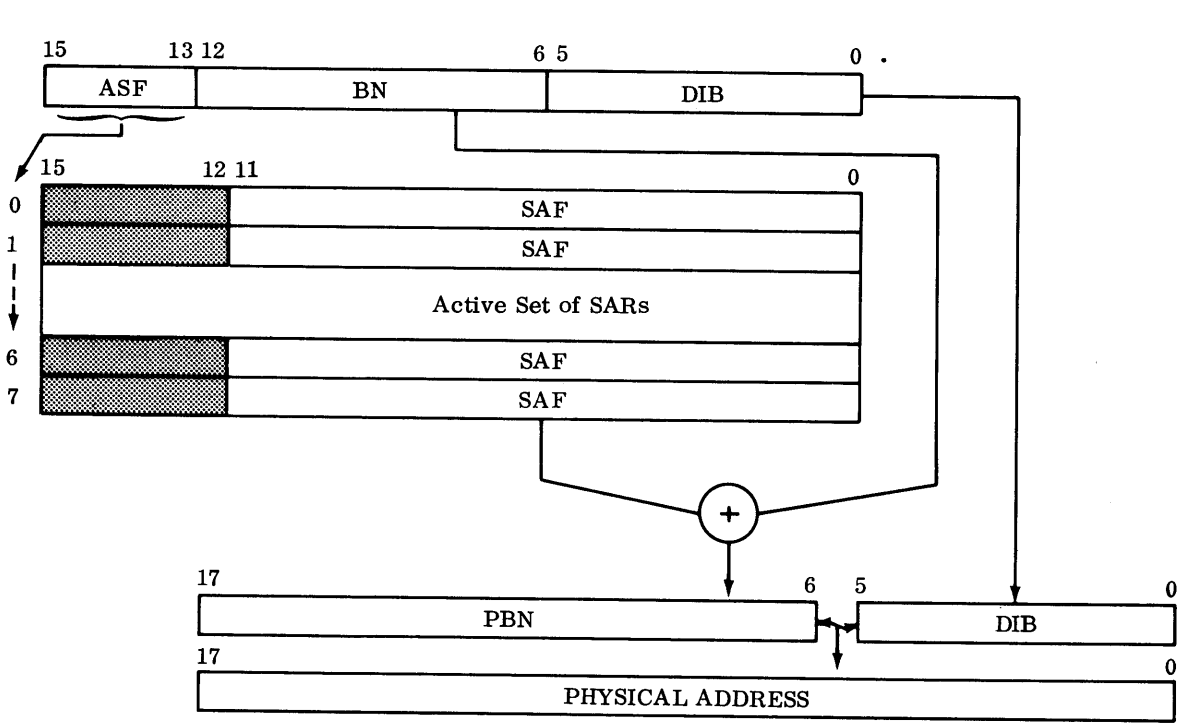
Instruction Set. PDP-11's instruction set is a powerful one and has several noteworthy features:
- The instruction format provides no direct addressing; all addressing is done through the internal registers.

- Stack manipulation is inherent in the addressing scheme; thus, no special stack instructions are needed.
- Most instructions are 2-address, so accumulators are not required for arithmetic or logical operations.
- The instruction set includes no I/O instructions because the addresses of the upper 4K words of memory are reserved to address I/O device registers. The full instruction set that addresses memory can be used to manipulate the contents of I/O registers.
- Most instructions can operate on either words or bytes; bits are manipulated via logical AND, OR, or Implication instructions.
- Only the PDP-11/45 and 11/50 include Multiply/Divide in the basic instruction set; the other processors require an extended arithmetic element (EAE) option to implement multiply/divide.
- Only the 11/35, 11/40, 11/45, and 11/50 have floating-point arithmetic hardware options; floating-point arithmetic is performed by subroutines on the other systems.
- All PDP-11 models use the same basic instruction set except that the 11/35, 11/40, 11/45, and 11/50 use supersets of the basic instruction set.

Instructions are 1, 2, or 3 words long. The first word always defines the instruction; the second and third words contain base values for the source and destination addresses in the indexed addressing mode.

The basic instruction set includes 70 instructions that perform the following operations:

- General Move; Compare; logical AND, OR, and Implication (clear), either byte or word.



Notes:

ASF = Active Segment Field

BN = Block Number

DIB = Displacement in Block

SAF = Segment Address Field

PBN = Physical Block Number

SAR = Segment Address Register: processor mode and type of memory access — instruction or data (PDP-11/45 and 11/50 only) — selects the active register set

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Figure 3. Digital PDP-11: Extended Memory Construction of a Physical Address

- Add/Subtract word.
- Increment; Decrement; Negate; Add/Subtract Carry, Test; and Shift/Rotate Right or Left byte or word 1 bit position.
- Jump; Conditional Branch; Exchange bytes in word; Return from Subroutine.
- Set or Clear condition bits; Halt; Wait; Return from Interrupt; I/O Trap; Reset (system); Emulator Trap; and Trap.

The Emulator Trap instruction is an interesting one. It can be coded to pass information to an emulating routine; 8 bits are available in the instruction for passing information.

The EAE option is a separate subsystem that connects directly to the Unibus and operates like an I/O device, asynchronous to the processor. It provides singleword multiply and divide, doubleword logical and arithmetic shifts, and doubleword normalize.

Hardware multiply/divide is standard on the 11/45 and 11/50. The 11/45 and 11/50 standard instruction set also includes logical eXclusive OR, Arithmetic Shift a single or double register right or left up to 32 bit positions, Sign Extend to Destination, Subtract One and Branch, Move To Previous mode's Instruction or Data space, and Move From Previous mode's Instruction or Data space.

The PDP 11/35 and 11/40 FPP uses four instructions, one each for add, subtract, multiply, and divide. Operands must be in the 2-word floating-point format.

The PDP-11/45 and 11/50 FPP option adds a full complement of instructions to perform single-precision (32-bit) and double-precision (64-bit) floating-point load, store, add, subtract, multiply, divide, and compare. Instructions for converting between integer (16-bit) or long integer (32-bit) and floating-point formats, as well as control instructions, are also included. All floating-point instructions use the six floating-point accumulators; thus, the processor can continue executing instructions once the floating accumulators are loaded.

The memory management options for the 11/35, 11/40, 11/45, and 11/50 also include a full set of instructions for program control.

Table 1 lists some typical instruction execution times for the PDP-11 processors.

Main Memory

PDP-11 main storage (except for the PDP-11/45 and 11/50, which are discussed separately later) consists of one or more storage modules of 4K, 8K, or 16K 16-bit words. Cycle time of standard 8K core modules is 0.9

Table 1. Digital PDP-11: Typical Instruction Execution Times

Instruction	Execution Time (μsec)(1) PDP-11/04 (2)	PDP-11/05, 11/10 (3)	PDP-11/15, 11/20 (4)	PDP-11/35, 11/40 (5)	PDP-11/45, 11/50 with Different Memories (6) Core	MOS	Bipolar
FIXED POINT							
MOVE (reg to memory)	3.4	5.4	3.7	2.42	1.84	1.01	0.75
MOVE (memory to reg)	3.1	3.9	3.8	2.24	1.84	1.01	0.75
Add/Subtract	3.4(2)	4.2	3.8	2.66	1.84	1.01	0.75
Multiply	6.6	7.5	6.7	9.66	4.68	3.86	3.60
Divide (avg)	7.4	7.8	7.0	11.30	8.58	7.76	7.50
FLOATING POINT	Subroutine	Subroutine	Subroutine				
Load				–	4.80/4.80	3.37/3.37	3.00/3.00
Store				–	4.80/4.80	3.37/3.37	3.00/3.00
Add (avg)				18.78	4.80/6.46	3.37/5.42	2.80/5.20
Subtract (avg)				19.08	4.80/6.46	3.37/5.42	2.80/5.20
Multiply (avg)				29.00	4.80/8.16	3.37/7.12	3.00/6.00
Divide (avg)				46.72	4.80/9.86	3.49/8.82	3.00/8.60
Multiply(7)				–	7.30/14.20	4.80/12.30	4.20/11.80
Divide(7)				–	7.30/17.50	4.80/15.40	4.20/15.00

Notes:
(1) Times depend on addressing modes; these times assume addressing mode 1; register contains operand address.
(2) Add/subtract register to memory; add/subtract memory to register 3.1 μsec.
(3) Core cycle time: 1.2 μsec per word.
(4) Core cycle time: 950 nsec per word.
(5) Core cycle time: 900 nsec per word. Memory management feature adds 150 nsec per memory access.
(6) In mixed-memory systems, times vary if instruction and data are in different types of memory. These items assume data and instructions in same memory type. Memory Management feature adds 90 nsec per memory access. Core, MOS, and bipolar memories have cycle times of 900, 450 and 300 nsec, respectively. Floating-point processor operates in parallel to CPU once operands are loaded; thus CPU can continue executing instructions during floating-point calculation. First number given is CPU time; second is floating-point processor execution time. Single-precision operands, 8-bit exponent and 24-bit signed fraction, except where noted.
(7) Double-precision operands, 8-bit exponent and 56-bit signed fraction.

microsecond per word. Cycle time of 16K-word core modules is 980 nanoseconds. Cycle time of 4K MOS modules used on the 11/04 is 725 nanoseconds. If total core storage equals 16K or more words, each 16K bank can be supplied as two interleaved 8K modules. All core modules have only one port of entry.

Memory parity checking is not a standard option but is available by special order. The standard processor can address 32,768 words of memory, but total memory capacity cannot exceed 28,672 words because memory addresses above 28,672 are reserved to address I/O device registers.

The PDP 11/35, 11/40, 11/45, and 11/50 have a standard expansion capability to address 131,072 memory words for a maximum memory of 126,976 words. Memory expansion beyond 28K words is available on special order for other PDP-11 systems.

The first 256 words of memory are commonly used for storing the processor status and addresses for interrupt servicing routines.

In addition, 32-word, customer-programmable, read-only memory modules are available for various purposes. There are also read-only modules programmed as bootstrap loaders for paper tape or mass storage.

PDP-11/35, 11/40, 11/45, and 11/50, like the other PDP-11 processors, reserve memory addresses 28,673 to 32,767 for addressing I/O device and other special-purpose registers. The PDP-11/35, 11/40, 11/45, and 11/50, however, concatenate 2 high-order bits with these addresses and map them into physical addresses 126,977 to 131,071.

The memory parity option checks for parity errors on memory read operations and generates an interrupt when a parity error is made.

The memory management option for the 11/35, 11/40, 11/45, and 11/50 checks for errors on memory access. If a memory access is not in accordance with the parameters set in the page segment descriptor register, the action taken is that provided by the access control field (see previous discussion of PDP-11/35 through 11/50 addressing).

PDP-11/45 and 11/50 Memories. The PDP-11/45 and 11/50 main memory can consist of up to 126,976 words of core memory, 32,768 words of MOS memory, 8,192 words of bipolar semiconductor memory, or a mixture of all three with a maximum memory capacity of 126,976 words. Memory expansion beyond 28,672 words requires the memory segmentation option. The central processor can support two semiconductor memory controllers; each controller can support either four 1,024-word modules of bipolar or four 4,096-word modules of MOS memory. Thus, semiconductor memory can consist of a total of 32K words of MOS, 8K words of bipolar memory, or 16K words of MOS and 4K words of bipolar memory.

The chief differences between the two models are in basic system packages. The 11/45 is all core, and the 11/50 is either all MOS or MOS and core mixed. Larger 11/45 and 11/50 systems can be expanded in such a way as to look identical, however.

Each memory word consists of 16 bits, two 8-bit bytes. The memory parity option adds 1 bit per byte. Memory cycle time is 900 nanoseconds per word for core memory, 495 nanoseconds per word for MOS memory, and 300 nanoseconds per word for bipolar memory. The 16K 980-nanosecond core module is available to either system.

Each 8K core memory module operates independently of all other modules and interfaces directly to the Unibus. Memory addresses are interleaved between two 8K modules in increments of 16K words. An odd 8K module in a system is not interleaved. Interleaving produces an effective memory cycle time of 650 nanoseconds for consecutive accesses to sequential core memory locations in operations such as I/O.

Core memory modules with different cycle times can be intermixed on a system. All core modules now available have a single port of entry.

All semiconductor memory modules for the 11/45 and 11/50 have two ports of entry. One port communicates with the processor via an internal bus. The other port can connect to the system Unibus or to the Unibus of a second PDP-11 family processor in a multiprocessor configuration. The dual-bus arrangement allows the processor to execute instructions from semiconductor memory simultaneously with data transfers between peripheral devices and core memory; see Figures 1 and 2.

Interrupt Control. PDP-11 interrupt system, except for the 11/35, 11/40, 11/45, and 11/50, consists of a 5-level internal trap system and a 1- or 4-line external interrupt system. When four lines are implemented, they are arranged in a priority sequence. All internal interrupts have a higher priority than external interrupts. The processor always operates at the priority level established by the processor priority code in the processor status register. This code inhibits all interrupts of an equal or lower priority level.

Traps are provided for bus errors, trap instructions, trace bit set, processor stack overflow, and power failure. Trap instructions include Input/Output Trap, Emulator Trap, and Trap. Halt, Wait, and SPL instructions trap on the 11/35, 11/40, 11/45, and 11/50 except in kernel mode.

The external interrupt system provides interrupt capability to devices connected to the Unibus. Any number of devices can interface to an interrupt line; the device

nearest the processor on the Unibus has highest priority on the line to which it is attached. This standard system has no practical limit for the number of interrupt levels that can be implemented.

The processor services an interrupt request at the end of the current instruction if the processor priority is lower than the priority of the interrupt request, no higher-priority interrupts are pending, and no devices are requesting nonprocessor data (DMA) transfers. The processor priority level is set in the processor status register (PS) automatically to provide an interrupt mask during the execution of interrupt servicing routines.

When an interrupt is granted, the interrupting device replies by sending an interrupt vector to the processor. The processor stores (pushes) the contents of PS and PC on the processor stack pointed to by the stack pointer (SP) register and loads PS and PC from the core location pointed to by the interrupt vector. Execution time of this automatic sequence is 8.7 microseconds for the 11/05 and 11/10, 7.2 microseconds for the 11/15 and 11/20, 5.2 microseconds for the 11/35 and 11/40, and 2.5 microseconds for the 11/45 and 11/50.

These stack operations give infinite nesting capability for interrupt requests, limited only by the size of the program-controllable stack.

The interrupt servicing routine is released with a Return from Interrupt instruction, which restores PS and PC from the processor stack; execution time is 7.8 microseconds for the 11/05 and 11/10, 4.8 microseconds for the 11/15 and 11/20, 2.9 microseconds for the 11/35 and 11/40, and 1.5 microseconds for the 11/45 and 11/50.

PDP-11/35, 11/40, 11/45, and 11/50 Interrupt Control. On PDP-11 processors with multiple processor modes, all interrupt processing is done on the kernel mode level. All interrupts and traps switch the processor to the kernel mode via the interrupt or trap vector. User (and supervisor on the 11/45 and 11/50) mode programs can call kernel mode programs only through the trap/interrupt system.

Like the other PDP-11 models, the PDP-11/35, 11/40, 11/45, and 11/50 interrupt systems consist of an internal interrupt system and a 4-line multilevel external priority interrupt system. Interrupts are serviced through trap/interrupt vectors in all PDP-11 systems.

The 11/35, 11/40, 11/45, and 11/50 have more interrupt/trap conditions than the other processors due to multiple processor modes and memory management and FPP options. The 11/45 and 11/50 also include a 7-level software interrupt facility; thus, different parts of an interrupt servicing routine can be queued for execution at lower priority levels. Table 2 lists the PDP-11 processor service hierarchy for traps, interrupts, and I/O transfers.

I/O Control

I/O devices communicate with the processor, memory, and other I/O devices via the Unibus. The Unibus contains 56 control, address, and data lines. Normally, the Unibus is under control of the processor. When a device requires bus control, it signals a request for bus use over one of the four BR interrupt lines or over the NPR (nonprocessor request) line. Devices signal interrupt requests via the BR lines and data transfer requests via the NPR line.

When a device is granted bus control following a BR request, it immediately sends an interrupt vector to the processor; the processor uses the interrupt vector as a pointer to the device's interrupt servicing routine.

Devices connected to the NPR line must be able to assume master control of the bus, to address a slave unit, and to transfer data independently of the processor. The data transfer can be between the master device and any slave unit. Normally the slave unit is memory; but it can be any slave device, such as a display or printer.

The processor services BR bus requests at the end of the current instruction and NPR requests at the end of the current bus cycle. All NPR requests have a higher priority than BR requests. The BR request lines have the following priority sequence from highest to lowest, BR 7 through BR 4. When more than one device is connected to the NPR line or to a BR line, the device nearest the processor on the Unibus has highest priority.

When a master gains bus control, it asserts bus Busy and places address and control information on the bus as well as an MSYN (master synchronization) signal. The slave device must respond with a SSYN (slave synchronization) to complete the transfer. Once the master receives SSYN, it stops asserting bus Busy so control can be passed to another master device. This signal response arrangement makes communication independent of device speed and distance between devices.

Each master keeps track of time between MSYN and SSYN signals. If an SSYN signal is not put on the bus within 5 microseconds after an MSYN, the processor traps.

Maximum data transfer rate over the Unibus is 2.5 million 16-bit words per second.

Addresses of the upper 4K words of memory are reserved to address I/O device registers, and the processor communicates with I/O devices through these registers. To the processor, an I/O device looks like a memory location.

PERIPHERALS

Digital supplies a broad range of peripherals for the PDP-11, including conventional low-speed devices, high-speed mass storage devices, special-purpose interfaces for

Table 2. Digital PDP-11: Processor Service Hierarchy for Priority Interrupt System, Traps, and I/O Transfers

Priority Level	Condition (1)	Action	Interrupt Vector	Comments
0	Odd address	Trap	4	Address not on even-byte boundary
0	Fatal stack violation (red)	Trap	4	16 locations above red boundary
0	Page violation (11/35, 11/40, 11/45, 11/50)	Trap	10	Violation of access code or page boundary
0	Timeout	Trap	4	No slave sync signal on Unibus for 5 μsec after master sync signal
0	Parity error	Trap	4	With parity option
1	FPP data transfer request (11/45 and 11/50 only)	Bus cycle	—	FPP = floating-point processor
2	Console flag	Console control	—	—
3	NPR (single cycle)	Cycle steal	—	Transfers 1 word between memory and I/O device
4	Console flag (single instruction)	—	—	—
5	Page management trap condition (11/35, 11/40, 11/45, 11/50)	Trap	250	Error in option
6	Warning stack violation (yellow)	Trap	4	16 locations above yellow violation
7	FPP execution trap (11/35, 11/40, 11/45, 11/50)	Trap	244	Error condition in FPP
8	Power/fail	Trap	24	—
—	CPU priority level 7	—	—	Masks out all interrupts or traps below priority level 8
9	PIRQ 7 (11/45, 11/50)	Trap	240	Software interrupt
10	BR7 (external interrupt on BR7 line)	Interrupt	Device dependent	From external device
—	CPU priority level 6	—	—	Masks interrupts below level 10
11	PIRQ 6 (11/45, 11/50)	Trap	240	Software interrupt
12	BR6 (external interrupt on BR6 line)	Interrupt	Device dependent	From external device
—	CPU priority level 5	—	—	Masks interrupts below level 12
13	PIRQ 5 (11/45, 11/50)	Trap	240	Software interrupt
14	BR 5	Interrupt	Device dependent	From external device
—	CPU priority level 4	—	—	Masks interrupts below level 14
15	PIRQ 4 (11/45, 11/50)	Trap	240	Software interrupt
16	BR 4	Interrupt	Device dependent	From external device
—	CPU priority level 3	—	—	Masks interrupts below level 16
17	PIRQ 3 (11/45, 11/50)	Trap	240	Software interrupt
—	CPU priority level 2	—	—	Masks interrupts below level 17
18	PIRQ 2 (11/45, 11/50)	Trap	240	Software interrupt
—	CPU priority level 1	—	—	Masks interrupts below level 18
19	PIRQ 1 (11/45, 11/50)	Trap	240	Software interrupt
—	CPU priority level 0	—	—	Masks interrupts below level 19
*	T-bit set and not RTT instruction	Trap	14	Causes a trace trap if RTT instruction is not being executed

Notes:
(1) All processors do not have all interrupt and trap conditions. PDP-11/15 has only 1 BR interrupt line; only the PDP-11/45 has the 7 PIRQ (Program Interrupt Requests); the 11/40 and 11/45 have other traps as noted.
* Serviced after all other conditions but not locked out by any processor level.

connecting noncomputer devices to the PDP-11, and data communications interfaces.

Low-Speed Peripherals. Low-speed peripherals are fully supported by the PDP-11 software. All of them interface with the PDP-11 via the Unibus. All except the CD11 Card Reader operate under program transfer control.

TELETYPE

LT33-D Teletype ASR 33 (includes paper tape reader and punch), LT33-C Teletype KSR 33, LT35-D Teletype ASR 35 (includes paper tape reader and punch), LT35-C Teletype KSR 35 — all are 10 cps, and require KL11-A controller or DM11-DA, DL11-A or C interfaces.

PAPER TAPE

PC11 High-Speed Paper Tape Reader/Punch — reader, 300 cps; punch, 50 cps.

PR11 High-Speed Paper Reader — 300 cps.

PUNCHED CARD

CR11 Card Reader (80-col cards) — 300 cpm.

CM11 Optical Mark Sense Card Reader (40-col EIA std punched cards) — 200 cpm.

CD11 High-Speed Punched Card Reader (80-col cards) — 1,000 cpm; transfers data direct to memory.

CD11-E High-Speed Punched Card Reader (80-col cards) — 1,200 cpm; transfers data direct to memory.

PRINTERS

LS11 Printer — 132-col line; 64-char set; 60 lpm.

LV11 Electrostatic Printer/Plotter — 132-col line; 96-char set; 500 lpm; 120,000 dots/sec.

LP11-F/LP11-J Printer — 80-col/132-col line; 64-char set; 300 lpm.

LP11-H/LP11-K Printer — 80-col/132-col line; 96-char set; 300 lpm.

LP11-R Printer — 132-col line; 64-char set; 1,200 lpm.

LP11-S Printer — 132-col line; 96-char set; 800 lpm.

High-Speed Peripherals. Digital continues to supply its ever-popular block addressable DECtape for small PDP-11 systems; industry-compatible magnetic tape units for larger systems requiring more storage and speed; and both fixed-head, high-speed discs, and movable-head disc cartridge units for large systems. All mass storage devices request access to the Unibus for a data transfer via the NPR line, the PDP-11 DMA facility.

MAGNETIC TAPE

TU56 Dual DECtape Transport — block-addressable tape unit; storage capacity 146,968 wd/tape; transfer rate 5,000 wd/sec; requires TC11 controller, which can handle up to 4 TU56 units; transfers data via NPR.

TU56-H Single DECtape Transport — block-addressable tape unit; storage capacity 146,968 wd; transfer rate 5,000 wd/sec; requires TC11 controller, which can handle up to 8 TU56-H units; transfers data via NPR.

TJU16 Magnetic Tape System — 9-track, 800 bpi-only drive and 800-bpi NRZI/1,600-bpi PE drive; 8 drives/controller.

TA11 Dual Cassette — 96K-byte storage; 550 bytes/sec transfer rate.

TU10-F Magnetic Tape Transport — 7-track tape; 200/556/800 bpi; 45 ips; 36K bytes/sec transfer rate; requires TM11, which can handle up to 8 TU10 units; transfers data via NPR; uses 0.5-in. industry-std tape.

DISC

RS03/RS04 Fixed-Head Discs — 256K-wd or 512K-wd slave drives, respectively; up to 8 total can be mixed on RJS03 (256K) or RJS04 (512K) masters; 8.5-msec avg access time; RJS03/RS03 transfer rate can be 4 or 8 msec/wd; RJS04/RS04 transfer rate is 4 msec/wd.

RJP04 3330-Type Moving Head Disk Subsystem — 44M wd/pack, 28-msec avg access; 403K wd/sec transfer rate, 8 drives/subsystem.

RS64 Fixed-Head DECdisk — storage capacity 64K wd; transfer rate 62,500 wd/sec; avg latency 16.9 msec; data stored in 32-wd sectors, 64 sectors/track, 32 tracks/disc; requires RC11 Controller, which can handle up to 4 RS64 drives; transfers data via NPR.

RS11 Fixed-Head Disk — storage capacity 262,144 wd; transfer rate 62,500 wd/sec; avg latency 16.9 msec; stores data in 32-wd sectors; 128 sectors/track; 128 tracks/disc; requires RF11 controller, which can handle up to 8 RS11 drives; transfers data via NPR.

RK05 DECpack Removable Disk Cartridge Drive — storage capacity 1.3M wd; transfer rate 90,252 wd/sec; head positioning time 12 to 85 msec; avg rotational delay 20 msec; uses disc cartridge similar to IBM 2315; requires RK11 controller, which can handle up to 8 drives; transfers data via NPR; fully supported by DOS; RSTS can utilize DECpack for file storage, swapping, and/or systems device.

RP03 Removable Disk Pack Drive — storage capacity 20.5M wd; transfer rate 134,600 wd/sec; head positioning time 7 to 29 msec; avg rotational delay 15 msec; requires RP11-C controller, which can handle up to 8 drives; transfers data via NPR; fully supported by RSTS and RSX-11D.

Special-Purpose Peripherals

A number of special-purpose peripherals for interfacing noncomputer devices to the PDP-11 are available. All special-purpose interfaces connect to the Unibus and transfer data under processor control, except the DR11-B General-Purpose Digital Interface, which transfers data directly to/from memory.

The GT40 and GT42 are total graphics systems that use the PDP-11/10 or PDP-11/40 respectively, as the controller.

CLOCKS

KW11-L Real-Time Clock — line frequency.

KW11-P Programmable Real-Time Clock — line frequency, 10 kHz, 100 kHz, or external trigger; program selectable; internal counting or interval repeat, programmable.

GRAPHIC DISPLAYS

EG11 Graphics Subsystem with controller — 42 x 73 characters/dot matrix VT11 display.

VT01 Tektronix 611 Storage Tube Display — display rate 30 Hz to 10 kHz; requires AA11-A controller.

VR01A Tektronix RM503 Oscilloscope Display — display rate 45 kHz max; requires AA11-B controller.

VR14-7- x 9-in. Point Plot Display — display rate 40 Hz to 40 kHz; requires AA11-C controller.

ANALOG TO DIGITAL

AD01-D Analog to Digital Conversion Subsystem — 10-bit unipolar or 10-bit + sign bipolar converter; mux controls 4-32 channels of high-level, single-ended inputs; conversion time of 22 μ sec; computer or external clock control; full-scale range of 0.0 to +10.0 V; program-selectable input gain.

AFC11 Low-Level Differential Analog Input Subsystem — 13-bit converter; programmable gain; 32 channels expandable to 128 channels.

LPS11-S Laboratory Peripheral System — 12-bit converter; clock; display controller; 8-channel MUX; 16-bit I/O; DMA access opt.

DIGITAL TO ANALOG

AA11-D Digital to Analog Converter Subsystem — 11 bits + sign converter; 4 channels; 1-4 converters; adjustable full-scale output voltage, 0 to + 10V at 10 ma; conversion time of 20 μ sec; output impedance less than 1 ohm; single buffered unit, storage scope, display scope options available; can interface to AA11-A, B, C.

DIGITAL CONTROL

UDC11 Master File — provides for 4 functional I/O modules (64 digital points) expandable to 16 digital wds (256 digital points).

M1623 I/O Interface — transfers wds or bytes to digital voltmeters, multimeters, and programmable power supplies; instruments connect directly to M1623 via cables.

M1621 I/O Interface — transfers data and status information from multimeters and voltmeters to PDP-11; includes self-contained bus drivers, multiplex and interrupt logic to access 34 bits of TTL-level data.

DATA COMMUNICATIONS

The PDP-11 has a complete line of data communications hardware and software for using the computer as a remote terminal controller (including 2780 emulation), data concentrator, front-end preprocessor, or store-and-forward message switcher. The COMTEX-11 communications software is modular and expandable. It provides user-level system control, system-level task scheduling, and system-level task support.

DN11 801 Dialer Control — dialer for Bell 801 automatic calling unit; up to 4 dialers in 1 system unit.

DL11 Full Duplex Asynchronous Line Interface Unit — for transmission speeds of 110, 150, 300, 600, 1,200, and 2,400 baud; for replacement purposes only; DL11 now replaces KL11.

DJ11 Asynchronous 16-line Multiplexors — customer-specified char size, speed, parity, stop bits; models for EIA/CCITT terminals or lines, external conditioning equipment like DC08 telegraph interfaces, and 20 ma level conversion.

DP11 Synchronous Line Module Set and System Unit — half-/full-duplex; double buffered for use with 201 or 303 modems; data sync register (for 10 to 12-bit char) and internal clock (up to 40.8K baud) options.

DC11 Dual Asynchronous Line Control — 4 program-selectable speeds, 50-10,000 baud; can split transmit and receive speeds; 1 or 2 line controls/unit; programmed char length, parity; allows DF11 Series line interfaces, full modem control.

H312A Null Modem Box — mounts 2 female RS232 connectors with jumper options to allow direct connection of data terminals (without intervening modems) or EIA-type peripherals to DC11; allows PDP-11 communications to connect to any RS232 peripheral or to another PDP-11.

DH11-AA/AB/AC Asynchronous 16-Line Multiplexors — for EIA/CCITT terminals or lines, external signal conditioning equipment (like DC08 interfaces), or 20 ma level conversion; all are programmable on an individual line basis for character size, baud rate, parity, and stop bits.

DH11-BB Multiplexors — for 16 lines of full modem control for Bell 100 Series and 202 modems; option for DH11-AA Series; used with DC08 TTY-level equipment.

DH11-DA/DB/DC Line Termination Interfaces — for 4 TTY/EIA/EIA lines; DA and DB for data only, DC has both data and control interfaces; option for DH11-AA Series.

DU11 Full-/Half-Duplex Synchronous Interface — up to 9,600 baud, for Bell 200 Series.

DQ11 Full-/Half-Duplex NPR Synchronous Interfaces — for up to 10,000 baud on Bell 200 Series or similar EIA/CCITT termination; for 1.0M baud on Bell 303-type modems; crystal clock option.

DC08 Telegraph Interface — up to 32 lines.

The terminals listed below include a 30 character-per-second page printer data terminal (LA30) as well as an alphanumeric VT05 CRT display, standard Teletypes, and data entry terminal for data collection systems.

TELETYPE

LT33-D Teletype ASR 33 (includes paper tape reader and punch) — 10 cps; requires KL11-A or DL11-A controller.

LT33-C Teletype KSR 33 — 10 cps; requires KL11-A or DL11-A controller.

LT35-D Teletype ASR 35 (includes paper tape reader and punch) — 10 cps; requires KL11-A or KL11-A controller.

LT35-C Teletype KSR 35 — 10 cps; requires KL11-A or DL11-A controller.

DECWRITER

LA30-P DECwriter — includes printer and 96/128-character keyboard; 132 cols; 30 cps; requires LC11-A controller.

LA36 DECwriter — includes printer and 96/128-char keyboard; 132 cols; 30 cps; DF11 Series communications interfaces and 11-key numeric pad optional.

ALPHANUMERIC DISPLAY

VT05 CRT Display — includes keyboard, full- or half-duplex transmission; 110-2,400 baud async; 20 lines, 72 char/line, internally buffered; EIA or 20-ma current loop operation; requires KL11 or DL11 controller or connects to 103 Series modem.

SOFTWARE

Digital offers a wide spectrum of software for the PDP-11: general-purpose operating systems, language processor, special-purpose operating systems and packages, other support facilities, and applications software. A Paper Tape Programming system is used for minimum configurations, while the Cassette Operating System offers all the advantages of a true operating system for a cassette-based, 4K-word system. Disc Operating System (DOS) for batch processing, RT-11 for single-user interactive processing, and RSTS for time sharing run on larger configurations. The extensively developed RSX-11 Real-Time Multiprogramming Executive takes advantage of the capabilities of the high end of the PDP-11 line. A COMTEX communications package runs under DOS. MUMPS-11 provides data management facilities. Language processors include assemblers, BASIC, FORTRAN IV, COBOL, and FOCAL. A data base management system called Wheaton Information System for Education (WISE) runs under RSTS.

Operating Systems

DOS. DOS is a keyboard-oriented system for program development and execution. It provides the user with

access to system programs, performs I/O transfers, and manages secondary storage in response to control commands from the Teletype or from the user program. The user can generate, edit, assemble or compile, debug, load, save, call, and run programs under DOS control.

DOS organizes memory into five areas:

- User area — stores user programs and buffers.
- Stack — temporarily stores parameters while control is passed between routines.
- Free memory or buffered area — divided into 16-word blocks that can be assigned to temporary tables, device drivers called in from the disc, data buffering, or user programs.
- Resident monitor — contains all permanently resident routines and tables.
- Interrupt vectors — point to the interrupt servicing routines.

Control commands are also provided to define data format; to obtain time of day, date, and system status; and to specify special device functions. Programmed control commands are incorporated in a user's assembled program.

DOS is modular and open ended; it allows a user to add programs as needed for a particular application. The BATCH system adds job-stream processing to the DOS system.

RSTS. The Resources Time Sharing System (RSTS) is available in two versions, the initial RSTS-11 and the enhanced RSTS/E version. The two differ mainly in system size and peripherals supported. RSTS-11, which runs on a PDP-11/20, 11/30, or 11/45 with 48K to 56K bytes of memory and RS11 or RK05 swapping disc, can support up to 16 users with maximum program size per user of 16K bytes. RSTS/E, which runs on a PDP-11/40 or 11/45 with 80K to 248K bytes of memory with an RS11 or 40M-byte PR03 swapping disc, can support up to 32 users with maximum program size per user of 32K bytes. Memory parity is required on RSTS/E configurations but it is optional on RSTS-11. RSTS/E can support the 1,200-lpm LP11 line printer or multiple line printers; it can store the run-time system in high-speed MOS memory (300-nanosecond cycle time); it also has a comprehensive error logging facility.

An RSTS system uses the BASIC Plus interactive language; it allows each user exclusive access to all peripherals except the shared disc. Data base management routines allow disc files to be created, updated, extended, and deleted interactively. Files can be random or sequential, and they can be protected on an individual, group, or universal basis. Up to 12 files are simultaneously available to each user. Commercial processing facilities provide sort/merge, indexed file access methods, decimal arithmetic, and printer spooling. The system usage accounting feature makes available on-line reporting of status, peripheral and memory usage, run time, and so on.

RT-11. This Real-Time Operating System is a core-based or disc-based system; it was designed to support a single interactive user developing programs in a scientific or research environment. The RT-11 runs on any PDP-11 with at least 8K words of memory, console terminal, and either tape or disc drive plus paper tape or cassette I/O. The system can be run in configurations with up to 28K words of memory without modification.

RT-11 fully supports the Laboratory Peripheral System (LPS-11), which enables the user to sample and display problems from A/D converters and digital I/O, in real time. LPS-11 commands are initiated by the BASIC RSTS-11 Call statement.

MUMPS-11. MUMPS (Massachusetts General Hospital Utility Multiprogramming System) is a compact single-language, time-sharing system designed for use primarily as a data management system. It was developed by the Laboratory of Computer Sciences, Department of Medicine, Massachusetts General Hospital and Harvard Medical School. The development effort was supported by Grant HS00240 from the National Center for Health Services Research and Development and by Grant GM15287 from the National Institute of Health. The MUMPS system consists of a time-sharing monitor, I/O monitor, reentrant interpreter, and set of utility routines.

The MUMPS time-sharing monitor contains facilities to support the DECdisk, the RP02 Disk Pack, DECtapes, paper tape reader/punch, and a set of terminal scanners used to interface remote devices, such as Teletypes, buffered display scopes, and line printers. Core memory, exclusive of the space required by the monitor and the interpreter, is divided into partitions, each partition containing an application program and its local data. All active users are assigned partitions of core memory. Activating a program requires finding an available partition and loading it with a program from the disc; as long as the program is active, it remains in core. The monitor also automatically overlays external program segments when required by an active program.

Proper linkages are arranged to return automatically to the program when execution of the segment terminates. Typically, 20 to 30 users can be simultaneously active; as many interactive terminals as required can interface to the system.

The MUMPS language is a JOSS-like, high-level, interpretive language that lets the programmer write, debug, edit, and run a program in a single interactive session at the terminal. The time-sharing and I/O monitors have been specifically designed to work efficiently with the interpreter. No attempt has been made to accommodate machine-language user programs.

RSX-11. Memory requirements for the five versions of RSX-11 vary: Version A can run in as little as 2K words of memory; C requires 12K words of memory; B

requires 12K words of memory plus disc storage; M requires 16K words of memory plus disc storage; and D requires at least 32K words of memory, disc storage, and the memory management option available only for the 11/35, 11/40, 11/45, and 11/50. Digital now actively markets only the M and D versions and supplies the RT-11 for single-user real-time systems. The A version was a very small foreground system. The B and C let up to 128 real-time programs run in the foreground with one batch program in the background; B was disc-based while C was core-based.

Digital Equipment Corporation's newest version of the real-time multiprogramming operating system is called RSX-11M. This smaller version of RSX-11D is also upward compatible with RSX-11D. RSX-11M can handle data acquisition, data manipulation, discrete manufacturing, process control, and laboratory data processing applications. A comprehensive file processing system and dynamic allocation of system memory contribute to fast system response time. With the introduction of the RSX-11M, the small system user can implement an operating system to fit his particular system size. Upgrading from the RSX-11M to the RSX-11D is easy since the same executive calls, operator commands, file system, disc layouts, data structures, I/O structure, and programs can be used on both systems.

RSX-11M requires a PDP-11 with a minimum of 16K words of memory, Teletype or DECwriter for the system console, 1.2-million word DECpack disc system, real-time clock, hardware bootstrap loader, and one additional storage unit: disc drive, DECtape, or cassette. Programs developed on a PDP-11/05, however, will not run under RSX-11D if the system is upgraded.

RSX-11M requires at least 16K words of memory to operate. Simultaneous real-time and background operation requires 24K words of memory. Any PDP-11 can be expanded to 28K words of memory, and the 11/35, 11/40, 11/45, and 11/50 can be expanded to 64K words with the memory management option. RSX-11M also supports secondary memory on disc, tape, or cassette. Overall system performance can be increased by upgrading the PDP-11 processor model or by adding a variety of peripheral equipment. The maximum task size in a system with memory management is 32K words; task size is limited to 28K words for a system without memory management. Up to 10 concurrent tasks can be run in 16K words of memory.

RSX-11M is an event-driven rather than clock-driven system. A significant event triggers task scheduling, interrupt, program execution, or program rescheduling. There are 250 task priority levels; the operator can assign or change a task's priority level when it is formed. Tasks are initiated by other tasks or by an operator. They can be scheduled to execute in response to time-of-day, at intervals, or in response to an external event. By using the interrupt system, RSX-11M determines which device caused the interrupt, and then executes the program specified. Interrupts can be generated by real-time events, as in a process control environment.

RSX-11M provides two source languages: MACRO-11 and FORTRAN IV. The Task Builder can combine one or more MACRO-11 or FORTRAN IV output files into a single task, create tasks with overlay structures, attach attributes to the task following language translation, and store the task on disc until it is retrieved for execution. A single task can be programmed using both FORTRAN IV and MACRO-11 source languages.

Tasks stored on disc are retrieved by name. The Task Builder creates a directory name entry for the task, and it links program requests for these tasks into the algorithm for searching and loading requested program sections. The Task Builder can incorporate any subroutine or reentrant library routine commonly used by the system, such as data and arithmetic conversions, into a task.

A checkpointing option allows the user to "roll out" copies of tasks to disc when a higher-priority task interrupts the system. When the higher-priority task is completed, the first task is "rolled in" at the point at which it had been preempted.

For system efficiency, RSX-11M allows multiprogramming of tasks. Two or more tasks are held in main memory waiting for system resources. Queued tasks are multiplexed to devices. System devices operate in parallel. Multiprogramming reduces response time and increases task throughput during peak loads.

Memory is divided into a number of fixed-size, named partitions which can be further divided into seven subpartitions. All programs held in partitions and subpartitions can execute concurrently in the multiprogramming mode. Each task is assigned a specific partition for execution. Language translation, which requires large areas of memory, can occur concurrently with system processing. Small tasks occupy subpartitions; they can reclaim partitions previously used for language translation to the system's available memory.

RSX-11M supports multitasking; that is, it allows tasks to communicate with each other. To maintain efficient response time, parallelism is induced in the single processor environment. A master task synchronizes the activity of the various tasks. Thus, every user task can become an Executive, extending the benefits of parallelism to all tasks.

System power is protected by power failure/restart under RSX-11M. When the system detects that the power is failing, the processor traps to the Executive. Volatile register contents are transferred to nonvolatile memory. The Executive resumes control of the system when power is returned and checks whether any user tasks have requested notification of power failure.

RSX-11M file management system comprises on-line automatic file allocation, file protection, random and sequential access, and fixed- and variable-length records.

- File allocation — allocating files on-line conserves memory space because space is not reserved in advance for a file of unknown size. Memory space can

be extended on-line, particularly useful during program development and debugging.
- File protection — a User Identification Code (UIC) is assigned to each file when it is created; this code identifies who can access the file: file owner, owner's user group, system, or all potential users.
- Random and sequential access — file management is independent of the method of file access, so all files can be accessed either sequentially or directly. For sequential access, the file buffer performs the blocking and deblocking of the record. For direct access, a complete block of data (256 words) is transferred directly to or from the buffers. Record numbers are used to call fixed-length records.
- Fixed- and variable-length records — file management controls the location of the record, whether fixed or variable in length. Whether the information resides in one or more buffers is transparent to the user.

Core, MOS, or bipolar memory can be used as primary storage to store the Executive and all associated routines, the I/O drivers and task loader, system tables, file system controls, monitor console routines (operator interface), user and system tasks, and shareable libraries and data areas.

The Executive is permanently memory-resident and provides the management facilities to allocate system resources. It resolves conflicts arising among tasks calling for the same system resources. The Executive schedules tasks on a priority and time-dependent basis, handles task I/O requests and intertask communication, and provides multiprogramming and check-pointing services. The power fail/system restart, memory partition management, and hardware memory management option support are controlled by the Executive. It is composed of modules assembled at system generation time to correspond to the needs of the user.

The I/O drivers are linked to the system at system generation time. They service interrupts, check addresses, and handle I/O queue management.

Monitor console routines provide communication between the user at the interactive terminal and the RSX-11M system to start, schedule, or abort a task.

The Executive creates a task partition directory, system task directory, clock queue, and I/O request queue for scheduling tasks. Memory is allocated at system generation time for directories and the queues. The amount of memory reserved is a function of the I/O activity, number of tasks, or amount of time-dependent scheduling.

System and user tasks are treated the same under RSX-11M. Each task is referenced by name and has its own priority. Each has a specific partition from which it executes, and it can be check-pointed. Tasks always occupy contiguous memory locations.

Packages commonly needed by more than one memory-resident task are contained in the shareable library. Library programs are in reentrant code, allowing access by several tasks executing at different priorities. A typical example of a shareable library package is the FORTRAN run-time package. Data commonly needed by several tasks is stored in contiguous memory areas called "commons."

Hardware memory management is implemented as an option at system generation; it is transparent to the user. Tasks developed on a system without memory management can run on any system with the option. Memory management provides protection for the Executive, between foreground and background tasks and among individual tasks. It also allows selective access (read/write, no access, read only) for different areas of the shareable files and provides for systems from 28K words of memory to 128K.

Program development is handled in the background mode under RSX-11M. New real-time programs can be created, tested, installed, and scheduled; existing programs can be modified. Background tasks can reside in main memory along with the real-time foreground programs. Smaller configurations can use the same memory for both; background tasks are brought in from disc only when no real-time tasks are in progress. Background tasks are automatically check-pointed and rolled out to disc when a real-time program needs the memory.

Program development facilities include preparation of the task, editing, translation into binary, task building, and task debugging.

Preparation and editing facilities include the source language input program (SLIPR), which simplifies creating new tasks and modifying existing tasks. Tasks can be added or edited from a terminal keyboard or they can be entered via disc or cassette.

The Macro-11 assembler and FORTRAN compiler translate ASCII source code into binary object modules. The macro assembler furnishes a complete listing of the symbolic program, including line number, memory location, octal representation, user macros, and user-generated mnemonics and comments. Object code is relocatable. Memory location assignment can be deferred until the code is linked with other object programs. The FORTRAN IV compiler is structured to make use of any advanced processor options, such as floating-point arithmetic. A comprehensive listing is output to aid the user in debugging and documenting the FORTRAN program. The listing includes the source program listing internal and external program symbols and program errors, and an object code; the listing is optional.

The Task Builder links the object modules with required subroutines and provides an automatic overlay capability. Large programs can be assembled in smaller

modules for ease of use. The Task Builder relocates each object module and assigns an absolute address; links the modules by correlating global symbols; optionally prints a load map displaying absolute addresses; searches the disc-resident library of subroutines and links subroutines containing global symbols requested by other modules; creates overlay segments; and outputs the final linked program to be loaded later by the Executive.

On-line Debugging Technique (ODT) operates interactively from a console terminal. The user can go through the execution of the program, make changes, and test the results. ODT can stop the program at up to eight user-defined breakpoints, skip the breakpoints, or continue execution upon demand.

Various utility programs are available. Peripheral interchange Program (PIP) performs transfers of data files from one device to another and performs some simple editing and control functions. File Verification Utility (VFU) allows the user to check the readability and validity of the file structure on any device. Librarian (LBR) system program allows the user to maintain, create, add, update, modify, or list additions to the library files. File Dump (DMP) produces a printed copy of the contents of a file. The file can be output to a line printer, keyboard, DECtape, or disc. File Exchange Utility program (FILEX) converts RSX-11M files to DOS-11 files and vice versa.

RSX-11M supports many hardware devices and software interfaces to communicate with other computers and operators. Asynchronous communication devices support line speeds of 110 to 2,400 baud, using ASCII code. Examples of these devices are the LA30 and 36 DECwriters with the VT05 A/N display and keyboard. These operate in a full-duplex mode and permit data entry and display.

Synchronous transmission is a more efficient means of communication when large amounts of binary ASCII data must be transferred between computers. RSX-11M can communicate with a DECsystem-10 over synchronous lines.

RSX-11D. The RSX-11D has all the features available for RSX-11M, and, in addition, is designed to make use of the 11/35, 11/40, 11/45, and 11/50 memory management option that allows dynamic memory allocation and hardware protection of individual tasks. RSX-11D is a real-time multiprogramming foreground/background operating system with tasks scheduled according to assigned priority levels that can be changed at run time. RSX-11D can also assign up to 250 priority levels for tasks. Direct access to hardware interrupts allows critical tasks to bypass system scheduling for service.

Tasks are stored on the disc in virtual format, that is, exactly as they will run in main memory. Task relocation and protection are performed by the memory management system by means of active page registers. The Task Builder determines which active page registers will be used and computes the contents for the task's access to common areas and reentrant library. These precalculations are stored with the virtual task. Thus, a task does not need to be changed no matter where it is loaded into memory.

I/O transfers on RSX-11D are performed on a queued, priority basis. I/O transfers for slow devices are spooled automatically to disc. All device handlers are implemented as tasks, allowing new ones to be developed and installed without modification (system generation) of the Executive. Tasks that require extremely fast response times can connect directly into the hardware interrupt structure and bypass the software scheduling algorithm.

A recent "TC/D" enhancement to RSX-11D provides up to 80 terminals with rapid access to the operating system. This enhancement reduces system overhead for multiple terminals by concentrating data from a number of terminals into a single high-speed line. Multiprocessing configurations enhance the effectiveness of the TC/D System.

Language Processors

DEC implements six major language processors for the PDP-11: PAL-11 assembler, Macro-11 assembler, FORTRAN IV, COBOL, BASIC, and FOCAL.

Assemblers. PAL-11 assembler is available in three versions: PAL-11A, PAL-11S, and PAL-11R. PAL-11A is a 2-pass assembler that produces absolute binary output code. A third pass is required for listing the output and punching a binary tape. PAL-11S is like the PAL-11A but produces relocatable output modules that can be linked by the LINK-11S Linker to produce an executable load module. PAL-11R operates under DOS and RSX-11D; it also produces relocatable output modules; the LINK-11 Linker produces executable load modules.

MACRO-11 is an extension of the PAL-11R assembler to provide macro definitions and calls.

FORTRAN IV. PDP-11 FORTRAN IV runs under DOS RSX-11M and RSX-11D. It is a full implementation of ANSI Standard FORTRAN IV with the following extensions:

- Random access I/O.
- Mixed-mode arithmetic.
- Generalized expressions for array subscripts.
- Implicit statements for data type of variables.
- Improved error diagnostics for error tracing.
- Arithmetic with 24- or 56-bit accuracy with or without the EAE option.
- One-word integers.
- Two output formats, one relocatable binary code and the other intermediate assembly code for custom modification.
- Extensive compiler diagnostics with text that can be omitted optionally.
- Comprehensive, reentrant math library and object run-time system.

The FORTRAN IV output code is compatible with both DOS and RSX-11; thus FORTRAN IV-generated programs can run under DOS and all current RSX-11 versions.

COBOL-74. The COBOL compiler conforms to the American National Standards Institute (ANSI) COBOL-74 specification x.3.23-1974. COBOL Sequential and Relative I/O modules meet ANSI specifications while the Nucleus, Table Handling, Segmentation, and Library modules offer the following extensions over and above ANSI's 1974 high-level specifications (which include ACCEPT and DISPLAY features and Inspect, String and Unstring Verbs):

- Low-level segmentation module, with optional Data Division allocation map and modular programming techniques.
- Full low-level library function with partial high Replacing facility.
- Conditional variables — Data Division level 88.
- Nested conditionals.
- Device assignments made at execution time.
- Source listings with imbedded diagnostics.
- Sort Utility, which accepts simple parameters as descriptions of files to process.
- Reformat Utility to convert PDP-11 terminal COBOL into conventional ANSI programs.
- COBRG, a high-level language for efficient report preparation and commercially oriented problem-solving capabilities.

The COBOL-74 System requires a PDP-11/35, 11/40, 11/45, or 11/50 CPU, 48K words of memory, printer, card reader, keyboard/display terminal, and the RSX-11M or RSX-11D operating system. The compiler itself occupies a 20K-word partition on the RSX-11M.

BASIC. PDP-11 BASIC is a superset of the Dartmouth BASIC language; Digital calls its main version BASIC Plus. BASIC Plus is implemented as a time-sharing version that operates under RSTS. Up to 32 users can run programs concurrently under RSTS/E. BASIC Plus includes the following extensions to Dartmouth BASIC:

- Extensive set of operators and functions for character string manipulation.
- An integer data type.
- Programmed format control of print files.
- Programmed error sensing and recovery.
- Access to sequential and random access disc files.
- Access to all system peripherals.
- Syntax extensions to permit more concise programs and more efficient program execution.

BASIC Plus includes 50 program statements, 34 system commands, 24 operators, 3 types of variables, 40 functions, matrix operations, and output formatting.

BASIC/RTS-11 extends Dartmouth BASIC to include optional string capability, CALL statement to interface assembly language functions, chain and overlay statements for overlaying, and support for LPS-11. BASIC/RTS-11 is a virtual memory system with up to seven sequential files and seven virtual files; it can also run in calculator mode.

Digital also offers a single-user BASIC for use on small systems.

FOCAL® Interpreter. Digital also supplies a software package to support its own FOCAL language, designed to assist scientists, engineers, and students in solving problems by direct communication with the computer. It uses a series of short, concise, easy-to-learn, English imperative statements input from a Teletype keyboard. Mathematical expressions are usually expressed in standard notation.

FOCAL is supplied in a single-user form that has the following important features:

- Device independence.
- Linkage to macro routines to establish a user library of commonly used functions.
- Use of COMMON to facilitate chaining in the same manner as with FORTRAN IV.

The FOCAL Interpreter can be used for simulating mathematical models, curve plotting, accounting functions, solving simultaneous equations in n-dimensional array form, and so forth.

Other System Software

These include loaders, text editors, object code debugging routines, I/O handlers, and math packages.

Application Packages

COMTEX-11. (Communications-Oriented Multi-Task Executive). COMTEX 11 is the major communications applications package for the PDP-11. It can run as a stand-alone package or as a job under DOS.

COMTEX-11 is an application-independent software system, designed to service communication line interfaces and terminals via reentrant subroutines. Applications for COMTEX-11 include the following: remote batch, store and forward, front-end processing, satellite processing, data concentrating, message switching, and telemetry processing.

Three basic program modules implement COMTEX-11:

- System Control Interface Package (SCIP) — provides the executive functions of intertask word queuing, multipriority task scheduling, and system time controls; includes an EMT (Emulator Trap) Command Interpreter to interface a user program to COMTEX-11.

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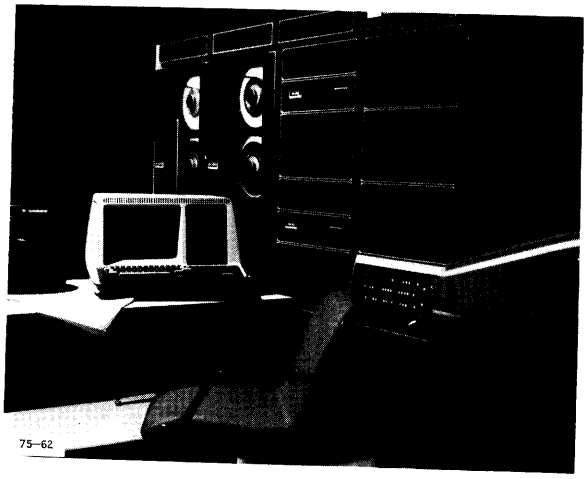
- Interrupt Service Routines (ISRs) — program modules that provide software support for all PDP-11 communication line controllers; program modules are independent of the type of remote terminal or application; modules interface only to SCIP.
- Terminal Applications Packages (TAPs) — program modules dependent only on the particular type of terminal supported; modules interface solely to SCIP.

Users develop programs via commands, which interface to COMTEX-11 through the PDP-11 Emulator Trap instruction. This instruction includes 256 operating codes, 16 of which are reserved for communication command expansion. The system is modular. New TAP and ISR routines can be added to the system as new line controller and terminal devices are developed.

WISE. The Wheaton Information System for Education (WISE) was developed at Wheaton College and was refined and tested by Digital. It provides generalized data base management functions and specific applications programs for colleges/universities. It includes programs to handle student records, alumni information, admissions information, course registration, grade reporting, grade transcripts, analysis of student characteristics, and analyses of alumni donation patterns.

WISE runs under RSTS/E and many of its programs can run simultaneously with student jobs.

DIGITAL EQUIPMENT CORPORATION
PDP-11/70 System



OVERVIEW

The PDP-11/70 is a PDP-11/45 processor with its I/O structure reorganized to triple overall throughput for a configuration with many peripherals. The PDP-11/70 does not depend on the UNIBUS as the only communication path among components. Instead, a bipolar cache memory (200-nanosecond cycle time) of 1,024 bytes is interposed between memory and other system units. Memory communicates with cache via an internal 32-bit-wide bus. The central processor and UNIBUS connect to cache via a 16-bit-wide data path while four high-speed data controllers connect to cache via a 32-bit-wide data path.

The PDP-11/70 is completely compatible with the rest of the PDP-11 line. The central processor generates 16-bit addresses, while the UNIBUS can carry 18-bit addresses the same as other PDP-11s.

The high-speed device controllers on the PDP-11/70 include a 32-bit-wide buffer. Data is transferred between the controller and its associated device as two 16-bit words and between the controller and cache as a 32-bit word. The buffers are used to assemble two 16-bit words into one 32-bit word and to disassemble the 32-bit word into two 16-bit words. Slow-speed peripherals interface to the UNIBUS.

Cache memory consists of up to 2,048 bytes or 256 32-bit doublewords. When memory is addressed, the address is first checked to determine if the content of the addressed location is in cache. If it is not in cache, memory is accessed and 32 bits (4 bytes) are transferred to cache. Most instructions and operands are only 16 bits long. Thus, the additional operand or instruction is stored in cache for a lookahead feature. Data remains in cache until it is replaced by more recently accessed data, and this provides a lookback feature. According to tests performed by Digital, the hit rate for finding an addressed word in cache is 90 to 95 percent for most applications.

Memory for the 11/70 is the same core memory as that used for the rest of the PDP-11 line; cycle time is 950 nanoseconds per 16-bit word. Two 32K-word modules are tied together to operate in tandem so that when a location is accessed, both modules read out simultaneously. All 32 bits are stored in cache, but only 16 bits at a time are transferred to the processor or the UNIBUS. With the 90 to 95 percent hit rate for cache, the effective memory cycle time is about 400 nanoseconds per 16-bit word.

All of the PDP-11/45 software will run on the PDP-11/70. In addition, a new multiuser, multilanguage, multifunction operating system called the Interactive Application System (IAS) is scheduled for delivery in November 1975. IAS is currently operating at two or three sites. It will handle multilanguage time sharing and batch processing concurrently with limited real-time processing.

The PDP-11/70 RSTS/E (Resources Timesharing System/Extended) supports 63 users employing the extended BASIC Interpreter in the foreground with an ANSI 74 COBOL-11 program in the background.

The RSX-11D operating system is available for dedicated real-time systems. RSX-11D supports FORTRAN IV and FORTRAN IV PLUS, an optimizing compiler.

The PDP-11/70 supports all the peripherals available for the PDP-11 line, including 1.2-million-byte fixed-head discs and 88-million-byte disc pack drives.

Digital expects to market the PDP-11/70 to all of its usual markets for Industrial, Business, Communications, OEM, Laboratory, Education, Computation, and Typesetting applications. Digital spokesmen indicated they expect the PDP-11/70 to outsell the PDP-11/45. To date, over 2,000 PDP-11/45 systems have been sold.

Cost of a PDP-11/70 system ranges from about $72,000 to $200,000.

COMPETITIVE POSITION

The PDP-11/70 was long overdue. Reports from the field for the past two years indicated the traffic over the UNIBUS kept throughput down on configurations with substantial I/O requirements. Competitors consistently claimed to outbenchmark the 11/45 in real-time environments. Digital offered dual-ported solid state memory with a second internal bus to the CPU on the 11/45. The second port could support a second UNIBUS for multiprocessor configurations, but generally it was connected to the system UNIBUS. Solid state memory was restricted to 32K words, thus throughput was increased only for programs executed from solid-state memory.

The PDP-11/70 removes traffic from the UNIBUS in two ways:

- High-speed devices bypass the UNIBUS except to exchange control and status information and transfer data to memory via cache and a 32-bit-wide data path.
- Transfers between memory and cache are over an internal 32-bit-wide data path.

The PDP-11/70 overlaps the low end of Digital's PDP-10 line, notably the older KA10 processor, which has not been actively marketed for two years. Digital recently upgraded the PDP-10 with the KL10 processor, which is several times as powerful as the older KA10. When asked if Digital plans to provide a bridge between the PDP-11 line and the PDP-10 line, Andrew C. Knowles, Vice President Digital Components Group, indicated such a bridge is at least two years away. One stumbling block is the PDP-10's 36-bit word, which is difficult to match with the PDP-11's 16-bit word.

The PDP-11/70 will compete with such systems as the Data General ECLIPSE, Interdata 8/32 Megamini, MODCOMP IV, and PRIME 300. Table 1 compares some features of the PDP-11/70 with the ECLIPSE and the 8/32.

HEADQUARTERS

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Table 1. Digital PDP-11/70 Mainframe Characteristics Compared to Data General ECLIPSE and Interdata 8/32

MODELS	PDP-11/70	ECLIPSE S/100, S/200	Interdata 8/32
CENTRAL PROCESSOR			
Microprogrammed	Yes	Yes	Yes
Control Memory	ROM	ROM	ROM
No. of Registers	10 accs: 3 stack pointers; 1 P.C.; all 16-bit; all can be used as indexers	8 accs: 4 16-bit (2 also used as index regs) and 4 64-bit fl pt regs	2 stacks of 16 32-bit gen regs std; 6 more sets opt
Addressing No. of Wds			
Direct	To 64K bytes	To 64K bytes	To 1M bytes
Indirect	Single level	Multilevel	No
Indexed	Yes	Yes	Yes
Mapping	Yes, to 2M bytes	No (S/100); yes (S/200 to 256K bytes)	Yes, to 1M bytes
Instruction Set			
Implementation	Firmware	Firmware	
Types	Singleword	Single- & doubleword	Single- and double-word
Number	400 std; 46 opt	86 std; 66 opt	214
Floating Point	Hardware option	Hardware option	Hardware option
Hardware Stack	Yes	Yes	
Instruction Execution Times (μsec)			
Fixed Point			
Add	3.1	0.6	1.1
Multiply	5.3	7.2	5.6
Divide	9.9	9.6	5.7
Floating-Point[2]			
Add	9.9	2.4	2.0
Multiply	11.9	3.9	3.2
Divide	12.9	4.6	5.0
Writable Control Store (256 56-bit words)	No	Opt; not software supported	No
Interrupts			
Levels	4 lines, 8 levels	16 ext	1,024
Type	Hardware	Hardware	Hardware
MAIN STORAGE			
Type	Bipolar (cache); core (main memory)	MOS; core	Core
Cycle Time* (μsec)	0.24 (bipolar); 1.0 (core)	0.8 (core); 0.7 (MOS); 0.2 (cache)	0.750
Basic Addressable Unit	Wd, byte	Wd, byte	Wd, halfword, byte
Bytes/Access	4	2	4
Cache Memory	Bipolar, 2,048 bytes	Bipolar, 32 bytes on MOS memory only	Bipolar, 16 bytes
Capacity (bytes)			
Min	64K	16K (S/100); 32K (S/200)	131,072
Max	2M	64K (S/100); 256K (S/200)	1,048,576
Increment Size (bytes)	64K	16K	128K
Ports/Module	1	1	1
Error Checks	Parity	ERCC opt	Parity
Memory Protection	Yes; memory management and 3 operating modes	No (S/100); opt (S/200); dual user memory maps, 1 data channel map	Yes, with memory management

Table 1. (Contd.)

MODELS	PDP-11/70	ECLIPSE S/100, S/200	Interdata 8/32
Overflow Entry			
Memory Management	Yes	No (S/100); yes (S/200)	Yes
Interleaving	Yes, 2-way	Core; 8-way; MOS 4-way	4-way
INPUT/OUTPUT			
Max Devices Addressable	No limit	59	1,024
Programmed I/O	Yes (UNIBUS)	Yes	Yes
DMA	Std (UNIBUS); plus high-speed data channel(1)	Std	Std for 112 devices
DMA Transfer Rate	4M bytes/sec (UNIBUS); 5.8M bytes/sec (data channel)	1,250K wds/sec	6M bytes/sec
Price for System with 128K-byte Memory	$54,600	$32,500	$49,900

Notes:

*Effective memory cycle time varies with type of memory and number of memory modules interleaved.

(1) UNIBUS is 16 bits wide; high-speed data channel is 32 bits wide.
(2) PDP-11/70 times include operand load times. Also floating point processor operates in parallel with central processor.

PRICE DATA

Model Number	Description	Purchase $
	Processors and Working Storage	
	All PDP-11/70 systems include: 11/70 central processor with memory management; 2K-byte parity bipolar cache memory with 1 byte = 8 data bits + 1 parity bit; 128K-byte parity core memory; bootstrap/diagnostic loader; line frequency clock; DECwriter II console terminal; terminal control; 2 cabinets for central processor and core memory; prewired space within the CPU chassis for mounted options	
11/70-EA/ ED*	PDP-11/70 with cartridge disc and control; cartridge disc; and expansion mounting chassis	72,650
11/70-FA/ FD*	PDP-11/70 with disc pack and control and magnetic tape and control	105,100
11/70-FE/ FJ*	PDP-11/70 system with dual access disc pack and 2 11/70 control units; magnetic tape and control	117,100
11/70-FK/ FN*	PDP-11/70 system with dual access disc pack with 11/70 control and general 11 control; magnetic tape control	117,100
11/70-GA/ GD*	PDP-11/70 system with cartridge disc and control; cartridge disc; fixed-head disc and control; magnetic tape and control; and expansion mounting chassis	109,350
11/70-HA/ HD*	PDP-11/70 with disc pack and control; fixed-head-disc and control; and magnetic tape and control	126,300
11/70-HE/ HJ*	PDP-11/70 with dual access disc and 2 11/70 control units; fixed-head disc and control; magnetic tape and control	138,300
11/70-HK/ HN*	PDP-11/70 with dual access disc pack with 11/70 control and general 11 control; fixed-head disc and control; and magnetic tape and control	138,300
11/77-FE/ FJ*	Dual processor PDP-11/70 with 2 magnetic tapes and control and dual access disc pack with 2 control units	187,200
FP11-B	Floating-point processor	5,600
	Memory	
MJ11-AC/ AD*	256K-byte parity core memory (includes cabinet, power supplies, and control)	33,000
MJ11-AG/ AH*	256K-byte parity core memory expansion frame (includes power supply and control)	31,000
MJ11-AA/ AB*	64K-byte parity core memory unit; expandable to a total of 256K bytes	13,500
MJ11-AE	64K-byte parity expander core memory	7,100
	Mass Storage	
	Discs	
RWP04-AA/AB*	88M-byte disc pack drive and control unit	35,000
RWP04-BA/BB* CA/CB	88M-byte disc pack drive (with dual access) and 2 control units	47,000
RP04-AA/ AB*	88M-byte disc pack drive (1.25-μsec/byte transfer time; 8.3-msec average access time)	25,900
RP04-BA/ BB*	88M-byte disc pack drive (with dual access; 1.25-μsec/byte transfer time; 8.3-msec average access time)	30,800
RWS03-BA/ BD*	512-byte fixed-head disc drive and control unit	14,900
RWS04-BA/ BD*	1M-byte fixed-head disc drive and control unit	21,200
RS03-AA	512K-byte fixed-head disc drive (2-μsec/ byte transfer time; 8.5-msec average access time)	9,500
RS03-AD		
	Input/Output	
	Magnetic Tape	
TWU16-EA/ED*	Program selectable 1,600/800 bpi magnetic tape transport and control unit	15,500
TWU16-EK/EN*	800-bpi magnetic tape transport and control unit	14,450
TU16-EE/ EJ*	Magnetic tape transport (45 in./sec; 9 tracks; industry-compatible)	8,950
	Software	
	Available on Magtape or DECpack	
QP210-AD/ AE/AF/AP	IAS (Interactive Application System)	7,800**
QP240-AD/ AE/AF/AP	BASIC (timeshares BASIC as an incremental compiler and compatible with the PDP-11 BASIC language processors for BASIC/PTS, BASIC/CAPS, and BASIC/RT-11)	500**
QP230-AD/ AE/AF/AP	FORTRAN IV	700**
QP010-AD/ AE/AF/AP	COBOL-11	7,000**

Notes:

*Indicates 230 VAC, 50-cycle power. First number is 115 VAC, 60-cycle power.

**License fee.

DIGITAL EQUIPMENT

PDP-15 System Report

75–15

OVERVIEW

The Digital Equipment PDP-15 is an 18-bit minicomputer system aimed at the midicomputer market and designed for laboratory, control, scientific, and mathematical applications that can benefit from the larger memory and greater arithmetic precision of the longer 18-bit word.

The system, which has been on the market since 1970, has acquired a very respectable body of software. Operating systems include scientific, FORTRAN-oriented DOS-15 and BUS-15 systems, ADvanced Software System (ADSS), and RSX PLUS III. The last is a new foreground/background real-time multiprogramming system supplanting earlier RSX-15 and RSX-PLUS systems. If systems are small, they can also run under a basic monitor and use a stand-alone assembler. Special operating systems are provided for applications like data management (MUMPS) and graphics (GRAPHICS 76). A new subscription service and software updating add to the software support.

All systems use the same central processor, and all are field expandable. Floating-point hardware, power failure protection, and memory parity are among the mainframe options. Features such as the extended arithmetic element, automatic priority interrupt, memory protect, memory relocate, and the real-time clock are either standard or optional depending on the configuration.

Main storage is a core memory that ranges in size from 4K to 132K words. The PDP-15/10, 20, 30, 35, 40, and 50 all use the MM15 and MK15 core memory, which has an 800-nanosecond cycle time. Since these systems are now considered traditional (nonstandard) products, they are available only on special order.

The PDP-15/76 Series uses the ME15 core memory, which has a 980-nanosecond cycle time and is available in 8K- and 16K-word modules. The newest family members are the PDP-15/78 and PDP-15/76C systems, which use the LA36 DECwriter II as the system console.

A memory multiplexer permits multiprocessing. The PDP-15 can support four multiplexers to permit a variety of memory and processor configurations. Several hardware/software system combinations provide for multiprogramming. Multiprocessing is not software supported except on the PDP-15/76, where the PDP-11/05 is supported as a peripheral processor (via Unichannel 15) by DOS-15, BOSS-15, and RSX PLUS III.

A number of applications packages are included in the software. There are electrocardiography (ECG-1500) packages for the medical field. Several interactive graphics packages (ARK-2) are for architectural project design and management and electronic circuit layout. Others cover such subjects as pulse height analysis (PHA-15) and spectral analysis (GASPAN) for the scientific community.

Digital also provides STATPAC (an open-ended package of statistical programs for the user with limited computer knowledge), SCOLDS (Spark Chamber On-Line Data System), two hybrid software systems, CSMP-15 (Continuous System Modeling Program), Lab RSX-15, GRASP-15 (Generalized Remote Acquisition and Sensor Processing), and REDAC (Real-Time Data Acquisition for electronic design tasks).

Competitive Position

The PDP-15 has been a strong competitor for applications in the midicomputer range. It is cheaper than comparable configurations of large computer systems, and it is more powerful than most top-of-the-line minicomputers. Memory capacity can range from 4K to 132K 18-bit words.

There has been a growing trend among minicomputer manufacturers to expand the capabilities of their major minicomputer lines through memory mapping options and various other stratagems in order to compete at the midicomputer level. Digital itself has done this with the PDP-11/45, while Data General, General Automation, Hewlett-Packard, and Interdata have all developed memory mapped systems and multiprogramming operating systems that can compete in the midicomputer range. Thus, the PDP-15 is going to find an increasingly competitive atmosphere in this sector of its market, particularly from recent systems taking advantage of new lower-cost MSI and LSI technologies to achieve lower prices.

One advantage of the PDP-15 over many competing products is its modular packaging into systems designed for specific markets. Users can add options, peripherals, and software in the field to expand these systems when needs change. This modular arrangement provides maximum performance from an optimum configuration since a user buys only the configuration he needs knowing the system can grow to meet future requirements.

A second advantage of the PDP-15 over competing minicomputer systems is the numeric precision of the

18-bit word over the 16-bit word. Floating-point (real) numbers can be represented in the PDP-15 with a 17-bit exponent and a 35-bit fraction (equal to 10 decimal digits).

Another competitive advantage is the amount of available interface equipment so that almost any laboratory or industrial customer can fit the PDP-15 to his needs using Digital hardware. If a customer requires special interfacing, Digital will usually make it to order.

A fourth advantage of the PDP-15 is its extensive software support.

Prime competitors to the PDP-15 are the new Data General Eclipse, Interdata 8/32, Prime 300, HP 21MX, Xerox 550, SEL System 80, Modular Computer Systems MODCOMP IV, IBM System 360/44, and Digital's own PDP-11/45. The Hewlett-Packard HP 3000 and Varian V70 will also be competing with the PDP-15 for some applications.

Although the PDP-15 architecture has changed little from that of the PDP-7 and 9 (now traditional products), Digital has enhanced the system consistently, providing up to 132K words of memory, floating-point processor, mass storage, many peripherals, and software. The PDP-15/70 Series, for example, uses the ME15 memory, which is considerably cheaper than the older MM15 memory. Use of a PDP-11/05 as a peripheral processor with the PDP-15/76 makes the PDP-11 peripherals available.

Digital as a company is responsive to user needs and supports DECUS (Digital Users Society), an active, outspoken users group.

Users we contacted bought the PDP-15 for a variety of applications. An air force base used one in a complex telemetry processing system that was a satellite to a CDC 6600. A medical school had developed an on-line EKG interpretation facility using a PDP-15 with 28K words of memory and 2 fixed-head discs. Users felt the system was very reliable; both hardware and software have lived up to expectations. The medical school spokesman noted that in today's market, a PDP-11/40 would probably satisfy their requirements and be less expensive.

Configuration Guide

Each PDP-15 standard model includes a central processor, core memory, and its own complement of features and peripheral devices to configure it for an application. Features and devices offered are common to all the family. Table 1 lists the standard models and their system components. Table 2 lists general system specifications.

Peripherals include a line of display and graphics equipment in addition to the more usual console typewriters, paper tape and punched card units, line printers, magnetic tape units, and disc memories. Process control devices and analog/digital equipment are also offered. Data communications equipment includes both controllers and terminals. The PDP-15/76 uses a PDP-11/05 as a peripheral processor to support the RK11E/RK05 Disk Cartridge System. Peripherals are listed in Table 3.

Table 1. Digital PDP-15: System Configuration Summary

CENTRAL PROCESSOR	
Type	Hardwired
No. of Internal Registers	1 GP, 1 index
Addressing	
Direct (no. of wds)	4,096
Indirect	1 level
Indexed	Yes
Instruction Set	
Implementation	Hardware
Number	65-222
Floating-Point Arithmetic	Optional hardware
Decimal Arithmetic	No
Priority Interrupt Levels	8 levels, 32 sublevels
MAIN STORAGE	
Type	Core
Cycle Time (μ sec)	980
Basic Addressable Unit	18-bit word
Bytes per Access	2
Cache Memory	No
Capacity (bytes)	8K-256K
Increment Sizes (bytes)	8K/16K
Ports Per Module	1
Error Checks	Parity; opt
Protection	Yes; opt
Memory Management	No
ROM	No
INPUT/OUTPUT	
I/O Channels	
Programmed I/O	Yes
DMA	Yes
Multiplexed I/O	No
Max DMA Transfer Rate	1M wds/sec

Operating systems and similar system control packages differ widely in the configurations they require. Table 4 summarizes the major system packages and indicates the minimum configuration needed for each.

Compatibility

The PDP-15 is upward-compatible with the older PDP-9, PDP-7, and PDP-4, but not the PDP-1. PDP-9 is a direct descendant of the PDP-7 and the PDP-4, and has an identical instruction repertoire but with expanded capabilities.

The instruction repertoire of the PDP-15 is even more extensive than that of the PDP-9. Twelve additional instructions are provided to clear, load, store, and increment the index register. Moreover, there are optional floating-point instructions.

Compatibility among programs written for the PDP-9 and PDP-15 varies with the programming language used. FORTRAN-coded programs are compatible because the software accommodates the hardware differences. Assembly language programs are restricted to the instruction subset and the addressing capability common to both the PDP-9 and the PDP-15.

Table 2. Digital PDP-15: Mainframe Specifications

Model No.	Description
Discs	
RF15/RS09	Up to 8 RS09 drives per RF15, 256K wds per drive; 15M-, 31M-, or 62M-wd/sec transfer
RP15/RP02	Up to 8 RP02 drives per RP15, 10M wds per drive; 135K-wd/sec transfer
RK15 Subsystem	RK11 control/RK05 DECpack System, 1.2M words per cartridge, 70-msec avg. access
Magnetic Tape	
TC59P/TU10	4 TU10 transports per TC59; TU10 is 7-trk or 9-trk, 800/556/800 bpi, 45 ips
TC15/TU56	DECtape control and dual DECtape transport, block addressable
Card	
CR15 Series	200-, 300-, or 1,000-cpm readers
Paper Tape	
PC15	200-char/sec reader; 50-char/sec punch
Printers	
LP15 Series	356-1,110 lpm or 253-843 lpm; 80 or 132 col; 64 or 96 char sets
Plotters	
XY15 Series	Calcomp 563 and 565 Drum Plotters; 12-inches and 31 inches, respectively
Displays/Graphics	
VP15 Series	Control & display, 5″ and 7 x 9″ models, BW or 2-color; 10-bit data word per direction; 1 part in 1,024 resolution
VR01	5″ diameter P7 phosphor oscilloscope
VR14	Oscilloscope 5 x 7″ P31 phosphor oscilloscope
VR20	Two-color x-y oscilloscope 7 x 9″
VT15 Series	Graphic-terminal, 17″ diagonal or 21″ diagonal
VT04	Display consoles, 17″ diagonal VT 15 Graphic Processor
VT07	Like VT04 but 21″
VL04/VL07	Light pens for VT04/VT07
VW01	Writing tablet & spark pen
Communications	
Teletypes	ASR 33, KSR 33, ASR 35, KSR 35
LA 30	DECwriter terminals; 110, 150, 300 baud
VT05	A/N video display terminal; 20 lines, 72 char
Analog/Digital	
AFC-15	Analog input subsystem; up to 192 input channels
UDC 15	Digital I/O; for up to 384 points
BD15	Control unit for up to 11 AFC15s and 11 UDC 15s; 2,048 analog inputs; 4,096 digital points
Laboratory	
NP15	Nuclear physics assembly
CA15-A	CAMAC interface for up to 7 CAMAC crates
AD15	A/D medium-speed subsystem; up to 128 channels
ADF15	A/D high-speed subsystem; up to 36 channels
AA15	D/A subsystem; up to 16 channels
AF04	Digital voltmeter; analog input for 10-1,000 differential inputs

Table 3. Digital PDP-15: Peripherals

Package	Description
Basic Monitor	For minimum 8K-word system with paper tape I/O, Teletype
Advanced Monitor	Like basic monitor but can dynamically alter I/O assignments; supports FORTRAN, FOCAL; requires 12K words
Background/ Foreground Monitor	Extension of Advanced Monitor to allow foreground/background multiprogramming
MUMPS-15	Massachusetts General Hospital Utility Multiprogramming System; compact systems using JOSS high-level language
DOS-15	Disk Operating System for batch systems; requires 16K words of core, DECwriter, paper tape I/O, clock, magtape, disc
BOSS-15	Batch Operating System; superset of DOS-15 using card reader, line printer
RSX PLUS III	Real-time foreground/background multiprocessing system; requires 32K words of core, 0.5M words of disc storage, terminal, memory relocation hardware, paper tape, magtape or DECtape, real-time clock
ALGOL	ALGOL 60 ECMA Level 1; some restrictions
FORTRAN IV	Core-based and disc-based versions; some exceptions from ASA x3.9-1966
FOCAL	DEC's desk calculator language, single user or multiuser
COMPACT	Absolute assembler; needs less than 3K words of core
MACRO-15	Macro Assembler
Utilities	Dynamic Debugging Technique (DDT), 8-15 Translator (ITRAN), System Generator, Copy, Dump, Library Update, System Patch, Editors, Peripheral Interchange, Linking Loader, Math Library, Magtape Dump, I/O Handlers
Applications Packages	Pulse Height Analysis, Gamma Spectral Analysis (GASPAN), Spark Chamber On-Line Data System (SCOLDS) for data acquisition, Continuous Systems Modeling Program (CSMP-15), STATPAC statistical programs, VT15 Graphics, Lab RSX-15, REDAC for electrical design tasks, ECG-1500 for electrocardiograms, ARK-2 for interactive graphics

Within the PDP-15 family, programs used on smaller systems will work on the larger systems without modification, but they generally will not use the full capability of the larger system.

MAINTENANCE AND SUPPORT

As the largest of the minicomputer manufacturers, Digital has one of the largest sales and service networks (not including the large computer companies) both in the

Table 4. Digital PDP-15: System Software Packages

PDP-15 Model	15/76-CE/F	15/76-CK/L	15/76-CP/R	15/76-CS/T	15/78-AA/B	15/78-BA/B
KP15 Central Processor	X	X	X	X	X	X
Core Memory	ME15	ME15	ME15	ME15	ME15	ME15
Model	32K	32K	32K	32K	24K	24K
Size (words)	X	X	X	X	X	X
KE15 Extended Arithmetic Element						
FP15 Floating-Point Processor						
KT15 Memory Relocate						
KA15 Automatic Priority Interrupt						
KM15 Memory Protect						
KW15 Real-Time Clock	X	X	X	X	X	X
DW15-A I/O Bus Converter			X	X		
Teletypewriter						
ASR 33						
KSR 33						
KSR 35						
LT15 Single Teletype Control						
LA36 DECwriter II	X	X	X	X	X	X
PC15 Paper Tape Reader & Punch	X	X	X	X	X	X
TC59-D Magnetic Tape Control			X	X		
TU10 Magnetic Tape Transport			X	X		
TC15 DECtape Control	X	X				X
TU56 Dual DECtape Transport	X	X				X
RF15 DECdisk Control						
RS09 DECdisk Drive						
RP15 Disk Pack Control						
RP02 Disk Pack Drive						
RK15 Cartridge Disk System	X	X	X	X		
Disk Package with UNICHANNEL-15	X	X	X	X		
UC15 Peripheral Processor (PDP-11/10)	X	X	X	X		
Core Memory						
Model	MM11-K	MM11-L	MM11-K	MM11-L		
Size (words)	8K	12K	8K	12K		
RK11E DECpack Control	X	X	X	X		
RK05 DECpack Cartridge	X	X	X	X		

United States and worldwide, numbering more than 2,100 engineers at over 200 service locations. Although minicomputer manufacturers have traditionally aimed at somewhat "self-sufficient" users, those who need considerably less software support and applications programming assistance than are provided by the large computer manufacturers, this picture is changing, as evidenced by Digital's recently added software support services.

Standard maintenance contracts provide for on-site preventive and emergency maintenance for 8-, 12-, or 16-hour periods. An on-site engineer can also be hired if requirements are critical; on the other hand, a user can choose to buy service on an individual call basis or to set up his own maintenance staff.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	SYSTEMS*		
PDP-15/76	Spooled Batch System	91,260	
PSX Plus III	Resource Sharing System	93,705	
PDP-15/76	Graphics Computer Aided Design System	121,020	
	Architectural Graphics System	111,845	
Graphic 76/ REDAC	Printed Circuit Layout Graphics System	104,770	
Mumps-15	Data Base Management System includes;	115,415	
	CENTRAL PROCESSOR AND WORKING STORAGE		
PDP-15/76-CE/CF	KP15 Central Processor (includes 32K Wds Core Memory; DECwriter II; High-speed Paper Tape Reader and Punch; Extended Arithmetic Element; Real-time Clock; TC15 DECtape Control; Dual DECtape Transport; Cartridge Disk System with UNICHANNEL-15; Peripheral Processor and 8K Core Memory)	68,500	634
PDP-15/76 CK/CL	Same as 15/76-CE/CF Model except peripheral processor has 12K-wd memory	71,200	655
PDP-15/76 CP/CR	Same as 15/76CE/CF Model except TC59-D Magtape control and TU10 Magtape transport used instead of TC15/TU56 DECtape system and DW15-A I/O Bus Converter added	75,000	687
PDP-15/76 CS/CT	Same as 15/76-CP/CR Model except peripheral processor has 12K-wd memory	77,700	708
PDP-15/78 AA/AB	KP Central Processor (including 24K Wds Core Memory; DECwriter II; High-speed Paper Tape Reader and Punch; Extended Arithmetic Element; Real-time Clock;	35,000	318
PDP-15/78 BA/BB	Same as 15/78-AA/AB except with TC15/TU56 Dual DECtape transport added	44,000	371
	Peripheral Processors and memory		
UC15-HE/HF	Peripheral Processor includes a PDP-11/10 in 10½ in. enclosure, 8K MM11 core memory, MX15-B memory mplxr, and interprocessor interrupt link	15,000	154
UC15-HK/HL	Peripheral Processor (Same as UC15-HE/HF except that PDP-11/10 contains 12K-wd memory)	17,700	175
MM11-K	4K wds of PDP-11core memory	2,700	21
MM11-F	4K wds of PDP-11core memory	3,780	27
	Processor Options		
KE15	Extended Arithmetic Element	2,800	27
KA15	Automatic Priority Interrupt	2,000	21
KM15	Memory Protect	1,000	15
KT15	Memory Relocation	2,000	32
KS15	Memory Management/Automatic Priority Interrupt Package	5,000	75
KF15	Power Fail	1,000	3
FP15	Floating Point Processor	9,750	80
KW15	Real-time Clock (Line frequency)	500	3
DW15-A	I/O Bus Converter	2,160	21
BA15	Control for LT15-A, PC15, and VP15 options	NC	10
BB15	Processor Expander Panel	1,500	11
	Memory Options		
	ME15 Core Memory (18-bit wds; 980 nsec)		
ME15-AA/AB	8K Memory	6,000	42
ME15-B/C/D	8K Expansion Element	6,000	42
ME15-E/F/ H/J	16K Memory	9,800	85
	MASS STORAGE		
	Discs		
RF15	DECdisk Control (for up to 8 RS09 DECdisks)	6,000	37
RS09/RS09-A	DECdisk Unit	9,000	48
RP152-A/B	Disk Pack Drive Unit and Control	27,000	207
RP02-AS/ RP02-BS	Disk Pack Drive Unit (10.2M wds/unit)	15,000	133
RP153-A/ RP153-B	Disk Pack Drive Unit and Control	32,000	233
RP03-AS/ RP03-BS	Disk Pack Drive Unit (20M wds/unit)	20,000	159
RP02-P	Spare Disk Pack for RP02 or RP03	295	–
RK15-HE/ RK15-HF	Cartridge Disk System (Includes UC15 HE/HF peripheral processor)	20,600	260
RK15-HK/ RK15-HL	Cartridge Disk System (Includes UC15 HK/HL peripheral processor)	23,300	281
RK05-AA/ RK05-BB	DECpack System (1.2M words; DECpack drive and removable disc cartridge)	5,100	60
RK03-KA	Spare Cartridge	99	N/A
	INPUT-OUTPUT		
CR15-FA/ CR15-FB	Card Reader and Control (300 cpm)	5,400	80
CR15-DA/ CR15-DB	Card Reader and Control (1000 cpm)	10,800	80
CR11/CR11-A	Card Reader and Control (300 cpm)	4,860	53
PC15/PC15-A	Paper Tape Reader/Punch	4,210	38
LP15-VA/ LP15-VD	Line Printer and Control (300-lpm)	11,500	82
LP15-WA/ LP15-WD	LP15-VA ILP15VD with 96 char set	13,500	82
LP15-RA/ LP15-RB	Line Printer and Control (1200-lpm)	40,000	154
LP11-VA/ LP11-VD	Line Printer and Control (300-lpm)	9,900	72
LP11-WA/ LP11-WD	Line Printer and Control (300-lpm)	11,900	72
LS11-A/ LS11-B	Line Printer and Control (60-lpm)	5,615	58
LV11-BA/ LV11-BB	Electrostatic Printer/Plotter (500-lpm)	11,770	53
TC15	DECtape Control	5,400	27
TU56	Dual DECtape Transport	4,700	32
TC59-D	Transport Control	6,950	37
TU10-FE/EE	Transport (7/9-track; 45 ips; requires TC59D)	7,505	74
LA36-CA/CB	DECwriter II Keyboard Printer	1,850	25
XY15-AA/BB	Plotter and Control (Tabletop Model 565)	9,610	32
XY15-BA/BB	Plotter and Control (Tabletop Model 563)	14,470	37
XY11	Incremental Plotter Control	1,300	5
CalComp-563	200 and 300 steps/sec	10,150	35
CalComp-565	300 steps/sec	5,830	35
Complot DP-1	300 steps/sec	6,050	35
Complot DP-10	300 steps/sec	3,445	35
XY311	Plotter and Control (1800 steps/sec)	18,900	75
VT05B-AA/ AD	A/N Display HDX/FDX (20 lines by 72 chars; up to 2,400 baud)	2,795	23
VT50-AA/AB	A/N Display FXD or FDX with local echo; 12-line by 80-char format; 64 ASCII chars; rates to 9,600 baud std)	1,250	22
VP15-A	Storage Tube Display and Control	6,260	91
VP15-B	Oscilloscope and Control	3,885	32
VP15-BL	VP15-B with Light Pen	5,640	37
VP15-C	Oscilloscope and Control (7 x 9-in. VR14 X-Y display with 10-bit data word per direction.)	6,260	47
VP15-CL	VP15-C with Light Pen	8,015	52
VR01-A	Oscilloscope (5-in. diameter screen)	1,080	15
VR14	Oscilloscope (7 x 9-in. screen)	3,240	19
VT01-A	Storage Tube Display (table mounted)	3,240	80
GT15-SA/SB	Graphic System	24,000	146
GT15-LA/LB	Graphic System Same	29,000	173
VT04-A	Graphic Display Console (CRT; 6 lighted function buttons) VT15	4,860	27
VT04-B			
VT07-A/B	Graphic Display Console	10,800	53
VV15-A	Arbitrary Vector Generator	5,000	21
VV15-K	VV15 Upgrade Kit (to VV15-A)	1,500	–
VM15-A	Display Mplxr (for up to 4-VT04's/VT07's)	5,000	21
LK35	Keyboard (for VT04)	1,295	32
LK37	Keyboard (for use with VT07 console)	1,295	32
VL04	Light Pen (for VT04)	755	7
VL07	Light Pen (for VT07)	755	7
VW01-BP	Writing Tablet and Control	3,780	32
VW01-MX	Writing Tablet Mplxr (for up to 4 VW01-MA writing tablets)	1,080	5
VW01-MA	Writing Tablet and Spark Pen	2,160	11
VW01-SP	Spark Pen	215	5
VW01-WT	Writing Tablet	860	11
	DATA COMMUNICATIONS		
LT19-D	Multi-station Terminal Control	1,940	11
LT19-E	Terminal Line Unit	864	3
LT19-F	EIA Line Adapter	108	3
LT19-H	Cable Set Connects and LT19-F to another LT19-F for interprocessor communication.		
	LT19-HA 50 ft	64	–
	LT19-HB 100 ft	70	–
	LT19-HC 150 ft	75	–
	LT19-HD 200 ft	81	–
	LT19-HE 250 ft	86	–
LT15-A	Single Terminal Interface	500	3
DC01-ED	Multi-station Terminal Control	6,480	21
DP11-DA	Full/Half Duplex Sync Line Module Set and System Unit	1,700	19
KG11-A	Communications Arithmetic Unit	900	6

*All systems include Installation plus 90 days free parts and service; 90 days SPR service for software at no charge, and 6 weeks training.

HEADQUARTERS

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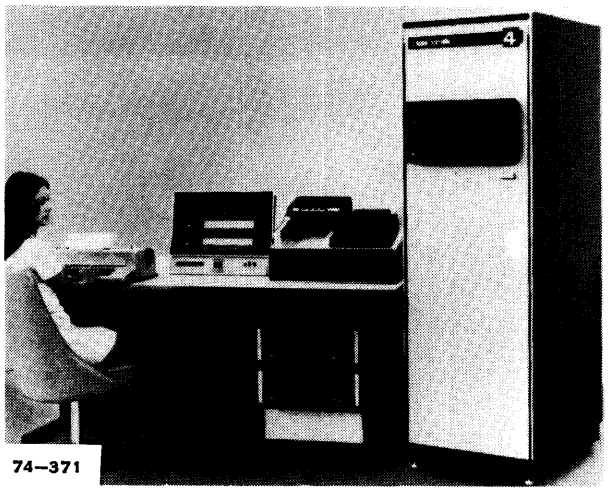
DIGITAL SCIENTIFIC

META 4 System Report



OVERVIEW

The Digital Scientific META® 4 system is a microprogrammed 16-bit minicomputer aimed at the same markets as IBM's 1130 and 1800 systems. The 4030 and the 4040 models provide complete emulation of IBM's 1130 and 1800 systems, respectively. Faster memory cycle time, faster command execution, higher-performance peripheral subsystems, and microprogrammability combined with lower prices for comparable configurations give the META 4 systems considerably better price/performance ratios than IBM equivalents. All IBM features and comparable peripheral subsystems are available to provide complete compatibility for 1130 and 1800 programs, to the extent that IBM diagnostics can run on a Digital Scientific Computer (DSC) system. Digital Scientific supplies software support for microprogramming and a set of system utilities to operate unique DSC peripherals. Operating systems and all other systems and applications software can be obtained from IBM.

Digital Scientific was started in 1967 as a customized systems house. The META 4 was introduced in 1970 as its only "standardized" product. Although the META 4 processor has been used for other types of applications, emulation of the 1130 and 1800 has continued to be the main marketing focus for the product line.

Digital Scientific has sales and service offices in New York City, Washington (DC), Detroit, Chicago, Dallas, and Los Angeles, with additional service offices in San Francisco, Phoenix, Tucson, Houston, Minneapolis, New Orleans, Pittsburgh, Philadelphia, Baltimore, Flint (MI), Danbury (CT), Clarkesburg (NJ), and Montreal (Canada). Headquarters are in San Diego. Leasing in the United States and Canada is handled by Digital Leasing Company. A distributor agreement with Mitsui and Company provides sales and service in Japan; an entry into western Europe is expected in early 1975.

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PERFORMANCE AND COMPETITIVE POSITION

Digital Scientific's main competitor in the 1130/1800 replacement market is the General Automation 18/30. The 18/30 is aimed more at 1130 replacement, because there are more 1130 than 1800 installations. IBM 1800 installations are more customized, hence more difficult to replace. General Automation, moreover, provides compatibility only at the CPU instruction level, and uses its own software to achieve comparable operating environments to some extent, but portions of user programs in some installations might have to be adapted. Also, GA does not attempt to provide any type of plug compatibility for peripheral subsystems. Digital Scientific provides compatibility for devices that attach to an IBM SAC channel and a wider range of peripherals.

For certain applications the META 4 has a significant price/performance edge even if GA's peripheral offerings meet software needs. Digital Scientific states that users have cut execution times by factors of 9, 10, and even 20 over the 1130 by using microcode, particularly for programs that use floating-point calculations. The memory cycle times for both DA and GA systems are half that for the IBM systems; consequently both cut execution times by a factor of at least two.

Other factors that increase the system performance for META 4 include overlapped cycle stealing for DMA transfers and the greater capacity of the disc subsystem, which can be expanded from 10M to 20M bytes. Table 1 compares the hardware of the DSC, GA, and IBM computers.

Digital Scientific is a smaller company than General Automation; both are about the same age. The GA system probably has a competitive advantage for small 1130 users who cannot significantly benefit from microcoding on the META 4 simply because the company is larger. In the 1800 replacement market, however, Digital Scientific is in a much stronger position vis-a-vis General Automation because their system is very similar to the IBM 1800, their microcoding capability can substantially improve performance, and they offer a full line of process I/O.

USER REACTIONS

Digital Scientific META 4 users proclaim it to be a reliable, fast, and price/performance effective system. Most users experienced no problems whatever in converting to the META 4 from their IBM 1130 and 1800 systems. One user said he was "delighted" with the ease of software conversion.

A spokesman for a civil engineering consulting firm handling highway and airport geometry as well as architectural and structural designs for schools, airports, and factories is very happy with the Model 4030. His META 4 improves on the speed and accuracy of this user's former

Table 1. Digital Scientific META 4: Mainframe Characteristics Compared to GA 18/30 and IBM 1130 and 1800

MODEL	DSC 4030	DSC 4040	GA 18/30	IBM 1130	IBM 1800
CENTRAL PROCESSOR					
Microprogrammed	Yes	Yes	No	No	No
No. of Instructions	55**	55**	32	29	31
No. of GP Registers	2*	2*	2	2	2
No. of Index Registers	3*	3*	3	3	3
Real-Time Clock	Yes	Yes	Yes	No	No
I/O					
Programmed I/O	Yes	Yes	Yes	Yes	Yes
DMA (no. of channels)	9	9	5	5	3 std, 6 opt
MEMORY					
Cycle Time (μsec)	0.90	0.90	0.96	2.2, 3.6	2.0, 4.0
Parity	Std	Std	Std	Std	Std
Protect	Std	Std	Std	None	Std
ROM (wds)	1K-4K	1K-4K	None	None	None
Core Size (wds)	8K-32K	8K-64K	32K	32K	64K
PERIPHERALS					
Max Speed for					
Card Reader (cpm)	1,000	1,000	1,000	1,000	400
Line Printer (lpm)	600	600	600	600	600
Mag Tape Drive (ips)	75	75	75	None	None
Disc Subsystem					
Capacity (wds/drive)	512K, 10M	512K	512K 2.5M, 10M	512K	512K, 2.5M
Access Time (μsec)	–	–	45	750	75

*Assigned from bank of 28 registers.
**34 standard, 16 with optional floating-point firmware.

IBM 1130 and he has had no downtime. This firm ran benchmarks written in FORTRAN using real-number arithmetic and no I/O and found the META 4 outperformed an IBM 370/135. This company had a fast 32K-word memory on the 1130, and FORTRAN programs with no I/O, ran 15 times faster on the META 4 than on the 1130. The firm wanted spooling to a card punch and a plotter. The META 4 system maintained the system cycle time, even with the spooling operations. With the flexibility shown by the META 4 system, the firm plans to add time-sharing terminals to the present 4030. The user investigated the IBM 370/125, DEC's PDP-11/45, the General Automation 18/30, and the option of enhancing the 1130. This user feels the decision to go with Digital Scientific has been a good one for the company.

A consulting firm for aerospace, government, and business agencies uses the META 4 Model 4030 for "scientific number-crunching." The system analyzes data from experimental tests and models physical processes. The META 4 is particularly effective in scientific simulation, handling numerical solutions of partial differential equations. The user looked at the General Automation 18/30, as did most of the users interviewed. This firm was primarily interested in maximum software compatibility with the 1130, which Digital Scientific assures. The user wanted the performance of a Univac 1108 or a CDC 6600 but without the expense of these large systems. The META 4, in this user's estimation, provides comparable performance, a bit slower, and certainly less expensive.

A software house specializing in IBM 1130- and 1800-compatible software uses a Model 4030 for software development and rents the machine to a service bureau for eight hours a day. This user thinks the META 4 is an excellent system, faster, and more capable than an IBM 1130. This user has had the system for over two years and has experienced no problems.

A major advertising agency uses the META 4 Model 4030 for scientific, statistical, and research processing. The firm finds the META 4 quite satisfactory for its needs and faster than the 1130. This system has been installed for over four years; the firm experienced some start-up problems but these have long since disappeared. The firm had minor mechanical problems with the first printer supplied; it was not rugged enough to withstand the beating it was given. Later printers proved more sturdy. One reason this firm chose the META 4 is its IBM-1130 compatibility. Many marketing research companies use 1130-type systems and they share programs among themselves.

Users of the META 4 Model 4040 are generally very pleased with their IBM 1800 emulators. One uses the

Model 4040 in a process control environment. It controls seven or eight laboratory stations handling tests for integrated circuits and frequency selective devices. This company had an IBM 1800 but found it was too slow and required too much space. Price and speed were the deciding factors for the META 4. This firm has recently added 40K bytes of memory and would like to add a high-speed line printer. The user has had problems with the console and systems printers, saying it was rare when both work simultaneously. He considered this a minor problem and stated he had no big problems with the system.

A scientific institute uses the META 4 as a flexible data base management and data acquisition system. This user had found the performance of the META 4 superior to that of his previous IBM 1800. Installed over two years ago, he has experienced no hardware downtime with the META 4 and no software problems. Benchmarks developed for the system ran ten times faster on META 4 than the IBM 1800. This user wanted hardware multiply and divide, which the IBM system did not have and needed to handle complex mathematical equations. The META 4 cost is half the price of the 1800.

A major automobile manufacturer uses the META 4 to test exhaust emission, engine endurance, and carburetor flow. This system was recently installed, so new acceptance tests are still being run. So far, the system is doing well aside from some initial burn-in problems, with no problems with software, previously run on an IBM 1800.

Digital Scientific's maintenance is described as good to excellent by most users; a few users are a little disappointed with response time and competency. One user was impressed with DSC's uniformly bright, knowledgeable, and experienced customer engineers. Another describes the service as competent but response time varies; it is usually within acceptable norms, however. A third user found that the customer engineers lack experience. A simple wiring error was at fault for one user's system failures and repeated visits by DSC brought no solution. This user found the error and corrected it himself.

CONFIGURATION GUIDE

The basic META 4 processor with an 8K-word memory consists of three models: the 4030 emulates the IBM 1130; the 4040 emulates the IBM 1800; and the 4031 provides for user-supplied emulation. The 4030 and 4040 differ in the standard emulation and I/O backplane controllers; thus, they support different I/O options. The Model 4030 processor options include a real-time clock, hardware (firmware), floating-point arithmetic, 1K-word (16 bits) ROM modules, and a storage access channel (SAC). Six interrupt lines, three index registers, two accumulators, and 39 instructions are standard features. The floating-point option adds 16 instructions for a total of 55.

Model 4040 includes a real-time clock and 14 interrupt levels as standard features, and, like the 4030, it provides ROM modules and floating-point arithmetic options. Nine DMA data channels are standard features; a set of five OEM channels (to attach non-IBM devices) and a selector channel are available. An I/O typer and controller can supplant the standard console.

Memory can be expanded in 8K-word increments up to 32K words on the 4030 and 64K on the 4040, but memory modules added above 32K words carry an additional field installation charge.

IBM specifies a maximum of 10 I/O devices on an 1130 and up to 12 data channels on an 1800. DS allows up to 28 devices to be attached to either system, but not all devices can go on both. Communications adapters are available for the 4030 for instance, and analog/digital I/O subsystems can be attached to the 4040.

Table 2 lists the peripherals available for the 4030 and 4040 as compared to those available for the 1130 and 1800. Digital Scientific supplies little software for the META 4 because the system is designed to run the software available for the 1130 and 1800. Only the software listed in Table 3 is available.

Table 2. Digital Scientific: META 4: 4030 and 4040 Peripherals

Device	DSC 4030	IBM 1130	DSC 4040	IBM 1800
Disc (512K wds)	1448	2310	1448	1810
Disc (100M wds)	1445	NA	NA	NA
M/7 (37 ips)	3412	NA	3412	2401/02
M/7 (75 ips)	3416	NA	3416	2401/02
Card rdr (600 cpm)	3463	2501	3463	NA
Card rdr (1,000 cpm)	3465	2501	3465	NA
Printer Keyboard	NA	NA	4133	1053/ 1816
P/T Reader	3431	1054	3431	1054
P/T Punch	3421	1055	3421	1055
Printer (600 lpm)	3482	NA	3482	NA
Printer (300 lpm)	3484	1403	3484	1443
Plotter	3442	1627	3442	1627
Digital Input	NA	NA	4200	Misc
Digital Output	NA	NA	4232	Misc
Analog Input	NA	NA	4258	1851
Analog Output	NA	NA	4234	1856
Process Interrupt	NA	NA	4214	Misc
Bisync Communications	4101	BSC adapter	NA	NA
Multiterminal Communications Adapter	4108	RPQ	NA	NA
Real-Time Clock	4185	NA	NA	NA
Floating-Point Firmware	9078	NA	NA	NA

COMPATIBILITY

The META 4 systems are compatible with IBM's 1130 and 1800 computers at the instruction level; they

Table 3. Digital Scientific META 4: Software

Package	Description
Microassembler	Converts symbolic microcode to machine language; requires 8K words of memory, card reader, printer, disc
System Utilities	Object deck punch, ROM debug; require 8K words of memory, disc, card reader, console printer

are also I/O-compatible in that IBM peripherals can be used with the META 4. DSC supplies compatible peripheral subsystems and some compatible controller interfaces to provide better price/performance. Controllers that effectively create 1130 SAC channels or 1800 data channels are attached to the META 4 backplane to allow any IBM controller to be attached.

The IBM 1130 instruction set is a subset of the 1800. Although the 1800 has a fuller complement of peripheral offerings, 1130 and 1800 programs can run on each other's systems if the peripheral environment is the same, and if the 1800 programs do not use instructions unavailable on the 1130. Unlike IBM's 1130, the DSC 4030 has provisions for handling 1800 instructions (among others) on the 1130 emulator.

MAINTENANCE

Digital Scientific handles maintenance through area service offices across the United States. The standard maintenance contracts provide for periodical preventive maintenance visits and emergency on-site service. Contracts can cover one, two, or three shifts during the week or on weekends. Users who have purchased systems can also obtain maintenance on an hourly basis instead of through a monthly contract. Provision is not made for a dedicated on-site engineer on a contractual basis although a large remote installation may have the undivided attention of the area engineer.

TYPICAL PRICES

Model Number	Description	Monthly Rental $ YR*	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE			
	Processor and Options			
4001-X[1]	META 4 Basic Processor	—	10,225	—
4011	Memory and I/O Register	—	1,500	—
4012	I/O Register	—	550	—
4013	Double-Bus Accumulator	—	350	—
4025	Scratch-Pad Memory	—	3,000	—
4150	Microprogrammer's Panel Firmware	—	975	—
1425	Read-Only Memory	—	2,725	—
9000	ROM Pattern Boards	—	400	—
9100	Custom Artwork	—	400	—
9101	Custom ROM Pattern Board	—	25 each	—
	IBM 1800 Emulator			
4040	Basic Processor	1,157	32,800	219
4118	OEM Channels (set of 5)	117	5,000	34
4125	Selector Channel (4040 prereq)	327	9,250	62
9078	Floating-Point Arithmetic	29	1,000	—
4133-0	I/O Typer and Controller	124	3,500	24
	IBM 1130 Emulator			
4030-1	Basic Processor — 8K	1,170	33,175	222
-2	Basic Processor — 16K	1,431	40,575	271
-3	Basic Processor — 32K	1,981	56,200	375
4031	Processor without Emulator	759	21,500	144
4130	Storage Access Channel	43	1,200	8
4185	Real-Time Clock	23	625	5
9078-1	Floating-Point Arithmetic	29	1,000	—
	4031 and 4040 Core Memory Subsystems			
4068-1	8K	351	9,925	67
-2	16K	611	17,325	116
-3	24K	901	25,550	171
-4	32K	1,162	32,950	220
-5	40K	1,475	41,830	279
-6	48K	1,736	45,230	329
-7	56K	2,026	57,455	384
-8	65K	2,286	64,855	433
4069	Auxiliary Core Feature for 4068	283	8,000	54
	MASS STORAGE			
	For 4040			
1444-2	Disc Subsystem (512K words)[2]	342	9,500	70
1448-2	High-Speed Disc Subsystem (512K)	406	11,500	77
	For 4030			
1445-1	Disc Subsystem (10M words)	775	21,000	175
-2	Additional Drive (20M word total)	604	16,500	132
1448-1	Disc Subsystem (512K words)	406	11,500	77
	INPUT/OUTPUT MAGNETIC TAPE[2]			
3410-2A	Single Drive (7-track; 37.5 ips; for 4040 only)	397	11,250	75
3410-2B	Dual Drive (7-track; 37.5 ips; for 4040 only)	608	17,250	115
3412-2A	Single Drive (9-track; 37.5 ips)	405	11,450	77
3412-2B	Dual Drive (9-track; 37.5 ips)	623	17,650	118
3416-2A	Single Drive (9-track; 75 ips)	492	13,950	93
3416-2B	Dual Drive (9-track; 75 ips)	711	20,150	135
	Punched Card[2]			
3463-1/2	Card Reader (600 cpm)	210	6,950	40
3465-1/2	Card Reader (1,000 cpm)	281	7,950	53
3472-2	Controller for IBM 1442 Model 5, 6, or 7	177	5,000	34
3463-1	Card Reader (600 cpm)	210	5,950	40
3472-1	Controller for IBM 1442 Model 5, 6, or 7	105	2,500	33
3474-1	Controller for Univac VIP 1710 Punch	106	3,000	20
	Paper Tape Equipment			
3421-X	Punch (50 cps)	129	3,640	25
3431-X	Reader (400 cps)	111	3,120	21
3432-X	Reader with Spooler	155	4,365	30
	Printers[2]			
3482-2	Printer (600 lpm)	864	24,500	164
3484-1/2	Printer (300 lpm)	442	12,500	84
3482-1	Printer (600 lpm)	731	19,875	163
3486-1	Printer (165 cps)	362	10,250	69
	Plotters[2]			
3443-X[1]	XY Plotter Controller for DSC 3442, Houston DP-1, CalComp 500, and IBM 1627	36	1,000	7

TYPICAL PRICES (Contd.)

Model Number	Description	Monthly Rental $ 1YR*	Purchase $	Monthly Maint. $
INPUT/OUTPUT MAGNETIC TAPE(2)				
3442	XY Plotter (3443-X required)	177	4,975	34
3444-1	Controller for CalComp 700 Communications (for 4030 only)	53	1,500	10
4101-1	Binary Synchronous Communications Adapter	152	4,275	29
4108-1	Multiple Terminal Communications Adapter (8 lines)	169	4,775	32
0401	Cabinet	27	750	5
4100-X	I/O Chassis Extender	89	2,500	17

Notes:
(1) X = 1 for 1130 Emulation System.
X = 2 for 1800 Emulation System.
(2) Subsystems include interface to META 4; generally submodel 1 refers to 4030 and 2 to 4040.
*Rental prices include maintenance.
— Not Applicable.

HEADQUARTERS

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GENERAL AUTOMATION

SPC-12 System Report

OVERVIEW

The General Automation SPC-12 systems are byte-oriented small minicomputers aimed at communications, industrial automation, and process control applications. The SPC-12 was General Automation's first product (1968). It uses a basic hybrid architecture; data is stored in 8-bit words (bytes), but addresses are 12-bit words developed from doubleword instructions.

The company had intended to extend the life of this line by adding an LSI model that used a unique silicon-on-sapphire (SOS) MOS technology. Unfortunately, however, problems with GA's supplier forced the company to withdraw the product, which had excited the interest of the minicomputer market because of its technological advances. GA continues to supply SPC-12 and LSI-12/16 systems to current OEM customers but the company's main computer is its SPC-16 line. Table 1 summarizes the mainframe characteristics.

PERFORMANCE

The SPC-12 computers enjoyed considerable success during their early years, supplying the foundation on which General Automation built its reputation. They will undoubtedly be sold for some time to OEM manufacturers who use the mini as the base for their own systems.

It is clear that the SPC-16 will supplant the SPC-12 product line for new customers. The only other major 12-bit system that remains on the market is Digital's popular PDP-8, which has remained viable because of the phenomenal volume of software that accompanies it.

User Reactions

An OEM manufacturer making automatic electronic insertion equipment chose the SPC-12 system over Digital, Data General, and other major minicomputers because of the system's size and reliability, its price and, most important, General Automation's willingness to help him with his problems. He felt that General Automation was particularly strong on support and responsiveness to the customer's individual needs — "they try harder" — and in the five years that he has used the SPC-12, he has been very pleased with the computer and with his relationship with General Automation.

Table 1. A Comparison of Specifications of General Automation Computers

MODEL NUMBER	SPC-12	SPC-16	18/30
CENTRAL PROCESSOR			
No. Programmable Registers	7	8 std, 8 opt	15
Addressing (no. of wds)			
Direct	4K	32K	32K
Indirect	16K	32K	32K
Indexed	16K	32K	32K
With Paging	—	64K	—
Instruction set			
Number (std; opt)	52	78; 5	32(2)
Decimal Arithmetic	No	No	No
Floating Point	Sub-routine	Opt	Sub-routine
Priority Interrupt Levels	1-64	64	8-61
MAIN STORAGE			
Type	Core	Core	Core
Cycle Time (μsec)	2.16	1.44; 0.960; 0.800(1)	0.960
Basic Addressable Units	8-bit word; 16-bit doubleword	Word, byte, bit	Word
Bytes/Access	1	2	2
Min Capacity (bytes)	4K	8K	16K
Max Capacity (bytes)	16K	128K	64K
Increment sizes (bytes)	4K; 8K	8K	8K
Parity	No	No	Std
Protect	Opt	Opt	Std
ROM			No
Use	Bootstrap	Program and/or loaders	—
Capacity (wds)	64	128K	—
I/O CHANNELS			
Programmed I/O	Yes	Yes	Yes
DMA Channels (No.)	Opt	Opt (8)	5
Multiplexed I/O	DMT	No	No
Max Transfer (wds/sec)			
Within Memory (K bytes)	460	173; 260; 320(1)	260
Over DMA (K bytes)	460	700; 1,040;	833
DMT	460 (burst) 100 (interleave)	1,250(1)	

(1) Submodels 40(45), 60(65), and 80(85) respectively.
(2) Additional instruction forms for double precision.

CONFIGURATION GUIDE

The SPC-12 processor has three submodels which differ in the maximum memory that can be housed in the chassis and the number of slots available for attaching subunit controllers. The 12/10 has a maximum memory size of 16K words (bytes) and no internal provisions for attachment of controllers. The 12/15 has a maximum memory size of 8K words (bytes) and provisions for the internal attachment of up to seven controllers. The 12/20 has a maximum memory size of 16K words (bytes) and provisions for the internal attachment of up to 19 controllers. All can be configured with 4K or 8K words of memory without impacting the number of available slots for peripherals. A Teletype interface, control panel, parallel and serial I/O, interrupt line, and power supply are standard. A ROM TTY bootstrap loader, memory protect, DMA channel, high-speed I/O access, power fail/automatic restart, and relative time clock/operations monitor alarm can all be added as options. All except the latter two items can be installed in the field; none require a processor slot except the DMA channel, which requires one slot.

Table 2. General Automation SPC-12: Peripherals

Model Number	Description
Teletypes	
1362/63	ASR 33/35, 10 cps
Minicontrollers	
1411	Digital Differential Input for 16 digital inputs
1412	Buffered bipolar power drive for 16 power drives
1413/14	Generalized Input/Output Buffers, 16 bits
1431	Digital Input Relay Receiver to 16 isolated relay coils
1432	Buffered Contact Output for 16 Form A outputs
1441	Analog I/O, 12 bits, 3.3 msec conversion
1451	High Level Input MUX 16 channels
1452	High Level Differential MUX, 8 channels
1453	Low Level Differential MUX, 8 channels
1481	Analog Output Holding Amplifier, 8 channels
Communications	
1541/1551	Bell 103A2 Controller, 110-300 baud, 1551 has 801 ACU
1542/1552	Bell 202C2 Controller, 1,000-9,600 baud, 1552 has 801 ACU

Peripherals for the SPC-12 consist of Teletypes, communication devices, and a series of process minicontrollers (see Table 2). SPC-12 minicontrollers are pre-engineered to eliminate redundant electronics and to permit economical field installations, expansion, and servicing.

The SPC-12 system requires three boards for the CPU, 4K words of memory, and electronics. The enclosure is 5.25 by 17.5 by 20 inches. The basic SPC-12 system weighs less than 30 pounds.

The software packages available for the SPC-12 are listed in Table 3.

HEADQUARTERS

General Automation, Inc.
1055 S. East Street
Anaheim CA 92805

Table 3. General Automation SPC-12: General-Purpose Software

Package	Characteristics
LANGUAGE PROCESSOR	
Conversational Assembly System (CAS)	Single-pass absolute assembler with on-line correction
UTILITIES	
PGS Loader/Puncher	Outputs selected areas of memory in object format; loads its own output or output from assemblers or memory load builder
Debug Test and Verify	For processor, memory, peripherals, controllers
Memory Load Builder	Performs program and extended memory linkages, producing absolute or relocatable object code and optional load map
Utilities Text Editor Input/Output System	Output is input to Assembler Calling sequences, std I/O drivers; user can add his own I/O drivers
Arithmetic Library	Floating point, double precision arithmetic, monitor interfacing
Concordance	Cross reference of symbolic names

TYPICAL PRICES

Model Number	Description	Purchase $ (1)	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE		
1211-1100	SPC-12/10 (includes 4K words of 8-bit core memory expandable to 16K; 3 hardware index registers; 4 hardware accumulators; control panel; priority interrupt control & interrupt line; 12-bit parallel I/O channel; serial I/O channel with interface for TTY Model 33 or 35; direct memory transfer channel and memory access facility; 5.25-in. high enclosure; cooling; & remote power supply for operation at 115 vac, 47-63 Hz input power)	2,980	30
1211-1200	SPC-12/10 (same as 1211-100 except has 8K words of memory)	3,850	40
1211-2100	SPC-12/10 (same as 1211-1100 except 230 vac, 47-63 Hz)	2,980	30
1211-2200	SPC-12/10 (same as 1211-1200 except 230 vac, 47-63 Hz)	3,850	40
1215-1100	SPC-12/15 (same as 1100 but expandable to 8K)	3,480	35
1215-1200	SPC-12/15 (same as 1215-1100 except has 8K words of memory)	4,350	45
1215-2100	SPC-12/15 (same as 1215-1100 except 230 vac, 47-63 Hz)	3,480	35
1215-2200	SPC-12/15 (same as 1215-1200 except 230 vac, 47-63 Hz)	4,350	45
1220-1100	SPC-12/20 (same as 1100 except in 10.5-in. enclosure with 19-subunit capacity)	3,980	40
1220-1200	SPC-12/20 (same as 1220-1100 except has 8K-word memory)	4,850	50
1220-2100	SPC-12/20 (same as 1220-1100 except 230 vac, 47-63 Hz)	3,980	40
1220-2200	SPC-12/20 (same as 1220-1200 except 230 vac, 47-63 Hz)	4,850	50

Model Number	Description	Purchase $ (1)	Monthly Maint. $
	Processor Options (2)		
12XX-0100	Additional 4K Memory	1,600	16
12XX-0200	Additional 8K Memory	2,500	26
12XX-0080	Hardware Bootstrap Loading	250	2
12XX-0090	Memory Protect	225	2
12XX-0001	Direct Memory Transfer Channel	1,500	10
12XX-0002	Memory Access Adapter	500	7
12XX-0004	Relative Time Clock/Operations Monitor Alarm	175	NC
12XX-0008	Power Failure Detection/Automatic Restart	250	NC
1210-0100	System I/O Adapter	400	5
1210-1100	System I/O Adapter and Power Supply	800	12
1210-1209	Power Supply	400	7
1210-2100	System I/O Adapter and Power Supply	800	12
1210-2209	Power Supply	400	7
1210-1110	System I/O Enclosure	800	12
1210-2110	System I/O Enclosure (230 vac, 47-63 Hz)	800	12
1210-0211	Cable Interface Translator	250	3
1210-0212	Function Interface Translator (3)	250	3
1210-0213	Priority Interrupt Expander (3)	500	5
1210-0214	Cable Interface Translator (CIT)	250	3
	INPUT/OUTPUT		
	Console Teletypewriter		
1362-0500	Teletype Modification Kit for ASR-33	25	—
1362-1000, 1	System Console TTY (ASR-33, 115 vac, 50/60 Hz)	1,250	35
1362-2000	System Console TTY (ASR-33, 220 vac, 50 Hz)	1,350	35
1362-6210	TTY Controller (TTC) (with ASR-33)	500	5
1363-0500	TTY Modification Kit for ASR-35	75	—
1363-1000, 2000	System Console TTY (ASR 35)	4,500	62
1363-6210	TTY Controller (TTC) (for use with ASR-35 half duplex)	500	5
	DATA COMMUNICATIONS		
	Bell System Data Set Controllers (requires 1210 System I/O Adapter) (3) (4) (5)		
1541-112A	103A2 (& 801 Automatic Calling Unit ACU, half-duplex; requires 2 subunit slots)	720	10
1541-122A	103A2 (& 801 ACU; full-duplex; requires 3 subunit slots)	1,020	15
1542-112B	202C2 and 801 ACU (half-duplex; 4-wire; requires 2 subunit slots)	720	10
1542-122B	202C2 and 801 ACU (full-duplex; 4-wire; requires 3 subunit slots)	1,020	15
1551-112A	103A2 (half-duplex; requires 2 subunit slots)	720	10
1551-122A	103A2 (full-duplex; requires 3 subunit slots)	1,020	15
1552-112B	202C2 (half-duplex; requires 2 subunit slots)	720	10
1552-122B	202C2 (full-duplex; requires 3 subunit slots)	1,020	15
	Data Set Interconnection Cable		
1541-7100	For 1541-112A	250	NC
1541-7200	For 1541-122A	400	NC
1542-7100	For 1542-112B	250	NC
1542-7200	For 1542-122B	400	NC
1551-7100	For 1551-112A	250	NC
1551-7200	For 1551-122A	400	NC
1552-7100	For 1552-112B	250	NC
1552-7200	For 1552-122B	400	NC
1901-1100	System Enclosure	1,200	7

Notes:

(1) Most items, excluding system enclosures, power supplies, and TTY units, are subject to discount, RPQ from manufacturer.

(2) Insert processor identifier in model number. Replace XX with 11 for SPC-12/10, 15 for SPC-12/15, and 20 for SPC-12/20.

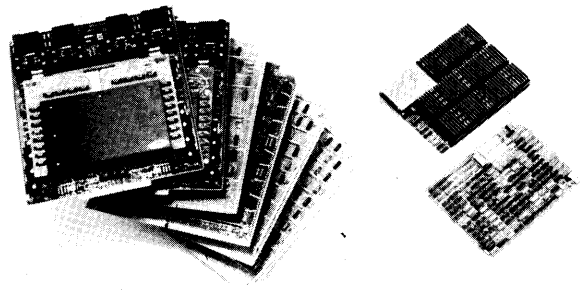
(3) Requires 1 subunit slot, unless noted otherwise. System wiring and test charges are $100/board. Price shown includes connectors and strain reliefs (cable clamps). If wiring and test are not desired, change 3rd digit of feature code to 4; i.e., 1411-1040. Price remains same.

(4) Insert baud rate identifier in model number. Replace A with 1 for 110 baud, 3 for 300 baud, and 5 for 150 baud. Replace B with 0 for 1,000 baud, 2 for 1,200 baud, 8 for 1,800 baud, and 4 for 2,400 baud.

(5) To order controllers without wiring and test or strain reliefs, change 3rd digit of feature code to 0 and reduce price by $20; i.e., 1541-110A – $700. Connector on cabling side of controller is included, where applicable.

GENERAL AUTOMATION

SPC-16 and LSI-16 Series



74-208

LSI-16 board (far right) has all power and performance of the six SPC-16 board on left.

OVERVIEW

General Automation introduced the SPC-16 Series as the "super performance" 16-bit industrial automation computers in its family of fourth-generation equipment. Featuring three models that differ only in core speed — 800, 960, or 1,440-nanosecond cycle time per 16-bit word — the company offers each model "bare-bones" OEM (SPC 16/45, 16/65, 16/85) or packaged (SPC 16/40, 16/60, 16/80) with a full set of features for real-time applications. Each SPC-16 model is a dual-speed computer in that its read/write core memories are interchangeable with faster read-only memories operating at 400, 480, and 720-nanosecond cycle time per word, respectively. Construction features multilayer printed circuit boards, medium-scale integrated circuits, and an operating environment of 0°C to 50°C with up to 90 percent relative humidity.

The General Automation LSI-16 is General Automation's new microcomputer utilizing SOS (silicon-on-sapphire) LSI technology, engineered into a system that is both hardware- and software-compatible with the SPC-16 line. GA's first SOS product was the LSI-12/16, a microprocessor with hybrid architecture (8-bit data word, 12-bit addressing, 16-bit I/O) that is program-compatible with the SPC-12 line but uses SPC-16 peripherals. Both the LSI-12/16 and the new LSI-16 have the CPU on one SOS chip, and control ROM (CROM) on a second chip; both chips with all basic interfacing circuitry are on one board. Both the LSI-12/16 and LSI-16 are sold either at the board level (without chassis and power) or at the system level (with chassis, power, console, and interfacing ready to attach a full complement of peripheral devices).

General Automation is also the first minicomputer manufacturer to use silicon-on-sapphire (SOS) technology. This technology was first developed by Autonetics, and it has been further refined by Rockwell International for aerospace and military applications. General Automation believes this technology is the way to achieve bipolar TTL performance at MOS/LSI circuit density and power consumption, combined with very high reliability. General Automation designed and developed the microcomputer but initial production fabrication has been done in cooperation with the microelectronics division of Rockwell International. The n-channel SOS technology used for the LSI-16 and LSI-12/16 processor chips is compatible with TTL logic, unlike p-channel MOS. Because more circuits can be placed on a single chip, load resistors (and power consumption) are smaller and higher processor speeds can be obtained, higher than speeds attainable using either p-channel or n-channel MOS. General Automation's processor chip contains around 2,000 gates on one 4,000 pico-acre chip, the equivalent of around 4,000 to 5,000 transistors.

One advantage of the new technology is lower cost. At the board level, the LSI-16 costs $1,350 for a processor with 1K words of memory and $5,750 for a processor with 32K words of memory with the minimum purchase order of 15 units. Systems cost $2,350 for 1K words and $7,100 for 32K words, with the minimum purchase order of five units.

In addition, the LSI-12/16 and LSI-16 are designed to be components and are sold without chassis and power supply. The LSI-12/16 CPU and up to 2K words of RAM or 8K words of ROM can be put on one board. The faster LSI-16 system has a minimum of two boards, but its 32K-word maximum memory is actually double the memory capacity of the LSI-12/16 because the LSI-16 uses 16-bit words and the LSI-12/16 uses 8-bit words for data storage. The LSI-16's speed, architecture, and memory enable it to be used as a component in OEM applications requiring more processing power and storage capacity than the LSI-12/16. The SPC-16 and LSI-16 mainframe characteristics are listed in Table 1.

There are only minimal differences in system architecture between the SPC-16 and the LSI-16. The SPC-16 submodels 16/45, 16/65, and 16/85 correspond to the 16/40, 16/60, and 16/80 respectively, but allow memory expansion up to 128K words. The LSI-16, on the other hand, has a cycle time of 1.8 microseconds; at the time of writing, it has no provisions for expanding memory to 128K words. Thus, it enters at the low end of the SPC-16 product line, rather than as a replacement. The instruction set, registers, I/O control, peripherals, software, and all other standard and optional features are identical to other members of the series, but some options are standard. Table 1 presents a comparison of the specifications of the SPC-16, LSI-16, and LSI-12/16 systems.

The first LSI-16s were delivered in the fall of 1974. General Automation expects to be mass-producing the system in January 1975.

General Automation recently announced its DM 100 Series, SPC-16/65-based systems. The DM 120 operates as a remote job entry (RJE) workstation that can communicate with other DM 100s or IBM Systems 360/370s. The DM 130 is a data base management system that operates in a multiprogramming/multitasking environment. It can support up to four CRT

Table 1. General Automation SPC-16 Series: Mainframe Characteristics

CHARACTERISTICS	SPC-16 Series	LSI-16 Series
CENTRAL PROCESSOR		
No. of Internal Registers	8 std; 8 opt	16
Addressing Direct (no. of words)	32K	32K
Indirect	32K	32K
Indexed	32K	32K
With Paging	128K	–
Instruction Set Number	78 std; 5 opt	78 std; 5 op
Decimal Arithmetic	No	No
Floating-Point Arithmetic	Opt	Opt
Priority Interrupt Levels	64	64
MAIN STORAGE		
Type	Core	MOS; Core
Cycle Time (msec)	1.44; 0.960; 0.800 (1)	1.8
Basic Addressable Unit	Word, byte, bit	Word, byte, bit
Bytes per Access	2	2
Min Capacity (bytes)	8K	1K
Max Capacity (bytes)	64K; 256K (2)	32K
Increment Size (bytes)	4K, 8K, 16K	1K, 4K
Parity	No	Opt
Protect	Opt	Opt
ROM		
Use	Program and/or loaders	Program and/or loaders
Capacity (bytes)	32K	32K
I/O CHANNELS		
Programmed I/O	Yes	Yes
DMA Channels (no.)	Opt (8)	Opt (8)
Multiplexed I/O	No	No
Max Transfer Rate (words/sec)		
Within Memory	173K; 260K; 320K	–
Over DMA	700K; 1,040K; 1,250K	–

(1) Cycle times determine whether model number is 40/45, 60/65, or 80/85 respectively.
(2) The first number refers to Models 40, 60, and 80, while the second refers to 45, 65, and 85.

workstations or perform batch compilations or communications in background. A DM 130/2 is a dedicated small business computer available from a distributor network on a turnkey basis. The DM 140, the most powerful system in the series, can support up to 32 remote CRT workstations in the foreground concurrently with background batch compilations or communications.

COMPETITIVE POSITION

In the past two years however, GA has been expanding its markets by adding sales and service offices in the United States and abroad and by providing better terms for OEM users. With an installed base of over 1,000 minicomputers, a substantial amount of system software, new compatible systems to effect cost performance savings, and its edge in the end-user market, GA is a strong competitor. Recent stringent controls on automobile design for safety and exhaust emission should provide an expanded market for the SPC-16.

To encourage OEM users, General Automation rents SPC-16 systems to potential OEM customers while they are designing their systems. OEM users can pass on their leftover warranty time to their customers. In addition, the period for counting time under quantity discount contracts does not begin until the OEM user makes the first delivery. Quantity discounts of up to 40 percent are available.

General Automation's SOS technology systems, because of their cost and compact size, occupy an intermediate position in the computer market between microprocessors and minicomputers; they compete in both markets as well as in new markets that will be developed because of their processing power, small size, and low price. The new technology should reduce reliability problems and attendant maintenance costs. Complex connections between CPU components are automatically reduced or eliminated when the processor is reduced to a single chip and the CPU and interfacing fit on a single board.

Computer Automation is the only other manufacturer to produce a 1-board computer; its Naked Mini LSI stores seven p-channel MOS/LSI chips plus up to 4K 16-bit words of RAM memory on one board. Although the system has more chips and is much slower (it is memory bound in the MOS version) it provides more RAM memory capacity on the CPU board, and so may be better suited to some applications. The Computer Automation board, which is about one-third larger than the 7¾ by 11-inch General Automation board, has been likened to a pizza box. The Naked Mini LSI, like the LSI-12/16 and LSI-16, can come "clothed" with chassis, independent power, and a full range of peripherals in the Alpha LSI systems.

Although the MOS version of the Alpha is slow, two higher-speed, more conventional TTL versions with CPU on one board and memory on another are like the GA LSI-16 in many respects. The General Automation LSI-12/16 systems have an edge in high volume applications because of lower price, higher speeds and support of various memory types, whereas the Computer Automation system costs less for lower volume applications. The LSI-16, on the other hand, is faster because it is memory-, not processor-bound. Instruction execution times are faster in spite of the slightly slower cycle speed of 1.8 microseconds.

GA stresses its strong systems engineering and applications expertise in the face of its competition. Computer Automation stresses that the company sells only to OEM manufacturers, thus they will not become competitors of their own customers.

General Automation is apparently going the same system route as other minicomputer manufacturers. Its new DM-100 Series systems (based on SPC-16/65), parallel the M230, M260, and S250 data management systems offered by Hewlett-Packard. Its DM-130/2, offered as a turnkey system via a distributor network, follows the same route Microdata has taken with its Reality system.

In addition, GA is offering a DM-200 Series of systems, functionally similar to the DM 100 Series, but based on the GA-18/30 computer, which has been sold as an IBM System 1130 upgrade since 1968. These systems will also emphasize data management functions, but they are oriented toward industrial applications. The 1130 upgrade system, now called the 230/2, will be distributed on a turnkey basis like the 130/2.

These systems will compete with the small business computers offered by the large mainframe manufacturers, as well as those offered by other minicomputer manufacturers.

USER REACTIONS

The SPC-16 users we interviewed were using their systems for a wide variety of applications. A large petroleum manufacturer was using a SPC-16 for high-speed data acquisition of seismologic data used in petroleum exploration — the system had discs magnetic tapes, and punched I/O cards and tape as well as plotters. A manufacturer of discs, tapes, and punched tape peripherals has several operating in engineering and testing applications (using their own peripherals). An OEM manufacturer uses dual processors to run a Telex switching system it markets. Another user had two SPC-16s operating online to IBM System 360/65s (special interface) to run an automated warehouse. A branch of a large western university uses a processor with multiplexor as a front end for 20 terminals communicating with a Burroughs 1700; another college was using it as an RJE terminal for an IBM System 370/165.

Users bought their systems for a variety of reasons related to their applications, but one common reason noted by several was the ease of programming. Several users (one of the colleges, the OEM manufacturer, and the petroleum company) were doing their own programming even at the systems level and found the instruction set well suited to their needs. The college found it ideal for communications; the petroleum company believed the Operate On Memory feature on the DMA channel was unique at the time it purchased its systems.

CONFIGURATION GUIDE

All processors can address up to 64 peripheral device controllers. Table 2 lists the available peripherals.

The LSI-16 is sold with a regular chassis, in which case it is like an SPC-40, 60, or 80, but with a slower cycle time and lower price. It is also sold at the board

Table 2. General Automation SPC-16 Series: Peripherals

Peripheral Device	Description
MAGNETIC TAPE	
3331, 3332, 3333 Magnetic Tape Subsystems	9-track; 25, 37.5, 75 ips; 800 bpi; 20K, 30K, 60K bytes/sec; 2,400-ft reel
3334, 3335, 3336 Magnetic Tape Subsystems	7-track; 25, 37.5, 75 ips; either 556/800 or 200/556 bpi; 2,400-ft reels; master unit includes 1 drive, can handle 3 more slave drives
FIXED-HEAD DISCS	
3342 Head/Track Storage Drive and Controller	128K or 256K-word capacity; access time 8.5 msec; transfer rate 2 MHz; requires 2 subunit slots
MOVABLE HEAD DISCS	
3341 Disc Storage System	Capacity 3.2M wds/drive; 10 disc surfaces; seek time, 10-65 msec; avg latency 12.5 msec; master unit has 1 drive; can control up to 3 more slave drives
3343 Disc Storage Subsystem	Capacity 12.8M wds/drive; 20 surfaces; seek time, 10-65 msec; avg latency, 12.5 msec; peak transfer rate; same configuration and submodels as 3341
3346 Disc Storage System	Capacity 2.5M wds/drive; 4 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 removable disc
3347 Disc Storage Subsystem	Capacity 1.25M wds/drive; 2 surfaces; seek time 14-85 msec; latency 20 msec; one fixed and 1 movable disc
3349 Floppy Disc Subsystem	Capacity 147K wds/drive; 288 wds/sector, 8 sectors/trk, 64 tracks
CONSOLE TYPEWRITERS	
3362 Teletype Model ASR 33	10 cps; includes pt read/punch
3363 Teletype Model ASR 35	10 cps; includes pt read/punch uses no subunit slot
PAPER TAPE	
3321 Paper Tape Reader and Controller	8-channel tape; 400 cps
3322 Paper Tape Punch and Controller	8-channel tape; 75 cps
3323 Paper Tape Reader/Punch and Controller	Combines 3321 and 3322; requires 2 slots
3325 Paper Tape Reader/Punch and Controller	8-channel tape; 300-cps reader; 75-cps punch; fan fold option; requires 1 subunit slot
PUNCH CARD (std 80-col card)	
3315 Card Reader and Controller	300 cpm; light duty

Table 2. (Contd.)

Peripheral Device	Description
PUNCH CARD (std 80-col card) (Contd.)	
3316, 17, 18 Card Reader and Controller	400, 600, 1,000 cpm; heavy duty
3314 Card Punch and Controller	35 cpm; includes keyboard
LINE PRINTERS	
3353 Line Printer and Controller	Up to 132 cols/line, 600-lpm; ASCII code
3357 Line Printer/Card Reader and Controller	Printer: 132 cols, 600 lpm; reader; 80-col cards, 400-cpm
3354-1000 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 7 x 8 dot matrix, 6 lpi; 125 lpm; card reader 300, 400, 600, 1,000 cpm
3354-1200 Series Low-Speed Printers with Controller (with or without card reader)	132 cols, 5 x 7 dot matrix, 6-8 lpi, 200 lpm; card reader, 300, 400, 600, 1,000 cpm
3355 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 1,000-cpm card reader (80 cols); print 6-8 lpi option
3358 Line Printer/Card Reader and Controller	600-lpm printer, 132 cols; 6-8 lpi 300-cpm card reader (80 cols)
A/D & D/A Available	
DATA COMMUNICATIONS	
1561 Asynchronous Communication Controller	For RS232-compatible data set (Bell 103 and 102); full-duplex; 75 to 2,400 bps rates available; 1, 2, or 4 lines
1571 Synchronous Communication Controller	For Bell 201 or equivalent data set; double-buffered, full-duplex; external timing permits wide range of data rates
1581 Series Asynchronous Communications Controller	Interface for full-duplex lines; std rates are same as 1561; 1, 2, or 4 lines
1567 Automatic Calling Unit Subsystem	Provides interface for 4 automatic calling units
1590 Communication Multiplexor Common Equipment	Double-buffered, full-duplex interface for async lines; same baud rates as 1581; up to 16 or 32 lines

level, with the CPU on one board and up to 32K words of memory on a second board — somewhat like an SPC-45, 65, or 85 with a slower cycle time, but with a lower price and much more compact. LSI-16s can attach the same peripherals as SPC-16s proper, but maximum memory is 32K words, compared to 128K words for the SPC-16/45.

Software packages available for the SPC-16 and the configurations they require are listed in Table 3.

Table 3. General Automation SPC-16 Series: Software

Model No.	Characteristics	Comments
BSP-16	Basic systems program package	Minimum configuration: CPU, 4K-word memory and Teletype
FSOS-16	Freestanding operating system, job-oriented, tape supported	Minimum system: CPU, 8K-word memory; HSPTR/CR, TTY
RTX-16	Real-time executive, runs under FSOS-16 or DBOS-II	CPU, 8K words of memory, TTY
DBOS-II	Disc-based operating system	CPU, 16K words of memory, disc, TTY
RTOS-II	Real-time operating system; multiprogramming, foreground/background	CPU, 24K words of memory, disc, TTY
CAP-16	Basic assembler	CPU, 4K words of memory, TTY
CAP-16M	Macro assembler	CPU, 8K words of memory, TTY
FORTRAN IV Compiler	Extended ANSI specifications; real-time compiler with code optimization	CPU, 12K words of memory, TTY
Commercial FORTRAN Compiler	FORTRAN with COBOL-like extensions, string manipulation	CPU, 12K words of memory, TTY
BASIC Interpreter for FSOS, DBOS, and RTOS	Single-user conversational language, or multiple users, real-time conversational mode	Dedicated CPU; 8K, 16K, and 24K words of memory, respectively; disc and TTY

COMPATIBILITY

The SPC-16 Series, including the new LSI-16 computers, are all compatible. Programs developed for one system can run on another, except in rare instances where the cycle time is used in some way by the program. The SPC-16 is not program compatible with either the SPC-12 family (including the new LSI-12/16), or the GA 18/30. SPC-16 programmed I/O peripherals, however, can be attached to the LSI-12/16.

MAINTENANCE

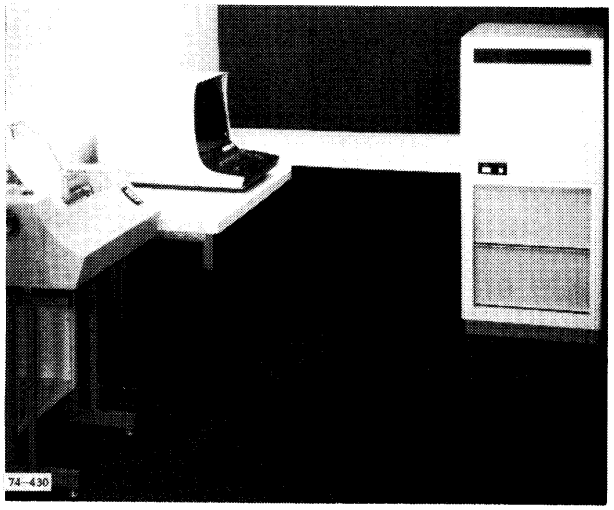
General Automation maintains its own systems out of its 25 sales and service offices in the United States.

HEADQUARTERS

General Automation, Inc.
1055 South East St.
Anaheim CA 92805
Tel. (714) 778-4800

GRI COMPUTER

GRI-99 Series, Models 10, 30, 40, and 50



OVERVIEW

The GRI-99 systems are moderately small general-purpose minicomputer systems suitable for functions ranging from dedicated controller applications and time-related applications to customized process control. Rather than aiming the systems at the general marketplace, GRI is directing the GRI-99 Series to OEM markets. The GRI-99 Series is very modular with respect to hardware but currently offers very little applications software.

There are four models in the GRI-99 Series: 10, 30, 40, and 50. The models differ in the processor features, the type of system console included, and the number of devices that can be connected. The Model 10 is the least powerful and offers the fewest features; each higher-numbered model offers progressively more power and options. The Model 10, then, is a stripped-down system suitable for dedicated controller applications. The Model 30 is an economical and versatile system particularly suited for real-time applications and for systems dedicated to complex tasks. The Model 40 is like the Model 30, but it has extended mathematics and floating-point arithmetic capabilities. The Model 50 includes context switching, stack processing, bit manipulation, block (byte string) extended arithmetic for effective data transfer and multiprogramming, and disc I/O facilities. Characteristics of the models appear in Table 1.

All systems are organized around an asynchronous bus that connects all system elements, functioning much like the PDP-11 Unibus. Although it is not a microprogrammed system in the usual sense of the word, customized macroinstructions are easily added to the system via ROM modules accessed by an External Instruction (EI). Other system elements such as extra registers can be added in the same manner.

GRI provides a variety of peripheral devices to choose from, including discs, Teletype, display, paper tape and card I/O, printers, magnetic tape systems, communications devices, and extensive A/D, D/A, and digital I/O interfacing. The Grisette II cassette tape system is used to provide a hardware/software combination enabling the user to create an automatic load-and-go system, using an auto loader feature. Peripherals available are listed in Table 2.

System software includes a cassette tape real-time executive operating system, a relocatable assembler, source text editor, utility package, and diagnostic and math packages. GRI has developed a small business system called System 99, which runs under a single-user or multiuser disc operating system that supports RPG II and Basic compilers, as well as various utilities. The System 99 is based on the Model 50.

The GRI-99 Series was introduced in 1972 and is successor to GRI's 909 Series first delivered in 1970. The earlier 909 Series had the distinction of being the first system on the market with the asynchronous single bus architecture, which has since been made famous by DEC's PDP-11. Texas Instruments (960A/980A) also uses roughly the same type of architecture. Many of GRI's early users chose the system because of this innovative architecture.

COMPETITIVE POSITION

Although the company does sell to end users, GRI's main impact is in OEM markets. Companies strong in the 16-bit OEM market include Computer Automation, Microdata, and General Automation. Computer Automation and General Automation recently strengthened their positions by delivering low-cost, compatible microcomputers that are very competitive in the market for dedicated controllers (the primary target for GRI-99 Model 10).

The introduction of Model 50 to the GRI line has considerably expanded the series' capabilities. Model 50 is the base of GRI's System 99, a small business system. Although it seems oriented for a wider market, GRI is currently marketing System 99 to OEM manufacturers, manufacturers' software houses, and distributors. GRI currently has around 2,000 installations, including a substantial number in Europe and Japan.

USER REACTIONS

Most of GRI's users chose the systems because of their architecture, and most find the systems quite satisfactory.

Manufacturer

One of GRI's first users was a manufacturer of customized process control systems designed mostly for public utilities. The company based its system on the GRI-909 because of the bus structure, which at the time was unique. The company also has considered Lockheed's MAC 16, Honeywell's H316 and Data General's Nova; the PDP-11 was not announced until about a year later.

Table 1. GRI: Mainframe Specifications

MODEL	10	30	40	50
CENTRAL PROCESSOR				
Control Memory	No	No	No	No
Microprogrammed	No	No	No	No
No. of Registers	10	11	17	19
Max No. of Devices	9	Unlimited	Unlimited	Unlimited
Instruction Set				
Number	229	229	233	245
Floating-Point Firmware	No	Opt	Std	Std
Block Manipulation/Stack Handling	No	Opt	Std	Std
Extended Arithmetic	No	Opt	Std	Std
Consoles				
Blank Panel	Std	Opt	Opt	Opt
Operator's Console	Opt	Std	Opt	Opt
Programmer's Console (5-register display)	Opt	Opt	Std	Std
Priority Interrupt Levels	16			
Number of Addressable Devices	64			
Addressing				
Direct (no. of words)	32,768			
Indirect	1 or 2 levels			
Indexed	Yes			
MAIN STORAGE				
Type	Core			
Cycle Time (μsec)	1.76 core; 0.88 ROM			
Basic Addressable Unit	16-bit word, 8 bit byte; block on Model 40			
Bytes/Access	2			
Capacity (min/max, words)	4K-32K			
Increment Sizes (bytes)	4K; 8K			
Parity	No			
Protect	No			
ROM				
Use	Bootstraps; extension to instruction set			
Capacity	32 words			
INPUT/OUTPUT CHANNELS				
Programmed I/O (wds/sec)	80,000			
DMA				
No. of Channels	1			
Max Transfer Rate (wds/sec)	568,000			

When GRI switched to the 99 Series, this user followed suit, so that now roughly half of its 37 to 40 installations are based on the 99. The company obtains the processors and an occasional disc from GRI. This user designs the rest of the peripherals in-house and does all the programming. A programmable bus switch has been incorporated into a number of its systems, allowing redundant systems to be set up. This user likes the engineering of the GRI systems (although the grounding on the original 909 was better) and stated that GRI's support has been quite satisfactory.

Laboratory

A large laboratory on the East Coast has a 909 and a 99, both obtained because of the system's bus structure and the 16-bit word length. At the time the decision was made, the PDP-11 had not been announced, and 16-bit machines were not so prevalent. The laboratory recently obtained a second GRI system because it was quite satisfied with the performance of the first one. Also, the user had designed a number of unique interfaces and wanted to retain compatibility. Although interested in the new 99/50 processor, because it had a lot of new features they could use, this user was hesitating because the upgrade would mean that could not be maintained.

Configuration Guide

GRI-99 processors are housed in a standard 19-inch cabinet with provisions for optional feature cards. Two major firmware options and up to nine firmware or interface modules can be added to the system; six slots are included in the basic system and five more can be added within the chassis. The number of peripherals interfaced

Table 2. GRI-99 Series Peripherals

LOW-SPEED PERIPHERALS

43101 Paper Tape Reader (300 cps; requires 43100 interface)
43102 Paper Tape Punch (75 cps; requires 43100 interface)
43103 Paper Tape Reader/Punch (300/75 cps; requires 43100 interface)
43110 Card Reader 300 or 400 (80-col cpm; tabletop unit; requires 43110 interface)
43131 Printer (dot matrix; 100 cps; requires 43130 interface)
43132 Printer (dot matrix; 135 cps; requires 43130 interface)
43133 Printer (dot matrix; 270 cps; requires 43130 interface)
43134 Printer (300 lpm; 132 cols; 64-char set; requires 43130 interface)
43135 Printer (356-1,100 lpm; 132 cols; 64-char set; requires 43130 interface)
43141 Teletype 33 ASR (10 cps; 43143 interface; 43140 TTY modification)
43142 Teletype 35 ASR (heavy duty; 10 cps; requires 43143 interface)

HIGH-SPEED PERIPHERALS

43211 Grisette II Duplex Read/Write Cassette Tape System (1 drive; 50-ft, or 300-ft cassettes; needs 43210 controller)
43212 Same as 43211 (but 2 drives included)
43221 Cartridge, Disc Drive (1 removable cartridge; 1.2M wds/cartridge, 20 *u*sec latency up to 4 drives/43220 controller)
43222 Dual Cartridge Disc Drive (1 fixed, 1 removable cartridge/drive (2.4M words per drive); 20 *u*sec latency; up to 4 drives/43220 controller)
43223 Dual Cartridge Drive (like 43222 except 5.3M words/drive)

SPECIAL PERIPHERALS

43144 Display (1,600 char; 20 lines, 80 char each; requires 43145 RS232 I/O interface, up to 2,400 baud)
42400 Digital I/O Interfaces (can include 42400 gate input card with 16 unfiltered gates, general output register; 42402 binary input multiplexor with 32 lines (2 groups of 16 unfiltered input gates) per card; the 42403 binary output MUX/Relay drivers with 2 16-bit registers, 42404 binary output MUX/Logic output drivers with 2 16-bit registers for driving TTL or DTC Logic; 42405 pulse input detector for 8 inputs; 42406 10-MHz interval timer; 42407 10MHz watchdog timer with dual output that includes a contact closer and audible alarm)
42408 DMA Selector Channel (provides control for high-speed block transfers via DMA)
43300 Series Analog/Digital and Digital/Analog Conversion Equipment

Table 2. (cont.)

Unipolar Equipment (includes 43300 A/D 8-bit converter with 6.1-msec conversion at ±5V; 43301 A/D 8-bit A/D converter with 15.5-msec conversion at ±5V; 43302 10-bit converter with 13.5-msec conversion time at ±5V; 43303 10-bit A/D converter with 21-msec conversion time at ±5V; 43304 8-bit A/D converter with 15.5 *u*sec with 6.1-msec conversion time at ±10V; 43306 A/D 10-bit converter with 21-*u*sec conversion at ±10V; 43307 10-bit A/D 10-bit converter with 13.5-*u*sec conversion at ±10V; 43308 A/D 12-bit converter with 23.6-*u*sec conversion at ±10V; and 43309 12-bit A/D converter with 15-*u*sec conversion at ±10V)

Bipolar Equipment (43310 8-bit A/D converter with 15.5-*u*sec conversion at ±V; 43311 8-bit A/D converter with 21-*u*sec conversion at ±5V; 43313 10-bit A/D converter with 15.5-*u*sec conversion at ±5V; 43314 12-bit A/D converter with 23.5-*u*sec conversion at ±5V; 43315 12-bit A/D converter with 15-*u*sec conversion at ±10V; 43316 8-channel MUX; 43317 16-channel MUX; 43311 24-channel MUX; 43319 32-channel MUX; 43320 sample and hold with 5-*u*sec setting and 50-nsec aperture; and 43321 ±28V auxiliary power supply)

D/A Conversion (43322 8-bit D/A converter with 39.22 MV accuracy and ±10V range; 43323 10-bit D/A converter with 9.78 MV accuracy and ±10V range; 43324 12-bit D/A converter with 2.442 MV accuracy and ±10V range; 43325 8-bit D/A converter with 39.37 MV accuracy and ±5V range; 43326 10-bit D/A converter with 9.785 MV accuracy and ±5V range; and 43327 12-bit converter with 2.443 MV accuracy and ±5V range)

can be further expanded by attaching external I/O extension chassis with 16 more slots each. Four slots are available for memory expansion with either 4K- or 8K-word memory modules.

The power monitor/auto restart, the console-mounted autoload switch, and the operating key-lockout-security device optional features must be specified when ordering the computer. Similarly, models cannot be upgraded in the field to the next highest model number.

The following can be field-installed:
42204 Blank console with power switch.

42205 Operator's console with LED display.
42206 Programmer's console like the 42205 but with LED display of five registers.
42207 Extended arithmetic, including six registers.
42208 Byte swap pack.
42209 Byte binary pack for skip tests on equal, less than, and not equal.
42210 Six general-purpose registers.
42211/42212 Real-time clocks.
42213 Auto loader for Grisette II cassette subsystem.
42214 Teletype ROM bootstrap.
42215 High-speed reader ROM bootstrap.
42216 Custom auto loader (to 32 instructions).
42217 Power for I/O extension chassis.
42218 I/O extension chassis with 16 slots.

Consoles do not require mainframe slots. The extended arithmetic option uses both of the processor's firmware ports, and the six general-purpose registers use one (note, however, that the arithmetic option includes six registers). The byte swap pack and the 8-bit binary comparator can use either an I/O or a firmware port. All other processor options except the expansion chassis power require one I/O port.

The GRI 99/50 represents a variation from the configuring rules because it is almost a complete package. The smallest system configuration consists of one GRI 99/50 processor, 16K words of core memory, one disc unit, one line printer, and one video display terminal. In its maximum configuration, it consists of one 99/50 processor, 32K words of core memory, four disc units, five video terminals, two line printers, one 80-column card reader/punch, one 96-column card reader/punch, one reel-to-reel magnetic tape drive, and one paper tape reader/punch.

Software for the business system is bundled and includes an executive, I/O service routines, RPG II, and run-time subroutines.

COMPATIBILITY

The GRI-99 Series processors are upward-compatible from Model 10 through Models 30, 40, and 50. All use the same peripheral devices. The GRI-99 is not compatible with any other line of computers. The GRI-99 Model 50 uses some of the peripheral device addresses that are unused on other models. If a user has assigned these addresses to special-purpose devices, the 99/50 will not be upward compatible with that GRI-99 or 909 system.

MAINTENANCE AND SUPPORT

Maintenance is usually provided by the OEM customer to the end user. The OEM customer keeps a supply of spare parts and sends defective parts back to GRI for repairs. GRI supplies maintenance contracts for users in the Boston area. Raytheon services GRI computers in other areas.

GRI provides training courses in programming and maintenance at its home office throughout the year.

PRICE DATA

Model Number	Description	Purchase $(1)
	CENTRAL PROCESSOR AND WORKING STORAGE	
GRI-99	Basic Processor	
41202*	99/18 (8K words of memory)	5,115
41204*	99/38 (8K memory and operator console)	5,505
41206	99/48 (8K memory, 6 additional general-purpose registers, programmer console and floating-point firmware)	6,170
41208	99/58 (8K memory, power switch, operator panel, arithmetic operator, 10 general-purpose registers, 1 additional processor port, 3 memory ports, 4 I/O ports, 223 classes of instructions)	6,410
	Memory (1 memory port required)	
4160	8K x 16-Bit Random Access Core Memory	2,625
	Processor Options	
42200	Input/Output Port Expansion	106
42201	Power Monitor/Auto Restart	60
42202	Autoload Switch	70
42203	Operating Key Lockout	50
42205	Operator's Console	683
42206	Programmer's Console	822
42207	Extended Arithmetic Operator	575
42208	Byte Swap/Pack	140
42209	8-Bit Byte Binary	120
42210	Six General-Purpose Registers	270
42211	Real-Time Clock	205
42212	Real-Time Clock	175
42213	Autoloader for Grisette II Cassette Tape System	335
42214	ROM Bootstrap Loader (for TTY)	335
42215	ROM Bootstrap Loader (for high-speed reader)	335
42216	Custom Auto Loader	200
42217	Additional +5 vdc, 25 Amps (for use with I/O extensions)	500
42218	I/O Port Extension Chassis	975
	MASS STORAGE	
	Disc	
43220	Moving-Head Cartridge Disc Drive Controller and Interface (controls up to 4 disc drives)	4,000
43221	Moving-Head Disc Drive (1.2M words)	5,395
43222	Same as 43221 Except 2.4M-Bit Words (1 fixed, 1 removable disc)	6,530
43223	Same as 43222 Except 5.3M Words	7,475
	INPUT/OUTPUT	
	Magnetic Tape	
43211	Grisette II Full-Duplex Read/Write Tape System	1,170
43212	Grisette II Full-Duplex Read/Write Tape System (includes 2 recorders)	1,270
	Punched Card	
43111	Card Reader (300-cpm, 80-col)	3,850
43112	Card Reader (300-cpm, 80-col)	3,150
	Printers (freestanding)	
43131	100-cps Matrix Printer	3,980
43132	135-cps Matrix Printer	6,740
43133	270-cps Matrix Printer	7,980
43134	Line Printer (300-lpm, 132-col, 64-char)	11,875
43135	Line Printer (356-1, 100 lpm (zone), 132-col, 64-char)	14,850

PRICE DATA (Contd.)

Model Number	Description	Purchase $(1)
	INPUT/OUTPUT (CONTD.)	
	Teletype and Display Terminals	
43141	Teletype Model 33 ASR	1,875
43142	Teletype Model 35 ASR	4,850
43144	20 Lines, 80-Char Video Display	Factory Quote
	Paper Tape	
43101	Paper Tape Reader (300 cps)	1,830
43102	Paper Tape Punch (75 cps)	3,550
43103	Paper Tape Reader, Punch	4,695
	DATA COMMUNICATIONS	
43120	Universal Async Serial Character Input/Output Interface	383
43121	Universal Synchronous Serial Character Input/Output Interface	410
44005	Connector Contact Crimping Tool	165
44107	Arithmetic Operator	450

** Specify power requirements for other than 60 Hz, 115 vac; add $100 each unit, except for processors.*

Note:

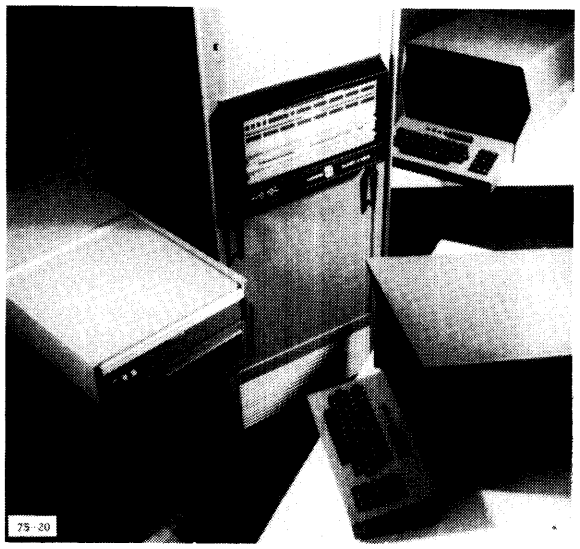
(1) Sold OEM only; quantity and OEM discounts available. Rentals not available. Maintenance not supplied by GRI except in Boston area, available through Raytheon and suppliers of end-user system.

HEADQUARTERS

GRI Computer Corp.
320 Needham Street
Newton MA 02164

HARRIS CORPORATION

Slash Series **System Report**



OVERVIEW

The Harris Slash Series consists of four computer models (Slash 1, 3, 4, and 5) manufactured by the Harris Computer Systems Division of the Harris Corporation (formerly the Datacraft Corporation) and intended primarily for high-speed, real-time, scientific applications. A fifth model (Slash 5R) is a ruggedized version designed for harsh environments. The Harris Computer Systems Division designs and sells core memory modules as well as computers. During 1974, Datacraft became a subsidiary of Harris. The Slash Series is marketed in France, West Germany, the United Kingdom, the Netherlands, and Belgium, as well as through eight offices in the United States.

Slash Series models differ from each other primarily in size, speed, and price.

Model	Cycle Time	Memory Capacity
Slash 1	0.6 microsecond	65K words
Slash 3	1.0 microsecond	65K words
Slash 4	0.75 microsecond	256K words
Slash 5	0.950 microsecond	65K words
Slash 5R	0.950 microsecond	65K words

Harris emphasizes scientific, control, and data acquisition applications, but the Slash Series is also marketed for use with communications, optical character recognition, and microfilm processing.

Harris computers are well suited for applications requiring large amounts of arithmetic calculations and fast throughput, such as the simulation of aircraft and missiles. During the past few years, the Slash Series computers have gained acceptance at several major universities where they were used in scientific and time-sharing environments under the old Datacraft 6024 Series label. The addition of Slash 4, with its memory capacity of 256K words, to the product line further extends penetration into the medium-scale computer market.

All Slash Series models are 24-bit word computers; each word can store 3 bytes. The 24-bit word length provides capabilities unavailable for the 16-bit word computers, and vies with 32-bit word machines for many applications.

The Slash 1 was announced in August 1968 as a 600-nanosecond digital computer. One year later, in December 1969, Slash 3, a reduced-speed version of Slash 1, was announced. Restricted in speed and I/O expansion, the Slash 3 processor is fully compatible with Slash 1. The Slash 5 was announced in January 1971; it is software and I/O compatible with its predecessors. Slash 5 originally featured a 1,200-nanosecond memory and was restricted to 32K words. Today, Slash 5's cycle time is 0.950-microsecond and memory capacity is 65K words. Slash 5R, a ruggedized version of Slash 5, was delivered in the first quarter of 1973. The newest addition to the line, Slash 4, was also introduced in 1973; it has a 750-nanosecond cycle time and a 256K-word memory capacity. Slash 4 is upward software- and I/O-compatible with the other systems, but virtual memory addressing prevents some Slash 4 software from running on the other models.

Slash 4 was developed in three phases. The Phase 1 system included a scientific arithmetic unit (floating point), bit processor (BP), and increased I/O capabilities. Phase 2 systems, which were delivered the third quarter of 1973, included virtual memory features with a maximum memory capacity of 256K words. Phase 3 systems, delivered during 1974, included an 8K- or 16K-word, multiple-ported semiconductor memory, 200-nanosecond cycle time, with an I/O processor interface. Phase 2 and 3 features can be easily field-installed on Phase 1 configurations. Since then, in late 1974, multiport (up to five) core memory modules have been added to the system.

Table 1 lists system specifications for each of the models.

PERFORMANCE AND COMPETITIVE POSITION

Harris occupies an almost unique position in the upper range of the minicomputer market. Its Slash Series computers use a 24-bit word while most minicomputer systems use a 16-bit word. Other notable exceptions are the Digital PDP-8 with its 12-bit word, and the Digital PDP-15 with its 18-bit word (other systems at the top of minicomputer lines are using 32-bit words, for example, Microdata 3200, Data General Eclipse, MODCOMP IV, Interdata 7/32 and 8/32, and PRIME 300). Compared with the 16-bit word, the 24-bit word places less constraint on the number of instructions that can be implemented and the number of memory locations that can be directly addressed. In addition, the precision of

Table 1. Harris Slash Series: Processor Characteristics

Model	Slash 1	Slash 3	Slash 4	Slash 5
Central Processor				
No. of Programmable Registers	5	5	5	5
No. of Instructions				
Standard	596 + SAU, BP	584 + SAU, BP	602 + SAU, BP	592
Optional	—	—	—	—
Fixed-point arithmetic				
Add/subtract	Hardware	Hardware	Hardware	Hardware
Multiply/divide	Hardware	Hardware	Hardware	Hardware
Add time (μsec)	1.2	2.0	1.5	1.9
Floating-point arithmetic	Opt hardware	Opt hardware	Opt hardware	Software
Addressing				
Direct (no. of words)	65,536*	65,536*	65,536*	65,536*
Indirect	65,536	65,536	65,536	65,536
Indexed	65,536	65,536	65,536	65,536
Max no. I/O devices	224	224	384	208
Priority Interrupt System				
Internal traps	0-7	0-7	0-7	0-7
External interrupt levels	4-72	4-24	4-48	4-24
Memory				
Type	Core	Core	Core, semiconductor	Core
Word Length (bits)	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit	24 + 1 parity bit
Cycle Time/Word (μsec)	0.6	1.0	0.75 (core), 0.20 (semiconductor)	0.950
Capacity (words)				
Max	65,536	65,536	262,124 (core), 32,768 (SC)	65,536
Min	8,192	8,192	8,192	8,192
Increments	8,192	8,192	8,192	8,192
Parity	Std	Std	Std	Std
Protect	Opt	Opt	Opt	Opt
I/O Channels				
No. of channels	14	14	24	13
No. of devices/channel	16	16	16	16
Programmed I/O channel	Std	Std	Std	Std
Direct memory access	Opt	Opt	Opt	Opt
No. of DMA channels (max)	14	14	12	13
Multiplexed I/O channel	N/A	N/A	N/A	N/A
Maximum transfer rate (words/sec)				
Within memory	416,667	250,000	333,335 (core)	263,158
Over DMA	1,666,667	1,000,000	1,333,333 per port (core) 5M per port (SC)	1,052,632

Notes:
** with special instructions*

the 24-bit word allows Slash Series computers to perform single-precision operations for many applications that require double-precision operations for a 16-bit word system.

Furthermore, each word can store 3 bytes of information. Thus, an 8K-word memory for a Slash computer can store the same amount of data as a 12K-word memory for the typical 16-bit word mini. At the same time, the Slash computers can compete with larger 32-bit word systems for certain applications.

Because Datacraft was a small company, it concentrated on producing systems primarily for real-time and scientific applications. Although the series includes five models, only Slash 4, Slash 5, and Slash 5R are actively marketed because they give the user a better price/performance than the older Slash 1 and Slash 3.

The absorption of Datacraft into the larger Harris Corporation should be a good move, allowing more room for marketing and expansion efforts. Unlike Perkin-Elmer, which acquired Interdata last year and has since allowed it to function almost autonomously, the Harris Corporation runs its Computer Systems Division. Most of Datacraft's top management is no longer with the company. The Harris Corporation has a long history of expanding through acquisition, and a computer division is a logical addition to its line of products.

Slash 4 is the workhorse of the line. It can range in size from a small system with 8K words of memory for under $25,000 to a medium-scale system with 256K words (768K bytes) of memory and a cost of several hundred thousand dollars. Slash 5 is primarily oriented toward the OEM market. Although it is available by special order in a small configuration with only 4K words of memory, it can be expanded to a rather substantial system with 64K words (192K bytes) of memory. Slash 5R is a special system that can be used for applications requiring a ruggedized system to withstand vibration and a harsh or abnormal environment.

The Slash Series competes with the Digital PDP-11/40 and 11/45, as well as PDP-15, the CDC 1700, Xerox 530, HP21MX, Interdata Models 7/32 and 8/32, Varian V73, and MODCOMP IV, PRIME 300, and Data General Eclipse. All of these systems are computers that can operate in real-time environments.

For certain applications, such as combined real-time, batch, and time-sharing, Slash 4 can also compete with the Xerox 550 and 56 and the Digital PDP-10.

The Slash 4 Virtual Memory (VM) system with its optional triple-port semiconductor memory competes most directly with the PDP-11/45 with its optional memory management system and dual-port semiconductor memory. Slash 4 has an optional I/O processor interface that can support four I/O processor channels. The PDP-11/45 with semiconductor memory can support a second PDP-11 processor. I/O transfer rate via the Slash 4 semiconductor memory can be 2.5 million words per second per channel or up to 5 million words per second for the four I/O processors interlaced. The user can connect directly to the third port of the semiconductor memory and achieve an I/O rate of 5 million words per second, provided the port is not needed for a second CPU, and the first CPU does not require access to the semiconductor memory at that time.

A number of other systems that also support virtual memory and compete with Slash 4 VM include Varian V73, PDP-11/45, MODCOMP IV, PRIME 300, and Microdata 3200.

User Reactions

Most Slash systems are used for aircraft simulation or for research projects, so a large number of systems are connected in some way to the federal government. The company has been gradually increasing its proportion of non-government users however. To date, more than 400 Slash 4 and Slash 5 systems have been installed, and Harris continues to fill orders for Slash at the rate of around 15 per year. User contacts comprised three non-government users who had either Slash 3 or 5 systems. One user is a major university that has nine systems in operation and one system on order. All users have found the systems fast and reliable, and all like the 24-bit word for data manipulation. The systems are used for such varied applications as computer network control, computer-aided instruction, data reduction from satellite, observatory management, ship-based polar exploration, batch processing, data base management, lab equipment management, data reduction from a mental retardation center, and link to MS 6000 microfilm system. Maintenance for one of the systems is provided through Singer and rated excellent. None of the users made any negative comments about the systems.

CONFIGURATION GUIDE

All Slash systems except Slash 4 VM use the same basic configuration: a Slash processor with 8K words of memory (24 bits plus 1 parity bit per word); hardware multiply, divide, and square root; priority interrupt system with four external interrupts; five registers of which three are index registers; 8-bit wide parallel I/O bus; and basic software.

The Slash 4 VM basic configuration includes memory to a total of 32K words, 120-Hz clock, stall alarm, Chain Block Controller (CBC), IOC, disc bootstrap, bit processor, CRT, 300 card-per-minute card reader, 200 line-per-minute printer, and 10.8-Megabyte disc.

Core memory can be expanded in increments of 8K words for all models. A recent addition allows core to be purchased in multiple-port (one to five ports) as well as single-port modules. In addition, up to 32K words of the Slash 4 memory can be multiple-port (up to five)) semiconductor memory with a 200-nanosecond cycle time. Maximum memory capacity is 64K words for all models except Slash 4, which has a maximum memory capacity of 256K words.

An I/O processor interface is available as an option for use with the triple-port semiconductor memory. The I/O processor interface can handle up to four I/O processors.

The following options are available:

- Program restrict and instruction trap (used with memory protect in multiprogramming environment).
- Address trap (address query, for software debugging).
- Stall alarm.
- Interval timers.
- Automatic Block Controller (ABC) for direct memory access — up to 16 devices can interface to each ABC unit.
- Priority interrupt levels — up to a maximum of 24 levels for Slash 5, 24 for Slash 3, 48 for Slash 4, and 72 for Slash 1.
- Bit Processor (BP) — to retrieve or store bits within a word in memory (not available for Slash 5 or Slash 5R).
- Scientific arithmetic unit — provides floating-point arithmetic (not available for Slash 5 or Slash 5R).
- Hardware bootstrap units for paper tape, card reader, disc, and magnetic tape.
- Additional I/O channels — 8-bit wide channel with up to three integral controllers, dual 8-bit wide channel, 24-bit wide channel — for a maximum of 14 channels for Slash 1; 24 channels for Slash 4; and 13 for Slash 5.

Of these channels, 14 can support DMA channels (ABC units) for all models except the Slash 4, which can support 12 DMA channels, and the Slash 5, which can support 13 channels.

All models use the same peripheral devices. Mass storage devices include fixed-head disc units, moving-head disc packs, and disc cartridges. Conventional peripherals include Teletype ASR and KSR 33, 35, and 38;

paper-tape reader and punch; card reader; card reader/punch; card punch/keypunch/verifier/interpreter and magnetic tape drives. Two drum plotters can also be interfaced: one uses a 12-inch drum and the other a 30-inch drum. Data communications facilities include a synchronous interface for transmission at 1,200 to 9,600 baud, an asynchronous interface for transmission at 112.5 to 9,600 baud, and a multiplexor that can connect to eight synchronous or 16 asynchronous units via line interface units. Table 2 summarizes the specifications for these peripherals.

The basic software package for the Slash computers includes a Resident Operating System (ROS), macro assembler, FORTRAN support library, utility package hardware diagnostics, and cross-reference package. If magnetic tape is included in the configuration, a Tape Operating System (TOS) is used instead of ROS. For disc systems, the Disc Operating System (DOS II) or Disc Monitor System (DMS) controls system operation. DMS supports real-time processing, time sharing, interactive terminals, and batch processing. FORTRAN IV, RPG, BASIC, Forgo (FORTRAN Compile and Go compiler), and Snobol can run under DOS II or DMS. In addition, FORTRAN IV and Forgo can run under ROS or TOS. Slash 4 can run under VULCAN, a disc-based, virtual memory system. Configuration requirements for the major software packages are listed in Table 3.

Table 2. Harris Slash Series: Peripherals

Device	Description
Terminals	
2100 Series	ASR, KSR 33/35/38 Teletypes, 10 cps
2300 and 8600 Series	CRT displays 24 lines, 80 char
2200 Series	Silent 700 terminals
Punched Cards	
3010/20/30	330/600/1,000-cpm readers.
3200	500-cpm reader, 100-cpm punch
3300	Keyboard/verifier/punch, 3172 interprets, 35 cpm
Punched Tape	
2005/2020	300-cps readers
2010	75-cps punches
2030	75-cps punches
2015	300-cps reader, 75-cps punch
Printers	
4030/4040	200-lpm line printers
4050/60/70	400/600/1,000-lpm line printers
4700 Series	Printer-plotters, 300-1,200 lpm
Magnetic Tape	
6660/70	9-track, 800/1,600 bpi, 75 ips
6040/50/60	9-track, 800 & 1,600 bpi, 100/150/200 ips
6210/20/30	7-track, 556 & 800 bpi, 100/150/200 ips
6630	7-track, 550 or 800 bpi, 45 ips
6640	9-track, 800 bpi, 45 ips
6650	9-track, 1,600 bpi PE, 45 ips
Discs	
5120/5130	Moving-head discs, 28/56M capacity
5230-5260	Moving-head cartridge discs, 2.7/10.8 capacity
5420/40/70	Fixed discs, 430Kb/860Kb/2,150Kb capacities
5500 Series	Disc pack subsystem, 40M bytes/pack
Process I/O	
9400	Analog/digital subsystem, to 128 channels, A/D, D/A, digital and high-level analog input systems
Communications	
9031MUX	Up to 16 async, 8 sync lines or 2/1 combination
9010	Synchronous controller, 1,200-9,600 baud
9020/1/4	Asynchronous controller, 112.5-9,600 baud

COMPATIBILITY

All models except Slash 4 are completely compatible. Slash 4 is software- and I/O-compatible with other Slash systems except for the optional paging scheme (virtual memory configuration) for systems with more than 64K words of memory. The Slash 4 is upward software-compatible with the other models.

MAINTENANCE

Harris supplies contracts for prime-shift, two-shift, or three-shift maintenance. Preventive maintenance and

Table 3. Harris Slash Series: Software

Package	Description
DMS	Disc Monitor System, a foreground multiprogramming system with a background batch processing capability; requires console, binary input device (2), 24K words of memory for minimum system
VULCAN	Virtual Memory Operating System, disc-based; requires 32K words of memory, Slash 4 VMS configuration, console must be CRT, disc, magnetic tape
DOS	Disc Operating System; uses a disc loader and utilizes a nonresident service area to bring in required modules; requires binary input device*, 8K words for minimum system
TOS	Tape Operating System; uses a magnetic tape loader, console, 3.5K words for op system, 8K words for minimum system
ROS	Core Resident Operating System; uses a paper-tape or card I/O loader and requires 3,500 locations plus I/O areas, console; minimum system requires 8K-word memory
FORTRAN IV	FORTRAN IV compiler, a superset of ANSI FORTRAN IV; requires 4,600 + N locations (N = size of the data pool); needs 8K words above operating system, except DMS or Vulcan
FORGO	Forgo Compiler (Load and Go FORTRAN) provides extensive debugging features; needs 8K words above minimum DOS/TOS/ROS, no extra needed for DMS or Vulcan.

Table 3.

Package	Description
RPG	RPG II; 8K above TOS or DOS, no extra memory needed for DMS or Vulcan
BASIC	Dartmouth BASIC for user; only available with DMS or Vulcan; no extra memory needed
SNOBOL	Snobol; character string manipulation language including compiler, interpreter, and storage allocation, needs 48K words of memory under DMS, TOS, DOS; no extra under Vulcan
MACRO	Assembler; requires 3,100 + N locations (N = size of symbol table); available in MACRO form when more than 8K system; otherwise use Basic Assembler
UTILITIES	FORTRAN support library, including single- and double-precision floating-point routines; utility package provides system software support routines that are not resident in core (source update, etc.); SORT/MERGE, indexed sequential, editor, cross-reference program, hardware diagnostics, object time trace, an interactive, program debugging aid.

Note: All software is available at no charge. The appropriate operating system is provided to meet the system configuration. Source software is subject to extra charges.
* Paper tape, magnetic tape, punched card

emergency calls during the contracted shift(s) are performed for a monthly fee. Harris can also supply a dedicated on-site service engineer on a contractual basis. If the user does not want a contract, service is available on a per-hour basis (4 hours minimum) plus expenses, or parts can be shipped to the Florida factory via the nearest service center.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS & WORKING STORAGE		
	Systems		
VM 1	Small Time-Share/Real-Time/Batch System (includes Slash 4 VMS, 10.8-MByte cartridge disc, 200-lpm printer, 300-lpm communications multiplexor, 3 dual async line interface units, 6 TTY replacement CRTs, and 19-inch peripherals cabinet)	126,500	1,175
VM 2	Medium Time-Share/Real-Time/Batch System (includes Slash 4 VMS, additional 96K bytes of core memory, 40-MByte disc, 400-lpm printer, 600-cpm card reader, 2 MTU, vacuum, 45 ips, 9T, 800/1,600 bpi, communications multiplexor, 4 dual async line interface units, 8 CRTs, TTY replacement, and 19-inch peripherals cabinet)	225,000	2,125
	System Options		
425	Run Time Meter	—	—
463	Multi-CPU Channel Adapter (8-bit)	950	10
464	Multi-CPU Channel Adapter (24-bit)	1,350	10
465	Multi-CPU Channel Adapter (CBC)	2,450	15
403	Multiport Core Memory (8K) (1st 8K)	12,000	70
404	Additional 8K MPC	7,000	40
485	Additional MPC Port	1,500	10
486	Custom MPC Interface	1,500	10
434	1K-Hz Real-Time Clock	1,500	10
487	Additional SCM CPU-Port	3,000	25
	Central Processors		
Slash 1	CPU with 24K bytes of core memory (600 nsec cycle time)	85,000	510
Slash 3	Same as Slash 1 except memory has 1.0 μsec cycle time	65,000	390
Slash 4	CPU with 24K bytes of core memory (750-nsec cycle time)	24,000	125
Slash 4 VMS	CPU with 96KBytes, scientific arithmetic unit, memory parity, 120-Hz clock, stall alarm, bit processor, disc bootstrap, CRT channel (8-bit IOC/IC), card reader/line printer channel (24-bit IOC), disc channel (CBC), 8 priority interrupts, CRT operator's console, VULCAN (VMS operating system), software processors and system utility software package	76,500	525
Slash 5	Same as Slash 4 except 950-nsec cycle time	16,500	100
Slash 5R	Same as Slash 5 except choice of either XBC or ABC and basic software (Available only by special order with prior confirmation from Harris Data Systems home office)	65,000	600
	Slash 1 and Slash 3		
101	24KByte Memory Increment for Slash 1	45,000	270
301	24KByte Memory Increment for Slash 3	29,500	180
116/316	Program Restrict and Instruction Trap	1,375	10
117/317	Stall Alarm	1,075	10
118/318	Interval Timer	1,370	10
119/319	Power Fail Shutdown and Restart	1,250	10
120/320	Address Trap	1,075	10
146/346	Automatic Block Controller (I/O channel for up to 16 units)	2,750	20
150/350	Priority Interrupts (4 levels)	1,075	10
124/324	Bit Processor	3,600	20
115/315	Scientific Arithmetic Unit	27,000	165
126/326	Hardware Bootstrap Unit		
	First Unit	1,370	10
	Each Additional Unit	1,075	10
152/352	Software Controlled Interrupt	500	10
175/375	CPU Memory Expansion Rack (holds 49,152 words of core, I/O channel chassis, and blower and logic power)	3,600	NC
	Slash 4, Slash 4VMS, Slash 5 option		
401	24KByte Memory Increment	7,000	40
409	24KByte Semiconductor Memory, Multiport (150-nsec cycle time)	26,750	160
410	Second 24KByte Semiconductor Memory	22,500	135
516/416	Program Restrict and Instruction Trap	1,000	10
517/417	Stall Alarm	650	10
518/418	Interval Timer	750	10
519/419	Power Fail Safe and Restart	500	10
420/520	Address Trap	650	10
447	Chain Block Control (I/O Channel for up to 16 units)	2,200	20
450/550	Priority Interrupt (1 level)	150	10
415	Scientific Arithmetic Unit	9,900	60
426/71/81	Hardware Bootstrap Units	750	10
436/7/8/9	Additional Bootstrap Units	250	10
452	Interrupt Generator	300	10
455	I/O Processor (for dual-port semiconductor memory)	3,500	25
TBD	Additional I/O Processor	TBD	
488	High-Speed Interface to SCM	3,000	20
461	ABC Link Cable	1,250	10
460	Computer Link Option	6,000	40
451	Priority Interrupt Expander (beyond 24 levels)	1,250	10
470	16K-Word Memory Expansion (beyond 65K words)	7,500	45
	Slash 5 Options		
501	24KByte Memory Increment	5,000	30
526/719	Hardware Bootstrap Unit	750	10
536/7/8/9	Additional Bootstrap Units	165	10
552	Interrupt Generator	300	10
561	ABC Link Cable	1,250	10
529S	Computer Link Option	5,750	35
570	Memory Expansion Chassis	3,500	20
572	I/O Expansion Chassis	3,500	20
	Slash 5R Options		
501R	24KByte Memory Increment	8,500	85
516R	Program Restrict and Instruction Trap	1,350	15
517R	Stall Alarm	1,200	15
518R	Interval Timer	1,350	15
519R	Power Fail Safe and Restart	1,000	10
520R	Address Trap	1,200	10
550R	Priority Interrupt (1 level)	500	10
526R/7R/8R/9R	Hardware Bootstrap Unit	1,300	15
536R/7R/8R/9R	Additional Bootstrap Units	900	10
552R	Interrupt Generator	500	10
561R	ABC Link Cable	1,500	15
570R	Memory Expansion (beyond 32K words; 16K words)	35,000	350
	MASS STORAGE		
	Cartridge Disc (CDC)		
5230	Cartridge Disc with Controller (2.7 mb, single platter)	10,900	130

PRICE DATA (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
5260	Cartridge Disc with Controller (10.8 mb, double platter)	12,900	155
5265	Cartridge Disc Platter (2.7 mb)	500	NC
5231	Additional Cartridge Disc Unit (2.7 mb, single platter)	8,000	100
5261	Additional Cartridge Disc Unit (10.8 mb, double platter)	10,000	120
	Moving-Head Disc (ISS)		
5120	Moving-Head Disc and Controller (28 mb)	30,000	360
5130	Moving-Head Disc and Controller (56 mb)	37,500	450
5121	Additional Moving-Head Disc Unit (28 mb)	22,500	270
5131	Additional Moving-Head Disc Unit (56 mb)	25,500	450
5135	Disc Pack (28 mb or 56 mb)	1,000	NC
	Fixed-Head Disc (DD)		
5404	Fixed-Head Disc and Controller (107 kb)	10,300	100
5406	5404 with 215 kb	11,100	115
5420	5404 with 430 kb	30,000	360
5440	5404 with 860 kb	40,000	480
5470	5404 with 2,150 kb	67,500	810
5415	5404 with 4,300 kb	32,500	490
5424	Additional Fixed-Head Disc Unit (107 kb)	5,800	65
5426	2424 with 215 kb	6,600	80
5421	2424 with 430 kb	20,000	240
5441	2424 with 860 kb	30,000	360
5471	2424 with 2,150 kb	57,500	690
5435	2424 with 4,300 kb	28,000	460
5500	Storage Module Drive with Controller (40Mbyte)	28,100	305
5510	Additional Storage Module Drive	17,100	210
5520	Storage Module Pac	750	NA
5410	FHD 268 kb w/Controller	25,000	300
5430	FHD 587 kb w/Controller	35,000	420
5450	FHD 1,075 kb w/Controller	45,000	540
5460	FHD 1,720 kb w/Controller	60,000	720
5411	268 kb FHD Add-On	15,000	180
5431	587 kb FHD Add-On	25,000	300
5451	1,075 kb FHD Add-On	35,000	420
5461	1,720 kb FHD Add-On	50,000	600
	INPUT/OUTPUT		
	I/O Interfaces with Slash 1 and Slash 3		
141/341	8-Bit Channel	1,370	10
142/342	16-Bit Channel Expander	1,075	10
143/343	24-Bit Channel	1,750	10
146/346	Automatic Block Controller	2,750	20
121/321	120-Hz Clock	300	10
	With Slash 4 and Slash 5		
421/521	120-Hz Clock	150	10
448/548	External Block Controller (XBC)	2,000	10
441/541	9-Bit Channel	650	10
442/542	Dual 8-Bit Channel	1,250	10
443/543	24-Bit Channel	1,200	10
445/545	8-Bit Channel/Integrated Controller	750	10
	With Slash 5		
546	Automatic Block Controller	2,000	15
	With Slash 5R		
546R	Automatic Block Controller	3,000	30
521R	120-Hz Clock	400	10
548R	External Block Controller	2,600	25
541R	8-Bit Channel	1,500	15
542R	Dual 8-Bit Channel	2,250	10
543R	24-Bit Channel	2,000	20
545R	8-Bit Channel/Integrated Controller	1,500	10
	Terminals		
2110	Teletype Model ASR 33 and Controller	2,500	50
2115	Teletype Controller (serial)	600	10
2130	Teletype Model ASR 33	2,100	50
2150	Teletype Model ASR 35	6,500	80
2140	Teletype Model KSR 33	1,900	35
2160	Teletype Model KSR 35	4,000	50
2180	Teletype Model ASR 38	2,750	35
2190	Teletype Model KSR 38	2,400	30
2220	733 KSR (Console)	4,000	50
2170	RO 35 Unit Only	TBD	TBD
8530	TTY ASR 33 for MUX	2,100	50
8540	TTY KSR 33 for MUX	1,900	35
8550	TTY ASR 35 for MUX	6,500	80
8560	TTY KSR 35 for MUX	4,000	50
8570	TTY RO 35 for MUX	TBD	TBD
8580	TTY ASR 38 for MUX	2,750	35
8590	TTY KSR 38 for MUX	2,400	30
	Paper Tape		
2010	Paper Tape Reader and Controller (300 cps)	2,500	30
2020	Paper Tape Punch and Controller (76 cps)	3,500	40
2030	Paper Tape Reader/Punch and Controller (300/75 cps)	5,750	75
2070	Spooler	2,000	25
2040	Paper Tape Reader (with spooler and controller; 300 cps)	3,500	45
2060	Paper Tape Punch (with spooler and controller; 75 cps)	4,500	60
2015	Same as 2010 w/fanfold	3,000	40
2025	Same as 2020 w/fanfold	4,000	50
2035	Same as 2030 w/fanfold	6,250	80
2050	Same as 2040, 7-1/4 inches	4,000	50
	Printer/Plotter		
4710	11 inch size, 500 lpm print, 1.2 ips plot, simultaneous print/plot, 96 char, 123 cols, 1,024 nibs	15,000	180
4720	Same as 4710, except 1,200 lpm print and 3 ips plot	16,500	200
4725	Paper Winder for Models 4710 or 4720	500	10
4730	20 inch size, 300 lpm print, 75 ips plot, simultaneous print/plot, 96 char, 232 cols, 1,856 nibs	17,500	210
4740	Same as 4730, except 1,200 lpm print and 3 ips plot	20,000	240
4745	Paper Winder for Models 4730 or 4740	600	10
	Card Equipment (includes controller)		
3010	Card Reader (300 cpm)	5,000	65
3020	Card Reader (600 cpm)	7,500	100
3030	Card Reader (1,000 cpm)	10,000	135
3160	Card Reader/Punch (500/100 cpm)	26,000	200
3170	Card Punch/Keypunch/Verifier (35 cpm)	11,500	145
3172	Card Punch/Keypunch/Verifier/Interpreter (35 cpm)	14,500	180
	Line Printers		
4030	Line Printer and 8-Bit Controller (200 lpm)	12,500	150
4040	Line Printer and 24-Bit Controller (200 lpm)	15,000	180
4050	Line Printer and 24-Bit Controller (400 lpm)	20,000	240
4060	Line Printer and 24-Bit Controller (600 lpm)	26,500	320
4070	Line Printer and 24-Bit Controller (1,000 lpm)	60,000	720
	Magnetic Tape		
6295	Option to Add Drives 3 and 4 9-track 800/1,600 bpi	3,000	15
6240	Magnetic Tape Unit and Controller (PE/NRZI; 100 ips)	31,000	440
6250	Magnetic Tape Unit and Controller (PE/NRZI; 150 ips)	44,000	550
6260	Magnetic Tape Unit and Controller (PE/NRZI; 200 ips)	48,000	530
6241	Additional Tape Unit (PE/NRZI; 100 ips)	25,000	300
6251	Additional Tape Unit (PE/NRZI; 150 ips)	2,900	350
6261	Additional Tape Unit (PE/NRZI; 200 ips) 7-track, 556/800 bpi	3,300	400
6210	Magnetic Tape Unit and Controller (100 ips)	3,800	415
6220	Magnetic Tape Unit and Controller (150 ips)	42,000	460
6230	Magnetic Tape Unit and Controller (200 ips)	46,000	505
6211	Additional Tape Unit (100 ips)	23,000	275
6221	Additional Tape Unit (150 ips)	27,000	325
6231	Additional Tape Unit (200 ips)	31,000	370
6630	MTU and Controller (for up to 4 drives, 45 ips, 7T, 800/556 bpi, tension arm)	11,000	135
6631	Additional MTU	7,000	90
6640	Same as 6630 except 9T, 800 bpi	12,000	145
6641	Additional MTU	8,000	100
6650	Same as 6640 except 1,600 bpi (PE)	16,000	195
6651	Additional MTU	10,000	120
6660	Same as 6650 except 800/1,600 bpi, vacuum col	19,000	230
6661	Additional MTU	12,000	150
6670	Same as 6660 except 75 ips	25,000	300
6671	Additional MTU	17,000	210
	CRT Display Units		
2310	Interactive CRT (24 lines, 80 char, TEC 425, with keyboard w/interface)	5,500	60
8610	CRT without Controller	4,150	55
2320	TTY Replacement CRT	3,200	35
2315	2310 w/Hard-Copy Device	9,000	110
2325	2320 w/Hard-Copy Device	6,700	85
8620	CRT without Controller (440 Model; used with 9022)	2,850	45
9022	Equipment Stand (for remote CRT)	2,500	15
7540	Equipment Stand (for local CRT)	750	NC
8610	Interactive CRT Terminal	5,150	55
8615	8610 w/Hard-Copy Unit	8,650	110
8620	TTY Replacement CRT Terminal	2,850	45
8625	8620 w/Hard-Copy Unit	7,350	100
8710	ASR-33 Terminal	4,500	55
8720	KSR-733 Terminal	3,500	45
	DATA COMMUNICATIONS		
8120-2	Modem Interface to IOC/IC	1,000	10
8130-2	Modem Interface (async)	2,500	15
8140-2	Modem Interface (async)	3,000	20
8340-2	Dual ASR/KSR 733 Terminal Interface	850	10
8110	Sync Controller (W/O cabinet)	2,500	15
8120-1	Async Controller	1,000	10
8130	Async Controller (mounts in 19-inch rack)	2,500	15
8140	Async Controller (mounts in 24-inch rack)	3,000	20
8310	Communications Multiplexor	3,000	35
8340-1	Dual Async Line Interface Unit	750	10
8330	Sync Line Interface Unit	1,200	15
	UNIVERSAL INTERFACES		
7310	Remote Integral Controller Interface (up to 3 standard IOC/IC controllers)	2,000	10
7600	Wire Wrap Interfaces for Customer-Designed Interfaces	—	—
8350-1	Dual Async Line Interface Unit, including cables, for Datacraft-modified 33 or 35 TTY connections to multiplexor	750	10

PRICE DATA (Contd.)

8350-2	Same as 8350-1 except no reader control	750	10
8360	For Datacraft-modified CRT connections to multiplexor	750	10
8370	For Datacraft Model 2200 Series terminal connections to multiplexor	850	10
8380	For RS232C-compatible terminals and/or Series 38 TTY connections to multiplexor	750	10
8320	Synchronous Line Interface Unit, including cables, for 301 modem connections to multiplexor, to 40.8Kbps	2,000	15
	I/O Cables for Slash 4, Slash 5		
7450	Cable Assembly (8-bit) (80-pin card edge connector to 75-pin rack connector (female) for use with Slash 1, Slash 3 peripherals)	500	10
7451	Cable Assembly (16-bit) (male)	500	10
7460	Cable Assembly (8-bit) (male; for connecting Slash 4, Slash 5 peripherals to Slash 1, Slash 3)	500	10
7461	Cable Assembly (16-bit) (female)	500	10
7470	Cable Assembly (8-bit) (80-pin card edge connector to 80-pin rack connector)	300	10
	Software		
6100	BASIC Software Package	NC	
6110	FORTRAN IV Compiler	800	—
6112	Forgo Compiler	800	—
6115	FORTRAN IV/Forgo Compilers	1,000	—
6120	Disc Operating System (DOS II)	750	—
6130	Object Time Trace	200	—
6145	SNOBOL	400	—
6150	Disc Monitor System (DMS)	2,500	—
6160	RPG	600	—
6170	BASIC	500	—

*DC — Slash 4 & 5 only
TBD — To Be Determined
— Not Applicable
NC No Charge

Note:

(1) Buy out and term leases are available. Monthly maintenance prices are per unit. Combinations and quantity buys are subject to discount and require a home office quote.

HEADQUARTERS

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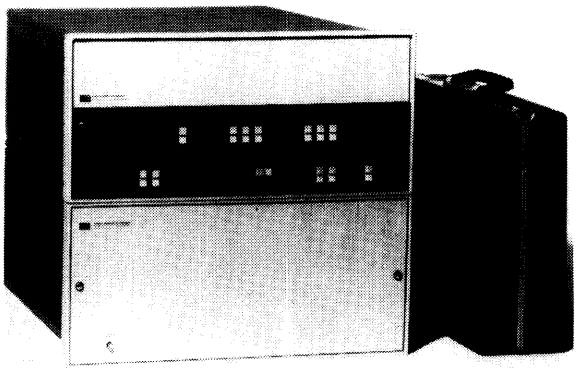
HEWLETT-PACKARD

HP 21MX System



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OVERVIEW

The HP21MX is Hewlett-Packard's latest implementation of its popular 2100 Series of computers. The 21MX is completely upward compatible with the 2100. Virtually all 2100 software can be used on the 21MX, and all 2100 peripherals can interface with the 21MX I/O channels. Features of the 21MX Series include microprogramming ability, semiconductor memories, and a potential address space of 1 million words. The system is intended for both OEM and end-user markets.

The 21MX series initially consists of two models: M/10 or HP 2105A and M/20 or HP 2108A. The M/10 is the smaller of the two models, differing from the M/20 primarily in memory capacity and in control store and I/O expandability.

The central processors provide 128 instructions in the standard set; 80 that emulate the HP 2100 Series, 42 that implement indexing, bit and byte manipulation, and byte and word moves, plus six that perform floating-point arithmetic. The instruction set implemented by microprogrammed firmware is supplied on four ROM modules of 256 locations each. Maximum control store capacity is 4,096 24-bit words. Additionally, writable control store RAMs are optionally available. Each module supplies 256 24-bit locations. The microprocessor instruction set includes 178 microinstructions.

Main memory consists of N-channel MOS semiconductor modules with a cycle time of 650 nanoseconds. Memory parity generation and checking are standard, and memory protect is optional.

Special power failure and brownout protection is standard, providing for memory integrity through a line loss of 10 Hz. Optional stand-by battery power is available to maintain 32K words of memory for two hours if a total power failure occurs. A direct memory access option for two channels is available for high-speed devices.

The system logically structures memory into 1K pages. Through a variety of addressing techniques (direct, indirect, indexing) any location in memory can be addressed.

The optional Dynamic Mapping System (DMS) provides techniques for expanding the system's physical address space to 1 million words. It supplies four sets of 32 registers each — two sets for mapping user and operating system and two sets for data control, permitting scatter/gather I/O operations. The DMS is available only on the M/20. A memory protect feature is included, which supplies both a programmable fence register and page oriented read/write protect.

The 21MX provides 60 levels of chained priority interrupt. The 2105A has four standard I/O channels, and the 2108A has nine standard channels. Both models can expand I/O capacity by 34 channels in increments of 17. The channels support a wide range of high- and low-speed peripherals, TTY and CRT terminals, plus special-purpose gear.

The systems are designed to withstand the same shocks and vibrations as HP's electronic instruments, and are protected against extremely high voltages. They will function in a temperature range of 0° to 55° Centigrade.

Software is provided to perform batch operations, multiprogramming, foreground/background processing, remote job entry, time sharing, and real-time processing. The system supports an assembly language system, FORTRAN, FORTRAN IV, BASIC, and ALGOL. Additionally, a terminal control system for data communications is available, plus a data base management system and over 1,000 canned programs and microcoded routines.

First customer deliveries were made in June 1974.

COMPETITIVE POSITION

The HP 21MX Series extends the processing capability of a popular line of minicomputers; over 9,000 HP 2100 systems have been installed. The series utilizes modern technology — all semiconductor memory, for example — to provide systems that are smaller, weigh less, consume less power, and cost less than the earlier 2100 systems. Almost all major minicomputer manufacturers are following this same route to modernize their computer lines.

In contrast to Interdata and MODCOMP, which use a 32-bit word for their top-of-the-line systems, Hewlett-Packard has kept the 16-bit word but has incorporated the ability to extend the power of its systems substantially by the simple expedient of adding larger memory capacity and a memory management unit, which generates 20-bit addresses. This allows addressing of 1,048,576 words of physical memory. The feature also provides significant hardware/software control over program and data page allocation with no impact on system cycle time.

The 21MX has a large 4K-word control memory which allows for a fairly broad set of microcoded user

application oriented routines. In the earlier 2100 series, a more limited control store provided throughput improvement over conventional programmed instructions of 10 to 50 times for some applications. Thus, increases of even greater magnitude can also be expected from the 21MX.

Major competition for the HP 21MX will be the Data General Nova/Supernova and ECLIPSE Varian V70 Series, Interdata 7/16 and 7/32, and the DEC PDP-11. Primarily due to its orientation to instrumentation, Hewlett-Packard has generally provided more application-oriented packages than other minicomputer manufacturers.

As processors continue to provide more and more power and performance for less and less money, and plug-compatible peripherals proliferate, minicomputer manufacturers must take the problem-solving system approach to marketing. Less sophisticated users want easy-to-use systems that do a job. This means manufacturers must provide application-oriented systems that can be easily customized for a specific job.

Hewlett-Packard has taken this approach previously with its time-sharing, test and measurement, and distributed processing systems, and is currently expanding it with its data base management and remote job entry systems. The same approach is being followed with the 21MX with its comprehensive range of software including seven operating systems, four languages, special-purpose processors such as data base management and query system and remote job entry, plus an extensive application program library.

The 21MX must be considered a major and serious entry into the minicomputer arena, and it should prove to be the prime contender in many competitive procurements.

MAINTENANCE AND SUPPORT

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world, including 60 service facilities in the United States and Canada backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides for full services, parts, and labor for 90 days. Follow-on agreements can provide for either guaranteed response times and full service or a per-call time and materials service.

CONFIGURATION GUIDE

A minimal 21MX configuration consists of a mainframe and 4,096 words of semiconductor memory. Peripherals can be added to the basic configuration, depending on the requirements of the user. Mainframe characteristics are given in Table 1. A complete list of available peripheral devices is supplied in Table 2.

Table 1. Hewlett-Packard 21MX: Mainframe Characteristics

Type	2105A Micro-programmed	2108A Micro-programmed
CENTRAL PROCESSOR		
Control Memory	Yes	Yes
Size	1,024 (24 bits)	1,024 (24 bits)
Use	Firmware	Firmware
No. of Internal Registers	9; additional 16 at micro level	9; additional 16 at micro level
Addressing		
Direct	2,048	2,048
Indirect	Multilevel; 32,768	Multilevel; 32,768
Indexed	Yes	Yes
Instruction Set		
Implementation	Firmware	Firmware
Number (std; opt)	128; 38; 178 micro-instr	128; 38; 178 micro-instr
Decimal Arithmetic	No	No
Floating-Point Arithmetic	Yes, firmware	Yes, firmware
User Micro-programming	Yes	Yes
Priority Interrupt System Levels	60	60
MAIN STORAGE		
Type	SC	SC
Cycle Time (μsec)	0.650	0.650
Basic Addressable Unit	Wd (16-bit)	Wd (16-bit)
Bytes/Access	2	2
Cache Memory		
Min Capacity (bytes)	8,192	8,192
Max Capacity (bytes)	65,563	393,216
Increment Size (bytes)	8K; 16K; 32K	8K; 16K; 32K
Ports/Module	1	1
Error Checks	Parity	Parity
Protection Method	No	Fence reg
Memory Management	No	Opt
ROM	Yes	Yes
Use	Control storage Firmware; loaders	Control storage Firmware; loaders
Capacity	1,024 (24-bit)	1,024 (24-bit)
RAM	Opt	Opt
Use	Writable control Store (WCS)	Writable control Store (WCS)
Capacity	256 (24-bit)	512 (24-bit)
I/O CHANNELS		
Programmed I/O	Yes	Yes
DMA Channels	2	2
Multiplexed I/O (no. subchannels)	4; 32	9; 32
Max Transfer Rate (wd/sec)		
Over DMA	616,666	616,666
Simultaneous Operation	Yes	Yes

Table 2. Hewlett-Packard 21MX: Peripherals

DEVICE MODEL NO.	DESCRIPTION
Discs	All Models Moving Head
12960A	Cartridge, 1 removable, 1 fixed; sectored 2.5M wds, 47.5 access time, xfer rate 126 kws
12961A	Same as 12960A except contain only 1 removable platter
12965A	Pack, 11.776M wds/pack, 32 msec access, xfer rate 155 kw/s
Magnetic Tape	
12971A	7-trk, 200/556/800 bpi, 25/37/45 ips
12970A	9-trk, 800 bpi, 25/37/45 ips
12972A	9-trk, 1,600 bpi, 25/37/45 ips
Console	
(listed under Terminals)	
Paper Tape	
12925A	Pchd PT reader, 500 cps
12926A	Tape punch, 75 cps
12927A	Tape punch, 120 cps
Punched Card	
12986A	Optical mark reader, 200 cpm
12985A	Card reader, 600 cpm
Line Printers	
12980A	200 lpm, 132 cols, 64-char set
12980A-001	150 lpm, 132 cols, 96-char set
12984A	300-1, 100 lpm, 80 cols, 64-char set
12982A	600 lpm, 132 cols, 64-char set
12982A-001	400 lpm, 132 cols, 96-char set
12987A	200 lpm, 132 cols, ROM customized char set
Displays	
7210A	Digital plotter, 20 vctrs/sec
7202A (also see under Terminals)	Graphic plotter, 2 vctrs/sec, 10/15/30 cps
A/D Subsystems	
12604A	Data source interface, 32 lines
D/A Subsystems	
12555B	D/A converter, 2 chan, 8 bits/chan
12597A	Duplex register, 8-bit, 48-pin
12566B	Micro-circuit duplex register, 16-bit, 48-pin
12930A	Universal interface, 16-bit
Digital I/O	
12539C	Clock, crystal bases (0.1ms to 1,000 sec Interval)
Data Communications	
12587B	Async data set interface (45-2, 400 bps)
12618B	T/R sync data set interface (9,600 bps)
12589A	Automatic calling unit interface
12531C/D	Async terminal interface (110-2, 400 bps)
12920A	Async multiplexor; 16 dev interfaces, 57-2, 400 baud
12880A	TTY or CRT channel, local or remote, buff/unbuff (110-2, 400 bps)
Terminals Supported	
2754A	TTY ASR 33 (10 cps)
2754B	Heavy-duty TTY ASR 35, (10 cps)
2762A	Term console printer KSR (35 cps, 75 cols)
2762A-006	Term printer KSR (30 cps, 118 cols)
2615A	Char mods CRT buffer 2,000 char
2616A	Pg mode CRT (stores/ 256 25 x 80 pgs)

Users operating under control of any of the operating systems described in Table 3 require (as a minimum) a paper tape reader, a console device such as a TTY, and the system device for the operating system, such as magnetic tape or disc. Beyond these limitations, the user is relatively free to expand the system up to the maximum memory capacity and maximum number of I/O channels — currently 196K words of memory with a potential for 1 million words, and up to 54 directly addressable devices.

The system's basic control memory provides for a maximum of 4,096 words of addressable ROM, the bulk of which is available to the user. In addition, a user can optionally add one (M/10) or two (M/20) modules of writable control store RAM (256 24-bit locations). Both the ROM and RAM facilities provide the user with extremely powerful implementation tools.

The 21MX Series is also available in several preconfigured versions at considerably reduced costs. The M/200 line is oriented towards a business environment;

Table 3. Hewlett-Packard 21MX: Software

PACKAGE NAME	DESCRIPTION
Basic Control System (BCS)	Executive monitor providing load, interrupt processing, and I/O drives; memory resident on min system; min config
Magnetic Tape System (MTS)	Batch processing; tape resident; can be used on single tape system; provides job control directives and executive functions
Disc Operating System-III (DOS-III)	Disc-resident batch processor; std executive function plus logical file mgmt and appl prog segmentation; 4,500 wds main mem; 400K bytes disc
Real-Time Executive (RTE)	Core or disc-resident; multi-programming, foreground/ background processing; prior prog sched; min config 16K
Time-Sharing System	Extended BASIC interpreter; up to 32 terminals
Language Processors	ASSEMBLY; FORTRAN; FORTRAN IV; BASIC; ALGOL
Special-Purpose IMAGE/2000	DBMS; allows structured data network; query and batch modes; uses min 5.5K memory, 300K bytes disc; will run under DOS-III
Remote Job Entry (RJE)	Remote job interface to OS360; will run under DOS-III
Terminal Control System (TCS)	Multitasking supervisor; up to 32 terminals; requires 6.5 memory
Applications Various	More than 1,000 applications-oriented macro and microcoded routines

the S/200 Series favors a scientific/engineering environment. Both packages provide highly sophisticated levels of data processing. The 21MX/55, a special disc-based configuration, is available for the OEM shop; it is based on M/20 with 32K words of high-density memory and includes 4.9 million bytes of disc cartridge storage.

The 21MX Series also provides facilities for data communication and time-sharing services. As noted in Tables 2 and 3, a wide variety of potential configurations are possible, operating under either the time-shared system or the terminal control system.

COMPATIBILITY

The 21MX Series of computers is fully compatible with previous versions of the 2100 line of processors. Virtually all peripherals are interchangeable between the two lines, and all software written for the 2100 line should be convertible to the 21MX with few, if any problems.

HEADQUARTERS

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Palo Alto CA 94304
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(See HP 21MX System Report for system overview, competitive position, and user interviews.)

MAINFRAME

The 21MX is designed to function in both the OEM and end-user markets. It is a microprogrammed, microprogrammable processor with a standard memory configuration of 4K to 32K words (MOS semiconductor), expandable to 196,000 words (theoretically to one million words), controlled through a dynamic mapping system. Dynamic mapping allows a program to be a full 32K words long with an additional full 32K words of data space. In addition to direct addressing, the system provides facilities for indirect addressing and indexing. Software is provided for batch processing, multiprogramming, remote processing, time sharing, and real-time processing. In addition, the system supports assembly language, FORTRAN, FORTRAN IV, BASIC, and ALGOL.

Up to 60 levels of chained priority interrupt are available with I/O slots for a maximum of 56 devices using an I/O extender channel.

CENTRAL PROCESSOR

The 21MX line has two processors — the 2105A and 2108A; they are essentially the same, except the 2108A can be configured with more memory and more I/O capacity than the 2105A. Memory cycle time is 650 nanoseconds per word. The instruction set uses a single-address format; it has a multilevel indirect addressing capability. It includes the standard and extended instruction sets from the older 2100 line, and floating-point arithmetic and data communication instructions. The instruction set provides memory referencing and register-to-register instructions, single- and doubleword integer arithmetic, floating point, indexing, and bit, byte, and word manipulation instruction groups. All instructions are microcoded on four modules of ROM control store. Table 1 lists the HP 21MX optional features.

Special Registers

The 21MX has two accumulators, registers A and B, which are used as a single- or doubleword accumulator by the arithmetic instruction sets. It has two index registers, X and Y, which can be used for address modification, loop control, and subroutine control.

Addressing

Memory is conceptually divided into 1,024-word pages. The basic memory reference instructions can directly address only the current page and the base page. The extended instruction set can address 32K words directly.

The processor includes 60 levels of chained priority interrupt, including power failure, memory parity, memory protect, and I/O levels.

Table 1. Hewlett-Packard HP 21MX: Optional Features

Feature	Model No.	Comments
Direct Memory Access Dual Channel Port Controller	12897A	Operates on cycle-stealing basis.
I/O Extender	2156A	Provides power supplies and prewired slots for 17 additional I/O channels.
Direct Memory Access for Extender	12899A	Requires DMA feature, 12895A, installed in 2100A computer.
Writable Control Store (WCS)	12908B	Permits software development and dynamic storage in RAM modules as an extension to machine control store.
Programmable ROM Writer (PROM)	12909B	Permits conversion of software developed with Writable Control Store into firmware, by "burning in" ROM flatpacks that are plugged into the space left for additional ROM in the control section of the microprocessor.
User Control Store Board	12945A	Mounting facility for user generated firmware.
Scientific Instruction Set	12977A	Enhanced Fast FORTRAN processor. Improves FORTRAN and assembly language program performance.

MICROPROCESSOR

The MX/21 microprocessor standard control store consists of 1,024 directly addressable locations. These are configured into four modules of 256 locations of 24 bits each. Four location stores six micro-orders. The total address space available is 4,096 locations.

Standard control store is used to implement the standard instruction set. In addition, the processor supports Write Control Store (WCS), the 2108A supports two WCS modules, and the 2105A supports a single WCS module.

Each WCS card plugs into a computer I/O slot and provides direct microprogramming capabilities. A card contains 256 24-bit locations of Random Access Memory (RAM), as well as address and read/write circuits. The locations can be accessed through the standard I/O instruction and can be referenced by assembly, FORTRAN, and ALGOL programs.

Software supplied with the WCS includes a micro assembler, debug editor, WCS I/O driver utility and diagnostic routines.

Instructions are executed using the ROM address and instruction registers directly; they are cable-connected to each WCS card. Thus, the cycle time of 325 nanoseconds per word is maintained, regardless of whether the module is in ROM or RAM; this speed is degraded only if the macroprocessor memory or I/O is addressed. In this case, the microprocessor may wait for an appropriate point to enter the macroprocessor 650-nanosecond cycle.

User-generated microprograms can be developed to access 14 registers in addition to the registers normally accessible to user programs. Use of these registers can greatly reduce the number of references to memory, thus increasing processing speed. The 3-operand format of the microinstruction word allows a function to be performed with the contents of two registers — storing the result in a third — all in one microinstruction cycle.

An Optional Programmed ROM Writer, HP 12909B, provides facilities for permanently transferring microprograms to programmable ROM chips. These can then be added to the processor's control store section.

DATA STRUCTURES

The basic data format for the 21MX is a single 16-bit word that can be divided into two 8-bit bytes or linked to another 16-bit word to form a 32-bit doubleword. A seventeenth bit is used for memory parity checking.

The byte format is used for character oriented input/output device; software drivers perform the packing and unpacking functions. The doubleword format is used for both floating-point and extended precision fixed-point arithmetic. Table 2 lists data formats used in the 21MX.

Table 2. Hewlett-Packard HP 21MX: Data Formats

Type of Data	Representation
Operands	
Nonarithmetic	1 wd (bit 15 determines truth value in logical format)
Fixed-Point Arithmetic	
Single	1 wd (15 bits + sign)
Double	2 wds (31 bits + sign)
Floating-Point Arithmetic	
Single Precision	2 wds (7-bit exponent + sign, 23-bit fraction + sign)
Double Precision	3 wds (7-bit exponent + sign, 39-bit fraction + sign)
Complex Numbers	4 wds (both imaginary and real parts have 7-bit exponent + sign and 23-bit fraction)
Hollerith	1 wd (2 ASCII char/word)
Instruction	1 wd (basic instruction set); 2 wds (extended instruction set)

SPECIAL REGISTERS

The 21MX has eight 16-bit registers (six of which can be selected for display and modification by operator control panel switches), two 1-bit registers, one 15-bit register, and a 16-bit display register. Twelve additional 16-bit scratch pad registers are available at the microprogramming level only.

Four of the 16-bit working registers are accessible by software: the A and B registers are accumulators; the X and Y registers serve as index registers. The two accumulators operate independently of each other, and each can store both an operand and the result for either arithmetic or Boolean operations. In addition, they can be linked as a doubleword for shift and rotate instructions. Standard I/O interfaces also use the A and B registers to move data between the mainframe and an interface buffer. The X and Y index registers are two of the scratch pad registers. They are accessible through the extended instruction group, and both can be used for operand address modification and loop control. Subroutine control, however, can be done only with the Y register.

INSTRUCTION SET

The 21MX has two classes of instructions: one emulates the instruction set of the 2100 Series computer, and the other implements new instructions. The 80 instructions from the 2100 are classified by format as memory reference, register reference, input/output, extended arithmetic memory reference, and extended arithmetic register reference. The new instructions include perform indexing, bit and byte manipulation, move and compare (word oriented), and floating-point arithmetic. These instructions are one, two, or three words long: the first word always contains the instruction code; words two and three contain the operand addresses.

Emulated 2100 Series Instructions

Memory reference instructions can directly address 2,048 words of memory: 1,024 words in the current page (the one containing the instruction) and 1,024 words in the base page (the first 1,024 memory words). Other memory locations can be addressed indirectly.

The memory reference class of instructions includes load, store, add, AND, inclusive and exclusive OR, jump, store return and jump to subroutine, compare, and increment memory and skip if zero.

Except for the jump instructions, the memory reference group can address either accumulator. Memory addresses 00 and 01 are reserved to address the two accumulators; thus either accumulator can be treated as a memory location.

Register reference instructions provide shift/rotate, test and skip on zero, increment, complement, and clear either accumulator. The 1-bit E-register used in shift and rotate instructions can be tested and manipulated. This

group also includes a no-op instruction. Register reference instructions can be microcoded to effect more than one operation per instruction.

The I/O group provides for transferring control and status information between either accumulator and an I/O device; for testing device status; for enabling/disabling individual interrupt levels or the whole interrupt system (except power/fail and parity interrupts, which are always enabled); for setting, clearing, or testing the overflow register; and for halting the processor.

The Series 2100 extended arithmetic memory reference instructions provide integer multiply and divide, and load and store double words in the A and B registers. These instructions are two words long: one word for the instruction, the other for the address.

The extended register reference group includes left/right, logical/arithmetic shift, and left/right rotate "n" places on doublewords in the two accumulators.

New 21MX Instructions

The index register instructions provide address modification, loop control, and two jump instructions to enter and exit from subroutines.

The bit and byte manipulation instructions compare, load, move, and store byte strings delimited by a string start address and count field. A separate scan instruction will search for a byte in a delimited string. Three additional instructions clear, set, and test the bit structures in words using a mask control.

The word manipulation instructions compare and move delimited word arrays.

Six floating-point instructions are provided: add, subtract, multiply, divide, fix, and float. Fix converts the floating-point number in the accumulators into an integer, which is placed in accumulator A. Float converts the integer in accumulator A into a 2-word, floating-point number that is stored in the two accumulators.

For the floating-point arithmetic instructions, one operand is assumed to be the contents of the two accumulators, which are treated as a single doubleword; the other operand is a doubleword located in memory. The result is placed in the accumulators.

Table 3 lists typical instruction execution times.

Table 3. Hewelt-Packard HP 21MX: Typical Instruction Execution Times

Instruction	Execution Time (μsec)
Fixed-Point	
Load/Store	1.94
Add	1.94
Subtract	7.12
Multiply	12.32-13.30
Divide	15.92-18.20
Double Load/Store	4.54
Accumulators	
Shift/Rotate	
1-16 Places	2.60-2.92
Floating Point	
Add (avg)	21.78-53.95
Subtract (avg)	22.75-57.20
Multiply (avg)	48.10-56.88
Divide (avg)	41.20-75.72
Fix (avg)	6.50-12.02
Float (avg)	10.72-34.42
Indirect Addressing	
(per level)	1.3

ADDRESSING FACILITIES

The basic address space of 32K words is logically divided into pages of 1,024 words each. The addressing scheme uses a 15-bit memory address composed of a 5-bit page address and a 10-bit word address within the addressed page.

The basic memory reference instructions are formatted so that the relative memory address can refer to a call to either the current page (the one containing the instruction) or the base page (page zero in memory). Thus, a basic memory reference can directly address 2,048 words. An indirect address bit can be set to indicate that the addressed cell contains a 15-bit effective address, which can address 32K words. Indirect addressing is recursive.

The extended memory referencing instructions use a multiword format; the second and third words contain address and/or control information. This provides for 15-bit addresses and one bit for indirect addressing.

Indexing is permitted only through a set of extended instructions newly developed for the 21MX. These instructions can use the contents of the specified index register to modify the 15-bit operand address contained in the second instruction word. Bit 15 of the address indicates direct or indirect.

When the processor attempts to write into nonexistent memory in a system, it executes a no-op. If a read is attempted from nonexistent memory, a word of zeros is transferred, and a parity error interrupt is not generated.

If the HP Dynamic Mapping System option is included in the system configuration, the 5-bit page address is concatenated with the contents of a 5-bit mapping register to provide a 20-bit address field which can address one million words of memory.

Interrupt Control

The priority interrupt system includes 60 interrupt levels. The two highest priority levels are assigned to power fail and parity error. A power fail interrupt cannot be disabled; parity error interrupt can be

disabled. The next two levels are reserved for DMA interrupts, which are generated by the two DMA channels when a DMA block transfer is complete. Channel 1 interrupt has priority over the channel 2 interrupt. The other 56 interrupt levels are assigned to the I/O device channels. Channel interrupts have priority, according to the order of channel number; the lower the channel number the higher its priority.

The master interrupt control can enable or disable all of the interrupt system except power fail and parity error interrupts. The master control can be set or reset by instruction or by the Interrupt System pushbutton on the control panel. It is automatically reset when power is first turned on; thus programs depending on the interrupt system must set the master control.

The next level of interrupt control resides in flag flip-flops associated with the I/O channels. When a channel flag is set, all interrupts from lower priority channels are inhibited.

The lowest level of interrupt control is an interrupt flip-flop that enables/disables an interrupt level.

When an interrupt occurs and it is the highest priority waiting for service, the processor relinquishes control at the end of the current instruction (with some exceptions), stores the program counter in a dedicated core location, and jumps to the address stored in the interrupt's pointer location. Jump indirect instructions and those that may affect the priorities of I/O devices must be completed, plus part of the next instruction, before an interrupt is granted. This allows for system stabilization and such contingencies as a jump to a protected location.

When any interrupt is granted, the interrupt system is disabled until two phases of the interrupt service routine are executed. The interrupt system is then enabled, and only interrupts at a lower priority are inhibited during the execution of the service routine.

MAIN MEMORY

The memory systems available for the 21MX are MOS/RAM semiconductor modules in either high or medium density configurations. The 2101A or X/1 high density memory system is available in either 8K- or 16K-word modules; the 2102A or X/2 medium density memory system is available in 4K- and 8K-word modules. Cycle time for either memory system is 650 nanoseconds, with a maximum memory to memory transfer rate of 310,000 words per second.

The 2108A or M/20 processor can be configured with a minimum of 8K words and a maximum of 64K words of high density memory or a minimum of 4K words, maximum of 32K words of medium density memory. The 2105A or M/10 processor can be configured with a minimum of 8K words, maximum of 32K words of high density memory, or 4K words minimum nd 16K words maximum of medium density memory.

A 12990 memory extender chassis can hold eight 16K-word memory boards or 128K words of memory. This unit, combined with the M/20 processor fully expanded to a 64K-word memory, provides a maximum system with 194K words of memory. Each word consists of 16 data bits and a parity bit. Memory parity checking is standard.

Although the first 64 locations of main memory are reserved for interrupt handling, some of these locations are available to the program if it requires fewer interrupt levels than the 60 provided. The first four words of main memory are not used: memory addresses 00 and 01 are used to refer to the A and B accumulators; addresses 02 and 03 are used for exit sequences if the accumulator contents are used as executable instructions.

The upper 64 locations of memory are reserved for the binary loader which is ROM resident. It is loaded by a pushbutton switch on the operator's console, and can be overlaid by the program.

Memory integrity is maintained through a line loss of 10 Hz; in a power failure, a recovery system option sustains memory up to two hours. The option also provides for automatic restart.

MEMORY PROTECT

The memory protect option, HP 12892A, is available for the 2108A processor only. Memory protect operates through a programmable fence register, which separates lower protected memory from the upper unprotected memory. Two exceptions are that locations 00 and 01 are unprotected because these addresses are reserved to address the accumulators, and the upper 64 memory locations are protected because the resident binary loader is stored there.

When memory protect is enabled, it prohibits the execution of all instructions that write into or transfer control to protected memory, and all I/O instructions in unprotected memory except those referencing the switch or overflow register. This limits I/O control to interrupt control only. If I/O interrupts are serviced by executive routines located in protected memory, the executive can have complete control of all I/O operations.

A memory protect violation causes a memory protect interrupt, which operates on the same level as the parity interrupt. The address of the illegal instruction and the bit indicating parity/protect error is located in the violation register, which can be transferred to the accumulator by instruction.

MEMORY MAPPING SYSTEM

The Dynamic Mapping System (DMS) option, HP 12976A (available only on the 2108A processor), provides up to one million words of address space. The

system operates through four sets of 32 mapping registers. Thirty-eight additional instructions are included for memory control functions.

The mapping system uses four dynamically alterable maps: two for programs and two for the Dual Channel Port Controller (DCPC) to allow scatter read gather write I/O in noncontiguous segments of memory.

In addition to the fence protection of the HP 12892A Memory Protect option, the DMS system provides an expanded memory protect feature. DMS provides read and/or write protection for individual pages of memory.

I/O CONTROL

All peripheral devices are interfaced to the mainframe through plug-in printed circuit assemblies (PCAs). The M/20 processor can accommodate up to nine interface PCAs; the M/10 can accept up to four. Both processors can be expanded by 32 interface slots by adding two optional HP 12979A I/O Extenders. Virtually all interfaces developed for the HP 2100 Series computers can be used with the HP 21MX series.

An interface PCA includes three basic elements, controllable by either the processor or the device for CPU-device communication: a control bit set by the CPU generates a start command; a flag bit indicates to the CPU that a data transfer between the PCA buffer and the device has been completed; and a buffer eight to 40 bits wide (depending on device requirements) operates as intermediate storage.

Device priority is determined by the physical mainframe slot used by the PCA interface. The slot defines the device's fixed address. When the Dual Channel Port Controller (DCPC) is included, it must be assigned to the highest priority I/O slot. If I/O Extenders are used, they are priority ordered differently on the two processors. On the 2105A, the first extender is assigned to channel 13 and addresses 14 through 35 are available for devices; a second extender uses address codes 36 through 57. On the 2108A, the first extender is assigned channel 20 and select codes 21 through 42; the second extender uses address codes 43 through 64.

Medium- and low-speed peripheral devices normally transfer data through the A and B registers (accumulators). Program control can be interrupt driven or via a software driver that examines a flag completion bit with interrupts disabled.

The optional DCPC provides a direct path between a high-speed device and memory. It operates on a memory cycle stealing basis, performing block transfers under count control or until terminated by program. When accessing memory, the DCPC has priority over the CPU for memory accesses.

Transfer rates on low- and medium-speed devices are a function of the device speed, the mainframe interrupt processing time, and the mix of devices simultaneously operating. With the DCPC, however, the maximum transfer rate for combined operation is 616,666 words per second. As channel 1 of the DCPC has priority over channel 2, the rate for channel 2 is the difference between 616K words per second and the operating rate of channel 1. Because DCPC has priority over the CPU, the CPU memory access rate can degrade to the difference between the maximum memory transfer rate and the effective rate of channels 1 and 2 combined, which can be 80 percent of maximum efficiency.

SIMULTANEOUS OPERATIONS

Hewlett-Packard supplies software I/O drivers that let simultaneous I/O operations proceed concurrently with processing. The priority interrupt system provides orderly multiplexing of I/O operations according to the system configuration. A system can have two DMA channels via the Dual Port Channel Controller; thus two devices can transfer data simultaneously via alternate DMA channels. All devices transferring data to or from the accumulators can operate at the same time. The only restriction on I/O simultaneity is imposed by the overall throughput capacity of the system.

Execution of microprograms inhibits standard I/O interrupts, but DMA transfers can occur simultaneously with microprogram execution.

Peripherals

All the conventional peripherals are offered: consoles, paper tape and punched card readers and punches, and platters.

Consoles

Modified Teletype ASR 33 and 35, Teletype KSR printers, and CRT consoles are available. These devices interface to the 21MX via communication lines conforming to EIA specification RS232.

- 2752A Teleprinter, a modified ASR 33 with paper tape reader and punch, which operates at 10 characters per second.
- 2754B Heavy-Duty Teleprinter, a modified ASR 35 with paper tape reader and punch, heavy-duty with pin feed, which operates at 10 characters per second.
- 2762A Terminal KSR Printer, which operates at 10/15/30 characters per second with 75 or 118 columns per line.
- 2615 Character Mode CRT, which includes a 2,000-character memory, asynchronous transmission rate of 110 to 9,600 baud, display area of 25 lines by 80 characters per line, and characters formed with 5 by 7 dot matrix.
- 2616A Page Mode CRT is the same as 2615, except it stores up to 2,048 characters or 256 lines that can be organized in pages of 25 lines each.

High-Speed Paper Tape

The paper tape subsystems read or punch 8-level tapes and operate in asynchronous single character mode.

- 12925A Punched Tape Reader System includes an HP 2748B reader that operates at 500 characters per second.
- 12926A Tape Punch Subsystem includes an H 2895B punch that operates at 75 characters per second, punches 5 or 8 level code. Uses paper, mylar or plastic tape.

Punched Cards

The HP 21MX supports three card reader subsystems and one card punch subsystem. All use 80-column cards.

- 12985A Card Reader Subsystem includes the HP 2892A reader with 1,000-card stacker/hopper. It operates at 600 cards per minute and uses a straight-through card track.
- 12986A Card Reader Subsystem includes the HP 7261A Optical Mark Card Reader that reads either punched or marked cards at rates up to 300 cards per minute. It has 300-card input hopper and can use cards up to 11⅛ inches long. A computer controlled select hopper is available for error or selected cards.
- 7260A Optical Mark Reader is similar to 7261A except for remote connection. It operates at rates up to 2,400 baud, via EIA RS-232C interface in half- or full-duplex mode, and accepts 128-character Hollerith code (card binary image is optional). Transmits data in 7-level ASCII code.
- 12989 Card Punch includes HP 2894A Card Reader Punch Subsystem with or without off-line keyboard punch and verify.

Line Printers

Four line printer subsystems are available.

- 12980A Line Printer Subsystem includes 2610A Line Printer (drum type) and interface, printing at speeds of 150/200 lpm in 132-col lines using 96/64 character set. Prints to six copies and includes 8-channel forms control.
- 12982A Line Printer Subsystem includes 2614A Line Printer (drum type) and interface. It prints at 400/600 lpm in 132-col lines using 96/34 character set on up to 6-part paper.
- 12984A Line Printer Subsystem includes 2767A line printer (drum type) and interface. It prints 300 to 1,100 lpm in 80-col lines and uses 64-character set.
- 12987A Line Printer Subsystem includes a 2607A Line Printer and interface and prints 200/165 lpm in 132-col lines. Uses 128/64-character set.

Magnetic Tape

All magnetic tape units produce IBM-compatible tapes. All include the controller interface, read after write check, and head cleaner; all use 2,400-foot reels.

- 12970A Nine-Track NRZI Magnetic Tape Subsystem includes 7970B tape drive. It records at 800 bpi, and operates on 115/230 volts, switch selectable at 25, 37.5 or 45 ips.
- 12971A Seven-Track NRZI Magnetic Tape Subsystem includes 7970B drive. It records at 200/556/800 bpi, and operates on 115/230 volts, switch selectable, at 25, 37.5 or 45 ips.
- 12972A Nine-Track Phase Encoded Magnetic Tape Subsystems includes 7970E tape drive. It records at 1,600 bpi and operates on 115/230 volts, switch selectable, at 25, 37.5, or 45 ips.

Plotters

One plotter and one plotter interface are offered.

- 12935A Digital Plotter Subsystem includes 7210A plotter. Data input can be in binary or BCD format at rates up to 20 vectors per second. Plots on paper 11 by 17 inches at maximum vector speed of 12 inches per second and resolution of 04-inch in 15 inches.
- 12560B Digital Plotter Subsystem for CalComp 563 or 565 plotter.

MASS STORAGE DEVICES

Fixed-head disc memory, disc cartridge subsystems, and disc files are available.

- 12610C Interface for 2766A Fixed-Head Disc Memory has a capacity of 1M to 4M bytes, average access time 8.7 msec; peak transfer rate 236K words/second.
- 12960A Cartridge Disc Subsystem includes 7900A dual disc subsystem. Capacity is 4.9M bytes, with expansion to 4 units for 19.6M-byte capacity. Features one fixed and one removable disc and average access time of 30 milliseconds.
- 12961A Cartridge Disc Subsystem is the same as 12960A, except it includes only one removable disc with 2.45M-byte capacity.
- 129655A Disc File Subsystem includes 2883A disc file and a controller and drive for 11-disc pack. Capacity is 23.5M bytes, expandable to two drives of 47M bytes. Average access time is 32 milliseconds; transfer rate is 118K words/second.

GENERAL-PURPOSE DEVICES

A number of general-purpose interfaces are available for a user's individual application.

- 12539C Time Base Generator generates real-time intervals from 100 microseconds derived from a crystal oscillator.
- 12551B Relay Output Register has 16 form-A contacts with 48-pin mating connectors for operating external devices. Readback is optional.
- 12554A Duplex Register has dual 16-bit register with 48-pin mating connectors for bidirectional data transfer between computer and external device, positive or negative true.

- 12555B D/A Converter features 2 D/A channels (8 bits/channel).
- 12566B Micro-circuit Duplex Register features dual 16-bit register with 48-pin mating connectors. Also bidirectional data transfer between computer and external device at DTL/TTL voltage levels; ground is positive or negative true.
- 12597A Duplex Register is a dual 8-bit register with 48-pin mating connector. Features bidirectional data transfer between computer and external device, positive or negative true.
- 12620A General-Purpose I/O Interface provides control and flag circuitry on I/O breadboard.
- 12604B Data Source Interface provides 32 lines for sensing external voltages relative to an externally provided reference level.
- 12930A Universal Interface provides a dual 16-bit register for bidirection high-speed data transfer (to 1M Hz) between CPU and external device.

DATA COMMUNICATIONS

Interface kits for connecting a Bell System (or equivalent) data set to a standard I/O channel are available, providing remote as well as local terminal processing. Software is provided to allow a maximum of 32 users.

- 12587B Asynchronous Data Set Interface is half- or full-duplex; echoplex; strappable to provide discrete clock from 45-2, 400 bps; character size to 8 bits; parity and line code under program control. Conforms to EIA RS232B interface; reverse channel can be keyed/detected. Data sets can be Western Electric 103 or 202 or equivalent.
- 12618A Transmit-Receive Synchronous Data Set Interface is half- or full-duplex clocked by data set at speeds up to 9,600 bps. Character size to 8 bits; line code under program control; character or block transfer. Conforms to EIA RS232B interface; reverse channel can be keyed/detected; data sets can be Western Electric 103 or 202 or equivalent.
- 12589A Automatic Calling Unit Interface is for use with Western Electric 801A or 801C Automatic Dialer.
- 12531C or D Asynchronous Terminal Interface is half-duplex; internal or external clocking at rates of 110, 220, 440, 880, and 1,760 bps for Model C and 150, and 300, 600, 1,200 and 2,400 bps for Model D. Internal clocking provided by jumpering; character size to 11 bits (includes start and stop); line code under program control. Current loop or RS232B interface; data sets can be Western Electric 103 or 202 or equivalent.
- 12920A Asynchronous Multiplexor is full-duplex, half-duplex, or echoplex with rates from 57 to 2,400 baud. Interfaces up to 16 devices.
- 12880A Teleprinter Communication, or CRT Channel can be local or remote versions of unbuffered (110, 220, 440, 880, or 1,760 baud) or buffered (150, 300, 600, 1,200, or 2,400 baud) EIA compatible interface, or can be control interface for 2600A CRT.

SOFTWARE

Hewlett-Packard provides a comprehensive set of software packages for the 21MX, including the bulk of the software developed for the earlier 2100 Series computers. Available systems and packages include basic control system monitor (BCS), magnetic tape system (MTS), disc operating system (DOS III), real-time executive (RTE), and terminal control system (TCS). A data base management system, IMAGE, and a remote job entry controller (RJE) are also available. Languages supported are: ASSEMBLER, BASIC, FORTRAN, FORTRAN IV, and ALGOL. In addition, system users have access to over 1,000 applications programs, plus a growing library of microcoded routines.

OPERATING SYSTEMS

The range of operating systems extends from a basic control monitor, which supplies loading and I/O and interrupt processing facilities, through sophisticated packages providing miltiprogramming, priority program scheduling, file management, editing and accounting, and a variety of functions normally associated with contemporary operating systems. Both disc- and magnetic tape-based systems as well as core-based systems are available.

Basic Control System (BCS)

The smallest configurations can use the BCS package. It is organized more like a monitor package than an operating system, but it does provide the basic auxiliary functions needed by most users. It provides link loader and relocation services, an interrupt processing controller, and a library of device drivers.

Magnetic Tape System (MTS)

MTS is a batch processing package that handles batch job stream assemblies, compilations, and loading of both absolute and relocatable programs. It contains a variety of job processing directives and library facilities for file storage of link and load application modules. It is a single tape system; that is, the system tape can store the system, user programs, and temporary data and scratchpad results. It handles programs written in any language support by the 21MX.

Disc Operating System III (DOS-III)

DOS-III is a modular batch processing system that requires a minimum of 4,500 words of main memory and approximately 400K bytes of disc space. It can be generated for a specific configuration to optimize core use for a given application. Noncore resident modules are rolled-in to an overlay area on an as-needed basis. DOS-III consists of an executive kernel module, modular I/O drivers, and a set of general-purpose modules for such functions as file management and memory management. Executing programs communicate with DOS-III

through system executive calls. Run time parameters are supplied to the system through directives entered from the system console.

DOS-III supports logical and physical access up to four disc drives. Logical access is through the Extended File Management Package (EFMP), which allows the user to define record size, security codes, and status information. Standard call procedures include create/destroy, open/close, read/write, reset, repack, copy, change name, and post.

Programs written in FORTRAN, FORTRAN IV, ALGOL, or ASSEMBLY language can run under DOS-III. Object programs can be segmented into main memory modules with subservient segments stored on the disc and called by the main program. Main memory modules and segments can share a common memory area.

DOS-III supports data communications (TCS) and remote job entry (RJE) through separate control programs and the data base management system (IMAGE). The system can incorporate user-defined executive functions for special memory protect and I/O error processing.

Real-Time Executive (RTE)

RTE is available in one core- and two disc-based versions. It is a multiprogramming, foreground/background system, but the core-based version does not provide background processing. One disc version is oriented toward fast response times and the other is oriented toward applications requiring large storage capacity for either programs or data.

RTE services events in real-time multiprogrammed mode with background batch processing. Each user program is classified as real-time (foreground) memory- or disc-resident or batch (background) memory- or disc-resident. Programs are fetched from the disc for execution automatically by the executive. Only one background program can be executed at a time — there is no multiprogramming of background programs. ASSEMBLER, FORTRAN IV, and ALGOL are available in segmented versions that run as background, disc-resident programs under RTE. The core-based version of RTE supports the assemblers and compilers only when the system is not running in a real-time processing mode.

The system provides the following services: program priority scheduling based on priority levels from 00 to 99; normal or privileged interrupt processing; I/O processing and scheduling for concurrent I/O and program execution; and both program and operator request directives. Normal interrupt response time is one to three milliseconds. Privileged response time is one-tenth millisecond. The system also provides data management and resource sharing facilities.

RTE requires a minimum of 16K words of memory (24 words to support ALGOL), high-speed paper tape reader, system Teletype, time-base generator clock, and a minimum of one moving-head disc cartridge subsystem for the disc-based version.

Time-Sharing System

The time-sharing system supports up to 32 interactive users through the Extended BASIC interpreter. Its system supports a variety of terminals and consists of an executive, multiplexor control program, accounting system, and library system.

The executive supervises I/O, bulk memory transfers, program execution, library usage, and accounting systems.

The multiplexor control program operates in response to signals from the terminals. It assigns users priorities based on the tasks they are doing. The scheduler uses a time-slice method to allocate system resources to the user with the fastest response time requirement.

The accounting system controls access to the system and accumulates system statistical data that can be collected into reports when requested by the operator.

The library system maintains public libraries and private user libraries. Public libraries can be accessed by any user, but they can be changed only by the system operator.

When the time-sharing system is not in use, it can be transferred to a removable disc cartridge or magnetic tape. The time-sharing hardware configuration can then be used to support operations under any of the other operating systems.

LANGUAGE PROCESSORS

Language processors for the 21MX include an assembler; Extended BASIC interpreter; and FORTRAN II, FORTRAN IV, and ALGOL compilers.

Assembler

The 21MX assembler is an extended assembler that provides one-to-one correspondence between instruction mnemonics and machine language codes. It also provides pseudo-operations to control the assembly and output listings. It produces absolute or relocatable output code. It has a macroinstruction to provide communication with programs written in microcode in WCS.

Time-Shared BASIC

The 21MX time-shared BASIC is a superset of Dartmouth BASIC. Time-shared BASIC has the following features:

- Matrix handling — addition, subtraction, multiplication, inversion, and transposition of one or two dimensional arrays.

- ASCII character string manipulation — input, output, comparison, storage, and retrieval of strings up to 126 characters.
- Data files — can be created and saved and arranged serially or randomly; maximum file capacity is 6,144 words for the 2000E and 8.4 million words for 2000F.
- Simultaneous access to data files — allows multiple users to read the same data file and a special group of users to write in the same data file.
- Program chaining — lets one BASIC program call another at execution time. A large program can be broken into segments and chained together. A COMMON statement allows variables to be passed between programs.
- System clock — accessible by users at execution time for time of day, day, and year.
- Diagnostics — the BASIC interpreter checks format and syntax of statements when entered, and performs program structural checks during execution.

FORTRAN

Both FORTRAN, an extended version of USASI Basic FORTRAN, and FORTRAN IV are available. FORTRAN IV is a full implementation of Standard FORTRAN. Programs written in Hewlett-Packard FORTRAN can be compiled by either compiler.

Hewlett-Packard FORTRAN includes the following extensions to Basic FORTRAN.

- Format specifications can be entered at execution time.
- COMMON array declarations are permitted.
- A function subprogram can change the values of its arguments and of COMMON storage; that is, the arguments of function subprograms are "called by name."
- External functions are included for Boolean operations.
- The "$" sign is included in the character set.
- A 2-branch form of the IF statement is included.
- A facility for octal constant specification is provided.

The compiler is available in paper tape and magnetic tape versions. For the paper tape version, the minimum is 4,096 words of main memory and a 2752A teleprinter, but the addition of a paper tape reader and punch significantly increases the compilation speed. Both versions of the compiler produce an object program in relocatable binary format for loading by the Basic Control System. The program can be linked to relocatable binary subprograms originating from assembly code or ALGOL source code.

FORTRAN IV compiler requires 7K words of core memory. It can run under DOS or RTE operating systems. RTE FORTRAN IV has special statements for real-time control.

ALGOL

Hewlett-Packard's ALGOL incorporates all the features described in the ALGOL 60 Revised Report, published in the *Communications of the ACM* for January 1963. The I/O statements are the same as for 21MX FORTRAN. All variables are treated as OWN variables. Other features of the source language include the following.

- Facilities for intermixing identifiers of types REAL and INTEGER in the same assignment statement.
- Provision for initializing variables and arrays.
- An EQUATE statement.

The compiler requires a main memory of 8,192 words and a teleprinter. The compiler operates in a single pass of the source code, and produces an object program in relocatable format for loading by the Basic Control System. Relocatable programs generated from ALGOL source language can be linked to subprograms generated from FORTRAN or assembly language source code. There are essentially no restrictions on the size of the ALGOL program that can be compiled.

UTILITIES AND SPECIAL-PURPOSE SOFTWARE

IMAGE/2000

IMAGE/2000 is a data base management system loosely patterned along the guidelines of CODASYL's Data Base Task Group Report of April 1970. It is composed of four subsystems: Definition, Utility, Management, and Query. It interfaces with DOS-III and requires a minimum of 1,500 words of dedicated memory for its information tables, plus 4K words for its management functions. The package is resident in approximately 300K bytes of disc storage.

An IMAGE system can have up to 255 data bases. Each data base can consist of 20 data sets of 32,767 data entries or records. Data entries are fixed length (up to 512 bytes long); individual data items or fields can be from 1 to 126 bytes long.

IMAGE provides a data base definition language so users can describe the data record format and the relationships among the records in the data base. The relationships are made using chain-linked lists that create a limited network within a given data base.

The Data Base Management subsystem is used to access the data base; it provides record/field search techniques using Boolean and relational conditionals.

A utility system allows users to create a data base from data streams formatted into data set/data entry groupings. Data sets are of two varieties — master and detail. Master data sets consist of key values, randomly distributed in the available data space according to a key hashing algorithm. Each entry also contains pointer data

for the detail elements associated with that key. Each master can have up to five associated detail data sets. Each contains a chain-linked record, with pointers back to the master key data set. Each detail data set can be linked to five different master data sets.

A query subsystem, oriented toward the nonprogrammer, provides on-line data access from a single console. Host language provides facilities to retrieve, update, add, and delete records; sort retrieved records; and specify report formats and report generating criteria.

HP Remote Job Entry (HP RJE)

The HP RJE emulates an IBM 2780 Models 1 and 3 for communication with an IBM 360/370 OS HASP facility. Job processing information, messages, records, transactions, or files can be transferred.

Terminal Control System (TCS)

This multitasking terminal supervisor can handle up to 32 terminals. It requires about 6.5K words of memory running under executive control of DOS-III. The system runs à single job, which can be broken up into a main program and segments that function as tasks or transaction processors. TCS provides the following services: priority scheduling, dynamic buffer allocation, queuing of I/O request, disc-resident program segment loading, and device locking. Hewlett-Packard advertises that the system can handle up to 10,000 transactions per hour, with an interactive terminal average response time of one second.

TCS services are provided to the application program segments through the call facilities of the program's host language.

APPLICATION PROGRAMS

The 21MX library includes over 1,000 tested and documented programs for data handling and programming utilities, scientific and numerical analysis, operations research, business applications, education, and demonstration routines.

HEWLETT-PACKARD

HP 3000CX Series

OVERVIEW

The HP 3000CX Series contains a group of preconfigured systems intended to satisfy the batch and on-line data processing requirements of the general user. Each system is based on the HP 3000 16-bit minicomputer configured with 32K to 128K bytes of memory, peripherals, and software. Although the series has a strong orientation towards the terminal user and Hewlett-Packard's traditional market — scientific/engineering, time-sharing, and real-time processing, typical business-oriented components — COBOL, RPG II, and a data base management system — give the system an appeal to an extremely wide market.

Four models or hardware configurations are marketed within the series: 50CX, 100CX, 200CX, and 300CX. The four models use a common operating system (MPE/C) that operates in both terminal and multiprogramming batch mode with full spooling capabilities. Software is build around full hardware implementation in the stack architecture of the HP 3000 CPU. Each model is upward compatible and can be field expanded with a minimum of dislocation.

The CPU stack architecture gives the user reentrant, recursive programming without the excessive overhead of non-stack systems. The code and data segments of a program are segregated so that each functions in its own domain and each is addressable through its own register set. (No instruction in the HP 3000 permits a program operating in task mode to modify the program.)

The system has 176 microcoded instructions that perform fixed- and floating-point arithmetic, relational operations, boolean functions, word and bit tests, byte and word move operations, scan and test functions, plus various shift and program and loop control instructions. In addition, optional decimal and extended floating-point instruction sets are available. Provisions are also made for both indirect and indexed address modification.

In addition to the stack processing mode, the HP 3000CX provides for maximum usage of available memory space through a virtual memory addressing technique that is largely transparent to the user. Virtual memory address space is 64K words.

The system allows up to 253 separate priority interrupt levels and handles a variety of peripheral equipments. Three modes of I/O operation are available: direct, multiplexed, and selector channel. The organization of the interrupt and I/O systems allows independent ordering of device service priority, device access priority, and device interrupt priority.

The entire system is organized around a Central Data Bus; the CPU, main memory, IOP and selector channels use the central data bus to communicate with each other. Although this path serves as a limiting factor on access time and aggregate transfer rate, its speed of 5.7M bytes per second is sufficient to handle virtually all situations.

Table 1 lists the mainframe characteristics.

In addition to the MPE/C operating system for the HP 3000CX, Hewlett-Packard provides both a BASIC interpreter and compiler, FORTRAN, COBOL, RPG II, SPL (Hewlett-Packard's Algol-like System Programming Language) IMAGE/3000, various utility packages, such as Sort and Trace, and a host of applications programs.

The system can be integrated into a network of HP 3000CX data centers or interfaced to a large computing facility. Additionally, BASIC programs from the smaller HP 2100 and 21MX Timesharing Series can be moved up to the HP 3000CX processors.

Table 2 lists the basic and optional configurations of the four models.

Competitive Position

The HP 3000CX is in an excellent competitive position for the medium-scale, general-purpose processing environments in which it will be marketed. Its commercial processing features, notably COBOL, IMAGE/3000 (a data base management system), RPG II, and a spooling capability, should appeal to users with a variety of jobs — scientific, engineering, and commercial processing — and a limited budget.

Prime competition for the 50CX and 100CX will be Digital's 11/40 and 11/45 under RSTS-11/E or RSX-11D or M at the lower end, and small Digital System 10s as well as XEROX 550 and 560 with the 200CX and 300CX at the top end. Systems such as the Data General ECLIPSE Series, Burroughs 1700 Series, IBM 370/115, 125, and 135, Modular Computer MODCOMP IV, PRIME 300, Varian V74, General Automation SPC-16/80, and Interdata Models 7/32 and 8/32 compete for some applications.

The prime thrust of Hewlett-Packard's marketing activities will be towards new installations and upgrades of obsolete or obsolescent installations, BASIC timesharing

installations, and small commercial and various engineering applications. Because of its comprehensive software, the 3000CX should be a prime contender for customers with a wide variety of data processing tasks and a small budget. Although minicomputer manufacturers are providing more support for commercial processing, none offer the wide variety available with the HP 3000CX, especially comparable to IMAGE/3000 for data base management. This variety has been the domain of Xerox with its Sigma line (now replaced by 550 and 560) and Digital with its PDP-10. The sophisticated operating systems required to perform this variety of tasks on general-purpose systems are available only for large configurations. Minicomputers such as the PDP-11/45 are moving in this marketing direction. Thus, Hewlett-Packard should "make hay while the sun shines" because the hay fields will soon be full of competing reapers.

Configuration Guide

Table 1 lists the configurations for the four models of the 3000CX Series. The range of configurations addresses a broad spectrum of applications from the 50CX, which is geared to both the small user and the OEM market, to the 300CX, which is adaptable to most medium-scale environments. It should be noted that all models are based on a common processor and a common operating system. This single feature provides the user with the capability to upgrade his computing, terminal, and I/O power without the usual trauma associated with such changes.

Table 3 lists the peripherals available. Table 4 provides a summary of the available software.

Compatibility

The four models of the HP 3000CX Series are fully compatible with each other at the CPU and program level.

Table 1. HP 3000CX Series: Mainframe Characteristics

Central Processor	
Type	Microprogrammed
Control Memory	
Size	2,048 (32 bit)
Use	Firmware
No. of Internal Registers	11
Addressing	
Direct	Variable for instructions + data
Indirect	1 level, 64K
Indexed	Yes
Instruction Set	
Implementation	Microprogrammed
Number	172
Decimal Arithmetic	Opt firmware
Floating-Point Arithmetic	Yes (opt extended F-P firmware)
User Microprogramming	No
Priority Interrupt System Operation Modes	
Levels	253
Main Storage	
Type	Core
Cycle Time (msec)	0.980
Basic Addressable Unit	Word (16-bit)
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	96K
Max Capacity (bytes)	28K
Increment Size (bytes)	32K
Ports per Module	1
Error Checks	Parity
Protection Method	Bounds/stack
Memory Management	Yes, stack
ROM	No
Use	
Capacity	
RAM	No
Use	
Capacity	
I/O Channels	
Programmed I/O	Yes
DMA Channels	4
Multiplexed I/O (no. of subchannels)	2 (32)
Max Transfer Rate	
Within Memory (Central Data Bus)	5.7M bytes
Over DMA	3.8M bytes
Simultaneous Operations	Yes

DATA COMMUNICATIONS

The HP 3000CX provides a wide variety of data communications facilities from a multi-terminal time-shared mode of operation to a multi-processing distributed network configuration and from a remote job entry or front-end facility to a large 370 type system.

When operating with a second processor, the interprocessor communications operations are multiprogrammed with both other terminal and batch jobs.

Maintenance and Support

Hewlett-Packard is noted within the industry for its product support. The company maintains 172 field offices in 65 countries throughout the world including 60 service facilities in the United States and Canada, backed by five regional offices. Two service and warranty plans are available under terms of the purchase agreement. One provides for "parts only" warranty for 15 months; a second provides full services, parts, and labor for 90 days. Follow-on agreements can provide for guaranteed response times and full service or operate on a per-call time-and-materials basis.

Hewlett-Packard also provides a set of diagnostics that function as a task of the operating system. A stand-alone set runs directly on the CPU without operating system aid. In addition, a set of microprogrammed micro-diagnostics can be executed and transmitted directly to Hewlett-Packard through a modem and common carrier line for immediate assistance on difficult problems.

Table 2. HP 3000CX Series: Basic Configurations and Options

Basic Configurations	50CX	100CX	200CX	300CX
Memory (bytes)	96K	96K	128K	128K
Disc (bytes)	5M (moving hd cartridge)	10M (moving hd cartridge)	2M (fixed hd) 47M (mov. hd pack)	2M (fixed hd) 47M (mov. hd pack)
Tape	800 bpi	800 bpi	800 bpi	800 bpi
Peripherals	—	200-lpm printer	200-lpm printer	1,250-lpm printer
	—	600-cpm reader	600-cpm reader	reader/punch 200 cpm (30-75 cpm)
Terminal	16-port Async term controller	16-port Async term controller	16-port Async term controller	16-port Async term controller
Software	MPE/C	MPE/C	MPE/C	MPE/C
	Utilities	Utilities	Utilities	Utilities
	SPL	SPL	SPL	SPL
	Comp. lib.	Comp. lib	Comp. lib	Comp. lib
	Trace	Trace	Trace	Trace
	Editor	Editor	Editor	Editor
	Sort	Sort	Sort	Sort
Options				
Memory (bytes)	128K	128K	—	—
Disc	Expandable	Expandable	Expandable	Expandable
Tape	1,600 bpi	1,600 bpi	1,600 bpi	1,600 bpi
Peripheral	—	Delete	Delete	Delete
Terminal	Add 202 capability	Add 202 capability	Add 202 capability	Add 202 capability
Software/Firmware*				
	MPET	MPET	MPET	MPET
		BASIC	Same as 100CX	Same as 200CX
		FORTRAN IV	Plus:- COBOL	
		RPG	IMAGE	
		Decimal Firmware, expanded floating-pt firmware		
Additional Hardware			Real-time data acquisition programmable controller	

**Available in packaged combinations at various prices*

Table 3. HP 3000CX Series: Peripherals

Device Model	Description
Discs	
30103A	Fixed head; 2M bytes; 236KW/sec
30102A	Moving head; 4.9M bytes; 156KW/sec
30110A	Moving head; 47M bytes; 246KW/sec
Magnetic Tapes	
30115A	9 trk; 800 bpi; 36KB/sec
30115A-100	9 trk; 1,600 bpi; 72KB/sec
Card	
30106	600-cpm reader
30119A	Reader/punch; 200 cpm/30-75 cpm
30119A-001	Keyboard + verify
Printer	
30118A	600 lpm; 64 char set; 132 col
30118A-002	128 char set option
30128	1,250 lpm; 64 char set; 132 col
30128-001	96 char option
30127	300 lpm; 64 char; 132 col
30127-001	96 char set
Paper Tape	
30104A	Reader: 500 cps
30105A	Punch: 75 cps
Data Communications	
30032	16-port async channel
30120A	Terminal/console, 30 cps/75 col, 300 baud
30120A-001	Opt 118 col
30124A	ASR-33, 10 CPS
30123A	CRT, 72 char x 25 line, switchable data rates HP2640 Terminal
30300A	Programmable controller, based on HP 2100 mini

Table 4. HP 3000CX Series: Software

MPE/C	Multiprogramming execution, multiprogrammed batch and on-line terminal; full logical level I/O and data communications handle.
MPET	A limited subset of MPE/C oriented to environments using primarily BASIC.
Language Processors	FORTRAN, COBOL, Systems Programming Language (SPL), RPG II, BASIC (both a compiler + interpreter version)
Special Purpose	Image/3000, a data base management system; Query/3000 terminal-based query facility for Image/3000 data base
Scientific Library	A collection of various functions and transforms
Other	Diagnostics, utilities, user library

HEADQUARTERS

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TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	PROCESSORS AND WORKING STORAGE		
30000C	Model 50CX (includes CPU with 96K bytes of core memory; multiplexor channel (15 device capacity); async terminal controller (16 ports); system console and cabinets; mag tape unit; 5M-byte cartridge disc unit; std power with 120/208V and 3 phase/60Hz)	99,500	687
32400C	Model 100CX (same as 30000C except multiplexor channel (16 device capacity); 10M bytes of disc storage; 5M byte cartridge disc unit plus additional 5M-byte drive; 600-cpm card reader subsystem; 200-lpm dot matrix printer)	129,500	953
32401C	Model 200CX (same as 32400C except CPU with 128K bytes of core memory; 2M-byte fixed-head disc; 47M-byte moving-head disc; 600-cpm card reader subsystem; 200-lpm dot matrix line printer)	171,000	1,134
32402C	Model 300CX (same as 32401C except with 1,250-lpm printer; reader/punch subsystem)	203,500	1,263
	Processor Options		
	All Processors		
001	MPET operating system in place of MPE	NC	NC
015	System AC power option with 230V	NC	NC
100	1,600-bpi tape unit replaces 800-bpi unit	1,500	30
202	Adds 202 type data set control to async terminal controller	1,240	8
	Processor Options 50CX		
181	Increases memory to 128K bytes	10,000	34
403	Delete disc cartridge system	8,000	136
	Processor Options 100CX, 200CX		
401	Deletes 600-cpm card reader	-6,000	-66
402	Deletes dot matrix printer	-9,000	-83
600	Timeshare package	NC	40
601	Scientific package	5,000	49
602	Commercial package	5,000	44
603	Commercial and scientific package	9,000	74
	100CX and 200CX Option		
102	128-char option for line printer	500	NC
	200CX and 300CX Options		
104	Expands fixed-head disc to 4M bytes	6,600	18
	300CX Options		
102	96 character option for line printer	2,000	18
106	Keyboard and verify capability added to reader/punch	2,000	NC
404	Delete card reader/punch subsystem	-12,000	-127
405	Delete high-speed printer	-28,000	-151
604	Commercial package without data base management capability	6,000	64
605	Commercial and scientific package without data base management capability	10,000	94
	MEMORY AND CPU ENHANCEMENTS		
30011A	Expanded instruction set	3,250	19
30011A-001	Replaces extended-precision floating-point instruction set with decimal firmware instruction set	1,000	NC
30011A-002	Adds the decimal firmware instruction set to the extended-precision floating-point instruction set	2,000	NC
30414A	Field-installed memory upgrade kit (increases memory to 96K-bytes)	11,000	46
30429A	Field-installed memory upgrade kit (increases memory from 64K-bytes to 128K-bytes)	21,500	80
30431A	Field-installed memory upgrade kit (increases memory from 96K-bytes to 128K-bytes)	11,000	34
	MASS STORAGE		
30102A/015*	47M-byte disc file subsystem	32,000	216
30102A/010*	Adds drive on same controller	-12,000	-40
30103A	Fixed-head disc subsystem with 1.0M bytes of storage	20,000	148
30103A-001*	Adds 1.0M bytes of storage	3,300	36
30103A-002*	Adds 3.0M bytes of storage	9,900	54
30110A/015*	Cartridge disc subsystem	15,000	136
30110A-010*	Adds additional 7900 drive (5M bytes)	-5,025	-19
	INPUT/OUTPUT		
	LINE PRINTERS		
30118A/015*	200-lpm subsystem (132 col; 64 char)	9,750	83
30118A-001*	128 char set	500	NC
30127A/015	300-lpm subsystem with 136 col and 64 char	13,500	135
30127A-001*	96 char set	2,000	NC
30128A/015*	1,250-lpm subsystem with 132 col and 64 char	36,000	151
30128A-001*	96 char set	2,000	NC
	PUNCHED CARD		
30106A/015*	Card reader subsystem: 600 cpm	7,160	66
30107A/015*	Card reader subsystem: 1,200 cpm	18,540	126
30107A/001*	Adds double read station	2,575	2
30119A/015*	Card reader/punch subsystem: reads 200 cpm, punches 75 cpm	13,500	127
30119A-002*	Adds off-line keyboard punch and verify capability	2,000	NC
	MAGNETIC TAPE		
30115A	Includes 2,400 ft of tape and cabinets; 9 channel, 800 cpi, 45 ips; includes controller interface. Handles up to four 9-channel mag tape units - one 30115A and mixture of up to three additional units (i.e. either 30115A-200's, 30115A-300's, or 30115A-400's)	12,000	93
30115A-100*	9 channel, 1,600 cpi, 45 ips. Includes controller interface, handles up to four 9-channel mag tape units	1,500	30
30115A-200*	Adds an additional 800 cpi, 45 ips, 9-channel drive	-2,450	-22
30115A-300*	Adds a 9-channel, 1,600 cpi, 45 ips, master drive	-975	8
30115A-400*	Adds a 9-channel, 1,600 cpi, 45 ips, *slave* drive	2,500	NC
	PAPER TAPE		
30104A	Cabinets + controller interface included; paper tape reader subsystem (500 cps)	3,350	32
30105A	Paper tape punch subsystem (75 cps)	4,225	52
	TERMINALS		
30120A/015*	Printer Terminal (30-cps, 75-col keyboard, and pin feed with paper guide; w/o pedestal)	4,920	38
30120A-001*	Adds 118 col facility and replaces pin feed with tractor mechanism; vertical tab/form feed, horizontal tab, and pedestal included	1,135	NC
30120A-003*	Friction feed replaces pin feed; with pedestal	NC	NC
30120A-015*	230V/30Hz ac power option	220	NC
30122A/015*	Character-mode CRT (2615A)	2,835	36
30124A	Teletype terminal (10 cps ASR-33)	2,650	68
30124A-015*	230V/50Hz ac power option	200	NC
	EXPANDED I/O CAPABILITY		
30030A	High-speed selector channel	6,080	13
30032B	Async terminal controller (Note: Option 001 or 002 must be ordered)	3,000	18
30032B-001*	For 103 type modems only	1,240	8
30032B-002*	For 103 and 202 type modems	2,480	16
	ADDITIONAL DEVICE INTERFACES		
30126A	CalComp plotter interface for 500 Series plotters	1,030	5
30300A/015*	Programmable controller with 8K of memory	18,000	207
30361A	Programmable controller interface kit	5,000	8
	REAL-TIME CAPABILITY		
30301A/015*	Real-time programmable controller (includes HP 2100S computer with 8K-words of memory, DMA, programmable time-base generator, hardware extended arithmetic and floating-point instructions; paper tape reader; teleprinter; interconnection interfaces; signal cable, cabinets; software	23,000	NA
30361A-001*	Option to the programmable controller interface kit replaces BCS/3000 software with the RTE C/3000 software	+2,000	NA
	DATA COMMUNICATION		
30130A	2780/3780 Emulation Subsystem	3,500	30
30441A	Adds 202 modem support to async term controller	1,500	8

*indicates option number
NA-information not available

HONEYWELL

System 700 System Report

OVERVIEW

System 700 is a line of general-purpose minicomputers, which are marketed primarily as components of a large data processing network. The 700 offers good I/O and interrupt facilities, a broad range of peripherals, and well-integrated software. Both hardware and software place emphasis on the real-time processing required for process control, data collection, and data communications environments.

The three models currently being offered for the 700 Series are all based on the 716 processor first announced in 1972. The 716 uses a 16-bit word, and memory cycle time is 775 nanoseconds per word. The models have letter suffixes indicating function: G for "general-purpose," S for "sensor-based," and "M" for rack-mounted version targeted at system builders who want to use their own cabinets. The 725-G/735-G General-Purpose System, the 725-S/735-S Sensor-Based System, and the 725-M Rack-Mounted System comprise the newest system offerings.

Standard features for the G and S systems are high-speed arithmetic, real-time clock, and 8K-word memory boards that allow memory to be extended to 64K words within the main processor chassis. Table 1 lists mainframe characteristics.

Peripherals available for the 700 Series include a wide variety of low-speed, mass storage, and special subsystems. Table 2 lists peripherals.

One strong point of the 700 Series is its data communications capability. There are several special-purpose "Datanet" 700 communications systems based on the 716 processor. These Datanet systems are designed to provide minicomputer-controlled remote batch processors, concentrators, and distributed processors that can be configured into a large network controlled by Honeywell or IBM computers. The equivalent of Datanet systems can be configured with 725-G/735-G systems, using RJE (HASP II) or the RCP 707 systems software packages.

Operating system support is provided by OS/700, a modular real-time, multiprogramming system that provides computer-to-computer communication, priority-oriented task scheduling, and centralized control of all system resources. OS/700 is available in both core-based (COS) and disc-based (DOS) versions. The FORTRAN IV compiler, BASIC interpreter, and Assembler can run under OS/700 or can operate in a free-standing environment. Host-resident software systems allow program development on other Honeywell or IBM computers. In addition, OS/700 can support extensive communications facilities and a file management package. Since the RJE (HASP II) and RCP 707 system software packages are also available, a user could implement a Datanet system from a 725 or 735, given the proper configuration. Table 3 lists software configuration requirements.

Table 1. Honeywell System 700: Mainframe Characteristics

Central Processor	
Type (microprogrammed)	No
Control Memory (RAM, ROM)	–
Size	
Use	
No. of Internal Registers	2 general-purpose, 1 index register; alternate index register
Addressing	
Direct (no. of words)	1,024(1)
Indirect	Multilevel
Indexed	Yes
Instruction Set	
Implementation (hardware, firmware)	Hardware
Number (std, opt)	78 std, 4 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	By subroutine
User Microprogramming	–
Priority Interrupt System Operation Modes Levels	3-48
Main Storage	
Type	Core
Cycle Time (μsec)	0.775
Basic Addressable Unit	16-bit word
Bytes per Access	2
Cache Memory	No
Min Capacity (bytes)	16K(2)
Max Capacity (bytes)	128K
Increment Size (bytes)	16K
Ports per Module	1
Error Checks	Parity (opt)
Protection Method	Memory lockout (opt)
Memory Management	–
ROM	
Use	Loaders
Capacity (bytes)	256-2,048 words
I/O Channels	
Programmed I/O	Yes
DMA Channels	Yes (no limit)
Multiplexed I/O (no. of subchannels)	DMC optional (8)
Max Transfer Rate	
Within Memory (wds/sec)	321,500
Over DMA (wds/sec)	1,290,000
Simultaneous Operations	None, except multiple peripherals with processing

Notes:
(1) Base sector and current sector; base sector is optionally relocatable.
(2) OS/700 requires 32K bytes of memory for a program development system. Execute-only systems can be configured with as little as 16K bytes of memory.

Relationship to Other Honeywell Products

The 700 line has undergone a number of evolutionary changes and reorganizations; most of these represent changes in pricing (getting more for less) and marketing (model numbering, definition of "BASIC" systems) coupled with some engineering developments (8K-word memory boards). The current 725-6/735-G General-Purpose System, for instance, directly replaces the 720/01 Terminal System and the 720/02 Peripheral System as well as retiring the 720/03 Multipurpose System and the

Table 2. Honeywell System 700: Peripherals

Fixed-Head Disc—64K, 128K, 256K, and 512K wds on 16, 32, 64, and 128 trks, respectively; avg access time, 12.5 msec; transfer rate, 82K wds/sec.
Removable-Head Disc—6 drives with capacities of 0.9M to 7.2M wds; 7.5M wds; 1.1M wds; 1.8M wds; 3.7M wds; and 7.5M wds.
Magnetic Tape—tape cassette system; 6 subsystems including 7-trk and 9-trk units, with 200-, 556-, 800-, and 1,600-bpi densities.
Printers—9 printers at 200, 300, 450, 650, 950, and 1,100 lpm; 96, 120, and 136 cols; 64 and 96 char sets.
Punched Card—readers at 300, 600, 800, and 1,050 cpm; punches at 400-1,000 cpm; reader/punches at 400 cpm read, 100-400 cpm punch.
Paper Tape—reader at 300-cps max transfer rate, 8-level tape; punch at 110-cps max transfer rate, 8-level tape.
Teletype—ASR 33, KSR 33, ASR 35; ASR includes paper tape reader/punch.

Table 3. Honeywell System 700: Software Configuration Requirements

Operating System	Configuration Required
OS/700	
DOS (disc-based)	716 processor, 16K-wd main memory, 1 disc with 128K wds/min, 1 programmed I/O device
COS (core-based)	716 processor, 24K-wd main memory, 1 programmed I/O device
BOS (Batch Operating System)	716 or 316 processor; 12K-wd core memory, 0.9M-wd disc storage, ASR 33 Teletype
OP-16 Real-Time Operating System	716 or 316 processor, 4K-wd main memory, real-time clock, ASR 33 or 35 Teletype

720/05 Batch Processing System, both of which were based on the H316 processor. The current 725-S/735-S directly replaces the 720/20 Sensor-Based System and the 720/21 Extended Sensor-Based System. Both the new G and S systems include as standard features several 720/xx options such as high-speed arithmetic and real-time clock; also both use only 8K-word memory boards, allowing 64K words of memory to be stored within the main processor chassis.

The 716 processor that serves as the foundation for the 700 Series is architecturally similar to the earlier 316 and 516 models. The 716 instruction set includes the 316 and 516 instructions as subsets. Since all 16 Series peripherals can attach to a 716 with the aid of the DMC adapter option, program compatibility is completely maintained given the same environments. In addition, all 316 and 516 programs can run on the 716. The OP-16 and BOS operating systems developed for the 316 are also available in 716 versions for users who want to run 316 programs on a 716.

The 716 processor has stack-register and register-addressing features unavailable on the Series 16 processors. These features include standard DMA channel, a complete line of data communications hardware, a new real-time operating system (OS/700), and host-resident software. In addition, the 716 is 20 percent faster than the DDP-516 and over twice as fast as the H316.

System 700 models can duplicate all of the major Series 16 systems except the 1640 Timesharing Systems. Honeywell currently has no plans to upgrade the time-sharing systems to use the 716 processor.

COMPETITIVE POSITION

Honeywell is not marketing the 716 processor chiefly as a minicomputer or as an upgrade to the Series 16 processors. The system is marketed by the commercial data processing sales force, which is concerned with the total computer network, so System 700 configurations are sold as component parts of that network.

The Series 16, forerunners of the 700 Series, were strong competitors in the minicomputer field. Unlike Digital with its PDP-11 line, Honeywell did not change the architecture of the 716 processor from that of the older Series 16 line. This evolutionary path to computer development protects the Series 16 users' software and peripherals, and provides the 716 system for upgrading.

The System 700 models span the breadth of the major part of the minicomputer market, including most of the OEM segment. System 700 is offered unbundled for the OEM market; contracts for the system are negotiated with the home office. There is no equivalent to the smaller, slower board-level "microcomputers" that manufacturers like General Automation and Digital are adding at the bottom end of their lines, mostly for OEM applications. Moreover, Honeywell has not added a memory mapping option to extend the line into the larger 128K- and 256K-word systems available from manufacturers like Hewlett-Packard and again Digital and General Automation, plus Interdata and Modular Computers.

The sensor-based systems compete directly with the IBM System/7, 1130 and 1800, CDC 1700, Xerox Sigma 3, and Digital PDP-11 for data acquisition, manufacturing, and process control applications. General-purpose models compete both as business minis and as terminal control systems. As such, they are directly competitive with such intelligent terminal systems as MODCOMP I and III; Four-Phase System IV/70; and, in some cases, IBM System/3. These systems are designed for data collection and limited processing from terminals in banks, factories, and laboratories.

Honeywell's advantage in this market is that customers can obtain a total distributed processing network from a single supplier. Univac offers this capability, but IBM has refrained from embracing this type of distributed systems concept, stressing instead large centralized systems. As a result, independents have developed the distributed processing idea — and Honeywell's 716-based HASP II RTE package directly competes in the general intelligent terminal market geared toward IBM computers.

The System 700's most direct competitor is PRIME Computer's PRIME 100, 200, and 300, which are program and peripheral compatible with the Honeywell Series 16

line. The PRIME computers utilize MSI and LSI technology plus all MOS memories. They offer many enhancements over the Series 16, including a substantial upgrade capability to the midi-range PRIME 300. Honeywell's shift of emphasis away from the minicomputer market to the network market has the advantage of consolidating its computer lines, but it has also left a vacuum in the minicomputer market that PRIME has moved to fill.

Configuration Guide

All 700 Series systems are based on the 716 processor. The 725 configurations have software and support separately priced, while the 735s have these items bundled. Basic configurations are as follows:

- 725-G/735-G General-Purpose System — includes 716 processor in a 60-inch cabinet with control panel, real-time clock, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base-sector relocation, and 8K words of core; a teleprinter is also part of the basic configuration.
- 725-M Rack-Mounted System — for system builders who want to use their own cabinets; identical to 725-G, but no cabinet and power distribution unit.
- 725-S/735-S Sensor-Based System — includes 716 processor with control panel, real-time clock, watchdog timer, multiline priority interrupt system with 3 levels implemented, power fail/auto restart, hardware multiply/divide, base sector relocation, analog/digital subsystem controller capable of holding 8 digital and 8 analog pages (1 digital page is implemented), 8K words of core, and 2 cabinets; a teleprinter is also part of the basic configuration.

Processor options include parity, an additional crystal-controlled clock, watchdog timer (for the 725-G/735-G), 512 to 2,048 words of ROM, the communications controller, and a wide variety of peripherals. Memory can be expanded to 64K words, but expansion over 32K requires an extended memory controller that slows memory cycle time to 855 nanoseconds for the first 32K words and to 1,030 nanoseconds for memory above 32K. Memory is added in 8K-word increments with all eight modules housed in the system cabinet.

DMA and programmed I/O channels are standard to all systems. An optional Direct Multiplex Control (DMC) adapter can be added in order to attach a maximum of eight controllers from the Series 16 line of peripherals.

A Binary Synchronous Down-Line Load Option (2,048-word ROM) and other communications devices can be attached to either processor. Only the 725-S/735-S, however, can handle the real-time interface for sensor-based applications.

Compatibility

The 716 instruction set includes the H316 and DDP-516 instruction set as a subset. An optional DMC adapter for the 716 allows connection of the H316 and DDP-516 peripherals that transfer data via a DMC unit.

Honeywell has introduced new peripherals that encompass all the other peripherals used with the H316 and DDP-516. As a result, virtually all software developed for the H316 and DDP-516 can run on the 716. The 716 processor has features that are unavailable for the H316 and DDP-516, so any 716 software using the new features cannot run on the other two processors.

MAINTENANCE AND SUPPORT

Honeywell provides world-wide marketing support, including several hundred local offices for its Field Engineering Division. An emergency network provides service 24 hours a day, 7 days a week.

For the System 700, Honeywell has trained its commercial data processing field support staff to furnish the applications-oriented service required by minicomputer users. Recently, this support has been further enhanced by the opening of nine more new service centers. The total solution approach and the level of support should appeal to a wide range of customers.

HEADQUARTERS

Honeywell Information Systems
Computer Controls Division
Old Connecticut Path
Framingham MA 01701

TYPICAL PRICES

Model Number	Description	Monthly Rental $ Short Term	Monthly Rental $ 3 yr.	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE (includes a 716 CPU, real-time clock, auto restart, high-speed arithmetic/base sector relocation, cabinets, and drawers; memory must be ordered separately)				
725-G	General-Purpose Minisystem (with separately priced support)	260	240	7,600	40
725-S	Sensor Based Minisystem (with separately priced support)	625	570	16,700	85
725-M	Modular General-Purpose Minisystem (with separately priced support)	NA	NA	6,000	40
735-G	General-Purpose Minisystem (with bundled support)	393	362	11,800	40
735-S	Sensor Based Minisystem (with bundled support)	758	692	20,900	85
	Memory and CPU Options for Models 725 and 735				
700-1209	8,192 Words of Main Memory (excludes parity)	115	105	3,200	30
700-1210	8,192 Words of Main Memory (with parity)	120	110	3,400	30
700-1220	256-Word ROM (for customer-supplied programs)	—	—	840	18
700-1222	1,024-Word ROM (for customer-supplied programs)	—	—	1,260	18
700-2022	Extended Memory System (for over 32K words of main memory; Model 735 only)	110	100	2,520	20
700-3000	Real-Time Clock/Watchdog Timer	26	23	720	5
700-3010	Direct Multiplex Control Adapter (for max of 8 controllers)	94	85	2,650	18
700-3030	Binary Sync Down-Line Load Option (2,048-word ROM)	53	47	1,480	10
	MASS STORAGE				
700-4510	Fixed-Head Disc Subsystem (64K words; includes control)	347	313	9,825	40
700-4511	Fixed-Head Disc Subsystem (128K words; includes control)	490	442	13,860	55
700-4512	Fixed-Head Disc Subsystem (256K words; includes control)	620	560	17,385	75
700-4513	Fixed-Head Disc Subsystem (512K words)	925	835	25,960	110
700-4710	Removable Disc Storage Subsystem (1.1 million words; Model 735 only)	655	590	18,000	95
700-4720	Removable Disc Storage Subsystem (7.5M words)	1,830	1,220	35,800	180
700-4721	Additional Disc Pack Drive (7.5M words)	1,505	1,005	29,500	125
700-4740	Removable Disc Storage Subsystem (1.1M words)	480	434	12,515	101
700-4741	Removable Disc Storage Subsystem (1.8M words)	575	525	15,000	120
700-4742	Removable Disc Storage Subsystem (3.7M words)	765	695	20,000	160
700-4743	Removable Disc Storage Subsystem (7.5M words)	1,115	1,010	29,000	200
	INPUT/OUTPUT				
	Magnetic Tape				
700-4041/51	Mag Tape Subsystem (7/9-track, 26 ips); includes control and 1 tape unit (add up to three 700-4042 units)	355	325	10,000	95
700-4042/52	Additional Mag Tape Unit for 700-4041	245	225	7,000	70

TYPICAL PRICES (Contd.)

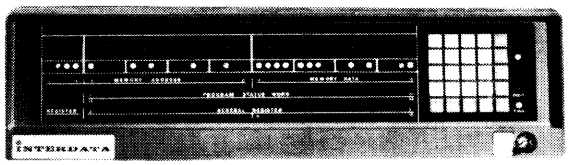
Model Number	Description	Monthly Rental $ Short Term	Monthly Rental $ 3 yr.	Purchase $	Monthly Maint. $
700-4150	Mag Tape Subsystem (9-track, 36 ips)	640	426	12,500	145
700-4180	Mag Tape Subsystem (35 ips, 1,600 bpi)	565	515	15,300	150
700-4190	Mag Tape Subsystem (70 ips, 1,600 bpi)	590	540	17,000	160
	Cassettes				
700-5400	Cassette Tape Subsystem	146	133	3,575	35
700-5401	Additional Cassette Drive for 700-5400	38	35	925	10
	Paper Tape				
700-5010	Reader with Control (300 cps)	114	104	3,200	22
700-5210	Punch with Control (110 cps)	118	107	3,300	20
	Punched Card				
700-5100*	Reader Subsystem (300 cpm)	184	164	6,000	40
700-5123	Reader Subsystem (600 cpm)	327	296	6,000	85
700-5121	Reader Subsystem (800 cpm)	378	342	9,000	86
700-5122	Reader Subsystem (1,050 cpm)	429	388	10,000	113
700-5140	Reader/Punch Subsystem (400-/100-400 cpm)	675	615	20,800	120
700-5141	Punch Subsystem (100-400 cpm)	496	496	17,000	105
700-5151	Reader Subsystem (punched cards, 300 cpm)	170	155	4,350	50
700-5152	Reader Subsystem (punched and marked cards, 300 cpm)	225	205	5,800	55
	Printers				
700-5515	200-lpm Printer Subsystem (96 cols; requires 700-3010)	475	429	12,000	100
700-5516	200-lpm Printer Subsystem (132 cols; requires 700-3010)	605	550	12,000	115
700-5520	300-lpm Printer Subsystem (120 cols; requires 700-3010)	665	605	12,000	165
	Teleprinters				
Note: ASR 33 or ASR 35 is mandatory on all systems for maintenance and warranty purposes. A KSR 33 can be substituted for the ASR on those systems that include a paper tape reader, Type 700-5010, or any card reader.					
700-5300	Teleprinter Interface Only	22	20	840	10
700-5307	ASR 33 Teleprinter with Control	92	87	2,150	40
700-5310	KSR 33 Teleprinter with Control	66	60	1,850	35
700-5507	ASR 35 Teleprinter with Control	184	166	5,200	35
	DATA COMMUNICATIONS				
	Synchronous/Asynchronous Equipment				
700-6312	Sync Single-Line Controller	55	50	1,400	15
700-6316	MIL STD 188C Interface	34	31	570	13
700-6321	Low-Speed Multiline Controller	268	241	6,885	40
700-6322	Universal Multiline Controller	277	250	7,140	40
700-6333	Medium-Speed Multiline Controller	58	53	1,615	10

NA Not Available

Notes: NA Not available
– Not applicable
* Not available on new orders

INTERDATA

7/32 System Report



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OVERVIEW

Interdata's Model 7/32 computer is a microprogrammed 32-bit minicomputer that is at the bottom of Interdata's new 32-bit line; at the same time, it can operate in a 16-bit mode to use application programs developed for Interdata's 16-bit systems. Because it uses a 32-bit word, the 7/32 can directly address 1 million bytes of memory and can handle higher-precision arithmetic operations than the 16-bit line. The 7/32 is a processor designed for the top end of the minicomputer market, designated by Interdata as the "mega-mini" market.

The 7/32 uses memory modules that can store up to 32 kilobytes of core memory on a single circuit board. Memory cycle time is either 750 or 1,000 nanoseconds for 2 bytes. Maximum memory capacity is 1,048,576 bytes for the 7/32.

The 7/32 falls between Interdata's 7/16 and 8/32 minicomputers. The 7/16 is a 16-bit machine that can be expanded in the field to a 7/32. The 7/32 can operate in either the 16-bit mode of the 7/16 or the 32-bit mode used exclusively in the faster 8/32.

Interdata's 7/16 is a 16-bit machine with the same basic architecture as the earlier "New Series," but with a larger instruction set and 32K-byte memory boards. The New Series consisted of Models 50, 55, 60, MS-5, 70, 74, 80, and 85; the first four models use special communications instruction sets and the latter four use general-purpose instruction sets. The 7/16 can be field upgraded to a 7/32 by means of a special "stretch 32" option.

The 7/32 uses the same basic architecture as Interdata's earlier computers but with some notable extensions: 32 hardware accumulators, 30 index registers, both multiplexor and selector I/O channels, large multilevel priority interrupt system, I/O Auto Drive Channels, and large instruction set. The 7/32 uses 136 instructions, a superset of the 16-bit New Series and 7/16 instruction set. Like the 7/16, the 7/32 is well suited for communications by virtue of its sophisticated interrupt handling system (up to 1,023 levels). The 7/32 also has a specialized set of standard instructions for data communications applications including code translation, CRC-16, and special character recognition. Table 1 lists the 7/32 mainframe characteristics.

The 8/32 is a 32-bit machine with a full 32-bit bus structure, four-way interleaved memory, 214 instruction set, up to 1 million bytes of directly addressed memory, dual 64-bit lookahead stacks and eight dual stacks of 16 32-bit general registers for user, I/O, and OS programming as well as rapid context switching. The 8/32 uses the same 750-nanosecond core modules (16-bit words) as the 7/16 and 7/32, achieving greater processing speed by virtue of the four-way core interleaving, the lookahead stacks, and 32-bit wide memory bus.

Table 1. Interdata Model 7/32: Processor Characteristics

Central Processor	
Type	Microprogrammed
No. of Internal Registers	32 (2 stacks of 16)
Use	general purpose; 30 indexable
No. of Instructions	
Standard	136
Optional	17
Fixed-Point Arithmetic	
Add/Subtract	Std
Multiply	Std
Divide	Std
Add time (μsec)	3.25 to 3.75
Floating-Point Arithmetic	Opt
Addressing	
Direct (16-bit half-words)	524,288 (1M bytes)
Indirect	No
Indexed	Yes (2 levels)
Max I/O devices	1,023
Priority Interrupt System	
Lines	8
Levels	1,023
Memory	
Type	Core
Word length (bits)	32 (two 16-bit fetches)
Cycle time/word (μsec)	0.75; 1.0
Capacity (16-bit half-words)	
Max	524,288
Min	8,167
Increment	2K, 4K, 8K
Parity	Opt
Protect	Opt
ROM	Std
Use	Microinstructions (control store)
I/O Channels	
Programmed I/O	Std (Auto Drive Channels)
Direct Memory Access	Std
No. of channels	7
Multiplexed I/O	Std
Selector Channel	Opt
Over DMA	2.6M
Over selector channel	2.0M

Software for the 7/32 includes two new operating systems, OS/32ST, a serial (batch) processing system, and OS/32MT, a multiprogramming real-time system. Language processors for the 7/32 include FORTRAN V, the CAL assembler common to both 32-bit and 16-bit lines, and BASIC. The 7/32 was first delivered in August 1974.

PERFORMANCE AND COMPETITIVE POSITION

The 7/32 is at the bottom of Interdata's 32-bit line, a line extending from minicomputer power at the level of the Digital PDP-11/40 and Data General ECLIPSE all the way up to the middle of the IBM System/370 line with the 8/32. The system will not impact the small-to-medium computer market that used to be the exclusive property

of the large mainframe manufacturers however, because the larger computer manufacturers offer software support and custom programming that puts them in another league. With the 7/32 competing against 16-bit systems in the minicomputer market, Interdata stresses not only cost but inherent software advantages over its competitors due to use of the 32-bit word. The 7/32 can address all large memories directly. Unlike 16-bit word computers, it does not require a memory management hardware unit to convert virtual memory addresses to physical addresses for memories beyond 64K addresses. The advantage is programming simplicity and easy-to-implement operating systems.

In addition, the 32-bit word restricts program size only to that of physical memory and not to the size of the largest virtual memory segment. Virtual addresses need not be converted to physical addresses via a memory management unit. This process slows down program execution time by lengthening memory access time and by increasing the operating system overhead for loading and maintaining memory mapping registers. Also, a real-time operating system is easier to develop when the system does not require a management unit, and it needs less memory for its implementation. Other minicomputer manufacturers, MODCOMP, for instance, have 32-bit machines, but so far, Digital and Data General are still using 16-bit lines. Part of the reason for staying with the 16-bit word is the cost of developing new software. Nevertheless, many industry observers feel that it will not be long before most mini makers will produce 32-bit systems (and cut into the market for big computers).

Interdata has produced both of the 7/32's operating systems on schedule, and this factor has considerably strengthened the system's original position vis-a-vis the minicomputer giants. Although addressing a large market with the 7/32, this market will be expensive to compete in, because of the strong systems already available. Interdata must develop considerable software to compete successfully. Having a larger system to offer users who are moving up strengthens the company's position. The 7/16 is now the entry-level system; users can then advance to the 7/32 for medium-range processing power, or go all the way to the powerful 8/32. The market range for Interdata computers is quite broad; not only have the 7/32 and 8/32 increased the size of the market for which these computers are applicable but they protect the firm's customer base from wandering as their processing needs increase.

Configuration Guide

The basic Model 7/32 system consists of a central processor with 136 instructions that include hardware multiply/divide, 32K bytes of core memory with cycle time of 0.75 microsecond, power supply, and chassis with 16 slots. The central processor uses three circuit boards, and each 32K bytes of memory uses one board. The 7/32 can be expanded by 32K-byte core memory modules to a maximum of 1,048,576 bytes. Other optional features include floating-point arithmetic, memory protect, power fail/auto restart and display console with hexadecimal display and hexadecimal character keys. The 7/32 uses a 16-bit wide I/O bus and can use the same peripherals as the 7/16. Table 2 lists the available peripheral devices.

Configuration requirements for the operating systems and language processors are described in Table 3.

Compatibility

Although not 100 percent compatible, the Model 7/32 can run application programs developed for the New Series processors and for the 7/16. The 7/32 uses a 32-bit word, but it can run programs in a 16-bit word mode under control of a mode bit in the program status doubleword. It uses the same chassis, power supplies, peripheral controllers, and memory modules used by all the New Series processors.

Table 2. Interdata Model 7/32: Peripherals

Model Number	Description
Punched Tape	
M46-240	300-cps reader
M46-242/250	300-cps reader, 75-cps punch
Punched Card	
M46-230/236	400-/1,000-cps reader
Printers	
M46-204	60 to 200- lpm, 132-col, 64-char set
M46-207/209	200/600- lpm, 132-col, 64-char set
Terminals	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N display, 4,920 char, to 9,600 baud
M46-108	Graphic display, to 9,600 baud, 1,024 x 1,024 point matrix
Magnetic Tape	
M46-400	Dual-drive cassette, 500K bytes/cassette, 1,000-cps xfer rate
M46-460	9-trk, 800-bpi magnetic tape, 45 ips
M46-465-467	9-trk, 1,600-bpi magnetic tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556- or 800-bpi (not both) magnetic tape subsystem, 4 drives/controller
Discs	
M46-410	2.5M bytes, 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0M bytes, fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0M bytes, 2316-type disc pack, 4 drives/controller
Process I/O	
M48 series	Wide-range analog input, up to 512 channels
M48 series	High-speed low-level analog input, up to 64 channels
M48 series	High-level analog I/O, up to 8 differential or 16 single-ended inputs
M48 series	Real-time analog controller, two 32-word solid-state buffer memories
M07/M48	Digital multiplexor subsystem, 2,048 input & 2,048 output lines
Communications	
M10-022	Auto dial units, 4-lines
M11-200	IBM 360/370 interface multiplexor (burst or block modes) channel
M47-000/001	Bell-type adapters, 201/301, to 9,600/40,800 baud
M47-100	Async line module controller, up to 92 lines, to 1,800 baud
M47-101/102	Programmable single-line module/adapter for Bell 103 & 202

Table 3. Interdata Model 7/32: Software

Package	Description
OS/32 MT	Real-time multiprogramming, multitask operating system, up to 255 priority levels; requires 32-bit Interdata computer, 65K bytes of memory, operator console, TTY, memory protect, clock
OS/32ST	Serial task operating system, upward compatible with OS/32MT; requires 32-bit processor, 65K bytes of memory, operator console, TTY
FORTRAN V	ANSI x 3.9 - 1966 FORTRAN IV with extensions including ISA calls, requires 32-bit CPU, 8K bytes of memory above operating system requirements, operator console, TTY
CAL	Common Assembly Language for both 16-bit and 32-bit systems; requires 8K bytes of memory above operating system requirements on 32-bit CPU, console, TTY
BASIC	Extended Dartmouth BASIC, for single user; requires 32-bit CPU (in 16-bit mode), 10.5K bytes of memory above operating system requirements, console, TTY

The 7/32 programs are upward compatible with those of the 8/32.

MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase-only basis. Users can negotiate separate maintenance contracts for on-site engineers (1, 2, or 3 shifts) or they can take damaged boards to a repair depot. Maintenance service can also be obtained on a per-call basis.

Interdata has offices in more than 34 locations in the United States and Canada as well as in Japan, Australia, Great Britain, and Germany.

HEADQUARTERS

Interdata
2 Crescent Place
Oceanport NJ 07757
(201) 229-4040

TYPICAL PRICES

Model Number	Description	Purchase $*	Monthly Maint. $
	MODEL 7/32 GENERAL PURPOSE PROCESSOR		
	32-bit processor capable of directly addressing 1,000,000 bytes of main memory; includes 32 GP Reg, each 32 bits wide, high-speed multiply/divide, DMA connection, privilege instruction detect, 1,024 hardware vectored interrupt levels, up to 1,024 automatic driver channels and autoload bootstrap instruction for initial loading		
M73-023	Model 7/32 Processor with 32,768 Bytes of Core Memory (750 nsec, 16-slot chassis, and power supply)	9,950	110
	MODEL 7/32 PROCESSOR OPTIONS		
M73-100	Power Fail Detection/Auto Restart	400	2
M73-101	Floating-Point Hardware	3,900	30
M73-103	DMA Buffer	350	5
M73-104	Memory Access and Protect Controller	3,500	25
M73-105	Extended Memory Selector Channel	1,000	10
M73-106	Local Memory Bank Interface	5,900	50
M73-107	Processor Parity Control	1,000	–
M71-101	Binary Display Panel	300	2
M71-102	Hexidecimal Display Panel	600	5
M70-104	Loader Storage Unit controller	500	10
M70-105	128-Byte Storage Module	100	–
M48-005	Multiplexor Bus Buffer	900	5
	MODEL 7/32 MEMORIES		
M71-300	8,192-Byte Memory Expansion Module (1-μsec core cycle time)	2,000	20
M71-302	16,384-Byte Memory Expansion Module (1-μsec core cycle time)	2,650	30
M71-304	32,768-Byte Memory Expansion Module (1-μsec core cycle time)	3,950	40
M73-306	M71-304 with 750-nsec core cycle time	4,500	45
M71-301	M71-300 with parity	2,500	20
M71-303	M71-302 with parity	3,150	30
M71-305	M71-304 with parity	4,450	40
M73-307	M73-306 with parity	5,000	45
	SYSTEM MODULES		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	600	5
M48-001	8-Line Interrupt Module	900	5
M48-002	General Purpose Interface Board (15 inches)	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,500	10
M48-107	Extension Cable Kit, 25 feet	175	–
M48-018/9	Manual Control Panel for I/O Bus Switch	200	–
	DISC		
M46-410	2.5M-Byte Removable Cartridge Disc System	10,000	80
M46-414	2.5M-Byte Removable Cartridge Disc System	10,100	80
M46-411	2.5M-Byte Removable Cartridge Disc Expansion Drive	5,500	50
M46-420	Removable Cartridge Disc Interface (for use with up to four 2.5M-byte disc drives)	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	–
M49-027	Expansion Power Supply for Single Drive Disc	600	–
27-039	2.5M-Byte Removable Cartridge Disc Pack	200	–
M46-416	10M-Byte Removable Cartridge Disc System	12,000	120
M46-417	10M-Byte Removable Cartridge Disc System	12,100	120
M46-418	10M-Byte Removable Cartridge Disc Expansion Drive and Power Supply	8,000	90
M46-419	50-Hz Version of M46-418	8,100	90
M46-421	Removable Cartridge Disc Interface (for use with up to four 10M-byte dual disc drives)	4,000	30
27-056	10M-Byte Removable Cartridge Disc Pack	270	–
M46-429	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	200
M46-430	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	200
M46-431	40M-Byte Removable Cartridge Disc Expansion Drive	17,950	200
M46-432	40M-Byte Removable Cartridge Disc Expansion Drive	18,100	200
M46-433	Removable Cartridge Disc Controller (for use with up to four 40M-byte disc drives)	7,000	50
M46-434	40M-Byte Removable Cartridge Disc Pack	500	–
	TELETYPE CONSOLES		
M48-010	ASR Model 33/35 TTY Interface (with internal cable)	350	5
M46-000	ASR Model 33 Teletypewriter (with external cable)	1,450	40
M46-002	50-Hz Version of M46-000	1,550	40
M46-001	ASR Model 35 Teletypewriter (with external cable)	4,200	40
M46-003	50-Hz Version of M46-001	4,300	40
	PAPER TAPE EQUIPMENT		
M46-250	Combination Paper Tape Reader/Punch Interface	900	10
M46-240	Paper Tape Reader, Uni-directional (300 cps)	1,300	20
M46-241	50-Hz Version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch (300/75 cps)	3,300	40
M46-243	50-Hz Version of M46-242	3,400	40
	PUNCHED CARD		
M46-235	Card Reader Interface (with internal cable)	900	10
M46-234	Hardware Hollerith to ASCII Conversion Option	350	–
M46-230	Card Reader (400 cpm; includes external cable)	3,000	40
M46-231	50-Hz Version of M46-230	3,100	40
M46-236	Card Reader (1,000-cpm; includes external cable)	5,900	80
M46-237	50-Hz Version of M46-236	6,000	80
	PRINTERS		
M46-202	Line Printer Interface (and internal cable for 60 to 200 lpm line printer)	500	10
M46-204	Fully Buffered Line Printer (60 to 200 lpm, 132 cols, 64 char set; includes external cable)	5,000	50
M46-205	50-Hz Version of M46-204	5,200	50
M46-206	Line Printer Interface (and internal cable for 200 or 600 lpm line printer)	750	10
M46-207	Full Buffered Line Printer (200 lpm, 132 cols, 64 char set; includes external cable)	12,350	90
M46-208	50-Hz Version of M46-207	12,650	90
M46-209	Fully Buffered Line Printer (600 lpm, 132 cols, 64 char set; includes external cable)	17,150	110
M46-210	50-Hz Version of M46-209	17,450	110
	MAGNETIC TAPE		
M46-400	INTERTAPE (cassette system with dual transports, 1,000 char per sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface)	4,200	30

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $*	Monthly Maint $
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface (interface controls up to 4 IBM compatible continuous read-after-write 45 ips drives; includes cyclic redundancy check hardware and read-after-write check)	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-461	50-Hz Version of M46-460	6,100	90
M46-473	7-Track, 556 bpi Magnetic Tape Transport Interface	2,900	20
M46-474	7-Track, 800 bpi Magnetic Tape Transport Interface	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport	6,000	90
M46-477	50-Hz Version of M46-476	6,100	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	–
M46-475	9-Track, 1,600 bpi, Magnetic Tape Transport Interface (controls up to 4 IBM compatible, continuous read-after-write 45 ips drives via a phase-encoded formatter supplied with M46-465 or M46-466)	1,500	10
M46-465	9-Track, 1,600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase Encoded Formatter (continuous transfer rate is 72,000 char/sec)	12,000	120
M46-466	50-Hz Version of M46-465	12,100	120
M46-467	9-Track, 1,600 bpi, 45 ips, Magnetic Tape Expansion Transport (for use with M46-475 and M46-465)	6,800	80
M46-468	50-Hz Version of M46-467	6,900	80
	VIDEO DISPLAY		
M46-107	1,200 Baud Local Current Loop Interface (with internal cable)	400	5
M46-100	Alphanumeric Video Display Unit (1,920 char (24 lines x 80 char); std 64-char ASCII subset; 110 or 1,200 baud via current loop interface; up to 9,600 baud with RS-232C)	2,250	30
M46-101	Std 50-Hz Version of M46-100	2,350	30
M46-102	M46-100 with complete processor and operator cursor control, a full range of editing features, and message and character modes	3,350	40
M46-103	50-Hz Version of M46-102	3,450	40
M46-108/9	Graphic Display Terminal	6,500	60
M46-104/5/6	External Cable Assembly	–	–
	DATA COMMUNICATIONS SYSTEMS MODULES		
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter (for 103/202 data set or local RS-232 terminal)	400	5
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	550	–
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable (for RS232 compatible data sets)	60	–
M10-056	Data Set Cable (for Bell 301 type data sets)	350	–
M47-200	IBM 360/370 Parallel Interface (single address interface)	3,500	50
M47-201	IBM 360/370 Parallel Interface (multiple address (up to 256) interface)	5,000	60
	CABINETS, CHASSIS, AND POWER SUPPLIES		
M49-020	System Chassis	700	–
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 to 15 inches)	150	–
M49-004	System Cabinet	650	–
	SOFTWARE**		
S90-000-16	BOSS-PLUS Source Paper Tape and Documentation Package	175	–
S90-001-16	DOS-PLUS Source Paper Tape and Documentation Package	500	–
S90-002-46	RTEX Source Card and Documentation Package	1,500	–
S90-003-26	RTOS Source Cassette and Documentation Package	2,000	–
S90-004-26	OS/16 MT Source Paper Tape and Documentation Package	950	–
S90-005-11	OS/32 ST Source and Object Paper Tape and Documentation Package	750	–
S90-007-11	OS/32 ST Object Paper Tape and Documentation Package	300	–
S90-006-41	OS/32 MT Source Card and Object Paper Tape and Documentation Package	3,000	–
S90-009-21	OS/32 MT Object Cassette and Documentation Package	2,500	–

* Quantity discounts are available on most items. NA Not Available – Not Applicable

**Additional Software Documentation Packages available.

INTERDATA

7/32 Detail Report

MAINFRAME

The orientation of the Model 7/32 is toward real-time applications that require priority-oriented multiprogramming. This is supported by the OS/32 MP real-time multiprogramming operating system. Batch processing is also accommodated with the OS/32 ST serial task operating system. Both systems support FORTRAN V and BASIC.

The 7/32 has hardware facilities for multiprocessing but does not yet offer special software support for multiprocessor configurations.

Central Processor

An LSI-bipolar ROM stores the microprogram that implements the processor's arithmetic, logical, control, and I/O functions. Microinstructions are 24 bits long and their average execution time is 250 nanoseconds. The processor operates under control of a 64-bit program status doubleword that defines current processor status. This includes:

- Location counter — 24 bits.
- Fullword Condition Code (4-bits) reflects results from operations using 32-bit operands; carry/borrow, overflow, greater than zero, or less than zero.
- Halfword condition code (4-bits) reflects results from operations using 16-bit operands.
- Relocation/Protection Enable.
- Register set in use.
- Wait state.
- External Interrupt Enable.
- Machine Malfunction Interrupt Enable.
- Fixed-point Divide Fault Interrupt Enable.
- Extended Mode — specifies 16-bit or 32-bit word operation.
- Floating Point Arithmetic Fault Interrupt Enable.
- System Queue Service Interrupt Enable.
- Protect Mode.
- Other bits unused.

Control instructions are provided to load, store, or exchange PSWs with one instruction so context switching is relatively easy and fast.

Data Structure. Table 1 lists the data formats used by the processor.

Special Registers. Model 7/32 is organized around sets of 16 general-purpose registers, 15 of which can be used as index registers. The 7/32 has two of these sets, one for user programs and the other for I/O operations. The general-purpose registers are 32 bits long.

Addressing Facilities. The processor can address all of main memory directly. In addition, it can index addresses by one of the 15 index registers, and perform indirect addressing.

Table 1. Interdata Model 7/32: Data Structure

DATA NAME	REPRESENTATION
Byte	8 bits
Halfword*	16 bits
Word	32 bits
Instructions	16, 32, 48 bits
Binary Operand	31 + 1 sign bit; 15 + 1 sign bit in 16-bit mode
Floating-Point Operand	Fraction 24 bits + sign; exponent 7 bits

*Interdata has always considered words 32 bits long and halfwords 16 bits long.

Instruction Set. The 7/32 instruction set is a superset of the New Series instruction set containing as standard some New Series options, such as hardware multiply/divide. Optional instructions include floating point arithmetic, fix and float, and bit manipulation instructions.

The 7/32 uses the same four instruction formats as the New Series: register-to-register (RR), short format (SF), register to indexed memory (RX), and register immediate (RI), plus four additional formats. The RX format is expanded into three formats: RX1, RX2, and RX3.

The RX format provides an 8-bit operation code, a 4-bit accumulator selection code, a 4-bit index register selection code, and a 16-bit address. The RX1 and RX2 formats are the same as RX except the address field contains a 14-bit absolute address for RX1 and a 15-bit relative address for RX2. RX3 format uses 48 bits. It uses the same fields as RX but extends the address to 24 bits and includes a second 4-bit index register selection code so that addresses can be indexed by the contents of a second index register.

The 7/32 also uses a second RI format that uses a 48-bit instruction and generates a 32-bit operand. Table 2 lists some typical instruction execution times.

Interrupt Control. The interrupt system is controlled by a vector table that is addressed by the interrupt level. The maximum number of interrupt levels is 1,023. The automatic response to an interrupt is to look up the address of the software routine associated with the interrupt in the vector table.

The processor hardware sequence requires a minimum of 6.5 microseconds to identify an interrupt and to switch context for the Model 7/32. Because it has two sets of general-purpose registers, one for user programs and one for the I/O system, the 7/32 need not store and restore the internal registers before and after the interrupt service routine.

Table 2. Interdata Model 7/32: Typical Instruction Execution Times

INSTRUCTIONS	EXECUTION TIME (μsec)[1] 7/32
Load/Store	3.5 to 3.75
Fixed Point Binary	
Add/Subtract	3.25 to 3.75
Multiply	16 to 16.5
Divide	100
Floating Point[2]	
Add/Subtract	15 to 25
Multiply	32 to 34
Divide	55 to 57
Logical	3.25 to 3.75
Branch	1.5 to 2.0
Shift	3.0 + .25 (n-1)[3]
Compare	5.75 to 6.25
I/O	4.5 to 5.0

Notes:

(1) Using memory with 750-nanosecond cycle time and RX format.

(2) Using hardware floating point arithmetic.

(3) N equals number of positions shifted.

An Auto Drive Channel is available for each of the 1,023 interrupts. These channels handle I/O with software intervention usually required only for special cases or end conditions. The Auto Drive hardware includes features like CRC-16 and LRC checking and generation, code translation, and special character recognition.

Main Storage

Main storage consists of core memory modules of up to 1 million bytes for the Model 7/32. Memory is available in four modules: 8K or 16K bytes with 1-microsecond cycle time and 32K bytes with 1-microsecond or 750-nanosecond cycle time. Memory parity check with interrupt is optional.

The Model 7/32 memory protect option is implemented by a memory access controller that contains 17 32-bit hardware registers used to segment, relocate, and protect user programs. It allows seven memory protect states: no access, no protection, read and write but no execute, read and execute but no write, read only, nonpresence, and trap after first write.

I/O Control

The I/O bus for both systems is 16 bits wide, and data transfers can consist of either eight or 16 bits.

Data can be transferred one or two bytes at a time under program control at a rate of about 88K bytes per second on the 7/32.

Blocks of data can be transferred under multiplexor channel program control at a rate of 360K bytes per second.

The 7/32 has one standard DMA channel. An optional DMA multiplexor is available for the 7/32 for the addition of DMA channels. Transfer rate over DMA is 2.6 million bytes per second. A selector channel is optional on the 7/32.

PERIPHERALS

Interdata provides a broad range of slow-speed, mass-storage, and special-purpose peripheral devices for its computers. All input/output devices communicate with the processor through the multiplexor channel. Some devices such as highspeed discs transfer only control information over the multiplexor channel, and use a selector channel for direct data transfers to or from memory.

Slow-Speed Peripherals. Interdata offers four Teletype consoles, paper tape and card readers, a combination reader/punch, and a line printer.

TELETYPE CONSOLE

M46-000 Teletypewriter (Teletype Model 33 ASR) — 10 cps, connects to the system by the multiplexor channel; for basic processor of all models; requires M48-010 interface.

M46-001 Teletypewriter (Teletype Model 35 ASR) — 10 cps, connects to the system by the multiplexor channels; for basic processor of all models; requires M48-010 interface.

PUNCHED TAPE

M46-240 Paper Tape Reader — 300 cps, connects to the system by the multiplexor channel; requires M46-250 interface.

M46-242 and M46-250 Combination Reader/Punches — 300 cps (read), 75 cps (punch), connects to the system by multiplexor channel; requires M46-235 interface.

PUNCHED CARD

M46-230 Card Reader — 400 cpm, connects to system by multiplexor channel; requires M46-235 interface.

M46-236 Card Reader, like the 230 but 1,000 cpm.

DISCS AND DRUMS

M46-410 Cartridge Disc with 1 x 4 Controller — storage capacity 2.5M bytes per disc unit; transfer rate 195K bytes/sec; avg access time 70 msec; movable head disc; disc expansion drive available; up to 3 expansion units can be added.

M46-411 Removable and Fixed Cartridge Disc Drive — storage capacity: 2.5M bytes, expansion drive for M46-410.

M46-416 Removable and Fixed Cartridge Disc Drive System with 1 x 4 Controller — storage capacity 10M bytes: avg access time 38 msec; transfer rate 310K bytes per sec, controller can handle up to 4 drives.

M46-418 Removable and Fixed Cartridge Disc Drive — storage capacity 10M bytes; expansion drive for M46-416.

M46-429 Removable Disc Pack Drive — storage capacity 40M bytes, 2314-type dual density disc pack, 35 msec avg. access, 310K bytes per sec transfer rate.

M46-431 — Expansion drive for M46-429.

Special-Purpose Devices. Special-purpose equipment includes analog/digital and digital/analog conversion equipment and a digital multiplexor subsystem.

DIGITAL MULTIPLEXOR SUBSYSTEM

M07-860 Digital Multiplexor Controller plus first expansion chassis (M07-864) — universal interface for both input and output scanner modules; can control up to 16 M07-861 and 16 M07-862 Modules; M07-861 is 128-line Input Module; M07-864 is 128-line Output Module.

Wide Range Analog Input Subsystem — speeds of 40, 100, or 200 samples/second; 13- or 15-bit resolution, programmable gain, 2.5mv to 10.24v; up to 512 channels.

High-Speed Low Level Analog Input Subsystem — up to 8,000 samples/second; 12-bit resolution, programmable gain, 5 mv to 1v; up to 64 channels.

High Level Analog I/O with up to 8 differential or 16 single-ended inputs — sample rate of 10,000 samples/second with 12-bit resolution.

DATA COMMUNICATIONS

Interdata produces four "New Series" computers designed specifically for data communications applications: Model 50, 55, 60, and MS-5. These computers are variations of Model 70 or 80 with a data communication instruction set added. Models 50 and 60 have a single-processor configuration, while Model 55 features dual processors. Models 50 and 55 are based on Model 70 with extensions, while Model 60 is based on the faster Model 80, again with extensions. The MS-5 is a turnkey store-and-forward message switching system. Data communications instructions that separately define these systems on the New Series are standard features to the 7/32.

Interdata supplies a variety of data communication facilities for the New Series and the 7/32, including Bell data set adapters for half- and full-duplex, synchronous and asynchronous operation. All can be added to the 7/32. Interdata also supports automatic dial unit controllers that provide fully buffered interfaces and program control of the Bell 801 (A/C) Data Auxiliary set and permit calling any telephone number in the switched network.

ADAPTERS

M47-000 Data Set Adapter — speeds to 9,600 baud, for Bell 201 or equivalent; half-/full-duplex sync; double-char buffered operation.

M47-001 Data Set Adapter — speeds to 40,800 baud, for Bell 301 or equivalent; half-/full-duplex sync; double-char buffered operation.

M47-102 Programmable Async Single Line Adapter — speeds to 75-9,600 baud, for Bell 103/202; half-duplex async; selectable char format.

M47-100 Async Line Module Controller — speeds up to 1,800 baud, for Bell 103/202; half- or full-duplex async; provides interface and control logic for up to 92 async lines; allows four selected clock rates for M47-101.

M47-101 Programmable Async Line Module — for Bell 103/202 half- or full-duplex interface for four async lines; selectable baud rate per line (one of four) and char format.

M10-022 Automatic Dial Unit Controller — provides fully buffered interface and program control of Bell 801 (A/C) Data Auxiliary set; permits calling any telephone number in the switched network; controls 4 lines.

M11-200 360/370 Interface Unit — provides multiplexor channel interface to IBM 360/370 systems, in Multiplex Burst or Block Multiplex modes.

TERMINALS

M46-102 Alphanumeric Video Display — 80 char/line; 24 lines; 110 to 9,600 baud rate message and char modes, editing features.

M46-100 Alphanumeric Video Display — 80-char/line; 24 lines; 110 to 9,600 baud rate meant as replacement for Teletype terminal.

M46-108 Graphic Display Terminal — 1,024 x 1,024 matrix, 2,590 char display (35 x 74), to 9,600 baud.

SOFTWARE

Software for the 7/32 consists of two operating systems, the OS/32-MT real-time multiprocessing system and OS/32 ST serial tasking batch system. Language processors include an assembler with versions in common for both 16-bit and 32-bit lines, FORTRAN V, and BASIC. Application programs developed on the 16-bit systems can run on the 32-bit computer for the most part, but systems software is not transferable.

Operating Systems

OS/32 MT. The OS/32-MT brings some large-scale mainframe software features to the minicomputer user through the use of a command processor, and it provides a complete interface to all real-time programs written in FORTRAN V. Interdata states that the 7/32 was designed with the software concepts in mind from the system's inception and this enabled the designers to include features in the software to make the end user's implementation easier. Interdata asserts that OS/32-MT requires 25 percent less core space than similar operating system packages implemented on extended memory systems with memory management units. Because of the 32-bit word the 7/32 user has the power of extended memory without the associated complexity and cost.

The minimum configuration required for the OS/32-MT is the 7/32 processor with 48K bytes of memory, a

memory access controller, console turnkey panel, console TTY, interval clock, and line frequency clock. Hardware allows addressing of up to one megabyte of memory. Total system addressing power is 16 megabytes of core directly. The OS/32-MT can perform the following functions in background operations: on-line compilations (FORTRAN V), assemblies, linking, editing, and on-line task installation. This background facility allows applications to be put on-line while other tasks are developed at the same time.

The OS/32-MT is highly modular; it consists of the following five major divisions:

- Executive — performs system supervisory functions such as memory management, task scheduling and management, internal interrupt handling (power fail, arithmetic fault), and supervisory call processing.
- Command Processor — a table-driven console command interpreter which accepts the user's commands and performs the requested function. A series of previously entered commands can be called by a single macrocommand.
- Resident Loader — fetches tasks or task overlays from disc.
- Input/Output Subsystem — the collection of device drivers or I/O handlers for the system's peripherals.
- File Management System — executes buffer control and allocation, volume label checking, file access, and file utility functions.

The Operating System provides facilities in a real-time environment for Task and Memory Management and File Management.

Task and Memory Management. These facilities create, schedule, and execute tasks. They communicate with the Task and provide special services for it. At the same time, they provide for efficient memory utilization. The user can choose one of three source codes: FORTRAN V, LEVEL I source, or Common ASSEMBLY Language. Tasks are established through the Task Establisher Task (TET), which can also be used to define an overlay structure for tasks. Each task is assigned a priority; 255 levels of priority are available and round robin scheduling allows many tasks to share one level. Tasks can be added or deleted by this program. A Memory Access Controller (MAC) handles shareable and nonshareable program or data segments to achieve efficient memory utilization. The Dynamic Relocatability feature of MAC allows an overwritten task to be restored to another area of core. A free memory list operates as a directory to the available 256-byte blocks, in order of increasing memory addresses. Freed blocks return to their original position in the list. The Executive determines when a task should be run. It locates the task, searches for available core of the proper size, and transfers the task from disc to core. All tasks are maintained on disc in core image format for fast loading. Memory Access and Protect hardware allow the task to be treated as a contiguous block of memory, even if its physical location is not contiguous. The Executive remembers the termination point of a lower priority task when a higher priority task usurps control. The first task continues from the termination point when the processor is available.

File Management. The following five functions are provided by file management:

- Named files and devices, using a 4-character volume identifier (VOLID), an 8-character file name, and 3-character extension.
- Three file organizations:
  - — Chained file structure processes logical records which are blocked and deblocked automatically. Sequential and random access modes are provided, but the structure is designed for heavy sequential use.
  - — Indexed file structure allows rapid access to individual data blocks. Blocking is similar to chained structure when the file is opened as a buffered file. When opened as an unbuffered file, it is similar to a contiguous file, except it is open-ended; thus records can be appended.
  - — Contiguous structure processes large blocks of data of variable length. This structure is used when direct, physical input/output is required.
- File protection at the file level is provided by write/read keys in the file itself; at the task level access privilege commands are set to trap illegal handling. This allows files to be shared either at a departmental level or a functional level within the department. System calls (or supervisor calls) and console commands facilitate file manipulation to open, close, delete, rename, reprotect, or allocate files. A set of privileged instructions — read only, read-write data access, and execute-only access constraints — provide system protection. Automatic power fail/recovery procedures monitor the total system and protect it against power failure.
- System calls allow the user to manipulate files. The calls perform the following functions:
  - — I/O operations.
  - — Service functions (log messages, interval wait, allocate memory, peek).
  - — End job.
  - — Fetch overlay.
  - — Call task.
  - — File handling functions.
  - — Simulated interrupts.
  - — Intertask communication/coordination.
  - — User-defined calls within the task.
- Console Commands allow the user to control the real-time environment as well as OS/32-MT. The Command Processor builds files of user commands, which can be recalled at a later date by the use of a macrocommand. Operator commands may be entered from any device on the system.

OS/32 ST. The serial tasking operating system, which is intended for batch processing and program

development, has many features in common with OS/32 MT. It includes a comprehensive file management system, as already described for the OS/32 MT, and a comprehensive operator command language as well as a macrocommand processor to customize operator commands. Program development support includes an editor, loader, debugger, and other utilities, FORTRAN V LEVEL 1, and the Common ASSEMBLER Language.

OS/32 ST requires a 32-bit processor, 32K bytes of memory, Operator Console, and TTY.

Language Processors

FORTRAN V LEVEL 1. The FORTRAN V package, which is designed to run under any operating system, uses an extended FORTRAN IV language that conforms to ANSI x 3.9-1966 specifications but, in addition, supports ISA calls. It allows a mix of FORTRAN statements and in-/line assembly code. Purdue ISA real-time extensions are included as well as bit and byte manipulation, complex and double precision (64-bit) arithmetic, and reentrant run time library routines.

FORTRAN V requires 16K bytes of memory above operating system requirements, a console, and TTY.

BASIC. Interdata's BASIC is a single user version conforming to the Dartmouth standard BASIC. Extensions provide matrix operations, string operations, and Boolean operations. In addition, statements such as LET, IF, INPUT, ON, PRINT, USING, CALL, and DIMENSION are available to the user.

BASIC is supplied in relocatable format on paper tape. The package is supported under BOSS, DOS, and RTOS. With BOSS a system of 8K words is required, with DOS a system of 12K words is needed, and with RTOS a system with 16K words is needed.

Assembler. The assembler is a 1-, 2-, or 3-pass assembler; the number of passes is specified in an option control statement. Normally, program assembly requires two passes. The first pass develops the symbol table; the second provides a listing, and a punched object tape. A third pass is required only if the hardware configuration does not allow punching and printing on the same pass.

The assembler provides one-to-one assembly of the Interdata instruction list as well as 44 extended branch mnemonics and pseudo-operations to define symbols and data, and to control the assembly. Object code is in relocatable binary format. Data can be defined as alphanumeric (7-bit ASCII code), hexadecimal, 16-bit binary, decimal, and address; or as floating-point single or double precision. The assembly lists one of eight error codes for statements in error and for symbol table errors. It also lists I/O device error messages when I/O devices malfunction.

INTERDATA
Model 8/32 MEGAMINI TM

OVERVIEW

After flirting with 32-bit word architecture for the past year and a half with its 7/32 system, Interdata has now "tied the knot" with the official introduction of the 8/32 Megamini. With the exception of the I/O buses, which are 16 bits wide to maintain compatibility with standard peripherals, the Megamini uses a 32-bit architecture throughout: arithmetic unit, internal registers and memory bus. The memory modules are the same ones used with the 7/32 and 7/16 systems, but two 16-bit word modules operate in tandem over two 16-bit wide buses to make up the 32-bit word.

The name Megamini highlights the wedding of a megabyte of memory to a minicomputer. It may also connote a "great or large minicomputer." Certainly, Interdata considers it an important product, and it is the first system introduced since Interdata's acquisition by Perkin-Elmer. President Daniel Sinnott called it "the most powerful minicomputer in the world today" and indicated it fit in the computer market at "precisely the point where the traditional minicomputer market intersects the large scale mainframe market."

TM-Trademark of Interdata.

The 8/32 Megamini features dual 64-bit lookahead stacks, multiple sets of internal registers for fast context switching, dual I/O buses, two-way memory interleaving, bit, byte, halfword, full word, and multiple-word instructions, floating-point hardware, and 240-nanosecond processor cycle time.

Memory

The Model 8/32 Megamini memory bus controller contains dual lookahead stacks, each 64 bits long. When a word is read out of memory, the stacks are loaded with the word in the next memory location. When a word is accessed from memory, the lookahead stacks are first checked to determine if the word is there.

Each 32Kb memory module operates independently of all other modules. Thus, a second memory read access to another module can overlap the write portion of a memory cycle. This makes the effective memory cycle time 300 nanoseconds.

Central Processor

The Model 8/32 processor includes two sets of 16 32-bit internal registers as a standard feature. Six extra sets of 16 internal registers are optional. They can be assigned to the operating system, to the I/O system, or to the user programs for rapid context switching among programs in a multiprogramming environment.

Addressing is to the byte level. The 32-bit word allows for 22-bit addresses, thus instructions can address up to four million bytes although memory is currently restricted to one million bytes.

The Memory Access Controller (MAC) uses a stack of 16 32-bit registers which are accessed by the 4 most significant address bits. Thus, memory is divided into 64K-byte segments for relocation purposes. Each relocatable memory module is 256 bytes long. The relocation register contains

12-bit fields to define the source limit and the relocation address, and one 4-bit control field. One bit indicates the module is not in memory, one indicates write protected, one indicates execute protected, and one is unused except for bookkeeping.

The user can program as though all of real memory, up to 1 million bytes, is available to a program, leaving it to the operating system to allocate memory space.

The instruction set consists of 214 instructions, which comprise a superset of the 7/16 and 7/32 instruction sets. A full set of arithmetic instructions are provided to operate on halfwords (16 bits) as well as full words (32 bits). List, byte handling, bit manipulation, and communications instructions are standard. Both single and double precision floating point arithmetic instructions are optional. Table 1 lists some typical instruction execution times.

Input/Output

The two I/O buses are the multiplexor bus for slow speed devices controlled by ROM-implemented auto driver channel programs, and the DMA bus. Up to 7 selector channels can be used on DMA with 16 devices per channel. Maximum transfer rate is 62.5Kb per second via the multiplexor bus and 6Mb per second via DMA.

The Model 8/32 Megamini can run under the OS/32 ST for batch program development and under OS/32 MT, a multitasking operating system, delivered in December 1974 for the 7/32. FORTRAN V, Level II is available for program development as well as Macro CAL, the assembler language common to all Interdata computers. Basic is available as a compiler or as an interpreter.

The Model 8/32 is designed using medium and large scale integration technology and high-speed Schottky logic. Interdata has gone to 15-inch, reinforced, multi-wire

Table 1. Interdata 8/32 Megamini: Comparison with Other Computer Systems

	Interdata 8/32	Digital PDP-11/70	Data General ECLIPSE 200	XEROX 550	IBM 370/158
Word Length	32 bits	16 bits*	16 bits	32 bits	32 bits
Instruction Times, μsec (Memory to Register)					
Integer Add	1.2	1.8	2.5	1.8	.9
Integer Multiply	3.5	3.9	8.8	6.2	2.0
Integer Divide	5.8	8.3	11.2	14.4	9.9
Floating Point Add	2.3	8.2	5.5	6.1	2.4
Floating Point Multiply	3.0	11.2	7.2	9.1	2.3
Floating Point Divide	5.3	12.2	7.9	23.3	8.9
Hardware I/O	Yes	No	No	Yes	Yes
Max. DMA Rate/Second	6MB	4MB (UNIBUS); 5.8MB (data-channel)	2MB	4MB	6.7MB
Max. Address Capability	1MB	64KB	64KB	1MB	16MB
General-Purpose Registers	8 Stacks of 16 each	2 Stacks of 8 each	1 Stack of 4	4 Stacks of 16 each	1 Stack of 16
Pricing ($)					
CPU + 128KB Memory	51,900	54,600	32,500	128,700	NA
+ 256KB Memory	70,900	68,800	54,100	178,700	NA
+ 512KB Memory	107,400	101,800	NA	278,700	1,779,200
+ 1048KB Memory	179,400	163,800	NA	478,700	1,905,700

*Uses 16-bit operands but data paths between cache and memory and high speed device controllers are 32 bits wide.

boards, away from multi-layer boards, because multi-wire boards have fewer interconnections and less failures than multi-layer boards, and they are easier to repair. Military type pin connectors are used for ruggedness. Plug-in modules are used to allow single fault detection, isolation, and fast repair.

Interdata has stuck to core memories for the 8/32 because they are cheaper, more reliable and more available than MOS memory. Interdata's experience indicates the MTBF on their core is 20,000 hours and only 6,000 hours for MOS memory. MOS memory performance is only 10 per cent higher than 4-way interleaved core modules and triple the cost.

The cost of the basic 8/32 processor with 132K bytes of memory is $51,900 as compared to $23,450 for a 7/32 similar configuration. The performance of the 8/32 should be 2 to 4 times that of the 7/32.

First deliveries of the 8/32 are scheduled for July 1975.

COMPETITIVE POSITION

The Model 8/32 Megamini is a fine addition to Interdata's line of computers, expanding the power and thus the market of its systems upward. Also, users of Interdata's smaller computers have a system to move up to as the need for power expands. The name of the game today is to capture the first time computer user when he enters the market; to maintain the customer base with a diversified compatible supply of computer products reaching up into the medium scale range; and to keep products price/performance competitive by redesigning products around new technologies. The loyalty of computer users to a product line has never been higher, primarily because of the user investment in software. A manufacturer cannot expect to capture very many new customers at the high end of the computer line.

Interdata already has $2,000,000 worth of orders for the 8/32, primarily for aerospace simulation and data communication applications. Because the 8/32 is powerful but low cost, Interdata believes new operations will be computerized for the first time, and this will open markets in the midi range. It remains to be seen how big that market is.

Table 1 presents some comparisons of the 8/32 with other computer systems. Interdata does not supply the same kind of applications software support provided by Xerox and IBM. In fact, Interdata advertises itself as the toolmaker who supplies the tools other people use to perform tasks. The 8/32 Megamini will primarily meet the ECLIPSE and the PDP-11/70 in the market place. The ECLIPSE is quite fast, but it is a 16-bit system. The PDP-11/70 is also a 16-bit computer, but it will be a powerful competitor particularly for applications with any commercial processing. Digital now offers COBOL with the PDP-11/70.

HEADQUARTERS

Interdata
2 Crescent Place
Oceanport, NJ 07757
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PRICE DATA

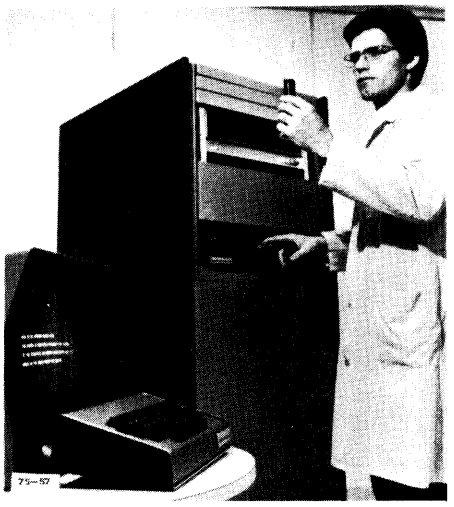
Model Number	Description	Purchase $	Monthly Maint. $
	MODEL 8/32 GENERAL PURPOSE PROCESSOR 32 bit fully parallel processor can Directly Address 1,048,576 bytes of Main Memory, CPU features instruction lookahead stacks and interleaved memory; cycle time 300 ns; includes two sets of sixteen 32-bit GP Regis; 1,024 hardware interrupt levels		
M83-023	Model 8/32 Processor with 131,072 Bytes of 750 ns; Core Memory	51,900	500
M83-101	Single precision 32-bit Floating Point Hardware	2,500	20
M83-102	Hexidecimal Display Panel	300	—
M83-107	Processor/Memory Parity Generation and checking hardware	1,000	—
M83-110	Extended Register Sets for 8/32 Processor Memories*	5,000	20
M84-300	Memory Expansion from 131,072 Bytes to 262,149 Bytes	19,000	180
M83-302	Memory Expansion from 262,144 Bytes to 393,216 Bytes	18,500	180
M83-304	Memory Expansion from 393,216 Bytes to 524,288 Bytes	18,000	180
M83-306	Memory Expansion from 524,288 Bytes to 655,360 Bytes	18,500	180
M83-308	Additional 131,072 Byte memory increments	18,000	180

*Add $1,000 for models with parity.

— Information Not Available

INTERDATA

Update to Report on 16-Bit Computer Model



New Computer Systems

Interdata Corporation has announced two new 16-bit computer systems called the RD800 and RD850 for scientific processing applications; they are based on the firm's Model 80 and 85 computers. Both systems include a central processor with 32K, 48K or 64K bytes of MOS memory, floating point hardware, power fail protect, display terminal and 2.5 bytes of disc storage with interfaces. Standard software includes assembly language, FORTRAN IV, BASIC and disc operating system.

The RD850 system includes 4K words of Dynamic Control Store, Interdata's writable control store module that can be microprogrammed by the user. Both systems feature an average memory cycle time of 270 nanoseconds, 16 general purpose registers (including 15 that can be used as index registers), multiply/divide, floating point arithmetic, and 255 vectored interrupt levels.

Interdata is aiming RD systems at the scientific market; they are well-suited for use in university research, as well as in petrochemical, aerospace and simulation applications and in situations that require high-speed numerical analysis. The RD850, with the Dynamic Control Store module that has a cycle time of 60 nanoseconds, can include user-alterable microprogramming in situations requiring high-speed, specially-designed algorithms.

The operating system features disc file structures supporting named access, blocking and deblocking of input/output, and read/write access protection. Files can be random, sequential and direct physical access types. Catalog procedures can be stored on any device to facilitate batch processing.

The systems are priced from $32,400 for a complete RD800 system with 32K bytes of memory, to $42,525 installed with 6 months maintenance. They are available for immediate delivery.

New Disc Drive

Interdata also has introduced a 2.5 megabyte fixed disc drive system that will be available in July. The system is designed for low cost random access bulk storage and includes the drive mechanism, controller, power supply and IBM 2315 disc or equivalent. The disc controller interfaces to all Interdata 16-bit and 32-bit processors.

Average access time of the disc drive is 70 milliseconds, and the track-to-track access time is 15 milliseconds. The nominal data transfer rate is 195K characters per second. The controller can cross sector and head boundaries, thus data can be transferred in block sizes from 156 bytes to 12,288 bytes.

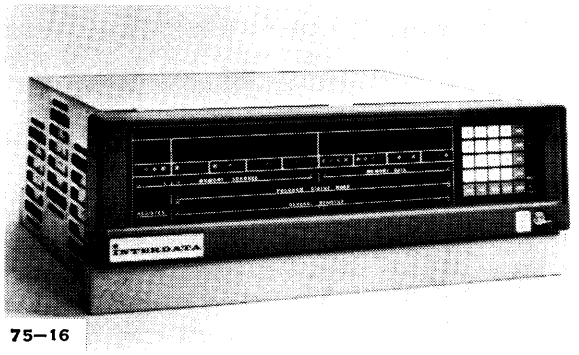
The controller operates with a selector channel for autonomous block transfers. It permits simultaneous seek, overlapping seek and data transfers in multiple disc drive configurations to minimize access time. Hardware error checking is also included.

The disc contains a single platter recorded at 2,200 bits per inch on 203 tracks on each surface. Data on each track is divided into 24 equal sectors, which include four main fields — sync, two-byte header, and 256-byte and 16-bit cyclic check fields.

Purchase price of the new disc system is $7,200 for single units, or $6,192 in quantities of 10 to 14.

INTERDATA

16-Bit Models: 70, 74, 80, 85, and 7/16



75–16

OVERVIEW

Interdata's line of microprogrammed 16-bit computers consists of the Models 70, 74, 80, and 85, the so-called "New Series" (a set of compatible general-purpose systems), and the 7/16, a newer, lower cost 16-bit word system that will eventually replace all the New Series models; the only models currently marketed are Models 70 and 7/16. The Models 50, 55, 60, 270X, and MS-5 are communications systems that have special instruction sets implemented on a Model 70 processor. The 7/16 system can be expanded in the field to the 7/32, the bottom of Interdata's new, developing 32-bit line for large mini and "megamini" systems. The recently announced Model 8/32 is the powerful top banana of the Interdata computer line.

The original Model 70, introduced in September 1971 and first installed in October of the same year, was quickly followed (in December 1971) by the faster, more powerful Model 80 with all MOS memory. Model 74, the smallest member of the New Series and aimed toward the OEM market, was introduced in July 1972. March 1973 brought announcement of the Model 85 as the most advanced processor in the Interdata 16-bit family. In fact, writable control store is featured as the major difference between Model 85 and the earlier Model 80. First delivery of the Model 85 was in June 1973. Meanwhile, the reconfigured Model 74, using a 16K-byte core memory board, was announced in June 1973 and delivered in the third quarter 1973. In September 1973, Interdata introduced the first member of its new 32-bit line, together with the 7/16, a new entry-level system, which also has a new CPU that can maintain compatibility with the other 16-bit models and expand to the 7/32 in the field via a special "stretch 32" option. The 7/32 performs operations on 32-bit operands but uses a 16-bit wide internal bus and I/O bus. The 8/32, on the other hand, uses a 32-bit wide internal bus and a 16-bit wide I/O bus. The 7/16, 7/32, and 8/32 all use the same core memory modules. Two modules operate in tandem for the 8/32 to accommodate 32-bit words.

These computers are general-purpose systems designed for stand-alone processing, control, data acquisition, and data communications applications. All use a 16-bit word. Core storage modules are used for main memory in Models 70, 7/16, and 74; MOS modules are used in Models 80 and 85. All models are built around a read-only memory (ROM) control store that holds the microinstructions used to implement the instruction set. All models use preloaded ROM modules. In addition, Model 85 has a writable control store module that can be microprogrammed by the user; Interdata calls this a "dynamic" control store.

The interrupt handling facilities make all of the Interdata computers unusually good for data communications and control applications. Interdata markets special programmable data communications configurations of Model 70 (called Models 50, 55, 60, 270X, and MS-5) with data communications instruction sets. Model 50 uses a single Model 70 processor with an instruction set oriented toward data communications. Model 55 is a dual-processor configuration consisting of a Model 50 and a Model 70. Model 60 is like the 50, but based on the higher-speed Model 80 processor with MOS memory. Model 270X is a plug-compatible front end for an IBM System/360 or 370; it replaces the IBM 2702 and 2703 control units. The MS-5 is a turnkey store-and-forward message switching system using Model 50.

Software for the line includes packages for small stand-alone systems and for systems using the BOSS (Batch Operating System), RTOS (Real-Time Operating System), OS/16 MT (OS/16 Multi-Task Operating System), or DOS (Disc Operating System). The systems support assemblers, BASIC, and several versions of FORTRAN. A compact telecommunications executive called RTEX is available for Models 50 and 60.

This report deals mainly with the general-purpose models, but remarks on the 50, 55, 60, MS-5, and 270X are included to give an overview of these systems. See Table 1 for system specifications.

Competitive Position

Interdata early recognized the advantage of using firmware — microprogrammed ROM — to implement processor logic, and all of the firm's computers have been built using it. Initially, the instruction execution times for Interdata's computers were slow because each instruction required the execution of several microinstructions. On the other hand, much of the I/O processing and interrupt handling were automatic, and Interdata computers gained a well-deserved reputation for good I/O and interrupt facilities. As ROM modules have become faster, other manufacturers have switched to microprogrammed logic. Now the instruction execution times for Interdata computers are fully competitive with those of other computers.

Model 70 has been the mainstay of Interdata's line, competing with such systems as the Digital PDP-11/40, Data General Nova/Supernova, and Hewlett-Packard 2100S. Model 74, a stripped-down version of the 70, was designed primarily for the OEM market and competed with the PDP-11/05, Nova 1210, and HP 2100A. Model

Table 1. Interdata 16-Bit Models: Mainframe Characteristics

Processor Characteristics	Model Numbers 70	74	80	85	7/16
CENTRAL PROCESSOR					
Type	Micropro-grammed	Micropro-grammed	Micropro-grammed	Micropro-grammed	Micropro-grammed
No. of Internal Registers	16	16	16	16	16
Use	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs	Accumulators: 15 index regs
Addressing					
Direct (no. of words)	32,768	32,768	32,768	32,768	32,768
Indirect	No	No	No	No	No
Indexed	Yes	Yes	Yes	Yes	Yes (1 level)
Max I/O devices	255	255	255	255	255
Instructions					
Implementation	Firmware	Firmware	Firmware	Firmware	Firmware
Number	113	110	127	131	104-125
Fixed-Point Arithmetic					
Add/subtract	Hardware	Hardware	Hardware	Hardware	Hardware opt
Multiply/divide	Hardware	Hardware	Hardware	Hardware	Hardware opt
Add time (μsec)	1.0 reg-to-reg)	1.5 (reg-to-reg)	0.53 (reg-to-reg)	0.53 (reg-to-reg)	1.5; 1.0
Floating-Point Arithmetic	Hardware	Subroutine	Hardware	Hardware	Hardware
User Microprogramming	No	No	No	Yes	
Priority Interrupt System					
Lines					
Internal	8, 1**	6	8, 1**	8, 1**	
External	2 gen; 3 dedicated	1 gen; 3 dedicated	1 gen; 3 dedicated	1 gen; 3 dedicated	1 std
Levels	256/gen line	256/gen line	256/gen line	256/gen line	255
Memory					
Type	Core	Core	Semiconductor	Semiconductor	Core
Word length (bits)	16	16	16	16	16
Cycle time/word (μsec)	1.0	1.0	0.270	0.270	0.75; 1.0
Capacity (words)					
Max	32,768	32,768	32,768	32,768	32,768
Min	4K, 8K, 16K	4K, 8K, 16K	8,192	8,192	4,096
Increment	4K, 8K, 16K	4K, 8K, 16K	8K	8K	4K, 8K, 16K
Parity	Opt	Opt	Opt	Opt	Opt
Protect	Opt	NA	Opt	Opt	Opt
ROM use	Implement processor logic	Implement processor logic	Implement processor logic	Implement processor logic	Implement processor logic
Writable Control Store	No	No	No	Yes	No
I/O Channels					
Programmed I/O	Std	Std	Std	Std	Std
Direct memory access	Std	Std	Std	Std	Std
No. of channels	4	1	4	4	4
Selector channel	Opt	Opt	Opt	Opt	Opt
No. of devices handled	16	16	16	16	16
Multiplexed channel	Std	NA	Std	Std	Std
Maximum Transfer Rate (words/sec)					
Within memory	273,972	273,972	815,660	815,660	340,300; 273,972
DMA	1,000,000	1,000,000	2,100,000	2,100,000	2,600,000
High-speed DMA	—	—	3,000,000	3,000,000	—

Notes:
* Integrated parallel double-buffered Teletype adapter included with processor Models 70, 80, 85.
** Optional protect interrupt.

80, over twice as fast as Model 70, competed with the PDP-11/45 and 11/50 and the Supernova SC. Model 85, basically the same as Model 80 but with dynamic control store, competed with other systems that have writable control store, such as the Varian 73, the Microdata 3200, and the HP 2100S. Writable control store is of interest to those who can use it to gain substantial increases in throughput for a particular application.

While Interdata is still marketing these systems, the new "bridge" model, the 7/16, has become the entry level system for 16-bit computers while the company's 32-bit line has taken over the medium range applications, formerly filled by the 80 and 85. What makes the 7/16 attractive to new users is its low cost and its role as a bridge system. It gives present users upward growth possibilities while letting them take advantage of Interdata's present software. The firm supplies a broad range of peripherals for its 16-bit systems plus a reasonable amount of software, four operating systems, FORTRAN IV and BASIC compilers, and data communications line handlers. The RTOS is the major piece of software for process control applications. OS/16 is a compact version used on the 7/16.

Interdata's strongest markets have been in data communications and process control applications. Over 60 percent of its business has been to OEM users, while 40 percent has been to end users.

Up to 255 peripheral devices can interface to the processor via the multiplexor bus. High-speed devices, such as discs, transfer only control information over the multiplexor channel, and use an optional selector channel for transferring data directly to or from memory. The selector channels interface directly to the processor through a DMA port. Although each selector channel can support up to 16 devices, only one device at a time can use the channel. Customer-designed channels can also interface to the DMA ports.

Interdata provides a broad range of peripheral devices for its computers. Conventional devices include Teletype units, alphanumeric video displays, paper tape reader/punch, punched card reader, and line printers. Mass storage devices range from magnetic tape cassette through industry-compatible 9-track magnetic tape drives to drum and disc cartridge units. Interdata also provides many data communications devices as well as A/D and D/A subsystems to connect noncomputer devices.

Compatibility

Model 74 is the bottom of the line, and Model 70 is upward program compatible with the Model 74. Model 80 is upward program compatible with Model 70. The Model 85 processor logic is identical to that of Model 80, except that Model 85 can use the dynamic control store memory.

All Interdata computers have compatible I/O buses and therefore use the same peripheral devices.

CONFIGURATION GUIDE

Interdata computers function in stand-alone configurations or as satellite or front-end processors for other systems. The basic central processors of Model 70, 7/16, 80, and 85 include 16 general-purpose registers, high-speed multiply/divide, 32-bit floating-point hardware, a buffer multiplexor channel with up to 255 subchannels, four Direct Memory Access (DMA) ports, a Teletype interface, a vectored hardware priority interrupt system for up to 255 devices, a display panel, a power supply, and 3 or 11 additional slots for memory expansion or I/O options.

Model 74 shares many processor characteristics with Models 70, 80, and 85 but also has the following differences: floating-point arithmetic is handled by subroutines; one DMA port is standard; the Teletype adapter and display panel are not included in the basic system; and five slots are provided for memory expansion or I/O options.

Memory ranges differ for the various Interdata New Series models. Minimum memory size is 4,096 16-bit words for Models 70 and 74, and 8,192 words for Models 80 and 85. Maximum memory size is 32,768 words (65,536 bytes) for all models. The Twin Chassis 70 and the reconfigured 74 use a new memory circuit board that stores 8K words of memory in the same space previously used by 4K words. The Twin Chassis 70 also provides 11 subassembly slots and a more powerful bulk power supply in its twin chassis. Model 85 also supports 1K 32-bit words of control memory that can implement a user-defined instruction set.

The basic Model 7/16, the most recent 16-bit system, includes the central processor, 8K bytes of core memory, power supply, and chassis with eight slots.

Standard options include a 16-slot chassis to configure large systems; 8K-, 16K-, and 32K-byte core memory modules with either a cycle time of 0.75 or 1.0 microsecond; memory parity; power fail detection and automatic restart; memory protect; binary or hexadecimal display panel; automatic loader; turnkey console; signed multiply/divide; high-speed arithmetic (multiply/divide, floating-point arithmetic, list processing and privileged instruction detect); and stretch 32 (converts 7/16 to 7/32 processor).

Table 2 lists the peripherals and Table 3 lists the software available for the Interdata computers.

MAINTENANCE AND SUPPORT

Interdata supplies systems on a purchase-only basis. Through separate maintenance contracts, users can negotiate for on-site engineers (1, 2, or 3 shifts), or take damaged boards to a repair depot (or have them replaced). Maintenance service is also available on a per-call basis.

Interdata has offices in more than 20 locations in the United States and Canada as well as in Japan, Australia, Great Britain, and Germany.

Table 2. Interdata 16-Bit Models: Peripherals

Model No.	Description
Punched Tape	
M46-240	300-cps readers
M46-242/250	300-cps reader, 75-cps punch
Punched Card	
M46-230/236	400/1,000-cps readers
Printers	
M46-204	60-200 lpm, 132 col, 64-char set
M46-207/209	200/600 lpm, 132 col, 64-char set
Terminals	
M46-000/001	ASR 33/35 TTY
M46-100-103	A/N display, 4,920 char, to 9,600 baud
M46-108	Graphic display, to 9600 baud, 1,024 x 1,024 point matrix
Magnetic Tape	
M46-400	Dual-drive cassette, 500K bytes/cassette; 1,000-cps xfer
M46-460	9-trk 800-bpi magnetic tape, 45 ips
M46-465-467	9-trk 1,600-bpi magnetic tape, 45 ips, 4 drives/controller
M46-476	7-trk, 556- or 800-bpi (not both) magnetic tape subsystem, 4 drives/controller
Discs	
M46-410	2.5Mb 5440-type removable cartridge disc, 4 drives/controller
M46-516	10.0Mb fixed/removable 5440-type cartridge disc, 4 drives/controller
M46-429	40.0Mb 2316-type disc pack, 4 drives/controller
Process I/O	
M48 series	Wide-range analog input, up to 512 channels
M48 series	High-speed low-level analog input, up to 64 channels
M48 series	High-level analog I/O, up to 8 differential or 16 single-ended inputs
M48 series	Real-time analog controller, two 32-word solid-state buffer memories
M07/M48	Digital Multiplexor Subsystem, 2,048 input & 2,048 output lines
Communications	
M10-022	Auto dial units, 4-lines
M11-200	IBM 360/370 interface multiplexor (burst or block modes) channel
M47-000/001	Bell-type adapters, 201/301, to 9,600/40,800 baud
M47-100	Async line module controller, up to 92 lines, to 1,800 baud
M47-101/102	Programmable single-line module/adapter for Bell 103 & 202

Table 3. Interdata 16-Bit Models: Software

Package	Description
BOSS PLUS	Batch system for 70, 80, or 85 processor with arithmetic traps for 74 and 7/16; requires 8KB memory, operator console, TTY
DOS PLUS	Disc operating system, core resident or disc resident, for 74 and 7/16; requires 16KB memory, operator console, TTY
RTOS	Multiprogramming multitask real-time operating system for 70, 80, 85, or a 7/16 with High-Speed ALU option; requires 24KB memory, operator console, memory protect clock, TTY
OS/16	Compact multiprogramming multitask system, for 70, 74, 80, 85, or 7/16; requires 8KB memory, operator console, power fail/auto restart, clock, TTY
FORTRAN IV	ANSI x3.9-1966 with extensions for BOSS PLUS, DOS PLUS, RTOS, and OS/16 MT; requires 70, 74, 80, 85, or 7/16, 16KB above operating system requirements, operator console, TTY
FORTRAN V	FORTRAN IV (above) but can support ISA calls for any operating system (including 7/32); same requirements as FORTRAN IV
BASIC	Interpreter conforms to Dartmouth conventions, with extensions; single-user version requires any CPU (including 7/32), 10.5KB memory above operating system requirements, console, TTY
MUBS	Multi-User Basic Operating System, self contained for up to 32 users (depending on system memory service); for 70, 74, 80, 85, or 7/16 processor, 16KB memory (4-user level) clock, TTY, console
CAL	Common Assembly Language for both 16- and 32-bit processors; requires 16KB memory above operating system requirements, console, TTY
DCSS	For program debugging microcode on 85's DCS option; requires Model 85, CPU, 16KB memory, TTY

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint $
	MODEL 7/16 GENERAL-PURPOSE PROCESSOR (includes 16 GP regs, buffered mplx bus, 4 high-speed DMA channels, and 255 hardware vectored interrupt levels; auto-load bootstrap instruction for initial loading)		
M71-011	8,192 Bytes of Core Memory. (1 μsec, 8-slot chassis and power supply)	3,200	45
M71-012	16,384 Bytes of Core Memory. (1 μsec, 8-slot chassis and power supply)	3,700	50
M71-013	32,768 Bytes of Core Memory. (1 μsec, 8-slot chassis and power supply)	5,300	60
M71-014	32,768 Bytes of Core Memory. (750 nsec, 8-slot chassis and power supply)	5,800	65
M71-021	M71-011 with 16-slot chassis	4,200	45
M71-022	M71-012 with 16-slot chassis	4,700	55
M71-023	M71-013 with 16-slot chassis	6,300	65
M71-024	M71-014 with 16-slot chassis	6,800	70
	MODEL 7/16 PROCESSOR OPTIONS		
M7 -100	Turnkey Console	100	
M71-103	Automatic Loader	400	2
M71-104	Power Fail Detection/Auto Restart	400	2
M71-105	Signed Multiply/Divide Hardware	950	5
M71-106	High-Speed ALU	4,900	20
M71-107	Automatic Memory Protect	1,450	5
M71-108	Processor Parity Control	500	
M71-109	Stretch/32 Module	5,000	
M70-103	Selector Channel	1,000	10
M71-101	Binary Display Panel	300	2
M71-102	Hexadecimal Display Panel	600	5
M70-104	Loader Storage Unit controller	500	10
M70-105	128-Byte Storage Module	100	
M48-005	Multiplexor Bus Buffer	900	5
	MODEL 7/16 MEMORIES		
M71-300	8,192-Byte Memory Expansion Module (1 μsec core cycle time)	2,000	20
M71-302	16,384-Byte Memory Expansion Module (1 μsec core cycle time)	2,650	30
M71-304	32,768-Byte Memory Expansion Module (1 μsec core cycle time)	3,950	40
M71-306	32,768-Byte Memory Expansion Module (750 nsec core cycle time)	4,500	45
M71-301	M71-300 with parity .	2,500	20
M71-303	M71-302 with parity.	3,150	30
M71-305	M71-304 with parity.	4,450	40
M71-307	M71-306 with parity.	5,000	45
	MODEL 70 GENERAL-PURPOSE PROCESSOR (includes 16 GP reg; high-speed mult/div; 32-bit floating-point hardware; buffered multiplexor bus with up to 255 auto I/O channels; read/write block, interleaved data channel to memory; 4 cycle-stealing DMA ports; character-buffered teletypewriter interface; hardware interrupt discrimination and vectoring for up to 255 devices; display panel and power supply)		
M70-000	Model 70 Processor (8,192-byte 1,000-nsec core memory and 8-slot chassis)	6,800	60
M70-002	Model 70 Processor (16,384-byte 1,000-nsec core memory and 16-slot chassis)	9,200	80
M70-004	Model 70 Processor (32,768-byte 1,000-nsec core memory and 16-slot chassis)	10,900	90
M70-001	Same as M70-000 with parity	7,800	60
M70-003	Same as M70-002 with parity	10,200	80
M70-005	Same as M70-004 with parity	11,900	90
	MODEL 70 PROCESSOR OPTIONS		
M70-100	Power Fail Protection/Auto Restart	200	2
M70-101	Automatic Memory Protect	2,900	5
M70-103	Selector Channel (provides true cycle-stealing to memory for 8- or 16-bit transfers at rates up to 2M bytes/sec)	1,000	10
M70-104	Loader Storage Unit Controller	500	10
M70-105	128-Byte Storage Module	100	**
M48-005	Multiplexor Bus Buffer	900	5
	MODEL 70 MEMORIES		
M70-300	8,192-Byte Memory Expansion Module (1,000-nsec core cycle time)	2,700	20
M70-302	16,384-Byte Memory Expansion Module (1,000-nsec core cycle time)	4,300	30
M70-304	32,768-Byte Memory Expansion Module (1.0- sec core cycle time)	5,000	40
M70-301	M70-300 with parity	3,200	20
M70-303	M70-302 with parity	4,800	30
M70-305	M70-304 with parity	5,500	40
	MODEL 80 GENERAL-PURPOSE PROCESSOR (Model 70 processor with 3 additional slots for expansion memory storage units or I/O options; includes M49-022 power supply for processor and I/O; memory fully powered for up to 64K bytes)		
M80-000	Model 80 Processor (16,384-byte MOS memory; average access time 270 nsec, and 8-slot chassis)	14,900	150
M80-001	Same as M80-000 with parity)	16,400	150
	MODEL 85 GENERAL-PURPOSE PROCESSOR (same as Model 80 but with 4,192-byte dynamic control store)		
M85-000	Model 85 Processor (16,384-byte MOS memory, average access time 270 nsec; 4,192-byte Bipolar Dynamic Control Store, 1,024 x 32 bits, and 8-slot chassis)	22,800	175
M85-001	Same as M85-000 with parity	24,300	175
	MODEL 80 AND 85 PROCESSOR OPTIONS		
M80-100	Power Fail Protection/Auto Restart	350	2
M80-101	Automatic Memory Protect	2,900	5
M70-103	Selector Channel (provides true cycle stealing to memory for 8- or 16-bit transfers at rates up to 3.15M bytes/sec)	1,000	10
M70-104	Loader Storage Unit Controller	500	10

Model Number	Description	Purchase $	Monthly Maint $
	MODEL 80 AND 85 PROCESSOR OPTIONS (Contd)		
M70-105	128-Byte Storage Module	100	–
M48-005	Multiplexor Bus Buffer	900	5
M80-102	Battery Pack	300	–
	MODEL 80 AND 85 MEMORIES		
M80-300	16,384-Byte Expansion Memory Storage Unit (270-nsec average MOS cycle time)	7,900	40
M80-301	Same as M80-300 with parity	8,900	40
	SYSTEM MODULES		
M48-012	Line Frequency Derived Clock	250	5
M48-000	Universal Clock Module	600	5
M48-001	8-Line Interrupt Module	900	5
M48-002	General-Purpose Interface Board (15 inches)	550	NA
M48-013	Universal Logic Interface	650	NA
M48-014	Input/Output Bus Switch	1,500	10
M48-107	Extension Cable Kit, 25 feet	175	–
M48-018/9	Manual Control Panel for I/O Bus Switch	200	
	DISC		
M46-410	2.5M-Byte Removable Cartridge Disc System	10,000	80
M46-414	2.5M-Byte Removable Cartridge Disc System	10,100	80
M46-411	2.5M-Byte Removable Cartridge Disc Expansion Drive	5,500	50
M46-420	Removable Cartridge Disc Interface (for use with up to four 2.5M-byte Drives)	4,000	30
M49-023	Expansion Power Supply for Single Drive Disc	500	–
M49-027	Expansion Power Supply for Single Drive Disc	600	
27-039	2.5M-Byte Removable Cartridge Disc Pack	200	–
M46-416	10M-Byte Removable Cartridge Disc System	12,000	120
M46-417	10M-Byte Removable Cartridge Disc System	12,100	120
M46-418	10M-Byte Removable Cartridge Disc Expansion Drive and Power Supply	8,000	90
M46-419	M46-418 with 50 Hz Power Supply	8,100	90
M46-421	Removable Cartridge Disc Interface (for use with up to four 10M-byte dual disc drives)	4,000	30
27-056	10M-Byte Removable Cartridge Disc Pack	270	-
M46-429	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	24,950	200
M46-430	40M-Byte Removable Cartridge Disc Drive and 1 x 4 Controller	25,100	200
M46-431	40M-Byte Removable Cartridge Disc Expansion Drive	17,950	200
M46-432	40M-Byte Removable Cartridge Disc Expansion Drive	18,100	200
M46-433	Removable Cartridge Disc Controller	7,000	50
M46-434	40M-Byte Removable Cartridge Disc Pack	500	–
	TELETYPE CONSOLES		
M48-010	ASR Model 33/35 TTY Interface (with internal cable)	350	5
M46-000	ASR Model 33 Teletypewriter (with external cable)	1,450	40
M46-002	50-Hz Version of M46-000	1,550	40
M46-001	ASR Model 35 Teletypewriter (with external cable)	4,200	40
M46-003	50-Hz Version of M46-001	4,300	40
	PAPER TAPE EQUIPMENT		
M46-250	Combination Paper Tape Reader/Punch Interface (with direct connect cable)	900	10
M46-240	Paper Tape Reader, Uni-directional (300 cps)	1,300	20
M46-241	50-Hz Version of M46-240	1,400	20
M46-242	Combination Paper Tape Reader/Punch (300/75 cps, rack mountable for use with fanfold tape)	3,300	40
M46-243	50-Hz Version of M46-242	3,400	40
	PUNCHED CARD		
M46-235	Card Reader Interface (with internal cable for 400 cpm or 1,000 cpm card reader)	900	10
M46-234	Hardware Hollerith to ASCII Conversion Option for Card Reader Interface	350	–
M46-230	Card Reader, (400 cpm includes external cable)	3,000	40
M46-231	50-Hz Version of M46-230	3,100	40
M46-236	Card Reader, (1,000 cpm; includes external cable)	5,000	80
M46-237	50-Hz Version of M46-236	6,000	80
	PRINTERS		
M46-202	Line Printer Interface (and internal cable for 60 to 200 lpm line printer)	500	10
M46-204	Fully Buffered Line Printer, (60 to 200 lpm, 132 columns, 64 char set; includes external cable)	5,000	50
M46-205	50-Hz Version of M46-204	5,200	50
M46-206	Line Printer Interface (and internal cable for 200 or 600 lpm line printer)	750	10
M46-207	Full Buffered Line Printer, (200 lpm, 132 cols, 64 char set; includes external cable)	12,350	90
M46-208	50-Hz Version of M46-207	12,650	90
M46-209	Fully Buffered Line Printer, (600 lpm, 132 cols, 64 char set; includes external cable)	17,150	110
M46-210	50-Hz Version of M46-209	17,450	110
	MAGNETIC TAPE		
M46-400	INTERTAPE (cassette system with dual transports, 1,000 char per/sec read/write speed, hardware read-after-write check, longitudinal redundancy check, 500,000-byte capacity per cassette; includes interface)	4,200	30
M46-470	9-Track, 800 bpi, Magnetic Tape Transport Interface	2,900	20
M46-460	9-Track, 800 bpi, 45 ips Magnetic Tape Expansion Transport, (continuous transfer rate is 36,000 char/sec)	6,000	90
M46-461	50-Hz Version of M46-460	6,100	90
M46-473	7-Track, 556 bpi Magnetic Tape Transport Interface.	2,900	20
M46-474	7-Track, 800 bpi Magnetic Tape Transport Interface.	2,900	20
M46-476	7-Track, 556/800 bpi, 45 ips Magnetic Tape Expansion Transport. (continuous transfer rate is either 25,320 or 36,000 char/sec)	6,000	90
M46-477	50-Hz Version of M46-476	6,100	90
M46-471/2	Magnetic Tape Transport Direct Connect Cable	100	–
M46-475	9-Track, 1600 bpi, Magnetic Tape Transport Interface (controls up to 4 IBM compatible, continuous read-after-write 45 ips drives via a phase-encoded formatter supplied with M46-465 or M46-466)	1,500	10

Model Number	Description	Purchase $	Monthly Maint. $
	MAGNETIC TAPE (Contd)		
M46-465	9-Track, 1600 bpi, 45 ips Magnetic Tape Transport and 1 x 4 Phase Encoded Formatter (continuous transfer rate is 72,000 char/sec)	12,000	120
M46-466	50-Hz Version of M46-465	12,100	120
M46-467	9-Track, 1,600 bpi, 45 ips, Magnetic Tape Expansion Transport (for use with M46-475 and M46-465)	6,800	80
46-468	50-Hz Version of M46-467	6,900	80
	VIDEO DISPLAY		
M46-107	1,200 Baud Local Current Loop Interface (with internal cable)	400	5
M46-100	Alphanumeric Video Display Unit (1,920 char (24 lines x 80 char); std 64-char ASCII subset; 110 or 1,200 baud via current loop interface; up to 9,600 baud with RS-232C)	2,250	30
M46-101	Std 50-Hz Version of M46-100	2,350	30
M46-102	M46-100 with processor and operator cursor control, a full range of editing features, and message and character modes. 110 to 9,600 baud with RS-232C connection	3,350	40
M46-103	50-Hz Version of M46-102	3,450	40
M46-108	Graphic Display Terminal	6,500	60
M46-109	50-Hz Version of M46-108	6,500	60
M46-104/5/6	External Cable Assembly	50	
	DATA COMMUNICATIONS SYSTEMS MODULES		
M47-000	Bell 201 Type Data Set Adapter or Equivalent	1,200	10
M47-001	Bell 301 Type Data Set Adapter or Equivalent	1,400	10
M47-102	Programmable Async Single Line Adapter (for 103/202 data set or local RS-232 terminal)	400	5
M47-100	Async Line Module Controller	500	10
M47-101	Programmable Async Line Module	1,200	10
M49-021	Programmable Async Line System Chassis	550	–
M10-022	Automatic Dial Unit Controller	1,600	10
M10-054	Data Set Cable (for RS232 compatible data sets)	60	–
M10-056	Data Set Cable (for Bell 301 type data sets)	350	–
M47-200	IBM 360/370 Parallel Interface (single address interface)	3,500	50
M47-201	IBM 360/370 Parallel Interface	5,000	60
	CABINETS, CHASSIS, AND POWER SUPPLIES		
M49-020	System Chassis	700	–
M49-024	Power Supply	800	5
M49-026	Bulk Power Supply	1,000	5
M49-003	Adapter Card (10 inches to 15 inches)	150	–
M49-004	System Cabinet	650	–

– Not Applicable
* Quantity discounts are available on most items.
** Additional Software Documentation Packages available.

HEADQUARTERS

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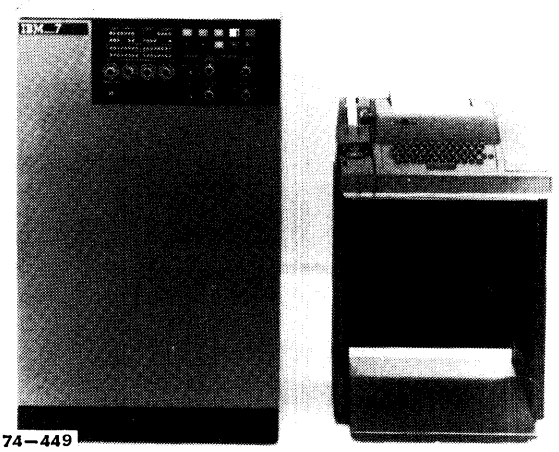
IBM

System/7



OVERVIEW

IBM's System/7 is a small processor designed to excel in real-time data acquisition, laboratory automation, process control, and data communication applications. It is aimed primarily at small, stand-alone, sensor-based applications and as a front end to a host computer.

IBM offers three series of System/7 processor models: A, B, and E. The A and B Series are identical in almost all respects. Their memory capacity is the same, but they differ in their ability to function as front-end processors with other IBM computers. Model Bxx (xx is memory size) interfaces directly with the IBM 1130 computer; Model Axx communicates with the IBM 1800, System/360, or System/370 computers via an asynchronous or bisynchronous communications interface. Model Axx also operates as a stand-alone system. Model Exx is most like Model Axx, but its memory capacity is much larger. Model Exx supports both synchronous and asynchronous data communications. It also has seven additional instructions in its instruction set and has memory protection facilities. Memory protection, however, is not supported by system software.

Main storage is monolithic; capacity ranges from 2K to 16K 18-bit words (one parity bit for each 8-bit byte) for Axx and Bxx models and from 16K to 64K words for Exx models. Memory cycle time is 400 nanoseconds per word. Standard peripheral equipment support for the System/7 includes an operator station incorporating keyboard, printer, and paper tape input/output capabilities; communication interfaces, a wide variety of analog/digital and digital/analog equipment, sensing devices, and 1.2 or 2.4 million words of disc storage.

A number of custom products and features are also available for specific applications, such as for enquiry/response or data communication systems.

The System/7 central processor features two interval timers, four processing levels with 16 sublevels each, an adapter for the 5028 Operator Station, seven index registers, one program counter, and one accumulator. Each processing level has power failure detection with automatic initial program load (IPL), and an internal air isolation environment. Switching time from one level to another is 800 nanoseconds.

The air isolation feature protects System/7 from atmospheric contaminants that may be present in industrial or laboratory environments. Internal air is recirculated through activated charcoal filters to absorb contaminants, and internal heat is dissipated via an air-to-air heat exchange that is part of the feature.

System/7 is designed to operate in rather severe environments: temperature ranges from 40 to 120 degrees Fahrenheit and relative humidity ranges from 8 percent to 85 percent are tolerable during operation. Thermal warning sensors sound an alarm when the temperature exceeds normal operating limits; and thermal shutdown occurs if component damage is imminent.

See Table 1 for mainframe characteristics.

Software for the System/7 allows it to function as a memory-based or disc-based stand-alone process control or DDC system, a front end for the 360/370, 1130, or 1800, a message switching system, or a member of a distributed processing network. Multiprocessing or multiprogramming are not supported.

This rather impressive set of features and selected peripherals allow System/7 to compete in several major application areas: data acquisition, process control, plant automation, and data communication.

IBM announced System/7 Models A and B Series on October 28, 1970. First deliveries were made in the last quarter of 1971. The E Series models were announced in July 1973, and first delivered in December 1973.

COMPETITIVE POSITION

IBM is naturally in a strong competitive position with respect to other vendors of front-end processors for its 1130, 1800, System/360, and System/370. Many corporations prefer one major supplier because equipment-related problems become the supplier's responsibility. IBM caters to this preference by offering user training and technical expertise in application areas.

Many corporations in the industrial community also understand the advantages of multiple suppliers and the need to practice continuing economy in data processing operations. Under these constraints, System/7 must prove its worth. Most minicomputers can communicate with large IBM systems via binary synchronous communication facilities.

Until the introduction of the E Series models, the System/7 had extremely limited expansion capability in

Table 1. IBM System/7: Mainframe Characteristics

Characteristic	5010 Model A	5010 Model B	5010 Model E
Announced	October 1970	October 1970	July 1973
Memory			
Type	Monolithic SS	Monolithic SS	Monolithic SS
Word length (bits)	16	16	16
Cycle Time/wd (nsec)	400	400	400
Capacity (wds)			
Min	2,048	2,048	16,384
Max	16,384	16,384	65,536
Increment Size	2,048	2,048	4,096
Parity	1 bit/byte	1 bit/byte	1 bit/byte
Protect	None	None	Yes(1)
Central Processor			
No. of Internal Registers	4 sets of 9		
No. of Instructions			
Std	40	40	47
Opt	—	—	—
Addressing			
Direct (no. of wds)	Short: 255 Long: 16,384	Short: 255 Long: 16,384	Short: 255 Long: 16,384
Indirect	None	None	None
Indexed	Yes	Yes	Yes
Priority Interrupt System			
Lines	4	4	4
Levels	16/line	16/line	16/line
I/O Channels			
Programmed I/O	Yes	Yes	Yes
Direct Memory Access (DMA)			
No. of Channels	1	1(2)	1
Multiplexed I/O			
No. of Subchannels	—	—	—
Max Transfer Rate			
Within Memory (wds/sec)	625,000	625,000	625,000
Over DMA	—	—	—

Notes:
(1) Memory protect meant for advanced programming use only, not supported by system software.
(2) The 1130 attachment provides direct memory access but does not provide block transfer of data.

comparison to other minicomputers, not only in peripherals but in main memory capacity, which was only 16 K words. The E Series quadrupled maximum memory capacity from 16K to 64K words and offered memory protection. IBM still offers no standard peripherals other than a disc unit, the operator station, and sensor-based devices for the System/7. Other peripherals such as magnetic stripe card reader, interactive console, serial printer, paper tape unit, and card data recorder, are available as custom products.

The System/7 is a well-designed system and features an advanced logical and technological architecture. It uses all semiconductor solid state memory with a 400-nanosecond cycle time. The processor always operates in one of four priority interrupt levels, and it can switch from one interrupt level to another in 800 nanoseconds. Each level has its own set of internal registers and processing at the new level can begin immediately, once the context is switched. Its architecture lends itself to real-time, sensor-based, and data communication applications.

IBM has chosen to market System/7 as a sensor-based front end for its 1130, 1800, System/360, and System/370 systems. Initially, the software for a stand-alone System/7 was rudimentary, and program preparation facilities resided in Modular System Program support (MSP/7) incorporated in the software of a host computer: 1130, 1800, System/360, and System/370. This is still offered, but IBM now also offers the MSP/7 program preparation facilities for the System/7. MSP/7 support includes a macro assembler, FORTRAN IV compiler, linking editor, formatter, and disc support.

System/7 started out as a powerful, small system surrounded by configuration and software constraints that made it almost inextricable from larger IBM systems. Stand-alone systems were practical only for dedicated applications. IBM is gradually loosening the constraints on the System/7 and configurations for general-purpose processing are now beginning to be feasible. System/7 still lacks conventional peripherals, but it is extremely fast and can compete with top of the line minicomputers

in sheer processing power. Its 64K-word memory capacity and program preparation facilities make it more competitive with other minicomputers on the market.

USER REACTIONS

All System/7 users we contacted were pleased with the performance of the System/7.

One user selected it because it was reliable and fast and was backed up by IBM. Also, IBM first presented the possibility of sensor-based computing for the application. This company uses the System/7 as a front end to a System/360 Model 30 to monitor film processing. The company is expanding the system to control all laboratory functions, including process control and personnel record keeping. System downtime has been minimal and the maintenance has been complete and comprehensive.

This user finds the software good, the programming languages easy to use, the hardware reliable, and interfacing sensor-based devices simple.

A second user has installed a factory data collection system built around the System/7 and the System/370 Model 135. The System/7 was selected because it was cheaper than its major competitor for this application. After a year, no failure has been attributed to the System/7. This user has had trouble keeping the 2790 collection system used with System/7 running. The total system is large, however, and many of the problems may have been due to initial design and startup bugs not yet eliminated from the system.

A third user has a stand-alone System/7 with 55 card readers to control the various gates and doors of an airport. The system is installed and operating. Downtime was less than 5 percent during startup.

CONFIGURATION GUIDE

System/7 operates either as a stand-alone computing system or a satellite processor linked to a host processor that is on-site or at a remote location. The system is structured independently of a host processor and is configured according to its application. A system consists of a central processor module and from one to 11 I/O modules housed in the appropriate 5026 enclosure. An I/O module is equivalent to a device controller. The 5026 enclosure provides the cabinetry, power supply, and physical interface connections. Memory and the Direct Control Channel (DCC) are part of the central processor module. The DCC includes the host-processor interface, the operator-station interface, and the two interval timers. Peripherals are listed in Table 2.

Basic Configuration. The most basic stand-alone configuration includes an A02 processor with 2,048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2). This configuration also includes an operator's console with paper tape facilities. An operator station is required with each configuration, but multisystem configurations can share a single station. Program preparation via an assembler requires a minimum of 4,096 words of memory.

The basic configuration of a System/7-1130 installation includes a B02 processor with 2,048 words of memory and one I/O module housed in a nonexpandable 5026 enclosure (Model A2).

Model B includes the 1130 attachment, which interfaces with the 1130 storage access channel (SAC).

Table 2. IBM System/7: Peripherals

MODEL NUMBER	DESCRIPTION
DISCS	
5022	
-001/-002	One fixed, 1 removable; 2.44M wds; 269/126-msec access
-003/-004	Fixed disc, 1.22M wds; 269/126-msec access
CONSOLE	
5028	Keyboard printer paper tape I/O
ANALOG/ DIGITAL	
5012	Multifunction analog I/O and digital I/O module, 32 analog input pts
5013	Digital I/O, to 128 input 64 output
5014	Analog input, to 128 pts 200 pt/sec or 20K pt/sec
COMMUNICATIONS	
1610	Async communications
2074	Binary sync adapter
2790 SUB-SYSTEM	
8185	Control for up to 16 subsystems of 16 data entry stations each, up to 128 displays
2795/6/7	Card and badge readers
2798	Guidance display 12/subsystem
1035	Badge reader
1053	Printer
CUSTOM PER-IPHERALS (RPQ)	
5029	Magnetic stripe card reader
5096-NI	Digital input multiplexor
5098-NI	Teleprocessing multiplexor, 16 lines
5098-N3	BSC module, 4 lines
5098-N5	Sensor-based Control connects 64 S/7 to S/370
7414-1	Interactive console
1017/1018	Paper tape attachment
1627	Plotter attachment
129	Card data recorder attachment
7431	Serial printer
–	Tape cassette records
–	Async comm for 1,200 or 50K bps
–	System 360/370 channel attachment

Expanded Configuration. The 5026 enclosure contains power and internal interface connections for the processor, memory, and input/output modules. There are five enclosures that can be used in various combinations for configuring a system. A system, however, can include a maximum of 11 I/O modules.

5026 Model	Accommodates
A2	1 CPU and 1 I/O module
C3	1 CPU and 2 I/O modules
C6	1 CPU and 5 I/O modules
D3	3 I/O modules
D6	6 I/O modules

Model A2 is not expandable; Models C and D contain multiplexors that allow I/O expansion, and they also accept the air isolation feature. Model D can be 200 feet from Model C so that contaminants, humidity, or temperature that affect it do not affect the central processor.

A/D Equipment Configuration. The input/output module is the basic building block for sensor-based I/O on System/7. Each module is self-contained and houses all the hardware to provide I/O functions. All I/O modules are interchangeable and can occupy any position except the processor position in the 5026 enclosure.

Three I/O modules are available for special equipment: the 5014 Analog Input Module, Models B, C, D, and E; the 5013 Digital Input/Output Module; and the 5012 Multifunction Module. The 5014 can handle up to 384 input points. The 5012 handles analog/digital subsystems (up to 128 digital inputs, 64 digital outputs, 32 analog inputs, and two analog outputs) and the 2790 Communications Subsystem, remote data-entry equipment peculiar to plant automation. The 5013 modules provide for attachment of 128 digital input points, 64 digital output points, the 2790 control, and special devices. The Figure 1 schematic presents major components of the A/D and the Remote Data Entry interfaces.

Other Expanded Configurations. The 5022 Disc I/O Module occupies one position in the 5026 enclosure. Only one disc module can be mounted in an enclosure. Modules not mounted in an enclosure require a 4650 Integral Power Supply. IBM software supports only one disc per system. One disc provides 2.44 million words (Models 1 and 2) or 1.22 million words (Models 3 and 4).

The optional asynchronous or bisynchronous communications feature on processor models A and E occupies the same space in the processor as the 1130 Channel Attachment on B models. These features are therefore mutually exclusive. The asynchronous communication feature with a line adapter can transmit data at a rate of 134.5 or 600 bits per second. Bisynchronous communication operates in half-duplex mode at a wide range of speeds: 1,200, 2,000, 2,400, and 7,200 bits per second and above. The channel attachment transmission rate is based on the cycle-stealing capability of the 1130 processor. Figure 2 illustrates a multisystem configuration with a shared operator console, asynchronous communications, and a remote data entry communications subsystem.

Software Configuration Requirements. The configurations demanded by the basic system software packages are listed in Table 3.

COMPATIBILITY

System/7 is not program compatible with any other system produced by IBM; it is marketed, however, as a front end for a host computer — IBM 1130, IBM 1800, System/360, or System/370. Data compatibility with these processors is maintained via the 16-bit word, which contains two 8-bit bytes. The host computers not only prepare programs for System/7, but they can also transmit object programs to System/7 for execution. The host computer can also perform initial program load. System/7 can also communicate with System/3 via BSCA facilities.

Table 3. IBM System/7: Software

PACKAGE	DESCRIPTION
MSP/7	Modular System Program for system control; with Disc Support System (DDS/7), requires disc, console, and 4K wds memory if program preparation on host or 8K-12K wds if stand-alone version
ASM/7	Macro Assembler, requires 4K wd memory, console
PREP/7 (HOST ASM/7)	Cross Assembler Link Editor and Loader for program preparation on 360/370; 360/370 DOS/VS requires 14K bytes of exclusive storage, 3 disc or tape units; OS-VS requires 44K bytes of exclusive storage
HOST PROGRAM (PREP II)	For program preparation on 1130 or 1800; requires same configuration as 1130 or 1800 macro assemblers and linkage editors
FORTRAN IV	Stand-alone or host versions; stand-alone version requires 12K memory, disc, console
UTILITIES	LINK/7 Linkage Editor, Format/7 formatting Loader, enhanced macro library/relocatable
AML/7	Application Module Library, a set of applications-oriented macros
CCAP/7	Stand-alone Message-Switching Control Program
PCP/7	Process Control Program for monitoring, DDC control
APG/7	Application Program Generator runs on host 360/370 to generate programs using AML/7 macros

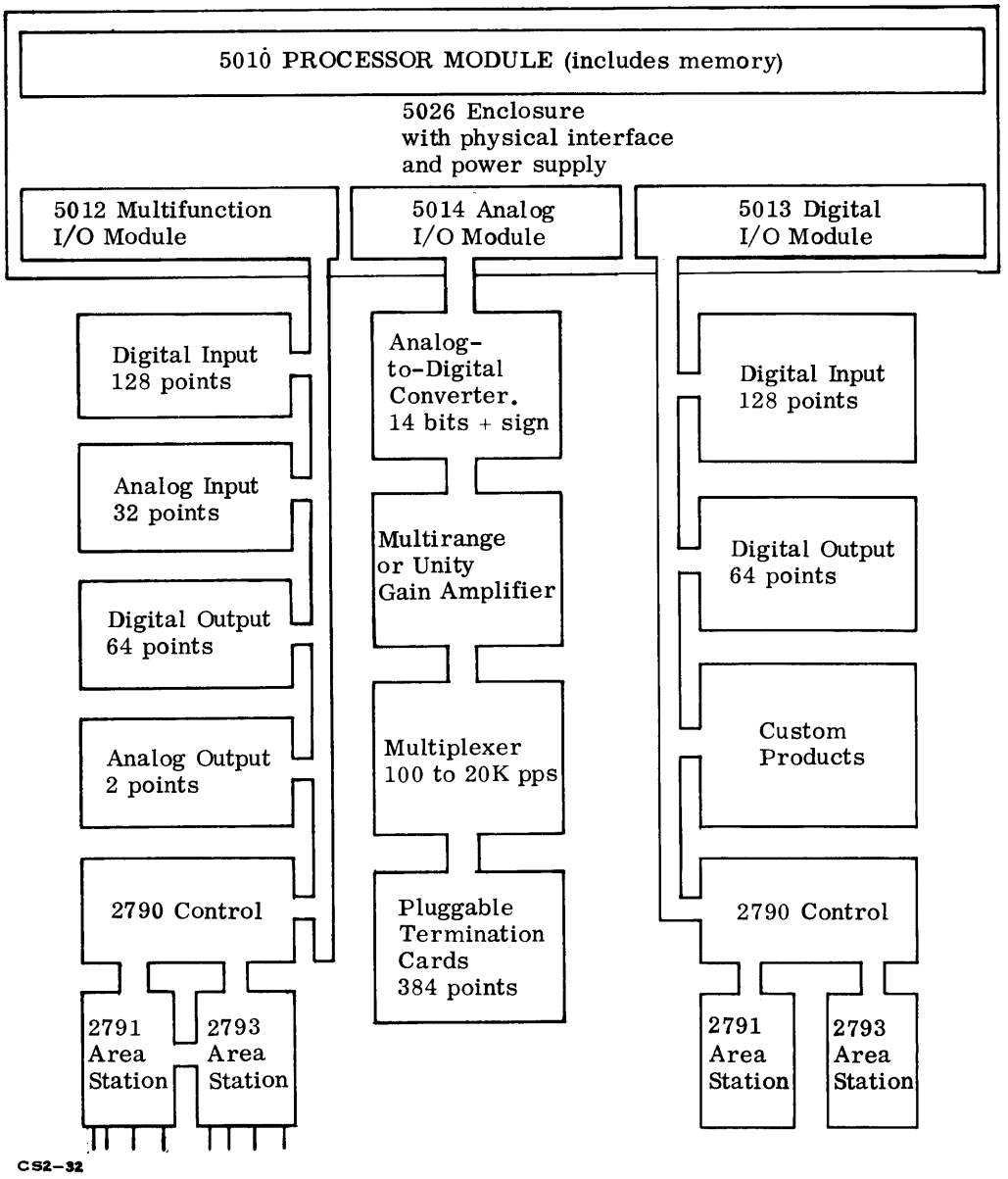


Figure 1. Special Equipment Interfaces to IBM System/7

Axx and Bxx models of the System/7 are identical except for external interfaces. Except for the Disk Support System/7 (DSS/7), the user is obligated to provide or coordinate the basic control software for System/7. Any physical change that affects either addressing or other I/O service becomes his responsibility. It is expected that without standards for processor organization, there will be little if any program compatibility between systems. Reassembly of programs appears mandatory.

The program preparation facilities under DSS/7 for stand-alone System/7 configurations are compatible with host computer preparation facilities. IBM states that it intends to release future enhancements to stand-alone and host FORTRAN program products simultaneously to maintain compatibility.

Programs developed for the Model A will run unmodified on a 16K-word Model E, but programs must be

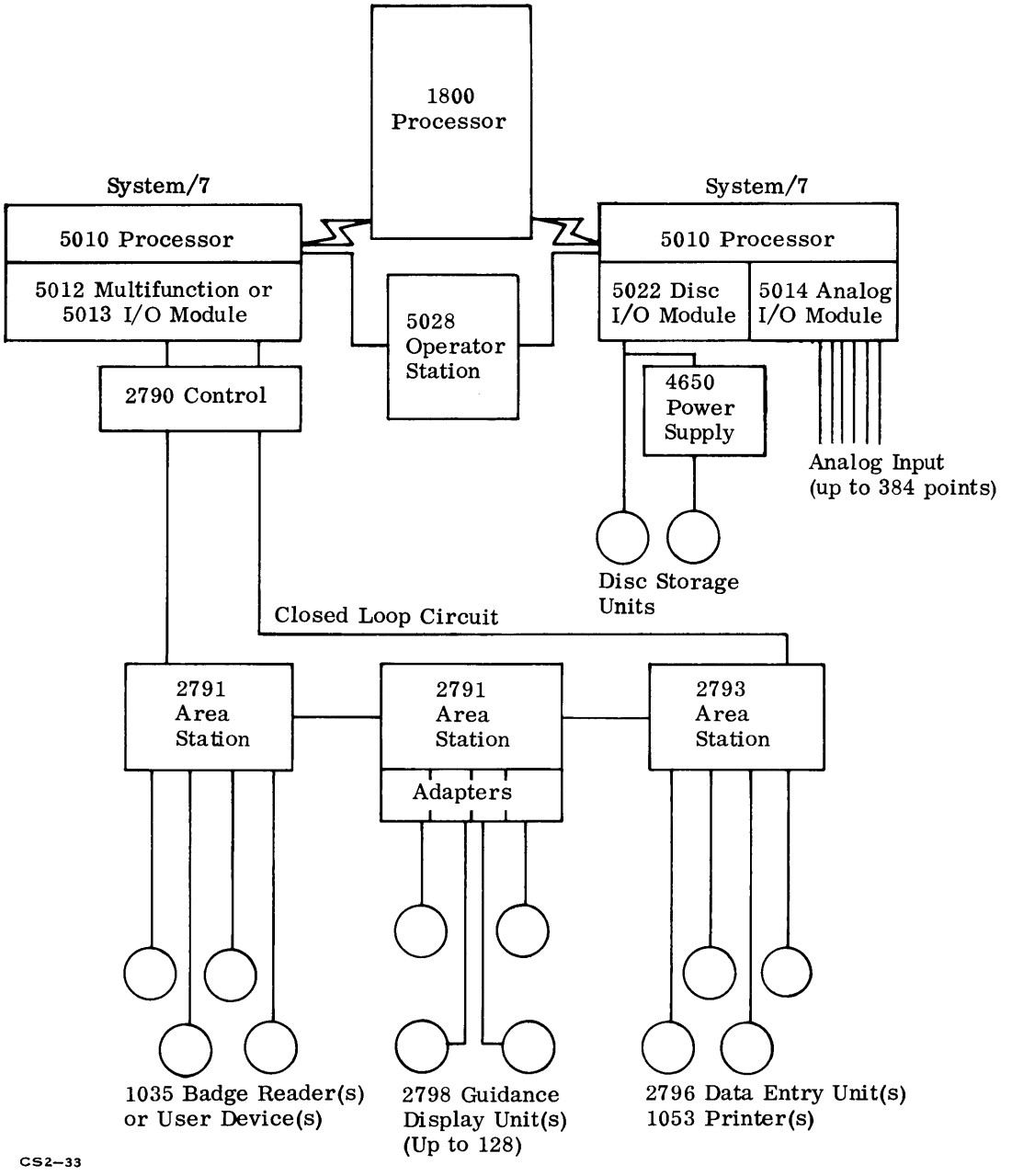


Figure 2. IBM System/7: A Multisystem with Data Communications

reassembled to run on models with more than 16K words.

MAINTENANCE AND SUPPORT

As the largest computer manufacturer in the world, IBM has the most widespread sales and service facilities, reaching into all corners of the globe. Part of IBM's success has been attributed by many industry observers to the efficiency and broad services offered by the sales and service network.

IBM provides a variety of maintenance contracts, depending on what the user needs and can pay for. The standard prime shift preventive maintenance contract provides for prompt emergency service.

PRICE DATA

Model Number	Description	Monthly Rental $	Purchase $	Monthly Maint. $
	IBM SYSTEM/7			
	CENTRAL PROCESSOR AND WORKING STORAGE			
5010-	System/7 Processor with Integral Memory Modules			
A02	2,048 Words	199	8,670	51
A04	4,096 Words	313	12,400	63
A06	6,144 Words	426	16,100	75
A08	8,912 Words	541	19,900	87
A10	10,240 Words (requires 7401 over 8K words)	654	23,600	99
A12	12,288 Words	767	27,400	111
A14	14,336 Words	881	31,100	123
A16	16,384 Words	994	34,900	135
B02	2,048 Words	307	12,700	60
B04	4,096 Words	421	16,400	72
B06	6,144 Words	534	20,200	83
B08	8,192 Words	649	23,900	95
B10	10,240 Words (requires 7401 over 8K words)	762	27,700	107
B12	12,288 Words	876	31,400	120
B14	14,336 Words	989	35,200	132
B16	16,384 Words	1,100	38,900	144
E16	16,384 Words	1,010	35,400	247
E20	20,480 Words	1,155	40,300	281
E24	24,576 Words	1,295	45,100	313
E28	28,672 Words	1,440	49,900	347
E32	32,768 Words	1,590	54,700	379
E36	36,864 Words	1,740	59,500	413
E40	40,960 Words	1,875	64,400	446
E44	45,056 Words	2,025	69,200	478
E48	49,152 Words	2,175	74,000	512
E52	53,248 Words	2,320	78,800	544
E56	57,344 Words	2,470	83,600	578
E60	61,440 Words	2,610	88,500	611
E64	65,536 Words	2,755	93,300	644
7401	Storage Power Addition (for A2)	16	652	1
2662	Cycle Steal Basic	48	1,830	3
5026-	Processor Enclosure for Processor and Up to 11 I/O Module Positions			
A02	1 I/O Position	108	4,710	26
C03	2 I/O Positions	248	10,200	31
C06	5 I/O Positions	367	14,400	50
D03	Extension of C3/C6 by 3 I/O Positions (requires 3715)	248	10,200	40
D06	Extension of C3/C6 by 6 I/O Positions (requires 3715)	367	14,400	59
3715	Dx Enclosure Attachment	37	1,420	5
4621	Internal Air Isolation (for C3/D3)	48	2,290	12
4622	Internal Air Isolation (for C6/D6)	65	3,060	24
5731	Power Failure Detect and Restart (1/enclosure)	54	2,040	1
7401	Storage Power Addition (for C3/C6)	17	652	1
5028-	Operator Station	150	2,280	51
	MASS STORAGE			
5022-	Disc Storage Module			
001	1 Removable, 1 Fixed Disc; 2.44M Words; Avg Access Time (269 msec)	421	15,100	91
002	Avg Access Time (126 msec; same as 001)	492	16,500	100
003	1 Fixed Disc; 1.22M Words; Avg Access Time (269 msec)	324	13,500	87
004	Avg Access Time (126 msec; same as 003)	394	14,800	95
4650	Integral Power Supply	37	1,420	1
2664	Disk Cycle Steal	16	612	1
	INPUT/OUTPUT			
5012-A01	Multifunction Module	42	1,830	8
	DATA COMMUNICATIONS			
	Asynchronous Communications			
1610	Async Communications Control	81	3,060	14
2165	Common Carrier Adapter		408	

PRICE DATA (Contd)

Model Number	Description	Monthly Rental $	Purchase $	Monthly Maint. $
4750	Line Adapter – Limited Distance Type 2B	27	1,020	15
4751	Line Adapter – Leased Line Type 1A	27	1,020	15
4752	Line Adapter – Leased Line Type 1B	27	1,020	15
	Remote Data Entry			
8195	2790 Control (for up to 16 2791/2793 area stations)	198	8,400	45
2791-001	Area Station Controller (for up to 16 units)			
8030	Attachment (for up to three 1035 badge readers; one 8030/station)	16	765	2
8050	Attachment (for 1053 Printer; one 8050 per station)	21	989	1
8295	Attachment (for up to 8 2795/2796/2797 units)	27	1,230	2
8296	Extension Unit to 8295	16	765	1
2795-001	Data Entry Unit (card-badge reader)	21	958	4
2796-001	Data Entry Unit (card-badge reader)	27	1,160	7
2797-001	Data Entry Unit	52	2,340	10
2791-002	Area Station Controller	146	6,920	45
2793-001	Area Station Controller	130	6,180	19
2798-001	Guidance Display Unit	96	4,400	19
7990	Basic Unit Attachment	54	2,440	12
7991	Additional Unit Attachments	21	979	4
1035-001	Badge Reader	27	1,110	4

HEADQUARTERS

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LOCKHEED ELECTRONICS

SUE

OVERVIEW

The SUE (System User Engineered) Computer systems, like their predecessors the MAC 16 and MAC Jr., are designed, marketed, and supported by the Lockheed Electronics Data Products Division, primarily as an OEM product; SUE systems are offered to the business end user as the System III product line. SUE systems are not compatible with the MAC 16 and MAC Jr., but a translator program is available for SUE to translate MAC machine language programs into SUE machine language programs.

SUE processors are 16-bit, byte- or word-oriented microprogrammed processors. Addressing is to the byte level. The SUE is the basic general-purpose system with a 108-instruction set. SUE-SIS designates a scientific version with 38 added instructions in the control ROM. Single processors can support up to 32K words of core.

The SUE systems are modular and flexible. A system can vary from an Infibus controller with user-designed modules to a multiprocessor configuration with up to four SUE processors. Multiprocessor configurations can handle up to 80K words of core by mixing dedicated and common memory banks. SUE is designed to protect the user from system obsolescence by making it easy to add new technology on a function basis. This is accomplished by designing the system around a central bus system called the Infibus, over which system modules communicate with each other on a signal-response basis. System modules operate asynchronously with respect to each other and are synchronized only for information transfer cycles.

Mainframe characteristics are summarized in Table 1. The central data bus architecture is similar to that of DEC's PDP-11 and Hewlett-Packard's HP 3000. SUE will compete with the low end of the PDP-11 line, specifically the PDP-11/05 and 11/15, which are aimed toward the OEM market, particularly the communications sector.

System software includes a Basic Operating System, a foreground/background Disc Operating System, an IOCS operator communications package, various utilities, and, recently, Fortran IV. Peripherals include discs, terminals, slow-speed devices of various kinds, and communications interfaces. Lockheed plans to introduce a multiprocessing operating system, BSC communications, and 2780 emulation during 1975.

The first SUE was delivered in March 1972. Over 2,000 systems have been delivered to date.

Table 1 lists the SUE's mainframe characteristics.

Table 1. Lockheed Electronics SUE: Mainframe Characteristics

CENTRAL PROCESSOR	
Microprogrammed	Yes
No. of Internal Registers	8 general-purpose
Addressing	
Direct (no. of words)	32K (doubleword instructions); 256 (singleword)
Indirect	Multilevel
Indexed	Yes
Instruction Set	
Number	108 (std), 146 (opt)
Decimal Arithmetic	Subroutine
Priority Interrupt	
System	
Lines	4
Levels	4 (unlimited sharing)
MAIN STORAGE	
Type	Core
Cycle Time (nsec)	800
Basic Addressable Unit	Byte/word
Bytes per Access	1 or 2
Ports to Memory	1
Min Capacity (bytes)	2K
Max Capacity (bytes)	64K
Increment Size (bytes)	8K; 16K
Parity	RPQ
Protect	RPQ
ROM	
Use	Control memory
Capacity (bytes)	256 or 512K, 2K possible
I/O CHANNELS	
Programmed I/O	Yes
DMA Channels (no.)	Yes (unlimited no.)
Multiplexed I/O	Yes
Max Transfer Rate (words/sec)	
Within Memory	2.2M (overlapped core)
Over DMA	5M

Competitive Position

The SUE competes primarily in the OEM market. Its software supports assembly language and Fortran programming, under core-based and disc-based operating systems. LEC provides discounts of up to 37 percent for quantity purchases of SUE systems. Discounts do not apply to peripheral devices because LEC buys the devices and provides only the controller interface. The company has sold SUE to communications, data entry, and COM systems OEMs, among others.

Competitors to the SUE include the DEC PDP-11/05 and 11/15; Computer Automation LSI Alpha 16 and Naked Mini 16; General Automation LSI SPC-16, Data General Nova 2, and Microdata 1600. Because SUE is similar in architecture to the PDP-11 and Digital is a large minicomputer manufacturer, it is not surprising that SUE's most vigorous competitor is the PDP-11.

LEC markets SUE chiefly in the communications and process control OEM markets. The introduction of the new DOS should make the system more competitive in these areas. This operating system is of the foreground/background type with one multitasking program operating in the foreground and one batch program operating in the background. Operating systems for real-time and multiprocessor applications will be developed later.

LEC has one advantage over many minicomputer manufacturers in the OEM market: it is a large core memory

supplier to the computer industry as a whole. Consequently, the cost of core memory for its system is low and total system cost is low.

User Reactions

SUE users we contacted were in accord both about the excellent SUE hardware, particularly for the OEM market, and the need for LEC to step up the pace of its software development. A spokesman for a cancer research group, using the system as the heart of a multiparameter analyzer for cells, went so far as to call the hardware design and overall system reliability, "Excellent enough to make Lockheed number 2 in the minicomputer market if the company would market the system more aggressively and concentrate more on software development." An OEM manufacturer developing the SUE as a communications network processor explained that the SUE is unique in the minicomputer market — the arbitration function that determines which component has control of the Infibus is separate from the CPU. Thus, it is easy to use the system building blocks in a multitude of patterns. This company developed a bus connector to allow both multiprocessor systems and multibus systems, some with memory, peripherals and processors on different busses.

CONFIGURATION GUIDE

A SUE computer system consists of a card frame guide; an Infibus and controller; power supply; SUE or SUE-SIS processors; up to 32K words of memory per processor; a control panel; and a universal serial or parallel controller for each peripheral device in the system.

The processors, like all other pluggable system modules, connect to the Infibus, which is in turn controlled by the Infibus controller; also like other pluggable modules, processors can be mixed in a multiprocessor system. Up to four processors can be connected to one Infibus.

The processor models differ basically in the functions they can perform rather than any effect on system configuration. The "SIS" models add instructions to the standard SUE to create a processor suitable for scientific processing and Fortran programming. The master processor is designated by proximity to the Infibus controller in a multiprocessor system, rather than by model. Model numbers are designated as SUE or SUE-SIS 1004, 1008, 1016, 1024, or 1032 depending on the number of words of memory included with the basic CPU.

A chassis consists of an Infibus and the card frame guide. All system modules are mounted on circuit cards that slide into a card guide slot and plug into the Infibus. Twenty-four slots are available for mounting system modules. An internal power supply requires eight slots; if an external power supply is used, other system modules can use the eight power supply slots.

Memory can consist of 4K- or 8K-word core memory modules. Any number of memory modules can be intermixed on a system, provided the total does not exceed 32K words in a single-processor system. Multiple processors can handle up to 80K words in one system by combining 16K dedicated memory banks with a 16K common area. Each core module requires three card slots. Effective memory capacity is limited to 30K words per processor, because the upper 2K-memory word addresses are reserved to address I/O device registers.

Each parallel or serial I/O controller requires one card slot. A block transfer adapter that requires one slot must be inserted next to each controller that needs block transfer capability.

Peripheral devices include Teletype units, high-speed paper tape reader/punch, card reader, line printers, industry-standard magnetic tape units, displays, discs, and asynchronous data communications controllers. A universal logic board is available for designing interfaces for special-purpose devices. The peripheral devices are listed in Table 2.

The 1825 Bus Extender allows two Infibuses to be connected to increase the system card slot capacity. Two SUE systems connected to a common Infibus via communications modules can communicate to obtain many of the advantages of a system doubled in size, including a wider variety of peripherals. The interrupt priority level of the intersystem communication modules can be assigned to any level desired by the system engineer and can be positioned on the Infibus to any priority within its assigned level. Software packages for the SUE with configuration requirements are listed in Table 3.

Table 2. Lockheed Electronics SUE: Peripherals

Model No.	Description
Disc	
6755	IBM 5444 compatible unit, one fixed and one removable cartridge, 2.5M bytes/disc, 4 drives/controller
Terminals	
6710	Teletype, ASR 33, 10 cps
6762	Printer Terminal, 100 cps
6770	CRT Terminal, 960 char
Printers	
6765	Line Printer, 200 lpm
6768	Line Printer, 600 lpm
Cards	
6733	Card Reader, 600 cpm
6734	Card Reader, 285 cpm
Paper Tape	
6717/18	Paper Tape Readers, 300 cps
6723	Paper Tape Punch, 75 cps
6719	Combination 6718 and 6723
Communications	
4651	Async Modem Controller, single line, 300/1200/1800/4800 baud
4530	Four-channel Async MUX to 9600 baud
4502	Serial I/O Controller, RS232C and 20mA polar control
4501/3/6	Parallel I/O Controller, TTL compatible

Table 3. Lockheed Electronics SUE: Software

Package	Description
DOS	Disc Operating System, foreground/background system, requires CPU, 16K words of core, disc, TTY, Card Reader; available mid 1975
BOS	Basic Operating System, includes loaders, I/O control system, Operator Utility Interface Package (OUIP), Debug, CPU Test, Memory Test, Peripheral Tests; requires 4K words of memory and Teletype; can support FORTRAN IV and assemblers.
FORTRAN IV	ANSI X3.9 - 1966 standard, requires CPU, 8K words of core, TTY.
Assemblers	Basic assembler requires 4K words and Teletypes while the Macro assembler requires 8K words and Teletype.

Compatibility

The SUE is not compatible with any other computer. Lockheed's System III product line is based on the SUE system so programs written in Fortran IV or assembly language are interchangeable, given comparable configurations. Programs developed for LEC's MAC 16 and MAC Jr., can be translated into SUE machine language code; the translator runs on SUE. Cross assemblers are available for the MAC 16 and the IBM System/360 so that SUE assembly language programs can be assembled on the MAC 16 or IBM System/360. A SUE simulator written in Fortran is available so that SUE-assembled object code can be tested or executed on any larger computer system that supports ANSI standard Fortran.

MAINTENANCE

Lockheed provides two types of maintenance contracts — a preventive maintenance contract with an extra emergency service charge per visit and an inclusive contract that provides both preventive and emergency service for a single fee. The Field Engineering Department has offices located throughout the United States. Repairs can also be handled at either the local service center or at Los Angeles headquarters. A 10-day course in the basic maintenance of a SUE system is offered free of charge for each SUE customer.

TYPICAL PRICES

Model Number	Description	Purchase $
	SUE Central Processor Systems include 16 slot chassis, SUE INFIBUS, integral power supply panel and bezel, power distribution unit and cooling fans; CPU includes 8 general purpose registers, basic instruction set of 108 instructions, 4 levels of shared priority interrupts, power monitor/auto restart and real time clock; core memory full cycle time is 800 nsec	
1004	CPU with Primary Instruction Set and 4,096 words of 16-bit Core Memory	4,350
1008	1004 with 6,192 words of 16-bit Core Memory	5,950
1016	1004 with 16,384 words of 16-bits of Core Memory, 24 slot Chassis, External Power Supply	7,945
1024	1016 with 24,576 words of 16-bit Core Memory	9,945
1032	1016 with 32,786 words of 16-bit Core Memory	11,445
1004/8/16/ 24/32 SIS	CPU with Scientific Instruction set	+500
1004/8/16/ 24/32 NCP	No control panel option	-400
	CPU OPTIONS	
1240	Autoload-automatically loads memory from selected input device	565
	MEMORY OPTIONS	
	Can be used in any combination up to 32,768 words of memory	
3310	Random Access Magnetic Core Memory with 4,096 16-bit words	2,000
3312	Same as 3310 except 8,192 words	2,200
	MASS STORAGE	
	DISC	
6755-10	Disc Storage Unit, IBM 5444 compatible	9,630
6755-11	Add-on Disc Storage Unit	6,330
6757	Removable Disc Cartridge	200
	INPUT/OUTPUT	
	Teleprinter	
6710-10	Teletypewriter-ASR model 33, Controller, Cable Paper Tape	2,030
	Includes controller & cable	
6717-10	High Speed Paper Tape Reader w/o spooler	2,155
6718-12	Same as 6717-10 except with spooler	3,255
6719-30	Combination High Speed Paper Tape Reader and Punch	5,015
6723-20	High Speed Paper Tape Punch	3,560
	Printers	
	Include controller, cable	
6762-11	Printer Terminal — 132 column, 64 character set, 100 characters per second rate, without stand	4,275
6762-12	6762-11 with stand	4,585
6765-21	Line Printer — 132 column, 64 character set, 200 LPM	12,145
6768-31	Same as 6765-21 except 600 LPM	15,820
	Card Readers	
	Include controller, cable	
6733-11	Card Reader — 80 column, 600 cards per minute	5,745
6734-10	Same as 6733-11 except 285 cards per minute	3,895
	Interfaces and I/O Controllers	
4501	Parallel I/O Controller	800
4502	Serial I/O Controller	565
4503	Parallel I/O Controller	800
4506	Low true input and high true output	800
4551	Custom Bus Interface	565
4590	Block Transfer Adapter	500
	Data Communications	
	DATA COMMUNICATIONS I/O CONTROLLER OPTIONS	
4651	Async Modem Controller	565
4530	Four Channel Async Line Multiplexor	1,050

HEADQUARTERS

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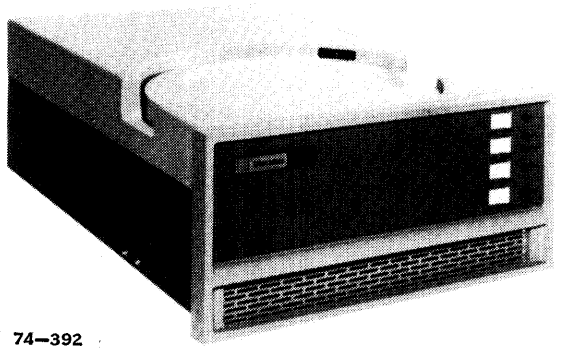
MICRODATA

Micro 800 and 1600 Series



74–392

OVERVIEW

The Microdata Micro 800 and 1600 Series are microprogrammed, stack-processing, byte-oriented systems aimed at general-purpose OEM markets. The two lines differ slightly in speed and packaging; the 800 series has a 1.1-μsec memory cycle time while the 1600 series has a 1-μsec memory cycle. The 1600, moreover, has different firmware to improve performance over and above that obtained from the shorter memory cycle time.

Microdata was microprogramming its systems long before microprogramming was widely implemented. The 800 series was introduced in the spring of 1969 by Micro Systems Incorporated, then a subsidiary of Microdata. Subsequently, as the line developed Micro Systems was totally merged into Microdata Corporation. The 800 line is still in production although it is a "discontinued" product; it has been replaced by the 1600, an optimized version that retains the same architecture, instruction set and peripherals as the 800. Both series, moreover, have submodels that differ mostly by the instruction set implemented in the ROM memory. The Micro 800 series includes the 800, 810, 820, and 821, which implement from 23 to 107 instructions. The 1600 Micro Series includes the 1600, 1600/10, 1600/20, 1600/21, 1600/30, 1600/40, and 1600/60, which implement instruction sets ranging from 23 to 111 instructions. The submodels with the same 2-digit ending, for example, correspond with the 821 and 1600/21, both contain the same instruction set. Model 10 has a few less instructions than Model 20. Model 21 has the same instruction set as the Model 20, but it has been recoded to achieve higher speeds. Model 30 has a few more instructions to handle dual processor configurations. Model 40 has a superset of the Model 20, with extra instructions to handle multiuser "Basic." Model 60 has no instructions available to the user; it is designed as a communications front end in a multiple processor configuration with Model 30, and its control ROM is dedicated to handling communications terminals.

The 821 and 1600/21 are so similar there is no compatibility problem in moving from one system to the other at this level — the same peripherals can attach to either, and all programs in similar operating environments can be run on either system. Similarly, all 800 programs can run on 1600 machines. The only exception might be programs with time-dependent subroutines that run on systems without real-time clocks. The 821-1600/21 instruction set, for example, comprises 107 instructions: 16 control, 12 arithmetic and logical shifts, 17 conditional jumps, 6 I/O, 19 interregister, 8 stack control, 5 character/string manipulation, 2 decimal add/subtract, 2 multiply/divide, and 20 memory reference instructions.

Software for the two series includes an operating system, assembler, Teletype debug facility, text editor, and diagnostics. The operating system is a simple Teletype/paper tape operating system (TOS) that requires high-speed paper tape facilities and a card reader in addition to the CPU, 4K words of memory, and Teletype. The assembler (MAP 810/820) is a 2-pass macro translator that generates absolute code. The BASIC language is also available at extra cost.

PERFORMANCE AND COMPETITIVE POSITION

Until the recent introduction of the 3200 and the Reality™ small business system, Microdata sold its systems almost exclusively OEM. More than 95 percent of the current installations (which now number in excess of 6,000) are OEM. A few universities and colleges also bought Microdata systems as end-user systems. Microdata markets their systems abroad through Intertechnique in France, Tejin Limited in Japan, and Allen Crawford Associates in Canada.

Microdata is vigorously working to expand its installed base, partly because a few customers accounted for a large part of its business and this made the company somewhat vulnerable. In 1973, Microdata reported that 74 percent of its sales went to five customers with one order accounting for 39 percent of total sales.

The 1600 Series has stiff competition from other OEM-oriented manufacturers, some of whom also provide the benefits of microprogramming to OEM customers. General Automation and Computer Automation as well as DEC, Data General, and Hewlett-Packard have big OEM businesses. General Automation and Hewlett-Packard, moreover, provide extensive support for microprogramming for their systems.

Microdata has kept step with its competitors at the low end of the market by introducing the Micro-One bipolar microcomputer, a computer-on-a-board that serves as an entry system to the 800/1600 series. The 3200 Series at the upper end provides another compatible line with higher performance characteristics than the 1600. Thus, the company has an integrated series of product lines with each series upward compatible with the next higher system in the line.

User Reactions

Most Microdata users bought their 800/1600 on an OEM basis and configured them into systems for their own end-users. The users interviewed were acutely aware of the reliability and performance of the Microdata processors; the processor's performance affects the performance of their completed systems and, ultimately, the company's very existence.

All users interviewed expressed pleasure with their Microdata processors. Most users handle their own maintenance; one user has never had a reason to call Microdata. Another user said he dealt more with Microdata engineers than with the field service people. A third user simply returns faulty chips to Microdata, which sends replacements in the mail.

Before selecting the Microdata equipment, users investigated the major minicomputer manufacturers: Digital Equipment, Hewlett-Packard, Varian, Computer Automation, General Automation, Interdata, IBM, and Texas Instruments. One user also looked at Systems Engineering Labs and the Four Phase small business system. Another user considered Intel's microprocessors for the low end of his systems. The reasons for choosing Microdata equipment varied. All users spoke of Microdata's early entry into microprogramming. One user wanted a microprogrammed machine with an instruction set that could be customized and optimized. He required many machines and wanted to be near the vendor. Another user chose Microdata because of the price and the ability to communicate with a CRT and a printer at the hardware and software levels. Another user found the Microdata dual-processor configuration to be the least expensive bid to meet required specifications. One user bought the Microdata 1600 because of its ability to emulate Varisystem's P-16 controller. This emulation afforded continuity for his end-users.

Most users developed their own languages and a few also developed their own operating systems. One user translated his business language into the Microdata assembly language.

Microdata machines are used in many environments. One firm has used the 1600 for two years as a photo unit controller for photocomposition machinery. This user found that service time in the field was reduced by changing from a "repairable" controller to a card controller; replacing the defective card was fast and simple. The user thought highly of the features provided to prevent memory loss. The firm discovered a minor malfunction in the back plane — one chip kept failing. Microdata changed the chip design from thin film to discrete components. The firm is planning to add more core in the near future.

Another user has a 1600 twin-processor configuration which operates as a communication controller for an IBM 360/75; it receives information from terminals in various areas. Most of the operating system is implemented in firmware. The user feels that Microdata has produced a balance of hardware, firmware, and software resulting in a very economical communication controller. In the dual configuration, the first processor communicates with the host computer through channel communications, and the second processor is dedicated to scanning the communication lines.

A turnkey systems house uses 1600 processors as the core of medical laboratory systems to handle medical billing, accounts payable and receivable. This company also sells its systems to small furniture manufacturers. The user has developed a disc operating system, implemented mainly in firmware. The company had some system integration problems, which were not caused by defects in the processor. This user found the 1600/20 instruction set to be "pretty darn good" operating in one-byte precision.

Another systems house uses a customized 1600 as an index table and controller for data storage and retrieval system which are tied on-line to a host computer. It converts key strokes to a location on film to retrieve data. This user found the 1600 to be reliable and the only computer available in the company's price range and compatible with its application.

A user of 1600/21 and 1600/30 processors configures this equipment into turnkey systems for wholesale pharmaceutical and warehouse applications. The firm has developed its own business language and disc operating system for these purposes. The firm had a good experience with Microdata, although Microdata's response to a minor fault in the disc controller was poor. This user assumes the responsibility of maintaining the finished system.

A company that produces small business systems uses the Microdata 1600 for its central processor. Microdata installs the user's custom firmware and tests it through a comparator for bits. This company also tests the equipment with its own diagnostics. This user has experienced fewer problems than expected and is pleased that Microdata delivers equipment on the date specified. This user believes the Microdata equipment has a proven track record and that is important.

CONFIGURATION GUIDE

The 800 and 1600 differ mostly in speed, ROM control memory, packaging (different systems panel) and a few options, but configuration details for both series are nearly identical. Basic configurations consist of a CPU, power supply, bank of 16 registers (6 working registers) control ROM implementing the instructions, priority interrupt system with 8 external interrupts, bootstrap loader, 3 I/O modes (DMA, buffered I/O, programmed I/O) and 8K words of memory. Processor options include a real-time clock, 8-level increments for the interrupt system up to 64 levels, expanded DMA capability, and memory expansion to 32K words. Power-fail detect/auto restart is optional on the 800 and standard on the 1600. The control ROM can be expanded up to 1,024 words in 256-word modules. See Table 1.

Table 1. Micro 800 and 1600: Specifications

CENTRAL PROCESSOR	
No. of General-Purpose Registers	6
Addressing: Indexed	To 32K words
Indirect	± 128 words
Instruction Set (no.)	23-107
Priority Interrupt Levels	8-64
MAIN STORAGE	
Type	Core
Word Length	16 bits
Cycle Time (μsec)	1.1 (800); 1.0 (1600)
Increment Size (words)	4K, 8K
Capacity (min-max) (words)	8K, 32K
Parity	No
Protect	No
ROM	
Use	Microprogram, user macros
Capacity	1,024 words
I/O CHANNELS	
Programmed I/O	Yes
DMA	Yes
Multiplexed I/O	No
OPTIONS	
Real-Time Clock	Yes
Floating-Point Processor	No

Model 1600/30 can be coupled with a 1600/60 in a multiprocessor configuration, but smaller models do not have this capability. Model 1600/40 has extra instructions to handle multiuser "Basic" configurations.

Central Processor

Instructions for all 800 and 1600 machines are microprogrammed. ROM control memory, usually implemented in semiconductor memory, contains the microcommands that define instruction sets. Its operation proceeds at the basic 220-nanosecond clock rate of both series. For all instructions except a JUMP, the next ROM word to be used is preloaded into the processor's control register; this lookahead feature reduces instruction execution times.

The CPU uses separate registers to address control memory and to buffer its output. In addition to implementing the instruction set, control memory can store firmware program constants.

Memory referencing instructions have eight possible addressing modes; namely, direct, direct relative, indirect, indirect relative, indexed, biased indexed, extended, and literal. The basic memory reference instruction is one byte containing two fields: a 5-bit operation code and a 3-bit M field that specifies the address mode. Additional bytes (up to five) contain the operand address, indirect address, base address, or a literal depending upon the addressing mode. Direct addressing can access the first 256 memory locations. Relative addressing can access the 127 locations above or 128 locations below the next instruction in memory.

Indirect address words are located in the first 256 core memory locations. Indexing adds the indirect address word and the index register to produce the effective address. Extended addressing and indexing require a multiple-byte instruction that can address all 32,768 words of storage.

Internal interrupts on the MICRO 800 and 1600 are higher in priority than external interrupts. They have the following priorities from lowest to highest: console-triggered interrupt, direct memory access channel termination, real-time clock, memory protect, memory parity, memory boundary error, power fail, and power on.

Individual interrupts from peripheral subsystems are handled by an external interrupt module, which provides for arming/disarming individual interrupts and enabling/disabling recognition of interrupts in a group. Standard external interrupt cards with eight priority interrupt lines are available. A total of 64 external interrupts can be implemented.

Programmable registers include 16-bit accumulator and extension register, 16-bit index register, 15-bit program counter, 2-bit word-length register, and a 1-bit overflow register.

Table 2 summarizes the characteristics of the different processor models.

Input/Output

Micro 800 and 1600 Series have three input/output facilities: serial Teletype interface, direct memory access (DMA), and a byte input/output bus. The serial Teletype interface can communicate with a full-duplex Teletype; a Parallel Teletype Controller option provides for transfer rates up to 300 characters per second, instead of the standard 10 characters per second. The DMA interface allows direct data transfers between memory and device controllers on an interleaved cycle-stealing basis at transfer rates up to 910,000 (821) or 1,000,000 (1600/21) 8-bit bytes per second.

Table 2. Micro 800 and 1600 Models

Model	Instructions
800	23
810	89
820	95
821	107
1600	23
1600/20	95
1600/21	107
1600/30	111
1600/40	107
1600/60	None*

* None accessible to user; acts as communications front end in multiprocessor configuration with the 1600/30.

The byte input/output facility allows programmed byte-by-byte I/O transfers and buffered block transfers between an external device and memory; maximum transfer rate is 20,000 8-bit bytes per second. All peripherals except Teletype units and discs use the byte I/O bus; discs use the DMA channel and Teletype units use the TTY bus. The byte I/O bus can attach up to 32 devices; the DMA channel can handle 4 standard or 8 optional.

Peripherals

Low-Speed Peripherals. The following peripherals are available.

- Teletype: ASR 33 with paper tape reader and punch, 10 characters per second.
- Paper Tape: Reader/punch reads 300 characters per second and punches 75 characters per second.
- Punched Card Reader: reads 300 cards per minute.
- Line Printers: 80 columns; 150 lines per minute for 80-column lines; 250 lines per minute for 132-column lines.

Mass Storage. Subsystems include both discs and magnetic tape units.

- 2853,4,5,6 Disc Systems (use 8000 Series Drives), 2.5, 5.0, and 10.0 million bytes; one removable or one fixed and one removable platter; single or double density recording; 75-millisecond access time (60-millisecond with fast access feature); transfer rate is 195,000 (312,000 with higher-speed feature) bytes per second over DMA channel.
- Magnetic Tape: up to four transports by way of one controller on byte I/O channel, transports can be selected from the following units: 7-/9-track, 800 bytes per inch, 12.5 inches per second (10,000 bytes per second), 7-/9-track, 800 bytes per inch, 25 inches per second (20,000 bytes per second). All transports on a controller must be the same types.

Communications Devices. A variety of interfaces are provided.

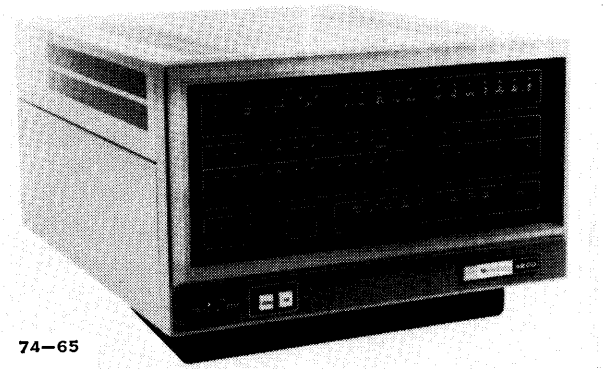
- Full-Duplex Synchronous Modem Interface and Control: (programmed, concurrent I/O and interrupt data transfer modes); rates up to 9,600 baud; EIA Standard RS232C interface.
- Synchronous Modem Interface with Auto Call/Answer Unit: full-duplex in the programmed transfer mode; half-/full-duplex in the concurrent I/O mode; rates up to 9,600 baud; EIA Standard RS232C interface.
- Asynchronous Communications Controller and Interface: programmed, concurrent I/O or interrupt on input character ready transfers at 110 to 9,600 baud rates; EIA Standard RS232C or 20-ma current loop interface to be specified at time of order.
- 4-Channel Communications Interface and Controller: simultaneous operation of 4 full-duplex asynchronous lines; each channel programmable for 75 to 2,400 baud; EIA Standard RS232C or Teletype 20-ma current loop interface.
- Eight-Channel Communications Interface and Controller: simultaneous operations of 8 full-duplex asynchronous lines; 75 to 2,400 baud; EIA Standard RS232C or 20-ma current loop interface.
- Modem/Communications Control: full-duplex 16 discrete inputs; 16 discrete outputs; EIA Standard RS232C interface.
- Automatic Call Unit Controller: controls up to 4 Bell Model 801 Automatic Call Units; EIA Standard RS232C interface.
- Eight-Channel Low-Speed Modem Interface: provides 8 full-duplex RS232B interfaces.
- Sixteen-Channel, Low-Speed Modem Interface: provides 16 full-duplex RS232B interfaces.
- Eight-Channel Teletype Control: provides 8 full-duplex 20-ma Teletype interfaces.
- Sixteen-Channel Teletype Control: provides 16 full-duplex 20-ma Teletype interfaces.

MAINTENANCE

Microdata provides maintenance through 15 plant and service depots and sales offices located in all major cities in the United States.

HEADQUARTERS

Microdata Corporation
17481 Red Hill Avenue
Irvine CA 92705



74–65

OVERVIEW

The Microdata 3200 is a 16-bit microprogrammed minicomputer aimed at both OEM and end-user markets. It consists of the microprogrammable 3200, 32/S, 32/S1, and the 32/S with MPL.

The 3200 is the bare hardware without a microprogram instruction set; no assembly-language level instruction set has been implemented. The 32/S is a complete computer with its architecture designed to make implementation of a compiler language easy. It is designed around a push down stack and a Monobus. The 32/S1 has an extended instruction set: floating-point doubleword arithmetic; string manipulation instructions and swapword in stack instruction set.

Programs are coded in MPL (Microdata Programming Language). MPL is a block-oriented, high-level language similar to PL/1. Currently, programs are cross compiled on an IBM System/360 with PL/1 compiler. A self-compiler implemented in firmware is scheduled for delivery in the first quarter of 1975.

The 3200 hardware modules are organized around a single fast "monobus" connecting all system components. The processor, memory, and peripheral devices operate as monobus subsystems that communicate with each other in a master-slave relationship. This type of bus-centered architecture permits connecting memory modules of different speeds to a system. In addition, the various memory modules and peripheral control cards can be attached in any order to monobus slots. Once initiated, data transfers between high-speed devices and memory can continue while the processor does other work. This architecture is similar to that of the GRI-99 and Digital PDP-11. The 3200 Series addresses peripheral devices as though they were memory locations; thus it has no separate set of I/O instructions.

Main memory can consist of 4K to 128K 16-bit words of MOS memory. The microprocessor utilizes 512 to 4,096 32-bit words of control memory, which can be read-only or a combination of read-only and read/write. Main memory cycle time is 400 nanoseconds for full read cycle; 300 nanoseconds for full write cycle; control memory cycle time is 135 nanoseconds. A high-speed hardware push-down stack, coupled with a look-ahead feature that queues the next software instruction in advance, acts like a cache memory to speed up processor throughput. Addressing is to the byte or word level.

The 32/S is a completely new system; it is not compatible with any system previously offered by Microdata. At present only the MPL cross compiler for the IBM 360, the 32/S self-compiler, and a rudimentary operating system called GENESIS are available.

Peripherals for all models of the 3200 Series are the same as those for Microdata's 800 and 1600 line.

The first 3200 Series system was delivered in January 1974, about 11 have been delivered to date, and over 40 are on order.

COMPETITIVE ANALYSIS

The 3200 joins a growing number of minicomputers featuring microprogramming that can be extended by the user. The versatility of microprogrammed systems, as compared with earlier systems which implement assembly/machine language level instructions with "hard-wired" logic, has led some industry observers to label microprogrammed systems "the fourth generation." Microdata has already had considerable experience with this type of system. Systems in the 800 and 1600 Series are all microprogrammed.

The 3200 Series combines high-speed, MOS semiconductor technology and a push-pop data stack with the inherent advantages of microprogramming. The stack-oriented Model 32/S, with its MPL language, is the first model to implement some of the special advantages of this unique combination of characteristics. The resulting system should be of interest to end users who want to do their own programming, particularly when Microdata develops more supporting software.

Currently, a cross microassembler called "CAP 32" and written in PL-1, Level F and a cross MPL compiler for execution on IBM System/360 running under OS are available. An MPL self compiler is scheduled for the first quarter, 1975.

While the 3200 Model is of greatest interest to the OEM market, Microdata is marketing to end users as well. One of the first 3200s was bought by an end user, who attached it to a PDP-11 for high-speed repetitive calculations. Another is being used to control a high-speed printing operation. Microdata anticipates that most early users of the system will come from the University market.

Microdata has over 5,000 computers currently in operation, and most have been sold to OEMs. Now, Microdata is working to attract more end users to its customer base. In the past, a large majority of Microdata

sales were to five customers, with one order accounting for over a third of total sales. To lessen the market vulnerability inherent in dependence on large accounts, Microdata hopes to extend its customer base so that no customer will account for more than 15 percent of sales.

Microdata also markets Reality, a small business system based on the 1600. For large companies, Microdata markets through its own staff while distributors handle sales to small end-user companies.

At the low end of the market, Microdata has the Micro-One microprocessor. It includes two total systems: a smart CRT terminal and an 8-channel programmable communications controller.

COMPATIBILITY

The 3200 and 32/S are not compatible with any other computer system in the Microdata line.

CONFIGURATION GUIDE

The basic 3200 system encompasses the CPU, main memories, and I/O controllers attached to a common asynchronous bus (the monobus). Units are mounted on printed circuit boards, three of which are used by the CPU control processor. Additional control memory boards are available. Main memory with power fail protect is supplied in 4K- or 8K-word modules to a 128K-word maximum. Four CPUs can operate on the same bus without overloading. MPL supports multiprogramming; moreover, all hardware is provided for communication between CPUs on a "handshaking" basis. Either a maintenance or an operator's console is included with the system. A battery option is available to maintain memory in case of power fluctuation.

The 32/S includes all the basic 3200 components plus the control memory to implement its architecture and instruction set. MPL is also implemented in firmware. Maximum main memory within the CPU chassis is 128K words. System memory protect is an optional feature. An external real-time clock with a variable interval is standard.

Both rack and desktop chassis are available for the 3200. Front panel, power supply, cooling fans, and 16 card slots are included. For these card slots, allocation is as follows: one for the front panel, three for the processor (including control memory), one for the power supply, and one for each 8K-word main memory module or I/O controller. An expansion chassis for main memory modules and/or I/O controllers is optional. The power supply is integral and can maintain data during power irregularities. A battery pack is available for longer protection.

Maintenance for the 3200 Series is relatively simple. Any board can be plugged into any connector in the backplane. If a board needs service, it can be plugged directly into the first available connector. No extender boards are needed. Table 2 lists the peripheral devices that can be used with the system. Table 3 lists the available system software.

Table 1. Mainframe Characteristics — 32/S

CENTRAL PROCESSOR	
Type	Microprogrammed
Control Memory	ROM
Size of Memory	512-4,096 32-bit words
No. of Internal Registers	32
Addressing	
Direct (no. of words)	128K
Indirect	Yes
Indexed	Yes
Instruction Set	
Implementation	Firmware
Number	52 + 32 (32/S1)
Decimal Arithmetic	Yes
Floating-Pt Arithmetic	Opt
User Microprogramming	No
Priority Interrupt Levels	10 int; 8-64 ext
MAIN MEMORY	
Type	MOS
Cycle Time (μsec)	0.3
Basic Addressable Unit	16-bit word
Bytes per Access	2
Min Capacity (bytes)	8K
Max Capacity (bytes)	256K
Increment Size (bytes)	8K
Ports per Module	1 (monobus)
Error Checks	Software (opt)
Protection Method	Opt
Memory Management	Firmware
ROM	Yes (512-4,096 32-bit wds)
Use	Firmware
Capacity	512-4,096 32-bit words
I/O CHANNELS	
Programmed I/O	Std
DMA Channels	Std
Multiplexed I/O (subchannels)	Opt
Max Transfer Rate (wds/sec)	
With Memory	2.5M
Over DMA	3.0M
Simultaneous Operations	Yes

MAINTENANCE AND SUPPORT

Microdata has service and parts centers in major cities throughout the United States. Monthly maintenance contracts are available for all equipment marketed.

HEADQUARTERS

Microdata Corporation
17481 Red Hill Avenue
Irvine CA 92705
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Table 2. Microdata 3200 Series: Peripherals

Device Model	Description
Discs	
3854	Cartridge, master, 1 fixed, 1 removable; 5M-byte capacity; access time: 35 msec; 200K bytes-per-second transfer rate
3861	Slave unit to 3854
3856	Same as 3854 but double capacity
3863	Slave unit to 3856
Magnetic Tape	
3812-3819	7-or 9-trk, 800 bpi; master, NRZI; 12.5/25 ips
3822-3829	Slave units for 3812-3819
3832-3839	9-trk; 1,600 bpi PE
3842-3849	Slave units for 3832-3839
Paper Tape	
3710	Reader/punch; 300-cps read/75-cps punch
3711	Reader only
3712	Punch only
Card Reader	
3720	300-cpm read, 80-col cards
3720-1	Mark sense capability for 3720
Line Printers	
3731	80-col, 64 char, 356 lpm 20-char buffer
3732	132-col, 64 char, 245 lpm, 24-char buffer
3733	132-col, 64 char, 300 lpm
3734	132-col, 96 char, 200 lpm
3736	132-col, 64 char, 60 lpm (165 cps)
Displays	
3750	CRT, 1,920 char; 27 x 80 screen, 110-2,400 baud
Controllers	
1311	General-purpose I/O, 126 14 or 16 IC sockets
1314	Multipurpose I/O, 75-9,600 baud
1330	Async comm; full-/half-duplex, 75-9,600 baud
Terminals Supported	33 ASR, 33 KSR, 35 KSR, TTY, RS232C
Consoles	
Maintenance	18 pairs, register display, manual interrupt, program load
Basic	Load and interrupt buttons

Table 3. Microdata 3200 Series: Software

Package	Description
Microdata Programming Language (MPL)	A PL/I subset for the basic instruction set
Genesis	A simple, disc-based operating system that allows user program storage on disc
Cross Assembler	For IBM System/360 with PL/1, F level compiler

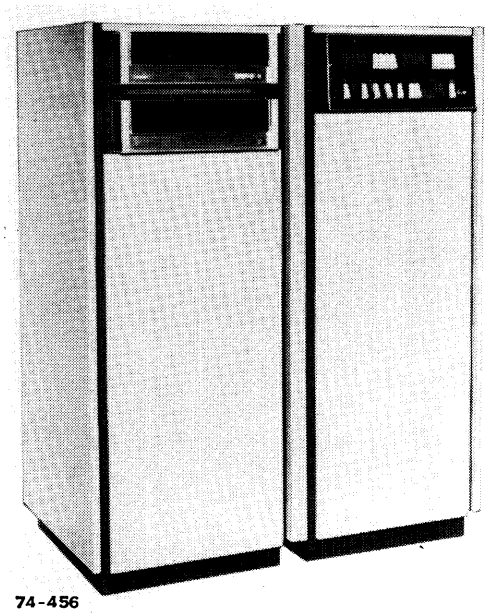
TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	MICRODATA 3200 SERIES CENTRAL PROCESSOR AND WORKING STORAGE		
	Microdata General-Purpose Programming Computer		
3200	3200 Card Cage	5,800	58
3250	32/S Stack-Architecture Microprogrammable Computer (with 2,048-word (32-bit) control memory; card cage with 11 available assembly slots)	7,400	74
	Main Memory Microdata MOS Memory Module		
1300	8K x 16 Bits	5,000	50
1300-1	4K x 16 Bits	3,000	30
1300-5	8K x 18 Bits, Parity	5,800	58
1300-6	4K x 18 Bits, Parity	3,400	34
	Control Memory Assemble (Requires 1 assembly slot)		
3310-xx	Accommodates up to 2,048 words of Programmed Read-Only Memory		
	512 Words	1,900	–
	1,024 Words	3,500	–
	1,536 Words	5,100	–
	2,048 Words	6,700	–
3320-xx	Accommodates up to 2,048 Words of Bi-polar Read-Only Memory		
	512 Words	900	–
	1,024 Words	1,500	–
	1,536 Words	2,100	–
	2,048 Words	2,700	–
1303	Writable Control Memory (WCM) (512 words, 32 bits)	3,000	30
3854	Disc System (including 100 tpi/2,400 rpm; 5M bytes of storage	9,300	100
3861	Add-On Disc Drive	5,025	60
3856	Disc System (200 tpi/1,500 rpm; 10M bytes of storage)	10,000	120
3863	Add-On Disc Drive (includes fixed disc and removable cartridge)	5,725	75
3710 and 3710-1	Paper Tape System (consists of 300-cps reader, 75-cps punch)	4,000	60
3711	Paper Tape Reader System (300-cps reader)	2,500	30
3712	Paper Tape Punch System (75-cps punch)	2,800	30
	Cards (equipment operates at 300-cpm, 80-col cards, 1,000-card hopper/stacker capacity)		
3720	Card Reader	3,750	50
3720-1	Mark Sense Card Reader	5,250	60
	Printers (equipment includes 64-char set, cables, and MPIO controller except 3736 and 3733-1; requires 1 computer assembly slot)		
3731	Line Printer (80 cols; 356 lpm)	9,750	150
3732	Line Printer (132 cols; 245 lpm, 12-channel VFU)	12,500	200
	Line Printer Options (prereq 3732)		
	Self Test Feature	285	–
	Parity Check	285	–
	Static Eliminator	390	–
3733	Line Printer (132 col, 300 lpm)	9,500	150
3734	Line Printer (132 col, 96 char set, 200 lpm)	10,500	150
3733-1	12-Channel Vertical Format (VFU)	400	–
3736-6	Line Printer (165 char/sec 60 lpm, 132 char/line)	6,500	100
	Magnetic Tape System (includes one 7- or 9-track, 800-bpi)		
	Speed / Transfer Rate		
3812	12.5 ips / 10K bps	6,300	75
3813	25.0 ips / 20K bps	6,400	75
3814	12.5 ips / 10K bps	6,500	75
3815	25.0 ips / 20K bps	6,600	75
3816	37.5 ips / 30K bps	6,500	75
3817	45.0 ips / 36K bps	6,600	75
3818	37.5 ips / 30K bps	6,700	75
3819	45.0 ips / 36K bps	6,800	75
	Add-On Magnetic Tape Drive (7- or 9-track, 800-bpi)		
	Speed / Transfer Rate		
3822-x	12.5 ips / 10K bps	3,850	50
3823	25.0 ips / 20K bps	3,850	50
3824	12.5 ips / 10K bps	3,850	50
3825	25.0 ips / 20K bps	3,850	50
3826	37.5 ips / 30K bps	3,850	50
3827	45.0 ips / 36K bps	3,850	50
3828	37.5 ips / 30K bps	4,100	50
3829	45.0 ips / 36K bps	4,100	50
	Magnetic Tape System (includes 1 transport 9-track, 1,600-bpi)		
	Speed / Transfer Rate		
3832	12.5 ips / 20K bps	7,200	100
3833	25.0 ips / 40K bps	7,300	100
3834	12.5 ips / 20K bps	7,770	100
3835	25.0 ips / 40K bps	7,870	100
3836	37.5 ips / 60K bps	7,400	100
3837	45.0 ips / 72K bps	7,500	100
3838	37.5 ips / 60K bps	7,970	100
3839	45.0 ips / 72K bps	8,070	100
	Add-On Magnetic Tape Drive (9-track, 1,600 bpi, phase encoded tape transport)		
	Speed / Transfer Rate		
3842-x	12.5 ips / 20K bps	4,050	75
3843	25.0 ips / 40K bps	4,050	75
3844	12.5 ips / 20K bps	4,300	75
3845	25.0 ips / 40K bps	4,300	75
3846	37.5 ips / 60K bps	4,050	75
3847	45.0 ips / 72K bps	4,050	75
3848	37.5 ips / 60K bps	4,300	75
3849	45.0 ips / 72K bps	4,300	75
	Terminals		
3750	CRT Alphanumeric Display and Keyboard	3,120	25
	General-Purpose and Utility Interfaces		
1311	General-Purpose I/O Wire Wrap Board	150	–
1311-1	General-Purpose I/O Wire Wrap Board	550	–
1314	Multipurpose I/O Interface (MPIO)	890	20
	DATA COMMUNICATIONS		
1330-1	Asynchronous Communications Controller	1,100	15

Note: No leasing available

MODULAR COMPUTER SYSTEMS

MODCOMP I, II and IV



74-456

OVERVIEW

The MODCOMP computers are a family of highly modular, microprogrammed 16-bit-word machines with an assortment of RAM, ROM, and core memories that have an 0.8- or 1.0-microsecond cycle time per word. Three basic computers are offered: MODCOMP I, II, and IV, each capable of extensive expansion.

A variety of model numbers have been assigned to configurations that include various subsets of the available features and system options: I/5 and I/15; II/5, II/10, II/20, II/25, II/25 MCP, II/45, and II/45 MCP; IV/5, and IV/25. The II is also available in two system configurations, II/200 and II/220, that support the MAX III operating system. Modular has also developed a 32K-word core memory module that is mounted on one board; six new MODCOMP II computer models have been developed around the new board: II/12, II/26, II/26CP, II/201, II/221, and II/231. All models can be upgraded to higher models by adding options, except that 0.8-microsecond systems cannot use the new 1.0-microsecond 32K-word memory boards. The model package is less expensive than a lower model system that has been expanded in the field.

MODCOMP computers serve in widely varied applications. MODCOMP I was specifically designed as a small dedicated controller for real-time measurement and control functions. It can also operate as a stand-alone processor with a full complement of peripheral devices. The MODCOMP II is a general-purpose computer for measurement, control, communications (MCP models), and information processing.

The MODCOMP IV, which is upward compatible with the I and II, is a dual-word processor with a memory capacity of 262,190 16-bit words (512K bytes). Because of its dual-word orientation, MODCOMP IV can compete with 32-bit machines for many applications. The first MODCOMP IV was delivered in September 1974.

Modular Computer Systems offers a broad range of software for its computers. Packages available for MODCOMP I includes MAX I Executive, four assemblers, relocatable and link loaders, link editor, utilities, diagnostics, and communication line and remote data acquisition handlers.

MODCOMP II software includes three versions of the MAX III real-time operating system, as well as MAXCOM, MAXNET, Real-Time FORTRAN IV, three assemblers, BASIC, and Real-Time BASIC. Utility processors include a debug executive, source update, source maintenance control, library update, link editor, cataloger, and direct access maintenance processor. MAXNET is a newly announced operating system designed for distributed processing, while MAXCOM is a communications run-time system with low overhead.

MODCOMP IV software includes all the software for Models I and II, plus the MAX IV Real-Time Multiprogramming System (designed specifically for MODCOMP IV), extended BASIC, and RPG II. Machine support software incorporates a file management system, a sort/merge package, and a media-to-media conversion package. Several bisynchronous communication dialects, as well as a remote job entry capability, are available. Table 1 lists the mainframe characteristics.

The MODCOMP II was first announced in 1970 followed by the I in 1971, the II in 1972, and the IV in 1973. The III is no longer actively marketed.

PERFORMANCE AND COMPETITIVE POSITION

MODCOMP has an enviable record; it has doubled its sales each year since its founding in 1970 (a period noted for uncertain economy), and the company has consistently been ahead of sales forecasts. To date, Modular has delivered over 1,000 systems, the typical system currently shipped includes 48K words of core memory. Modular has been a quiet competitor that has never participated in the raucous fighting for the low end of the minicomputer market.

From 50 to 60 percent of new orders are from Modular customers. The company tries to stay out of markets where low price is the main criterion for an order. Instead, it seeks markets where no other company can do what Modular does.

However, as minicomputer manufacturers look for new markets to sustain their phenomenal growth rates, Modular Computer Systems, with its gross sales of $25,000,000 this year, will not be able to hide. When the company branches out into territories already served by Data General, Digital Equipment, and Hewlett-Packard,

Table 1. MODCOMP I, II, and IV: Mainframe Characteristics

MODEL			
CENTRAL PROCESSOR			
Type	Microprogrammed	Microprogrammed	Microprogrammed
Control ROM	Yes	Yes	Yes
No. of Internal Registers	3	16	Up to 16 sets of 16
Addressing			
Direct (no. of wds)	256	256	256
Indirect (no. of wds)	32K	64K	64K
Indexed	Yes	Yes	Yes
Instruction Set			
Implementation	81	106	242
Number (std, opt)	81	106-176	242
Floating Point	No	Opt	Opt
User-Microprogramming	No	Opt	Opt
Priority Interrupt			
Levels	2; 2*	4; 6*	8; 16*
Sublevels	16	64	64
MAIN STORAGE			
Types	Core; solid state	Core	Core
Cycle Times (μsec)	0.8	0.8 or 1.0	0.64
Basic Addressable Unit	Byte; word	Byte; word	Byte; word
Bytes/Access	2	2	2
Cache Memory	No	No	No
Capacity (min/max bytes)	4K-64K	8K-128K*	8K-512K*
Increment Size (bytes)		8K; 16K; 32K; 64K	
Ports/Module	1	1 std; 4 opt	1; 2; 4
Protection	—	Opt*	Opt*
Memory Management	No	No	Opt*
Error Checks	—	Parity option	—
ROM	1K; protect	No	No
INPUT/OUTPUT			
I/O Channels			
Programmed I/O	Std	Std	Std
DMA	Opt	Opt	Opt
Multiplexed	Opt	Opt (8-channel)	Opt (2-channel)
Max Transfer (wd/sec)			
Within Memory	135; 270	135; 270	769; 231
Over DMA	—	1,250,000	1,562,500
Over DMP	300K	300K	300K

*Depends on submodel or option.

the competition will be rougher. All the major manufacturers are going after the markets for substantial minicomputer systems: Digital with its PDP-11/40, 11/45, and 11/50; Data General with its ECLIPSE; and Hewlett-Packard with its 21MX and 3000. Other competitors are General Automation SPC-16, Interdata 7/16 and 7/32, Microdata 3200, Xerox 530, and CDC System 17.

The manufacturers of all these systems recognize that real-time, on-line applications and network processing fit the traditional minicomputer environment better than the batch environment exploited so long by the large mainframe manufacturers. The real-time operating systems with foreground/background processing were developed for real-time control applications, test and measurement, and data acquisition. The demands made by these real-time applications for on-line program development, backup to avoid downtime, fast response times, and program protection are the same ones now required for real-time, on-line commercial processing.

All the minicomputer manufacturers are scrambling to get a firm place in the market before the large mainframes can become on-line transaction oriented. Furthermore, the large mainframe manufacturers not only expect larger markups on their system prices than minicomputer manufacturers; they cannot yet compete on a price/performance basis with minicomputers.

Modular's spectacular success proves the validity of its goals. Its system and software orientation has worked. Still, the pressure on the low end of the minicomputer market from microprocessors and the saturation of the market to sophisticated end users have forced all serious minicomputer manufacturers to become system- and software-oriented. Thus, Modular will have to try harder if it is to continue its winning ways as an unquiet competitor.

MODCOMP IV's double-precision instruction set appears to make the system considerably faster than the PDP-11/40 and ECLIPSE for fixed-point double-precision arithmetic. The IV's floating-point hardware, on the other hand, is no faster than the floating-point hardware for the PDP-11/40 and is slower than the new unit for Data General's ECLIPSE. The main area where the IV appears to be at a competitive advantage over these other two systems is in its I/O channel arrangement and multiple ports to memory. Since MODCOMP IV can have up to four memory ports per module, the effective I/O transfer rate can be 3.75 million words per second without degrading processor throughput.

Because of its low price, systems built around MODCOMP's new memory board cost 18 to 27 percent less than comparable configurations using 16K-word boards. The 32K-word module is also substantially more reliable than two 16K-word modules; it has less components and less interconnectors to fail. The MTBF is expected to be 60,000 hours. Currently, the new memory module is available for MODCOMP II only; it will be available for the IV later.

Modular sees Hewlett-Packard as its strongest communications competitor. The Hewlett-Packard 9700 Distributed Processing System is most similar to MAXNET III. Data General's ECLIPSE system also has well-developed software and hardware facilities for distributed processing systems.

USER REACTIONS

Users interviewed included two OEMs as well as six end users. All customers except one end user are extremely satisfied with their systems and would buy more MODCOMP computers. The one user who had trouble with his system reported less than 10 percent downtime. His system has equipment built especially for the application; it had a few faulty chips, an I/C that was too fast for the application, and a fluke in a multiplexor design which caused trouble during test but not in normal operation. This user, however, is buying three more systems.

Other users feel the architecture is good, the hardware reliable, and the software powerful. One user who is not computer oriented mentioned that MODCOMP FORTRAN allows him to program the system interface to his process control hardware. Most users, including the two OEMs, consider MAX III an excellent base operating system. One OEM who uses the II/25 adds an uninterruptible power supply that keeps current within two percent of ideal; the systems have been installed for several months with no failures.

Several users mentioned that it is easy to interface nonstandard devices to the MODCOMP computers. One user selected a MODCOMP computer because an adapter to interface it to a CDC 6000 system is a standard product. This company has a MODCOMP III, another III on order, and a MODCOMP I. It plans to add 30 or more MODCOMP computers in the future.

Our interviews indicate that Modular Computer Systems maintains a good relationship with its users. Most either expressed an intent to buy more MODCOMP computers or said they would buy another MODCOMP system when needed.

CONFIGURATION GUIDE SYSTEM DESIGN

MODCOMP I is available in two models: the barebones I/5 and the I/15 for larger configurations. Model I/5 can be field upgraded to a I/15. The I/15 includes the arithmetic unit, general register file (three registers), modular bus control interface, priority interrupt system with two levels (16 sublevels each), basic control panel, memory expansion to 32,768 words, power supplies and an 8¾-inch rack-mountable enclosure.

The I/15 incorporates the following features in addition to the I/5 features: an option plane with power for two optional features (multiply/divide, custom macro instructions, direct memory processor, Teletype and paper tape reader controller, and asynchronous data modem interface); hardware fill; real-time clock; Teletype controller; I/O connector assembly; and mounting slides.

Memory for either the I/5 or I/15 system can consist of up to 32K words, composed of core, solid-state RAM, solid-state ROM modules, or a combination of all three types. Core is available in modules of 2K, 4K, 8K, and 16K words. RAM is available in 2K-word modules only. ROM is available in 512-word modules only. Memory parity of the bit per byte is optional. Cycle time for all memory is 0.8 microsecond per word.

A power failsafe and auto-start feature is optionally available for either system. With the direct memory processor for automatic block transfers, the system can handle up to eight peripheral devices concurrently for an aggregate maximum transfer rate of 300K words per second.

Peripherals include a variety of high-speed, low-speed, process I/O, and communications attachments as listed in Table 2. Table 3 lists the hardware configurations required by the major software packages.

MODCOMP II is available in 15 versions, which can be roughly grouped into minimum, MAX II, MAX III, and communications configurations. Nine models use 0.8-microsecond memory modules like those on the MODCOMP I, and six models use the new 1.0-microsecond 32K-word boards. Each model represents a different configuration package, which is priced lower than a bare-bones system with all options added in the field. Table 4 shows the components of each submodel.

A minimum configuration (II/5) includes an arithmetic unit, a read-only control memory, a general register file (15 registers), register I/O and three interrupts (two I/O and unimplemented instruction trap), hardware fill, an operator console, memory expansion to 32K words, power supplies, and an 8¾-inch rack-mountable enclosure.

Four external priority interrupts are options with all models. All features are standard for a model, except maximum memory capacity and different speed memory modules, which are optionally available for the other systems. All peripherals available for MODCOMP I can be used on the II.

Table 2. MODCOMP I, II, and IV: Peripherals

DEVICE MODEL	DESCRIPTION
Discs	
4102-4103	Fixed-head discs; 128K-, 256K-, 512K-wd capacities
4106	Fixed-head discs; 1M capacity
4108	Fixed-head discs; 384K-wd capacity
4126/4127	1M-wd moving-head discs; 97.8K wds/sec transfer
4128/4129	2M-wd moving-head discs; 97.8K wds/sec transfer
4132/4133	12M-wd moving-head discs; 156K wds/sec transfer
4134/4135	26M-wd moving-head discs; 156K wds/sec transfer
Magnetic Tape	
4148/4151	9-trk; 800 bpi, 45 ips
4149/4152	7-trk; 556/800 bpi, 45 ips
4155	9-trk; 1,600 bpi, 45 ips
4160/4162	9-trk/7-; 12.5 ips
Keyboard Printers	
4233-4235	ASR 33; KSR 35; ASR 35 respectively; local
4223-4225	ASR 33; KSR 35; ASR 35 respectively; remote
Paper Tape	
4511/4513	625-cps readers
4512	625-cps reader and 110-cps punch
Cards	
4411/4412	300/1,000-cpm readers
4421	100-cpm punch
Printers	
4211/4214	600/300 lpm; 132-col
4213	50-150 lpm; 132-col
Process I/O	
1200/1500	High-level analog input subsystem; single-ended/differential input
1300	Wide-range analog input subsystem, to 512-channel bipolar signal
1400	Wide-range relay analog input subsystem, to 512-channel bipolar system
1500	Modular data acquisition subsystem; 7 I/O modules
1199	Modular I/O interface subsystem to 16 (16-bit) channels
Communications	
1906	Universal controller (2/system) for 4-32 full-duplex channels
1905	Async controller (4/system) for 2-32 full-duplex channels
5710	Freestanding process data terminal
1115/1116	Async comm interfaces; 110-9,600 baud; 1 half-duplex channel
4810/4811	Async comm interfaces; 75-9,600 baud; 2 full-duplex channels
1911/1912	Async comm channels 2 full duplex lines
4825	Sync comm interface; 110-20K baud; 2 full-duplex channels
4820	16-bit parallel computer link; 100K wds/sec
5813	Async interface with remote fill hardware; 75-9,600 baud, 1 duplex channel
5820	High-speed computer link; 15K-125K wds/sec; 2 half-duplex channels and remote fill

Table 3. MODCOMP I, II, and IV: Software

Device Model	Description
MAX I	Core-resident batch system; requires 4K words of memory, ASR 33; for MODCOMP I
MAX II	Core for disc-resident batch system; requires multiply/divide, 12K words of memory, ASR 33, binary I/O device/paper tape, card, or mag tape; disc version requires DMP channel and 128K-word disc; for MODCOMP II or III
MAX III	Real-time multiprogramming system with foreground/ middleground/ background modes; foreground requires CPU multiply/ divide, 12K words of memory, ASR 33 console; background needs protect and 24K memory; disc version requires 128K disc; extended disc version requires 24K words of memory, 256K words disc; for MODCOMP II or III
MAX IV	Mapped version of MAX III for up to 256K words, (4 maps); requires MODCOMP IV CPU, 24K words of memory, 2.5M disc, ASR 33
MAXCOM	Communications run-time system for high throughput, low overhead; requires 4K words of memory, communications interfaces
MAXNET	Distributed network operating system; requires CPU, 32K words of memory, disc, ASR 33, communications links to satellite CPUs; for MODCOMP II
Assemblers	Standard requires 2K words of Memory and ASR 33; Extended requires 4K words of memory, real-time clock, and ASR 33; Macro requires 12K-word memory and II or IV CPU
Cross Assemblers	IBM 360/370, CDC 6000; both require 65K bytes of memory, card reader, line printer, card punch, disc or mag tape
FORTRAN IV	ANSI 2.9 1966; requires CPU, 20K words of memory, console
BASIC	Subset of macro assembler; generates absolute or relocatable code; also multiterminal Extended version; requires 12K memory, ASR 33
Utilities	Diagnostics, editing, media conversion loaders, debugging, math library

MODCOMP IV Dual Word Processor Computer is marketed in two basic configurations: the IV/10 and the IV/25. The IV/10 consists of a 32-bit and 16-bit arithmetic unit with multiply and divide hardware, a 32-bit parallel bus, executive features (real-time clock, console interrupt, and task scheduler interrupt), 15 general-purpose registers, a priority interrupt system with eight levels (expandable to 16 levels), 32K bytes of core memory with an effective cycle time of 640 nanoseconds for 16-bit words and 1.2 microseconds for 32-bit words, memory parity, memory expansion to 128K bytes with one, two, or four ports to memory, a power failsafe/auto start, control console, and a stall alarm.

Table 4. MODCOMP II: Submodels

SUBMODELS	5	10	20	25, 25CP	45, 45CP	200	220	12	26, 26CP	201	221	231
MEMORY												
Capacity												
Min K Bytes	8	32	8	32	32	64	64	64	64	64	64	64
Max K Bytes	64	64	128	128	128	128	128	128	128	128	128	128
Increments (K bytes)	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	8/16/32	64	64	64	64	64
Cycle (μsec)	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0
Parity	–	Std	–	Std	Std	Std	Std	Std	Std	Std	Std	Std
Protect	–	–	–	–	–	Std	Std	–	–	Std	Std	–
Ports	1	1	1	1	4	1	1	1	1	1	1	1
CPU												
Multiply/Divide	–	–	–	–	–	Std	Std	Std	Std	Std	Std	Std
INPUT/OUTPUT												
DMA	–	–	–	–	–	Std	Std	–	Std	Std	Std	Std
Modular Bus Control	–	–	–	–	–	–	–	–	–	–	–	Std
Peripheral Control	–	–	–	–	–	Std	Std	–	–	–	–	Std
Communications Macros	–	–	–	On CP	On CP	–	–	–	On Cp	Std	Std	–
Universal Communications MUX	–	–	–	–	–	–	–	–	–	–	–	Std
MUX Control	–	–	–	–	–	–	–	–	–	–	–	Std
Console/Paper Tape	–	–	–	–	–	Std	Std	–	Std	Std	Std	Std
Disc	–	–	–	–	–	–	Std	–	–	–	Std	–

The IV/25 has all the features of the IV/10 plus 16 sets of general-purpose registers (16 registers per set) and a memory management system permitting expansion to 512K bytes, which includes 1,024 memory mapping registers organized in four files of 256 registers, automatic memory allocation hardware, and memory protect on the basis of a 256-word page.

Optional features for the IV include 32K-byte modules of core memory, a simultaneous direct memory processor for up to 12 device controllers, an extended arithmetic unit for floating-point arithmetic (32-bit, 48-bit, and 64-bit operands), system protect compatibility with MODCOMP II, and 3-level increment of external interrupts.

Dual II and IV processors can share common core modules by way of the multiple port option. Special system products are available to link a MODCOMP computer to a CDC 3000 or 6000 by way of the CDC 3000 data channel, or to an IBM System/360 or 370 selector or multiplexor channel. Peripheral controller switches are also available for program or manual switching of up to four controllers between two MODCOMP computers.

The 32K-word memory module and the MAXNET IV communications package are under development for the IV.

COMPATIBILITY

MODCOMP systems are upward compatible in both hardware and software. The same functional hardware modules and the same peripheral devices are used in all systems. All programs are upward compatible.

In addition, programs assembled on large MODCOMP II, III, or IV configurations can run on small MODCOMP II or III configurations because unimplemented instructions are trapped and simulated by subroutines. Programs assembled on MODCOMP II or IV using the MODCOMP I instruction set can run on MODCOMP I.

FORTRAN-coded cross assemblers allow compilation of MODCOMP programs on the IBM System/360 and System/370 computers.

MAINTENANCE

Modular Computer Systems has 14 sales and 21 service centers located in the United States, Canada, and Puerto Rico. European headquarters are in Surrey, England, with marketing also in Germany. The company plans to expand its marketing organizations in Europe, Canada, and South America in fiscal 1975; currently only 15 percent of sales are from customers outside the United States.

Modular Computer does not rent systems. The company has four maintenance plans for purchased systems: resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis. Full service provides both scheduled and on-call emergency services for a single fee, while the other two plans are priced separately.

PRICE DATA

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE		
	MODCOMP I		
I/5	General-Purpose 16-Bit Digital Computer	2,000	16
I/15	General-Purpose 16-Bit Digital Computer (same as I/5 except includes 3130 option plane, 3742 hardware fill, 3743 real-time clock, 3751 Teletype controller, 3750 control panel interface, 3131 programmer's control panel, 0011 I/O connector assembly, 0010 mounting slides)	3,600	25
I/25	General-Purpose 16-Bit Digital Computer (same as I/15 except with 16,384-word memory module; memory parity; power fail-safe/auto start)	7,400	64
	I/5 and I/15 Memory (max 32K)		
	Read/Write Core Memory (0.8-μsec cycle time)		
3603-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3607	Memory Parity	500	3
	I/5 and I/15 Processor Options		
3504	Multiply/Divide	700	4
3505	Custom Macro Instructions (requires 3130)	NA	NA
	MODCOMP I Input/Output and Interrupt Options		
0010	Slides for MODCOMP I Enclosure (for I/5 only)	70	NA
0011	I/O Connector Assembly	60	NA
3130	Option Plane	200	1
3131	Programmer's Control Panel	250	2
3709	Direct Memory Processor (requires 3130)	1,000	5
3741	Power Fail-Safe/Auto Start	300	2
3742	Hardware Fill	400	2
3743	Real-Time Clock	300	2
3750	Programmer's Control Panel Interface	150	1
	MODCOMP II		
II/5	General-Purpose 16-Bit Digital Computer (with 16,384-word memory included)	9,500	8
II/10	General-Purpose 16-Bit Digital Computer (same as II/5 except has multiply/divide; power fail-safe/auto start; memory parity; priority interrupts for executive features; executive features; and 16,384-word memory)	11,500	93
II/12	General-Purpose 16-Bit Computer (same as II/5 except 32K-word memory; arithmetic unit; ROM; memory expansion to 64K words; gen reg file with 15 regs; reg I/O and 8 interrupts; multiply/divide; power fail-safe/auto start)	13,000	
	With 64K-Word Memory	21,000	
II/20	General-Purpose 16-Bit Digital Computer (same as II/5 except modular bus control interface and memory expansion to 65K words)	5,000	50
	With 16,384-Word Memory Included	10,000	83
II/25	General-Purpose 16-Bit Digital Computer (same as II/20 except has multiply/divide; power fail-safe/auto start; memory parity; interrupt levels for executive features; executive features; and 16,384-word memory)	12,500	95
II/25/CP	Communication Processor (same as II/5 with 3513 communication macros and modular bus control logic)	16,000	130
II/26	General-Purpose 16-Bit Computer (same as II/12 with modular bus control interface and controller for both console and p tape reader; expandable for high-performance floating-point processor)	16,000	
	With 64K-Word Memory	24,000	
II/26CP	General-Purpose 16-Bit Computer (same as II/26 with communications macros and modular bus control logic)	20,500	
	With 64K-Word Memory	28,500	
II/45	General-Purpose 16-Bit Digital Computer (same as II/25 with Controller for Teletype and p tape reader; executive features)	16,500	135
II/45/CP	Communications Processor (same as II/45 with communication macros and modular bus control logic)	20,000	170
II/200	Computer System (II/25 CPU with 32,768 words of 800-nsec memory; CPU options required to support MAX III together with a PCI)	19,500	148
II/201	Computer System (same as II/26 with peripheral controller interface enclosure, direct memory processor, system protect; 1 cabinet included)	16,500	
	With 64K-Word Memory	24,500	
II/220	Computer System (II/25 CPU with 32,768 words of memory; options to support MAX III, PCI; moving-head disc; 2 cabinets)	32,000	260
II/221	Computer System (same as II/201 with 2.5M-word moving-head disc; 2 cabinets)	30,000	
	With 64K-Word Memory	38,000	
II/230	Communications System (II/25/CP with CPU options to support MAXCOM software system; PCI and universal communications multiplexor; mounted in 2 std cabinets)	29,500	219
II/231	General-Purpose 16-Bit Computer (same as II/26CP with peripheral control interface enclosure; direct memory processor; multiplexor controller and universal multiplexor; 2 cabinets included)	27,500	
	With 64K-Word Memory	35,500	

PRICE DATA (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSORS AND WORKING STORAGE (Cont'd.)		
	Memory Options for MODCOMP II		
	Read/Write Core Memory (0.8-μsec cycle time)		
3601-1	4,096 Words	2,400	12
3608	8,192 Words	4,200	21
3609	16,384 Words	6,500	33
3618	8,192 Words	4,200	21
3619	16,384 Words	6,500	33
3606	Memory Parity	500	3
	II/5/10/20/25 Processor Options		
3503	Multiply/Divide	500	3
3512	Hardware Floating Point	4,000	20
	Input/Output and Interrupt Options		
3704	Direct Memory Processor	1,500	8
3708	External Direct Memory Processor	4,000	40
3629	System Protect Feature (requires 3731)	1,000	5
3730/1	Priority Interrupt Group	500	3
3732	External Priority Interrupt (4 interrupt levels)	500	3
3737	Executive Features (includes real-time clock with 5-msec interrupt, console interrupt, and task scheduler interrupt; requires 3730)	500	3
3739	Power Fail-Safe/Auto Start Feature	500	3
	MODCOMP IV		
IV/10	General-Purpose Digital Computer	15,500	148
IV/20	General-Purpose Digital Computer (same as IV/10 with memory expansion to 384K bytes; context switching file with 240 reg; memory management system including 1,024 memory mapping reg consisting of 4 files of 256 registers each; auto memory allocation hardware; memory protect on a 256-word basis)	19,500	188
IV/25	General-Purpose Digital Computer (same as IV/10 with 16 sets of general-purpose registers containing 15 registers/set; memory management system permitting expansion to 512K bytes, including: 1,024 memory mapping registers consisting of 4 files of 256 registers each, automatic memory allocation hardware, and memory protect on a 256-word basis; 4-port memory interface)	23,500	224
	IV/10 and IV/25 Memory		
3661	Core Memory Module (32K bytes; 16-bit cycle time — 640 nsec; 32-bit cycle time — 1.2 μsec; 1 module included with CPU and required for lower half of each 64K-byte module pair)	8,000	40
3662	Core Memory Module (same as 3661 except used in upper half of each 64K-byte module pair)	6,000	30
	IV/10 and IV/25 Processor Options		
3712	Simultaneous Direct Memory Processor	4,000	30
3646	Dual Memory Ports	6,500	55
3515	Extended Arithmetic Unit	5,500	28
	IV/10 and IV/25 Input/Output and Interrupt Options		
3631	System Protect	1,500	8
3734	External Interrupt Group	500	3
3134	Remote Control Console Control Panel and Enclosure	1,000	10
	Input/Output and Interrupt Options for MODCOMP II		
3751	Controller (for Teletype and p t reader)	400	2
3752X	Controller (for async RS232C-compatible console device and for p tape reader)	400	4
3753-X	Controller (for async 420 console device and for p tape reader)	400	4
	MASS STORAGE		
	Fixed-Head Discs		
4103	262,144 Words (8.7-msec avg access time)	15,000	105
4104	524,288 Words (same as 4103)	19,000	133
4106	1,048,576 Words (same as 4103)	38,000	170
	Moving-Head Discs		
4126	1,299,200 Words (70-msec avg positioning time; 20-msec avg latency)[3]	11,000	99
4127	1,299,200 Words (same as 4126 except controller not included; requires 4126)[3]	7,000	84
4128	2,598,400 Words (same as 4126)[3]	14,000	126
4129	2,598,400 Words (same as 4128 except controller not included; requires 4128)[3]	10,000	111
4132	12,312,230 Words (35-msec avg positioning time; 12.5-msec avg latency)[3]	23,000	145
4133	12,312,230 Words (same as 4132 except controller not included; requires 4132)[3]	18,000	130
4134	26,624,640 Words (same as 4132)[3]	28,000	185
4135	26,624,640 Words (same as 4134 except controller not included; requires 4134)[3]	23,000	160
4140	Disc Cartridge (for 4126-4129)	180	NA
4141	Disc Pack (for 4132-4135)	500	NA

PRICE DATA (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	INPUT/OUTPUT DEVICES		
4903[2]	Peripheral Controller (for 1-4 controllers)	1,200	6
4906	Peripheral Controller (switch for programmed switching of up to 4 controllers between 2 MODCOMP computers)	3,000	25
4701	Interval Timer	1,000	5
4701-10	External Clock	1,000	5
4801	General-Purpose Controller Module	600	—
4705-1	General-Purpose 16-Bit Data Terminal	1,500	15
4810/4811	Asynchronous Communications Interface	1,250	13
4815/17	Synchronous Communications Interface (2 full-duplex channels)	1,250	13
4820	Computer Link	4,000	40
	Teletypewriters		
4205	Data Communication Printer (tabletop; KSR; 30 cps)	4,400	38
4206	Data Communication Printer (same as 4205 except 120 cps; 120 print col; external forms tractor)	6,100	54
	Remote Teletypewriters		
4223	ASR 33	1,250	12
4224	KSR 35	3,250	55
4225	ASR 35	5,250	61
	Console Teletypewriters (require 3744 or 3751)		
4233	ASR 33	1,500	
4234	KSR 35	3,500	
4235	ASR 35	5,500	
3747/9	Programmable Power On/Off Controls for 4233 Teletypewriters	300	—
4253	Programmable Power On/Off Control for 4223 Typewriter	300	2
	Paper Tape		
4512	Paper Tape Reader and Punch	5,000	42
4513	Paper Tape Reader	2,000	12
	Floppy Discs		
4521	150-Word Storage Capacity (controller included)	4,000	40
4522	Dual; 300K-Word Storage Capacity	6,000	60
	Punched Card [3]		
4411	Card Reader (300 cpm; controller included)	4,000	24
4412	Card Reader (same as 4411 except 1,000 cpm)	9,000	54
4421	Card Punch (100 cpm; controller included)	30,000	162
	Line Printer [3]		
4211	600 lpm, 132 Columns	17,900	125
4213	50-150 lpm, 132 Columns	7,000	91
4214	300 lpm, 132 Columns	14,000	91
	DATA COMMUNICATIONS		
1905	Controller (for async communications multiplexor)	1,200	12
1910	Asynchronous Communications Multiplexor	1,600	16
1911/2/3	Asynchronous Communications Channel	500	5
1906-1	Controller (for universal communications multiplexor)	4,500	45
1920	Universal Communications Multiplexor	1,600	16
1922/3	Synchronous Communications Channel	1,200	12
1924/5/6	Asynchronous Communications Channel	1,000	10
1941	MODCOMP-CDC Satellite Coupler	8,000	80
1950	MODCOMP-IBM 360/370 Interface	7,000*	70
4216	Electrostatic Printer	9,000*	99
4217	Electrostatic Printer/Plotter	13,000	140
4219	VERSAPLOT Plotting Software	1,500*	—
4426	Keypunch/On-Line Card Punch/Automatic Interpreter	15,000	110

* Delivery subjects to home-office quotation.

Notes:
(1) Modular Computer has 4 maintenance plans — resident service, full service, scheduled maintenance, and on-call. Resident service provides a trained service engineer on a 1-shift basis at a cost of $32,000/year. This column lists the full-service maintenance charge. Cost of other plans available on request.
(2) No charge if purchased in conjunction with 3 or more peripheral controllers or analog input subsystem controllers.
(3) Requires any 4900 Series peripheral control unit.

HEADQUARTERS

Modular Computer Systems
1650 W. McNab Road
Ft. Lauderdale FL 33309

(See report number S700.011.203/180.5025.203 for MODCOMP Computers OVERVIEW, COMPETITIVE POSITION, USER REACTIONS, CONFIGURATION GUIDE, and COMPATIBILITY.)

MAINFRAME

The MODCOMP mainframe is modular, expandable, and flexible. Smaller MODCOMP computers are limited, dedicated machines. Multiprogramming is available in the middle range of MODCOMP II models configured to execute the MAX II software system. The MAX IV operating system, upward compatible with MAX III, makes use of the memory management facilities available only on the MODCOMP IV. MAX III and IV provide three operating levels for program execution: foreground, middleground, and background. MODCOMP II and IV processors can share common memory modules by way of multiple ports.

The MODCOMP IV includes two independent Arithmetic/Logic Units (ALUs) to allow parallel processing of a 32-bit doubleword or simultaneous mixed arithmetic and logical functions.

CENTRAL PROCESSORS

The central processors of the MODCOMP I, II, and IV are essentially the same CPU but with various extensions to increase the capabilities of the system. MODCOMP II, for instance, adds a more extensive I/O subsystem and can add more ports to memory. Instruction sets can be altered from model to model by changing the ROM controller because the system is microprogrammed. Figure 1 shows block diagrams comparing typical II and IV systems.

Data Structure. The 16-bit word is the basic information format for the MODCOMP computers. Some instructions operate on doublewords consisting of 32 bits stored in consecutive registers or memory locations. Many instructions and peripheral devices operate on 8-bit bytes packed two per register or memory location. Hexadecimal digits are often used as a convenience in representing binary, byte, word, or doubleword values. ASCII is the standard character code in MODCOMP computers and peripherals. Parity adds one bit per byte.

Fixed-point binary integer format is the standard arithmetic format; it consists of a sign bit (the most significant) and 15 or 31 data bits. Two's complement representation is used for negative numbers. The floating-point format consists of a 9-bit binary exponent and a 22-, 38-, or 54-bit signed binary fraction. Hardware sets the exponent to all zeros if the fraction is zero.

Special Registers. MODCOMP I has three general registers, all of which can be used as index registers. MODCOMP II and IV have 15 general registers; seven can be used as index registers. In addition, the data entry register on the control panel of all the models is addressed by instructions as a general register.

Operands and intermediate results for almost any subroutine can be held in the register file and operated on by the fast register-to-register instruction set.

The MODCOMP IV utilizes 15 general-purpose registers and an optional 240-word context file that can save 16 unique copies of the 15 registers. One 15-word block at a time operates as the active general register set. Hardware interrupts can assign any one of the copies to the interrupt level. Switching register sets occurs in approximately the same amount of time as a normal interrupt entry. Surplus sets of registers can be assigned to the system context switching routine for use in different user and executive tasks.

Addressing Facilities. Four memory addressing modes — direct, indexed, immediate, and short displaced — are provided in MODCOMP I instructions. MODCOMP II includes these four plus indirect, indexed and indirect, and short indexed. The MODCOMP IV adds relative branch addressing and a program mode-controlled virtual addressing hardware option. In each of the modes, except virtual addressing, a 16-bit effective word address is calculated in the CPU and sent to the memory system along with a read and write request. The effective word address provides an addressing range of 65,536 words.

Direct, indirect, indexed, and indexed with indirect addressing modes use a 2-word instruction format. The first word contains an 8-bit operation code field and a second 8-bit field divided into two subfields. One subfield selects a general register; the other specifies a second general register, an index register, or the displacement with respect to a register. The second word contains a 16-bit address.

When indexing is specified, the effective address is the sum of this value and the contents of the specified general register. Indexing does not increase execution time. Indirect addressing, for which one level is provided, adds one memory cycle to the instruction execution time. When indexing and indirect addressing are specified in the same instruction, indexing is performed first.

Immediate mode uses the 2-word format. The second instruction word contains an operand.

The short displaced mode uses a singleword format to process lists of operands occupying 16 or less consecutive memory locations. In this mode, the displacement specified in the second subfield and the contents of the base register are added to generate the effective word address.

The set of byte instructions can address any byte in memory, and the bit manipulation instructions can address any bit in memory or in a general register.

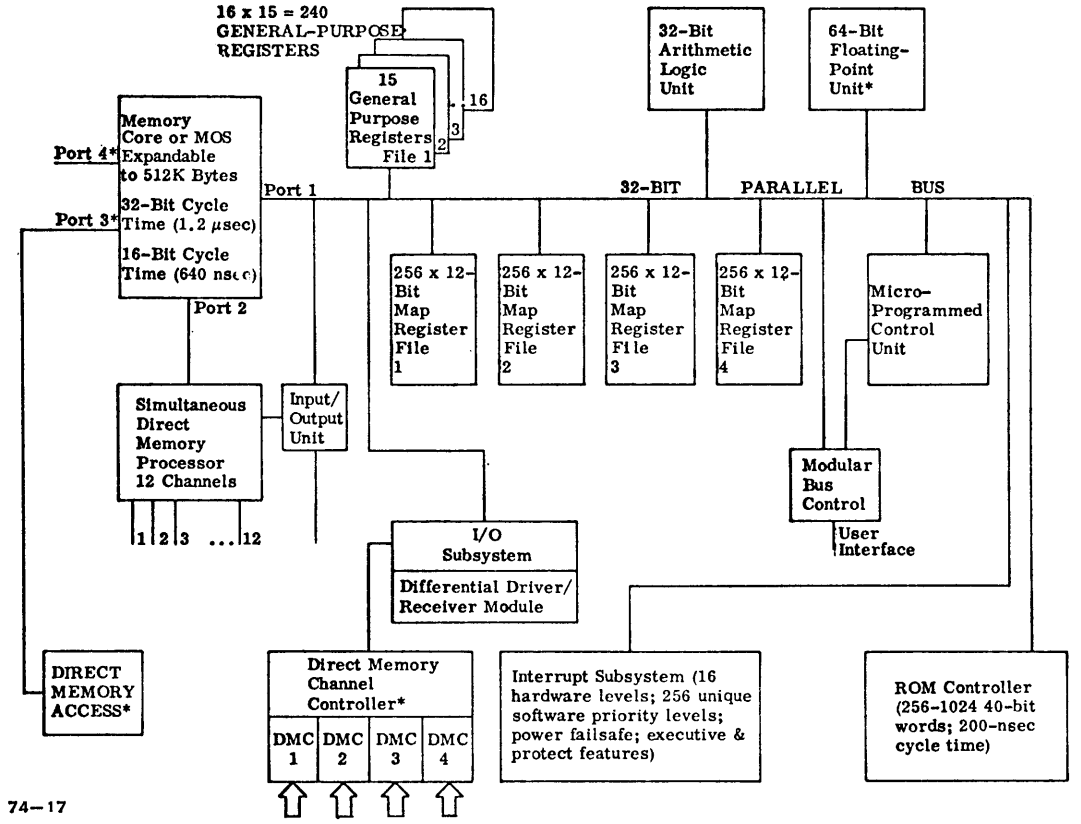


Figure 1. Comparison of MODCOMP II and IV Architecture

MODCOMP IV offers, as standard, addressing modes that are compatible with MODCOMP II plus virtual addressing modes for systems with more than 64K words of memory. The short addressing mode is extended on the IV to include a relative branch addressing mode. Relative branch addressing provides both conditional and unconditional branch instructions that use an 8-bit displacement field and algebraically add this sign-extended field to the program register to effect branches or hops (skips).

The virtual addressing mode does not alter the MODCOMP II-compatible address generation but simply uses the final effective MODCOMP II-compatible address as a virtual 16-bit address. The virtual addressing option adds a 2-bit map select register and four memory maps. Each map contains 256 words, 12 bits each, to provide 10 address bits to select a 256-word physical page and a 2-bit system-protect/access-rights control code. The protect code provides four levels of access protection.

Instruction Set. A summary of the instruction set and typical execution times is given in Table 1. Three principal instruction formats are used: singleword, immediate, and doubleword.

All register-to-register, shift, I/O, control, and many of the memory reference instructions use the singleword format. The immediate addressing mode uses a doubleword format; the second word is the operand. In doubleword format the second word contains either a 16-bit operand address or an indirect address.

Multiply/divide instructions are optionally available with MODCOMP I and II and are standard on the IV. A MODCOMP II computer that includes this optional instruction set can execute MODCOMP III software. Floating-point arithmetic is an option for MODCOMP II and IV. The MODCOMP IV also provides a branch and link instruction as well as a full set of conditional skip instructions based on the setting of the condition code.

Interrupt Control. MODCOMP I has two interrupt levels, expandable to four; MODCOMP II has three levels, expandable to eight. The basic MODCOMP IV contains eight standard interrupt levels, expandable to 16 levels.

Each level on the MODCOMP I or II is assigned a pair of memory locations: one for the entry address of the interrupt routine and one for the return address. The return address is stored automatically when the processor grants the interrupt.

The MODCOMP IV has four dedicated memory locations per level: two store the entry and return addresses unique to each priority level and two store the old and new program status words.

On MODCOMP I and II, a program can selectively disable all levels except power failsafe. On MODCOMP IV, a program can disable all the external interrupt levels but the following levels are always enabled: levels 0 (power failsafe/auto start), 1 (memory parity), 2 (system protect), 4 (unimplemented instruction trap), and 5 (floating-point overflow).

All of the MODCOMP computers have the following two special program control features. Request signals for

Table 1. MODCOMP I, II, and IV: Typical Execution Times

Type	Execution Times (μsec)			
			MODCOMP IV(1)	
	MODCOMP I	MODCOMP II	16-Bit Mode	32-Bit Mode
Load and Store	1.6-2.4	1.6-2.4	1.6	2.4
Fixed-Point Binary				
(+)	0.8-3.4	0.8-3.4	1.6	2.4
(-)	0.8-2.4	0.8-2.4	1.6	2.4
(x)	10.27	6.0-7.2	–	–
(÷)	12.27	11.0-12.2	–	–
Floating-Point(2)				
(+, -)	–	15.0/20.5	–	6.24/10.1
(x)	–	12.5/16.0	–	5.2/8.0
(÷)	–	13.0/16.5	–	6.7/11.2
Logical	0.8-2.4	0.8-2.4	1.6	2.4
Branch	0.8-2.4	0.8-1.6	1.6	1.6
Shift	2.0 + 0.2(s-1)	2.0 + 0.2(s-1)	0.6	0.6
Control	0.8	0.8	–	–
Interrupt and Call	1.2-1.8	1.2-1.8	–	–
I/O	2.0-1.2	2.0-1.2	–	–

s – no. of shifts

Note:
(1) Using core memory; solid-state RAM will be slightly faster.

(2) Times listed are for single/double-precision formats, register to register.

all levels can be program generated both to aid in debugging and to reduce overhead in monitor operations. Also, the priority queue can be program manipulated by temporarily inhibiting the processing of interrupts below any selected level.

Two of the standard interrupt levels are party line and connect to all of the peripheral devices. Up to 64 devices can attach to each of these levels. The program connects devices to the levels, so only selected devices are linked to each level at a given time. One level is used by each device to request a character or word transfer and the other to signify an end-of-record or end-of-execution condition, if appropriate. The MODCOMP IV accommodates up to 16 distinct levels plus the common data and service interrupt levels which can each link to 64 different service routines for 142 unique external interrupt entry points.

Power failsafe/auto start feature is optional on MODCOMP I and II but standard on MODCOMP IV. When provided, it has the highest priority level, is always enabled, and cannot be disabled by instruction execution. If the power service voltage drops below the specified level, an interrupt is generated and at least 200 memory cycles are available in which to protect volatile data. When power is restored, memory writing is inhibited until the system is normalized.

An unimplemented instruction trap is a standard interrupt in MODCOMP II and IV. It occurs if the execution of an optional multiply, divide, macro, or floating-point instruction is attempted in a computer without provision for it. The executive features, optional on the II and III but standard on the IV, consist of three hardware features, each of which connect to a separate interrupt level and are required by MAX II, III, and IV software systems. They consist of a real-time clock, which generates an interrupt at a 120-Hertz rate derived from the ac power frequency; a console interrupt, which provides the operator with a switch to interrupt the computer without halting it; and a task scheduler interrupt issued by MAX III to maintain a software queue below the hardware priority queue. A 1,000-Hertz real-time clock interrupt is optionally available on MODCOMP I.

System protect is optionally available for MODCOMP II and IV/10 and standard on the IV/25. It offers memory protect and privileged instruction trap capabilities. The protect feature is enabled and disabled by a key switch on the control panel. When activated, the switch disables all other panel switches except the data switches and the console interrupt switch. As part of this feature, the memory parity signal connects to an interrupt level to permit response to a memory parity error by an interrupt routine rather than have the machine halt.

With memory protect, part of memory can be guarded against modification or entry by programs in unprotected memory. The resident executive and real-time tasks can be protected from modification by undebugged programs that are brought into core for execution. With the privileged instruction trap, no instruction that affects I/O, interrupts, or machine operating status can be executed by unprotected programs. A trap is generated at any attempt to execute one of the privileged instructions.

The four-level memory protect system, combined with the memory mapping segmentation of the MAX IV operating system, extends the memory protection system of the MODCOMP IV to both user and executive services. Programs can be protected in pages of 256 words by a 2-bit code that specifies the following: no access; read only; read and branch only; and read, branch, and write.

Console. The MODCOMP console is panel mounted. A remote control console option for the IV allows the console to be mounted on a table or desk 20 cable feet away from the CPU. The full complement of controls and indicators on the control panel is standard with MODCOMP II and IV but optional for MODCOMP I. Many MODCOMP I computers are dedicated and need only the RUN/HALT, FILL, and MASTER CLEAR switches provided on a basic control panel. The console features a full complement of indicators and switches to control the system.

Main Memory

All MODCOMP computers use core memory, solid-state ROM, solid-state RAM, or a combination of all three.

MODCOMP I can accommodate a maximum memory of 32K words. Memory modules are available in 2K, 4K, 8K, and 16K words for core memory, 2K words for solid-state RAM, and 512 words for solid-state ROM.

Maximum memory capacity is 32K words for the II/5 and II/10 and 64K words for all others, made up of 4K-, 8K-, 16K-, and 32K-word core memory modules. Memory parity is standard on the II/10, II/25, II/45, II/200, II/220, and optional on the II/15 and II/20. Model II/45 memory can have up to four ports of entry.

Cycle time for all 4K-, 8K-, and 16K-word boards on the I and II is 0.8 microsecond. The IV memory cycle time is 640 nanoseconds per 16-bit word and 1.2 microseconds per 32-bit dual word.

The new 32K-word board for the II includes 16 data bits and one parity bit per word. Cycle time is 1 microsecond per word. Effective cycle time is reduced to 850 nanoseconds when memory is expanded to 64K words because of overlapping memory accesses. Read access time is 420 nanoseconds.

MODCOMP IV has a maximum memory capacity of 64K words for the IV/10 and 256K words for the IV/25. Memory consists of 32K-byte core memory modules, made up of two 16K-byte modules interleaved. Cycle time is 640 nanoseconds per word and 1.2 microseconds per 32-bit dual word. Memory parity is standard.

The IV/25 has a memory management system that provides virtual memory addressing and memory protection. Memory management divides memory into pages of 256 words. A user's program can address 64K words of virtual memory; the virtual memory can be made up of 256 physical memory pages, and each page can have its own protect code.

Maximum transfer rate within memory is 135,270 words per second for MODCOMP I and II and 454,545 words per second optionally for MODCOMP II. Maximum transfer rate for the MODCOMP IV is 208,333 words per second for 32-bit dual words and 769,231 words per second for 16-bit words stored in core memory.

Maximum data transfer rate by way of DMP is 300K (I and II) and 400K (IV) words per second. The maximum transfer rate by way of DMA channel is 1,250,000 words per second (II) and 1,562,500 words per second (IV). A MODCOMP II with 4-port memories can transfer data from four different memory modules at 5 million words per second, while the MODCOMP IV with 4-port memories has a maximum transfer rate of 6 million words per second.

I/O Control

The basic I/O facility of the MODCOMP computers consists of a time-shared (party-line) bus capable of transferring data, commands, and device status. Data can be transferred between any general register and any of up to 64 addressable peripheral devices. Up to 16 bits can be transferred in parallel over the bus under program control. Three modes are available for program-controlled transfers: interrupt, test and transfer, and burst.

Interrupt mode can be used with any device that generates a transfer request signal. This includes all standard computer peripheral devices. The transfer request signal is connected to an interrupt level. Interrupt service routines can perform transfers and all required overhead functions at rates up to about 60K words per second.

Test and transfer mode consists of testing a device with a status instruction until the device is ready for a transfer. Individual device speed determines the maximum transfer rate in this mode.

Burst mode can be used with devices that can transfer a word any time the computer executes an I/O instruction to the device. Output bursts of up to 15 words (one per register) can be transferred at the rate of 833K words per second. Input bursts can be transferred at 500K words per second.

A DMA option is available for MODCOMP II and IV to handle customer or other special devices. It is not used by standard MODCOMP peripherals. DMA operates on a cycle-stealing basis except on systems that implement multiple memory ports. A second memory port enables the CPU and DMA to connect to different memory ports; thus, the processor and DMA can overlap memory accesses to different memory modules and effectively double the maximum transfer rate. Both the CPU and DMA can maintain maximum simultaneous memory transfer rates of 1.25 million words per second (II) and 1.56 million words per second (IV).

Direct memory channels (DMCs) are available for use with MODCOMP IV to handle word transfer rates of up to 1.56 million words per second. Up to four DMCs, using a common controller, can be attached. A separate transfer path between the channel and the peripheral controller or subsystem is provided for each DMC to support the high transfer rate and to avoid conflicts with the party-line bus. DMCs use the same memory port as the CPU; thus, they operate on a cycle-stealing basis.

MODCOMP IV computers with heavier I/O loading than can be supported by DMCs can be configured with a direct memory processor (DMP) connected to the memory through the second memory port. DMP options with different capabilities are available for all MODCOMP systems.

The DMP option provides direct memory access to four peripheral device controllers in a MODCOMP I computer, to 16 peripheral device controllers in a MODCOMP II computer, or to 12 controllers in a MODCOMP IV computer. A pair of dedicated memory locations is assigned to each of the device controllers — a transfer count (TC) location and a transfer address (TA) location. All of the controllers can transfer blocks of data to and from memory at the same time on an interleaved basis. Devices connected to DMP channels also accept transfer commands when not performing DMP-controlled block transfers. DMP transfers are made on the standard party-line bus for the I and II.

The four top-priority DMP channels on the MODCOMP II, all four channels on the I, and all 12 channels on the IV each contain a pair of 16-bit registers to hold both the memory address for the next transfer and the number of words remaining to be transferred in the current block. These channels can transfer words at combined rates of up to 400K words per second in MODCOMP IV or 300K words per second in MODCOMP I and II. The transfer parameters for the remaining DMP channels in MODCOMP II are stored in dedicated memory locations; these channels handle transfer rates of up to 180K words per second.

If a series of data blocks are to be transferred over a channel, the blocks can be chained together by setting a chain flag in the word count location. Any number of blocks can be chained together. Maximum block length is 16,384 words.

Two interrupts are associated with DMP. One is an end-of-block signal; the other is a service request signal, which occurs when the device is ready to transfer another block.

The DMP is used to connect such high-speed, block-oriented peripheral devices as disc units, magnetic tape units, and the High Level Analog Input Subsystem to the computer.

When the MODCOMP IV system includes more than 64K words of memory the DMP channels operate in virtual addressing mode. The channel TA registers in DMP are 18 bits long; thus, they can address any word in memory. When a DMP channel is initialized, its corresponding TA register is loaded with an address that has been translated using the operating system's map image and the task map image. Also, if blocks of data are chained together, each new virtual TA is translated into a physical address by way of the task map image.

PERIPHERALS

In MODCOMP computers, all peripherals except the directly connected teletypewriter and paper tape reader are attached by means of controllers packaged in a peripheral controller interface (PCI) enclosure. The PCI contains I/O bus and direct memory processor interfaces, plus the power supplies required by the controllers. Multiple PCI enclosures can be connected to one computer to enable use of almost any combination of peripherals. Unless otherwise noted for a specific device, the appropriate controller is included.

Low-Speed Peripherals

KEYBOARD PRINTERS

4233 Keyboard/Printer ASR 33 — 10 cps.

4234 Keyboard/Printer ASR 35 — 10 cps.

4235 Keyboard/Printer ASR 35 — 10 cps; not used with MODCOMP I.

4223 Remote Teletypewriter ASR 33 — 10 cps; requires 1115 async communications interface.

4224 Teletypewriter KSR 35 — 10 cps; requires 1115 async communications interface.

4225 Remote Teletypewriter ASR 35 — 10 cps; requires 1115 async communications interface.

PAPER TAPE

4511 Paper Tape Reader (and controller) — 625 cps; MODCOMP II only; computer console mounted.

4513 Paper Tape Reader (and controller) — 625 cps; MODCOMP I only; rack mounted.

4512 Paper Tape Reader and Punch (and controller) — 625 cps read; 110 cps punch; computer console-mounted reader; rack-mounted punch; for MODCOMP II.

PUNCHED CARD

4411 Punched Card Reader (and controller) — 300 cpm; tabletop model.

4412 Punched Card Reader (and controller) — 300 cpm; tabletop model.

4421 Card Punch (and controller) — 100 cpm; freestanding.

LINE PRINTERS

4211 Line Printer (and controller) — 600 lpm; 132-col; variable width; freestanding.

4213 Line Printer (and controller) — 50-150 lpm; 132-col; variable width; tabletop model.

4214 Line Printer (and controller) — 300 lpm; 132-col; fixed width; freestanding.

High-Speed Peripherals

FIXED-HEAD DISC STORAGE UNITS

4102 Fixed-Head Disc (and controller) — 131,072 words capacity; 8.7-msec access time (avg); 265K wd/sec transfer rate; rack mountable.

4103 Fixed-Head Disc (and controller) — 262,144 words capacity; 8.5-msec access time (avg); 130K wd/sec transfer rate; rack mountable.

4104 Fixed-Head Disc (and controller) — 524,288 words capacity; 8.5-msec access time (avg); 247K wd/sec transfer rate; rack mountable.

4106 Fixed-Head Disc (and controller) — 1,048,576 words capacity; 8.7-msec access time (avg); 265K wd/sec transfer rate; rack mountable.

4108 Fixed-Head Disc (and controller) — 393,216 words capacity; 8.7-msec access time (avg); 265K wd/sec transfer rate; rack mountable.

MOVING-HEAD DISC STORAGE UNIT

4126 Moving-Head Disc (and controller) — 1,299,200 words capacity; 70-msec head positioning time (avg); 20-msec latency (avg); 97.8K wd/sec transfer rate; rack mountable.

4127 Moving-Head Disc — same as 4126; rack-mountable; controller not included; used w/4126.

4128 Moving-Head Disc (and controller) — 2,598,400 words capacity; 70-msec head positioning time (avg); 20-msec latency (avg); 97.8 wd/sec transfer rate; rack mountable.

4129 Moving-Head Disc — same as 4128; rack-mountable; controller not included; used w/4128.

4132 Moving-Head Disc (and controller) — 13,000,000 words capacity; 35-msec head positioning time (avg); 12.5-msec latency (avg); 156K wd/sec transfer rate; freestanding.

4133 Moving-Head Disc — same as 4132 freestanding; controller not included; used w/4132.

4134 Moving-Head Disc (and controller) — 26,000,000 words capacity; 35-msec head positioning time (avg); 12.5-msec latency (avg); 156K wd/sec transfer rate; freestanding.

4135 Moving-Head Disc — Same as 4134, freestanding; controller not included; used w/4134.

MAGNETIC TAPE UNITS

4148/51 Magnetic Tape Unit (and controller) — 9-track; 45 ips; 800 bpi; 10.5-in. reel; cabinet included.

4149/52 Magnetic Tape Unit (and controller) — 7-track; 45 ips; 556/800 bpi; 10.5-in. reel; cabinet included.

4155 Magnetic Tape Unit (and controller) — 9-track; 45 ips; 1,600 bpi; IBM-compatible; phase encoding cabinet included.

4160 Magnetic Tape Unit (and controller) — 9-track; 12.5 ips; 800 bpi; rack mountable.

4162 Magnetic Tape Unit (and controller) — 7-track; 12.5 ips; 556/800 bpi; rack mountable.

Process I/O Peripherals

MODCOMP offers 4 analog input subsystems and an I/O subsystem.

1200 and 1500 High-Level Analog Input Subsystems (HLAIS) — provides analog multiplexing, Model 1200 for single-ended inputs and Model 1500 for differential inputs; HLAIS can select either randomly or sequentially, from 16 to 128 single-ended or differential inputs and digitize their analog values to 11-bit-plus-sign digital values at a 50-kilohertz throughput rate; choice of 8 different RC single-pole filter configurations.

Model 1300 Wide Range Analog Input Subsystem (WRAIS) — provides bipolar analog signal multiplexing; subsystem is expandable in 8-channel increments up to a total of 512 channels; 12 programmable input ranges from ± millivolts to 10.24 volts, full scale; allows many low-level signals or a variety of transducer types; zero suppression capability can be added to increase resolution; a choice of 7 RC single-pole or 7 double-pole filter configurations allows signal bandwidth limiting; standard throughput rate is 20 kilohertz; with zero suppression it is 10 kilohertz, and with auto ranging it is 6 kilohertz.

Model 1400 Wide-Range Relay Analog Subsystem — bipolar analog signal multiplexing for measurement and control applications; channel capacity can be expanded from the basic 128 to 512 in 8-channel increments, 12 programmable input ranges from ± 5 millivolts to ± 10.24 volts, full scale; opt zero suppression capability to increase its resolution from 12 to 15 bits option of 7 different RC single-pole input filters; 6 scan rates range from 5 to 100 samples/second.

Model 1600 Modular Data Acquisition (MODAC) Subsystem — provides data acquisition for a small number of analog and digital inputs and outputs; interface for up to 7 I/O modules; each digital input or output module handles 32 bits; each analog input module produces up to 8 outputs; MODAC Model 1600 operates with either MODCOMP II or IV, interfacing directly with the basic I/O bus.

Model 1199 Modular Input/Output Interface Subsystem (IOIS) — gives capability to input and output real-time information; can accept digital inputs and produce digital outputs, ac outputs, and analog outputs; can include communications line, CRT terminal, Teletype, and other interfaces; basic IOIS enclosure houses the controller, logic, and basic circuitry; can accommodate up to 16 interface channels of 16 bits each and options for 2 types of synchronizers, 2 interrupt couplers, and 1 external interrupt coupler; channel multiplexor can interface with 1 of the 16 basic channels to connect an expander unit (which adds 16 multiplexed channels); 4 such expander units can be attached to provide 64 multiplexed channels; up to 16 multiplexors can be accommodated in the basic IOIS file; options defining interface channel include logic level, positive or negative voltage, contact sense or closure, and analog output. Other options include a common alarm input channel, a storage display interface, and an asynchronous communications interface.

DATA COMMUNICATIONS

Modular Computer Systems offers two multiplexed data communications interfaces: the Model 1906 Universal Communications Controller, which can handle up to 64 full-duplex, synchronous, and asynchronous channels; and the Model 1905 Asynchronous Communications Controller, which can handle up to 128 full-duplex, asynchronous channels. A number of smaller interfaces and a special-purpose terminal device are also available.

1906 Universal Controller — connects 1 or 2 multiplexors; 3 program-selectable transfer modes can be used individually for each channel; DMP mode permits transfer of strings of data (1 to 1,024 bytes) automatically (any combination of channels can operate concurrently); interrupt-driven mode allows single-character transfer under program control, data interrupt is generated each time an active channel requires a data transfer; test and transfer mode similar to the interrupt-driven mode, except that the program addresses the channel and tests status to determine when service is required; multiplexor, used with the universal controller, accommodates 4 to 32 full-duplex channels, expandable in increments of 4 channels; with increment of either sync or async channels, each channel can be configured to interface Teletypes or RS232C or TTL-compatible modems.

Async Channel — EIA RS232C modems; TTL modems; TTY 60/20-ma current loop patchable rates from 75 to 9,600 baud w/max of 5 different rates/multiplexor; program selectable: codes 5, 6, 7, or 8 bits + parity, 1 or 2 program selectable stop bits program selectable: parity (none, odd, or even), echoes on full-duplex line.

Sync Channel — EIA RS232C modems; TTL modems patchable to 50K baud w/max of 5 different rates/multiplexor; patchable sync character.

1905 Async Controller — connects up to 4 multiplexors; permits CPU communication with each data channel in either the interrupt-driven transfer or the test and transfer modes; accommodates 2 to 32 full-duplex, async channels; capacity expands in 2-channel increments; each channel can be configured to interface Teletypes or RS232C or TTL-compatible modems.

5710 Freestanding Process Data Terminal — enables remote communication; 2 input capabilities, a static card reader, and a 16-key numeric display with decimal capability and a 24-position rear-projection display constitute output.

1115 Async Comm Interface — 110 to 9,600 baud, 20-ma current loop with 1 half-duplex channel.

1116 Async Comm Interface — 110 to 9,600 baud, RS232C-compatible with 1 half-duplex channel.

1911 Async Comm Channels — 110 baud, 60/20-ma current loop with 2 full-duplex lines.

1912 Async Comm Channels — 75 to 9,600 baud, RS232C-compatible with 2 full-duplex lines.

4810 Async Comm Interface — 75 to 9,600 baud, 20-ma current loop with 2 full-duplex channels.

4811 Async Comm Interface — 75 to 9,600 baud, RS232C-compatible with 2 full-duplex channels.

4815 Sync Comm Interface — 110 to 20K baud, RS232C-compatible with 2 full-duplex channels; supported with async line protocol.

4820 MODCOMP — 16-bit parallel computer link, 100K words/second.

5813 Async Comm Interface — 75 to 9,600 baud, 1 full-duplex channel and remote fill hardware; RS232C or current loop.

5820 High-Speed Serial Computer Link — 15K to 125K words/second, with 2 half-duplex channels and remote fill hardware.

SOFTWARE

Extensive software is available from Modular Computer Systems for its MODCOMP computers. The software is designed around a modular concept, which permits configuring it to match the hardware complement of a particular machine. Four Modular Application Executive (MAX) systems have common interfaces between modules and language processors. A MAX system can be tailored, by means of a system generation procedure, to match the hardware configuration and to contain desired system elements. Thus, the same software modules can be used throughout all hardware systems. They can also be added when a hardware addition expands system capability.

MODCOMP can supply two communications operating systems: MAXCOM for low-overhead running and MAXNET for distributed processing. MODCOMP also supplies three assemblers, two cross-assemblers, a FORTRAN IV compiler, two BASIC interpreters, and a variety of utilities.

Operating Systems

MAX I. A core-resident operating system designed for use on minimum configuration systems that include 4K words of memory and an ASR 33, MAX I provides operator communications, I/O handlers, debug features, and load/dump capabilities. It allows direct operator control for assemblies, program debugging operations, and program executions from the console teletypewriter or card reader.

MAX II. The MAX II system is batch oriented and is either core or disc resident. It assembles, compiles, and executes programs in a batch processing mode. The significant features of MAX II are:

- Operator intervention and communication facilities available at all times.
- Queued I/O operations performed concurrently with processing.
- A job control language that directs all system activities.
- An on-line compile-and-execute feature for performing media-to-media conversions and for editing and merging data.
- Program assembly using Assembler or Macro Assembler.
- Program compilation using the FORTRAN IV compiler.
- A variety of execution time services to facilitate implementation of user programs.
- Easy-to-use program debugging services.
- Program loading, including linking of external routines and COMMON blocks.

The recently announced improved I/O system integrates the process and logical I/O systems. New handlers have been incorporated into the operating system:

- The disc handler supports floppy discs and overlapped seek on multiunit controllers.
- The modified impact printer handler now supports serial matrix printers.
- The Teletype handler supports a variety of unbuffered printers and terminals.

The following symbiont tasks are available:

- IBM 2780 and CDC terminal emulators used for binary synchronous communications.
- Spooler for print devices.

The core-resident version of MAX II requires a CPU with executive features, multiply/divide hardware, and a minimum of 12K words of memory. If the FORTRAN IV compiler and the Macro Assembler are included, a minimum of 20K words of memory are required. This version also needs an ASR 33 and a binary I/O device combination, which can include a paper tape reader/punch, a card reader, or a magnetic tape unit. Besides the preceding, the disc version requires a DMP and a disc with a capacity of no less than 128K words, and the overlay version of the FORTRAN IV compiler. Executive features include real-time clock, and console, external, and task scheduler interrupts.

MAX III. A real-time multiprogramming system with foreground/middleground/background processing modes, MAX III is a task-oriented system that handles up to 256 active tasks: 128 foreground, 127 middleground, and one background. A variety of configurations are available because MAX III consists of software modules linked to form a real-time executive tailored to the hardware complement and operating environment. It is available as a core-resident version, a basic disc version, or an extended disc version.

The core-resident (foreground only) version of MAX III requires a processor with 12K words of memory, Executive features, multiply/divide, an ASR 33, and a binary I/O device. It provides these real-time features:

- Real-time clock for maintaining the time of day, timing task delays, and updating system watchdog timers.
- CPU execution control executive driven by the clock and external event interrupts to permit efficient execution of system-connected tasks on up to 128 unique foreground priority levels.
- Optional execution of more than one task at each priority level.
- Activation of tasks by hardware interrupt, operator request, request from another active task, elapsed time, or time of day.
- Reentrant executive services for system-connected tasks with critical response requirements.

- Queued I/O services, which can be performed concurrently with task execution or with the calling task suspended; error recovery is automatic or under control of the calling task.
- Ability to assign an I/O device exclusively to a privileged task or group of tasks.
- A modular, expandable communications package giving the operator complete control of all system resources.
- Good operator communications via the Operator Communication Task, which can be placed at any priority level, or can be deleted in a dedicated system.
- An off-line system generation program for configuring the resident elements and tasks of the system, thereby allowing generation of a large core-resident system in a small core configuration.
- Transient allocation of any core not used for the resident elements.
- Ability to declare library subroutines resident at system generation; reentrant subroutines, core tables, and variables can be made global for inter-task communication.

The basic MAX III disc version requires 12K words of core memory and a disc with a minimum capacity of 128K words, a CPU with Executive functions and hardware multiply/divide, DMP, ASR 33, and binary I/O device. It provides all of the services of the core-resident version plus the following additional ones:

- Loads, relocates, and executes nonresident tasks on demand.
- Performs dynamic allocation of peripherals, disc partitions, and core space to a task when it is activated or is being loaded automatically into core. Additional core blocks and peripherals can be requested during execution.
- Provides program overlays in a fixed core area. Any task can consist of a main body and many overlays.
- Permits off-line cataloging to establish all disc-resident elements. Cataloging can be directly to the disc or to a secondary device.

MAX III's extended disc version requires a MODCOMP computer system like the basic disc version's except with 24K words of core memory and a disc with a capacity of at least 256K words. It uses the system protect option to provide features beyond those of the basic disc version. In the extended disc version, core memory is partitioned into several areas to allow for execution of core-resident or disc-resident tasks that are protected (foreground) or unprotected (middleground). The lowest priority level can also be used for background batch processing operations. Undebugged tasks can be allocated to the unprotected core region so that illegal operations are aborted with no effect on foreground tasks or resident system services. The lowest (background) task priority can be used to execute a special JOB CONTROL task in a fixed core area, which can be either protected or unprotected by operator option.

When the background area is required by the foreground, the background operation can be checkpointed and its core region automatically appended to the foreground core. When no longer required, the memory area is released and the background program resumed automatically.

The "round-robin" method of task execution allows all tasks at the same priority level to share processor time on a cyclic basis. A new task loading nonresident startup routine, with the help of TAKE and GIVE functions, allows tasks to use an entire disc pack exclusively when loading foreground tasks. This routine allows nonresident tasks to be loaded faster from moving head discs.

Core partitioning allows up to 15 core partitions to be specified in addition to foreground and middleground core pools. A nonresident task can be assigned to a core partition instead of a core pool. This specific designation to a partition rather than a pool allows faster execution if no checkpointing is involved. Many tasks can execute in a partition simultaneously. Lower priority tasks can be checkpointed or rolled-out to allow a higher-priority task to execute. If the foreground core pool needs to be expanded, whole partitions can be checkpointed.

MAXCOM

MAXCOM is a special-purpose operating system designed especially to handle the communications environment at runtime. This operating system connects tasks to events and has been optimized for high throughput/low-overhead switching. MAXCOM efficiently handles line concentration, message switching preprocessing, and on-line inquiry for up to 256 terminals. Services like I/O control, timing, task activation, queue manipulation, debug facilities, device handlers, computer-to-computer protocol, and operator directives for controlling tasks and physical resources are based to a large extent on the related operating system.

MAXNET III

MAXNET III is a new operating system that adds network processing capability to the extended version of the MAX III Operating System. MAXNET III allows multiple MODCOMP computers to function in a distributed processing environment. The host system is a MODCOMP II with 32K words of memory, disc, console device (Teletype or CRT), and a communications link to each satellite MODCOMP computer. The link can be any of those listed in Table 2.

All computers in a network have all the software available to users of the extended disc ("F") version of MAX III, plus MAXNET functions and tasks. Network functions are interfaced to application programs via executive services, callable subroutines, or operator commands. Operator directives to the host and the satellites can perform

Table 2. Communications Links Among Computers Under MAXNET III

Model	Description
1115	Async comm interface, 110 to 9,600 baud, 20-ma current loop with 1 half-duplex channel
1116	Async comm interface, 110 to 9,600 baud, RS232C-compatible with 1 half-duplex channel
1911	Async comm channels, 110 baud, 60/20-ma current loop with 2 full-duplex lines
1912	Async comm channels, 75 to 9,600 baud, RS232C-compatible with 2 full-duplex lines
4810	Async comm interface, 75 to 9,600 baud, 20-ma current loop with 2 full-duplex channels
4811	Async comm interface, 75 to 9,600 baud, RS232C-compatible with 2 full-duplex channels
4815	Sync comm interface, 110 to 20K baud, RS232C-compatible with 2 full-duplex channels; supported with async line protocol
4820	MODCOMP 16-bit parallel computer link, 100K words per second
5813	Async comm interface, 75 to 9,600 baud, 1 full-duplex channel and remote fill hardware; RS232C or current loop
5820	High-speed serial computer link; 15K to 125K words per second, with 2 half-duplex channels and remote fill hardware

the following functions in a remote system: initial program load; create or change logical file assignment or a logical file default assignment; resume, hold, kill, or activate a task; establish or disestablish task; interrogate logical file; or read task status. The host computer can give background to allow the satellite to use a batch processing task and can retake background to regain use of the batch processing task. The satellite can use the host's background and peripherals for program development.

Users can call the following services in a remote system in ASSEMBLER language or FORTRAN: establish, resume, disestablish, activate, kill, and hold task; assign default; and inform task.

At system generation time, the following system tasks can be incorporated into MAXNET III:

- Link — allows device independent I/O transfers over multiple computer links; a symbiont interface to logical I/O system; interface looks like software I/O controller.
- Loader — allows tasks on a host disc to be loaded to a satellite computer.
- Simultaneous output — takes data from one device and outputs it on two devices simultaneously, such as consoles on a satellite and host.
- Linking loader — checks computer link for binary data during remote fill; does a checksum on record basis; and requests retries if error found.
- Software device interface — allows user to transfer data in and out of core partitions either locally or remotely; the partitions which are normally subdivisions of global common areas are defined at system generation.

MAX IV. Effectively a combination of the MAX II and MAX III operating systems (which are subsets of MAX IV), MAX IV uses the hardware features of the MODCOMP IV to fully utilize its capabilities. The 256-word optional MODCOMP IV general-purpose register context file is of central importance to the operating system.

The MAX IV system manages four optional MODCOMP IV hardware memory maps to solve hardware relocation and memory fragmentation problems. These maps are switchable addressing ranges, called virtual memory areas; each can be associated with 64K words of physical memory. Physical memory is organized in 256-word pages, expandable to 1,024-pages (256K words). The four maps allow duplication of memory pages for common global areas, and some pages are not associated with any map at all. The maps permit the addressing of any physical memory location in any 256-word page up to a program's 64K-word addressing limit.

One map is dedicated to the system to allow instant access to vital memory pages. Interrupt vectors, I/O handlers, executive service routines, task control blocks, and executive tasks fall into the system map. Additional pages, as they are needed, are mapped from the address pool of unused memory locations.

The other three memory maps are for user tasks, of which three with highest priority are assigned to these maps. Executive tasks do not affect user task context switching overhead because executive tasks utilize the system map for their execution. Memory maps do not have to be saved during an interrupt as a copy of each task's map image is maintained in core in the system map under its task control block. Memory maps need to be retransmitted during context switching operations only if the number of interrupting programs exceeds three levels.

Executive tasks operate in the system map, which limits the tasks in several ways. Size is a problem, as the entire system map, including tasks, has a 64K-word maximum. Some tasks are resident in the operating system, while others are disc resident and are loaded and activated from disc. The disc-resident tasks must have core allocations provided. Hardware relocation and user task isolation are unavailable to the executive tasks. The major advantage to offset these difficulties is that the executive tasks are more closely related to the operating system and its privileged instructions.

All user tasks are protected from all other user tasks but are unprivileged. The tasks view the system as a full 64K-word computer. Memory that is not used by the task is virtually nonexistent as far as that task is concerned. One or more tasks, however, can be doing independent batch processing. The Reentrant Executive Service (REX) is the only operating system task that is visible to the user task. REX performs I/O queuing, executive control, code conversion, and other utilities.

In addition, other reentrant or recursive executive services and subroutines can be user developed and incorporated in the executive. MAX IV assigns global or

intertask common memory areas to the user's maps for intertask and system communication. Protect keys are assigned to each map and are as shown in Table 3.

Object code can be stored on secondary storage in an absolute format. System load then becomes a disc read into core, while larger tasks are loaded in single blocks of 16K words. Job control can be customized to user needs to provide a MACRO-like language for the user.

Only the write access area of an interrupted task needs to be written on a disc checkpoint area. MAX IV arranges contiguous task map areas despite the actual physical scattering of the memory pages. When a task is bumped from memory it loses only the exact number of pages needed by the higher priority task. This allows partial task reloads rather than full task reallocation.

Although the user is generally limited to a 64K-word block, including all local, global, or common data areas, the MAX IV on MODCOMP IV can grant the use of two full memory maps (128K words). To achieve this, however, all instructions must be in one map with all the operands (local and global) in another. Larger programs with large data bases benefit from this option.

The interrupt system for the MODCOMP IV with the MAX IV operating system allows up to 256 unique software priority levels. Tasks executing at the same level operate on a cyclic time-shared basis.

The optional hardware context file of 16 copies of 15 general-purpose registers allows the dedication of a general register block to a subroutine. If only a few registers are needed by a subroutine, they can be dedicated to it and the rest of the register set shared with another interrupt level. Pointers and data values can then remain in registers from one program to the next.

The two control registers, the Program Register (PR) and Program Status Register (PS), are saved and restored in two sets of two dedicated memory locations. PS stores the condition codes, general register block, and memory maps available for the task. The new word moved into the PS register swaps the processor to the environment for the new task.

Dedicated register files are assigned to the most frequently used interrupt levels. These levels include the taskmaster, clock interrupt, data interrupt party line, and service interrupt party line. The pointers, addresses, and constants used by these subroutines are assigned dedicated registers. Other dedicated register blocks are assigned to and shared by the remaining interrupt levels. Entire or partial general register blocks can be dedicated to user-coded interrupt levels. User-coded interrupt routines can also be added to operate "above the system" to process critical programs requiring fast response times.

User and executive tasks operate at interrupt levels assigned to them by the taskmaster routine. The taskmaster operates at the lowest interrupt priority and

Table 3. MODCOMP II and IV: Protect Keys

Key	Access	Typical Use
0	No access	Nonpresent memory
1	Read only	Reference data and common
2	Read and branch only	Nonmodifiable program instructions; reentrant libraries
3	Read, branch, and write	Scratch data areas and common

can manipulate the background time into many task levels. Taskmaster always interrupts the currently executing task, and it returns control to the interrupted program or to a program of higher priority. As the taskmaster exists, it reassigns surplus general-purpose register files and memory maps to the executing task.

The MODCOMP IV with the MAX IV system can operate completely without saving or restoring general-purpose registers if the number of sets of general-purpose registers equals or exceeds the number of tasks.

Real-time features of MAX IV include periodic or 1-shot timers which can be addressed with elapsed-time or time-of-day arguments. A real-time clock provides delay timers, task scheduling timers, watchdog timers, and CPU counters for use by the various tasks.

MAX IV supports all standard MODCOMP II, III, and IV peripheral devices, including special process I/O devices and communications multiplexors. I/O operations can be performed either concurrently with task execution or with the calling task suspended until the I/O operation is complete. Any delayed I/O operations are queued to avoid program delays due to a busy controller. Device handlers have both device independent and dependent modes of use allowing a program to utilize the particular device characteristics when device independence is not required.

I/O devices are addressed indirectly by way of assignable files, which can be private or global. Each file has both normal and default procedures. Files can be assigned to other files or addressed by name or numerical index. A file can be bypassed completely when direct device I/O is required. I/O error recovery can be automatic with unrecoverable errors reported to the operator. Error recovery can also be under the complete control of the calling task. This method allows critical tasks to perform error recovery techniques, including device substitution.

Input spooling is available as an option to permit a single job entry device to schedule several parallel batch processing jobs concurrently. Output spooling, also optional, permits any number of imaginary devices to be defined, using any number of physical output devices. Optional spooling tasks and symbionts can be used to simulate special device characteristics or to buffer slow devices to and from disc files.

Language Processors

ASSEMBLER, EXTENDED ASSEMBLER, FORTRAN-Coded CROSS ASSEMBLER, MACRO ASSEMBLER, MODCOMP FORTRAN IV, Real-Time FORTRAN IV, BASIC, EXTENDED BASIC, and RPG II are the language processors Modular Computer Systems offers for use with MODCOMP II, III, and IV.

ASSEMBLER and EXTENDED ASSEMBLER. Designed to operate under the MAX systems, ASSEMBLER requires two passes, with the source input being copied to a scratch file if one is assigned. The input to the second pass is then the scratch file.

ASSEMBLER includes the following features:

- Absolute (ASSEMBLER) and relocatable (EXTENDED ASSEMBLER) object code.
- Free-field assembly format.
- An extensive directive set to aid in expressing constants, allocating storage, interprogram communication, and formatting listed output files.
- Ability to define new instructions implemented in the ROM controller.

In addition, ASSEMBLER accepts constants both as operands and as immediate instructions in data statements. Decimal integer, hexadecimal integer, character string, address constant, and compressed alphanumeric character string are all recognized constants.

The basic ASSEMBLER requires only 2K words of memory and an ASR 33 I/O device. It can utilize additional memory and the high-speed paper tape reader and punch.

EXTENDED ASSEMBLER operates in 4K or more words of memory and produces relocatable object output. It will operate with only an ASR 33 I/O device but can support a card reader, line printer, paper tape reader and punch, disc, and magnetic tape unit. A 4K system is able to handle up to 200 symbol names. With more core memory available, the symbol table can be extended at the rate of one symbol for every three words of memory.

The MACRO ASSEMBLER is a superset of the assemblers, which contains all of EXTENDED ASSEMBLER's capabilities plus the generation of nested macros, recursive MACRO calls, conditional ASSEMBLY statements, assembly time branches, macro exits, and other features. Additional constants recognized are fixed-point single precision, fixed-point double precision, floating-point single precision, and floating-point double precision.

MACRO ASSEMBLER is designed to operate under at least MAX II in a system having a minimum of 12K words of memory.

All assemblers are upward compatible in both syntax and object code.

The FORTRAN-Coded CROSS ASSEMBLER permits MODCOMP programs to be assembled on an IBM System/360 or 370 under DOS. It requires a hardware configuration that includes 65K bytes of memory, a card reader, a line printer, a card punch, and a disc file or magnetic tape unit. The object output can be executed by the MODCOMP I and up.

MODCOMP FORTRAN IV. The FORTRAN IV compiler meets ANSI specification ANS X2.9 1966, except the MODCOMP version uses only the first five characters as identifiers. In addition, it has a set of real-time extensions to make it a data acquisition and control language.

With MODCOMP FORTRAN IV, source programs incorporating in-line ASSEMBLY language coding, including MACRO directives, can be written. For maximum run-time efficiency, all of the MAX executive services can be called through in-line ASSEMBLY language coding.

A set of CALL subroutines is included and is compatible with process control industry recommendations. Array extensions provide the capability of using any arithmetic expression as an array subscript.

BASIC. A subset of the MACRO ASSEMBLER, BASIC generates relocatable as well as absolute object code. It operates under MAX II, MAX III, and MAX IV and is useful in performing mathematical computations. BASIC incudes a CALL statement, which permits the preparation and calling of a set of subroutines to perform special functions.

EXTENDED BASIC. A multiterminal system with real-time extensions, EXTENDED BASIC operates as a single task under the MAX III and MAX IV Executive.

Utilities

An advanced set of computer and peripheral diagnostics is available as a maintenance aid. Utility programs include absolute and relocatable loaders, source and object file editing, media-to-media conversion, and program debug capabilities. The available math library meets ANSI FORTRAN standards.

PRIME COMPUTER

Prime 100, 200, and 300 Series

74-451

OVERVIEW

The Prime series consists of three computers particularly oriented toward software and services designed for users' convenience. The main markets for the systems are currently data communications and industrial control. The largest system also competes in time-sharing and multiprogramming environments.

The Prime 200 is the "pivot" model in the line: it was first delivered in September 1972. The Prime 100 is essentially a slow 200 with a few features missing; it was first delivered in January 1973. The Prime 300 is much more powerful than the 200; it supports virtual memory and allows up to 50 million words of disc storage to be used as an extension of main memory. The 300 was first delivered in September 1973.

All three models are 16-bit microprogrammed minicomputers that feature all-MOS memory, instruction sets compatible with Honeywell Series-16 and extensive software. The 100 is a 4K- to 32K-word system (1.0 μsec memory cycle time), the 200 is a 4K- to 64K-word system (750-nanosecond memory cycle time), and the 300 is an 8K- to 256K-word system (600- or 750-nanosecond memory cycle time). The three systems are upward compatible and use the same system software and peripherals.

All three models can address up to 64 peripheral devices: magnetic tape and disc units, printers, paper tape and card equipment, communications devices and analog/digital equipment. The larger minicomputer manufacturers currently have a larger assortment of peripherals than Prime offers with its systems. However, Prime continues to add peripherals to its line, such as an IBM-compatible floppy disc and a 2314-compatible moving head disc.

The I/O structure for the line is flexible with five types of I/O channels available. Stack manipulation instructions and a 64-level priority interrupt system are standard features on all processors. The Prime 200 and 300 can also attach floating-point hardware; the 300 supports writable control store.

The Prime systems are particularly well suited to communications because of their DMC/DMT I/O facility. DMC is like a slower-speed DMA, with channel control words stored in memory instead of the DMA register file; there is no logical limit to the number of devices it can support. The DMT channel is faster than Prime's DMA channel because the current addresses for data transfers are supplied by device controller registers for DMT, rather than channel registers for DMA.

Communications functions are further supported by a line of synchronous and asynchronous single line and multiline controllers.

The software available is quite extensive: two full-fledged operating systems — DOS and RTOS, Macro Assembler, BASIC Interpreter and FORTRAN IV compiler can operate stand-alone. The Prime 300 uses virtual memory versions of the standard operating systems (DOS/VM and RTOS/VM).

There is no software especially geared to communications except the software drivers for the line controllers and the RTOS operating system.

The Prime processors are also marketed as processors for value-added networks and for satellite voice communications.

From its beginning, Prime has used all MOS memory for its computers, thus the company has had considerable experience with it. Prime developed the first 32K-word MOS memory board. It uses 4K chips from a variety of suppliers. The board is 16 by 18 inches. Table 1 lists the mainframe characteristics.

COMPETITIVE POSITION

The Prime series computers are marketed for industrial control and data communication applications. The line is not being marketed as liberators of H316s or DDP-516s, even though the Prime computers are program compatible with the Honeywell Series 16 computers.

In general, the Prime systems are cost and performance competitive with similar systems, and their hardware and software offerings are well-rounded. The focus on industrial control and data communications is a wise path for a small company to follow, for it can concentrate its resources and be truly competitive with larger companies.

The DMC/DMT I/O channels, together with the communications facilities and related software, make the

Table 1. Prime Computer Series: Mainframe Characteristics

	100	200	300
CENTRAL PROCESSOR			
Type (microprogrammed)	Yes	Yes	Yes
No. of Internal Registers	26	26	26
Addressing			
Direct	Yes	Yes	Yes
Indirect	Multilevel	Multilevel	Multilevel
Indexed	Yes	Yes	Yes
Instruction Set Implementation	Hardware	Hardware	Hardware
Number	112 std, 8 opt	117 std, 37 opt	145 std, 29 opt
Decimal Arithmetic	No	No	No
Floating-Point Arithmetic	Subroutine	Subroutine	Subroutine
User Microprogramming	No	No	Optional
Priority Interrupt Levels	64	64	64
MAIN STORAGE			
Type	MOS	MOS	MOS
Cycle Time (μsec)	1.0	0.75	0.60 or 0.75
Basic Addressable Unit	Wd (16 bits)	Wd (16 bits)	Wd (16 bits)
Bytes/Access	2; 4	2; 4	2; 4
Cache Memory	No	No	No
Min Capacity (wds)	4K	4K	8K
Max Capacity (wds)	32K	32K std, 64K opt	256K
Increment Size (wds)	4K; 8K	4K; 8K	8K; 32K
Ports/Module	1	1	1
Error Checks	None	Parity	Parity
Protection Method	None	None	Software
Memory Management	No	No	Yes
ROM			
Use	Bootstrap loader, control store	Bootstrap loader, control store	Bootstrap loader, control store
I/O CHANNELS			
Programmed I/O	Yes	Yes	Yes
Direct Memory I/O (no. of subchannels)			
DMA	8 (programmable)	8 (programmable)	8 (programmable)
DMT	No limit	No limit	No limit
DMC	4,096	4,096	4,096
Max Xfer Rate (wds/sec)			
Over DMA	694,444	925,925	1,157,406
Over DMC	225,225	271,739	339,674
Over DMT	694,444	1,084,956	1,250,000

systems particularly good for communications applications. The RTOS operating system allows foreground/background processing, combining real-time data acquisition and control in the background with program development in the foreground. The addition of the larger, faster Prime 300 system adds to the line's range of processing power in both markets, and strengthens its competitive position for multiprogramming and time-sharing applications through the standard memory mapping and virtual memory techniques.

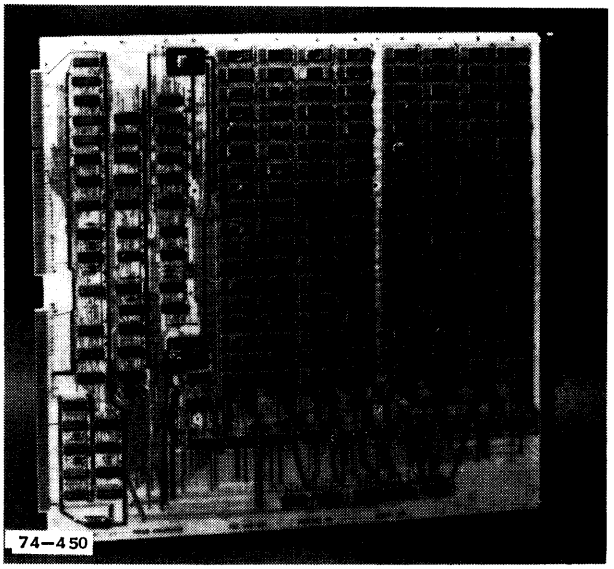
The Prime 100 competes with the DEC PDP-8, PDP-11/05, and 11/10; Data General Nova 1200, and ECLIPSE S/100; and Interdata Model 7/16. The Prime 200 competes with the DEC PDP-11/40, Data General Nova 800, ECLIPSE S/200, Interdata Models 70/80 and 7/16, and General Automation SPC-16. The Prime 300 competes in the upper range of minicomputers with such systems as DEC PDP-11/45, Interdata 7/32, Varian Data Machines V74, MODCOMP IV and Hewlett-Packard HP 21MX.

Some of the competitive systems with the 100 and 200 can expand memory beyond 64K words and can use memory management systems that make them more appropriate for multiprogramming and real-time applications. The Prime 100 and 200 computers do not have hardware memory protection, but the Prime 300 does. It also has a relatively sophisticated memory management option, allowing addressing of up to 256K words of real memory.

Although some manufacturers have had considerable difficulty with MOS memory reliability, Prime has developed a board testing technique to allow consistent production of reliable large memories.

USER REACTIONS

Users we contacted were unanimous in extolling Prime's service and support organization, and its general attitude of helpfulness when any problem arose. One user had some of its first new DAC boards and had some problems with the Digital Output module. This user expected some problems with a new item, however, and felt confident the company would soon set things right. Another user had a Prime 300 system for more than a



year, and the system had been down only twice: once for an hour, and once, when a part had to be flown in, for less than a day.

Users generally bought the Prime systems after considering the larger, well-established minicomputer manufacturers.

Appliance manufacturer. A large appliance manufacturer using a Prime 300 chose the system over those manufactured by Digital and Hewlett-Packard because the company had high performance demands and limited funds. This 32K-word virtual memory system supports engineering design and test functions in a time-shared mode. Various data acquisition instruments are attached to the system, as well as a number of Tektronix graphics terminals. This user is pleased with the result; interfacing to the system has been easy. This user felt the documentation for interfacing could be improved, however. When we spoke to him, he had placed an order for the hardware floating-point processor and was waiting for the RTOS-VM A/D and D/A software drivers to be completed, so they could run their data acquisition system under RTOS instead of DOS.

Newspaper Production. Another user bought Prime 200 systems to control a line of automated newspaper production systems. This user looked at Digital, Data General, and others before selecting the 200. The Prime system attracted them because this company already had used Honeywell 316s to run its phototypesetters, and some of the already developed software could be used on the Prime 200. This user feels Prime has particularly good documentation for its software, an important point because the documentation tended to be used over and over again, whereas hardware interfacing documentation problems were usually one-shot affairs.

Diversified Manufacturer. A very large diversified manufacturer selected the Prime 300 as the processing unit for a product line in telecommunications routing centers. The CPUs in the system will be used for switching, logging, and routing functions for TV, telephone, and data transmission via satellite. The manufacturer began developing the system using a Honeywell Series 16 processor, but became very dissatisfied with Honeywell's service. The company discovered the Prime product line and is delighted with the change; the Prime 300 is faster, costs less, and has more expansion capability than the Honeywell system. The Prime system software was one of its strong points. This user will undoubtedly become one of Prime Computer's larger accounts; each routing system will consist not only of multiple CPUs (two to four), but also discs, tape drives, and printers — in short, a whole system OEMed, not just the processor.

CONFIGURATION GUIDE

Minimum configurations include a processor with 4K or 8K words of MOS memory, programmed I/O, eight programmable DMA channels, power supply, 64-level vectored priority interrupt system, and console. Basic systems provide additional subassembly slots for memory expansion modules and I/O device interfaces. The basic models have five standard subassembly slots; 10 or 17 are optional. Each 4K-, 8K-, or 32K-word memory modules requires one slot, and the central processor requires one slot. Modules can be arranged in any order on the universal bus system.

Table 2 lists the peripherals available for the Prime computers.

Table 2. Prime Computer Series: Peripherals

Magnetic Disc. Moving Head: Capacities of 1.5M wds, 3.0M wds, 12.0M wds (access time 15 msec min, 70 msec avg, 110 msec max; 12.5 msec avg latency) and 25M wds (IBM 2314-type).
Fixed Head: 128K wds, 256K wds capacity.
Diskette: 138 wds. (IBM-compatible.)

Magnetic Tape. 7-track, 800 bpi, 45 ips; 9-track, 800 bpi, 45 ips.

Punched Card. 150 to 300 cpm reader, 400 cpm/100-285 cpm Reader/Punch.

Graphics Display. Alphanumeric Display with keyboard.

Printer. 165 cps Serial Printer; 300 lpm line printer; Both 132 col.

Paper Tape. Readers at 200 cps; reader/punch at 200/75 cps respectively. 8-channel fanfold tape.

Teletypes. TTY 33 ASR, KSR; TTY 35 ASR characteristics.

Analog/Digital. A/D Conversion, D/A Conversion subsystems; Digital Input and Digital Output Subsystems.

Communications. Async multiline controllers, sync multiline controller, multiple auto call interface.

Prime offers central processor in four submodels for the 100 Series, in 12 submodels for the 200, and in six submodels for the 300. Processor models vary in basic memory size, electrical environment, mounting chassis, and standard processor features, at prices slightly lower than adding them optionally to the processors.

The 200 Series processors have a few standard features that are available as options for the 100 Series; byte parity and an asynchronous serial communications interface are standard features, for instance. In most respects, the 100 is a slower 200, with essentially the same features on a smaller scale.

Memory can be incremented in modules of 4K, 8K, or 32K words. The I/O bus can handle a maximum of eight controllers for high-speed DMA devices like magnetic discs and tapes. All eight can operate simultaneously and time share the I/O bus. Devices with their own control registers can also use the ultra-high-speed DMT channel, which is optional on both the 100 and 200 and standard on the 300. Slower-speed devices like the serial printer, paper tape, card I/O devices, Teletypes, and the analog/digital and communications interfaces use programmed I/O or the DMC — optional on either the 100 or 200 and standard on the 300. The DMC can handle a maximum of 4,096 individual devices, although the system as a whole can directly address only 64 device controllers. The DMC channel requires four memory cycles for each word transferred.

A minimum 300 Series system is similar to a 200 Series minimum system with most options included as standard. For instance, all 200 Series models have the following options to expand processing power: extended addressing to 64K words of memory, hardware multiply/divide, double precision arithmetic, micro-verification routines, automatic program loading from paper tape, and DMC/DMT channels.

These items are standard on the 300 Series, except extended addressing is to 256K words of memory. The following major features provided for the 300 Series are unavailable for the 100/200 Series:

- Virtual memory addressing to 64K words.
- Physical MOS memory capacity to 256K words with virtual memory up to disc capacity.
- Two distinct processor modes — paging mode and restricted mode — can be designated separately or together to allow processing at user, supervisor, or base operating level.
- Memory cycle time of 600 nanoseconds per word.
- Optional floating-point processor that executes 19 floating-point instructions.
- Writable control store.

Three special interfaces are provided: one allows a user's own device to connect to a system, a second allows controllers from the Honeywell Series 16 computers to interface to a system, and the third allows a second Prime processor to be linked to a system.

COMPATIBILITY

Prime 100 and 200 Series computers are completely program-compatible; given the appropriate configuration, programs compiled on one computer can run on the other. The 100 Series uses a subset of the 200 Series instruction set. Both processors have an "unimplemented instruction" trap that allows a jump to a subroutine to perform the missing instruction. Honeywell Series 16 programs can be run on either the 100 or 200. Both Prime computers use the same software and peripherals, but they use different memory modules. The 100 Series modules do not include memory parity; the modules used with the 200 Series include two parity bits per word, one per byte.

Both the Prime 100 and 200 are upward compatible with the Prime 300. The use of the unimplemented instruction trap on the smaller computers means that programs compiled on the 300 can run on the 100 and 200 as well. The 300 also has the trap, but since all 100 and 200 instructions are standard on the 300, there is no immediate use for it. Table 3 lists the software packages available for the Prime computers.

MAINTENANCE AND SUPPORT

Prime markets its systems through its own sales and service facilities, and also through representatives. There are 11 sales offices in the United States, and four service centers (Massachusetts, Pennsylvania, Michigan, and California), as well as offices in England, Germany, Sweden, Denmark, Norway, Finland, Belgium, Switzerland, Austria, Netherlands, and Australia. All systems are sold, with monthly maintenance contracts available. These provide for both preventive maintenance and emergency service. Software is warranted for one year, with revisions and corrections made free of charge during that period.

Table 3. Prime Computer Series: Software

Package Software	Configuration Required	Comments
OPERATING SYSTEMS		
DOS	8K memory; Teletype ASR and interface; real-time clock; disc	Basic batch operating system for PRIME computers; written in Fortran; multiple directories, volume control, and access methods. Can run as background task under RTOS-VM.
RTOS	8K memory; Teletype ASR and interface; real-time clock	Compact, real-time multiprogramming system; can be disc- or memory-resident.
RTOS-VM	32K memory; Teletype ASR and interface; real-time clock; disc	Like RTOS but with paging algorithm, swapping, protection.

Table 3. (Contd.)

Package Software	Configuration Required	Comments
DOS-VM	Same as RTOS-VM	Up to 15 users can time-share with each user up to 64K words of memory.
ASSEMBLERS/ COMPILERS		
FORTRAN IV	12K memory; Teletype ASR and interface	One-pass compiler, extended instruction set, support library.
Macro Assembler	Minimum configuration	Pseudo Ops, symbol and data definition, program linking, storage allocation, user-defined macros.
Micro Assembler	32K memory; DOS or DOS-VM	For symbolic assembly of micro-code on model 300 with WCS.
BASIC UTILITIES	12K memory, Teletype	Extended; batch, conversational and immediate modes.
Desectorizing Link Loader	Minimum configuration	Loads, links, binds relocatable, or absolute program modules.
I/O Control Subsystem	Minimum configuration	Control routines and device drives; includes source file editing and merging.
Editors	Minimum configuration	Full-context editor for editing lines, characters, and multiple changes of same text in program.

TYPICAL PRICES

Model Number	Description	Purchase $
	Prime 100 Central Processors	
P1004A-05	Prime 100 Central Processor unit (with 4K wds of MOS memory; 1 μsec; 8-chan programmable DMA; full addressing modes; virtual instruction package; 4-chan, bit serial full-duplex interface; 5-board chassis; multi-level vectored priority interrupt system)	4,600
P1004A-10	Prime 100 in 10-board chassis	5,600
P1004A-17	Prime 100 in 17-board chassis	7,600
	Prime 200 Central Processors	
P2004B-05	Prime 200 Central Processor Unit (with 4K wds of MOS memory, 750 nsecs, byte parity; full addressing modes; 8-chan programmable DMA; multi-level vectored priority interrupt system; virtual instruction package; power supply; 10-board chassis; interface)	5,600
P2004B-10	Prime 200 in 10-board chassis	6,500
P2004B-17	Prime 200 in 17-board chassis	8,400
	Prime 300 Central Processors	
P3008B-05	Prime 300 Central Processor Unit (with 8K wds of MOS memory; 750 nsec; virtual memory; stack procedure instructions; microverification routines; hardware multiply/divide; double-precision arithmetic; DMC/DMT Capability; automatic program load; byte parity; full addressing modes; virtual instruction package; 8-chan programmable DMA; bit serial full duplex interface; Multi-level vectored priority interrupt system; 5-board chassis)	11,700
P3008B-10	Prime 300 in 10-board chassis	12,500
P3008C-10	P3008B-05 with 600-nsec memory in 10-board chassis	13,000
	Prime 100 Options	
157	Hardware multiply/divide, double-precision arithmetic and DMC/DMT capability	1,000
	Prime 200 Options	
253	Microverification routines	800
257	Hardware multiply/divide, double-precision arithmetic, DMC/DMT capability, and microverification routines	1,000
	Prime 300 Options	
361	Writeable control store (256 wds, 64 bits per microinstruction)	3,500
362	Double-and single-precision floating-point arithmetic, and writeable control store	5,000
369	Microprogramming training course, 1 man, 1 wk	1,000
	Prime 100 and 200 Options	
150/250	Hardware multiply/divide and double-precision arithmetic	800
151/251	DMC/DMT capability	500
142/242	Automatic program load from Teletype and paper tape reader	400
145/245	Automatic program load from multi-devices; includes Teletype, paper tape reader, disc, magnetic tape	600
	Prime 200 and 300 Options	
9501	Field Exerciser Panel (FEP); display unit, control unit and cable	600
260/360	Double-and single-precision floating-point arithmetic (14-digit accuracy)	2,000
	Prime 100, 200, & 300 Options	
146/246/346	Custom automatic program loader (256x16-bit wds)	600
147/247/347	One-time documentation charge for custom APL	1,200
140/240/340	Power monitor, power failure interrupt and automatic restart protection including battery backup for standby power for MOS memory	600
141/241/341	Additional battery	200
	MASS STORAGE	
	Discs and Diskettes	
4000	Disc controller for any combination of two fixed-head and for moving head discs	3,500
4103/5	128K/256K word fixed-head disc	9,500/ 11,000
4121	1.5M word moving-head disc	7,500
4123	3.0M word moving-head disc	9,500
4127	6.0M word moving-head disc	11,500
4300	Diskette controller and 2 drives	5,200
4166/67	Diskette cartridge, IBM/Prime format (73/77 data tracks)	25
	Prime 100 Memory Expansion	
UM008A-016A	8K board, 1-μsec cycle time; no parity	3,800

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $
UM016A-032A through UM048A-064A	16K board, 1-μsec cycle time; no parity (16K to 32K to 48K to 64K words)	6,800
UM032B-064B	32K board, 750-nsec cycle time; parity	11,000
UM008B-016B	8K board, 750-nsec cycle time; parity	3,900
	INPUT/OUTPUT	
3006/7	Real-time clock (line or external frequency), async line controller	1,800
3022	Sync line control capability	200
3023	Watchdog Timer (100 msec, RTC/PRTC, or external interval)	300
3025	Second 16-bit buffered parallel I/O controller (hdx)	500
3101	Teletype ASR 33	1,500
3103	Teletype KSR 33	1,200
3105	Teletype ASR 35	4,800
3121	Paper tape reader; 200 cps, for fan-fold 8-chan paper tape	1,900
3123	Paper tape reader/punch (reads 200 cps, punches 75 cps, for fan-fold 8-chan paper tape)	3,800
3141	Controller and card reader (300 cpm, binary and Hollerith formats)	5,000
3181	Controller and card reader/punch (400 cpm reader/100-285 cpm punch)	25,000
3161	Controller and line printer (300 lpm, 132 col, 64 char)	12,000
3191	Controller and card reader and line printer	17,000
3195	Controller and card reader/punch and line printer	34,500
3127	Character printer: 165 cps, EIA RS232-C compatible	6,000
4020	Controller for up to 4 magnetic tape transports	3,500
4141/3	Magnetic tape transport: 7/9 track, 45 ips, 556/800 bpi, industry compatible	7,000
3129	Alphanumeric CRT with keyboard, EIA RS232-C compatible	3,100
7000	General-Purpose Interface Board	1,200
7010	General-Purpose Interface Board	1,500
7030	Interprocessor Controller	3,500
	Async Multi-Line Controllers (AMLC; RS232-C/CCITT V24 compatible)	
5002/4	AMLC (for 103/202 data sets; 8/16 lines)	4,000/5,000
5052/4	AMLC (for direct connected devices; 8/16 lines)	2,600/3,000
5201/2/3/4	Multiple Sync Line Controller (RS232C compatible; for 201/203 data sets; 1/2/3/4 lines; + $200/line)	2,400
5244	Byte packing and char recognition (SYN, DLE, EOM, special)	400
5245	Byte packing, char recognition, transparent mode, and CRC12, CRC16, CRCCCITT, LRC	800
5246	Hardware bisync procedures for USASCII, EBCDIC, and SBTC codes	800
5402	MACI for 801 autocall units (4 lines)	2,000

HEADQUARTERS

Prime Computer
145 Pennsylvania Avenue
Framingham MA 01701
(617) 879-2960

(Please refer to report S770.011.100/180.5525.100 for general coverage of the Prime 100, 200, and 300 Series including OVERVIEW, COMPETITIVE POSITION, USERS' REACTIONS and CONFIGURATION GUIDE.)

MAINFRAME

Central Processor

The Prime processors are microprogrammed machines with the whole system of program counter, registers, and the like duplicated at a micro level and controlled by a stored program in read-only control memory. Writable control store can be added to the 300 Series, but this option is not yet software-supported.

The CPU is the control unit for the entire system. It connects to memory via a memory bus and to peripheral equipment via an I/O bus. The entire CPU, including the instruction logic, parity checking, eight DMA channels and asynchronous serial interface, is on a single board that can plug into any slot in the chassis. Priority relationships to I/O controllers are determined by their nearness to the CPU board.

Because of the demands of multiprogramming, the 300 Series processor is more complex than the 100 or 200 Series processor. It operates in combinations of four states or modes: paging, nonpaging, restricted, or unrestricted. These modes allow three program levels to be defined: base, user, and supervisor levels.

The base level program is the resident executive, which operates in the nonpaging and unrestricted modes. The supervisor level program is the nonresident executive, which operates in the paging and unrestricted modes. User level programs operate in the paging and restricted modes.

The resident executive handles interrupts from I/O devices, real-time clock, page-fault, restricted execution fault, and disc transfers, and it handles bookkeeping chores for the operating state and high-speed memory allocation. The nonresident monitor is an extension of the executive, inherently slower than the resident monitor because it can be disc resident. It can be used for the following file management and internal operating commands:

- Attach a user file space to a terminal.
- Read batch commands from a selected file and execute them.
- Load a memory image file.
- Save memory on a user file.

The user level is for application programs.

Data Structure. The basic data unit is the 16-bit word. Parity checking is unavailable for the 100 Series. Two parity bits, one for each byte, are provided for each word on the 200 and 300 Series, and parity is checked with each memory or I/O transfer.

Instructions and operands can be one or two words long. The same add, subtract, load, or store instructions handle single- or double-length operands depending on whether the processor is operating in single- or double-precision mode. Separate mnemonics are provided for the programmer's convenience. Negative numbers are represented in two's complement form. Multiplication produces a 2-word product. Division uses a 2-word dividend, a single word divisor, quotient, and remainder. An instruction is supplied to allow a single word product or dividend if the user desires. Floating-point single-precision and double-precision operands use 2- and 3-word formats (1-bit sign, 8-bit exponent, and 23- or 39-bit fraction) respectively.

The 15 memory reference instructions are one word long and handle 1-word operands. The double precision option on the Prime 200 (standard on the 300) uses 2-word operands. In systems with memories of 32K or more words, some memory addressing instructions are two words long with the second word a 15- or 16-bit address that can reference all of memory directly. The Prime 300 operating in paging mode divides the 16-bit address into a 7-bit virtual page address and a 9-bit word address within the page. Table 1 summarizes the data formats.

Table 1. Prime 100/200/300: Data Formats

Data Name	100	200/300
Character/Byte/ Halfword (bits)	8	8 + 1 parity
Word (bits)	16	16 + 2 parity
Doubleword (bits)	32	32 + 4 parity
Instructions (wds)	1 or 2	1 or 2
Decimal Operands	No	No
Binary Operands (wds)	1 or 2	1 or 2
Floating-Point Operands	2 or 3 wds (8-bit exponent, 1 sign bit, and 23- or 39-bit fraction)	2 or 3 wds (8-bit exponent, 1 sign bit, and 23- or 39-bit fraction)

For addressing purposes, memory is effectively divided into sectors of 512 words. All memory referencing instructions in all modes use the I, X, and S addressing bits that can be individually set or reset. The I and X bits are always interpreted in the same way; S varies somewhat depending upon the addressing mode.

- I — indirect addressing.
- X — index by the contents of register X or S as specified by the addressing mode.
- S — sector or relative addressing.

Special Registers

In addition to the program counter (P), the Prime computers use two accumulators (A, B), an index register (X), and a stack register (S) as the standard working registers. A single-bit overflow register (C) saves the last bit dropped out of A or B in shift operations, and one

register holds the normalized shift count. Two registers, Y and M, hold the address for a memory access, and the data read into or out of memory. Registers X, A, B, S, P, and normalized shift count can be addressed as memory locations, although they are physically located in a 32-word high-speed register file.

Eight pairs of registers, also addressable as memory locations, are associated with the eight DMA channels. These registers are also located in the high-speed register file. They hold the address and word count for DMA transfers. Four registers are reserved for the microprogram; six are also reserved for use by the Prime 300 to complete the total of 32 high-speed registers.

Only 26 of the 32 addressable registers are implemented on the Prime 100 and 200. The Prime 300 implements five more to handle the virtual memory addressing. The Page Map Address Register (PMAR) is used to access a program's memory map. Four Content Associative Memory (CAM) registers are used to expedite throughput by holding the last four map entries accessed.

The processor also uses a status word (that is not strictly speaking a register, but a collection of flags or keys) to reflect processor status. The program can read the status word and can input "keys" to change the processor's status.

Instruction Set. The basic instruction set for the Prime 200 consists of 114 instructions. These include the 72 standard and 14 optional instructions that correspond to the Honeywell Series 16 instruction set, plus 28 instructions found only on the Prime computers. The Prime 100 computer lacks hardware multiply/divide, parity checking, the integral serial interface, and double-precision arithmetic and the 18 instructions that refer to these features are not implemented. The Prime 100, however, has an "unimplemented instruction" trap (like the 200) to allow programs compiled on the 200 to run on the 100; unimplemented instructions are handled by subroutines.

Prime has added instructions to aid in compiler implementation: six logicize instructions convert arithmetic comparisons into logical variables, an instruction calculates an effective address and puts it in the accumulator, and a 3-way branch simulates the arithmetic IF statement.

The instruction set for the Prime 300 includes 145 standard and 24 optional instructions. These include all of the Prime 200 set plus five instructions to implement virtual memory, a group of stack-procedure instructions, and a group of conditional branch instructions that combine conditional testing and branching. The high-speed Floating-Point Arithmetic (FPA) feature adds the 19 optional instructions to the repertoire.

It adds high-speed floating-point load, store, add, subtract, multiply, divide, compare, skip, fix, float, complement, and round up instructions. Floating-point operands use two words: 8-bit exponent and 24-bit signed fraction. The FPA instruction set is optimized for FORTRAN IV Real Arithmetic operations. The Macro Assembler and FORTRAN IV compiler support FPA. Without the FPA feature, a software package will support the FPA instructions.

Virtual memory adds the following five instructions:

- Supervisor Call — generates an interrupt — operates in any mode, but is primarily used by user programs to get the attention of the executive.
- Enter Paging Mode and Jump — transfers control to a supervisor or user program.
- Leave Paging Mode and Jump — transfers control to a base-level program from supervisor mode.
- Enter Restricted Execution Mode and Jump — enters restricted mode and enables interrupts.
- Enter Virtual Mode and Jump — combines the functions of Enter Paging Mode and Jump and Enter Restricted Execution Mode and Jump.

Execution Times. Table 2 lists typical instruction execution times.

Addressing Facilities

Addressing is controlled by the processor status register and the memory referencing instruction.

The basic addressing modes that can be specified in the status register are as follows: 16K sectored, 32K sectored, 32K relative, and 64K relative. The normal addressing mode is 16K sectored, and the processor clears to this mode. The other addressing modes are selected by executing an instruction to change the contents of the status register. Once an addressing mode is selected, all subsequent memory referencing instructions calculate effective addresses with respect to the mode. The mode determines not only the type of addressing but also determines the length of the address and the index register.

256K-Word and Virtual Memory Addressing on the Prime 300. The Prime 300 uses a relatively simple memory management system for addressing real memory up to 256K words and virtual memory up to 50 million words. Programs can execute in the paging or nonpaging mode and in the restricted or unrestricted mode.

Programs operating in the paging mode are assigned a 256-word memory map, containing 128 entries. The first word of each map entry designates the address of a 512-word page in physical memory and indicates whether or not the page is resident in main memory or on the disc and whether or not the page is write protected. The second word usually contains the disc address of disc-resident pages.

When a program operating in the paging mode addresses memory, the 16-bit address is divided into a 7-bit virtual page address and a 9-bit word address within

Table 2. Prime 100/200/300: Typical Instruction Execution Times

Instruction	Execution Time (μsec) Prime 100	Prime 200	Prime 300
Fixed-Point			
Add, Subtract	1.76 - 2.44	1.36	1.88/1.56
Double Add, Subtract	4.56	3.56	3.28/2.80
Multiply	11.26	10.48	9.04/8.72
Divide	13.78	13.24	11.20/10.95
Floating-Point			
Add, Subtract	NA	9.35	8.75/8.10
Multiply	NA	27.82	25.20/24.56
Divide	NA	39.46	37.92/37.28
Normalize	3.42 + 1.08N	2.96 + 0.68N	2.68 + 0.6N/2.24 + 0.6N
Logicize, AND, OR	2.12 - 2.48	1.64 - 1.84	1.56 - 1.76/1.4 - 1.6
Complement	1.76	1.36	1.28/1.12
Change Bits or Signs	1.76	1.36	1.28/1.12
Interchange Bytes	1.76	1.36	1.28/1.12
Load	2.44	1.88	1.88/1.56
Double Load	3.72	2.96	2.72/2.24
Store	2.32	1.96	1.76/1.52
Double Store	3.72	3.04	2.64/2.32
Floating Load/Double Load	NA	4.6	4.36/3.72
Interchange A & Memory	3.72	2.88	2.72/2.32
Jump	1.76	1.28	1.28/1.12
Conditional Jump			
Interchange Register Contents	2.84	1.88	1.84/1.68
Compare 2 Numbers, Skip	2.12-4.24	1.52-3.20	1.48/1.32
Compute Effective Address	2.84	2.04	2.04
I/O	2.84	1.88	2.04/1.88

*Prime 300 times are given for 2 different memories: first number is for 750-nanosecond memory; second number is for 600-nanosecond memory.

NA – Not available.

the page. The virtual page address is doubled and indexed by a PMAR (Page Map Address Register) and used to access the appropriate entry in the program's memory map. The executive sets PMAR to the base address of the program's memory map before entering a program. If the page is in memory, the physical page address from the memory map is combined with the word address (from the address generated by the instruction) and used as an 18-bit physical memory address. If the page is not in memory, a page fault interrupt is generated, and the processor leaves the paging mode so that the executive can load the missing page. If the instruction is a write instruction and the page is write protected, a write protection interrupt is generated.

This procedure requires one memory cycle for translating a virtual memory address to a real memory address. To reduce overhead, four Content Associative Memory (CAM) registers are used to hold the last four map entries referenced. The virtual memory feature examines the contents of the CAM registers before using the memory map. If the required page entry is already in CAM, the translation from virtual to actual address requires only 80 nanoseconds. If the page entry is not in CAM, it is loaded into the CAM register holding the entry that was referenced the longest time ago. Prime studies indicate that only 3 to 4 per cent of the map references are not found in CAM.

Reserved Memory. The first 32 memory locations are inaccessible to the programmer as memory locations because their addresses are reserved to address the high-speed register file that implements internal registers.

Interrupt Control. There are two interrupt modes on the Prime computers, the standard and the vectored modes. In the standard mode, any device has priority to interrupt any program (even an interrupt servicing routine) unless the interrupt system is inhibited. In the vectored mode, the processor accepts interrupts only from devices with higher priority than the one currently being serviced.

In standard mode, all interrupts are multiplexed through memory location octal 63. In vectored mode, each device specifies a unique address, which is usually octal 100 greater than its own device address. Memory locations octal 100-177 are reserved for this purpose. The unique address can also be program-specified if the device has an address register for this purpose.

The two modes also differ in the way device priority is determined. The standard mode establishes a basic priority by the order in which the service routine tests devices and by setting or resetting Interrupt Enable flags on other devices in the system while a particular device is being serviced. The vectored mode, on the other hand, has a built-in priority structure by virtue of the bus positions to which devices are interfaced. Devices closest to the processor on the I/O bus have highest priority for both the DMA and interrupt line.

Internal interrupts or traps are also furnished for power failure, supervisor call, unimplemented instruction, memory parity error, machine check recovery, missing memory module, and illegal instruction. All internal interrupts have a higher priority than external interrupts. Each internal interrupt selects a unique memory location to pick up the pointer to the service routine.

Processor Console. All processors have a control panel which has indicators to display internal conditions and switches to control the system and to enter data into the internal registers. Control switches allow the operator to request a display, enter contents of data switches, start and stop a program, and single-step through a program.

MAIN MEMORY

The Prime 100, 200, and 300 computers use MOS semiconductor memory exclusively. Memory can range in size from 4K to 32K words on the 100, 4K to 64K words on the 200, and 8K to 256K words on the 300. Memory is composed of 4K-word, 8K-word, and 32K-word modules. Prime was the first minicomputer manufacturer to supply a 32K-word memory board.

Cycle times are 1.0, 0.75, and 0.60 microsecond for the 100, 200, and 300, respectively. Memory is refreshed by a sequence of staggered cycles; each cycle refreshes 1/32nd of the entire memory. Because the microprogrammed processor logic continues during the cycle, the amount of time taken from the program to refresh memory is negligible.

Octal Locations 0-37 and 100-177 in sector 0 are reserved memory locations. Addresses of the first set of locations are used to address the high-speed register file. The second set of locations is used for a variety of purposes such as storing standard and internal interrupt pointers, a real-time-clock counter, and the vectored interrupt system's pointers. Neither of the two smaller models has memory protection but the Prime 300 implements memory protection in three ways. The mapping technique itself prevents pages outside the program's own map from being accessed. The map further specifies which pages can be altered and which pages cannot be altered within the user program. Finally, the restricted execution mode prevents programs operating in this mode from executing instructions that alter the processor's control state.

Memory is divided into 512-word "pages" or sectors. The 16-bit address field normally allows up to 65,536 words (128 pages) to be addressed, but the mapping logic for virtual memory addressing generates 18-bit addresses which can address up to 262,144 words of "real" high-speed memory and 50 million words of "virtual" memory on random-access disc storage.

Input/Output Control

There are five possible ways to perform I/O operations over the single I/O bus:

- Programmed I/O standard feature.
- DMA (eight channels standard).
- DMC (option).
- DMT (option).
- Serial Interface (standard feature).

All modes use the same set of data, address, and mode control lines. Programmed I/O, used for slower-speed devices, requires the execution of I/O instructions to complete the transfer of one data word. DMA allows greater transfer rates by transferring blocks of up to 4,096 words: DMA uses locations in the high-speed register file within the CPU to store the word count and current address.

DMC transfers are like DMA transfers, but the channel control words are stored in main memory rather than the high-speed register file. Therefore, the maximum data transfer rate is slower for DMC than DMA.

In the DMT mode, which is the fastest of the modes, the current address for the data transfer is supplied by registers in the device controller rather than in a channel, thus the controller can access memory directly.

The processor serial interface provides a 4-bit input register and a 4-bit output register. An individual bit in each register can interface to an independent line. Therefore, four serial lines can input data simultaneously to the processor, and the processor can output serial data simultaneously to four lines. The instructions that load and store these registers operate on all four bits. The program must then perform the housekeeping required to change an output bit or to sample an input bit. The interface operates at EIA standard levels, and it can be used for any application requiring the reception or transmission of serial data. If the interface is used to control data communication lines directly, the program must determine character length and transmission frequency.

I/O instructions are one word long and allow up to four class codes, specification of 16 functions, and addressing for 64 devices.

The four types of instructions are for sending control pulses out to a device, testing device conditions for a skip, inputting data or information from a device, and outputting data or information to a device. Function codes vary in meaning depending upon the device they refer to.

PERIPHERALS

Teletypes, paper tape readers and punches, a card reader, serial printer magnetic tapes and discs are the standard peripherals offered with the Prime computers. A selection of special analog/digital equipment is also offered. Most peripherals are available for 60 Hz, 117 Vac and 50 Hz, 230 Vac power sources.

TELETYPES

3101 — TTY 33 ASR — requires 3001 or 3003 interface.

3103 — TTY 33 KSR — requires 3001 or 3003 interface.

3105 — TTY 35 ASR — requires 3001 or 3003 interface.

PAPER TAPE

3121 Paper Tape Reader — 200 cps; fanfold 8-channel tape; Remex 3075; requires 3002 or 3003 interface.

3123 Paper Tape Reader/Punch — 200/75 cps respectively; fanfold 8-channel tape; Remex 3075; requires 3002 or 3003 interface.

PUNCHED CARDS

3125 Punched Card Reader — 150 cpm; documentation; has EIA RS232C interface and controller; occupies 1 subassembly slot.

CRT

3129 Alphanumeric Display — with keyboard — includes EIA RS232C interface; requires 3001, 3003, or AMLC.

PRINTERS

3127 Serial Printer — 165 cps; Centronics matrix printer; has EIA RS232C interface and controller; occupies 1 subassembly slot.

3161 Line Printer — 300 lpm, 132 pp; includes controller.

MAGNETIC TAPE

4141 Magnetic Tape Transport — 7-track; 800 bpi; 45 ips; Pertec unit; requires 4020 controller .

4133 Magnetic Tape Transport — 9-track; 800 bpi; 45 ips; Pertec unit; requires 4020 controller.

MASS STORAGE DEVICES

4103 Fixed-Head Disc — 128K wds capacity; requires 4000 controller; 2 drives /controller.

4105 Fixed-Head Disc — 256K wds capacity; requires 4000 controller; 2 drives/controller.

4121 Moving-Head Disc — 1 removable cartridge; capacity 1.5M words; access time 15 - 110 msec; 12.5 msec avg latency; 3,680 wds/track; 460 wds/sector, 203 tracks/surface, 2 surfaces/disc; peak transfer rate 6.4 μ sec/wd; requires 4000 controller; 4 drives/controller; uses 4123 (2315-type) cartridge.

4123 Moving-Head Disc — 1 fixed and 1 removable cartridge; capacity 3.0M wds; same specifications as 4121.

4125 Moving-Head Disc — 1 fixed and 1 removable cartridge; capacity 12.0M wds; same as 4123 except double density in both wds/trk and trks/surface; same as 4121/4122.

4131/4131-A Moving-Head Disc — capacity 25M wds; IBM 2314-compatible.

4300 Diskette — capacity 138M wds; includes controller and 2 drives. Uses 4166, 4167 cartridge.

ANALOG/DIGITAL

6000 Analog-to-Digital Conversion Subsystem — converts 11 bits + sign; 50,000 samples/sec; prog selectable input ranges — ± 1.25, ± 2.5, ± 5, and ± 10; includes I/O interface for prog I/O, DMA; MUX 16-64 channels.

6060 Digital-to-Analog Conversion Subsystem — two 10-bit converters; output of ± 10 @ 10 ma; expandable to 4 channels.

DIGITAL CONTROL

6020 Digital Input Subsystem — 64 differential inputs; contact sense; contact interrupt; two 16-bit counters; requires 5V input @ 10 ma; industrial conditioning offered.

6040 Digital Output Subsystem — 64 buffered outputs; 1 counter.

DATA COMMUNICATIONS

A substantial number of synchronous and asynchronous interfaces and subsystems can be directly attached to Prime computers. All models can also attach a wide variety of communications devices via the DMC option, which allows direct data transfers between memory and up to 4,096 devices.

5052/5054 Asynchronous Multiline Controller — 8/16 lines for direct-connected devices RS232C/CCITT V24; requires DMC/DMT option; 8.6/11.0 amps at 5 Vdc.

5075 Asynchronous Multiline Controller — 16 lines for direct-connected devices; 8 lines at 20 ma and 8 lines at RS232C/CCITT V24; requires DMC/DMT option; 9.1 amps at 5 Vdc.

5002/5004 Asynchronous Multiline Controller — 8 or 16 lines for 103/202 data sets; RS232C/CCITT V24 compatible; requires DMC/DMT option; 8.6/11.0 amps at 5 Vdc.

520/2/3/4 Synchronous Multiline Controller — 1, 2, 3, or 4 lines for 201/203 data sets; RS232C compatible; options include byte packing character.

5402 Multiple Auto Call Interface — four lines for 801 auto call units; recognition, transparent mode CRC 12/16, CRC CCITT, LRC, and hardware bisync provides for USASCII, EBCDIC, and SBTC codes.

SOFTWARE

The main software packages available for the Prime computers are two operating systems, BASIC interpreter, FORTRAN IV compiler, and Macro assembler. An I/O Control Subsystem, Desectorizing Link Loader, two Text Editors, and Debugging package are included with the operating systems.

Prime has developed virtual memory (VM) versions of their DOS and RTOS operating systems by adding a paging algorithm.

DOS and DOS-VM Operating Systems. DOS is a general-purpose console-oriented operating system. It consists of three basic modules: disc management routines, interactive command language, and supporting utilities, such as loaders, device handlers, and editors. It functions as a batch operating system, providing automatic job and data stream routing.

Disc files have forward and backward pointers to prevent snowballing of lost files. The system file management features include multiple directories, multiple volume control, and multiple file access methods. Files are addressed by name rather than by absolute location.

DOS-VM enables 15 users to time share a system; each user can access a memory segment of up to 64K words. As little as 32K words of real memory are required for this system. Additional memory is not necessary to expand the number of users or tasks handled by the system. Additional memory can, however, make the system response time faster.

DOS-VM provides the same type of disc file management facilities as DOS. Both operating systems are written in FORTRAN IV.

RTOS and RTOS-VM Operating Systems. RTOS is a compact operating system designed to coordinate processes in a multiprogramming environment. It requires 8K words of memory. It provides multiprogram scheduling, simultaneous I/O, interrupt handling, and general supervisory functions. It can operate in either disc-based or memory-based configurations and has all the utilities available with DOS. DOS and RTOS use the same file structures and I/O drivers. RTOS can also support FORTRAN IV on configurations with 16K words of memory. DOS can operate as a background batch processing program in a foreground/background RTOS system without raising the minimum memory requirement. Conversely, real-time programs can be developed under DOS.

RTOS-VM allows foreground tasks to reside in memory or be swapped in from disc. RTOS-VM also protects tasks against unwanted alterations by other tasks. DOS can run in the RTOS-VM background as it does in RTOS proper.

Assembler. The Macro Assembler produces relocatable or absolute object code. Pseudo Ops provide for assembly control, listing, loading, data and variable definition, storage allocation, program linking, conditional assembly, and macro definition. Constants can be defined as decimal, octal, hexadecimal, ASCII, double precision, floating point, or literals.

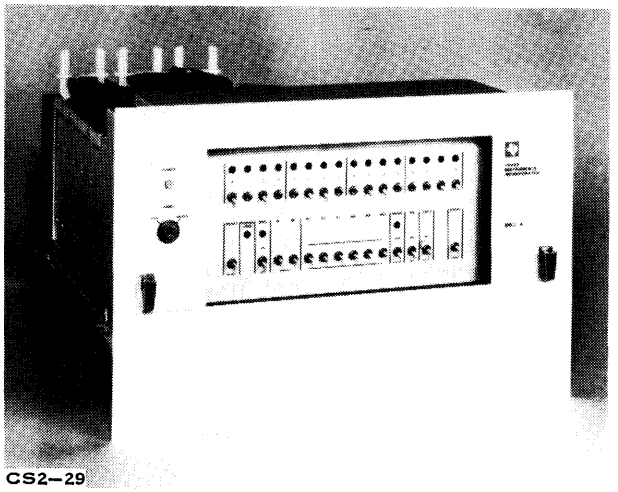
Micro Assembler. The Micro Assembler uses a set of macro and table definitions to permit symbolic development of microprograms which can be executed by the microprocessor of a Model 300 with Writable Control Store. The microassembler includes some automatic error detection capabilities, including misuse of mnemonics and missing parameters. The Micro Assembler runs under DOS and DOS-VM and requires 32K words of memory.

FORTRAN IV Compiler. The FORTRAN IV compiler is a 1-pass, extended ASA Fortran IV compiler that can run in a stand-alone environment as well as under DOS, DOS-VM, RTOS, and RTOS-VM. Special intrinsic functions have been added to the language; these functions allow the compiler to generate in-line coding by using additions made to the instruction set instead of calling a subroutine. These functions are XOR, AND, NOT, IABS, and SHFT. Logical and arithmetic statements have similarly been optimized to eliminate the need to call function subroutines. A special array called LIST allows references to absolute memory locations; this feature is useful when the FORTRAN compiler is used to write an operating system. Finally, Prime FORTRAN IV is backed by a library of standard mathematical functions defined by the Workshop on Standardization of Industrial Computer Languages.

Interpreter. The BASIC interpreter is an extended BASIC capable of operating under DOS and DOS-VM or as a stand-alone system. Three modes are possible: conversational, batch, and immediate. BASIC programs can call subroutines written in FORTRAN or assembly language. Numeric, string, and array values can be specified, and arithmetic string and relational operators can be used. The memory required for the interpreter can be from 7.2K to 10.2K words or more depending on whether or not formatted printing, matrix, handling, and double-precision arithmetic are included.

TEXAS INSTRUMENTS

TI 960B System Report



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OVERVIEW

The Texas Instruments 960B is a microprogrammed minicomputer using a high-speed MOS memory (750 nanoseconds) and automatic error checking and correction. The system replaces the earlier 960A, also a semiconductor-based system but with a smaller chip necessitating more memory boards per system. The 960A originally introduced in November 1971 in turn was predated by the 960, a core-based system no longer in production. Texas Instruments continues to support the 960A but actively markets only the 960B.

TI 960B uses a 4K semiconductor random access memory chip; one board can contain 8K, 16K, or 24K words of memory. The main chassis can now hold up to 65K words of memory, thus eliminating the need for a memory expansion chassis.

The 960B features:

- Sockets for each 4K chip, simplifying plug-in replacement.
- Error detection and correction circuits; light-emitting diodes provide easy identification of failed parts.
- Memory protect.
- 78 basic instructions, the same instruction set as the 960A.
- Up to 8K I/O lines.
- Communication Register Units (CRUs) that provide easy interfacing for many devices.
- Power fail/auto restart.
- Power supply that accommodates U.S., European, and Japanese ac power requirements.
- Rack-mounted chassis.

TI's 960B rack-mounted processor includes power supply, direct memory access channel, automatic error detection/correction, four CRU ports, and 8K words of memory. See Table 1 for the processor characteristics. Peripherals include standard terminal, magnetic tape, punched card, and paper tape devices, printers, and discs, process I/O subsystems, and communications interfacing. A large capacity 3330-type disc has recently joined the product line. A special set of CRU data modules simplifies attaching non-TI equipment.

Table 1. Texas Instruments TI 960B Processor Characteristics

CENTRAL PROCESSOR	
Microprogrammed	Yes
Number of internal registers	Two sets of 8 accumulators and index registers
Number of instructions	
Standard	78
Optional	22
Fixed-point arithmetic	
Add/subtract	Standard
Multiply/divide	Optional
Add time (μsec)	3.6
Floating-point arithmetic	Subroutines
Special features	Worker/supervisor operating modes
ADDRESSING	
Direct (number of words)	65,536 for 1-address format
Indirect	Yes, for 1-address format
Indexed	Yes
MAX NUMBER OF I/O DEVICES	256
OTHER FEATURES	Addressing to bit level
PRIORITY INTERRUPT	
System	
Lines	3
Levels	Software
MEMORY	
Type	MOS semiconductor
Word length (bits)	
Cycle time/word (μsec)	750 nsec
Capacity (words)	
Minimum	8,192
Maximum	65,537
Increment size, words	8K, 10K, 24K
Checking	6 bits, auto correct
Protect	Std, not programmable
ROM	Optional
Use	Bootstrap loader, Control ROM
I/O CHANNELS	
Programmed I/O	CRU register
Direct Memory Access (DMA) Channels	1 std; 6 opt
Multiplexed I/O	No
MAXIMUM TRANSFER RATE (WORDS/SEC)	
Within memory	214K without indexing; 170K with indexing
Over DMA	1.3 million

TI offers a battery pack option for the 960B to solve the problem of the volatile nature of semiconductor memory. The battery pack plugs into the processor chassis and can supply standby power to 16K words of semiconductor memory for a minimum of two weeks. It includes an automatic switchover circuit for power failures and startups and a circuit for fast battery recharge.

The 960B uses the same software as the 960A; its operating systems are Programming Support Monitor and

Process Automation Monitor. The 960B languages are Symbolic Assembly Language (SAL) and Process Control Language (PCL/A), which is an extension of basic FORTRAN and uses the Texas Instruments Language Translator (TILT).

The 960B like the 960A is a "manufacturer's control computer"; hardware features and software support bit manipulation for communication with control devices. It also is well suited to data acquisition and process control applications. The Communications Register Unit (CRU) facility provides from 32 to 8,192 I/O lines to connect noncomputer and slow-speed peripheral devices to the 960B. The processor can address and sense or set individual lines or groups of lines. The 960B FORTRAN language extends basic FORTRAN to support bit processing and real-time operations and make it a Process Control Language (PCL). TI also provides a general-purpose macro processor that translates user-defined languages into the 960B's FORTRAN or ASSEMBLER language for programming special-purpose applications.

The operating system and the Process Automation Monitor—both disc (PAM/D) and nondisc (PAM) versions—provide a multiprogramming environment using executive and worker modes for real-time, on-line processing.

Competitive Position

The TI 960B hardware and general software are well suited for data acquisition, process control, and manufacturing control applications. The Communications Register Unit, the bit manipulation capability in the instruction set and the 960B FORTRAN language, the Process Automation Monitor, and the TILT macro processor make the TI 960B stiff competition in the large process and industrial control segments of the minicomputer market. Only systems designed for a specific type of process, manufacturing facility, or data collection application or general systems with software and special-purpose devices for particular applications can match the 960B's price/performance.

Texas Instruments is a major semiconductor maker, and thus can obtain its semiconductor chips in-house. The 960B incorporates the 4K chip and error-correcting logic at a price that makes it highly competitive with today's lower priced system.

Because TI is a large manufacturing company and uses many control computers in its operation, it has considerable experience in control applications. TI, however, is relatively inexperienced in marketing minicomputer systems as compared to the large minicomputer manufacturers. Thus, the success of the 960B in the marketplace will depend on TI's commitment to marketing and sales support of the system.

User Reactions

An OEM manufacturer setting up an industrial instrument monitoring data collection system selected the 960A over Interdata and Digital Equipment processors largely because the CRU interfacing allowed the system to handle I/O lines individually instead of in groups of eight. This user felt the system was a "hardware man's computer," in spite of a variety of reliability problems TI was having with the semiconductor chips. This user noted that TI was stepping up software development and he is impressed with the user's group.

CONFIGURATION GUIDE

The TI 960B is modular and can range from a processor with 8K words of memory, a Teletype ASR/TBE for I/O, and four CRU modules to a system with 65K words of semiconductor memory within the main chassis, line printer, magnetic tape, disc units, and 256 CRU modules. Ten CRU modules are currently available for digital control and data transfers, interfacing with analog devices, data communications equipment, timers, and interrupts.

Optional features include hardware multiply/divide, ROM bootstrap loader; CRU expansion from 4 to 16 ports, battery pack, and auto restart for emergency power; and additional memory.

Up to eight high-speed devices, such as magnetic tape transports or disc drives, can interface to a system via the direct memory access channel. Slow-speed devices interface to a system via CRU ports. See Table 2 for a list of system peripherals.

Table 3 outlines the configuration requirements for the basic general-purpose software packages. In addition Texas Instruments supplies a special disc-based ATS-960 Automated Test System for operating test instruments on analog, digital, and hybrid instruments at high speeds. The system accommodates up to four test stations, and uses a special ATLAS language designed for testing.

Compatibility

The TI 960 is upward program-compatible with the 960A and 960B. The 960A and B have some instructions not in the 960's instruction set, thus software developed for the 960A and B may not run on the 960. The 960 line is not program compatible with the TI 980, but they are data compatible and use many of the same peripheral devices. A disc or magnetic tape recorded by one computer, for example, can be read by the other.

MAINTENANCE

Texas Instruments provides three types of contract maintenance for purchased systems: basic, standard, and full coverage. Basic coverage provides for prime shift preventative and emergency maintenance, Monday through Friday, for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site. Standard coverage provides preventative and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventative service around the

Table 2. Texas Instruments TI 960B Series: Peripherals

Model No.	Description
Terminals	
6DT772/6DT733	"Silent 700" KSR/ASR Data Terminals, 30 cps
6DT033	Teletype ASR33, 10 cps
6VT912	Model 912 CRT 24 lines, 80 char, 2400 baud
6VT240	CRT with Edit, 27 lines, 74 char, 2400 baud
Paper Tape	
6PT300	300 cps reader
6PT375	300 cps reader, 75 cps punch
Punched Card	
6CR302	300 cpm reader
Printers	
6LP165/6LP330	165/330 cps dot matrix printers 64 char set 132 col
6LP080/808	356 lpm line printer, 64 char set, 132 col
6LP356	Same as 6LP080 except interfaces to DMA channel
Discs	
6DS330	3330-Type Disc Subsystem, 1-4 drives, 50M wds/drive
6DS100	Cartridge Disc Subsystem, 1-4 drives, 1.14M wds/drive
6DS114/6DS115	Head-per-track disc, 229K/456K wds/drive
6DS060/090/110	Head-per-track discs, 688K/917K/1147K wds/drive
6DS130/160/180	Head-per-track discs, 1.4M/1.6M/1.8M wds/drive
Magnetic Tape	
6MT979	9-track 800 bpi, 37.5 ips, 1-3 drives/controller
Process I/O	
6AD130/6AD150	Wide-Range A/D Converter Systems, 13-bit, 5 msec/15 bit, 25 msec up to 16 8-channel inputs
6AD409/6AD102	High-Level A/D Converter Systems, ± 4.096V/± 10.24V Full Scale analog inputs, up to 16 8-channel inputs
6DA030	General-Purpose D/A Converter System, 12-bits ± 5.12V, ± 10.24 and 4-20 ma D/A cards
CRU201/2/3	D/A Converters with 1, 2, or 3 registers, 12-bit number converted to ± 5V, ± 10V, or 0-± 10V
CRU401/2/3/4	A/D Converters, 1-16 channels, single-ended analog single converted to 12-bit number
CRU Data Modules	
CRU016/014	32 lines, all input or all output, respectively
CRU065/62/64	OCI interrupts for 5, 12, or 24 VDC, respectively
CRU019	Interrupt Module, 8 interrupt flip/flops, 8 mask flip flops
CRU571/72/74/78	Interval Timers for 1-, 2-, 4-, or 8- msec time intervals
CRU017	Communications Module for Bell 103A or F, 202C, or D Data Sets
CRU101	Data Module for 16 I/O lines EIA 232C compatible

clock, 7 days a week. In addition to these contracts, Texas Instruments provides service on an on-call basis for users without a contract, or outside of contracted hours, with the fee depending on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift, or on Sundays and holidays.

Table 3. Texas Instruments TI 960B System Software

Package	Description
PSM	**Program Support Monitor, single-program executive, requires 8K words of memory**
PAM	**Process Automation Monitor, on-line, real-time multiprogramming system requires 12K words of memory**
PAM/D	**Disc-based version of PAM, with file handling routines, requires 16K words of memory, disc**
PCL FORTRAN	**ANSI X3 10-1966 Fortran with extensions and deletions, requires 16K words of memory**
SAL	**Symbolic Assembly Language, runs under PSM, PAM, or PAM/D with 6.5K words of memory; cross Assembler version for IBM 360 requires 108K bytes of memory**
TILT	**Macro preprocessor for macro definitions**
Utilities	**Link Editor, Librarian, Bootstraps**

TYPICAL PRICES

Model Number	Description	Purchase $ (1)	Monthly Maint. $ (2)
	CENTRAL PROCESSOR AND WORKING STORAGE		
	960A Central Processor Unit (CPU; with memory parity, memory write protect, power fail warning interrupt, power-up interrupt with battery, removable control panel with key lock, 4 ports for semiconductor memory modules of 4K or 8K words, 1 port for DMAC interface, 4 ports for CRU cards, port for extended arithmetic option, space for battery pack option and internal CRU expansion option, power supply, rackmount chassis and slides; requires 12.25-in. vertical panel space)		
960A04	With 4,096 Words Semiconductor Memory	2,850	80
96A08	With 8,192 Words Semiconductor Memory	4,350	85
960B08	960B Central Processor Unit (Includes 8,192-word semiconductor memory expandable to 65K words)	4,350	85
	Semiconductor Memory Expansion		
6EX100	External Memory Expansion Chassis	500	2
AEX004	4K Expansion Module	1,400	8
AEX008	8K Expansion Module	2,500	12
BEX008	8,192-Word Expansion Module, 960B	2,000	12
BEX016	16,384-Word Expansion Module, 960B	3,500	24
BEX024	24,576-Word Expansion Module, 960B	5,000	36
	CPU Features		
6EX006	Battery Pack	100	NC
6EX055	+or - 15V Regulator	200	4
6EX500	Stand-Alone Cabinet	200	NC
6EX001	Extended Arithmetic Option	900	8
6EX005/033	ROM Bootstrap Loader	250	4
	Communications Register Unit (CRU) Options		
CRU210	Internal CRU I/O Expansion	300	NC
CRU205	CRU Expansion Chassis (+5V power, 14 amp; provides ports for 16 CRU modules; up to 4 can be interfaced to CPU through CRU interface card)	1,200	10
CRU515	CRU Expansion Chassis (includes + or -15V at 4 amp power supplies for operation of Video Terminal, EIA, A/D, and D/A converter modules+ all other CRU modules)	1,500	10
CRU555	CRU Expansion Card For 16 Address Modules	60	NC
CRU504	3 or 4 CRUs-to-CRU interface or Expansion Card For 1600 32 Address Modules	450	NC
CRU501	1 CRU-to-CRU Interface or Expansion Card	115	NC

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $ (1)	Monthly Maint. $ (2)
CRU502	2 CRUs-to-CRU Interface or Expansion Card	250	NC
	CRU Interface Modules (each requires 1 CRU port)		
CRU012	Data Module (16 inputs, 16 outputs; 2-way communication between CPU and devices that are operated by or generate on-off signals	200	5
CRU016	Data Module (32 inputs; 1-way communication between CPU and devices that generate on-off signals)	200	5
CRU014	Data Module (32 outputs; 1-way communication between CPU and devices operated by on-off signals)	200	5
CRU015	Data Module (contractor; 2-way communication between CPU and external relay-controlled devices; 8 inputs and 8 outputs, each able to act independently or as part of a group)	300	5
CRU019	Interrupt Module	150	5
CRU571/ 2/4/8	Interval Timer Module	200	5
CRU017	Full-Duplex EIA-Compatible Interface Module	350	5
	MASS STORAGE		
	Disc		
6DS330	3330 Type Disc Controller (230 VAC power required) Supports up to 4 disc drives, each storing up to 50 million words data; transfer rate 403,000 words/sec	15,950	150
6DS333	Primary Disc Drive	17,650	120
6DS311/2/3	First/Second/Third Add-on Disc Drive	17,650	120
6DS530	Disc Pack	1,000	–
6DS100	Magnetic Disc Master Kit, Moving-Head Removable	5,100	46
6DS808	DMAC Interface Only Kit for Moving-Head Disc	3,300	12
	Magnetic Disc Secondary Kit, Moving-Head Removable-Same as 6DS100 except without controller		
6DS201	First and third secondary units without disc power supply	6,000	38
6DS202	Second secondary unit with disc power supply	6,500	40
	Magnetic Disc Kit, Head-Per-Track, Heavy Duty		
6DS114	229K words	6,950	80
6DS115	458K words	10,300	100
6DS919	DMAC Interface Only Kit for Fixed-Head Disc	3,100	12
	Magnetic Disc Kit, High-Capacity, Head-Per-Track, Heavy Duty (Fixed-head, organized in fixed-length sectors each having 32 16-bit words; average access time 8.7 ms, transfer rate 220K words/second, includes rackmount disc unit, power supply, and cables)		
6DS060	688K words	28,400	105
6DS090	917K words	31,200	110
6DS110	1,147K words	41,100	115
6DS130	1,376K words	44,200	124
6DS160	1,606K words	47,300	130
6DS180	1,835K words	50,600	140
6DS919	DMAC Interface Only Kit for Fixed-Head Disc	3,100	12
	INPUT/OUTPUT		
	Magnetic Tape		
6MT979	Magnetic Tape Transport, Master Kit (TI Model 979 Transport, 9-track, 800-bpi, 37-1/2 ips)	7,950	38
6MT279	Magnetic Tape Transport, Secondary Kit	5,200	34
	Paper Tape		
6PT300	High-Speed Sprocket Drive Reader To 300 cps; bi-directional, async	850	13
6PT838	High-Speed Tape Reader Interface Kit Includes interface card and cable	500	5
6PT375	High-Speed Tape Reader/Punch Combination	2,800	35
6PT878	High-Speed Tape Reader/Punch Combination Interface Kit	700	8
	Punched Card		
6CR302	Card Reader Kit, 300-cpm	2,700	35
6CR828	Card Reader Interface Kit, 300-cpm	500	5
	Line Printers		
	Line Printer Kit, 132-Column, Medium Duty		
6LP165	165 cps	4,750	75
6LP330	330 cps	5,300	75
6LP838	Line Printer Interface Only Kit	750	5
6LP500	Line Printer Stand	250	–
6LP080	Line Printer Kit, 80-Column, 356-lpm, Heavy Duty	11,550	135
6LP808	Line Printer Interface Kit 80-Column, 356-lpm, Heavy Duty	450	5
	A/N DISPLAY		
6VT240	Video Display Terminal Kit, with Edit (includes 60 Hz, 115V, CRT display unit which provides 1,998-char screen (27 lines of 74 char)	3,650	23
6VT727	Video Display Interface Kit	450	5
6VT912	Video Display Terminal TI Model 912 CRT display unit	2,100	25
6VT717	Video Display Terminal Interface	450	5
6VT962	Slave Monitor for Display Only	635	10
	Typewriter-Oriented Terminals		
6DT772	"SILENT 700" KSR Data Terminal	1,500	20
6DT702	Interface Kit for "SILENT 700" KSR Data Terminal	450	5
6DT733	Twin Cassette "SILENT 700" ASR Data Terminal	3,100	25
6DT703	Interface Kit for Twin Cassette "SILENT 700" ASR Data Terminal	450	5
6DT033	Teleprinter, Teletype	1,500	45
6DT707	Interface Only Kit for ASR33-5JE (6DT033)	450	5
6EX701	Stand for ASR Single DMAC Controller CPU Mounting Kit	110	–
6MC050/ 1/2	For moving-head disc, fixed-head disc, 979 mag tape	500	5
6MC053	Unwired for custom application	450	5
	Single DMAC Controller Rack Mounting Kit		
6MC800/1 /2	For moving-head disc, fixed-head disc, 979 mag tape	1,000	10
	External DMAC Expansion Kit		
6MC215	A half-size, 28-connector motherboard	800	15
6MC210	A full-size motherboard	1,200	18
6MC500	DMAC Expansion Chassis	1,400	10
6MC909	DMAC Interface Card	200	2

NC – No Charge – Not Applicable

HEADQUARTERS

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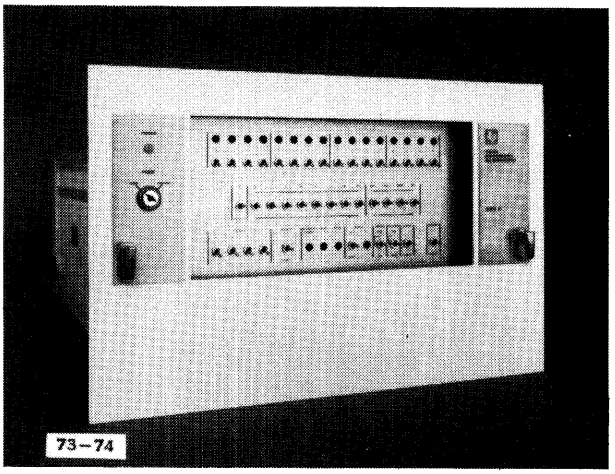

OVERVIEW

The TI 980B is a recently introduced microprogrammed replacement for the TI 980A system. Both use high-speed semiconductor MOS memory, but the 980B uses a 4K chip with error correction facilities to achieve even better price/performance than the 980A. Model TI 980B together with the Model TI 960B form Texas Instruments' current 900 series of fast (750-nanosecond cycle time), data-compatible 16-bit computers. They share many of the same options and peripherals but are not program-compatible with each other. The TI 980A, which was announced July 17, 1972 and delivered to the first customer outside of Texas Instruments on August 5, 1972, is still supported by Texas Instruments, but only the 980B is actively marketed.

The 980B 4K semiconductor random access memory chip allows 8K, 16K, or 24K words of memory to fit on one board. The main chassis can now hold up to 65K words of memory. The 980B features:

- Fault isolation indicator lights, providing easy identification of failed parts.
- Built-in single-bit error correction and multi-bit error detection.
- New power supply which accommodates U.S., European, and Japanese AC power requirements.
- 98 basic instructions (16, 32, or 48 bits).
- Bit/word/byte-string data addressing.
- Four hardware priority interrupt levels (optional interrupt expansion).
- Power failure interrupt/auto restart.
- I/O-oriented executive type monitor.
- Plug-in battery pack and auto restart upon power restoration (optional).

TI 980B is a general-purpose computer that complements the TI 960B by providing greater flexibility and power for problem solving through an extended instruction set and such arithmetic and control features as hardware multiply/divide, programmable memory protect, and privileged instructions. The TI 960B, on the other hand, is a "manufacturer's control computer" with hardware features and software to support bit manipulation for communication and control devices, data acquisition, and process control.

The two systems can be linked directly via an auxiliary processor port on the 980B that puts the 980B into a wait mode to allow the TI 960B to access or transmit data at memory speed. This is not a true multiprocessing environment because each operates independently of the other. The auxiliary processor port will also be used to connect other processing modules in the future, such as another 980B or a floating-point processor.

Two distinguishing characteristics are shared by the TI 960B and the TI 980B — semiconductor memory and low price. When the 960A and 980A were first announced, TI's low price for semiconductor memory made them cost competitive with large core memories for the first time anywhere in the computer industry. Although semiconductor memories are available for more minicomputer systems today, the prices of the 960B and 980B systems have made the product line maintain its favorable price/performance ratio. TI uses only semiconductor memory and no longer offers core memory even as an option.

Furthermore, the TI 980B includes many standard features characteristic of more expensive systems. In addition to the hardware multiply/divide, memory protect/privileged instruction set, and auxiliary processing features already mentioned, a basic system includes a ROM bootstrap loader, power fail detection, auto restart, one DMA channel and four I/O channels (expandable to eight and 256, respectively) and three levels of priority interrupt expandable to 67 levels. The real-time clock option available for the 960B is also available for the 980B.

TI offers a battery pack option to solve the problem of the volatile nature of semiconductor memory. The battery pack plugs into the processor chassis and can supply standby power to 16K words of semiconductor memory for a minimum of 2 weeks. It includes an automatic switchover circuit for power failures and startups and a circuit for fast battery recharge.

Peripherals for the 980B include discs, magnetic tape drives, printers, card and punched tape I/O, process I/O subsystems, and communications devices.

The two basic operating systems for the 980B are the basic system monitor (IOP) and the DX 980 multipurpose operating system. The 980B also uses the link editor, terminal source editor, symbolic assembler, FORTRAN IV compiler, BASIC/980 interpreter, expanded debug package, utility library, and the Texas Instruments Language Translator (TILT).

Table 1 lists the specifications for the 980B.

Table 1. Texas Instruments TI 980B: Mainframe Characteristics

CENTRAL PROCESSOR	
Microprogrammed	No
No. of Internal Registers	9
Addressing	15 modes
Direct (no. of words)	65K
Indirect	Yes
Indexed	Yes
Instruction Set	
Number (std, opt)	98, 106
Decimal Arithmetic	No
Floating-Point Arithmetic	Subroutine
Priority Interrupt Levels	3-67
MAIN STORAGE	
Type	MOS semiconductor
Cycle Time (nsec)	750
Basic Addressable Unit	Word
Bytes/Access	2
Min Capacity (words)	8,192
Max Capacity (words)	65,537
Increment Size (words)	8K, 16K, 24K
Checking	6-bits/wd, auto correct
Protect	Yes
ROM	
Use	Bootstrap loaders
Capacity (bytes)	512 (256 words) each
I/O CHANNELS	
Programmed I/O	4-256 ports
DMA Channels (no.)	1-8 ports
Multiplexed I/O	No
Max Transfer Rate Over DMA (words/sec)	1M (device limited)

Competitive Position

TI 980B is designed as a companion to the TI 960B which is used for data acquisition and control functions while the 980B is used for general processing functions. The 980B has an auxiliary processor port so the two systems can communicate with each other in a dual-processor configuration.

Although the 980B is more powerful than the 960B, the two systems have many characteristics in common, as well as a number of important differences. Both use the same MOS memory modules, power supplies, and peripherals. The 980B interfaces to peripherals via a conventional programmed I/O (PIO) or DMA channel. The 960B, however, has a special process automation interface instead of a PIO bus; this interface, called a Communications Register Unit (CRU), connects special-purpose peripherals and data communications controllers to the 960B.

Texas Instruments has designed special-purpose modules to interface to the CRU; these modules cannot be used with the 980B. Multiply/divide is standard on the 980B and optional on the 960B. Memory protect is programmable on the 980B and jumper selectable on the 960B. In addition, the memory protect feature is more sophisticated on the 980B than on the 960B. It includes a base register for program relocation and an upper limit register so that user programs can be relocated and confined to a specific memory segment.

The TI 980B is comparable in performance to other 16-bit minicomputers like the HP21MX, Data General Nova 820, Interdata Model 70, Digital PDP-11/40, General Automation SPC-16, Computer Automation Alpha 16, and Prime 200. The TI 980B does not have memory mapping or other facilities for extending systems into the small and medium computer range. Although Texas Instruments has been slow to develop software support, the recent introduction of the DMX 980 Multiprogramming Operating System and the Basic/980 package puts the system in a more competitive stance. The type of software support and its low cost make the 980B most competitive for the OEM market. The 980B combined with the 960B is a strong competitor with the systems mentioned earlier for control applications that require extensive processing or off-line program development.

Texas Instruments is a major semiconductor manufacturer, which partially explains the low price of the large MOS semiconductor memories available for the 960B and 980B. In addition, the firm is a large user of its own minicomputer systems for control and general processing applications; thus it has designed its systems to meet the needs of this segment of the minicomputer market.

User Reaction

One large OEM user of the 980A incorporated the TI processor into two different types of systems. In one system, the 980A is the central controller driving 40 remote POS terminals. In the second, it is being developed as a front end to a Honeywell CPU for a service bureau. The TI 980A processor was chosen for the POS system over Digital Equipment and Data General systems because it is faster, uses a larger instruction repertoire, and is considerably less expensive. Another attractive feature was the built-in hardware arithmetic. The 980A was chosen over the 960A because the 980A FORTRAN was better, enabled by the more developed arithmetic capabilities and instruction set. The 980A was chosen for the communications processor because the OEM user was already familiar with it and had found it to be reliable.

CONFIGURATION GUIDE

The 980B rack-mounted processor includes 8K words of MOS memory with a 750-nanosecond cycle time; hardware multiply/divide; double precision instructions for load, store, add, and subtract; programmable memory protection and privileged instructions; hardware relocation address register; ROM bootstrap loader; I/O bus with four ports (expandable to 13 ports in main chassis and 256 ports overall); a DMA channel expandable to eight ports; eight directly addressable hardware registers, and a status register. The processor is priced at $4,975 in single unit quantity; this price is reduced to $3,915 for quantity purchases of 50 units.

Up to eight controllers for high-speed devices, such as magnetic tape transports or disc drives, can interface to a system in most combinations via DMA. Slow-speed devices interface to a system via the I/O bus. One high-speed device controller connects to each DMA channel; there are no restrictions on the combination of different controllers that can be connected to a system with multiple DMA channels, other than the upper limit of eight DMA channels. Modules are currently available for digital control and data transfers, interfacing with analog devices and data communications equipment. Printers, punched tape and paper tape I/O, and several types of terminals can also be attached; see Table 2. The configuration requirements of the basic software packages are listed in Table 3.

Table 2. Texas Instruments TI 980B: TI Series Peripherals

Model No.	Description
Terminals	
8DT772/8DT733	"Silent 700" KSR/ASR Data Terminals, 30 cps
8DT033	Teletype ASR33, 10 cps
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8VT240	CRT with Edit, 27 lines, 74 char, 2,400 baud
Paper Tape	
8PT300	Reader, 300 cps
8PT375	Reader, 300 cps, punch, 75 cps
Punched Card	
8CR302	Reader, 300 cpm
Printers	
8LP165/8LP330	Dot matrix printers 64-char set, 132 cols, 165/330 cps
8LP080/808	Line printer, 356 lpm, 64-char set, 132 cols
8LP356	Same as 6LP080 except interfaces to DMA channel
Discs	
8DS330	3330-Type Disc Subsystem, 1-4 drives, 50M wds/drive
8DS100	Cartridge Disc Subsystem, 1-4 drives, 1.14M wds/drive
8DS114/DS115	Head-per-track disc, 229K/456K wds/drive
8DS060/090/110	Head-per-track discs, 688K/917K/1147K wds/drive
8DS130/160/180	Head-per-track discs, 1.4M/1.6M/1.8M wds/drive
Magnetic Tape	
8MT979	9-track 800 bpi, 37.5 ips, 1-3 drives/controller
Process I/O	
8AD130/8AD150	Wide-Range A/D Converter Systems, 13-bit, 5 msec/15-bit, 25 msec, up to 16, 8-channel inputs
8AD409/8AD102	High-Level A/D Converter Systems, ± 4.096V/± 10.24V full scale analog inputs, up to 16 8-channel inputs
8DA030	General-Purpose D/A Converter System, 12 bits ± 5.12V, ± 10.24 and 4-20 ma D/A cards
Communications	
8EX777	Communications Module for Bell 103A or F, 202C, or D DataSets
8EX886/880	Data Module for 16 I/O lines, TTL compatible
8EX555	Vectored Interrupt Module, 8 levels, preassigned priority
8EX579	Interval Timer Module, 12-bit counter, 10 μsec, 100 μsec, 1 msec, or 10 msec

Table 3. Texas Instruments TI 980B: System Software

Package	Description
Basic System Monitor (IOP)	Single program monitor for minimum system with 8K-word memory, console terminal; paper tape I/O, card I/O, disc option
DX980 Operating System	Multiprogramming, real-time operating system; requires 16K-word memory, interval timer, operator console, 100K-word disc, and input device (magnetic tape, cassette, punched card or paper tape)
Fortran IV	ANSI Fortran IV x 3.9-1966 standards with extensions, requires 24K-word memory under IOP or DX980
BASIC/980 Interpreter	Dartmouth BASIC with extensions for up to 8 terminals; requires 8K words of memory and terminals
SAPG Assembler	Two-pass absolute or relocatable assembler; requires 8K-word memory
TILT	Macro processor designed as prepass to assembler or compiler for language extension via macro definitions or added functions
Utilities	Link Editor, Terminal Source Editor, Disc Build Routines, Non-Disc SYSGEN, Expanded Debug, Math library, code conversion routines

Compatibility

The 980A and 980B are completely compatible with one another, given comparable configurations. TI 980B is not program compatible with the TI 960 A/B but they are all data compatible and use many of the same peripheral devices. A disc or magnetic tape recorded by one computer, for example, can be read by the others.

Memory modules and power supplies for the 960A and 980A are interchangeable, and similarly memory supplies for the 960B and 980B are interchangeable. Two cross assemblers are available, a 960A or B Cross Assembler for assembling 960A or B programs on the 980A or B and a 360 Cross Assembler for assembling 980A or B programs on an IBM System/360 operating under either OS or DOS.

MAINTENANCE

Texas Instruments provides three types of contract maintenance for purchased systems — basic coverage, standard, and full. Basic coverage provides for prime shift preventive and emergency maintenance, Monday through Friday, for any 9 consecutive hours between 7 a.m. and 6 p.m. at the user's site Standard coverage provides preventive and emergency service at the user's site for 16 consecutive hours between 7 a.m. and 1 a.m., Monday through Friday. Full coverage provides for on-site emergency and preventive service around the

clock, 7 days a week. In addition to these contracts, Texas Instruments provides service on an on-call basis for users without a contract, or outside of contracted hours, with the fee depending on whether equipment is delivered to a repair depot or is repaired on-site during the prime shift or outside the prime shift, or on Sundays and holidays.

TYPICAL PRICES

Model Number	Description	Purchase $ (1)	Monthly Maint. $ (2)
	CENTRAL PROCESSOR AND WORKING STORAGE		
	980A Central Processor Unit (CPU; wired for internal expansion to 32K words)		
980A04	With 4,096-Word Semiconductor Memory	3,475	90
980A08	With 8,192-Word Semiconductor Memory	4,975	95
	980B Central Processor Unit (includes 8,192-word semiconductor memory expandable to 65K words)	4,975	85
980B16	With 16,384-Word Semiconductor Memory	6,475	97
980B24	With 24,576-Word Semiconductor Memory	7,975	109
	Semiconductor Memory Expansion		
8EX100	External Memory Expansion Chassis	500	2
AEX004	4K Expansion Module	1,400	8
AEX008	8K Expansion Module	2,500	12
BEX008	8,192-Word Expansion Module, 980B	2,000	12
BEX016	16,384-Word Expansion Module, 980B	3,500	24
BEX024	24,576-Word Expansion Module, 980B	5,000	36
	CPU Features		
8EX066	Battery Pack	100	NC
8EX055	+ or -15V Regulator	200	4
	I/O Bus Options		
8EX213	980A Internal I/O Bus Expansion	450	6
	980A External I/O Bus Expansion Kit		
8EX217	Kit, 7.5 amp at 5 VDC and 1.5 amp at ±15 VDC	1,200	12
8EX227	Kit, 14.5 amps at 5 VDC	1,200	10
8EX887	980 I/O Expansion Card	200	5
	980 I/O Bus Interface Modules		
8EX886/880	Input Module	300	5
8EX196	16 I/O Data Module Test Kit	20	–
8EX777	980 Communication Module A FDX TTY-EIA module that plugs into any I/O bus slot; serves as the serial interface for Bell data sets 103A or F, 202C or D, terminal device with an RS232C interface, and OCI coupled current loop	450	6
8EX797	980 Communication Module Test Kit	35	–
8EX555	Vectored Interrupt Module	500	5
8EX579	Interval Timer Module	300	5
	DMAC Expansion Options		
	Single DMAC Controller CPU Mounting Kit		
8MC050/1/2	Moving-head disc; fixed head, mag tape	500	5
8MC053	Unwired for custom application	450	5
	Single DMAC Controller Rack Mounting Kit	450	5
8MC800/1/2	For moving-head disc; fixed head, mag tape	1,000	10
	External DMAC Expansion Kit		
8MC215	Half-size, 28-connector, motherboard prewired for the expansion cards, with 24 unwired connectors	800	15
8MC210	Full-size motherboard prewired for all DMA controllers	1,200	18
8MC500	DMAC Expansion Chassis	1,400	10
8MC909	DMAC Interface Card	200	2
8DS330	3330-Type Disc Controller, supports up to 4 disc drives, each storing up to 50 million words data 403,000 words/sec	15,950	150
8DS333	Primary Disc Drive	17,650	120
8DS311/12/13	Additional Add-on Disc Drives	17,650	120
8DS530	Disc Pack	1,000	–
8DS100	Magnetic Disc Master Kit, Moving-Head Removable 1.14 million 16-bit words fixed-length sectors, each with 32 16-bit words, sector addressable, transfer rate 1.56 million bits/second	5,100	46
8DS808	DMAC Interface Kit for Moving-Head Disc	3,300	12
	Magnetic Disc Secondary Kit, Moving-Head Removable (w/o controller)		
8DS201	First and third secondary units without power supply	6,000	38
8DS202	Second secondary unit with disc power supply	6,500	40
	Magnetic Disc Secondary Kit, Moving-Head Nonremovable		
8DS211	First and third secondary units w/o disc power supply	3,600	38
8DS212	Second secondary unit with disc power supply	4,450	40
8DS500	Disc Cartridge		
	Magnetic Disc Kit, Head-Per-Track Heavy Duty Fixed-head, sealed disc enclosure, organized in fixed length sectors each having 32 16-bit words; average access time 8.7 ms, transfer rate 220K words/second	150	–
8DS114	229K words	6,950	80
8DS115	458K words	10,300	100
8DS919	DMAC Interface Kit for Fixed-Head Disc	3,100	12
	Magnetic Disc Kit, High-Capacity, Head-Per-Track, Heavy Duty Fixed-head, continuous helium purge of sealed disc enclosure, organized in fixed-length sectors each having 32 16-bit words; average access time 8.7 ms, transfer rate 220K words/second		
8DS060	688K words	27,500	105
8DS090	917K words	31,200	110
8DS110	1,147K words	41,100	115
8DS130	1,376K words	44,200	124
8DS160	1,606K words	47,300	130
8DS180	1,835K words	50,600	140
8DS919	DMAC Interface Only Kit for Fixed-Head Disc	3,100	12
	INPUT/OUTPUT		
	Teleprinters		
8DT772	"SILENT 700" KSR Data Terminal	1,500	20
8DT702	Interface Kit for "SILENT 700" KSR Data Terminal	550	7
8DT733	Twin Cassette "SILENT 700" ASR Data Terminal	3,100	25
8DT703	Interface Kit for Twin Cassette "SILENT 700" ASR Data Terminal	550	7
8EX701	Stand for ASR	110	–
8DT033	Teleprinter, Teletype	1,500	45
8DT707	Interface Only Kit for ASR33-5JE	450	4
	CRT		
8VT912	Video Display Terminal TI Model 912 CRT display unit	2,100	25
8VT717	Video Display Terminal Interface Only	550	7
8VT962	Slave Monitor for Display Only	635	10
8VT240	Video Display Terminal with Edit	3,550	23
8VT727	Video Display Interface Only Kit	550	7
	Paper Tape		
8PT300	High-Speed Sprocket Drive Reader	850	13
8PT838	High-Speed Tape Reader Interface Kit	500	5
8PT375	High-Speed Tape Reader/Punch Combination	2,800	35
8PT878	High-Speed Tape Reader/Punch Combination Interface Kit	700	8
	Punched Card		
8CR302	Card Reader, 300 cpm	2,700	35
8CR828	Card Reader Interface Kit, 300 cpm	500	5
	Line Printers		
	Line Printer, 132-Column, Medium Duty		
8LP165	165 cps	4,750	75
8LP330	330 cps	5,300	75
8LP838	Line Printer Interface Kit	750	5
8LP500	Line Printer Stand	250	–
8LP356	Line Printer, 80-Column, 356 lpm	11,300	135
8LP606	Line Printer DMAC Interface-Only Kit, 80-Column, 356 lpm (includes controller)	700	10
	Magnetic Tape		
8MT979	Magnetic Tape Transport, Master Kit TI Model 979 Transport, 9-track, 800 bpi, 37½ ips	7,950	38
8MT279	Magnetic Tape Transport, Secondary Kit	5,200	34

NC – No Charge

Notes:
(1) Discount schedules available from manufacturer upon request.
(2) Monthly maintenance prices are for basic coverage of 8 hours/weekday. Coverage of 16 hours/weekday plus 9 hours on Saturday available at 25% increase and 24 hour/day, 7 day/week coverage available at a 65% increase.

HEADQUARTERS

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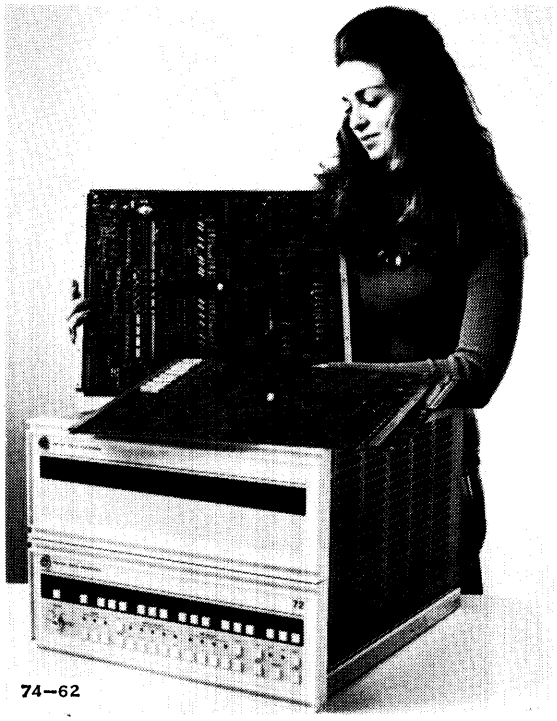

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OVERVIEW

The Varian V-70 Series consists of four models: V-71, V-72, V-73, and V-74, all based on a general-purpose, microprogrammed digital computer. Microprogramming for the basic system is implemented by a read-only memory of 512 64-bit words contained in the processor. Up to three Writable Control Store (WCS) modules of 256 or 512 words (64-bit) can be added to a system to store microprograms. The processor can execute these microprograms from either the basic control or WCS.

Main memory for the V-71 and V-72 consists of core modules only. For the V-73 and V-74, it can consist of core modules, semiconductor modules, or a combination. Each semiconductor module and some of the core modules have two ports of entry. While the V-71 and V-72 use only single-port modules, the V-73 and V-74 basic systems are dual-port systems that can attach either single- or dual-port memory modules. Differences among the models are summarized in Table 1.

Word length is 16 bits, increasing to 18 bits with the addition of memory parity. Cycle time per word is 660 nanoseconds for core memory and 330 nanoseconds for semiconductor memory.

The basic V-71, V-72, V-73, and V-74 microprocessors are Varian 620/f emulators. Thus, they can execute all the software that has been programmed for the 620 Series of computers and can also use all the 620 Series peripherals. The internal design of the microprocessor, however, has many features that are unavailable for the 620f: facility for a WCS of 256 to 1,536 words, 16 general-purpose registers, 18-bit-wide address bus, instructions to load the WCS from main memory and to jump to and return from WCS, and (optionally) hardware-implemented floating point. In addition, the microprograms executed from WCS can implement an entirely different instruction set from that of the 620/f, and can address 65K words of memory. Optional memory mapping, standard on the V-74, extends addressing to 256K words for V-72 and V-73. (Memory mapping is unavailable on the V-71.)

Varian uses WCS in three basic ways:

- To enhance the 620/f emulator by adding such features as a microprogrammed floating-point processor, byte move and compare instructions, stack manipulation, Fortran — do-loop terminator, and parameter passing optimizing.
- To microprogram functions specific to a user's application. Varian supplies a microassembler plus test and debug aids.
- To define new instruction sets that utilize the processor's advanced features, such as multiple general-purpose registers and 18-bit-wide address bus.

Table 1. Differences among V-70 Series Models

CHARACTERISTIC	V-71	V-72	V-73	V-74
MAIN STORAGE				
Type	Core (single port)	Core (single port)	Core (single or dual port); MOS (dual port)	Core (single or dual port); MOS (dual port)
Cycle Time (μsec)	1.2	0.66, 1.2	0.66 or 1.2 (core); 0.33 (MOS)	0.66 or 1.2 (core); 0.33 (MOS)
Min Capacity (bytes)	32K	16K	16K	64K
Max Capacity (bytes)	64K	64K (in std CPU); 512K with mapping	64K (in std CPU); 512K with mapping	512K (mapping std)
Increment Size (bytes)	32K	Core: 16K, 64K	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)	Core: 16K (dual port), 32K or 64K (single port); MOS: 16K (dual port)
Parity	No	Opt	Opt	Opt
Protect	Opt	Std	Std	Std
Memory Mapping	No	Opt	Opt	Std

The memory mapping option with virtual memory addressing of 262,144 words is supported by VORTEX II, a new version of the Varian Omni-Task Real-Time Executive (VORTEX) operating system. With VORTEX II, memory mapping is transparent to the user.

When the models of the V-70 Series are operating as 620/f emulators, they are faster than the 620/f and inherit the extensive software library from the 620 Series, first introduced in 1965. The 620 Series computers have been used extensively for process control, test and measurement, scientific processing, data acquisition, and general-purpose processing. Software support ranges from monitoring for small-scale stand-alone systems to real-time and batch operating systems for medium- to large-scale installations. The V-70 and 620/f specifications are compared in Table 2.

Today, the V-70 Series is a strong contender in the data communications market. Standard hardware configurations are available for front-end preprocessing, remote concentration, data switching, remote job entry, and network control. Special software runs under the VORTEX/VORTEX II operating systems.

Varian markets its minicomputers from 20 sales offices across the United States, four in Canada, and one in Mexico. Outside North America, the company has offices in Australia, Brazil, Germany, Belgium, France, Holland, Israel, Sweden, Switzerland, and the United Kingdom. The European organization's headquarters in Zug, Switzerland, also handles marketing to Yugoslavia, Spain, Portugal, Italy, Greece, Turkey, Africa, India, the Near East, and Socialist countries.

All Varian users are invited to become members of the VOICE Users Group, which promotes library maintenance and program exchange. Varian acts as a communications channel for the group in order to eliminate redundant effort when several users are trying to solve the same problem.

COMPETITIVE POSITION

Varian Data Machines has consistently been a leader in the minicomputer field with its 520 and 620 Series of computers. The 520 Series, which is no longer marketed, was based on 8-bit words and aimed primarily at OEM buyers. The 620 Series was well-designed initially, and

Table 2. Varian V-70 Series Compared with Varian 620/f

CHARACTERISTIC	620/f	Varian 70 Series
CENTRAL PROCESSOR		
Instruction Set		
Number (std, opt)	142 std, 8 opt	175 std, 18 opt
Floating-point arithmetic	Subroutine	Subroutine or hardware
Microprogramming	No	Yes
No. of Programmable Registers	3	3
Decimal Arithmetic	No	No
Addressing		
Direct (no. of wds)	32K	2K; 32K*
Indirect	Multilevel to 32K	Multilevel to 32K
Indexed	—	Pre and post to 32K wds
Priority Interrupt Levels	0-64 in 8-level increments	0-64 in 8-level increments
MAIN STORAGE		
Type	Core (single port)	Core (single or dual port); MOS (dual port)
Cycle Time (μsec)	0.75	0.66, 1.2 (core); 0.33 (MOS)
Memory Mapping	No	Yes (opt on V-72, V-73; std on V-74)
Min Capacity (bytes)	8K	16K (core); 16K (MOS)
Max Capacity (bytes)	64K	512K with mapping
Increment Size (bytes)	8K, 16K	16K, 32K, or 64K (core); 16K (MOS)
Parity	No	Opt
Protect	Opt	Std
ROM	Opt	Std control store; WCS opt
Use	Program	Microcode
Capacity (bytes)	—	1,528 wds (64-bit wd)
I/O CHANNELS		
Programmed I/O	Std	Std
DMA Channels (no.)	Std (up to 4 with BICs); PMA opt (4)	Std (up to 4 with BICs); PMA opt (4)
Multiplexed I/O (no. of subchannels)	No	No
Max Transfer Rate (wds/sec)		
Within memory	222,222	252,525 (core); 505,050 (MOS)
Over DMA	274K; 1.3M (PMA)	382.7K; 1.5M (PMA-core memory); 3.3M (PMA-MOS memory)

its longevity rivals that of such durable competitive systems (and their compatible successors) as the DEC PDP-8, Honeywell 16 and 700 Series, Hewlett-Packard 2100 and 21MX Series, and IBM 1130. Like the manufacturers of these systems, Varian has kept the 620 Series competitive by adding new features: faster memories, better I/O facilities, more interrupt levels, new peripherals, and extensive software support.

Although the V-70 Series uses a microprogrammed processor that is quite different from the 620 Series processors, the basic system provides upward software and peripheral compatibility with the 620 by emulation. The V-70 Series, however, is much more powerful and flexible than the 620 because it can implement new features and new instruction sets in WCS. Also, fast MOS memory modules can be used on the V-70 to increase throughput.

With memory mapping, the V-70 can support up to 256K words (512K bytes) of main memory as compared to 32K words on the 620 Series (65K on 70 Series systems using WCS). The floating-point processor, released in 1974, is about 30 times faster than the 620 floating-point subroutines.

The V-70 competes with the systems mentioned previously, in real-time data acquisition, process control and industrial control applications, data communications, and general-purpose batch processing jobs. With its expanded memory capacity, using memory mapping, it also competes with such larger systems as the PDP-11/45, PDP-15, Sigma 5, Hewlett-Packard 3000, and the new Data General Eclipse.

The path Varian has chosen for the V-70 Series protects the 620 customers' investment in software and peripherals, and gives the 620 users a system for upgrading. In addition, the V-70 expands the market for Varian computers. Outside the OEM market, customers who will microprogram WCS are probably few. The feature adds considerable system flexibility and can significantly increase throughput for certain applications.

The new V-71 model, meanwhile, extends the V-70 Series downwards, providing new customers with a low-cost entry-level system. The compact 16K-word memory modules can be used on the other processors, effectively lowering the price of the whole line.

Varian's floating-point processor (delivered in 1974) handles both single and double floating-point operations. Tests run by Varian on the V-72 and V-73 indicate problems, such as double-precision A = B + C, A = B • C and A = B ÷ C running in the actual operating system environment compare favorably with a Data General 840 operating under FORTRAN V and with a PDP-11/45.

User Reactions

A southern company that specializes in computer-based law enforcement, hospital, and other special control systems selected the V-73 for its law enforcement system because of the VORTEX software. The company felt that VORTEX was the best real-time operating system on the minicomputer market. At present this company uses Digital and Hewlett-Packard computers as well as the Varian 620 in hospital and other control systems.

The largest of the five law enforcement systems that this firm currently has in operation includes dual processors. Each processor has 32K words of core, a 200-million-word disc subsystem, two tape drives, two TTYs, card reader, paper tape reader, printer, two communication controllers, a variety of user-interfaced terminals, and special peripherals and disc and line switches installed by the user. Since its introduction, the system has been used successfully to emulate IBM 2740s that can communicate with state-owned computers. This law enforcement system is basically a data bank for wanted criminals, stolen goods, vehicle registration checks, and so on. VORTEX software has lived up to the company's high expectations, and the Varian components are extremely reliable. The user noted, however, that the OEM electromechanical devices were not quite as reliable.

A second V-73 user is a manufacturer primarily involved with the design and development of NASA's mission control center in Houston. The company also has a contract with NASA to maintain the medical records' storage and retrieval system for the space center's employees.When the system was set up, the first choice was the Hewlett-Packard 3000. Although Varian 73 was the second choice, it was still selected because of price. Additional savings resulted from "borrowing" peripherals from the seven Varian 620s already being used by the firm for other purposes. The programming staff could readily handle the required major modification to VORTEX because the assembly language was already familiar.

In retrospect, this user was glad the company had chosen Varian, because the installation was set up in a reasonably short time. Hewlett-Packard would have required a longer period because it had some initial problems with the 3000 software. Varian, moreover, compares favorably with other minicomputer manufacturers for system support and hardware reliability. NASA's mission control center has 15 minicomputers, including three Digital PDP-11/45s, seven Varian 620s (used mostly in dedicated applications), the V-73, and four minicomputers from other manufacturers. The V-73 has performed very well — this user, in fact, characterized it as a "better, cheaper 11/45."

CONFIGURATION GUIDE

All models in the V-70 Series are based on the same processor hardware. The chief differences among the

four models are the type of memory used and its related options. The V-71 and V-72 use single-port core memory exclusively. The V-73 handles dual-port core and MOS memory modules. Minimum systems include 8K words (V-72 and V-73) or 16K words (V-71) of memory; memory expansion to 32K words is standard. With the memory mapping option, memory expands to 256K words. The minimum V-74 system is a 32K-word, dual-port system using either core or MOS modules. A number of V-72 and V-73 options, such as memory mapping, are standard features.

The basic processor for all three systems has hardware multiply/divide, at least one real-time clock, power fail/restart, memory protection, I/O bus with direct memory access (DMA), at least one automatic bootstrap loader (three are standard on the V-74), chassis for up to 32K words of memory, power supply, and programmer's console. In addition to a larger initial memory and memory mapping, the V-74 processor includes as standard the following features: priority memory access (PMA), 512 64-bit words of WCS, the equivalent of the first I/O chassis (18 slots), the equivalent of a memory expansion chassis with power for four memory modules, and a keyboard/CRT display terminal. All of these items are options on the V-73, so it can theoretically expand to the equivalent of any V-74 configuration. However, an expanded V-73 is more expensive than the equivalent V-74 configuration. The V-71 and V-72 are more restricted; they are single-port systems and cannot handle the faster MOS memory modules. As a result, they are slower and less powerful than the V-73 and V-74; moreover, the V-71 cannot support the mapping option.

All three systems have various submodels to designate whether core or MOS memory, memory parity, or PMA are included. Table 3 lists the features of the various processor submodels.

Up to 32K words of memory can fit the mainframe for all processors; an expansion chassis is attached for each additional 32K words of memory (one expansion chassis is standard on the V-74). Each processor has a number of printed-circuit slots within the mainframe for attachment of options and peripherals ("P" slots). An I/O expansion chassis is available to attach additional peripheral devices and related options (such as the priority interrupt modules). Peripheral devices or options require either an I/O- or P-type slot. In addition to the number of P slots, expansion of the peripheral load must consider the bus load, which expands in increments of 10 loads after the original 10 in the main chassis have been exhausted.

In addition to the optional memory parity, memory mapping, and PMA features already described, a number of important options add flexibility to the processor and facilitate use of the peripherals. The WCS option can add up to three increments of 256 or 512 64-bit words to extend the processor's read-only control memory for additional user- or Varian-defined microinstructions. A data save option provides battery power to preserve the

Table 3. Varian V-70 Series: Standard Features for Processor Submodels

Processor Submodel	Memory Size (wds)	No. of P Slots	PMA	Parity (2 bits)	Memory	Data Save	System Availability			
							V-71	V-72	V-73	V-74
1000	32K	5	—	—	Core	—	—	—	—	X
1050	32K	5	—	Yes	Core	—	—	—	—	X
1100	8K	14	—	—	Core	—	—	X	X	—
1101	8K	14	Yes	—	Core	—	—	X	X	—
1200	8K	14	—	Yes	Core	—	—	X	X	—
1201	8K	14	Yes	Yes	Core	—	—	X	X	—
1300	16K	14	—	—	Core	—	—	X	—	—
1301	16K		Yes	—	Core	—	—	X	—	—
1330	16K	4	—	—	Core	—	X	—	—	—
1340	16K	4	—	—	Core	—	X	—	—	—
1350	16K	4	—	—	Core	—	X	—	—	—
1400(1)	16K	14	—	Yes	Core	—	—	X	—	—
1400(2)	32K or 16K	8	—	—	MOS	—	—	X	—	X
1401	16K	14	Yes	—	Core	—	—	X	—	—
1450	32K	8	—	Yes	MOS	Yes	—	—	—	X
1500	8K	4	—	—	MOS	—	—	—	X	—
1501	8K	4	Yes	—	MOS	—	—	—	X	—
1600	8K	4	—	Yes	MOS	—	—	—	X	—
1601	8K	4	Yes	Yes	MOS	—	—	—	X	—

Notes:
(1) Two Model 1400 processors are defined: one is a 16K-word core-based processor and the other is a 32K-word MOS-based processor.

contents of semiconductor memory modules during a loss in line voltage. The Priority Interrupt Module (PIM), Buffer Interlace Controller (BIC), and Block Transfer Controller (BTC) are particularly important for efficient handling of the various peripheral I/O subsystems. In addition, the hardware floating-point processor can appreciably enhance throughput for some applications.

In addition to the "basic" V-71, V-72, V-73, and V-74 processors, Varian offers five "standard" hardware/software packages:

- Model 72-0001 — 16K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, paper tape reader, and Teletype.
- Model 72-0002 — 24K-word, V-72-based Batch/FORTRAN Processing System with cartridge disc, line printer, nine-track magnetic tape drives, card reader, and Teletype.
- Model 72-0011 — 24K-word, V-72-based real-time operating system under VORTEX, with cartridge disc, card reader, and Teletype.
- Model 73-0020 — 32K-word, V-73-based real-time operating system under VORTEX, with cartridge disc, line printer, nine-track magnetic tape drive, card reader, and Teletype.
- Model 74-0050 — 64K-word, V-74-based real-time operating system with 512-word WCS and FORTRAN accelerator firmware, memory mapping, high-density (14.5-million-word) disc, line printer, nine-track magnetic tape drive, card reader, paper tape reader and punch, keyboard/CRT, and BTC.

Included in each package is the appropriate number of PIMs, BICs, I/O chassis, and cabinets to support the configuration.

The peripheral device complement for the V-70 Series includes: teletypewriters, paper tape and punched card equipment, line printers, and an impressive number of magnetic tape and disc storage units. Special peripherals are an oscilloscope display, plotters, various digital I/O controllers, and an extensive list of analog/digital equipment. Controllers are also offered for a number of commercial communications data sets. See Table 4 for a listing of peripherals with specifications.

Software includes two full-blown operating systems: VORTEX, which provides multiprogramming capability with real-time foreground processing and background batch processing, and MOS, which controls batch processing systems. VORTEX II is a special version of VORTEX used on systems with memory mapping.

Several language processors are available: DAS assembler (three versions), FORTRAN IV, two versions of BASIC, and RPG IV. BEST, a real-time monitor, provides control for small, dedicated real-time systems. Maintenance, debugging, and editing programs are offered, along with a math library. Table 5 lists major software packages and configuration requirements.

Table 4. Varian V-70 Series: Peripherals

Model No.	Description
Discs	
70-7500/01	Moving-head disc, 14.5M wds/2316-type pack, 4 drives/controller
70-7510/11	Moving-head disc, 46.7M wds/2316-type pack, 2 drives/controller
70-7600/01	Moving-head dual disc, 2.34M wds/drive, 1 fixed, 1 removable 5540-type cartridge, 2 drives/controller
70-7610/11	Moving-head disc, 1.17M wds/drive, 2315-type pack, 3 drives/controller
70-7700/1/2/3	Fixed-head discs, 61K/123K/246K/491K wds capacity, 17-msec avg access
Magnetic Tape	
70-7100/1	9-trk, 800 bpi, 25 ips; 4 drives/controller
70-7102/3	9-trk, 800 bpi, 37.5 ips; 4 drives/controller
Paper Tape	
70-6300	300-cps reader
70-6310/11	75-cps punch
70-6320	300-cps reader and 75-cps punch
Punched Cards	
70-6200	300-cpm reader
70-6201	35-cpm keypunch/punch
Terminals	
70-6100/2/4	Teletype ASR 33/ASR 35/KSR 35; 10 cps
70-6401	A/N CRT display with keyboard, TTY compatible
70-6400	Oscilloscope, Tektronix 611
Printers	
70-6701	245-1,100 lpm, 132 col, 64 char set
70-6720/21	300 lpm, 136 col, 64 char set
Printer/Plotters	
70-6606	80 styli/in. (1,320 A/N lines/in); 8.5-in. paper width
70-6608/02	100 styli/in. (1,000 A/N lines/in.); 11/14.875-in. paper width
70-6640	Model 70-6606 with 7x7 dot matrix print/plot, 64 char set
70-6641/42	Model 70-6608/02 with 7x11 dot matrix print/plot, 123-char set
70-661/3/5/7	100 styli/in. printer/plotters; 460/410/370/210 A/N lpm, 8.5/11/14.875/22-in. paper widths
70-6621/3/5/7	100 styli/in. printer/plotters with linear writing head, 690/890/690/550 lpm; 8.5/11/14.875/22-in. paper widths
Process I/O	
70-8000 Series	High-Level Analog Input Systems; 16-256 channels, differential & single-ended inputs
70-8100 Series	Low-Level Analog Input Systems; 13-bit A/D conversion, 16-256 channels
70-8200 Series	Digital-to-Analog (DAC) Subsystem; 10-, 12-, and 14-bit channels, to ± 10 volts, ± 10 mA; to 64 channels
70-8300	Digital Controllers; 1 16-bit input, 1 16-bit output register
70-8310/11	Digital Output; 2 16-bit output registers, 1 buffered input
70-8410/11	Digital Input; 4-256 16-bit input registers
70-8500	Relay Contact I/O modules
70-8601	Interface Console; for 16 channels, high-level analog input, 8 analog output, 1 digital I/O, 8 sense and control lines, timer, LED display

Table 4. (Continued)

Communications	
70-5201/2/3	MUX; for 16/32/64 sync, async, or direct-connection to 9,600 baud terminals
70-5211/2/3	Like 5201/2/3 but for systems with memory map
70-5702/12	BSC MUX; for up to 8 BSC channels via DMA; without/with memory mapping system
70-5401/02	Single/Dual Data Set Controller; for Bell 103 or 202
70-5501/02/03/04	Single or Dual Synchronous Controllers; to 2,400 or to 50K baud
70-5505/06/15/16	BSC Controller; for 1 or 2 channels, with or without memory mapping system
70-5601/02/03	Universal Async Controllers; with RS-232 C/20-60 ma current loop/20 ma relay
70-570	ACU Controller; for Bell 801

Table 5. Varian V-70 Series: Software

Package	Description
VORTEX	Real-time multitasking operating system with FORTRAN IV, RPG IV; requires CPU, PIM, BIC, 24K-word memory, TTY or CRT, and card, paper tape, or magnetic tape I/O
VORTEX II	Like VORTEX but with memory mapping management; same requirements as VORTEX except 32K memory and memory mapping option
MOS	Batch operating system with FORTRAN IV and RPG IV; requires CPU, PIM, BIC, 8K words of memory, magnetic tape I/O
Dataplot II	Adds Statos 31/33 printer/plotter capability to MOS; requires 16K words of memory
BEST (stand-alone)	Core-only real-time monitor; requires PIM, BIC, console
VPERT	Minimum 8K-word system software, paper tape I/O, runs under VORTEX (II) or MOS; requires either card reader or paper tape in addition to operating system
FORTRAN (stand-alone)	Requires CPU, paper tape I/O, PIM, BIC
RPG IV (stand-alone)	Requires CPU, card reader, card punch, line printer
Microprogramming support	Runs under MOS or stand-alone; requires paper tape card or magnetic tape I/O
BASIC	Single terminal version; requires TTY or CRT, 8K-word memory, paper tape I/O; extended version requires TTY or CRT, 16K words of memory, paper tape I/O, disc
HASP/RJE	Runs under VORTEX (or VORTEX II); requires card or magnetic tape I/O
VTAM	VORTEX telecommunications access method; runs under VORTEX or VORTEX II
NCM	Network Control Module, using Network Definition Language (NDL); interface between operator and system to simplify network definition

COMPATIBILITY

The V-70 Series is upward software compatible with Varian's 620 Series computers. Magnetic tape data formats are IBM compatible. The V-70 Series uses the same peripheral devices as the 620.

MAINTENANCE

Varian supplies two types of on-call service contracts. The full-service plan provides on-call, on-site maintenance and replacement of needed parts for the contracted shift(s), while the limited-service plan charges lower monthly fees but requires the customer to pay for replacement parts. Full-time, on-site maintenance contracts are also provided. Customers who do not want maintenance contracts can choose individual, on-call, on-site repairs, charged on a per-hour basis. As an alternative, they can take equipment to an authorized factory service location.

TYPICAL PRICES

Model Number	Description	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR & WORKING STORAGE		
	V-71 CPU (includes multiply/divide, I/O bus with DMA, chassis, power supply and programmer console, 1,200-nsec cycle time)		
71-1330	With 16K Core, 4 P Slots	7,200	120
71-1340	With 16K Core (includes power fail/restart, Teletype controller, automatic bootstrap loader for teletypes, real-time clock, 4 P slots)	8,100	120
71-1350	With 16K Core (same as 71-1340 except with memory protect)	9,100	120
71-2102	With 16K Core (includes single-port memory)	3,250	30
	V-72 CPU, 14 P slots		
72-1100	With 8K Core	10,500	120
72-1101	With 8K Core, Priority Memory Access (PMA)	11,500	125
72-1200	With Memory Parity and 8K Parity Core	11,500	125
72-1201	Same as 72-1200 with PMA	12,500	130
	V-73 CPU Same as V-72 except (chassis for up to 32K of dual-port memory, 14 P slots)	14,500	120
72-1300	With 16K Core	10,250	120
72-1301	With 16K Core (includes PMA)	11,250	125
72-1400	With 16K Parity Core (includes memory parity)	10,750	125
72-1401	With 16K Parity Core (includes memory parity and PMA)	11,750	130
73-1100	With 8K Core	14,500	120
73-1101	With 8K Core, PMA	15,500	125
73-1200	With Memory Parity and 8K Parity Core	15,000	125
73-1201	Same as 73-1200 with PMA	16,000	130
73-1500	With 8K MOS Memory, 4 P Slots	15,000	130
73-1501	With 8K MOS Memory, PMA, 4 P Slots	16,000	135
73-1600	With 8K Parity MOS Memory, 4 P Slots	15,500	135
73-1601	Same as 73-1600 with PMA, 4 P Slots	16,500	140
	V-74 CPU (same as V-73 except keyboard CRT display terminal, 3 automatic bootstrap loaders, console switch selectable PMA, direct memory access (DMA), memory map with memory protection for up to 256K of dual-port memory, 512 words of WCS, control console, processor, I/O, and memory chassis with associated power supplies in a single cabinet; provides 18 I/O slots, 8 MX slots, with power for up to four additional MOS or core memory modules and P slots as noted)		
74-1000	With 32K Core, 5 P Slots	35,900	345
74-1050	With Memory Parity and 32K Parity Core Memory, 5 P Slots	37,900	350
74-1400	With 32K MOS Memory, 8 P Slots	38,400	395
74-1450	With Memory Parity, 32K Parity MOS Memory, Data Saver, 8 P Slots	40,400	400
	CONFIGURATIONS		
V71-0007	V71-Based Real-Time Operating System (running under VORTEX 32K core memory; interleaved 1,200 nsec; ASR-33, TTY and a 2.34-M word disc; includes V71 with 16K-core memory; 16K core memory (1,200 nsec); disc – ABL; core memory interleaving; PIM; ASR-33 TTY; card reader, 300-cpm; disc., 2.34-M words; I/O chassis with PIM and BIC; equipment cabinet; VORTEX installation package; Maintain II)	29,500	305
72-0011	24K V-72-Based Real-Time Operating System (running under VORTEX w/a 2.3M-word cartridge disc, TTY, and card reader; includes V-72 with 8K core memory; 8K core memories (2); PIM (2); BIC (2); ASR-33		

TYPICAL PRICES (Contd.)

Model Number	Description	Purchase $	Monthly Maint. $
	Teletype; card reader (300 cpm); disc (2.34M-words); I/O chassis; cabinet; VORTEX installation package)	39,850	380
73-0020	32K Core Memory, V-73-Based Real-Time Operating System (includes V-73 with 8K core memory; 8K core memories (3); PIM (2); BIC (2); ASR-33 Teletype; card reader (300 cpm); line printer (245 lpm); 9-track mag tape (37.5 ips and control); disc (2.34M words); I/O chassis; cabinet (2))	71,600	515
74-0050	High Performance V-74-based Real-Time Operating System (includes V-74 with 32K memory; 8K core memories (4); block transfer controller; PIM (2); BIC; card reader (300 cpm); paper tape reader (300 cps) and punch (75 cps); line printer (245 lpm); mag tape (9-trk, 37.5 ips and control); disc (14.5M words); I/O expansion chassis; VORTEX installation package)	101,750	942
	Core Memories		
XX-2100	8K Word (16 bits) 660-nsec Cycle	3,500	30
XX-2101	8K Word (18 bits) 660-nsec Cycle	4,000	35
XX-2102	16K Word (16-bit) Core Memory (1,200-nsec cycle time, single port)	3,250	30
XX-2103	16K Word (18-bit) Core Memory (1,200-nsec cycle time, single-port)	3,750	35
XX-2400	32K Words	15,000	130
XX-2411	Same as 2401 except 18-bit.	17,000	150
	Semiconductor Memories		
	Available in dual-port models for V-73 and V-74. XX indicates the CPU series.		
XX-2500	8K Words (16 bits), 330-nsec Cycle	4,000	40
XX-2501	8K Words (18 bits), 330-nsec Cycle	4,500	45
	PROCESSOR OPTIONS		
XX-3001/2	Auto Bootstrap Loader	250	5
XX-3003/04	Automatic Bootstrap Loader (for rotating memory instead of "standard" for Teletype for 72 & 73)	950	10
XX-3010	Real-Time Clock	250	5
XX-3030	Core Memory (odd/even interleaving)	2,000	10
XX-3031	Odd-Even Interleaving (for single-port 1,200-nsec core memory in expansion chassis, up to 256K for 72, 73)	1,000	10
XX-3032	Odd/Even Interleaving (for 32K words of single-port 1,200-nsec core memory in CPU)	500	10
XX-3050	Wrap-Around Addressing Feature	250	5
XX-3060	230V ac, 50-Hz System Power Input	500	0
XX-3100	Block Transfer Controller (BTC)	1,500	10
XX-3101	Priority Interrupt Module	500	5
XX-3102	Buffer Interlace Controller (BIC)	500	5
73-3200	Data Saver Power Supply and Battery for 32K Words of Semiconductor Memory (V-73 only)	500	5
XX-3300	Memory Map	2,500	35
XX-3400	Floating-Point Processor	4,950	35
XX-4000	Writable Control Store (256 Words of Semiconductor Memory)	3,000	20
XX-4001	Writable Control Store (512 words)	4,000	25
XX-4002	Writable Control Store (512 words)	5,000	35
	MASS STORAGE*		
70-7500	Disc Memory and Controller (2316 pack, moving head, 14.5M words single spindle)	16,400	190
70-7501	Slave Unit for 70-7500	12,150	150
70-7510	Same as 7-7500 except 46.7M Words; Dual Head	30,300	275
70-7511	Slave Unit for 70-7510	25,550	235
70-7600	Disc Memory and Controller (5440 pack, moving head, 2.34M words, one fixed and one removable disc)	12,500	100
70-7601	Slave Unit for 70-7600	8,000	75
70-7610	Disc Memory and Controller (2315 pack, moving head, 1.17M words)	10,000	85
70-7611	Slave Unit for 70-7610	6,000	65
70-7700	Fixed-Head Disc and Controller (61K words, 17-msec avg access)	7,000	65
70-7701	With 123K Words	8,000	65
70-7702	With 246K Words	9,500	80
70-7703	With 491K Words	16,000	125
	INPUT/OUTPUT		
70-6100	ASR-33	1,580	35
70-6102	KSR-35	3,265	25
70-6104	ASR-35	5,320	30
70-6200	Card Reader and Controller (300 cpm)	4,000	40
70-6201	Card Punch and Controller (35 cpm)	8,000	60
70-6300	Paper Tape Reader and Controller (300 cps)	2,300	22
70-6310	Paper Tape Punch and Controller (75 cps, tabletop)	3,000	25
70-6311	19" panel mounted	3,000	25
70-6320	Paper Tape System (includes time-share controller, 300-cps reader, 75-cps punch)	4,700	47
70-6400	Oscilloscope Display	5,675	45
70-6401	Keyboard and Alphanumeric CRT	2,850	25
70-6402	Same as 70-6401 with 70-5602 controller	3,250	30
70-6403	Same as 70-6401 with kit and instructions to connect to controllers, or a spare unit	2,950	25
	PRINTER/PLOTTERS		
	STATOS® 31 FAMILY		
70-6606	8½-in. wide w/Controller (80 styli/in., 2.75 ips, 1,320 A/N lpi)	8,625	70
70-6640	Same as Model 70-6606 with 64-char 5 x 7 dot matrix hardware character generator and simultaneous print/plot options	9,325	70
70-6608	11-in. Wide Printer/Plotter with Controller/110 styli/in., 2.2 ips, 1,000 A/N lpi)	8,825	70
70-6641	Same as Model 70-6608 with 123 char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,525	70
70-6602	14-7/8-in. Wide Printer/Plotter with Controller (100 styli/in., 2.2 ips, 1000 A/N lpi)	9,025	70
70-6642	Same as Model 70-6602 with 123-char uc/lc, 7 x 11 dot matrix character generator, and simultaneous print/plot options	9,825	70
	Bi-Scan™ Writing Head Models		
70-6611	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1 ips, 460 A/N lpi)	7,975	70
70-6613	11-in. Wide Printer/Plotter with Controller (100 styli/in., 0.9 ips, 410 A/N lpi)	8,175	70
70-6615	14-7/8-in. Wide Printer/Plotter with Controller (100 styli/in., 0.8 ips, 370 A/N lpi)	8,875	70
70-6617	22-in. Wide Printer/Plotter with Controller (100 styli/in., 0.6 ips, 210 A/N lpi)	11,925	70
70-6621	8½-in. Wide Printer/Plotter with Controller (100 styli/in., 1.5 ips, 690 A/N lpi)	7,975	70
70-6623	Same as 70-6613 except 1.5 ips, 890 A/N lpi	8,175	70
70-6625	Same as 70-6621 except with 14-7/8-in. Wide Printer/Plotter with Controller	8,875	70
70-6627	Same as 70-6617 except 1.2 ips, 550 A/N lpi	1,925	70
	Line Printers		
70-6720	Line Printer and Controller (300 lpm, 136 col, 64 char, 11-position form length selector switch)	9,900	99
70-6721	Same as 70-6720 except 12-channel paper tape vertical format unit	10,200	102
70-6760	Static Eliminator Option	500	
70-6701	Line Printer (245 to 1,100 lpm, 132-col, segmented, buffered)	15,500	90
70-7100	Mag Tape Unit and Controller (9-trk, 800 bpi, 25 ips)	7,500	50
70-7101	Mag Tape Unit Slave	5,600	40
70-7102	Same as 70-7100 with 37.5 ips; includes control for 4 units	9,000	75
70-7103	Mag Tape Unit Slave	7,000	60
	DATA COMMUNICATIONS		
70-5201/11	Data Communications Multiplexor (including message oriented control for up to 16 high-performance communication channels)	2,750	25
	Data Communications (Contd.)		
70-5202/12	Data Communications Multiplexor (for up to 32 communications channels)	4,000	35
70-5203/13	Data Communications Multiplexor (for up to 64 communications channels)	7,000	60
	DCM LINE ADAPTERS		
70-5301	Asynchronous Line Adapter with RS232C and CCITT V24	1,000	6
70-5302/3/4	Direct-Connection Line Adapter	1,000	6
70-5305	Synchronous Line Adapter with RS232C and CITT V24	1,500	10
70-5306	Binary Synchronous Communication Line Adapter (for 1 communication channel)	1,500	10
70-5307	Automatic Call Unit Line Adapter	1,000	10
70-5308	Programmable Asynchronous Line Adapter (with RS232C or CCITT V24 compatibility for 4 channels of full- or half-duplex async operation up to 9,600 baud)	1,400	10
	ASYNCHRONOUS MODEM CONTROLLERS**		
70-5401	Data Set Controller	650	5
70-5402	Dual Data Set Controller	800	5
70-5501	Data Set Controller	1,250	8
70-5502	Dual 70-5501 Data Set Controller	1,800	12
70-5505/15	Binary Synchronous Communication (facilities for 1 communication channel)	3,000	20
70-5506/16	Binary Synchronous Communication (facilities for 2 channels)	4,500	20
	UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLERS		
70-5601/2/3	With RS232C Interface/20 or 60mA Current Loop or With 20 or 60mA Relay Interface	600	5
70-5701	Auto Call Unit Controller	1,250	8
	MULTIPLEXOR		
70-5702	Binary Synchronous Communication Multiplexor	2,000	20
	OPTIONS		
70-5801	Binary Synchronous Communications (wide-band interface option for Bell 300 Series modems.)	250	5

Notes:
* All controllers require ±12V dc.
(1) Varian Data Machines does not lease its systems.
(2) Maintenance prices are for full service contract; include on-call maintenance and replacement of required parts on the entire system. Prices are effective for installations within 100 miles of service center.

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HEADQUARTERS

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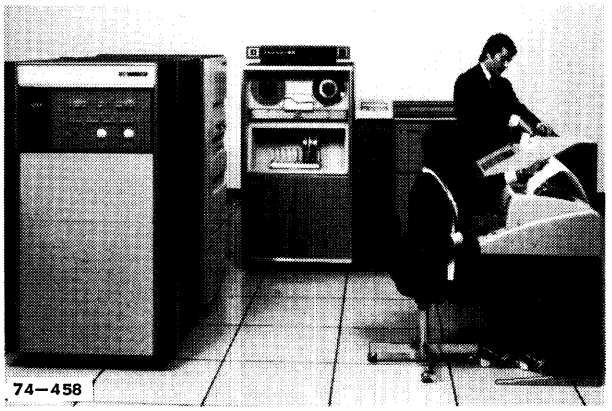
XEROX

530 System



OVERVIEW

Xerox 530 is a small, fast, modular computer that is designed to handle any type of processing, from business to process control. The basic 530 model contains a central processing unit (CPU), one input/output processor (IOP) with 16 channels, and one basic 8K-word core memory module. An expanded version of the 530 can include up to seven more 8K-word memory modules, a second IOP with 12 channels, a DIO interface, two DMA interfaces, and a dual processor adapter.

The 530 is intended for multiprogramming and multiprocessing environments. Its major applications are in process control, data acquisition and applications that require some scientific processing support. Always one of Xerox's strong points, the I/O capabilities of the 530 are good for a system of its size although not as extensive as the capabilities of larger members of the series. The I/O facilities function efficiently, especially in a process control or data acquisition application where the capabilities of the processor are directed almost exclusively toward I/O control.

A dual processor adapter (DPA) can connect two 530s (but not a 530 and a Sigma Series System) in master/master or master/slave relationships which are useful for back-up processors, front ends, and shared memory banks; DPA is not yet supported under BCM and RBM operating systems, however.

The priority interrupt system handles up to 40 unique hardware interrupt levels. Interrupts are divided into internal and external categories. The priorities are hardware defined and are sorted and identified by the CPU.

Xerox offers a useful standard maintenance feature on the 530, called Remote Assist, which allows the user to link into a Xerox maintenance office through a special Teletype interface built into the CPU. A Xerox Remote Assist specialist can link into the system through this interface to interrogate the fault system, run diagnostics, and even debug programs. Communication is over the common carrier dialup network.

The 530 is supported by two real-time operating systems, three FORTRAN compiler versions, a COBOL compiler, an RPG compiler, two assemblers, sort, a substantial set of users' aids, and a large library of engineering and scientific subroutines. All of the applications packages developed for the Sigma 3 will run on the 530.

The Xerox 530 was first delivered in August 1973.

COMPETITIVE POSITION

Although completely compatible with the Sigma 3, the Xerox 530 is an architecturally different computer. It uses extensive MSI/LSI technology, a microprogrammed CPU and a different memory. In addition, the 530 has features unavailable for the Sigma 3: remote assist, floating-point hardware, and field addressing. The floating-point hardware will increase throughput dramatically over that of Sigma 3 for many applications. Field addressing allows the programmer to manipulate bits and bytes around the constraints of word boundaries for table and string processing. The field addressing hardware also provides for storing and retrieving data in pushdown stacks.

Xerox has also improved the basic 530 hardware by standardizing many Sigma 3 options. These include the memory protect feature (for foreground/background processing), several internal interrupt levels, and a comprehensive fault detection and interpretation system. The internal fault detection system, which includes a multipurpose fault register, is substantially augmented by a standard communications link to a full-time, on-call Xerox Remote Assist specialist (maintenance technician) 24 hours a day. This provision allows the user to establish a Teletype land-line link directly into a Xerox office, where the specialist can communicate with the 530 (hardware and software) for remote diagnosis. The specialist can run diagnostics, interrogate the fault system, and even debug programs — all remotely.

Xerox has reduced the number of available interrupt levels from 116 (Sigma 3) to 40, has eliminated multiple memory ports, and has gone to an internal busing technique that utilizes a fairly elaborate cycle-stealing/priority memory accessing technique. The results of these changes are difficult to evaluate, especially within the context of what Xerox is trying to achieve for the 530. Obviously, fewer interrupt levels reduce the 530's process control capabilities, and less simultaneity affects the throughput rate, even with the shorter core memory cycle time (800 nanoseconds compared to 975 nanoseconds). But all this is not necessarily bad, because it does create a price versus capabilities balance that can be a bargain for the small to medium user. Furthermore, 40 interrupts are adequate for most applications.

The 530 is aimed at enlarging the market area filled by the Sigma 3, concurrent real-time and batch processing. The 530 offers the user a substantially better

price/performance ratio, as well as COBOL and RPG. The Sigma 3, on the other hand, is still available for those users who need a more elaborate interrupt structure and more simultaneity.

Strongest competition for the Xerox 530 will come from the Digital Equipment line, specifically the PDP-11/40 and 11/45. other competing systems include the Interdata Model 80, MODCOMP II, Varian Data Machines V70 Series, Prime 300, and Hewlett-Packard 21MX. All of these systems compete across a broad range of applications.

Although the Xerox 530 system is well designed and price competitive, it does not have elaborate memory management hardware like that available for the PDP-11/40 and 11/45, or the writable control store available with some of the other systems. Writable control store, however, has limited utility for most end users. On the other hand, memory management hardware supported by a good operating system should be an asset for real-time processing. It should be pointed out, however, that the 11/40 and 11/45 require memory management to address memory beyond 28K words, while the 530 does not. The Xerox 530 has a good structure for applications requiring extensive I/O.

One of the Xerox 530's strong points is its major operating system, the Real-Time Batch Monitor (RBM), which provides for real-time foreground processing, combined with background scientific or commercial processing. RBM supports ANSI FORTRAN IV, RPG, COBOL. Xerox has had considerable experience with the RBM software and its environment. The new features of the 530 and the COBOL compiler, combined with the overall system cost should make the 530 attractive for small to medium scale users. Of the major competitors, only Digital supplies COBOL.

Xerox also supplies a Satellite Processing Package allowing the system to submit jobs to any computer using IBM's "HASP" BSC multileaving protocol. This enables the user to send jobs and receive output from Xerox CP-V IBM HASP hosts, such as IBM 1130, 1800, 360/370, UCC COPE, and other 530 systems. Remote communications are concurrent with real-time and batch processing. These facilities allow the 530 to compete in the growing distributed processing market served by both intelligent terminals and small business systems with extensive communications capabilities. In this market, the 530 competes with companies like Four-Phase, Datapoint, MDS, and Sanders, who offer large terminal systems capable of a considerable amount of local processing, as well as with established small business suppliers like Basic Four and IBM (to some extent) who have popular business systems with extensive communications capabilities. Competition is also offered by major minicomputer manufacturers like Honeywell, Univac, Digital, and many others who have minicomputer systems with the hardware and software to function both as RJE terminals and business systems.

The 530 has also been adapted to attack the data entry market, with the Interactive Data Entry package (IDEN) allowing on-line data entry from up to 64 terminals. The Intelligent Display System package simulates an IBM 3790 entry system. These allow the 530 to compete in the growing market for multiterminal shared processor (disc-based) entry systems, with a number of companies devoted to this market, like Computer Machinery and Inforex, as well as major mainframe manufacturers like Honeywell.

User Reactions

Xerox 530 users interviewed for this report were very satisfied with both the system's performance and its reliability. All users reported excellent experiences with Xerox software support and maintenance service.

A Phoenix-based manufacturer of sounding rockets and satellites has three Xerox 530s, the first one installed a year ago. They chose the 530 to replace their IBM 1130 because of increased speed. One of the systems is used for normal data processing applications, while the other two are used to track rockets in a real-time situation. This company had two Xerox 530s operating on board a ship for several months and reports that the system performed admirably even under adverse conditions.

A school district uses the Xerox 530 as a remote batch terminal in conjunction with a Xerox Sigma 9. The system was chosen as part of a bid and is being used for student accounting, budgetary accounting, grade reporting, truant tracking, and other student processing applications. Sigma 9 software is being used successfully on the 530.

In an unusual application, one Xerox 530 is being used by a California fire department to dispatch fire apparatus to areas where it is needed most. The fire department has had the system for six months and has been very satisfied with it. According to the fire chief, none of the fire department members are computer-oriented, although two people are being sent to school to learn about the 530, so Xerox has provided excellent start-up and continuing support. The fire district plans to purchase two more systems to expand its capabilities.

A scientific research organization uses the Xerox 530 for process control. The company has four 530s and has had them for one year. Each system has a 65K-word memory and a 48-megabyte moving-head disc. The systems have paper tape, punched card, magnetic tape, and printers. The firm chose the 530 because it was compatible with the Sigma 2s and 3s they had used previously; and this firm's 530s have proved more reliable than the Sigma models.

CONFIGURATION GUIDE

The overall configuration of the 530 CPU, with its standard and maximum configurations and its general internal organization, is illustrated in Figure 1.

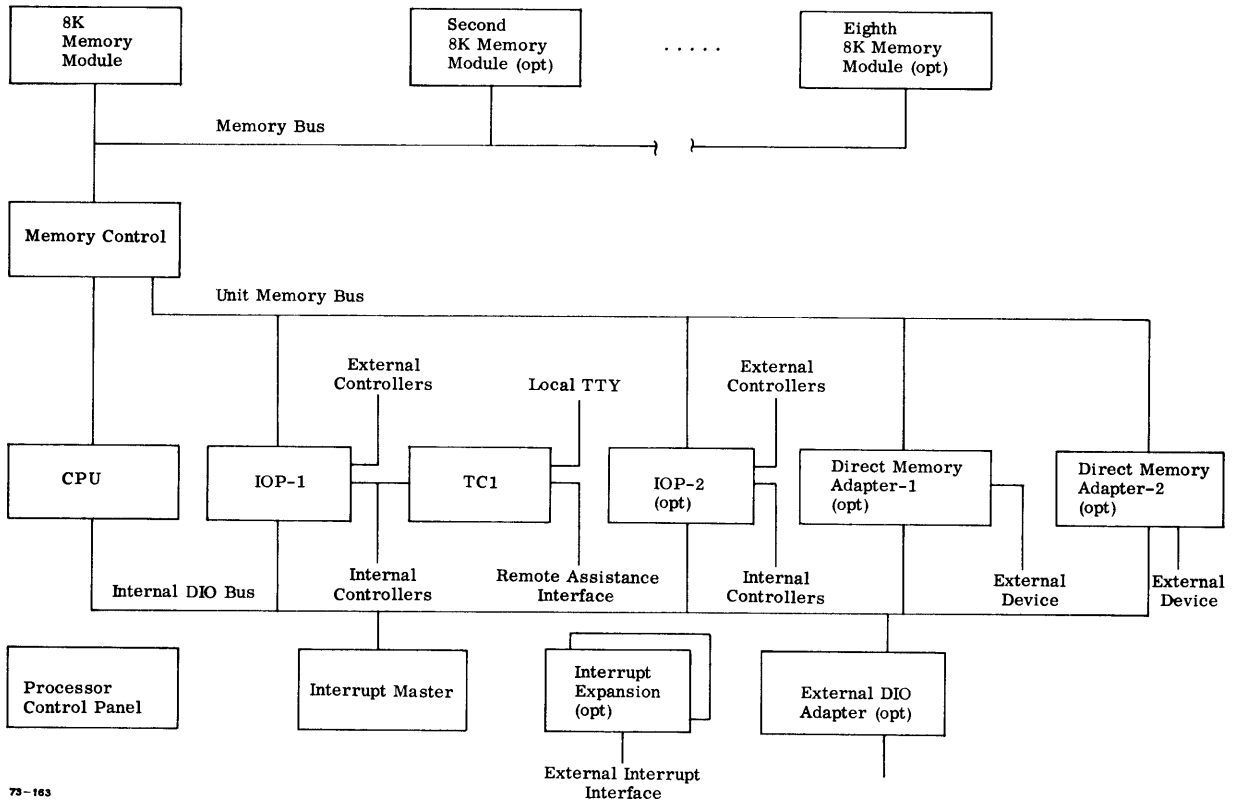


Figure 1. Xerox 530: Central System Block Diagram

Xerox sells the 530 in a basic 4101 configuration and in seven standard configurations that are considerably lower in price than the sum of the component prices.

The 4101 includes the CPU, one IOP (input/output processor) processor control panel, interrupt master, memory control, and 8K-word memory module. The IOP includes 16 I/O subchannels, and the CPU incorporates extended arithmetic (multiply/divide), two real-time clocks, fault interrupts, memory protect, power monitor, 10 internal and six external interrupt levels, and keyboard/printer control. A telecommunications controller, if included, interfaces to the IOP.

Optional features include: a second IOP with 12 subchannels, up to two direct memory access adapters, external DIO (direct input/output) adapter, up to seven additional memory modules of 8K words each (total 64K words), and Interrupt Expansion to 30 external levels. System options are available for floating-point arithmetic, field addressing, 2-byte interface on the standard or optional IOP, and dual processor adapter.

Xerox 530 mainframe characteristics are shown in Table 1.

The first eight channels of IOP-1 and the first four channels of IOP-2 can handle single- or multiunit controllers. All other channels are restricted to single-unit

Table 1. Xerox 530: Mainframe Characteristics

CENTRAL PROCESSOR	Xerox 530
Type (microprogrammed)	Yes
Control Memory	
Size	NA
Use	NA
No. of Internal Registers	8 general, 16 protection, 4 arithmetic/control
Addressing	
Direct	1,024 wds
Indirect	Forward/backward, 256 locations
Indexed	2 levels
Instruction Set	
Implementation	Hardware
Number	72 std, 10 opt
Decimal Arithmetic	No
Floating-Point Arithmetic	Yes
User Microprogramming	No
Priority Interrupt Levels	16 std; 28/40 opt
Main Storage	
Type	Core
Cycle Time (μsec)	0.8
Basic Addressable Unit	16-bit wd
Bytes/Access	2
Cache Memory	No
Min Capacity (wds)	8,192
Max Capacity (wds)	65,536
Increment Size (wds)	8,192
Ports/Module	1
Error Checks	Parity
Protection Method	Registers
Memory Management	No
ROM	No

controllers. Each multiunit channel can address up to eight controllers and up to 16 devices per controller. The theoretical device handling capacity of a Xerox 530 system with two IOPs is 144 devices. The two types of controllers cannot be mixed on a single channel.

The DIO interface can, again theoretically, address up to 65,536 separate devices through its 16-bit control word. Table 2 lists available peripheral devices.

Table 2. Xerox 530: Peripherals

Magnetic Disc. Rapid Access Data (RAD) files: capacities of 0.75, 1.5, or 3.0M bytes/storage unit; transfer rate of 188,000 bytes/sec; avg access time of 17 ms.
Removeable Disc: capacities from 24.5M to 196.6M bytes; transfer rate of 312,000 bps; avg access time of 87.5 ms.

Magnetic Tape (IBM-compatible). 7-track units (37.5 ips, transfer rates up to 20,800 bps); 9-track (75 ips, transfer rates up to 60,000 bps).

Punched Card. Reading speeds up to 200 or 400 cpm; punching speeds up to 100 cpm.

Line Printers (buffered). 310 to 1,100 lpm; up to 132 print positions; up to 91 char.

Keyboard/Printers (10 cps). Avail with paper tape reader (20 cps) and punch (10 cps).

Paper Tape. Reading speeds up to 300 cps; punching speeds up to 120 cps.

Graph Plotters. Digital incremental, drift-free plotting in 2 axes in up to 300 steps/sec at speeds from 30 millimeters to 3 ips.

Data Communications. Char-oriented and message-oriented equipment to connect remote user terminals via common carrier line, and local terminals directly.

Analog/Digital. Input/output controllers (analog and digital), IOP-DIO adapter, frequency controller, device subcontroller.

Obviously, the total device-handling capacity of the 530 can never be used completely; however, the I/O interfaces are significant indications of the multipurpose design of the 530 system architecture. Normal business/scientific data processing is supported by the IOPs and, to some extent, the DMAs. Large-scale data base manipulation and swapping require the high-speed bulk data transfer capability given by the DMAs. The DIO interface is naturally suited for process control operations.

The remaining seven standard configurations offered by Xerox are: 41C1 Paper Tape System; 41C2 Paper Tape and Card System; 41C3 Paper Tape, Card, and Printer System; 41C4 Card System; 41C5 Card and Printer System; 41C6 Card, Printer, and Magtape System; and 41C7 Card, Printer, and Magtape System (two drives).

The Xerox Interactive Data Entry Network (IDEN) for distributed processing, which runs under RBM, requires 32K words of memory, a disc, communications controller, magnetic tape unit, network of CRTs, and keyboard/printer.

The Xerox Satellite Processor package runs under RBM or BCM. Thus, it requires a configuration to support the operating system. The RBM with Satellite Processor requires ACPU, 16K words of memory, Teletype KSR 33, Disc (0.75M-byte capacity), card reader, and procedure-oriented communications controller. The BCM version requires only 8K words of memory and does not require the disc. Otherwise, the configuration is the same as for RBM.

Several processor features are interesting. Field addressing, for example, allows the processor to address up to 16 bits without regard to internal word boundaries. This useful bit and byte manipulation feature gives the 530 the ability to construct pushdown stacks and to operate on tables and strings.

External priority interrupts are expanded in two increments of 12 levels each to a maximum of 40 interrupt levels.

The Model 4185 Dual Processor Adapter (DPA) is an option that requires some changes to the CPU backplane. The changes are standard to all processors manufactured after April 1, 1974. Configurations can be either master/master or master/slave. Masters attach the DPA to communicate with DMA on a slave. Slaves can become masters by adding a DPA unit to the slave to connect to the other processor's DMA channel. A total of 64K words of memory can be addressed by either processor. All combinations of memory arrangements are possible, as long as each processor has a minimum of 8K words: 8K in the master, and 56K in the slave, 48K in the master and 16K in the slave, 32K in each, and so on.

In addition to an extensive line of standard peripherals, Xerox offers impressive analog/digital and data communication subsystems. A 530 with a fully expanded I/O system can interface to 144 peripheral devices. Most of the standard peripherals available for the rest of the Sigma line can interface to the 530. The configurations required for BCM and RBM and their supporting software are shown in Table 3.

COMPATIBILITY

The 530 is completely compatible with the Sigma 3. Unlike the Sigma 3, however, the 530 cannot share common memory with other Sigma computers or with the 550 and 560, which reduces its usefulness as a front-end processor for the larger Sigma computers. Xerox manages a reasonable degree of compatibility between the 16-bit 530 and the 32-bit 550 and 560 and Sigma

Table 3. Xerox 530: Software Systems

SOFTWARE	SYSTEM RBM(1)	BCM(2)
FORTRAN COMPILERS		
ANS FORTRAN IV	X	–
BASIC FORTRAN IV	X	–
BASIC FORTRAN	–	X
ASSEMBLERS		
Extended Symbol	X	–
Symbol	X	X
SCIENTIFIC SUBROUTINES	X	X
COMMERCIAL		
RPG Compiler	X	–
Sort	X	–
PHSORT (FORTRAN callable) Commercial Subset(3)	X	–
COBOL Compiler	X	–
IBM 1130 CONVERSION KIT	–	–
USER SYSTEM AIDS	X	X
Real-Time Debug	X	–
RAD Editor	X	–
Debug	X	X
Math Library	X	X
Concordance	X	X
Media Copy	X	X
Source Text Editor	X	X
Absolute Loader	X	X
Relocatable Loader	X	X
Plotter Handler*	X	X
RAD Handler	X	–
COC Handler	X	–
SIU Handler*	X	–
Applications Packages		
Satellite Processor	X	X
Interactive Data Entry Network (IDEN)	X	–
Civil Engineering Coordinate Geometry (COGO)	X	X
Structural Engineering System Salver (STRESS)	X	X
Heating Ventilation and Air Conditioning (HCC III) Design System	X	X
Project Control System (PCS)	X	X
UCLA Biomedical Statistical Package (BMD)	X	X
Event Oriented Simulation (GASP II)	X	X
Continuous System Simulator (CSS/3)	X	X

Notes:
(1) RBM requires 16K memory, 750K wds of RAD auxiliary storage, a RAD controller, a keyboard printer with paper tape reader/punch, and 1 interrupt level.
(2) BCM requires 8K memory, a Teletype unit, and 1 interrupt level.
(3) Available through the Xerox Users' Group Library.

Series computers through a byte-oriented interface. The source or destination computer is responsible for word assembly or partitioning to establish format consistency. The 530 can operate in a distributed processing system as an interactive remote data entry terminal communicating with a host computer such as Sigma 6 or 9, Xerox 560, or IBM Systems 360/370 via HASP BISYNC multileaving protocol.

MAINTENANCE AND SUPPORT

Xerox supplies standard maintenance and support contracts via 13 district sales and service offices and three around-the-clock remote assist centers. The 13 district offices have full spare parts inventory and are staffed by both software and system engineers. On-site maintenance contracts are available for large remote sites.

HEADQUARTERS

XEROX Corporation
701 S. Aviation Boulevard
El Segundo CA 90245

PRICE DATA

Model Number	Description	Monthly Rental $[1]	Purchase $	Monthly Maint. $
	CENTRAL PROCESSOR AND WORKING STORAGE			
	Xerox 530 Processor			
4101	Central Processor (includes first IOP with 16 I/O char, 2 real-time clocks, memory protect, power monitor, 6 levels of external interrupt, first keyboard/printer control and 8,192 wds core memory)	700	20,000	150
	Processor Options			
4105	2-Byte Interface for First IOP	50	1,500	15
4118	Floating-Point Arithmetic	167	3,500	35
4119	Field Addressing Instruction	50	1,500	15
4125	Priority Interrupt (12 levels)	20	600	5
4151	Core Memory Expansion (8,192 wds)	300	5,500	45
4170	External Interface Feature	14	400	5
4171	Second IOP with 12 I/O Channels	167	5,000	35
4175	2-Byte Interface for Second IOP (requires 4171)	50	1,500	15
4180	Direct Memory Adapter	40	1,200	10
4190	Second Keyboard/Printer Control	14	400	5
4191	Keyboard/Printer-KSR35 (requires 4101 or 4190)	110	3,300	15
4192	Keyboard/Printer-ASR35 (requires 4101 or 4190)	165	5,000	15
4193	Keyboard/Printer-KSR33 (requires 4101 or 4190)	45	1,300	15
4194	Keyboard/Printer-ASR33 (requires 4101 or 4190)	60	1,700	15
	MASS STORAGE			
7201	Rapid Access Data (RAD) Storage Controller (for 7202, 7203, and 7204 RAD units)	200	8,000	36
7202	RAD Storage Unit (0.75 Mb; 188 kb/sec transfer rate; requires 7201)	325	13,000	95
7211	RAD Controller	398	18,000	52
7212	RAD Storage Unit, 5.3 + MB	1,235	60,000	265
7240	Removable Disc Controller	500	20,000	104
7241	Extended Width Interface Feature (for 7240; 2 or 4 bytes)	63	2,500	16
7242	Removable Disc Dual Spindle Storage Unit (24.5M words; 156K word/sec transfer rate; requires 7240)	800	25,000	281
7243	Device Pooling Feature (for 7242)	200	8,000	52
7244	Disc Pack (for 7242 or 7246)	31	600	NC
7246	Removable Disc Single Spindle Storage Unit (12.2M words; 156K word/sec transfer rate; requires 7240)	450	15,000	212
7250	Cartridge Disc Control (requires IOP)	200	8,000	35
7251	Cartridge Disc, 2.3Mb (requires 7250)	140	5,500	50
7252	Cartridge Disc, 4.6Mb (requires 7250)	225	9,000	75
	Paper Tape			
7060	7062 Reader, 7063 Punch, 7064 Spooler with 7061 Controller and Rack (requires IOP)	200	11,000	90
7062	Reader (300 cps; requires 7061)	50	2,000	16
7063	Punch (120 cps; requires 7061)	63	2,500	27
7064	Spooler	38	1,500	11
	Punched Card			
7121	Reader (200 cpm)	220	7,500	55
7122	Reader (400 cpm)	400	12,000	127
7165	Punch (100 cpm)	490	19,600	140
	Buffered Line Printer			
3451	350 lpm, 64-Char Set	500	22,000	250
7441	1,100 lpm, 64-Char Set	1,150	46,000	292
7442	1,100 lpm, 91-Char Set	1,250	50,000	292
	Magnetic Tape			
7315	Mag Tape Controller (with 1 7316 drive; requires IOP); Max 1 Controller/CPU	600	16,000	200
7316	Add-On Tape Drive; Max Drives/Controller (requires 7315)	450	12,000	180
7361	Mag Tape Controller (for 7362)	150	6,000	42
7362	Mag Tape Unit (37.5 ips, 556 bpi)	475	19,000	133
	Display Equipment			
7530	11-In. Graph Plotter	325	13,000	80
7531	30-In. Graph Plotter	550	22,000	106
7601	Data Set Controller	175	7,000	36
7602	Full-Duplex Feature (requires 7601)	20	800	NC
7603	Automatic Dialing Feature (requires 7601)	20	800	NC
7604	Local Batch Terminal Controller	210	8,400	36
7605	Procedure-Oriented Data Set Controller (requires IOP)	230	9,500	50
7611	Communications Controller	253	10,500	47

Note:
(1) Rental prices are based on a 1-year lease.
NC No Charge.

(Please refer to report number S962.011.300 for general coverage of the Xerox 530 including OVERVIEW, COMPETITIVE POSITION, USER REACTIONS, CONFIGURATION GUIDE.)

MAINFRAME

The Xerox 530 mainframe is a modular design that can be modified to match a changing workload. It can handle real-time and general-purpose assignments concurrently. The system monitor with memory protect registers controls all multiprogramming tasks. Foreground real-time programs are scheduled by the interrupt hardware; background programs are scheduled by the system monitor. The number of interrupt-driven programs is limited to approximately 30 by the hardware interrupt system. Software can extend this number considerably.

Central Processor

The same CPU is used for all 530 configurations. It is a single-address, sequential, binary processor. The CPU includes an arithmetic and control unit consisting of arithmetic/logic circuits, microprogramming control circuits, and four 16-bit internal registers, eight 16-bit general registers, and sixteen 16-bit system protection registers (memory protect).

Data Structure

A word is 16 bits long. Two parity bits, one per byte, are added to each word in core storage. Data for all fixed-point arithmetic operations is represented by 15 data bits and one sign bit. Double-precision operands are two words long. Positive numbers are in true binary form; the sign bit is 0. Negative numbers are in two's-complement form; the sign bit is 1. Alphanumeric data in the computer can be handled in variable length strings of 8-bit bytes or 4-bit decimal digits. The standard internal data code is EDCDIC. All code translations and radix conversions are handled by standard Xerox subroutines. Floating-point operands are three words long: 16-bit exponent and 32-bit fraction.

All instructions are one word long, except field addressing instructions, which are two words long.

The basic addressable unit of RAD (rapid access data) storage is a sector of 360 bytes; the sector for a disc pack is 1,024 bytes.

Registers

The eight general registers are as follows: program address register (P); zero source register (Z); link address register for reentrant subroutines (L); temporary storage register (T); index register 1 (X); index register 2, used as base register (B); accumulator (A); and extended accumulator for multiple-precision operands (E).

The CPU also contains sixteen 16-bit memory protect registers. Each bit of each register protects one 256-word block of core storage. A specified protect register is loaded from the accumulator. If an unprotected instruction attempts to alter the contents of a protected core location, an interrupt is generated.

In addition, the CPU has one pair of registers for each I/O channel. Instructions that supply control information for the I/O interface and subsystem address the I/O channel registers.

The four 16-bit registers in the arithmetic and control portion of the processor are: a memory address (MA) register, a memory buffer read (MBR) register, a memory buffer write (MBW) register, and a working (W) register. The MA, MBR, and MBW registers are used to access main memory and to provide temporary storage for data in transit to or from memory. The W register is not accessible to the program; it is used as intermediate storage when developing effective addresses or instructions. Its contents can be displayed on the control panel.

A CPU fault system monitors internal operation and stores any abnormal conditions in a fault register. The fault system can be interrogated (by instruction) to copy the contents of 16 fault registers into a register. The fault register is reset when copied.

Units that can be identified by the fault register are: CPU, special system, IOP-1, IOP-2, interrupt master or external DIO system, or DMA channel. Up to 32 different fault conditions can theoretically be identified for each unit. Actually, 19 different faults are identified for the CPU; less are identified for the other units.

Instruction Set

The instruction set provides direct data transfer between the main memory, the accumulator, and index register 1. An instruction subset, referred to as a copy instruction, provides 18 instructions for register-to-register operations. Singleword multiply/divide instructions are standard. (Seven doubleword instructions, including add and subtract, are also standard.)

The Read Direct (RD) and Write Direct (WD) instructions are privileged and can be executed only if accessed from protected core locations. An instruction from protected core can be executed following an instruction from unprotected core only in response to an interrupt.

The general instruction types and typical execution times are shown in Table 1.

The time required for the 530 to perform an instruction is the sum of the preparation and execution times. The maximum preparation time is 0.800 microsecond.

Table 1. Xerox 530 System: Instruction Execution Timings

Instruction	Time (msec)
Add/Subtract	
Single Precision	1.92
Double Precision	4.00
Multiply (single precision)	8.00
Divide (single precision)	12.12
Load/Store	
Single Precision	1.92/2.20
Multiple Precision	4.64 - 8.48/5.28 - 8.32
Floating Add/Subtract	8.80
Floating Multiply	32.96
Floating Divide	77.56
AND	
OR (inclusive or exclusive)	1.92
	0.96
Branch	0.8 to 1.92
Shift	2.56 + 0.32N
Direct Control	3.84-4.16
I/O Internal	5.44-11.20
Copy (register-to-register)	0.96-1.76
Interrupt Acknowledge	8.96-14.72
Interrupt Exit	11.52-15.46

Addressing Facilities

The 530 memory referencing instruction format provides a 4-bit operation code, a 3- or 4-bit modification field, and an 8- or 9-bit displacement. The displacement field limits direct addressing to the first 256 words of memory, but the address modification field provides the following additional addressing capability: indirect addressing to one level, relative addressing, preindexing, and postindexing.

All of the address modification techniques can be used singly or in combination to provide a highly flexible means for deriving an effective address with a limited instruction word size. Because the 530 generates a 16-bit effective address, it can address 64K words of memory.

Field Addressing. Field addressing instructions can address any contiguous group of bits without regard to word boundaries. The field can be one to 16 bits long.

Interrupt Control

The priority interrupt system can handle up to 40 interrupt levels (16 standard, 24 optional). Standard interrupts consist of 10 internal and six external interrupts. The 24 optional interrupts are external. Interrupt priority is fixed by hardware.

The interrupts have the following order in priority:

- Power on.
- Power off.
- Counter 2 (real-time clock).
- Counter 1 (real-time clock).
- Machine fault.
- Protection violation.
- Integral external interrupt level 5.
- Integral external interrupt level 6.
- I/O.
- Control panel.
- Counter 2 = 0.
- Counter 1 = 0.
- Integral external interrupt level 1.
- Integral external interrupt level 4.
- External interrupts (first 12).
- External interrupts (second 12).

In addition to being individually enabled or disabled under program control, an interrupt level can be in the armed, disarmed, waiting, or active mode. A disarmed interrupt level neither recognizes nor remembers an interrupt condition. An armed interrupt recognizes an interrupt condition and remembers the condition by advancing to the waiting state. An instruction is available to enable/disable interrupt groups under program control. A 3-bit code in the effective address word specifies various combinations of arm/disarm and enable/disable interrupt levels. The contents of the accumulator determine which interrupt levels within the specified interrupt group are to be enabled/disabled. Power on/off, machine fault, and protection violation interrupt levels cannot be altered by a WD instruction. The counter 1 and 2 levels are partially restricted.

The status of all interrupt levels except the power on/off interrupts can be interrogated by instruction.

A separate core location for each interrupt level contains the address to which control is transferred after the processor acknowledges an interrupt. Another interrupt cannot be recognized until after the initial instruction of the interrupt servicing routine is executed. If the routine is interrupted, it is treated in the same way as an interrupted program. Any number of interrupt routines can thus be stacked, implying a fifth interrupt state in the servicing sequence. At the end of an interrupt servicing routine, an exit sequence references the program status doubleword to restore the original program status.

MAIN MEMORY

Up to seven optional 8K memory modules can be added to the standard 8K module for a total main memory capacity of 65,536 16-bit words. Multiprocessor configurations can support larger memories, but only 65,536 words can be common to both processors.

Cycle time is 800 nanoseconds per word. Using straight line coding, the effective internal transfer rate is about 243,000 words per second with direct addressing, and about 175,000 words per second with indirect addressing. Using a programmed loop, the effective rate is 146,000 words per second with indirect addressing. Peak transfer rate is 1,250,000 words per second.

All of the memory modules are linked through a common bus that connects to the memory control unit. The memory control unit is accessed in two ways: directly from the CPU or through a unit memory bus. The

unit memory bus links the IOPs (Input Output Processors) and the DMA (Direct Memory Access) units. The optional DIO (Direct Input Output) adapter effectively uses both the unit memory bus and the CPU port, but it is operationally buffered. There are no provisions in the 530 for multiple memory ports.

Each word of core storage contains 16 data bits and two parity bits. Parity is checked on both read and write. Parity error indicators are incorporated into the general machine fault interrupt.

The memory is divided into 256-word blocks for protection by as many as 16 protection registers of 16 bits each. Each bit of a register is uniquely assigned to protect one related block of memory. When a protect bit is set, the corresponding block cannot be altered or entered by a program residing in unprotected memory. There is no protection against reading.

Sixty-four core locations are reserved for program loaders. Up to 38 locations are reserved for interrupt-servicing entry points.

Auxiliary storage is provided by random access data storage units or disc storage units.

I/O CONTROL

The I/O system of the standard 530 consists of one 16-channel byte-oriented I/O processor (IOP-1). The IOP has an external and an internal interface. An optional 2-byte interface feature is offered to adapt the external interface to 16-bit word transfers. A fully expanded (all I/O options exercised) 530 system contains a mixed media of byte- and word-oriented interface units. A second 12-channel IOP (IOP-2) can be added to increase the total capacity to 28 I/O channels. Two word-oriented, single-channel, DMAs can be added for high-speed block data transfers. Through a DIO Adapter, a DIO interface can also be installed.

Except for the DIO interface, all other operations are controlled by I/O Control Doublewords (IOCDs); the operations are stored in dedicated channel registers by the CPU before I/O operations. Operations that require more than one IOCD automatically cause additional IOCDs to be fetched from a table in main memory. The IOCDs specify all necessary control/response patterns that are required by the applicable Xerox peripheral devices.

The maximum IOP data transfer rate is 640,000 bytes per second through the internal interface, and 543,000 bytes per second through the external interface with the optional 2-byte interface feature.

The DMA interface can handle a peak transfer rate of 850,000 bytes per second.

Special I/O Functions

A standard independent telecommunications interface permits the user to link to a Xerox remote-assist specialist through a teletypewriter terminal.

A Dual Processor Adapter (DPA) is available for two processors to share a common memory in a master/slave or master/master relationship. The facility is provided primarily for system backup in situations when the system cannot be allowed to go down. Registers in the adapter can be loaded by the master to define the shared memory locations. At least 8K words are private to each processor. Each processor can address a maximum of 64K words of memory.

PERIPHERALS

Xerox provides a variety of peripherals for the 530: conventional low-speed devices, high-speed mass storage units, and special-purpose items. All standard peripherals connect to the system through the byte-oriented interface. The basic I/O code for all units is EBCDIC.

KEYBOARD/PRINTER

A variety of keyboard/printers is available; one of the following is required per system:

4193 Keyboard/Printer (KSR 33) — 10 cps.

4194 Keyboard/Printer (ASR 33) — 10 cps with paper tapes.

4191 Keyboard/Printer (KSR 35) — 10 cps reader and punch.

4192 Keyboard/Printer (ASR 35) — 10 cps with paper tape reader and punch.

PAPER TAPE

7060 Paper Tape Punch/Reader Spooler, Controller — reads 300 cps; punches 120 cps.

7062 Paper Tape Reader — 300 cps; requires 706/controller.

7063 Paper Tape Punch — 120 cps; requires 7061 controller.

7064 Spooler — 1,000 ft tape capacity.

PUNCHED CARD

7121 Card Reader — 200 cpm; 300-card stacker; 300-card hopper.

7122 Card Reader — 400 cpm; 1,000-card stacker; 1,400-card hopper; cards can be read in EBCDIC or binary mode; validity check in EBCDIC only; cards can be punched in EBCDIC or binary code.

7165 Card Punch — 100 cpm w/300-cpm fast skip; 1,000-card stacker w/offset feature; 1,000-card hopper; cards can be read in EBCDIC or binary mode; validity check in EBCDIC only; cards can be punched in EBCDIC or binary code.

LINE PRINTER

3451 Buffered Line Printer — 350 lpm; 64-char font; 32-col.

7441/7442 Buffered Line Printer — 1,100 lpm; 64/91-char font; 32-col.

MAGNETIC TAPE UNIT

All are IBM-compatible tapes.

7322 Magnetic Tape Unit — 9-channel; 60,000

bps peak; 75 ips; 800 bpi; requires 7321 controller which handles up to 8 drives.

7323 Magnetic Tape Unit — 9-channel; 120,000 bps peak; 150 ips; 800 bpi; requires 7321 controller which handles up to 8 drives.

7316 Magnetic Tape Unit — 9-channel; 60,000 bps peak; 75 ips; 800 bpi; requires 7315 controller which handles 2 drives.

7362 Magnetic Tape Unit — 7-channels; 15,637 bps peak in binary-packed mode; 20,850 bps peak in BCD or binary-unpacked mode; 37.5 ips; 556 bpi; requires 7361 controller which handles 2 drives.

DISC STORAGE

7202/7203/7204 RAD Storage Units — fixed head 0.75/1.5M/3M bytes; 187.5K byte/second peak transfer rate; 17-msec access time; requires 7201 controller which can handle up to 8 drives.

7242/46 Disc Storage Unit (disc pack) — dual/single spindle; 49M/25M-byte capacity; 312.5K byte/second peak transfer rate; 12.5-msec latency; 75-msec avg head positioning time; requires 7240 controller which handles up to 4 drives.

7251/7252 Cartridge Disc Storage Unit — 2.3M/4.6M-byte capacity; 312.5K-bps peak transfer rate; requires 7250 controller which handles up to 4 drives.

Special Peripherals

Xerox provides a number of analog/digital subsystems that connect to either a channel of a byte-oriented IOP or to the optional DIO interface channel. These devices, along with two graph plotters, constitute the special-purpose peripheral complement as follows:

7916 Analog Input Controller — connects to IOP channel; can control up to 1,024 lines; max rate 100K conversions/second.

7910 Analog Output Controller — connects to an IOP channel; D/A converter channels; can control up to 256-bit converters; max rate: 100,000 conversions/second.

7929 IOP-DIO Adapter — converts any IOP channel to a DIO channel; thus devices normally connected to DIO can use an IOP channel; transfer rate of 70,000/110,000 operations per second.

7935 Digital Input/Output Controller — 8-bit bidirectional channel, transfer rates of 30K to 50K words/sec; connects to DIO interface.

7900 Device Subcontroller — provides std interface for user-supplied devices.

7530/7531 Graph Plotter (11/30-in.) — length 120 feet, incremental plotting speed of 200 to 300 steps/second.

DATA COMMUNICATIONS

Both character-oriented and message-oriented data communications equipment can be used with the 530 computer. Software is also available to support the two types of communications equipment.

Model 7611 Character-Oriented Communications Controller is the central element in the character-oriented communications subsystem; up to 16 can be attached per 530 system; and each requires one IOP channel, the optional DIO interface, and two priority interrupt levels. The 7611 contains one integral line interface unit and can accommodate up to seven additional units; each line interface unit can accommodate eight terminals that operate in simplex, half-duplex, full-duplex, or any combination of modes. All send and receive modules are functionally independent in the system. The controller provides the central source of timing and control for the communications subsystem.

A 530 can control 128 high-speed lines (eight lines per controller, up to 16 controllers), and 896 low-speed lines (up to 56 lines per controller, up to 16 controllers), or 1,024 low-speed lines (up to 64 lines per controller, up to 16 controllers). Table 2 lists the transmission groups.

Table 2. Xerox 530 System: Character-Oriented Transmission Format Groups

Formatted S/R Modules (Levels/Units)	Matching Timing Modules (char/sec)	(bits/sec)	Speed Range	Typical Terminal Devices
5/7.5	6.0	45	Low	Teletype, Models 28 & 32
	6.6	49.5	Low	Teletype, Models 28 & 32
	7.5	56.25	Low	Teletype, Models 28 & 32
	10.0	75	Low	Teletype, Models 28 & 32
7/9	14.8	133.2	Low	IBM 1050 or 2741
8/11	10.0	110	Low	Teletype, Models 33 & 35
8/10	15.0	150	Low	Teletype, Model 37
	30.0	300	Low	Special systems
	30.0	300	High	Special systems
	60.0	60	High	Special systems
	120.0	1200	High	Special systems
	180.0	1800	High	Special systems
	240.0	2400	High	Special systems

All data is transmitted from the 530 computer to the communications controller through the optional DIO interface; the data is sent to the 530 computer through IOP-1 or IOP-2. For every output, the central processor must identify the line requesting service and send out the appropriate character. The automatic nature of the IOPs allows received characters to be stored in memory without processor intervention. Data from the lines connected to a controller are interlaced in memory, and a program must de-multiplex the data. Two bytes are stored in memory for each character that is received; one byte contains the line address, and the other contains data. Xerox also provides an interface to telegraph lines for simplex, half-duplex, and full-duplex service, and a controller for automatically dialing Bell System 800 Series auxiliary data sets.

Model 7601 Data Set Controller and Format Unit is the central functional element in a message-oriented communications subsystem. Every data set controller consists of control circuits and one format unit. Each format unit contains a separate bit serializer for input and output. The data set controller interfaces with the 530 through the

IOPs and requires one I/O channel for half-duplex operation and two channels for full-duplex operation.

A single data set controller can control one data set that operates in half-duplex mode. A full-duplex option is provided to extend control for a data set that operates in full-duplex mode.

Data is transmitted between the computer and the data set controller in 8-bit bytes. The character transmitted to and/from the data set controller can consist of from one to eight bits as selected by the computer program. Transmission formats available for use with the Model 7601 are summarized in Table 3.

An automatic dialing option is available for the Model 7601 equipment.

The 7605 Procedure-Oriented Data Set Controller is a 7601 with additional facilities to handle communications using a foreign protocol, such as BSC.

Table 3. Xerox 530 System: Message-Oriented Transmission Formats

Type	Format	Transmission Rate
S	2- to 8-level, under program control	Up to 230,400 bps*
A	5-level	60 wpm
A	5-level	66 wpm
A	5-level	75 wpm
A	7-level	148 wpm
A	8-level	100 wpm
A	8-level	150 wpm

A – Asynchronous
S – Synchronous
* – Timing provided by dataset

SOFTWARE

Xerox provides a large set of software for the 530. The software package is supplemented by the packages offered with the Xerox Sigma 3, because the systems are compatible. Software enhancements in the 530 system permit addition of the field addressing option, the Remote Assist feature, the floating-point arithmetic hardware, and the comprehensive fault detection and analysis system in addition to Sigma 3 facilities. A variety of communications and specific 530 applications programs have also been developed.

Operating Systems

Operation is integrated through the use of an operating system: Basic Control Monitor (BCM) or Real-Time Batch Monitor (RBM).

BCM. BCM requires an 8K-word memory, a Teletype unit, and one interrupt level. The BCM has been designed for configurations that do not include RAD or disc pack storage. General BCM features and capabilities are summarized as follows:

- Real-time processes are directly interfaced with the BCM.
- It performs and controls all privileged functions for the background including I/O, interrupts, and memory protection.
- User I/O functions are initiated by I/O calls to the monitor.
- Foreground facilities are dedicated to the real-time process.
- Full I/O buffering is available.
- Complete memory protection is provided for the operating system and the foreground process. Operator communication facilities are available at all times.
- There is provision for program simulation of unimplemented hardware options.
- Background programs are run when storage and processor time are left over from the real-time process.
- Background tasks can be run sequentially because of the self-initialization of the various language processors.
- Core storage requirements are minimized since the BCM calls for only those utility routines that are required for the current foreground and background tasks.

BCM provides concurrent multiusage on a minimum hardware configuration. Real-time foreground processes are loaded from the background stack. The BCM, with its foreground and essential service routines, is loaded into core memory; from the core memory, the BCM establishes protection control and creates the environment for multiusage operations.

An operator can control all background processing via the console keyboard. The keyboard can also be used to communicate with the foreground process. Conflicts between the foreground and background processes are minimized because all requisite machine facilities are automatically assigned to the foreground task by the direct assignment of priority interrupts to the foreground process. BCM recognizes the priority of the foreground task I/O and interrupt processing.

A background task can be loaded from the card reader or paper tape reader by typing the appropriate control characters from the keyboard, or by using control cards. The BCM allocates storage within the available memory. Legality checks are made to ensure that the operating system and real-time tasks are protected.

Besides their I/O interfaces with the BCM, the background processors act as stand-alone processors that

operate in the available background space. In general, the background processors reinitialize themselves upon completion of a task, and begin to process the next task that waits in the peripheral input device. Sequential production jobs, such as assemblies or compilations, can be performed simply with minimal operator intervention. BCM can include additional I/O handlers, larger memories, and additional functional modules from the RBM. BCM is upward compatible with RBM.

RBM. The RBM is a self-contained system that can generate a specific operating system for a particular application. The RBM is built in two phases, SYSGEN and SYSLOAD. SYSGEN selects the particular options and peripheral devices for a system, allocates RAD storage areas, and optionally produces a rebootable version on cards, paper tape, or magnetic tape. SYSLOAD is an initialization phase. SYSLOAD writes RBM, RBM overlays, and the RBM symbol table on RAD and stores information in the RAD bootstrap to load RBM from RAD. Once built, RBM is not regenerated unless system requirements change.

RBM can handle up to 30 real-time tasks in the foreground concurrently with one background task. A task is a group of operations that can be performed independently of all other tasks; tasks are not reentrant. Both monitor and user real-time tasks are interrupt driven. Each task is associated with only one hardware interrupt, and operates at the priority level of its related hardware interrupt. A task can call another task only through the interrupt system.

The lowest-priority hardware interrupt is associated with the RBM Control Task; this control task controls all communication with the operator and all background batch processing. The control task also performs all subtasks on a software priority basis.

The background task is not associated with a hardware interrupt, but operates as if it were associated with an interrupt level that is below all hardware interrupt levels.

RBM provides a group of reentrant monitor service routines that can be used by any task in the system. The service routine operates at the priority level of the task that requests the service.

The monitor provides the following primary services to foreground tasks:

- Responds to I/O interrupts.
- Responds to an operator's request made via the console.
- Supervises the file activities on RAD.
- Supplies software floating-point arithmetic if configuration has no floating-point hardware.
- Loads a foreground program from RAD on request.
- Provides foreground tasks with standard system constants such as pointers to current floating-point accumulator, current task reentrant temporary stack, and IOCS table.
- Provides a 63-word "mailbox" to pass information among foreground tasks.

RBM provides a set of routines called,the Job Control Processor, for background tasks. These routines provide facilities for controlling a background processor, loading, initializing, executing, checkpointing, and restarting. The Job Control Processor has three main parts: control task, subtasks, and control command interpreter.

All foreground tasks are executed in protected memory, and their associated peripheral devices are protected. Background tasks operate in unprotected memory except for the special case of the command interpreter, which operates as a background task in protected memory. Foreground tasks can issue I/O commands directly because their peripheral devices can be dedicated (or they can be shared with background programs). Background tasks issue I/O commands through the monitor, which checks to determine whether the I/O operation violates the integrity of a foreground task.

Background processors available under RBM are the Extended Symbol assembler, which can assemble programs written in either Symbol or Extended Symbol, BASIC or ANSI FORTRAN IV, RPG, and Sort. RBM can perform background job accounting, maintain a log of background jobs, and provide watchdog services on background execution time. A debug program is also available for background jobs.

Service programs include an overlay loader, RAD editor, utility subsystem, and concordance.

RBM divides core into five major areas: resident RBM, public library, resident foreground, nonresident foreground, and background. If a nonresident foreground program that requires more than the allotted core area for execution is called, the background task is checkpointed and rolled out to RAD. The background area is then released to allow expansion of the nonresident foreground core area for loading and executing the foreground programs. After its execution, RBM returns the nonresident foreground core area to normal, reloads the background program, and continues its execution.

RBM uses RAD for the main control storage medium. As such, RAD stores RBM and its related processors. In addition, it provides both permanent and temporary storage for user programs and data.

The most important unit of RAD storage is a file, which is a contiguous area that is treated as a unit on RAD. Files can be blocked or unblocked. I/O for blocked files is done in terms of blocks; block size is determined at SYSGEN time. I/O for unblocked files is executed in terms of logical records.

A master directory, for functional RAD areas, is core resident; four words are required per file. In addition,

the permanent RAD functional areas have file directories to their contents; this directory must be read into core before a permanent RAD file can be loaded. Temporary files do not have directories to their contents other than the master directory in core. Permanent files can be created or changed only by the RAD editor. Temporary files can be created and defined, or closed and deleted, by simple command statements.

RBM requires a 530 processor with 16K words of memory, a keyboard printer with paper tape reader/punch, a RAD controller, and 0.75 million bytes of RAD storage. A disc pack controller and disc pack can be used instead of RAD storage.

RBM can support any of the following units: disc packs, additional core memory, keyboard/printer, high-speed paper tape reader/punch, card reader, card punch, RAD units, 7-track or 9-track magnetic tape with BCD and binary packing option for 7-track tape, line printer, plotters, and character-oriented and message-oriented communications devices.

Other devices can be added to the system, but RBM supplies only generalized support for them.

RBM also supports the Remote Assist, fault register, and error logging features of the 530.

Language Processors

Two assemblers, Symbol and Extended Symbol, are available for the 530. Symbol is the basic assembler, and can be used on a minimum configuration with the three software systems. Extended Symbol is a superset of Symbol, which is used only with RBM.

There are four compilers: Xerox Basic FORTRAN, Xerox Basic FORTRAN IV, Xerox ANS FORTRAN IV, COBOL, and RPG. Basic FORTRAN is an extended implementation of USASI Basic FORTRAN X3.10-1966. Basic FORTRAN IV is an extended implementation of Basic FORTRAN and is, essentially, a subset of USASI Standard FORTRAN. ANS FORTRAN IV exceeds the standards set by ANSI X3.9-166. COBOL is a subset of proposed ANSI X3.23-1973.

Xerox Basic FORTRAN is used with BCM. It includes USASI Basic FORTRAN as a subset and accepts directly most programs written in IBM Operating System/360 FORTRAN IV (E-level subset). In addition, Xerox Basic FORTRAN will accept, with slight modification, programs written in IBM 1620 FORTRAN II, IBM 709/7090 FORTRAN II, and Xerox 900 Series FORTRAN II.

The Basic FORTRAN includes integer and real data types, 3-dimensional arrays, unrestricted use of blanks, no reserved words, and magnetic operations.

Xerox Basic FORTRAN IV is used with RBM. It is quite similar to the IBM 1130/1800 TSX FORTRAN, which is an extended implementation of USASI Basic FORTRAN. In addition to the capabilities of the Xerox Basic FORTRAN, Basic FORTRAN IV includes double-precision floating-point operations. The extended precision operations use three data words for nine-digit precision.

Also included are READ and WRITE statements for RAD and disc I/O, an EXTERNAL statement for reference to external symbols, and a data statement. The READ statement can specify an End of File or Error branch, similar to the IBM 360 FORTRAN.

Xerox ANS FORTRAN IV is also used with RBM. It is a superset of ANS X3.9-1966 and is compatible with most existing FORTRAN compilers.

FORTRAN code can be tied to the real-time interrupt structure through the Connect statement. The compiler generates reentrant code that can be run in either foreground or background. Also included are extensive debug features, which are controlled by the user.

The COBOL compiler has the following Level 1 modules:

- Nucleus.
- Table handling.
- Sequential access.
- Relative/random access.
- Index sequential access.
- Interprogram communication.
- Library.
- Debug.

Extensions to Level 1 modules include the ability to handle variable binary, packed decimal, and EBCDIC data formats, as well as combinations of file structures. As an additional optional capability, Xerox offers a number of programming aids: cross-referenced listing, diagnostics, and object program statements interspersed with source language statements. The Xerox COBOL compiler requires the RBM operating system and 24K words of memory, that is, 16K words in the background.

With minor modifications, the COBOL compiler can handle most COBOL programs written for the IBM System/3 and 1968-ANSI standard COBOL compilers, with modules corresponding to the Xerox systems.

Report Program Generator (RPG) provides a convenient programming language for users who wish to perform commercial data processing, as well as the existing batch and real-time processing. RPG runs under RBM. Code for IBM 1800, 1130, and 360/20 compilers can be accepted as input by the Xerox 530 RPG.

Other System Software

Satellite Processor runs as a foreground task under BCM and RBM concurrently with normal foreground and background jobs. It allows a remote 530 to submit jobs to

a host Xerox CP-V system and/or an IBM OS-HASP-compatible installation using IBM HASP Binary Synchronous (BISYNC) Multileaving Protocol. The 530 can be configured to be functionally equivalent to an IBM 360/20 HASP workstation or to a Xerox CP-V slave station. For terminal-to-terminal interchanges the Satellite Processor can directly exchange data with other 530 Satellite Processors, IBM HASP-compatible workstations; Xerox CP-V sites, UCC COPE terminals, and IBM 1130/1800.

Data can be spooled to magnetic tape (RBM or BCM) or disc (RBM only) for optimum resource use. A set of commands are used to define data, to control activity, and to allocate resources.

The system supports half- and full-duplex transmission at data rates from 2,000 to 9,600 bits per second over leased or dialup lines. A log is maintained of transmission errors, number of jobs, and number of responses.

Interactive Data Entry Network (IDEN) provides support for the 530 operating as a terminal system for interactive data entry, validation, and inquiry. It interfaces to the Satellite Processor for communication with a host computer at a central site and to the local batch facilities of the RBM operating system. Information from local terminals can be processed and retained for local use, or it can be sent to the host computer for further processing or for central storage.

The system is modular so that changes in terminals, file structure, editing rules, or application require module change only.

IDEN has an Edit capability to allow validation checks interactively from CRT displays. A dynamic file management system allows a terminal operator to store, retrieve, and modify individual records. The software/hardware structure of IDEN and RBM allows foreground real-time tasks and background programs to run concurrently with IDEN.

The minimum configuration to run IDEN includes 32K words of memory, a disc storage device, communications controller, magnetic tape unit, network of CRTs, and keyboard/printer.

Host computers can be a Xerox Sigma 6 or 9, Xerox 560, or IBM System 360/370.

Sort affords a generalized file sorting capability; it operates under RBM as a background job. A minimum 8K memory is required, but the program will take advantage of any larger memory available. The hardware must include one RAD or disc pack drive for intermediate work files. Sort is compatible in sort controls and file formats with Sigma 5 and 9 Sort programs and will process files created by RPG and ANS FORTRAN IV.

A Concordance Program is used to debug and document programs. Input to the program is a source program in Symbol or Extended Symbol assembly language. The output is an alphabetically ordered table that lists all the symbolic names used in the program and the line numbers on which each name is listed. Control cards can be used to limit or extend the listing.

A Mathematics Library can be used by both Basic FORTRAN and Basic FORTRAN IV. The library is written in Symbol assembly language. Real numbers require two words (32 bits) and are consistent with the short floating-point format used on the Sigma 7.

The System Generation Program allows the 530 user to generate a BCM or an RBM system that is tailor-made for installation and requirements. The generation of a system requires two passes. An absolute master deck is turned into a self-loading system on any output device. In installations lacking magnetic tapes, the system generation program can use cards or paper tape.

System interface unit software includes programs and subroutines designed to serve the wide variety of external analog and digital devices that can connect to a 530 system. The following programs operate in any 530 configuration:

- Interface unit diagnostic programs provide for analog calibration and checkout, closed-loop testing of digital I/O via special test cables, and open-loop testing through oscilloscope displays. These programs run on a stand-alone configuration.
- Interface unit handler subroutines are provided to perform I/O by way of the system interface units. Some of the subroutines are intended for use by the assembly language programmer, and others can be called by Basic FORTRAN and Basic FORTRAN IV programs. These handling routines can operate under BCM and RBM or can be used on the stand-alone configuration.

Application Packages

The Xerox 530 and Sigma 2/3 share a collection of over 500 available programs to cover a variety of applications and tasks. All run under RBM. The most important packages follow:

- COGO (Civil Engineering Coordinate Geometry) — a problem-oriented system developed with familiar engineering terminology to solve problems in coordinate geometry. Computational problems including control surveys, highway design, right-of-way surveys, interchange design, bridge geometry, subdivision work, land surveying, and construction layout are covered by COGO.
- STRESS (Structural Engineering System Solver) — a program utilizing linear analysis in matrix form to find solutions to structural analysis problems. Two or three dimensions and from two to six joints with various degrees of freedom can be accommodated by this system. Output reports for forces, reactions, moments, displacements, and so forth are provided by STRESS.

- HCC-III — a heating, ventilation, and air-conditioning design system.
- PCS (Project Control System) — designed primarily for management in government or industry involved with construction, repair, or maintenance. All critical path users could benefit from PCS as there are no definite industry requirements for such systems.
- BMD (UCLA Biomedical Statistical Package) — encompasses 63 programs to handle specialized data. The programs are divided into the following classes: description and tabulation, multivariate analysis, regression analysis, special programs, time-series analysis, and variance analysis.
- GASP II (Event Oriented Simulation) — an event-oriented generalized activity simulation program used for discrete simulation by writing the events to be simulated in FORTRAN. Inventory models, computer systems, and event versus queuing simulations are included in the applications.
- CSS/3 (Continuous System Simulator) — a block-oriented language to allow digital simulation of continuous processes through a large function selection of functional elements. CSS/3 uses the 7530 or 7531 plotters, and the console data switches permit an interactive on-line operation.
- Commercial Subset — 20 subroutines used for basic business applications with either FORTRAN or Extended Symbol Language. These subroutines remove the limit to the number of digits that can be handled.
- Ideal FORTRAN — 36 business application subroutines used to increase accuracy, I/O character sets, and output capabilities while storage requirements and I/O and execution times are decreased. FORTRAN IV is the intended language although Extended Symbol can be used.
- PHSORT — a FORTRAN Callable sort. Any number of keys in a record can be sorted by PHSORT. Integer, decimal, packed decimal, alphanumeric, and standard and extended-precision floating-point keys can be employed.

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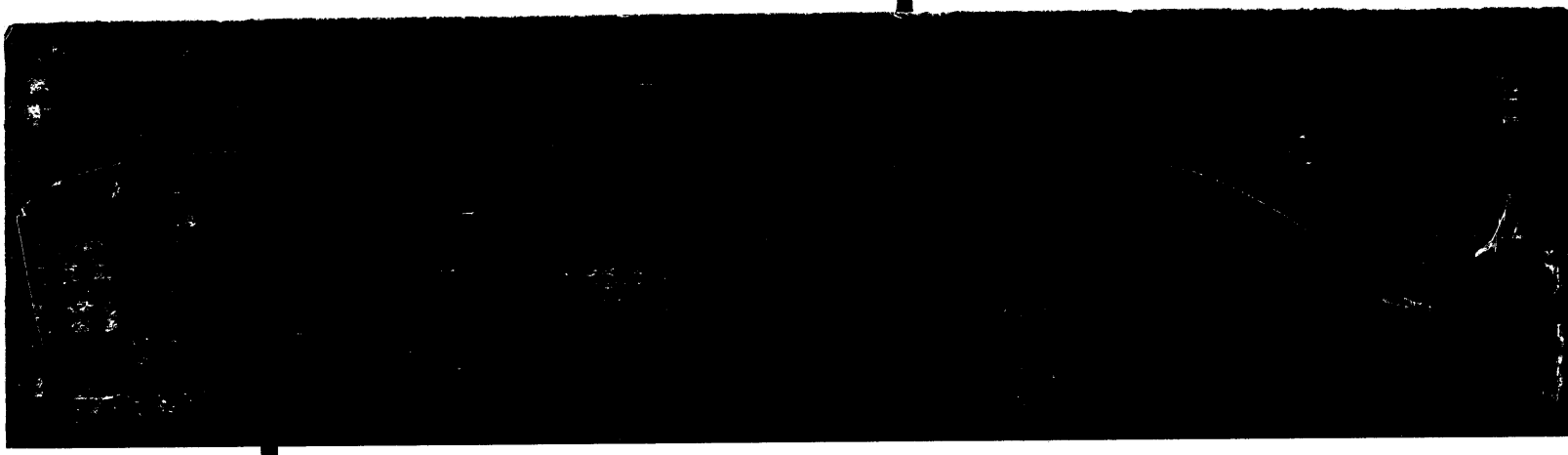

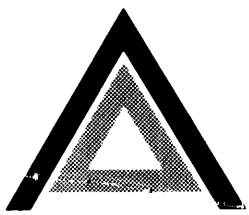

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