Burroughs

B 1870/B 1860 Systems

REFERENCE MANUAL

PRICED ITEM

Printed in U.S.A. March 1979 1090644

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Correspondence regarding this document should be addressed directly to Burroughs Corporation, P. O. Box 4040, El Monte, California 91734, Attn: Publications Department, TIO – West.

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PREFACE

The sophistication and diversity of data processing applications continues to increase, and computer technology adapts to meet new challenges. Burroughs, with its B 1800 series of small-to-medium-scale computer systems, has coupled the acknowledged benefits of today's fourth-generation hardware with the outstanding flexibility, ease of use, and power that is characteristic of Burroughs operating systems and software. Consequently, the B 1800 series yields significant gains in reliablity and maintainability and retains traditional Burroughs cost-effectiveness.

INTRODUCTION

SCOPE

This reference manual provides information on the concepts behind and implementation of B 1800 computer systems. Subjects are treated with varying degrees of detail to benefit a diverse cross-section of readers. A knowledge of electronic theory and hardware detail is not required, but some familiarity with basic hardware terms is helpful, particularly for understanding certain "bit-level" discussions.

The manual is designed for several generic classes of readers: Prospective customers and Burroughs sales personnel will be interested in basic machine concepts and the data dealing with the machine peripheral complement and configuration possibilities, the latter in conjunction with additional marketing literature.

Users, especially those of high technical acumen, will find particular satisfaction in the discussion of machine registers, microprogramming, and Cache Memory.

The Burroughs technical forces will find in this manual a comprehensive treatment of specific fields, down to the bit level, with which the software is concerned. This permits self-training or knowledge refreshment, and provides a ready reference for resolving or isolating anomalies or suspected system abnormalities.

Students in intermediate computer science classes will find a plethora of material dealing with the functioning of a modern digital computer system.

Students in advanced microprogramming courses utilizing B 1800 systems will find the information on microinstructions and the discussions of the I/O subsystem useful in the design of experimental firmware for the machine.

ORGANIZATION

The manual is organized as follows:

Section 1, Concepts, outlines the concepts and features of the system. Following this overview, the most significant or novel of these concepts are discussed in detail.

Section 2, System Elements, includes a discussion of the physical and functional configuration of the system and goes on to describe in detail the Central Processor, data paths, Cache Memory, Scratchpad, S (main) Memory, and the input/output (I/O) subsystem.

Section 3, Control Panels, Section 4, Registers, and Section 5, Microinstructions, provide user-oriented specifics on these system facilities.

Section 6, I/O Subsystem and Device Controls, gives specific information on the operation of the peripheral controls within the context of the overall I/O subsystem.

The appendices (A, B, and C) summarize information on microinstructions, data representation, and number conversions.

RELATED DOCUMENTS (SYSTEM SOFTWARE REFERENCE MANUALS)

Form No.	Title
1068731	System Software Operational Guide
1067535	BASIC
1090586	CANDE (Command and Edit) User Manual
1057197	COBOL
1089992	Data Communications Information Manual
1089794	DMSII (Data Managements System II)
1081882	FORTRAN
1090578	HASP
1088010	MCP (Master Control Program)
1072568	MIL (Micro Implementation Language)
1073715	NDL (Network Definition Language)
1057189	RPG (Report Program Generator)
1081346	SDL (Software Development Language)
1090610	TEXT/EDITOR
1067170	UPL (User Programming Language)

APPLICABILITY

Throughout the manual, the designation "B 1800" collectively refers to Burroughs B 1835, B 1865, B 1860, and B 1870 systems. Specific model numbers are used where differentiation is required.

Burroughs B 1830/B 1825 systems are not included in this edition.

SYSTEM PERIPHERALS

The following is a current listing of peripheral devices available for use with B 1800 systems.

80-Column Card Devices

B 9115	Reader, 300 cpm
B 9116	Reader, 600 cpm
B 9117	Reader, 800 cpm
B 9111	Reader, 800 cpm
B 9112	Reader, 1400 cpm
B 9212	Punch, 150 cpm
B 9213	Punch, 300 cpm
B 9418-2	Reader/Punch, 200 cpm read, 45 cpm punch/print

96-Column Card Devices

B 9119-1	Reader, 300 cpm
B 9119-2	Reader, 1000 cpm
B 9419-2	Reader/Punch/Data Recorder, 300 cpm read, 60 cpm punch/print
B 9419-6	Multipurpose Unit, 300 cpm read, 60 cpm punch/print

Line Printers

(all: 132 print positions)

B 9249-1	85 lpm
B 9249-2	160 lpm
B 9249-3	250 lpm
B 9247-12	400 lpm*
B 9247-13	750 lpm*
B 9247-14	1100 lpm*
B 9247-15	1450 lpm*

* Includes 12-channel format tape.

Magnetic Tape

B 9490-25	Magnetic Tape Cassette, 10 ips
B 9491-2	10 KB, 9 channel
B 9496-2	20/40 KB, 9 channel, 800/1600 bpi*, B 9499-3X MEC required
B 9496-4	40/80 KB, 9 channel 800/1600 bpi*, B 9499-3X MEC required
B 9495-2	60/120 KB, 9 channel 800/1600 bpi*, B 9499-1X MEC required

* NRZ, PE, or both.

Disk Cartridge

B 9480-12	Dual Drive, 4.6 MB, 80 ms average access time
B 9481-12	Dual Drive, 9.2 MB, 100 ms average access time
B 9482-32	Dual Drive, 18.4 MB, 55 ms average access time

Disk Pack

B 9499-7	1x2 Disk Storage/Controller, 174.4 MB, 30/12.5 access/latency times(ms)
B 9499-8	1x2 Disk Storage/Controller, 87.2 MB, 30/12.5 access/latency times(ms)
B 9484-25	1x2 Disk Storage/Controller, 65.2 MB, 25/8.3 access/latency times(ms)
B 9484-55	1x4 Disk Storage/Controller, 130.4 MB, 25/8.3 access/latency times(ms)
B 9486-4	Dual Drive Increment, 174.4 MB, 30/12.5 access/latency times(ms)
B 9484-5	Increment, 130.4 MB, 25/8.3 access/latency times(ms)

Disk File (Head-per-Track Systems Memory)

B 9470-2	Primary Storage Unit, 5.9 MB, 5 ms average access time
B 9470-12	Add-on Storage Unit, 5.9 MB, 5 ms average access time

Industry Compatible Mini-Disk

B 9489-15	Single Unit, 44'' Cabinet, 243 KB, 260 ms average access time
B 9489-16	Dual Unit, 44'' Cabinet, 486 KB, 260 ms average access time
B 9489-17	Single Unit, 30'' Cabinet, 243 KB, 260 ms average access time
B 9489-18	Dual Unit, 30'' Cabinet, 486 KB, 260 ms average access time

Reader Sorters

B 9134-1	4 Pocket, 1625 documents per minute (dpm)
B 9135-2	8 Pocket, 900 dpm, E13B, Off-Line Sorting
B 9135-3	12 Pocket, 900 dpm, E13B, Off-Line Sorting
B 9137-1	4 Pocket, 1625 dpm

SECTION 1.
CONCEPTS

OVERVIEW

Some of the more significant conceptual and architectural features to be found in the B 1800 series of computers are outlined in the paragraphs that follow.

Complete upward and downward compatibility of all user source and object programs, in all languages, between all B 1700 and B 1800 computer systems.

Modularity and easy expandability. Memory size can be easily increased, in modules, from a minimum of 64K bytes (1K=2**10=1024) to a maximum, depending on the model, of 1024K bytes. Memory and peripherals can be readily added or changed with no costly and laborious system regeneration or software changes. The operating system reconfigures itself after a restart that involves pushing two buttons; this process takes about a minute. Consequently, the computer system can be expanded in small increments to meet the user's changing data processing requirements. A large capital outlay is avoided for machine resources that are not required.

Variable micrologic. The architecture of the computer varies its appearance to the programs of each language, presenting the ideal execution environment for each program. Thus, if a FORTRAN program and a COBOL program are being simultaneously run, the FORTRAN program perceives the computer as an ideal FORTRAN machine in such matters as instruction set, word size, and subroutine linkage mechanism, whereas the appearance of the computer to the COBOL program is vastly different, being advantageous to the optimal execution of COBOL. This phenomenon is accomplished by the imposition of a body of microprogrammed firmware, termed an "interpreter", between the object program and the underlying hardware, thus simulating the predefined "ideal machine" and rendering the actual computer hardware totally transparent to the user program. The concept of interpretation is discussed in more detail later in this chapter.

Bit addressability. All memory is addressable to the bit; all field lengths are expressable to the bit. Memory access hardware fetches or stores one or more bits from any location with equal facility. This results in what is termed the "defined field" concept. As the hardware is uniformly adept at manipulation of arbitrarily-sized fields, the idea of "word size" ceases to exist as a formally-defined value. Any number of bits may be defined to be a field; there is no such thing as "word alignment" whereby units of information of fixed length must begin at certain locations in memory. Bit addressability is discussed in detail in the next subsection.

Cache memory. Cache is a high-speed memory that ensures immediate availability of microinstructions.

A hardware-managed stack structure. The B 1800's stack structure facilitates procedure exit and return at the interpreter level and encourages structured implementation of interpreters.

A three-phase processor "pipeline" schema. Pipelining permits the functions of fetching, decoding, and executing microinstructions to be performed separately and concurrently.

A modular, integrated-circuit (IC) main memory. The B 1800's memory design provides speed, reliability, easy expansion, and extensive memory error detection and correction capabilities.

Error detection and correction measures used throughout the Central Processor ensure validity of data storage and manipulation.

An optional port interchange enables independent, rather than processor-dependent, access to main memory by such devices as the multi-line data communications (datacomm) control.

An independent, modular, expandable I/O subsystem uses fully buffered control logic to interface to a wide variety of peripherals. Device types are listed below:

96-column punched card
80-column punched card
Line printers
Disk cartridge
Disk pack
Head-per-track disk
Industry-compatible mini-disk
Magnetic tape
Cassette tape
Reader-sorter
Data communications

Physical and electrical partitioning of the circuitry along common boundaries facilitates system maintainability.

Small size results in efficient use of floor space and minimal power consumption and heat dissipation requirements.

DESIGN PHILOSOPHY

Certain facets of the design philosophy behind the B 1800 are more closely allied with software than with the hardware concepts with which this manual primarily deals. These facets are briefly discussed in the interest of providing the reader with a general understanding of the overall system.

The operating system consists of two firmware routines, GISMO, and the MICRO.MCP, plus the main executive program, the MCP (Master Control Program).

The MCP is similar in function and user interface to those used in larger Burroughs systems. It manages memory, dynamically assigns system resources, communicates with the system operator, logs usage, maintains the periphery that the user perceives as files, initiates and terminates programs, maintains automatically and transparently a directory of all disk files, handles peripheral error conditions, and supervises system operation.

A comprehensive data management system is part of the MCP, and a full complement of compilers, utility routines, and program products is available to the user.

All programs are automatically re-entrant; this means that multiple users use one copy of a given program, only maintaining individual data areas, in order to maximize memory usage. Code and data areas are segmentable at the source language level; execution-time management and switching of segments is a function of the interpreters and operating system and is completely invisible to the user. If a needed segment is not in memory, it is automatically loaded from disk by the MCP. This true virtual memory system is efficiently implemented through data and code dictionaries created by the individual compilers and made part of each object program on disk. The MCP continuously attempts to maximize memory utilization by initiating new programs or by permitting active programs to retain code space, data space and file (buffers, tables) space.

The interface to data communications equipment is facilitated by a Network Definition Language (NDL). NDL is compiled by is own compiler to generate a program that handles all aspects of data communications. This program, called a "handler", performs all the requisite data-communication input/output operations, audits messages and exception conditions, provides line and terminal service based upon management priorities, and processes and supervises message flow from application programs and remote stations.

NDL, a true high-level language, is the means by which numbers and characteristics of lines, terminals, addresses, priorities, and similar network information is provided in a descriptive, free-format,

easy-to-use manner. Hence, the user, through the application program, can deal with the data communications network as a file, precisely like a printer or magnetic tape file or any other I/O file.

BIT ADDRESSABILITY AND THE DEFINED-FIELD CONCEPT

The B 1800 has none of the hardware-dictated word size or alignment restrictions found in traditional computers. Memory addressing at the hardware and microcode level is accomplished through a 24-bit FA (Field Address) register that can directly address 16,777,215 bits as though they were in a continuous bit string. The B 1800 uses the FA register to address any portion of memory, reading or writing memory either forward or backward from the address contained in FA. From 0 to 24 bits may be processed in one operation that takes one memory cycle of 167 nanoseconds. The width of the read or write data is specifiable at compile time as a literal number of bits, the literal forming one subfield of the microinstruction. Dynamically variable read or write operations of up to 65,535 bits are accomplished at execution time by use of the 16-bit FL (Field Length) register. A microprogrammer typically constructs an extremely tight loop of microcode to transfer 24 bits at a time; one particular microinstruction, named Bias (3E), facilitates handling the exit from this loop as well as the handling of odd-length (<24 bits) last-iteration remainders. The FL and FA registers constitute a data descriptor referencing a specific field of memory by specifying the bit length and absolute bit address.

The primary benefit of bit addressability is a reduction in memory requirements for various blocks of information. Despite the ever-decreasing cost of memory and the availability of large quantites of mass storage, the phenomenon of "thrashing" is always a potential problem on a machine utilizing the concepts of virtual storage, such as the B 1800. By maximizing the compaction of various blocks of information, program working sets are diminished in size, resulting in fewer and smaller overlays. Readers familiar with formal information theory will recognize this as an example of raising information content by reducing redundancy.

Bit addressability permits the defined-field concept to be efficiently implemented; information can be represented in field size and format based on the magnitudes of the quantities that are to be stored, not upon hardware word sizes. Consequently, such units of information as op codes or data and code addresses are represented in B 1800 memory in far less space than in traditional fixed-unit-length computers. In comparison with byte-oriented machines, the B 1800 generally represents programs in approximately half the memory space; comparison with word-oriented machines shows an even more dramatic ratio.

A practical example of the defined-field concept illustrates the advantages.

Suppose there exists a computer that, for the sake of simplicity, has a repertoire of precisely six instructions. Let it be postulated that, after examination of several typical programs, one of the six instructions is found to occur 1000 times, whereas the other five are found exactly 200 times apiece. This situation, although simplistic, is quite typical of op codes on any computer; relative frequencies vary widely. For maximum efficiency, the op code would be represented in the traditional machine as a three-bit field. Routine calculation yields the required storage space for these op codes.

Instruction	Op Code	Occurrences	Total Bits
1	000	1000	3000
2	001	200	600
3	010	200	600
4	011	200	600
5	100	200	600
6	101	200	600
			6000

A computer such as the B 1800, with variable-length instructions, can use the technique of "frequency-based encoding" to more efficiently represent the same information, by expressing the more frequently found possibilities in shorter fields.

Suppose the most frequently found instruction is encoded with precisely one bit. This bit, if a zero, represents that instruction; if a one it acts as an "escape code" to signify that three more bits of op code follow. Thus, one particular instruction is represented in one bit and the other five instructions each require four bits. The memory utilization of the same example is again computed.

Instruction	Op Code	Occurrences	Total Bits
1	0	1000	1000
2	1000	200	800
3	1001	200	800
4	1010	200	800
5	1011	200	800
6	1100	200	800
			5000

A thousand bits of storage have been saved for the op codes alone, a decrease of 16.7 percent.

A still better encoding algorithm can be devised: one instruction taking one bit as before, another instruction taking two bits, and the remaining four instructions taking four bits each. The instruction to be assigned two bits is irrelevant here, but would normally be that one of second highest incidence.

Instruction	Op Code	Occurrences	Total Bits
1	0	1000	1000
2	10	200	400
3	1100	200	800
4	1101	200	800
5	1110	200	800
6	1111	200	800
			4600

The 1400-bit saving represents 23.3 percent more efficient memory utilization compared to fixed-length encoding. Note that this particular algorithm has no room for expansion, as all possible bit combinations have been used. This may or may not be significant in the design of a given language.

The defined field concept is readily applicable to other units of data commonly found in memory. Consider the operand subfields that, along with the op code, form a typical instruction at the hardware level. For example, a branch instruction might have a bit to signify that either a long or a short displacement subfield follows. The more frequently expected short form of the instruction, generated for the majority of operations, would cause an overall decrease in code space. The long form of the branch instruction would be necessary only for those few branch operations of too large a magnitude to be represented in the shorter form. Thus, the capability exists for branches of any realistic magnitude, but excessive unused operand space is not required for each such instruction in a program, unlike the situation in a non-defined-field machine.

The defined-field concept facilitates the interpretation of non-B 1800 object programs, as the architecture of any computer (not only Burroughs), is readily implemented in microcode, allowing the direct execution of object code from that machine. A number of widely-used machines have been implemented in microcode by Burroughs; these "foreign" programs are as "normal" to the B 1800 as are RPG or COBOL programs, and, hence, can be freely multiprogrammed.

THE CONCEPT OF INTERPRETATION

General-purpose computer systems are usually designed to process programs written in a variety of programming languages; the diversity of these languages necessitates a central processor that is able to work with widely differing data structures and possessing an instruction set adequate to handle the differing functions of each language. The traditional approach to this process dictates that each compiler on a system generate code appropriate to that language, utilizing a subset of the total pro-

cessor capability. This philosophy is represented pictorially in figure 1-1. For example, a processor whose capabilities encompass the efficient execution of COBOL must have a variety of instructions for efficient movement, manipulation, and transformation of digit and character data. A FORTRAN-oriented processor must have fast algebraic and numeric capabilities. The processor oriented toward block-structured languages such as ALGOL must have the capacity to effectively process stack structures and the ability to represent data with major variations in format.

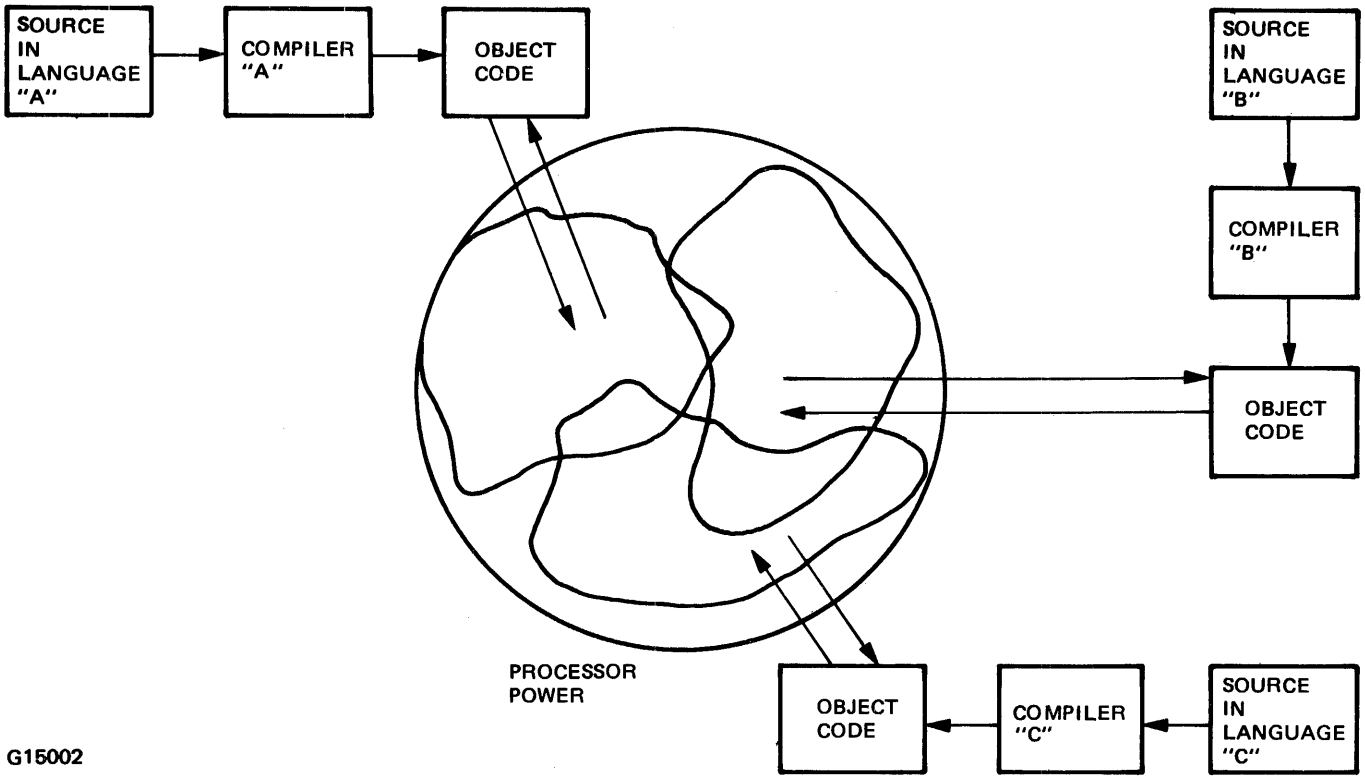


Figure 1-1. Traditional Approach to Interpretation

In the worst case, such a processor is designed to process one class of languages in a superb manner; other compilers generate code which runs with moderate to severe inefficiency, being "shoehorned" into an architecture unsuitable to satisfactory execution of that language.

The B 1800 is designed to be a general-purpose computer system, efficiently accommodating users of widely differing needs. Intended as a relatively inexpensive system despite its power, the B 1800 attacks the problem of efficiently processing diverse languages and applications in an elegant, rather than "brute force", manner. An unusually low-level instruction set is coupled with bit-addressable memory as previously described to form a general-purpose architecture that is completely invisible to all programs running on the system, including the operating system. This permits an architecture that has almost unlimited versatility as well as hardware that is relatively inexpensive to manufacture and maintain, resulting in an efficent, powerful, cost-effective machine.

The above description of the B 1800 design philosophy may seem dichotomous. How can a simple, low-level architecture efficiently process diverse applications and dissimilar language classifications? How can an architecture be transparent to an object program, let alone the operating system which manages the resources of the machine itself? How can a system without a large, complicated instruction repertoire claim to provide a near-optimal execution environment for programs of widely dissimilar nature?

The answers to these questions follow from the fact that object code generated by B 1800 compilers does not execute directly upon the hardware of the B 1800 processor. Instead, Burroughs has cre-

ated microprograms, defined to be sequences of primitive microinstructions, which, alone, directly execute upon the low-level hardware of the processor. The function of each of these bodies of microinstructions (termed "interpreters") is to emulate the behavior of a machine deemed ideal for execution of a given language. In the case of object code for a "foreign" machine, such as the Burroughs B500, the interpreter emulates that particular machine, allowing the object code to behave as it would on the real computer.

The code generated by B 1800 compilers does not actually run on the B 1800 hardware; therefore, technically, it is not object code. It is termed "S" code – "S" for "system", "soft", or "simulated". The environment presented to that code by each interpreter is called the "S-machine" for a given language. Each interpreter uses B 1800 memory and registers to represent registers, accumulators, and stacks needed to optimally execute programs of a language. Individual object code instructions are not fetched by the processor; instead, an interpreter fetches (by reading memory) individual instructions (termed "S-ops") from the S-code and invokes appropriate micro-routines to perform each S-op.

If the interpreters were to be considered part of the hardware, then the individual S-ops could be characterized as being fetched and executed by the processor. However, the environment presented by one interpreter is vastly different from all others in terms of instruction set, data formats, addressing methods, and even the physical layout of the object code file as it resides on disk; therefore, the interpreter cannot really be considered to be part of the hardware.

Neither is an interpreter strictly part of the software. Although it is composed of series of instructions, those instructions are at a far more primitive level than those of the software being interpreted.

Consequently, the interpreter is best described as a body of "firmware", possessing attributes of both hardware and software that enable successful operation of both. Figure 1-1 depicted the relationship of source and object code to the processor. Figure 1-2 gives a somewhat different view of these relationships as they apply to the B 1800 system. An interpreter is analogous to a collection of separate routines, each handling one S-op, with a master "driver" loop fetching one S-op at a time. For example, consider the following paragraph from a typical Cobol program:

```
ENTER-RECORD.
    MOVE TRAN-FILE-KEY TO TBL-FL-NM(TABLE-KEY).
    MOVE TRAN-KEY TO RCD-SYM-KEY(TABLE-KEY).
    MOVE 1 TO REPLY-TYPE.
    GO TO END-TABLE-SEARCH.
```

This source code happens to generate four S-ops, which are most easily comprehended with their English mnemonics:

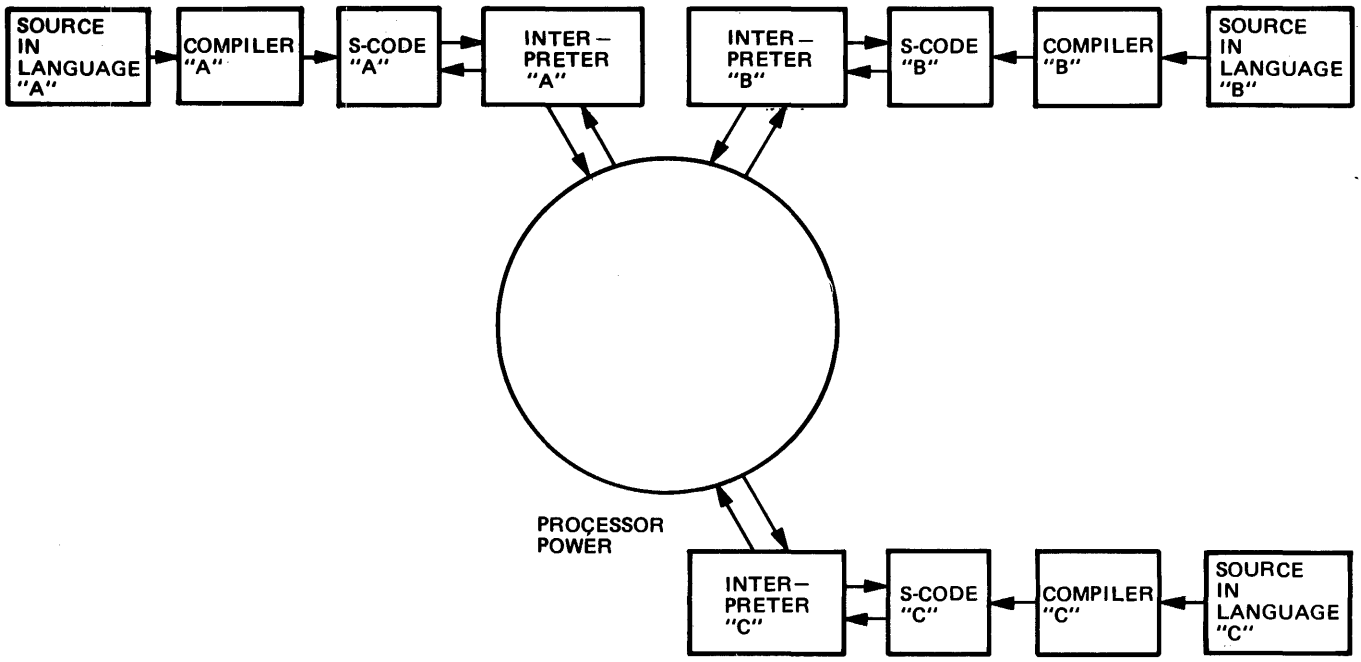
```
<MOVE NUMERIC> <OPERANDS>
<MOVE ALPHANUMERIC> <OPERANDS>
<MOVE NUMERIC> <OPERANDS>
<BRANCH UNCONDITIONALLY> <OPERAND>
```

The interpreter processes these S-ops repetitively, as follows.

a. Fetch and decode the next S-op:

```
MOVE NUMERIC (OP CODE = 001)
```

COBOL uses previously-discussed principles of frequency-based encoding and bit-addressability. The seven most frequently-used S-ops are encoded in three bits; other S-ops have an escape code of 111 in the first three bits and a total length of nine bits for the op code. "MOVE NUMERIC" happens to be a three-bit op code.



G15001

Figure 1-2. B 1800 Approach to Interpretation

b. Index into a table of subroutine locations:

```
THREE.BIT.OPS
CASE OP.CODE
     GO TO MOVE.ALPHANUMERIC.OP                  % 000
==>GO TO MOVE.NUMERIC.OP                         % 001
     GO TO INCREMENT.OP                          % 010
     GO TO BRANCH.UNCONDITIONALLY.OP             % 011
     GO TO COMPARE.ALPHANUMERIC.OP               % 100
     GO TO COMPARE.NUMERIC.OP                    % 101
     GO TO PERFORM.ENTER.OP                      % 110
     GO TO ESCAPE.CODE...HANDLE.9.BIT.OPS        % 111
END CASE
```

NOTE

The above is an English-like pseudo-language that expresses the actions of the COBOL interpreter; it does not reflect the actual Burroughs microprogramming language.

c. Branch as instructed and perform the microcode that emulates the behavior of a hard-wired MOVE NUMERIC instruction:

```
MOVE.NUMERIC.OP
     <Microcode to perform the move. Operands for this instruction specify the location of
     the source and destination variables on which this S-op will act>
GO.TO.MAIN.FETCH LOOP     % return
```

d. Repeat the process, this time for the MOVE ALPHANUMERIC S-op.

The microcode for a given instruction varies according to the complexity of the operation being emulated. An S-op such as Branch Unconditionally involves little more than the manipulation of a code

address pointer to affect the location from which the next S-op is fetched. This contrasts with, for example, an S-op that involves the searching of a linked list of items until a certain criterion is satisfied. The latter is a task of considerable more complexity, but is needed for the interpreter that handles the language in which the operating system is written.

In summary, the action of a particular S-op can be anything that the designers of an S-language believe will enhance the efficient execution of that language. If experience or the requirements of a new computer application reveal that the available set of S-ops in a language is inadequate to efficiently execute a needed task, new S-ops can be added to the interpreter, and the logic to generate those S-ops can be added to the appropriate compiler. On the traditional, hard-wired computer the addition of a new instruction necessitates physical changes to the electronics of each processor. This is a task of considerable difficulty and expense when the size of a vendor's user base is considered. Likewise, an already-existing S-op can be rewritten if it is found to be deficient or to act erroneously in certain circumstances. A new interpreter is easily provided to every user, in the same manner as any piece of software is distributed.

Thus, it is the interpreter which shields the object program from the actual hardware, presenting the illusion of a machine ideally suited to optimal execution of a given language. One valid question remains: The interpreter represents a level of separation between program and machine. Although the interpreter provides benefits by allowing each language to execute upon a computer architecture best suited to itself, might not the multiple levels of the program-interpreter-processor hierarchy be a disadvantage, in that a valuable system resource (the processor) is only being indirectly used by the object program?

The power of the B 1800 offers proof to the contrary. The system resources and effort necessary to accomodate architecture that changes from program to program is less than that wasted when one architecture is used for all applications. Definable structure permits the representation of information logically, based upon the inherent structure of that information. Manipulations at the object level are defined in a manner expeditious to the efficient execution of programs. The sophisticated S-machines are more powerful than would otherwise be possible and, when executed on the B 1800 variable-image processor, result in speed, small demand on system resources, and, consequently, more throughput per unit cost.

Microinstructions deal with the processor at such a primitive level that they are generally individually executable in one or two clock cycles on the 6-MHz processor. Further, the B 1800 has a special, high-speed, hardware-managed "Cache" memory, described in detail later in this chapter, that permits the processor to fetch and execute individual microinstructions with extreme rapidity. As a result, the advantages of the S-machine substantially outweigh any degradation that results from the hierarchical structure.

THE CONCEPT OF NANOPROGRAMMING

The term "pipelining" is generally refers to the ability of certain processors to actively work on more than one hardware operator simultaneously. The B 1800 Central Processor falls into this category, for, at any instant, the processor is dealing with three microinstructions, performing concurrently the actions of fetching, decoding, and executing. Figure 1-3 characterizes this capability.

At the time micro A is being executed, the next microinstruction, A+1, is being decoded into the N (nano) register, and a third microinstruction, A+2, is being fetched from the M register. The fetch concept is well-understood. However, the decoding process requires discussion.

Within the B 1800 Central Processor, decoding is the process of setting various bits in the N register, which is a 114-bit internal mask whose bits represent allowable control signals that direct data movements and transformations during the execute phase. Each of these 114 possible actions, called "nanos", represents the most detailed level of action specifiable within the processor hardware.

The decode process is not controllable through firmware; the most basic (and only) level of action within the firmware is the microinstruction.

The decode process is implemented by means of PROMs (programmable read-only memories) and, thus, can be modified and augmented without major hardware changes when the need arises.

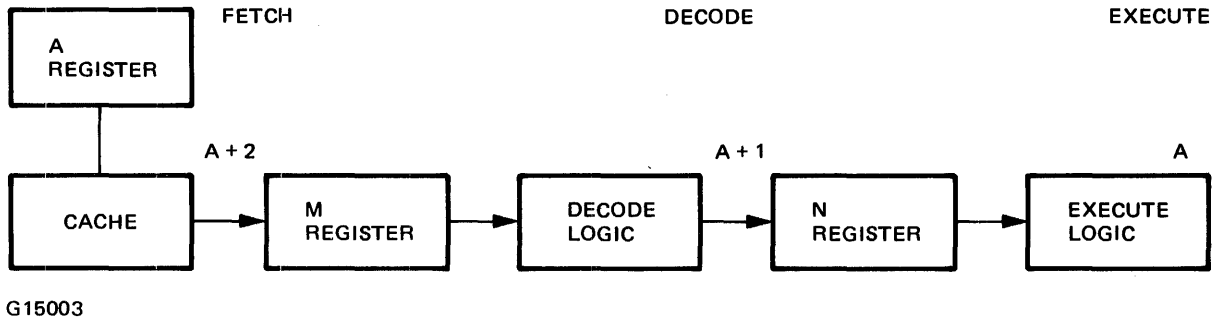


Figure 1-3. Nanoprogramming

SECTION 2.
SYSTEM ELEMENTS

PHYSICAL CONFIGURATION

The term "central system" is used to refer to the non-peripheral portions of the computer system. In terms of physical modules, these include the Central Processor, S Memory, the I/O bases and controls, the port interchange (if used), operator and field engineering interface facilities, power subsystems, and ventilation equipment. B 1800 central systems are housed in two cabinet styles, pictured in figure 2-1.

Cabinet panels are readily removable for access to components. All circuit elements are rack-mounted and the assemblies form a vertical column for efficient ventilation and cooling. All logic circuitry is constructed on modular, pluggable circuit cards; connections between logic cards are made by point-to-point wiring on the backplane and by multiple-conductor flat ribbon cable on the front plane. DC power is distributed to the circuitry by a network of bus bars.

Each central system also includes two control panels, one or two magnetic tape cassettes, and a console with keyboard and display. These are all shown in figure 2-1.

FUNCTIONAL CONFIGURATION

Overall functional configuration is represented by the block diagram in figure 2-2. Details are implicit in the subsections and sections that follow.

CENTRAL PROCESSOR

The B 1800 Central Processor, including its clock and I/O distribution facilities, is contained on a set of modular printed circuit boards or "cards". These cards comprise the circuitry that performs logical and arithmetic operations, data movement and storage, and all operations that interface the processor with memory, the port interchange (for memory contention, if required), and the I/O subsystem

Several distinct sections are found in the processor:

1. Registers for storage of operands, addresses, literals, and various control signals.
2. A 24-bit Arithmetic and Logic Unit (ALU) for performing arithmetic and logical operations, as well as data transformations.
3. The A and M registers, plus the A-stack, for controlling the source of microinstructions and providing a path to the decoding and execution logic.
4. Cache Memory, for local (in-processor) storage of microinstructions, providing rapid access for the program being interpreted.
5. S-memory interface, to provide communication with main storage.
6. I/O interface, for communication with system peripherals.

The Central Processor may also be considered to include both control panels and the keyboard and display units, and the magnetic tape cassette unit.

Figure 2-3 is a detailed layout of the Central Processor. (Note that this diagram does not include the microinstruction decoding and control logic.)

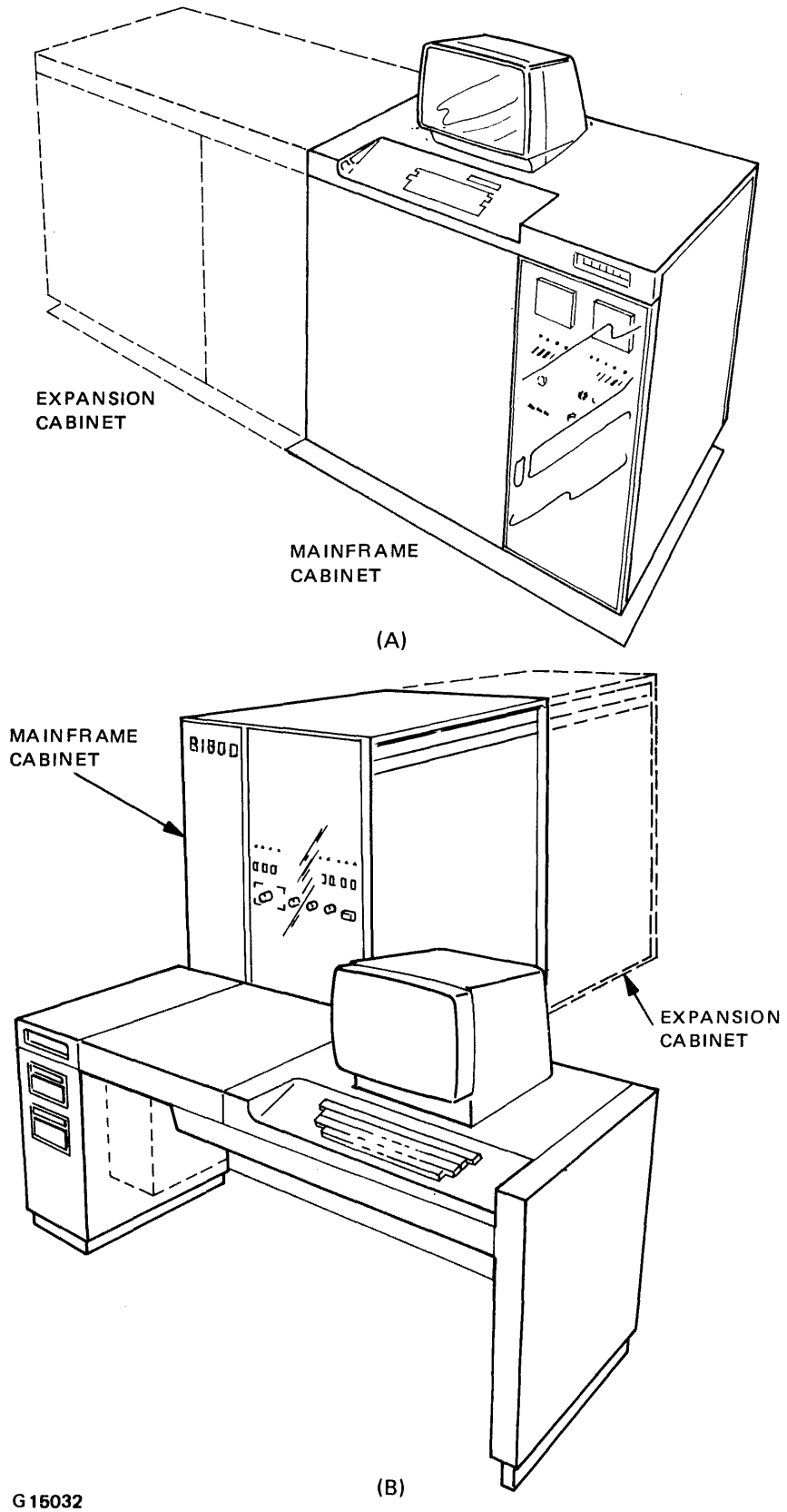


Figure 2-1. Physical Configurations, B 1800 Central Systems

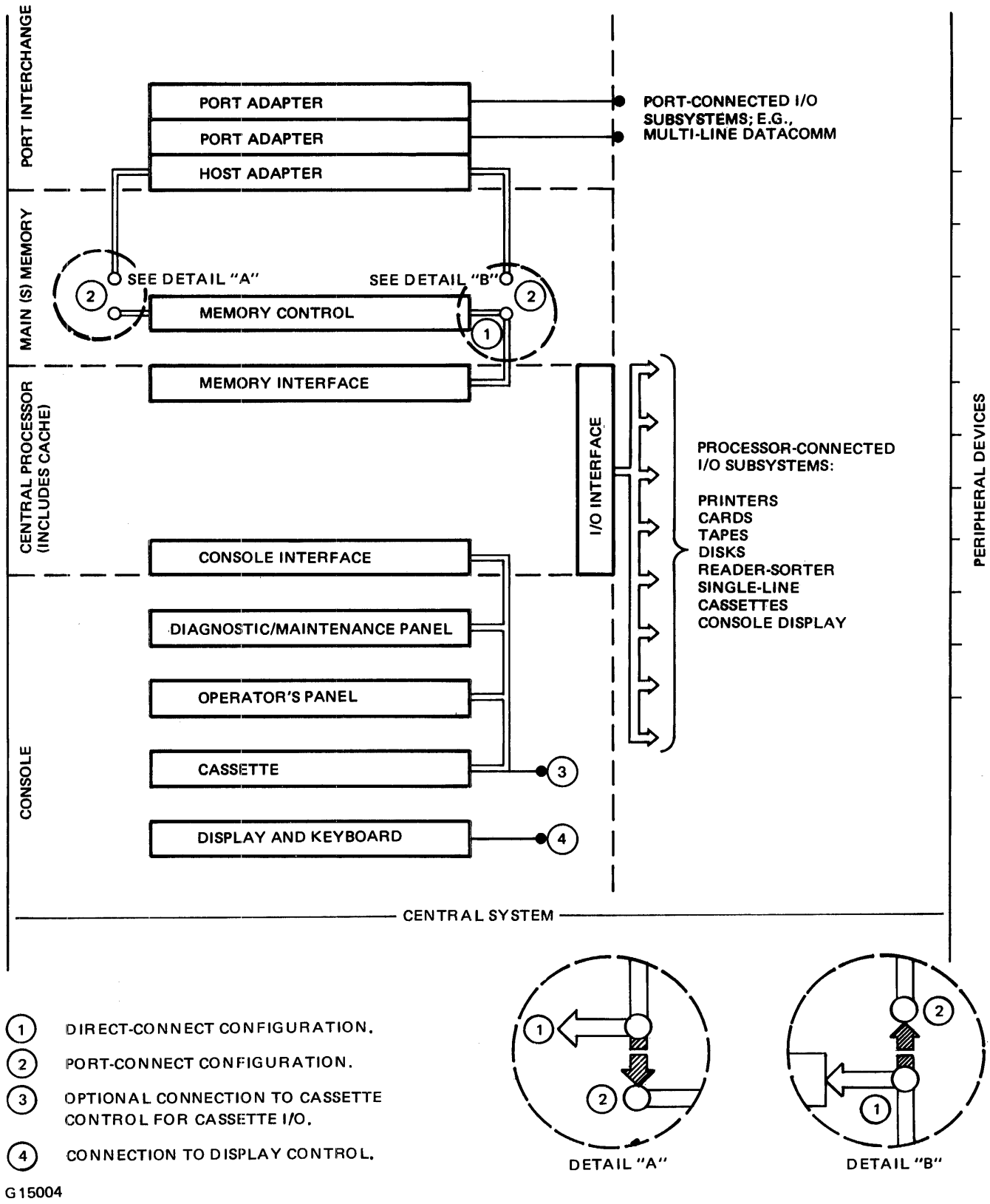


Figure 2-2. Functional Configuration, B 1800 Central Systems

DATA PATHS

Data movement within the processor is generally a function of the 24-bit Main Exchange (MEX), with its two subdivisions MEXA and MEXB. (These are evident in figure 2-3.) MEX represents the common input and output connections of a number of logic elements within the processor. The output of the 24-bit function box is fed to MEX, which routes data to working registers through MEXA and MEXB. The output of the working registers is fed to the 24-bit function box, through which data must pass to reach MEX. Additional connections include the S Memory interface, A and M registers, the A Stack, and Cache Memory.

Certain microinstructions involve the simultaneous movement of data to and from certain working registers (FA and FB). To accomplish such swap operations, the working registers are divided into two sections, electrically isolated from each other. One section is fed by MEXA, the other from MEXB. The distinction between MEXA and MEXB is relevant only to the simultaneous data movement instructions.

MAIN MEMORY (S MEMORY)

S Memory is the primary data storage medium within the B 1800 system. S Memory can be accessed directly by the Central Processor and, if a port interchange is used, by certain I/O subsystems.

Although constructed in 16-bit units, S Memory is seen by the processor as an continuous string of bit locations that are randomly accessible beginning at any selected bit. Memory accesses can involve from 0 to 24 bits per clock cycle. In addition to the 16 bits of data storage in the basic memory unit, six error correction bits are available. These are stored and accessed by the processor in parallel with the associated data. Thus, the actual width of the basic memory unit is 22 bits, although only 16 bits are normally seen by the microprograms. Special diagnostic microinstructions permit access, if needed, to the error correction bits.

Within each IC chip, precisely one bit location is accessible at a time. Addressing is accomplished with six binarily-weighted address lines, with the required 12 address bits being provided in two accesses by the processor. Decoding is provided within the chip itself. Multiple-bit data fields can be accessed and stored because the chips are arrayed and can be addressed in parallel. For efficient manipulation, the 16-element size of this array corresponds to the length of a microinstruction. This array structure is shown in figure 2-4.

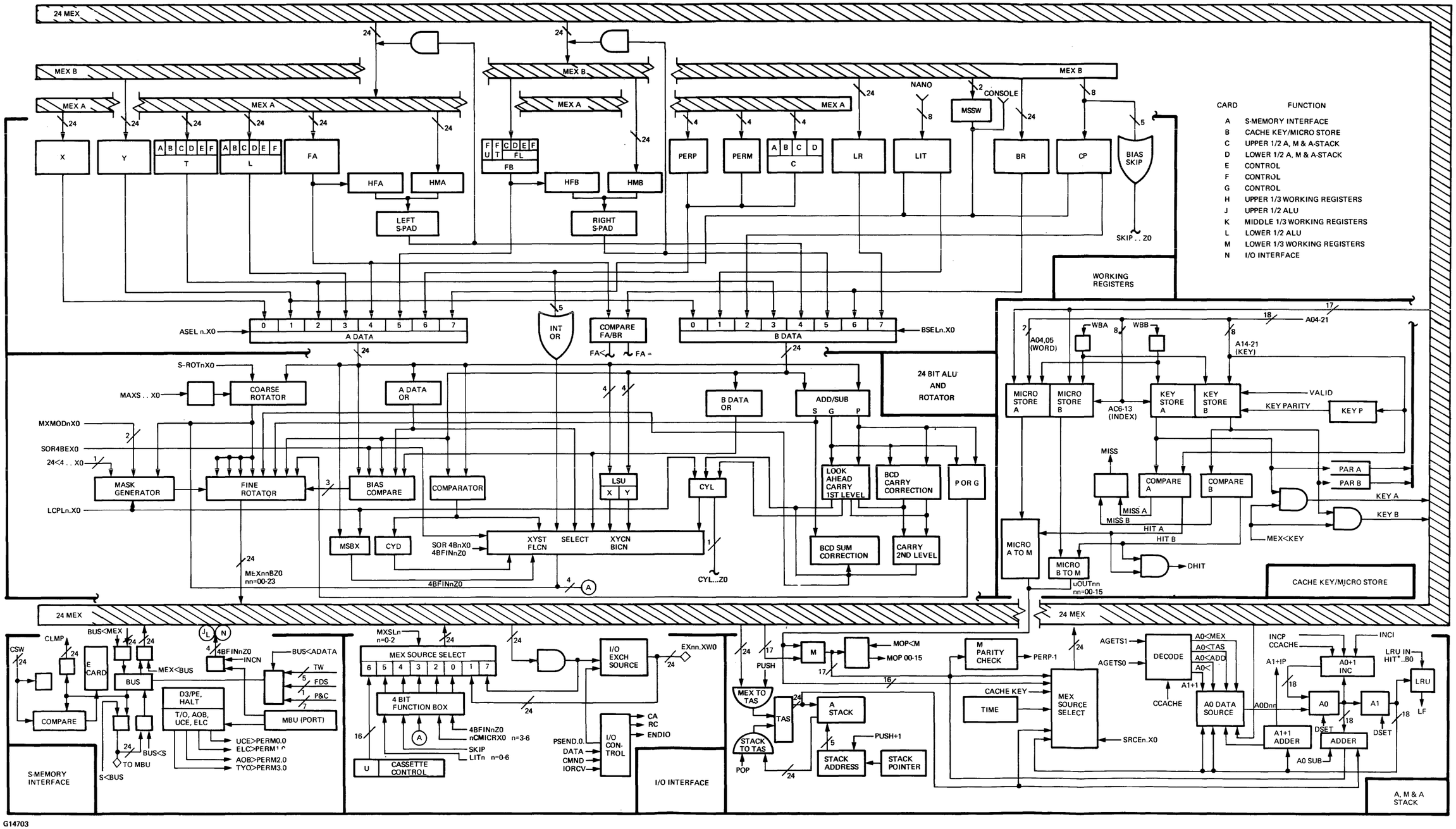


Figure 2-3. Block Diagram, B 1800 Central Processor

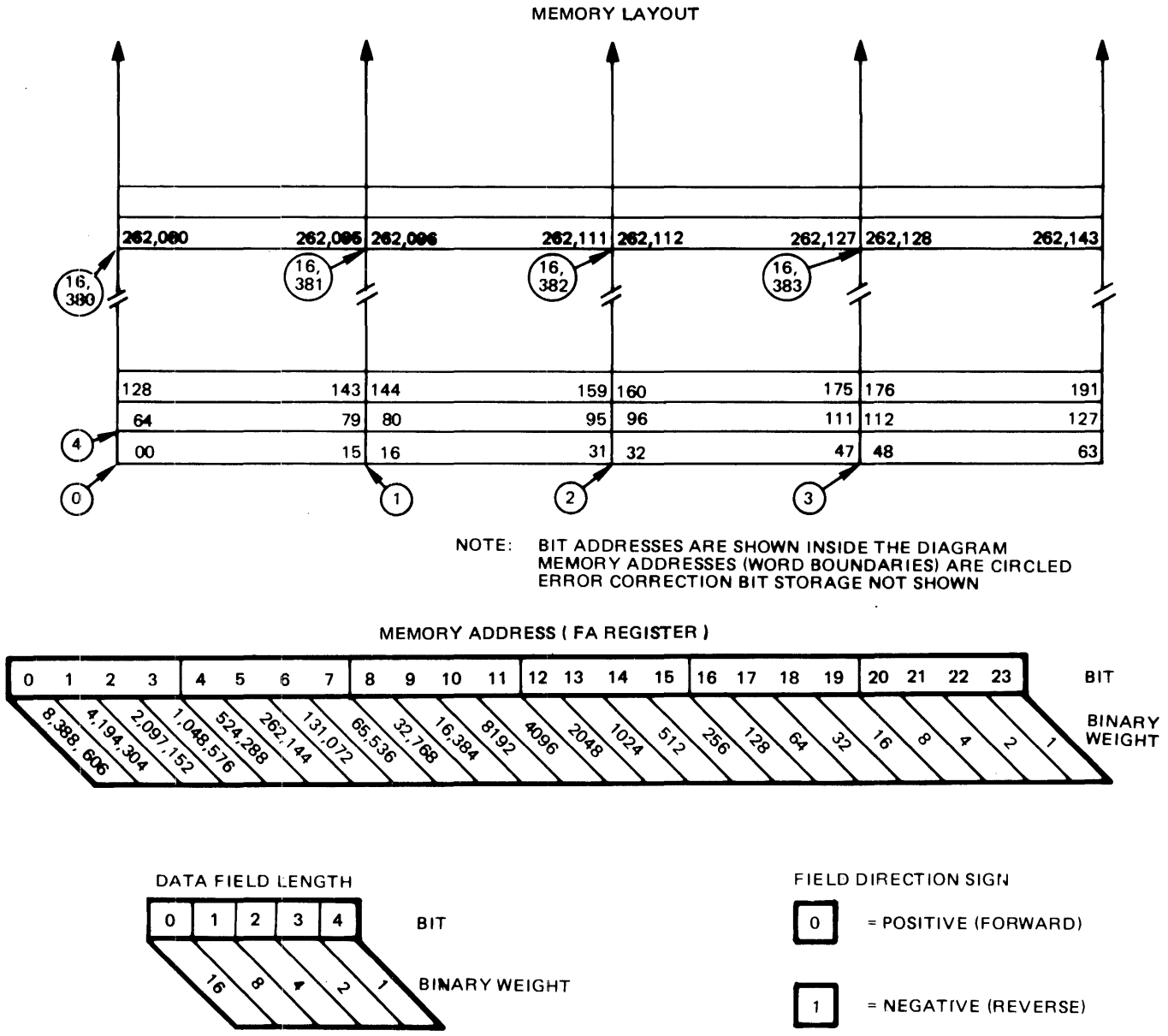


Figure 2-4. S Memory Layout and Access Parameters

SCRATCHPAD

The Scratchpad is a random-access, high-speed memory that provides the processor with general purpose temporary storage. Scratchpad can be addressed as either thirty-two 24-bit units or sixteen 48-bit entities. Scratchpad is typically used for important pieces of global data within an interpreter, such as top-of-stack entries, for which registers cannot be spared. Various microinstructions can directly access individual Scratchpad "words", avoiding problems of memory addressing.

The right half of Scratchpad word 0 has additional usage, in that it may be considered congruent with the FU and FL portions of the FB register, which is heavily involved in data access within S Memory. Processor hardware continuously compares SFU and SFL, the corresponding subfields of this Scratchpad word, to FU and and FL, setting certain bits in the FLCN pseudo-register to indicate the results. This comparison has been found to be useful by microprogrammers, allowing efficient data manipulation without the need to continuously move Scratchpad data into registers for testing purposes.

Figure 2-5 depicts the Scratchpad.

CACHE MEMORY

Cache is a high-speed, hardware-managed memory located within the Central Processor and used to hold microinstructions in readiness to be fetched and executed. Cache has a capacity of 2,048 (2K) sixteen-bit microinstructions, plus 256 pairs of 8-bit Cache "Keys".

The Cache delivers to the processor the microinstruction specified by the A register. When the micro specified is not found in Cache, it is fetched from S Memory and loaded into Cache. (All microprograms reside in their entirety in S Memory.) The algorithm used to locate a microinstruction in Cache is of the hashing family (indexed-associative organization).

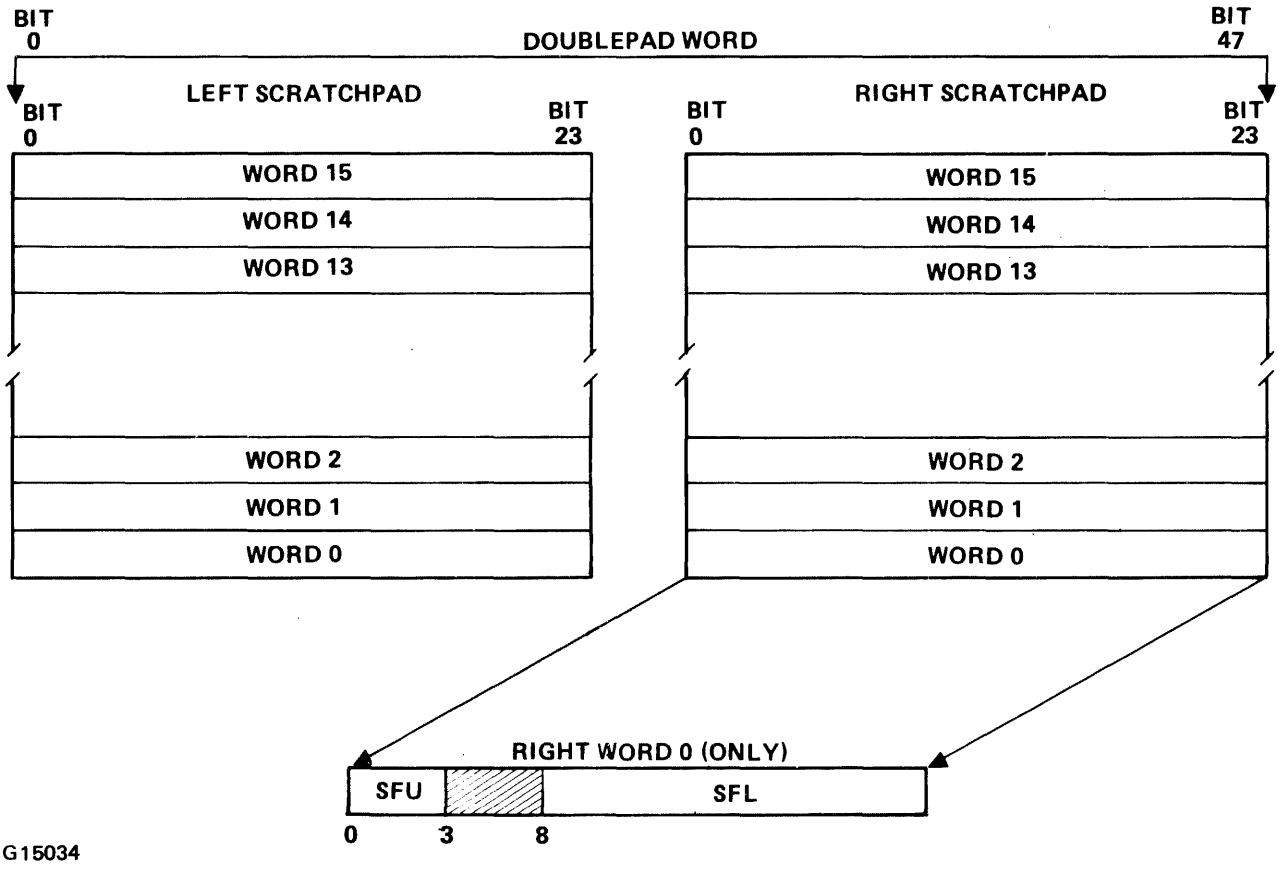


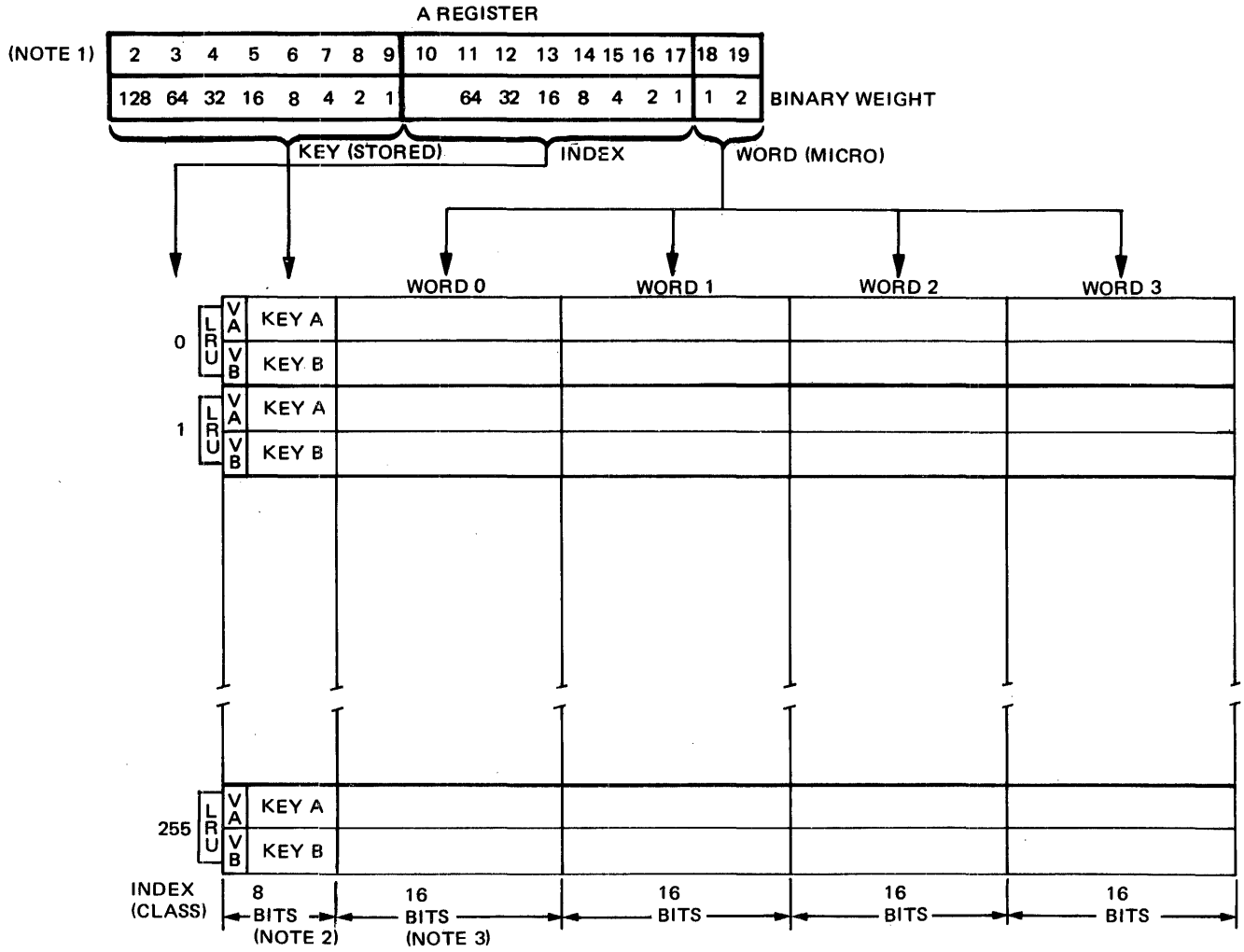
Figure 2-5. Scratchpad

Cache is partitioned into 256 "classes"; indexes to Cache. Each class consists of two "blocks" of four 16-bit words. One microinstruction can be stored in each word. Each of the two blocks contains a "key" field that holds the 8-bit key plus one "validity" bit and one parity bit. Each of the 256 has an associated "least recently used" (LRU) bit. Figure 2-6 diagrams the organization of Cache memory and its relationship to the A register

The 18-bit A register contains the absolute S Memory address of the microinstruction to be executed. The design of this address is directly related to the organization of Cache.

The INDEX portion of the A register can hold a value between 0 and 255 to directly specify which Cache index will be examined for the specified microinstruction. The KEY portion of A enables an associative comparison to be made with the two Cache keys (A,B) of that index.

"Associative" comparison means comparing by contents; that is, rather than comparing first key A and then key B for a match, comparison is tested for both simultaneously. No match is termed a "Miss", one match is a "Hit". (If both match, an error has occurred; this condition is covered in the discussion of the PERP register.) On a Hit, the microinstruction fetched is the one specified by the WORD field (0-3) in the A register.



NOTES
1. BITS 0 AND 1 ARE NOT USED.
2. KEY STORAGE IS ACTUALLY 10 BITS: 8 ADDRESS, 1 VALIDITY, 1 PARITY.
3. MICRO STORAGE IS ACTUALLY 17 BITS INCLUDING PARITY.

G15035

Figure 2-6. Cache Memory Organization

On a Miss, a Cache loading process takes place. Four sequential microinstructions (64 bits) are read from S Memory, starting at the absolute address specified by the A register, or, if the A address is not evenly divisible by 4, at the preceding modulo-4 boundary. (The latter phenomenon is infrequent and results from a Branch Relative or Call Relative microinstruction.)

The four sequential micros are to be written into the least recently used of the two Cache blocks specified by KEY in the A register. The specific block is determined by testing the LRU bit associated with the Cache index: LRU=0 means block A was least recently used for a micro fetch, LRU=1 means block B. Following this operation, the LRU bit is complemented. (The LRU bit is also changed by a Hit to show that the other block has become least recently used.)

The final concept needed for an understanding of Cache operation relates to the validity bit, which indicates whether or not a given block contains valid information. The term "invalidity bit" is more accurate because V=1 indicates that the microinstructions in that block are not valid. When Cache is cleared by the Clear Cache (5F) micro or from the console, all validity bits are set (1). As Cache is loaded, either by the algorithm described above or from the console, the appropriate validity bit is reset. A validity bit of 1 inhibits that block from registering a hit.

Cache can be cleared only by means of the Clear Cache micro. This micro is issued by the operating system whenever an interpreter's user count reaches zero or when the interpreter's segment in S Memory is overlayed. This precludes a problem that could arise when an interpreter is placed in an area of S Memory previously used by another intepreter. If Cache were not to be cleared, the prior microinstructions could erroneously become available to the new interpreter in any Cache location that remained unoverlayed. To summarize this conceptual discussion of the Cache memory, a list of terms is presented below, followed by an example of Cache operation.

Address Register
: The register that points to a word in Cache. It may be pictured as comprising three distinct subfields, INDEX, KEY, and WORD. This is the A register in B 1800 systems.

Block
: A number of words transferred from S Memory when a Miss occurs. Each Cache key, with its validity bit, refers to a single block of microinstructions in Cache. In the B 1800, each block includes four words.

Class
: One of 256 Cache units addressed by the INDEX field in the A register.

Hit
: A term that connotes that the microinstruction specified by the A register has been found in Cache.

Hit Ratio
: The ratio of hits to total number of access attempts.

INDEX
: The A register field that specifies which of the 256 Cache classes is being sought.

KEY
: The A register field that is associatively compared with the Cache's Key Store to determine whether the class specified by INDEX includes the block being sought.

Key Store
: The areas in Cache that hold the addresses to the blocks of microinstructions.

Least Recently Used
: (LRU) A method for keeping the set of micros "up-to-date," by replacing, when necessary, that block of micros (in the pair) that has been unused for the longest time.

Micro Store
The areas in Cache that hold the microinstructions. Each block contains two classes, each class consists of four micros (words) for a total 2048 micros.

Miss
A term that connotes that the microinstruction specified by the A register has not been found in Cache. When a Miss occurs, four sequential microinstructions are fetched from S Memory and loaded into the Cache block that was specified.

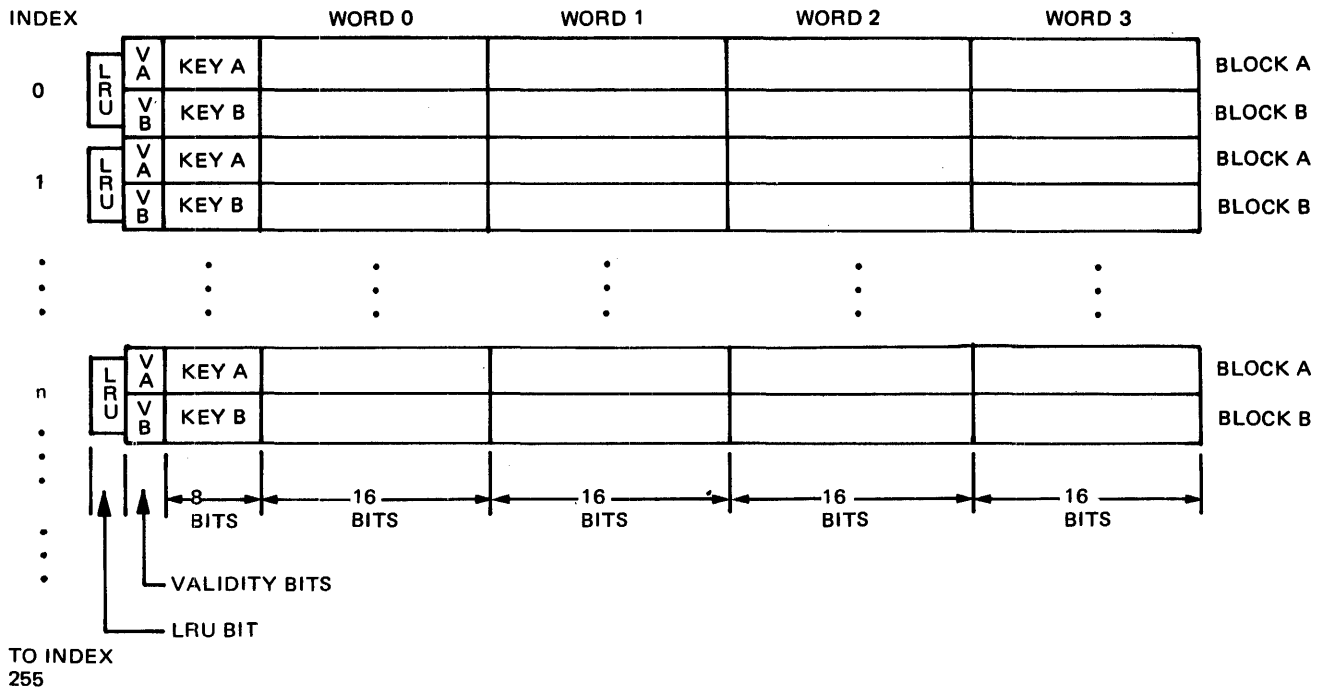
Parity Bit
Two parity bits are associated with Cache. One is used with the information in the Key Store and generates odd parity over the other nine bits (8 information, 1 validity). The other parity bit is associated with the 16-bit microinstruction and generates even parity to detect single-bit errors.

Replacement Algorithm
The algorithm used to determine which block in Cache is to be replaced with new micros to resolve a Miss condition. (See LRU, above.)

Validity
A bit in the Cache's Key Field that registers the fact a valid microinstruction was loaded into Cache. This bit is reset (0) when Cache is cleared.

EXAMPLE

Recall the layout of Cache:



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Further, recall the manner in which the address of a particular microinstruction is divided into subfields for use in the indexed associative hashing algorithm, as shown in the A register schema, below

0	0	Key	Index	n n	0 0 0 0
0	1	<2 9>	<10 17>	<18 19>	<20 23>

Bits 0, 1 are unused; bits 20-23 are always zero. nn=00 to nn=11 specifies Word 0 to Word 3.

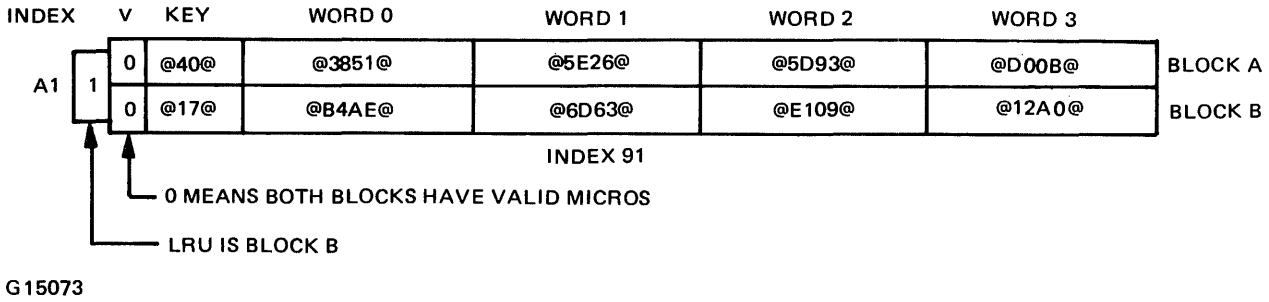
Consider a typical situation in which the A register addresses a microinstruction at address @05D6D0@:

0	0	0 0 0 1 0 1 1 1	0 1 0 1 1 0 1 1	0 1	0 0 0 0

Key = @17@ = 23
Index = @5B@ = 91
Word = 1
(@@ denotes hexadecimal values)

There are two mutually-exclusive possibilities: (1) the micro is already in Cache, or (2) the micro is not in Cache and must be loaded from S Memory.

Case (1) is pictured as follows:



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B 1800 hardware resolves the following questions:

Is either Cache Key equal to @17@ within Index 91?

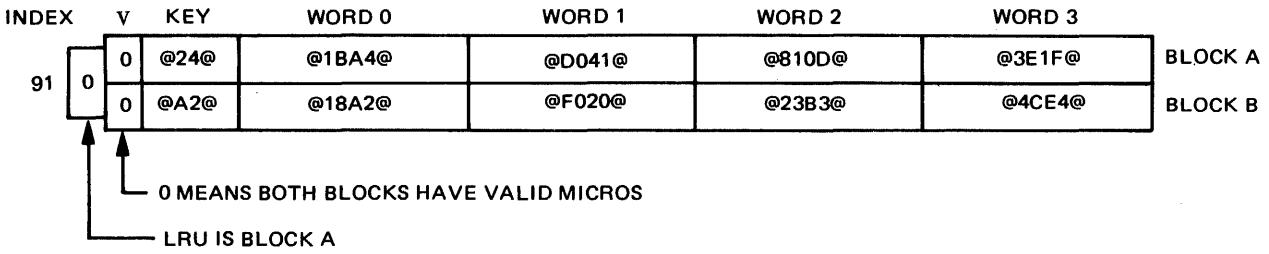
Answer: Yes, Key B has a value of @17@.

Is the validity bit of that block set?

Answer: No, the validity bit for block B of Index 91 is reset (0), meaning that the block contains valid micros.

Therefore, Word 1 of Block B of Index 91 has the desired microinstruction, and that microinstruction is fetched from Cache. This is termed a "hit." Further, the LRU flag is now reset, meaning that Block A (the other block) is the first candidate for overlay.

Now for the case in which the desired micro is not in Cache. Index 91 has the following layout:



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As before, the hardware must ascertain whether the micro is already in Cache:

Is either Cache Key equal to @17@ ?

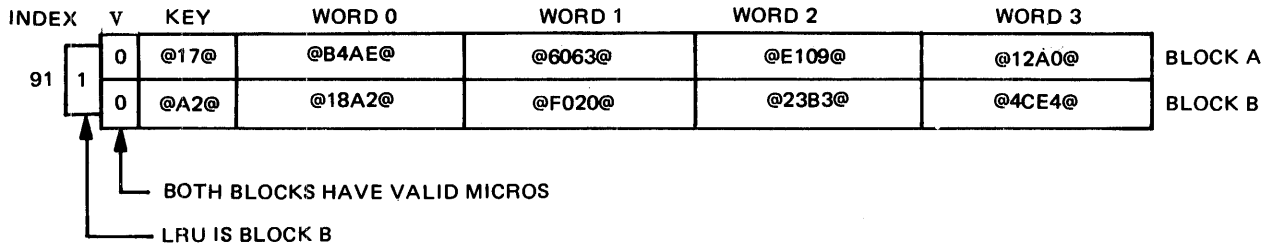
Answer: No. This is the situation termed a "Miss."

Therefore, the hardware loads four microinstructions into Cache Block A, the least recently used block. Loading begins from the A location that hashes into Word 0, in this case, the immediately preceding microinstruction. This relation is expressed mathematically as follows:

S.MEMORY.CACHE.LOAD.STARTING.ADDRESS ←A ∧ @3FFFC0@

where ∧ represents a logical AND operation.

Thus, the four microinstructions residing at absolute memory locations @05D6C0@ through @05D6F0@ are loaded into Cache Block Index 91, and the LRU bit is complemented to make Block B the next in line for overlay:



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I/O SUBSYSTEM

Introduction

In B 1800 systems, the interface between S Memory and the I/O controls is "soft", meaning that I/O controls do not directly access memory. Rather, memory access is provided by firmware routines (GISMO and MICRO.MCP within the standard operating system environment). These routines handle the transfer of commands, data, and result specifiers to and from the I/O controls, and manage the logical I/O functions such as blocking and deblocking. These routines may also call upon the operating system (MCP) to handle specialized functions such as error anaylsis.

NOTE

The interface to the Multi-line Control is an exception. This control accesses memory directly, via a port interchange.

It is the MCP that manages peripherals in a manner that maintains the concept of files which the user perceives as the I/O subsystem. The entire I/O subsystem may be pictured as an interpreter which, rather than intepreting S-code of a compiled program, happens to interpret I/O commands.

To comprehend the intricacies of B 1800-series I/O, a number of concepts must be understood. This section covers these concepts.

I/O Driver

The "I/O Driver" is defined to be a firmware program, typified by GISMO, which acts in the aforementioned manner to interpret I/O instructions and, hence, act as the processor's agent to the I/O subsystem.

I/O Buffers

Associated with every file opened by a user program is one or more areas of memory, termed "buffers", which have the capacity to hold one physical block of information. Such a physical block contains one or more "logical" records which are moved, one at a time, to or from an area of memory the user has declared within his program. These logical records, which are moved upon each Read or Write in the user's program, represent the record concept in the traditional sense.

I/O Descriptor

For each buffer, there is an area in S Memory by means of which I/O to that buffer can be initiated, monitored, and controlled. This area is termed the "I/O Descriptor". Consisting of a number of 24-bit fields, each with a specific meaning, the I/O Descriptor is set up to describe an I/O operation to be performed and to indicate results of the completed I/O operation.

The I/O Descriptor has a number of fields which are useful in describing what is to be done upon completion of an I/O operation or in debugging applications. Seven of these fields are of particular interest in conjunction with the actual I/O process. These fields appear as depicted in figure 2-7 and are described in the list that follows.

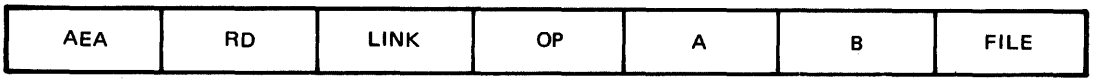

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Figure 2-7. Pertinent I/O Descriptor Fields

AEA
Actual Ending Address; defined to be the ending address plus 1 of the last bit in memory to be processed by a given I/O operation. As with all system-oriented data within memory, it is a binary number.

RD
Result Descriptor; the field of greatest interest to the operating system. By means of a unique bit pattern for each operation, the Result Descriptor indicates that an I/O operation is to be performe on the associated buffer. Conversely, on completion of an operation, a particular bit in the Result Descriptor is set as a flag, and other bits indicate the presence of an I/O exception condition and the particular difficulty that has occurred. The address of the Result Descriptor is termed the "Reference Address." The Reference Address is the normal means by which a particular Result Descriptor is addressed; the address of the Result Descriptor itself is merely Reference Address minus 24. For both Reads and Writes, the Reference Address is returned to indicate which Result Descriptor is being passed to or from the I/O subsystem. In the case of a Read operation, this further serves to identify the particular buffer that is to be filled by the operation.

LINK
The Link field contains the Reference Address of the next I/O Descriptor in the case of a multi-buffer file, or merely its own Reference Address should only one buffer exist. By moving through the Link fields and repetitively dispatching I/O operations, a constant supply of full buffers ideally will be available, minimizing the tendency of a program to be I/O bound, spending an excessive amount of time waiting for I/O operations to come complete before processing can continue.

OP
Represents the operation Code – the precise operation to be performed. Typical operations are Read, Write, Space, Test Status, or Rewind. Additionally this field identifies which peripheral device, of the several that might be connected to a given control, is to perform an I/O operation.

A,B
The A field contains the beginning memory address of the buffer and the B field contains the address one bit past the end of the buffer. Thus the quantity B minus A represents the amount of data to be transferred in an I/O operation, and the end of the buffer is represented by the B address minus 1 (the B-minus-1 address).

FILE
For disk devices, the File Address contains the absolute sector address to which the I/O is to be directed. This field is generally ignored for other devices.

I/O Operation

Initiation

An I/O operation is initiated at the request of the MCP or logical I/O Driver. Input or output is a two-phase operation. First, the operation is started by sending a request to the appropriate control. This process is actually a number of discrete steps:

1. The Op Code is fetched out of the I/O Descriptor and passed to the control.
2. The File Address is likewise obtained and passed. Note that this field is not necessarily used by all controls, but is always sent; this minimizes analysis and decision-making within the firmware and, consequently, maximizes throughput.
3. For an output operation, the actual data is sent.
4. Last, the Reference Address is sent to the control.

Service Request

Ultimately the physical action required of the peripheral device is completed (or aborted), and the device notifies the I/O subsystem that it needs attention by raising a service request. This involves setting a register bit which is periodically examined by the I/O subsystem. (The subsystem has the ability to issue a command causing each channel desiring service to identify itself by setting its own bit in a channel mask.) The highest channel needing attention, represented by the highest set bit in the channel mask, generally is serviced first.

Service is a multi-step process similar to I/O initiation. The sequence is outlined, using Read as the example, as follows:

1. The highest channel needing service is ascertained.
2. The Reference Address is received to identify the I/O descriptor and corresponding input buffer.
3. The data is received.
4. The Result Descriptor is received, indicating any errors that occurred during the operation.

Completion

At this point, a physical I/O has been completed. The I/O Driver causes any job waiting on the I/O operation to be marked as being in a state wherein the logical I/O subsystem can move data in logical units (''records'' in the user sense) to the program. The I/O subsystem is now free to find the next I/O Descriptor to execute.

In summary, an I/O operation involves the transfer of certain information fields in both directions:

<I/O subsystem> <======> <I/O controls>

CA-RC Cycle

To understand how these fields are actually moved, one must be aware of the Command Active, Response Complete (CA-RC) cycle. This series of commands, generated by the I/O Driver, causes a given control to perform data transfer (the CA) and requests that the control acknowledge that the data transfer has transpired (the RC). With one exception, there is a one-to-one correspondence between CA and RC, allowing the I/O subsystem to maintain close contact with the progress of an I/O operation. The one exception involves the transfer of the actual user data for certain high-speed peripherals (disk pack, head-per-track disk, phase-encoded tape), for which a single CA causes a multiplicity of RCs as the data is ''streamed'' to or from the control. The latter, however, is but a conceptual extension to the one-to-one rule.

Each CA-RC cycle involves the transfer of a relatively small amount of information, generally one or two 8-bit bytes. A complete I/O operation takes many CA-RC cycles, each of which, because it is a very basic process, can be conducted at high speed.

It is of utmost importance, in a soft I/O system, to maximize the efficiency of the I/O Driver routines. Efficiency and, consequently, speed, are inversely proportional to the complexity of the task that must be performed. Complexity is reduced in the B 1800 by keeping the sequence and content of fields to be transferred basically identical for all I/O controls. This concept was illustrated earlier when it was noted that the file address field of the I/O Descriptor is always provided, even though it is meaningless for some controls. The fairly rigid protocol for the transfer of information between processor and I/O control allows the I/O subsystem firmware to be relatively "clean", with a minimal number of decisions and, hence, a straightforward path from beginning to end.

Status Counts

For each I/O control, the processor interface logic must follow certain rules. It must, at any point in time, exist in one of precisely 23 well-defined states. Each one of these states, termed a "status count" (STC), indicates a specific condition common to all controls. Not every status count is appropriate for every control; various counts are skipped by various controls.

An I/O operation begins at STC1 and ends at STC23. The precise sequence between STC1 and STC23 is quite similar for all input operations and all output operations to conform to the requirement for minimal decision-making. The status count of a given control can be easily interrogated at any time by the I/O Driver. All the possible status counts are defined in table 2-1.

Table 2-1. Status Counts

STC	Meaning
0	Not ready or control not present.
1	Ready to receive byte 1 of Op code.
2	Ready to receive byte 2 of Op code.
3	Ready to receive byte 3 of Op code.
4	Ready to receive byte 1 of File Address.
5	Ready to receive byte 2 of File Address.
6	Ready to receive byte 3 of File Address.
7	Ready to receive byte 1 of Reference Address.
8	Ready to receive byte 2 of Reference Address.
9	Ready to receive byte 3 of Reference Address.
10	Busy; peripheral is performing the operation.
11	Ready to transmit byte 1 of Reference Address.
12	Ready to transmit byte 2 of Reference Address.
13	Ready to transmit byte 3 of Reference Address.
14	Ready to receive <n> bytes of data.
15	Ready to transmit <n> bytes of data. (n = 1 or 2 bytes depending on the control.)
16	Ready to receive or transmit last byte of data in current buffer load, with more to follow.
17	Ready to receive or transmit last byte of data in last (or only) buffer load.
18	Ready to transmit byte 1 of Reference Address.
19	Ready to transmit byte 2 of Reference Address.
20	Ready to transmit byte 3 of Reference Address.
21	Ready to transmit byte 1 of Result Descriptor.
22	Ready to transmit byte 2 of Result Descriptor.
23	Ready to transmit byte 3 of Result Descriptor.

During the RC portion of most I/O cycles, the control being handled reports its current status in a manner detailed below. This is picked up by the I/O subsystem and used as the basis for determining what will occur during the next CA-RC cycle. Note particularly that the status count thus returned is that which the control is in at that instant. The status count of a control often changes at the end of a CA-RC cycle, and the I/O subsystem cannot deduce the result of the current cycle from the status received. Therefore, the subsystem possesses a command that allows the current status count of the control to be interrogated with no associated data transfer.

Figure 2-8 illustrates the progression of a typical I/O control through the status count sequence. If the control is for an input-only peripheral or an output-only peripheral, then those status counts associated with the other direction are not entered.

Exactly one CA-RC cycle occurs in most status counts, with an exit to the next status count occuring after the cycle. During status counts 14 or 15 (the data transfer state), many CA-RC cycles occur, each transferring one or two bytes of data. (In the case of high-speed peripherals, mentioned earlier, one CA can be followed by many RCs.)

Status count 10 marks the time that the control is busy actually handling the peripheral attached to it. This signifies the end of I/O initiation and exists for an indeterminate period of time. The I/O Driver firmware normally exits from the control flow sequence at this time to perform other operations. When peripheral activity is complete, the I/O control changes from STC10 to STC11 or STC18, depending on the direction of the operation. This change is unknown to the I/O Driver; consequently, the previously mentioned service request bit is set, indicating that at least one control needs service. The I/O Driver periodically checks this bit. Upon ascertaining which control is ready, the I/O Driver enters the second phase of the I/O operation and goes on to normal completion.

I/O and Control Busses

The processor, with the I/O Driver doing the processing, can communicate with the soft I/O controls through the I/O bus, a 24-bit parallel bidirectional interface. An associated 5-bit control bus carries control signals between the processor and the I/O controls and indicates when meaningful data is present on the I/O bus. The interface is depicted in figure 2-9

The processor is always in control of the I/O interface; an individual control can place information thereupon only when given permission by the I/O Driver. This protocol is a direct byproduct of the CA-RC cycle. The CA portion is a specific command indicating what is to be transferred, and the particular control to which this command is directed. In most cases the control is allowed access to the I/O bus during the second half of the cycle (the RC), at which time data or status information is sent back to the processor.

The processor places information on the I/O bus by using a Register Move (1C) or Scratchpad Move (2C) microinstruction with the CMND register as a destination. (CMND is a pseudoregister, being in actuality the I/O bus itself.) This process maintains the information on the I/O bus for two clocks and simultaneously generates the CA signal on the control bus.

Collection of information from the I/O bus is performed using either of the same two (1C or 2C) microinstructions with the DATA register as a source. DATA, like CMND, is a pseudoregister representing the I/O bus. Execution of the microinstruction generates the RC signal on the control bus, indicating that the I/O Driver is collecting data from the I/O bus. If the previous CA involved a command to place data on the bus, the control should be doing so at this time.

Consequently, a typical information transfer between processor and control takes two microinstructions; for example:

```
MOVE X TO CMND
MOVE DATA TO Y
```

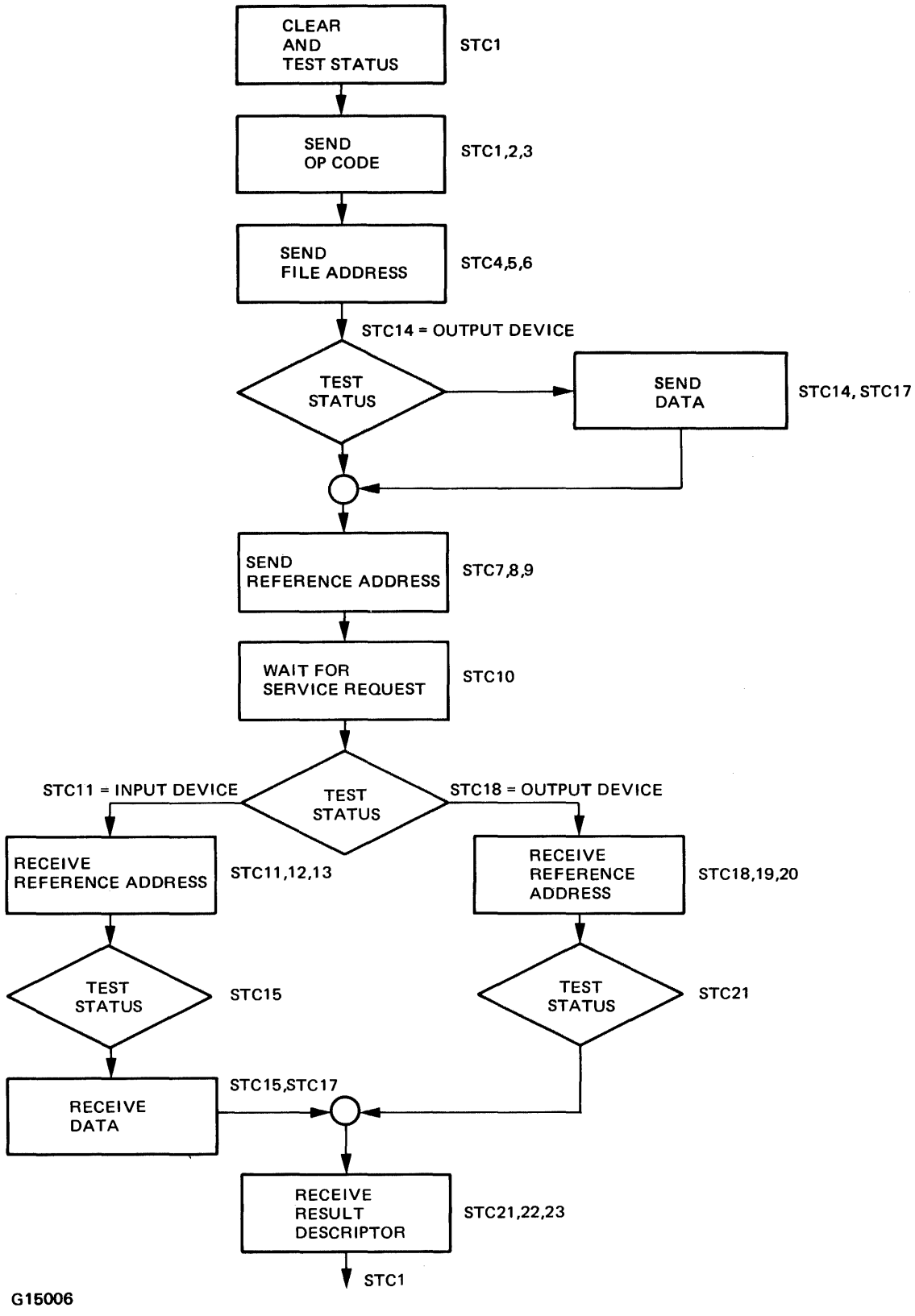

Figure 2-8. Status Count Sequence for an I/O Control

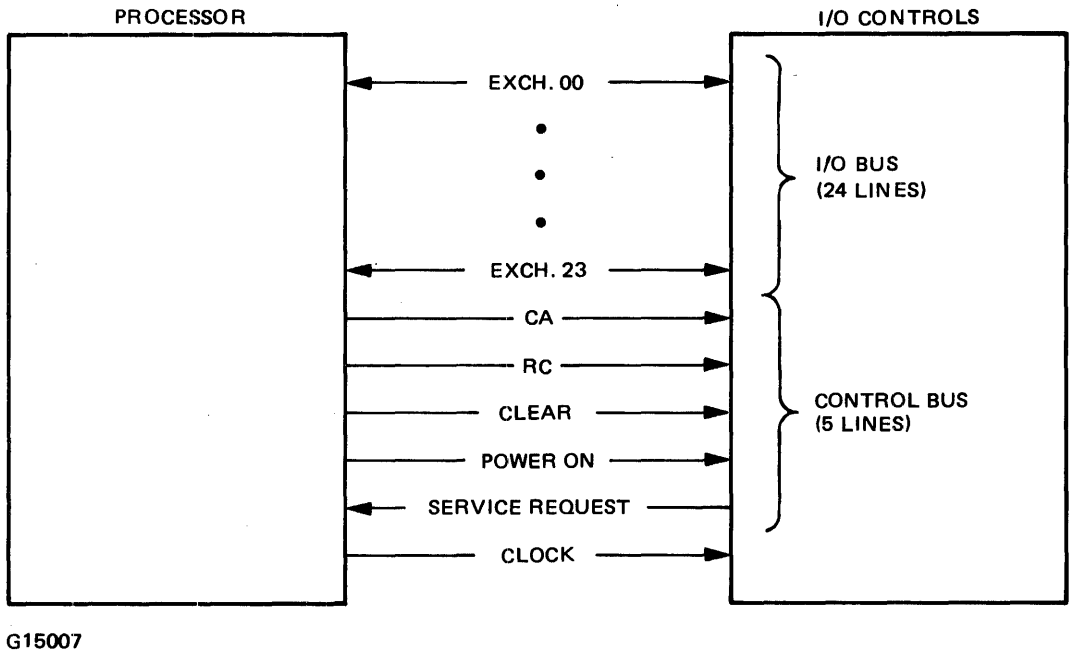

Figure 2-9. Processor-I/O Interface

I/O Commands

I/O commands are listed and described in the paragraphs that follow. Detailed layouts of commands and responses are provided in table 2-2.

Test Status:
The I/O Driver requests, and is returned, the current status count and the device ID. This information enables the Driver to select its next action.

Clear and Test Status:
The control is cleared, meaning that various internal registers and flip-flops are set to predetermined initial values. The results returned are identical to those returned in response to a Test Status command.

Test Service Request:
The I/O Driver requests, and is provided with, a mask of all channels needing service.

Terminate Data:
Used to end data transfer for peripherals with no fixed record size requirement.

Transfer Out A:
Specifies the movement of 1 or 2 data bytes from main memory to the control. Data is sent at CA time; the Result Status is returned by the control at RC time.

Transfer Out B:
Specifies the movement of 3 data bytes from main memory to the control

Transfer In:
Specifies the movement of 1, 2, or 3 data bytes from the control to main memory. Data is sent at RC time. If fewer than 3 bytes are sent, the Result Status is also sent.

Table 2-2. CA-RC Formats

		0000 0123	0000 4567	0011 8901	1111 2345	1111 6789	2222 0123
Test Status	CA	0001	CCCC	XXXX	XXXX	XXXX	0001
	RC	TTTS	SSSS	XXXX	XXXX	XIII	III X
Odd Byte Out	CA	0001	CCCC	XXXX	XXXX	XXXX	0010
	RC	TTTS	SSSS	XXXX	XXXX	XXXX	XXXX
Clear and Test Status	CA	0001	CCCC	XXXX	XXXX	XXXX	0011
	RC	TTTS	SSSS	XXXX	XXXX	XIII	III X
Test Service Request	CA	0001	XXXX	XXXX	XXXX	XXXX	0101
	RC	TTTX	XXXX	MMMM	MMMM	MMMM	MMMM
Terminate Data	CA	0001	CCCC	XXXX	XXXX	XXXX	0110
	RC	TTTS	SSSS	XXXX	XXXX	XXXX	XXXX
Transfer Out A	CA	0010	CCCC	DDDD	DDDD	DDDD	DDDD
	RC	TTTS	SSSS	XXXX	XXXX	XXXX	XXXX
Transfer Out B	CA	0011	CCCC	XXXX	XXXX	XXXX	XXXX
	RC	DDDD	DDDD	DDDD	DDDD	DDDD	DDDD
Transfer In	CA	0100	CCCC	XXXX	XXXX	XXXX	XXXX
	RC	XXXS	SSSS	DDDD	DDDD	DDDD	DDDD
	or	DDDD	DDDD	DDDD	DDDD	DDDD	DDDD
Transfer In Byte Count	CA	0110	CCCC	XXXX	XXXX	XXXX	XXXX
	RC	XXXS	SSSS	VXXX	XXXB	BBBB	BBBB
Transfer Out Byte Count	CA	0111	CCCC	XXXX	XXXB	BBBB	BBBB
	RC	XXXS	SSSS	XXXX	XXXX	XXXX	XXXX

CA Bits: 00-03 = type
04-07 = channel
08-23 = variant

RC Bits: 00-02 = toggles
03-07 = status
08-23 = variant

NOTES

CCCC = channel 0-15
SSSSS = status count
IIIIII = device ID
V = valid byte count sentinel
TTT = toggle subfield of RC word:
All devices: bit 02=1, reverse
Tape devices: bit 00=1, odd byte transferred in
bit 01=1, drive through gap
Reader-sorters: bit 01=1, pocket select.
M...M = channel mask, rightmost bit = 0, leftmost = 15.
D...D = data; each D represents 1 or 2 bytes.
B...B = byte count
X = not used

Odd Byte Out:
Notifies the control that the preceding data transfer consisted of 1, not 2, bytes of data.

Transfer Out Byte Count:
Used in high-speed data transfer; sent by the I/O Driver to tell the control the number of data bytes in the record to be transferred.

Transfer In Byte Count:
Used in high-speed data transfer; sent by the control to tell the I/O Driver the number of data bytes in the record to be read.

Service Request

The Service Request bit is CC(1). This bit is set by any or all controls to indicate a need for service. Service Request is one of the interrupt signals which are OR'ed together to form the ANY.INTERRUPT bit, addressable as bit 2 of the XYST pseudoregister. Every interpreter, prior to executing any S-op, examines ANY.INTERRUPT. If it is set, control is transferred to the I/O Driver. Thus, the Driver, through examination of those bits which are OR'ed to form ANY.INTERRUPT ascertains that Service Request has been raised.

A Test Service Request is then emitted by the I/O Driver. The RC portion of this CA-RC cycle delivers a channel mask of those controls currently awaiting service. Through a Normalize X (3F) microinstruction the highest set channel in the mask is found, signifying the control that is to receive service.

A control is in STC11 or STC18, ready to send the Reference Address, when Service Request is raised. (Exception: Seek Complete result for a disk device control.) This field is accepted, enabling the I/O Driver to locate the I/O Descriptor for which this I/O operation has come complete. A Test Status enables determination of what action is needed by the control, and the operation is completed in the appropriate manner.

Data Transfer

The transfer of data between I/O Driver and control involves one or more iterations, each of which involves exactly one control buffer. Certain peripherals, generally slow speed "unit record" devices such as printers or card readers, have one buffer which always contains the full data record. Other controls have records of indeterminate length; these have multiple buffers which are processed serially by the I/O Driver.

Upon analyzing the channel mask and determining which control is to be serviced, the I/O Driver sends out Transfer Out A commands to obtain the Reference Address. A Test Status is performed; if the control is in STC14 or 15, data transfer is performed in the manner detailed below. Data transfer continues until the control buffer is emptied or until the B address in the I/O Descriptor is reached. If the buffer goes empty, the control switches to STC7 after transfer of the last data character (or characters). In the latter case, a Terminate Data command is sent upon reaching the B Address.

Certain controls do not respond to a Terminate Data command and require data transfer to continue until the end of the control buffer is reached. On output to such devices, the I/O Driver merely sends the required number of blank characters. On input, data received after the B Address is reached is discarded.

Data is transferred in multiples of one, two, or three bytes:

One-Byte Transfer:
This mode is used for unit-record devices, MICR reader-sorters, and the Single Line Control (datacomm). The I/O Driver enters a CA-RC loop, transferring data one byte at a time until the buffer in the control is filled or the B Address is reached. Buffer completion is signified by the control sending or receiving the last byte (STC16 or 17).

Two-Byte Transfer:
Most tape and disk devices transfer data two bytes at a time. The loop consists of a CA-RC cycle during which two bytes are passed together. Disk input or output is terminated when the B Address is reached; the I/O Driver pads the remainder of the buffer, corresponding to the end of that sector, with zeroes. For tape output, the odd-length record case is handled with a special "Odd Character Count" CA-RC cycle telling the control that the previous transfer was only intended to be one byte. On tape input, an odd-length record causes one of the toggle bits in the RC field to be set on the last data transfer.

Three-Byte Transfer:
High-speed peripherals, defined to be phase-encoded tape, disk pack, and head-per-track (5N) disk, use this mode of data transfer. Three-byte data transfer is unique in that one CA may be followed by more than one RC. Prior to entering the data transfer loop, the I/O Driver on an input operation uses a Transfer In Byte Count CA-RC cycle to determine how many RCs are necessary to perform the operation. One CA is followed by the requisite number of RCs, each transferring three bytes of data. For output, the Driver issues a Transfer Out Byte Count CA-RC instruction cycle notifying the control of how many RCs to expect and performs the data transfer with Transfer Out B command during the CA portion of the cycle and as many RCs as are necessary.

Figures 2-10 and 2-11 illustrate the actions of the I/O Driver and the interactions between it and an I/O control for a typical single-buffer device.

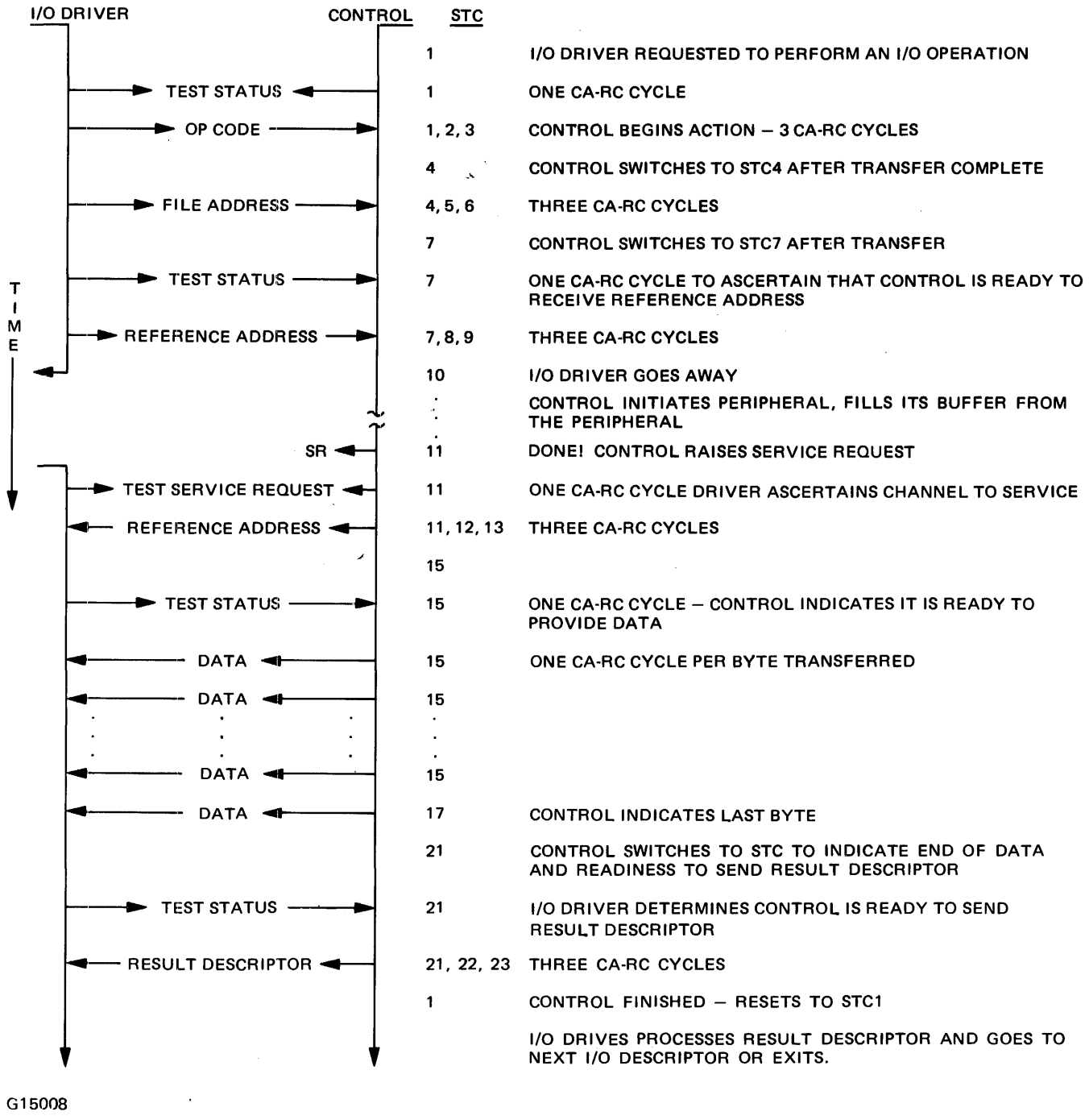

Figure 2-10. I/O Driver-I/O Control Interaction; Read

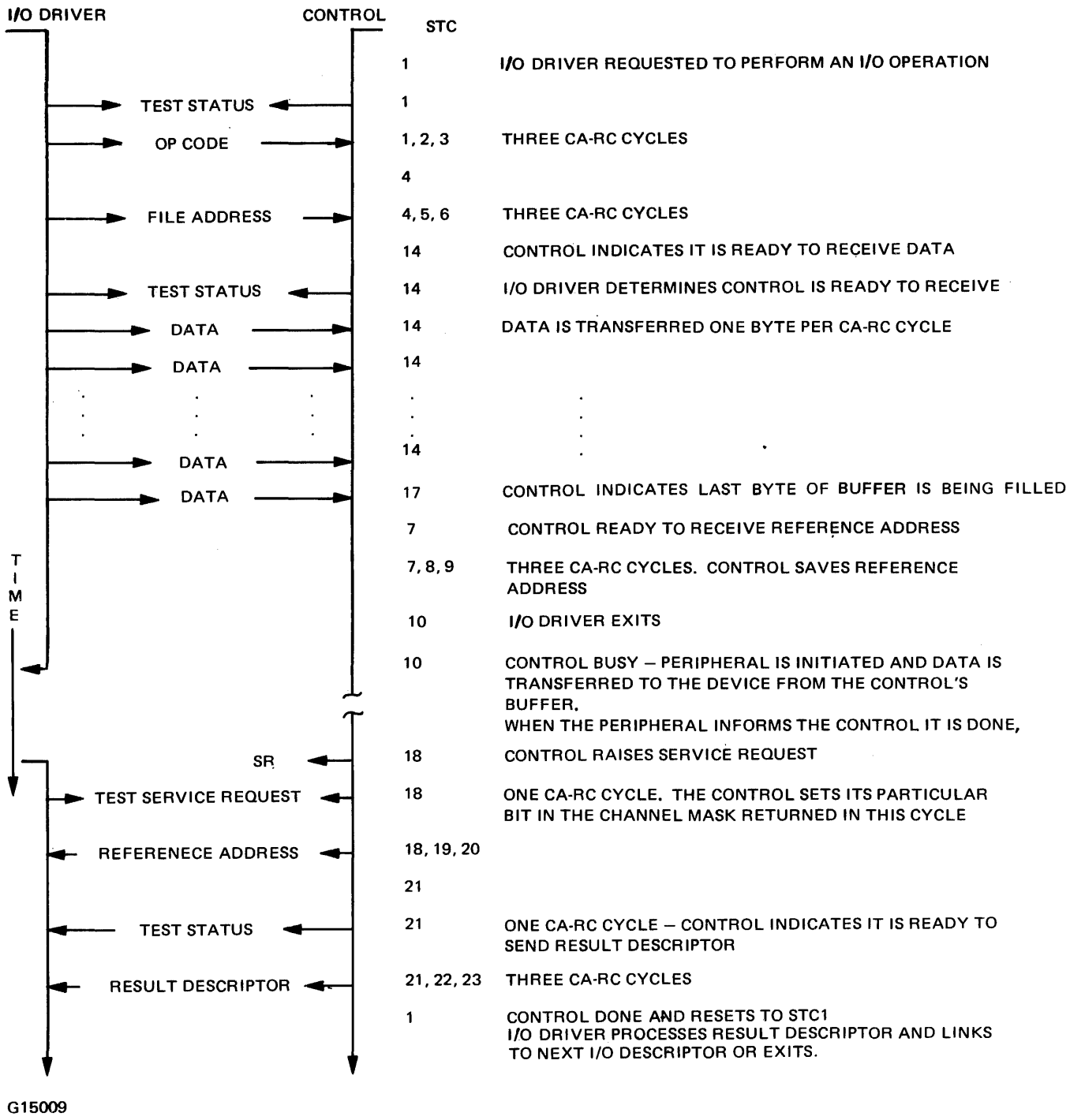

Figure 2-11. I/O Driver-I/O Control Interaction; Write

SECTION 3.
B 1800 CONTROL PANELS

INTRODUCTION

Control facilities for B 1800 systems are grouped on two control panels, the Diagnostic and Maintenance (D/M) panel and the Operator's panel. Panel appearances and locations for each system style (B 1870/B 1860 and B 1865/B 1835) may be seen in figure 2-1 (Section 2, System Elements).

The D/M panel provides facilities for examining and modifying the state of Central Processor. The Operator's panel enables the system operator to perform all normal processor initialization, and operational procedures.

The panels for both system styles are virtually identical, and the descriptions that follow do not differentiate between system styles. The only difference is in the system power switch, a pushbutton on the Operator's panel in B1865-B1835 systems versus a toggle located in the left pedestal (under the console table) in B 1870-B 1860 systems.

OPERATOR'S PANELS

This panel includes switches and indicators used by the system operator to start, interrupt, and clear the processor and to operate the cassette tape drive unit. Both versions of this panel are pictured in figure 3-1

Cassette Tape Drive

The cassette tape drive provides a means for initially "bootstrapping" the processor. The system operator uses it to load stand-alone programs into memory so that they can be executed in the absence of the Master Control Program (MCP). Bootstrapping permits the MCP to be loaded to the system from magnetic tape or disk. This procedure and the associated program are called COLD-START.

Another procedure, with an associated cassette program called CLEAR/START, is used to (1) construct the MCP environment in memory, (2) bring in portions of the operating system from disk, and (3) start the Central Processor executing.

The cassette tape drive is also used to enter "stand-alone" programs (programs that are not run under MCP control), for example, diagnostic routines or experimental microprograms.

Controls and Indicators

The Operator Panel includes five switches. Normally, these are all the controls needed to bootstrap and run the B 1800.

RWD/BOT Pushbutton/Indicator

When RWD is pressed, the drive rewinds the cassette. When beginning of tape is reached, the BOT light goes on.

INTRPT Pushbutton/Indicator

When INTRPT is pressed, bit CC(3) is set. This bit may also be set by firmware. In either case, the indicator lights. This switch does not directly cause an interrupt; system firmware periodically examines bit CC(3), and issues a HALT micro-instruction when CC(3) is set.

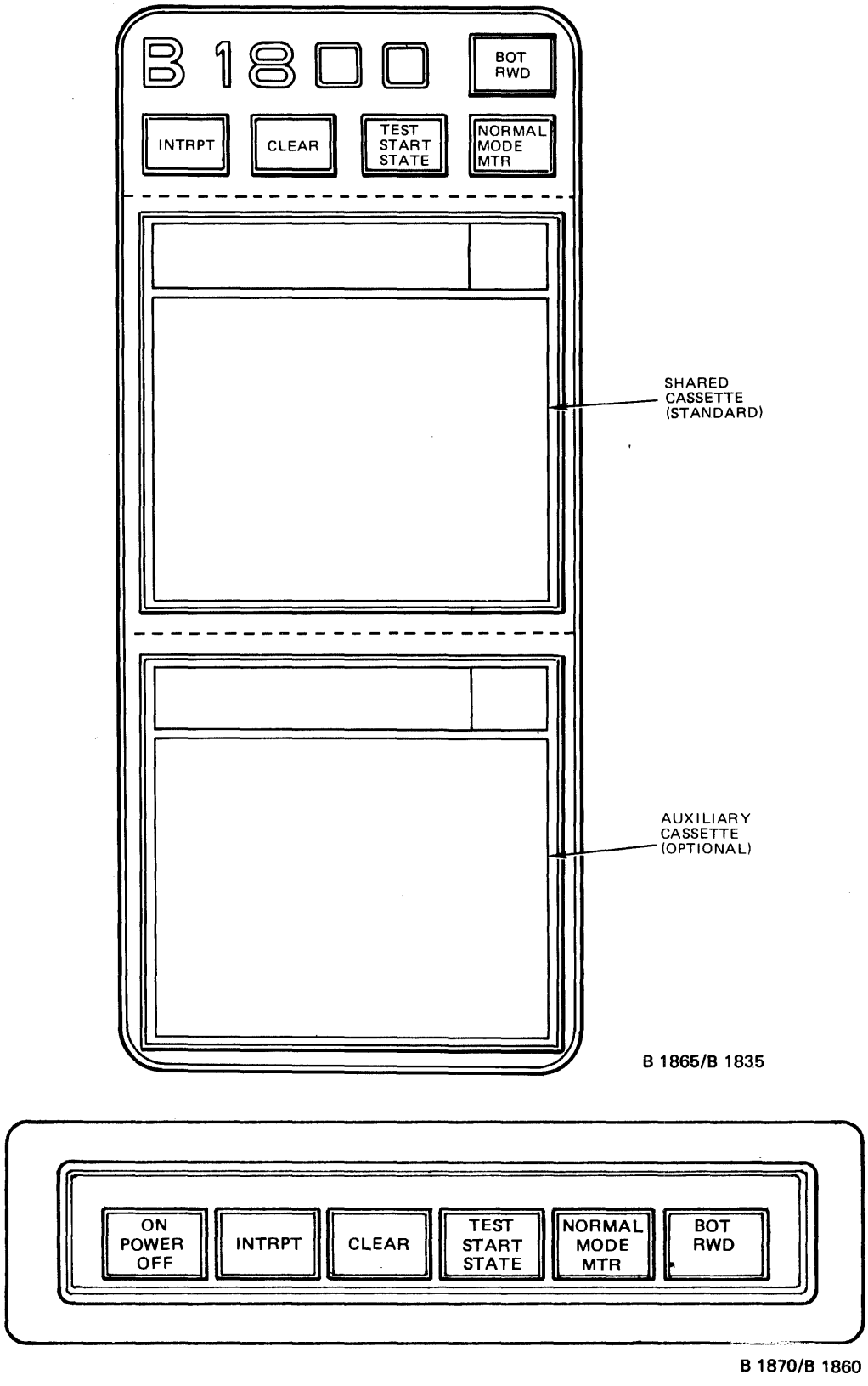

Figure 3-1. Operator (Op) Panels

Mode Pushbutton, NORMAL/MTR Indicator

The MODE pushbutton is used to specify the microinstruction source. Each time the button is pressed, the source is changed, from cassette (MTR) to memory (NORMAL) or vice versa, and the appropriate light goes on.

Microinstructions are fetched from the cassette when the MTR light is on and the CASSETTE SELECT switch (on the D/M panel) is set to SYSTEM. Microinstructions are fetched from Cache or S Memory when the NORMAL light is on.

CLEAR Pushbutton

This momentary pushbutton, which is not active during the RUN state, resets all registers to zero and resets various internal flip-flops to predefined initial values. (CLEAR on the D/M panel is functionally identical.)

START Pushbutton, TEST STATE Indicator

START, a momentary pushbutton, transfers the system from the LOAD/DISPLAY state into the RUN state. If MTR (NORMAL/MTR indicator) is on, a cassette start signal is issued when START is pressed.

The TEST STATE indicator is independent of and unrelated to the START pushbutton. The indicator lights when (1) INTRPT is pressed, (2) the SINGLE MIC/CONT switch (D/M panel) is set to SINGLE MIC, or (3) the MICRO SOURCE switch (D/M panel) is switched out of NORMAL.

DIAGNOSTIC AND MAINTENANCE PANEL

The D/M panel enables the user to examine, analyze, and modify the state of the processor. It includes the following components:

Indicators	24 Main Exchange data lights, STATE light, RUN light, ERROR light, OVERTEMP indicator.
Toggle Switches	24 Data Entry switches, INTERRUPT switch, SINGLE MIC/CONT switch.
Rotary Switches	REGISTER GROUP, REGISTER SELECT, MICRO SOURCE, CASSETTE SELECT.
Pushbuttons	HALT, CLEAR, START, LOAD, INC, POWER (B 1865-B 1835 only).

The D/M panel is pictured in figure 3-2.

Indicators

Data Lamps

These 24 red light-emitting diodes (LEDs) are connected to the 24 lines of the central processor's Main Exchange. In LOAD/DISPLAY state, data in a selected source is automatically moved to the Main Exchange and latched causing its value to be displayed in the data lamps. In RUN state, the lights flicker, indicating that they are continuously monitoring the exchange.

STATE

This LED is on when bit CC(0) (bit 0 of the CC register) is set (1). The MCP sets bit CC(0) when it takes control of the Central Processor; the STATE light notifies the operator that the MCP, rather than a user program, is running.

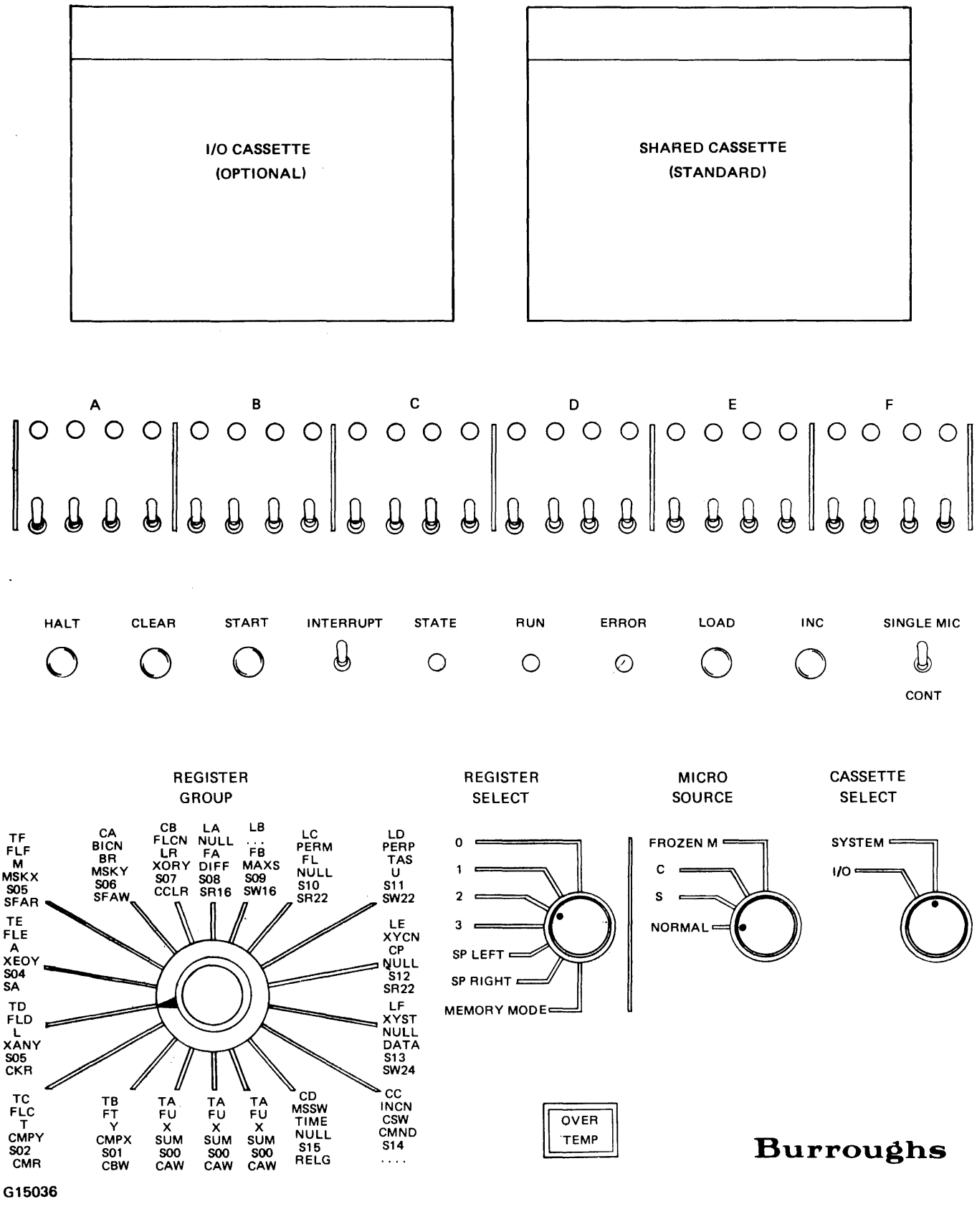

Figure 3-2. Diagnostic and Maintenance (D/M) Panel

RUN

This LED is on when the system is in RUN state.

ERROR

This LED is on when one or more bits in the PERM or PERP registers are true, indicating that an irrecoverable parity error has occurred. (Parity error conditions are defined in the PERM and PERP register discussions in Section 4.) Both registers are reset to zero and the light goes out when START or LOAD is pressed.

OVER TEMP

This indicator goes on to warn that internal airflow is insufficient for processor cooling. If the machine environment cannot be further cooled or if the site is already quite cool, Burroughs Field Engineering personnel should be contacted. When the OVER TEMP light is on, all AC power to the processor is turned off by a relay; the main power switch must be cycled to restore power when the cause of the temperature problem is corrected.

Toggle Switches

Data Switches

These 24 two-position switches, also termed "console switches," are used to represent data. "Up" represents binary 1, "down" is binary 0 When the LOAD pushbutton is pressed, the contents of the switches are entered into a selected register, a scratchpad word, or a Cache or S Memory location.

In situations specified in the discussion of REGISTER GROUP and REGISTER SELECT, these switches are also used to form "masks" that enable processor halts.

INTERRUPT

This 2-position switch is normally set to the down position. When it is up, bit CC(3) is set. (This bit may also be set by firmware.) Switch operation does not directly halt the machine; firmware periodically examines CC(3) and issues a HALT (1F) microinstruction if CC(3) is set.

This action and its results are identical to that caused by pressing INTRPT (Operator's panel). However, this is not a momentary toggle; when CC(3) is cleared by the system, if the toggle is still up, CC(3) is again set to 1. Also, once CC(3) is set, switching the toggle down will not reset it.

SINGLE MIC/CONT

This 2-position switch allows microinstruction execution to be continuous or one-at-a-time.

In the normal mode of Central Processor operation, this switch is in the CONT position. When START is pressed, the system transfers to RUN state. and microinstructions are executed until a console or microinstruction Halt occurs. On receiving Halt, the system transfers to the LOAD/DISPLA state.

With the switch in the SINGLE MIC position, each press of START causes the system to go into RUN state, execute precisely one microinstruction and return to LOAD/DISPLAY state.

Rotary Switches

REGISTER GROUP, REGISTER SELECT

These two rotary switches are used together to provide selection of a total of 112 (7 x 16) possible conditions. The specific entities and functions available with each combination of settings are listed in table 3-7, at the end of this section.

REGISTER SELECT has 7 positions, as identified in table 3-1.

Table 3-1. REGISTER SELECT Switch Labels

Position	Label
1	0 (top)
2	1
3	2
4	3
5	SP LEFT
6	SP RIGHT
7	MEMORY MODE

REGISTER GROUP has 18 actual but only 16 functional positions – the three lowest positions on the dial are identical (note the labels; figure 3-2). Table 3-2 shows the labels for each switch position, reading clockwise from 6 o'clock.

Table 3-2. REGISTER GROUP Switch Labels
Position (clockwise from 6 o'clock)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TA	TB	TC	TD	TE	TF	CA	CB	LA	LB	LC	LD	LE	LF	CC	CD
FU	FT	FLC	FLD	FLE	FLF	BICN	FLCN	NULL		PERM	PERP	XYCN	XYST	INCN	MSSW
X	Y	T	L	A	M	BR	LR	FA	FB	FL	TAS	CP	NULL	CSW	TIME
SUM	CMPX	CMPY	XANY	XEOY	MSKX	MSKY	XORY	DIFF	MAXS	NULL	U	NULL	DATA	CMND	NULL
S00	S01	S02	S05	S04	S05	S06	S07	S08	S09	S10	S11	S12	S13	S14	S15
CAW	CBW	CMR	CKR	SA	SFAR	SFAW	CCLR	SR16	SW16	SR22	SW22	SR22	SW24	....	RELG

Positions 0, 1, 2 and 3 of REGISTER SELECT in conjunction with 0-15 of REGISTER GROUP define all the addressable registers. Note, in table 3-7 at the end of this section, that these combinations form the specification table used by microinstructions to address specific registers.

Positions 4 and 5 of REGISTER SELECT with 0-15 of REGISTER GROUP address each of the 16 left scratchpad (SP LEFT) and 16 right scratchpad (SP RIGHT) words.

REGISTER SELECT position 6, MEMORY MODE, with 0-15 of REGISTER GROUP, enables certain Cache and S Memory operations, plus examination of the Error Log register.

With three exceptions, all of the functions or entities addressed by REGISTER GROUP in conjunction with REGISTER SELECT are implemented when the system is in LOAD/DISPLAY state, by means of the LOAD or INC pushbuttons. (LOAD and INC are discussed later in this section.)

The three exceptions are REGISTER SELECT position 6 in conjunction with REGISTER GROUP positions 4, 5, and 6. When addressed, with the system in RUN, each of these settings can cause a conditional Halt, as defined in table 3-3.

Table 3-3. Switch-Selectable Conditional Halts

RG	RS	Condition for Halt
6	4	Register A is equal to the value (mask) set in the data switches.
6	5	During a READ microinstruction, the FA register is equal to the value set in the data switches.
6	6	During a WRITE microinstruction, the FA register is equal to the value set in the data switches.

Micro Source

This 4-position rotary switch is used to specify the source for microinstructions to be placed in the M register when the system is in RUN state. Table 3-4 defines the labels.

Table 3-4. MICRO SOURCE Switch Labels

FROZEN M	The current microinstruction (in M) is executed repetitively.
C	Microinstructions are fetched only from Cache. When a miss occurs, the system halts.
S	Microinstructions are fetched from S Memory only.
NORMAL	Microinstructions are fetched from Cache. When Misses occur, microinstructions are loaded to Cache from S Memory, then fetched.

Cassette Select

This 2-position rotary switch is used to assign the cassette tape drive to the processor (SYSTEM) or to the cassette I/O control (I/O).

Pushbuttons

HALT

This momentary pushbutton halts the processor (transfers the system from RUN to LOAD/DISPLAY state) upon completion of the currently-executing microinstruction. The next microinstruction is fetched and stored in the M-register.

Certain hardware states may render the HALT Switch ineffective; in such cases, pressing HALT and CLEAR simultaneously will halt the processor.

CLEAR

This momentary pushbutton, which is not active during the RUN state, resets all registers to zero and resets various internal flip-flops to predefined initial values. (CLEAR on the Operator's panel is functionally identical.)

START

This momentary pushbutton transfers the system from the LOAD/DISPLAY state to RUN. Also, if tape mode (MTR on Op panel) is on, a cassette start signal is issued. (The START portion of the START/TEST STATE switch-indicator on the Operator's panel is functionally identical.)

LOAD

Depending on the setting of REGISTER GROUP and REGISTER SELECT, pressing LOAD causes the actions listed in table 3-5 to take place. (The central processor must be in the LOAD/DISPLAY state.)

Table 3-5. Action of LOAD Pushbutton

RG	RS	Action When Load is Pressed
All	0-3	Load contents of data switches into the specified registers. (Exceptions: RG=13, 14, RS=3; see next two entries.)
13	3	(DATA) Load contents of data switches into the I/O bus and issue Response Complete (RC).
14	3	(CMND) Load contents of data switches into the I/O bus and issue Command Active (CA).
All	4,5	Load contents of data switches into the specified Scratchpad location.
0	6	(CAW) Load contents of the rightmost 16 data switches into the Cache Block A location specified by the A register and increment A by 16.
1	6	(CBW) Load contents of the rightmost 16 data switches into the Cache Block B location specified by the A register and increment A by 16.
9	6	(SW16) Load contents of the rightmost 16 data switches into the S Memory location specified by the FA register and increment FA by 16.
11	6	(SW22) Load 16 data bits plus 6 check bits plus current parity from the data switches into the S Memory location specified by the FA register; increment FA by 16. Data switch settings must follow the format described in the discussion of the Diagnostic Read/Write Memory (11D) microinstruction in Section 5.
13	6	(SW24) Load contents of all 24 data switches into the S Memory location specified by the FA register.
2	6	(CMR) Display the contents of the Cache location specified by the A register in the rightmost 16 console lights. If the value of A results in a Cache hit, increment A by 16.
3	6	(CKR) Display the Cache Key appropriate to the location specified by the A register. Display format is identical to that specified in the Diagnostic Cache Read Keys variant of the Read Write Cache (7E) microinstruction described in Section 5. Increment A by 16.
8	6	(SR16) Display in the rightmost 16 console lights the contents of the S Memory location specified by the FA register; increment FA by 16.
10	6	(SR22) Display the contents of the S Memory location specified by the FA register. Include the 16 data bits plus 6 check bits and parity. Readout is in the format described in the discussion of the Diagnostic Read/Write Memory (11D) microinstruction in Section 5. Increment FA by 16.
12	6	(SR24) Display the 24 bits in the S Memory location specified by the FA register.
15	6	(RELG) Display the contents of ELOG. ELOG is the Error Log register.
8	6	(CCLR) Clear Cache.

INC

INC (increment) is a momentary pushbutton that enables the FA or A register to be incremented by specified amounts. REGISTER SELECT must be set to MEMORY MODE (position 6), REGISTER GROUP specifies the register to be incremented and the amount of the increment. Possible actions are shown in table 3-6.

Table 3-6. Action of INC (Increment) Pushbutton

RG (RS=6)	Action
0,1,2,3	Increment A by 16
8,9,10,11	Increment FA by 16
12,13	Increment FA by 24

REGISTER GROUP/REGISTER SELECT CAPABILITIES

Table 3-5, in the LOAD Pushbutton subsection, indicates use of the REGISTER GROUP/REGISTER SELECT switches to address specific registers and Scratchpad, S Memory, and Cache locations. Table 3-7, below, gives the complete layout of the address capabilities of this combination.

Table 3-7. REGISTER GROUP, REGISTER SELECT Switch Combinations

Register Group	Register Select 0	1	2	3	4	5	6
0	TA	FU	X	SUM[1]	S00A	S00B	CAW
1	TB	FT	Y	CMPX[1]	S01A	S01B	CBW
2	TC	FLC	T	CMPY[1]	S02A	S02B	CMR
3	TD	FLD	L	XANY[1]	S03A	S03B	CKR
4	TE	FLE	A	XEOY[1]	S04A	S04B	SA[2]
5	TF	FLF	M	MSKX[1]	S05A	S05B	SFAR[2]
6	CA	BICN[1]	BF	MSKY[1]	S06A	S06B	SFAW[2]
7	CB	FLCN[1]	LR	XORY[1]	S07A	S07B	CCLR
8	LA	NULL	FA	DIFF[1]	S08A	S08B	SR16
9	LB	———	FB	MAXS[1]	S09A	S09B	SW16
10	LC	PERM	FL	NULL[1]	S10A	S10B	SR22
11	LD	PERP	TAS[3]	U[3]	S11A	S11B	SW22
12	LE	XYCN[1]	CP	NULL	S12A	S12B	SR24
13	LF	XYST[1]	NULL	DATA[3]	S13A	S13B	SW24
14	CC	INCN[1]	CSW[1]	CMND[3]	S14A	S14B	———
15	CD	MSSW	TIME[3]	NULL	S15A	S15B	RELG

[1] Source only
[2] Active in Run state (conditional mask).
[3] TAS Source only; push or pop of stack inhibited; Write inhibited.
[3] DATA LOAD pushbutton will generate CA.
[3] CMND LOAD pushbutton will generate RC.
[3] TIME Source only; if used as destination, timer resets.
[3] U Neither a source nor a destination from D/M panel.

SECTION 4
REGISTERS

Registers are high-speed data storage fields accessible by microinstructions. Pseudoregisters represent the outputs of certain logic gates and Central Processor subsections and are generally read-only entities. Pseudoregisters, like registers, are directly accessible by microinstructions; therefore, the distinction is generally academic.

In this section, all the registers and pseudoregisters of the B 1800 are described, grouped by function as follows:

general-purpose registers, used solely as storage media and as inputs to the logical, transformational, and arithmetic sections of the Central Processor;

addressing and execution registers, which hold the currently active microinstruction, point to instructions in memory, address data fields in memory, and provide memory protection through bounds checking;

arithmetic/logical registers, which may contain, at any point in time, the results of certain defined manipulations on the data that is in certain of the general-purpose registers at that time;

interrupt and processor-status registers;

scratchpad, a data-storage area possessing qualities of both registers and regular memory;

miscellaneous registers, not conveniently groupable by function.

GENERAL PURPOSE REGISTERS

L

The L register, besides being addressable as an entity, is subdivided into six 4-bit groups termed LA, LB, LC, LD, LE, and LF which themselves may be thought of as registers, being individually addressable. L is generally the register to which the REGISTER SELECT dial on the D/M panel is pointed; through common agreement, all firmware indicates reasons for machine halts through the L register.

L has specific uses in the execution of the Dispatch (1E) and Transfer Control (4F) microinstructions.

The 4-bit registers LA through LF are available for analysis and manipulation using the 4-bit Function Box. Manipulate, Skip, and Bit-test-branch instructions can operate on these registers.

T

Like L, T is divided into individually-addressable four-bit groups TA through TF. Furthermore, besides its usage as a general purpose register, T has a specific role in the Dispatch (1E) and Transfer Control (4F) microinstructions.

T is more flexible than L in that the Extract From T (11C) and Shift/Rotate T (10C) microinstructions can operate on its data.

X and Y

Besides being convenient general purpose registers, X and Y are the prime inputs to the 24-bit Function Box, which provides all arithmetic and logical operations for the firmware. Both registers are capable of comprehensive shift/rotate operations, as is that pseudo-entity, X-concatenated-with-Y.

The X register is the operand of the Normalize X (3F) microinstruction and holds data for Cache Diagnostic Read/Write operations.

The Y register also holds data for Cache Diagnostic Writes, and is the destination register for various Diagnostic Read/Write Memory operations.

The equality or non-equality of X and Y can be tested in the Cassette Control (2E) microinstruction to either stop movement of cassette tape or to cause an instruction on the tape to be skipped.

Note that neither X nor Y is divided into addressable four-bit entities.

TAS and A STACK

The A Stack is a memory structure consisting of thirty-three 24-bit "words". Despite the similarity in names, the A-Stack has no working relationship with the A register. The stack pointer for the A-Stack has 32, not 33, states; the last A Stack element is for internal hardware use only. The A Stack can be accessed only by means of the 24-bit TAS (Top 0f A Stack) register. Moves to TAS result in the current contents of TAS being pushed onto the A Stack. Moves from TAS cause the A Stack to be popped into TAS. Thus, the A Stack is a true last-in, first-out stack.

Aside from its convenience as temporary storage, the A-Stack is typically used for address storage in call/return programming. The Call microinstructions (14C, 15C) cause the value of A (address of the next sequential microinstruction) to be pushed into TAS and then branch elsewhere. The return from a called routine is merely a move of TAS to A, thus causing execution to resume after the point at which that subroutine was called. The depth of the stack permits substantial nesting and/or recursion.

ADDRESSING AND EXECUTION REGISTERS

F

The F (Field Definition) register specifies the address, length, and unit length (defined below) of data fields in main memory. Note carefully that this value represents the address of data on which a microinstruction will operate, not the address of the microinstruction itself.

The F register is a 48 bits long and is referenced as an entity by three microinstructions: Store F Into Doublepad Word (4E), Load F From Doublepad Word (5E), and Swap F With Doublepad Word (4F). More commonly, various registers which are subfields of F are manipulated by microinstructions. The layout of these subregisters is depicted in figure 4-1 as a structure in a typical programming language as well as pictorially.

All these registers are valid sources and destinations.

FA

The FA (Field Address) register is generally used to hold an absolute bit address for a main memory data field. Thus, owing to the 24-bit length of FA, fields at addresses 0 through 16,777,215 can be directly addressed. Practically speaking, the firmware can directly address all of memory.

FB

The 24-bit second half of FA, termed FB, has no specific use as a single entity. It has general use as a convenience in storing or fetching the subregisters en masse from a scratchpad.

FU

The 4-bit FU (Field Unit) register is typically set by an interpreter to indicate the length of the most basic unit in which it will work. For a language such as Fortran, with fields expressed as binary values, FU is set to 0. For a language such as COBOL, with fields in which the data is represented in packed format, FU is set to 4, indicating four-bit "chunks" are the field units. By means of one variant of the Bias (3E) microinstruction, the FU register can be used in setting the CP register (thus affecting basic arithmetic operations of the hardware).

FT

The 4-bit FT (Field Type) register has no specific usage; it may be used by an interpreter to indicate in some sense descriptive information of interest to itself.

FL

The 16-bit FL (Field Length) register describes the length of that field addressed by the FA register. Consequently, data fields may be of any length from zero to 65,535 bits. FL can overflow and will wrap around to zero; underflow, however, will result in FL being left at zero. The F register is shown in figure 4-1.

STRUCTURE	NAME	BIT COUNT
1	F	BIT(48)
2	FA	BIT(24)
2	FB	BIT(24)
3	FU	BIT(4)
3	FT	BIT(4)
3	FL	BIT(16)
4	FLC	BIT(4)
4	FLD	BIT(4)
4	FLE	BIT(4)
4	FLF	BIT(4)

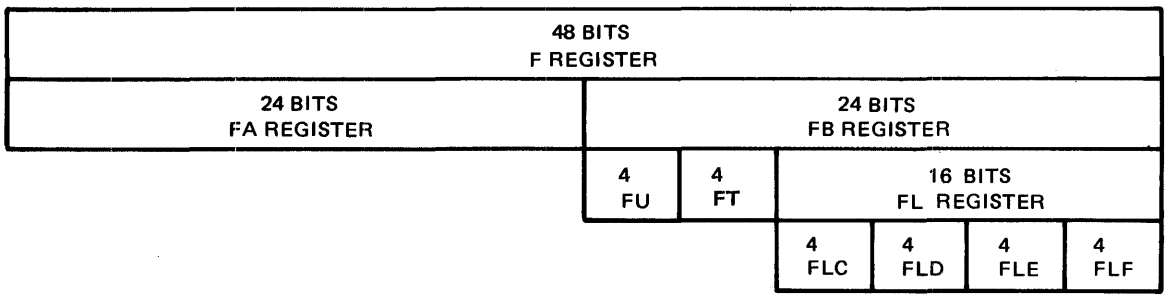

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Figure 4-1. F Register and Subregisters

M

The M (micro) register is a 16-bit (plus odd parity) register which holds the currently-active microinstruction; it is this register which is decoded to cause the proper flow of control within the processor. Thus, instruction fetch on the B 1800 may be globally defined as the process of moving a micro from some storage medium to the M register. Although not individually addressable as distinct registers, the four 4-bit groupings of M are often referred to as the C, D, E, and F portions of M; hardware-oriented people frequently refer to a "3D" micro, which merely means that the first non-zero 4-bit group in the microinstruction is a 3 in the second group (03nn).

M is valid as either a source or a destination. In the latter case, except in TAPE mode, the source being moved to M is OR'ed with the next micro to be fetched. This anomaly provides an efficient means of simulating the equivalent of the "case" capability found in many higher-level languages. The following example, in MIL (Micro Implementation Language, in which the firmware is written), is intuitive; MIL training should be unnecessary. We need only know that Branch Forward (12C) is a microinstruction in which the last 12 bits specify the number of microinstructions to branch from the next micro. The "JUMP FORWARD" command merely causes generation of a branch forward of zero micros, which, when OR'ed with the value moved in from TF, causes the desired jump forward.

```
Code                    Source Instruction
(1525)      MOVE TF TO M % ASSUME TF IS CASE #: 0-3
(C000)      JUMP FORWARD % ZERO, BUT OR'ED WITH ABOVE
(C003)          GO TO CASE.ZERO
(C04D)          GO TO CASE.ONE
(C01F)          GO TO CASE.TWO
(C038)          GO TO CASE.THREE
          CASE.ZERO  %%% CODE FOR THIS CASE FOLLOWS
                     %%% OTHER LABELS ELSEWHERE IN THE SOURCE
```

If TF contains the value 2 in the above example, the C000 micro, when OR'ed with the 2 being moved to M, becomes at that instant a C002 micro causing a branch to the line GO TO CASE.TWO. CASE.TWO is merely a location @1F@ (31) microinstructions from the next microinstruction.

A

The system's "program counter" is the A register, an 18-bit microprogram address register that can address 2**18 = 262,144 microinstructions located in S Memory and/or Cache. Associated with A is a high-speed adder, such that A is automatically incremented when the system is in Run mode, and such that branch operations can be rapidly handled. Wrap-around of A in either direction is permitted. A is addressable as either source or destination.

We must now consider the fact that each microinstruction is precisely sixteen bits; when we move a value to A, for example, that value is in terms of microinstructions, and we need to refer to such absolute addresses in bits. How can this be efficiently handled?

The problem is neatly solved, not by lining up the A register with the rightmost 18 bits of the Main Exchange but, rather, by shifting it left four bits. Thus, when used as a source, the contents appear to the machine to be multiplied by 16. Conversely, moves to A automatically lose the rightmost four

bits, which should be @0@. Note that this phenomenon does not affect operation of the adder associated with A and mentioned above.

When a microinstruction is to be fetched from S Memory, the A register thus refers directly to the desired memory location. Discussion of instruction fetch from Cache is discussed in the section on Cache.

The Transfer Control (4F) microinstruction uses A as a destination.

BR and LR

These two 24-bit registers (Base Register, Limit Register) are used for memory protection and base-relative addressing. Memory protection is achieved by ensuring, upon execution of any microinstruction that references S Memory, that the value of FA lies inclusively within BR and LR. Should the address in FA be out of bounds, CD(2) is set on a Read operation or CD(3) is set on a Write or Swap. Out-of-bounds Reads are merely flagged and not inhibited; out-of-bounds Writes are permitted only if the override flag, CD(1), is set. Note that this memory protection is provided only on a comparison of the initial value of FA with BR and LR. If FL is greater then 1, the adjacent 1 to 23 bits past FA may be referenced without hardware detection. If an attempt is made to reference outside the recognizable bounds of memory (<0 or >MAXS), the error flag PERM(1) is set.

Base-relative addressing is not a function of the hardware. Rather, compilers generate zero-relative data addresses, which, at execution time, are converted into absolute addresses. (The interpreter merely adds the value of BR to this address.) At this point, the memory protection discussed above ensures system integrity. Note that this process also permits data areas associated with individual user programs to be freely moved in memory by the operating system.

U

The 16-bit U register is primarily used for bit-by-bit input from the console cassette unit. It is a source register only. In RUN mode, execution of a microinstruction referencing U will be delayed until all sixteen bits have been filled from cassette. If the data is not processed in time, it will be lost with no indication thereof.

In TAPE mode, wherein microinstructions are fetched from the console cassette, U is automatically moved to M for execution, with one exception. When microinstructions are executed which reference U as a source register, the data in U is processed accordingly and is not treated thereafter as an executable microinstruction. The next micro will be fetched from the cassette. Furthermore, in TAPE mode, one can move data to M, in which case it will be OR-ed with the next microinstruction, as in RUN mode. Branch operations will change the A register as in RUN mode, but the next microinstruction will be fetched from cassette. Finally, the U register is not addressable in RUN mode after a Cassette Control (2E) microinstruction specifying stop has been executed.

MAXS

MAXS (Maximum Size of S Memory) indicates the size of available S memory. It is wired by a field engineer and will generally correspond to the actual amount of S Memory physically installed on a system. The least significant sixteen bits of this 24-bit register are always zero, meaning resolution of memory is in 8K-byte (8192-byte) units.

C

The C (Control) register is a 24-bit grouping of several other registers. C is not addressable as a single entity. It is a compendium of the registers and flip-flops listed and depicted in figure 4-2.

The CPU and CPL subregisters are discussed here. CYF properly belongs in category C, arithmetic/logical registers, and is discussed in that subsection. CC, and CD provide interrupt or processor functions and are discussed in subsection D; CA and CB, really general-purpose registers, are kept with CC and CD for convenience.

CPU

CPU (Control Parallelism Unit) is a 2-bit register accessible only as a destination register by the Bias (3E) microinstruction. Only the least significant bit, CPU(1), is considered. If CPU is zero, the arithmetic unit will treat operands as binary fields; if this register bit has a value of one, operands will be treated as 4-bit packed fields

CPL

CPL (Control Parallelism Length) specifies, in bits, the length of operands being input to the arithmetic unit and may be a maximum of 24. It must be an integral multiple of the unit size as indicated by CPU.

ARITHMETIC AND LOGICAL REGISTERS

CYF

CYF is the Carry Flip-Flop for the arithmetic unit; it indicates, if set, the existence of a carry or borrow beyond the most significant portion of the operands, as defined by CPL. CYF is always input to the arithmetic unit along with X and Y. Hence the bit should be reset after an arithmetic operation before accessing the SUM or DIFFerence of new operands. CYF is usable as source or destination; the Set CYF (6E) microinstruction explicitly sets this bit, based on the results of the previous arithmetic operands.

STRUCTURE	NAME	BIT COUNT
1	C	BIT(24)
2	CA	BIT(4)
2	CB	BIT(4)
2	CC	BIT(4)
2	CD	BIT(4)
2	CP	BIT(8)
3	CYF	BIT(1)
3	CPU	BIT(2)
3	CPL	BIT(5)

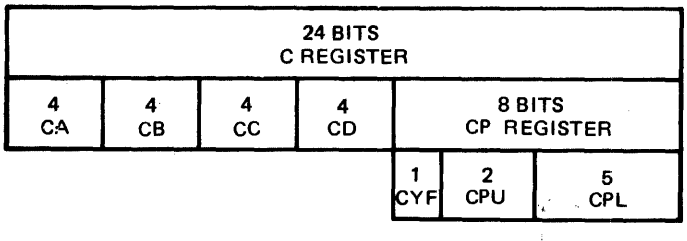

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Figure 4-2. C Register and Subregisters

24-Bit Function Box

The Function Box is composed of a 24-bit Arithmetic Unit and a 24-bit Combinatorial (logical) Unit. Input to this circuitry are the X and Y registers and the CP (CYF, CPU, and CPL) subregisters of C. Results from the Function Box are generated immediately from the input; a move to one of the input registers of the Function Box causes immediate availability of all outputs, even for the next microinstruction. The outputs are used either by moving to a destination register or by testing one of the four-bit condition registers. All outputs are available as source only.

Results of arithmetic operations are not defined if the operand length in CPL is not an integral multiple of the unit size as defined by CPU, nor if CPL exceeds 24. If CPL is less than 24, results appear right-justified with zero-fill.

SUM

Sum is a 24-bit pseudoregister equal to the sum of X, Y, and CYF. The carry-out level is bit (24 minus CPL) of X+Y+CYF if CPL is greater than 1; if CPL=0 then the carry-out level is CYF, the other operands having zero length.

If CPU=00 or 10, the binary sum is produced. If CPU=01 or 11, X and Y are considered to be six 4-bit units and the packed sum is produced. Results are undefined in the latter case if any 4-bit unit exceeds 9 (1001).

DIFF

This 24-bit pseudoregister is equal to X-Y-CYF. The borrow-out level CYD is based on a comparison of all 24 bits of X and Y despite the setting of CPL and is defined as the result of the logical function (X<Y)+CYF(X=Y).

Negative results appear in twos-complement form for binary subtraction (CPU=00 or 10); the difference is in tens-complement form for the BCD case (CPU=01 or 11).

XANY, XORY, XEOY

These three 24-bit pseudoregisters hold the results of the logical functions (X AND Y), (X OR Y), and (X EXCLUSIVE.OR Y) respectively.

CMPX, CMPY

CMPX and CMPY are 24-bit pseudoregisters that denote the Complement of X and Complement of Y, respectively, and hold the result of that logical function.

MSKX, MSKY

MaSK of X and MaSK of Y are 24-bit pseudoregisters hold the least significant CPL bits of X and Y, with zero-fill to the left. Thus, if X=@E12ABC@ and CPL=10, CMPX=@0002BC@, the rightmost 10-bits of X.

BICN

BInary ConditioNs is a 4-bit pseudoregister that indicates the following conditions:

LSUY	CYF	CYD	CYL
0	1	2	3

BICN(0)
LSUY is true if the least significant unit of Y is at its highest possible value, that is, if it denotes the result of the following logical function:

$$((Y_{23})(NOT(CPU)) + (Y_{19,4} = 9)\ CPU)$$

BICN(1)
CYF is available here as a convenience in testing.

BICN(2)
CYD, the borrow-out level discussed under DIFF.

BICN(3)
CYL, the carry-out level discussed under SUM.

XYCN

The 4-bit X-Y-ConditioNs pseudoregister holds the following conditions:

MSBX	X=Y	X<Y	X>Y
0	1	2	3

The Most Significant Bit of X is defined as the state of the bit in X most significant as defined by CPL, and not affected by CPU:

MSBX = If CPL=0 then 0 else X(24-CPL).

The three relational results are based on the binary values of all 24 bits of X and Y; neither CPL nor CPU affect the comparison.

XYST

X Y STates is another 4-bit pseudoregister holding the following relational conditions:

LSUX	INT	X NEQ 0	X NEQ Y
0	1	2	3

LSUX reflects the state of the Least Significant Unit of X, defined analogously to LSUY in BICN.

INT is a convenient interrupt flag equal to the logical OR of the following flags, which are described elsewhere in this section:

INCN(0): Missing port device.
INCN(2): Port interrupt.
CC(1): Real-time clock interrupt.
CC(2): I/O service request interrupt.
CC(3): Interrupt switch.
CD(0): Memory Read data error interrupt.
CD(3): Memory Write/Swap out-of-bounds interrupt. The two relationals are based on all 24 bits of X and Y, uninfluenced by CPL or CPU.

4-Bit Function Box

This 4-bit arithmetic/combinatorial unit of the processor accepts two inputs, one a 4-bit literal within a microinstruction and one a register, also indicated within that microinstruction. The register is one of the following:

CA-CD	BICN	PERM	FU	FT
LA-LF	FLCN	PERP	NULL	
TA-TF	INCN	XYST	RESERVED	

Microinstructions that reference the 4-Bit Function Box include 4-Bit Manipulate (3C), Bit Test Branch Bit Test Branch (4C, 5C), and Skip When (6C). Output of the box can be tested, or directed back to the register that was one of the inputs, provided that register is not a source-only pseudoregister. The outputs of the box include most of the commonly-needed logical function or actions between the two input sources: Set, And, Or, Exclusive Or, Increment, Decrement, and Masked Compares. In the case of the increment or decrement, a microinstruction can be skipped, if a carry or borrow is produced, past the four bits. Likewise, the various masked compares can result in a microinstruction being skipped if the result is true or false.

INTERRUPT and PROCESSOR STATUS REGISTERS

CA and CB

Included here (with CC and CD) so as not to break up the set, CA and CB have no special function and are available as 4-bit general purpose registers, usable as either source or destination.

CC and CD

CC and CD are used for storing processor states, conditions, and interrupts.

CC(0) When set, causes the STATE light on the D/M panel to be lit.

CC(1) Real time clock interrupt, set by the hardware every 100 milliseconds.

CC(2) Indicates an I/O service request by one or more controls.

CC(3) Set when the INTERRUPT switch on the machine is flipped. Note that this does not actually cause a processor halt; firmware periodically checks this bit and, on finding it set, executes a HALT microinstruction to stop the processor.

CD(0) This bit, termed the Memory Read Data Error Interrupt Bit, is set upon occurrence of any of the following conditions:

M-register micro fetch parity error
Cache Key parity error
Cache double hit
Console cassette parity error
Uncorrectable S Memory parity error
PERM register has changed
S Memory field out of bounds
S Memory microinstruction time-out

CD(1) Memory Write/Swap out-of-bounds override.

CD(2) Memory Read out-of-bounds interrupt.

CD(3) Memory Write/Swap out-of-bounds interrupt.

INCN

INterrupt ConditioNs is a 4-bit pseudoregister that reflects the state of the interface between the processor and the port interchange (if the latter is present).

INCN(0) Port device missing flag.

INCN(1) High priority port interrupt.

INCN(2) Port interrupt.

INCN(3) Port lockout.

If a particular machine does not have a port interchange, INCN(1) and INCN(2) are strapped false, and INCN(3) is strapped true. INCN(0) may still be set by the Dispatch (1E) microinstruction, which is the only microinstruction that ever references INCN as a destination. INCN is available as a source register in the same manner as are the other four-bit pseudoregisters.

PERP

The 4-bit Parity ERror Processor register, valid as either source or destination, provides an indication of error conditions occuring within the processor. It may be manually reset in either of two ways: by restarting the processor after execution of a Halt (1F) microinstruction, or by pushing the LOAD button with the processor in the Halt state and REGISTER SELECT switch in MEMORY mode.

The bits of PERP have the following significance:

PERP(0) Cache Double Hit. A Cache Double Hit results when each of the two blocks of a particular Cache Index registers a Hit on the associative Cache key query. This can happen only when manually forced by use of the Write Cache (7E) microinstruction. PERP(0) as well as CD(0), the Memory Read Data Error Interrupt bit, are set. If Cache is enabled as a microinstruction source, the processor halts.

PERP(1) Cache Key Parity Error. Set when a parity error occurs on a Read of the Cache Key store for store for either Block A or Block B. The two blocks are read together, therefore, a parity error on either store will set the bit. Parity is odd, based on the 8-bit Key and one validity bit. After a processor Clear, each key is 0, each validity bit is 1; hence, parity bits are 0. If Cache is enabled as a source of microinstructions, a Cache Key parity error during fetch will halt the processor. Whether or not Cache is enabled PERP(1) as well as CD(0) are set.

PERP(2) M Register Parity Error. This bit is set, and the processor halts, when a data parity error occurs on a micro fetch from either Cache or S Memory. The parity checking will be disabled whenever the M register is used in another manner; for example, in loading micros from cassette or from the console switches, or when a move to M results in OR-ing with the next microinstruction.

PERP(3) Cassette Read Error. PERP(3) is set when an uncorrectable cassette Read error occurs. The processor halts when this occurs in TAPE mode.

MSSW

The 2-bit Micro Source SWitch register is available as either source or destination; all move instructions that apply to 4-bit registers are valid for MSSW; normal justification and truncation results. In RUN mode, this register controls the source of microinstructions in the following manner:

MSSW=00 The source of microinstructions is Cache. When a specified microinstruction cannot be found in Cache (a Miss) the microinstruction is executed from S Memory. Simultaneously, that micro and the next three in the sequence are loaded to Cache. This is the normal mode of B 1800 operation.

MSSW=01 The microinstruction source is S Memory; the Cache is disabled.

MSSW=10 Microinstructions are fetched solely from Cache. A Miss results in a processor halt.

MSSW=11 The M register is "frozen"; the current microinstruction is repeated indefinitely.

MSSW behaves uniquely in that its output is a bit-OR of its contents and the MICRO SOURCE switch (D/M panel). The switch contents correspond in value with its setting, based on the above description. The microprogrammer must be cognizant of this fact when altering the MSSW register. Furthermore, extreme care must be exercised because the microinstruction source affects the processor pipeline; system synchronization relative to the intended order of microinstruction execution can be affected.

PERM

The 4-bit Parity ERror Memory register provides an indication that a problem has occurred in memory. The four bits, set by the processor, signify the following conditions:

PERM(0) S Memory Microinstruction Time-Out. All microinstructions that access S Memory are checked for time-out, defined to be failure to complete in two real-time clock pulses. Real time is between 101 and 199 milliseconds, depending on when the microinstruction commences execution relative to the real-time clock. Relevant microinstructions are Read/Write Memory (7C), Swap Memory (2D), Diagnostic Read/Write Memory (11D), and Dispatch (1E). If memory times out, this bit is set and the processor halts with the stuck microinstruction executing.

PERM(1) This bit indicates, for any memory-accessing microinstruction on either a Read or a Write, that the bounds of usable memory (> MIN (MAXS, physical memory)) have been exceeded.

PERM(2) This bit is set to indicate that there has been a change in the Error Log register.

PERM(3) This bit indicates that an uncorrectable CPU access error to S Memory has occurred. If this occurs during a fetch, a processor Halt results.

When any of the above conditions occur, CD(0), the Memory Read Data Error Interrupt bit, is set.

Error Log

Extensive parity checking within the Central Processor ensures the accuracy of data movement. Single-bit errors are corrected; multiple-bit errors are detected. Abnormalities are reported in the Error Log register and flagged in the PERM register. The operating system maintains a detailed summary of this information for use when needed by Burroughs Field Engineering personnel.

Errors are classified in a priority scheme (low to high):

Single-bit correctable error.
Non-processor (port device) correctable error.
Processor uncorrectable error.

Information of higher priority overwrites uncleared information of lower priority in the Error Log. However, flags for lower priority information remain set to enable the operating system to determine whether overwriting has taken place.

Details of the meanings of the subfields comprising the Error Log register is presented within the discussion on the Diagnostic Read/Write (11D) microinstruction in Section 5.

SCRATCHPAD

Possessing qualities of both register and memory is a group of sixteen 48-bit containers collectively referred to as the "scratchpad" or "scratchpads". The microprogrammer has the freedom to use them as 48-bit entities, denoted as S0 through S15, or, alternatively, as thirty-two 24-bit storage units, referred to as S0A, ..., S15A and S0B, ..., S15B. All are valid as either source or destination, and microinstructions are available that make data transfer to and from registers quite efficient. The scratchpad is generally used to store frequently-referenced data, such as data descriptors and stack pointers; main memory could be used for these purposes, but this would tend to degrade performance.

The only scratchpad with specific meaning is S0B. The first four bits of S0B are a pseudoregister denoted as SFU; the last sixteen bits are called SFL. Note that they correspond in position to FU and FL in the FB register. Comparisons of FU with SFU and FL with SFL affect the operation of the hardware, either automatically or after execution of specific microinstructions.

MISCELLANEOUS REGISTERS

CMND

The 24-bit, destination-only CMND (command) pseudoregister provides a means for transferring commands to devices on the I/O bus. When data is moved to CMND, the processor first generates a CA (Command Activate) signal to the I/O interface and moves the data from the source to the I/O bus. The Register Move (1C), Scratchpad Move (2C) and Shift/Rotate T (10C) microinstructions all can reference CMND. The hardware ensures, for timing purposes, that a CA will occur no sooner than 4 clock pulses from a RC (Response Complete) signal.

DATA

By means of this 24-bit pseudoregister, data may be transferred to or from the I/O bus. When DATA is used as a source, an RC signal is generated to the interface, and 24 bits are accepted from the I/O bus. When DATA is a destination, an RC is generated and 24 bits are moved to the I/O bus. Multiple RC's occur no fewer than 8 clock pulses apart.

FLCN

FLCN is a four-bit pseudoregister denoting Field Length Conditions. One or more bits will be on at any instant, representing the state of comparison between FL and SFL. FLCN is valid as source only. The following conditions are represented when the corresponding bits are set:

Bit 0: FL = SFL
Bit 1: FL > SFL
Bit 2: FL < SFL
Bit 3: FL NEQ 0

NULL

Five NULL positions exist on the REGISTER GROUP dial (see figure 3-2); they all refer to the same register. NULL may be used as a source or a destination. When used as a source, zeroes are supplied; as a destination, the source data is not accepted and merely disappears. The latter phenomenon is of use in popping unwanted data off the A-Stack.

A reserved (empty, denoted by ....) position also exists on the REGISTER GROUP dial. When referenced, results are as described for NULL

CSW

The 24-bit, source-only Console SWitches pseudoregister indicates the position of the 24 toggle switches on the D/M panel. The "up" switch setting corresponds to 1 in the analogous register bit position.

TIME

TIME is a 24-bit register that is incremented every three system clock pulses. TIME is accessible as a source register only by the Register Move (1C) microinstruction; as a destination register it can be used by Move 8-Bit Literal (8C), Move 24-Bit Literal (9C), and Shift/Rotate T (10C). However, TIME behaves uniquely; when used as a destination, it simply resets to zero in all cases. Wraparound of TIME to zero occurs without restriction.

SECTION 5
MICROINSTRUCTIONS

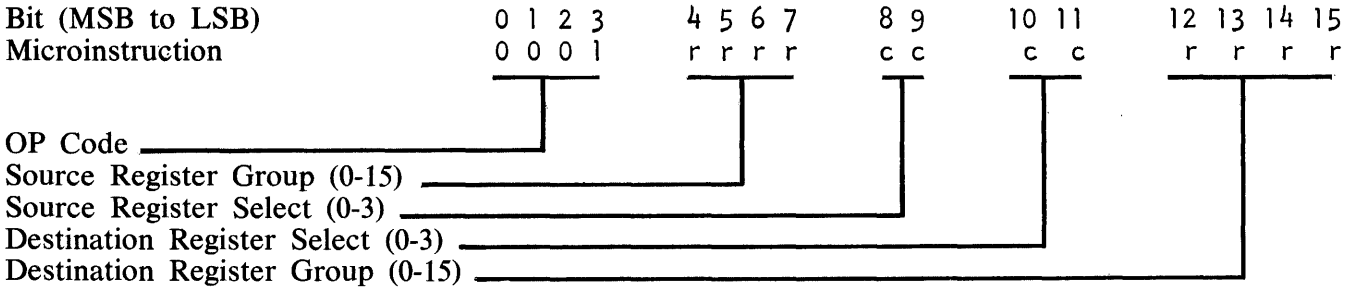
Microinstructions are the interface between software and hardware; thus, they are frequently referred to as "firmware". They represent the only level of programming that can execute directly upon and, hence, manipulate B 1800 hardware. Sequences of microinstructions form the operators (S-ops) that, to the user-language object (or "S-code") instructions, appear to be the system. Consequently, compiler-generated S-code sees an environment, simulated by microinstructions, that is analogous to the traditional hardware environment seen by the object code generated by traditional compilers and assemblers. In summary, microinstructions program the hardware to enable system software and user programs to execute.

All the microinstructions used in B 1800 systems are described in this section. All micros are also summarized in a concise chart provided in Appendix A.

Notation Used in This Section

X(n)	The nth bit from the left of register X.
X_n	Same meaning as X(n).
$X_{m,n}$	Bits m through n of register X.
V	Logical OR.
$\wedge$	Logical AND.
$\oplus$	Logical EXCLUSIVE OR.
$\neg$	Logical NOT.
$\leftarrow$	Assignment operator.
SxA,SxB	Left (A), right (B) halves of Scratchpad X.
n*	The next sequential microinstruction.
@nn@	A hexadecimal (base 16) number. Example: @BD31@
@(1)nn@	A binary number. Example: @(1)01101@
CAT	Concatenation. Example: ABCD CAT 1234 = ABCD1234

1C REGISTER MOVE

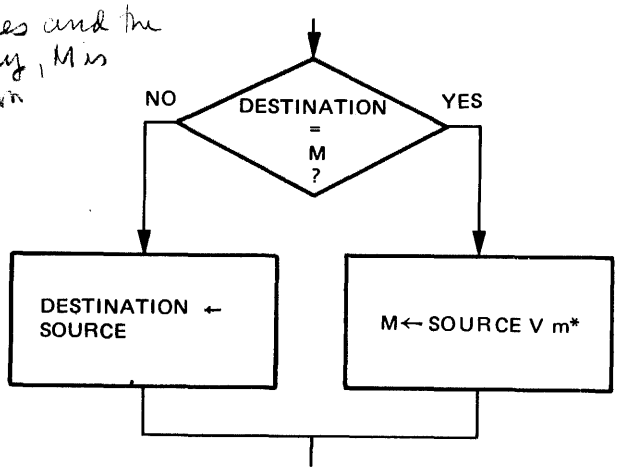


The contents of the source register are moved to the destination register, with left zero-fill or left truncation as appropriate if the two registers differ in size. The source remains unaffected. If the destination register is M, the operation is changed: the source register is bit OR-ed with the next microinstruction fetched to M.

Register Group	Register Select 0	1	2	3
0	TA	FU	X	SUM[1]
1	TB	FT	Y	CMPX[1]
2	TC	FLC	T	CMPY[1]
3	TD	FLD	L	XANY[1]
4	TE	FLE	A	XEOY[1]
5	TF	FLF	M	MSKX[1]
6	CA	BICN[1]	BF	MSKY[1]
7	CB	FLCN[1]	LR	XORY[1]
8	LA	NULL	FA	DIFF[1]
9	LB	-	FB	MAXS[1]
10	LC	PERM	FL	NULL
11	LD	PERP	TAS	U[1,2]
12	LE	XYCN[1]	CP	NULL
13	LF	XYST[1]	NULL	DATA
14	CC	INCN[1]	CSW[1]	CMND[2]
15	CD	MSSW	TIME[1]	NULL

[1] Invalid source.
U is invalid source in STEP mode only

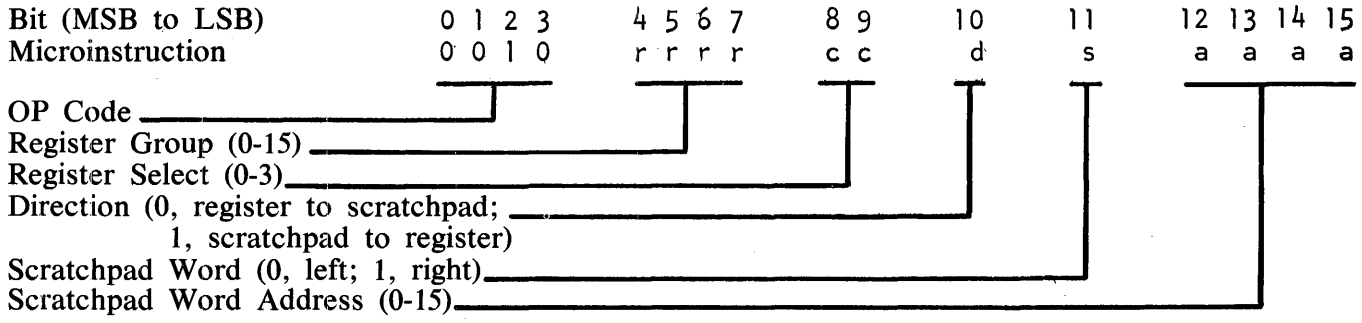
[2] Invalid destination.
If DATA is source, neither CMND nor DATA are valid destinations.



G15077

m* = NEXT MICROINSTRUCTION

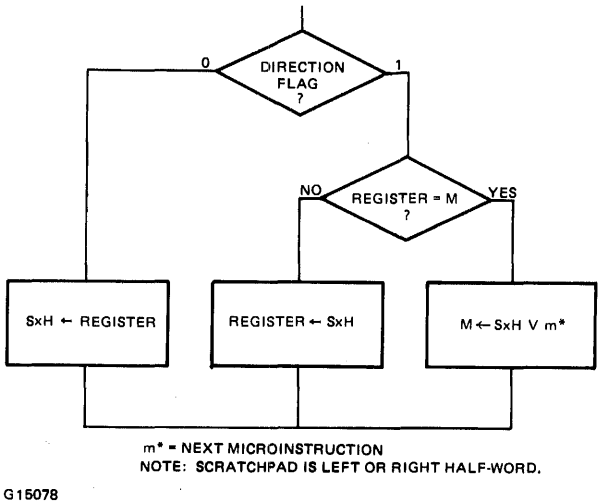
2C SCRATCHPAD MOVE



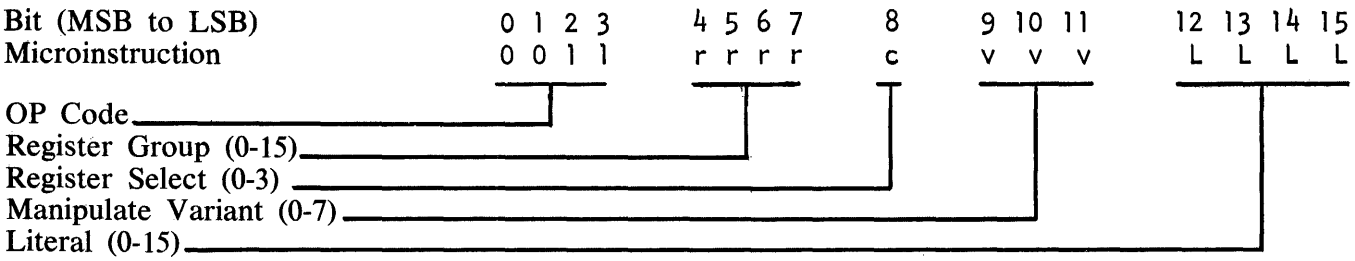
The contents of the source are moved to the destination. Source and destination are determined by the direction variant. Scratchpad Word specifies which half of the doublepad word is used. Left zero-fill or left truncation is performed as appropriate if lengths differ. Contents of the source are unchanged. If the destination register is M, the scratchpad word-half is bit-ORed with the next microinstruction fetched to M.

Register Group	Register Select 0	1	2	3
0	TA	FU	X	SUM[2]
1	TB	FT	Y	CMPX[2]
2	TC	FLC	T	CMPY[2]
3	TD	FLD	L	XANY[2]
4	TE	FLE	A	XEOY[2]
5	TF	FLF	M[1]	MSKX[2]
6	CA	BICN[2]	BF BR	MSKY[2]
7	CB	FLCN[2]	LR	XORY[2]
8	LA	NULL	FA	DIFF[2]
9	LB	-	FB	MAXS[2]
10	LC	PERM	FL	NULL[2]
11	LD	PERP	TAS[2]	U[1,2]
12	LE	XYCN[2]	CP	NULL
13	LF	XYST[2]	NULL	DATA
14	CC	INCN[2]	CSW[2]	CMND[1]
15	CD	MSSW	TIME[1,2]	NULL

[1] Invalid source.
(U is invalid source in STEP mode only)
[2] Invalid destination.

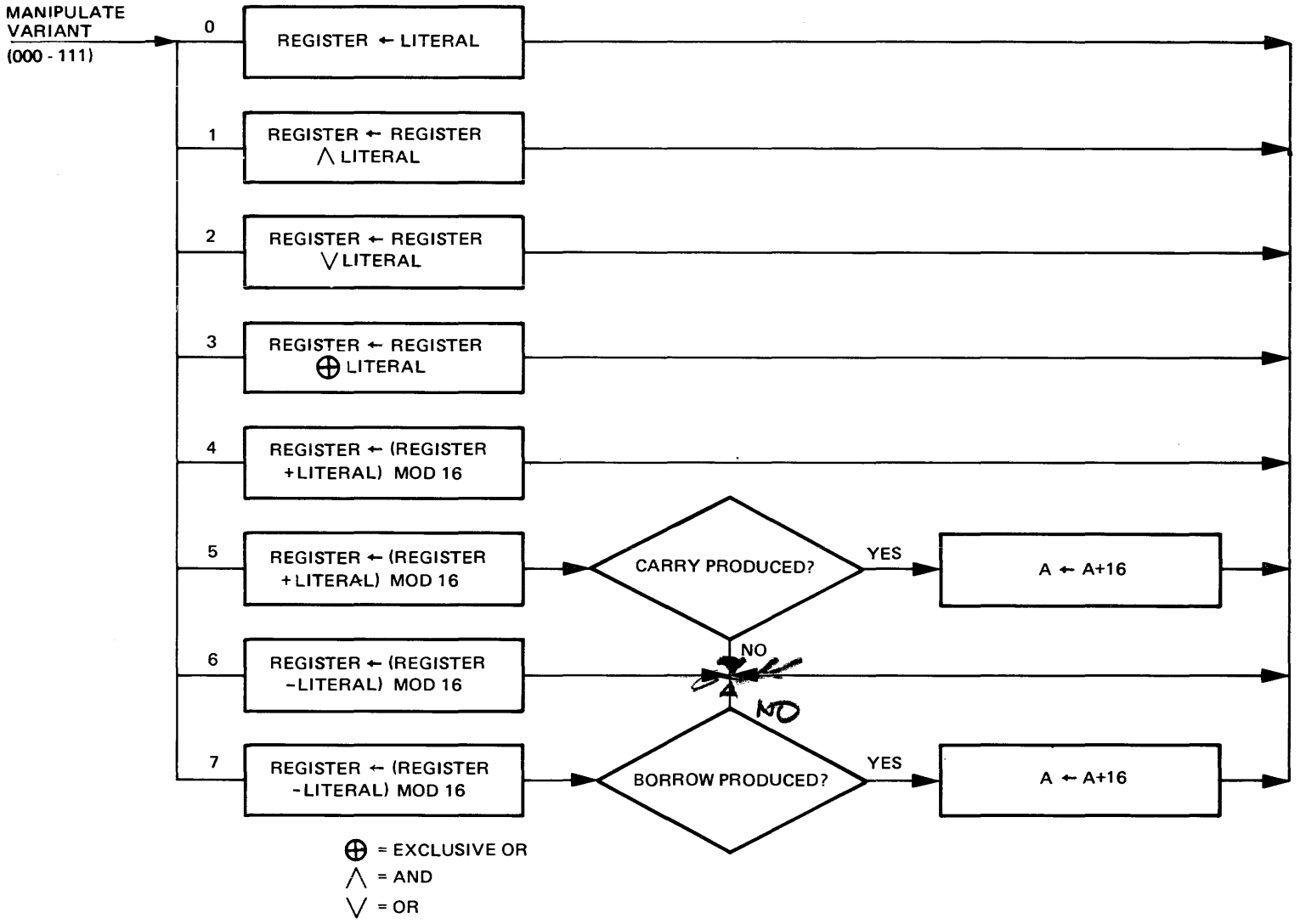


3C 4-BIT MANIPULATE



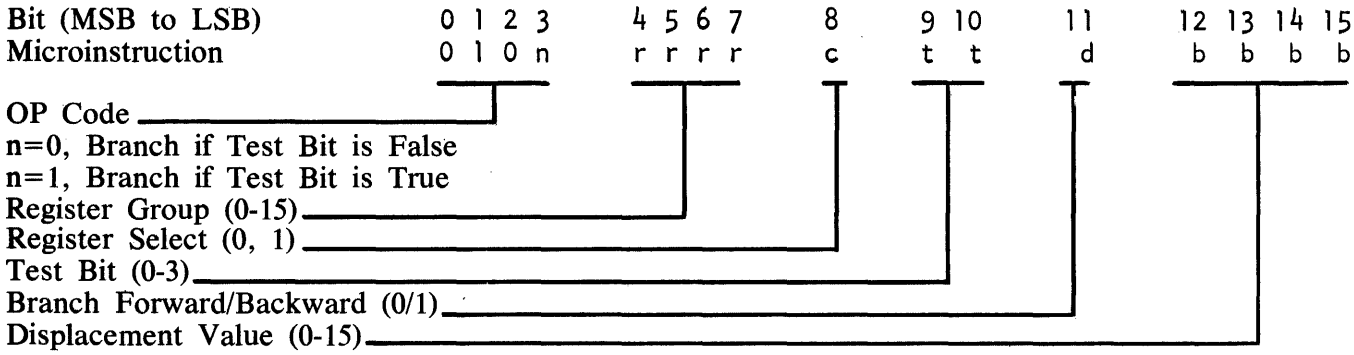
A logical operation is performed with a literal and a four-bit register as operands. Valid operations are ASSIGN, AND, OR, EXCLUSIVE-OR, SUM, and DIFFERENCE. Skip of the next microinstruction can be specified if SUM or DIFFERENCE results in a carry or borrow in the most significant position.

Note that the pseudoregisters BICN, FLCN, XYST, XYCN, and INCN are not changed by this microinstruction, but the carry or borrow is produced if the appropriate manipulate variant is specified. A microinstruction can thus be skipped.



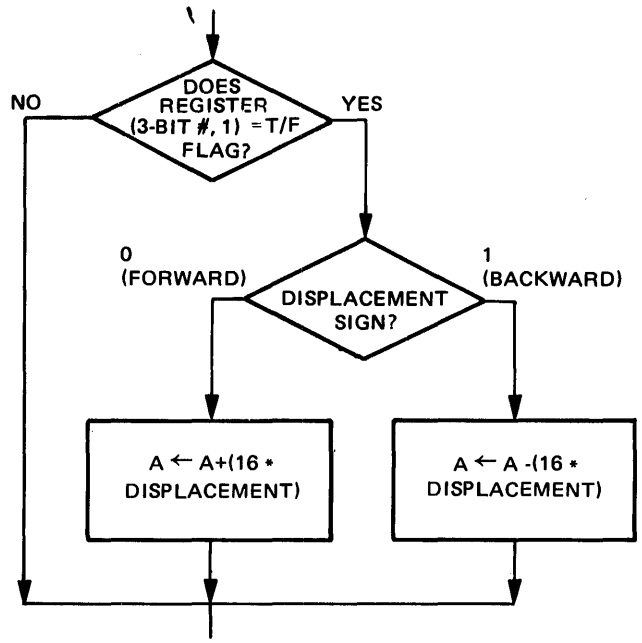
3C 4-Bit Manipulate

4C, 5C BIT TEST BRANCH RELATIVE



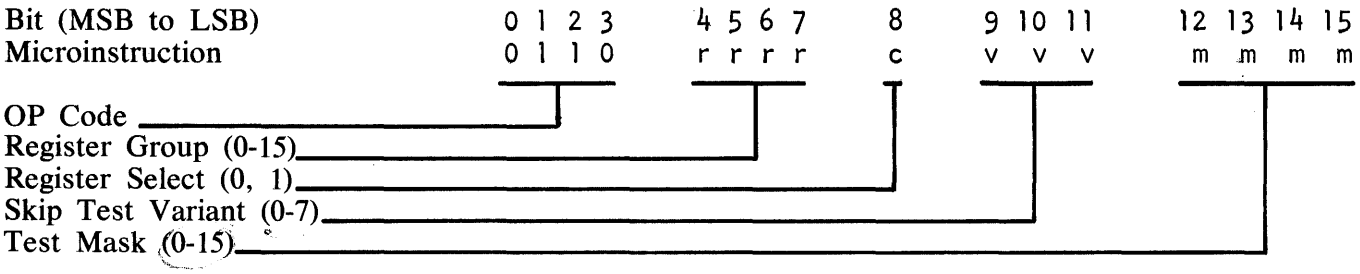
A specific bit, defined by the Test Bit value, within a register is tested (true/false). Depending on the state of n, a branch of the magnitude specified by bbbb takes place in the direction specified by d. The branch is relative to the next microinstruction.

This is often considered to be two distinct microinstructions: 0100 = Branch If False (4C); 0101 = Branch If True (5C).

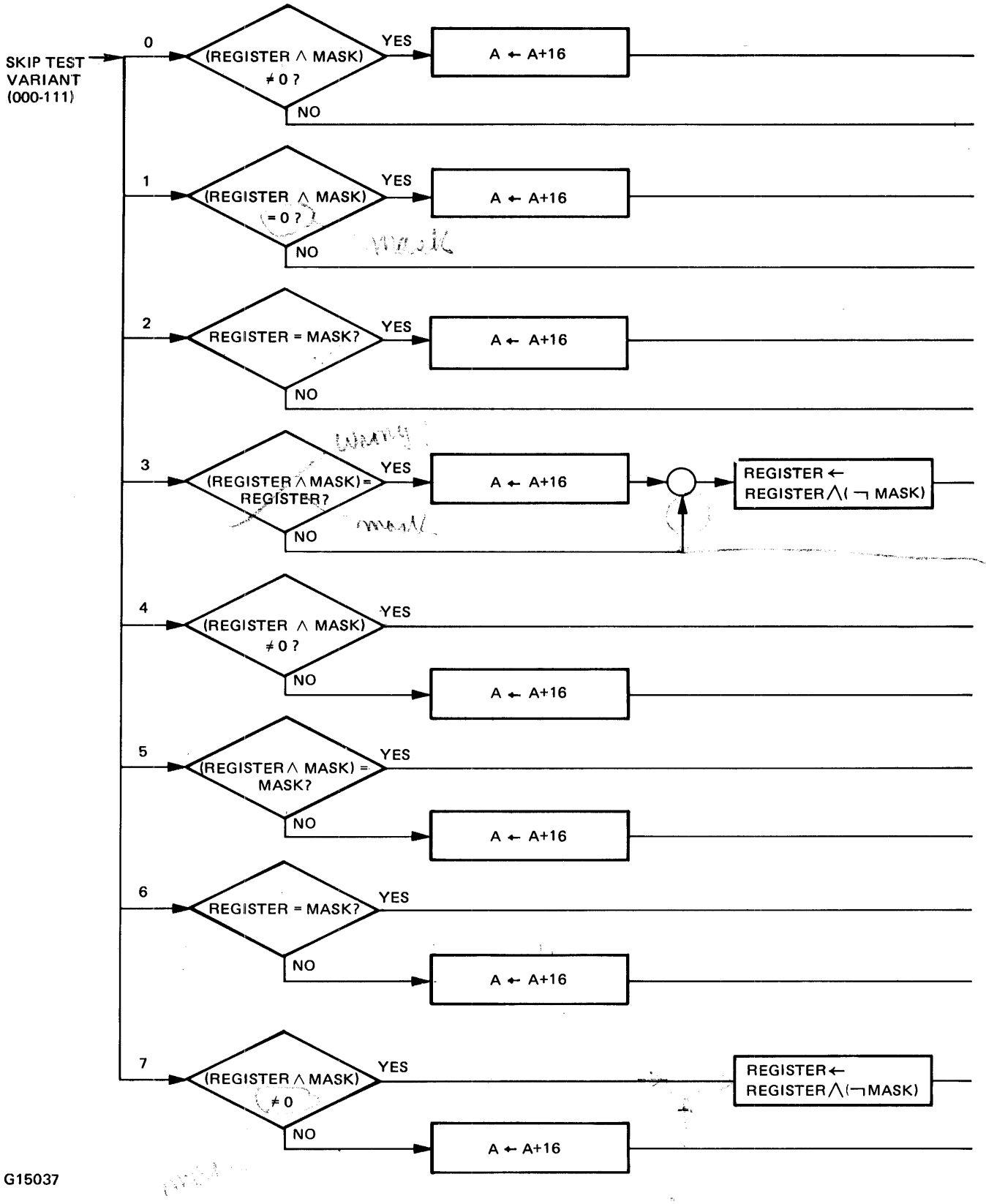


4C, 5C Test Branch Relative

6C SKIP WHEN

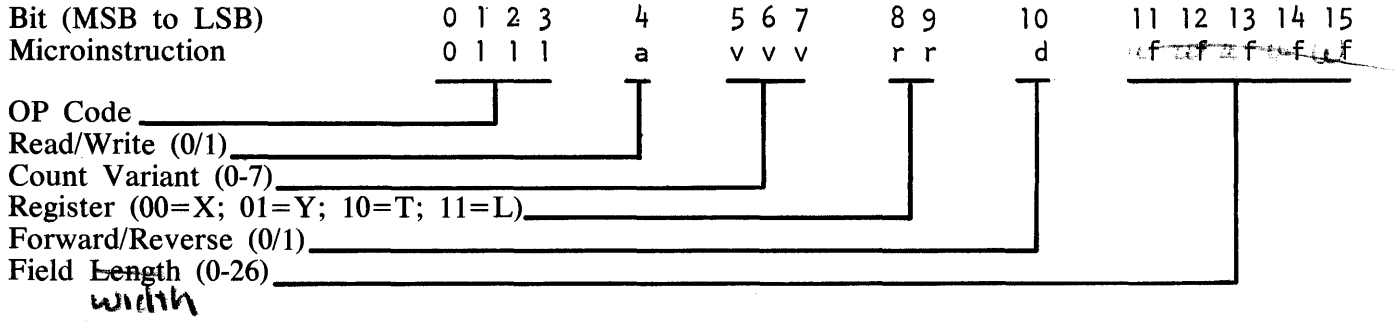


All bits, or only those bits referenced by the 4-bit Test Mask, in the specified four-bit register are tested for no, any, or all ones, as designated by the Skip Test variant. As a result of the test, the next-in-line microinstruction can be skipped. If the Skip Test variant specifies 3 or 7, the masked bits may be reset.


SKIP TEST VARIANT (000-111)
0
(REGISTER ∧ MASK) ≠ 0 ?
YES
NO
A ← A+16
1
(REGISTER ∧ MASK) = 0 ?
YES
NO
A ← A+16
2
REGISTER = MASK?
YES
NO
A ← A+16
3
(REGISTER ∧ MASK) = REGISTER?
YES
NO
A ← A+16
REGISTER ← REGISTER ∧ (¬ MASK)
4
(REGISTER ∧ MASK) ≠ 0 ?
YES
NO
A ← A+16
5
(REGISTER ∧ MASK) = MASK?
YES
NO
A ← A+16
6
REGISTER = MASK?
YES
NO
A ← A+16
7
(REGISTER ∧ MASK) ≠ 0
YES
NO
A ← A+16
REGISTER ← REGISTER ∧ (¬ MASK)
G15037

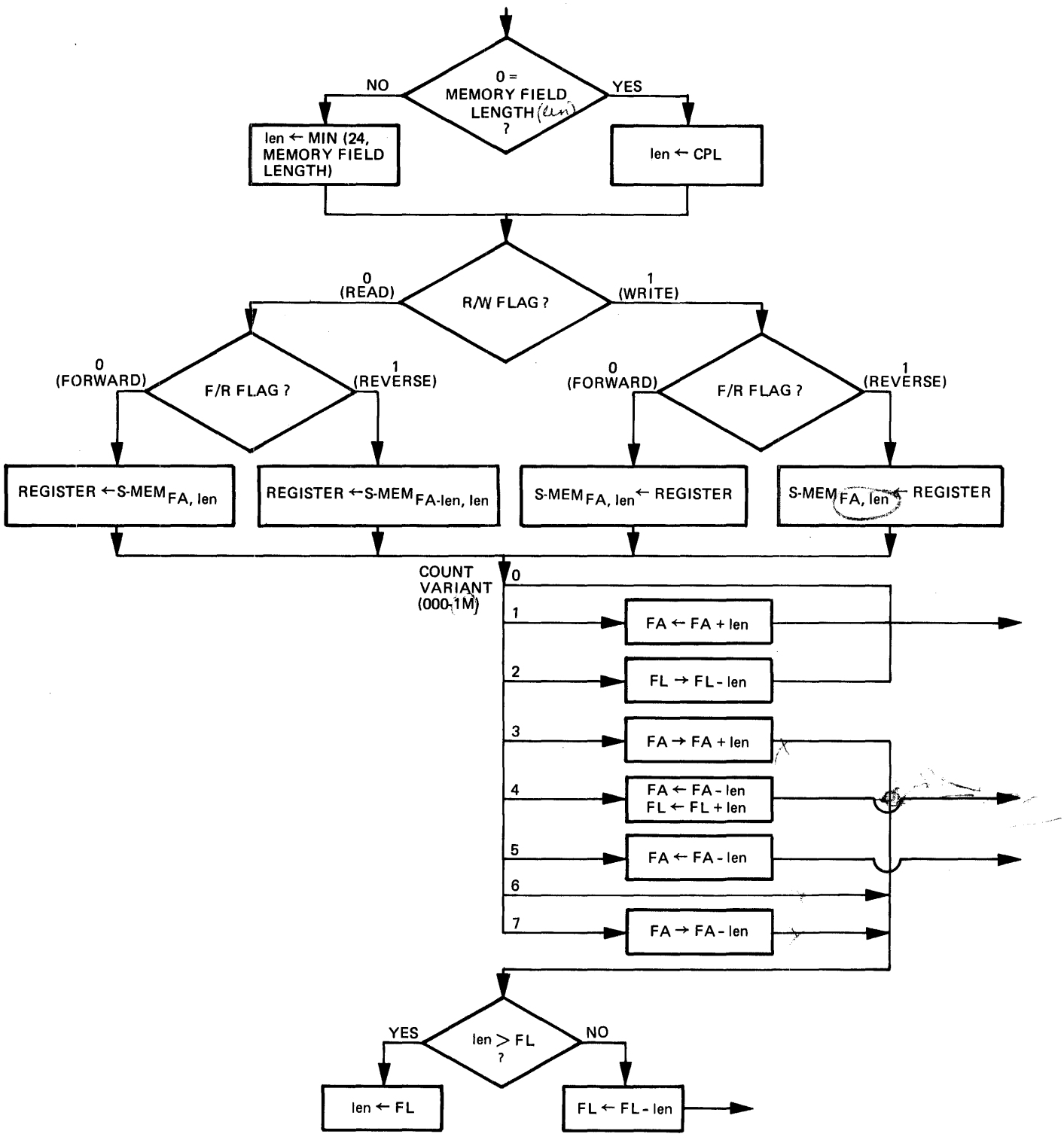
6C Skip When

7C READ/WRITE MEMORY



Data is moved from a register to memory or from memory to a register; the source is unaffected. If the Field Length (data transfer width magnitude, 0-26) is less than 24, data is right-justified with left zero-fill when memory is read; when memory is written, the rightmost number of bits specified by fffff are taken from the register. If the displacement sign is positive (0), FA contains the S-memory field address; if the sign is negative (1) FA addresses the last position plus 1, meaning that the Write will actually occur at FA minus field length.

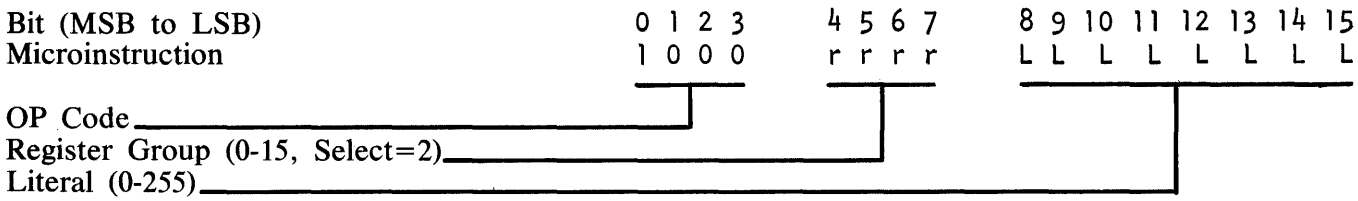
Field lengths of 0, 25, and 26 are special cases. If field length is zero, the value of CPL is used. Values of 25 and 26 are truncated to 24. For Write with field length = 25, correct data (valid parity and check bits) is written and error logging and reporting is suppressed. Other cases are treated normally.



G15038

7C Read/Write Memory

8C MOVE 8-BIT LITERAL



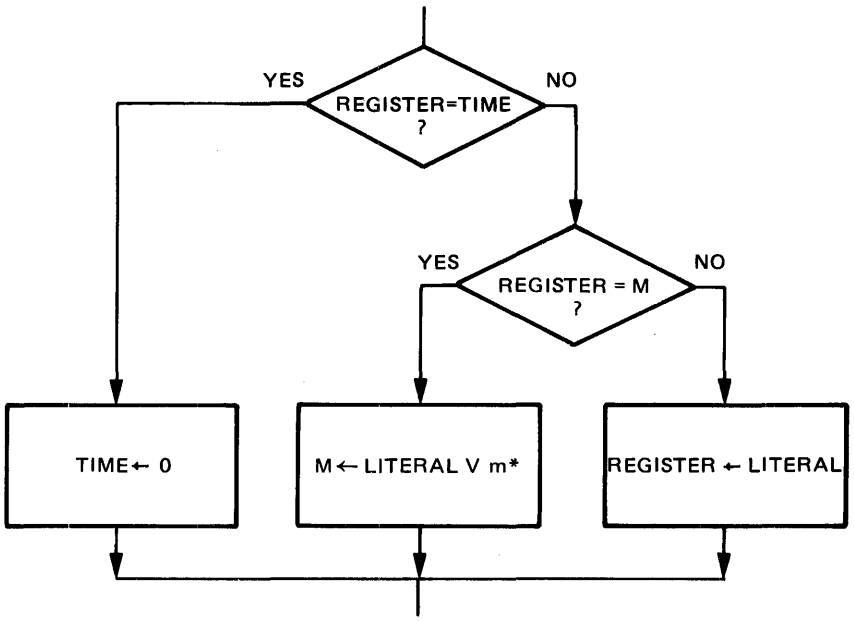
The eight-bit literal within the microinstruction is moved to a destination register. The literal is right-justified with left zero-fill.

Moves to the source-only CSW pseudoregister are invalid. Any move to TIME merely resets that register to zero.

Moves to M are treated differently: the instruction is changed to a bit-OR which modifies the next-in-line microinstruction within the processor; the original microinstruction source (Cache or S memory) is not affected.

Register Group	Register Select 0	1	2	3
0	TA	FU	X[1]	SUM
1	TB	FT	Y[1]	CMPX
2	TC	FLC	T[1]	CMPY
3	TD	FLD	L[1]	XANY
4	TE	FLE	A[1]	XEOY
5	TF	FLF	M[1]	MSKX
6	CA	BICN	BF[1]	MSKY
7	CB	FLCN	LR[1]	XORY
8	LA	NULL	FA[1]	DIFF
9	LB	-	FB[1]	MAXS
10	LC	PERM	FL[1]	NULL
11	LD	PERP	TAS[1]	U
12	LE	XYCN	CP[1]	NULL
13	LF	XYST	NULL[1]	DATA
14	CC	INCN	CSW	CMND
15	CD	MSSW	TIME[1]	NULL

[1] Valid destination

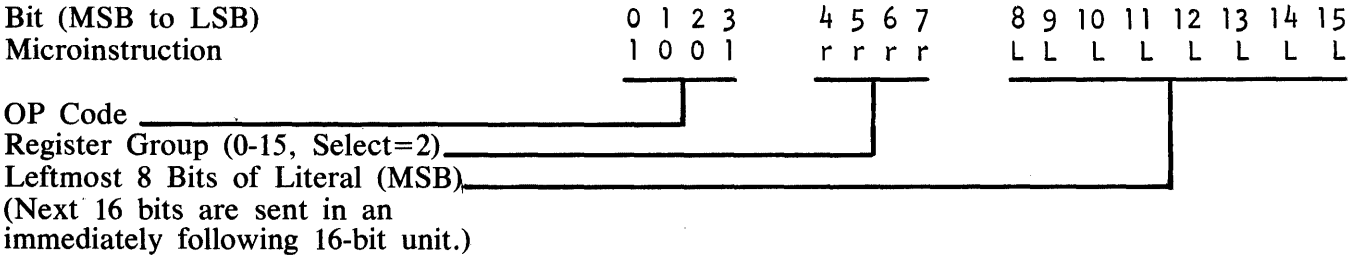


m* = NEXT MICROINSTRUCTION

G15039

8C Move 8-Bit Literal

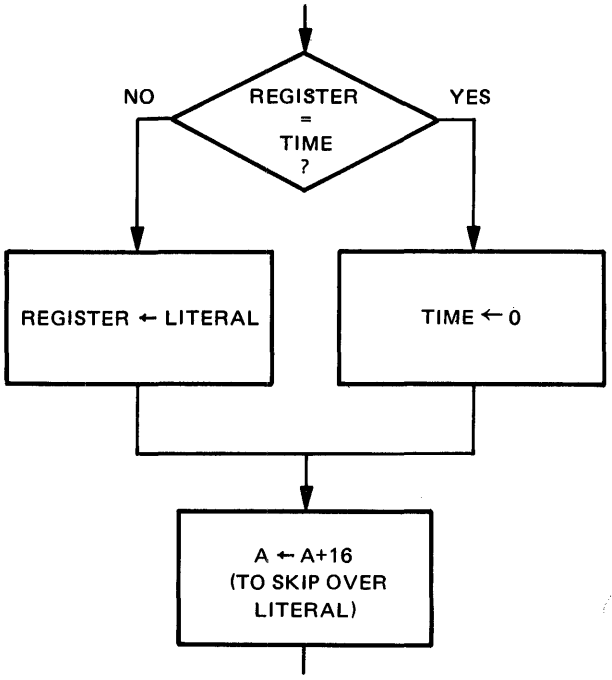
9C MOVE 24-BIT LITERAL



A 24-bit literal, consisting of 8 bits within the microinstruction and the next 16-bit unit, is moved to a register. Left truncation takes place if required. Moves to TIME reset that register to zero; moves to CSW and M are not allowed.

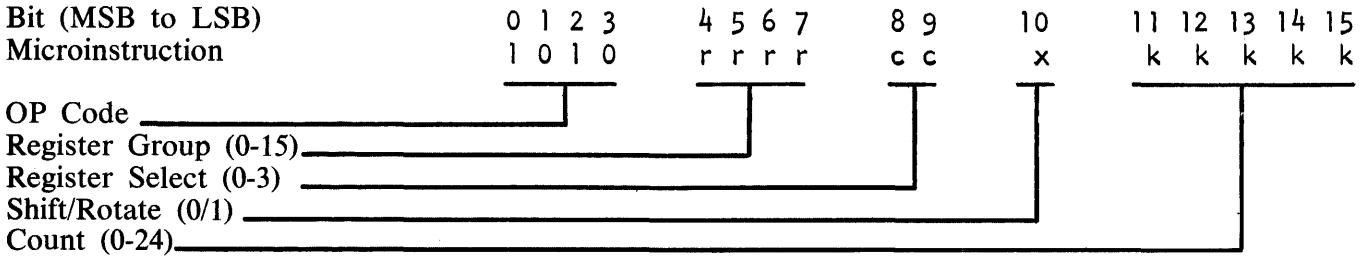
Register Group	Register Select 0	1	2	3
0	TA	FU	X[1]	SUM
1	TB	FT	Y[1]	CMPX
2	TC	FLC	T[1]	CMPY
3	TD	FLD	L[1]	XANY
4	TE	FLE	A[1]	XEOY
5	TF	FLF	M[1]	MSKX
6	CA	BICN	BF[1]	MSKY
7	CB	FLCN	LR[1]	XORY
8	LA	NULL	FA[1]	DIFF
9	LB	-	FB[1]	MAXS
10	LC	PERM	FL[1]	NULL
11	LD	PERP	TAS[1]	U
12	LE	XYCN	CP[1]	NULL
13	LF	XYST	NULL[1]	DATA
14	CC	INCN	CSW	CMND
15	CD	MSSW	TIME[1]	NULL

[1] Valid destination



9C Move 24-Bit Literal

10C SHIFT/ROTATE T

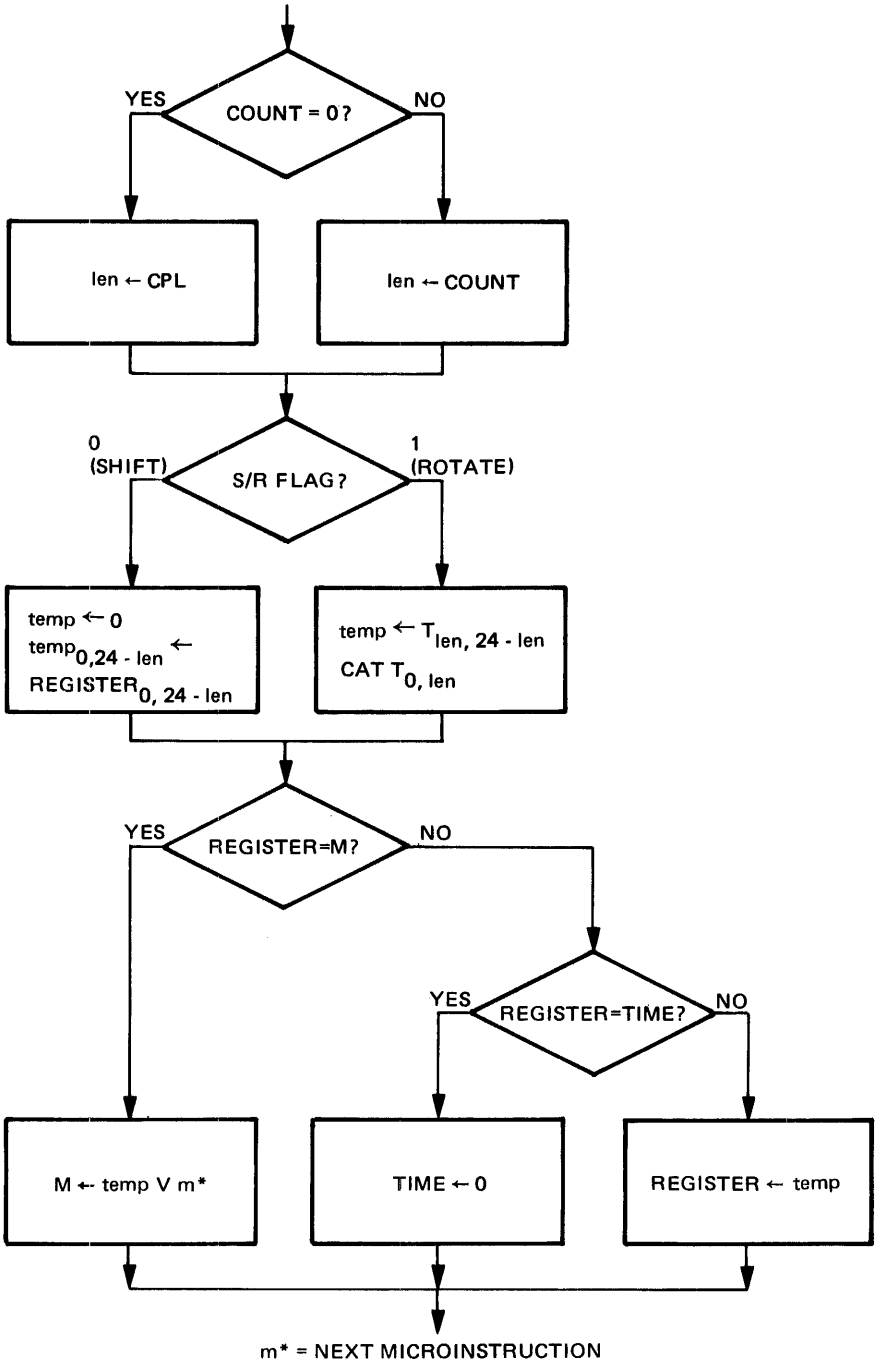


T is shifted/rotated left 1 to 24 positions, as specified by the Count variant, and the 24-bit result is moved to the destination register. T remains unchanged unless it is the destination. Right zero-fill and left truncation occurs for the shift operation. If Count is zero, the value in CPL is used instead. If TIME is the destination, it is reset to zero.

If M is the destination, the operation is changed to a bit-OR of the shifted/rotated data with the next-in-line microinstruction.

Register Group	Register Select 0	1	2	3
0	TA	FU	X	SUM[1]
1	TB	FT	Y	CMPX[1]
2	TC	FLC	T	CMPY[1]
3	TD	FLD	L	XANY[1]
4	TE	FLE	A	XEOY[1]
5	TF	FLF	M	MSKX[1]
6	CA	BICN[1]	BF	MSKY[1]
7	CB	FLCN[1]	LR	XORY[1]
8	LA	NULL	FA	DIFF[1]
9	LB	-	FB	MAXS[1]
10	LC	PERM	FL	NULL
11	LD	PERP	TAS	U[1]
12	LE	XYCN[1]	CP	NULL
13	LF	XYST[1]	NULL	DATA
14	CC	INCN[1]	CSW[1]	CMND
15	CD	MSSW	TIME[1]	NULL

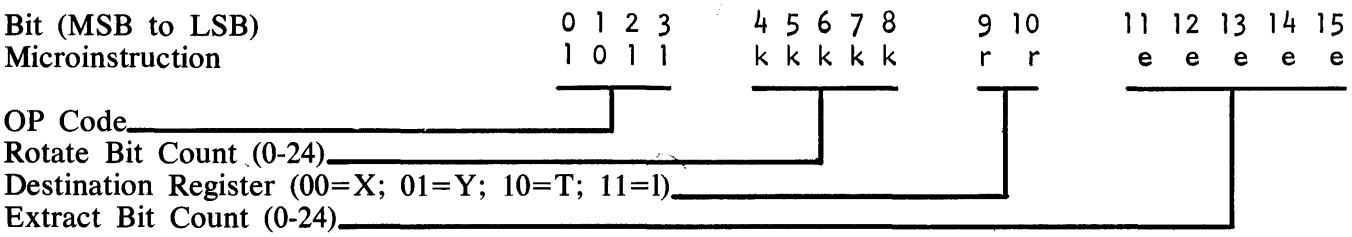
[1] Invalid source.



G15041

10C Shift/Rotate T

11C EXTRACT FROM T



After temporarily rotating T left by the Rotate Bit Count, the rightmost number of bits specified by the Extract Bit Count are moved, right-justified, to a destination register, with zero-fill on the left. The destination register is X, Y, T, or L. The source (T) is unaffected unless it is also the destination.

Example:

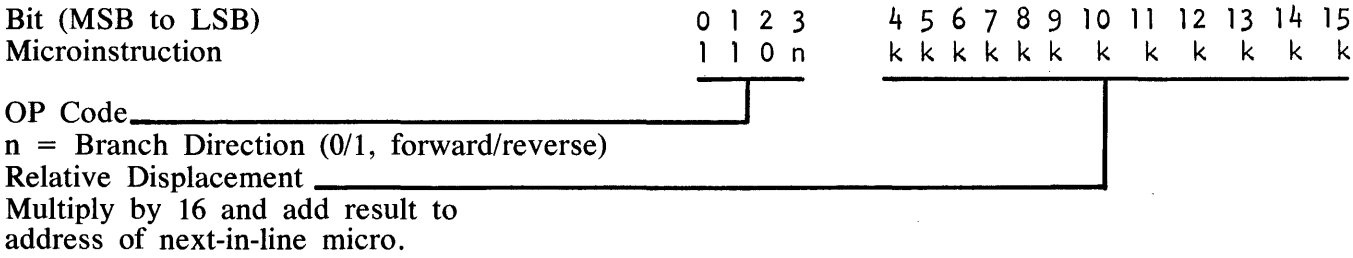
Micro = @B5A9@ = 1011 0101 1010 1001
Thus, destination register = 01 (Y)
rotate bit count = 11
extract bit count = 9

T at the start = @0B1800@ = 0000 1011 0001 1000 0000 0000
T after temporary rotation = 1100 0000 0000 0000 0101 1000

The rightmost nine bits are moved to Y, which becomes @000058@.

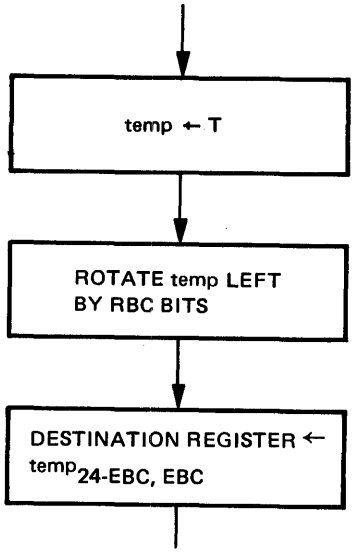
Note: It may be useful, in cases where wrap-around is not a factor, to consider this microinstruction as extracting the number of bits specified by the Extract Bit Count from the portion of T ending with the bit specified by the Rotate Bit Count minus 1.

12C, 13C BRANCH RELATIVE FORWARD, REVERSE

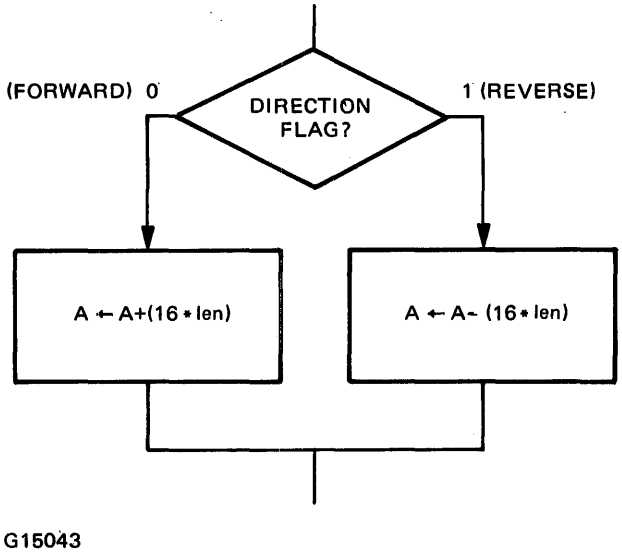


The next microinstruction is fetched from the address obtained by adding the signed Relative Displacement value multiplied by 16 to the address of the next-in-line microinstruction. Bit 3 of the OP code specifies positive or negative displacement (forward or backward jump). Note that the Relative Displacement value is in words (or "micros") for convenience, hence the automatic multiplication by 16 to convert to actual bit count

This is often considered to be two distinct microinstructions: 12C, Branch Relative Forward; 13C, Branch Relative Reverse.



11C Extract From T



12C, 13C Branch Relative Forward, Reverse

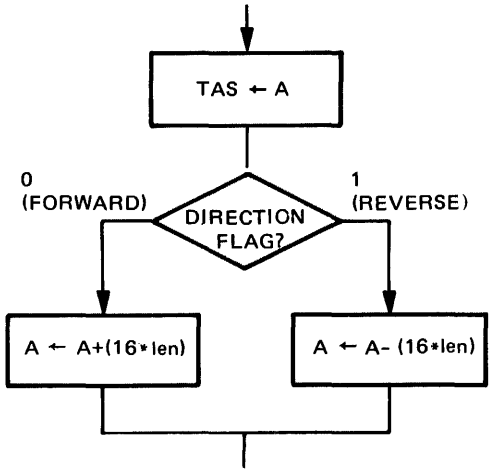
14C, 15C CALL RELATIVE FORWARD, REVERSE

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	1	1	1	n	k	k	k	k	k	k	k	k	k	k	k	k

OP Code
n = Displacement ± (0/1)
Call Address Displacement
Multiply (observe sign) by 16 and add result to address of next-in-line microinstruction.

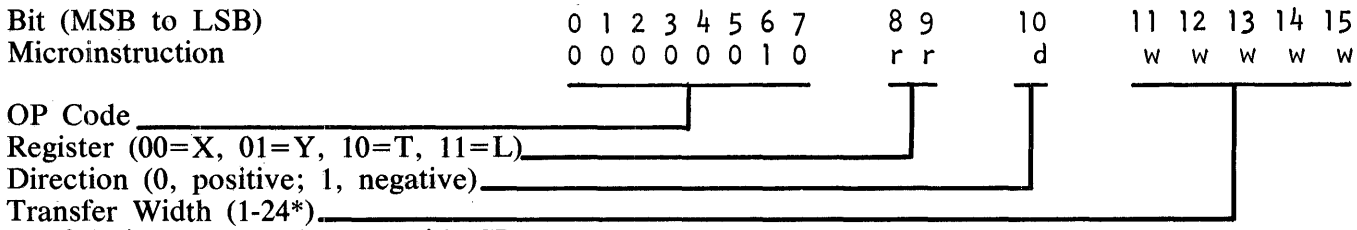
The address of the next-in-line microinstruction is ~~multiplied by 16 and~~ pushed on the A stack; then, address of the next micro that is to be fetched is obtained by adding the signed displacement value (Call Address Displacement) to the address of the next-in-line microinstruction. Bit 3 of the OP code specifies positive or negative displacement (forward or backward jump).

Note that this is the standard technique for call/return programming in microcode. A return is executed by a Register Move from TAS to A (microinstruction @1BA4@).



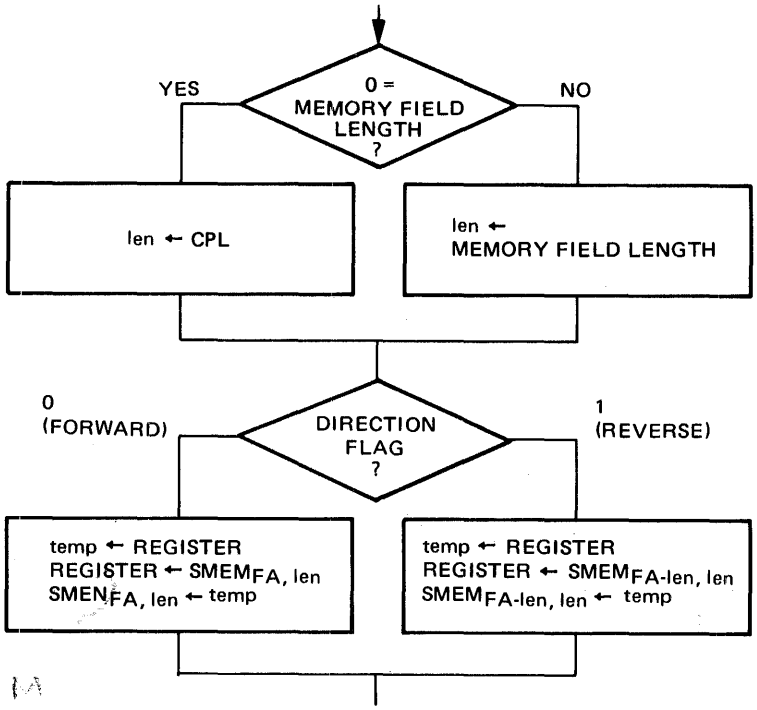
G15044

2D SWAP MEMORY



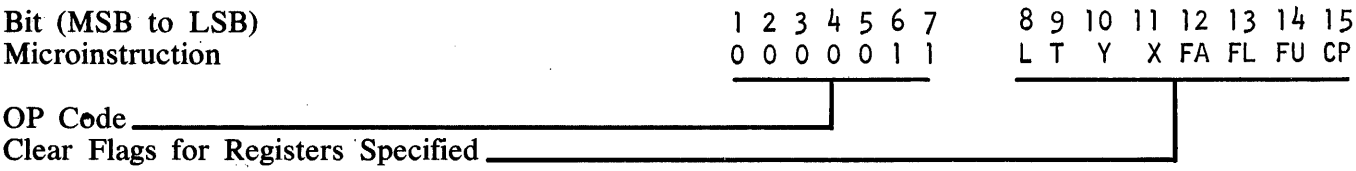
* If 0, ignore rr and swap with CPL.

Data from S memory is swapped with one of the general-purpose X, Y, T, L registers. If Transfer Width is less than 24, data from memory is right-justified in the register, with left zero-fill, and data from the register is left-truncated. A Transfer Width of zero causes the value of CPL to be used as the transfer width. Memory is addressed by FA, which contains the first bit address if the direction variant is 0 or the last bit address plus one if the Direction variant is 1.



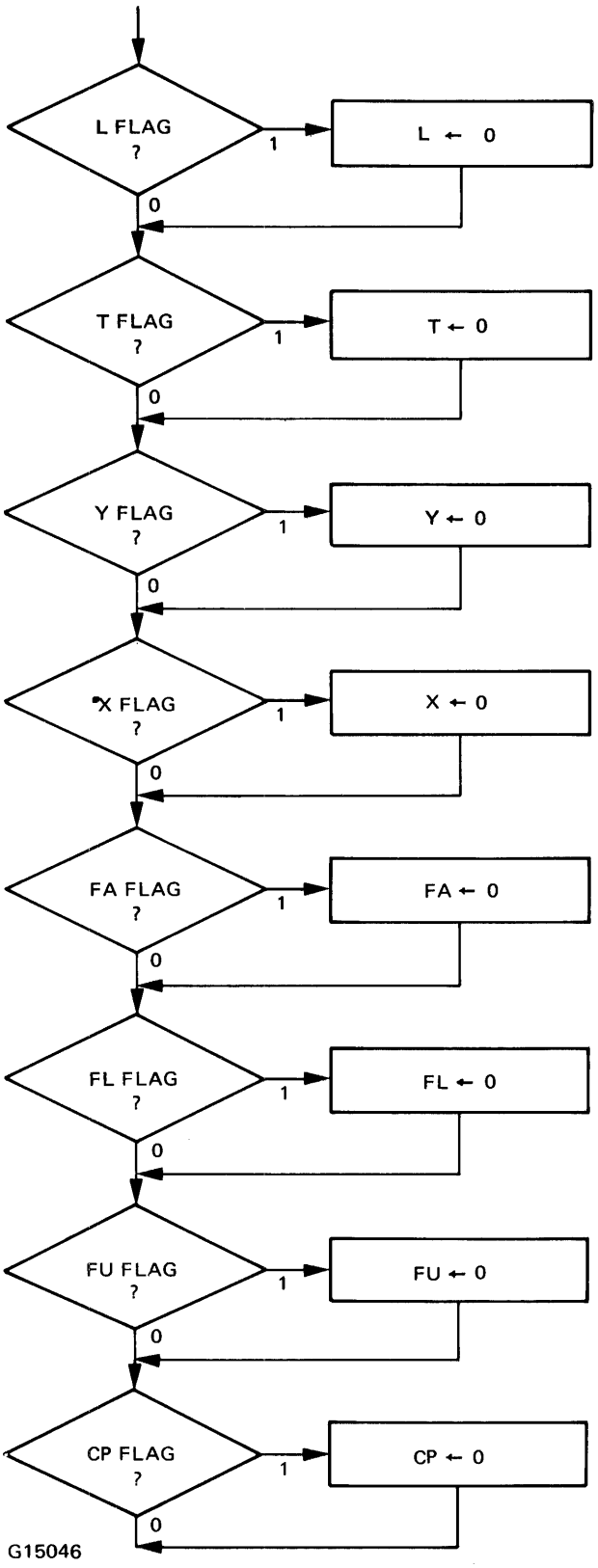
G15045

3D CLEAR REGISTERS



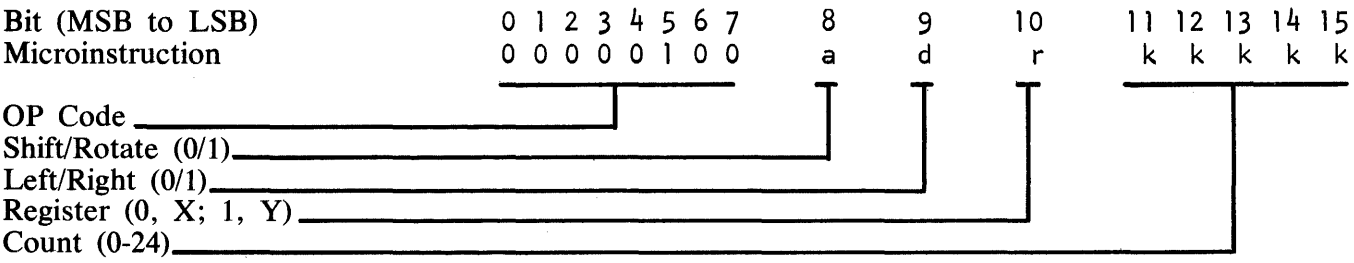
None, some, or all of the following registers are zeroed by setting to ones the appropriate Clear Flags in the microinstruction:

L, T, Y, X, FA, FU, CP

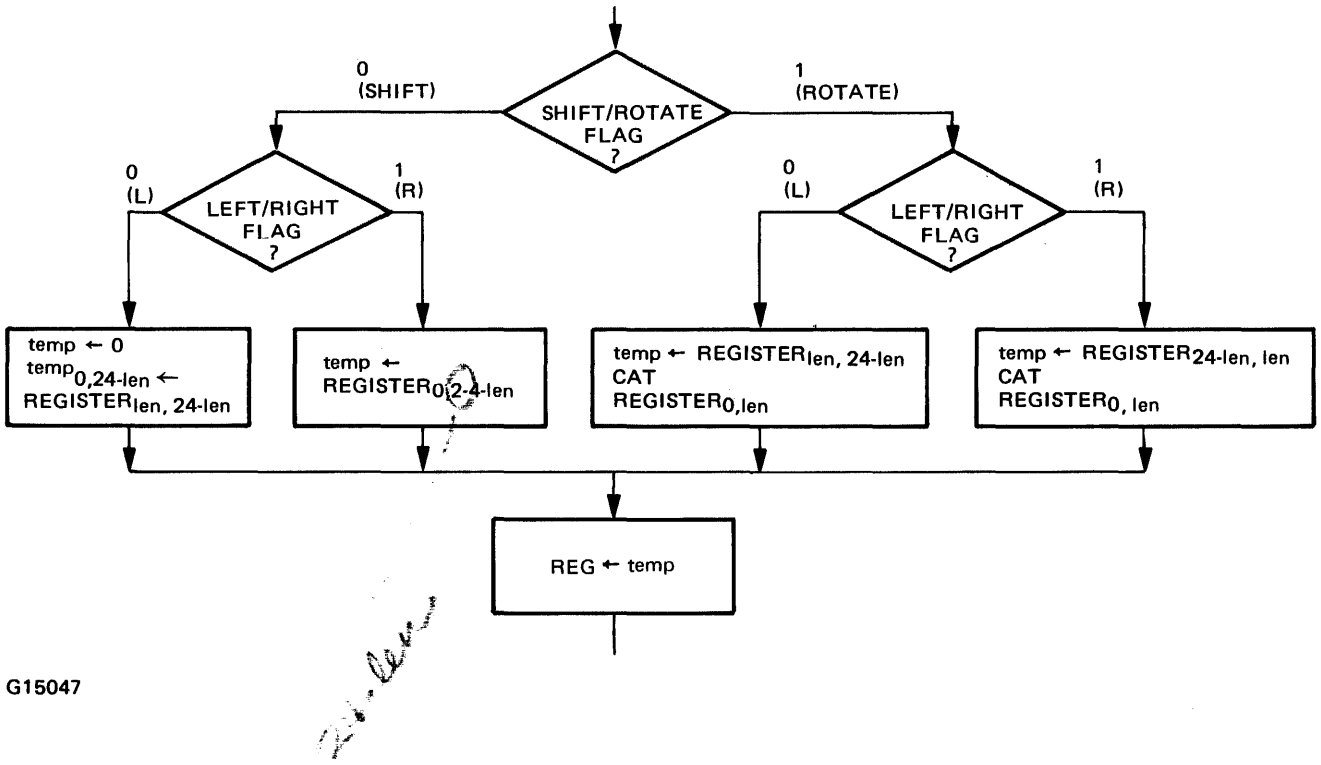


3D Clear Registers

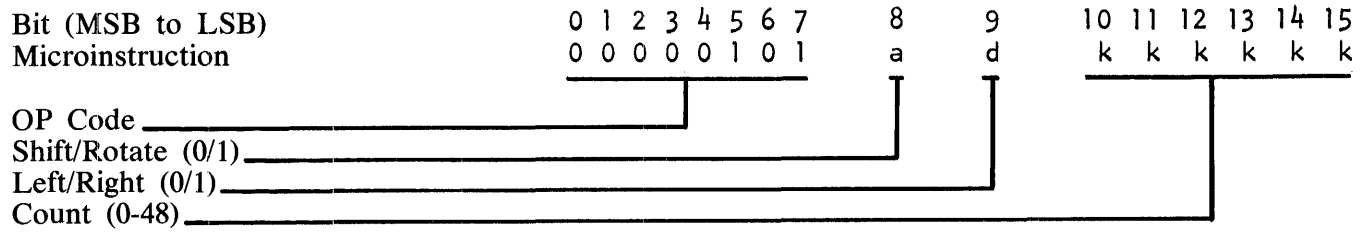
4D SHIFT/ROTATE X OR Y



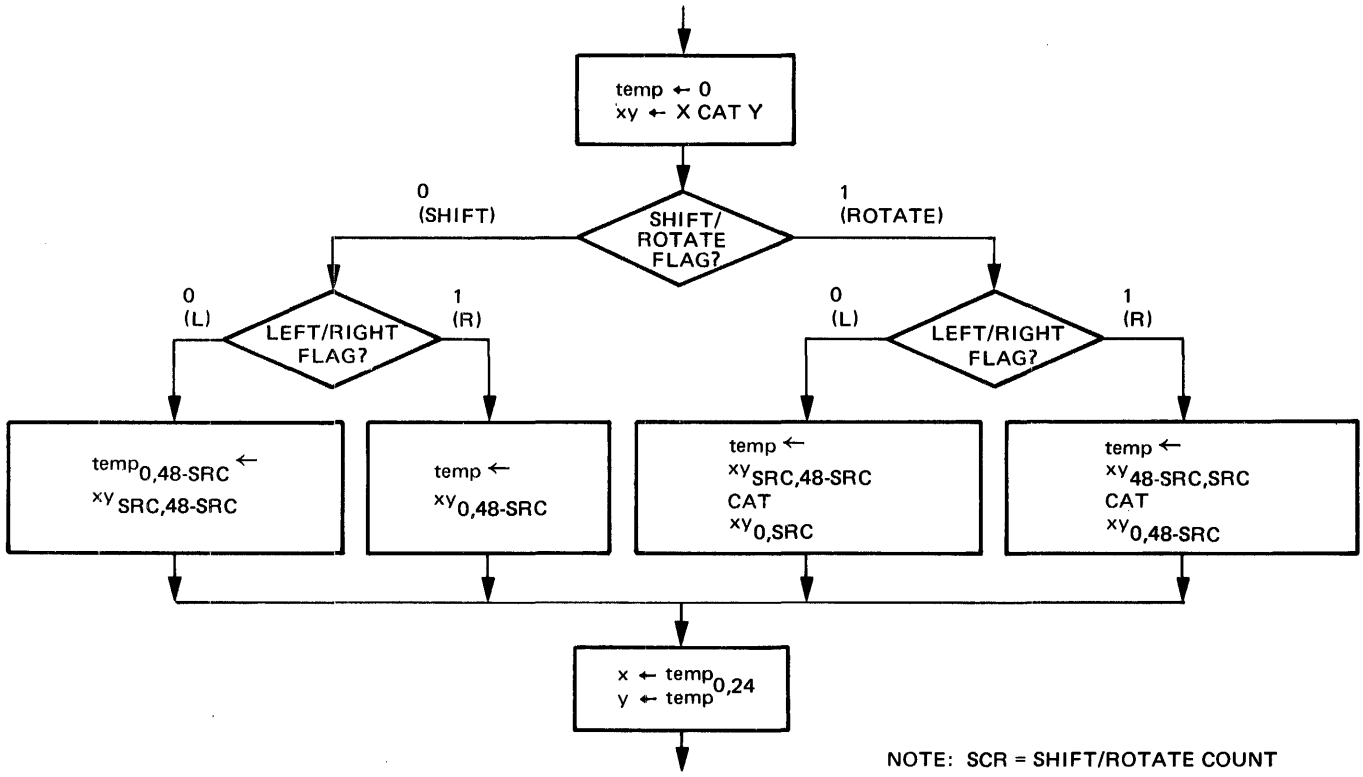
Either X or Y is shifted left or right bit the number of bits specified by the Count variant. For the shift operation, zero-fill takes place.



5D SHIFT/ROTATE X CONCATENATED WITH Y

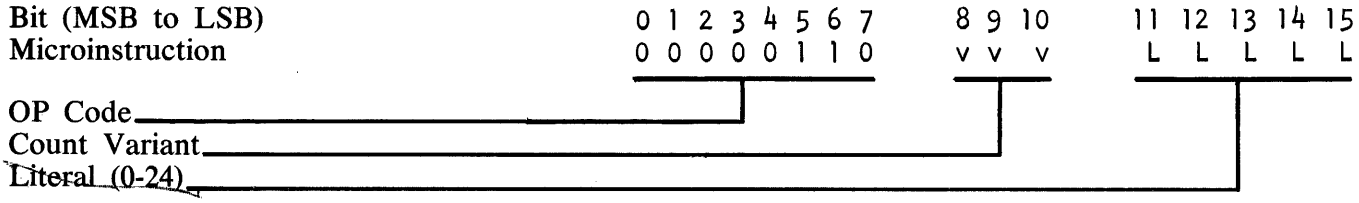


The 48-bit entity formed by X concatenated with Y is shifted/rotated left or right. Note that X is the leftmost (more significant) register. On a shift operation, zero-fill takes place on the side opposite the shift-out.

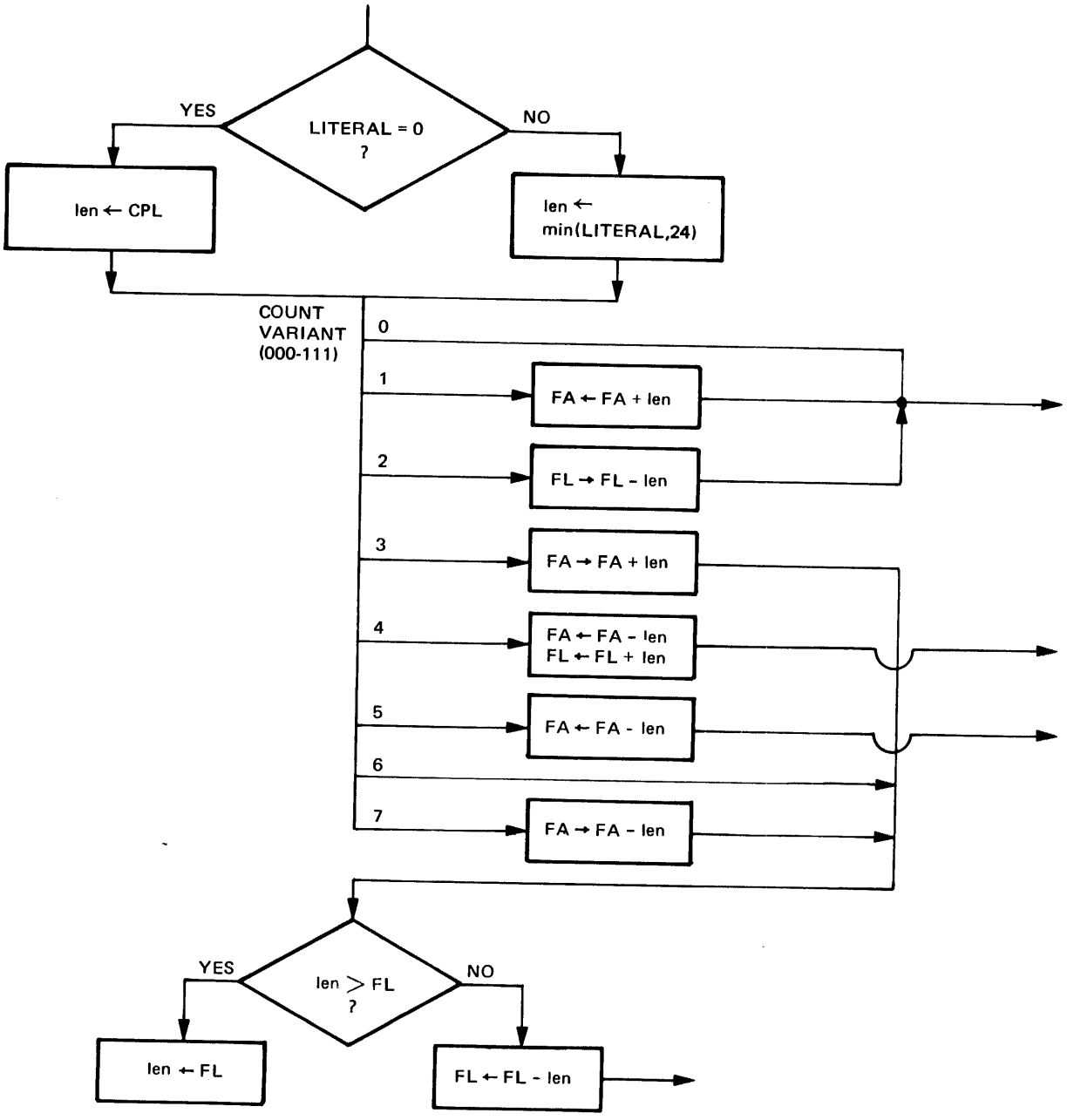


G15048

6D COUNT FA/FL

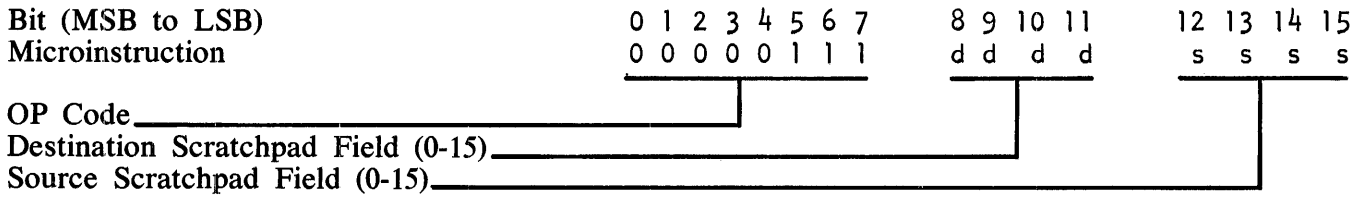


Register FA and/or FL may be counted up or down in various combinations by the value of the literal in the microinstruction. If this literal is zero, the value of CPL is used. Specific actions are listed in the flow chart. Note that FA and FL may not be counted up simultaneously; all other combinations are valid. Literal (or CPL) values greater than 24 are truncated to 24. FA may overflow or underflow, it merely wraps around. FL may overflow and wrap around to zero; underflow of FL is detected by the processor, however, and a value of zero is left in FL when this occurs.

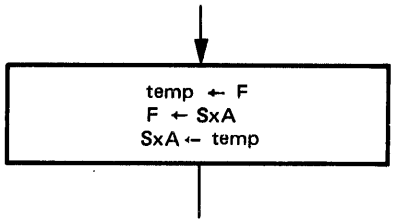


G15049

7D EXCHANGE F WITH DOUBLEPAD WORD

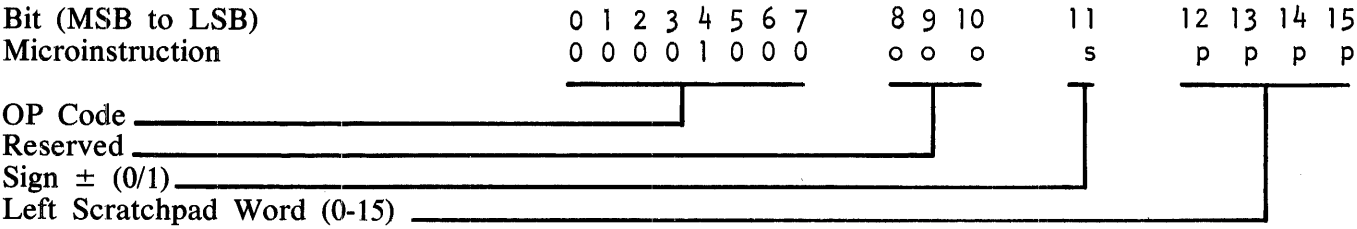


The contents of the 48-bit F register are moved to a temporary area. The 48-bit double scratchpad word specified by Source Scratchpad Field is moved to F, and the contents of the temporary area are moved to the double scratchpad word specified by Destination Scratchpad Field. Note that source and destination may be (and generally are) identical; the result is a swap of the contents of the double scratchpad word with the contents of F.

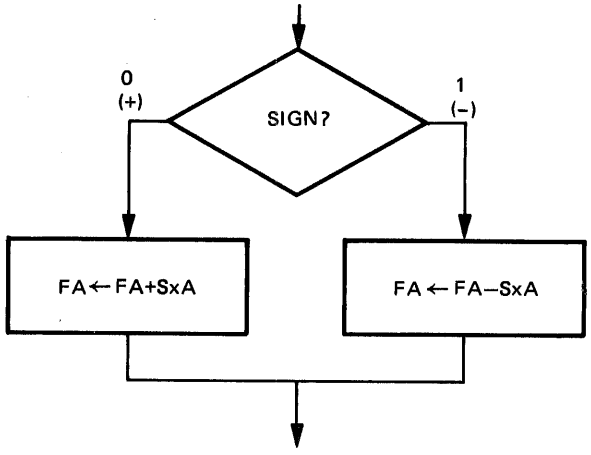


G15050

8D SCRATCHPAD RELATE FA

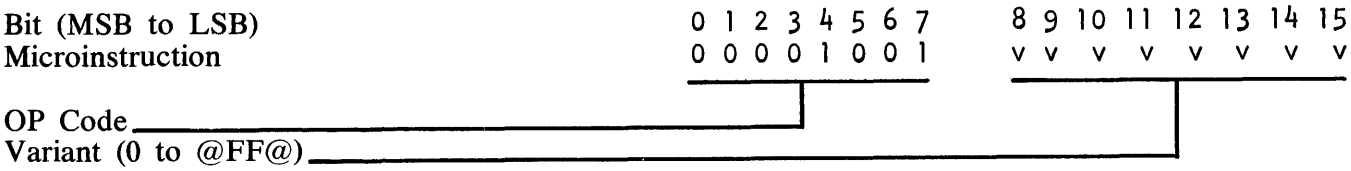


The value of FA is added to the signed Left Scratchpad Word. The binary sum is stored in FA. Overflow and underflow of FA are neither restricted nor detected.

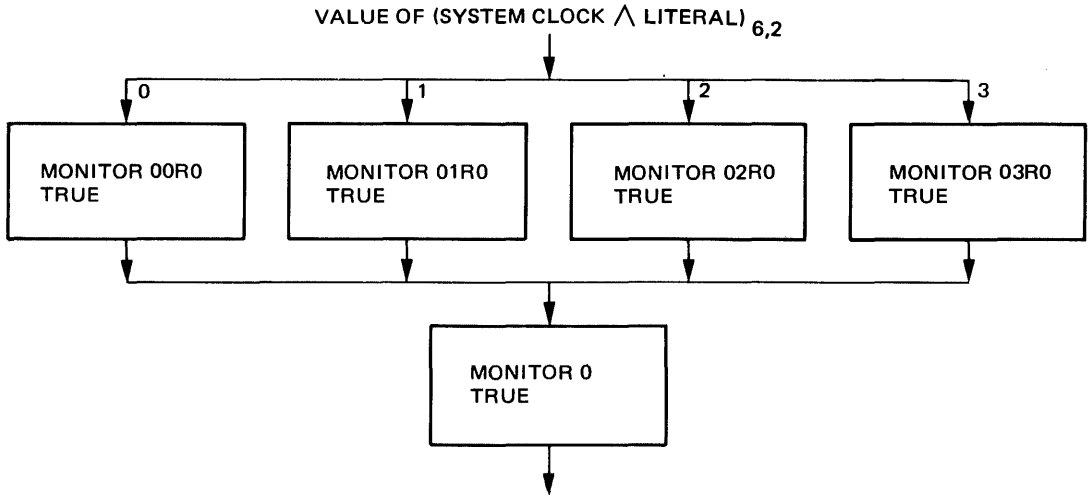


G15051

9D MONITOR



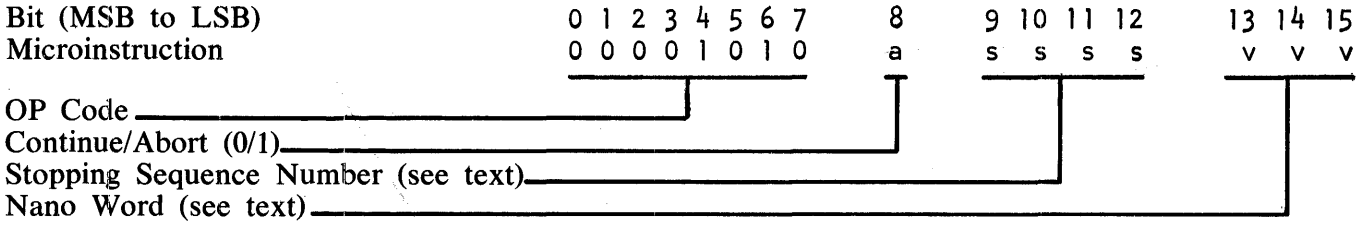
During the time this microinstruction is executing, the "MONITOR 0" backplane pin is true and the 8 bits specified in the variant are available at the backplane. Bits 14 and 15 of the microinstruction are ANDed with the system clock and the last two bits (bb = 00, 01, 10, 11) of the resulting quantity turn on one only of the backplane pins MONITOR 00R0, MONITOR 01R0, MONITOR 02R0, or MONITOR 03R0. This enables hardware monitors to measure system performance based on the inclusion of the microinstruction at various points within the software.



NOTE: MONITOR 0 AND MONITOR 0nR0 ARE BACKPLANE PINS

G15052

10D NANO MOVE



This microinstruction is a diagnostic tool. It enables "snapshots" of portions of the N (Nano) register to be taken by diagnostic routines (or by entries through the console). N is a 114-bit register from which masks can be formed to represent control signals which direct the processor in performing specific microinstructions during the execute phase. A given microinstruction, when decoded, will thus cause one or more of the bits in N to be set. N may be considered as being segmented into five nano words, termed W.0 through W.4. W.0 has 18 bits, the other four nano words have 24 bits each.

Let the stopping sequence count (ssss in the microinstruction) be the ssssth nano (origin = 0) executed for some microinstruction. For example, if a particular microinstruction results in bits 13, 41, and 102 of N being set, ssss = 1 corresponds, for this micro, to the execution of nano 41. If the micro results in only bit 18 of N being set, ssss = 1 is inapplicable; ssss = 0 corresponds to bit 18 and there are no more bits.

Nano Move has no externally apparent effect on the processor until the execution of some subsequent microinstruction. Execution of the next microinstruction with an ssssth nano is suspended when that nano is reached. The nano word specified by nnn is shifted into the BR register. If the abort flag is zero, execution of the suspended microinstruction resumes; if this flag is one, the micro is aborted, i.e., N is cleared and the next microinstruction is fetched. If nnn = 000, W.0, which has 18 bits, appears in the rightmost 18 bits of BR.

This is an unusual micro, with no utility in standard software. It is provided to enable the isolation of malfunctions in the decode logic, down to a specific control path.

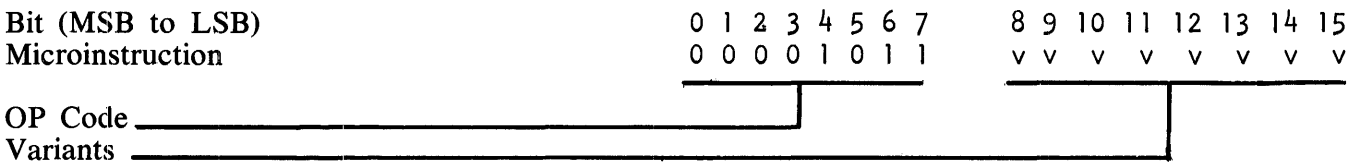
Nano Move Options: The abort flag is restricted for certain microinstructions, as shown in table 5-1. Entries in column LS (last sequence) are equal to the number of nanos minus 1; in order to "snap" a particular microinstruction following a Nano Move, the value of ssss in that Nano Move must not exceed the LS value. If it does, some subsequent microinstruction will be snapped.

Table 5-1. Nano Move Options

Micro	Name	Variant	Nanos	LS=	Group
1C	REGISTER MOVE	Except @1BA4@	1	0	A
@1BA4@	EXIT		1	0	B
2C	SCRATCHPAD MOVE		1	0	A
3C	4-BIT MANIPULATE		1	0	A
4C,5C	CONDITIONAL BRANCH		1	0	B
6C	SKIP WHEN		1	0	A
7C	READ/WRITE MEMORY READ		4	5	C
WRITE			5	4	C
8C	MOVE 8-BIT LITERAL		1	0	A
9C	MOVE 24-BIT LITERAL		1	0	A
10C	SHIFT/ROTATE T		1	0	A
11C	EXTRACT FROM T		1	0	A
12,13C	BRANCH RELATIVE		1	0	B
14,15C	CALL RELATIVE		1	0	B
2D	SWAP MEMORY		4	5	C
3D	CLEAR REGISTERS		B	7	D
4C	SHIFT/ROTATE X OR Y		1	0	A
5D	SHIFT/ROTATE X AND Y		1	0	A
6D	COUNT FA/FL	0, 1, 2, 5, 6	1	0	A
		3, 4, 7	2	1	D
7D	EXCHANGE F WITH DPW		1	0	A
8D	SCRATCHPAD RELATE FA		1	0	A
9D	MONITOR		1	0	A
10D	NANO MOVE		1	0	
11D	READ/WRITE MEMORY	READ	3	2	C
		WRITE	4	3	C
1E	DISPATCH		3	2	C
			5	4	C
2E	CASSETTE CONTROL		1	0	A
3E	BIAS		1	0	A
4E	STORE F INTO DPW		1	0	A
5E	LOAD F FROM DPW		1	0	A
6E	SET CARRY FLIP-FLOP		1	0	A
7E	READ/WRITE CACHE		12	11	E
1F	HALT		1	0	B
3F	NORMALIZE		3	2	D
4F	TRANSFER CONTROL		1	0	A
5F	CLEAR CACHE		6	5	E
6F	INCREMENT		1	0	A

NOTES (pertain to group column)
A All cases valid (single sequence).
B Abort invalid (partial execution during decode).
C Continue invalid (S Memory affected).
D All cases valid (multi-sequence).
E Abort invalid (Cache micros change A).

11D DIAGNOSTIC READ/WRITE MEMORY



xx000000 Read 22-bit Word (16 data + 6 Error Correction Code) to Y.

rr000100 Write 22-bit Word from X, Y, T, or L.

rr001001 Echo Write Data from X, Y, T, or L to Y.

xx001010 Echo Modified Address forward from FA to Y.

xx001011 Read and Clear Error Log to Y.

xx011000 Read Port Data Latch to Y.

rr111000 Echo Through Port Interchange from X, Y, T, or L to Y.

rr111001 Echo Through Port Adapter 1 from X, Y, T, or L to Y.

rr111010 Echo through Port Adapter 2 from X, Y, T, or L to Y.

rr111011 Echo through Port Adapter 3 from X, y, t, or L to Y.

All other Undefined.

xx: These bits are ignored.

rr: Source register; 00 = X, 01 = Y, 10 = T, 11 = L

Diagnostic Read reads all 22 bits (16 data bits and 6 Error Correction Code bits) of a memory storage word into the Y register in a format detailed in the sketch below. An odd-parity bit is generated by the hardware and returnes as bit 7. Single-bit errors are not corrected but all errors are reported. If a single-bit error is detected within the 16 data bits, the odd parity bit is complemented to cause even parity.

Diagnostic Write writes 22 bits (16 data, 6 ECC) from a specified register into memory. The source register must be in the format shown in the sketch; the P bit (bit 7) is ignored. Errors are not corrected or reported.

ECC bits	0	P	Data
0 → 5	6	7	18 → 23

Y REGISTER (11D Read/Write Information Format)

P is a parity bit, generated by hardware, on the Read variant only.

All Diagnostic Read/Write accesses must be in the forward direction on stack boundaries.

Echo Write Data sends 24 bits from the specified source register to the processor's memory base unit, which returns it to the Y register. The memory base unit (MBU) is that portion of the processor in control of addressing, rotation, masking, and merging functions needed for Read or Write memory accesses.

Echo Modified Address sends to the MBU a·24-bit address which is returned to the Y register either decremented or incremented by 16, depending on the variant.

Read and Clear Error Log reads the MBU Error Log register (see Section 4) to the Y register and clears the Error Log. Error Log format is shown below.

ER	UP	UN	CSB	OP	reserved	SB	R	S
0	1	2	3	4	5 → 11	12 → 15	16	18 → 23

ERROR LOG FORMAT

A ER = Error Repeat; flags multiple errors of the same type.
B UP = Uncorrectable processor error flag.
C UNP = Uncorrectable non-processor error flag.
D CSB = Corrected single bit error flag.
E OP = Operation: 0=Read, 1=Write.
F SB = Storage Board of failed chip.
G R = Row of failed chip.
S Syndrome. See tables 5-2 and 5-3.

A priority scheme causes information about the error location and the syndrome for an Uncorrectable Processor error to replace that for and Uncorrectable Non-Processor error; the latter, in turn, overrides that for a Correctable Single-Bit error. Furthermore, error information for a memory Read operation replaces that for a Write of equal or lower priority.

Table 5-2. S Memory Syndrome Interpretation

Interpretation		Single-Bit Error Syndrome						
			Syndrome					
Syndrome	Meaning	Bit	6	5	4	3	2	1
0 0 0 0 0 0	No Error	0	0	0	1	0	1	1
		1	0	1	0	0	1	1
Single 1-Bit	Check Bit Error	2	1	0	0	0	1	1
		3	0	0	1	1	0	1
		4	1	0	0	1	0	1
1 0 1 0 1 0 0 1 0 1 0 1 1 1 1 0 0 0 0 0 0 1 1 1	Multiple Error	5	0	1	1	0	0	1
		6	1	0	1	0	0	1
		7	1	1	0	0	0	1
		8	0	0	1	1	1	0
		9	0	1	0	1	1	0
Even 1-Bits	Multiple Error	10	1	0	0	1	1	0
		11	0	1	1	0	1	0
		12	1	1	0	0	1	0
5 1-Bits	Multiple Error	13	0	1	1	1	0	0
		14	1	0	1	1	0	0
		15	1	1	0	1	0	0
1 1 1 1 1 1	Multiple Error or Missing Board	16	0	0	0	0	0	1
		17	0	0	0	0	1	0
		18	0	0	0	1	0	0
		19	0	0	1	0	0	0
All Others	Single-Bit Error	20	0	1	0	0	0	0
		21	1	0	0	0	0	0

Read Port Data Latch reads to the Y register the current contents of this hardware latch. These contents are equal to the most recent of (a) a memory address from the last port device Write cycle, or (b) Read data from the last port device Read cycle, or (c) echo data from the last echo cycle.

Echo Through Port Interchange or Port Adapter sends 24 bits of data from the designated source register to be captured in the port interchange data latch. The data is returned to the Y register by one of four paths; the port interchange itself or one of the associated adapters.

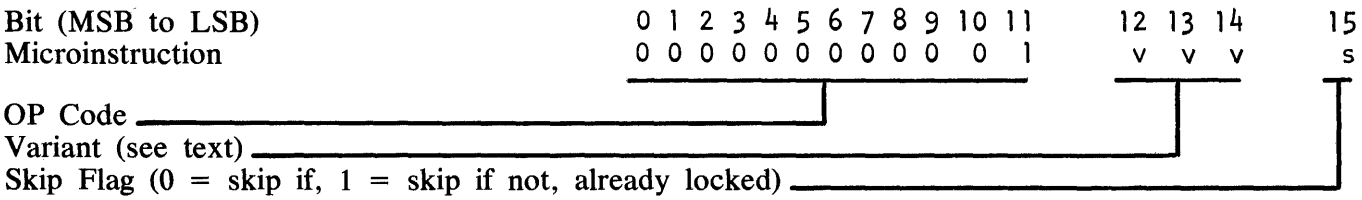
Table 5-3. Syndrome Summary

	Syndrome Pattern	Interpretation	Action
0	0 0 0 0 0 0	NO ERROR	NO ACTION
1	0 0 0 0 0 1	CHECK BITS, BIT 6 ERROR	REPORT SINGLE ERROR
2	0 0 0 0 1 0	CHECK BITS, BIT 5 ERROR	REPORT SINGLE ERROR
3	0 0 0 0 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
4	0 0 0 1 0 0	CHECK BITS, BIT 4 ERROR	REPORT SINGLE ERROR
5	0 0 0 1 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
6	0 0 0 1 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
7	0 0 0 1 1 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
8	0 0 1 0 0 0	CHECK BITS, BIT 3 ERROR	REPORT SINGLE ERROR
9	0 0 1 0 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
10	0 0 1 0 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
11	0 0 1 0 1 1	DATA BITS, BIT 15 ERROR	CORRECT BIT 15, REPORT SINGLE ERROR
12	0 0 1 1 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
13	0 0 1 1 0 1	DATA BITS, BIT 14 ERROR	CORRECT BIT 14, REPORT SINGLE ERROR
14	0 0 1 1 1 0	DATA BITS, BIT 13 ERROR	CORRECT BIT 13, REPORT SINGLE ERROR
15	0 0 1 1 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
16	0 1 0 0 0 0	CHECK BITS, BIT 2 ERROR	REPORT SINGLE ERROR
17	0 1 0 0 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
18	0 1 0 0 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
19	0 1 0 0 1 1	DATA BITS, BIT 12 ERROR	CORRECT BIT 12, REPORT SINGLE ERROR
20	0 1 0 1 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
21	0 1 0 1 0 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
22	0 1 0 1 1 0	DATA BITS, BIT 11 ERROR	CORRECT BIT 11, REPORT SINGLE ERROR
23	0 1 0 1 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
24	0 1 1 0 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
25	0 1 1 0 0 1	DATA BITS, BIT 10 ERROR	CORRECT BIT 10, REPORT SINGLE ERROR
26	0 1 1 0 1 0	DATA BITS, BIT 9 ERROR	CORRECT BIT 9, REPORT SINGLE ERROR
27	0 1 1 0 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
28	0 1 1 1 0 0	DATA BITS, BIT 8 ERROR	CORRECT BIT 8, REPORT SINGLE ERROR
29	0 1 1 1 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
30	0 1 1 1 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
31	0 1 1 1 1 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ODD ERROR
32	1 0 0 0 0 0	CHECK BITS, BIT 1 ERROR	REPORT SINGLE ERROR
33	1 0 0 0 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
34	1 0 0 0 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
35	1 0 0 0 1 1	DATA BITS, BIT 7 ERROR	CORRECT BIT 7, REPORT SINGLE ERROR
36	1 0 0 1 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
37	1 0 0 1 0 1	DATA BITS, BIT 6 ERROR	CORRECT BIT 6, REPORT SINGLE ERROR
38	1 0 0 1 1 0	DATA BITS, BIT 5 ERROR	CORRECT BIT 5, REPORT SINGLE ERROR
39	1 0 0 1 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR

Table 5-3. Syndrome Summary (Cont)

	Syndrome Pattern	Interpretation	Action
40	1 0 1 0 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
41	1 0 1 0 0 1	DATA BITS, BIT 4 ERROR	CORRECT BIT 4, REPORT SINGLE ERROR
42	1 0 1 0 1 0	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
43	1 0 1 0 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
44	1 0 1 1 0 0	DATA BITS, BIT 3 ERROR	CORRECT BIT 3, REPORT SINGLE ERROR
45	1 0 1 1 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
46	1 0 1 1 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
47	1 0 1 1 1 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
48	1 1 0 0 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
49	1 1 0 0 0 1	DATA BITS, BIT 2 ERROR	CORRECT BIT 2, REPORT SINGLE ERROR
50	1 1 0 0 1 0	DATA BITS, BIT 1 ERROR	CORRECT BIT 1, REPORT SINGLE ERROR
51	1 1 0 0 1 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
52	1 1 0 1 0 0	DATA BITS, BIT 0 ERROR	CORRECT BIT 0, REPORT SINGLE ERROR
53	1 1 0 1 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
54	1 1 0 1 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
55	1 1 0 1 1 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
56	1 1 1 0 0 0	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
57	1 1 1 0 0 1	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
58	1 1 1 0 1 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
59	1 1 1 0 1 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
60	1 1 1 1 0 0	EVEN NUMBER ERROR	REPORT MULTIPLE ERROR
61	1 1 1 1 0 1	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
62	1 1 1 1 1 0	MULTIPLE ODD ERROR	REPORT MULTIPLE ERROR
63	1 1 1 1 1 1	EVEN NUMBER OF ERRORS OR MEMORY ABSENT	REPORT MULTIPLE ERROR

1E DISPATCH



vvv =
000 Lockout
001 Write Low
010 Read
100 Write High
101 Port Absent
110 Undefined
111 Undefined

The Dispatch microinstruction allows the processor to send and receive interrupt information from ports other than port 7 (the "soft I/O" port). As all ports share a common interrupt system, the processor needs to get control of the interrupt system with a successful Dispatch Lockout before executing a Dispatch Write.

The Lockout variant sets the Lockout bit (bit 3 of the INCN register and allows skipping or not skipping depending on whether or not the Lockout bit is set. This action is specified by the setting of the Skip flag.

The Write High and Write Low variants set the Lockout and Interrupt bits of the INCN pseudoregister. These bits represent flip-flops in the port interchange. The contents of the L register are written into absolute memory locations 0 through 23, and the least-significant 7 bit of the T register, representing the destination port and channel, are written into an identification register in the port interchange. Write High causes a High Interrupt flip-flop in the specified port interchange to be set; Write Low resets this condition.

The Read variant stores the contents of absolute memory locations 0 through 23 into the L register and the contents of a port/channel identification register in the port interchange into bits 17 through 23 of the T register. (Bits 0 through 16 of T are left unchanged.)

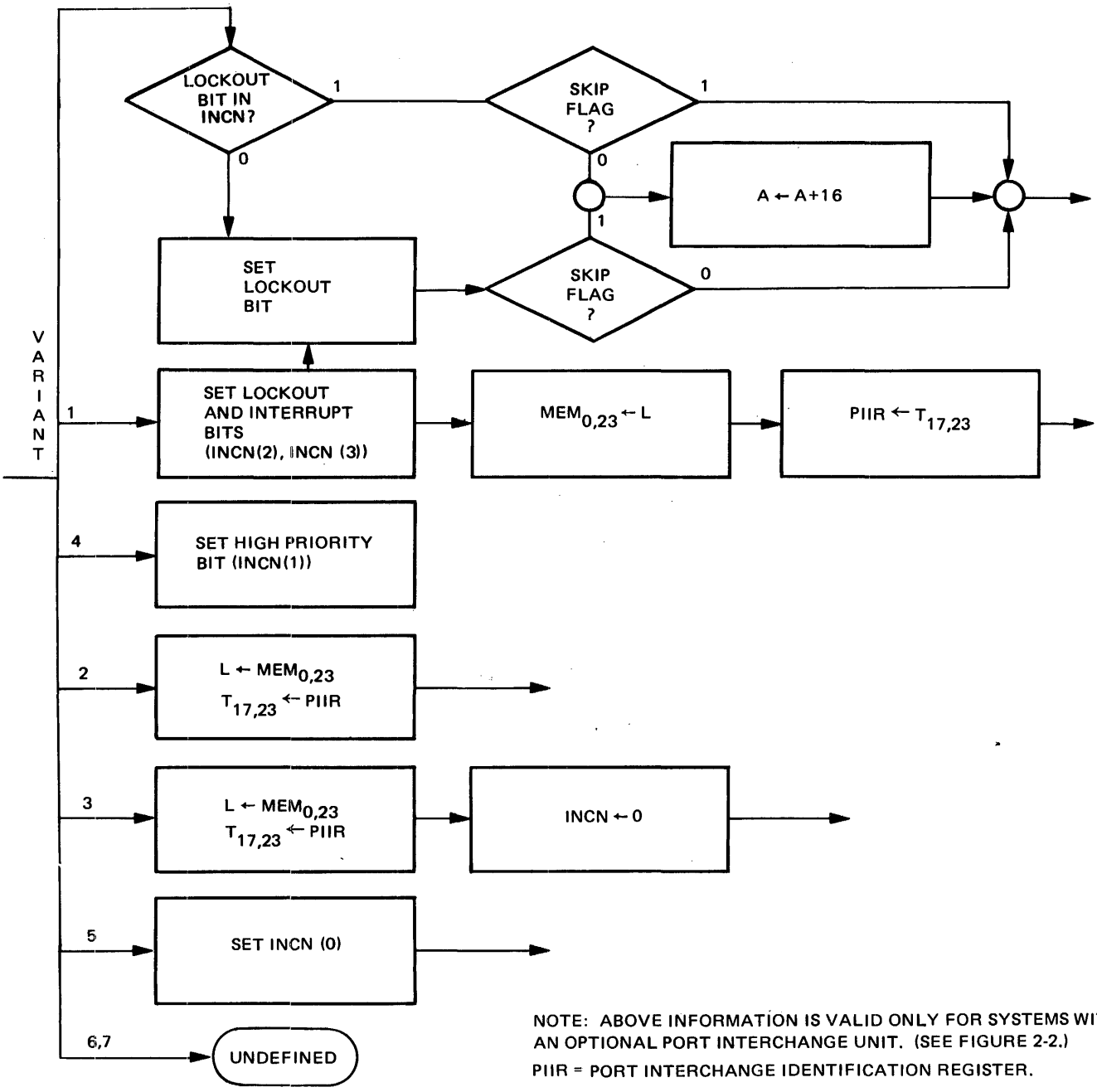
With the Read and Clear variant, all functions of a Read are performed. Additionally, the four flip-flops comprising the INCN pseudoregister are cleared.

A Dispatch microinstruction with the Port Absent variant set allows the processor to return a Port Device Absent signal to another port.

A B 1800 with no non-soft I/O ports installed is wired such that Dispatch options are limited:

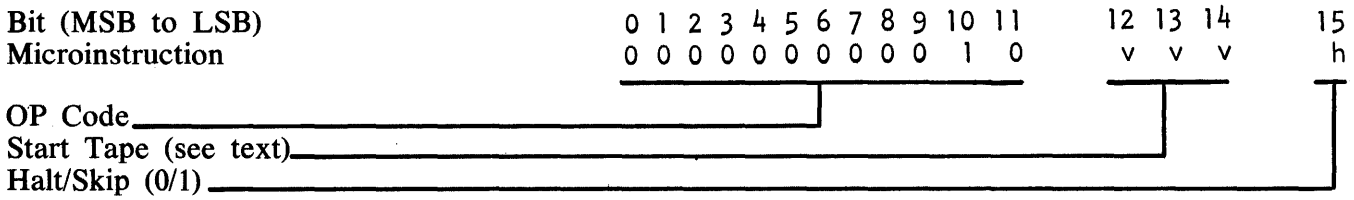
1. Lockout always skips.
2. Write Low always sets Port Device Absent to indicate absence.
3. Read and Clear resets Port Device Absent to indicate presence.
4. No changes occur in the L and T registers. In INCN, the Port Device Absent bit can change; the Lockout, Interrupt, and High Priority bits are strapped false.

No other Dispatch operations are defined.


LOCKOUT BIT IN INCN?
1
0
SKIP FLAG ?
1
0
A ← A+16
1
SET LOCKOUT BIT
SKIP FLAG ?
0
VARIANT
1
SET LOCKOUT AND INTERRUPT BITS (INCN(2), INCN (3))
MEM0,23 ← L
PIIR ← T17,23
4
SET HIGH PRIORITY BIT (INCN(1))
2
L ← MEM0,23
T17,23 ← PIIR
3
L ← MEM0,23
T17,23 ← PIIR
INCN ← 0
5
SET INCN (0)
6,7
UNDEFINED
NOTE: ABOVE INFORMATION IS VALID ONLY FOR SYSTEMS WITH AN OPTIONAL PORT INTERCHANGE UNIT. (SEE FIGURE 2-2.)
PIIR = PORT INTERCHANGE IDENTIFICATION REGISTER.
G15055

1E Dispatch

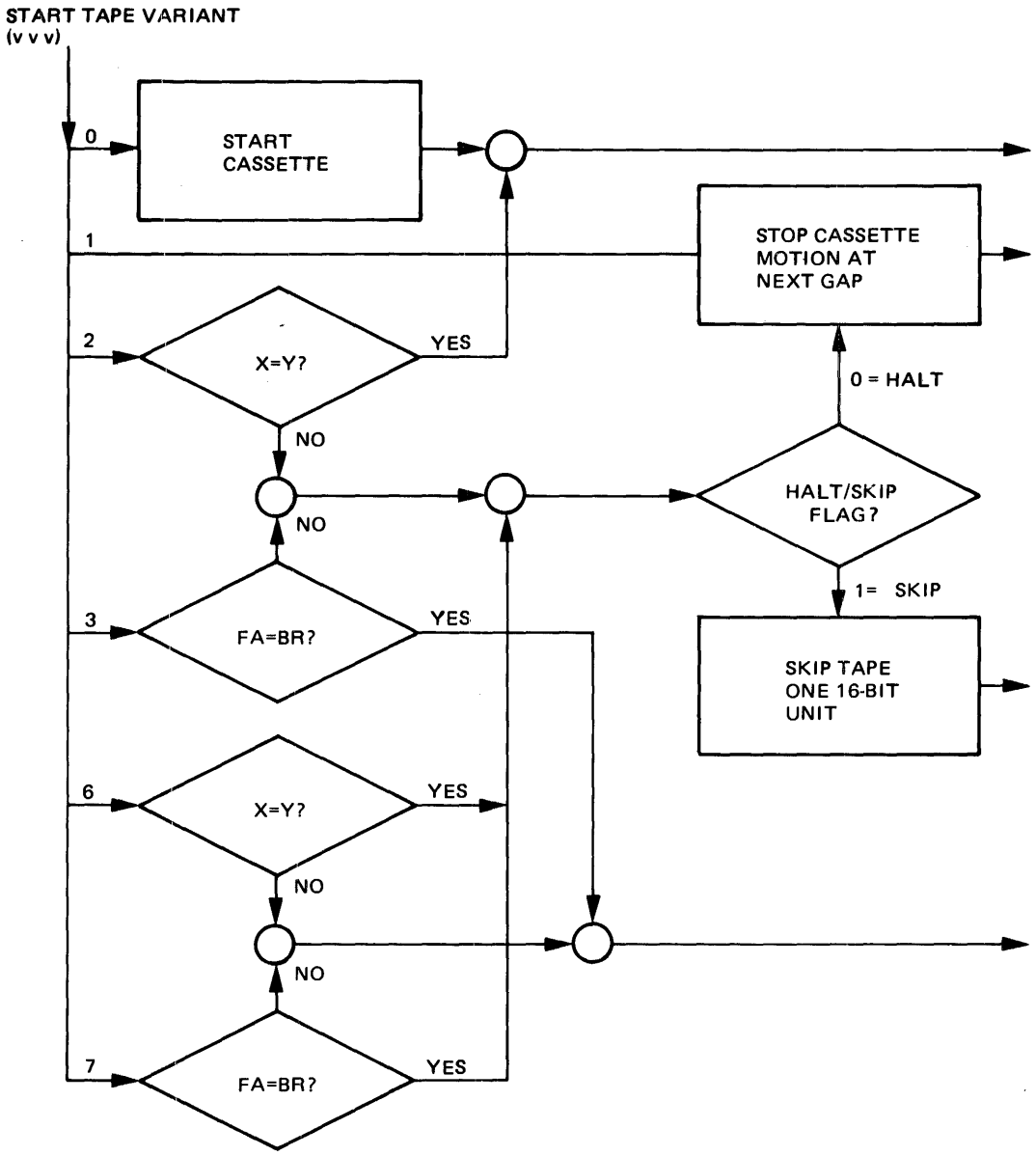
2E CASSETTE CONTROL



When a remote cassette tape station is assigned to the processor (SYSTEM setting on the CASSETTE SELECT switch), the associated cassette tape drive comes under the control of this microinstruction. The Start Tape variant causes tape to be moved and 16-bit units of data to be continuously fed to the U register. The firmware has responsibility for retrieving these data units in time.

For other valid variant values, the Halt/Skip flag specifies that tape movement is to stop (h/s = 0) or that a unit of data is to be skipped (h/s = 1), either unconditionally or on the basis of comparison of various registers.

In TAPE mode, microinstructions are fetched and executed from cassette tape; a cassette stop causes a processor Halt.

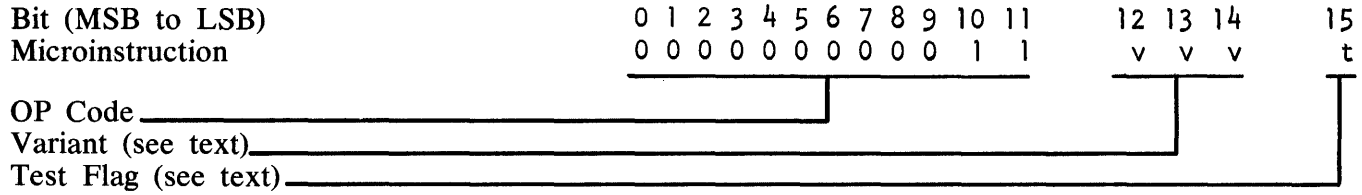


NOTE: VARIANTS 4 AND 5 ARE RESERVED

G15056

2E Cassette Control

3E BIAS



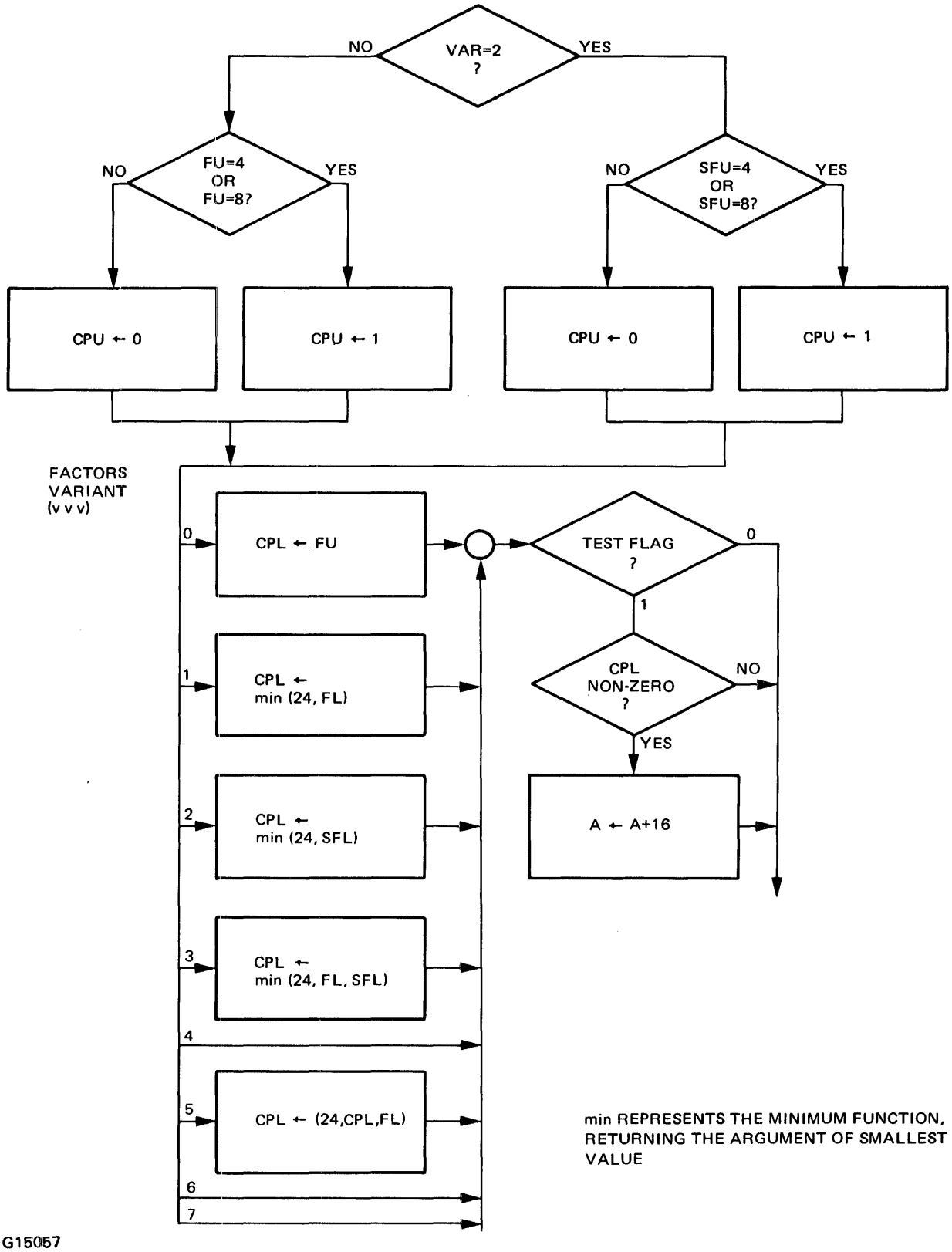
The Bias microinstruction sets CPU and CPL. Its greatest use is found allowing data to be efficiently manipulated in loops. It handles even odd-length, last-time-through cases smoothly.

First, Bias sets CPU to 1, if FU is either 4 or 8, or to zero otherwise. Recall that FU is generally set by an interpreter to indicate its basic arithmetic "chunk" size, with FU = 4 implying a BCD language such as COBOL and FU = 0 implying a binary-field-oriented language such as FORTRAN. CPU is the means by which the processor is instructed to do arithmetic operations in either a 4-bit BCD manner or in a binary manner. Thus, the first function of Bias is to correlate the firmware-settable FU register with CPU, which it alone can address as a destination. A variant of 2 (vvv = 010) causes the value of SFU to be used instead of FU, with identical effect.

The second, more dynamic, feature of Bias is to set CPL, which is the specifier of operand lengths to the arithmetic unit and of default field lengths for the Read/Write Memory microinstruction. The flow chart shows that CPL is set to the smallest of n different quantities for each vvv value:

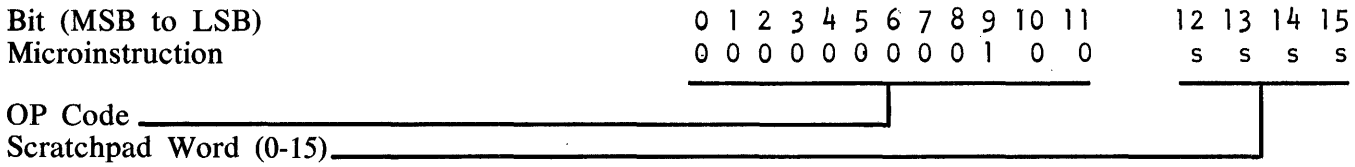
vvv	Factors
0	FU
1	24 and FL
2	24 and SFL
3	24 and FL and SFL
4	CPL
5	24 and CPL and FL
6	CPL
7	CPL

If Test Flag is set (1), the next 16-bit microinstruction is skipped if CPL is not zero after Bias is executed.


VAR=2 ?
NO
YES
FU=4 OR FU=8?
NO
YES
SFU=4 OR SFU=8?
NO
YES
CPU ← 0
CPU ← 1
CPU ← 0
CPU ← 1
FACTORS VARIANT (v v v)
0
CPL ← FU
TEST FLAG ?
0
1
1
CPL ← min (24, FL)
CPL NON-ZERO ?
NO
YES
2
CPL ← min (24, SFL)
A ← A+16
3
CPL ← min (24, FL, SFL)
4
5
CPL ← (24,CPL,FL)
6
7
min REPRESENTS THE MINIMUM FUNCTION, RETURNING THE ARGUMENT OF SMALLEST VALUE
G15057

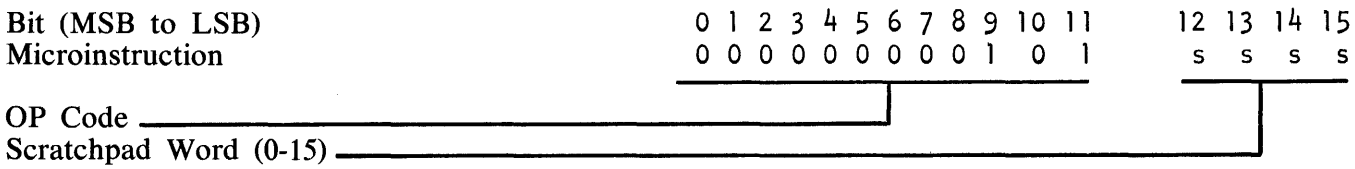
3E Bias

4E STORE F INTO DOUBLEPAD WORD



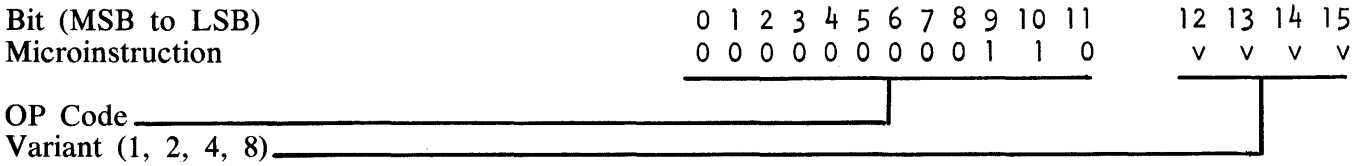
The contents of F are moved into the specified double scratchpad word. F remains unaltered.

5E LOAD F FROM DOUBLEPAD WORD

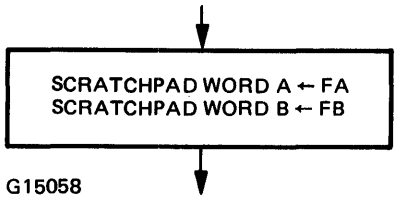


The contents of the specified doublepad word are moved into F. The scratchpad remains unaltered.

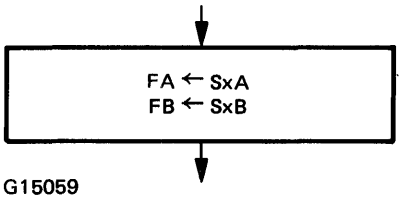
6E SET CARRY FLIP-FLOP



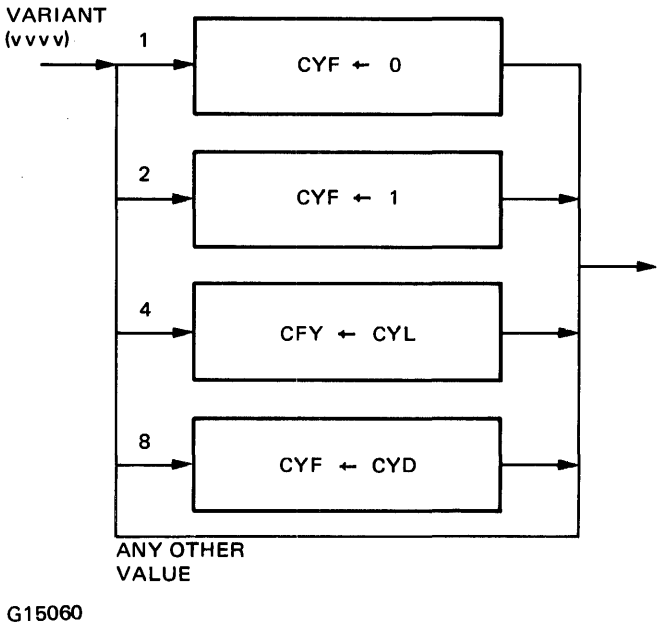
CYF, the carry flip-flop, is set to either an unconditional zero or one, or to the carry-out or borrow-out flip-flops CYL or CYD. Recall that there are three inputs to the 24-bit arithmetic unit, X, Y, and CYF; thus, the latter two cases provide means for feeding any overflow past the most significant unit on one calculation into the arithmetic unit on the next calculation.



4E Store F Into Doublepad Word

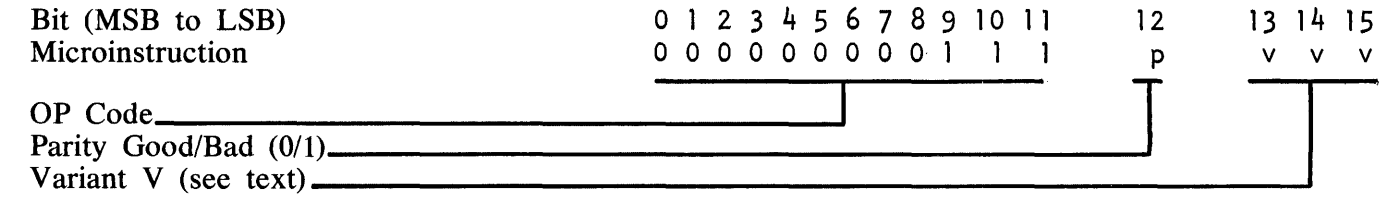


5E Load F From Doublepad Word



6E Set Carry Flip-Flop

7E READ/WRITE CACHE



The Cache Memory is accessible only through this microinstruction, aside from clearing Cache. Of the eight variant values, the first five are executable only from the console. (See Register Group and Register Select switches in the section on the Diagnostic and Maintenance Panel.) The variants are discussed separately. (vvv binary = V decimal.)

V=0: Write From Console One Word Into Block A

The 17 rightmost console switches define a 16-bit "word" plus parity, which is loaded into Cache Block A at the location addressed by A. Console switch 7 is the parity bit, which should be such as to make the 17 bits odd. Console switches 8 through 23 define the data.

The LRU bit of the Cache Index is not affected by the operation. The Validity Bit for Block A of the index is reset, indicating valid data in block A.

A is not automatically incremented by the operation, but pressing the INC switch causes A to be incremented 16 bits (one microinstruction).

V=1: Write From Console One Word Into Block B

This acts identically to variant 0, affecting Block B instead of Block A.

V=2: Read One Word From Cache to Data Lights

If there is a Hit on Cache as addressed by A, the Cache entry is read into the 16 rightmost data lights (8-23) and the parity bit will appear in data light 7. LRU for that index is set to indicate the unselected Block. No parity check is done on the data read from Cache, but both Cache Keys are checked for correct parity. A Miss results in zeroes appearing in the data lights.

A is not automatically incremented by the operation but can be incremented by one 16-bit unit by operation of the INC switch.

V=3: Read Cache Keys to Data Lights

The index portion of A is used in the normal manner to read the two Cache Keys. The data appears in the following format on this non-associative Read:

Bit	Information
0	LRU
1	0
2	HIT B
3	HIT A
4	B PARITY
5-12	KEY B
13	VALID B
14	A PARITY
15-22	KEY A
23	VALID A

Data bits, LRU bits, A-validity and parity bits are not affected. The Key fields are checked for parity; an error causes PERP(1), CD(0), and the PARITY light to be set.

V=4: (No Function Assigned)

V=5: Diagnostic Cache Write

The FA register contains an address to select a Cache location; bits 2 through 9 contain the Key and bits 10 through 17 contain the Index. LRU determines which Cache Block will be written but does not change as a result of the Write. Either good or bad parity can be forced.

Four 17-bit words are written to Cache. Words 0, 1, 2, and 3 are filled from the X, Y, T, and L registers, respectively. Bit 7 is the parity bit in each register (odd = good); the data is in bits 8 through 23. Sequence of operations:

1. Save A
2 A ← FA
3. Write X to Cache Word 0
4. Write Key portion of A to Cache Key
5. Generate and write Key parity
6. Write Y to Cache Word 1
7. Write T to Cache Word 2
8. Write L to Cache Word 3
9. Restore A

V=6: Diagnostic Cache Read Data

One word of 16 bits plus a parity bit is read from Cache to X. FA contains the address of the word in Cache; the format is similar to the normal A register schema:

FA:

*	Key	Index	Word	*
0-1	2 → 9	10 → 17	18 → 20	21 → 23

*=not used

The Read is associative; a Miss causes a Read of zeroes, a Hit occur in the block for which the Key matches if the validity bit is reset. LRU is set to the block not selected if there is a Hit. Data from Cache is returned in bits 8 through 23 of X with the parity bit is bit 7. Sequence of operations:

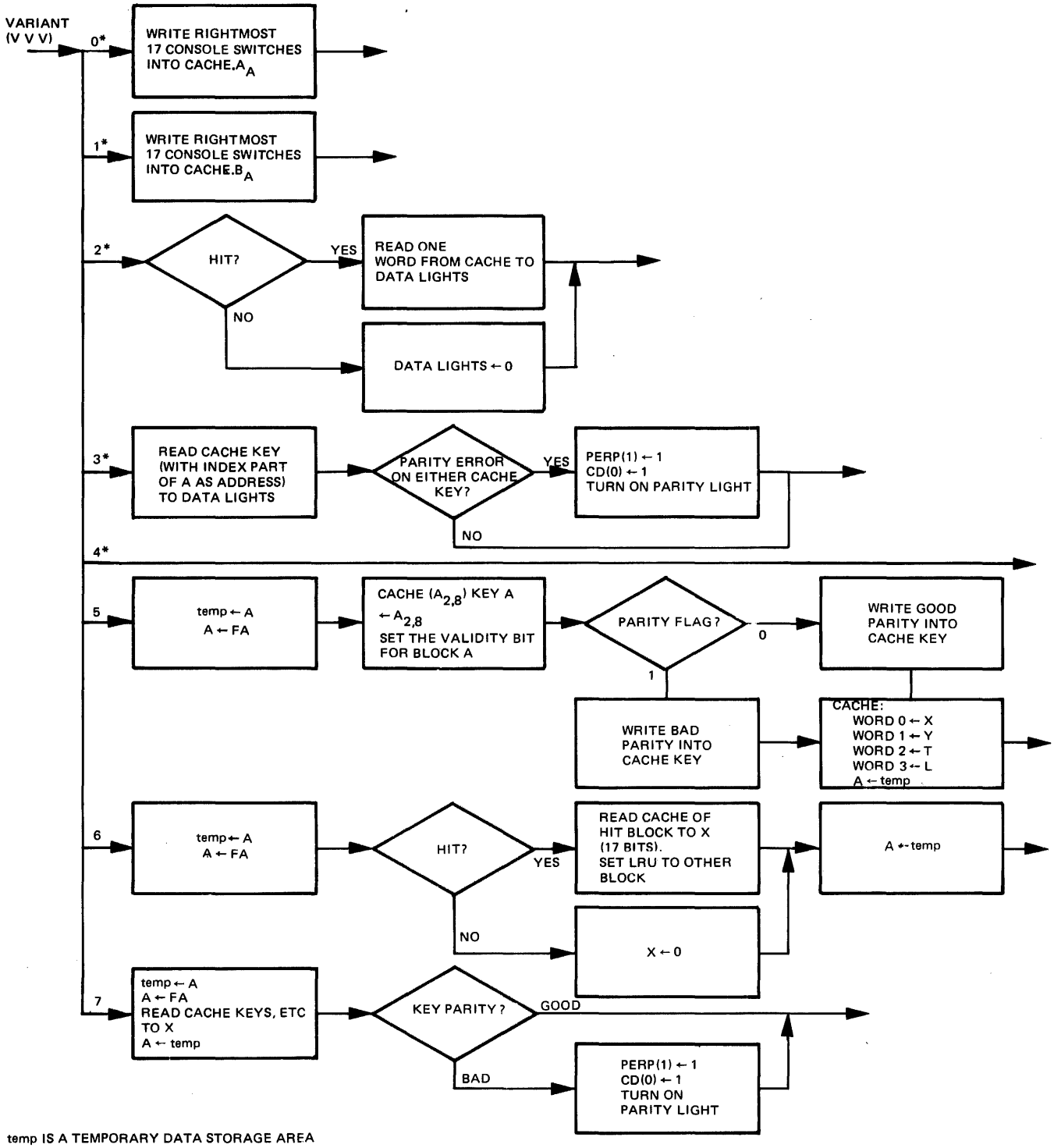
1. Save A
2. FA ← A
3. Read 17-bit Cache word to X
4. Restore A

No parity check is performed on the data, but both Keys are checked for correct parity.

V=7: Diagnostic Cache Read Keys

Bits 10 through 17 of FA are used as a Cache Index; a non-associative Read is done as described under V = 3, above, and data is returned to X in precisely the same format as for Variant 3. Cache, including the LRU bit, remains unchanged by the microinstruction. The Keys are checked for parity, with CD(0), PERP(1), and the parity light set if a parity error occurs. Sequence of operations:

1. Save A
2. A ← FA
3. Move Cache Keys, etc., to X



temp IS A TEMPORARY DATA STORAGE AREA
*FROM CONTROL PANEL ONLY.

G15061

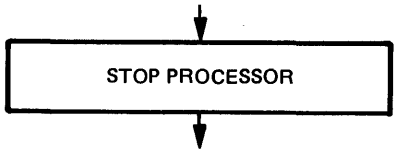
7E Read/Write Cache

1F HALT

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

OP Code

Execution of microinstructions terminates. In the RUN state, the next microinstruction has been fetched and is in the M register; likewise, A points to the second following micro. In TAPE mode, the next micro is not fetched.



G15062

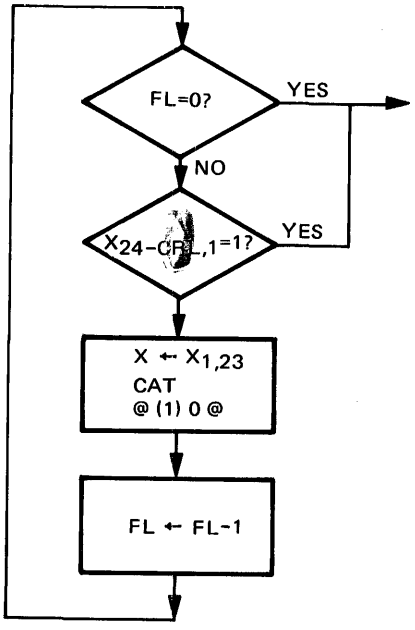
3F NORMALIZE X

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

OP Code

The contents of the X register are shifted left, with right zero-fill, while FL is counted down. The shift stops when FL = 0 or when CPL references bit 0 of X.

CPL is one-origin for this microinstruction; this means that CPL = 1 references bit 0 of X and CPL = 24 references the rightmost bit of X, bit 23. CPL = 0 is undefined.



G15063

4F TRANSFER CONTROL

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

OP Code

The 24-bit sum of L and T is moved to A. In keeping with normal concepts of A-register manipulation, the four least significant bits of this sum are truncated, as are the two most significant bits, due to the length of A. This microinstruction is the normal means of transferring between disparate bodies of firmware, as L and T may be the base and the desired displacement within the firmware to which control is given.

5F CLEAR CACHE

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

OP Code

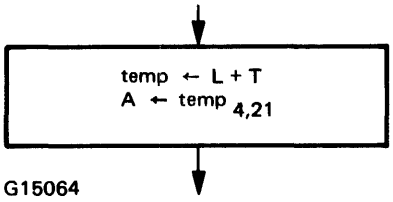
All of Cache is cleared by zeroing all Key fields, setting all Validity bits, resetting all parity bits, and setting all LRU bits. The last-named operation arbitrarily causes Block A to be first used. The microinstruction does not zero or affect the Cache data; this would serve no valid purpose.

6F INCREMENT A

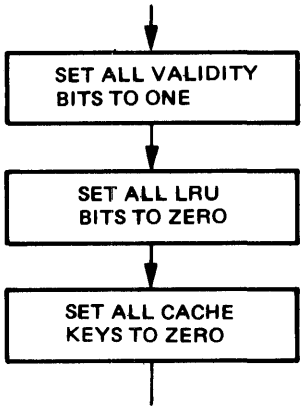
Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

OP Code

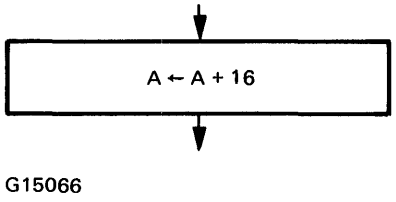
The A register is counted up by one 16-bit unit.



4F Transfer Control



5F Clear Cache



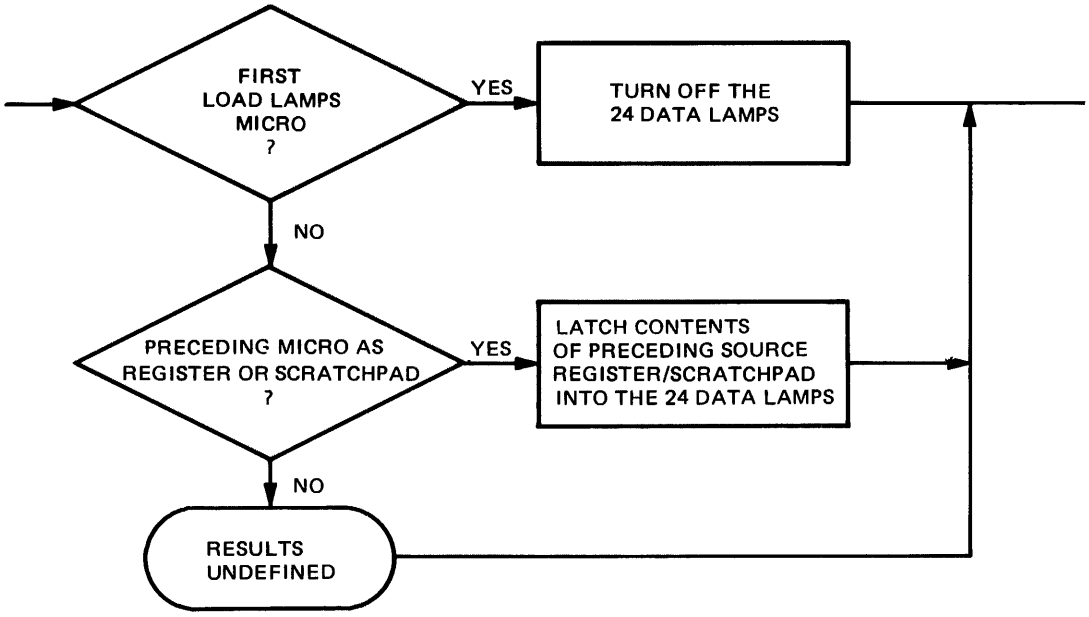
6F Increment A

7F LOAD LAMPS

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

OP Code

When the processor is in Run mode, the 24 data lamps on the D/M panel normally monitor the Main Exchange lines. The lamps appear to be glowing faintly; they are actually flickering very rapidly because of the high rate of information transfer on the lines. This behavior is altered upon the first execution of a Load Lamps microinstruction after entry into Run mode. All the data lamps are turned off until execution of a subsequent Load Lamps micro or a Halt. Subsequent Load Lamps micros are valid only immediately after a Register Move or Scratchpad Move microinstruction. The contents of the source register or Scratchpad in the preceding microinstruction are latched and continuously displayed in the lamps until another Load Lamp micro or a Halt occurs. Consequently, the firmware is able to utilize the data lamps to dynamically indicate some aspect of system behavior or status. The Load Lamps microinstruction is valid only in Normal or Cache-Only processor states. In Normal, the automatic Cache load from S Memory is not permitted between the preceding Register Move or Scratchpad Move and the Load Lamps microinstruction.



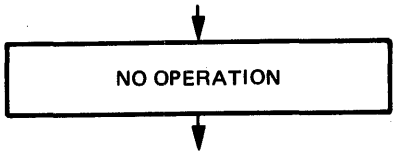
G15067

0 NO OPERATION

Bit (MSB to LSB)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Microinstruction	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OP Code

This microinstruction occupies space and time. It merely causes a skip to the next-in-line microinstruction.



G15068

SECTION 6
I/O SUBSYSTEMS and DEVICE CONTROLS

The subsections that follow provide detailed information on the operation of the individual I/O subsystems and associated device controls used in B 1800 systems. Each subsection deals with a control type (e.g., card device controls, disk pack controls). Each subsection includes the following basic topics:

INTRODUCTION: General information on the device subsystem including, where necessary, its configuration.

OPERATIONS: Detailed information on the operation codes and variants and the operation of the control.

RESULT DESCRIPTOR: Detailed information on the significance of the Result Descriptor.

The following subsystems and associated controls are covered:

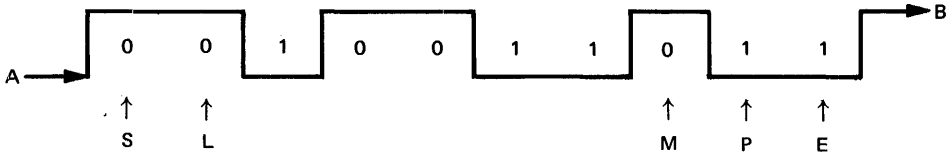
1. Display Console
2. 80-column and 96-column Card
3. Line Printer
4. Cassette
5. Magnetic Tape
6. Mini-Disk
7. Disk Cartridge
8. Disk Pack
9. Disk File
10. Reader-Sorter
11. Data Communications

DISPLAY CONSOLE SUBSYSTEM

Introduction

Operator interface to B 1800 systems is provided by the display console subsystem. The display console control (called SPO Control-2 or SPOC-2) is the link between the Central Processor and a terminal which consists of a cathode ray tube (CRT) display and a keyboard. This terminal is similar to the Burroughs TD 830 data communications terminal.

SPOC-2 uses the RS-232-C interface and may be placed on any I/O channel from 0 to 7. Data transfer between SPOC-2 and the terminal is in 8-bit (7 data, 1 parity) serial format. Transmission of ASCII 0110010, the graphic character 2, is illustrated in figure 6-1.



A = PRECEDING CHARACTER
B = NEXT CHARACTER
S = START BIT (ALWAYS 0)
E = STOP BIT (ALWAYS 1)
L = LEAST SIGNIFICANT (RIGHTMOST) BIT
M = MOST SIGNIFICANT (LEFTMOST) BIT
P = PARITY BIT (PARITY IS EVEN)

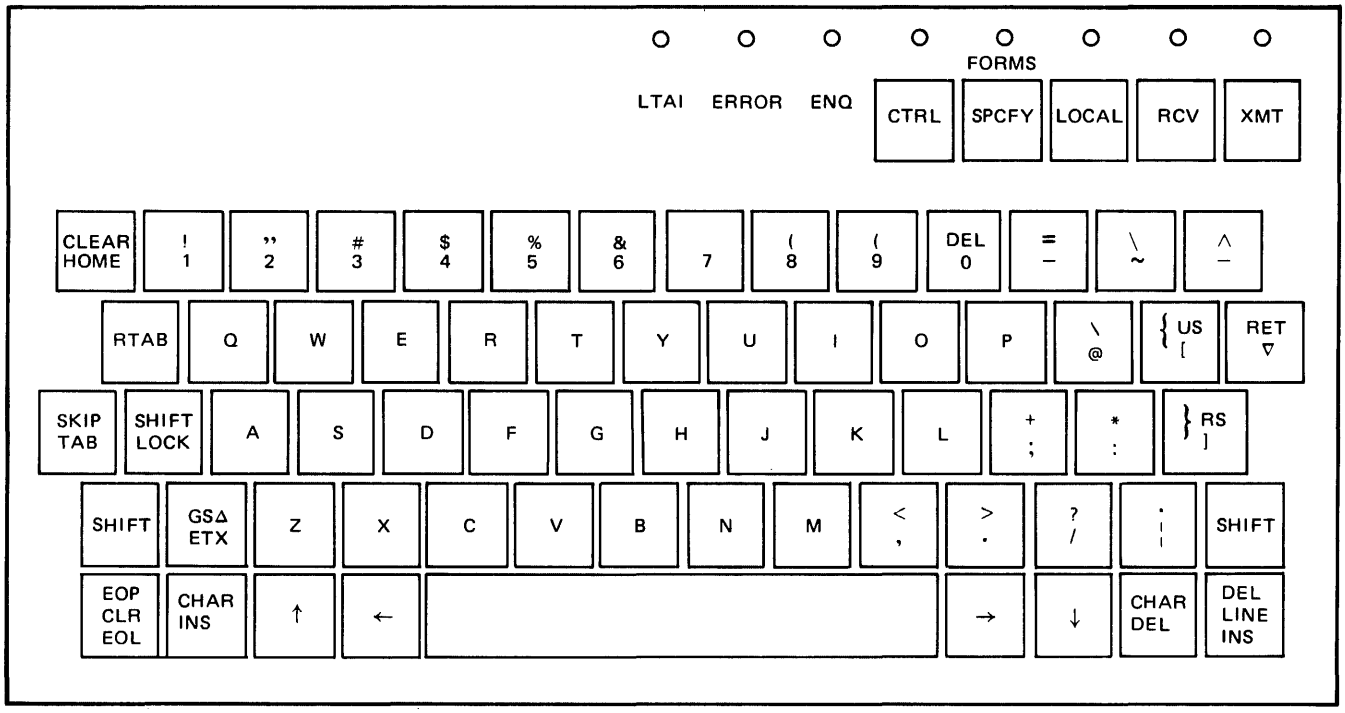
G15012

Figure 6-1. Character Transmission, Display Console Control

SPOC-2 includes a single 101-character buffer that is used for data storage on both Read and Write operations. The control translates ASCII to EBCDIC on data entry (Read), inserting a zero bit into the high-order position before translation, and translates EBCDIC to ASCII for display (Write), discarding the high-order bit in the translated result. (See the EBCDIC/ASCII translation chart in appendix B for translation specifics.)

SPOC-2 operates at a rate of 9600 baud; its transmission on a Read operation is from cursor to ETX or to end-of-screen if no ETX has been inserted.

The terminal's keyboard layout is shown in figure 6-2. Figure 6-3 shows the codes and graphics for ASCII-7.



G15013

Figure 6-2. Display Console Keyboard (B 9348-32)

Operations

Operation Codes, Display Console Control

	← 0(MSB)				23(LSB) →	
READ	0000	00BU	0000	0000	0000	0000
WRITE	0100	00B0	0000	0000	0000	0000
TEST	100R	XD00	0000	0000	0000	0000

Variants are defined in the text.

b_7 —(MSB)→					0	0	0	0	1	1	1	1
b_6 →					0	0	1	1	0	0	1	1
b_5 →					0	1	0	1	0	1	0	1
b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	↓ ROW / COL →	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P		p
0	0	0	1	1	SOH	DC 1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC 2	"	2	B	R	b	r
0	0	1	1	3	ETX ⧖	DC 3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC 4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	¦
1	1	0	1	13	CR ▼	GS Δ	–	=	M	]	m	}
1	1	1	0	14	SO	RS ◁	.	>	N	^	n	~
1	1	1	1	15	SI	US ▷	/	?	O	–	o	DEL

G15014

Figure 6-3. ASCII Character Codes for Display Console Graphics (Graphics are outlined.)

Read

The Read operation transfers data, as represented on the CRT screen, to the system. The sequence of data transfer is left to right, character by character, and from top to bottom, row by row, until an ETX is sent or until the terminal receives a Terminate Data request.

To enter data, the operator switches the terminal to LOCAL mode and begins typing. (If the terminal is in Receive (RCV) mode with no message being received, it switches to LOCAL when any non-control key is actuated.) When ETX (end-of-text) is pressed, the end-of-text graphic appears at the current cursor position and the cursor moves to the home position (row 1, column 1). Transmission takes place when Transmit (XMT) is pressed.

Transmission is from current cursor position (the operator may move it from home) forward to the ETX symbol. (Screen position 1920 (row 24, column 80) is an automatic ETX.) The terminal automatically switches into RCV if the Read is successful.

If variant B=1, SPOC-2 performs a Read Buffer operation in which the contents of SPOC-2's buffer are transferred without translation until terminated by either a Buffer Empty signal or a Terminate Data request. Data is read from the rightmost position of the buffer, following which the buffer is shifted right by one position. An empty buffer is defined to be the absence of a valid character in the rightmost position; thus, only valid data is transferred unless the buffer is initially empty, in which case one transfer of all zeros will occur at Status Count 16. Note that a buffer is empty after a normal Write.

The concept of the Block Check Character (BCC) must be mentioned at this point. BCC is a longitudinal parity-check character, algorithmically formed, that validates preceding data. It is generated by the terminal and checked by SPOC-2 on a Read; the reverse order applies on a Write. BCC normally follows the ETX and checks the entire transferred character stream.

Diagnostic operations provide for reading the control's buffer and checking its UART (Universal Asynchronous Receive/Transmit) chip. If the U variant is set, the following sequence of events is performed:

1. Data is shifted right in the buffer until a valid character reaches the rightmost position. Results are undefined if no valid character is present in the buffer.
2. Data is transferred through the UART chip and back into the leftmost side of the buffer. The transfer is terminated solely by absence of a valid character, not by the presence of an ETX. A special WRITE-BCC is generated on the data going to the UART and a READ-BCC on the data being placed in the buffer. Both codes appear in the buffer. Due to the expansion of the character count, only 99 valid characters are permitted in the SPOC-2 buffer prior to this operation.
3. Data is again right-justified as defined in a., above.
4. Data is transferred back to the system as in a normal Read, terminated by an ETX or a Terminate Data command. Should an ETX or a READ-BCC appear, the operation will be terminated prior to the transfer of the WRITE-BCC, leaving the buffer uncleared.

Write

A Write to the display console can only be accomplished when the terminal is in RCV mode. Should this not be the case, an alert tone is sounded. Data to be written, which must include an ETX character, is sent to SPOC-2 and on to the terminal in 101-character bursts. The terminal receives the entire message, then displays it.

Should the B variant be set, a Diagnostic Write is performed, wherein the SPOC-2 buffer is loaded until terminated by a full buffer or by a Terminate Data request. Data is loaded from the left and shifted right as a new character appears. A full buffer is defined as a character in the rightmost buffer position. Termination by the Terminate Data command leaves the data non-right-justified.

Test

The R and X variants affect the results of the SPOC-2 Test operator:

RX=00
The Result Descriptor is returned immediately, along with terminal mode (Ready, Not Ready, Local, Receive, or Transmit) and control ID (@2E@).

RX=01
The Result Descriptor is returned after the terminal enters Transmit mode. Neither terminal mode nor control ID are returned.

RX=10
The Result Descriptor is returned after the terminal enters Receive mode. Neither terminal mode nor control ID are returned.

RX=11
The Result Descriptor is returned after the terminal enters either Receive or Transmit mode. Mode and control ID are returned. If the D variant is set, a pseudo Test cycle is initiated. No test is made for terminal mode.

The Test operation serves two purposes. In the normal (RX=00) mode, the current status of the control and terminal is ascertained, including mode, readiness, and ID. When altered by the RX variants, the operation becomes a Test and Wait for specific circumstances.

A Test and Wait on a terminal with power off will normally complete when power is applied and the appropriate mode is achieved. However, line transients during the power-up sequence might cause the mode report to be incorrect.

If other operations are initiated on SPOC-2 when it is in the Test and Wait state, the control must be cleared with a Test Status and Clear from the I/O Driver before initiation can be completed. No result is stored for this Test.

Result Descriptor

The Result Descriptor for the display console control is listed below. Bits not included are reserved.

Result Descriptor, Display Console Control

Bit	Meaning	Operations
0	Operation complete	All
1	Exception (Bits 2, 11, or 12 set)	Read, Write, Test*
2	Unit not ready	Read, Write, Test*
11	Time out	Read, Write
12	Data error	Read, Write
13	Local	Test*
14	Receive	Test**
15	Transmit	Test**
16	Operation complete	All
17-23	Control ID: 0101110 (@2E@)	Test**

* When RX=00
** When RX=00 or 11

Not Ready

Not Ready is defined as one of the following: (1) terminal off during a Test with RX=00, (2) terminal off or in Local or Receive mode on Read or (3) off, Local, or Transmit on Write, (4) busy moving data from a previous Write between the communications buffer and the display buffer when a new Write is initiated.

Timeout

A timeout occurs after 4 milliseconds under the following conditions: (1) no response from the terminal on Read, (2) a timeout period between individual characters ends during a Read, (3) no response is received on a Read after the normal ACK response to a message is sent, (4) no response to two normal parts of the polling sequence for a Write (EOT-ENQ or ETX-BCC). No response to EOT-ENQ can indicate that the terminal is off.

Data Error

This bit is set if a NAK is received from a terminal in response to a transmitted message. It indicates one of several errors: BCC error, terminal-detected parity error, BCC parity or character parity error detected by SPOC-2 on a Write operation.

Mode

In response to a Test operation with RX=00, either the Not Ready bit or one of the three mode bits (Local, Receive, Transmit) is set.

Control ID

The control identification is 0101110 (@2E@).

CARD SUBSYSTEMS

The B 1800 I/O subsystem includes controls and peripheral devices that enable all standard punched card operations to be performed with either 80-column or 96-column cards. These operations are Read, Punch, and Print. Read-only and punch-only as well as multipurpose (read-punch-print) peripheral devices are available.

All controls are capable of translating the appropriate card code to internal EBCDIC (Read), EBCDIC to card code (Write), or both. Translation from card code to print code takes place within the device.

All controls are also capable of dealing with binary data wherein each punch position is defined and transferred as either a zero or one bit.

The different control types are discussed in the subsections that follow.

80-COLUMN CARD READER CONTROL

Introduction

The 80-column card reader control (CRC80) accepts standard EBCDIC card code from the card reader. Eighty columns of data (960 bits) are transferred bit-serially from the reader to the control, translated if so specified to 8-bit EBCDIC internal code, and stored.

If translation is specified, 256 possible valid hole combinations can be handled by the control; invalid combinations are translated to the "?" character. The contents of each card column occupy one 8-bit byte in memory. Eighty bytes are required for each card read; the I/O Driver supplies blanks for cards with less than 80 bytes.

In binary mode, translation is bypassed and the 960 bits (eighty 12-bit columns) are stored as ones and zeroes. As above, the I/O Driver supplies blanks to fulfill the 80-column requirement.

Operations

Operation Codes, 80-Column Card Reader Control

	← 0(MSB)					23(LSB) →
READ	000B	0000	0000	0000	0000	0000
TEST	100V	V000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

Definitions of Variants

Bit	Meaning
B	Code translation.
0	Translate card code to EBCDIC.
1	Do not translate (binary mode).
VV	Test variant.
00	Return result immediately.
01	Return result when unit goes Not Ready.
10	Return result when unit goes Ready.
11	Not valid.

Read

Eighty columns of data are read to the control, translated to EBCDIC if so specified by the B variant, and transferred to memory. A Result Descriptor is returned.

Test

The unit is tested for Not Ready and the control is requested to report its ID. The Result Descriptor is reported as specified by VV.

Pause

The Pause operator never appears in the linked chain of I/O Descriptors. It is generated by the I/O Driver upon reaching a descriptor not yet ready for execution, and tells the control to return a service request after a pause of 7 to 8 milliseconds. Bit 16 in the Result Descriptor, returned after the request has been serviced, is reset (zero).

Stop

Stop, performed by the I/O Driver and never sent to the control, enables the MCP to instruct the I/O Driver to stop linking through the descriptor chain and return a result.

Result Descriptor

The Result Descriptor for the 80-column card reader control is listed below. Bits not included are reserved. Discussions of the individual exceptions may be found in the subsection on the 80-column card read-punch-print control. Result Descriptor, 80-Column Card Reader Control

Bit	Meaning
0	Operation complete.
1	Exception: bits 2, 3, 6 (any or all) set.
2	Not ready. *
3	Validity error. (Invalid character translated to ?.)
6	Read check.
16	Second operation complete bit.
17-22	Control ID: 0101010 (@2A@). Returned on Test only.

* Not Ready is defined to be any of the following:
Power off or not yet fully up. START not yet pressed. STOP pressed. Open interlock. Feed failure (feed check). Card jam. Empty hopper or empty wait station. Stacker full. Read check.

80-COLUMN CARD PUNCH CONTROL

Introduction

The 80-column card punch control (CPC80) handles punch-only peripheral units. The control executes I/O descriptors and controls the punching of data in either EBCDIC mode or in binary mode. In the EBCDIC mode, data is sent three 8-bit bytes at a time to the control until 80 bytes are transferred or until the B-Address is reached, whichever comes first. Because the unit's punch buffer requires 80 columns of data in order to punch, the I/O Driver supplies blanks if the B address is reached before 80 bytes are transferred. The control translates EBCDIC to card code and sends 960 bits (12 per column) serially to the unit.

In binary mode, data is sent two 12-bit columns at a time to the control until 80 columns are transferred or until the B-Address is reached. As described above, the I/O Driver blank-fills to assure the unit its required 80 columns. The control forwards the 960 bits of data, untranslated, bit-serially to the unit.

The control provides an automatic echo check that verifies that eighty data bits are received for each row and that 12 rows are transferred. Furthermore, a comparison is made between the number of holes actually punched and the number of one bits transferred to the unit. A failure on either test causes punch error to be flagged in the Result Descriptor.

Punch units may be equipped with three stackers, "normal," "auxiliary," and "error." The error stacker is usually reserved for storing mispunched cards for later discard.

Operations

Operation Codes, 80-Column Card Punch Control

	← 0(MSB)					23(LSB) →
WRITE	010B	00SS	0000	0000	0000	0000
TEST	100V	V000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

Definitions of Variants

Bit	Meaning
B	Card translation.
0	Translate card code to EBCDIC.
1	Do not translate (binary mode).
SS	Stacker selection.
00	Error stacker.
01	Normal stacker.
10	Auxiliary stacker.
VV	Test variant.
00	Return Result Descriptor immediately.
01	Return Result Descriptor when unit goes Not Ready.
10	Return Result Descriptor when unit goes Ready.
11	Not valid.

Write (Punch)

A card feed is initiated. Data is transferred from ascending memory locations beginning at the location specified by the A Address and ending after 80 columns are transferred or when the B address minus 1 is reached. Data is translated or not as specified by the B variant, then transferred to the punch unit where 80 columns are punched. The card is stacked as specified by the SS variant.

Test

The unit is tested (VV variant). The control is requested to report its ID.

Pause

Pause never appears in the linked chain of I/O Descriptors. It is generated by the I/O Driver upon reaching a descriptor not yet ready for execution, and tells the control to return a service request after a pause of 7 to 8 milliseconds. Bit 16 in the Result Descriptor, returned after the request has been serviced, is reset (zero).

Stop

Stop, performed by the I/O Driver and never sent to the control, enables the MCP to instruct the I/O Driver to stop linking through the descriptor chain and to return a result.

Result Descriptor

The Result Descriptor for the 80-column card punch control is defined below. Bits not included are reserved. All exceptions are reported on all operators unless otherwise noted. Result Descriptor, 80-Column Card Punch Control

Bit	Meaning
0	Operation complete.
1	Exception: bits 2, 3, 5 (any or all) set.
2	Not ready. (Reported on Write or Test only.)
3	Punch error.
5	Memory parity error.
16	Second operation complete bit.
17-23	Control ID: 0000100 (@04@).

Not Ready

Not Ready is defined to be any of the following conditions:

Power off or not yet fully up.
START not yet pressed.
STOP pressed.
Open interlock.
Feed failure.
Card jam
Empty hopper or empty wait station.
Stacker full.
Punch die not in place.
Punch error (B 9210 only).

If the punch unit is not ready when a Write is sent to the control, the control accepts one bufferload of data and sets the Not Ready bit in the Result Descriptor.

The Not Ready conditions listed above may occur after card feed begins. The following paragraphs define most of the possible events.

Power Off

In the case of inadvertent power down, including the opening of an interlock, the result is undefined.

Stop

If STOP is pressed or if an empty hopper, empty wait station, or full stacker condition occurs, the current operation is completed and Not Ready is reported when the next operation is sent to the control.

Feed Failure

Not Ready is reported for the card that fails to feed. This card remains in the feed hopper or the wait station.

Card Jam

The feed mechanism stops and the result is undefined.

Punch Error

Punch error is reported on failure of the "echo" check, a real time comparison between holes being punched and one bits sent to the unit. The punch error report is returned in time to permit repeat punching. Recovery is programmatic.

Memory Parity Error

Memory parity error in data transferred to the control and the punch unit is checked by the I/O Driver following the punch operation. Therefore, the card is stacked normally. The I/O Driver reports the error and terminates linking. The MCP reports an error message at the operator's display console; this message identifies the stacker to which the card was routed. The MCP then waits for the unit to go Not Ready, then Ready, indicating that the operator has removed the card. Processing resumes and a card is repunched under MCP direction.

80-COLUMN-CARD READ-PUNCH-PRINT CONTROL

Introduction

The Data Recorder

The B 1800 80-column card read-punch-print control (RPP80) enables on-line use of the B 9418 Data Recorder for card reading, punching, and printing. These operations can be performed individually or in any combination on each card. Punch information and print information for the same card can be identical or different.

The data recorder, which can also be used off line for keypunching, interpreting, duplicating, verifying, and merging cards, includes two feed hoppers, a read station, a wait station, a print station , a punch station, a post-punch read station, and two stackers.

A factory-installable option permits use of 51-column cards.

Read Check

Each card fed undergoes a read check. When a read check problem is encountered, the unit remains ready and Read Check is reported to the control. Feed of the next card causes the condition to be reset. (This is a function of the Unit Option switch, which must be preset at the factory or by the Burroughs Field Engineer to position 2.)

Punch Check

Punch checking provides verification that data sent by the control to the data recorder's punch buffer is identical with data read at the post-punch read station. A failure causes the unit to go Not Ready.

Stacker Selection

Stacker selection has two modes, termed "stacker select" and "overflow." In stacker-select mode, all error cards, except punch check error cards, are routed to the stacker specified in the SSS variant. Punch check error cards are routed to stacker 2, regardless of the SSS variant value, along with as many as two following cards. A stacker-full signal is emitted when either stacker reaches capacity.

In overflow mode (variant SSS=011), stacking is governed by the setting of a manually operated "outstack" switch. With outstack ON, non-error cards are routed to stacker 1 and all error cards to stacker 2. A stacker-full signal is emitted when either stacker reaches capacity. With outstack OFF, all non-error cards go to stacker 1 until it reaches capacity and then to stacker 2, and all error cards are routed to stacker 2 at all times. The stacker-full signal is not emitted until stacker 2 reaches capacity; that is, when both stackers are filled. The overflow mode, once set, is in effect until manually reset.

Operations

Operation Codes, 80-Column Read-Punch-Print Control

	← 0(MSB)			23(LSB) →		
READ	0000	0SSS	10IH	0B0C	0000	0000
STACKER SELECT & READ	0001	0SSS	00IH	0B0C	0000	0000
PUNCH	0100	0SSS	00IH	0B00	0000	0000
PRINT	0010	0SSS	00IH	0B00	0000	0000
PUNCH & PRINT	0110	0SSS	0WIH	0B00	0000	0000
PUNCH & PRINT & READ	0XX1	0SSS	0WIH	0B0C	0000	0000
TEST	100V	V000	0000	0000	0000	0000

Definitions of Variants

SSS	Stacker selection.
000	Error stacker.
001	Stacker 1.
010	Stacker 2.
011	Overflow mode. If set, remains until manually cleared.
100 to 111	Not valid.

I	Inhibit feed
0	Do not inhibit.
1	Inhibit feed of next card.
H	Hopper selection.
0	Primary hopper.
1	Secondary hopper.
B	Card translation
0	Translate.
1	Do not translate (binary mode).
W	Punch/print equivalency.
0	Punch and print data are identical.
1	Punch and print data are non-identical.
XX	Action variant for Punch Print Read operator
00	Same as Stacker Select and Read operator.
01	Print card in wait station, read card in H-specified hopper. (W must be 0.)
10	Punch card in wait station, print card in H-specified hopper. (W is irrelevant.)
11	Punch and print card in wait station, read card in H-specified hopper. (W may be 0 or 1.)
VV	Test variant.
00	Return Result Descriptor immediately.
01	Return Result Descriptor when unit goes Not Ready.
10	Return Result Descriptor when unit goes Ready.
11	Undefined.

Read

If the data recorder's read buffer has data at the start of this operation, an 80-character transfer is made to the control. The card in the wait station is stacked as specified by the SSS variant, and a new card is read to refill the buffer. If the buffer is empty at the start, a card is fed, read to the buffer, and stacked. This data is transferred to the control. A second card is fed, read to the buffer, and stopped at the wait station. The data from this second card is in the data recorder's read buffer at the end of the operation.

Should a validity error be detected, feed of the next card is inhibited. The Result Descriptor reflects the validity error, depending on the setting of the C variant, and the invalid card is stacked.

An empty hopper condition is not reported while the read buffer is full. When the next Read is initiated, however, the buffer empties and the appropriate hopper (primary or secondary) is reported as empty.

Stacker Select and Read

A card in the wait station is moved to the stacker selected by the SSS variant or overflow rules previously described. Card feed is initiated. The new card is read, its data is transferred from the read buffer to the control, and the card stops at the wait station. The read buffer must be initially empty. The discussion of Read, above, is appropriate for this operation as well.

Punch

A card is moved from the wait station to the punch station for punching, to the post-punch read station for punch check, and through the print station to the stacker specified by the SSS variant or overflow rules. A new card is fed, read-checked, and stopped at the wait station. Any read check error is reported. A card must be present in the wait station at the start of this operation. No attempt is made to feed from an empty hopper; this condition is reported in the Result Descriptor.

Print

Data from memory is sent by the control to the data recorder's punch buffer, translated from card code to print code, and moved to the print buffer for printing.

Details of card movement are as described under Punch, above.

Punch and Print

Information from memory is punched into a card; equal or different information is printed on the same card. Punch and print data must each define 80 positions in the manner appropriate for the mode (binary or EBCDIC) specified by the B variant. If punch and print data are equal, 80 columns of data are expected; if different, 160 columns. The W variant provides this information.

Details of card movement are as described under Punch, above.

Punch, Print, and Read

Data from memory is punched and/or printed into a card as described under Punch and Print, above. This card is stacked as specified by the SSS variant or by the overflow rules, and a new card is fed. Data from the new card moves from read buffer to control, then to memory locations immediately following those from which the output (punch and/or print) data was drawn. The new card stops at the wait station.

Test

The data recorder is tested and the result is stored as specified by the VV variant. Three items are tested: hopper not ready, hopper 1 ready, hopper 2 ready.

Stop

The Stop operation is provided by the I/O Driver on MCP request. It is never sent to the control. It specifies that linking be stopped and a Result Descriptor returned. An interrupt is provided on request.

Pause

This operation is generated by the I/O Driver to allow suspension of activity to the control should a descriptor be encountered which is not yet set up for dispatching. The Pause descriptor, being a random phenomenon, will not appear in the linked descriptor chain. The operation specifies an 8-millisecond pause, then the return of a Service Request. The second operation-complete bit (bit 16) in the Result Descriptor is reset (0).

Result Descriptor

The Result Descriptor for the 80-column read-punch print control is defined below. Bits not included are reserved.

Result Descriptor, 80-Column Read-Punch-Print Control

Bit	Meaning	Operations
0	Operation Complete.	All
1	Exception: bits 2,3,5-10 (any) set	All
2	Not Ready.	All
3	Validity Error.	Read
5	Memory Parity Error.	Write
6	Read Check.	All
7	Punch Check.	Write
8	Primary Hopper Empty.	Write,Read,Test
9	Secondary Hopper Empty.	Write,Read,Test
10	Input Check.	Write,Read
16	Operation Complete.	All
17-23	Control ID: 00000010 (@02@)	Test,Pause

Not Ready

Not Ready is defined to be any of the following:

1. Input check error.
2. Output check error; stacker full, feed check, open interlock, post wait-station jam, early or late arrival of card at punch or print station.
3. Wait station and both feed hoppers empty.
4. Stop/Reset key pressed.
5. Punch check error.

If any of the conditions listed occurs before an operation starts, the control escapes by moving through the status count sequence: STC6-STC10, STC18-STC13, and STC1. This also holds true for an incomplete Read operation.

If Not Ready is detected while the control is in STC14 or STC16 (data transfers) on a Write operation, the data is discarded and the exit sequence becomes STC14 or STC17 and STC7-STC10, STC18-STC23, and STC1.

A Not Ready from an input check error is reported immediately and bits 2 and 10 in the Result Descriptor are set. If the operation includes punching and/or printing, the output card is correct.

A Not Ready from an output check error is reported immediately and the operation is terminated. This does not apply to stacker-full conditions.

If the hoppers and wait station go empty or the STOP/RESET button is pressed, the appropriate Not Ready condition is reported before the next scheduled operation begins.

Validity Errors

A validity error is defined to be reading of an invalid card code while variant C (invalid character flag) is not set. For the Stacker Select and Read operator, the card being read stops in the wait station, and can be sent programmatically to a specific stacker. The setting of variant I (inhibit feed) determines whether or not a new card is fed. In the case of a plain Read operation, the card is ejected normally but no card is fed.

Memory Parity Errors

This bit indicates that a data parity error occurred in information transferred to the control on a Read or Read and Write. The sequence is terminated normally.

Read Check Errors

Read Check errors are reported whenever they occur for every card that passes through the read station, whether or not a Read operation is specified. The Unit Option Switch must be in position 2, which specifies that the unit will remain ready.

Stacking of the bad card is controlled by the Outstack switch. Should the operation be a Stacker Select and Read, the card remains in the wait station for subsequent programmatic disposal. Variant I (Feed Inhibit) is set as desired.

Punch Check Errors

A Punch Check error can affect the disposition of as many as three cards: the one in error, a card moving to the punch station, and one in the wait station. Not Ready is reported only upon a subsequent operation. All three cards normally are sent to the error stacker.

Empty Hopper Conditions

As mentioned previously, an empty hopper condition is not reported if read data is obtainable from the data recorder's read buffer. Should this buffer be empty, the error condition is reported. The condition is also reported if the card in the wait station is punched and the hopper selected for the next card feed is empty. Note that the status of both hoppers is reported on Test.

Input Check Errors

If a feed is initiated and no card has reached the read station after 800 milliseconds, the data recorder goes not ready and bits 2 and 10 are set.

Second Operation Complete Bit

For all operations except Pause, Bit 16 is set as well as bit 0.

96-COLUMN CARD READ-PUNCH-PRINT CONTROL

Introduction

The B 1800 96-column card read-punch-print control (RPP96) handles a data recorder similar to the 80-column device described in the preceding subsection. Introductory statements on read check, punch check, and stacker selection in that subsection apply here also.

Operation Codes, 96-Column Read-Punch-Print Control

	← 0(MSB)			23(LSB) →		
READ	0000	0SSS	10IH	0B00	0000	0000
STACKER SELECT & READ	0001	0SSS	00IH	0B00	0000	0000
PUNCH	0100	0SSS	00IH	0B00	0000	0000
PRINT	0010	0SSS	00IH	0B00	0000	0000
PUNCH & PRINT	0110	0SSS	0WIH	0B00	0000	0000
PUNCH & PRINT & READ	0XX1	0SSS	0W0H	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000
TEST	100V	VP00	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

Definitions of Variants

SSS — Stacker selection
000 — Error stacker.
001 to 110 — Stacker 1 to Stacker 6, respectively.
111 — Overflow mode; remains in effect until manually reset.

I — Inhibit feed
0 — Do not inhibit.
1 — Inhibit feed of next card.

H — Hopper selection.
0 — Primary hopper.
1 — Secondary hopper.

B — Card translation
0 — Translate.
1 — Do not translate (binary mode).

W — Punch/print equivalency.
0 — Punch and print data are identical.
1 — Punch and print data are non-identical.

XX — Action variant for Punch Print Read operator
00 — Same as Stacker Select and Read operator.
01 — Print card in wait station, read card in H-specified hopper. (W must be 0.)
10 — Punch card in wait station, print card in H-specified hopper. (W is irrelevant.)
11 — Punch and print card in wait station, read card in H-specified hopper. (W may be 0 or 1.)

VV — Test variant.
00 — Return Result Descriptor immediately.
01 — Return Result Descriptor when unit goes Not Ready.
10 — Return Result Descriptor when unit goes Ready.
11 — Undefined.

P — Pause initiation flag. Recognized by the I/O Driver only.
0 — Test and return result in the manner specified by VV.
1 — Ignore VV, initiated Pause, do not store result. After 8 milliseconds, the next I/O Descriptor, with RS bits 0 and 1 set, is initiated.

Details of these operations correspond quite closely to those given for the 80-column device controls.

Result Descriptor

The Result Descriptor for the 96-column read-punch print control is defined below. Bits not included are reserved.

Result Descriptor, 96-Column Read-Punch-Print Control

Bit	Meaning	Operations
0	Operation complete.	All
1	Exception: any or all bits 2,3,6-10 set.	All
2	Not Ready.	Read, Write
3	Control card.	Read
6	Read check.	Read, Write
7	Punch check.	Write
8	Primary hopper empty.	All
9	Secondary hopper empty.	All
10	Feed check.	Write
16	Operation complete.	All
17-23	Device ID: 0000101 (@05@)	Test

Not Ready

Not ready is defined to be any of the following:

1. Input check error.
2. Output check error; stacker full, feed check, open interlock, post wait-station jam, early or late arrival of card at punch or print station.
3. Wait station and both feed hoppers empty.
4. Stop/Reset key pressed.
5. Punch check error.

A Not Ready from an input check error is reported immediately and bits 2 and 10 in the Result Descriptor are set. If the operation includes punching and/or printing, the output card is correct.

A Not Ready from an output check error is reported immediately and the operation is terminated. This does not apply to stacker-full conditions.

If the hoppers and wait station go empty or the STOP/RESET button is pressed, the appropriate Not Ready condition is reported before the next scheduled operation begins.

Control Card

A control card is defined as a card with an invalid character in column 1. This is interpreted (printed on the card) as a ? character. A control card is sent to the error stacker and feed of the next card is inhibited on read-punch-print devices. Bits 2 and 3 in the Result Descriptor are set when a control card is encountered on all devices.

Read Check Errors

Read Check is a comparison of card data with read buffer data for that card. Read Check errors are reported whenever they occur for every card that passes through the read station on an operation that specifies Read. The unit remains ready but no new card is fed.

On Stacker Select and Read operations, read-punch-print devices, the card that triggers the check remains at the wait station unit a another Stacker Select and Read with I=1 is initiated.

Punch Check Errors

Punch Check is a comparison of punch buffer data with that data that has actually been punched into the card. A Punch Check error can affect three cards: the one in error, a card moving to the punch station, and one in the wait station. Not Ready is reported only upon a subsequent operation. All three cards normally are sent to the error stacker.

Empty Hopper Conditions

An empty hopper condition is reported after all hoppers and the device's read buffer go empty. The condition is also reported after the card in the wait station is released if the hopper selected for the next card feed is empty. Note that the status of both hoppers is reported on Test.

Input Check Errors

If a feed is initiated and no card has reached the read station after 800 milliseconds, the device goes not ready and bits 2 and 10 are set.

Second Operation Complete Bit

For all operations aside from Pause, Bit 16 is set as well as bit 0.

LINE PRINTER SUBSYSTEM

Introduction

Two controls, Printer Control-4 (PC-4) and Printer Control-5 (PC-5) interface the system with a variety of 120-and 132-column line printers. These printers range in print speed from 85 to 1500 lines per minute. Either control may occupy any channel from 0 to 14; typically, printer controls use channels 1, 2, 3 or 4 to be higher than the SPO and card devices.

PC-4 controls the B 9249 series of chain printers, used where print requirements are relatively modest. The series includes three models with speeds of 86, 150, and 250 lines per minute. PC-5 controls the B 9247 series, with speeds of 400, 750, 1100, or 1500 lines per minute. One control interfaces with one printer.

Both control types include one 132-byte buffer, which represents the maximum number of characters on a print line. Some printers have shorter lines (120 characters, or 80 characters); for these, the control cannot look for a full buffer. Instead, data transfer is terminated, the control switches to Status Count 17 to receive the last bytes, and blank-fills the buffer.

PC-5 transfers paper motion information to the printer and returns the Result Descriptor to the I/O Driver after all non-blank characters have been printed, whereas PC-4 returns the Result Descriptor after all characters have been printed. Both controls permit the buffer to be filled while paper motion from the prior Write is in process. Buffers in the printers also may be filled during the paper motion period.

Code Translation and Print Trains

PC-4 provides hardware translation from EBCDIC, used within the system, to ASCII, required by the printer. All 256 EBCDIC characters are first translated to ASCII-8; then, the high-order bit is dropped to yield ASCII-7. The ASCII-7 code of seven ones (DEL) or any ASCII-7 code whose two high-order bits are 00 are translated to hexadecimal 3F, the question mark ("?") graphic. This graphic represents control codes. Tables B-1 and B-2 (Appendix B) provide EBCDIC/ASCII and ASCII/EBCDIC correspondences.

Table 6-1 shows the graphic set for the standard 48- and 64-character print chains used on printers serviced by PC-4. The graphics are displayed in a tabular EBCDIC column/row format. The columns signify the most significant four bits of the EBCDIC character, translated into hexadecimal format; similarly, the rows signify the least significant four bits of the character.

For example:

column/row 7/B = @7@/@B@ = 0111/1011 = decimal 123

PC-4 also services printers using a 96-character katakana print chain. An optional katakana translator adapter is used; this disables the standard EBCDIC/ASCII translator in the control and provides translation between internal EBCDIC and the katakana chain.

Table 6-1. PC-4: Graphics for 48-and 64-Character Print Chains

LEFTMOST FOUR BITS

RIGHTMOST FOUR BITS: COL / ROW	4	5	6	7	C	D	E	F
0	SPACE	&	-				\	0
1			/		A	J		1
2					B	K	S	2
3					C	L	T	3
4					D	M	U	4
5					E	N	V	5
6					F	O	W	6
7					G	P	X	7
8					H	Q	Y	8
9					I	R	Z	9
A	[◢	] ◢		: ◢				
B	.	$	,	#				
C	< ◢	*	%	@				
D	(◢	) ◢	— ◢	'				
E	+ ◢	; ◢	> ◢	= ◢				
F	! ◢	¬ ◢	? ◢	" ◢				

◢ = 64-CHARACTER CHAIN ONLY

The graphics corresponding whith this special code are shown in table 6-2. Note that the EBCDIC codes for "@", "(", ")", and ":" differ from those given in table 6-1.

Codes shown as blank entries in table 6-2 are translated into ASCII 3/F, the "?" character, and are printed as such.

PC-5 provides translation from the system's internal (EBCDIC) code to a printer code (link numbers) by means of a firmware memory that is loaded from main memory by the MCP. Each link number is related to a specific character position on a given print train and, thus, to a specific character on that train. EBCDIC numbers are shown in the column/row format described for tables 6-1 and 6-2. Link numbers are also in hexadecimal format.

For "standard" print trains, the firmware memory is designed to relate the EBCDIC codes to link numbers corresponding, for the most part, to the graphic set shown in table B-1 (Appendix B). However, a variety of print trains are available, as shown in tables 6-3A and 6-3B.

Main memory is loaded with codes appropriate to specific groups of print trains from disk files provided with the printers, which contain standard translation sequences. EBCDIC to link number correspondences for the two sets of line printers serviced by PC-5 are shown in tables 6-4A and 6-4B.

Operations

Operation Codes, Line Printer Control

	← 0(MSB)					23(LSB) →
WRITE	010P	SSSS	DD00	0000	0000	0000
SPACE/SKIP	101P	SSSS	0000	0000	0000	0000
LOAD TRANSLATOR*	0110	0000	DD00	0000	0000	0000
TEST	100R	0000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000

* PC-5 only.

Definitions of Variants

Bit	Meaning
SSSS	Space/Skip after printing.
0000	No paper advance.
0001	Skip to channel
to	1 ... 12
1100	(Channel 12 valid with PC-5 only.)
1101	Skip to first line; 1500-lpm printer only. (This variant is not presently used by any software.)
1110	Single space.
1111	Double space.
DD	PC-5 diagnostic variants (discussed in text).
P	End-of-page-handling variant.
R	Wait-until-ready variant.

Table 6-2. PC-4: Graphics for 96 Character Katakana Chain

LEFTMOST FOUR BITS

RIGHTMOST FOUR BITS: COL / ROW	4	5	6	7	8	9	A	B	C	D	E	F
0	SPACE		-			ー						0
1			/		｡	ｱ	ﾁ		A	J		1
2					｢	ｲ	ﾂ		B	K	S	2
3					｣	ｳ	ﾃ		C	L	T	3
4					､	ｴ	ﾄ		D	M	U	4
5					･	ｵ	ﾅ		E	N	V	5
6	･				ｦ	ｶ	ﾆ		F	O	W	6
7					ｧ	ｷ	ﾇ		G	P	X	7
8					ｨ	ｸ	ﾈ		H	Q	Y	8
9					ｩ	ｹ	ﾉ		I	R	Z	9
A					ｪ	ｺ	ﾊ	ﾚ				
B	.	@	,	#				ﾛ				
C	(	*			ｬ		ﾌ	ﾜ				
D					ｭ	ｽ	ﾍ	ﾝ				
E	+		)	:	ｮ	ｾ	ﾎ	ﾞ				
F					ｯ	ｿ	ﾏ	ﾟ				

Table 6-3. Train Modules For Use With PC-5

A. 400-LPM AND 750-LPM PRINTERS

CHARACTERS PER SET	16	48	48	48	48	64	64	64	64	96
CHARACTER SET GRAPHIC	EBCDIC	RPG	EBCDIC	FOR-TRAN	B 500 SIMUL.	EBCDIC	BCL	ASCII	EBCDIC W/OCR A NUMERICS	TEXT
	0	0	0	0	0	0 P	0 P	0 P	0 P	0 [
	1	1	1	1	1	1 Q	1 Q	1 Q	1 Q	1 <
	2	2	2	2	2	2 R	2 R	2 R	2 R	2 &
	3	3	3	3	3	3 S	3 S	3 S	3 S	3]
	4	4	4	4	4	4 T	4 T	4 T	4 T	4 ;
	5	5	5	5	5	5 U	5 U	5 U	5 U	5 /
	6	6	6	6	6	6 V	6 V	6 V	6 V	6 %
	7	7	7	7	7	7 W	7 W	7 W	7 W	7 >
	8	8	8	8	8	8 X	8 X	8 X	8 X	8 #
	9	9	9	9	9	9 Y	9 Y	9 Y	9 Y	9 =
	.	.	.	.	.	. Z	. Z	. Z	. Z	. \
	$	$	$	$	$	$ (	$ (	$ (	$ (	$ |
	*	*	*	*	*	*)	*)	*)	*)	* —
	-	-	-	-	-	- :	- :	- :	- :	- !
	,	,	,	,	,	, @	, @	, @	, @	, '
	?	?	?	?	?	? "	? "	? "	? "	? ¬
		@	+	+	+	+ [	+ [	+ [	[	+ .
		A	A	A	A	A <	A <	A <	A	A a
		B	B	B	B	B &	B &	B &	B &	B b
		C	C	C	C	C]	C]	C]	C]	C c
		D	D	D	D	D ;	D ;	D ;	D ;	D d
		E	E	E	E	E /	E /	E /	E /	E e
		F	F	F	F	F %	F %	F %	F %	F f
		G	G	G	G	G >	G >	G >	G	G g
		H	H	H	H	H #	H #	H #	H #	H h
		I	I	I	I	I =	I =	I =	I	I i
		J	J	J	J	J \	J \	J \	J \	J j
		K	K	K	K	K |	K ←	K }	K |	K k
		L	L	L	L	L —	L ≠	L —	L —	L l
		M	M	M	M	M !	M x	M !	M !	M m
		N	N	N	N	N '	N ⩾	N '	N '	N n
		O	O	O	O	O ¬	O ⩽	O ^	O ¬	O o
		P	P	P	P					P p
		Q	Q	Q	Q					Q q
		R	R	R	R					R r
		S	S	S	S					S s
		T	T	T	T					T t
		U	U	U	U					U u
		V	V	V	V					V v
		W	W	W	W					W w
		X	X	X	X					X x
		Y	Y	Y	Y					Y y
		Z	Z	Z	Z					Z z
		&	(	(	(					(¢
		/	)	)	)					) ¤
		%	:	/	/					: {
		#	@	=	@					@ }
		'	"	\	#					" ■

* Standard with B 700 and B 1710 Systems.

≠ Available on 9247-3/13 train printers only.

Table 6-3. Train Modules For Use With PC-5 (Cont)

B. 1100-LPM AND 1500-LPM PRINTERS

CHARACTERS PER SET	18	48	48	48	48	72	72	72	72	96
CHARACTER SET GRAPHIC	EBCDIC	RPG	EBCDIC	FOR-TRAN	B 500 SIMUL.	EBCDIC	BCL	ASCII	EBCDIC W/OCR A NUMERICS	TEXT
	0	0	0	0	0	0 A	0 A	0 A	0 A	0 <
	2	2	2	2	2	2 E	2 E	2 E	2 E	2 &
	3	3	3	3	3	3 F	3 F	3 F	3 F	3 %
	5	5	5	5	5	5 K	5 K	5 K	5 K	5 #
	6	6	6	6	6	6 L	6 L	6 L	6 L	6 =
	8	8	8	8	8	8 J	8 J	8 J	8 J	8 ¬
	9	9	9	9	9	9 S	9 S	9 S	9 S	9 ¤
	$	$	$	$	$	$ T	$ T	$ T	$ T	$ ■
	@	#	@	=	@	@ U	@ U	@ U	@ U	@ ¢
	4	4	4	4	4	4 W	4 W	4 W	4 W	4 /
	"	'	"	\	#	" X	" X	" X	" X	" a
	7	7	7	7	7	7 Z	7 Z	7 Z	7 Z	7 b
	1	1	1	1	1	1 <	1 <	1 <	1 ¦	1 [
	.	.	.	.	.	. &	. &	. &	. &	.]
	*	*	*	*	*	* %	* %	* %	* %	* >
	-	-	-	-	-	- #	- #	- #	- #	- \
	,	,	,	,	,	, =	, =	, =	, ¥	, |
	?	?	?	?	?	? ¬	? ⩽	? ⩒	? ¬	? !
		M	M	M	M	M ¤	M ¤	M ¤	M ¤	M '
		N	N	N	N	N ■	N ■	N ■	N ■	N {
		O	O	O	O	O ¢	O ¢	O ¢	O ¢	O ·
		P	P	P	P	P /	P /	P /	P /	P }
		Q	Q	Q	Q	Q a	Q a	Q a	Q a	Q _
		R	R	R	R	R b	R b	R b	R b	R ;
		B	B	B	B	B [	B [	B [	B [	B c
		C	C	C	C	C]	C]	C]	C]	C i
		D	D	D	D	D >	D >	D >	D ⌟	D d
		G	G	G	G	G \	G \	G \	G \	G j
		H	H	H	H	H |	H ←	H |	H |	H e
		I	I	I	I	I !	I x	I !	I !	I I
		V	V	V	V	V '	V ⩾	V '	V '	V m
		Y	Y	Y	Y	Y {	Y {	Y {	Y {	Y n
		/	)	)	)	) ·	) ·	) ·	) ·	) o
		%	:	/	/	: }	: }	: }	: }	: p
		&	(	(	(	(_	(_	(_	(_	(q
		@	+	+	+	+ ;	+ ;	+ ;	;	+ r
		A	A	A	A					A s
		E	E	E	E					E u
		F	F	F	F					F w
		K	K	K	K					K x
		L	L	L	L					L y
		J	J	J	J					J z
		S	S	S	S					S g
		T	T	T	T					T f
		U	U	U	U					U h
		W	W	W	W					W v
		X	X	X	X					X t
		Z	Z	Z	Z					Z k

Table 6-4. PC-5: EBCDIC to Link Number Correspondence

A. 400-LPM AND 750-LPM PRINTERS

LEFTMOST FOUR BITS

RIGHTMOST FOUR BITS

ROW \ COL	4	5	6	7	8	9	A	C	D	E	F
0	00	33	0E	3E				5E	5F	3B	01
1			36		42	4B	5D	12	1B		02
2					43	4C	54	13	1C	24	03
3					44	4D	55	14	1D	25	04
4					45	4E	56	15	1E	26	05
5					46	4F	57	16	1F	27	06
6					47	50	58	17	20	28	07
7					48	51	59	18	21	29	08
8					49	52	5A	19	22	2A	09
9				41	4A	53	5B	1A	23	2B	0A
A	31	34	5C	2E							
B	0B	0C	0F	39							
C	32	0D	37	2F							
D	2C	2D	30	3F							
E	11	35	38	3A							
F	3C	40	10	30							60

B. 1100-LPM AND 1500-LPM PRINTERS

LEFTMOST FOUR BITS

RIGHTMOST FOUR BITS

ROW \ COL	4	5	6	7	8	9	A	C	D	E	F
0	00		0F	41				43	45	3F	60
1			39		3A	4B	36	24	29		0C
2					3B	5F	54	18	27	2A	01
3					48	4D	5E	19	28	2B	02
4					4A	4E	55	1A	12	2C	09
5					4C	4F	5D	25	13	1E	03
6					5B	50	56	26	14	2D	04
7					5A	51	57	1B	15	2E	0B
8					5C	52	58	1C	16	1F	05
9				45	49	53	59	1D	17	2F	06
A	3C	3D	38	21							
B	0D	07	11	33							
C	30	0E	32	08							
D	22	20	46	42							
E	23	47	3E	34							
F	40	35		0A							37

Write

Data is written on the printer. Up to 132 columns of data can be accepted, column one first. The printer control will supply trailing blanks if a given printer so requires. If the P variant is set and the operation calls for single or double spacing after end-of-page (EOP) has been reported by the printer, a skip to Channel 1 will occur. EOP is not reported in the result descriptor in this case.

PC-4 single spaces with no exception reported if the operation calls for double spacing and the printer "Stop" button is pushed during the operation. Furthermore, if no 12-channel tape is installed, circuitry must be adjusted to render the End-of Page report impossible and to cause all skips to channels 2 through 12 to be converted to skips to channel 2 only. These adjustments are made by the Burroughs Field Engineer.

Space/Skip

The paper is moved as specified in the SSSS variant, but no printing takes place. Movement is as specified in the description of the Write operation.

Load Translator (PC-5 only)

The translator memory is loaded with data defining 257 characters. The link positions for all possible 8-bit codes are represented by 256 of these characters. The 257th character is an 8-bit binary value that indicates the number of characters in the train: 0 = 16 or 18; 1 = 48, 2 = 64 or 72, 3 = 96.

Test

The printer and the control bus are tested for the following conditions:

Not ready
End-of-page (not reported by PC-4 if R = 1).
Character set (PC-5 only).
Printer type (PC-5 only).
Control ID: PC-4, @10@; PC-5, @3E@.

If R=0, a result is returned immediately for PC-4. PC-5 turns the train motor on if necessary and, thus, obtains a valid train ID before returning a result. That train ID is retained by the control as long as the printer remains ready; the train motor may stop without affecting this storage.

If R=1, result reporting is delayed until the printer is ready and paper motion has ceased. PC-4 will turn off the train motor if it is on; PC-5, as before, will turn on the train motor if necessary to obtain a valid train ID.

Pause

A service request is returned after 8 milliseconds if bit 17 = 0.

Result Descriptor

Meanings of the bits in the Result Descriptor for PC-4 and PC-5 are defined below. Bits not included are reserved. Certain of the conditions reported are discussed in the paragraphs that follow.

Result Descriptor, Line Printer Controls

Bit	Meaning	Operations
0	Operation complete.	All
1	Exception; any or all of bits 2-6 set.	W, S, T
2	Not Ready.	W, S, T
3	Invalid train-position (link) number.	W
4	Invalid code (PC-5 only)	W
6	End of page.	W, S, T
7-13	Character set ID (PC-5 only): 0000000 - no automatic ID 0000001 - 18-character EBCDIC 0000100 - 48-character EBCDIC 0000101 - 72-character EBCDIC 0010000 - 96-character EBCDIC Others - see printer specifications	T
14-15	Printer type ID (PC-5 only): 00: 400/750 lpm 01: 1100/1500 lpm 10,11: reserved	T
16	Operation complete.	
17-23	Control ID: 0010000: PC-4 (@10@) 0111110: PC-5 (@3E@)	T

W=Write, S=Space, T=Test

A result is never stored for the Pause operation.

Exception Condition

One or more bits 2-6 are set. An interrupt is always returned. PC-5 sets this bit if an invalid operation code (000 or 011) is received.

Not Ready

If the printer goes Not Ready after the start of any operation except Test with R=1, the operation is immediately terminated and Not Ready is reported. On a Write operation, one buffer of data is accepted before the Result Descriptor is returned.

PC-5 reports a Not Ready and does not perform the operation even if the printer is ready if a Clear signal has been received or if the printer has changed from ready to not ready since the last non-Pause operation. This allows software to fire off a Test operation to check for a change in train ID.

Invalid Train Position Number

This condition is reported on a Write operation if a link number greater than the highest position actually on the train is obtained during data translation.

Invalid Code

This condition is reported if a link number greater than 128 (@80@) is obtained by PC-5 during Write data translation. The graphic printed is that represented by the link number minus 128 (@80@).

End of Page

The EOP signal does not terminate any operation. It is reported if this condition is true at the start of any Test, Write, or Space/Skip operation unless the operation specifies a channel skip or the P variant is set or a Test op with R=1 is received. PC-4 reports EOP in the Result Descriptor for a Space (P=0) or a Write-Space (P=0) operation, even though EOP is not initially true, if the EOP signal is received during paper motion of that operation and the Result Descriptor has yet to be processed by GISMO. In this case, EOP is also be reported on the next operation because the condition remains valid.

Character Set Identification (PC-5)

At present, only the 1100-lpm and 1500-lpm printers have automatic train recognition.

PC-5 Diagnostic Operations

The DD variant in the Read and Write operators provides diagnostic capabilities. Read-Diagnostic operations enable data to be read from the print line buffer while monitoring two signal lines (CSL, PSCL) from the printer. Write-Diagnostic operations allow certain portions of PC-5 logic to be bypassed in order to isolate problems. Further discussion is not included here because these specialized maintenance operations are normally found only in test routines used by Burroughs Field Engineers.

Load

DD=00

The normal Load operation, in addition to loading the translator memory, transfers that same data to print line buffer positions 0 through 255. The hammer-fired bit in each buffer location is set. Locations 192-194 and 0 are overwritten with the Reference Address and character set size, respectively.

DD=01

PC-5 transfers to the system the contents of the print line buffer; locations 0 through 255 during Status Count 15 and location 0 again during Status Count 17. A Terminate Data command may be received at any time. PC-5 accepts and loads data into the print line buffer regardless of the ready state of a printer; this allows the translator portion of the control to be checked out with no printer actually connected.

DD=10

The status of interface lines CSL and PCSL is monitored during Status Count 15 until a Terminate Data command is received.

Write

DD=00

A translation error resulting in an invalid link location prevents the hammer-fired bit for that location from being set on a normal Write operation.

MAGNETIC TAPE CASSETTE SUBSYSTEM

Introduction

B 1800 cassette tape handling capability includes (1) an integrated console cassette unit that reads information into the system from magnetic tape cassettes, (2) a cassette control that permits the console cassette unit to be used as a read/write peripheral device, (3) an optional cassette tape station, serviced by the same control, and (4) provision for a second control and one or two additional cassette tape stations. The integrated console cassette unit is used primarily for program and test routine loading. Regardless of the number of controls and drives, use of the integrated unit is retained for system (as contrasted with I/O) needs.

The cassette control is called "MTCC-1" or simply "the control" throughout this section.

Data transfer between control and unit is bit serial. The transfer rate is 8000 bits per second. (Recording density: 800 bpi; tape speed: 10 ips.) There is no hardware restriction upon maximum record length of the data, which is recorded in a binary mode.

Two 800-bit buffers alternately receive data during transfer operations. The control ensures that 85 milliseconds elapse between the end of one operation and the start of the next; furthermore a Buffer-Full or Terminate command must be received before tape motion commences on a Write operation. No Result Descriptor is returned until tape motion has ceased.

NOTE

The field termed "File Address" in the description of the I/O Subsystem is called the "C field" in this section. File Address is irrelevant to a tape device. The C field contains a pointer to the RS field of an entity called a "lock descriptor" for a given unit. The lock descriptor, details of which are presented later, enables one control to service more than one unit (unit). Each unit's individual descriptor chain is managed by the I/O Driver without confusion.

Operation Codes, Magnetic Tape Cassette Control

	← 0(MSB)				23(LSB) →	
READ	000D	0000	0000	0000	0000	00UU
SPACE-TO-EOF	1100	0000	0000	0000	0000	00UU
WRITE	010E	T000	0000	0000	0000	00UU
REWIND	0110	0000	0000	0000	0000	00UU
TEST	100V	VP00	0000	0000	0000	00UU
LOCK	1010	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000

The UU variant, used in the first five operators listed, provides the cassette drive unit number: UU=00, unit 1; UU=01, unit 2; UU=10, unit 3; UU=11, unit 4.

Definitions of Variants

Bit	Meaning
D	Tape motion direction.
0	Forward.
1	Backward.
E	Erase
0	Write. (Do not erase.)
1	Erase the amount of tape that would have been written if E were 0.
T	Tape mark
0	Do not write a tape mark.
1	Write a tape mark. (Ignore A and B addresses.)
VV	Result Descriptor storage timing
00	Store Result Descriptor immediately.
01	Store Result Descriptor if unit is ready and not rewinding.
10	Store Result Descriptor if unit is not ready.
11	Not valid.
P	Pause variant – for software use only

Read

In forward reading, data is stored beginning at the memory location specified by the A address (in the I/O descriptor) and ending at the location specified by the B address minus 1, or upon detection of an interrecord gap (IRG). Backward reading is from the B-minus-1 address to the A address, or until an IRG is detected.

Space-to-EOF

Tape is spaced forward past the first EOF record.

Write

Data is transferred to forward-moving cassette tape. If E, the Erase variant, is set, the amount of tape that would otherwise be written is erased. This is useful at the end of a valid file in order to create a software-detectable gap. (Note that there is no separate erase head on the cassette drive unit.)

Rewind

This op code causes the drive to rewind tape until clear leader is reached. Operation Complete is reported immediately. Tape is rewound from any position, even end-of-tape; neither EOT nor BOT is reported in the Result Descriptor.

Test

The unit is tested for conditions defined by those bits applicable to Test in table 6-18. The conditions are: Not Ready, EOT, Write Lockout, Rewinding, Unit Present, and Device ID. If data is to be stored, Result Descriptor bit 16 is set; otherwise, only bit 0 is set.

Lock

One lock descriptor is specified for each cassette unit serviced by a control. This descriptor is used solely for management, by the I/O Driver, of the multiple-unit situation; the Lock operator is never sent to the control. The procedures involved are described later in this section. (See I/O DESCRIPTOR INITIATION.)

Stop

The I/O Driver executes this operator (it is not sent to MTCC-1), stops linking through descriptors, and returns a Result Descriptor.

Pause

The I/O Driver generates and sends Pause to MTCC-1 after encountering any combination of four consecutive Test descriptors or descriptors that are not yet ready for execution. MTCC-1 returns a Service Request after 8 milliseconds, Result Descriptor bit 0 is set, and bit 16 is reset. Linking continues, following the 8-millisecond pause.

Result Descriptor

The Result Descriptor for MTCC-1 is defined below. Unless otherwise noted (in parentheses at the end of each paragraph), each bit/definition applies to all operators. Result Descriptor, Magnetic Tape Cassette Control

Bit	Meaning
0	Operation Complete
1	Exception condition; one or more of bits 2-15 are set.
2	Not Ready at start or during an operation. On a Write, one buffer of data is accepted before Not Ready is returned. A unit is considered Ready while rewinding is in process.
3	Data error. A Read or a read check (following a Write) that results in a CRC error detection turns on this bit. No error correction capability is provided in this subsystem. (Read, Write)
4	Memory access error. Data received on a Read before a buffer is free overwrites prior data. This bit is turned on after the operation. One or more buffers of data may be lost. On Write, if data is not received in sufficient time, the Write is terminated, a normal CRC pattern is written, the next buffer load is accepted, and then a Result Descriptor with a Memory Access Error exception is returned. (Read, Write)
5	Memory Parity Error. This bit is set by the I/O Driver when this error occurs. (Write)
6	End of Tape (EOT). EOT does not terminate any operation. It is reported for any action except Rewind at or after the EOT marker. All operations including Test will report the condition, which implies that approximately 12 inches (25 cm) of tape are still available for recording. (Read, Write, Space-to-EOF, Test)
7	Beginning of Tape (BOT). Detection of BOT will terminate the Read-Backward operation. It is reported on the Read during which it occurred and all subsequent Read-Backwards until a forward operation occurs. Read-Backward will not be performed if the tape is already at at BOT. Rewind operations are performed as usual on a tape at BOT, but BOT is not reported. (Read-Backward, Write, Test)
8	Write Lockout. This condition is reported on Write and Test operations whether the unit is ready or not. It is not reported on a rewinding unit. Any Write operation is immediately terminated.
9	End of File (EOF). Detection of a tapemark during a Read causes the EOF bit to be set. (Read, Space) For the Test operation only, this bit when set means that the unit is present.
10	Rewinding. For any operation except Test with VV=10, the operation is immediately terminated with this exception condition reported in the Result Descriptor. A rewinding tape is considered ready, (Read, Write, Rewind, Test)
11	Timeout. A preamble field precedes each record. A record is defined to be at least 16 data bits with no 4-bit dropout. Upon receiving the preamble, should no record be detected, a timeout exception is reported. A Write operation for which no data is received on the read check after roughly 32 milliseconds is terminated and a timeout is reported. Should a record be detected, an interrecord gap is defined to be the occurrence of no data for 0.5 milliseconds. (Read, Write, Space)
16	Second Operation Complete bit on all operations except Pause.
17 to 23	Device ID: @3A@ (Test).

I/O Descriptor Initiation

A description of the I/O Descriptor initiation algorithm for the cassette subsystem follows. The process is decidedly non-trivial and the reader is urged to study this section a number of times in order to best understand the subject.

Figures 6-4 and 6-5 illustrate the concepts discussed in the following paragraphs. Figure 6-4 depicts the chaining process. Figure 6-5 shows the linkages. Note, in figure 6-5, that the AEA field is unused, RS is used to lock or unlock, and LINK is a normal exit link to the next lock descriptor (possibly itself). Link field A (LINK-A) points to the first non-lock descriptor for the unit, while link field B (LINK-B) points to the current (non-lock) descriptor to be processed.

The I/O Driver is initiated with a start address pointing to the RS field of a descriptor. The Driver inspects the first two bits of the RS field looking for an unlocked (00) condition. If an unlocked condition is not found, the I/O Driver exits by fetching the link (L field) address which points to the RS field of another descriptor. The inspection is repeated. If an unlocked condition is found, an attempt is made to lock the descriptor by swapping 01 with the first two bits in the RS field. If the lock is not successful (00 not received back, the Driver exits as described before by fetching the link (L field) address. The inspection is repeated.

If the lock is successful, the Driver checks the OP field. If the OP is a non-lock OP, the descriptor is executed (initiated to the control). After execution, the I/O Driver fetches the link (L field) address and uses it as a new start address. If the OP is a Lock OP, GISMO is marked as being in a locked state. GISMO then fetches the link (B field) address, which points to the RS field of the current I/O descriptor, which might be (bit 0 = 0; bit 1 = 0) or might not be (bit 0 = 1) ready for execution.

If the descriptor is not ready for execution, the pointer to its RS field is saved and the Driver exits by fetching the link (C field) to the RS field of the lock descriptor. The Driver stores the saved RS pointer into the B field of the lock descriptor and then unlocks by setting the first two bits of the lock descriptor's RS field to 00 and setting itself to an unlocked state. The Driver then exits by fetching the link (L field) to the next I/O descriptor.

If the descriptor is ready for execution, it is executed. If there is no exception after the execution, the Driver fetches the link (L field) address looking for another descriptor to be executed. If the execution has an exception condition, an interrupt is returned, the pointer to the RS field having the exception is saved and the Driver exits by fetching the link (C field) to the RS field of the lock descriptor. The Driver then stores the saved RS pointer into the B field of the lock descriptor and then unlocks by setting the first two bits of the lock descriptor's RS field to 00. The Driver, now in an unlocked state, exits by fetching the link (L field) to the next I/O descriptor.

If a lock descriptor is encountered during the search for a descriptor to be executed (the Driver in a locked state), the Driver moves the RS pointer, which points to the first descriptor in the chain, from the A field to the B field of the lock descriptor. This move re-establishes the pointer to the current descriptor. The Driver then unlocks by setting the first two bits of the lock descriptor's RS field to 00 and setting itself to an unlocked state. The Driver then exits by fetching the link (L field) to the next I/O Descriptor.

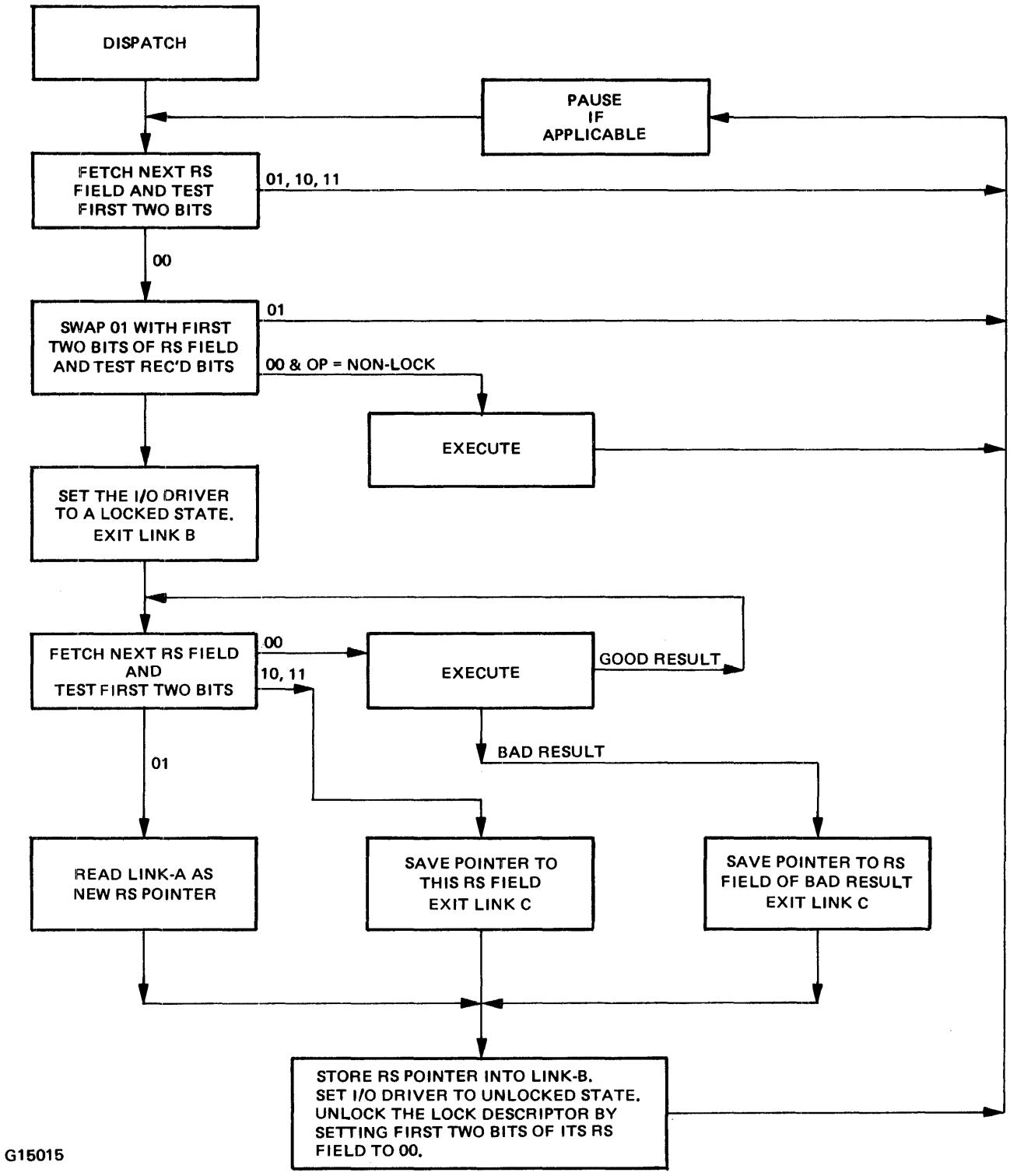
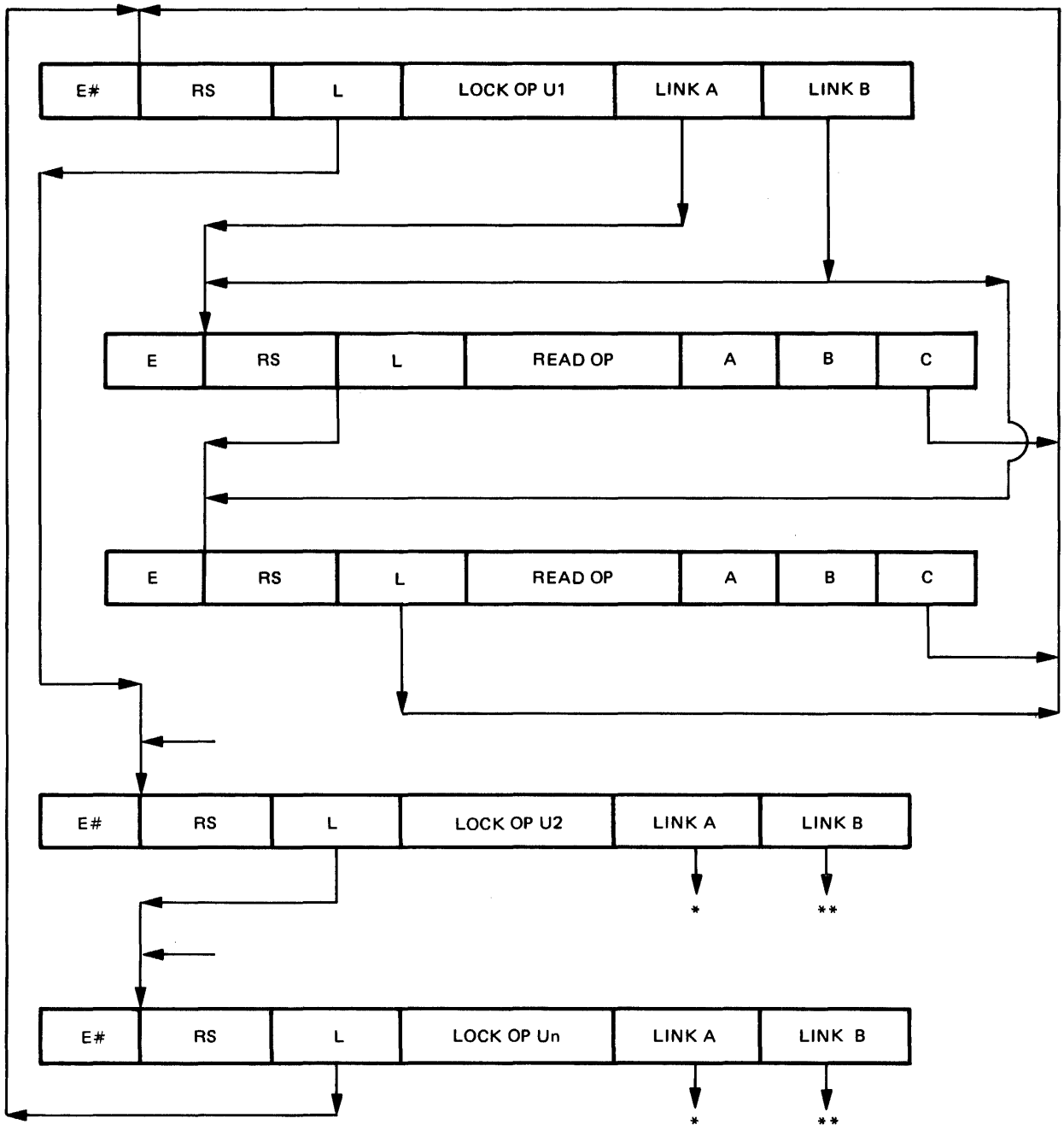


Figure 6-4. Chaining Process



* FIRST DESCRIPTOR IN CHAIN
** CURRENT DESCRIPTOR IN CHAIN. (NEXT TO BE EXECUTED.)
# UNUSED

G15016

Figure 6-5. I/O Descriptors Showing Linkages

Exceptions:

1. A Stop is not initiated to the control but causes the GISMO to simply exit from the chain and leave the control idle until the Driver is re-initiated with another start address for that control.

2. If the Driver receives a memory parity error signal during the fetch of an I/O descriptor (RS, OP, A, B, C, RS swap, or link fields), or during the fetch of the start address, it sends a special interrupt message to port #0, channel #15, consisting of an address pointing near the field in error, and then exits.

NOTE

Individual I/O Descriptors other than the lock descriptor are not permitted to be locked.

At the completion of an operation and after the actual ending data address is stored, the information in the RS field is exchanged with the result status bits from the operation. Note: This exchange must be accomplished without the possibility of another process interfering.

The information read from the result status field includes one interrupt request bit, one high interrupt bit, one 3-bit port number and one 4-bit channel number. (See figure 6-6.)

If the interrupt request bit is true, the I/O Driver generates an appropriate interrupt message to the port indicated. The interrupt returned is a high interrupt type if the high interrupt bit is true and a normal interrupt type if the high interrupt bit is false.

If the interrupt request bit is false, the Driver generates an interrupt message only if the result status bits returned include an exception (bit 2 set).

The interrupt message is a 24-bit address pointing between the result status bits and the link address. The channel # contained in the Result Descriptor's status area is also returned to the port indicated.

Any new initiate sent to a busy control represents a system malfunction. The Driver initiates with no provision to protect against, signal, or correct the malfunction.

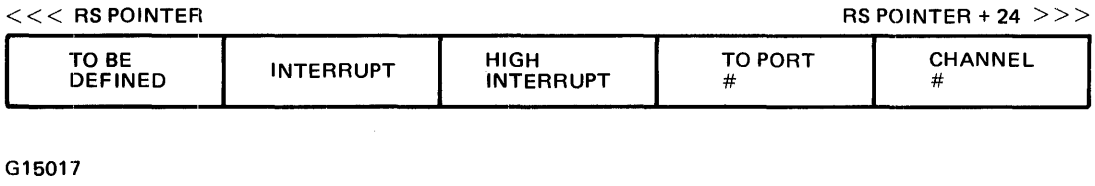


Figure 6-6. Result Status Field Definition

MAGNETIC TAPE SUBSYSTEMS

Introduction

Two distinct control types provide B 1800 system interfaces with Burroughs magnetic tape units. Magnetic Tape Control-3 (MTC-3) handles 800-bpi NRZ peripheral devices; Magnetic Tape Control-5 (MTC-5) handles 1600-bpi PE devices. No other densities are supported.

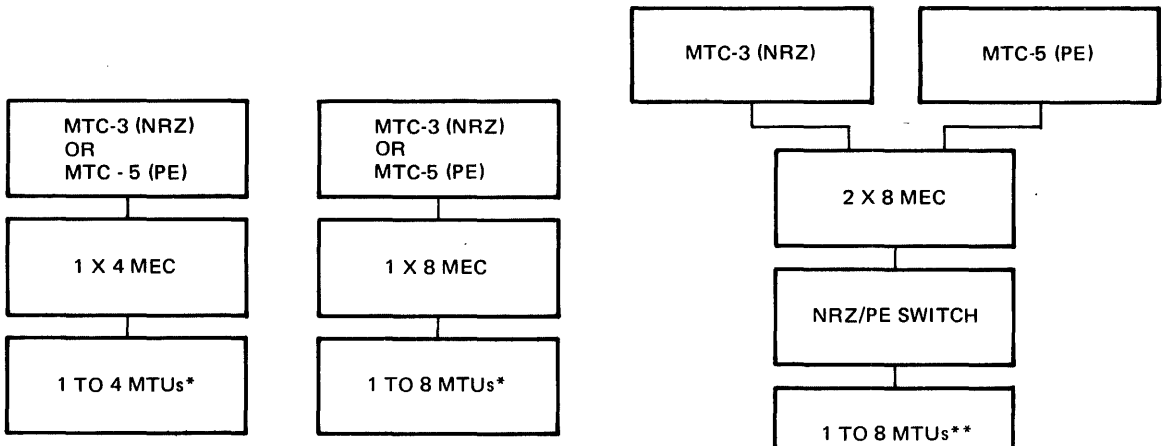
Figure 6-7 shows typical configurations. Note that all configurations require a Master Electronics Control (MEC), all configurations that include more than four drive units require a Master Electronics Exchange, and all PE/NRZ switchable configurations require an PE/NRZ switch option in the exchange.

The MEC (or the exchange) handles localized drive functions such as op-code decoding, buffering, parity checking and error correction, formatting, and deskewing. All tape drives connected to an MEC must operate at the same speed.

MTC-3 may be connected to any channel, 0-14; MTC-5 is limited to channels 8-14. In practice, magnetic tape controls are placed on lower channels than those assigned to data communications or reader-sorter controls, but higher than other controls, including disk controls. (Rationale: a retry is physically easier for disk, which needs to wait only one revolution, than for tape because the process of switching tape direction and initiating tape movement must occur twice.) If MTC-3 and MTC-5 are used on the same system, MTC-3 is usually placed one channel lower than MTC-5.

Descriptor linkage in the tape subsystem is more complex than in other I/O subsystems because of the presence of multiple units. Any unit can require attention at any time. Furthermore, the ordering of descriptors to be executed for each unit must not be violated. For a description of the algorithm by which software and hardware achieve the desired independence and control, see the preceding subsection (Magnetic Tape Cassette Subsystem).

The two controls and subsystems differ sufficiently to warrant separate descriptions, which follow.



*FOR MTC-3, 20 KB, 40 KB OR 60 KB UNITS;
FOR MTC-5, 40 KB, 80 KB OR 120 KB UNITS.

**ANY MIX TO EIGHT TOTAL: 20 KB NRZ AND 40 KB PE UNITS, OR
40 KB NRZ AND 80 KB PE UNITS, OR
80 KB NRZ AND 120 KB PE UNITS.

NOTE: TWO MTC-3's OR TWO MTC-5's WITH 1 TO 8 APPROPRIATE MTUs MAY BE USED IN THIS CONFIGURATION.

G15018

Figure 6-7. Magnetic Tape Subsystem Configuration

NRZ TAPE SUBSYSTEM (MTC-3)

Introduction

MTC-3 contains three buffers of 400 bytes each which are used in a cyclic manner to collect data during I/O operations. The control transfers data in 16-bit multiples. Odd-character final transfers are zero filled. This fact does not alter in Read-Backward or Space operations. Should consecutive operations be received before a timeout period within the passage of the interrecord gap (IRG) past the tape read head, tape motion will continue smoothly. Otherwise a non-interruptable deceleration of the tape is initiated; only when the tape has completely stopped can motion be restarted for the following operation.

During Read-Forward, Space-Forward, or Write operations, the IRG is signalled by the absence of data for twenty bits of time (2-1/2 characters). Consequently, a three-character or longer dropout can cause an incorrect halt.

IRG detection in reverse is somewhat more sophisticated to prevent tape position from becoming indeterminate. Initial IRG detection is based on a 2-1/2-character dropout as in the forward case, and a timer is initiated. If fewer than 8 read characters are detected before this timer times out, a dropout is assumed and IRG detection is re-enabled. Dropout error is reported; the character count is erroneous but correct positioning is maintained.

Operations

Operation Codes, Magnetic Tape Control 3

	← 0(MSB)				23(LSB) →	
READ	000D	CTTT	0S00	0000	0000	UUUU
SPACE	110D	N000	0S00	0000	0000	UUUU
WRITE	010E	M000	0R00	0000	0000	UUUU
REWIND	0110	0000	0000	0000	0000	UUUU
TEST	100W	WP00	0000	0000	0000	UUUU
LOCK	1010	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000

The variant UUUU, which appears in the first five operators in the table, specifies magnetic tape unit (drive) number:

UUUU = 0001 to 1000; units 1 to 8.
UUUU = 0000, 1001 to 1111; invalid.

Definitions of Variants

Bit	Meaning
D	Tape movement direction
0	Forward
1	Backward
C	Track correction; forward direction only
0	No correction.
1	The track specified by TTT is corrected.
TTT	Track to be corrected; 001 to 110 (1 to 8)
S	Noise burst rejection criterion flag
0	A noise burst of up to 15 characters will be rejected during a search for a valid record.

1	Noise burst rejection is limited to 6 characters or less.
N	Length of spacing
0	Tape is spaced past the next EOF; data is not transferred to the I/O Driver, data errors are not reported.
1	Tape is spaced 1 record; data is received by the Driver but is not stored.
E	Erase variant
0	Do not erase (write)
1	Erase (do not write)
M	Tape mark variant
0	Erasing (E=1); no tape mark is written.
1	Writing (E=0); A and B addresses are ignored, data is not transferred, tape mark is written.
R	Odd-even character count flag; software use only.
WW	Result Descriptor storage protocol
00	Store result immediately.
01	Store result when unit is Ready and not rewinding.
10	Store result when unit is Not Ready.
11	Invalid.
P	Pause variant; for software use only.

Read

On a Read-Forward (D=0), data is stored in ascending memory locations beginning with the location specified by the A address and ending with the location specified by the address preceding the B address (B address minus 1). On a Read-Backward (D=1), data is stored in descending locations beginning with the location specified by the B address minus 1 and continuing to the location specified by the A address. In addition to terminating on reaching the B address (forward) or the A address (backward), a Read is terminated on reaching an IRG.

Results are undefined if an invalid or non-present unit is specified by the UUUU variant.

Space

Tape is spaced in the direction and according to the parameters specified by the variants.

Write

Data from the location specified by the A address to the location specified by the B address minus 1 is written to tape, or, if E=1, the amount of tape that would normally be written is erased. During an erase, data is transferred from MTC-3 to allow character counting.

Rewind

Tape is rewound to BOT. Operation Complete is immediately reported without awaiting the actual completion of the physical tape movement. If tape is at the beginning of the reel when the operator is received, BOT is not reported, nor is EOT reported if tape is at the end. The tape unit remains ready during and after the rewind.

Test

The meanings of the bits in the result status (RS) field for the Test operator are given below. (Bits omitted in the table are unused and reserved.) The unit specified by UUUU is tested for the conditions specified by bits 2-4, 6-10 and 12-14. If the result is to be stored, the second Operation Complete bit (bit 16) in the Result Descriptor is set. Storage protocol is defined by the WW variant in the Test operator. If a Result is returned that is not to be stored immediately, the first two bits of the RS field must be reset to permit later interrogation. Test results from a busy unit are undefined. If the specified unit is not present, only bits 3, 4, 9 and 17-23 are returned.

Result Descriptor, MTC-3 Test Operator

Bit	Meaning
0	Operation complete.
1	Exception: one or more of bits 2, 6, 7, 8, or 10 set.
2	Not Ready.
3-4	Subsystem number (wired by Burroughs Field Engineer): 00 = no exchange, 01 = Subsystem #0, 10 = Subsystem #1, 11 = Subsystem #2.
6	EOT
7	BOT
8	Write lockout.
9	Unit present (wired by Burroughs Field Engineer).
10	Rewinding
12-14	Tape density: 101 (@9F@) = 800 bpi.
16	Operation Complete; if 0, result is not to be stored.
17-23	Control ID: 0110000 (@30@).

LOCK

A Lock operation is used for software control of the drive and is never sent to the control. There is one Lock descriptor per drive. The reader is directed to the section on the magnetic tape cassette subsystem for details.

Stop

The Stop operation is recognized and performed by GISMO and is never sent to the control. GISMO stops linking and returns a result. An interrupt is also returned if requested.

Pause

The Pause operator is sent to MTC-3 after a complete scan through the descriptor chain finds no operation ready to be performed. A service request is returned after a delay of 4 to 5 milliseconds. The result is returned with bit 0=1 and bit 16=0. This frees the processor for other duties. Pause is performed by the I/O Driver and does not appear in the descriptor chain.

Result Descriptor (Non-Test Operators)

Result Descriptor, MTC-3 Non-Test Operators

Bit	Meaning	Operations
0	Operation complete.	All
1	Exception: one or more of bits 2-12, 20 set.	All
2	Not ready. (The operation is not performed.)	All
3	Data error: vertical parity, longitudinal parity, CRC, or dropout.	R, W, S
4	Access error.	R, W, S
5	Memory parity error; software-generated.	W
6	EOT	RF, SF, W
7	BOT (The operation may be incomplete.)	RB, SB
8	Write lockout.	W
9	EOF (End of File) tape mark detected.	R, S
10	Rewinding.	R, W, S
11	Timeout: 3 feet of blank tape;	R, S
	no data from Read head	W
12	CRC correction possible.	RF, SF
13-15	Track in error. Significant only if bit 12=1.	All
16	Operation complete.	All
20	Late Initiation.	W

R=Read, W=Write, S=Space, F=Forward, B=Backward

Exception Condition

An exception condition causes an interrupt to be generated.

Not Ready

A Not Ready condition causes the operation to terminate immediately. on 90-ips and 120-ips drives, the Not Ready result is reported on any operation commenced during a period 200 to 600 milliseconds after the interrupt. Write lockout can sometimes be inadvertently reported as well.

Data Error

Data error (dropout) is defined as one or more missing characters. Data error does not terminate an operation.

Access Error

An access error is defined as a failure to receive a bufferload of data necessary to continue an in-process operation.

On Write or Erase, MTC-3 immediately completes valid formatting of the partial record, halts the tape, accepts the last bufferload of data and returns the result.

On Read or Space, the tape is stepped to the next IRG. Any exception conditions occurring on the entire record are reported, as well as access error. One bufferload of data is returned following the access error; any remaining data in the record is not returned. Character count is incorrect.

Memory Parity Error

Memory parity errors during I/O Descriptor fetch are not reported in the RS field.

End of Tape (EOT)

EOT terminates no operation but is reported for the operation in which it is sensed and all following operations (except Read-Backward) until reset by a Rewind. Rewind at BOT is not executed and, hence, does not reset EOT.

Beginning of Tape (BOT)

BOT terminates any backward operation. The tape is stopped and remains at BOT. This condition is reported for the operation that causes it and for all following operations until a forward operation is performed. A Rewind performed on a unit at BOT is returned as complete; BOT is not reported.

Write Lockout

Write Lockout causes any Write or Erase to be terminated without tape movement after one bufferload of data is received.

End of File Tape Mark Detected

No data is returned to the processor if a tape mark is detected during Read or Space. Tape marks written by MTC-3 are surrounded by extended (0.8-inch) IRGs on both sides, in contrast to the usual 0.5-inch IRG. MTC-3, however, can detect the occurrence of a tape mark even if not provided this extra, protective measure.

Rewinding

Rewinding is reported when any non-rewind operation is attempted on a tape that is rewinding.

Timeout

A timeout is reported when a Read or Space operation detects three feet of blank tape. Timeout cannot be detected on an Erase operation. During a Write, if data being read is not received in a reasonable time, the operation is terminated and Timeout is reported. Operator intervention may be required.

CRC Correction Possible

This condition is reported to enable software to perform CRC correction on a Read-Forward or Space-Forward operation. It is not reported if the parity track is the track in error. Software can reposition the tape and re-read with appropriate variants set to correct the erroneous track. Failure to correct is sensed and reported again. Correction should be attempted only after a number of unsuccessful retries. If the correction variants are set on a Read-Backward operation, the results will be undefined.

Late Initiation

Late Initiation is similar to Access Error. If the control is in an idle state and receives a Write (or Write-Erase) initiate, tape movement immediately begins. If the first bufferload of data is not ready, tape movement is stopped and Late Initiation is reported.

PE TAPE SUBSYSTEM (MTC-5)

Introduction

MTC-5 contains six 300-character data buffers. Data transfer between the MEC and MTC-5 is 16 bits parallel; data transfer between MTC-5 and the processor is 24 bits per transfer.

PE tape is considered a high-speed device; GISMO transfers as many as 100 three-character bursts, each with a Response Complete signal, for one Command Active signal. A provision exists for efficient transfer of a partial last buffer: a special Transfer-Out count command transfers a 9-bit value between 1 and 300 to indicate the number of characters in the last buffer. This counter is decremented during transfers and can be interrogated by a Transfer-In count command. Should the number of characters in the transfer not be modulo 3, the final transfer is right-zero-filled on a forward operation or left-zero-filled on a backward operation.

Operations

Operation Codes, Magnetic Tape Control 5

	← 0(MSB)			23(LSB) →		
READ	000D	0000	0000	0000	0000	UUUU
SPACE	110D	NB00	0000	0000	0000	UUUU
WRITE	11ET	0000	0000	0000	0000	UUUU
REWIND	011V	0000	0000	0000	0000	UUUU
TEST	100S	S000	0000	0000	0000	UUUU
LOCK	1010	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000

The variant UUUU, which appears in the first five operators in the table, specifies magnetic tape unit (drive) number:

UUUU = 0001 to 1111; units 1 to 15.
UUUU = 0000, unit 16.

Definitions of Variants

Bit	Meaning
D	Tape movement direction
0	Forward
1	Backward
N	Spacing
0	Tape is spaced past the next EOF; data is not transferred to the I/O Driver, data errors are not reported.
1	Tape is spaced 1 record; data is transferred to the Driver but is not stored.
B	If B=1 with D=1 and N=1, tape is backspaced two records; otherwise, B=1 is invalid.
E	Erase variant
0	Do not erase. (Write)
1	Erase. (Do not write)
T	Tape mark variant
0	Erasing (E=1); no tape mark is written.
1	Writing (E=0); A and B addresses are ignored, data is not transferred, tape mark is written.
V	Rewind and unload variant
0	Normal rewind.
1	Rewind and unload tape.
SS	Result Descriptor storage protocol
00	Store result unconditionally.
01	Store result only if unit is Not Ready or not present.
10	Store result only if unit is Ready and not rewinding.
11	Undefined.

Read

On a Read-Forward (D=0) data is stored in ascending memory locations beginning with the location specified by the A address and ending with the location specified by the address preceding the B address (B address minus 1). On a Read-Backward, data is stored in descending locations beginning with the location specified by B address minus 1 and continuing to the location specified by the A address.

Detection of an IRG terminates the operation. Detection of a tape mark instead of data causes that fact to be flagged in the Result Descriptor, but the tape mark is not stored into memory. Terminate Data Commands are ignored by MTC-5.

Space

The tape is appropriately spaced (D=0, forward; D=1, backward). No data is transferred to the I/O Driver. N=1 causes a space to EOF with no reporting of errors on non-EOF records. A single record space in either direction causes data error detection and reporting identical to that on Read operations. A Tape Mark is considered a record. Should D, N and B all be set, a backward space of two records is performed. Other variant combinations are undefined.

Write

Data from the location specified by the A address to the location specified by the B address minus 1 is written to tape. The MEC generates preamble, postamble, and vertical parity fields independently of MTC-5. A full width erase head is energized during the this operation.

The E variant causes a forward (only) erase of approximately the amount of tape that otherwise would be written. Data is transferred from memory to MTC-5; the character count function is used to determine the proper amount of tape to erase.

Rewind

The tape on the given unit is rewound to BOT. Operation Complete is immediately reported and the unit remains ready during and after the rewind. The V variant, if set, causes the unit to go Not Ready and the tape to be totally rewound and unloaded. Not Ready is reported in the Result Descriptor.

Test

The meanings of the bits in the result status (RS) field for the Test operator are defined below. The unit specified by UUUU is tested for the conditions specified by bits 2-14 and 17-23.

Bit 16 indicates to the I/O Driver whether or not the result is to be stored in the result status field of the Test operator's I/O Descriptor. If bit 16 = 0, the result is not stored; such an operator is considered to be a non-executable operation to the link mechanism. If bit 16 = 1, the operator is considered to be good and linking continues. A non-stored Test result necessitates the resetting of Result Descriptor bits 0 and 1 by the I/O Driver. Result Descriptor, MTC-5 Test Operator

Bit	Meaning
0	Operation complete.
1	Exception: set if one or more of bits 2, 5-8, and 10-14 = 1, or bit 9 = 0.
2	Unit Not Ready or not present or busy
3-4	Subsystem number (wired by Burroughs Field Engineer): 00 = no exchange, 01 = Subsystem #0, 10 = Subsystem #1, 11 = Subsystem #2.
5	Transmission error.
6	EOT
7	BOT
8	Write lockout.
9	Unit present (wired by Burroughs Field Engineer).
10	Rewinding
11	MEC or MTC timeout.
12-14	Tape density: 101 = 800 bpi (NRZ); 111 = 1600 bpi (PE).
16	Operation Complete; if 0, result is not to be stored.
17-23	Control ID: 0110100 (@34@).

Lock

This unique operation is never sent to the control but rather is used for software control of the individual tape drives connected to one control. The E field is unused, the RS field is used to lock or unlock a drive, the LINK field is the normal exit to the next lock descriptor, the A address points to the first non-lock descriptor for that unit, and the B address points to the current non-lock descriptor. The reader is directed to the discussion of the the locking algorithm in the subsection on the Magnetic Tape Cassette Subsystem for details.

Stop

This operation, recognized by the I/O driver only and never sent to MTC-5, causes linking to stop and a result to be returned. If so requested, an interrupt is also generated.

Pause

The Pause operator causes a service request to be returned after a 4 to 5 millisecond pause. Bit 16 in the Result Descriptor is reset. This operator is no longer used by B 1800 software.

Result Descriptor

Result Descriptor, MTC-5 Non-Test Operators

Bit	Meaning	Operations
0	Operation complete.	All
1	Exception Condition: one or more of bits 2-11, 21 or 22 set.	All
2	Unit Not Ready, not present, not compatible, or busy.	All
3	Data error. (Read, Write, Erase, Space)	R, W, E, S
4	Access error.	R, W, E
6	EOT	R, W, E, S
7	BOT	RW, EB, SB
8	Write lockout.	W, E
9	EOF (tape mark detected).	R, S
10	Rewinding.	R, W, E, S
11	Timeout (MEC or MTC).	All
16	Operation complete.	All
21	MEC-detected transmission error.	All
22	MTC-detected transmission error.	All

R=Read, W=Write, E=Erase, S=Space, RW=Rewind, B=Backward

Exception Condition

Regardless of request, an interrupt is generated if this bit is set

Not Ready

Not Ready is returned at the start of an operation if the unit is not ready. Should the condition occur during an operation, that operation is immediately terminated and the exception condition is reported. The same result is returned if the unit is busy or not present. The operation is terminated with no tape movement if a non-PE (non-compatible) unit is addressed, or if a transmission error occurs during the initiate phase.

Data Error

Non-correctable data errors are reported. These include: vertical parity errors, multi-track dropouts, excessive multi-track slew, a dropout on one track and excessive slew on another, and invalid preamble or postamble (more than 44 or less than 36 zeroes or no @FF@ character.)

During a Write, the read-after-write data is checked for any of the above causes. Additionally, even correctable skew errors or single-track dropouts are reported. Correctable errors are not reported on Read or Space operators; on Space-to EOF, errors on intermediate records are reported. Data detected by the Read-after-Erase is reported, but this apparent failure to erase does not terminate the Erase operation. (This is not the case on other operations.)

A transmission error detected by either MTC-5 or the MEC on a Test operation is reported and invalidates other status indicators.

End of Tape (EOT)

EOT terminates no operation. It is reported if, at the end of a given operation, the tape is positioned at or beyond the point at which EOT is detected.

Beginning of Tape (BOT)

BOT terminates any backward operation; the tape is immediately decelerated, stops, and remains at BOT. It is reported on the following operation and all subsequent operations until any forward operation repositions the tape forward past the BOT marker. All backward operations (except Rewind-and-Unload) to a tape at BOT are suppressed. Rewind-and-Unload is executed and a non-BOT result is returned.

This is defined as absence of a Write ring on the tape selected. It causes immediate termination of a Write or Erase operation with no tape movement and no data transfer. The condition is also reported on a Test operation.

Tape Mark Detected

If this occurs on a Read or Space operation, no data is transferred to the central processor. On a Test operator this bit indicates unit present and invalidates other RS bits.

Rewinding

This is returned if a non-Rewind operation is attempted on a ready but rewinding tape unit. Not Ready is also reported unless the tape is rewinding due to a Rewind or Rewind-and-Unload operation.

Timeout

Timeout is generated by the MEC should an operation not commence within approximately 2.5 seconds of initiation. MTC-5 times out if a command (other than Space-to-EOF) is directed to the MEC and a completion does not occur within approximately 4 seconds. Both possible causes are OR'ed into the Result Descriptor.

Tape Format

This represents the setting of the density switch on the specified drive, and is reported from the MEC to MTC-5. If the setting is 1600 bpi (PE), this is reported. If the setting is 800 bpi (NRZ), Unit Ready and Invalid Operation are reported by the MEC, MTC-5 assumes 800 bpi, and reports this.

Transmission Error

This represents a parity error in information transferred in either direction between the MEC and control. Should such an error occur during initiation when op codes are sent to the MEC, the MEC reports Transmission Error and Invalid Request to the control and goes idle. MTC-5 returns Not Ready and Transmission Error. If this error occurs on a data transfer, the operation is still completed; bits 1 and 21 are returned for a Write operation, 1 and 22 for a Read operation. If the error occurs during the transfer of the Result Descriptor from the MEC, bit 22 is set. The remaining exception bits may be incorrect. The error source is undeterminable for a Test operation, as bit 5 reflects the OR'ing of transmission errors detected by the MEC and MTC-5.

Diagnostic Commands

MTC-5 permits a number of additional commands, intended solely for diagnostic usage. They are presented here in the interest of completeness.

Channel Address (AAAA)

AAAA = 1XXX (X = don't care) specifies that the control is kept in the diagnostic mode, preventing interaction with the MEC until a microoperator with this bit reset is received.

AAAA = X1XX specifies a Diagnostic Read. Data receipt from the MEC is simulated by moving data from an internal register to a data bus within the control.

AAAA = XX1X causes the Ready line from the MEC to appear true.

AAAA = XXX1 forces even parity until reset by a microoperator with this bit reset.

Diagnostic Variant (VVVV)

Issuance of diagnostic operators various VVVV values permits the detailed simulation of the complex interaction between the MEC and MTC-5, allowing individual actions to be frozen and examined.

INDUSTRY COMPATIBLE MINI-DISK SUBSYSTEM

Introduction

The B 1800 mini-disk subsystem includes one or two industry-compatible mini-disk units, interfaced to the system by means of a single control. These units (often called "floppy" or "flexi-" disk units) include single-spindle, 243K-byte drives and dual-spindle, 486K-byte drives. Any combination of up to two units (1 to 4 spindles) may be attached to the control.

Format and Disk Layout

The control provides two 128-byte (sector size) buffers. The I/O Driver must ensure that data is written and read in 128-byte multiples, but reading may be terminated at any intermediate point by the I/O Driver. The control uses the industry-compatible format detailed in figure 6-8. Disk characteristics are listed in table 6-5.

Table 6-5. Mini-Disk Characteristics

Recording surfaces	1
Tracks (1 index, 73 data, 2 spare, 1 FE)	77
Sectors per track	26
Characters per sector	128
Bits per character	8
Bit transfer rate (bps)	250K
Total formatting capacity	242,944 bytes
Recording technique	FM*

* Double frequency; bits of the clock pattern (usually FF), appear between data bits.

Track 00, the outermost track, is defined to hold a track index to files on the disk. This index track furthermore contains information such as a list of bad tracks.

The Polynomial Check Code shown in figure 6-8 is defined to be the 16-bit truncation of the polynomial $X^{16} + X^{12} + X^5 + 1$.

where X is the preceding 5 bytes. This hexadecimal field is initially set to @FFFF@. Consequently, this field allows a hashing check of the sync byte and actual track and sector address fields.

It should be noted that certain clock fields differ from the normal "FF", providing a means of ascertaining the point at which address and data fields occur. The sync byte can be used to denote a special record by varying the normal @FB@/@C7@ to @F8@/@C7@. Where "FF" or "00" is specified, either is usable; "FF" is provided by this control. A bad track is coded with "FFFFFFFF" (8 "F"s) in the track/sector address field and contains no data sync bytes.

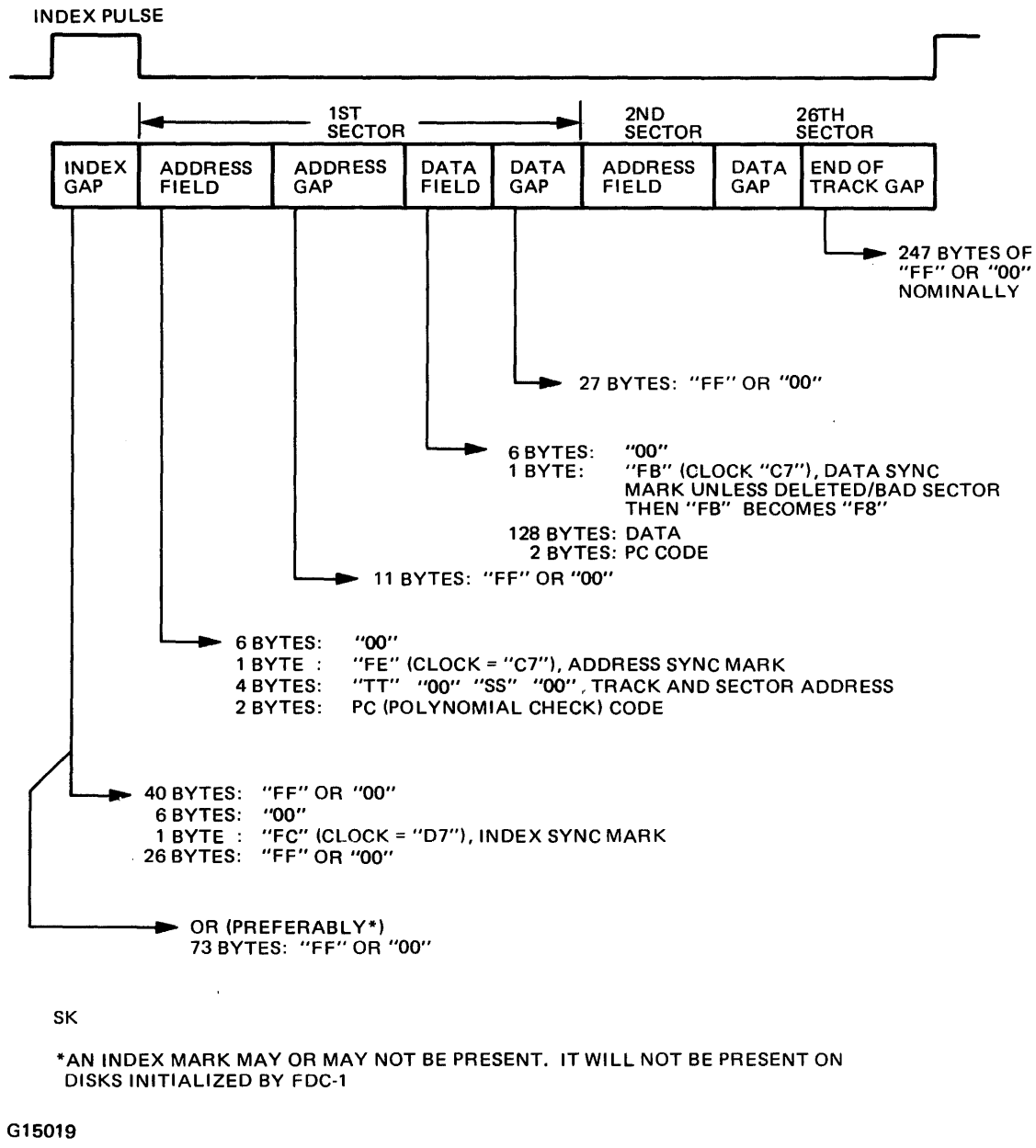


Figure 6-8. Mini-Disk Recording Format

Operations

Operation Codes, Mini-Disk Control

	← 0(MSB)			23(LSB) →		
READ DATA	000A	0000	0000	0000	0000	00UU
WRITE DATA	010D	0000	0000	0000	0000	00UU
TEST	100R	N000	0000	0000	0000	00UU
RESTORE	1010	0000	0000	0000	0000	00UU
INITIALIZE	011V	0000	0000	0000	0000	00UU
READ ABSOLUTE	1100	0000	0000	0000	0000	00UU

Definitions of Variants

Bit	Meaning
A	Sector transfer selection
0	All sectors without deleted-data sync marks are transferred.
1	All sectors are transferred.
D	Sector write selection
0	All sectors are written.
1	Specified sectors are written, preceded by deleted-data sync marks.
RN	Ready/Not Ready result status return protocol
00	Return result unconditionally.
01	Return result if the unit is Not Ready.
10	Return result if the unit is Ready.
11	Not valid.
2	Unit
V	Read/write head movement
0	The read/write head is not moved.
1	The read/write head is stepped 1 track.
UU	Spindle selection
00	Spindle 0.
01	Spindle 1.
10	Spindle 2.
11	Spindle 3.

Read Data

Data is read from consecutive sectors starting from that sector specified in the File Address portion of the I/O descriptor (or next higher available, should that sector be deleted) until either terminated by the I/O Driver or until sector 26 is transferred (or reached, should it be marked as deleted). Any sectors marked as deleted will not be transferred, unless the A Variant flag, signifying a read of all sectors, is set.

Write Data

Data is written in 128-character quanta to consecutive sectors starting with that sector specified by the File Address field. Writing continues until the I/O Driver terminates data transfer or until sector 26 is written. Should the D variant be set, all sectors written are preceded with a special @F8@/ @C7@ data sync byte, defined as the indication of a bad sector.

Test

The control and the unit specified are tested and three items of information are returned in the RS field:

1. Unit Ready or Not Ready.
2. Unit present or not present.
3. Control ID (@08@).

The manner in which Test completes can be varied with the R (Ready) and N (Not Ready) variants. If bit 16 of the Result Status field is set, the Result Descriptor will be returned; otherwise, the I/O Driver will retry later.

Restore

The read/write head is stepped to track 0.

Initialize

Address fields (6 zero bytes, 1 sync byte, 4 address bytes, and 2 polynomial check bytes) are written on the selected drive and track. All gaps and data fields are written with @FF@. The N variant, if set, advances the read/write head to the next track before initialization is done. Twenty-six 4-byte addresses in the sector order desired must be provided, followed by 24 bytes of filler data to satisfy the 128-unit Write requirement. Each 4-byte address must be in the format TZSZ where T and S represent 8-bit binary track and sector values and Z is @00@.

Note that the Initialize operation does not initialize data fields but, rather, puts basic information on the disk such that normal writes are possible. Thus a normal write operation is necessary to provide data sync bytes, data, and check codes before the disk can be read.

Byte 2 of the File Address in the I/O Descriptor must contain a value indicating the physical track. This control uses this value to manage the unit itself.

Read Absolute

Given a specific drive and track, as much as 256 characters of information is read, unformatted, starting N milliseconds after the index byte is detected. N is defined to be 2.5 times the binary value of the low-order 8 bits of the File Address Field. Data is transferred until all 256 bytes are moved, or until requested to cease. When executing this operation, the control first initiates a Restore and then moves to the track specified in byte 2 of the File Address field.

Result Descriptor

Upon completion of an I/O operation, the control returns a 24-bit result status field indicating the success of that operation. Bit 16=1 indicates that the field is valid. The Result Descriptor for this control is defined below. Specific meanings of certain of these bits are clarified in the subsections that follow.

Result Descriptor, Mini-Disk Control

Bit	Meaning	R	W	T	RST	INIT	RABS
0	Operation complete	X	X	X	X	X	X
1	Exception	X	X	X	X	X	X
2	Unit not ready	X	X	X	X	X	X
3	Data PC error	X					
7	Unit present	X	X	X	X	X	X
8	Write fault		X			X	
9	Track seek error	X	X				
10	Sector search error	X	X				
11	Time out	X	X	X	X	X	X
12	Address PC error	X	X				
13	Special sector	X					
15	End of cylinder	X	X				
16	Store result	X	X	X	X	X	X
17-23	Control ID 000 1000 @08@	X	X	X	X	X	X

R=Read, W=Write, T=Test, RST=Restore, INIT=Initialize, RABS=Read Absolute.

Exception Condition

One or more of bits 2, 3, 8, 9, 10, 11, 12, 13, or 15 are set, or bit 7 is not set.

Not Ready

One or more of the following conditions will cause the unit to go Not Ready: power off or not fully up, unit not present, disk rotational velocity not within limits, other hardware malfunctions. The Not Ready condition will terminate any operation in which it occurs, aside from Test.

Data PC (Polynomial Check) Error

This error does not abnormally terminate the operation.

Write Fault

Write Enable with no head load or Write Enable without write data.

Track Seek Error

Valid address not found on the track within two disk revolutions. Addresses with PC error are considered invalid and do not determine track identity. Should the first track searched be unidentifiable, the search is terminated. A successful search enables computation of the number of tracks that the head must be moved to reach the desired track and this head movement is initiated. The new location is searched for correct track ID. A failure causes a head step of one track in the same direction; if the failure persists, the head step is repeated one more time. This elaborate procedure is due to the unit's relocation algorithm; up to two relocated tracks, with track addresses of @FF@, are permitted.

Sector Search Error

The given sector (1 to 26) cannot be found within two disk revolutions. Addresses with PC errors are considered invalid and do not cause a true comparison. Note that physically consecutive sectors need not have consecutive addresses.

Timeout

A time out occurs (1) if the unit fails to transmit data or clock pulses within two disk revolutions while reading a track address or data, or (2) track 0 cannot be found within 77 head steps during a Restore operation or a Read Absolute operation (with its implied Restore), or (3) an invalid operation code (first four bits are 0001, 0110, or 0111) is received, or (4) a Test operation with RN=11 is received.

Special Sector

A Read Data operation encountered a deleted sector.

End of Cylinder

A request is made for a cylinder with an address that exceeds the track limit of 26. In this case, data is discarded on a Write.

Control ID

The identification for the B 1800 mini-disk control is 0001000 (@08@).

DISK CARTRIDGE SUBSYSTEM

Introduction

Disk Cartridge Control-3 (DCC-3) enables the system to interface with one or two Burroughs disk cartridge drives, each of which can have one or two spindles. Three different cartridge drives are available:

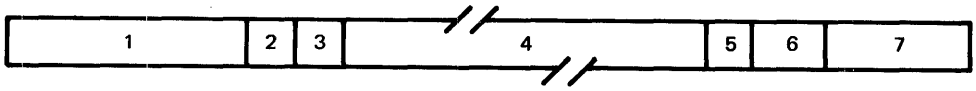
B 9480 2200 bpi, 203 tracks, 32 sectors per track
B 9481 2200 bpi, 406 tracks, 32 sectors per track
B 9482 4400 bpi, 203 or 406 tracks, 64 sectors per track

If two drives are connected, a 1 x 4 adapter is mandatory. B 9480 and B 9481 drives may be paired on the same control, but neither may be paired with a B 9482 drive.

Although DCC-3 can be connected to any channel (0-14), channel 5 is recommended and almost universally used to achieve compatibility with other B 1800 and B 1700 installations, because channel number is one subfield in disk addresses used by software.

Burroughs standard cartridge format, required, is outlined in figure 6-9.

The Address field differs among the three drives, as shown in figure 6-10. The outermost cylinder, upper disk surface, and first complete sector after the index pulse are all assigned the value zero.



[READ DOWN]

1	– PREAMBLE	– 33 BYTES OF ZEROES
2	– SYNC	– 1 BYTE (@1E@)
3	– ADDRESS	– 2 BYTES
4	– DATA	– 180 BYTES
5	– LPC	– 1 BYTE
6	– ECC	– 4 BYTES
7	– POSTAMBLE	– 25 BYTES OF ZEROES (NORMALLY)

G15020

Figure 6-9. Burroughs Cartridge Disk Format

	+---16 BITS---+	C=CYLINDER		T=TRACK	S=SECTOR	
B 9480	00CCCCCCCCTSSSSS	8 BITS	(0-202)	1 BIT	5 BITS	(0-31)
B 9481	0CCCCCCCCCTSSSSS	9 BITS	(0-405)	1 BIT	5 BITS	(0-31)
B 9482	0CCCCCCCCTSSSSSS	8 BITS	(0-202)	1 BIT	6 BITS	(0-63)

G15021

Figure 6-10. Address Field Format, B 9480, B 9481, B 9482

LPC represents a Longitudinal Parity Check byte generated with an exclusive OR-ing algorithm upon the 180 data bytes. For the B 9482 cartridge drive, LPC additionally encompasses the address bytes.

ECC represents the Error Correction Code bytes which allow detection and correction of various data errors occurring within the 180 data bytes. ECC is a form of Hamming code which appears only on the B 9482 cartridges.

The Postamble field ranges from 6 to 30 bytes, being affected by physical phenomena such as drive speed perturbations, differences in the write clock, and sector pulse spacing variation.

Disk Cartridge Subsystem Operational Details

Two forms of synchronization, bit and data, are involved in reading the cartridge. Bit synchronization is necessary for each sector read, as the sector-to-sector data transition is not continuous. Following detection of a sector pulse, reading is disabled briefly and re-enabled, allowing the drive electronics to resync on a pattern that must be all zeros. Consequently bit synchronization is obtained at some point within the preamble, and a search is made for the sync byte. The sync search is started 60 to 64 microseconds after the sector pulse is detected on the 32 sector/track units, and 28 to 33 microseconds after detection on the B 9482 unit.

Should a 1 that is not part of a valid sync pattern be detected during the sync search, either a 1 has been picked up in the preamble or the sync byte has been missed or is invalid. DCC-3 abandons its sync search until the next sector in this case.

Before a normal Read or Write can be performed, DCC-3 must ascertain the position of the read/write head by address search. Upon achieving synchronization, the address read from disk is compared with the desired address. For Read operations, this is the sector to be read; for Write operations it is the address of that sector on the same physical surface that precedes the sector to be written. Two address compares are required before the actual I/O operation is performed, in order to lessen the the probability of address search error. With the first comparison, DCC-3 verifies that the drive has been positioned to the correct cylinder. Only a cylinder and track comparison is needed. A second address compare must be performed before the operation is performed. This dual comparison is also necessary for the first sector operation following an internal seek. The B 9482 drive verifies the address comparison by checking the length of the address field and the correctness of the LPC field and postamble. It furthermore requires a correct ECC and LPC in the sector physically preceding that to be written on a Write operation.

DCC-3 must check cylinder positioning for a normal Read or Write operation. Should the position be correct, the operation may be undertaken. Otherwise a seek is necessary. Note that seeks are all implicit in the B 1800 I/O subsystem.

Four Seek Status flip-flops in the control, one per possible drive, indicate, if set, that a drive is seeking. This avoids a possible ping-pong effect of multiple descriptors repetitively causing seeks with no operation ever actually being completed. Should the appropriate Seek Status flip-flop be set, the control exits by returning a Result Descriptor with bit 16 reset. Otherwise, the flip-flop is set, a command is issued to move the head, and a result, also with bit 17 reset, is returned. The operation remains in a queue. This frees the control to handle operations on other cartridge drives during the head movement period. No seek will be performed until this flip-flop is reset, generally by a Read or Write on the sought cylinder, although the system CLEAR button or a Test-and-Clear command will also reset it. The Read or Write that clears the flip-flop need not be the precise one that set it, but must start on the sought cylinder. Two operations, Write Index and Read Absolute, clear the seek status flip-flop and are not inhibited thereby.

Software must be informed when a seek has completed; a Service Request will be raised when three conditions are true:

Status Count = 1,
Seek Status flip-flop set on a drive,
Seek Complete sensed on same drive.

Service Request is maintained until the control advances beyond status count 1. No indication of which drive completed a seek is provided; when the I/O Driver, in the course of its normal operation, executes a descriptor which has the File Address field in the sought cylinder on the drive for which the seek status flip-flop is set, the flip-flop will be cleared. Until that time, all other descriptors to that drive will return the aforementioned result with bit 16 = 0.

One condition can cause a disk cartridge drive to hang unless the situation is cleared by software. This problem occurs when the Seek Status flip-flop is set and the descriptor chain contains no operation for the cylinder at which the heads are currently positioned. This phenomenon is usually caused by an undetected seek error or an implicit seek. Any operation for the drive is returned with bit 16 reset, specifying that the operation, including the one causing the implicit seek, is to be performed later. This is because the Seek Status flip-flop is normally reset only upon a successful Read or Write operation to the cylinder to which the heads are positioned after an implicit seek. The condition is hence indefinite.

Recovery must be provided by software. The Seek Status flip-flop can be reset by initiation of a Read Absolute or Test-and-Clear operation. Note that this is not in fact performed by GISMO or the standard B 1800 MCP.

In transferring data on a normal Read or Write operation, DCC-3 continues the operation across sectors, tracks, and cylinders as appropriate until ordered to stop by a Terminate Data command. The I/O Driver remains dedicated to the particular operation in progress even through implicit seeks that occur if the operation happens tn span cylinders.

Initialization is a procedure (not an operation) with the purpose of writing all sector addresses on a disk, testing the disk to identify and delete faulty tracks, and writing the label. The process is begun with a Write Index operation on a particular track, followed by a normal Write operation of 31 (or 63) sectors starting at sector 1. Data, albeit meaningless, must be provided for each sector. Upon thus writing correct sync patterns and addresses on all sectors, test data is normally written and read from every sector to verify correct functioning. Detection of a faulty sector causes software to delete the entire track from its available disk table. Such faulty sectors should be addressed solely by initialization routines. Due to the presence of the label and other critical information thereupon, detection of a faulty sector on either track of cylinder 0 causes the disk to be considered unusable by the B 1800 system.

Operations

Operation Codes, Disk Cartridge Control

	← 0(MSB)				23(LSB) →	
READ	000A	0000	0000	0000	0000	00UU
WRITE	010I	0000	0000	0000	0000	00UU
TEST	100W	WW00	0000	0000	0000	00UU
PAUSE	1110	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

UU = unit number; other variants are described under the appropriate operation.

Read

Reading starts at the sector indicated by the File Address fields. Data is transferred to memory starting at the location specified by the A address and continuing to the location specified by the B address minus 1. The entirety of all sectors, including incomplete ones, is checked for parity.

If the head is not positioned correctly, an implicit Seek will be initiated if the unit is not already seeking, as previously described. A correct cylinder causes the control to continuously check sectors for correct cylinder, track, and sector addresses. Upon detecting the correct sector, data is fed into the first data buffer. DCC-3 signals the system to empty that buffer when it is filled, and concurrently starts its search for the next higher sector. The fact that this is physically the next sector is irrelevant to the hardware.

Reading continues until terminated by a Terminate Data command from the I/O Driver. During the transfer of the highest-numbered sector on a cartridge, Terminate Data must be sent before DCC-3 reaches Status Count 10, or another Service Request and a report of Illegal Address will be sent.

A sector ready to be read but with no buffer to receive its data merely causes a wait until a buffer is free and the sector is again in position. Reading of a sector is terminated when all data and the LPC have been read. DCC-3 checks neither the ECC bytes nor whether the postamble is all zeros.

Setting the A variant causes a Read Absolute operation in which everything read is sent, including the part of the preamble read after bit synchronization has been achieved, address, data, LPC, ECC, and postamble as physically present on a given cartridge type. No addresses, including the sector actually being read, are checked by DCC-3. Consequently, a Seek is mandatory. After a Seek completes, the control detects the index pulse and counts sector pulses to locate the desired sector. Two complete buffers of information, the second zero filled, are sent to the system. Reading terminates after a sector pulse is detected. Note particularly that there is no indication of the point at which postamble stops and zero-fill begins; this point varies widely from sector to sector. A Terminate Data command must be sent to complete the operation and cause the result to be returned.

Write

Data is written into sectors starting with the sector specified by the File Address Field, from the the memory location specified by the A address to the location specified by the B address minus 1.

Upon receipt of a Write Operation, DCC-3 verifies correct head positioning. Incorrect head position causes operation termination, as previously described, with one buffer load of data (which must be discarded) received. Valid head position causes the control to read sector address fields searching for that sector physically preceding the one to be written. Upon detection thereof, the control stops reading and prepares to write after receiving the next sector pulse. As previously mentioned, ECC and LPC codes must be correct on this preceding sector.

DCC-3 generates the preamble, sync, address, LPC, and postamble fields for every sector written. The B 9482 drive ignores the last of these fields and generates the ECC and end gap fields itself.

Data is stored in four-sector (180-byte) buffers. Any number of bytes are transferrable; termination is by a Terminate Data command. Each buffer load of data is written to a consecutively higher sector. Should the last sector be incomplete, it is zero-filled by DCC-3. Actual writing commences immediately after the first buffer is filled. Conversely, when no Terminate Data command has been received and any buffer is empty, the control requests additional write data. Should all four buffers be empty when a sector is to be written, DCC-3 will wait indefinitely until data is present and the appropriate sector is in position.

No position checking is done when advancing from track to track on the same cylinder. After crossing cylinders, the control must re-establish position by reading and searching for the sector physically preceding track 0, sector 0. This generally causes a one disk revolution interruption.

A Write operation whose File Address and length are sufficient to cause advancement past the highest sector on a given disk causes the operation to be terminated and a result returned indicating an Illegal Address exception condition.

Setting the I variant causes a Write Index operation in which sector 0 of a particular cylinder and track is written, ignoring any data already present. The rest of the track is zero filled in order that a normal Write operation can initialize that track. DCC-3 first causes a seek to the desired cylinder (even if already there). Writing commences following the first sector pulse after the index pulse, thus writing sector zero. All data as appropriate for the particular cartridge type must be provided by the system, including the preamble, sync, address, data, LPC, and postamble. This requires two of the control's buffers. The B 9482 unit generates the ECC and postamble fields, the latter overriding that sent by the control.

If sufficient data to write the complete sector is not provided, DCC-3 zero-fills that sector. On the 32 sector-track units, neither data, LPC, nor postamble need be provided, as the primary function of the Write Index is to write the address; addresses are valid regardless of data or LPC. Consequently the system can send a minimum of preamble, Sync, and address, followed by a Terminate Data command. The B 9482 requires a correct LPC to write a subsequent sector, as previously discussed. Consequently, at least some data (to ensure a zero LPC) or all data and the LPC must be written.

Actual writing begins after the first buffer load of data has been received, whether or not a second buffer load or a Terminate Data command has been received. There is a finite but low probability of an access error, defined to be failure to fill the second DCC-3 buffer before the first buffer has been emptied; this phenomenon causes a sector of zeros to be written.

Test

The control and drives are tested for the following conditions:

Ready
Write Lockout
Peripheral Seek Timeout (B 9480/B 9481 only)
Seek Status flip-flop set
Drive not seeking
Controi ID (@1A@)
Drive presence and types

Peripheral Seek Timeout is defined to be failure to reach a sought cylinder within 200 milliseconds. It is reported until DCC-3 initiates another seek. The variants allow, among other possibilities, the software to be notified when the Ready status of a given drive changes. By alerting software when a disk cartridge is replaced, a new cartridge can have its label read and other appropriate measures performed.

The WWW (wait) variants are defined as follows:

WWW	Wait Variants
000	Store result unconditionally
001	Return Service Request after a 4 millisecond pause, with bit 16 reset to indicate that the result is not to be stored.
010	Store result only if the unit is present and not ready.
100	Store result only if the unit is ready.
101 to 111	Undefined

Pause

A result with bit 16 = 0 is returned after 4 milliseconds. This operation is generated by the I/O Driver and does not appear in the descriptor chain.

Stop

The I/O Driver stops linking and returns a result. The STOP operation is never sent to the control.

Result Descriptor

The meanings of the bits in the Result Descriptor for DCC-3 are defined below. Each bit applies to all operators unless otherwise noted. Bits not included are reserved. Certain of the conditions are discussed in the paragraphs that follow.

Result Descriptor, Disk Cartridge Control

Bit	Meaning	Operations
0	Operation complete.	All
1	Exception condition. (One or more of bits 2-6, 11, 14 set or bit 9 not set.)	All
2	Not Ready.	All
3	Parity error on Read	R
4	Parity error detected by B 9482.	R, RA, W
5	Memory parity error on Write. Generated by software.	W
6	Write lockout.	W, WI, T
7-8	Unit ID, wired by Burroughs Field Engineer. 00 = 32 sectors, 203 cylinders 01 = 32 sectors, 406 cylinders 10 = 64 sectors, 203 cylinders 11 = 64 sectors, 406 cylinders	T
9	Unit presence. (Not reported on Pause.)	All
10-11	Sector Address Error. If both bits are set, illegal address has been detected on Read or Write; or Seek Incomplete has occurred on any operation except Pause, B 9480/81 only; or Address Coincidence has not been achieved (R, W)	R, W
12	Not seeking.	T
14	Seek Status flip-flop set.	T
16	Operation complete and result to be stored.	All
17-23	Control ID (@1A@).	T

R=Read, W=Write, T=Test. RA=Read Absolute, WI=Write Index

Not Ready

Not Ready conditions include the following:

Power off or not fully up.
Cartridge not mounted on drive.
Disk rotational speed not within limits.
Unit physically not present.

One buffer load of data is transferred on a Write operation before the Not Ready result is returned. Any operation except for Pause or Test is terminated and any Read or Write operation must be considered to have failed.

Parity Error

Parity errors are detected by the control on all units and, additionally, by the drive on the B 9482 unit. The LPC is checked for an error during normal Read operation for every sector read; in the multiple-sector-Read case, there is no indication of which sectors are in error. The LPC is not checked during a Read Absolute operation. Parity errors do not terminate any operation.

The B 9482 drive checks the LPC and ECC on all Read operations including the address search preceding an operation, and checks the LPC on all Write operations. Errors are reported to DCC-3, which reports the error only if data is actually read from the erroneous sector. For a Write operation the control reports Parity only if detected on the sector to be written or its physical predecessor. The control terminates the operation without actually writing the sector in question, but accepts all data in the normal manner before returning the exception result. Memory parity errors are detected by GISMO after a Write or Write Index operation. The operation is not terminated abnormally. No indication of which sectors were in error is furnished on multiple-sector Writes.

Write Lockout

Write Lockout is returned upon receiving any Write operation on a disk put in the Write Lockout state by the operator; any Write causes one bufferload of data to be accepted and discarded. Note that most system operations require certain status information to be stored on the disk itself due to the removable nature of the disk cartridge medium. Consequently it is generally not possible to use a disk set to write lockout status for normal operations. The feature is intended for such specialized media as alignment cartridges and test cartridges.

Unit Not Present

Unit Not Present is returned when a an operation is directed to a non-attached unit on a control with fewer than the maximum four units attached. Not present is a condition wired by a Burroughs Field Engineer and need not reflect the actual presence or absence of a drive. A unit wired as present but actually disconnected returns present but Not Ready; a unit connected but wired in the control as not present will not return Present but will return Ready.

Address Coincidence Not Achieved

Address Coincidence Not Achieved is the result of failure to locate a given address within 2 index pulses. The operation is terminated with this exception condition, even if data has been sent to the system or received from the system and partially written. The Seek Status flip-flop is reset. This exception cannot occur on Write Index or Read Absolute operations as the control is pulse directed and does not search for specific addresses in these cases.

Illegal Address

Illegal Address is reported by a drive when a cylinder address exceeds the maximum valid value. The cylinder field in the address is used for determination of this exception condition. DCC-3 clears the Seek Status flip-flop, initiates a seek to cylinder 0, and returns the exception result. This procedure provides compatibility with disk pack address error recovery functions.

Seek Incomplete

Seek Incomplete is an error detected only on the 32-sector/track units when a Seek fails to position the head correctly within 200 milliseconds. The signal of this condition is reset only upon another Seek being initiated by DCC-3.

The control responds immediately to a Seek Incomplete during these four circumstances:

Write Index
Read Absolute
Internal seek during multiple-cylinder Read operation.
Internal Seek during multiple-cylinder Write operation.

DCC-3 terminates the operation, reports the exception, leaves the Seek Status flip-flop reset, and initiates a Seek to cylinder 0. Should this latter seek also fail, the drive will be in a Seek Incomplete state when a later operation is initiated.

Should Seek Incomplete occur during an implicit Seek caused by an ordinary Read or Write operation, the originating operation is terminated before the exception occurs and is consequently unaffected. For the next 200 milliseconds the drive will be seeking, following which the Seek Incomplete occurs and is signaled by the drive. DCC-3 takes no action until another operation is initiated to that drive. When this occurs, for any operation, the control resets the Seek Status flip-flop, reports the exception condition, and initiates a Seek to cylinder 0.

Seeking

Seeking is true when any operation is received for a drive which is seeking, whether or not the Seek Status flip-flop is set. One bufferload of data is received for a Write or Write Index operation; for those operations of Read or Read Absolute operations a result is returned with bit 16 reset. The Seek Status flip-flop is unaffected.

A Test operation sent to a seeking drive reports that fact without setting the exception condition. Seek Status flip-flop set prevents an implicit Seek for a Read or Write operation, to permit a previous operation causing a Seek to complete. This avoids the possibility of a potentially eternal series of conflicting Seeks. The condition is also reported on a Test operation.

DISK PACK SUBSYSTEM

Introduction

The interface between the B 1800 systems and various multiple-platter disk packs is provided by the disk pack subsystem. This subsystem includes one or more dual drive disk pack units, a disk pack electronic control (DPEC), and the disk pack control (DPC-2). The subsystem may also include an expansion adapter, as shown in figure 6-11. Current subsystems range in capacity from 65 to 175 megabytes. Table 6-6 summarizes the characteristics of the disk pack units.

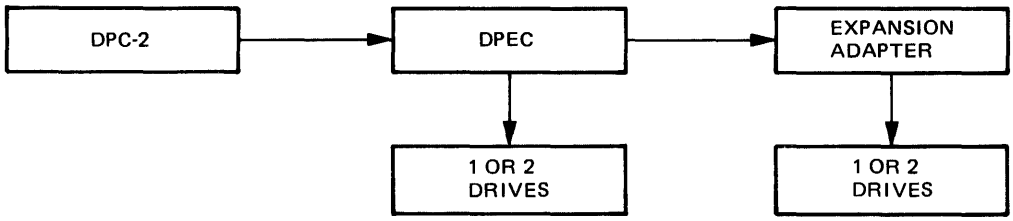


Figure 6-11. Disk Pack Subsystem Configuration

Table 6-6. Characteristics and Capacities of Disk Pack Units

	B 9499-7	B 9499-8	B 9484-25	B 9484-55
Model No.	225	225	205	206
Tracks/Surface	406	203	416	208
Sectors	485,170	242,585	362,230	181,115
Bytes/Pack	87,330,600	43,655,300	65,201,400	32,600,700
Tracks/Inch		200		370
Density (bpi)		4400		6000
Sectors/Track		60		90
Recording Surfaces		20		5
Access Time (ms)		30		25
Latency (ms)		12.5		8.3
Peak Transfer Rate (MB)		5		10

General Information

DPC-2 provides the interface between the Central Processor and a disk pack electronics controller, which, in turn, is the interface to the disk pack units. DPC-2 can be assigned any channel from 8 to 14; it is generally placed on channel 9 for software compatibility with other B 1800 or B 1700 sites. (Channel number is part of all actual sector addresses perceived by software.) Data is transferred between control and system in 24-bit parallel fashion. DPC-2 includes five 180-byte (sector-size) buffers. Each cylinder on a pack has five sectors, termed "spare sectors", to which sectors that are found to be unusable on the cylinder are relocated. Relocation of such faulty sectors is normally an initialization function. The DPEC transparently switches from a sector flagged as defective to the appropriate spare sector. Spare sectors not used for sector reassignment are not addressable by the disk pack subsystem.

Consecutive sectors addresses on the B 9499 drives correspond to contiguous physical sectors that start at head 0, cylinder 0 (outermost cylinder) and continue by head and cylinder. (The latter incrementing less frequently.) Every surface except the first has 60 sectors (0-59). The first surface, served by head 0, has 55 sectors (0-54); the five spare sectors are in the positions that would otherwise be assigned 55 through 59.

On B 9484 packs, the incrementation of file addresses corresponds to interlaced sectors, neglecting spares and relocated sectors, which commence on head 0, cylinder 0 and continue by head and then by cylinder. Each surface but the last has 90 sectors, corresponding to the order: 45, 0, 46, 1, 47, 2, ..., 89, 44

On the last surface, the five spare sectors occupy what otherwise would be sectors 85 through 89.

Table 6-7 presents formulae to be used to calculate the head and cylinder on which a given non-relocated secton "n" is found:

Table 6-7. Head/Cylinder Calculation Formulae

B 9484	B 9499
cylinder = n DIV 445	cylinder = n DIV 1195
let m = n modulo 445	let m = n modulo 1195
head = m/90	head = (m>=55)*(1+m–55)

DIV specifies integer division (discard remainder). (m>=55) is Boolean and returns 0 or 1.

The B 9484 drives include a reserved cylinder that enables the Burroughs Field Engineer to perform tests on a given pack without endangering valid user information. This maintenance cylinder can be addressed in the normal manner by the 445 sector addresses following the highest sector. These sector addresses are in no way illegal and result in no exception condition; a software convention that they are not to be considered in the valid address continuum causes them to be unused and hence reserved for the intended maintenance function.

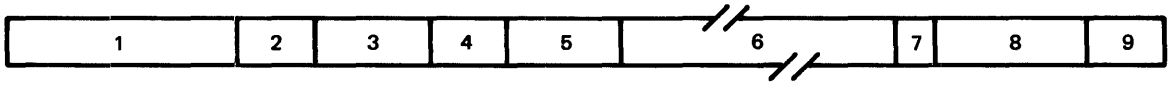
Figure 6-12 shows track format for the B 9499; figure 6-13 for the B 9484.

Operations

Operation Codes, Disk Pack Control

	← 0(MSB)			23(LSB) →		
READ	000M	WVED	XYZ0	0000	P000	UUUU
WRITE	0100	WV00	0000	0000	0000	UUUU
INITIALIZE	011A	WVOR	0000	0000	0000	UUUU
RELOCATE	1010	WVOR	NNN0	0000	0000	UUUU
TEST	100T	TPR0	0C00	0000	0000	UUUU
PAUSE	1110	0000	0000	0000	0000	UUUU

UUUU = unit (spindle) number. V is the Automatic Restore After Seek-Error variant; if V=1, automatic restore is disabled (B 9499 only). Other variants are defined under the appropriate operation.



1	– BOT GAP	– A 30-BYTE FIELD OF ZEROES RESERVED FOR VARIATIONS IN INDEX PULSE DETECTION
2	– SECTOR GAP	– A 6-BYTE FIELD OF ZEROES RESERVED FOR VARIATIONS IN SECTOR PULSE DETECTION
3	– ADDRESS PREAMBLE	– A 16-BYTE VFO PHASE-LOCK FIELD OF ZEROES AND A SYNC CODE BYTE OF ONES
4	– GAP A	– A 9-BYTE FIELD, UNDEFINED, ALLOWING READ-TO-WRITE SWITCHING TIME
5	– DATA PREAMBLE	– A 14-BYTE VFO PHASE-LOCK FIELD OF ZEROES AND A SYNC CODE BYTE OF ONES
6	– DATA	– 180 BYTES
7	– CHECK BITS	– 8 POLYNOMIAL CHECK CODE BITS FOR DATA VERIFICATION
8	– GAP B	– A 20-BYTE FIELD, UNDEFINED, ALLOWING WRITE-TO-READ SWITCHING TIME
9	– GAP C	– A 6-BYTE FIELD OF ZEROES RESERVED FOR VARIATIONS IN SYNC PULSE DETECTION

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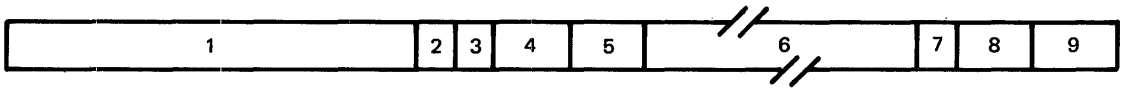
Figure 6-12. B 9499 Track Format



1	– BOT GAP	– A 60-BYTE FIELD OF ZEROES RESERVED FOR VARIATIONS IN INDEX PULSE DETECTION.
2	– ADDRESS PREAMBLE	– A 3-BYTE ADDRESS MARK, A 7-BYTE PHASE LOCK FIELD OF ALL ZEROES, AND A 4-BIT SYNC CODE OF @F@.
1	– ADDRESS	– A 32-BIT FIELD: 1 FLAG BIT (SET IF THE SECTOR IS AN UNUSED SPARE), 10 BITS FOR CYLINDER NUMBER, 5 BITS FOR HEAD NUMBER, AND 8 BITS FOR SECTOR NUMBER
1	– GAP A	– A 12-BYTE FIELD, UNDEFINED, ALLOWING READ-TO-WRITE SWITCHING TIME
5	– DATA PREAMBLE	– A 7-BYTE PHASE-LOCK FIELD OF ZEROES AND A 4-BIT SYNC CODE OF @F@
6	– DATA	– 180 BYTES
7	– CHECK BITS	– 8 BITS FOR PARITY VERIFICATION
8	– GAP B	– A 5-BYTE FIELD OF ZEROES ALLOWING WRITE-TO-READ SWITCHING TIME
9	– EOT GAP	

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Figure 6-13. B 9484 Track Format

Read

Data is read from pack starting at the given File Address until terminated by the system. For each sector read, ninety 16-bit data words are transferred by the DPEC, plus two error code words and one 16-bit result status word reflecting the status of the entire operation up to that point. Unless M or E variants are set, only the 180 bytes of data are returned to the system.

Should all buffers be filled prior to a Terminate Data command from GISMO, the control enters a "slip" mode wherein data transfers from disk are temporarily suspended until a buffer has been unloaded. A Terminate Data command may be received at any time; a full buffer load is not necessary. Data transfer in this case is immediately stopped and the operation is terminated.

The substantial number of variant bits which change the behavior of the Read operation are clarified below. All variant combinations not cited are invalid and produce undefined results.

If variants MEDP = 0E00, variants W, X, Y, and Z, sent to the DPEC, specify the following Read operation options:

0000 Normal Read (B 9484).
10Y0 Enable strobe; Y gives direction: 0 = , 1 = + (B 9484).
0X01 Enable offset; X gives direction as above (B 9484).
1XY1 Enable strobe and offset; directions as above (B 9484).
1000 Disable Automatic Restore after Seek Error (B 9499).

If variants MEDP = 0E01, Read data is verified. The W, X, Y, and Z variants are sent to the DPEC.

XYZ = 000 indicates normal sectors.
XYZ = 001 through 101 indicates spare sector 1 through 5 on the given cylinder. In the latter case only one sector is read. A spare sector cannot be selected if it is in use as an actual replacement sector. The V variant must be 0 on the B 9484; on the B 9499 it disables Automatic Restore after a Seek Error.

If E is set in any of the above variant combinations, 32 bits of the error code and the DPEC 16-bit result are returned after the data for each sector read. In the final result for that operation, bits 16 and 21-23 are set to 0001.

M=1 Sync code, address, data, data check bits and postamble are returned as well as the 16-bit DPEC result. Should the sector be relocated, the sync Code and Address field will be all ones. The operation is not terminated by parity error or wrong address. A seek is unconditionally executed if so needed. Sector positioning is ascertained by counting sector pulses after detecting the index pulse, not by actual address. All other variants except MV must be zero; on the B 9484 drive, V also must be zero.

D=1 This causes a Read Extended Status Data (defined later) from the DPEC. This behaves identically to a normal Read operation except that the data transfer from the DPEC to DPC-2 is terminated after 64 bits (if not terminated earlier by the I/O Driver). Similarly, the data returned to the system is automatically terminated after 264 bytes if a Terminate Data is not received. Data in excess of 64 bits is undefined. (This operation is not permitted on older, Design Level 1, models of the B 9499.)

W=0 DPC is not to wait on a busy exchange. The final Result Descriptor is returned with bits 0, 1, 16 = 110.

W=1 DPC-2 must wait on a busy exchange.

Write

Data is written to pack, starting with the sector specified in the File Address field, until terminated by the system. Zero fill on an incomplete last segment is automatically provided by DPC-2. Ninety 16-bit words are sent from DPC-2 to the DPEC, plus two dummy words. While the dummy words are being transferred, the DPEC writes the error code on disk.

Should all five buffers become emptied prior to receipt of a Terminate Data command, the control enters the slip mode and waits for a Terminate Data command or a buffer load of data.

W Wait-on-Busy-Exchange variant. See Read, above.

V=1 Automatic-Restore-After-Seek-Error is disabled (B 9499).

Initialize

All format bits are written starting with the entire track on which the File Address sector lies. That track of the remainder of the pack can be written. Spare sectors are also initialized. Data fields of all sectors initialized are written with the data pattern specified by the R Variant. DPC-2 considers this to be a form of Write Operation, but the DPEC normally accepts only one 16-bit data transfer.

A=0 Calculated track only.

A=1 Entire pack past and including calculated track.

W=1 Wait for Busy Exchange variant (see Read).

Q=0 Data fields are written with the @FF@ sync byte and the actual sector address is repeated 45 times (B 9499), or with the actual sector address and EPL repeated 45 times (B 9484). EPL is an Error Protection Logic code used within the DPEC.

R=1 Data fields are written with the first two characters of data received from the system repeated 90 times.

Relocate

The Address Field of the sector specified by the File Address field of the I/O descriptor is marked as relocated. The Address Field of spare sector NNN is marked as that same address; the spare sector's data field is written with the pattern selected by the R variant. Both sectors involved in this operation are located by counting sector pulses following the index pulse. Spare sectors must be allocated in reverse order: N=5 (the last physical sector on the track) first.

DPC-2 considers the relocation operation to be a form of Write Operation, but the DPEC will accept only one 2-character data transfer.

W	Wait-On-Busy-Exchange variant (see Read).
V=1	Disable Automatic-Restore-After-Seek-Error (B 9499 only).
R	Data Specification variant (see Initialize operation).
NNN	Specifies the desired spare sector on the designated cylinder. (Sector 1 to 5 only; other bit combinations are not valid.)

Test

The drive is tested, the action specified by the variants is performed, and a result is returned. If the unit is busy, DPC-2 will wait on an exchange until a path to the unit is available. Information returned includes:

1. Ready Status
2. Write Lockout status of drive
3. Drive ID
4. Exchange configuration
5. Seek status
6. Flip-flop status
7. Transmission error
8. Control ID (@1E@)

The Test and Wait (TT) variants have the following meanings:

00	Return result immediately.
01	Store result only if drive is not present or not ready.
10	Store result only if drive is present, ready, and not seeking.
11	Undefined.

Other Test operation variants are defined as follows: Place drive off-line for disk pack removal if unit is present and available. TTP must be 000.

P=1	Execute a pause of 1 to 2 milliseconds pause before returning a Service Request. Bit 16 in the Result Descriptor is reset (0).
C=1	Clear all seek status flip-flops. (This function is also performed by the Test and Clear primitive or the CLEAR pushbutton.)

Pause

After a pause of 1 to 2 milliseconds, DPC-2 returns a Service Request; bit 16 in the returned result is reset to inhibit storage of the Result Descriptor by GISMO.

Result Descriptor

The Result Descriptor for DPC-2 is defined below. Each bit is valid for all operators unless otherwise noted. Bits not included in the table are reserved. Exception conditions are discussed in the paragraphs that follow.

Result Descriptor, Disk Pack Control

Bit	Meaning
0	Operation complete.
1	Exception: any of bits 2-4, 6, 9, 10-15, or 22 set on all operations except Test; 2, 6, 12, 14, or 15 set on Test.
2	Not Ready.
3	Read data error. (Read)
4	Attention.
6	Write lockout. (Write, Initialize, Relocate) On the B 9499, this bit is also returned on Test. In Error Correction mode, this bit is returned on Read only (both drives).
7	Slip occurred. (Read, Write)
7-9	Unit ID (Test); wired by Burroughs Field Engineer: 000, not present; 001, B 9499-8; 010, B 9499-7; 011, B 9499-55; 100, B 9499-25; 101 to 111, reserved.
9	Address parity error or sync code error. (Read, Write)
10	Sector address error. (Read, Write, Relocate)
11	Timeout. (Read, Write, Test, Relocate)
10-11	Configuration (Test), wired by Burroughs Field Engineer: 00, no exchange; 01, 10, 11 = exchange 1, 2, 3, respectively.
12	Seeking. (Test)
14	Seek Status flip-flop set. (Read, Write, Relocate, Test)
15	Transmission parity error.
16	Operation complete.
17-23	Test: Control ID, @1E@ for DPC-2. Special flags: 001 is returned on Read with E=1; 001 is also returned on Read, Write, Initialize, and Relocate to signify that the Extended Status Report is available.

Not Ready

If, at the start of or during any operation, the selected DPEC or drive is or becomes Not Ready or Unsafe, the operation is terminated and a Not Ready is exception reported. An drive is defined as unsafe if rotational velocity levels or certain voltage levels move outside defined bounds.

Not Ready is also reported on all operators except Test with TT=10 if the drive is not present.

Not Ready is reported if the missing spindle is addressed on a single-spindle drive, but Not Present is not reported.

Read Parity Error

During a Read operation, the Error Check Code (ECC) following the actual data within a given sector is checked by the DPEC. Detection of an error causes a report to the control, which returns this exception (unless the E variant is set) upon completion of the operation.

The ECC provides for detection of any error burst of 32 or fewer bits, detection of almost all error bursts exceeding 32 bits, and correction of all error bursts of 11 or fewer bits. Correction is an algorithmic software phenomenon achieved after re-reading a faulty sector with E=1.

Attention

Bit 4 is set to indicate a DPEC or drive failure, specifics of which can be ascertained by a Read-Extended-Result-Status operation.

Write Lockout

This result causes any Write, Initialize, or Relocate operation to be immediately terminated. The condition is reported on a Test operation for the B 9499 drive only.

Error Correction Made

Reported if an ECC error was detected and corrected.

Slip Occurred

This result is for information only and is not considered an exception condition. Hence, Result Descriptor bit 1 is not set.

Address Parity Error

Detection of this phenomenon after the initial desired sector is encountered causes the operation to be immediately terminated. Failure to detect sector pulses on a B 9499 unit causes bits 4, 9, 10, 11, 22, 23 to be set on the same unit, failure to detect read data causes bits 9, 10, and 11 to be set.

Sector Address Error

Reported during a Read, Write, or Relocate operation when cylinder and head address fields indicate correct head positioning but the correct sector cannot be found despite an absence of sector address parity errors. The operation immediately terminates. On the B 9499 drive, this condition can be evoked if read data continues into the next sector.

Timeout

A Timeout exception is caused when no clock pulse is received for 1 second during a Read, Write, or Relocate operation.

A Seek Timeout during a Read, Write, Initialize, or Relocate operation also causes this exception.

The B 9499 drive reports timeout upon failure to decode cylinder or head address fields.

Seeking, Seek Status Flip-Flop Set

The reader is referred to a discussion of the seek process within the section on the B 1800 Disk Cartridge Control.

Transmission Error

Transfers of the operator, the File Address, data, and the result between DPC-2 and the DPEC are parity checked. Detection of even parity constitutes a Transmission Error. Occurrence during the initiate phase of an operation terminates that operation immediately; detection after the initiation phase causes this exception condition to be reported upon completion.

Should Transmission Error occur during transfer of the result from the DPEC, only bits 0, 1, 7, 15, and 16 can be guaranteed valid, except for the result from a Test operation, in which case, bits 7-11 and 17-23 are correct.

Second Operation Complete Bit

Bits 0 and 10 are always set in the Result Descriptor to indicate completion of an operation. Certain special cases cause the result as returned to GISMO to have bit 16 reset to indicate that a result is not to be stored in the Result Status field within the I/O descriptor. These cases include:

Pause complete.
Test operation with TT=10; unit Not Ready, Not Present or Seeking.
Test operation with TT=01; unit Ready.
Read, Write, or Relocate operation: unit seeking or seek already initiated by another descriptor to that drive.
Read, Write, Relocate, or Initialize operation: unit busy and W=0.
Read, Write, or Relocate operation: Unit Seek Status flip-flop set and address is for another cylinder.

Other special cases cause bit 16 to be reset and special flags to be set to indicate to the I/O Driver that additional action is required. The I/O Driver sets bit 16 in these cases before storing the result. The cases are:

Read with E variant set (Special Flags = 001).
Read, Write, Relocate, or Initialize operation caused a bit in extended status field to be set, necessitating an Extended Status Read for analysis (Special Flags = 011).

Should a Transmission Parity Error (bit 15) occur, bit 16 will always be set.

Table 6-8. DPEC Extended Status Word

Bit	Meaning
0	Read data error.
1	Write Lockout/B 9484 DPEC ECC correction made.
3	Drive Not Ready (positioner not settled).
4	Drive off-line.
5	Drive unsafe.
6	Address parity or sync code error. (Data sync error on B 9484.)
7	Sector address error.
8	Seek timeout.
9	Drive not present.
13	Operation complete in local. (Design Level 2 B 9499.)
14	Transmission parity error or illegal command.
15	Attention. (Not possible with Design Level 2 DPEC.)

Table 6-9. Relationship of DPEC and DPC-2 Results and B 9499, B 9484 Extended Status Results

DPEC Result	DPC-2 Result	Extended Status Result Bits	
		B 9499	B 9484
0	3	-	-
1	6	-	44
2	14	-	-
3	12	-	-
4	2	-	-
5	2	37,42,48-61	53,58,60,61
6	9	33,37,40	-
7	10	37,40	-
8	11	32,34,35,40,42	51
9	2	-	-
10		-	-
11		-	-
12		-	-
13		-	-
14	15	-	-
15	4,22,23	40-42,44-46,48-61	32-37,43-53,55-63

Table 6-10. Extended Status Result Descriptor, B 9499, B 9484

Bit	Meaning - B 9499	Meaning - B 9484
0	Always reset (0)	Cylinder 512 Address Decode
1	Cylinder 256 Address Decode	Cylinder 256 Address Decode
2	Cylinder 128 Address Decode	Cylinder 128 Address Decode
3	Cylinder 64 Address Decode	Cylinder 64 Address Decode
4	Cylinder 32 Address Decode	Cylinder 32 Address Decode
5	Cylinder 16 Address Decode	Cylinder 16 Address Decode
6	Cylinder 8 Address Decode	Cylinder 8 Address Decode
7	Cylinder 4 Address Decode	Cylinder 4 Address Decode
8	Cylinder 2 Address Decode	Cylinder 2 Address Decode
9	Cylinder 1 Address Decode	Cylinder 1 Address Decode
10	Head 16 Address Decode	Cylinder 1024 Address Decode
11	Head 8 Address Decode	Always reset (0)
12	Head 4 Address Decode	Head 4 Address Decode
13	Head 2 Address Decode	Head 2 Address Decode
14	Head 1 Address Decode	Head 1 Address Decode
15	Always reset (0)	Sector 64 Address Decode
16	Sector 32 Address Decode	Sector 32 Address Decode
17	Sector 16 Address Decode	Sector 16 Address Decode
18	Sector 8 Address Decode	Sector 8 Address Decode
19	Sector 4 Address Decode	Sector 4 Address Decode
20	Sector 2 Address Decode	Sector 2 Address Decode
21	Sector 1 Address Decode	Sector 1 Address Decode
22	Op code byte 1	Op code byte 1
23	Op code byte 2	Op code byte 2
24	Op code byte 3	Op code byte 3
25	Unit 4	Unit 4
26	Unit 2	Unit 2
27	Unit 1	Unit 1
28	Old, new cylinders not equal	Variant N0 (V)
29	Variant N1 (X)	Variant N1 (Z)
30	Variant N2 (Y)(D)	Variant N2 (Y) (D)
31	Variant N3 (Z)	Variant N3 (X)
32	Address sync start fault	DPEC blower failure
33	Data sync start fault	Read/Write clock absent
34	Head equal fault	Address mark absent
35	Cylinder equal fault	Read data not received

Table 6-10. Extended Status Result Descriptor, B 9499, B 9484 (Cont)

Bit	Meaning - B 9499	Meaning - B 9484
36	Forced head to zero	Index mark absent
37	Read data not received	Bit 37 true (1): Control Message (CM) error, bits 38 to 61 contain the last CM sent to the drive. Bit 37 false (0): Bits 38-61 contain the contents of the drive's status register (SR01-23; see table 6-11).
38	Spare	
39	Spare	
40	Sector pulse absent	
41	Drive Write data absent	
42	Seek Incomplete	
43	Sequence Count = 1 to 9	
44	Read/Write Clock absent	
45	DPEC blower failure	
46	Data skew	
47	Not used	
48	Speed error	
49	DC unsafe	
51	DC voltage low	
52	Read/Write error	
53	Write-current error	
54	Write/Erase current error	
55	Erase-current error	
56	Read-current error	
57	Head-select error	
58	Air-pressure error	
59	First Seek error	
60	End of cylinder	
61	Illegal cylinder	
62*	Sequence Count = 10	Bad DM response
63*	External Seek	Address overflow

* B 9499 only:
bits 62-63 = 00 - bits 40 to 63 are valid; bits 0 to 31 are valid for the previous operation if bit 43 is set (1).
= 01 - bits 0 to 31 and 40 to 63 are valid.
= 10 - undefined.
= 11 - all 64 bits are valid.

Table 6-11. B 9484 Status Register (Bits 38-61 of Extended Result Status Words)

Bit	Meaning
0	0 = B 9484-25; 1 = B 9484-55
1	Reserved
2	0 = 180-byte sector; 1 = 100-byte sector
3	0 = interlaced format; 1 = sequential format
4	Maintenance mode; reset by Power On or Reset Maintenance CM.
5	Write data absent.
6	Write protected and Write Enable.
7	Seek command while Not Ready.
8	Illegal head; reset by correct head selection or Restore operation.
9	Illegal cylinder; reset by Restore operation.
10	Spindle address error.
11	Offset during Write Enable.
12	Seek during offset.
13	Seek Incomplete; reset by Restore operation.
14	Off-track and Write Enable.
15	Carriage hits forward or rear stop; power goes down. Reset by cycling STOP/RUN or AC power.
16	Reserved.
17	Write current and no Write-Gate, or Write-Gate and no Write current.
18	No MFM transitions.
19	Head select fault.
20	DC power fault; drive powered down.
21	Temperature warning; reset when temperature goes below threshold 1.
22	Temperature critical; drive powered down. Reset when temperature goes below threshold 2.
23	RPM low; drive powered down. Reset by cycling STOP/RUN or or AC power.

NOTES

Except where noted, all bits are cleared when status is reported to DPC-2.

A Status Register error report occurs when one or more of bits 5-20, 22, 23 is true or when bit 21 first becomes true.

The DPEC automatically performs a Restore when bits 8, 9, or 13 are reported.

Should a second spindle report Attention before the DPEC Status Register is cleared (by being read), the DPEC reports this fact to DPC-2 but does not change the Extended Status words.

HIGH-SPEED SYSTEMS MEMORY SUBSYSTEM

Introduction

Disk File Control-3 (DFC-3) allows the B 1800 I/O Subsystem to connect to and utilize a Disk Electronics Unit (DEU) which itself may connect to a primary Disk Storage (DS) Unit and from one to three add-on DS units. These DS units are ultra-high-speed, head-per-track devices with individual capacities of 5,898,240 bytes and an average access time of 5 milliseconds.

A DEU may be connected to an exchange, permitting use of as many as 16 DEs, each with 1 to 4 DSs. The configuration scheme is shown in figure 6-14.

DFC-3 can be assigned any channel from 8 to 14. Information transfer between DFC-3 and the DEU is bit serial at a rate of 10 million bits per second. Transfer between processor and DFC-3 is 24 bits parallel. The control includes three 180-byte (sector) buffers; each buffer also provides space for a 32-bit error check code and a 16-bit intermediate result.

The DEU can be adjusted by a Burroughs Field Engineer to include a Segment Interleaving Option; this lowers the effective transfer rate to one-half or one-fourth the full rate to avoid monopolizing processor capacity in smaller systems. This option is seldom, if ever, needed with a B 1870 processor.

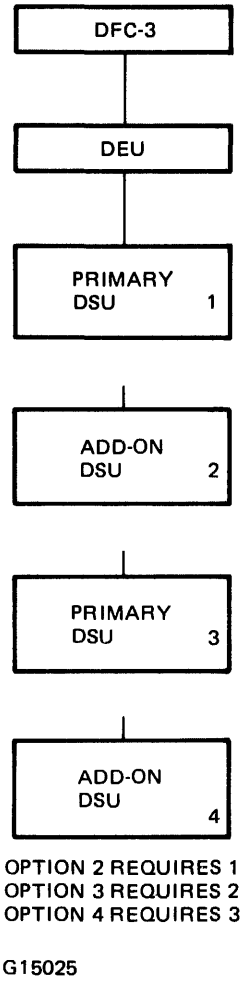


Figure 6-14. Disk File Subsystem Configuration

On a Read operation, if all three buffers are filled before a Terminate command is received from the I/O Driver, the control enters a "slip" mode of operation whereby data transfer from disk is suspended until a buffer is available. Likewise, should all three buffers become empty during a Write, the slip mode is again entered until receipt of a Terminate or until the processor fills a buffer. The Terminate may be received prior to a buffer being emptied. On a Write operation this causes zero filling; on a Read, the data transfer is immediately concluded.

Operations

Operation Codes, 5N Disk Control

	← 0(MSB)				23(LSB) →	
READ	000M	W0ED	0000	0000	0000	UUUU
WRITE	010M	W000	0000	0000	0000	UUUU
TEST	1000	0000	0000	0000	0000	UUUU
PAUSE	1110	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

UUUU = DE unit number; other variants are described under the appropriate operation.

Read

The disk is read, starting from the File Address field, from the memory location specified by the A address to the location specified by the B address minus 1. The length (B-A) need not be an integral sector multiple, but parity checks are performed on all sectors fully or partially read.

Only the data bits are sent to memory unless the E Variant is set, which causes the 32-bit Error Correction Code (ECC) to be returned with each sector of information. In this case, the result is returned with bit 16 = 0 and bits 21-23 = 001.

D = 1 causes the DE unit to return extended status data. (At this writing, the length of this field is 64 bits.) This data is then transferred to the system until terminated by the I/O Driver or by the transfer of a full (180-byte) buffer load. The M and E variants must be reset. The Extended Result Descriptor provides a more detailed exception analysis than can be contained in the 24-bit result status field. (See table 6-13.)

Write

Data, starting with the File Address, is transferred to disk from the memory location specified by the A address to the location specified by the B address minus 1. Zero bits are written to complete the last sector. DFC-3 transmits a sector of data followed by a 32-bit Error Correction Code for each sector written. After all sectors are transferred, an 8-bit result reflecting the cumulative status of that Write operation is returned by the DE unit.

Test

DFC-3 and the selected DE and DS unit combination is tested for Ready/Not Ready, Busy/Not Busy, Write Lockout, DE Unit ID, Configuration, or Control ID.

Pause

A 3 to 4 millisecond pause occurs before returning a service request. To indicate that the I/O Driver should not store the Result Descriptor, bit 16 = 0 and bits 21-23 = 000.

Stop

This operation is performed by the I/O Driver and is not sent to DFC-3. The I/O Driver stops linking and immediately returns a result with an interrupt request.

Result Descriptor

Table 6-11A defines the meanings of the Result Descriptor bits for DFC-3. Bits not included in the table are reserved. Bits apply to all five operators unless the applicable operations are listed in parentheses.

Table 6-11A. Result Descriptor, Disk File Control

Bit	Meaning
0	Operation Complete
1	Exception Condition; one or more of bits 2,3,5,6,10-13,15, 22 set. (Note: This bit is not set on a Test operation if only one or more of bits 6,7,8,9,10, and 11 are set.) An interrupt is always returned.
2	Not Ready. The selected DS or DE unit went Not Ready, or a Test operation failed to complete within 500 milliseconds. (Read, Write, Test) Not Ready is also reported if a unit is not present on a Read or Write.
3	Read Parity Error Detected by DE (Read), or unit is busy (Test). The 32-bit Error Correction Code (ECC) returned with the Read of every sector is incorrect. This code provides for detection of all error bursts of 32 bits or less and the great majority of those exceeding 32 bits. All error bursts of 11 bits or less are correctable by the software. The ECC polynomial is $X^{32}+X^{30}+X^{21}+X^{9}+1$.
5	Memory parity error. Set by software; applicable to data transfer only. A parity error during an I/O descriptor fetch generates the usual port 0, channel 15 interrupt.(Write)
6	Write lockout. (Write, Test)
7	Slip occurred. This is not an exception condition criterion. (Read, Write)
7-9	Unit ID. This value, set by the Burroughs Field Engineer, may be 000 for unit not present or 001 for the 5N disk storage unit. All other possible values are reserved. (Test)
10	Address error. This condition occurs if (1) an address compare is not achieved within 15 milliseconds after the start of a segment address search, or (2) the track address read from the disk at the beginning of each segment differs from that held by the DE, or (3) data cannot be located on the specified track within 15 milliseconds. In all cases, the operation is terminated. (Read, Write)
11	Timeout. The operation does not complete within 500 milliseconds. (Read, Write)

Table 6-11 A. Result Descriptor, Disk File Control (Cont)

Bit	Meaning
10 to 11	Configuration (Test). Set by the Burroughs Field Engineer: 00 = DFC-3 is directly connected to a DEU (no exchange); 01, 10, 11 = DFC-3 is connected to Exchange #1, #2, or #3.
13	Command parity error . (Read, Write, Test) Two conditions can cause this bit to be set: (1) A parity error is detected in one of the internal commands between DFC-3 and the DEU or between the DEU and the DS unit. The operation is terminated. (2) A parity error is detected during the result status transfer phase. Bit 15 is also set; the operation is not terminated. (Note: Not Ready, Read Parity Error, Write Lockout, Address Error, and DE attention may be incorrectly reported in this case.)
15	Data transmission error. Detected by DFC-3 on Read and by the DEU on Write.
16	Operation complete. Exceptions: (1) Read or Write with the DEU reporting fault or warning conditions: bit 16 = 0, bits 21-23 = 011; the I/O Driver sets Bit 16 after receiving the result. (2) On a Read or Write with E = 0: bit 16 = 0, bits 21-23 = 001; the I/O Driver sets bit 16. Exception (1) takes precedence if it occurs simultaneously. A result is never stored on a Pause or on a Read or Write operation with W = 0 a busy or absent DEU. In these cases, bits 16 and 21-23 are reset and the Driver does not store the result.
17 to 23	Control ID (returned on Test only) ~~0011000~~ 0100100 (@24@) must list all
21 to 23	Special flags: 21-23 = 001, Read complete (Read with E =1) 21-23 = 011, DE attention (Read, Write)

Table 6-12 defines the result status byte that is returned by the DEU.

Table 6-12. Result Status Byte Received From DEU

Bit 0	DS unit Not Ready
1	Write lockout
2	Address error
3	Command transmission error
4	Data transmission error
5	Warning
6-7	Unused

Table 6-13 defines the contents of the Extended Status Register. This 64-bit block of information is returned after a Read operation with the D variant set. The Extended Status Register is cleared after each Read, Read-Maintenance (Read with M = 1), Write, Write-Maintenance (Write with M = 1) and Test operation.

Table 6-13. Extended Status Register (64 Bits)

	Reported as Not Ready:
Bit 0	*Excessive temperature
1	*Head retracted
2	*Head-touch
3	*Disk speed low
4	*Write driver overheat*
5	*Negative housing pressure
	Reported as Warning:
Bit 10-13	Temperature high, DS unit 0, 1, 2, 3; reported only on change from normal.
14	AC power low
	Reported as Address Error:
Bit 17	Address redundancy check error
18	Phi bit timeout (no data on track)
19	Address search timeout
	Reported as Command Parity Error:
Bit 21	Internal address parity error
22	Control channel parity error
23	Invalid request
	Reported as Data Transmission Error:
Bit 28	ECC error (Read)
29	ECC error (Write)
30	Clock sync error (Write)
31	Write failure (Write)
	Not Reported in Result Status Field:
Bit 41-42	DS unit number 0-3
46-49	Head number 0-15
50-54	Track number 0-31
57-63	Segment number 0-107

* In addressed DS unit.
Note: Omitted bits are not used.

READER SORTER SUBSYSTEM

Introduction

Reader Sorter Control-2 (RSC-2) provides the system interface with any of several MICR or numeric OCR reader-sorters. Although RSC-2 may be assigned any channel 0 through 14, it is generally placed on channel 13 because the reader-sorter is a high-speed, on-line device. (Channel 14 is recommended for the single-line data communication control, if present; this allocation of channels yields optimal performance.)

A reader-sorter is wired by the Burroughs Field Engineer to supply data to RSC-2 in either 4-bit or 7-bit form. Tables 6-14 and 6-15 provide the appropriate representation. The translated data is placed in a buffer within RSC-2; formatting is performed.

Table 6-14. 4-Bit Read Data

Sorter Symbol		Sorter		EBCDIC
CMC7	E13B	Code	EBCDIC	Graphic
0	0	0000	1111 0000	0
1	1	0001	1111 0001	1
2	2	0010	1111 0010	2
3	3	0011	1111 0011	3
4	4	0100	1111 0100	4
5	5	0101	1111 0101	5
6	6	0110	1111 0110	6
7	7	0111	1111 0111	7
8	8	1000	1111 1000	8
9	9	1001	1111 1001	9
S1	Amount	1010	0111 1011	#
S2	Transit	1011	0111 1100	@
S3	On-Us	1100	0111 1010	:
S4	Hyphen	1101	0110 0000	-
S5	(1)	1110	0111 1101	'
(2)	(2)	1111	0101 1100	*

(1) not used; (2) can't read

Table 6-15. 7-Bit Read Data

Sorter Symbol		Sorter		EBCDIC
OCRA	OCRB	Code	EBCDIC	Graphic
0	0	011 0000	1111 0000	0
1	1	011 0001	1111 0001	1
2	2	011 0010	1111 0010	2
3	3	011 0011	1111 0011	3
4	4	011 0100	1111 0100	4
5	5	011 0101	1111 0101	5
6	6	011 0110	1111 0110	6
7	7	011 0111	1111 0111	7
8	8	011 1000	1111 1000	8
9	9	011 1001	1111 1001	9
Hook	<	011 1100	0100 1100	<
Fork	(1)	011 1101	0111 1110	=
Chair	>	011 1110	0110 1110	>
|	|	010 0001	0100 1111	|
(2)	(2)	010 0000	0100 0000	(2)
(3)	(3)	001 1010	0011 1111	(2)Sub
(1)	+	010 1011	0100 1110	+

(1) not used; (2) can't read; (3) blank

Control-to-processor transfers are always in 100-character bursts of data, even if zero characters are read. RSC-2 transfers one character at a time with the rightmost character first. Following the data transfer, a delimiter character (@7D@) is sent, followed by enough blank characters (@40@) to fulfill the 100-character requirement. Note that a buffer of zero characters merely results in the sequence @70@ and 99 (@40@). RSC-2 does not recognize the Terminate Data command.

As a document passes a read head, if a buffer is available, that data will be loaded thereinto regardless of the receipt of a Read operation. Should no control buffer be available, Too-Late-To-Read immediately results. All characters that cannot be read from a document are transferred to the system by RSC-2.

MICR data contains no blank characters except for the aforementioned blank-fill characters. Seven-bit OCR data can accept blank characters if contained on the document. However, multiple consecutive blanks are reported to the control as a single blank. Detection of Canadian checks is the responsibility of software.

Upon completion of a Read operation, it is the function of an application program to determine the pocket into which a given document is to go, and whether or not an endorsement is required. Information is placed by the program into the I/O descriptor and the I/O Driver is given control. A Test Status command is emitted to the Reader Sorter Control, which must be in Status Count 1. RSC-2 indicates to the I/O Driver by a flag in the returned result, that pocket and endorsement information is required. I/O Driver transfers out this data in the following format:

Command	Channel	Zeros	Pocket/ Endorsement Info.
4 Bits	4 Bits	9 Bits	8 Bits

where the pocket/endorsement field is comprised of

2 bits - Validity
5 bits - Pocket Select
1 bit - Endorsement

Validity is normally 00, unless "double document" has been reported on Read. This is elaborated in the discussion of the Result Descriptor later in this section. If the endorsement bit is set, the non-impact endorser will process the document. Should this option not be present on the reader-sorter, the bit will be ignored.

Upon accepting the pocket/endorsement data and returning status, the I/O Driver enters a loop in which a Test Status is repetitively performed until RSC-2 indicates that a result is ready. This typically requires 10 to 12 microseconds. The I/O Driver is then able to transfer in the following information:

Status 8 bits (should be @01@)	Zeros 8 bits	Result 8 bits

where RESULT may be:

@40@ = double document routed to Reject Pocket
@80@ = successful Pocket Select
@CO@ = too late to Pocket Select

This is stored in the File Address field (commonly termed the "PS" field when describing the reader-sorter) of the I/O Descriptor, and the normal linking to the next descriptor occurs unless the report was Too-Late-To-Pocket-Select, in which case the I/O Driver merely exits. It should be noted that a successful result provides indication that pocket selection was completed in time, but there is no guarantee against a later jam or missort. Too-Late-To-Pocket-Select is defined to be the failure to receive the pocketing information before the document physically reaches the appropriate area of the reader-sorter. This condition, aside from affecting the I/O Driver operation as described above, causes the reader-sorter to turn off the document feeder and to stop reading. Documents still flowing that preceded the problem item are pocketed normally. The problem item and those following are routed to the Reject pocket during the 350-millisecond period commencing when the last item is fed. Normal operation resumes during or after this timeout period upon receipt of any operation code.

Reader Sorter I/O Descriptor Fields

A brief review of the meaning of certain fields in the I/O Descriptor for the reader-sorter follows.

The Actual Ending Address (AEA) field is defined only for the Read Operation. Because this is a reverse-read device, the final AEA value must equal the B address minus (100*8), due to the 100-character-burst mode of this peripheral.

Upon storing the Result Status (RS) information and returning any requested interrupt, the Driver exits from a Read operation and waits for pocket select information from the user program.

After the pocket select information and transferred to the control, assuming no Too-Late-to-Pocket-Select condition or any exception conditions, the Link address is fetched to locate the next descriptor's RS field. After a non-Read operation, the Driver normally links to the next I/O descriptor unless an exception condition has occurred.

The 24-bit Op field contains the operation code (bits 0, 1, 2) and may also contain variant bits.

The A and B addresses have meaning only for a Read operation.

Finally, the Pocket Select (PS) field, also 24 bits wide, receives pocket select and endorsement data from the program, as well as the Pocket Select Result from GISMO.

Operations

Operation Codes, Reader-Sorter Control

	← 0(MSB)				23(LSB) →	
READ	000H	R000	0000	0000	0000	0000
BATCH COUNT	1010	0000	0000	0000	0000	0000
POCKET LIGHT	010N	NNNN	0000	0000	0000	0000
TEST	100W	0000	0000	0000	0000	0000
PAUSE	1110	0000	0000	0000	0000	0000
STOP	1110	0000	0000	0000	0000	0000

H = 1, halt feeder;
R = 1, read first station;
W = 1, wait for Ready;
NNNNN, pocket number.

Read

Data is read into descending memory locations starting at the location specified by the B address minus 1 to and including the location specified by the A address, or until all data is stored. RSC-2 delimits data with @7F@ followed by blanks (@40@) until a total of 100 characters is reached. Reading is permitted only in flow mode, defined to be the state in which documents are being fed from the input hopper at maximum rate. Documents are processed sequentially; data is sent to the processor and pocket select information is sent to the reader-sorter before the next Read initiate is sent to the control.

Data is stored into descending memory locations due to the fact that documents flow right edge first.

The feeder may be smoothly halted with the H variant. This affects the read in no way; the document in process when H is detected generally will not be the last one processed before the reader-sorter actually stops.

Batch Count

An option for the reader-sorter is an endorser, enabled or disabled manually, to endorse the back of every document passing through the reader-sorter. This has no relation to the programmatic non-impact endorser previously discussed. One item printed by the endorser is a batch number. Execution of a Batch Count operation increases the batch number thus printed by one. Certain hardware timing restrictions ensure that this operation cannot occur while documents are flowing. A 350-millisecond timeout period must lapse after the last Read operation before the operation is sent from the control to the reader-sorter and the result is returned.

Results are undefined if a Batch Count operation is received by a control attached to a reader-sorter with no endorser.

Pocket Light

The Pocket Light specified by NNNNN is illuminated; the reader-sorter goes Not Ready and accepts only Pocket Light operations. NNNNN may have the following values:

NNNNN	Pocket
00000	0
00001	1
.	.
.	.
.	.
11110	30
11111	reject

This provides a means of program/operator communication. Each pocket has a clearly-visible light. These lights may at times be illuminated by the reader-sorter itself to indicate such conditions as full pocket or missort. When a pocket light goes on for any reason, the reader-sorter goes Not Ready. The initial Pocket Light operation lights a light only if the unit is Ready. Subsequent Pocket Light operations can be performed only if the unit is Not Ready. Other types of operations are not permitted between Pocket Light operations; however, if one occurs, the next Pocket Light operation is handled as an initial Pocket Light operation and is not executed because the unit is Not Ready, which is the condition that is reported in the Result.

Not Ready is not reported when RSC-2 executes the Pocket Light operation. A request to illuminate a non-existent Pocket Light has undefined results.

Test

The reader-sorter is tested for the following conditions:

Not Ready
Jam
Missort
Control ID (@14@)

W = 1 specifies that a result is to be returned when the unit goes Ready; otherwise, the result is returned immediately.

Pause

A service request is returned after a pause of 7 to 8 milliseconds. Bit 0 of the Result Descriptor must be set (1); other bits are undefined. On completion of this operation, a test is made by the I/O Driver to see if the operation on which the Pause occurred is ready for execution. If so, that operation is initiated; if not, the Pause operation is repeated.

Stop

The I/O Driver stops linking through descriptors and returns a result and and an interrupt if so requested. This operation is not sent to RSC-2.

Result Descriptor

The Result Descriptor for RSC-2 is listed below. Bits not included in the list are reserved. Each bit is applicable to the operators listed in parentheses; when none are listed, the bit applies to all RSC-2 operators.

Result Descriptor, Reader-Sorter Control

Bit	Meaning
0	Operation complete. (Set in all cases.)
1	Exception condition. (Any of bits 2, 3, 5, 9, 10-14 set.)
2	Not ready. (Read, Batch Count, Test, Pocket Light)
3	Unencoded document. (Read)
5	Cannot read. (Read)
7	OCR data. (Test)
9	Double document. (Read)
10	Too late to read. (Read)
11	Jam. (Read, Test)
12	Missort (Read, Test)
13	Batch ticket - this is the last item in the path. (Read)
14	Halt variant - this is the last item in the path. (Read)
16	Operation complete.
17	Control ID: 0010100 (Test)
to	or – Terminate Linking. (Any of bits 3, 11-15 set.) (Read)
23	

Operation Complete

Bits 0 and 16 are always set upon completing an operation. A Pause operation never stores a result.

Exception Condition

An interrupt is always returned when this bit is set.

Not Ready

Not Ready is defined as any of the following conditions:

1. Power off or not fully up.
2. Unit not on-line.
3. Jam.
4. Missort.
5. Empty feed hopper.
6. Full pocket.
7. START/STOP bar depressed while unit is Ready.
8. Pocket Light illuminated by unit or by RSC-2.
9. Feed check – feeder on, but no item fed within a reasonable time period.
10. Transport shuts down after feeder has been off for several minutes.
11. Open interlock (cover lifted).

Not Ready turns the feeder off immediately and RSC-2, upon sensing the Not Ready, also signals the feeder to halt. However, where practical, the transport continues in order to read, pocket select, and pocket those items already in motion. "Practical" may be defined as empty feed hopper, full pocket, stop bar pressed, and feed check.

After processing the last document and receiving initiation for another Read operation, a 350-millisecond timeout interval occurs, following which an invalid buffer-load of data and a Not Ready result are returned. The program must not Pocket Select.

In the "non-practical" instances, such as open interlock or power down, the transport immediately stops. This condition probably requires the operator to remove several documents from the transport. On some models, the transport covers are physically locked while the transport mechanism is in motion to avoid this problem. Neither the control nor software can distinguish the cause of a Not Ready; operation proceeds as if all documents in motion will be processed normally. Therefore, the operator must remove documents that stop in the transport area and assist in the appropriate recovery.

Unencoded Item

This result reflects a document from which no non-blank characters not even a "Cannot Read" character, are read. This condition is not reported, the document must be Pocket-Selected, and operation continues normally.

Cannot Read

This condition occurs when one or more characters on a document cannot be interpreted. Cannot Read and Unencoded Item (discussed above) are mutually exclusive.

The Cannot Read condition does not invalidate the data that has been read. The problematic characters appear in the data as shown in the translation charts (tables 6-38, 6-39). If the bad data is not in a field actually needed by the program, normal program execution can continue. Whether this is the case or not, the document causing the condition must be pocket selected. Execution continues normally.

OCR Data

This bit is returned on a Test operation to distinguish OCR from MICR translation.

Double Document

Bit 9 is a signal that one of several conditions involving document motion has occurred, including double feeding, underspacing between documents and over-or under-length documents between the feeder and the read station, or document slippage between the read head and the reject pocket. Slippage is reported immediately on detection. Other conditions are reported after the first affected document reaches the read station. The reader-sorter remains ready. Upon receiving the Double Document report, RSC-2 signals the feeder to halt and stops reading. The Read result is returned 350 milliseconds after the last document is fed provided the Double Document report is received before the control raises a Service Request. Otherwise the result is returned immediately.

Data read for the document for which this exception condition occurs is not valid. It is mandatory that the program issue invalid-pocket information (first two bits not 00) for the item in question unless certain additional exception conditions (Not Ready, Too Late to Read, Jam, or Missort) also occur, in which case pocket selection must not be made. RSC-2 will route the double document and following items to the Reject pocket.

If RSC-2 is waiting for pocket-select information when Double Document occurs, the pocket-select data is accepted and sent to the reader-sorter. The document is pocketed normally.

Unless Not Ready,Too Late to Read, Batch Ticket, Jam, or Missort are on or the H (halt) variant is true, RSC-2 automatically restarts the feeder without receiving a new initiate 350 milliseconds after the last item is fed.

Too Late to Read

This condition occurs when a document reaches the read head while the buffer in the control is still involved with the previous Read operation. RSC-2 immediately signals the feeder to halt and reading stops. The condition is generally reported in the result for the preceding item without the 350-millisecond timeout period. Timing, however, may be such that the condition is not reported on the prior document; in such cases, that document must be pocket-selected as usual. RSC-2 waits 350 milliseconds and returns the (erroneous) data and the result for the late item. The program must not send pocket-select information for the document. It and following items are routed to the Reject pocket by the control.

RSC-2 will accept another operation at any time, but will not execute a Read, Batch Count, or Pocket Light operation until 350 milliseconds after the feeder stops.

Jam

Detection of a jam causes the reader-sorter to immediately go Not Ready and stop the feeder. The control also signals the feeder to stop.

Jam is reported on the next Read result sent to the processor. This result is returned 350 milliseconds after the last document is fed if the Jam signal is received before the control raises a Service Request. Should the Jam signal be received after the Service Request is generated, the result is returned at once.

Read data is invalid for the item on which jam is reported, and the program must not issue pocket select information for it. However, if the control is waiting for pocket select information when the jam occurs, that information will be accepted and sent to the sorter. That document and preceding ones may or may not be properly pocketed, depending on the jam location.

The jam can occur before the read head, in which case all pocket-selected documents will be properly pocketed. If the jam occurs in the transport or pocket areas, the transport immediately halts. The operator must clear the jam and manually pocket the affected items.

If a jam occurs after the last item has its Read result returned, the jam cannot be reported to the system until a Read or Test operation is initiated, even though documents may be lodged in the transport area.

Missort

Detection of a sort mistake causes the reader-sorter to immediately go Not Ready and the feeder to stop. RSC-2 also signals the feeder to stop. The reader-sorter lights the pocket into which the document was erroneously routed. The discussion under Jam is precisely relevant to system behavior for Missort.

A document directed to a non-existent pocket on a reader-sorter with fewer than 32 pockets is reported as a Missort to the highest pocket and is reported on a subsequent document.

Batch Ticket

A batch ticket is a special document used to denote the end of a group of documents and to stop the feeding of further documents. It has a large black area detected photo-optically by the reader-sorter almost immediately after it is fed, enabling the feeder to be stopped before the next item is fed. The reader sorter signals the control that a batch ticket has been detected, and the control immediately signals the feeder to stop. Normal reading, pocket selection, and pocketing occur for the items in the sorter.

When RSC-2 senses that the last item (the batch ticket) has reached the read station, it performs a normal read, reporting Batch Ticket in the result. The data record from the batch ticket is valid and the user program must pocket-select the batch ticket. Errors and conditions are reported as with a normal document. The control will accept a new operation at any time, but will not execute a Read, Pocket Light, or Batch Count operation until a 350-millisecond period elapses after the feeder is turned off.

Second Operation Complete Bits

On a Read operation, bit 16 is not set by RSC-2 to tell the I/O Driver not to link to the next descriptor until pocket selection has been issued. The I/O Driver itself sets bit 16. All other operations set both bit 0 and bit 16 upon completion.

Control ID

On a Test operation, bits 17-23 are set to @14@.

Terminate Linking

Bit 23 is set in the RS field to indicate that descriptor linking is to be terminated because Not Ready, Too Late to Read, Jam, Missort, or Batch Ticket are on or the H (halt) variant is set (1). Pocket selection is required for Batch Ticket or H=1.

Control Behavior Under Multiple Exception Conditions

For any one or more of Jam, Not Ready, Too Late to Read, or Missort, the user program must not issue pocket selection information and RSC-2 will not restart the feeder. Any other simultaneous report, including Double Document, has no effect.

Not Ready is always reported at the same time as Jam. It also will be reported concurrently with Double Document, Too Late to Read, Halt, Batch Ticket, or Missort if the reader-sorter is not ready when the result is returned.

Batch Ticket and/or halt can be reported at the same time as Double Document. The control halts the feeder, clears the document path, waits 350 milliseconds, and sends the data and result. Invalid pocket select information must be sent to the control, which will not restart the feeder.

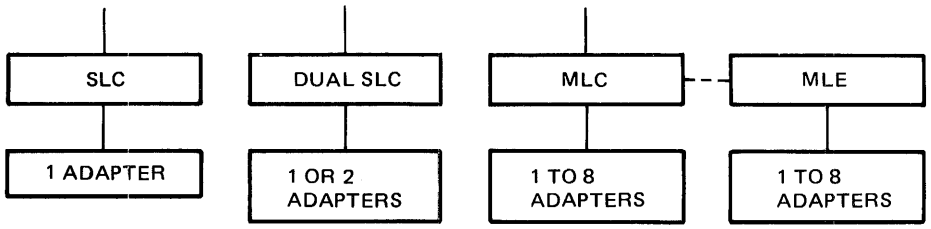
Unencoded Document or Cannot Read are mutually exclusive phenomena which may be reported with Double Document. The handling is identical to that for Double Document alone.

DATA COMMUNICATIONS SUBSYSTEM

Introduction

Two types of data communications controls are available for use in B 1800 systems, a Single Line Control (SLC) and a Multi-line Control (MLC). Both types operate with all defined B 1800 adapters, can answer the phone on Read, Write, or Test operations, and can translate EBCDIC to or from ASCII, as defined in Appendix B. Datacomm subsystem configurations are shown in figure 6-15.

As the figure shows, there are two versions of the SLC. These can be considered functionally identical; differences are noted where appropriate. Also, the multi-line extension (MLE) can be used with the MLC; this does not affect the discussion of the MLC.



G15026

Figure 6-15. Data Communications Subsystem Configurations

Single Line Control

A SLC with one adapter services one data communications line. It provides two 13-byte buffers which cyclically hold data during data transfer operations. Data is transferred to or from the system in an 8-bit parallel manner. A data loss due to unavailability of a buffer is flagged as a memory access error.

The following basic functions are provided by the SLC:

1. Interface to I/O Driver routines.
2. Data buffering.
3. Reference Address storage for an adapter.
4. Initiation of an adapter to an appropriate operating mode.
5. Servicing of adapters requesting data transfer.
6. ASCII/EBCDIC translation if selected.
7. Result status handling.
8. Automatic polling (auto poll; not included with dual SLC).

It is recommended that the B address in the I/O Descriptor contain precisely the number of characters to be transferred, due to the fact that some units can respond to a poll or acknowledgment within one millisecond. Because data is transferred to the adapter until the B address is reached, a break character such as ETX stops the adapter from transmitting data, but, until the B address is reached, the adapter cannot go into Read mode.

Data is transferred from the control to the adapter in 8-bit parallel fashion. Six system clocks are required to service an adapter.

The interface between the I/O subsystem and the SLC differs little from other B 1800 I/O interfaces. A linked chain of I/O Descriptors is initiated in sequence. If the first two bits of a given descriptor are not 00, implying that the descriptor is not yet ready to initiate, a Pause operation is initiated to the SLC. The same descriptor is re-examined. An identical process applies to completed operations.

A new initiate can be handled only when the SLC is at Status Count 1. Should the control be at any other status count, it will be cleared by the I/O Driver with a Test-and-Clear command before the new operation is initiated. A Test-and-Clear command will not disconnect a dial-up telephone line.

Multi-Line Control

An MLC can service eight communication lines (sixteen with an MLE). One adapter per line is required, and any adapter may be plugged into any of the 16 MLC adapter positions. The MLC differs from the SLC and all other B 1800 controls in that it can directly access memory through a port interchange. (The port interchange is required with MLC subsystems.) A maximum of two MLCs are permitted on a B 1800 system. Consequently, one B 1800 can service as many as 32 communication lines.

The MLC employs scanning to detect an adapter requesting service. The time required to so service an adapter varies according to the number of adapters simultaneously requesting service and the position of the request line relative to the scanning pointer. Approximately 32 clock pulses are required to scan 16 adapters without servicing. Servicing requires 2 to 10 clocks. The average time to detect and service an adapter requesting attention is 24 clocks.

The MLC provides one character of buffering in addition to the one character accumulated by the buffer in each adapter. It employs a scanning algorithm in servicing memory accesses for the buffers in the control, and data is stored or fetched 8 or 16 bits per access. Memory accessing can occur at a maximum rate of once every 8 microseconds except during data transfer. The MLC takes 7 clocks to transfer the first character into memory, but only one clock per character is needed for the next six characters. This procedure is repeated for the length of the message. An adapter's status can be accepted at any time, because the Result Descriptor is not stored in the data buffer.

A synchronization flip-flop in the Port Interchange must be strapped in to run the MLC. The following functions are provided in the MLC:

1. I/O initiate handling.
2. I/O Descriptor fetch for an adapter.
3. Storing of Link, A, and B Addresses for an adapter.
4. Initiation of adapters to appropriate operating modes.
5. Servicing of adapters requesting character transfer.
6. ASCII/EBCDIC translation if selected.
7. Result status handling.
8. Interrupt handling.
9. Linking.
10. Automatic polling (auto poll).

MLC initiation is caused by receipt of an interrupt indicating that a 24-bit message pointing to the RS field of an I/O Descriptor is present at absolute memory location zero. The MLC fetches this address via a Read-and-Clear operation which zeroes out the 24-bit field (termed the "GISMO DISPATCH" word) for later use. The adapter specified in the op code field is given control of the descriptor fetched by the MLC. This descriptor must be ready for operation.

Following execution of this initial descriptor, additional linked descriptors are initiated if ready (Bit 0=0). A locked descriptor (Bit 0=1) causes pauses of 8 to 10 milliseconds to idle the control until that descriptor is ready to execute. When the descriptor is ready, the remainder of the descriptor is fetched and normal execution commences.

The fact that the MLC is capable of handling more than one adapter affects exception handling:

1. An exception condition causes the MLC to go idle for the adapter involved after returning the result and an interrupt.
2. A Stop op code received by the MLC causes the MLC to return the result (and the interrupt, if requested) and go idle for that adapter only. All adapters must be idle before the MLC itself goes idle.
3. A memory parity error during a fetch of any field of an I/O Descriptor or during the Read-and-Clear of the GISMO DISPATCH word causes an interrupt to Port 0, Channel 15 consisting of the address+24 at the error field. The MLC then halts.

A control will accept all I/O initiations directed to it regardless of state. Directing an I/O initiate to a busy control destroys all traces of the in-process operation including a pending interrupt, and forces the control to commence the new operation.

Should the MLC be servicing a Write interrupt, it can back off and service either a normal memory access request or a Read-and-Clear operation whenever the INCN (Interrupt Conditions) register is marked as locked. This can be done only when the lockout bit is is true, but before the memory cycle has been granted.

Line Adapters

The character-oriented line adapters that have been released for use in the B 1800 series data communications subsystem are listed in table 6-16.

Table 6-16. B 1800 Data Communications Adapters

Standard Line Adapters
Standard Direct Asynchronous (STD/DIR)
Standard Synchronous (STD/SYNC)
Standard Asynchronous (STD/ASYNC)

Teletype ® Line Adapters
Teletype Asynchronous (TTY/ASYNC)
Teletype Direct Asynchronous (TTY/DIR)

Binary Synchronous Communications Line Adapters
EBCDIC Bisynchronous (BISYNC/EBCDIC)
Wideband Bisynchronous (BISYNC/WIDEBAND)

Automatic Dial Out Adapter
Automatic Calling Unit (ADO-801)

All these adapters operate in half-duplex mode. An adapter accumulates one character of data following which a delay of 14 to 17 microseconds occurs for internal functioning before service is again requested from the control. An adapter must perform character assembly, timing checks, character and block parity checks and generation, and other logical operations.

Standard Line Adapters

Standard line adapters allow attachment of the terminals and terminal series listed in table 6-17.

Table 6-17. Terminals For Use With Standard Line Adapters

TC500	TD700	TT102	TU500/TU910	S1000
TC700	TD800	TT142	TU700/TU910	S1200
TC3500			TU500/DC140	
TC4000			TU700/DC140	
TC5100				

Transmission corresponds to the ASCII-7 1967 code. Seven data bits are transmitted, least significant bit first, followed by a parity bit to make even parity for asynchronous operation and odd parity for synchronous operation. In asynchronous transmission these eight bits are firmed by a start bit (space) of zero polarity and a stop bit (mark) of one polarity.

A Block Check Code (BCC) and its parity bit are normally transmitted after the Ending Code of any message with a Start Code. This BCC is formed by taking the sum modulo 2 on each data bit

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after the Start Code, including the Ending Code. The Burroughs Field Engineer can suppress this feature if it is not desired.

For all adapters except Binary Synchronous, either EBCDIC or ASCII-8 codes can be accepted from the system on a Write. EBCDIC is translated to ASCII-8 by the control. The adapter, by ignoring the high-order bit, translates the ASCII-8 to the required ASCII-7 code. Conversely, ASCII-7 is translated to ASCII-8 by the adapter on Read, following which the control can translate to EBCDIC if so requested by the appropriate op code variant.

The STD/DIR line adapter requires no data sets. An initial timeout of either 1.2 or 2.5 seconds may be wired into the adapter, defining the time within which a data character must be received if it is not to be considered absent. A timeout of 1.2, 2.5 or 20 seconds may likewise be wired to specify the period during which further data characters are receivable. Both timeout features may be programmatically inhibited, although not individually. Direct adapters can be strapped for Write delays of 0, 3, 15, and 63 milliseconds to allow response time for remote units.

The STD/~~ASYNC~~ DIRECT line adapter permits a direct two-wire interface length of up to 1000 feet (305 meters). This adapter has a source capacity of 420 milliamperes and a sink capacity of 80 milliamperes, both while processing a logical zero. Transmission speeds of 150, 300, 1200, 1800, 2400, 4800, or 9600 bits per second are selectable by the Burroughs Field Engineer.

Operation with data sets is provided by the STD/SYNC and STD/ASYNC (non-direct) line adapters. A Read timeout of 1.2 or 2.5 seconds can be wired into the adapter, and may be programmatically inhibited. The Write delay period can be wired as either zero or any desired period between 81 and 192 milliseconds. (This is not true for wire-wrapped versions of the STD/SYNC adapter.)

Non-direct adapters permit either two-wire or four-wire operation. In two-wire usage, a squelch circuit is enabled to prevent the reflected data from being mistaken for receive data. Duration of squelch after line turn-around is 63 milliseconds for the STD/SYNC adapter and 127 milliseconds for the STD/ASYNC adapter.

If Clear-to-Send or Data-Set-Ready is not received within 20 seconds after Request-to-Send is transmitted, the non-direct adapters time out.

A controlled/continuous carrier option allows elimination of the Request-to-Send/Clear-to-Send delay in four-wire connection. Data sets must in this mode be strapped to controlled/continuous mode, with the adapter strapped for Request-to-Send. Continuous-carrier mode is invalid for two-wire connections which require controlled-carrier mode.

The STD/SYNC adapter allows connection of the terminals tabulated in table 6-17 with dial service (DDD) at 2000 2400? baud or leased line service at 600, 1200, 2400, 4800, or 9600 baud. The standard RS-232-C interface is used, and clocking is supplied by the data set.

Likewise, the STD/ASYNC adapter provides for connection of the listed terminals with a RS-232-C interface. Speeds of 150, 300, 600, or 1200 baud for dial (DDD) service or 150, 300, 600, 1200, or 1800 baud for leased line service can be selected by the Burroughs Field Engineer.

Teletype Adapters

The Teletype Asynchronous Adapter (TTY/ASYNC) and Teletype Direct Asynchronous Adapter (TTY/DIR) allow connection of the data set cable or direct line cable of Teletype 33, 35, or 37 teletypewriter terminals or their equivalents. TTY/ASYNC also permits attachment of a TWX station. The Burroughs Field Engineer can wire the various options summarized in table 6-18.

Table 6-18. Field Strappable Options for TTY Adapters

Option	ASYNC	DIR
Switched/leased line selection	yes	no
One/two stop bits (for TTY Model 37/Models 33,350	yes	yes
Speed selection 110/150/300 bps (for TTY Models 33,35/Model 37/all models)	yes	yes
811 disconnect on EOT/disuse (with TWX)	yes	no
Zero/225-ms. delay after Clear-to-Send (for 81183,81184/81181,81182 with TWX)	yes	no
Long/short receive and transmit break (for late Model 37/all others)	yes	no

yes, strap option present; no, strap option not present

Transmission corresponds to the USASCII-7 1967 code, with the least significant of seven data bits transmitted first. An even parity bit follows the seventh data bit. Parity checking may be specified with an appropriate variant in the op code, allowing compatibility with adapters generating odd parity or no parity at all. Each character is framed by a start bit of logical zero and a stop code of one or two logical ones (depending on the particular device).

Teletype line adapters have approximately 14 to 17 microseconds less than one character time to handle a character before data loss of the next character occurs.

TTY/ASYNC adapters provide an RS-232-C interface to Teletype terminals at rates of 110, 150, or 300 baud. or their equivalents.

With a TWX terminal and 811 Auxiliary Data Set, the TTY/ASYNC adapter may be strapped to disconnect (turn off Data-Terminal-Ready) upon receiving an EOT; otherwise, it disconnects after extended inactivity. In a TWX network, EOT causes the remote terminal to hang up. After transmission of the EOT, a disconnect operation must be initiated within 100 milliseconds. Therefore the Write descriptor is normally linked to a Break descriptor with the disconnect variant set.

When using a TWX terminal with a 811B1 or 811B2 Auxiliary Data Set, the adapter must be wired for a 225-millisecond delay after receiving a Clear-to-Send signal; with 811B3 or 811B4 Auxiliary Data Sets, a zero delay must be selected.

On dial lines or leased lines, a Teletype 198420 coupler is required for voltage interface between the terminal and the WE103 data set.

When using TTY/ASYNC with a late Model 37 Teletype, the adapter must be wired for long receive (255 msec) and transmit (486-567 msec) breaks. The early Model 37 Teletypes require short breaks (127 msec receive, 255 msec transmit).

TTY/ASYNC provides a 20-second Read timeout period to detect the absence of data characters. The timeout period commences upon receipt of the op code and can be programmatically inhibited. A non-inhibitable Write timeout occurs if no Clear-to-Send is received within 20 seconds of a Write initiation.

The TTY/DIR line adapter provides current for a standard 20-milliampere terminal loop interface. A 1000-foot (305 meter) cable is permitted, and 110-, 150-, or 300-bps capability can be wired into the adapter. A 600-msec transmit break and an 11-bit receive break time are characteristic of TTY/DIR. Likewise, a 40-second Read timeout period begins after I/O initiation and can be programmatically inhibited.

Binary Synchronous Line Adapters

The BISYNC/EBCDIC and BISYNC/WIDEBAND adapters permit connection of any terminal compatible with the character-oriented line discipline, using the common carrier services and data sets enumerated in tables 6-19 and 6-20.

When in Receive mode before synchronization, a four-second absence of two contiguous SYN characters is detected by a BISYNC adapter. This timeout period can be shortened to one second with an op code variant, allowing timeout to be considered a negative response. The four-second timeout can be programmatically inhibited; the one-second timeout cannot be.

A non-suppressable 20-second timeout period occurs if Clear-to-Send or Data-Set-Ready is not returned within 20 seconds of Request-to-Send.

Transmission is EBCDIC (transparent) data. Data is transmitted in eight-bit groups, least significant bit first, with no parity. Bisynchronous adapters have approximately 14 to 17 microseconds less than one character time to process a character before data loss occurs.

BISYNC/EBCDIC provides an RS-232-C interface usable with two-wire or four-wire operation. In two-wire switched line operation, a 96-ms squelch time option protects the input data line against reflections following line turn-around. As zero squelch delay can also be strapped.

Strapping BISYNC/EBCDIC for leased-line operation turns on a Data-Terminal-Ready signal. Request-to-Send can be similarly strapped, allowing data set turn-around time to be eliminated in four-wire (only) operation. Request-to-Send is true only when the telephone is off hook and a Write operation is active. Request-to-Send cannot be enabled in all off-hook conditions. Write delay times of 4, 32, or 128 milliseconds can be wired to assure proper remote unit operation.

In summary, the Burroughs Field Engineer can select the following options:

1. Switched/leased line operation.
2. Squelch period enable/disable.
3. Two/four-wire operation.
4. Controlled/continuous carrier.
5. With/without new sync control.
6. Check/no check for pad after control code on Read.
7. 4/32/128 millisecond Write delay time.
8. Zero squelch delay.

Table 6-19 enumerates common carrier services and data sets usable with the BISYNC/EBCDIC adapter.

Table 6-19. Data Sets and Services; BISYNC/EBCDIC Adapter

Speed (bps)	Service	Data Sets
600,1200,2400	—	Datel 7 V.26
2000	Dial (DDD)	WE201A3
2400	Leased	WE201B3, WE201B1; TA734/24, TA774/24
3600,7200,9600	Leased	—
4800	Leased/Switched	WE208, TA733/48, TA773/48

Speeds of 19,200 and 50,000 bits per second are permitted with the BISYNC/WIDEBAND adapter, as noted in table 6-20.

Switched or leased-line operation is wired by the Burroughs Field Engineer. For switched, Request-to-Send may be strapped to be true whenever the phone is off-hook or when the phone is off-hook and a Write operation is active. When leased-line operation is selected, Data-Terminal-Ready and Request-to-Send are both turned on.

EBCDIC/WIDEBAND has zero Write delay and zero squelch time.

The options selectable by the Burroughs Field Engineer are summarized below:

1. Switched/leased line operation.
2. Check/no check for pad after control code on Read.
3. Request-to-Send true always when phone off-hook, or phone off-hook and Write operation active.

Table 6-20. Data Sets and Services; BISYNC/WIDEBAND Adapter

Speed (BPS)	Service	Data Sets
19200	Leased	WE303
50000	Leased/Dataphone 50 (switched)	WE303

Automatic Dial Out Adapter

The Automatic Dial Out (ADO) adapter provides an RS-366 interface to as many as four Bell Series 801 Automatic Calling Unit (ACU) data sets, one of which may be replaced by a Burroughs data set with automatic dial-out (ADO) capabilities. The adapter can be busy with only one data set at a time; the ADO data set provides dial-out capability for one switched-line adapter. When attached to the SLC, the ADO adapter and its associated line adapter both use the control, necessitating a variant in op codes to select one or the other. The ADO adapter occupies one position in the MLC.

The ADO adapter receives an 8-bit character on each data transfer, but only the four low-order bits are used for dialing. If these four bits are @F@ or @C@, a 3-second pause is initiated by the adapter before the next character is requested from the control. This pause character is ignored in the sense of being an actual dialing digit; it is used for those sites in which a switching delay is necessary in obtaining an "outside" line and receiving a new dial tone.

Some ADO adapters have no circuitry to detect the answer-back tone from a called station. An End-of-Number (EON) code is necessary to end dialing and to transfer the communications lines to the associated data set. Conversely, some data sets do not generate the answer-back tone. In either case, the adapter can be wired to transfer the @C@ EON code to the data set, additionally causing a 20-second delay before returning a Dial operation Result Descriptor. This allows completion of the phone connection before any Read or Write operation is initiated. It is preferable, however, to use answer-back data sets and answer-back-detecting ADOs to absolutely assure a completed connection. Whether or not EON is wired in, the adapter must have Data-Terminal-Ready true, through use of a variant in the Test operation, in order that the ADO provide the communication line.

The ADO adapter provides a 320-millisecond delay between dial operations to allow the exchange to properly clear after a call. A timeout occurs if a call is not completed within 60 seconds of transferring the last dial digit to the ADO.

Upon returning an "abandon call, try again" or timeout from the ADO adapter, Data-Terminal-Ready must be false for a Burroughs data set; the false condition is also recommended for 801 units to avoid accidentally answering a call. This is accomplished by a Break-Disconnect operation.

Result Reporting

Operations are not terminated for any adapter upon detection of a parity error or BCC error; the exception condition is reported after normal operation termination. Likewise, a memory access error does not terminate an operation, although at least one character will be lost on a Read operation. Should the access error occur on a Write, a transmission of synchronizing characters (SYN in non-transparent mode and DLE-SYN sequences in transparent mode) occurs on synchronous lines and a constant marking condition occurs on asynchronous lines. No data is lost. An adapter attached to the SLC is not notified of memory parity errors and terminates normally. If attached to an MLC, termination may be normal, or a bad BCC or abort code (for bisynchronous adapters) may be forced. Loss of carrier is flagged in the Result Status field but does not terminate the operation. Should this occur during the receipt of data, a timer of approximately one second is initiated. If the carrier returns in this period, operation continues with the carrier loss flagged in the RS field. Only if the carrier fails to return does the operation terminate, with Timeout and Loss-of-Carrier exception bits set in the RS field.

Data-Set-Ready absent at the start of a Write operation (non BISYNC/WIDEBAND) or loss of this signal during the operation causes termination, with the problem flagged in the RS field. BISYNC/WIDEBAND reports the condition only after a 20-second timeout period, and also reports the timeout. No adapter reports a temporary loss of Data-Set-Ready between two operations. Standard adapters generate the Data-Terminal-Ready before returning a Read or Write result.

Receipt of a Break from a terminal during a Write operation causes the adapter to terminate the operation and report Break-Received in the RS field.

It is possible for an adapter to be instructed to terminate before an Ending Code is received. A bit is returned to the control in this case meaning "Ending Code expected but not received" and the control flags this condition in the Result Status field. The I/O Driver itself generates this bit when an SLC is terminated after the Ending Code is received but not yet transferred to the system.

Operations

Operators (op codes) applicable to the SLC and MLC are listed below. Variant definitions are provided within the discussions of the individual operators, in the subsections that follow. The variant UUUU identifies the specific adapter to which the operation is directed. (UUUU is ignored by the SLC.)

Data Communications Operation Codes

	← 0(MSB) 23(LSB) →					
READ	0000	TADX	CEVV	P000	0000	UUUU
WRITE	0000	TD0W	0EAA	PLLL	L000	UUUU
BREAK-DISCONNECT	1100	00VX	AB00	0000	0000	UUUU
TEST	100V	ODMI	0000	0000	0000	UUUU
ADO-TEST	1000	0D0W	00AA	0000	0000	UUUU
STOP	1100	0000	0000	0000	0000	UUUU
PAUSE	1110	0000	0000	0000	0000	0000

Read

Data from a remote device is read from the location specified by the A address to the location specified by the B address minus 1, unless terminated earlier by an Ending Code. Variants are defined as follows:

T Translation Variant.
0 No translation.
1 Translate ASCII to EBCDIC.

A ADO adapter designation.
0 No ADO adapter.
1 ADO adapter; SLC only. (Ignored by MLC.)

D All timeout functions are disabled if D=1.

C If C=1 and no data is received during timeout period, the operation is completed without a timeout exception. This allows an absent terminal to be polled without the Operation-Complete bit being set in the Result Descriptor. For TTY devices only, C=1 causes character parity to be checked.

E If E=1, EOT is ignored as a response code (Standard and Bisynchronous adapters only), and (TTY only) CR is accepted as a valid Ending Code.

VV Linking variant.
00 Normal linking and fetch of the next descriptor takes place.
01 If a non-negative response is received, the Linking-Terminated bit in the Result Descriptor is set and linking is terminated. Thus, linking continues only on a negative response, such as NAK.
10 Linking is terminated as above, but for a non-positive response; for a positive response such as ACK or ENQ, linking continues.
11 Undefined.

P Auto poll variant. If set (P=1) and no exception has been received, a Result is not stored. Instead, the next I/O Descriptor is fetched. If an exception condition exists, the operation is terminated normally (data and the Result are stored), but linking does not take place and the next I/O Descriptor is not fetched. TTY adapters ignore this variant.

Write

Data is written to the remote device from the memory location specified by the A Address to the location specified by the B address minus 1 unless terminated by an Ending Code.

T Translation variant. (As above.)

D Dial variant. If D=1, the SLC directs the operation to the ADO in order to dial a switched line.

W If W=1, the ADO adapter simulates normal ADO handshaking routines and executes a normal dial operation. A Result is returned designating which ADO unit was selected, the type of ADO unit (801 or Burroughs – if AA=00), and four bits of data. Should the adapter be strapped for a Burroughs data set, data, except @C@ or @F@, will be returned as @1@. Otherwise, data returned will have the value of the least significant four bits of the last byte of data received by the adapter.

The ADO unit must be powered off or disconnected from the ADO adapter to allow successful execution of this variant.

E If E=1, EOT is ignored as a valid response code. (Valid for non-TTY adapters only.)

AA ADO unit number 0 to 3. (Recognized by ADO adapter.)

P If P=1, non-TTY adapters are directed to write (poll) starting at the E location.

LLL Length (2 to 13) in bytes of the Poll address sequence for each terminal when P=1. (Ignored by MLC.)

Break-Disconnect

This operation terminates an in-process operation and, depending on the setting of the V variant, transmits a Break to the given remote terminal (V=0) or disconnects (V=1). This is valid for non-ADO adapters only. A Break is defined as the continuous transmission of spaces for durations specified in table 6-21.

V=0

V=1 Disconnect but do not send Break signal.
AB Reserved for diagnostics.

Binary synchronous adapters ignore V and act as if it V=1. Non-switched adapters send a Break and disconnect if V = 1.

The STD/DIR adapter immediately returns a result; all other standard adapters return a result after failing to receive data for the strapped period (1.2 or 2.5 seconds) after transmission of the Break signal. BISYNC adapters return a result one second after turning off Data-Terminal-Ready.

Table 6-21. Break Signal Durations

Adapter	Signal Duration	
	Transmit	Receive
STD/DIR	32 bits	10 bits
STD/SYNC, STD/ASYNC	255 ms	10 ms
TTY (with late Model 37)*	486-567 ms	255 ms
TTY (with all other models)*	255 ms	127 ms
TTY/DIR	600 ms	11 bits

* Strapped according to Teletype model.

Test (Line Adapters)

The adapter is tested for identity and various conditions. If D=1, the SLC directs the Test operation to the ADO adapter. The V, M, and I variants are defined below.

VMI

000 The operation is to be completed normally and the Data-Terminal-Ready signal is not affected.
001 Undefined.

010 Data-Terminal-Ready is made true and the operation is completed.
011 Undefined.
100 The adapter waits until a switched line is ringing and then completes the operation. The operation will never complete if the line is non-switched.
101 Reserved.
110 Data-Terminal-Ready is made true; Data-Set-Ready must go true before the operation will complete (switched lines only). Two-wire-direct lines wait forever; leased lines complete immediately.
111 Undefined.

Issuance of a Test operation with M=1 is mandatory before dialing; either automatic or manual, so that the ADO unit or dialer can switch the communications lines. A Test operation with V=1 and M=1 is the only method of answering a phone.

Test (ADO Adapters)

D=1 Directs the operation to the ADO adapter (SLC only.)

W=1 Identify Adapter. Instead of returning the ADO identification number, the unit number of the switched line adapter associated with the ADO selected by the AA variant and the power-up status of the ADO is returned. The adapter number, if zero, is valid only if the ADO is connected and powered on.

AA ADO unit number 0-3 (recognized by ADO adapter). For the SLC, this variant must be 00.

Stop

The Multi-Line control goes idle for the adapter specified by UUUU The adapter ID is first stored in the Result Status field and an interrupt is signalled if so requested. Other adapters are not affected.

The I/O Driver traps the Stop operator for the SLC; it simulates the idle and stores only bits 0 and 16 in the RS field.

Pause

A Pause operation is sent by the I/O Driver to the SLC when a non-ready descriptor is encountered. SLC returns a Service Request after 7 to 8 milliseconds, with bit 16 reset in the result. Results with the MLC are defined by the Stop operator in the preceding paragraph.

Table 6-22. Result Descriptor, Data Communications Subsystem

	ops R W T S B	Significance	adapters S T B A
0	X X X X X	Operation complete.	X X X X
1	X X – X X	Exception; bits 2-15 (any) set.	X X X –
1	– X – – –	Exception; bits 5, 6, 11, 12 (any) set.	– – – X
2	– – – – –	Reserved.	X X X –
2	– a – – –	Bit 7 of echo data from ACU adapter.	– – – X
3	X – – – –	Character parity of BCC error.	X X X –
3	– a – – –	Bit 3 of echo data from ACU adapter.	– – – X
3	– – – – –	Reserved.	
4	X – – – –	Memory access error.	X X X –
4	– – – – –	Reserved.	– – – X
5	X – – – –	Memory parity error.	X X X X
6	X X – – –	Timeout.	X X X –
6	– b – – –	Timeout. (Call not completed in 60 sec; timer reset after each digit to ACU.)	– – – X
7	– X – – –	Break received.	X X – –
7	– – – – –	Reserved.	– – X X
7	– X – – –	Frame aborted (Memory parity error or memory access error or TLS error.)	– – – –
8	X X – – –	Ending Code expected, not received.	X X X –
8	– c – – –	With bit 9, tells data set ACU is strapped for: –– (See bit 9.)	– – – X
8	X – – – –	Long record.	– – – –
9	d – – – –	Linking terminated.	X X X –
9	– c – – –	(With 8) 01 = WE801; 10 = Burroughs.	– – – X
10	– – – – –	Reserved.	X X X –
10	– a – – –	Bits 10, 13, 14 = 000, AA = 0; 001, AA = 3; 010, AA = 2; 100, AA = 1.	– – – X
10	X – – – –	New frame error.	– – – –
11	X X – – X	Loss/initial absence of Data Set Ready.	e X X –
11	– a – – –	Bit 2 of echo data from ACU adapter.	– – – X
11	– b – – –	WE801: Abandon call and re-dial. (Call not completed in time as strapped: 7, 10, 15, 25, 40 seconds.)	– – – X

Table 6-22. Result Descriptor, Data Communications Subsystem (Cont)

	ops R W T S B	Significance	adapters S T B A
12	X – – – –	Loss of carrier.	e X X –
12	– X – – –	Loss of Clear to Send.	e X X –
12	– a – – –	Bit 0 of echo data from ACU adapter.	– – – X
12	– b – – –	Associated line in use. (WE801 ACU: DATA LINE OCCUPIED already true. Burroughs ACU: DATA TERM READY = false.)	– – – X
12	– – – – –	Reserved.	– – – –
13	– – – – –	Reserved.	X X X –
13	– a – – –	See bit 10.	– – – X
14	– – – – –	Reserved.	X X X –
14	– a – – –	See bit 10.	– – – X
15	– – – – –	Reserved.	X X X X
16	X X X X X	Operation complete.	X X X X
17	– – X X –	Datacomm control presence.	X X X X
18	– – X X –	Non-switched (0)/switched (1) line.	X X X X
19	– – X X –	Adapter ID, see table 6-23.	X X X X
20	– – X X –	Adapter ID, see table 6-23.	X X X X
21	– – X X –	Narrowband (0)/Wideband (1).	X X X X
22	– – X X –	Adapter ID, see table 6-23.	X X X X
23	– – X X –	Adapter ID (always 0).	X X X X

ops: R = Read, W = Write, T = Test, S = Stop, B = Break-Disconnect
adapters: S = STD, T = TTY, B = BISYNC, A = ADO

a - variant W = 1 b - variant W = 0 c - variants WAA = 100
d - variants VV = 00 or 01 e - non-direct adapters only

Table 6-23. Adapter Identification Key

	Bit State							
	17	18	19	20	21	22	23	Adapter Type
	1	0	0	0	0	0	0	no adapter
	1	0	0	0	0	1	0	STD/DIR, STD leased
	1	1	0	0	0	1	0	STD switched
	1	0	0	1	0	0	0	TTY leased and direct
	1	1	0	1	0	0	0	TTY switched
	1	0	0	1	0	1	0	BISYNC/EBCDIC leased
	1	1	0	1	0	1	0	BISYNC/EBCDIC switched
	1	1	0	1	1	1	0	BISYNC/WIDEBAND leased
	1	0	0	1	1	1	0	BISYNC/WIDEBAND switched
	1	1	0	0	0	0	0	ADO adapter (switched)
W*	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**Significance for ADO Adapter**
0	1	0	0	0	0	0	0	Adapter not present
0	1	1	0	0	0	0	0	ADO adapter present
1	1	1	U	U	U	U	0	ADO unit power on; associated switched line adapter is unit number UUUU
1	1	0	U	U	U	U	0	ADO unit power off; associated switched line adapter is unit number UUUU

* Test variant

Descriptor Linkage Mechanisms

The normal linking process is somewhat altered in the data communications subsystem. Figure 6-16 illustrates the polling mechanism.

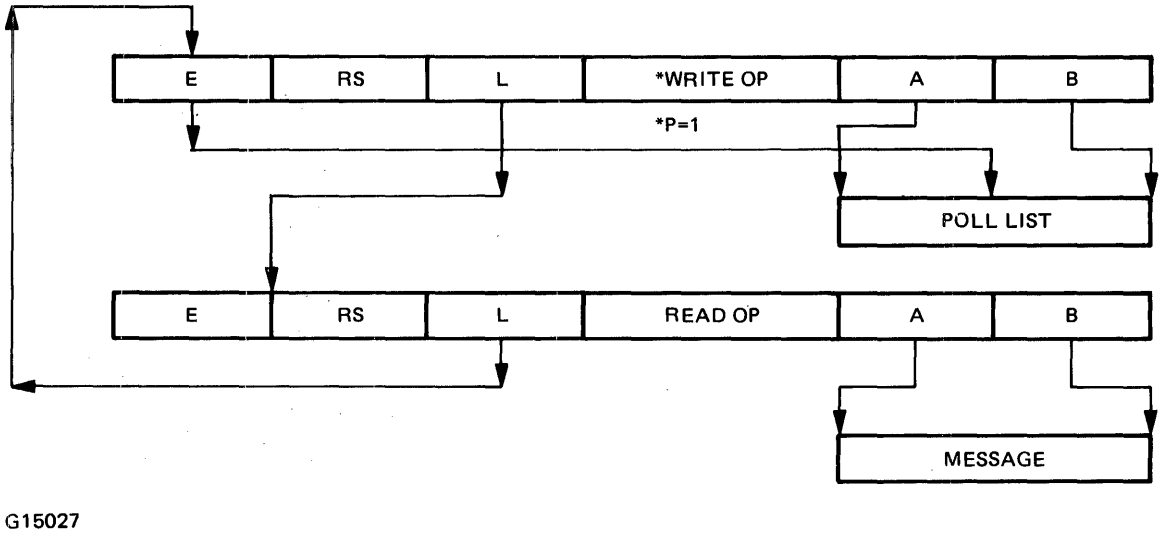

Figure 6-16. Use of Linking for Polling Operations

On a Write with P=1, the MLC uses the E address, not the A address, as a starting address when it is dispatched. E points to the poll address sequence for the next terminal due to be polled. After the poll address sequence is transmitted, the E field is updated by the MLC to point to the next item in the Poll list. If no errors are reported, bit 0 (Op complete) is reset and the next descriptor is fetched. Upon reaching the B address, implying that the poll list has been exhausted, the A address is used to continue the procedure. Upon detecting a Write error, the MLC stores the 24-bit result in the Result Status field and stops linking.

When a Write with P=1 is dispatched to an SLC, the number of bytes defined by the LLLL variant in the Op subfield is accepted. These bytes define a poll address sequence and are obtained from the E address in the I/O Descriptor. After every data transfer, the I/O Driver stores the final address (the next poll item) into E unless B is reached, in which case, the A address is substituted.

If the result information has no exceptions, the SLC suppresses bit 16 and sets bit 23; GISMO can then link to the next descriptor.

With the P variant and Link-on-Negative-Response variants set, the MLC stores data and a final address on a Read operation. If a negative response is received with no errors, bit 0 (Op complete) is reset and normal linking to the next descriptor can occur. When a non-negative response is received, MLC stores the 24-bit result into the Result Status field, sends an interrupt, and does not fetch the next descriptor. The SLC returns a result with bit 16 reset if a negative response with no exceptions is received. The I/O Driver does not store such a result, and links to the next descriptor. A negative response with exceptions or a non-negative response causes linking to end, an interrupt to be generated, and a normal result stored with Linking Terminated set.

Linking for a normal Read operation is illustrated in figure 6-17.

An exception result causes linking to terminate and an interrupt to be generated. A normal completion causes the control to link to the Write descriptor, return an ACK, and link to another (perhaps the same) Read. The Write descriptor should not be readied (Bit 0 set to 0) until a Read buffer is available.

Linking for a Write operation is illustrated in figure 6-18.

The Read operation uses a Link-on-Positive-Response variant to terminate linking when a negative response is received. The Read data should be examined before changing the Write data.

Figure 6-19 shows descriptor linking for a dialout operation.

The Test descriptor is sent to a line adapter to cause Data Terminal Ready. The Write descriptor to which the Test descriptor is linked has the D variant set, causing it to be sent to the ADO adapter. This, in turn, is linked to the desired Read or Write descriptor to cause actual data transfer.

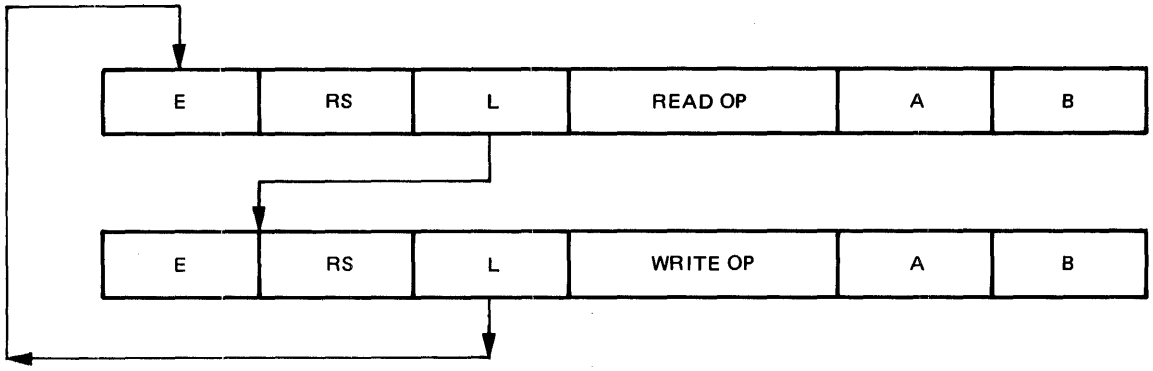

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Figure 6-17. Use of Linking for Read Operation

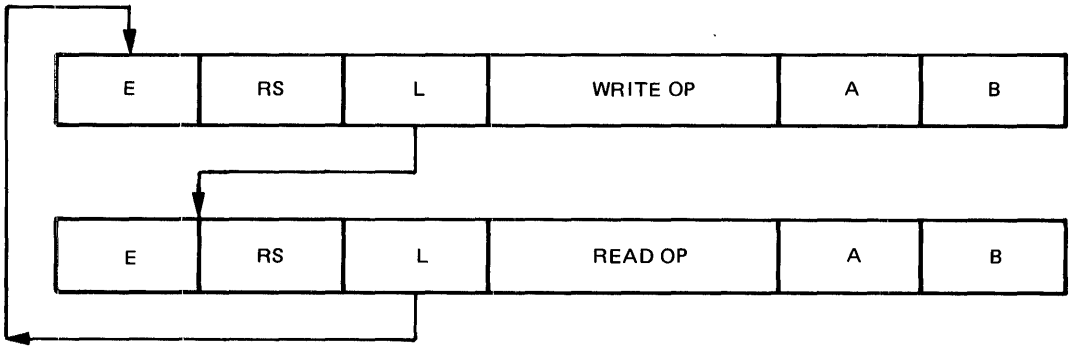

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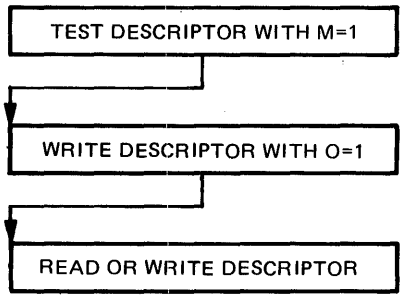
Figure 6-18. Use of Linking for Write Operation



G15030

Figure 6-19. Use of Linking for Dialing

APPENDIX A
MICROINSTRUCTION SUMMARY

Figure A-1 is a convenient reference to the formats and allowable variants of all B 1800 microinstructions. In addition (sheet 3), summaries of the meanings of bits in certain pseudoregisters and interrupt registers are included.

	MICRO NAME	MC 0	MC 1	MC 2	MC 3	MD 4	MD 5	MD 6	MD 7	ME 8	ME 9	ME 10	ME 11	MF 12	MF 13	MF 14	MF 15	VARIANTS	0 00 000	1 01 001	10 010	11 011	100	101	110	111
1C	REGISTER MOVE	0	0	0	1	REG 1 GROUP SOURCE REGISTER				REG 1 SELECT		REG 2 SELECT		REG 2 GROUP SINK REGISTER												
2C	SCRATCHPAD MOVE	0	0	1	0	REGISTER GROUP SOURCE OR SINK				REG SELECT		MOV DIR	DPW 1/2	DOUBLE PAD WORD ADDRESS				MOV DIH: 1/2 DPW:	P←R LEFT	R←P RIGHT						
3C	4-BIT MANIPULATE	0	0	1	1	REGISTER GROUP 4-BIT SOURCE AND SINK				REG SEL	MANIPULATE VARIANTS			4-BIT MANIP LITERAL				MANIP VARIANTS	SET	AND	OR	EOR	INC	INC TEST	DEC	DEC TEST
4C	BIT TEST REL BRANCH FALSE	0	1	0	0	REGISTER GROUP 4-BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG				DSP SIGN:	+	-						
5C	BIT TEST REL BRANCH TRUE	0	1	0	1	REGISTER GROUP 4-BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG				DSP SIGN:	+	-						
6C	SKIP WHEN	0	1	1	0	REGISTER GROUP 4-BIT SOURCE AND SINK				REG SEL	SKIP TEST VARIANTS			4-BIT TEST MASK				SKIP TEST VARIANTS	ANY CLR/	ALL CLR/	EOL CLR/	ALL CLR	ANY/ CLR/	ALL/ CLR/	EOL/ CLR/	ALL/ CLR
7C	READ/WRITE MEMORY	0	1	1	1	R/W VAR	COUNT FA/FL VARIANTS			DATA REG CODE		DSP SIGN		DATA TRANSFER WIDTH MAGNITUDE				READ/WRITE: DISPLACEMENT SIGN:	R LEFT	W RIGHT						
																		REG. CODE:	X	Y	T	L				
																		COUNT FA/FL UP ↑; DOWN ↓	NOP	FA↑	FL↑	FA↑ FL↓	FA↓ FL↑	FA↓	FL↓	FA↓ FL↓
8C	MOVE 8-BIT LITERAL	1	0	0	0	REGISTER GROUP REG SEL IS 2				ENTIRE 8 BITS OF 8-BIT LITERAL																
9C	MOVE 24-BIT LITERAL	1	0	0	1	REGISTER GROUP REG SEL IS 2				8 MOST SIGNIFICANT BITS OF FULL 24-BIT LITERAL																
10C	SHIFT/ROTATE T-REG	1	0	1	0	SINK REGISTER GROUP				SINK REG SELECT		S/R VAR		LEFT SHIFT/ROTATE & COUNT				S/R VAR:	SHFT	ROT						
11C	EXTRACT FROM T-REG	1	0	1	1	RIGHT BIT POINTER FOR EXTRACTION FLD						SINK REG CODE		EXTRACTION FIELD WIDTH				SINK REG CODE:	X	Y	T	L				
12C	BRANCH RELATIVE FORWARD	1	1	0	0	RELATIVE DISPLACEMENT MAGNITUDE																				
13C	BRANCH RELATIVE REVERSE	1	1	0	1	RELATIVE DISPLACEMENT MAGNITUDE																				
14C	CALL RELATIVE FORWARD	1	1	1	0	RELATIVE CALL ADDRESS MAGNITUDE																				
15C	CALL RELATIVE REVERSE	1	1	1	1	RELATIVE CALL ADDRESS MAGNITUDE																				
2D	SWAP MEMORY	0	0	0	0	0	0	1	0	DATA REG CODE		TW SGN		DATA TRANSFER WIDTH MAGNITUDE				TW SIGN: REG CODE:	+ X	- Y	T	L				
3D	CLEAR REGISTERS	0	0	0	0	0	0	1	1	L-REG	T-REG	Y-REG	X-REG	FA REG	FL REG	FU REG	CP REG									
4D	SHIFT/ROTATE X OR Y	0	0	0	0	0	1	0	0	S/R DIR VARIANT		X/Y VAR		LEFT OR RIGHT X OR Y SHIFT/ROTATE COUNT				X/Y VAR:	X	Y						
5D	SHIFT/ROTATE X AND Y	0	0	0	0	0	1	0	1	S/R DIR VARIANT		LEFT OR RIGHT, X AND Y SHIFT/ROTATE COUNT						SHIFT/ROTATE VARIANTS DIRECTION	SFT←	4D AND 5D SFT→	ROT←	ROT→				

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Figure A-1. Formats and Allowable Variants of all B 1800 Microinstructions (Sheet 1 of 3)

	MICRO NAME	MC 0	1	2	3	MD 4	5	6	7	ME 8	9	10	11	MF 12	13	14	15
6D	COUNT FA/FL	0	0	0	0	0	1	1	0	COUNT FA/FL VARIANTS				COUNT SCALAR MAGNITUDE			
7D	EXCHANGE DPW	0	0	0	0	0	1	1	1	SINK DPW ADDRESS				SOURCE DPW ADDRESS			
8D	SCRATCHPAD RELATE FA	0	0	0	0	1	0	0	0	0	0	0	SPD SGN	LEFT HALF PAD WORD ADDRESS			
9D	MONITOR	0	0	0	0	1	0	0	1	LITERAL OCCURRENCE IDENTIFIER							
10D	NANO MOVE	0	0	0	0	1	0	1	0	C/A VAR	STOPPING SEQUENCE NUMBER			NANO REGISTER WORD PORTION			
11D	DIAGNOSTIC READ/WRITE MEMORY	0	0	0	0	1	0	1	1	SOURCE REGISTER		FDS OR P.I. R/E	MBU/ P.I.	MEM/ ECHO	MEM R/W	ECHO VAR	
										X	X	0	0	0	0	0	0
										r	r	0	0	0	1	0	0
										r	r	0	0	1	0	0	1
										X	X	0	0	1	0	1	0
										X	X	1	0	1	0	1	0
										X	X	0	0	1	0	1	1
										X	X	0	1	1	0	0	0
										r	r	1	1	1	0	0	0
										r	r	1	1	1	0	0	1
										r	r	1	1	1	0	1	0
										r	r	1	1	1	0	1	1
										r	r						
										X	X						

VARIANT	0 00 000	1 01 001	10 010	11 011	100	101	110	111
COUNT FA/ FL VAF :	NOP	FA↑	FL↑	FA↑ FL↓	FA↓ FL↑	FA↓	FL↓	FA↓ FL↓
SPAD SIGN:	+	-						
CONTINUE/ABORT:	C	A						
STOPPING SEQ. NUMBER:	0/8	1/9	2/10	3/11	4/12	5/13	6/14	7/15
WORD PORTION:	0	1	2	3	4	5	6	7
SIGNIFICANCE	(ALL OTHER BIT PATTERNS ARE UNDEFINED)							
READ 22-BIT WORD (16 DATA + 6 ECC) TO Y.								
WRITE 22-BIT WORD FROM X, Y, T, OR L.								
ECHO WRITE DATA TO Y FROM X, Y, T, OR L.								
ECHO MODIFIED ADDRESS FORWARD, FA TO Y.								
ECHO MODIFIED ADDRESS BACKWARD, FA TO Y.								
READ AND CLEAR ERROR LOG (READ TO Y).								
READ PORT DATA LATCH TO Y.								
ECHO THRU PORT INTERCHANGE TO Y FROM X, Y, T, OR L.								
ECHO THRU PORT ADAPTER 1 TO Y FROM X, Y, T, OR L.								
ECHO THRU PORT ADAPTER 2 TO Y FROM X, Y, T, OR L.								
ECHO THRU PORT ADAPTER 3 TO Y FROM X, Y, T, OR L.								
SOURCE REGISTER: X Y T L								
IGNORE								

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Figure A-1. Formats and Allowable Variants of all B 1800 Microinstructions (Sheet 2 of 3)

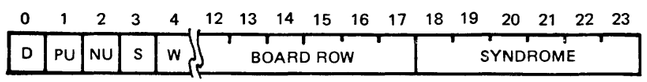
	MICRO NAME	MC 0	1	2	3	MD 4	5	6	7	ME 8	9	10	11	MF 12	13	14	15
1E	DISPATCH	0	0	0	0	0	0	0	0	0	0	0	1	DISPATCH VARIANTS			SKP FLG
2E	CASSETTE CONTROL	0	0	0	0	0	0	0	0	0	0	1	0	CASSETTE MANIP. VARIANTS			HLT=0 SKP=1
3E	BIAS	0	0	0	0	0	0	0	0	0	0	1	1	BIAS VARIANTS			TEST FLAG
4E	STORE F 1NTO DPW	0	0	0	0	0	0	0	0	0	1	0	0	SINK DPW ADDRESS			
5E	LOAD F FROM DPW	0	0	0	0	0	0	0	0	0	1	0	1	SOURCE DPW ADDRESS			
6E	SET CARRY FLIP-FLOP	0	0	0	0	0	0	0	0	0	1	1	0	CYF ← CYD	CYF ← CYL	CYF ← 1	CYF ← 0
7E	READ/WRITE CACHE	0	0	0	0	0	0	0	0	0	1	1	1	PAR-ITY	READ/WRITE VARIANTS		
1F	HALT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
3F	NORMALIZE X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4F	TRANSFER CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5F	CLEAR CACHE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6F	INC A	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7F	LOAD LAMPS	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
ZERO	NO OPERATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VARIANTS	0 00 000	1 01 001	10 010	11 011	100	101	110	111
SKP FLAG: DISP VAR:	FAIL LOCK	SUCC WRTLC	READ	R&C	WRTHI	ABSNT	UNDEF	UNDEF
CASSETTE MANIPULATE:	START TAPE	STOP AT GAP	STOP OR SKIP ON X ≠ Y	STOP OR SKIP ON FA≠BR	UNDEF	UNDEF	STOP OR SKIP ON X = Y	STOP OR SKIP ON FA≠BR
TEST FLAG: BIAS:	TEST/ UNIT	TEST F	S	FS	NO-OP	FCP	NO-OP	NO-OP
PARITY: READ/WRITE:	GOOD R	BAD E S E	R V E	D	DIAG BLKA	WRITE BLKB	READ MICRO	READ KEYS

	0	1	2	3
PERP	CACHE DOUBLE HIT	CACHE KEY PARITY ERROR ON KEY A OR KEY B	PARITY ERROR OF FETCHED MICRO IN M-REGISTER	CASSETTE ERROR NOT CORRECTABLE
PERM	S-MEMORY MICRO INSTRUCTION TIME-OUT	S-MEMORY FIELDS OUT OF ADMINIS-TRATIVE BOUNDS	S-MEMORY E-LOG REGISTER LOGGED	UNCORRECTABLE S-MEMORY ERROR IN PROC. OPS
MSSW	NULL BIT	NULL BIT	S1: MICRO SOURCE FROM CACHE OR FRO-ZEN IN M-REGISTER	S0: MICRO SOURCE FROM S-MEM OR FRO-ZEN IN M-REGISTER

INT. = ANY ONE OR MORE OF: CC0, CC1, CC2, CD0, CD3, INCN1, INCN3.

THE ERROR LOG REGISTER HAS MEANINGS AS FOLLOWS:



PU: UNCORRECTABLE ERROR ON CPU ACCESS
NU: UNCORRECTABLE ERROR ON NON-CPU ACCESS
S: SINGLE BIT ERROR (CORRECTED IN DATA OR CHECK-BIT)
D: DUPLICATE ERROR OCCURRENCE (LOGGING DATA LOST)
W: BOARD/ROW/SYNDROME LOADED ON WRITE OPERATION

NOTE: REGISTER BITS AS WELL AS MICRO INSTRUCTION BITS ARE NUMBERED ACCORDING TO HARDWARE CONVENTION. MSB IS HIGHEST-ORDER (AND LEFTMOST) BIT.

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REGISTER SELECT

REGISTER GROUP	0	1	2	3
0	TA	FU	X	SUM
1	TB	FT	Y	CMPX
2	TC	FLC	T	CMPY
3	TD	FLD	L	XANY
4	TE	FLE	A	XEOY
5	TF	FLF	M	MSKX
6	CA	BICN	BR	MSKY
7	CB	FLCN	LR	XORY
8	LA	NULL-A	FA	DIFF
9	LB	RESV	FB	MAXS
10	LC	PERM	FL	NULL-C
11	LD	PERP	TAS	U
12	LE	XYCN	CP	NULL-D
13	LF	XYST	NULL-B	DATA
14	CC	INCN	CSW	CMND
15	CD	MSSW	TIMR	NULL-E

INDIVIDUAL BITS OF SOME 4-BIT REGISTERS HAVE SPECIAL MEANINGS AS NOTED BELOW:

	0	1	2	3
BICN	LSUY	CYF	CYD	CYL
XYCN	MSBX	X = Y	X < Y	X > Y
XYST	LSUX	INT	Y NEQ 0	X NEQ 0
FLCN	FL = SFL	FL > SFL	FL < SFL	FL NEQ 0
INCN	PORT DEV. MISSING	PORT HI PRIORITY	PORT INTERRUPT	PORT LOCKOUT
CC	CONT. PANEL STATE LAMP FLIP-FLOP	REAL TIME CLOCK INTERRUPT	I/O BUS SERV. RQST INTERRUPT	CONTROL PANEL INTERRUPT
CD	MEM. READ ERROR INTERRUPT	MEM. WRITE/SWAP (LR/BR CHK) OUT OF BDS OVERRIDE	MEM. READ ADDR. (LR/BR CHK) OUT OF BDS	MEM. WRITE/SWAP (LR/BR CHK) OUT OF BDS INTERRUPT

Figure A-1. Formats and Allowable Variants of all B 1800 Microinstructions (Sheet 3 of 3)

APPENDIX B

Table B-1 is a listing of the 8-bit EBCDIC internal code together with the USASCII-7, 80-column-card, and 96-column-card codes and the associated control or special codes or graphics. Table B-2 presents similar information, restricted to and in sequence of the USASCII-7 code. Table B-3 explains all the control or special codes. Column headings have the following meanings in tables B-1 and B-2:

A EBCDIC sequence number and decimal value
B EBCDIC hexadecimal representation
C ASCII-7 sequence number and decimal value
D ASCII-7 hexadecimal representation
E 80-column card code
F 96-column card code
G Graphic or code

"Hexadecimal representation" means that standard convention is followed for the 8-bit internal codes, which are presented as pairs of hexadecimal numbers that are translated as shown in the following examples:

		8 4 2 1	8 4 2 1
8 =	@08@ =	0 0 0 0	1 0 0 0
57 =	@39@ =	0 0 1 1	1 0 0 1
190 =	@BE@ =	1 0 1 1	1 1 1 0
15 =	@0F@ =	0 0 0 0	1 1 1 1

Table B-1. B 1800 Codes in EBCDIC Sequence

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
0	00	0	00	12-0-1-8		NUL (Null)
1	01	1	01	12-1-9		SOH (Start of Heading)
2	02	2	02	12-2-9		STX (Start of Text)
3	03	3	03	12-3-9		ETX (End of Text)
4	04			12-4-9		
5	05	9	09	12-5-9		HT (Horizontal Tab)
6	06			12-6-9		
7	07	127	7F	12-7-9		DEL (Delete)
8	08			12-8-9		
9	09			12-1-8-9		
10	0A			12-2-8-9		
11	0B	11	0B	12-3-8-9		VT (Vertical Tab)
12	0C	12	0C	12-4-8-9		FF (Form Feed)
13	0D	13	0D	12-5-8-9		CR (Carriage Return)
14	0E	14	0E	12-6-8-9		SO (Shift Out)
15	0F	15	0F	12-7-8-9		SI (Shift In)
16	10	16	10	12-11-1-8-9		DLE (Data Link Escape)
17	11	17	11	11-1-9		DC1 (Device Control 1)
18	12	18	12	11-2-9		DC2 (Device Control 2)
19	13	19	13	11-3-9		DC3 (Device Control 3)
20	14			11-4-9		
21	15			11-5-9		NL (New Line)
22	16	8	08	11-6-9		BS (Backspace)
23	17			11-7-9		

Table B-1. B 1800 Codes in EBCDIC Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
24	18	24	18	11-8-9		CAN (Cancel)
25	19	25	19	11-1-8-9		EM (End of Medium)
26	1A			11-2-8-9		
27	1B			11-3-8-9		
28	1C	28	1C	11-4-8-9		FS (File Separator)
29	1D	29	1D	11-5-8-9		GS (Group Separator)
30	1E	30	1E	11-6-8-9		RS (Record Separator)
31	1F	31	1F	11-7-8-9		US (Unit Separator)
32	20			11-0-1-8-9		
33	21			0-1-9		
34	22			0-2-9		
35	23			0-3-9		
36	24			0-4-9		
37	25	10	0A	0-5-9		LF (Line Feed)
38	26	23	17	0-6-9		ETB (End of Transm. Block)
39	27	27	1B	0-7-9		ESC (Escape)
40	28			0-8-9		
41	29			0-1-8-9		
42	2A			0-2-8-9		
43	2B			0-3-8-9		
44	2C			0-4-8-9		
45	2D	5	05	0-5-8-9		ENQ (Enquiry)
46	2E	6	06	0-6-8-9		ACK (Acknowledge)
47	2F	7	07	0-7-8-9		BEL (Bell)
48	30			12-11-0-1-8-9		
49	31			1-9		
50	32	22	16	2-9		SYN (Synchronous Idle)
51	33			3-9		
52	34			4-9		
53	35			5-9		
54	36			6-9		
55	37	4	04	7-9		EOT (End of Transmission)
56	38			8-9		
57	39			1-8-9		
58	3A			2-8-9		
59	3B			3-8-9		
60	3C	20	14	4-8-9		DC4 (Device Control 4)
61	3D	21	15	5-8-9		NAK (Negative Acknowledge)
62	3E			6-8-9		
63	3F	26	1A	7-8-9		
64	40	32	20	No Punches		Space
65	41			12-0-1-8-9		
66	42			12-0-2-9		
67	43			12-0-3-9		
68	44			12-0-4-9		
69	45			12-0-5-9		
70	46			12-0-6-9		
71	47			12-0-7-9		
72	48			12-0-8-9		
73	49			12-1-8		
74	4A	91	5B	12-2-8		[(Left Bracket)
75	4B	46	2E	12-3-8	BA821	. (Period, Decimal Pt.)

Table B-1. B 1800 Codes in EBCDIC Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
76	4C	60	3C	12-4-8	BA84	< (Less-Than Sign)
77	4D	40	28	12-5-8	BA841	((Left Parenthesis)
78	4E	43	2B	12-6-8	BA842	+ (Plus Sign)
79	4F	33	21	12-7-8	BA8421	| (Vertical Bar)
80	50	38	26	12	A82	& (Ampersand)
81	51			12-11-1-9		
82	52			12-11-2-9		
83	53			12-11-3-9		
84	54			12-11-4-9		
85	55			12-11-5-9		
86	56			12-11-6-9		
87	57			12-11-7-9		
88	58			12-11-8-9		
89	59			11-1-8		
90	5A	93	5D	11-2-8		] (Right Bracket)
91	5B	36	24	11-3-8	B821	$ (Dollar Sign)
92	5C	42	2A	11-4-8	B84	* Asterisk
93	5D	41	29	11-5-8	B841	) (Right Parenthesis)
94	5E	59	3B	11-6-8	B842	; (Semicolon)
95	5F	94	5E	11-7-8	B8421	¬ (Logical Not)
96	60	45	2D	11	B	- (Minus, Hyphen)
97	61	47	2F	0-1	A	/ (Slash)
98	62			11-0-2-9		
99	63			11-0-3-9		
100	64			11-0-4-9		
101	65			11-0-5-9		
102	66			11-0-6-9		
103	67			11-0-7-9		
104	68			11-0-8-9		
105	69			0-1-8		
106	6A	124	7C	12-11		
107	6B	44	2C	0-2-8	A821	, (Comma)
108	6C	37	25	0-4-8	A84	% (Percent Sign)
109	6D	95	5F	0-5-8	A841	_ (Underscore)
110	6E	62	3E	0-6-8	A842	> (Greater Than Sign)
111	6F	63	3F	0-7-8	A8421	? (Question Mark)
112	70			12-11-0	B82	! (Exclamation Point)
113	71			12-11-0-1-9		
114	72			12-11-0-2-9		
115	73			12-11-0-3-9		
116	74			12-11-0-4-9		
117	75			12-11-0-5-9		
118	76			12-11-0-6-9		
119	77			12-11-0-7-9		
120	78			12-11-0-8-9		
121	79	96	60	1-8		
122	7A	58	3A	2-8	82	: (Colon)
123	7B	35	23	3-8	821	# (Number or Pound Sign)
124	7C	64	40	4-8	84	@ (At Sign)
125	7D	39	27	5-8	841	' (Apostrophe)
126	7E	61	3D	6-8	842	= (Equal Sign)
127	7F	34	22	7-8	8421	" (Quotation Mark)

Table B-1. B 1800 Codes in EBCDIC Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
128	80			12-0-1-8		
129	81	97	61	12-0-1		a
130	82	98	62	12-0-2		b
131	83	99	63	12-0-3		c
132	84	100	64	12-0-4		d
133	85	101	65	12-0-5		e
134	86	102	66	12-0-6		f
135	87	103	67	12-0-7		g
136	88	104	68	12-0-8		h
137	89	105	69	12-0-9		i
138	8A					
139	8B					
140	8C					
141	8D					
142	8E					
143	8F					
144	90			12-11-1-8		
145	91	106	6A	12-11-1		j
146	92	107	6B	12-11-2		k
147	93	108	6C	12-11-3		l
148	94	109	6D	12-11-4		m
149	95	110	6E	12-11-5		n
150	96	111	6F	12-11-6		o
151	97	112	70	12-11-7		p
152	98	113	71	12-11-8		q
153	99	114	72	12-11-9		r
154	9A			12-11-2-8		
155	9B			12-11-3-8		
156	9C			12-11-4-8		
157	9D			12-11-5-8		
158	9E			12-11-6-8		
159	9F			12-11-7-8		
160	A0			11-0-1-8		
161	A1	126	7E	11-0-1	BA821	¢ (Cent Sign)
162	A2	115	73	11-0-2		s
163	A3	116	74	11-0-3		t
164	A4	117	75	11-0-4		u
165	A5	118	76	11-0-5		v
166	A6	119	77	11-0-6		w
167	A7	120	78	11-0-7		x
168	A8	121	79	11-0-8		y
169	A9	122	7A	11-0-9		z
170	AA			11-0-2-8		
171	AB			11-0-3-8		
172	AC			11-0-4-8		
173	AD			11-0-5-8		
174	AE			11-0-6-8		
175	AF			11-0-7-8		
176	B0			12-11-0-1-8		
177	B1			12-11-0-1		
178	B2			12-11-0-2		

Table B-1. B 1800 Codes in EBCDIC Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
179	B3			12-11-0-3		
180	B4			12-11-0-4		
181	B5			12-11-0-5		
182	B6			12-11-0-6		
183	B7			12-11-0-7		
184	B8			12-11-0-8)		
185	B9			12-11-0-8]	should be	12-11-0-9
186	BA			12-11-0-2-8		
187	BB			12-11-0-3-8		
188	BC			12-11-0-4-8		
189	BD			12-11-0-5-8		
190	BE			12-11-0-6-8		
191	BF			12-11-0-7-8		
192	C0	123	7B	12-0		{ (Left Brace)
193	C1	65	41	12-1	BA1	A
194	C2	66	42	12-2	BA2	B
195	C3	67	43	12-3	BA21	C
196	C4	68	44	12-4	BA4	D
197	C5	69	45	12-5	BA41	E
198	C6	70	46	12-6	BA42	F
199	C7	71	47	12-7	BA421	G
200	C8	72	48	12-8	BA8	H
201	C9	73	49	12-9	BA81	I
202	CA					
203	CB					
204	CC					
205	CD					
206	CE					
207	CF					
208	D0	125	7D	11-0	BA	} (Right Brace)
209	D1	74	4A	11-1	B1	J
210	D2	75	4B	11-2	B2	K
211	D3	76	4C	11-3	B21	L
212	D4	77	4D	11-4	B4	M
213	D5	78	4E	11-5	B41	N
214	D6	79	4F	11-6	B42	O
215	D7	80	50	11-7	B421	P
216	D8	81	51	11-8	B8	Q
217	D9	82	52	11-9	B81	R
218	DA					
219	DB					
220	DC					
221	DD					
222	DE					
223	DF					
224	E0	92	5C	0-8-2		\ (Reverse Slash)
225	E1					
226	E2	83	53	0-2	A2	S
227	E3	84	54	0-3	A21	T
228	E4	85	55	0-4	A4	U
229	E5	86	56	0-5	A41	V

Table B-1. B 1800 Codes in EBCDIC Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
230	E6	87	57	0-6	A42	W
231	E7	88	58	0-7	A421	X
232	E8	89	59	0-8	A8	Y
233	E9	90	5A	0-9	A81	Z
234	EA					
235	EB					
236	EC					
237	ED					
238	EE					
239	EF					
240	F0	48	30	0	A	'0
241	F1	49	31	1	1	1
242	F2	50	32	2	2	2
243	F3	51	33	3	21	3
244	F4	52	34	4	4	4
245	F5	53	35	5	41	5
246	F6	54	36	6	42	6
247	F7	55	37	7	421	7
248	F8	56	38	8	8	8
249	F9	57	39	9	81	9
250	FA					
251	FB					
252	FC					
253	FD					
254	FE					
255	FF					

Table B-2. B 1800 Codes in ASCII-7 Sequence

EBCDIC A	EBCDIC B	USASCII-7 C	USASCII-7 D	E	F	G
0	00	0	00	12-0-1-8-9		NUL (Null)
1	01	1	01	12-1-9		SOH (Start of Heading)
2	02	2	02	12-2-9		STX (Start of Text)
3	03	3	03	12-3-9		ETX (End of Text)
55	37	4	04	7-9		EOT (End of Transmission)
45	2D	5	05	0-5-8-9		ENQ (Enquiry)
46	2E	6	06	0-6-8-9		ACK (Acknowledge)
47	2F	7	07	0-7-8-9		BEL (Bell)
22	16	8	08	11-6-9		BS (Backspace)
5	05	9	09	12-5-9		HT (Horizontal Tab)
37	25	10	0A	0-5-9		LF (Line Feed)
11	0B	11	0B	12-3-8-9		VT (Vertical Tab)
12	0C	12	0C	12-4-8-9		FF (Form Feed)
13	0D	13	0D	12-5-8-9		CR (Carriage Return)
14	0E	14	0E	12-6-8-9		SO (Shift Out)
15	0F	15	0F	12-7-8-9		SI (Shift In)
16	10	16	10	12-11-1-8-9		DLE (Data Link Escape)
17	11	17	11	11-1-9		DC1 (Device Control 1)
18	12	18	12	11-2-9		DC2 (Device Control 2)
19	13	19	13	11-3-9		DC3 (Device Control 3)
60	3C	20	14	4-8-9		DC4 (Device Control 4)
61	3D	21	15	5-8-9		NAK (Negative Acknowledge)
50	32	22	16	2-9		SYN (Synchronous Idle)
38	26	23	17	0-6-9		ETB (End of Transm. Block)
24	18	24	18	11-8-9		CAN (Cancel)
25	19	25	19	11-1-8-9		EM (End of Medium)
63	3F	26	1A	7-8-9		SUB (Substitute)
39	27	27	1B	0-7-9		ESC (Escape)
28	1C	28	1C	11-4-8-9		FS (File Separator)
29	1D	29	1D	11-5-8-9		GS (Group Separator)
30	1E	30	1E	11-6-8-9		RS (Record Separator)
31	1F	31	1F	11-7-8-9		US (Unit Separator)
64	40	32	20	No Punches		Space
79	4F	33	21	12-7-8	BA8421	| (Vertical Bar)
127	7F	34	22	7-8	8421	" (Quotation Mark)
123	7B	35	23	3-8	821	# (Number or Pound Sign)
91	5B	36	24	11-3-8	B821	$ (Dollar Sign)
108	6C	37	25	0-4-8	A84	% (Percent Sign)
80	50	38	26	12	A82	& (Ampersand)
125	7D	39	27	5-8	841	' (Apostrophe)
77	4D	40	28	12-5-8	BA841	((Left Parenthesis)
93	5D	41	29	11-5-8	B841	) (Right Parenthesis)
92	5C	42	2A	11-4-8	B84	* (Asterisk)
78	4E	43	2B	12-6-8	BA842	+ (Plus Sign)
107	6B	44	2C	0-2-8	A821	, (Comma)
96	60	45	2D	11	B	- (Minus Sign, Hyphen)
75	4B	46	2E	12-3-8	BA821	. (Period)
97	61	47	2F	0-1	A	/ (Slash)
240	F0	48	30	0	A	0
241	F1	49	31	1	1	1
242	F2	50	32	2	2	2

Table B-2. B 1800 Codes in ASCII-7 Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
243	F3	51	33	3	21	3
244	F4	52	34	4	4	4
245	F5	53	35	5	41	5
246	F6	54	36	6	42	6
247	F7	55	37	7	421	7
248	F8	56	38	8	8	8
249	F9	57	39	9	81	9
122	7A	58	3A	2-8	82	: (Colon)
94	5E	59	3B	11-6-8	B842	; (Semicolon)
76	4C	60	3C	12-4-8	BA84	< (Less-Than Sign)
126	7E	61	3D	6-8	842	= (Equal Sign)
110	6E	62	3E	0-6-8	A842	> (Greater-Than Sign)
111	6F	63	3F	0-7-8	A8421	? (Question Mark)
124	7C	64	40	4-8	84	@ (At Sign)
193	C1	65	41	12-1	BA1	A
194	C2	66	42	12-2	BA2	B
195	C3	67	43	12-3	BA21	C
196	C4	68	44	12-4	BA4	D
197	C5	69	45	12-5	BA41	E
198	C6	70	46	12-6	BA42	F
199	C7	71	47	12-7	BA421	G
200	C8	72	48	12-8	BA8	H
201	C9	73	49	12-9	BA81	I
209	D1	74	4A	11-1	B1	J
210	D2	75	4B	11-2	B2	K
211	D3	76	4C	11-3	B21	L
212	D4	77	4D	11-4	B4	M
213	D5	78	4E	11-5	B41	N
214	D6	79	4F	11-6	B42	O
215	D7	80	50	11-7	B421	P
216	D8	81	51	11-8	B8	Q
217	D9	82	52	11-9	B81	R
226	E2	83	53	0-2	A2	S
227	E3	84	54	0-3	A21	T
228	E4	85	55	0-4	A4	U
229	E5	86	56	0-5	A41	V
230	E6	87	57	0-6	A42	W
231	E7	88	58	0-7	A421	X
232	E8	89	59	0-8	A8	Y
233	E9	90	5A	0-9	A81	Z
74	4A	91	5B	12-2-8		[(Left Bracket)
224	E0	92	5C			\ (Reverse Slash)
90	5A	93	5D	11-2-8		] (Right Bracket)
95	5F	94	5E	11-7-8	B8421	¬ (Logical Not)
109	6D	95	5F	0-5-8	A841	– (Underscore)
121	79	96	60	1-8		
129	81	97	61	12-0-1		a
130	82	98	62	12-0-2		b
131	83	99	63	12-0-3		c
132	84	100	64	12-0-4		d
133	85	101	65	12-0-5		e

Table B-2. B 1800 Codes in ASCII-7 Sequence (Cont.)

EBCDIC		USASCII-7				
A	B	C	D	E	F	G
134	86	102	66	12-0-6		f
135	87	103	67	12-0-7		g
136	88	104	68	12-0-8		h
137	89	105	69	12-0-9		i
145	91	106	6A	12-11-1		j
146	92	107	6B	12-11-2		k
147	93	108	6C	12-11-3		l
148	94	109	6D	12-11-4		m
149	95	110	6E	12-11-5		n
150	96	111	6F	12-11-6		o
151	97	112	70	12-11-7		p
152	98	113	71	12-11-8		q
153	99	114	72	12-11-9		r
162	A2	115	73	11-0-2		s
163	A3	116	74	11-0-3		t
164	A4	117	75	11-0-4		u
165	A5	118	76	11-0-5		v
166	A6	119	77	11-0-6		w
167	A7	120	78	11-0-7		x
168	A8	121	79	11-0-8		y
169	A9	122	7A	11-0-9		z
192	C0	123	7B	12-0		{ (Left Brace)
106	6A	124	7C	12-11		
208	D0	125	7D		BA	} (Right Brace)
161	A1	126	7E	11-0-1	BA821	¢ (Cents Sign)
7	07	127	7F	12-7-9		DEL (Delete)

Table B-3. Meanings of Control and Special Characters

Symbol	Name/Function
NUL	Null: The all zeros character which may serve to accomplush time fill and media fill.
SOH	Start of Heading: A communication control character used at the beginning of a sequence of characters which constitute a machine-sensible address or routing information. Such a sequence is referred to as the "heading." An STX character has the effect of terminating a heading.
STX	Start of Text: A communication control character which precedes a sequence of characters that are to be treated as an entity and entirely transmitted through to the ultimate destination. Such a sequence is referred to as "text." STX may be used to terminate a sequence of characters started by SOH.
ETX	End of Text: A communication control character used to terminate a sequence of characters started with STX and transmitted as an entity.
EOT	End of Transmission: A communication control character used to indicate the conclusion of a transmission which may have contained one or more texts and any associated headings.
ENQ	Enquiry: A communication control character used in data communication systems as a request for a response from a remote station. It may be used as a "Who Are You" (WRU) to obtain identification, or may be used to obtain station status, or both. Are You: Use of this character for confirmation type of answer back has been discontinued until a more suitable arrangement can be devised.
ACK	Acknowledge: A communication control character transmitted by a receiver as an affirmative response to a sender.
BELL	Bell: A character for use when there is a need to call for human attention. It may control alarm or attention devices.
BS	Backspace: A format effector that controls the movement of the printing mechanism one print position backward on the same print line.
HT	Horizontal Tabulation: A format effector that controls the movement of the printing mechanism to the next in a series of predetermined positions along the print line. (Applicable also to the skip function on punched cards.)
LF	Line Feed: A format effector that controls the movement of the paper one line at a time.

Table B-3. Meanings of Control and Special Characters (Cont)

Symbol	Name/Function
VT	Vertical Tabulation: A format effector that controls the movement of paper to the next in a series of predetermined print lines.
FF	Form Feed: A format effector that controls the movement of the printing position to the first predetermined printing line on the next form or page.
CR	Carriage Return: A format effector that controls the movement of the print mechanism to the first print position on the same print line.
SO	Shift Out: A control character indicating that the code combinations that follow shall be interpreted as outside of the character set of the standard code table until a Shift In character is reached.
SI	Shift In: A control character indicating that the code combinations that follow shall be interpreted according to the standard code table.
DLE	Data Link Escape: A communication control character that will change the meaning of a limited number of contiguously following characters. It is used exclusively to provide supplementary controls in data communication networks.
DC_1 DC_2 DC_3 DC_4	Device Controls: Characters for the control of ancillary devices associated with data processing or telecommunication systems, more especially switching devices ON or OFF. (If a single "stop" control is required to interrupt or turn off ancillary devices, DC_4 is the preferred assignment.
NAK	Negative Acknowledge: A communication control character transmitted by a receiver as a negative response to the sender.
SYN	Synchronous Idle: A communication control character used by a synchronous transmission system in the absence of any other character to provide a signal from which synchronism may be achieved or retained.
ETB	End of Transmission Block: A communication control character used to indicate the end of a block of data for communication purposes. ETB is used for blocking data where the block structure is not necessarily related to the processing format.
CAN	Cancel: A control character used to indicate that the data with which it is sent is in error or is to be disregarded.

Table B-3. Meanings of Control and Special Characters (Cont)

Symbol	Name/Function
EM	End of Medium: A control character associated with the sent data which may be used to identify the physical end of the medium, or the end of the used, or wanted, portion of information recorded on a medium. (The position of this character does not necessarily correspond to the physical end of the medium.)
SUB	Substitute: A character that may be substituted for a character which is determined to be invalid or in error.
ESC	Escape: A control character intended to provide code extension (supplementary characters) in general information interchange. The Escape character itself is a prefix affecting the interpretation of a limited number of contiguously following characters.
FS GS RS US	File Separator, Group Separator, Record Separator, and Unit Separator: These information separators may be used within data in optional fashion, except that their hierarchical relationship shall be: FS is the most inclusive, then GS, then RS, and US is least inclusive. (The content and length of a File, Group, Record or Unit are not specified.)
SP	Space: A normally non-printing graphic character used to separate words. It is also a format effector which controls the movement of the printing position, one printing position forward.
DEL	Delete: This character is used primarily to "erase" or "obliterate" erroneous or unwanted characters in perforated tape. (In the strict sense, DEL is not a control character.)

APPENDIX C
DECIMAL/HEXADECIMAL CONVERSIONS

SYMBOLS

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

HEXADECIMAL TO DECIMAL CONVERSION

Given any hexadecimal number @FFFFFF@ or lower, locate the "hexades" sequentially in the hexade chart (table C-1) and sum the results.

Table C-1. Hexade Chart

Hexade:	6	5		4		3		2		1	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15

Example, given N_{16} = 2F9B:

B (Hexade 1) =	11
9 (Hexade 2) =	144
F (Hexade 3) =	3840
2 (Hexade 4) =	8192
Result:	12187

DECIMAL TO HEXADECIMAL CONVERSION

Let the hexades of the desired hexadecimal number H be numbered right to left from 0 upward; that is, H_0 is the rightmost hexadecimal digit, H_1 is the next, ..., as far as required. Repetitively divide the number by 16, letting R be the remainder. For the nth iteration of this loop, Hn becomes R expressed in base 16. The loop terminates after the division by 16 results in a value of zero. Note that this algorithm yields the hexadecimal digits from right to left, that is, the least significant hexadecimal digit is obtained first.

Example, given N_{10} = 802063:

N	N/16	Γ_{R10}	Γ_{R16}	H 5	H 4	H 3	H 2	H 1	H 0
802063	50128	15	F						F
50128	3133	0	0					0	F
3133	195	13	D				D	0	F
195	12	3	3			3	D	0	F
12	0	12	C		C	3	D	0	F
STOP									

Result: @C3D0F@

The process is summarized in figure C-1.

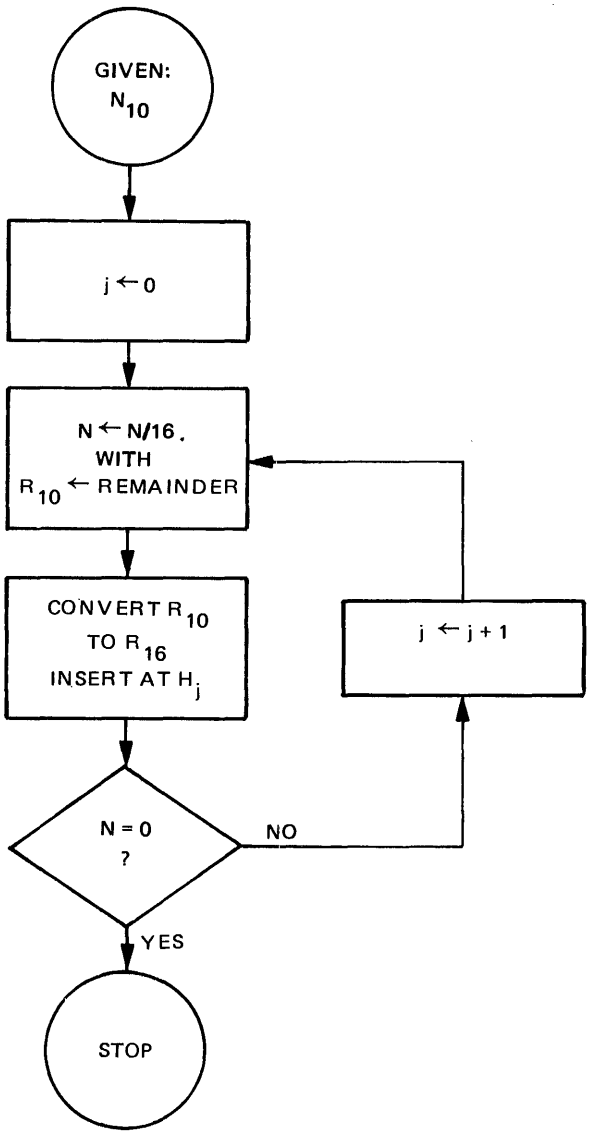
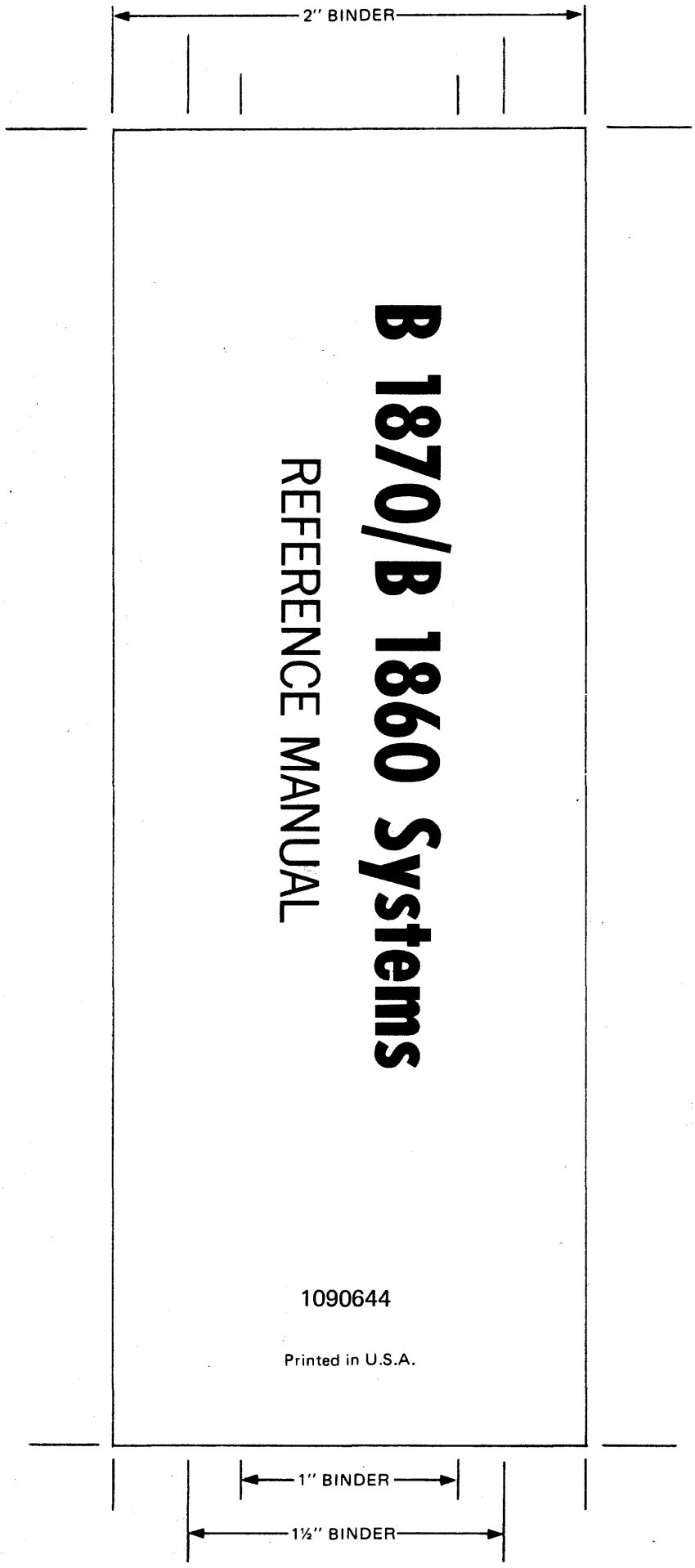


Figure C-1. Decimal to Hexadecimal Conversion Flow Chart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