Burroughs

SERIES

B5500

B5283 INPUT/OUTPUT

TRAINING MANUAL

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TABLE OF CONTENTS

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TABLE OF CONTENTS CONTINUED

SECTION 1

INTRODUCTION OF I/O SYSTEM

GENERAL

The primary function of the 5282 Input/Output Control Unit (I/O Control Unit), shown in Figure 1-1, is to synchronize and control the flow of information in one direction at any one time between any Memory Module and any peripheral device attached to the system.

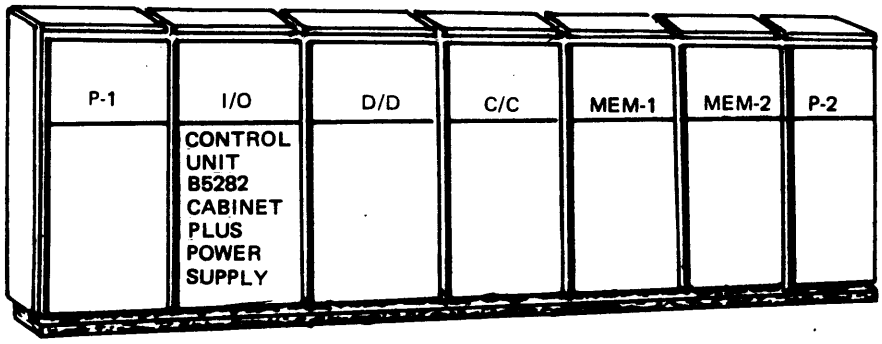

FIGURE 1-1. B5282 I/O CONTROL SUBSYSTEM

A B5500 System must have at least one I/O Control Unit (B5283); and, depending on the predicted volume, can incorporate up to a maximum of four independently controlled units. The number of I/O Control Units included in a system determines the number of simultaneous input/output operations which may take place; that is, if there are four I/O Control Units, there can be as many as four simultaneous operations. The type and quantity of peripheral devices which may be incorporated in a system are listed in Figure 1-2.

The simultaneity of separate input/output operations is accomplished by the use of an "interrupt" system in which the processing function of the system is interrupted and the specified input/output operation initiated.

The term "interrupt" is used in a special sense in the B5500. It does not imply that processing is halted during the input/output operation or that the system is held static in any way. Rather, a transfer of control is taking place, during which the Master Control Program (MCP) may initiate certain types of operations that can proceed simultaneously with computation by the Processor.

Input/output operations, for example, are conventionally controlled by the individual program currently being processed. However, the relatively slow speed of input/output devices normally cause a certain amount of idleness (usually excessive) of the Processor while controlling the input/output operation. This, in turn, results in a serious reduction of actual processing time. This situation is especially prominent in business applications where input/output operations, under control of the Processor, may constitute a large percentage of the computers operating time.

The B5500 has been designed to preclude this condition by permitting maximum use of all peripheral equipments concurrent with computation by the Processor. The simultaneous operation of both input/output equipment and the Processor is accomplished through a centralized communications control which causes a temporary interrupt in

computation when an input/output operation is required. Each time an interrupt condition occurs, processing pauses momentarily while the MCP initiates the specified input/output operation. Control is then returned to the object program being processed. The minute amount of processing time that is lost through MCP control during the interrupt condition can be considered insignificant when compared to the increase of computation time as a result of simultaneous input/output and Processor operation.

All input/output operations are performed and synchronized by the I/O Control Unit after initiation by the Processor. Actually, the initiation is a result of an "Initiate I/O" operator of the MCP. The Processor, in turn, provides the necessary logic to Central Control, which selects an I/O Control Unit and provides the initiation logic levels. Control information for the I/O Control Unit is in the form of a standard 48-bit word which contains all the information pertinent to effecting the I/O operation. This word is called an I/O Data Descriptor.

During the input/output operation possible error conditions are monitored; e.g., correct memory parity, address error conditions, and peripheral unit errors in the form of non-availability levels. These error conditions are recorded in the form of a Result Descriptor word similar in structure to the Data Descriptor. When the specified operation has been completed or an error condition detected, the I/O Control Unit sends the Result Descriptor to Memory for subsequent interrogation by the MCP. This I/O Result Descriptor then indicates whether or not the operation was completed successfully and provides information regarding the type of operation performed. The I/O Control Unit signals the system that the operation has been completed and that the Result Descriptor has been stored in Memory by setting an "I/O Finished" interrupt.

An I/O Control Unit also has the capacity of being placed in local mode: independent of system control and unavailable for system use. While in this mode, the I/O Control Unit may be used to control repetitive operation of any peripheral unit for diagnostic purposes, such that it will not interfere with normal operation of the remainder of the system.

PERIPHERAL UNIT	MINIMUM	MAXIMUM
Magnetic Drum Unit	0	2
Magnetic Tape Unit	0	16
SPO/Keyboard	1	1
Line Printer	0	2
Card Reader	1	2
Card Punch	0	1
Paper Tape Reader	0	2*
Paper Tape Punch	0	2*
Disk File Control	1	2
Data Transmission Control	0	1

* Paper Tape Units have a combined maximum of 3 units.

FIGURE 1-2. PERIPHERAL UNIT CONFIGURATION LIMITS

THE I/O CONTROL UNIT

The B5282 I/O Control Subsystem cabinet includes the physical hardware necessary to enclose from one to four B5283 I/O Channels. In all operational descriptions of a

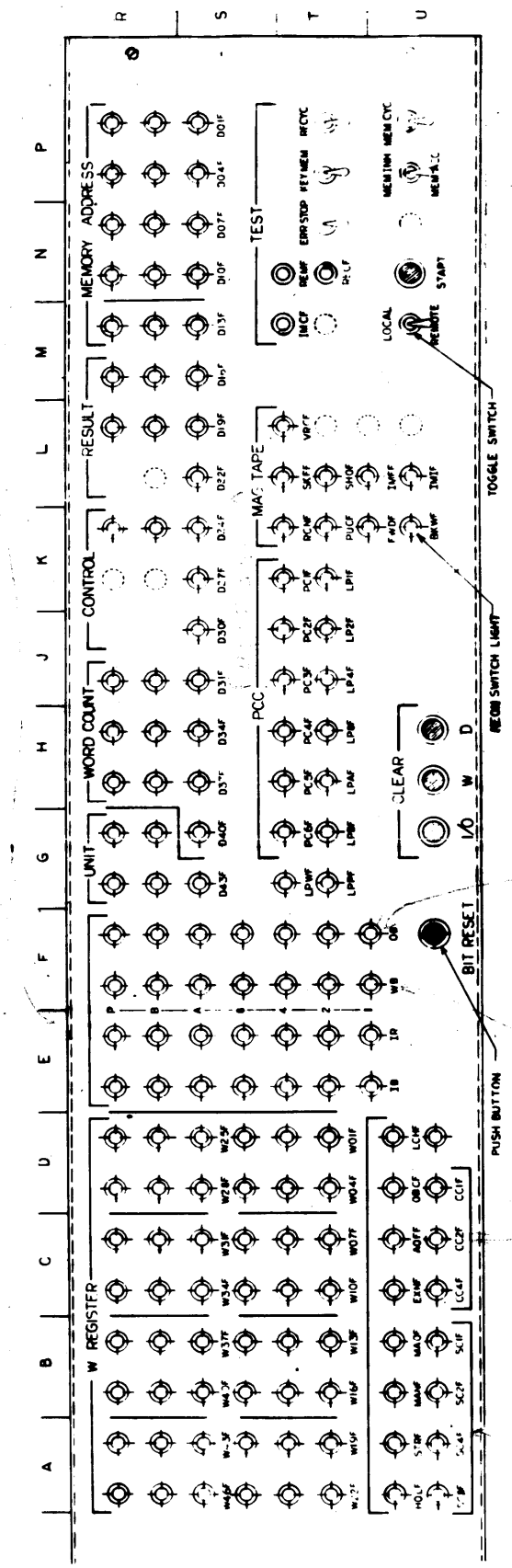

FIGURE 1-3 D & D I/O DISPLAY PANEL

B5283 I/O Channel, the term "I/O Control Unit" is used and should be interpreted to mean both: the B5282 I/O Control Subsystem (Cabinet and Power Supply) and one B5283 I/O Channel (logics racks).

All B5283 I/O Channels are identical in operation, appearance, and physical hardware orientation, and differ only in their physical placement within the B5282 I/O Control Subsystem cabinet.

Each B5283 I/O Channel (I/O Control Unit) is completely independent of the others in operation and is capable of controlling the transfer of information between any peripheral device attached to the B5500 system and any Memory Module.

Transfer of information between core Memory and an I/O Control Unit is accomplished by a parallel transfer, to or from, the peripheral units, a transfer of one character, or a partial character at a time. Essentially, therefore, the I/O Control Unit may be considered as a one word buffer between two different transfer rates.

Illustrated in Figure 1-3 is the I/O display panel located in the Display and Distribution Cabinet. There is one I/O display panel for each B5283 logics rack. Elements within the I/O control unit may be divided into three general areas according to the function of the elements. They are:

1. Functional Areas: Those logical elements used for information and/or control storage and manipulation.

2. Control Areas: Logical elements controlling the flow of information and/or generation of control or information levels.

3. Input/Output Areas: Include both internally and externally generated control inputs or outputs.

A listing of the indicated elements according to these described general areas is as listed below. Included is the appropriate paragraph of the manual describing each.

Functional Areas:

1. W Register
2. D Register
3. Input Parity Generator
4. Longitudinal Parity Buffer (LPnF)
5. Input Alpha/Binary Decoder
6. Output Binary/Alpha Encoder
7. Output Parity Generator
8. Character Routing Matrix
9. Input Read Buffer (IRnF)
10. Input Buffer (IBnF)
11. Output Buffer (ØBnF)
12. Write Output Buffer (WBnF)

Control Areas:

13. Sequence Counter
14. Character Counter
15. Pulse Counter
2. D Register - Word and Address Counters

Input/Output Areas:

16. Sensing Matrix
17. Control Matrix
2. D Register - Address and Unit Designate

Elements of the I/O maintenance panel are grouped according to function as follows:

1. W-Register: W01F - W48F

2. D-Register: D01F - D22F, D24F - D27F, D30F - D45F

   a. Memory Address Field
   b. Result or Error Field
   c. Control Field
   d. Word Count Field
   e. Unit Designate Field

3. IB (Input Buffer): IB1F - IBPF

4. IR (Tape Input Read Buffer): IR1F - IRPF

5. ØB (Output Buffer): ØB1F - ØBBF, ØBPD

6. WB (Tape Write Output Buffer): WB1F - WBPF

7. Magnetic Tape Control

   a. RCNF: Record Control
   b. PUCF: Pile-Up Control
   c. FWDF: Forward
   d. BKWF: Backward
   e. SKFF: Skew
   f. SHØF: Skew Holdover
   g. IMFF: Information
   h. IMIF: Information Index
   i. VRCF: Valid Record

8. General Synchronization and Control

   a. HØLF: Holdover
   b. STRF: Strobe
   c. MANF: Memory Access Needed
   d. MAØF: Memory Access Obtained
   e. EXNF: External

8. General Synchronization and Control (Continued)

   f. AØFF: Address Overflow
   g. ØBCF: Output Buffer Call
   h. LCHF: Last Character
   i. LPWF: Longitudinal Parity Write

9. LP (Longitudinal Parity Buffer) LP1F - LPPF

10. Counters

    a. Sequence Counter: SC8F, SC4F, SC2F, SC1F
    b. Character Counter: CC4F, CC2F, CC1F
    c. Pulse Counter: PC6F, PC5F, PC4F, PC3F, PC2F, PC1F

11. Manual Control

    a. Clear: I/O Control Unit; W Registers: D Register
    b. Bit Reset:

12. Test

    a. IMCF: Initiate Maintenance Cycle
    b. REMF: Remote-Local
    c. RECF: Recylde
    d. ERR/STOP: Stop on Error
    e. KEY MEMORY:
    f. RECYC: Recycle
    g. LOCAl-REMOTE:
    h. START
    i. MEM INH-MEM ACC: Memory; Inhibit Memory Access
    j. MEM CYC: Memory Cycle

SIGNAL LINES BETWEEN I/O AND MEMORY

The interconnecting lines between the I/O Control Unit, Central Control and Memory are defined as follows:

MANF — A Memory Access is needed by the I/O Control Unit.

AOOS — Start Memory Cycle. This level is generated by Central Control when a MANF is received from the I/O Control Unit. AOOS will be true when the appropriate crosspoint flip-flops are set and its associated MCYF is reset.

MWRD — Generated in the I/O Control Unit. Indicates that a Memory write operation is to be performed (D24F set).

WOOD — Composed of MWRD and AOOS. Indicates when true that a write operation is to be performed. When false, a read operation will follow.

MTOD Memory Time 0. A timing interval generated by Central Control during the first microsecond of a Memory access, signals the I/O Control Unit that a Memory cycle has started. MTO also indicates during a write operation, that the write operation has been completed, thus allowing the release of the requesting I/O Control Unit.

MT2D Memory Time 2. States that the read information levels are available to the I/O Control Unit, allowing release of the I/O Control Unit and enabling the set of MAØF (Memory Access Obtained). In the four microsecond memories MT2D is generated by MP=1.

MPED Memory Parity Error. Indicates, when true, that a parity error exists in the word presently contained in the MIR (Memory Information Register).

MAED Memory Address Error. When true, this level indicates to Central Control that the designated Memory Module is nonexistent; i.e., the designated unit is in LOCAL, not up to power or is not part of the system. This level is developed as a result of MNAL (Memory Not Available).

D01F'-D12F' Core Address Levels. Specify a particular word in a Memory Module. These levels originate from the reset side of the flip-flops in the ADDRESS field of the D register.

D15F'-D13F' Memory Module Designate Levels. Specify and Memory Module from 0-7.

W01F'-W48F' I/O Control Unit Information Levels. Originate from the reset side of the W-Register Flip-flops.

A01S-A12S Core Address Levels. These levels are the D01F'-D12F' levels in their switched form and enable the MAR (Memory Address Register).

W01S-W48S Memory Module Input Information Levels. These are the levels W01F'-W48F' in their switched form.

R01S-R48S I/O Control Unit Input Information Levels. Switched information levels originating in MIR and switched in Central Control.

I01F'-I48F' Memory Module Output Information Levels. Originate from the reset side of the MIR Flip-flops. They are sent to Central Control and switched to the form R01S - R48S.

I/O OPERATION AS A PROGRAM FUNCTION

The Master Control Program contains instructions which initially starts a particular input/output operation. In turn, the MCP is notified that an input/output operation is needed by the object program which transfers control to the MCP by generating a "Program Release Interrupt" or a "Continuity Bit Interrupt". At this time the Processor is halted.

After the I/O Control Unit is initiated by the MCP, the Processor is restarted and continues processing the object program.

When the I/O operation is completed, the I/O Control Unit sets an "I/O Finished Interrupt" which, again, interrupts the Processor and transfers control to the MCP. The MCP interrogates the I/O Result Descriptor to see if the input/output operation was completed successfully. If the operation was successful, the MCP allows the Processor to continue; otherwise, control is transferred to another portion of the MCP so necessary corrective action may be initiated.

Figure 1-4 illustrates the general flow of an input/output operation from the time that an I/O operation is needed by an object program until the I/O operation is completed and the object program processing continues. The program processing that occurs in parallel with the I/O operation may or may not be the same object program that needed the I/O operation. This is determined by the priority of the program and whether the program can be continued before the I/O operation is completed. In general, the I/O operation can be divided into three parts:

A. Programmatic initiation of the I/O Operation.
B. Actual I/O operation under control of the I/O Control Unit.
C. Programmatic termination of the I/O operation.

PROGRAM INITIATION - FIGURE 1-4.

When the Object program encounters a Read or Write statement, indicating an input or output operation is required, the process of retrieving the I/O Data Descriptor from Memory is initiated by a Program Release Operator which, through the Processor, performs the following:

1. Fetches the specified I/O Data Descriptor.
2. Alters the Status Bit (46) indicating the specified area is not available as a memory area.
3. Sets a Program Release Interrupt.
4. Stores the address of the Descriptor in R +11.

Following a Store for Interrupt Operator, the system is forced into the Control State under supervision of the MCP. Next, the MCP examines the interrupt condition and starts the I/O operation by generating an Initiate I/O Operator which stores the address of the I/O Data Descriptor in absolute cell address 10.

In addition to this transfer and storage of the I/O Data Descriptor address, the Initiate I/O Operator generates the control levels CMTL (Commence Timing Level) and CMIL (Commence I/O) which are used as primary logic to develop the actual I/O initiate signal, ADNS (Admit Descriptor Now) which is shown in Figure 1-5.

I/O OPERATION

ADNS, in turn, causes the I/O Control Unit to perform a standard Memory access of cell 10 for the address of the designated I/O Data Descriptor. A second Memory access is then performed and the actual I/O Data Descriptor is transferred to the I/O Control Unit. The I/O operation is then performed under instructions contained in the Data Descriptor and the success or failure of the operation recorded in the form of a Result Descriptor word which is then returned to a specific location in memory for interrogation by the MCP. Also, to signal that the I/O operation has been completed, the I/O Control Unit sets a specific "finished" bit in Central Control which develops an address in the Interrupt Address Register (IAR) referencing an "interrogate interrupt routine".

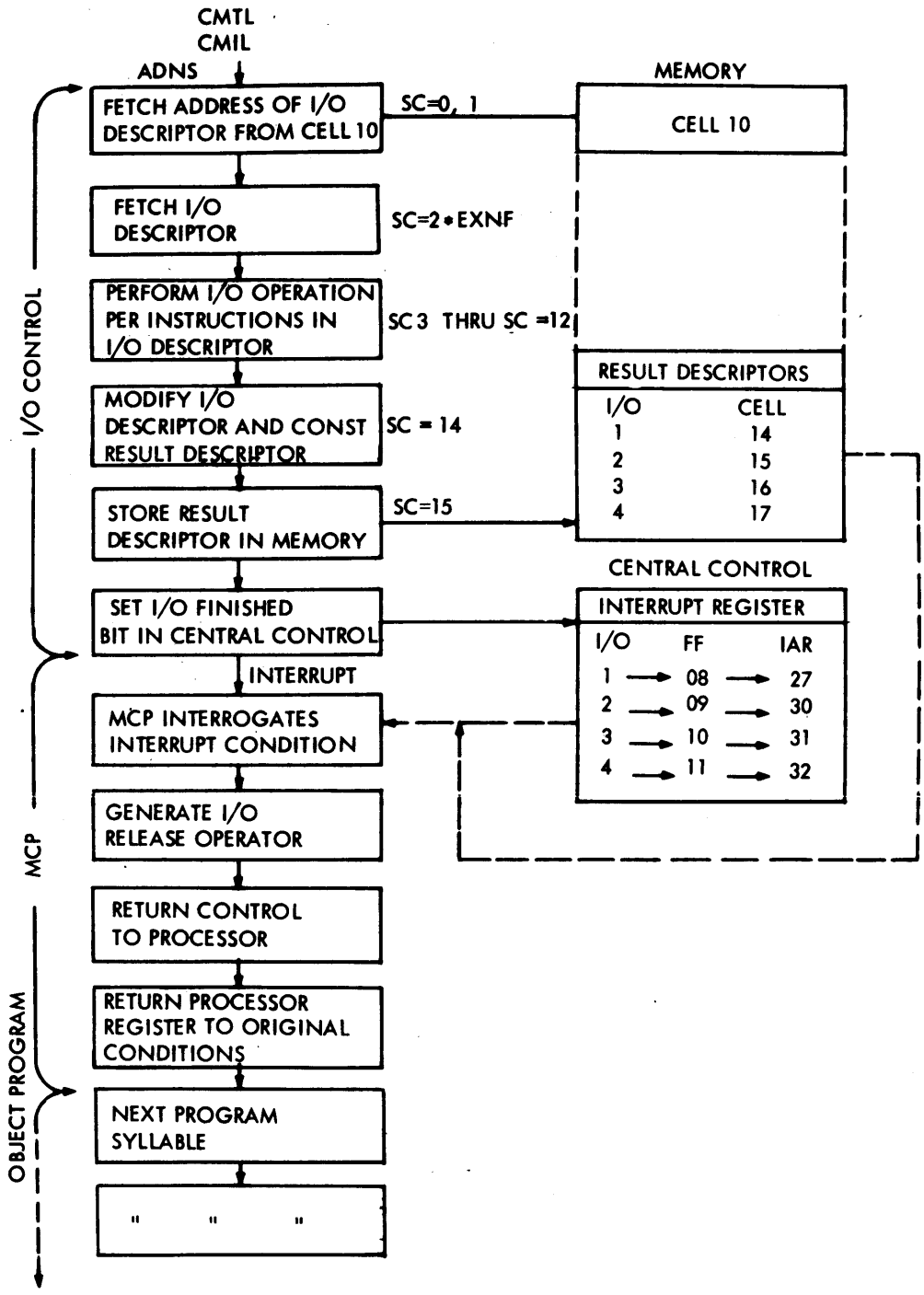

FIGURE 1-4 I/O OPERATION

PROGRAMMATIC TERMINATION

Control now branches to the MCP which, using the specified "interrogate interrupt routine" examines the Result Descriptor for future action. At this point, three courses of action are possible.

1. If the operation was successfully completed, the I/O Control Unit is made available immediately. If another Data Descriptor is ready for processing, the MCP initiates the specified operation before returning control to a program segment in the object program or to the next one scheduled by the MCP.

2. If the operation was not successfully completed, the MCP examines the Result Descriptor for the cause of failure and attempts to rectify the situation. For example, in the event of incorrect reading from tape, the tape is automatically positioned backward and reread. Persistent failure results in operator notification. The program is then interrogated to determine whether to bypass the faulty record or to exit the program at that point. When an I/O operation is unsuccessful, the MCP prevents the destruction to any transferred information.

3. If the Result Descriptor indicates that a Drum transfer operation has just been completed, the MCP determines whether a part of the MCP has been loaded into Memory. (If so, control is transferred to itself.) It should be emphasized that processing is interrupted only when an I/O Control Unit is ready and only long enough to initiate the specified operation, after which the I/O Control Unit together with the designated peripheral unit proceed independently of Processor control. After initiation of any I/O operation, control is immediately returned to a program segment.

In the example shown in Figure 1-4, the result of interrogation of the Result Descriptor (successful operation) is to generate an I/O Release operator which ultimately returns control to the Processor, places the Processor's registers in their pre-interrupt condition, and transfers control to the next program syllable in the object program.

DEVELOPMENT OF ADNS

To initiate an I/O Control Unit, it is necessary to develop an ADNS (Admit Descriptor Now) level for the particular I/O Control Unit designated, that is,

	ADNS-1	I/O #1
	ADNS-2	I/O #2
	ADNS-3	I/O #3
or	ADNS-4	I/O #4

To simplify the explanation of the generation of ADNS by Central Control, we will limit the description to I/O Control Unit #1 (ADNS-1). Selection of the I/O Control Unit to be initiated is determined in Central Control and identical logic is used to initiate the respective ADNS.

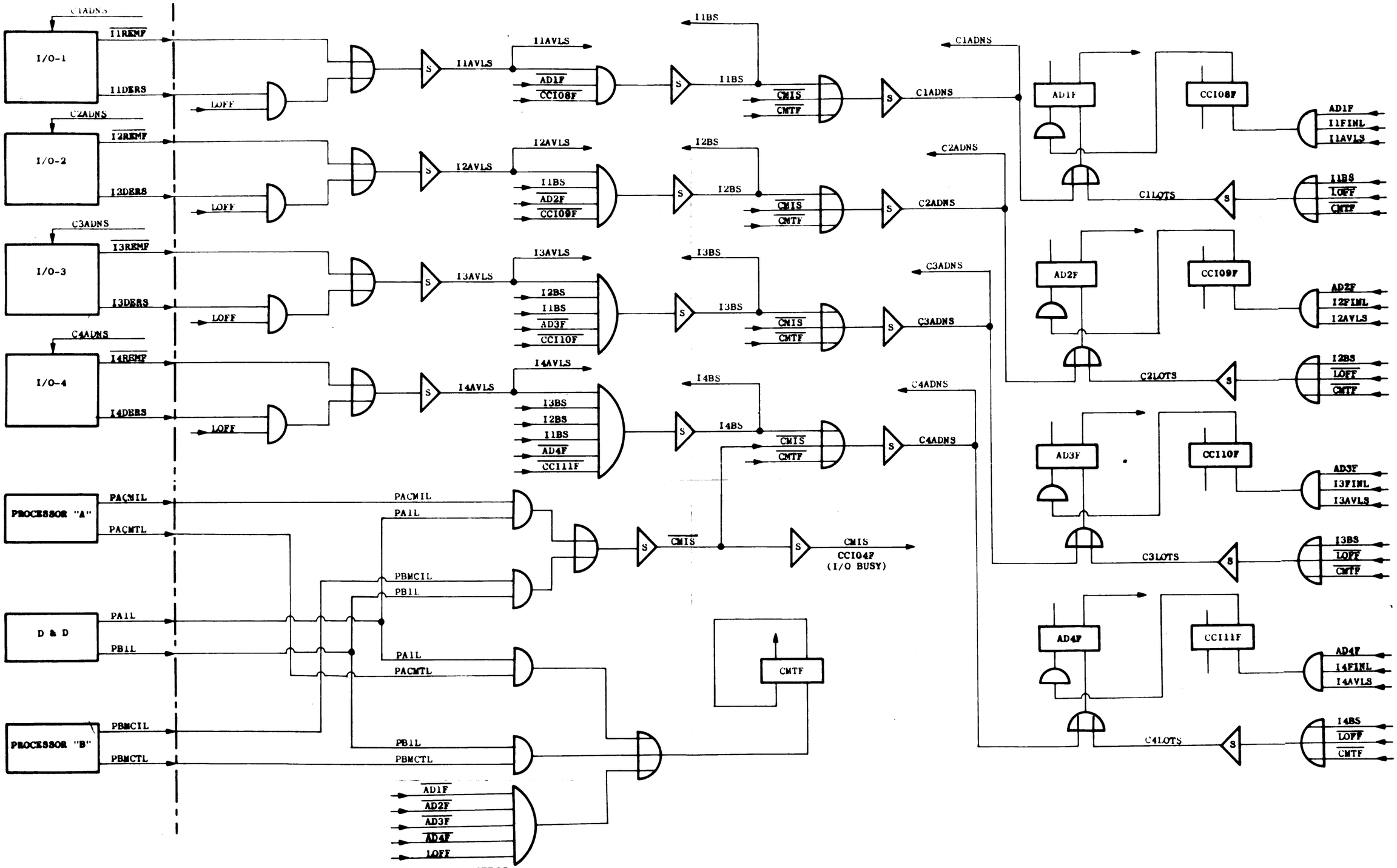

FIGURE 1-5 I/O SELECTION IN CENTRAL CONTROL

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Referring to Figure 1-5, as indicated in this figure, whether or not ADNS-1 will be true depends directly upon the state of:

	I1BS	(I/O #1 Busy Switch)
	CMIS	(Commence I/O)
and	CMTF	(Commence Timing).

All three of these levels must be false in order for ADNS-1 switch to be true.

Development of these levels is as follows:

1. I1BS: The state of the I/O #1 Busy Switch will be true if any one of the following exists:

I1AVLS'	(I/O #1 not available)
AD1F	(I/O #1 busy)
or	
CCI08F'	(I/O #1 not finished)

   where

   I1AVLS generally indicates the physical availability of the I/O Control Unit and will be true to indicate the I/O is available if the term I1REMF' (not remote) is held false by the I/O Control Unit. This level is developed in turn by a manual switch which places the unit either in local or remote. If the REMF line is true or not present, the I1AVLS switch will be false and indicate the non-availability of the unit. Also, I1AVLS will go false during a LOAD operation (LØFF) if an error should occur during the load cycle and is detected in the ERROR field of the D register. I1DERS (D Register Error).

   AD1F (I/O Busy Flip-flop) will normally be false prior to an input/output operation having been reset at the termination of the previous I/O operation by CCI08F (I/O #1 Finished). AD1F is set true when ADNS-1 goes true and indicates an I/O operation has started.

   CCI08F (Finished Interrupt Flip-flop) is set true when it receives an I1FINL (I/O #1 Finished) from the I/O Control Unit at the termination of an operation. CCI08F will be false prior to the generation of ADNS.

2. CMTF: CMTF (Commence Timing Flip-flop) is used to allow the generation of ADNS-1.
   CMTF is set from the level CMTL which is generated as a result of an "Initiate I/O Operator".

3. CMIL: CMIL (Commence I/O Level) is used in conjunction with CMTL to differentiate between an I/O Control Unit and a Processor.

Briefly, the generation of ADNS may be summarized as follows:

Initially, all flip-flops are cleared, CCI08F had been set to indicate the previous input/output operation was completed but is reset at the next clock pulse. AD1F had been reset when CCI08F was set. Also, CMTF was reset at the pulse following the previous CMTL.

Therefore, the I1BS switch will be false, since all three of its input conditions are true. That is,

I1AVLS * CCI08F' * AD1F' = 1

In turn, ADNS-1 will go true when the levels CMTL and CMIL are generated by Central Control from the logic,

I1BS * CMIS' * CMTF' = 0.

ADNS-1 is returned to the I/O Control Unit and the I/O operation initiated. ADNS-1 also sets AD1F indicating that the I/O Control Unit is engaged in an I/O operation. As will be seen later, ADNS-1 is true for only one microsecond, going false when CMIL is terminated, it allows the I/O Control Unit to initiate the first of two memory cycles required to fetch the I/O Data Descriptor.

NOTE

ADNS sets D17F which, in turn, initiates MANF (Memory Access Needed Flip-flop).

The second memory cycle is generated internal to the I/O Control Unit by EXNF (External Flip-flop).

When the I/O operations end, the event is signalled by I1FINL which is generated by the I/O Control Unit after construction of the Result Descriptor. I1FINL, together with AVLS and AD1F (true during the input/output operation) set CCI08F.

If a Card Load or Drum Load operation is to be performed, then the action of CMTL and CMIL is generating an ADNS is simulated by the Load Flip-flop (LOFF), which initiates the I/O Control Unit with its generated level, LOTS. LOFF is set when the LOAD push button is pressed on the Operators Console.

Initially, AVLS will be true since all four terms on the input to AVLS are false, that is;

AD1F • I1DERS • LOFF • I1REMF = 0.

When the LOAD push button is pressed, LOFF will be set at the next clock pulse (note that the same level which sets LOFF previously clears all other flip-flops).

LOFF then sets CMTF from the logic,

CMTF = LOFF * AD1F.

At this same time, LØTS will go true from,

LØTS = I1BS' * CMTF * LØFF,

where LØTS had been previously held false by CMTF and LØFF.

LØTS sets AD1F, indicating the I/O operation has started, which then causes I1BS to go true from the logic:

I1BS = I1AVLS' + CCI08F + AD1F.

In this section, LØTS becomes the primary logic in initiating the load cycle where the function of ADNS is replaced and the construction of a Data Descriptor forced directly in the I/O Control Unit by LØTS itself.

LØTS is held true for 1 μs and goes false when I1BS goes true. CMTF goes false at the same pulse time being reset, by itself, at the pulse following the set condition.

ERROR ON LOAD

If, during the load operation an error is detected and recognized by setting the appropriate bit in the D Register ERROR field, then the level I1DERS (I/O #1 D Register Error) will go true. In turn, AVLS will be forced to go false. If this should occur, then the I/O Finished Flip-flop CCI08F will not be allowed to be set at the end of the operation. This may be seen from the logic to set the I/O #1 Finished Interrupt, as follows:

CCI08F to 1 = AVLS * AD1F * I1FINL.

The load operation then idles until corrective action is taken. This situation is signalled by the fact that the CONTROL state lamp on the Operator's Console stays lit; i.e., the system never enters NORMAL state operation.

I/O CONTROL UNIT MEMORY ACCESS - STANDARD MEMORY CYCLE

The I/O Control Unit has the ability to read from, and write into any Memory Module (0-7) designated by the three higher order bits of the ADDRESS field in the I/O Data Descriptor.

When a Memory access is needed by the I/O Control Unit the level MANF (Memory Access Needed) is generated alone, indicating a "read from Memory" information or with MWRD (Memory Write) specifying a "write into Memory". These levels, in turn, are sent to Central Control Memory Exchange and initiate the respective read or write operation.

Memory Module selection is then determined by Central Control which decodes the Module Address bits (D15F-D13F), examines this address and determines the following:

1. Is more than one I/O Control Unit requesting the same Memory Module; i.e., is there a conflict in address designations?

2. If #1 is true, determine the priority of the requesting I/O Control Units and allow that I/O Control Unit with the highest priority access to the designated Memory Module.

3. Before the actual selection of the Memory Module occurs (through crosspoint control), the addressed module is interrogated to determine if it is presently engaged in a memory cycle. If it is, crosspoint selection is delayed until the current access has ended (delay will be under 4 μs).

Assuming that all the conditions of 1, 2, and 3 have been satisfied, the designated Memory Module is logically connected to the requesting I/O Control Unit by setting the appropriate crosspoint flip-flops. This allows the transfer, to Memory, of the address and information levels, the Memory Start level (AOOS), and the type of operation to be performed; i.e., WOOD (Write) or WOOD' (Read).

STANDARD LOGIC

GENERAL

Standard logic is defined as those Sequence Count intervals which are common to the initiation and termination of an I/O Operation for all peripheral equipment. Generally, Sequence Counts (SC's) 0, 1, 2, 14, and 15 are assigned to initiate certain logical procedures and establish communication between Memory, a designated peripheral unit, Central Control, and the I/O Control Unit.

Specifically, Sequence Counts 0, 1, and 2 are assigned the task of performing certain logical operations to initiate an I/O Operation, while Sequence Counts 14 and 15 are used to terminate the I/O operation. Briefly, the function of the standard SC's are summarized as follows:

SC 0, 1, 2:
- A. Initial load of an I/O Data Descriptor
- B. Construct Descriptor for memory load
- C. Construct Card Reader Descriptor for memory load.

SC 14, 15:
- A. Construct Result Descriptor and return to Memory.

All operations are started when an ADNS (Admit Descriptor Now) level is received from Central Control. ADNS indicates that the particular I/O Control Unit addressed by Central Control is ready for normal operation.

INITIAL LOAD OF I/O DATA DESCRIPTOR

During this operation, a specified I/O Data Descriptor will be addressed, called from Memory, and placed in the I/O Control Unit. The operational Sequence Count cycle involved in this process is in the order SC=0, 1, 2, 0, 1, 2 at the end of which control is transferred to SC=3 of the designated peripheral unit.

When an ADNS level is received from Central Control, the following general events occur. Applicable logic for this operation may be found in Figure 1-8. The entire operation is summarized in a decisional flow chart shown in Figure 1-7.

SC=0
- A. Generate memory cell address 10. (Cell 10 contains the address of the desired I/O Data Descriptor.
- B. Initiate a memory cycle.
- C. Load word in cell 10 into the W register.
- D. Check for memory parity and address error (from Memory to I/O).
- E. SC+1.

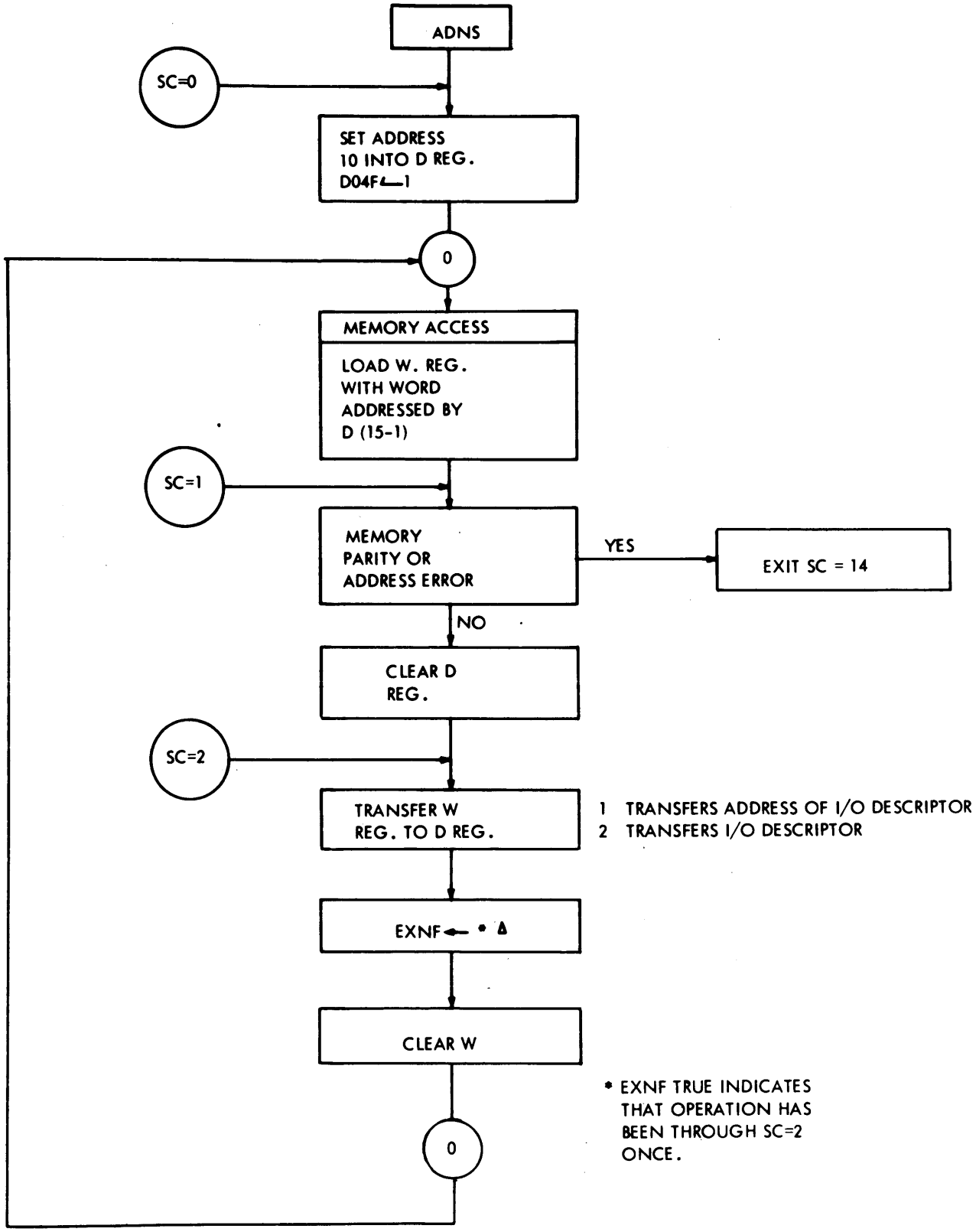


FIGURE 1-6 I/O DATA DESCRIPTOR LOAD 0, 1, 2, 0, 1, AND 2

SC=1:
- A. If either a memory parity or address error exists, exit to SC=14. If a normal load occurred,
- B. Clear the D-register.
- C. SC+1.

SC=2:
- * A. Transfer W(15-1) to D(15-1). The address of the desired I/O Data Descriptor is now in the ADDRESS field of the D register.
- * B. Transfer W(45-24) to D(45-24). Information transferred is insignificant since the word presently in the W register contains only the address of the desired I/O Data Descriptor.
- C. Clear the W register. All pertinent information has been transferred from the W register to the D register.
- D. Return control to SC=0.

SC=0:
- A. Initiate another memory cycle.
- B. Load the word addressed by D(15-1) into the W register. (W register now contains the specified I/O Data Descriptor).
- C. Check for memory parity and address error (from memory to I/O).
- D. SC+1.

SC=1:
- A. If either a memory parity or an address error exists, exit to SC=14. If a normal load occurred,
- B. Clear the D register (Address 8 information erased).
- C. SC+1.

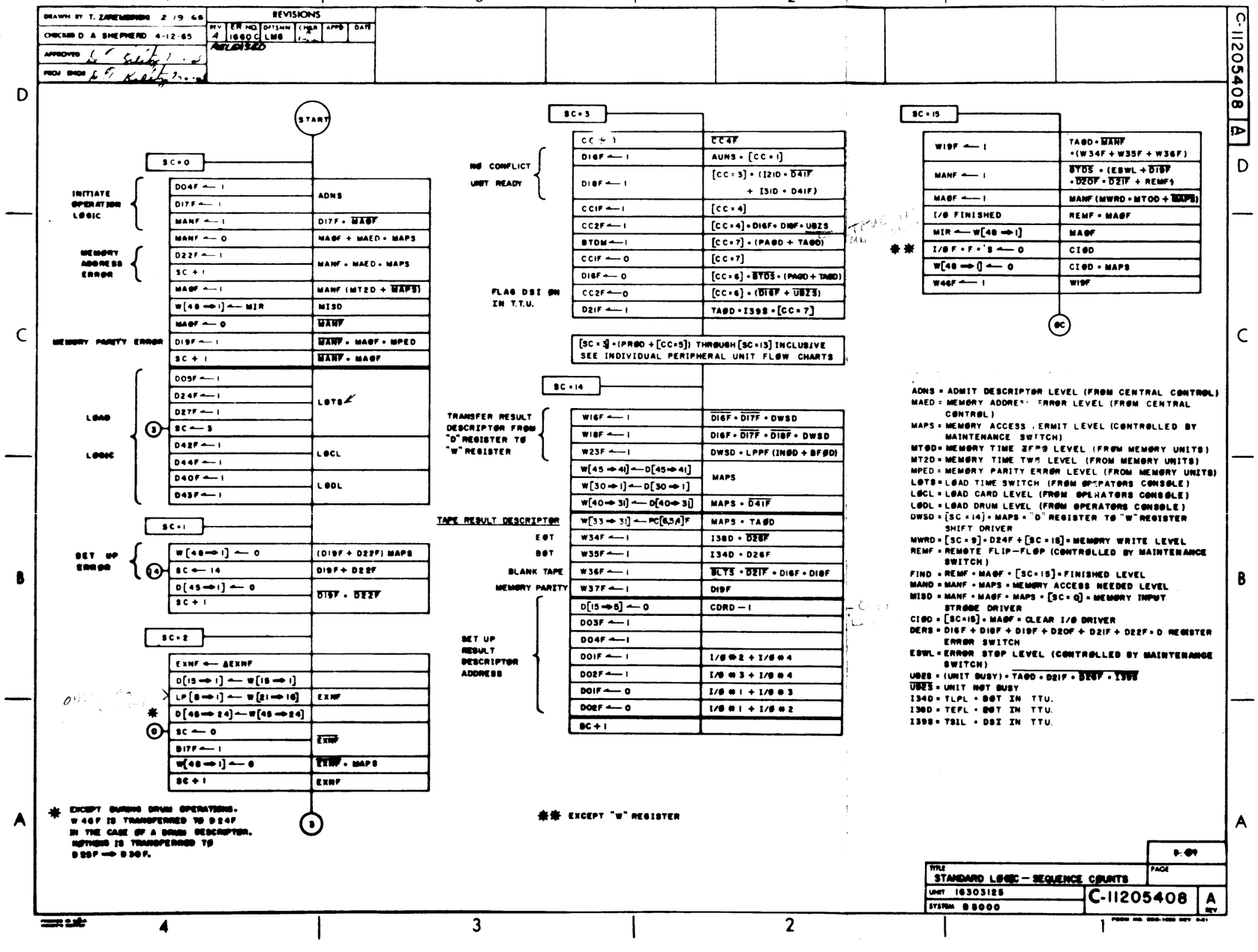
SC=2:
- * A. Transfer W(15-1) to D(15-1). D(15-1) now contains the core memory address where the transfer of information is to start. (Read or Write)
- * B. Transfer W (45-24) to D(45-24). D(45-24) now contains the UNIT DESIGNATE number and other information pertinent to the characteristics of the information to be transferred.
- C. Transfer W(21-16) to LP(B-1). For Drum this is the first six bits of the Drum Address. For the Drum Printer this is a portion of the format control field. In all other Descriptors this area is not used. This transfer is made in order to insure that the ERROR field is clear in subsequent error interrogations.
- D. SC+1.

*NOTE

Except Drum where W 25 - 30 are not transferred and D24 is set from W46.

This completes the load of the specified I/O Data Descriptor. Control is now transferred to the designated peripheral unit at Sequence Count =3.

Illustrated in Figure 1-7 is the symbolic representation of the logical units used during Sequence Counts 0, 1, and 2.


DRAWN BY T. ZARELLI 2/9/66
CHECKED D A SHEPHERD 4-12-65
APPROVED
FROM ENGR
REVISIONS
REV 4 ER NO 1660 C DATE/INIT LMG CHKR APPD DATE
RELEASED
C-11205408 A
START
SC=0
INITIATE OPERATION LOGIC
DO4F ← 1
D17F ← 1
MANF ← 1
ADNS
D17F • MAGF
MEMORY ADDRESS ERROR
MANF ← 0
D22F ← 1
SC + 1
MAGF + MAED • MAPS
MANF • MAED • MAPS
MEMORY PARITY ERROR
MAGF ← 1
W[48 ⇒ 1] ← MIR
MAGF ← 0
D19F ← 1
SC + 1
MANF (MT2D + MAPS)
MISD
MANF
MANF • MAGF • MPED
MANF • MAGF
LOAD
LOAD LOGIC
D05F ← 1
D24F ← 1
D27F ← 1
SC ← 3
D42F ← 1
D44F ← 1
D40F ← 1
D43F ← 1
LØTS
LØCL
LØDL
SC=1
SET UP ERROR
W[48 ⇒ 1] ← 0
SC ← 14
D[45 ⇒ 1] ← 0
SC + 1
(D19F + D22F) MAPS
D19F + D22F
D19F • D22F
SC=2
EXNF ← ΔEXNF
D[15 ⇒ 1] ← W[15 ⇒ 1]
LP[8 ⇒ 1] ← W[21 ⇒ 16]
D[48 ⇒ 24] ← W[48 ⇒ 24]
SC ← 0
D17F ← 1
W[48 ⇒ 1] ← 0
SC + 1
EXNF
EXNF • MAPS
EXNF
* EXCEPT DURING DRUM OPERATIONS. W 46F IS TRANSFERRED TO D 24F IN THE CASE OF A DRUM DESCRIPTOR. NOTHING IS TRANSFERRED TO D 25F ⇒ D 30F.
SC=3
NO CONFLICT UNIT READY
CC + 1
D16F ← 1
D18F ← 1
CC1F ← 1
CC2F ← 1
BTDM ← 1
CC1F ← 0
D16F ← 0
CC2F ← 0
D21F ← 1
CC4F
AUNS • [CC=1]
[CC=3] • (I21D • D41F + I31D • D41F)
[CC=4]
[CC=4] • D16F • D18F • UBZS
[CC=7] • (PA0D + TA0D)
[CC=7]
[CC=6] • BTDS • (PA0D + TA0D)
[CC=6] • (D16F + UBZS)
TA0D • I39S • [CC=7]
FLAG DSI ON IN T.T.U.
[SC=3] • (PR0D + [CC=5]) THROUGH [SC=13] INCLUSIVE SEE INDIVIDUAL PERIPHERAL UNIT FLOW CHARTS
SC=14
TRANSFER RESULT DESCRIPTOR FROM "D" REGISTER TO "W" REGISTER
W16F ← 1
W18F ← 1
W23F ← 1
W[45 ⇒ 41] ← D[45 ⇒ 41]
W[30 ⇒ 1] ← D[30 ⇒ 1]
W[40 ⇒ 31] ← D[40 ⇒ 31]
W[33 ⇒ 31] ← PC[6,5,4]F
D16F • D17F • DWSD
D16F • D17F • D18F • DWSD
DWSD • LPPF (IN0D + BF0D)
MAPS
MAPS • D41F
MAPS • TA0D
TAPE RESULT DESCRIPTOR
EOT
BOT
BLANK TAPE
MEMORY PARITY
W34F ← 1
W35F ← 1
W36F ← 1
W37F ← 1
I36D • D26F
I34D • D26F
BLTS • D21F • D16F • D18F
D19F
SET UP RESULT DESCRIPTOR ADDRESS
D[15 ⇒ 6] ← 0
D03F ← 1
D04F ← 1
D01F ← 1
D02F ← 1
D01F ← 0
D02F ← 0
CDRD − 1
I/0 ⇔ 2 + I/0 ⇔ 4
I/0 ⇔ 3 + I/0 ⇔ 4
I/0 ⇔ 1 + I/0 ⇔ 3
I/0 ⇔ 1 + I/0 ⇔ 2
** EXCEPT "W" REGISTER
SC=15
W19F ← 1
MANF ← 1
MAGF ← 1
I/0 FINISHED
MIR ← W[48 ⇒ 1]
I/0 F • F • 's ← 0
W[48 ⇒ 0] ← 0
W46F ← 1
TA0D • MANF • (W34F + W35F + W36F)
BTDS • (ESWL + D18F • D20F • D21F + REMF)
MANF (MWRD • MT0D + MAPS)
REMF • MAGF
MAGF
CI0D
CI0D • MAPS
W19F
ADNS = ADMIT DESCRIPTOR LEVEL (FROM CENTRAL CONTROL)
MAED = MEMORY ADDRESS ERROR LEVEL (FROM CENTRAL CONTROL)
MAPS = MEMORY ACCESS PERMIT LEVEL (CONTROLLED BY MAINTENANCE SWITCH)
MT0D = MEMORY TIME ZERO LEVEL (FROM MEMORY UNITS)
MT2D = MEMORY TIME TWO LEVEL (FROM MEMORY UNITS)
MPED = MEMORY PARITY ERROR LEVEL (FROM MEMORY UNITS)
LØTS = LØAD TIME SWITCH (FROM OPERATORS CONSOLE)
LØCL = LØAD CARD LEVEL (FROM OPERATORS CONSOLE)
LØDL = LØAD DRUM LEVEL (FROM OPERATORS CONSOLE)
DWSD = [SC=14] • MAPS = "D" REGISTER TO "W" REGISTER SHIFT DRIVER
MWRD = [SC=9] • D24F + [SC=15] • MEMORY WRITE LEVEL
REMF = REMOTE FLIP-FLOP (CONTROLLED BY MAINTENANCE SWITCH)
FIND = REMF • MAGF • [SC=15] • FINISHED LEVEL
MAND = MANF • MAPS • MEMORY ACCESS NEEDED LEVEL
MISD = MANF • MAGF • MAPS • [SC=0] • MEMORY INPUT STROBE DRIVER
CI0D = [SC=15] • MAGF • CLEAR I/0 DRIVER
DERS = D16F + D18F + D19F + D20F + D21F + D22F • D REGISTER ERROR SWITCH
ESWL = ERROR STOP LEVEL (CONTROLLED BY MAINTENANCE SWITCH)
UBZS = (UNIT BUSY) • TA0D • D21F • D26F • I39S
UBZS = UNIT NOT BUSY
I34D = TLPL • BOT IN TTU.
I36D = TEFL • BOT IN TTU.
I39S = TSIL • DSI IN TTU.
TITLE STANDARD LOGIC — SEQUENCE COUNTS
PAGE B-09
UNIT 16303128
SYSTEM B5000
C-11205408
A REV

SC=0: Upon receipt of an ADNS from Central Control, D04F and D17F will be set from the logic:

$$D04F = ADNS * SC = 00$$
$$D17F = ADNS * SC = 00$$

D04F logically sets the ADDRESS field of the D register to an absolute address of 10. Cell 10 contains the address of the desired I/O Data Descriptor.

D17 is initially set to allow the set of MANF (Memory Access Needed) and logically indicates that an ADNS has been received. Since the level ADNS is true for only 1μs D17F allows a second memory access to be performed when the I/O Data Descriptor is brought from Memory.

The pulse following the set of D17F sets MANF from the logic:

$$MANF = D17F * MAOF/$$

MANF, in turn, initiates a standard memory access and the word addressed by the ADDRESS field of the D register will be accessed and transferred into the W register. Briefly, this memory access is performed as follows.

Memory Access. Initially, MANF and MAØF are reset. MAPS (Memory Access Permit) will be true when the I/O Control Unit is in the remote mode. As previously explained, the first pulse following the set of D17F sets MANF. As soon as MANF goes true, MAND (Memory Access Needed) level is developed and sent to high speed memory where a standard memory cycle is initiated. The memory clock is started (MT0-MT3) and the crosspoint flip-flops set with the address contained in the D register (Cell 10). Prior to setting the crosspoint flip-flops, the Memory Unit Address (enabled as soon as the D register was set with an address) is interrogated; and if an error in address designation is detected, e.g., addressing a non-existent module, the level MAED (Memory Address Error) is returned to the I/O Control Unit. If MAED is true, then the event is flagged by setting D22F in the error field of the Result Descriptor and the SC counted +1.

$$D22F = MANF * MAED * MAPS$$

Also, to disable the current request for a memory access, MANF is reset from the logic:

$$MANF/ = MAED * MAPS$$

In absence of a MAED condition, the memory access proceeds normally; and when Memory Time 2 is generated, (MT2) MAØF will be set. (Notice that MAØF is set with the pulse when MT2 is true--or at the set of (MT1).

$$MAOF = MANF * (MT2D + MAPS/)$$

In turn, the Memory Information Strobe (MISD) goes true (Gate "r"); and at the next pulse, the information in MIR (Memory Information Register) is shifted into the W register. This transfer occurs at MT2 time.

$$MIR \text{ to } W[48 \Rightarrow 1] = MISD$$

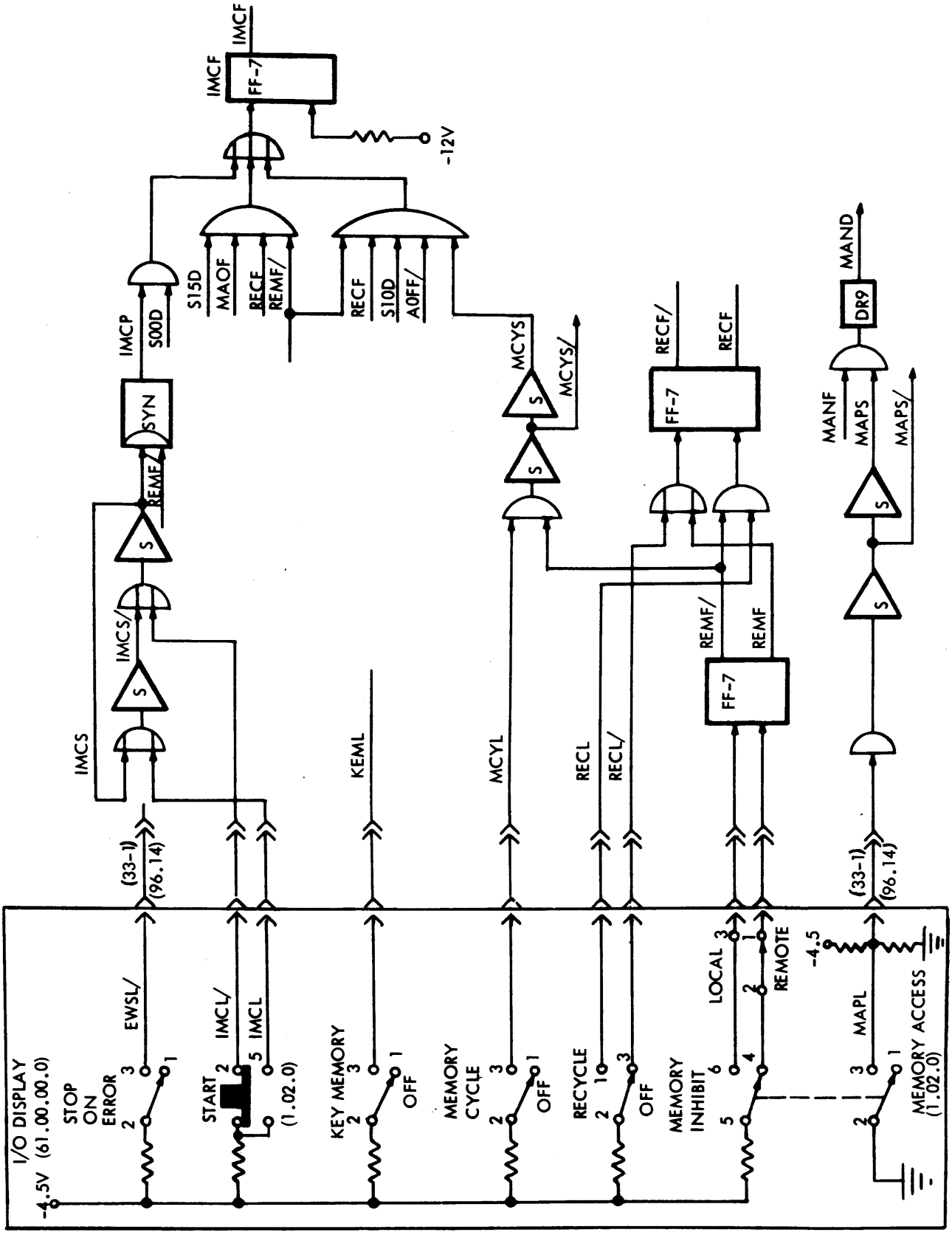


FIGURE 1-8 INITIATE MAINTENANCE

The same clock pulse which sets the W register with memory information resets MANF indicating a memory access is no longer needed.

$$MANF/ = MA\emptyset F$$

At the next pulse, the completion of the memory access is signalled by resetting MAØF:

$$MAOF/ = MANF/$$

The only remaining action involved in accessing a word from memory is detecting whether a Memory Parity Error (MPED) existed when the transfer from memory was accomplished. If an MPED does exist, the level MPED (detected at MT3) is returned to the I/O Control Unit and at the next pulse will set D19F in the error field of the Result Descriptor.

$$D19F = MANF/ * MAOF * MPED$$

This completes the memory access of the word addressed by the ADDRESS field of the D register. In this case, the W register now contains the address of the specified I/O Data Descriptor.

Normal exit from SC=0 is accomplished at the pulse following the set of the W register with memory information from the logic:

SC=1: To this point, operations performed or conditions detected may be summarized as follows:

The address of the specified I/O Data Descriptor was constructed in the ADDRESS field of the D register and the word specified by this address (Cell 10) accessed by a standard memory cycle and placed in the W register. If a MAED was detected, (non-existent memory module) D22F was set. If a MPED was detected, D19 was set.

If either a Memory Parity Error (MPED) or a Memory Address Error (MAED) was detected in the previous SC=0, the W register is cleared by:

$$W[48 \Rightarrow 1]/ = (D19F + D22F) * MAPS$$

and control transferred to SC=14.

In normal operation the D register is cleared, erasing the address of the address now contained in the W register. Also, the SC is counted +1.

SC=2: The first clock pulse following entry to SC=2 complements (Δ) EXNF (External Flip-flop). EXNF, originally reset, is a logical flip-flop used in Standard Logic SC 0, 1, 2 to indicate, when set, that SC=0 and 1 of the first half cycle (0, 1, 2) have been completed. As will be shown later, EXNF allows transfer of control to SC=3, after the second half cycle of Standard Logic has been completed. EXNF is set, ungated, from the logic:

$$\Delta EXNF = SO2D$$

Essentially, all of the W register is transferred to the D register with the exception of W(16-23). Information in the area of W48 - W16 is insignificant at this point, since the word in the W register contains only the address located in W(15-1).

Control is now transferred back to SC=0 and D17F is set to enable another memory access. (D17F had been reset during SC=1). This transfer of control is accomplished through the following logic:

SC/ = EXNF/ * SO2D
D17F = EXNF/ * SO2D

As control is transferred to SC=0 the W register is cleared in anticipation of the next word load from memory. All of the actions described in SC=2 occur during the 1 μs interval (SC=2 is true.)

SC=0: Upon entering SC=0 and with D17F and MAØF/ true, a second memory cycle is initiated by setting MANF. The I/O Data Descriptor specified by the address in D01-D15 is accessed and placed in the W register in the manner previously explained.

SC=1: Actions performed during the second SC=1 are identical to those effected during the first half cycle.

SC=2: Operations performed during SC=2 of the second half cycle are identical to those performed during SC=2 of the first half cycle with the exception of actions whose secondary logic is dependent upon the control EXNF/. EXNF is now true as a result of complementing logic performed during the previous SC=2.

Termination of the Standard Logic cycle for an initial I/O Data Descriptor load is performed as follows. Note that all actions occur at the first pulse following entry to SC=2.

Δ EXNF = SO2D
W[15 => 1] to D[15 => 1] = SO2D
W[45 => 24] to D[45 => 24] = SO2D

In addition to, and as a result of complementing EXNF/ at the previous SC=2, the following transfer and exiting logic is enabled:

W[21 => 16] to LP[B => 1] = EXNF * SO2D

The final result of the Standard Logic Cycle 0, 1, 2, 0, 1, 2---3 is illustrated in Figure 1-6.

All bit positions of the I/O Data Descriptor have been shifted to the D register except for the PERIPHERAL CONTROL field D21-D16 which is temporarily stored in the LP Buffer Register. This action is necessary since this field contains information in Magnetic Drum and Drum Printer operation which would be destroyed by ERROR field information developed in subsequent operations.

PERIPHERAL CONTROL information is retained in the LP Buffer until needed by the Drum or Drum Printer at later SC's.

LOAD LOGIC

General

The purpose of initial Load Logic is to load high speed core memory with a portion, or all, of the MCP or, alternately, a diagnostic program. Input to the I/O Control Unit is either from cards or drum and depends upon the physical location of the LOAD SELECT switch on the operator's console. TWO control levels are generated from this switch, termed:

LODL = Load Drum Level
LOCL = Load Card Level

In order to read the MCP into core memory from the Drum or Card Reader it is first necessary to construct an appropriate I/O Data Descriptor specifying details of the operation to be performed; e.g., Unit Designate Number, starting core memory address, mode of operation and the number of words to be transferred. Also, if an LØDL operation is to be performed, the starting Drum address must also be specified.

Construction of an I/O Data Descriptor for the Drum or Card Reader is accomplished by setting certain significant flip-flops in the D register whose bit position and assigned weight correspond to the commands necessary to effect the load of memory.

Essentially, the D register is placed in a condition comparable to the terminal state of a standard I]O Data Descriptor load from memory. (SC=2 second half-cycle). When the proposed input operation has been completely described by the constructed Data Descriptor, control is transferred to SC=3 of the applicable unit and the operation commences.

Initiation of LODL or LOCL occurs when LOTS (load time switch) goes true at the depression of the LOAD pushbutton. The following operations will occur, depending upon whether a card load (LOCL) or Drum load (LODL) has been selected.

A. DRUM LOAD = LOTS and LODL: Depressing the LOAD switch initiates the generation of an I/O Drum Descriptor which, in turn, loads high speed core memory from Band 0 of the Drum. The load of memory will start from memory cell 20 and ascend in address location to a specified 1000 words. Additional loading of further information is dependent on instructions contained in the already loaded portion of the MCP. Although the MCP can consist of 16,384 words, additional load instructions are required since the number of words to be read is specified and, therefore, limited by the capacity of the WORD COUNT field of the I/O Data Descriptor, or 1023 words (D40-D31).

B. CARD READER Load = LOTS and LOCL: Depressing the LOAD switch causes one binary card to be read from the Card Reader with the lowest UNIT DESIGNATE number. Card information is loaded into core memory, starting from cell 20 octal in ascending address location to a specified maximum of 20 words (Cell 43). Additional load instructions are dependent upon internal control instructions contained in the first twenty words.

At the end of both LODL and LOCL a check is made to insure that information transfer has been performed without error. If the transfer is not complete or an error occurs, control is branched to memory cell 16 and the system left in such condition to allow another attempted load operation when the LOAD switch is again depressed. If transfer has been completed, without error, and Processor 1 is idle; then subsequent control of Processor 1 is transferred to cell 20.

Detailed Operation.

DRUM Load. Initially, both the D and W registers are cleared. When the LOAD pushbutton is depressed with the LOAD select switch in the LOAD DRUM position, the levels LOTS (Load Time) and LODL (Load Drum) will go true. As indicated in the Standard Logic Flow Chart in Figure 1-7, certain flip-flops in the D register will be set, forcing the construction of an I/O Drum Descriptor. Simultaneously, control is transferred to SC=3 of Drum operation. Applicable Drum load logic contained in the Standard Logic flow is shown in Figure 1-7.

The significance of this logic is explained as follows:

Address Field. Setting D05F specifies that the starting core memory address (where the load of memory is to commence) is equal to absolute cell address 20.

I/O Control Filed. D24F indicates that this is a Drum read operation. Normally, a DRUM Descriptor contains this information in the W46F position which is then transferred to the D24F position, during the final W to D shift in SC=2 of the Standard Logic Cycle for an I/O Data Descriptor Load.

D27F signifies that the DRUM read operation will be performed in binary mode.

Word Count Field. D40F specified that 512 words are to be read from the DRUM.

Unit Designate Field. D43F indicates the DRUM 04 shall be used in this operation.

The starting DRUM address is specified in the D16F-D30F field of the W register and in this case is equal to 0. The DRUM read will, therefore, start from Band 0 on the DRUM.

RESULT DESCRIPTOR

Terminate I/O Operation General. SC=14 and 15 of this Standard Logic Routine are used to terminate an I/O operation by constructing a Result Descriptor and returning this Descriptor to a specified address in Memory. This exit routine may be initiated by a number of logical situations arising during the processing of information through a peripheral device, but in general, is started as a result of two main conditions. Either:

1. An error condition has been detected during the course of an I/O operation and further information transfer is to be inhibited, or

2. The specified number of words have been transferred successfully (or unsuccessfully) and a normal exit from the I/O operation is to be performed.

In either case, a J14D (Jump to SC=14) level is generated and control transferred to SC=14.

The generation and storage of the I/O Result Descriptor is performed in two logical intervals as follows:

SC=14: Transfer the Result Descriptor from the D register to the W register and set up a Result Descriptor Address for the particular I/O Control Unit used for the I/O operation.

SC=15: Perform a Memory access write operation and transfer the Result Descriptor to the address specified in SC=14. After storage, clear the I/O Control Unit for the next operation.

Detailed Operation - SC=14. Transfer, upon entry to SC14, the D register contains the original I/O Data Descriptor modified in form and contents to include various results of error interrogations performed during the I/O operation. In order to transfer the Result Descriptor to Memory, it is necessary to shift all pertinent information from the D register to the W register (only W accesses memory directly). This action is accomplished at the first pulse following entrance to SC=14 through the generation of DWSD (D to W register shift) from the logic:

DWDS = S14S • MAPS

This is not a direct 45-bit transfer (as indicated) for all bits; however, since the state of D16F and D18F reflect the complement state of the corresponding W register flip-flop. That is, W16F and W18F are specified as true in the Result Descriptor when the designated unit is BUSY and NOT-READY; the opposite state of the logical conditions are established for D16F and D18F at the time of the BUSY-Ready test performed during SC=3.

As previously stated, W16F is set with D16F' and indicates that the designated unit is BUSY. D17F' is also included and logically indicates that a BUSY test was performed. If D17F' was not included, W16F would be set, even though the BUSY test was not performed since D16F is normally in the reset state.

NOTE

D17F, when set and recognized as such at SC=14, indicates, logically, that either MPED (Memory Parity Error) or a MAED (Memory Address Error) occurred while accessing the Descriptor address of the Descriptor itself. Normally, D17F is used as enabled logic for MANF and is set twice during the Standard Logic Cycle to allow the two memory accessed required to fetch the I/O Data Descriptor. At SC=1 of each access, if no MPED or MAED (D19F/ or D22F/) error occurred, D17F is normally reset when the D register is cleared with the operation continuing normally into SC=2 and then SC=3. If, however, an error is detected (D19F or D22F) the operation exits immediately to SC=14; and the D-Register is not cleared. Thus, upon entry to SC=14, D17F will still be set indicating that an MPED or MAED occurred while accessing the Data Descriptor or its address.

Conversely, if D17F is reset, it indicates that two memory accesses were performed successfully and that the operation did continue into SC=3--the logical interval where the BUSY and READY tests were performed. Therefore, upon entry to SC=14, D17F reset implies that a BUSY and READY test was performed and valid information is stored in D16F and D18F.

W18F is set with D18F' and D16F and signifies that the designated unit is NOT-READY although NOT-BUSY. As with W16F, D17F' is included in the logic to indicate that a READY test has been performed at SC=3.

CONSTRUCTING MEMORY ADDRESS

Concurrent with the transfer of the D-Register to the W-Register is the construction of an absolute address for returning the Result Descriptor to Core Memory. Each I/O Control Unit has a specific location in Memory for storage of its particular Result Descriptor as follows:

I/O	Address
1	12_{10}
2	13_{10}
3	14_{10}
4	15_{10}

Since all addresses contain the common configuration D03F and D04F, these bits are set with the level CDRD-1 (Clear D-Register).

D03F = CDRD-1
D04F = CDRD-1
CDRD-1 = S14S

NOTE

D03F and D04F specify Address 12 for I/O #1.

The remaining addresses (13, 14, and 15) are defined by D01F and D02F which will be set according to the particular I/O Control Unit in use.

SC=14 operations (1 μs) are terminated by transferring control to SC=15 with the same pulse which effects the register transfer and address construction operations.

Detailed Operation SC=15

Upon entry to SC=15, the following situations exist:

1. The Result Descriptor has been transferred to the W register.
2. An address has been constructed in the ADDRESS field of the D register to which the Result Descriptor is to be returned.

The purpose of SC=15 is to generate a memory access cycle and write the Result Descriptor into the address specified by D01F-D15F. Upon completion of the transfer an I/O Finished Level is generated and returned to Central Control and the I/O Control Unit cleared for the next I/O operation.

When the SC is counted to 15 MWRD (Memory Write) is generated. At the clock pulse following entry to SC=15, a Memory Access Needed (MANF) is enabled which, in turn, generates MAND which is sent to core memory.

MAND initiates a standard memory cycle by starting the memory clock (MT0 - MT3). The next pulse sets the crosspoint flip-flops in Central Control connecting the I/O Control Unit to the Memory Module addressed (in this case Memory Module 0 or D13F-D15F=0).

MT0 (Memory Time = 0) is now true; and with the next clock pulse, the address of the desired core location is set into MAR (Memory Address Register) from information contained in D01F-D12F. The same pulse transfers the 48-bit Result Descriptor into MIR (Memory Information Register). The transfer of information into MAR and MIR is signaled by setting MA0F from the logic:

$$MA0F = MANF * (MWRD * MT0D + MAPS/)$$

MAPS/, in this expression, is concerned with maintenance operations and is not pertinent to this operation.

SECTION 2

CARD READER CONTROL

GENERAL

The purpose of this section is to describe the tie-in of the Card Reader to the B5500 I/O Channel. It is written with the assumption that the reader does not have a detailed knowledge of either the Central Control or I/O Control Exchange Channel logic. The intention is to enable a preliminary observation of the Card Reader operation from the I/O Channel, and thereby help to ascertain whether a malfunction is within the Card Reader or is external to the Card Reader. Sufficient detail is presented to enable operation of the I/O Channel and cause the reading of a card and the subsequent interrogation of the I/O Result Descriptor.

The following is a list of card readers compatible to the Model III Input/Output Controls:

B9110 or B122 - Card Reader 200 cards/minute.

B123 - Card Reader 475 cards/minute. B124 transport speed and stacker blower removed; electronics adjusted to card speed.

B9111 or B124 - Card Reader 800 cards/minute. B129 transport speed slowed down and stacker blower removed; electronics adjusted to card speed.

B9112 or B129 - Card Reader 1400 cards/minute. Electronics adjusted to card speed.

B9918 - Postal Money Order Feature is available on B123, B124 or B129.

INTERCONNECTING LINES

The Card Reader cables are plugged into Winchester type connectors which are located at the rear of the Display and Distribution panel. Two connectors are provided for Card Reader use; one labeled Card Reader-1, the other labeled Card Reader-2. It should be noted that if only one Card Reader is incorporated within a system, it must be plugged into the connector labeled Card Reader-1. This requirement is due to the fact that when a load operation is initiated (i.e., LOAD button is pressed with Select switch in Card Load position), the logic assumes a Reader plugged into the Card Reader-1 connector.

The interconnecting lines which make up the cable from the Card Reader, may, for discussion purposes, be sub-divided into three groups:

1. Power supply and power control lines
2. Information lines
3. Logical control lines; to and from the Card Reader

Figure 2-3 illustrates the Card Reader cable plugged into the Winchester connector at the rear of the Display and Distribution panel. The figure, as drawn, assumes the Card Reader plugged into the Card Reader-1 connector with I/O Channel #4 selecting (via I/O Exchange logic of Central Control) Card Reader-1.

POWER SUPPLY AND POWER CONTROL LINES

Six lines make up the power supply and power control lines (illustrated in Figure 2-3). The six lines are routed from the Winchester connector to the power control distribution unit which is located at the top rear panel of the Display and Distribution unit.

INFORMATION LINES

The information lines (CC1L through CCBL) are externally cabled to a connector at Display and Distribution and then into the I/O Exchange area of Central Control. The internal cables for the Card Readers from Display and Distribution to Central Control are numbered 17-1 and 17-2; corresponding to Card Reader-1 connector and Card Reader-2 connector, respectively. Figure 2-3 assumes a Reader plugged into Card Reader-1, hence cable 17-1 lines are illustrated. The information lines are gated through the I/O Exchange area to the requesting I/O Channel via the Unit Designate level; in the example illustrated, U10D from I/O Channel #4. On the D.A. Schematics, the mnemonics utilized by each I/O Channel to designate Card Reader-1 are I1U10D, I2U10D, I3U10D and I4U10D, respectively. Likewise, for Card Reader-2, the mnemonics are I1U14D, I2U14D, I3U14D and I4U14D.

The information lines CC1L through CCBL pass through drivers in the I/O Exchange area of Central Control. Thereafter, the names of the information lines become I01D through I06D. On the D.A. Schematics, the information line designation for I/O Channel #1 is I1I01D through I1I06D. Only one peripheral unit may be connected to any I/O Control Unit at any one time. The information lines I01D through I06D are gated, unclocked, into the Input Buffer (IB) of the designated I/O Control Unit.

If the Card Reader has been plugged into the Card Reader-2 Winchester connector instead of Card Reader-1, as illustrated, the information lines would have been gated through to the requesting I/O Control Unit via the level I4U14D (assuming I/O Channel #4 is the requesting Control Unit).

LOGICAL CONTROL LINES

The logical control lines from the Card Reader to the specified I/O Channel are gated through the I/O Exchange area of Central Control in a manner similar to the gating of the information lines. The levels $\overline{\text{CRL}}$, $\overline{\text{CCL}}$ and $\overline{\text{CREF}}$ are switched in Central Control to become CRS, CCS and CRES, respectively. The output levels from the drivers to the specified I/O Control Unit are I21D, I22D, I24D, I25D and I28D. (Figure 2-3)

The logical control lines which are sent to the Card Reader ($\overline{\text{SCCL}}$, $\overline{\text{CBIL}}$ and $\overline{\text{CBHL}}$) are gated through I/O Exchange of Central Control via the enabling level U10D or U14D; in Figure 2-3, the level U10D is illustrated.

LOGICAL DESCRIPTION

NOTE

All address cells in this section refer to absolute addressing which is octal base.

INFORMATION AND CONTROL

An I/O Control Unit, when it receives an initiate level from Central Control, obtains from cell 10 of Memory "0" the address of the I/O Descriptor. Then the I/O Descriptor is accessed and subsequently placed in the D register of the I/O Control Unit. Once the D register contains the I/O Descriptor, the unit designate field, in conjunction with D16F and D24F, specifies (in the case of a Card Reader Descriptor) Card Reader-1 or Card Reader-2. Note that D16F does not appear in the original Descriptor but is set as an internal function of the I/O Control Unit operation. D16F is set as a result of the I/O Control Unit ascertaining that the specified Card Reader is not busy; this enables the start of a Card Reader operation. The enabling level developed via the Unit Designate field, D16F and D24F is termed U10D for Card Reader-1 and U14D for Card Reader-2. This enabling level, U10D or U14D, effectively connects the Card Reader to the requesting I/O Control Unit through I/O Exchange in Central Control. Figure 2-3 illustrates I/O Control Unit #4 selecting Card Reader-1.

The initiation of a card feed occurs when the I/O Control Unit sets bit D26F, causing the Start Card Cycle "not" line ($\overline{\text{SCCL}}$) to go false. Once the Card Reader has been initiated as indicated by the level $\overline{\text{CCL}}$ going false, the D register bit D26F is reset. This removes the initiating start level to the Card Reader ($\overline{\text{SCCL}}$ goes true).

As each column of a card is read, the information lines are gated, unclocked, into the Input Buffer (IB) register. The column strobe pulse, going true, indirectly gates the transfer of a character from the IB register to the specified character position of the W register. The character positions of the W register are specified by the character counter which counts from 0 through 7. In the case of alphanumeric read, the BCL character code is converted to internal B5500 code in conjunction with the IB to W transfer. When a complete word has been assembled in the W register, a memory cycle is initiated to store the W register contents into the cell specified by the address field of the I/O Descriptor contained in the D register. As each word is stored into memory, the address field in the D register equals one greater than the last storage address. The memory storage of the W register contents occurs after the eighth character transfers to the W register and prior to the next character transfer to the W register. In alphanumeric mode, 10 words are stored. In binary mode, 20 words are stored.

In the event of a card read error ($\overline{\text{CREL}}$ goes false), bit D20F is set for subsequent indication in the Result Descriptor. For an END-OF-FILE condition, bit D21F is set in the Result Descriptor for EOF indication.

The D register bits D27F and D17F are utilized to determine the status of the level $\overline{\text{CBIL}}$ and $\overline{\text{CBHL}}$ to the Card Reader. The setting of D17F is an internal logical function of the I/O Control Unit. In the binary mode of operation, D17F, when set with the trailing edge of the column strobe pulse (CSP), results in the level $\overline{\text{CBHL}}$ going true for subsequent reading of the lower half of a column. In this case, the I/O Control Unit developes its own sync to gate the transfer of a character from IB to the W register.

I/O CONTROL PANEL CONTROL

Reading a Result Descriptor

A function of the I/O Control logics is to construct an I/O Result Descriptor which is stored in memory. I/O Control Unit #1 stores its result descriptor in cell 14.

Unit #2 in cell #15, Unit #3 in cell #16, and Unit #4 in cell #17. If it is desired to manually interrogate the I/O Result Descriptor, following an I/O operation, the following procedure may be utilized:

1. Place the I/O Control Unit in the local status.
2. Place the appropriate descriptor address in the address field of the D register.
3. Place the Memory Cycle switch in the memory cycle position (UP).
4. Insure that the system clock is running.
5. Press the I/O Channel START button.

The word addressed by the 15 low order bits of the D register will be brought to the W register where interrogation may be accomplished. The interpretation of the various bit positions is as follows: (See Figure 2-1)

Bits 48 through 46 - These bits are all off in the Result Descriptor

Bits 45 through 41 - Unit designate; 24 for Reader-1, 34 for Reader-2

Bits 40 through 23 - Bits 24 and 27 retain their original status; remaining bits will be reset

Bits 15 through 01 - Core storage address of last word stored plus one

Bit 16 - If set indicates designated unit (Card Reader) was not busy

Bit 17 - Descriptor Parity Error; either on access of Descriptor, or address of Data Descriptor

Bit 18 - Designated unit (Card Reader) was ready

Bit 19 - Set if invalid character sensed by IB

Bit 20 - Read check error; set by CREL from the Reader

Bit 21 - End-of-File; set by EOFL from the Reader

Bit 22 - Memory address error; memory overflow of non-existent address

Initiating a Read

The initiation of a card read cycle may be accomplished from the I/O Control Unit. The procedure to be described requires that an I/O Descriptor be constructed in the W register and stored in memory. Thereafter, the address at which the I/O Descriptor was stored is placed in cell 10 of memory. The card read I/O operation may then be initiated. The complete procedure to be followed is given below:

STEP 1 - Construct I/O Descriptor and store

1. Place I/O Channel in the local status

2. Construct I/O Descriptor in the W register

3. Place address at which it is desired to store descriptor in the D register

4. Set D register bit D24F to specify memory write operation

5. Place Memory Cycle switch in memory cycle position (UP)

6. Insure system clock is running

7. Press the I/O Control Unit START button

STEP 2 - Store Address of I/O Descriptor in Cell 10

1. Place address at which I/O Descriptor was stored in W register

2. Place cell address of 10 in the D register

3. Set D24F to specify memory write

4. Press I/O Control Unit START button

STEP 3 - Initiate I/O operation

1. Place the Memory Cycle switch in the down position

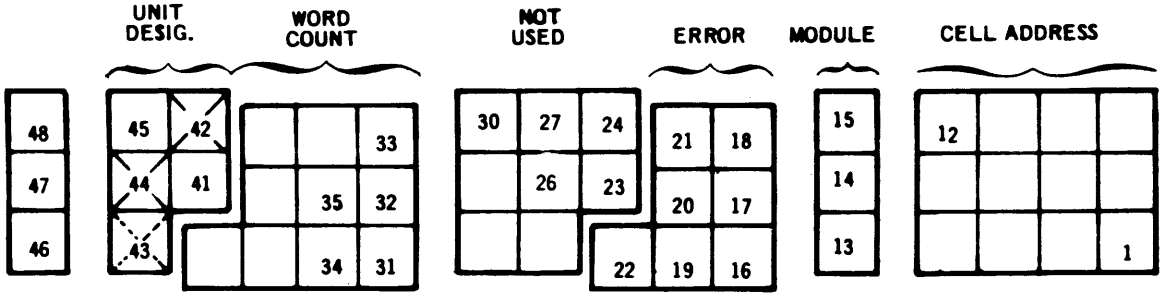
2. If desired, to perform repetitive card read cycles, place the Recycle switch UP; otherwise, leave it down

3. Press the I/O Control Unit START button

Upon completion of STEP 3 the I/O Channel will cause the card read cycle to take place. The I/O Result Descriptor may then be interrogated by the procedure previously described.

Error Stop

If repetitive card read cycles are initiated via the Recycle switch being placed in the UP position, the Error Stop switch may also be placed in the UP position. Utilizing this procedure, cards will continue to be fed (provided cards in the hopper and stacker not full) until an ERROR is detected in the Result Descriptor.



Card Reader #1 octal designation 0 24 000 004 00 m aaaa

Card Reader #2 octal designation 0 34 000 004 00 m aaaa

Card Reader I/O finished
Result Descriptor (no errors) 0 24 000 004 00 m (aaaa + 13 or 25) Ø

FIGURE 2-1 CARD READER DESCRIPTOR

DETAILED DESCRIPTION OF OPERATION CONTROL

NOTE

Use the Standard Flow and the Card Reader flow in conjunction with this writeup. See Figure 2-4.

Sequence Count Equals Zero (Standard Logic 1.01)

Obtain Descriptor Address. The Admit Descriptor level (ADnS-C) sets D17F to one and D04F to one. The latter operation establishes memory address 10 as the location to be accessed. D17F with Memory Access Obtained Flip-flop off ($\overline{\text{MAØF}}$) allows Memory Access Needed Flip-flop (MANF) to be set. This initiates a memory read cycle which sets the Data Descriptor address into Memory Information Register (MIR). When MAØF is set by Memory Access Needed and Memory Timing Two Driver, MANF will be reset and also Memory Information Strobe drive (MISD) will place the information into the W register. With $\overline{\text{MANF}}$, reset MAØF; with $\overline{\text{MANF}}$ and MAØF, count Sequence Counter up one.

Obtain Descriptor. With $\overline{\text{MAØF}}$ and D17F (from SC = 2), set MANF. Since the above operation placed the address of the descriptor in D, this memory operation brings up the descriptor. When MAØF is set, MISD will place the word in W and MANF is reset. With MANF, reset MAØF and count the Sequence Counter up one.

If there is a Memory Address Error (MAED-C), set D22F and reset MANF, and if there is a Memory Parity Error (MPED-M), set D19F.

If a card load cycle is to be initiated, the switch on the Operator's Console must be in the Load Card position, (LØCL-C) and when the LOAD pushbutton is depressed, the Load Timing switch (LØTS-C) initiates the setting of Sequence Counter to 3, setting D24F to signify a read, setting D27F to read in binary mode, and D05F to place the first word read in memory location 20. With LØCL-C, D44F and D42F set, this designates a Card Reader Unit. From this point on, the Card Reader flow is normal.

Sequence Count Equals One (Standard Logic 1.01)

If previously detected error conditions exist, set Sequence Counter to 14 and clear "W", if not, clear "D" and count Sequence Counter up one.

Sequence Counter Equals Two (Standard Logic 1.10)

Unconditionally, complement the External Control Flip-flop (EXNF) and place the contents of the "W" register in "D" register. If the address is being transferred (first time through), $\overline{\text{EXNF}}$ will set D17F and set the Sequence Counter to zero. Memory Access Permitted switch output will clear the "W" register in remote operation. If the descriptor is being transferred (second time through), W goes to D and EXNF is reset but Sequence Counter is counted up one. The Longitudinal Parity Decade (LP [B➡1]) is not used during the card read operation.

GLOSSARY OF I/O TERMS:

D17F	During the binary card cycle, it is used to indicate to the Card Reader which half of the card column is needed by the I/O Unit.
D19F	If an invalid character should be read from a card, this flip-flop remembers it. It is part of the Result Descriptor
D20F	If a Card Reader Error Level has occurred during the card read cycle, this flip-flop is set for this indication in the result descriptor.
D21F	If an End-of-File condition is initiated in the Card Reader, this flip-flop remembers it.
D31F➡D40F	These flip-flops are part of the D register. They make up the Word Counter for all operations. The Card Reader operation uses D31F➡D35F only.
EØFL	End-of-File Level - This level is sent to the Central Control Unit when an End-of-File condition exists in the Card Reader. This level comes from the Central Control in the I/O Unit as I23D.
HØLF	Hold Over Flip-flop - Used to allow only one group of actions to take place for any one CSP during alpha card read. Allows two groups of actions to take place for any one CSP during binary card read.
I01D➡I06D	These are the 6 drivers in the Central Control Unit that send across the six information bits of a character to the I/O Unit.
LCHF	Last Character Flip-flop - This flip-flop is used to cause the Result Descriptor to be sent back to Core Memory. Also causes the Read Error Flip-flop (D20F) to be set. This flip-flop is set only when a card has been read, but all 80 CSP's were not received in the I/O Control Unit.
LØCL-C	Load Card Level - Derived from a toggle switch, used to cause a card read operation. The card is read binary mode.
LØTS-C	Load Timing Switch - Used to initiate a card read cycle or an operation.

SCCL Start Card Cycle Level - Sent to the Card Reader by Ø21D at SC = 3 if the Card Reader is not busy and is ready.

STRF Strobe Flip-flop - This flip-flop is used for control purposes in the I/O Control Unit. It is turned on with every CSP from the Card Reader in alpha mode, twice in binary mode.

GENERAL DESCRIPTION OF OPERATION

The function of the I/O Control Unit for a card read operation is to provide the external logics necessary to read a punched card in either alphanumeric or binary mode with either the 200 CPM, 800 CPM or the 1400 CPM Reader.

Information is read in from the card serially, by column, starting with column one. The word is formed in the W register of I/O Control, with the most significant character first. Memory is counted up as each word is stored. In alphanumeric mode, one card column reads in as one character and eight characters fill one word in memory, making a total of ten words from one card. In binary mode, each column of the card makes two characters, four columns make one word and twenty words make one card. The upper half of the column is the most significant character of the two characters. Any unpunched column of the card is read as a binary zero.

When the object program finds that the memory area designated for input information is empty, the Master Control Program (MCP) will call for a Data Descriptor to fill this area in memory from the Card Reader. The Unit Designate Field of the Data Descriptor (bit positions 45 ➡ 41) designates the Card Reader. If there are two Card Readers on the system, it also designates which one. Unit designate number (octal) 24 is for Card Reader #1, (octal) 34 is for Card Reader #2.

When the MCP finds the Data Descriptor for the Card Reader, it will store the address of the descriptor in cell (octal) 10. At the same time the Processor will signal the Central Control that an I/O operation is needed. Central Control will signal the lowest numbered I/O Unit which is not busy, to access cell 10 for the address of the Data Descriptor. This action will initiate the I/O Control into action to load from the Card Reader the requested area in memory.

BASIC FLOW

The card read sequence of operations is shown in Figure 2-2, while a general block diagram of signal and control paths is contained in Figure 2-3.

SC = 0, 1 & 2: Operation initiated by ADNS or LØTS signal from Central Control. Two memory accesses are performed:

1. Read Descriptor Address from Memory cell 10
2. Read Descriptor from Memory

SC = 3: Interrogate peripheral unit trunk, Designate peripheral unit, and interrogate peripheral unit's status (READY - BUSY).

SC = 8: Transfer information presented by Card Reader into "W" (Word) register. Alpha cards present 10 words of 8 characters each; Binary cards present 20 words of 16 octads each as each character on the card fills one octade.

SC = 9 & 10: Access Memory and transfer the Data Word accumulated in the W register to memory. Index the Word Counter and Address Counter.

SC = 14: Shift Result Descriptor.

SC = 15: Transfer Result Descriptor to Memory and clear I/O Unit.

SEQUENCE COUNT EQUALS THREE

There are two parts to this count; the first box is located within the standard sequence counts (1.01), and the second is located on the Card Reader flow (4.01).

The Character Counter is utilized in this area to maintain a controlled delay, while waiting for the Card Reader to become available and ready to read information.

STANDARD LOGIC (1.01)

As long as the 4's bit of the Character Counter is not set, the CC + 1 stays active. This allows the counter to count to four before delay logics become active.

CHARACTER COUNTER EQUAL ONE

Through the AUNS logic of Central Control, interrogate the other I/O Units to see if they are using the Card Reader at this time. If they are not, set D16F to indicate "No conflict present". This will initiate the connection of the Card Reader to the I/O Unit through the Central Control Unit.

CHARACTER COUNTER EQUAL TWO

This count is used only to allow the connection of I/O to the Card Reader to quiescent voltages before further interrogation is started.

CHARACTER COUNTER EQUAL THREE

D41F is set only for magnetic tape operation. The only logic of use here is for interrogation of the Unit Ready status, via I21D level which is the CRL level in the Card Reader. If I21D is true, then D18F is set to signify that the Card Reader is ready to read cards.

CHARACTER COUNTER EQUAL FOUR

At this point the I/O is ready to make a decision; to start feeding the card in the Card Reader or to initiate a delay for the Card Reader to finish a previous cycle.

A no error condition will allow the CC1F flip-flop to be set (CC = 5) and branch to Card Reader flows (4.01) for Reader operation.

The set of CC2F to one indicates that the Card Reader is; available, by D16F being set, and ready, by D18F being set. But at this time, Card Cycle Level (CCL) from the Card Reader is still true from the previous operation. The level CCL being true causes UBZS to be true, as the logics are:

$$UBZS = \overline{D41F} \cdot \overline{I22S}$$

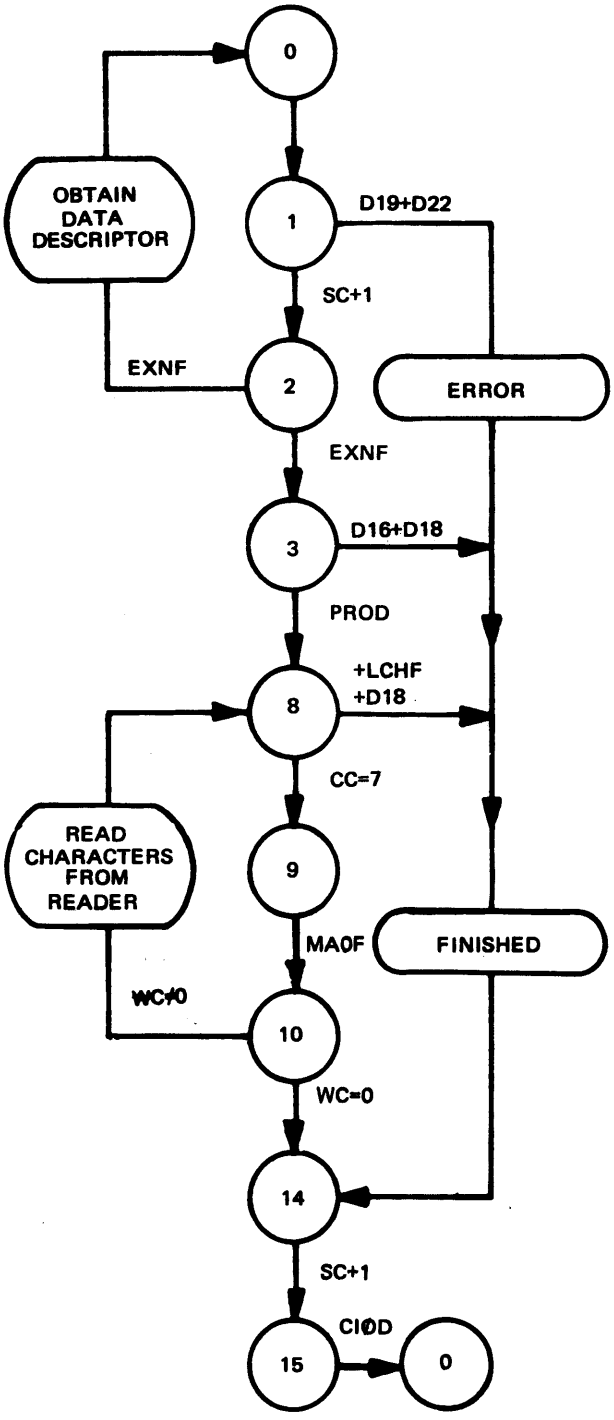


FIGURE 2-2 SEQUENCE COUNT CHART

If UBZS is true, the following action takes place. CC1F and CC2F will be set at the same time. This sets the Character Counter to seven. The next clock pulse will reset CC1F and the logic will remain here at CC = 6 until CCL in the Card Reader goes false and, in turn, UBZS goes false, resetting CC2F, which will make the Character Counter equal to five. This enables the logics on Flow Chart 4.01 (Card Reader Flow).

CHARACTER COUNTER EQUAL FIVE (CARD READER FLOW)

The top three lines in this box are for the cases where D16F or D18F are not set in the previous boxes. These flip-flops being not set indicate that the Card Reader is not available or not ready, therefore, clear the IB and the W register of I/O and prepare to construct a Result Descriptor to indicate this to the MCP.

PROD will be true if D16F and D18F are set with CC = 5 and SC = 3. This will enable the logics to proceed, set D25F to enable the Word Counter logic. Set D26F to bring SCCL true to the Card Reader for a start operation. At the same time the Character Counter will be set to zero to point to the first character in the W register, the Word Counter will be set to ten if the word is to be read in the alpha mode or to twenty if in the binary mode. The Sequence Counter will be set to eight to prepare for the incoming information.

SEQUENCE COUNTER EQUALS EIGHT

Setting D26F at SC = 3 signalled Central Control that I/O was prepared to accept information. It initiates a card cycle via Start Card Cycle Level output (SCCL is positive). Soon after (10μs) the Card Cycle Level is available ($\overline{CCL}$ is positive, I22D) and SCCL output goes negative. A time delay ensues until the card is under the reading station and the Reader can read and decode the outputs from the photocells sensing the card column. The outputs are sent to Central Control as Column Character Lines (CCnL's) and sent to I/O as I01D ➡ I06D.

These are available at the Input Buffer Flip-flops (IBnF's) a long period before the Column Strobe Pulse (CSP) is developed. The CSP is sent to Central Control and reestablished as I24D to the I/O Unit. With this output, the IBnF's are set by CCnL's. The CCnL's are either BCL alphanumeric or straight binary depending on the D27F bit configuration in the descriptor (D27F = 0, alphanumeric; D27 = 1, binary).

When I22D is true, a card is being passed through the Reader. Holdover Flip-flop has not been set ($\overline{HØLF}$) which indicates the information now available has not been sensed by the I/O. I24D is the Column Strobe, the timing pulse for the information present. These conditions set the Strobe Flip-flop (STRF). When STRF comes on, along with the condition $\overline{HØLF}$, the InnD's, D24F bit on indicating a read, Drum Operation Switch (not) ($\overline{DRØS}$) which says this read is not from drum and D41F off ($\overline{D41F}$), indicating this is not tape read; the set of IBnF's occurs unclocked. One pulse after STRF is set, STRF along with D41F causes the Holdover Flip-flop (HØLF) to be set. With both STRF and HØLF, the IBnF's are reset, the Character Counter (CC) is counted up one and STRF is reset. At the same time, these conditions along with the Character Counter at some value 0 ➡ 7, Memory Access Permitted switch and D24F; the IBNF configuration is transferred into the W register in the character position indicated by the Character Counter. If the IBnF's equal zero, D27F is off, indicating alphanumeric translation, and D24F is on, for a read operation; an invalid character was sensed in the Reader. This error is flagged by setting D19F to one in the Result Descriptor.

If the Card Read Error Level (CREL) initiates I25D, D20F will be set to one to flag the error in the Result Descriptor.

In binary mode (D27F On) D17F is complemented. The first character transferred found D17F off and the character information was from the six upper rows in the column. The character was gated by the Card Binary level sent to the Reader by Central Control (CBIL = 022D - D27F • DROD. CROD is the Card Reader Operation Driver) and Card Binary Half level (not) ($\overline{\text{CBHL}}$). This decoding looks at only the binary significance in terms of the bits. D17F On will allow a second setting of Strobe Flip-flop after Holdover Flip-flop is reset. In alphanumeric, only the CSP (I24D) sets STRF. In binary, STRF is set twice. D17F On, gates Card Binary Half Level into the Reader (CBHL = 023D = CROD • D17F). This level is present at the gates in the Reader decoder to cause only the bottom six rows to be sent I/O information drivers. The information set into IBnF's is placed in the W register by the method already described. Note that invalid character error checking is inhibited in binary by D27F.

The reset of HØLF occurs when the CSP vanishes. Since no further reading can occur (unless STRF is set specially, as above) when the CSP is gone and it will not reappear until new information is available, each character (or pair of characters) is read in sequential order, until the Character Counter is seven. At this time the eighth character is read, placed in W and the Sequence Counter is set to 9.

If a read error is detected (Card Read Error Level is available through I25D) D20F is set as a flag in the Result Descriptor. If the Card Reader loses the Card Ready Level (CRL), this condition is signalled by $\overline{\text{I21S}}$. If not reading a character ($\overline{\text{STRF}}$ • $\overline{\text{HØLF}}$), and I21S condition is true, reset D18F to flag the not-ready condition in the Result Descriptor, also use it to set Sequence Counter to 14 and with Memory Access Permitted (MAPS), clear W.

If the Word Counter is not zero or the Character Counter is not zero when the Card Cycle Level goes positive ($\overline{\text{I22S}}$) (meaning it has finished passing a card through the Reader) and D26F is off (indicating that a cycle has been initiated), one or more CSP's was missing for that card, so set the Last Character Flip-flop (LCHF). On the next pulse set D20F to flag this error in the Result Descriptor. Also, set Sequence Counter to 14 to exit the operation. With Memory Access Permitted, clear W.

SEQUENCE COUNTER EQUALS NINE

When Sequence Counter is 9, with Address Overflow Flip-flop off ($\overline{\text{AØFF}}$) and Word Counter not zero, set Memory Access Needed Flip-flop (MANF). At the same time, with D25F on (use Word Counter) and MANF, count the Word Counter down one. With MANF, Memory Write Driver (MWRD = [SC = 9] • D24F) and Memory Timing Zero Driver, MANF, Memory Write Obtained Flip-flop. With MAØF set, reset MANF, count the Sequence Counter up one and along with D24F (read) and Memory Access Permitted, clear W. MWRD will reset MAØF. The word in W was written into Memory.

If any address errors had existed for the address designated, Memory Address Error (MAED-C) and Memory Access Permitted (MAPS) would have reset MANF, set D22F to flag this in the Result Descriptor and count Sequence Counter up one.

If an Address Overflow had occurred earlier, AØFF with D24F (read) would count Sequence Counter up one, along with Memory Access Permitted, clear W and set D22F as above.

If the Key Memory Switch in Central Control is in the Key Memory position (UP), the Key Memory Switch Level (KEML) output is true and the Memory Cycle switch is true with MANF off; the output of the D to W shift driver (DWSD) will be true, which will place D register contents into W register.

SEQUENCE COUNTER EQUALS TEN

If D24F is on (read) and Word Counter is not zero, set Sequence Counter to 8 and read the next word. If Word Counter is zero, all of the cards have been read, set Sequence Counter to 14. If the operation is not Printer (PTOS) and not Tape ($\overline{D41F}$), and the 15 bit address field of D is not all ones; count the field up one to store the next word in the next higher location. If the address field of D is all ones, set the Address Overflow Flip-flop.

If in local operation and the Memory Cycle switch is true (UP), set Sequence Counter to zero to start the cycle again. If the Recycle Flip-flop is on with no address overflow, set IMCF to cycle continuously through to this point.

SEQUENCE COUNTER EQUALS FOURTEEN

D register is transferred to W register. The bits 15 through 1 of the D register are cleared to allow the setting of an address for the Result Descriptor storage location. D04F and D03F bits are always set. I/O Channel one clears D02F and D01F, resulting in an address of 12. I/O Channel two clears D02F and sets D01F for an address of 13. I/O Channel three sets D02F, and clears D01F, so its address is 14. I/O Channel four sets both D02F and D01F, which is 15.

If D16F and D17F had both been off, set W16F to show that the unit was busy. If D16F had been on but D17F and D18F were both off, set W18F to show that the unit was not-ready. The Sequence Counter is then counted up one.

SEQUENCE COUNTER EQUALS FIFTEEN

Unconditionally set MANF to initiate the write in Core Memory of the Result Descriptor. When Memory Timing Zero Driver output with Memory Write Driver output comes true, set MAOF. With MAOF, set all I/O flip-flops to zero except W (CIOD); and clear W if MAPS is true. The conditions of remote, MAOF and SC = 15 cause the output of Finished Driver (FIND) to be sent to Central Control.

If in local ($\overline{REMF}$) with Recycle Flip-flop On (RECF) Memory Access Obtained (MAOF) turn on IMCF to enable the Reader to repeat the cycle.

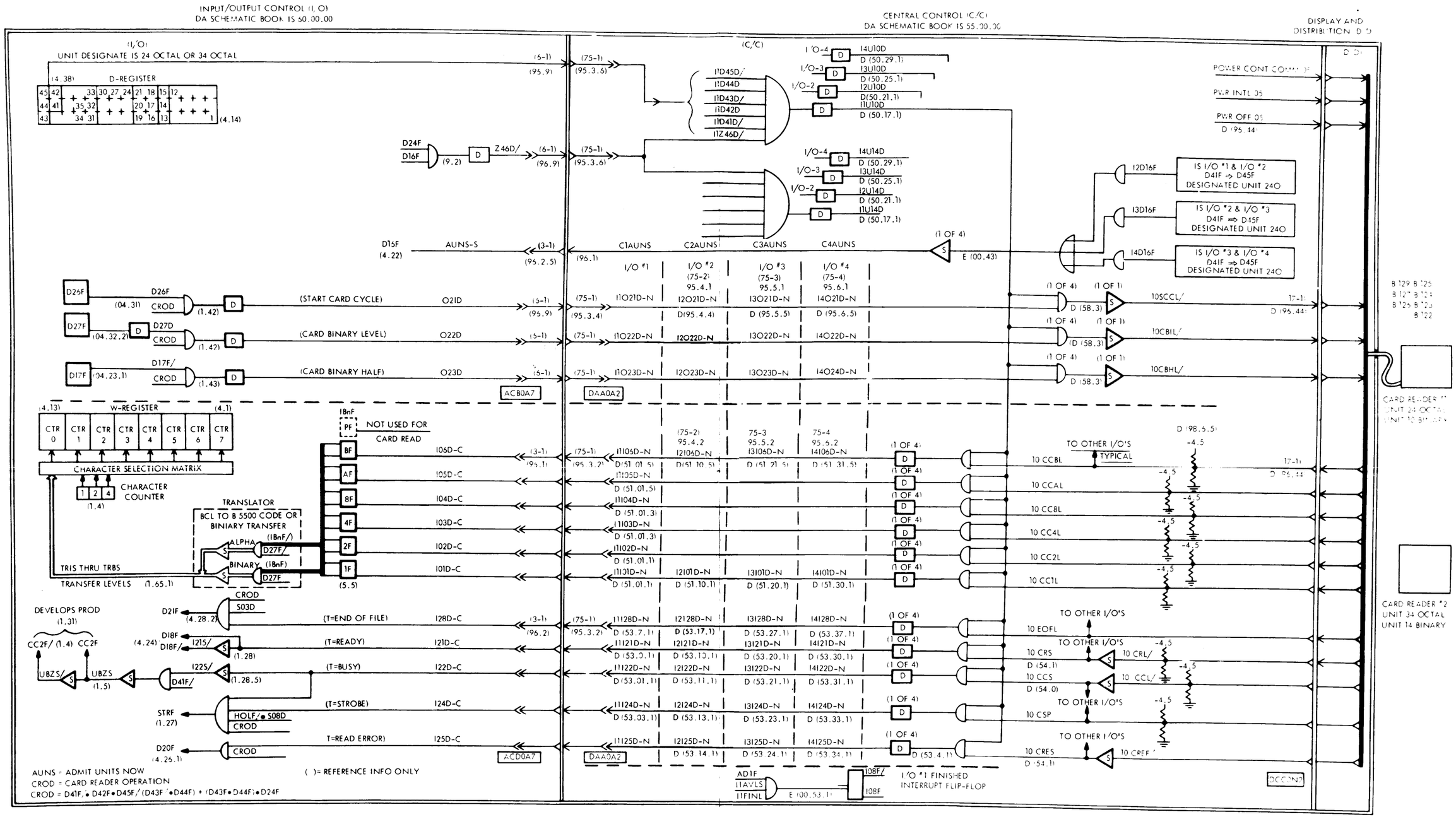


FIGURE 2-3 CARD READER INFO & CONTROL PATH

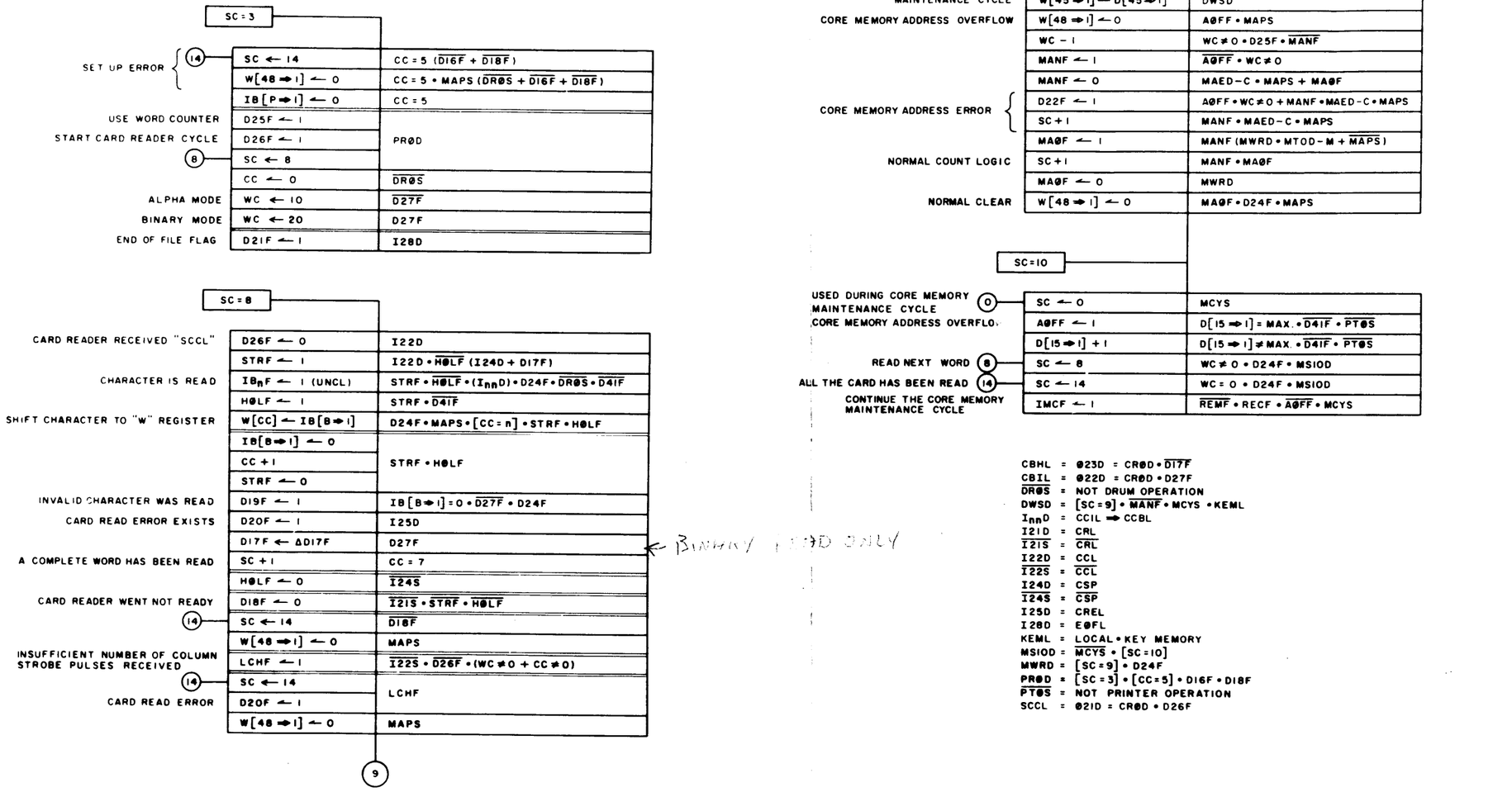


FIGURE 2-4 CARD READER FLOW

SECTION 3

CARD PUNCH CONTROL

INTRODUCTION

The Input-Output (I/O) Control is a multi-purpose control and buffer which provides the information link and external control necessary for any one of several peripheral devices. This section is devoted exclusively to the necessary information transfer and control of the Card Punch Unit.

The information word is read in parallel from the Memory Module to the W register, located in the I/O Unit. Here it is analyzed with incoming signals from the Card Punch and the information is decoded and read into the Punch Buffer Register serially for each row of the card. After this word is decoded and read into the Punch, the I/O Unit will request another word from Memory and this word is decoded and punched. This continues until the contents of 10 words are analyzed for each row and punched into the card. Since there are 12 rows on the card, this required 120 memory cycles to punch one card. The Punch, being a comparatively slow device compared with the Processor, allows memory cycles of the I/O to be integrated with the Processor memory cycles without hindering normal Processor operation.

This section is not written to provide complete training on the I/O Unit. Any circuit or logic which deals with a memory unit or another peripheral unit is deleted where possible. The purpose of this section is to familiarize the student with the necessary logics and information to operate the Card Punch from the I/O Display Panel, located in the Display and Distribution Cabinet. A basic description of the information flow through the Central Control Unit will be given, however, any extensive troubleshooting will require someone who has been completely trained on this unit.

The following is a list of card punches compatible to the Model III Input/Output Controls.

B9210 or B303 - Card Punch 100 cards/minute

B9211 or B304 - Card Punch 300 cards/minute

B9212 - Card Punch 150 cards/minute

B9213 - Card Punch 300 cards/minute

CARD PUNCH OPERATION

When the MCP receives instruction from the object program for a Card Punch operation, it will start the I/O with an "Initiate I/O" operator. This operator will develop CMTL (Commence Timing Level) and CMIL (Commence I/O Level) in the Central Control Unit. Here it is used to select the lowest numbered I/O Control Unit available to the system. If number 1 I/O Unit is busy it will select number 2, etc. When an I/O Unit is found available and ready, the Central Control Unit will develop a level called ADNS (Admit Descriptor Now). The I/O Unit senses the ADNS level going true and sets a 10 into the address area of the D register (D01F ⇒ D15F) and MANF to request a memory cycle. This will read the word from cell 10 of Memory Unit #0 into the D register. This word is the memory address of the I/O Descriptor which in this case will be for a Card Punch. Another memory cycle follows which loads this Descriptor into the D register, via the W register. This descriptor contains

the Unit Designate of the peripheral unit which for the Card Punch is #10 and D24F off. If D24F was on, it would designate a Card Reader #1. Also, the Descriptor contains the base location of the address in memory where the information to be punched is located. The punching will start from this cell and punch the words found in the next nine cells.

As soon as the descriptor arrives in the D register, Central Control analyzes the unit designate coding and prepares to connect the Card Punch to the I/O Unit through the I/O Exchange Matrix located in the Central Control cabinet. Since it is quite possible that the Card Punch could be punching from another I/O Unit, the Central Control Unit will check for this and if the Card Punch is busy, will notify the I/O Unit by holding AUNS (Admit Units Now) false. This will cause the I/O Unit to terminate the operation and notify the MCP that the Card Punch was busy. A similar flow exists if the Card Punch was found to be not available or not ready.

When the I/O Unit that caused the Card Punch to be busy completes its punch cycle, it notifies the MCP and the MCP will again initiate the I/O Unit to start the Punch and punch the information called for in this descriptor.

The initiating operation will be repeated, except this time the AUNS level will be true. This will set D16F in the I/O Unit, which is the final gating in the I/O Exchange area of Central Control, to connect the Card Punch to the requesting I/O. The I/O Unit will request the first word from the Memory cell whose Address is designated by the I/O Descriptor. This word is read into the W register of I/O and the Card Punch is started. The information of this word is analyzed to see if there are characters which require "12" row holes in the card. As each character is analyzed by the decoder, a single bit level is developed which is sent from the OB1F (Output Buffer #1) through the Central Control I/O Exchange area to the Punch Buffer flip-flops located in the Card Punch. If a "12" row punch is needed, the flip-flop is set. If the punch is not needed, the flip-flop is off. This information is set into the buffer serially and the buffer is shifted laterally for each character in the W register. When the contents of one word has been analyzed, the next word in memory is set into the W register and the Character Counter is reset to zero to analyze the first character of the new word. After the tenth word has been analyzed, the Card Punch Buffer Register will have received 80 lateral shifts. The flip-flop setting for the first character analyzed will be the state of the first column flip-flop. Now the Punch will punch the holes in the card for the "12" row of the card. The card will be advanced one row, the I/O will request the memory for the first word again and the process will be repeated to decode the necessary punches for the "11" row of the card. This process is repeated for each row of the card until the "9" row is decoded and punched.

This completes the punching of one card. The I/O Unit will develop an I/O Result Descriptor, read it into the memory MCP area and signal the system that it is finished by setting an I/O Finished Interrupt. The Card Punch is now dropped from the I/O Unit and the I/O registers are cleared, ready for another I/O request from the MCP

GLOSSARY OF TERMS

AOFF - Address Overflow Flip-flop - When this flip-flop is set, it indicates that the memory address in the D register has exceeded the memory capacity.

CPØD - Card Punch Operation Driver - When D41F ➡ D45F is set to binary 10 and $\overline{\text{D24F}}$, this level is true.

CPTD - Card Punch Timing Driver - This level is a composite of several levels necessary to transfer an information bit to OB1F.

D Reg. - This register is located in the I/O Unit and is used to store the I/O Descriptor for logical functions during the operation.

D17F - During the Punch Cycle, this flip-flop is used to indicate the information for the last row has been sent to the Punch Unit.

D20F - This flip-flop is set by PUEF from the Card Punch when an error has occurred during a previous punch cycle.

D26F - When this flip-flop is set, it indicates that SPØL (Start Punch Order Level) is being sent over to the Punch Unit via Central Control to start the Punch.

D31 ➡ D40F - These flip-flops are used to make up the Word Counter for all operations. The Card Punch operation only uses D31F D34F for a word count of 10.

D01F ➡ D15F - These flip-flops are used to make up the Memory Address of the next word in memory. Positions D12F D15F indicate the memory modules where the address is located.

D16F - This flip-flop must be turned on to allow Central Control to complete the connection of the I/O Unit to the peripheral unit. This flip-flop is set at sequence Count of 3, in standard logic. D16F in the Punch Descriptor selects the auxiliary stacker.

D18F - This flip-flop is set at SC = 3 and CC = 3 if PURL (Punch Unit Ready Level) is true from the Card Punch Unit.

HØLF - Hold-Over Flip-flop - This is used with STRF for control purposes.

EXNF - During SC = 1, 2 or 3, this flip-flop indicates whether the word in memory is the descriptor address or the descriptor word. During a Card Punch operation, it is used to recognize the PINL level from the Punch Unit.

LPnF - Longitudinal Parity 1 ➡ P flip-flops - LP1F is used during the Card Punch operation to retain the Punch Auxiliary Stacker Select Level.

MAØF - Memory Access Obtained Flip-flop - This is used to indicate that a memory cycle for this I/O is completed and the I/O Unit may continue its operation.

MANF - Memory Access Needed Flip-flop - This is used to indicate that a memory cycle for this I/O is needed.

MAPS - Memory Access Permitted Switch - When this switch is up, the memory cycle is inhibited. When down, the memory cycle is permitted.

MCYS - When this switch is in the up position, it allows only sequence count 0, 9 and 10.

MISD - Memory Information Strobe Driver - This is used to read memory information into the W register.

MPED - Memory Parity Error Driver - When this level is true, it indicates that the memory had a parity error during normal access of information.

ØB - Output Buffer - This consists of six flip-flops and a parity generator. Card Punch operation used ØB1F only.

PASL - Punch Auxiliary Stacker Level - This level is sent to the Punch Unit by Ø26D and when true indicates the card being punched will be sent to the auxiliary stacker.

PINL - Punch Information Needed Level - This level is from the Punch Unit through I27D in the Central Control and is a request for more information from the I/O Unit.

PC - Pulse Counter - The Pulse Counter counts at a one megacycle rate and is used to divide down the 1 MC clock to some predetermined rate. For the Card Punch the count is 14, which provides a 66 KC recycle rate.

PRAL - Punch Row Group A Level - A row level from the Card Punch via Central Control driver I23D.

PRBL - Punch Row Group B Level - A row level from the Card Punch via Central Control driver I24D.

PRCL - Punch Row Group C Level - A row level from the Card Punch via Central Control driver I28D.

PRDL - Punch Row Group D Level - A row level from the Card Punch via Central Control driver I26D.

PROD - Proceed Driver - This level indicates that the peripheral unit is available and ready, so proceed with the operation.

PUCL - Punch Unit Cycle Level - This level comes from the Punch Unit via I22D in Central Control and when positive indicates a punch cycle is in progress.

PUCP - Punch Unit Clock Pulse - This is a 3 μs pulse sent to the Punch Unit by Ø25D. It occurs at PC = 9, 10 and 11.

PUEF - Punch Unit Error Flip-flop - This level comes from the Punch Unit via I25D in Central Control. It indicates an error in a previous Punch operation.

$\overline{\text{PURL}}$ - Punch Unit Not Ready Level - Produced by I21S of the I/O Unit. This level is true when the Punch Unit is not ready.

REMF - Remote Flip-flop - When this flip-flop is set, it indicates to Central Control that the I/O Unit is available to the system.

SPOL - Start Punch Order Level - Sent to the Card Punch by ø24D at SC = 3, by the set of D26F in I/O.

STRF - Strobe Flip-flop - This flip-flop is used for control purposes in the Input/Output Control Unit. It is turned on once every 15 μs by the Pulse Counter equal to 14 during the Card Punch operation.

W Reg. - This register is used as a buffer to hold the punching word from the memory unit for the Card Punch

INTERCONNECTING LINES

The Output Drivers, located in the I/O Unit, and the Input Drivers, located at the Central Control Unit, are drivers which drive the control levels through the Central Control I/O Exchange to the interconnecting unit. There are eight Input Drivers and seven Output Drivers. They are not all used for the Card Punch. Those that are used are listed below:

Output Drivers

ø24D	SPOL - Start Punch Order Level
ø25D	PUCP - Punch Unit Clock Pulse
ø26D	PASL - Punch Auxiliary stacker

Input Drivers

I21D	PURL - Punch Unit Ready Level
I22D	PUCL - Punch Unit Cycle Level
I23D	PRAL - Punch Row Group A
I24D	PRBL - Punch Row Group B
I25D	PUEF - Punch Unit Error Level
I26D	PRDL - Punch Row Group D
I27D	PINL - Punch Information Needed Level
I28D	PRCL - Punch Row Group C

Information Drivers

ØB1F	Output Buffer One Level - Used for information decoded bit to punch.

LOGICAL DESCRIPTION

In order to understand the logical flow the student must understand the general information flow of the B5000 Processor. The I/O operation is independent of the Processor Unit. The only point in common to the two units is the Memory Units. When the Processor needs information it will advise the Central Control Unit, which will initiate an I/O Unit to fill the vacancy in memory. At this time the Processor is released from the operation while the I/O Unit continues the loading of this section of memory. This same sequence is utilized to read out of memory on a Punch operation.

CARD PUNCH INFORMATION AND CONTROL FLOW

Figure 3-1 is a diagram for the basic flow of information and control to the Card Punch. The I/O section shows the relative location of the W and the D registers, as

well as the basic logical boxes necessary to decode the characters into information compatible to the Card Punch.

The center section of the drawing shows the necessary gating in Central Control to connect the I/O Unit to the Card Punch. The same connection is used with either the B303 or B304 Punch. The information and control lines from Central Control gating lead to the Display and Distribution cabinet where they terminate at a Winchester connector. At this terminal, either the B303 or B304 Card Punch can be attached. This connector is only used for the Punch as separate connectors are used for the Card Reader, even though it uses the same unit designate number.

Information to and from the memory IB register can only be handled through the W register. During the request for the I/O descriptor, the descriptor is read into the W register, then transferred into the D register. The information words are read into the W register where they are stored for decoding into the Punch Unit. The W register is a 48 bit register, while the D register has only 45 bits. The information word in the W register is sub-divided into eight characters of six bits each.

These characters are read one at a time reading from the left to right of the register through the Routing Matrix box and the Alpha encoder into the Card Punch Decoder network. The Routing Matrix is a network which compares the output of the W register with the number located in the Character Counter Register. When this register has a zero in it, the Routing Matrix network will read the first character in the W register into the Alpha and Punch Decoder matrix. When the Character Counter reads a seven, the eighth character is read into the Decoding Matrix.

The Card Punch Decoder is a network which compares the card row of the Card Punch Unit with the character in the W register pointed to by the Character Counter and decides if the Punch should punch a hole in the corresponding column in the card. If a hole is needed, the output of the decoder is true. This sets the ØB1F Flip-flop of the Output Buffer Register. ØB1F level is switched in Central Control to $\overline{\text{PBCS}}$ to the Card Punch. The Card Punch signals to the Decoding network come in through the I23D, I24D, I26D and I28D lines. These lines correspond directly with the PRAL, PRBL, PRCL and PRDL levels in the Punch Logics.

CENTRAL CONTROL

The Central Control logics necessary for Card Punch control are shown on Figure 3-1. Each I/O Unit has a separate set of logics to connect that I/O to the common OR gate for the Card Punch. The explanation here will explain the I/O Exchange logic of Central Control for only one I/O Unit, as the logic is identical for the other I/O Units.

The unit designation decoding matrix is the key in selecting the Card Punch Unit for this I/O. At the top of the Central Control box, in Figure 3-1, the unit designate decoding is shown.

As soon as D41F → D45F is set to a binary 10, the lower five legs of the designate AND gate are true. Also, the lower five legs of the designate AND gate for the Card Reader are true. However, the upper leg of the AND gate separates the two machines. If D24F is set, the Card Reader is selected. If D24F is off, then the Card Punch is selected.

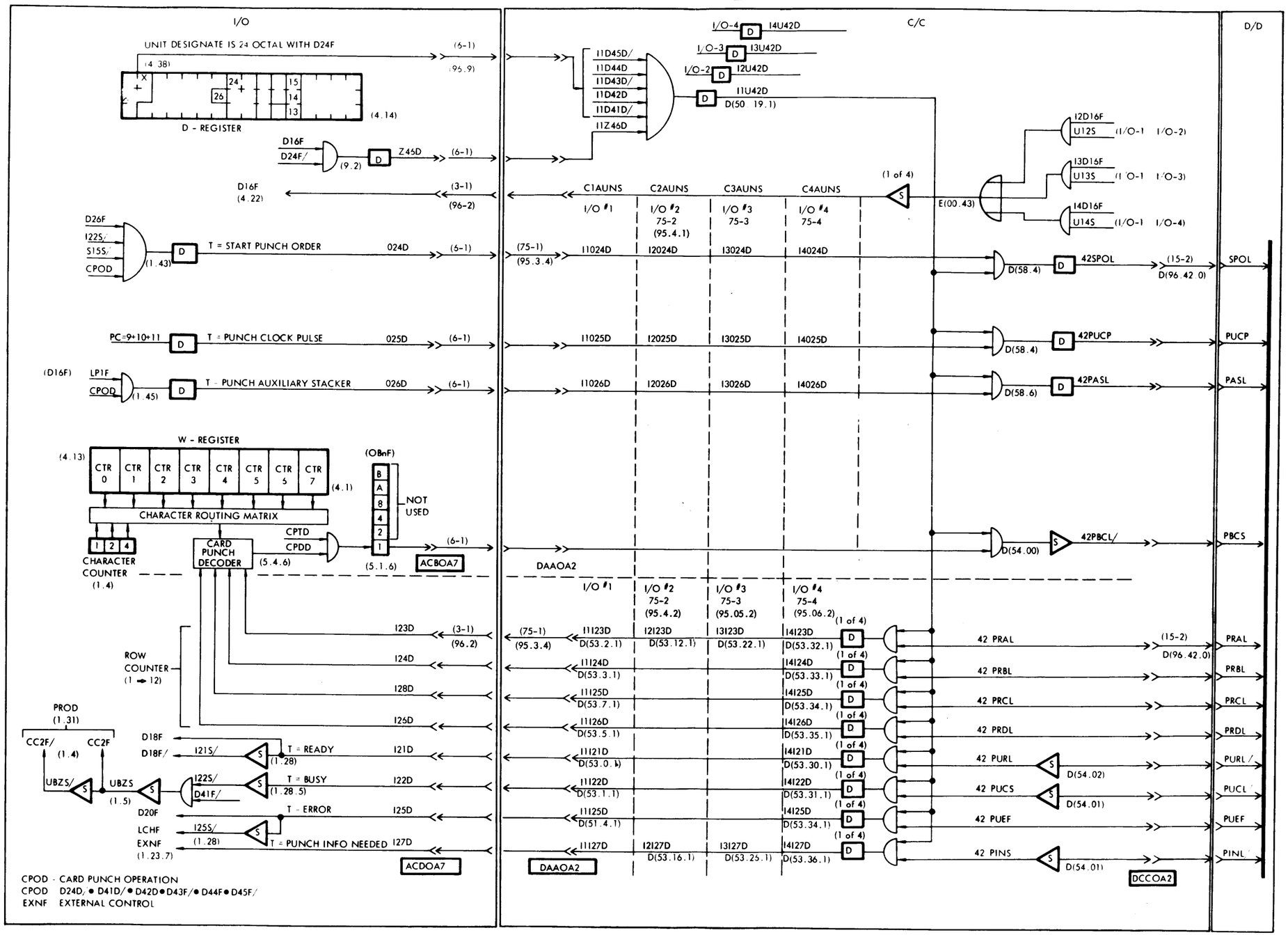


FIGURE 3-1 BASIC FLOW

The final level to permit the selection of the Card Punch is the enabling level, D16F. After the I/O Unit interrogates the availability and busy status through Central Control, a level from Central Control called AUNS (Admit Units Now) sets D16F in the D register of I/O. This level will enable Z46, which, in turn, enables the AND gate in I/O Exchange to connect the I/O Unit to the Card Punch.

Reading from the Top of Figure 3-1, the connecting lines are:

I/O to CC

Ø24D - This is an output driver from the D26F (1) bit of the D register. The level from D26F is amplified by the Ø24 driver and directed through the enabled AND gate to the OR gate. This OR gate allows any one of the four I/O Units to control the Punch. There are no conflicting levels from two I/O Units as the AUNS level mentioned previously prevents more than one I/O Unit from accessing the Card Punch at a time. From the OR gate the Ø24D level is again restored, in phase, by a driver, and sent to D & D (Display and Distribution Cabinet) as a true level to start the Card Punch. In the Card Punch this level is called SPOL.

Ø25D - This level comes from the PCC (Pulse Clock Counter) of I/O Control. This counter counts through 14 and recycles. During the period when PCC = 9, 10 and 11, Ø25D is true into Central Control. The internal logic of the Central Control Unit is similar to Ø24D. The output level is called PUCP (Punch Clock Pulse) to the Card Punch Unit.

Ø26D - This level comes from the LP1F Flip-flop in I/O Control. This level is gated in Central Control similar to Ø25D and enters the Card Punch as PASL (Punch Auxiliary Stacker Level).

ØB1F - All other peripheral units require six or seven information lines. Since the Punches only require one line for the buffer input to the Punch, the Central Control I/O Exchange only provides for this one line. This line originates with ØB1F in the I/O Unit. This level enters Central Control to the Designating AND gate, to the common OR gate, and a switch to become $\overline{\text{PBCS}}$ to the Card Punch Unit.

CC to I/O

I23D - PRAL
I24D - PRBL
I28D - PRCL
I26D - PRDL

These input drivers are inputs for the Card Punch Encoder located in the I/O Unit. These input levels are the binary coded input which is the equivalent to the actual row being punched with the Card Punch.

I21D - This input driver comes from the Card Punch as PURL (Punch Unit Ready Level) into the D & D cabinet and to Central Control unit designate AND gate, and to a common OR gate which allows other peripheral units to use the I21 Driver for its controls. If the Punch Unit is ready, the output of the I21 Driver is used to set D18F of the D register in I/O Control.

I22D - This input driver comes from the Card Punch as PUCL (Punch Unit Cycle Level). This level is similar in Central Control gating to the I21D line. When it enters I/O Control, it sets UBZS (Unit Busy Switch).

I25D - This input driver comes from the Card Punch as PUEF (Punch Unit Error). This level is similar in Central Control gating to the I21D line. When it enters I/O Control, it sets D20F.

I27D - This input driver comes from the Card Punch as PINL (Punch Information Needed Level). This level is similar in Central Control gating to the I21D line. When it enters the I/O Control, it sets EXNF (External Control Flip-flop).

I/O DESCRIPTOR

There are two types of Descriptors used in conjunction with I/O operation, the I/O Descriptor (Punch) and the Result Descriptor. In the following descriptions refer to Figure 3-2.

I/O Descriptor

This is used to select the Card Punch by the I/O Control Unit. This information will be used to set up the I/O Display Panel in the D & D Unit.

The bits of the I/O Descriptor have the following significance in the D register:

D48 ➡ 46	Non existent in D register; in memory they have the same meaning as a Data Descriptor, i.e., Flag bit and Presence bit.
D45 ➡ 41	Unit Designate (Binary ten)
D40 ➡ 31	Word Counter (Set to ten by hardware)
D30	Not used
D29 ➡ 28	Non existent in D register
D27	Must be reset to indicate Alpha
D26	SPOL
D25	Use Word Counter
D24	Read/Write Control (must be off)
D23	Non existent in D register
D22 ➡ 19	Error field
D18	Set if Punch is ready
D17	Used to indicate row 9 information has been transferred
D16	Selects Auxiliary Error Stacker
D15 ➡ 01	Memory address location

Result Descriptor

This is used to indicate to the MCP the results of the operation. The bits have the following significance as they would appear in the W register and in core memory:

W45 ➡ 41	Unit Designate
W40 ➡ 31	Should be equal to zero
W22	Set for Memory Address error
W20	Set for Punch error
W19	Set for Parity error (Memory to I/O)
W18	Set for Unit Not Ready
W17	Set for Memory error while accessing I/O Descriptor
W16	Set for Unit Busy on entry

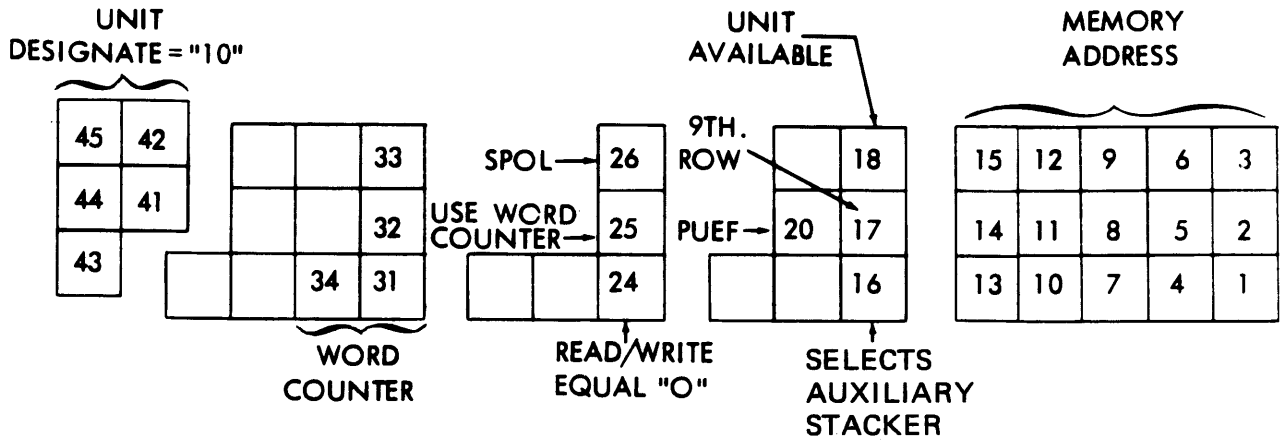


FIGURE 3-2 PUNCH DESCRIPTOR

OPERATIONAL FLOW

The Standard logic for the Card Punch is the same as for the other peripheral units. The initial memory cycle for the Descriptor Address and the subsequent memory cycle for the Descriptor is accomplished during SC = 0, 1, 2 and 3. The write-up for this operation is found in the I/O Orientation Manual. Also, SC = 14 and 15 are the same. This is the period that the Result Descriptor is constructed and D15 D01 are set to the memory address for the Result Descriptor. The final operation for the flow is to initiate a memory cycle, store the Result Descriptor in memory module "0", cells 0014 for I/O-1, 0015 for I/O-2, 0016 for I/O-3, or 0017 for I/O-4.

SC = 3. The UBZS (Unit Busy Switch) logic is necessary for the Card Punch as the I/O Unit is cleared as soon as the Result Descriptor is developed. This allows approximately 12° (B304) on the punch index before PUCL goes false. It is possible for another Card Punch cycle to be initiated in this time interval. When this happens, the normal I/O cycle will take place until SC = 3. At this time the I/O Unit will hold up with the Character Counter equal to six until $\overline{\text{UBZS}}$ goes true indicating PUCL is false. Then the I/O Unit will continue the normal sequence count.

Normal Card Punch Logic Flow (Refer to Figures 3-3 and 3-4)

SC = 3. I25D is the error level (PUEF) from the Card Punch. This error is always one card cycle late. When the error is sensed, the Punch logic will set up the card handling routine within the Card Punch Unit, and PUEF will remain true until reset by SPOL (Start Punch Order Level). I25D is sensed just prior to the clock pulse that set D26F and if true, D20F is set.

When the character counter is equal to five, a check is made for unit availability. If D18F is not set, indicating the unit is not available, or D16F is not set indicating the unit is busy, terminate the operation by jumping to SC = 14. Also, if memory access is permitted by MAPS being true, reset the W register in preparation for construction of a Result Descriptor.

PROD (Proceed Driver) is true when D16F, D18F and CC = 5 are true, meaning that the Punch Unit is available and ready. This level will set:

a. D25F to indicate the use of the word counter.

b. D27F off, to indicate the "Alpha mode" is to be used.

c. CC to zero, to prepare the Character Counter for the first character in the W register.

d. D26F on, this develops SPOL (Start Punch Order Level) for the Punch.

e. WC set to 10, to count memory words.

Depending on the status of D20F, a sequence count jump will be initiated. If there is a previous Punch error, D20F will be set. If set, jump to SC = 8. If not set, jump to SC = 9 for normal Punch operation.

Normal Punch Cycle - SC = 8, 9, 10 and 11

The Punch Cycle Flow Chart, Figure 3-3, shows the basic flow routing for the normal Punch cycle and Figure 3-4 shows the detailed flow of the Card Punch operation. With D20F off, the normal Punch cycle flow starts with SC = 9.

SC = 9. The first operation here is to request, from memory, the first word to be punched. This is signalled by MANF to 1. This starts the memory cycle and when the memory access is completed it sets MAOF to 1, which signals that memory access is obtained. MAOF clears the OB register and counts down the Word Counter one word. The first word is now in the W register. With MANF and MAOF set, count the sequence counter to 10.

SC = 10. At this time count the memory address (D15 ➡ D01) up one to point to the next word. Do not place the zero character in the W register into the Punch Decoder as D26 is still on. With memory cycles permitted and CPOD (Card Punch Order Driver), the sequence count jumps to eight.

SC = 8. At this point the I/O Unit is ready to be synchronized with the Punch Unit. The Position Counter is reset to zero as EXNF is off. The I/O Unit waits for PINL (Punch Information Needed Level) from the Punch. PINL comes through I27D of the Central Control Unit and sets EXNF to one. When EXNF is first turned on, D26F is still on. The first character in the W register is placed into the Card Punch Decoder and the Punch information into ØB1F. At the same time EXNF counts the character counter up one to point to the next character in the W register and turns off D26F as the appearance of PINL verified that the Card Punch has started.

The Position Counter starts counting as soon as EXNF is set. It counts to 14, then clears and recycles. It continues this for 80 cycles, one for each column on the card.

The Pulse Counter counts up until it is equal to 9, 10 and 11. During this time, the I/O Unit sends a PUCP (Punch Unit Clock Pulse) level to the Card Punch Unit via Ø25D in Central Control. This reads the bit in ØB1F and transfers it to the Punch Buffer register in the Punch.

As PC = 13, the level CØBD (Clear ØB Driver) is developed by PC = 13 and CPØD. This clears the ØB register.

At PC = 14, STRF (STRobe Flip-flop) is set and the Position Counter is reset to zero.

At PC = 0, STRF sets HØLF (Hold Over Flip-flop).

At PC = 1, STRF and HØLF and CC ≠ 0 will cause the following actions:

a. The next character in W register is sent to ØB1F
b. Character Counter pulse one
c. HØLF and STRF are reset

This sequence will recycle until the Character Counter counts through seven to zero. Then at PC = 1 time, the setting of HØLF and STRF will result in:

a. Sequence Counter plus one
b. EXNF turned off
c. HØLF and STRF are reset

This counts the Sequence Counter to nine.

SC = 9. At this time another memory cycle is requested to read the second word from memory, as the Word Counter is not equal to zero. Clear the ØB register, Count the Word Counter down one and count SC to 10.

SC = 10. At this Count the Memory Address is incremented by one. The first character in W is decoded into the ØB1F, the character counter is counted up one and the Sequence Counter set to eight.

SC = 8. The logic here is similar to previous discussion except that EXNF is set when entering SC = 8.

NOTE

This sequence will continue until the Word Counter equals zero. At this time and SC = 9, the Sequence Counter will be set to eleven.

SC = 11. If the Punch Unit is still ready, meaning no mechanical failures, D26F is set by I21D level which comes from PURL (Punch Unit Ready Level) in the Punch Unit. When the Punch has the information for the ninth row, PRDL (Punch Row D Level) and PRCL (Punch Row C Level) are true, resulting in the setting of D17F.

The setting of D17F then sets SC = 14 which allows the I/O Unit to construct the Result Descriptor and complete the cycle, releasing the I/O Unit from the Punch.

If at SC = 11 this is other than the last row of the card, D17 is not set; instead, the Word Counter is counted up to 10, the Address in the D register (D15 → 01) is counted down to its original value. When the Word Counter is equal to 10, the SC is set to 9 and the operation continues as previously described in Sequence counts 9, 10 and 8.

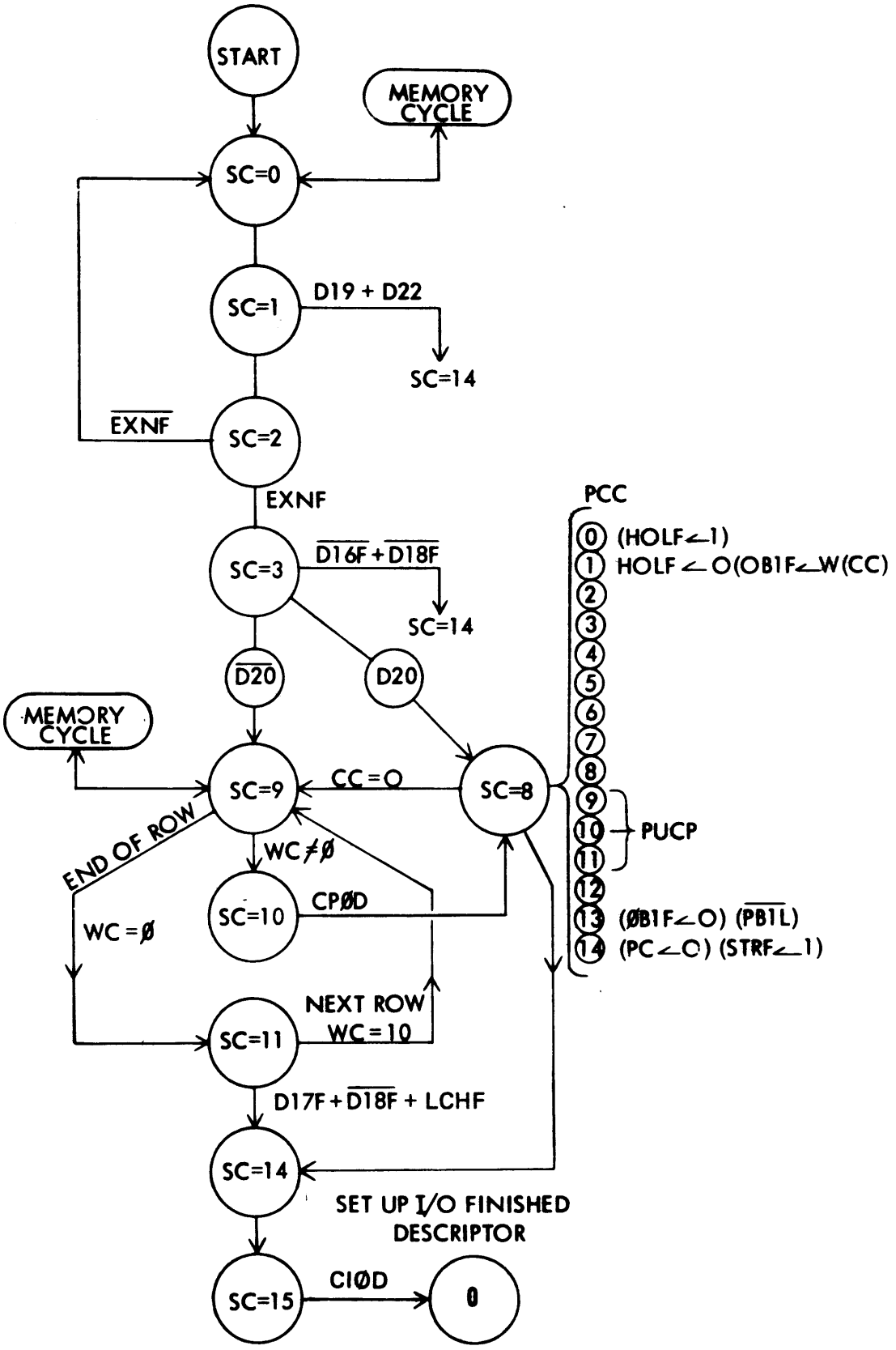


FIGURE 3-3 PUNCH CYCLE FLOW

Error Logic Flow

There are several types of errors which can be recognized by the I/O. The I/O Result Descriptor will reflect these errors.

Punch Check Error

The Card Punch has internal logic for testing punching errors. If one of these errors is sensed, the I/O Unit will not be notified during the punching cycle. The reason for this is the card just punched will be read and checked by the read brushes of the Punch during a second card cycle of the Punch.

When the error is sensed, the Card Punch could be starting the third card cycle after the error was punched. This error is sensed in I/O by I25D from Central Control being true. This sets D20F in I/O during SC = 3.

SC = 3. When I25D is true on SC = 3, D20F is set. PROD will still be true, however, logic will now shift to Sequence Count equal eight.

SC = 8. Before PINL becomes true, D20F and $\overline{\text{I25S}}$ will set LCHF (Last Character Flip-flop). The next clock pulse and LCHF will jump control to SC = 14. This will allow a Result Descriptor to be developed. Also, LCHF will reset D26F to drop SPOL to the Punch Unit. This will prevent the starting of the Card Punch for the third cycle.

The Result Descriptor will have D20F on to signal the Card Punch error to MCP.

Card Punch Not Available or Not Ready

In the event that the Card Punch is requested and the unit is not physically ready or already busy, the Result Descriptor must indicate this. In SC = 3 at CC = 5, the I/O Unit checks the operating status of the Card Punch.

If D18F is off, it indicates the unit was not ready. If D16F is off, it indicates the Card Punch is in use by another I/O Unit. In either case, the operation must be terminated and the MCP notified of the reason for not successfully completing the operation.

SC = 3. At Character Count equal to five, the status of D16F and D18F is checked. If either flip-flop is reset, the W register is cleared and the Sequence Count jumped to fourteen.

SC = 14. If D16F and D17F are reset, indicating an incomplete punch cycle, then set W16F to have bit 16 set in the Result Descriptor.

If D16F is set and D17F and D18F are reset, then set W18F in the W register to have bit 18 set in the Result Descriptor.

To summarize, if the Card Punch is not available, the 18 bit will be set in the Result Descriptor. If the Card Punch is busy, then the 16 bit will be set in the Result Descriptor.

Punch Cycle Error

If the Card Punch should start correctly and during the card cycle a mechanical error occurred, the Punch would go "Not Ready." This would make PURL false somewhere during the cycle. The I/O Unit must recognize this and construct a Result Descriptor to signal this.

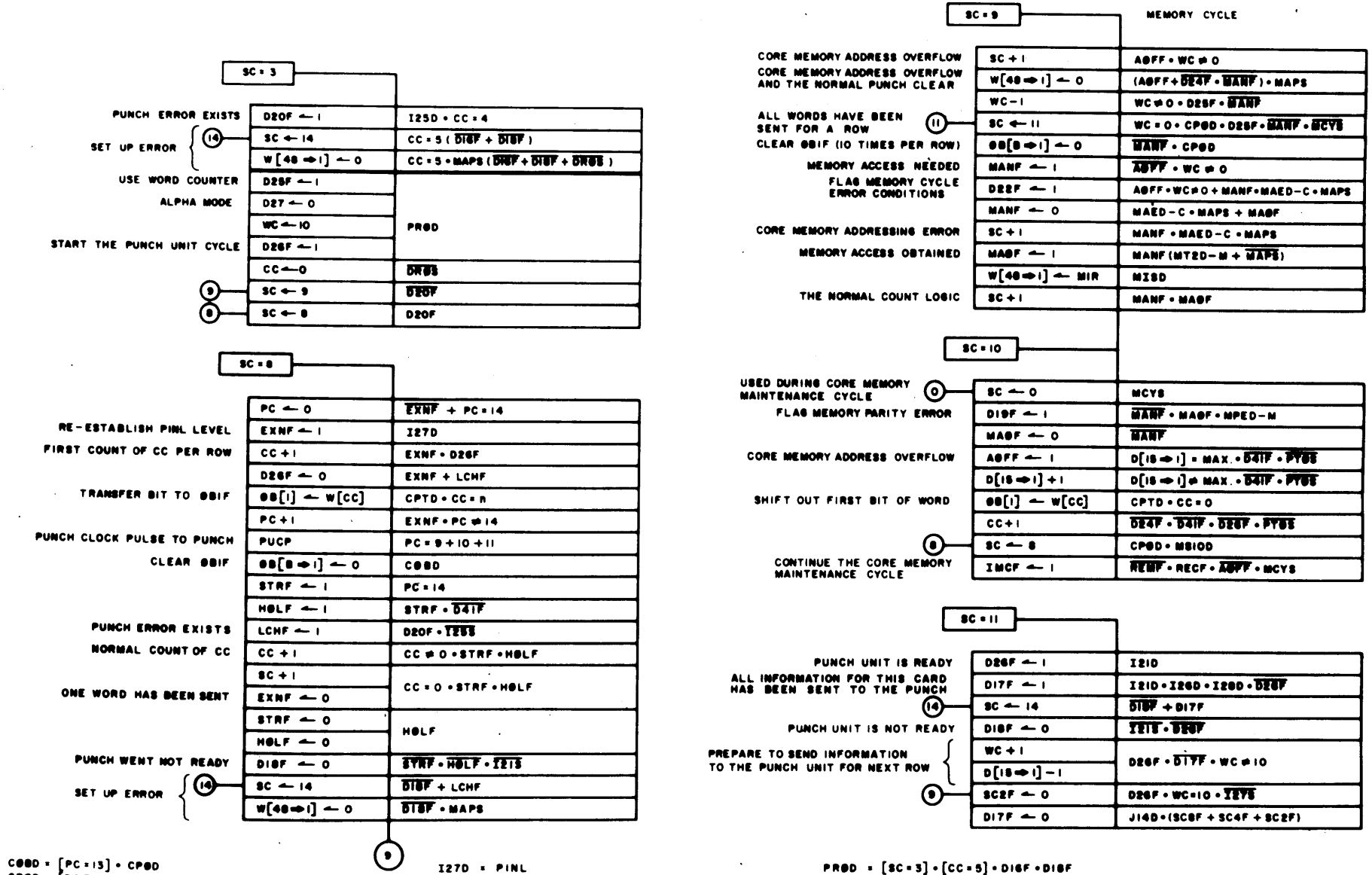
The punch cycle would be normal to the point where PURL went false. The cycle would continue until Sequence Count equal nine. When the Word Counter equal zero at SC = 9, the I/O Control jumps to Sequence Count equal seven.

SC = 11. At this time I21D is false so D26F will not be set. This prevents the setting of D17F, resets D18F and jumps the Sequence Count to fourteen. In the event that D17F had been set just as PURL went false, it would be reset as the card might not have row nine punched.

The jump to SC = 14 will develop a Result Descriptor in which the 18 bit will be set. This signals the MCP that the Card Punch went "Not Ready."

Memory Errors

There are several memory errors listed in the Standard and Card Punch flows. These will not be covered in this write-up as they require a complete understanding of memory flows. This is covered in the I/O Control Training Manual.



C00D = [PC = 13] • CP0D
CP0D = [D41F ⇒ D45F = 10] • D24F
CPTD = [SC = 8] • CP0D • (STRF • H0LF • CC ≠ 0 + EXNF • D26F)
OR [SC = 10] • CP0D • D26F
DNBS = NOT DRUM OPERATION
I21D = PURL
I21S = PURL
I22D = PUCL
I25D = PUEF I25S = PUEF
I26D = PROL

I27D = PINL
I27S = PINL
I28D = PRCL
J14D = JUMP SC TO 14
MISD = [SC = 9] • MANF • MA0F • D24F • MAPS
MSI0D = MCYS • [SC = 10]
0240 = SP0L = CP0D • D26F • I22S • [SC ≠ 15]
025D = PUCP
026D = PASL = CP0D • LPIF • [SC ≠ 3]
MCYS = MCYL • REMF

PR0D = [SC = 3] • [CC = 5] • D16F • D18F
PYBS = NOT PRINTER OPERATION
I23D = PRAL
I24D = PRBL

FIGURE 3-4

TITLE	CARD PUNCH
UNIT	1197533I
SYSTEM	B5000

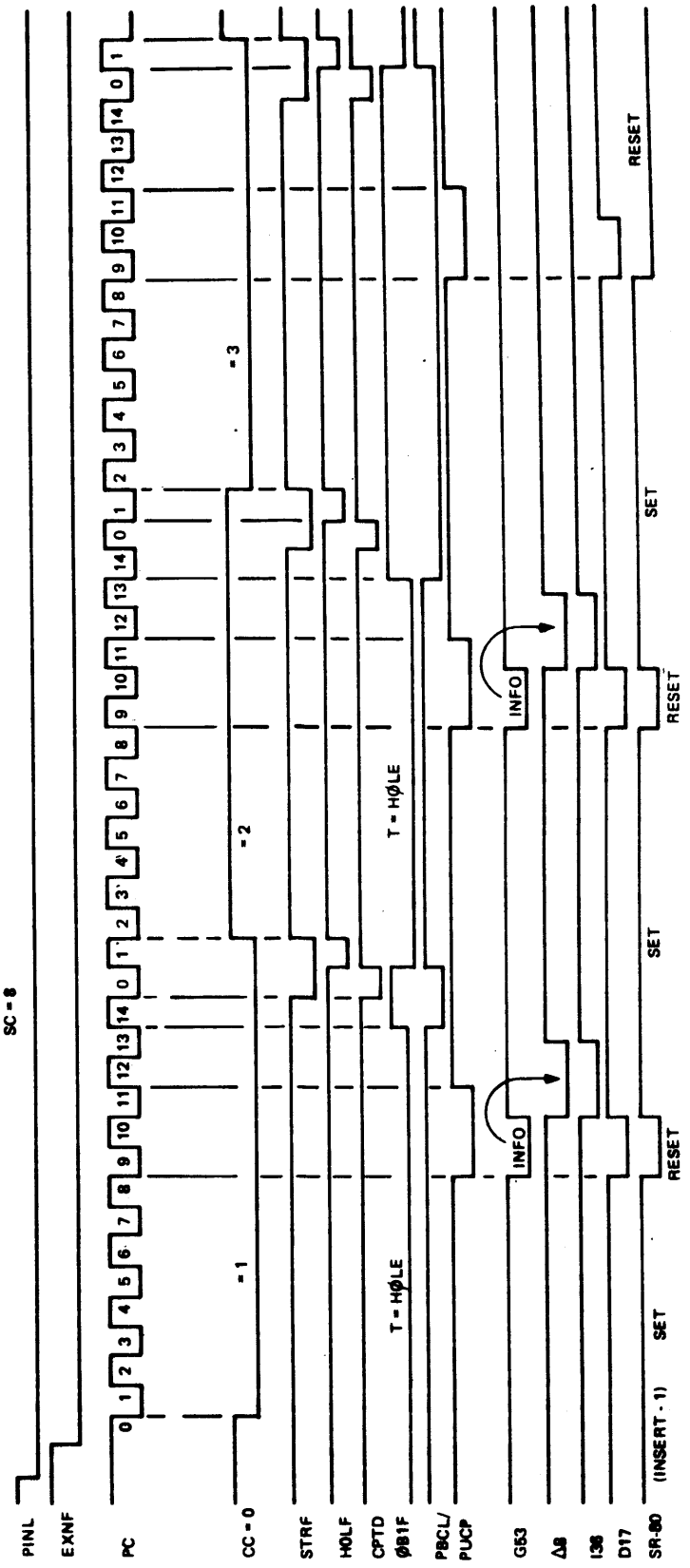


FIGURE 3-5 PUNCH INFORMATION

SECTION 4

B 5500 LINE PRINTER

GENERAL PRINTER OPERATION

The B5500 Input/Output Control (I/O Control) is a multi-purpose control and buffer which provides the information transfer and external control necessary for any one of several peripheral devices. This section is devoted exclusively to the necessary information transfer and control for the Line Printers.

All line printers used with the B5500 must contain a buffer memory capable of storing one line of print (either 120 ctrs or 132 ctrs). Below is a list of the different Line Printers presently compatible with the Model III I/O Controls.

				B320	475 LPM NO QC MEMORY	120 PP
		B9240	or	B321	700 LPM NO QC MEMORY	120 PP
				B325	700 LPM NO QC MEMORY	132 PP
		B9241	or	B328	700 LPM WITH QC (PRINT OF > 37 CTRS) 1040 LPM WITH QC (PRINT of ≤ 37 CTRS)	120 PP 120 PP
B9241	plus	B9941	or	B329	700 LPM WITH QC (PRINT of > 37 CTRS) 1040 LPM WITH QC (PRINT of ≤ 37 CTRS)	132 PP 132 PP
FEATURE:		B9941			12 Print Columns	
FEATURE:		B9946			"CR" Symbol for B325, B328 or B329	
FEATURE:		B9940			High Speed Slew (Available only on Unbuffered Printers (B9242)	
		B9245-2			315 LPM NO QC MEMORY	120 PP
		B9245-3			315 LPM NO QC MEMORY	132 PP

The Output File Declaration requires the programmer to specify the number of decimal words in the output buffer.

FILE OUT PTR 1 (1, 15)

Fifteen words are normally used when printing on a 120 column printer. The earlier B5000 systems used only 120 column printers. With these systems, the word count field (bits 40 through 31) of the printer I/O Descriptors contained a zero. The Model I and II I/O Control logics always assumed 120 columns to be printed and hardware forced the word count field to 15 decimal words at execution time.

The B5500 systems with Model III I/O Controls are capable of printing with either 120 or 132 column printers. Printer I/O Descriptors compiled on the B5000 require no program changes to be run on a 120 or 132 column printer while using Model III I/O Controls. The Model III I/O Controls allows the programmer to print any number

of words (one to 17) in memory on the line printer. A typical buffer size may be declared in the output file declaration as:

```
FILE OUT PTR 1 (1, 1)
FILE OUT PTR 1 (1, 17)
```

The compiler now places the buffer size of memory in the word count field (bits 35 through 31) of the printer I/O Descriptor. No printing without paper motion is permitted on the B5500 systems. A Paper Motion Cycle in the line printer is necessary to set the Printer Finished Interrupts in C/C. Without the printer finished interrupt, the MCP cannot print the next line.

When a WRITE Statement is encountered in the object program, the LIST and FORMAT routines load the buffer to be printed out. The FILE routine in this WRITE Statement notifies the Master Control Program (MCP) when the output buffer in memory is loaded and a Printer operation is desired. The MCP will check to see if a Printer operation can be performed and if so, the MCP will end its routine with an Initiate I/O Syllable (IOOL) which is forced into the T-register.

The IOOL Syllable places the address of the Line Printer Descriptor into cell 10 and notifies Central Control (CC) to commence I/O operation. The I/O Control Unit is already selected by Central Control before the address of the I/O Line Printer descriptor is read from cell 10 in memory.

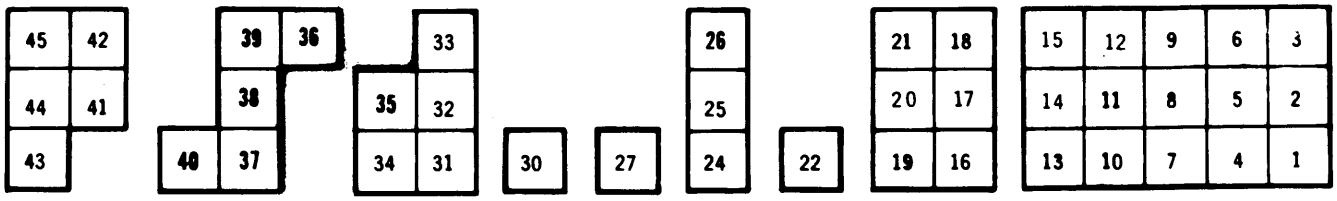
The I/O Line Printer descriptor is used to transfer either 120 or 132 characters from memory to the Line Printer. Data to be printed on the Line Printer is read one word at a time from a memory module. This 48-bit word is transferred, in parallel, by bits, from memory to the W-register which is located in any one of four I/O Control Units.

The I/O Control Unit being relatively fast, compared to the Printer, uses the Printer clock to synchronize the transfer of each character to the Printer. After all characters have been transferred, the I/O Control Unit constructs the Result Descriptor to be stored in an appropriate I/O Result Descriptor cell in memory, at octal addresses 14, 15, 16 or 17. Now the I/O Control Unit generates an I/O Finished Interrupt. The I/O Finished Interrupt forces an octal address of 27, 30, 31 or 32 into the Interrupt Address Register (IAR) in Central Control. In these cells is a branch routine which will allow the MCP or the individual programmer to decide what is to be done next.

The Printer Finished Interrupt does not occur until all paper motion has been completed (PAML/ going true) which is approximately 70 ms after the I/O Finished Interrupt occurred. During this 70 ms period, the I/O Control Units are useable by any of the other peripheral units. When the Printer Finished Interrupt occurs (I06F or I07F is set in CC), it forces an octal address of 25 or 26 into the Interrupt Address Register in Central Control. The very next Interrogate Interrupt Syllable (IINL) initiated by the Processor will unconditionally set the Processor's S-register to 100 and the C-register to 25 or 26 and L=0 (25 if Printer No. 1 is finished or 26 if Printer No. 2 is finished). In cell 25 or 26 is a branch routine which will possibly allow initiation of another I/O Print Descriptor.

DESCRIPTOR SIGNIFICANCE

The I/O Descriptor is set into the D-register in the I/O Display Panel to select any one of two Printers. The bits of this descriptor have the following significance.



D48F, D47F = 1, 0 (Identifies Descriptors as Data and I/O) Lost in the transfer of W-register to D-register.

D46F = Presence Bit: Specifies availability to output unit.
0 - Area available to output unit.
1 - Area available to program only.
This bit lost in the transfer of W-register to D-register.

D45F through D41F = Unit Designate (Octal 54 or 64)

D40F through D36F = These bits are not used in the I/O descriptor.

D35F through D31F = These bits contain the number of octal words in memory to be printed on the printer. The I/O logics always transfers either 120 or 132 characters corresponding to the memory buffer size. 15 decimal words becomes 17 octal words. 16-1/2 decimal words becomes 21 octal words.

D30F = 1 - Inhibits data transfer to Printer.
0 - Allows data transfer to Printer.

D29F, D28F = Lost in the transfer of W-register to D-register.

D27F = Binary/Alpha Bit: Must always be reset to allow alpha transfer from W-register to Line Printer.

D26F = 1 - Printer Long Line Level (PLLL) being true sets D26F indicated the selected printer requires 132 characters with each load cycle.

= 0 - PLLL being false allows D26F to remain reset. D26F/specifies 120 characters are required with each line of print.

D25F = Specifies the word counter is to be used.

D24F = Specifies an output operation from memory. If this bit was set, the Printer would not be designated.

D23F = Lost in the transfer of W-register to D-register.

D22F = Not Used

D21F = Single Space Flip-flop: This flip-flop is set to cause Printer to advance the paper one line space after each print cycle.

D20F = Double Space Flip-flop: This flip-flop is set to cause the Printer to advance paper two line spaces after each print cycle. If both Single Space and Double Space Flip-flops are set, the double space operation takes precedence in the Line Printer.

D19F through D16F = Format Control Flip-flops: Only at (SC=2 • EXNF). Binary 1 ⇒11 selects channels 1 ⇒11. These flip-flops must be equal to zero for single or double space operation because the skip operation takes precedence over single or double spacing in the Printer. Channel 12 can be designated in these flip-flops, however, this is a program error since the Printer does not provide skipping to channel 12. Channel 12 is reserved only for detecting end-of-page punches in the format tape.
At SC = 3:
D18F is set if Printer is ready.
D16F is set if Printer is not busy.
D19F - Not Used

D17F = 1 - D17F is a logical flag used to indicate when the contents of memory are to be transferred to the line printer

= 0 - As long as D17F remains reset only blank characters are transferred to the line printer.

D15 through D13F = Memory Module (0 through 7).

D12F through D01F = Specifies most significant memory address.

RESULT DESCRIPTOR

The Result Descriptor is formed just prior to the generation of each I/O Finished Interrupt. The error field indicators in the Result Descriptor for a Line Printer operation are as follows:

D40F through D36F = Represents the number of words printed on the Printer (1 through 21Ø). This field always represents the number of words in memory the programmer desires to be printed on the Line Printer. This field contains the original word count field in D35F through D31F. If D35F through D31F was equal to zero in the Printer I/O Descriptor, then D40F through D36F would contain 17 octal in the result descriptor.

D35F through D31 = This field would always be zero.

D22F = This bit is set when a memory address error occurs.

D21F = This bit is set when the Print Descriptor bits, D19F through D16F, fail to designate a channel on the format tape when an End-of-Page Level is generated by the Line Printer. EOPL is generated with each hole punched in channel 12 or when the operator fails to mount a format tape in the Printer.

D21F being on in the result descriptor specifies an end-of-page has been sensed by the Line Printer and the programmer did not provide some channel skipping. A load cycle has been performed without a paper motion cycle. No EPRL is generated at SC=13 to reset EOPF in the Line Printer. With these logical conditions, the programmer must provide branching to a Skip operation to reset EOPF. When programing the B5500 with end-of-page functions, the programmer may count the lines printed on each page in order to anticipate when format skipping is necessary.

D20F = Indicates a parity error occurred in the Line Printer while printing the previous line.

D19F = Set to indicate a parity error occured in memory.

D18F = Set when the Printer is in a Not Ready status.

D17F = When D17F is on with D19F or D22F, the error indicated by D19F or D22F occurred during the access of either the I/O Descriptor or its address.

D17F being reset with D19F or D22F indicates the error occurred during the Printer operation.

D16F = Indicates the Printer is in a not ready status or that there was an I/O Conflict when the Printer operation was initiated (two I/O Control Units trying to access the same Printer).

D15F through D01F = Indicates one word address lower than the address of the last word transferred to Printer. The reason being that the address in the D-register is counted down after each memory access.

GLOSSARY OF TERMS

AOFF — Address Overflow Flip-flop: This flip-flop is set when the memory address in the D-register has exceeded the memory capacity.

AMNS — Address Minimum Switch: This level becomes true when the address in the D-register is counted down from all Off to all On, indicating an address underflow or when the memory address is counted up from all on to all off (D15F through D01F).

DC = 0 — Designate Channels 0 through 11: The designate channel level is equal to zero (DC=0) when the LP1F through LP8F are all reset.

D reg. — The Printer I/O Descriptor is placed in the D-register of any one of four I/O Control Units.

DWSD — D to W Register Shift Driver: This level is used in a local operation to shift, repeatedly, the contents of the D-register to the W-register for printout when the I/O Control Unit is in LOCAL.

EPRL — End-of-Page Reset Level: This level is generated when an End-of-Page is detected and any one of eleven channels is designated in LP1F through LP8F. EPRL is used by the Printer to reset the End-of-Page Flip-flop (EOPF).

EXNF — External Control Flip-flop: During SC=1, SC=2 or SC=3, this flip-flop indicates whether the word in memory is the descriptor address or the descriptor word. At SC=8, EXNF is used as a logical flip-flop to delay the first digits transferred to the Line Printer by 10 μs after PITL becomes true with the first word to be transferred. This delay is necessary to allow Printer to get set up for memory cycles (set PINCF).

HOLF — Hold Over Flip-flop: This flip-flop is used to allow one character to be transferred from the W-register to the Printer at each Printer clock pulse time.

LOBD — LPnF's to OB Shift: This level allows the space or skip information to be shifted to the OB register after 120 characters have been transferred to the Printer buffer memory.

LPnF — Longitudinal Parity P thru 1 Flip-flops: Used to temporarily store the spacing or skipping information for the Printer.

MAND — Memory Access Needed: Used to obtain a memory access.

MISD — Memory Information Strobe Driver: Information from the MIR register in memory is transferred to the W-register in I/O by this level.

PLCL — Printer/Lister Command Level: This is a 10 μs level generated at SC=13 in the I/O Printer Descriptor. PLCL's are used in the Line Printer to initiate print cycles and to allow the Paper Motion Flip-flop (PMCF) to be set to remember the fact that paper motion is to be initiated after each line has been printed. A PLCL cannot be generated until all paper motion has stopped (D25F/) from the previous line. A PLCL is also used to gate the transfer of format control and space information to PFCnF, PMCF or PDSF Flip-flops located in Printer. The jumper package located on the Printer logics rack must be wired properly for B5500 systems to provide proper remote paper motion operations.

PLCP — Printer/Lister Clock Pulse: PLCP's are .5 μs pulses which are generated in the Printer and transferred to the Central Control at 10 μs intervals. This pulse is always present in Central Control as long as power is up on the Printer.

PLLL — Printer Long Line Level: This level originates in the Line Printer and when true the printer is identified as containing 132 print columns.

PROD — Proceed Driver: The output of this driver allows I/O to proceed in the I/O Printer flow when Printer is ready (PRRL/ false), not busy (PCYL false) and designated.

PTOD	Printer Operation: This level is true when a Printer Descriptor is placed in the D register. PTOD = Binary 22 or 26 in D45F through D41F.
WC = 0	Word Counter Equal to Zero: This level is true when the word counter D40F ⇒ D31F is equal to zero.

OPERATION FLOW

GENERAL DESCRIPTION

The print operation is started with an initiate level (ADNS) from the Central Control. This level sets the address register and initiates a memory cycle to bring the word in cell 10 of memory, into the I/O Unit. This word contains the address of an I/O Data Descriptor. A second Memory Cycle is then initiated to bring the Data Descriptor into the I/O Control Unit (D register). If during this process a memory address or parity error condition occurs, the operation is terminated; and a result descriptor, showing these errors, is sent back to the Processor.

With the Data Descriptor in the D register the status of the peripheral unit (Printer) is checked. If the unit is ready and not busy, the operation continues. Otherwise, the operation is terminated; and a result descriptor is sent back to the Processor. The Data Descriptor address is increased by 15 to address the least significant word. Memory is then accessed to bring the 15th word into the word register of the I/O Control Unit. The transfer of characters commences with the Least Significant character. Characters are transferred from the Word Register to the output buffer and then to the Printer information register. As each word is exhausted, a new word is brought up and transferred character by character until 15 words have been transferred.

When all information is transferred, the Format Control digits are transferred to the output buffer and then to the format control flip-flops in the Printer. At the same time that the format digits are transferred, the print cycle is initiated. End-of-Page sensing also occurs at this time. The Result Descriptor is sent back to memory and I/O Finished interrupt condition is set in Central Control and the Operation is complete. The Printer Print Cycle continues independent of the I/O Control Unit.

The Printer Buffer is located within the Printer Unit and requires 15 computer words per line of print.

The I/O Control Unit causes 8 characters per computer word to be printed.

No editing or format control of data is accomplished by the Printer.

Vertical format control is specified in the descriptor. Spacing and skipping take place after printing.

An end-of-page signal is recognized before completion of the last line of print on a page. The End-of-Page signal is noted in the result descriptor of that line, and line space is inhibited. Only a "skip" operation can be accomplished when an End-of-Page level is being detected.

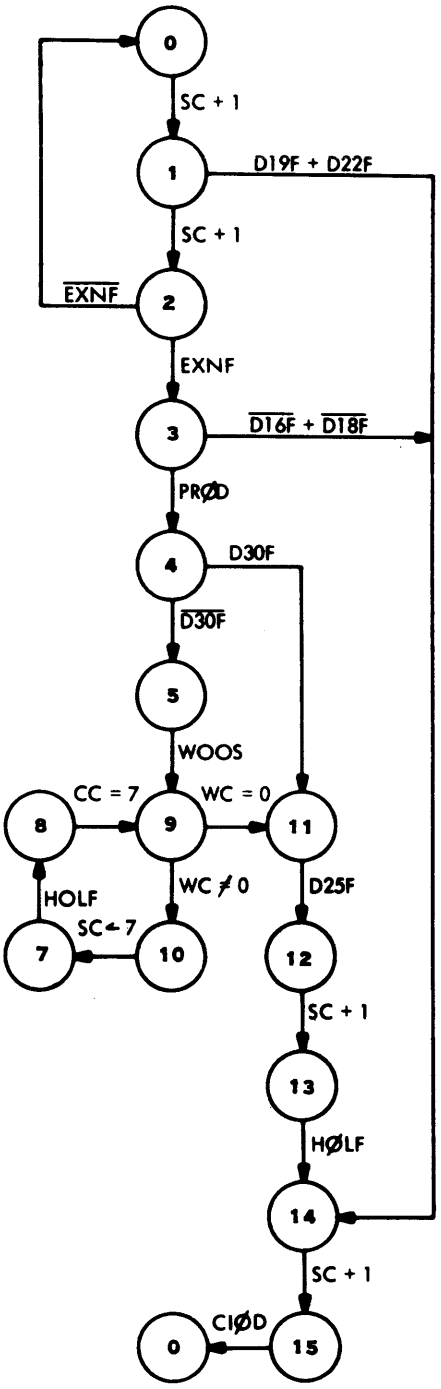


FIGURE 4-1 PRINTER OPERATION - SEQUENCE COUNTS

If the descriptor for the last line of print contains a skip, the end-of-page signal is not noted in the result descriptor, and the Printer skips to the stop in the specified channel.

Paper may be spaced or skipped without printing by specifying print inhibit in the descriptor (D30F set).

Overprinting a line of print is possible by not specifying a line space or skip for the line to be overprinted.

On completion of a line of print, a bit is placed in the Interrupt Register. These bits will generate the following addresses which are placed in the C register when the Processor enters the control state.

Address 21 for Printer, unit 22
Address 22 for Printer, unit 26

A Print Check error for one line of print will be noted in the result descriptor of the next line but will not inhibit the print of the new line.

SC = 0, 1, and 2: Operation initiated by AUNS from Central Control. Two memory accesses are performed. (EXNF/ first memory cycle and EXNF set second memory cycle).

1. Read descriptor address from memory.
2. Read descriptor from memory.

SC = 3 Check peripheral unit for Ready (D18F) and Not Busy (D16F).

SC = 4 Check state of D30F. (D30F set = No data transfer).

1. D30F = Control Descriptor = JUMP to [SC = 11].
2. D30F/ = Not Control Descriptor = SC + 1.

SC = 5 Increase Memory address by 15, set WC to 15.

SC = 7 Sync on Printer clock.

SC = 8 Transfer data word to Printer.

SC = 9 and 10 Access memory for Data Word.

SC = 11 Wait for End-of-Paper motion.

SC = 12 Transfer format control bits from LP to ØB.

SC = 13 Transfer format control bits to Printer and initiate print cycle.

SC = 14 Construct Result Descriptor in W register and address in D [15 ➡ 1].

SC = 15 Transfer Result Descriptor to memory and clear I/O Unit.

DETAILED DESCRIPTION OF OPERATIONAL FLOW

STANDARD LOGIC SEQUENCE CHART

SC = 0

The standard flow for the Line Printer is the same for all peripheral units. At SC=0, 1 and 2, the initial memory cycle is for the descriptor address (EXNF/) and the second memory cycle is for the descriptor (EXNF set). At SC=3 the Printer is checked to see if it is ready (I21D true) and no conflict (AUNS). Example: C1AUNS is a true level developed in CC and sent to I/O 1 when I/O 2, 3 or 4 is not using

the same Printer designated by I/O 1. If the Printer happened to be busy at SC=3 (UBZS true) because PCYL is true, the character counter will count from 0, 1, 2, 3, 4, 7 and then to 6, as shown in Figure 2.5-4. Character Counter is held at the count of six until UBZS/ goes true. At this time the character counter is counted to 4 and then to 5 which is the normal exit of the standard logic flow.

D17 to 1 - D04F to 1

If the Admit Descriptor Needed Switch is True in Central Control (ADNS-C) or if the Initiate Maintenance Cycle Flip-flop is On and the memory cycle switch is Off (IMCF * MCYS), then set the D17 bit and the D04 bit in the D register of I/O Control. The setting of these two bits, D17 and D04, starts a normal cycle in remote operation (ADNS-C) and a normal cycle for maintenance in local (IMCF * MCYS/).

MANF to 1

With D17F On, set the Memory Access Needed Flip-Flop (MANF) On to start the memory cycle.

Floating Memory Cycle Logics-MANF to 0

When the memory access is obtained (MAOF) or if there is a memory address error and Memory Access is Permitted (MAED-C * MAPS), then turn the Memory Access Needed Flip-flop Off.

D22F to 1 SC + 1

If the memory Access Needed Flip-flop is On and there is a memory address error (MAED-C) and Memory access is permitted (MAPS) then set the memory address error bit in the D register (D22F) and advance the Sequence Counter plus one. The memory address error is a result of addressing a nonexistent unit.

MAOF to 1

If Memory access was needed (MANF) and either at Memory Time 2 (MT2D-M) or with the Memory Access is Permitted switch Off (MAPS/) set the Memory Access Obtained Flip-flop. This allows the information to be transferred in Normal operation (MT2D-M) or to simulate an access obtained when Memory Access is not Permitted (MAPS/).

MIR to W Register

With the Memory Input strobe pulse (MISD) transfer the information from MIR register to the W register.

MAOF to 0

With the Memory Access Needed Flip-flop Off (MANF/), Access Obtained Flip-flop Off. These two Flip-flops essentially gate each other.

D19F to 1

With the Memory Access Needed Flip-flop Off (MANF/), Access Obtained Flip-flop On (MAOF), and with a Memory Parity Error (MPED-M) then set the parity error bit in the result descriptor (D19F). This is an indication that there was a parity error in the information just transferred to the W register.

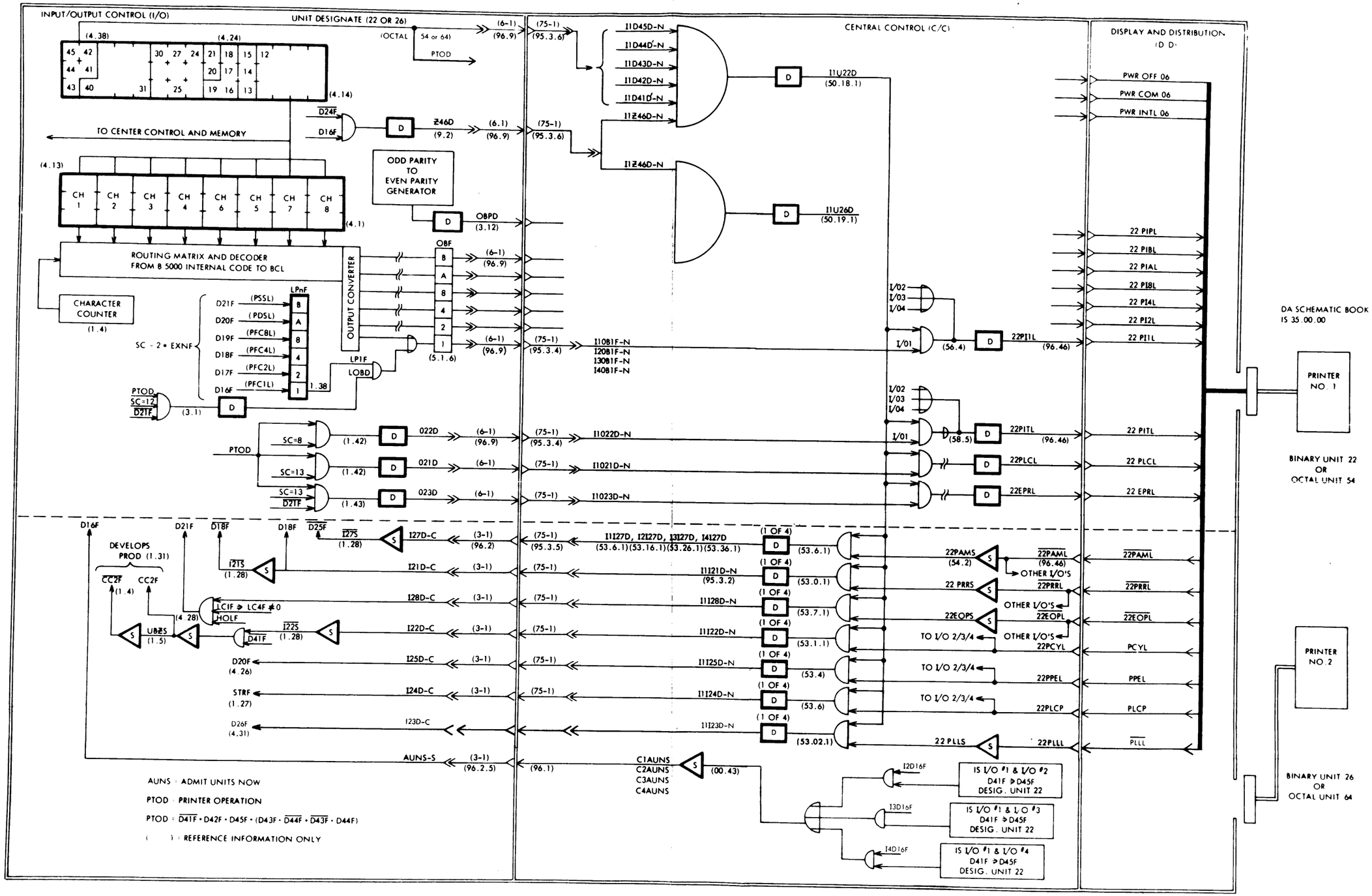


FIGURE 4-2 B5500 PRINTER OPERATION

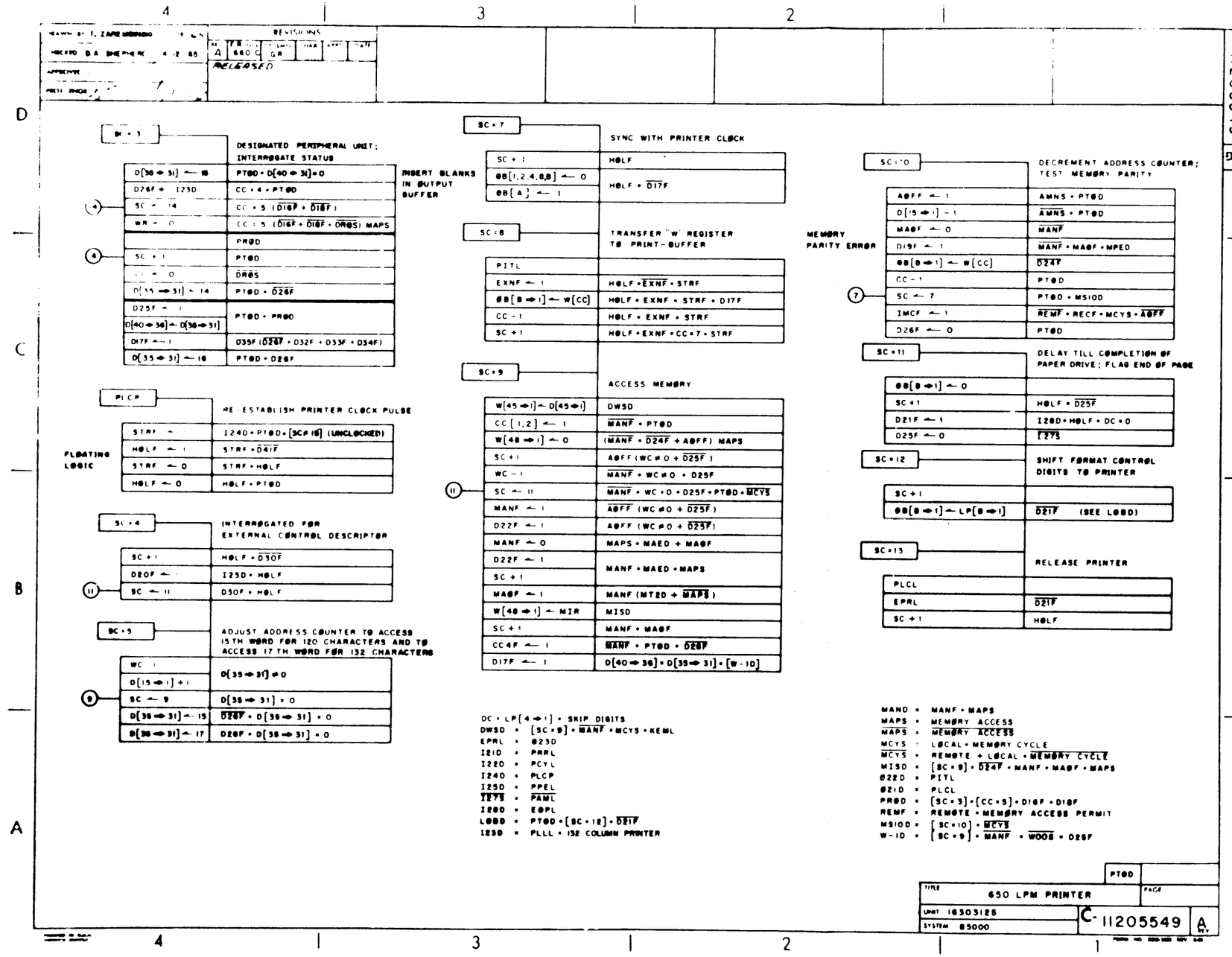


FIGURE 4-3 PRINTER FLOW

SC + 1

Count the sequence counter plus one if the Memory Access Needed Flip-flop is Off (MANF/) and the Memory Access Obtained Flip-flop is On.

SEQUENCE COUNT EQUALS ONE

This is the logical box for error set-up, if required.

W Register to 0

Clear the Word register if there is either a parity error (D19F) or a memory address error (D22F) and memory access was permitted (MAPS).

SC to 14

Set the sequence counter to 14, to terminate, if there was either a memory parity or address error (D19F + D22F).

D[45 → 01] to 0, SC + 1

Clear the D register and count the sequence counter up one if there is no parity or address error (D19F/ * D22F/).

SEQUENCE COUNT EQUALS TWO

EXNF

Complement the External Control Flip-flop. EXNF functions as a counter to allow an alteration of the SC=0, 1, 2 cycle. EXNF is set on the first pass and reset on the second.

W[21 → 16] to LP [B → 01]

If the External Control Flip-flop (EXNF) is On (Second Pass) shift the space and format control bits from the Data Descriptor in W into the Longitudinal Parity Flip-flop for storage. This action only occurs after we have made the second memory access, which places the Drum Printer Data Descriptor in the W register of the I/O Control Unit.

W[45 → 25] to D[45 → 25] and W[15 → 0] to D[15 → 0]

Transfer the word in W to the corresponding fields in D. W register contains address of the Data Descriptor on the first pass and the Data Descriptor on the second pass.

SC to 0

D17F to 1

If the External Control Flip-flop is Off (first pass) then reset the Sequence counter to 0 and turn D17F On. This will allow the start of another memory cycle to bring the I/O Data Descriptor from memory to the W register.

W[48 → 01] to 0

If the External Control Flip-flop is Off (first pass) and Memory access permitted, clear the W register in preparation for a load from Memory.

SC + 1

When the External Control Flip-flop (EXNF) is On (second pass), count the sequence counter to three.

SEQUENCE COUNT EQUALS THREE

CC + 1

If the Character Counter is not 4 (CC4F/) or, if the character counter is 4 and the unit Designator is even (not a Tape Unit), then count the character counter plus one. The character counter will continue to count, until it reaches 5.

D16F to 1

If the Admit Unit Now (AUNS) level is true and the character counter has counted 2 (CC=2), set the D16F complete peripheral designation and interconnection.

D18F to 1

If the Printer Ready Level is true (I21D) and the character counter is equal to 4 (CC=4) set D18F On. The settings of D16F and D18F are used here to flag that the unit is Not Busy and Ready.

D16F to 0

If the Printer Cycle Level is true (I22D) indicating that a Print Cycle is in progress, and the Character Counter is equal to 4 (CC=6), reset D16F.

SC to 14

If the character counter is equal to 5 (CC=5) and either the unit is busy (D16F/) or not-ready (D18F/), then set the sequence count to 14 to terminate the operation.

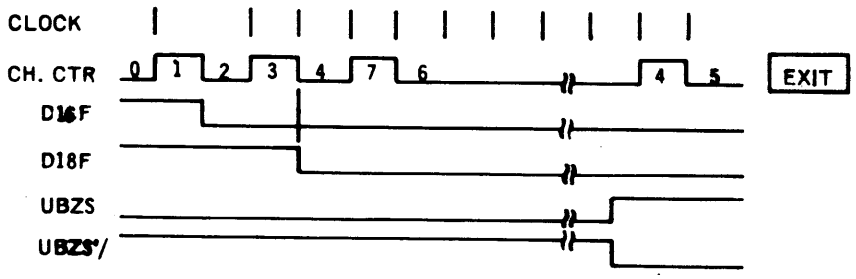


FIGURE 4-4. PERIPHERAL UNIT NOT BUSY

Enter Printer Flow (Refer to Figure 2.5-3).

D[35 through 31] to 17 octal

Normally the word count field contains some value of octal 1 through 21. If D40F through D30F is equal to zero then this I/O descriptor was compiled before the Model III I/O controls were available and 15 decimal words are to be printed on the line printer. At this time, D35 through 31 contain the number of words in core memory to be printed on the line printer.

D26F to 1

If the designate printer contains 132 print columns, I23D is true and D26F is set. D26F is used to select the proper address modification at CC = 5 PROD.

Clear W register

If the Character Counter is equal to five (CC=5) and if either the unit is busy or not ready or not a drum operation (D16F/ + D18F/ + DROS/) and a Memory Access is Permitted (MAPS), then clear the word register.

SC + 1

In addition to the Common Logic gate above (PROD), if the unit designated is a Printer Operation (PTOD), then advance the sequence counter one.

CC to 0

In addition to the Common Logic gate above, if this is not a Drum Operation (DROS/), then clear the character counter.

D[35 through 31] to 16 octal

If D26F is reset when PROD becomes true, the printer requires 120 characters. The word count field is therefore set to an octal 16. This value is to be used at SC = 5 to modify the D-register address portion to access the 17th octal word from the starting address. Sixteen through zero represents 17 octal addresses.

D 35 through 31 to 20 octal

If D26F is set when PROD becomes true, the printer requires 132 characters. The word count field is therefore set to an octal 20. This value is to be used at SC = 5 to modify the D-register address portion to access the 21 octal word from the starting address. Twenty through zero represents 21 octal addresses.

D35 through 31 to D 40 through 36

Transfer the number of core memory words to be printed on the printer into D40 through 36 because D35 through 31 is used as a counter during address modification. The beginning address in D15 through 1 must be modified because the line printer requires the least significant character transferred first.

D25 to 1

D25F is set to allow the use of the word counter D35F through D31F.

D17 to 1

If D17F is not set, the logics transfers blank characters to the printer at SC = 8. After D17F is set the logics allows the contents of core memory to be transferred to the printer.

The clock pulse that finds PROD true could find D35F through D31F equal to 21 octal words (132 ctrs) and D26F set (132 column printer). D17F would not be set because 21 octal words represents 4 characters in excess of 132 print columns. In this case, D17F would be set at the first entry into SC = 9.

D17F is set at SC = 3 * PROD when the number of program words to be printed are greater than the capacity of the printer.

```
D17F = D26F * D35 * D32F (22, 23, 26, 27)
       D26F * D35 * D33F (24, 25, 26, 27)
       D26F * D35 * D34F (30, through 37)
       D26F/ * D35       (20, through 37)
```

D17F being set at SC = 3 represents a program error. No error flags in the Result Descriptor are generated for this condition.

The following actions are not dependent on any particular sequence count setting. They occur with each print line clock pulse (PLCP).

STRF to 1

If there is a Printer Lister Clock pulse (I24D) and a Printer is designated (PTOD), set the Strobe Flip-flop On.

HOLF to 1

If the Strobe Flip-flop (STRF) is On and the unit designated is not a tape unit (D41F/), then set the Holdover Flip-flop On.

STRF to 0

With the Strobe and Holdover Flip-flops (STRF • HOLF) On, reset the Strobe Flip-flop.

HOLF to 0

With the Holdover Flip-flop On and a Printer designated, reset the Holdover Flip-flop.

SEQUENCE COUNT EQUALS FOUR

SC + 1

With the Holdover Flip-flop On and not a Control Descriptor (HOLF • D30F/), advance the sequence counter to five.

D20F to 1

If the print parity error level (I25D) is true and the Holdover Flip-flop (HOLF) is on, then set the D20F. D20F flags printer error from the previous line of print.

SC to 11

If the D30F is On (control descriptor) and the Holdover Flip-flop On, set the sequence counter equal to eleven.

SEQUENCE COUNT EQUALS FIVE

WC -1, D[15 ➡ 1] +1

If the word counter is not zero (WOOS/), count the word counter D[35 through 31] down one for each clock pulse and count the address register plus one.

SC to 9, D[35 through 31] to 17 or 21 octal

When the word counter is equal to zero (WOOS), then set the sequence counter to nine and access memory. D[35 through 31] represents the number of octal words that must always be transferred to the Line Printer.

SEQUENCE COUNT EQUAL NINE

DR to WR

If Memory Access Not Needed (MANF/) and the Maintenance Cycle Switch (MCYS) On and the Key Memory Level (KEML), then transfer the word in D to the W register. This function is active during the maintenance cycles only.

CC to 7

If the Memory Access Needed Flip-flop (MANF/) is Off and a backward read tape operation is specified (D26F * TAOD) or it is a Printer Operation (PTOD), then set the character to 7.

WR to 0

If Memory Access Not Needed (MANF/) and output operation is specified (D24F/) or there is an Address Overflow (AOFF), then clear the word register.

SC + 1

If there is an Addressing Error (AOFF) and either if there are still words to be transferred (WC≠0) or if the D25F bit is Off, then advance the sequence counter to 10.

WC -1

If Memory Access Not Needed (MANF/) and the word counter is not zero and D25F is On, count the word counter down one. [W-1D] becomes a true level at this time.

SC to 11

If Memory Access Not Needed (MANF/) and the word counter is equal to zero (WC=0) and the D25F bit is On, set the sequence count to 11 to check for End-of-Page and format.

MANF to 1

If there is no Address Error (AOFF/) and either the word counter is not zero (WC≠0) or the D25 bit is Off, then set the Memory Access Needed Flip-flop On to initiate a memory access.

D22F to 1

If there is an Address Error (AOFF) condition (AMXS + AMNS) and either the word counter is not zero (WC≠0) or D25F is Off (D25F/), then set the memory address error bit in the descriptor (D22F) to one.

MANF to 0

If there is a Memory Address Error (MAED-C) or upon completion of the Memory Access (MAOF) reset the Memory Access Needed Flip-flop.

D22F to 1

SC + 1

If the Memory Access Needed Flip-flop is On and there is a Memory Address Error (MAED-C) then set the memory address error bit (D22F) in the descriptor and count the sequence counter plus 1.

MAOF to 1

If a Memory Access (MANF) was requested, then set the Memory Access Obtained Flip-flop, at Memory Time 2 (MT2L), to release the Control Unit and continue the operation. MAPS/ would be true if the Memory Inhibit Switch was in the Inhibit position.

MIR to WR

Transfer the information from the memory information register to the word register with the memory input strobe (Read operations only).

MISD

Allow the memory input strobe if the Memory Access Needed and Memory Access Obtained Flip-flops are On and if there is an output operation (D24F/).

SC + 1

Count the sequence count to 10 if the Memory Access Needed and Memory Access Obtained Flip-flops are On.

CC 1, 2 to 1

In a printer operation,
The first clock pulse into SC = 9 always allows the setting of character counter 1 and 2 bits.

CC4F to 1

When printing 132 columns on the printer (D26F set), CC4F must be inhibited from setting with the first word accessed from memory. This logics allows only 4 characters of the first word accessed from memory to be transferred to the printer.

D17F to 1

D 40 through 36 represents the number of words the programmer wishes to be printed on the printer. D 35 through 31 initially represents the maximum number of words the printer must receive with each line of print. If these two fields are not equal, D17F cannot be set. Only blanks are transferred to the line printer at SC = 8, when D17F is not set. If the number of words the programmer chose to print was greater than the maximum number of words the printer is capable of printing, D17F would never be set with this logic. This condition, however, is covered in the setting of D17F at SC = 3.

SEQUENCE COUNT EQUAL TEN

AOFF to 1

Set the Address Overflow Flip-flop if the address counter is at the minimum (AMNS) and a Printer operation.

A -1

If the address counter is not at the minimum (AMNS/) and it is a Printer Operation (PTOD) then count the address counter down one.

MAOF to 0

If the Memory Access Needed Flip-flop is Off, reset the Memory Access Obtained Flip-flop. This setting of MAOF to 0 occurs one microsecond later for a read operation to allow time for a parity check.

D19F to 1

If the Memory Access Needed Flip-flop is Off, the Memory Access Obtained Flip-flop On (MANF • MAOF) and there is a Memory Parity Error (MPED-C), then set the parity error bit (D19F).

WR to OB

With the transfer W clock level true (will be with D24F/ * PTOD), transfer a character from the word register to the output buffer register. The Character transferred is the L.S.D. as the character counter was previously set to 7 at SC=9 time.

TWCD

Allow the transfer W clock level to come true if the D24F bit is Off (D24F/) and it is a Printer Operation (PTOD).

C-ID

If a Printer Operation (PTOD), count the character counter down one to point at the next character to be transferred to the output buffer.

SC to 7

If a Printer Operation, set the sequence counter to seven to commence/continue the transfer of characters to the output buffer.

D26F to zero

D26F is unconditionally cleared because all printers appear the same to the logics from this point on.

SEQUENCE COUNT SEVEN

Entry into this state is from the SC=10 state.

SC + 1

If the Holdover Flip-flop (HOLF) is On, advance the sequence counter to eight.

SEQUENCE COUNT EIGHT

Entry into this state is from SC=7.

PITL

SC=8 • PTOD activates the Printer Information Transfer Level which allows the character in the output buffer (I/O) to transfer the storage register in the Printer (LSD first).

EXNF to 1

If the Holdover Flip-flop is On and the External Flip-flop is Off (HOFF • EXNF/), then set the External Flip-flop On. EXNF serves to delay the transfer of the least significant character for one Printer Lister clock pulse.

Transfer Character (n+1) to Output Buffer Register

CC -1

If the Holdover Flip-flop is On and the External Control Flip-flop is On, then transfer the character pointed at by the character counter from the Word register to the output buffer register and decrement the character counter by one. This cycle will continue until one full word (8 characters) has been transferred.

SC + 1

If the Holdover Flip-flop (HOLF) is On and the External Control Flip-flop is On and the character counter is equal to 7, indicating that eight characters have been transferred, advance the sequence counter to continue the operation.

SEQUENCE COUNT ELEVEN

Entry into this sequence count is when the word counter is equal to zero at sequence count 9.

Clear OB

Unconditionally, clear the output buffer register.

SC + 1

With the Holdover Flip-flop (HOLF) On and no paper motion in the Printer (D25F set), advance the sequence counter to 12. The operation may be delayed at this point by I27S/ being false indicating paper motion from the previous line of print has not been completed. D25F is set when I27S/ goes true.

D21F to 1

If the end-of-page level is true (I28D) and Holdover Flip-flop (HOLF) On and channel 0 is designated (DCOS), that is not skip digits, then set the end-of-page designated bit (D21F).

SEQUENCE COUNT TWELVE

SC + 1

Unconditionally, count the sequence count to 13.

LPR to OB

If it is not the end-of-the page or end-of-page with a skip specified (D21F/), transfer the format control bits from the longitudinal parity register to the output buffer register. The format control bits were originally transferred to the parity buffer register at Sequence Count 2.

SEQUENCE COUNT THIRTEEN

PLCL

Unconditionally, allow the Printer Lister Command Level to transfer the format control digits into the Format Control Flip-flops in the Printer. PLCL also initiates a Printer print cycle.

EPRL

If it is not the End-of-Page or End-of-Page with a skip specified (D21F/), activate the End-of-Page Reset Level (EPRL).

SC + 1

If the Holdover Flip-flop (HOLF) is On, advance the sequence counter to 14.

D17F to zero

D17F is unconditionally cleared because it does not represent an error condition.

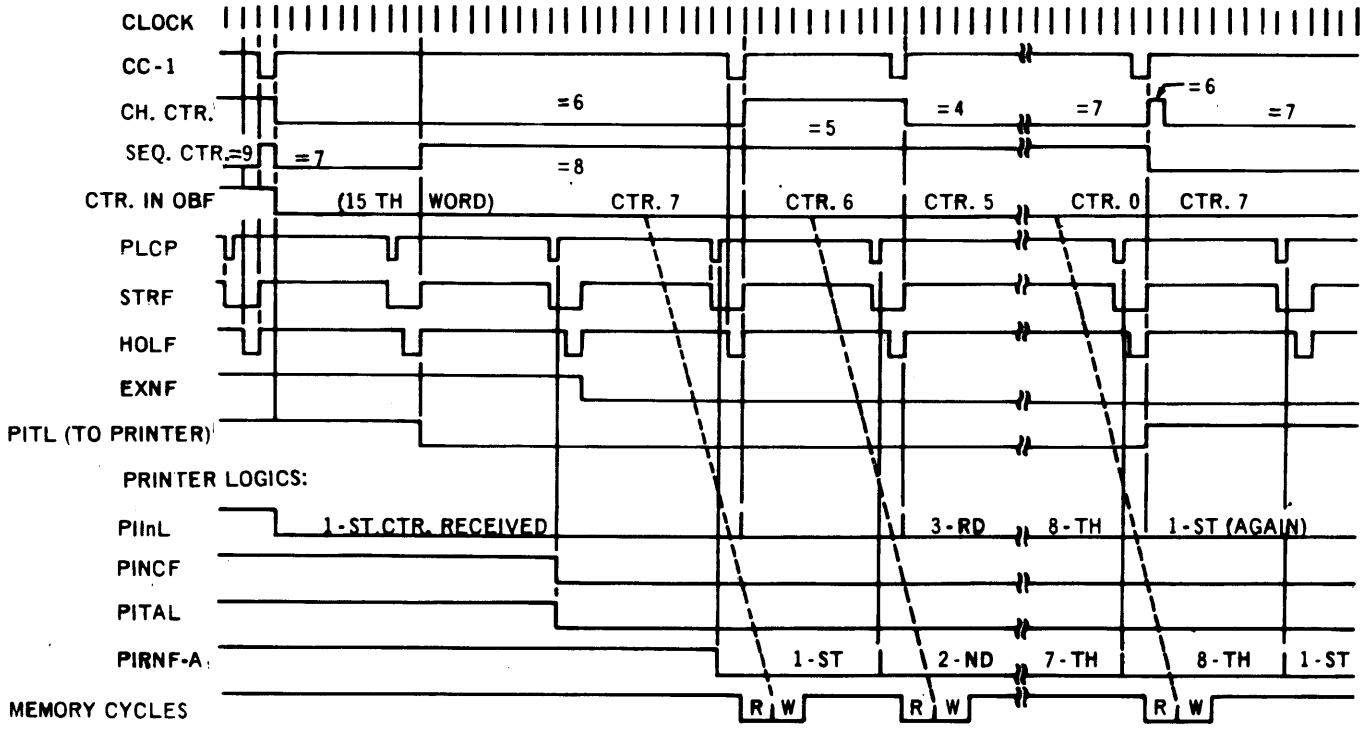


FIGURE 4-5. INFORMATION TRANSFER AT SC = 8

SEQUENCE COUNT EQUAL TO FOURTEEN

At SC=14 the result descriptor in D is shifted to W. The address portion of the D register is then set with the octal address where result descriptor now in W is to be stored in memory. This octal address is cell 14 for I/O #1, cell 15 for I/O #2, cell 16 for I/O #3 and cell 17 for I/O #4.

This sequence count is where the result descriptor is transferred from D and assembled in the word register.

W16F to 1

If the Designated unit was busy (D16F/), D17F is Off, and the Transfer D register to W register level is true (will be at SC=14), then set the W16F bit On to indicate unit busy in the result descriptor being constructed in W.

W18F to 1

If the designated unit was not busy (D16F), D17F is Off, and the designated unit was

not-ready (D18F/) and the transfer D to W level is present, set the unit not-ready bit (W18F/) On in the result descriptor being constructed in W.

D[45 ➡ 01] to W[45 ➡ 01]

If the transfer D to W level is true (DWSD), then transfer D to the W register.

D[15 ➡ 01] to 0

Clear the 10 high order bits of the address portion of D if the Clear D register level is true (CDRD-1). This will set the high order portion (module and area) of the address for storage of the result descriptor.

D03F to 1

Set the 4-bit On in the address portion of the D register if the clear D register level is true (CDRD-1). All of the result descriptor addresses have the 4 and 8 bits On.

D04F to 1

Set the 8's bit on in the address portion of the D register if the clear D level is true (CDRD-1). This sets the other common bit needed to address the result descriptor storage area.

D01F to 1

If the I/O Control Unit is designated as 2 or 4, set the first bit in the address portion of D. For I/O 2: this, in conjunction with the previous setting of the 8 and 4 bit and the reset of the 2 bit, will place an address of 13 in the address field in D. For I/O 4: this, in conjunction with the setting of 8 and 4 bits and the setting of the 2's bit, will result in an address of 15 in the address field in D.

D02F to 1

If the I/O Control Unit is designated as 3 or 4, set the 2's bit On in the address field in D. For I/O 3: this, in conjunction with the previous conditions and the setting of the 1's bit to zero, will result in an address of 14 in the address field in D.

D01F to 0

If the I/O Control Unit is designated as 1 or 3, indicating address of 12 or 14 required, turn off the 1's bit in the address field in D.

D02F to 0

If the I/O Control Unit is designated as 1 or 2, indicating an address of 12 or 13, then turn off the 2's bit in the address field in D.

SC + 1

Unconditionally, count the sequence counter to 15.

SEQUENCE COUNT EQUAL FIFTEEN

MANF to 1

Unconditionally, set the Memory Access Needed Flip-flop On. The result descriptor must be stored in the memory cell reserved for it.

MAOF to 1

With the Memory Access Needed Flip-flop (MANF) On and with the Memory Write Level (MWRD) and at Memory Time Zero (MTOD) or if Memory Access (not) Permitted (MAPS/) set the Memory Access Obtained Flip-flop On.

I/O Finished

If the Remote Operation (REMF) and memory access has been obtained (MAOF), set the I/O Finished interrupt bit in Central Control.

W Register to MIR

With the Memory Access Obtained (MAOF), replace the word in the memory cell addressed by the address field of 2 (12, 13, 14, or 15) with the result descriptor in W. The result descriptor will be written into memory at write time of the memory cycle.

I/O Flip-flops to 0

With the clear I/O level true (CIOD) clear all of the I/O Flip-flops, except the W register.

W[48 → 01] to 0

With the clear I/O level (CIOD) true and the Memory Access Permitted (MAPS), clear the W register. This logic inhibits clearing of the W register for maintenance operations only.

IMCF to 1

If not in Remote Operation (REMF/), the Maintenance Recycle switch is On (RECF), and memory access has been obtained (MAOF), set the initiate Maintenance Cycle Flip-flop On to initiate another cycle.

PRINTER FINISHED INTERRUPT

Approximately 70 ms after the I/O Finished Interrupt occurs, I06F is set to indicate that Printer #1 has finished printing and spacing paper for the previous line. I06F being set forces an octal address of 25 into the Interrupt Address Register. I07F is set when Printer #2 has finished printing and spacing paper for its previous line. I07F being set forces an octal address of 26 into the Interrupt Address Register.

Only Printer #1 operation is considered here since the overall operation for Printer #1 and Printer #2 is identical. In the static state 22 PPRS/ is a false level and 22 PAML/ is a true level. Refer to Figure 2.5-6. 22 PAML/ being

switched causes 22 PAMS-E to be false. This in turn causes 22 PCYS/ to be a true level. 22 PCFS/ is a true level in the static state. This causes 22 PCFS to be false and thus prevents the setting of I06F. 22 PCFS is two cross-coupled switches which logically operate as a Flip-flop. 22 PCF is reset in a static state.

As paper motion is initiated, 22 PAML/ goes false and causes 22 PCFS to become a true level. These cross-coupled switches are now considered in the set state. About 70 ms later, 22 PAML/ goes true causing the level 22 PCYS/ to be true and I06F is set. As soon as I06F/ goes false 22 PCFS is reset to disable the set level to I06F. An octal address of 25 is forced into the Interrupt Address Register. The Master Control Program takes over from here.

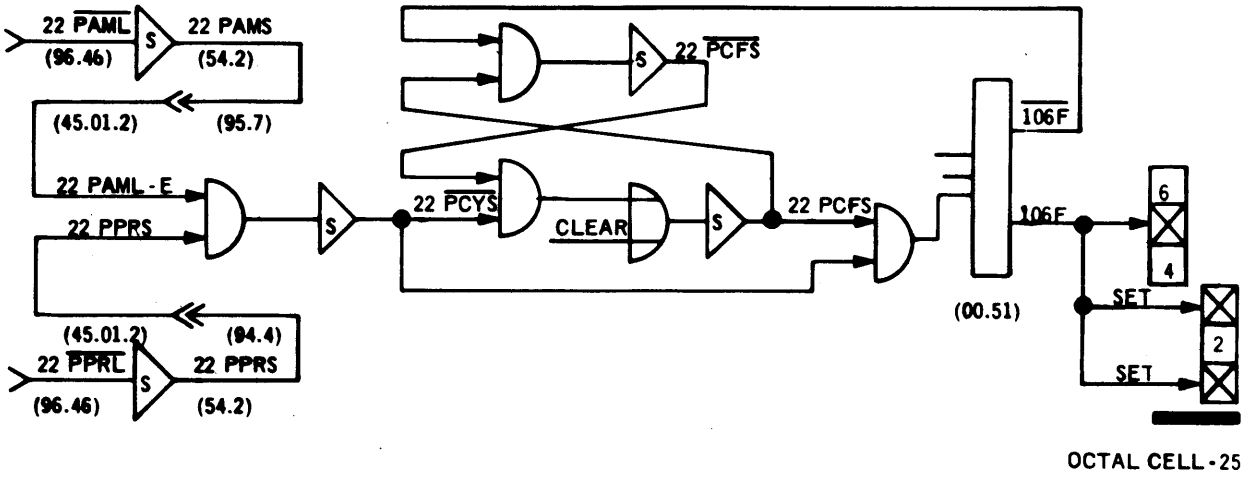


FIGURE 4-6. PRINTER FINISHED INTERRUPT

SECTION 5

MAGNETIC TAPE CONTROL

OPERATING CHARACTERISTICS

Magnetic tape is normally used as an auxilliary storage device. In this capacity, large amounts of data may be stored for future reference and can be considered as permanent storage. Approximately 12 to 15 million 7 bit characters at high density can be stored on a 2400 ft. tape.

The B422 Magnetic tape units have a capstan speed of 120 inches/second and allows reading or writing at high or low densities. A special modification kit is available to allow the 120 inch per second tape units to operate at 800 BPI. The character transfer rate is 96.0 KC.

The B423 tape units also have a capstan speed of 120 inches/second but the low density switch is locked in the low density position.

The B424 tape units have a capstan speed of 83.4 inches/second and the density select switch is locked in the very high density position. An interim B425 which is no longer available had a tape speed of 83.4 inches per second. Three tape densities were available.

The B425 tape units have a capstan speed of 90 inches/second and have a three position density switch to allow character packing densities of low density, high density or very high density.

B421 Magnetic tape units have a capstan speed of 90 inches/second with high or low packing densities selection available to the operator.

Usually all tape units connected to the B5500 system have the same capstan speed even though different model numbers may be intermixed. Any I/Ø control may access any one of 16 tape units. All tape units must function identically with any I/Ø control because only one set of tape control multi's for each density are contained in the I/Ø. Tape units operating at 83.4 inches per second and tape units operating at 120 inches per second can be intermixed on the same system. If this is done, the 120 inch per second units can operate only at 200 BPI or 555 BPI. In this case the set of 800 BPI multi's are adjusted to read tape with a capstan speed of 83.4 inches per second. These same multi's must be readjusted if 800 BPI are to be read when using a tape capstan speed of 120 inches per second. This is why one set of multi's cannot be used to read 800 BPI at two different tape speeds at the same time.

When mounting a tape reel, the operator must use the density select switch to select the corresponding density at which the tape read or write is to be performed. Consistent parity errors result on a tape read operation if the operator selects a density other than what the tape reel had previously been written. Figure 5-1 shows the character transfer rate at different capstan speeds.

All tape units rewind 2400 ft., of tape in less than 90 seconds.

TAPE SPEED	90IPS	120IPS	83.4IPS	83.4IPS	90IPS
200 BPI	18.0KC	24.0KC	–	16.7KC	18.0KC
555 BPI	50.0KC	66.7KC	–	46.3KC	50.0KC
800 BPI	–	–	66.7KC	66.7KC	72.0KC
CHANNELS	7	7	7	7	7
MTU	B 421 B 9390	B 422 B 9396	B 424	B 425 INTERMEDIATE	B 425 B 9391

FIGURE 5-1 TAPE TRANSFER RATE OPTIONS

The magnetic tape format uses standard 1/2 inch magnetic tape for data storage. The physical placement of information in character form is shown in Figure 5-2.

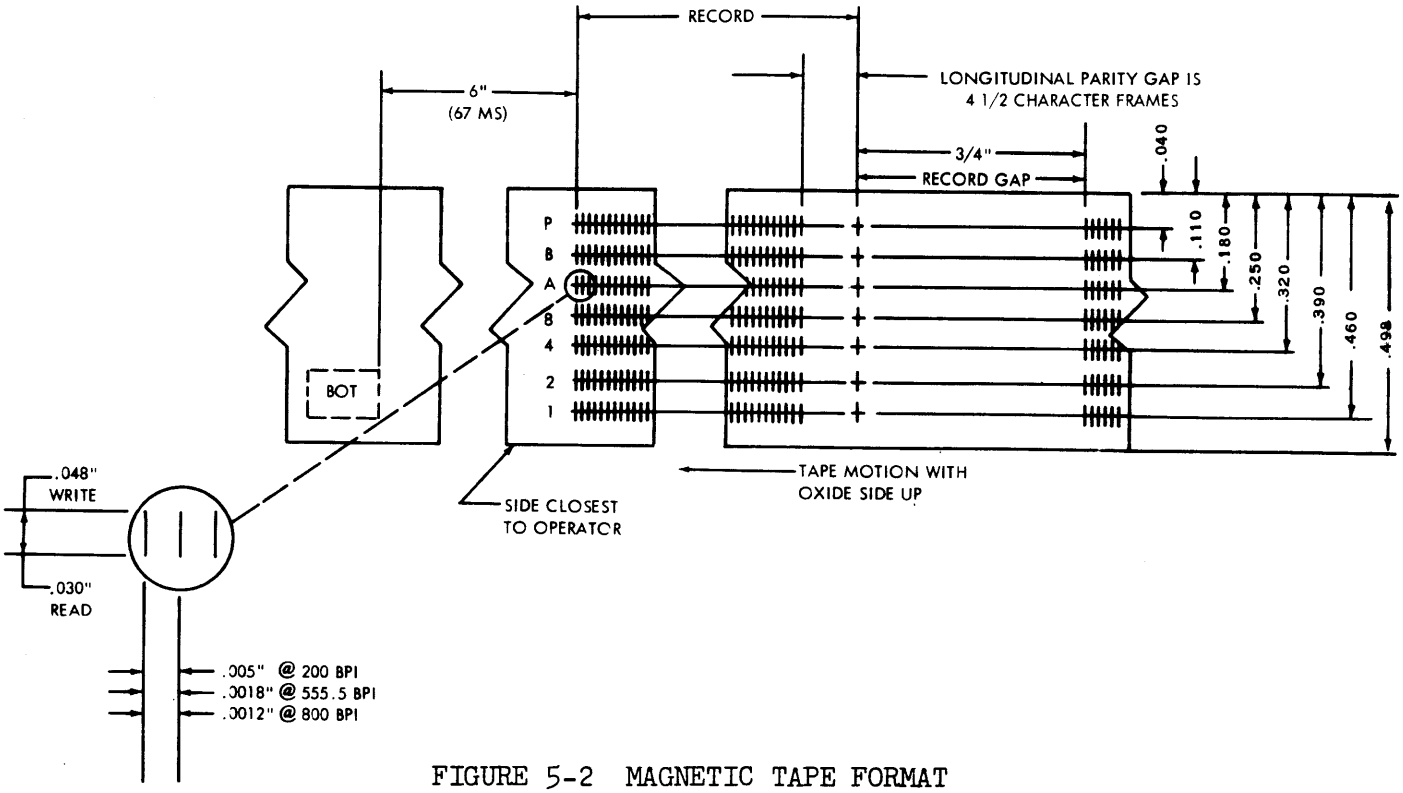


FIGURE 5-2 MAGNETIC TAPE FORMAT

INFORMATION CHARACTERISTICS

The tape format consists of 7 tracks, one of which is used for vertical parity checking. Each vertical frame (7 tracks) comprises a character that may be written in three densities; low, high, or very high. A frame refers to a one bit space in each of seven channels. In alpha mode each frame represents an

alpha character (BCL code) of 6 bits plus an even parity bit. In binary mode each frame represents a binary character (internal code) of six bits plus an odd parity bit.

Alpha information is represented by character in the B5500. Each character consists of six bits: B, A, 4, 2, 1. With these six bits, there is a possible combination of bits to form 64 characters. These 64 characters are the alphabetic characters A-Z, the numeric characters 0-9 and special characters.

When information is represented internally, as Binary information, eight characters make up a "word". The word is referred to in this way only since eight characters have a total of 48 bits, a word has 48 bits, and a character is not split between words. Alpha information is thought of as a number of characters grouped together in successive words to form a "string." The first character of a string is in the lowest memory location. The character in a string succeeding a character which occupies the last character position of a word is the first character in the word with the next higher memory location.

Information is recorded in variable length groups with blank spaces of tape between each group. These groups of information are called records. Each record is written entirely in either Alpha or Binary mode. The length of a binary coded record may be from 1 to 1023 words. The alpha write operation may be terminated by a group mark detected in the W-register or when the word counter has been counted down to zero. A tape write instruction can only be executed in the forward direction.

The longitudinal parity character is written four and 1/2 character frames after the last character of every record. A series of records followed by an End of File character is called a file. An End of File character is a BCL ">" and is the only valid one character record. All other alpha records must be at least 7 characters in length. All Binary records must be from 1 word to 1023 words long. An End of File character has the same bit configuration for both alpha and binary mode. Refer to Figure 5-3.

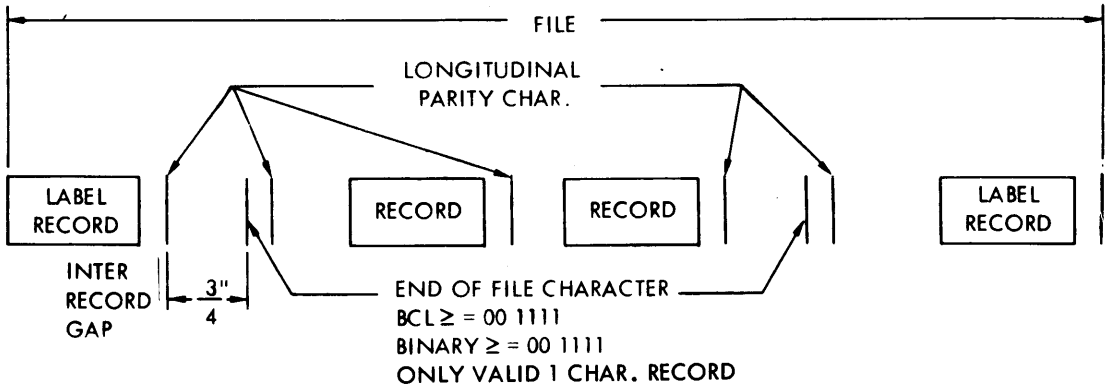


FIGURE 5-3 TAPE FILE

PHYSICAL AND DIMENSIONAL CHARACTERISTICS

Magnetic tape is made with iron oxide powder mixed with a binder which holds it to a plastic base. If the oxide is held between two layers of plastic, it is

called a sandwich tape. The magnetic tape units use non-sandwich type magnetic tape. Burroughs supplies an oxide coated tape with a 1.5 mil Mylar base. Acetate based tape (of the same size) used by some tape units can be accepted. The Burroughs tape is wound on a plastic reel with a hub diameter of 3.7 inches which fits an expandable type reel lock.

The marker strip, on the Mylar side, is placed at approximately 11 feet from the beginning of the tape. Another marking strip, on the same side, is placed approximately 15 feet from the end of the tape. These marker strips are reflective pieces of aluminum foil which are used in sensing the beginning (BOT) and end (EOT) of the tape. Refer to Figure 5-4.

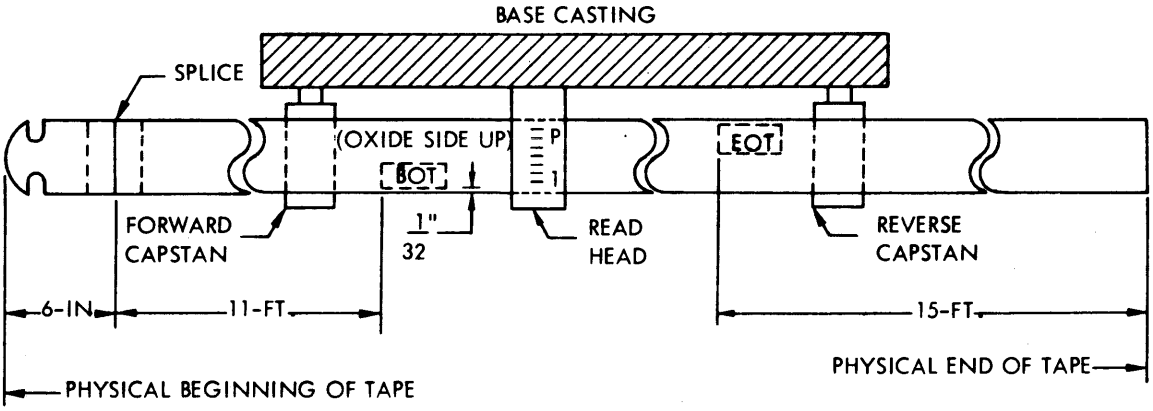


FIGURE 5-4 POSITIONING BOT AND EOT MARKER STRIPS

Two leaders are used with the TTU. A female leader, constructed of magnetic tape, is attached to the take-up reel. It is attached so that the mylar side runs next to the magnetic head. The total length of this leader is normally about 15 feet as shown in Figure 5-5. A reflective marker strip is applied to the oxide side of the leader and appears approximately 63 inches from the junction end of the leader. This marker strip is used for the unload operation and is positioned in a manner that allows it to be sensed by the EOT (End-of-Tape) sensor.

A 6-inch male leader is spliced to the file tape. This leader is constructed of non-magnetic black Mylar film. It is inserted into the female leader slot by compressing the edges.

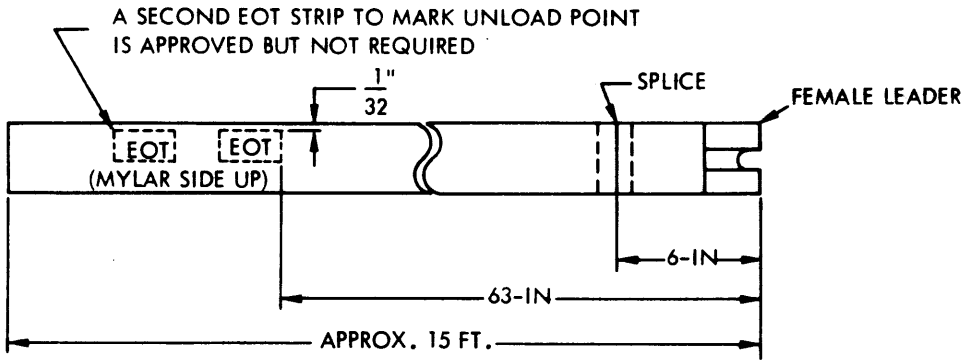


FIGURE 5-5 POSITIONING UNLOAD MARKER STRIPS

DATA DESCRIPTORS

Tape I/Ø Data Descriptors are used primarily for reading or writing on magnetic tape. Erase and Rewind are available as variants of the Write instruction. Forward and backward space are available as a variant of the Read instruction. There are other minor variants of the Read and Write instructions for maintenance purposes.

Dreg	30	24	27	26	25	Word Counter	OPERATION PERFORMED
1.	1	0	0	1	0	Not Used	Rewind (Write-Backward)
2.	0	0	0	0	0	Not Used	Write – Alpha terminated with GM in memory
3.	0	0	0	0	1	WC≠0	Write – Alpha terminate when WC=0
4.	0	0	1	0	1	WC≠0	Write – Binary terminated when WC=0
5.	X	0	1	0	1	WC=0	No Operation – Used to interrogate TTU for Ready and Write Ring
6.	1	0	0	0	0	Not Used	Erase – Alpha terminated with GM in memory
7.	1	0	0	0	1	WC≠0	Erase – Alpha terminated when WC=0
8.	1	0	1	0	1	WC≠0	Erase – Binary – 1023 words erases 15 in. at high density
9.	0	1	0	0	0	Not Used	Read – Alpha – Forward stop at longitudinal parity; I/O inserts GM
10.	0	1	0	1	0	Not Used	Read – Alpha – Backward stop at inter-record gap; no GM insert
11.	0	1	0	0	1	WC≠0	Read – Alpha – Forward word-counter end
12.	0	1	0	1	1	WC≠0	Read – Alpha – Backward word-counter end
13.	0	1	1	0	0	Not Used	Read – Binary – Forward – stop at longitudinal parity; no GM insert
14.	0	1	1	1	0	Not Used	Read – Binary – Backward – stop at inter-record gap; no GM insert
15.	0	1	1	0	1	WC≠0	Read – Binary – Forward – word-counter end
16.	0	1	1	1	1	WC≠0	Read – Binary – Backward word-counter end
17.	0	1	X	0	1	WC=0	Normal Space – Forward 1 record
18.	0	1	X	1	1	WC=0	Normal Space – Backward 1 record
19.	1	1	0	0	1	WC=0	Maintenance Space Forward 2 Records & Mark inter-record gap
20.	1	1	1	0	1	WC=0	Maintenance Space Forward & Mark time to valid record
21.	1	1	1	1	1	WC=0	Maintenance Space Backward & Mark time to valid record

X = 1 or 0

FIGURE 5-6 MAGNETIC TAPE DESCRIPTORS

Tapes created by the B5500 always have a label record about 6 inches from the BØT marker strip. The label record is the first record immediately followed by a one character (≥) tape mark record. When the EØT marker strip is sensed, the MCP writes a one character tape mark record followed by a label record. It is possible for the programmer to ignore the EØT result descriptor and continue reading or writing in the forward direction. When the physical end of tape is reached the tape unit loses vacuum and power in dropped on the tape unit.

When reading backwards and the BØT marker strip is sensed the tape logics stops tape movement and prevents all backward movement beyond the BØT marker strip.

MAGNETIC TAPE WRITE (Always performed in the forward direction)

D48,47 = 1,0 (Flag, I.D. bits)
D46 = X (Presence bit)
D45 - D41 = Unit designate.
u = 1, 3, 5, ... 31 (D41F always = 1) A, B, C→T.
D40 - D31 = Word count n specifies the number of words to be written in the binary or alpha mode. 0-1023.
If n = 0 in binary mode, there is no tape movement. This instruction used primarily by MCP.
D30 = 1 No Data Transfer (Erase or Space Operation)
D29,28 = XX (integer, continuity bits)
D27 = 0 Alphanumeric Write
= 1 Binary Write
D26 = 0 Forward
D25 = 0 Alphanumeric (terminated by group mark) - Don't use word counter.
= 1 Use word counter alphanumeric or binary (terminated after n words have been written).
D24 = 0 Output from memory (tape write).
D23 - D16 = Not Used
D15 - D1 = Starting memory address
Words are written from successively higher memory addresses.

MAGNETIC TAPE READ

D48,47 = 1,0 (Flag I.D. Bits)
D46 = X (Presence bit)
D45 - D41 = Unit Designate = 1, 3, 5, ... 31 (D41 always = 1) A, B, C→T
D40 - D31 = Word Count n specifies the maximum number of words to be transferred to memory, and is significant only if D25 = 1.

If n = 0 and D26 = 1 Backspace one record without memory transfer.

If n = 0 and D26 = 0 Forward space one record without memory transfer.

D30 = 1 Inhibit data transfer
= 0 Unit Control bit

D29,28 = xx (Integer Continuity bits)
D27 = 0 Alphanumeric Read
= 1 Binary Read
D26 = 0 Forward Read
= 1 Backward Read
D25 = 0 Transfer all character of the record to memory.
= 1 Inhibit memory transfers after the word count n has been satisfied. No group mark is stored in memory. If the tape record terminates before n has been satisfied, D25 has no effect. Tape motion stops when the inter-record gap is reached regardless of the count in the word counter.
D24 = 1 Input operation
D23 - D16 = 1 not used
D15 - D1 = Starting memory address.
Forward Read places words of the record in successively higher memory addresses.
Backward Read places words of the record in successively lower memory addresses.

MAGNET TAPE WRITE RESULT DESCRIPTORS

The basic error and control field of D16, D17, D18 and D22 are utilized.
D16 = 1 indicates unit busy - in use with another I/Ø.
D17 = 1 used as a logical flip flop for maintenance operations.
D18 = 1 Unit not Ready (power off or in local).

In addition to the basic field, the following bits are used as flags:

1. D19 = 1 Parity Error from memory to I/Ø
2. D20 = 1 Parity Error from Magnetic Tape while writing or dropout detected.
3. D21 = 1 End-of-Tape indicator (I/Ø model I and II only; not used in model III).
4. D20 and D22 = 1 Write Lockout (I/Ø attempted to write on reel without a write ring in model I, II or III.)
5. D22 = 1 Core memory address error
6. D24 ⇒ D30 See figure 5-6.
7. D34 = 1 The EØT aluminum strip has been detected.
8. D35 = 1 The BØT aluminum strip has been detected.
9. D36 = 1 Nine feet of blank tape has been detected on a read-back.
10. D37 = 1 Set if there is an information parity error from memory to I/O (model III only).
11. D46 and D19 = 1 Both flip flops are set if D34, D35, D36 or D37 is set. D46F is used on model III only to flag an extension of the normal error field.
D31, 32, and 33 not used in write result descriptor.

READ RESULT DESCRIPTOR

The basic error and control field of D16, D17, D18 and D19 are utilized the same as in a write operation.

D20 = 1 A vertical character parity error from tape to I/O on either a longitudinal parity error has been detected. In model III I/O's a drop-out being detected forces the set of the parity error flag.

D21 = 1 An End-of-file character (a BCI ≥ = 99 1111) has been detected in the IB register.

D22 Not used in a read result descriptor

D23 Not used

D24 ➡ D30 See Figure 5-6.

D31, D32, D33 Contains the contents of the character counter at End-of-operation (EOPS) time.

FORWARD: If D31 ➡ 33 = 0, the last word read was a full word. If D31 ➡ 33 ≠ 0, then the number of characters read in the last word is contained in D31 ➡ 33.

BACKWARD: D31 ➡ 33 = 7 the last word read was a full word. If D31 ➡ 33 ≠ 7 then the contents of D31 ➡ 33 subtracted from 7 equals the number of characters stored in the last partial word.

D34, D35, D36, D37 and D46 along with D19 are utilized the same as in a write operation.

TAPE OPERATIONS CONTAINING QUESTION MARKS

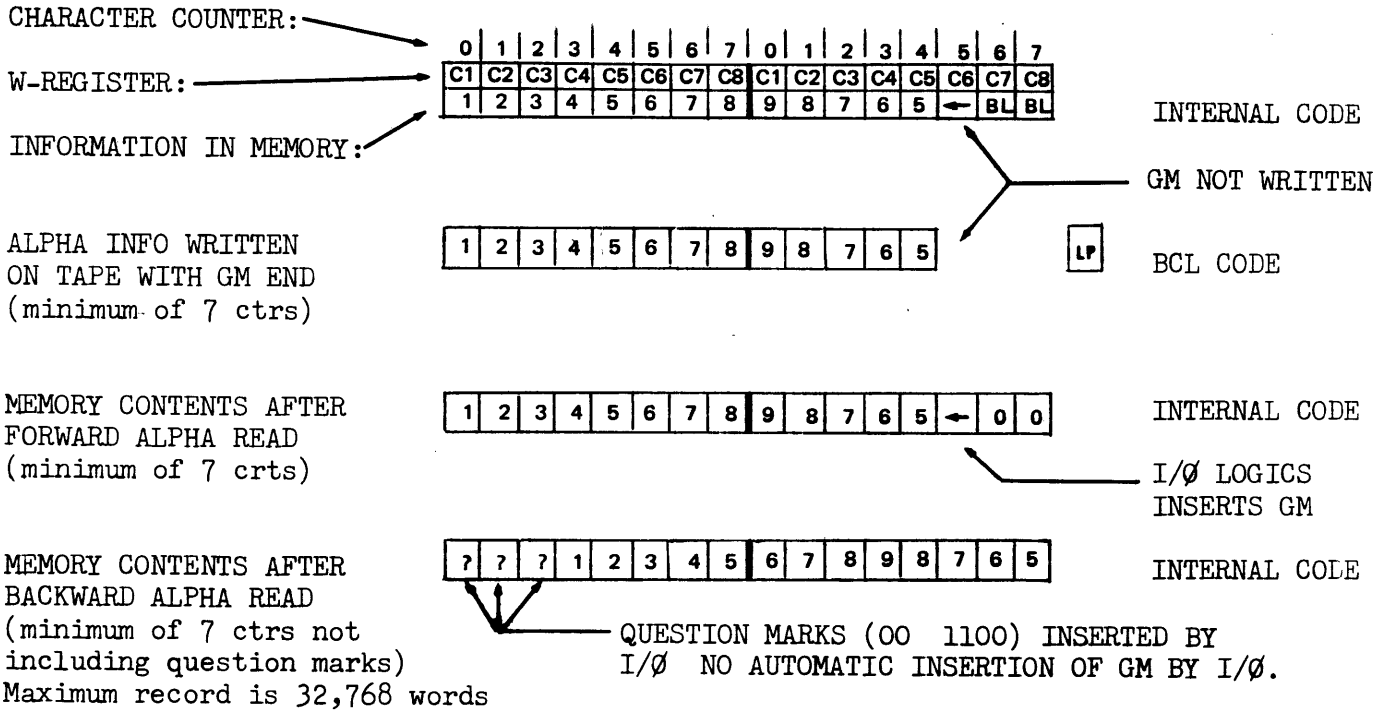


FIGURE 5-7 ALPHA READ AND WRITE WITH GROUP MARK END

NOTE

No shifting of information occurs on backward read if information on tape is in modulo eight.

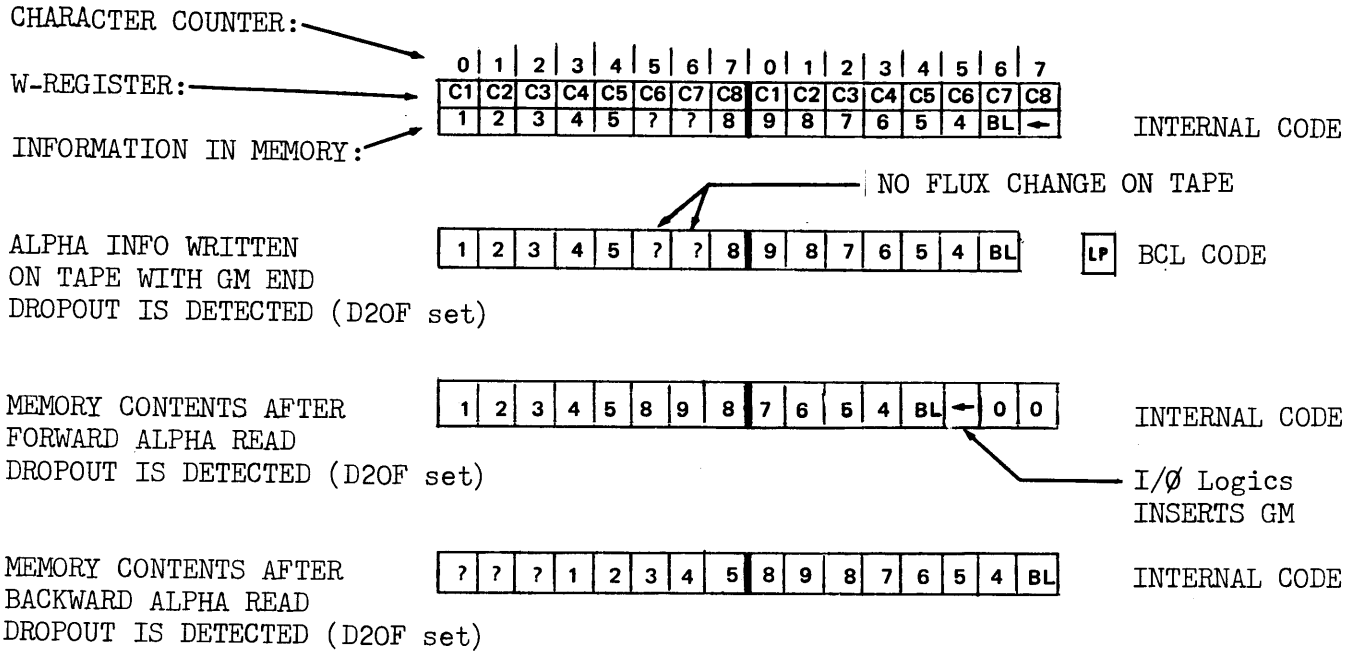


FIGURE 5-8 ALPHA READ AND WRITE WITH QUESTION MARKS

NOTE

The B5500 MCP will DS any program containing a question mark to be written in alpha on magnetic tape. However, BCL question marks may be on tapes created by other systems. Note the above results.

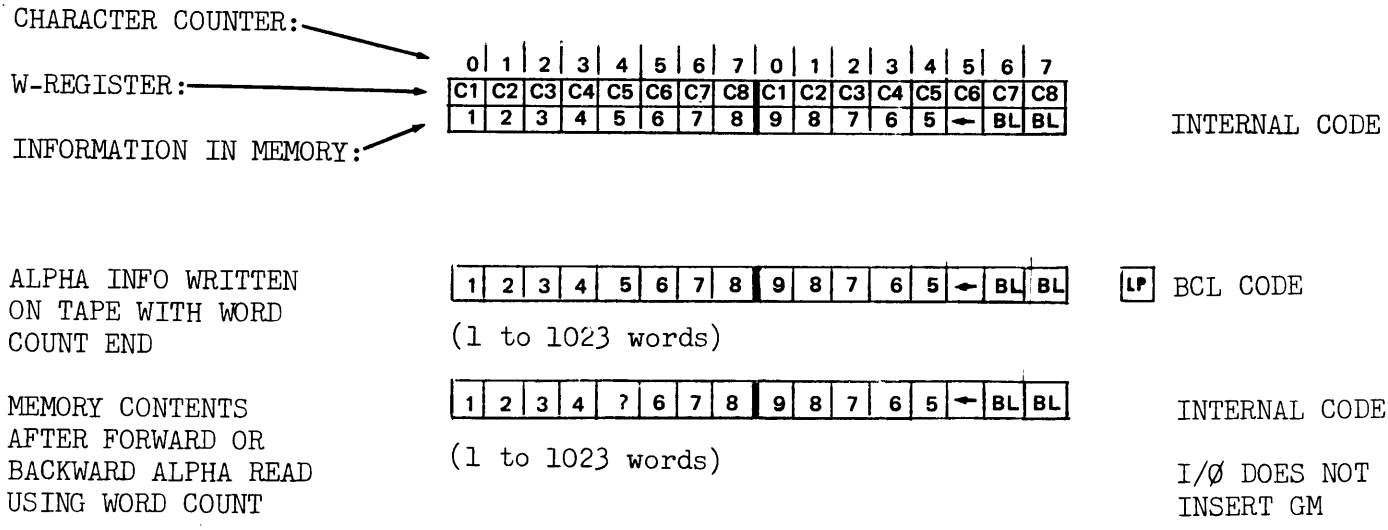


FIGURE 5-9 ALPHA READ AND WRITE WITH WORD COUNT END

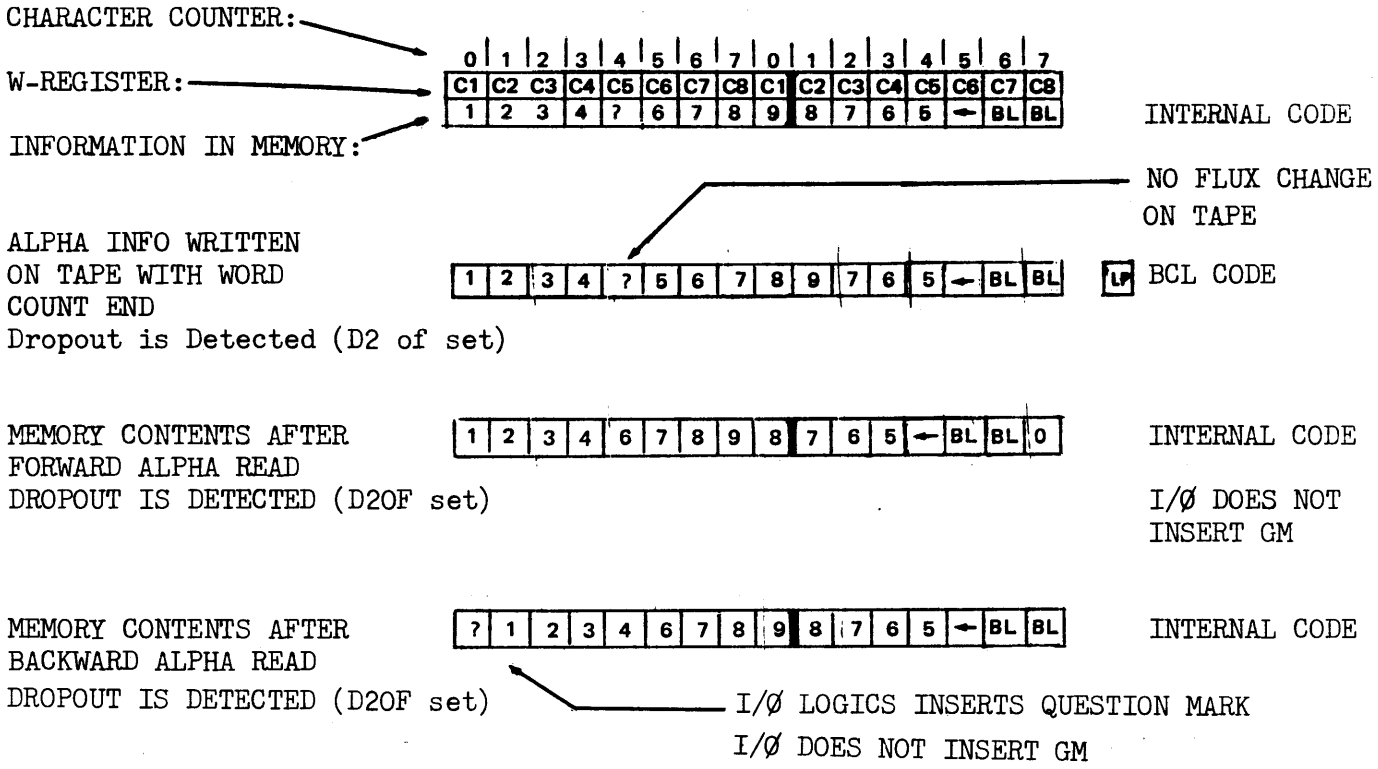


FIGURE 5-10 ALPHA READ AND WRITE WITH QUESTION MARK

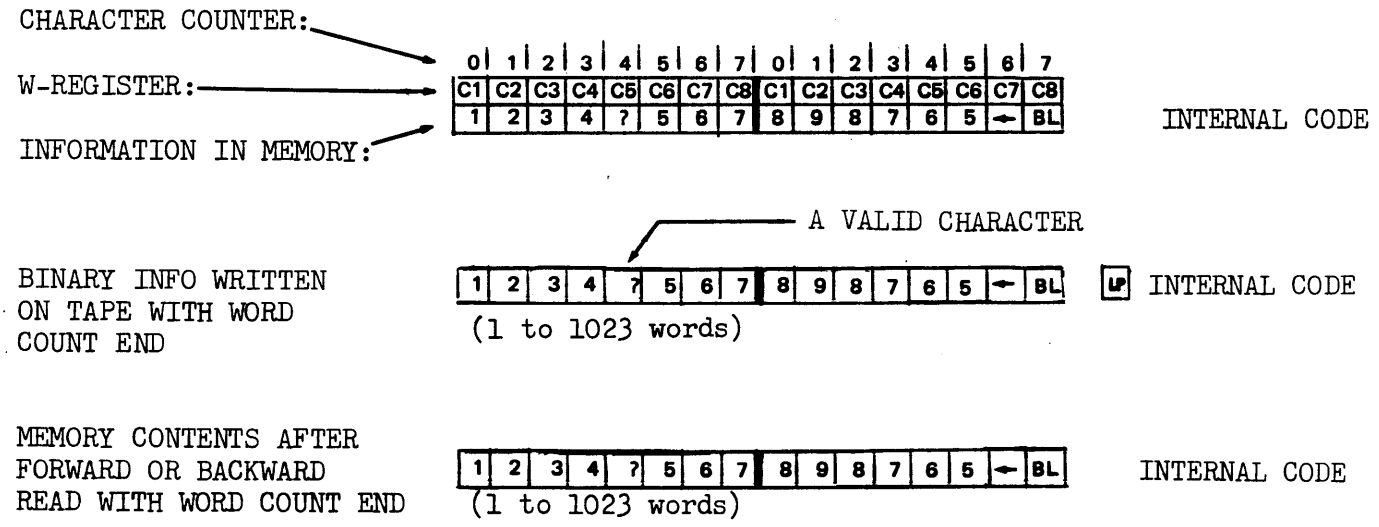


FIGURE 5-11 BINARY READ AND WRITE

NOTE

If the word counter is not used (D25F/) in a binary read, the read operation is terminated with the end of information. A group mark is not inserted by I/O on a forward or backward binary read.

B 5500 MAGNETIC TAPE GLOSSARY

2 BID 200 Bits per inch Driver: true when low density is selected

5 BID 555 Bits per inch Driver: true when high density is selected

8 BID 800 Bits per inch Driver: true when very high density is selected

ABØP A-panel blocking oscillator clock pulse

AØFF Address Overflow Flip-flop - Indicates the flip-flops D01F →D15F were all equal to one when Memory Cycle took place. Inhibits any further transfer of information to or from Core Memory.

BDL/ Backward Drive Level Not - This level is sent to the TTU through output drive Ø23D of the I/Ø Control Unit via Central Control, and when positive causes tape to drive backward providing the TTU is designed and ready.

BF2M Backward Flaw Multi for 200 BPI. This multi functions to restore the I/Ø Control read logics after any flaw has been read from tape.

BF5M Backward Flaw Multi for 555 BPI. This multi is the logical equivalent of BF2M.

BF8M Backward Flaw Multi for 800 BPI. This multi is the logical equivalent of BF2M.

BFMS/ Backward Flaw Multi Switch Not - Its output is true when BF2M, BF5M and BF8M have all timed out.

BKWF Backward Drive Flip-flop - Used to control Backward Tape Drive.

BLTM Blank tape Multi: The purpose of this multi is to prevent tape runaway during a write or read operation. When no read-back of information occurs, for 5 feet, BLTM times out and causes W36F to be set in the result descriptor.

BRIM Backward Read Inhibit Multi - This multi is used to inhibit Tape Read Level for 6.6 ms when performing a tape turnaround. A tape turnaround is when a backward read is initiated with the Tape Transport Unit in the write status.

BTDM Busy Test Delay Multi - Busy Test Delay Multi is used in the standard sequence logics at SC=3 and CC=6. This multi delays the busy test when the TTU is initially found busy. During successive forward operations the tape drive is not stopped provided the second forward operation follows the first forward operation before DSI in the tape unit has tired out. The second operation waits about 800 us or less before DSI times out. DSI is not triggered in a backward read.

BTDS/ Busy Test Delay Multi Switch Not - This is the switched output of BTDM. BTDS/ is true after BTDM has timed out.

BWIM Backward Index Multi: This multi is triggered when an Information Multi times out in a backward read. BWIM prevents the reset of BKWF for 1.2 ms to insure the TTU drives the tape well into the inter-record gap. EOPS is also produced with BWIM.

CWBD Clear Write Buffer Driver - The WB register is cleared with this driver at the beginning of the LP gap during a write operation.

D01F→D15F These 15 flip-flops are part of the D register. Normally, during an operation they always contain the address of core memory that information is being sent to or taken from. During maintenance operations, they are used to measure tape start time and inter-record gaps.

D17F During the magnetic tape operation, it is used to indicate the Mark Inter-Record Gap command, or Mark Start Time to Record command is to be executed.

D20F If a Tape Storage unit is in the Write Lockout status when attempting to execute a Write Descriptor, this flip-flop remembers it along with D22F. If a Write Descriptor or Read Descriptors is executed and a lateral parity error or longitudinal parity error is sensed, this flip-flop remembers it. D20F is also used during the Mark Start Time and Mark Inter-Record Gap commands to enable the counting of D01F→D15F portion of the D register. It is part of the Result Descriptor.

D21F This flip-flop is part of the D register. During a read operation, it flags an End-of-File Record; during a write operation, it flags the sensing of End-of-File Reflective strip. It is part of the Result Descriptor.

D22F For Tape Write, D22F is set in conjunction with D20F when the transport is found in the Write Lockout condition.

D26F This flip-flop is part of the D register. When this flip-flop is On, tape is to be driven backward during this operation. When this flip-flop is Off, tape is to be driven forward during this operation.

D27F This flip-flop when set, specifies a binary operation.

D30F For Write Descriptors D30 being on causes an Erase Operation; for Read Descriptors D30 activates the Maintenance Logic.

DØED Dropout Detected Driver - Every character read from tape re-triggers the selected lost digit multi. The lost digit multi timing out indicates one character has been dropped. However, this dropout is not detected unless another character is read before the selected information multi times out.

DS2M Digit Skew Multi for 200 BPI.

DS5M Digit Skew Multi for 555 BPI.

DS8M Digit Skew Multi for 800 BPI.

DS2S/ Digit Skew 200 BPI Switch. This switch output is true when DS2M has timed out.

DS5S/ Digit Skew 555 BPI Switch. This switch output is also true when DS5M has timed out.

DS8S/ Digit Skew 800 BPI Switch. Compatable to DS2S/ and DS5S/.

DSI Delay Standard Index-Multi located in TTU that delays the stopping of tape drive in the forward direction. Tape will continue to drive forward after the FWDF Flip-flop is turned off in the I/O. DSI is not used when moving tape backwards.

DSWM Digit Skew Write Multi: at 120 inches per second capstan speed, this multi is set at 2.5 us. This means that while writing a tape the maximum skew allowed for the characters or readback is held to within 2.5 us.

EØFL End-of-File Level - This level is produced by sensing the output of the Input Buffer. IB [8⇒1] all equal to one and IB [B⇒A] both equal zero indicates a tape mark character (≥) in BCL code has been read. This is the only valid 1 character record.

EØFS Tape End-of-File Switch - The output of this switch is true when an End-of-File character (BCL ≥) is read from tape and the Character Counter and VRCF verify that only one flux change has been read in the forward or backward direction. This is the only valid 1 character record.

EØPS End of operation Switch: this switch output is true when the end of a tape record has been sensed. EØPS indicates that either LP2M, LP5M, LP8M or BWIM is on.

EXNF During a magnetic tape operation it is used to activate the pulse counter and interlock indexing logic while the I/Ø unit is transferring information to the transport.

FDL/ Forward Drive Level Not - This level is sent to the TTU by Ø22D of the I/Ø through Central Control, and when positive, causes tape to drive forward providing the TTU is designated and ready.

FWDF Forward Drive Flip-flop - Used to control forward tape drive.

GPMS Group Marker Switch - The output of this switch will come true when ØB [B⇒1] all equal one during a write operation. (Alpha GM.)

HØLF Hold-Over Flip-flop - Used in conjunction with STRF to sync various multi functions with the one megacycle clock.

IIMS/ Information Multi Switch Not - Its output is true when IM2M, IM5M and IM8M have all timed out.

IM2M Information Multi - 200 BPI: It is set to "one" by the first flux change of a record and held over by subsequent flux changes, if they occur at 24 KC. IM2M is activated during the low density mode only.

IM5M Information Multi - 555 BPI: It is set to "one" by the first flux change of the record and held over by subsequent flux changes if they occur at 67KC. IM5M is activated during the high density mode only.

IM8M Information Multi - 800 BPI: This multi is set by the first flux change that is read from tape when the very high density switch is selected in the tape unit. This multi is retriggered with each subsequent flux change when reading 800 BPI tape.

IMCF Initiate Maintenance Cycle Flip-flop.

IMCP Initiate Maintenance Cycle Pulse.

IMFF Information Flip-flop - It remembers that one of the Information Multi's (IM2M, IM5M or IM8M) has been set.

IMIF Information Index Flip-flop - Used in conjunction with IMFF to sync the indexing logic with the one megacycle clock.

InnP Information read pulses: The InnP lines originate in Central Control and are used to transmit the 2 us tape read pulses to the Input/Output control. The tape read pulses are reshaped by pulse compressor packages to 0.5 us pulses in Central Control.

IRnF Tape Information Read Buffer - Information from the Tape Transport units is received in this buffer. It is made up of IR1F⇒IRPF.

IWSS/ IB to W register Shift Level Not: When false, this level transfers the contents of the IB register to the W register.

LCHF Last Character Flip-flop - This flip-flop, along with LPWF, remembers that the last characters of a record are about to be written on tape. LCHF and LPWF on, along with CC4F on, and the Pulse Counter equal to zero or one, form the gate to produce the Tape Write Reset Pulse.

LP2M Longitudinal Parity Multi 200 BPI: Used to delay the testing of the Longitudinal Parity Character and to generate the (EOPL) End-of-Operation Level. While LP2M is on, the Longitudinal Parity Character is read from tape.

LP5M Longitudinal Parity Multi 555 BPI: It is the high density equivalent of LP2M.

LP8M Longitudinal Parity Multi 800 BPI: It is the very high density equivalent of LP2M.

LPES Longitudinal Parity Error Switch - This level becomes true when any of the LPnF's are found off at EØPS time and SC=8.

LPIM Load Point Inhibit Multi - This multi inhibits the Tape Read Level while traversing the gap between the Load Point Reflective Strip and the first record on tape.

LPnF Longitudinal Parity [1➡P] Flip-flops - Used during the tape operations to accumulate longitudinal parity. Any one of these flip flops being off after the longitudinal parity character has been read causes LPES to be true and D20F is set to flag a parity error.

LPWF Longitudinal Parity Write Flip-flop - This flip-flop along with LCHF remembers that the last characters of a record are about to be written on tape. LCHF and LPWF on, along with the CC4F on, and the Pulse Counter equal to zero or one, form the gate to produce the Tape Write Reset Pulse.

MRD Restart Delay Multi - Located in the TTU that delays reading from tape after stopping forward tape drive and restarting another tape drive. This condition may allow the tape to come to a complete stop between records.

ØBCF Output Buffer Call Flip-flop - When set to "one", signifies that new information is to be shifted to OB.

PC Pulse Counter - The Pulse Counter counts at a one megacycle rate and is used to divide down the 1 MC clock to some predetermined rate.

PC=14/41 Pulse Counter Equal Fourteen - The PC is recycled at 14-time or 41-time during a magnetic tape operation, this providing a 66KC or 24KC recycle rate with a tape speed of 120 inches per second. Information will be read back at 15 us or 42 us intervals respectively.

PELS Parity Error Level Switch: Its output may become true when vertical parity has been violated for any character read into the IB register.

PUCF Pile-up Control Flip-flop - When on, signifies that the IB Buffer contains a character which is to be shifted to the W register.

RCNF Record Control Flip-flop - When on, signifies that the body of a record is being read from tape.

RECF Recycle Flip-flop - Used to allow consecutive maintenance cycles of a particular operation to occur.

REMF Remote Flip-flop - On when the I/Ø Control unit is in the remote mode.

RIMS/ Read Inhibit Multi Switch Not - Its output is true when both LPIM and BRIM have timed out.

SHØF Skew Holdover Flip-flop - Used in conjunction with SKFF to sync the input clocking logic with the one megacycle clock.

SKFF Skew Flip-flop - Serves as a storage element to signify the setting of one of the Digit Skew Multi's.

STRF Strobe Flip-flop - This flip-flop is used for control purposes in the I/Ø Control unit. It is turned on when it is necessary to sync in on the one megacycle clock.

TAØD Tape Operation Driver.

TCP/ Tape Clock Pulse Not - This pulse is sent to the TTU by 021D of the I/Ø through Central Control, and when positive, causes a flux change to be written on the tape. What is written on tape is controlled by the levels coming to the TTU from the outputs of the Write Buffer of the I/Ø.

TDCS Tape Drive Conflict Switch: This switch output is true when a backward read follows a write operation. This logics is used to drive tape initially forward before going backward.

TEFL/ Tape End-of-File Level Not - This level comes from the TTU via I38D of Central Control, and when positive, indicates the tape has been driven forward onto the end-of-file marker. TEFL remains positive until tape is driven backward off the end-of-file marker.

THDL/ Tape High Density Level Not - This level comes from the TTU via I37D of Central Control, and when positive, indicates the High Density Switch is in the High Density position (555 BPI) or very high density position (800 BPI).

THVL/ Tape Very High Density Level Not - This level is false when the density select switch is in the 800 BPI position.

TLPL/ Tape Load Point Level Not - This level comes from the TTU via I34D of Central Control, and when positive, indicates the load point marker has been sensed while moving tape in reverse direction. This level remains positive until tape is driven forward off the load point marker.

TREL/ Tape Read Ready Level Not is positive when all the following conditions exist:

1. Power is on.
2. Circuit Breakers are on.
3. Cabinet door is closed.
4. Tape is properly loaded in columns.
5. Vacuum pressure is correct
6. Positive Air Pressure is correct.
7. All end-of-tape lamps (EOT, BOT and PRE-BOT) are on.

8. Unit is in Remote.
9. Unit is not rewinding.
10. Restart Delay Multi (MRD) is not on.

TREL/ is true for 6 ms when MRD in the TTU is timing out.

TRL/ Tape Read Level Not - This level is sent to the TTU by Ø26D of the I/Ø through Central Control, and when positive, activates the TTU's read circuitry.

TRP-n Tape Read Pulses [B ⇒ 1] and Parity Bit - These pulses come to the I/Ø from the Central Control as I11P ⇒ I17P. The 2 us wide pulses are reshaped to less than .5 us wide.

TRWL/ Tape Rewind Level Not - This level is sent to the TTU by Ø25D in the I/Ø through Central Control, and when positive, indicates to the TTU to rewind tape.

TSCM Tape Speed Check Multi - This multi is set at the beginning of a write or read operation to check that tape has attained its proper speed.

TSCS Tape Speed Check Switch - The output of this switch goes true when TSCM times out before the first character is read at SHOF time with RCNF reset. DØED is forced true to set D2OF. In this manner the tape has been sensed as not attaining its proper speed at the beginning of a record.

TSIL Tape Standard Index Level - This level is false when Delay Standard Index is on in the TTU. This level is received in the I/Ø via I39D.

TTØL/ Tape Transport Operate Level Not - This level comes from the tape transport via I31D in Central Control. When positive this level the transport has the following conditions.

1. Power is on.
2. Circuit Breakers are on.
3. Cabinet door is closed.
4. Tape is properly loaded in columns.
5. Vacuum pressure is correct.
6. Positive air pressure is correct.
7. End of tape lamps (EOT, BOT and PRE-BOT) are all on.
8. Unit is in Remote & designated.

TWCD Transfer from W Clocked Driver - Used to shift information, a character at a time, from the W register to the Output Buffer (OB [B ⇒ 1] clocked.

TWFD Tape Write Forward Driver - Used in the I/O Control unit at SC = 4.

TWI-n/ Tape Write Information Levels [B ⇒ 1] and Parity Level Not - These levels are sent to the TTU through Central Control. A flux change is written on tape as the TCP level goes positive.

TWL/ Tape Write Level Not - This level is sent to the TTU by O24D of the I/O through Central Control, and when positive, places the TTU in the Write

Status. TWL sets the Write Status Flip-flop in the TTU if the TTU is write ready and designated.

TWRL/ Tape Write Ready Level Not - This level comes from the TTU via I35D of Central Control, and when positive, indicates the file protection ring is on the Tape Reel and TREL is positive.

TWRP/ Tape Write Reset Pulse Not - This pulse is sent to the TTU by 027D of the I/O through Central Control, and when positive, is used to reset the write flip-flops. The resetting of the write flip-flops causes the writing of the longitudinal parity character.

TWSL Tape Write Status Level - This level comes from the TTU via I36D of Central Control, and when positive, indicates the TTU is in the Write Status.

TUD6/ Tape Unit Designate Level Not - This level is grounded in Central Control and always keeps a tape unit designated.

VRCF Valid Record Flip-flop - It is set to the one state after seven characters have been read from tape.

WB Tape Write Buffer - This buffer consists of 7 flip-flops and is used to reflect the state of the Output Character to the TTU.

W [CC] Portion of the W register designated by the state of the CC.

WGBM Write Gap Beginning of Tape Multi - Used to provide a time delay between drive activation, while at Load Point of tape (TLPL = 1), and the beginning of information transfer. WGBM will provide a gap of approximately 6 inches between the Load Point Market and the beginning of the first record.

WGCM Write Gap Continuous Multi - This multi is set when the I/O initials another tape operation within about 800 us after the previous tape operation was completed. Tape does not stop between records and this multi is responsible for the 3/4 inch inter-record gap.

WGMS/ Write Gap Multi Switch Not - Its output is true when all three of the Write Gap Multi's are Off.

WGNM Write Gap Normal Multi - Used to provide a time delay between drive activation and the beginning of information transfer. The time delay is established as to provide a 3/4 inch gap between successive records. This multi is only used when tape comes to a complete stop between records.

BASIC WRITE OPERATION

In the alpha mode, a record length is determined by a group mark in memory or word count field. The group mark is the last character of a record and causes an inter-record gap of 3/4" on the tape. The group mark is not recorded on tape. This group mark is not lost because the I/O reinserts this group mark at EOPS time in an alpha forward read only.

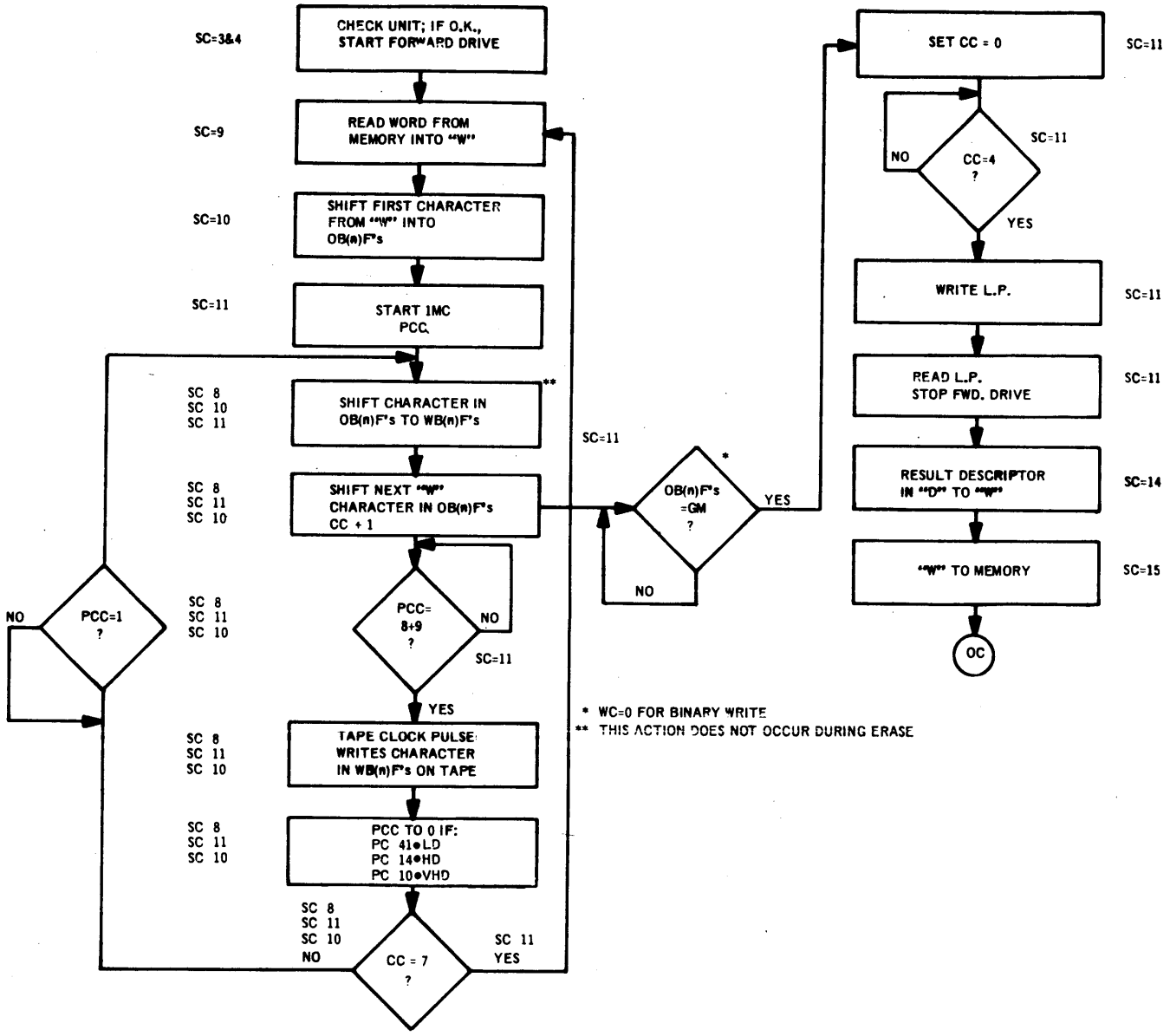


FIGURE 5-12 TAPE WRITE OR ERASE ALPHA AND BINARY

In alpha or binary mode, record length is determined by the number of words called for in the word count field of the descriptor (from 1 to 1023). At high density 1023 words requires approximately 15 inches of tape. At low density 1023 words require approximately 42 inches of tape.

If a binary write is specified with a word count of zero, no operation of the tape unit takes place. A result descriptor is returned with appropriate indications of the following conditions: Busy - D16F/ -, Not Ready - D18F/, Write Lockout - D20 and D22F set, Beginning-of-tape - D34F set or End-of-tape - D35F set.

A binary tape end-of-file gap is not provided automatically by the Input/Output Control Unit. It is provided programmatically by erasing tape for 3 inches then writing an end-of-file mark in the alpha mode. The end-of-file record is the only valid one character record and it has the same character configuration for both alpha or binary.

If the invalid character (00 1100 - a question mark in internal mode) is included in output to magnetic tape when in the alphanumeric mode, the result will be a non-recorded area for that character space. Unless it is recorded for maintenance purposes, this character should be included only at the beginning of a record.

A memory parity error being detected during a write operation causes a group mark (internal code) to be inserted into the W-register-bits 1 through 5 - at SC=10. The operation is terminated with this group mark if a write to group mark is being performed.

If a Magnetic Tape Write extends beyond the highest memory address, the condition is signalled in the result descriptor (D22) and the operation terminated after the highest memory access (alphanumeric); or in binary operation, zeros are used to fill out the remainder of the record for word count (Binary).

If the designated Magnetic Tape Unit is in the process of stopping, the I/O Control Unit waits until it has stopped, then proceeds immediately with the specified operation. A "unit busy" flag (D16) is not set, unless the unit is still busy after the I/O Control Unit has waited long enough to permit deceleration (BTDM timed out after 6.6 ms at SC=3 and CC=6).

Magnetic Tape Erase is a variant of Magnetic Tape Write. Erase is specified by the D30 descriptor bit.

There are two options for erase:

1. Binary: The number of words to be erased (1-1023) must be specified. Specifying 1023 words erases approximately 15 inches of high density tape or 42 inches of low density tape.

2. Alphanumeric: Starting memory address is specified and tape is erased until a group mark is encountered or until the word counter is counted down to zero.

The choice of the binary or alphanumeric option is determined by the descriptor bit D27.

SEQUENCE COUNT = 3

General. The primary purpose of SC = 3 is to perform a "Busy Test Delay Cycle" in which the designated tape transport unit is interrogated for its "Busy" and "Ready" status. If the tape transport is busy (being used by another I/O) and/or not-ready, the operation is terminated and exit made to SC = 14 to notify the system through the construction of a result descriptor.

SEQUENCE COUNT = 3 and CC = 0

In sequence count 3 operation, the character counter (CC) is used as a subroutine counter. Upon entry into sequence count 3, the character counter (CC) will be at zero (CC = 0). At the first SC = 3 clock pulse CC will be counted up +1 and will be counted +1 on each clock pulse until CC4F is set at CC = 4.

$$CC + 1 = CC4F/$$

At CC = 1, D16F, the Unit Available (not busy with another I/O) flip-flop will be set if AUNS is true. AUNS is a level from Central Control that indicates that the peripheral designated in the designate field is not connected (or in use) to one of the other I/O Control Units.

$$D16F = CC = 1 * AUNS$$

NOTE

D16F is used by Central Control to complete the Unit Designate in Central Control and connect (gate through) the desired tape unit into the I/O Control. This will bring the input sensing lines, I31D-I40D, and output control lines 021D-027D into the I/O Control Unit.

At CC = 3, D18, the unit ready flip-flop will be set if I31D or TTOL (Tape Transport Ready Level) is true.

$$D18F = CC = 3 * I31D * D41F$$

$$I31D = TTOL \text{ From Tape Transport}$$

At CC = 4 the level UBZS will be used to check the peripheral tape unit designated to see if the tape unit is in a Read Ready (TREL-I32D) status with the tape units restart multi timed out. To insure that the tape is fully stopped after each tape operation, the tape unit has a restart delay multi which is started when the forward (or reverse) drive is removed from the tape unit. This multi takes 6 ms to time out which is enough to insure that tape motion is completed. During the time out of the restart multi, the level Tape Read Ready Level (TREL) is held false. I32D and UBZS are used in the I/O Control to sense and indicate this level.

$$UBZS/ = (D41F/ * I22S) + (TAOD * I32D) + (D21F * I39S * D26F/)$$

$$UBZS = (TAOD/ * I22S) + (D41F * I32D/)$$

At CC = 4, if UBZS is true (TREL is false) both CC1F and CC2F are set which sets CC = 7. However, if UBZS is false or if D16F or D18F are false, only CC1F is set which sets CC = 5.

CC2F = CC = 4

CC2F = CC = 4 * D16F * D18F + UBZS

If UBZS is true, indicating that MRD (Restart Delay Multi) located in the tape unit is still on, the CC is set to seven. The Busy Test Delay Multi, BTDM, in the I/O Control will be set with the next clock pulse. BTDM is a 6.6 ms delay and its time out is longer than MRD which 6.0 ms, therefore, TREL should go true and UBZS should go false during the time out of BTDM. CC1F is reset at CC = 7 to allow waiting for restart delay multi to time out at CC = 6.

BTDM = CC = 7 * TAOD

CC1F/ = CC = 7

The character counter remains at a count of 6 and waits for the restart delay multi to time out. When it times out, TREL and I32D will go true and UBZS will go false and reset CC2F to set CC = 4. If the TREL level stays false for longer than 6.6 ms, BTDM will time out, BTDS/ will reset D16F and D16F/ will reset CC2F. At CC = 4, CC1F will be set and the I/O Control goes to SC = 3 and CC = 5. At this time the sequence counter is set to 14 to form a result descriptor because of D16F/.

D16F/ = CC = 6 * BTDS/ (TAOD + PAOD)

CC2F/ = CC = 6 * UBZS/ + D16F/

The timing relationship of the Test-for-Busy CC = 7 cycle is shown in Figure 5-13.

D21F = TAOD * I39S * CC = 7

At sequence count of 3 and character count 4 the tape unit is checked for being busy (UBZS true). UBZS remains true while tape is decelerating to a stop after the forward flip-flop in the I/O was reset from the previous operation.

The output of the MRD (Multi Restart Delay) in the tape unit continues to remain true for 6 ms after the forward flip-flop in I/O is reset at Longitudinal Parity Character time in a tape write operation. The purpose of MRD is to allow the tape to come to a complete stop between records before restarting tape drive again. As long as MRD is timing out TREL/ is true and UBZS is held true. The I/O normally waits with the character counter setting at 6 until MRD times out. This means that tape comes to a complete stop after every tape operation.

DSI (Delay Standard Index) in the tape unit is a delay circuit that follows forward drive level and is adjusted to time out about 2 ms after the forward drive level goes false. The forward drive level goes false when the forward flip-flop is reset as the Longitudinal Parity Character is written. DSI holds the pinch rollers energized to keep the tape up to its proper speed until the read-back has been completed. Read-back is not completed until 1.25 ms after the LP character was written. This condition is caused by the physical displacement of 0.15 in. between the write head and the read head. At 120 inches/second tape speed, 1.25 ms in time

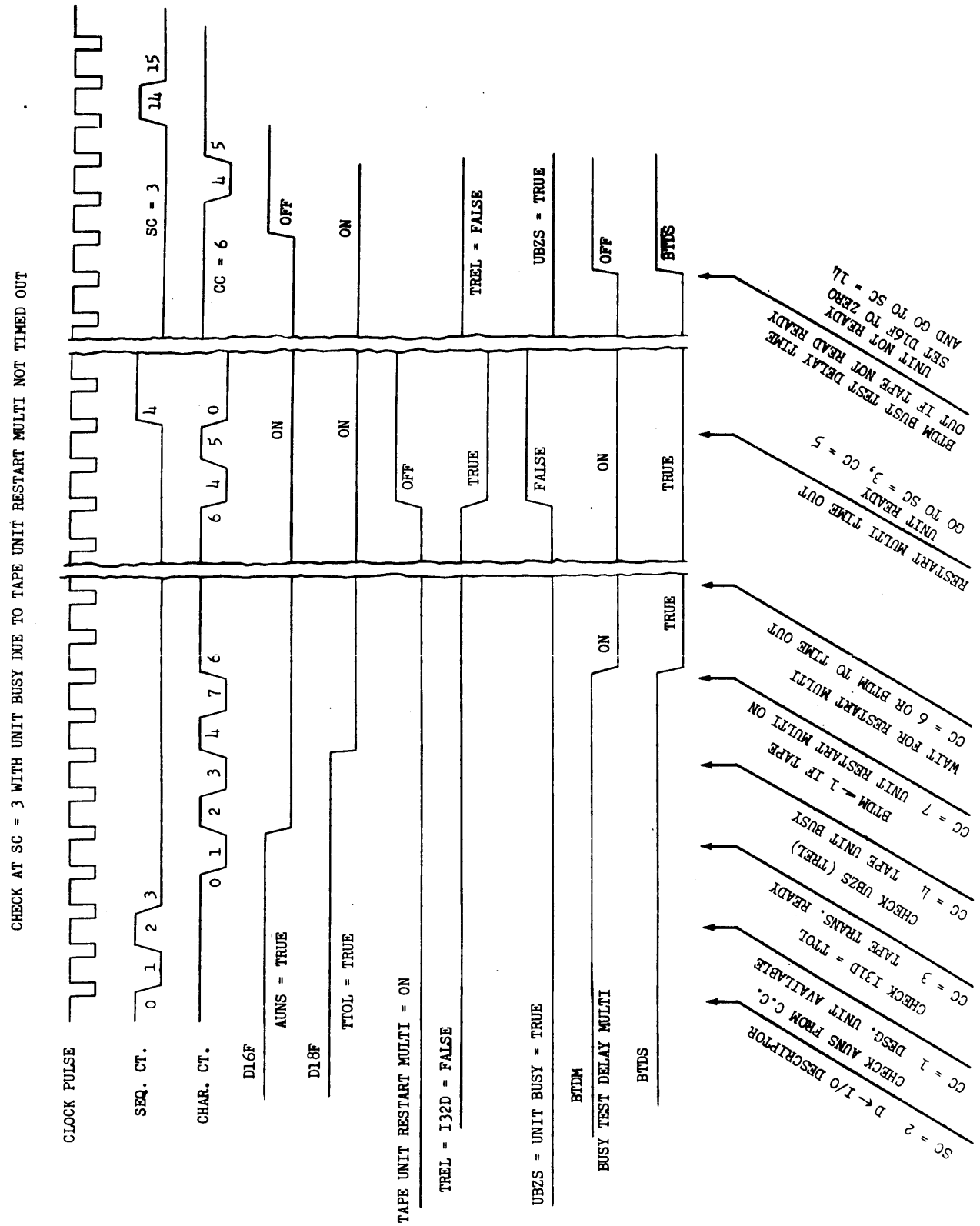


FIGURE 5-13 TEST - FOR BUSY - SC = 3

is required to move the tape 0.15 inches. DSI is adjusted to time out well after 1.25 ms to not only assure a good read-back but also to position the read-write head well into the inter-record gap. DSI remaining true causes TSIL/ in Central Control to be false and thus holding I39S true to set D21F at a character count of 6. D21F is used as a logical flag to remember that another successive tape operation is to be performed while the pinch rollers are still energized from the previous tape operation.

The I/O Finished Interrupt is set 1.25 ms after the forward flip-flop is reset in a tape write operation. If another tape write is performed within approx. 800 us after the previous I/O finished interrupt then DSI will be found timing out and D21F is set. The logics waits for DSI to finish timing out and at that time I39S/ becomes true. With D21F set, UBZS is forced false even though TREL/ is true (MRD still timing out). UBZS/ going true resets CC2F and the character counter is counted to 4 and then to 5 with the next clock pulse.

$$D21F = TAOD * I39S * CC = 7$$

SEQUENCE COUNT = 3 and CC = 5 (FIGURE 5-18)

The first clock pulse that occurs after the sequence counter is set to 3 unconditionally holds the Pulse Counter (PC) reset. After the clock counter reaches a count of 5, the Holdover Flip-flop (HOLF), the Information Buffer (IB) and the Write Buffer (WB) are all cleared.

$$PC \leftarrow 0 = SC = 3$$
$$HOLF = CC = 5 * (D24F + D26F/)$$
$$IB\ [P \Rightarrow 1]/ = CC = 5$$
$$WB\ [P \Rightarrow 1]/ = CC = 5$$

Also, the state of D16F and D18F are checked. If either D16F or D18F are reset, the Sequence Counters (SC) is set to 14. At SC = 14 the Result Descriptor is formed.

$$SC \leftarrow 14 = D16F/ + D18F/$$

In addition, if MAPS (Memory Access Permit) is true and either D16F or D18F is reset, the "W" register is cleared. DROS, which is mentioned on the flow chart, is applicable to drum logic (DROS' = not drum).

$$W\ [48 \Rightarrow 1]/ = MAPS\ (D16F/ + D18F/ + DROS/)$$

In all peripheral equipment I/O operations, except drum, it is normal to clear the W register at this time even if an error does not exist. If no error exists in drum operation the W register cannot be cleared since it contains the drum address. The common term DROS/ insures that the W register will be cleared in all peripheral equipment, except drum.

If an error does not exist at this time, PROD (Proceed) will be true and with DROS/ will set the CC = 0. Also, the SC is counted +1.

$$PROD = SC = 3 * CC = 5 * D16F * D18F$$

$$CC \leftarrow 0 = PROD * DROS/$$

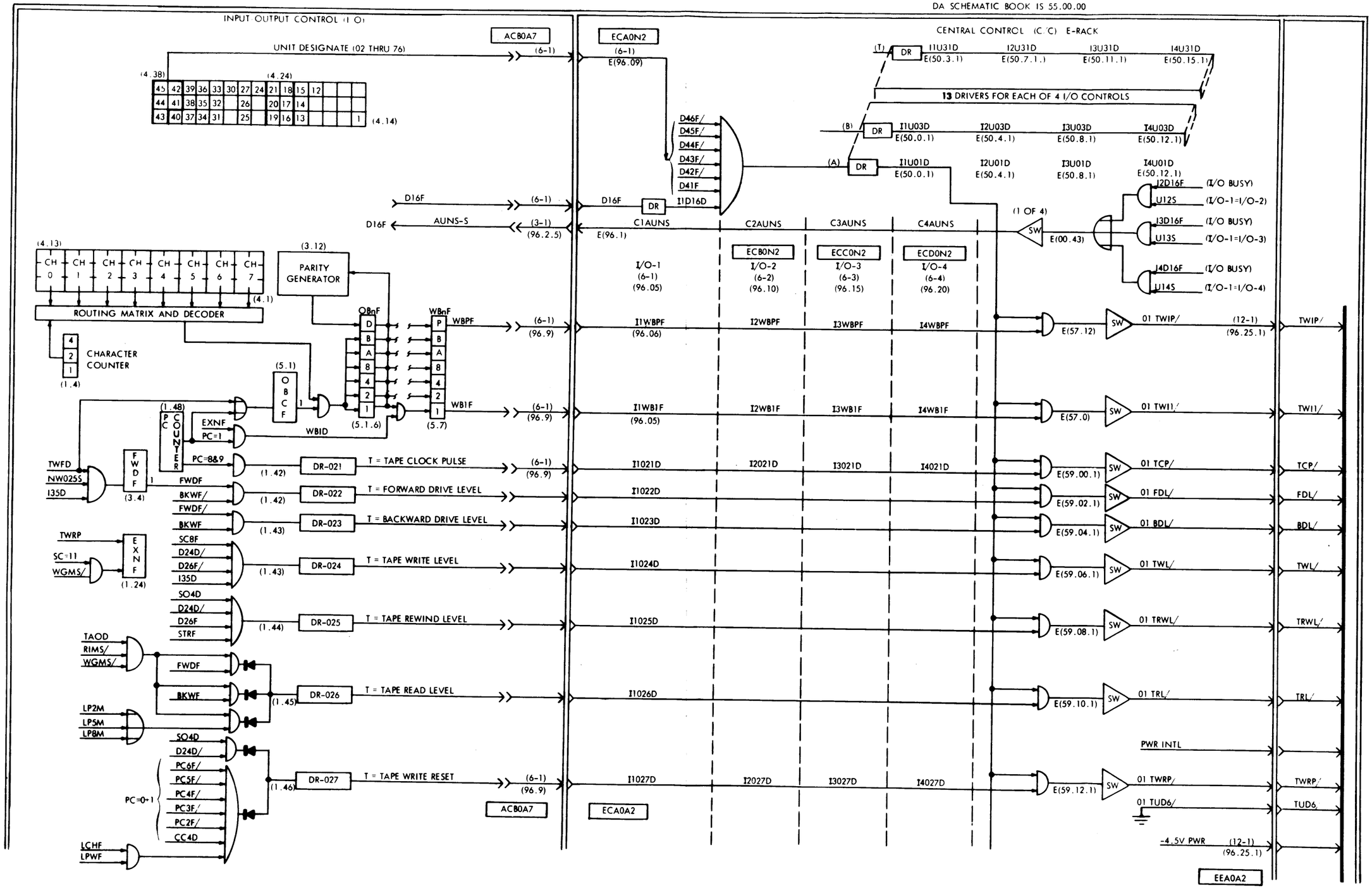


FIGURE 5-14 I/O TO TAPE SIGNAL LINES

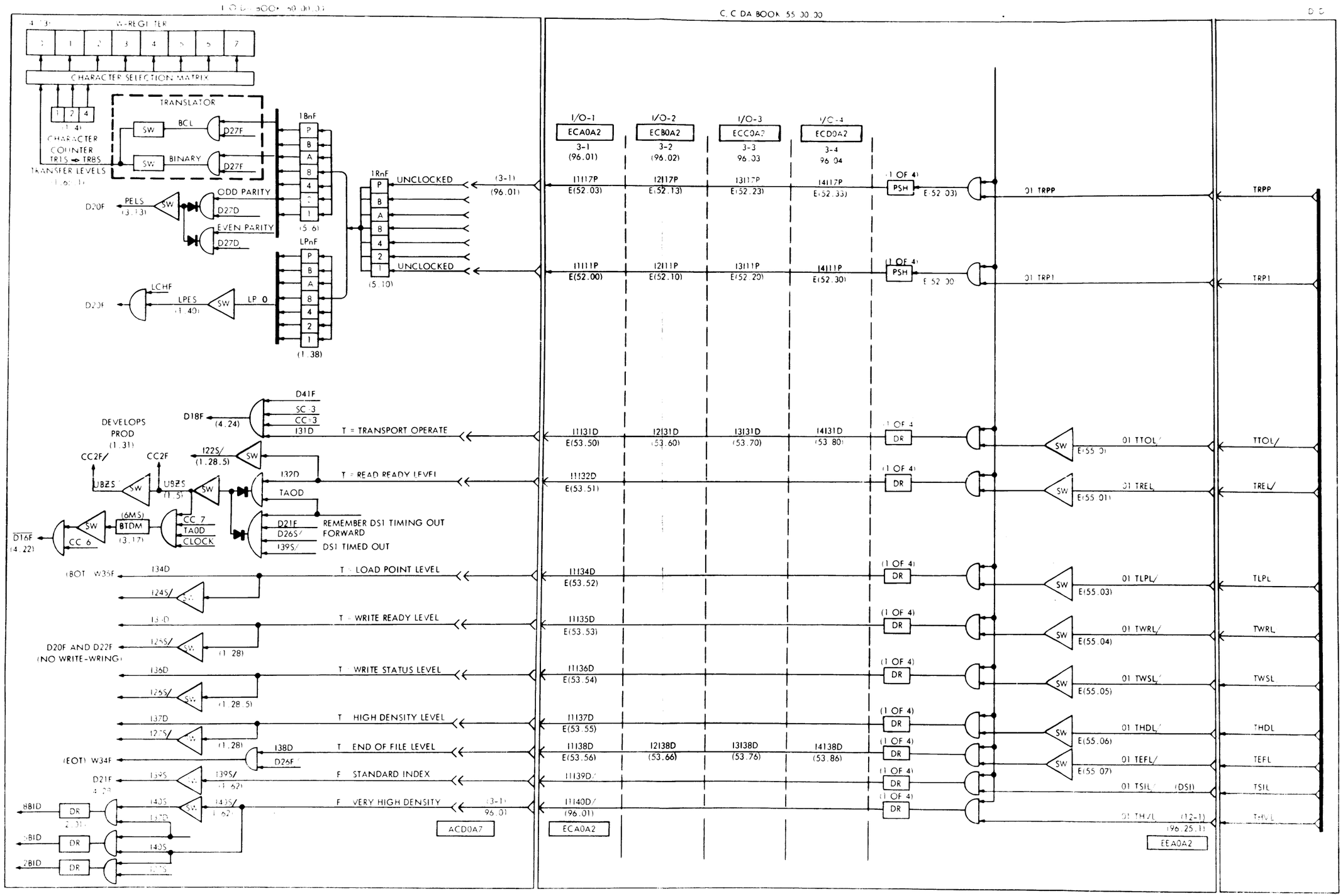


FIGURE 5-17 TAPE TO I O SIGNAL LINES

NAME	LOCATION	TYPE	DA PAGE	SETTING			SCOPE SET-UP						TAPE OPERATION	DENSITY	SPECIAL INSTRUCTIONS
				83.4 ips	90 ips	120 ips	OUTPUT	SYNC	SLOPE	A TRACE	B TRACE	MODE			
BTDM	AD B0 A2	MMN	63.03.17	7.8ms	7.8ms	6.6ms	AD B0 F0	AA D8 P2 (S03D)	NEG	AD B0 F0 (BTDM)	——	A ONLY	CONTINUOUS WRITE	ANY	SYNC POINT STARTS 6µs BEFORE BTDM.
DSWM	AA A6 A2	MUM	63.04.24	3.6µs	3.3µs	2.5µs	AA A6 F0	INTERNAL	NEG	AA A6 F0 (DSWM)	——	A ONLY	CONTINUOUS WRITE	ANY	
DS2M	AA B7 A2	MUG	63.03.03	28µs	26µs	19µs	AA B7 F0	AA A6 F0 (DSWM)	NEG	AA B7 F0 (DS2M)	——	A ONLY	CONTINUOUS READ	200 bpi	
DS5M	AA B7 N2	MUF	63.03.03	9.3µs	8.5µs	6.0µs	AA B7 U0	AA A6 F0 (DSWM)	NEG	AA B7 U0 (DS5M)	——	A ONLY	CONTINUOUS READ	500 bpi	
DS8M	AA A7 N2	MUF	63.03.03	6.0µs	5.5µs	3.9µs	AA A7 U0	AA A6 F0 (DSWM)	NEG	AA A7 U0 (DS8M)	——	A ONLY	CONTINUOUS READ	800 bpi	
LP1M	AA B8 N2	MUV	63.03.10	21ms	20ms	15ms	AA B8 U0	AA D8 V0 (S04D)	NEG	AA B8 U0 (LP1M)	——	A ONLY	REWIND FOLLOWED BY READ	ANY	
LP2M	AA B9 A2	MUJ	63.03.09	1000ms	900µs	700µs	AA B9 F0	AB C2 U4 (IMIF)	NEG	AA B9 F0 (LP2M)	——	A ONLY	CONTINUOUS WRITE OF SHORT RECORDS	200 bpi	
LP5M	AA B8 A2	MUI	63.03.09	360µs	330µs	250µs	AA B8 F0	AB C2 U4 (IMIF)	NEG	AA B8 F0 (LP5M)	——	A ONLY	CONTINUOUS WRITE OF SHORT RECORDS	500 bpi	
LP8M	AA A7 N7	MUI	63.03.14	260µs	240µs	200µs	AA A7 U5	AB C2 U4 (IMIF)	NEG	AA A7 U5 (LP8M)	——	A ONLY	CONTINUOUS WRITE OF SHORT RECORDS	800 bpi	
WGNM	AA B4 N2	MMN	63.03.10	4.7ms	4.7ms	4.7ms	AA B4 U0	AA D8 V0 (S04D)	NEG	AA B4 U0 (WGNM)	——	A ONLY	CONTINUOUS WRITE OF SHORT RECORDS	ANY	GROUND OUT AF B2 X2 (D21F) IF WRITES ARE DONE LOCALLY AND RECYCLE IS ON.
WGCM	AA B5 A2	MMN	63.03.10	5.7ms	5.1ms	5.5ms	AA B5 F0	AA D8 V0 (S04D)	NEG	AA B5 F0 (WGCM)	——	A ONLY	CONTINUOUS WRITE	ANY	
WGBM	AA B4 A2	MMØ	63.03.10	75ms	68ms	52ms	AA B4 F0	AA D8 V0 (S04D)	NEG	AA B4 F0 (WGBM)	——	A ONLY	REWIND FOLLOWED BY WRITE	ANY	
BF2M	AB B4 A2	MUI	63.03.02	400µs	350µs	250µs	AB B4 F0	AB C2 U4 (IMIF)	NEG	AA B4 F0 (BF2M)	——	A ONLY	BACKWARD READ	200 bpi	USE A RECORD FORMAT WHICH CONTAINS AN LP CHARACTER.
BF5M	AB B4 N2	MUH	63.03.02	145µs	130µs	100µs	AB B4 U0	AB C2 U4 (IMIF)	NEG	AB B4 U0 (BF5M)	——	A ONLY	BACKWARD READ	500 bpi	
BF8M	AB A4 N2	MUH	63.03.01	105µs	95µs	75µs	AB A4 U0	AB C2 U4 (IMIF)	NEG	AB A4 U0 (BF8M)	——	A ONLY	BACKWARD READ	800 bpi	
BWIM	AA B6 N2	MMQ	63.03.02	1.2ms	1.2ms	1.2ms	AA B6 U0	INTERNAL	NEG	AA B6 U0 (BWIM)	——	A ONLY	BACKWARD READ	ANY	
BRIM	AB B4 A7	DMJ	63.03.02	6.6ms	6.6ms	6.6ms	AB B4 E9	AB B4 H5 (BRIM-IN)	POS	AB B4 E9 (BRIM)	——	A ONLY	WRITE FOLLOWED BY BACKWARD READ	ANY	
IM2M	AA B6 A7	DUS	63.03.08	135µs	125µs	95µs	AA B6 F5	AA A4 W5 (TRPS)	NEG	AA B6 F5 (IM2M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE OF SHORT RECORDS	200 bpi	ADJUST MULTI TIME DURATION FROM THE NEGATIVE SLOPE OF THE LAST SHOF PULSE OF THE RECORD.
IM5M	AA B6 A2	DUR	63.03.08	50µs	45µs	35µs	AA B6 F0	AA A4 W5 (TRPS)	NEG	AA B6 F0 (IM5M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE OF SHORT RECORDS	500 bpi	
IM8M	AA A6 N2	DUE	63.01.53	35µs	32µs	25µs	AA A6 U0	AA A4 W5 (TRPS)	NEG	AA A6 U0 (IM8M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE OF SHORT RECORDS	800 bpi	
LD2M	AB A0 N2	DUF	63.03.02	85µs	78µs	58µs	AB A0 U0	AB C1 U4 (SKFF)	NEG	AB A0 U0 (LD2M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE ALPHA (7 CHARACTERS)	200 bpi	USING DELAYED SWEEP, SELECT LAST SHOF PULSE BEFORE GAP AND EXPAND THIS PORTION TO MAKE PROPER MULTI ADJUSTMENT.
LD5M	AA A9 N7	DUE	63.03.02	30µs	28µs	21µs	AA A9 U5	AB C1 U4 (SKFF)	NEG	AA A9 U5 (LD5M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE ALPHA (7 CHARACTERS)	500 bpi	
LD8M	AB A0 A7	DUQ	63.02.01	21µs	20.5µs	16µs	AB A0 F5	AB C1 U4 (SKFF)	NEG	AB A0 F5 (LD8M)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE ALPHA (7 CHARACTERS)	800 bpi	
BLTM	AA B5 N2	DMS	63.03.05	.72sec	.67sec	.50sec	AA B5 U0	AA B5 V4 (BLTM-IN)	NEG	AA B5 U0 (BLTM)	——	A ONLY	CONTINUOUS READ	ANY	USE A DEGAUSSED TAPE.
TSCM	AB C4 A2	MMQ	63.03.03	2.1ms	2.0ms	1.5ms	AB C4 F0	AB C3 U4 (FDWF)	NEG	AB C4 F0 (TSCM)	AA C9 F4 (SHOF)	ALGEBRAIC ADD	CONTINUOUS WRITE	ANY	SHOULD NOT TIME OUT PRIOR TO SHOF. TO CHECK LOGIC, CREATE TAPE DRAG WITH FINGER PRESSURE. D20F SHOULD SET.

FIGURE 5-16 MODEL III MULTI SETTINGS

At the conclusion of the test-for-busy cycle, the D register common field is sensed for certain subsequent operations. Specifically the binary erase is sensed in the write flow at SC = 3 and CC = 5. A space operation is sensed in the read flow at SC = 3 and CC = 5. Variations of the space operations is a mark inter-record gap or mark start time to valid record.

SEQUENCE COUNT = 4

If the Perform Busy Test Delay Cycle has been successfully completed, i.e., not-busy, then the write process is initiated. Events occurring and for situations developed may be summarized as follows:

1. The delay standard index flag (D21F) is cleared.
2. Blank tape multi triggered to prevent tape runaway in case of no read-back.
3. The Tape Write Reset Pulse is generated and sent to the TTU.
4. The TTU is interrogated for operational ability to perform the write operation, namely, Write Lockout. If the TTU is in the Write Lockout condition, the operation is terminated. The appropriate bits in the error field of the Result Descriptor are set and the operation exits to SC = 14.
5. If the TTU is capable of and ready for writing, the following operation is initiated:

    a. The Sequence Counter is set to 9.
    b. The Output Buffer Call Flip-flop is set.
    c. The forward drive level to the TTU is set.
    d. Either the normal gap multi (WBNM) the beginning of the tape multi (WGBN) or the write gap continuous multi (WGCM) is triggered.

A flow chart of operation is illustrated in Figure 5-18 . Since this is a magnetic tape write operation, TAOD and D24F/ are true.

HOLF is used as a logical flip-flop to set the Blank Tape Multi.

TAOD had been enabled by decoding the unit designate field of the I/O Descriptor (D45 through D41F). TAOD is merely the detection of the D41F bit which is true for all tape units (all are odd numbered).

D24F/ is true by selection (data descriptor) and indicates that this is a write operation.

These two levels, TAOD and D24F/ are combined to develop TWRP (Tape Write Reset Pulse).

$$TWRP = TAOD * D24F/$$

TWRP, in turn, is sent to the TTU through output driver 027D and used to reset the write flip-flops in the TTU. The occurrence of TWRP resets all write flip-flops containing a "one". The primary purpose of TWRP is to generate the longitudinal parity character. In this case, however, TWRP is used as a precautionary device to insure that the write flip-flops are reset prior to the write operation to follow.

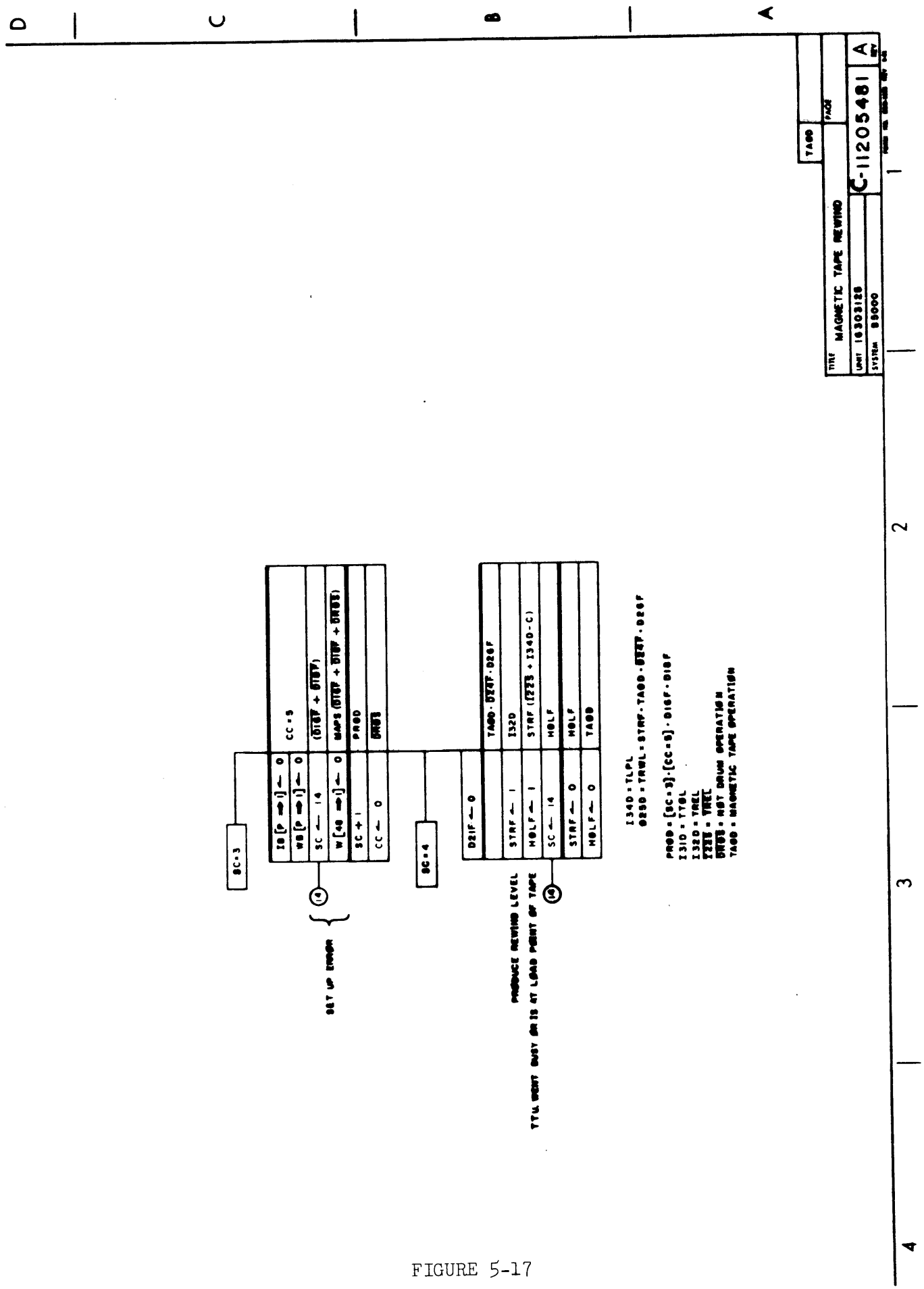

D
C
B
A
TAGD
PAGE
C-11205481
A
TYPE MAGNETIC TAPE REWIND
UNIT 10303128
SYSTEM B5000
SC-3
IB [P ⇒ 1] ← 0
WB [P ⇒ 1] ← 0
SC ← 14
W [48 ⇒ 1] ← 0
SC ← 1
CC ← 0
CC ← 5
(DIBF + DIBV)
MAPS (DIBF + DIBV + DMBS)
PROD
DMBS
SET UP ERROR
SC-4
D2IF ← 0
TAGD · DEAF · D2EF
STAF ← 1
I32D
HOLF ← 1
STAF (I22S + I34D-C)
SC ← 14
HOLF
STAF ← 0
HOLF
HOLF ← 0
TAGD
PRODUCE REWIND LEVEL
TTUL UNIT BUSY ON IS AT LOAD POINT OF TAPE
I34D : TLPL
D2EF : TRWL · STAF · TAGD · DEAF · D2EF
PROD : [SC = 3] · [CC = 0] · DIEF · DIBF
I31D : TTOL
I32D : TREL
I22S : TREL
DMBS : MDT DRUM OPERATION
TAGD : MAGNETIC TAPE OPERATION
1
2
3
4

FIGURE 5-17

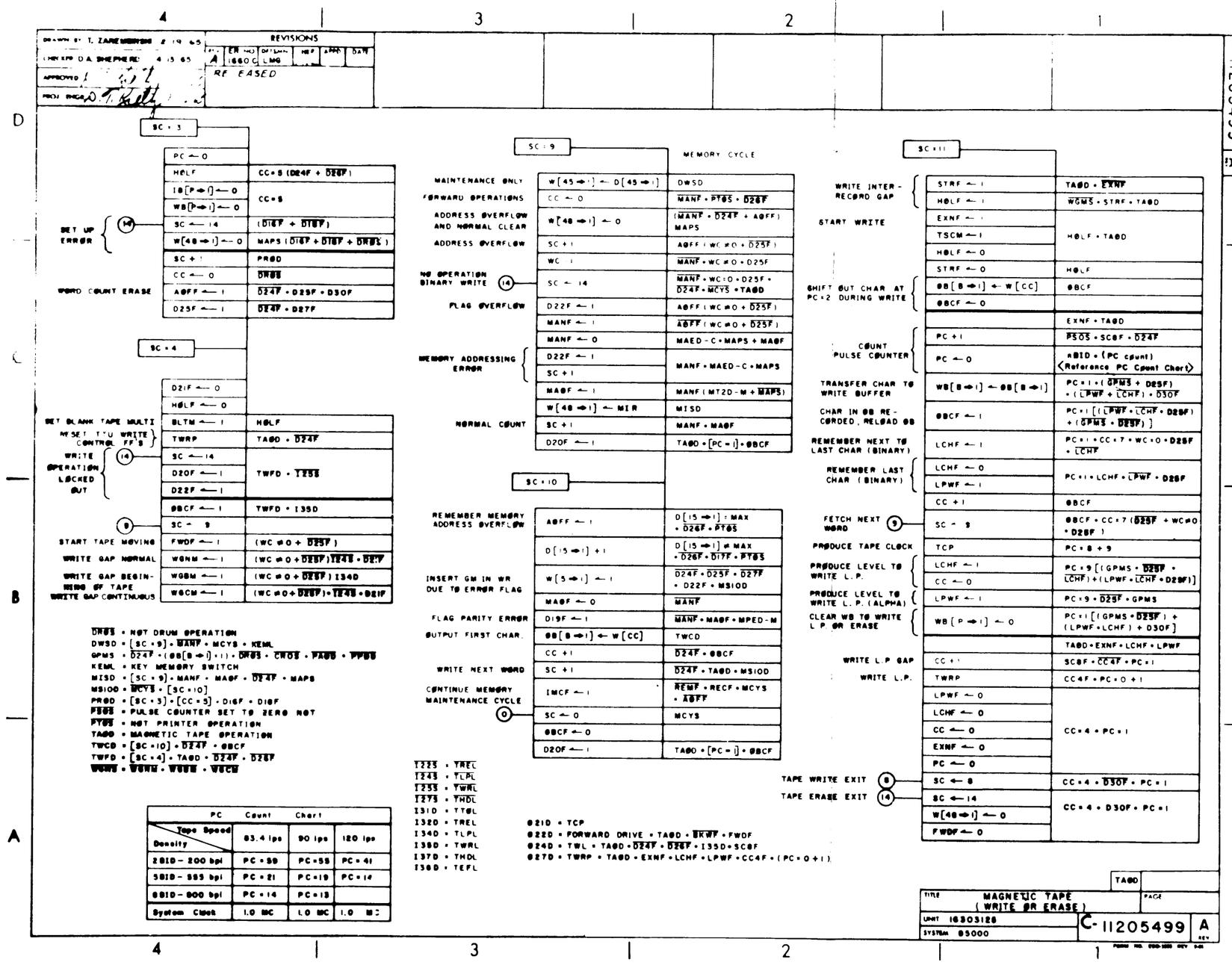


FIGURE 5-18 MAGNETIC TAPE WRITE OR ERASE

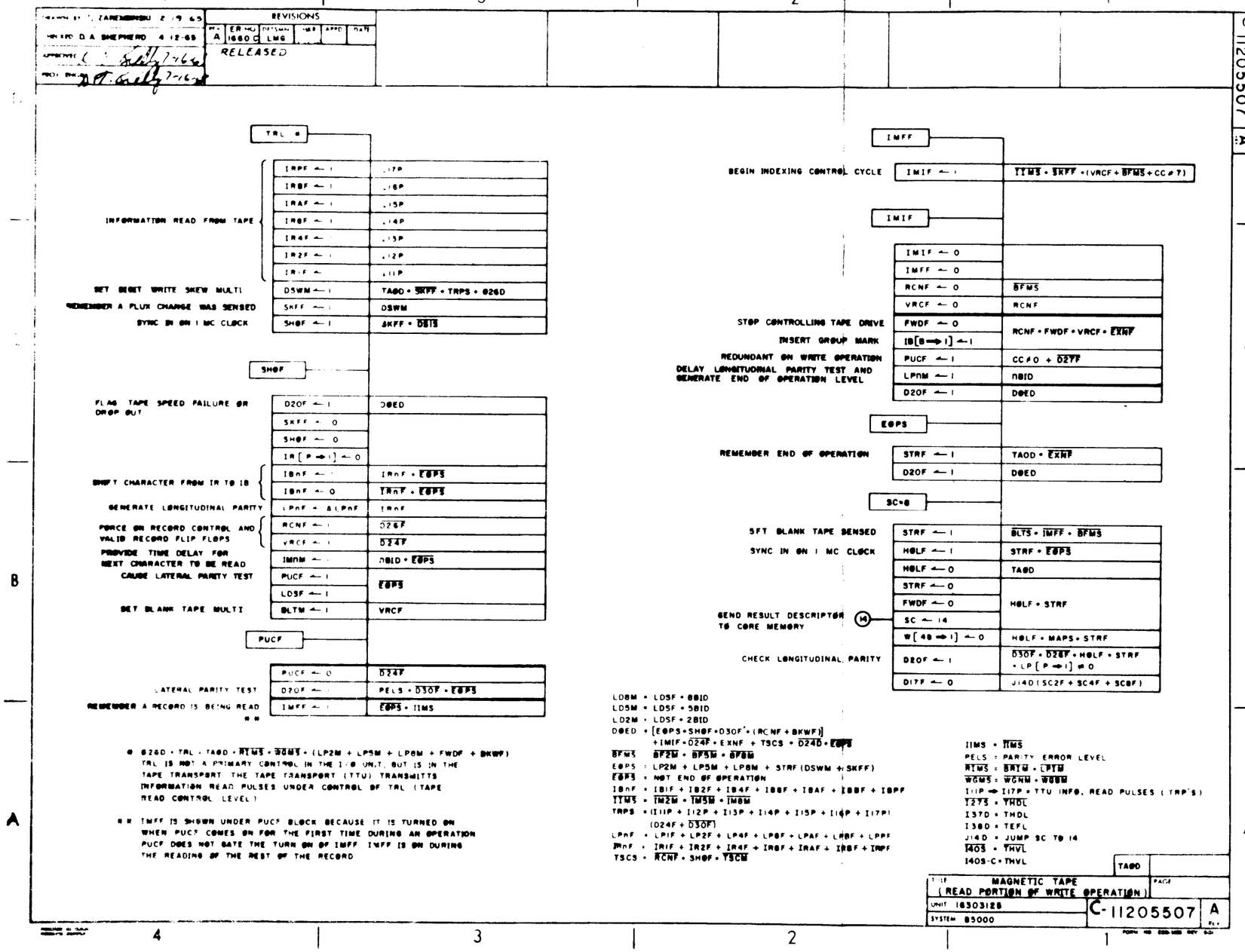

REVISIONS
A ER 1660 C LMG RELEASED
C-11205507 A
TRL ø
INFORMATION READ FROM TAPE
IRPF ← 1 .17P
IRBF ← 1 .16P
IRAF ← 1 .15P
IR8F ← 1 .14P
IR4F ← 1 .13P
IR2F ← 1 .12P
IR1F ← 1 .11P
SET BEGT WRITE SKEW MULTI
DSWM ← 1 TA0D • SKFF • TRPS • 026D
REMEMBER A FLUX CHANGE WAS SENSED
SKFF ← 1 DSWM
SYNC IN ON 1 MC CLOCK
SH0F ← 1 SKFF • D8IS
SH0F
FLAG TAPE SPEED FAILURE OR DROP OUT
D20F ← 1 D0ED
SKFF ← 0
SH0F ← 0
IR[P⇒1] ← 0
SHIFT CHARACTER FROM IR TO IB
IBnF ← 1 IRnF • E0PS
IBnF ← 0 TRnF • E0PS
GENERATE LONGITUDINAL PARITY
LPnF ← &LPnF IRnF
FORCE ON RECORD CONTROL AND VALID RECORD FLIP FLOPS
RCNF ← 1 026F
VRCF ← 1 024F
PROVIDE TIME DELAY FOR NEXT CHARACTER TO BE READ
IMnM ← 1 nBID • E0PS
CAUSE LATERAL PARITY TEST
PUCF ← 1 E0PS
LDSF ← 1
SET BLANK TAPE MULTI
BLTM ← 1 VRCF
PUCF
PUCF ← 0 024F
LATERAL PARITY TEST
D20F ← 1 PELS • D30F • E0PS
REMEMBER A RECORD IS BEING READ
IMFF ← 1 E0PS • IIMS
IMFF
BEGIN INDEXING CONTROL CYCLE
IMIF ← 1 IIMS • SKFF • (VRCF + BFMS + CC ≠ 7)
IMIF
IMIF ← 0
IMFF ← 0
RCNF ← 0 BFMS
VRCF ← 0 RCNF
STOP CONTROLLING TAPE DRIVE
FWDF ← 0 RCNF • FWDF • VRCF • EXNF
INSERT GROUP MARK
IB[8⇒1] ← 1
REDUNDANT ON WRITE OPERATION
PUCF ← 1 CC ≠ 0 + 027F
DELAY LONGITUDINAL PARITY TEST AND GENERATE END OF OPERATION LEVEL
LPnM ← 1 nBID
D20F ← 1 D0ED
E0PS
REMEMBER END OF OPERATION
STRF ← 1 TA0D • EXNF
D20F ← 1 D0ED
SC=8
SFT BLANK TAPE SENSED
STRF ← 1 BLTS • IMFF • BFMS
SYNC IN ON 1 MC CLOCK
H8LF ← 1 STRF • E0PS
H8LF ← 0 TA8D
STRF ← 0
FWDF ← 0 H8LF • STRF
SC ← 14
SEND RESULT DESCRIPTOR TO CORE MEMORY
W[48⇒1] ← 0 H8LF • MAPS • STRF
CHECK LONGITUDINAL PARITY
D20F ← 1 D30F • D24F • H8LF • STRF • LP[P⇒1] ≠ 0
DI7F ← 0 J14D(SC2F + SC4F + SC8F)
LD8M • LD5F • 8BID
LD5M • LD5F • 5BID
LD2M • LD5F • 2BID
D0ED • [E0PS • SH0F • D30F' • (RCNF + BKWF)] + IMIF • D24F • EXNF + TSCS • D24D • E0PS
BFMS = BF2M • BF5M • BF8M
E0PS : LP2M + LP5M + LP8M + STRF (DSWM + SKFF)
E0PS = NOT END OF OPERATION
IBnF = IBIF + IB2F + IB4F + IB8F + IBAF + IBDF + IBPF
IIMS = IM2M • IM5M • IM8M
TRPS = (I11P + I12P + I13P + I14P + I15P + I16P + I17P) (D24F + D30F)
LPnF = LPIF + LP2F + LP4F + LP8F + LPAF + LPDF + LPPF
IRnF = IRIF + IR2F + IR4F + IR8F + IRAF + IRDF + IRPF
TSCS = RCNF • SH0F • TSCM
IIMS = IIMS
PELS : PARITY ERROR LEVEL
RTMS = BRTM • LPTM
WCMS = WCNM • W8BM
I11P ⇒ I17P = TTU INFO. READ PULSES (TRP'S)
I27S = THDL
I37D = THDL
I38D = TEFL
J14D = JUMP SC TO 14
140S = THVL
140S-C = THVL
@ D26D = TRL • TA0D • RTMS • WCMS • (LP2M + LP5M + LP8M + FWDF + BKWF)
TRL IS NOT A PRIMARY CONTROL IN THE I/O UNIT, BUT IS IN THE TAPE TRANSPORT. THE TAPE TRANSPORT (TTU) TRANSMITTS INFORMATION READ PULSES UNDER CONTROL OF TRL (TAPE READ CONTROL LEVEL)
@@ IMFF IS SHOWN UNDER PUCF BLOCK BECAUSE IT IS TURNED ON WHEN PUCF COMES ON FOR THE FIRST TIME DURING AN OPERATION. PUCF DOES NOT GATE THE TURN ON OF IMFF. IMFF IS ON DURING THE READING OF THE REST OF THE RECORD
TA0D
TITLE MAGNETIC TAPE (READ PORTION OF WRITE OPERATION)
PAGE
UNIT 18303128
SYSTEM B5000
C-11205507 A

FIGURE 5-19

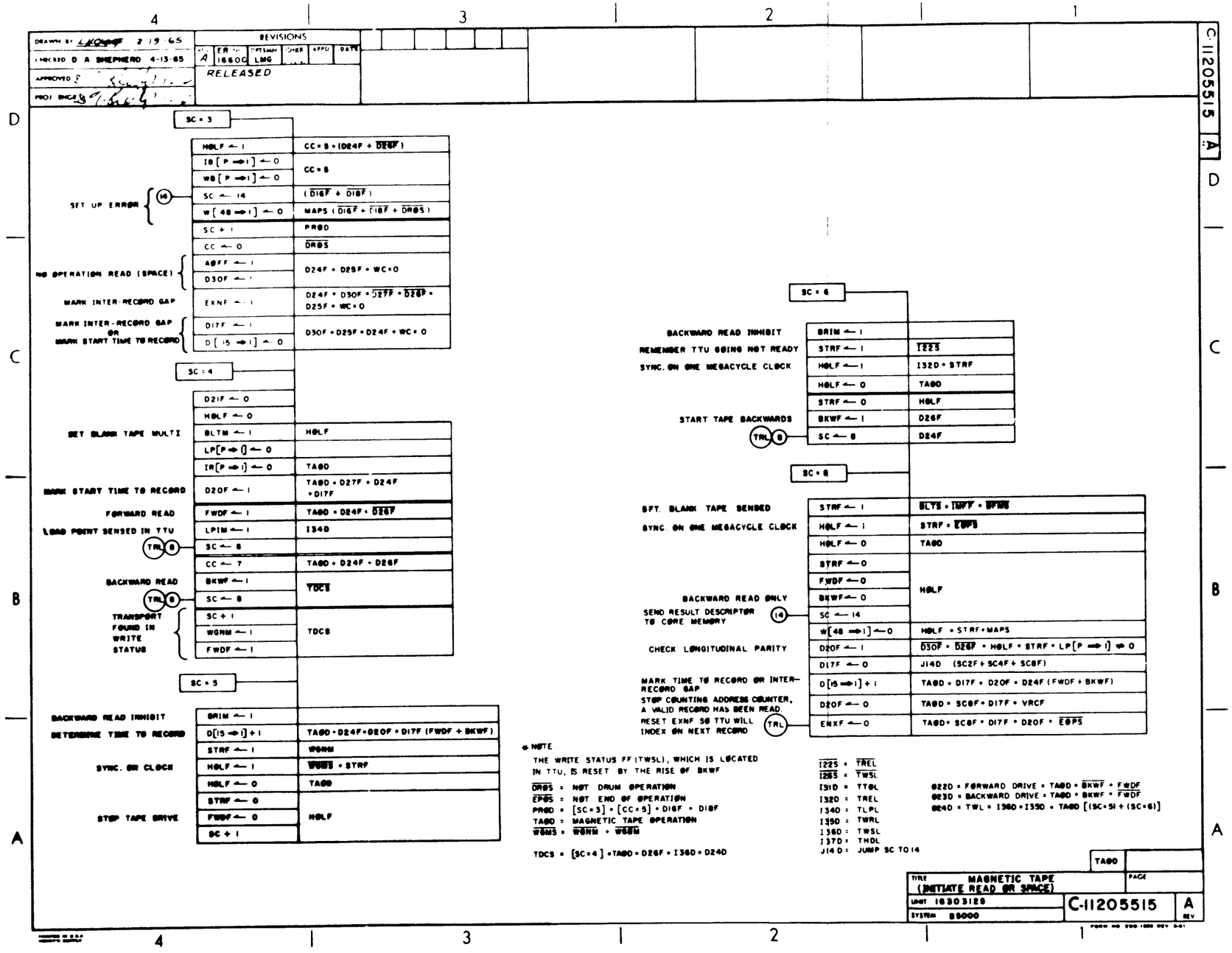

DRAWN BY L.K. Cooper 2 19 65
CHECKED D A SHEPHERD 4-13-65
APPROVED
PROJ ENGR
REVISIONS
A ER 16600 LMG RELEASED
C 1120 5515 A
SC = 3
HOLF ← 1 | CC = 5 • (D24F + D26F)
IB[P ⇒ 1] ← 0 | CC = 5
WB[P ⇒ 1] ← 0
SET UP ERROR (14) SC ← 14 | (D16F + D18F)
W[48 ⇒ 1] ← 0 | MAPS (D16F + D18F + DR05)
SC + 1 | PR0D
CC ← 0 | DR05
NO OPERATION READ (SPACE) A0FF ← 1 | D24F • D25F • WC=0
D30F ← 1
MARK INTER-RECORD GAP EXNF ← 1 | D24F • D30F • D27F • D26F • D25F • WC=0
MARK INTER-RECORD GAP OR MARK START TIME TO RECORD D17F ← 1 | D30F • D25F • D24F • WC = 0
D[15 ⇒ 1] ← 0
SC = 4
D21F ← 0
H0LF ← 0
SET BLANK TAPE MULTI 8LTM ← 1 | H0LF
LP[P ⇒ 0] ← 0
IR[P ⇒ 1] ← 0 | TA0D
MARK START TIME TO RECORD D20F ← 1 | TA0D • D27F • D24F • D17F
FORWARD READ FWDF ← 1 | TA0D • D24F • D26F
LOAD POINT SENSED IN TTU LPIM ← 1 | I34D
TRL 8 SC ← 8
CC ← 7 | TA0D • D24F • D26F
BACKWARD READ TRL 8 BKWF ← 1 | TDCS
SC ← 8
TRANSPORT FOUND IN WRITE STATUS SC + 1
W0NM ← 1 | TDCS
FWDF ← 1
SC = 5
BACKWARD READ INHIBIT 8RIM ← 1
DETERMINE TIME TO RECORD D[15 ⇒ 1] + 1 | TA0D • D24F • D20F • D17F (FWDF + BKWF)
STRF ← 1 | W0NM
SYNC. ON CLOCK H0LF ← 1 | W0NM • STRF
H0LF ← 0 | TA0D
STRF ← 0
STEP TAPE DRIVE FWDF ← 0 | H0LF
SC + 1
SC = 6
BACKWARD READ INHIBIT 8RIM ← 1
REMEMBER TTU GOING NOT READY STRF ← 1 | I225
SYNC. ON ONE MEGACYCLE CLOCK H0LF ← 1 | I32D • STRF
H0LF ← 0 | TA0D
STRF ← 0 | H0LF
START TAPE BACKWARDS BKWF ← 1 | D26F
TRL 8 SC ← 8 | D24F
SC = 8
SFT. BLANK TAPE SENSED STRF ← 1 | 8LTS • IBWF • BPMS
SYNC. ON ONE MEGACYCLE CLOCK H0LF ← 1 | STRF • EOPS
H0LF ← 0 | TA0D
STRF ← 0 | H0LF
FWDF ← 0
BKWF ← 0
BACKWARD READ ONLY SEND RESULT DESCRIPTOR TO CORE MEMORY (14) SC ← 14
W[48 ⇒ 1] ← 0 | H0LF • STRF • MAPS
CHECK LONGITUDINAL PARITY D20F ← 1 | D30F • D26F • H0LF • STRF • LP[P ⇒ 1] ≠ 0
D17F ← 0 | J14D (SC2F + SC4F + SC8F)
MARK TIME TO RECORD OR INTER-RECORD GAP D[15 ⇒ 1] + 1 | TA0D • D17F • D20F • D24F (FWDF + BKWF)
STOP COUNTING ADDRESS COUNTER, A VALID RECORD HAS BEEN READ D20F ← 0 | TA0D • SC8F • D17F • VRCF
RESET EXNF SO TTU WILL INDEX ON NEXT RECORD TRL ENXF ← 0 | TA0D • SC8F • D17F • D20F • EOPS
* NOTE
THE WRITE STATUS FF (TWSL), WHICH IS LOCATED IN TTU, IS RESET BY THE RISE OF BKWF
DR05 = NOT DRUM OPERATION
EP05 = NOT END OF OPERATION
PR0D = [SC = 3] • [CC = 5] • D16F • D18F
TA0D = MAGNETIC TAPE OPERATION
W0MS = W0NM • W08M
TDCS = [SC = 4] • TA0D • D26F • I36D • D24D
I225 = TREL
I265 = TWSL
I31D = TTOL
I32D = TREL
I34D = TLPL
I35D = TWRL
I36D = TWSL
I37D = THDL
J14D = JUMP SC TO 14
022D = FORWARD DRIVE = TA0D • BKWF • FWDF
023D = BACKWARD DRIVE = TA0D • BKWF • FWDF
024D = TWL = I36D • I35D • TA0D [(SC=5) + (SC=6)]
TA0D
TYPE MAGNETIC TAPE (INITIATE READ OR SPACE)
PAGE
UNIT 1830128
SYSTEM B5000
C-11205515
A
REV

FIGURE 5-20

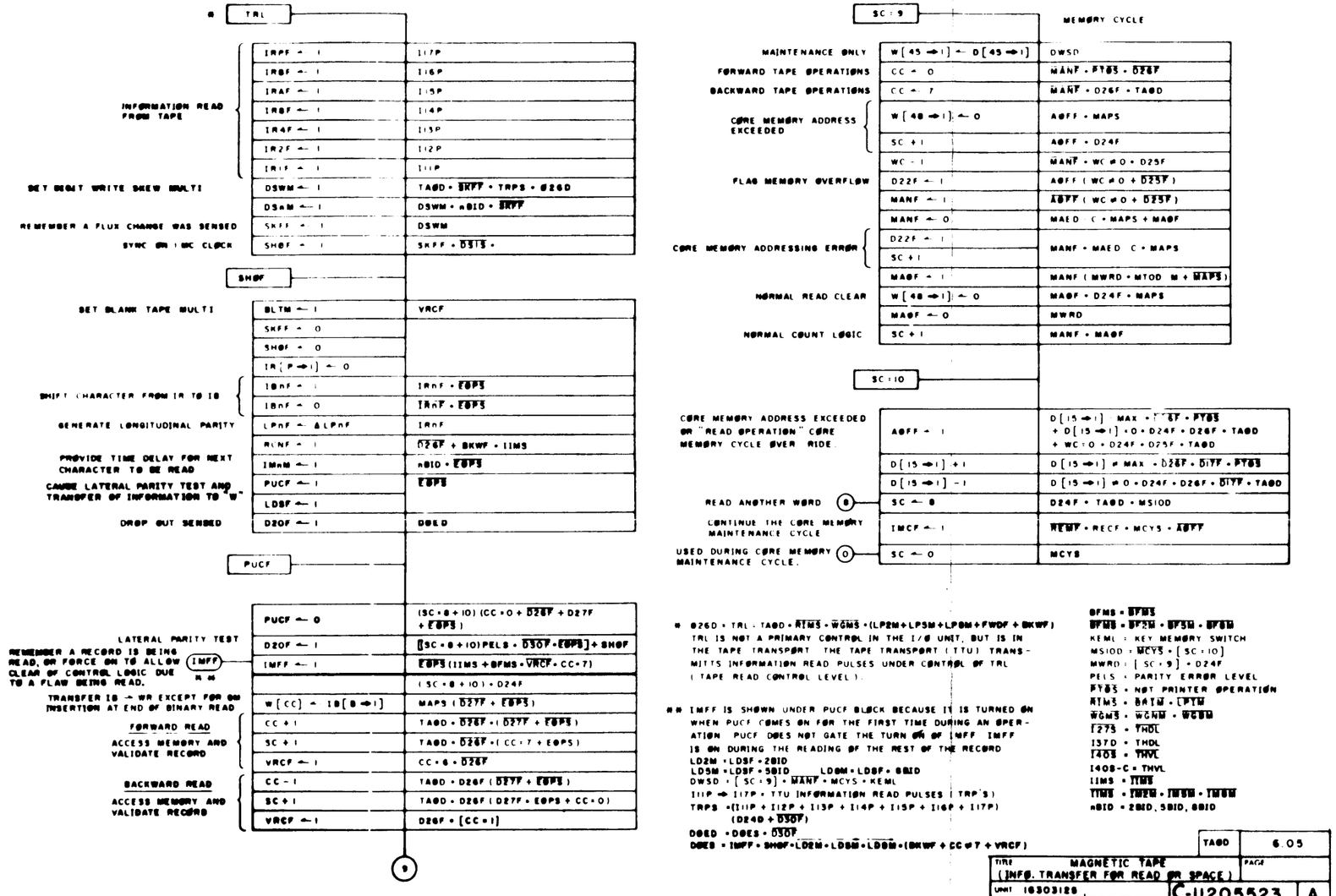
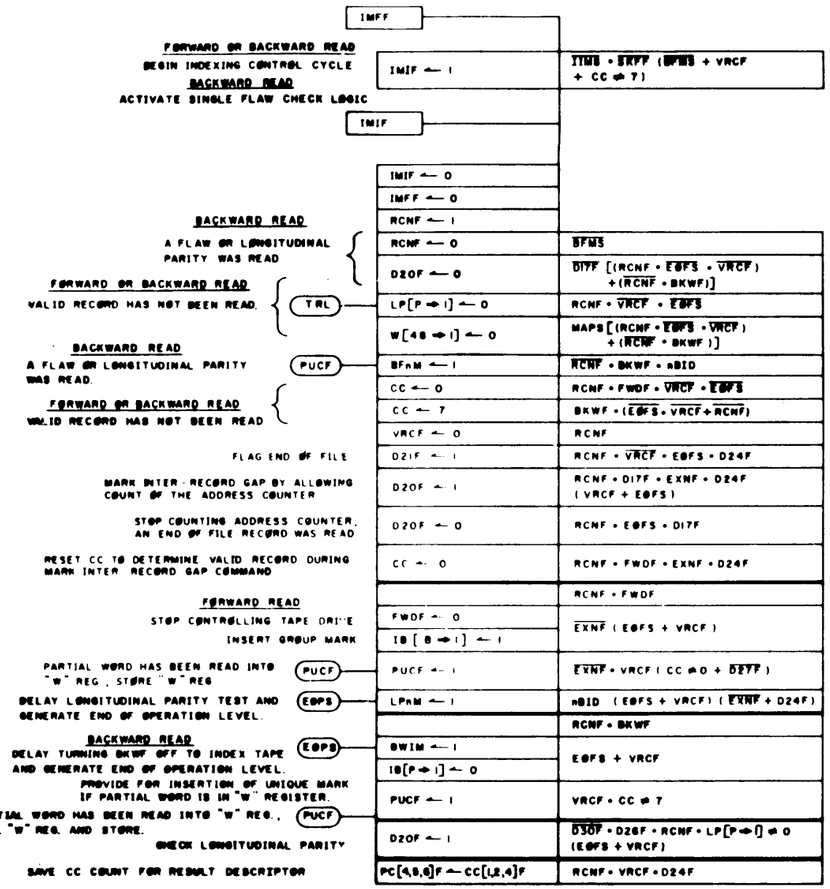

0
TRL
IRPF ← 1
I17P
IR8F ← 1
I16P
IRAF ← 1
I15P
IR8F ← 1
I14P
IR4F ← 1
I13P
IR2F ← 1
I12P
IR1F ← 1
I11P
INFORMATION READ FROM TAPE
DSWM ← 1
TA0D • SKFF • TRPS • 0260
SET EIGHT WRITE SKEW MULTI
DSaM ← 1
DSWM • nBID • SKFF
SKFF ← 1
DSWM
REMEMBER A FLUX CHANGE WAS SENSED
SH0F ← 1
SKFF • 0315 •
SYNC ON 1 BIC CLOCK
SH0F
BLTM ← 1
VRCF
SET BLANK TAPE MULTI
SKFF ← 0
SH0F ← 0
IA[P ⇒ 1] ← 0
IBnF ← 1
IRnF • EOPS
SHIFT CHARACTER FROM IR TO IB
IBnF ← 0
IRnF • EOPS
LPnF ← ALPnF
IRnF
GENERATE LONGITUDINAL PARITY
RCNF ← 1
0260 + BKWF • 11MS
IMnM ← 1
nBID • EOPS
PROVIDE TIME DELAY FOR NEXT CHARACTER TO BE READ
PUCF ← 1
EOPS
CAUSE LATERAL PARITY TEST AND TRANSFER OF INFORMATION TO "W"
LDBF ← 1
D2OF ← 1
DBED
DROP OUT SENSED
PUCF
PUCF ← 0
(SC = 8 + 10) (CC = 0 + 0260 + D27F + EOPS)
D2OF ← 1
[(SC = 8 + 10) PELS • 0300 • EOPS] + SH0F
LATERAL PARITY TEST
IMFF ← 1
EOPS (11MS + BFMS • VRCF • CC = 7)
REMEMBER A RECORD IS BEING READ, OR FORCE ON TO ALLOW CLEAR OF CONTROL LOGIC DUE TO A FLAW BEING READ.
IMFF
R ##
(SC = 8 + 10) • D24F
TRANSFER IB → WR EXCEPT FOR ON INSERTION AT END OF BINARY READ
w[CC] ← IB[8 ⇒ 1]
MAPS (0277 + EOPS)
FORWARD READ
CC ← 1
TA0D • 0260 • (0277 + EOPS)
ACCESS MEMORY AND VALIDATE RECORD
SC ← 1
TA0D • 0260 • (CC = 7 + EOPS)
VRCF ← 1
CC = 8 • 0260
BACKWARD READ
CC ← 1
TA0D • D26F (0277 + EOPS)
ACCESS MEMORY AND VALIDATE RECORD
SC ← 1
TA0D • D26F (D27F • EOPS + CC = 0)
VRCF ← 1
D26F • [CC = 1]
9
SC = 9
MEMORY CYCLE
MAINTENANCE ONLY
w[45 ⇒ 1] ← D[45 ⇒ 1]
DWSD
FORWARD TAPE OPERATIONS
CC ← 0
MANF • PY0S • 026F
BACKWARD TAPE OPERATIONS
CC ← 7
MANF • D26F • TA0D
CORE MEMORY ADDRESS EXCEEDED
w[48 ⇒ 1] ← 0
A0FF • MAPS
SC + 1
A0FF • D24F
WC = 1
MANF • WC ≠ 0 • D25F
FLAG MEMORY OVERFLOW
D22F ← 1
A0FF (WC ≠ 0 + 0235F)
MANF ← 1
A0FF (WC ≠ 0 + 0235F)
MANF ← 0
MAED C • MAPS + MA0F
CORE MEMORY ADDRESSING ERROR
D22F ← 1
SC + 1
MANF • MAED C • MAPS
MA0F ← 1
MANF (MWRD • MTOD M + MAPS)
NORMAL READ CLEAR
w[48 ⇒ 1] ← 0
MA0F • D24F • MAPS
MA0F ← 0
MWRD
NORMAL COUNT LOGIC
SC + 1
MANF • MA0F
SC = 10
CORE MEMORY ADDRESS EXCEEDED OR "READ OPERATION" CORE MEMORY CYCLE OVER RIDE.
A0FF ← 1
D[15 ⇒ 1] = MAX • 1 • 6F • PY0S + D[15 ⇒ 1] • 0 • D24F • D26F • TA0D + WC = 0 • D24F • D25F • TA0D
D[15 ⇒ 1] + 1
D[15 ⇒ 1] ≠ MAX • D26F • 01FF • PY0S
D[15 ⇒ 1] − 1
D[15 ⇒ 1] ≠ 0 • D24F • D26F • 01FF • TA0D
READ ANOTHER WORD
8
SC ← 8
D24F • TA0D • MSIOD
CONTINUE THE CORE MEMORY MAINTENANCE CYCLE
IMCF ← 1
MEMF • RECF • MCYS • A0FF
USED DURING CORE MEMORY MAINTENANCE CYCLE.
0
SC ← 0
MCYS
0260 • TRL = TA0D • RTMS • WGMS • (LP2M + LP5M + LP8M + FWDF + BKWF)
TRL IS NOT A PRIMARY CONTROL IN THE I/O UNIT, BUT IS IN THE TAPE TRANSPORT. THE TAPE TRANSPORT (TTU) TRANSMITTS INFORMATION READ PULSES UNDER CONTROL OF TRL (TAPE READ CONTROL LEVEL).
IMFF IS SHOWN UNDER PUCF BLOCK BECAUSE IT IS TURNED ON WHEN PUCF COMES ON FOR THE FIRST TIME DURING AN OPERATION. PUCF DOES NOT GATE THE TURN ON OF IMFF. IMFF IS ON DURING THE READING OF THE REST OF THE RECORD
LD2M = LD8F • 2BID
LD5M = LD8F • 5BID
LD8M = LD8F • 8BID
DWSD = [SC = 9] • MANF • MCYS • KEML
I11P ⇒ I17P = TTU INFORMATION READ PULSES (TRP'S)
TRPS = (I11P + I12P + I13P + I14P + I15P + I16P + I17P) (D240 + 0300)
DBED = DBES • 0300
DBES = IMFF • SH0F • LD2M • LD5M • LD8M • (BKWF + CC ≠ 7 + VRCF)
BFMS = BFMS
BFMS = BF2M • BF5M • BF8M
KEML = KEY MEMORY SWITCH
MSIOD = MCYS • [SC = 10]
MWRD = [SC = 9] • D24F
PELS = PARITY ERROR LEVEL
PY0S = NOT PRINTER OPERATION
RTMS = RATW • LPTW
WGMS = WG4W • WG8W
I27S = TH0L
I37D = TH0L
I40S = TH1L
I40S-C = TH1L
I1MS = TIMS
TIMS = TMFM • TM5M • TM8M
nBID = 2BID, 5BID, 8BID
TA0D
6.05
TITLE MAGNETIC TAPE (INFO. TRANSFER FOR READ OR SPACE)
PAGE
UNIT 1830328
SYSTEM B5000
C-11205523
A
REV

FIGURE 5-21



nBID = 2BID, 5BID, 6BID
TSCS = TSCM • SMOF • RCNF
BFMS = BF1M • BF5M • BF6M
EOFS = EOFL • VRCF (D3OF • CC ≠ 1 + D26F • CC ≠ 6)
EOFL = (IB[8 ⇒ 1] ≠ 1) • (IB[8 ⇒ A] ≠ 0)
EOPS = LP2M + LP5M + LP6M + STRF • (DBWM + SKFF)
TTMS = TM2M • TM5M • TM6M
T27S = THDL
I37D = THDL
I4QB = THVL
I4QB-C = THVL
DOED = + EOPS • SMOF • D3OF (BKWF + RCNF) + TSCS • D24D' + EXNF • IMIF • D24F'

	TAGD	
TITLE MAGNETIC TAPE INDEXING & FLAW CONTROL FOR READ OR SPACE		PAGE
UNIT 16303125	C-11205531	A
SYSTEM B5000		LEV

FIGURE 5-22 INDEXING & FLOW CONTROL

The level TWFD (Tape Write Forward) is developed from the control levels D24F/ and D26F/ contained in the I/O Descriptor and when true indicate a write (D24F/) Forward (D26F/) operation.

I25S/ is used to invert the input level I35D. I35D being false signifies that tape write ready level not (TWRL/) is true and the TTU is not in a write status (no write ring). If a reel of tape is to be written upon a "write ring" must be attached to the reel. The write ring, when attached, physically enables write circuity in the TTU. The write ring is a precautionary device which, when absent, prevents accidental writing on library tapes.

If the TTU is not in a WRITE-FORWARD status then I25S/ will be true. I25S/ is gated with TWFD to flag the condition by setting D20F and D22F in the error field of the result descriptor. If this condition exists, the write operation is terminated by exiting to SC = 14. The combination D20F and D22F is subsequently interpreted by the MCP as a Write-Lockout error.

If a file protect ring is in place, then I35D will be true. This condition is gated with TWFD to start the normal write operation. The term (TWFD * I35D) is the primary logic for a number of operations which start the write operation. These operations are discussed separately as follows:

1. The Sequence Counter is set to nine where a memory access of the first word to be written will be performed. Also, the Output Buffer Call Flip-flop (OBCF) is set indicating that new information is needed in the Output Buffer (OB).

$$SC = 9 = TWFD * I35D$$

OBCF set allows an information transfer from the W register to the OB. It will be seen later that this transfer is asynchronous with respect to the Sequence Counter.

2. The Forward Drive Flip-flip is set under three conditions:

    1. Binary mode with word counter $\neq$ 0 and D25F set.
    2. Alpha mode is specified WC $\neq$ 0 and D25F set.
    3. Alpha mode is specified WC = 0 and D25F reset (Group Mark Ending).

$$FWDF = WC \neq 0 + D25F/$$

If D25F is reset (Alpha) the Word Counter need not be considered since the record length to be written is determined by placement of a Group Mark in the record.

If D25F is set (Binary or Alpha), the Word Counter must be at some other value than zero (record length determined by word count). Binary mode with a Word Count field equal to zero has no significance as a tape command and is considered a No Operation condition.

3. There are two possible positions of the tape prior to a write or read command.

    1. Beginning-of-Tape (BOT) Load Point Marker.
    2. In the inter-record gap.

If the tape is positioned at the BOT, then it is necessary to inhibit the write operation for a sufficient length of time to provide at least a 6 inch gap between

the load point marker and the first record to be written. This is accomplished by triggering the Write Gap BOT multi (WGBM) whose time interval is 52 ms or approximately 6 inches. As will be seen in Sequence Count = 11 operations, WGBM will inhibit, starting the Pulse Counter and thus the write operation until it times out. Whether the tape is initially at the BOT load point or in the inter-record gap is determined by the external level I34D. I34D will be true if the tape is positioned at the BOT load point. The logic for setting WGBM is, therefore:

$$WGBM = (WC \neq 0 + D25F/) * I34D$$

Similarly, if the tape is not at the BOT load point, then I34D will be false; and I24S/, which reflects the complement state of I34D, will be true.

When true, I24S/ will trigger the Write Gap Normal Multi (WGNM) whose time interval of 4.7 ms inhibits the write operation while traversing approximately 0.58". As with the WGBM logic, I24S/ is gated with the term (WC ≠ 0 + D25F/), for binary and alpha operation, to trigger WGNM.

Write Gap Continuous Multi (WGCM) is set with the same logic as Write Gap Normal Multi except D21F being on disables the set of WGNM and sets WGCM. The delay Standard Index Multi in the tape unit found not timed out means the pinch rollers are still engaged and tape never stopped. The forward flip-flop being set produces the Forward Drive Level to the selected tape unit and keeps the forward pinch rollers engaged. In this, case, tape never stopped between records.

$$WGNM = (WC \neq 0 + D25F/) * I24S/ * D21F/$$

SEQUENCE COUNT = 9

At Sequence Count = 4, the TTU was interrogated for its ability to perform a write operation. If the TTU was not in a Write Lockout condition the Output Buffer Call Flip-flop (OBCF) was set indicating that information is needed in the I/O Control Unit to continue the write operation. In order to retrieve information from memory for subsequent output to the TTU, the Sequence Counter is advanced to 10; and the normal write operation continues.

To simplify, detailed explanation of the operations which do, or could occur during Sequence Count = 9, are divided into two sections. The first describes a normal write operation (no errors), while the second explains various coexisting error conditions.

SEQUENCE COUNT = 9 WITHOUT ERRORS

The first pulse following the entrance to Sequence Count = 9 initiates the following actions:

1. Sets the Character Counter to 0.
2. Clears the W register.
3. Counts the Word Counter -1.
4. Sets MANF (Memory Access Needed).

The Character Counter is set to zero from the logic,

$$CC/ = MANF/ * PTOS/ * D26F/$$

This is necessary since the transfer of information from memory to tape is from the most significant character to the most significant word to the least.

The term PTOS/ (not printer) is included in the logic to differentiate between the printer and all other peripheral output devices. In the case of the printer, information is transferred from the least significant position. Further logic (D26F/) limits the clearing of the Character Counter to the forward direction only. (For example, in a backward read lease significant character first the character counter would have to be positioned at Character 7.)

$$W\ [48 \rightarrow 1]/ = (MANF/ * D24F/) * MAPS$$

The W register is normally cleared at this point in anticipation of a load from memory.

$$WC\ -1 = MANF/ * WC \neq 0 * D25F$$

If the word counter is used, the word count field of the data descriptor is counted down one and will be counted down by one at each Sequence Count = 9 until it is zero.

The same pulse, which counts the word count field to zero, sets MANF allowing access to the last word.

$$MANF = AOFF/ * (WC \neq 0 + D25F/)$$

If an address overflow does not exist (AOFF/) and either an alpha write to group mark (D25F/) or a write operation using word counter (WC ≠ 0 and D25F) is indicated; the Memory Access Needed Flip-flop (MANF) is set. Setting MANF initiates a normal memory access of the word specified by the address contained in the data descriptor. Briefly, MANF starts the memory time counter (external). At Memory Time 2 (MT2), MAOF (Memory Access Obtained) is set. MAOF, together with MANF develop the strobe level MISD (Memory Information Strobe).

$$MAOF = MANF * (MT2D + MAPS/)$$

$$MISD = MANF * MAOF * MAPS * (SOOD + [SO9D * D24F/])$$

MISD, in turn, is used as enabling logic to set the information contained in the MIR (Memory Information Register) into the W register. This transfer is accomplished in parallel (all 48 bits simultaneously) and occurs at the first clock pulse following MISD. This transfer may be represented as follows:

$$W\ [48 \rightarrow 1] \leftarrow MIR = MISD$$

or

$$W\ [48 \rightarrow 1] \leftarrow R\ [48 \rightarrow 1] = MANF * MAOF * MAPS * SO9D * D24F/$$

The same pulse which effects the transfer of information from the MIR to the W register counts the Sequence Counter +1.

SEQUENCE COUNT = 9 WITH ERRORS

Three conditions are interrogated during Sequence Count = 9, prior to initiating the memory cycle previously described. They are:

Address Overflow (AOFF)
Memory Addressing Error (MAED)
Binary Write - No Operation

A tape parity error is forced if memory access required too much time in obtaining the next word to be written on tape. Characters are written on tape with a pulse count of 8 or 9. The output Buffer Call Flip-flop (OBCF) found set indicates the OBnF has no valid character for the Write Buffer. When the Pulse Counter is found equal to one at Sequence Count of 9 and OBCF set, a character is required by the WB register before a memory access was completed.

$$D20F = TAOD * PC = 1 * OBCF$$

ADDRESS OVERFLOW

There are five separate situations which can cause an Address Overflow indicating in tape operation. Of these five, only one is applicable to a magnetic tape write forward operation. It is:

$$AOFF = S10D * AMXS * D26F/ * PTOS$$

where, S10D = Sequence Count = 10

AMXS = Address Field of Descriptor is a maximum (D15F ⇒ D01F = 1)
D26F/ = Forward
PTOS/ = Not Printer

NOTE

PTOS/ is included to differentiate between printer operation and all other output devices. Address Overflow in Printer operation is detected as AMNS (Address Minimum).

When AOFF is true, further memory transfers are inhibited.

If AOFF is true at Sequence Count = 9 time, then the W register is cleared and the Sequence Counter is counted +1.

$$W\ [48 \Rightarrow 1]/ = MAPS * AOFF$$

$$SC + 1 = AOFF * (WC \neq 0 + D25F/)$$

$$D22F = AOFF * (WC \neq 0 + D25F/)$$

Further, the overflow condition is flagged by setting D22F in the error field of the Result Descriptor.

MEMORY ADDRESS ERROR (MAED)

MAED (Memory Address Error) is generated in Central Control and, when true, indicates that the memory module selected (D13F-D15F) is not available. If a memory addressing error exists, the condition is flagged in the Result Descriptor by setting D22F and the Sequence Counter Counted +1.

$$D22F = MANF * MAED * MAPS$$

BINARY WRITE - NO OPERATION

One function of the MCP is to interrogate the TTU's for their ability to perform a write operation. Ability, in this case, is defined as "Not-Busy", "Ready", and a Write-Ring installed.

Since the TTU has been checked during Sequence Count = 3 for its operational ability (Ready - Not-Busy), it is necessary only to check for the presence of the Write-Ring to complete the interrogation. If a Write-Ring is not in place the operation is terminated normally in Sequence Count = 4 by flagging the condition in the Result Descriptor and exiting to Sequence Count = 14. However, if a Write-Ring is in place, the operation is advanced normally to Sequence Count = 9. In order to terminate the write status interrogation, it is necessary to provide exit logic in Sequence Count = 9. This is accomplished by No Operation logic which, when detected, transfers control to Sequence Count = 14.

SEQUENCE COUNT = 10

During Sequence Count = 9 a memory access was performed and the word specified by the address portion of the Descriptor loaded into the W register.

In addition to counting the Word Counter down by one, certain possible error conditions were examined; namely, Address Overflow (AOFF), and Memory Address Error (MAED), or a memory access requiring too much time (D2OF set). In all cases, if an error existed, the condition was flagged in the error field of the D-register and the Sequence Counter advanced +1.

There are, then, four possible conditions which can exist upon entry to Sequence Count = 10. They are:

1. A normal memory cycle has been performed and the W register is loaded.
2. An Address Overflow (AOFF) has been detected and the memory cycle inhibited.
3. A Memory Address Error has occurred and the memory cycle inhibited.
4. Too much time required to access the next word from memory.

All four of the above possible conditions advance the Sequence Counter +1.

During Sequence Count = 10, the first character of the word in the W register will be transferred to the Output Buffer. Operations performed in this transfer are summarized as follows:

1. The address field is counted up +1.
2. MAOF is reset.
3. The first character is transferred to the Output Buffer.
4. The Character Counter is counted +1.
5. The Sequence Counter is advanced +1.
6. The Output Buffer Call Flip-flop is reset.

In addition, certain error conditions are interrogated. They are:

1. Address field of Descriptor is examined for overflow.
2. A Group Mark is inserted in the W register if a Memory Address Error has occurred while performing an alpha write with GM ending.

3. Memory Parity Error is interrogated (MPED).
4. The WBnF requiring a character from the OBnF before the OBnF was loaded with a new character. This condition couldn't happen during the first memory access.

To simplify, detailed explanation of the events occurring during Sequence Count = 10 separated into two sections - Normal and Error.

Flow charts for the preceding general comments are illustrated in Figure 5-18 while timing relationships are shown in Figure 5-23.

SEQUENCE COUNT = 10 WITHOUT ERRORS

The address field of the Data Descriptor is sampled; and if it is not yet a maximum, it is counted +1 in order to address the next word in memory. This action is restricted to a forward operation (D26F/) and occurs, if a printer operation is not involved. (Printer operations count down the address field). Additional logic (D17F/) insures that a normal count will take place, except during maintenance operations.

$$D\ [15 \rightarrow 1] + 1 = D\ [15 \rightarrow 1] \neq MAX * D26F/ * D17F/ * PTOS/$$

The Memory Access Obtained Flip-flop (MAOF) is reset. It should be noted that resetting MAOF occurs normally as a result of a memory access. The fact that MAOF is reset under Sequence Count = 10 is significant only because it does occur at Sequence Count = 10 time. This may be seen by examining the timing chart for Sequence Count = 9. MAOF does not depend on the primary logic of S10D to be reset.

The character of the "W" register which is selected by the Character Counter (W [CC]) is shifted to the Output Buffer. This character will later be shifted to the WB (Write Buffer) register. This is represented logically as,

$$OB\ [B \rightarrow 1] \leftarrow W\ [CC] = TWCD$$

TWCD (Transfer W Register Clocked) is generated at Sequence Count = 10 time. D24F/ signifies that this is a write operation while OBCF indicates that the Output Buffer is ready to receive information.

$$TWCD = S10D * D24F/ * OBCF$$

The Character Counter is advanced +1.

$$CC + 1 = D24F/ * OBCF$$

This positions the Character Counter at the next character to be transferred (Character Position 1). As with the transfer of the first character to the Output Buffer, this operation is initiated by signifying a write operation (D24F/) and OBCF (Write-Ready). The Sequence Counter is counted +1 to 11.

$$SC + 1 = D24F/ * TAOD * MS10D$$

This action occurs when a tape (TAOD) write (D24F/) command is to be executed if MS10D (Maintenance Sequence Counter) is true. MS10D will be true in a normal write operation if the Memory Cycle Switch (MCYS) is false and the Sequence Counter = 10. The logic for MS10D is as follows:

MS10D = CAG 67 * MCYS/

CAG 67 = SC1F/ * SC2F * SC4F/ * SC8F

MCYS is true during a maintenance operation.

Since a character has been transferred to the Output Buffer the OBCF is reset to indicate the OB is loaded and new information not needed.

SEQUENCE COUNT = 10 WITH ERRORS

At the time the character in the W-register is transferred to the OB, three error conditions are interrogated. They are:

Address Overflow (AOFF)
Memory Address Error (MAED)
Memory Parity Error (MPED)
Too late to transfer a character (PC = 1 * OBCF)

ADDRESS OVERFLOW (AOFF)

The initial setting of AOFF occurs during Sequence Count = 10 and is recognized at Sequence Counter = 9 of the next cycle (See Sequence Count = 9: Error Conditions). An Address Overflow is recognized by examining the Address Field of the Descriptor. If all bit positions of D15F through D01F are equal to one, the condition is recognized AMXS (Address Maximum) and AOFF is set. The logic for setting AOFF is:

AOFF = (D [15 → 1] = MAX) * D26F/ * PTOS/

D26F/ indicates this is a forward operation while PTOS/ signifies this is not a Printer operation.

MEMORY ADDRESS ERROR (MAED)

As explained under Sequence Count = 9 operation of either a Memory Address Error (Unavailable Memory Module) or an Address Overflow (AOFF) will set the error flag D22F in either alpha or binary mode.

If either condition exists, it is necessary to terminate the operation. When in binary mode the operation is normally terminated when the Word Counter = 0 with all memory cycles inhibited after the error is recognized. However, in alpha mode, the only way the operation may be ended is by recognition of a Group Mark within a word accessed from memory. Since AOFF and MAED both inhibit further memory cycles, it is impossible, in alpha mode, to access the normal insert Group Mark logic and thus end the operation. To terminate an alpha-write-forward error condition, the I/O Control Unit first recognizes that an error condition exists and then simulates an alpha end command by inserting a Group Mark in the W register for subsequent recognition at Sequence Counter = 11 (Group Mark exit). Recognition is (as explained previously) performed at Sequence Count = 9 while Group Mark insertion is performed at Sequence Counter = 10 from the logic:

W [5 ➡ 1] = D24F/ * D25F/ * D27F/ * D22F * MS10D

where,

D24F/ = Write Operation
D25F/ = Alpha Write
D27F/ = Alpha Mode
D22F/ = AOFF or MAED
MS10D = MCYS/ * S10D

MEMORY PARITY ERROR (MPED)

If, during the last memory access a Memory Parity Error was detected (MPED), D19F is set to flag the condition in the Result Descriptor. MPED will go true at MT2 time and is logically available to set D19F, clocked, at MT4 time. D19F will be set only if a Memory Access is not needed (MANF/), a Memory Access has been obtained (MAOF), and the parity error level MPED is true.

D19 = MANF/ * MAOF * MPED

Again D20F is set to flag an error if the tape unit requires a character in the WB register before one is available from OBnF. This type of error normally wouldn't occur during the first pass through SC = 9 and SC = 11.

SEQUENCE COUNT = 11

Entrance to Sequence Count = 11 can only be made from Sequence Count = 10 where one of two conditions exists upon exit.

1. The tape was initially positioned in an inter-record gap or at the BOT mark. Depending on the starting position of tape, either the Write Gap Normal or Write Gap BOT multi has been triggered. While the tape is being driven forward through the gap, the first word of the record to be written has been loaded into the W register (SC = 9) and a partial transfer of information effected (SC = 10). The OB, W, and WB are in the following configuration with subsequent operation inhibited until time out of either WGNM or WGBM.

   a. The OB contains the first character of the first word.
   b. The Character Counter is pointing to the second character of the word in the W register (CC = 1).
   c. The WB register is cleared.

2. The write operation is in process and a record is in the process of being written in either Alpha or Binary mode. More information has been requested in the previous SC = 11 to continue the write operation and, as a result, a new word has been loaded into the W register (SC = 9) and a partial transfer has taken place (SC = 10). The information registers are in the same configuration as in Condition 1, preceding, with subsequent character transfers occurring without delay upon entrance to SC = 11. During Sequence Count = 11 information from the W register is transferred to the Write Buffer (WB) via the Output Buffer (OB) for subsequent output to tape at a rate determined and controlled by a Pulse Counter (PC).

In addition to preliminary synchronization of asynchronous inter-record gap and BOT logic, SC = 11 operation initiates memory requests for new information and terminates the write operation when the end of an Alpha or Binary record is detected. Control is then transferred to SC = 8 where a read check operation is performed upon information just written.

Detailed operation during SC = 11 may be divided into three specific areas according to primary function. They are:

Phase I- Synchronization of Inter-record Gap or BOT logic with system clock.

Phase II- Develop timing and information transfer rates for I/O Control and the TTU. (Pulse Counts (PC) and Tape Clock Pulses (TCP).

Phase III- Initiate memory requests for new information.

Phase IV- Recognize and terminate the write operation.

A. Alpha
B. Binary

PHASE I

Synchronization

During Sequence Count = 4 either WGNM (Write Gap Normal) or WGBM (Write Gap Beginning of Tape) or WGCM (Write Gap Continuous) had been triggered depending upon the initial position of the tape. While any of the multi's output is true, further write operations are inhibited. After the respective multi has timed out (4.7 ms for WGNM, 5.2 ms for WGBM, 5.5 ms for WGCM) it is necessary to resynchronize additional write operations with the system clock. This is accomplished by the action of STRF (Strobe) and HOLF (Holdover).

STRF is initially set upon entrance to Sequence Count = 11 by EXNF/ and TAOD.

As soon as WGNM, WGBM or WGCM time out, the level WGMS/ (Write Gap Multi Not) will go true.

HOLF = WGMS/ * STRF * TAOD

HOLF, in turn, sets the logical flip-flop EXNF. The same pulse sets the tape speed multi (TSCM) to set up for a logical check to make sure the tape is up to proper speed during initial read-back. A flux change must be read within the next 1.5 ms or the tape is assumed to not have attained its proper speed. A parity error is forced by the setting of D2OF when the first flux change is sensed (SHOF). To complete synchronization, HOLF also resets STRF.

D2OF = DOED
DOED = TSCS * D24D/ * EOPS/
TSCS = RCNF/ * SHOF * TSCM/
EXNF = HOLF * TAOD * SC = 11

PHASE II

Timing Rates

Logical operations during Phase II of the write operation are dependent upon the primary logic of EXNF * TAOD. EXNF may be considered as the logical indication that synchronization has been effected with the system clock following the asynchronous operation of WGNM, WGBM or WGCM.

PC + 1 = PSOS/ * SC8F * D24F/ * EXNS * TAOD

The Pulse Counter (presently at zero) is counted +1. If the Sequence Counter is at 8 or above, as indicated by SC8F, and a write operation is signified (D24F/), the Pulse Counter is counted +1 with the additional term PSOS/. The term PSOS/ (Pulse Counter set to zero) does not imply that the Pulse Counter is equal to zero, but rather that the level which initially set the Counter to zero is false.

WB [B⇒1] ← OB [B⇒1] = PC = 1 * (GPMS/ + D25F) * (LPWF/ + LCHF/) * D30F

The character in the OB (loaded at Sequence Count = 10) is transferred to the WB (Write Buffer). To simplify, when the Pulse Counter is equal to one, EXNF is true; and if this is a tape operation, then any of the following conditions will generate WBID (Write Buffer Input). They are:

Alpha with GM End

GPMS/ * LPWF/ * D30F/

GPMS/ * LCHF/ * D30F/

Any Alpha or Binary Operation Using Word Count End

D25F * LPWF/ * D30F/

D25F * LCHF/ * D30F/

In other words, if this is not an Erase operation (D30F/), then the contents of the OB will be transferred to the Write Buffer if, in alpha mode, the character to be transferred is not a Group Mark and is not a longitudinal parity write or a last character. Similarly, alpha mode with word count end or in binary mode. This is not a Longitudinal Parity Write or the Last Character. All of these conditions are discussed in Phase III to follow.

Since the character in the OB has been transferred to the WB, new information is needed in the OB to continue the operation. To signify that the OB is ready to accept another character, OBCF is set from the logic;

OBCF = PC = 1 [(LPWF/ * LCHF/ * D25F) + (GPMS/ * D25F/)]

As with the generation of WBID, the set logic for the OBCF may be simplified as follows:

With the Pulse Counter equal to one, EXNF true and a tape operation, OBCF will be set when,

Alpha Write with GM End: GPMS/ * D25D/

Alpha or Binary Write
with Word Count End: LPWF/ * LCHF/ * D25F

The OBCF is set when, in alpha with group mark ending the character is not a Group Mark. OBCF is set in alpha or binary with word count ending at each PC = 1 if this is not a Longitudinal Parity Write or the last character.

With OBCF true, the second character is transferred from the W register (CC = 1) to the OB.

$$OB\ [B \rightarrow 1] \leftarrow W\ [CC] = OBCF * SC8F$$

To signify that the OB is loaded, the OBCF is reset from,

$$OBCF/ = SC8F$$

The Character Counter is counted +1 (Character 3) in anticipation of the next character transfer.

$$CC + 1 = OBCF$$

Conditions now existing in the I/O Control Unit may be summarized as follows:

1. EXNF set.
2. PC = 2.
3. First character of word in WB.
4. Second character of word in OB.
5. Character Counter set to 2 (3rd character of word).
6. OBCF reset.

The Pulse Counter will now continue to count +1 with each clock pulse from the logic previously described as,

$$PC + 1 = PSOS/ * SC8F * D24F/$$

When the Pulse Counter is equal to 8 or 9, a TCP (Tape Clock Pulse) will be generated from the logic,

$$TCP = (PC = 8 + 9)$$

This 2 us pulse is sent to the TTU through Output Driver 021D and when true, clocks the information lines from the WB to the seven Write Flip-flops in the TTU.

The formal logic for TCP is as follows. Notice that TCP will be true for a pulse count of 8 or 9 by not gating PC1F.

$$TCP = 021D = TAOD * EXNF * PA2F/ * PC3F/ * PC4F * PC5F/ * PC6F/$$

After the generation of a TCP at pulse count time of 8 and 9 the Pulse Counter continues counting +1 until one of the following conditions exists:

1. The Pulse Counter = 41 and this is a 200 BPI Operation.
2. The Pulse Counter = 14 and this is a 555 BPI Operation.
3. The Pulse Counter = 10 and this is a 800 BPI Operation.

As explained in I/O Orientation, the purpose of the Pulse Counter is to scale down the system clock to read or write magnetic tape information at the TTU designed rate of 24, 67KC or 96KC for low density, high density or very high density operation.

Consequently, when the Pulse Counter reaches the recycle point for high or low density operation, it is reset and restarted. The recycle point is determined from the logic,

PC/ = (I37D * PC = 14) + (I27S/ * PC = 41) + (I37D * I40S * PC = 10)

where,

127S/ = Low Density (I37D Switched).
137D = High Density
137D * I40S = Very High Density

When the first recycle point is reached (41 + 14 + 10), one complete character write operation has been performed; i.e.,

1. The first character has been written on tape by TCP (PC = 8 + 9).
2. The second character has been transferred from the W register to the OB.
3. The Character Counter is pointing at the next character to be transferred to the OB (Character 3, Character Count = 2).

The Pulse Counter will continue to recycle with one character being written with each TCP until one of the following conditions occurs:

1. The last character of the word (Character 8, Character Counter = 7) has been set into the OB and a new word is required from memory to continue the write operation.
2. The last character of the record has been set into the OB.

    a. In Alpha or Binary mode this is recognized by the character counter = 7 and the word counter = 0.
    b. In alpha mode with D25F/ the last character of the record is detected as a Group Mark.

Each of the two preceding conditions is explained separately in the following sections.

PHASE III

Memory Requests

When the last character of a word is set into the OB during Sequence Count = 11, the operation exits to Sequence Count = 9 to perform a memory access for new information. During Sequence Count = 9 the next word addressed by the Descriptor is accessed and placed into the W register. At the time exit is made from Sequence Count = 11 the following conditions exist:

1. Character 7 of the 1st word is in the WB.
2. Character 8 of the 1st word is in the OB.
3. The Character Counter has been set to 0.
4. The previous TCP has written Character 6 on tape.

Coincidental with the memory access of Sequence Count = 9 and 10 is the writing of character 7 of the first word. Completion of writing the first word is performed when the memory cycle has been completed and control returned to Sequence Count = 11. Character 8 of the first word is written during the second cycle of the Pulse Counter.

It is important to note that these two actions; i.e., memory access and completion of writing the first word occur concurrently. Action of the Pulse Counter is independent of the primary logic S11D where operation was initiated and only depends upon the Sequence Counter being equal to or greater than a value of 8.

PHASE IV

When the Character Counter is counted to 7 it signifies that the counter is pointing at the last character of the word (character 8) and new information is required in the W register. This condition effects a transfer of control to Sequence Count = 9 by the logic,

$$SC \leftarrow 9 = OBCF * CC = 7 (D25F/ + WC \neq 0 * D25F)$$

This logic is significant in differentiating between the last character of a word and the last character of a record.

If this is the last character of a record where word counter is used (D25F) then the write operation is to be terminated. This situation is recognized as the Word Counter = 0 and, when true, inhibits exit to Sequence Count = 9.

Similarly, in the case of a last character of a record in Alpha mode with group mark ending the OBCF will not be set, due to the recognition of a Group Mark in the last character position.

To continue, when character 8 is recognized and, further, that this is the last character of a word, control is transferred to Sequence Count = 9.

During Sequence Count = 9, a standard memory cycle is performed during which:

1. Character 8 is transferred to OB (under control of the Pulse Counter).
2. Character Counter is reset.
3. W-Register cleared prior to access.
4. Word Count reduced by 1.
5. AOFF and MAED interrogated.
6. Sequence Counter advanced +1.

Operation at Sequence Count = 10 is identical to that described in SC = 10 without errors with the exception that the character pointed to by the Character Counter is not transferred to the OB (second word - first Character) and the Character Counter is not advanced +1. This is done to prevent shifting the first character of the second word to the OB which already contains Character 8 of the first word. Inhibiting these two actions is a result of resetting the OBCF when the operation left control of Sequence Count = 11. This may be seen by examining the logic, where, TWCD = S10D * D24D/ * OBCF

$$OB [B \rightarrow 1] \leftarrow W [CC] = TWCD$$

Figure 5-23 shows the timing relationship of Sequence Counts 9, 10, and 11 when the last character of a word is recognized and a memory cycle initiated.

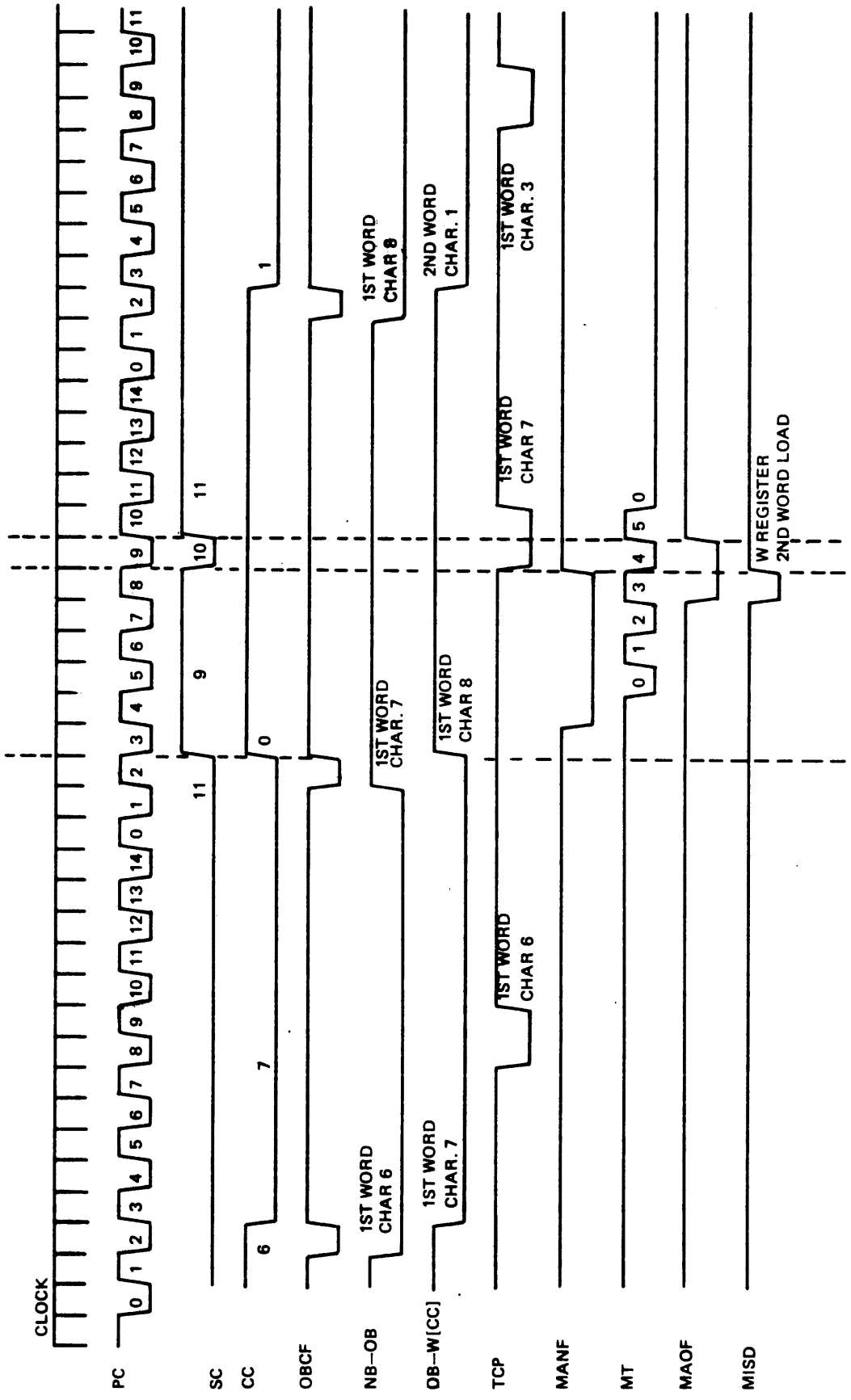


FIGURE 5-23 MAGNETIC TAPE WRITE - MEMORY ACCESS AFTER FIRST WORD

ALPHA WITH GROUP MARK TERMINATION

As described previously, during a magnetic tape write operation, eight character words are continuously accessed from memory and written on tape under control of the Pulse Counter. This procedure is continued until the last character of the word is recognized.

In Alpha mode with D25F/ all records are terminated by a Group Mark indicating that the character string is ended or that an address overflow or memory address error has occurred (Sequence Count = 10).

The Group Mark is used as an ending flag for an Alpha record since the record can consist of a series of characters whose total number may or may not equal an integral number of words.

Therefore, recognizing the end of a record by a Word Count of 8 and Character 8 is of no significance since the end of the record (last character) may appear in any character position of the last word accessed.

In terminating an Alpha record, recognition of a Group Mark initiates the following:

1. Recognition of Last Character.
2. Complete writing record.
3. Generate the Longitudinal Parity Gap.
4. Write Longitudinal Parity.

At the same time the Longitudinal Parity Character is written, control is transferred to Sequence Count = 8 (Read portion of Write Operation). Specific logic for terminating an Alpha write is shown in Figure 5-23.

In order to exemplify terminating an Alpha record a situation has been selected where a seven character record is ended with a Group Mark in the eighth position.

At the initial stage, illustrated in Figure 5-23, the following conditions exist:

1. Character 6 has been transferred to the Write Buffer.
2. The seventh character has been transferred to the Output Buffer.
3. The Character Counter has been counted to 7.

A Tape Clock Pulse is generated at PC 8 * 9 and character 6 is written on tape.

When the Pulse Counter recycles at the following PC = 1 (41 + 14 + 10) for the next character write (character 7) a normal transfer of information occurs i.e., character 7 is transferred to the WB and the eighth character (Group Mark) is shifted to the OB.

The state of the flip-flops in the OB are sampled and the Group Mark detected from the logic,

GPMS = OBBF * OBAF * OB8F * OB4F * OB2F * OB1F *

D24F/ * DROS/ * CROS/

where,

D24F' = a write operation
DROS' = not a drum operation
CROS' = not a card reading operation

Character 7 is written normally at the following PC = 8 and 9. Coincidental with writing Character 7 is the recognition that this is the last character of the record. The event is flagged by setting LCHF (Last Character Flip-flop) from the logic,

$$LCHF = PC = 9 * (GPMS * LCHF/ * D25F/)$$

Since this is the last character of the record, it is now necessary to initiate the operation of generating the Longitudinal Parity Gap and writing the Longitudinal Parity Check Character following the LP gap. The operation is started by setting LPWF (Longitudinal Parity Write Flip-flop) from,

$$LPWF = PC = 9 * D25F/ * GPMS$$

The Longitudinal Parity Gap is generated by inhibiting the write of the LP check character for a period of time equal to four and 1/2 character spaces regardless of density selected. This time interval is produced by tallying pulse counter cycles ($0 \Rightarrow 41$ at low density, $0 \Rightarrow 14$ at high density or $0 \Rightarrow 10$ at very high density) with the character counter. In low density this longitudinal parity gap is 187 us while in high density it is 67 us. Four 1/2 character spaces represents 49 us at very high density.

Briefly, the fixed time interval, representing the Longitudinal Parity Gap between the last character of the record and the LP check character, is produced as follows:

1. The Character Counter is set to 0.
2. The Pulse Counter is allowed to count at the system clock rate.
3. Each time the Pulse Counter recycles the Character Counter is counted +1.
4. Writing the Longitudinal Parity check character at a specified character and Pulse Counter time.

As stated in the flow shown in Figure 5-23, this action occurs at the same PC = 9 initially setting the Character Counter to zero from the logic,

$$CC/ = PC = 9 * (GPMS * D25F/ * \overline{LCHF})$$

In the example illustrated in Figure 5-23, this action occurs at the same PC = 9 which generates the TCP for writing the last character of the record (Character 7).

At the next PC = 1 interval, the Character Counter is counted +1 by,

$$CC + 1 = SC8F * \overline{CC4F} * PC = 1$$

Normally, at this time, the OBCF would be set to initiate another load of OB and WB. However, both actions are inhibited (because of the Group Mark) by the condition,

$$OBCF = PC = 1 * (\overline{GPMS} * D25F/)$$

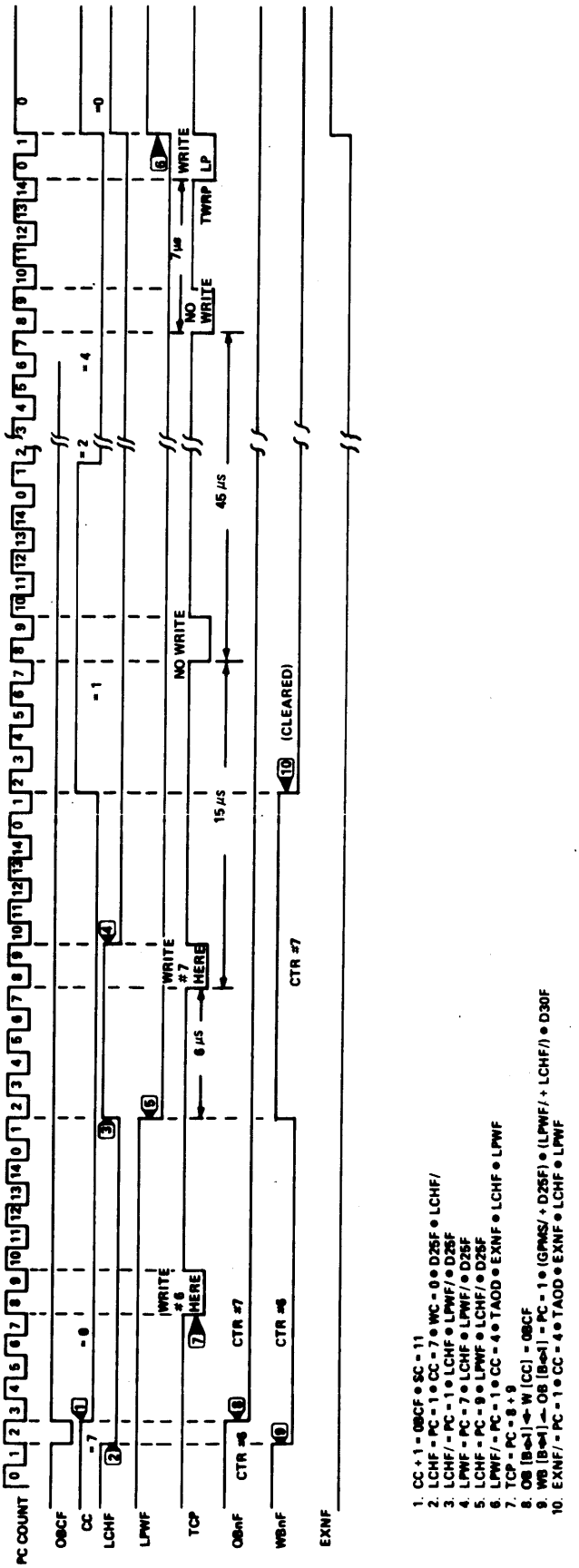


FIGURE 5-24 END OF WRITE WITH WORD COUNT

The WB is also cleared to prevent further flux changes on tape between the last character of the record and the LP character. Effectively the last character of the record is "smeared" on tape up to the LP character.

$$WB\ [P \Rightarrow 1]/ = PC = 1 * (GPMS * D25F/)$$

The Pulse Counter continues to count at the system clock rate and with each PC recycle counts the Character Counter +1.

When the Character Counter is equal to 4 and the Pulse Counter is equal to 0, 67 us will have elapsed from the writing of the last character. At this time a TWRP (Tape Write Reset Pulse) is generated from the logic,

$$TWRP = CC4F * PC = 0 + 1$$

TWRP, in turn, is sent to the write circuitry of the TTU through 027D. The occurrence of TWRP resets the "1" state flip-flops, causing a "1" bit to be written on the associated track. This action represents the Longitudinal Parity Check Character.

The formal logic for TWRP is as follows,

$$TWRP = 027D = TLPD * CC4D * PC2F/ * PC3F/ * PC4F/ * PC5F/ * PC6F/$$

where, TLPD (Tape Longitudinal Parity) = EXNF * LCHF * LPWF * TAOD.

Notice that TWRP is similar to a TCP in that a 2 us pulse is developed by not gating PC1F.

The write operation can be considered complete at this point and at the same PC = 1 which is generating TWRP a reset action is developed as follows,

$$LPWF/ = CC = 4 * PC = 1$$

Control is also transferred to Sequence Count = 8 where a read operation will be performed of the information just written on the tape (Post-Write Read Operation) control transfer is a result of the logic,

$$SC \Leftarrow 8 = CC = 4 * D30F * PC = 1$$

where, D30F indicates this is not an erase operation; ie., data to be transferred.

WORD COUNTER TERMINATION

Terminating a magnetic tape write operation with word counter, is similar to ending an Alpha write with group mark in that the method of generating the Longitudinal Parity Gap and writing the Longitudinal Parity Check Character is identical. However, in Alpha mode, with group mark ending, writing the last character (Group Mark) is inhibited while in Binary mode the last character must be included as part of the record.

Recognition of character 8 or a word normally initiates a memory cycle to fetch the next addressed word. However, when it is recognized that the last character of a word is coincident with the Word Count being equal to zero then the situation is detected as an end of record. An Alpha or binary record terminated when word counter is zero as follows:

1. Recognition of the Last Character.
2. Complete writing record.
3. Generate the Longitudinal Parity Gap.
4. Write the Longitudinal Parity Check Character.

At the time the Longitudinal Parity Check Character is written, control is transferred to Sequence Count = 8. (Read portion of a Write Operation).

Specific logic for terminating a write with word counter equal to zero, is shown in Figure 5-19.

An example has been chosen where the write operation is to end after reading a two word record.

As illustrated in Figure 5-23 the following conditions exist prior to the transfer of the eight character of the second word to the OB.

1. Character 6 has been shifted to the Write Buffer.
2. Character 7 has been transferred from the W register to the OB.
3. The Character Counter has been counted to 7.
4. The word Counter has been counted to zero (Sequence Count = 9).

Continuing, a TCP is generated at PC = 8 and 9 and character 6 written on the tape.

When the Pulse Counter recycles for the next character write (Character 7), a normal transfer of information occurs; i.e., Character 7 is transferred to the WB and the eighth character (last character) is shifted to the OB at PC = 1.

At this same PC = 1 the LCHF is set from the logic,

$$LCHF = PC = 1 * CC = 7 * WC = 0 * D25F * \overline{LCHF}$$

Logically, setting LCHF at this time is significant in that it indicates that this is the next to the last character of the record. When LCHF is set, character 8 is in the OB and character 7 in the WB. Actually, another transfer cycle is necessary to transfer cycle is necessary to transfer character 8 to the WB. This was also true in the case of the Alpha ending previously described. However, in an Alpha ending, when LCHF is set it does indicate that the last character of the record is in the WB, since the Group Mark is now written on tape.

Character 7 is written normally at the following PC = 8 and 9.

When the Pulse Counter recycles, LCHF will be reset and LPWF will be set if LCHF had been set at the previous PC = 1.

$$LCHF/ = PC = 1 * LCHF\ 8\ \overline{LPWF} * D25F$$

These actions occur as the last character (character 8) is transferred from the OB to the WB.

Character 8 is written at the following PC = 8 and 9. At the same PC = 9 which generated the TCP to write character 8, the LCHF is again set to indicate the last character has been written. The character counter is set to zero with the same pulse

and signifies the beginning of generating the Longitudinal Parity Gap.

$$LCHF = PC = 9 * (LPWF * \overline{LCHF} * D25F)$$

The Write Buffer (WB) is cleared at the following PC = 1 (prior to next TCP) in order for subsequent TCP's to write zeros on tape during the Longitudinal Parity Gap.

$$WB\ [P \Rightarrow 1/] = PC = 1 * (LPWF * LCHF)$$

Further operation in generating the LP gap and writing the LP Check Character is identical to that described for an Alpha ending.

Briefly, the Pulse Counter continues to generate TCP's at each PC = 8 and 9. At each recycle point, the Character Counter is counted +1. When the Character Counter is equal to 4 and the Pulse Counter equal to zero, a 2 us pulse is developed, named TWRP, which writes the Longitudinal Parity Character.

Only those write flip-flops found set and are reset with TWRP produce a flux change on tape to form the Longitudinal Parity Character.

When the LP Check Character is written, the operation is terminated and control transferred to Sequence Count = 8 where a read operation is performed upon the previously written information. This read operation is not completed until 1.25 ms later because of the displacement between the read and write head.

POST-WRITE READ OPERATION (See Figure 5-19)

During any write operation, a simultaneous read check of previously written material is in progress. The purpose of this read-check operation is to sample successive characters and interrogated for proper lateral parity (Alpha-even; Binary-odd).

At the end of the record, Longitudinal Parity is checked and the post-write read operation terminated by exiting to the indexing control cycle which, in turn, stops the tape read.

The read head of the dual gap head is physically separated from the write head by a distance of 0.15". Therefore, a time delay of 1.25 ms exists between the writing of a character and a post-write read operation of the same character, At 120IPS. (1.67 ms at 90)

Read logic is activated for this checking procedure by the level TRL (Tape Read Level), which is enabled during any write operation as soon as the prerecord gap (inter-record or BOT) has ended. Read operation is identical to the normal read operation discussed in the next section with the exception that characters are not transferred to the W register for subsequent storage in memory.

This post-write read provides a means of checking the character parity and Longitudinal Parity of information just written on tape without initiating a separate read instruction. No information on read-back is placed into the W register.

The post-write read operation can be divided into 5 specific actions. They are:

1. TRL (Tape Read Level). Read character from tape into IR. Check skew characteristics and synchronize character with the system clock.

2. SHOF (Skew Holdover). Transfer character from IR to IB. Generate Longitudinal Parity and check repetition rate of character input.
3. PUCF (Pile-Up Control). Check lateral parity and initiate indexing control logic.

4. IMFF (Information Flip-Flop). Begin indexing control cycle or recycle for next character.
5. IMIF (Information Index). Index and terminate operation.

To demonstrate the general operation of the post-write read operation an example has been selected where an eight character alpha record has been written and control transferred to SC = 8. As illustrated in the timing charts, the example includes reading parity, indexing, end-of-operation detection, and writing the longitudinal parity check character.

Tape Read Logic is considered true upon entry to the example from the logic,

026D = TRL = TAOD * RIMS/ * WGMS/ * (LP2M + LP5M + LP8M + FWDF + BKWF)

which, in essence, indicates that neither WGNM, WGBM nor WGCM is true. Also, the term RIMS' indicates that the Backward Read Inhibit (BRIM) and the Load Point Read Inhibit (LPIM) multi's are false.

Tape Read Pulses (TRP's) will be set into their respective IR Buffer Flip-flops, unclocked, during the interval determined by the Digit Skew Multi (DSWM). When the character has been completely read, as determined by the skew multi timing out, synchronization with the system clock is accomplished by setting SHOF and transferring control to the Skew Holdover logical cycle (SHOF).

SHOF (Skew Holdover): During the SHOF logic cycle (1.0 us), the following operations occur as part of a normal read operation.

1. A dropout is detected if this is not the first character and all Lost Digit Multies are found timed out.
2. Skew and synchronization logic are reset in anticipation of the next character.
3. The character in the IR Buffer is transferred to the IB and the IR Buffer cleared for the receipt of the next character.
4. Longitudinal Parity is generated by complementing the LP register flip-flops whose corresponding IR Flip-flop is set.
5. The Information Index Multi (IM2M, IM5M or IM8M) is triggered for character repetition checking.
6. The Record Control Flip-flop (RCNF) is set at the first character signifying that the body of a record is being read.
7. Control is transferred to PUCF (Pile-Up Control).

Logic not included as part of a normal read cycle but necessary in a post-write read operation is validating the record at SHOF time by setting VRCF. Normally, record validation occurs during PUCF logic under control of the Character Counter and D24D (Read) and enables indexing logic (IMIF).

However, in a post-write read operation the W register is not used to tally input characters and, consequently, is not under Character Counter Control (concurrent write operation is in process). Further, D24D is not true. Therefore, record validation, and thus entrance to indexing logic, is simulated by setting VRCF.

The first character detected causes SHOF (Skew Holdover flip-flop) to be set and the respective Lost Digit Multi is initially set. Anyone of the Lost Digit Multi times out in one and 1/2 character frames regardless of density selected. EOPS/ (End of Operation Pulse) being true indicates that the Longitudinal Parity has not been detected because none of the Information Multi's are set.

$$LDSF = SHOF * \overline{EOPS}$$

DOED becomes true when a one character dropout has been selected in a record. IMFF, VRCF and LD5F are both set with the first character read. One of the Lost Digit Multi's is set to keep DOED false. The selected Lost Digit multi is prevented from timing out with each character read if no characters are read for one and 1/2 character frames (21 us at high density), then LD5M times out and DOED becomes true. However, this dropout would not be detected unless another character was read (SHOF set) before the information multi timed out. No flux changes for two and 1/2 character frames in succession indicates a Longitudinal Parity Gap has been detected.

$$DOED = IMFF * SHOF * LD2M/ * LD5M/ * LD8M/ * (BKWF/ + CC \neq 7 + VRCF)$$

DOED also becomes true if TSCM (Tape Speed Check Multi) times out before the first character is read (SHOF set) by the read head.

$$DOED = TSCS * D24D * EOPS/$$

$$TSCS = RCNF/ * SHOF * TSCM/$$

TSCM (Tape Speed Check Multi) is initially set at the beginning of an active write and times out 1.5 ms later. If the tape is moving at 120 inches/ second the first character of a record is read 1.25 ms after it was written. SHOF is therefore normally set about 250 us before TSCM times out. When TSCM times out before RCNF is set to indicate the beginning of a record, the tape is detected as not being up to proper speed when the beginning of the record was written. This means the packing density has been increased and individual characters could not be read reliably in a read operation.

PUCF (Pile-Up Control). The primary purpose of PUCF logic during a post-write read operation is to flag a vertical Parity Error (PELS) by setting D20F in the error field of the Result Descriptor. This action occurs from the logic,

$$D20F = PELS * \overline{D30F} * \overline{EOPS}$$

where, D30F/ indicates that this is not a maintenance operation and EOPS/ signifies this is not the end of the read operation.

IMFF (Information Flip-flop) is set during PUCF time and logically indicates that one of the Information Index multi's (IM2M + IM5M + IM8M) has been triggered. IMFF is shown under PUCF logic because it is set when PUCF is set for the first time. However, though indicated on the flow, PUCF is not primary logic for setting IMFF, which, when set, remains true during the reading of the rest of the record.

IMFF (Information Flip-flop). When IMFF is set it indicates that a record is being read. Once set, it is necessary to recognize when the record is complete, which is detected as the time-out of (IM2M + IM5M + IM8M).

When all of the Information Index Multi's are found timed out, the indexing cycle is initiated by setting IMIF (Information Index Flip-flop) from the logic,

$$IMIF = \overline{IIMS} * \overline{SKFF} * \overline{D26F}$$

where, IIMS/ = IM2M/ * IM5M/ * IM8M/ and SKFF' indicates that a following character has not set a skew logic cycle. Simply, control of a read operation is transferred to an indexing cycle when character separation is greater than the time interval of the respective Information Index Multi; i.e.,

IMIF set

BFMS/ (Backward Flow Multi Switched) output is true during any forward tape operation. VRCF (Valid Record) and RCNF (Record Control Flip-flop) are both on at this time if at least one character has been read. The clock pulse that finds IMIF set resets RCNF, VRCF and FWDF. EXNF was reset as the LP character was written. Therefore EXNF has been reset for 1.25 us at 120 in/sec. before the LP character is read. The insertion of a Group Mark and the setting of PUCF at this time is redundant.

$$FWDF/ = RCNF * FWDF * VRCF * EXNF/ * IMIF$$

A Longitudinal Parity Multi is set corresponding to the Bit Density selected by the operator. Any one of the three Longitudinal Parity multies being set causes EOPS (End of Operation Pulse) to be true:

$$LPnM = nBID * IMIF$$
$$EOPS = LP2M + LP5M + LP8M$$

A DOED (Drop-Out) is detected at this time if a write operation is still in progress (EXNF set) and no flux changes detected for two and 1/2 character frames (IIMS/ true) after at least one character was read to set an information multi.

$$DOED = IMIF * D24F/ * EXNF$$

However, a one character drop-out is not detected unless another character is read (SHOF set) before the information multi times out and causes Valid Record and Information Flip-flops to be reset. The detection of a one character drop-out is inhibited during an erase rewind or maintenance operations spacing

$$DOES = IMFF * SHOFF * LD2M/ * LD5M/ * LD8M/ * VRCF$$

$$DOED = DOES * D30F/$$

A two character drop-out allows the information multi to time out and reset VRCF and RCNF. A longitudinal parity multi would be set and cause EOPS to be true.

With any Longitudinal Parity Multi set, the logics expects to read one LP character and set SHOF. The next clock pulse sets RCNF and resets SHOF. If a second character was read during the LP gap, SHOF would be set again and find RCNF set. This logic says two or more LP characters have been read and this is an error, which causes D20F to be set. D30F/ indicates this is not an erase operation.

$$DOED = EOPS * SHOF * D30F/ * RCNF$$

SC = 8

STRF is normally set with the next clock pulse that finds a Longitudinal Parity Multi set (EOPS true). After the Longitudinal Parity Multi times out EOPS/ becomes true and sets HOLF. STRF and HOLF both set the sequence counter to 14. The W-register is cleared in preparation for doing a D-register to W-register transfer at SC = 14.

MAGNETIC TAPE REWIND (See Figure 5-17)

The common logics for all tape operations is performed at Sequence Count equal to three.

Sequence Count = 4

D21F is used as a logical flip-flop at SC = 3 and CC = 6 to check for Delay Standard Index Multi (DSI) in the tape unit being on.

If DSI is found on at SC = 3 and CC = 6, the logics holds until DSI times out and then proceeds to SC = 3 and CC = 5. At SC = 4, D21F is unconditionally reset.

STRF the Strobe Flip-flop (STRF) is set when all tape movement has stopped (TREL true). A rewind level is produced and sent to the tape unit when STRF is set. However, exit of this flow is not attained until after the tape unit has begun to execute the rewind (I22S/ true).

BASIC READ OPERATION (See Figure 5-20)

Magnetic tape may be read forward or backward. When reading in the forward direction, the low order destination address in the descriptor is specified. Words are read into the most significant position first; subsequent characters are read into successively lower character positions.

Eight consecutive characters are accumulated in the W register and then sent to Core Memory. This continues until an inter-record gap is encountered. If the Word Counter feature is utilized D25 set in descriptor memory accesses are terminated after the designated number of words has been read, provided that the inter-record gap has not been encountered. The I/O remains connected to the tape unit until the inter-record gap is encountered.

A group mark (01 1111 - BCL code) is inserted as the last character after the inter-record gap is encountered during alphanumeric forward read only. No group mark is inserted in binary read; or if the word counter feature terminates memory accesses during alphanumeric read. If a binary record or an alphanumeric record read forward does not constitute an integral number of words, the remaining character spaces of the last word are filled with the character (00 0000 internal code). The contents of the character counter is placed into the result descriptor bits D31, 32 and 33.

If an alphanumeric record read backward does not constitute an integral number of words, the remaining character spaces of the last word are filled with the question mark character (00 1100 internal code).

When reading in the backward direction, the high order destination address is specified in the descriptor. Words are read into successively lower memory addresses.

Characters within a word are read into the least significant position first; subsequent characters are read into successively higher character positions.

A particular tape record will occupy identical memory spaces (word for word, character for character) whether read forward or backward only if the record is an integral number of words. For other records, there is a maximum displacement of seven characters when identical memory areas are specified.

To permit uniformity of Alpha records appearing on magnetic tape, provision is made during the write operation to pass the question mark character (00 1100 internal code) through the I/O without recording a character on magnetic tape. This function permits an alphanumeric record to be read backwards and then rewritten exactly as it appeared on tape provided the question marks appear at the beginning of the record.

Forward space and Backward space are variants of Magnetic Tape Read. See Figure 5-20.

If a Magnetic Tape Read extends beyond the highest memory address, the condition is signalled in the result descriptor (memory address error, D22) and information beyond this address is not written in memory.

If the designated Magnetic Tape Unit is in the process of stopping (TREL/ true and TS1L/true), the I/O Control Units wait until it has stopped, then proceeds immediately with the specified operation. A "unit busy" flag (D16) is not set unless the unit is still busy, after the I/O Control Unit has waited long enough to permit declaration. (BTDM timed out). If DSI in the tape unit has not timed out at SC = 3 * CC = 6 then the logic waits until DSI does times out (I39/ true).

The logics then proceeds CC = 5 and then to SC = 4. Here the FWDF is set and tape does not stop between records. No provision is made to perform a backward read operation that attempts to read backward beyond the first record on tape. If such an operation is attempted, the tape stops after the beginning of tape signal occurs; but the Input/Output Control Unit remains connected to the tape unit and no result descriptor is returned until the blank tape multi times out.

It is expected that a backward read, beyond recorded data will be prevented by program. (This may be accomplished by the use of an end-of-file mark ($\geq$) recorded on tape immediately following the tape label).

SEQUENCE COUNT = 3 and CC = 5 FORWARD READ

A forward or backward read is identical at Sequence Count = 3.

Space Forward or Backward	AOFF = D24F * D25F * WC = 0 D30F/Inhibit D17 and D [15 ➡ 1]
Mark Inter Record Gap (FWD Only)	EXNF = D30F * D24F * D25F * WC = 0 * D27F/ * D26F/ D175F = D30F * D24F * D26F * WC = 0 D [15➡1] ⬅ 0
Mark Start Time To Record (Forward Only)	D17F = D30F * D24F * D26F * WC = 0 D27F (Inhibit EXNF) D [15➡1] ⬅ 0

SEQUENCE COUNT = 3 and CC = 5 FORWARD READ

The Holdover Flip-flop (HOLF) is set at a Character Count of 5 in all tape operations except a rewind. HOLF has one logical usage at this time and that is to set the Blank Tape Multi (BLTM) at SC = 4.

If the descriptor in the D-register specifies a forward or backward space, the Address Overflow Flip-flop (AOFF) and D30F are both set. D30F being set prevents the detection of a one character drop-out in a record or more than one LP character while the longitudinal parity multi is set. D30F also prevents any character parity errors from being detected when PUCF is set or longitudinal parity errors at SC = 8. AOFF being set inhibits memory cycles at SC = 9 by preventing the set of MANF.

A tape space is a normal read forward or backward but no information is transferred into memory and all parity errors are inhibited. Tape movement stops when an inter-record gap is detected. Maintenance functions are omitted here because they are covered in a separate section.

SEQUENCE COUNT = 4 and CC = 0 FORWARD READ

HOLF being on allows the Blank Tape Multi to be set. The purpose of BLTM is to prevent tape run-away in case the tape is blank or some malfunction prevents read-back. The Longitudinal Parity Flip-flop are all reset and the Information Register is cleared in preparation for the first character to be read from tape. Any forward read operation (D24F * D26F/) causes the Forward Flip-flop to be set. FWDL (Forward Drive Level) is now true and energizes the forward pinch rollers. The tape being at its load point (I340 true) causes the Load Point Inhibit Multi (LPIM) to be set to prevent reading of information for the first 15 ms of tape movement. No information is written on tape for the first 52 ms when initiating a tape write descriptor and the tape is initially found at its load point. The Forward Flip-flop being on causes TRL to be true after LPIM times out. Read Inhibit Multi Switched (RIMS/) is false if LPIM or BRIM is set.

$$026D = TRL = TAOD * RIMS/ * WGMS/ * (FWDF)$$
$$RIMS = BRIM/ * LPIM/$$

SEQUENCE COUNT = 4 and CC = 0 BACKWARD READ

Only when a backward read follows a write operation is the tape advanced forward before going backwards. The reason for moving the tape forward first is to allow the tape more time to attain 120"/sec. before reading the LP character in the backward direction. Also, moving the tape forward allows the tape to be erased and a long inter-record gap is constructed to prevent indexing problems.

The tape unit read-write head does not stop in the center of the inter-record gap at any time. At the end of a forward operation, the read-write head stops near the end of the record just read or written. If a backward read was initiated just after a write operation then the LP character is positioned very close to the read-write head. Four milliseconds maximum is required for the tape to attain 120"/second speed. The I/O descriptor in the D-register specifies a backward read with D24F and D26F on. With no tape drive conflict detected (TDCS/true), the Backward Flip-flop (BKWF) is set, the character counter is set to seven and the Sequence Counter is set to 8. The Backward Drive Level follows BKWF and causes the backward pinch rollers to become energized. Tape now moves in the backward direction.

Tape Drive Conflict (TDCS) is true when the tape unit is found in a write status (I36D true) and a backward tape read is being executed at SC = 4.

TDCS = TAOD * D26F * I36D * D24D * SC = 4

TDCS causes Write Gap Normal Multi (WGNM) to be set. The Forward Flip-flop being set causes the tape unit to move forward until WGNM times out. The Sequence Counter advances plus one.

SEQUENCE COUNT = 5 BACKWARD READ

Backward Read Inhibit Multi (BRIM) is set to prevent reading of any information while tape is being advanced forward for 4.7 ms. WGMN being on at SC = 5 causes STRF to be set and the logics waits for 4.7 ms before WGNM times out. WGMS/ goes true after WGNM times out and allows HOLF to be set. STRF and FWDF are now reset and the Sequence Counter is advanced plus one.

SEQUENCE COUNT = 6 BACKWARD READ

Again the Backward Read Inhibit Multi is held in the set state and not allowed to time out until 6.6 ms after leaving Sequence Count of 6. STRF is set immediately upon entranc to SC = 6 because MRD is found timing out in the tape unit and causes I22S to be true. MRD times out in approximately 6 ms after FWDF is reset at SC = 5. I32D becomes true (TREL/false) when MRD times out. Tape has now stopped completely and is ready to be move backward. HOLF is set and allows BKWF to also be set as the Sequence Counter is set to 8 The backward pinch rollers are energized and tape now moves in the backward direction.

SEQUENCE COUNT = 8 FORWARD READ

In Figure 5-20, STRF cannot be set until the Blank tape Multi times out (BLTS/) in 500 ms

STRF = BLTS/ * IMFF/* BFMS/

This means that HOLF cannot be set to allow an exit to SC = 14 until STRF is first set.

HOLF = STRF * EOPS/

The logics to normally set STRF is found in Figure 5-21 at EOPS time.

STRF = TAOD * EXNF/ * EOPS

TRL (Tape Read Level) Figure 5-21

The purpose of the TRL logic is to read and store Tape Read Pulses from the TTU into the IRNF (Tape Input Read) Buffer. Reference Figure .

These pulses, which enter the I/O Control Unit through input drivers I11P-I17P, are gated unclocked into the IRnF's and then synchronized with the I/O (system) clock for subsequent transfer to the W register. Refer to Figure 5-15.

Synchronization of the Read pulses is necessary because of the asynchronous nature of the TTU and the inherent skew properties of the character being read.

Skew is defined as the longitudinal separation in distance (therefore time) between

bits of a character and is due to electromechanical inaccuracies existing in the TTU read-write head.

To insure that all bits of a character will be read, it is necessary to assign an interval of time to the read process which will bracket the maximum allowable longitudinal displacement in time. At the end of this interval all the bits of the character will be available and then can be gated with respect to time (synchronized). Also, such a circuit will detect excessive skew in the form of a parity error, since one or more bits may fall outside of the normal read interval and be lost to the parity checking circuit.

Examination of the specifications for skew show that a maximum of 200 u inches skew displacement is allowable in the high-density format. At a velocity of 120"/second this is a time interval of 1.6 us. However, the read interval (skew) for the I/O Control Unit (high-density) is 6.0 us a figure which has been assigned to the read interval to achieve compatibility with the quality of other than Burroughs tape format and TTU's. It should be remembered that the figure of 200 u inches is a design specification for the TTU read-write head and is only a measure of quality of the transport itself.

The Tape Read Level is sent to the TTU through 026D and, when true, activates the TTU's Read circuitry. The TTU transmits information read pulses under control of TRL and can be considered the primary control of the TTU read cycle. TRL will be true under the following conditions:

026D = TRL = TAOD * RIMS/ * WGMS/ * (LP2M + LP5M + LP8M + FWDF + BKWF).

The term RIMS' (Read Inhibit Multi-Not) will be true when both the Backward Read Inhibit (BRIM) and the Load Point Read Inhibit (LPIM) multi's are off. The logic for RIMS' is as follows:

RIMS/ = BRIM + LPIM.

Being a switched term the actual "to happen" form of the expression becomes:

RIMS/ = BRIM/ * LPIM/

and is significant when the tape is at the BOT (TLPL). If the tape is at the BOT marker, then LPIM will be triggered and TRL inhibited for 15 ms. Similarly, TRL will be inhibited if BRIM/ is false indicating the TTU is performing a turnaround which results from initiating a Backward Read with TTU in the Write Status.

BRIM = TAOD * (WGNM * D24D * D26F + S05D + S06D)

The term WGMS/ (Write Gap Multi-Not) will be true when the Write Gap Normal (WGNM), the Write Gap BOT (WGBM) and the Write Gap Continuous (WGCM) multi's are reset. WGMS/ is, essentially, inhibiting the read function if the tape is traversing either the gap following the BOT marker or the inter-record gap.

Detailed Operation - IR Buffer Input. As the tape is moved past the read head in the TTU, all heads are read simultaneously. Flux changes, sensed by the read heads, are amplified and shaped in single channel stages and then sent to the read buss drivers which, in turn, develop a negative going pulse for each flux change.

This pulse is delivered to a compressor circuit (I/O Exchange) which reshapes an input pulse of approximately 2.0 us duration to an output pulse with a width of 0.5 us. This pulse, in turn, sets (unclocked) the corresponding IR Buffer Flip-flop in the I/O Control Unit.

Interconnecting information lines and compressor action are shown in Figure 5-15 . Specific logic for this action is shown as Information Read in Figure 5-21.

The first TRP output to go true (InnP) will trigger DSWM (Digit Skew Write Multi). If high density is selected when DSWM becomes true the Digit Skew High Density Multi and SKFF are set.

```
DSWM = TAOD * DSIS/ * SKFF/ * InnP
DS5M = DSWM * 5 BID * SKFF/
```

Initially DSIS/ is true to indicate that the Digit Skew multies are all timed out and ready to accept an input character. SKFF (Skew Flip-flop) is also found reset initially to specify that the IB register contains no valid information. The first clock pulse, following DSWM going true, sets SKFF. SKFF now serves as a storage element and indicates that one of the Digit Skew Multies has been triggered. SKFF also specifies at least one bit has entered the IR Buffer. DS5M times out 6.0 us after the first flux change was read and allows DSIS/ to become true. The Skew Holdover Flip-flop (SHOF) is set with the next clock pulse to set up logics to transfer this character from the IR to IB register.

```
DSIS/ = DSWM/ * DS2M/ * DS5M/ * DS8M/
SHOF = SKFF * DSIS/
```

SHOF (Skew Holdover Flip-flop) Figure 5-21

SHOF now is reflecting that the Digit Skew multi has timed out --further, that a complete character is contained in the IR Buffer (assuming normal skew characteristics) and that one character read has been completed. The timing relation between the Digit Skew Multi, SKFF and SHOF are illustrated in Figure 5-25.

During the time interval that SHOF is true (1.0 us), it initiates a secondary read phase to the process of reading a character into the W register. During this logical interval the following operations are performed:

A. The character in IR is shifted to IB.
B. The IR Buffer is cleared for receipt of a new character.
C. Input skew logic and synchronization logic is reset.
D. Longitudinal parity is generated.
E. The information multi's are triggered to provide a time delay until the next character.
F. RCNF (Record Control Flip-flop) is set signifying that the body of a record is being read.
G. PUCF (Pile-Up Control) is set indicating that the IB Buffer contains a character which is to be shifted into the W register.
H. LDSF (Lost Digit Flip-flop) is set to trigger a Lost Digit multi.

The formal logic for the above events is shown in Figure 5-21.

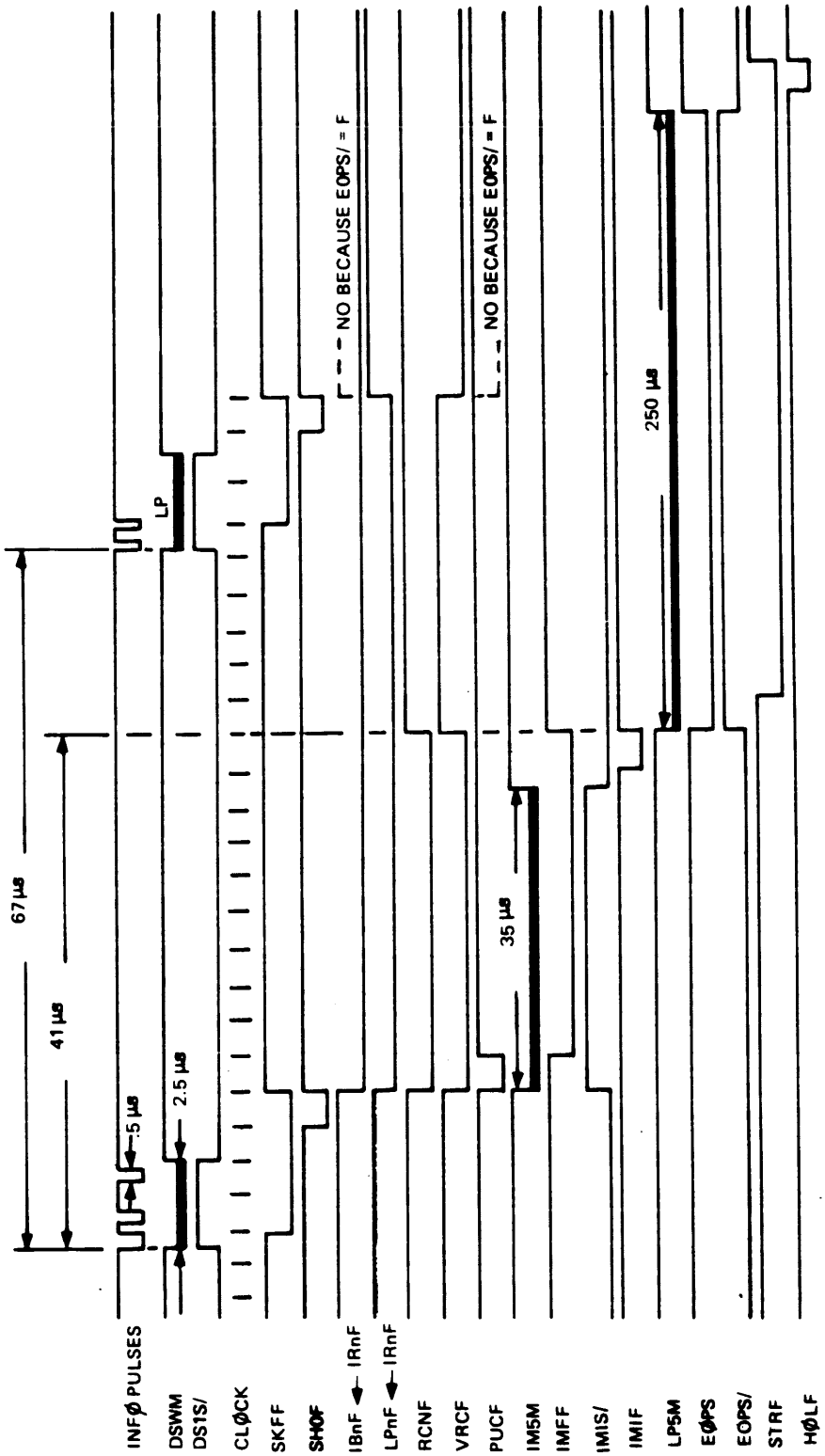


FIGURE 5-25 READ BACK AFTER WRITE OF ONE CHARACTER

The first pulse following the set of the Skew Holdover Flip-flop (SHOF) initiates all of the following operations:

1. Input synchronization circuitry is reset in anticipation of the next character. This includes resetting the IR Buffer. This action occurs ungated upon entry to the SHOF logic cycle.

   SKFF = SHOF

2. The contents of the IR Buffer are shifted to the Input Buffer (IB) from the levels:

   IBnF = IRnF * EOPS

   IBnF = $\overline{\text{IRnF}}$ * $\overline{\text{EOPS}}$

3. Longitudinal Parity (LP) is generated.

   LPnF LPnF = IRnF

4. The Record Control Flip-flop (RCNF) is set, indicating that the body of a record is being read.

   RCNF = FWDF

5. Either IM2M (Information Index Multi) IM5M or IM8M will be set depending upon whether low, high or very high density format is being read and has been selected.

The purpose of Information Multi's is to provide logical notice to the Information Flip-flop (IMFF) that a sequence of normally spaced characters are being accrued in the W register, i.e., that a record is being read. This is accomplished by indirect detection of <u>other</u> than normal intervals of character displacement -- that is, packing density. Normal intervals, in this case, are defined as the times between characters. These intervals at 120"/second capstan speed are:

Low Density	=	42 us
High Density	=	15 us
Very High Density	=	11 us

Initially, one of the three information multi's is set with the recognition of the first character in the record (first SHOS). IM5M is designed to time out in 35 us, but will restart its timing interval with each input trigger (character).

Now, if the tape is moving at normal velocity such that characters are being read at 67KC (High Density), then IM5M will be retriggered to time with each character. This is evident since the time-out interval of IM5M is greater (35 us) than the interval between successive characters in high density (15 us).

Consequently, IM5M will never time out while normally spaced input characters are generating SHOS.

6. The Pile-Up Control Flip-flop (PUCF) will be set, indicating that the information in IB can be transferred to the W register provided the

end of the record has not been detected (IMnM set).

$$PUCF = \overline{EOPS}$$

7. The Lost Digit Flip-flop is set to trigger one of the Lost Digit Multi's. However, no drop-out could be detected on the first character read.

PUCF (Pile-Up Control) FORWARD READ

In Figure 5-21 Pile-Up Control logic is enabled by SHOF * $\overline{EOPS}$ and indicates that the IB contains a character which is to be shifted to the W register.

During the time interval that PUCF is true (1.0 us), it initiates phase three of the process of reading a character into the W register. During this period, the following operations are performed if the Sequence Counter is at 8 or 10:

A. IB is transferred to the W register.
B. The Character Counter is counted + 1.
C. A lateral parity test is performed (PELS checked).
D. The Information Flip-flop (IMFF) is set indicating that information has been encountered.
E. PUCF will be reset, signifying that the character in IB has been transferred to the W register.
F. If seven characters have already been read, VRCF (Valid Record Flip-flop) is set.
G. The Sequence Counter is counted +1 if the Counter is equal to seven - indicating the eighth character has just been placed into the W-register.

The formal logic for the above events is shown in Figure 5-21.

The first pulse following the set of the Pile-Up Control Flip-flop (PUCF) initiates all of the following operations:

1. The contents of the IB are transferred to that character position in the W register indicated by the Character Counter (CC).

$$W(CC) \leftarrow IB(B\ 1) = MAPS * D27F/ + EOPS/$$

All information appearing in the Input Buffer is first directed through the input converter (Alpha decode) and then to the W register character routing matrix.

The expression, MAPS * D27F/ + EOPS/, actually indicates generation of the shift level IWSS/ in alpha (D27F/) and binary (EOPS). Both terms are used to generate the term C + 1D (CC + 1), which in turn enables the primary inputs to IWSS/ composed of D24D (Read), SC8F (Sequence Count 8) and MAPS (Memory Access Permit). The logic on the flow merely signifies the two modes of operation.

The symbolic representation of the generation of IWSS/ is shown in the Figure .

2. The character counter is counted +1. This, also, may be seen by examining Figure . In generating IWSS/, C + 1D is enabled as the shunt level for IWSS/. This action is indicated by the following representative logic:

$$CC + 1 = TAOD * D26F/ * (D27F/ + EOPS/)$$

As we will see later the expression (D27F/ + EOPS/) will inhibit group mark insertion at the end of a binary read operation (D27F/ and EOPS/ false).

3. Lateral (character) parity is checked.

   D20F = (SC = 8 + 10) * PELS * D30F/ * EOPS/ + SHOF

   D20F will be set in the error field of the D-register if an error exists (PELS). The term D30F/ indicates that this is not a maintenance cycle, space or erase and that a normal data transfer is to be allowed while EOPS/ signifies that this is not the end of the operation. If this were the end of an operation, then the next character to be checked would be the longitudinal check character which could be either odd or even laterally. The result would be an erroneous detection of lateral parity in normal operation.

Characters are read at 11 us intervals at very high density. When the W-register is filled with the eighth character a memory access is requested by I/O. Due to Central Control priority logics this access may not be granted immediately. Eleven microseconds later the next character can be read from tape and placed in IB register. PUCF would be set and SHOF reset to remember a character is in IB but cannot be transferred to W-register until the memory access has been granted and the sequence counter returned to Sequence Count of 10 or 8. Again, 11 us later another character is read from tape and placed in IR register unclocked. SHOF is again set and the new character in IR is placed in the IB register. IB contained the prior character. An error has occurred and D20F is unconditionally set with the next clock pulse that finds PUCF and SHOF set.

4. IMFF is set and logically signifies that one of the Information Multi's has been set; thus, the beginning of a record is being read.

   IMFF = EOPS/ * (IM1M + IM2M)

5. PUCF is reset, indicating that the character in the IB is to be transferred to the W-register.

   PUCF/ = (SC = 8 + 10) * (CC = 0 + D26F/ + D27F + EOPS/)

6. Since valid record is specified as seven or more serial characters, the VRCF (Valid Record Flip-flop) will be set when the seventh character has been transferred to the W register.

   VRCF = CC = 6 * D26F/

   D26F/ (Forward) is used to insure validation of the record with CC = 6 in the forward direction only, since, if we were reading backward, CC = 6 could be the second character read.

7. The Sequence Counter (SC) is counted +1 upon transfer of the eighth character to be read or this is the end of the operation (EOPS). As will be seen in SC = 9 operations, a memory store will take place when the W-register contains a full word (8 characters).

SC + 1 = PUCF * TAOD * D26F/ * (CC = 7 + EOPS) Full Word
Partial Word or
End of Record

PUCF being on when the end of a record is reached (EOPS) may find the W-register partially filled and a memory access is required. An IB to W-register transfer is prevented if this is the end of a binary write (D27F/ and EOPS/ both false).

As with VRCF, D26F/ is used to differentiate between a backward and forward read. In the case of a backward read, character 7 would be the first character detected in the record.

IMFF Figure 5-22

When an Information multi times out (only one set at a time) two possible conditions are implied:

A. Either the repetition rate of the input character string has fallen below normal specifications (internal greater than 35 us at high density) through a decrease in tape speed or improper density.
B. A space has been encountered (as would be the case at the end of a record). The separation between the last character and the LP check character is four and 1/2 character spaces (67 us at high density). This space is recognized as an improper character interval by IM5M timing out.

IIMS/ becomes true when all information multi's have timed out. Also, SKFF is normally found reset to indicate no other characters are being read at this time. IMFF is set when seven or more characters have been read (VRCF on). When reading less than seven characters, the character counter would be found not equal to seven (CC $\neq$ 7) and the invalid record is treated as a tape flaw.

IMIF Forward Read and Valid Record

IMIF, RCNF, VRCF and FWDF are all on for the following discussion and each has the following significance:

IMIF - Indexing started
RCNF - Information Encountered
VRCF - Valid Record
EXNF/ - Not a maintenance check of the inter-record gap.

The following logics are performed when a normal end of record has been detected (IMIF).

FWDF reset

The Forward Flip-flop is reset if a valid record or the End-of-File character has been read.

IBnF set to Group Mark

A Group Mark is inserted at the end of an alpha forward read or if the End-of-File character was read by itself.

EOPS Valid Record

End of Operation level becomes true when any longitudinal parity multi is set and has the same duration. Initially when EOPS becomes true during a forward read, PUCF is set to initiate an IB to W transfer for the group mark insertion. The Sequence Counter is counted +1 to allow the storing of a partial word.

W [CC] ← IB [B ➡ 1] = MAPS (D27F/ + EOPS/
SC + 1 = TAOD * D26F/ * (CC = 7 + EOPS)

During EOPS time the longitudinal parity character is read because TRL remains true after the forward Flip-flop is reset.

TRL = TAOD * RIMS/ * WGMS/ * (LP2M + LP5M + LP8M + FWDF)

SHOF is set as normally done to allow only Information Register Flip-flop that is set to complement its respective longitudinal parity flip-flop. The contents of the IR register being transferred to the IB register is redundant since the LP character is not information. The LP character is used to condition the Longitudinal Parity Flip-flops to the "all off" status. Any Longitudinal Parity Flip-flop found set indicates a parity error. See Figure 5-20.

D2OF = D3OF/ * D26F/ * HOLF * STRF * LPOS/ * SC = 8

The information Multies cannot be set during EOPS time. In Figure 5-22, the first clock pulse that finds EOPS true sets STRF. Figure 5-20 shows how HOLF is set when EOPS goes false. This logic delays the longitudinal parity check until well after the LP character has been read.

HOLF = STRF * EOPS/

With HOLF and STRF on, the next clock pulse sets the Sequence Counter to 14 and the result descriptor is formed. Any Longitudinal Parity Flip-flop found set at this time (LPOS/) indicates a parity error occurred while reading this record.

EOPS and Droupout Detected

Two or more longitudinal parity characters read during EOPS time in the forward direction is detected with the dropout logic. At the same clock pulse that sets one of the longitudinal parity multies RCNF is reset. EOPS level follows one of the longitudinal parity multies. During EOPS time one LP character is normally read and SHOF is set. See Figure 5-21. RCNF is set with this first character.

RCNF = (D26F/ + BKWF * IIMS) * SHOF

If another character was read during EOPS time SHOF would again be set. DOED now becomes true.

DOED = EOPS * SHOF * D3OF/ (BKWF + RCNF)

Notice that none of the information multi's can be set during EOPS time. This means that RCNF is not cleared until the sequence counter reaches 15 with Clear I/O Driver (CIOD).

PUCF set

Pile Up Control Flip-flop is set for two reasons. The first reason is to allow the Group Mark in IB to be placed into the W-register if this is a group mark ending. The second reason is if an alpha forward read with group mark or word count ending was being performed and a partial word was accumulated in the W-register a memory cycle must be initiated by counting the sequence counter +1.

CC transferred to PC

The contents of the character counter is placed into the pulse counter for temporary storage only if at least seven consecutive characters have been read (VRCF set). At Sequence Count of 14 the pulse counter is transferred into the result descriptor.

LPnM set

The appropriate Longitudinal Parity Multi is set to allow the reading of one and only one LP character.

LP2M is on for 700 us (low density)
LP5M is on for 250 us (high density)
LP8M is on for 200 us (very high density)

Only one of the LP multi's is set to delay the "end of operation" until sufficient time has been allowed to read the longitudinal parity character.

IMIF Forward Read with Flaws

An Information Multi timing out does not reset the Forward Flip-flop unless a valid record was read (VRCF set).

RCNF is reset at this time for all conditions while going in the forward direction.

D2OF - Parity Error Flag is reset if six or less characters read in succession are handled as flaws. These flaws generally create parity errors and since the flaws are invalid records any parity errors detected are also invalid.

```
D2OF/ = D17F/ [(RCNF * EOFS/ * VRCF/)
              +(RCNF/ * BKWF)] * IMIF
```

The longitudinal parity is checked by all the longitudinal parity flip-flops being reset after the LP character is read. Since a flaw has been read the logics assumes there will be no LP character. The LPnF are all reset in preparation for the reading of a new record.

```
LPnF/ = RCNF * VRCF/ * EOFS/ * IMIF
```

Whatever has been read into the W-register is also invalid. Therefore the W-register and the character counter are cleared in preparation for a new record.

```
W [48 ➡ 1]/ = MAPS (RCNF * EOFS/ * VRCF/ + (RCNF/ * BKWF) * IMIF
      CC/ = RCNF * FWDF * VRCF/ * EOFS/ * IMIF
```

END OF FILE RECORD - FORWARD

D21F Set For EOF Flag

A one character record would normally be detected by the logics as a flaw. If a one character record had been read the character would be in two places at the time IMIF was found set. Character position zero of the W-register always contains the first character when reading in the forward direction. The IB register is not cleared after the transfer from IB to W-register at SHOF time. The IB register retains the End-of-File character. EOFS remains true as long as the "≥" character remains in the IB register. Since only one character has been read VRCF is found reset. EOFS being true causes EOFS/ to be false. EOFS/ being false disables all the logics that is normally cleared when flaws are encountered. D20F, LPnF, W-register and the Character Counter cannot be cleared because EOFS/ is false at IMIF time.

FWDF reset with EOF

The Forward Flip-flop is reset and a Group Mark is inserted into the IB register. EOFS goes false with the next clock pulse. Since PUCF cannot be set, the Group Mark insertion is redundant since it cannot be stored into the W-register. Also, the End-of-File character in the W-register cannot be stored in memory at EOPS time because PUCF is not set to count the sequence counter +1.

LPnM set with EOF

The appropriate longitudinal parity multi is set with the clock pulse that finds IMIF set. EOPS now becomes true and the LP character is read with the same logics used to read all LP characters. The LP character in this case has the same bit configuration as the "≥" character.

EOPS/ with EOF

When the longitudinal parity multi times out EOPS/ becomes true and finds STRF set. The next clock pulse sets HOLF, causes the logics to check the Longitudinal Parity Flip-flops for a possible parity error. Exit is made to Sequence Count of 14 to form the result descriptor with W21F set. The End-of-File character is not placed in memory.

TRL IN BACKWARD READ

When reading in the backward direction TRL becomes true with the setting of BKWF at SC = 4.

TRL = TAOD * RIMS/ * WGMS/ * BKWF
RIMS/ = BRIM/ * LPIM/

There are two conditions under which Read Inhibit Multi's Not (RIMS/) prevent TRL from becoming true with the setting of Backward or Forward Flip-flops. The tape unit being at the loadpoint causes LPIM to be set and inhibit reading for 15 ms in the forward direction. The second case is where RIMS/ is held false when a backward read is performed immediately following a write operation. BRIM is held true at SC = 5 or 6 and keeps BRIM/ false until a tape turn-around has been completed.

LP Character

The tape unit now driving tape in the backward direction encounters the LP character first. The LP character is placed into the IR register and Skew Holdover Flip-flop is set.

SHOF - Backward Read

The LP Character in IRnF is transferred to the IB register. IR is cleared in preparation for the next character. Any IR Flip-flop found set complements its respective Longitudinal Parity Flip-flop. Record Control Flip-flop is not set because an Information Multi has not yet been set.

RCNF = BKWF * IIMS * SHOF
IIMS = nBID * EOPS/ * SHOF
IIMS/ = IM2M/ * IM5M/ * IM8M/

SHOF and the next clock pulse causes one of the Information Multi's to start timing out. The LP character is 4 and 1/2 character frames away from the last character of the record. The Information Multi's (IMnM) time out in 2 1/2 character frames and IIMS/ becomes true once again.

During the time out of the information multi (35 us at high density) Pile Up Control and Lost Digit Flip-flops are set. PUCF being set causes the LP character to be transferred from the IB to W-register. This LP character is handled as normal information initially and the character counter is counted down by one. The Information Flip-flop is also set at PUCF time.

IMFF = EOPS/ * IIMS * PUCF
CC-1 = TAOD * D26F * EOPS/ * PUCF
W [CC] ← IB = MAPS * EOPS/ * PUCF
PUCF/ = SC = 8 * EOPS/ * PUCF

The Lost Digit Flip-flop could detect an error if after reading the LP character a flaw was detected and set SHOF the second time before the information multi timed out.

DOED = IMFF * SHOF * LD2M/ * LD5M/ * LD8M/ * BKWF
D2OF = DOED * SHOF

IMFF - Backward Read

The information multi timing out in two and 1/2 character frames causes IIMS/ to become true. Information Index Flip-flop is set with the following logic.

IMIF = IIMS/ * SKFF/ * BFMS/ * IMFF

IMIF - Backward Read

Information Index Flip-flops (IMIF) is set for one clock pulse time. At this time RCNF is set in preparation for the record to be read. A parity error may have been detected while reading the LP character. If so, the parity error is ignored because D2OF is reset at this time.

D2OF/ = IMIF * D17F/ * RCNF/ * BKWF

Also the W-register is cleared and the character counter is set back to seven. The LP character that was initially set into the W-register is now lost. The Backward Flaw Multi is set to indicate a flaw or a LP character has been read.

BFnM = RCNF/ * BKWF * nBID * IMIF

TRL and RCNF - Backward Read

The last character of the record is read first and placed into the IR register. SHOF is set to transfer this character into IB and to complement the LPnF. The Information Multi corresponding to the selected density is set. The Lost Digit Flip-flop is set to provide drop-out detection.

PUCF - Backward Read

During the time Pile Up Control Flip-flop is set the character in IB is transferred into the W-register. The character counter is counted down by one. If this is the seventh character, VRCF is set to remember a valid record has been read. When the W-register has been filled, (CC = 0) the sequence counter is counted to nine to store the word in memory. Also, the Information Flip-flop is set to provide for indexing logics when all information multi's have timed out.

IMFF = EOPS/ * IIMS * PUCF

SC = 9

The logics indicates the W-register is filled when the character counter has been counted to zero. At SC = 9 a memory cycle is performed to write the contents of the W-register into memory. The character counter is set to seven as the word counter is counted down by one. No Memory Accesses are granted if the word counter is already found equal to zero.

SC = 10

The D register bits 1 ➡ 15 are counted down since the beginning address was assumed to point to the least Significant address. The sequence counter is set to 8 and the logics wait for the next word to be read from tape.

IMIF - Backward Read Indexing

If, after two and one-half character spaces no more characters are read from tape to reset the information multi, IIMS/ becomes true. At high density the backward flaw multi times out in 100 us after the last character was read from tape the corresponding information multi, timed out in 35 us IMIF is set when the information multi times out and a valid record has been read.

IMIF = IIMS/ * SKFF/ * VRCF * IMFF

IMIF * RCNF * BKWF

The Backward Index Multi (1.2 ms) is set if an End-of-File level is true or if VRCF is on. This multi provides the delay in resetting BKWF to allow the read/write head to be positioned well into the inter-record gap. The IB register is cleared at this time.

A partial word has been left in the W-register if the character counter is found not equal to seven. The logics sets PUCF to allow the transfer of the IB register into the W-register.

Only in a backward alpha read is the W-register filled with question marks in this manner. Each clock pulse that finds PUCF on does an IB to W transfer of a question mark. PUCF cannot be reset until the character counter has been counted to zero.

PUCF/ = SC = 8 * (CC = 0 + D26F/ + D27F + EOPS/)

In a binary backward read, no question mark insertions are allowed when the character counter is not equal to seven at IMIF time. PUCF is set to seven at IMIF time. PUCF is set for one clock pulse time to allow a SC + 1 to store the partial word. An IB to W transfer is prohibited at EOPS time and a binary read is performed.

W [CC] ← IB [B → 1] = MAPS * (D27F/ + EOPS/) * PUCF

EOPS for Backward Read

BWIM being set at IMIF time causes EOPS (End Operation Pulses) to be true for 1.2 ms. STRF is set with the first clock pulse. During this 1.2 ms period any flux changes being read causes a dropout to be detected.

DOED = EOPS * SHOF * D30F/ * BKWF
D20F = DOED

The Backward Flip-flop is not reset until EOPS goes false with STRF set. At SC = 8 in Figure 5-20 HOLF and STROF resets BKWF. At the same time the sequence counter is set to 14 to form the result descriptor.

SECTION 6

B5500 MODEL II SPO

GENERAL

The Teletype Model 33 Typewriter is used as a Supervisory Print Out (SPO) of MCP messages. The SPO is also used as a keyboard entry for the operator to interrogate or instruct the MCP operation.

The I/O Control provides the logics necessary to transfer messages between core memory and the Supervisory Printer.

The B495 Model I SPO (Smith - Corona) with associated logics rack and the B495 Model II SPO (Teletype Model 33) with its associated logics rack are directly interchangeable with all versions of the I/O controls (Models I, II or III). Since the Model I SPO's are being discontinued only the Model II SPO is discussed here. Only one B495 SPO may be cabled to a B5500 System. The Model II SPO logics rack is located in the B5310 Console as was the Model I logics rack. The Model II SPO logics rack and Model I SPO logics rack are not interchangeable without exchanging the typewriters.

INPUT REQUEST SWITCH

No input message can be entered until the operator first depressed the INPUT REQUEST switch. Central Control's Input Request Interrupt Flip-flop (CCI05F) is set and the MCP branches to a SPO Read Instruction. At this time, the READY light is lit and the operator may begin his input message. The depression of each key on the keyboard causes the characters to be transferred to the W-register. The END-OF-MESSAGE Switch is depressed by the operator when the input message has been completed. A Group Mark Character is placed into the W-register by the END-OF-MESSAGE Switch. The remainder of the W-register behind the Group Mark Character is left cleared. The contents of the W-register is written into memory. No Group Mark Character is printed on the SPO. The END-OF-MESSAGE Switch also causes the SPO to perform a Carriage Return and a Line Feed.

PARITY CHECK

All input characters from the SPO are checked for character parity while each character is in the IB-register. Input characters are generated in USASCII code by the keyboard switches. The SPO logics rack in the B5310 Console contains a USASCII to BCL translator. Characters enter the IB-register via the Input Character lines in BCL code plus even character parity. D20F in I/O is set when any odd character parity is found in the IB-register.

No parity check is made in the SPO logics rack for characters leaving or entering the I/O. The I/O logics does not check the output of the OBnF since no character parity is transmitted to the SPO.

ERROR SWITCH

In case of an operator error, the operator may wish to change or correct his input message by depressing the Error Switch and then re-enter the entire message. The

Typewriter Error Switch performs the same identical functions as the END-OF-MESSAGE Switch except a parity error is forced in the translator on the Group Mark Character. D20F is set by the parity error on the Group Mark Character in IB. The MCP must be programed to return to the beginning of this Read Instruction if D20F is found on in the Result Descriptor. When the Input Ready Light again becomes lit, the operator re-enters his message.

SPO WRITE

The MCP may initiate a SPO Write at any time. This output message can only be terminated with a Group Mark Character in memory. Messages printed on the SPO do not require any special editing or formatting. After 72 characters have been printed, a switch closes and causes an automatic Carriage Return and Line Feed. The Group Mark Character may occur at any character location. The SPO logics rack converts the Group Mark into a Carriage Return and a Line Feed, thus inhibiting the printing of the Group Mark.

READ OR WRITE DESCRIPTORS

The I/O Descriptor is placed into the D-register of any of four I/O controls. The bits of this read or write descriptor have the following significance.

D48F, D47F, D46F = These bits are lost in the transfer of W-register to D-register.
D45F thru D41F = Unit Designate (Octal 74)
D40F thru D31F = Word Count Field not used with SPO.

D30F = 0 Allows data transfer between the I/O and the SPO.

D27F = 0 Binary/Alpha Bit: All SPO reads or writes are performed in Alpha Mode.

D26F = 0 Not used with SPO

D25F = 0 This bit is always reset since the word counter is not used.

D24F = 1 This bit being on causes a Keyboard Read operation to be performed.

D24F = 0 This bit being off causes a SPO Write operation to be performed.

D23F = 0 Not used.

D22F = 1 When a memory cycle is attempted on a non-existent address MAED-C is returned to I/O as a true level. D22F is set at SC=9 and becomes a part of the Result Descriptor. At SC=10, D22F forces the termination of a SPO Write when a Group Mark Character is forced into the W-register.

D21F = 0 Not used.

D20F = 1 Any character parity errors sensed in the output of the IB register during a Keyboard Read are remembered with this flip-flop. D20F becomes part of the result descriptor. No parity errors are sensed in the output of the OBnF during a SPO Write.

D19F = 1 D19F is set when a Core Memory parity error occurs during memory accesses with I/O. This bit is part of the Result Descriptor.

D18F = 1 D18F is on in the Result Descriptor if TRDL/ was found true. TRDL/ indicates the Typewriter was in a Local or Not Ready status when the I/O tried to connect up to the SPO at SC=3 and CC=3.

D17F = 1 Used only to request memory accesses in Standard Sequence count logics.

D16F = 1 If D16F is found on in the Result Descriptor, then some other I/O was already using the SPO when this I/O tried to connect up to the SPO at SC=3 and CC=1.

D15F thru D01F = The beginning core memory address. In the Result Descriptor, D15 thru 1 represents the last core memory location accessed plus one.

GLOSSARY OF TERMS

SIGNAL LINES TO SUPERVISORY PRINTER

ODRL/ Output Driver Level Not: ODRL is only used during a SPO Write. When ODRL/ in I/O is false OUTS in the typewriter is held true to gate the OBnF's into the typewriter print decoder.

TOPL/ Typewriter Operation Level Not: This level remains true all during a SPO write operation to keep LINS false in the typewriter. RUNS is therefore held true and PUMP is continuously timing out. The Control Counter being counted to the START position causes the selector magnet to be deenergized. Anytime the selector magnet is deenergized the selector clutch is mechanically tripped and causes the typewriter to commence a print cycle. TOPL/ remains false during a Keyboard Read Operation to keep the Ready light on in the SPO.

INnL Information Levels 1 through B: These information levels are developed from the outputs of the OBnF in I/O and are used to transmit characters to the typewriter during a SPO Write.

SIGNAL LINES FROM SUPERVISORY PRINTER

ICnL Input Character Level 1 through P: These levels originate in the typewriter translator and represent the character depressed on the keyboard in BCL code.

ICRL/ Input Character Ready Level Not: This term goes false with a Control Count of 3 during a Keyboard Read operation. LINS being false during a SPO write inhibits ICRL at C=03.

OCRL/ Output Character Ready Level Not: The typewriter logics causes this level to go false during a SPO write with clock counter equal to 8. OCRL/ is not used during a keyboard read.

TINL/ Typewriter Interrupt Level Not: This level becomes a false level when the operator depressed the Input Request Switch on the typewriter. TINL/ going false sets CCI05F in Central Control.

TRDL/ Typewriter Ready Level Not: This level is at ground potential when system power is on and the typewriter LOCAL/LINE switch is in the LINE position.

GENERAL DESCRIPTION OF OPERATION

A SPO read or write operation is initiated identically as reads or writes on any other peripheral device. The Unit Designate field being equal to an octal 74 connects the SPO to the I/O control. See Figure 6-2.

The Processors Initiate I/O Syllable places the address of the I/O descriptor into absolute Cell 10 and sets the Commence Timing F/F CMTF in Central Control. Central Control gating selects any idling I/O and forces that I/O to access cell 10 immediately to obtain the I/O descriptor address. All I/O operations are performed independent from the processor. Figure 6-1 shows the sequence of operation and the information and control paths are shown in Figure 6-2. The logics must proceed through the standard sequence count logics to SC=3 and CC=5 as do all I/O operations.

SPO/KEYBOARD FLOW (FIGURE 6-3)

KEYBOARD READ SC=3 AND CC=5

The next clock pulse clears the Character Counter and D25F. With D24F on, the Sequence Counter is set to 8.

SEQUENCE COUNT EQUALS EIGHT

STRF to 1

During a Keyboard Read, the I/O does not know a character is on the ICLn lines until I24D becomes a true level and HOLF is off. Input Character Ready Level (ICRL/) going false causes I24D to become true. ICRL/ becomes false during Control Counter equal to 3 in Model II SPO logics rack.

HOLF to 1

With STRF on the next clock pulse sets HOLF provided this is not a tape operation (D41F/).

STRF to 0

With HOLF on, the next clock pulse clears STRF.

HOLF to 0

ICRL/ going true causes I24S/ to become true 9.09 ms after STRF was set and clear HOLF. ICRL/ goes true after the Control Counter in the typewriter logics rack leaves the count of 3.

CC + 1

The clock pulse that transfers a character from IB to W-register (STRF * HOLF) also counts the Character Counter plus one.

IB (P thru 1) to 0

Normally the clock pulse that transfers IB to W also clears IB in preparation for the next input character. When the input character in IB is a Group Mark, GPMS becomes true. The Group Mark is placed into the W-register with HOLF and STRF but the IB is not cleared because GPMS/ would be false. The IB register must retain the Group Mark while the partial or full word in the W-register is written into memory at SC=9. At SC=10 GPMS remaining true causes the logics to exit to SC=14 instead of returning to SC=8.

IB (P thru 1) to W (CC)

After STRF is set the next clock pulse sets HOLF. With HOLF and STRF both set, the IB register is gated into the W-register with the next clock pulse. The setting of the Character Counter determines which character position in the W-register the contents of IB is placed.

D2OF to 1

The character entering the IB register is in BCL code and thus requires even parity. Any odd parity found in the IB register causes PELS to be true and set D2OF.

EXNF to 1

STRF is reset the next clock pulse after HOLF was set. HOLF remains set while ICRL/ is false (9.09 ms). EXNF may be set the next clock pulse after STRF is reset if the W-register contains a full word (CC=0) or a partial word (GPMS).

SC + 1 and EXNF to 0

EXNF is used as a logical flip-flop to count the Sequence Counter to 9. Once SC=9 EXNF is no longer needed.

SEQUENCE COUNT EQUAL TO NINE

Here a normal I/O to memory write of the W-register is performed. MANF is set with the first clock pulse. If no other I/O or processor is accessing the requested memory module, MTOD-M is returned from memory through C/C to I/O. D24F being set causes MWRD to be true in C/C. MAOF is set with the second I/O clock pulse. The third clock pulse clears the W-register, MANF, and advances the Sequence Counter to ten.

SEQUENCE COUNT EQUAL TO TEN

The first clock pulse finds MANF reset and therefore clears MAOF. The address portion of the D-register (15 thru 1) is counted plus one provided the address flip-flops are not already all on (MAX/).

If the IB does not contain a Group Mark, GPMS/ would be true during a Keyboard Read (KSOD) and the logics would return to SC=8. A Group Mark Character can only be placed into the IB register by the operator depressing the End of Input or Error Switches on the typewriter.

GPMS being true at SC=10 forces the logics to exit to SC=14 and write the result descriptor into absolute cells 14, 15, 16 or 17.

SPO WRITE

A Keyboard Read descriptor is converted to a SPO Write by resetting D24F. At SC=3 and CC=5, D24F being reset causes the logics to proceed to SC=9 and access the first word from memory to be written on the SPO.

SEQUENCE COUNTER EQUAL TO NINE

The first clock pulse sets MANF to request access to a memory module. Central Control grants access to I/O and initiates a memory cycle. At read strobe time, memory returns MT2D-M through C/C to I/O. Memory Access Obtained Flip-flop (MAOF) is set with the next clock pulse that finds MT2D true.

$$\text{MAOF to 1} = \text{MANF} * \text{MT2D-M}$$

With MAOF set, the next clock pulse gates the contents of Memory Information Register (MIR) from memory through C/C to the W-register in I/O. MANF is cleared as the Sequence Counter is advanced plus one.

SEQUENCE COUNTER EQUAL TO TEN

MAOF to 0

MANF being reset causes MAOF to be reset with the first clock pulse.

D (15 thru 1) plus 1

The core memory address portion of the SPO write descriptor is advanced plus one provided the maximum core memory address has not already been reached.

W (CC) to OB (B thru 1)

At this time the I/O Character Counter is pointing to character zero in the W-register (CC=0). Character position zero of the W-register is gated into the OBnF with the first clock pulse.

CC + 1

The Character Counter is counted plus one and now points to character position one in the W-register.

SC to 8

Keyboard-SPO Operation Driver (KSOD) is held true by an octal 74 in the unit designate field D45F thru D41F. MS1OD is true because the Sequence Counter is equal to 10 and the Inhibit Memory Cycle switch is in the down position. Group Mark Switch Not (GPMS/) is true as long as the OBnF do not contain a Group Mark.

$$\text{GPMS} = \text{D24D/} * [\text{OB (B thru 1)} = 1] * \text{AGMS}$$

$$\text{AGMS} = [\text{CROD} + \text{PAOD} + \text{PPOD} + \text{DROD} + \text{INOD} \bullet \text{LCHF}]^{-1}$$

HOLF to 1

The Holdover Flip-flop (HOLF) is set to prevent STRF from being set with the first clock pulse at SC=8. In this manner HOLF prevents an end of character timing cycle from being performed before the first character in OBnF has been printed on the SPO.

SEQUENCE COUNT EQUAL TO EIGHT WITH D24F/

The initial entry to SC=8 finds HOLF set to prevent the setting of STRF with I24D true. The output of O21D is made true upon entry to SC=8. ODRL/ is therefore false and causes OUTS in the typewriter to gate the outputs of OBnF into the print decoder.

$$O21D = HOLF * STRF/ * D24F/ * KSOD * SC=8$$

Typewriter Operate Level Not (TOPL/) is sent to the typewriter as a true level because D24F is reset. TOPL/ causes LINS to go false in the typewriter. LINS going false causes RUNS to become a true level. RUNS starts the Clock Gate Multi (CLGM) timing out. Every 9.09 ms a clock pulse is produced in the typewriter logics rack to count the Control Counter. At this point the Control Counter has not had time to print the first character. OCRL (Output Character Ready Level) remains true in the SPO until the Control Counter reaches the count of 8.

$$OCRL = TOPL/ * C \neq 08$$

OCRL/ to C/C remains false until the print cycle in the typewriter is completed at Control Count of 8. At C=08, OCRL/ becomes true and I24S/ in the I/O also becomes true. The next I/O clock pulse resets HOLF. I24S/ going true indicates each character sent to the SPO has been printed and initiated the end of character timing cycle in I/O.

STRF to 1

With HOLF reset STRF is set with the next clock pulse that finds I24D true. The typewriter Control Counter has left the count of 8.

W (CC) to OB (B thru 1)

The next clock pulse finds STRF set and HOLF reset. If the character already in the OBnF is not a Group Mark, GPMS/ is true and the next character pointed to by the character counter is gated into the OBnF.

HOLF to 1

The next clock pulse that finds STRF set causes HOLF to be set.

IB (P thru 1) to ZERO

This is a redundant operation during a SPO print.

STRF to 0

With HOLF on, the next clock pulse clears STRF. HOLF cannot be cleared until I24S/ becomes true again with Control Counter equal to 8.

SC + 1

The Sequence Counter is counted to nine to access the next word from core memory. The last character in the W-register has been placed in the OBnF when the Character Counter has been counted back to zero. (CCOD true).

EXNF to 1

External Control Flip-flop (EXNF) is used as a logical flip-flop to terminate a SPO write. The first character is shifted into the W-register at SC=10. If this character was a Group Mark, then EXNF is set with the first clock pulse at SC=08.

EXNF = STRF/ * CC1D * GPMS

The second or any succeeding character placed into the OBnF may be a Group Mark and cause GPMS to become a true level. EXNF would be set with the next clock pulse after the Group Mark was placed into the OBnF.

EXNF = STRF * HOLF * GPMS

The OBnF containing the BCL code for a Group Mark cause GPMS in the typewriter logics rack to also become true. GPMS in the typewriter causes an automatic carriage return and a Line Feed on the typewriter. The Group Mark character is not printed on the SPO.

W (48 thru 1) to 0

At the completion of the Group Mark Character print cycle on the SPO (C=08), STRF is again set. At this time the logics clears the W-register and exits to SC=14. The Group Mark Character is not Printed on the SPO because the Carriage Return Switch output becomes true at Control Count of 1. A Carriage Return is thus performed instead of the printing of a Group Mark.

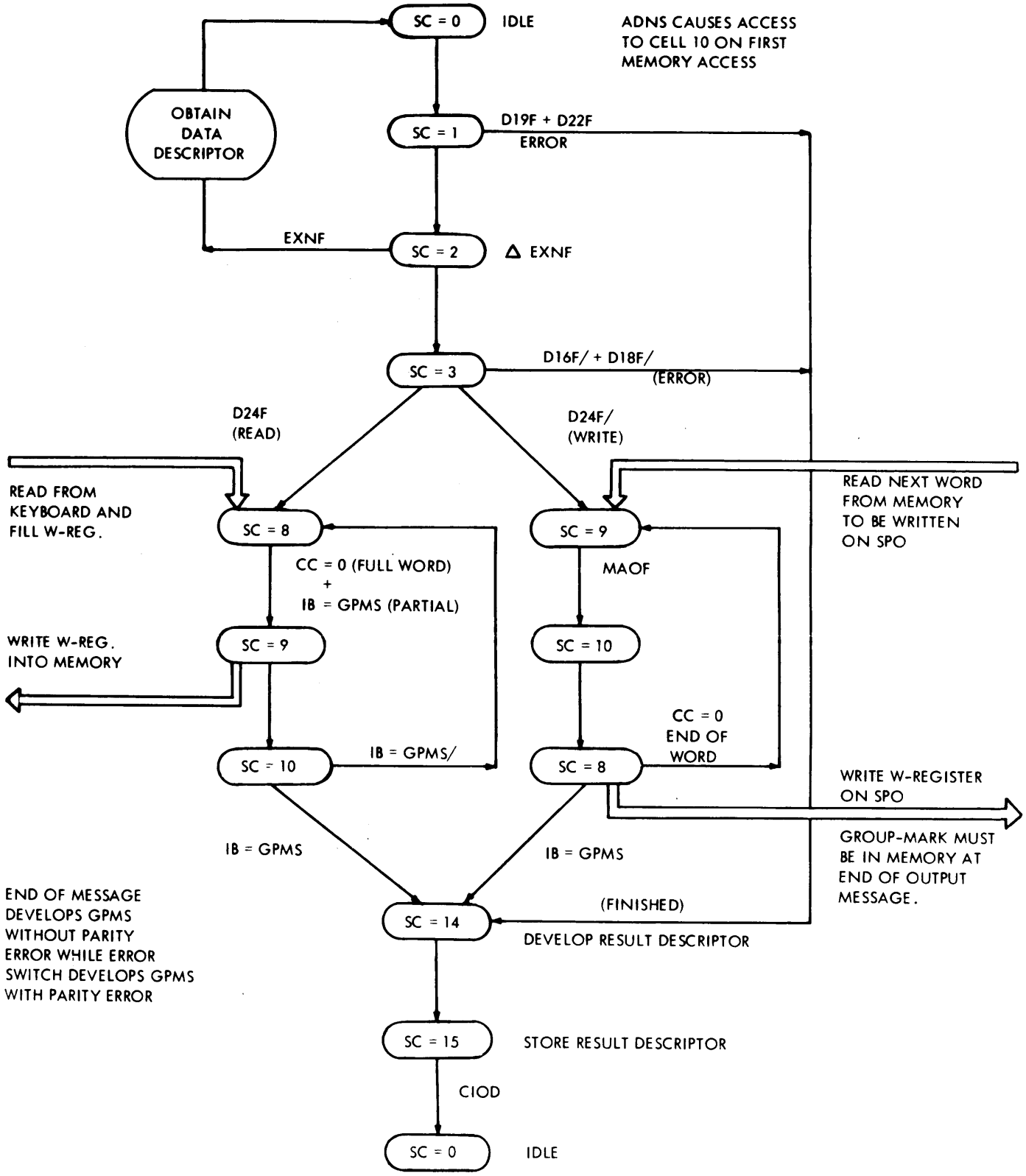


FIGURE 6-1 GENERAL BLOCK DIAGRAM

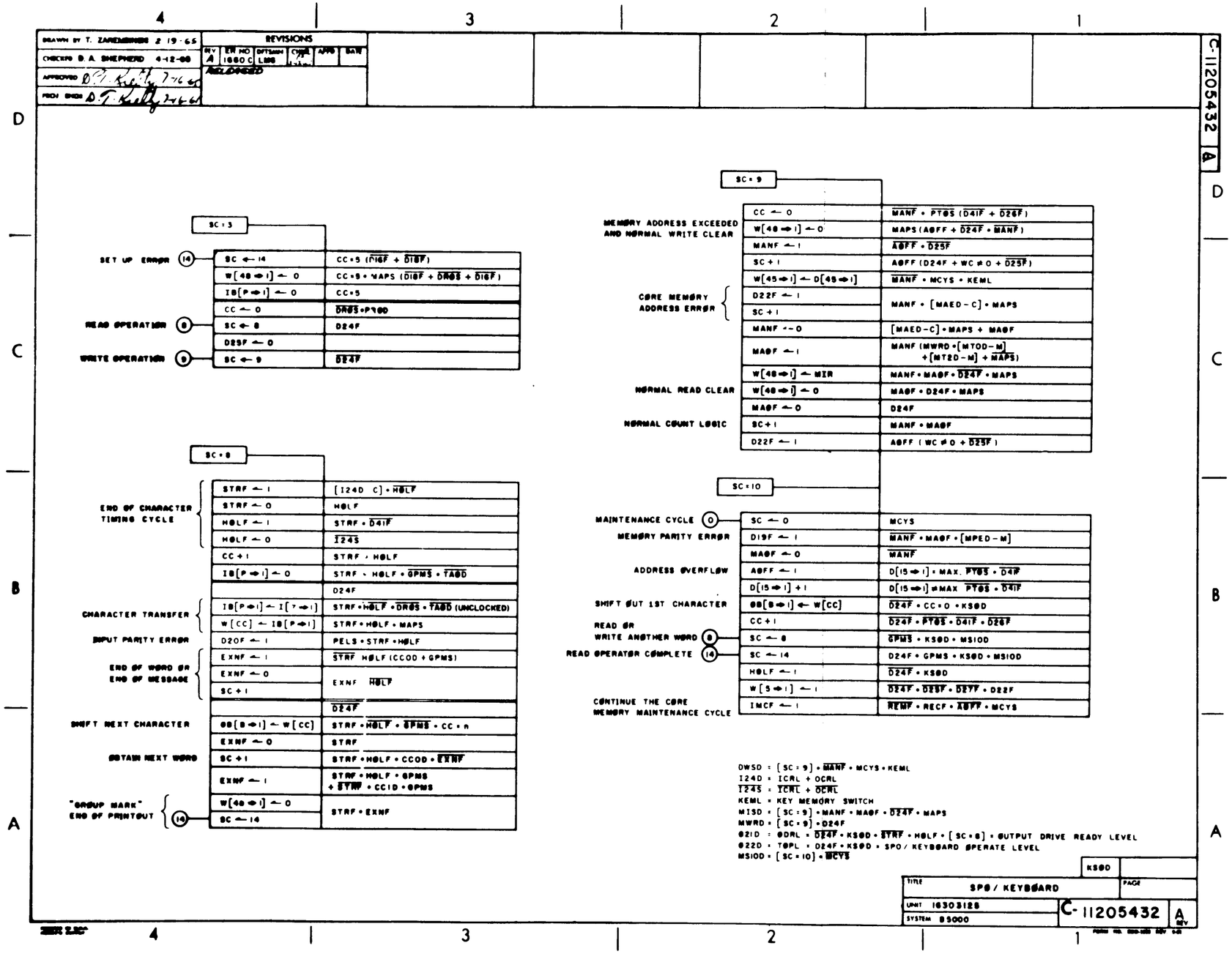


FIGURE 6-2 I/O FLOW

SPO TRANSLATOR INPUTS AND OUTPUTS

		FROM KEYBOARD	BCL CODE TO OR FROM SYSTEM	CODE TO SELECTOR MAGNET	
LOCAL	REMOTE	INPUT LEVELS (TT) TO TRANSLATOR	OUTPUT LEVELS (IC) FROM TRANSLATOR	PRINT BARS SELECTED IN TYPEWRITER	
		1234 5 678	1248 A B	1234 5 678	
				BCL	
SP	SP	0000 010	0000 1 0	0000 0 101	EXCEPTION
>	.	0111 010	1101 1 1	1101 1 011	
LF	[	0101 000	0011 1 1	0011 1 011	
9	(	1001 010	1011 1 1	1011 1 011	
]	<	0111 110	0111 1 1	0111 1 011	
NONE	GM	1111 101	1111 1 1	CR and LF	
7	&	1110 010	0000 1 1	0000 1 011	
4	$	0010 010	1101 0 1	1101 0 011	
8	*	0001 010	0011 0 1	0011 0 011	
-	)	0000 001	1011 0 1	1011 0 011	
,	;	1101 110	0111 0 1	0111 0 011	
"	∨	1111 110	1111 0 1	1111 0 011	
≠	-	0101 110	0000 0 1	0000 0 011	
:	/	1011 010	1000 1 0	1000 1 101	
@	,	0011 010	1101 1 0	1101 1 101	
5	%	1010 010	0011 1 0	0011 1 101	
NONE	=	1111 111	1011 1 0	1011 1 101	
.	]	1101 101	0111 1 0	0111 1 101	
2	"	0100 010	1111 1 0	1111 1 101	
3	#	1100 010	1101 0 0	1101 0 101	
1	@	1000 010	0011 0 0	0011 0 101	
#	:	1101 010	1011 0 0	1011 0 101	
%	>	0011 110	0111 0 0	0111 0 101	
≥	≥	1111 010	1111 0 0	1111 0 101	
0	+	0101 010	0101 1 1	0101 1 011	
J	A	1000 001	1000 1 1	1000 1 011	
K	B	0100 001	0100 1 1	0100 1 011	
L	C	1100 001	1100 1 1	1100 1 011	
M	D	0010 001	0010 1 1	0010 1 011	
N	E	1010 001	1010 1 1	1010 1 011	
O	F	0110 001	0110 1 1	0110 1 011	
P	G	1110 001	1110 1 1	1110 1 011	

SPO TRANSLATOR INPUTS AND OUTPUTS

		FROM KEYBOARD	BCL CODE TO OR FROM SYSTEM	CODE TO SELECTOR MAGNET	
LOCAL	REMOTE	INPUT LEVELS (TT) TO TRANSLATOR	OUTPUT LEVELS (IC) FROM TRANSLATOR	PRINT BARS SELECTED IN TYPEWRITER	
		1234 5 678	1248 A B	1234 5 678	
				BCL	
Q	H	0001 0 011	0001 1 1	0001 1 011	
R	I	1001 0 011	1001 1 1	1001 1 011	
=	X	1011 110	0101 0 1	0101 0 011	
X	J	0101 0 011	1000 0 1	1000 0 011	
$	K	1101 0 011	0100 0 1	0100 0 011	
*	L	0011 0 011	1100 0 1	1100 0 011	
)	M	1011 0 011	0010 0 1	0010 0 011	
;	N	0111 0 011	1010 0 1	1010 0 011	
≤	O	1111 0 011	0110 0 1	0110 0 011	
&	P	0000 1 011	1110 0 1	1110 0 011	
A	Q	1000 1 011	0001 0 1	0001 0 011	
B	R	0100 1 011	1001 0 1	1001 0 011	
¢	≠	0011 101	0101 1 0	0101 1 101	
C	S	1100 1 011	0100 1 0	0100 1 101	
D	T	0010 1 011	1100 1 0	1100 1 101	
E	U	1010 1 011	0010 1 0	0010 1 101	
F	V	0110 1 011	1010 1 0	1010 1 101	
G	W	1110 1 011	0110 1 0	0110 1 101	
H	X	0001 1 011	1110 1 0	1110 1 101	
I	Y	1001 1 011	0001 1 0	0001 1 101	
+	Z	0101 1 011	1001 1 0	1001 1 101	
?	0	0000 1 101	0101 0 0	0101 0 101	
/	1	1000 1 101	1000 0 0	1000 0 101	
S	2	0100 1 101	0100 0 0	0100 0 101	
T	3	1100 1 101	1100 0 0	1100 0 101	
U	4	0010 1 101	0010 0 0	0010 0 101	
V	5	1010 1 101	1010 0 0	1010 0 101	
W	6	0110 1 101	0110 0 0	0110 0 101	
X	7	1110 1 101	1110 0 0	1110 0 101	
Y	8	0001 1 101	0001 0 0	0001 0 101	
Z	9	1001 1 101	1001 0 0	1001 0 101	
6	?	0110 010	0000 0 0	0000 1 101	EXCEPTION
				BCL	

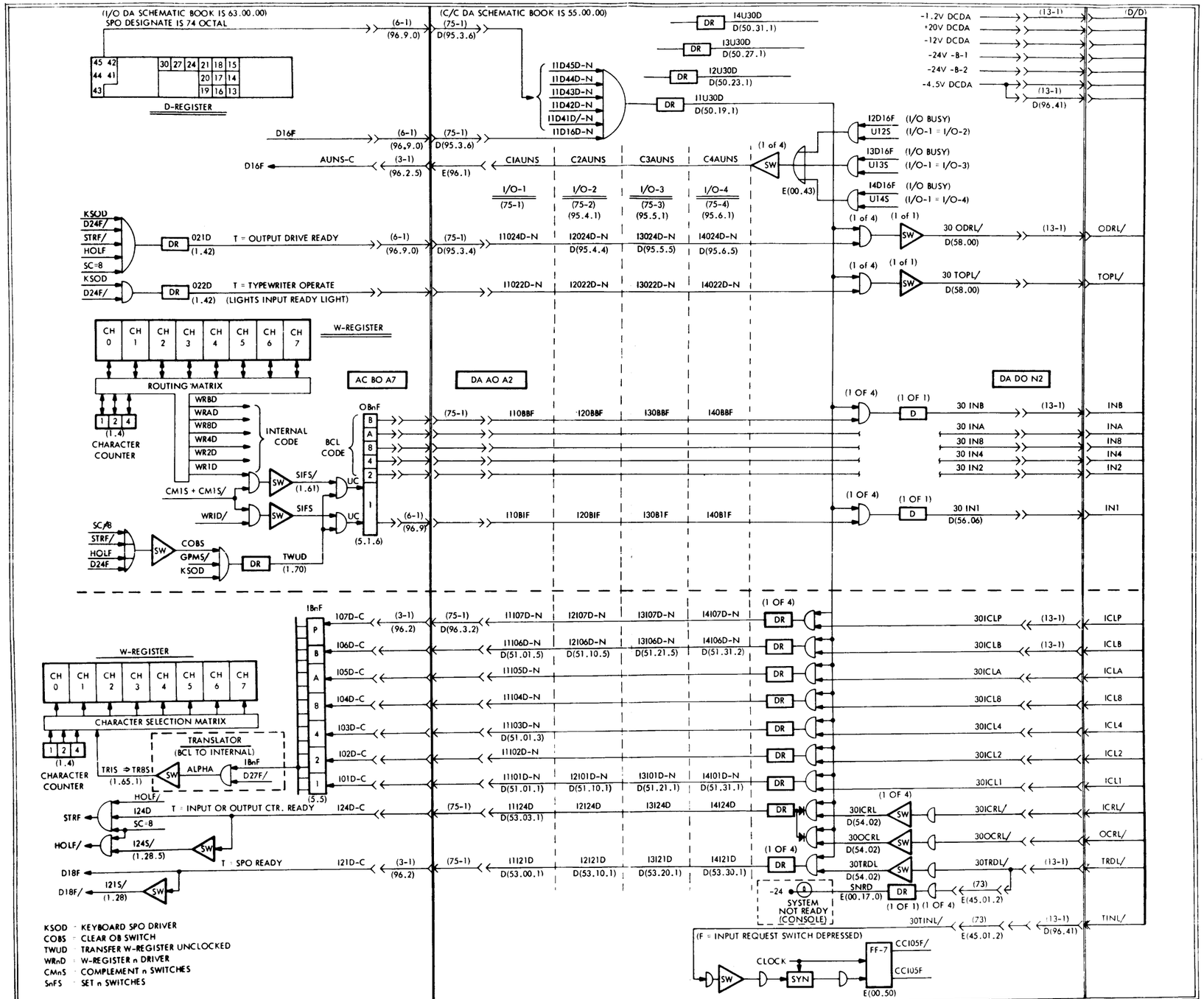


FIGURE 6-3 CONTROL SIGNALS BETWEEN SPO LOGICS RACK & I/O.

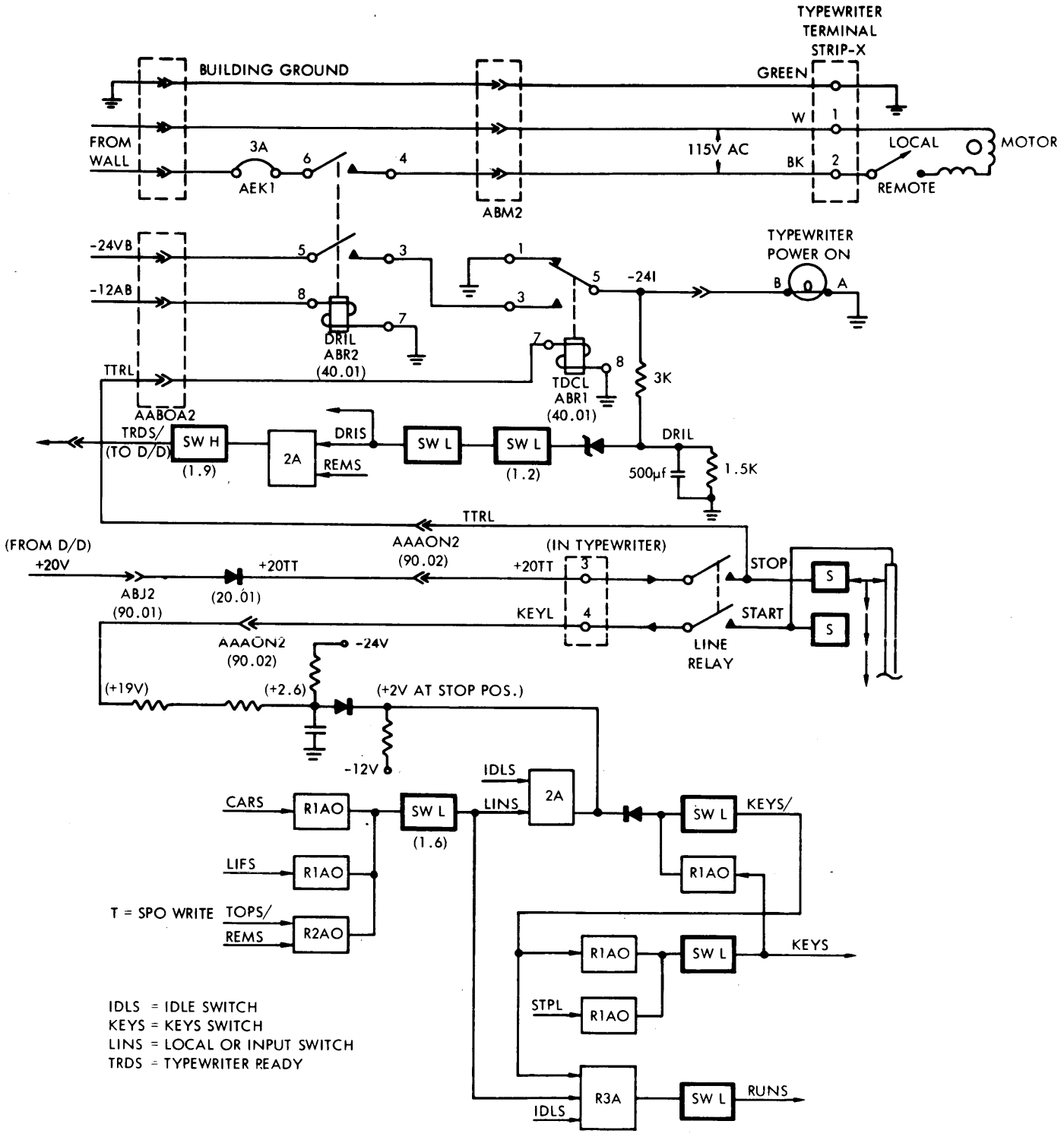


FIGURE 6-4 TYPEWRITER READY CIRCUIT

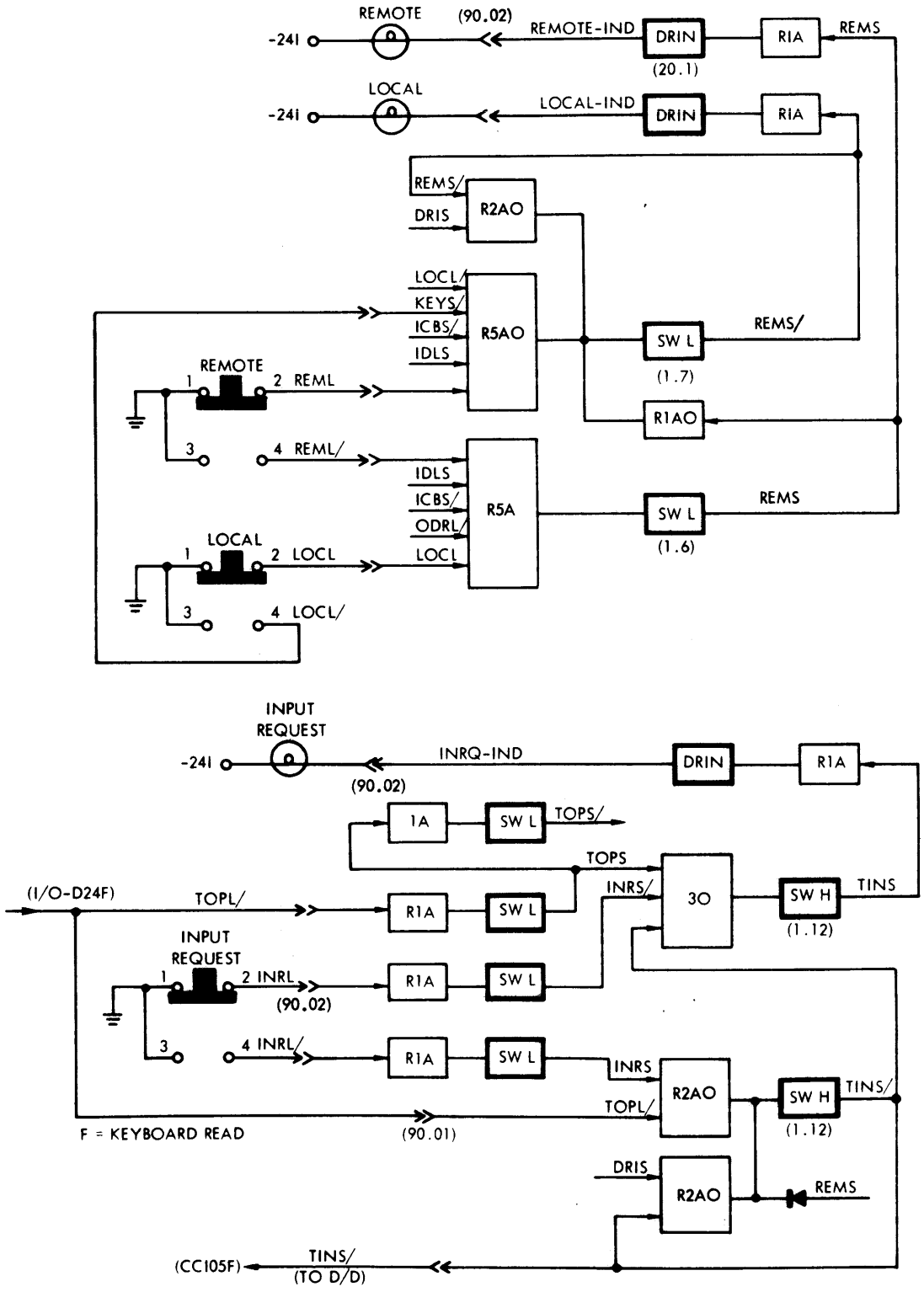


FIGURE 6-5 REMOTE AND INPUT REQUEST

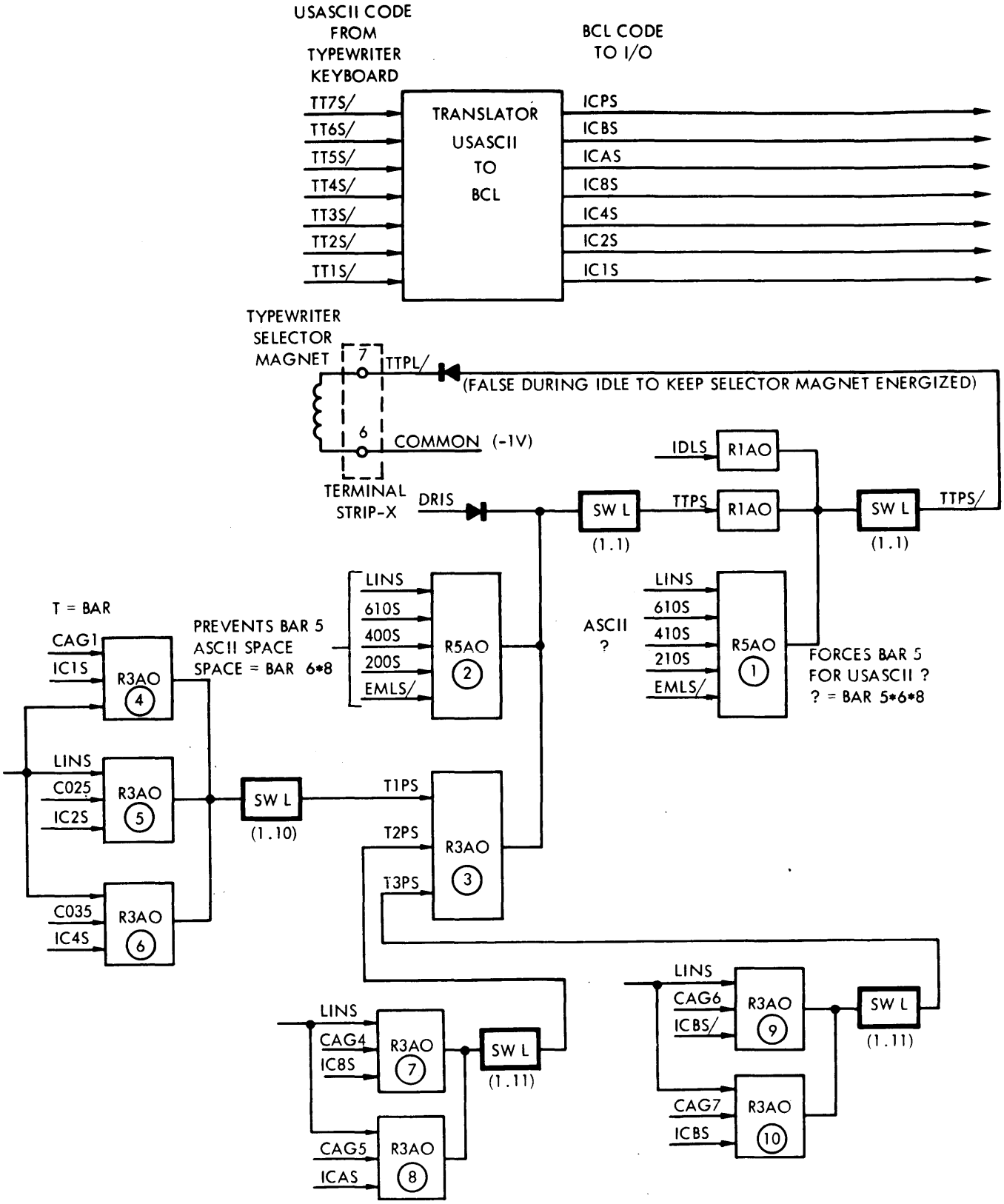


FIGURE 6-6 BCL TO SELECTOR MAGNET CODE

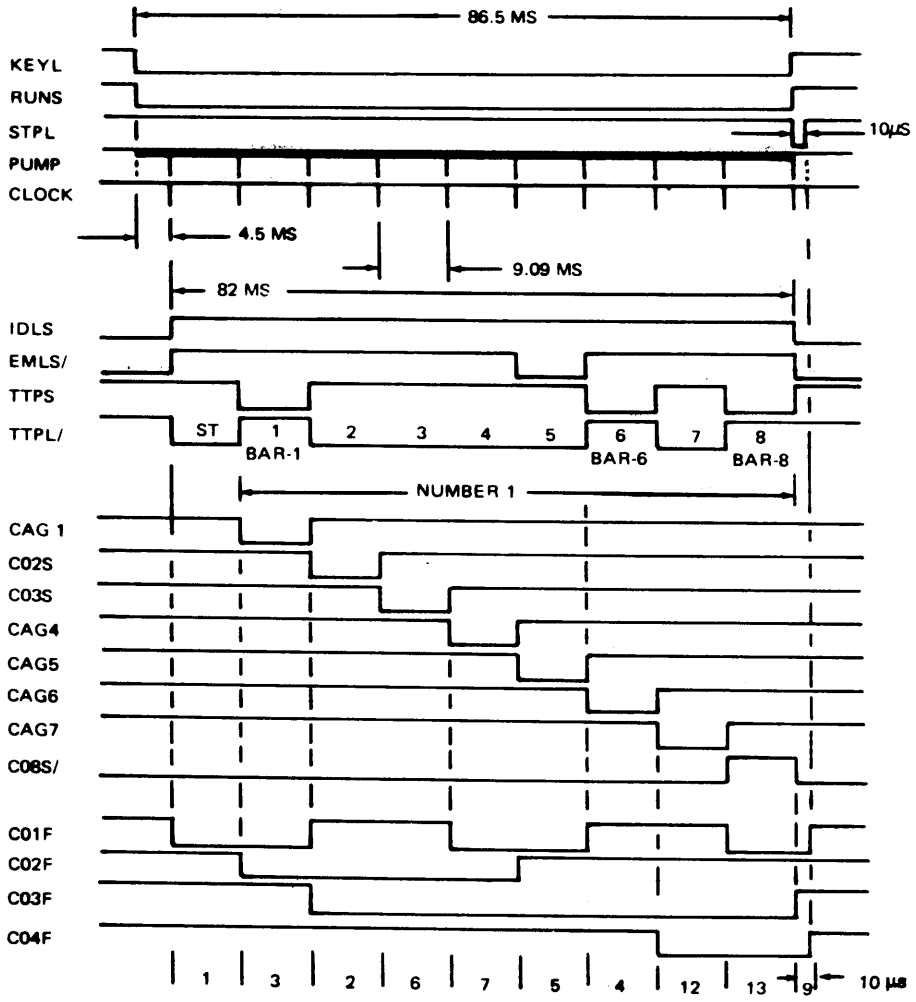


FIGURE 6-7 TYPEWRITER PRINT FROM KEYBOARD

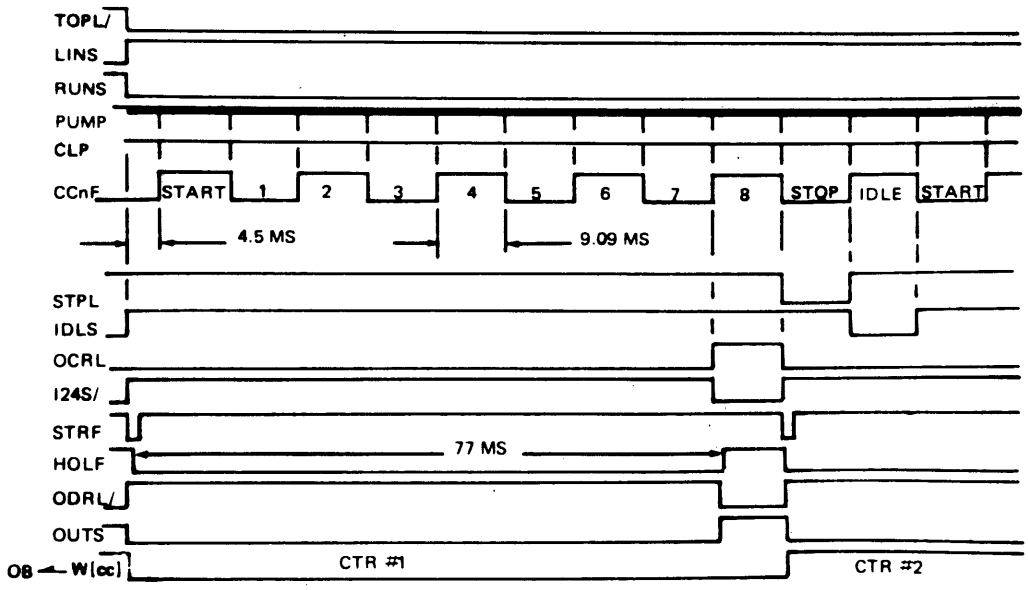


FIGURE 6-8 I/O WRITE TO SPO

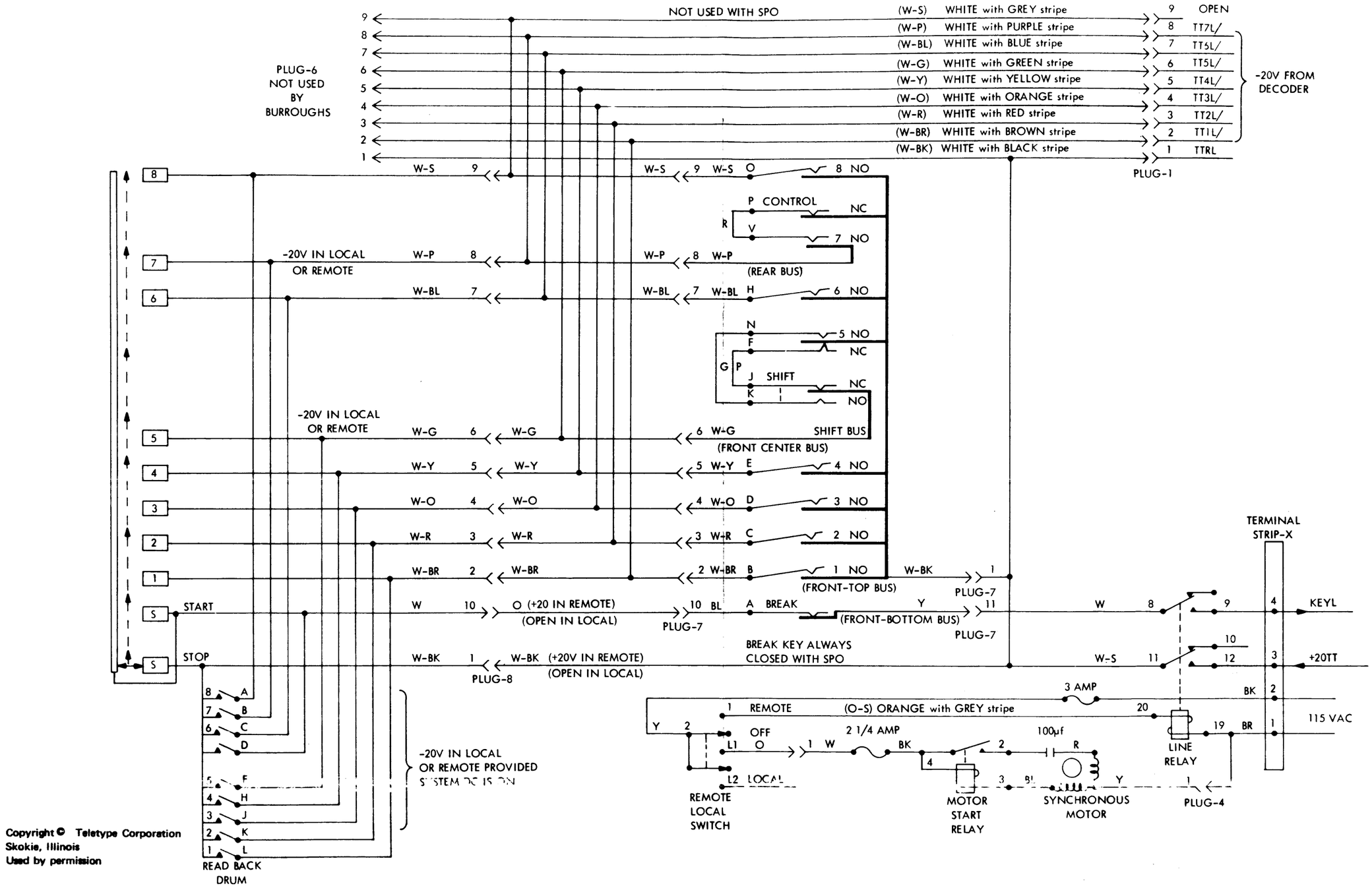


FIGURE 6-9 MODEL II TYPEWRITER DISTRIBUTOR

SECTION 7

B5500 DISK FILE

GENERAL

The Disk File Storage units provide large data storage for the B5500 System. Random access of large or small segments of data is only one of the major advantages of a Disk File System. Listed below are the different Disk Files compatible with the B5500 MODEL I, II and III I/O.

		B5470	DISK FILE CONTROL
B9373	=	B471	ELECTRONICS UNIT (40 ms MAX ACCESS)
B9374-1	=	B475	STORAGE MODULE (9.6 MILLION CTRS. 240 CTRS/SEG.)
		B5470-1	DISK FILE CONTROL (IB) DATA BANK
B9373-8	=	B473	ELECTRONICS UNIT (IB-80 ms MAX ACCESS)
B9376-9	=	B477-2	STORAGE MODULE (IB-19.2 MILLION CTRS. 240 CTRS./ SEG.)
		B5470-1	DISK FILE CONTROL (IB) DATA BANK
B9373	=	B471	ELECTRONICS UNIT
B9374-1	=	B475	STORAGE MODULE

Reading or writing on the Disk File is modular only by 240 characters per segment. Each read or write operation may encompass from 1 to 63 consecutive segements. Segment count is a function of the Disk File Control Unit.

The Disk File I/O Descriptor specifies the number of segments and the core memory location of the disk address. Word count override of from 1 to 1023 words may be used. The disk file address is stored in the first word of memory pointed to by D01F thru D15F in the descriptor. The disk file address is not part of the word count. The disk address word is always a binary transfer of seven digits; zero through nine. The I/O descriptor may specify either an alpha or binary information transfer.

When a write operation is terminated by word count override, any remaining part of the segment or remaining segments are filled with blanks for alpha writes or zeros for a binary write. A write descriptor overflowing into a locked-out disk causes a termination of the operation and the error condition is flagged in the result descriptor.

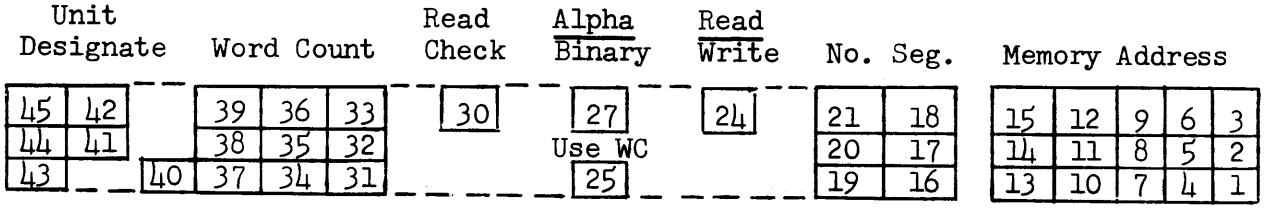
If a parity error occurs while obtaining any descriptor from memory or when transferring a disk address to the Disk File Control, the operation is terminated and the error condition is reported in the result descriptor.

For a Read Check descriptor, the I/O Control unit transfers the address word and the segment count to the Disk File Control. A Read Check is initiated and a result descriptor is returned to the system. The Read Check operation in the Disk File Control continues independently from the I/O Control unit. Termination of a Read Check is indicated by a Read Check Finished Interrupt (CCI15F set).

An Interrogate operation causes no reading or writing on any disk. This operation transfers a disk address word and returns a result descriptor with appropriate indications about this address. Any disk file operation checks the prior operation for a parity error (D23F). A non-existent disk address (EU Not Ready) and a write lockout check is made with each Write Interrogate operation. A Read Interrogate only checks for a non-existent address as well as the normal parity error check on the prior disk operation.

B5500 DISK FILE I/O DESCRIPTOR

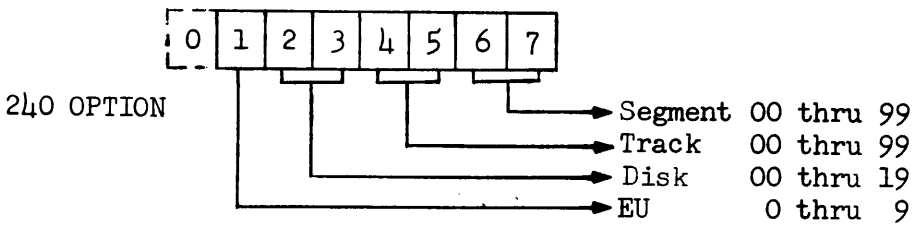
The Disk File I/O descriptor can specify one of four I/O operations, Disk File Read, Disk File Write, Read Check or Interrogate.



WC=0	Interrogate operation	014000 010 00 Maaaa
WC=0	Read operation - 770 Segs.	014000 004 77 Maaaa
WC=0	Write operation - 770 Segs.	014000 000 77 Maaaa
WC≠0	Read operation - 17770 Words	015777 014 00 Maaaa
WC≠0	Write operation - 17770 Words	015777 010 00 Maaaa
	Read check	014000 104 77 Maaaa

D48 = 1	Flag ON for descriptor
D47 = 0	Always OFF for descriptor
D46 = 1	Presence bit
D45 thru D41	Unit designate BCD 06 or 14ø for D.F.C.U. #1 DCD 12 or 30ø for D.F.C.U. #2
D40 thru D31	Word Count
D30 = 1	Read Check
= 0	for Read, Write, or Interrogate
D27 = 0	Alphanumeric Information
= 1	Binary Information
D25 = 1	Word Count Usage
D24 = 1	Read Operation
= 0	Write Operation
D21 thru D16	Number of Segments (00-77 octal segments)
D15 thru D1	Core Memory Address Note: The last seven (7) characters of first word contains the Disk File Address.

Disk Address



DESCRIPTOR COMBINATIONS

40 - 31 WORD COUNT	30	27	25	24	21 - 16 SEGMENT COUNT "n"	OPERATION
	1				$1 \leq n \leq 77\emptyset$	READ CHECK
		0	0	1	$1 \leq n \leq 77\emptyset$	Read with BCL translation; ignore Word Count
		1	0	1	$1 \leq n \leq 77\emptyset$	Read without translation (Binary); ignore Word Count
$1 \leq WC \leq 1777\emptyset$		0	1	1	$1 \leq n \leq 77\emptyset$	Read with BCL translation; Word Count Override
$1 \leq WC \leq 1777\emptyset$		1	1	1	$1 \leq n \leq 77\emptyset$	Read without translation; Word Count Override
		0	0	0	$1 \leq n \leq 77\emptyset$	Write with BCL translation; ignore Word Count
		1	0	0	$1 \leq n \leq 77\emptyset$	Write without translation; ignore Word Count
$1 \leq WC \leq 1777\emptyset$		0	1	0	$1 \leq n \leq 77\emptyset$	Write with BCL translation; Word Count Override
$1 \leq WC \leq 1777\emptyset$		1	1	0	$1 \leq n \leq 77\emptyset$	Write without translation; Word Count Override
WC - 0			1			Interrogate (Samples SC=00; 01; 02; 03)

NOTE: The "0" and "1" are required where shown, and blanks are irrelevant.

DISK FILE RESULT DESCRIPTOR

	45							24	21	18	15				
		41						23	20						
		40			31			22	19	16					1

48 ➡ 46 = 0

45 ➡ 41 = Unit Designate

BCD 6 = DFCU 1
or 14ø

BCD 12 = DFCU 2
or 30ø

40 ➡ 31 = Remaining Word Count

24 = 1 if Operation was Read, 0 if Operation was Write

23 = 1 if Disk information parity error on prior Read Check operation

22 = 1 for Core Memory Address Error

D21 = 1 if Disk File Electronics Unit goes Not Ready because of a non-existent address being encountered on the disk during a Read or Write operation. D21F is also set if the initial address in the DFCU attempts to access a non-existent disk address.

20 = 1 if PARITY ERROR on transfer of data from Disk to I/O during Read Operation

19 = 1 if Core Memory Parity Error; Parity Error during Disk File Address Transfer, or Data Transfer during Write Operation, to DFCU.

18 = 1 if DFCU NOT READY

16 = 1 if DFCU is busy with another I/O channel

15 ➡ 1 = last address accessed + 1 for all Read/Write Operations or initial address + 1 for Read Check and Interrogate Operations.

GLOSSARY OF TERMS

SIGNAL LINES TO DISK FILE CONTROL

FASL — File Address Select Level: This level going true notifies the Disk File Control the I/O control wishes to transfer a disk address. The first FDTL that finds FASL true causes the Disk Control to leave its Idle State and enter SC = 04.

FBIL — File Binary Information Level: FBIL is always true during an address transfer. FBIL follows D27F for the information transfer.

FDTL/ — File Data Transfer Level: FDTL/ goes false to produce a clock pulse in the Disk Control.

FWIL/ — File Write Information Level Not (1 through P): The FWIL lines reflect the status of each character in the OBnF's.

FWRL/ File Write Level Not: This level going false causes information to be written on the disk.

SIDL System Identification Level: SIDL always remains true when a B5500 is connected to a Disk File Control Unit.

SIGNAL LINES FROM DISK FILE CONTROL

FCBL/ File Control Busy Level Not: This level goes false to notify the I/O control that the Disk File Control has accepted the disk address and has begun an address search.

FCLP File Clock Pulse: This clock pulse is generated in the Disk Control. During a Read operation, FCLP's notifies the I/O logics to accept the character on the File Read Lines. During a Write operation, FCLP's causes the I/O logics to place a new character in the OBnF's.

FCRL File Control Ready Level: This level is true when D.C. power is on in the Disk File Control Unit.

FERL/ File Error Level Not: FERL goes false when the Disk Control detects a parity error on information received from I/O Control.

FINP/ File Interrupt Pulse Not: FINP/ goes false when the Disk File Control has finished a Read Check Operation, and causes CCI15F to be set in central control.

FOCL File Operation Complete Level:

FSRL/ File Storage Ready Level Not: This level goes false when the Sequence Counter in the Disk File Control Unit is idling at SC=03. The level being false causes D21F to be set in the result descriptor. The address just transferred is now flagged as not being available for reading or writing.

FWCL/ File Word Coincidence Level Not: This level goes false during active word time on the disk.

FWLL/ File Write Lockout Not: This level goes false when the Disk File Control Unit idles at SC=02. D20F is set in the result descriptor to flag the address just transferred to the Disk File Control Unit as being mechanically locked out for write operations.

B5500 DISK FILE OPERATION

Sequence counts 01, 02 and 03 are used as normal to obtain the I/O descriptor from memory. The Longitudinal Parity Flip-flops contain the number of segments to be read or written. The Sequence counts are shown in Figure 7-1.

SC = 3 Condition logics for a memory read cycle; set EXNF exit to SC = 9.

SC = 9 Request a memory access for the disk file address.

SC = 10 EXNF being on causes the logics to exit to SC = 04.

SC = 4 Transfer a disk address for all disk operations. The logics stays at SC = 4 until the disk control returns FCBL. At this time, D17F is set and the logics may exit to SC = 8, SC = 9 or SC = 14.

SC = 8 Read: Each File Clock Pulse sets STRF and a character is read from the File Read lines provided File Word Coincidence level is true from the Disk File Control. After eight characters have been read the logics proceed to SC = 9 to execute a memory write cycle. The Read operation has been completed when the Disk File Control Unit returns to its Idle condition FCBL/ and Word coincidence is false (I23S/ true).

SC = 8 Write: Each File Clock Pulse again sets STRF and a new character is placed into the OBnF. Each FCLP notifies the I/O control logics that the prior character in the OBnF's has been written on disk and the next character is being requested. The logics proceeds to SC = 9 when all the characters in the W-register have been written on disk. The write operation is terminated when EXNF is set by I22S/ and I23S/ both becoming true.

SC = 14 The result descriptor is formed after the Read or Write operation has been completed.

SC = 15 The result descriptor is stored in memory and the I/O is cleared.

SEQUENCE COUNT EQUALS THREE

LPPF to 1

I28D is true when the Disk File Control Sequence Count is at SC=01. When a parity error is detected during any read or read check operation SC4F is set in the DFCU. SC4F is transferred to SC1F when the DFCU has completed the operation.

SC to 14

Normally D16F and D18F are both on to prevent the SC from being set to 14.

Wr and IB to ZERO

If the character counter is counted to 5 and this operation is not a drum operation (DROS/), the I/O descriptor in the W-register is cleared.

PROD

The original contents of D24, D25 and D27 are transferred to D20, D21 and D17 respectively for temporary storage. D24, D25 and D27 are used as logical flip-flops during an address transfer. D27F is used to make the binary level true for all address transfers. D25F is cleared to prevent the word counter from being counted when the disk file address is accessed at SC=9. D24F is reset to prevent the disk file address in the W-register from being cleared when MAOF is set. D24F being on specifies a write operation into memory and the logics would normally clear the W-register. During an address access the disk file address must be retained in the W-register until it has been transferred to the disk file control.

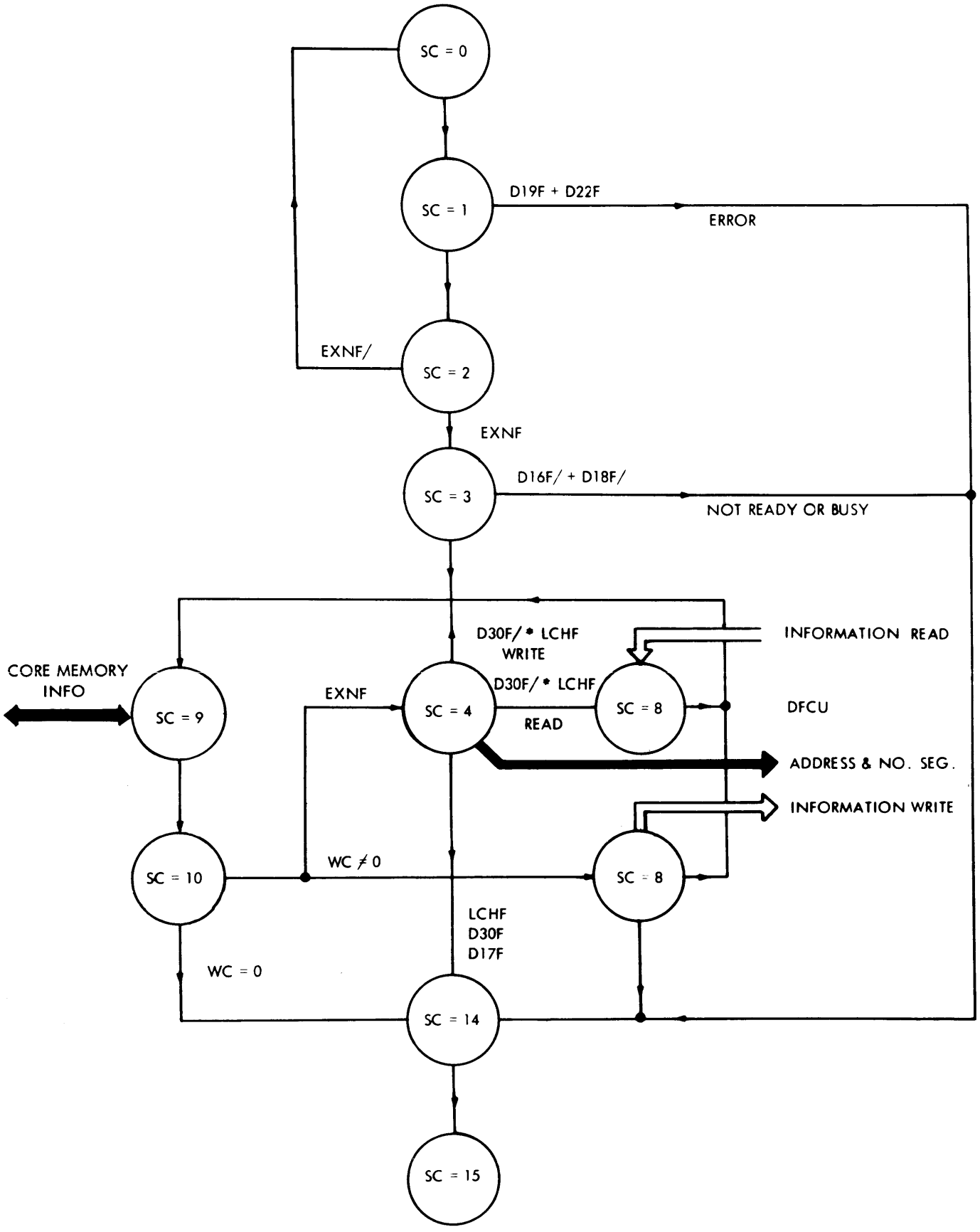


FIGURE 7-1 DISC FILE SEQUENCE COUNT FLOW CHART

EXNF is set here and used as a logical flip-flop at SC=10 to force an exit to SC=4. EXNF is also used at SC=10 to restore the original setting of D24 and D25. Error bits D20 and D21 are cleared for error flags.

If this is an interrogate operation (D25F on and WC=0) unconditionally set D30F. After the address has been transferred at SC=4, the logics exits to SC=14 with D30F, D17F and LCHF set.

A Read check operation is performed with D30F on. D27F is cleared to make FBIL false upon initial entrance to SC=4. This logics allows RCKF to be set in the DFCU.

SEQUENCE COUNT EQUALS NINE

Wr to 0

The first clock pulse at SC=9 clears the W-register with D24F/, MANF/ and MAPS.

MANF to 1

Memory Access Flip-flop is set with the first clock pulse because D25F was reset at SC=4. AOFF/ would normally be true at the first memory access.

MAOF to 1

MT2D-M (Memory times two Driver) originates in memory when the Memory Pulse Counter is equal to one. When using the six microsecond memory MT2D becomes true when Memory Pulse Counter is equal to two. Memory Information Register (MIR) is set just prior to the clock pulse that sets MAOF. Due to the length of cabling the outputs of the MIR register cannot reliably be gated into the W-register with this system clock.

MIR to W 48 thru 1

The output of the Memory Information Strobe Driver (MISD) is true when MAOF and MANF are both set. This logics allows the outputs of the MIR register one microsecond to stabilize before being gated into the W-register in I/O.

SC+1

The Sequence Counter is advanced to SC=10 as the W-register is filled with the Disk File Address (MANF * MAOF).

WC-1

The Word Counter is prevented from counting down with the first memory access because D25F was reset at SC=3.

Wr to 0

The W-register cannot be cleared with MAOF set because D24F was unconditionally cleared at SC=03.

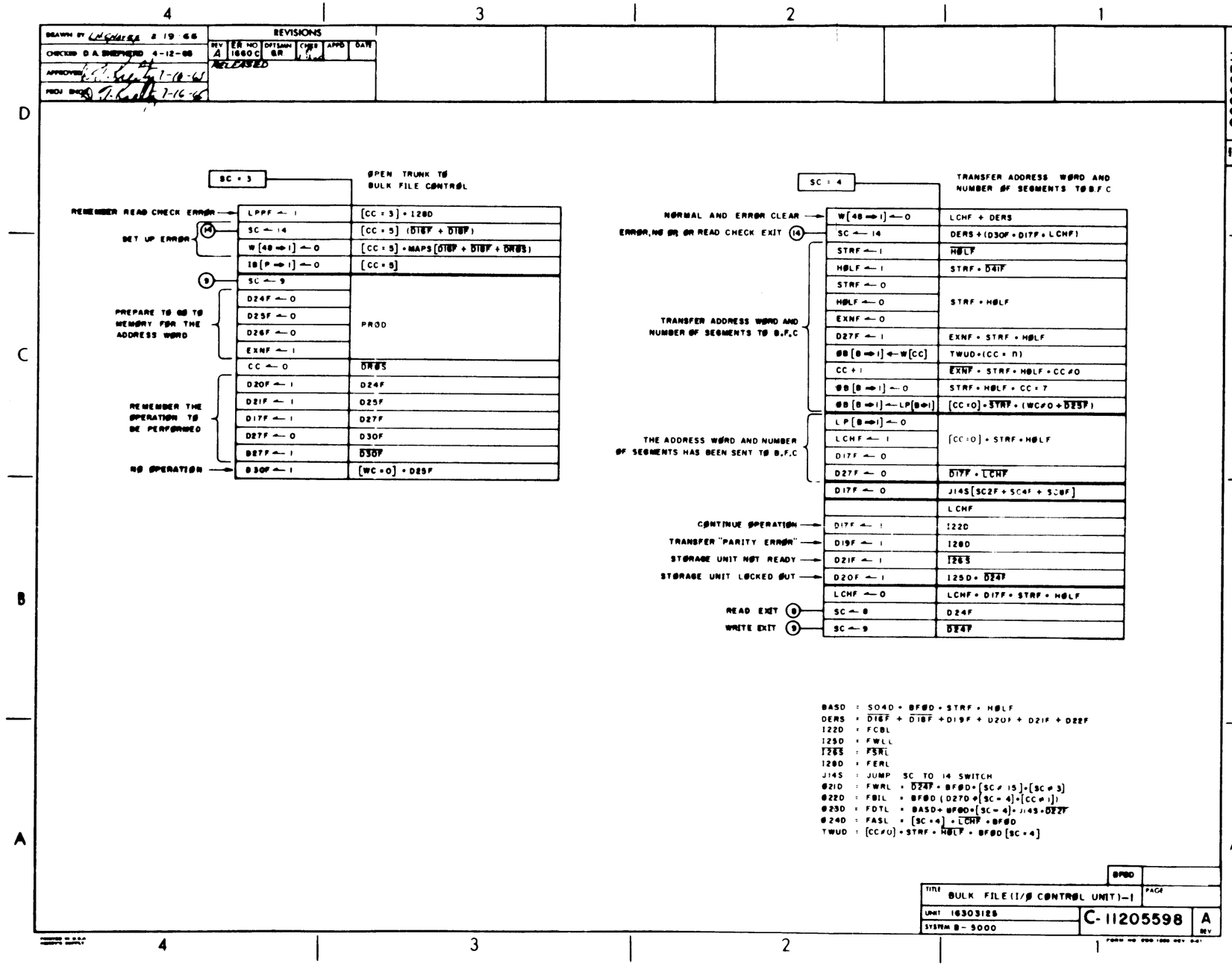

REVISIONS
REV A ER NO 1660 C DIT/MAN GR CHKD APPD DATE
RELEASED
C-11205598 A
SC = 3
OPEN TRUNK TO BULK FILE CONTROL
REMEMBER READ CHECK ERROR
SET UP ERROR
PREPARE TO GO TO MEMORY FOR THE ADDRESS WORD
REMEMBER THE OPERATION TO BE PERFORMED
NO OPERATION
LPPF ← 1
SC ← 14
W[48 ⇒ 1] ← 0
IB[P ⇒ 1] ← 0
SC ← 9
D24F ← 0
D25F ← 0
D26F ← 0
EXNF ← 1
CC ← 0
D20F ← 1
D21F ← 1
D17F ← 1
D27F ← 0
D22F ← 1
D30F ← 1
[CC = 3] • 1280
[CC = 5] (D16F + D18F)
[CC = 5] • MAPS[D16F + D18F + DNØS)
[CC = 9]
PRØD
DNØS
D24F
D25F
D27F
D30F
[WC = 0] • D25F
SC = 4
TRANSFER ADDRESS WØRD AND NUMBER ØF SEGMENTS TØ B,F,C
NORMAL AND ERROR CLEAR
ERROR, NO ER ØR READ CHECK EXIT
TRANSFER ADDRESS WØRD AND NUMBER ØF SEGMENTS TØ B,F,C
THE ADDRESS WØRD AND NUMBER ØF SEGMENTS HAS BEEN SENT TØ B,F,C
CONTINUE ØPERATION
TRANSFER "PARITY ERRØR"
STØRAGE UNIT NØT READY
STØRAGE UNIT LØCKED ØUT
READ EXIT
WRITE EXIT
W[48 ⇒ 1] ← 0
SC ← 14
STRF ← 1
HØLF ← 1
STRF ← 0
HØLF ← 0
EXNF ← 0
D27F ← 1
ØB[8 ⇒ 1] ← W[CC]
CC ← 1
ØB[8 ⇒ 1] ← 0
ØB[8 ⇒ 1] ← LP[8⇒1]
LP[8⇒1] ← 0
LCHF ← 1
D17F ← 0
D27F ← 0
D17F ← 0
D17F ← 1
D19F ← 1
D21F ← 1
D20F ← 1
LCHF ← 0
SC ← 8
SC ← 9
LCHF + DERS
DERS + (D30F • D17F • LCHF)
HØLF
STRF • D41F
STRF • HØLF
EXNF • STRF • HØLF
TWUD • (CC = 11)
EXNF • STRF • HØLF • CC ≠ 0
STRF • HØLF • CC = 7
[CC = 0] • STRF • (WC ≠ 0 + D25F)
[CC = 0] • STRF • HØLF
D17F • LCHF
J14S[SC2F + SC4F + SC8F]
LCHF
1220
1280
1265
1250 • D24F
LCHF • D17F • STRF • HØLF
D24F
D24F
BASD = SO4D • BFØD • STRF • HØLF
DERS = D16F + D18F + D19F + D20F + D21F + D22F
1220 = FCBL
1250 = FWLL
1265 = FSRL
1280 = FERL
J14S = JUMP SC TO 14 SWITCH
Ø21D = FWRL • D24F • BFØD • [SC ≠ 15] • [SC ≠ 3]
Ø22D = FBIL • BFØD (D27D ⇒ [SC = 4] • [CC ≠ 1])
Ø23D = FDTL • BASD • BFØD • [SC = 4] • J14S • D22F
Ø24D = FASL = [SC = 4] • LCHF • BFØD
TWUD = [CC ≠ 0] • STRF • HØLF • BFØD [SC = 4]
BFØD
BULK FILE (I/Ø CONTRØL UNIT)-1
UNIT 16303125
SYSTEM B-5000
C-11205598 A REV

FIGURE 7-2

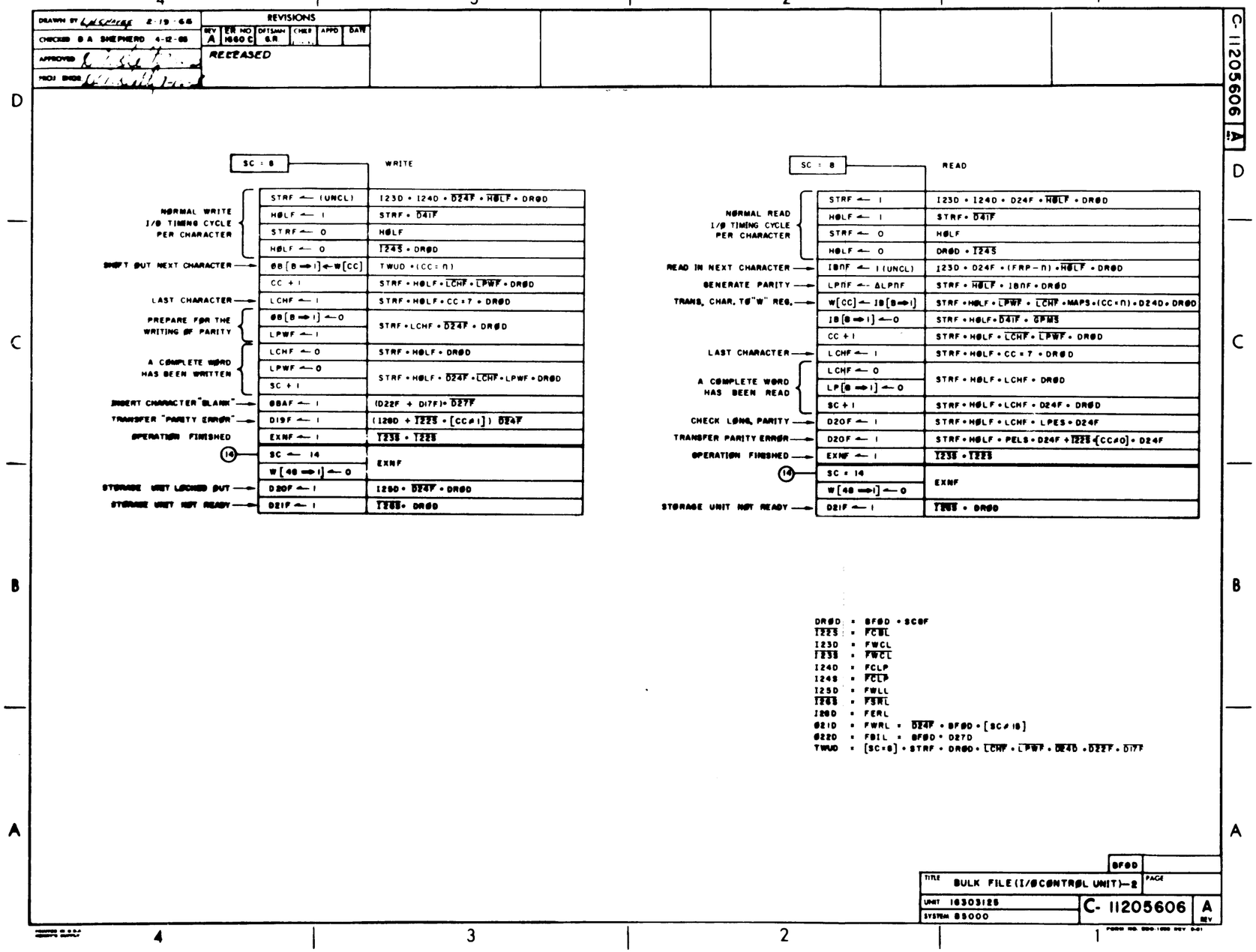

DRAWN BY L.A. SCHRADE 2-19-68
CHECKED B.A. SHEPHERD 4-12-68
APPROVED
PROJ. ENGR.
REVISIONS
REV A | ER NO 1660 C | DFTSMAN G.R. | CHIEF | APPD | DATE
RELEASED
C-11205606 A
SC = 8
WRITE
NORMAL WRITE I/O TIMING CYCLE PER CHARACTER
SHIFT OUT NEXT CHARACTER
LAST CHARACTER
PREPARE FOR THE WRITING OF PARITY
A COMPLETE WORD HAS BEEN WRITTEN
INSERT CHARACTER "BLANK"
TRANSFER "PARITY ERROR"
OPERATION FINISHED
STORAGE UNIT LOCKED OUT
STORAGE UNIT NOT READY
STRF ← (UNCL) | I23D • I24D • D24F • HØLF • DRØD
HØLF ← 1 | STRF • D41F
STRF ← 0 | HØLF
HØLF ← 0 | I24S • DRØD
ØB[8 ⇒ 1] ← W[CC] | TWUD • (CC = Ø)
CC + 1 | STRF • HØLF • LCHF • LPWF • DRØD
LCHF ← 1 | STRF • HØLF • CC = 7 • DRØD
ØB[8 ⇒ 1] ← 0 | STRF • LCHF • D24F • DRØD
LPWF ← 1
LCHF ← 0 | STRF • HØLF • DRØD
LPWF ← 0 | STRF • HØLF • D24F • LCHF • LPWF • DRØD
SC + 1
ØBAF ← 1 | (D22F + D17F) • D27F
D19F ← 1 | (I28D + I22S • [CC≠1]) D24F
EXNF ← 1 | I23S • I22S
14 SC ← 14 | EXNF
W[48 ⇒ 1] ← 0
D20F ← 1 | I28D • D24F • DRØD
D21F ← 1 | I28S • DRØD
SC = 8
READ
NORMAL READ I/O TIMING CYCLE PER CHARACTER
READ IN NEXT CHARACTER
GENERATE PARITY
TRANS. CHAR. TØ "W" REG.
LAST CHARACTER
A COMPLETE WORD HAS BEEN READ
CHECK LONG. PARITY
TRANSFER PARITY ERRØR
OPERATION FINISHED
STORAGE UNIT NOT READY
STRF ← 1 | I23D • I24D • D24F • HØLF • DRØD
HØLF ← 1 | STRF • D41F
STRF ← 0 | HØLF
HØLF ← 0 | DRØD • I24S
IBNF ← 1 (UNCL) | I23D • D24F • (FRP − Ø) • HØLF • DRØD
LPNF ← ΔLPNF | STRF • HØLF • IBNF • DRØD
W[CC] ← IB[8 ⇒ 1] | STRF • HØLF • LPWF • LCHF • MAPS • (CC ≠ Ø) • D24D • DRØD
IB[8 ⇒ 1] ← 0 | STRF • HØLF • D41F • GPMS
CC + 1 | STRF • HØLF • LCHF • LPWF • DRØD
LCHF ← 1 | STRF • HØLF • CC = 7 • DRØD
LCHF ← 0 | STRF • HØLF • LCHF • DRØD
LP[8 ⇒ 1] ← 0
SC + 1 | STRF • HØLF • LCHF • D24F • DRØD
D20F ← 1 | STRF • HØLF • LCHF • LPES • D24F
D20F ← 1 | STRF • HØLF • PELS • D24F + I22S • (CC≠Ø) • D24F
EXNF ← 1 | I23S • I22S
SC = 14
W[48 ⇒ 1] ← 0 | EXNF
D21F ← 1 | I28S • DRØD
DRØD = ØFØD • SCØF
I22S = FCBL
I23D = FWCL
I23S = FWCL
I24D = FCLP
I24S = FCLP
I25D = FWLL
I25S = FSWL
I28D = FERL
ØZ1D = FWRL = D24F • ØFØD • [SC≠18]
ØZ2D = FØIL = ØFØD • D27D
TWUD = [SC=8] • STRF • DRØD • LCHF • LPWF • D24D • D22F • D17F
ØFØD
TITLE BULK FILE (I/O CONTROL UNIT)—2
PAGE
UNIT 16303128
SYSTEM B5000
C-11205606 A
REV

FIGURE 7-3

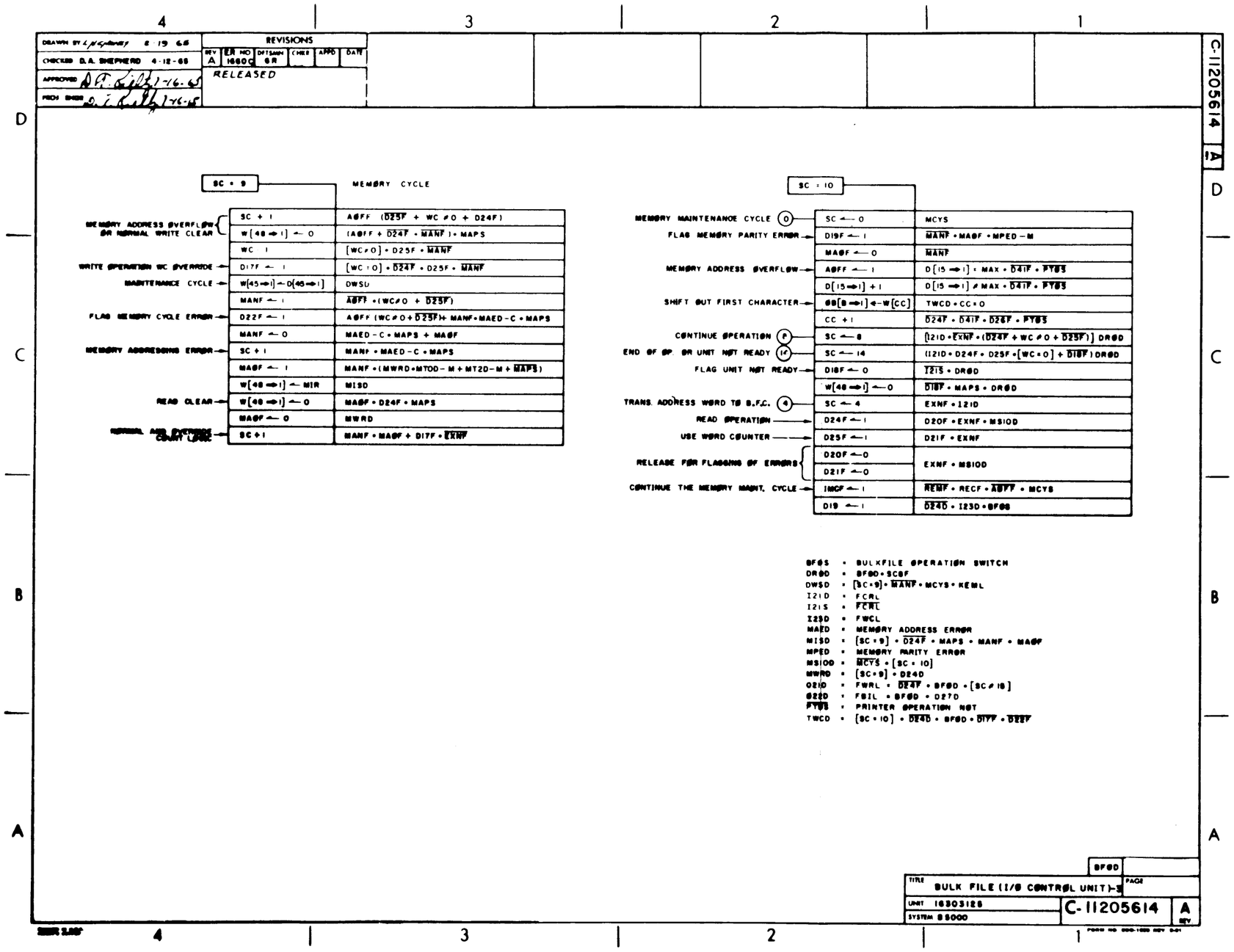

C-11205614 A
REVISIONS
REV A ER NO 16600 DPTSMN GR CHKR APPD DATE
RELEASED
SC + 9
MEMORY CYCLE
SC + 1 A0FF (D25F + WC ≠ 0 + D24F)
MEMORY ADDRESS OVERFLOW OR NORMAL WRITE CLEAR
W[48 ⇒ 1] ← 0 (A0FF + D24F · MANF) · MAPS
WC 1 [WC ≠ 0] · D25F · MANF
WRITE OPERATION WC OVERRIDE D17F ← 1 [WC = 0] · D24F · D25F · MANF
MAINTENANCE CYCLE W[45 ⇒ 1] ← D[46 ⇒ 1] DWSD
MANF ← 1 A0FF · (WC ≠ 0 + D25F)
FLAG MEMORY CYCLE ERROR D22F ← 1 A0FF (WC ≠ 0 + D25F) + MANF · MAED-C · MAPS
MANF ← 0 MAED-C · MAPS + MA0F
MEMORY ADDRESSING ERROR SC + 1 MANF · MAED-C · MAPS
MA0F ← 1 MANF · (MWRD · MTOD-M + MT2D-M + MAPS)
W[48 ⇒ 1] ← MIR MISD
READ CLEAR W[48 ⇒ 1] ← 0 MA0F · D24F · MAPS
MA0F ← 0 MWRD
NORMAL ADD. EXTENSION COUNT USAGE SC + 1 MANF · MA0F + D17F · EXNF
SC + 10
MEMORY MAINTENANCE CYCLE (0) SC ← 0 MCYS
FLAG MEMORY PARITY ERROR D19F ← 1 MANF · MA0F · MPED − M
MA0F ← 0 MANF
MEMORY ADDRESS OVERFLOW A0FF ← 1 D[15 ⇒ 1] = MAX · D41F · FYBS
D[15 ⇒ 1] + 1 D[15 ⇒ 1] ≠ MAX · D41F · FYBS
SHIFT OUT FIRST CHARACTER 00[8 ⇒ 1] ← W[CC] TWCD · CC = 0
CC + 1 D24F · D41F · D26F · FYBS
CONTINUE OPERATION (P) SC ← 8 (I21D · EXNF · (D24F + WC ≠ 0 + D25F)] DR0D
END OF OP. OR UNIT NOT READY (14) SC ← 14 (I21D · D24F · D25F · [WC = 0] + D18F) DR0D
FLAG UNIT NOT READY D18F ← 0 I21S · DR0D
W[48 ⇒ 1] ← 0 D18F · MAPS · DR0D
TRANS. ADDRESS WORD TO B.F.C. (4) SC ← 4 EXNF · I21D
READ OPERATION D24F ← 1 D20F · EXNF · MSI0D
USE WORD COUNTER D25F ← 1 D21F · EXNF
RELEASE FOR FLAGGING OF ERRORS D20F ← 0 EXNF · MSI0D
D21F ← 0
CONTINUE THE MEMORY MAINT. CYCLE I18CF ← 1 NEMF · RECF · A0FF · MCYS
D19 ← 1 D24D · I23D · BF0S
BF0S = BULKFILE OPERATION SWITCH
DR0D = BF0D · SC0F
DW5D = [SC = 9] · MANF · MCYS · KEML
I21D = FCRL
I21S = FCRL
I23D = FWCL
MAED = MEMORY ADDRESS ERROR
MISD = [SC = 9] · D24F · MAPS · MANF · MA0F
MPED = MEMORY PARITY ERROR
MSI0D = MCYS · [SC = 10]
MWRD = [SC = 9] · D24D
O2ID = FWRL · D24F · BF0D · [SC ≠ 18]
O2ED = FBIL · BF0D · D27D
FYBS = PRINTER OPERATION NOT
TWCD = [SC = 10] · D24D · BF0D · D17F · D22F
BF0D
TITLE BULK FILE (I/O CONTROL UNIT)-B
PAGE
UNIT 1830128
SYSTEM B5000
C-11205614 A REV

FIGURE 7-4

D17F to 1

D17F is used as a logical flip-flop to provide an exit to SC=10 when Word Count override logics is used. MANF would be prevented from being set when the Word Counter is equal to zero (WC=0) and D25F is on. D25F being on specifies the word counter is to be used. D17F is set with the first clock pulse at SC=9 that found WC=0 * D24F/ * D25F * MANF/.

SC+1

The next clock pulse that finds D17F set and EXNF reset would advance the Sequence Counter to ten.

SEQUENCE COUNTER EQUAL TO TEN

MAOF to 0

The first clock pulse at SC=10 unconditionally clears MAOF.

D 15 thru 1 plus 1

When the D-register memory address portion is not maximum (NOT 77777), the level D15F thru D01F ≠ MAX is true. D41F/ specifies the I/O is not performing a magnetic tape operation. PTOS/ being true specifies also a printer operation is not being performed.

W[CC] to OB[B thru 1]

The term W[CC] specifies the character in the W-register pointed to by the Character Counter is to be gated into the Output Buffer. The outputs of the OBnF are gated into a parity generation circuit. The Parity Driver output provides the proper parity for each character transmitted to the Disk File Control. TWCD (Transfer W-register Clocked Driver) is a level that gates the clocked input to the OBnF.

TWCD = SC=10 * D24D/ * BFOD * D17F/ * D22F/

D24F was cleared at SC=3. D17F is normally found reset except during a write operation when word count override becomes effective. D22F is not set unless an address overflow or memory address error has been detected.

CC+1

The Character Counter is advanced plus one because D24F was cleared at SC=3. The logics is performing a normal Write Operation on the Disk File address.

SC to 4

The Sequence Counter is set to four if the Disk File control unit is ready (I21D) and EXNF set. EXNF was set at SC=3 to provide an exit to SC=4 when the logics passes through SC=10 the first time. EXNF being set prevented the normal exit to SC=8.

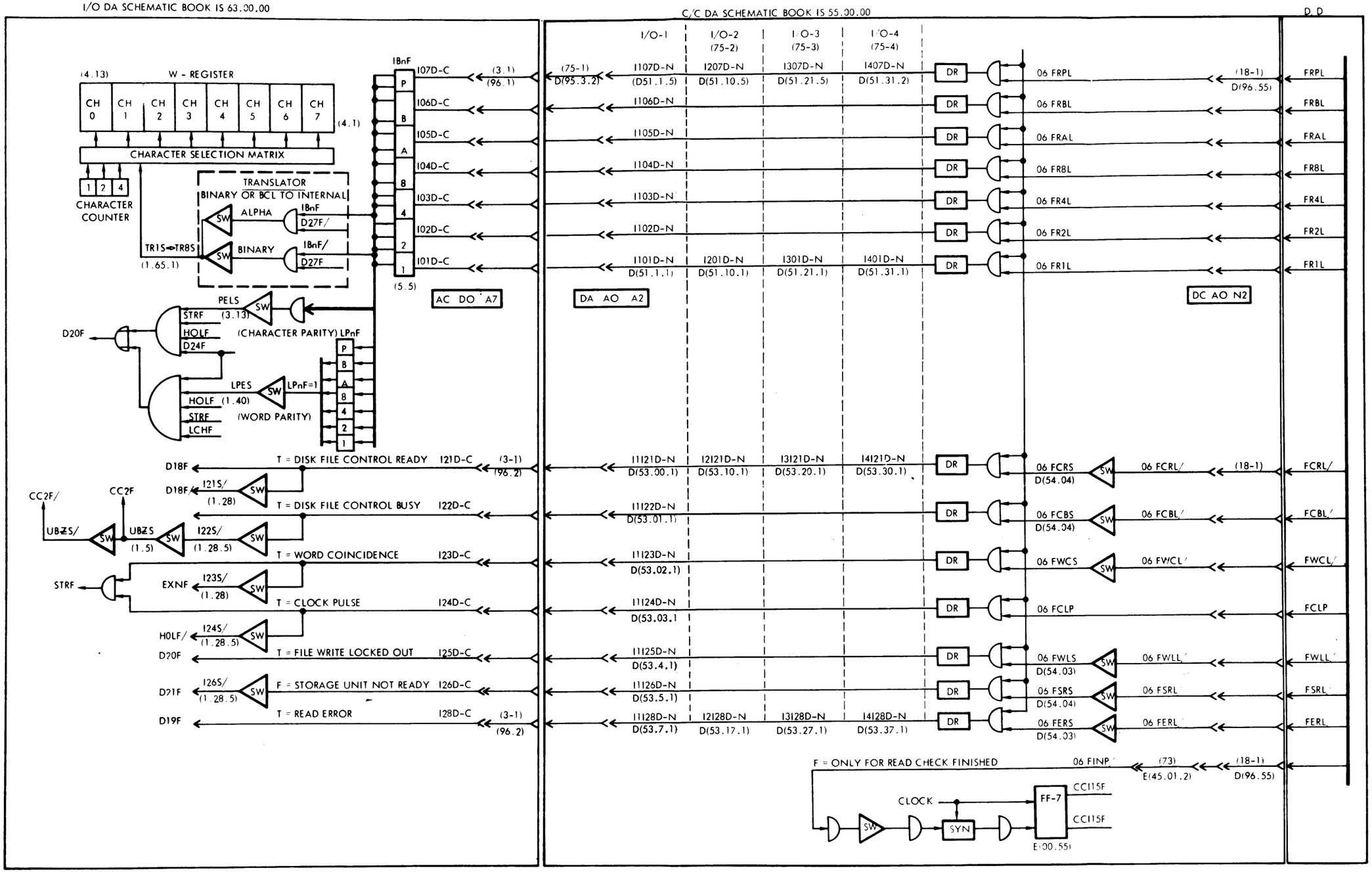


FIGURE 7-5 B 5500 MODEL III DISK FILE CONTROL INPUT SIGNAL

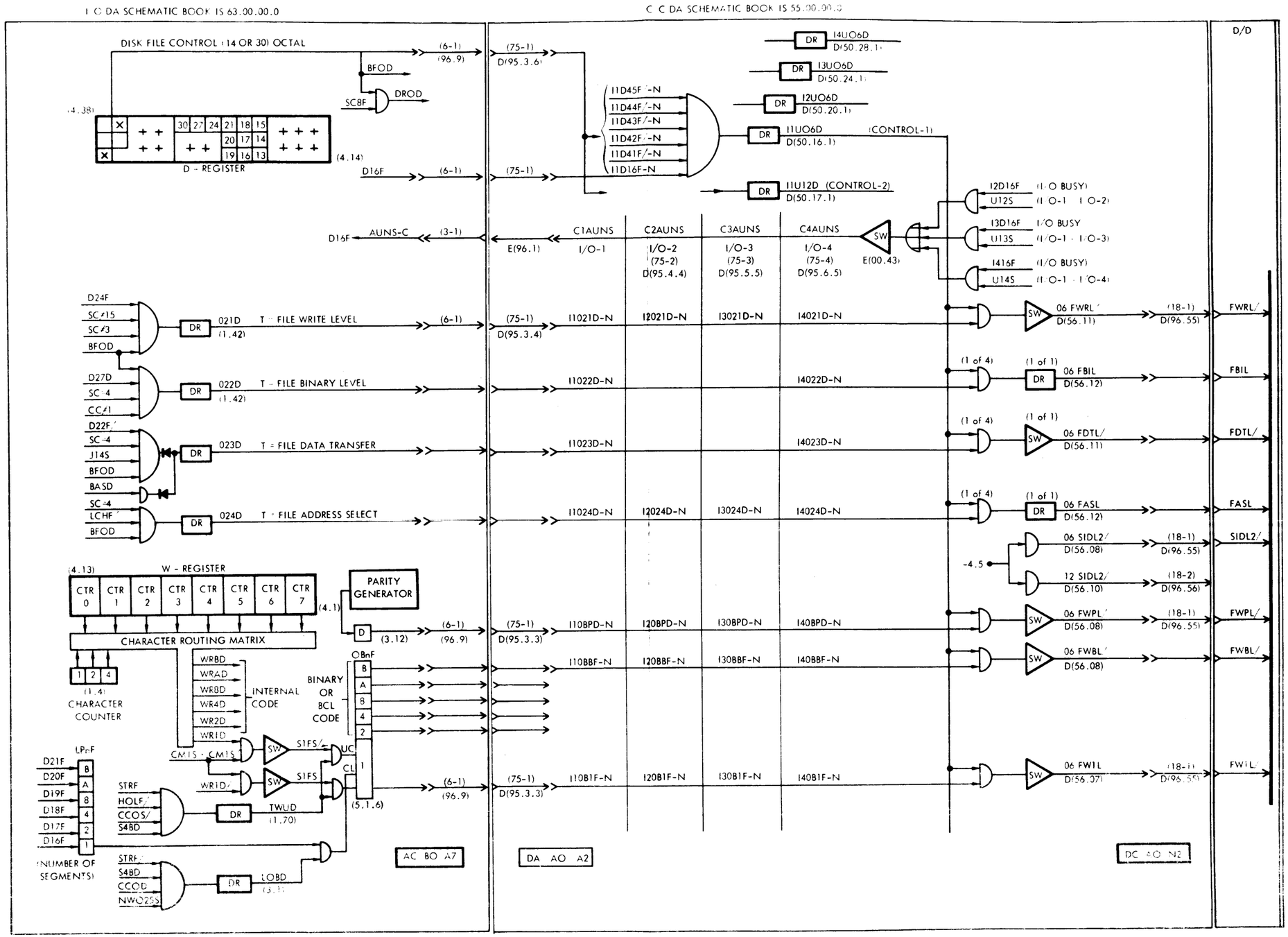


FIGURE 7-6 B 5500 MODEL III DISK FILE CONTROL OUTPUT SIGNALS

D24F and D25 to 1

The original setting of D24F and D25 was temporarily stored in D20F and D21F respectively. With EXNF on, D24 and D25 are restored to their original values in the I/O descriptor.

D20F and D21F to 0

These flip-flops in the error field are cleared to restore them for error flagging.

D19F to 1

This error flip-flop would normally be set in an active Read or Write Operation when I/O exchange required more than thirty-two microseconds for a memory access.

SC to 8

EXNF being set inhibits an exit to SC=8 when I21D is found true.

D18F to 0

If the Disk File Control Unit is found not ready (I21S/ true), D18F is reset with I21S/ * DROD. A large portion of the drum logics is used with the Bulk File Operation (BFOD).

SC to 14 and Wr to 0

The next clock pulse that finds D18F reset causes the W-register to be cleared and the logics to exit to SC=14. At SC=14, a result descriptor would be developed indicating the Disk File Control was found Not Ready. DROD (Drum Operation Driver) is brought true during a Disk File operation.

SEQUENCE COUNT EQUAL TO FOUR

Wr to 0

The W-register is cleared at the end of an address transfer (LCHF set) for a Disk File Read, Read Check, Write or Interrogate. DERS (D-register Error field) is true if either D16F, D18F, D19F, D20F, D21F or D22F becomes set. The W-register is cleared to prepare for developing the result descriptor.

SC to 14

Any disk file operation would be terminated if a parity error was detected by the Disk File Control Unit during an address transfer. The Disk File Control would return to its own Sequence Count of one and cause D19F to be set. DERS now becomes a true level. Also, the Disk File address sent to the control unit may address a non-existent module. The Electronics Unit would go Not Ready and the Control Unit forces its Sequence Counter to three. I26S/ is made true to set D21F. DERS again becomes true.

The disk address passed to the control unit during a Write Operation may address a portion of disk memory that is Write Locked Out. When this happens, the control unit forces its Sequence Counter to two. I25D becomes true in I/O and causes D20F to be on in the result descriptor. Again, DERS becomes a true level.

ADDRESS TRANSFER TO DISK FILE CONTROL

SEQUENCE COUNT EQUAL TO FOUR

STRF to 1

The first clock pulse at SC=4 that finds HOLF/ sets STRF.

HOLF to 1

HOLF is set with the next system clock that finds STRF set.

STRF, HOLF, EXNF to 0

STRF and HOLF being set clears HOLF, STRF and EXNF.

D27F to 1 (effective for Read Check Only)

The clock pulse that found HOLF, STRF and EXNF set would unconditionally set D27F if D27F had not already been set at SC=3. D27F is used in developing File Binary Level (FBIL). FBIL/ and File Address Select Level (FASL) are used together to set the Read Check Flip-flop in the Disk Control Unit. A Read Check (D30F on) would have prevented D27F from being set at SC=4, D27F would have been found reset and therefore causes FBIL to be false.

FBIL = BFOD (D27D + SC=4 * CC ≠ 1)

FBIL being false for one clock pulse (D27F/) and FASL true at initial entry to SC=4 causes RCKF in the Disk File Control to be set.

W[CC] to OBnF

Transfer from W-register to OBnF Unclocked becomes a true level when STRF is initially set. The first character loaded into OBnF at SC=10 is now overwritten with the second character (CC=1) in the address word. The first STRF * HOLF combination finds EXNF set and prevents the counting of the character counter.

CC+1 = EXNF/ * STRF * HOLF * CC≠0

EXNF is reset with the first STRF * HOLF level and leaves CC=1. The second setting of STRF causes the second character in the W-register to again be transferred into OBnF. The I/O logics initially found the Disk File control at its SC=00 (IDLE).

FASL and a File Data Transfer Level (FDTL) causes the Disk File Control unit to leave its IDLE condition and go to its SC=04. The Disk File Control Unit is now prepared to receive the address word. The I/O logics transferred the second character in the W-register to the Disk File Control as the Disk Control entered SC=04. The Disk Control Unit could not have received the first character. EXNF

being on with the first STRF * HOLF combination prevented the character counter from being counted. EXNF is reset at this time. The next STRF * HOLF combination finds the character counter pointing to character position one and the first address digit is reloaded into the OBnF. A File Data Transfer first address digit is reloaded into the OBnF. A File Data Transfer Level (FDTL) is produced to gate this digit into the B470 Control Unit.

OBnF to 0

The last address digit has been transferred when the character counter is pointing to character position seven. A STRF * HOLF combination occurs and the character counter is counted from seven to zero.

OB[B => 1] LP[B => 1]

The number of segments were placed into the Longitudinal Parity Flip-flops for temporary storage. The seventh disk address has been transferred when the character counter is counted from 7 to zero. At this time, the segment number is placed into the OBnF.

LP[B thru 1] to OB[B thru 1] = CC=0 * STRF/ * WC≠0 + D25F/)

Only the interrogate operation (WC=0 * D25F) inhibits the transfer of LPnF to OBnF.

LP[B => 1] to 0; LCHF to 1; D17F to zero

The character counter being counted from seven to zero specifies the address transfer has been completed. The next STRF * HOLF combination occurs after the segment number has been transferred. Last Character Flip-flop (LCHF) is set to clear the W-register and to restore D27F and D17F to their original setting at SC=03. D17F must be cleared to allow the sensing of FCBL from the Disk File Control Unit.

D17F to 1

LCHF remains set for approximately 600 μs waiting for DCPM in the Disk File Control Unit to time out. After DCPM times I22D (FCBL) becomes true and sets D17F with the next I/O clock pulse.

D19F to 1

A parity error being detected by the Disk File Control on an address transfer causes the DFCU Sequence Counter to an IDLE state with SC=01. I28D becomes true and D19F is set. DERS becomes true and the next clock pulse forces the Sequence Counter to 14 and D17F is cleared.

D21F to 1

Each address transferred is decoded in the DFEU. The selected Disk File Electronics Unit goes Not Ready if a non-existent disk is being addressed. The Sequence Counter in the DFCU returns to SC=03. FSRL/ becomes false and causes I26S/ to become true. D21F is set with the next I/O clock pulse. DERS becomes true to force the logics to exit to SC=14.

D20F to 1

The Disk File address transferred during a Write operation may select a disk where a Write Lockout Switch is thrown to prevent writing. A FWLL is returned to the DFCU by the DFEU. The Sequence Counter in the DFCU returns to SC=02. I25D becomes true in the I/O and D20F is set with the next I/O clock pulse. DERS forces the logics to leave SC=04 and form the result descriptor at SC=14.

LCHF to 0

D17F is set because the DFCU became busy and no error conditions occurred to set D19F, D20F or D21F. DERS becoming true causes the I/O logics to exit to SC=14 before D17F can be set. If D17F is set with LCHF on at SC=04 then no error conditions occurred and the Disk Read or Write operation may be continued.

DISK FILE READ; SEQUENCE COUNT EQUAL TO EIGHT

File Word Coincidence Level (FWCL) must be true before the I/O control recognizes any characters on the File Read Lines. FWCL is true only during active word time on the disk.

File Clock Pulses (FCLP) are true for 1.6 μs. FCLP is generated from the SCLM multi which is located in the DFCU. SCLM must be 1.1 μs minimum in duration to assure that each FCLP is gated with one I/O clock pulse.

Each character read from disk is available on the File Read Lines (FRnL) for 1.6 μs. The FRnL's are generated in the DFCU by the Storage Read Switches (SRnS). The SRnS inputs are gated by the 1.6 μs multi SCLM. Therefore, the I/O control receives a FCLP in coincidence with each character on the File Read Lines.

STRF to 1

Each FCLP generated with FWCL true in the DFCU sets STRF with the next I/O clock pulse.

HOLF to 1; STRF to 0

STRF is set to cause a normal HOLF, STRF sequence to occur.

HOLF to 0

HOLF cannot be cleared until after the termination of FCLP. I24S/ becomes true when no File Clock Pulses are present.

IBnF to 1 (UNCL)

The 1.6 μs File Read Pulses sets its respective Input Buffer Flip-flop with the unclocked inputs.

LPnF to LPnF

The I/O clock pulse that finds STRF set gates the outputs of the IBNF's into the Longitudinal Parity Register. Any IBnF Flip-flop that is found set complements the appropriate LPnF.

IB[B thru 1] to W[CC]

The disk character in the IBnF is gated into the W-register with each STRF, HOLF combination.

IB[B thru 1] to 0

The same I/O clock pulse that gates the disk character from IBnF to the W-register also clears the IB-register in preparation for the next disk character. Group Mark characters are not allowed to be sensed with any Disk Read or Write operation because Allow Group Mark Switch (AGMS) output is held false.

CC + 1

The character counter is counted plus one as each disk character is transferred from the IBnF to the W-register. LCHF being set inhibits the counting of the character counter.

LCHF to 1

LCHF is set when the eighth character is read from the disk file. LCHF being set freezes the character counter at a count of zero.

LCHF to 0; LP[B thru 1] to 0

The next STRF * HOLF combination occurs on the LP character read for this word. The LP character is not placed into the W-register because LCHF is set. This character is used only to complement the LPnF's. With LCHF on, the reading of the LP character causes LCHF and LPnF to be cleared.

D2OF to 1

The clock pulse that cleared LCHF samples the outputs of the Longitudinal Parity Register. All LPnF's being set causes LPES to be false. Any one of the LPnF's reset causes D2OF to be set.

D2OF may also be set if a parity error is detected on any character in the IB-register. PELS becomes true to set D2OF.

The Disk File Control Unit terminates a read operation by its Sequence Counter returning to the Idle state. FCBL becomes false to make I22S/ true. If the character counter was at some count other than zero, then a partial word has been read from the disk. This error condition is flagged in the Result Descriptor by D2OF.

SC + 1

As the LP character is checked for parity errors the Sequence Counter is counted to nine in preparation to write the contents of the W-register into memory.

EXNF to 1

The Read Operation is terminated when Word Coincidence Level becomes false with the Disk File Control Idling (I22S/).

SC to 14

With EXNF on I26S/ is checked to determine if the Read operation was terminated because the Electronic Unit became Not Ready. A programmer may designate a valid beginning address but the segment count may cause the operation to overflow into a non-existent disk. When this happens, the Electronic Unit becomes Not Ready and the DFCU returns to its SC=03. I26S/ is found true when EXNF is set. This error condition is flagged in the Result Descriptor by D21F.

DISK FILE WRITE; SEQUENCE COUNT EQUAL TO EIGHT

After the disk file address has been accepted by the DFCU, the I/O logics proceeds to SC=09 and accesses from core memory the first word to be written on the disk. At SC=10 the first character is placed into the Output Buffer Flip-flops (OBnF) provided the word count override flag, D17F, is reset and no memory address errors have been detected, D22F reset.

A FCLP during a write indicates the character in the OBnF has been accepted by the DFEU. The I/O logics must place another character in the OBnF before the next FCLP is generated by the disk.

STRF to 1 (UNCL)

Word Coincidence Level must be true before a FCLP is allowed to set STRF.

HOLF to 1; STRF to 0

A normal STRF * HOLF combination occurs after STRF is set.

HOLF to 0

The FCLP is 1.6 μs induration and I24S/ again becomes true when the clock pulse has terminated. The Holdover Flip-flop is reset with the next system clock.

W[CC] to OB[B => 1]

The next I/O clock pulse that finds STRF set causes the next character in the W-register pointed to by the character counter to be transferred into the Output Buffer Flip-flops. Transfer from W-register unclocked (TWUD) is the level that accomplishes this transfer.

$$TWUD = DROD * STRF * (SC=8) * LCHF/ * LPWF/ * D24D/ * D22F/ * D17F/$$

Last Character Flip-flop (LCHF) being set indicates all characters in the W-register have been transferred into the OBnF's.

Last Character Flip-flop (LCHF) being reset indicates valid characters remain in the W-register to be written on disk. Longitudinal Parity Write Flip-flop (LPWF) being reset indicates the LP-character is not being written.

No memory address errors have occurred at SC=09 if D22F is reset. A word count override has not occurred to prevent transferring data to the disk when D17F is found reset.

CC + 1

The Character Counter is advanced by one count with each FCLP generated character counter is inhibited from counting during the writing of the LP-character.

LCHF to 1

The Last character Flip-flop is set as a logical flag to prevent counting the character counter when the last character is in the OBnF's.

OB[B => 1] to 0; LPWF to 1

The FCLP that occurs with the last character in the OBnF's indicates to the logics that the longitudinal parity character remains to be written on disk. No more information is to be supplied by the Output Buffer Flip-flops. LPWF is used as a logical delay to prevent the W-register from being reloaded before the LP-character has been written on the disk. The Longitudinal Parity character is generated by the Disk File Control Unit.

LCHF to 0

Last Character Flip-flop is reset after the last character in the OBnF is transferred to the disk.

LPWF to 0

The Longitudinal Parity Flip-flop is set prior to the writing of the LP-character on the disk. LPWF is reset with the FCLP that transfers the LP character in the DFCU to the Electronic Unit.

SC + 1

The same FCLP that reset LPWF also counts the Sequence Counter to nine to access the next word from core memory.

OBAF to 1

A Memory address error or a word count override occurring during a BCL write causes "blank" characters to be written for the remainder of the write operation.

A binary write with word count override (D17F set) prevents any of the OBnF's from being set. Therefore, all zeros are written on disk for the remainder of the write operation.

D19F to 1

I28D is sampled at the termination of a Write Operation. Each character in the OBnF's is transferred into the BA-register in the DFCU. The DFCU checks the outputs of the BAnF's for proper parity. S04F in the DFCU is set if any parity error has been found. The I/O logics has no way of knowing when a parity error occurred until after termination of the write operation. At this time, the DFCU logics idles at SC=01 and in the I/O control. D19F would be set to flag a parity error occurred during write.

The only way the Disk File Control Unit can terminate any Read or Write operation is to read the next disk address. By the time the Control Unit has detected the next address, the I/O control has gone through SC=09 and SC=10 and accessed the next word. At SC=10, the first character is placed into the OBnF's and the character counter is counted plus one. At SC=08 the logics waits for either a FCLP or for the DFCU to go not busy (FCBL/ true). The DFCU going to its idle state, SC=00, 01, 02 or 03 causes I22S/ to become true. If whole words were written on the disk, the character counter should be setting at CC=1 and the first character is in the OBnF's. The DFCU going not busy (FCBL/ true) causes the logics to check the setting of the character counter. Normally, the character counter is equal to one and D19F is not set.

EXNF to 1

I23S/ should be true because File Word Coincidence Level is false during inactive word time. I22S/ being true because the DFCU is idling causes EXNF to be set with the next I/O clock pulse. EXNF being set indicates to the logics that this operation has been completed and the Result Descriptor must be developed.

D20F to 1

The Write operation would have been terminated if it tried to overflow to a disk that was "write locked out." The DFCU would have idled at SC=02 and I25D would be found true with EXNF set. This program error condition is flagged in the Result Descriptor by setting D20F.

D21F to 1

The Write operation may also be terminated if this operation "overflowed" to a non-existent disk module. In this case, the Electronics Unit goes Not Ready and the DFCU idles at SC=03. I26S/ becomes true and it is checked when EXNF is set. This error condition is flagged in the Result Descriptor by D21F being set.

DISK FILE INTERROGATE

A Write Interrogate operation has D24F reset, D25F set and the Word Counter equal to zero. Any segment number in D16F thru D21F is inhibited from being transferred to DFCU by I/O. The Write Interrogate checks the address supplied with this operation as being write locked out or non-existent. A Read Interrogate performs exactly the same function as a Write Interrogate except a write lock out check is not made.

Both Interrogates check for a parity error on the prior operation. The Disk File Control Unit idling at SC=01 indicates a parity error was detected by the Disk File Control Unit while performing its last Read or Write operation. If a parity error is detected by the DFCU during any address transfer, its logics exits to SC=01 and refuses to perform an address search. W23F being on in Result Descriptor from an Interrogate operation indicates the DFCU detected a parity error on the prior operation. W19F being on in the Result Descriptor after an Interrogate indicates a parity error was detected by the DFCU during the address transfer for this operation. Bit W20F flags the address as being write locked out while W21F flags the address as not being present to the system.

SEQUENCE COUNT EQUAL TO THREE

SC to 9

The Sequence Counter is unconditionally set to nine to read the disk file address from core memory.

D24F to 0

D24F must be reset to allow the I/O Control to execute a memory read cycle on the disk file address at SC=09.

D24F to D20

The status of D24F is temporarily stored into D20 to remember a disk Read or Write operation.

D25F to 0

The starting disk address is never included in the word count filed. The word count field being equal to zero in an interrogate operation inhibits the count down of the word counter at SC=9. D25F being reset also disables the word count override logics to set D17F when the Word Counter is found equal to zero at SC=09. D17F is normally used to prevent any data from being transferred to the DFCU.

D25F to D21F

The original status of D25F is temporarily stored into D21F to remember if word count override is to be used in a disk Read or Write Operation.

D26F to 0

D26F has no logical function in any Disk File Operation.

EXNF to 1

The External Flip-flop is used as a logical flag to cause branching to SC=04 while in SC=10 after the disk file address has been read from core memory.

D27F to D17F

The original status of D27F is temporarily stored into D17F to remember a binary read or write operation. D17F being ON at SC=10 inhibits a character transfer from the W-register to OBnF. This character transfer is always redundant prior to an address transfer and therefore D17F has no effect on the overall operation. At SC=04, D17F again has no effect on the disk address transfer.

D27F to 0

D30F is only ON for the Disk File Read Check Descriptor. D27F would be reset here and again set the first clock pulse upon initial entry into SC=04. D27F is reset here and is again set one clock pulse after FASS goes true at SC=04. This logical sequence sets the Read Check Flip-flop in the DFCU.

RCKF = FBIL/ * FASS * FDTL

D27F must be on during an address transfer.

D27F to 1

All operations except Read Check set D27F to cause FBIL to become a true level upon initial entry into SC=4. FBIL and FASS going true together prevent the Read Check Flip-flop in the DFCU from being set.

D30F to 1

The Interrogate operation (D25F WC=0) sets D30F at this time. D30F has no logical function until D17F is set with LCHF on at SC=4. This logics forces the Sequence Counter to 14 to form a Result Descriptor. I28D, I26S/ and I25D are sampled before D17F is set.

SEQUENCE COUNT EQUAL TO NINE

The disk address on which the interrogate is to be performed is read from memory. If D17F had been set at SC=3, it would have no logical effect at SC=9.

SEQUENCE COUNT EQUAL TO TEN

Since D24F was unconditionally cleared at SC=3, the character counter always counts plus one for all disk file operations. If D17F had been set at SC=3, the transfer of character Zero into the OBnF would have been inhibited. This is of no importance because the disk address contains seven characters. The first character is logically discarded anyway.

EXNF being ON forces the logics to exit to SC=4.

SEQUENCE COUNT EQUAL TO FOUR

An interrogate operation has D30F set upon initial entry to SC=4. The condition of D17F is of no importance until the address transfer has been completed (CC=0).

OBnF to 0

The OBnF's are cleared after the last address character has been transferred.

LPnF to OBnF

The segment is inhibited from being transferred in an interrogate operation because D25F is set and Word Counter is equal to zero.

LCHF to 1

The Last Character Flip-flop is set with the HOLF * STRF combination that normally transferred the segment number to the DFCU.

D17F to 0

D17F is used as a logical flip-flop to determine when the DFCU becomes busy. Up until this point in the logics, D17F has been a temporary storage for D27F. D27F is restored to its original setting. About 600 μs after LCHF is set D17F is set and the logics exits to SC=14. The Result Descriptor is developed to indicate the status of the disk address just interrogated.