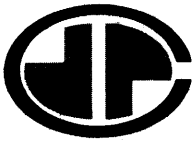
CDP-XI/00 PROCESSOR
MAINTENANCE MANUAL

VOLUME II



california data processors

2019 south ritchey street · santa ana, california 92705 · (714) 558-8211

CDP-XI/00 PROCESSOR
MAINTENANCE MANUAL

VOLUME II

DOCUMENT 21518003
Revision X2
May 1974

california data processors

PREFACE

This volume of the CDP-XI/00 Processor Maintenance Manual is a customized volume of information for the optional elements incorporated in a specific version of the processor. This volume is divided into parts separated by index tabs. Each part is a self-contained document describing one optional element.

The following page of this volume is a list of documents included in each part.

CONTENTS OF VOLUME II

2019 south ritchey street · santa ana, california 92705 · (714) 558-8211

CDP-XI/35

EMULATE BOARD

TECHNICAL MANUAL

DOCUMENT 21518007
Revision X1
May 1974

california data processors

$4.00

REVISIONS

Revision	Date	Approval	Description
X0	5-74		Preliminary
X1	5-74		Release edition

The revision history of each page in this document is indicated below:

	Revision		
Page	X0	X1	
i	✓	✓	
ii	✓	✓	
1-1	✓	✓	
1-2	✓	✓	
2-1	✓	✓	
2-2	✓		
2-3	✓	✓	
2-4	✓	✓	
2-5	✓	✓	
2-6	✓	✓	
2-7	✓	✓	
3-1	✓		
3-2	✓		
4-1	✓		
4-2	✓		
5-1	✓	✓	
5-2	✓	✓	
5-3	✓	✓	
A-1	✓		
A-2	✓		
A-3	✓	✓	
A-4	✓		
A-5	✓	✓	
A-6	✓	✓	
A-7	✓	✓	
A-8	✓	✓	
A-9	✓	✓	
B-1	✓	✓	
B-2	✓		
B-3	✓		

CONTENTS

APPENDICES

TABLES

ILLUSTRATIONS

SECTION 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides the information needed to understand, install and maintain the CDP-XI/35 Emulate Board (part number 81080210) when used with Drawing Package 21518021. The information in this manual is for the use of a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques. A basic knowledge of design principles and circuits used in small computers is assumed, hence no tutorial material of this kind is included. An understanding of the PDP-11/35 computer system emulated by this system and of the CDP-XI/00 processor is also assumed. Detailed information about the former is available in manuals published by the computer manufacturer. The latter is described in the CDP-XI/00 Processor Maintenance Manual (Volume I).

As a stand-alone publication, this manual has a good functional and physical description of the emulate board, providing the information needed to understand the capabilities and features of the board. The maintenance coverage of this manual is commensurate with the pre-requisite skills and knowledge of the defined user, characteristics of the product and maintainability requirements established by Cal Data.

1.2 DOCUMENTATION

This manual describes the CDP-XI/35 Emulate Board of a CDP-XI computer system that also includes a CDP-XI/00 processor and chassis, a power supply and I/O devices.

The following paragraphs define publications and conventions that support this manual.

1.2.1 Publications

The emulate board is one hardware element of a CDP-XI/35 system that is described at the macro level and micro level by two manuals:

21518003	CDP-XI/00 Processor Maintenance Manual, Volume I
21518036	CDP-XI/35 Emulation User Manual

For maintenance purposes, this manual is supported by Drawing Package 21518021, which contains theory of operation, schematic diagrams, assembly drawings and other required engineering drawings. The drawing package is updated with the latest revision of each drawing. Since

certain revisions may result in reassignment of drawing numbers, the text of this manual makes reference to drawings by title rather than by number.

1.2.2 Abbreviations and Conventions

Table 1-1 lists the abbreviations found in this manual.

Conventions used in the text of this manual include:

a. ZERO and ONE for binary logic "0" and "1" states, respectively.
b. Signal names capitalized for easy identification.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data or CDP	California Data Processors
cm	Centimeter
psi	Pounds per square inch
kg/cm^2	Kilograms per square centimeter
cfm	Cubic feet per minute
cmm	Cubic meters per minute
ROM	Read-only memory
EIA	Emulate-interrupt address
PSW	Processor status word

SECTION 2
DESCRIPTION

2.1 GENERAL

The CDP-XI/35 Emulate Board (Figure 2-1) is a "language concentrator" that allows the CDP-XI/00 processor to emulate the DEC PDP-11/35* computer (and the PDP-11/40, which uses the same instruction set) at average speeds comparable to the machine being emulated.

Because of differences in system architecture, some PDP-11/35 instructions are executed faster and some slower in the CDP-XI system with the emulate board. For this reason, and due to the asynchronous operation of the MACROBUS™ (whereby direct-memory-access devices can come on-line at any time), time-dependent program loops should be avoided to ensure complete program interchangability between the XI/35 and the machine being emulated.

2.2 FUNCTIONAL DESCRIPTION

The CDP-XI/00 processor with the CDP-XI/35 Emulate Board and firmware forms a system (Figure 2-2) that emulates the functions of the PDP-11/35 computer. To the user, the CDP-XI system is an 11/35 (or 11/40) and is transparent to all applicable PDP software.

The CDP-XI/00 processor comprises two engine boards and an I/O board, in addition to the emulate board. The engine has all the elements of a very fast and versatile processor, but without an I/O structure. An I/O capability is provided by the I/O board and MACROBUS structure. These three boards are all that are required to emulate the PDP-11/35 and UNIBUS*. Such an emulation, however, would be slow due to the distribution of data and control bits that must be analyzed in different PDP-11 instructions. This makes decoding and arithmetic comparisons difficult. The emulate board works with the engine to provide custom, high-speed instruction-decoding logic to emulate the PDP-11/35 at comparable average program speed.

2.2.1 Instruction Emulation

To emulate instructions, the processor executes appropriate microcommand sequences from control memory. Depending on the instructions being emulated, different sequences are executed in a specific order. To save time, emulate-board logic (Figure 2-3) sufficiently decodes each instruction to determine the microcommand sequence(s) to execute. Furthermore, the emulate board generates (by table-lookup) the starting address within control memory of each required microcommand sequence. This address is called the emulate-interrupt address (EIA).

---

*The following are trademarks of Digital Equipment Corporation: PDP, UNIBUS, DEC.

TM: MACROBUS is the trademark of California Data Processors.

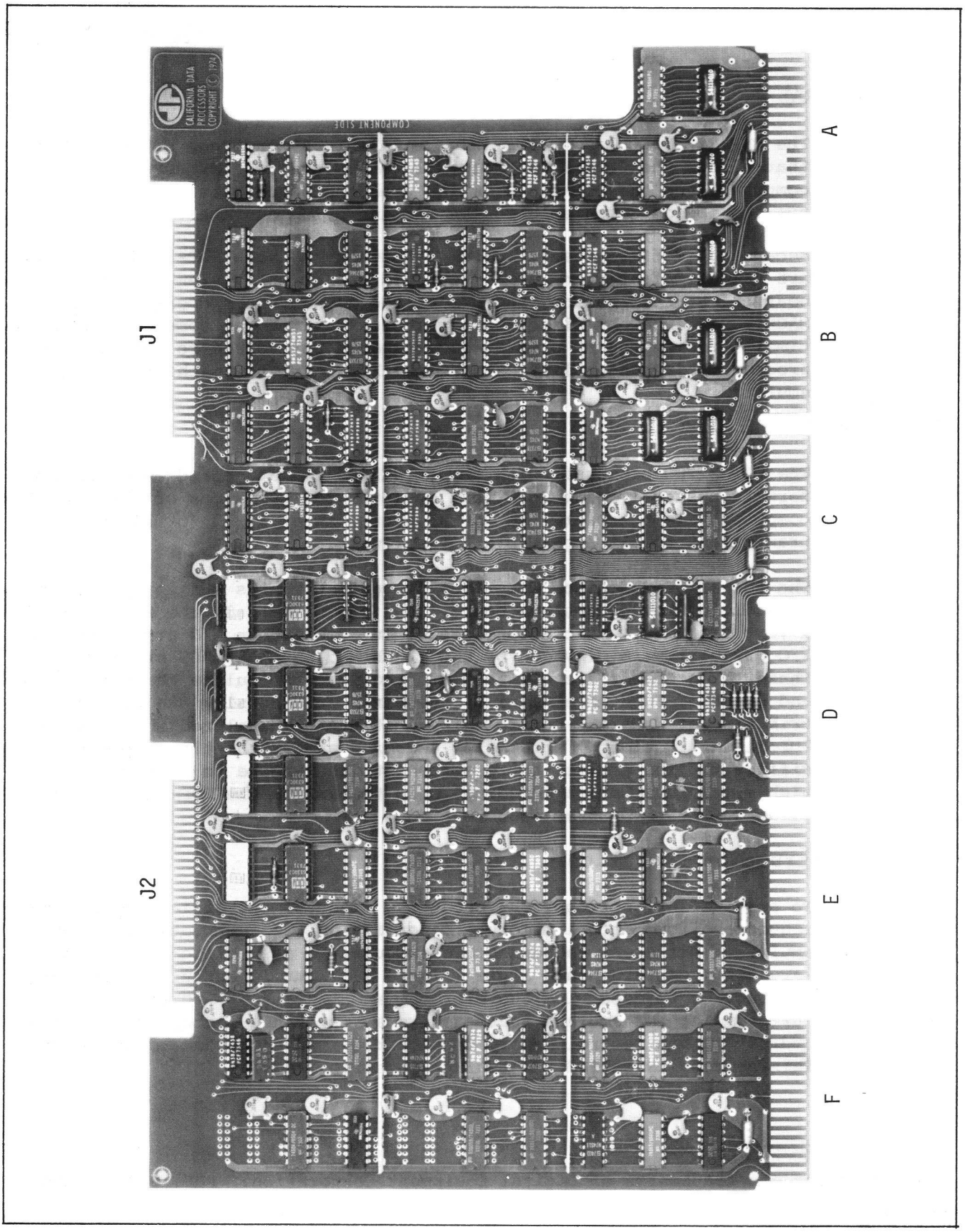


Figure 2-1. CDP-XI/35 Emulate Board, Component Side

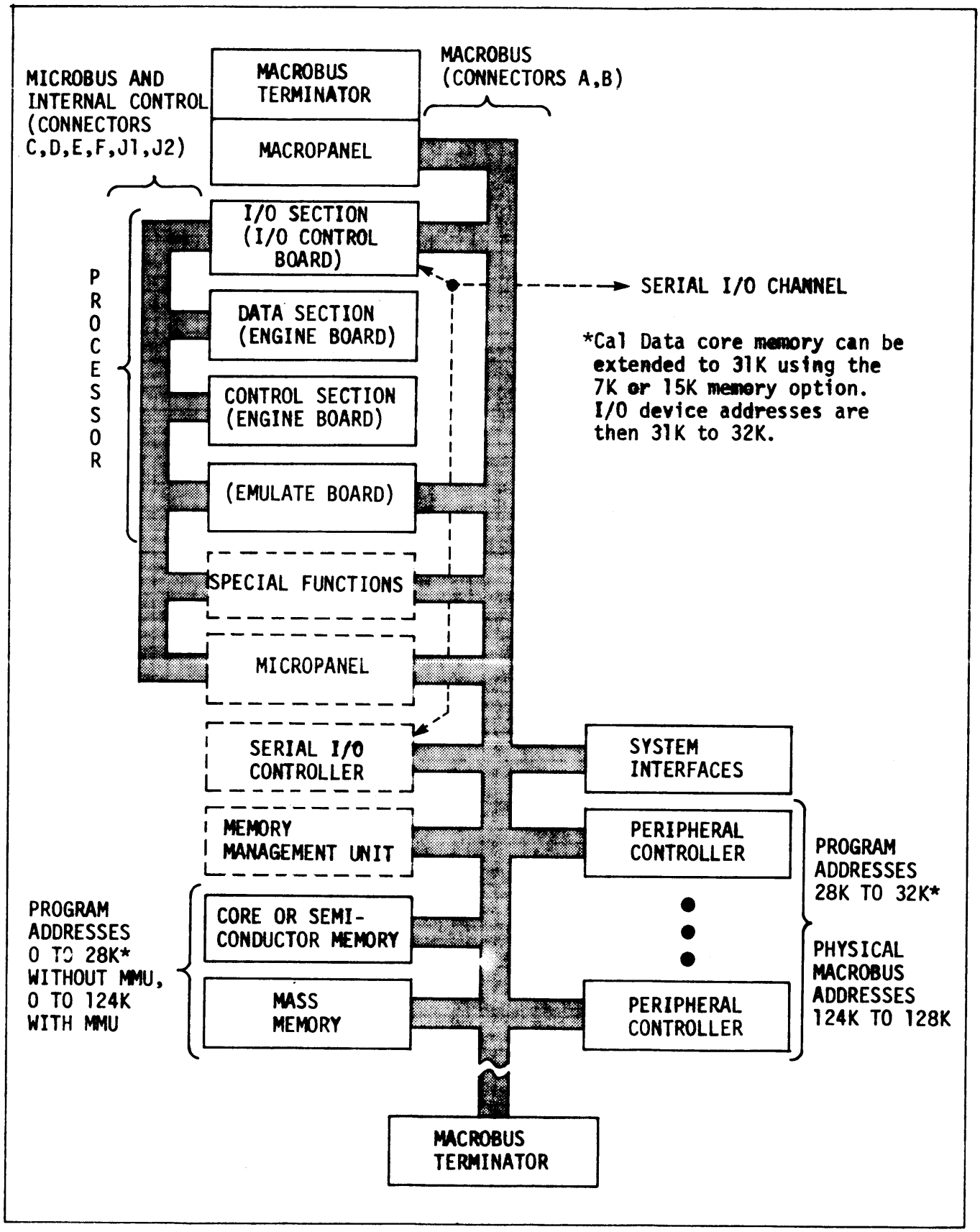


Figure 2-2. CDP-XI System Organization

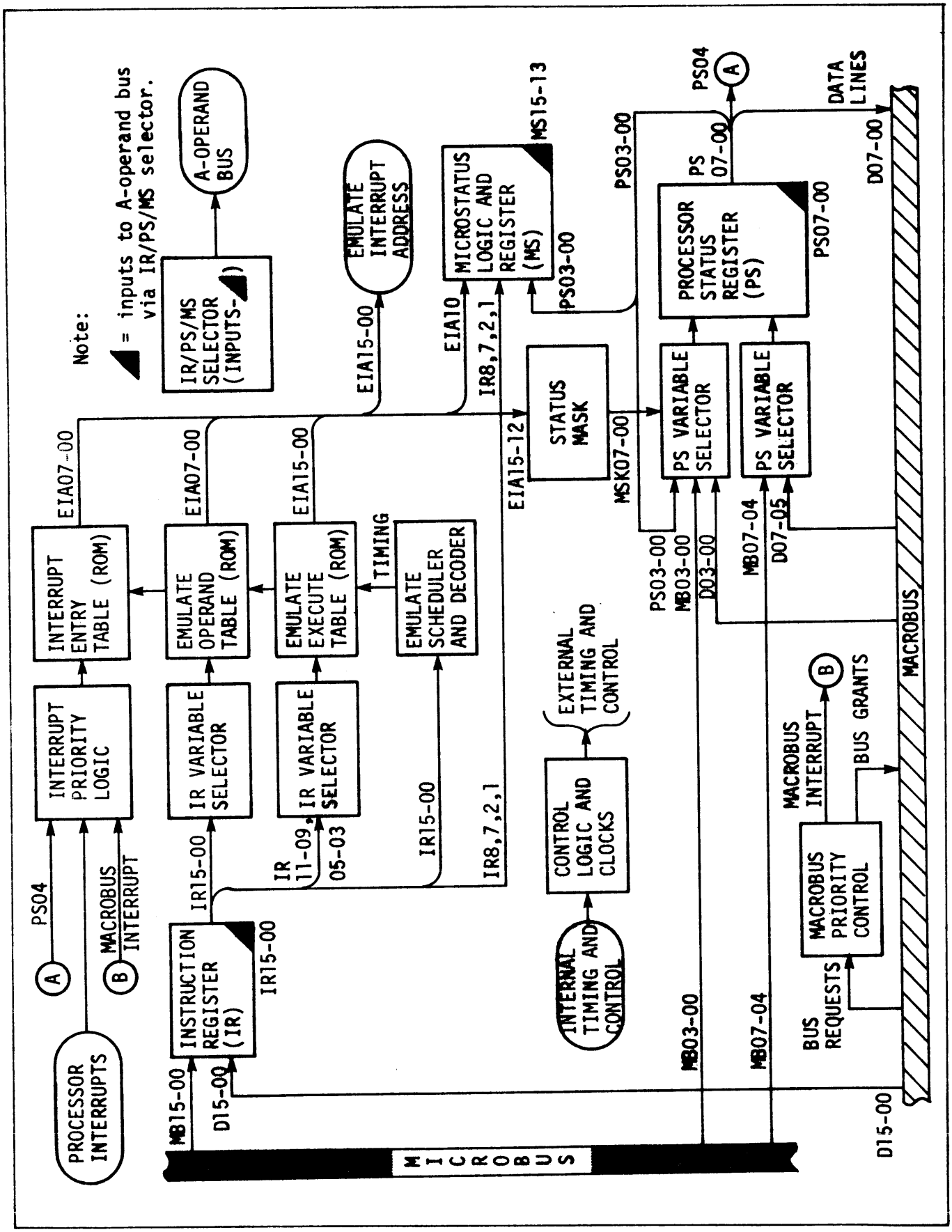


Figure 2-3. Emulate Board Simplified Block Diagram

2.2.2 Emulate-Interrupt Address (EIA)

Three kinds of EIA are generated by the emulate board, according to the sequence being processed:

a. Operand-sequence addresses from the emulate operand table.
b. Execution-sequence addresses from the emulate execution table.
c. Processor-interrupt vector addresses from the interrupt entry table.

Table 2-1 shows the relationship between operand and execution sequences within the complete emulation sequence for double-operand, single-operand and control instructions. Processor-interrupt vector addresses are enabled by the interrupt priority logic.

One or two *operand sequences* are required for each single- or double-operand PDP-11 instruction, respectively. Each operand sequence fetches one operand from the appropriate location.

An *execution sequence* is required for the emulation of any instruction, with or without operands. The execution sequence performs the function specified by the emulated instruction. Although different instructions often call for execution of the same operand sequences, each instruction generally has a separate execution sequence. Firmware associated with the execution sequence indicates the end of a complete emulation and enables the beginning of the next emulated instruction, if any.

An *interrupt vector address* is generated for each recognized interrupt.

2.2.3 Emulate-Execute Table

The emulate-execute table is an ROM addressed by selected control bits of the instruction being emulated. For each possible combination of bits selected by the variable selector and the decoder, and applied to the table, a 16-bit control word is output.

Eight bits of the output control word comprise the execution-sequence EIA sent to the processor control memory. Four bits are used for special control functions within the emulation logic.

The most-significant four bits output from the emulate-execute table control the modification of bits 03 to 00 of the processor status word (PSW). This modification is under firmware control. These PSW bits are the status flags required by the program (03 negative, 02 zero,

Table 2-1. Emulation Sequences

Step	Double-Operand Instruction	Single-Operand Instruction	Control Instruction
1	Operand sequence	Operand sequence	Execution sequence
2	Operand sequence	Execution sequence	---
3	Execution sequence	---	---

01 overflow and 00 carry). The emulate-execute table provides rapid and specific updating of these bits in the single cycle following the execution of the instruction, i.e., just after the fetch for the next instruction is issued. The updated PSW can be read from the emulate board at either the macro level via the MACROBUS, or the micro level via the A-operand bus (AB). The instruction register (IR) or the microstatus register (MS) can also be read via AB, with the information on that bus being determined by the emulate IR/PS/MS selector, which is in turn governed by the address generated in the A-operand field.

2.3 PHYSICAL DESCRIPTION

The emulate board is a hex-height board 15.69 inches (39.85 cm) by 8.94 inches (22.70 cm) that normally plugs into slot 5 of the CDP-XI/00 backplane.* The right-hand edge of the board has a 1.0 by 5.5 inch (2.54 by 13.97 cm) cutout as clearance for the side-mounted cooling fans in the chassis.

There are six printed-circuit connectors (A through F) on the bottom edge of the board, and two (J1 and J2) on the top edge. Connectors A and B interface with the MACROBUS. Connectors C through F, and J1 and J2 interface with the other processor boards. Connectors A through F are standard backplane connectors. Connectors J1 and J2 plug into the two small processor interconnection boards.

2.4 SPECIFICATIONS

General specifications for the emulate board are given in Table 2-2.

*Because of the universal connections in the processor area of the backplane, the emulate board can operate in any slot assigned to a basic or optional processor board, including the macropanel.

Table 2-2. CDP-XI/35 Emulate Board General Specifications

Characteristic	Specification
Interface	Two connectors (A and B) interface with the standard CDP-XI MACROBUS. Six connectors (C, D, E, F, J1 and J2) interface with other processor boards.
Power	Operating Amperes / Voltage Tolerance
+5V	7.0±10% / ±5%
	*As part of a four-board CDP-XI/35 processor set with a 512-word control memory.
Configuration	Hex-height printed circuit board.
Dimensions	15.69 by 8.94 inches (39.85 by 22.70 cm).
Mounting Centers	0.75 inch (1.91 cm) recommended minimum.
Ambient Temperature	0 to +50° C with 200 cfm (5.6 cmm) airflow.
Ambient Humidity	0 to 90 percent without condensation.

SECTION 3
INTERFACE

3.1 GENERAL

The emulate board interfaces with the other processor boards via the CDP-XI chassis backplane, which includes the MACROBUS, and via two small interconnection boards spanning the tops of the processor boards.

The interface with the MACROBUS (connectors A and B) conforms to all standard PDP-11 interfacing rules for I/O compatibility. This section assumes an understanding of the MACROBUS and UNIBUS I/O structures, described in other publications.

3.2 SIGNALS

Backplane connectors are labeled A through F. A and B carry the MACROBUS. Connectors on the small processor-interconnection boards are labeled J1 and J2. Pin assignments for all interface connectors are listed in Appendix A.

3.3 CIRCUITS

Because the emulate board is attached to the MACROBUS along with peripheral devices and memory, the MACROBUS loading introduced by the board is an important system consideration for configurations containing a large amount of memory or numerous peripheral devices. The emulate board minimizes the loading of receivers and the leakage current of drivers in the high state (these being the critical bus-loading parameters). This is accomplished in two ways:

a. The driver leakage load is limited to that of one gate instead of two (as is common in some logic designs).
b. A CDP proprietary bus receiver circuit improves speed and reduces drive requirements.

3.3.1 Line Driver

The line driver is a TTL buffer. The critical MACROBUS specifications for the device are:

Output low voltage at 50 mA sink (V_{OL})	+0.5 V, max.
Output high leakage current at 2.5 V (I_{OH})	+60 µA, max.

3.3.2 Line Receiver

The emulate board uses a CDP line receiver. The critical MACROBUS specifications for this device are:

Input high threshold (V_{IH})	+2.5 V min.
Input low threshold (V_{IL})	+1.4 V max.
Input current at +2.5 V (I_{IH})	+60 µA max.
Input current at 0.0 V (I_{IL})	±25 µA max.

3.3.3 MACROBUS Loading

The limiting MACROBUS loading occurs on the bidirectional data lines that have one receiver and one driver for each I/O module. Worst-case MACROBUS load specifications are:

V_{IH}	+2.5 V min.
V_{IL}	+1.4 V max.
I_{IH}	+120 µA max. at +2.5 V.
I_{IL}	±25 µA max. at 0.0 V.

SECTION 4
INSTALLATION

4.1 GENERAL PROCEDURES

When used as part of a CDP-XI computer, the emulate board will have been installed and tested by Cal Data prior to shipment. Thus, the following procedures describe the installation of a board received individually for addition to an existing installation.

The emulate board is designed for direct installation in the CDP-XI processor chassis. The installation procedure consists of inserting the emulate board into slot 5 of the backplane so that the A and B board-edge connectors interface with the MACROBUS backplane connectors.

Power and ground connections to the emulate board are made via the backplane connectors as given in Appendix A.

4.1.1 Unpacking and Inspection

When the emulate board is not part of a system, it is shipped in an individual padded shipping container for protection during transportation. This container can be saved for future use if the unit is returned for repair or reshipped separately from the associated computer system.

The following steps are recommended for unpacking and inspecting the board:

1. Prior to opening, inspect the box for obvious damage.
2. Cut the packing tape, open the box and remove the board. Next, remove the plastic wrapper and inspect the board for physical damage.
3. Inspect the board connector pins for any foreign matter and clean if necessary for reliable contact with the connectors.

It is important to note immediately any physical damage that might have resulted from shipment. The carrier should be notified of such damage and given the opportunity to inspect the unit and container. This helps establish the validity of any claims for shipping insurance.

4.1.2 Handling

The emulate board can withstand all normal shock and vibration encountered in shipping and when installed in a computer system. While not a fragile device, the unit should be handled with reasonable care to avoid damage that might result in operational failure. The following are general pointers on handling the unit during inspection, installation and maintenance operations:

a. Avoid bending components when handling the board. To prevent oxides from forming on the gold plating, do not touch the connector pins.
b. Always insert and remove the board with the system power OFF.
c. When inserting the board, ensure that the component side faces the correct direction (toward the front of the chassis) and that the board is properly aligned in the card guides.

d. Insert and remove the board slowly and carefully so that it does not make contact with adjacent boards.
e. Never use components as finger grips. Use the grip areas at the corners of the board.

4.2 INSTALLATION IN THE CDP-XI SYSTEM

Insert the emulate board carefully into slot 5 of the backplane with the component side of the board facing the front of the chassis. When all processor boards are in place, press the two small processor-interconnection boards onto the top connectors (J1 and J2) of the emulate and other processor boards. Do not use force in making these connections, but be sure that all connectors are firmly seated.

SECTION 5
MAINTENANCE

5.1 GENERAL

This section describes preventive and corrective maintenance procedures that apply to the CDP-XI/35 Emulate Board. In general, corrective maintenance is limited to the isolation of a fault to the emulate board followed by replacement of the board. Troubleshooting can then be used to verify that the suspected module is malfunctioning and to help diagnose the specific problem. Repair should be conducted at the factory or by an authorized representative.

5.2 PREVENTIVE MAINTENANCE

The emulate board is a reliable solid-state device designed to perform continuously for many years. Preventive maintenance consists of performing the following tasks every six months:

a. Inspect the board for damaged wires, components or other obvious defects.

b. Using a low pressure source of air (75 psi one foot from the board or 5 kg/cm^2 30 cm from the board), blow off accumulated dust and foreign matter.

5.3 CORRECTIVE MAINTENANCE

Repair or adjustment of the emulate board in the field is not recommended. If a malfunction is detected, replace the board with a spare known to be operating properly and return the malfunctioning board for repair to California Data Processors or an authorized representative.

Malfunctions can be detected with the aid of the test programs described in the following paragraphs.

5.3.1 Test Programs

When the emulate board is installed in a CDP-XI computer system, it can be tested by the DEC programs MAINDEC-11-D0AA to D0MA. This group of 13 tests, which incrementally test and isolate faults on the emulate board, should be run in numerical order:

1.	Unconditional branch test	D0AA
2.	Conditional branch test	D0BA
3.	Single-operand (unary) instruction test	D0CA
4.	Single/double-operand (unary/binary) instruction test	D0DA
5.	Rotate/shift test	D0EA
6.	Equality comparison test	D0FA
7.	Nonequality comparison test	D0GA
8.	Move test	D0HA
9.	Bit set/clear test	D0IA
10.	Addition test	D0JA
11.	Subtraction test	D0KA
12.	Jump test	D0LA
13.	JSR/RTS/RTI test	D0MA

These programs occupy all of the lowest 4K of memory, except for locations 017500 to 017776, which are required by the boot and absolute loader. All test programs start at 0200.

After starting, the program loops and rings a bell after a fixed number of iterations. The times given in the program description are the times between bells.

5.3.1.1 Program Description

D0AA (5 minutes) tests the execution of the unconditional-branch instruction and ensures that a long program can be loaded into and executed from any position in memory.

D0BA (2.5 minutes) tests the execution of all conditional-branch instructions, using microprogram operations to manipulate the condition codes.

D0CA (3 minutes) tests the execution of single-operand instructions and their effect on condition codes.

D0DA (6 minutes) is a combined test of the execution of single- and double-operand instructions, their results and condition codes.

D0EA (5 minutes) tests the execution of rotate/shift instructions in both word and byte mode. Applicable registers and memory locations are all tested.

D0FA (6 minutes) tests the execution of instructions involving comparisons for equality, including all conditional branches that branch on equality. D0FA tests both word and byte operations.

D0GA (5 minutes) tests the execution of instructions involving comparisons where there is no equality e.g., branch when not equal, branch when greater than, branch when less than.

D0HA (6 minutes) tests the execution of the MOVE instruction to both memory and registers.

D0IA (3 minutes) tests the execution of the bit-set, -clear and -test instructions to both memory and registers.

D0JA (4 minutes) tests the execution of the ADD instruction.

D0KA (2 minutes) tests the execution of the SUB instruction.

D0LA (4 minutes) tests the execution of the JMP instruction.

D0MA (2 minutes) tests the execution of the JSR, RTS and RTI instructions.

The tests described above contain subtests that frequently use the SCOPE and HLT subroutines. SCOPE is a no-operation instruction that occurs between each two subtests within each of the twelve tests; this allows insertion of a scope loop with a branch to a previous SCOPE location from the current SCOPE location so that one or more subtests can be rechecked. HLT stops the program and displays PC+2 when the ADDR/DATA switch is in ADDR, thus locating the faulty subtest; if ADDR/DATA is in DATA, the contents of R0 are displayed and the listing indicates whether the data are significant for that subtest.

In addition, the following tests are also applicable to the CDP-XI/35:

a. T14 trap test (MAINDEC-11-DONB-PB).
b. T15 11-family instruction set test (MAINDEC-11-DCQKC-P1-PB).
c. SXT instruction test (MAINDEC-11-DCKBA-A-PB).
d. XOR instruction test (MAINDEC-11-DCKBC-A-PB).
e. MARK instruction test (MAINDEC-11-DCKBD-B-PB).
f. RTI/RTT instruction test (MAINDEC-11-DCKBE-B-PB).

5.3.1.2 Loading, Starting and Running

To load and start the program:

1. Using the ABS loaders load the program into the lowest 4K of memory.
2. Using the switch register, load starting address 0200.
3. Press START.

The program loops and on completion of each test rings the teleprinter bell. Any error will cause a halt.

If the program halts in trap/interrupt vector area (0 to 0400), examine stack pointer R6 to find the address of the program-counter instruction that caused the trap. This address contains the PC value of the instruction following the one where the trap occurred. To recover from a trap-error halt, restart the program at 0200 and press CONT.

APPENDIX A
CONNECTOR PIN ASSIGNMENTS

Figure A-1 shows the layout of the connectors on the CDP-XI/35 Emulate Board. Tables A-1 to A-8 give the pin assignments for connectors A to F, J1 and J2.

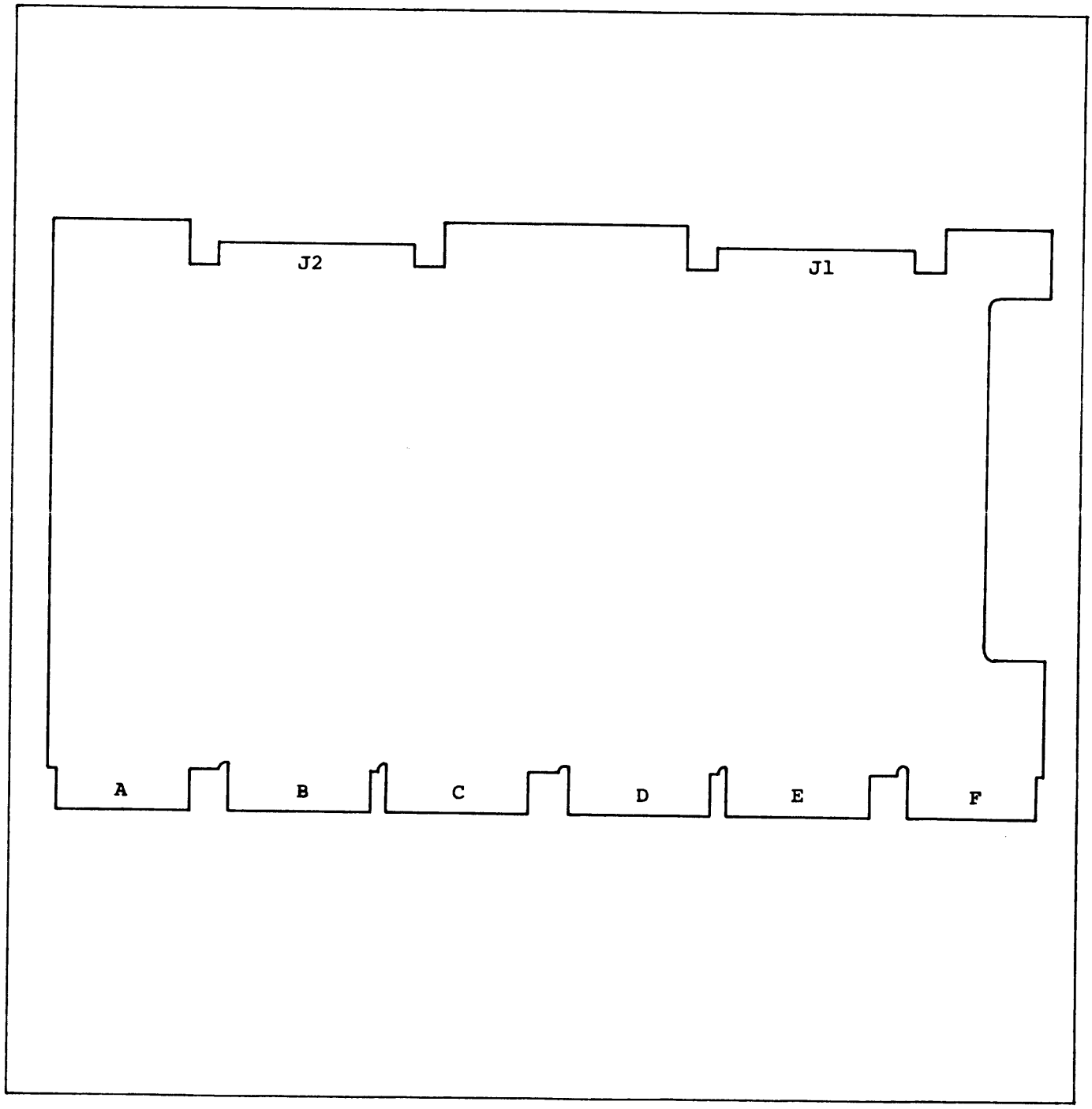


Figure A-1. CDP-XI/35 Emulate Board Connectors

Table A-1. Connector A Pin Assignments, MACROBUS

Name	Signal	Pin	Pin	Signal	Name
Initialize	BUS INIT-L	A1	A2	+5V	+5 Vdc
Interrupt	BUS INTR-L	B1	B2	GND	Ground
Data 00	BUS D00-L	C1	C2	GND	Ground
Data 02	BUS D02-L	D1	D2	BUS D01-L	Data 01
Data 04	BUS D04-L	E1	E2	BUS D03-L	Data 03
Data 06	BUS D06-L	F1	F2	BUS D05-L	Data 05
Data 08	BUS D08-L	G1	H2	BUS D07-L	Data 07
Data 10	BUS D10-L	J1	J2	BUS D09-L	Data 09
Data 12	BUS D12-L	K1	K2	BUS D11-L	Data 11
Data 14	BUS D14-L	L1	L2	BUS D13-L	Data 13
Parity Bit Low	BUS PA-L	M1	M2	BUS D15-L	Data 15
Ground	GND	N1	N2	BUS PB-L	Parity Bit High
Ground	GND	P1	P2	BUS BBSY-L	Bus Busy
Ground	GND	R1	R2	BUS SACK-L	Selection Acknowledgement
Ground	GND	S1	S2	BUS NPR-L	Nonprocessor Request
Ground	GND	T1	T2	BUS BR7-L	Bus Request 7
Nonprocessor Grant	BUS NPG-H	U1	U2	BUS BR6-L	Bus Request 6
Bus Grant 7	BUS BG7-H	V1	V2	GND	Ground

Name	Signal	Pin	Pin	Signal	Name
Bus Grant 6	BUS BG6-H	A1	A2	+5V	+5 Vdc
Bus Grant 5	BUS BG5-H	B1	B2	GND	Ground
Bus Request 5	BUS BR5-L	C1	C2	GND	Ground
Ground	GND	D1	D2	BUS BR4-L	Bus Request 4
Ground	GND	E1	E2	BUS BG4-H	Bus Grant 4
AC Low	BUS ACLO-L	F1	F2	BUS DCLO-L	DC Low
Address 01	BUS A01-L	H1	H2	BUS A00-L	Address 00
Address 03	BUS A03-L	J1	J2	BUS A02-L	Address 02
Address 05	BUS A05-L	K1	K2	BUS A04-L	Address 04
Address 07	BUS A07-L	L1	L2	BUS A06-L	Address 06
Address 09	BUS A09-L	M1	M2	BUS A08-L	Address 08
Address 11	BUS A11-L	N1	N2	BUS A10-L	Address 10
Address 13	BUS A13-L	P1	P2	BUS A12-L	Address 12
Address 15	BUS A15-L	R1	R2	BUS A14-L	Address 14
Address 17	BUS A17-L	S1	S2	BUS A16-L	Address 16
Ground	GND	T1	T2	BUS C1-L	Control 1
Slave Synchronization	BUS SSYN-L	U1	U2	BUS C0-L	Control 0
Master Synchronization	BUS MSYN-L	V1	V2	GND	Ground

Table A-3. Connector C Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Microbus 00	MB000-L	A1	A2	+5V	+5 Vdc
Microbus 01	MB001-L	B2	B2	-15V	-15 Vdc
Microbus 02	MB002-L	C1	C2	GND	Ground
Microbus 03	MB003-L	D1	D2	MB004-L	Microbus 04
Microbus 05	MB005-L	E1	E2	MB006-L	Microbus 06
Microbus 07	MB007-L	F1	F2	MB008-L	Microbus 08
Microbus 09	MB009-L	H1	H2	MB010-L	Microbus 10
Microbus 11	MB011-L	J1	J2	MB012-L	Microbus 12
Microbus 13	MB013-L	K1	K2	MB014-L	Microbus 14
Microbus 15	MB015-L	L1	L2	AB000-H	A Bus 00
A Bus 01	AB001-H	M1	M2	AB002-H	A Bus 02
A Bus 03	AB003-H	N1	N2	AB004-H	A Bus 04
A Bus 05	AB005-H	P1	P2	AB006-H	A Bus 06
A Bus 07	AB007-H	R1	R2	AB008-H	A Bus 08
A Bus 09	AB009-H	S1	S2	AB010-H	A Bus 10
Ground	GND	T1	T2	AB011-H	A Bus 11
A Bus 13	AB013-H	U1	U2	AB012-H	A Bus 12
A Bus 15	AB015-H	V1	V2	AB014-H	A Bus 14

Table A-4. Connector D Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Power Failure Interrupt	PFINT-H	A1	A2	+5V	+5 Vdc
Halt Interrupt	HLINT-H	B1	B2	-15V	-15 Vdc
Data Switch 16	DS16-H	C1	C2	GND	Ground
Data Switch 17	DS17-H	D1	D2	LTCL-L	Line-frequency Clock
Virtual Address	VIRTAD-H	E1	E2	PBBSY-L	Processor Bus Busy
Control Count 00	CC000-L	F1	F2	HALTP-L	Panel Halt
Control Count 01	CC001-L	H1	H2	MSR15-L	Microstatus Register 15
Control Count 02	CC002-L	J1	J2	RESET-L	Reset
Control Count 03	CC003-L	K1	K2	BUS BG7-IN	Bus Grant 7 In
Control Count 04	CC004-L	L1	L2	BUS BG7-OUT	Bus Grant 7 Out
Control Count 05	CC005-L	M1	M2	BUS BG6-IN	Bus Grant 6 In
Control Count 06	CC006-L	N1	N2	BUS BG6-OUT	Bus Grant 6 Out
Control Count 07	CC007-L	P1	P2	BUS BG5-IN	Bus Grant 5 In
Control Count 08	CC008-L	R1	R2	BUS BG5-OUT	Bus Grant 5 Out
Control Count 09	CC009-L	S1	S2	BUS BG4-IN	Bus Grant 4 In
Ground	GND	T1	T2	BUS BG4-OUT	Bus Grant 4 Out
Control Count 10	CC010-L	U1	U2	BUS NPG-IN	Nonprocessor Grant In
Control Count 11	CC011-L	V1	V2	BUS NPG-OUT	Nonprocessor Grant Out

Table A-5. Connector E Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Control Memory 00	CM000-H	A1	A2	+5V	+5 Vdc
Control Memory 01	CM001-H	B1	B2	-15V	-15 Vdc
Control Memory 02	CM002-H	C1	C2	GND	Ground
Control Memory 03	CM003-H	D1	D2	CM004-H	Control Memory 04
Control Memory 05	CM005-H	E1	E2	CM006-H	Control Memory 06
Control Memory 07	CM007-H	F1	F2	Reserved	
Control Memory 09	CM009-H	H1	H2	CM008-H	Control Memory 08
Control Memory 11	CM011-H	J1	J2	CM010-H	Control Memory 10
Decode Address 00	DAD00-H	K1	K2	CM012-H	Control Memory 12
Control Memory 13	CM013-H	L1	L2	CM014-H	Control Memory 14
Control Memory 15	CM015-H	M1	M2	DAD01-H	Decode Address 01
Control Memory 17	CM017-H	N1	N2	CM016-H	Control Memory 16
Control Memory 19	CM019-H	P1	P2	CM018-H	Control Memory 18
Switch Register 0	SRO-L	R1	R2	CM020-H	Control Memory 20
Control Memory 21	CM021-H	S1	S2	CM022-H	Control Memory 22
Ground	GND	T1	T2	CM024-H	Control Memory 24
Control Memory 23	CM023-H	U1	U2	CM026-H	Control Memory 26
Control Memory 25	CM025-H	V1	V2	CM027-H	Control Memory 27

Name	Signal	Pin	Pin	Signal	Name
Control Memory 28	CM028-H	A1	A2	+5V	+5 Vdc
Control Memory 29	CM029-H	B1	B2	-15V	-15 Vdc
Control Memory 31	CM031-H	C1	C2	GND	Ground
Control Memory 30	CM030-H	D1	D2	CM032-H	Control Memory 32
Control Memory 33	CM033-H	E1	E2	CM034-H	Control Memory 34
Control Memory 35	CM035-H	F1	F2	DAD02-H	Decode Address 02
Control Memory 37	CM037-H	H1	H2	CM036-H	Control Memory 36
Control Memory 39	CM039-H	J1	J2	CM038-H	Control Memory 38
Instruction Repeat	IRPTE-L	K1	K2	CM040-H	Control Memory 40
Control Memory 41	CM041-H	L1	L2	CM042-H	Control Memory 42
Control Memory 43	CM043-H	M1	M2	CPEN-L	Control Panel Enable
Control Memory 45	CM045-H	N1	N2	CM044-H	Control Memory 44
Control Memory 47	CM047-H	P1	P2	CM046-H	Control Memory 46
Decode Address 03	DAD03-H	R1	R2	ACMSL-L	Alterable Control Memory Select
	Reserved	S1	S2	AUXRM-L	Auxiliary ROM Select
Ground	GND	T1	T2	IRINH-L	Instruction Inhibit
	Reserved	U1	U2	IWAIT-L	Instruction Wait
System Clock	SYSCK-L	V1	V2	GND	Ground

Table A-7. Connector J1 Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Skip	SKIPP-L	1A	1B	EMA00-H	Emulate Address 00
AR Write Enable	ARWEN-L	2A	2B	EMA01-H	Emulate Address 01
Stack Limit Write Enable	SLWEN-L	3A	3B	EMA02-H	Emulate Address 02
Slave Synchronization Error	SSYER-H	4A	4B	EMA03-H	Emulate Address 03
Double Slave Synchronization Error	DSYER-H	5A	5B	EMA04-H	Emulate Address 04
Load Special Function	LDSPF-H	6A	6B	EMA05-H	Emulate Address 05
Fatal Interrupt	FINTP-L	7A	7B	EMA06-H	Emulate Address 06
Special Function	SPFNC-H	8A	8B	EMA07-H	Emulate Address 07
Panel Halt	HALTP-L	9A	9B	Reserved	
	Reserved	10A	10B	Reserved	
Carry	CARRY-H	11A	11B	Reserved	
	Reserved	12A	12B	Reserved	
Address Error	ADERR-H	13A	13B	Reserved	
Program Status 03	PS003-L	14A	14B	Reserved	
	Reserved	15A	15B	XD007-L	Inhibit Destination File 0 to 7
	Reserved	16A	16B	XD815-L	Inhibit Destination File 8 to 15
	Reserved	17A	17B	XB815-L	Inhibit B-Field File 8 to 15
Control Count Write Enable	CCWEN-H	18A	18B	XB007-L	Inhibit B-Field File 0 to 7
Static Condition	STATIC-L	19A	19B	LITRL-L	Literal
Master Synchronization	MSYN-H	20A	20B	PLUS1-L	Plus 1
Special Function 04	SPF04-L	21A	21B	PSWEN-L	Processor Status Write Enable
B-Bus Inhibit	BBINH-L	22A	22B	IRWEN-L	IR Write Enable
B Bus 01	BB001-H	23A	23B	BB000-H	B Bus 00
B Bus 03	BB03-H	24A	24B	BB002-H	B Bus 02
B Bus 05	BB005-H	25A	25B	BB004-H	B Bus 04
B Bus 07	BB007-H	26A	26B	BB006-H	B Bus 06
B Bus 09	BB009-H	27A	27B	BB008-H	B Bus 08
B Bus 11	BB011-H	28A	28B	BB010-H	B Bus 10
B Bus 13	BB013-H	29A	29B	BB012-H	B Bus 12
B Bus 15	BB015-H	30A	30B	BB014-H	B Bus 14

Name	Signal	Pin	Pin	Signal	Name
Load CC Register	LOADC-L	1A	1B	Reserved	
Bus Request	BREQ-H	2A	2B	MINTP-L	Microinterrupt
Bus Grant	BGRNT-L	3A	3B	BYTDA-L	Byte Data
Bus Grant Enable	BGEN-H	4A	4B	Reserved	
Memory Management Inhibit	MMINH-L	5A	5B	Reserved	
Data Inhibit	DAINH-L	6A	6B	CCCEN-H	CC Count Enable
Special Function 7	SPF07-L	7A	7B	SPR1A-L	Special Register 1A
Special Function 5	SPF05-L	8A	8B	SPR19-L	Special Register 19
Special Function 6	SPF06-L	9A	9B	SPR1B-L	Special Register 1B
Special Function Decode	SPFNC-H	10A	10B	MLTPY-L	Multiply
Inhibit B Field	INHBF-L	11A	11B	ENSFC-H	Enable Special Function
Emulate	EMLAT-H	12A	12B	CR008-H	Microcommand Register 08
Power Failure	PFAIL-L	13A	13B	Reserved	
AU Carry In	AUCIN-L	14A	14B	Reserved	
Write	WRITE-L	15A	15B	FILE6-H	File 6
IR Read	IRERD-H	16A	16B	XA815-L	Inhibit A-Field File 8 to 15
Interrupt	INTR-H	17A	17B	XA007-L	Inhibit A-Field File 0 to 7
Memory Management C0	MMC0-L	18A	18B	RSTRA-L	Restore A
Memory Management C1	MMC1-L	19A	19B	YELLW-L	Yellow
Microcommand Register 07	CR007-H	20A	20B	BYTMD-L	Byte Mode
Stack Limit Interrupt	SLINT-H	21A	21B	MS006-H	Microstatus Register 06
DR Write Enable	DRWEN-L	22A	22B	RRWEN-L	RR Write Enable
Emulate Interrupt Address 01	EIA001-H	23A	23B	EIA000-H	Emulate Interrupt Address 00
Emulate Interrupt Address 03	EIA003-H	24A	24B	EIA002-H	Emulate Interrupt Address 02
Emulate Interrupt Address 05	EIA005-H	25A	25B	EIA004-H	Emulate Interrupt Address 04
Emulate Interrupt Address 07	EIA007-H	26A	26B	EIA006-H	Emulate Interrupt Address 06
Emulate Interrupt Address 09	EIA007-H	27A	27B	EIA008-H	Emulate Interrupt Address 08
Emulate Interrupt Address 11	EIA011-H	28A	28B	EIA010-H	Emulate Interrupt Address 10
Emulate Interrupt Address 13	EIA013-H	29A	29B	EIA012-H	Emulate Interrupt Address 12
Emulate Interrupt Address 15	EIA015-H	30A	30B	EIA014-H	Emulate Interrupt Address 14

APPENDIX B

CDP-XI/35 INSTRUCTION TIMING

The tables in this appendix give approximate instruction-execution times for the CDP-XI/35 emulating representative PDP-11/35 operations. The values given have a tolerance of ±10% and are calculated assuming a 165-ns clock and one CDP-8KX16 Core Memory.

Table B-1. Single-Operand Instruction Timing (Microseconds)

Instruction	Address Mode							
	0	1	2	3	4	5	6	7
JMP	-	1.5	1.8	2.1	2.0	2.3	2.1	2.8
JSR	-	2.8	3.0	3.3	3.0	3.4	3.3	4.0
TST(B)	1.6	2.0	2.6	3.0	2.6	3.1	3.0	3.8
CLR(B)	1.6	2.1	2.5	2.6	2.5	2.8	2.6	3.5
COM(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
INC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
DEC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
NEG(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ASL(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ADC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
SBC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ASR(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ROR(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0

Table B-2. MOV(B) Instruction Timing (Microseconds)

Destination Mode	Source Mode 0	1	2	3	4	5	6	7
0	2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
1	2.5	3.1	3.1	3.8	3.1	3.8	3.8	4.6
2	2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
3	3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.6
4	2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
5	3.1	4.0	4.0	4.6	4.0	4.6	4.6	5.4
6	3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.3
7	3.6	4.5	4.5	5.1	4.5	5.1	5.1	5.9

Table B-3. Typical Double-Operand Instruction Timing (Microseconds): BIS(B), BIC(B), ADD, SUB

Destination Mode	Source Mode 0	1	2	3	4	5	6	7
0	2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
1	3.1	3.8	3.8	4.5	3.8	4.5	4.5	5.3
2	3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
3	3.6	4.3	4.3	4.9	4.3	4.9	4.9	6.1
4	3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
5	3.8	4.5	4.5	5.1	4.5	5.1	5.1	5.9
6	3.6	4.3	4.3	5.0	4.3	5.0	5.0	5.6
7	4.9	4.9	4.9	5.6	4.9	5.6	5.6	6.4

Table B-4. Control, Branch and Miscellaneous Instruction Timing

Instruction	Time (microseconds)
Conditional Branch	1.5 for branch 2.0 for no branch
RTS	2.1
RTI	3.0
RTT	3.1
Traps	5.6
Branch (BR)	1.7
SCC	1.5
CCC	1.5
HALT	1.5
MARK	2.3
SOB	1.6 for branch 1.5 for no branch
WAIT	1.3 (interrupts checked every 0.33 microseconds)