



**CONTROL DATA®
COMPUTER SYSTEMS
CORDWOOD MODULES**

MODULES A-J

Volume 1 of 3

PRINTED CIRCUIT MANUAL

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

RECORD of REVISIONS

REVISION	NOTES
A thru F	Affects Volumes 1 and 2 only (60042900).
G	6600 Information and Circuit Module Schematics added as Volume 3.
H (5-7-65)	Vol. 3, addition of revised Record of Revisions. Replace the following revised pages: 6600-4, 6600-5, 6600-8, 6600-14, and add new pages 6600-15, 6600-16 and schematics MK and AC.
J (10-1-65)	Change Order CA11567. Major revision to this manual obsoleting all previous editions.
K	Publication Change Order CA13034. Title changed to Printed Circuit Manual Cordwood Modules.
(3-15-66)	Vol. 1, A-J; Vol. 2, K-U; Vol. 3, V-Z. Introduction revised. Printed circuit card information added and reorganized. This printing obsoletes all previous editions.
L (9-9-66)	Engineering Change Order 13534. Modules XL01 thru XL10 revised.
M	Field Change Order 13812. Module Z07 revised.
N (9-9-66)	Engineering Change Order 13441. Modules V17 and V43 revised.
P (9-9-66)	Publications Change Order 14574. To incorporate corrections and additions.
R (11-22-66)	Publications Change Order 15171. To incorporate corrections and additions.
S (3-2-67)	Publications Change Order 15937. To incorporate corrections and additions.
T (5-12-67)	Publications Change Order 16432. To incorporate corrections and additions.
U (7-21-67)	Publications Change Order 16938. To incorporate corrections and additions.
V (3-13-68)	Publications Change Order 17486. To incorporate corrections and additions.
W (3-13-68)	Publications Change Order 18211. To incorporate corrections and additions.
Y (3-13-68)	Publications Change Order 18883. To incorporate corrections and additions.
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AA	Engineering Change Order 24619, document change only.
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AB (5-5-70)	Engineering Change Order 25341, publications change only. To incorporate corrections and additions.
AC	Engineering Change Order 26839. No change to this manual.
(11-15-71)	
AD	Field Change Order 26792. RDZ and REN Modules added.
(11-15-71)	
AE	Field Change Order 26611. REJ Module added. Also to incorporate corrections and additions.
(11-15-71)	
AF (4-10-72)	Engineering Change Order 30954. Pages LX, RCT, TCW, RDS, REM, REX, V17, ZO, ZR, ZS, ZT, are revised.
AG	Manual revised; includes Engineering Change Order 30804. RFM module is added.
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AH	Engineering Change Order 30429. No change to this manual.
(9-8-72)	
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REVISION LETTERS I, O, Q AND X ARE NOT USED

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RECORD of REVISIONS (CONT'D)

PREFACE

The logic schematic diagrams of cordwood modules are entered into these volumes in alpha-numeric sequence. The logic schematic pages in these volumes are updated when the LS page of the engineering document (number at top of each logic schematic) is changed by revision. The revision letter of the engineering document shown at the top of each schematic is not changed in this manual when only parts list pages of the document are revised.



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INTRODUCTION

CIRCUITS

The circuits of most CONTROL DATA* cordwood modules use the inversion property of transistors to obtain logical OR and AND configurations. Two inverters may also be cross-connected, input to output, to form flip-flops (FFs) for storing data temporarily. Special circuits drive twisted-pair or coaxial-cable transmission lines, control storage or read out of data in the magnetic core memory, amplify and detect magnetic tape or disk file head signals, and control other functions.

PACKAGING

Circuits are packaged in modules (Figure 1) which use printed circuit wiring. Circuit components are mounted on and between two printed circuit boards in a method referred to as "cordwood packaging". A double-rowed 30-pin connector fastened at one end of the module allows electrical access to the circuits. The module connector mates with a chassis connector, the pins of which are wired to other similar circuits. An anodized aluminum plate with captive screws is fastened to the module at the end opposite the connector. This plate fastens the module to the chassis mechanically and carries the identifying number and/or letter for the module and six test point terminals. The test points are numbered one through six from top to bottom and are connected to various parts of a circuit to allow circuit operation to be viewed on an oscilloscope.

COOLING

Two modes of cooling are used: freon and air. Although the modules are mounted differently in each case, any module currently in production may use either mode simply by changing its face plate. Figure 1(A) shows a freon-cooled module, while 1(B) shows an air-cooled module.

Freon Cooling

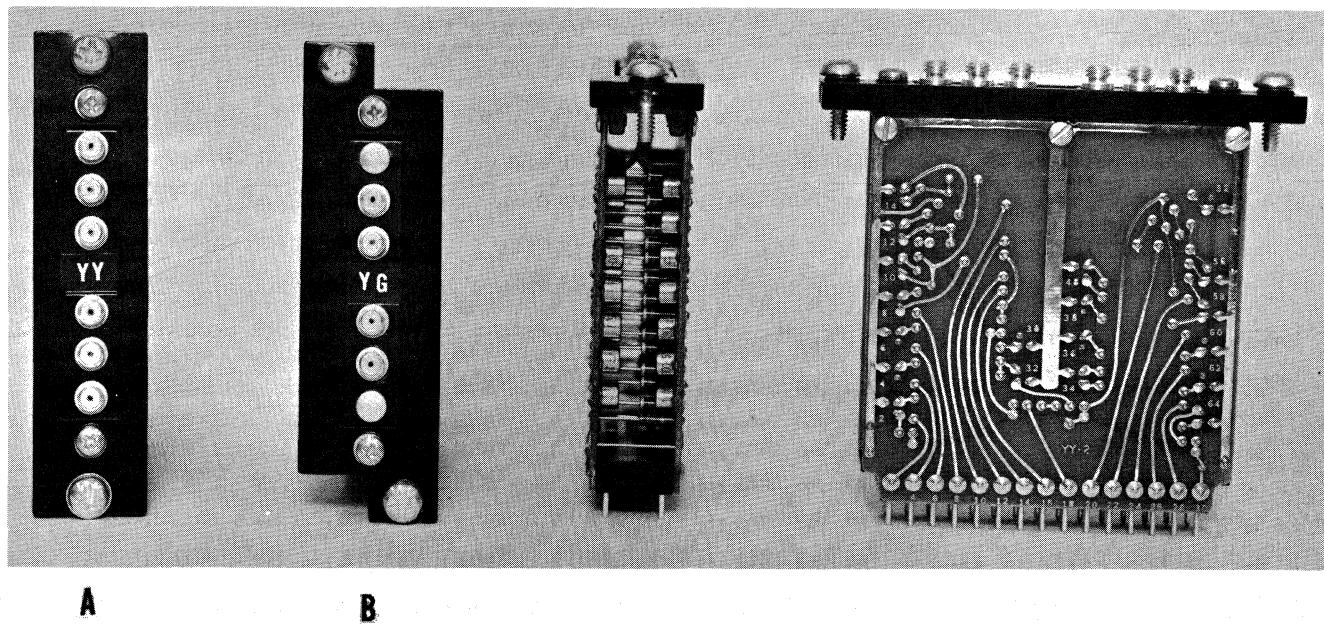
Modules are mounted vertically in the chassis in separate compartments. Compartment side walls, the connector (back), and module plate (front) have a black finish. Rows of modules are separated and supported by metal plates which form the top and bottom of the compartments. A copper tube imbedded in each bar is connected to a

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freon refrigeration system. Component heat from each module is carried to the cold bars and cooling system by convection and by conduction. Blank module locations are covered by a plate but if large sections are unused in the chassis, a heat dissipation module (formerly type XO, now module type WZ) is used about every fourth location (6400 and 6600 Computer Systems use this type of cooling).

Air Cooling

Modules are mounted vertically but without compartment side walls. They are supported at the top and bottom by bars at the front of the chassis. Air is forced up through the modules and may or may not be refrigerated. Blank module locations are covered with a plate.



1927

Figure 1. Cordwood Modules

BASIC CIRCUIT ANALYSIS

The basic circuit is a single NPN silicon transistor connected in a grounded emitter amplifier circuit (Figure 2). The transistor operates from a +6 vdc supply. The inherent 180° phase shift of the transistor provides the basic inversion (or NOT) function.

The two signal levels and their logical significance are:

$+0.2\text{v}$	=	"1"
$+1.2\text{v}$	=	"0"

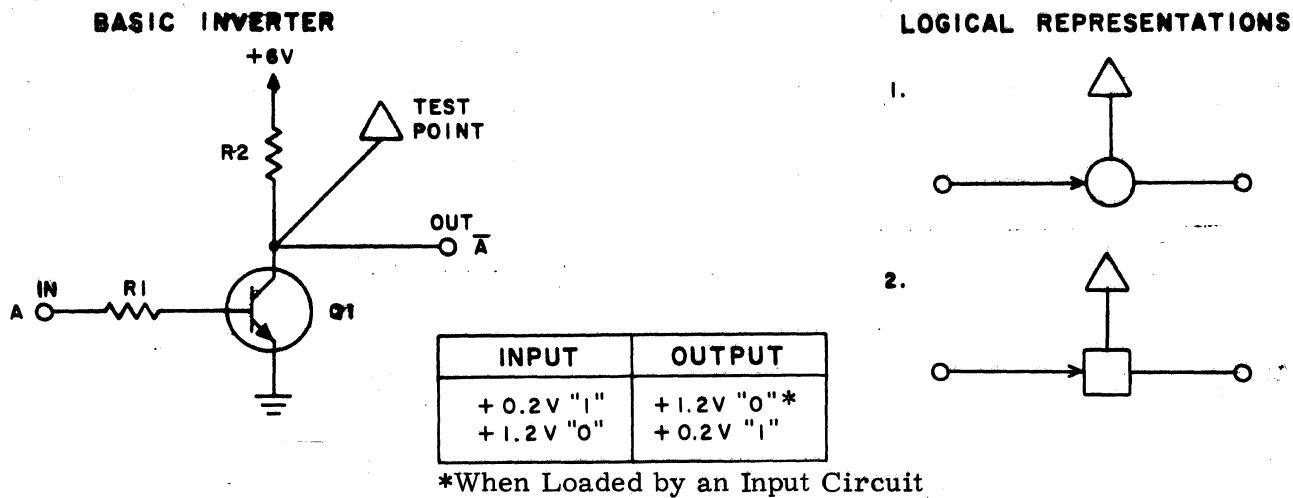


Figure 2. Basic Inverter

A $+1.2\text{v}$ input turns on the transistor and drives it to saturation. The output signal is then the drop across the transistor, $+0.2\text{v}$. When a $+0.2\text{v}$ input cuts off the transistor the output rises toward $+6\text{v}$ but is held to $+1.2\text{v}$ by the voltage-dividing effect of the collector resistor and the input resistance of the driven load.

The threshold voltage on the base of the transistor is approximately $+0.8\text{v}$ (virtually no conduction below $+0.7\text{v}$) which permits the circuit to reject noise signals up to about $+0.5\text{v}$. Circuit parameters for cutoff and saturation are listed below.

	V_B	V_C	I_B (min)	I_C	Average Switching Time
Cutoff	0.2	1.2	0	0	4 or 5 nsec
Saturation	0.8	0.2	1 ma	10 ma	

AND and OR Combinations

To combine signals from two circuits, the collectors are connected to a common load resistor, as in Figure 3. This provides $\overline{A} + \overline{B} = \overline{AB}$ as the output signal. This method of combining signals is sometimes called NAND logic. (The name derives from NOT

AND since the circuit consists of an AND with phase inversion or negation of the output.) Up to six transistors may be connected to a common collector resistor in this way.

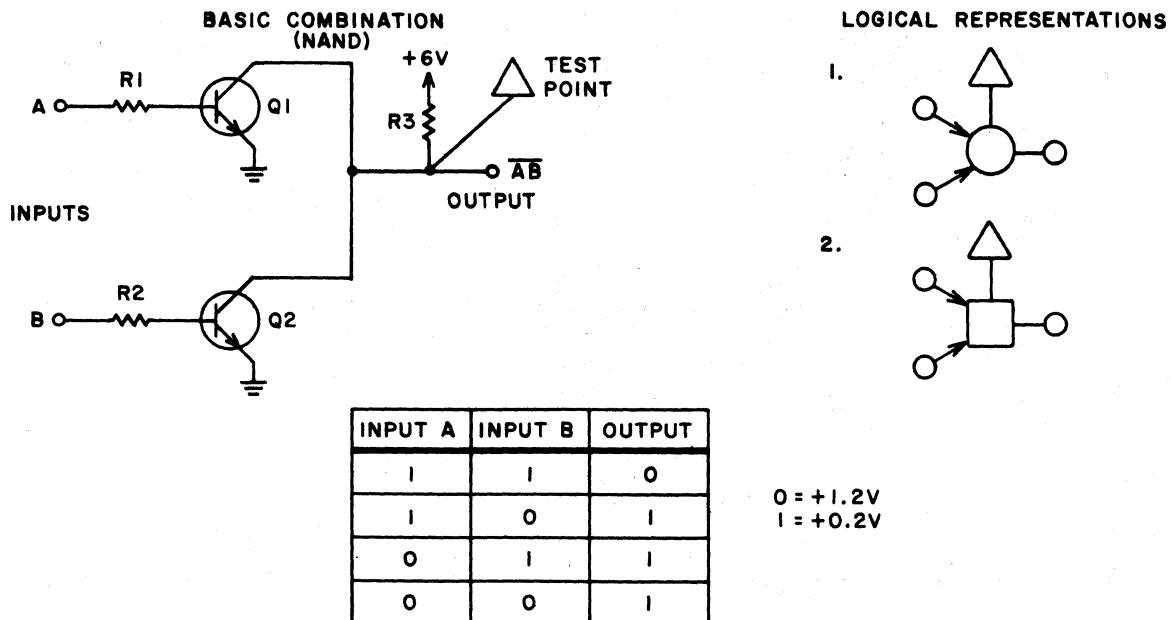


Figure 3. Basic (NAND) Combination

A circuit showing the basic AND combination appears in Figure 4. When either input A or input B is +1.2v, Q1 or Q2 is biased to saturation and the potential at point C is +0.2v. This in turn cuts off Q3 and the output is +1.2v. But when both inputs A and B are +0.2v, both Q1 and Q2 are cut off, and the potential at point C goes to +1.2v*. With point C at +1.2v, Q3 conducts into saturation, forcing the output to +0.2v. Hence, the output is +0.2v only when both inputs A and B are +0.2v.

The circuit of Figure 5 shows the OR combination of two signals A and B, in which a +1.2v at either input A or B results in a +0.2v output.

*It should be noticed that point C is +1.2v only when R4 and Q3 are present as a load to the circuit. Otherwise point C would rise to +6v.

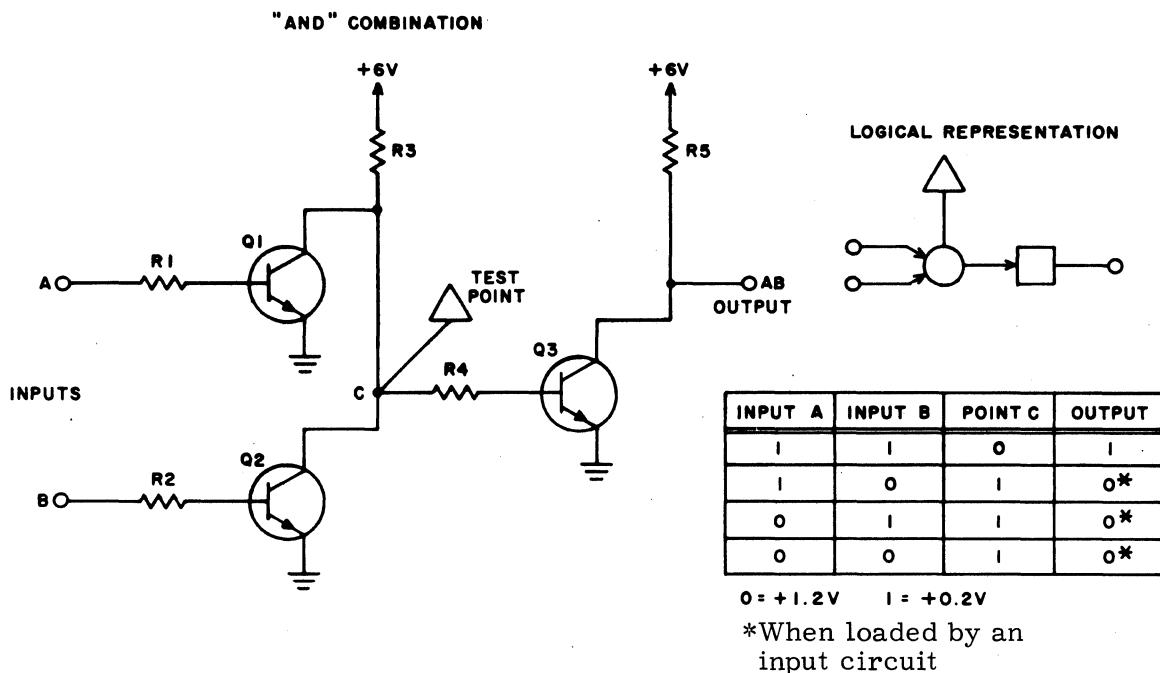


Figure 4. AND Combination

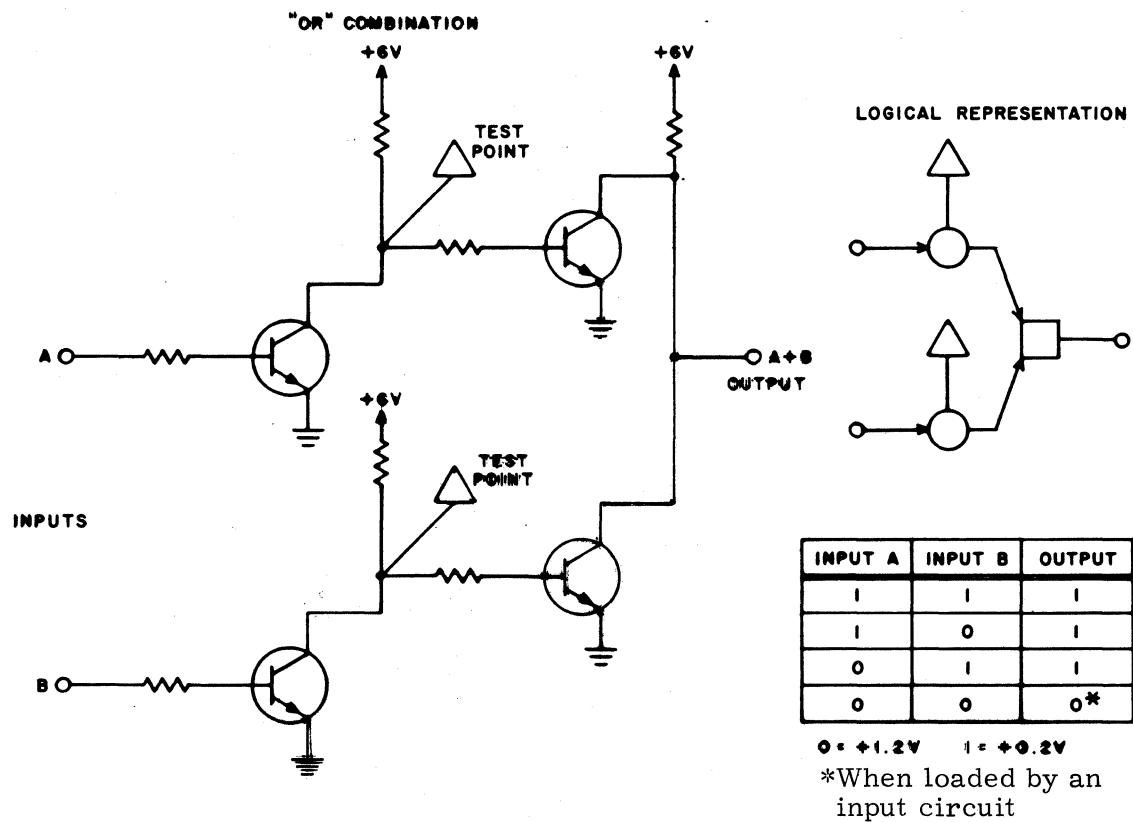


Figure 5. OR Combination

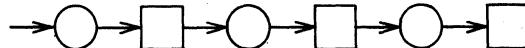
Logic Diagram Symbols

The symbols used to represent circuits on logic diagrams are as follows:

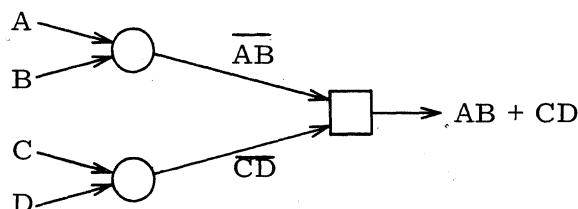
<u>Symbol</u>	<u>Literal Significance</u>
→	transistor (including its base resistor)
□	collector load resistor
○	collector load resistor

The use of two symbols, circle and square, to represent the combining of signals is a convenient way to indicate alternating logical levels. This alternation results from the inversion accompanying each successive combination. Logic is performed by a succession of steps: invert, combine, invert, combine, invert, combine, etc.

A diagram of such a logical string of steps appears as:



Where possible, diagrams have circles and squares appearing in alternation and in such a way as to indicate whether the effect of a combination is an AND or an OR. Consider the logical circuit shown below:



Its output is $\overline{AB} \cdot \overline{CD}$ which simplifies to $AB + CD$. The square may be thought of as representing an OR.

Flip-Flop with Clear/Set Input

The circuit of a flip-flop and its clear/set input is shown in Figure 6. The basic flip-flop may have up to five set inputs and five clear inputs; in this example only one of each are shown. The set input is fed by a 3-way AND gate, of which one input comes from the clear/set network.

The clear/set network enables the flip-flop to be cleared and reset by the same gating pulse. In many cases, this will be a 25 nanosecond clock pulse. Figure 7 shows the logical representation of this circuit and a timing chart for the clear/set operation.

A +0.2v "1" clear/set input to point 1 results in +0.2v "1" outputs from B and E. This simultaneously clears the flip-flop while enabling AND gate C to reset it, if "1" inputs are present at points 2 and 3. Assuming "1" inputs, the +1.2v "0" output of C drives the output of D to a +0.2v "1". In this state, D and E both are producing "1" outputs and flip-flop is an indeterminate condition. However, when the clear/set pulse drops, the "1" output from A allows E to switch to "0", providing feedback to D which holds the flip-flop in the set condition. Meanwhile, the "0" output of B has forced C to remove the set input from D, but the delay time through B and C will allow the set input to stay up long enough after the clear input drops so that the flip-flop assumes the set state.

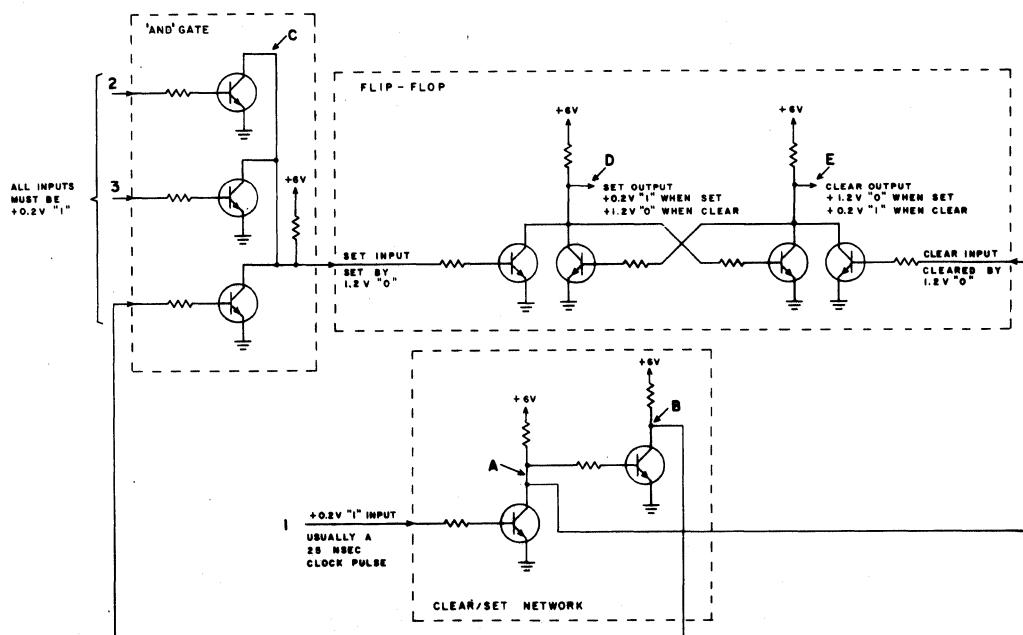
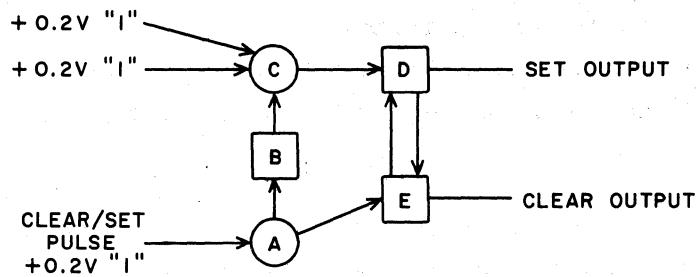


Figure 6. Basic Flip-Flop with Clear/Set Input

LOGICAL
REPRESENTATION:



(INVERTER DELAY ASSUMED 5 NANOSECONDS)

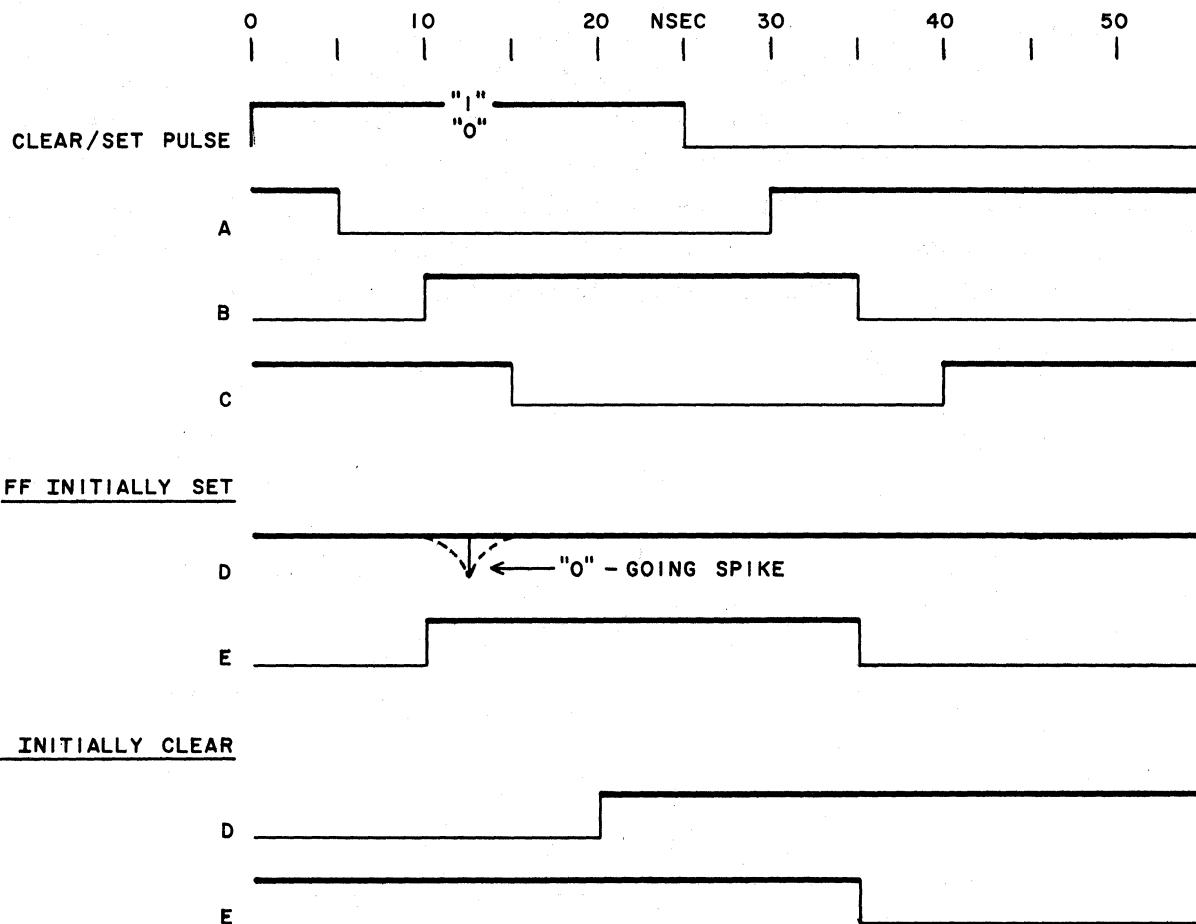


Figure 7. Flip-Flop Logical Representation and Timing Chart

Circuit Loading

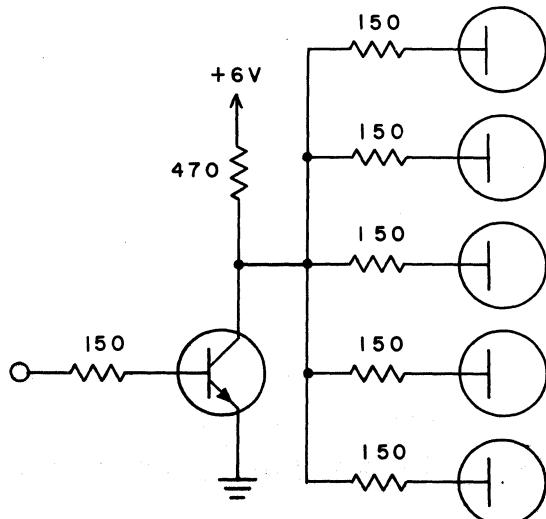
One circuit, which may be a common collector connection of several transistors, can drive several other transistors which may be on the same module, on a separate module, or a combination of the two. Figure 8 shows examples of loading.

A circuit may drive up to five transistors when all transistors (including driver) are on the same module. This loading limitation is due to variations in base threshold voltage and corresponding base current demands. For each load configuration, the driver collector resistor and base resistors of the driven transistors are adjusted to balance and limit the base currents. This loading arrangement allows ample slave networks to provide multiple outputs.

The following table lists component variations for circuit loading within a module.

	Driver Collector Resistor	Base Resistor of Driven Transistors
1 Load	680	47
2 Loads	680	100
3 Loads	680	150
4 Loads	560	150
5 Loads	470	150

TYPICAL FAN-OUT



LOGICAL
REPRESENTATIONS

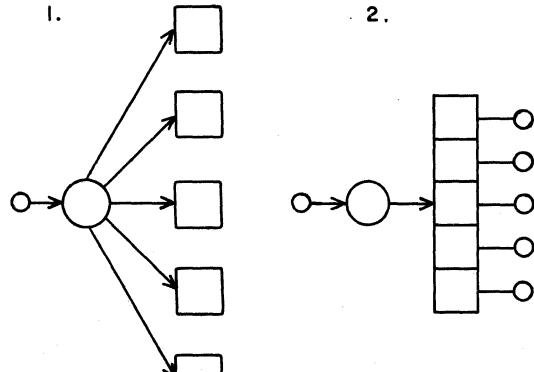


Figure 8. Base Resistor Loading

Other load limits apply when the circuit load is on a separate module. A circuit can simultaneously drive up to two transistors on the same module and up to two transistors on a separate module. Loading in this case accounts for the loss on the transmission line connecting the two modules as well as variations in base threshold voltage noted earlier. The significance of this loading scheme is presented in the discussion on line drivers.

The following table lists component variations for a transistor driving loads within the same module, in addition to the twisted-pair line.

Number of Local Loads	Driver Collector Resistor	Output Line Resistor	Base Resistor of Driven Transistors	Output Shunt to Ground
None	470	56	---	120 plus diode
1	470	56	100	---
2	470	56	220	---

Line Drivers

Modules which are located on the same chassis are connected with twisted pair lines; modules located on separate chassis are connected by coaxial cable. Line driver circuits are provided for each type of transmission line.

Twisted-Pair Driver: The twisted pair driver is shown in Figure 9. Initially, consider Q1 conducting so that its collector is at +0.2v. With Q2 off, the transmission line is terminated in an open circuit.

A +0.2v "1" input causes the collector of Q1 to rise to +1.2v. This voltage is greater than the +0.8v diode threshold, and a part of the resulting current drawn through R2 is diverted through R3 and CR1 to ground. The remaining current passes R4 and is placed on the line.

A finite time later this wavefront reaches the end of the line and appears at the input to R5, the base resistor for Q2. Since, at this instant, the voltage at the base of Q2 is +0.2v, this voltage adds to the incoming wavefront to result in a voltage of approximately +1.2v at the input to R5.

At the next instant, the Q2 threshold is exceeded and base current flows.

Transmission line theory shows that power is reflected back to the source when the line is terminated in a load which does not absorb all of the transmitted power. The reflected current is shunted to ground by diode CR1. In the absence of CR1, the line voltage would rise to the +6v source.

The low base current, resulting from the line mismatch, retards the build-up of ground noise which occurs as a result of large ground currents.

The shunt diode and series resistor R3 are replaced by a transistor and its base resistor when it is necessary to drive a circuit on the same chassis and a circuit on another chassis. The transistor and diode thresholds are nearly alike so that circuit operation follows the same principle.

The time required by the wavefront to travel down the line is a function of the type of line and its length. The twisted pair line provides a delay of 1.3 nsec per foot. The clock system, for example, uses this feature to establish the 25 nsec duration of clock pulses.

The twisted pair driver is represented on the logic diagrams by the standard square or circle. However, the output of the square or circle is connected to a pin of the module in question and wired from there to a pin on another module. The ground wire of the pair is wired to the connector ground bus of each module.

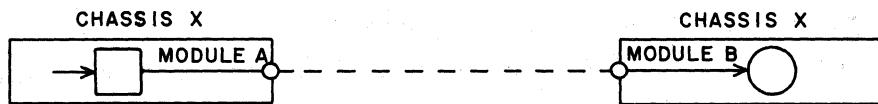
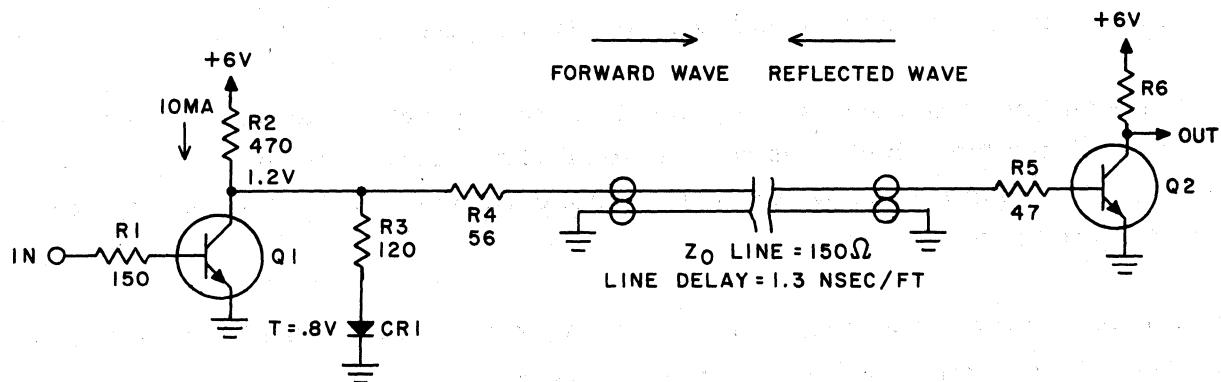
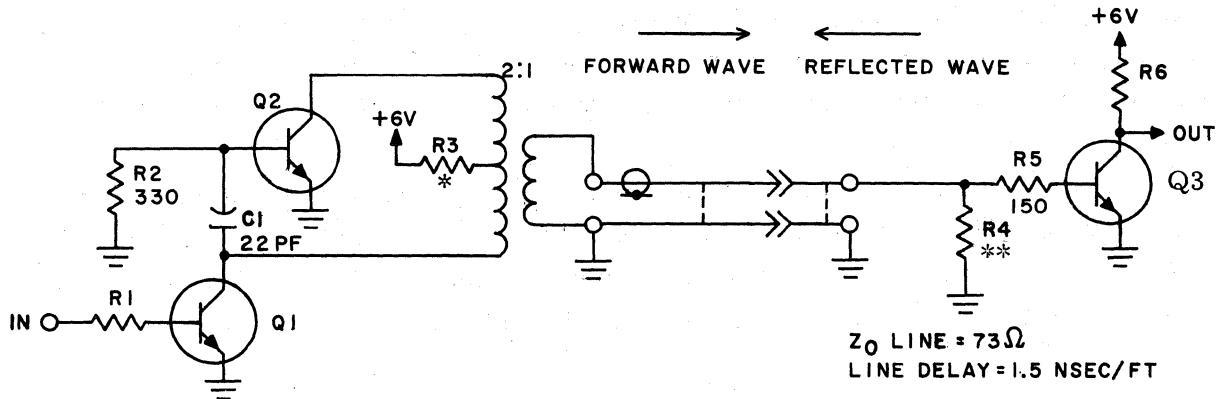


Figure 9. Twisted Pair Driver Circuit



* R3 is 150 ohms or 120 ohms (120 ohms in newer modules).

** R4 is 68 ohms or 82 ohms (82 ohms in newer modules).

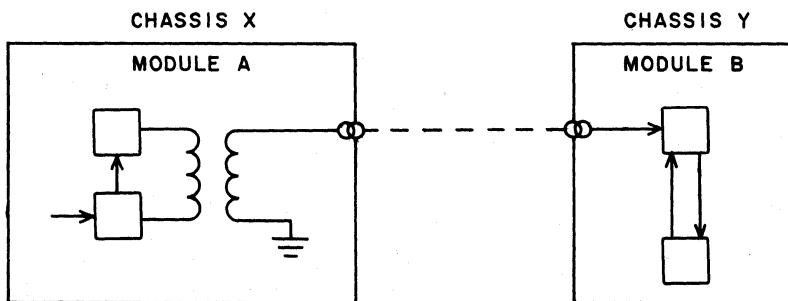


Figure 10. Coaxial Cable Driver Circuit

Coaxial Cable Driver: The coaxial cable driver is shown in Figure 10. All transmissions between chassis are 25 nsec pulses on coaxial cables.

Initially, Q1 and Q2 are off so that their collectors are at the source voltage, +6v. No current flows in either primary winding. When Q1 is turned on, a current flows in the transformer primary winding to which its collector is connected. The voltage drop across R3 and step-down action of the transformer (and transformer loss) produce a voltage pulse on the secondary winding. The pulse duration on the line follows the 25 nsec pulse on the base of Q1. This pulse travels down the coaxial cable and turns transistor Q3 on. Resistor R4 terminates the line in either 68 ohms or 82 ohms.

Capacitor C1 couples the change in Q1 collector voltage to the base of Q2. Capacitor C1, R3, R2, and the base/emitter diode of Q1 will cause Q2 to conduct about 25 nsec later than Q1. When Q2 conducts, current flows in the primary winding to which the Q2 collector is connected. The resulting signal in the transformer secondary is equal to but of opposite polarity from the previous signal and lags by 25 nsec. The net effect of this is to provide an equal and opposite magnetizing force in the transformer for each pulse. This prevents the transformer from building up a bias on the line which could occur under the high switching rates.

The coaxial cable driver circuit is represented on logic diagrams as shown in Figure 10. The time delay on the 75 ohm coaxial cables is 1.5 nsec per foot. All coaxial cable lengths are standardized at 10 feet to allow synchronous timing signals on all chassis. Coaxial cables pass directly through a chassis feed-through connector (without soldering) and connect directly to the transmitting or terminating circuit.

**STORAGE
MODULE**

FUNCTION PIN

Address

S ⁰	22
S ¹	20
S ²	8
S ³	10
S ⁸	12
S ⁹	14
S ¹⁰	18
S ¹¹	16

Store

Z ²	6
Z ³	26
Z ⁶	28
Z ⁷	4
Z ¹⁰	30
Z ¹¹	2

Read

2 ⁰	1
2 ⁰	3
2 ¹	27
2 ¹	29
2 ⁴	5
2 ⁴	7
2 ⁵	23
2 ⁵	25
2 ⁸	19
2 ⁸	21
2 ⁹	9
2 ⁹	11

Inhibit

S ¹¹	24
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Power

+5 To Inhibit	13
+5 To Inhibit	17
Ground	15

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JACK PIN LG

FUNCTION PIN

Address

S ⁴	7
S ⁵	9
S ⁶	13
S ⁷	11

Store

Z ⁰	29
Z ¹	5
Z ⁴	27
Z ⁵	1
Z ⁸	3
Z ⁹	25

Read

2 ²	28
2 ²	30
2 ³	2
2 ³	4
2 ⁶	6
2 ⁶	8
2 ⁷	24
2 ⁷	26
2 ¹⁰	10
2 ¹⁰	12
2 ¹¹	20
2 ¹¹	22

Inhibit

S ⁴	15
S ⁵	17
S ¹⁰	19

Control

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Write Enable	21

Power

+8 To Drive	18
+6 To Drive	14
Ground	16

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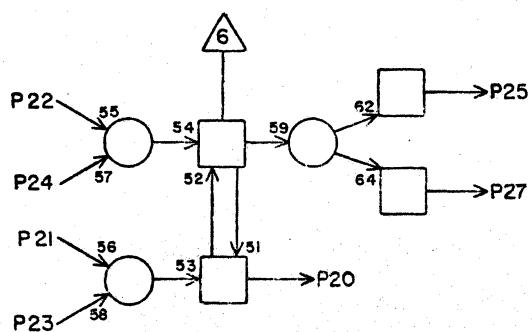
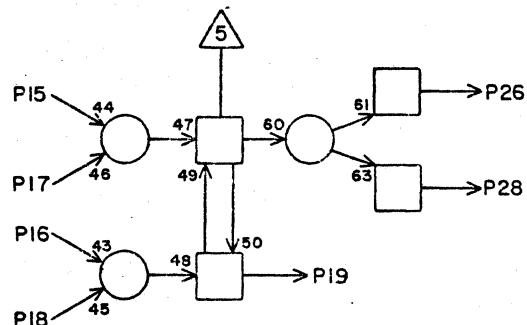
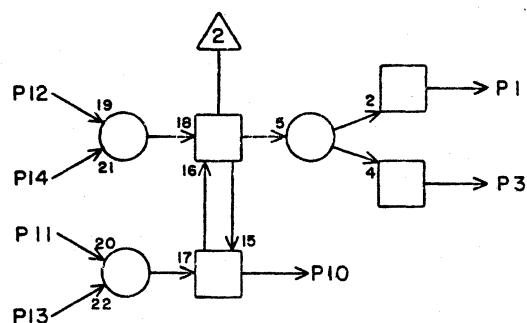
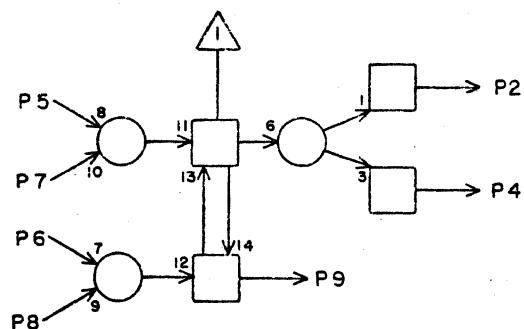
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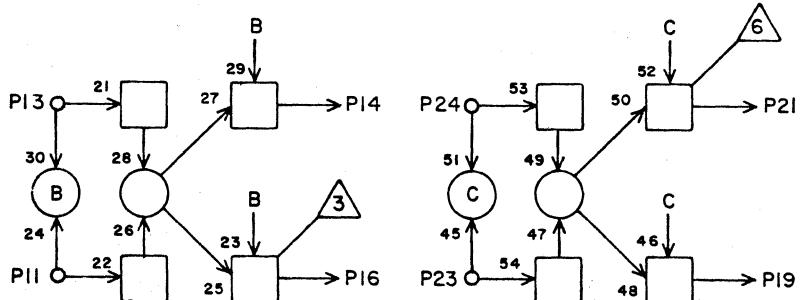
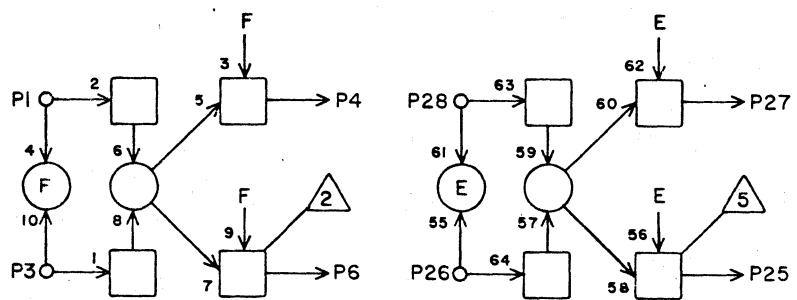
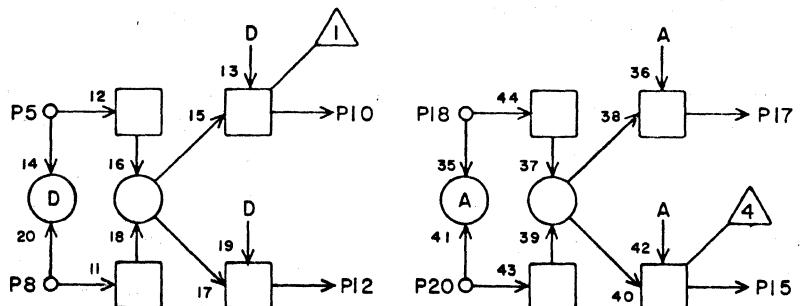
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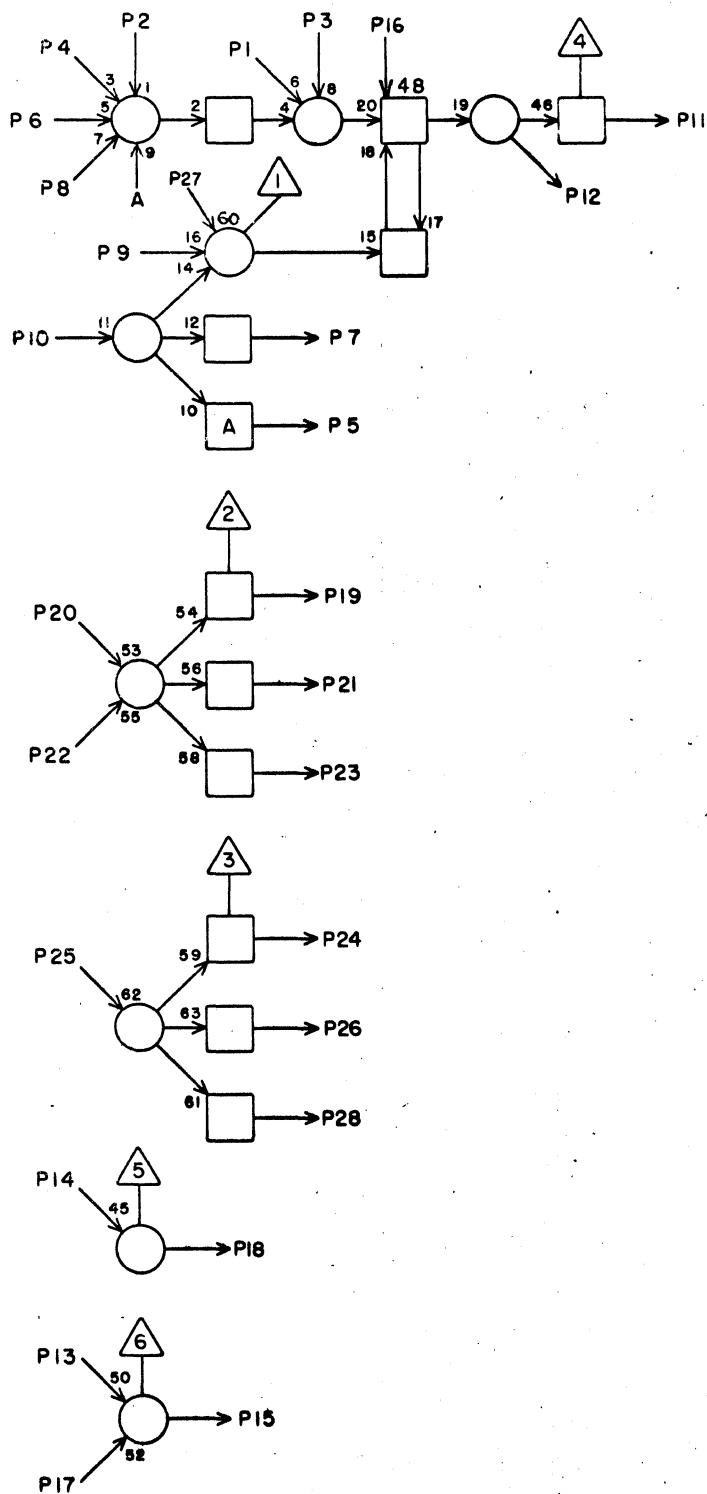
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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JACK PIN LG

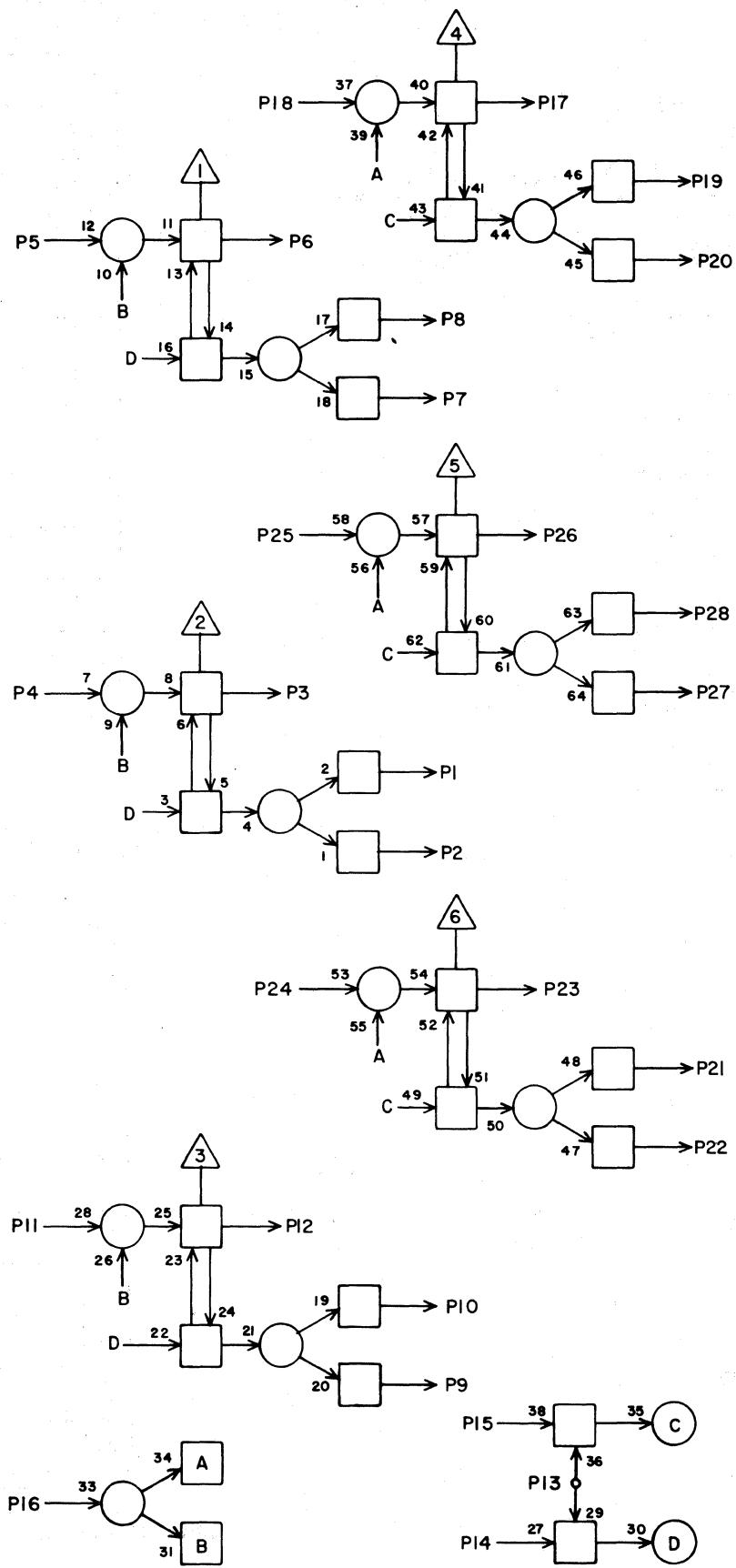
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

LS 63040300
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JACK PIN LG

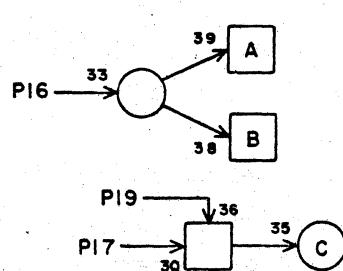
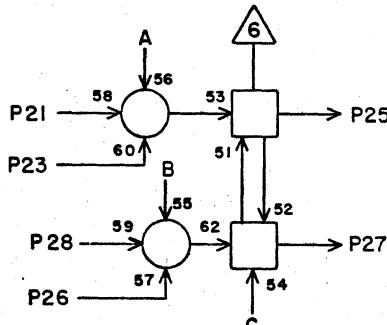
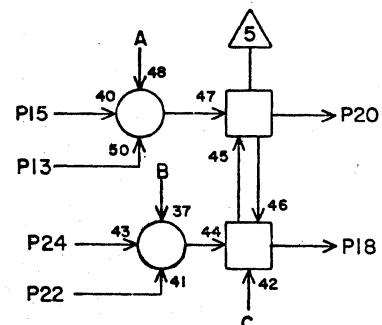
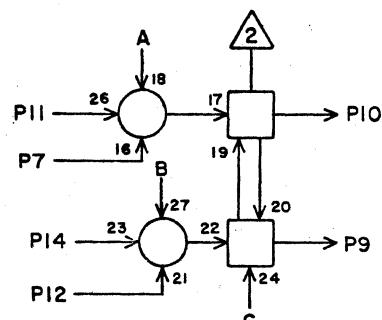
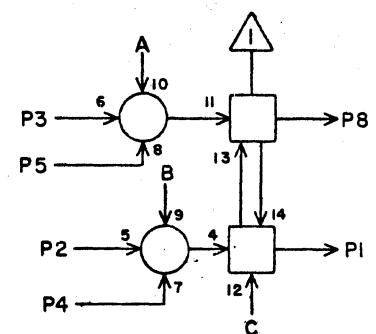
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

LS 63040400
ASSY

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JACK PIN LG

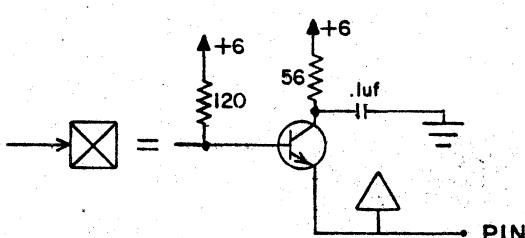
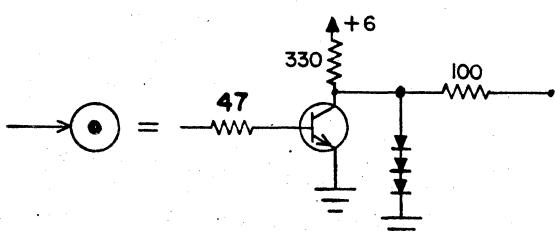
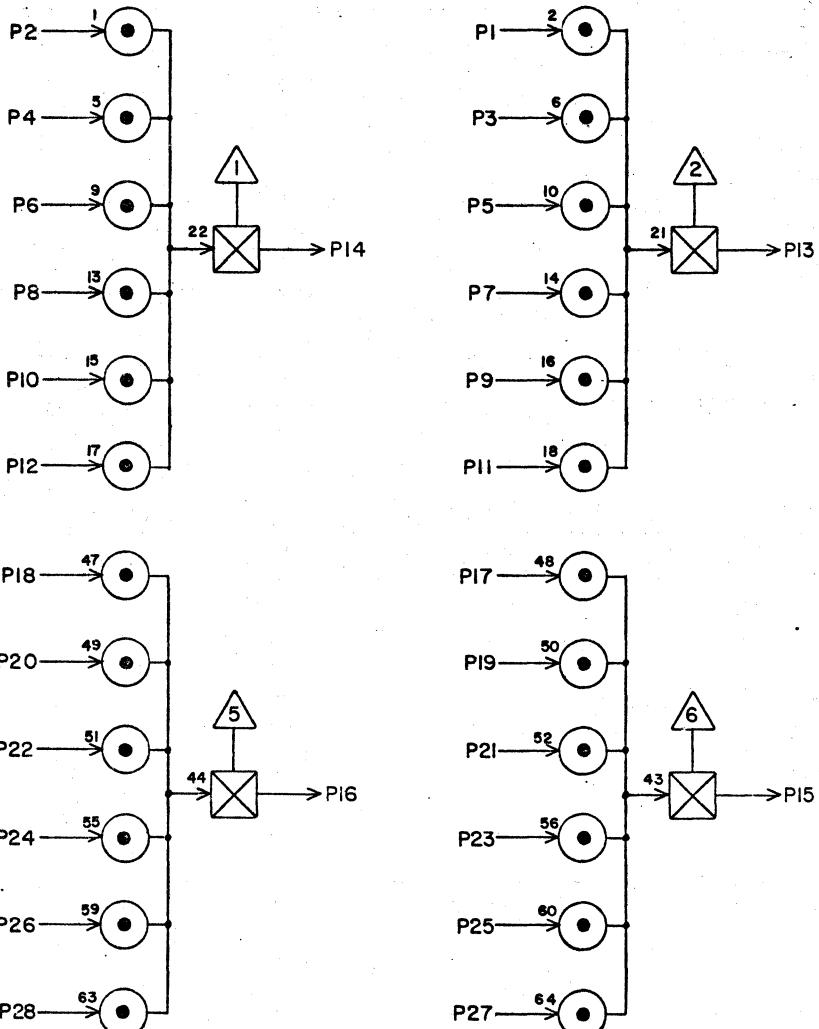
CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

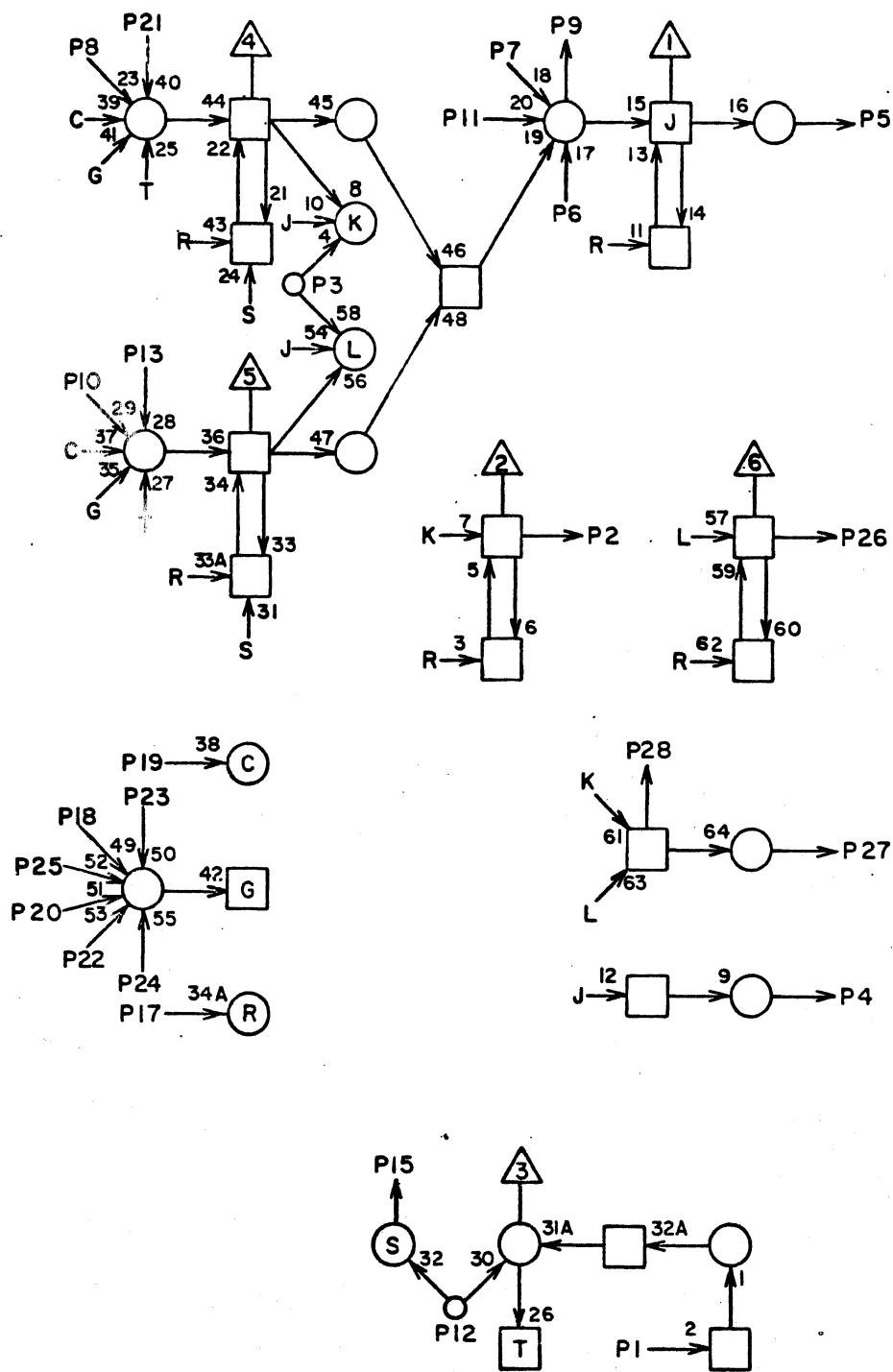
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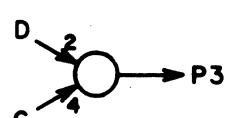
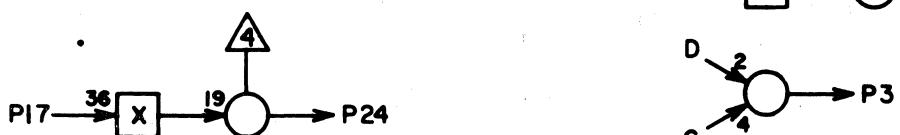
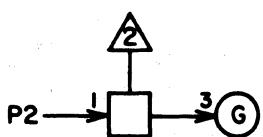
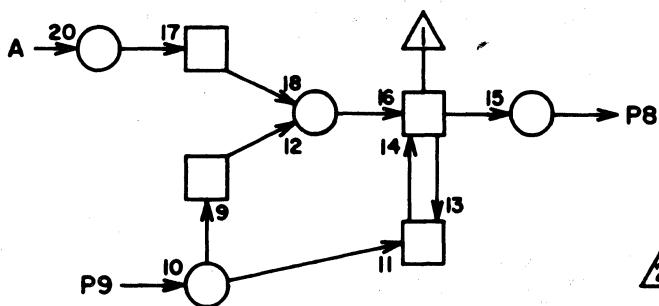
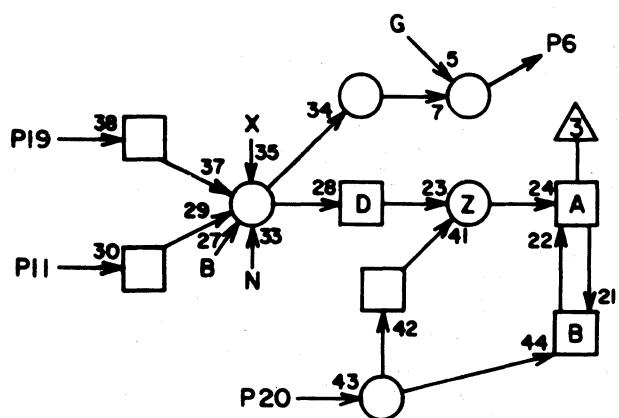
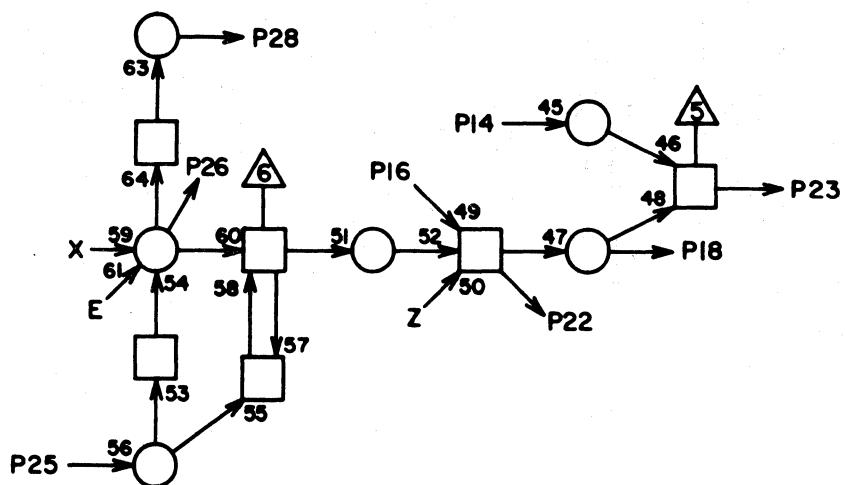
JACK PIN LG

SEE CIRCUIT SPECIFICATION

11827600
60042700 Rev. V

LS 18056700 B
ASSY REV

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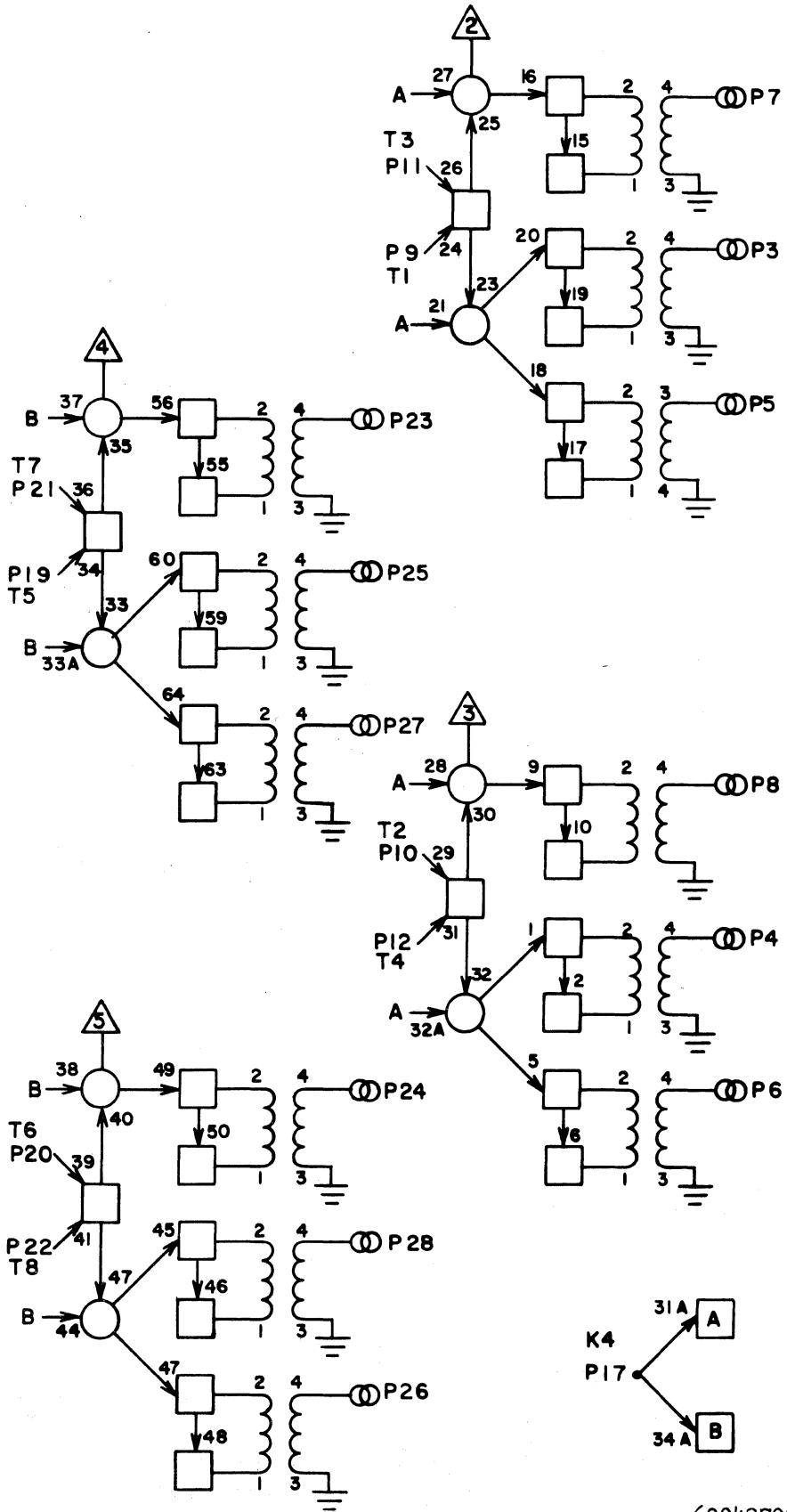
JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev. P

LS 18056900
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JACK PIN LG

SEE CIRCUIT SPECIFICATION

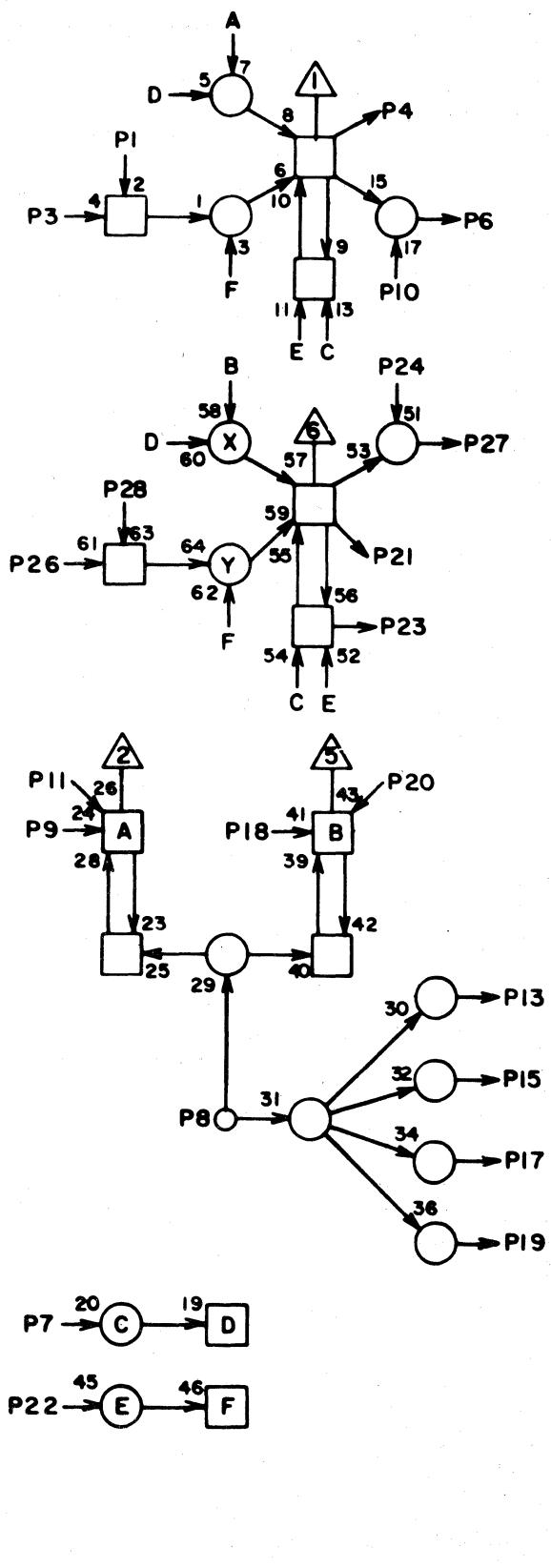
60042700 Rev. K

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LS 18057100

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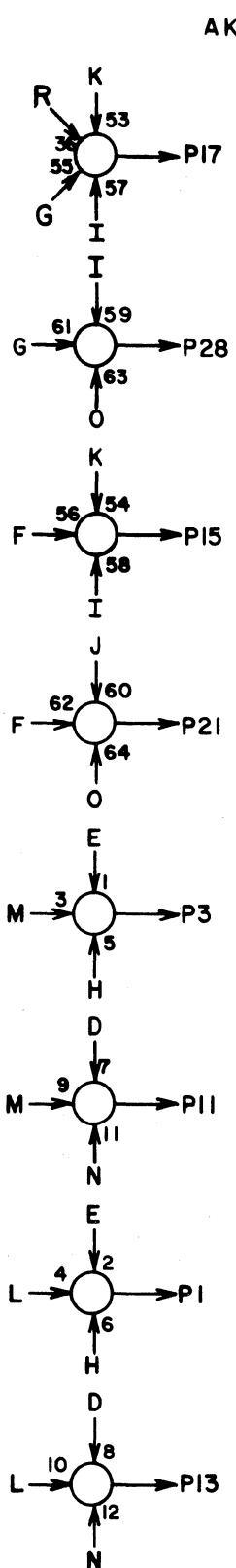
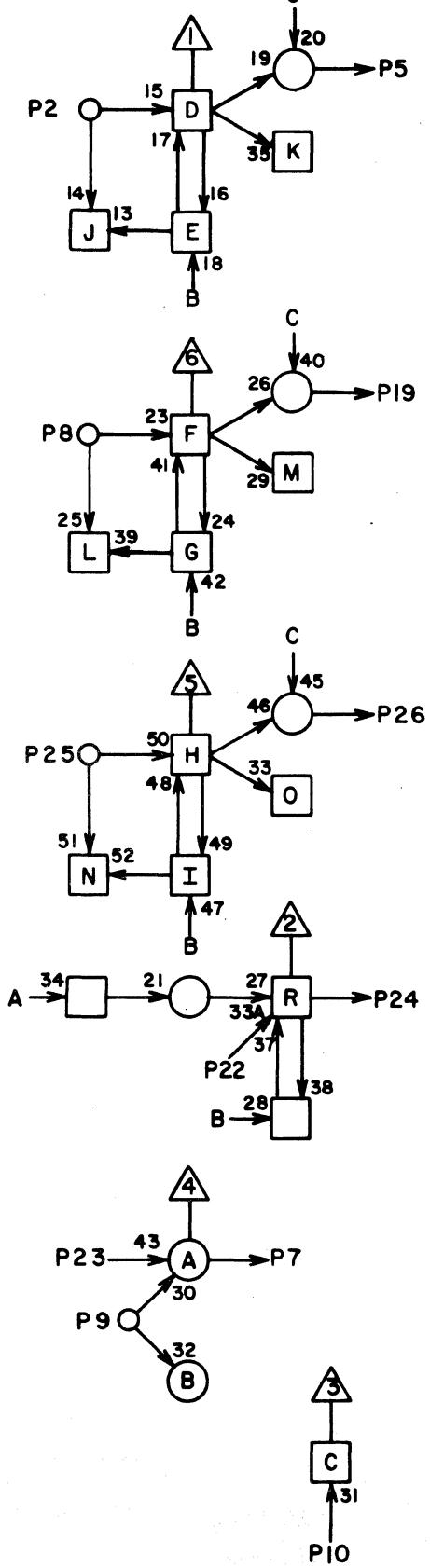
JACK PIN LG

SEE CIRCUIT SPECIFICATION

11827600

60042700 Rev. P

LS 18057300 C
ASSY REV



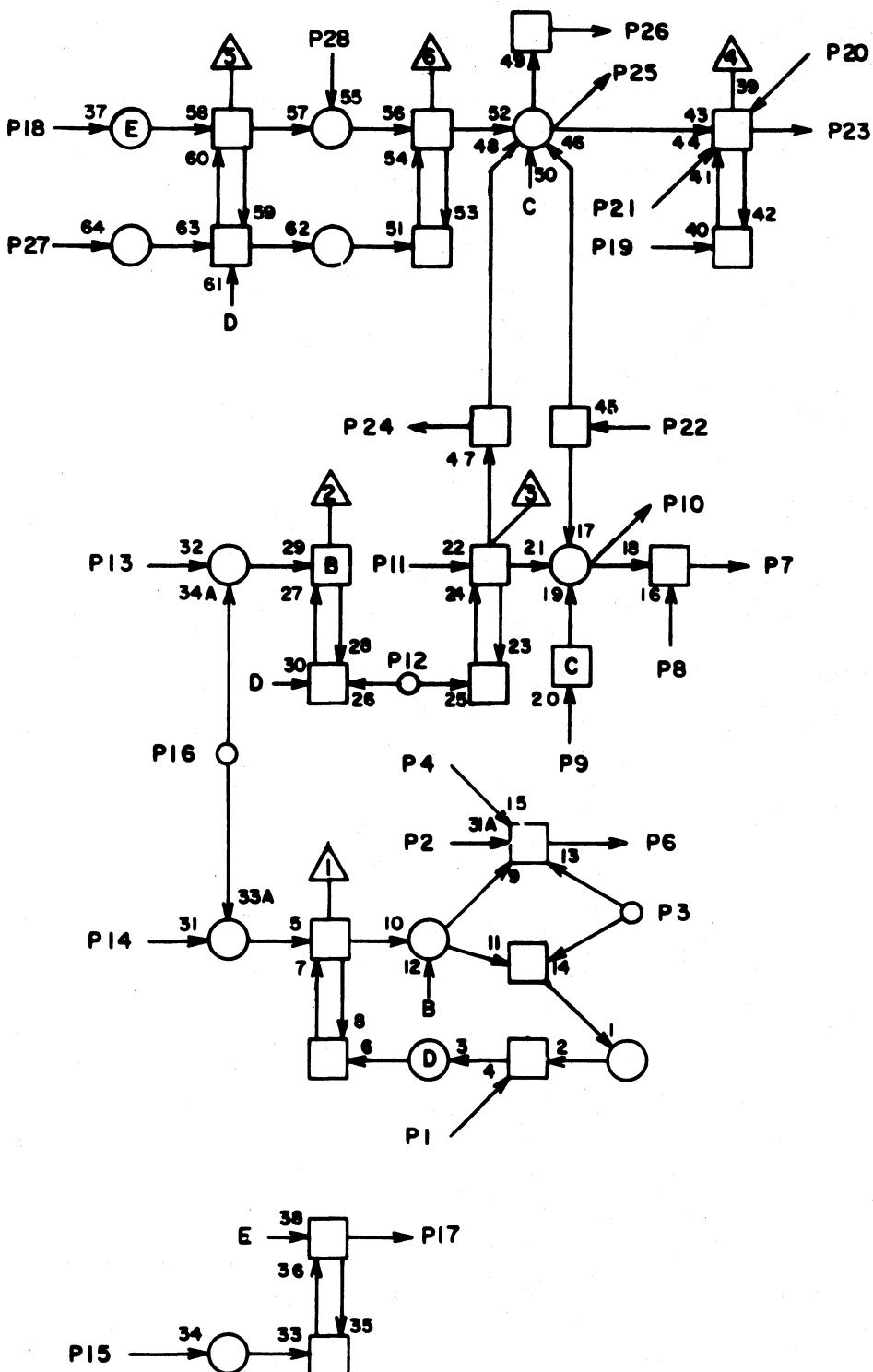
SEE CIRCUIT SPECIFICATION

11827600
60042700 Rev. R

LS 18057500
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JACK PIN LG

SEE CIRCUIT SPECIFICATION
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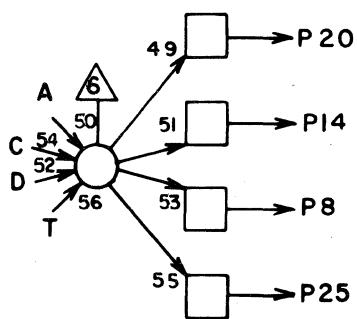
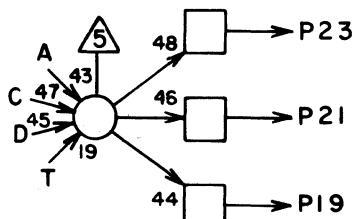
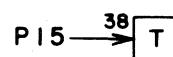
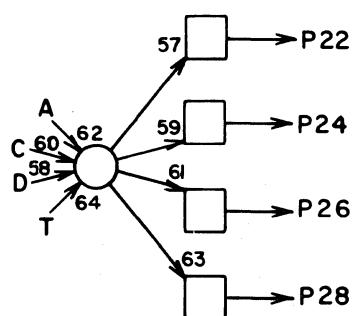
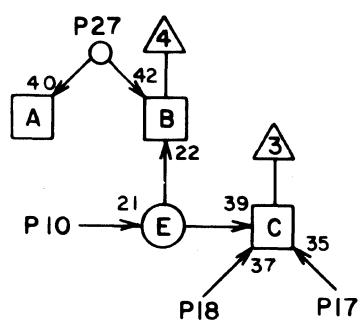
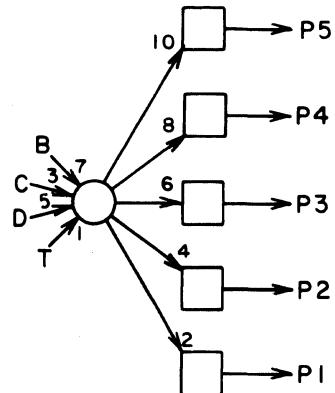
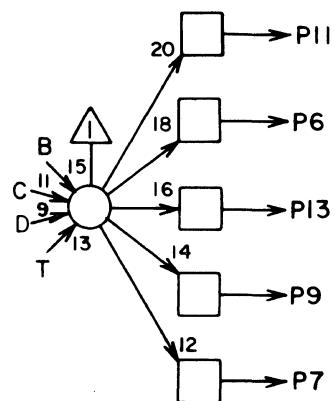
60042700 Rev. P

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JACK PIN LG

SEE CIRCUIT SPECIFICATION
11827600

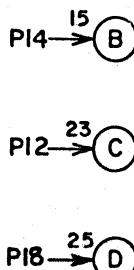
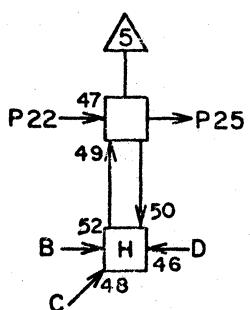
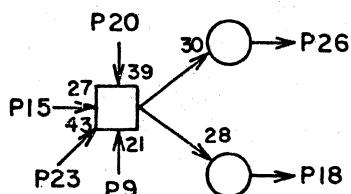
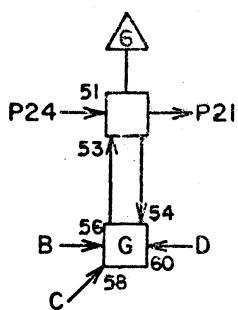
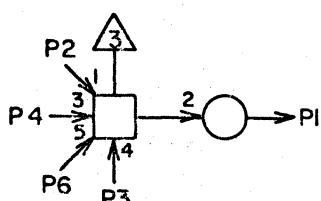
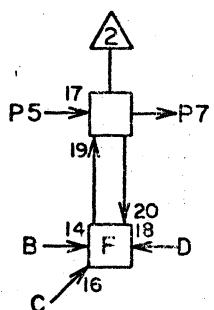
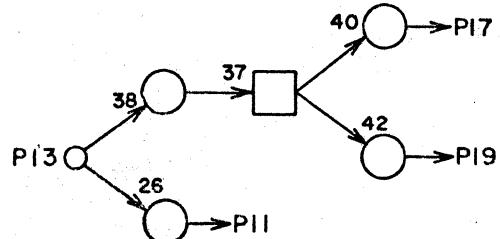
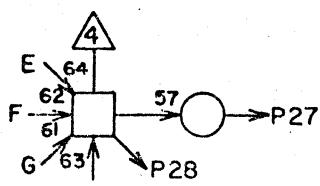
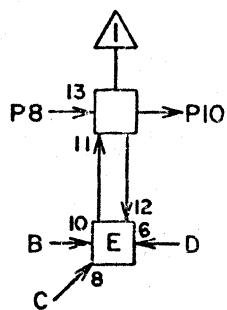
60042700 Rev. AB

LS 18057900

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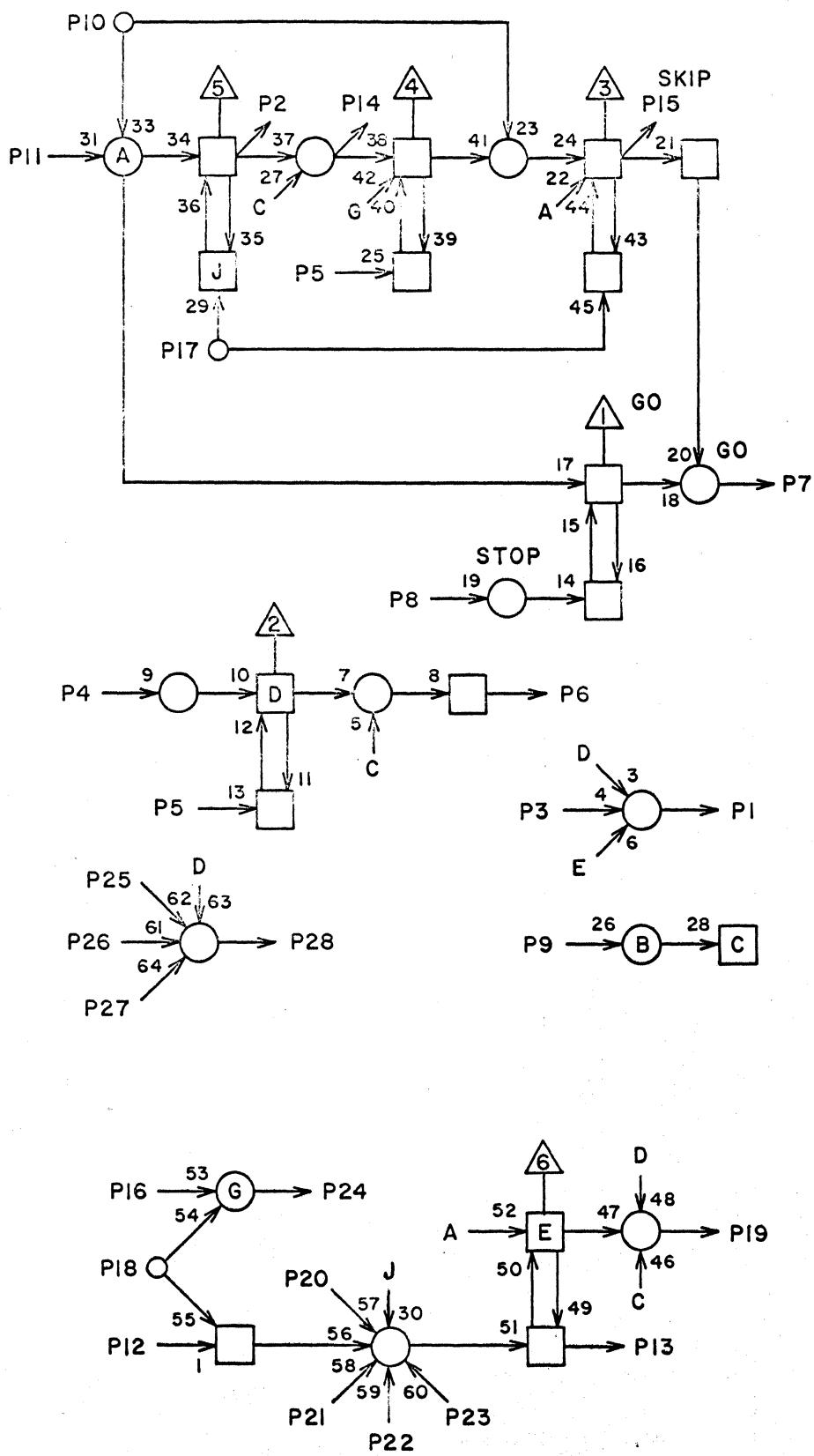


SEE CIRCUIT SPECIFICATION 11827600

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JACK PIN LG

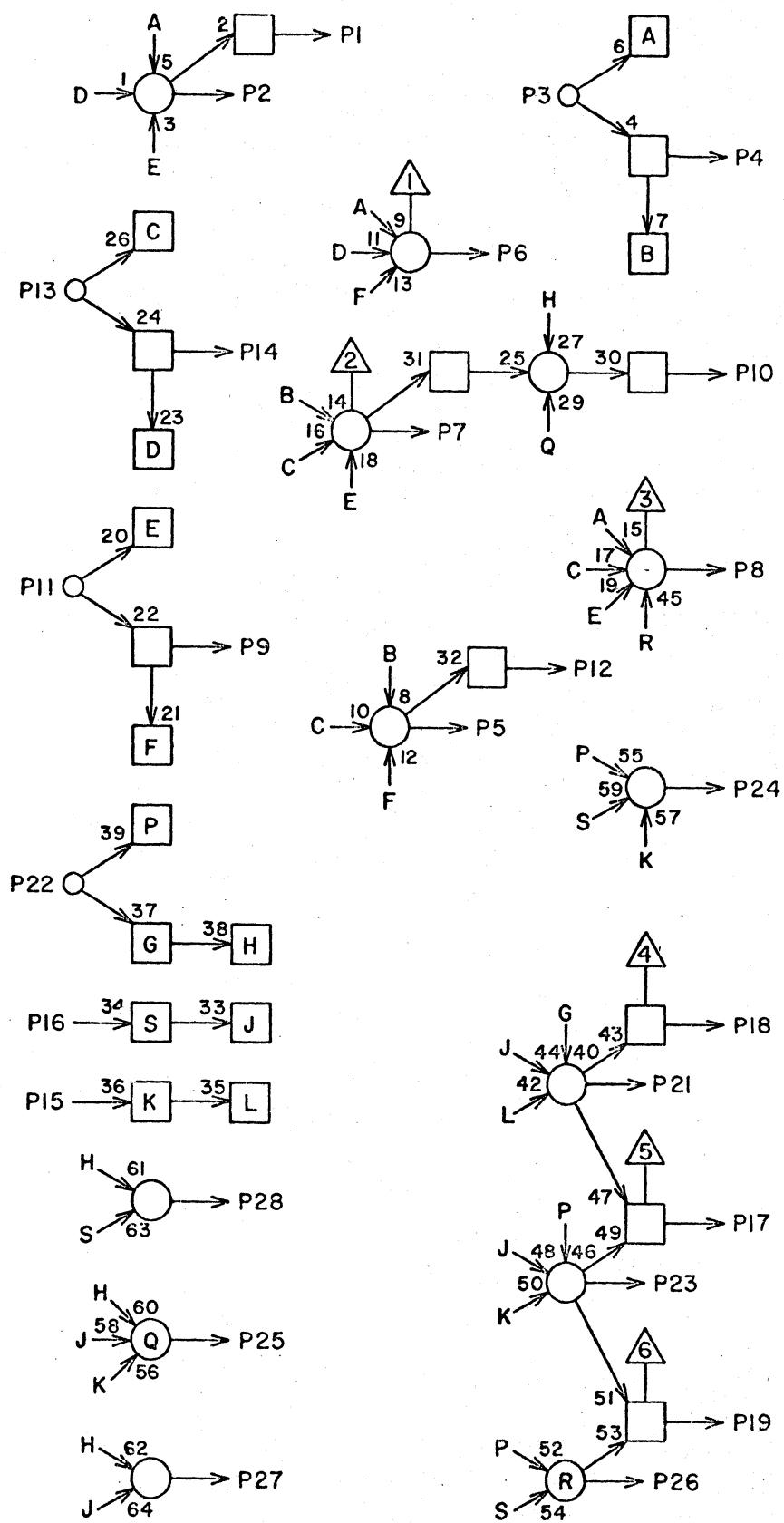
60042700 Rev. AB



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LS 18415300 B
ASSY REV

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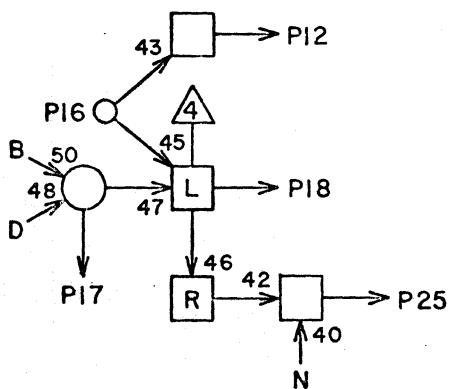
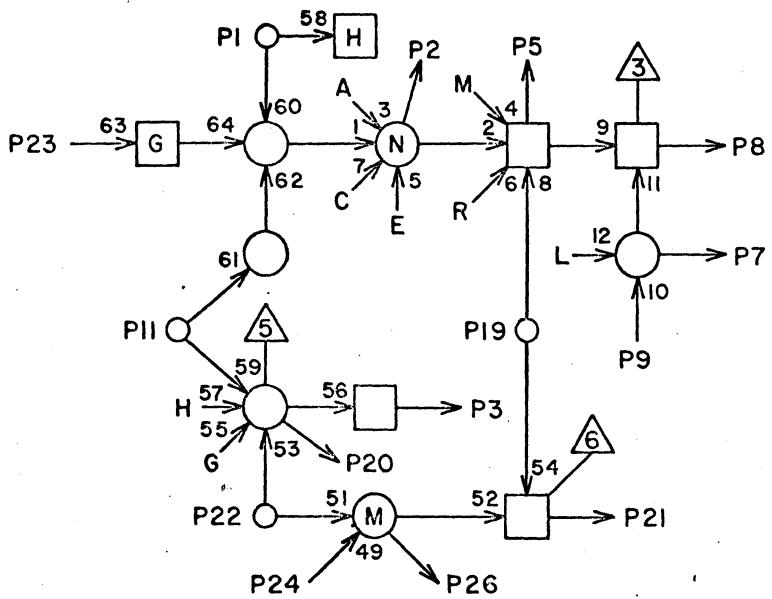
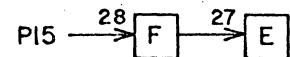
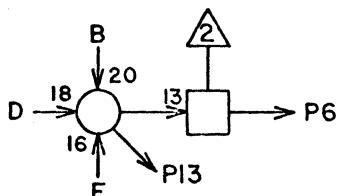
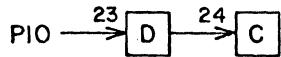
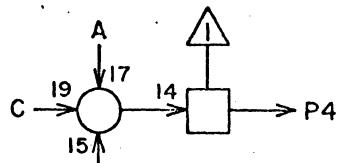
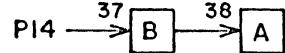
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SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev. T

LS 18415500 B
ASSY REV

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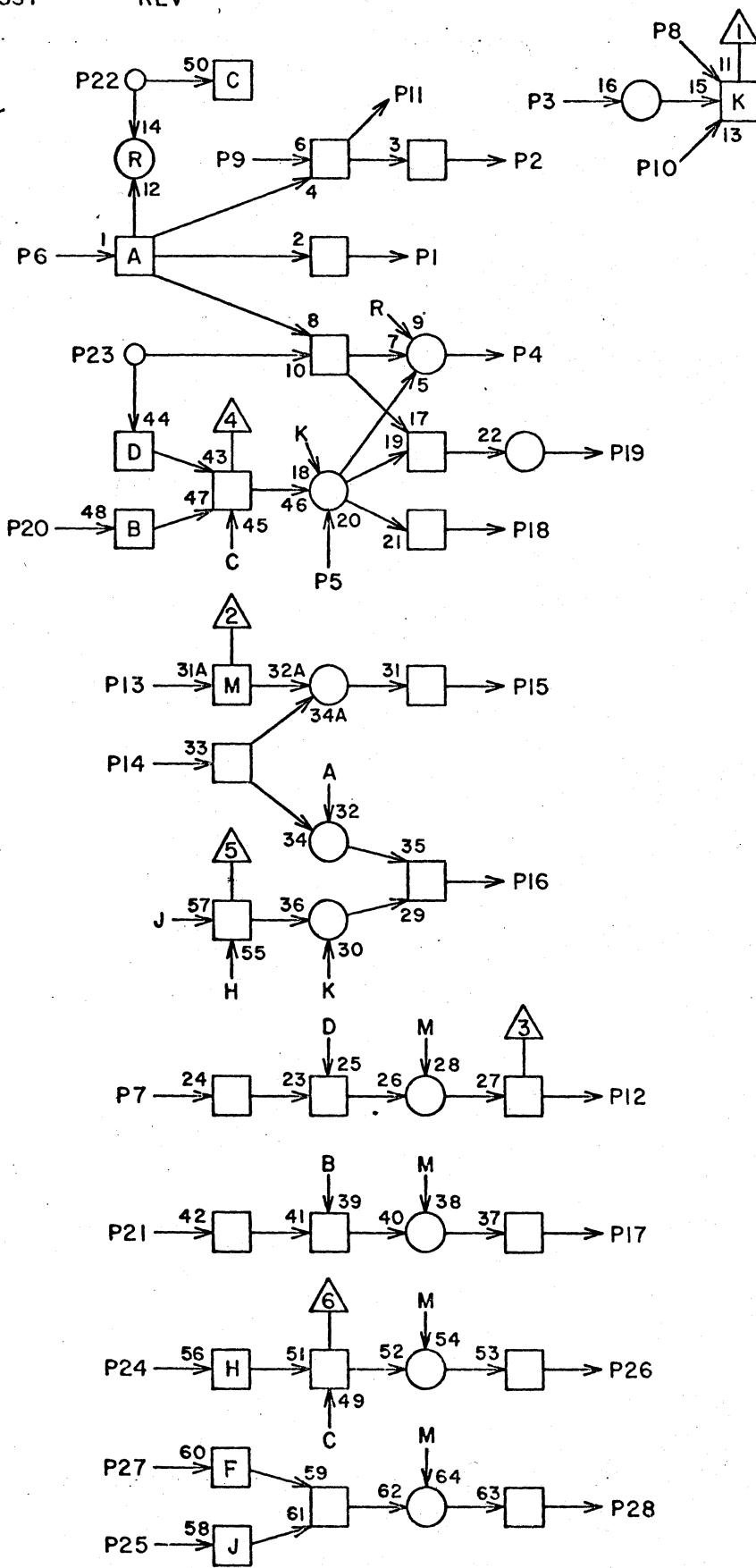
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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. T

LS 18415400
ASSY

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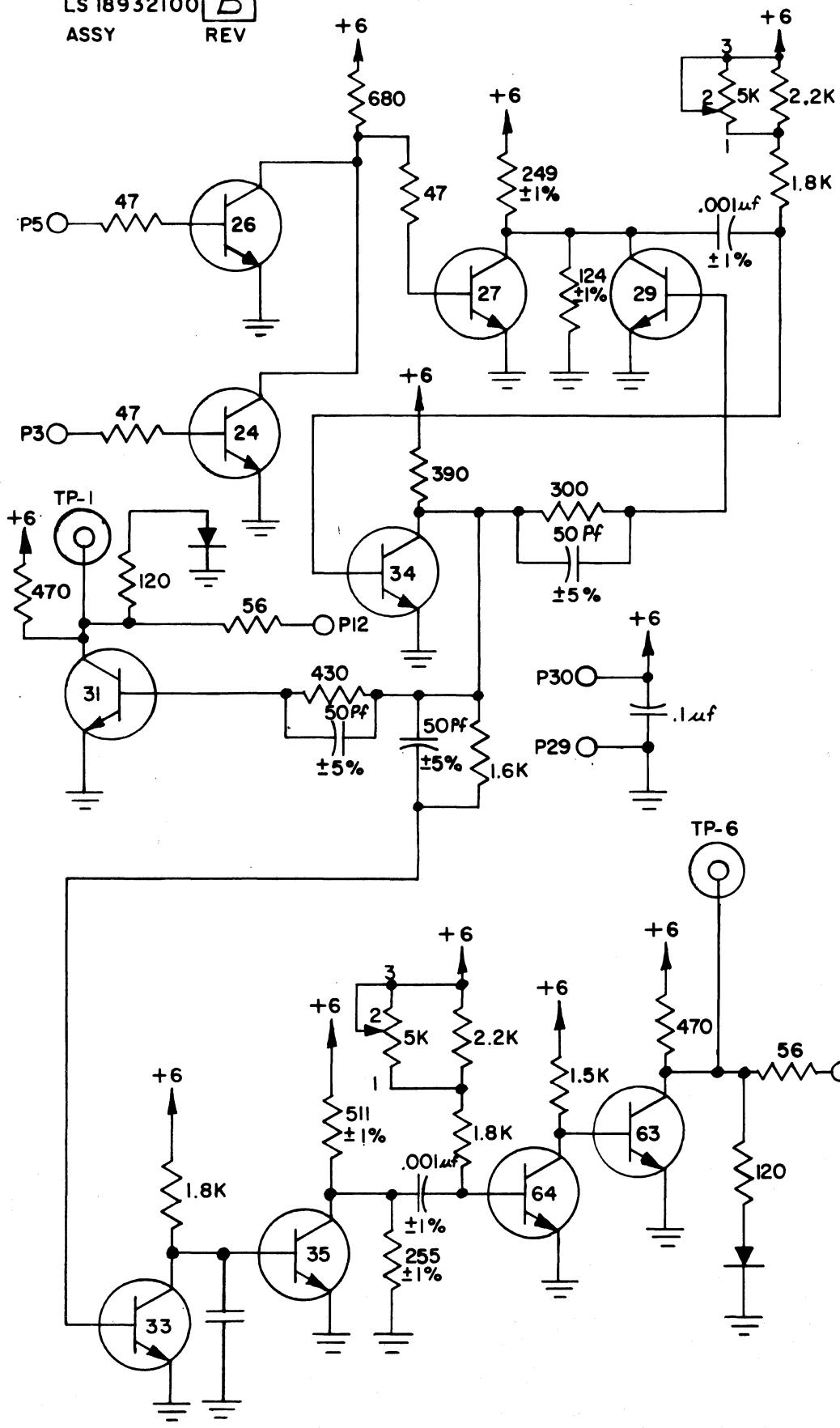


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JACK PIN LG
SEE CIRCUIT SPECIFICATION
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60042700 Rev. T

LS 18932100 B
ASSY REV



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JACK PIN LG
SEE CIRCUIT SPECIFICATION
52301600

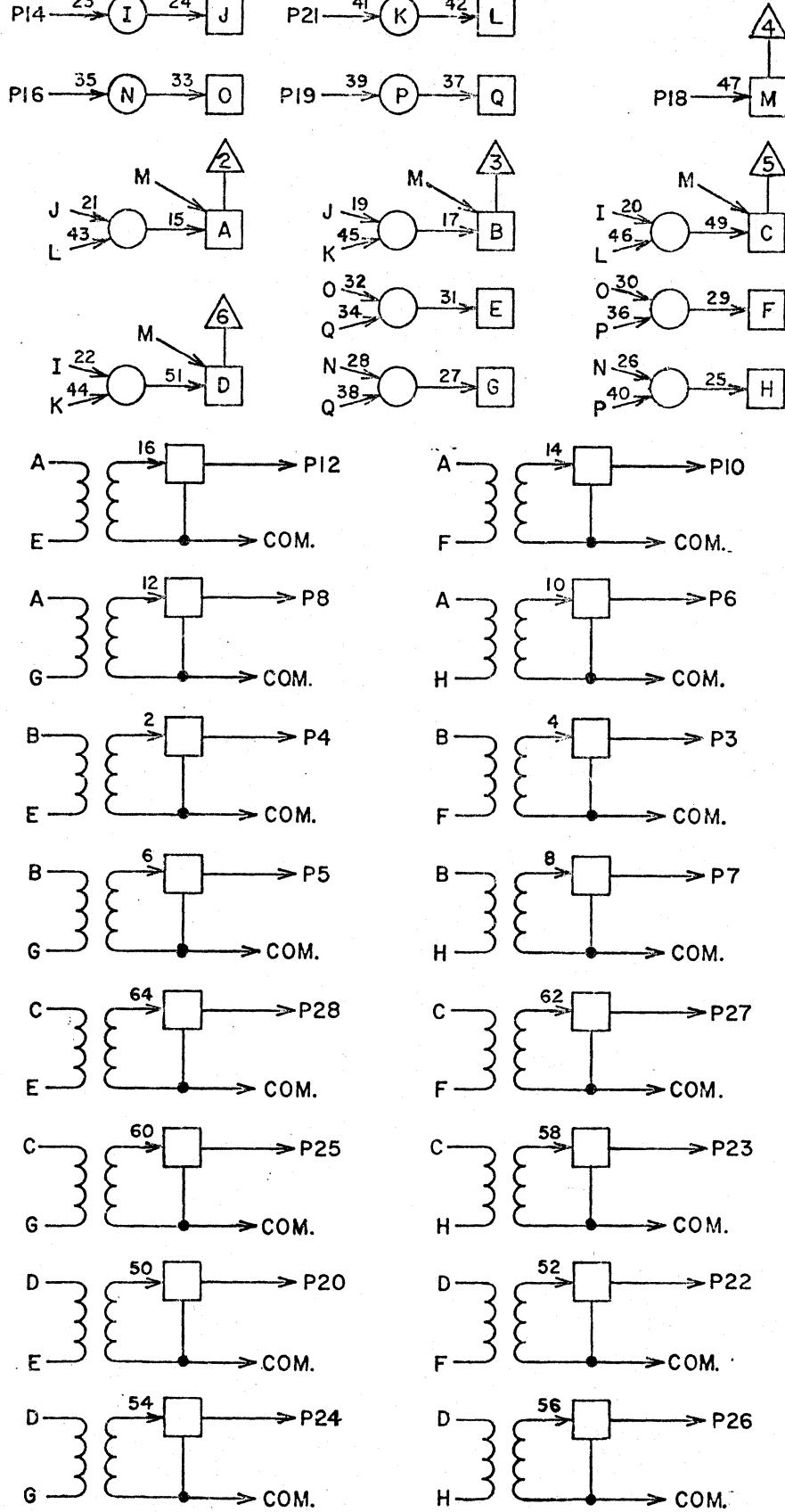
60042700 Rev. Z

LS 17985600
ASSY

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SPECIAL MODULE
SEE PRINTED CIRCUIT MANUAL
PUB. NO. 60042700

BA



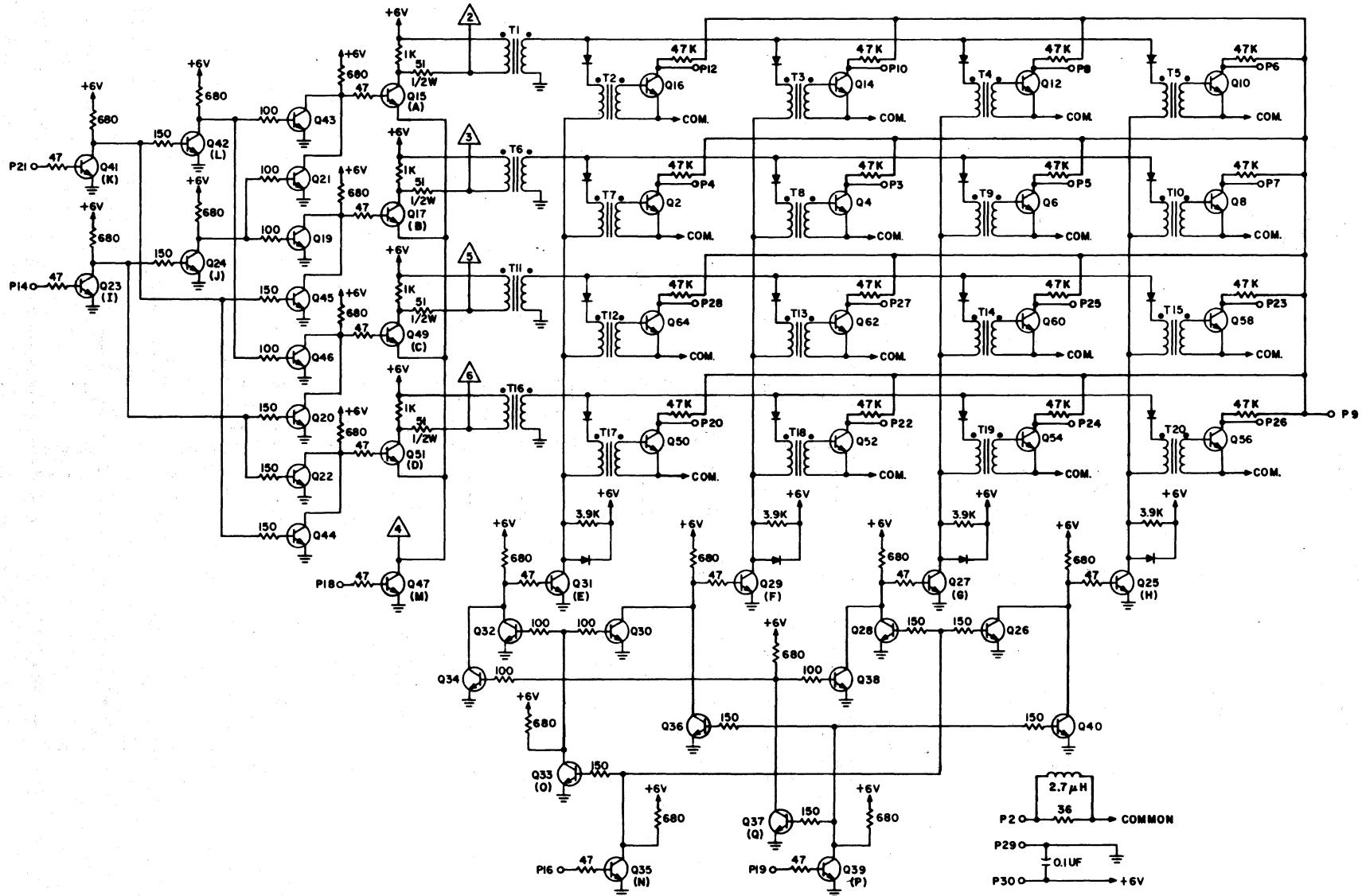
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JACK PIN LG
CIRCUIT SPECIFICATION
II842200

TIE DOWN → 9

COMMON → P2

60042700 Rev. U

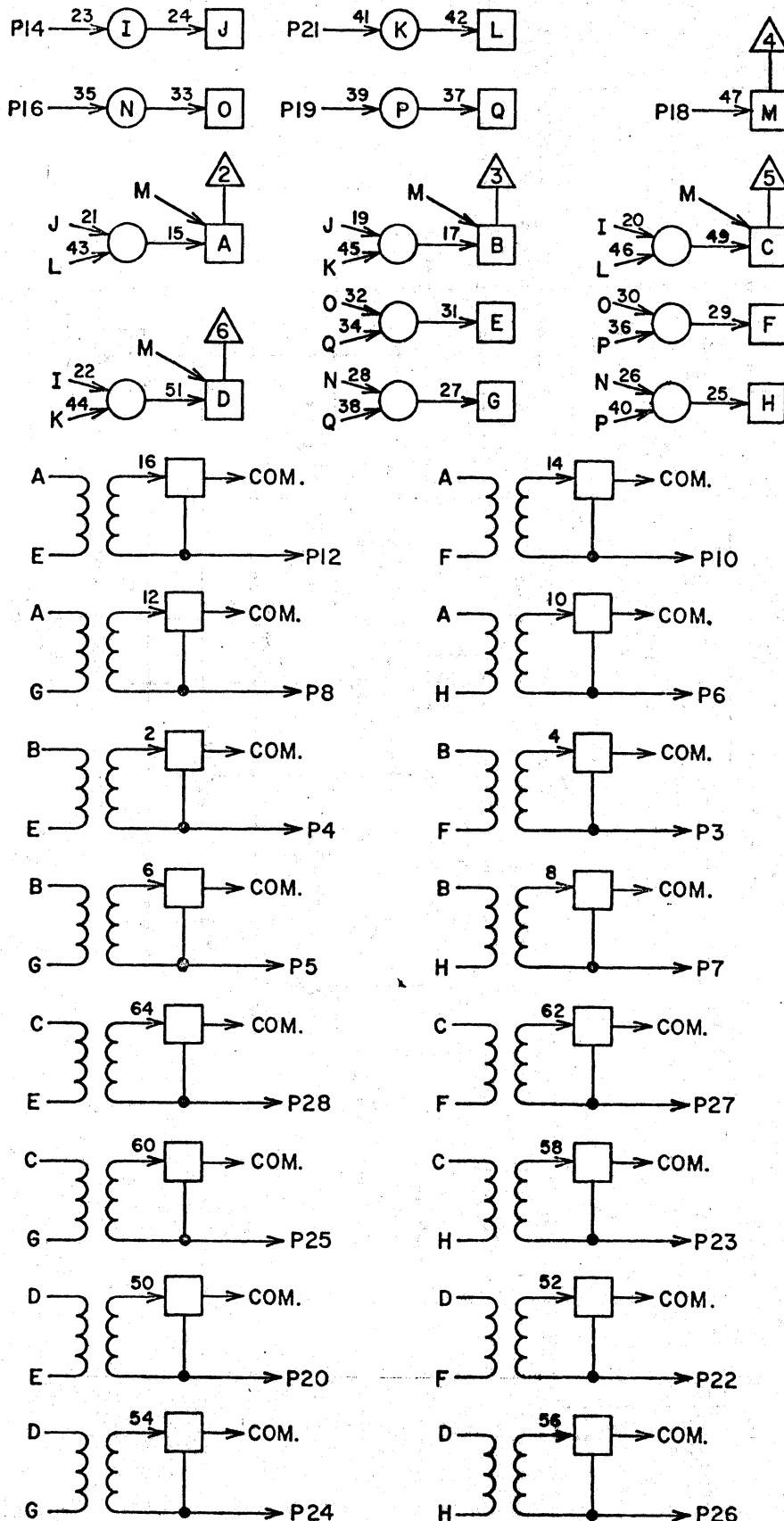


BA MODULE
ASSY LS 17985600

LS 17985700
ASSY

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REV

SPECIAL MODULE
SEE PRINTED CIRCUIT MANUAL
PUB. NO. 60042700

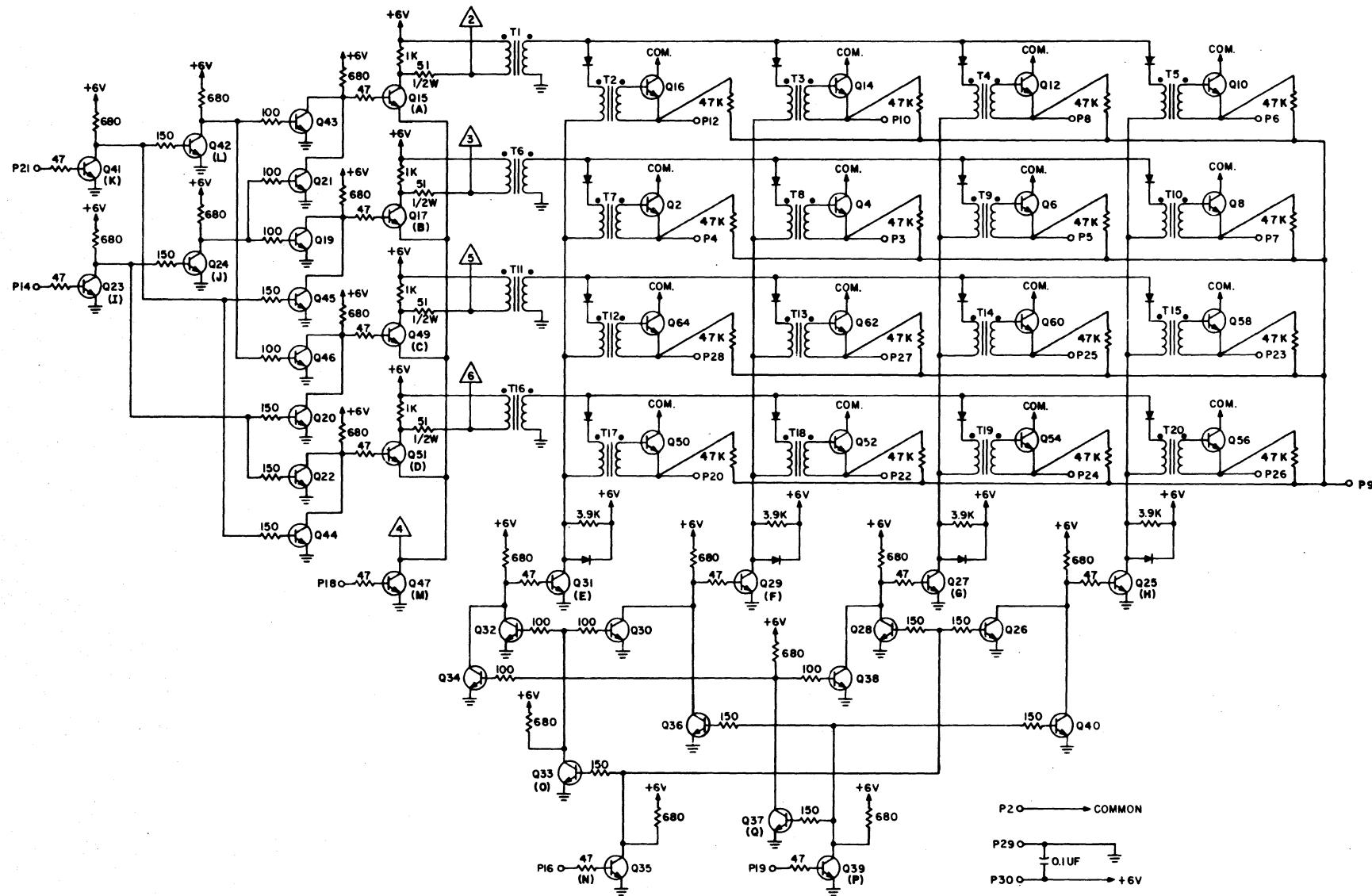


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JACK PIN LG
CIRCUIT SPECIFICATION
II842300
60042700 Rev. U

TIE DOWN → 9

COMMON → P2

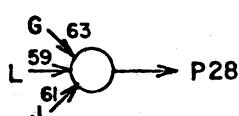
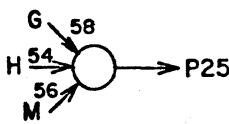
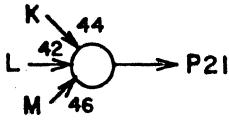
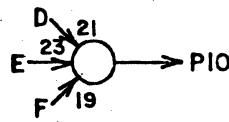
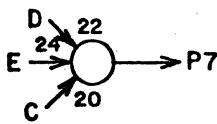
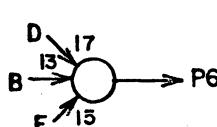
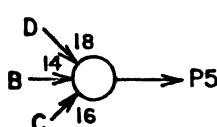
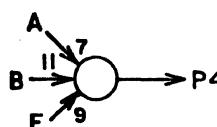
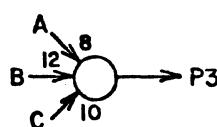
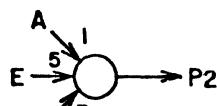
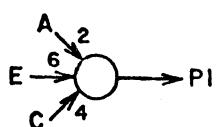
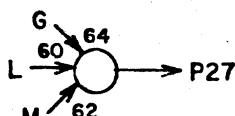
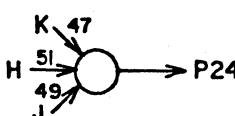
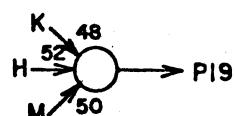
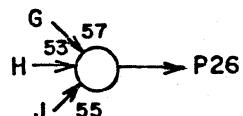
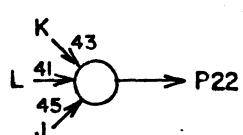
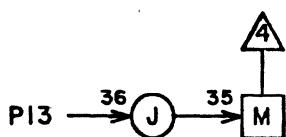
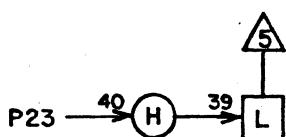
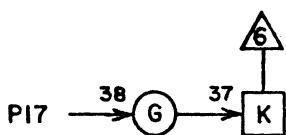
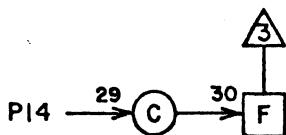
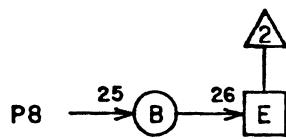
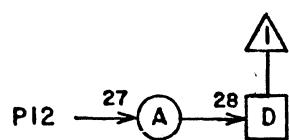


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JACK PIN LG

CIRCUIT SPECIFICATION

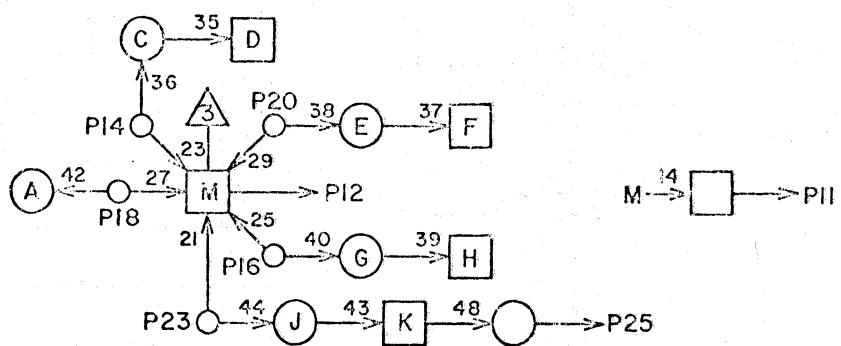
60042700 Rev. U

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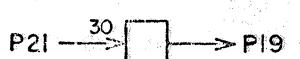
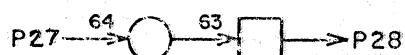
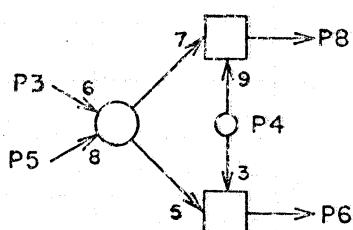
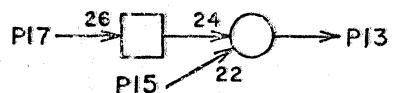
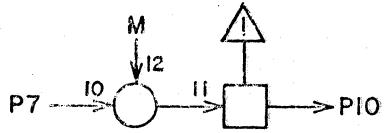
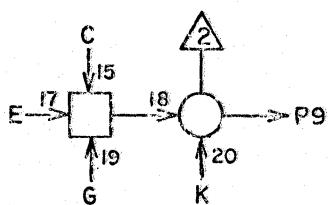
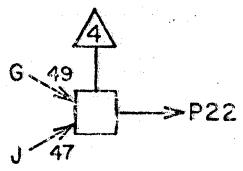
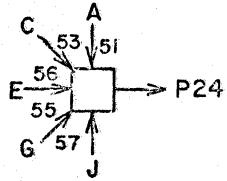
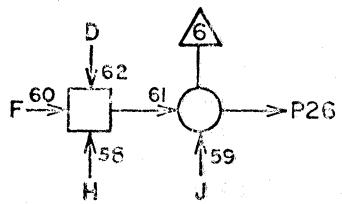
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JACK PIN LG
CIRCUIT SPECIFICATION

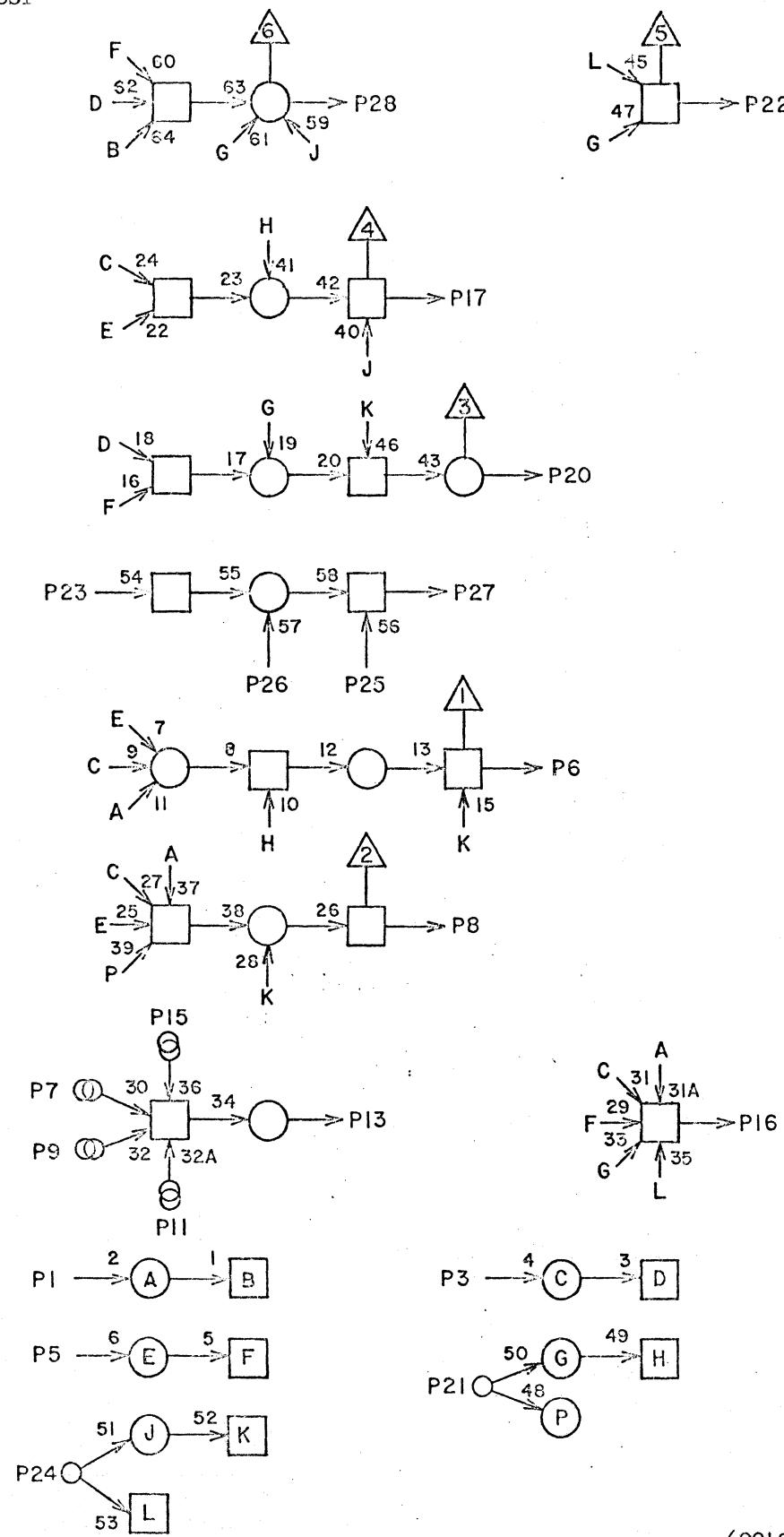
60042700 Rev. U

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JACK PIN LG
CIRCUIT SPECIFICATION

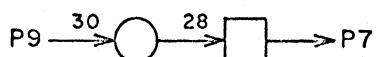
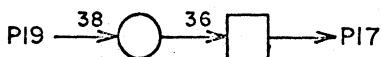
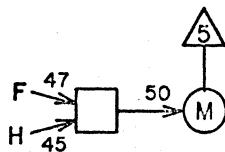
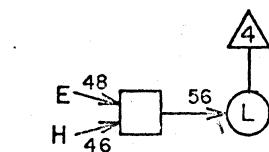
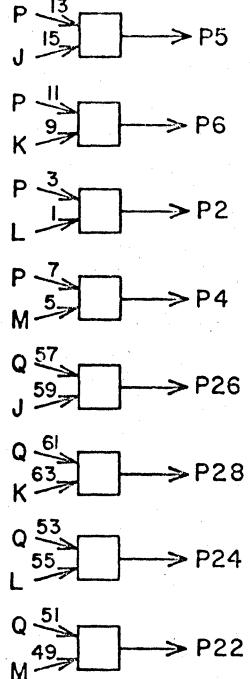
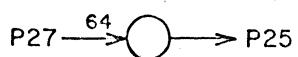
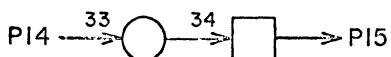
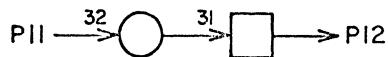
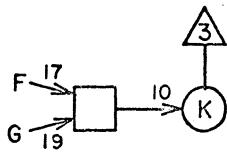
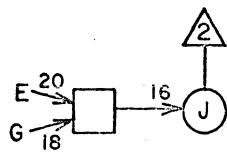
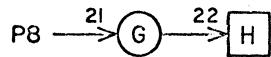
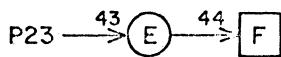
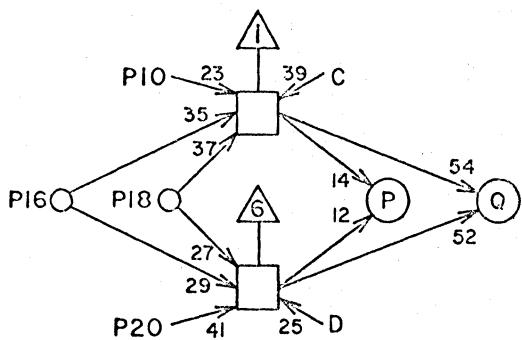
60042700 Rev. U 11827600

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JACK PIN LG

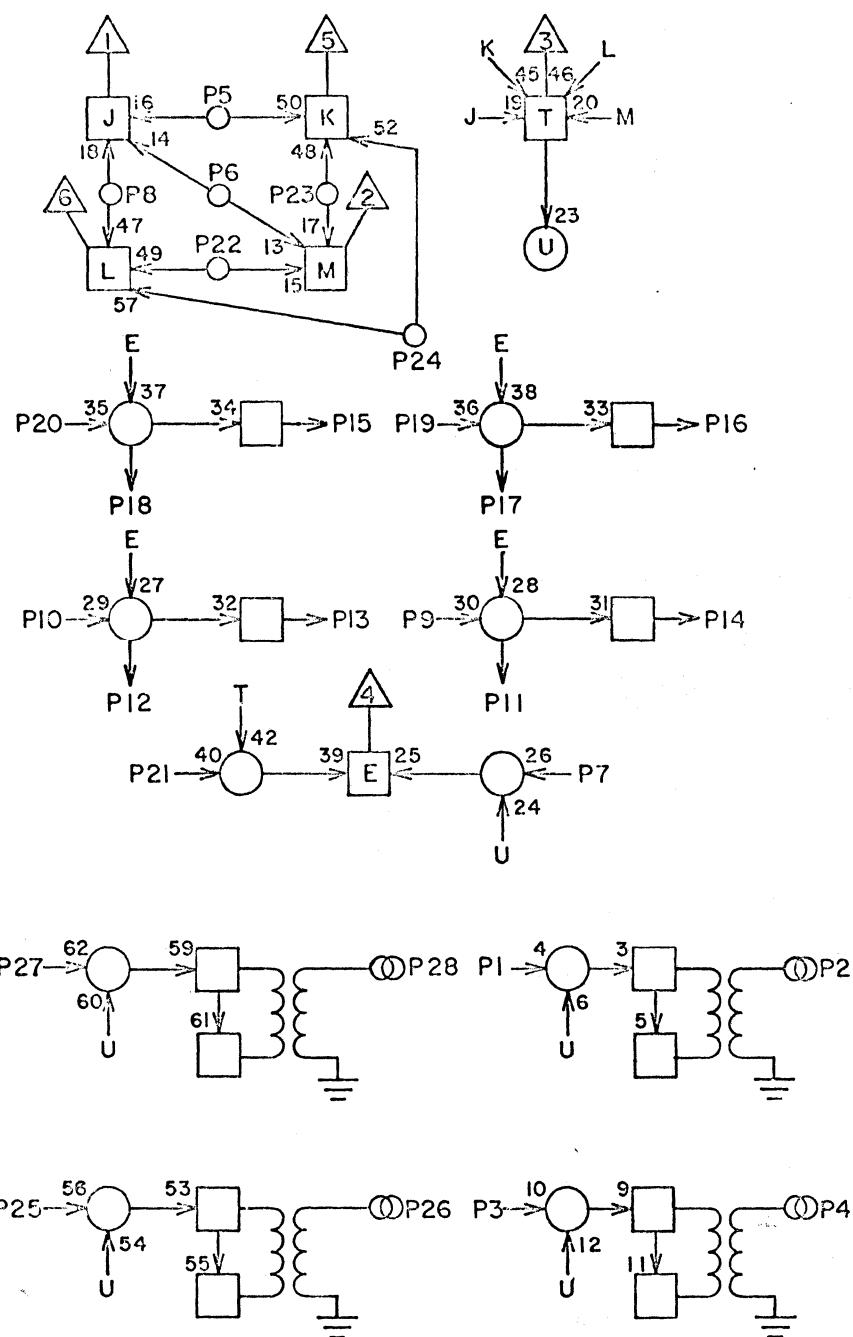
CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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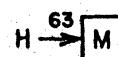
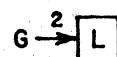
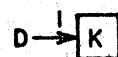
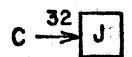
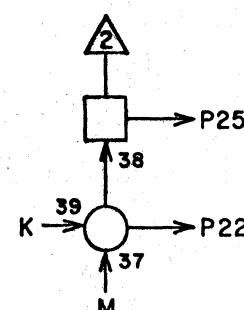
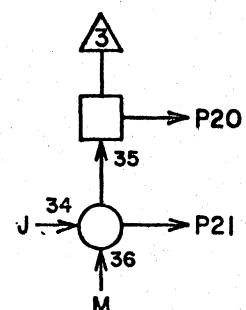
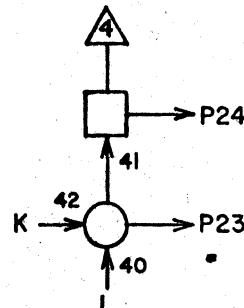
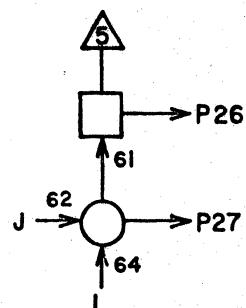
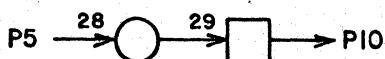
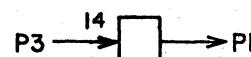
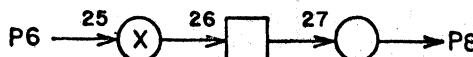
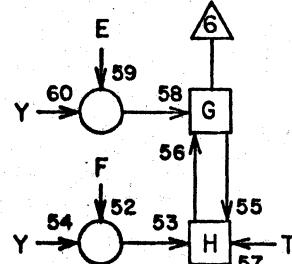
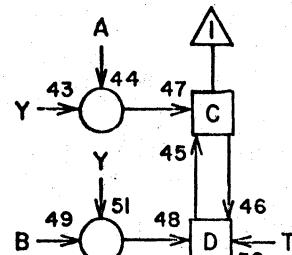
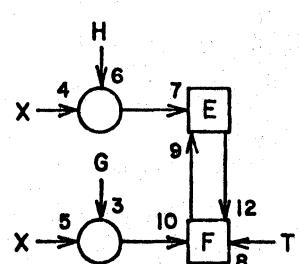
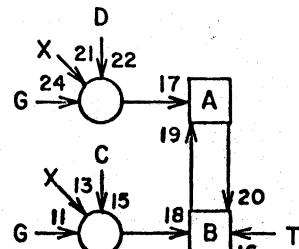
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JACK PIN LG
CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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P11 —————→ +6

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P15 —————→ +6

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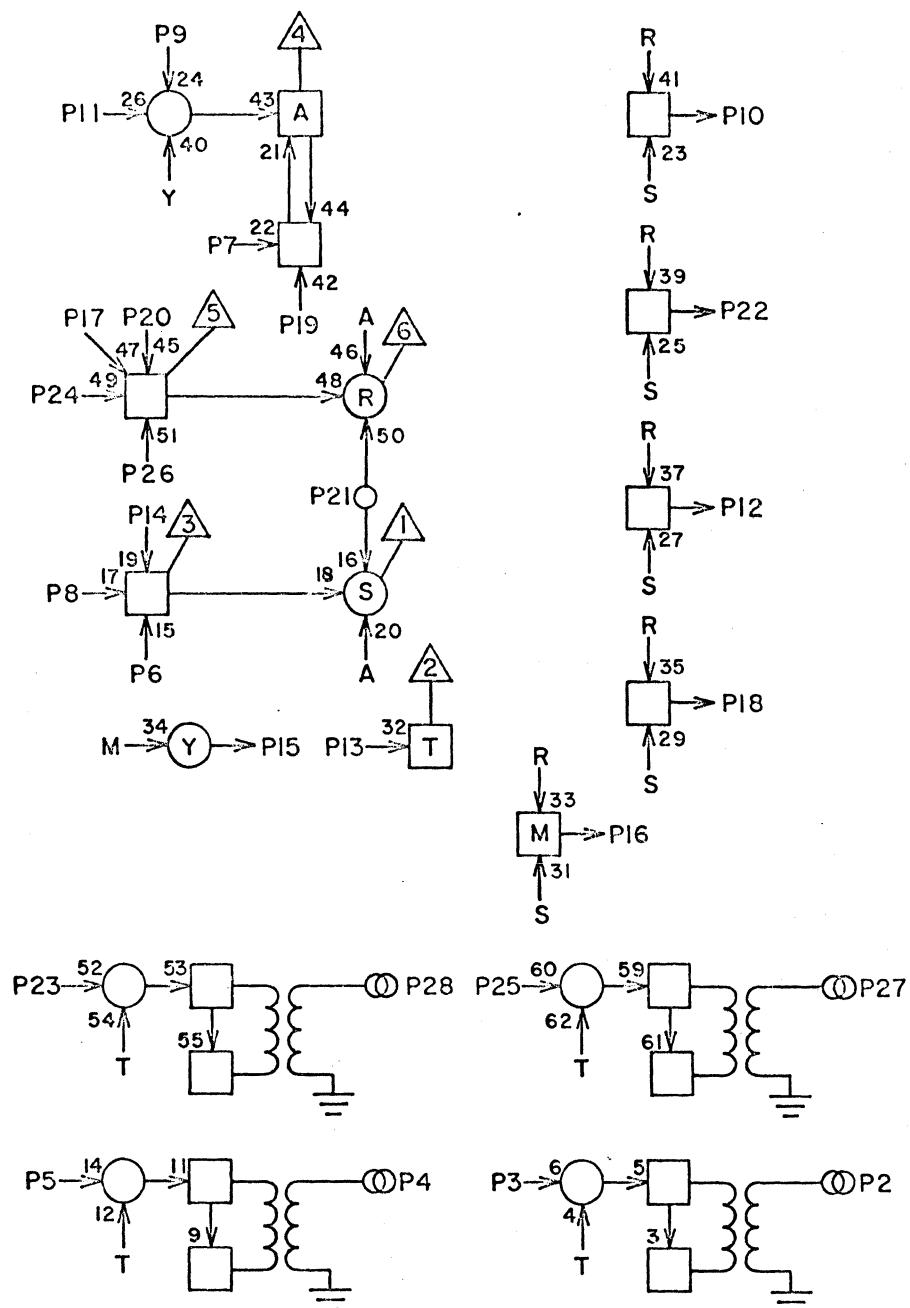
JACK PIN LG
CIRCUIT SPECIFICATION
11827600

60042700 Rev. U

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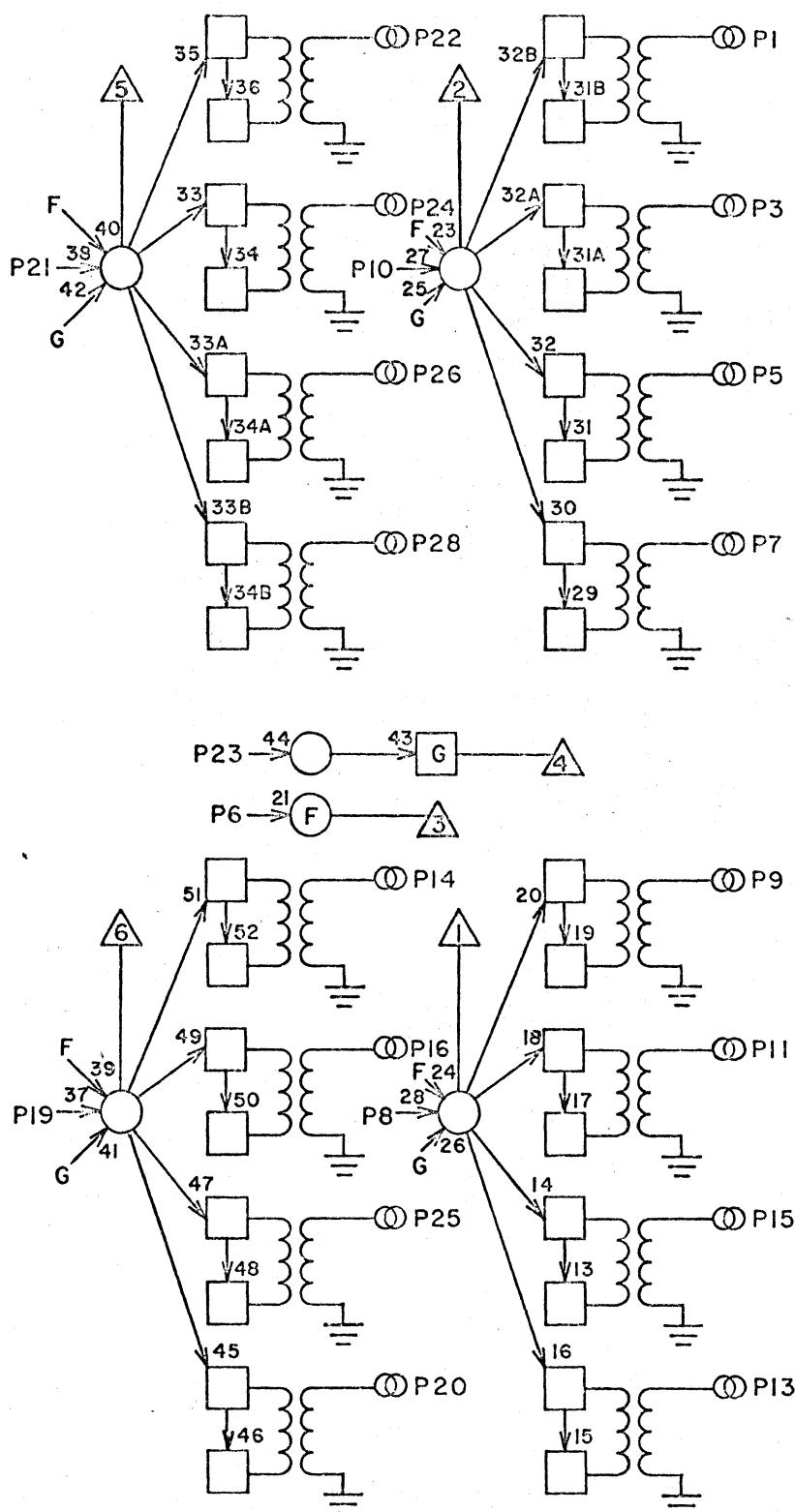
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CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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JACK PIN LG

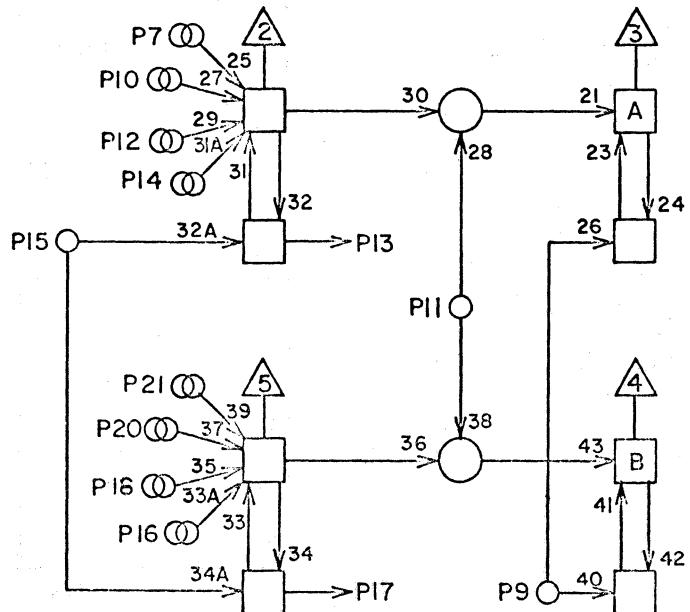
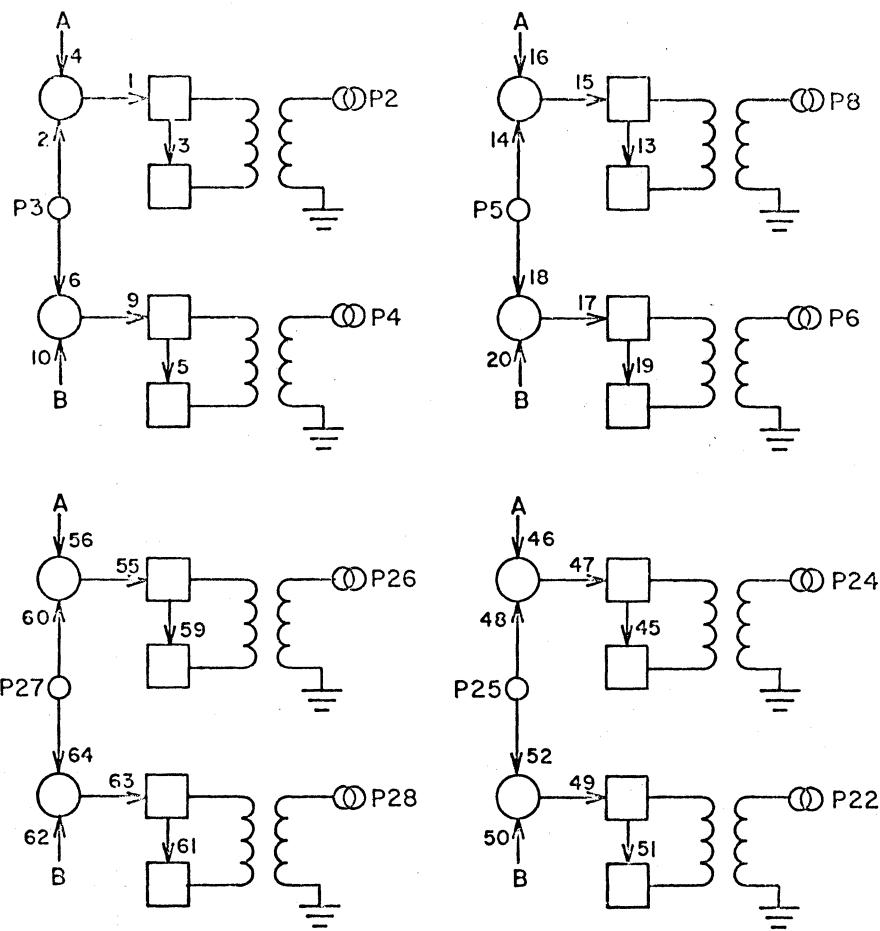
CIRCUIT SPECIFICATION

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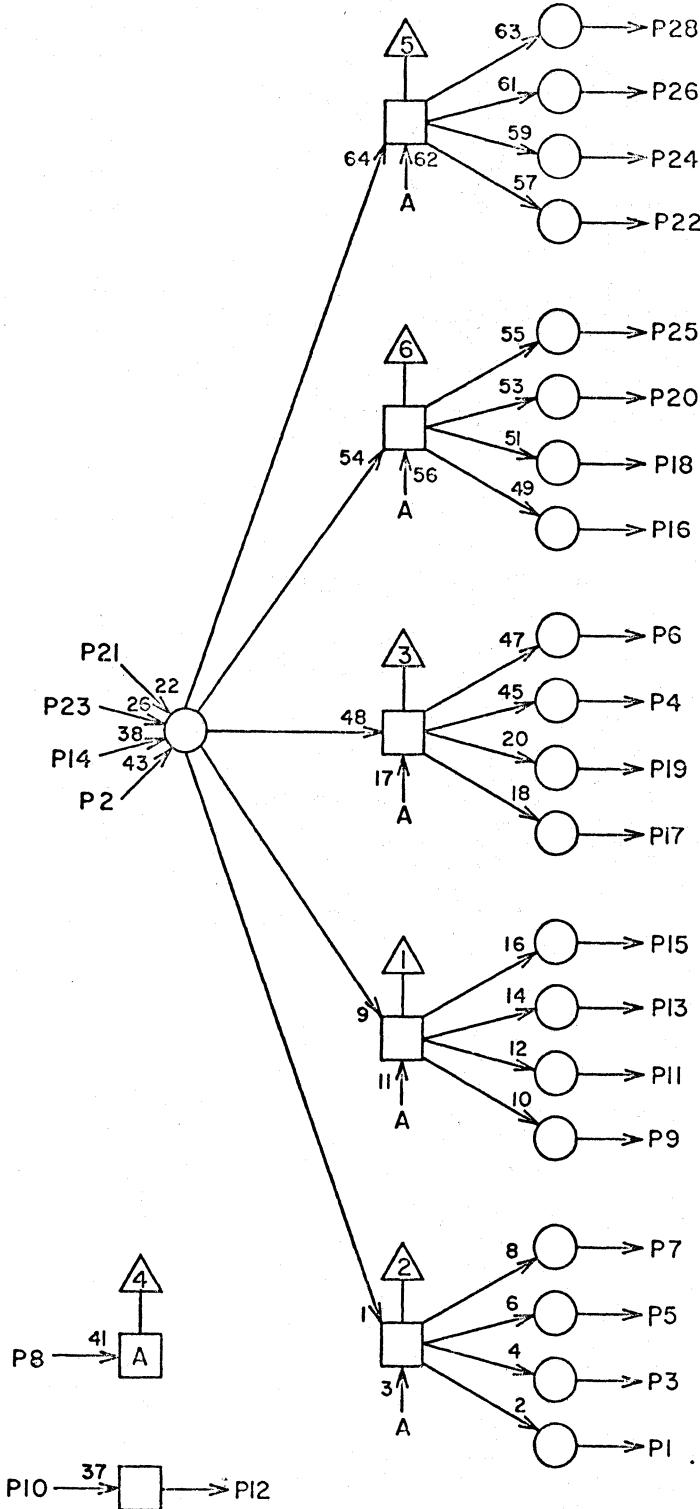
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CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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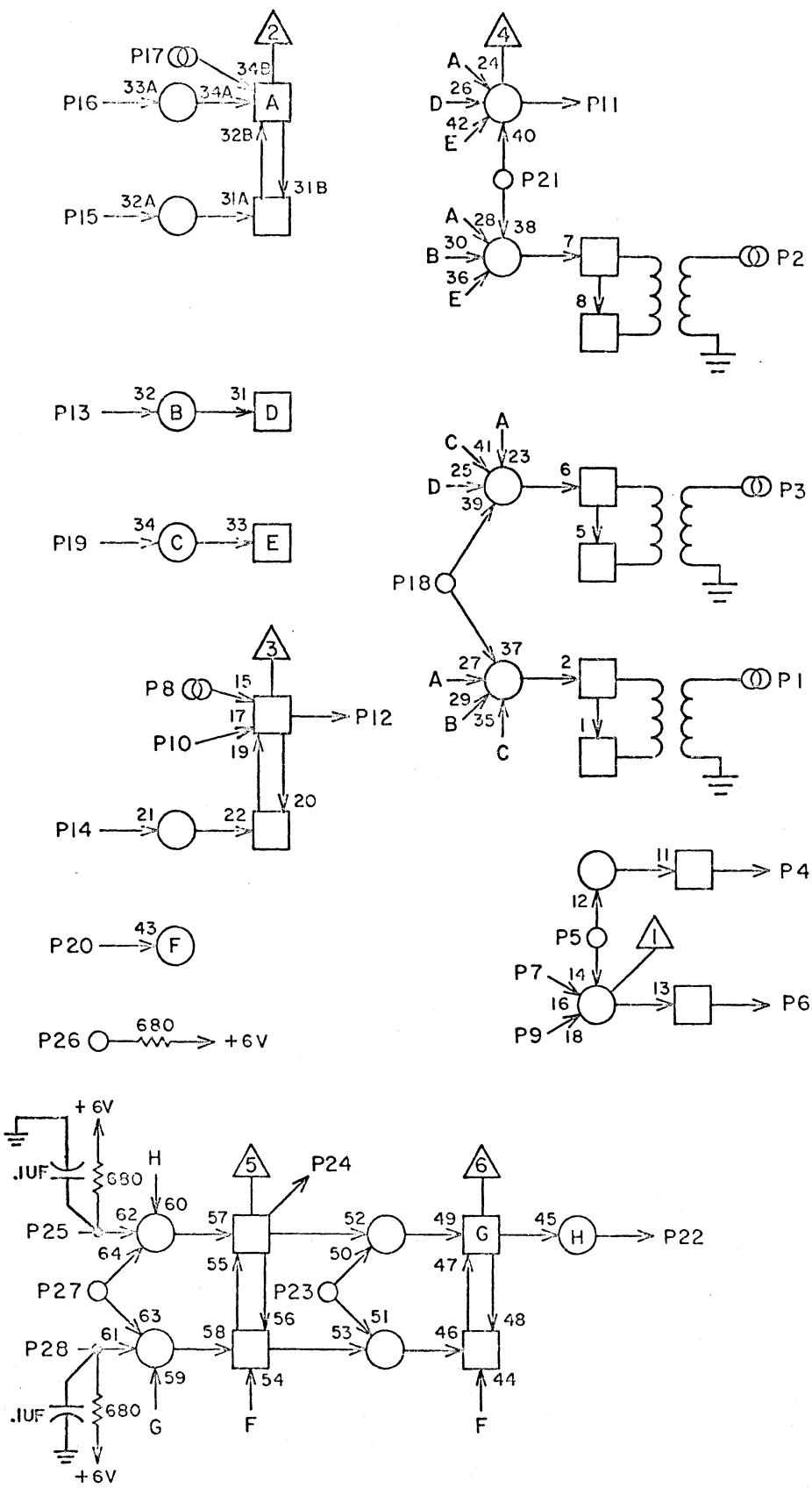
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CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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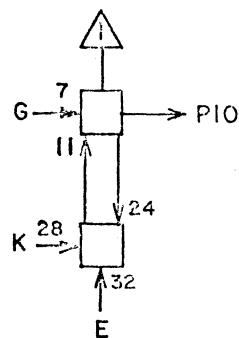
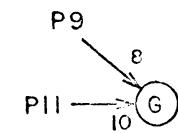
CIRCUIT SPECIFICATION

60042700 Rev. U 11827600

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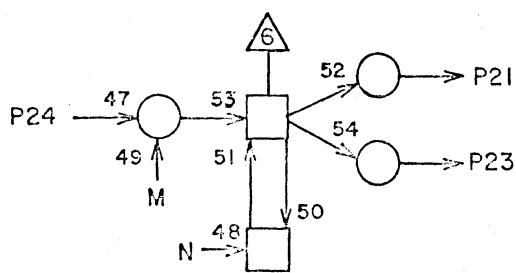
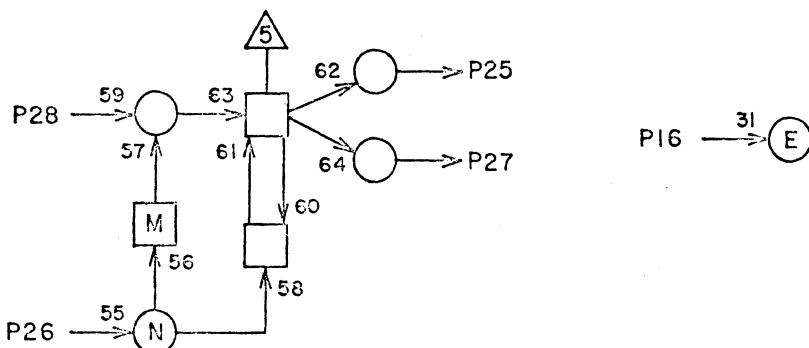
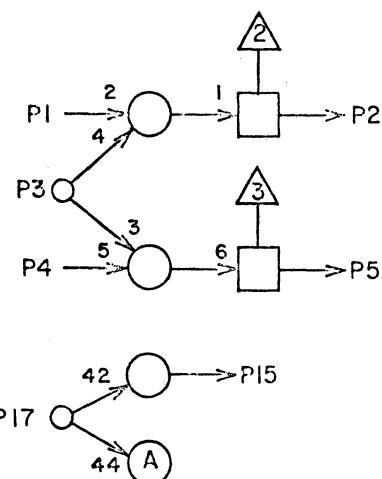
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JACK PIN LG



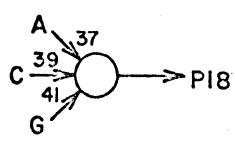
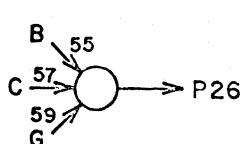
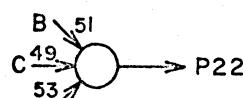
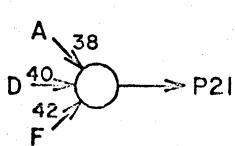
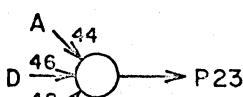
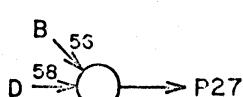
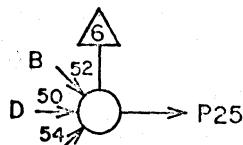
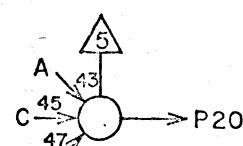
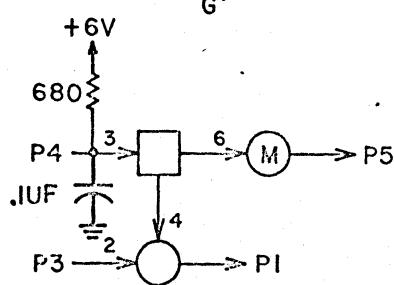
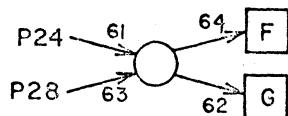
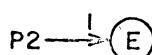
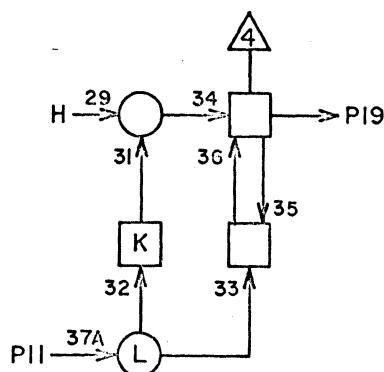
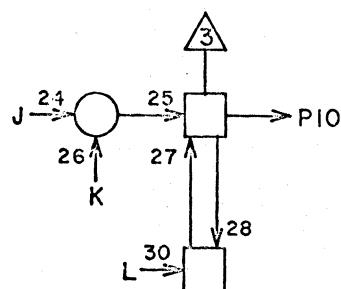
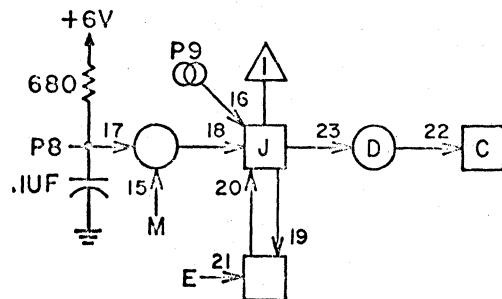
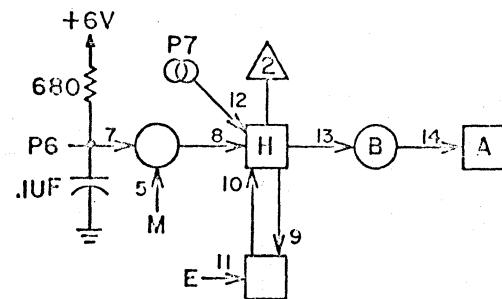
CIRCUIT SPECIFICATION
11827600

60042700 Rev. U

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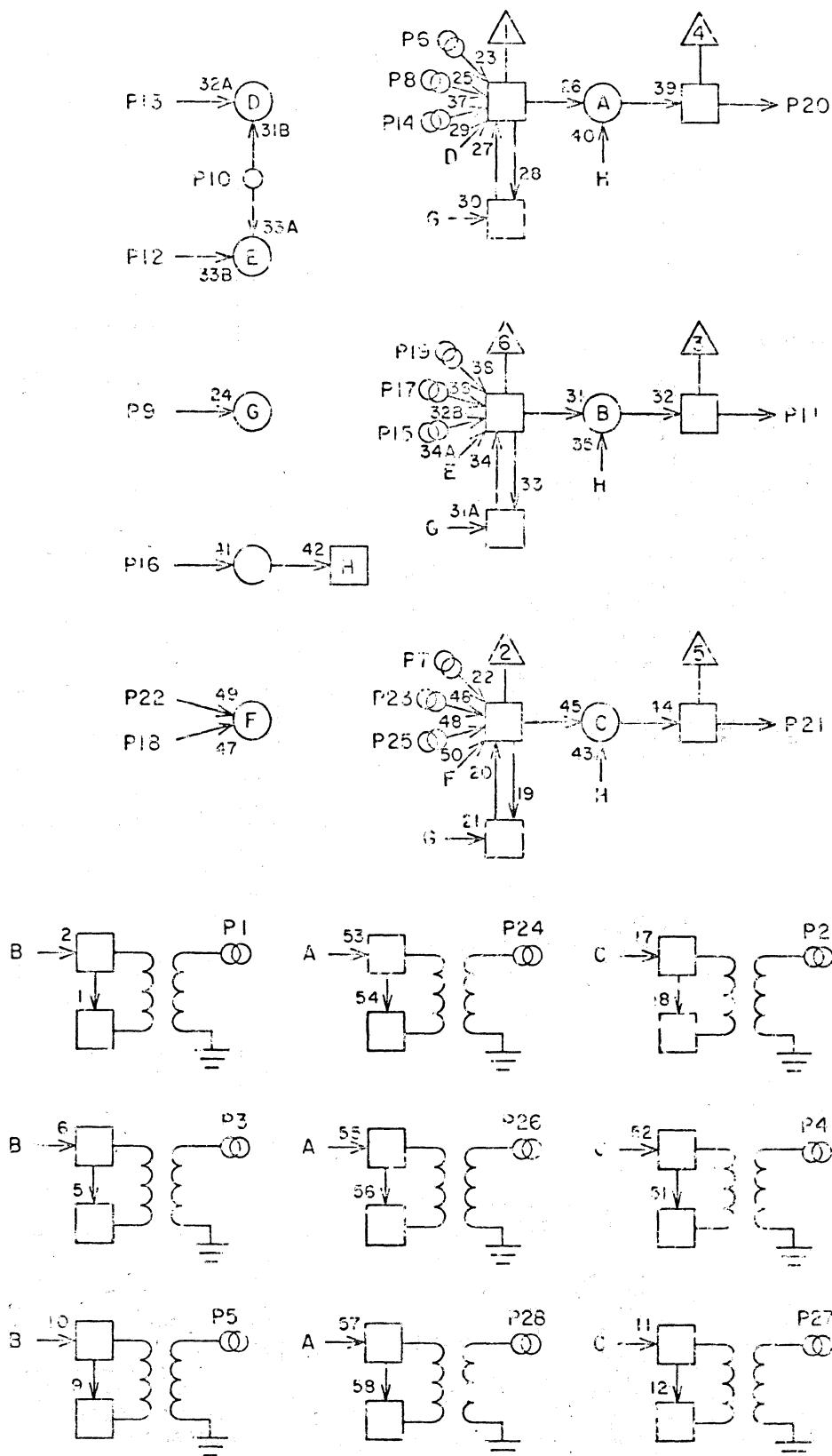
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CIRCUIT SPECIFICATION
11827600
60042700 Rev. U

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BACK PIN LG

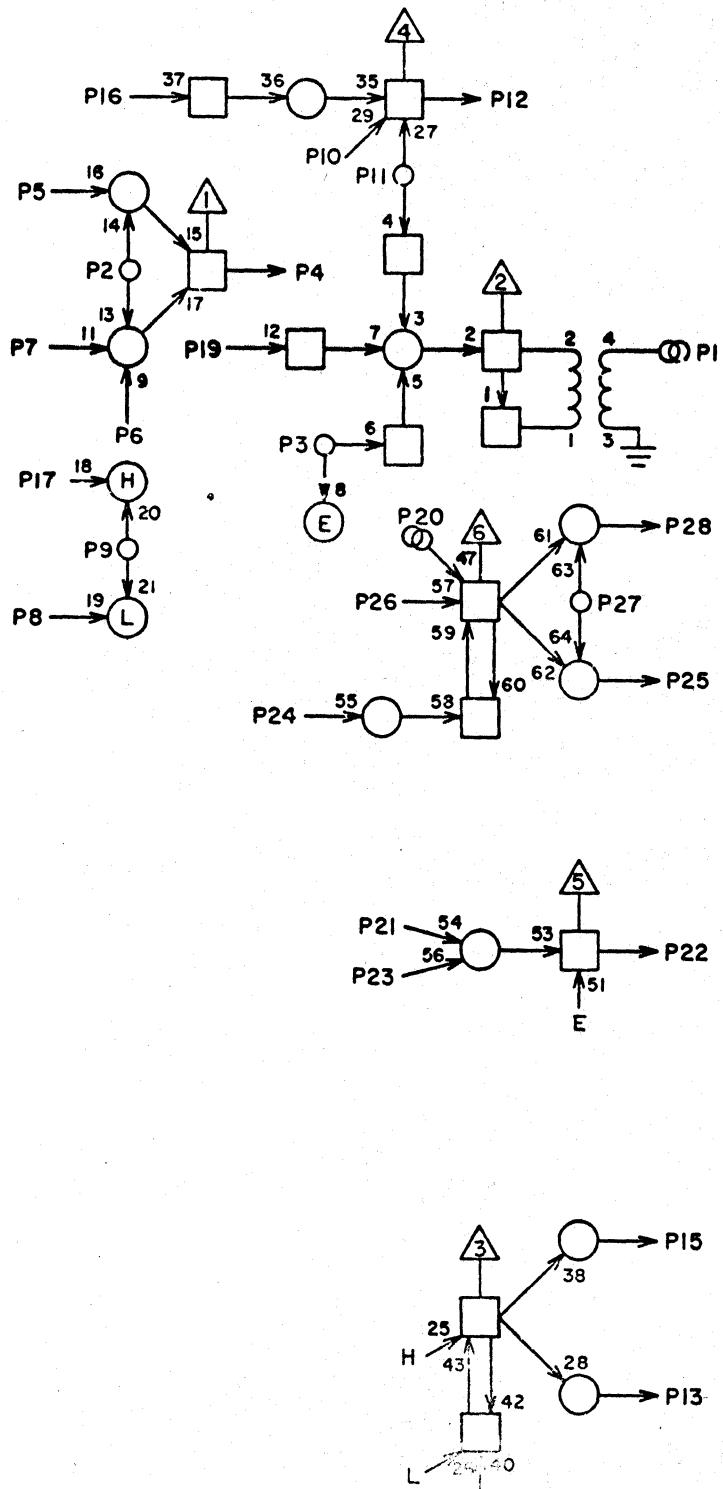
CIRCUIT SPECIFICATION
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60042700 Rev. U



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JACK PIN LG
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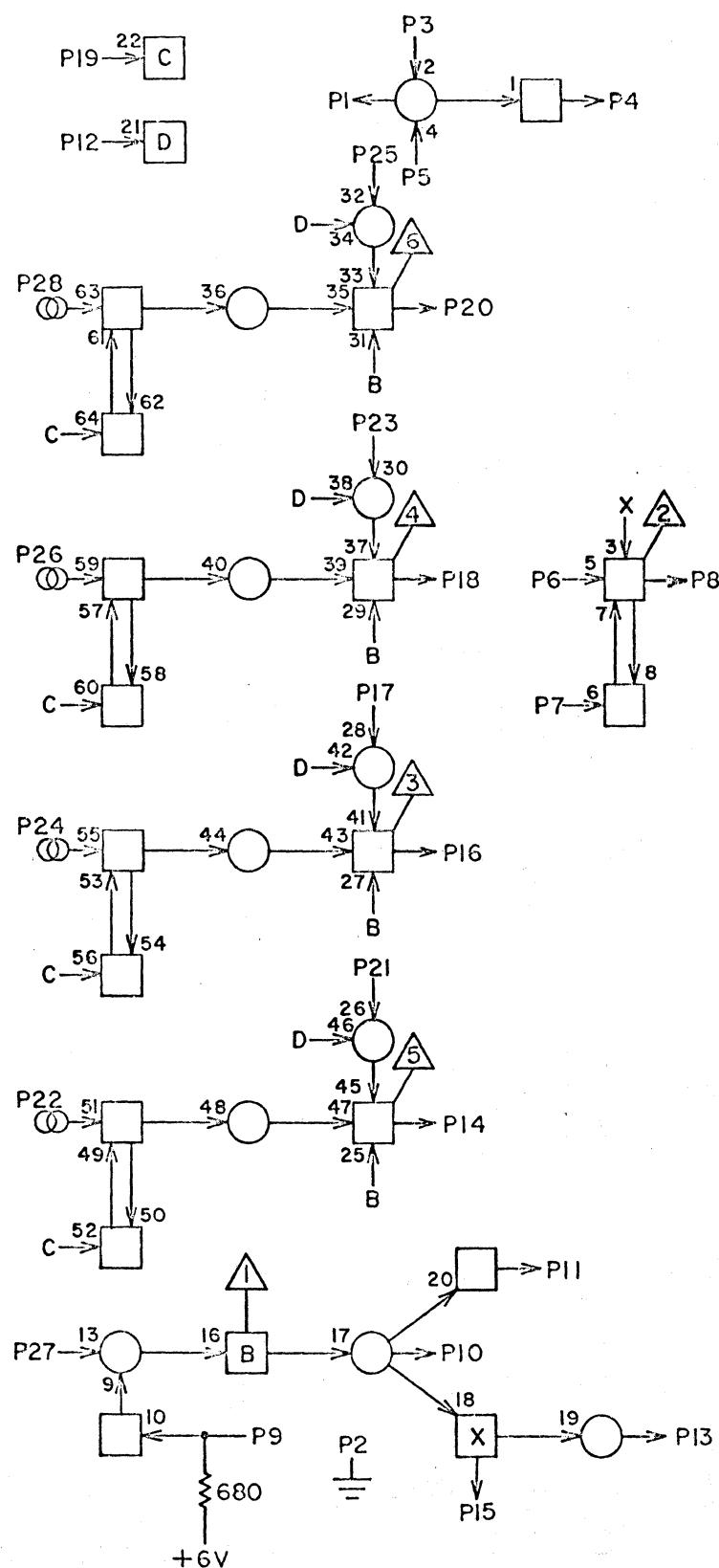
60042700 Rev. AN

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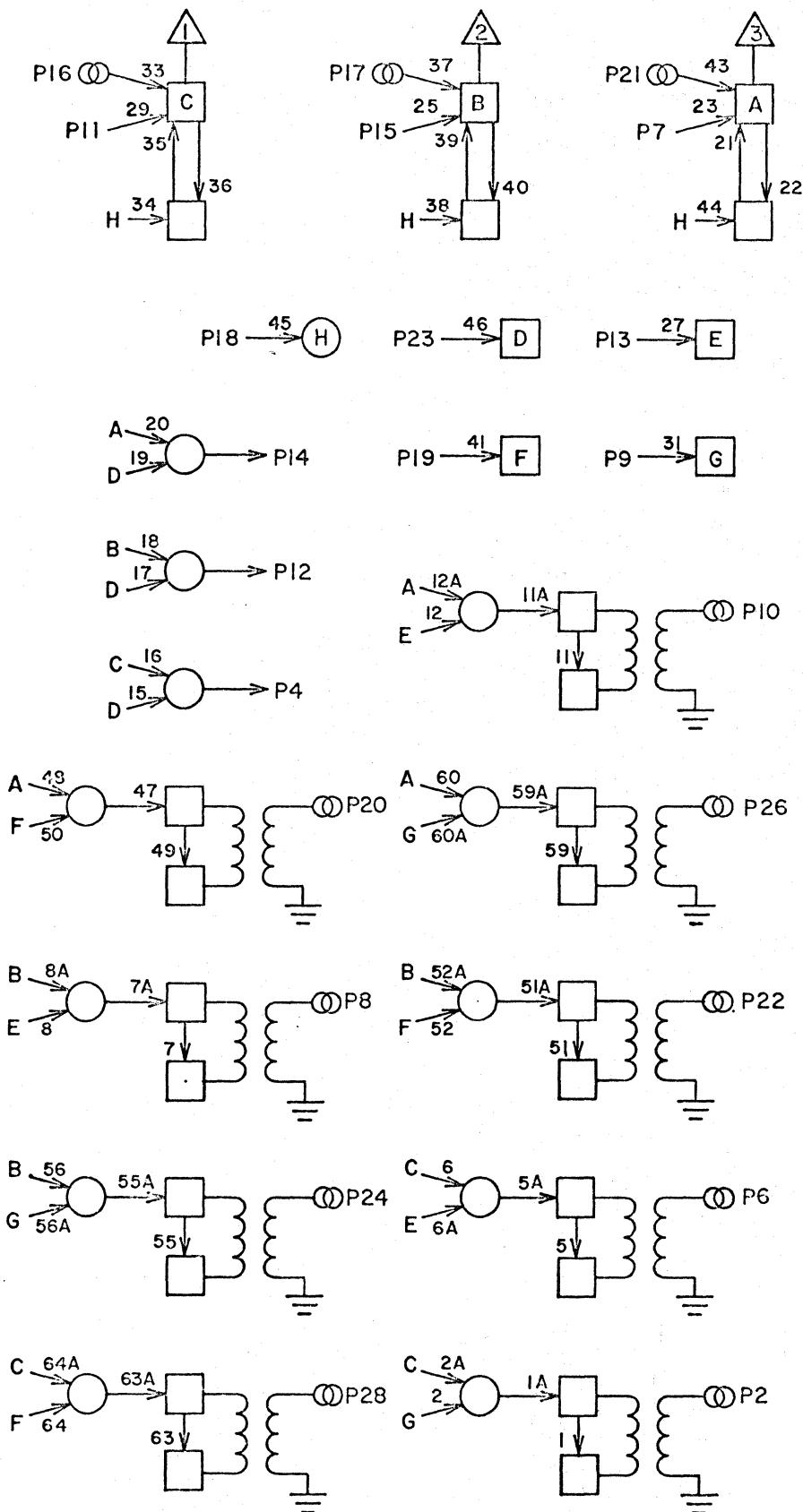
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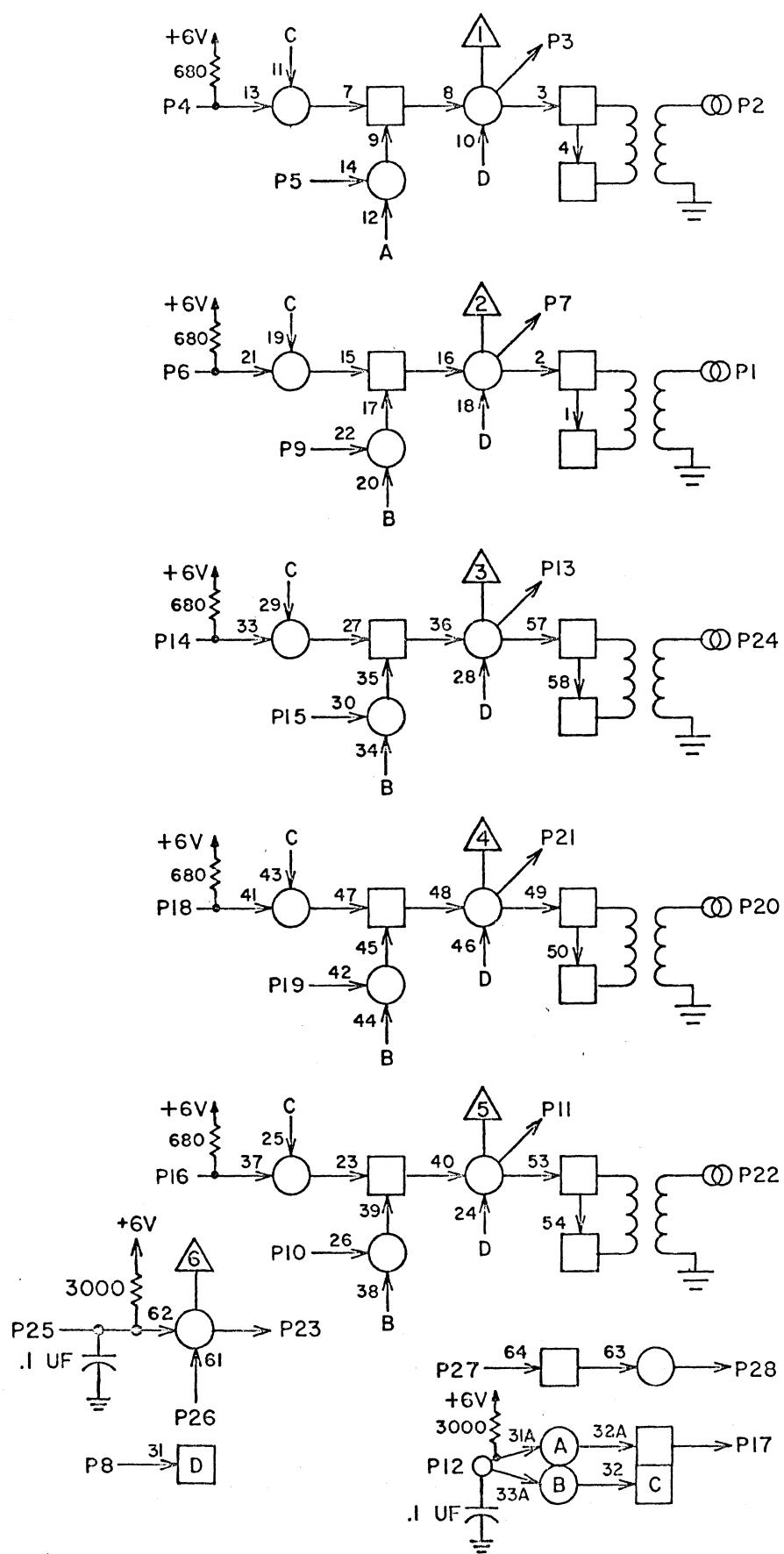
60042700 Rev. U



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JACK PIN LG
CIRCUIT SPECIFICATION
11827600

60042700 Rev. U



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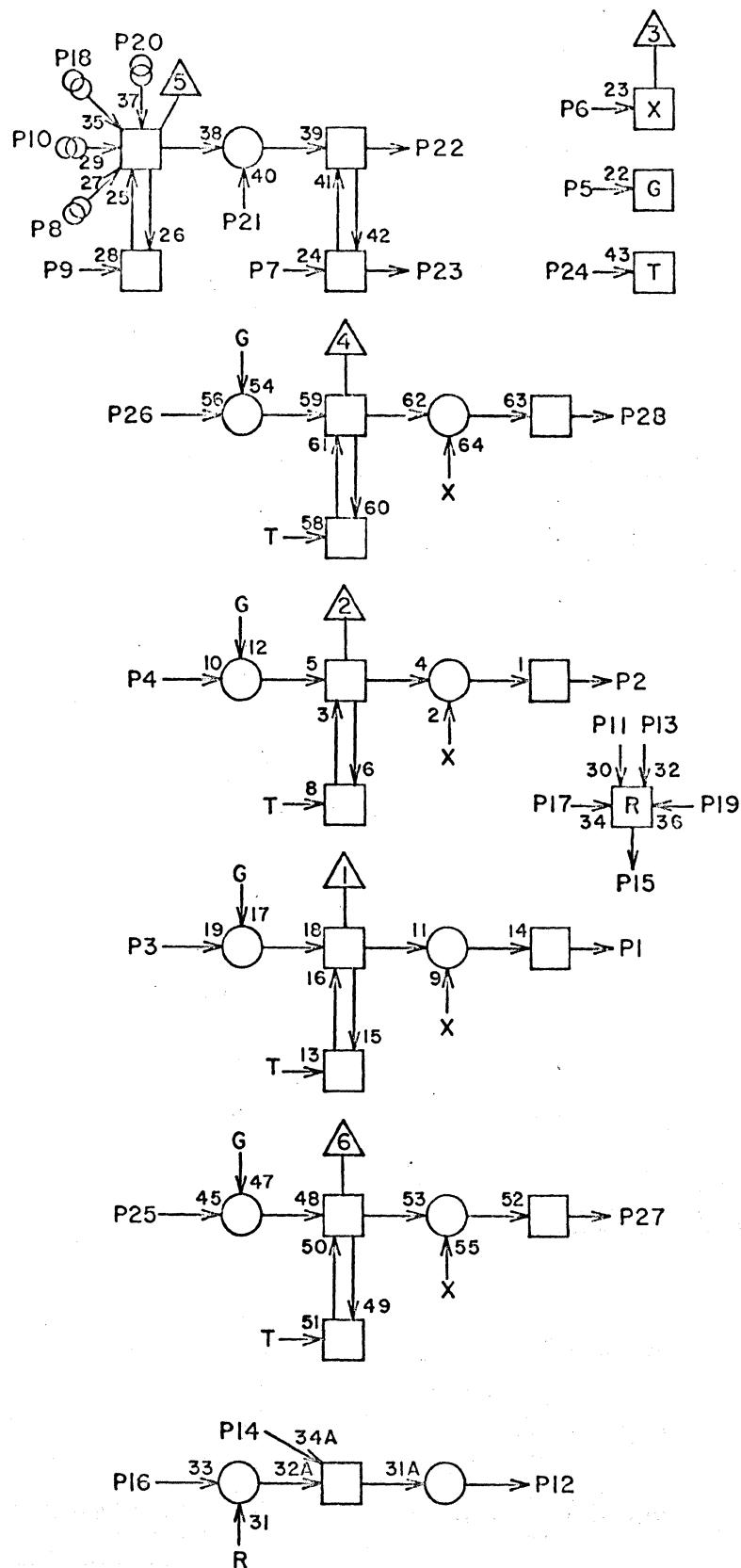
JACK PIN LG
CIRCUIT SPECIFICATION
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60042700 Rev. U

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JACK PIN LG
CIRCUIT SPECIFICATION

11827600

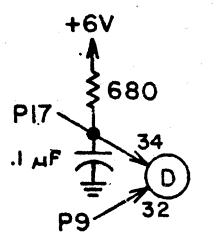
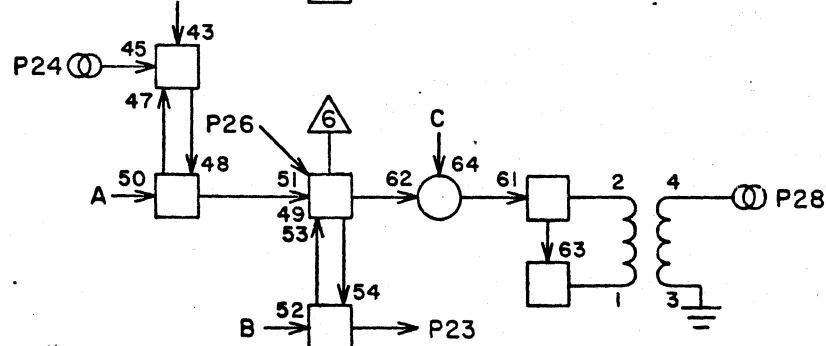
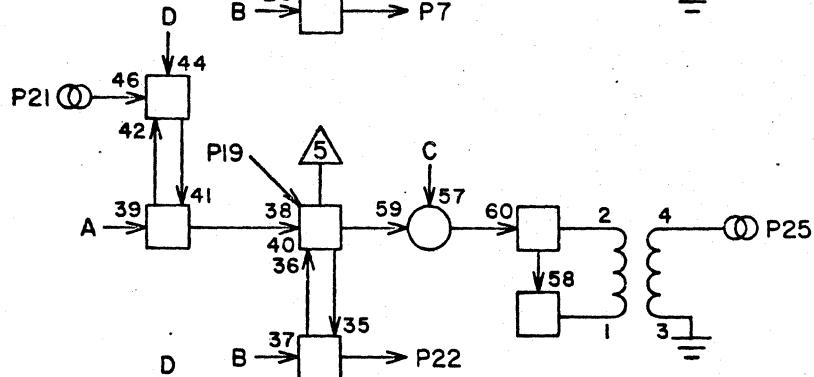
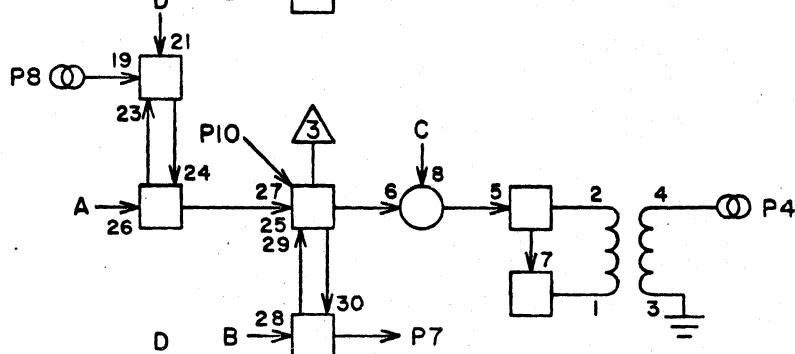
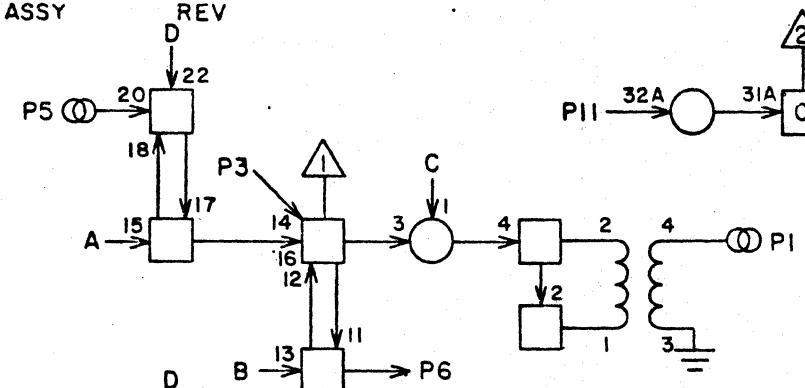
60042700 Rev. U

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P12 → 31 → B

P15 → 34A → P13

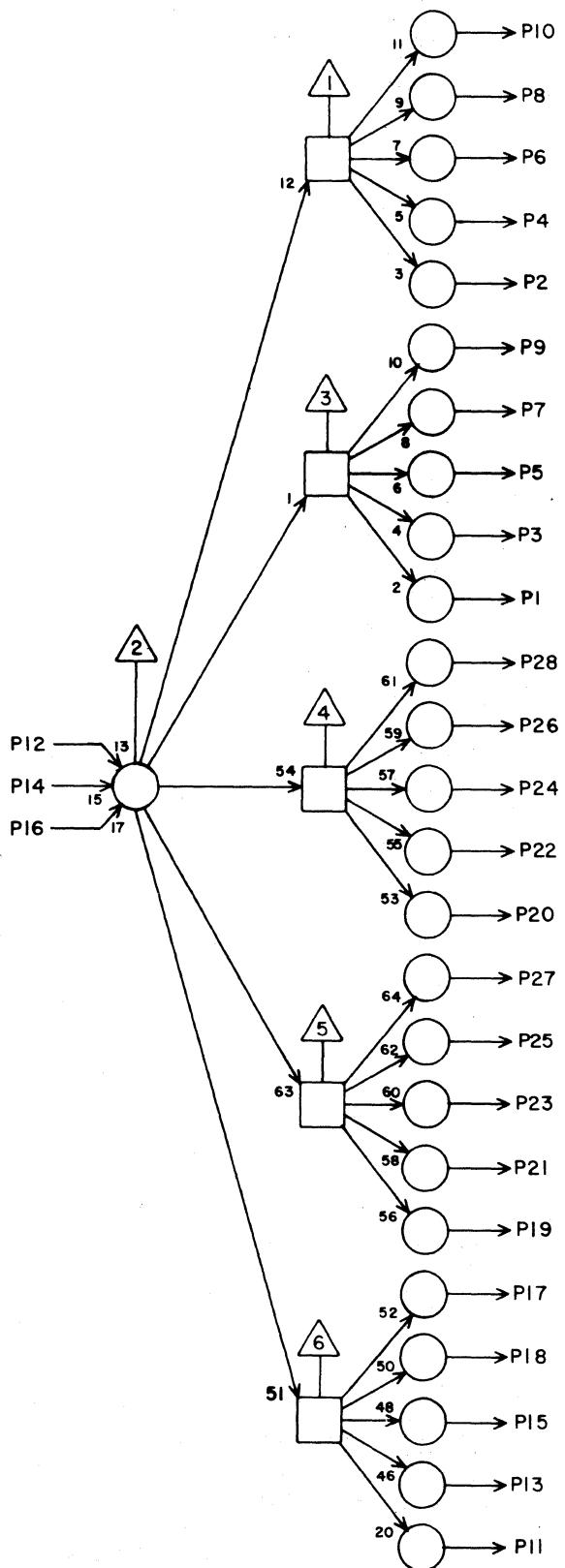
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JACK PIN LG
 SEE CIRCUIT SPECIFICATION
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 60042700 Rev Y

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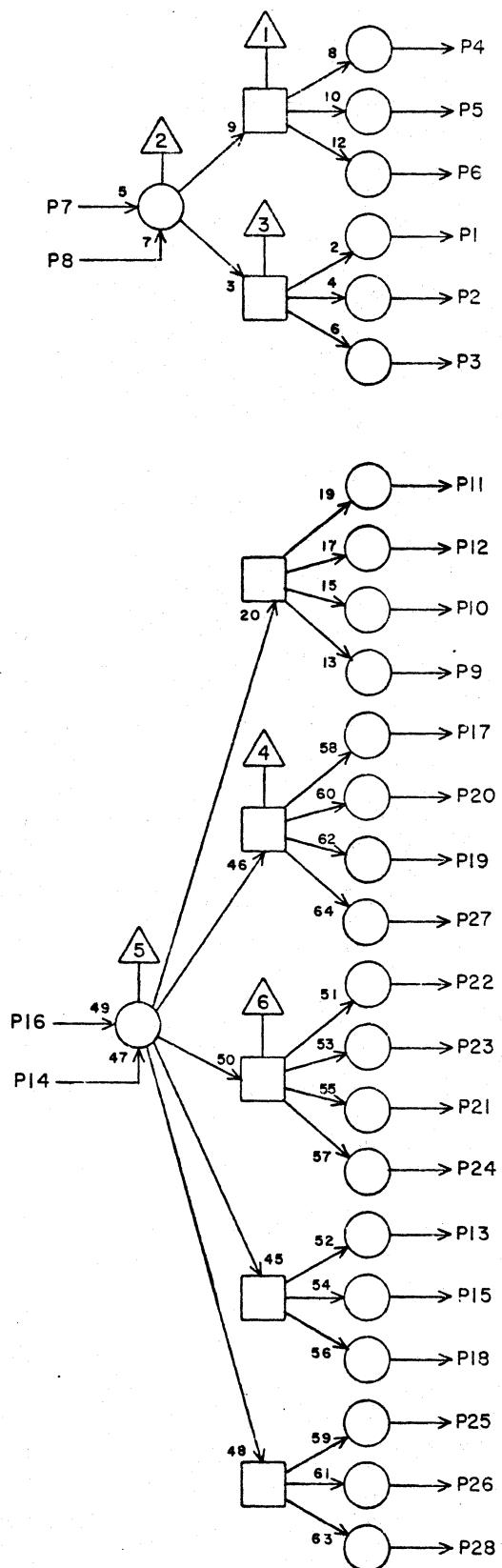
CIRCUIT SPECIFICATION II827600

60042700 Rev. P

LS 63040700
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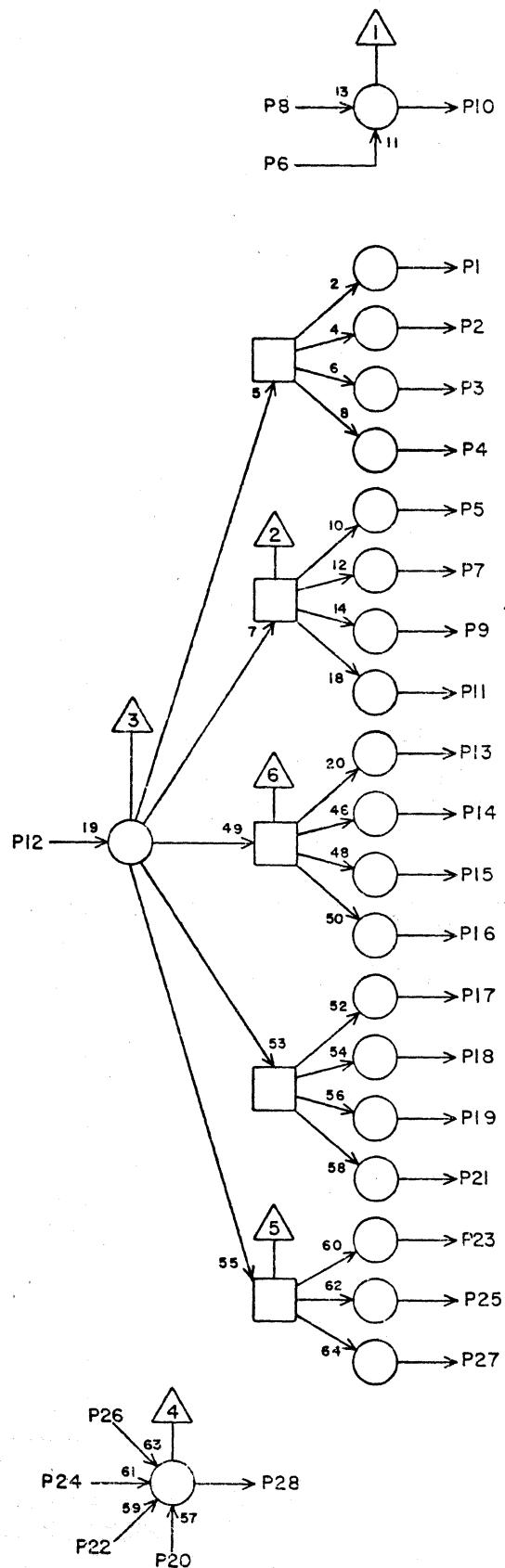
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CIRCUIT SPECIFICATION II827600
60042700 Rev. J

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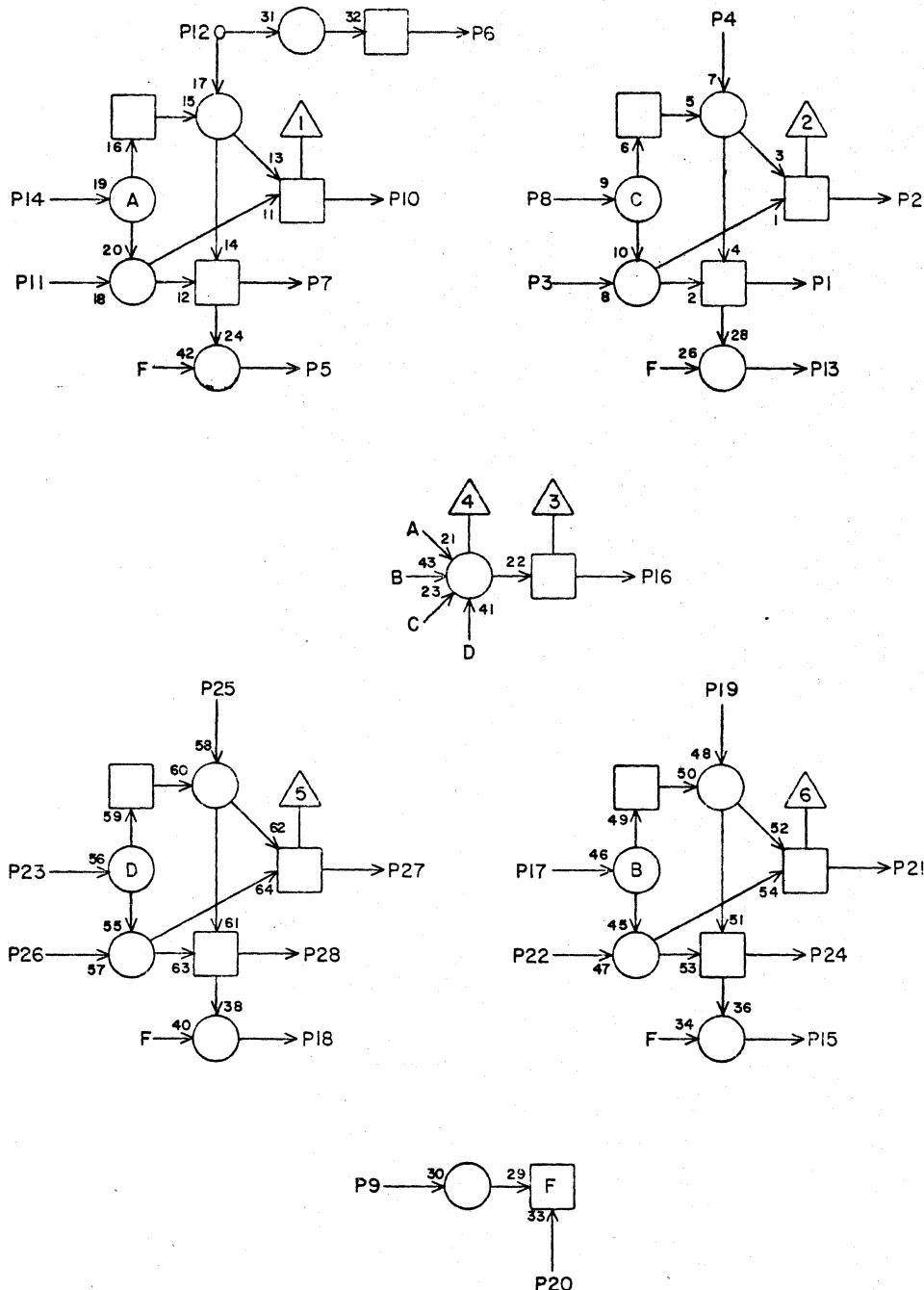
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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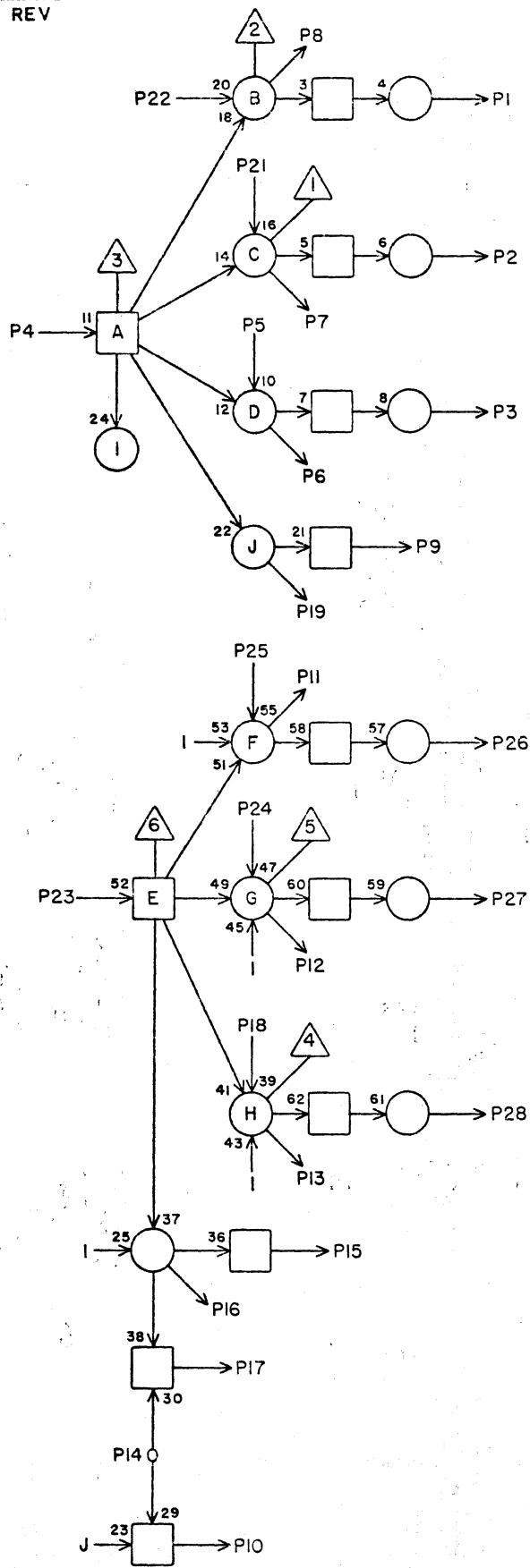
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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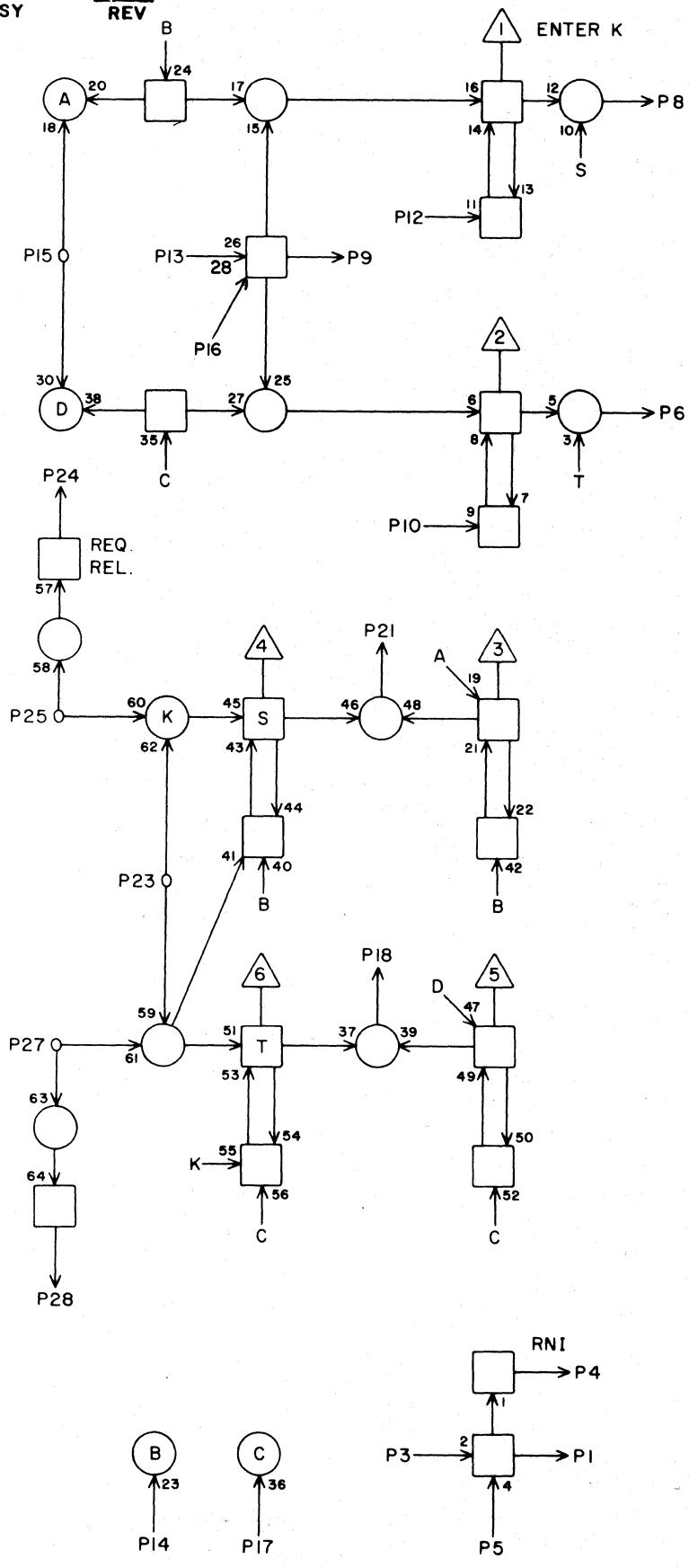
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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JACK PIN LG

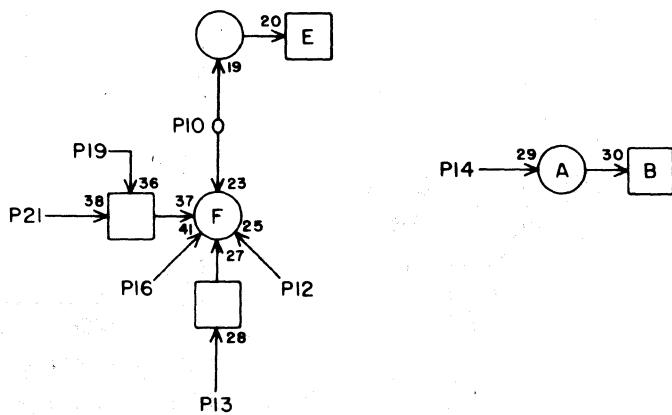
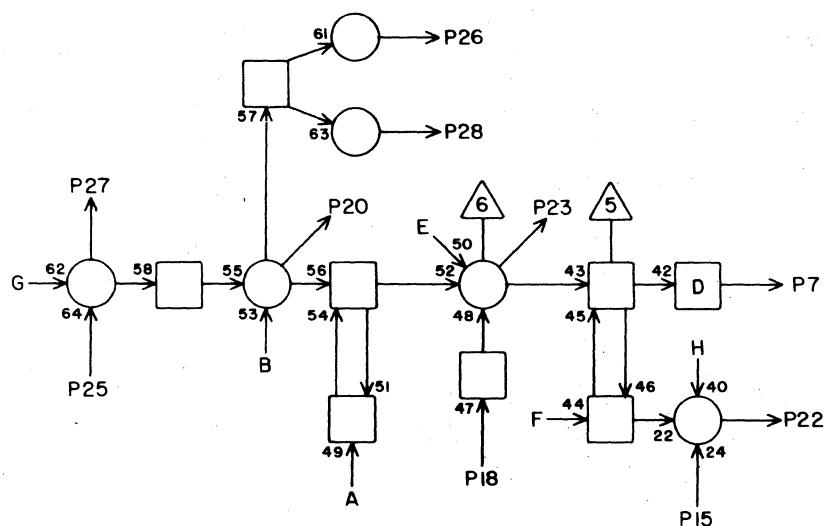
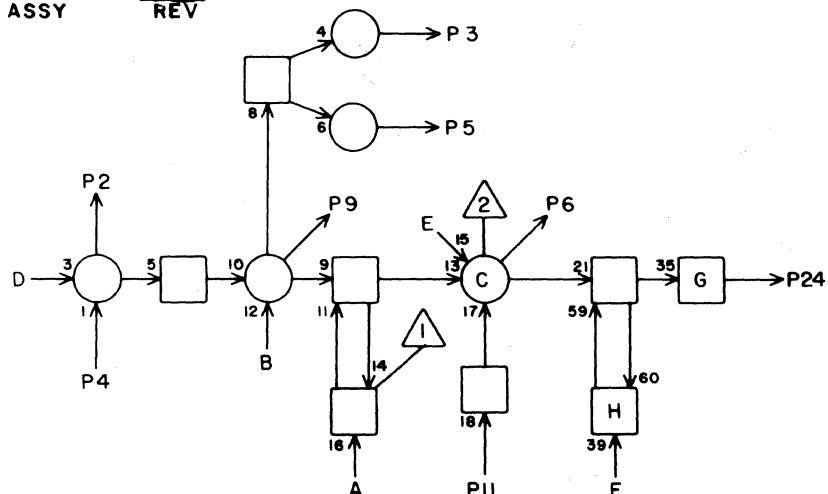
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

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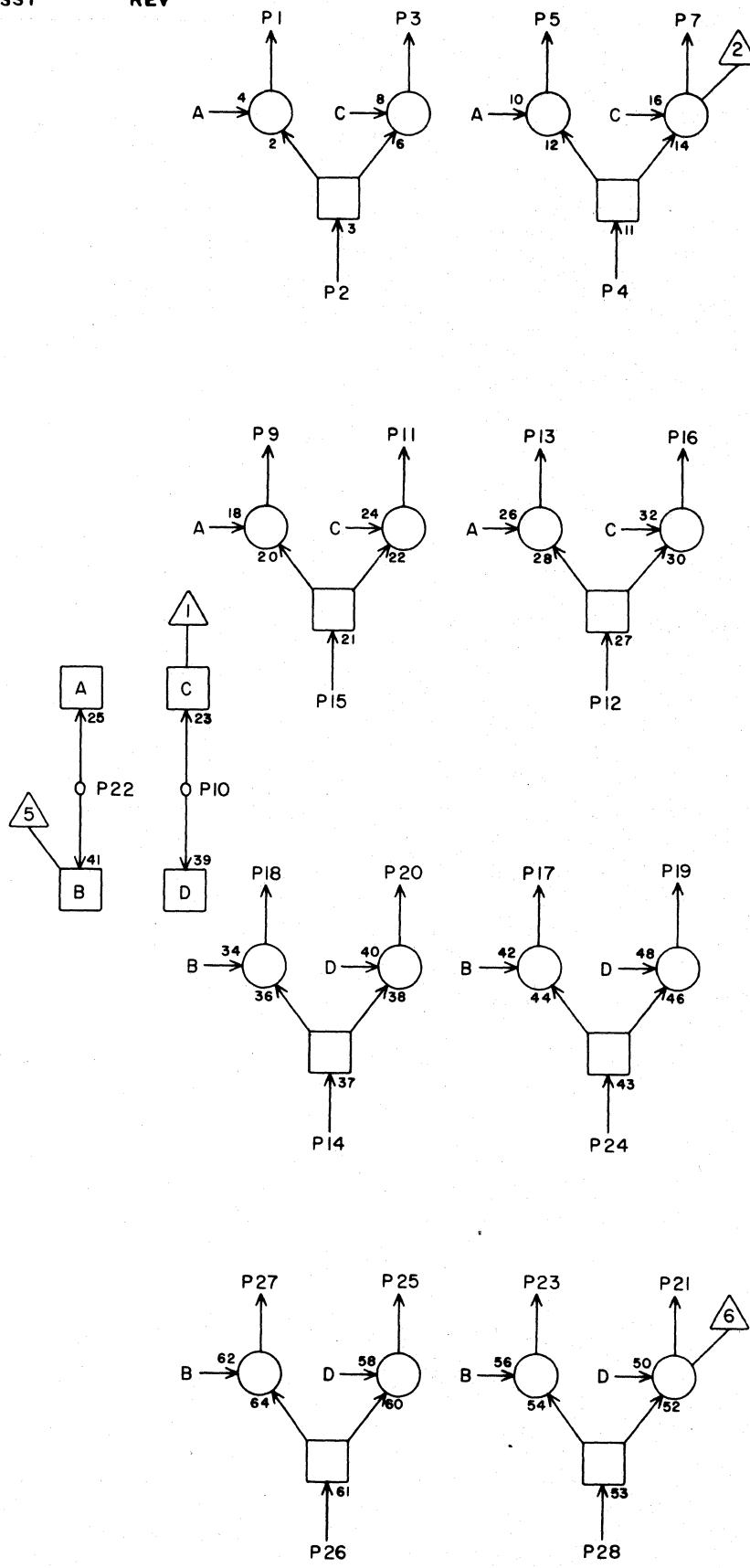
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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JACK PIN LG

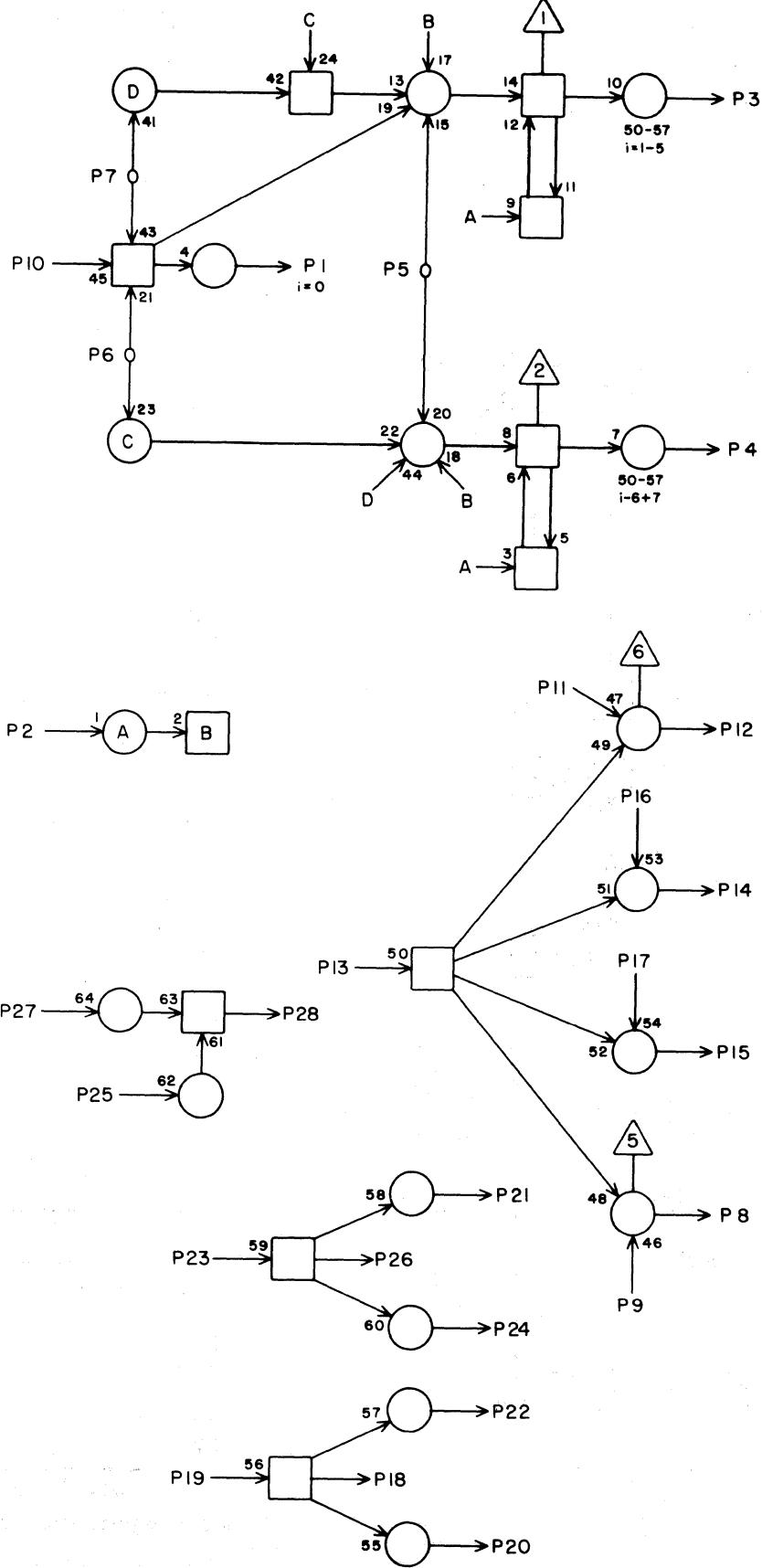
CIRCUIT SPECIFICATION 11827600

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JACK PIN LG

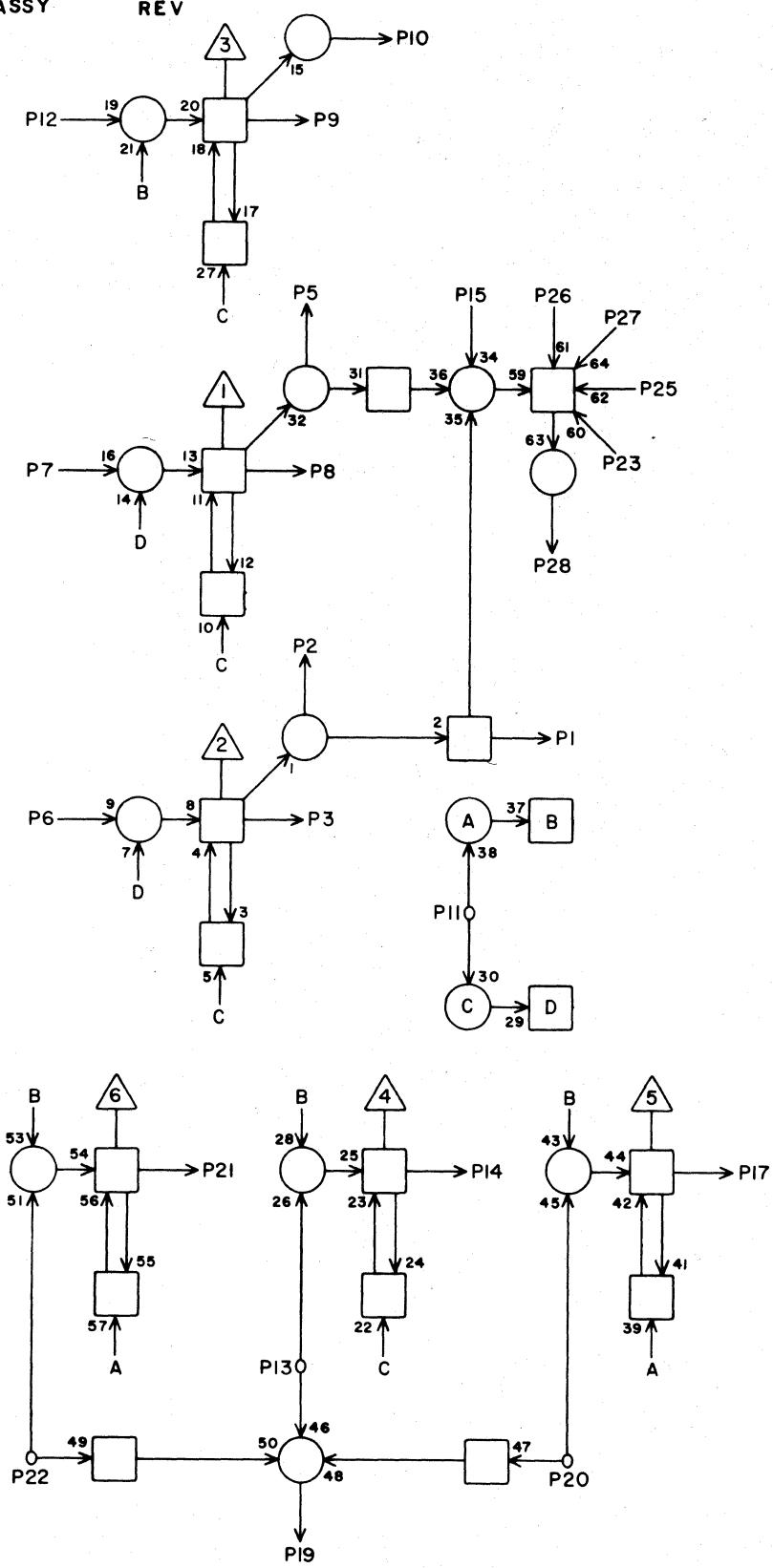
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60042700 Rev. J

LS 63041500
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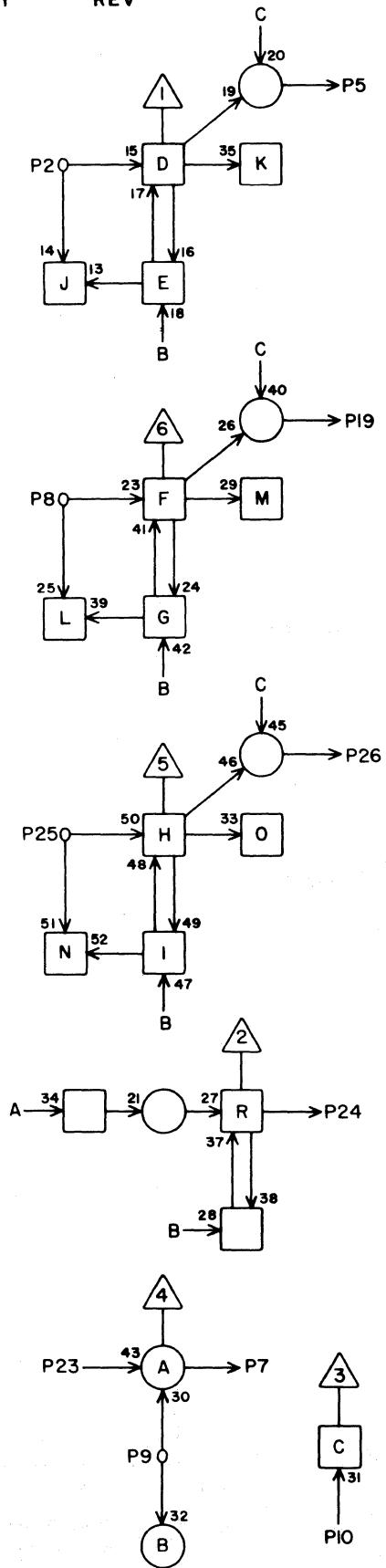
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CIRCUIT SPECIFICATION 11827600

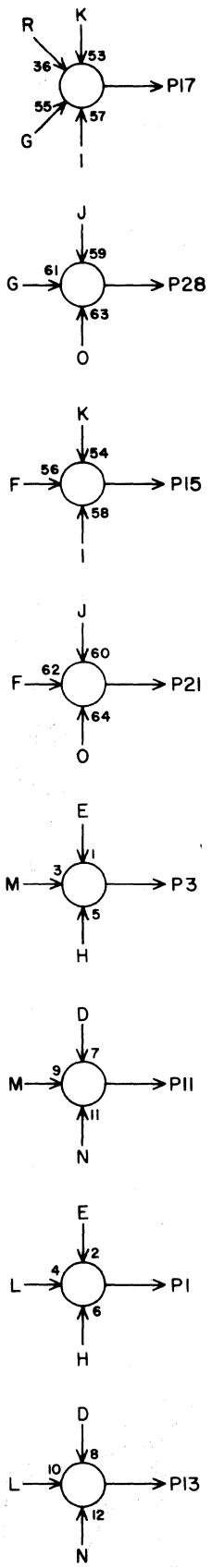
60042700 Rev. J

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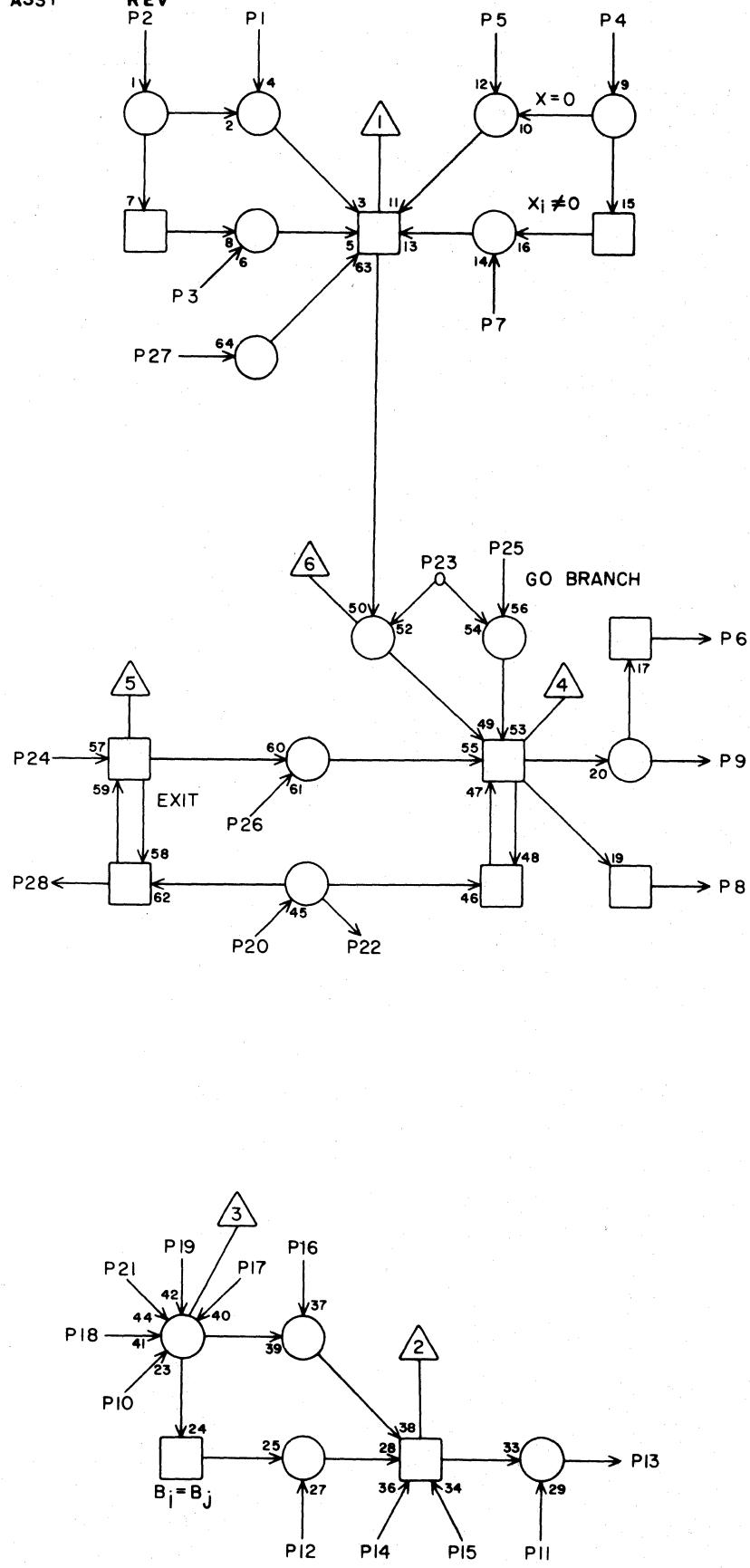
JACK PIN LG

CIRCUIT SPECIFICATION II827600

60042700 Rev. J

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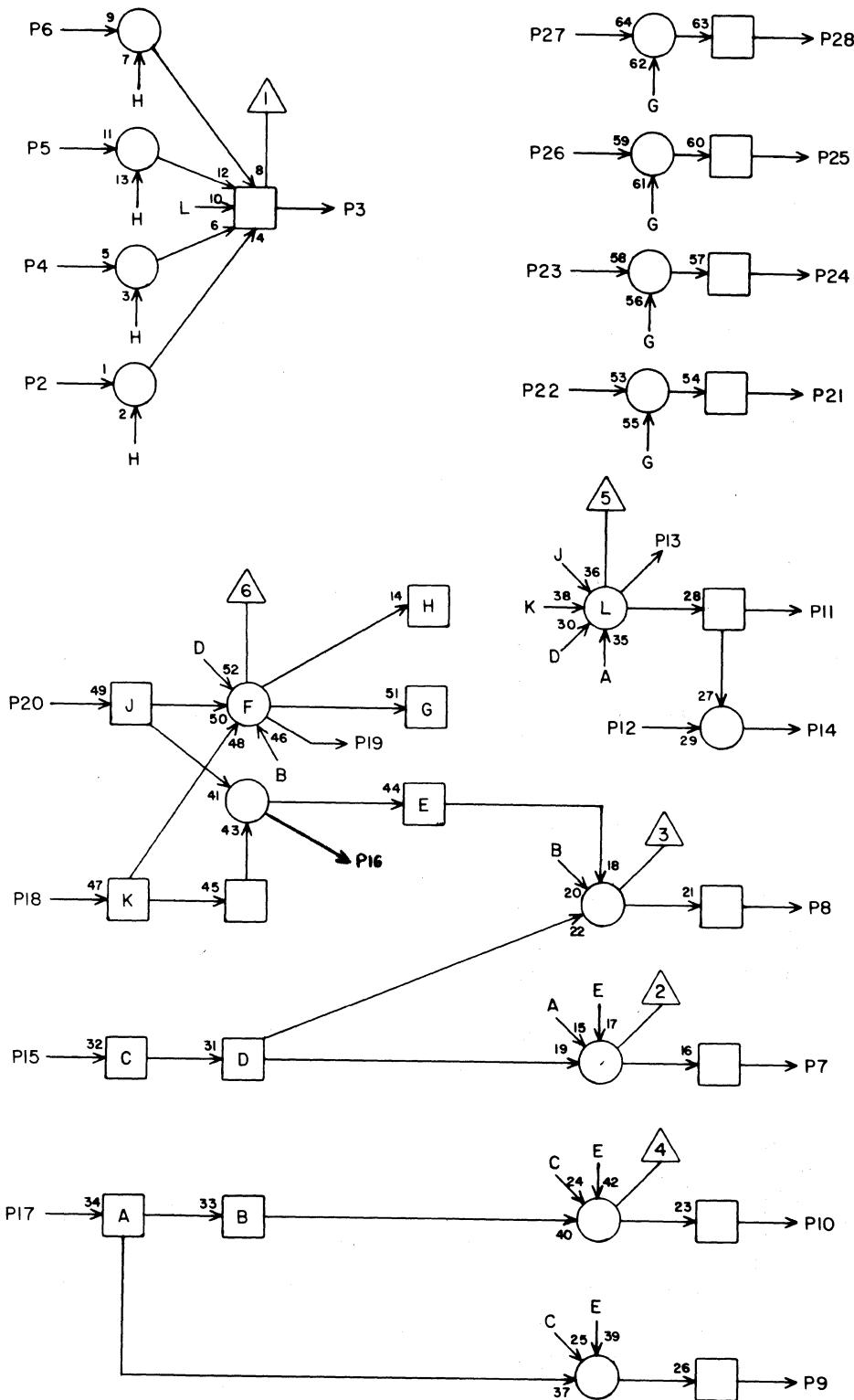
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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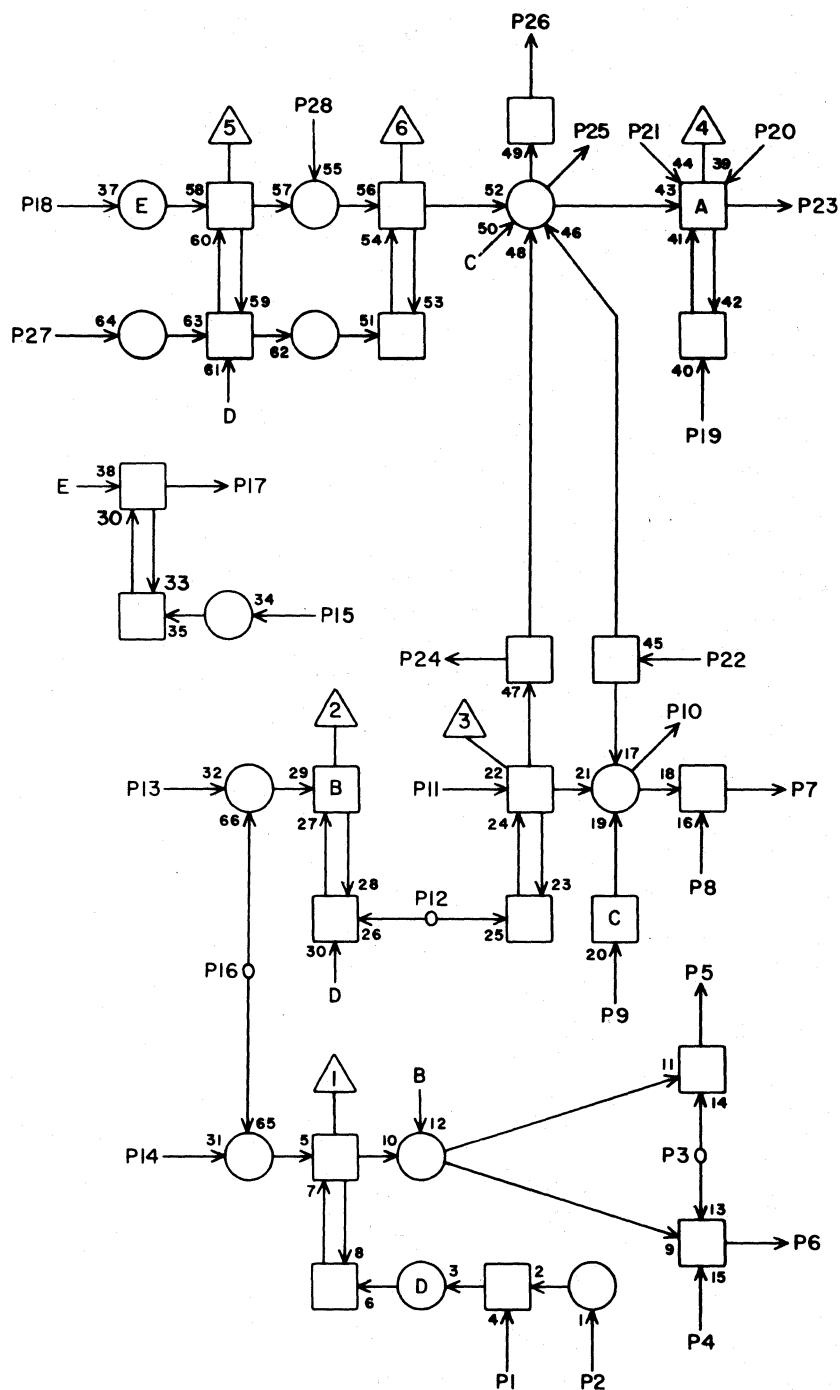
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CIRCUIT SPECIFICATION 11827600
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JACK PIN LG

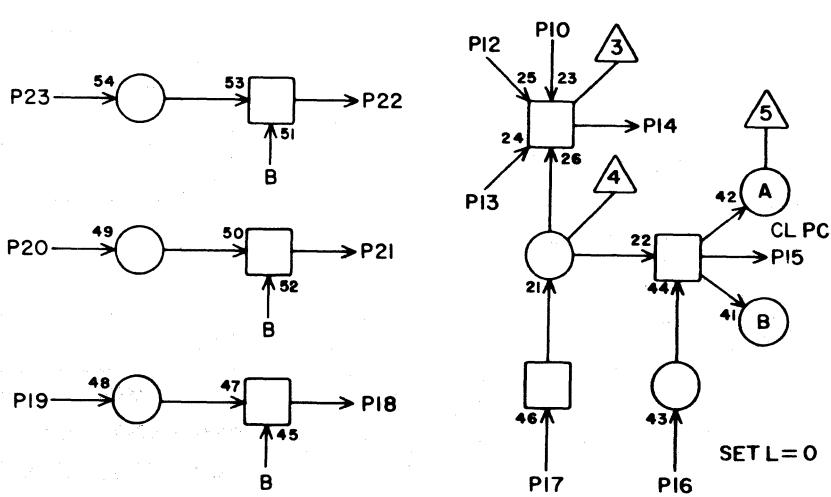
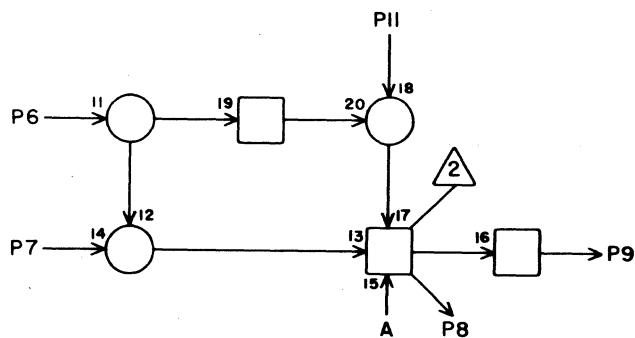
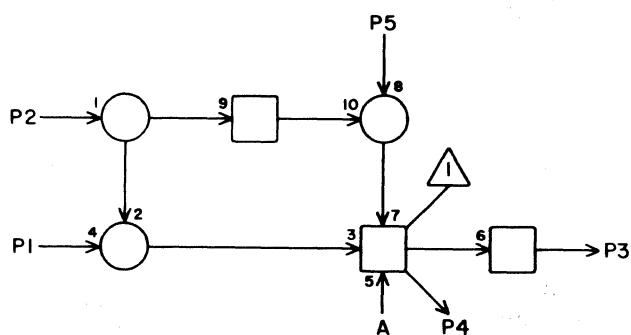
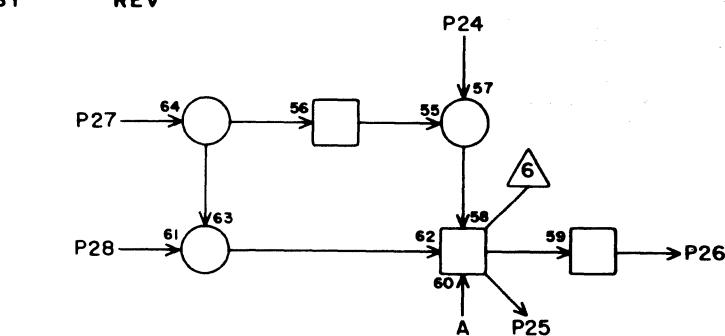
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63042000
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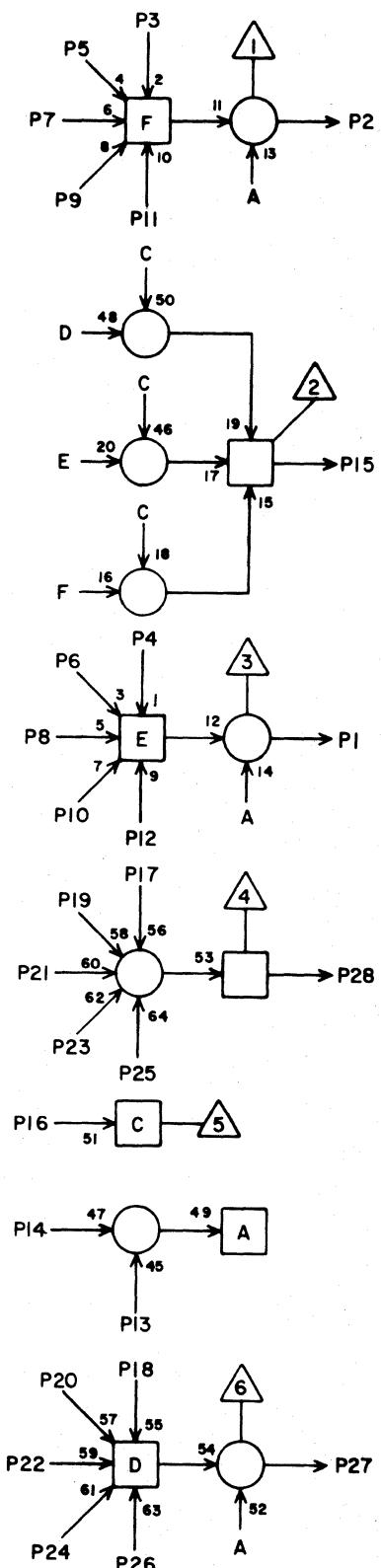
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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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JACK PIN LG

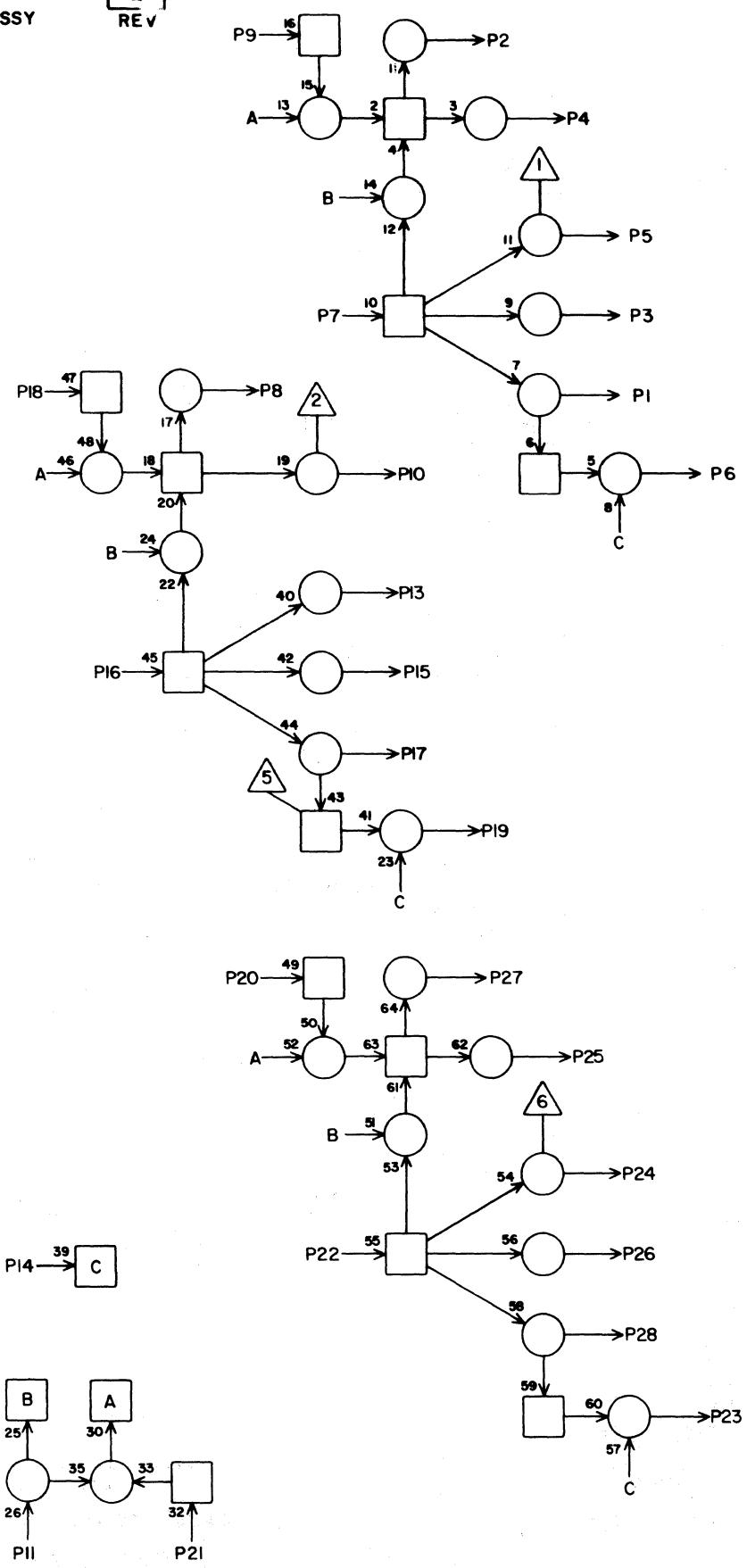
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63042200
ASSY

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JACK PIN LG

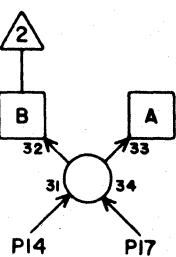
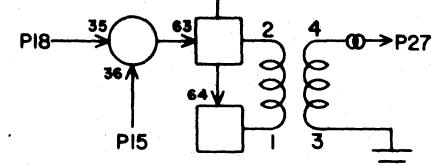
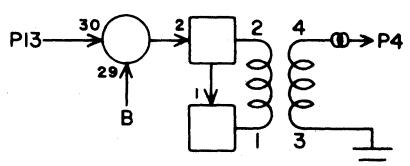
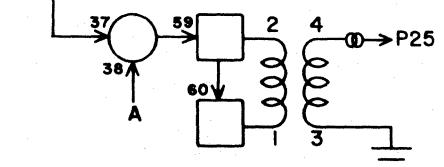
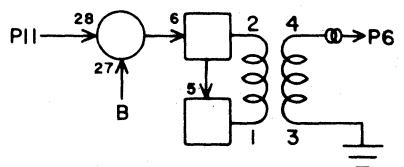
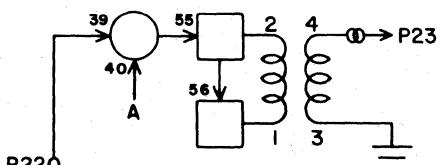
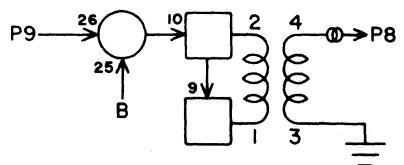
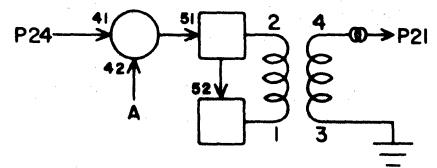
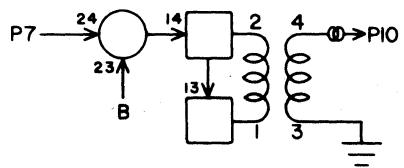
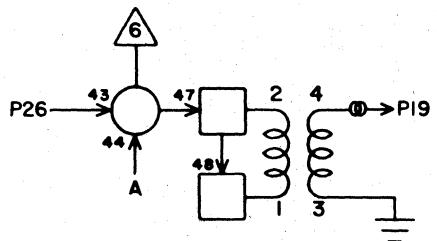
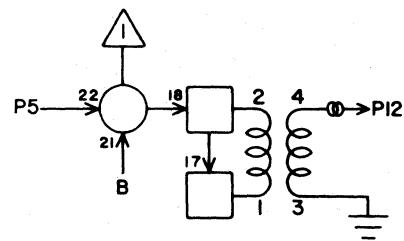
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63042300

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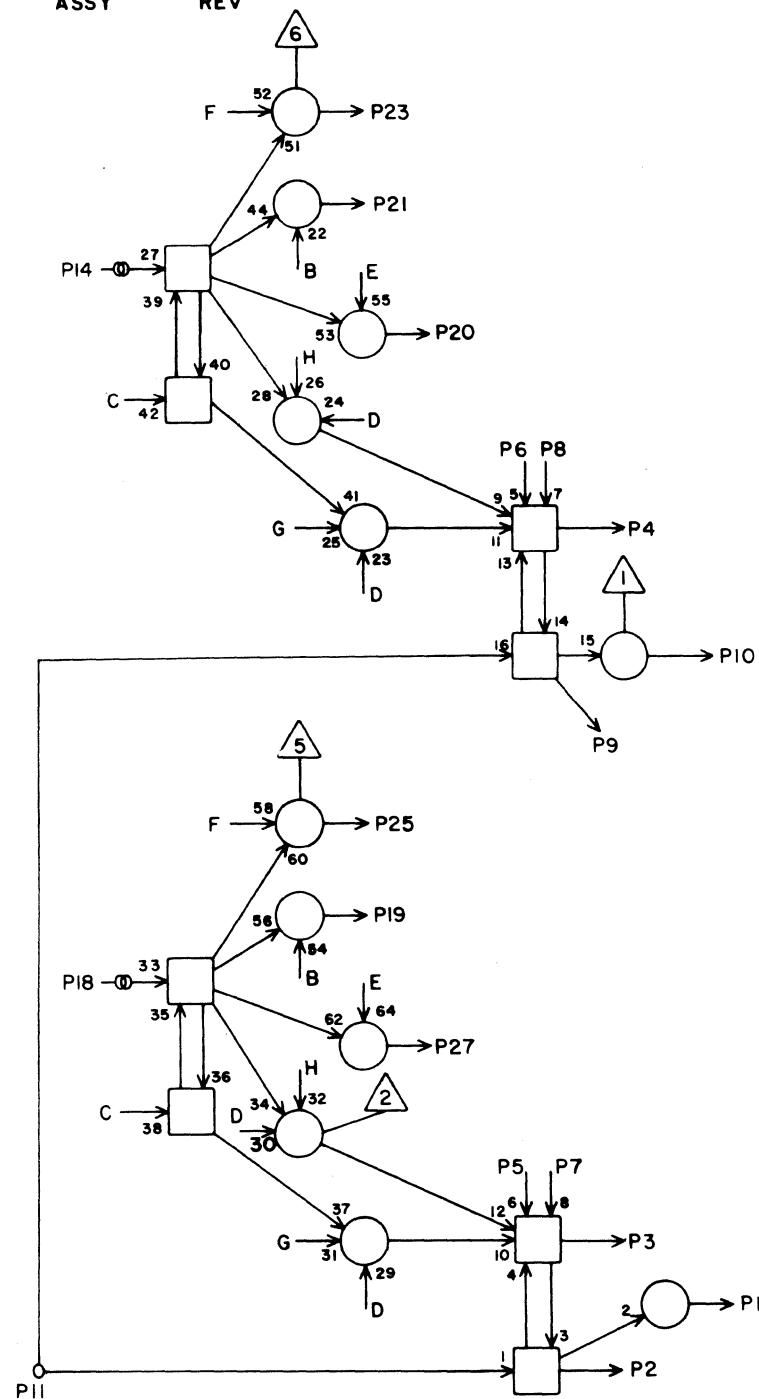
CIRCUIT SPECIFICATION U1827600

60042700 Rev. J

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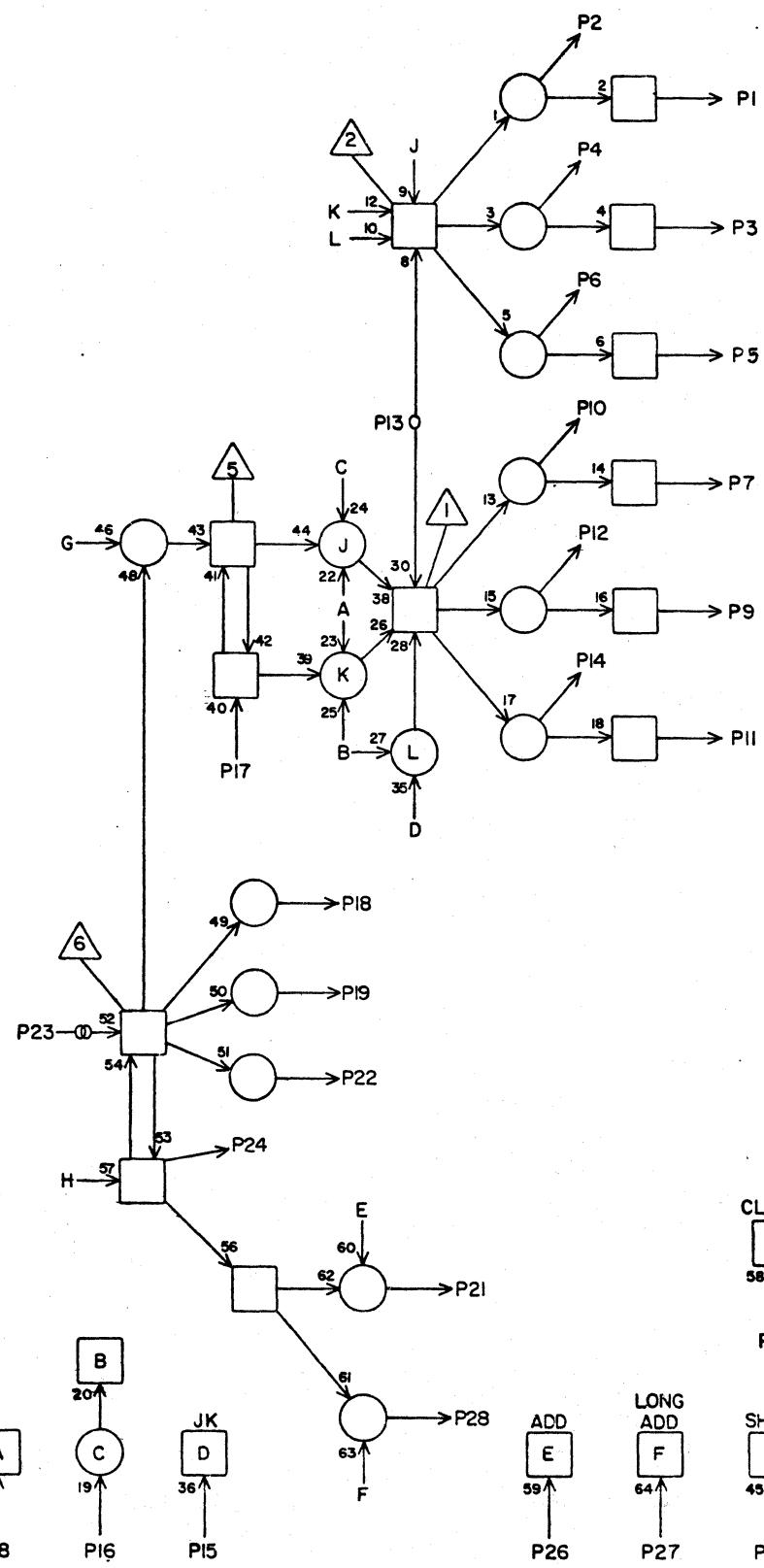
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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JACK PIN LG

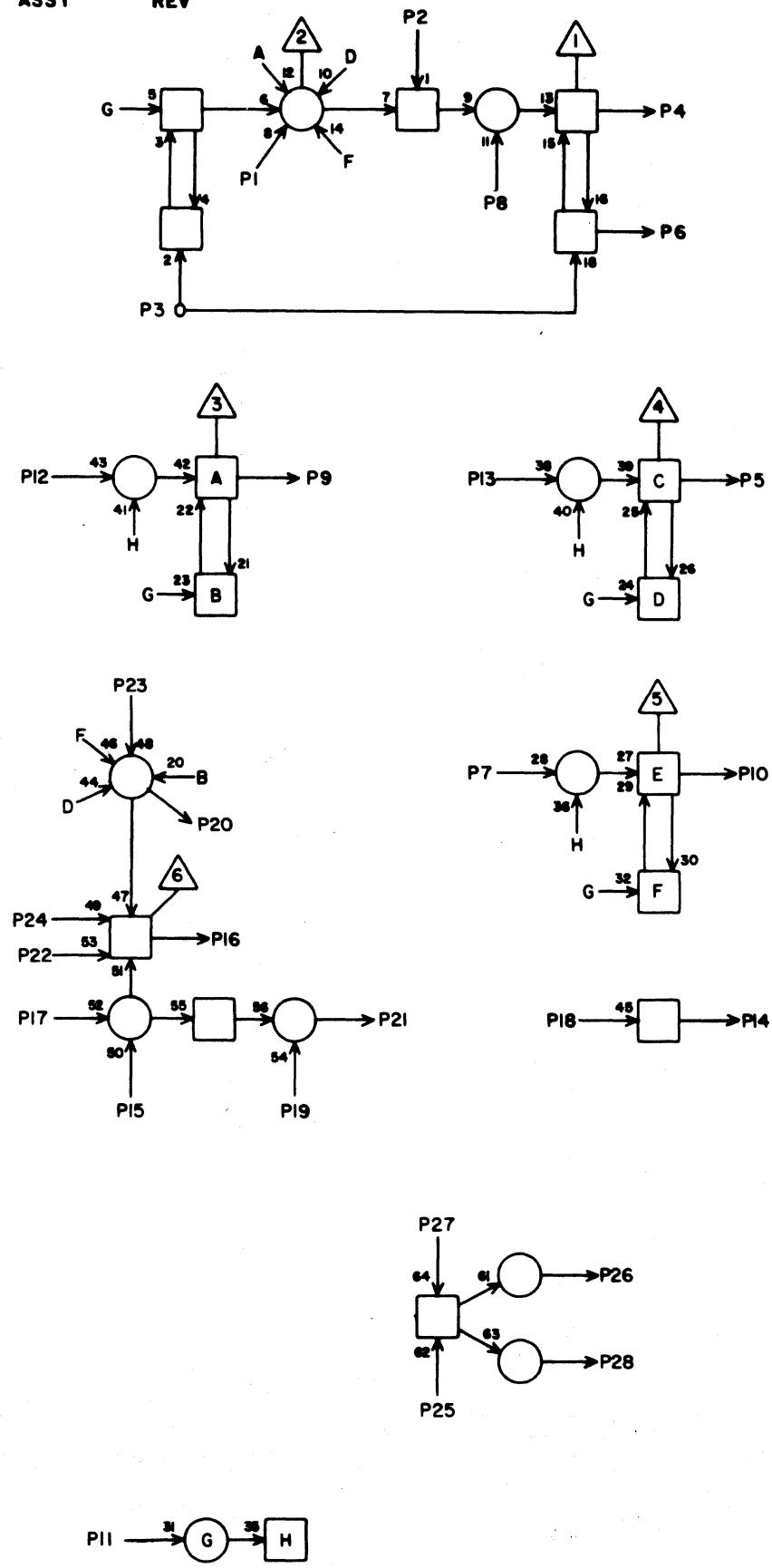
CIRCUIT SPECIFICATION 11827600

60042700 Rev. Y

LS 63042600
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JACK PIN LG
CIRCUIT SPECIFICATION 11827600

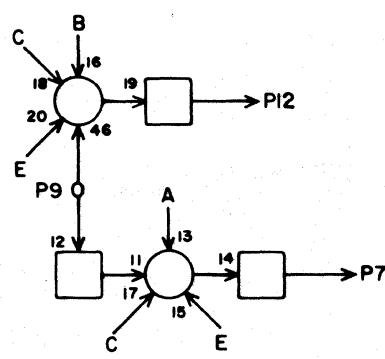
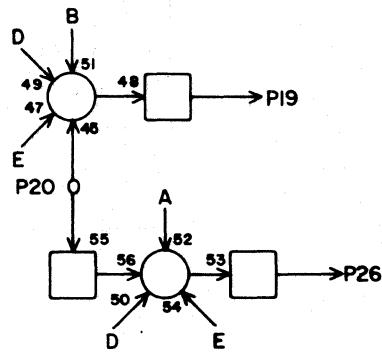
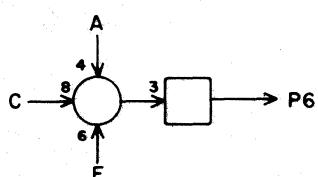
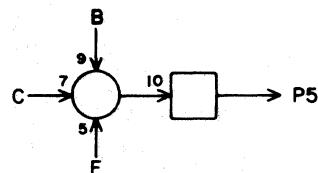
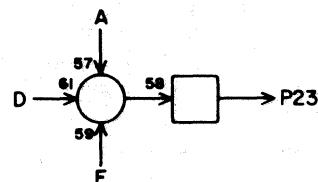
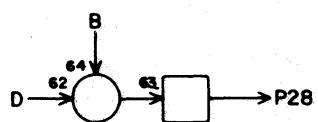
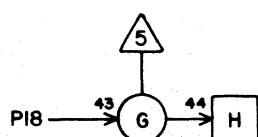
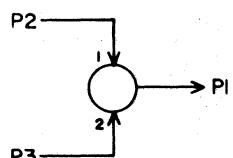
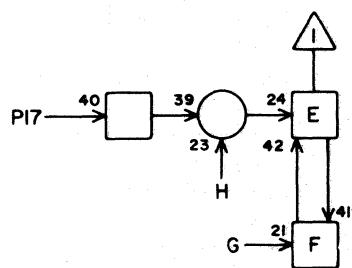
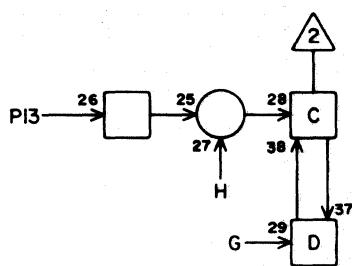
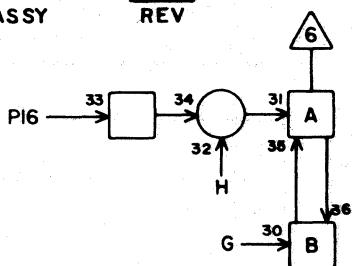
60042700 Rev. J

LS 63042700

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JACK PIN LG

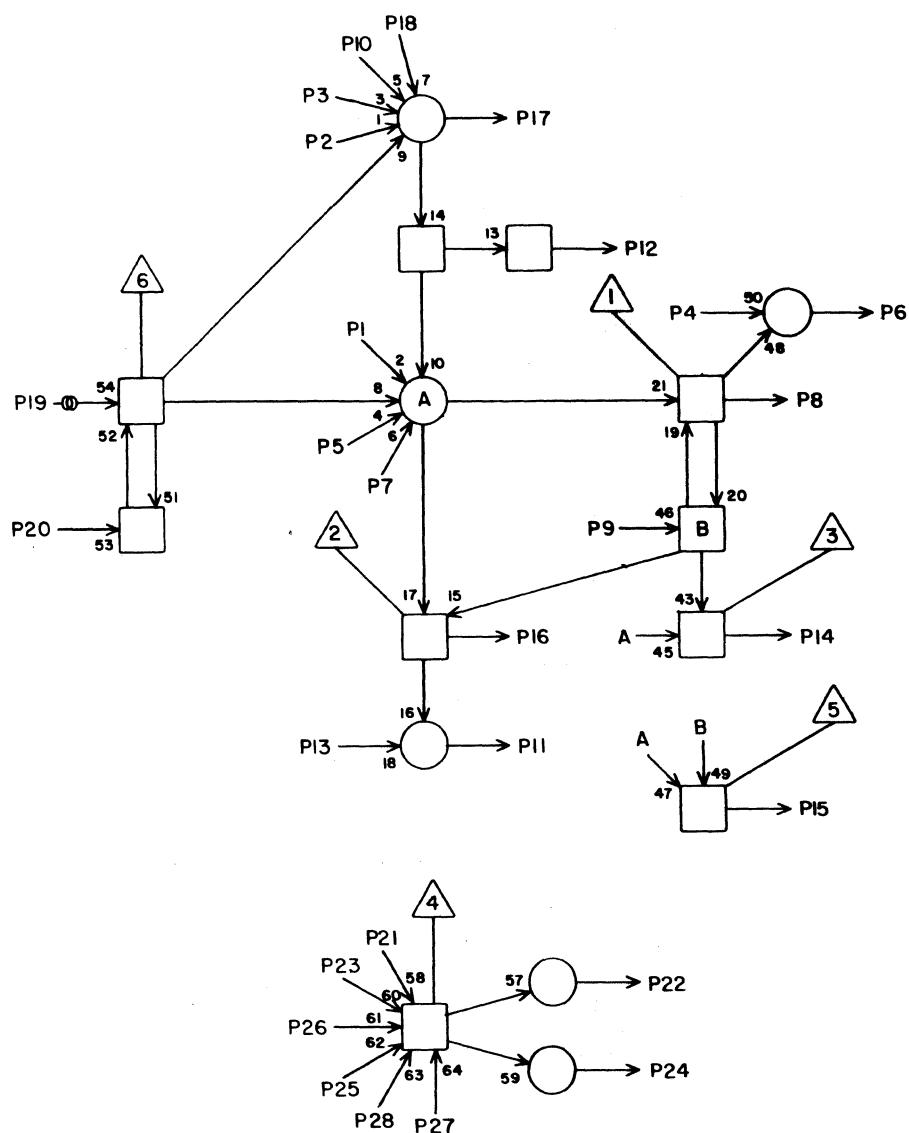
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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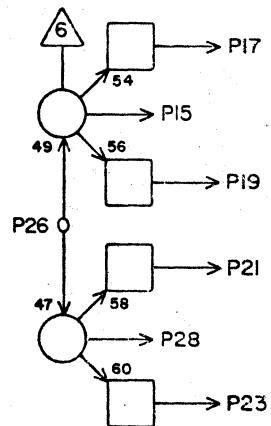
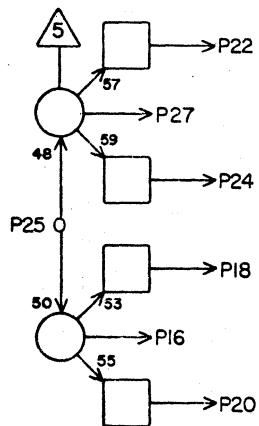
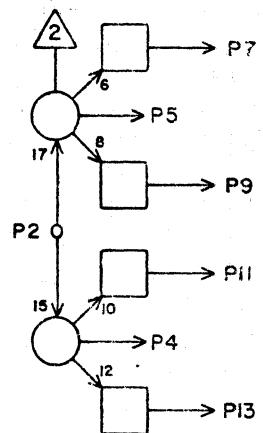
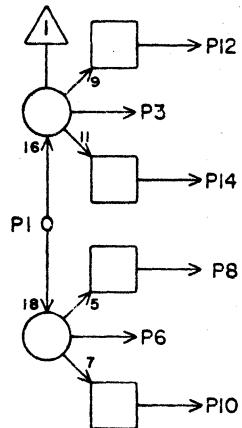
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

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JACK PIN LG

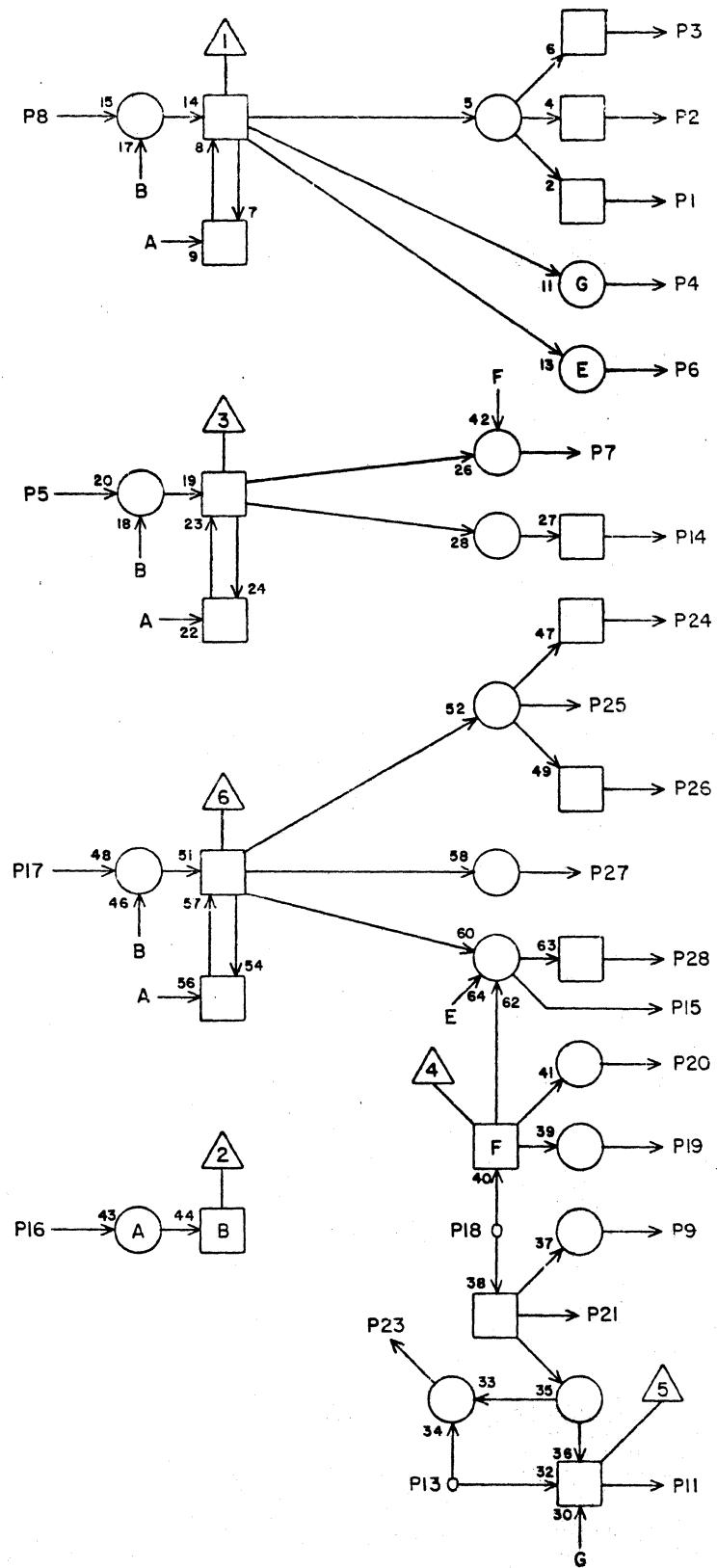
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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JACK PIN LG

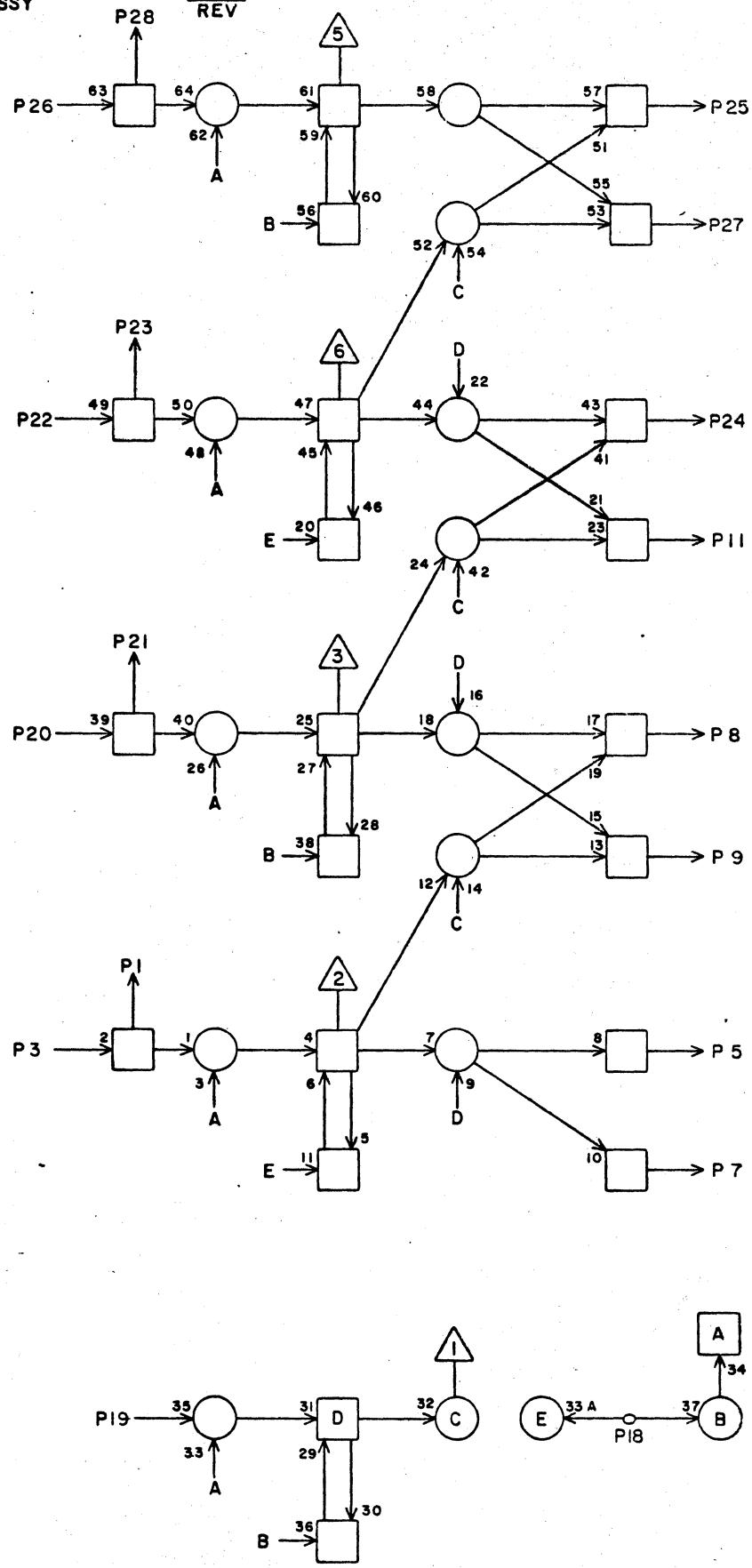
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60042700 Rev. J

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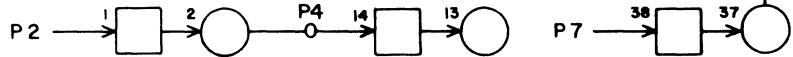
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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

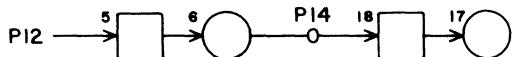
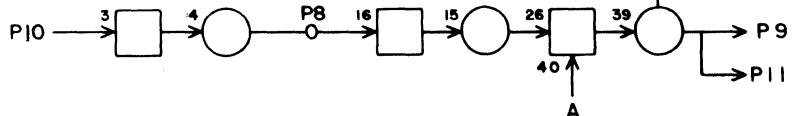
LS 63043200
ASSY

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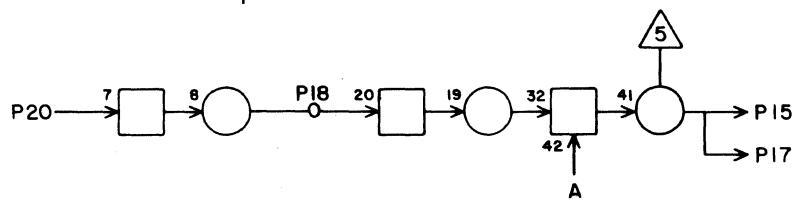
DA
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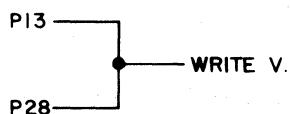
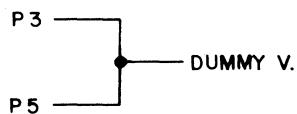
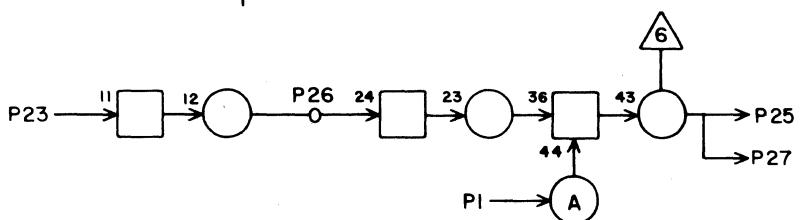
||—OP6



||—OP16



||—OP24



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CIRCUIT SPECIFICATION 11827600

60042700 Rev. J



LS 63043400
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JACK PIN LG

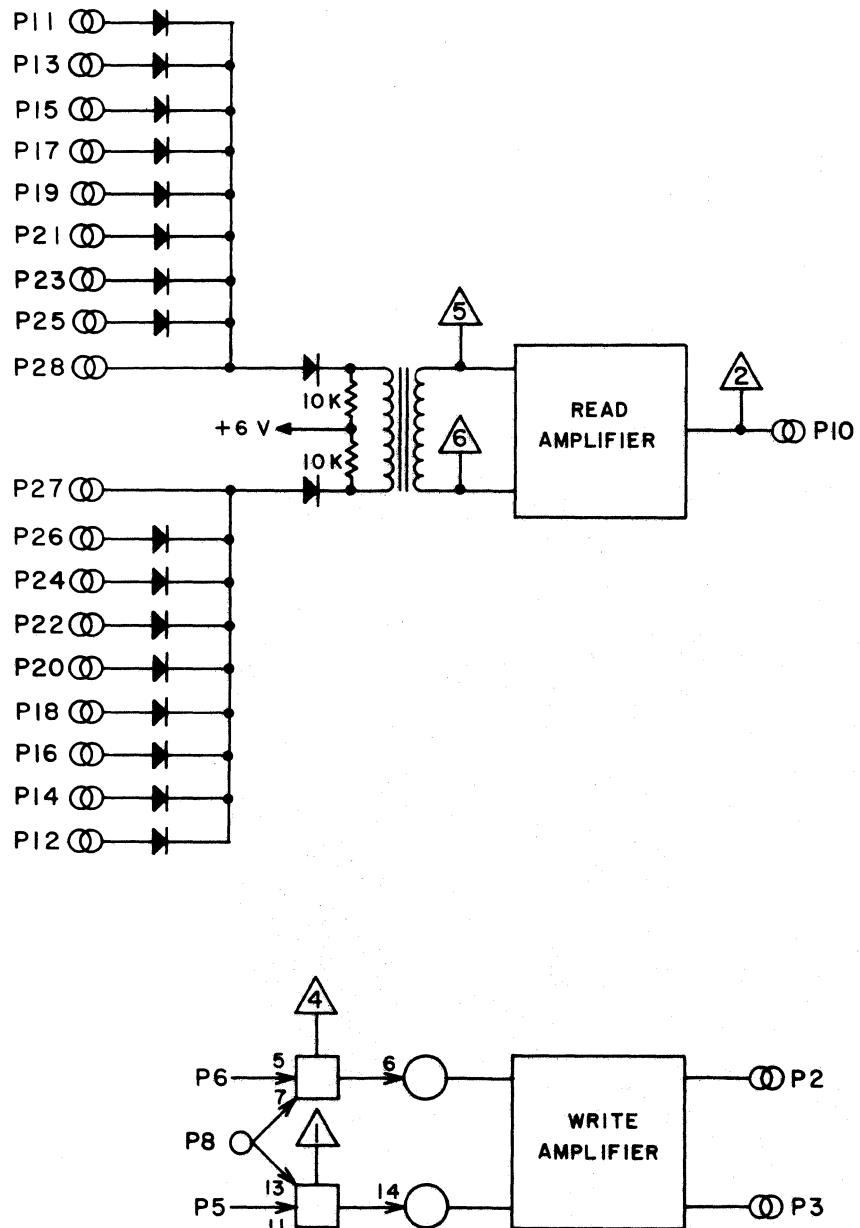
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 18117300 D
ASSY REV

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Page 1 of 3

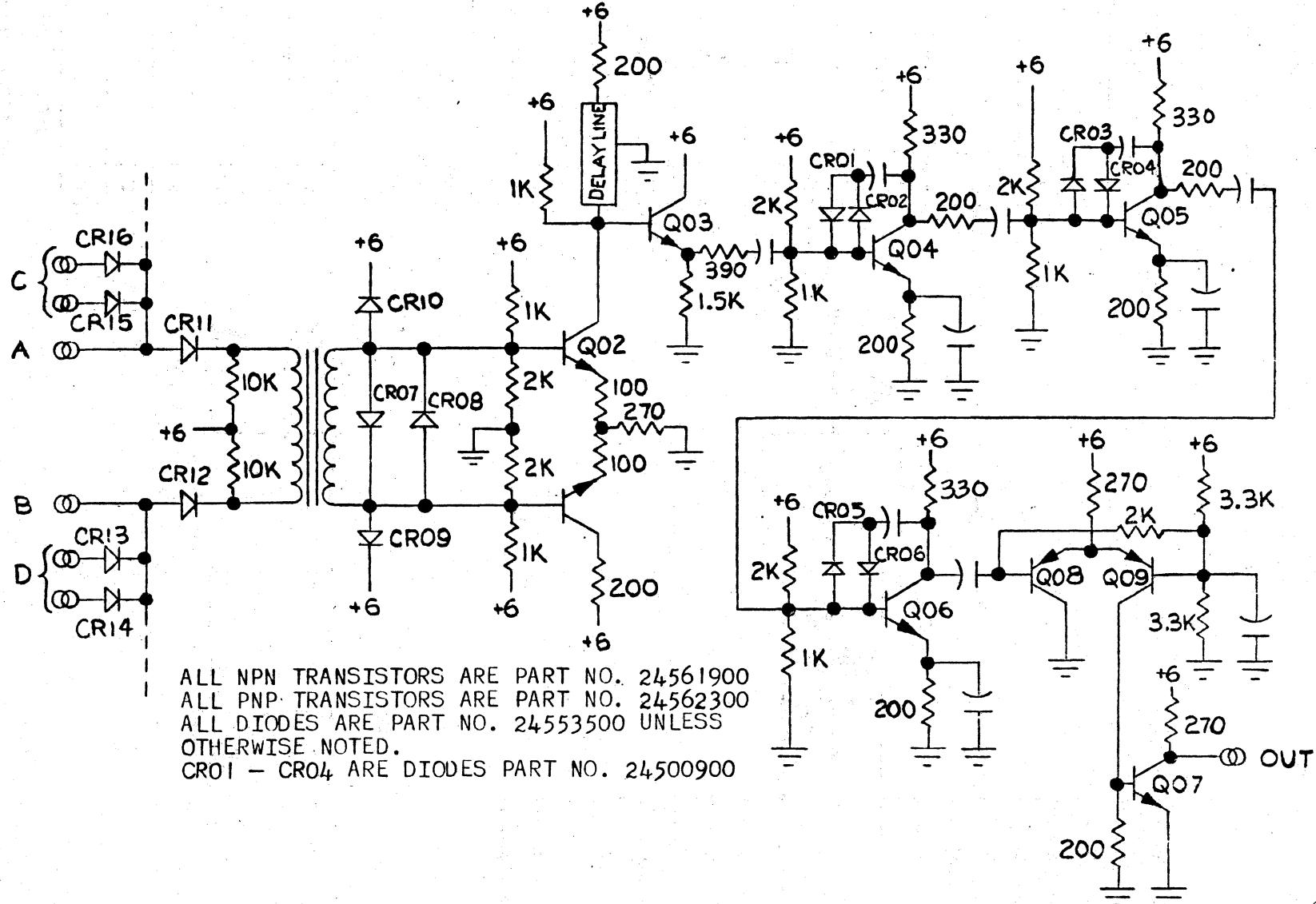


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JACK PIN LG

60042700 Rev. W

READ AMPLIFIER

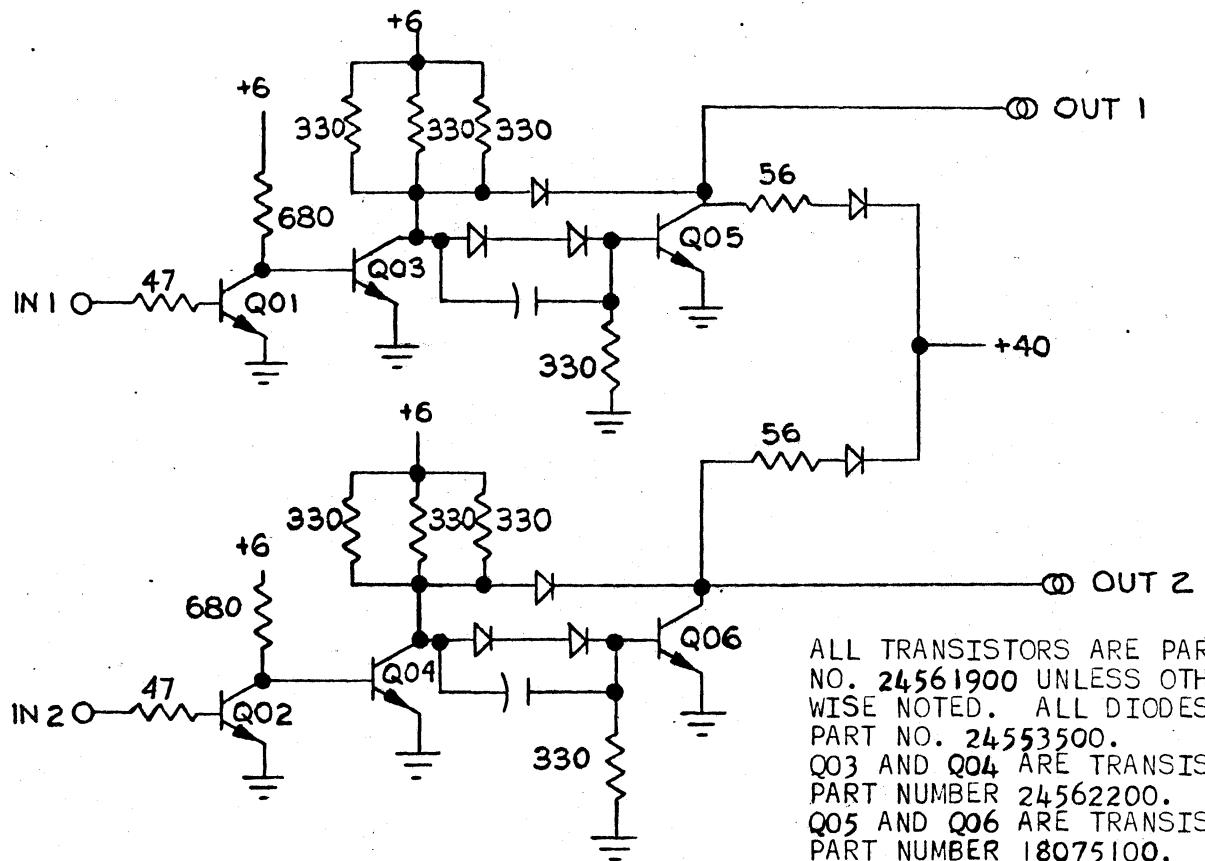


L.S. 18117300

DE

PAGE 3
REV. D

WRITE AMPLIFIER



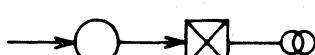
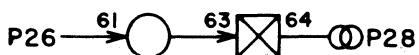
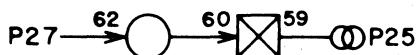
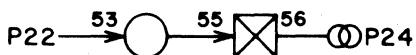
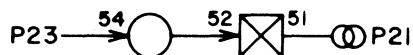
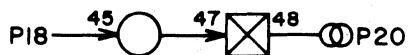
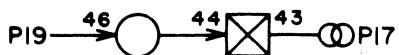
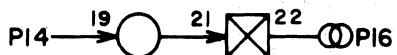
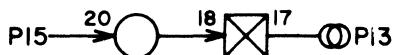
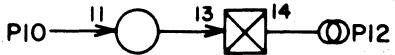
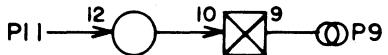
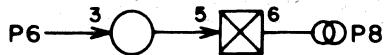
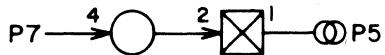
ELECTRICAL SCHEMATIC

LS 18117500
ASSY

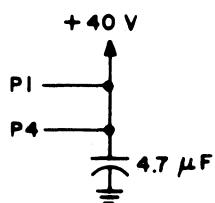
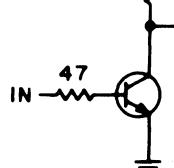
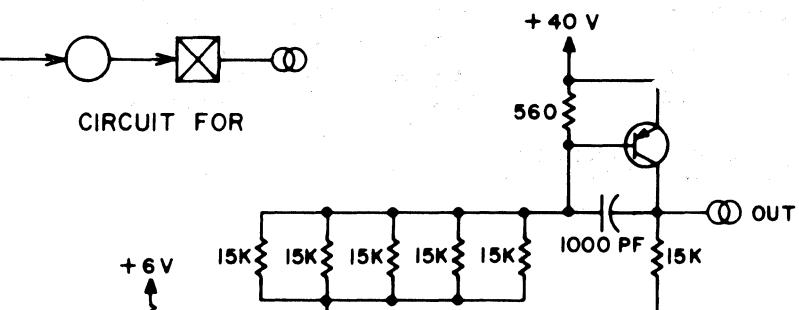
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Page 1 of 2



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JACK PIN LG

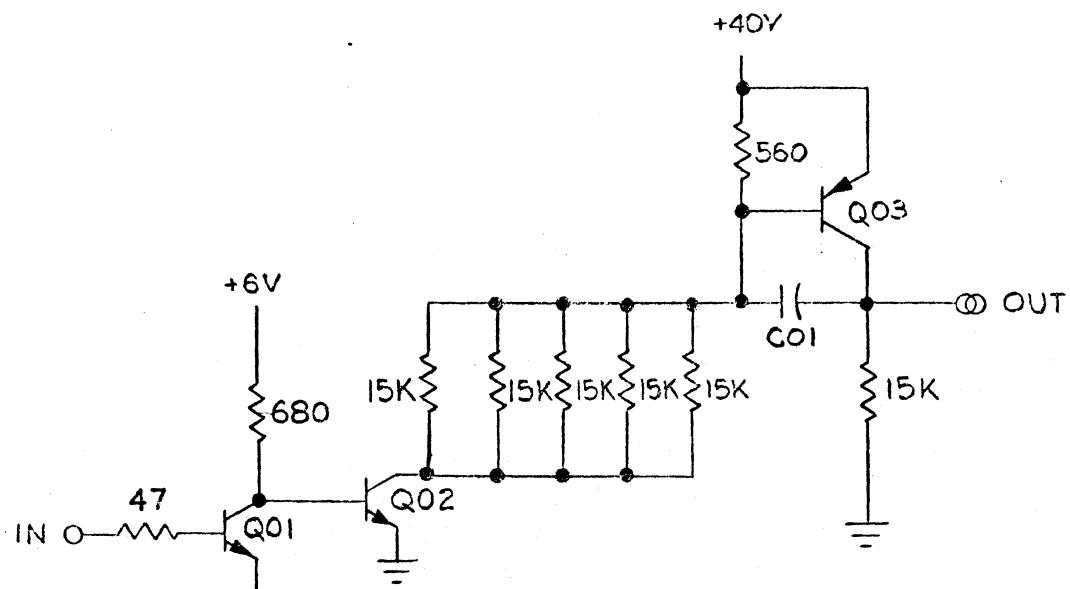
60042700 Rev. W

CAUTION:
AT LEAST 10 INPUTS MUST HAVE LOGIC 0
AT ANY GIVEN TIME. (OTHERWISE CARD WILL
DISSIPATE MORE THAN 4 WATTS).

L.S. 18117500

DF

PAGE 2
REV. D

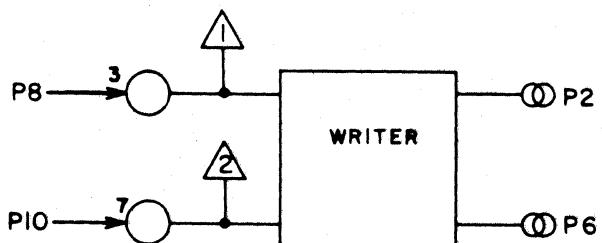
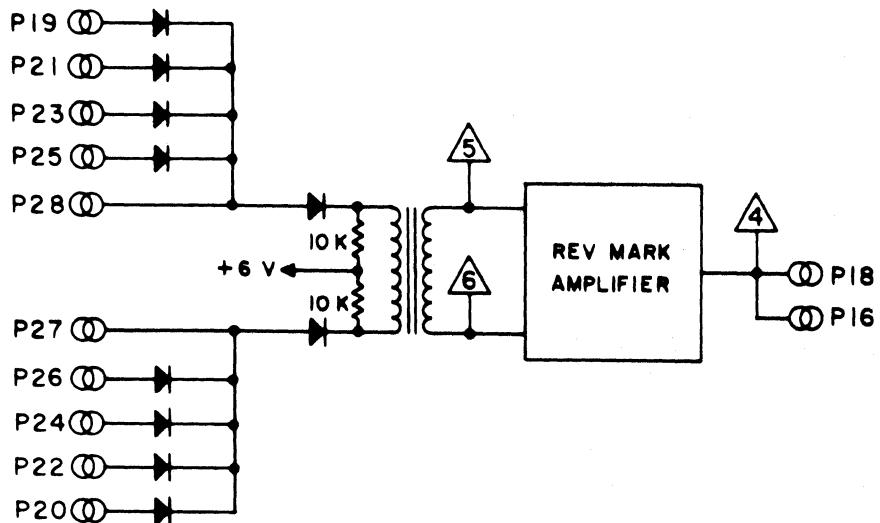


Q2 TRANSISTOR IS PART NO. 18075100
Q3 TRANSISTOR IS PART NO. 17942801

ELECTRICAL SCHEMATIC

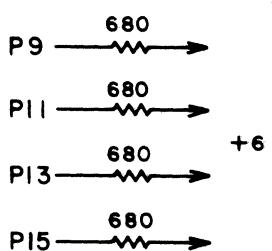


Page 1 of 3

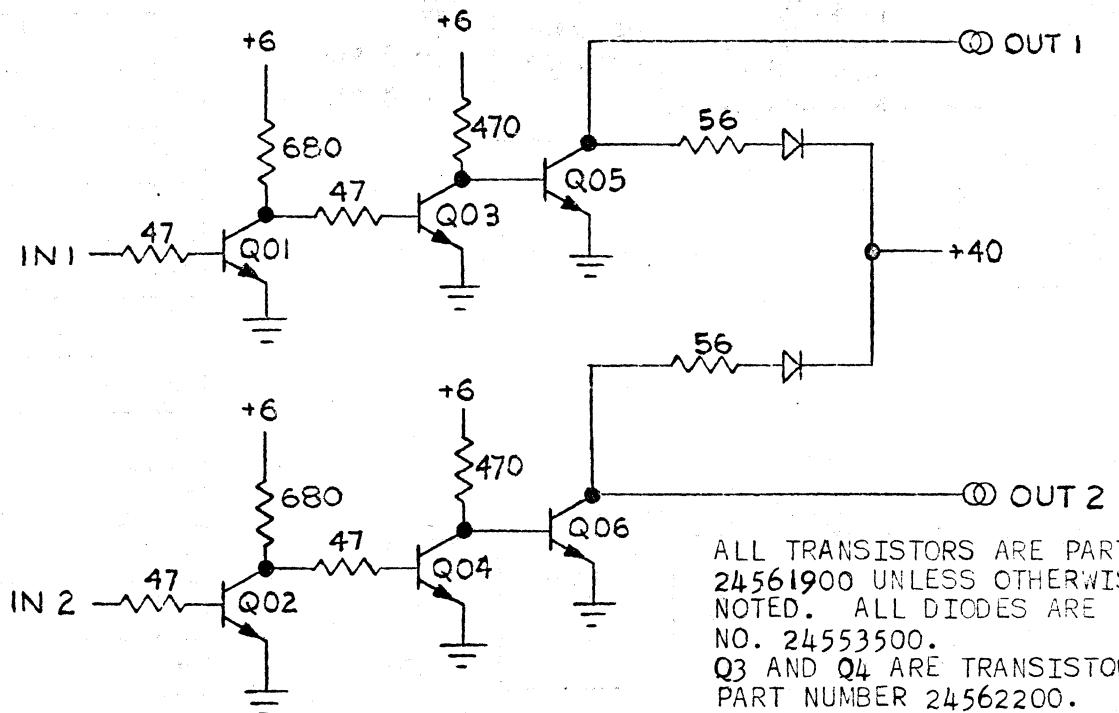


NOTE:

GROUND TEST POINTS 1 & 2
TO WRITE REV MARK.



	JACK	PIN	LG
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REV. MARK WRITER

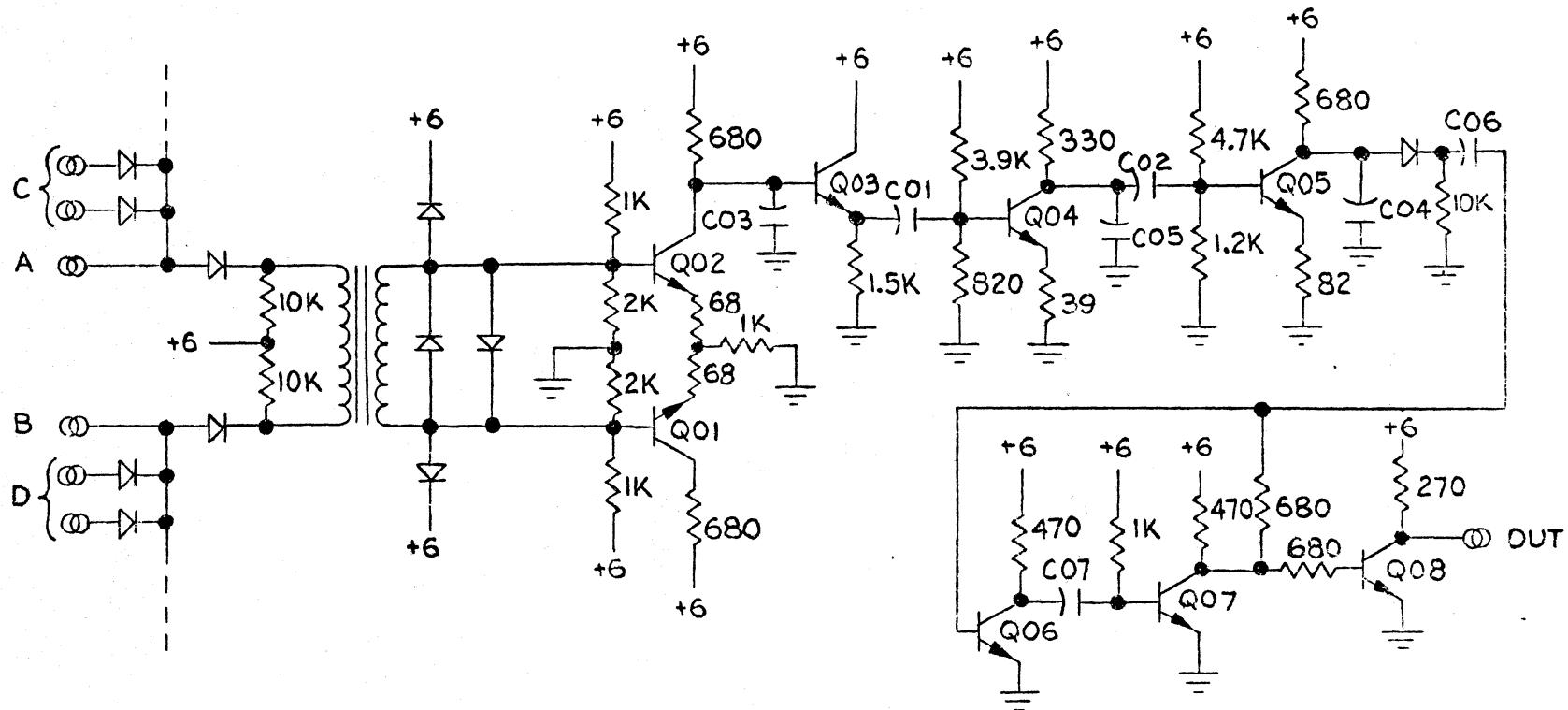
ALL TRANSISTORS ARE PART NO.
24561900 UNLESS OTHERWISE
NOTED. ALL DIODES ARE PART
NO. 24553500.
Q3 AND Q4 ARE TRANSISTORS
PART NUMBER 24562200.
Q5 AND Q6 ARE TRANSISTORS
PART NUMBER 18075100.

ELECTRICAL SCHEMATIC

L.S. 18117700

DG PAGE 3
REV.E

REV, MARK AMPLIFIER



ALL TRANSISTORS ARE PART NO. 24561900

ALL DIODES ARE PART NO. 24553500

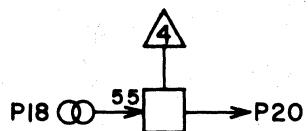
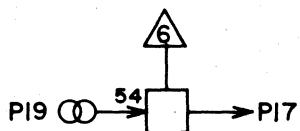
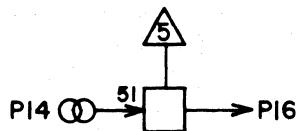
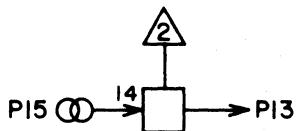
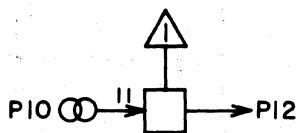
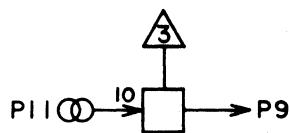
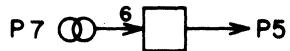
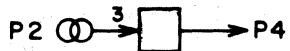
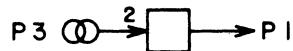
ELECTRICAL SCHEMATIC

LS 18117900
ASSY

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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

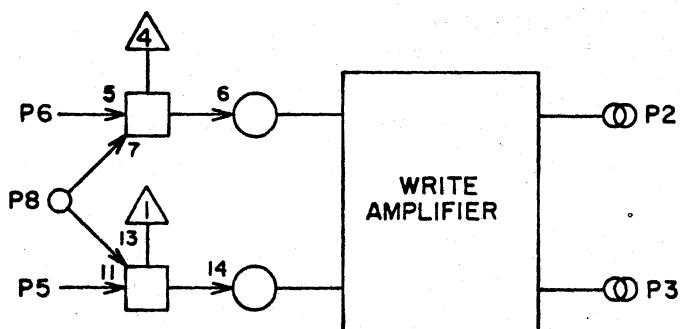
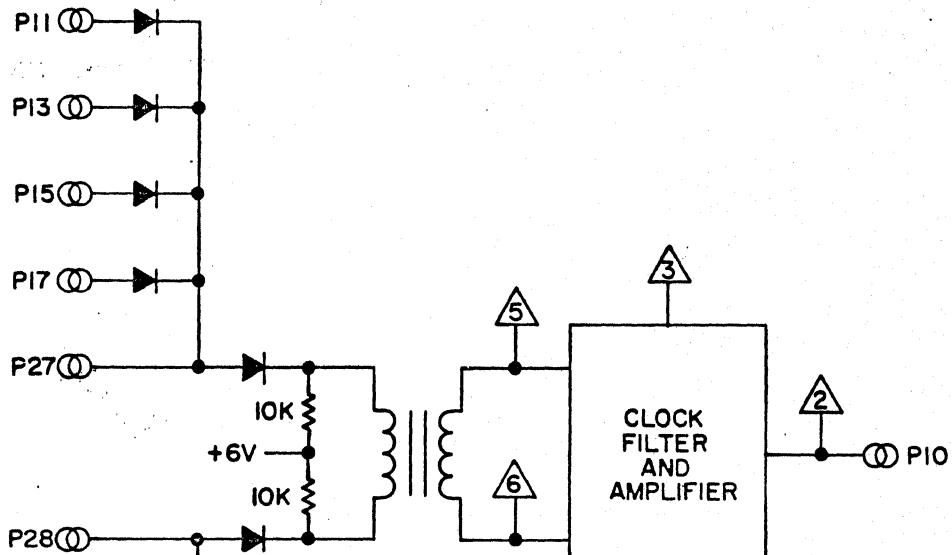
60042700 Rev. K

LS 18762300
ASSY REV B

DJ

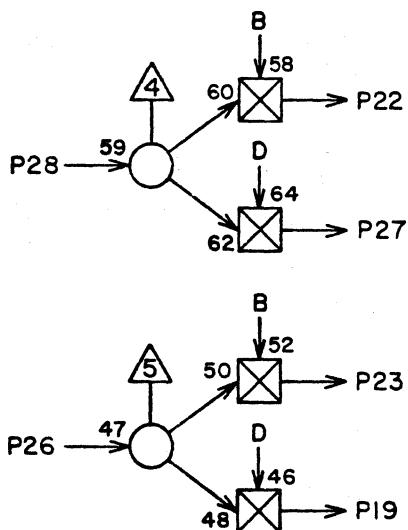
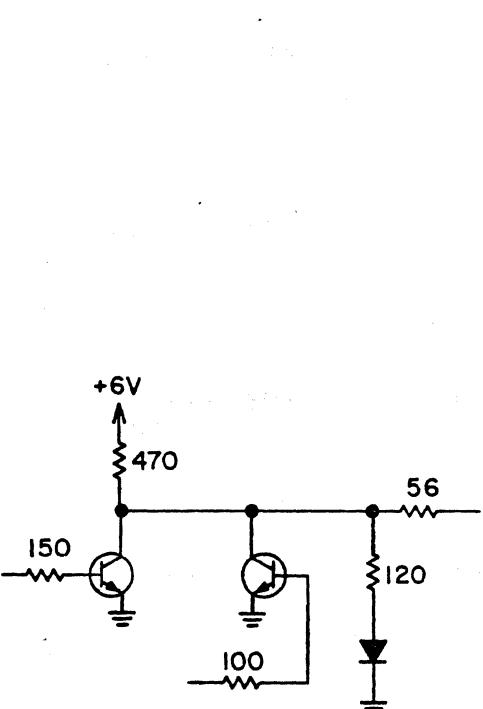
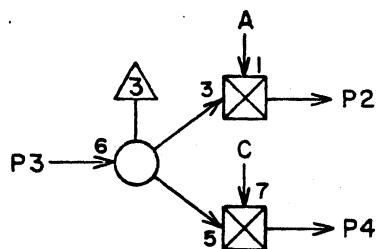
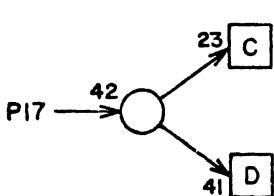
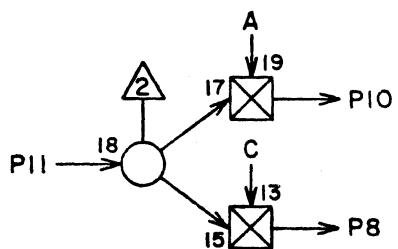
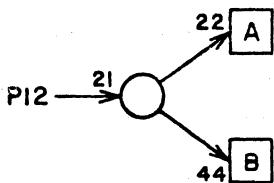
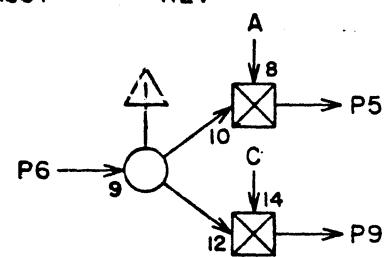
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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. Y

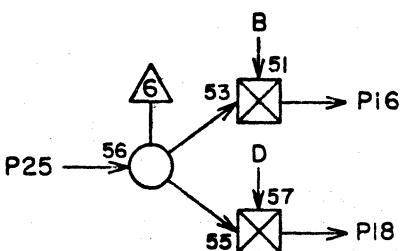
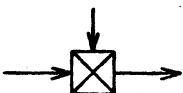


LS 18453400 B
ASSY REV

DK



CIRCUIT FOR

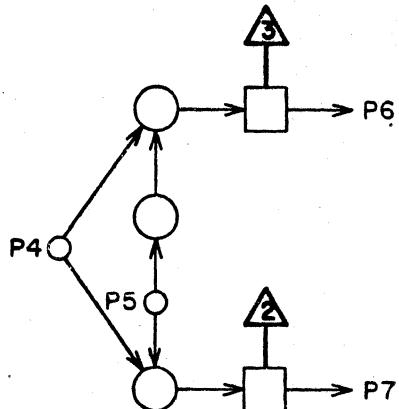
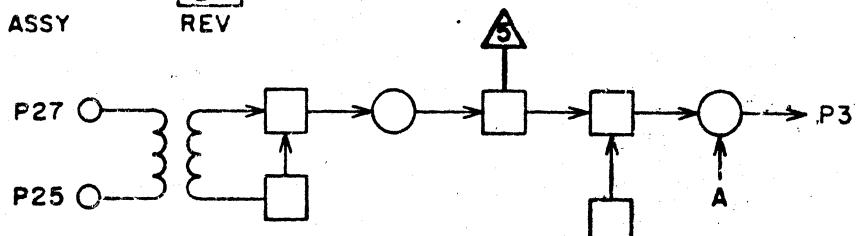


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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. Y

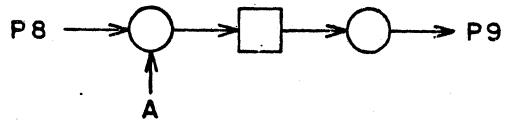
LS 18453600 B
ASSY REV

SPECIAL
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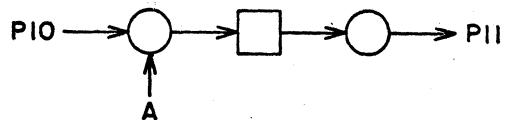


P1 → -6V

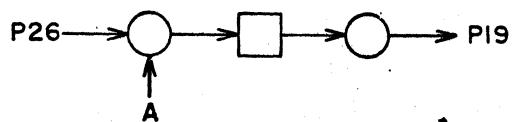
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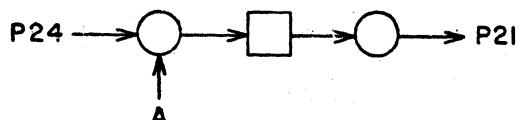
P2 → +6V



P29 → \ominus



P17 → \ominus



P13 → A

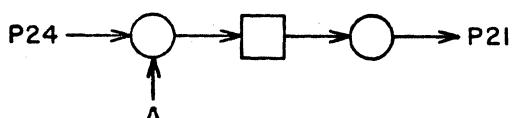
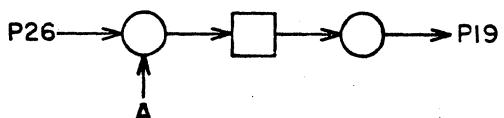
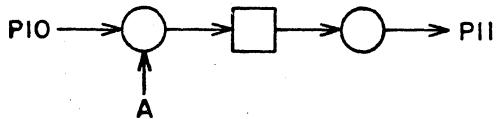
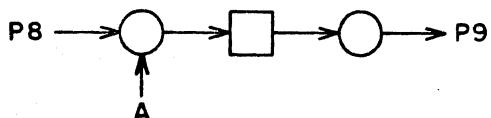
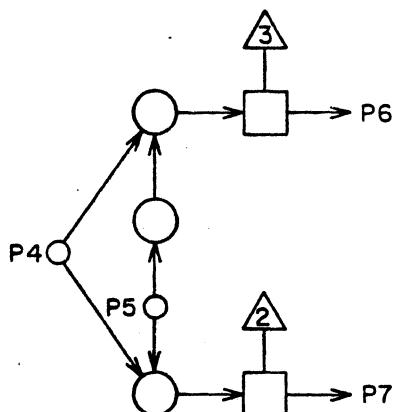
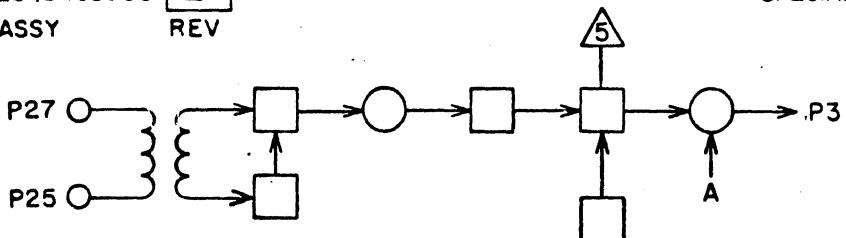
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FOR CIRCUIT EXPLANATION SEE ELECTRICAL
SCHEMATIC, DWG NO. 18453900

JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. Y

LS 18453800 **B**
ASSY REV

SPECIAL DM



P1 → -6V

P20 → +40V

P2 → +6V

P29 →

P17 →

P13 → A

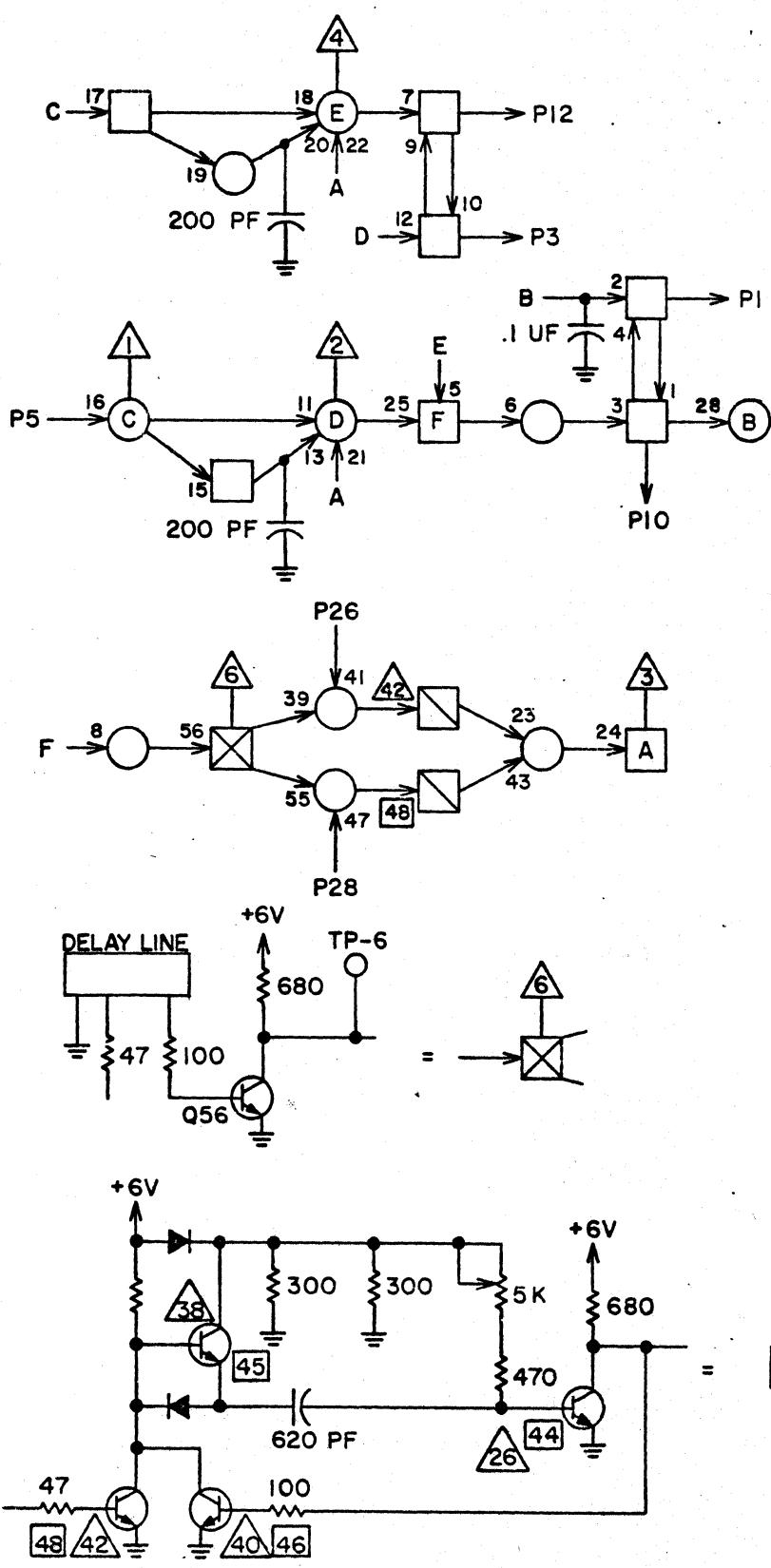
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FOR CIRCUIT EXPLANATION SEE ELECTRICAL
SCHEMATIC, DWG NO. 18454000

JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. Y

LS 18438500 B
ASSY REV

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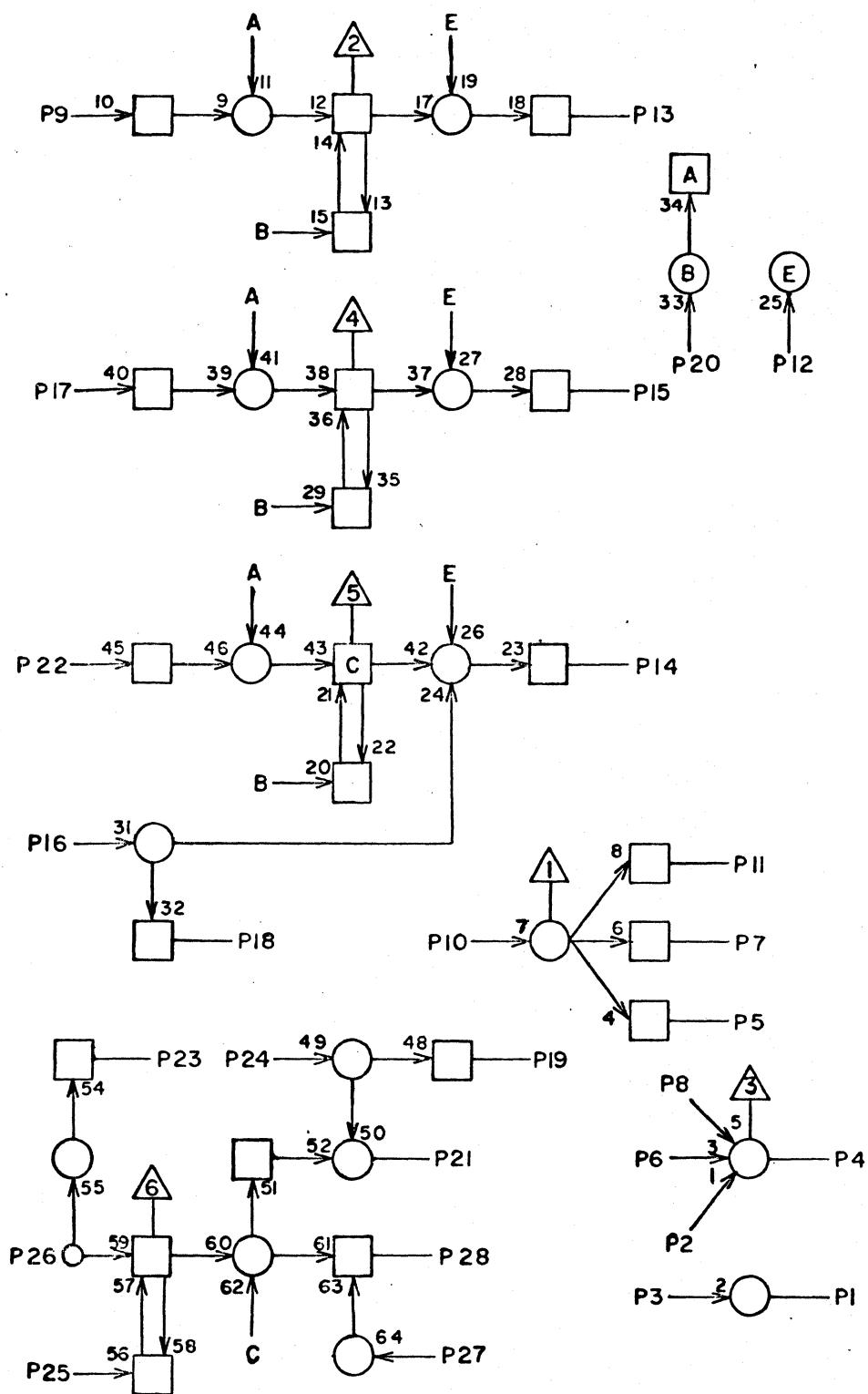
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SEE CIRCUIT SPECIFICATION
.11827600
60042700 Rev. Y

NOTE

- I. INDICATES ZONE (1)
 INDICATES ZONE (2)

LS18745400 B
ASSY REV

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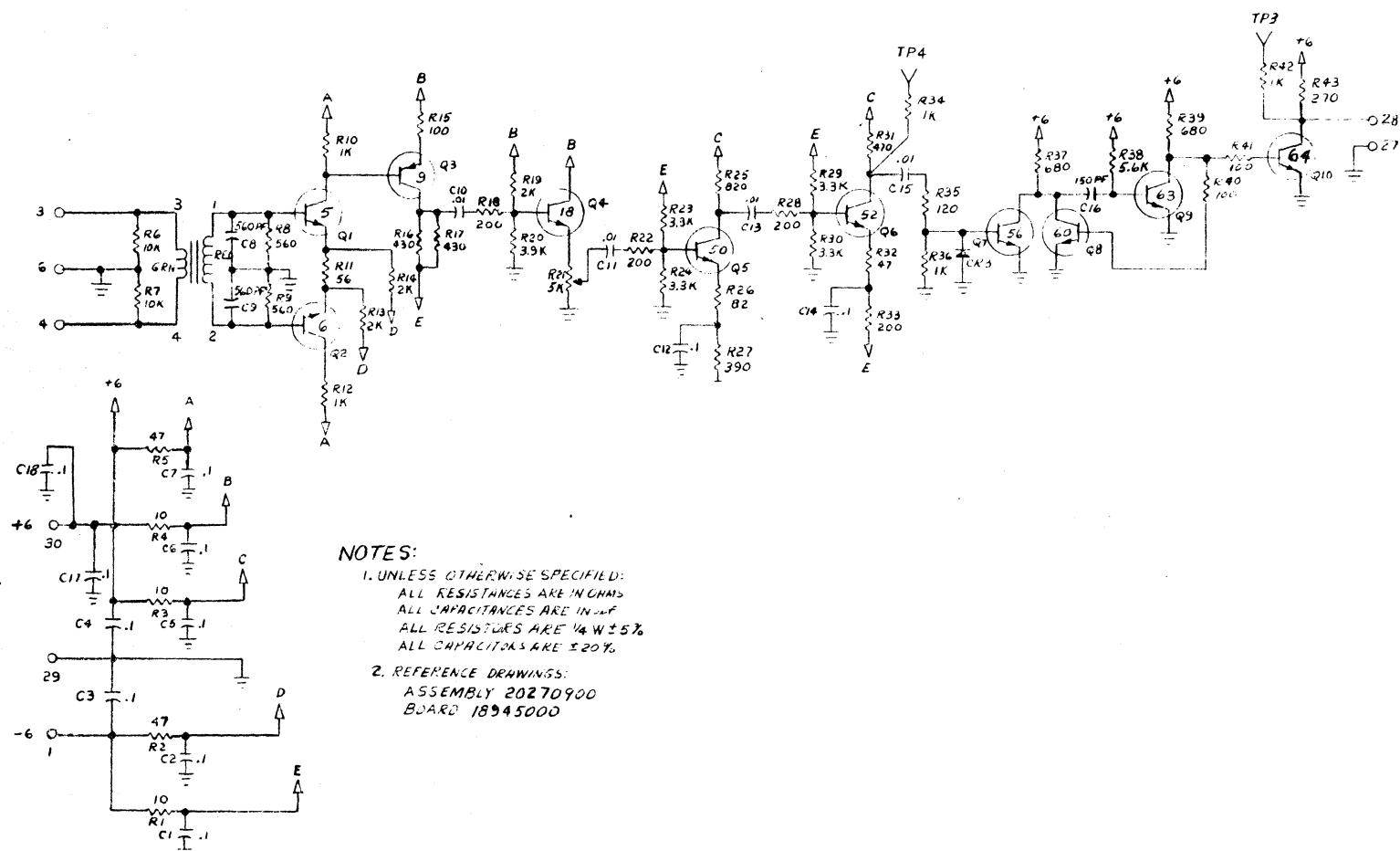


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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

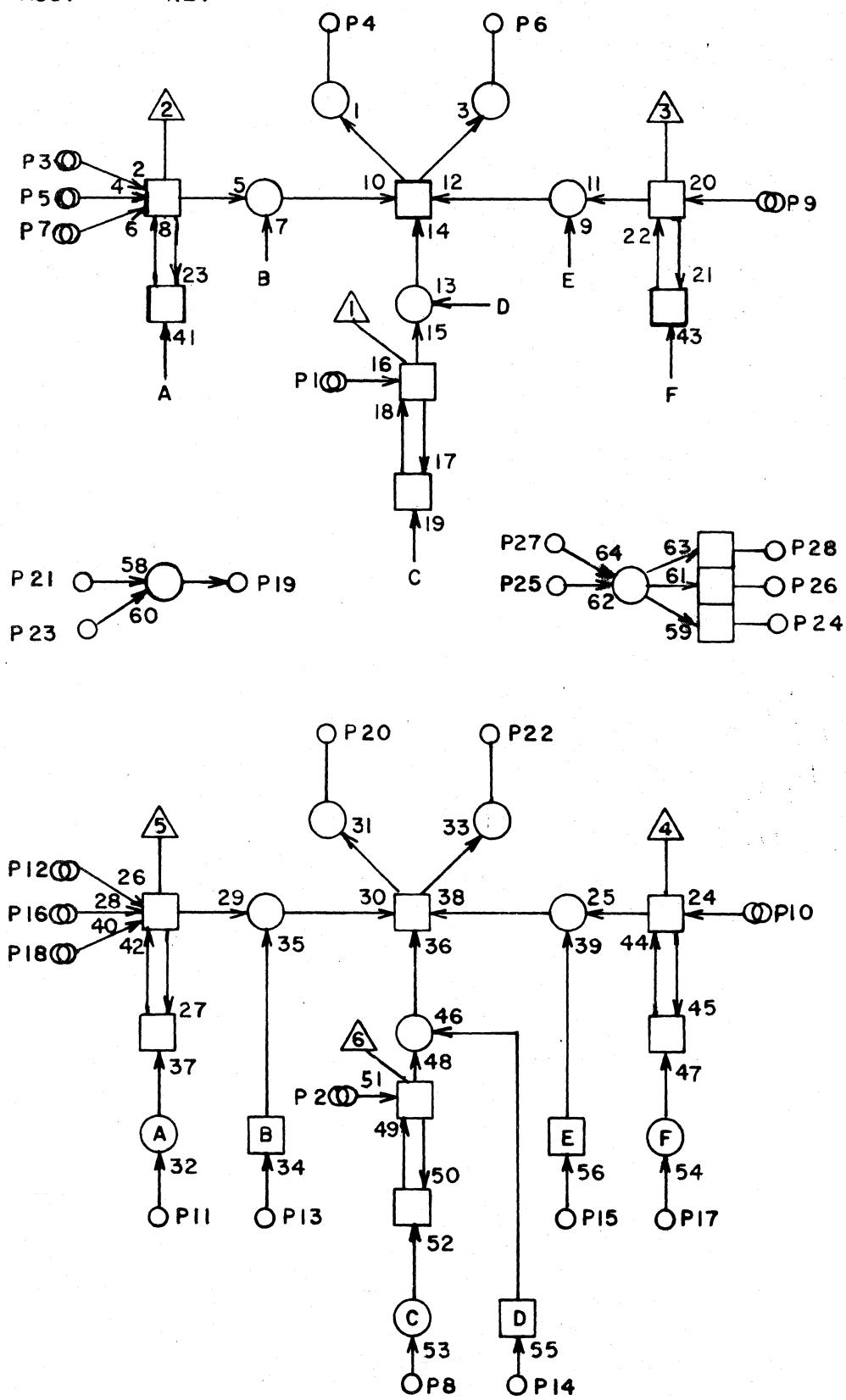
60042700 Rev. Z

DQ
Electrical Schematic



LS 23235000 C
ASSY REV

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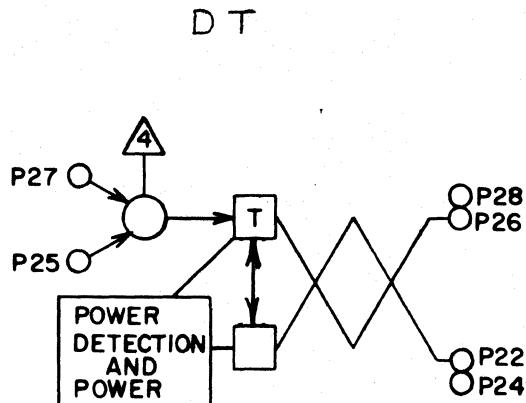
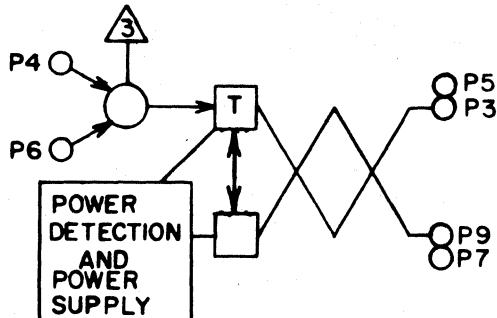
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SEE CIRCUIT SPECIFICATION
52302100

60042700 Rev AB



LS 52518200 F
ASSY REV

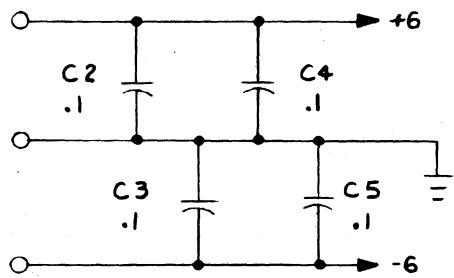
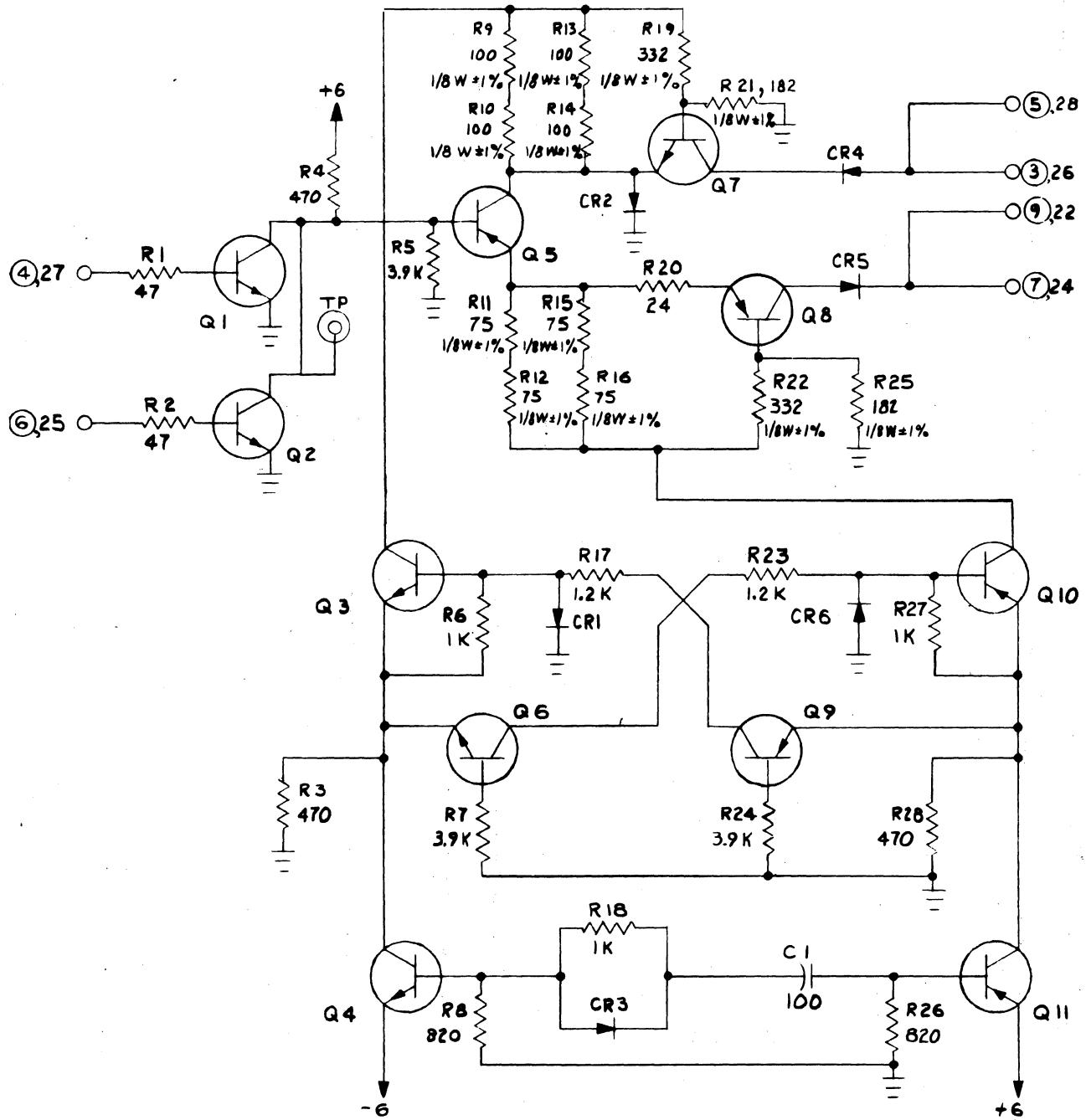


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60042700 Rev AB

JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

DT Electrical Schematic



60042700 Rev AB

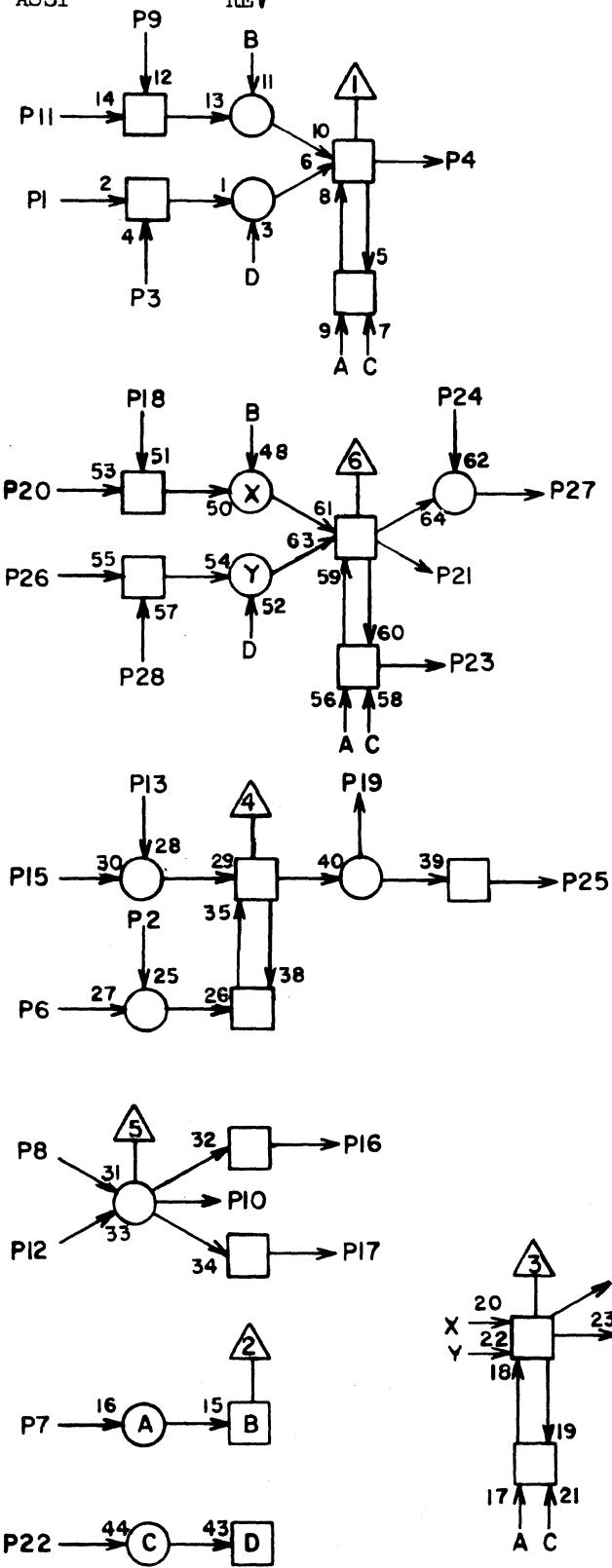


LS 52631200

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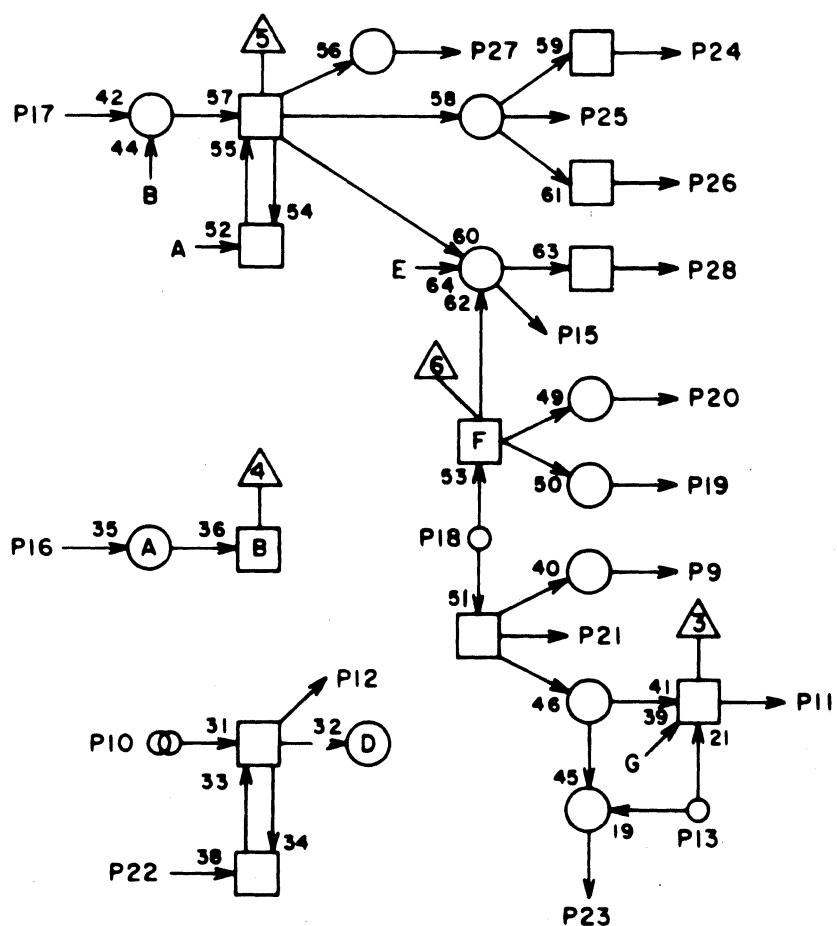
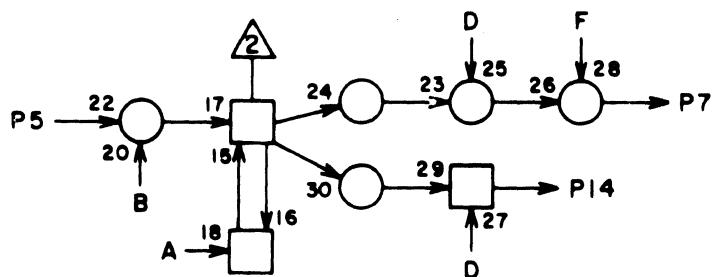
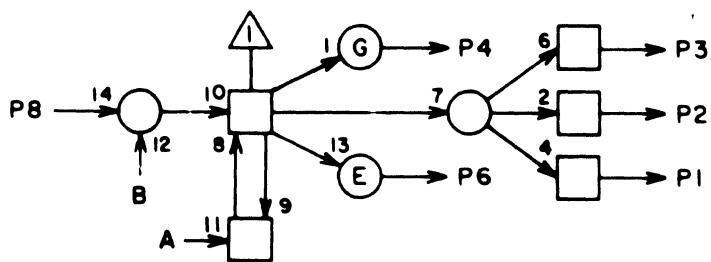
60042700 Rev AB

SEE CIRCUIT SPECIFICATION 11827600

LS 18058100
ASSY

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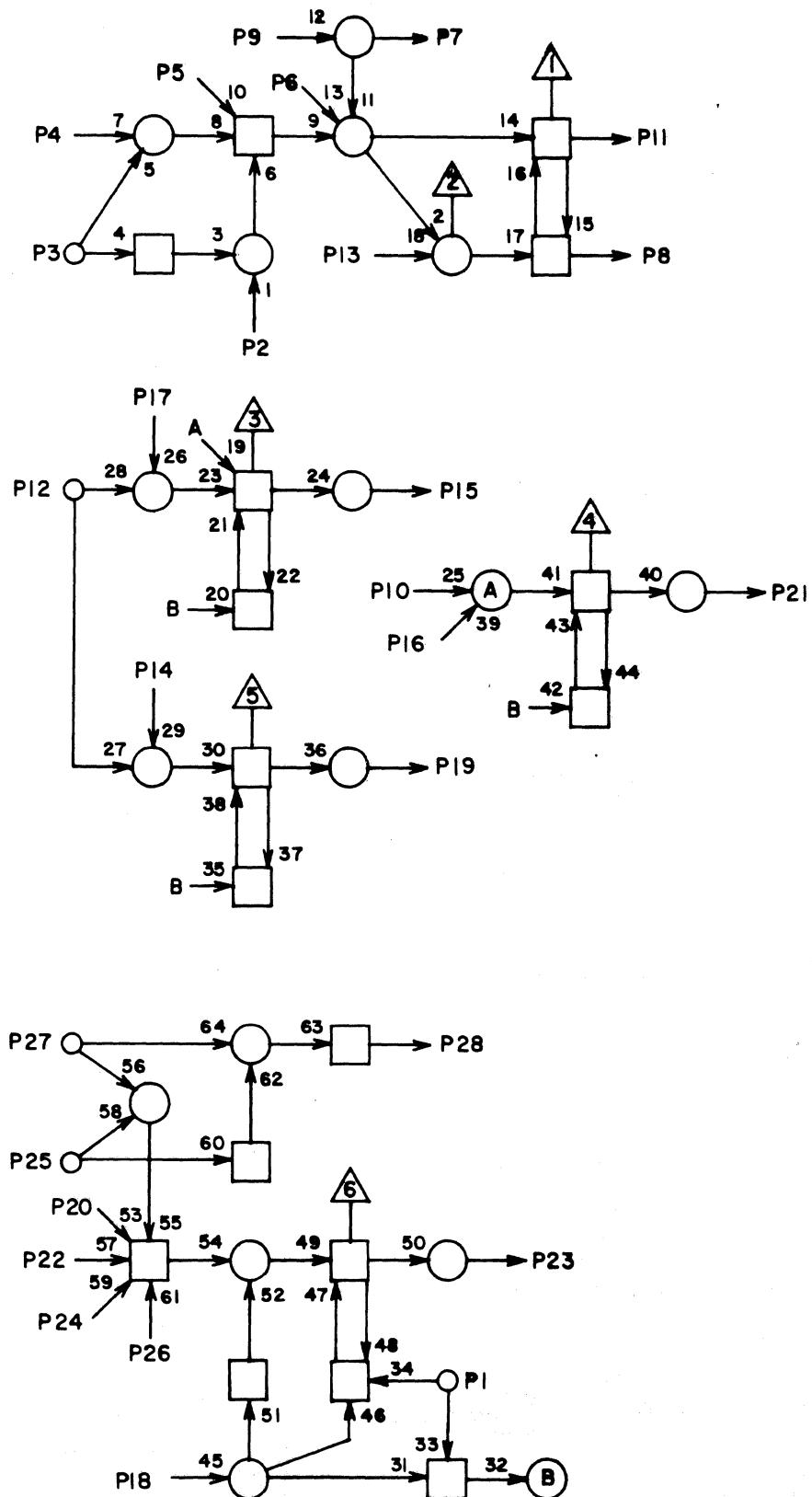
JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. P



LS 17967600
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CIRCUIT SPECIFICATION
11827600

60042700 Rev. K

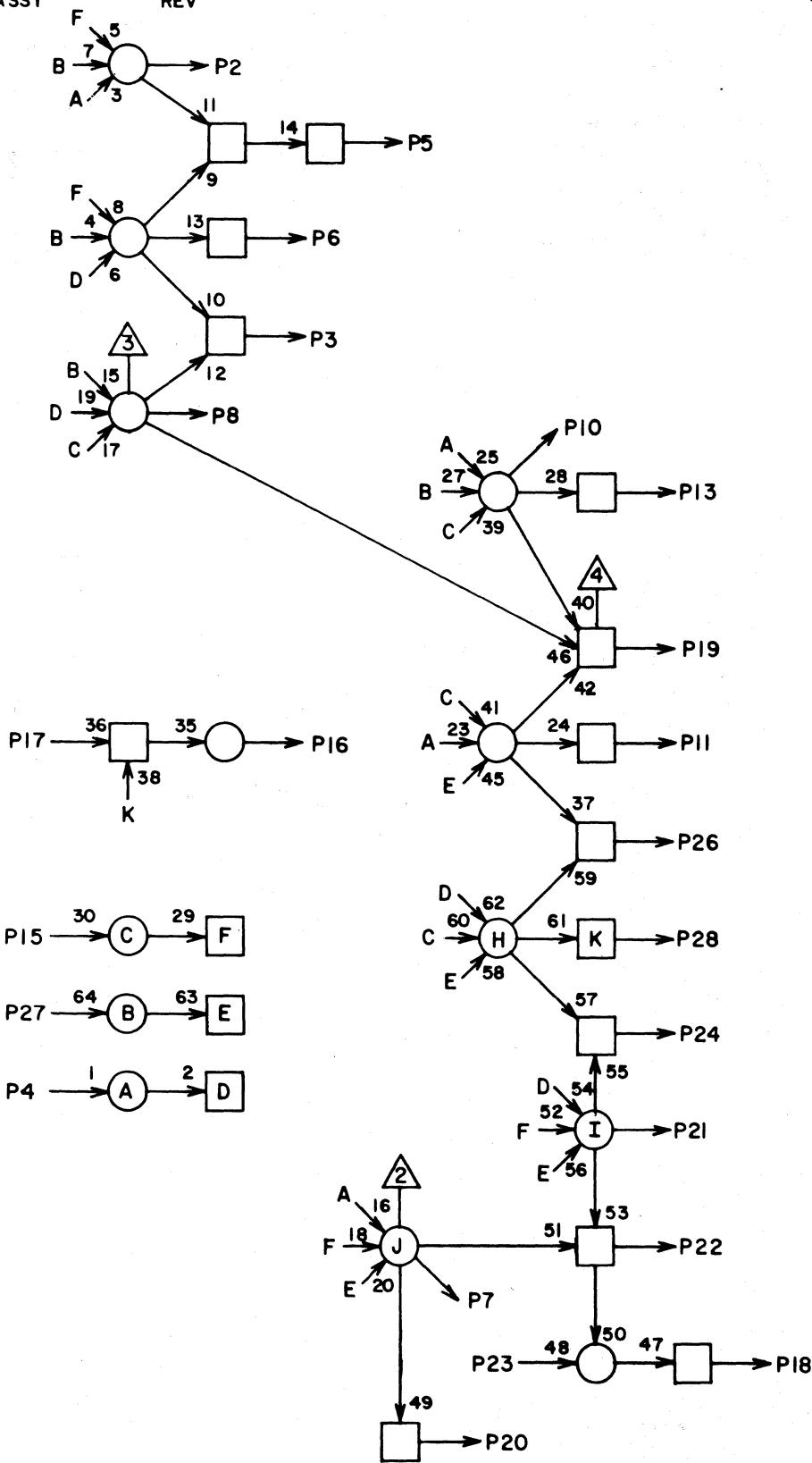
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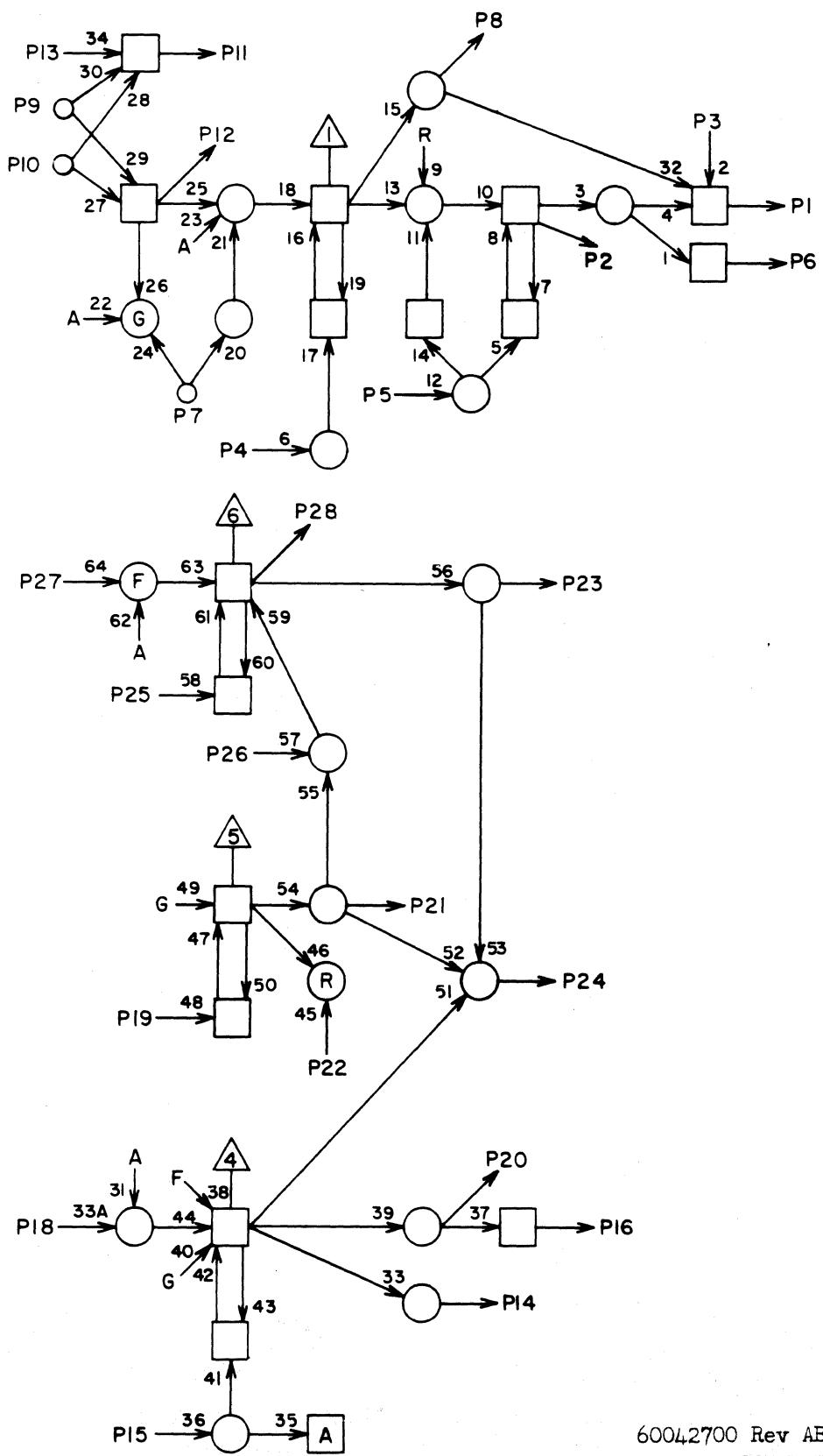
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CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

LS 17968000 B
ASSY REV

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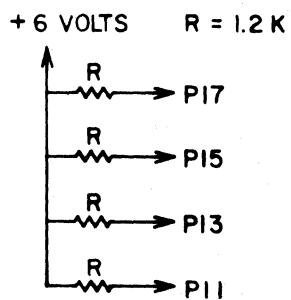
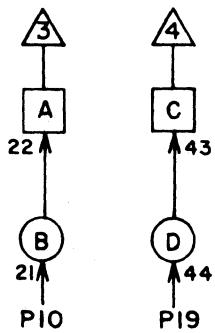
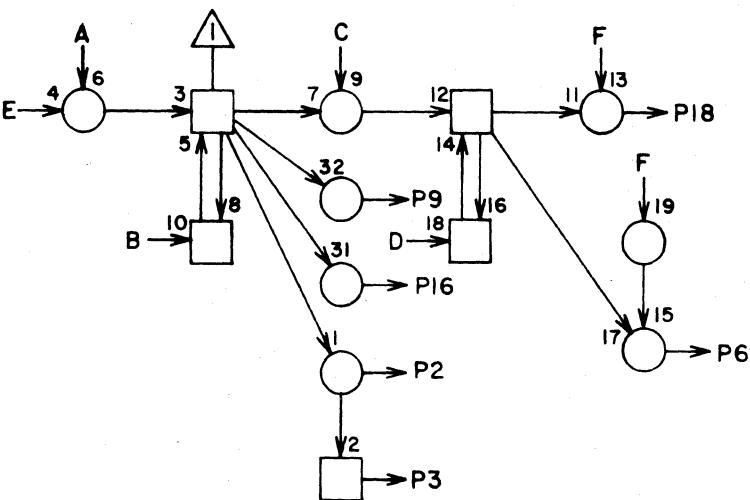
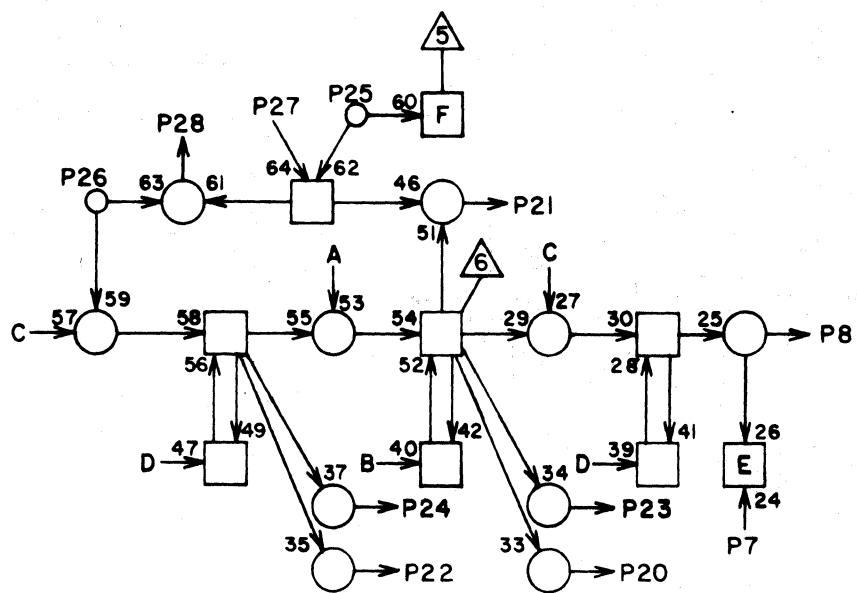
60042700 Rev AB
CIRCUIT SPECIFICATION 11827600

JACK PIN LG

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JACK PIN LG

CIRCUIT SPECIFICATION

11827600

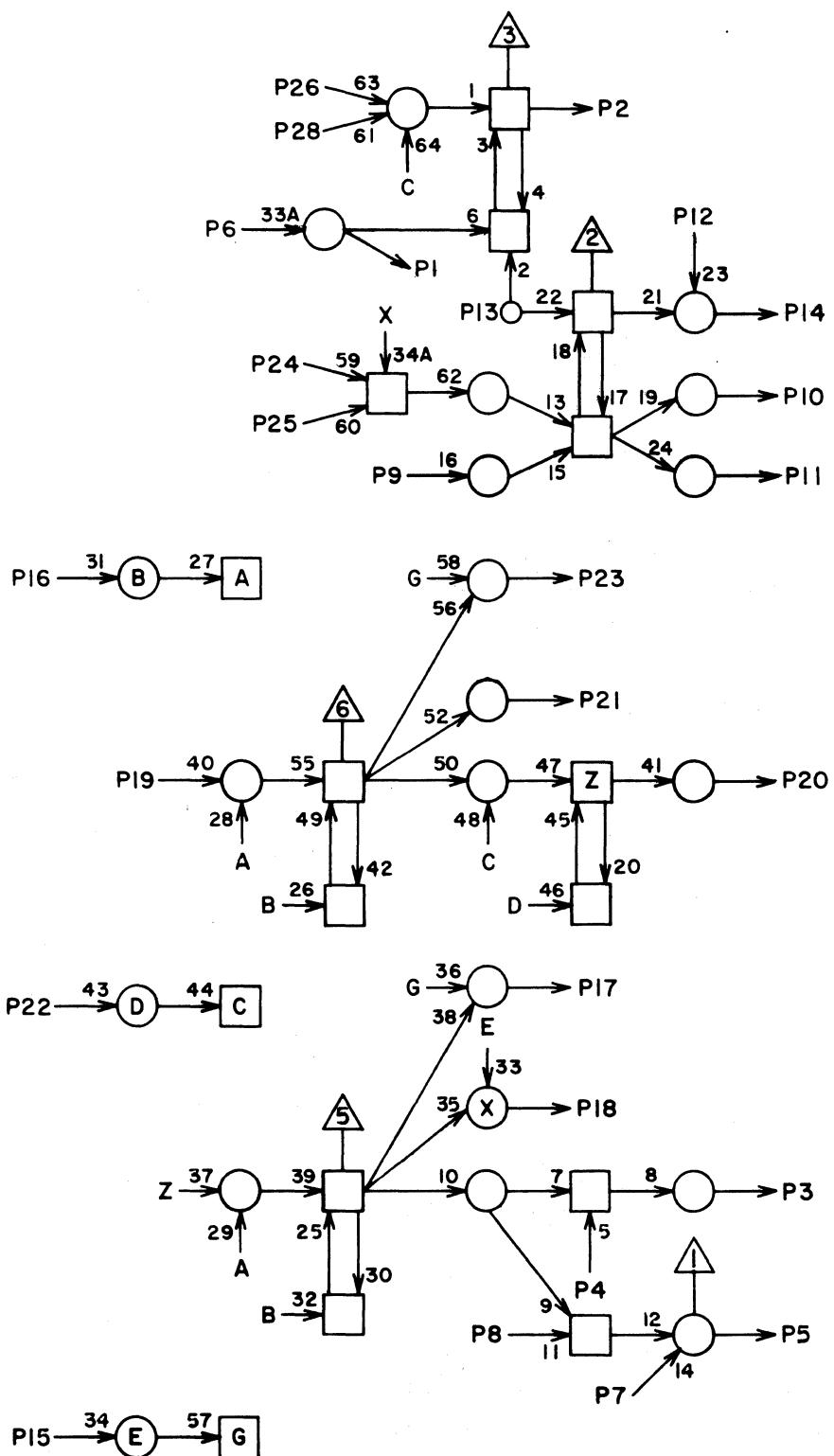
60042700 Rev. K

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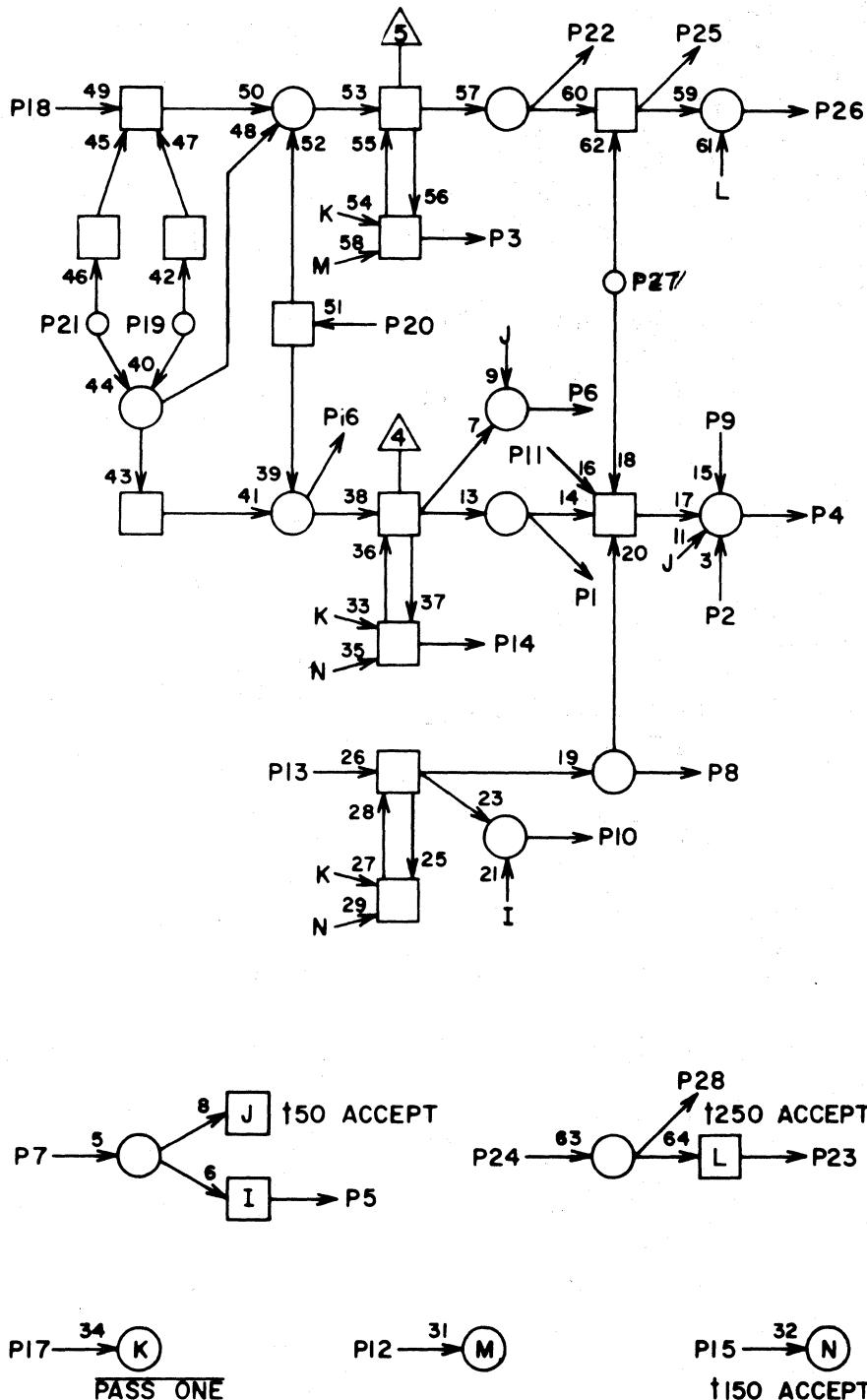
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JACK PIN LG
CIRCUIT SPECIFICATION
60042700 Rev AB 11827600

LS 17968600
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JACK PIN LG

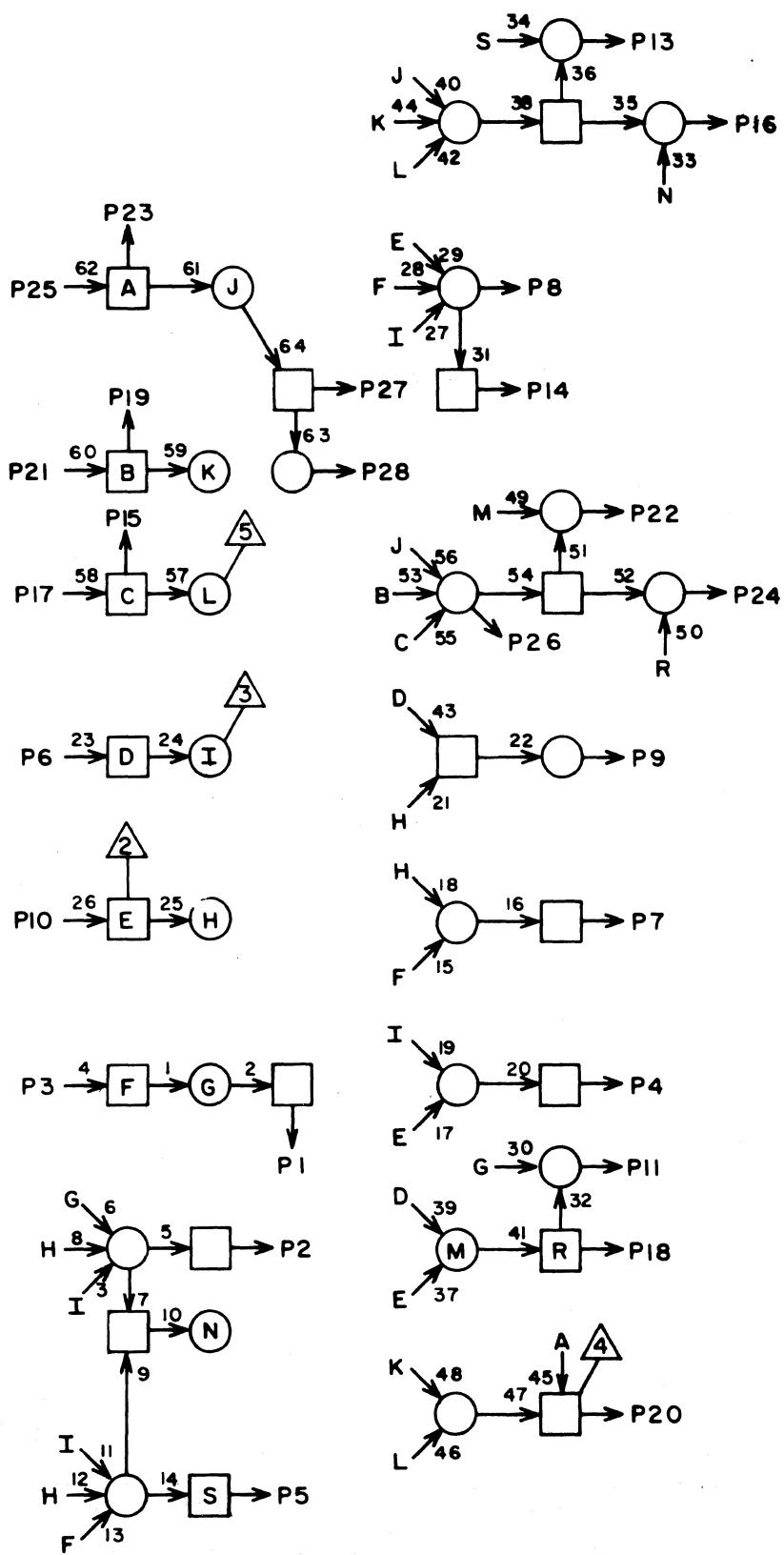
CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

LS 17968800
ASSY

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REV

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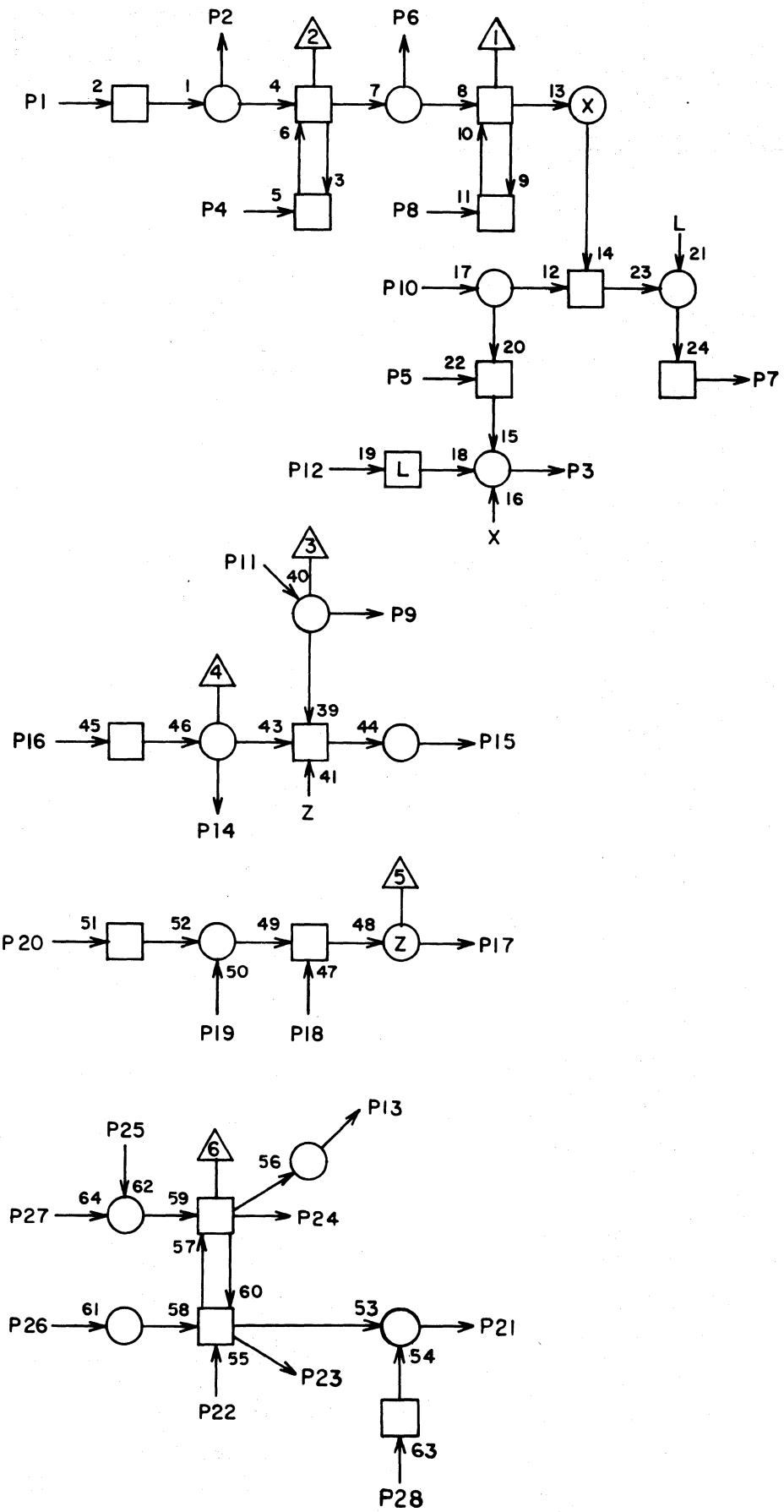
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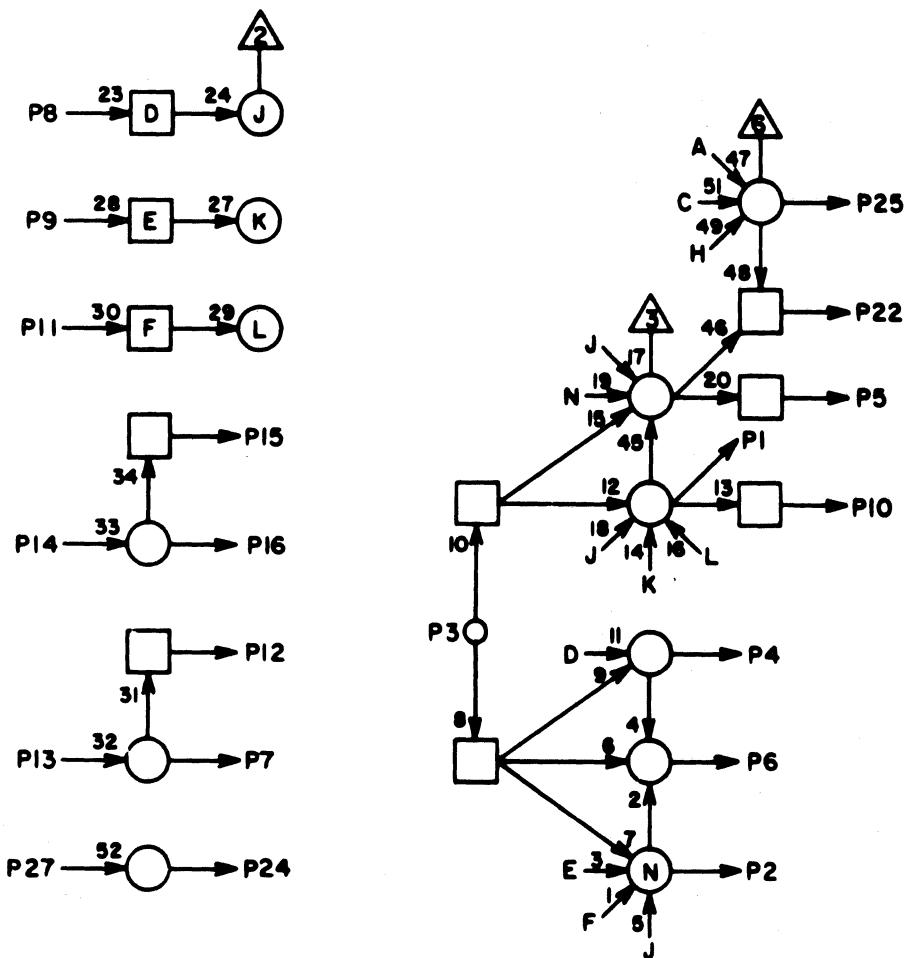
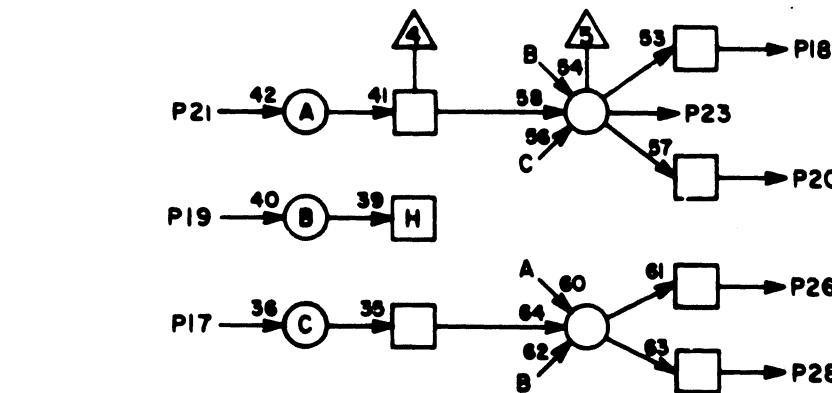
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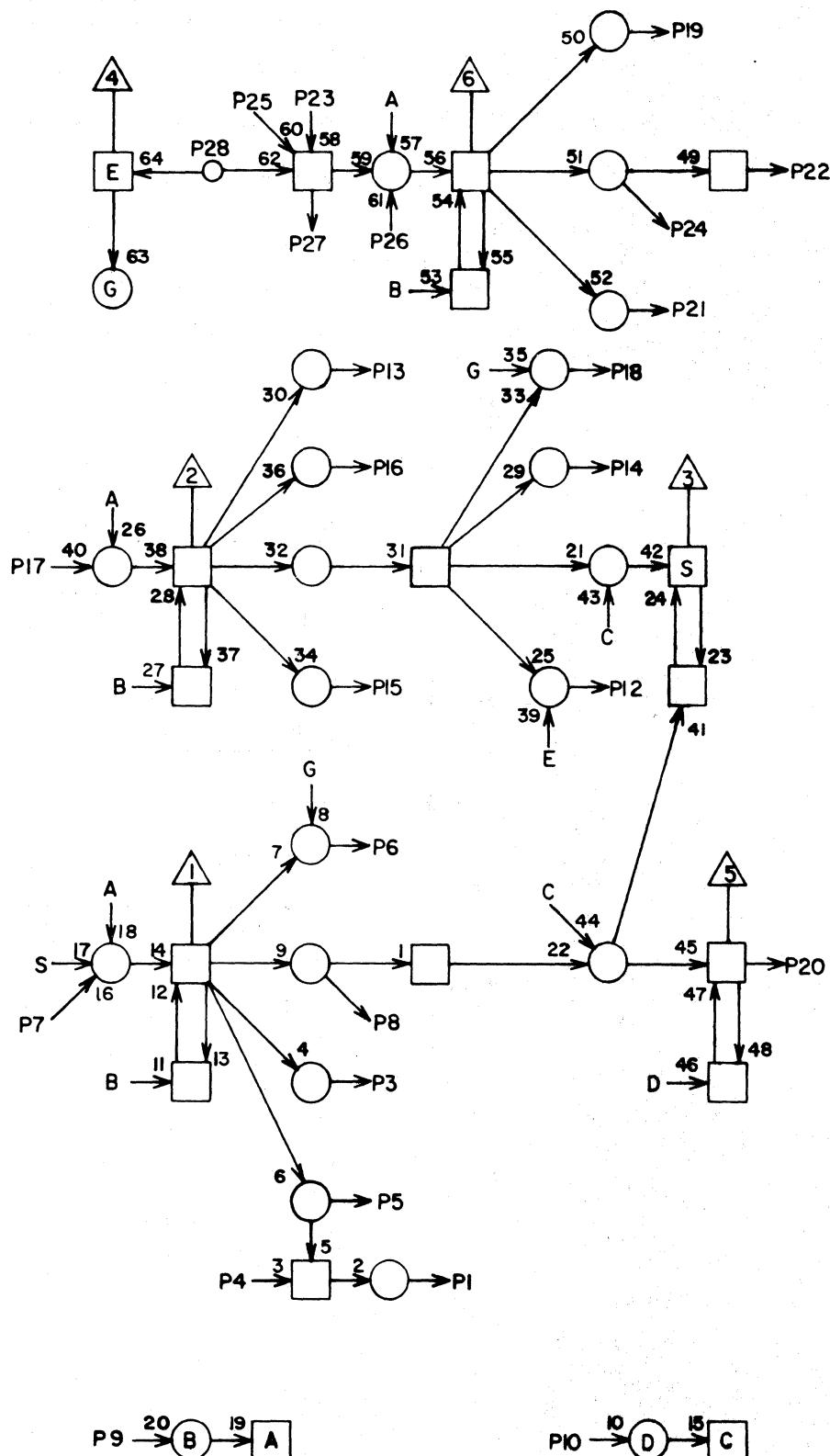
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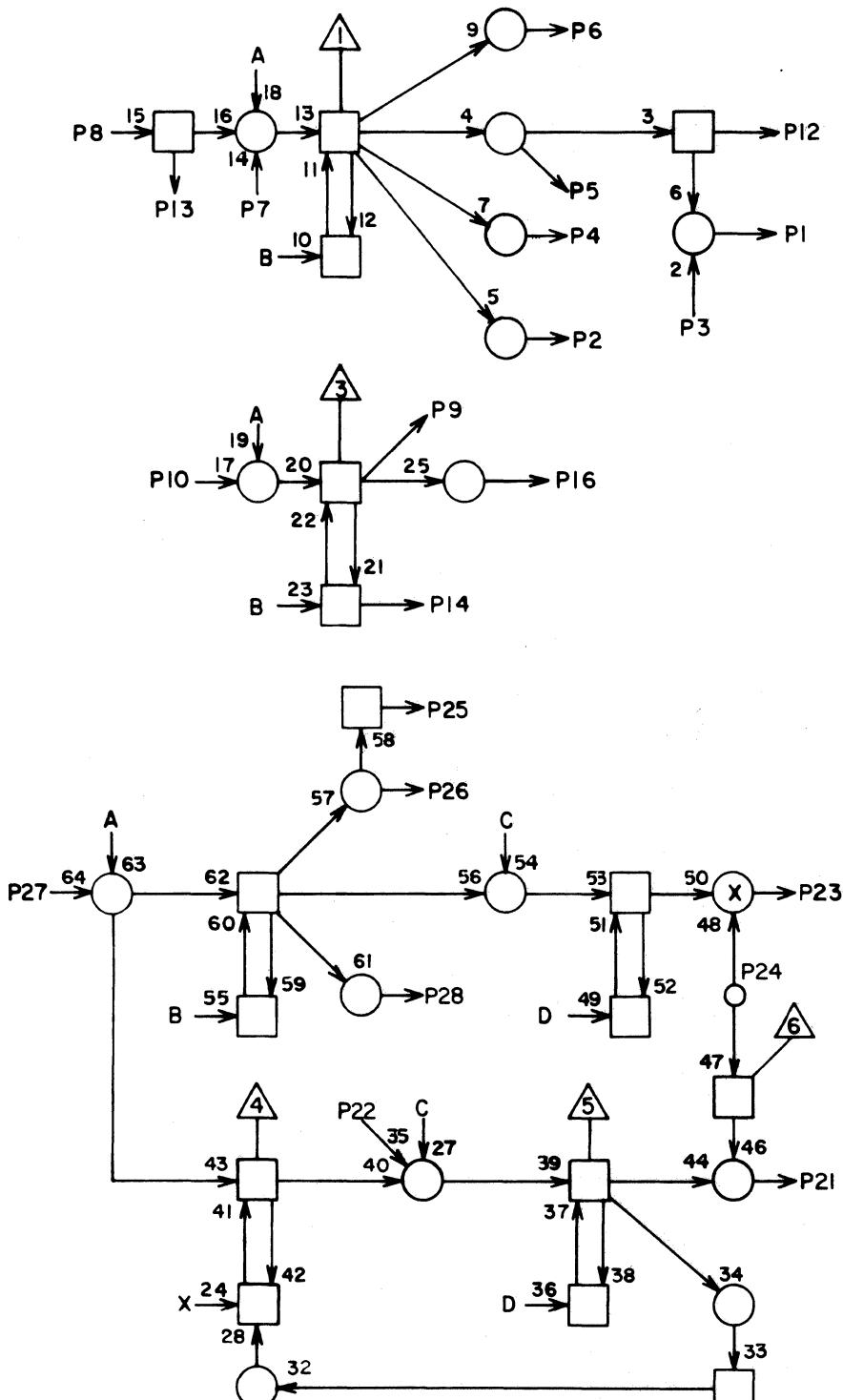
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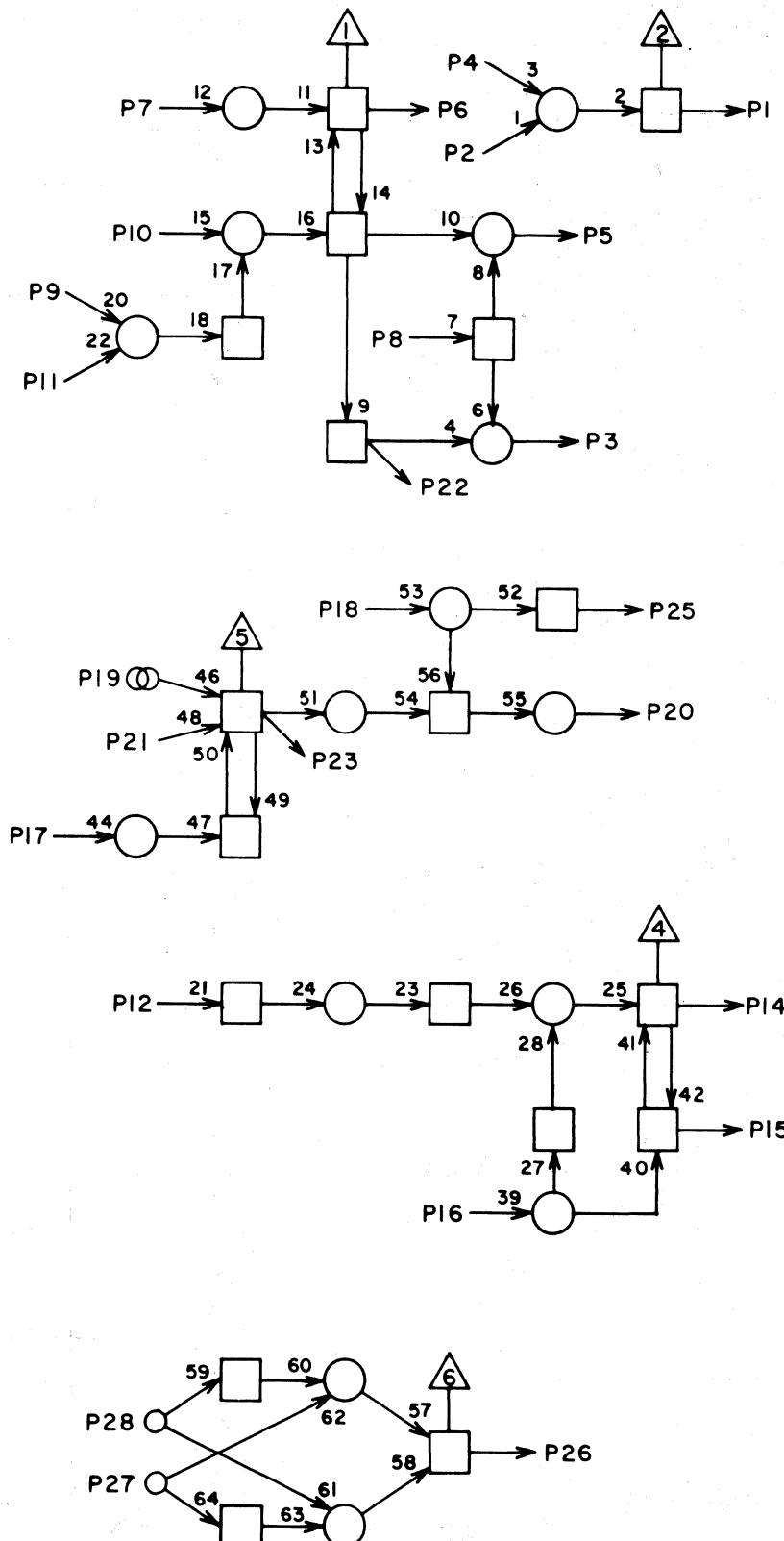
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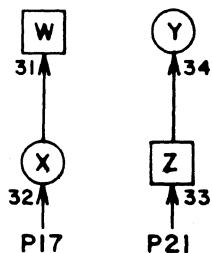
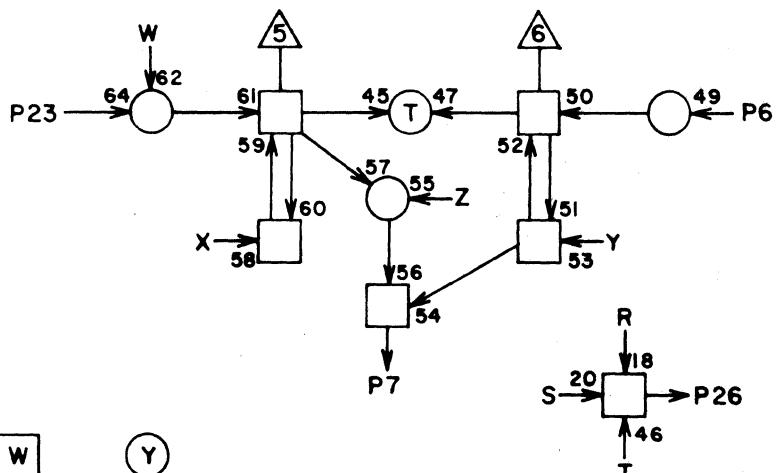
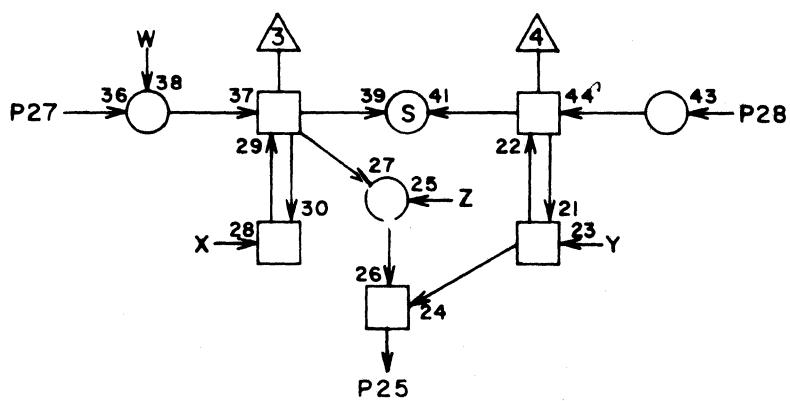
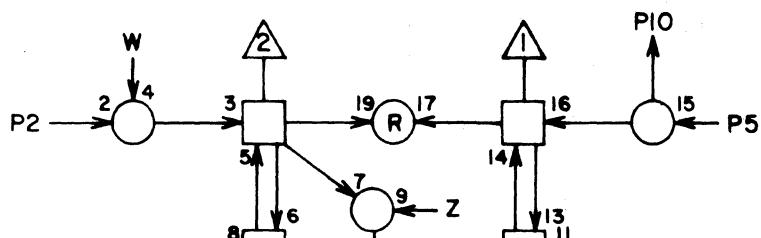
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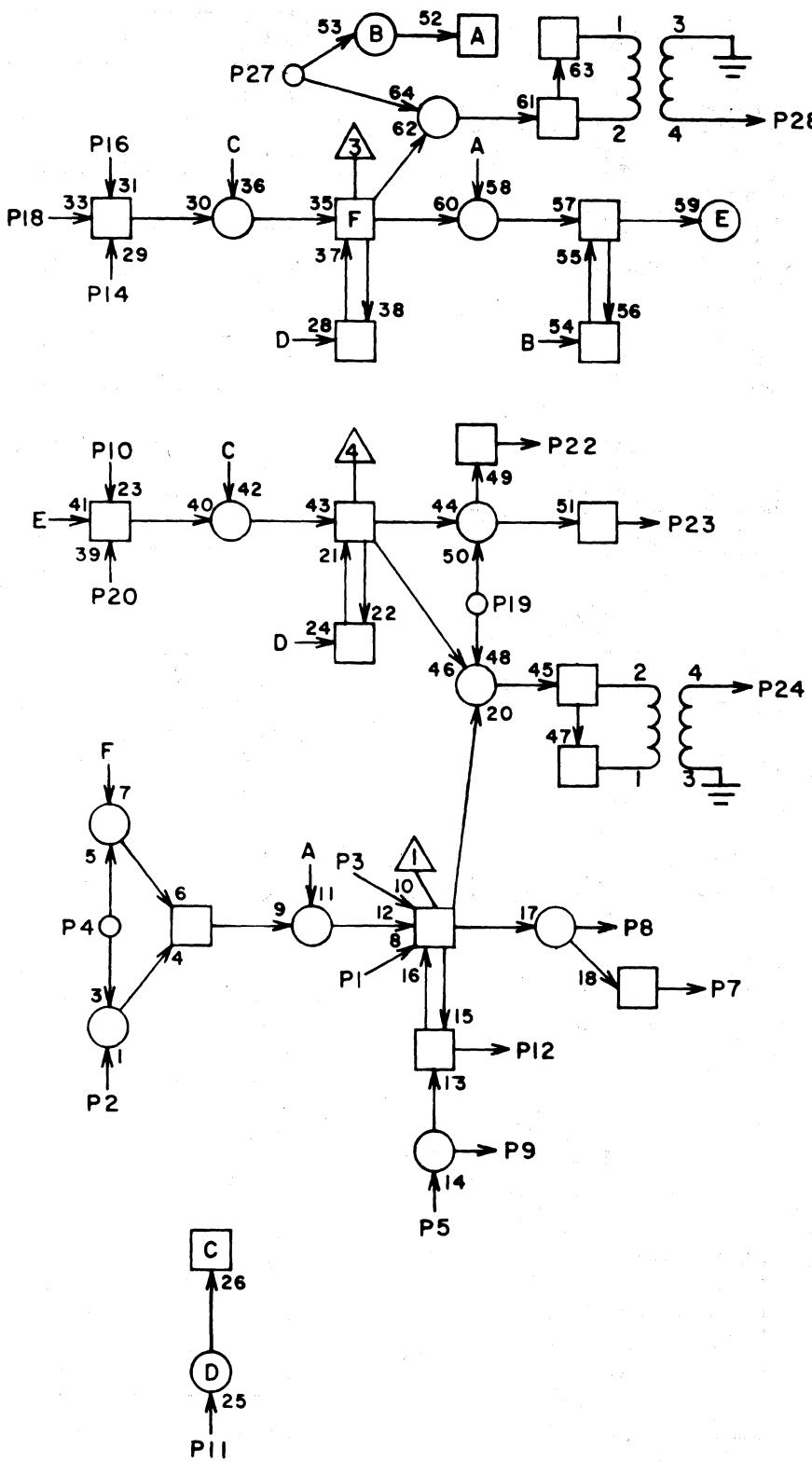
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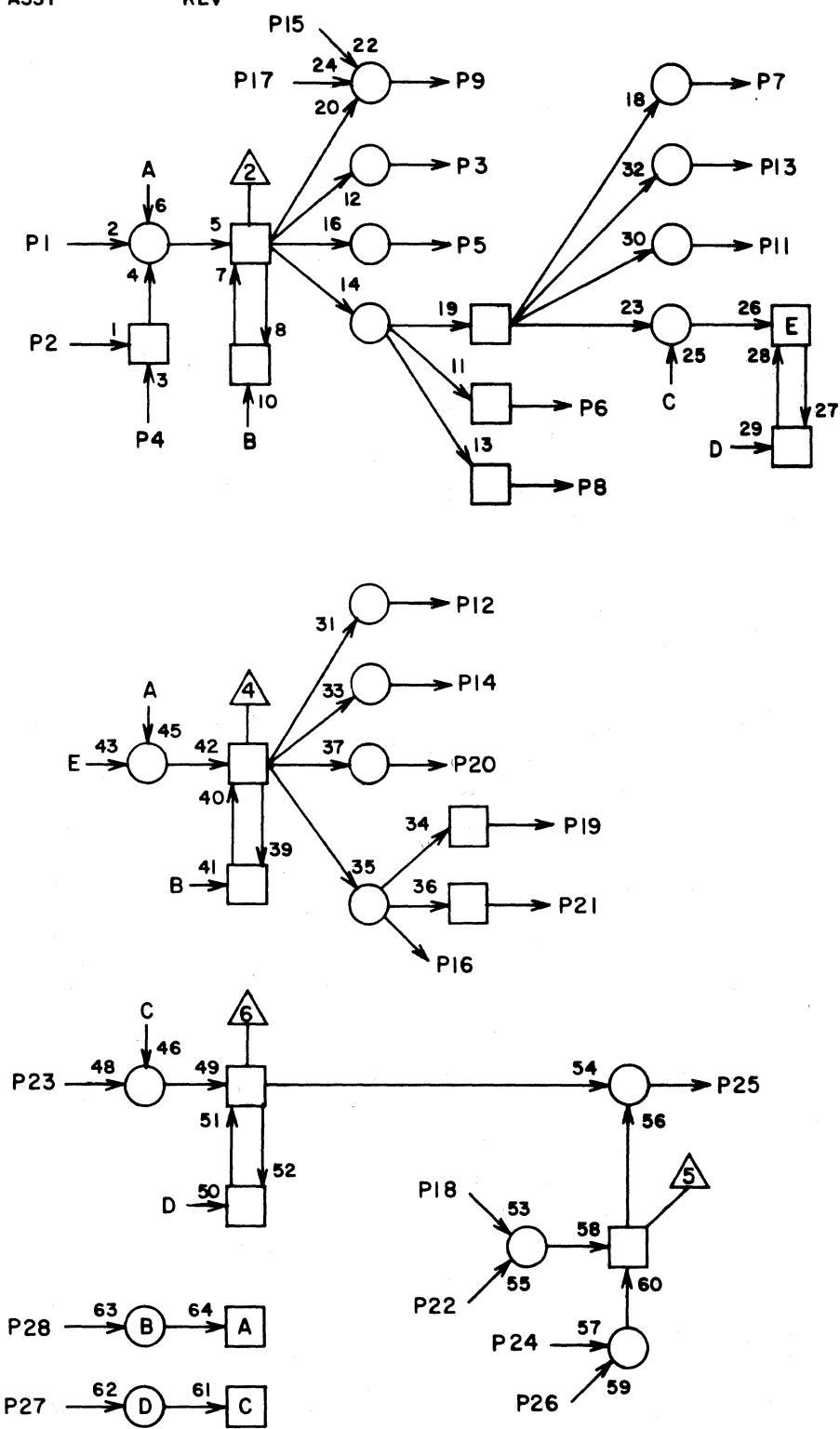
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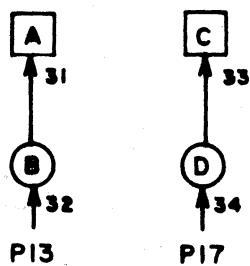
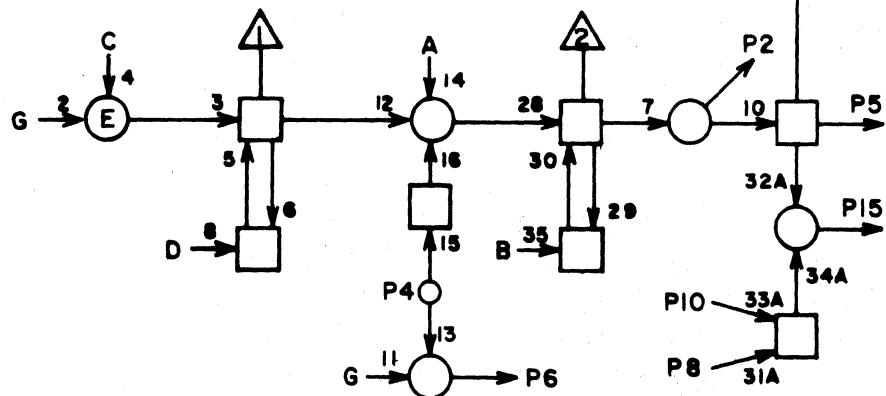
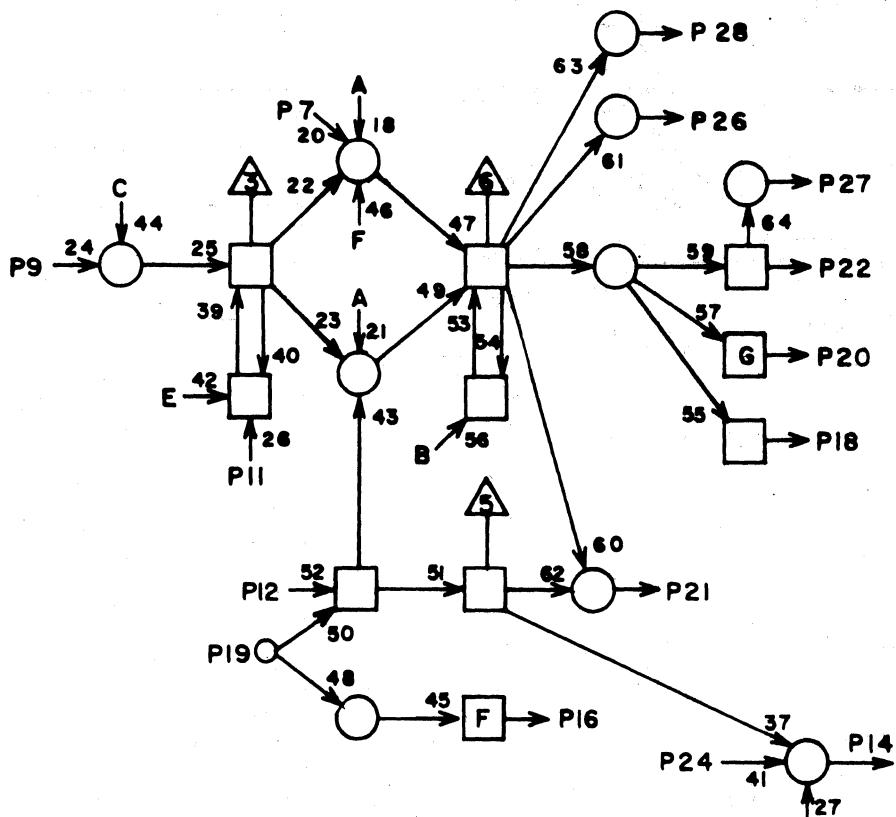
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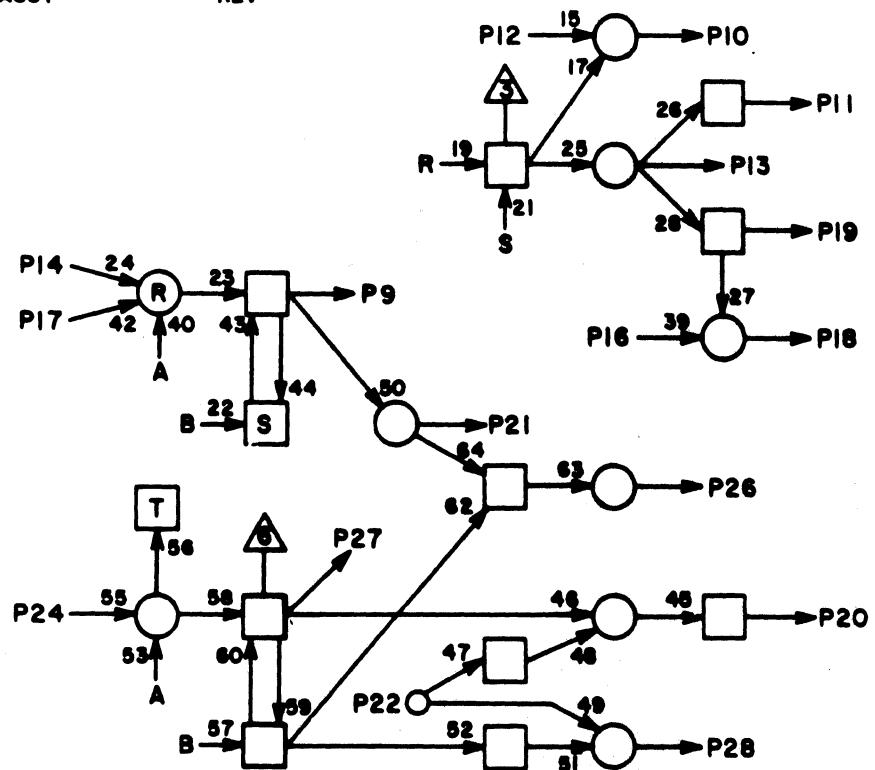
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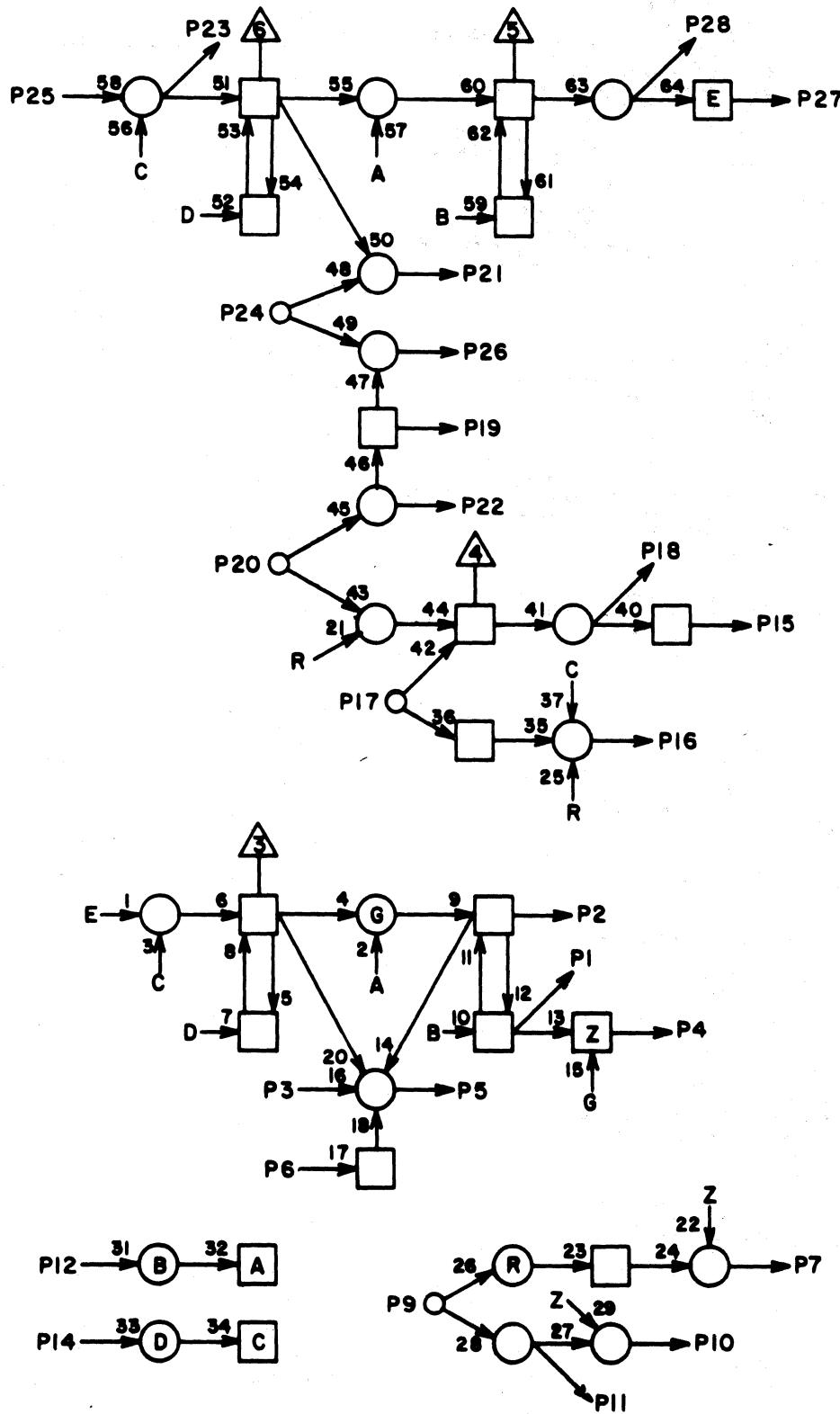
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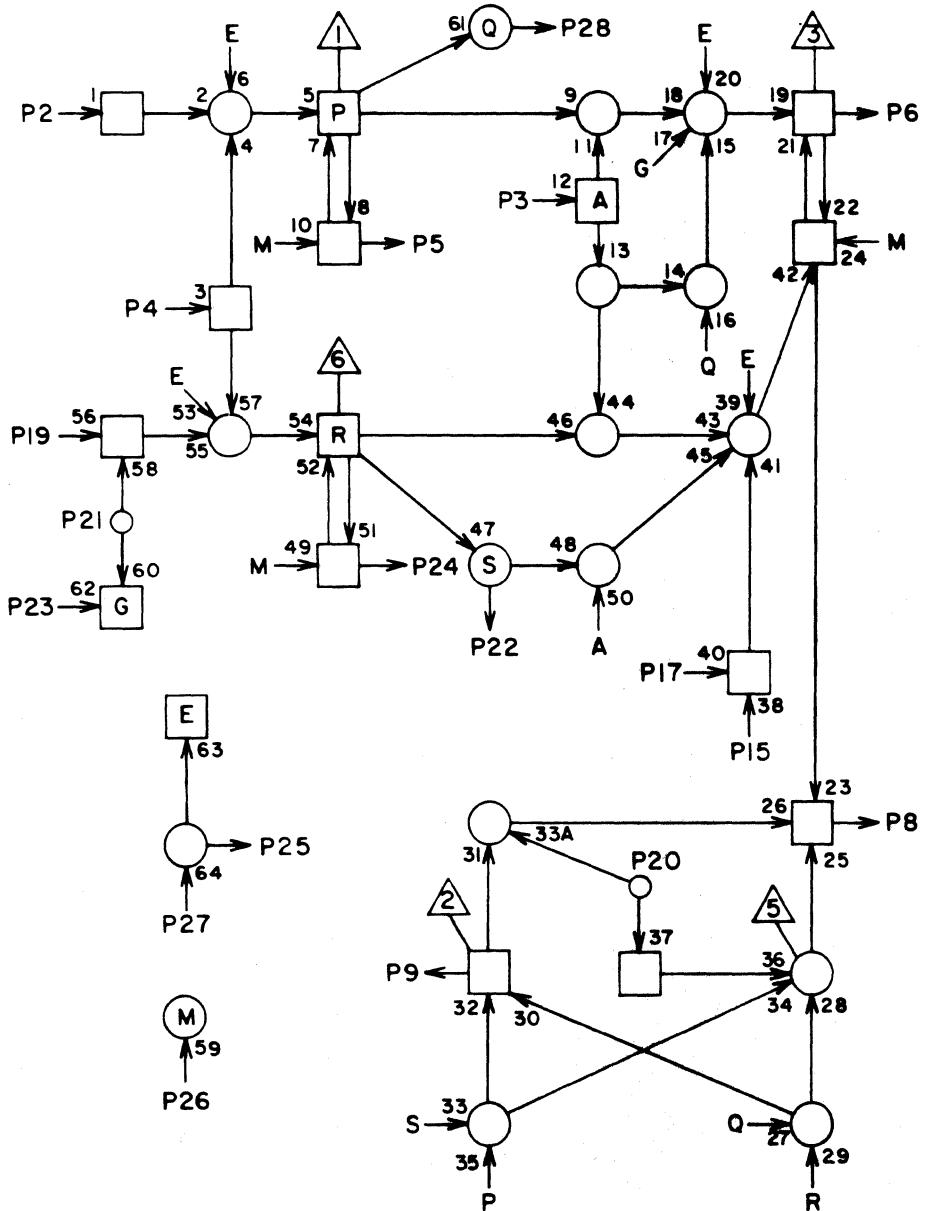
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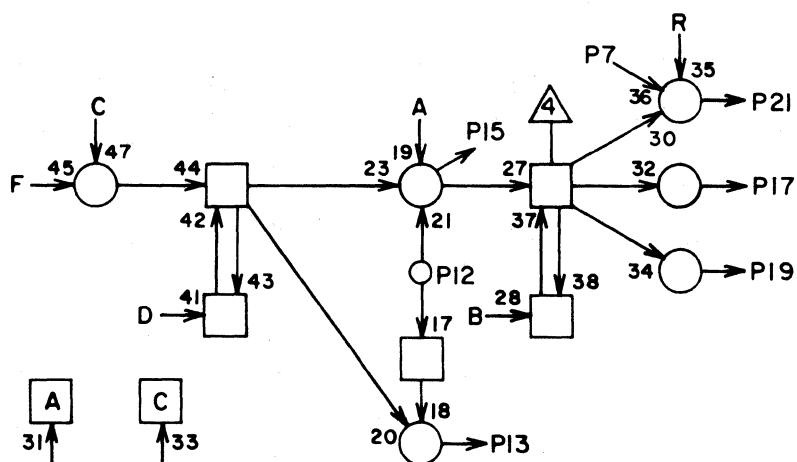
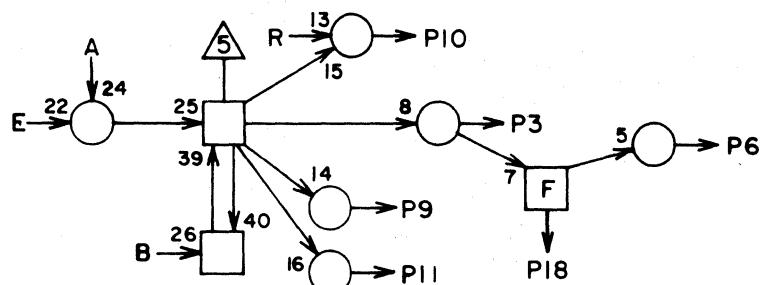
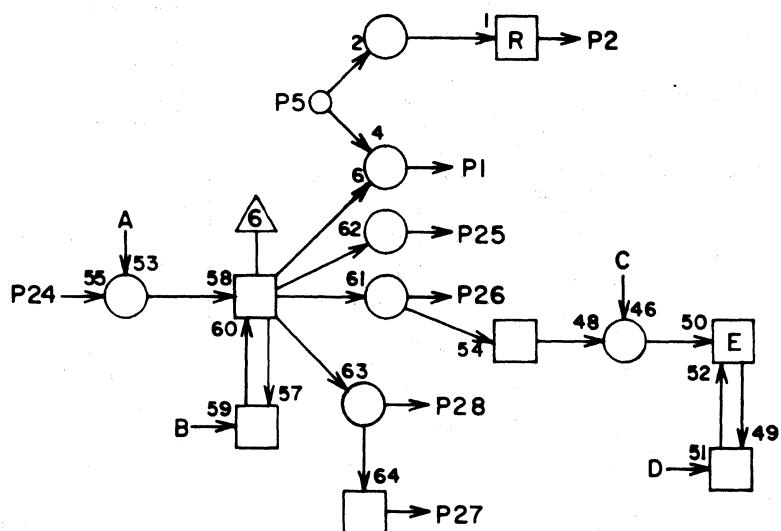
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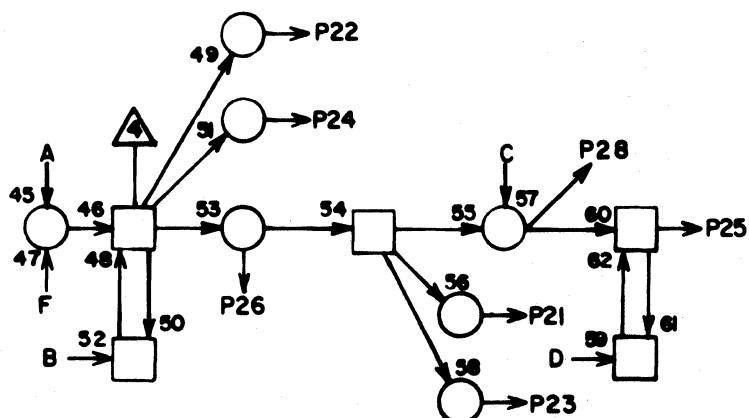
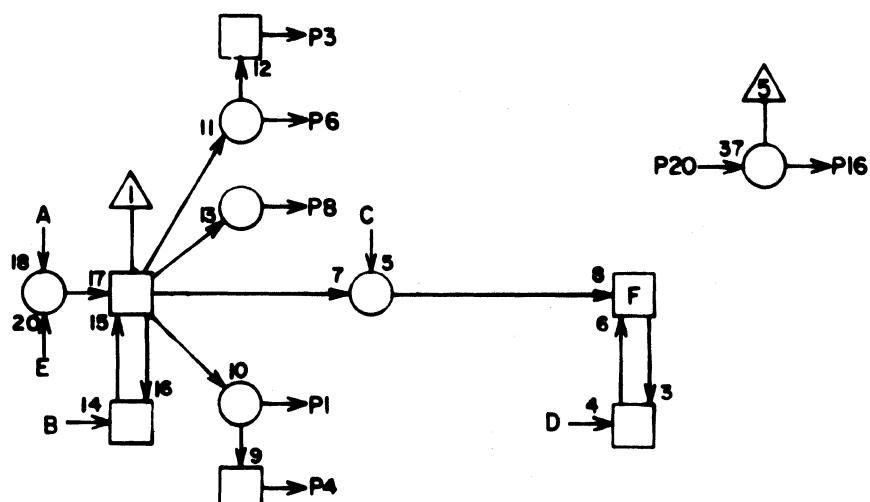
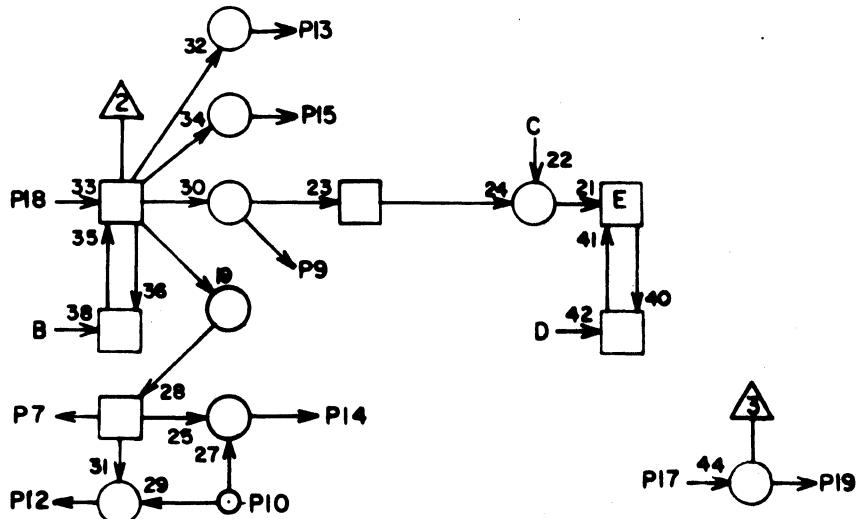
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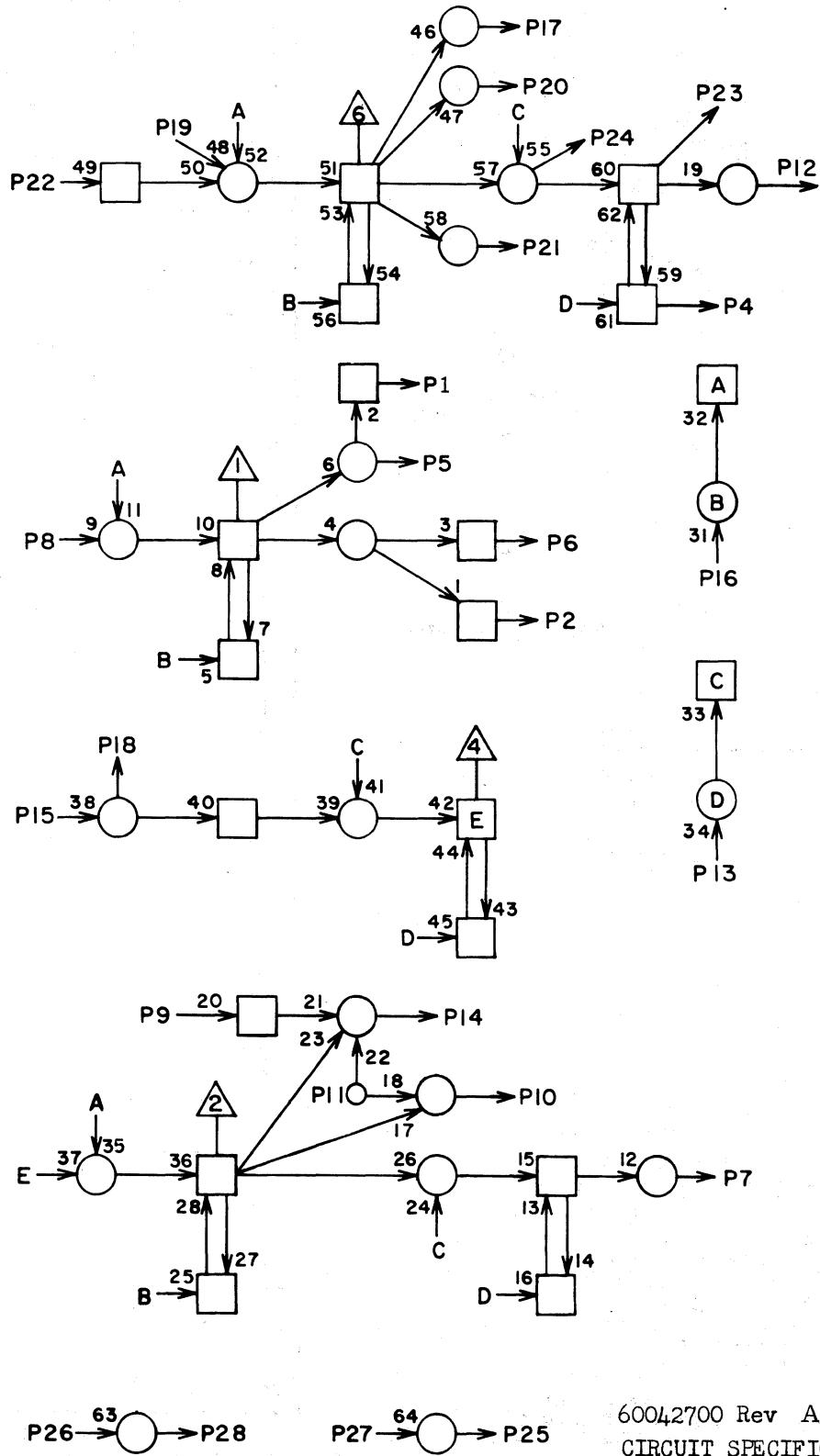
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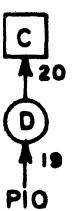
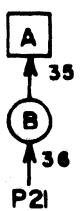
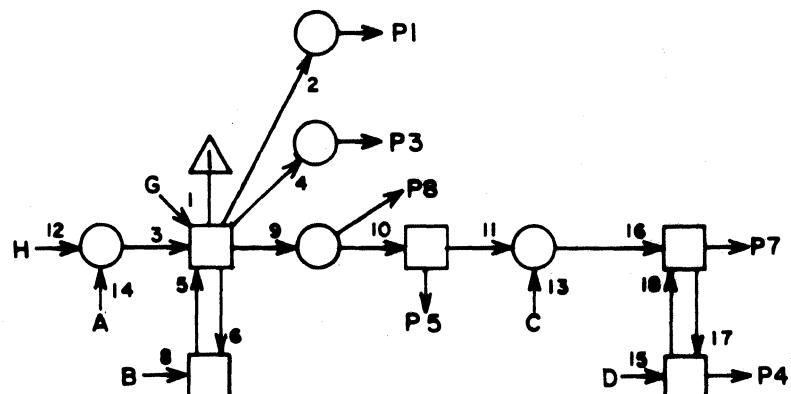
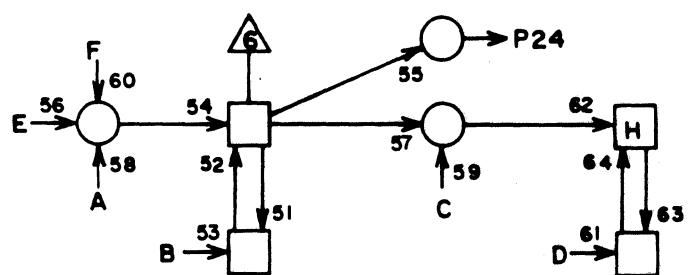
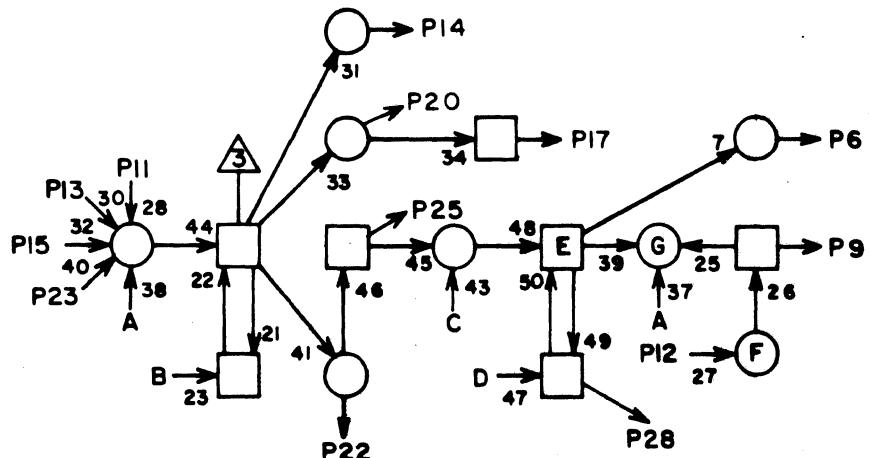
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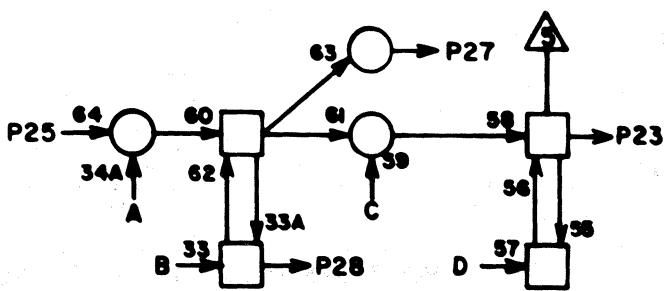
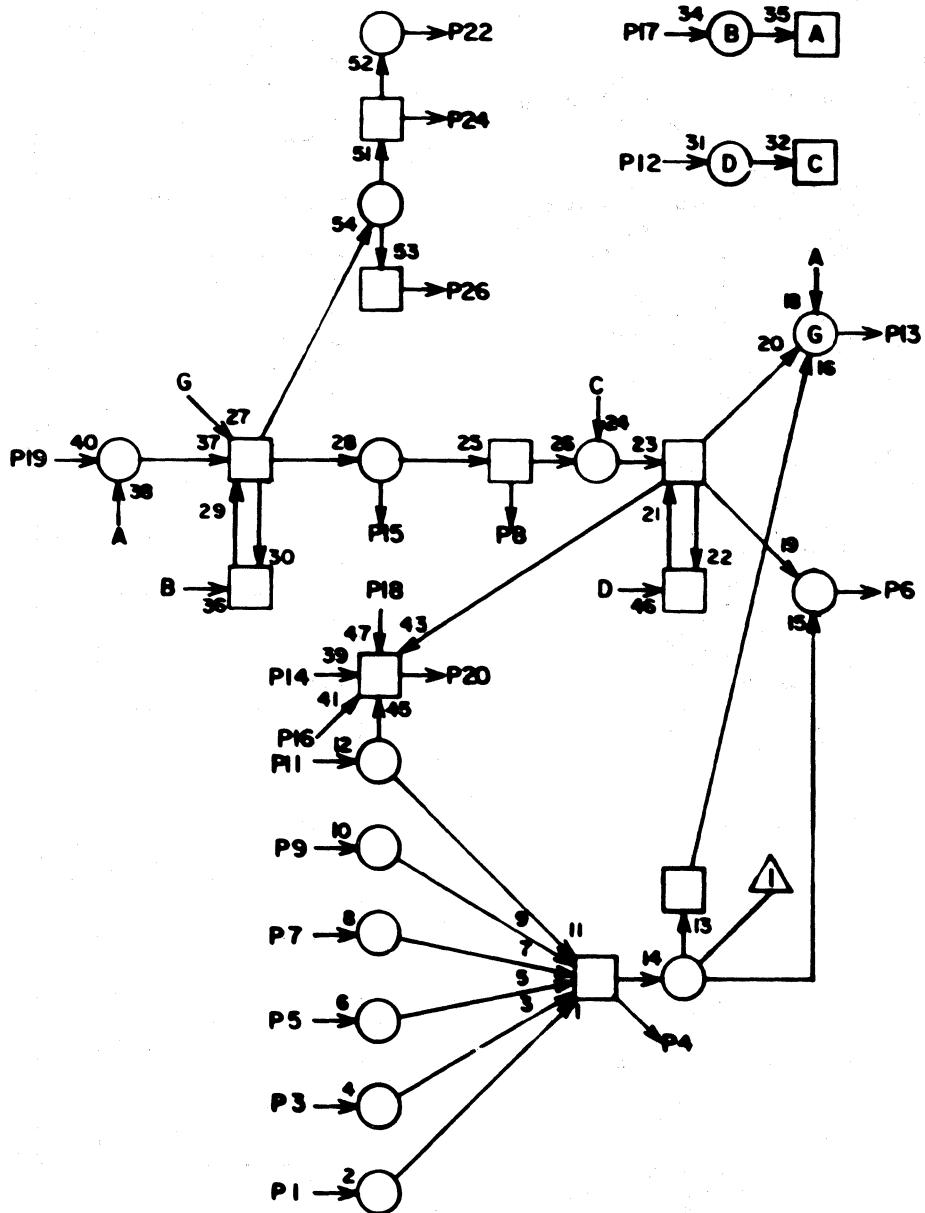
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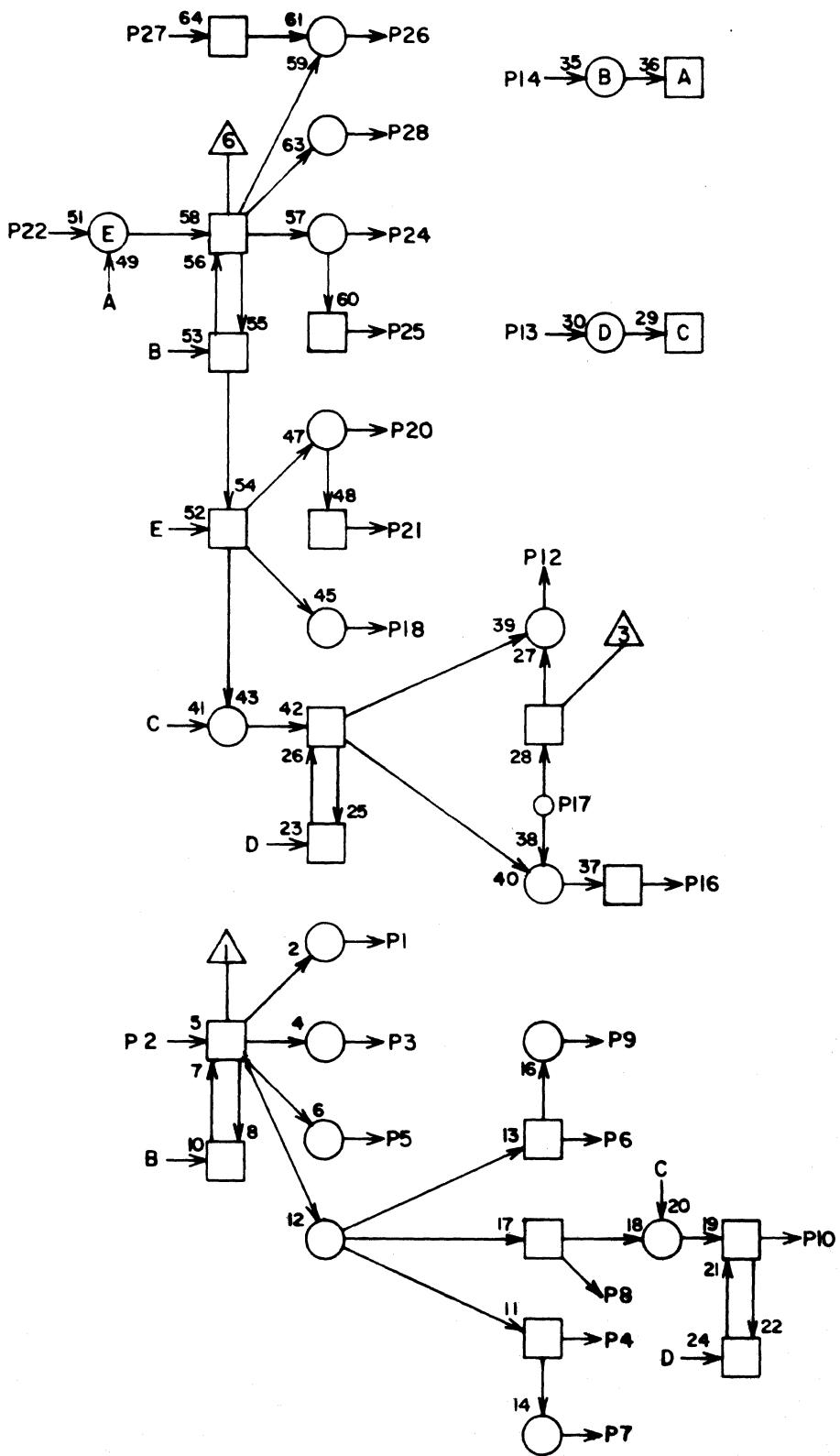
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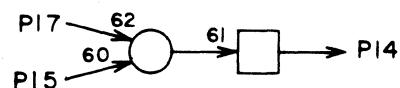
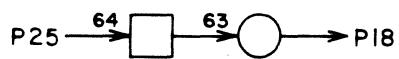
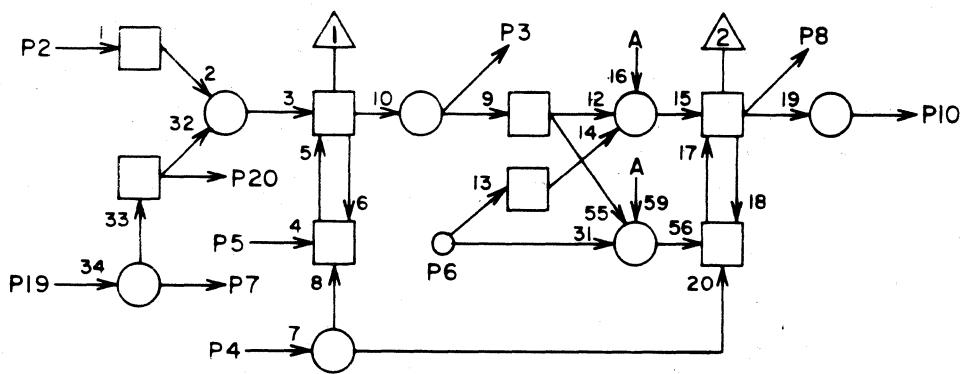
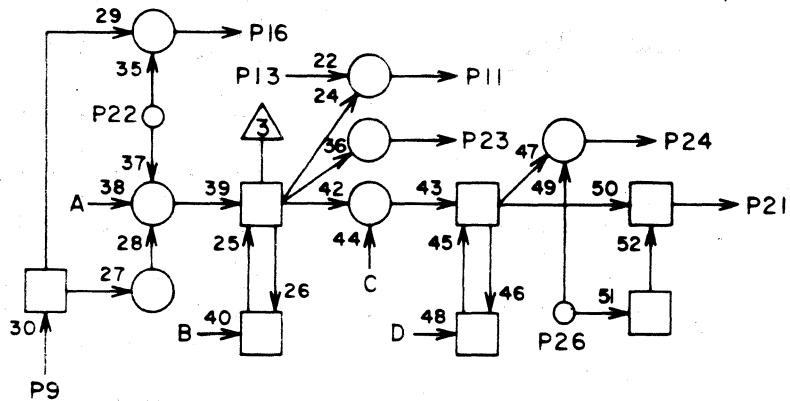
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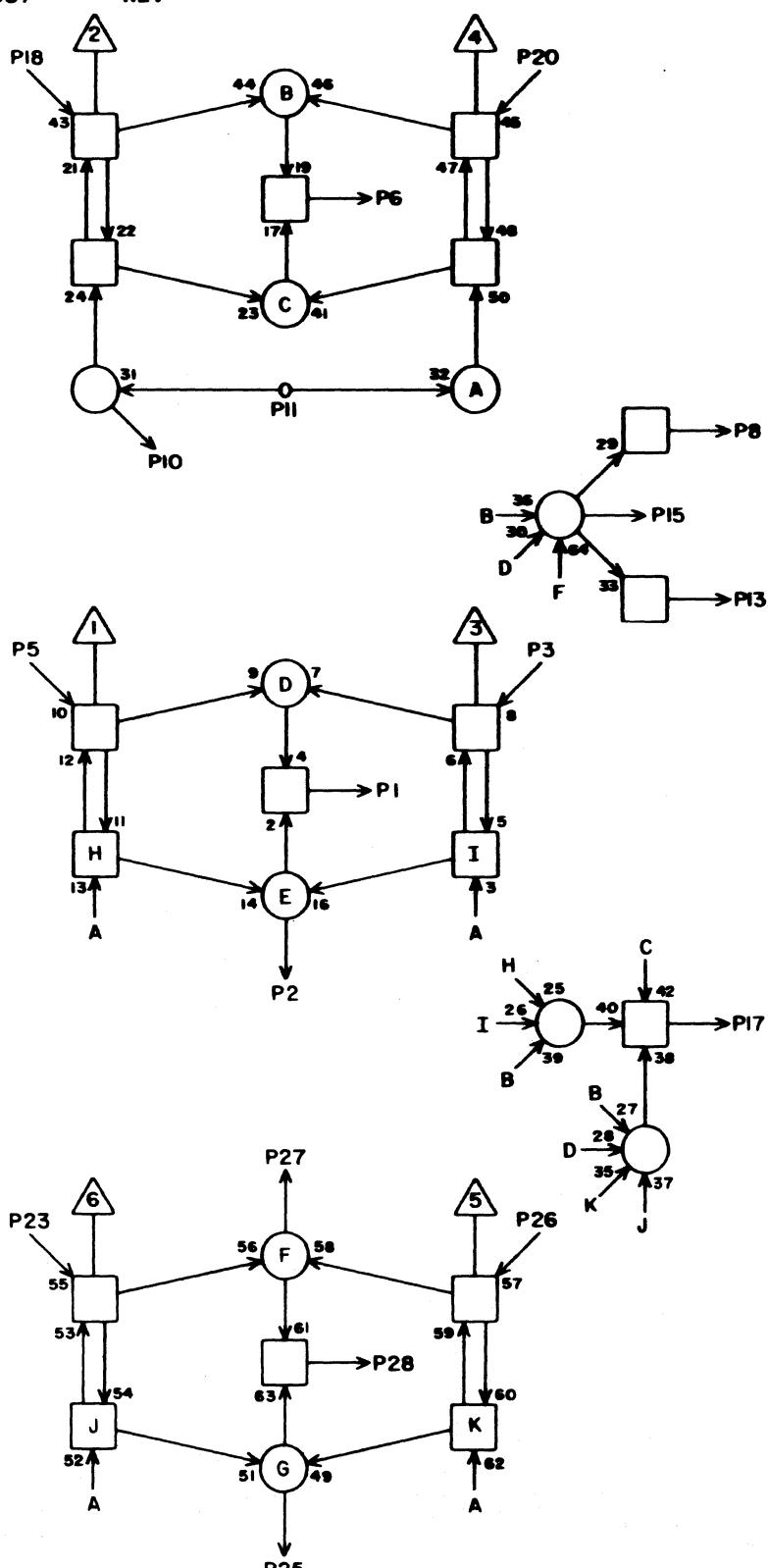
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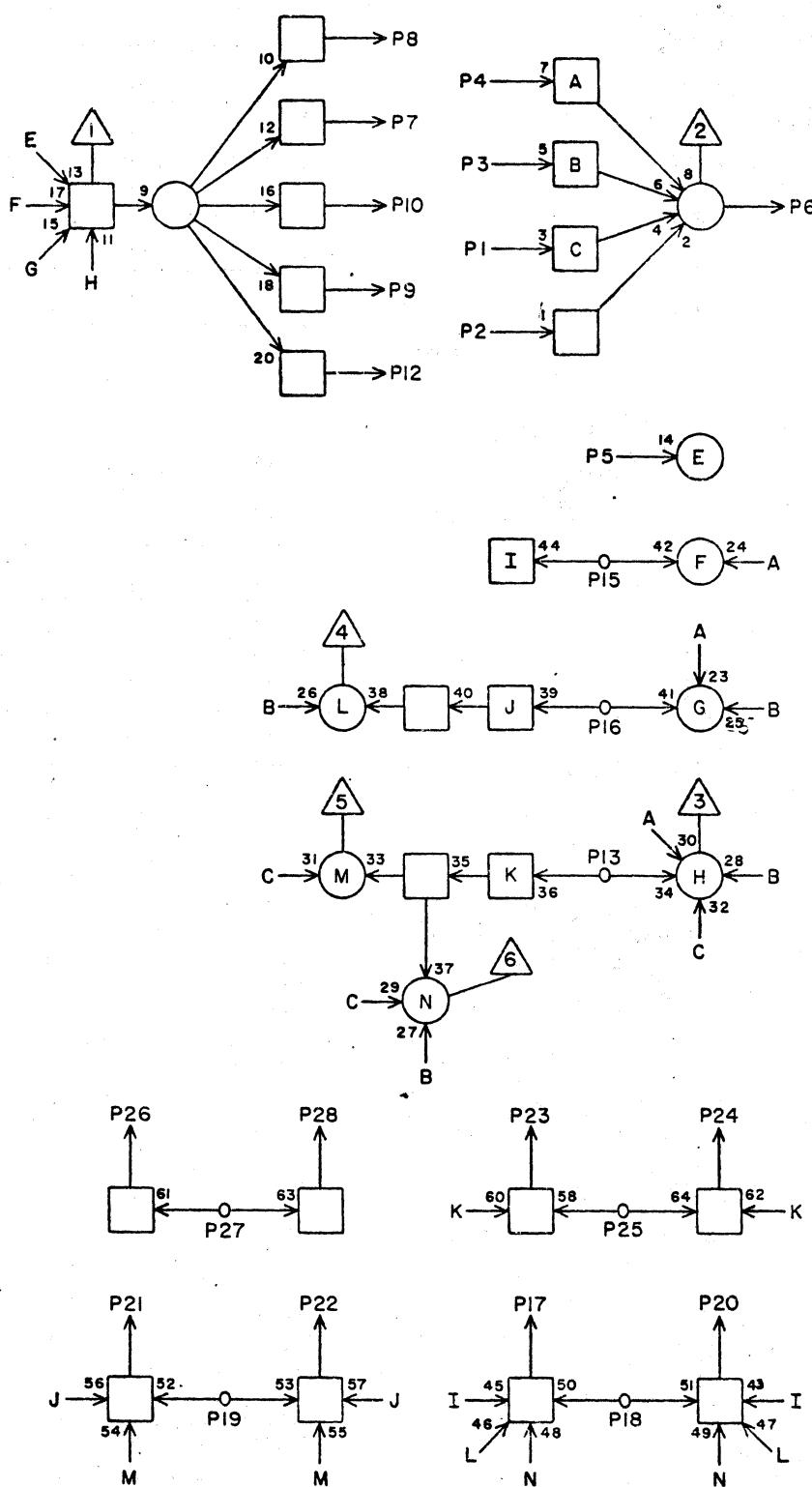
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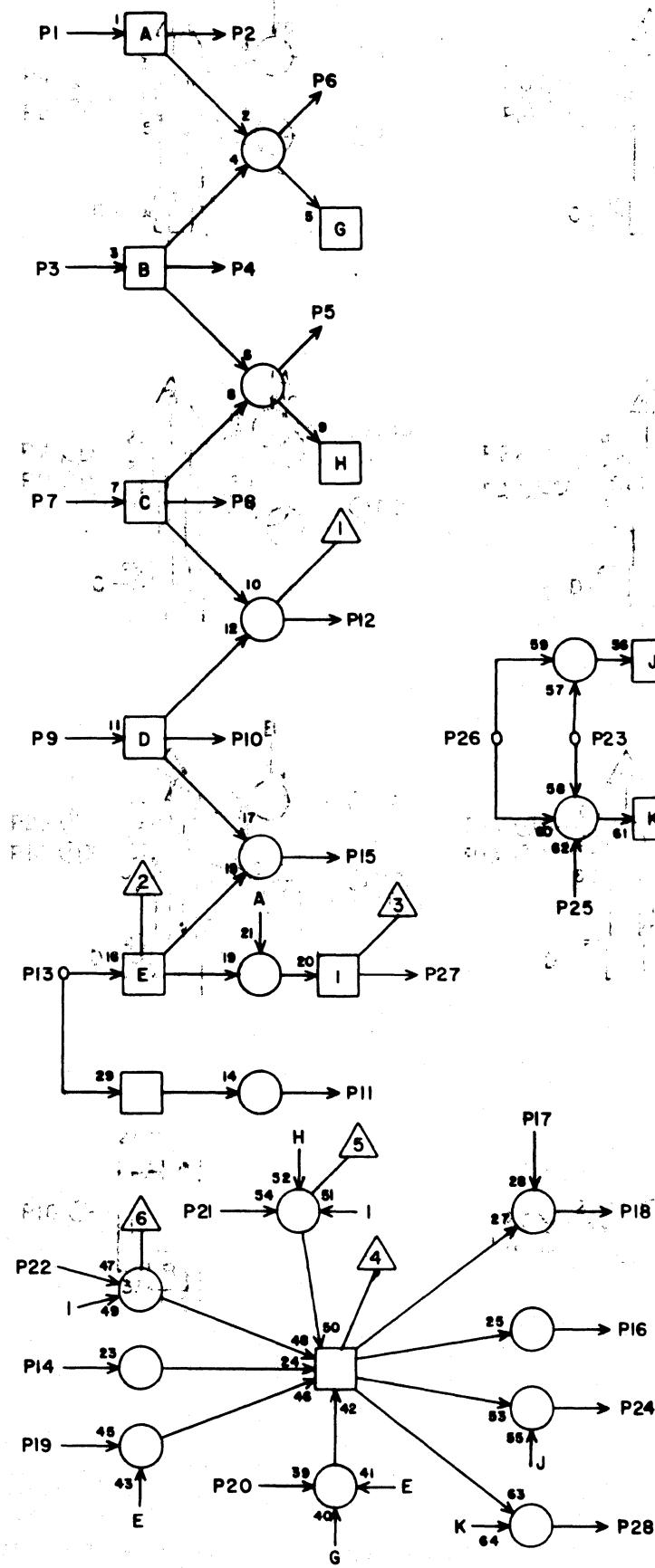
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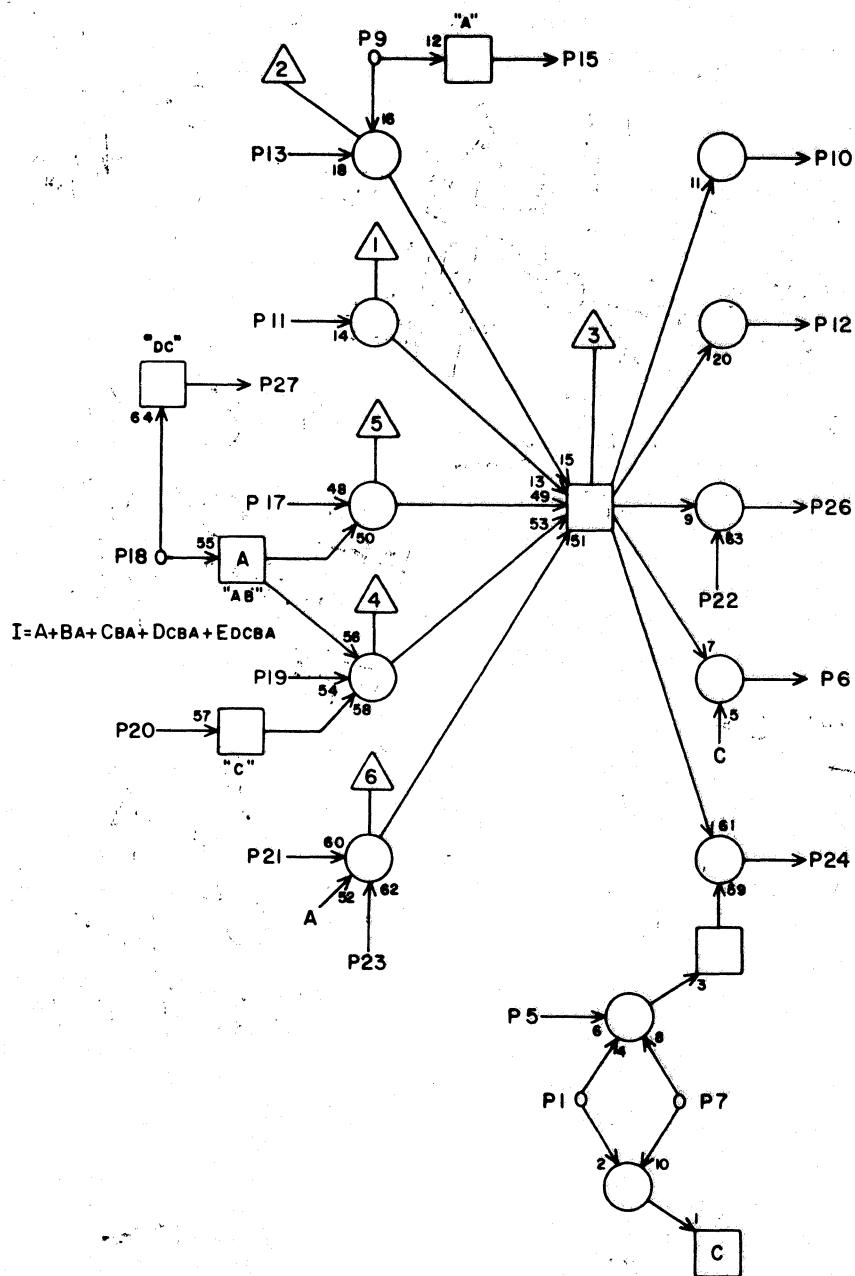
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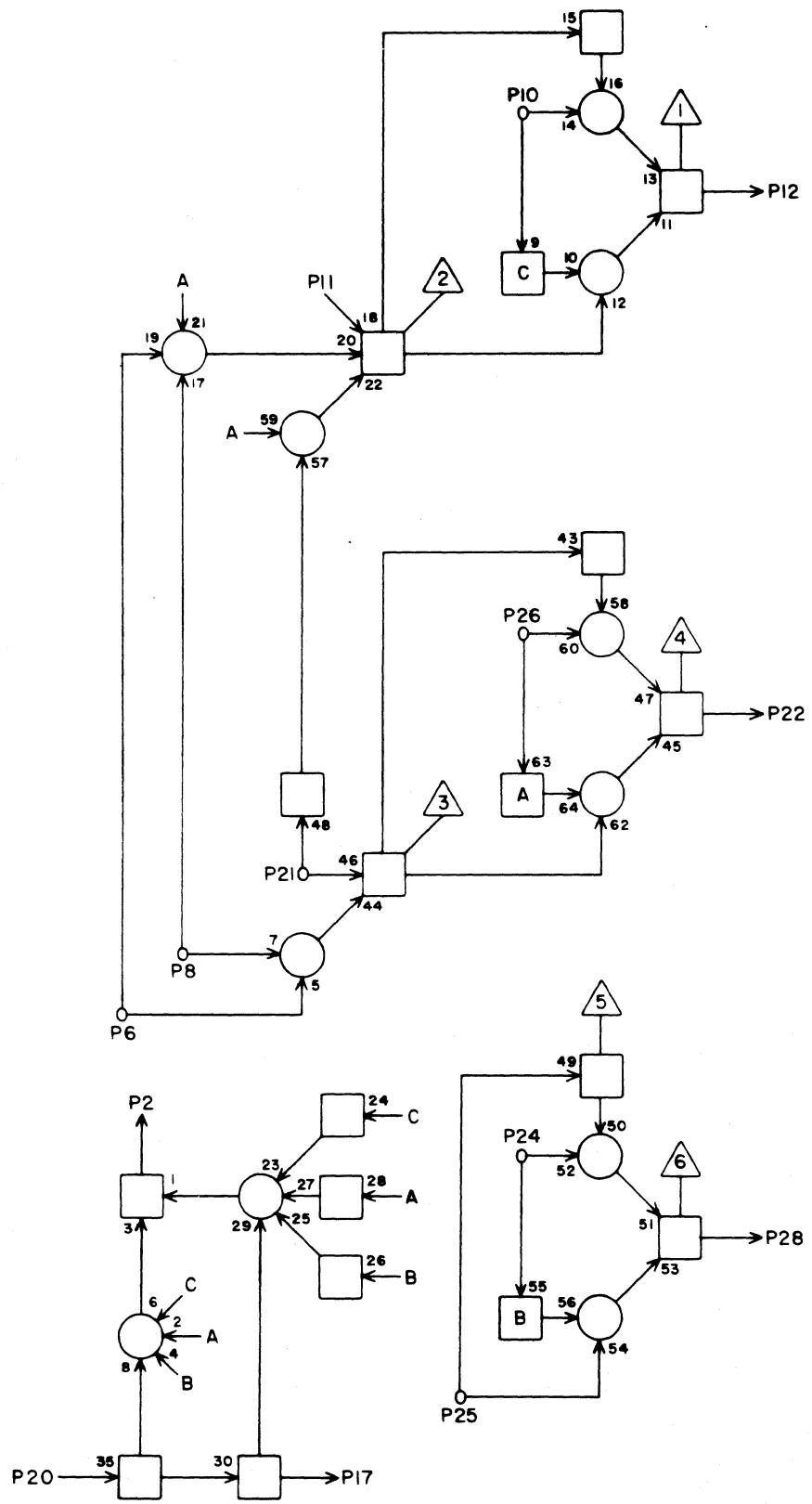
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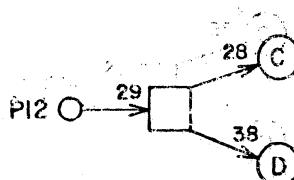
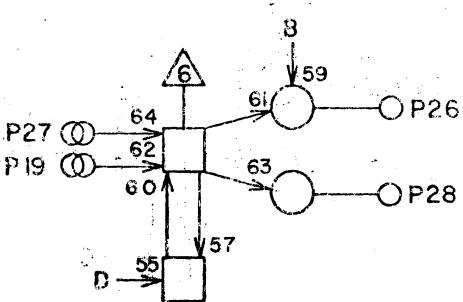
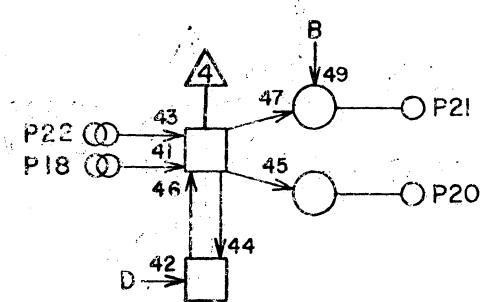
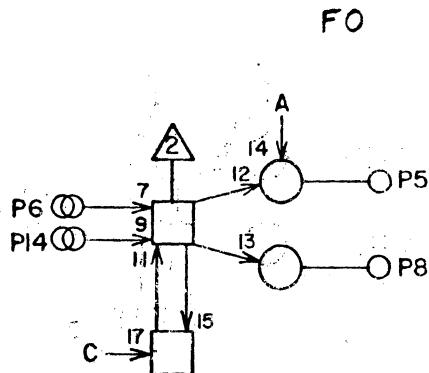
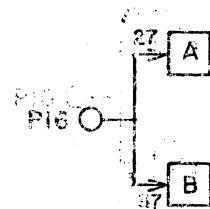
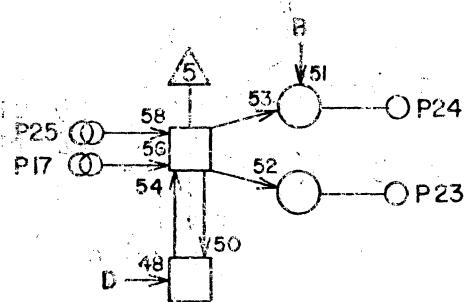
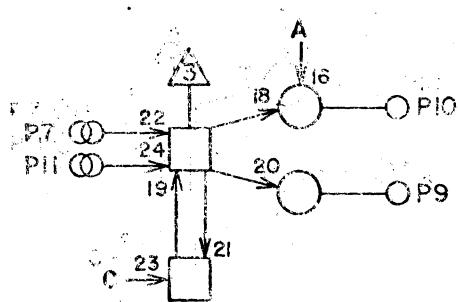
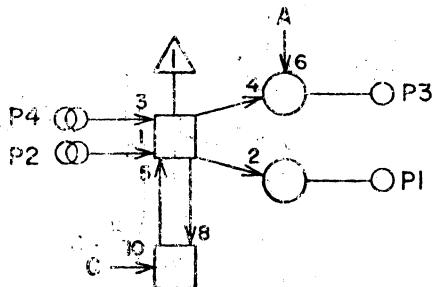
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J



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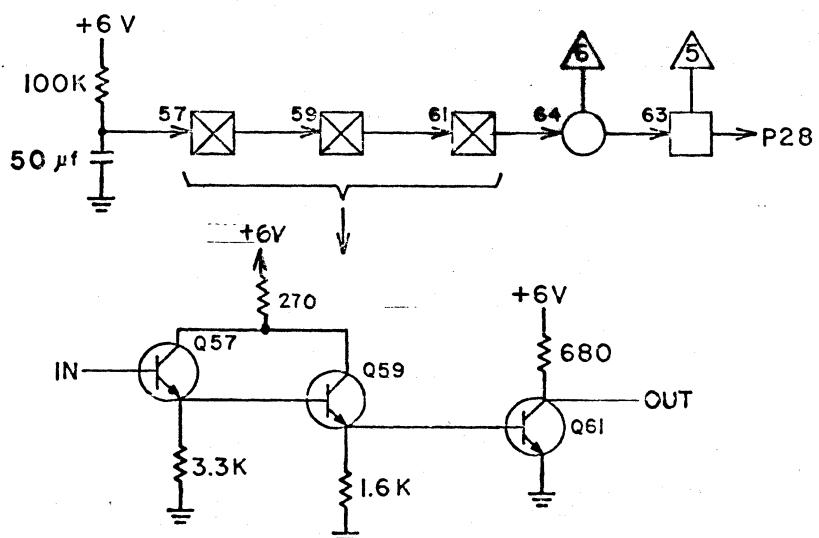
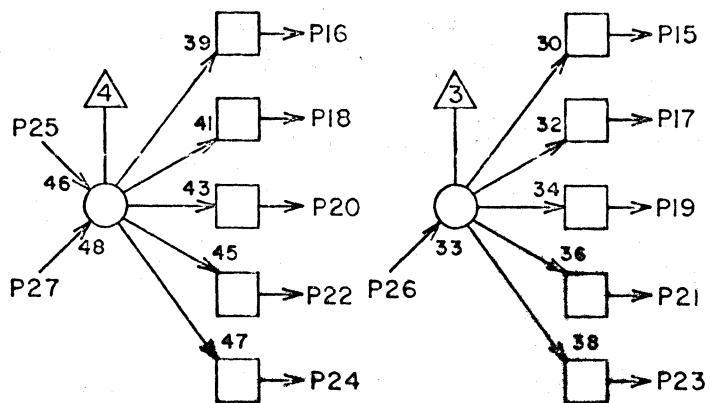
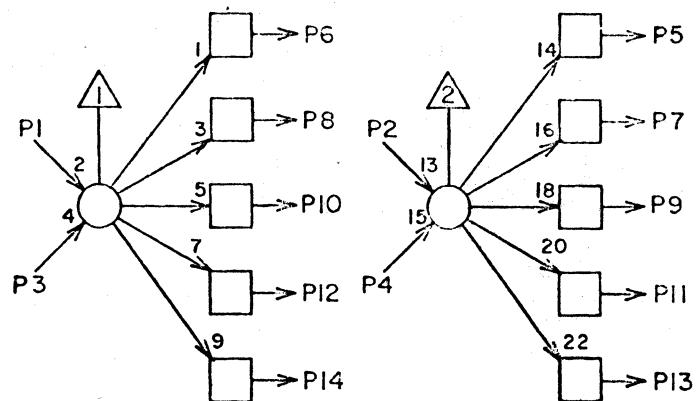
60042700 Rev Z

JACK PIN LG
SEE CIRCUIT SPECIFICATION
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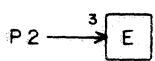
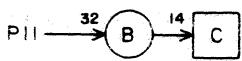
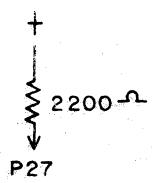
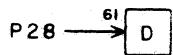
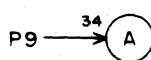
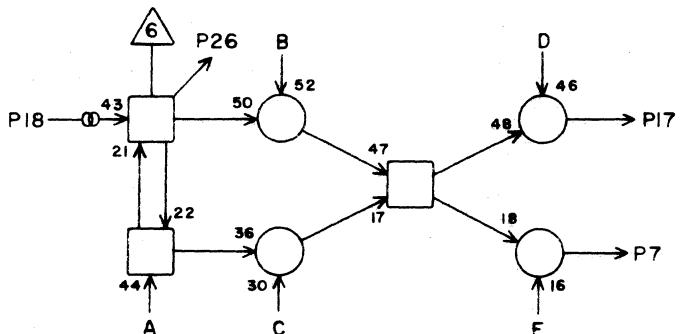
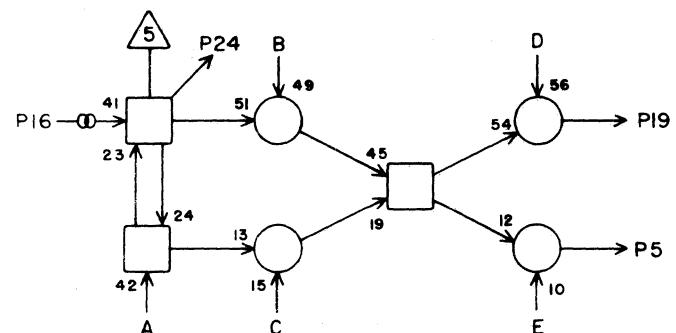
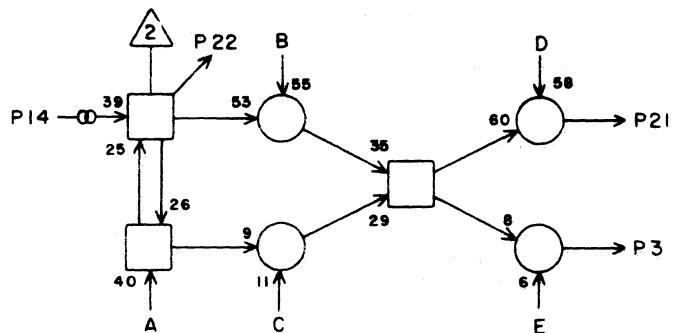
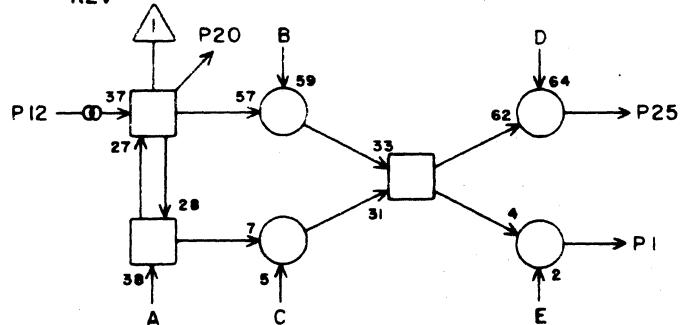
60042700 Rev. Z

JACK PIN LG
SEE CIRCUIT SPECIFICATION
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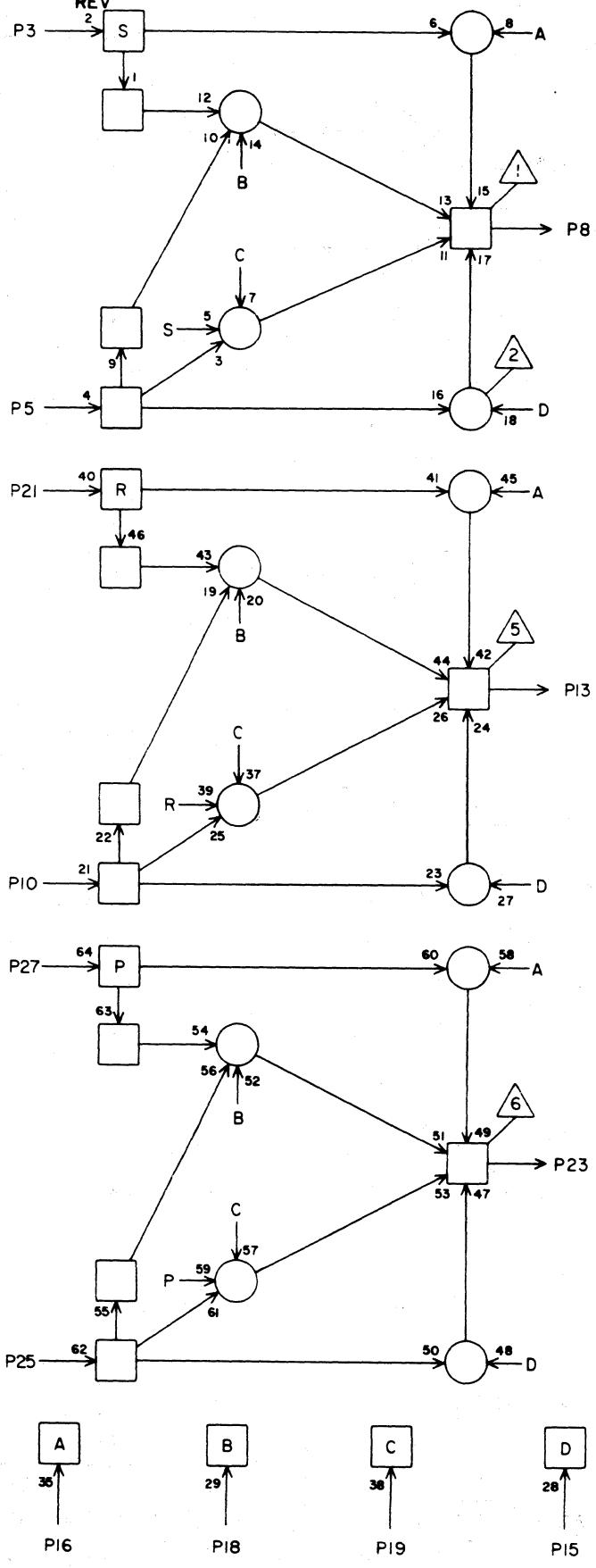
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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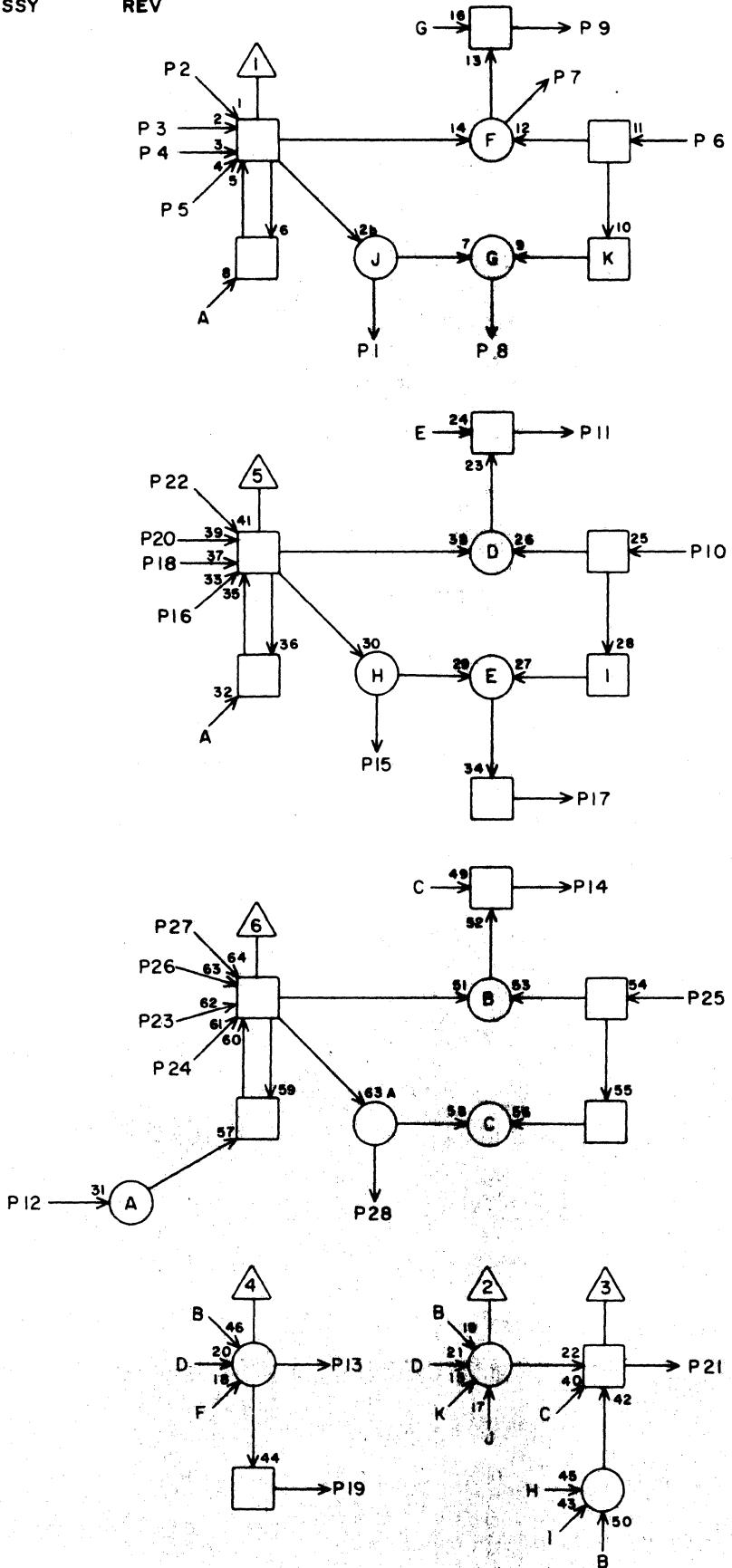
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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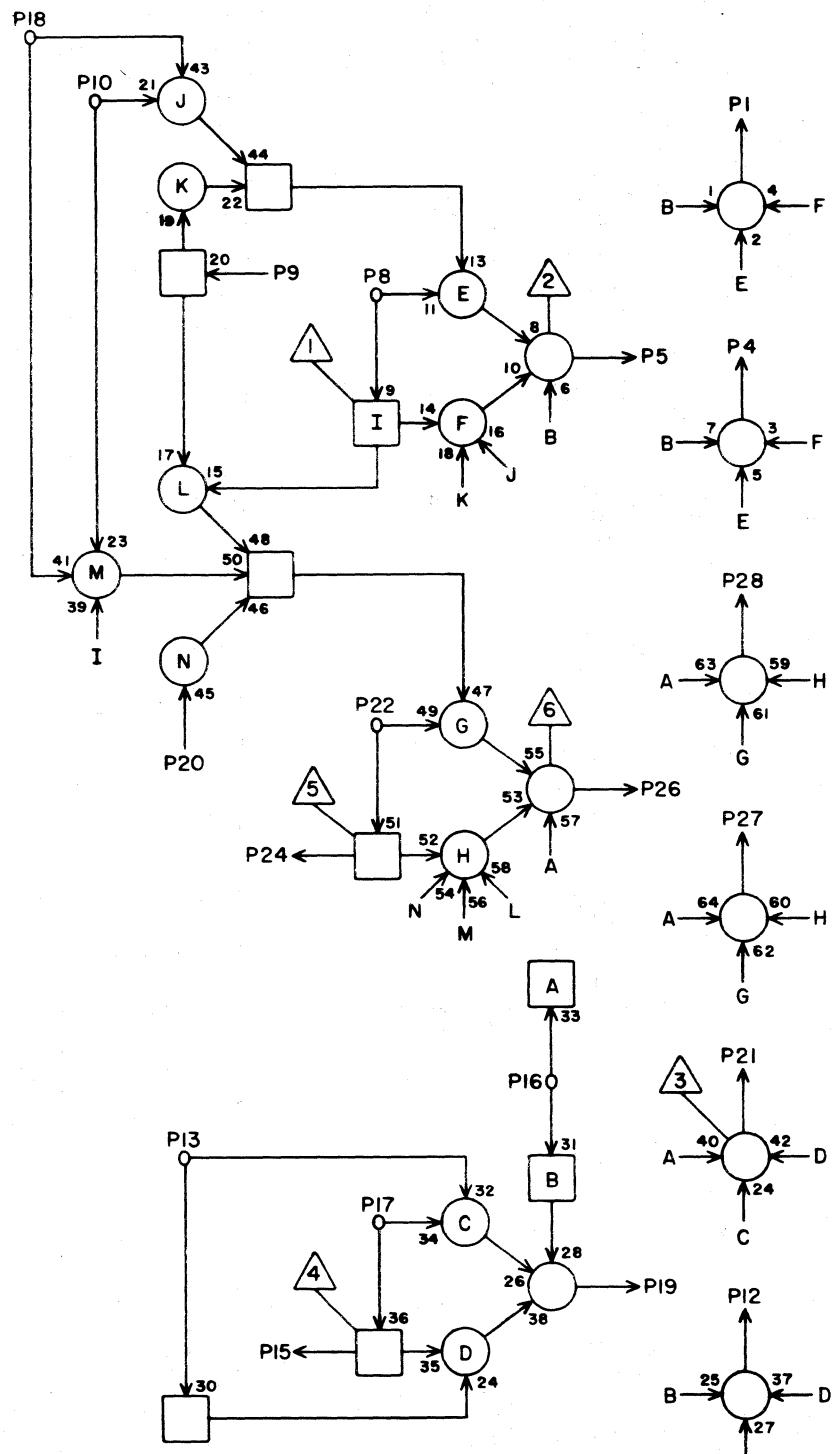
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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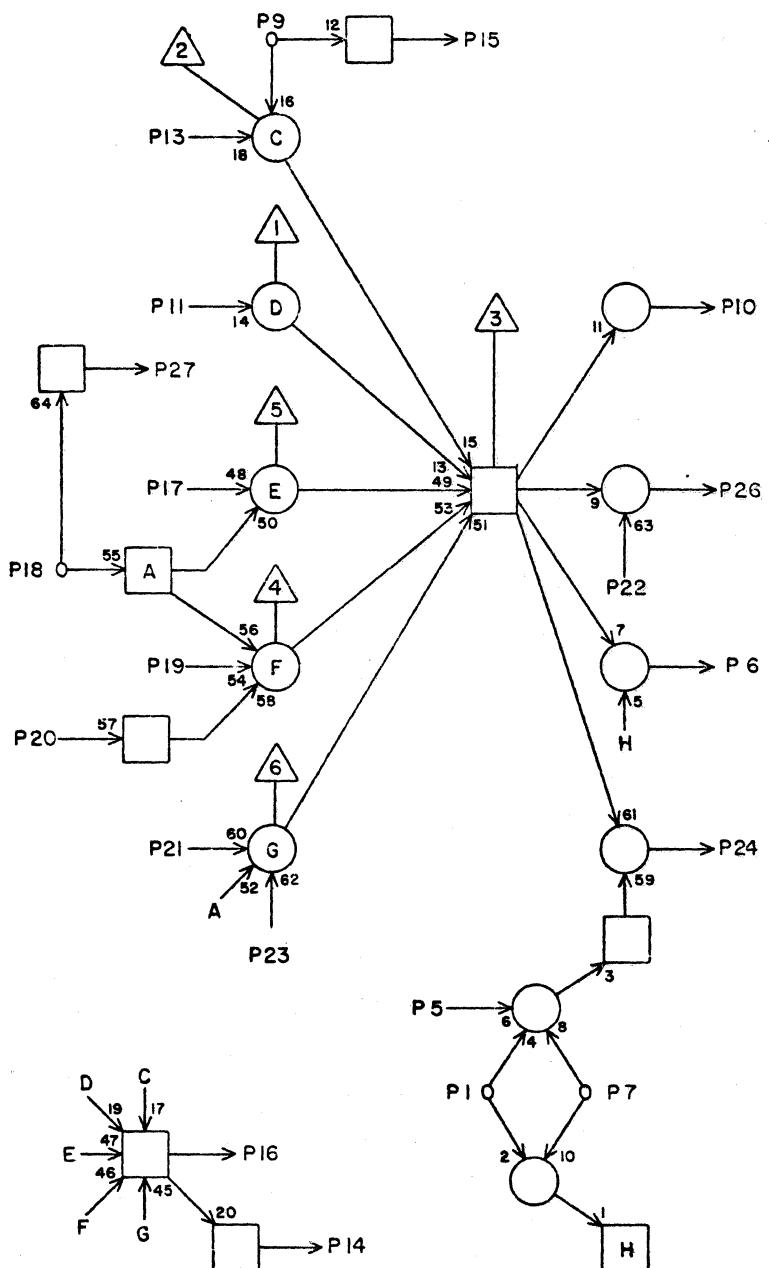
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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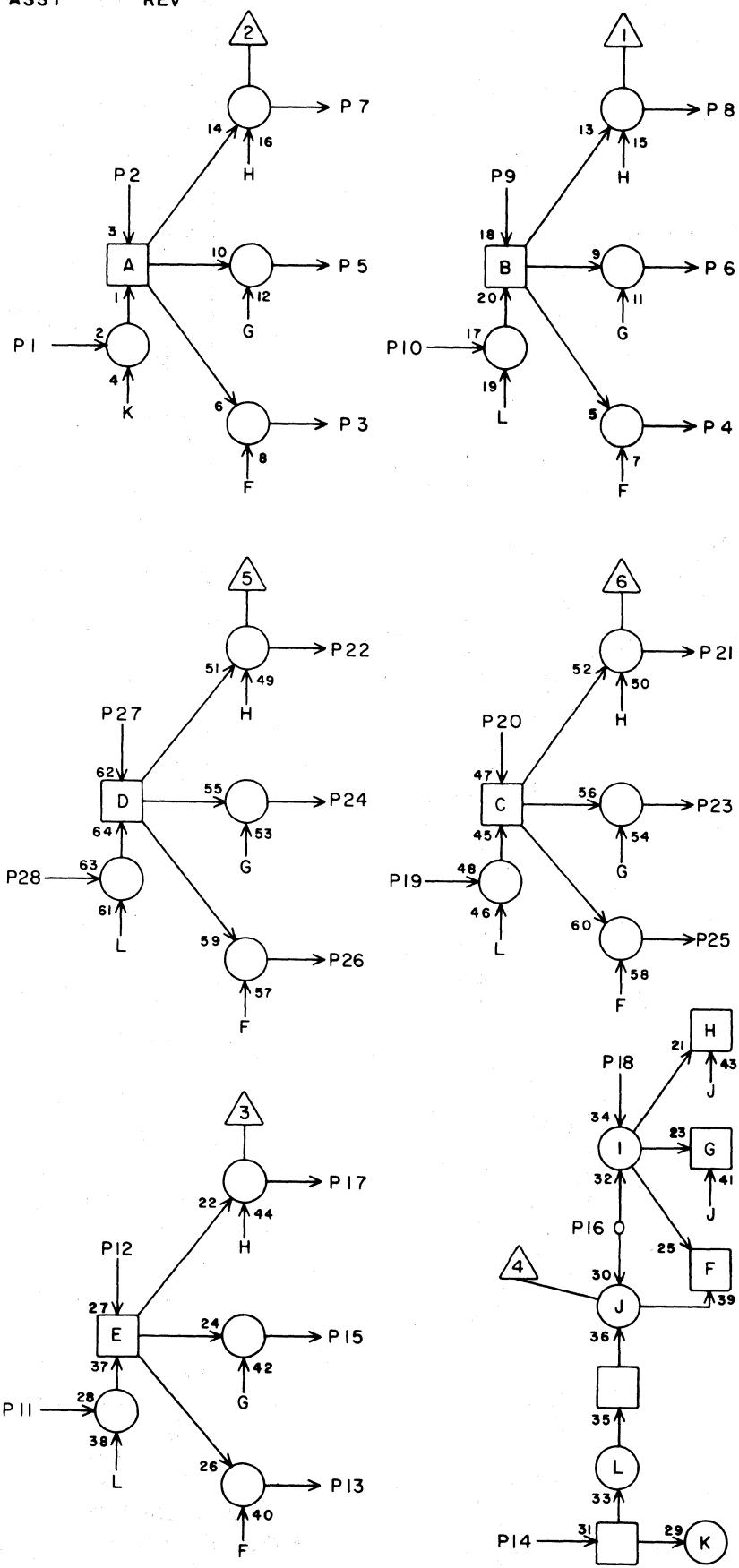
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60042700 Rev. J

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CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

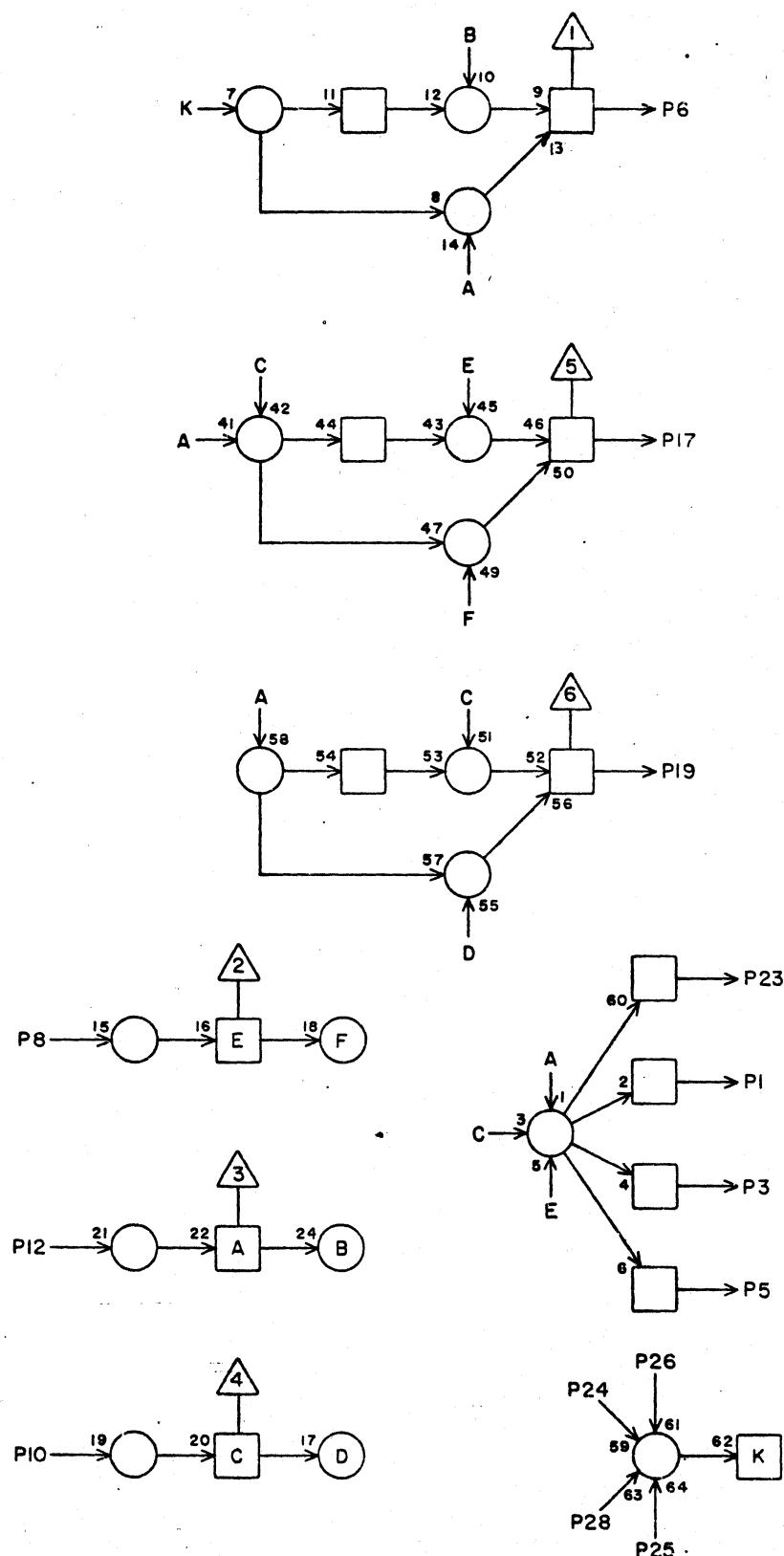


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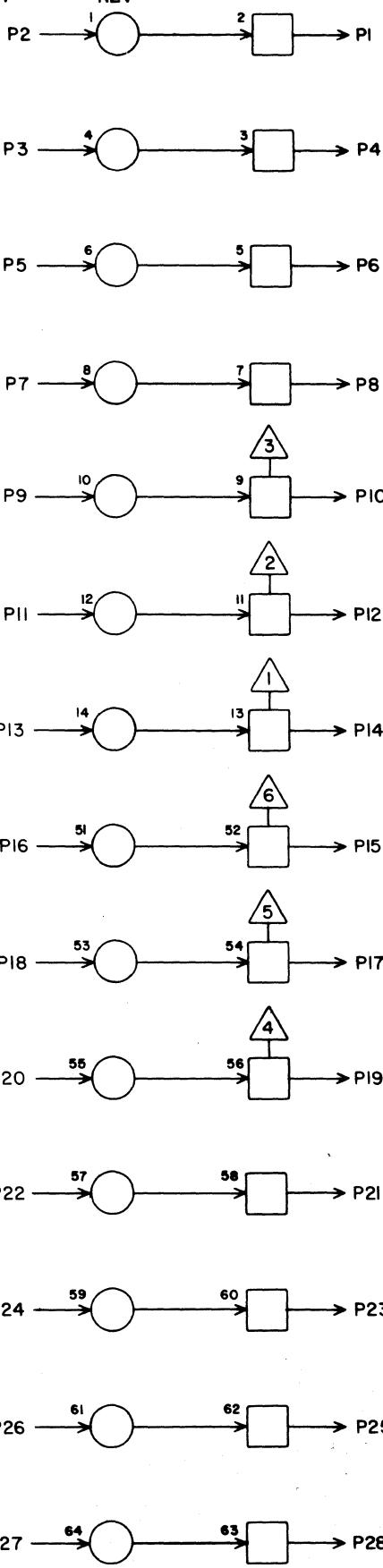
CIRCUIT SPECIFICATION 11827600
60042700 Rev. Y

JACK PIN LG

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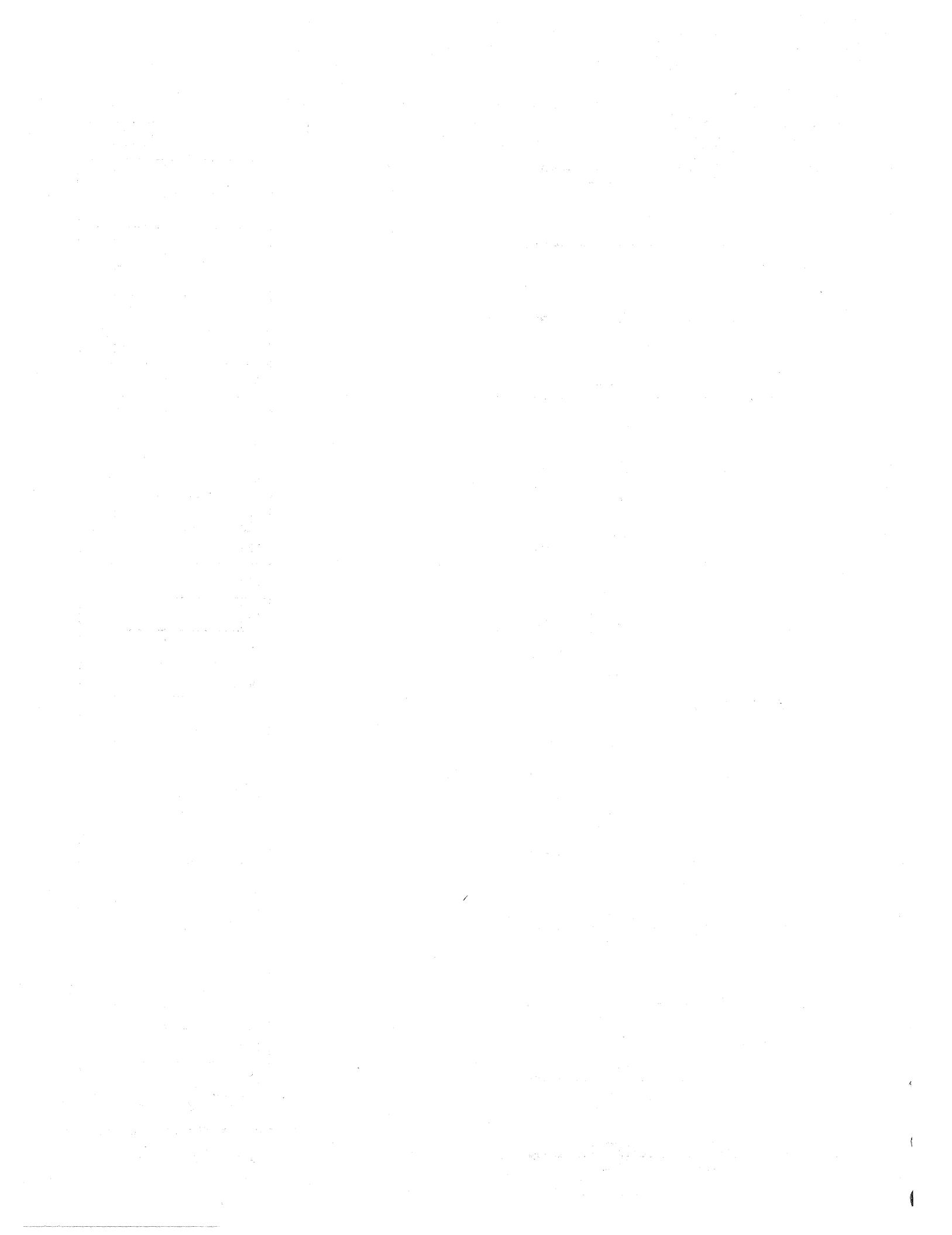
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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

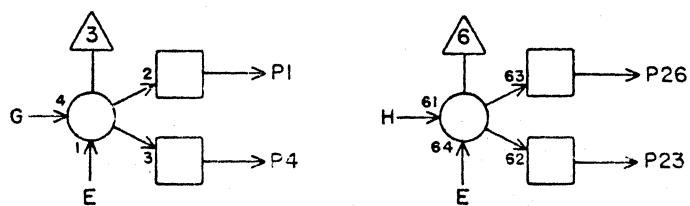
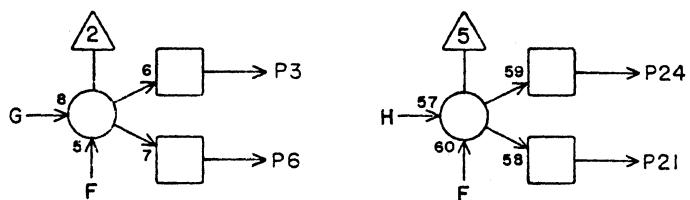
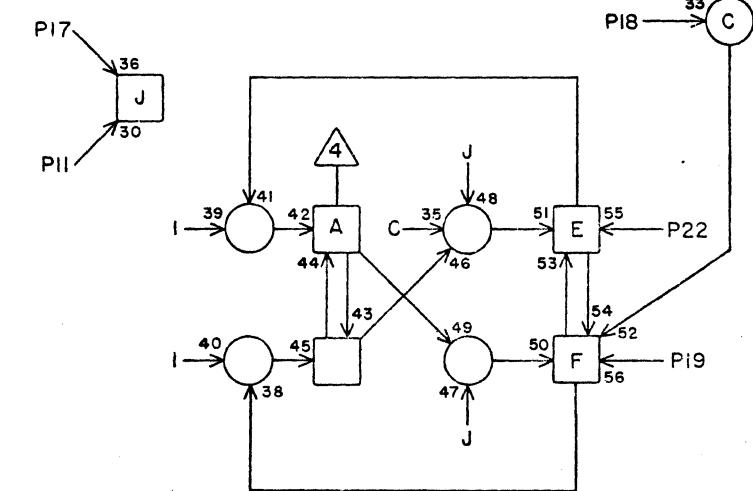
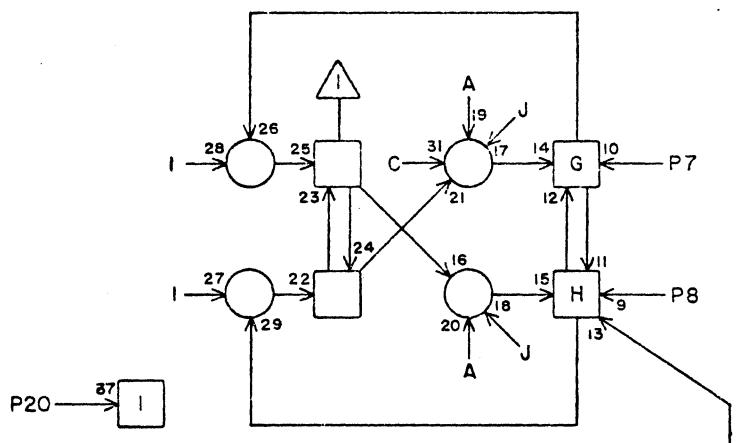
60042700 Rev. J



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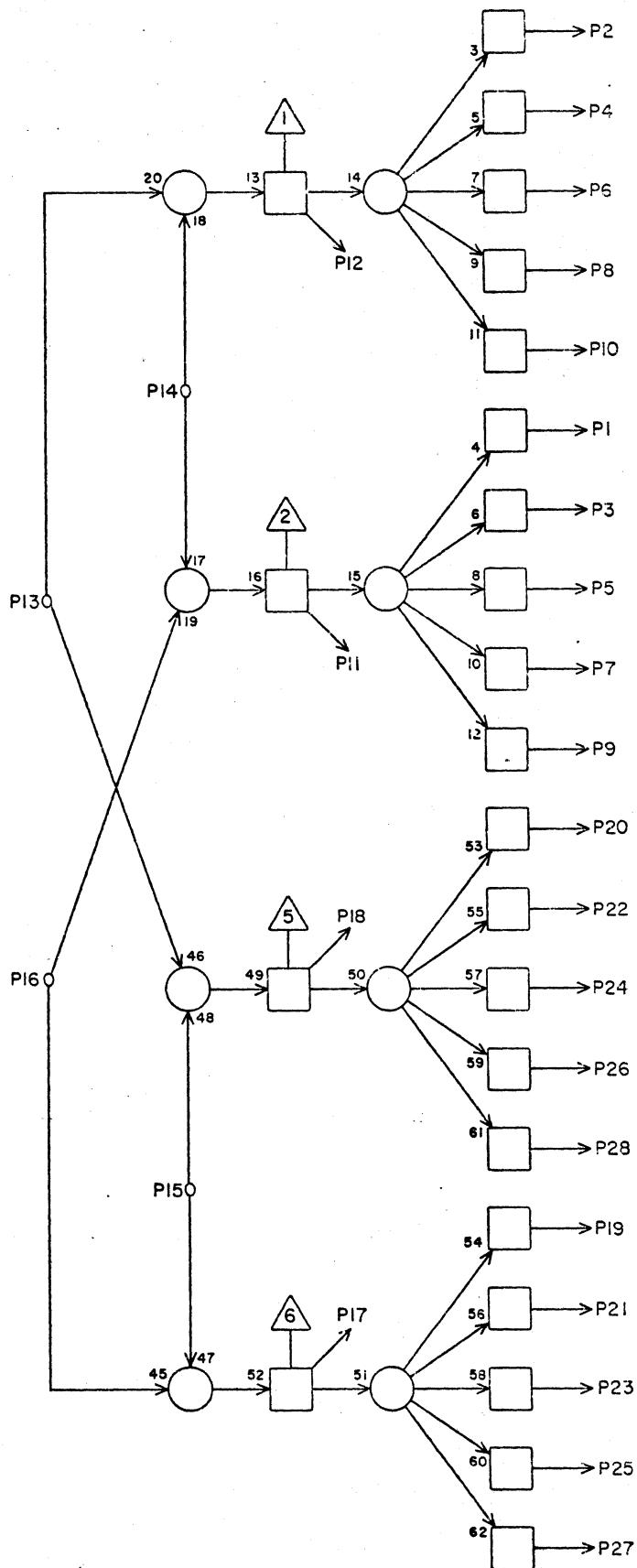
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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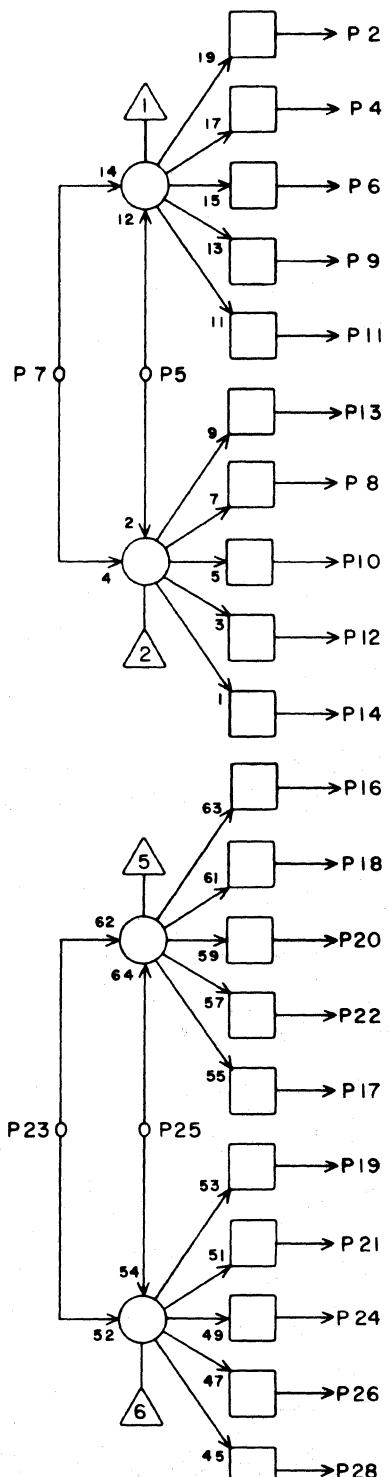


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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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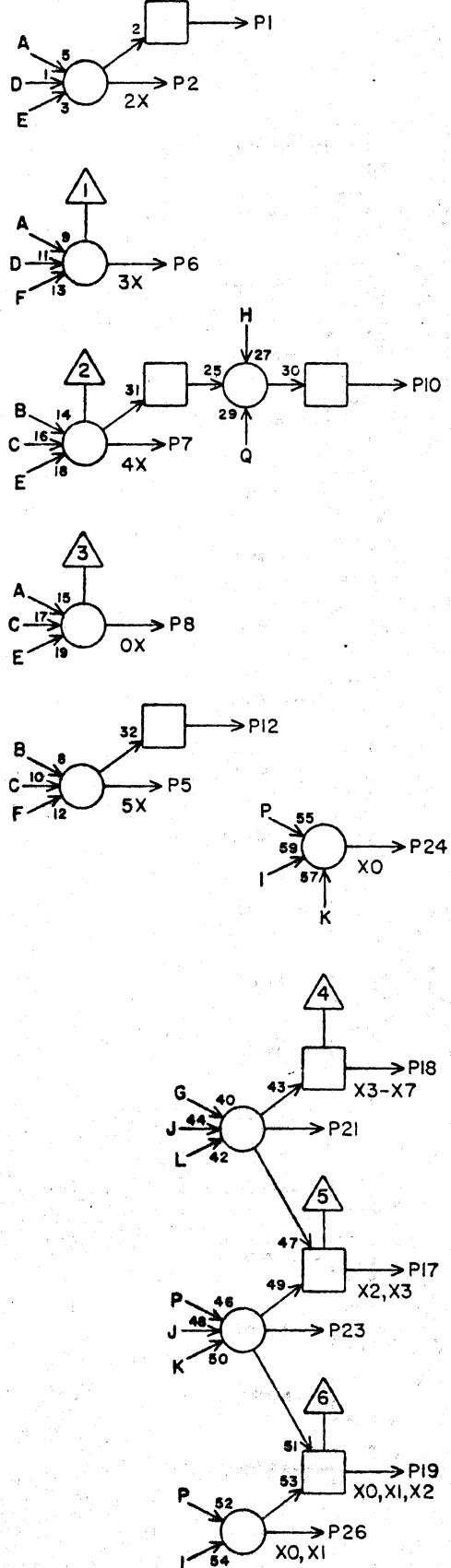
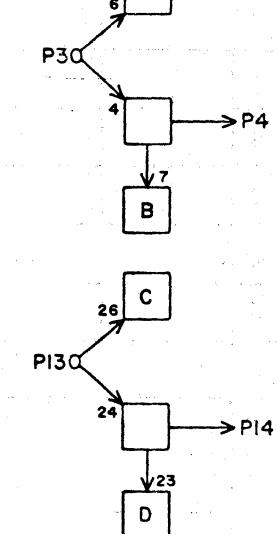
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CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

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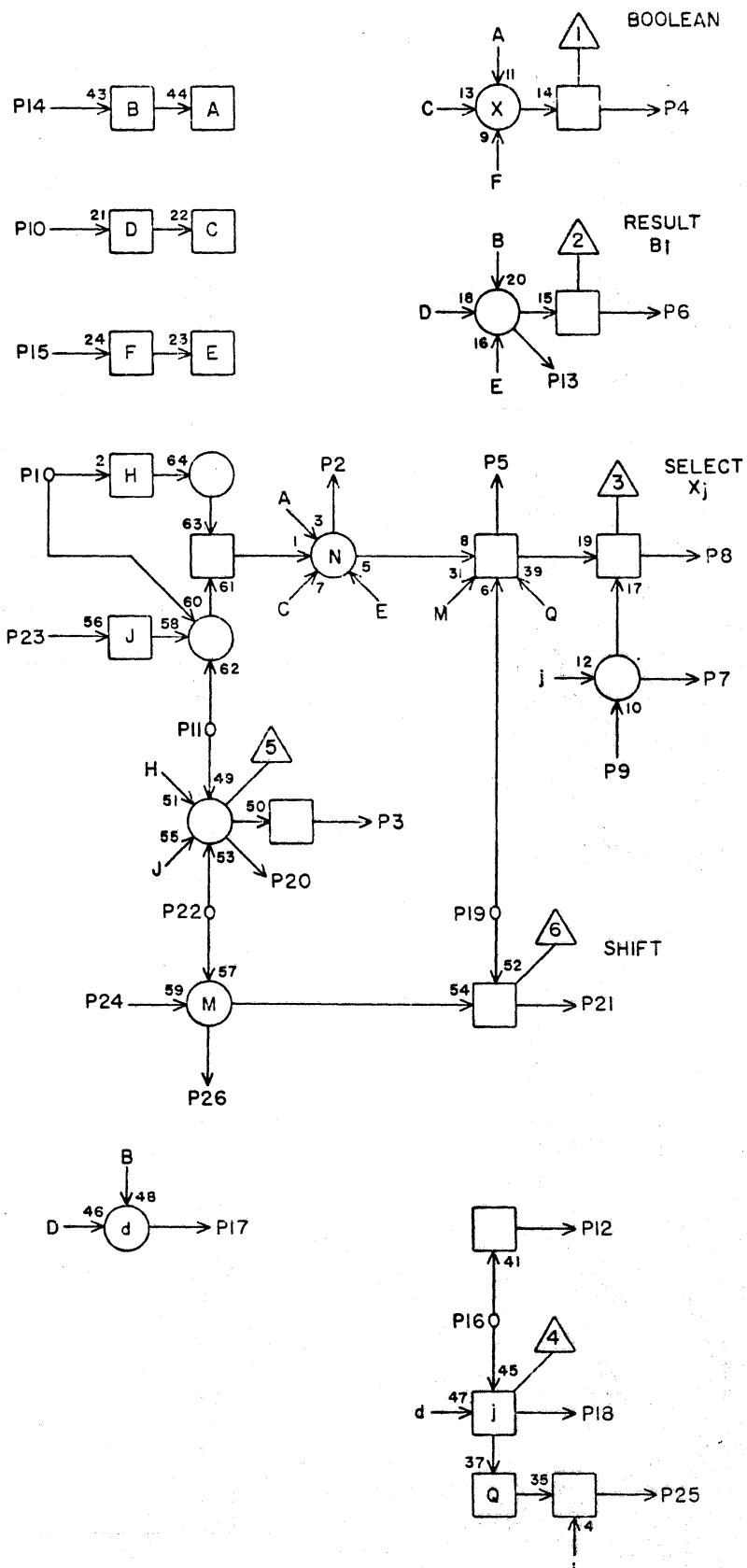
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60042700 Rev. J

LS 63045000
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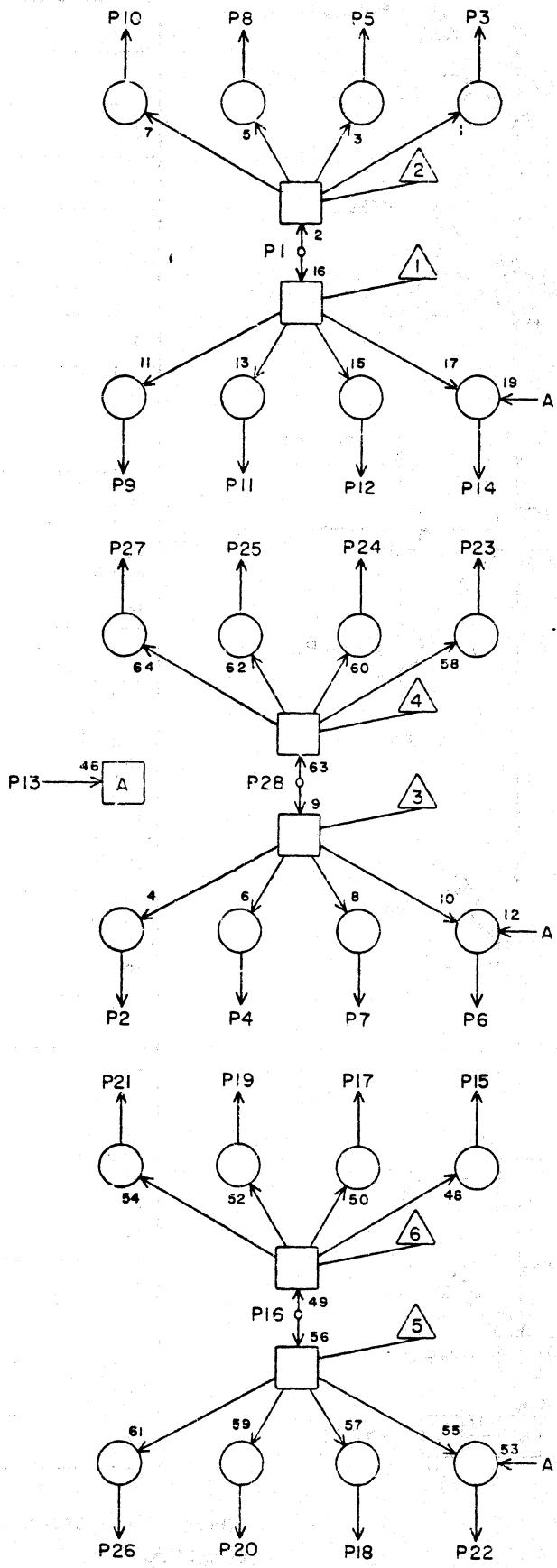
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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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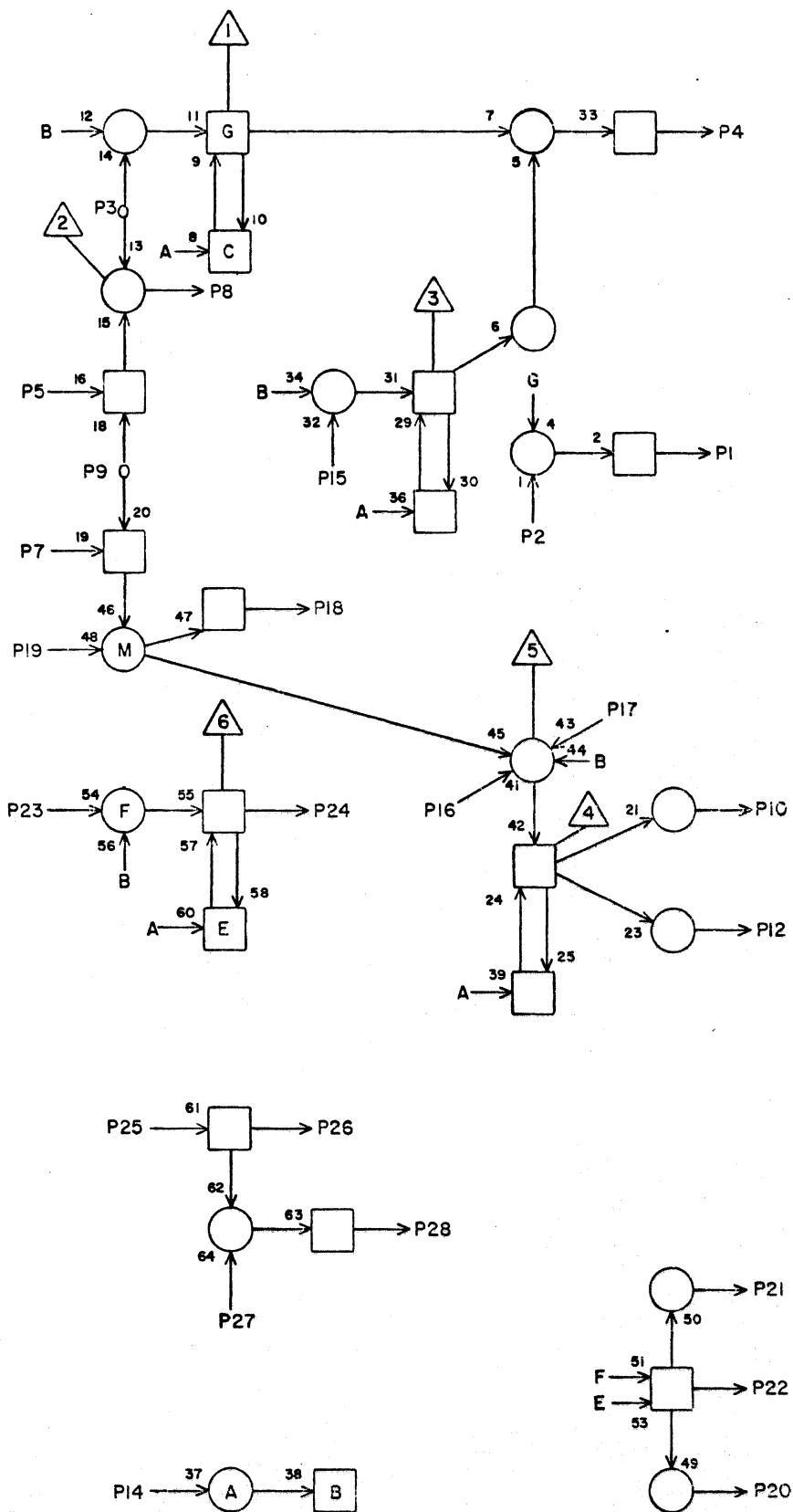
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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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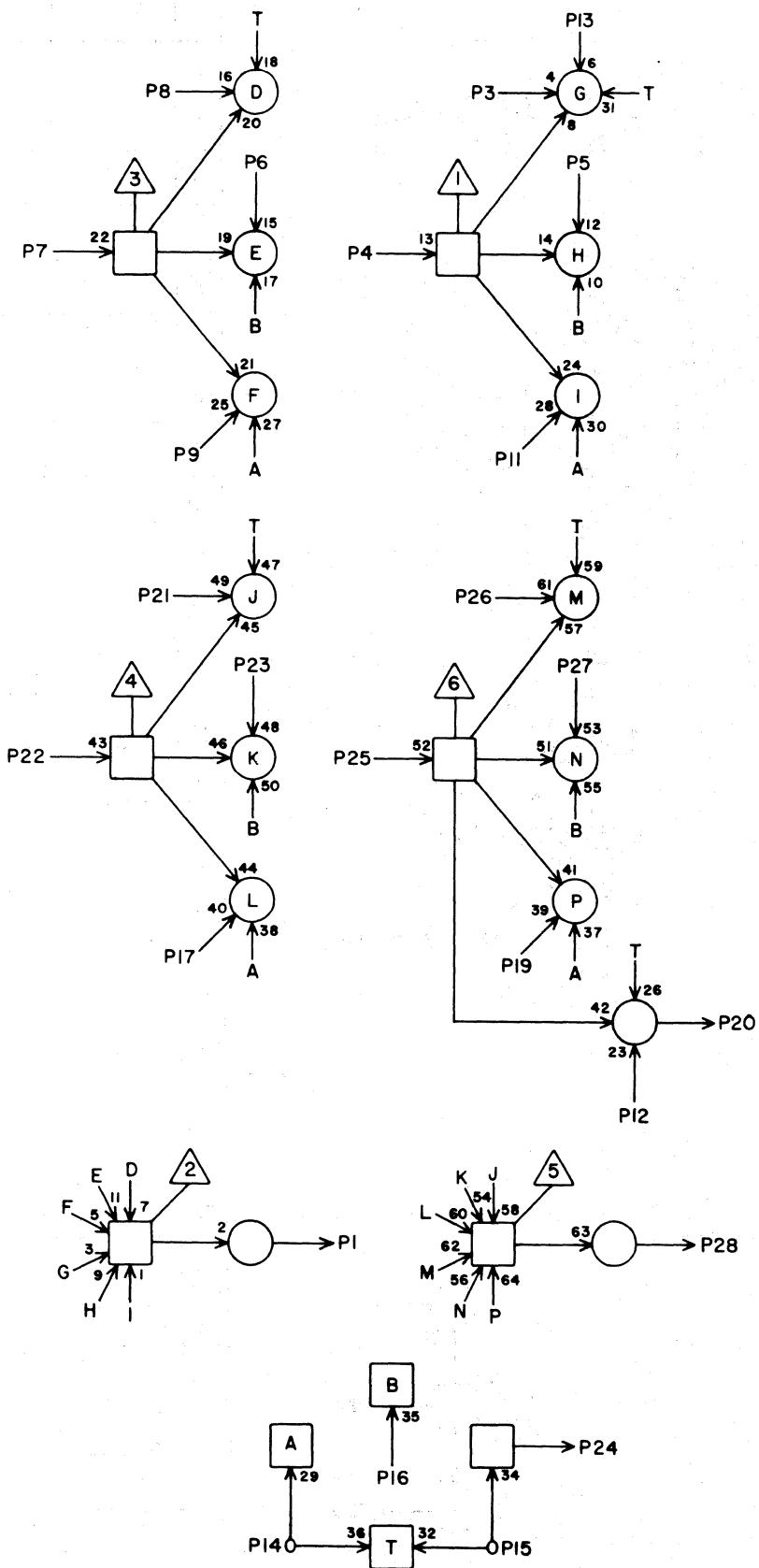
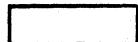
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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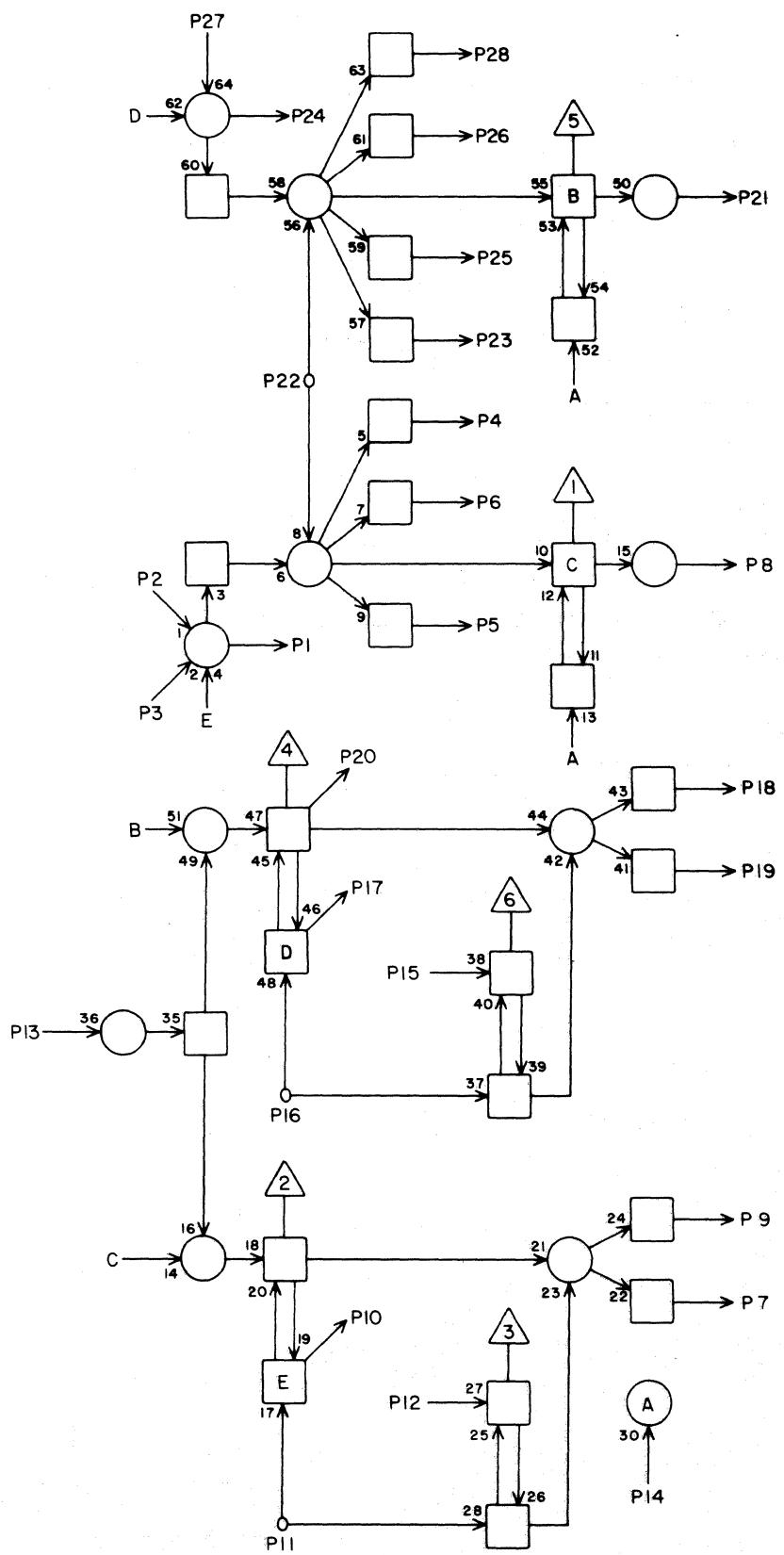
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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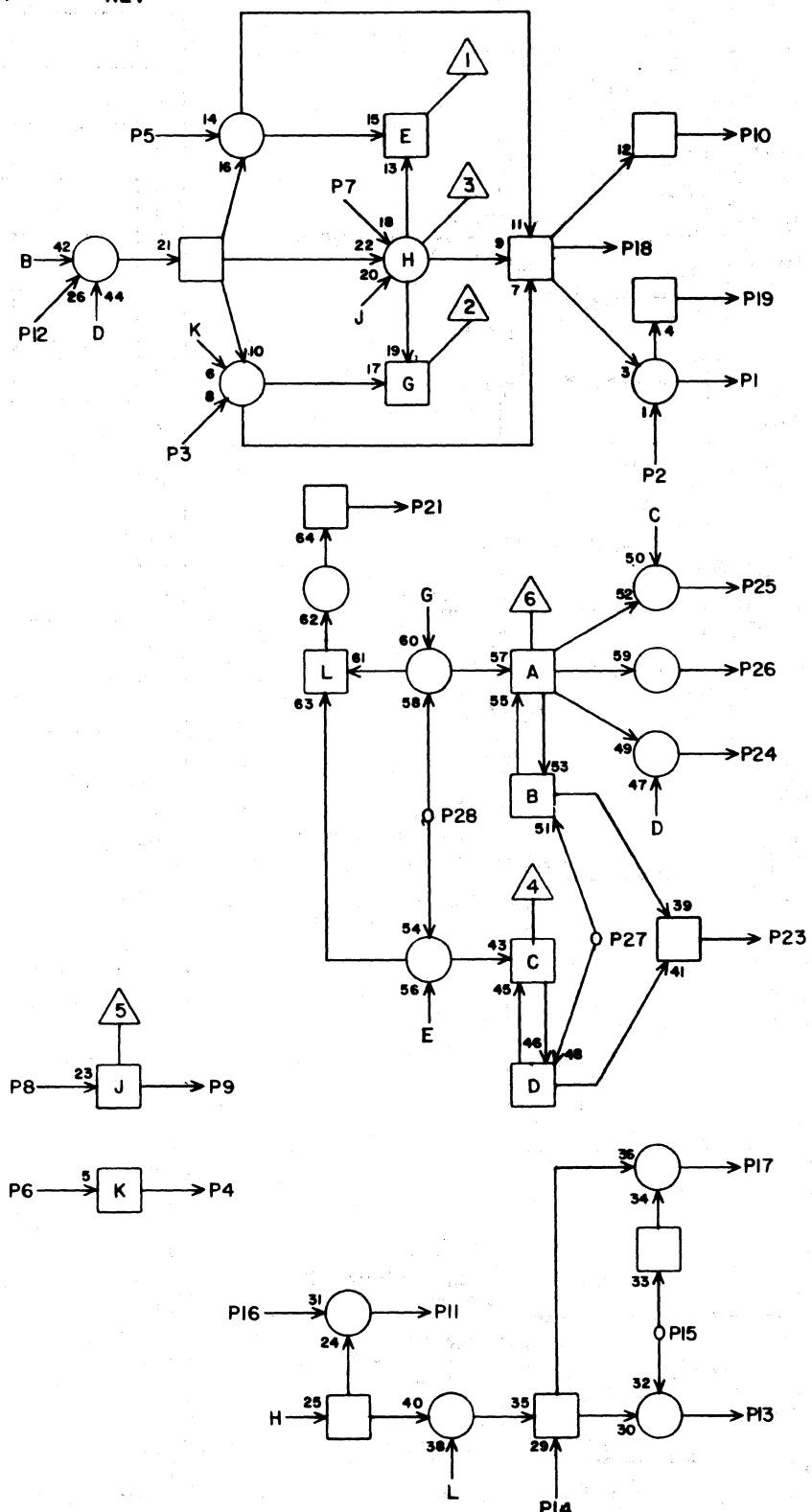
JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

LS 63045500
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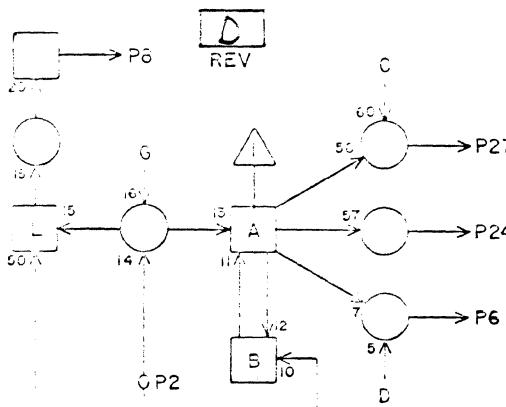
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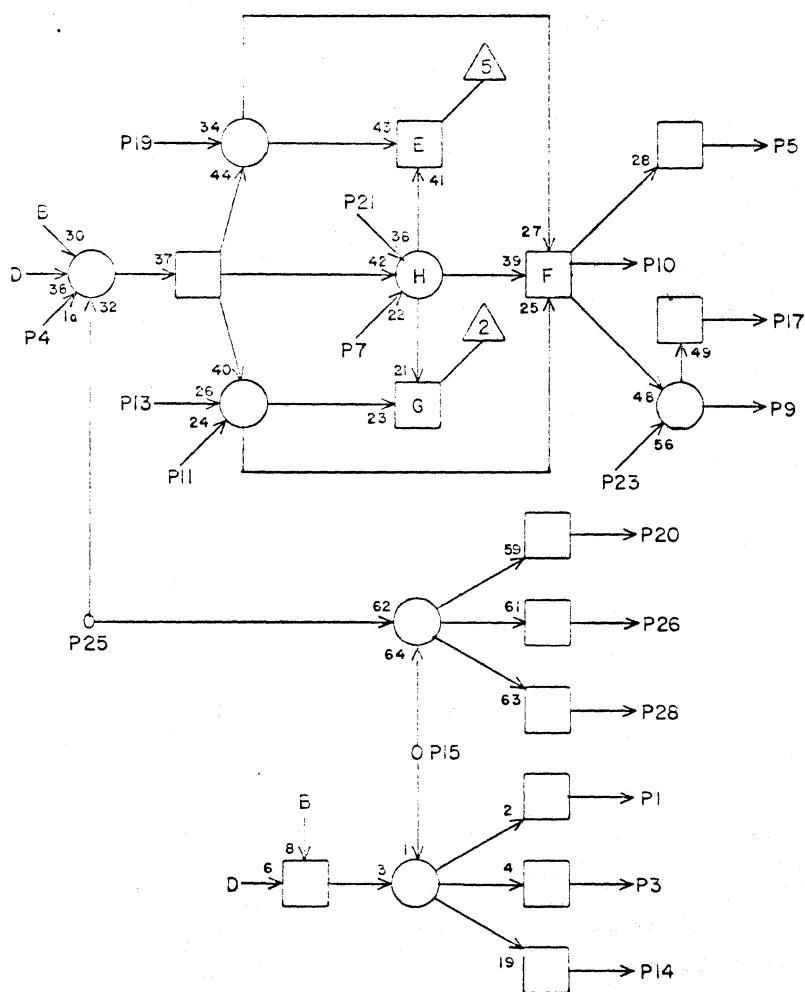
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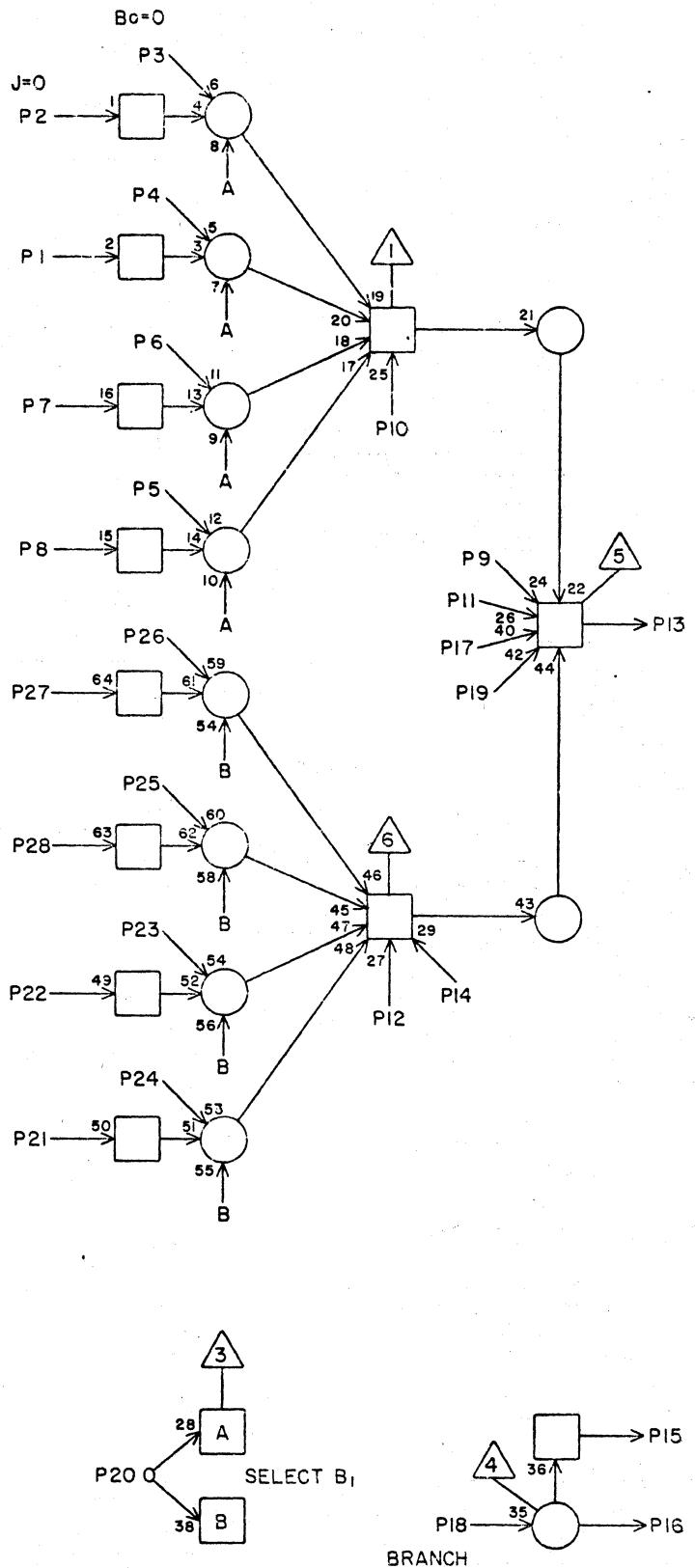
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

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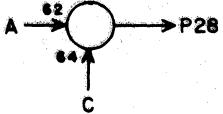
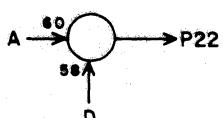
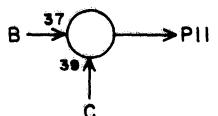
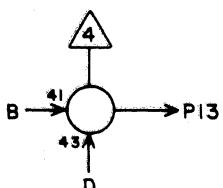
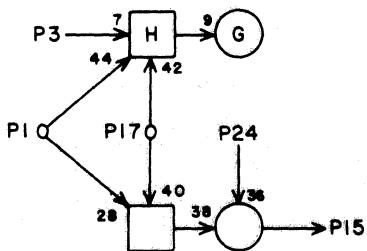
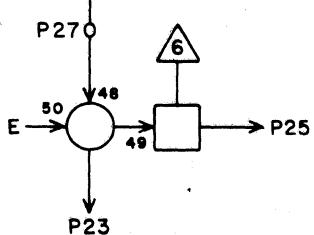
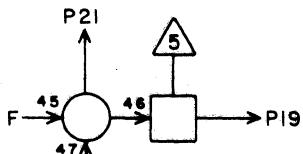
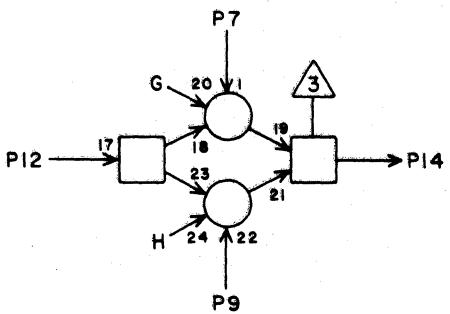
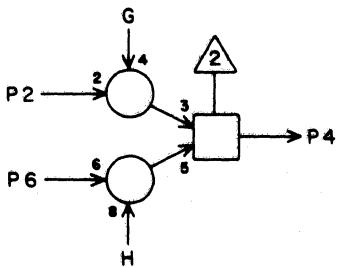
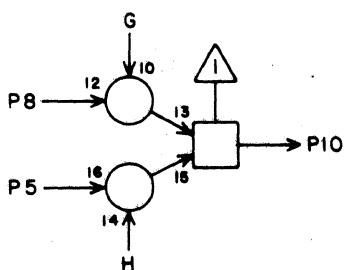
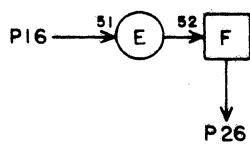
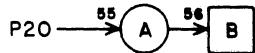
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CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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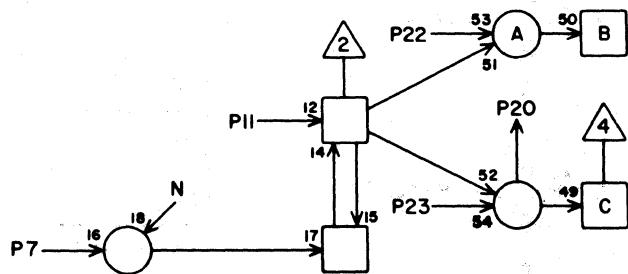
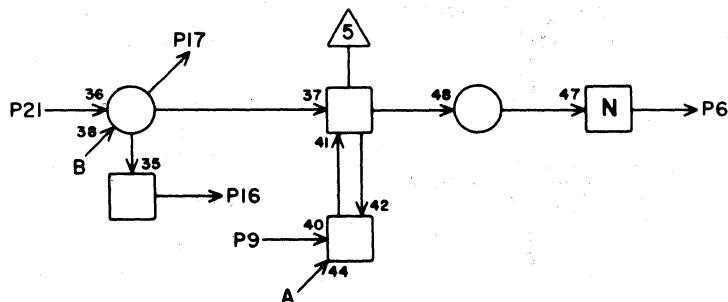
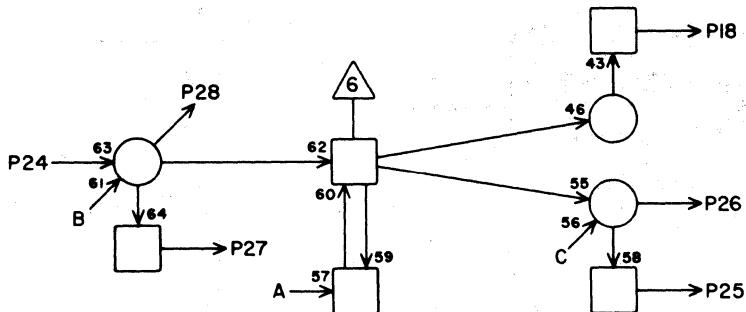
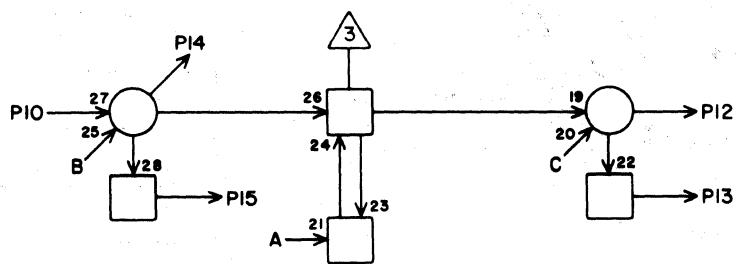
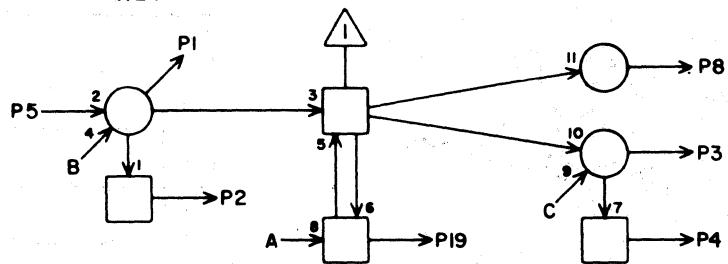
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CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

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CIRCUIT SPECIFICATION 11827600

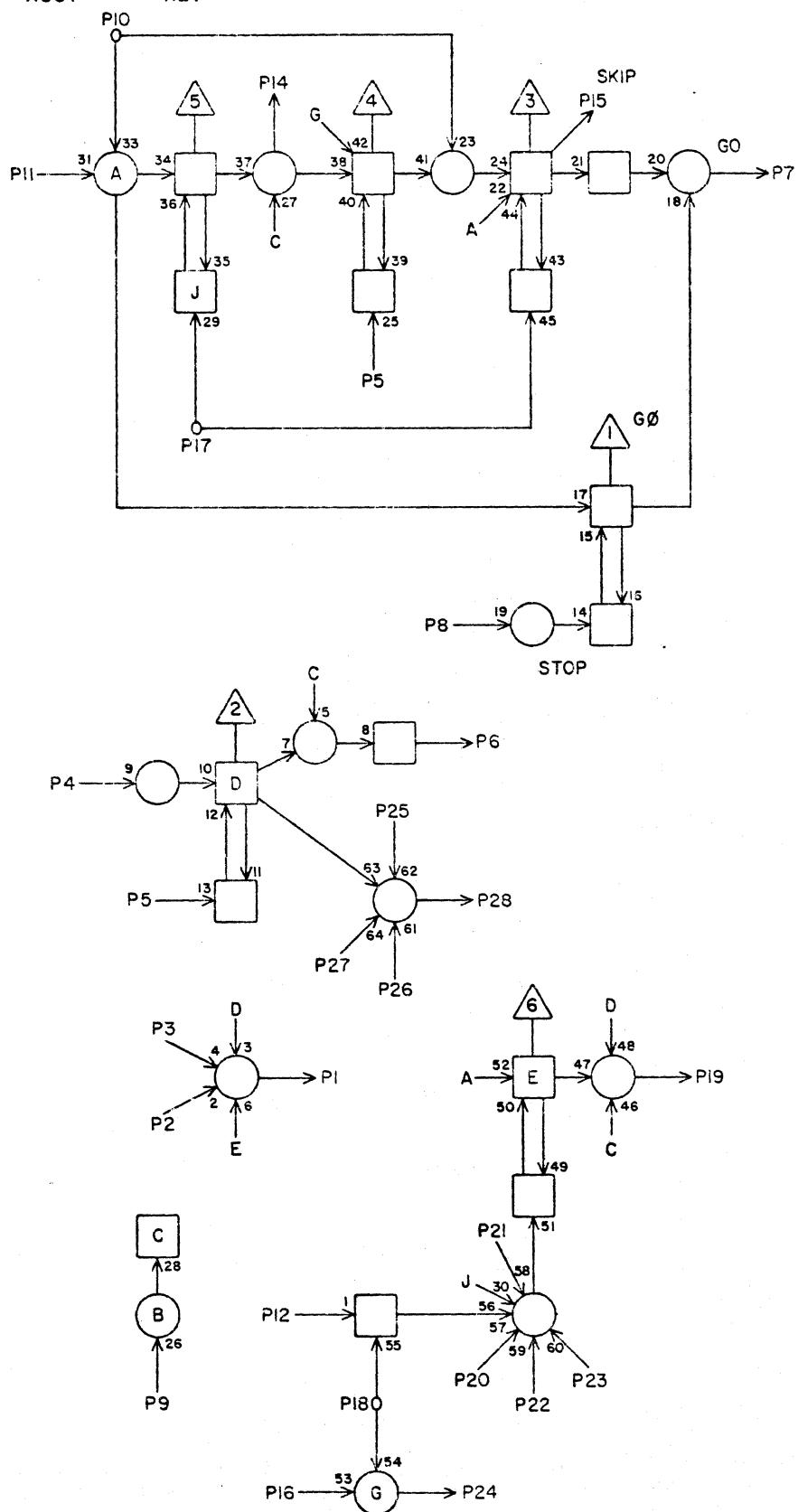
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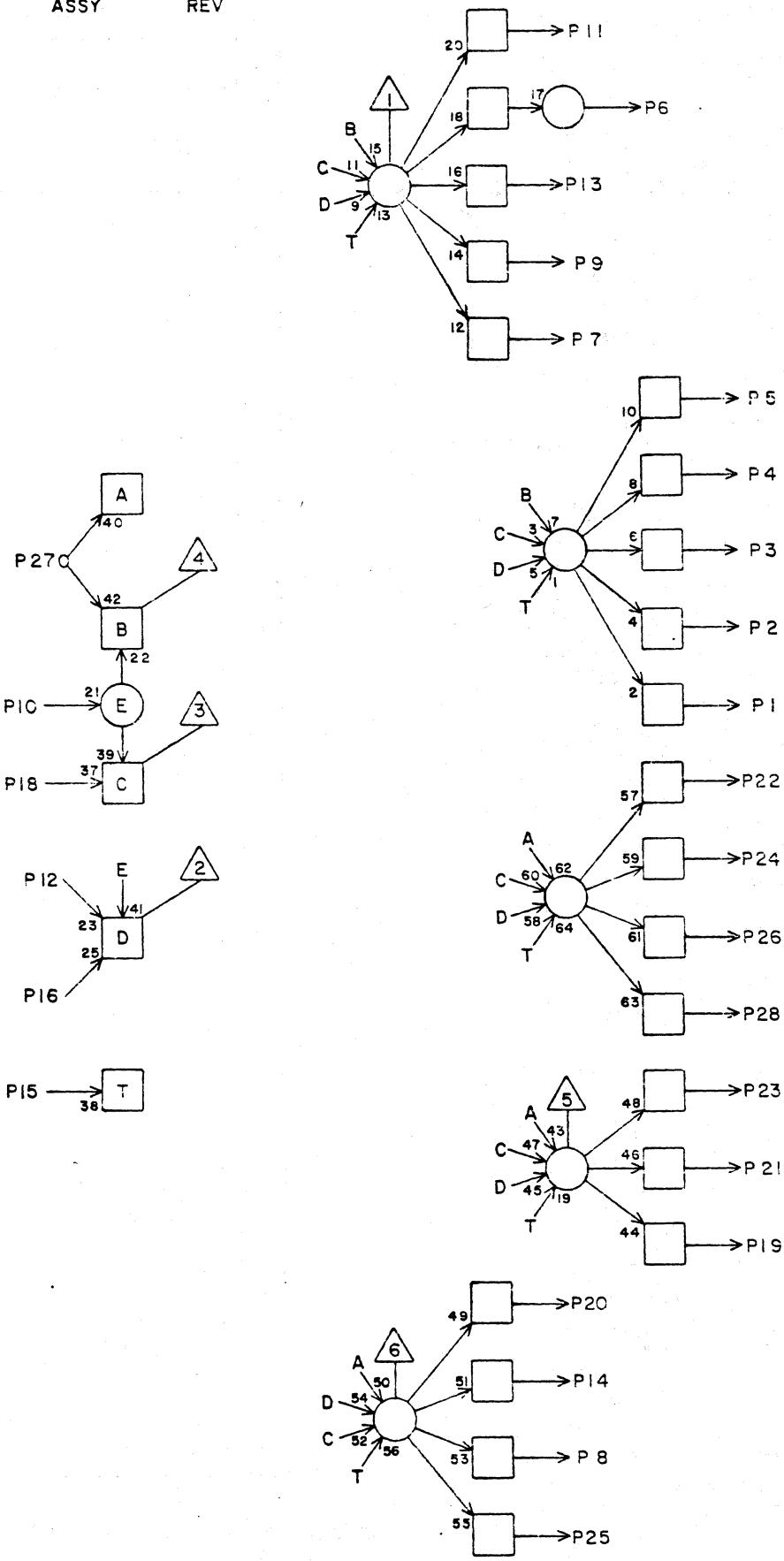
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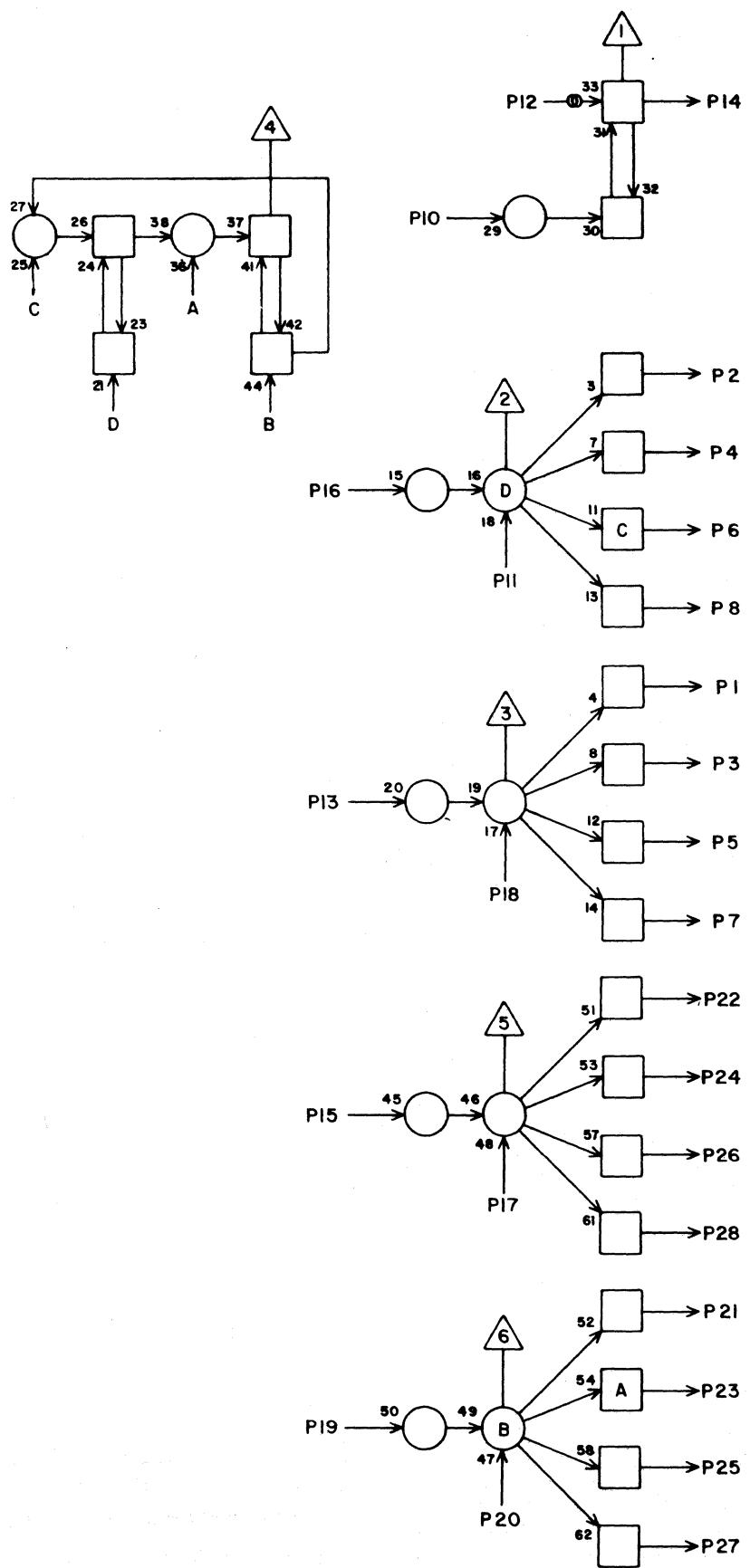
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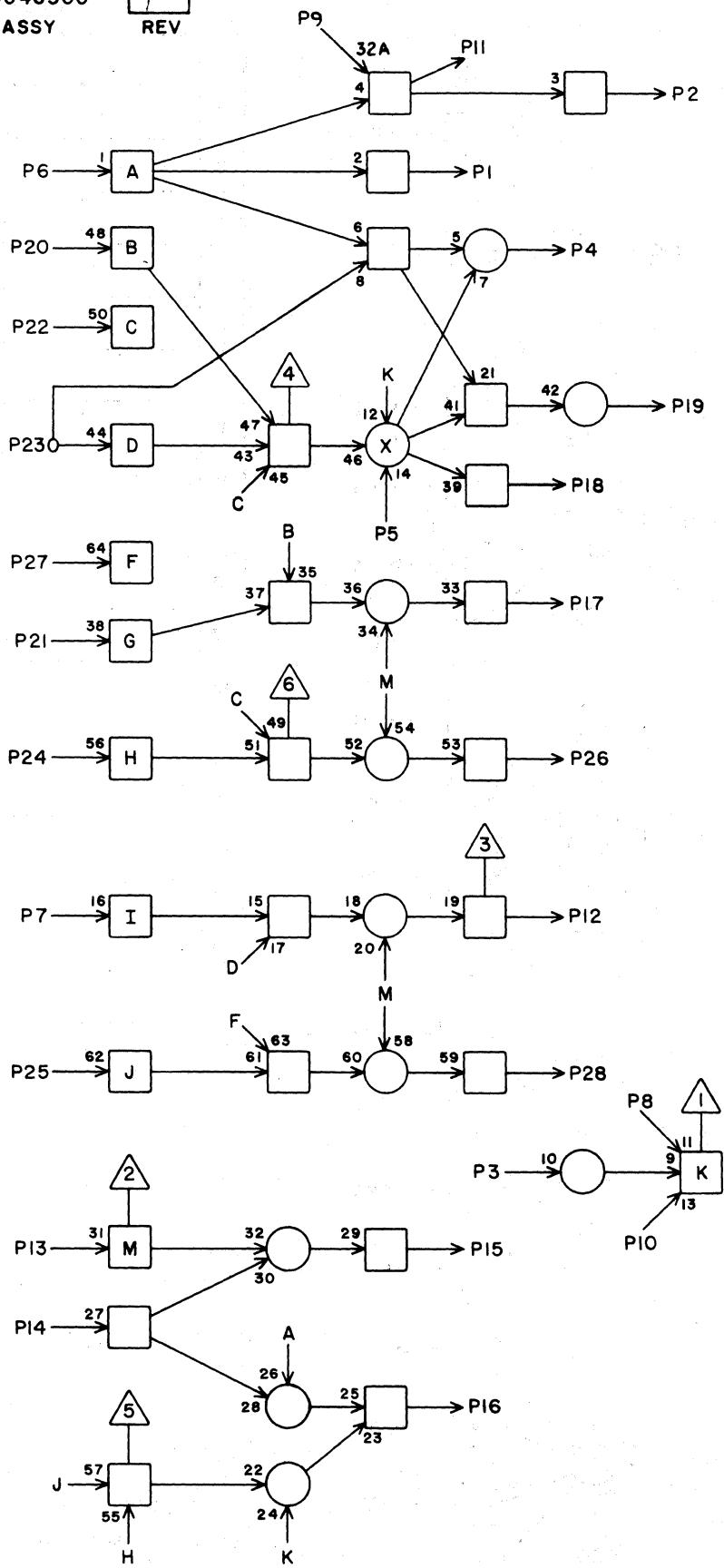
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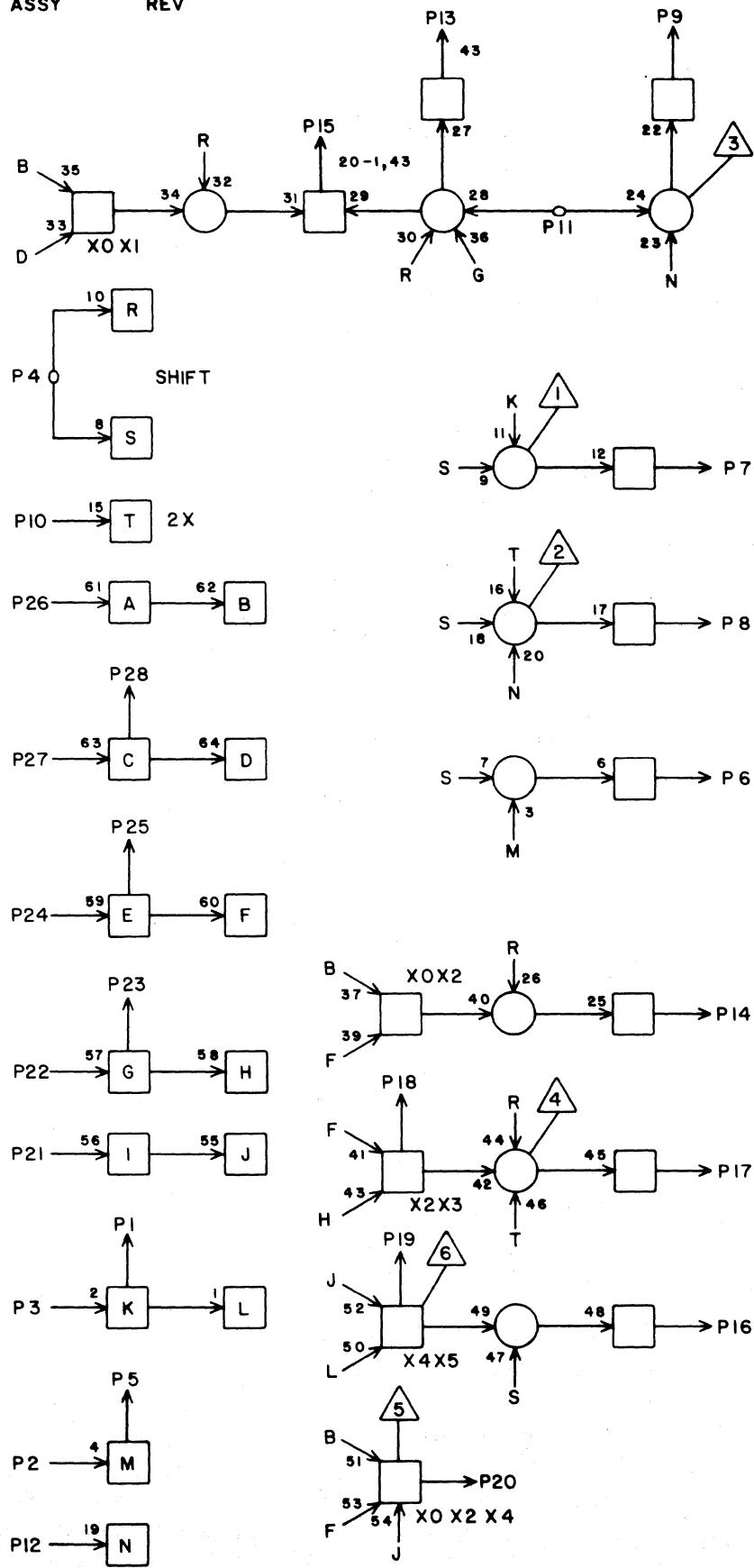
CIRCUIT SPECIFICATION 11827600

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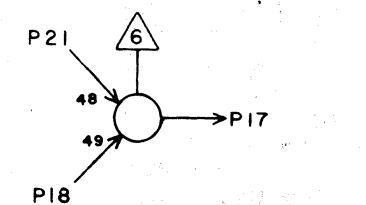
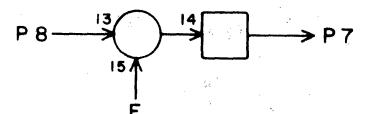
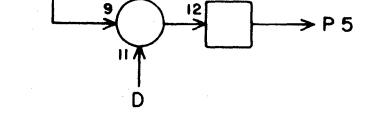
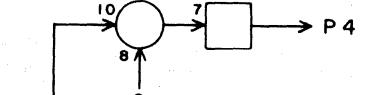
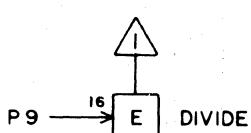
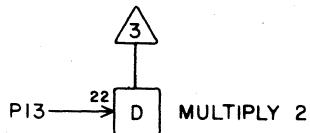
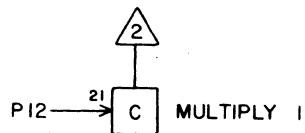
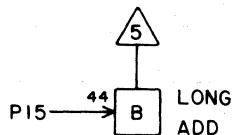
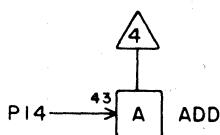
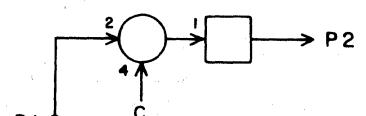
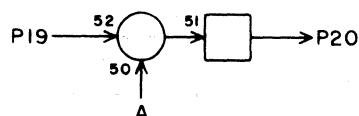
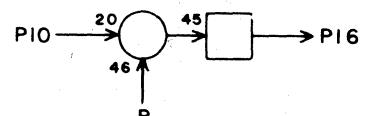
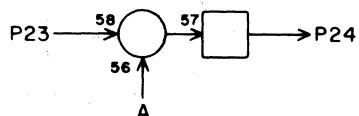
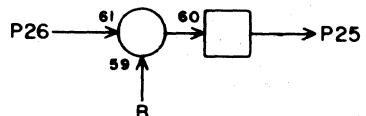
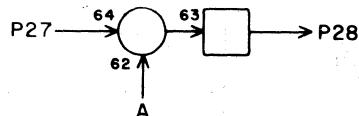
CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

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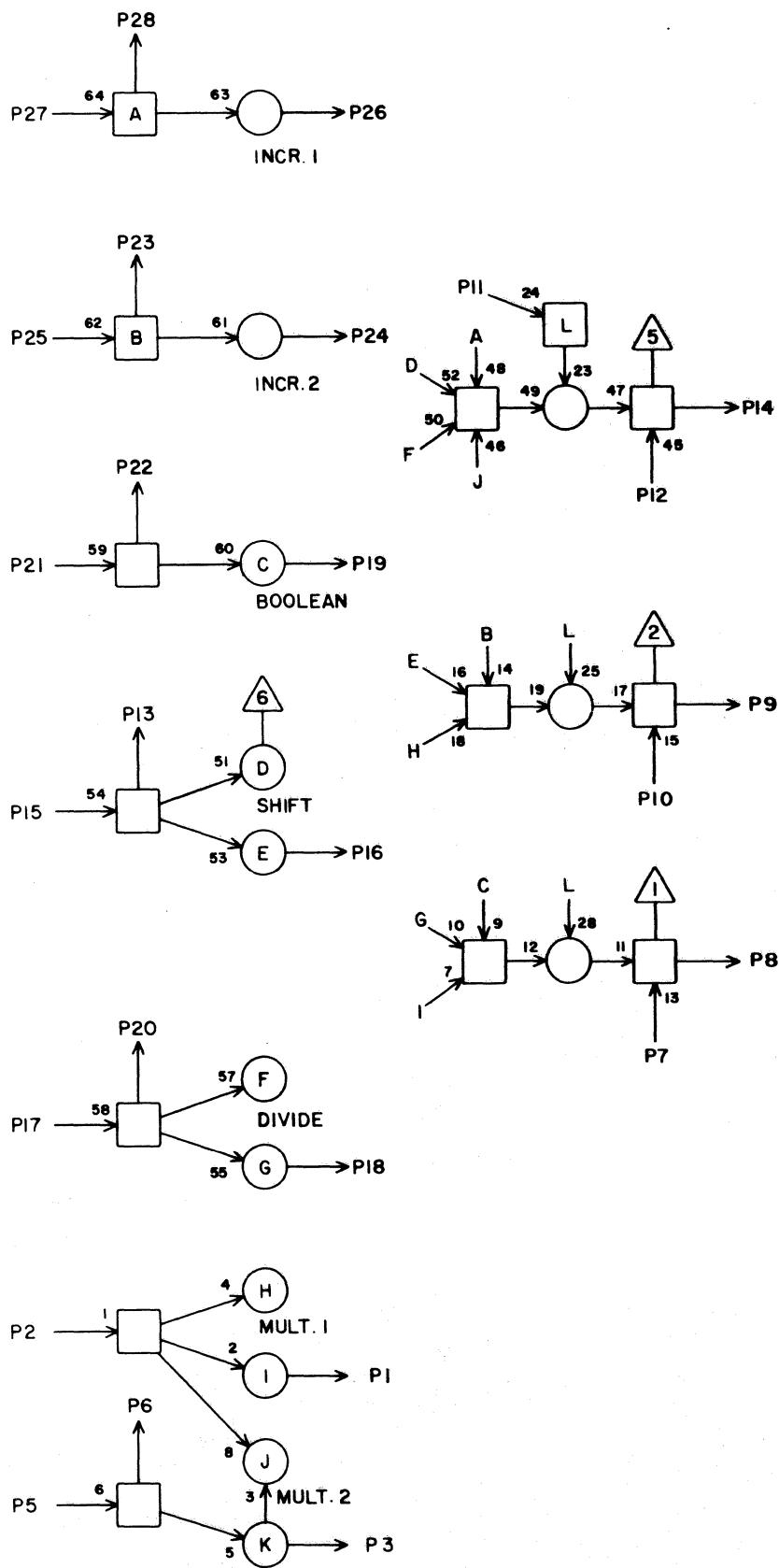
JACK PIN LG

CIRCUIT SPECIFICATION 11827600
60042700 Rev. J

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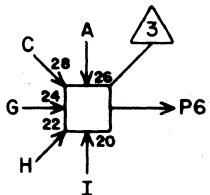
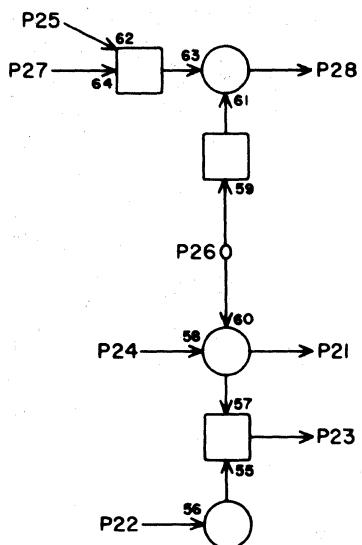
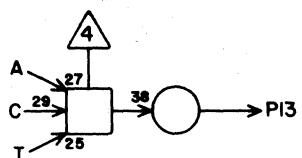
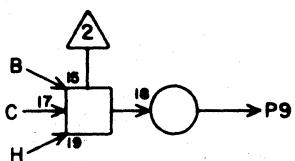
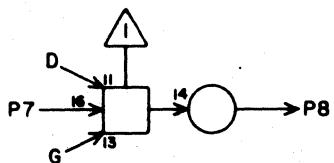
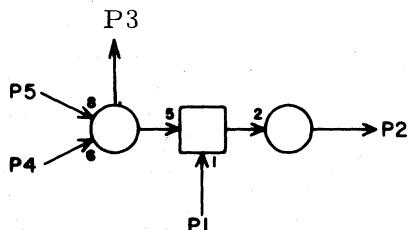
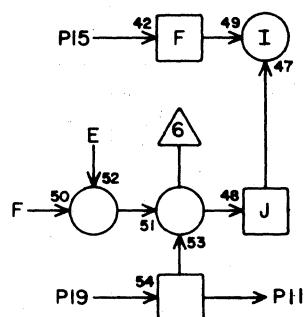
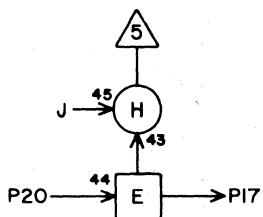
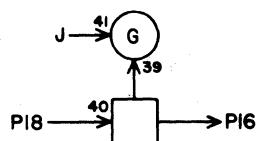
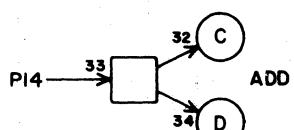
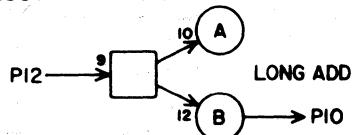
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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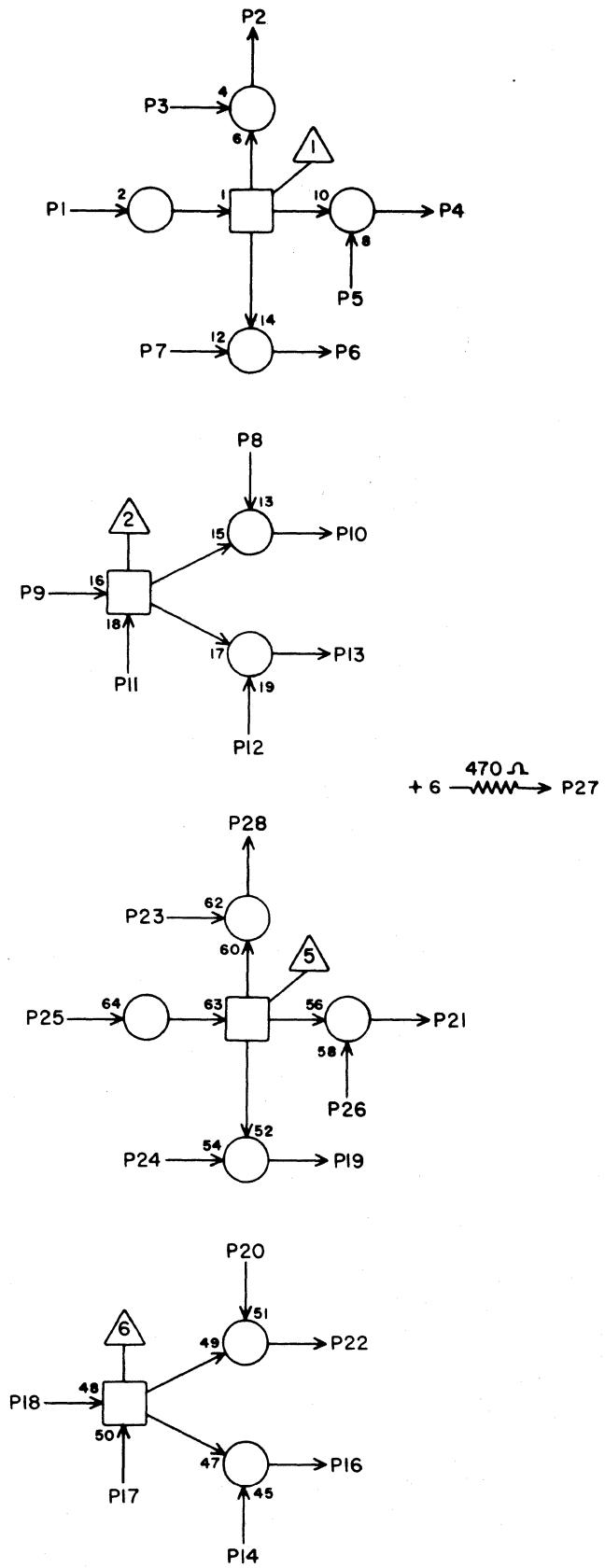
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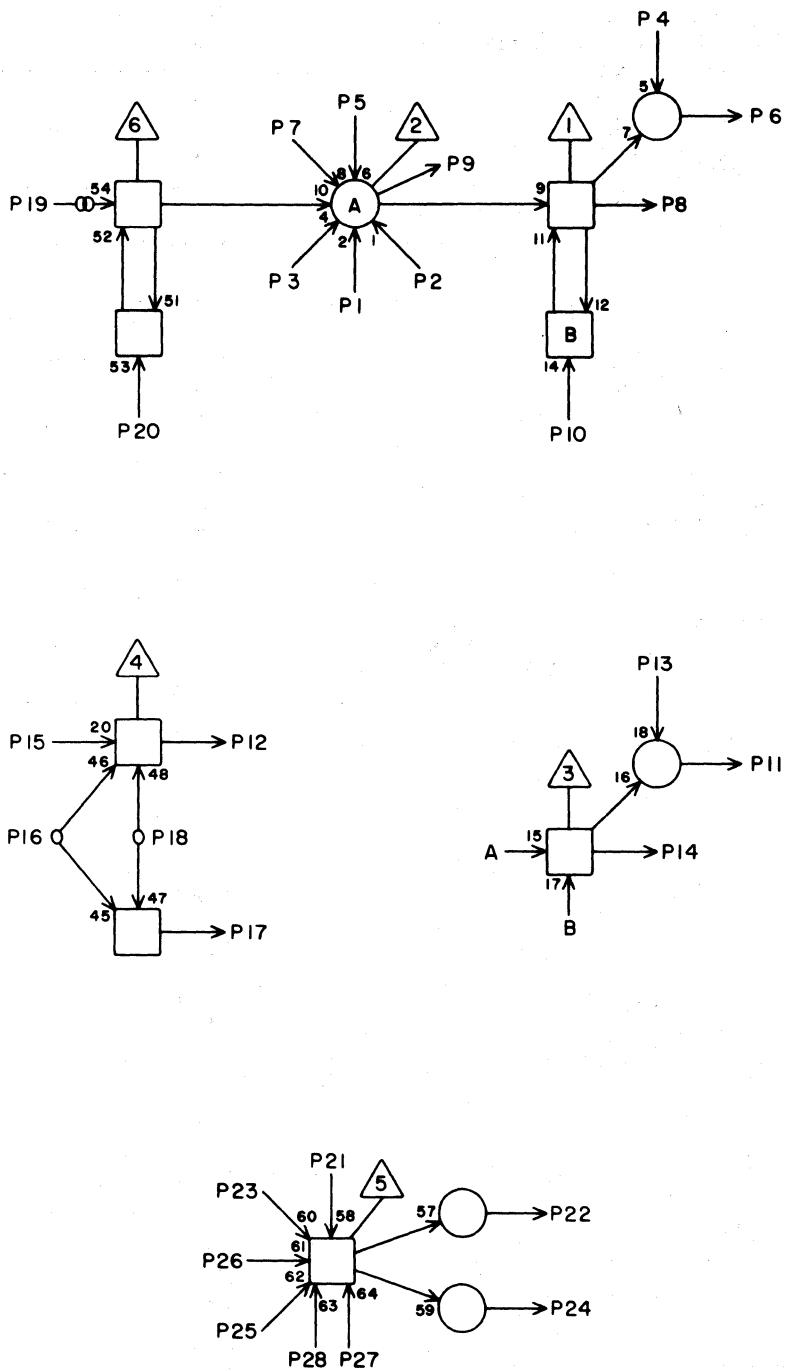
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60042700 Rev. J

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60042700 Rev. J

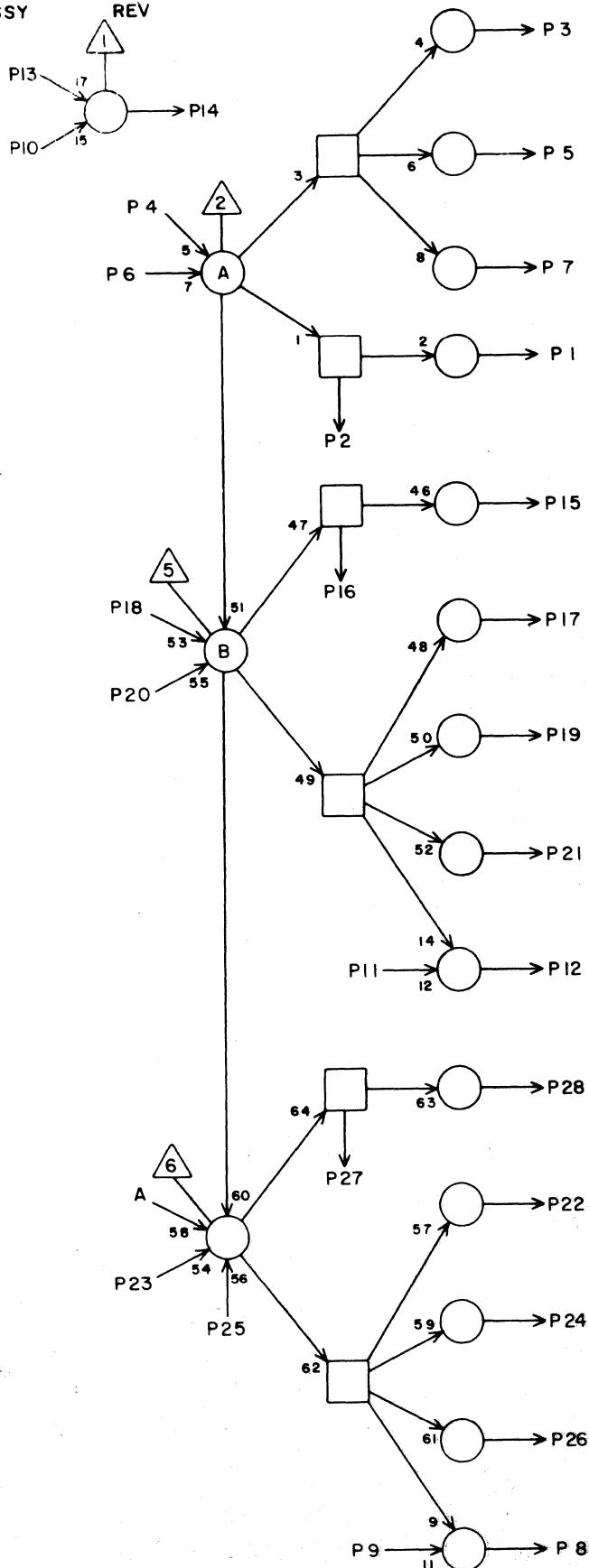
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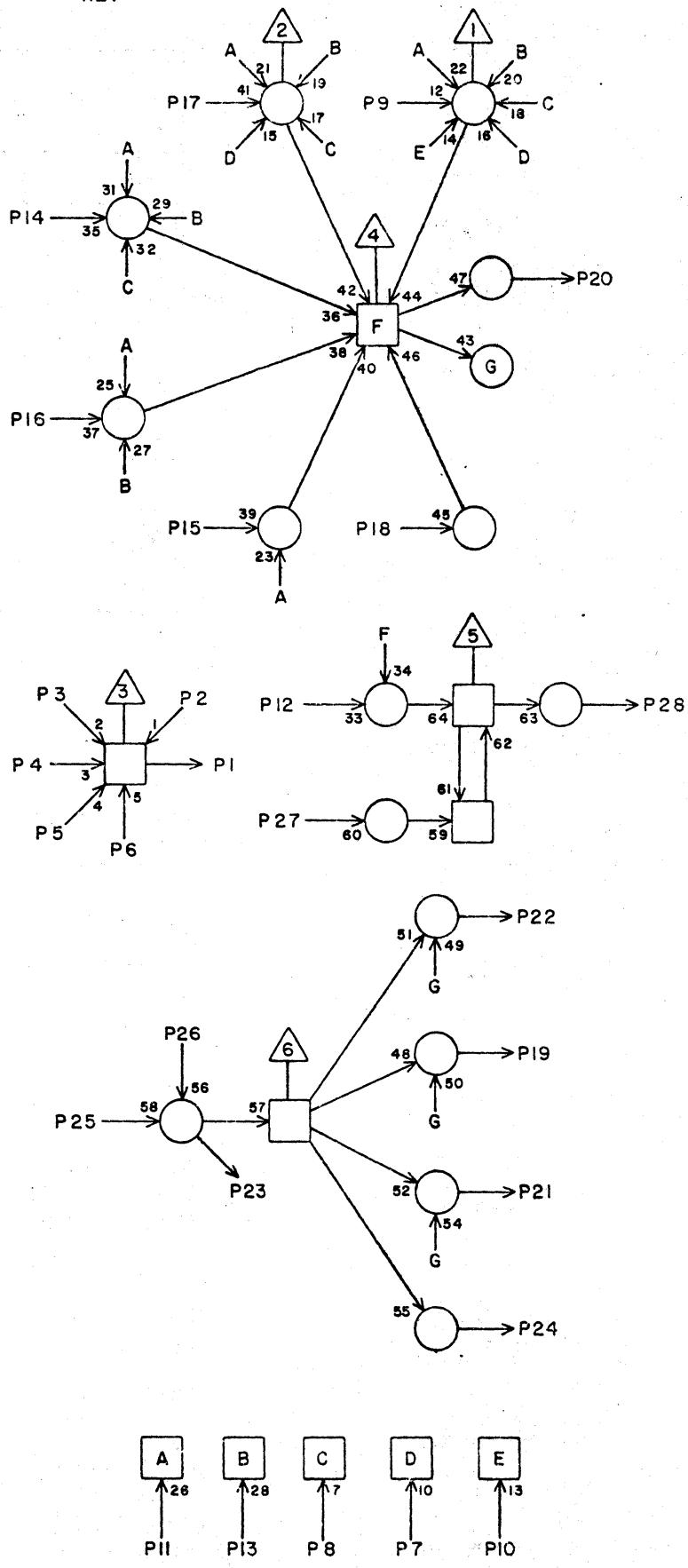
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CIRCUIT SPECIFICATION 11827600
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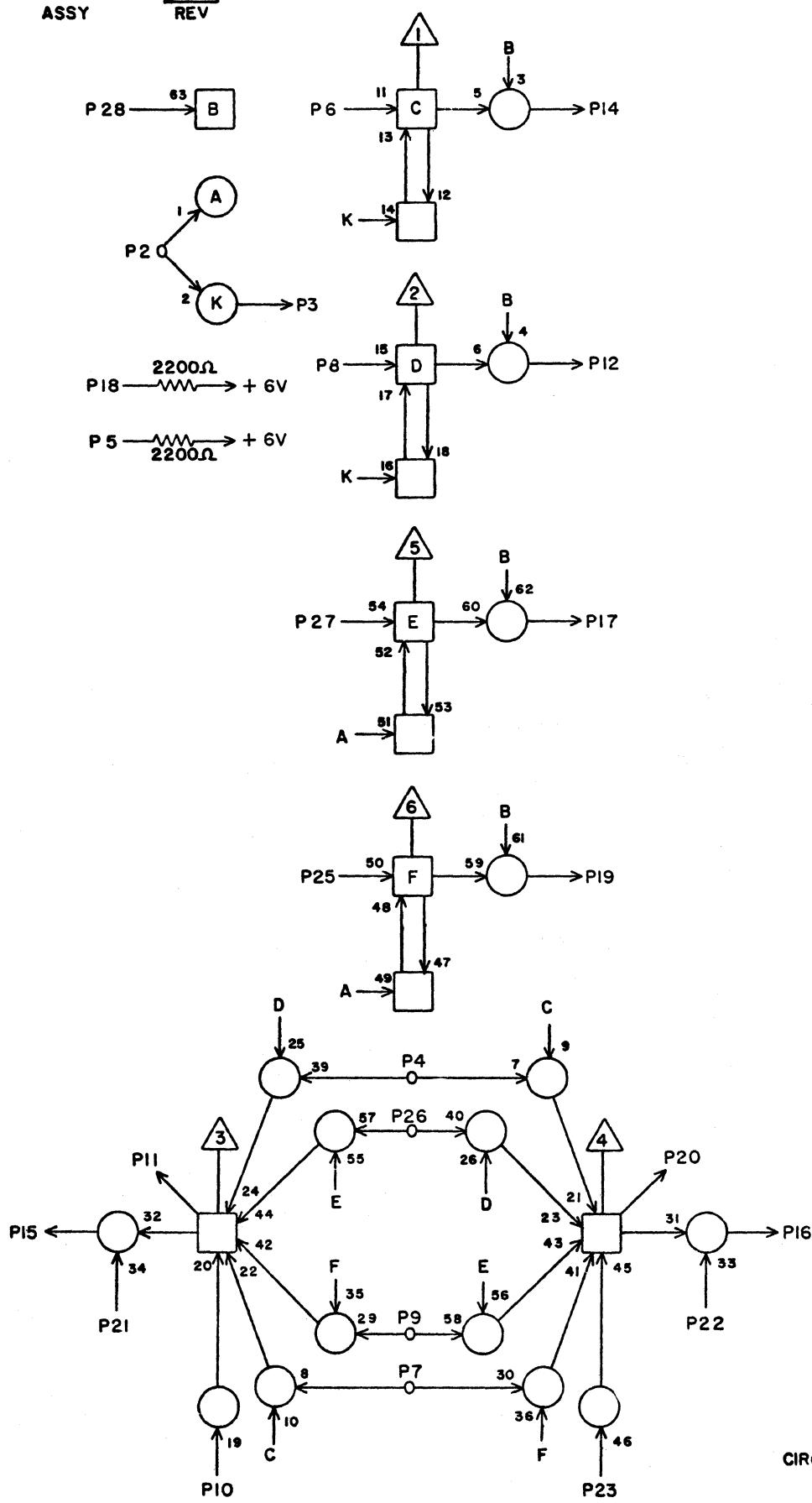
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CIRCUIT SPECIFICATION 11827600

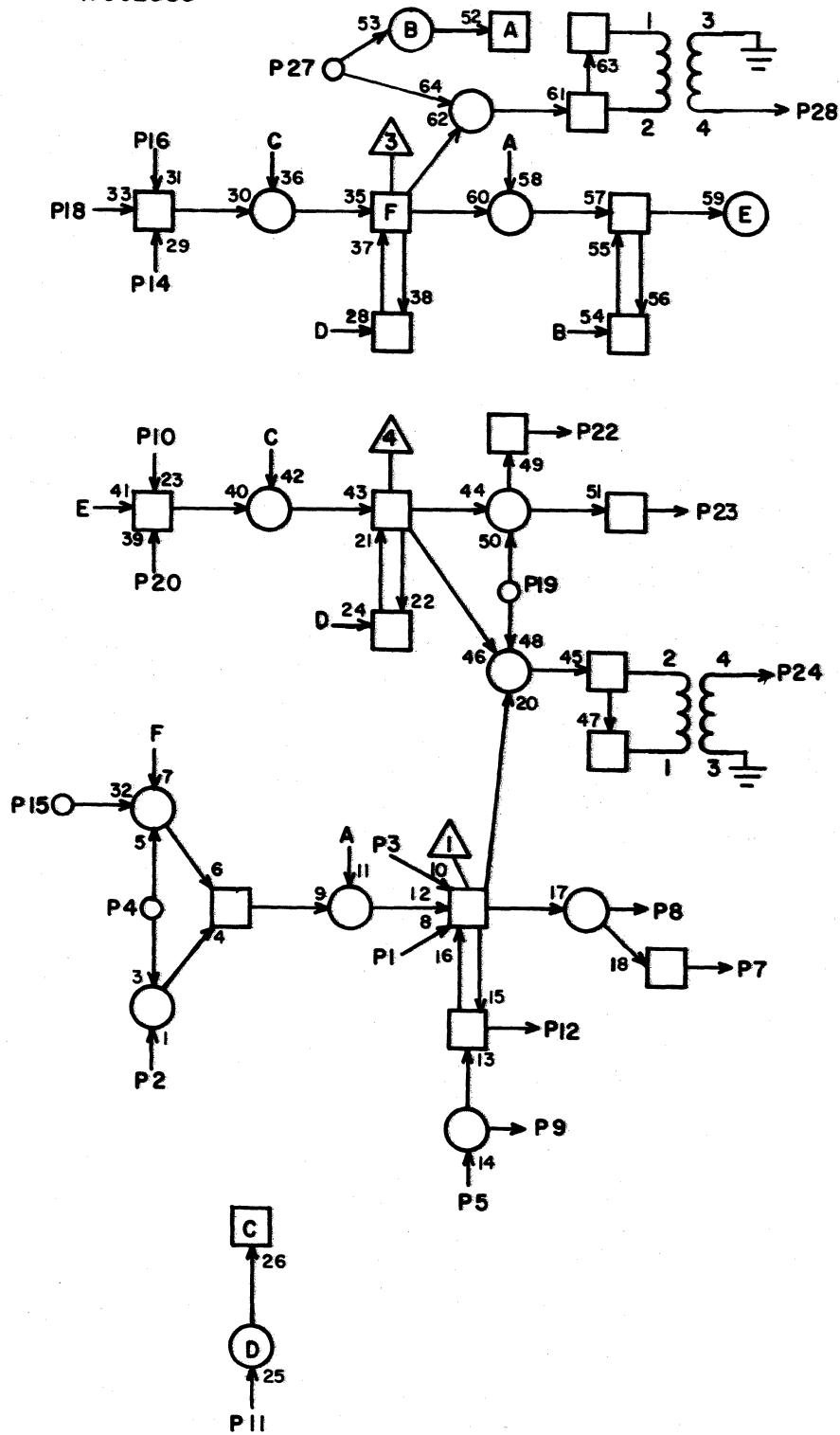
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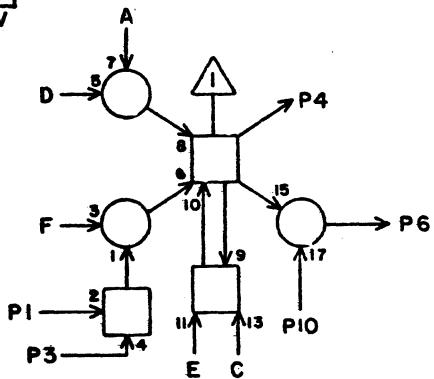
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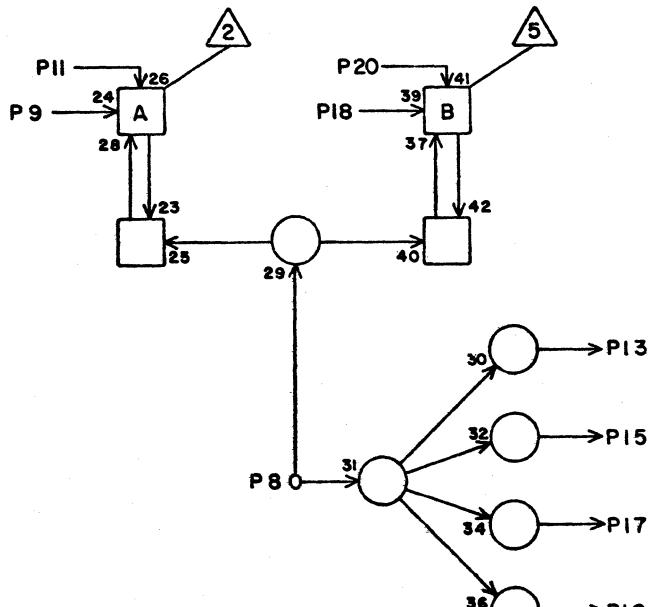
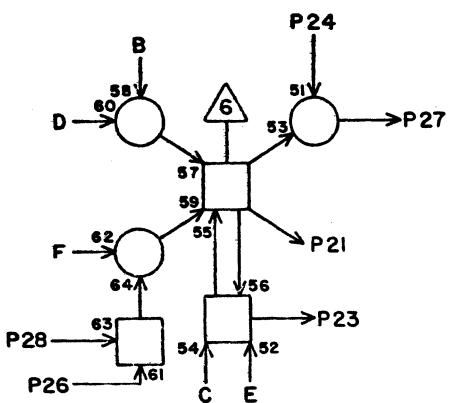
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JACK PIN LG

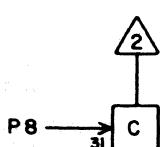
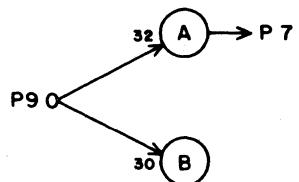
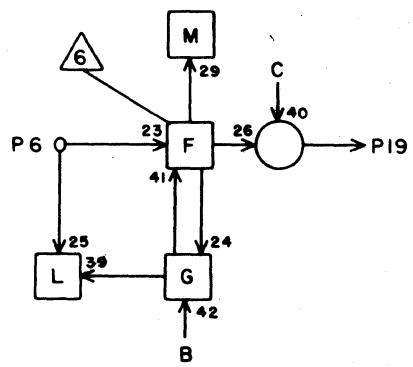
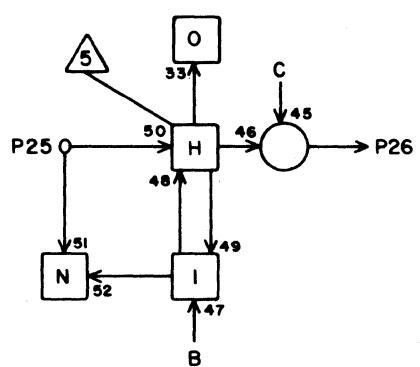
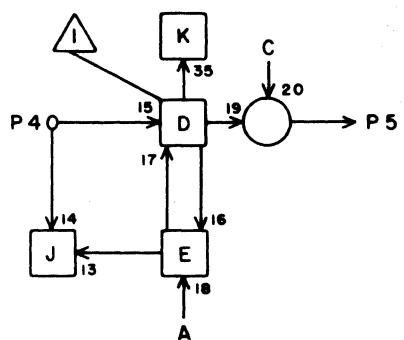
CIRCUIT SPECIFICATION 11827600

60042700 Rev J

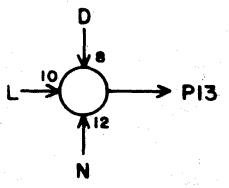
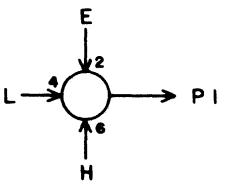
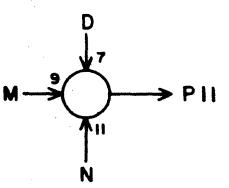
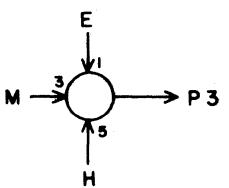
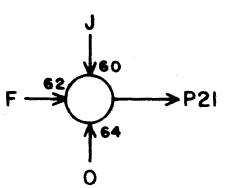
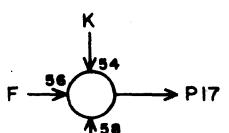
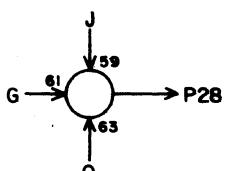
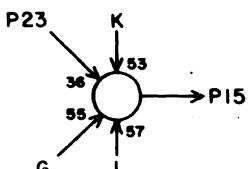


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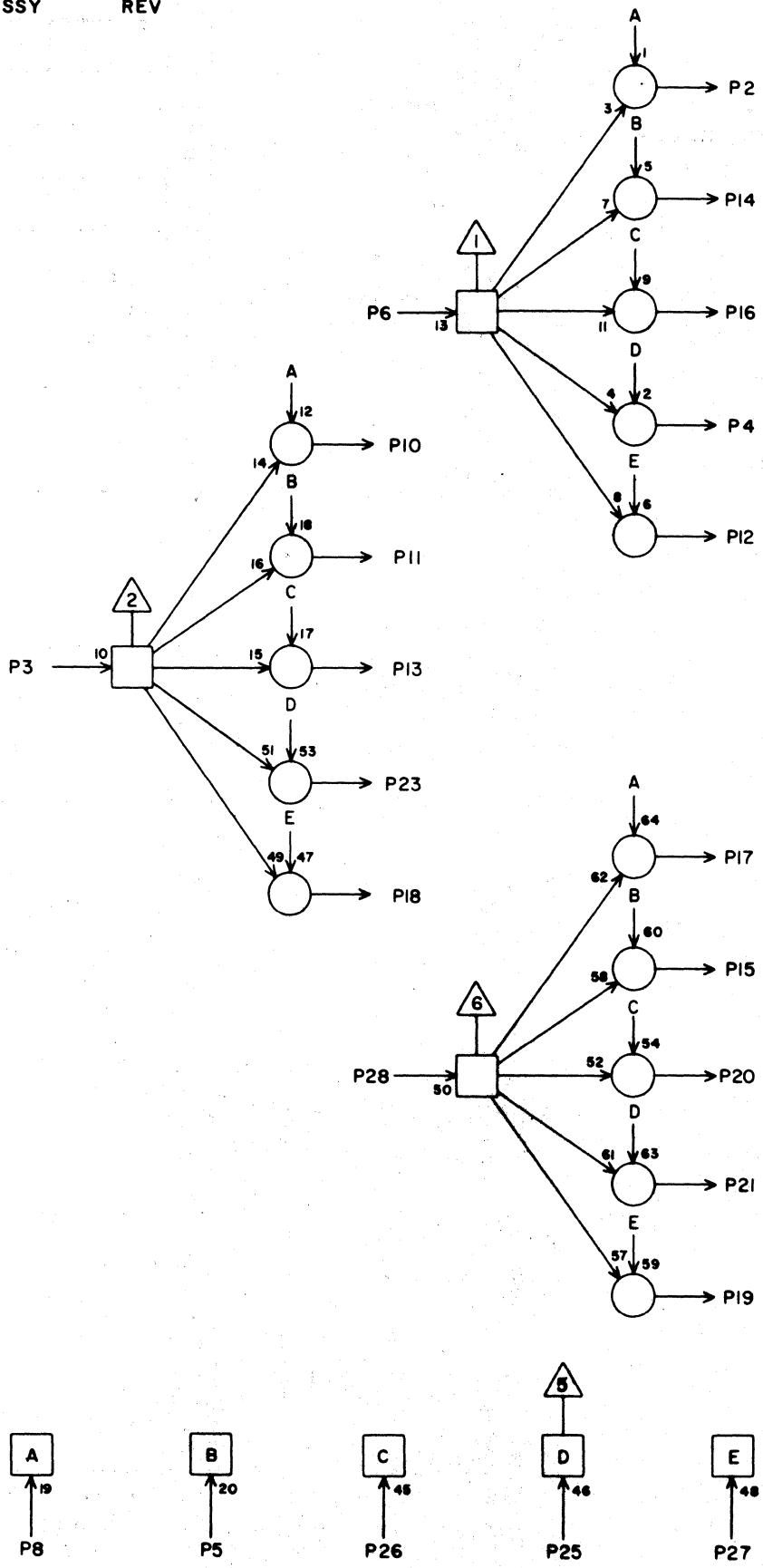
CIRCUIT SPECIFICATION II827600

60042700 Rev. J

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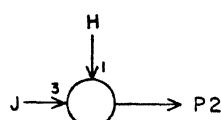
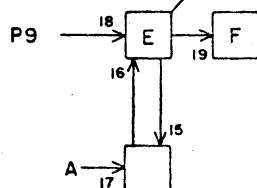
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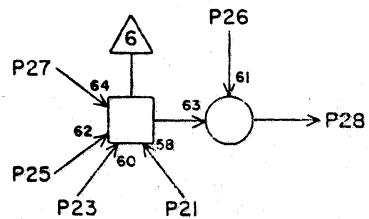
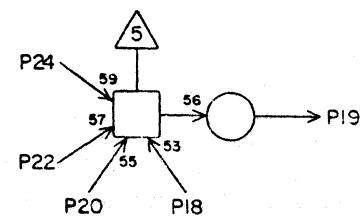
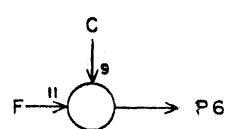
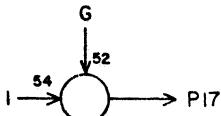
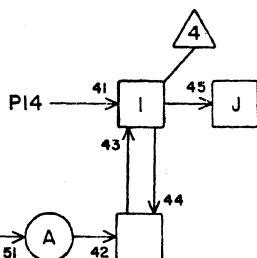
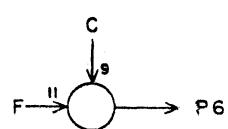
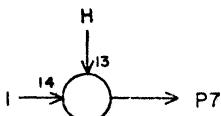
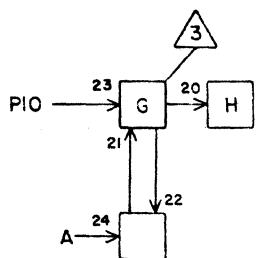
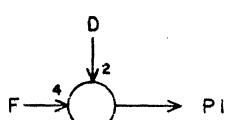
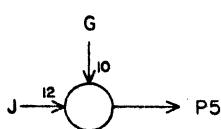
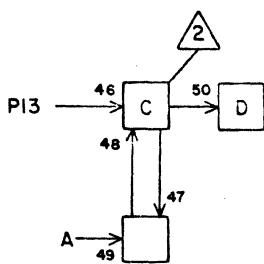
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CIRCUIT SPECIFICATION 11827600

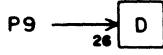
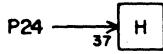
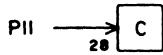
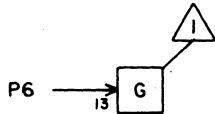
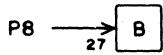
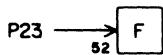
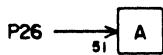
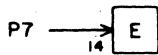
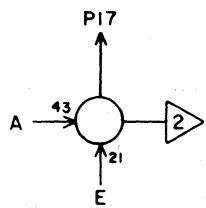
60042700 Rev J

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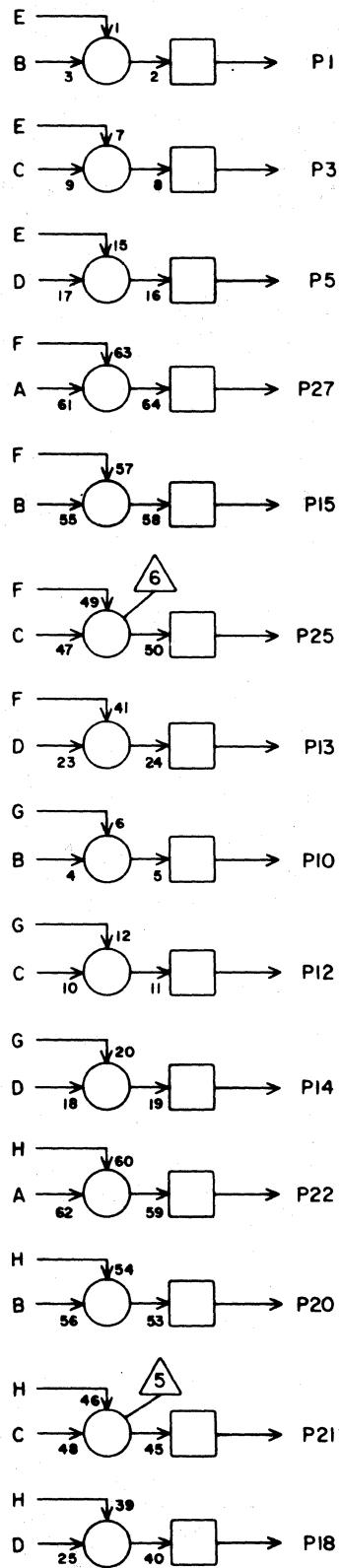
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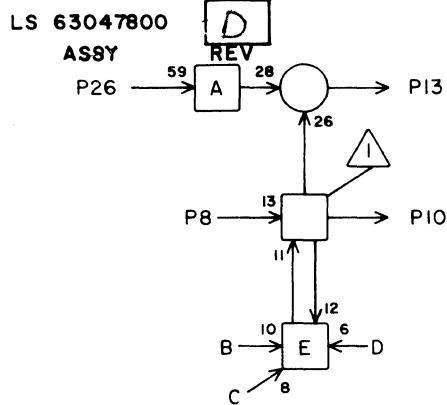
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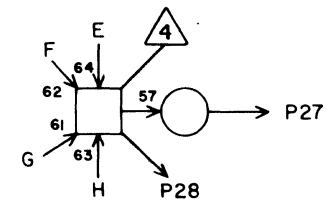
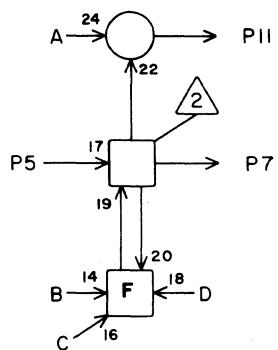
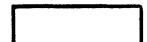
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CIRCUIT SPECIFICATION 11827600

60042700 Rev. J



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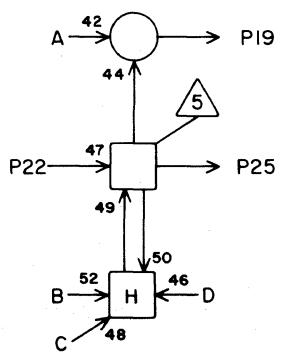
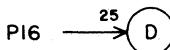
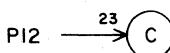
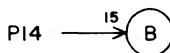
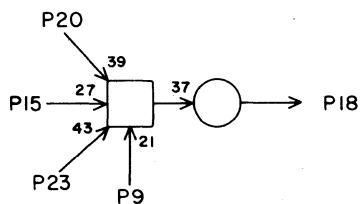
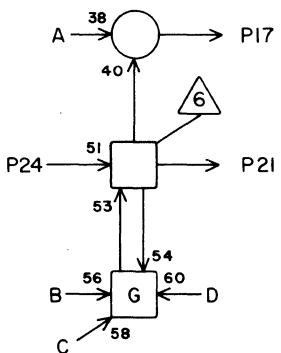


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CIRCUIT SPECIFICATION 11827600

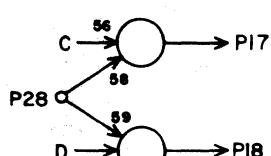
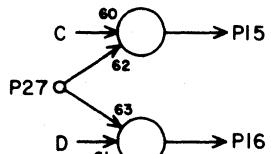
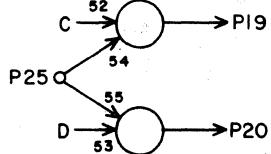
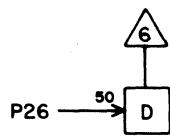
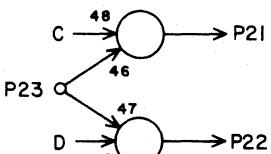
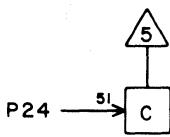
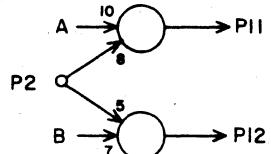
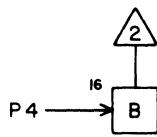
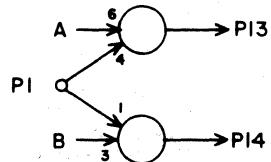
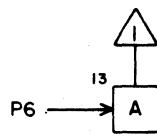
60042700 Rev. J



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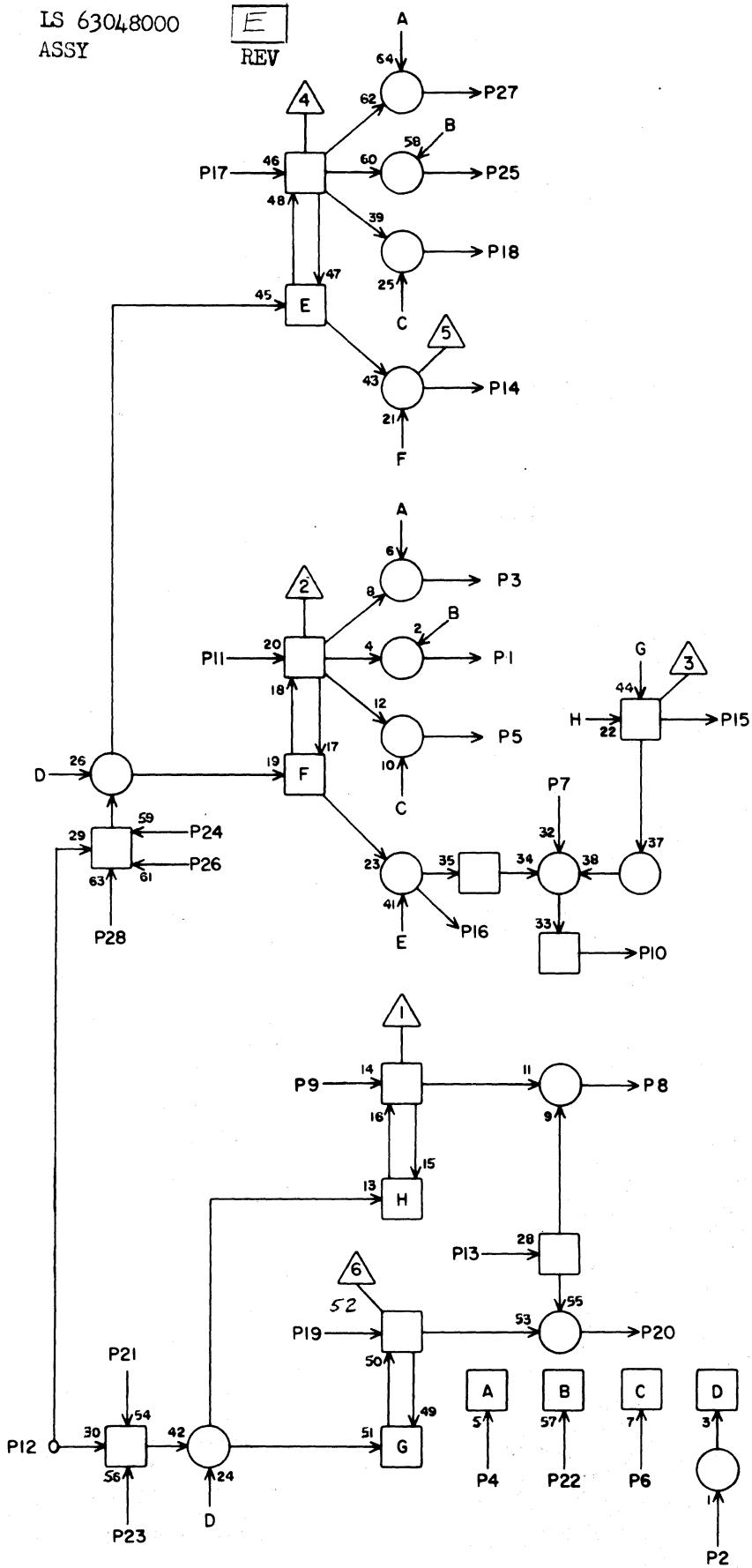
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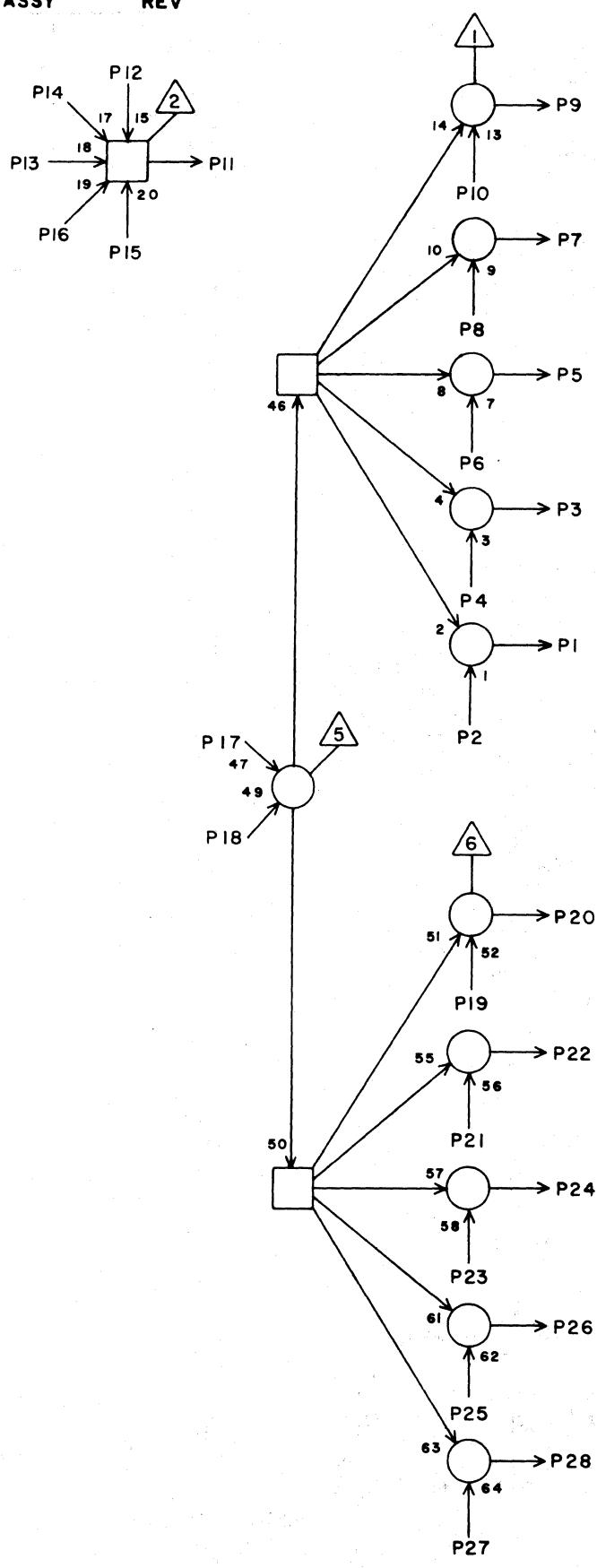


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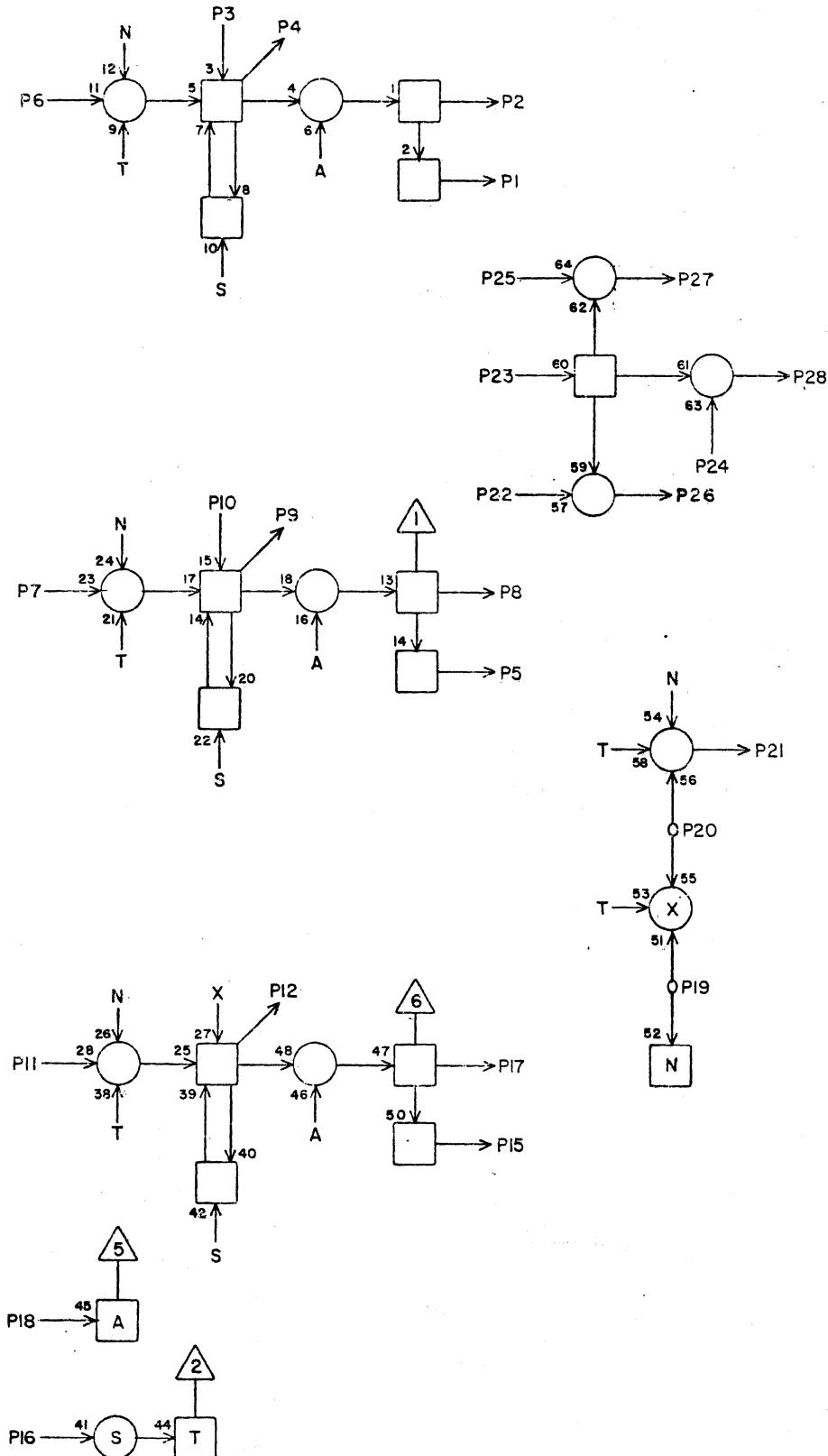
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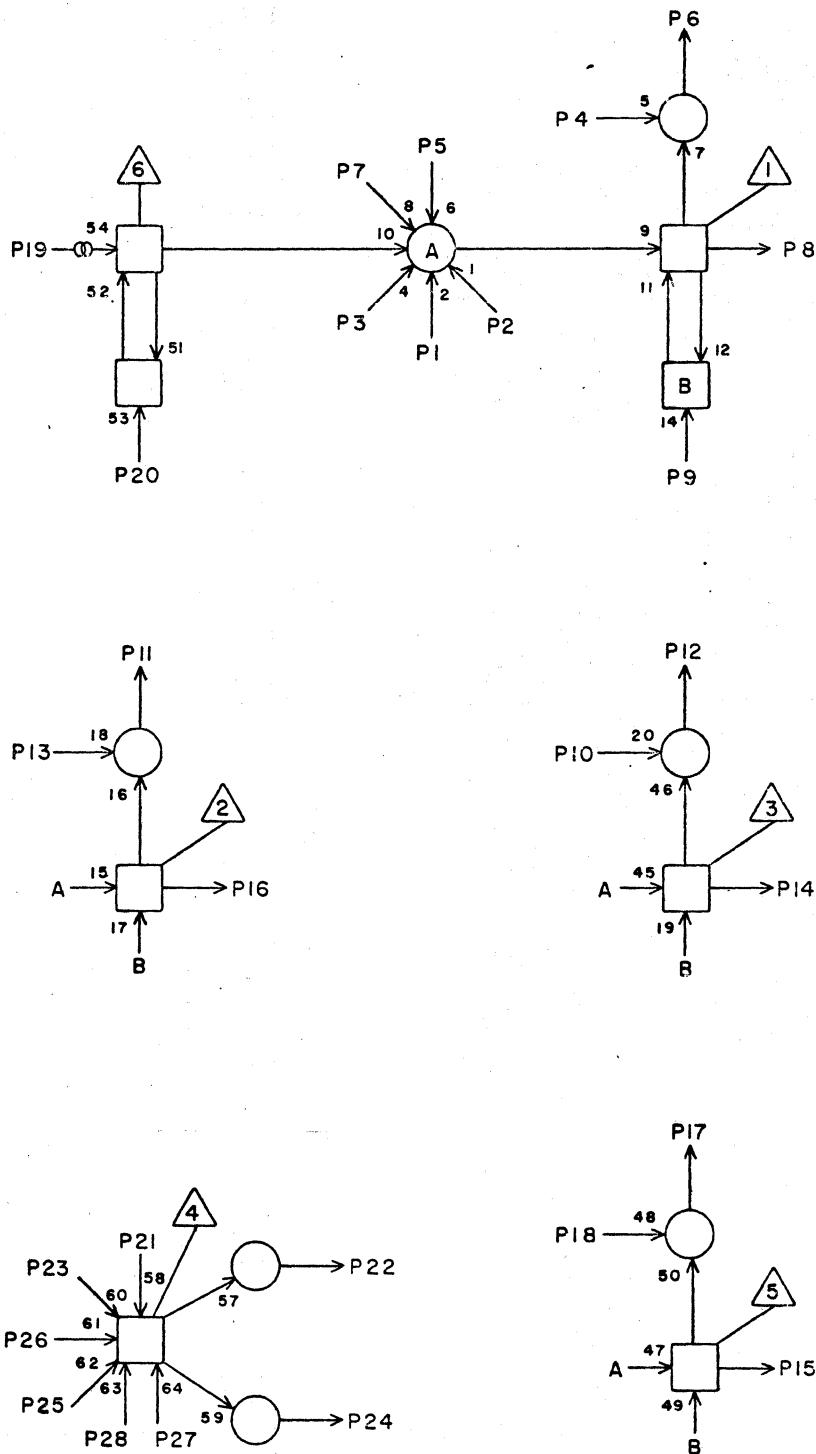
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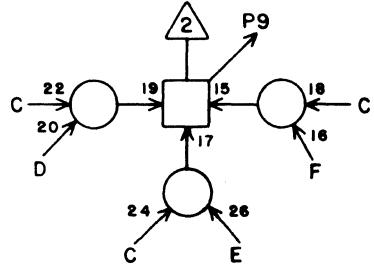
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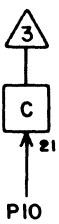
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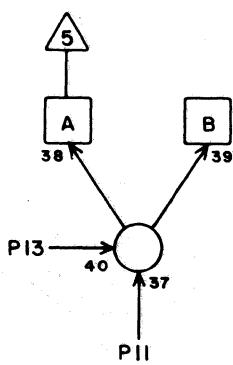
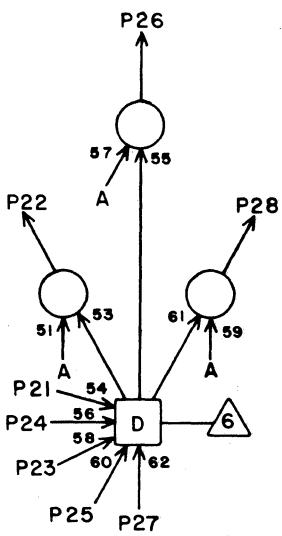
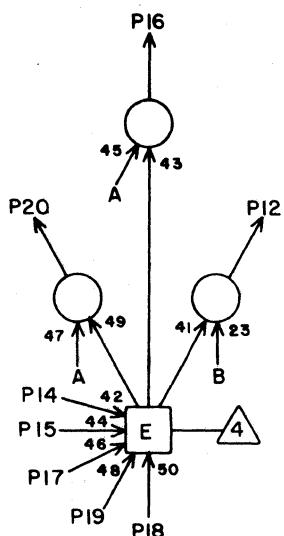
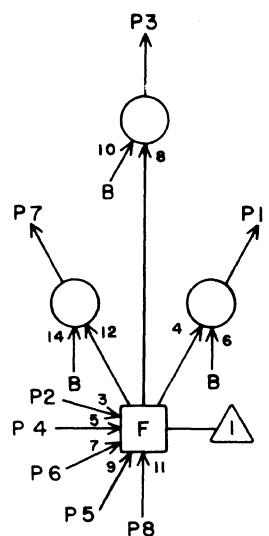
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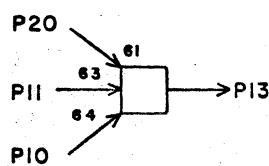
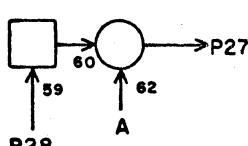
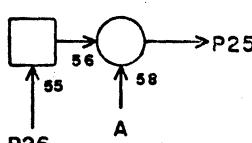
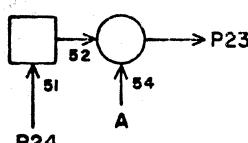
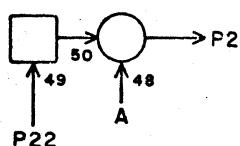
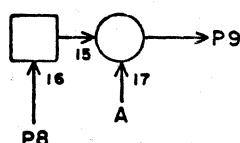
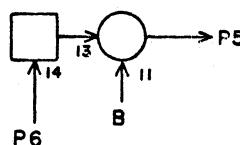
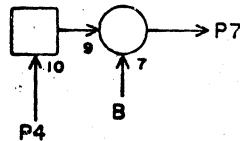
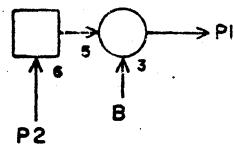
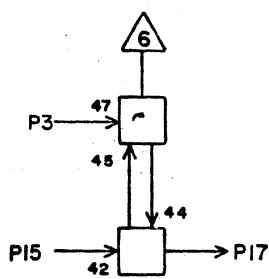
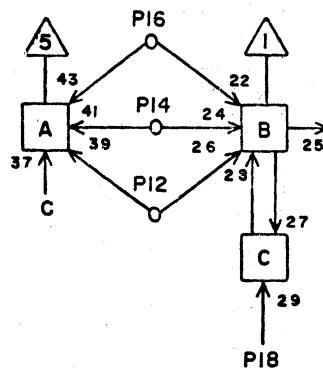


60042700 Rev. J

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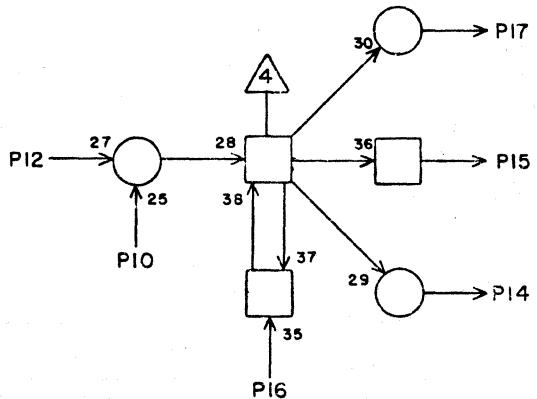
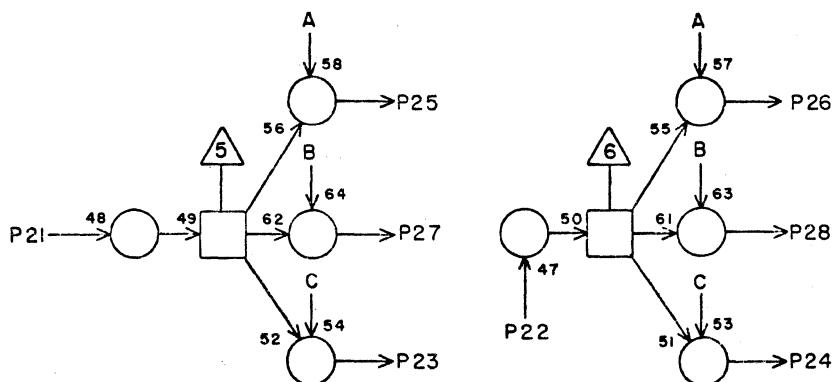
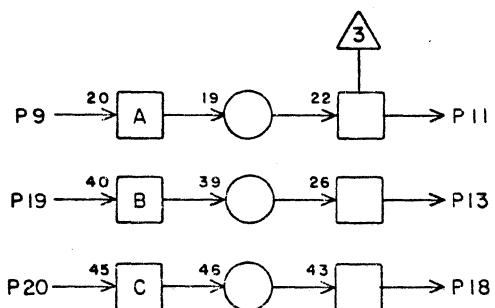
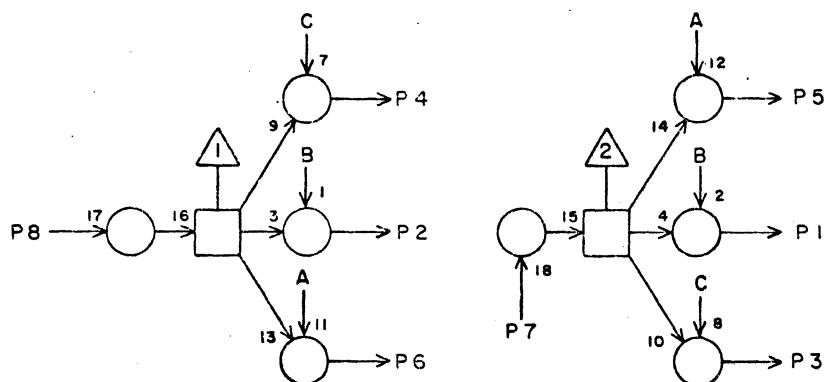


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CIRCUIT SPECIFICATION 11827600

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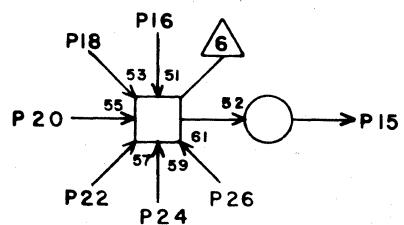
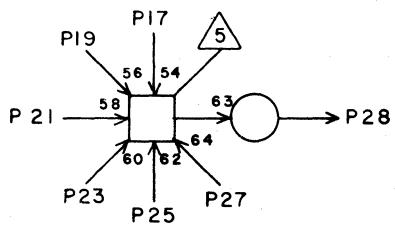
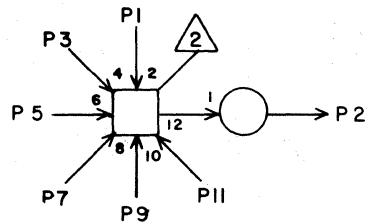
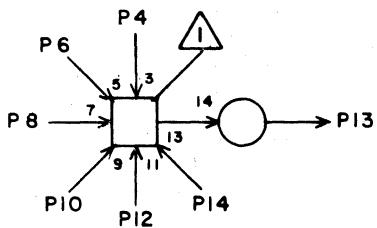
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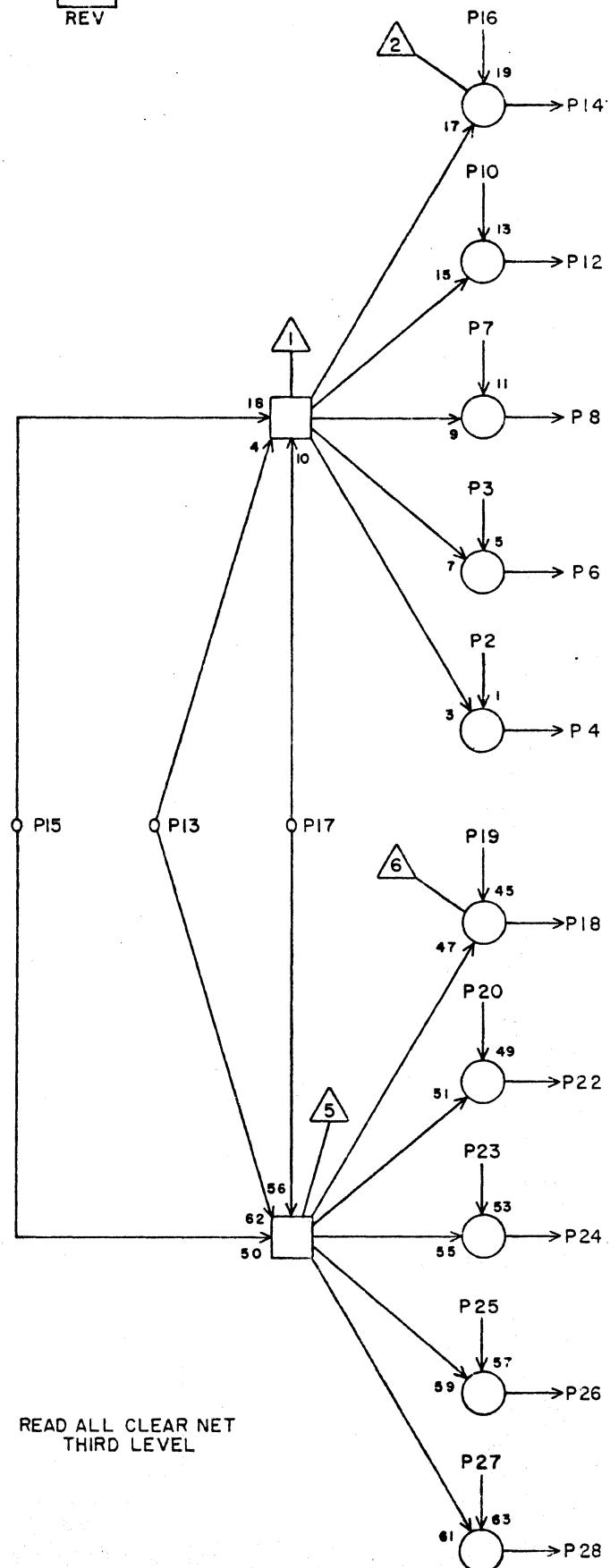
CIRCUIT SPECIFICATION 11827600

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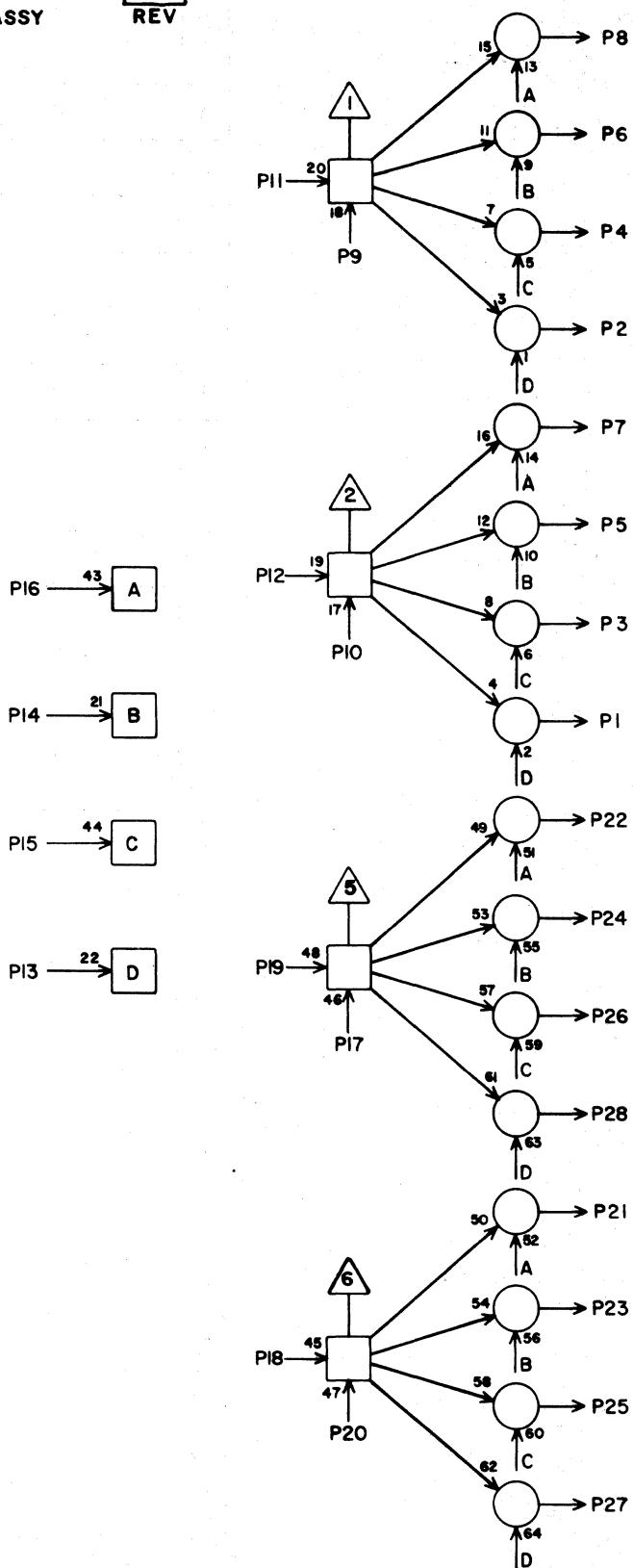
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60042700 Rev. J

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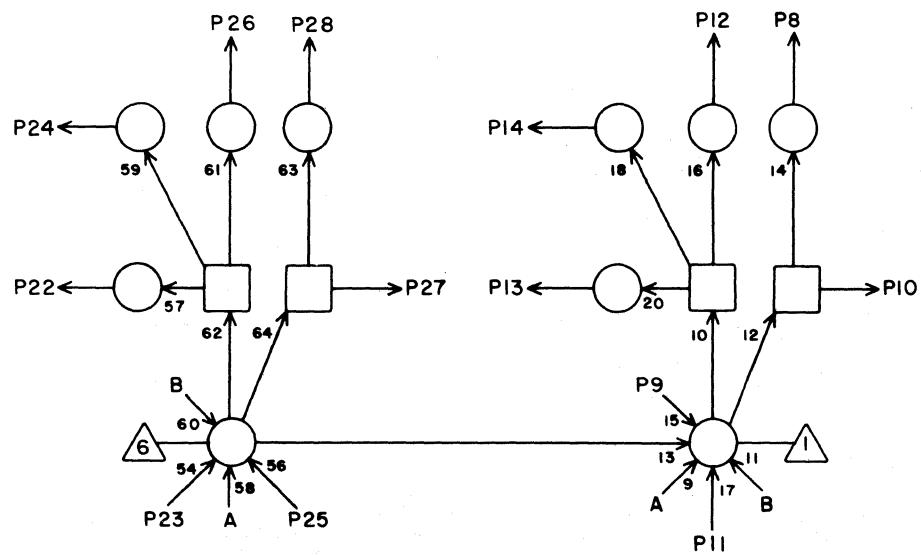
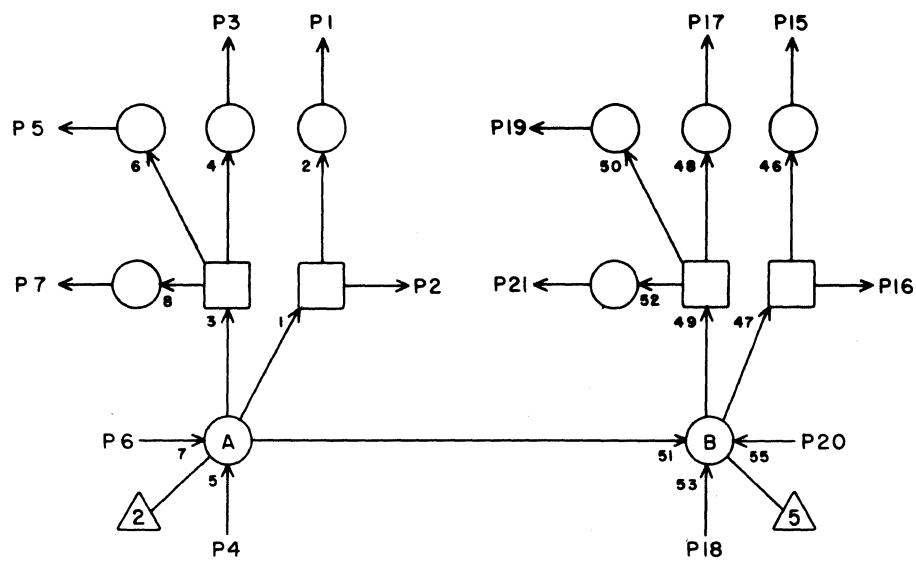


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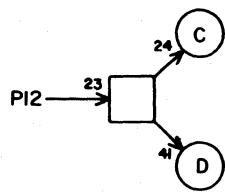
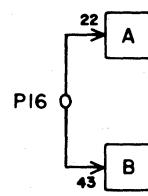
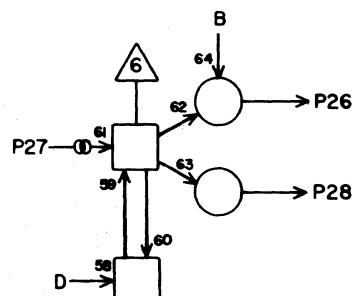
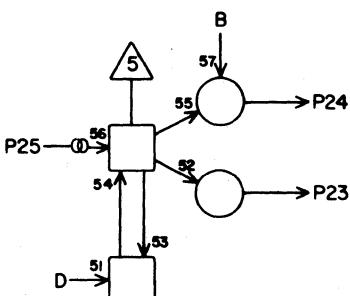
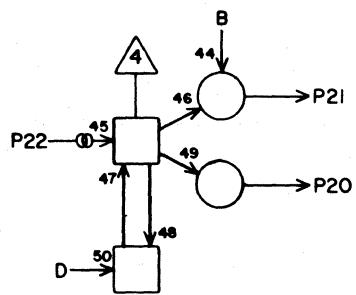
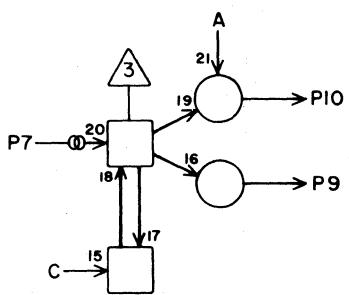
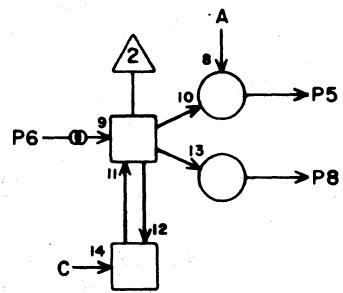
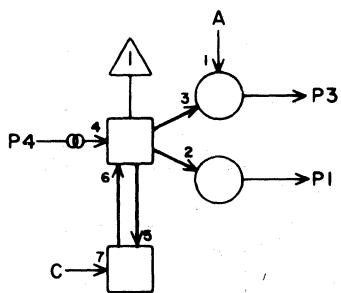
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CIRCUIT SPECIFICATION 11827600

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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

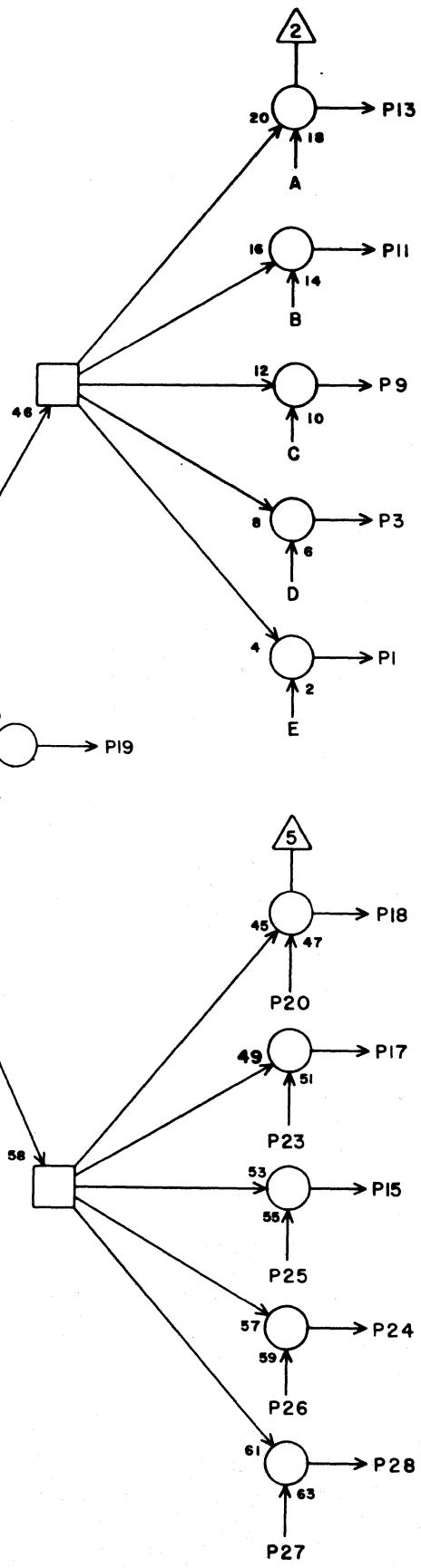
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JACK PIN LG

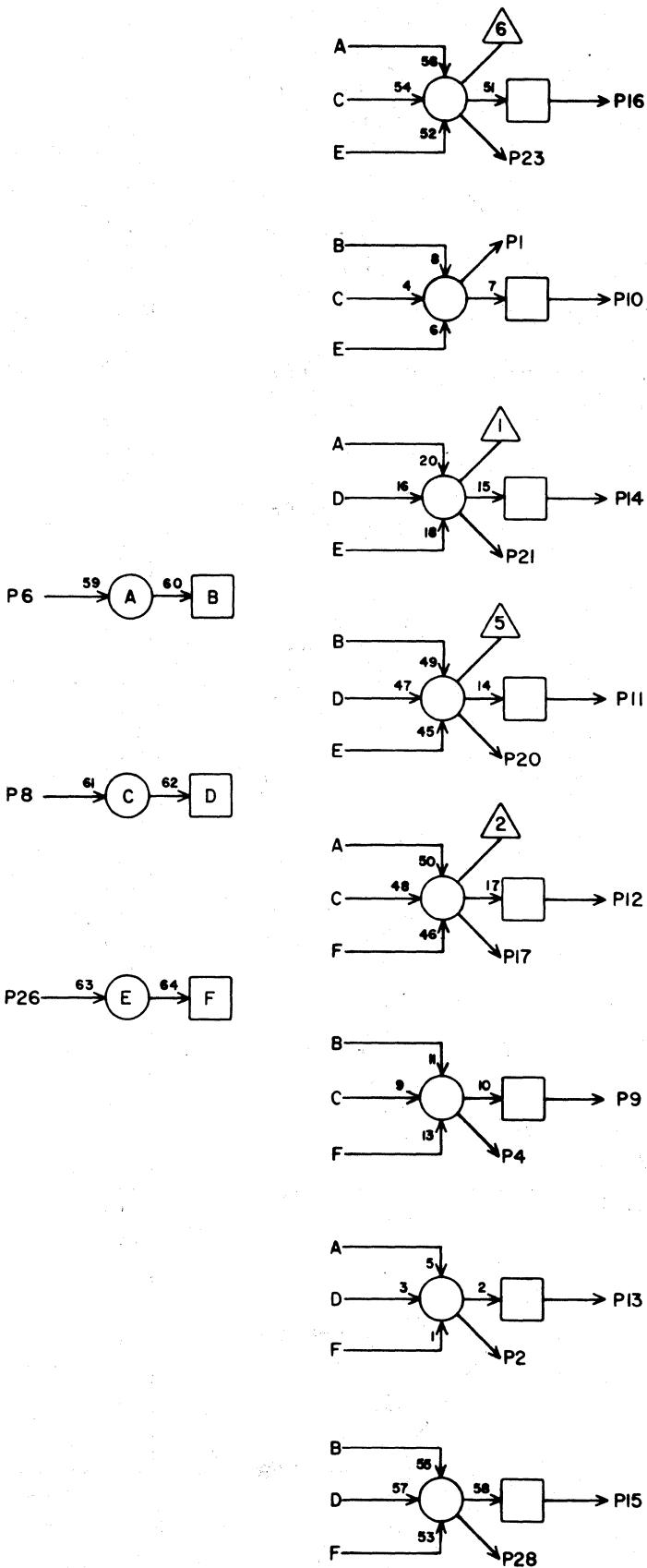
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60042700 Rev. J

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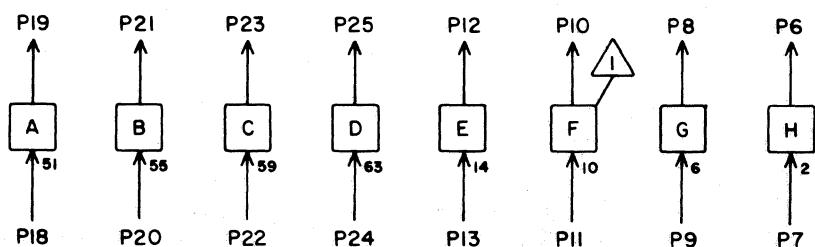
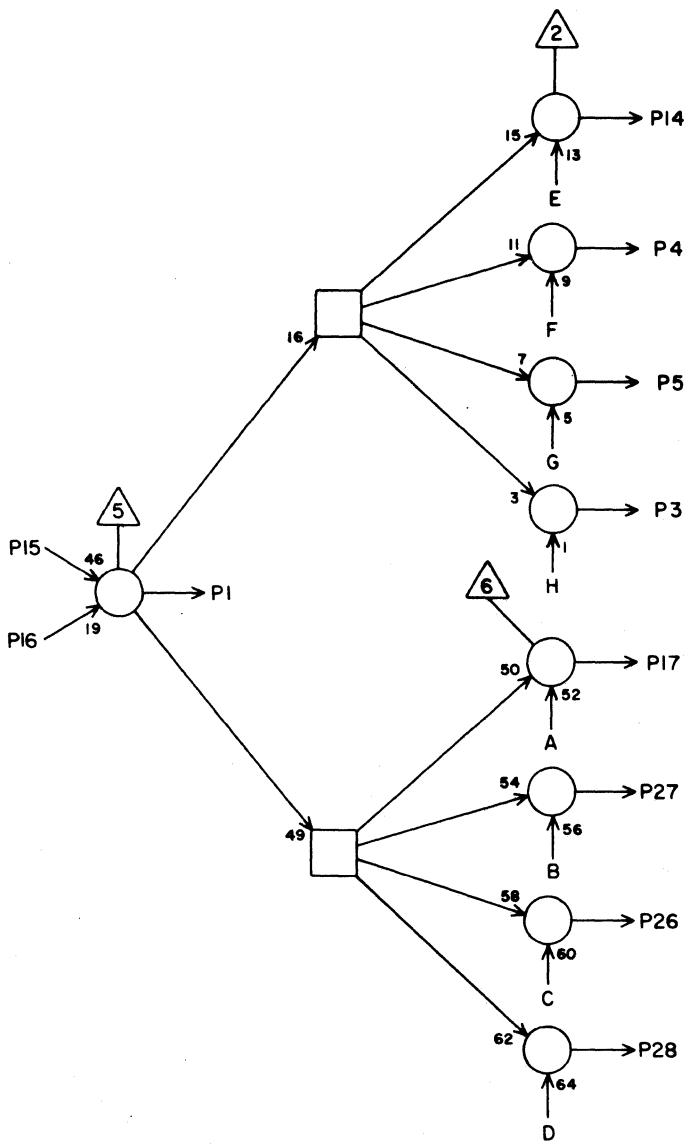
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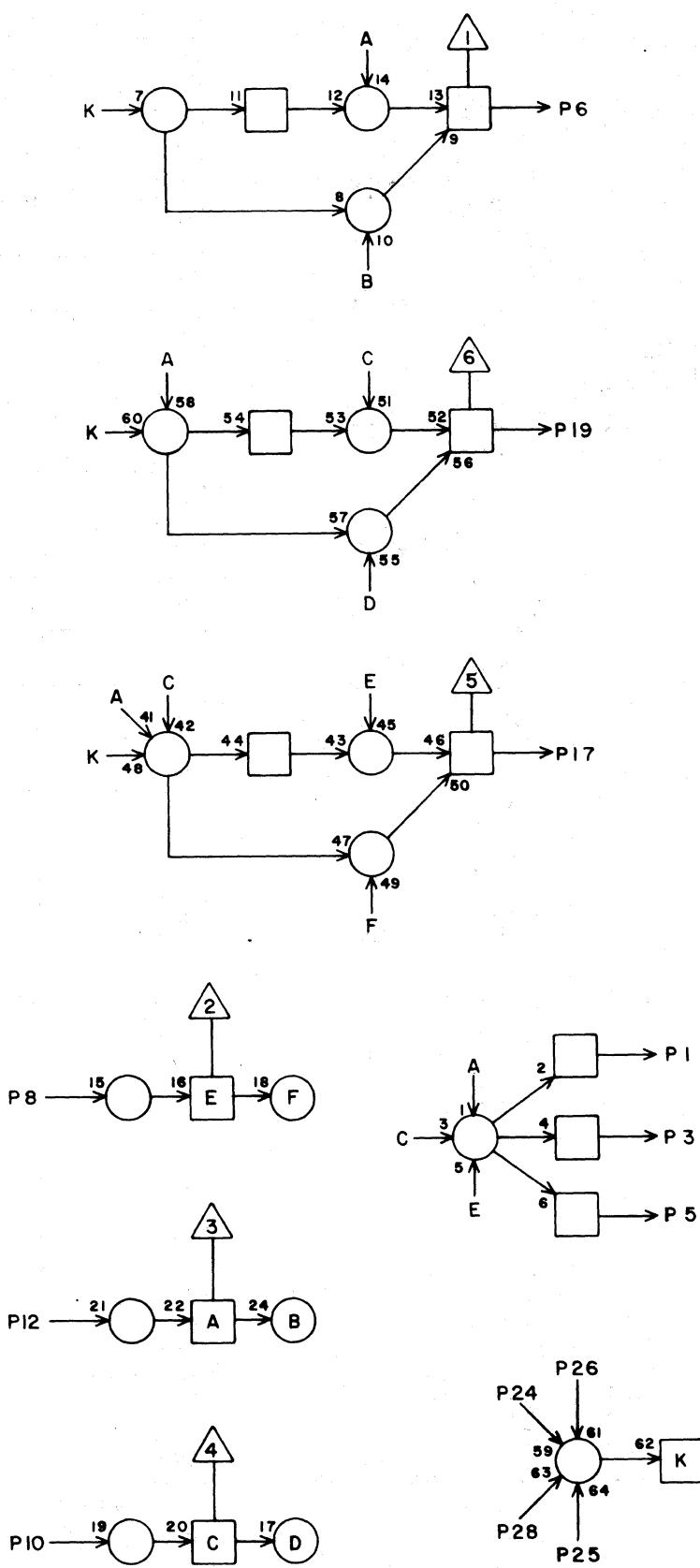
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60042700 Rev. J

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CIRCUIT SPECIFICATION 11827600

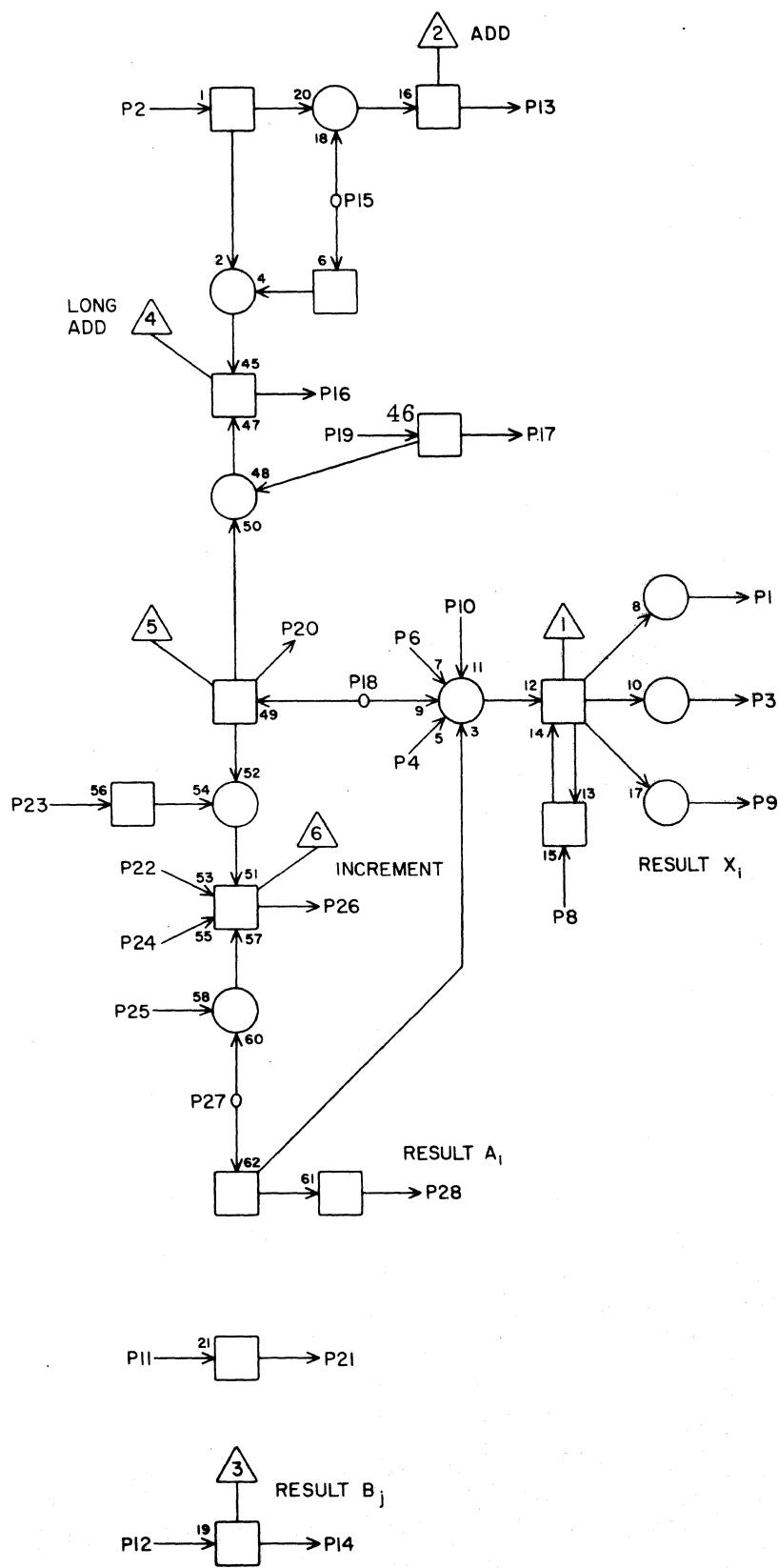
60042700 Rev. J

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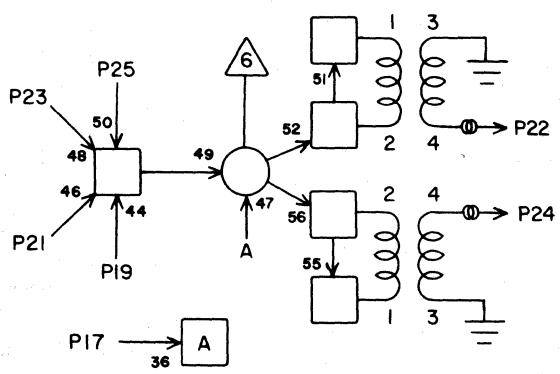
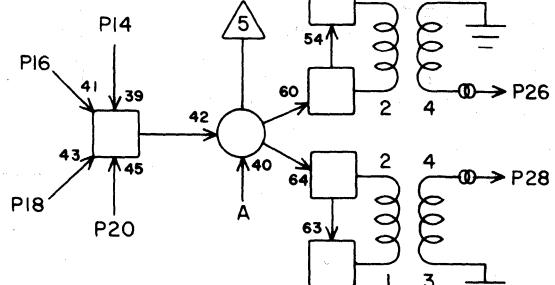
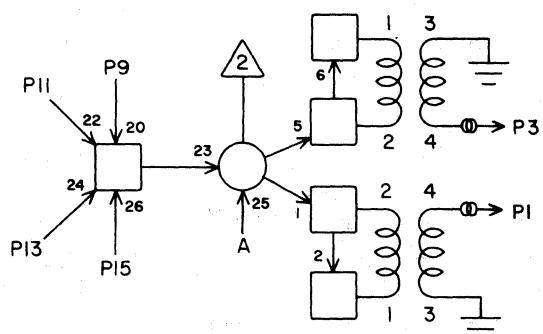
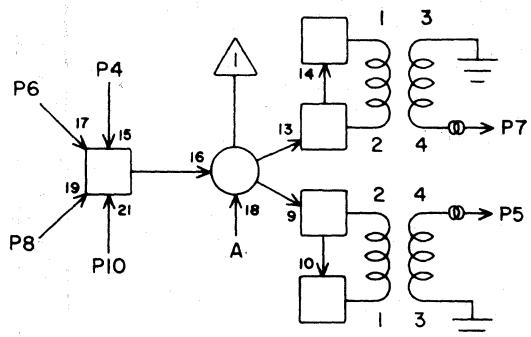
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60042700 Rev. AP

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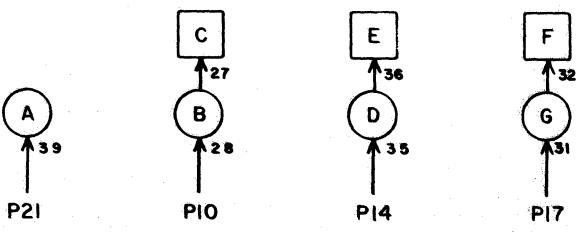
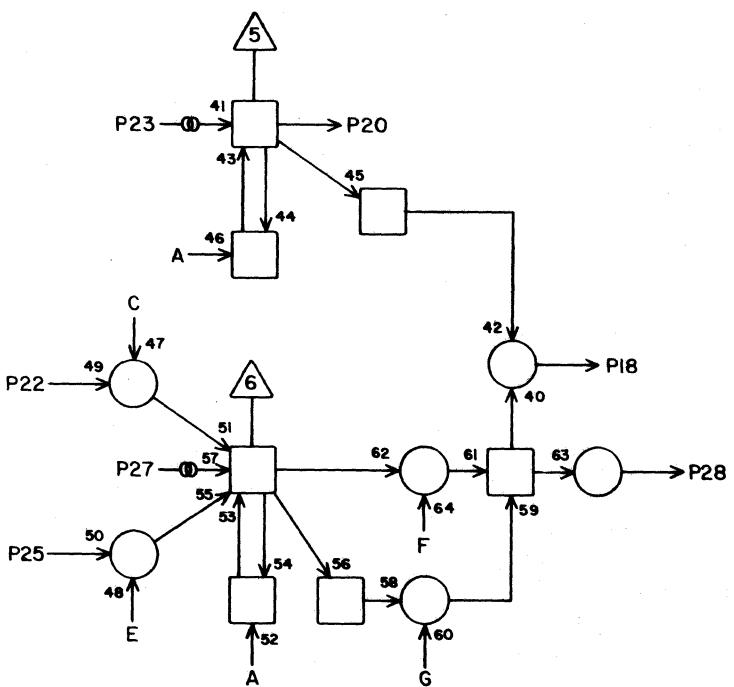
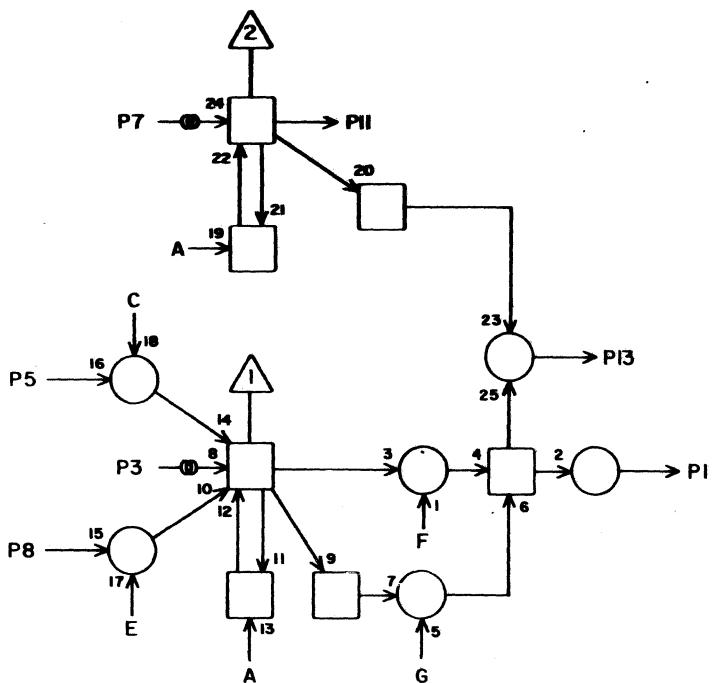
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JACK PIN LG
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60042700 Rev. J

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CIRCUIT SPECIFICATION II827600

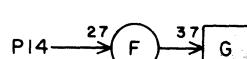
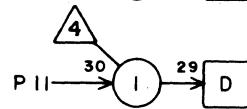
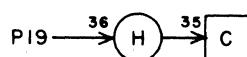
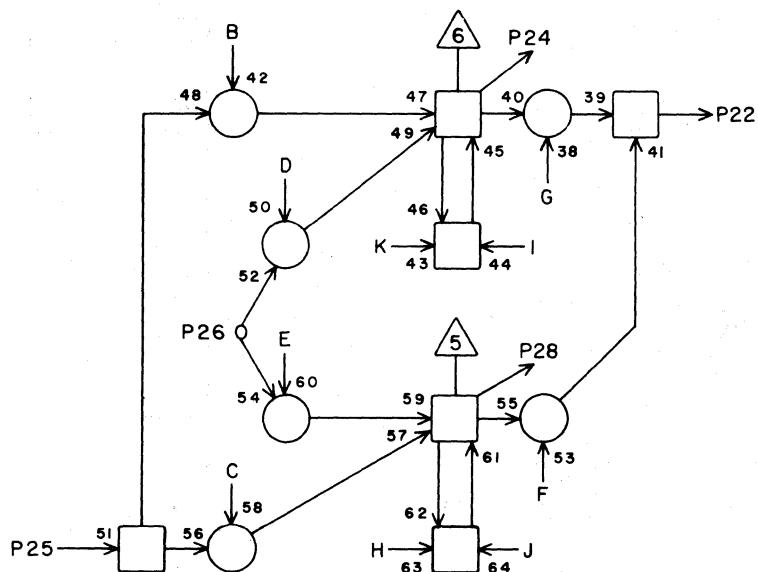
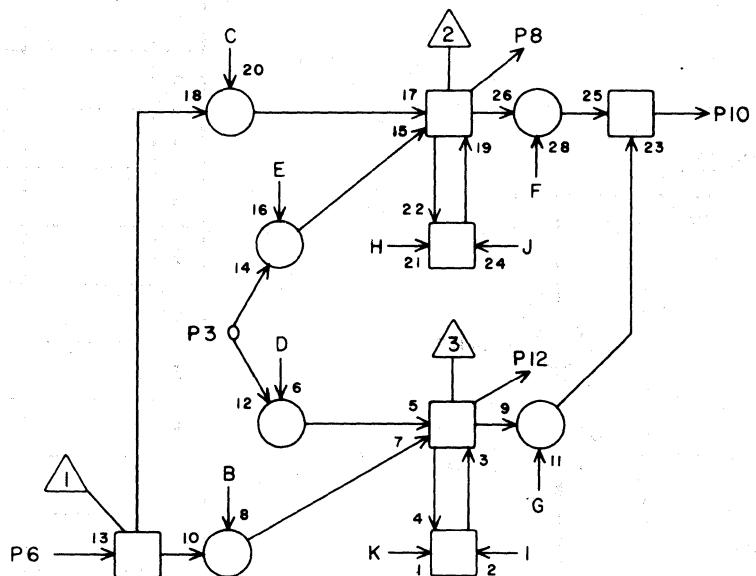
60042700 Rev. J

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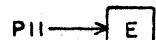
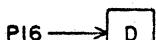
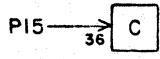
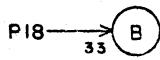
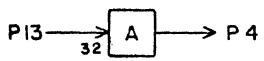
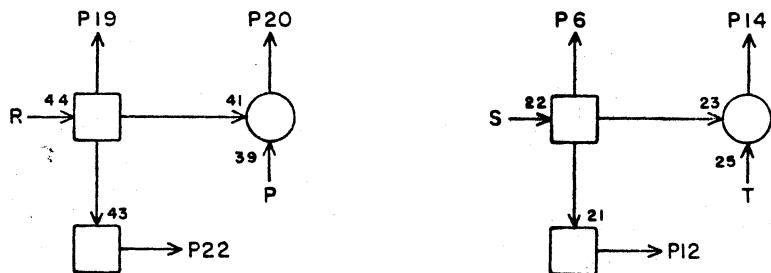
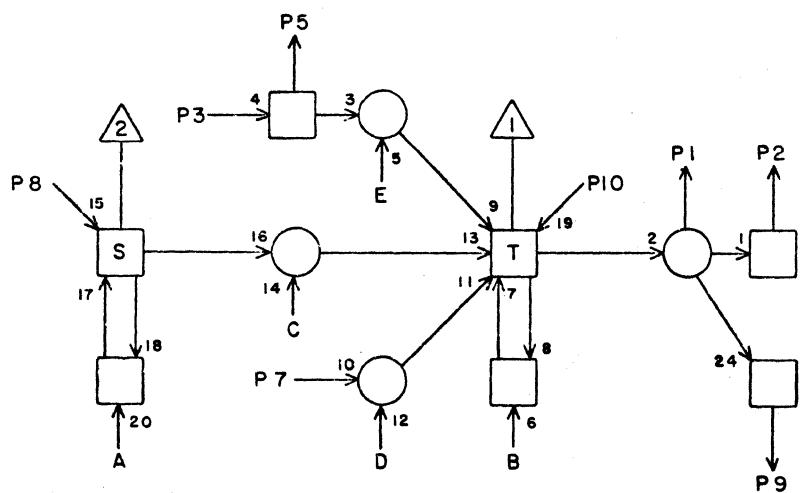
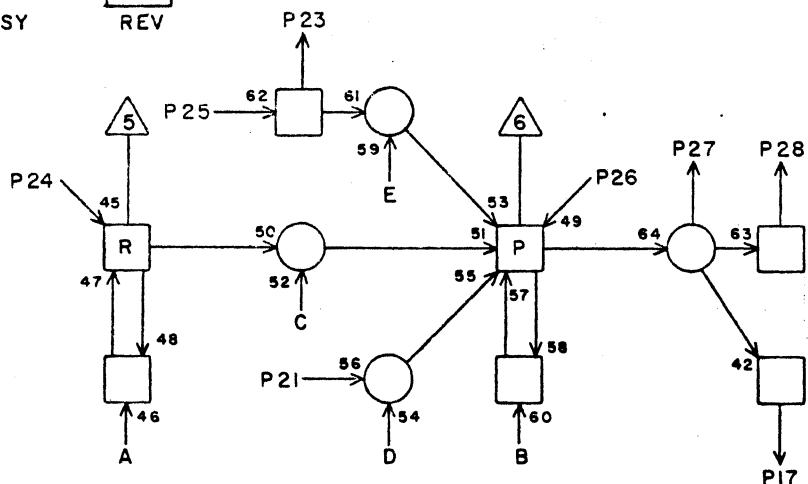
CIRCUIT SPECIFICATION II827600

60042700 Rev. J

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CIRCUIT SPECIFICATION 11827600

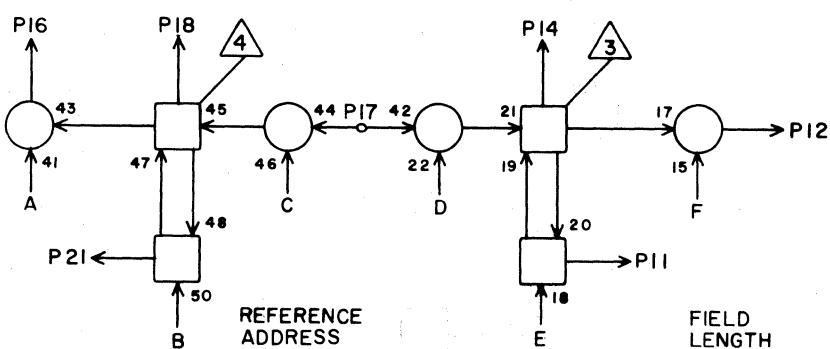
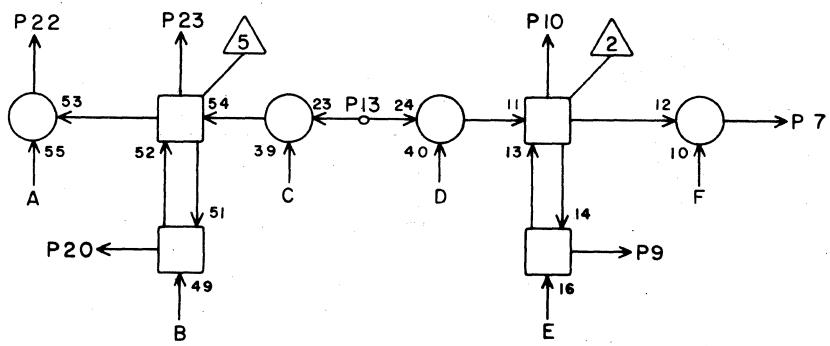
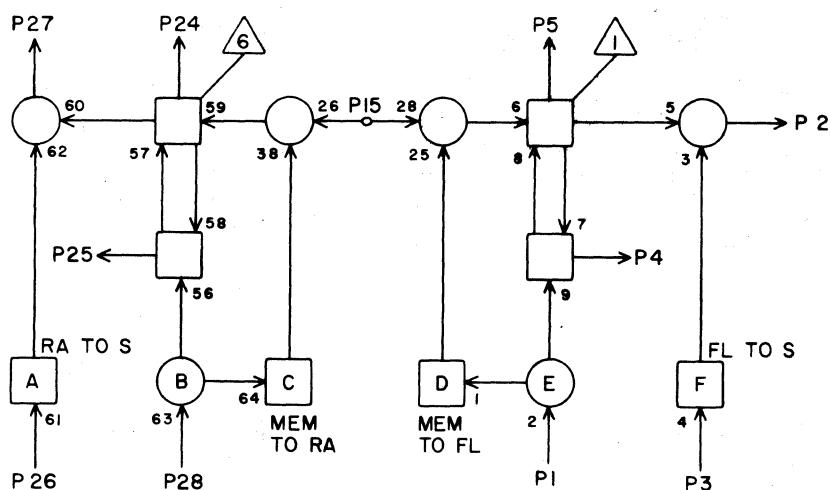
60042700 Rev. J

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JACK PIN LG

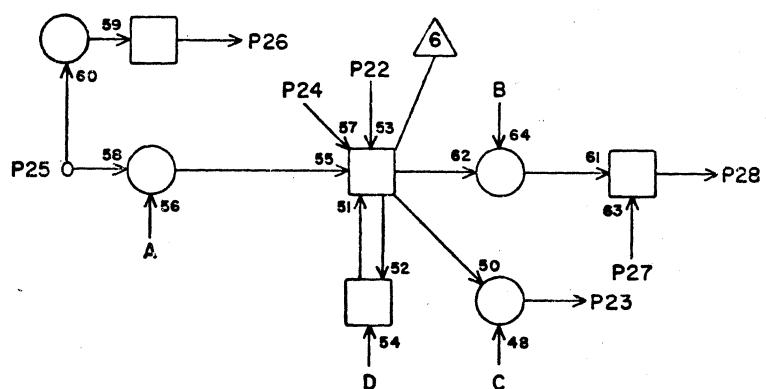
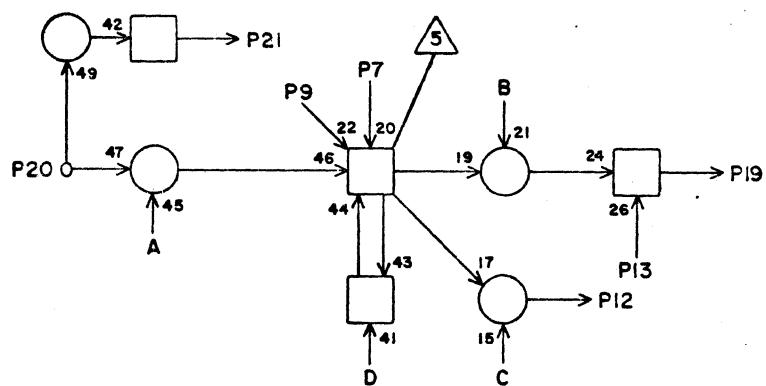
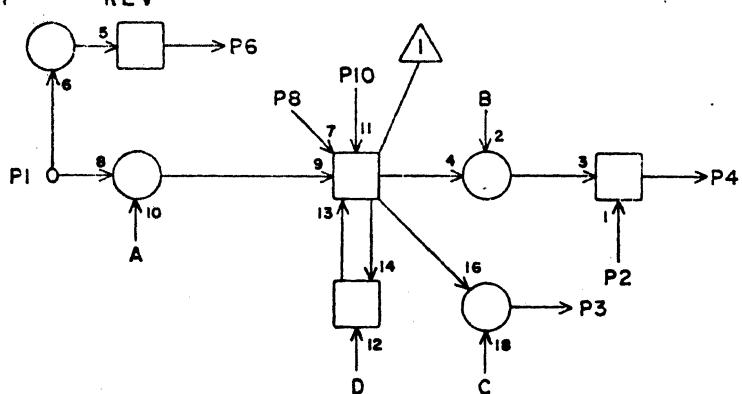
CIRCUIT SPECIFICATION 11827600

60042700 Rev P

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JACK PIN LG

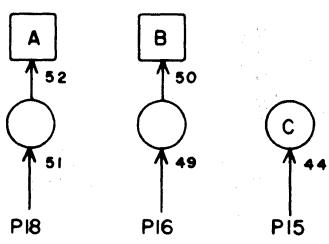
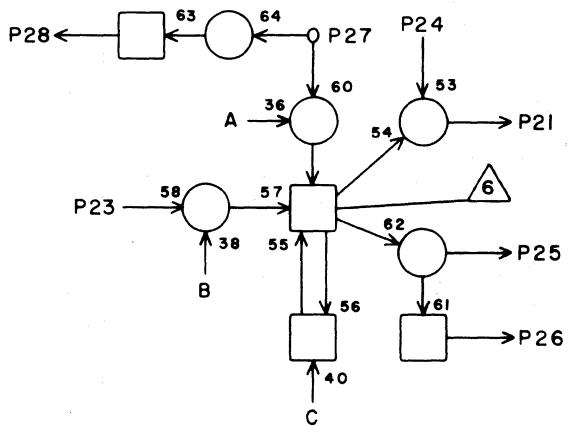
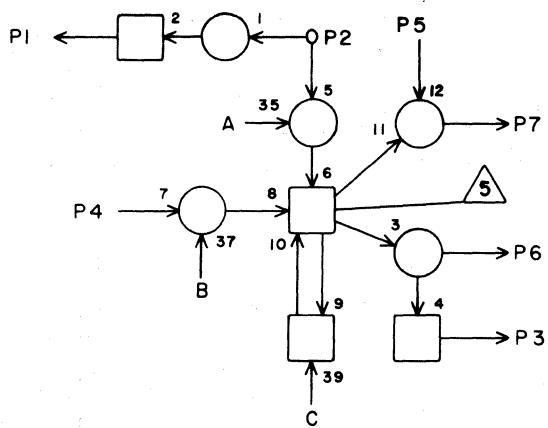
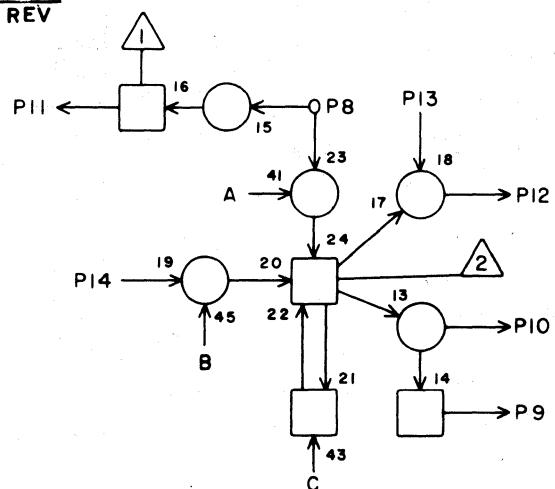
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63050300
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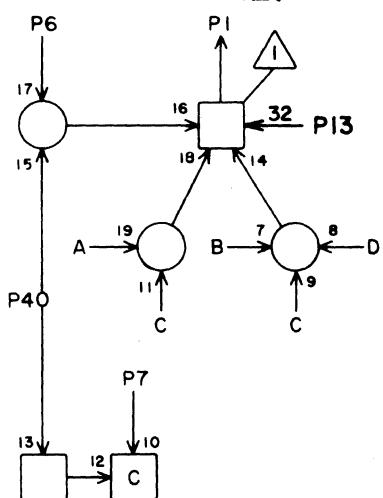
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63050400
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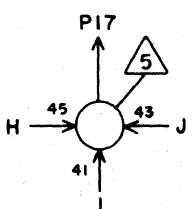
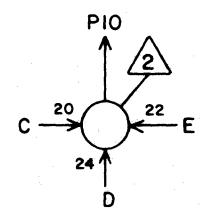


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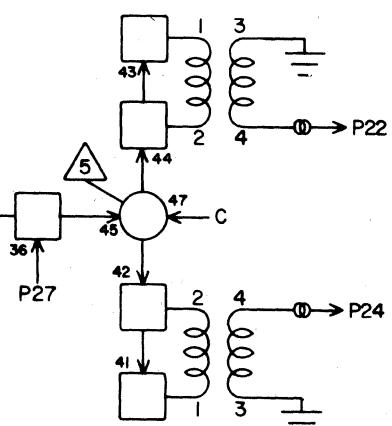
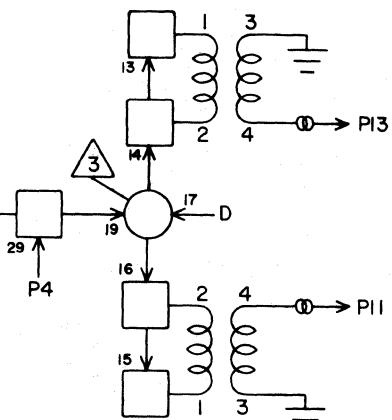
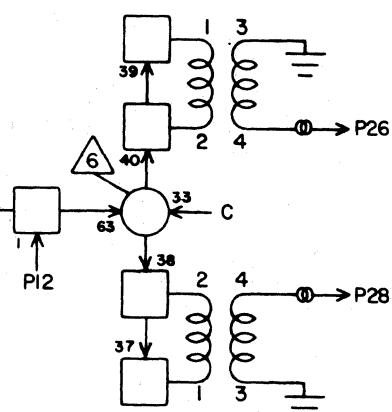
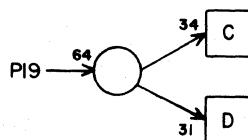
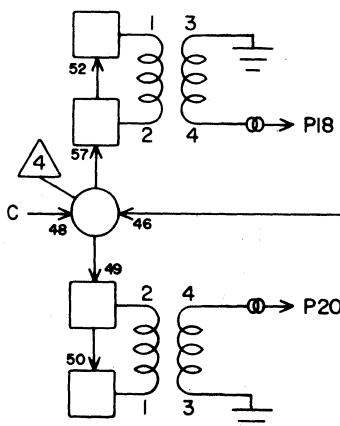
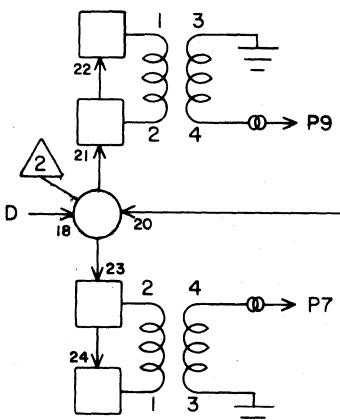
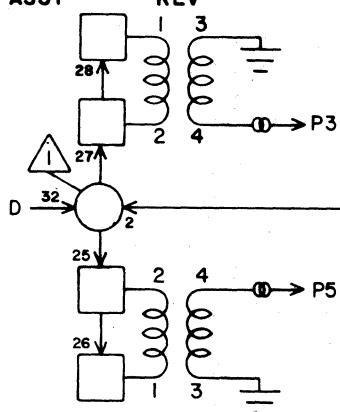
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JACK PIN LG



CIRCUIT SPECIFICATION 11827600
60042700 Rev AB

LS 63050500 C
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60042700 Rev J

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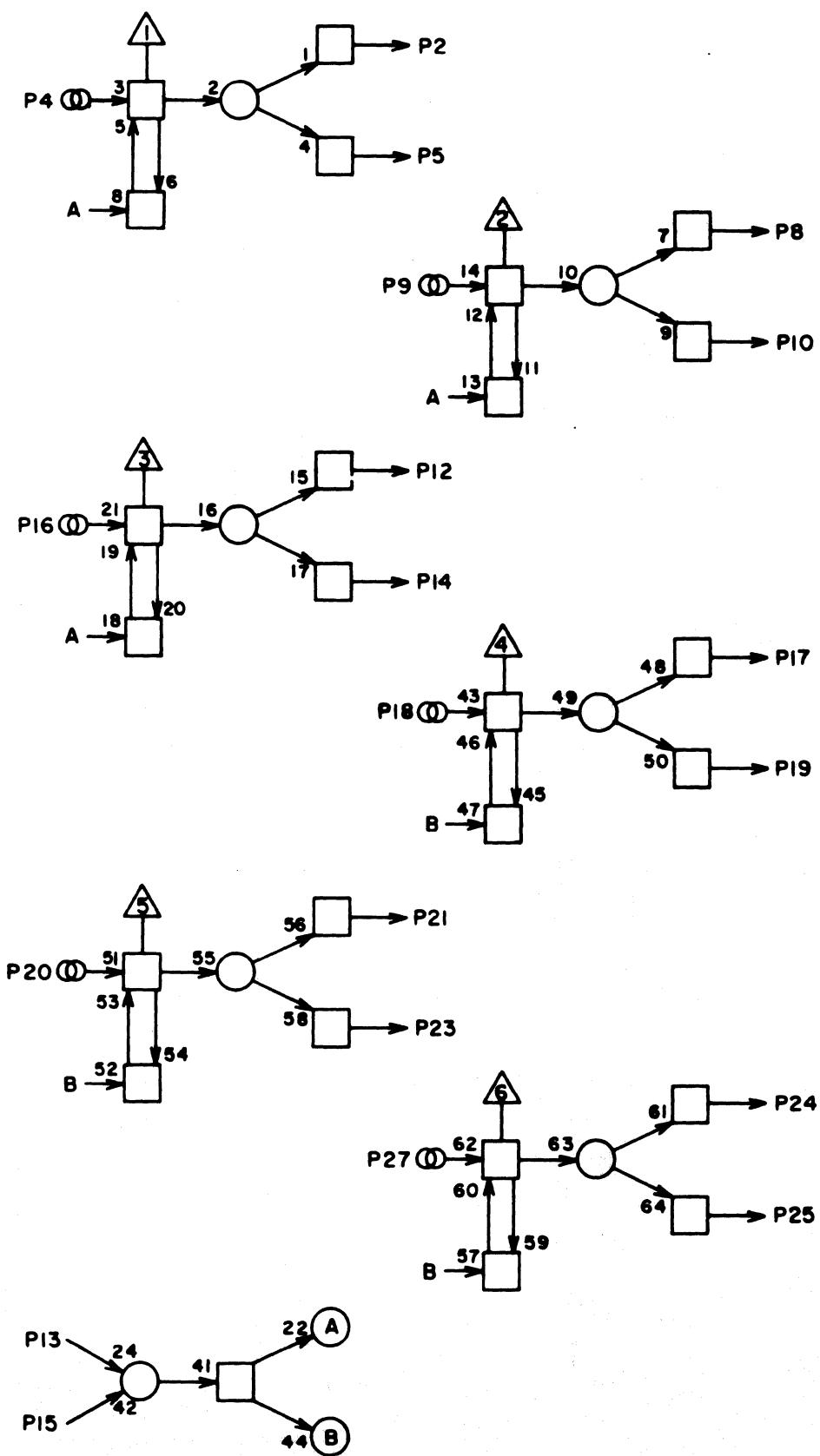
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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

LS63050600 B
ASSY REV

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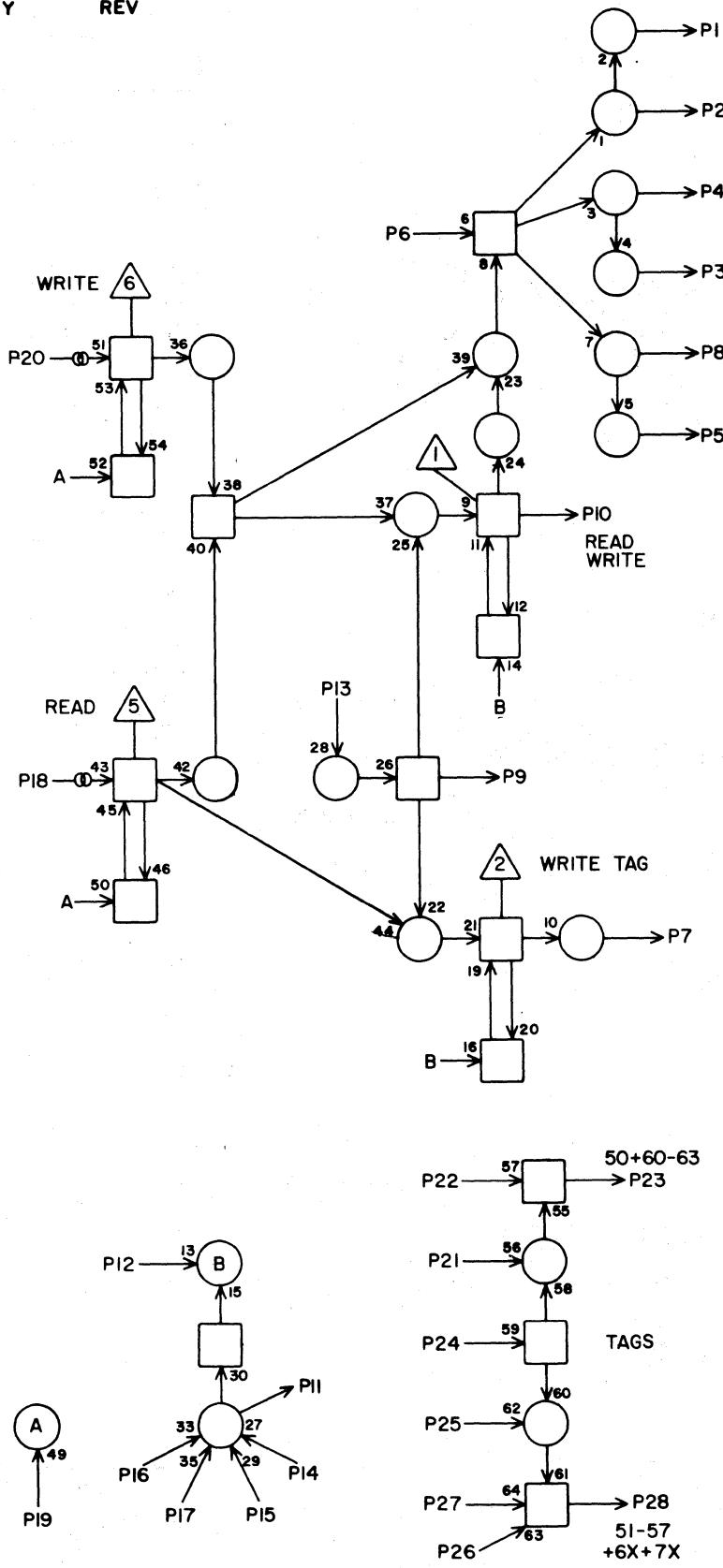
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev. P

LS 63050700
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CIRCUIT SPECIFICATION 11827600

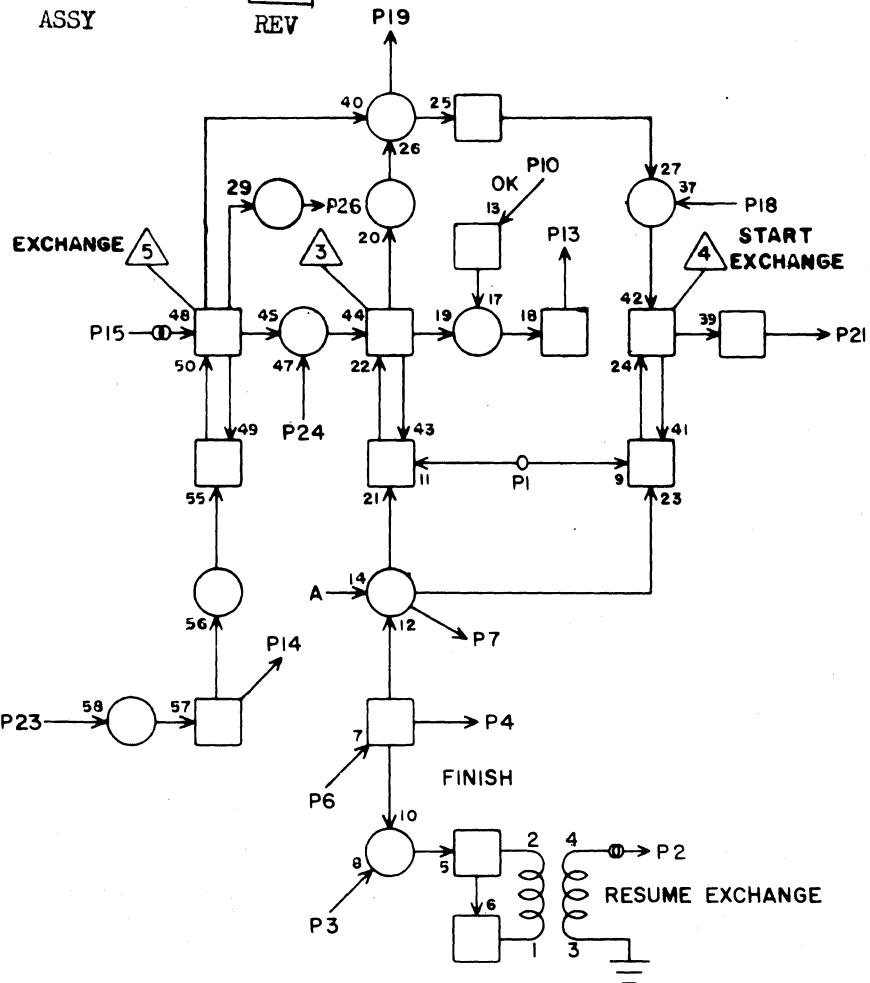
60042700 Rev. P

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JACK PIN LG

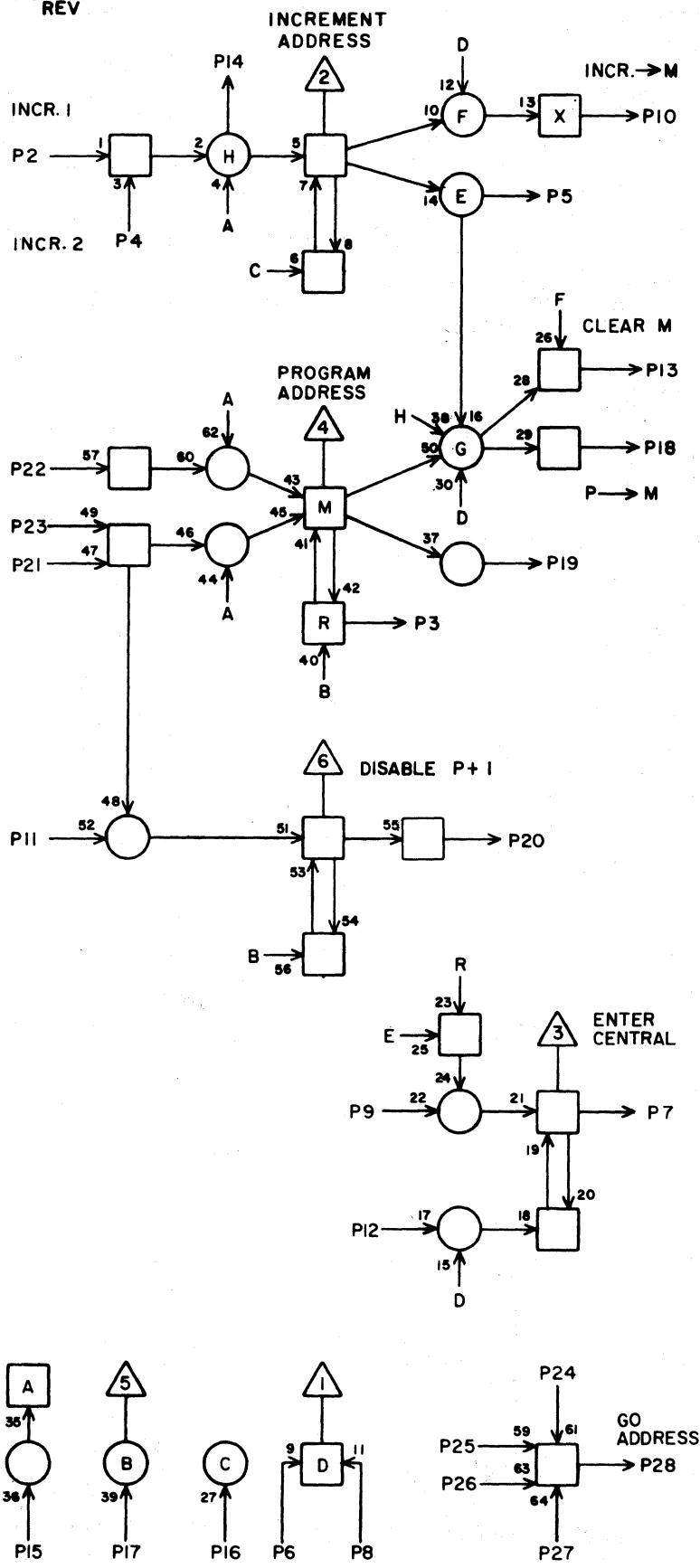
CIRCUIT SPECIFICATION 11827600

60042700 Rev AB

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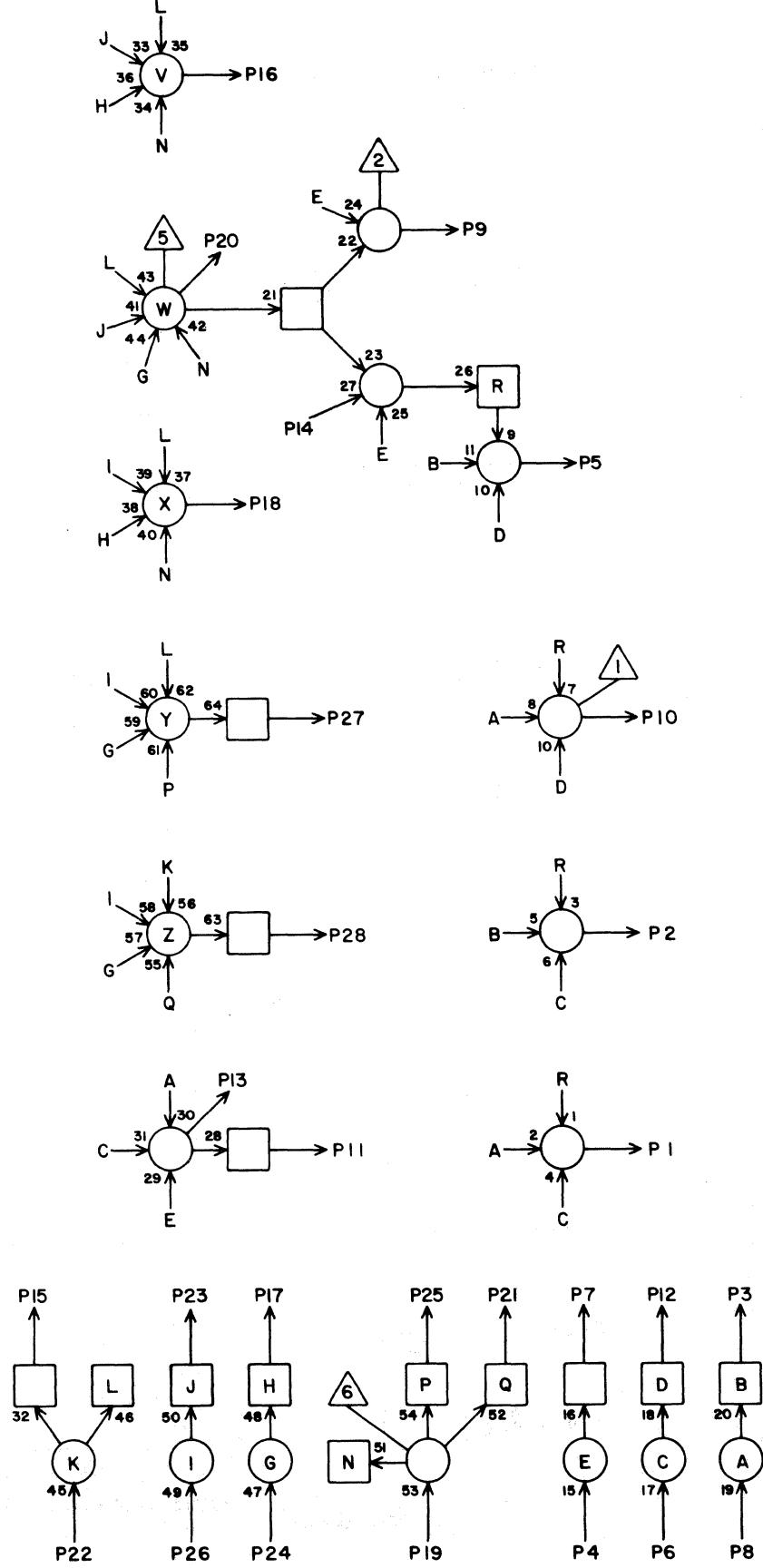
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 63051000
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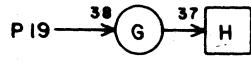
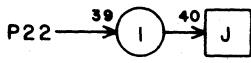
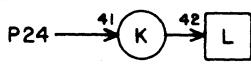
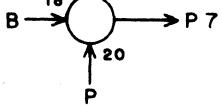
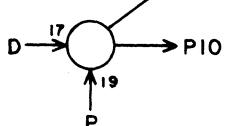
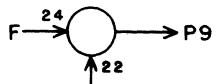
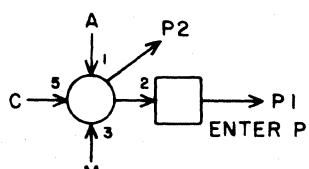
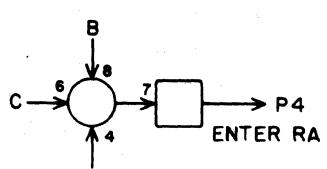
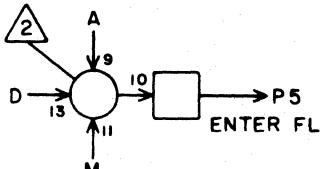
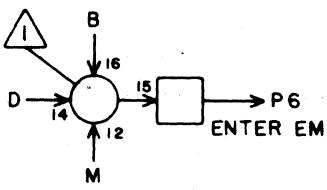
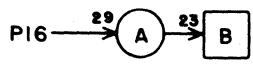
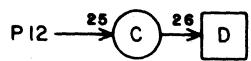
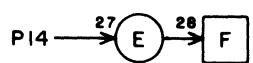
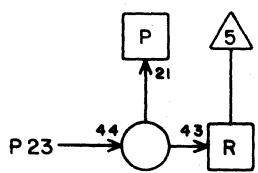
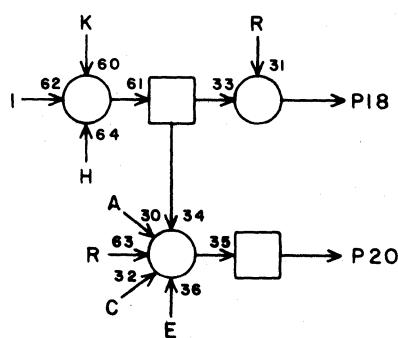
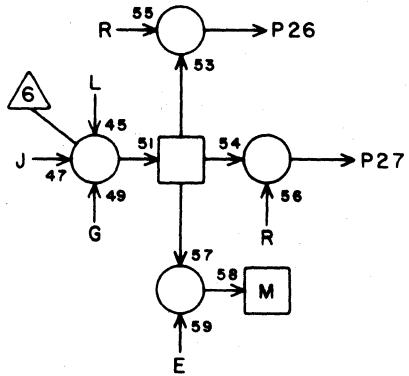
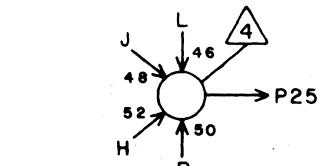
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JACK PIN LG
CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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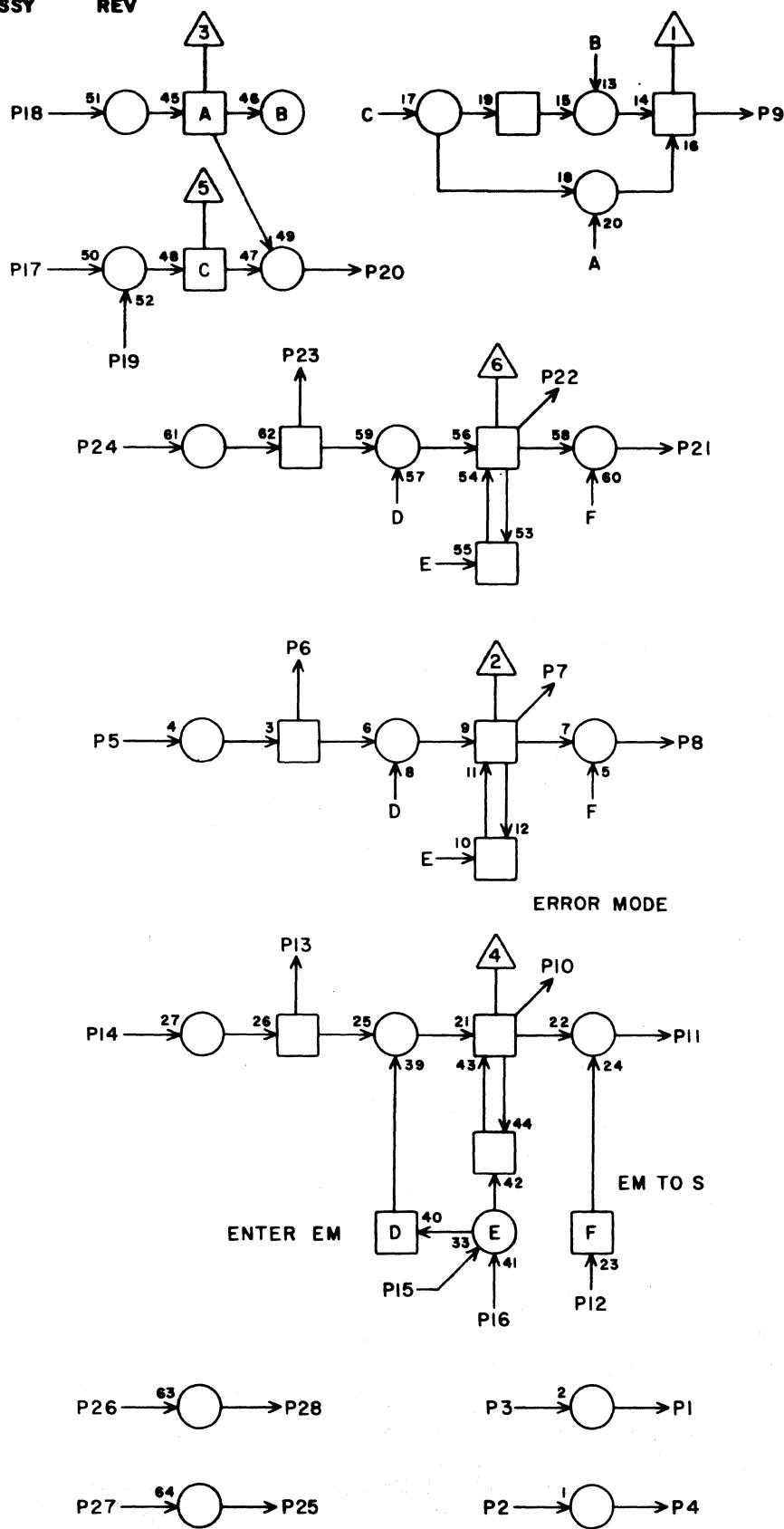
JACK PIN LG

60042700 Rev J

CIRCUIT SPECIFICATION 11827600

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JACK PIN LG

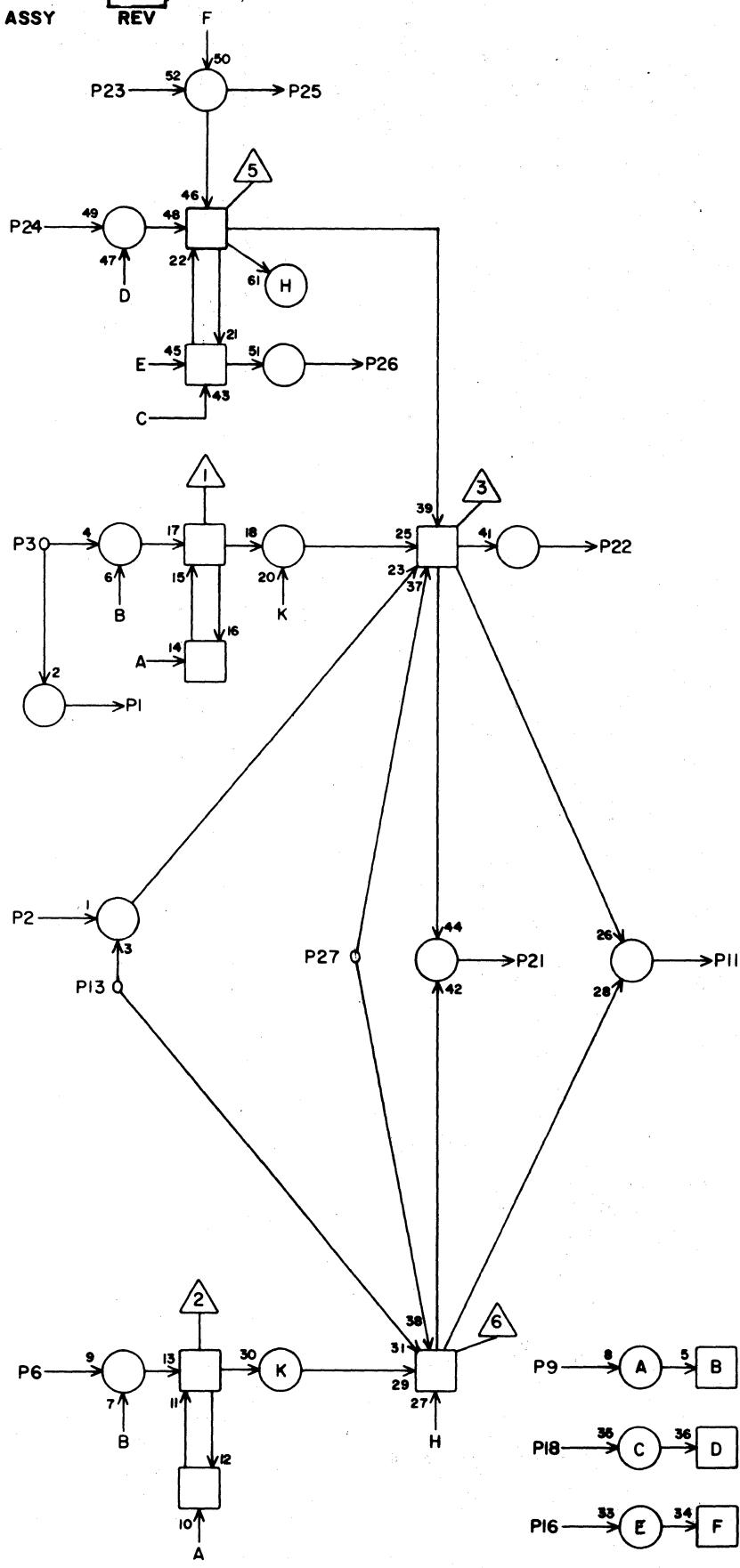
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60042700 Rev. P

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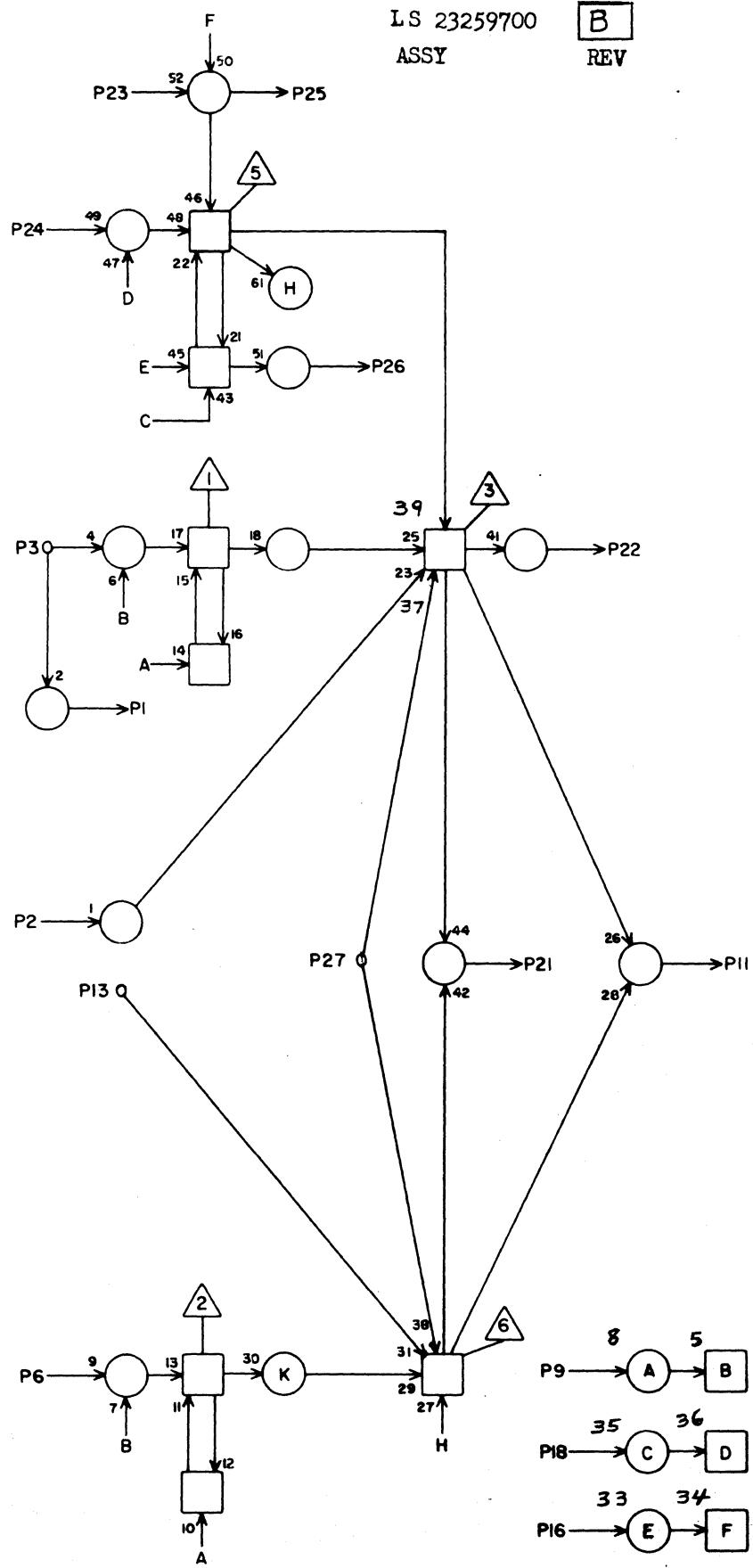


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CIRCUIT SPECIFICATION 11827600

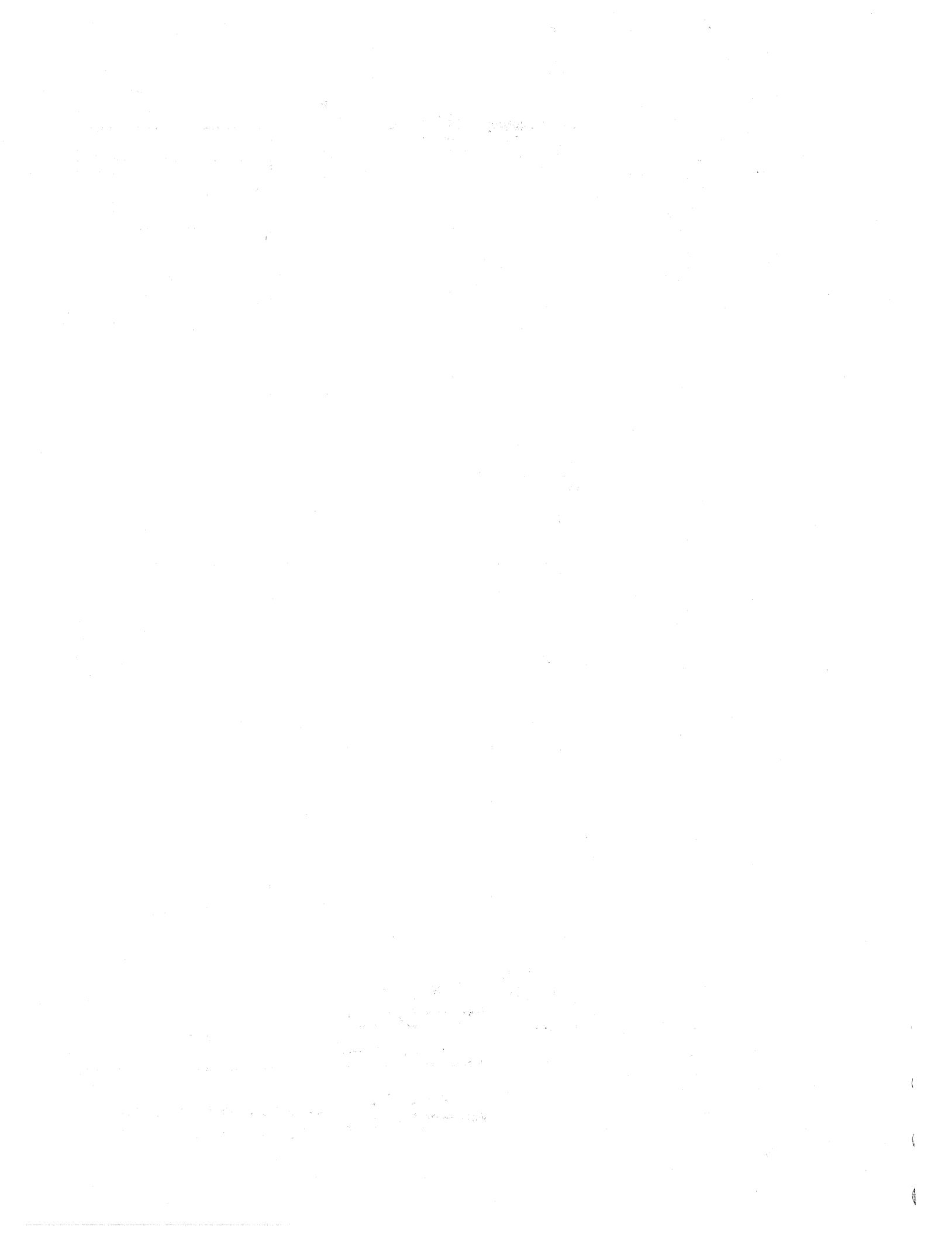
60042700 Rev. J

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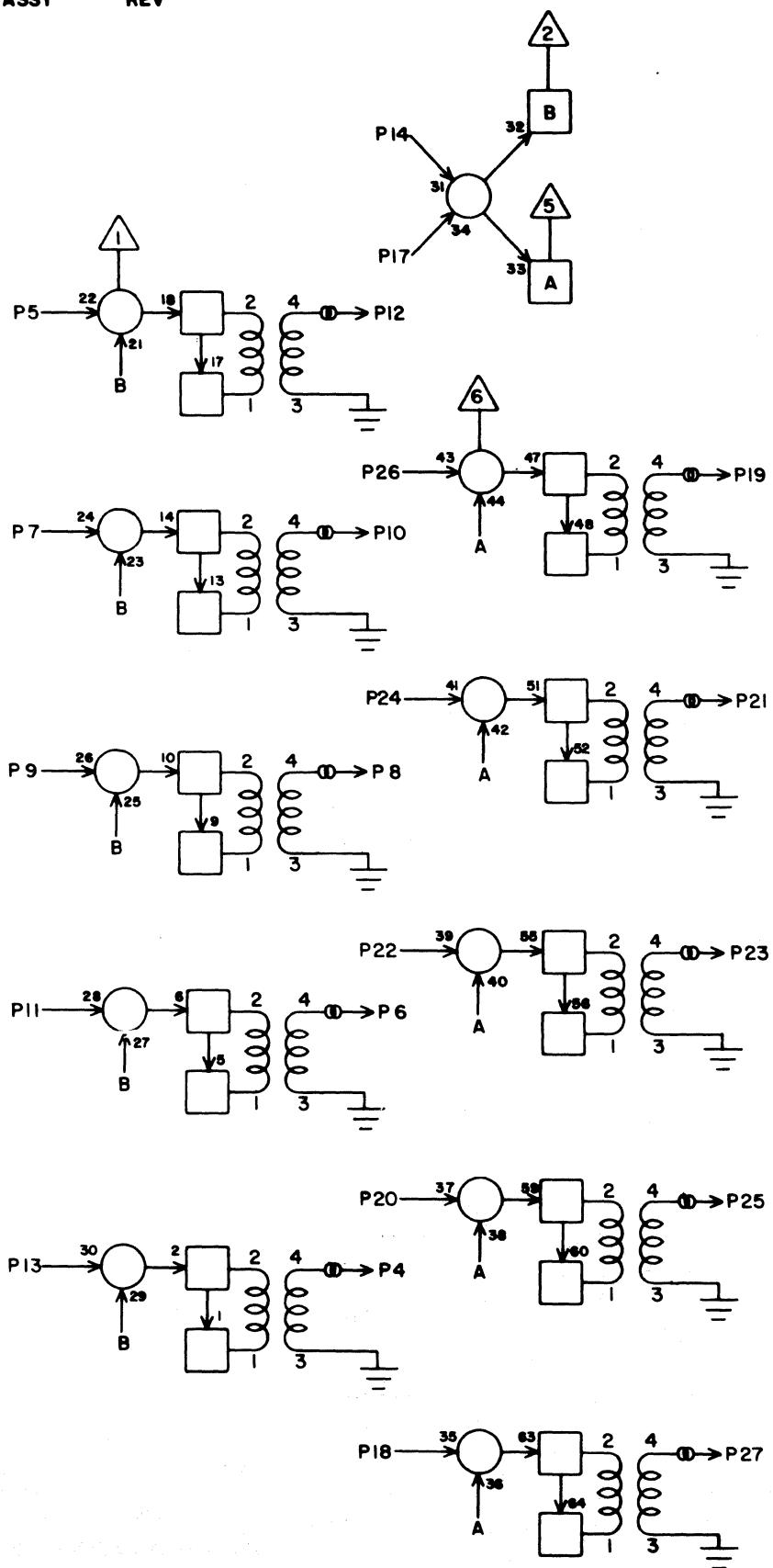
CIRCUIT SPECIFICATION 11827600
60042700 Rev AB



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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

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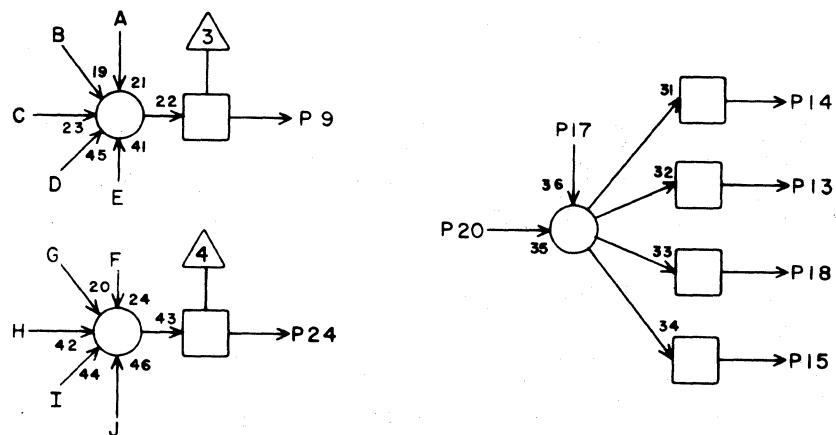
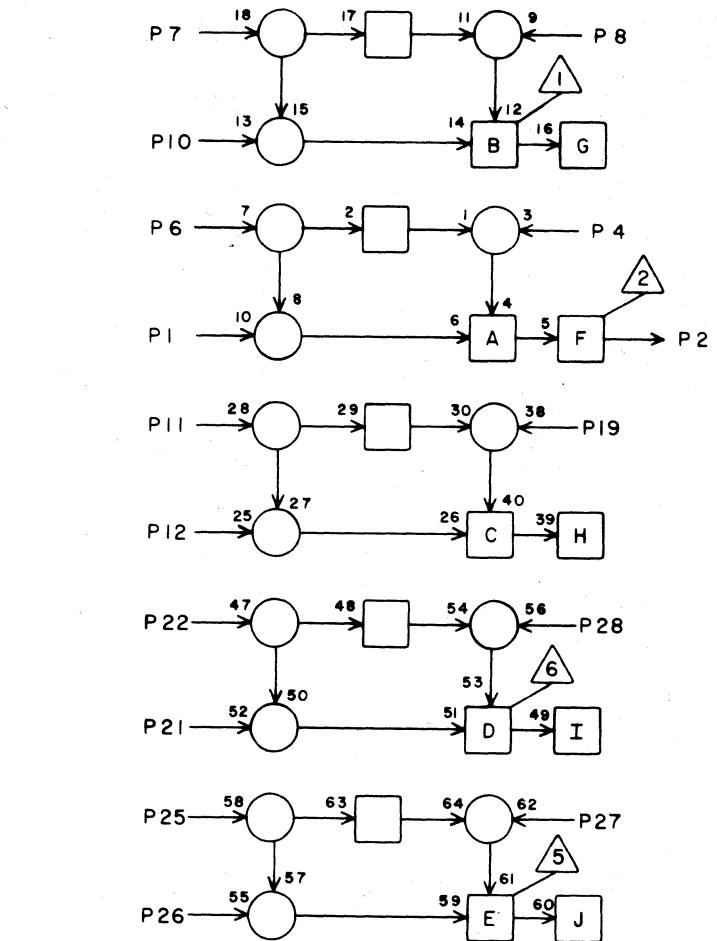
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JACK PIN LG

CIRCUIT SPECIFICATION 11827600

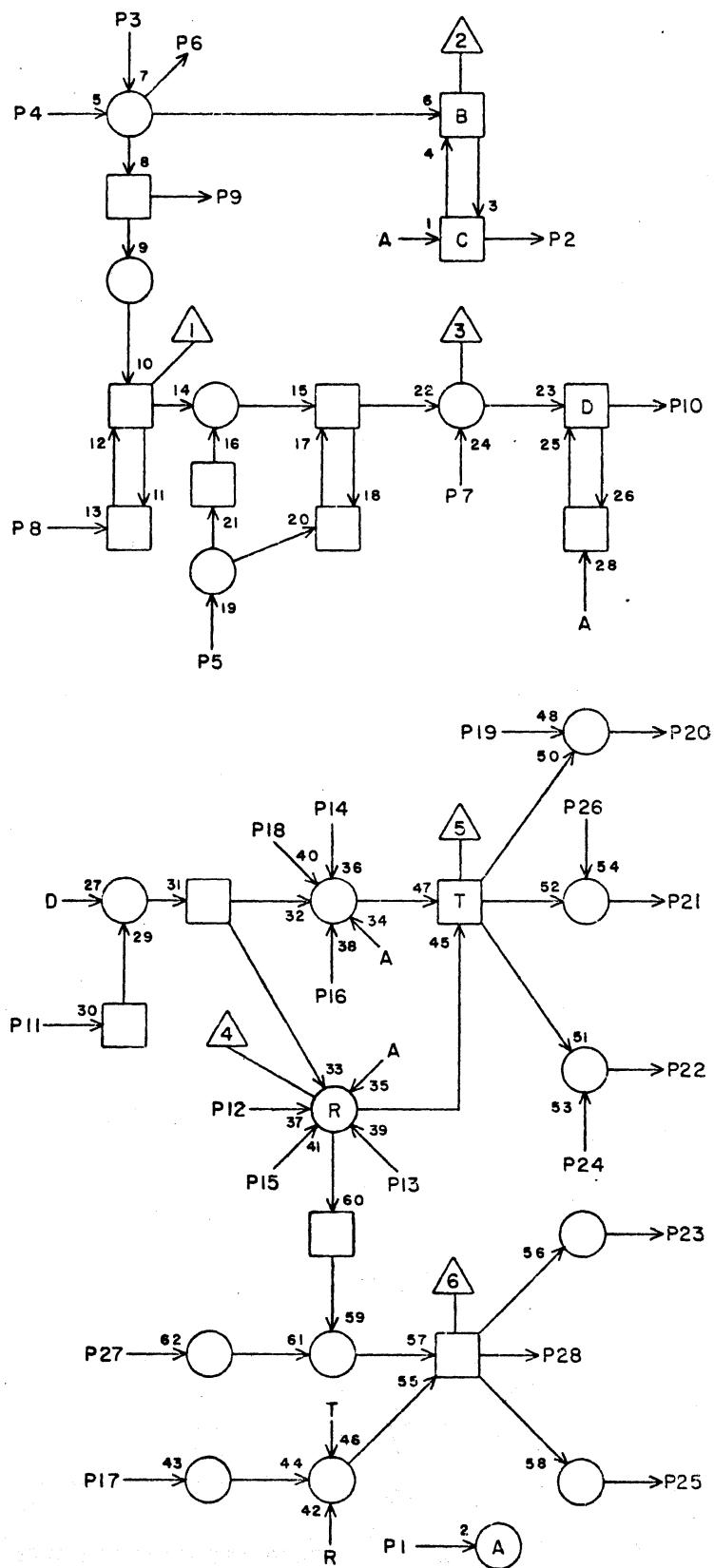
60042700 Rev. P



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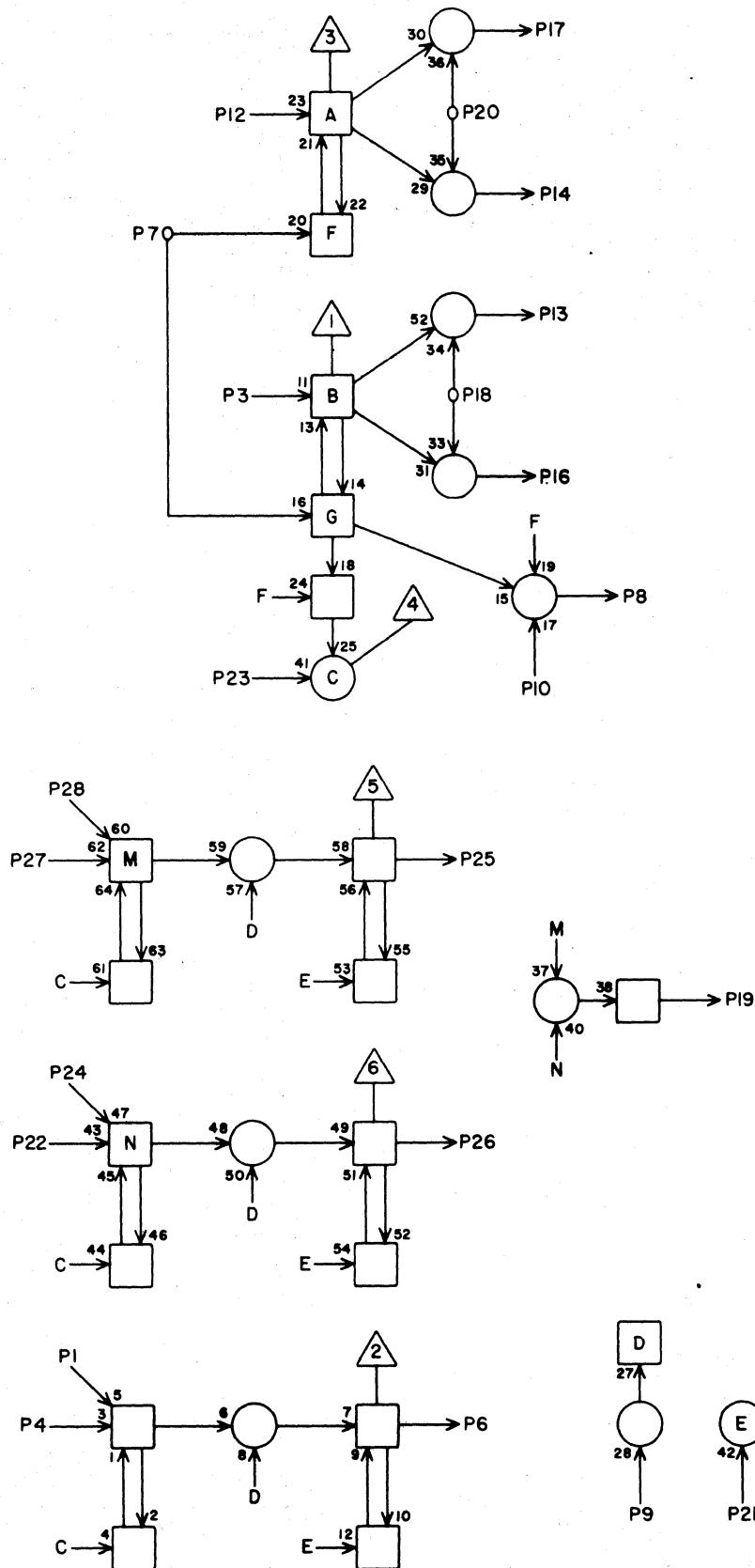
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CIRCUIT SPECIFICATION 11827600

60042700 Rev J

LS 63051700 D
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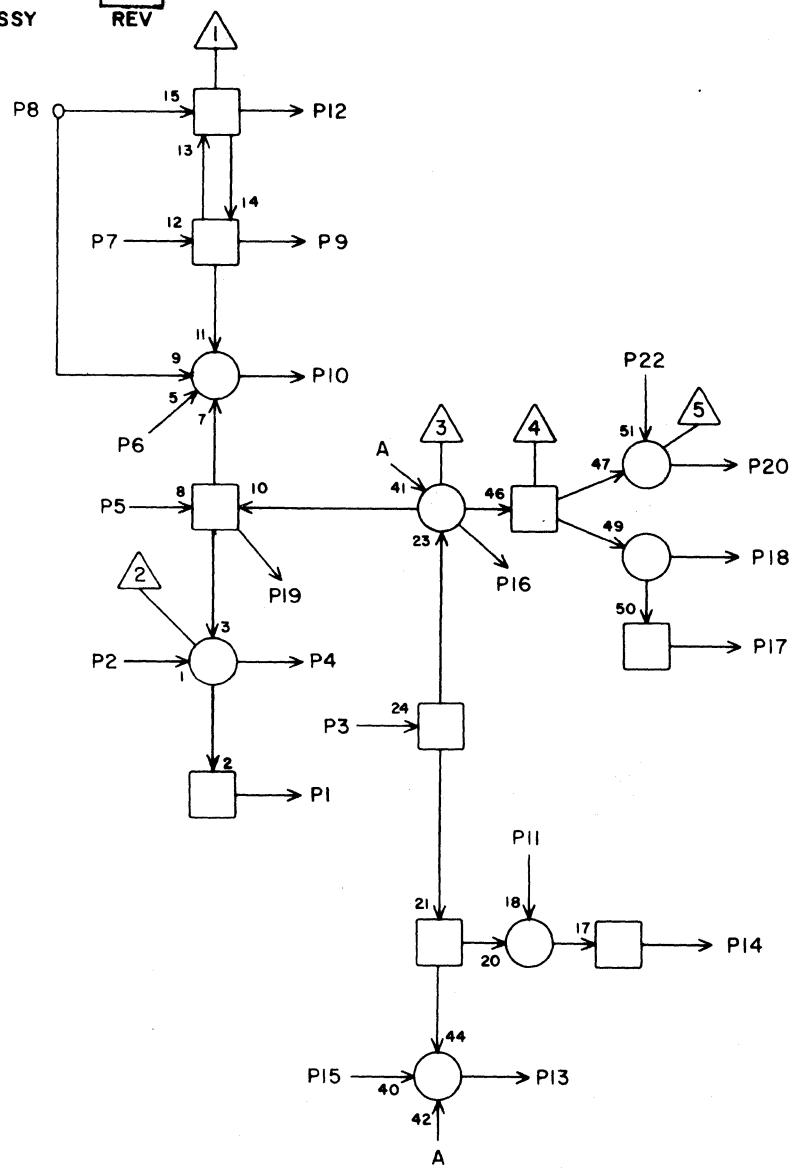
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CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

LS 63051800
ASSY REV D

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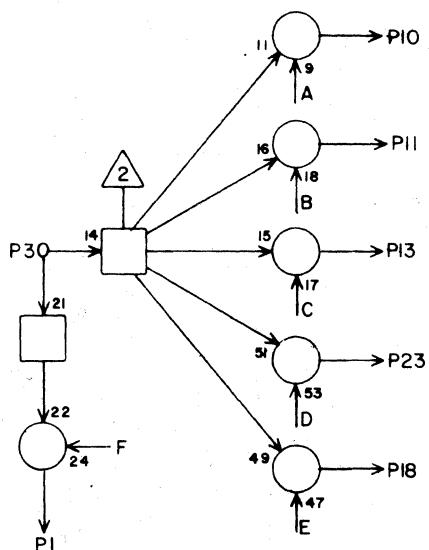
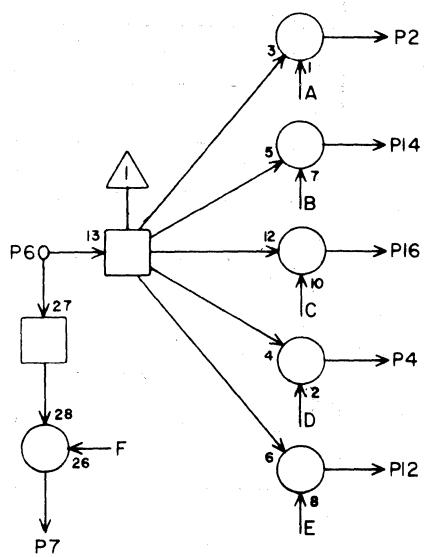
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

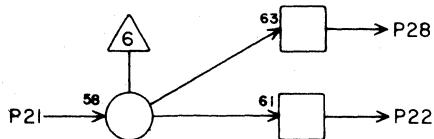
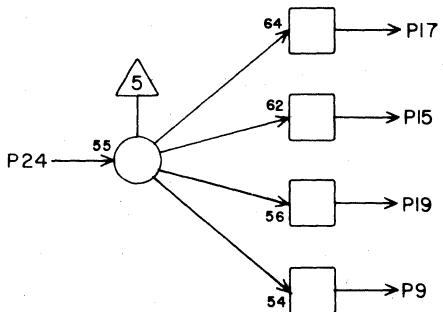
LS 63051900
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P8 → A

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P26 → C

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P27 → E

P20 → F

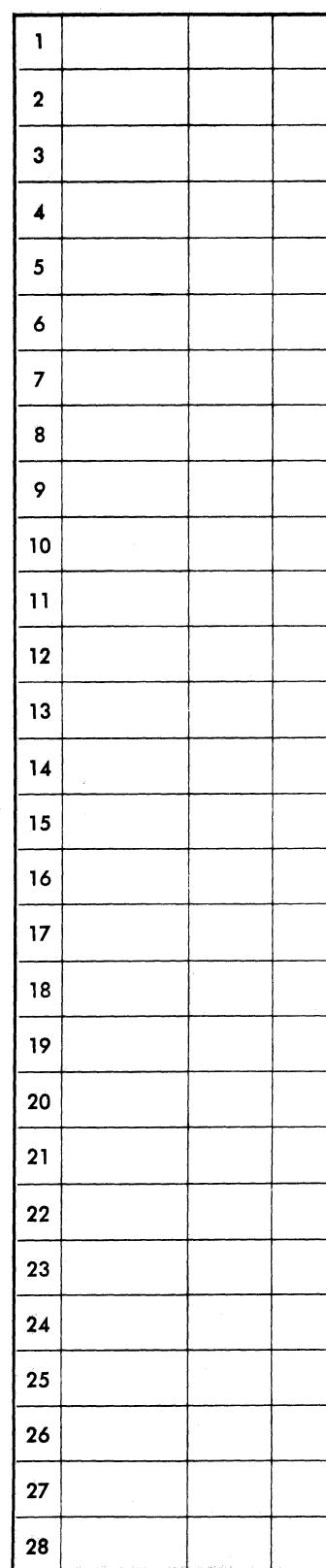
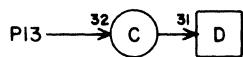
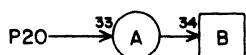
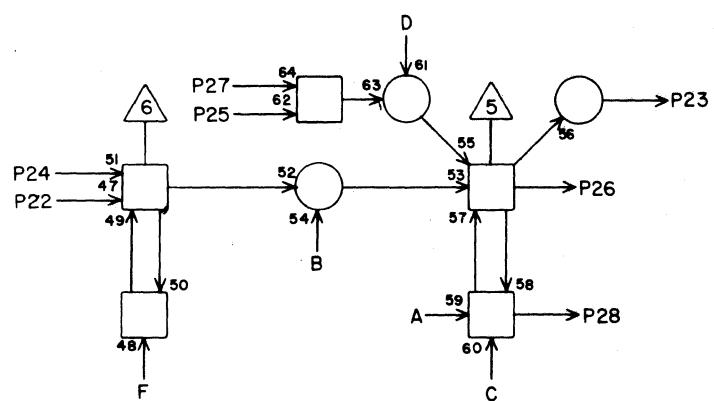
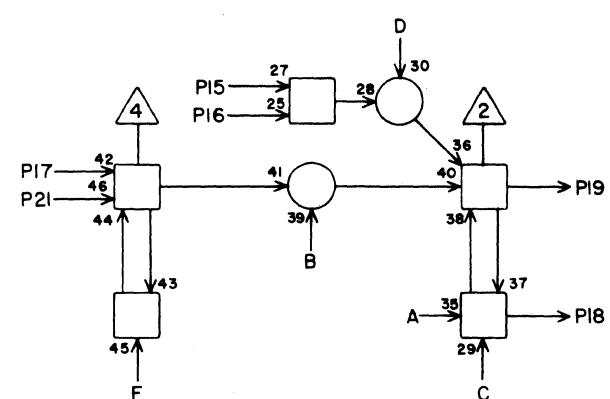
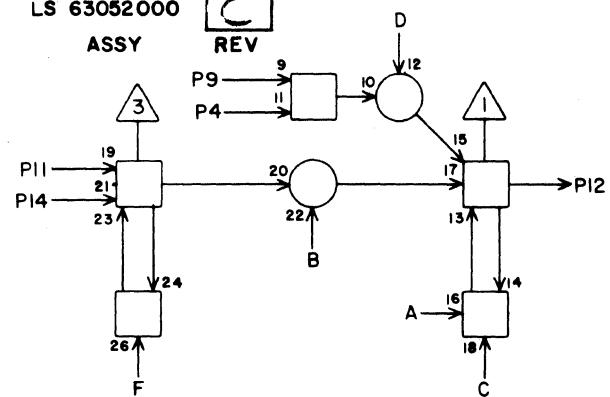
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

LS 63052000 ASSY REV C

JW

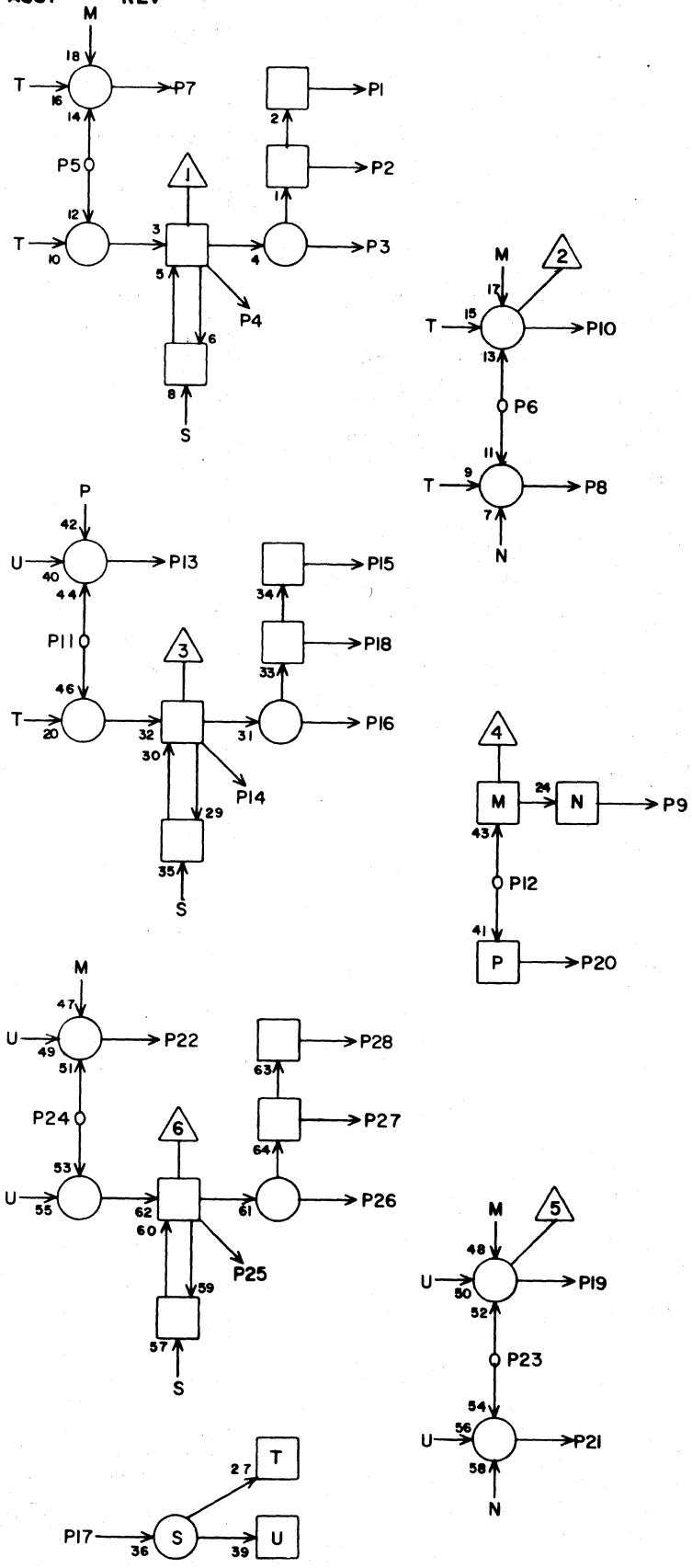


JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. K

LS 63052100 D
ASSY REV



JX

	JACK	PIN	LG
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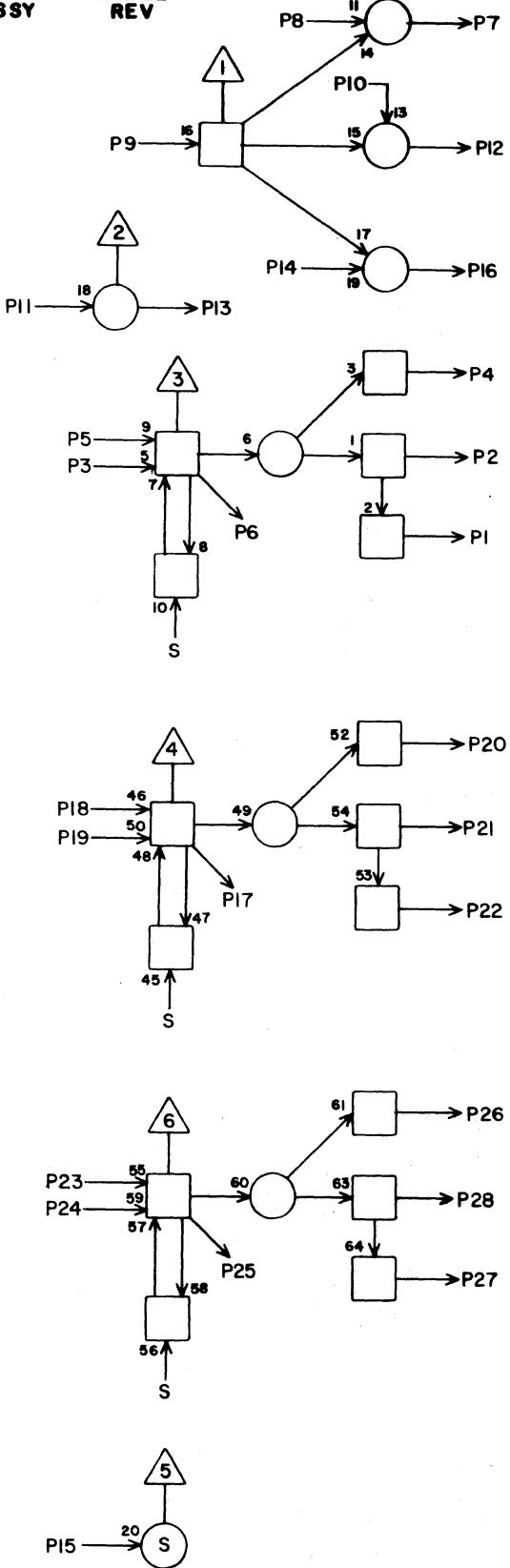
CIRCUIT SPECIFICATION 11827600

60042700 Rev. P

LS 63052200
ASSY

D
REV

JY



	JACK	PIN	LG
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CIRCUIT SPECIFICATION II827600

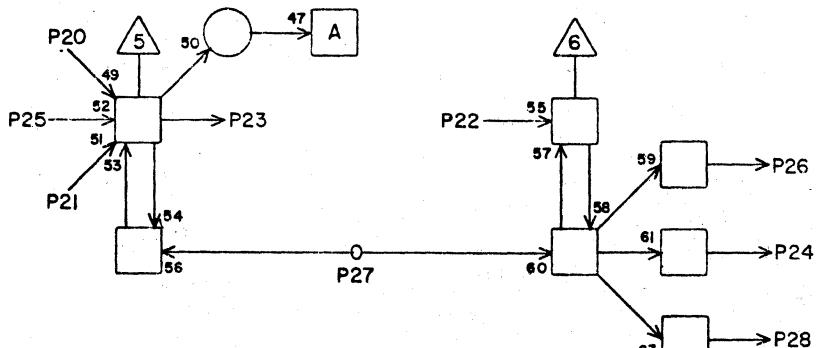
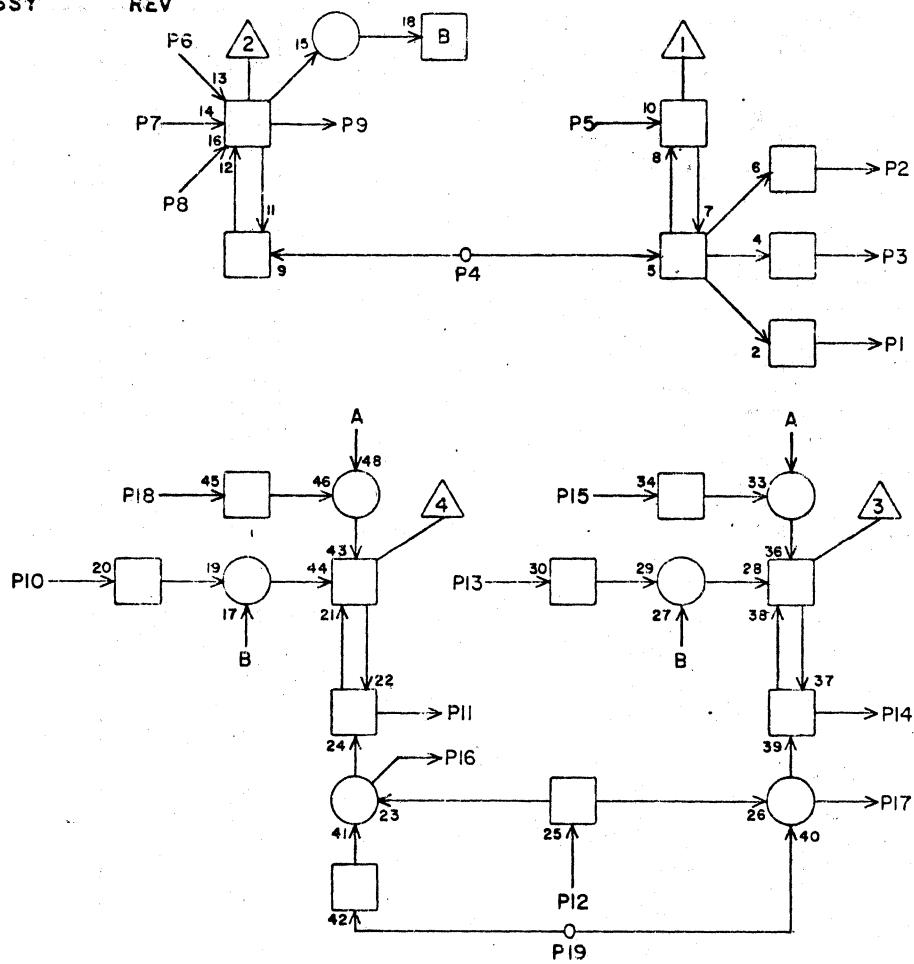
60042700 Rev. J

LS 63052300

ASSY

C
REV

JZ



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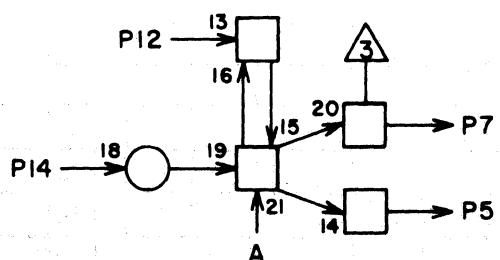
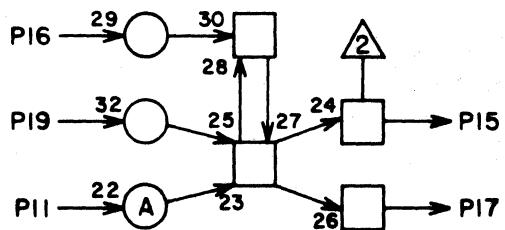
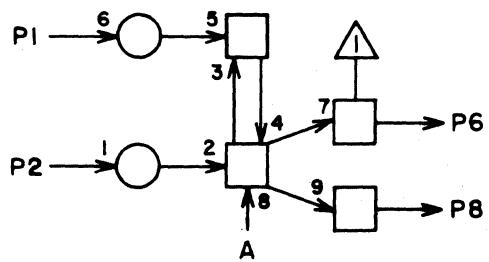
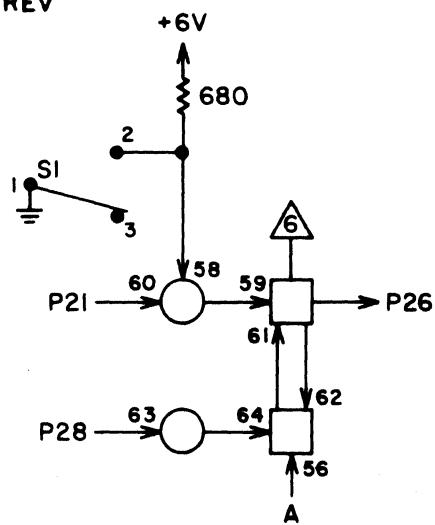
JACK PIN LG

CIRCUIT SPECIFICATION 11827600

60042700 Rev. J

LS 18377800 C
ASSY REV

JOO



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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev. R

LS17773900

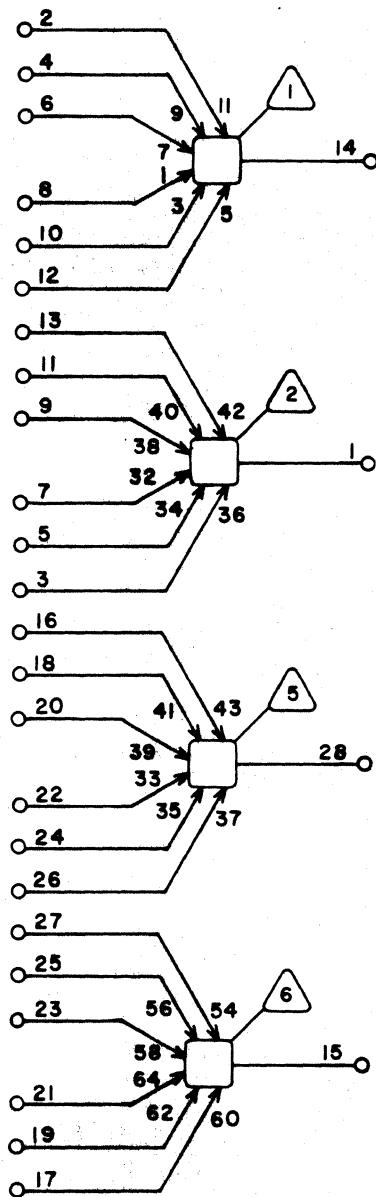
A

REV

JACK

JOI

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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60042700 Rev. K

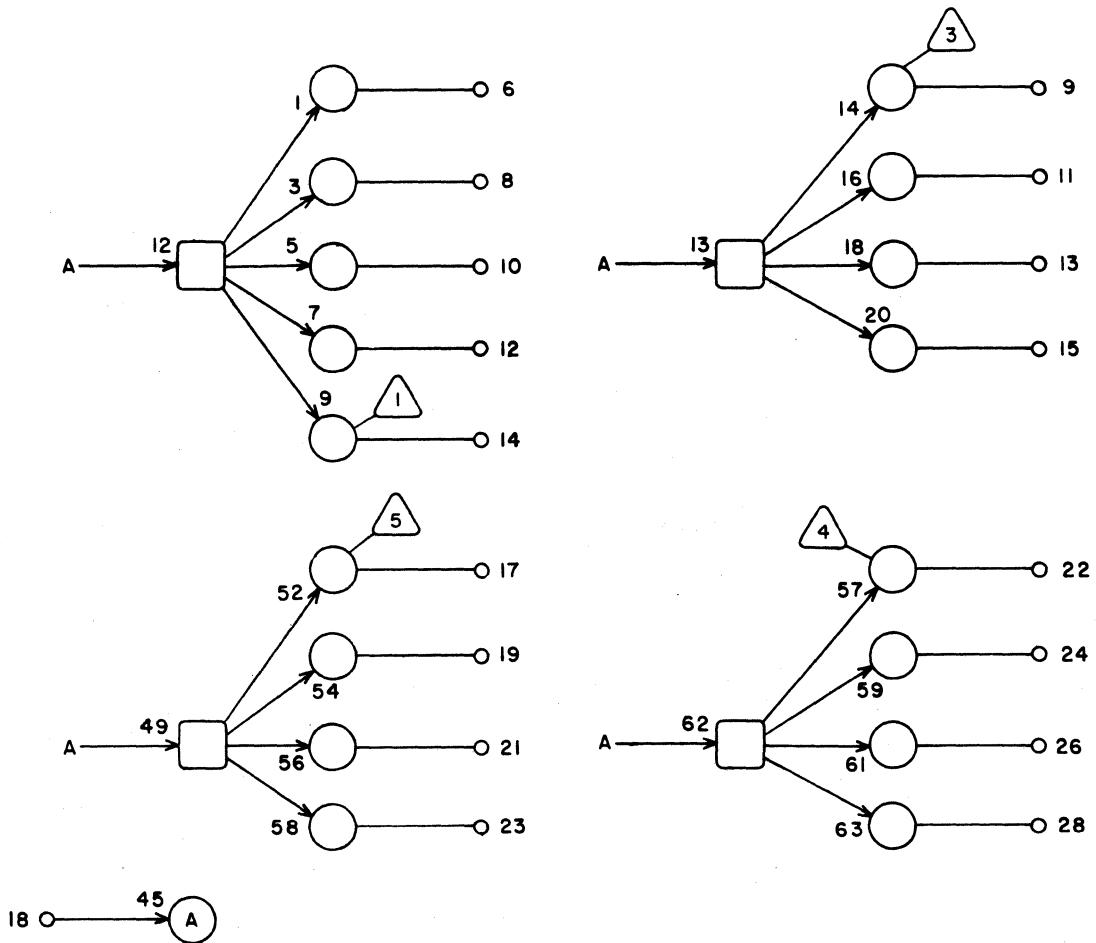
LS 17774000

B
REV

JACK

JO2

CIRCUIT SPECIFICATION 11827600



60042700 Rev. K

PIN JACK PIN LG

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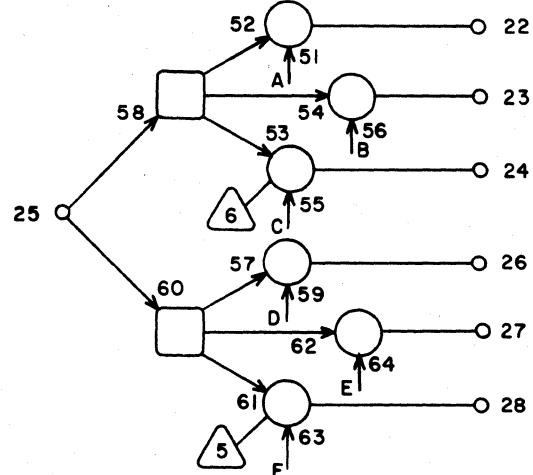
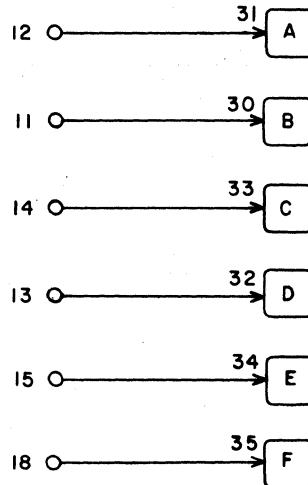
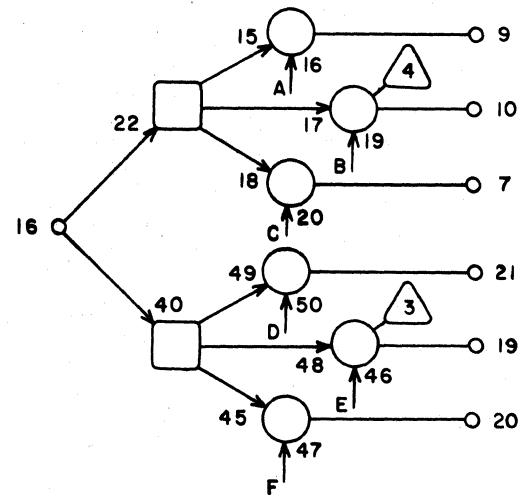
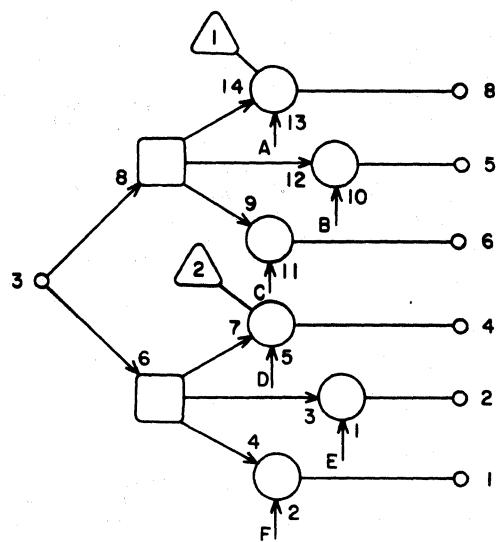
LS 17774100

B
REV

JACK

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J03

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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60042700 Rev. K

LS 17774200

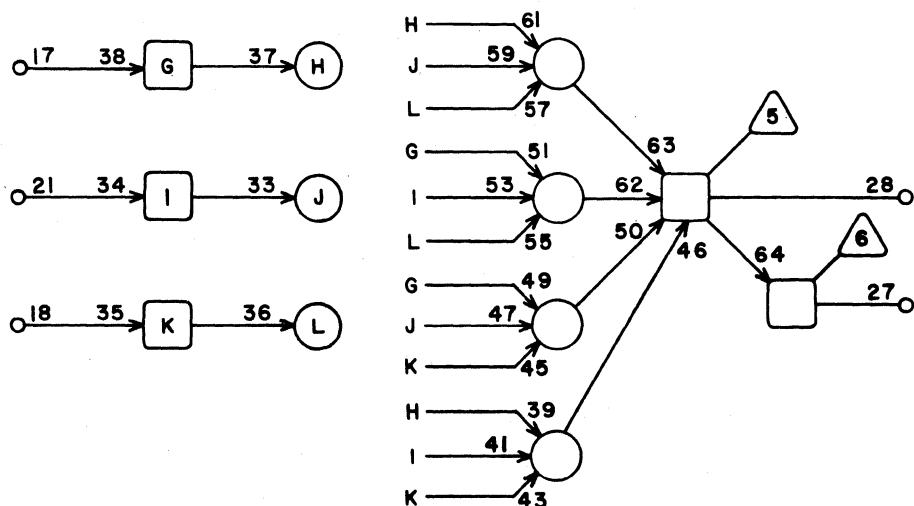
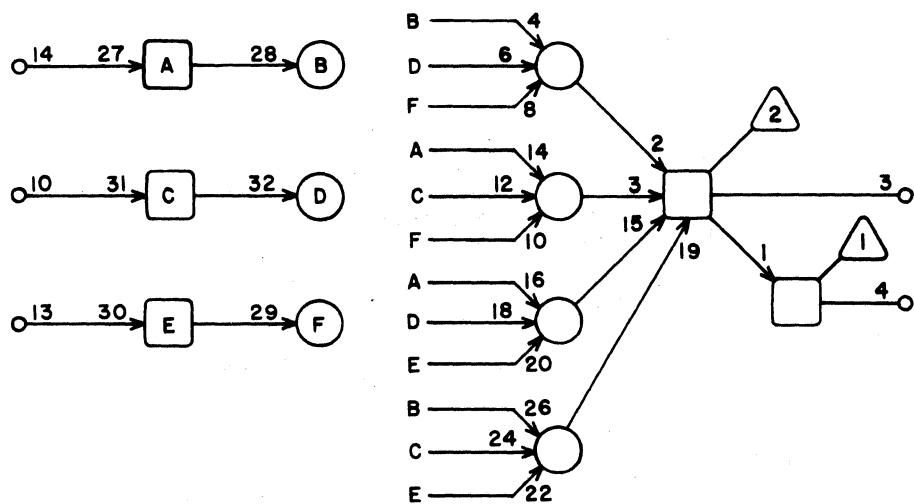
B

REV

JACK

JO4

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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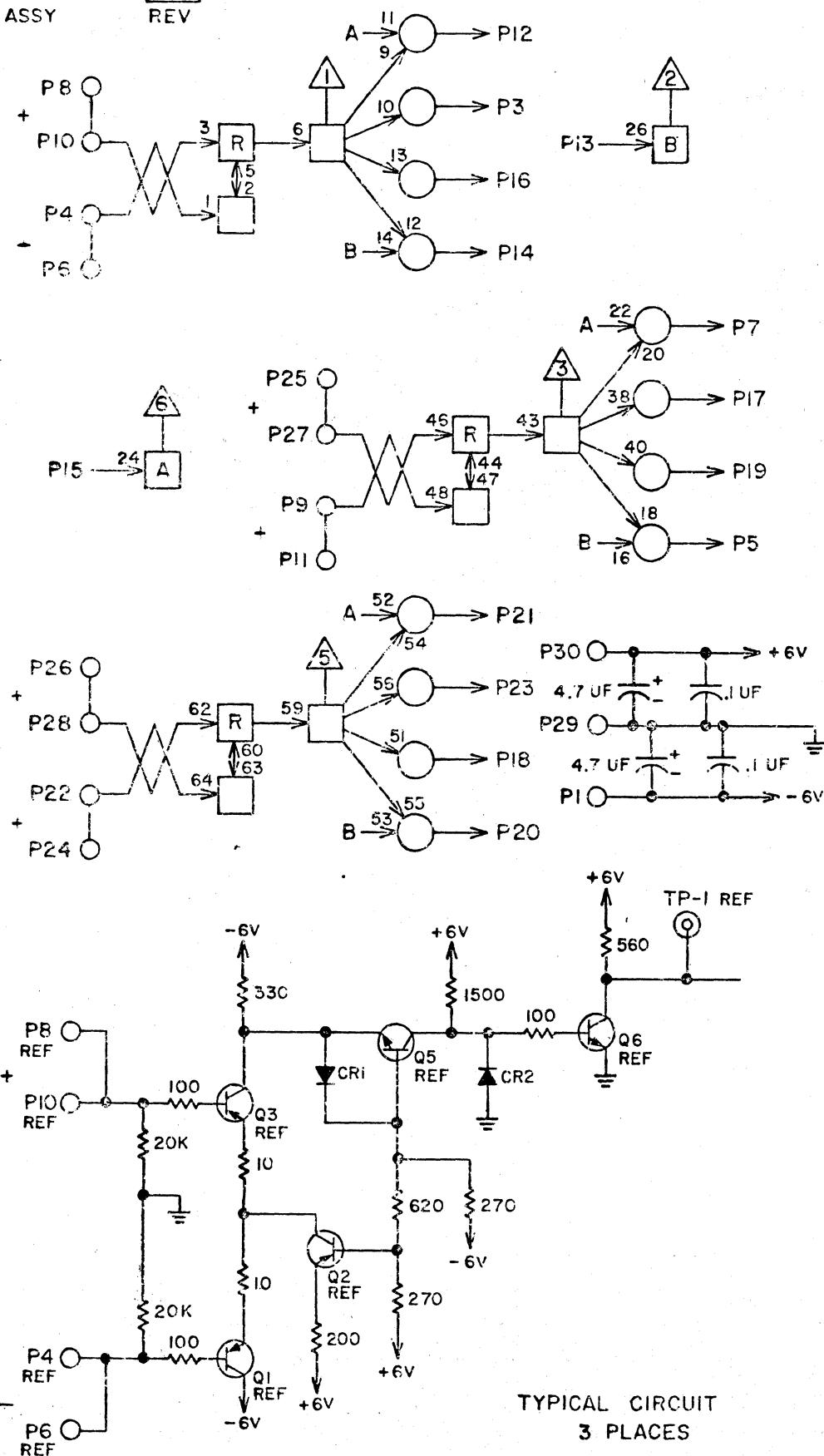
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60042700 Rev. K

LS 18446500
ASSY

E
REV

J05



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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
52000006

60042700 Rev. T

LS 17774400

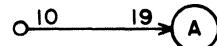
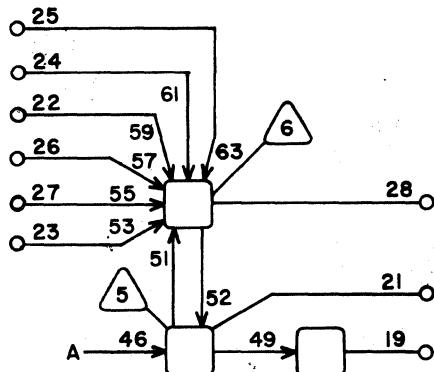
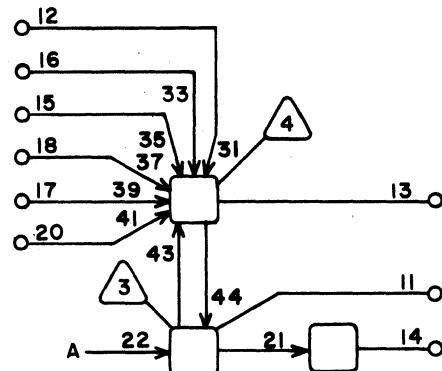
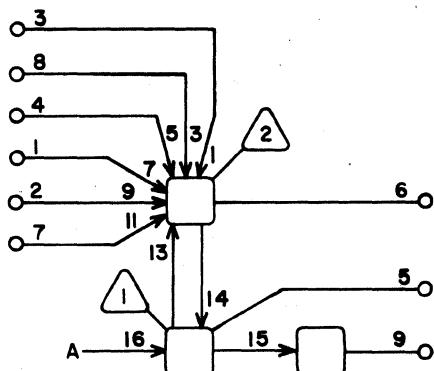
B

REV

JACK

JO6

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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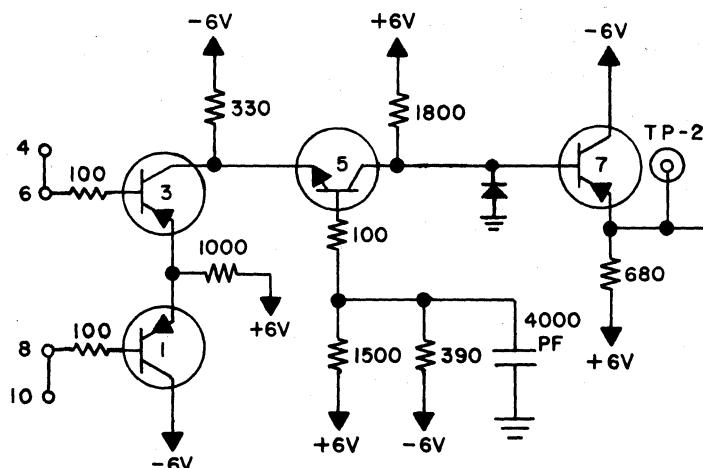
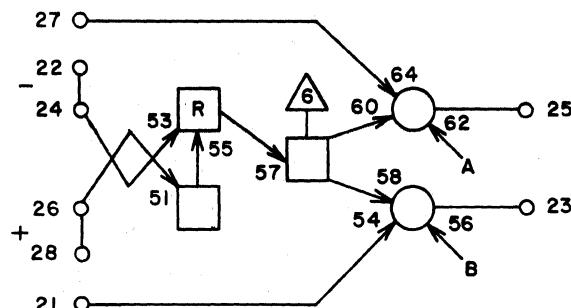
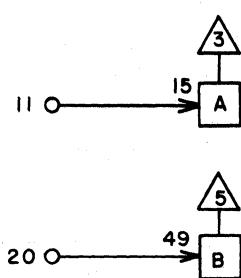
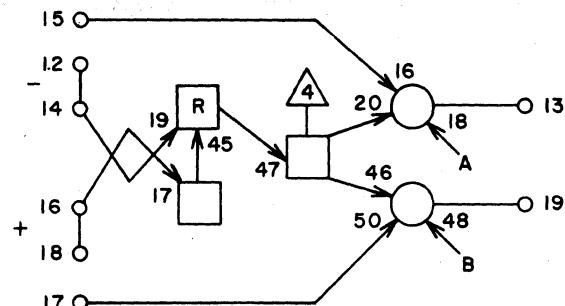
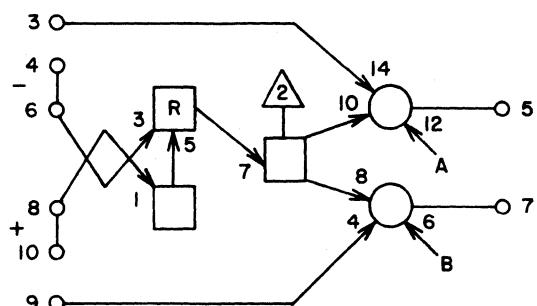
60042700 Rev. K

LS 18446700

C
REVCIRCUIT SPECIFICATION 11827600
52000005

JACK

J07



60042700 Rev R

PIN	JACK	PIN	LG
1	-6V		
2	GRD		
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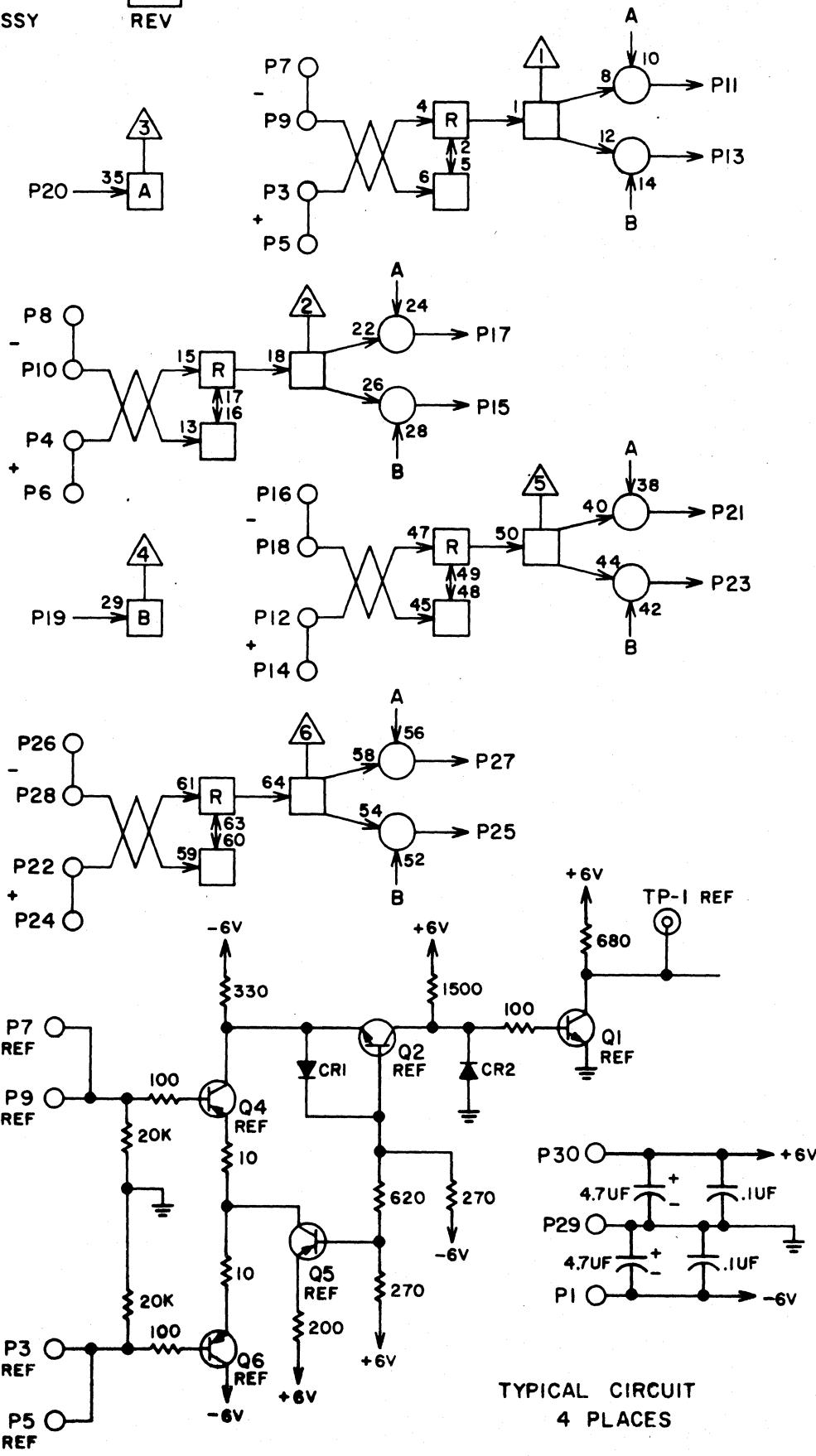
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LS 18446600 E
ASSY REV

J09



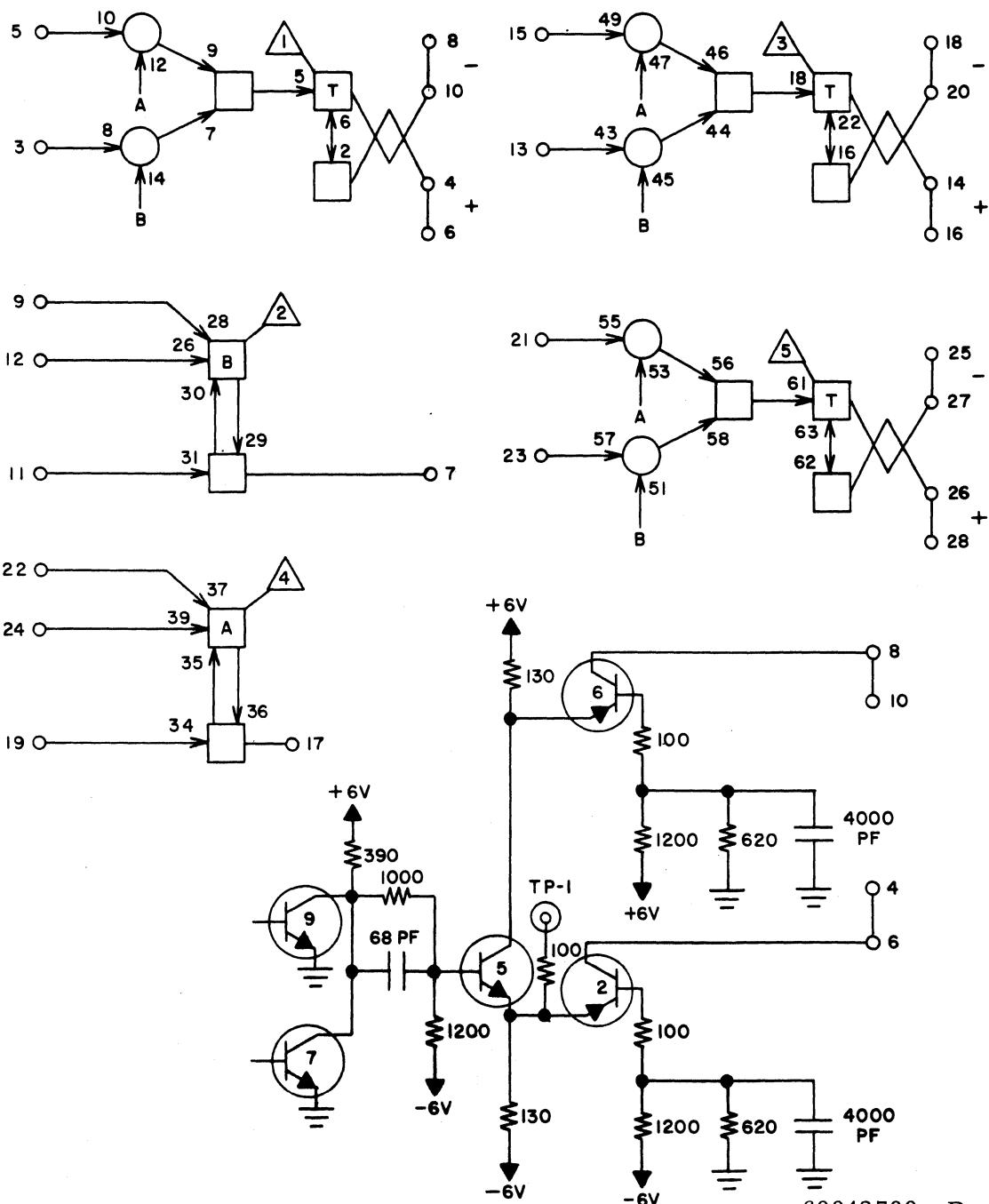
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TYPICAL CIRCUIT
4 PLACES

JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
52000006

60042700 Rev. S

LS 17774700

B
REVCIRCUIT SPECIFICATION 11827600
52000007JACK
J10

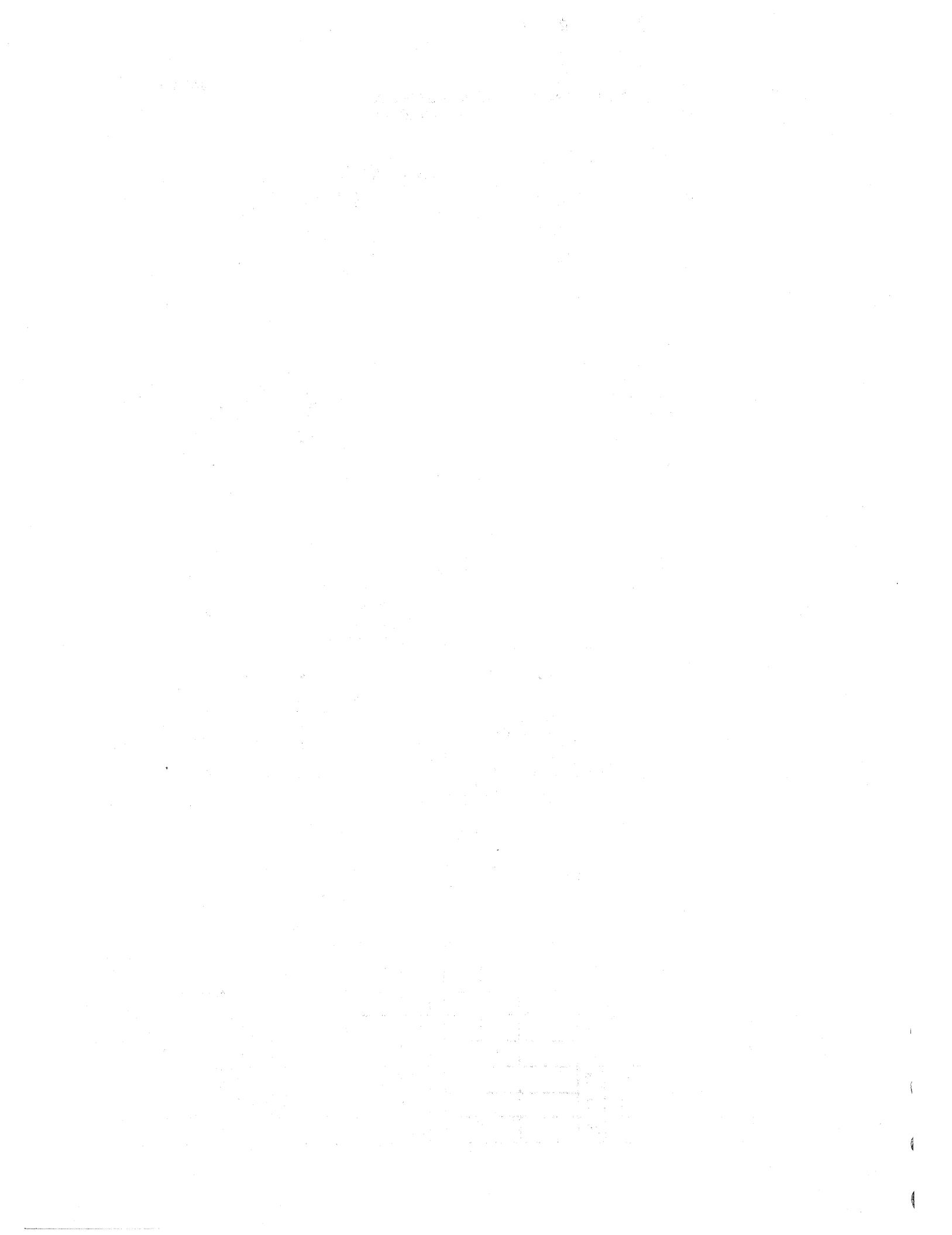
PIN	JACK	PIN	LG
1	-6V		
2	GRD		
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60042700 Rev. K



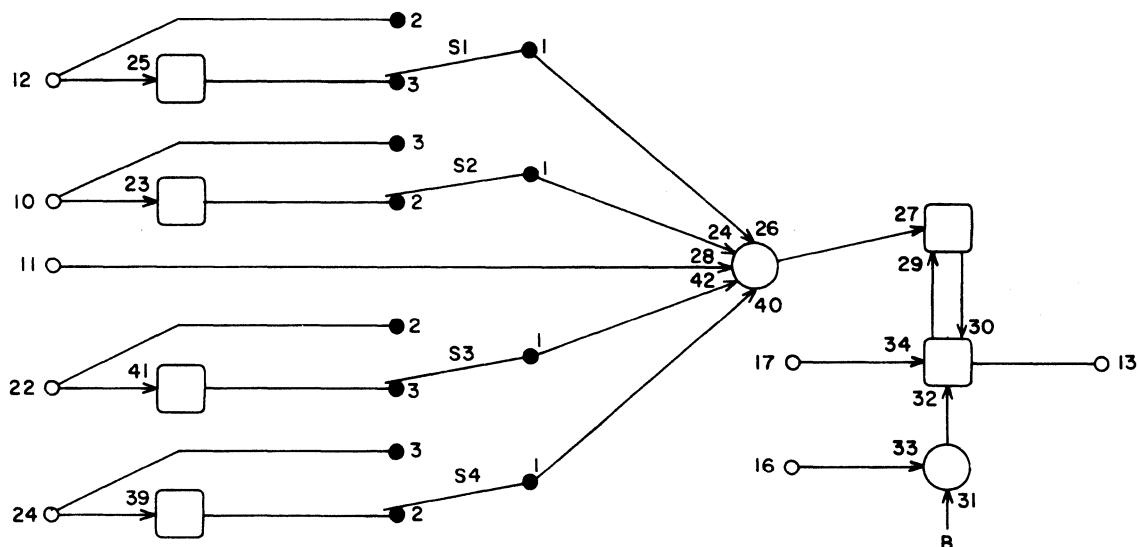
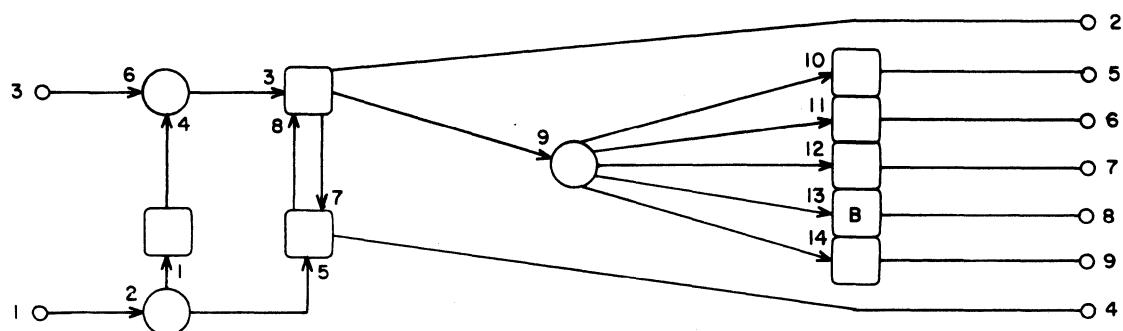
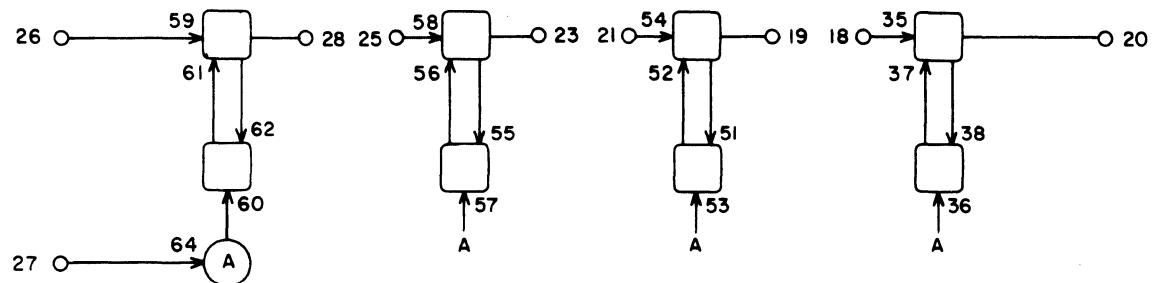
LS 17774900

C
REV

CIRCUIT SPECIFICATION 11827600

JACK

J12



PIN JACK PIN LG

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60042700 Rev. K

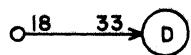
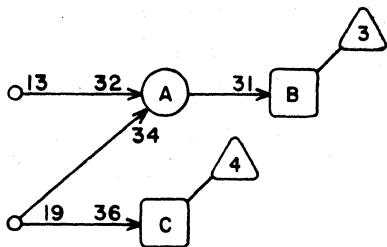
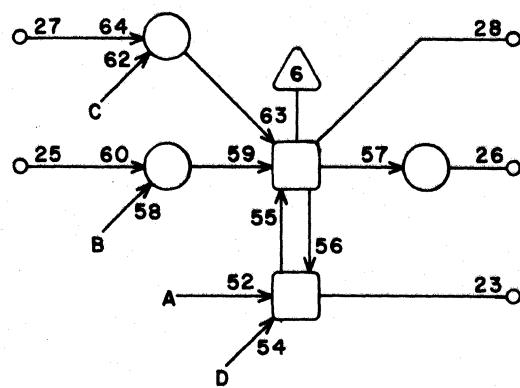
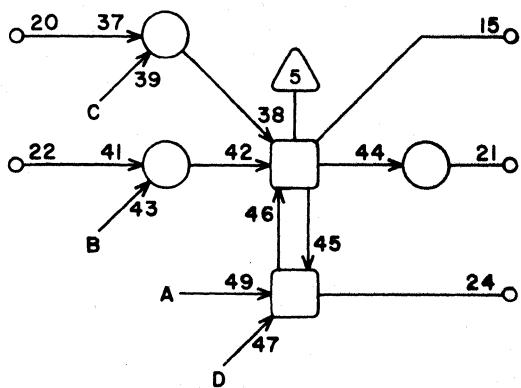
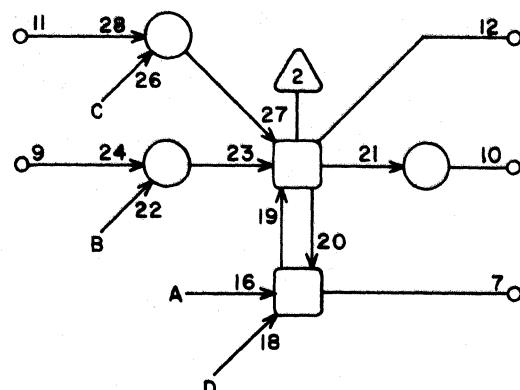
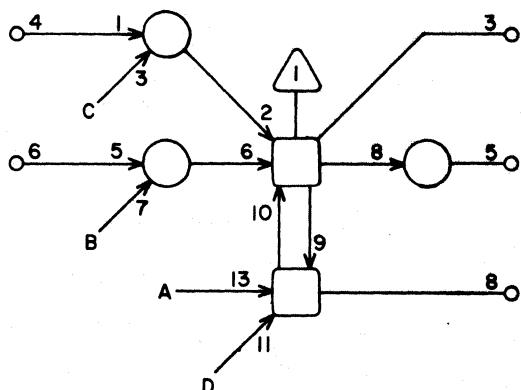
LS 17775000

B
REV

JACK

J13

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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60042700 Rev. K

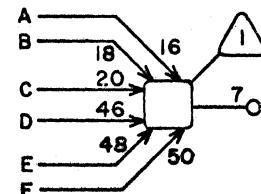
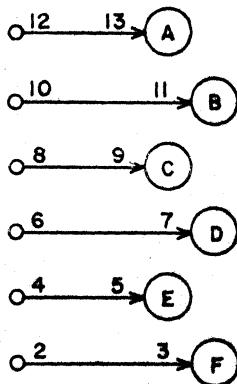
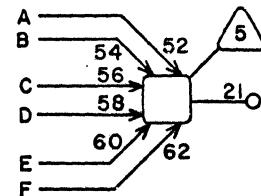
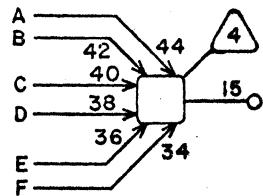
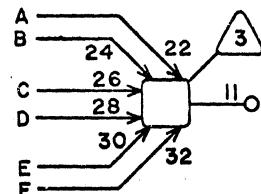
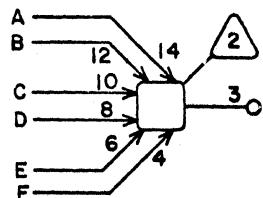


LS 17775200

C
REV

JACK
J15

CIRCUIT SPECIFICATION 11827600



PIN	JACK PIN	LG
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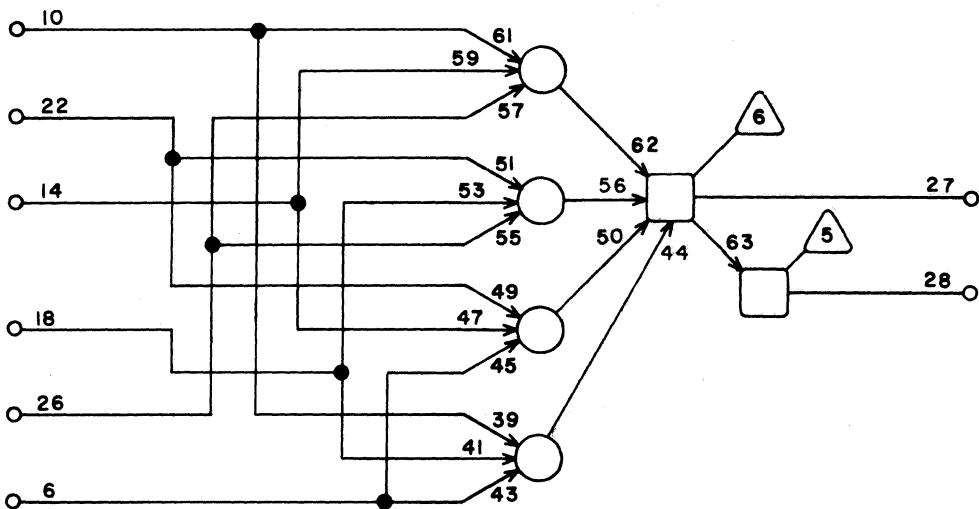
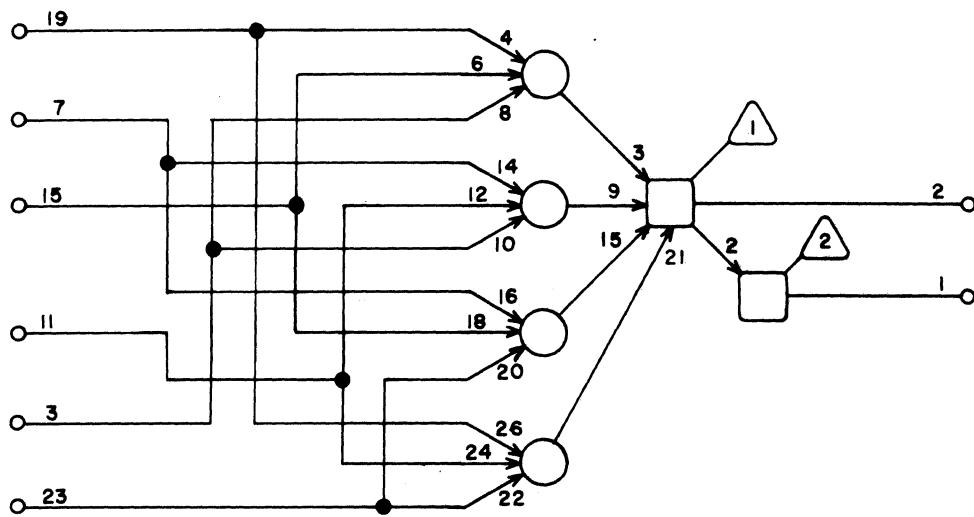
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LS 17775300 B
REV

JACK
J16

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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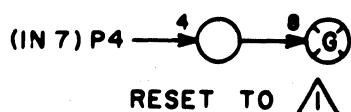
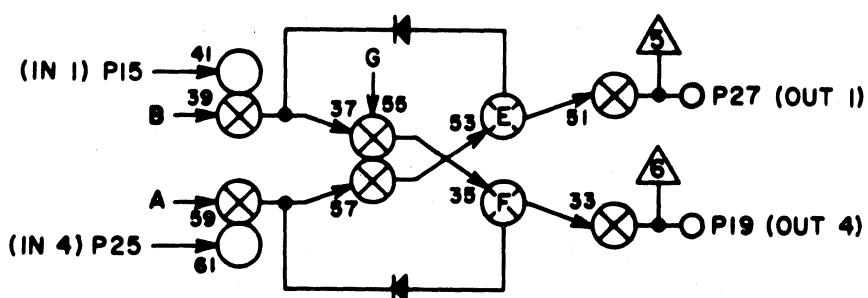
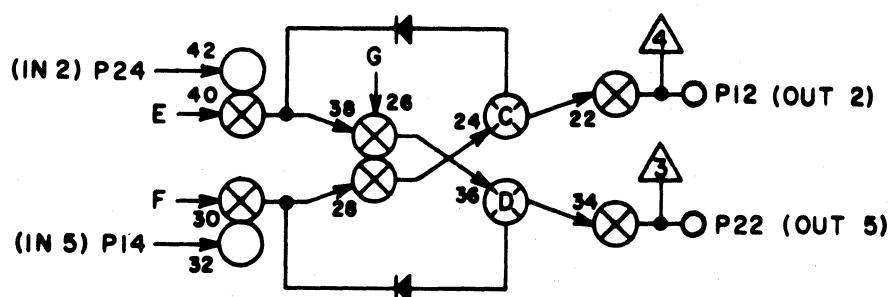
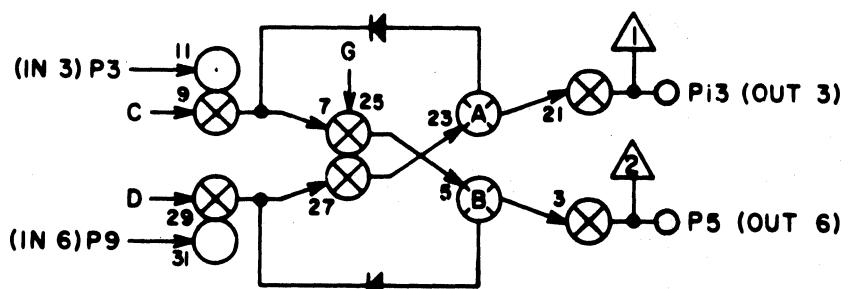
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60042700 Rev. K

LS18323200 E
ASSY REV

J17

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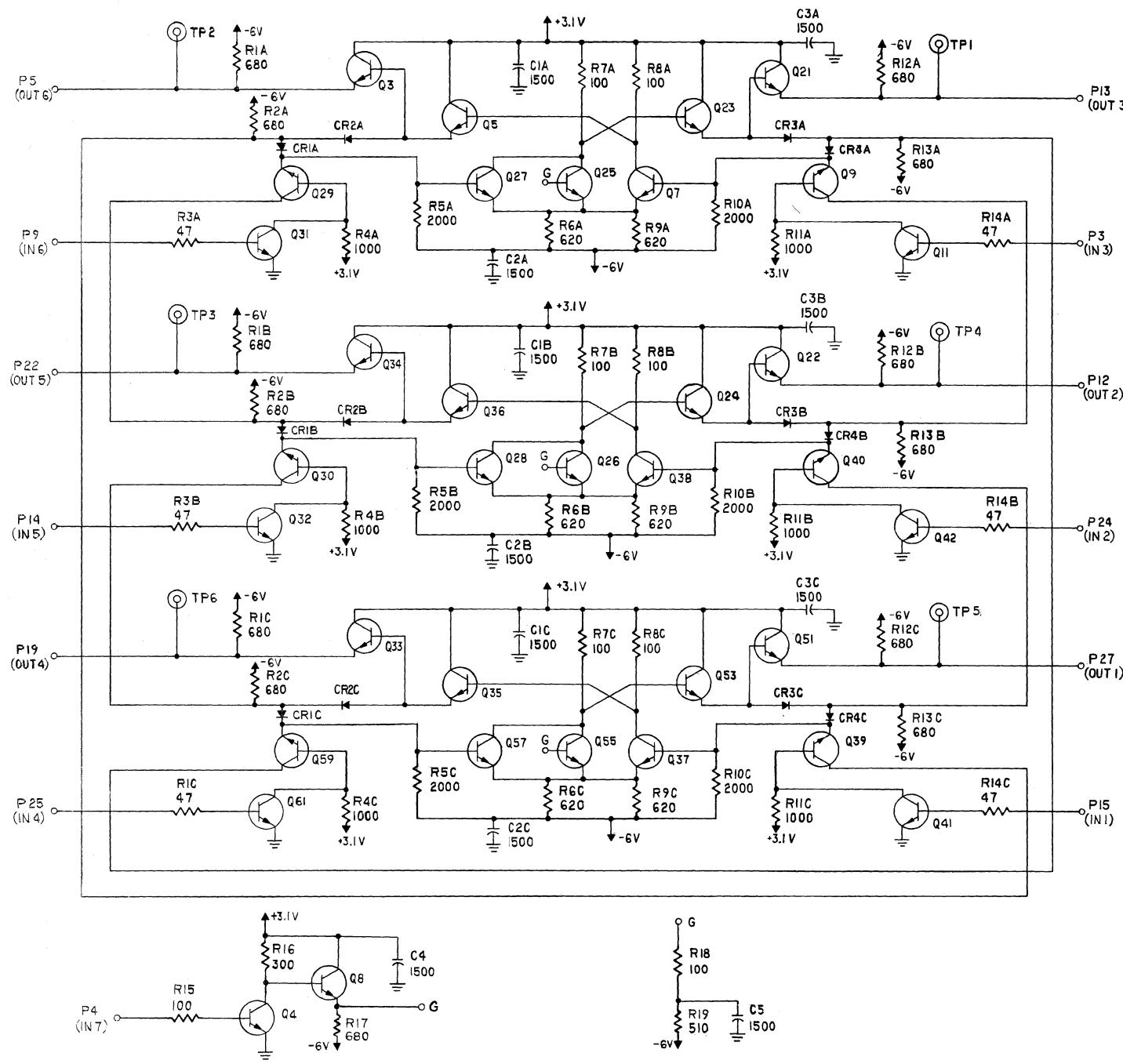


1	-6V	
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28	+3.1V	

FOR SCHEMATIC SEE DRAWING 18323400

JACK PIN LG
SEE CIRCUIT SPECIFICATION

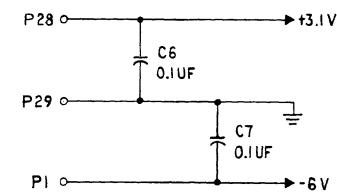
52000003
60042700 Rev. P



NOTES:

- I. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCES ARE IN OHMS.
ALL CAPACITANCES ARE IN PF.
ALL RESISTORS ARE 1/8 W, $\pm 5\%$.
ALL CAPACITORS ARE $\pm 25\%$.
ALL TRANSISTORS ARE 24561900.
ALL DIODES ARE 17814100.

2. REFERENCE DRAWINGS:
ASSEMBLY 18323200.
BOARD 18325300.



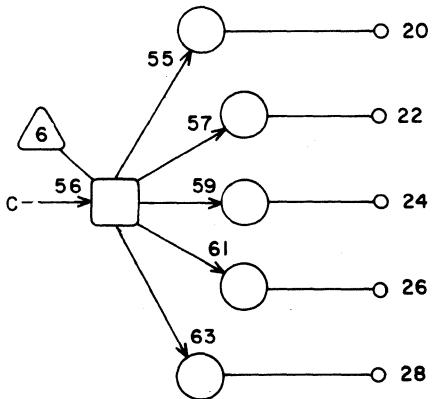
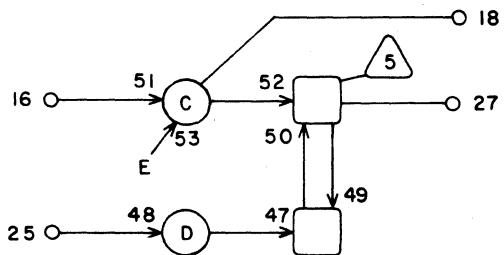
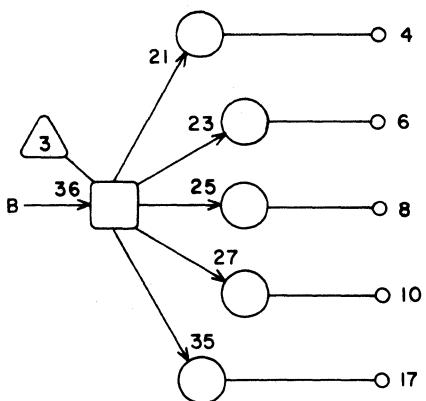
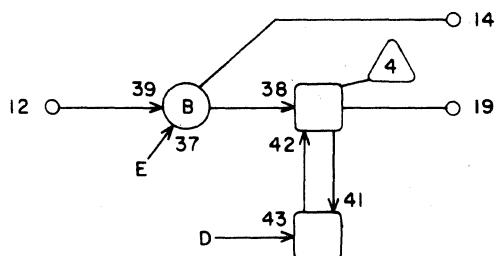
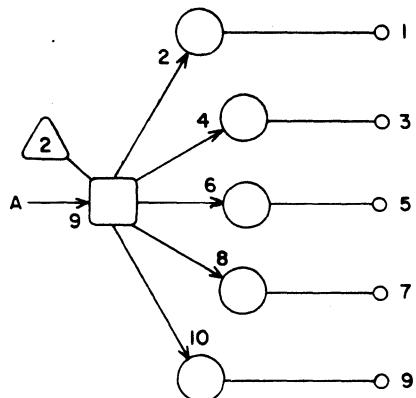
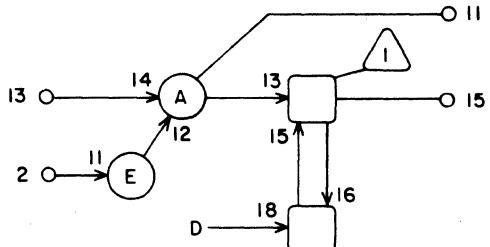


LS 17775500

B
REV

JACK
J18

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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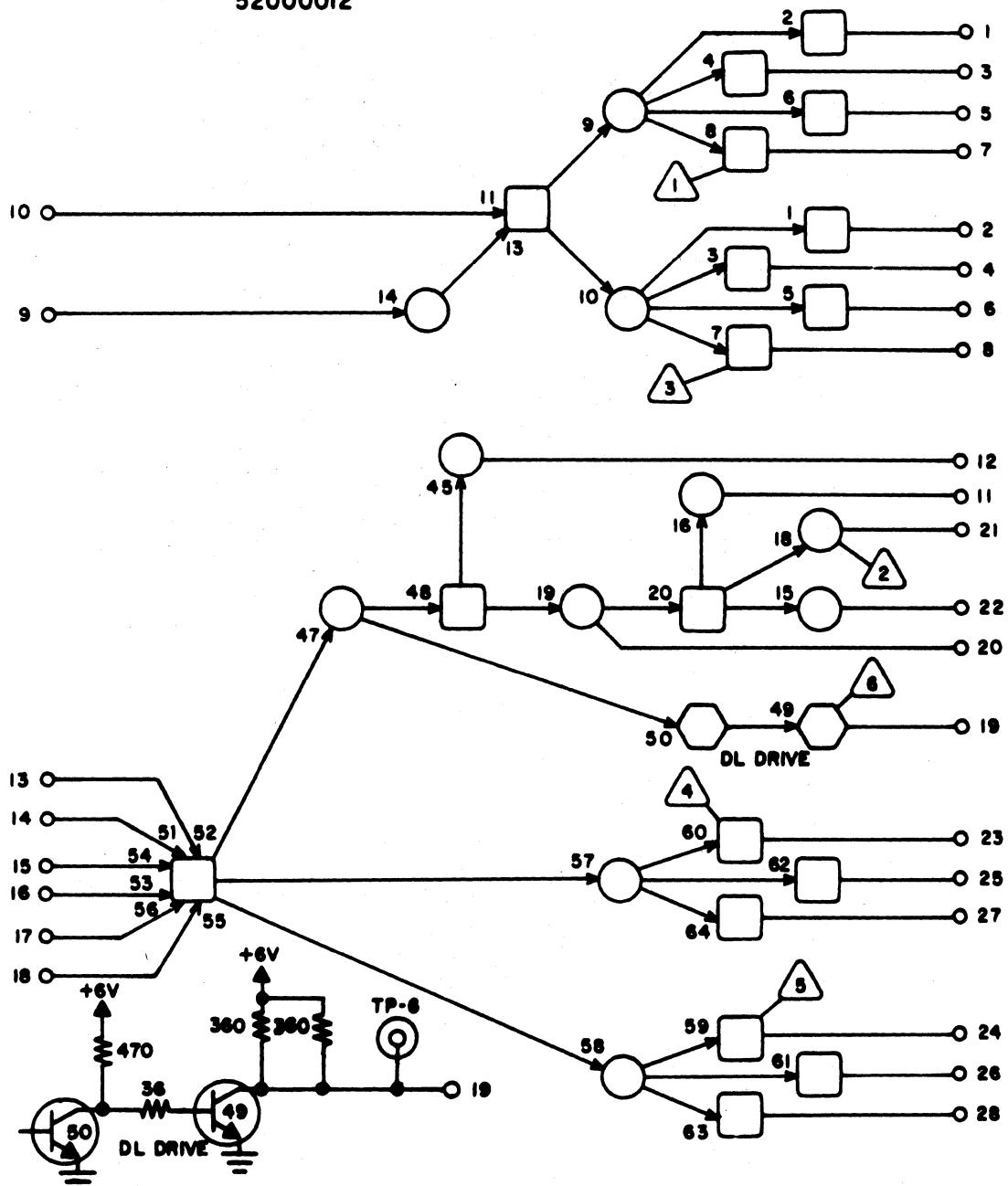
60042700 Rev. K

LSI7775600

C
REV

JACK

**CIRCUIT SPECIFICATION 11827600
52000012**



PIN JACK PIN LG

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60042700 Rev. P

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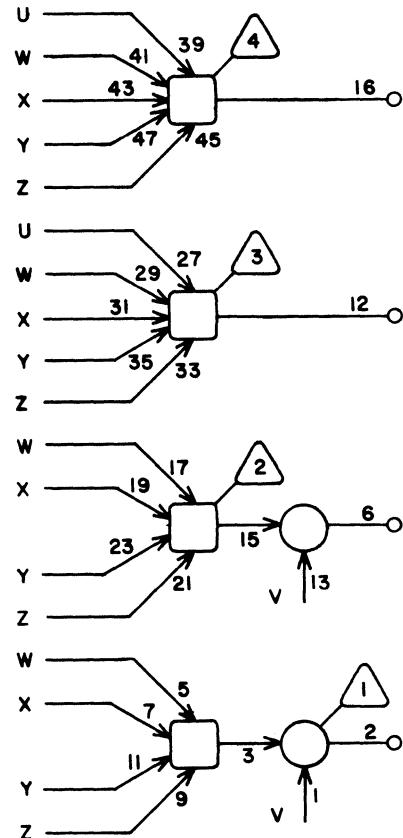
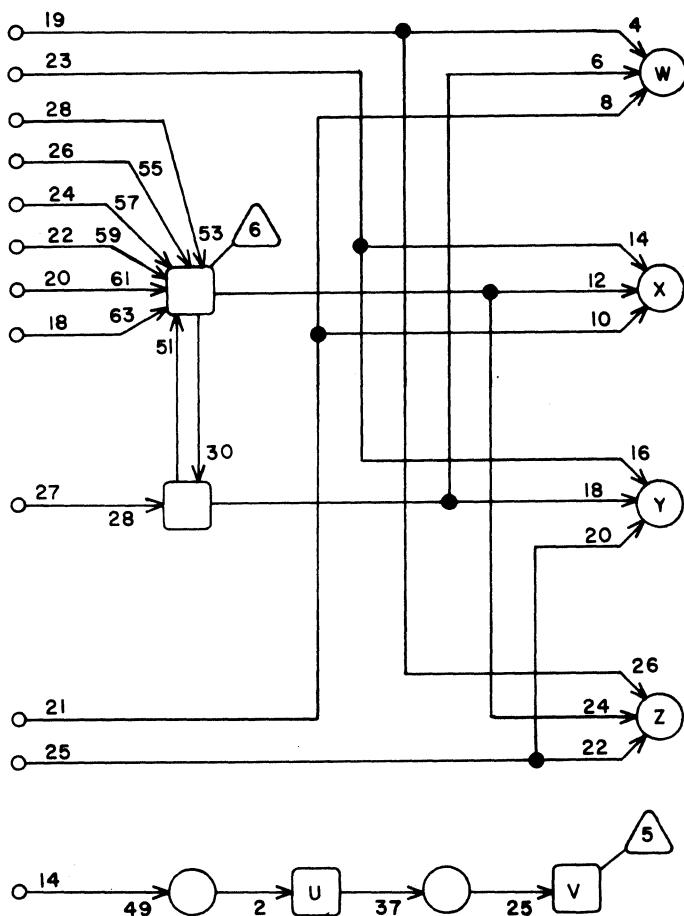
LS 17775700

B
REV

JACK

J20

CIRCUIT SPECIFICATION 11827600



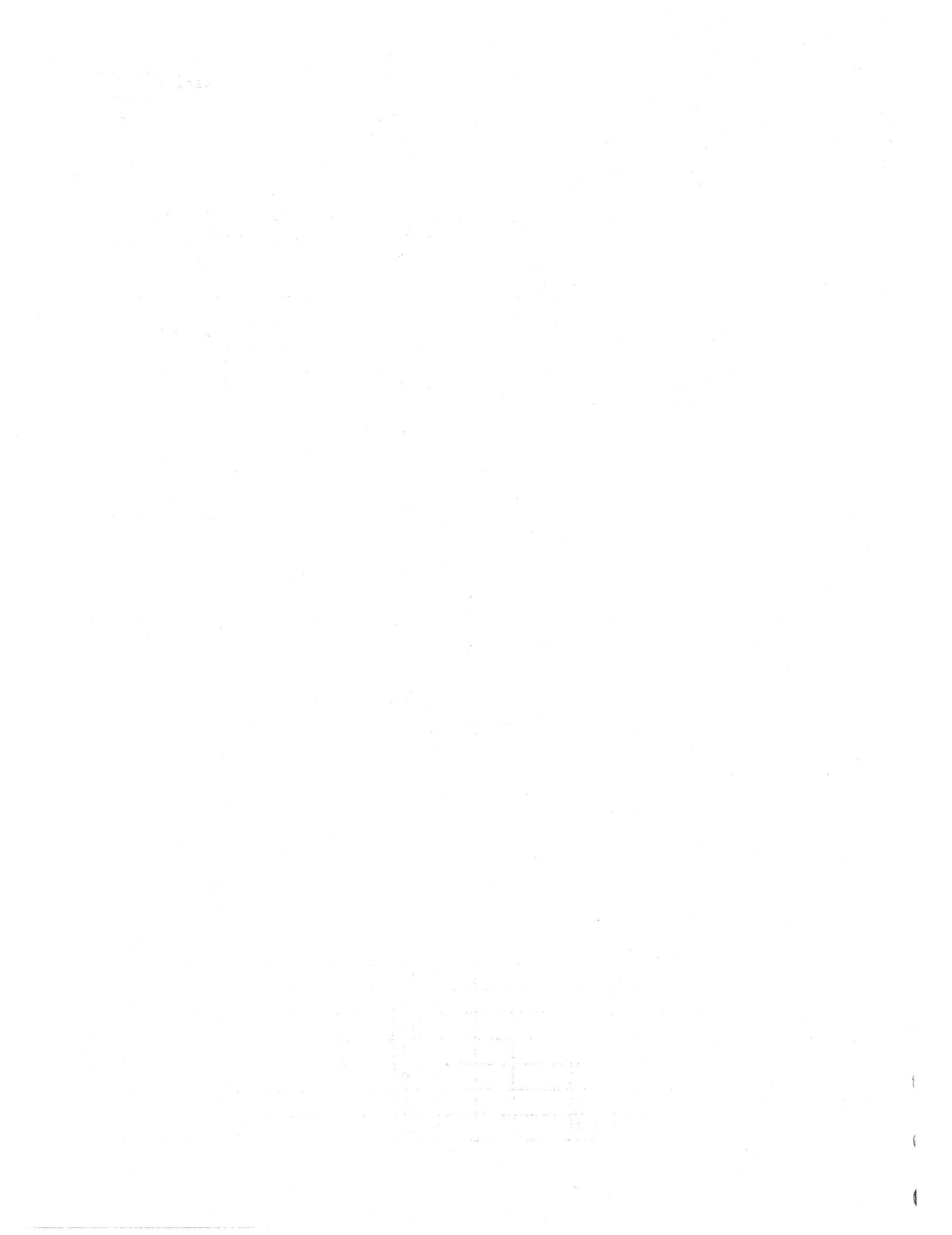
60042700 Rev. K

PIN	JACK	PIN	LG
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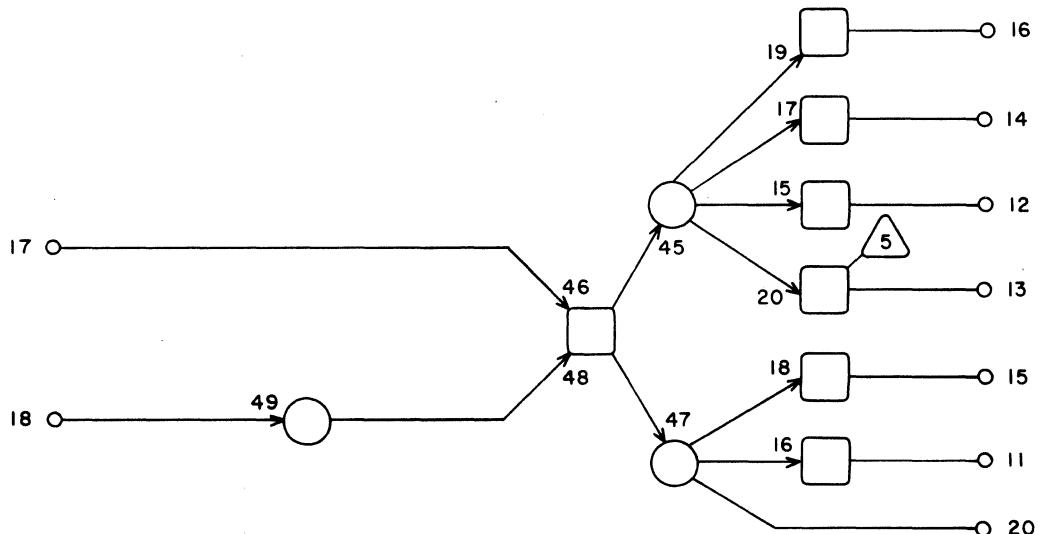
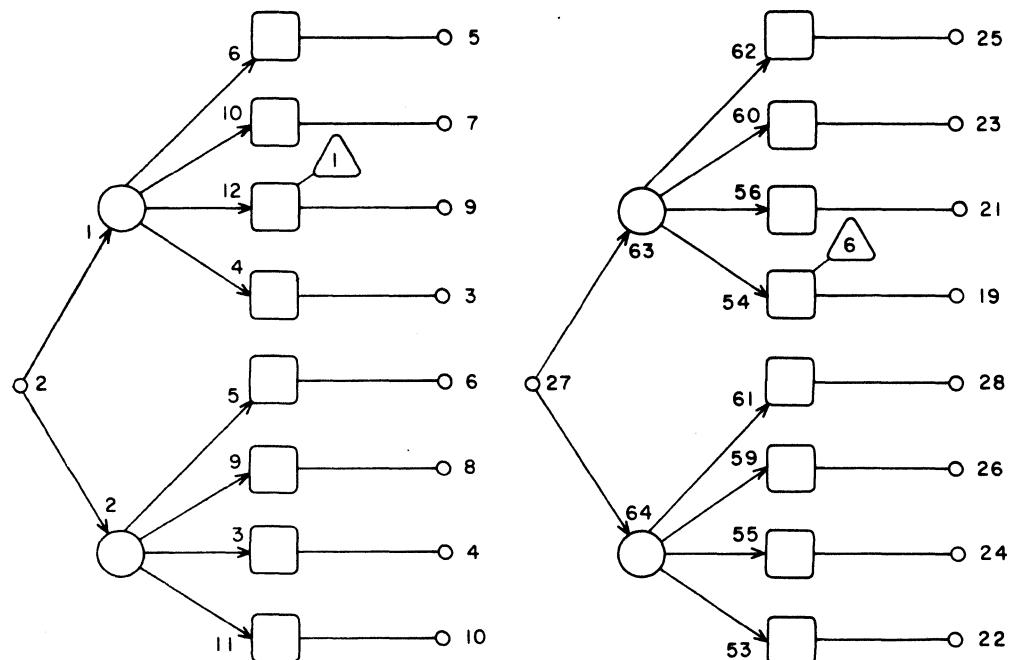
LS 17775900

B
REV

JACK

J22

CIRCUIT SPECIFICATION 11827600



PIN JACK PIN LG

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60042700 Rev. K

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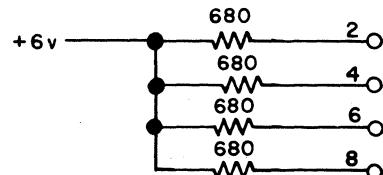
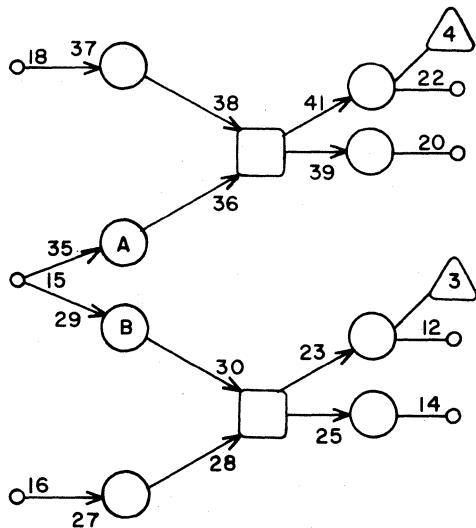
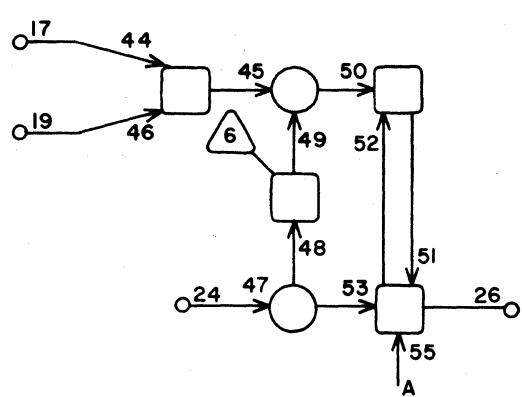
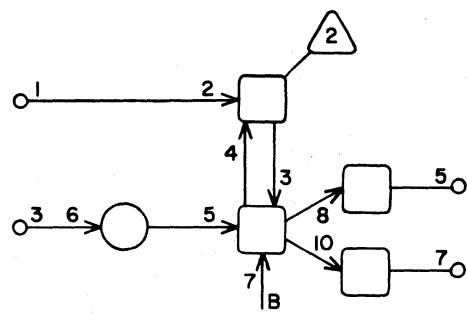
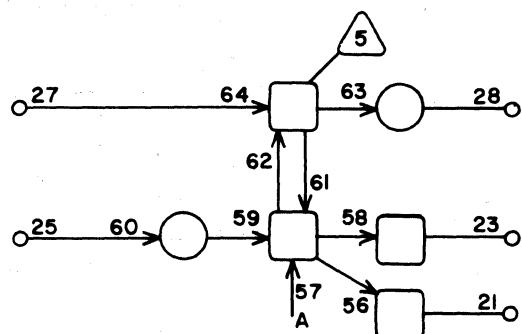
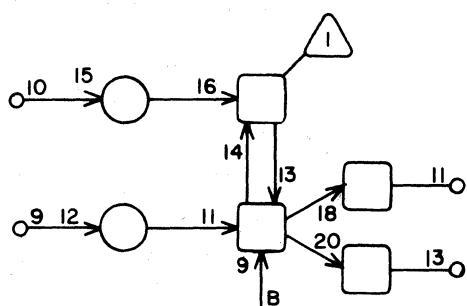
LSI7776000

B
REV

JACK

J23

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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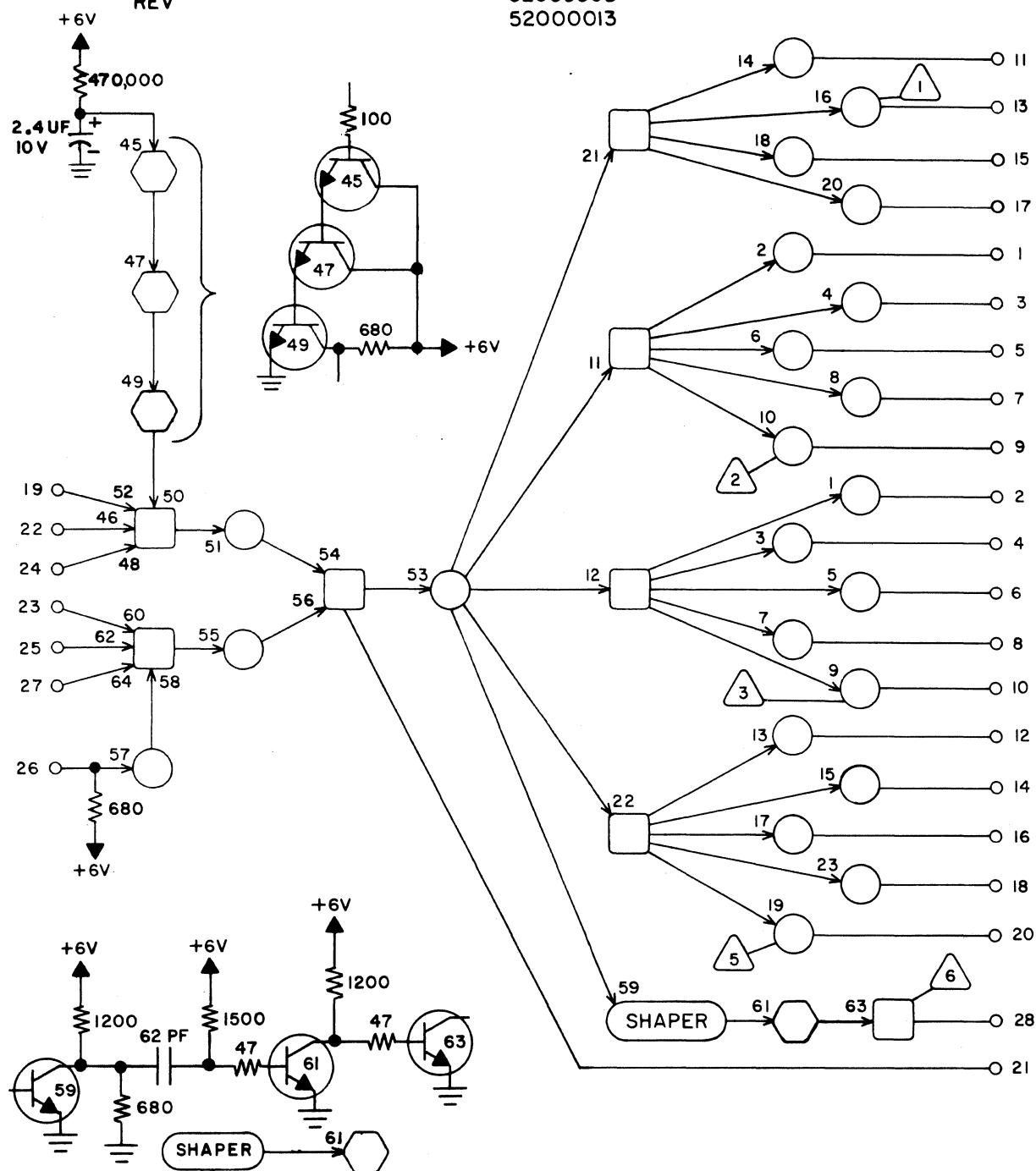
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60042700 Rev. K

LS17776100

B
REV

CIRCUIT SPECIFICATION

11827600
52000008
52000013JACK
J24

60042700 Rev. K

PIN	JACK	PIN	LG
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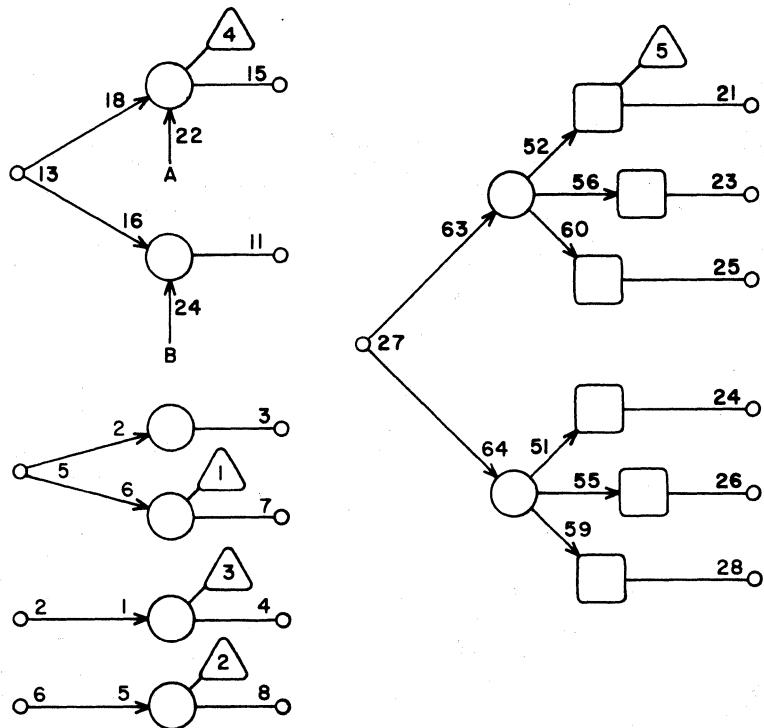
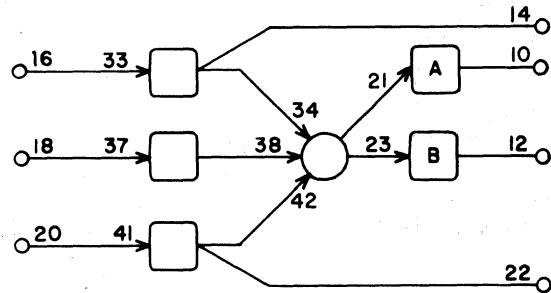
LS 17776200

B
REV

JACK

J25

CIRCUIT SPECIFICATION 11827600



PIN	JACK	PIN	LG
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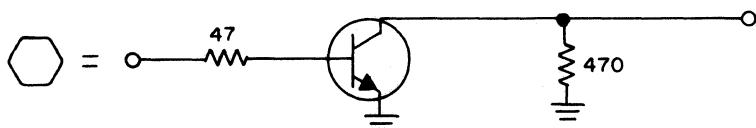
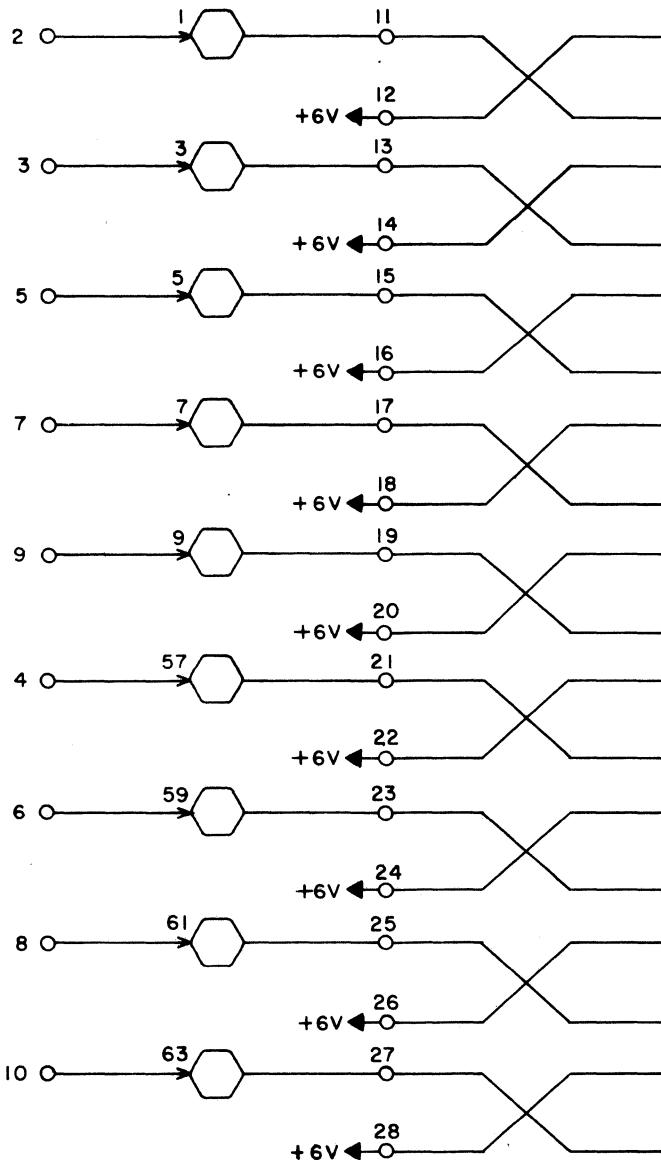
60042700 Rev. K

LS 17776300

B
REV

CIRCUIT SPECIFICATION 52000009

JACK

[]
J26

PIN JACK PIN LG

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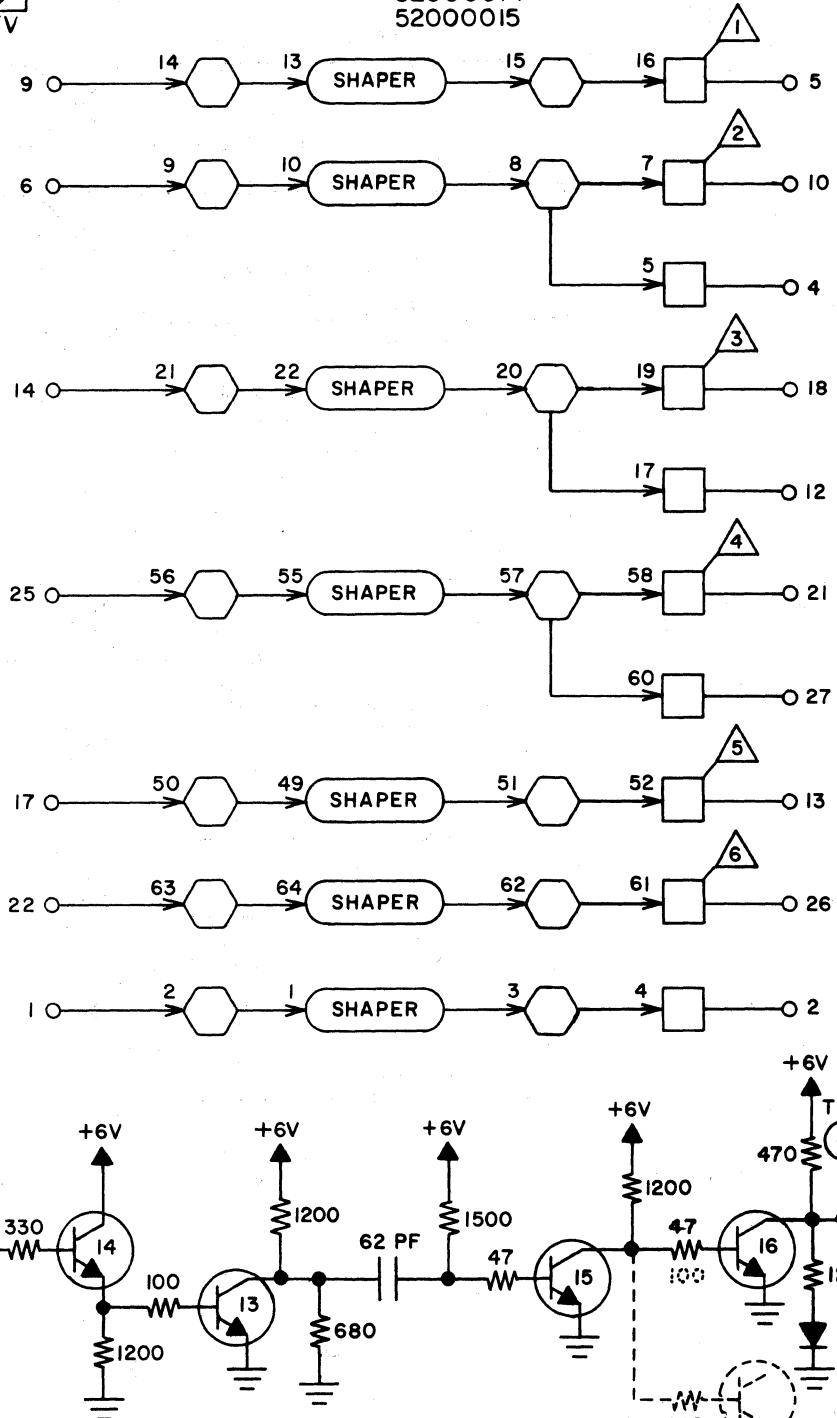
60042700 Rev. K

LS17776400

B
REV

CIRCUIT SPECIFICATION
52000008
52000014
52000015

JACK
J27



PIN	JACK	PIN	LG
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60042700
Rev. K

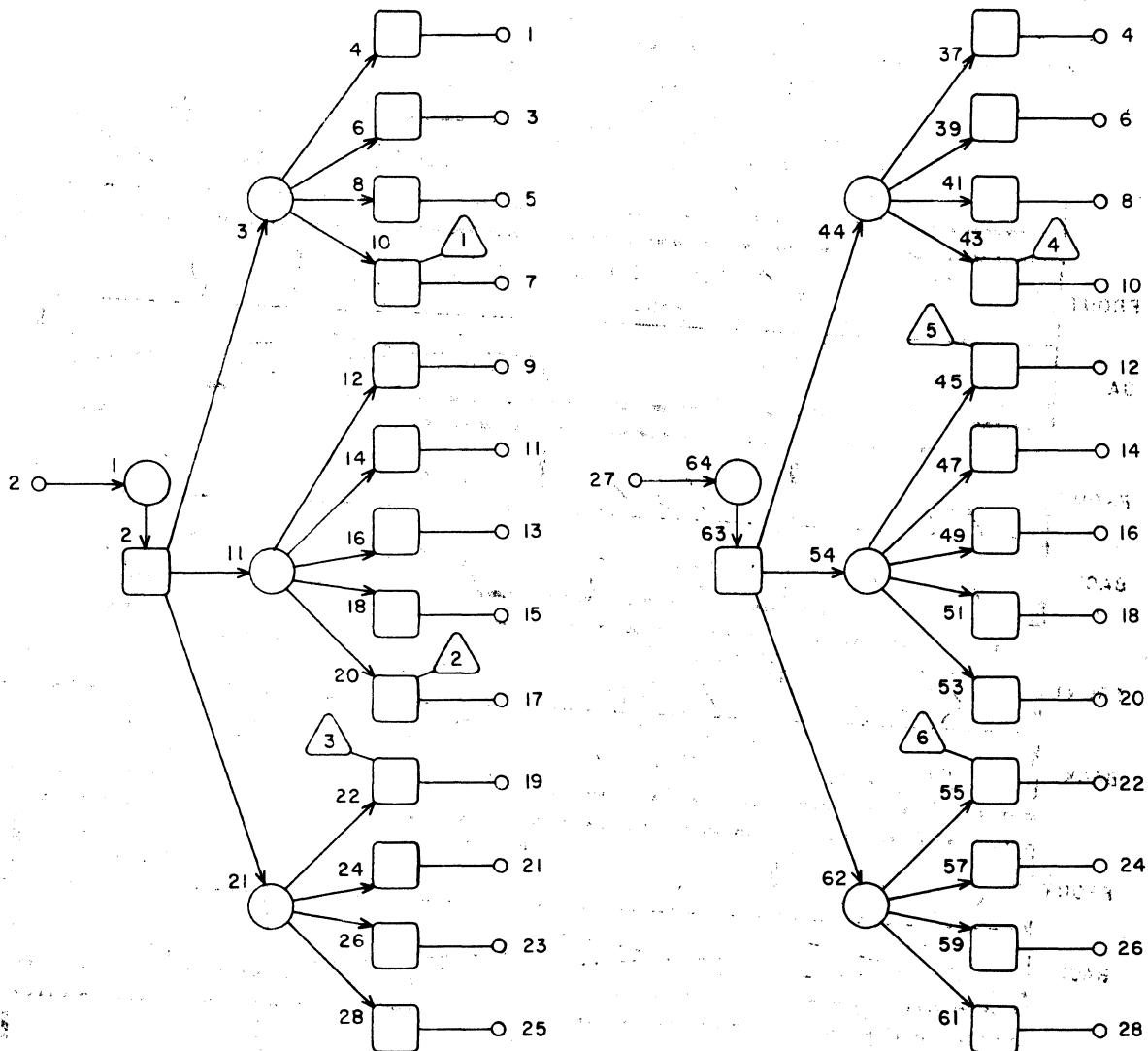
LS 17776500

C
REV

JACK

J28

CIRCUIT SPECIFICATION 11827600



PIN JACK PIN LG

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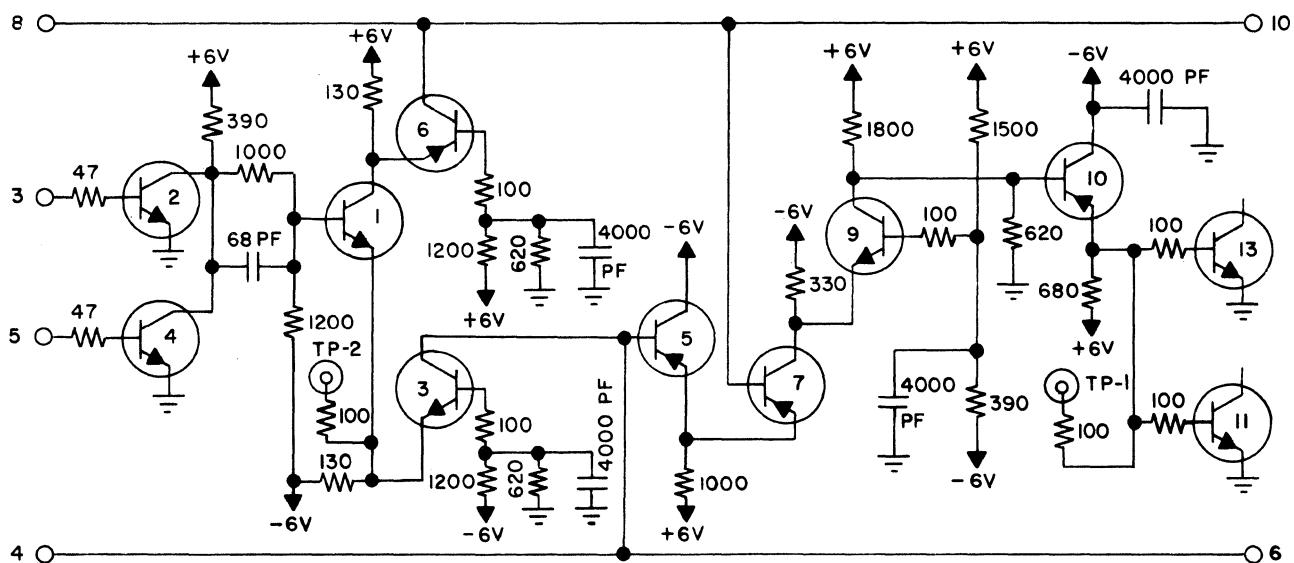
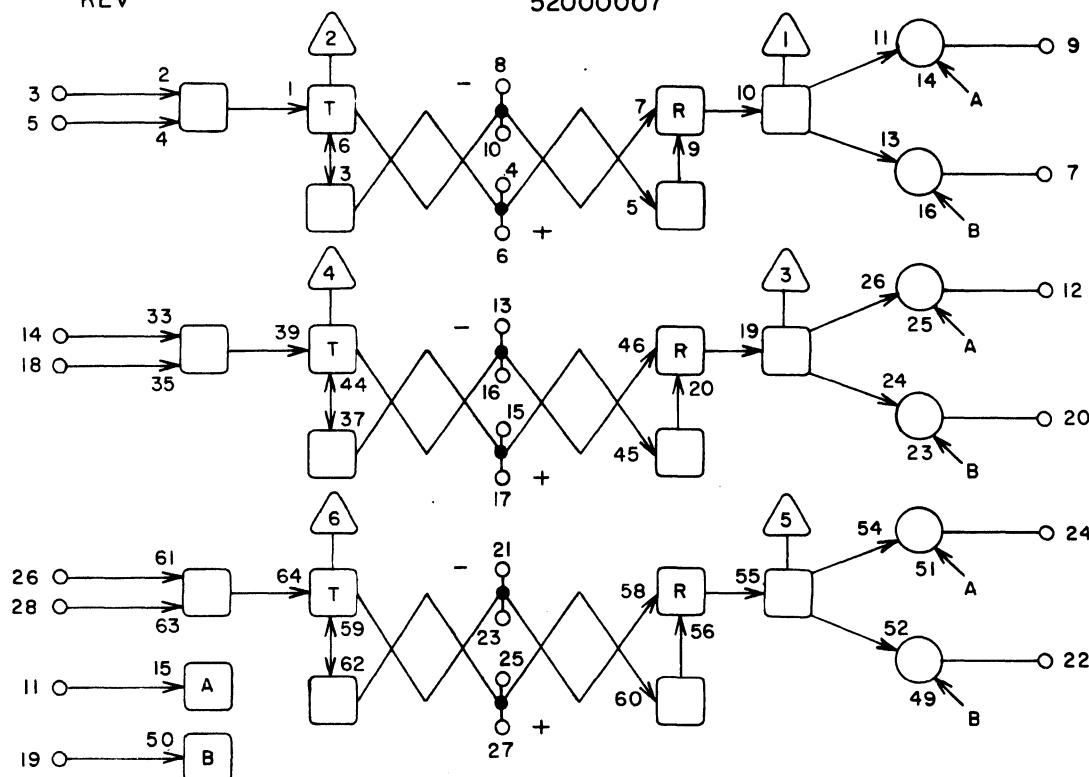
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60042700 Rev. K

LS 17776700

C
REV

CIRCUIT SPECIFICATION

11827600
52000005
52000007JACK
J48

PIN JACK PIN LG

1	-6V	
2	GRD	
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60042700 Rev. P

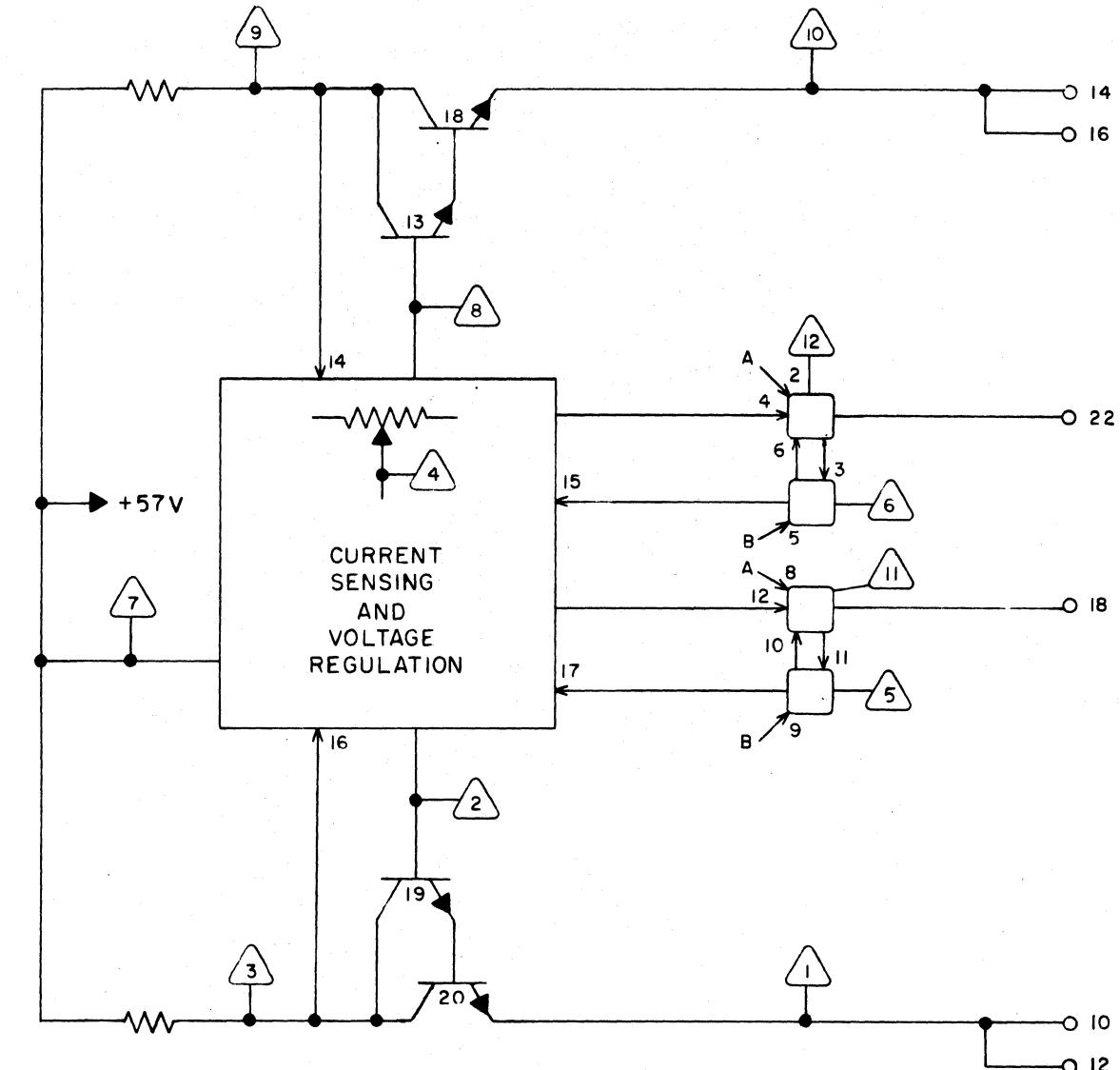
LS 17776800

A
REV

JACK

J51

CIRCUIT SPECIFICATION 520000II



20 O → A

FOR SCHEMATIC SEE DRAWING 17800100
60042700 Rev AB

PIN	JACK	PIN	LG
2	GRD		
4	GRD		
6	+57V		

8	+57V	
10		
12		
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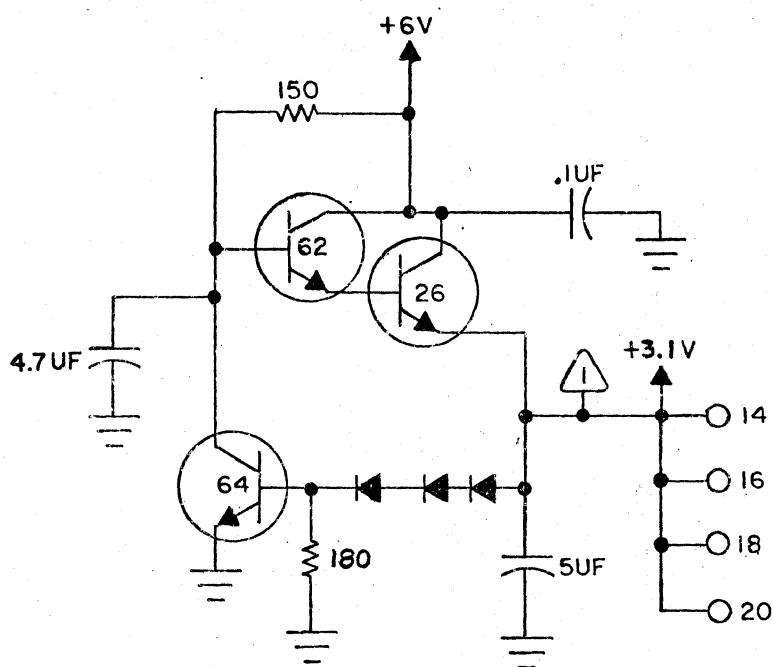


LS17776900

G
REV

JACK J53

CIRCUIT SPECIFICATION 52000004



60042700 Rev. T

PIN	JACK	PIN	LG
1			
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3			
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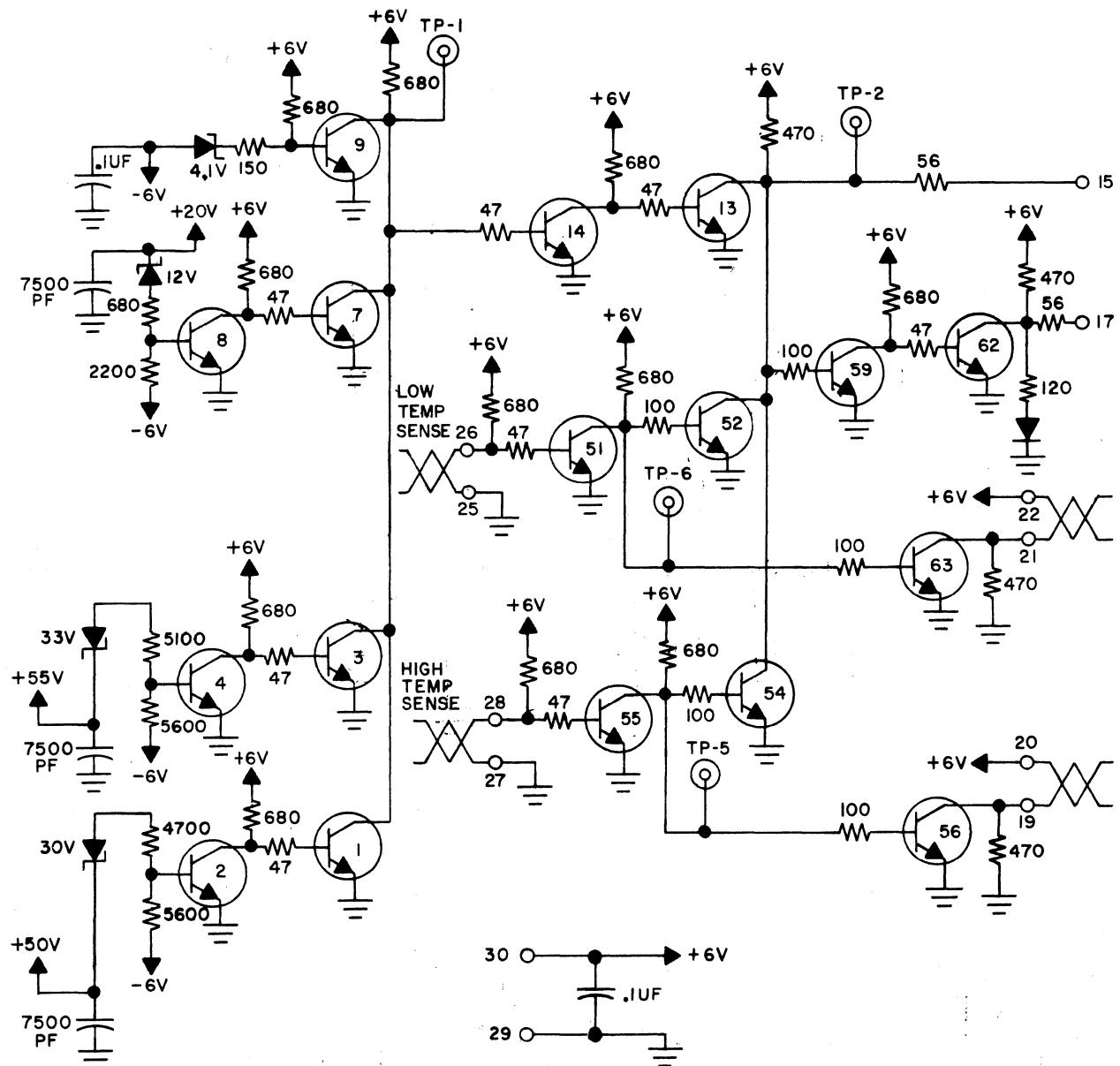
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LS 17883500 B
REV

JACK J54

CIRCUIT SPECIFICATION 520000010



PIN JACK PIN LG

1	-6V		
2			
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4			
5			
6	+50V		
7			

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9			
10	+55V		
11			
12	+20V		
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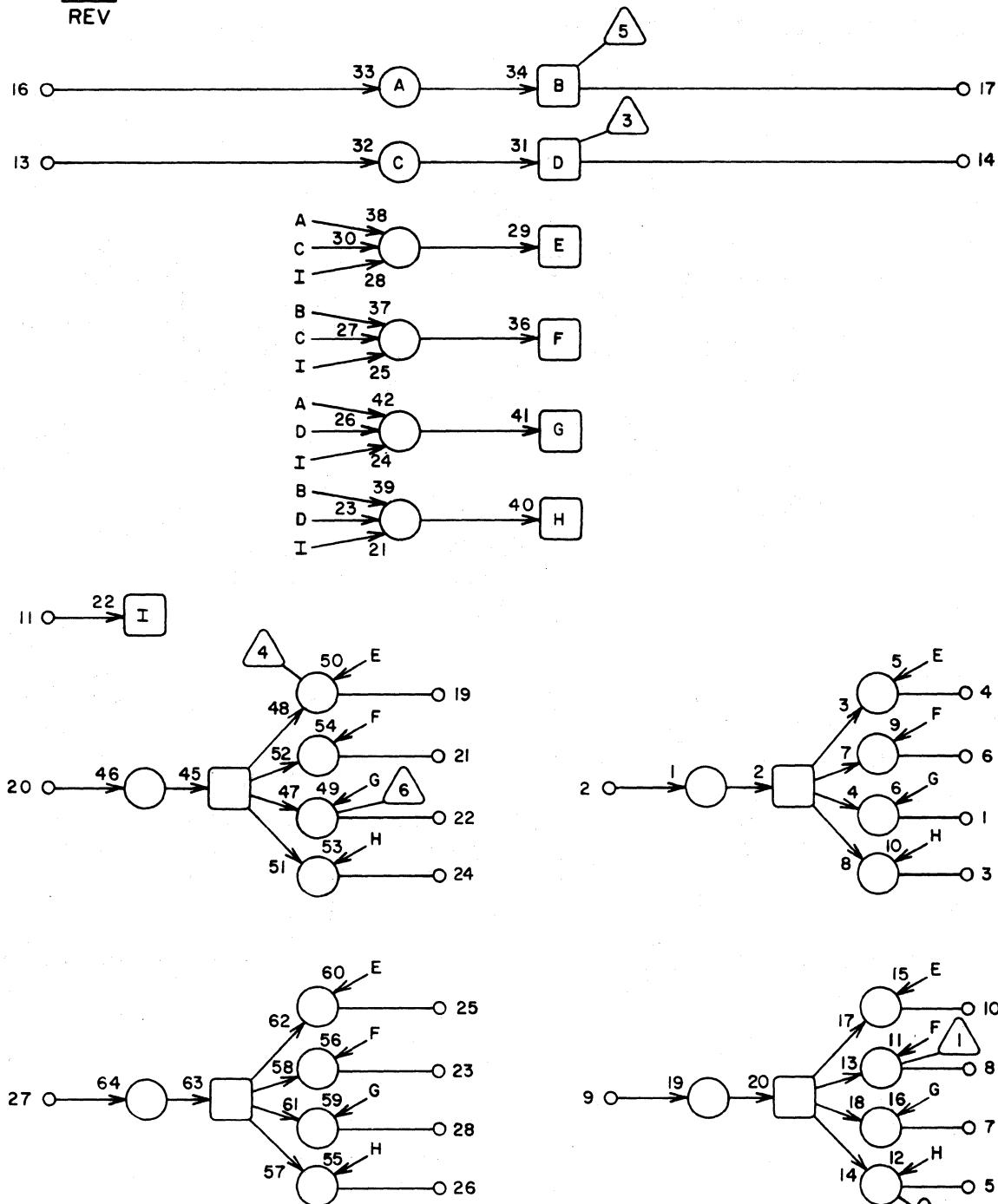
60042700 Rev. K

LS 17774800



CIRCUIT SPECIFICATION 11827600

REV

JACK
J55

PIN	JACK	PIN	LG
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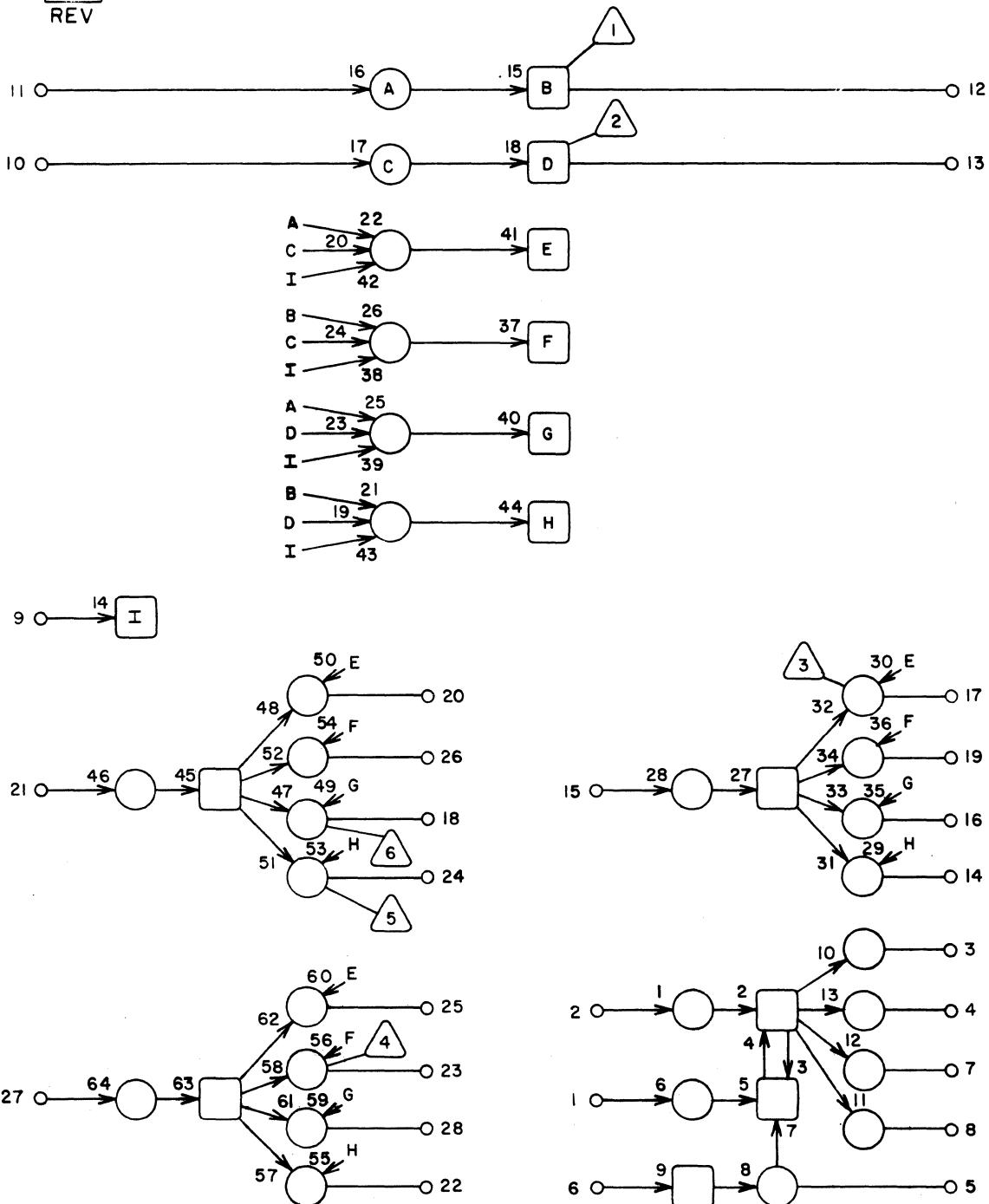
60042700 Rev. K

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LS 17775100

B
REV

CIRCUIT SPECIFICATION 11827600

JACK
J56

PIN JACK PIN LG

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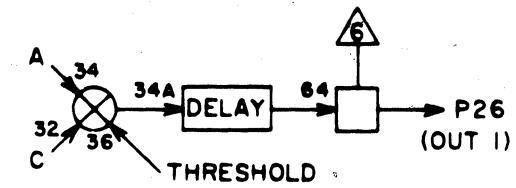
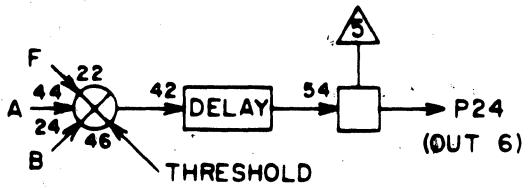
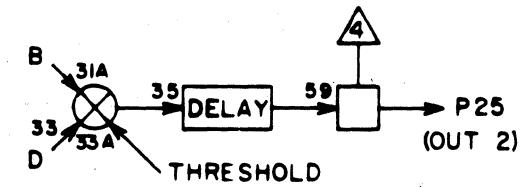
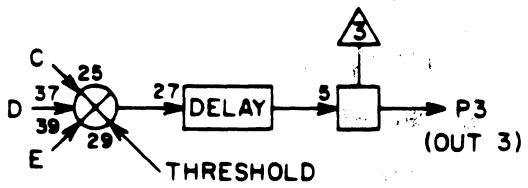
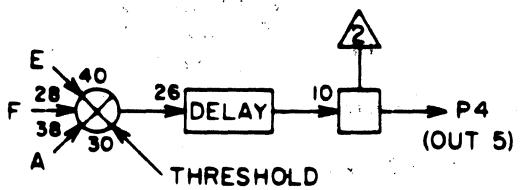
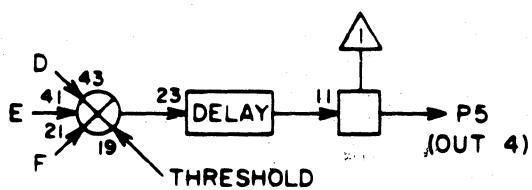
60042700 Rev. K

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LS 18323500
ASSY

3
REV

J57



P22 O → A
(IN 1)

P23 O → D
(IN 4)

P7 O → B
(IN 2)

P20 O → E
(IN 5)

P8 O → C
(IN 3)

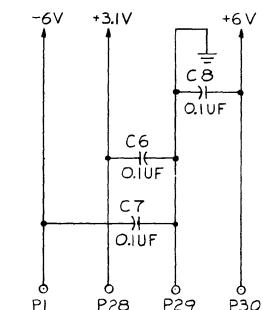
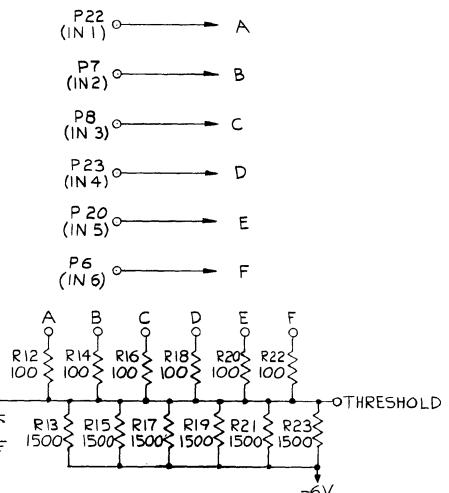
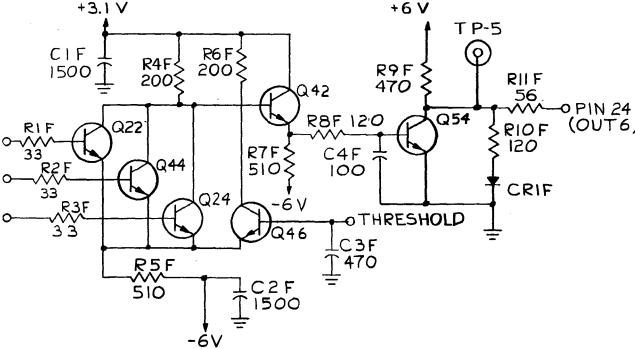
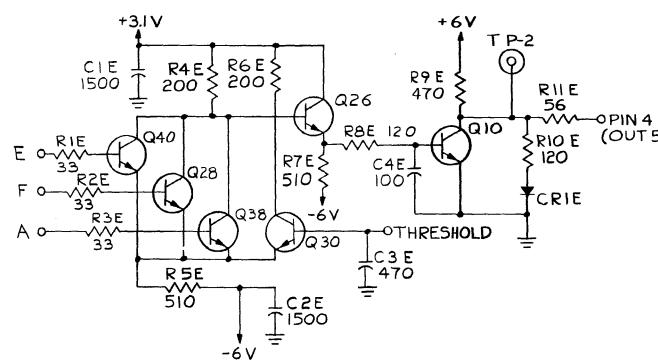
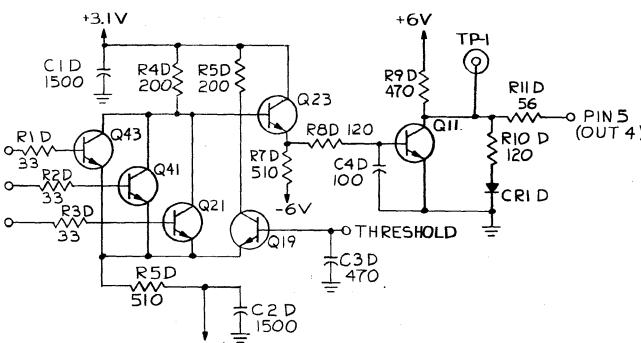
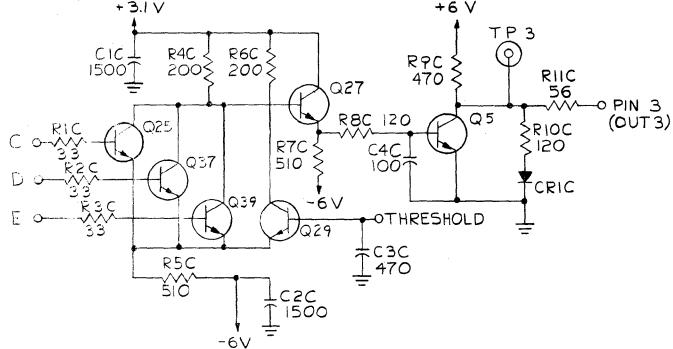
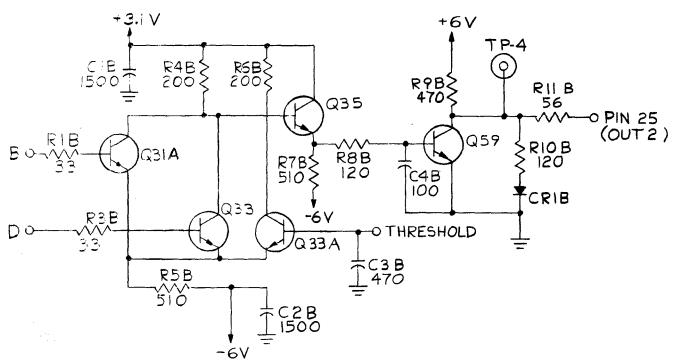
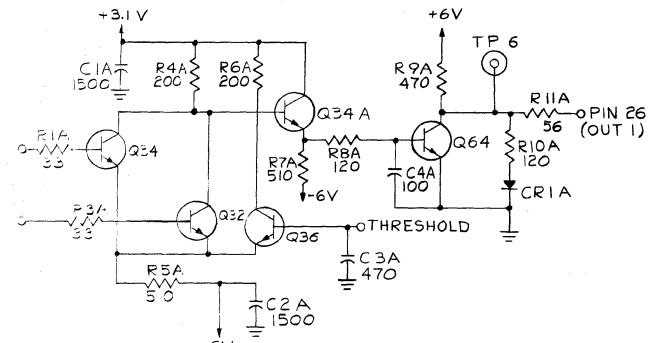
P6 O → F
(IN 6)

FOR SCHEMATIC SEE DRAWING
18323700

1	- 6V		
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28	+ 3.1V		

JACK PIN LG
SEE CIRCUIT SPECIFICATION
52000032

60042700 Rev. P



NOTES:

- I. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCES ARE IN OHMS.
ALL CAPACITANCES ARE IN PF.
ALL RESISTORS ARE 1/8 W ± 5%.
ALL CAPACITORS ARE ± 25%
ALL TRANSISTORS ARE 24561900

2. REFERENCE DRAWINGS:
ASSEMBLY 18323500
BOARD 18323600

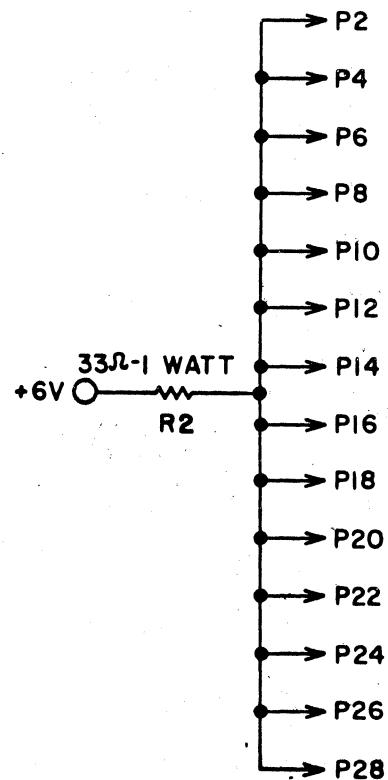
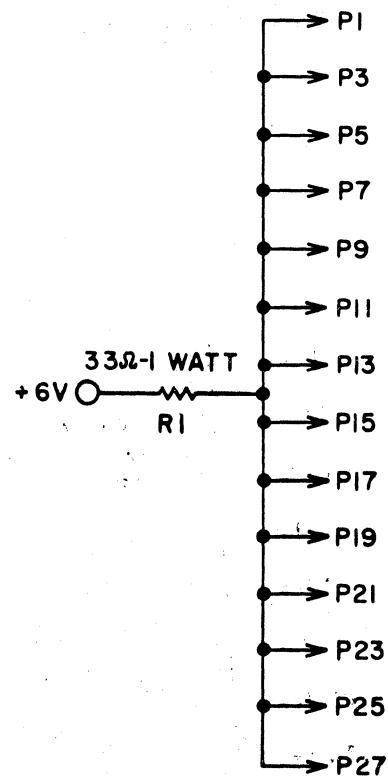
3. UNLESS OTHERWISE SPECIFIED ALL
DIODES ARE CONTROL DATA DRAWING
NUMBER 17814100 POLARIZED.



LS 18378200
ASSY

B
REV

J58



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JACK PIN LG

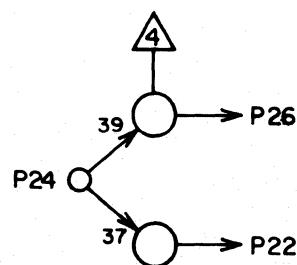
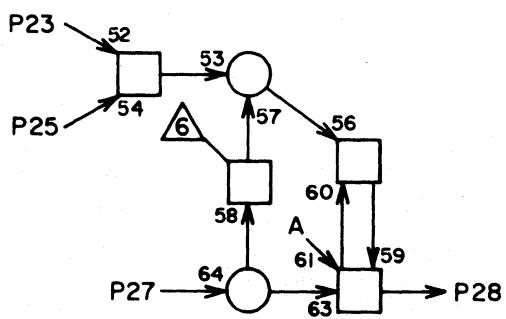
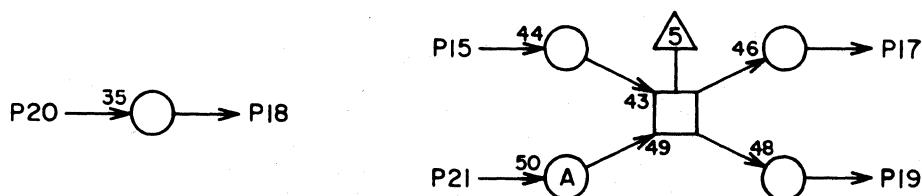
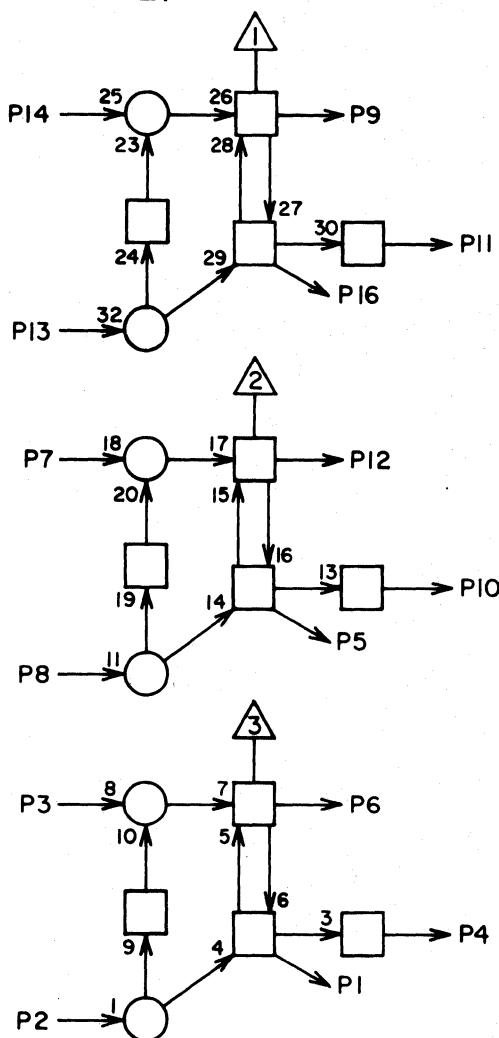
60042700 Rev. P



LS 18294700
ASSY

B
REV

J59



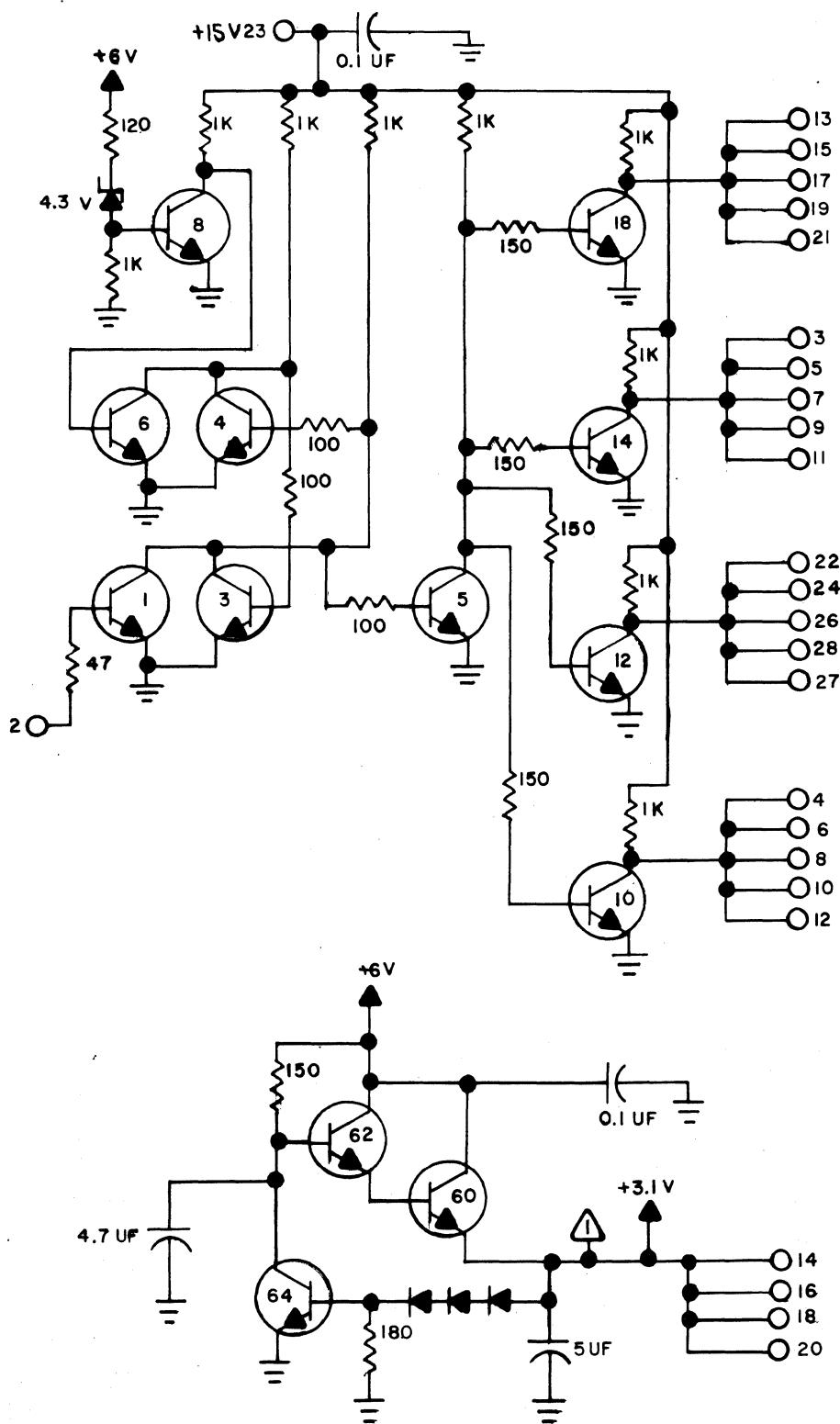
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JACK PIN LG
SEE CIRCUIT SPECIFICATION
M207600

60042700 Rev AB

LS 20264000 B
ASSY REV

J60



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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

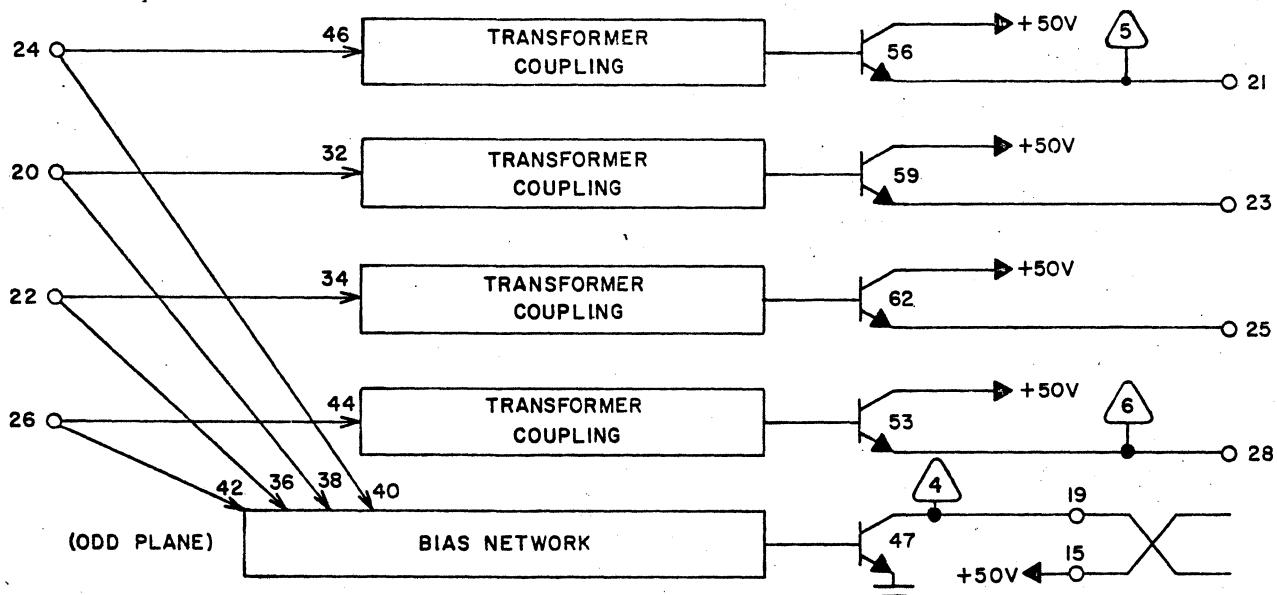
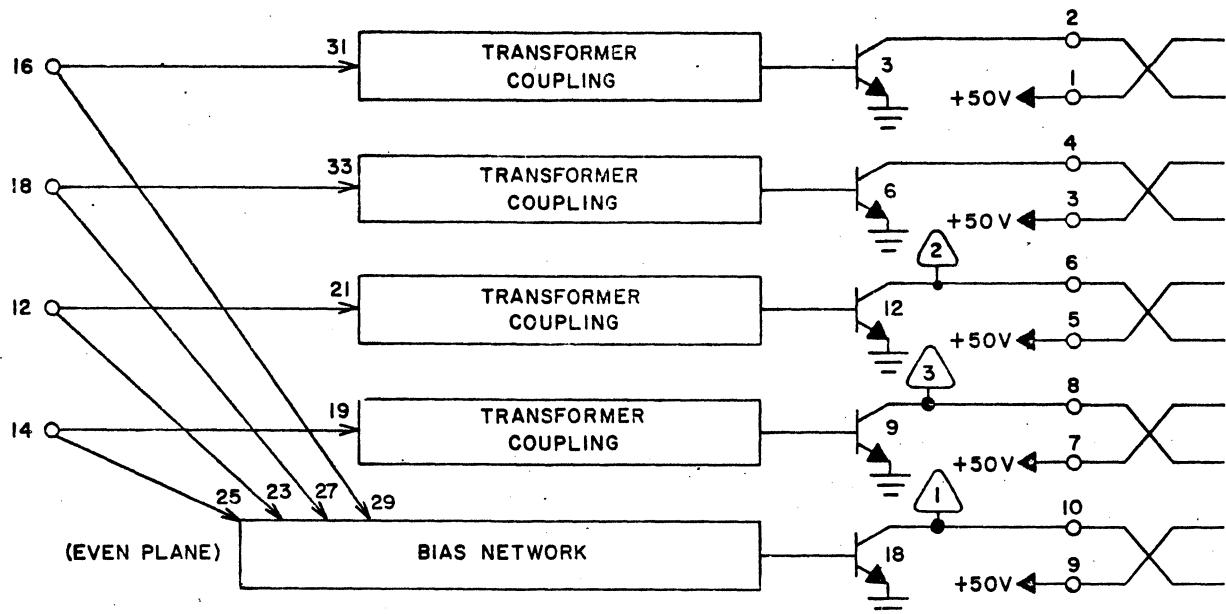
60042700 Rev. BA



LS 17776600
ASSY

B
REV

CIRCUIT SPECIFICATION 11832500

JACK
J80

FOR SCHEMATIC SEE DRAWING 17785800

PIN JACK PIN LG

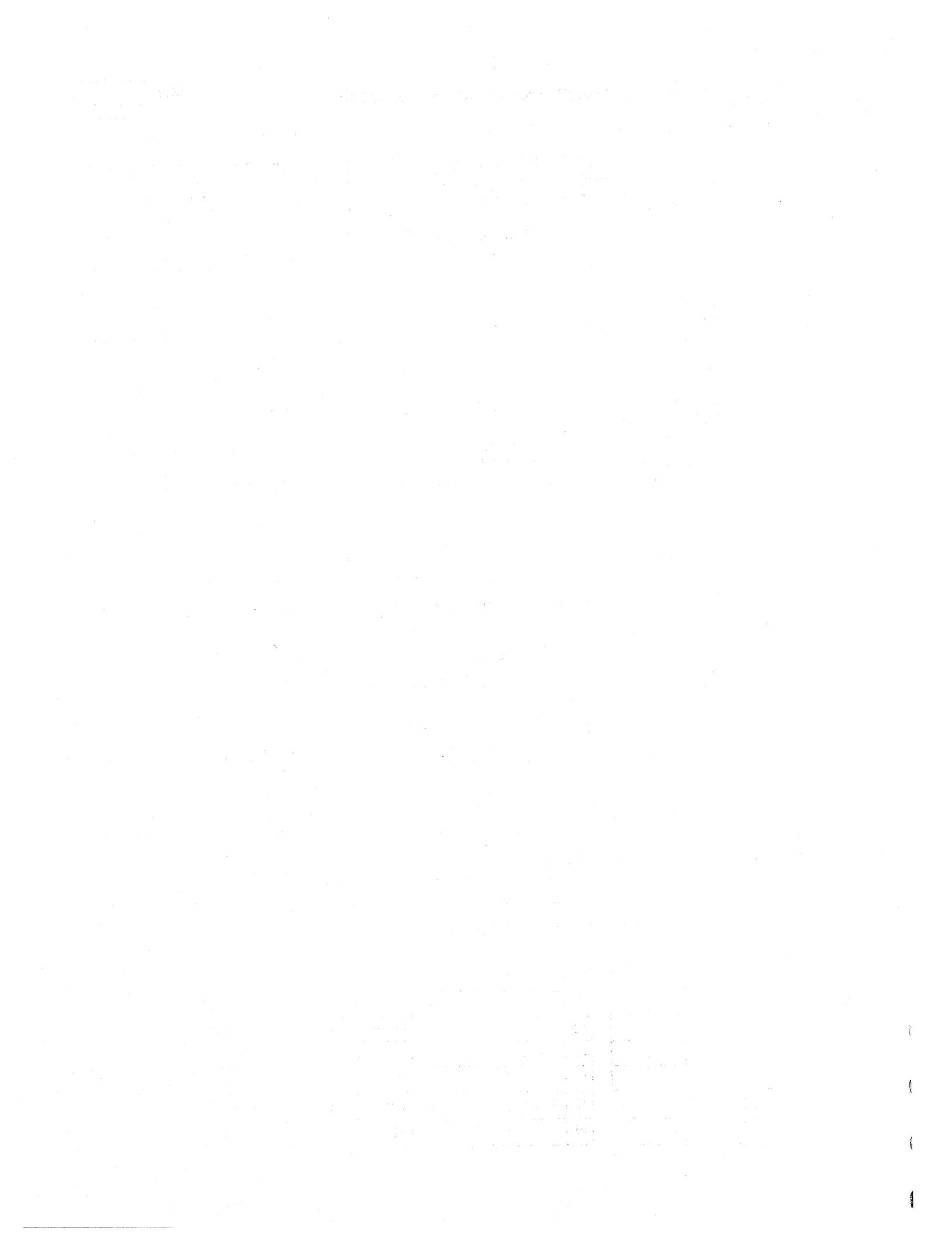
60042700 Rev. Y

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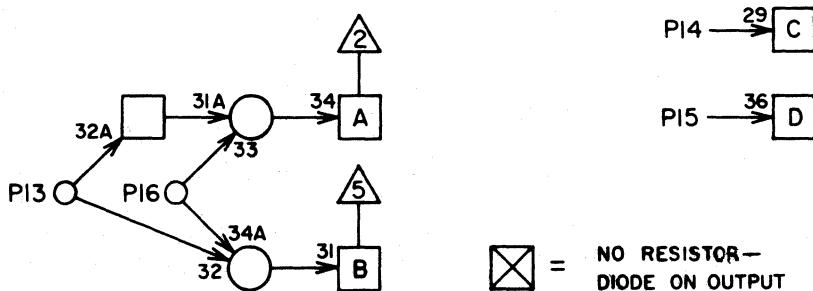
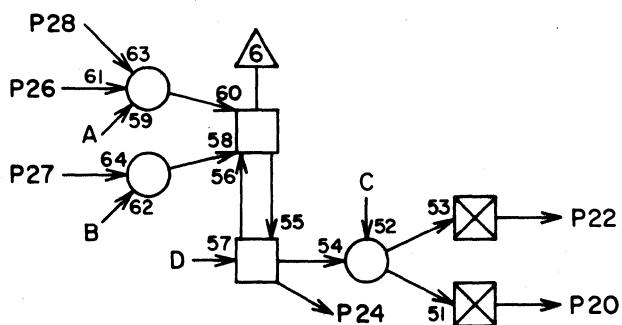
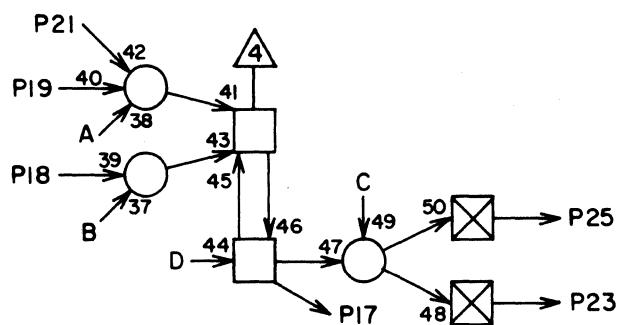
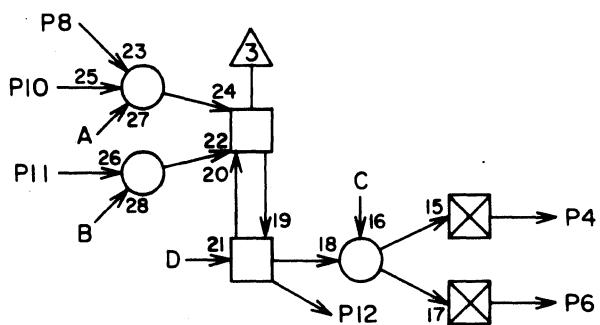
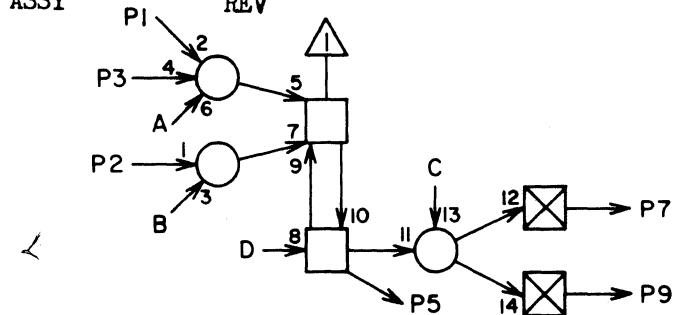
LS 18285900

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ASSY

REV

J82



= NO RESISTOR—
DIODE ON OUTPUT

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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
60042700 Rev AB

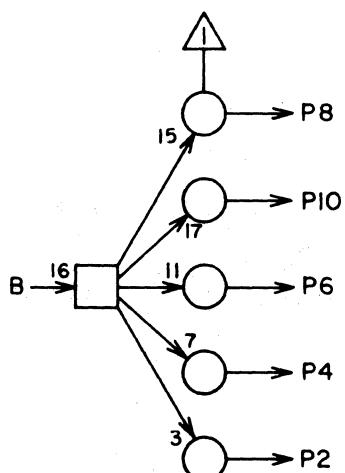
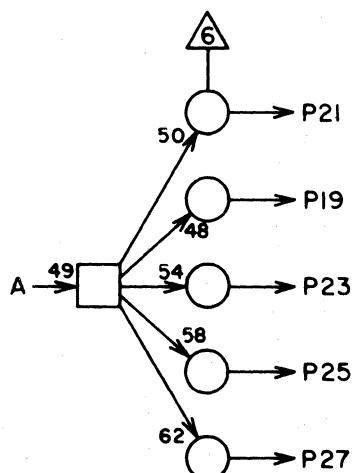
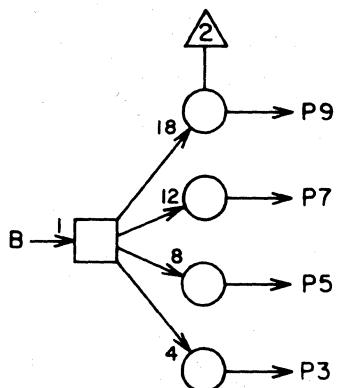
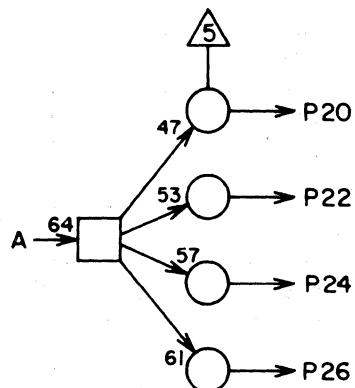
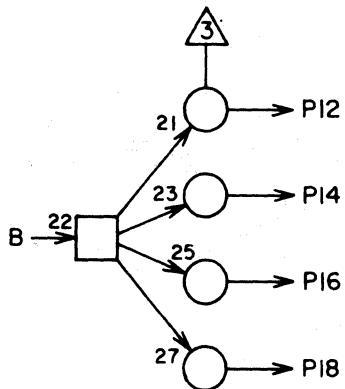
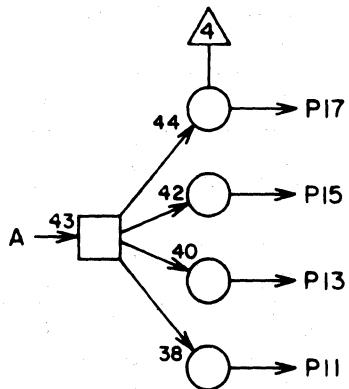
LS 18286200

ASSY

[B]
REV

J83

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P28 → 63 (A)

PI → 2 (B)

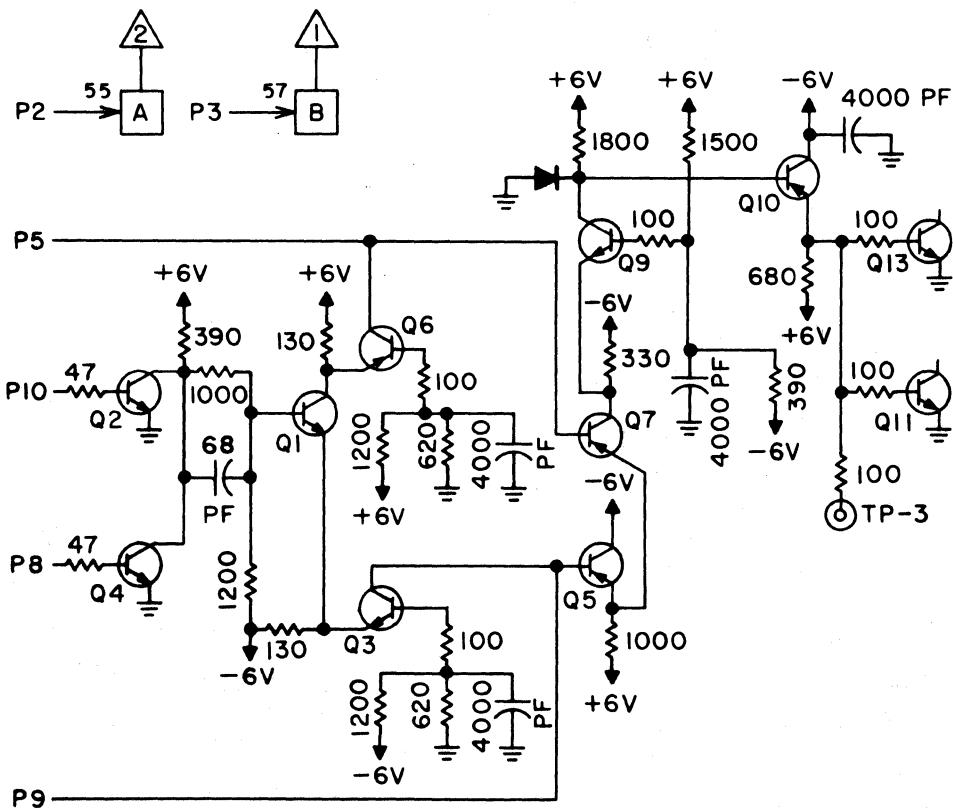
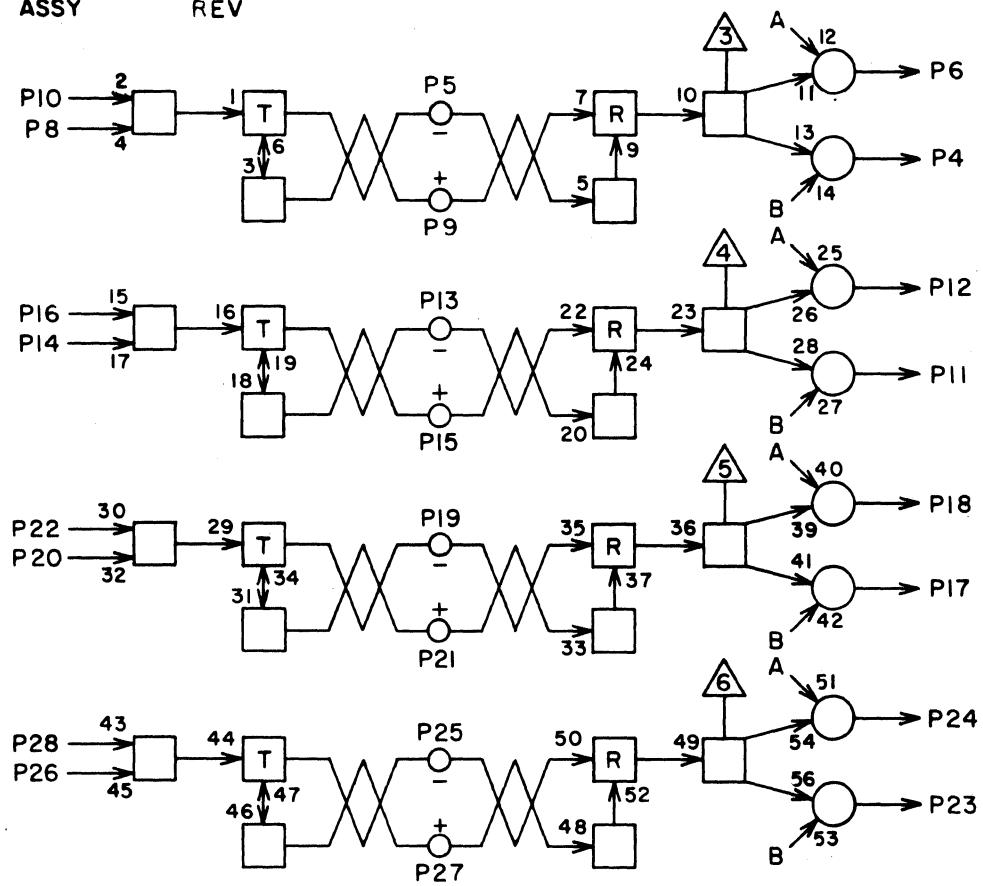
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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev AB

LS18286400 E
ASSY REV

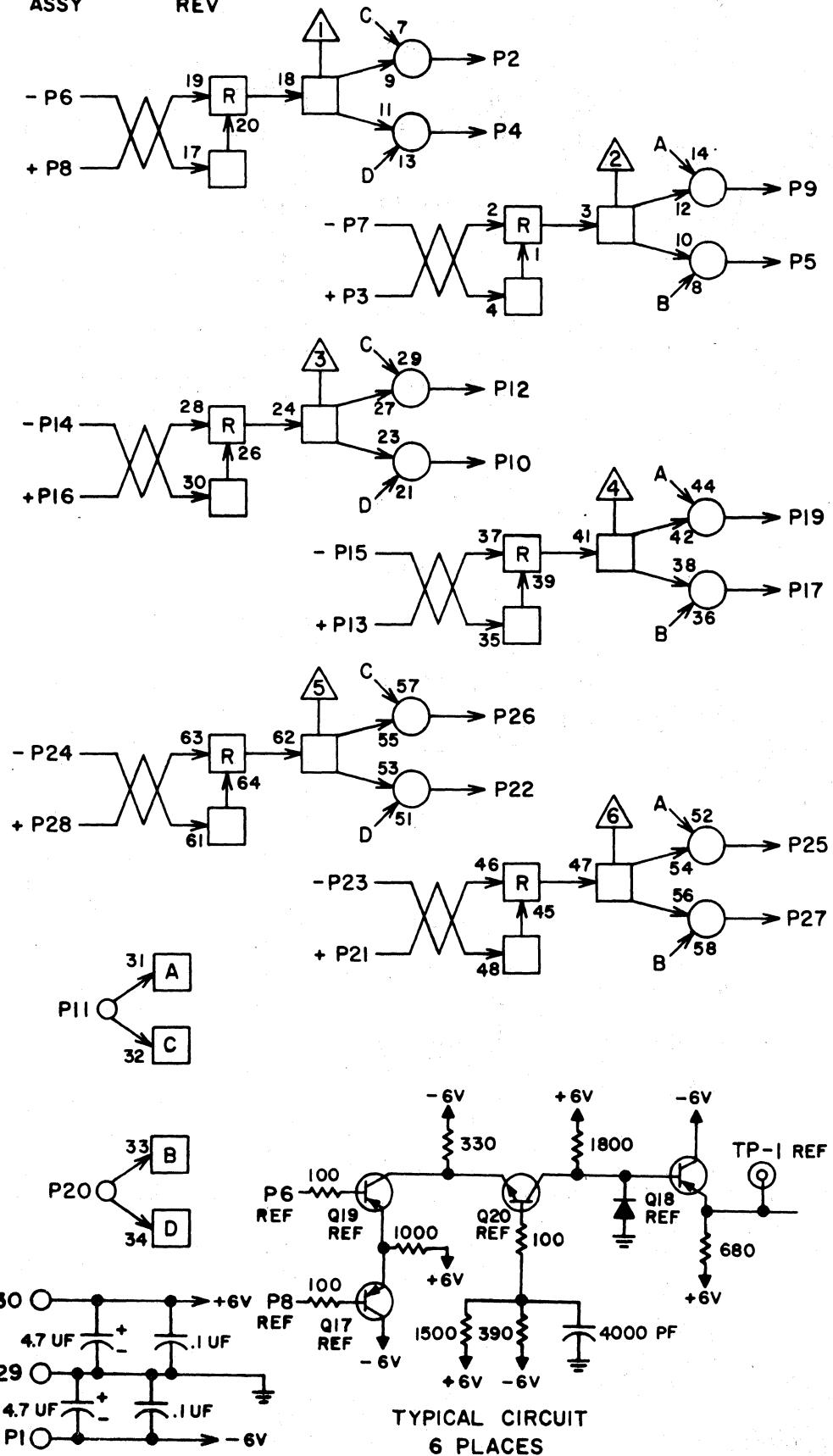
J84



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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev AB



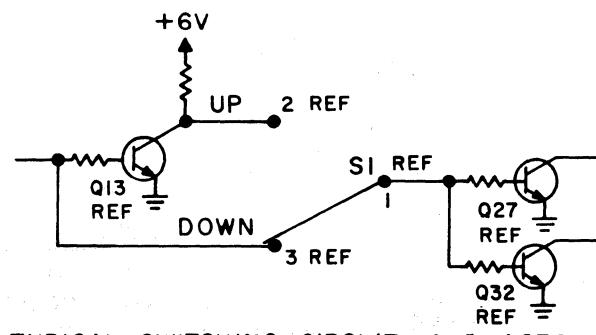
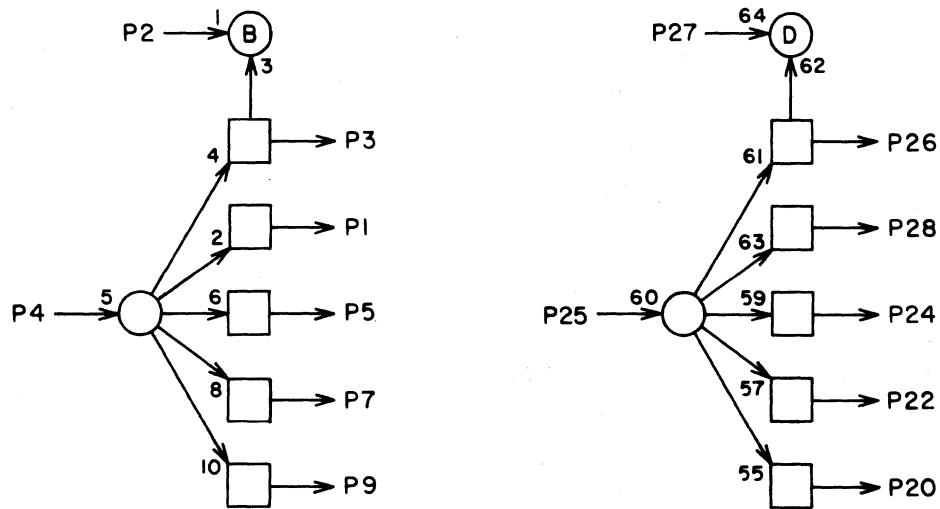
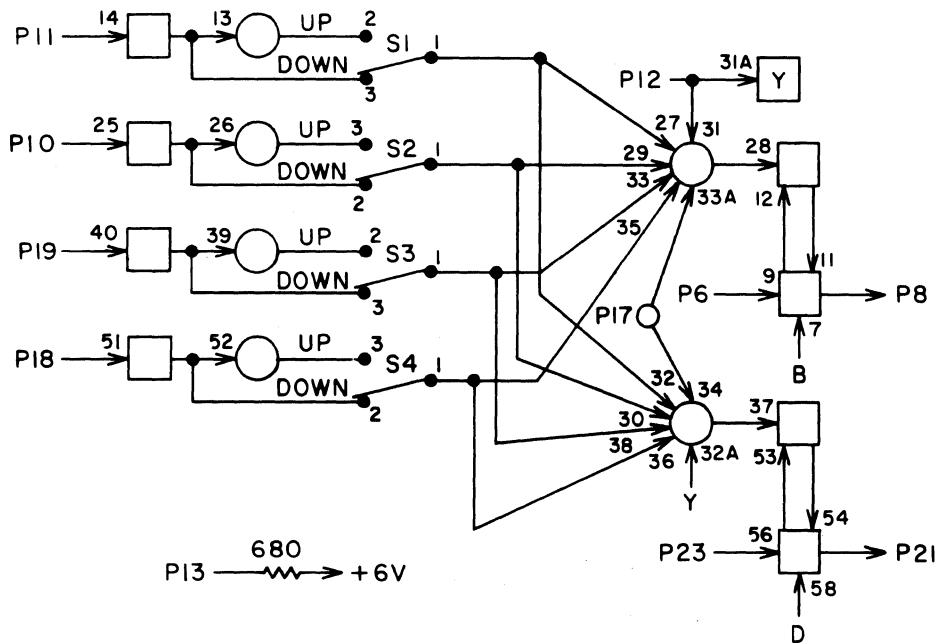
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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600
52000005

TYPICAL CIRCUIT
6 PLACES

LSI18290900 D
ASSY REV

J86



TYPICAL SWITCHING CIRCUIT 4 PLACES

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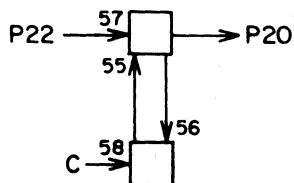
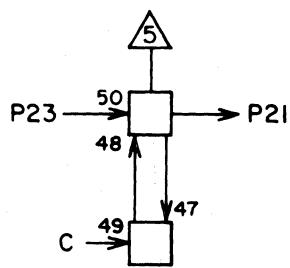
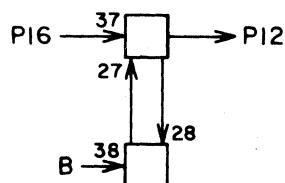
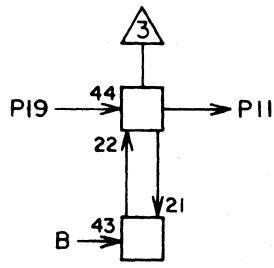
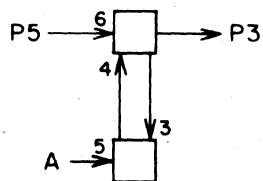
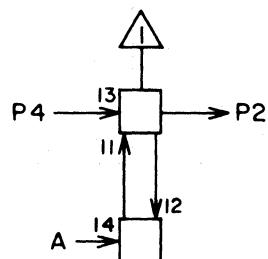
JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev AB

LS 18291000

B
REV

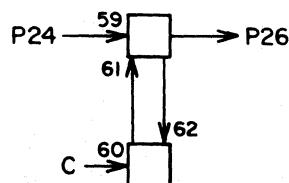
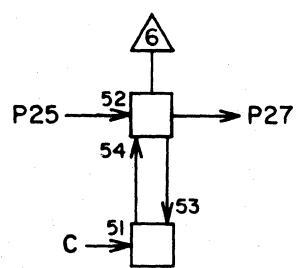
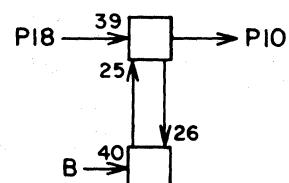
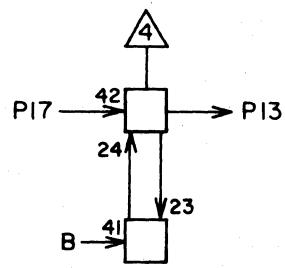
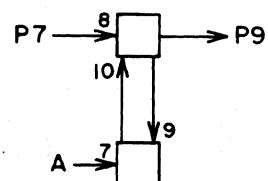
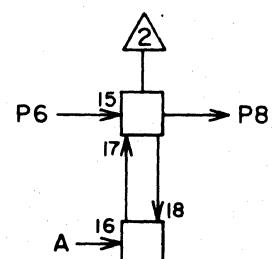
J 87



PI → 2 A

PI4 → 35 B

P28 → 63 C

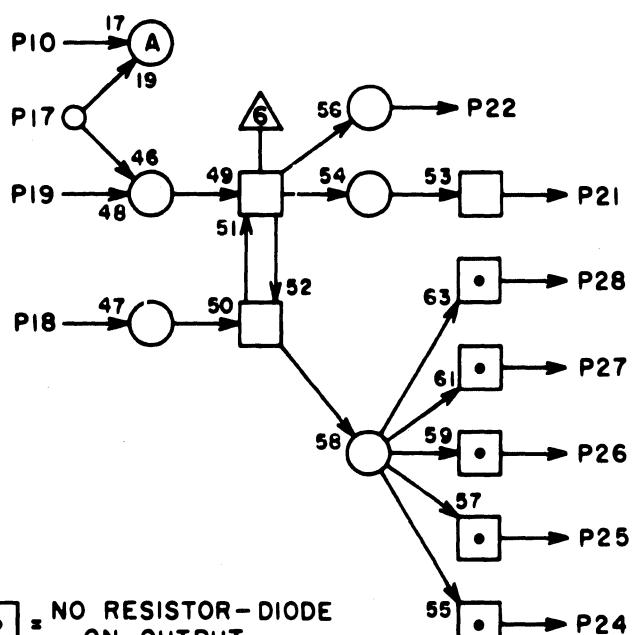
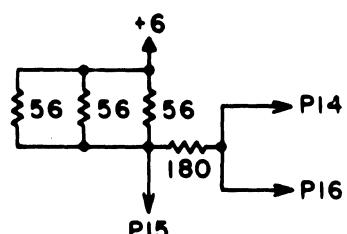
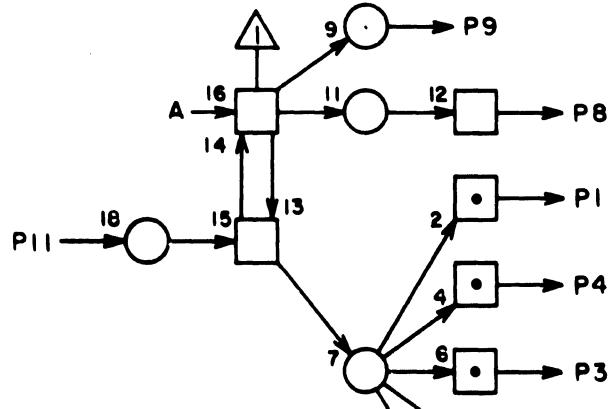


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SEE CIRCUIT SPECIFICATION
60042700 Rev AB 11827600

LS18294000 
ASSY REV

J88



 = NO RESISTOR-DIODE
ON OUTPUT

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JACK PIN LG
SEE CIRCUIT SPECIFICATION
11827600

60042700 Rev. P

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Printed Circuit Manual

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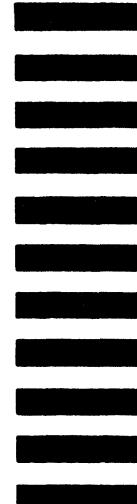
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