Century Data Systems
A Xerox Company

Marksman

Performance Specification

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Revision C

PREFACE

This document describes the MARKSMAN Disk Drives. The information contained in this document is intended as a reference for controller designers. Changes and updates to this manual will be contained in ERRATA Sheets.

RECORD OF REVISIONS	
REVISION	**NOTES**
0	ORIGINAL ISSUE
1	Revised – December 1978
2	Major changes incorporated in the revision are:
	• Modification of start time
	• Addition of expanded status
	• Updating of command flow charts
	• Expanded on the HEAD ADVANCE command
	• Updating of timing charts
	• Addition of spec for interfaces lines with PIA chip

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ILLUSTRATIONS

TABLES

SECTION 1
INTRODUCTION

1.1 PURPOSE

This manual contains information necessary to interface a MARKSMAN disk drive to a controller and ultimately to a computer system and provides the technical specifications for reference in OEM contracts.

1.2 RELATED DOCUMENTS

Companion documents on MARKSMAN that are available include:

MARKSMAN Technical Manual	P/N 76220-100
T-2004 Exerciser Technical Manual	P/N 76221-100

1.3 GENERAL DESCRIPTION

MARKSMAN represents a breakthrough in cost-performance ratio for rigid disk drives. With a marriage of fourth generation technology for high performance and floppy disk techniques for maximum economy, it offers the best of two worlds.

Data integrity comparable to that found in large disk systems is assured by the use of Winchester style heads and media. System reliability is maximized by the sealed contamination controlled disk compartment and the reduction in the parts count achieved by the use of a microprocessor.

The economy is achieved by the use of a band positioner driven by a stepper motor. The microprocessor controls this motor, allowing it to slew at high speeds, thus creating significant improvements in stepper motor performance.

MARKSMAN is designed to enable the OEM systems manufacturer to achieve a high degree of flexibility and the largest practical percentage of added value in the memory subsystem. The drive electronics include all of the analog functions, and those digital functions that are intimately related to the mechanics such as the stepper motor slew control and fault monitoring. The interface to the drive is by direct connection to the microprocessor Parallel Interface Adaptor (PIA).

- 10MB or 20MB of low cost, high performance storage.
- Winchester Technology Heads and Media provide state-of-the-art performance.
- High speed Start/Stop and landing zones maximize head/media life.
- Single/Board Microprocessor Based Electronics provide flexibility and simplify maintenance.
- MicroInterface optimizes the microprocessor based controller interface.
- Compatible with Floppy Disk power supplies.
- Data Transfer Rate Improvement of 15:1 over double density floppy disks.
- Access Time Improved Over 100%, to 12 times the data as compared to floppy disks.
- VFO Data Separator standard.
- No Preventive Maintenance required.
- Provision for Mounting embedded customer designed formatters and controllers.

SECTION 2
SPECIFICATIONS

2.1 OPERATIONAL SPECIFICATIONS

2.1.1

Operational specifications for MARKSMAN 10m and 20m Disk Drives are listed in Table 2-1 below.

Table 2-1. Disk Drive Specifications

MODEL	M-10	M-20
Bytes per track	24000	24000
Tracks per cylinder	2	4
Bytes per cylinder	48000	96000
Number of cylinders	210	210
Bytes per drive	10.08M	20.16M
Single track positioning time	3 milliseconds	
Average positioning time	43 milliseconds	
Maximum positioning time	113 milliseconds	
Head Settling time[1]	17 milliseconds	
Rotational speed (nominal)	2400 RPM	
Average latency time	12.5 milliseconds	
Recording density	7545 BPI	
Track density	182 TPI	
I/O Transfer rate	960 Kilobytes/second (7.68 Megahertz)	
Bit Cell time	130 nanoseconds	
Recording code	MFM	
Interface code (data)	NRZ Serial	
Positioning method	Stepper motor-driven band positioner	
Start time (nominal)	3 minutes	
Write-To-Read Delay	16 μsec	
Read-To-Write Delay	100nsec	

[1]Add settling time to positioning time to obtain data access time.

2.2 RELIABILITY

2.2.1 Mean Time Between Failures

MTBF is defined by the expression:

$$\text{MTBF} = \frac{\text{Operating Hrs.}}{\text{No. of Equipment Failures}}$$

Operating hours relate to the total "AC Power On" hours less any maintenance time. Equipment failures are defined as those failures requiring repairs, adjustments or replacements on an unscheduled basis, i.e., emergency maintenance required because of hardware failure or substandard performance due to operator error, adverse environment, power failure, controller failure, cable failure or other failures not caused by the drive.

The basic MARKSMAN has a designed MTBF of 8000 hours. The sealed mechanism alone has a designed MTBF of 25,000 hours.

To establish a meaningful MTBF, operating hours must be greater than 20,000 hours and include all sites where the drives are used.

2.2.2 Mean Time To Repair

MTTR is defined as the time for an adequately trained and competent serviceman to diagnose and correct a malfunction at the subassembly level. MARKSMAN is designed so that the MTTR is expected to be less than 0.5 manhours. The sealed portion of the drive is not field repairable and must be returned to the factory for repair in a special clean room environment.

2.2.3 Preventive Maintenance Time

No preventive maintenance is required.

2.3 DATA INTEGRITY

2.3.1 Recoverable Errors

A recoverable error is one which may be corrected by no more than 5 attempts to read the record. Any combination of seek-write, seek-read, seek-rezero is allowed without limitation of combination or duty cycle. Data patterns and track position do not affect data error rate performance. The recoverable read error rate for MARKSMAN Is less than one error in 10^{10} bits read.

2.3.2 Non-Recoverable Errors

A non-recoverable error is one which remains after 5 attempts to read the record in which an error is located.

The non-recoverable error rate for MARKSMAN is less than one error in 10^{13} bits read.

2.3.3 Positioning Errors

The positioning error rate is less than one error in 10^{6} seek executions.

2.3.4 Media

CalComp guarantees 210 of 213 available cylinders, including cylinder zero (0), head zero (0) to be error free. This is based upon twelve data read passes over the entire surface. All media defects will be identified to the customer by a written notice attached to the disk drive.

SECTION 3
INTERFACE SIGNALS

3.1 DISK DRIVE INTERFACE SIGNALS

Signals appearing at the MARKSMAN Disk Drive interface and their use are shown in Tables 3-1 and 3-2.

Table 3-1. Control Signals

Signal Name	Mnemonic	I/O	Description
Control Bus	CBUSO-7	Both	A high active 8 bit wide bus used to transfer commands from the interface and status to the interface.
Control Request	CREQ	I	A high active line from the interface, used in conjunction with the CACK line to form a handshake between the Interface and the Drive, CREQ indicates to the Drive: 1. The interface has placed a byte of command or a byte of data on the Interface Data Bus. 2. The Interface has accepted the ending status from the Drive.
Control Acknowledge	CACK	O	A high active line from the drive to the Interface to: 1. Acknowledge receipt of a byte of command or data from the Interface. 2. Notify the Interface the drive has placed a byte of status information on the Data Bus.
Control Ready	CRDY	O	A high active line from the Drive to the Interface indicating the drive is in the input mode and is waiting for a command.
Control Status	CSTAT	O	A high active line from the Drive to the interface indicating that the drive has placed a byte of status information on the data bus.
Drive Ready	DRDY	O	A positive true line from the drive to the interface indicates that the drive is up to speed and DC power is safe.
Reset	RST/	I	A low active signal from the interface which provides the drive with an unconditional reset and causes the heads to be relocated to Track 229. The pulse width must be $\geqslant$10 microseconds.
Index	IDX	O	A high active line from the drive used to indicate the physical beginning of a track of data. The INDEX pulse width is nominally 100 microseconds. The leading edge of index is the beginning of the first sector.

Table 3-1. Control Signals (Continued)

Signal Name	Mnemonic	I/O	Description
Sector	SEC	O	A high active line from the drive used to indicate the physical beginning to the data record within a track. The SECTOR pulse width is nominaly 1.02 microseconds. Note that there is no sector pulse at the beginning of the first sector (See Index).
Write Unsafe	WRTUSF	O	A positive true line from the drive to the interface used to indicate an unsafe write process was attempted. (i.e., multi-head DC unsafe, write on protected head). Shall be cleared when status is requested.

Table 3-2. Read/Write Signals

Signal Name	Mnemonic	I/O	Description
Write Data	NRZIN	I	A positive true line from the interface to the drive used to transmit serial write data to the drive.
Write Clock	WRTCLK	O	A positive true line from the drive to the interface used to clock write data from the interface. This clock shall be phase locked to the spindle rotation at all times. The leading edge of the pulse signifies a bit, and the nominal pulse duration is 130 nanoseconds.
Write Gate	WRTGATE/	I	A negative true line from the interface to the drive used to write data on the selected head.
Read Data	NRZOUT	O	A positive true line from the drive to the interface used to transmit serial read data to the interface. This output shall be connected to the interface only, after RDGATE becomes true. All other conditions shall provide a clamped logic zero output state.
Read Clock	RDCLK	O	A positive true line from the drive to the interface used to clock read data from the drive. The leading edge of the pulse signifies the beginning of a bit cell, and the nominal pulse duration is 130 nanoseconds.
Read Gate	RDGATE	I	A positive true line from the interface to the drive shall start lock-up of the phase lock loop (PLL) in the Data Separator (which controls the RDCLK output). Read Gate true must not be raised over write splice (read gap) areas and must occur after seek complete. Read Gate false must occur prior to any write splice and must be maintained no less than 4 bytes before allowing Read Gate true.
MPU Clock	1MHZ	O	This one megahertz clock is provided for use by the controller in functions that do not require syncronization to the disk speed.

SECTION 4
INTERFACE DESCRIPTION

4.1 GENERAL

The controller interface functions may be divided into four areas:

- Single Byte Commands (SEQUENCE, REZERO, STATUS, REQUEST, HEAD ADVANCE)
- Two Byte Commands (SEEK, SET SECTOR, DIAGNOSE)
- Data Transfer (READ & WRITE operations)
- Drive Malfunctions and Controller Errors

4.2 ONE BYTE COMMANDS (Figure 4-1, 4-1A, 4-2 & 4-2A)

4.2.1 Sequence

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	X

Bit 0 = 0 Sequence Up

Bit 0 = 1 Sequence Down

The SEQUENCE command causes the disk drive motor to power up (Bit 0 = 0) or power down (Bit 0 = 1). During a power up, the speed of the disk is checked and when speed is within tolerance, the heads are positioned to cylinder zero, head zero. DRDY and CRDY are both held inactive for 3 minutes. During a power down, the heads are positioned to the landing zone before power is removed from the drive motor. A sequence UP command must be used to bring the drive up to speed and ready. If power fails, the heads land where they are.

4.2.2 Rezero

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0

The rezero command causes the heads to be repositioned to cylinder zero, head zero.

4.2.3 Status Request

7	6	5	4	3	2	1	0
0	0	0	0	0	X	X	X

XXX

000	Status
001	Expanded Status
010	Last Command (MSB – 1st or only byte)
011	Last Command (LSB – 2nd byte on 2 byte commands)
100	CAR (Current Cylinder)
101	Sector Per Track
110	Diagnostic Bits (TBD)
111	Diagnostic Bits (TBD)

Status Bit Significance

Bit 0	Track zero: heads are located over track zero.
1	Landing zone: heads are located over landing zone.
2	Illegal Command (Set if any of bits 2, 4, 5, 6, or 7 of expanded status set.)
3	Ready: the disk is up to rotational speed.
4	Spin acceleration/deceleration out of limit.
5	End of cylinder (Head 3 is selected)
6	Diagnostic error
7	Track zero error

Expanded Status Bit Significance

Bit 0	Sector Length
1	Switches
2	Illegal Set Sector
3	Sector Per Track set by 0 = Sector Length Switches 1 = Set Sector Command
4	Illegal Rezero or Illegal Seek (Drive not up to speed or Seek attempted from landing zone)
5	Illegal Cylinder
6	Illegal Command
7	Attempted Write on On a Write Protected Head

The Status Request command causes the current status of the drive to be returned to the interface. Status bits are cleared after being presented to user except for bits 0, 1, 3 and 5. Expanded status bits are cleared after a specific request for expanded status except bits 0, 1, 3 and 5.

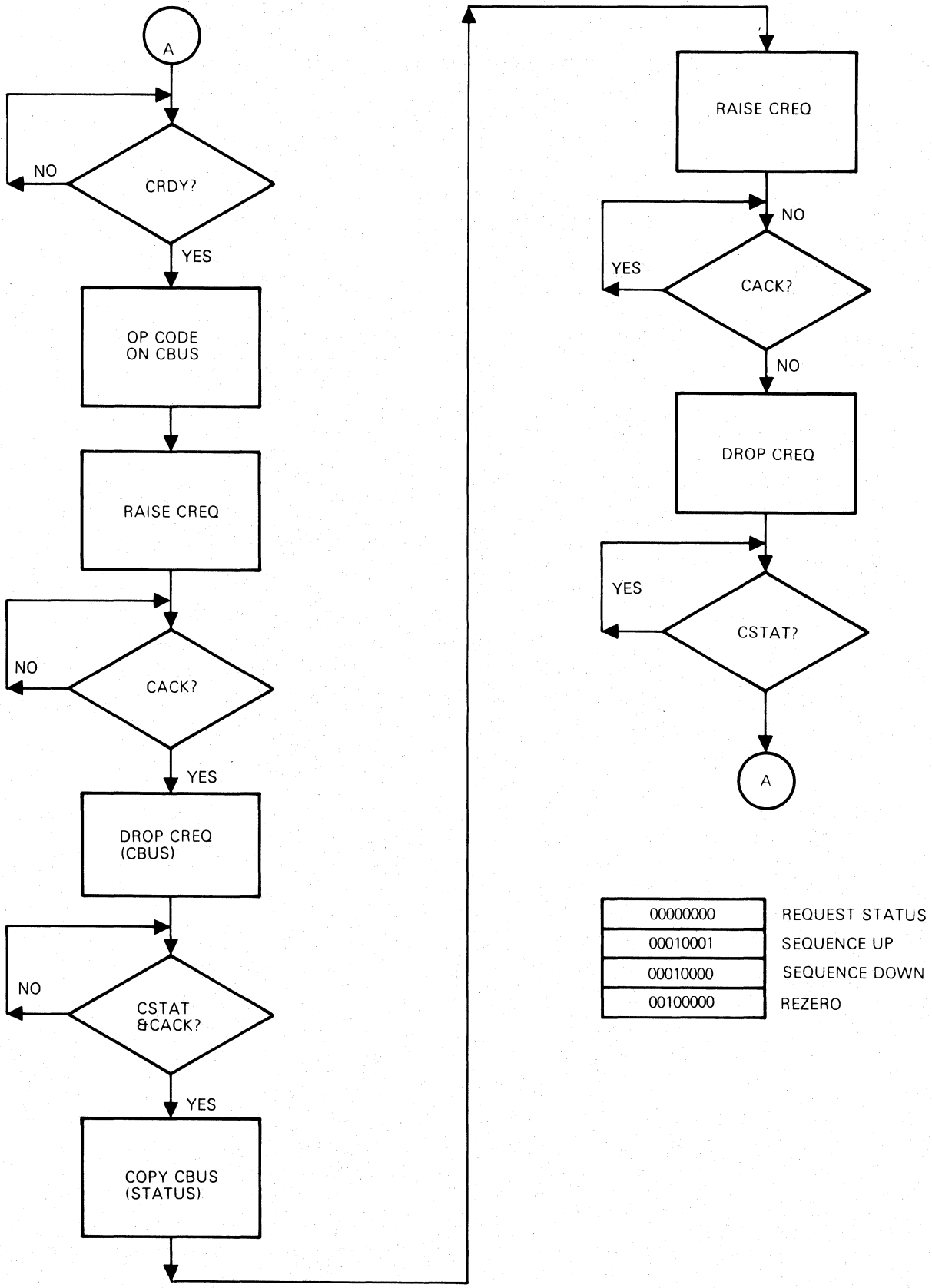


Figure 4-1. One Byte Commands (Except Head Advance) Flow Chart (Suggested Procedure for User)

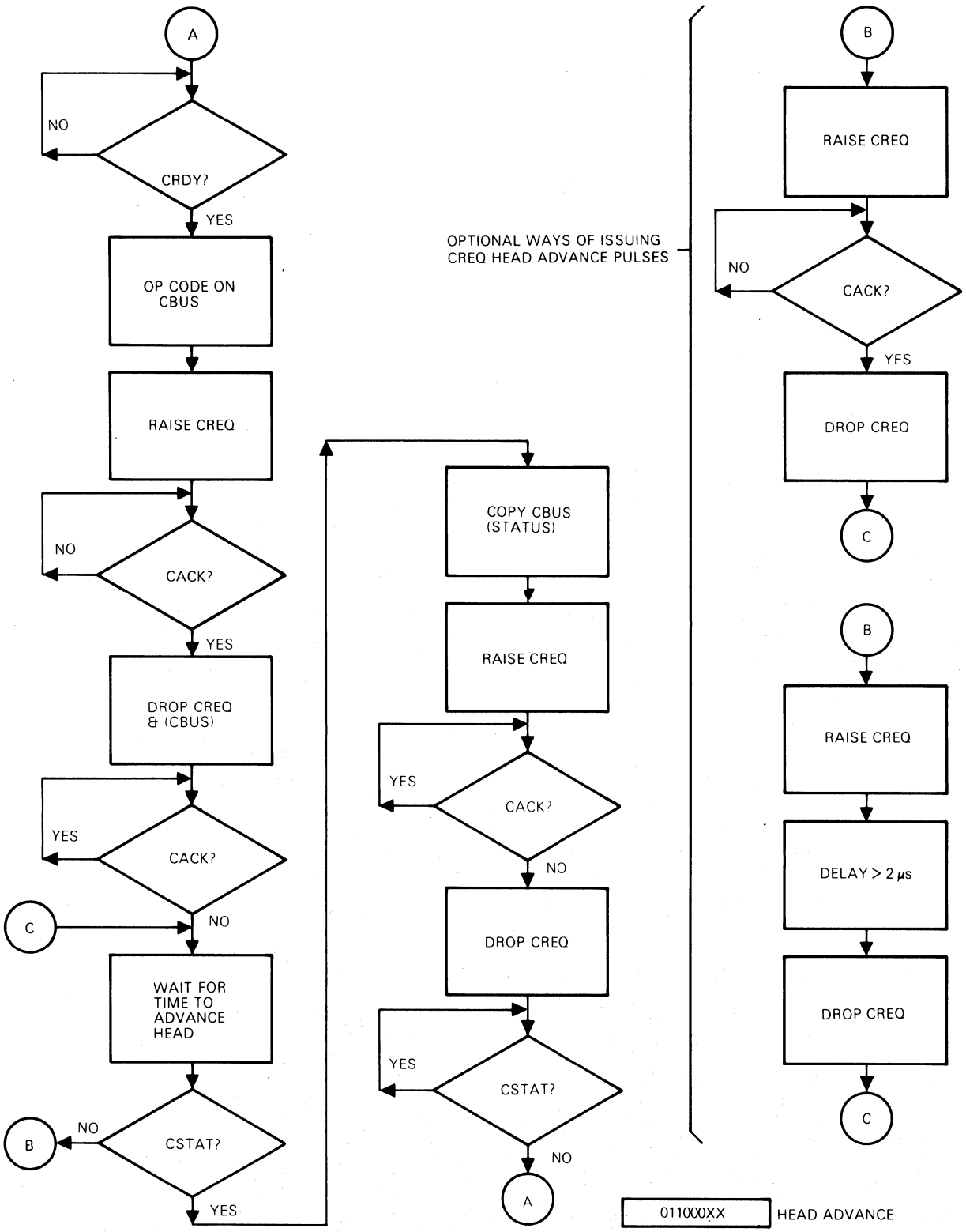


Figure 4-1A. One Byte Command Head Advance Command Flow Chart (Suggested Procedure for User)

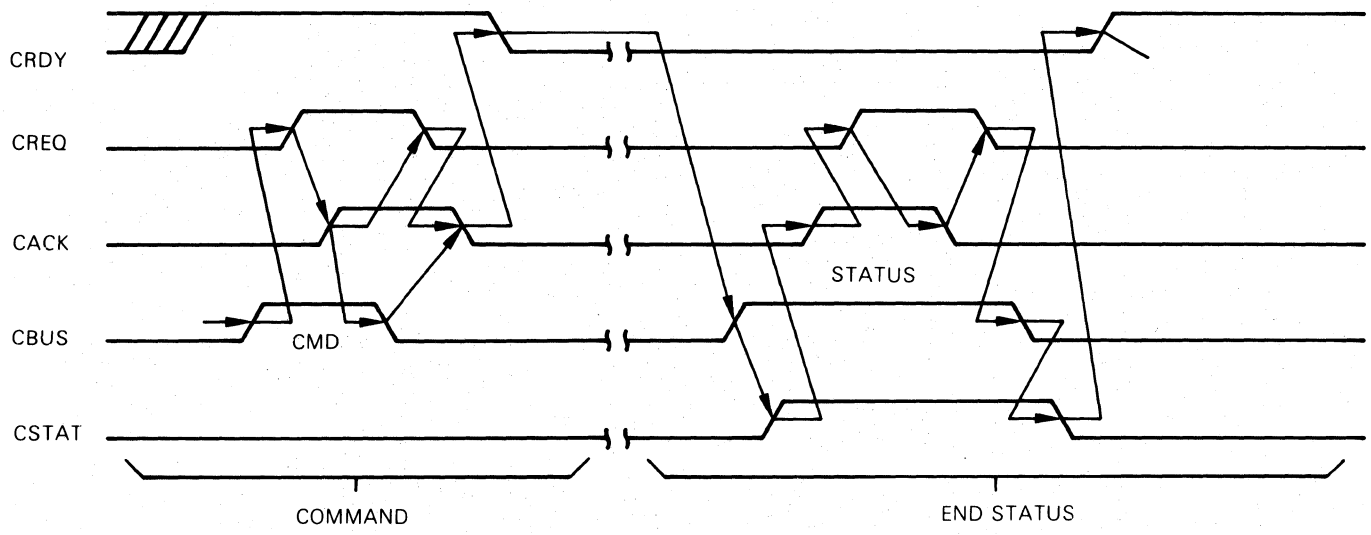
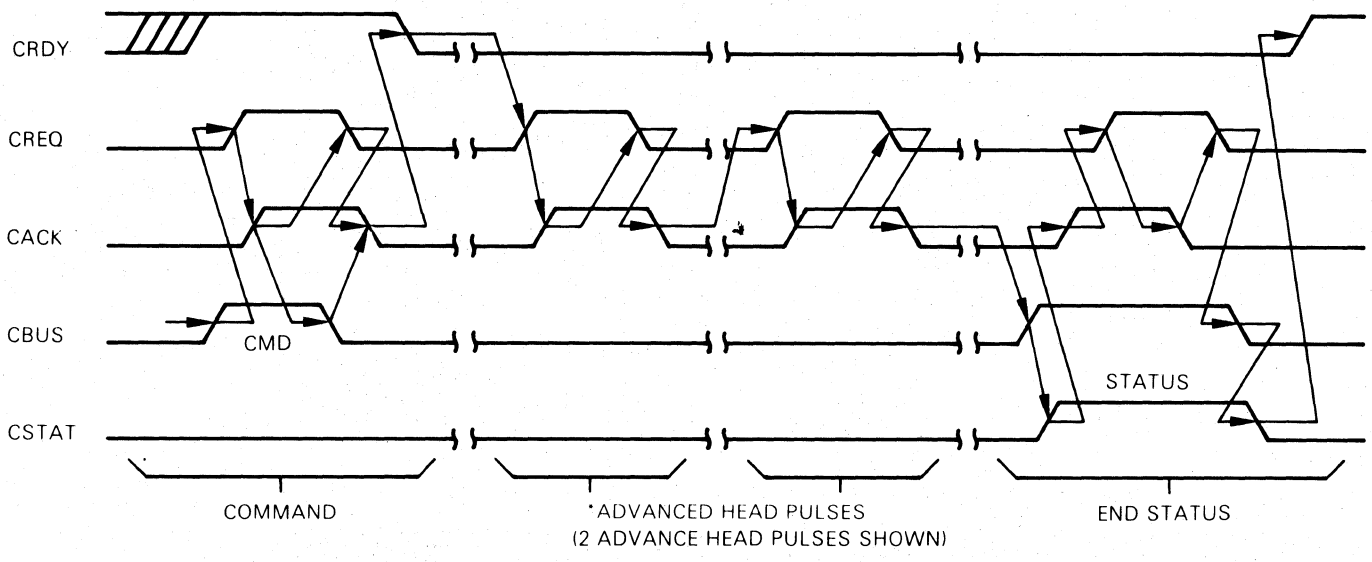


Figure 4-2. One Byte, Commands (Except Head Advance) — Timing Diagram



*NOTE: CACK will echo the CREQ head advance pulses but can rise after CREQ has dropped if CREQ IS very narrow. (The head advance operation is still performed prior to the rise of CACK). CREQ for head advance, should be at least 2 μs wide.

Figure 4-2A. One Byte Command Head Advance Command — Timing Diagram

4.2.4 Head Advance

7	6	5	4	3	2	1	0
0	1	1	0	0	0	X	X

XX

00	NO OP
01	Advance Head One Time
10	Advance Head Two Times
11	Advance Head Three Times

This command provides a means of advancing the head address more rapidly than can be done using the SEEK COMMAND thereby allowing sequential sector accesses across head boundaries.

The HEAD ADVANCE COMMAND places the drive in a state where it waits for the rise of CREQ. The drive advance the head address in about 11 μs to 25 μs after CREQ goes active. During the CREQ-CACK handshake, the drive does not copy the CBUS. STATUS is presented when either the commanded head advance count is depleted or the head address is advances to the last head. CRDY will remain inactive (and the drive incapable of accepting another command) until the STATUS is delivered. The last-head bit (bit 5) in the STATUS word will be active whenever the last head is selected.

4.3 TWO BYTE COMMANDS (Figure 4-3 & 4-4)

4.3.1 Seek

7	6	5	4	3	2	1	0
0	1	0	0	0	0	H	H
Cylinder Address							

The SEEK command is used to position the heads over the specified cylinder and select the head addressed by the low order bits of the command byte. The SEEK command requires one Byte transferred with the command to specify the cylinder.

4.3.2 Set Sector

7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0
Sector Count							

This command is used to override the switch setting of S1 and S2 and define the number of sector pulses from 3 to 255.

This selection will remain until another SET SECTOR command is issued or upon re-powering-up, at which time, it will use the switch settings.

4.3.3 Diagnose (Optional)

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0
0 TEST NUMBER							

This command and op code are reserved for future use.

4.4 DATA TRANSFER

4.4.1 Media Initialization Figure 4-5

New media or media which has had a format change must first be formatted before data can be written onto the disk. Please refer to Section 5 for format requirements.

The cylinder and track are selected in accordance with the previously mentioned procedure. At INDEX time, WRITE gate is activated and the appropriate data is written.

4.4.2 Reading (Figures 4-6, 4-6A)

A. **Non-Imbedded ID Field**

Sixteen bytes after the SECTOR pulse, READ gate is activated. Zeros appear on the NRZ data out signal until the PLL is in sync or locked. Immediately following the SYNC byte is the ID or header field. At the end of the ID field, READ gate must be deactivated for a four byte time period and reactivated. This action enables the read circuitry to reaquire lock before the SYNC byte.

B. **Imbedded ID Field**

The READ gate is activated sixteen bytes after INDEX pulse and deactivated after the data field. READ gate must not be activated until at least 16μs have passed after WRITE gate is deactivated or the head is selected.

4.4.3 Writing (Figures 4-7, 4-7A)

A. **Non-Imbedded ID Field**

The READ gate must be activated sixteen bytes after the SECTOR pulse. At the end of ID field,

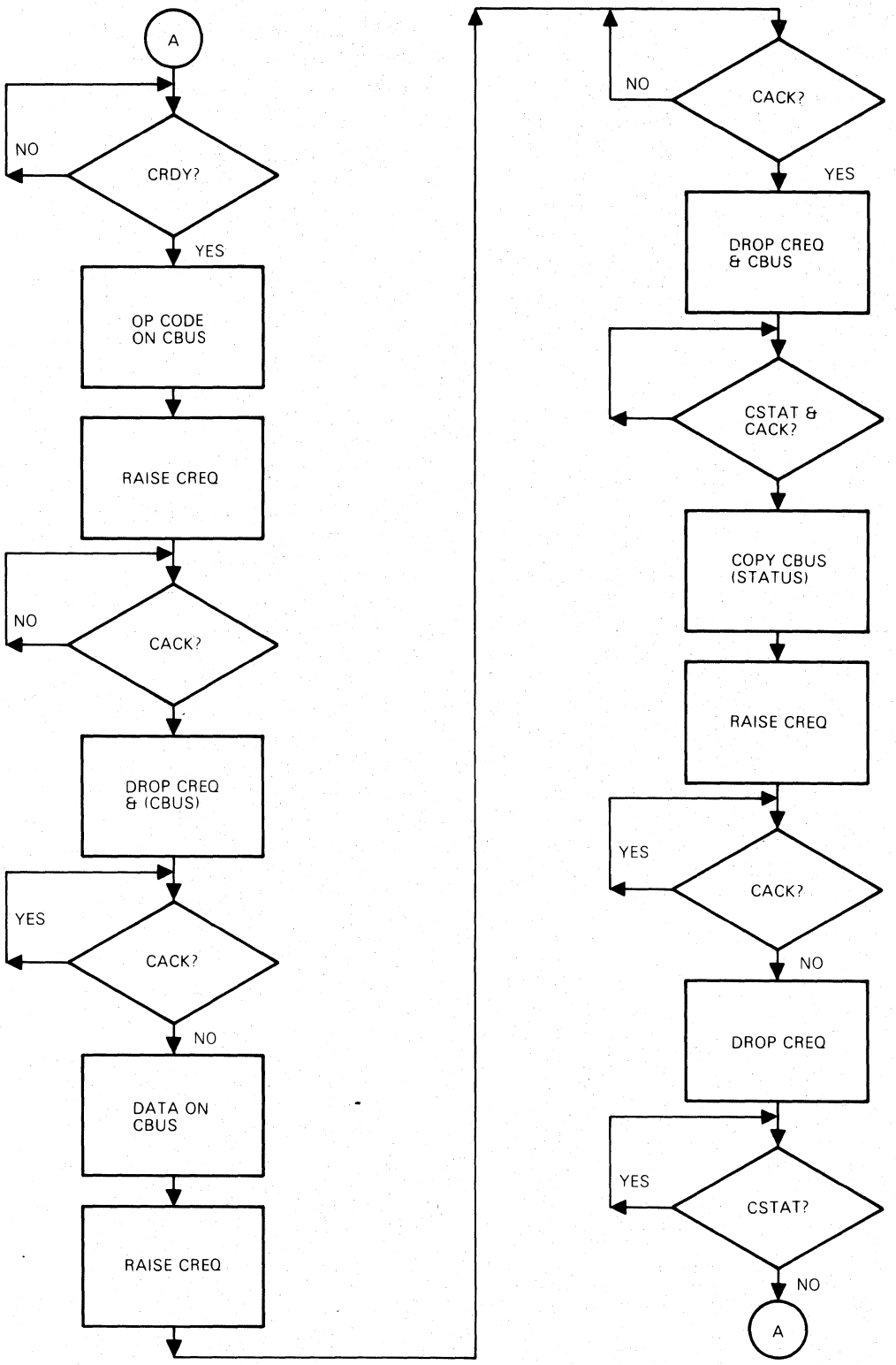


Figure 4-3. Two Byte Commands — Flow Chart (Suggested Procedure for User)

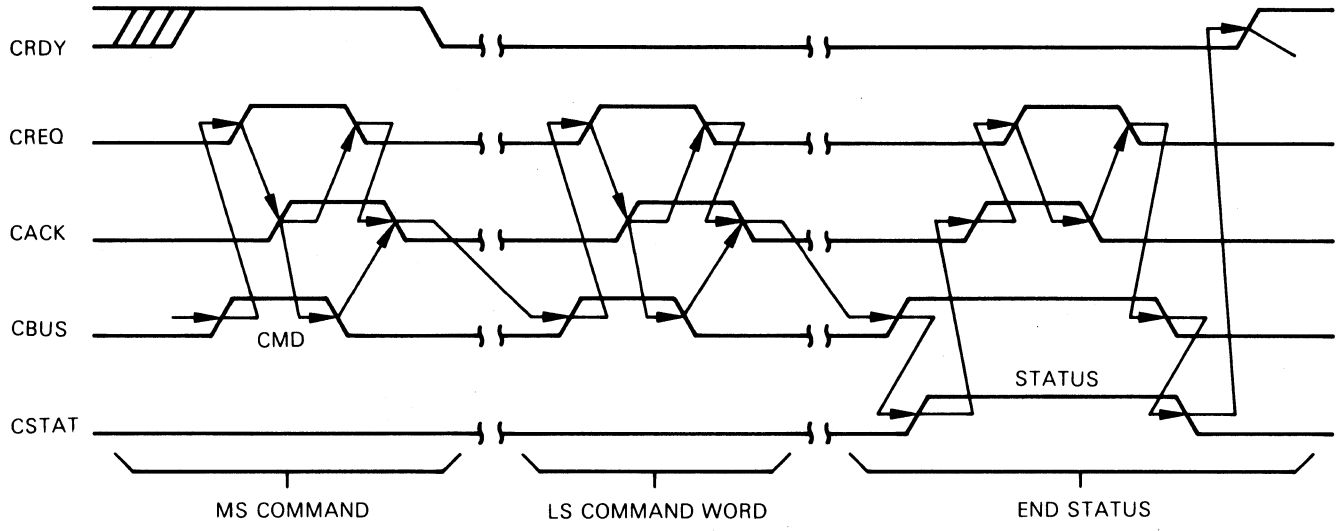


Figure 4-4. Two Byte Commands — Timing Diagram

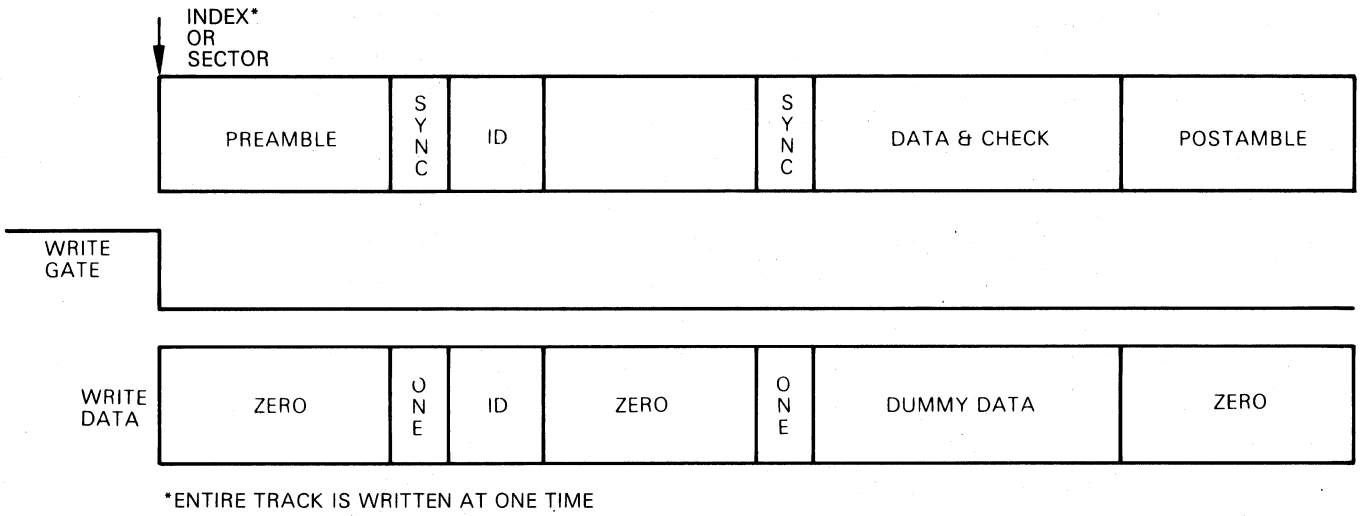


Figure 4-5. Media Initialization

READ gate is deactivated, WRITE gate is activated, and the appropriate data is written. WRITE gate is deactivated one byte into the postamble.

B. **Imbedded ID Field**

The WRITE gate is activated at SECTOR pulse time and deactivated one byte into the postamble.

4.4.4 Read Clock Phasing

The positive going transition of read clock should be used as the data strobe.

Write Clock Phasing

Since the MARKSMAN provides the write clock, the data/clock phase relationship is a function of the cable length and internal controller delays. This relationship, *measured at the disk drive*, should have the positive transition of the internal capture clock, Chip A46, pin 11, occuring nearest the center of the NRZ data, Chip A46, pin 12. Should this not be true, the connection between Test Points E20 and E21 should be broken and E20 and E22 established.*

*Below Rev. H, E21 is the output and the connection should be from E20 to E21 or E22 to E21.

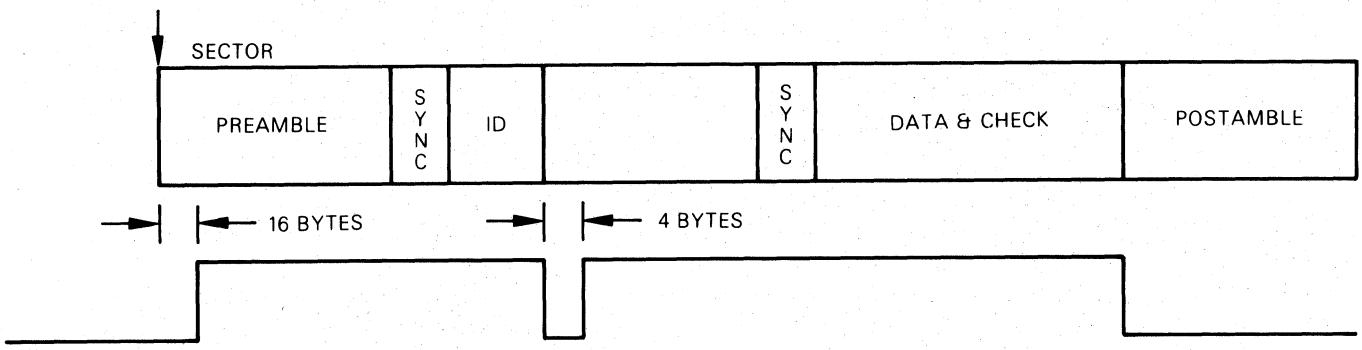


Figure 4-6. Non-Imbedded ID Field Read Timing

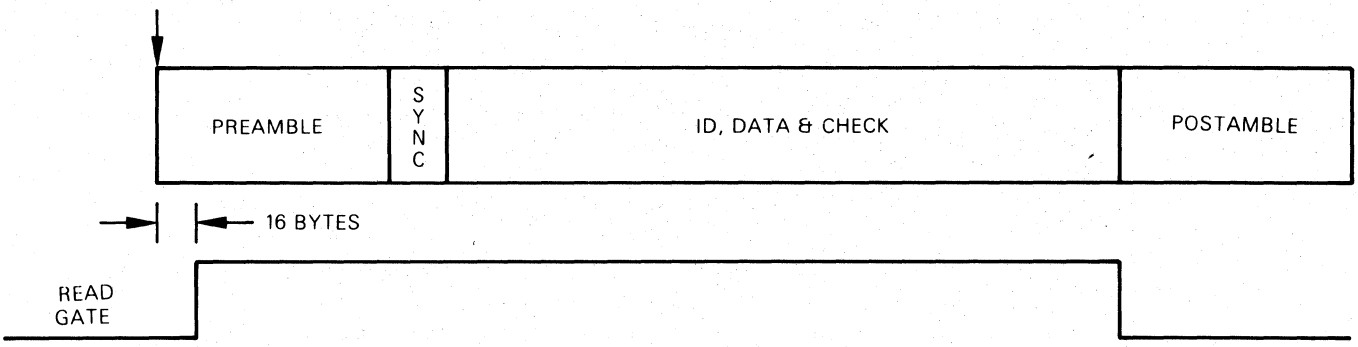


Figure 4-6A. Imbedded ID Field Read Timing

4.5 DRIVE MALFUNCTIONS & CONTROLLER ERRORS

The MARKSMAN internal logic monitors a number of conditions which, if they occur, will comprise data integrity. They are as follows:

Multiple Heads Selected
Write Unsafe (WRTUSF) signal is set. Resets when status is requested.

Write Command to Protected Head
Write Unsafe (WRTUSF) signal is set. Resets when status is requested.

Power Fault
Write Unsafe (WRTUSF) signal is set. Resets when status is requested.

Illegal Address Received
Bit 2 of status word is set. Resets when status is requested.

Spin Acceleration/Decelleration Out of Limit
Bit 4 of status word is set. Resets when status is read. Repeated operation when this condition exists could lead to excessive wear of the head and disk and result in data loss over a period of time.

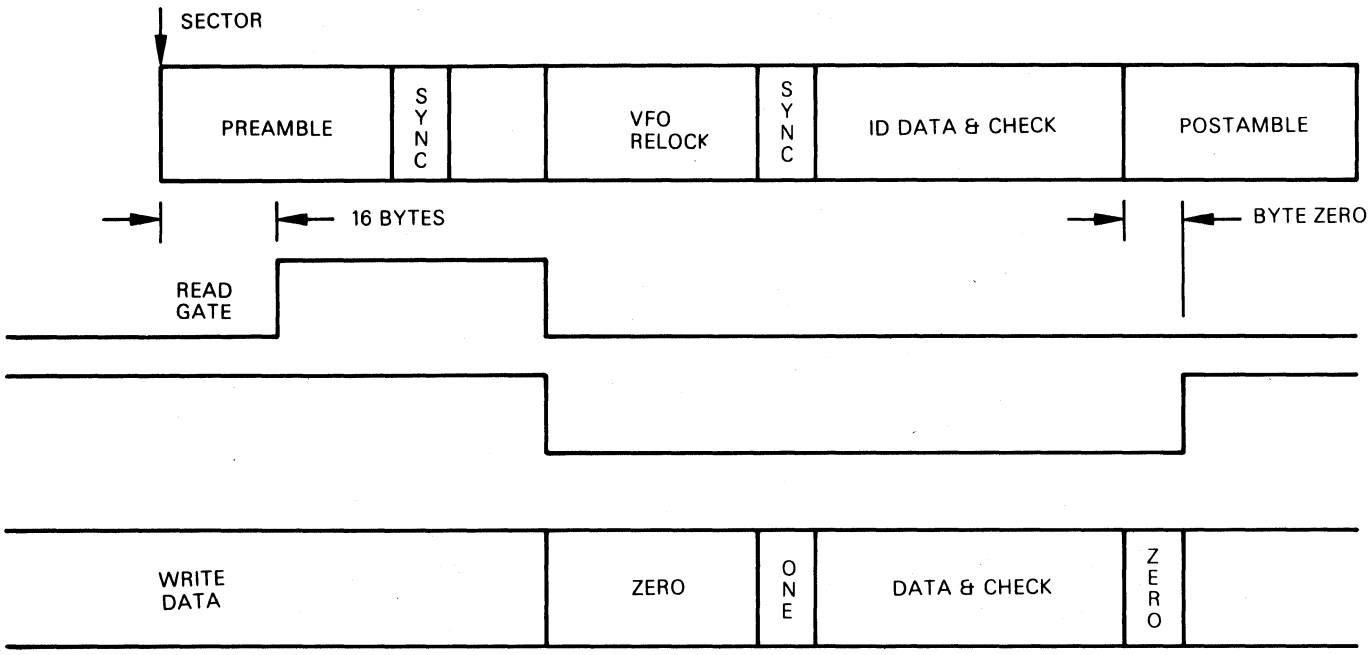


Figure 4-7. Non-Imbedded ID Field Write Timing

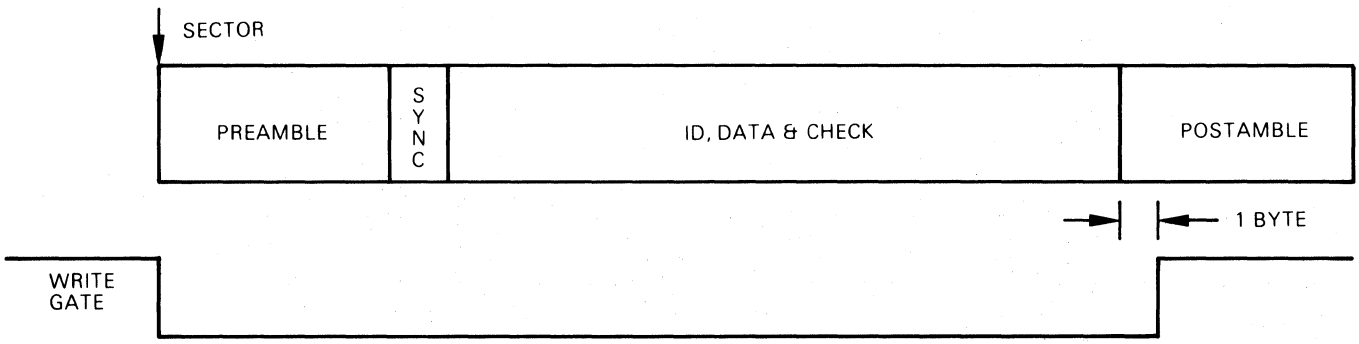


Figure 4-7A. Imbedded ID Field Write Timing

SECTION 5
FORMAT REQUIREMENTS

5.1 GENERAL

In order to guarantee operations over the entire temperature range, allow for component tolerances and compensate for cable and controller delays, all disk drives must have a preamble and postamble attached to each sector. The amount of overhead is a function of the electrical and mechanical tolerances and the bit transfer rate as well as the system requirements. The preamble and postamble contain all ZEROS.

5.2 FORMAT DEFINITIONS

Four different formats have been suggested for MARKSMAN. They are illustrated in Figure 5-1.

Format I requires the least amount of overhead. Format II is similar, but separates the header (ID) field from the data, allowing the data to be updated without rewriting the header. They are both designed for sequential operation, however, with either of the above formats, it

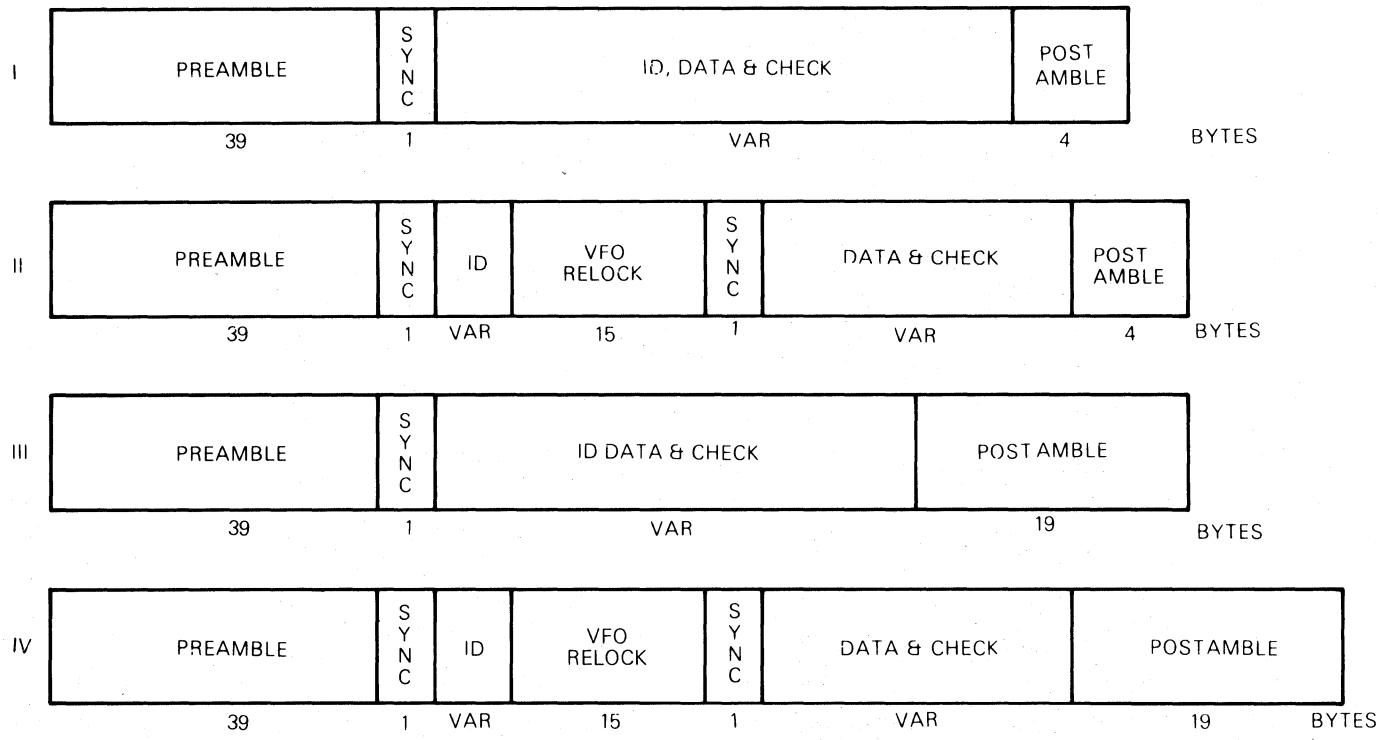


Figure 5-1. Sector Formats

is possible to miss the succeeding sector when a head advanced command is issued. Should this be undesirable, Formats II and IV have a larger postamble to insure that after a head advanced command is issued the succeeding sector is not missed.

5.3 SECTOR CALCULATIONS

The following formula is used to calculate the number of sectors for any given sector size. Table 5-1 and 5-2.

$$N = \text{INT}\ \frac{24000}{DATA + ID + OH}$$

WHERE: INT (Number) – Greater Integer Contained Within Number

N = number of sectors (whole integer)
Data = length of data field plus check characters
ID = length of header
OH = Length of overhead field
= 44 for Format I
= 60 for Format II
= 59 for Format III
= 75 for Format IV

The first N-1 sectors are of length = INT $(\frac{24000}{N})$ bytes. The last sector is of length = 24000 – [(N – 1) INT $\frac{24000}{N}$)]. Whenever it is necessary to change at the end of a track and continue operation without losing a revolution, and end-of-track pad, which accommodates the command execution and head switching, must be provided.

The command sequence for a no-motion seek takes over 500 μs (500 bytes) to complete, measured from the initial rise of CREQ to the rise of CRDY after end status. (The actual time depends on the controller's contribution to sequence delays). The target head is selected no earlier than 300 μs (300 bytes) after the initial rise of CREQ. The end-of-track pad for seek is, therefore, very large.

The use of the HEAD ADVANCE command sequence yields selection of the target head 11 μs to 25 μs after CREQ rises. READ gate must be delayed 16 μs after head selection, but does not occur (in the specified formats) until 16 bytes (16 μs) after the sector pulse, hence, the head-advancing CREQ must rise no later than 25 μs before the sector pulse. It may rise as early as 11 μs (10 bytes at low disk speed) before the end of the last data to be read. The minimum end-of-track pad for head advance is, therefore, 15 bytes. The raw sector length calculation above shows that most sector formats provide some inherent pad in the last sector.

Table 5-1. Number of Sectors Per Track

Sector Size	Format I	Format II	Format III	Format IV
128 Bytes	129	119	119	111
256 Bytes	76	72	72	69
512 Bytes	42	41	41	40
1024 Bytes	22	21	21	21

Assuming an 8 byte ID field and a 5 byte check character.

Table 5-2. Net Capacity (20 Megabytes)*

Sector Size	Format I	Format II	Format III	Format IV
128 Bytes	13.87	12.79	12.79	11.93
256 Bytes	16.34	15.48	15.48	14.84
512 Bytes	18.06	17.63	17.63	17.20
1024 Bytes	18.92	18.06	18.06	18.06

*(M-10 capacity is one half of that shown)

5.4 SECTOR SELECTION

The Sector Length switches (described in Section 7) determine the number of sector pulses that occur without the use of the SET SECTOR command. They select either 111, 69, 40, or 21 sectors per track. Ref. to Sections 7 for switch settings.

SECTION 6
SIGNAL LEVELS

6.1 CBUS0-7, CREQ, CACK

These signals interface directly to the Motorola MC6821 Peripheral Interface Adaptor (PIA).

Electrical Characteristics ($V_{CC}=5.0V+5\%, V_{SS}=0$, $T_A=T_L$ to T_H unless otherwise noted)

6.2 ALL OTHER SIGNALS

All other signals interface to 74LSXXX Logic. Refer to the IC manufacturer's literature for drive capability.

6.3 MATING CONNECTORS

Interface	3M # 3432-2002 or Cannon # UND4B040D3D
DC Power	Molex 1292-9R with 1189 sockets
AC Power	Molex 1991-4R with 1189 sockets

6.4 CABLE LENGTH

The drive is supplied with a four inch cable. The controller logic must be placed in close proximity to this cable. If additional cable length is required, the Driver/Receiver Option described in Appendix A or equivalent must be used.

Table 6-1. Electrical Characteristics

Characteristics		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	CRQ	I_{in}	–	1.0	2.5	Adc
Input High Current (V_{IH} = 2.4 Vdc)	CBUS0-7 CACK	I_{IH}	−200	−400	–	Adc
Input Low Current (V_{IL} = 0.4 Vdc)	CACK	I_{IL}	–	1.3	−2.4	mAdc
Output High Voltage (I_{load} = −200 μ Adc) (I_{load} = −10 μ Adc)	CBUS0-7 CACK	V_{OH}	V_{SS} +2.4 V_{CC} −1.0	– –	– –	Vdc
Output Low Voltage (I_{load} = 3.2 MAdc)		V_{OL}	–	0	V_{SS} +0.4	Vdc
Capacitance (V_{in} = 0, T_A = 25° C, F = 1.0 MHz		C_{in}	–	–	10	pF

Table 6-2. Interface Pin Numbers

J1-1	CACK	J1-21	SEC
2	RST/	22	GRD
3	CBUSO	23	CSTAT
4	CBUS1	24	GRD
5	SPARE	25	WRTCLK
6	CREQ	26	GRD
7	GRD	27	NRZIN
8	CBUS2	28	GRD
9	CBUS6	29	RDCLK
10	CBUS7	30	GRD
11	CBUS5	31	NRSOUT
12	CBUS3	32	GRD
13	SPARE	33	WRTGA
14	IDX	34	GRD
15	GRD	35	RDGATE
16	DRDY	36	SPARE
17	CRDY	37	SPARE
18	GRD	38	SPARE
19	1MHZ	39	WRTUSF
20	GRD	40	CBUS4

Table 6-3. DC Cable Pin Numbers (W/O Power Supply Option)

J2-1	+5V	J2-6	SPARE
2	GRD	7	+24V
3	−12V	8	+24V Stepper Ground
4	+12 (Output)		
5	GRD	9	SPARE

Table 6-4. AC Cable Pin Numbers (W/O Power Supply Option)

J3-1	AC High
2	AC Common
3	Chassis Ground
4	Spare

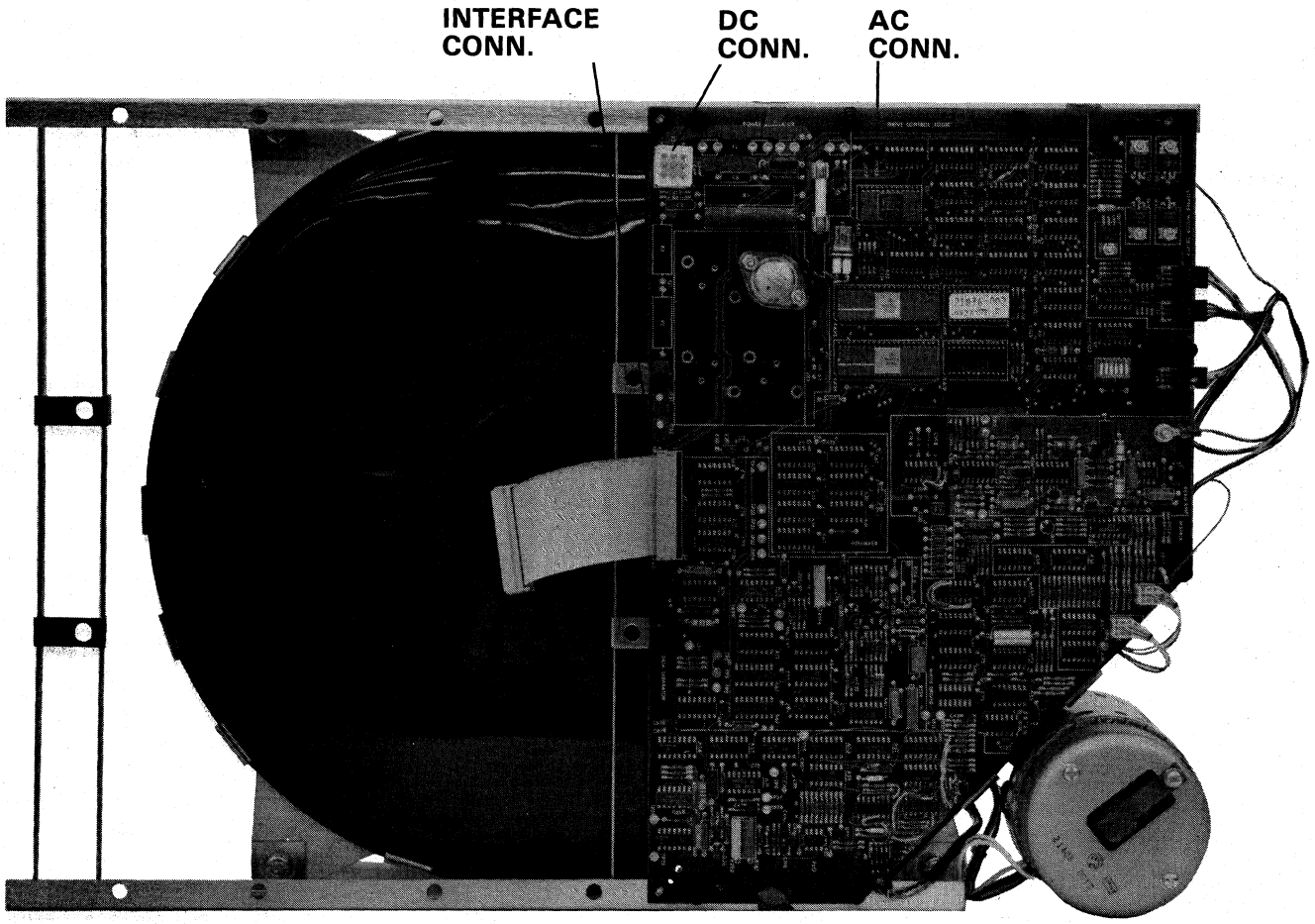


Figure 6-1. Connector Locations

SECTON 7
CONTROLS AND INDICATORS

7.1 GENERAL

Front Panel
None

Rear Panel
None

Internal
Location S-1 on the Basic Control PCB (Sector Length and Write Protect Switches). Tables 7-1 and 7-2.

Table 7-1. Number of Sector Switches

Switch S2		Number of Sectors	Sector Length (using Format IV)
−1	−2		
Closed	Closed	111	128 Bytes
Closed	Open	69	256 Bytes
Open	Closed	40	512 Bytes
Open	Open	21	1024 Bytes

Table 7-2. Write Protect Switches

Switch S1				Protected Head Number
−3	−4	−5	−6	
Closed	−	−	−	1
−	Closed	−	−	2
−	−	Closed	−	3
−		−	Closed	0

SECTION 8
ENVIRONMENTAL CHARACTERISTICS

8.1 TEMPERATURE (with or without optional enclosure)*

Equipment:	
Operational:	50°F to 104°F (10°C to 40°C) with a max. gradient of 18°F (10°C) per hour.
Equipment Non-Operational:	−40°F to 140°F (−40°C to 60°C)
Temperature Cycling:	No condensation shall result.

*without enclosure, 200 feet/minute air velocity must be maintained over the base casting.

8.2 HUMIDITY (with or without optional enclosure)

Equipment Operational:	10% to 90% R.H., with a wet bulb temp. limit of 80°F (27°C) (provided there is no condensation.)
Equipment non-Operational:	5% to 95% R.H., provided there is no condensation.

8.3 ALTITUDE (without optional enclosure)

Equipment Operational:	From 1000 feet below sea level to 6000 feet above sea level. Optional kit to 10,000 feet.

8.4 VIBRATION (with optional enclosure)

Equipment Operational:	The equipment shall withstand a peak displacement of ±0.006 in. (.015 cm) for the frequency range of 20 Hz to 40 Hz and ± 1g for the 40 Hz to 200 Hz range.
Equipment Non-Operational:	The equipment when packed for shipment shall withstand ±1.5g from 5 Hz to 55 Hz for one hour along each of the three mutually perpendicular axes, with a 20 minute sweep time.

8.5 SHOCK

The equipment shall perform all read/write operations (no seek) according to specifications, while being subjected to 18 impact shocks of 3g (±10%) consisting of 3 shocks along each direction of three mutually perpendicular axes. Each shock impulse shall be half sine wave with a time duration of 11 (±1) msec.

SECTION 9
POWER REQUIREMENTS

9.1 BASIC DRIVE

9.1.1 AC Power

100/115V (+10%, −15%), 50/60 Hz (±1 Hz)
Running: 1.5A
Starting: 11.0A

220/240V (+10%, −15%), 50/60 Hz (±1 Hz)
Running: 0.8A
Starting: 5.5A

9.1.2 DC Power

+24V, ±5%, 2.7A*

−12V, ±5%, 0.3A**

+5V, ±5%, 2.5A**

*Tolerance includes ripple less than 10 KHz. Greater than 10 KHz ripple should be less than 0.5%.

**Ripple must be less than +0.5% from 10 Hz to KHz.

9.2 POWER SUPPLY AND DRIVE

9.2.1 AC Power

100/115 (+10%, −15%) 60 Hz (±1 Hz)
Running: 3.5A
Starting: 13.0A

200/220/240V (+10%, −15%) 50 Hz (±1 Hz)
Running: 2A
Starting 6A

SECTION 10
PHYSICAL CHARACTERISTICS

10.1 PHYSICAL SIZE

	Basic Drive	Enclosure Option
Height	8.62" (219 mm)	8 ¾" (222 mm)
Width	16.24" (412 mm)	17 ½" (445 mm)
Depth	23.88" (607 mm)	27 ¼" (690 mm)
Weight	45 lbs. (20.0 kg)	85 lbs* (43.0 kg)

*110 lbs. (50 kg) with power supply option

10.2 MOUNTING ATTITUDES

Horizontal — spindle pully down
Vertical — unit on side motor on top

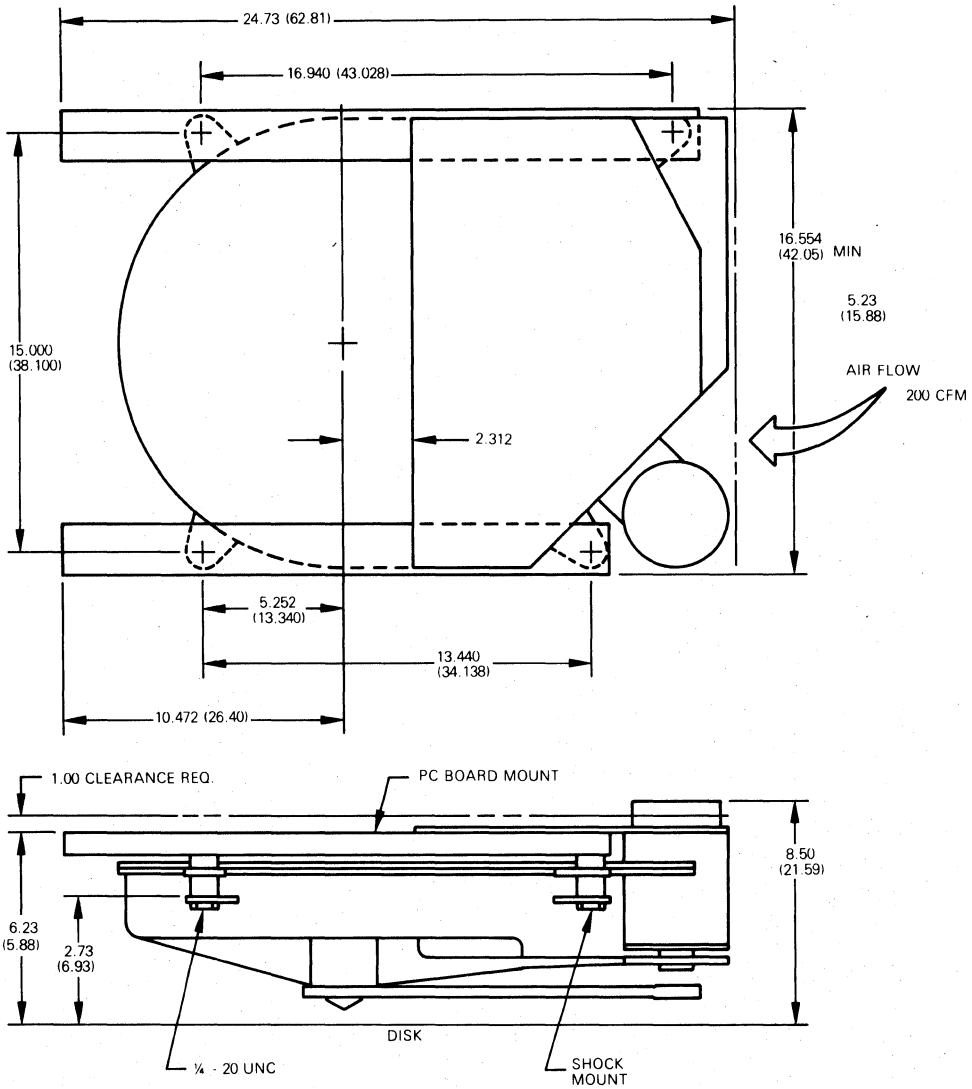


Figure 10-1 Basic Drive Dimensions

APPENDIX A
DRIVER/RECEIVER OPTION

GENERAL

The MARKSMAN Driver/Receiver Feature increases the allowable interface cable length of the MARKSMAN from 4 inches to 50 feet. It also provides the means by which drives may be daisy chained.

INTERFACE

Refer to Tables A-1 through A-4 for interface pin assignments.

Table A-1. Interface Pin Assignments — Bus

J1-	J2-	Serial Name	Source Ckt	Dest Ckt
1	1	GRD		
2	2	ICBUS 6/	75462	74LS240
3	3	ICBUS 5/	75462	74LS240
4	4	ICBUS 7/	75462	74LS240
5	5	ICBUS 2/	75462	74LS240
6	6	ICBUS 4/	75462	74LS240
7	7	ICBUS 0/	75462	74LS240
8	8	ICBUS 3/	75462	74LS240
9	9	ICBUS 1/	75462	74LS240
10	10	GRD		
11	11	GRD		
12	12	IRST/		74S367
13	13	GRD		
14	14	SPARE		

Table A-2. Interface Pin Assignments — Signal

J1-	J2-	Serial Name	Source Ckt	Dest Ckt
15	15	GRD		
16	16	IRDGATE/		74S367
17	17	GRD		
18	18	IWRGATE/		74S367
19	19	GRD		
20	20	ICREQ/		74S367
21	21	GRD		
22	22	IDRDY/	75462	
23	23	GRD		
24	24	ICRDY/	75462	
25	25	GRD		
26	26	IWRTSUF/	75462	
27	27	GRD		
28	28	ICACK/	75462	
29	29	GRD		
30	30	ISEC/	75462	
31	31	GRD		
32	32	IIDX/	74562	
33	33	GRD		
34	34	ICSTAT/	75462	
35	35	GRD		
36	36	TERMIN		
37	37			
38	38			
39	39			
40	40			

Table A-3. Interface Pin Assignments — Data

J3-	Serial Name	Source Ckt	Dest Ckt
1	GRD		
2	GRD		
3	IWDATAP	**	
4	IWDATAM	**	
5	GRD		
6	ISELECT		74LS132,
7	GRD		
8	IRDATAM	*	
9	IRDATAP	*	
10	GRD		
11	IRDCLKM	*	
12	IRDCLKP	*	
13	GRD		
14	IWRTCLKM	*	
15	IWRTCLKP	*	
16	GRD		
17	RCRDY	75462	
18	+5V		
19	+5V		
20	RSEC/	75462	
21	RIDX/	75462	
22	RSELECTED/	75462	
23			
24			
25			
26	GRD		

*See Table A-1
**See Table A-2

Table A-4. DC Pin Assignments

J6-	Serial Name
-1	+5V
-2	GRD
-3	-12V
-4	+12V
-5	GRD

APPENDIX B

Customer Designed Printed Circuit Board

Customer designed PCB's should meet the specifications in figure B-1. Since the T-2004 exerciser receives its power from the same cable which feeds this PCB, the power connector location and pin numbers (Figure 6-1) must be located as on the drawing. The MARKS-MAN optional enclosure expects the I/O cables to exit from the locations shown for the 40 pin and 60 pin connectors. If this enclosure is not used, these connectors may be relocated.

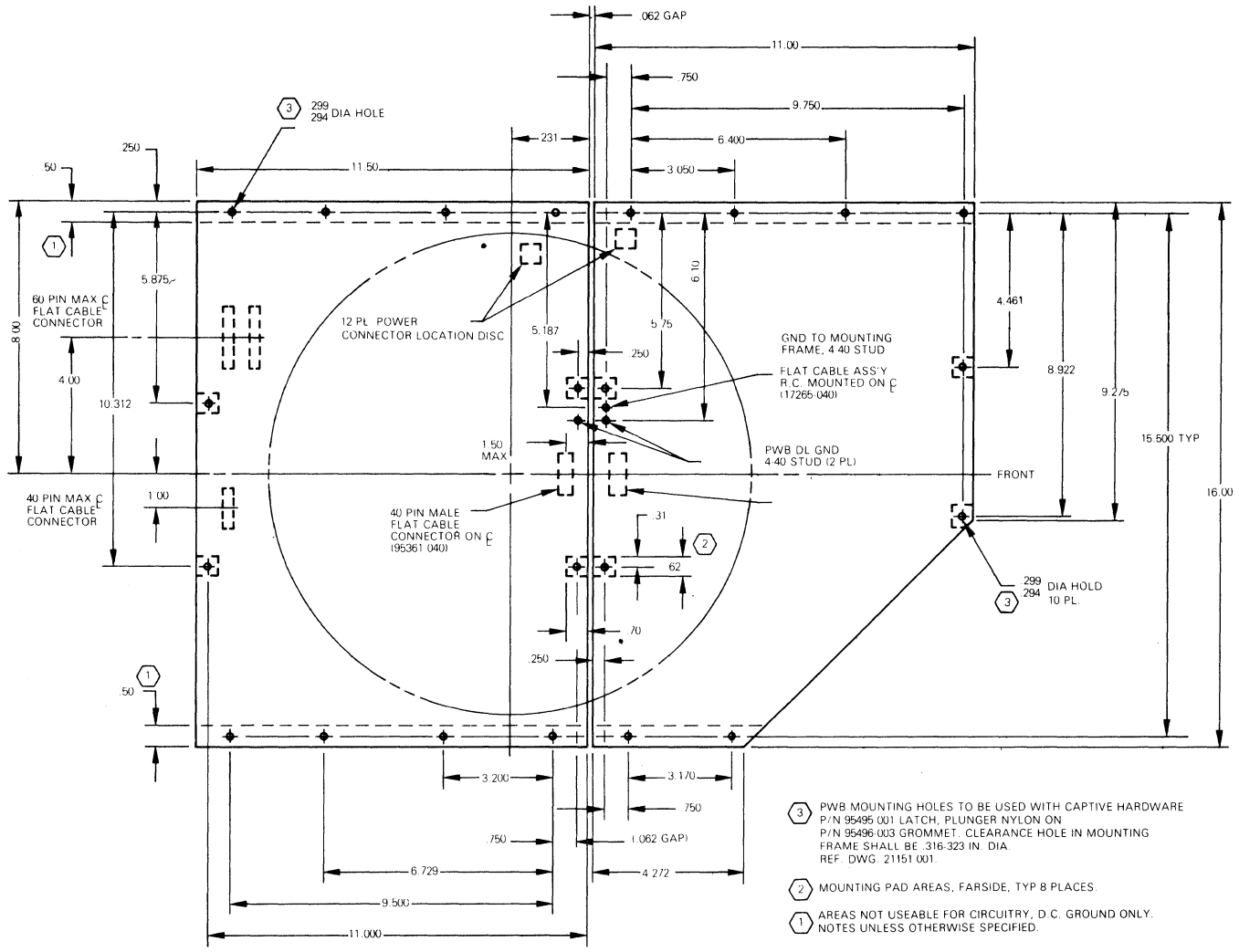


Figure B-1. Customer Designed PCB Physical Requirements

Century Data Systems
A Xerox Company

TECHNICAL MANUAL CHANGE

MANUAL TITLE		
MARKSMAN PERFORMANCE SPECIFICATION		
PART NUMBER	DATE	CHANGE NO.
76220-902	May 15, 1979	1
SHEETS:	AUTHORIZATION	
1 of 1	Leo A. Shaffer	

1. On page 4-5, add the paragraph 4.2.5 which is attached.

2. On page 4-5, delete the paragraph 4.3.3.

4.2.5 DIAGNOSE (Optional)

7	6	5	4	3	2	1	0
1	0	0	0	X	X	X	X

Where XXXX is the diagnostic test number.

Status is returned in extended status bytes 6 and 7.

Test No.

0 RAM Test stores 55_{16} in all RAM locations and checks contents of all locations. Stores AA_{16} in all locations and checks contents of all locations. Stores incrementing pattern in successive locations and checks contents of all locations. Exits with status bytes clear if OK. If bad, exits with diagnostic error flag set in status byte Ø, address of bad RAM location in extended status byte 6 and bit pattern of bad location in byte 7.

1 Real Time Clock Test - checks real time clock timeouts against programmed timeouts. Exits with status bytes clear if OK. If bad, exits with diagnostic error flag set in status byte Ø and appropriate bits set in extended status byte 6 as follows: bit 4 = timeout; bit 5 = unsolicited; bit 6 = interrupt; bit 7 = error. Status word 7 is always clear.

2 Track Zero Test - checks track at which track zero flag resets while stepping in and the track at which the flag sets while stepping out. Exits with extended status byte 6 containing track number at which track zero flag reset; status byte 7 contains track number at which it is set. If bad, diagnostic error bit is set in status byte 0 contains track number at which it is set. If bad, diagnostic error bit is set in status byte Ø and extended status bytes 6 and 7 contain FF_{16}.

3 Disk Speed Test - measures time between index pulses with real time clock. Exits with MSB of speed in status byte 6 and LSB in status byte 7. If bad, exits with diagnostic error bit set.

4 Read RAM - The contents of RAM are sequentially output to the user starting with address Ø.

5 ROM Test - builds a checksum for each 256 bytes of program PROM and compares it to a checksum table. Exits with status bytes clear if OK. If bad, diagnostic error bit is set and upper address of bad block is in extended status byte 6 and lower address is in byte 7.

6 MPU Test - a non-exhaustive MPU exercise which checks stack manipulation, addressing modes, interrupt and sub-routine linkage. Exits with the status bytes clear if OK. If bad, (although it is unlikely you will get this far) the diagnostic error bit is set and the condition code is returned in diagnostic status byte 6. Status byte 7 is clear.

7 Handshake Test - This is a two-byte command. The second byte will be echoed to the user as status. Normal status will not be presented and the diagnostic status bytes will not be changed. For effective testing of the user interface, the following sequence will test all data lines. ØØ, Ø1, Ø2, Ø4, Ø8, 1Ø, 2Ø, 4Ø, 8Ø, FF, FE, FD, FB, F7, EF, DF, BF, 7F (all in hex).

8 Seek Test - The seek test will seek from track ØØ to track N. N being track one and incrementing until N equuals track 212. It will verify that the carriage returns to track zero each time by looking at the track ØØ bit. If test fails, the last track that was successfully restored from N to zero will be stored in status byte 6. Byte 7 will be cleared and the diagnostic error bit will be set in status byte Ø. If test passes, status byte 6 and 7 and the diagnostic error bit in status byte Ø will all be cleared.

On power up or reset, the following diagnostic tests will be performed automatically:

RAM Test
ROM Test
MPU Test

On sequence up, the following diagnostic tests will be performed automatically:

Real Time Clock Test
Seek Test

If an error occurs, the diagnostic status bit in status byte Ø will be set, however the diagnostic status bytes (status bytes 6 and 7) will be unaffected. The user must then run each test to determine which test (s) failed.

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