CHROMATICS

CGC 7900 COLOR GRAPHICS COMPUTER SYSTEM

Disk DMA Interface
Technical Reference Manual

Printed 1 Jun 83
Part Number 070225

Table of Contents

Section 1 -- Introduction

Section 2 -- Hardware Interface Description

Section 3 -- Software Interface

Appendix A -- Installation Procedure

Section 1 -- Introduction

The CGC 7900 Disk DMA Interface (DDMA) is a single CGC 7900 digital circuit board which allows the Disk Controller to perform Direct Memory Access transfers on the 7900 system bus.

The DDMA is shipped already configured for Idris and DOS usage. The following versions support the DDMA:

- Idris Version 3

- DOS Version 1.7

This manual describes functional characteristics and installation procedures for the DDMA.

Section 2 describes the digital hardware.

Section 3 describes the software interfaces.

Appendix A describes installation procedures.

A diagram of the DDMA board, showing jumper and connector locations, is on page 2.

J5 -- Disk

```
3 2 1 | 6 5 4 3 2 1
```
BGLVL
ILVL

```
3 2 | 6 5 4 3 2 1    J10
```

(Priority
Connector)
-- P3 --

☐ J11

☐ J12

☐ J6

IRQ   BG   BRQ
☐   ☐   ☐
J9   J8   J7

--P2--

--P1--
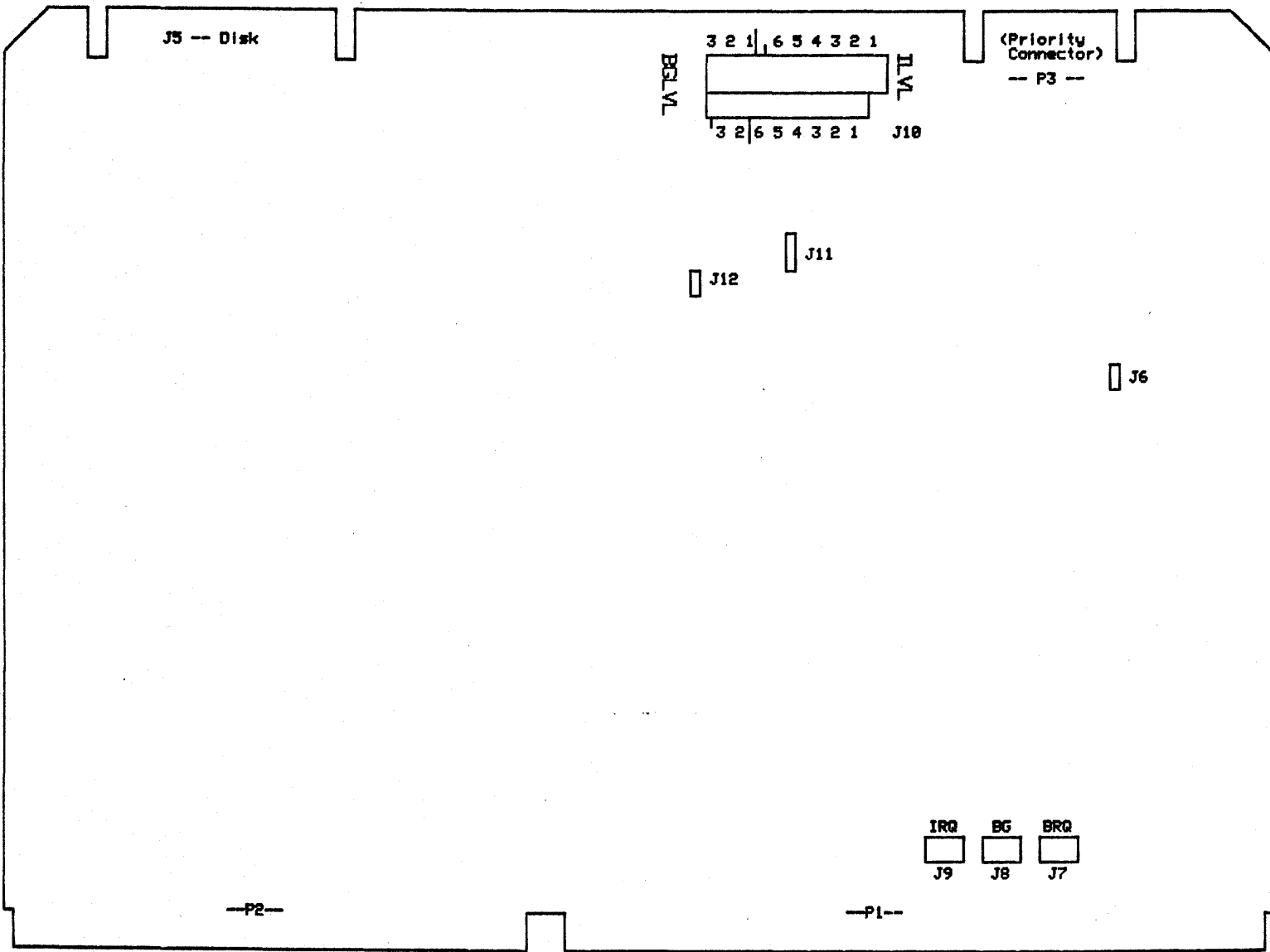
DDMA Board Layout

Section 2 -- Hardware Interface Description

2.1 System Connections

The DDMA has 4 connections to different parts of the 7900:

P1   is the main CPU bus connection.

P2   connects to the video bus and is not used by this board.

P5   is the connector to the Disk Controller.

P3   is the Bus Grant and Interrupt Priority connector.

2.1.1 P1 -- System Bus Connector

The **P1** connector on the DDMA contains all data, address, and control signals used in the transfer of information within the CGC 7900. This is a 140-pin card edge connector and is part of the 7900 mother board. All but four signals are buffered using 74LS240s, 74LS244s, and 74LS245s. The four exceptions are DTACK, BGACK, IRQ(X), and BRQ(X). These four signals are open collector type, and are driven using 74LS38s and 74LS09s.

2.1.2 P5 -- Disk Interface Connector

Connector **P5** is the interface to the Disk Controller. This is a 50-pin right angle locking connector located at the outer edge of the DDMA. The signals on this connector conform to the Shugart Associates Standard Interface Specification (SASI) described in the the OMTI User Manual. See Figure 1 in section 2.2 for the connector pinout and signal descriptions.

2.1.3 P3 -- Bus Grant and Interrupt Priority Connector

Connector **P3** is a 26 pin card edge connector used to daisy chain interrupts and bus grant signals within the CGC 7900. The position at which the DDMA will sit in the chain is selected by jumpers located on the circuit board (see section 2.4).

2.2 P5 Signal Descriptions

Pin no.	Signal Name	Pin no.	Signal Name	
1	Ground	2	Data Bit 0	
3	Ground	4	Data Bit 1	
5	Ground	6	Data Bit 2	
7	Ground	8	Data Bit 3	
9	Ground	10	Data Bit 4	
11	Ground	12	Data Bit 5	
13	Ground	14	Data Bit 6	
15	Ground	16	Data Bit 7	
17	Ground	18	Parity Bit	
19	Ground	20	No Connect	
21	Ground	22	No Connect	
23	Ground	24	No Connect	
25	Ground	26	No Connect	
27	Ground	28	No Connect	
29	Ground	30	No Connect	
31	Ground	32	No Connect	
33	Ground	34	No Connect	
35	Ground	36	BUSY	(BSY)
37	Ground	38	ACKNOWLEDGE	(ACK)
39	Ground	40	RESET	(RST)
41	Ground	42	MESSAGE	(MSG)
43	Ground	44	SELECT	(SEL)
45	Ground	46	CONTROL/DATA	(C/D)
47	Ground	48	REQUEST	(REQ)
49	Ground	50	INPUT/OUTPUT	(I/O)

Figure 1. Disk Interface Connector (P5).

NOTE:

All signals are active low at the interface connector.

Signals on the Disk Interface Connector are used as follows:

Data Bits 0-7   Bi-directional data path between the Disk Controller and and the DDMA circuit board.

BUSY   When active, indicates that a Controller operation is taking place.

ACKNOWLEDGE   Response by the DDMA to the Disk Controller indicating that data is ready to be transferred or has already been transferred.

RESET   Causes controller to halt the present operation and return to an idle state.

MESSAGE   Pulsed active by the controller to indicate that the status byte for the present operation is now on the data bus. Also indicates end of operation.

SELECT   Driven by the host to indicate to the controller that a new command is ready to transfer. Reset by the controller with the BUSY signal.

CONTROL/DATA   Driven by the controller to indicate the type of information presently being transferred across the data bus.

REQUEST   Driven by the controller, to request the transfer of data to or from the controller.

INPUT/OUTPUT   Driven by the controller to indicate the direction of the transfer.

2.3 Data Transfer Control

All data transferred between the Disk Controller and main memory is done using DMA operations.

Since the interface transfers data one byte at a time, the DDMA will word-pack the bytes before transferring them into main memory. This operation reduces the number of bus requests by 50% and decreases the overall bus time required by the transfer.

2.4 Hardware Jumpers

Two DDMA circuit boards can operate in a 7900 at the same time. For this reason, certain functions of the board are jumper selectable. The functions selected by jumpers on the circuit board are:

1) Address
2) Bus Master Level
3) Interrupt Level
4) Interrupt Vector

2.4.1 Address Selection

Jumper location J6 is used to select the base address of the DDMA registers. With the jumper in the 500 position, the registers will begin at $FF8500; with the jumper in the 510 position, the registers will begin at $FF8510.

2.4.2 Bus Master Jumpers

There are six bus master levels available in the 7900, numbered 0 through 5. Several of these levels are reserved for options supplied by Chromatics, as follows:

0 - Raster Processor   3 - Disk DMA Interface
1 - Hardware Vector Generator   4 - Available to User
2 - PIO/DMA   5 - Available to User

Level 3 has been assigned to the DDMA. To assign the DDMA, put a jumper in position 3 at jumper location J7 and J8, and BGLVL1 at J10. Jumper J7 insures that the Bus Request is made at Level 3 and J8 insures that the corresponding Bus Grant signal is received at Level 3.

Jumper J10 is used for Bus Master level expansion and is discussed in section 2.4.5.

2.4.3 Interrupt Level Jumpers

There are seven interrupt levels available in the 7900. Level assignments are as follows:

1 - Serial Port Controller   5 - CPU
2 - Available to User   6 - Available to User
3 - Available to User   7 - Power up and Parity Error
4 - CPU

NOTE:

The PIO/DMA board can operate at _any_ available interrupt level. If you have more than one PIO/DMA board, make sure that there will be no conflict between it and the DDMA.

Two of the four available interrupt levels are accessible by the DDMA circuitry. Jumpers J9 and J11 are used to select the interrupt level of the DDMA. Note that J11 has only two positions (2 and 6) while J9 has four (1, 2, 3 and 6). Placing a jumper in position 2 of both J9 and J11 will set the interrupt level of the DDMA to 2 and position 6 will set it to 6. Positions 1 and 3 of J9 MUST NOT be used.

2.4.4 Interrupt Vector

Jumper J12 selects the interrupt vector location for the DDMA. With J12 installed, the interrupt vector is at location $144. With J12 removed, the interrupt vector is at location $154.

2.4.5 Level Expansion

In order to allow for multiple I/O boards to share the same interrupt and Bus Master level, an expansion connector (J3) has been provided. By using a 26-pin card edge connector, multiple I/O boards can be sequentially prioritized (or "daisy chained") within levels.

2.4.5.1 Bus Master Level Expansion

If two Bus Master boards are to share the same Bus Master level, the jumper used to select the Bus Request Level (J7) must be the same on both boards. Designate the higher priority board with a jumper at J8 and another jumper in BGLVL1 at J10. The lower priority board will NOT have a jumper on J8 and will have a jumper at BGLVL2 of J10.

Now, if a bus request is made by the second board in the chain, the first board will receive the bus grant. Since it has not requested the bus, it will send the signal to the second board in the system.

2.4.5.2 Interrupt Level Expansion

If two boards are to share the same interrupt level, the jumpers at locations J9 and J11 must be the same for both boards. Install jumper J12 for one and remove the jumper (if any) on the other. This sets the interrupt vector locations for the boards; see section 2.4.4.

The higher priority board will have a jumper installed at position ILVL1 of J10. The lower priority board will have a jumper at ILVL2 at J10.

Section 3 -- Software Interface

This section describes the registers used for the disk interface. The descriptions are mainly for illustration; Idris and DOS drivers for the DDMA are available from Chromatics.

3.1 Register Descriptions

There are three registers which will be used for Disk transfers:

1)   The <u>Address Register</u>, located at $FF8502

2)   The <u>Control/Status Register</u>, located at $FF8507

3)   The <u>Command Register</u>, located at $FF8500

NOTE:

These addresses assume jumper J6 is in the 500 position. For the 510 position, add $10 to each address.

3.1.1 Address Register

The Address Register is a 23-bit read/write register which is loaded with the starting <u>word address</u> of the transfer to be performed. (The <u>word address</u> is the normal byte address shifted right one bit.) This register is a **long word** register located at $FF8502.

Example:

The block of data to be transferred starts at address $100120. Let register A7 contain this address:

| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Shift it right one bit to form the word address:

    LSR.L   #1,A7

This value is $080090.

| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Store it in the Address Register:

    MOVE.L   A7,$FF8502

3.1.2 Control/Status Register

The Control/Status Register is an 8-bit register which contains control and status information pertaining to the Disk interface. The register is defined below:

Control/Status Register

Address: $FF8507 (Byte)

```
 ┌─┬─┬─┬─┬─┬─┬─┬─┐
 │7│6│5│4│3│2│1│0│
 └┬┴┬┴┬┴┬┴┬┴┬┴┬┴┬┘
  │ │ │ │ │ │ │ └── IED   (R/W)
  │ │ │ │ │ │ └──── Not Used
  │ │ │ │ │ └────── AIE   (R/W)
  │ │ │ │ └──────── DRSET (R/W)
  │ │ │ └────────── PER   (R/W)
  │ │ └──────────── DxDone (R)
  │ └────────────── Not Used
  └──────────────── NEX   (R)
```
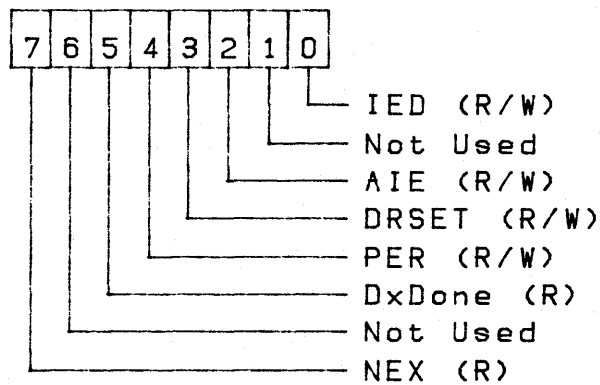
(R/W) - Read/Write Bit

(R)   - Read Only Bit

Each bit is described as follows:

Interrupt Enable Disk (IED)

This bit enables interrupts to occur upon completion of the next disk operation. (Active = 1)

Address Increment Enable (AIE)

This bit enables incrementing of the address register at the end of each DMA cycle. (Active = 1)

Disk Controller Reset (DRSET)

This bit resets the Disk Controller and all associated interface circuitry. This bit must be cleared to enable the Disk Controller. Delay at least 100 microseconds before issuing any new commands to the controller. (Active = 1)

Parity Error (PER)

This bit indicates that during the last data transfer from the Disk Controller, a parity error was detected in one of the data bytes. Clear this bit by setting DRSET to 1. (Active = 1)

NOTE: Parity checking is currently disabled on the Disk Controller; thus, this bit can be ignored. To enable parity checking, move the P/P-NOT jumper on the Disk Controller to position P.

Disk Transfer Done (DxDone)

This bit indicates that the Disk Controller has completed all requested operations and is ready to receive another command descriptor block. This bit is reset when the completion status is read back from location $FF8500. (Active = 1)

Non-Existent Memory (NEX)

This bit indicates that the last DMA operation attempted was to a non-existent area of memory. Clear this bit by setting DRSET to 1. (Active = 1)

3.1.3 Command Descriptor Register (CDR)

This is a 16-bit register which is used to:

1) Transfer <u>Command Descriptor Blocks</u> (CDBs) from the CPU to the Disk Controller.

2) Transfer completion status messages from the controller to the CPU.

During a command transfer, the CDB is written out to location $FF8500 with the first byte of each word in the high 8 bits.

Example:

```
First word      15              8 7              0
                +---------------+---------------+
                |    byte 1     |    byte 2     |
                +---------------+---------------+


Second word     15              8 7              0
                +---------------+---------------+
                |    byte 3     |    byte 4     |
                +---------------+---------------+


Third word      15              8 7              0
                +---------------+---------------+
                |    byte 5     |    byte 6     |
                +---------------+---------------+
```

The CPU write operations and the associated DTACK signal are interlocked with the control signals at the disk interface. This feature eliminates the need for bit checking between words of the CDB.

When a disk operation is complete, two bytes of Completion Status are transferred from the controller to the interface. These two bytes are read be the CPU at location $FF8500. The status byte is in the high byte and the completion message is in the low byte.

3.2 Interrupt Vectors

There is one interrupt vector associated with the DDMA. Depending on jumper J12, it is either at location $144 or location $154 and is used to indicate completion of a disk operation. See section 2.4.4, "Interrupt Vector Jumper."

In order for interrupt processing to occur, the Interrupt Enable bit must be set to 1 in the Control/Status Register.

3.3 Disk Controller Software Interface

Once the operations discussed in section 3.1 are completed (i.e.: Address Register and Control/Status Register setup), Disk Controller Operations can be initiated.

A Disk Controller operation is initiated by writing out the desired Command Descriptor Block (CDB) to location $FF8500. This is a word operation with the most significant byte in the high eight bits and the least significant byte of the word in the low eight bits. This operation is repeated until the entire CDB is transferred. These write operations can be performed one after another with no checking or waiting between words.

Once the CDB is completely transferred, the DMA operation (if the CDB requires one) will start automatically. Transfer completion can be determined by polling the DxDone bit in the Control/Status Register, or by setting up the Interrupt Enable bit and associated Interrupt Vector location.

Upon completion of the operation, the completion status of the transfer is read back from location $FF8500, with the status byte in the high byte. The completion message byte is in the low byte. This read operation resets the DxDone bit and the interrupt.

Appendix A -- Installation Procedure

The DDMA is shipped configured for operation with the DMA versions of Idris and DOS. Use the following procedure to install the DDMA and associated software:

1) Power down the 7900 and open the back door of the unit.

2) Remove the air filter panel below the back door.

3) Remove the card edge connector from P9 on the CPU board.

4) Remove the heat shrink tubing from the inline disk adapter board. This board is attached to the cable that was just removed from the CPU.

5) Unplug the 50-pin cable coming from the Disk Controller from the inline adaptor board.

6) Plug this 50-pin cable into J5 of the Disk DMA circuit observing pin 1.

7) Install the Disk DMA board into the 7900 card cage as close to the CPU as possible.

8) Replace the air filter panel below the back door.

9) Remove the Raster Processor from the card cage and replace the DOS and Idris PROMS with the DMA versions (if not already installed).

10) Insert the Raster Processor into the 7900 Mother Board.

11) Replace the air filter panel, close the back door, connect power and boot either Idris or DOS.

If you have any problems, contact Customer Service.

The DDMA, as shipped, is configured as follows:

Base Address	= $FF8500	Interrupt vector	= $144
Bus Master level	= 3	Daisy chain levels	= 1
Interrupt level	= 6		