Technical Manual No.
799816-007
Revision B

MODELS M890 AND M891 CACHETAPE UNIT

VOLUME II

THEORY OF OPERATION

Cipher Data Products
10225 Willow Creek Road
San Diego, California 92131

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SECTION I

DESCRIPTION AND SPECIFICATIONS

PHYSICAL DESCRIPTION

1-1. The CacheTape Unit (CTU) is a dual-speed, dual-density tape transport manufactured by Cipher Data Products, Inc., San Diego, California. The CTU is designed to be rack-mounted in a standard 19-inch equipment rack. All components are mounted on a precision-machined, cast aluminum plate. When the equipment rack is securely anchored, the PWB and other internal components can be made accessible from the front by releasing the equipment latch located inside the front panel (bottom) and pulling the CTU forward on slides.

1-2. The CTU simulates traditional tape drives by means of an internal cache memory that performs the logical functions of a physical drive. The host system interfaces directly with the logical drive. Data records from the host are stored in cache memory and then written on tape by the physical drive, independent of the host. The physical drive is thus virtually transparent to the host system.

1-3. There are two CTU models: the Model M890 and the Model M891. Each model records at 1600 bytes-per-inch (BPI), and each has an option of recording at 3200 BPI. The primary differences in the two models are performance factors. The Model M890 has a maximum data transfer rate of 120 kilobytes-per-second (KBS) and has built-in start delays to simulate the physical tape ramp time of conventional start/stop transports. The Model M891 has a maximum data transfer rate of 384 KBS and has the capability of burst mode operation in which the simulated ramp delays are not used. The burst mode is switch-selected during system setup.

1-4. There are two different access positions for the CTU. The first position, operator maintenance access, provides accessibility to the supply reel, head, and tape roller guides. The second position, service access, provides access to all electronic components as well as mechanical parts. Refer to Volume I for instructions on each position.

PHYSICAL TAPE DRIVE MECHANISM

1-5. The reel-to-reel drive mechanism employs two direct-drive, dc, torque motors to drive the tape reels. An optical tachometer assembly on the takeup hub regulates tape speed. Tape tension is maintained at approximately 7 ounces by a single tension arm.

1-6. The tape path includes roller guides, a dual-gap head, and a tape cleaner. All roller guides incorporate precision bearings to minimize friction and wear. The roller guides, positioned on both sides of the head, utilize polished ceramic washers to guide the tape across the head. This arrangement minimizes skew and the effect of tape-width variations.

1-7. A tape cleaner is mounted adjacent to the head to minimize tape contamination.

FUNCTIONAL DESCRIPTION

1-8. Figure 1-1 is a system block diagram. The CTU can be functionally divided into the logical tape unit and the physical tape unit, both of which are controlled by the Z8002 microprocessor. The logical unit consists of the cache memory and associated logic circuits, while the physical unit consists of the read/write circuits, read/write head, the physical drive mechanisms, and the related sensing and controlling devices. The DMA controller, under the overall control of the microprocessor, directly controls the cache memory.

1-9. The microprocessor is supported by 16K words of control storage (ROM) and 2K words of RAM. The microprocessor also has analog input and output ports for diagnostic purposes, control of motor drivers, and read threshold selection.

1-10. The interface logic in the CTU consists of the following:

a. Read/write latches and strobes.

b. Command and status latches.

The read/write latches and strobe logic are connected to the DMA controller and cache memory through device request logic. The microprocessor determines the rate of access. The command and status latches interface directly with the microprocessor logic. The host interface communicates only with the logical tape drive.

1-11. Cache memory consists of nine 64K dynamic random access memories (DRAM's). The memory is logically a circular buffer and is addressed by the DMA controller. The four channels of the DMA controller perform the following services in the priority listed:

a. Physical tape drive

b. Logical tape drive

c. Microprocessor/Cache memory communications

d. DRAM refresh

1-12. The write formatter is under the direct control of the microprocessor. The ID burst, preamble, postamble, and file mark are generated internally by the formatter. The formatter output is sent to the write electronic circuits, which drive the physical tape drive head to write the formatted data on the tape.

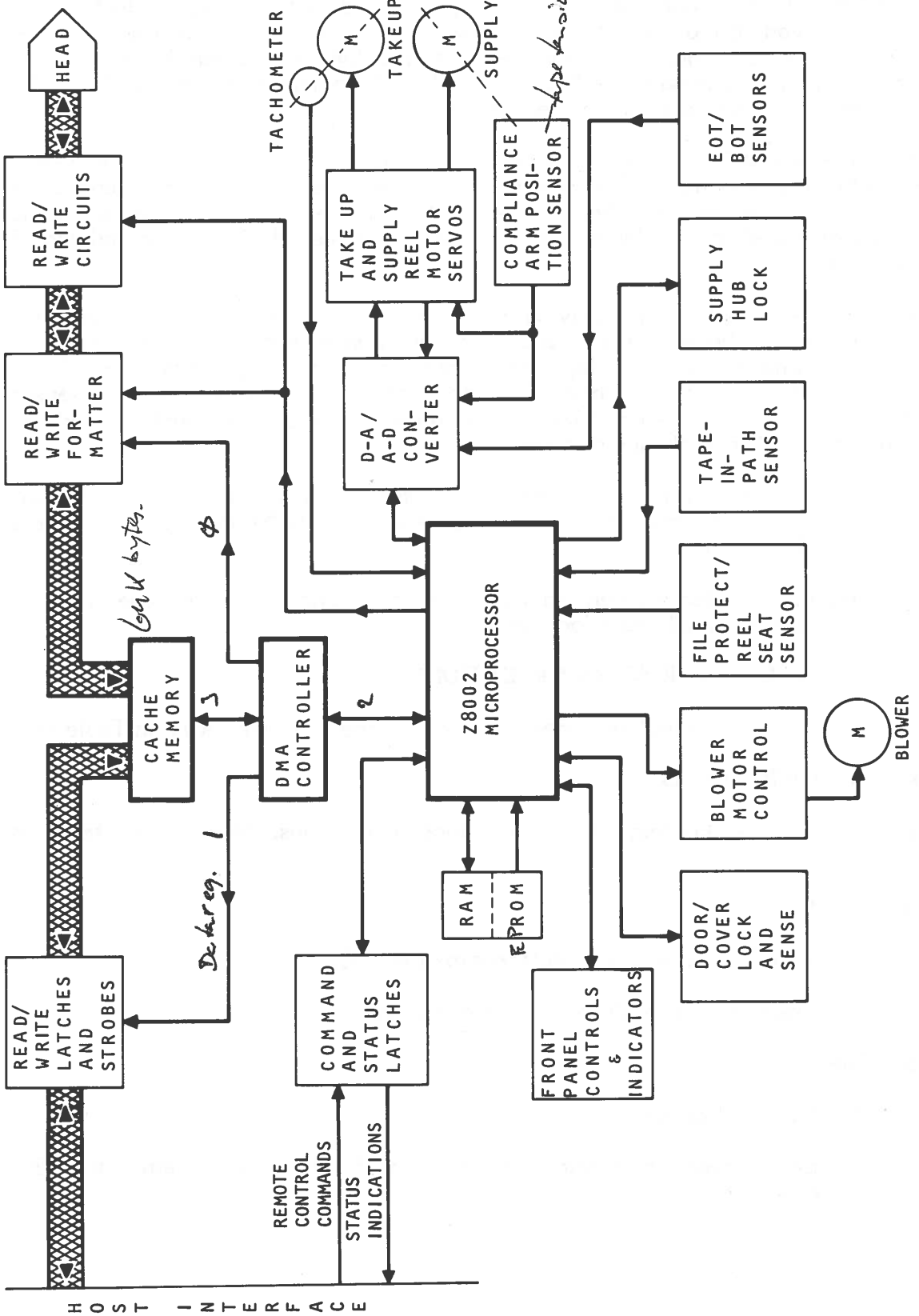

Figure 1-1. System Block Diagram

1-13. During a read operation, the read electronic circuits recover the low-voltage read signals from the read head, condition the signals, and route the signals to the read formatter. The read formatter detects the polarity of the data transitions and sends input requests to the serial processing and skew buffer in the read formatter logic. When a full data character is assembled by the skew buffer, the buffer requests that the DMA controller recover the character and place it in cache memory.

1-14. Tape movement in the physical tape drive is controlled primarily by the takeup servo and tachometer assembly. The velocity information generated by the tachometer assembly is used to develop the drive voltage for the takeup motor. The tachometer is also used to derive position displacement information between the beginning and end of consecutive tape records.

1-15. The supply motor is the driving mechanism of a position servo loop that maintains the tape at the proper tension. The compliance arm is held at a position between its two limit stops. Any tape movement causes a change in position of the compliance arm, resulting in a feedback signal from the compliance arm position sensor to the supply reel servo. The servo adjusts or decreases the supply reel motor speed and direction to correct the compliance arm position.

1-16. The end-of-tape (EOT) and beginning-of-tape (BOT) sensors consist of two-channel infrared detectors operating on reflections from ANSI metallized markers applied to standard tape reels.

1-17. An infrared detector adjacent to the supply reel senses that the tape is in the tape path. This ensures reliable tape loading.

MECHANICAL AND ELECTRICAL SPECIFICATIONS

1-18. The mechanical and electrical specifications for the CTU are shown in Table 1-1.

INTERFACE SPECIFICATIONS

1-19. Table 1-2 and 1-3 contain a list of interface connections. Signal characteristics are as follows:

a. Levels

(1) True is low: 0 to +0.4 volt (approximately).

(2) False is high: +3.0 volts (approximately).

b. Pulses

(1) Levels as above.

(2) Edge transmission delay over 25 feet of cable is not greater than 200 nanoseconds.

1-20. The interface circuits are so designed that a disconnected wire results in a false signal. Figure 1-2 shows the interface configuration for which the transport is designed.

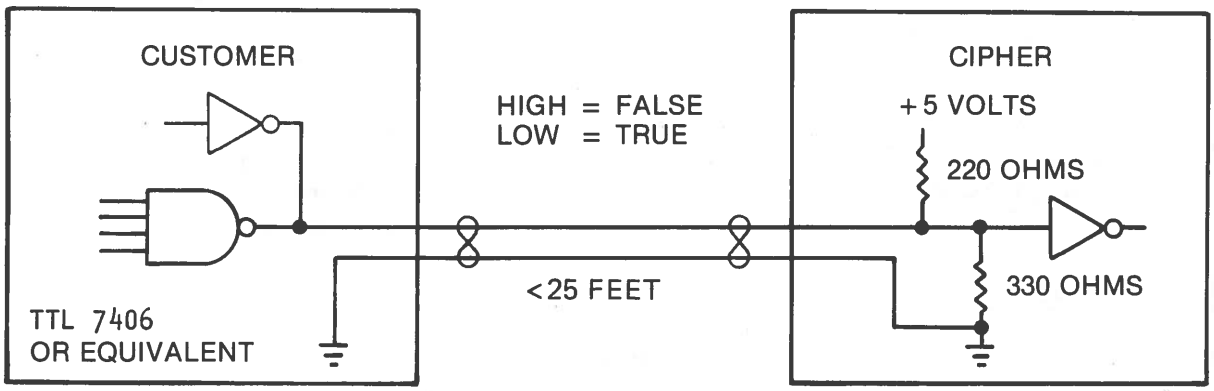

Figure 1-2. Interface Configuration

Recording Method	Phase Encoded (PE)	
Data Tracks	8	
Parity Tracks	1	
Density	1600 bpi standard, 3200 bpi optional	
Operation Speeds	100 ips (1600 bpi), 50 ips (3200 bpi)	
Character Rate (Kilobytes per second)	M890 20 kbs-120 kbs (Selectable)	M891 72 kbs -384 kbs (Selectable)
Burst Mode (Ramp Disable)	Not Available	Standard (Ramp may be inserted in logical interface by DIP switch selection.)
Physical Dimensions		
Height	8.75 inches (22.2 cm)	
Width	17.0 inches (43.18 cm)	
Width (front panel)	19.0 inches (43.26 cm)	
Depth (from mounting surface)	22.0 inches (55.80 cm)	
Overall Depth	24.5 inches (62.23 cm)	
Weight	82 pounds (37.65 kg)	
Environmental		
Operating		

NOTE

The ambient temperature must be such that media be retained within ANSI limits for data integrity to be maintained; i.e., 32 degree centigrade ambient maximum.

Dry Bulb Temperature	10° to 40°C
Wet Bulb Temperature	26°C maximum
Relative Humidity	20 to 85%
Barometric Pressure	20" Hg to 32" Hg (68 kPa to 109 kPa)
Altitude	Sea Level to 10,000 ft (3 km)
Temperature Shock	1 min. minimum per 1°C change
Generated Heat	270 watts rated maximum; 750 BTU/hour average maximum (vented to enclosure)

Table 1-1. Mechanical and Electrical Specifications

Non-operating (Long Term)	
Dry Bulb Temperature	-40° to 50°C
Wet Bulb Temperature	30° maximum
Relative Humidity	90% maximum
Altitude	Sea level to 10,000 ft (3 km)
Shipping and Short Term Storage	
Dry Bulb Temperature	-40° to 70°C
Wet Bulb Temperature	40°C maximum
Relative Humidity	95% maximum
Altitude	Sea level to 49,000 ft (15 km)
Vibration	
Operating	
Frequency Range	5 to 500 Hz
Peak Acceleration Level	0.3g
Application	Each direction of 3 orthogonal axes
Non-operating (in shipping container)	
Frequency Range	5 to 500 Hz
Peak Acceleration Level	1.5g
Application	Each direction of 3 orthogonal axes
Shock	
Operating	Undefined
Non-operating (in shipping container)	
Peak Acceleration	5g
Duration	5 to 50 ms
Waveshape	1/2 Sine
Application	Each direction of 3 orthogonal axes
Pollutants	
Dust	60 milligrams/1000 cu ft of air by weight of particles (5 micron diameter)

Table 1-1. Mechanical and Electrical Specifications (Continued)

Tape Speed (Determined by density)	100 ips (at 1600 BPI) or 50 ips (at 3200 BPI)
Long Term Speed Variation (LSV)	±1% of nominal
Instantaneous Speed Variation (ISV)	±2% of long term
Write Skew	300 micro-inches maximum
Rewind Speed	180 ips typical (10-1/2" reel)
Tape (computer grade) ANSI X3.40-1976	
Width	0.5 inch
Thickness	1.5 milli-inch
Reel Size	7 in, 8.5 in, or 10.5 in
Tape Tension	7 oz nominal
Data Reliability (errors other than media faults)	
Write	1 error in 10^8 bytes
Read Recoverable	1 error in 10^9 bytes
Read Permanent	1 error in 10^{10} bytes
Undetected	1 error in 10^{11} bytes
MTBF (20% duty cycle)	5,500 hours
MTTR (to isolate and repair major assemblies)	30 minutes
Interblock Gap	0.6 in
Formatter Interface	Industry compatible
Interface Impedance	130 ohms at 3 Vdc
Logic Low	0.4 Vdc maximum
Logic High	2.4 Vdc minimum
Rise/Fall	100 nanoseconds maximum
Cable Characteristics	28 AWG flat ribbon 22 or 24 AWG twisted pair
Daisy Chain	25 feet maximum

Table 1-1. Mechanical and Electrical Specifications (Continued)

Power	
Nominal input voltage (slow-averaged rms, including brownouts)	100, 120, 220, 240, 208, 230
Range of nominal voltage except 208, 230	+10%, -15%
Range of nominal 208, 230 voltage	+10%, -10%
Modulation	1% max
Harmonics (total)	10% max
Operating Frequency	
Frequency	49 to 63 Hz
Tolerance	included above
Rate of Change	1.5 Hz/sec max

Table 1-1. Mechanical and Electrical Specifications (Continued)

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P1	4	3	Last Word (ILWD)	Level	When true, during write, indicates that the character to be strobed into the formatter is the last character of the record.
P1	6	5	Write Data 4 (IW4)	Level	-
P1	8	7	Initiate Command (IGO)	Pulse	With CTU ready and on line, the command specified on the command lines is latched into the CTU on the trailing edge of IGO.
P1	10	9	Write Data 0 (IWO)	Level	-
P1	12	11	Write Data 1 (IW1)	Level	-
P1	18	17	Reverse (IREV)	Level	When true, with CTU ready and on line, causes tape to move in the reverse direction, and when false, causes tape to move in the forward direction.
P1	20	19	Rewind (IREW)	Pulse	With CTU ready, on line, and not at BOT, this pulse causes tape to rewind in reverse direction.
P1	22	21	Write Data Parity (IWP)	Level	-
P1	24	23	Write Data 7 (IW7)	Level	-

Table 1-2. Interface Input Connections

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P1	26	25	Write Data 3 (IW3)	Level	-
P1	28	27	Write Data 6 (IW6)	Level	-
P1	30	29	Write Data 2 (IW2)	Level	-
P1	32	31	Write Data 5 (IW5)	Level	-
P1	34	33	Write (IWRT)	Level	When true, specifies the write mode of operation, and when false, specifies the read mode of operation.
P1	38	37	Edit (IEDIT)	Level	When true, with IWRT true, causes the CTU to operate in the edit mode.
P1	40	39	Erase (IERASE)	Level	When true, with CTU on line, specifies the erase mode of operation.
P1	42	41	Write File Mark (IWFM)	Level	When true, and IWRT also true, causes a file mark to be written on the tape.
P1	46	45	Transport Address 0 (ITAD0)	Level	The CTU is selected by a combination of levels on the ITAD0, ITAD1, and IFAD lines and the position of switches S1, S2, and S4.

Table 1-2. Interface Input Connections (Continued)

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P2	18	17	Formatter Enable (IFEN)	Pulse	Enables the CTU. With CTU on line and IDBY true, pulse will reset a command "runaway" condition.
P2	24	23	Rewind/Unload (IRWU)	Pulse	When true, with CTU on line, causes the selected unit to go off line and rewind tape to the BOT marker. The CTU will unload the tape when BOT marker is detected.
P2	46	45	Transport Address I (ITADI)	level	The CTU is selected by a combination of levels on the ITAD0, ITAD1, and IFAD lines and the position of switches S1, S2, and S4.
P2	48	47	Formatter Address (IFAD)	Level	The CTU is selected by a combination of levels on the ITAD0, ITAD1, and IFAD lines and the position of switches S1, S2, and S4.

Table 1-2. Interface Input Connections (Continued)

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P1	2	1	Formatter Busy (IFBY)	Level	Goes true within one microsecond of trailing edge of IGO; goes false on completion of tape motion.
P1	48	47	Read Data 2 (IR2)	-	-
P1	50	49	Read Data 3 (IR3)	-	-
P2	1	-	Read Data Parity (IRP)	-	-
P2	2	-	Read Data 0 (IR0)	-	-
P2	3	-	Read Data (IR1)	-	-
P2	4	-	Load Point (ILDP)	Level	True when BOT marker is positioned in front of photosensor.
P2	6	5	Read Data 4 (IR4)	-	-
P2	8	7	Read Data 7 (IR7)	-	-
P2	10	9	Read Data 6 (IR6)	-	-

Table 1-3. Interface Output Connections

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P2	12	11	Hard Error (IHER)	Pulse or Level	When true, indicates that an uncorrectable read error has been detected by the CTU.
P2	14	13	File Mark (IFMK)	Pulse	When true indicates that the CTU has detected a file mark.
P2	16	15	Identification (IDENT)	Pulse	Pulsed when the BOT marker passes over the read head, to identify 1600 bpi (PE) tapes.
P2	20	19	Read Data 5 (IR5)	-	-
P2	22	21	End of Tape (IEOT)	Level	When true, indicates that the EOT marker has been detected. IEOT remains true until the EOT marker is sensed in the reverse direction.
P2	28	27	Ready (IRDY)	Level	True when load sequence is complete and CTU is on line and not rewinding. (CTU is ready to receive a remote command.)
P2	30	29	Rewinding (IRWD)	Level	True when CTU is in a rewind to beginning of tape sequence.

Table 1-3. Interface Output Connections (Continued)

PLUG NO.	LIVE PIN	GRD PIN	SIGNAL	TYPE	FUNCTION
P2	32	31	File Protect (IFPT)	Level	True when CTU is selected and a reel of tape without a write-enable ring is mounted on the CTU.
P2	34	33	Read Strobe (IRSTR)	Pulse	Pulses to indicate a read character is present on the controller interface.
P2	36	35	Write Strobe (IWSTR)	Pulse	When true (trailing edge), indicates that the character on the data lines has been written on tape and the next character is needed.
P2	38	37	Data Busy (IDBY)	Level	True after simulated ramp delay; remains true during active execution of all commands initiated by IGO.
P2	42	41	Corrected Error (ICER)	Pulse	When pulsed during a write/read operation, indicates that a single-track correctable error has occurred.
P2	44	43	On Line (IONL)	Level	When true, indicates that the selected CTU is accessible to the host controller.

Table 1-3. Interface Output Connections (Continued)

SECTION II

THEORY OF OPERATION

GENERAL

2-1. The basic concepts of digital recording, magnetic tape transport applications, and principles of operation of the Cachetape Unit (CTU) are presented in this section. A thorough knowledge of this section will be of considerable value in troubleshooting this equipment.

BASIC CONCEPTS OF DIGITAL RECORDING

2-2. The use of magnetic tape as a digital recording medium has increased steadily as a result of the increased use of microprocessor technology and the increasing versatility and decreasing cost of tape transports. The digital recording process involves methods and equipment capable of recording and reading information expressed in digital (binary) code.

DATA RECORDING/READING WITH MAGNETIC TAPE

2-3. The recording of data on magnetic tape originates with the input device, whose nine channels of digital signals are transmitted to the corresponding data channels of the transport in parallel bytes composed of 9 bits aligned across the width of the magnetic tape. A bit is a binary 1 or 0 which is presented in magnetic tape recording by the presence or absence of a flux reversal, or by a plus or minus direction of flux reversal, depending upon the coding system. (One of these channels is the parity channel, which is used to correct errors which occur when one of the other eight bits is not properly recorded.) These signals produce corresponding electrical currents in the write head of the transport, which, in turn, produces positive and negative magnetic polarities corresponding to the original data and parity signals in the tracks of the tape passing over it. In phase-encode writing, a binary 1 signal produces a transition to the erase polarity on the tape when moving tape in the forward direction (Figure 2-1); a binary 0 produces a transition away from the erase polarity.

2-4. As written tape passes across the magnetic read head of a transport, the head responds to each change of flux arriving at its gap and produces a read voltage waveform for each track as illustrated in Figure 2-1. (Refer to paragraph 2-5 for a detailed description of magnetic tape recording/reading in the phase-encode mode.)

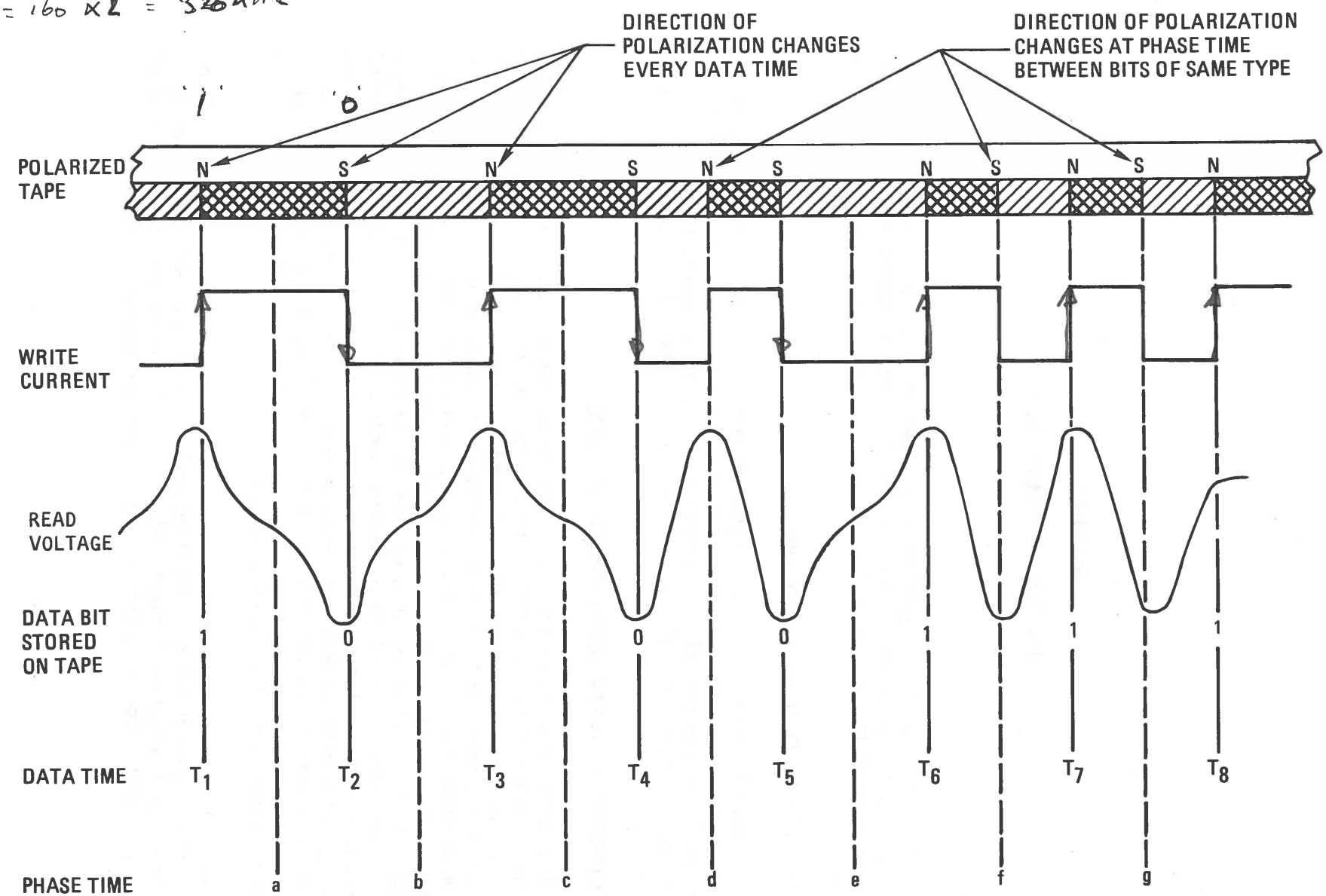

Figure 2-1. Phase-Encoded (PE) Tape Magnetization

2-5. **Phase-Encode System.** Phase-encoded (PE) recording is used for 1600 bits per inch (bpi) format in the nine-track mode only. A major advantage offered by the PE format is the fact that the data is self clocking which allows each channel to be synchronized using a preamble. This allows greater packing density.

a. There must be a change of tape polarity between data bits of the same polarity (consecutive 1 or 0 bits) at phase time.

b. There must be a change of tape polarity at each data bit time.

c. There must not be a change of tape polarity at phase time between 1 and 0 bits.

d. A change of tape polarity at data bit time, when reading forward, to erase polarity is a 1; away from erase polarity, a 0.

e. The PE transport records and reads data at a density of 1600 and 3200 bits per inch (bpi).

2-6. For clarification, the term "change of polarity" is also referred to as a flux change or flux reversal. As noted above, there must be a flux reversal with each data bit, whether it be a 0 or 1. Therefore, 1600 bpi equates to a minimum of 1600 flux reversals per inch (frpi) in any given channel. (This would occur in the case of alternate 0 and 1 bits.) The maximum case would occur with consecutive 0 or 1 bits, resulting in 3200 frpi. The flux reversal at each bit time accounts for the self-clocking feature of PE writing.

2-7. Details of the PE format are given in Figure 2-2. Channels 0 through 7 contain data bits, with the bit in channel 0 as the most significant bit. Channel P contains the parity bit, which in the PE format is always odd. No Cyclic Redundancy Characters (CRC) or Longitudinal Redundancy Characters (LRC) are used in the PE format. Each PE data block, however, is preceded by a preamble consisting of 40 bytes of all zeros followed by one byte of all ones. This is used to establish synchronization for the data block. The all ones byte identifies the end of the preamble and the start of the data bytes in the block. Following each PE data block is a postamble which is the mirror image of the preamble; i.e., one byte of all ones and 40 bytes of all zeros.

2-8. A 1600 BPI phase-encoded tape requires an identification burst (ID) of 1600 frpi in the P channel and erasure in all other channels at the beginning of the tape. The burst must begin at least 1.7 inches ahead of the trailing edge of the beginning of tape (BOT) marker and extend beyond the trailing edge of the marker and end at least 0.5 inch before the first block of data. The initial gap requirements are given in Figure 2-2. The typical distance for a gap is 3.75 inches. A similar ID burst is generated during 3200 bpi (optional) except that it is written on Channel 0.

2-9. The ANSI specification defines a PE file mark as a special control block consisting of 64 to 256 flux reversals (at 3200 frpi) in channels 2, 6, and 7. Channels 1, 3 and 4 are dc erased, but channels 0, P, and 5 in any combination, may be dc erased or recorded in the manner stated for channels 2, 6, and 7. The CTU writes an IBM compatible file mark with 80 flux reversals (40 characters) at 3200 frpi in channels P, 0, 2, 5, 6, and 7 with channels 1, 3, and 4 dc erased. The PE file mark is preceded by a gap of approximately 3.56 inches followed by a normal interblock gap (IBG) of 0.6 inch.

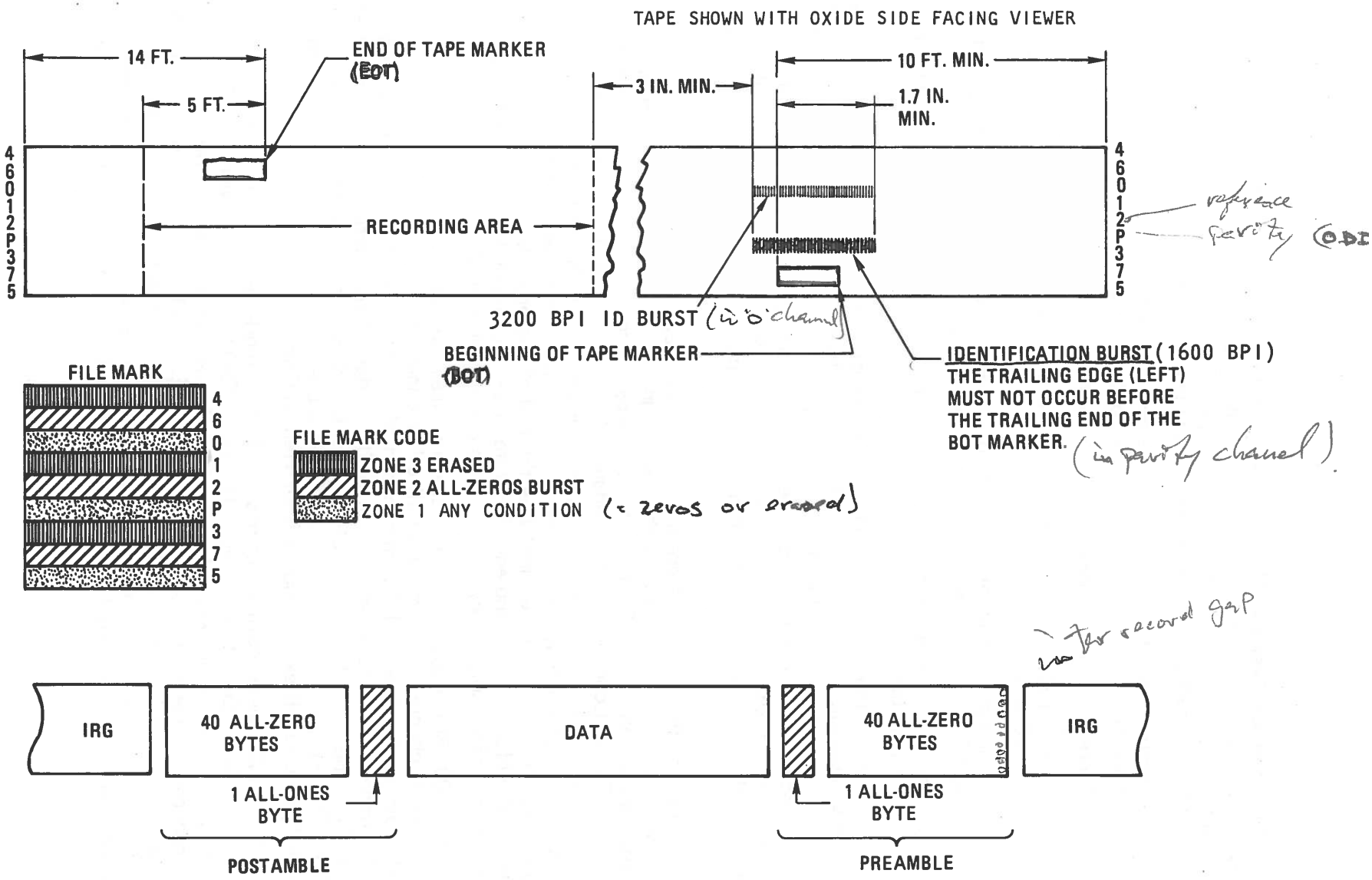

Figure 2-2. Nine-track PE Data Format

CACHE-TAPE OPERATION

2-10. Cache-tape operation consists of the CTU receiving data from the host computer, placing the data in cache memory, and then writing the data on tape when the physical write head is available. This permits faster write speeds, when viewed from the host system, in that write data as it is available, is transferred to the cache-tape unit and stored in cache memory. The CTU then writes the data on tape in a time frame independent of the host transfer rate. The cache memory allows the CTU to perform most of the housekeeping chores normally assigned to the host, freeing the host for other system activities. The cache memory thus acts as a logical drive in its interfacing with the host.

2-11. The cache memory can contain 150 records or 64K bytes of data. Exceeding either limit will cause the logical interface to wait until the physical drive fixes data to tape and reduces the cache memory data to the above limits.

2-12. The cache memory has storage limits that are reduced as the amount of tape remaining on the supply reel approaches end-of-tape (EOT). The system determines an impending EOT detection approximately ten feet in advance of the EOT marker and lowers the cache limits accordingly to assure that all data contained in cache will be written on the tape. The system operates in a streaming mode, as described in Paragraph 2-13, when the cache is full and no further write data can be accepted from the host.

STREAMING-TAPE OPERATION

2-13. Streaming-tape operation is simply writing data to tape without stopping and starting between each record block. Interblock gaps, as required in the ANSI format, are inserted automatically "on the fly". Figure 2-3 illustrates in the simplest form what a streaming drive will automatically perform if for any reason the unit must start and stop after each block. As can be seen in the diagram, there is a period of time called Command Reinstruct Time. This is the time after reading or writing the last character of the last block in which the system must instruct the tape drive to continue or, after reaching point B, the tape drive will enter what is called repositioning cycle. If the command to continue reading or writing is not received by the time normal forward velocity reaches point B, the drive automatically accelerates, coming to rest at point E. This sequence is called repositioning. After coming to rest at point E, the unit waits for the next command to read or write.

2-14. Because the tape acceleration and deceleration times required by the CTU are not related to tape velocity by the usual formula, it is not possible to start and stop the tape in the normal 0.6 inch interblock gap (IBG). It therefore becomes necessary, during certain command sequences, to reposition the tape so that it will be in the correct position with respect to the record head when record velocity is attained following a subsequent command. However, if the subsequent command is of the same category and is given within the reinstruct time, repositioning will not be required; tape motion will continue at the normal recording velocity.

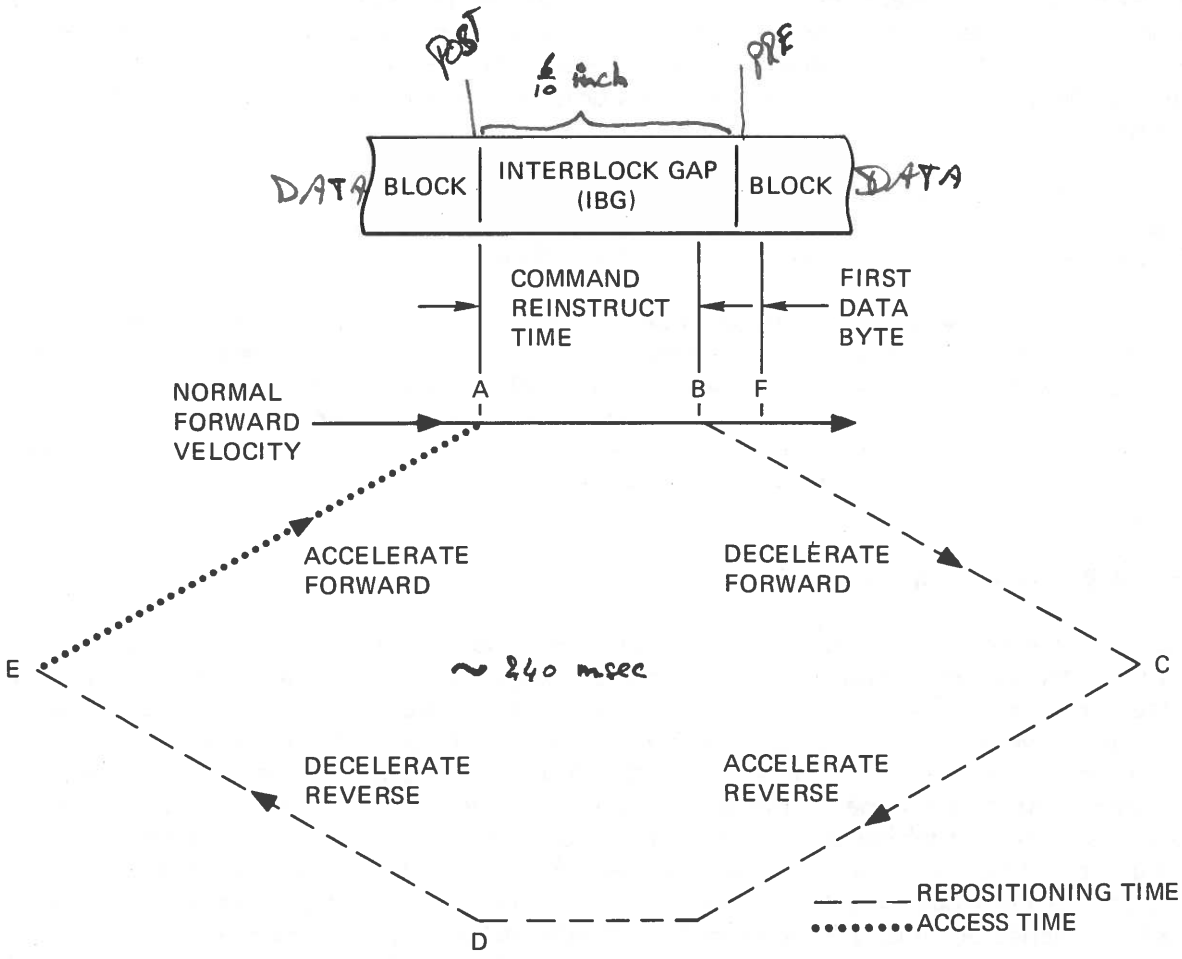

Figure 2-3. Repositioning Cycle

2-15. **Repositioning.** Repositioning is accomplished in three steps:

a. Deceleration of tape to a rest position (forward).

b. Acceleration of tape to a maximum velocity in the opposite direction (reverse).

c. Deceleration of tape to rest position (reverse).

Figure 2-4 illustrates these three steps and shows the relative positions of the record head with respect to the recorded data. The velocity achieved during acceleration is equal to the record velocity of the tape (100 ips). A write operation is used for the purpose of illustration; however, a read operation is identical, except that recorded data might be on either side of the record head. Figures 2-4A, B, and C show the position of the head and the last data block following acceleration or deceleration. Figure 2-4D is a composite showing the position of the record head at any instant in time during repositioning. Segments AB, BC, and CD represent the actual repositioning, and segment DA is the acceleration after another command is issued (access time).

2-16. To allow for minor variations in acceleration and deceleration rates, the tape is allowed to run at speed for short distances during repositioning. This provides an offset, which is shown as points C and C' in Figure 2-4D. After repositioning, the record head might be left several data blocks in front of the point at which the next write or read operation is to take place. If one microprocessor command is followed by another in the opposite direction, it becomes necessary to perform an additional repositioning to allow the required distance for tape acceleration, as illustrated in Figure 2-5. This illustration represents a reverse read following a write forward. It can be seen that the second repostion is a retrace of the first. It is shown offset in time for clarity only.

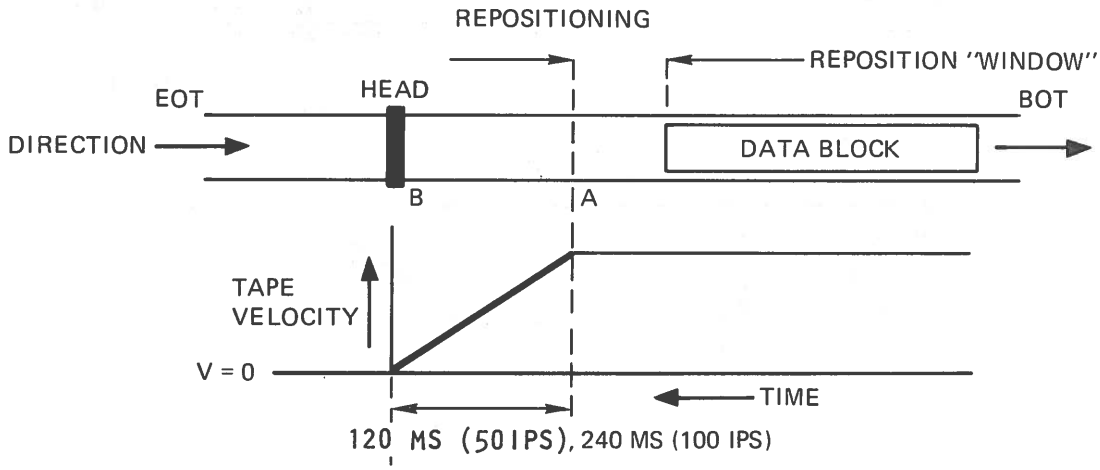

Figure 2-4A. Ramp Down (FWD)

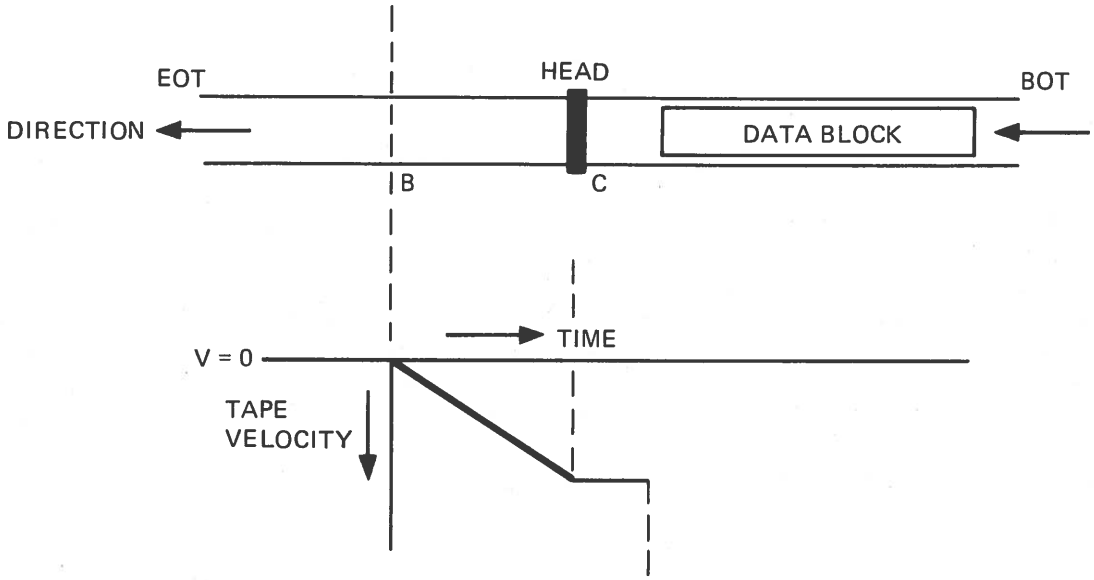

Figure 2-4B. Ramp Up (REV)

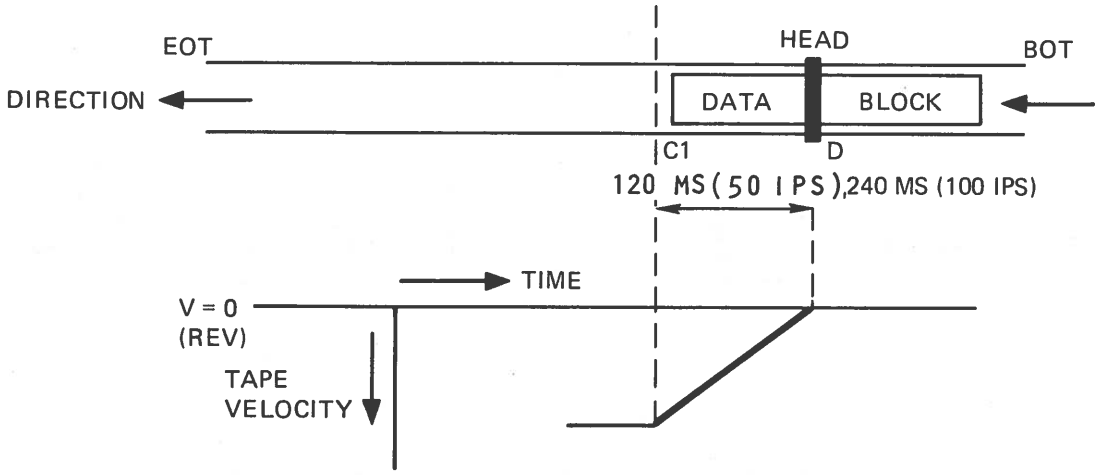

Figure 2-4C. Ramp Down (REV)

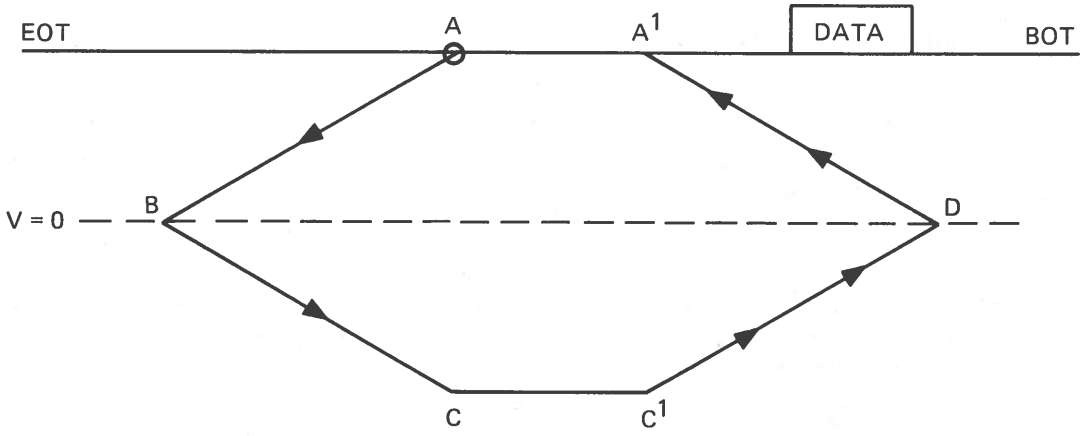

Figure 2-4D. Composite Ramps at 100 ips

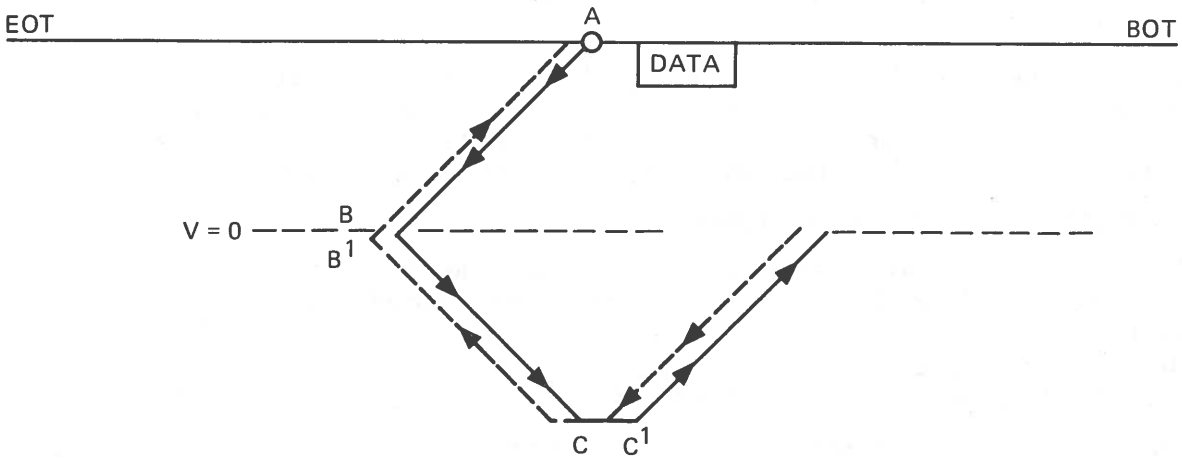

Figure 2-5. Reverse Direction Repositioning

MAJOR TRANSPORT COMPONENTS

2-17. The CTU is composed of three main assemblies: the drive assembly, which includes the tape drive components and the compliance arm system; the power supply system, which consists of a transformer and a power supply assembly mounted on the bottom of the top plate; and the formatter printed wiring board (PWB), which contains the voltage regulation circuitry, servo control logic circuitry, reel motor servos, sensor circuits, write and read circuits, and input/output (I/O) interface circuits.

2-18. **Power Supply/System Failure Detect Circuit.** The power supply assembly consists of an RFI line filter, ac line fuse, and rectifier circuits. The voltage regulators and system failure detect circuits are located on the formatter PWB. The system failure detect circuitry removes the drive voltage from the servo motors in the event of a power failure.

2-19. **Control Logic Circuitry.** A Z8002 microprocessor with associated I/O chips serves as the primary control element in the CTU. The program is stored in 16K of on-board programmable read-only memory (PROM) circuits.

2-20. **Takeup/Supply Servo Circuits.** Both takeup and supply servos incorporate current feedback lines which are used to control the speed and torque of the reel motors. The voltage mode of operation is simulated by the microprocessor.

2-21. **Sensor Input Circuits.** The CTU utilizes 3 optical sensors as inputs to the microprocessor to monitor tape position and speed, tape in path, write enable, and EOT/BOT. Door sense status is indicated by a microswitch.

2-22. **Write Circuitry.** The write circuitry converts the phase encoded data from the system to write current levels which are applied to the write head. A full width erase bar is also used to ensure thorough erasure of the tape prior to normal write operation. A protection circuit is used to eliminate erroneous operation of the write head when the transport is powered up initially.

2-23. **Read Circuitry.** The analog signals generated in the read head are amplified, detected, and converted to phase encoded digital inputs for the data formatting circuitry. The formatter multiplexes the digital inputs into a set of buffers which allows electronic deskewing of the read data before it is strobed to the interface.

DETAILED CIRCUIT DESCRIPTIONS

2-24. **Power Supply.** (Refer to Figure 2-6.) The ac input to the power supply is filtered by EMI filter FL1. The ac voltage is then routed through J5 to the POWER switch on the front panel and then through J9 to the primary of transformer T1. Solid state relay K1, located on the power supply PWB, is controlled by microprocessor output port Z2C2 which, when low, activates the blower motor B1.

2-25. The four secondary outputs of T1 are rectified by U1, U2, CR1, and CR2. The +30- and -30-volt power supplies are rectified by U2. A 50/60 Hz, 7Vac signal is output at J7 pin 14 for use in the +5Vdc noise injection circuitry. The +9-volt power supply is rectified by CR1 and CR2. Rectifier U1 produces the +20- and -20-volt power supplies.

2-26. **Voltage Regulators.** The voltage control and regulator circuits are located on the formatter PWB and shown in Figure 2-7. The V20P signal is routed to VR2 which produces the +15V signal at TP84. A +12V signal is input to Q16 which produces the +5R signal at TP63. Q16 provides a constant current source to the system failure detect and servo position sensor circuits to isolate these inputs from the +5VCC loading. The V20M signal is regulated by VR1 to provide -12Vdc at TP82 and -6Vdc at R314. Q7 regulates the V9P input to provide +5Vdc at TP81 for the -5VCC circuits.

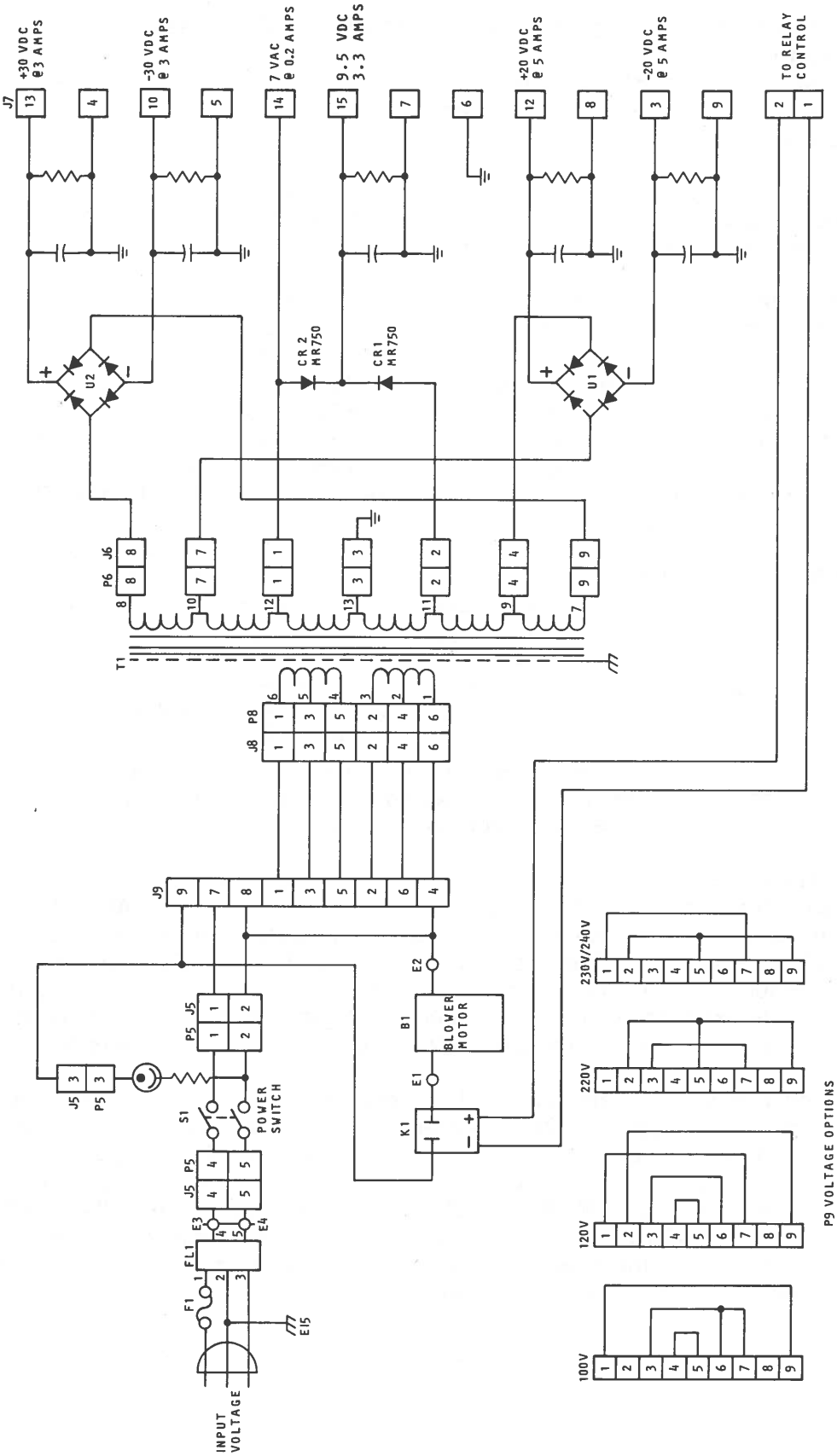

Figure 2-6. Power Supply Circuit

2-27. **Power Control and System Failure Detect Circuits.** (See Figure 2-8.) The +5R and +5Vdc voltages initiate the power-on sequence by charging C124 and C108 through R187 and R146. After an RC delay of greater than 1/2 but less than 1 second, the ouput of U3H-1 switches from low to high which clears the RES* line and enables the microprocessor.

2-28. The V20P signal is routed to the door lock and hub lock circuits and energizes the door lock solenoid when the CIO output Z2B3 is high. The hub lock solenoid is activated when the CIO output Z2B2 is high.

2-29. **Microprocessor Section.** (See Figure 2-9.) The microprocessor circuit controls the operation of the CTU. When power is applied to the unit, the crystal-controlled (Y1) oscillator circuit generates a 7.68-MHz clock signal. The 7.68-MHz clock signal is applied to a counter (U3K), which divides the signal by two to produce a 3.84-MHz clock signal at U3K-5. The counter also produces a divide-by-sixteen output (0.48 MHz) at U3K-12 that is used by the digital-to-analog converter logic. The 3.84-MHz clock signal is inverted at U2K-8 and U2K-10. The U2K-8 signal clocks the microprocessor (U2N), and the U2K-10 signal (CLK4) is used as a peripheral clock (PCLK) by the CIO's, and by the DMA controller logic and the cache memory addressing circuit.

2-30. When the 3.84-MHz microprocessor clock is initiated, the microprocessor begins executing instructions at address location 0 in memory. Typical instructions may be to jump to another location in memory, change a register, output a command, etc. The microprocessor obtains these instructions by way of multiplexed address/data lines AD$\emptyset$ through AD15. The AD$\emptyset$ through AD15 outputs from the microprocessor are also latched by U2L and U1L to produce latched address signals AL$\emptyset$ through AL15. The latched address signals address memory to obtain the instructions that are returned to the microprocessor on the AD$\emptyset$ through AD15 lines. An instruction is fetched from memory and strobed into the microprocessor by DS* when MREQ* and latched address AL15 are low and R/W from the microprocessor is high.

2-31. Address/data lines AD$\emptyset$ through AD15 route instructions and data to the microprocessor from the EPROM's and RAM's. Address/data lines AD6 through AD15 provide input data to the digital-to-analog converter (U6M), and address/data lines AD8 through AD15 interface with the cache memory bus. The functions of latched address lines AL$\emptyset$ through AL15 are detailed in Table 2-1. The WAIT* input to the microprocessor is sent from the DMA control logic during a communication cycle between the microprocessor and the DMA controller to synchronize the operation.

2-32. Read and write operations of bus data are initiated by the microprocessor. The state of the R/W* signal at U2N-25 determines whether a read or write operation is specified. An active (low) data strobe (DS*) signal from U2N-17 causes a low at U11P-3 to be applied gates U5K-2 and U5K-4. When R/W* is high, signalling a read operation, it is inverted at U2K-2 to assert RDIN* at U5K-8 when I/O* is active. When R/W* is low, signalling a write operation, WROUT* is asserted at U5K-11 when I/O* is active. RDIN* and WROUT* are used by the transport status register logic, the DMA control logic, and the DAC to specify read or write I/O functions.

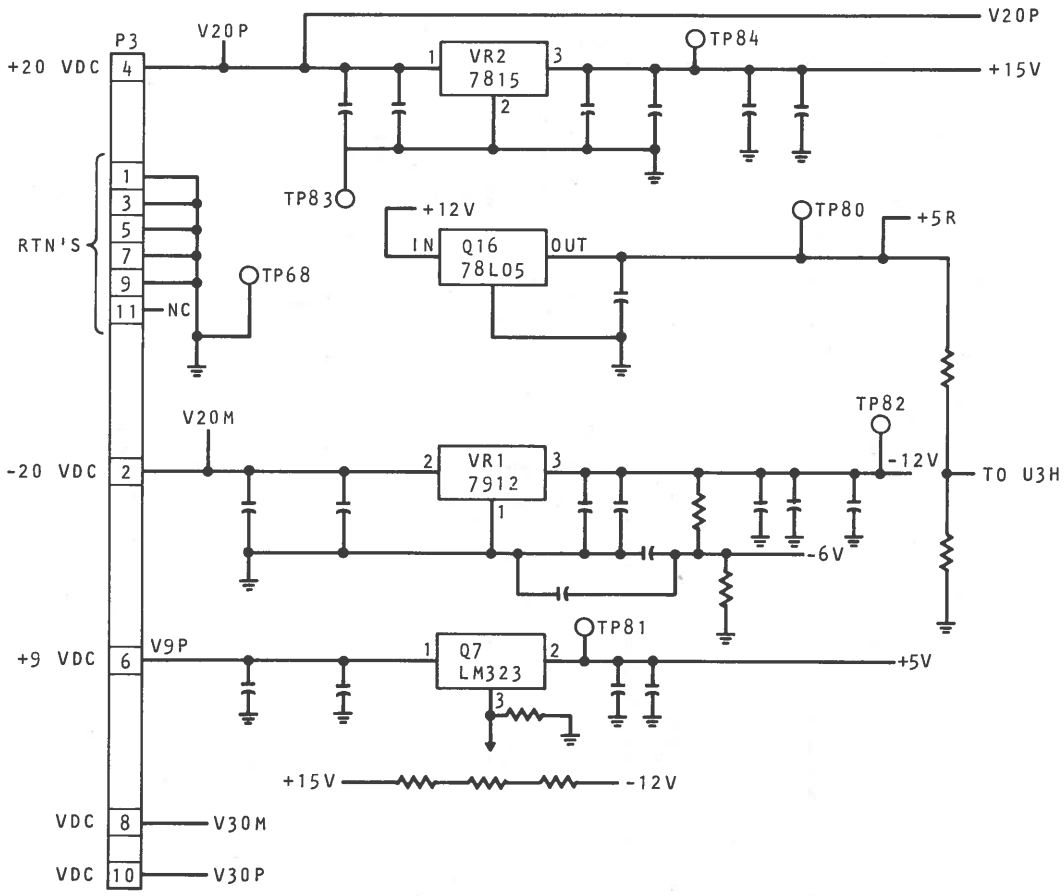

Figure 2-7. Voltage Regulator Circuits

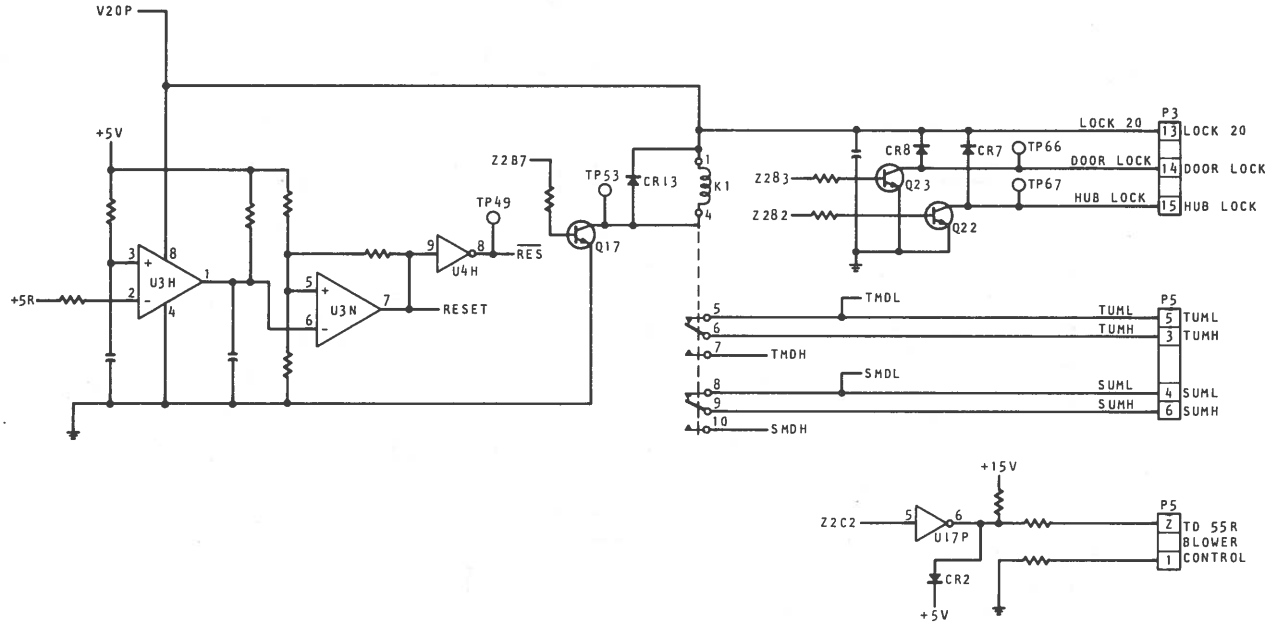

Figure 2-8. System Failure Detect Circuit

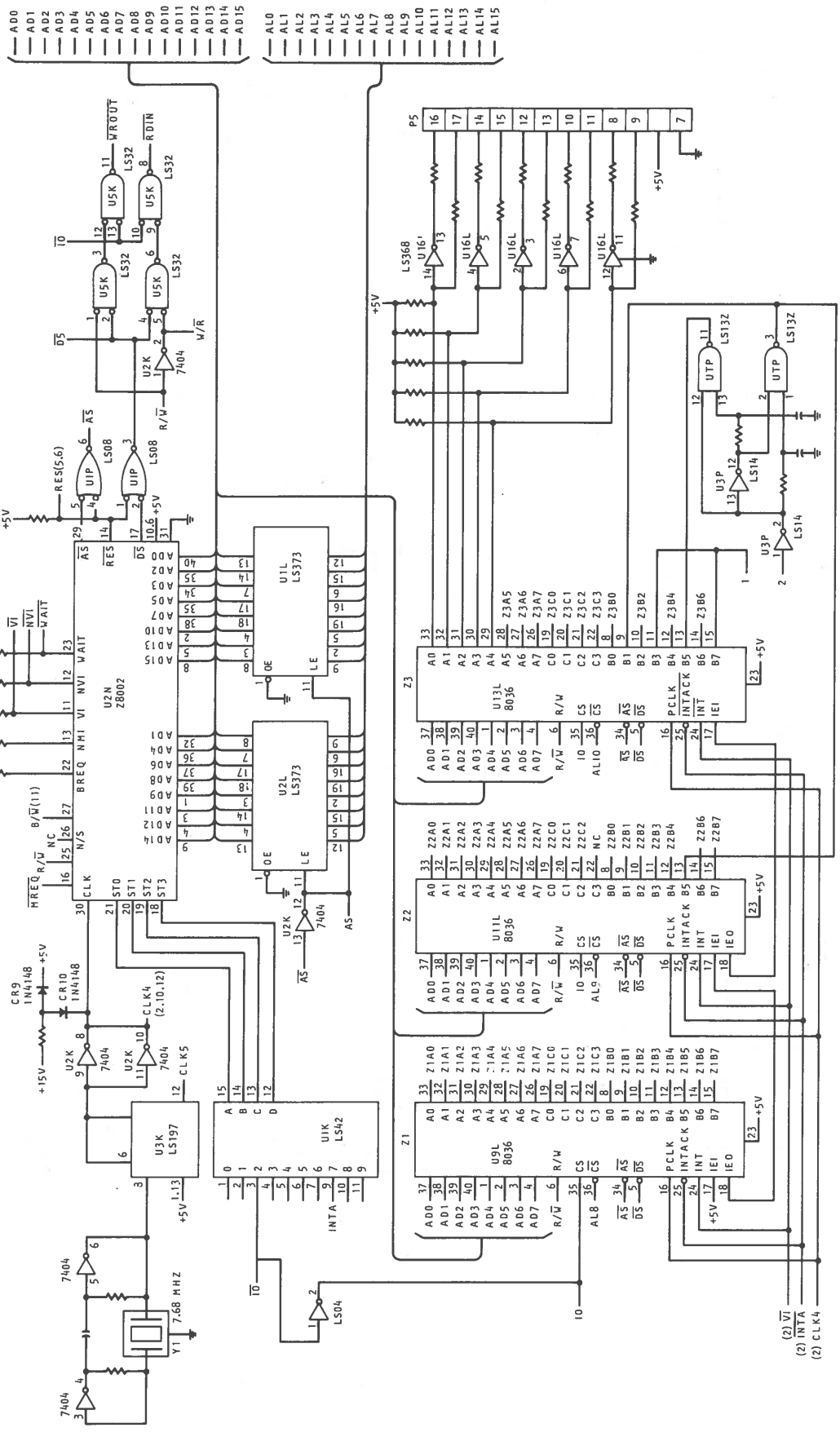

Figure 2-9. Microprocessor Section

LATCHED ADDRESS LINE(S)	FUNCTION(S)
AL1-AL11	RAM addressing
AL1-AL14	EPROM addressing
AL1-AL4	Inputs to address drivers AXØ-AX3 in DMA control logic
ALØ-AL2	Transport status register circuit addressing
AL8-AL10	Chip Select (CS*) inputs to CIO's Z1 (U9L), Z2 (U11L), and Z3 (U13L) in microprocessor section
ALØ	Control signal to RAM write control circuit
AL11	Enables DMA controller to assume control of DMA bus during an I/O operation
AL12	Transport status register circuit enabling signal
AL14	Chip Select (CS) input to analog-to-digital converter (U6N)
AL15	(1) Gated with Read Data In (RDIN*) from microprocessor section to produce Read Command (RDCMD*), which enables transport status register drivers and enables outputs of input tape motion command latch (U2W) (2) Chip Select (CS) input to digital-to-analog converter (U6M) (3) Chip Select (CS*) input to EPROM's and RAM's

Table 2-1. Latched Addresses ALØ-AL15 Functions

2-33. The microprocessor section utilizes counter/timer and parallel I/O units (CIO's) (U9L, U11L, and U13L) to provide both timing and I/O communications for internal CTU circuits. The programmable CIO's each contain three I/O ports and three counter/timers. The CIO's are clocked by peripheral clock signal CLK4 and are sequentially selected by latched addresses AL8, AL9, and AL10. The microprocessor addresses the CIO's on the address/data bus (AD0-AD7). Bi-directional communications with system circuits is provided on the A0-A7, B0-B7, and C0-C3 output lines from each CIO. The inputs from system circuits are returned to the microprocessor on the AD0-AD7 address/data bus.

2-34. **DMA Control Logic.** (See Figure 2-10.) The DMA control logic consists of DMA controller U2T and associated logic circuit. The DMA control logic controls the operation of the cache memory in response to service requests from the microprocessor requests on a priority basis, as follows:

Priority	Request/Function
1	DREQ Ø - I/O, cache to physical tape
2	DREQ 1 - I/O, interface to cache
3	DREQ 2 - Z8002/Cache communications via DMA
4	DREQ 3 - Refresh cache

When the DMA control logic is busy performing a function in response to a microprocessor request, and one or more additional requests are received, the DMA controller completes its present cycle and then selects the highest priority request pending.

NOTE

DREQ 3, the refresh cache request, is always set when a refresh is not taking place. As other requests are received, the controller processes them in the order of their priorities. However, after every three cycles of servicing higher priority requests, the controller will service DREQ 3. The longest period between refreshes is 8.4 microseconds. Refreshing is disabled during active channel 0 and 1 operations. When no other requests are pending, cache is continuously being refreshed.

2-35. The service requests from the microprocessor are latched by D-type flip-flops. The respective Data Request signals are sent to the DMA controller (U2T), which sets Hold Request (HLDR) to request control of the cache from the microprocessor. When the microprocessor acknowledges the request, Hold Acknowledge (HLDA) is received by the DMA controller, which then issues a Data Acknowledge (DACK) signal to reset the DREQ line. The microprocessor signals, request/acknowledge signals, and the devices for each of the DREQ signals are as follows:

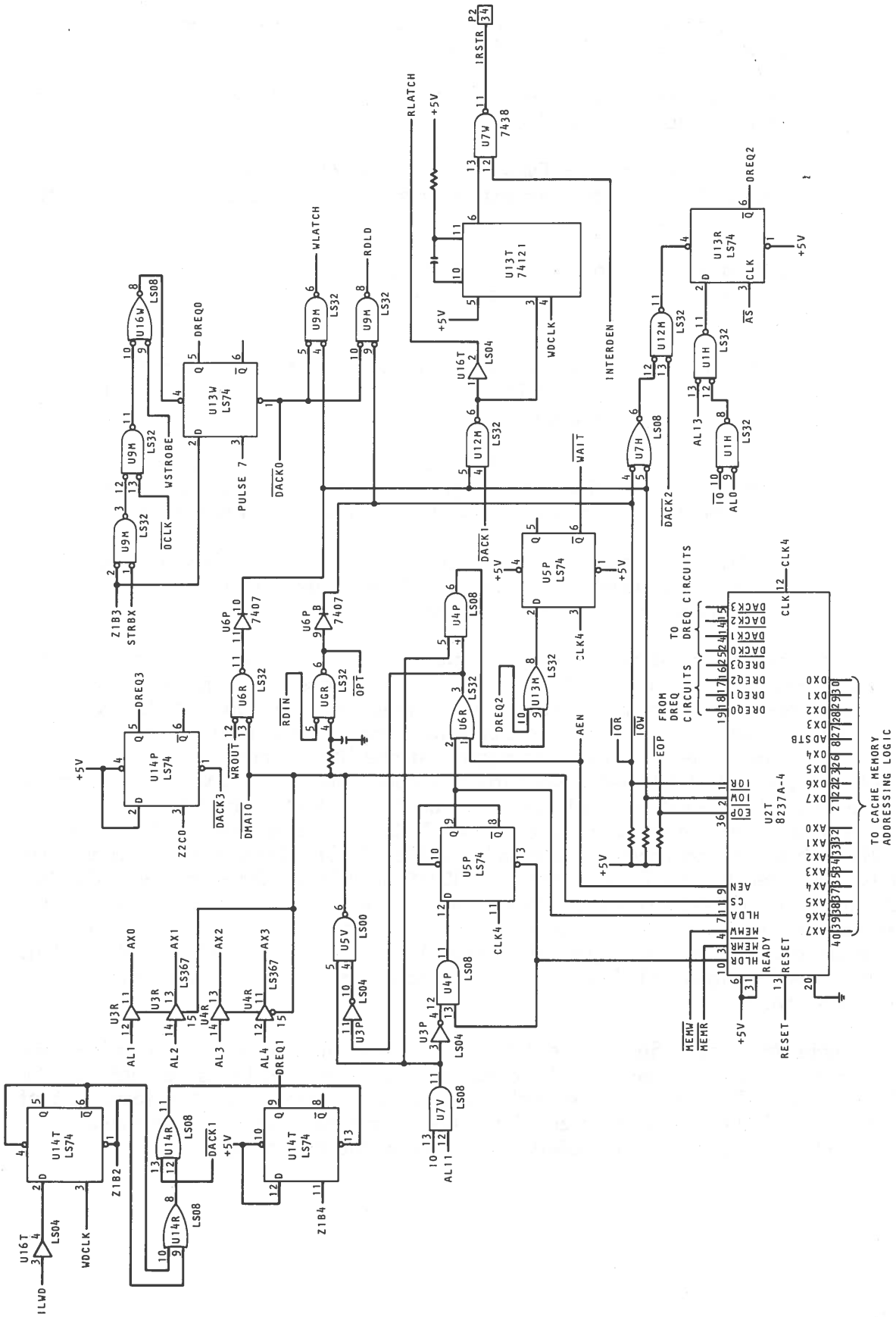

Figure 2-10. DMA Control Logic

2-36. A typical example of the data request sequence and the response of the DMA control logic when servicing a DREQ 1 is as follows:

a. U14T is set by Z1B4 (Formatter Interface Clock) from the processor C10, asserting DREQ 1 at U14T-9.

b. DREQ 1 is sent to the DMA controller (U2T-18), which generates Hold Request (HLDR) to request control of the cache bus from the microprocessor.

c. HLDR is sent to flip-flop U5P-13 and gate U4P-13. This removes the low reset signal at U5P-13 and conditions AND gate U4P-11 for the signal from inverter U3P-4.

d. The IO signal from the microprocessor is high at U7V-13 and AL11 is low at U7V-12. The resulting low at U7V-11 is inverted by U3P-4, sending a high to U4P-12 to enable the AND gate.

e. The high at U4P-11 sets U5P on the next CLK4 pulse from the microprocessor section clock logic, resulting in a high at U5P-9 that is sent to the Hold Acknowledge (HLDA) input of the DMA controller.

f. The DMA controller assumes control of the cache bus and generates DACK1* to acknowledge receipt of HLDA. DACK1* resets U14T via OR gate U14R and returns DREQ 1 to low.

2-37. The DREQ2 circuit provides communication between the microprocessor and the cache bus when a cache I/O read or write is not in progress or requested. With IO* and latched address AL0 from the microprocessor logic low, the signal at U1H-8 is low. When latched address AL13 is low, the input to latch U13R-2 from U1H-11 is high, causing the latch to be reset on the next address strobe (AS*) from the microprocessor. The high DREQ2 signal at U13R-6 is sent to DMA controller U2T-17, which responds by sending the DACK2* request acknowledgement signal. DACK2* enables bus transceivers U7T (shown in the parity generator logic, Figure 2-10E), which interfaces the cache bus (RD0-RD7) with the microprocessor address bus (AD8-AD15). When an I/O read or write request is generated by the DMA controller (IOR* or IOW*, U7H-6 is low. The low DACK2* signal at U12M-13 sends U12M-11 low, setting U13R and causing the DREQ2 signal to go low, disabling the microprocessor/cache communication mode. During the DREQ2 sequence, the DREQ2 signal at U13M-10 sends a high to latch U5P-2. This asserts the WAIT* signal at U5P-6, which synchronizes the microprocessor/cache communication cycle.

2-38. **Cache Memory.** (See Figure 2-11.) The cache memory consists of nine 4864 dynamic random access memories. The devices store up to 64K bytes per each of the nine channels (0-7, P); however, the cache size actually used is not the total size of cache memory. Rather, it is the size of the cache memory minus the selected block size. The cache is addressed by the DMA via the cache addressing logic.

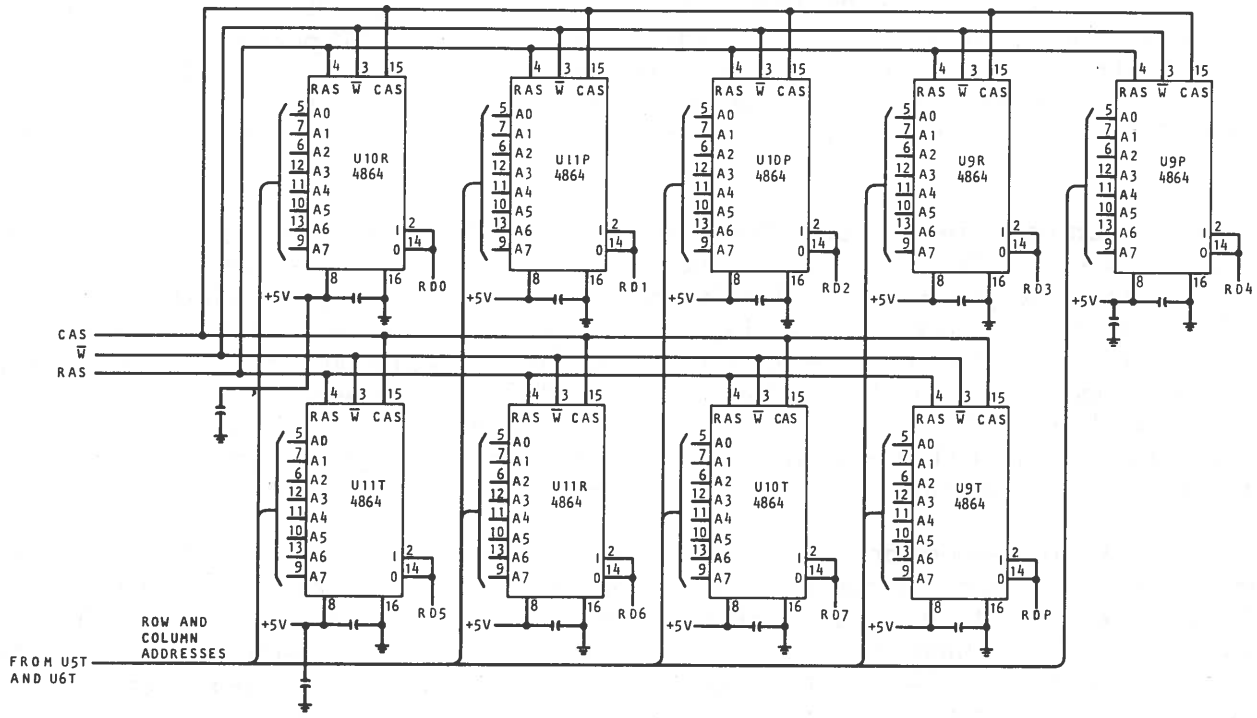

Figure 2-11. Cache Memory

2-39. **Cache Memory Addressing Logic.** (See Figure 2-12.) The cache memory is addressed by the DMA control logic on the DX0-DX7 and AX0-AX7 lines. Row addresses are latched by U6T and column addresses are latched by U5T. The outputs of the respective latches are enabled by the MEMR* or MEMW* signal from the DMA controller. When either signal is active, the output U5V-11 is inverted by U5R-10, and then enables the row addresses from U6T. The signal is then delayed by U5R-12 and then enables the column addresses from U5T. The MEMW* signal, when active, enables the cache memory for a write operation. The outputs of U5R-2, U5R-4, and U5R-6 delay the generation of the CAS signal to provide proper timing of the CAS and RAS strobes. The RAS is generated by latch U13W-8 when ADSTB from the DMA controller is active.

2-40. **Cache Read Circuit.** (See Figure 2-13.) Corrected read data (CDATAX) is received at U14W-1,2 from the read circuits in serial form. Serial-to-parallel converter U14W, clocked by the PECLK, converts the serial data to an 8-bit parallel character that is latched by U15W and then routed to cache memory on the cache bus (RD0-RD7). Data from the cache memory bus is read to the host interface via latches U15V and U14V. The RLATCH signal from the DMA control logic clocks the data through the latches during a logical tape operation.

2-41. **Cache Write Circuit.** (See Figure 2-14.) The cache receives data from the host interface on the IW0-IW7, IWP lines. The write data is latched into U11W by the write data clock generated by U12M-8. When a logical I/O operation is initiated by the microprocessor, the DMA control logic sends IOR* low and toggles DACK1* for each character to be written into the cache memory. The 8 bits of input write data are routed to cache memory from U11W via the cache bus (RD0-RD7). The parity bit, RDP, is sent to U16N-13, where it is XORed with the SODD signal from the parity generator circuit. The output of U16N-11 is applied to U17R-12. When a parity error exists, U17R is set by the write clock, asserting Z1A6 to inform the microprocessor of the error.

2-42. **Parity Generator.** (See Figure 2-15.) The parity generator (U11V) receives the RD0-RD7 inputs from the cache bus and determines whether the summation of the eight lines is even or odd. If the summation is even, the SODD signal is low and the EEVEN output at U11V-5 is high. The EEVEN signal sets U13R-9 during a memory read (MEMR*) function, asserting Z1A4 to notify the microprocessor of the memory parity error. The SODD signal is sent to the cache write logic to signal the parity status for purposes of parity error detection.

2-43. The U17T bus transceivers provide the microprocessor access to the cache bus. The RD0-RD7 lines are interfaced to address/data lines AD8-AD15. The transceivers are enabled by an active DACK2* signal from the DMA controller. The direction of data flow is determined by the state of the W/R* signal from the microprocessor.

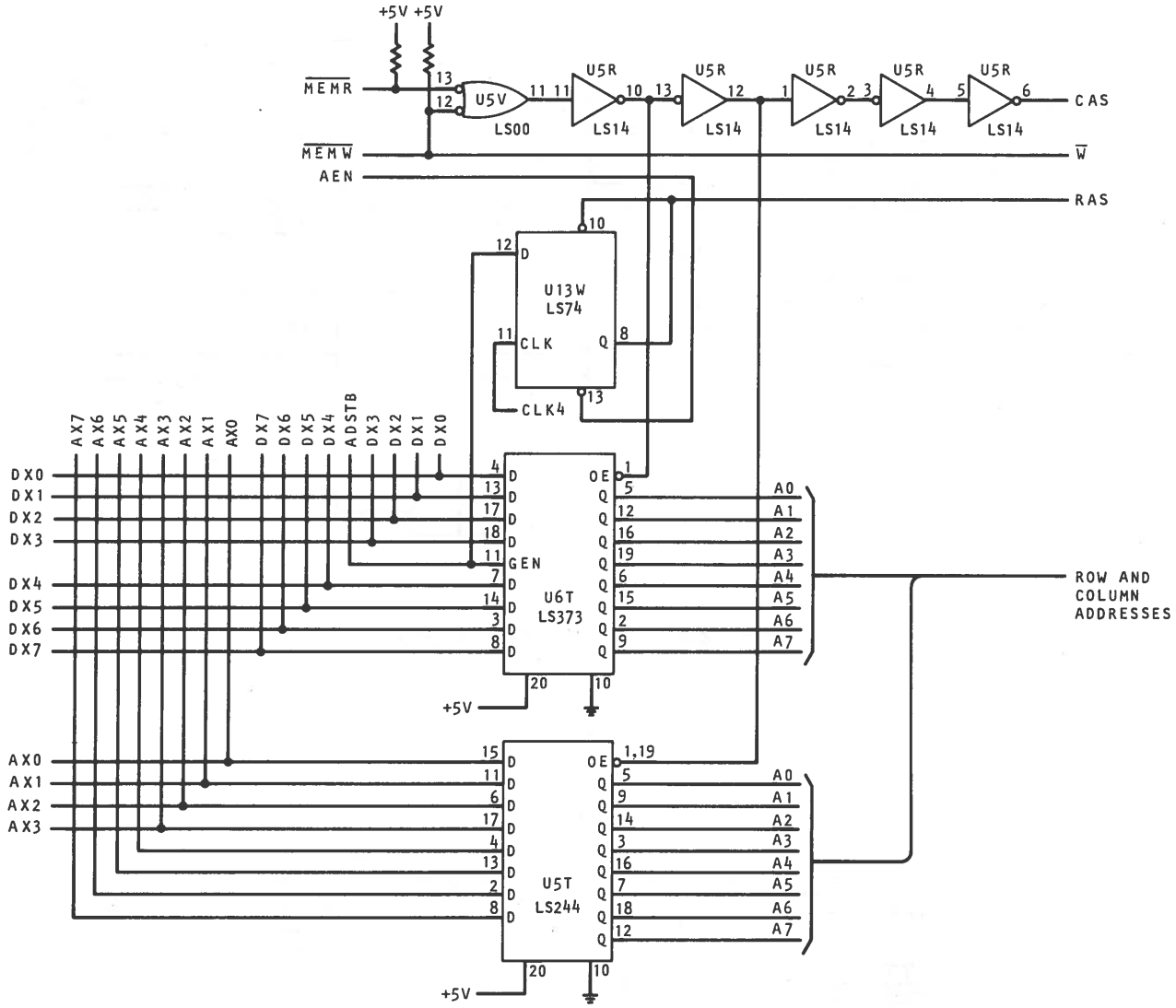

Figure 2-12. Cache Memory Addressing Logic

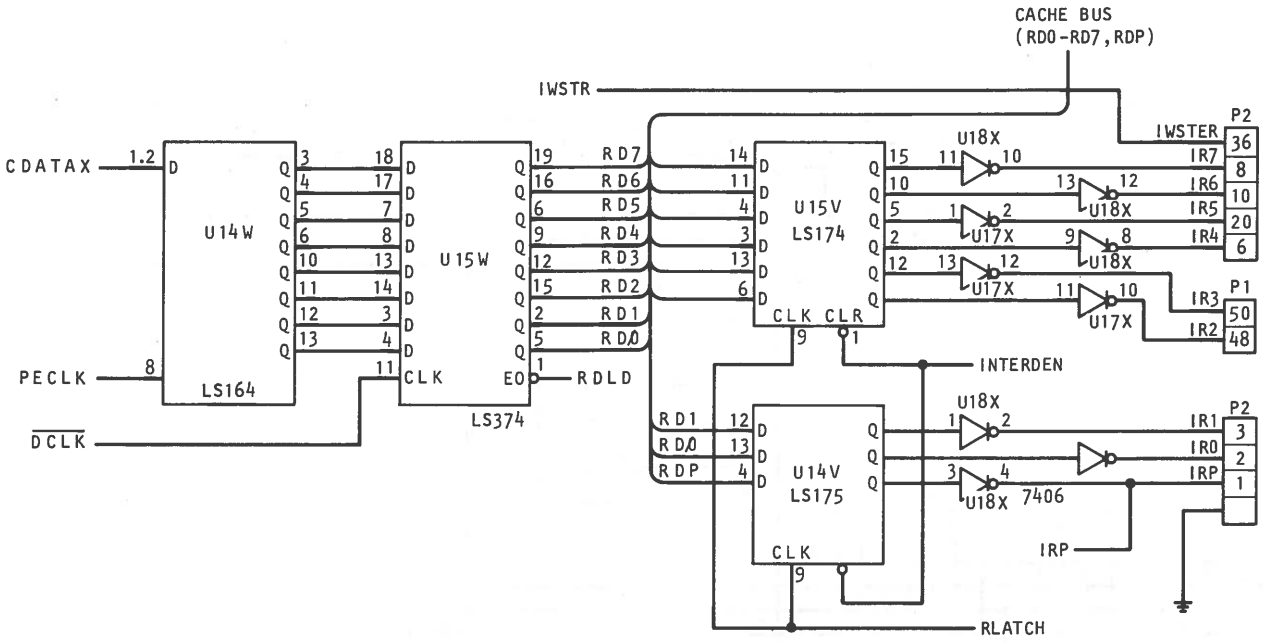

Figure 2-13. Cache Read Circuit

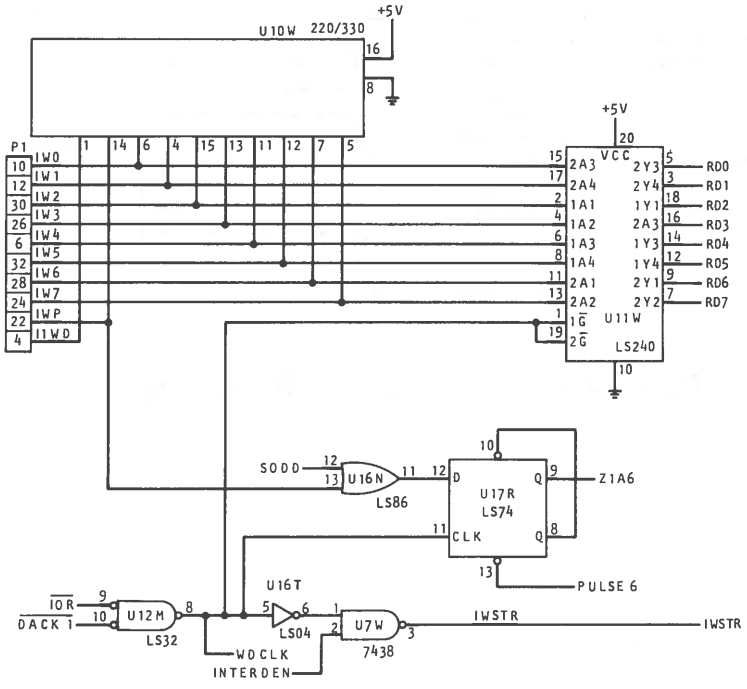

Figure 2-14. Cache Write Circuit

2-44. **EPROM and RAM Circuits.** (See Figure 2-16.) The EPROM's (U5L and U3L) provide 16K words of control storage, and the RAM's (U3N and U5N) provide 2K words of variable storage. The EPROM's and RAM's are enabled and addressed by the microprocessor. Latched address AL15, when low, selects the devices, and the ORed data strobe (DS*) and memory request (MREQ*) signals enable the devices via U6R-8. The EPROM's, when selected and enabled, are addressed by latched addresses AL1-AL14 from the microprocessor circuit, and returns the selected data to the microprocessor on address lines AD0-AD515. Write/read signals (W/R*, R/W*, and B/W*) and latched address AL0 from the microprocessor circuit are decoded in the RAM logic to specify a write or read operation at the WR* inputs of the RAM devices. The RAM's are addressed by latched addresses AL1-AL11 from the microprocessor circuit. When enabled and selected, the addressed RAM data is sent to the microprocessor on address lines AD0-AD15.

2-45. **Transport Status Registers.** (See Figure 2-17.) Latched address lines AL$\emptyset$, AL1, and AL2 are the address inputs that select the output of decoder/multiplexer U6W, the AL$\emptyset$ input is the least significant and the AL2 input is the most significant. U6W is enabled by the low true input WROUT* and the high true latched address line AL12 from the microprocessor section. A binary input on the AL$\emptyset$-AL2 lines enables the selected output of U6W to go low when the A7 line is asserted. The PULSE $\emptyset$ output at U6W-15 provides a clock input to output status register U6V. The low to high transition of the PULSE $\emptyset$ line causes U6V to output the status conditions that are on address/data lines AD$\emptyset$ through AD5. The PULSE 1 output at U6W-14 sets on-line (ONL) latch U8V-6. The PULSE 1 line corresponds to the ON-LINE front panel switch. The status of ONL is sent to the microprocessor on address/data line AD8 via driver U13P-11. The PULSE 2 output at U6W-13 resets the rewind (RWD) latch (U8V-11), sending the IRWD status output false. The rewind latch is set by the IREW input, which is gated with FSEL in the motion control circuit, or the PULSE 3 line, which corresponds to the front panel REWIND switch when offline. The status of RWD is sent to the microprocessor on address/data line AD9 via driver U13P-6. When the rewind operation is completed, the PULSE 2 line resets U8V-11. If the tape reel is positioned at BOT (ILDP true), the output from U3V-8 inhibits the IREW or PULSE 3 input. The PULSE 4 line or the IRWU input via U2V-10 and U3V-8 resets the on-line latch. The PULSE 5 line is not used.

The PULSE 6 line resets IGO detect flip-flop U14P. The flip-flop is set by GO from the input tape motion commands logic. The high output at U14P-9 is sent to the microprocessor logic on the ZIA1 line and is also ORed with the OUTLATCH $\emptyset$ line from output status register U6V-10. Either the higher U14P-9 output or a high OUTLATCH $\emptyset$ signal generates the formatter busy (FBY) signal. PULSE 6 is also used in the write data circuit to reset the parity error flip-flop after a parity error has been detected. PULSE 7 is the dynamic RAM enable signal and is used in the DMA control logic to clock the DREQ $\emptyset$ flip-flop, which requests a write operation to the physical tape. The status of the formatter select (FSEL) signal is sent to the microprocessor on address/data line AD1$\emptyset$ via driver U13P-8.

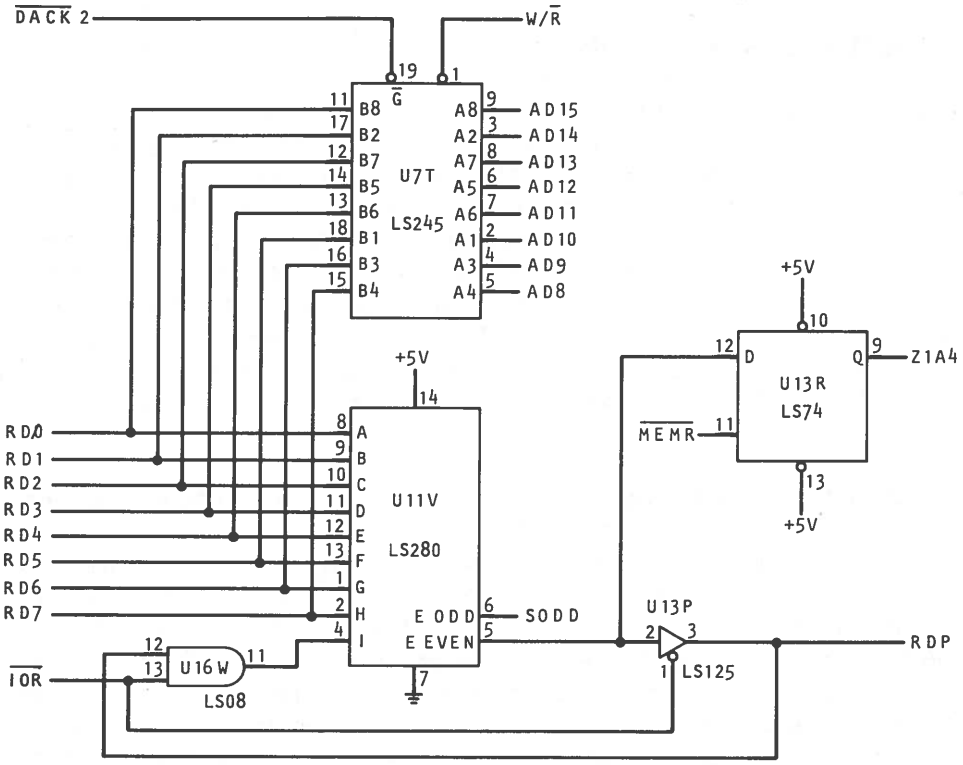

Figure 2-15. Parity Generator

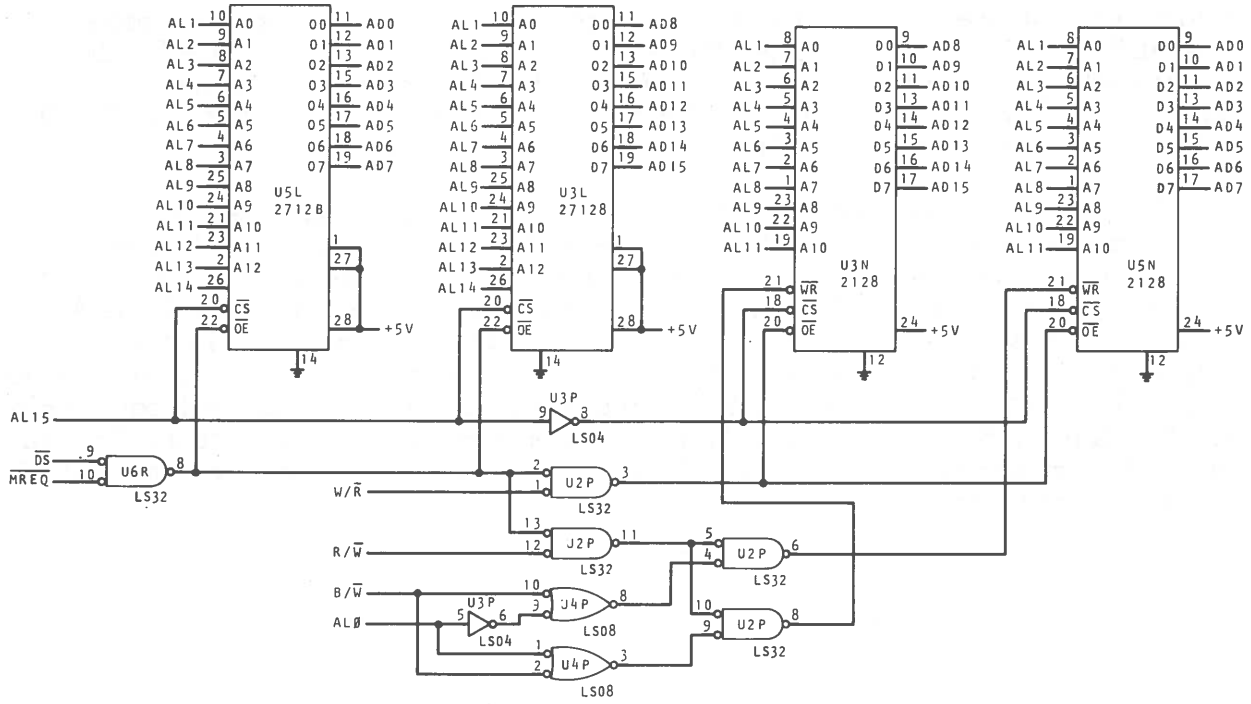

Figure 2-16. EPROM and RAM Circuits

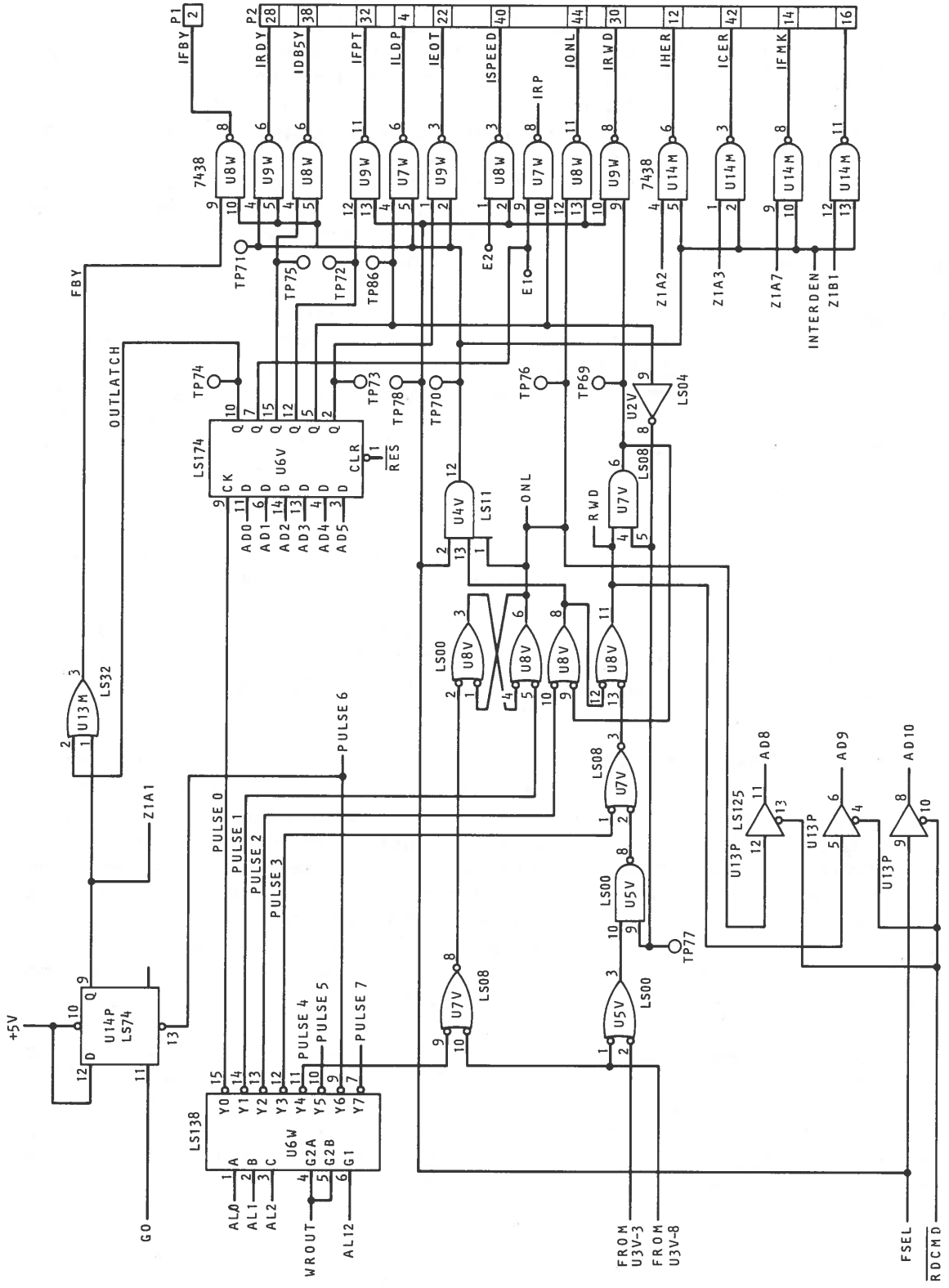

Figure 2-17. Transport Status Register Circuits

2-46. **Motion Commands Circuit.** (See Figure 2-18.) The input motion commands reverse (IREV), write (IWRT), write file mark (IWFM), edit (IEDIT), erase (IERASE), and high speed (IHSP) are latched by U2W and then routed to the microprocessor on address/data lines ADØ through AD5. The U2W inputs for the AD6 and AD7 lines are reserved. The U2W latch is clocked by GO from U3V-11. The outputs of U2W are enabled by the low true RDCMD* signal from the transport status register circuits. GO is generated by the input IGO signal, which is inverted and then gated with FSEL at U3V-11. The GO signal also is used by the transport status registers circuits to set the IGO detect flip-flop, the output of which is sent to the microprocessor logic on the Z1A1 line to indicate that IGO has been detected. Switch U5W is used to set the unit address. The U5W outputs are applied to exclusive -OR gates U4W-2, U4W-10, and U4W-12. The other inputs to the exclusive -OR gates are ITADØ, ITAD1, and IFAD. The combination of U5W outputs and the levels on the IFAD, ITADØ, and ITAD1 lines select the unit by producing high outputs at U4W-3, U4W-8, and U4W-11. These highs are applied to AND gate U4V-8, generating a high formatter select (FSEL) signal. The input formatter enable (IFEN) signal is gated with FSEL at AND gate U3V-6, and the resulting level is sent to the microprocessor logic on the Z1AØ line. The input rewind (IREW) signal is inverted by U2V-2 and gated with FSEL at U3V-3. The resulting level is sent to the rewind latch in the transport status register circuits. The input rewind unload (IRWU) signal is inserted by U2V-10 and gated with FSEL at U3V-8. The resulting level is sent to the transport status register circuits to set the rewind latch and reset the on-line latch.

2-47. **Input Sensors.** (See Figure 2-19.) The CTU contains four optical sensors that are used to detect EOT/BOT, File Protect/Reel Seat, Tape-in-Path, and Tape Position. Each sensor includes an infrared LED transmitter and a phototransistor receiver.

2-48. **EOT/BOT Sensors.** The reflective strips for the EOT and BOT sensors are placed at the end and beginning, respectively, of the magnetic tape reel. The VINØ signal is the EOT sensor input to the analog-to-digital converter circuit. The VIN1 signal is the BOT sensor input to the analog-to-digital converter circuit.

2-49. **File Protect/Reel Seat Sensor.** The reflective tabs for both the file protect and reel seat functions are attached to the supply reel hub. These tabs reflect the infrared light beam from the LED source to the phototransistor receiver, which are both encased in a single device and mounted to the top plate adjacent to the supply reel motor. When the reel of tape is properly seated on the supply reel hub, the inside flange of the tape reel depresses the reel seat tab, which has a piece of non-reflective black tape in its center. As the tab moves past the sensor, the reflected light beam produces two pulses that are sent to the microprocessor on the Z3B6 line. When a supply reel with a file protect ring is placed on the supply hub, the second reflective tab is depressed and an additional pulse is produced as the tab moves past the sensor.

2-50. **Tape-In-Path Sensor.** The tape-in-path sensor is located at the entrance of the tape path between the supply reel and the compliance arm. It consists of an LED transmitter and a phototransister, located on opposite sides of the tape path. As the tape moves through the tape path during the load sequence, the light beam is obstructed by the tape, informing the microprocessor of the tape presence on the Z2B6 line. The microprocessor can thus determine the status of the load operation.

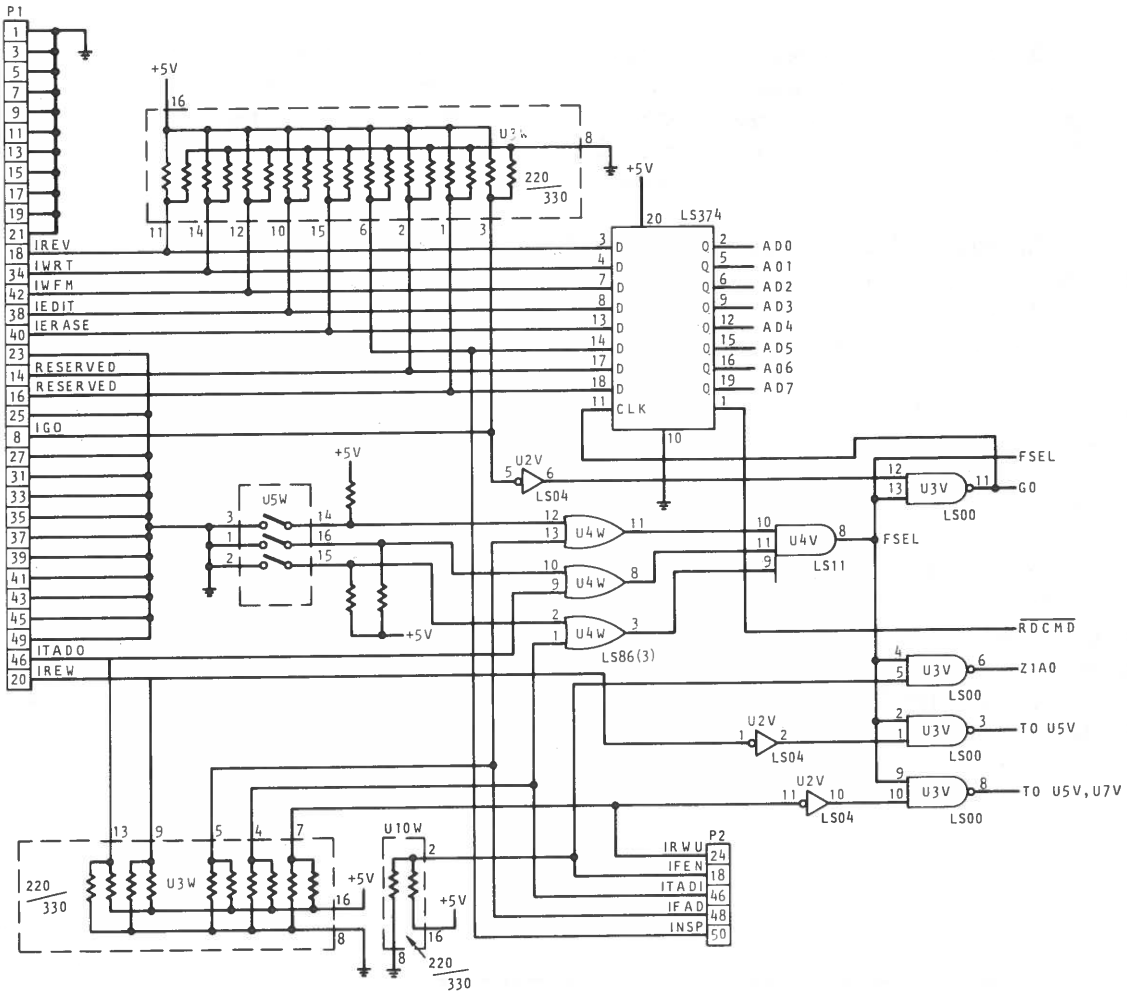

Figure 2-18. Motion Commands Circuit

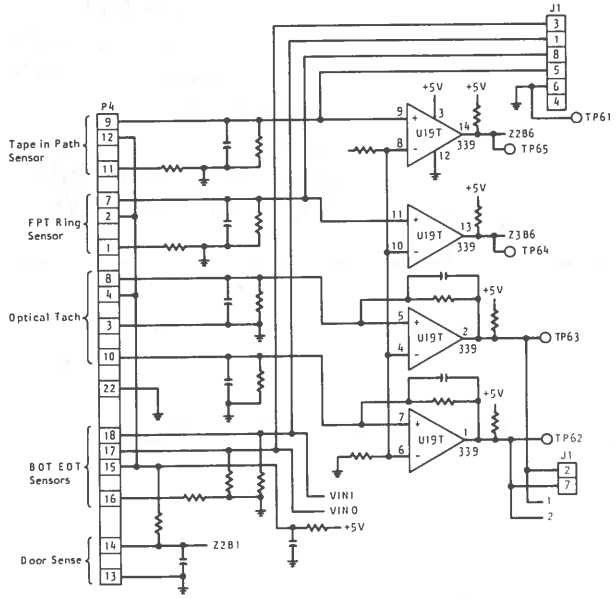

Figure 2-19. Input Sensors

2-51. **Optical Tachometer.** The optical tachometer sensor consists of two LED transmitters and receivers separated by an optical disk that is etched with about 400 lines. As the opaque lines move between the transmitters and receivers, two square wave outputs (Ø1 and Ø2) are produced. These outputs are used by the microprocessor logic to determine tape speed, direction of travel, and position.

2-52. **Digital-to-Analog Converter (DAC).** (See Figure 2-20.) The DAC (U16M) is a multiplying digital-to-analog converter that interfaces directly with the microprocessor via address/data lines AD6-AD15. The DAC reads the ten address/data lines twice to acquire a 12-bit data input under the control of AL15 from the microprocessor, which strobes the DAC every 2 milliseconds. The DAC output is buffered by U6L-7 and amplified by U6L-1 and is then applied to multiplexer U7J. The outputs of the multiplexer are selected by Z3C0, Z3C1, and Z3C3 from the microprocessor. The multiplexer outputs consist of the supply reel servo current (ISU), takeup reel servo current (ITU), and read threshold (ITHR).

2-53. **Analog-to-Digital Converter.** (See Figure 2-21.) The analog-to-digital converter consists of multiplexer U7N, A/D converter U6N, and associated logic. The multiplexer receives VIN0-VIN4, VIN6, and VIN7, which represent the analog data shown in Table 2-2. The multiplexer outputs are selected by Z3C0, Z3C1, and Z3C2 from the microprocessor. The A/D converter converts the analog values to digital data and routes the digital data to the microprocessor via address lines AD8-AD15.

INPUT SIGNAL	FUNCTION
VIN0	End-of-Tape (EOT)
VIN1	Beginning-of-Tape (BOT)
VIN2	Compliance Arm Position
VIN3	Supply EMF
VIN4	Takeup EMF
VIN6	Compliance Arm Rate
VIN7	DAC Servo Offset Voltage

Table 2-2. Analog-to-Digital Converter MUX Inputs

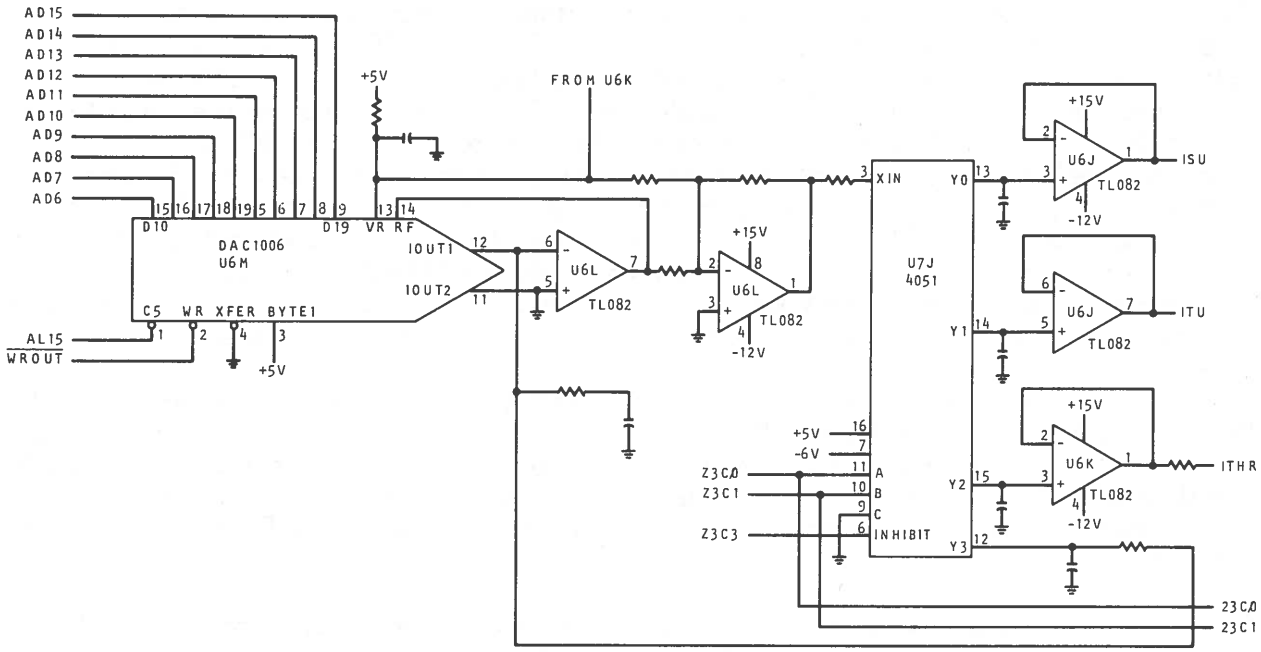

Figure 2-20. Digital-to-Analog Converter

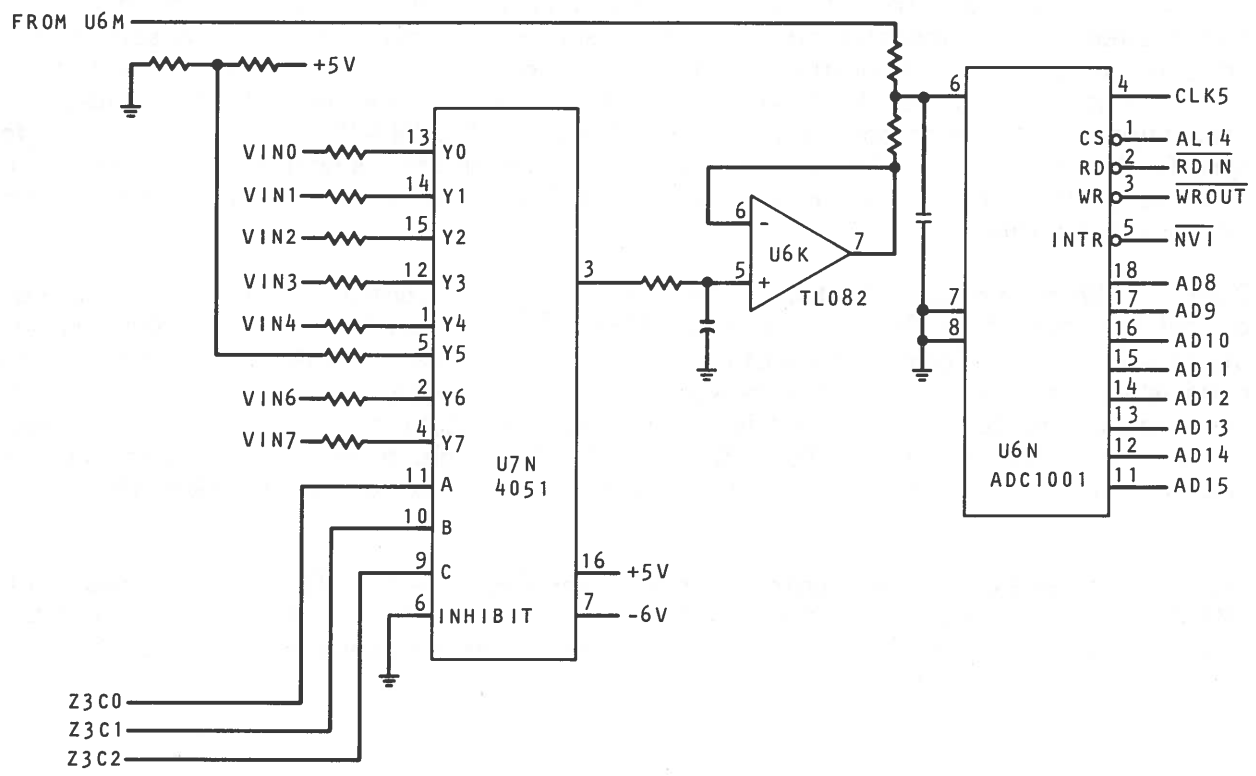

Figure 2-21. Analog-to-Digital Converter Circuit

2-54. **Supply and Takeup Servo Circuit.** (See Figure 2-22.) Two positive (V20P and V30P) and two negative (V20M and V30M) voltage sources are applied to the servo circuits. The microprocessor selects either the V20P and V20M or the V30P and V30M voltage sources based on the operating requirements of the CTU. The Z3A6 signal from the microprocessor turns Q6 on and enables the V30P voltage source to the collectors of output drivers Q1 and Q3. CR11 isolates the V20P source from the V30P line when Q6 is enabled. The V30P voltage supply is selected during the load sequence (to lock the supply reel on the supply hub) and during operation at 100 ips in the forward direction. For all other operations, the V20P voltage source is enabled. The Z3A5 output from the microprocessor controls Q24 and Q25 which generate the VHMON* signal. VHMON* (low true) turns Q5 on to enable the V30M voltage source, which is applied to the collectors of Q4 and Q2. CR12 isolates the V30M and V20M voltages when Q5 is enabled.

2-55. The ISU input to U2A-1 is the drive signal (supply current) from the DAC. The ISU signal, through U2A-3 and U2B-2, turns Q14, Q15, and Q3 on for forward tape motion, or Q12, Q13, and Q4 for reverse tape motion. Z3A7 selects the U2B-1 output to stabilize U2A-3 when the supply motor is not enabled. SMDH, through U2C-10, develops the VS and VIN3 signals. Current limiting feedback is provided by R130, U2A-10, and U2C-12.

2-56. The takeup motor servo circuit is identical to the supply circuit except that the ITU input provides the drive signal from the DAC.

2-57. **Arm Position and Rate Circuit.** (See Figure 2-23.) The arm position and rate circuit monitors the position of the compliance arm and the rate at which the arm changes position. The circuit issues error signals to the DAC circuit to control the tape speed. A square wave from the microprocessor on the Z1B0 line is received at U17P-1 and applied to an integrator circuit. The resulting sawtooth waveform is sent to the compliance arm air capacitor via P4-6. The air capacitor is connected to a differentiator circuit at U20M-14. The frequency of the output at U20M-12 is proportional to the arm position. The VIN2 output of U20N-10 is sent to the DAC to specify the position of the arm. Resistor R35 creates an error signal when the arm is not at its original position. The VIN6 output to the DAC indicates the rate at which the arm changes its position.

2-58. **Write Voltage Control.** (See Figure 2-24.) Control for the write voltage circuit is provided by the RES* signal. When RES* is low, Q20 starts conducting and disables P21. This forms a protection circuit which eliminates glitches from the write head when the transport is being powered up initially. After the power-on reset delay has elapsed (greater than 1/2 but less than 1 second), Z3B0 may enable the write head current for write operation. The Z3B4 signal, when high, turns Q19 off to reduce the head current during 3200 bpi operation. The erase bar is controlled independently by Z3B2.

2-59. **Write Formatting Control Circuit.** (See Figure 2-25.) The write 2 times clock (W2XCLK) is received from the microprocessor section on the Z1CØ line. The W2XCLK signal is applied to U17R-3, a divide-by-two circuit, which operates the BITCLK at the same frequency as the data rate.

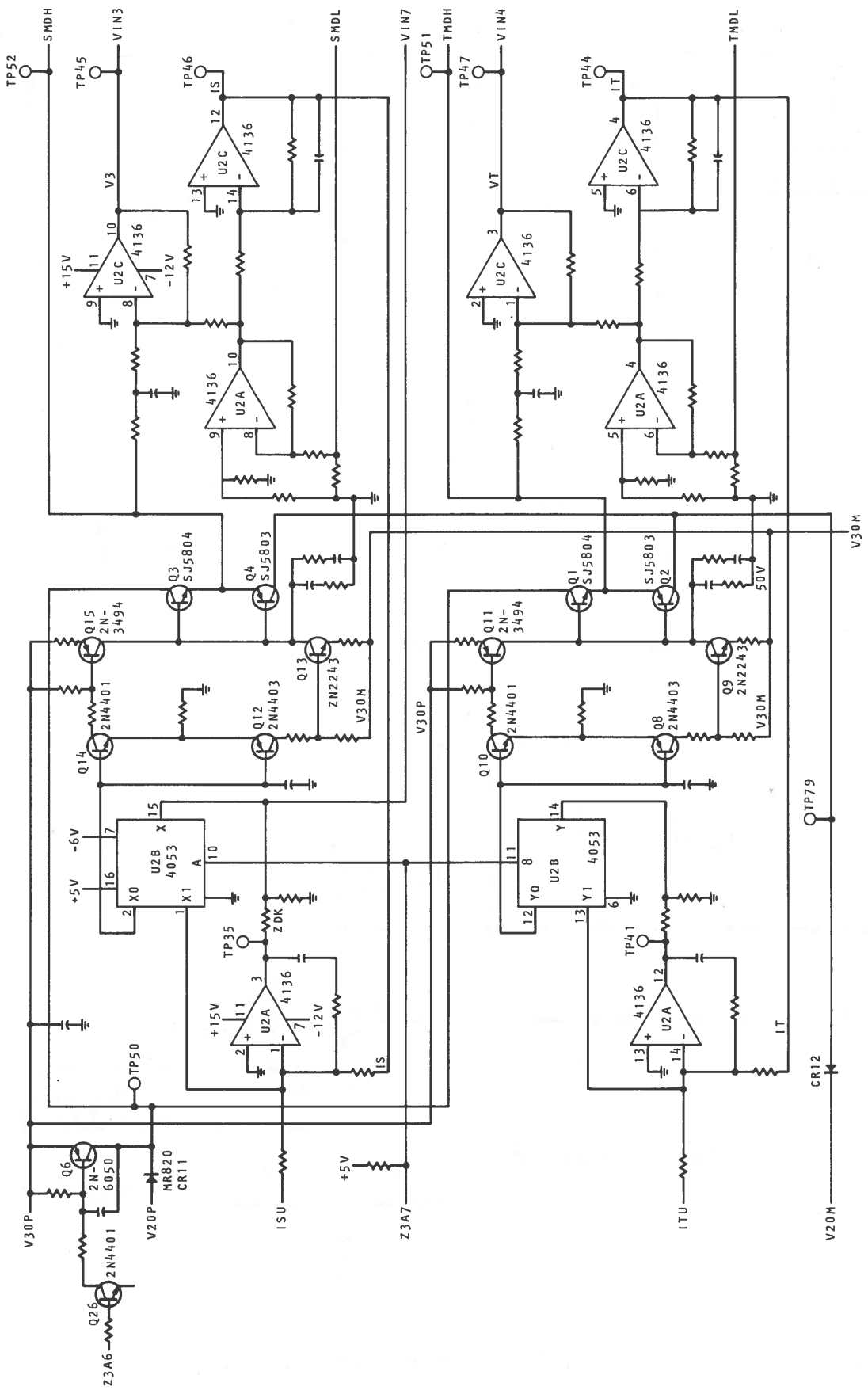

Figure 2-22. Supply and Takeup Servo Circuit

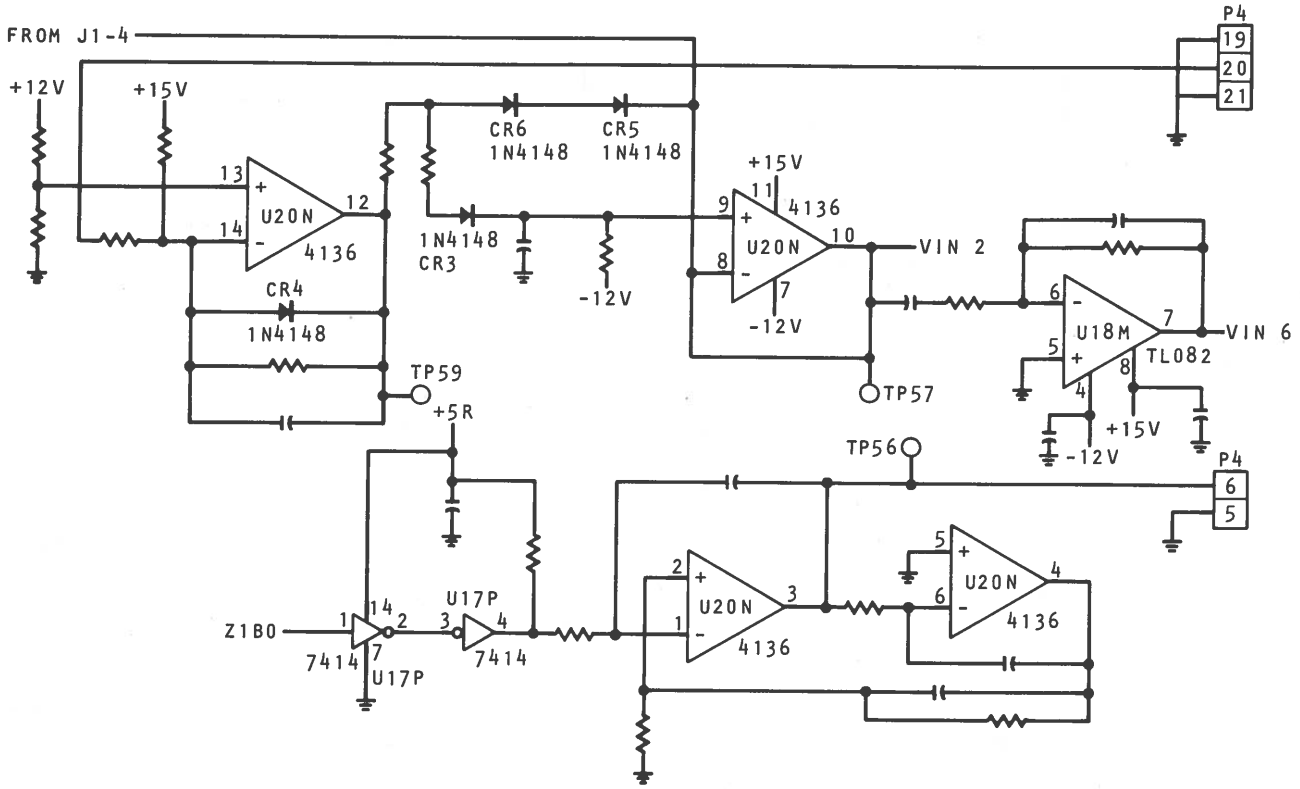

Figure 2-23. Arm Position and Rate Circuit

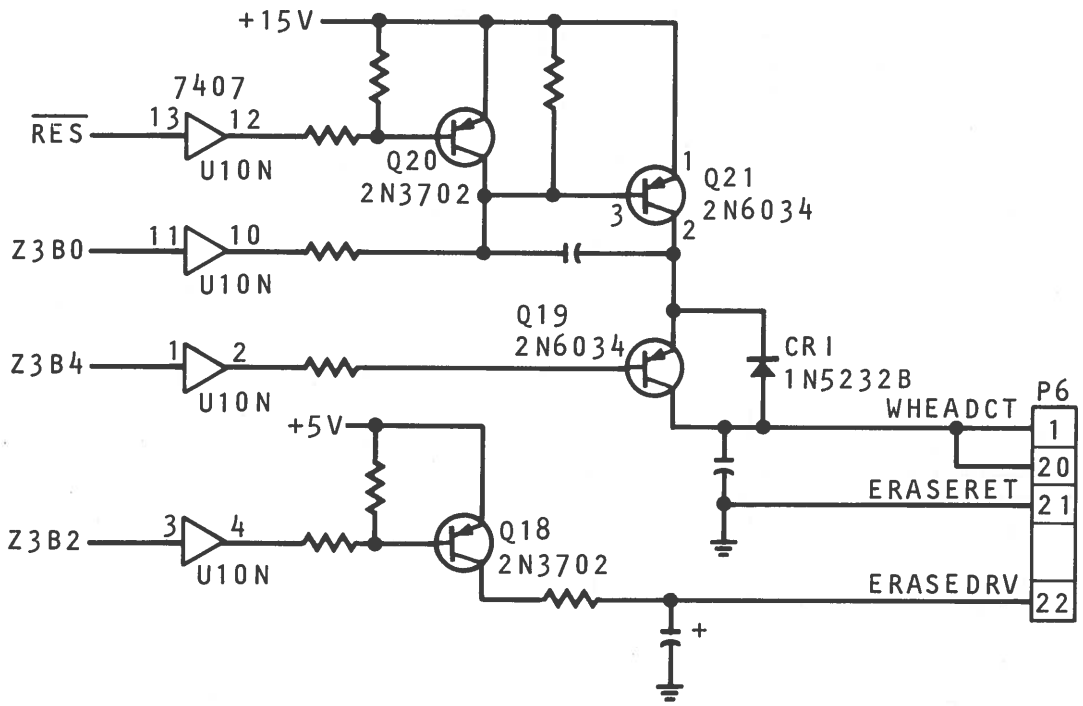

Figure 2-24. Write Voltage Control Circuit

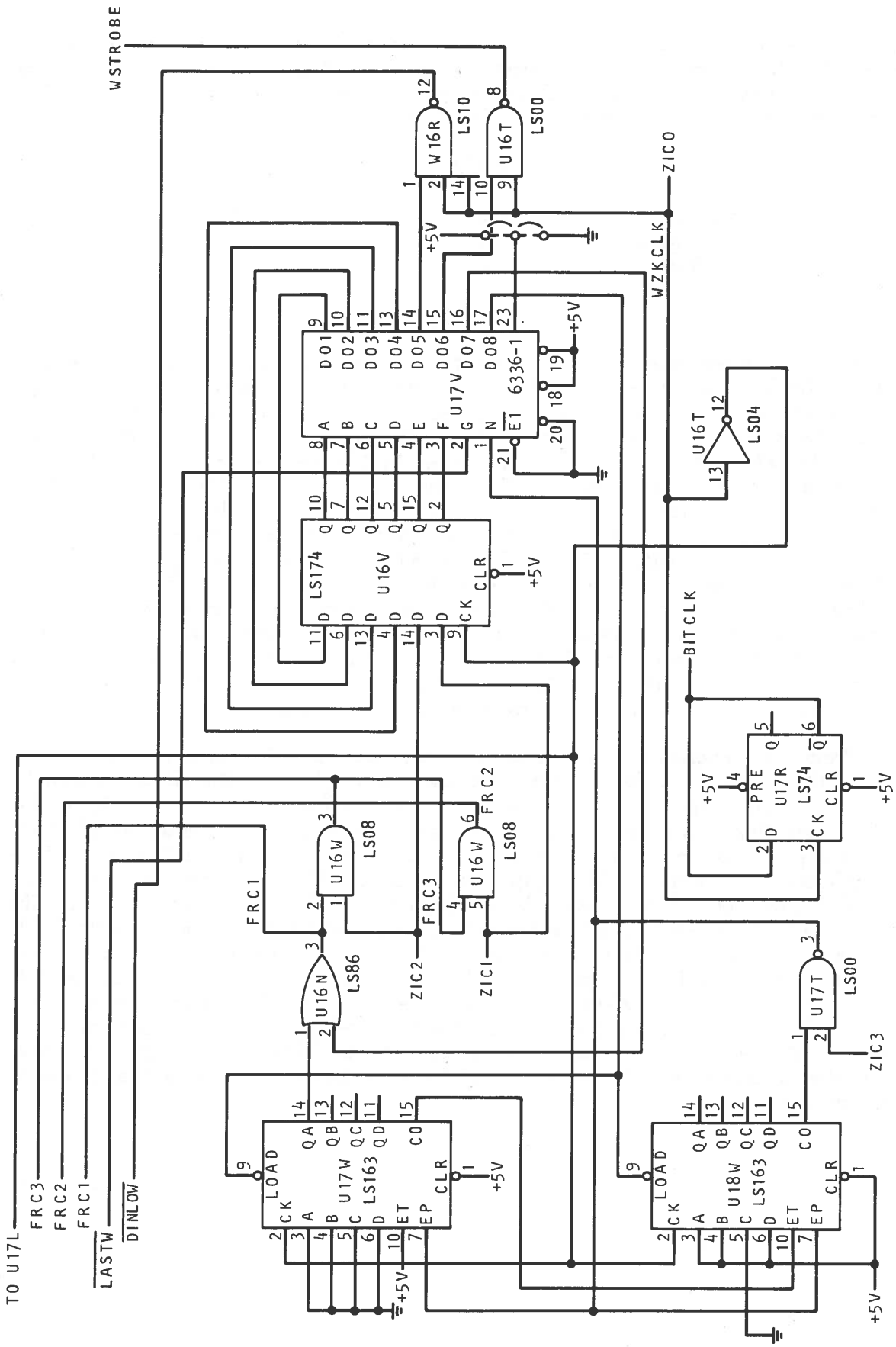

Figure 2-25. Write Formatting Control Circuit

2-60. The ZIC1 and ZIC2 signals are received from the microprocessor section and are applied to U16V-3 and U16V-14 respectively. The W2XCLK signal, inverted by U16T-12, clocks these signals to the E and F inputs of the data write EPROM (U17V). These inputs are decoded by the data write EPROM as follows:

	ZIC2	ZIC1
Reset	0	0
File Mark	1	0
ID Burst	0	1
Write Block	1	1

2-61. **ID Burst Generation.** The ID Burst is generated when the ZIC2 signal is inhibited and the ZIC1 signal is asserted. These signals are clocked through D-type flip-flops U16V by W2XCLK* and applied to the respective inputs of data write EPROM U17V to initialize the state machine sequence. The DO5 output of U17V is asserted, which enables the DINLOW* signal, thus inhibiting both write data registers (U16P and U17N) in the write data circuit. (See Figure 2-26.) The DO7 output of U17V remains low, conditioning XOR gate U16N-3 for the signal from counter U17W-14 (QA) at U16N-1. Counter U17W is clocked by the inverted W2XCLK pulses and divides the clock by two to produce pulses at the data rate at U17W-14. These become the FRC1 signal at U16N-3. The 1600 frpi FRC1 signal is sent to U16K-13 in the write data circuit (Figure 2-26) and clocked through to the write head drivers, thus generating the ID Burst on channel P only. After initializing the ID Burst on the ZIC2 and ZIC1 lines, the microprocessor allows an internal delay to ensure that the length of the ID Burst is correct, and then sends a reset command (ZIC2=Ø, ZIC1=Ø) to the U17V via U16V to terminate the operation. Figure 2-27 illustrates the ID Burst generation timing.

2-62. **Preamble Generation.** The write preamble function is initiated when ZIC1 and ZIC2 from the microprocessor section are asserted. During the write preamble operation, the DO6 output of U17V applies a low to U17T-10, which inhibits the WSTROBE signal, thus inhibiting data from the cache memory. The DO8 output of U17V goes low and preloads counters U17W and U18W, which are used to count 80 flux reversals (40 zero characters). The output pulses of U17W-14 are applied to pin 1 of exclusive -OR gate U6N. Since U6N-2 is held high by the DO7 output from U17V, U6N inverts the U17W-14 pulses to produce the FRC1, FRC2, and FRC3 signals. Both U17W and U18W are disabled by the carry output of U18W-15, which goes high at the end of the preset count of 80. The DO7 output of U17V then goes low and is applied to U6N-2. U6N-1 is held high by the U17W-14 output, thus preventing the flux reversal transitions of the FRC1, FRC2, and FRC3 signals. Since the flux reversal transition does not occur following the 40th zero character, an all-ones character is written on the tape indicating the end of the preamble and the beginning of the data block. The preamble timing is shown in Figure 2-28.

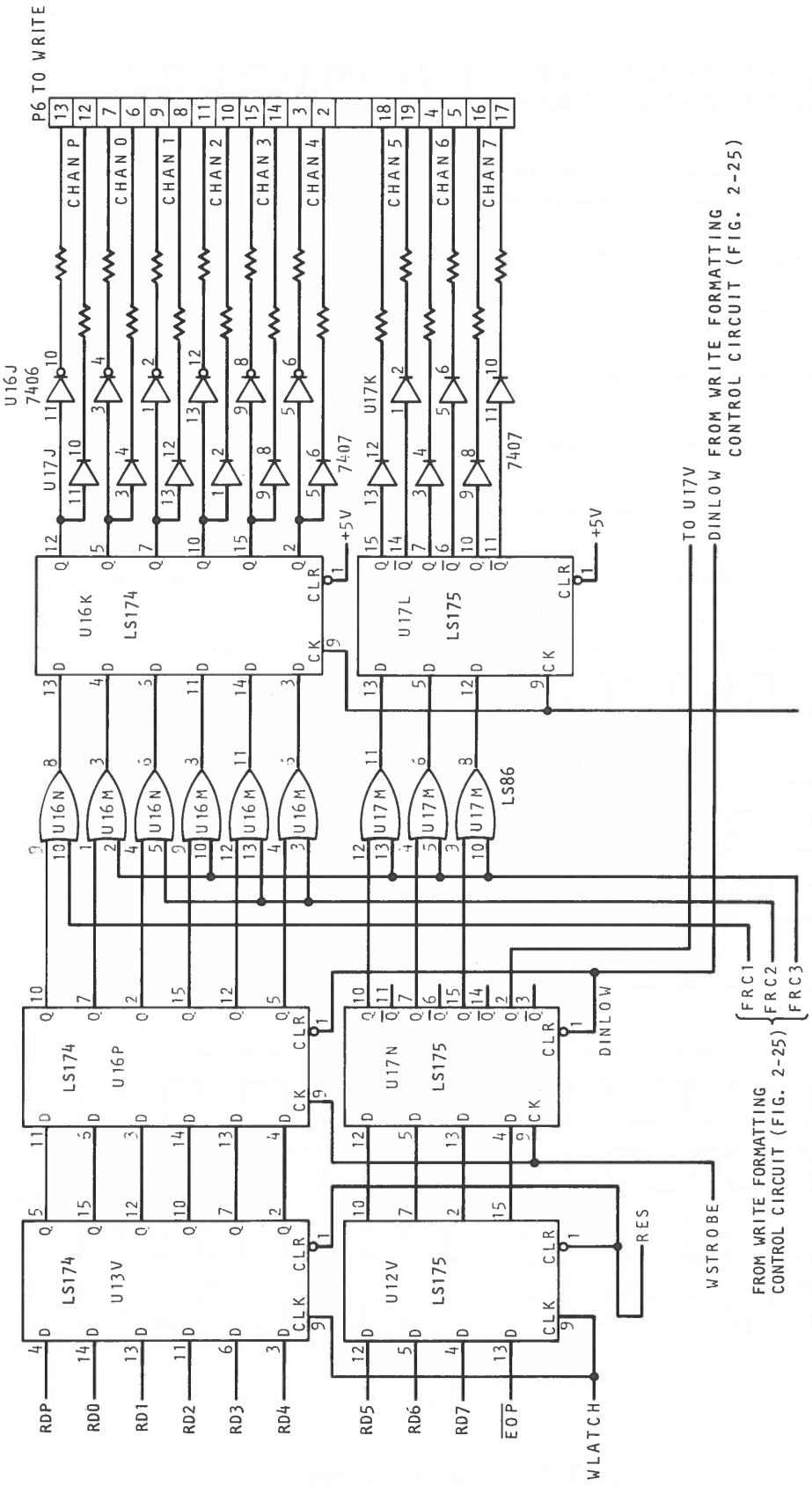

Figure 2-26. Write Formatter Circuit

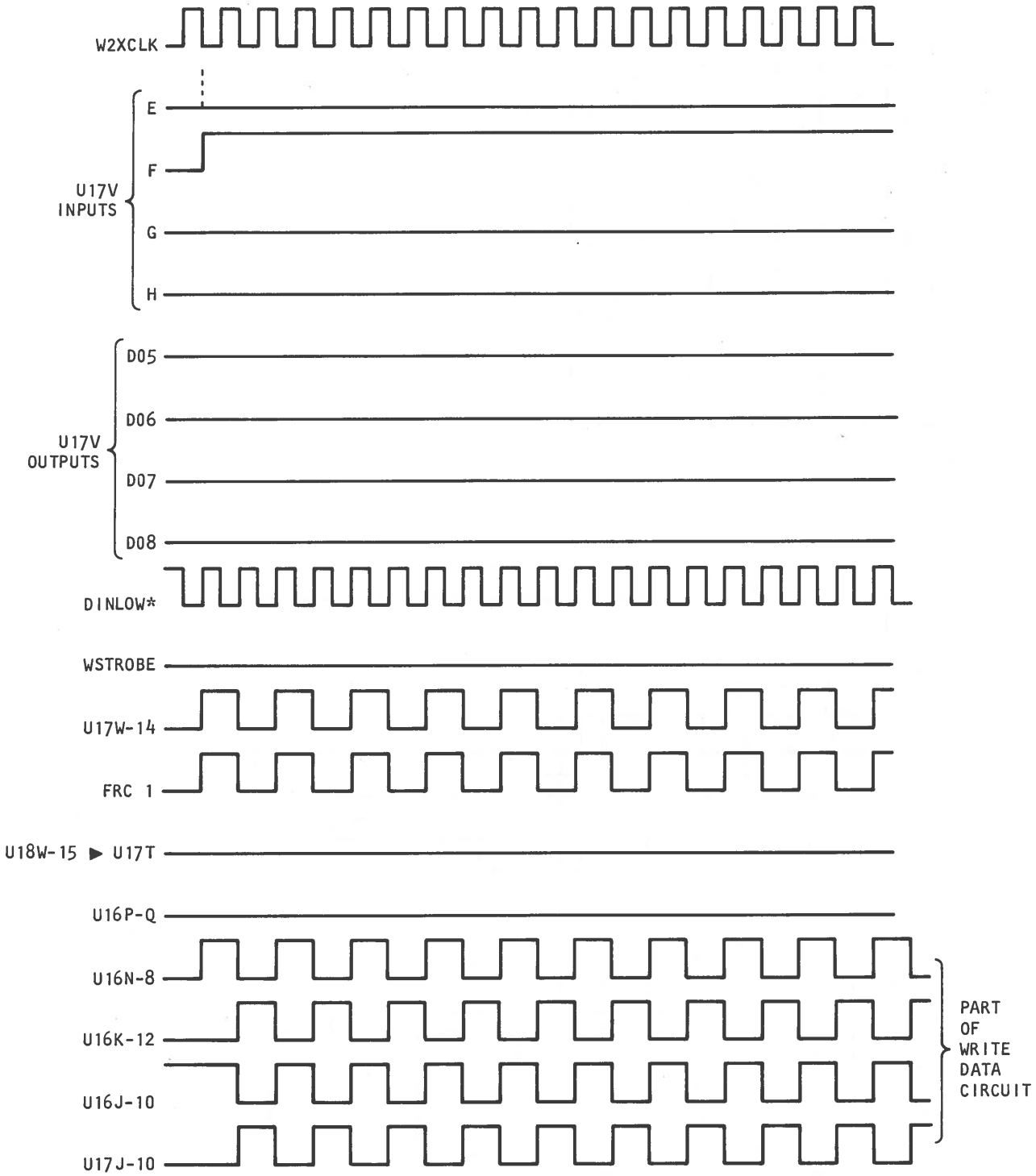

Figure 2-27. ID Burst Timing

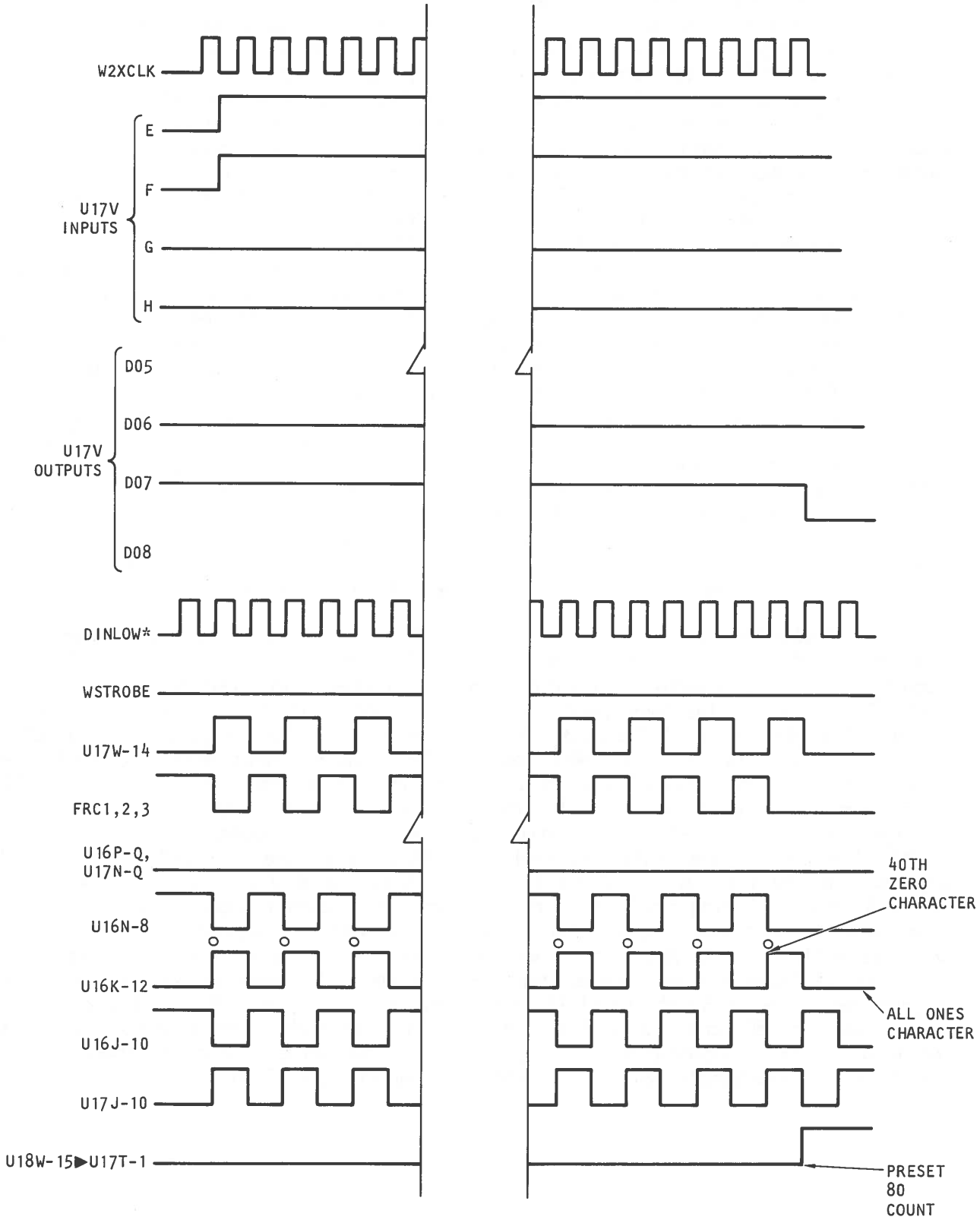

Figure 2-28. Write Preamble Timing

2-63. **Write Data Block Operation.** (See Figure 2-29.) To simplify the following explanation of the write data block operation, only the operation of the parity (P) channel is described. Immediately following the all ones character of the preamble, the D06 output of U17V starts toggling on the leading edge of W2XCLK. The W2XCLK and the D06 output are inverted by NAND gate U17T-8, developing the WSTROBE* clock which transfers write data from the cache memory to U16P and U17N. If the first character to be written on channel P is a one bit, a phase transition must be generated since the previous character was the one bit required to terminate the preamble. The FRC1 signal, now generated by the D07 output of U17V, switches from low to high at the same time as the WSTROBE* clock transfers the data (1 bit equals a low) from the cache to the output of U16P-10 via U13V. This low is XORed with the FRC1 signal causing the output of U16N-8 to go high. On the next W2XCLK* the output of U16K-12 goes high. The phase transition is written on the tape by the write head drivers U16J-10 and U17J-10. When the FRC1 line goes low, the output of U16N-8 switches from high to low, and through U16S-10 and U17S-10, reverses the flow of current through the write head winding which produces a one bit on the tape. If the next character in the data block is a zero bit, a phase transition will not be generated and the RDP line must be switched from a low to a high. This high is transferred to U16P by the WSTROBE* clock and is routed to U16N-9. The FRC1 signal goes high which causes the output of U16N-8 to remain low. Since there is no change of state on the D input of U16P-11, the next W2XCLK* does not generate a phase transition on the tape. The zero data bit is applied to the D input of U16P-11 as a high when the FRC1 signal goes low and, on the next W2XCLK* pulse, is applied to the write head drivers U16J-10 and U17J-10 which produces a flux reversal to write a zero bit on the tape. Write data is transferred from the interface to the tape in this manner until the ILWD interface line is asserted.

2-64. **Postamble Generation.** (See Figures 2-25 and 2-26.) The write postamble function is initiated when the last word (LASTW*) pulse is transferred to U17V-2. This occurs when the last byte of the data block is clocked into U16P and U17N by the WSTROBE signal. This increments data write ROM U17V to its next state, which initiates the generation of the postamble by asserting the DO5 output. The high DO5 output is applied to pin 1 of NAND gate U16R. On the next W2XCLK pulse, the DINLOW* output at U16R-12 goes low, clearing write input registers U16P and U17N, and begins to toggle at the W2XCLK rate. The Q outputs of registers U16P and U17N are low, and are applied to nine write data exclusive -OR gates U16N, U16M, and U17M. The other inputs to the nine exclusive -OR gates are the FRC1, FRC2, and FRC3 signals. The FRC1 signal is inhibited for one clock period at U16N-3 by the DO7 output of U17V, thus inhibiting FRC2 and FRC3. Since both inputs to each of the nine write data exclusive -OR gates are low, the outputs of the gates go low, and are applied to the D inputs of U16K and U17L. These lows are transferred to the write head drivers U16J, U17J, and U17K, where the all-ones character required at the beginning of the postamble is generated. The DO8 output of U17V goes low, loading counters U11P and U12P to the preset count of 80, and the DO7 output of U17V goes high. The 40 zero characters required for the postamble are then generated in the same manner as those in the preamble. The postamble generation timing is shown in Figure 2-30.

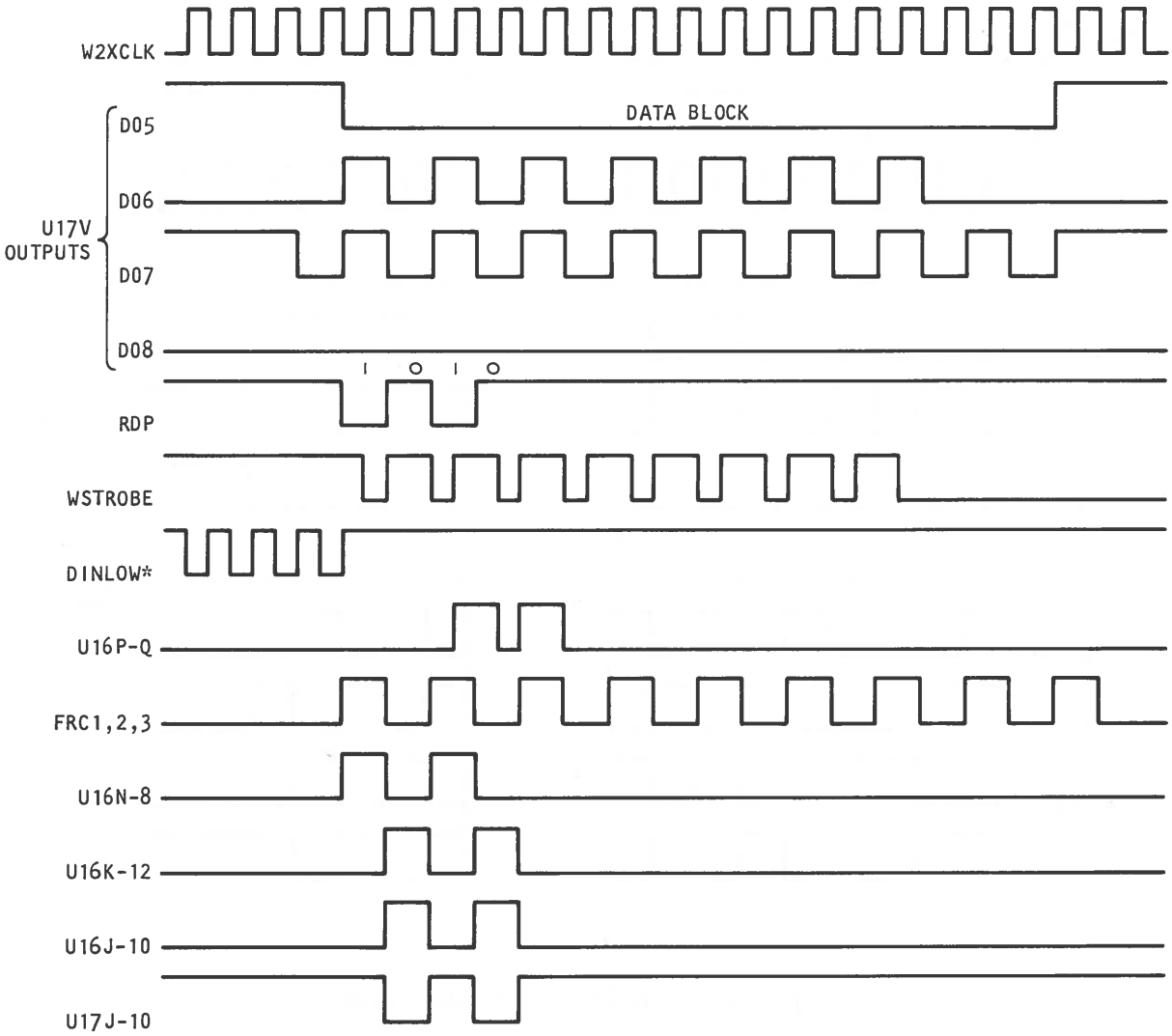

Figure 2-29. Write Data Block Timing

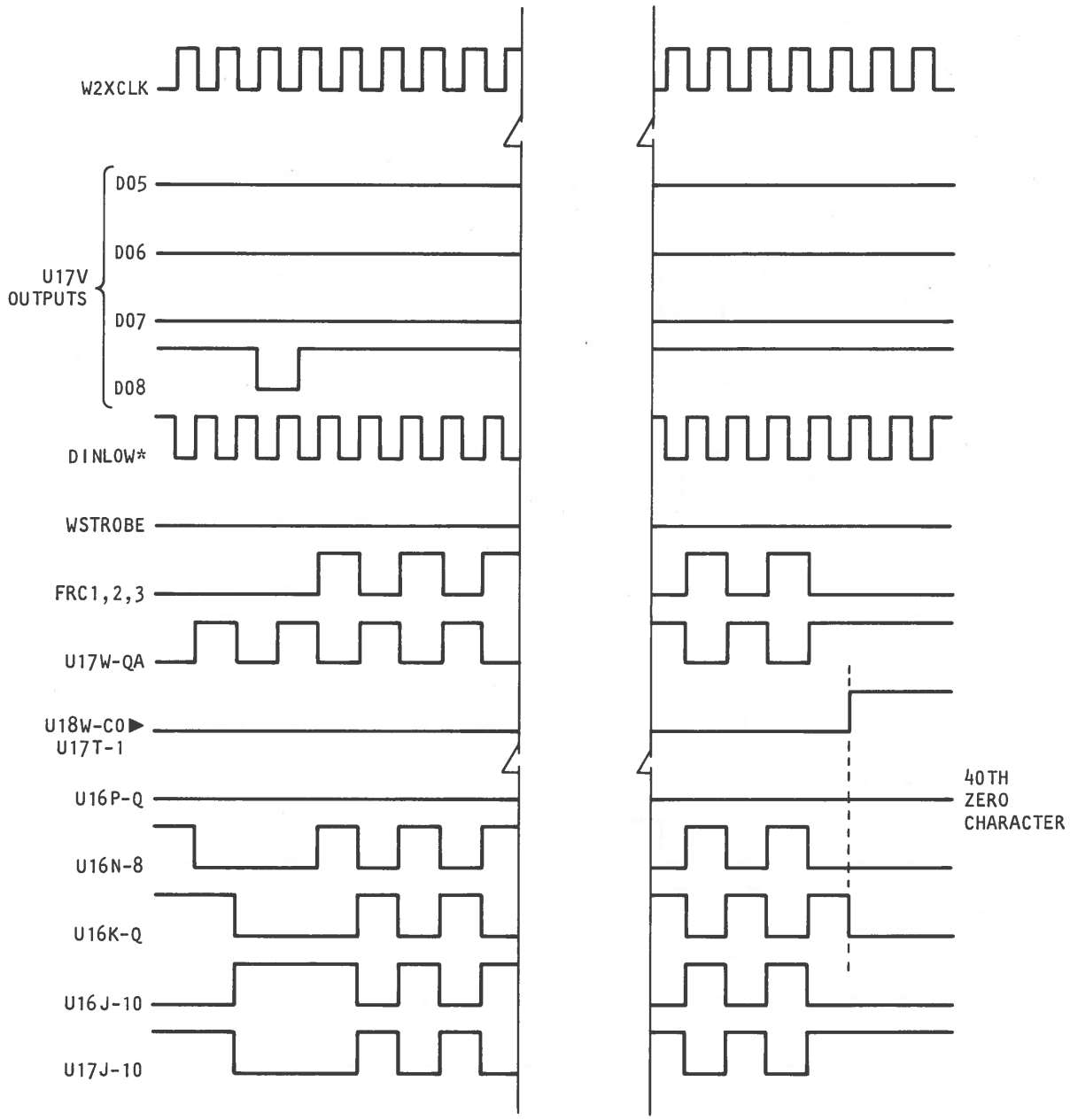

Figure 2-30. Write Postamble Timing

2-65. **File Mark Generation.** The write file mark function of data write ROM U17V is initiated when the ZIC2 line is asserted and the ZIC1 line is inhibited. The DO6 output of U17V is low, holding the WSTROBE signal high at NAND gate U17T-8. This prevents any data from the cache memory from being written during the file mark operation. Counters U17W and U18W are enabled by the DO8 output of U17V. The output of U17W-14 is XORed with the DO7 output of U17V, which is asserted during a file mark operation. The U17W-14 signal is thus inverted at U16N-3. These pulses are applied to the FRC1 and FRC3 lines only since the FRC2 line is inhibited by the low input of ZIC1 at U16W-5. This allows 40 zero characters to be written on channels P, 0, 2, 5, 6, and 7 only. After the 40 zero characters are written, the counters are disabled by the CO output of U18W-15. The processor is notified that the file mark has been written by cache structures in RAM that have a bit set indicating the structure has been fixed to tape. A reset command (ZIC2=Ø, ZIC1=Ø) is issued by the microprocessor to clear U17V. The write file mark timing is shown in Figure 2-31.

2-66. **Test/Diagnostic Write Operation.** Operation of the write circuitry during Service Aid 12 is initiated when the microprocessor asserts both the ZIC1 and ZIC2 lines, thus beginning the preamble. (See paragraph 2-62.) When the preamble is complete, U17V increments to the next write state and begins normal write data operation. (See paragraph 2-63.) The DO5 output of U17V is low, holding DINLOW* high and causing the U16P-Q and U17N-Q outputs to be low. A 40-character record of all zeros is sent to the write head drivers. At the completion of the write operation, the microprocessor issues a reset (ZIC1 = 0, ZIC2 = 0) to terminate the write data function. Service Aid 13 activates the file mark circuitry by asserting the ZIC2 line and inhibiting the ZIC1 line. A complete file mark is then written. (Refer to paragraph 2-65.)

2-67. **Read Amplifier Circuits.** (See Figure 2-32.) The read amplifier and phase discrimination theory presented applies to channel 2, and is typical of all nine read channels. The first two amplification stages consist of operational amplifiers U19E-6 and U18E-1. U18E-7 is configured as a voltage follower that buffers the signal before it is applied to threshold detector U15F-7. The ITHR signal is an analog voltage level developed by the DAC circuit which, in conjunction with R109, establishes the peak detection threshold at U14F-9. Once R109 is properly adjusted, the microprocessor controls the final threshold level according to the interface command. The data signal is also applied to the non-inverting input of comparator U14F-4. The inverting input, U14F-5, is tied to ground and holds the output, U14F-12, at a 5-volt level until the negative transition of the data signal. Thus, RDATA2 is an inverted and digitized representation of the data signal.

2-68. **Read Discrimination Circuits.** (See Figure 2-33.) The RDROP*2 signal is applied to the K input of U13F-13 and is transferred to the Q* output on the next PECLK pulse (22 X data rate) as the CHDROP2 signal. The RDATA2 signal is routed from the read amplifier circuit to U13D-3 and after two PECLK pulses is XORed with the FWD signal at U12D-13. During the first part of the preamble, the PENAB* signal is inhibited, which causes the output of U12E-6 to remain high until a phase transition is detected by U12D-3. When a phase transition is detected, U12E-6 goes low and enables the load input of U9D-9. Since the first character in the preamble is a zero, represented by a logic low at U12D-13, the output of U12D-11 goes high and asserts the DATA2 signal. This high is loaded into the four data inputs of U9D and causes its count to output 15, which asserts the CO output at U9D-15. The CO, routed to U12E-1, allows the next transition to be detected as a 0 data bit. The output of U12E-3 pulses low when the data transition is detected and is routed to the K input of U7A-3. The SCAN 2 signal, which is low at this time, is inverted by U8B-5 and applied

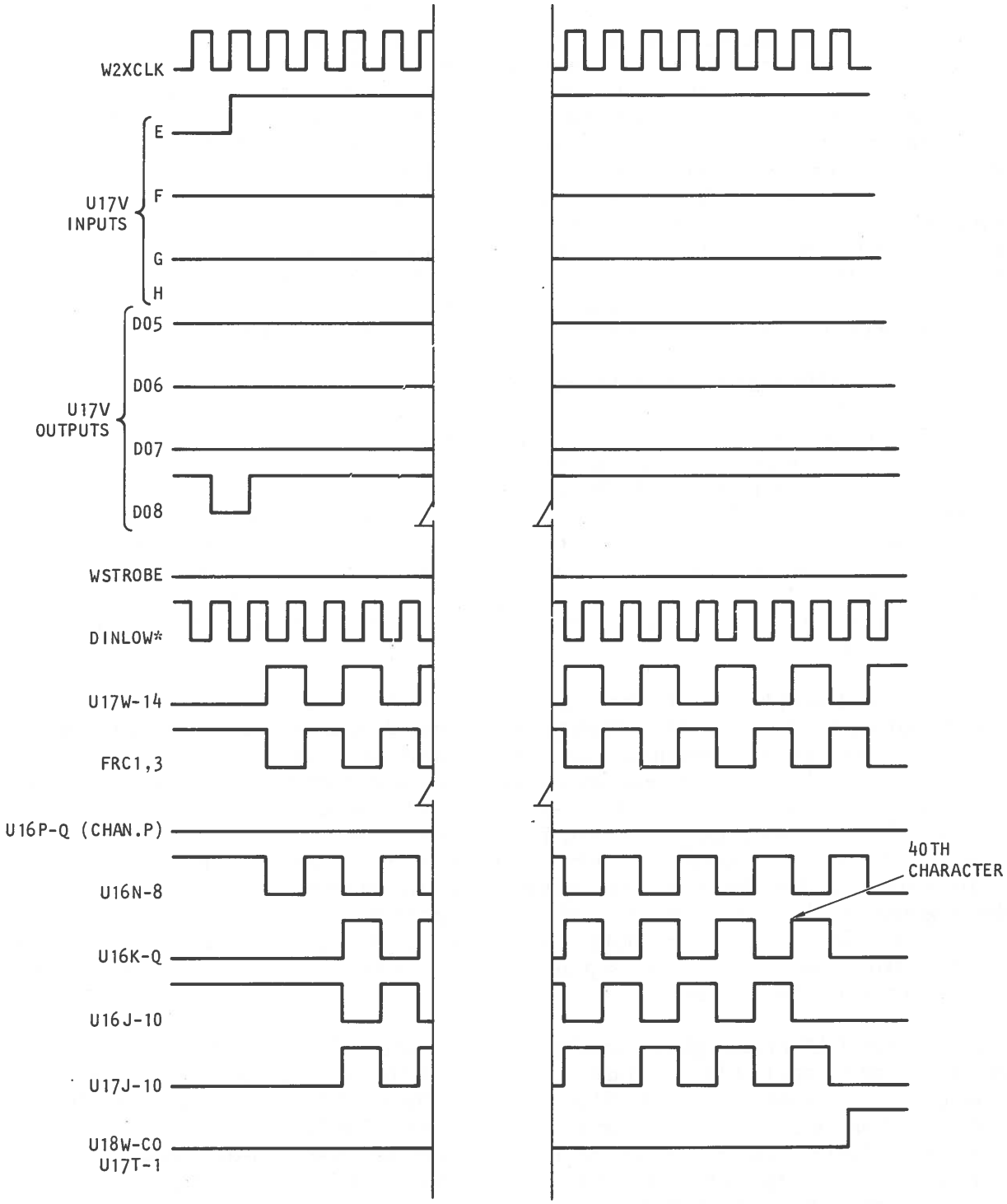

Figure 2-31. Write File Mark Timing

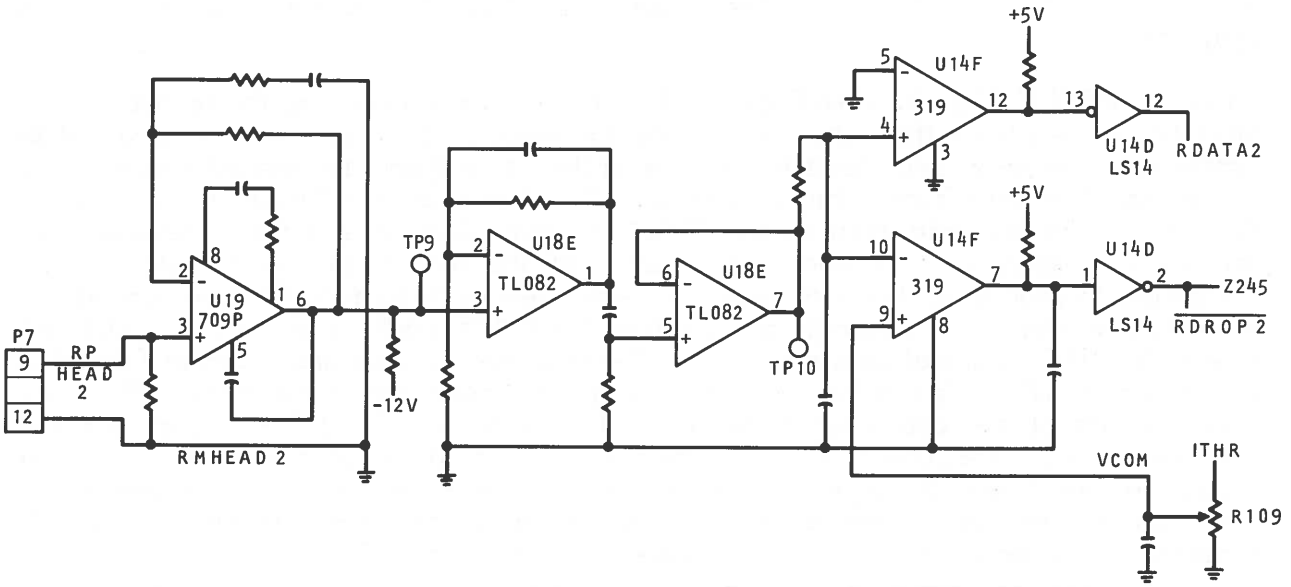

Figure 2-32. Read Amplifier Circuit (Typical)

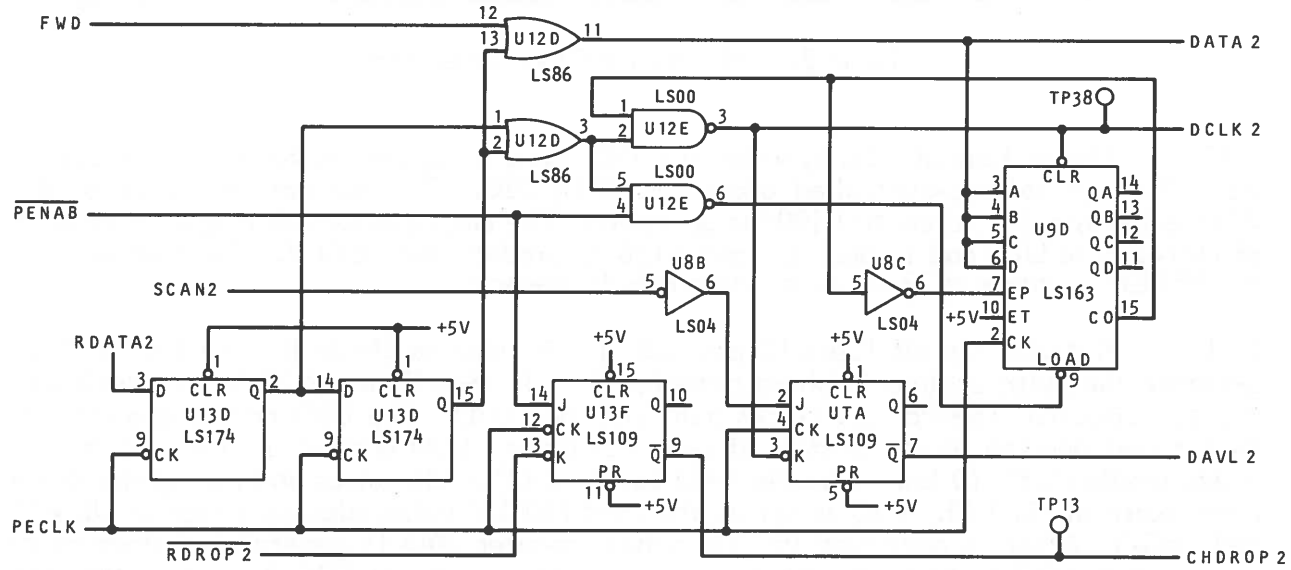

Figure 2-33. Read Discriminator Circuit (Typical)

to the J input of U7A-2. On the next PECLK, the Q* output of U7A-7 goes high and asserts the DAVL 2 line. When the SCAN2* pulse goes high, the Q* output of U7A-7 is inhibited on the next PECLK. See Figures 2-34 through 2-36 for read data timing diagrams.

2-69. **PECLK Circuit.** (See Figure 2-37.) For PE tape recording, the recovery clock must be derived from the data itself, since the velocity of a tape transport cannot be controlled precisely and head-to-tape velocity is subject to instantaneous speed variations. The data from either channel 2 (DCLK2) or channel 1 (DCLK1) is selected by decoder U7E as the data input to the PECLK circuit. Channel 2 is the preferable input because it is physically located in the center of the read head and is therefore less vulnerable to read data dropouts caused by tape skew or instantaneous speed variations. When two or more data channels are inactive, the GAP* signal is asserted and U7E will select the BITCLK signal as a reference. The selection codings are shown in Table 2-3. The output at U7E-7 is a pulse, selected as described from one of the three U7E inputs, which occurs at the character frequency. The pulse at U5G-3 (the phase detector) attempts to track the pulse on U5G-1. The phase detection produces positive or negative pulses on pins 5 and 10, depending upon the difference in the two frequencies on pins 1 and 3. The two voltage pulses either add to or subtract from the charge stored in capacitor C104, which increases or decreases the voltage at U5G-8.

CHDROP 2 (U7E-14)	GAP* (U7E-2)	SELECTED CLOCK (U7E-7)
0	0	BITCLK
0	1	DCLK2
1	0	BITCLK
1	1	DCLK1

Table 2-3. Reference Clock Selection

2-70. The voltage at U5G-8, which is a DC level, is applied to the frequency control input through voltage-controlled oscillator (VCO) U3C. The natural frequency of the VCO is set by C101 to control 100 ips operation. The output of U3C-8 is applied to pin 4 of NAND gate U2E and through L1 and R138 to produce the PECLK. The frequency of the PECLK is stable at 22 times the data rate frequency.

2-71. A divide circuit (U4D-15 and U3D-10) is used to divide the PECLK by 22 to generate the pulse applied to phase detector U5G-3. (See Figure 2-38 for the timing of the ÷22 circuit.) The PECLK clocks both U4D and U3D. The U4D device is a counter that is preloaded to 10 at the start of each ÷22 cycle. U3D is reset on the first PECLK pulse, sending U3D-10 low. Counter U4D counts six PECLK pulses and then generates a carry pulse at U4D-15. U3D is set on the next PECLK pulse, placing a high at U2G-10 and U5G-3. After 16 additional PECLK pulses, counter U4D-15 generates another carry pulse. With U3D-10 high, the carry pulse generates a low at U2G-8, causing the load signal at U4D-9 to go low and reload counter U4D to 10 for the next ÷22 cycle. U3D is reset on the next PECLK pulse, sending the low ÷22 signal from U3D-10 to U5G-3. The cycle is then repeated.

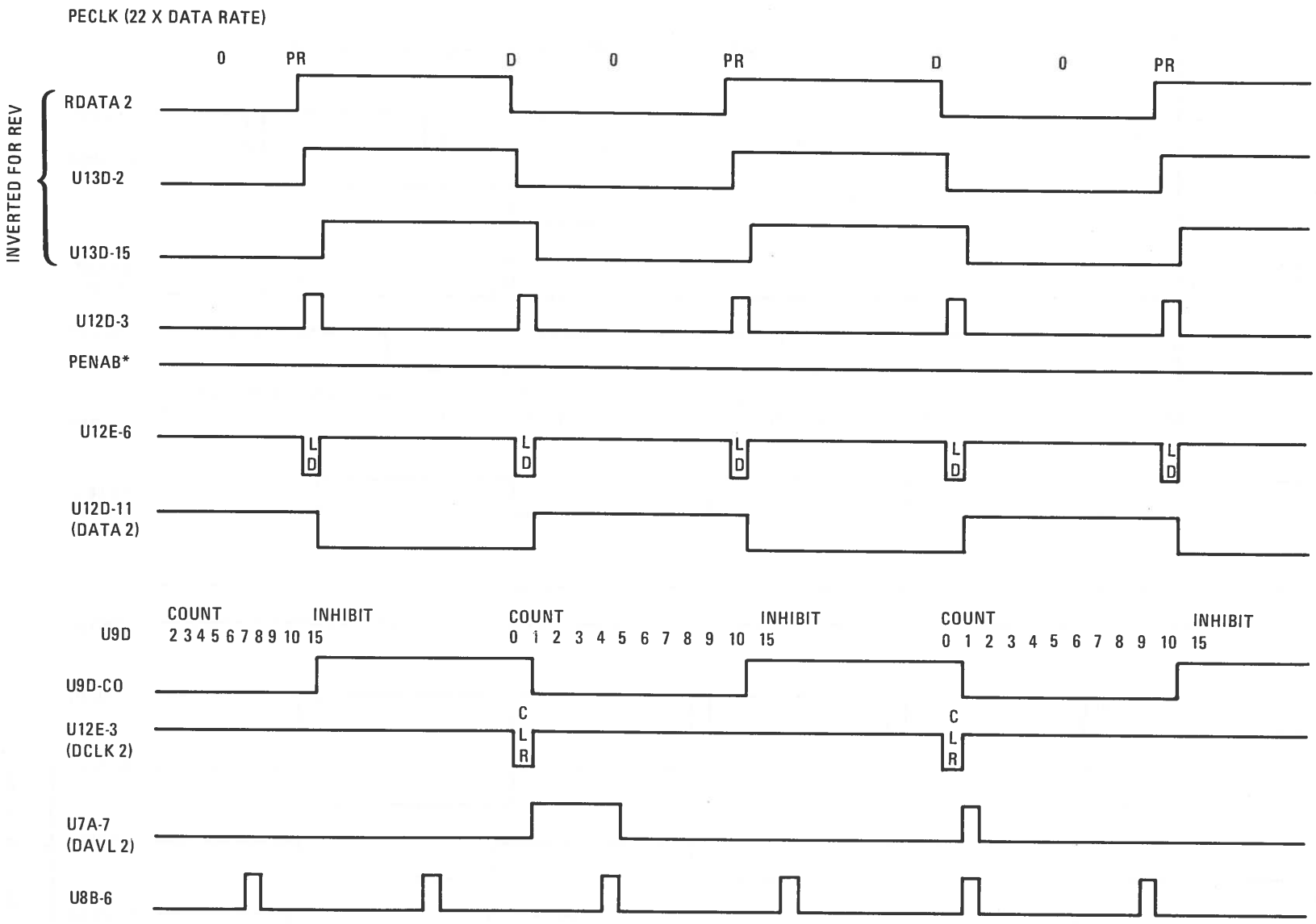

Figure 2-34. Read Data Timing, Forward Preamble (Block False)

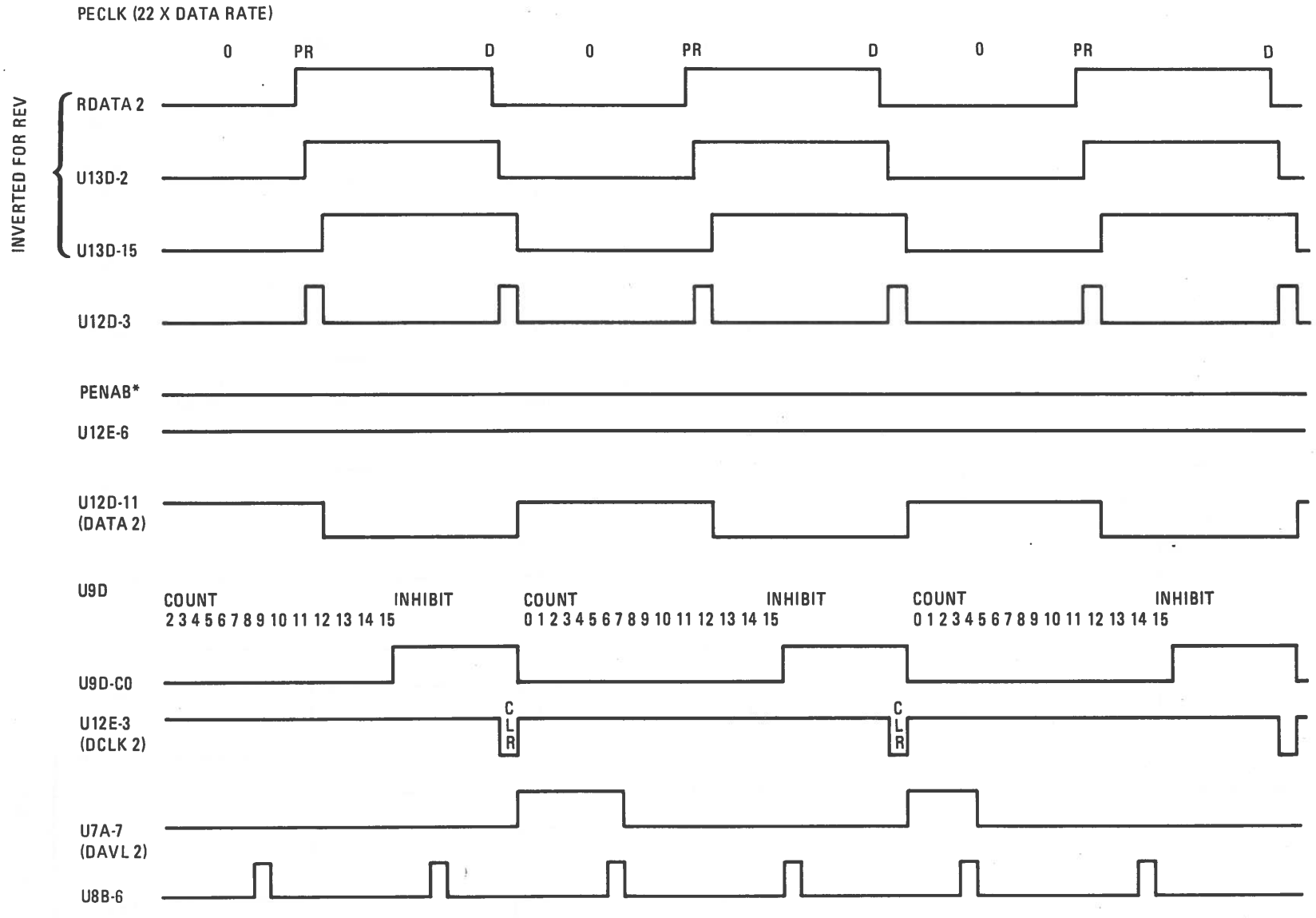

Figure 2-35. Read Data Timing, Forward Preamble (Block True)

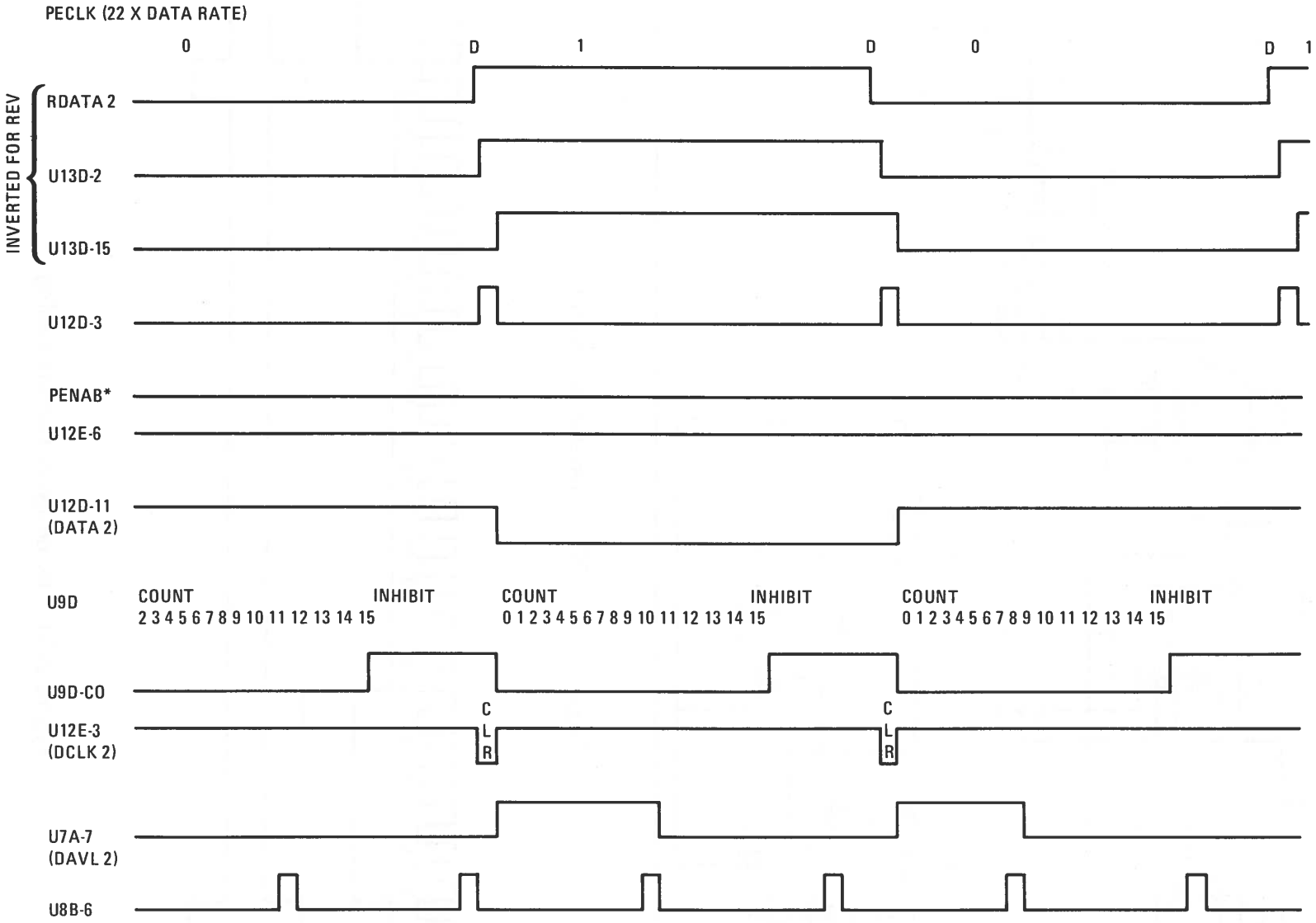

Figure 2-36. Read Data Timing (Forward)

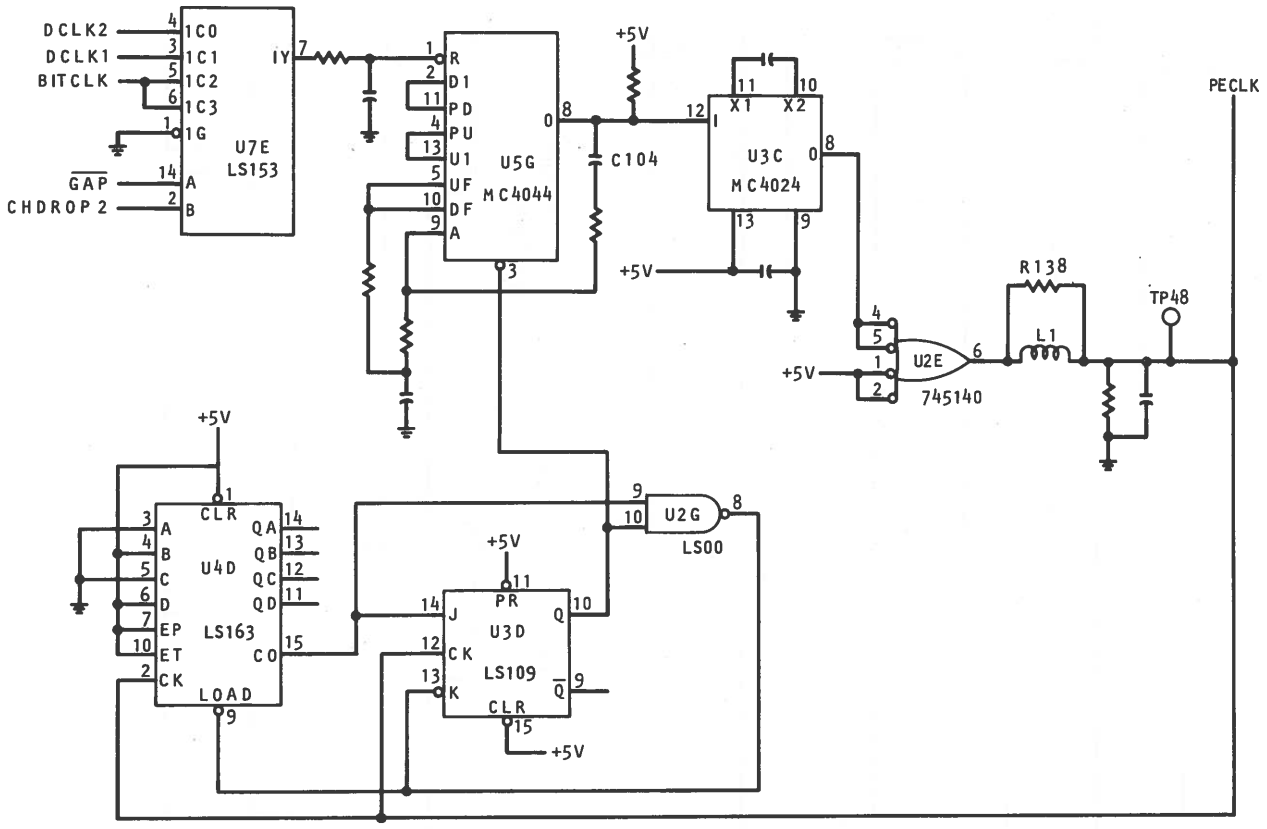

Figure 2-37. PECLK Generation Circuit

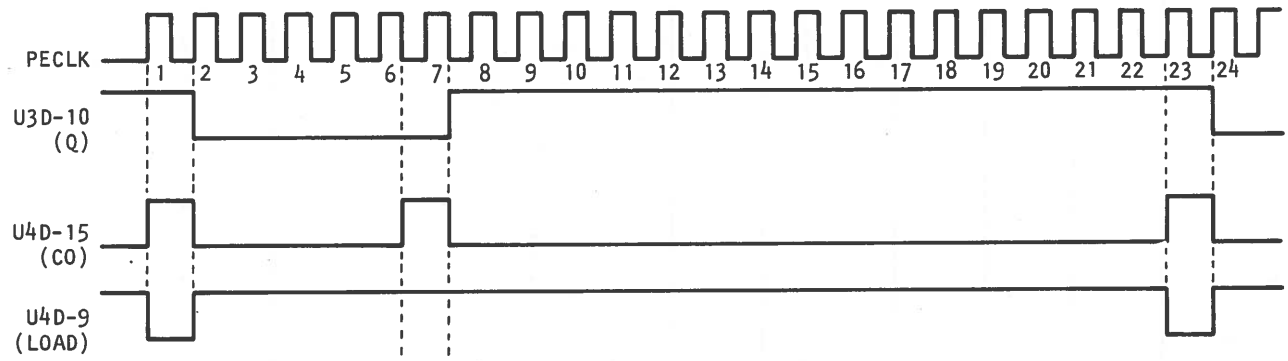

Figure 2-38. Divide-by-22 Circuit Timing

2-72. **Scan Generator.** (See Figure 2-39.) Four-bit binary counter U7D and decoder U8D generate signals to the read discriminator that multiplex 9 channels of parallel data into a serial bit stream. Counter U7D, which is clocked by the PECLK, produces a, b, and c outputs that represent a serial count (1, 2, 3...8). U8D decodes the a, b, and c inputs and sequentially enables the SCANØ* through SCAN7* outputs. The parity (SCANP*) output is generated by U7D when the counter has completed its 8-bit count. The output at U7D-11 asserts PSEL and is inverted by U4G-4 to produce SCANP*, which synchronously clears U7D. Each SCAN* (0-7, P) pulse at its appropriate channel time is sent to the read discriminator and resets the DAVL latch for the respective channel. The outputs of the read discriminator circuits (DAVLØ-7, P; DATAØ-7, P; CHDROPØ-7, P) are multiplexed from parallel to serial form by U7C, U10F, U10G, and U9E. The a, b, and c lines select each of the data lines and parity for each of the channel times. This permits each read channel to assert a data input to the read skew buffer circuit registers time-independent of all other channels if the data bytes on the tape are skewed with respect to the head.

2-73. **Read Skew Buffer Circuit.** (See Figure 2-40.) The following description assumes there is no read skew. The serialized outputs of the scan generator multiplexers (DAVLX, DATAOX, and CHDROPX) are applied to the A4, A5, and A7 inputs of skew buffer ROM U9G. U9G outputs 04, 03, 02, and 01 are applied to 9-bit serial shift registers U9F/U6F-15 (shift register 1), U8F/U6F-12 (shift register 2), U8E/U6F-10 (shift register 3), and U7F/U6F-2 (shift register 4). For each SCAN(n) time corresponding to a read data channel (Ø-7, P), when A4 (DAVLX) is true, the logic level at A5 (DATAOX) is inverted at 04 and routed to shift register 1. For each succeeding bit time, if DAVLX is true, the bit for that channel is moved into shift register 1. If a channel is dropped, CHDROPX pulsing at that SCAN(n) time on input A7 forces a zero to be entered into the shift register. As each data bit is input, bits for that SCAN(n) time entered previously in shift register 1 will now be at the A3 input, and the 03 output will be applied to shift register 2. Data in shift registers 2 and 3 will be moved to the next register in the same manner (A2 to 02 and A1 to 01). For SCAN(n) times that data has not been detected (DAVLX false), any bits entered will be recirculated within the same shift register (A3 to 04, A2 to 03, A1 to 02, and A0 to 01) until a new input is asserted to cause a shift up one register.

2-74. Prior to detecting a data block, the inverted PEN* signal clears each shift register to all zeros. As the preamble all zeros are read and input to the skew buffer, the shift registers effectively remain cleared. The first non-zero byte read will be the all ones preceeding the first data byte of the record. It will be input to register 1. The first data byte forces the all ones byte into shift register 2, and the second data byte moves the all ones to shift register 3. The third data byte moves the all ones to shift register 4 and asserts a non-zero at 01 for the first time. This flags U7G, the PE control ROM, on input A4, that the skew buffer is full. Outputs are asserted at the SCAN0 time following the first bit flagging U7G at A4. PSEL pulses at input U7G-15 (A7) at SCANP time and asserts output 02. Delayed for one clock period at U6F-5, DOUT asserts at SCAN0 time and will remain true through SCANP time. With DOUT asserted at the A6 input and the all ones serving as pointers, U9G will output the first data byte at U9G-15, the 06 output, beginning with 0 through 7 and P in turn. The output logic levels are inverted again and through U11F-8 (CDATAX) are input to serial-to-parallel shift register U14W in the cache bus interface logic. U5F-8 asserts DCLK* when the serial output has set up on U14W (DOUT, PSEL, and PECLK*). DCLK* clocks U15W in the cache bus interface logic to latch the data bits to the read data lines. DCLK* also is used in the DMA control logic to reset DREQ0 (write to physical tape).

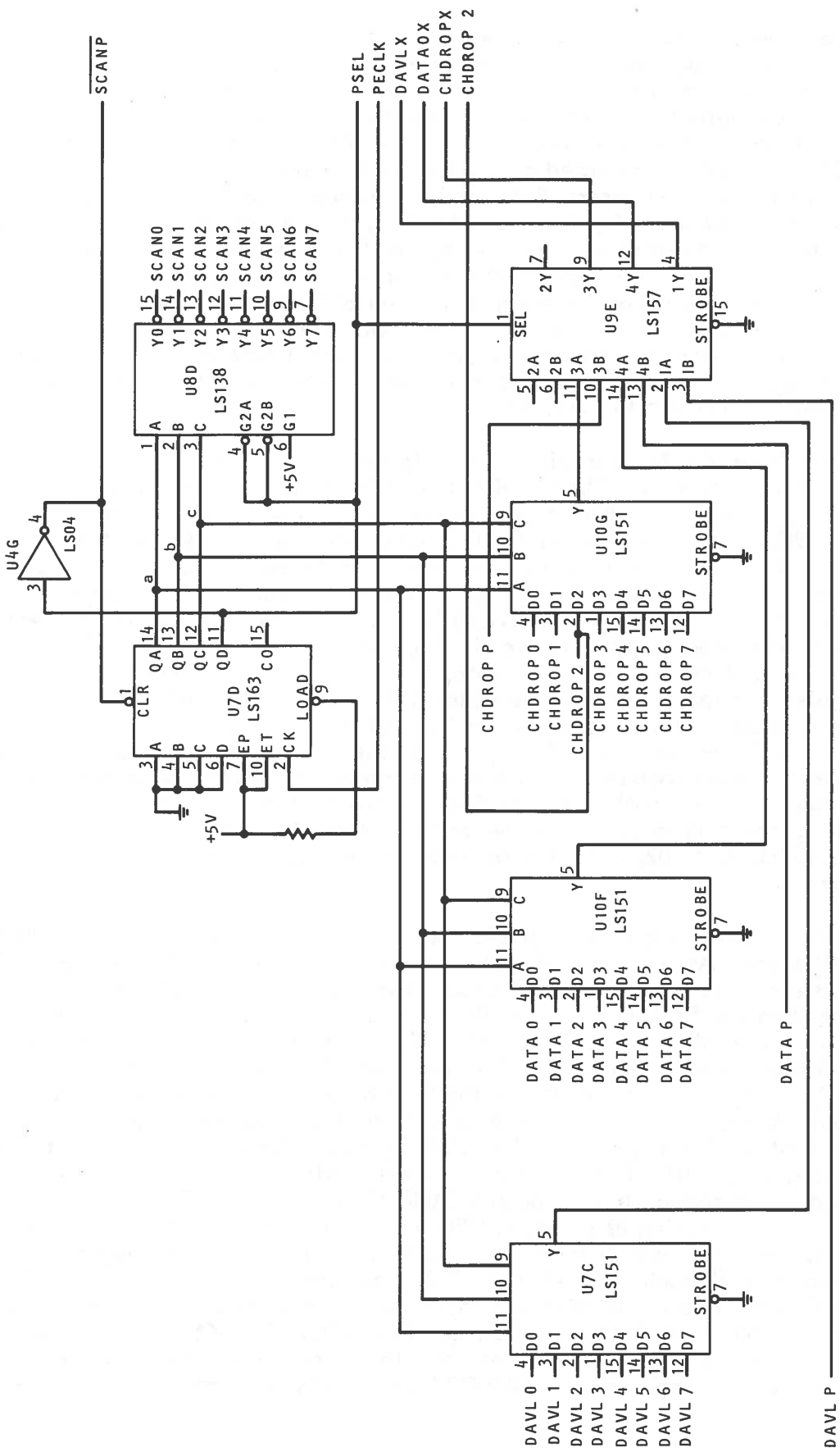

Figure 2-39. Scan Generator Circuits

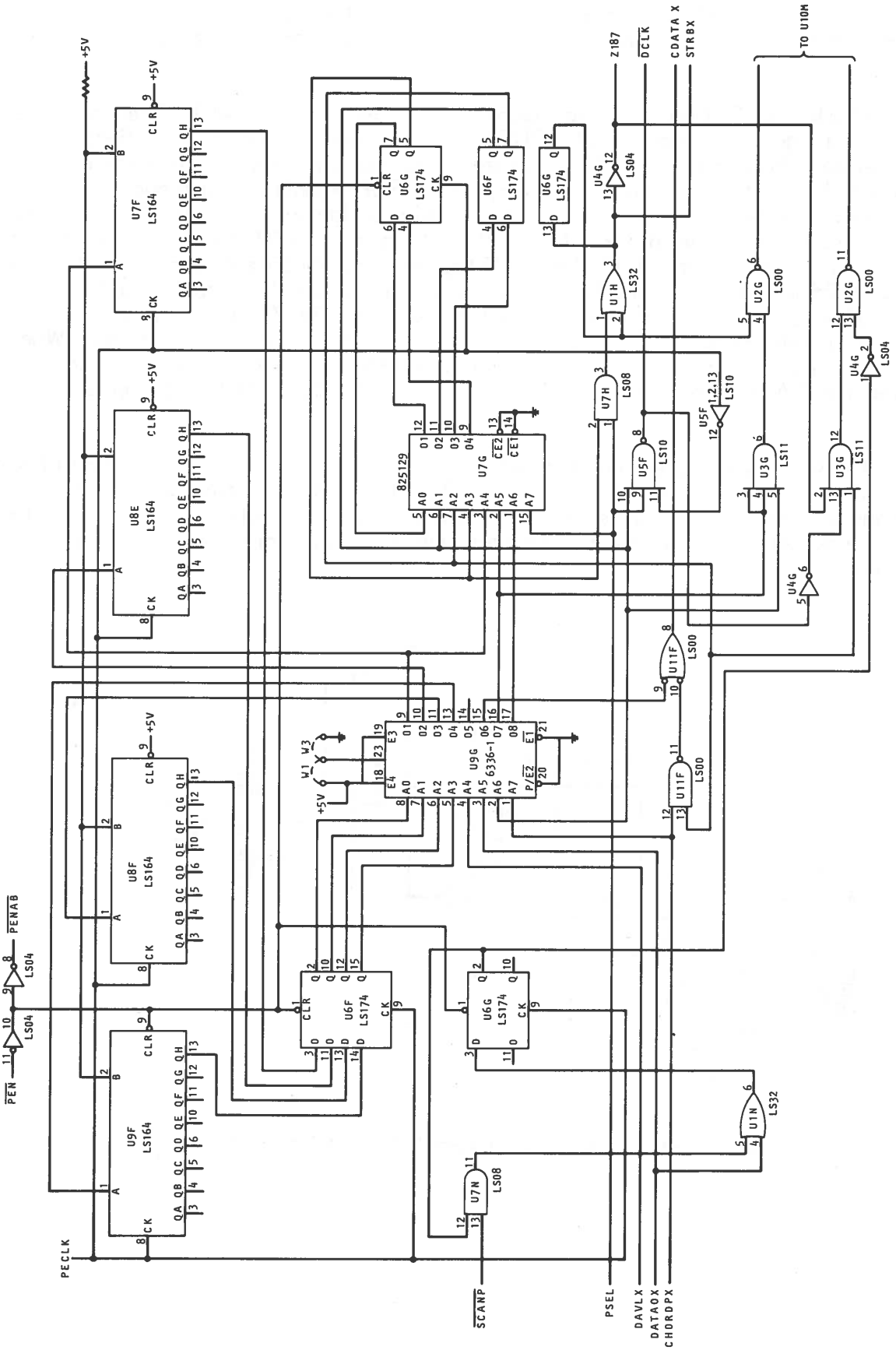

Figure 2-40. Read Skew Buffer Circuit

2-75. The all ones byte is re-positioned in shift register 3 by U9G and will be used in the same manner through the remainder of the data block to initiate outputs through U7G.

2-76. **Block/Gap Detect Interrupt Generator.** (See Figure 2-41.) The block/gap detect interrupt generator consists of a PROM (U12W), two differential amplifiers (U6H), a J-K flip-flop (U5H), and timing (R-C) components. The circuit determines the activity taking place (ID burst, gap, etc.) by checking the RDROP signals for each channel. When two or more channels are active, the PROM generates a high output at U12W-12. A time constant circuit consisting of resistor R110 and capacitor C92 provides a delay of approximately 25 characters at 100 ips, 1600 bpi, to allow stabilization of read data on the lines. U5H is clocked by the PECLK signal and is set by the output of differential amplifier U6HP-13 when two or more channels are active. The Z2B4 output at U5H-10 is sent to the microprocessor via C10 U11L to notify the CPU of the data activity. When no channel activity is occurring, the output at U12W-11 causes U6HP-1 to go low, generating the GAP* signal and resetting U5W to notify the CPU that a gap has been detected.

2-77. **Configuration Selection Circuit.** (See Figure 2-42.) The configuration selection circuit consists of eight switches (U3T) that are used to select system options. The options selected by the U3T switch positions are shown in Tables 2-4 and 2-5. The switches are polled during power-up. When any switch positions are changed, power must be recycled.

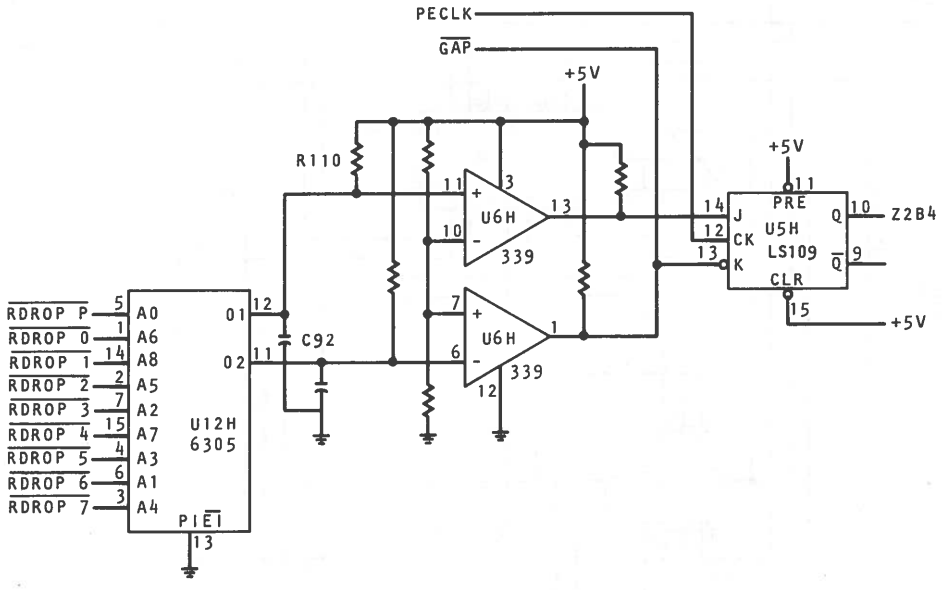

Figure 2-41. Block/Gap Detect Interrupt Generator

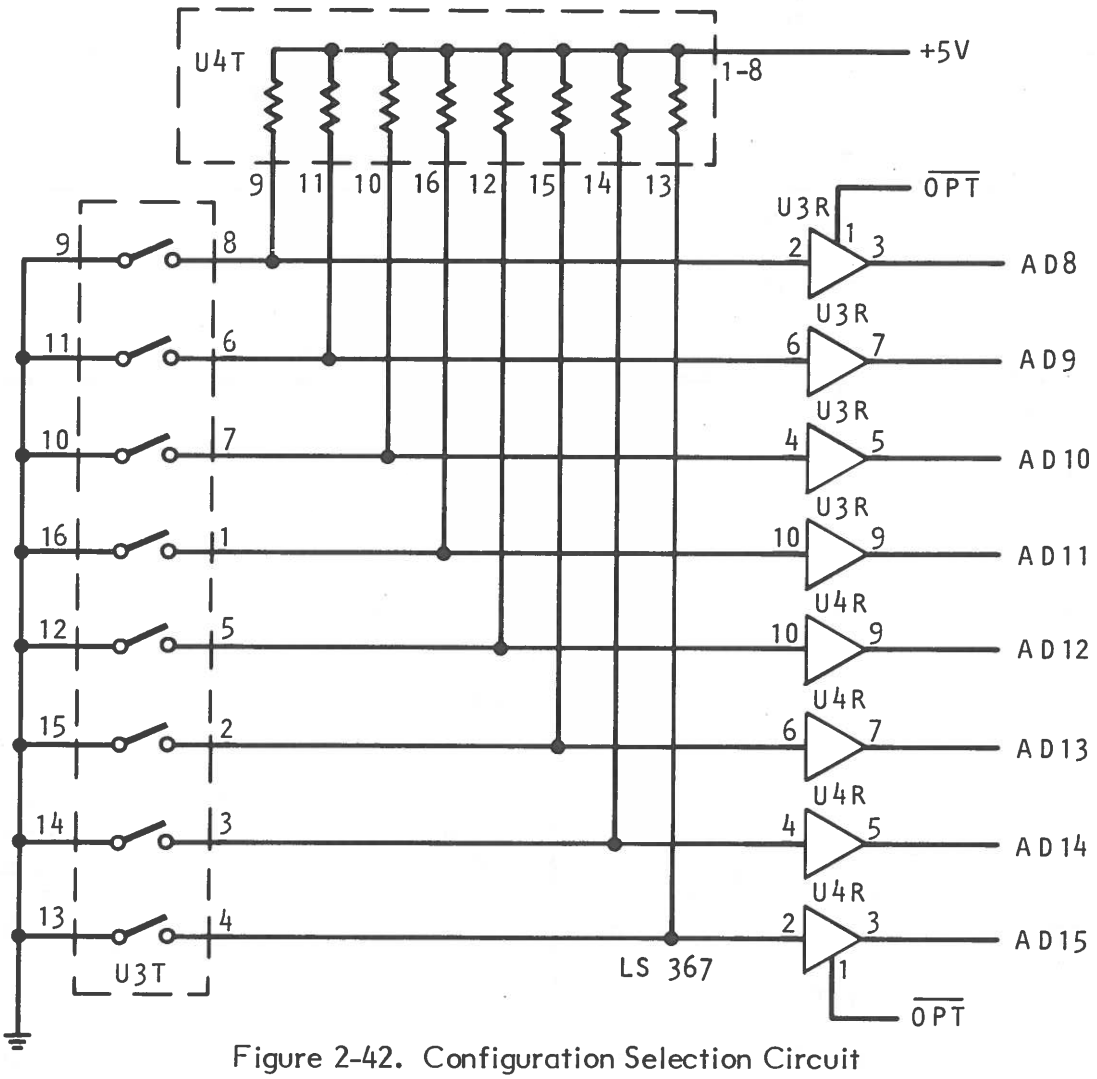

Figure 2-42. Configuration Selection Circuit

POSITION			FUNCTION		
1 Closed (On) 1 Open (Off)			EOT LOCATION Enabled EOT LOCATION Disabled		
2 Closed (On) 2 Open (Off)			External Parity Internal Parity		
3	4		Select max. block size		
open	open		9 K bytes		
closed	open		16 K bytes		
open	closed		24 K bytes		
closed	closed		32 K bytes		
5			Not Used (Leave Off)		
6	7	8	Select Simulated Speed (ips)	Data Rate (KBS)	Ramp Delay (ms)
open	open	open	12.5	20	30
closed	open	open	25	40	15
open	closed	open	37.5	60	10
closed	closed	open	45	72	8.3
open	open	closed	75	120	5.0
closed	open	closed	75	120	5.0
open	closed	closed	75	120	5.0
closed	closed	closed	75	120	5.0

Table 2-4. Configuration Switches U3T Selections (Model 890)

POSITION	FUNCTION
1 Closed (On)	EOT LOCATION Enabled
1 Open (Off)	EOT LOCATION Disabled
2 Closed (On)	External Parity
2 Open (Off)	Internal Parity

3	4	Select max. block size
open	open	9 K bytes
closed	open	16 K bytes
open	closed	24 K bytes
closed	closed	32 K bytes

5 open	Enable ramp delay
5 closed	Disable ramp delay

6	7	8	Select Simulated Speed (IPS (Avg & Min/Max)	Data Rate (KBS) (Avg & Min/Max)	Ramp Delay (msec) (If Enabled)
open	open	open	45	72	8.3
closed	open	open	75	120	5.0
open	closed	open	100	160	3.7
closed	closed	open	112 (103/120)	180 (165/192)	3.0
open	open	closed	125 (108/140)	200 (172/225)	2.6
closed	open	closed	155 (138/170)	250 (220/272)	2.2
open	closed	closed	185 (160/206)	295 (256/330)	1.5
closed	closed	closed	250 (200/300)	400 (320/480)	1

Table 2-5. Configuration Switches U3T Selections (Model 891)

SECTION III

GLOSSARY OF TERMS

AD0-AD15	Multiplexed address/data lines used to provide addresses and route data between the microprocessor and certain memory devices.
A/D	Analog-to-digital converter.
ADSTB	DMA address strobe output used to strobe the upper address byte into the cache address latch.
AL0-AL15	Latched address lines used by the microprocessor to address and enable control circuit memory devices and I/O devices.
AS*	Microprocessor address strobe. When active, indicates that the signals on the address lines are valid addresses.
AX0-AX7	DMA address lines. The four least significant bits (AX0-AX3) are bidirectional; the four most significant bits are outputs and are enabled only during DMA service.
BITCLK	Bit Clock. Used to generate PECLK when both channel two and channel one are dropped.
Block	Term identifying a data record. Block sizes of 9K, 16K, 24K, or 32K bytes are selectable via configuration switch U3T.
BOT	Beginning of Tape. Indicated by a reflective marker placed on the tape that is detected by an optical sensor.
BPI	Bits per inch. Specifies the packing density of data on the tape (1600 bpi standard, 3200 bpi optional).
B/W*	Byte/Word. A microprocessor output that defines the type of memory reference on the address/data bus.
CAS	Column Address Strobe. Used in cache memory addressing to enable columns of data in the cache RAM's.
CDATAX	Corrected Data Multiplexed. Data byte that is sent to the cache bus register in serial form.

CHANP, 0-7	Write data transmitted to the write head via drivers U17J and U17K.
CHDROP P, 0-7	Channel Drop Multiplexed. This signal represents the multiplexed channel drop signals.
CIO	Counter/timer and parallel I/O unit. Devices used to generate timing signals and provide I/O parts for the microprocessor.
CLK4	A 3.84-MHz clock signal used as a peripheral clock (PCLK) by the CIO's, and by the DMA logic and cache memory addressing circuit.
CLK5	A 3.84-MHz clock signal used to clock the analog-to-digital converter.
Command Reinstruct Time	During streaming operation, a period of time after reading or writing the last character of a data block in which the system must instruct the tape drive either to continue or enter a repositioning cycle.
CTU	Short form for the Models M890 and M891 CacheTape Unit.
DAC	Digital-to-analog converter device.
DACK0*-DACK3*	Data acknowledge signals from the DMA. Used to acknowledge the receipt of Data Request signals (DREQ0-DREQ3) from the microprocessor.
DATA0X	Data Zeroes Multiplexed. This signal represents the serialized data bits input into the skew buffer.
DATA P, 0-7	Data. Refers to the data lines from the read logic to the formatter.
DAVL P, 0-7	Data Available. Term identifying data that is positioned at the read head and is ready to be clocked into the formatter.
DAVLX	Data Available Multiplexed. This signal is used to input the serialized data into the skew buffer.
DCLK*	Data Clock. Generated in read skew buffer circuit; used in the cache bus interface logic to latch data bits to the read data lines.
DCLK1	Data Clock 1. Alternate input to the formatter read clock circuitry. Used in the event of data dropout in Read Channel 2.
DCLK2	Data Clock 2. Primary input to the formatter read clock circuitry. Synchronizes PE clock to the data rate.
DINLOW*	Data in Low. Enables write data to be clocked into the write formatter circuit from the write formatting control circuit.
DMA	Direct Memory Access controller. Provides control of cache memory operations independent of direct microprocessor control.

DMAIO — DMA Input/Output. Generated in the DMA control logic by signals from the microprocessor; used as a chip select signal to enable the DMA controller.

DOUT — Data Out. This signal is used to enable the output from the skew buffer.

DREQ0 — DMA Request 0. Request for DMA service to transfer data between cache memory and physical tape. (Highest priority DMA request.)

DREQ1 — DMA Request 1. Request for DMA service to transfer data between cache memory and host interface.

DREQ2 — DMA Request 2. Request for DMA service to perform microprocessor/cache memory communications via DMA.

DREQ3 — DMA Request 3. Request for DMA service to refresh cache memory. (Lowest priorty DMA request.)

DS* — Data Strobe. This signal is initiated by the microprocessor and is used to strobe data in and out of the CPU.

DX0-DX7 — DMA data bus lines. Bidirectional three-state signals used to transfer data between the cache memory and the DMA.

EEVEN — Generated by the parity generator and used during a memory read function to notify the microprocessor that a parity error (even parity) has been detected.

EOP* — End of Process. Generated by the DMA to indicate the completion of the current DMA service operation.

EOT — End of Tape. Indicated by a reflective marker placed on the tape that is detected by an optical sensor.

FBY — Formatter Busy. Generated by the transport status registers to signal the host interface on the IFBY line that tape motion is occurring.

File Mark — A special control block consisting of 80 flux reversals (40 characters) at 3200 frpi in channels P, 0, 2, 5, 6, and 7 with channels 1, 3, and 4 dc erased.

FRC1,2,3 — Flux Reversal Control Lines. These lines determine the write formatter mode of operation. They are used as follows:

	FRC1	FRC2	FRC3
Write ID Burst	1	0	0
Write File Mark	1	0	1
Write Data	1	1	1

frpi	Flux reversals per inch. The number of changes of polarity, or flux changes, that occur during each one-inch segment of tape.
FSEL	Formatter Select. This signal indicates drive is selected by comparing the unit number of the drive to the IFAD and ITAD lines. FSEL enables drive status information (IONL, IRDY, etc.) to be sent to the controller.
FWD	Forward. This signal indicates forward tape motion to the read discriminator circuit.
GAP*	Gap Detected. Generated by the block/gap detection logic when no channel activity is occurring to notify the microprocessor that a gap has been detected.
GO	Initiated by IGO from the interface. Indicates that the CTU is on-line and selected, and that a tape motion command has been initiated.
HLDA	Hold Acknowledge. Signals the DMA that the microprocessor has relinquished control of the cache bus.
HLDR	Hold Request. Sent from the DMA to the microprocessor to request control of the cache bus.
IBG	Interblock Gap. A 0.6-inch gap between blocks of data recorded on the tape.
ICER	Correctable Error. Interface output signal. During a read/write opration, indicates the occurrence of a correctable error.
ID Burst	Identification Burst. A burst at the beginning of the tape of 1600 frpi in the P channel and erasure in all other channels to indicate a PE tape.
IDBY	Data Busy. Interface output signal. Goes true after simulated ramp delay and remains true during execution of all channels initiated by IGO.
IDENT	Identification. Interface output signal. Pulsed when read head passes BOT marker to identify a 1600 bpi (PE) tape.
IEDIT	Edit. Interface input signal. With IWRT true, causes CTU to operate in the edit mode.
IEOT	End of Tape. Interface output signal indicating that the EOT marker has been detected.
IERASE	Erase. Interface input signal specifying the erase mode of operation.
IFAD	Formatter Address. Interface input signal used in combination with ITAD0 and ITAD1 and switches S1, S2, and S3 to select the CTU.

IFBY	Formatter Busy. Interface output signal indicating that tape motion is occurring.
IFEN	Formatter Enable. Interface input signal. Enables the CTU.
IFMK	File Mark. Interface output signal. Indicates that the CTU has detected a file mark.
IFPT	File Protect. Interface output signal indicating that a reel of tape without a file protect ring is mounted on a selected CTU.
IGO	Initiate Command. Interface input signal used to latch the command specified on the command lines into the selected CTU.
IHER	Hard Error. Interface output signal used to indicate that an uncorrectable error has been detected by the CTU.
ILDP	Load Point. Interface output signal used to indicate that the BOT marker is positioned in front of the photosensor.
ILWD	Last Word. Interface input signal used during a write operation to indicate that the character to be strobed into the formatter is the last character of the record.
INTA*	Interrupt Acknowledge. Generated in the microprocessor logic and sent to the CIO's to indicate that an interrupt acknowledge cycle is in progress.
Interblock Gap	See IBG.
INTERDEN	Interface Device Enabled. Generated by PULSE2, FSEL, and ONL; when true, indicates that the device is not rewinding, is selected, and is on-line.
I/O*	Input/Output. Generated in microprocessor section to specify that an input/output operation is taking place.
IONL	On-Line. Interface output signal. Indicates that selected CTU is accessible to the host controller.
IOR*	I/O Read. Control signal used to access data from host controller when writing data in cache memory.
IOW*	Input/Output Write. Used in conjunction with DACK0* to generate WLATCH when transferring data under DMA control from cache memory to the write formatter.
ips	Inches per second. The speed at which tape is moved through the physical transport.
IRDY	Ready. Interface output signal. Indicates that CTU is on-line, not rewinding, and ready to accept a remote command.

IREV	Reverse. Interface input signal. With CTU ready and on-line, causes tape to move in the reverse direction when true and in the forward direction when false.
IREW	Rewind. Interface input signal. With CTU ready, on-line, and not at BOT, causes tape to rewind in reverse direction.
IRP, IR0-IR7	Read Data. Interface output signals that carry read data from the CTU to the host controller.
IRSTR	Read Strobe. Interface output signal. Pulses to indicate that a character is present on the controller interface.
IRWD	Rewinding. Interface output signal that indicates the tape is rewinding to beginning of tape.
IRWU	Rewind/Unload. Interface input signal. With CTU on-line, causes selected unit to go off-line, rewind to BOT marker, and then unload the tape.
ISU	Supply reel servo current. The drive signal from the DAC to the supply servo circuit.
ITAD0, ITAD1	Transport Address 0 and 1. Interface input signal used with IFAD and switches S1, S2, and S3 to select the CTU.
ITHR	Read Threshold. Generated by the DAC and used in the read circuits to set the level at which a read signal is detected.
ITU	Takeup reel servo current. The drive signal from the DAC to the takeup servo circuit.
IWFM	Write File Mark. Interface input signal. With IWRT true, causes a file mark to be written on the tape.
IWP, IW0-IW7	Write Data. Interface input signals that carry write data from the host controller to the CTU.
IWRT	Write. Interface input signal. When true, specifies the write mode, and when false, specifies the read mode.
IWSTR	Write Strobe. Interface output signal. Indicates that the character on the data lines has been recorded and the next character is needed.
KBS	Kilobytes per Second. Density of the data recorded on tape with respect to tape speed.
LASTW*	Last Word. This signal indicates the last data character to be written is present on the interface.
MEMR*	Memory Read. Three-state DMA signal used to access data from cache memory during a DMA read operation.

MEMW*	Memory Write. Three-state DMA signal used to enable the cache memory write function during a DMA write operation.
MREQ*	Memory Request. Tri-state output active low signal which indicates that the address bus holds a valid address for a memory read or write operation.
NVI*	Non-Vectored Interrupt. Generated by the analog-to-digital converter and sent to the microprocessor to request a non-vectored interrupt.
ONL	On-Line. Set by the microprocessor via the PULSE1 signal to indicate that the CTU is ready to accept commands from the host controller.
OUTLATCH0	Generated by the output status register to initiate the Formatter Busy (FBY) status signal.
PCLK	Peripheral Clock. The CPU clock signal used to clock the CIO's.
PE	Phase-Encode. The data recording format used by the CTU.
PECLK	Phase Encode Clock. Clock (22 times the data rate) that is used to synchronize the data in the formatter.
PENAB*	Phase Encode Enable. This signal enables formatter to send read strobes and data information.
Postamble	One all-ones byte and 40 all-zero bytes following a data block.
POSTERR*	Postamble Error. This signal is true when an error has been detected in the postamble.
Preamble	40 all-zero bytes followed by an all-ones byte preceding a data block.
PSEL	Parity Select. This signal gates parity channel from the read logic to the formatter.
PULSE 0	Pulse 0. This signal clocks the I/O Control register.
PULSE 1	Pulse 1. This signal sets the on-line flip-flop.
PULSE 2	Pulse 2. This signal resets the rewind flip-flop.
PULSE 3	Pulse 3. This signal sets the rewind flip-flop.
PULSE 4	Pulse 4. This signal resets the on-line flip-flop.
PULSE 6	Pulse 6. This signal resets the IGO flip-flop and the parity error flip-flop in the write data circuit after an error has been detected.
PULSE 7	Pulse 7. This signal is the dynamic RAM enable signal and is used to clock the DREQ0 flip-flop in the DMA control logic.

RAS	Row Address Strobe. Used in cache memory addressing to enable rows of data in the cache RAM's.
RDATA P, 0-7	Read Data. These signals are the nine data lines being read off tape.
RDCMD*	Read Command. Enables the outputs of the input motion commands latch, routing the motion commands to the microprocessor on the AD0-AD5 lines.
RDIN*	Read In. Generated in the microprocessor section during a CPU I/O read cycle; indicates that the CPU requests read data from the input motion commands logic, the DMA, or the analog-to-digital converter.
RDLD	Read Load. Enables the output of the read data latch in the cache read circuit.
RDROP P, 0-7*	Read Drop. This signal indicates the loss of data for a minimum of four character times. Used for block, file mark, and ID Burst detection.
Repositioning	In certain command sequences during streaming tape operation, places the tape in the correct position with respect to the record head when record velocity is attained during a subsequent command.
RES*	Reset. Input to the microprocessor. Active low signal that forces program counter to zero and initializes the CPU.
RESET	Generated in the RES* logic and sent to the DMA to clear the command, status, request, and temporary registers. DMA is in the idle state following RESET.
RLATCH	Read Latch. Generated in the DMA control logic; clocks read data into the data latches in the cache read circuit.
RDP, RD0-RD7	Read data from the cache memory RAM's.
R/W, R/W*	Read/Write. Specifies the read/write status of the CPU.
RWD	Rewind. Set by the rewind latch in the motion commands circuit to specify a rewind operation.
SCAN P, 0-7	This signal selects which data channel will be multiplexed into the formatter.
SMDH	Supply Motor Drive High. This signal is used for the supply motor drive voltage.
SMDL	Supply Motor Drive Low. This signal is used for the supply motor return and current sense.

SODD	Summation Odd. This signal indicates the parity (odd or even) of the read data.
STRBX	This signal enables read strobes and read data from the formatter. Used to disable read strobes when the postamble has been detected.
SUMH	Supply Motor High. This signal is the supply motor drive signal that directly drives the motor.
SUML	Supply Motor Low. This is the return signal from the supply motor.
TMDH	Takeup Motor Drive High. This signal is used for the takeup motor drive voltage.
TMDL	Takeup Motor Drive Low. This signal is used for the takeup motor return and current sense.
TUMH	Takeup Motor High. This signal is the takeup motor drive signal that directly drives the motor.
TUML	Takeup Motor Low. This is the return signal from the takeup motor.
V9P	Voltage 9 Positive. This signal is the positive 9-vdc signal from the power supply that is used to generate the +5-vdc signal.
V20M	Voltage 20 Minus. Negative 20-vdc drive voltage for the reel servo circuits (clockwise rotation).
V30M	Voltage 30 Minus. Negative 30-vdc drive voltage for the reel servo circuits (counterclockwise rotation).
V30P	Voltage 30 Positive. Positive 30-vdc drive voltage for the reel servo circuits (clockwise rotation).
VHMON*	Voltage High Minus On. This signal enables -30 volts to the takeup and supply motors.
VI*	Vectored Interrupt. Used by the CIO when requesting a CPU interrupt.
VIN0	Voltage Input Zero. This signal is input voltage from the EOT sensor.
VIN1	Voltage Input One. This signal is input voltage from the BOT sensor.
VIN2	Voltage Input Two. This signal is input voltage from the compliance arm transducer logic.
VIN3	Voltage Input Three. This signal is used to determine supply servo EMF and voltage.

VIN4	Voltage Input Four. This signal is used to determine takeup servo EMF and voltage.
VIN6	Voltage Input Six. This signal is used to indicate the speed at which the compliance arm changes position.
VIN7	Voltage Input Seven. This signal is used to indicate the DAC servo offset voltage.
VRCERR*	Parity Error. This signal is true when a read parity error has been detected.
W2XCLK	Write 2 Times Clock. This signal clocks the data to the write head.
WAIT*	When active (low), this signal causes the CPU to go into the wait state.
WDCLK	Word Clock. This signal is used during a cache memory write operation to clock data from the host controller onto the cache bus.
WLATCH	Write Latch. This signal is used during a physical tape write operation to clock write data from the cache bus into the write formatter.
W/R*	Generated by R/W* from the CPU; specifies the read/write status of the CPU.
WROUT*	Write Out. Generated in the microprocessor section during a CPU I/O write cycle; indicates that the CPU wants to input commands to the motion commands logic, the DMA, and the DAC.
WSTROBE	This signal is a clock that latches the write data into the formatter.
Z1A0-Z1A7, Z1B0-Z1B7, Z1C0-Z1C3, Z2A0-Z2A7, Z2B0-Z2B7, Z2C1, Z2C2, Z3A5-Z3A7, Z3B0-Z3B7, Z3C0-Z3C3	Input/output signals to/from the CIO's; used to interface with the CPU on the AD0-AD7 lines.