S-PAC Instruction Manual

1 MC

Honeywell

COMPUTER CONTROL DIVISION

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Instruction Manual

1-MC SERIES
S-PAC DIGITAL MODULES

January 10, 1966

Honeywell

COMPUTER CONTROL DIVISION

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SECTION I
INTRODUCTION

1-1 SCOPE

This instruction manual provides complete descriptive and reference material for the basic 1-MC Series of S-PAC Digital Modules of Computer Control Company, Inc. The basic series of S-PACs includes gates, flip-flops, power amplifiers, one-shots, clocks, and special-purpose PACs. Refer to table 1-1.1.

For information on auxiliary S-PAC equipment and logic application notes, refer to the Instruction Manual For Supplementary S-PAC Modules and Equipment. Supplementary equipment of Computer Control Company, Inc., includes PAC mounting assemblies (BLOCs), power supplies, analog-digital PACs, indicating decimal counting PACs, and special input-output PACs. Refer to table 1-1.2.

Computer Control Company, Inc., also has available complete instruction manuals for the 200-KC and 5-MC Series S-PAC Digital Modules.

1-2 S-PAC LINE

The S-PAC series of digital modules are standard products that provide the complete capability for building computer and data processing systems. All S-PACs use static logic and all three S-PAC frequency series (200 KC, 1 MC, and 5 MC) are mechanically and electrically compatible. Each series shares the same circuit arrangements and performs identical logic functions. They use a common system of model names, pin numbers, color coding, and connector polarization. The power supply voltages and logic levels are the same in each series.

Figure 1-2.1 shows the mechanical dimensions of a standard S-PAC. All PACs use etched printed circuits. All S-PAC components are dip-soldered onto etched circuit boards that provide maximum uniformity, ruggedness, and dimensional stability. Metal frames are added to the card to provide rigidity and to facilitate proper guidance into the mating connector. The PAC type is clearly indicated on the frame by model number and color code. All S-PACs are individually polarized by type and mating connectors can be polarized to accept only one type of S-PAC. The 34-pin connectors used are gold-plated with a spring-contact, self-wiping action.

1-3 BASIC PACS

The S-PAC series employs negative logic with the following nominal voltage levels:

Logic ONE: -6 volts
Logic ZERO: 0 volt

Table 1-1.1. Types of 1-MC S-PACs

Description		Model No.
Gate PACs	Diode PAC	DC-30
	Parallel Gate PAC	DF-30
	NAND PAC	DI-30
	Parallel NAND PAC	DJ-30
	NAND PAC	DL-30
	Gate PAC	DN-30
Flip-Flop PACs	Counter PAC	BC-30
	Gated Flip-Flop PAC	FA-30
	Basic Flip-Flop PAC	FF-30
	Multi-Purpose Flip-Flop PAC	MF-30
	Shift Register PAC	SR-30
	Universal Flip-Flop PAC	UF-30
Power Amplifier PACs	Power Amplifier PAC	PA-30
	Non-Inverting Power Amplifier PAC	PN-30
Delay Multivibrator PACs	Delay Multivibrator/Pulse Shaper PAC	DM-30
	Adjustable Delay Multivibrator PAC	DM-30A
	Delay Pulse PAC	DS-30
	Adjustable Delay Pulse PAC	DS-30A
Clock PACs	Master Clock PAC	MC-30
	Master Clock PAC (Special Precision)	MC-30X
	Multivibrator Clock PAC	MV-30
Serial Memory PACs	Serial Memory PAC	SM-30
	Serial Memory PAC (Long Line)	SM-30L
Special Purpose PACs	Octal/Decimal Decoder PAC	OD-30
	Transmission Line Driver PAC	XD-30

Table 1-1.2. Types of Supplementary S-PACS and Equipment

Description		Model No.
Input-Output PACs	Signal Adapter PACs	DI-21,31,36
	Display Driver PAC	DD-31
	Positive Logic Level Converter PAC	LC-35
	Lamp Driver PAC	LD-30
	Gate/Shaper PAC	MS-30
	Nixie Driver PAC	ND-31
	Vertical Relay PAC	RV-30
	Solenoid Driver PAC	SD-30

Table 1-1.2. Types of Supplementary S-PACS and Equipment (Cont)

Description		Model No.
	System Normalizer PAC	SN-30
	Schmitt Trigger PACs	ST-30,35
	Timing Distributor PAC	TD-30
Analog-Digital PACs	Converter Clock PAC	CA-30
	Analog Comparator PAC	CD-30
	Digital Attenuator PAC	LN-30
	Adjustable Digital Attenuator PAC	LN-30A
	Precision Digital-to-Analog Converter PAC (4 Bit)	LP-30
	Precision Digital-to-Analog Converter PAC (6 Bit)	LP-31
	Multiplexer Switch PAC	MX-30
	Operational Amplifier PAC	OA-30
	Precision Reference PAC	PR-30
	Precision Reference (Slave) PAC	PR-31
	Analog Switch PAC	SA-30
Indicating Decimal Counting Unit PACs	Counter-Indicator PAC	CI-20
	Counter-Indicator (High Level) PAC	CI-21
	Counter-Converter PAC	CP-20
	Counter-Converter (High Level) PAC	CP-21
	Indicator-Converter PAC	IP-30
	Storage Indicator PAC	SI-30
	Storage-Converter PAC	SP-30
Special Purpose PACs	Blank PACs	BP-30,31
	Electrostatic Shield PAC	ES-31
	Transistorized Unit Indicators	UI-10,30,31
	Utility PAC	UT-30
	PAC Extender	XP-30
Power Supplies	Plug-In Power Supply	PB-30
	IDCU Power Supply	PD-30
	Power Supplies (Rack Mounted)	RP-30, 31, 32, RP-31E, 32E, 33E
BLOCs	S-BLOCs	BL-30 thru 33
	Split Drawer Units	BS-34 thru 39
	Tilt Drawer Units	BT-32,33
Auxiliary Equipment	Cooling Unit	CU-30
	Jumper Lead Set	JL-30

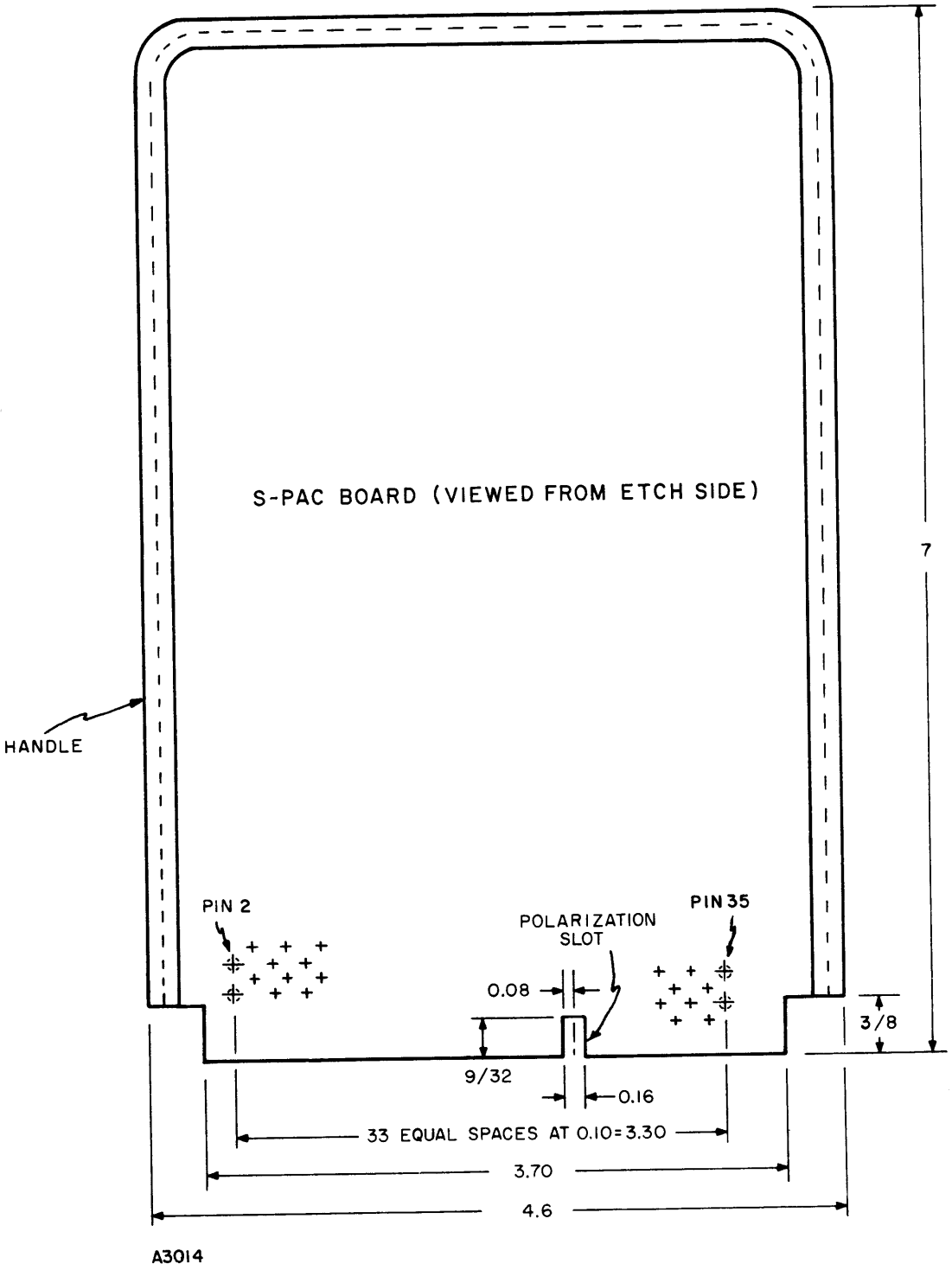


Figure 1-2.1. Standard S-PAC Mechanical Dimensions

The NAND gate configuration is the standard circuit used throughout the S-PAC line. For positive logic, this gate becomes a NOR gate.

In general, S-PACs contain two input configurations: a DC input, as in a NAND gate, and an AC input, as in complementing flip-flops. The DC input is direct-coupled and level sensitive, while the AC input is sensitive to a positive-going voltage transition. All inputs are diode buffered. When there is a node (common point of the input diodes), a gate can be expanded using a diode cluster. Refer to figure 2-5. 1 in Section II of this instruction manual.

The NAND gate consists of a multi-input diode AND gate followed by a single transistor, inverter amplifier. When all inputs are at logic ONE (or not connected), the output of the NAND gate is a logic ZERO. When an input is at ZERO, the output is at ONE. The NAND gate provides power amplification and level restoration.

The basic flip-flop circuit consists of two cross-coupled NAND gates with DC set and reset inputs and set and reset outputs. A flip-flop is considered to be in the ONE state when its SET output is a logic ONE. The quiescent or no-input signal to a DC set or reset input is a logic ONE. When a logic ZERO is applied to any DC set input, the flip-flop will assume the ONE state.

AC inputs are used on flip-flops that can perform counting and shifting functions. The AC input and its associated level control inputs form a gate where information is placed statically on the level control input and the AC input is strobed. For a common AC input with a logic ZERO on the set level control and a logic ONE on the reset level control, the flip-flop will assume the logic ONE state when the common AC input changes from a ONE to a ZERO. A ZERO is the conditioning signal on a level control input.

The activation of a flip-flop on the logic ONE to logic ZERO transition of an AC input is referred to as trailing edge triggering. Trailing edge triggering allows the output of a flip-flop to be gated with the AC input signal to allow nonambiguous sensing for the state of the flip-flop.

1-4 LOGIC SYMBOL STICKERS

To aid in the use of S-PACs, an S-PAC Logic Symbol Kit, Model SK-30 (figure 1-4. 1), is available. This kit contains symbol stickers as well as detailed technical information on individual PAC connections and applications. Using the symbol kit greatly simplifies system logic design and wiring and effectively minimizes the drafting requirements for the production of final engineering drawings. The logic symbol, applicable pin connections, and circuit identification are printed directly on each sticker. In addition, space is provided for designating the physical location of the PAC in the respective S-BLOC.

The entire kit is assembled as a booklet and includes symbol sheets and applicable instructions for use. Individual sheets of logic symbols are also available.

Figure 1-4.1. Application of S-PAC Stick-On Symbols

SECTION II
SPECIFICATIONS AND CIRCUITRY

2-1 LOGIC AND VOLTAGE LEVELS

The following specifications apply to all 1 MC gates and flip-flops. Any exceptions for other PAC types are listed in the individual specifications.

Input Logic Levels

Logic ONE: -4.5 to -8.0 V

Logic ZERO: 0.0 to -1.5 V

Output Logic Levels

Logic ONE: -6.0 to -6.6 V

Logic ZERO: 0.0 to -0.5 V

Input Pulse Specifications

To activate the AC input of any 1-MC Series S-PAC, the signal must meet the following requirements (figure 2-1.1):

Rise time (T_r) = 0.2 μsec (max)

Fall time (T_f) = 0.6 μsec (max)

Positive time (T_2) = 0.25 μsec (min)

Negative time (T_1) = 0.6 μsec (min)

Time period (T_3) = 1.0 μsec (min)

Voltage amplitude (V) = 5.5 volts (min)

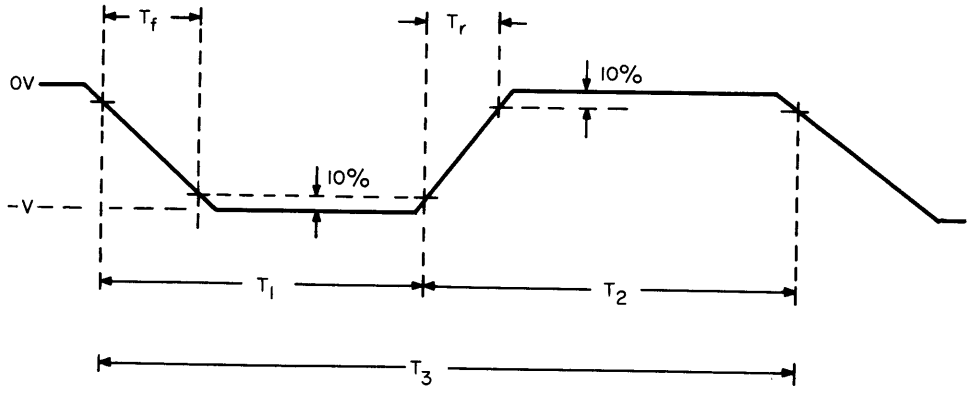


Figure 2-1.1. Input Pulse Requirements

To activate the DC input of a 1-MC Series S-PAC, the signal must meet the following requirements (figure 2-1.2):

Time at logic ZERO (T_1) = 0.25 μsec (min)

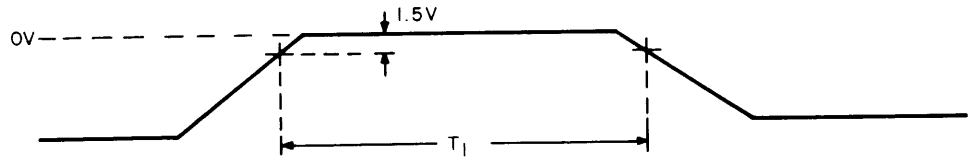
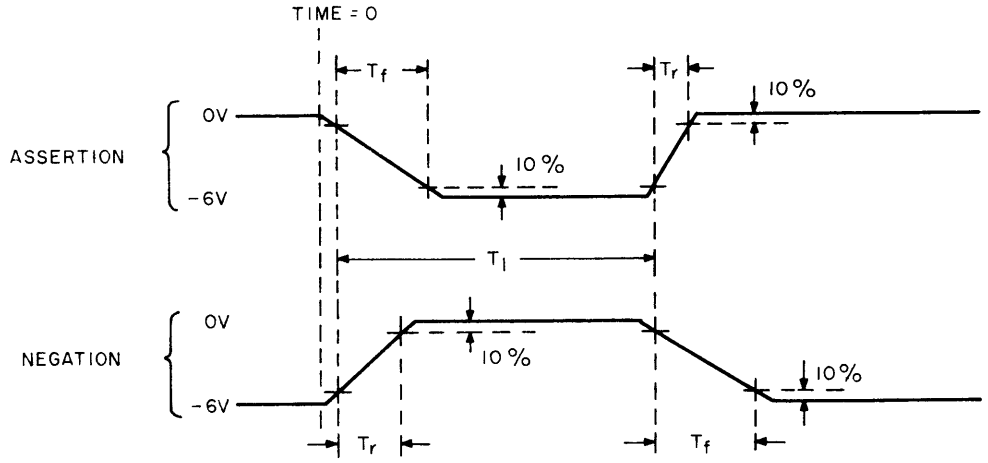


Figure 2-1.2. DC Level Requirements

Standard Output Pulse Specifications

When referring to the outputs of circuits, the terms SET and RESET denote level outputs and ASSERTION and NEGATION denote pulse outputs. S-PAC flip-flops produce level outputs; one-shots and clocks produce pulse outputs (figure 2-1.3).



(T_r) = 0.2 μsec (max)
(T_f) = 0.5 μsec (max)
(T_l) = 0.6 μsec for standard output pulses

Figure 2-1.3. ASSERTION and NEGATION Pulses

2-2 PRODUCT LINE SPECIFICATIONS

All performance specifications listed below are guaranteed minimums based on worst-case tolerances. Actual performance will invariably exceed these guaranteed minimums. The following specifications apply to all 1 MC gates and flip-flops. Any exceptions for other PAC types are listed in the individual specifications.

Frequency Range

DC to 1 MC

Noise Rejection

Ground level:	1.5 V (min)	2 V (typ)
-6 volt level:	1.5 V (min)	2 V (typ)

Temperature Range

Operating: -20°C to +55°C

Storage: -55°C to +85°C

Input Loading

The power required to drive a 1-MC NAND gate is defined as a standard 1-MC unit load (1 U load). All logic circuits are specified in terms of U loads for input loading and output drive capability. This system makes it easy to determine fan-out capability when many different types of circuits are used.

The input specifications are as follows:

NAND gate input: 1 U load

DC flip-flop input: 1 U load

Level control input: 1/2 U load

AC input: 2 U loads

Output Drive Capability

NAND gate output: 7 U loads and 400 pf stray capacitance (logical gain of 7)

Flip-flop output: 6 U loads and 400 pf stray capacitance (logical gain of 6)

Fan-In

All input gates are expandable to 10 inputs at 1 MC.

Rise Time

0.1 μsec (typ) 0.2 μsec (max)

Fall Time

The fall time is primarily dependent upon the amount of stray capacitance on the output.

0.15 μsec (typ) in a typical system

0.50 μsec (max) with maximum rated stray capacitance

Circuit Delay

The circuit delay of a NAND gate, measured at the 50-percent point (-3 volts) of the output swing, and averaged over two stages is as follows:

0.06 μsec (typ) 0.1 μsec (max)

The circuit delay of a flip-flop, measured at the 50-percent point of the voltage swing, is as follows.

0.06 μsec (typ), 0.10 μsec (max) — Set input to set output or reset input to reset output

0.15 μsec (typ), 0.25 μsec (max) — Reset input to set output or set input to reset output

Current Requirements

Current requirements are listed in the specifications for each individual PAC. The requirements are calculated on a nominal worst-case basis, in which the inputs of the

circuits are assumed to be in the condition capable of causing the maximum current drain for that particular voltage. In most cases, it is impossible for the PAC to draw the maximum rated current for each supply voltage simultaneously.

The nominal worst case is selected instead of the extreme worst case to provide a more realistic figure for power requirements and therefore drive more equipment from a power supply. Since it is inconceivable that all gates in a system would be on at the same time, the nominal worst-case calculations provide a considerable safety factor.

The current specifications include only the current used in the specific PAC and do not reflect the current going to an external load. Since the input load current is included in the specification, a simple summation of all currents for the PACs used in a system gives the total power requirements.

Power Specifications

The power dissipation for each PAC is listed in each individual PAC specification. The power dissipation specifications are calculated assuming that the circuits are in their highest dissipation state.

2-3 PRODUCT LINE FEATURES

The S-PAC series of modules provides maximum reliability and flexibility to the logic design engineer. A wide variety of versatile S-PACs is available to meet data processing applications. Long and extensive experience by Computer Control Company, Inc. in the design and application of digital and analog circuits provides the S-PAC line with the optimum use of transistors and other semiconductor elements. One basic transistor type and two basic types of diodes are used in all logic PACs. A minimum number of quality passive components and values are incorporated in the circuit design.

The metal frame on each S-PAC is color coded to identify each PAC type by model number. In addition, each PAC is provided with two polarizing slots. The mating connectors on the S-BLOC can be polarized so that only the corresponding S-PAC can be seated in any one position of the S-BLOC. Table 2-3.1 lists the color code and polarization pins for each type of S-PAC and figure 2-3.1 illustrates the S-PAC handle identification.

Table 2-3.1. S-PAC Color Code and Polarization

PAC Type	Handle Color Code		Polarization	
	Long Bar	Short Bar	Pin No.	Pin No.
BC-30	Blue	Orange	28	30
DC-30	Red	Blue	14	16
DF-30	Red	Purple	4	30
DI-30	Red	Yellow	28	32
DJ-30	Red	Brown	20	30
DL-30	Orange	Red	16	20
DM-30	Yellow	Yellow	18	20
DM-30A	Yellow	Black	18	20

Table 2-3.1. S-PAC Color Code and Polarization (Continued)

PAC Type	Handle Color Code		Polarization	
	Long Bar	Short Bar	Pin No.	Pin No.
DN-30	Red	Red	6	8
DS-30	Yellow	Green	14	32
DS-30A	Yellow	Green	14	32
FA-30	Blue	Brown	4	32
FF-30	Blue	Blue	16	18
MC-30	Brown	Brown	22	32
MC-30X	Brown	Brown	22	32
MF-30	Green	Orange	14	20
MV-30	Brown	Yellow	16	32
OD-30	Purple	Yellow	8	32
PA-30	Green	Green	20	22
PN-30	Green	Yellow	6	28
SM-30	Green	Black	20	28
SM-30L	Green	Black	20	28
SR-30	Blue	Red	4	6
UF-30	Blue	Yellow	30	32

2-4 COMPATIBILITY OF DIFFERENT FREQUENCY LINES

The three S-PAC lines (200 KC, 1 MC, and 5 MC) use the same voltage and logic levels and are electrically compatible. This compatibility permits the design of systems that use any combination of the different frequency types.

The standard NAND gate requires input power to keep the transistor OFF (condition when an input is at ground). The output is then at -6 volts. The gate does not require input power to turn the transistor ON (condition when all inputs are at -6 volts or not connected). Ratings are therefore given for an output at ground, which is the power driving state. The static current requirements to drive 200-KC, 1 MC, and 5 MC gates are 1.8, 2.4, and 3.2 milliamperes, respectively.

The unit loads for the various frequency lines (200 KC, 1 MC, and 5 MC) are noted as W, U, and V loads, respectively. A W load represents the amount of power necessary to drive a 200-KC NAND gate, a U load for a 1-MC NAND gate, and a V load for a 5-MC NAND gate. Input loading and output drive capability are rated in terms of these units. An input loading of 3 W loads corresponds to about 5.4 milliamperes of current required and an output drive capability of 2 V loads corresponds to about 6.4 milliamperes available.

Any S-PAC can drive the standard DC input of any other S-PAC directly or the standard AC input of any S-PAC in the same frequency line or in a lower frequency line. When driving the AC input of a higher frequency S-PAC from any lower frequency PAC, a gate circuit of the higher frequency must be interposed to reshape the waveform. Any of the standard NAND gate PACs may be used for this purpose.

The conversion factors for connecting S-PACs of different frequency series are listed in table 2-4.1.

EXAMPLE: Determine how many circuits rated with an input loading of 2 W loads can be driven from a circuit rated with an output drive capability of 4 U loads.

4 U = (4) (1.4) = 5.6 W capability.

Therefore

$$\frac{5.6\ W}{2\ W} = 2.8 \text{ circuits that can be driven.}$$

Table 2-4.1. Mixed Loading Conversion

Output Drive Capability		Input Loading		
		W loads	U loads	V loads
200 KC	1 W load	1.0	0.7	0.5
1 MC	1 U load	1.4	1.0	0.7
5 MC	1 V load	2.0	1.4	1.0

2-5 NAND GATE CIRCUIT ANALYSIS

The standard NAND gate in an S-PAC is a grounded-emitter, inverter amplifier with a clamped output (figure 2-5.1). All inputs are diode buffered and the output is either the voltage of a saturated transistor or the clamp voltage (-6 volts).

When all inputs are at logic ONE (-6 volts) or open, the transistor is turned on and the output is driven to ground through the saturated transistor. If an input is at ground, the transistor is turned off and the output falls to the clamp voltage of -6 volts. The operation of the NAND gate is summarized in tables 2-5.1 and 2-5.2.

The number of inputs of any gate can be expanded by tying the node of a gate to the node of a diode cluster as shown in figure 2-5.1.

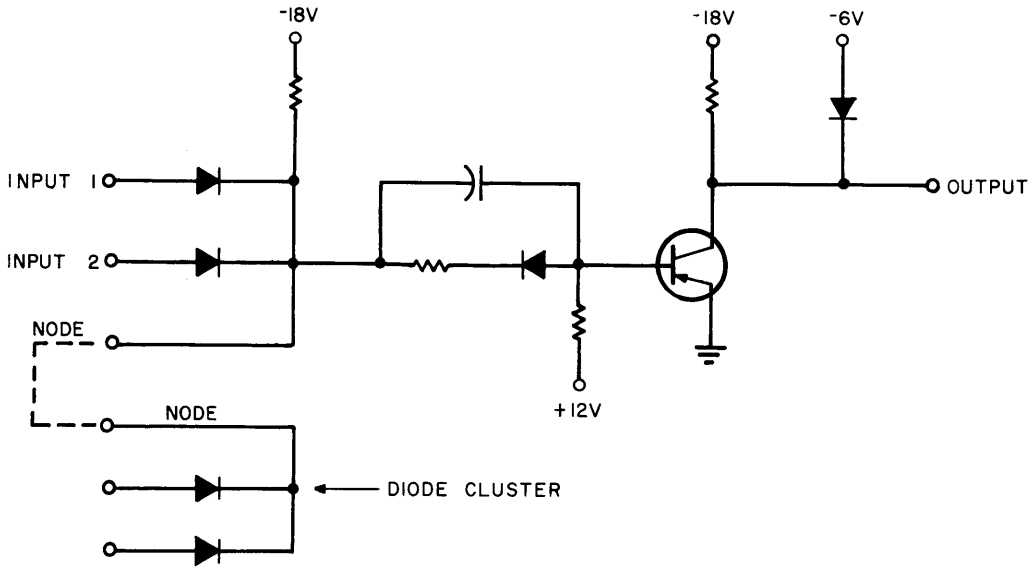


Figure 2-5.1. NAND Gate

Table 2-5.1. Voltage Truth Table

Input 1	Input 2	Output
Ground	Ground	-6 V
Ground	-6 V	-6 V
-6 V	Ground	-6 V
-6 V	-6 V	Ground

Table 2-5.2. Logic Truth Table

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Two NAND gates can be wired back-to-back to form a SET-RESET flip-flop as shown in figure 2-5.2.

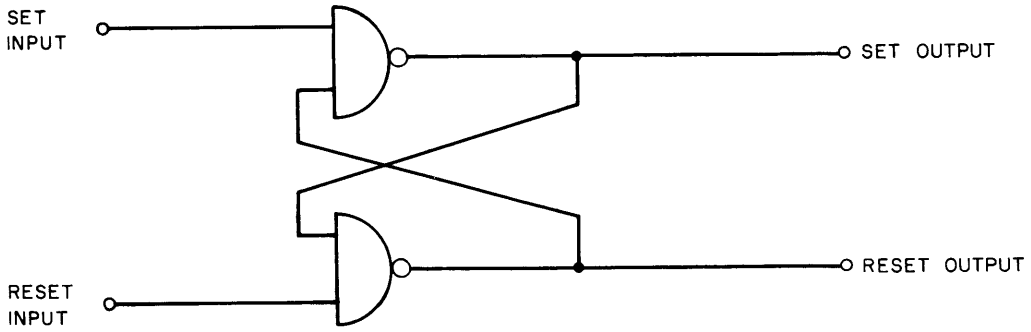


Figure 2-5.2. Flip-Flop from NAND Gates

2-6 PEDESTAL GATE CIRCUIT ANALYSIS

The pedestal gate, which is used on flip-flops with counting and shifting capabilities, is an AC-coupled, voltage-transition sensitive gate. The single-pedestal gate has an AC input and a level control input as shown in figure 2-6.1. If the level control is at ground when the AC input undergoes a positive voltage transition, the output transistor is driven off (if not already in the off state) and the output becomes -6 volts. If the level control is at -6 volts when the AC input goes positive, the output does not change state.

When the level control is at ground, point C is clamped at ground. When point A drops to -6 volts from ground, diode CR1 opens. Point B charges exponentially toward -18 volts with a time constant R_1C_1. When the voltage at point B reaches -6 volts, diode CR1 conducts and clamps point B to -6 volts, which is the potential of point A. There is then a 6-volt charge across capacitor C1.

When point A returns to ground with a fast rise time, point C rapidly becomes +6 volts and the charge of capacitor C1 is transferred into the saturated transistor to turn it off rapidly (figure 2-6.2). Point C then discharges exponentially toward -18 volts with a time constant R_2C_1 and becomes clamped to the level control voltage.

If the level control is held at -6 volts, the function of turning off the transistor is inhibited. In this case, point C is clamped to -6 volts. On the positive 6-volt transition at point A, point C rapidly becomes ground, which is not enough to turn off the transistor.

In summary, the circuit (figure 2-6.3) follows rules a and b.

a. To turn off the transistor, point B must be at -6 volts and point C must be at ground prior to the positive transition of the AC input; that is, point A. To insure that point B is -6 volts prior to the positive transition at point A, point A must be -6 volts for a designated time. This time is dictated by the time constant R_1C_1 and the action of the potential at point B heading for -18 volts but clamping at -6 volts, and must be a minimum of 0.4 microsecond.

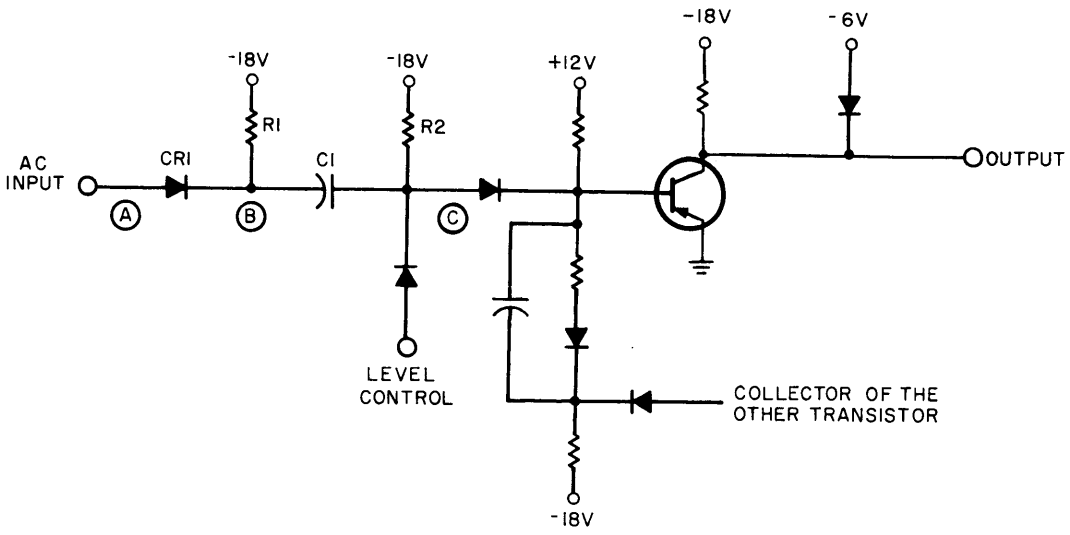


Figure 2-6.1. Single Pedestal Gate

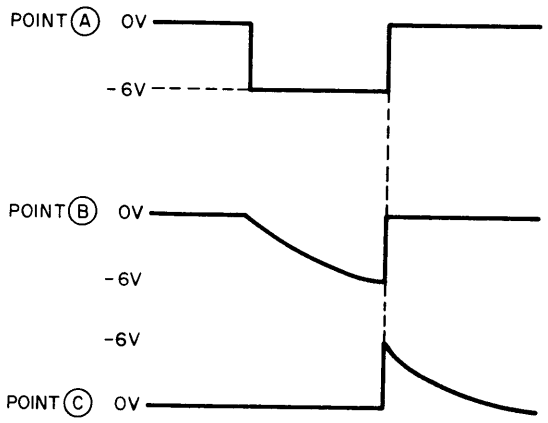


Figure 2-6.2. Waveforms for Transistor Turnoff

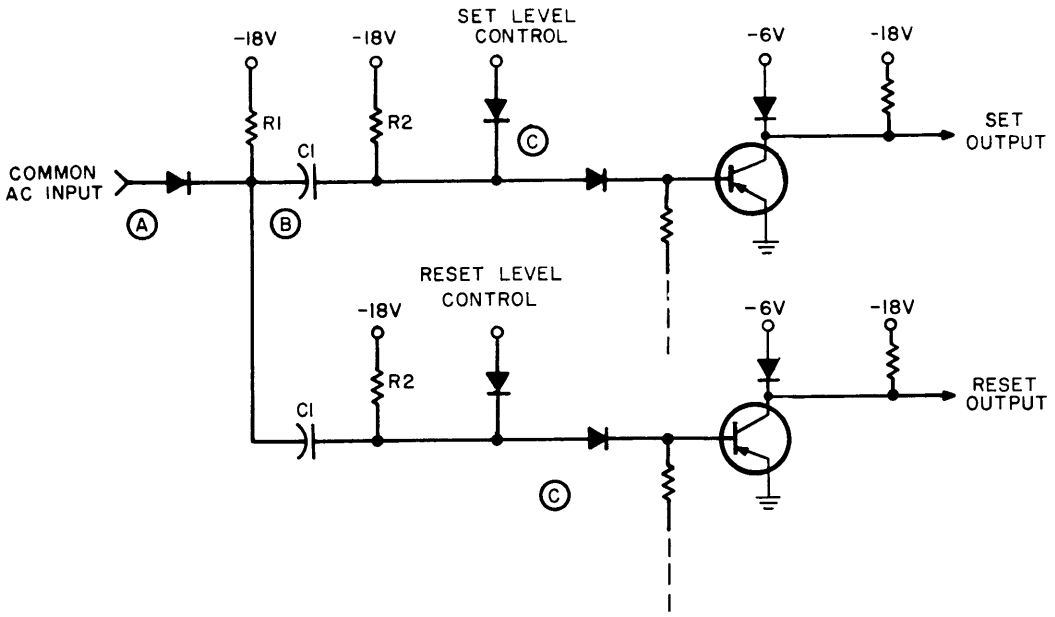


Figure 2-6.3. Double Pedestal Gate

b. To inhibit turning off the transistor, point C must be at -6 volts prior to the positive transition of the AC input; that is, point A. In addition, the amplitude of the positive transition should not exceed 6 volts.

Single pedestal gates are found on the UF-30 and FA-30 PACs as AC set and AC reset inputs. Double pedestal gates are found on the BC-30, MF-30, SR-30, and UF-30 PACs.

In double pedestal circuits the set and reset level controls perform the function of steering the AC input signal to the proper side of the flip-flop. Normally, one level control input is at 0 volt and the other is -6 volts. The level control at 0 volt must conform to rule a and the level control at -6 volts must conform to rule b.

Double pedestal gates differ from single pedestal gates because, to fulfill rule a, the AC input must be negative for a longer period to allow point B to charge to -6 volts. This is necessary because the time constant $R_1 \times 2C_1$ is twice as large as the single pedestal gate time constant.

There are two modes of operation with pedestal gates: pulse mode and step mode (figures 2-6.5 and 2-6.6). The distinction between the two modes is based upon the time necessary to insure that a level control is able to inhibit a flip-flop from changing state when the AC input goes positive. In the case of a double pedestal gate, usually one level control tries to inhibit while the other level control tries to enable, thereby placing the flip-flop in a known state.

The pulse mode of operation is defined as the condition when a level control switches negative while the AC input signal is positive (ground). Point C (figure 2-6.4) can start toward -6 volts with a time constant R_2C_1. If the AC input should go negative before point C has reached -6 volts, the AC input will pull point C down with it. In this mode of

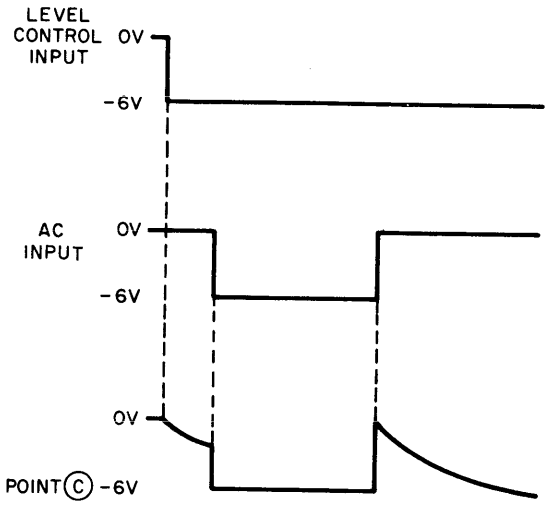


Figure 2-6.4. Waveforms to Inhibit Transistor Turnoff

operation, the AC input signal must remain negative for at least 0.6 microsecond (0.4 microsecond for a single-pedestal gate) prior to a positive transition. The pulse mode of operation is inherent in counter and shift registers when there are no intervening stages between flip-flops. Under no conditions can the negative setup time be less. An example of pulse mode operation in a BC-30 counter PAC is shown in b of figure 2-6.5. The opposite level control is shown enabling while the inhibiting level control is dropping to -6 volts.

The step mode of operation is defined as the condition when a level control switches negative while the AC input signal is negative. Point C (figure 2-6.4) must start toward -6 volts, but the AC input does not help it to go negative. The time constant R_2C_1 determines how long a time is necessary before the AC input can go positive and not cause incorrect operation of the flip-flop. For this mode of operation, the AC input must remain negative for 1.4 microseconds after the level control switches negative. The step mode of operation is encountered when systems are run asynchronously. In b of figure 2-6.6 (the step mode operation), one level control is shown enabling while the inhibiting level control is dropping to -6 volts.

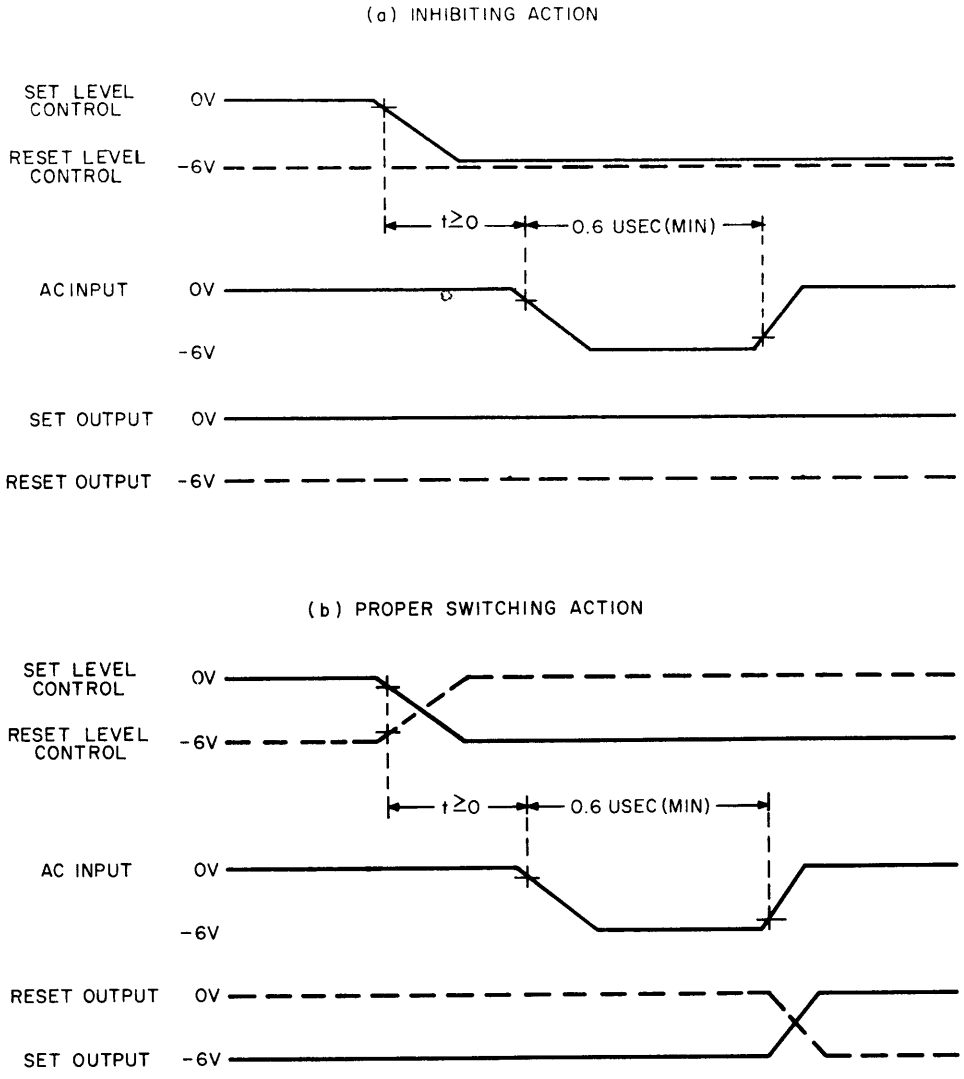


Figure 2-6.5. Pulse Mode Timing

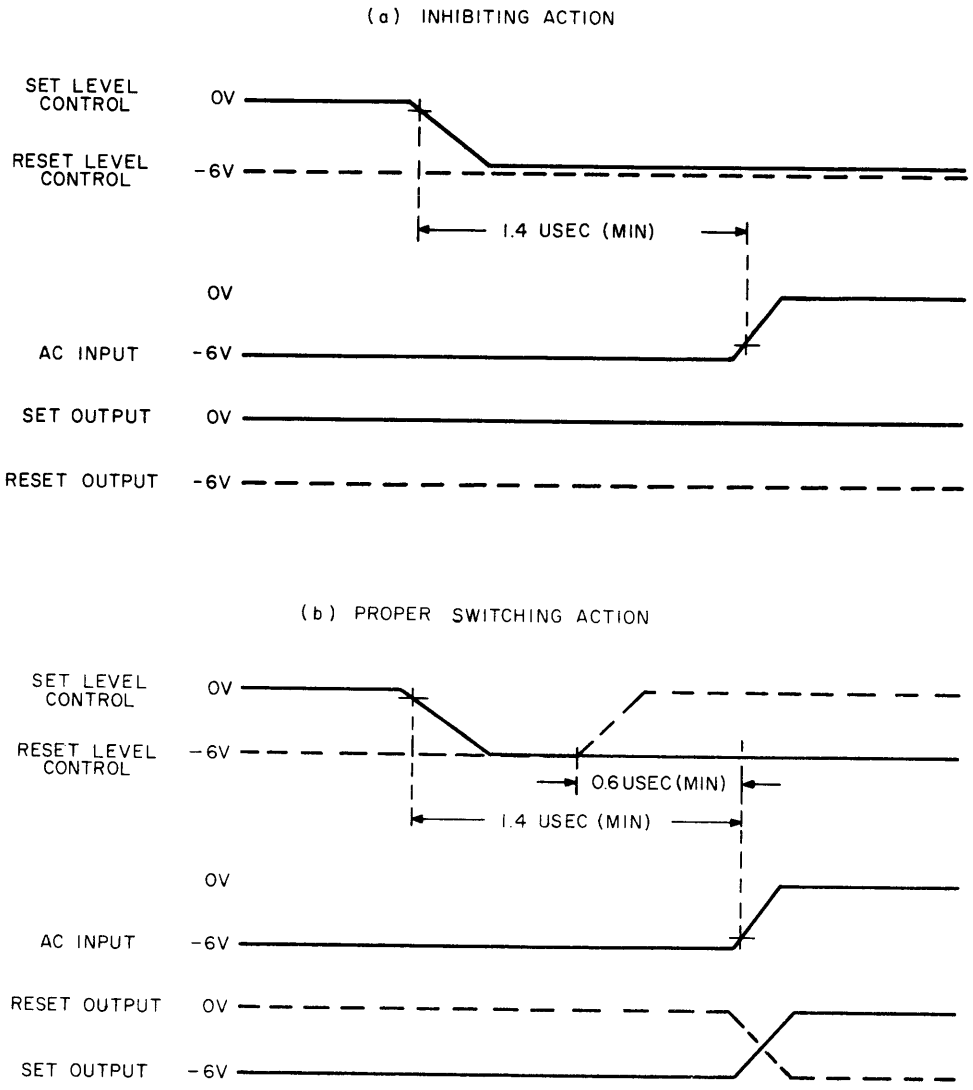


Figure 2-6.6. Step Mode Timing

SECTION III
DESCRIPTIONS OF S-PAC DIGITAL MODULES

3-1 COUNTER PAC, MODEL BC-30

GENERAL DESCRIPTION

The Counter PAC, Model BC-30, contains four independent, 1-MC counter stages which can be wired for binary or binary-coded-decimal (BCD) operation. Internally provided gating permits 8421 BCD counting as well as divide-by-six and other feedback counting modes (figures 3-1.1 through 3-1.3). Parallel drop-in to the counter is possible in both modes. The BC-30 (figure 3-1.4) can be used to implement up-down counters, instantaneous carry counters, etc., by the use of external S-PAC logic. The individual BC-30 flip-flops can also be used as independent complementing flip-flops.

Each stage has a complement input that employs either leading- or trailing-edge triggering. Trailing-edge triggering allows the counter output to be gated with a count signal pulse without the use of delay circuits or two-phase clocks.

CIRCUIT FUNCTION

The basic flip-flop circuit (figure 3-1.5) consists of two cross-coupled NAND gates. One DC set input plus node is provided for each flip-flop. When reset logic is desired, diode clusters may be wired to the reset node.

Common Reset. A 1- μsec positive pulse applied to the common reset input clears (resets) the four counter stages simultaneously.

Complement Input. The complement input is an AC-coupled input sensitive to positive steps. For trailing-edge counting or complementing, negative signals with a minimum duration of 0.6 μsec should be used. For leading-edge triggering, positive signals with a minimum durationof 0.25 μsec are needed, with the requirement that the positive signals represent a maximum duty factor of 40 percent at 1 MC. At any count rate and in any mode, a 0.6- μsec minimum negative input pulse is required for proper counter operation.

In general, only one logic operation can be performed on a BC-30 in any 1- μsec interval. An exception is the DC set and reset inputs, which can be operated twice in a 1- μsec interval.

Gated Complement Input. The second stage of the BC-30 has a gated complement input for use in BCD and binary counters. When either is at ONE (-6 V), or open, a positive transition at the other input produces the same effect as a simple complement input. Thus, either diode can be used as a simple complement input. When one input is already at ground level, a positive transition on the other input has no effect. In the BCD mode, this gate inhibits the carry into the second stage onthe tenth count.

Gated AC Reset. The fourth stage of the counter is provided with a gated AC reset input. A positive transition applied to either diode when the counter stage is in the set condition resets the stage. In the BCD mode, this gate resets the fourth stage onthe count of 10.

NOTE

In all applications of the BC-30, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

DC inputs: 1 unit load each

Common reset: 4 unit loads each

Complement inputs: 2 unit loads each

AC reset input: 2 unit loads each

Input Waveform Requirements

Common reset: 1 μsec at logic ZERO

Circuit Delay

0.25 μsec (max propagation time)

0.15 μsec (typ propagation time)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Total Power

1.8 watts

Polarization

Pins 28 and 30

Timing

See figures 3-1.1 through 3-1.3

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V	108 ma	
-6 V	46 ma	(reverse current into supply)
+12 V	5 ma	

Handle Color Code

Long: Blue

Short: Orange

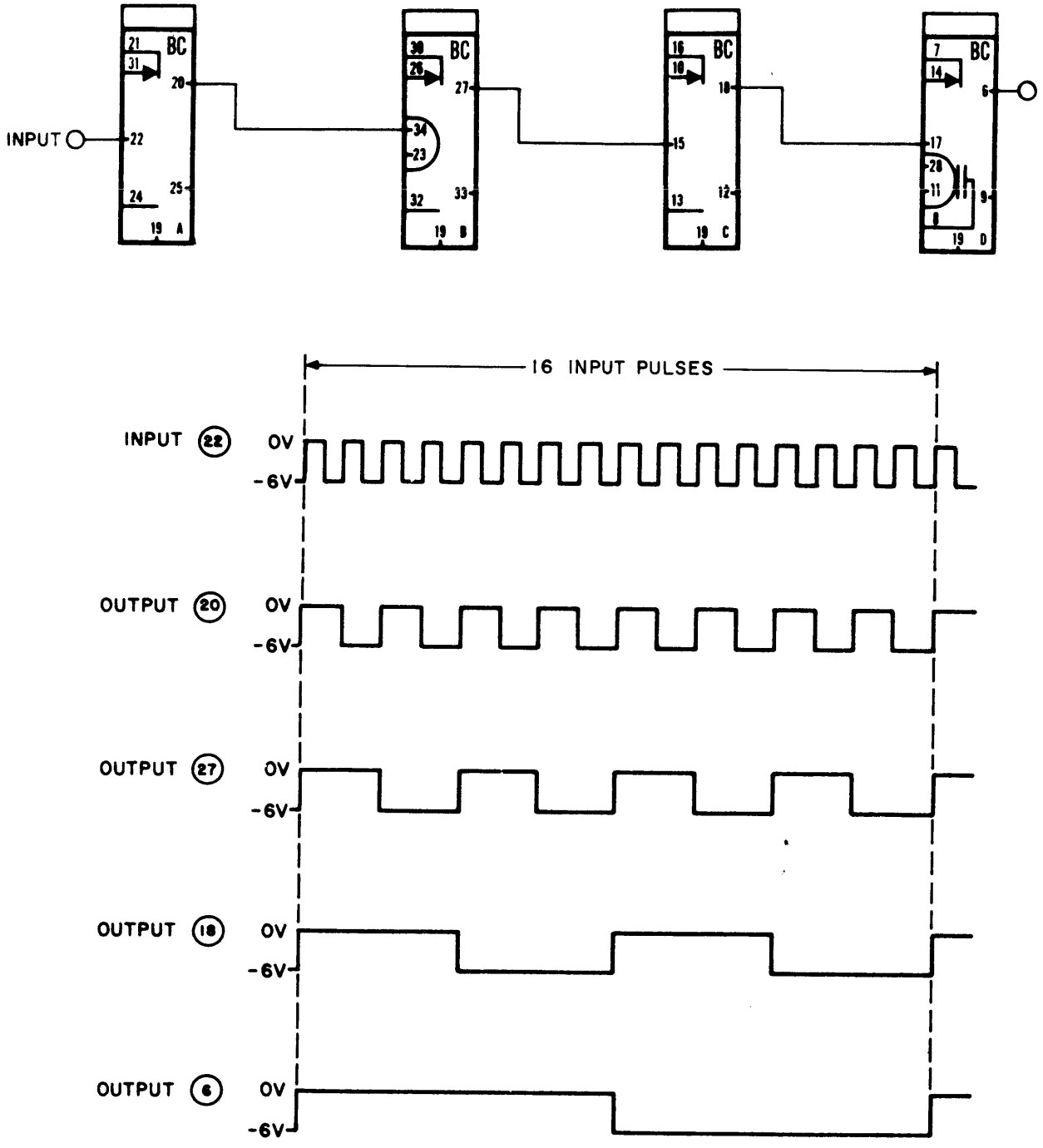


Figure 3-1.1. Binary Count Mode

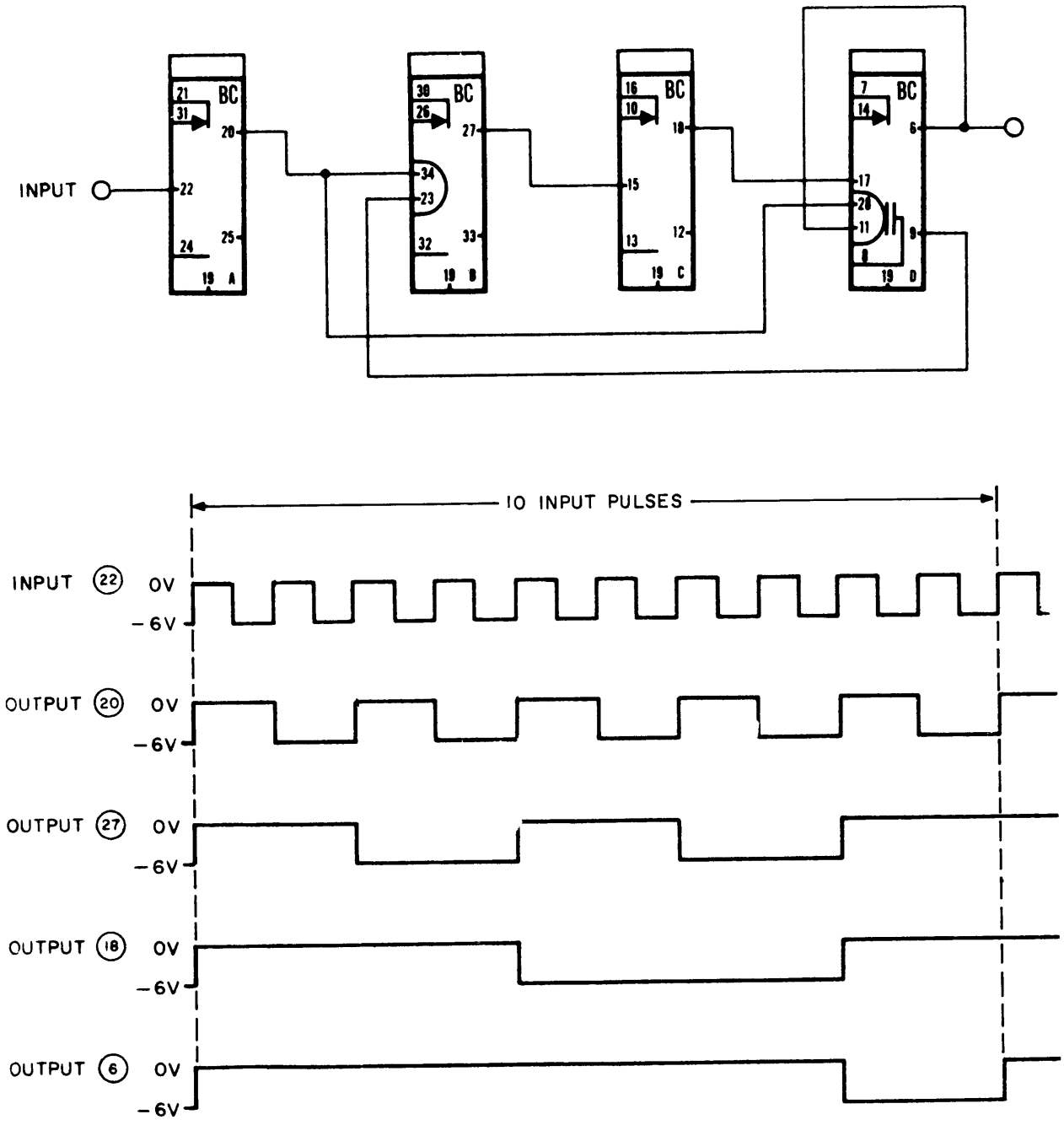


Figure 3-1.2. 8421 BCD Count Mode

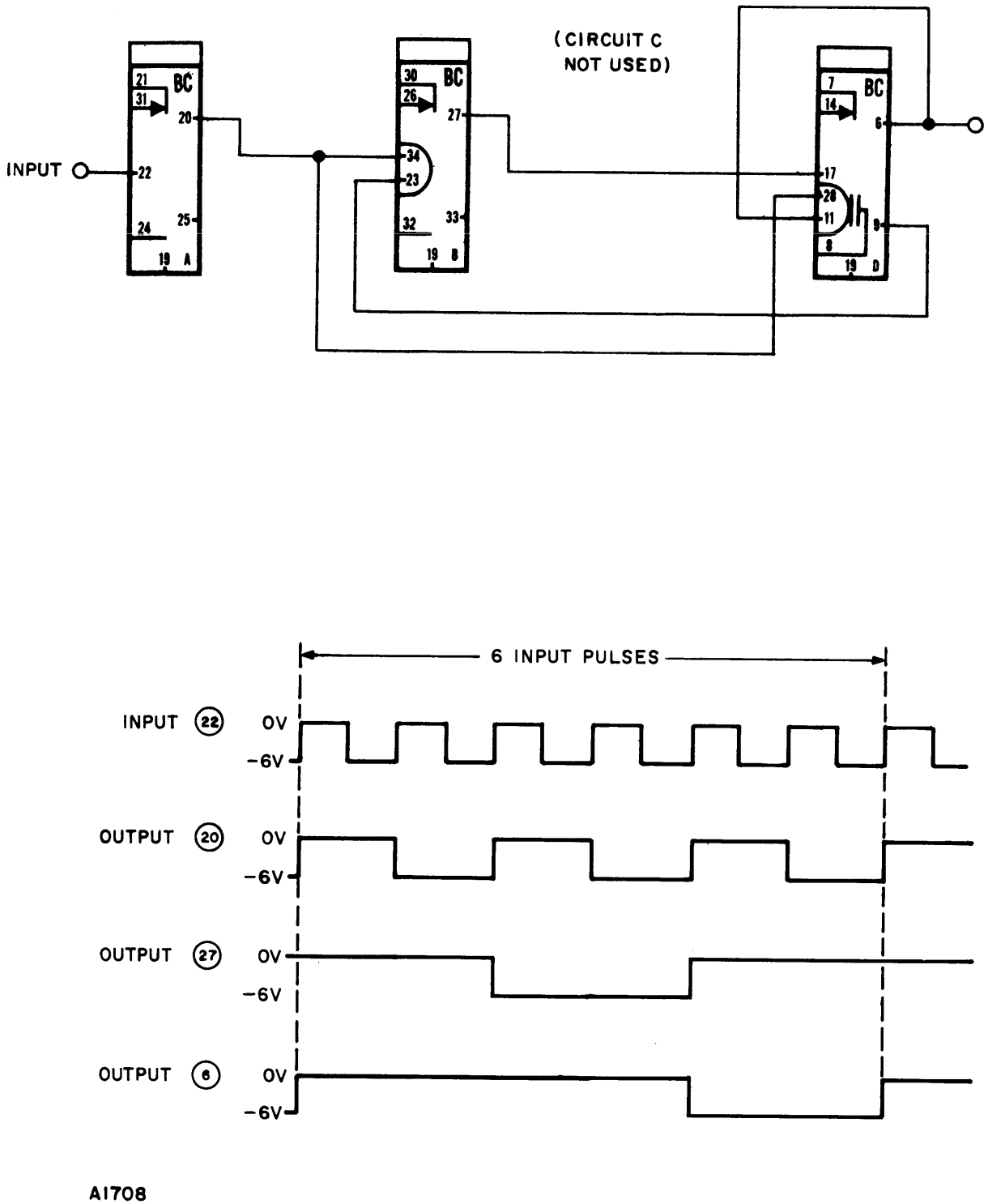


Figure 3-1.3. Divide-by-Six Mode

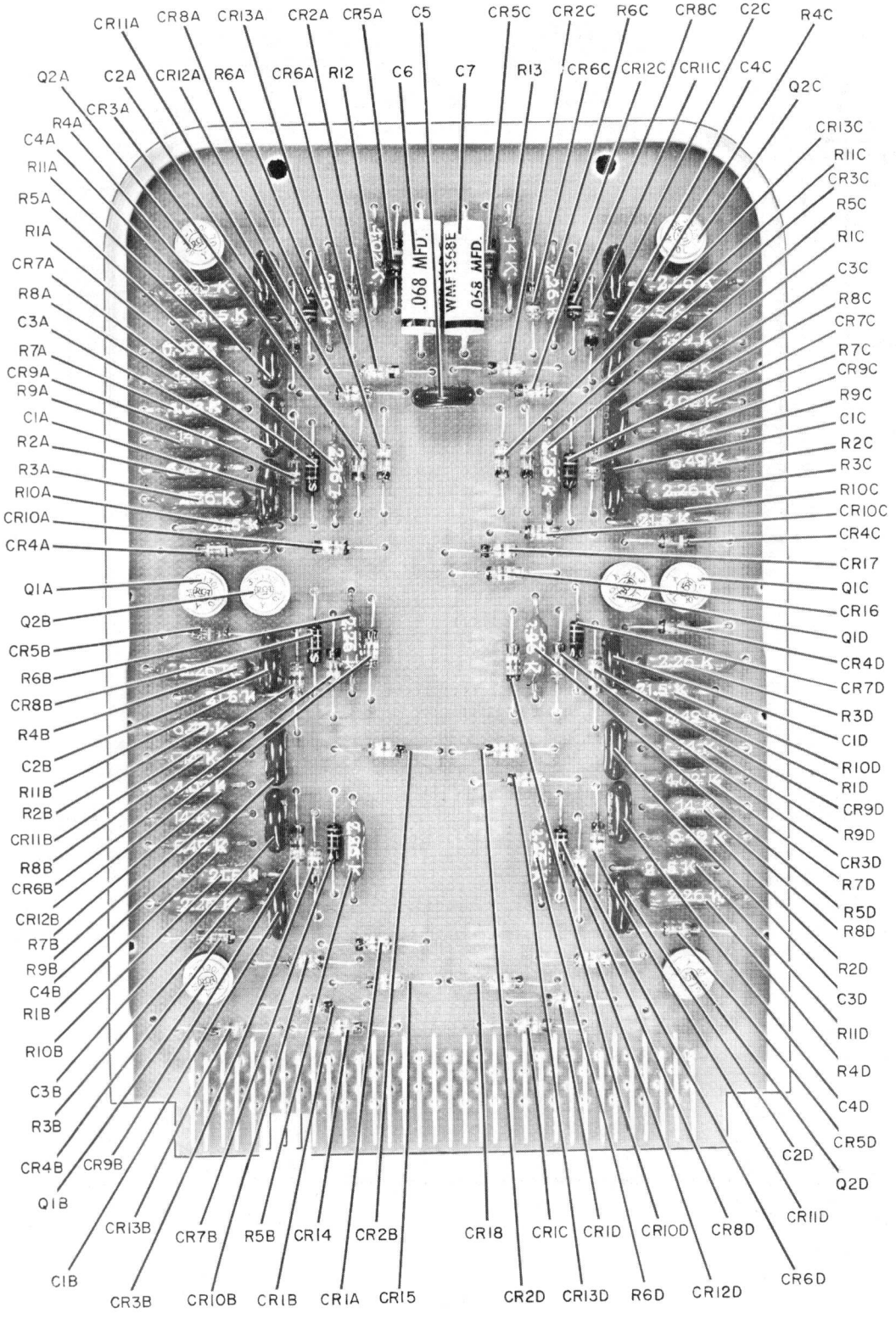
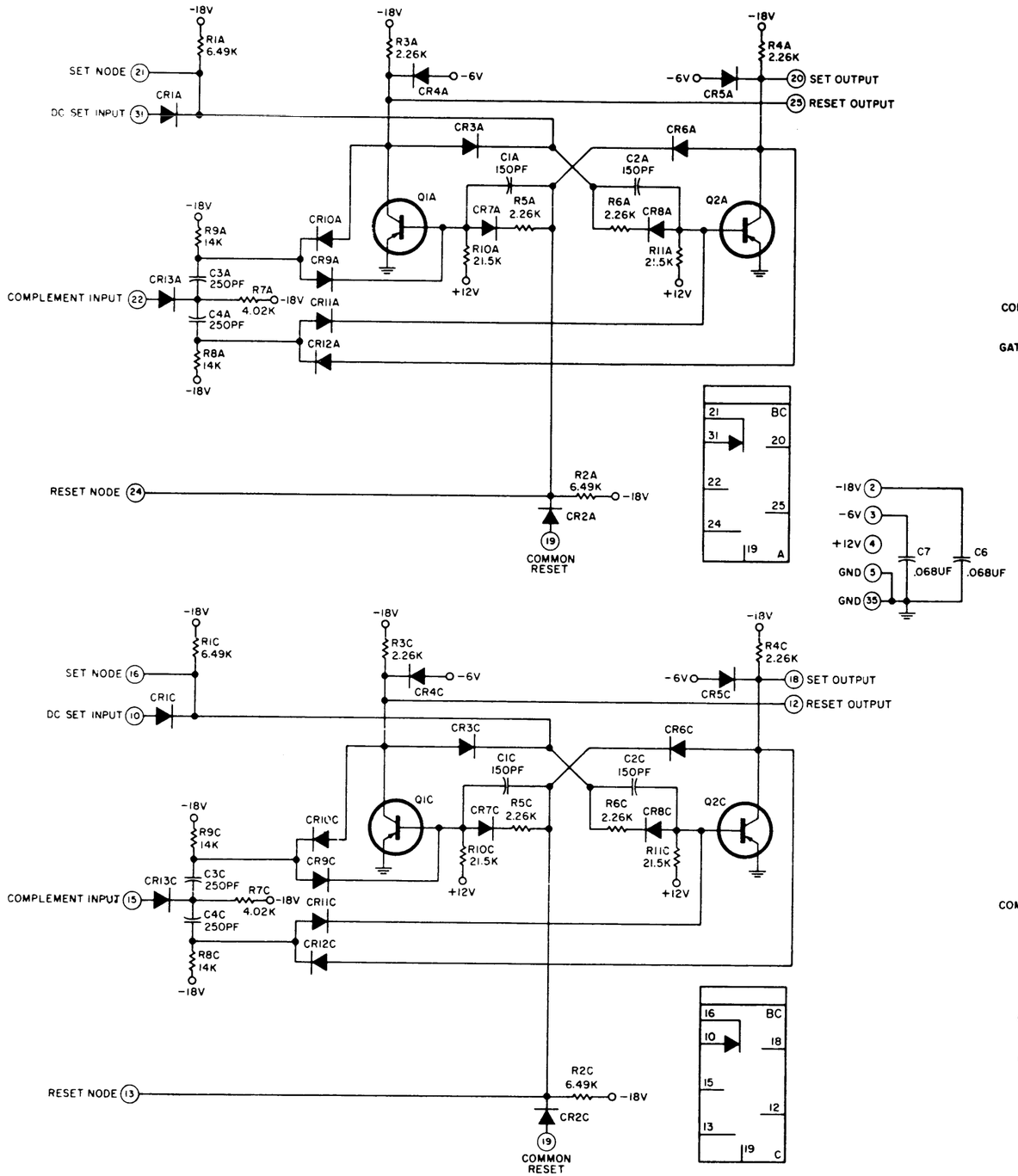
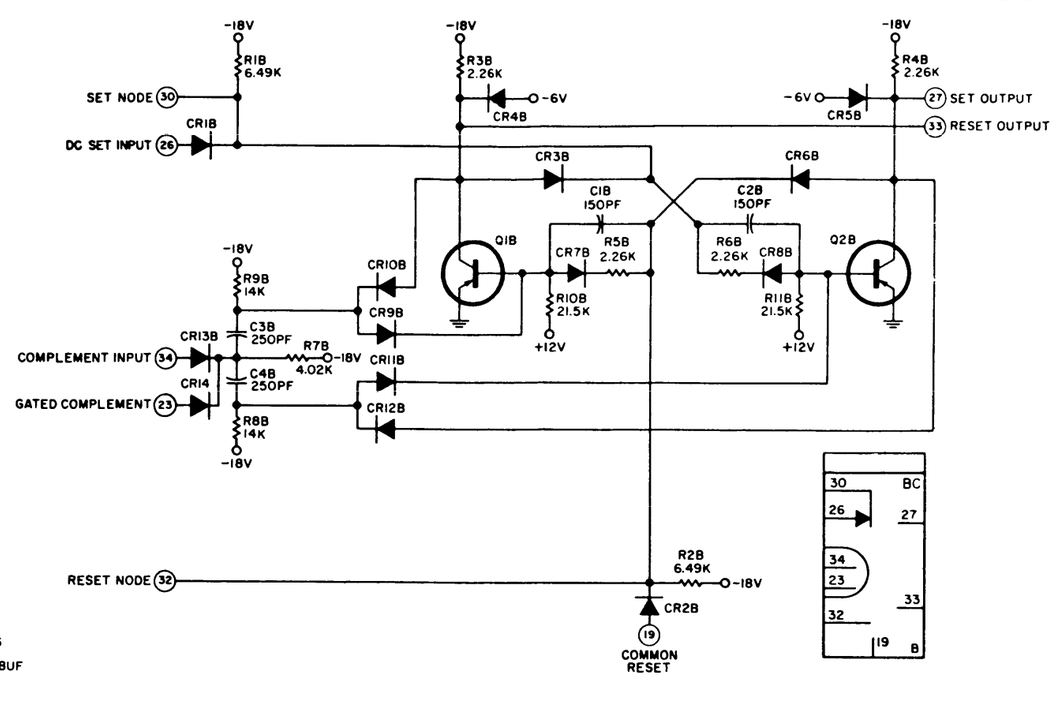


Figure 3-1.4. Counter PAC, Model BC-30, Parts Location





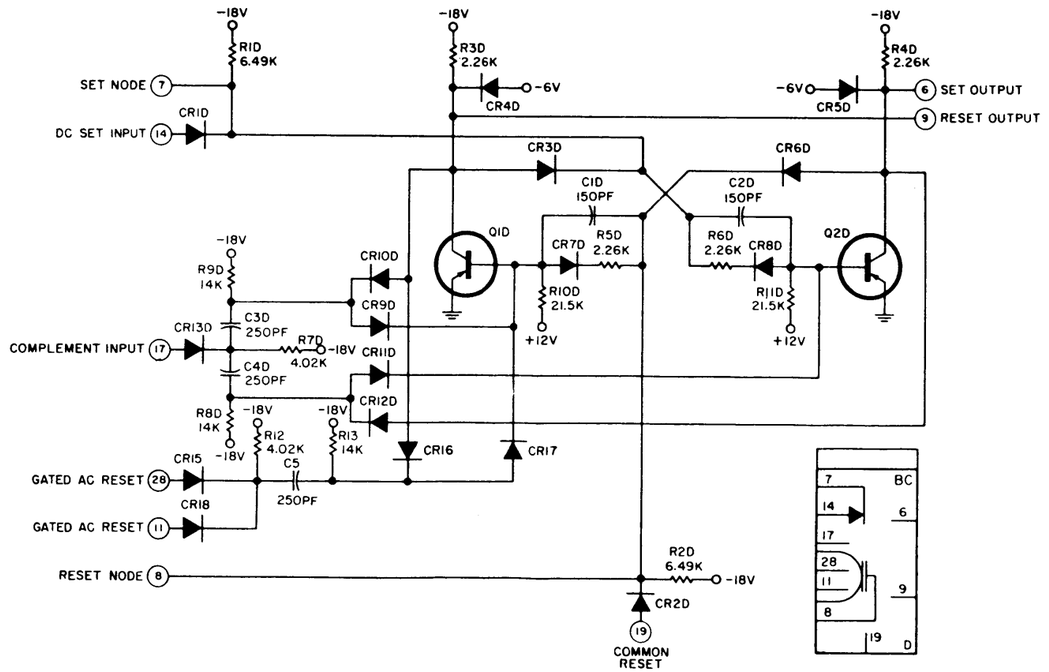


Figure 3-1.5. Counter PAC, Model BC-30, Schematic and Logic Diagram

3-2 DIODE PAC, MODEL DC-30

GENERAL DESCRIPTION

The Diode PAC, Model DC-30 (figure 3-2.1), contains one 2-input NAND gate, five 3-diode clusters, and two 2-diode clusters. The DC-30 NAND gate input can be expanded by adding the diode clusters or the diode clusters can be used to expand the inputs to other S-PAC circuits.

CIRCUIT FUNCTION

The DC-30 NAND gate (figure 3-2.2) consists of a 2-input diode gate followed by a transistor inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to 0 volt. When an input goes to 0 volt, the transistor is turned off and the output falls to the clamp voltage of -6 volts.

The diode clusters can be wired to the node input of any S-PAC for expansion of its inputs up to a maximum of 10. Care should be taken to insure that diode cluster connections are made to local S-PACs and that the interconnecting leads are not cabled. The recommended maximum lead length is 1-1/2 feet.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)

0.1 μsec (max)

0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

0.2 watts

Polarization

Pins 14 and 16

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V	11 ma
- 6 V	6 ma (reverse current into supply)
+12 V	0.7 ma

Handle Color Code

Long: Red

Short: Blue

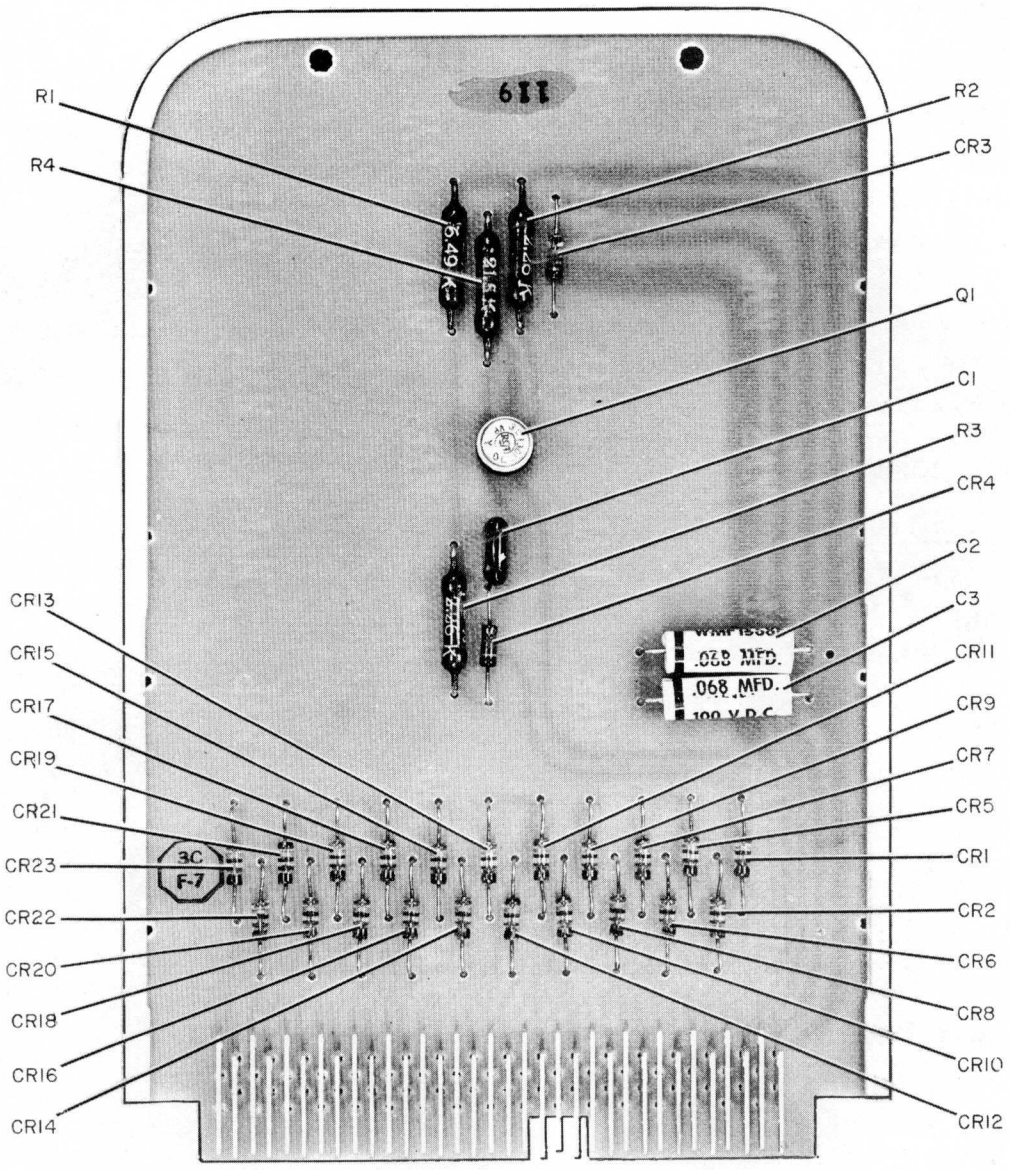


Figure 3-2.1. Diode PAC, Model DC-30, Parts Location

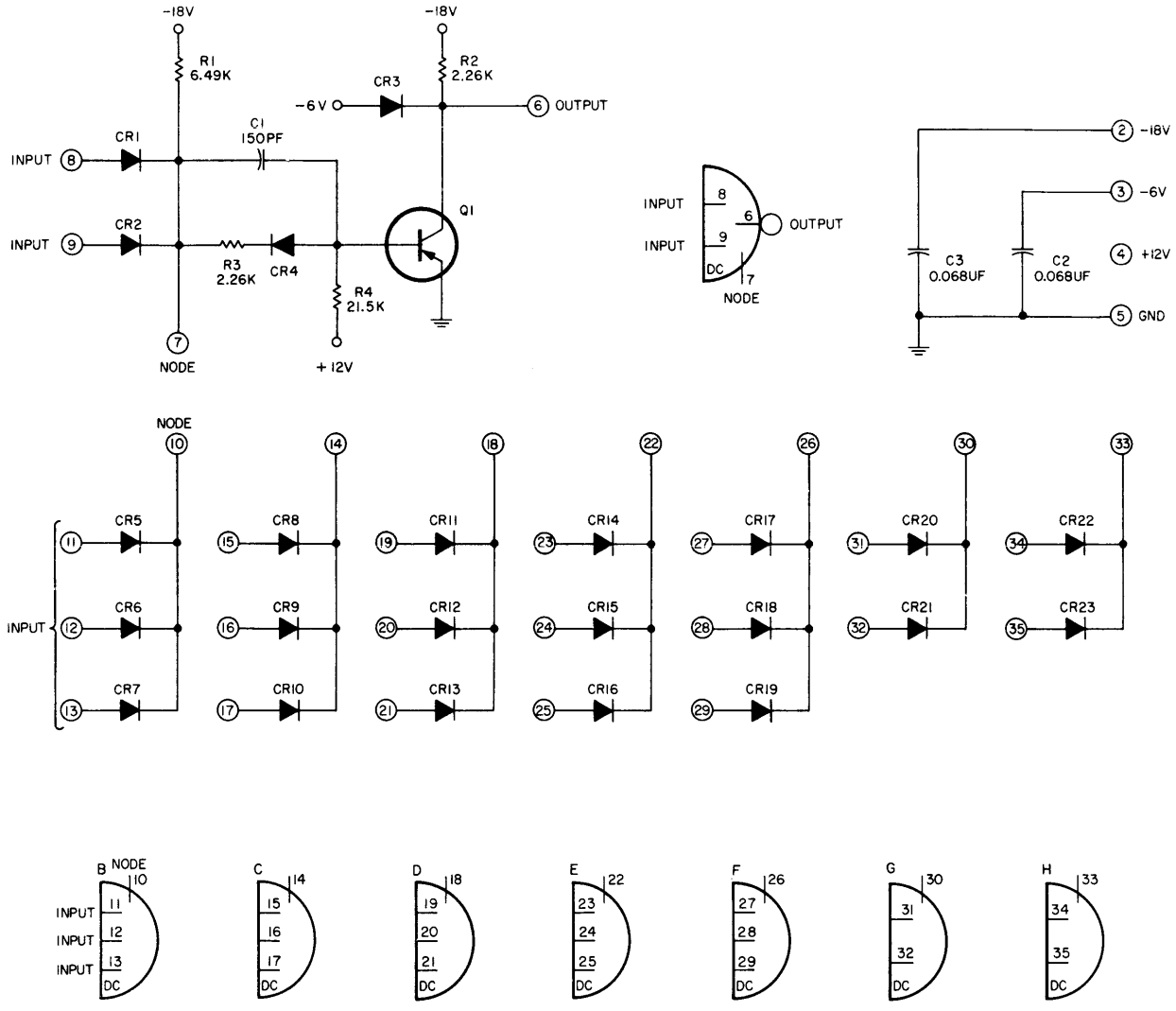


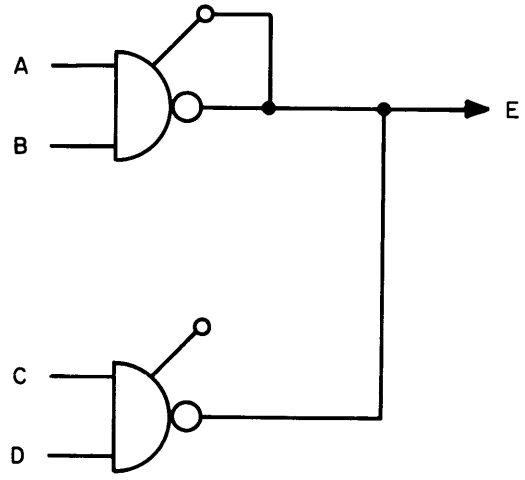
Figure 3-2.2. Diode PAC, Model DC-30, Schematic and Logic Diagram

3-3 PARALLEL GATE PAC, MODEL DF-30

GENERAL DESCRIPTION

The Parallel Gate PAC, Model DF-30 (figure 3-3.1), contains four 2-input NAND gates, one 3-diode cluster, and two 2-diode clusters. The circuits allow the connection of NAND gates in parallel without decreasing the output drive capability (fanout). The diode clusters can be used to expand the number of inputs to the NAND gates and to other S-PACs. The gates operate with levels, pulses, or with a combination of both.

NAND gates with parallel collectors can perform logic functions as shown in the following illustration.

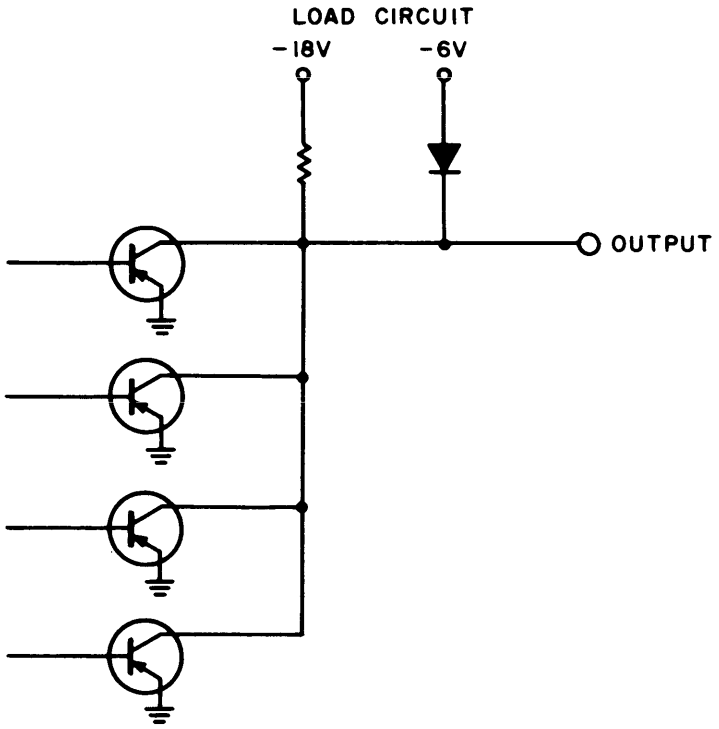


$$E = \overline{AB + CD} = (\overline{A}\overline{B})\cdot(\overline{C}\overline{D})$$

At the point where the outputs are tied together, an OR operation with logic ZEROs (AND operation with logic ONEs) is performed.

CIRCUIT FUNCTION

The DF-30 (figure 3-3.2) contains four 2-input NAND gates with separate collector load circuits. These load circuits consist of a resistor to the -18 volt supply and a clamp diode to the -6 volt supply. Each collector load can be jumpered to a corresponding gate circuit to form a standard NAND gate; however, a single load circuit can be tied to the output of several parallel-connected gate circuits without affecting the fanout. If the inputs are such that one or more transistors are conducting, the output will be at 0 volt. The maximum drive capability with up to 10 collector outputs jumpered in parallel is 7 unit loads. The following illustration shows all DF-30 gates on a PAC tied in parallel.



Model DF-30, Parallel Gate Configuration

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)

0.1 μsec (max)

0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

0.7 watts

Polarization

Pins 4 and 30

Frequency of Operation

DC to 1 MC (max)

Number of Outputs in Parallel

Limited only by total fall time acceptable

Fall time increases 0.015 μsec per parallel DF-30.

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V	40 ma
-6 V	21 ma (reverse current into supply)
+12 V	3 ma

Handle Color Code

Long: Red

Short: Purple

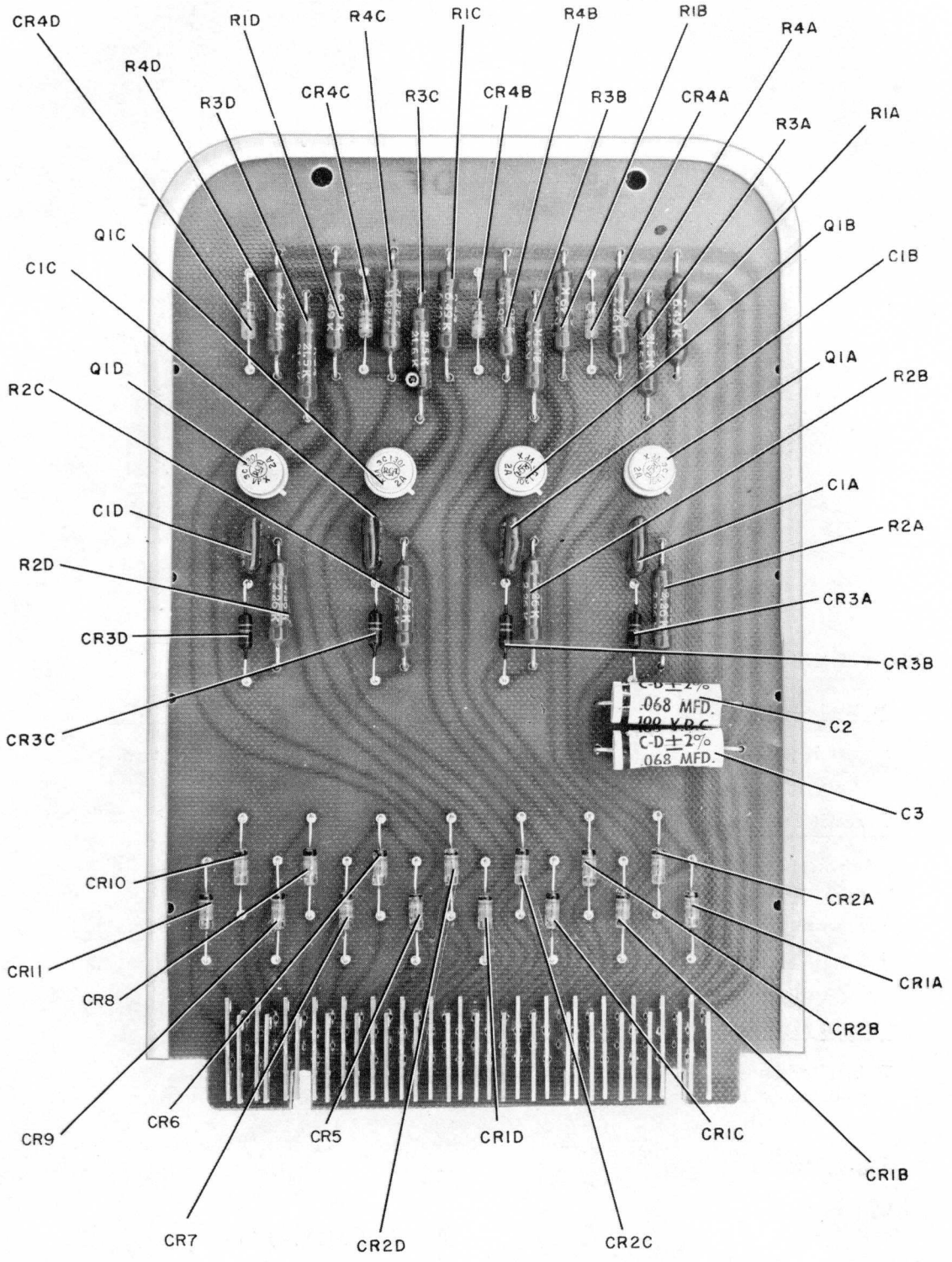


Figure 3-3.1. Parallel Gate PAC, Model DF-30, Parts Location

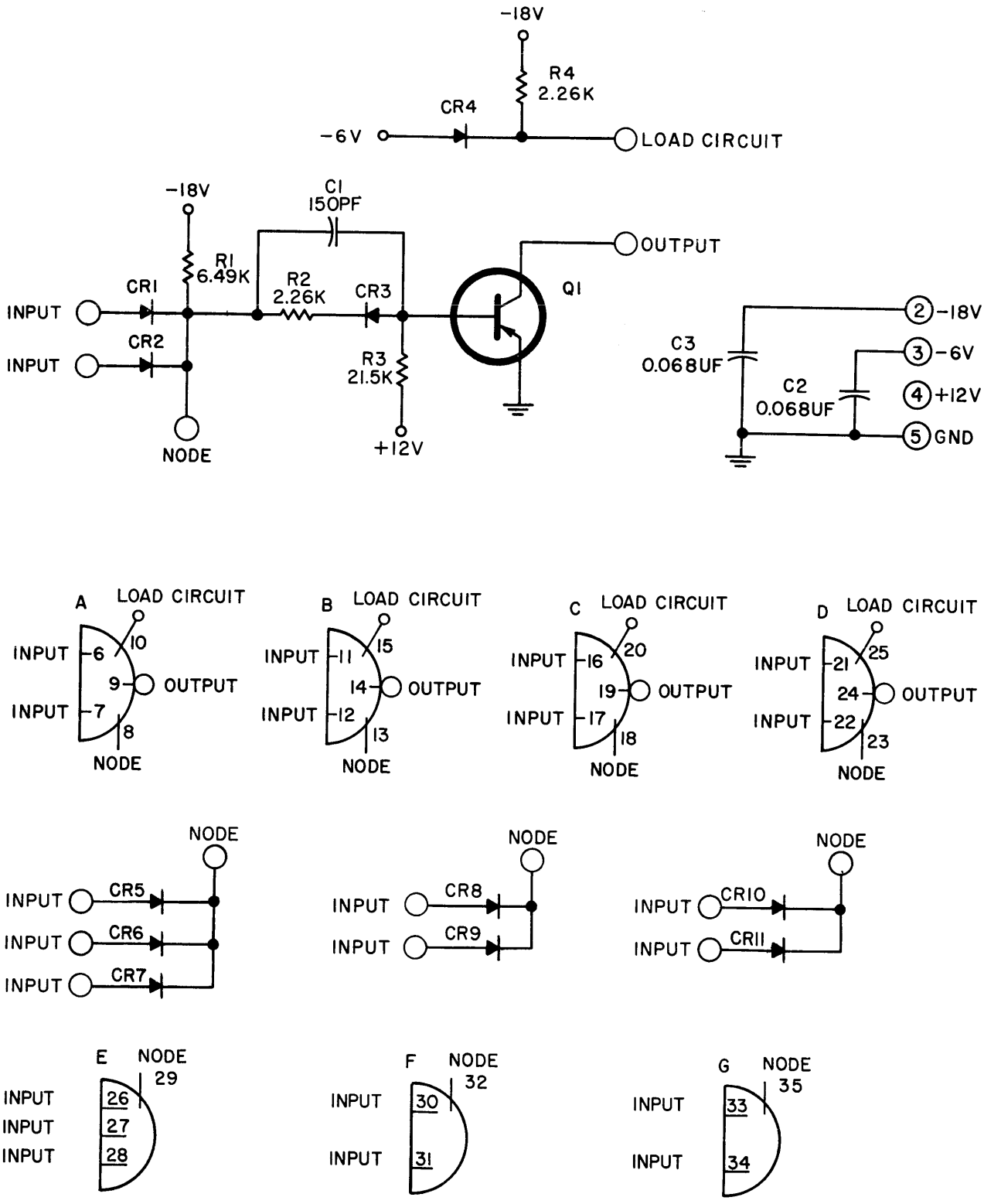


Figure 3-3.2. Parallel Gate PAC,
Model DF-30, Schematic and Logic Diagram

3-4 NAND PAC, MODEL DI-30

GENERAL DESCRIPTION

The NAND PAC, Model DI-30 (figures 3-4.1 and 3-4.2), contains eight 2-input NAND gates. These gates are expandable up to a maximum of 10 inputs by connecting diode clusters contained in the DC or DN S-PACs. Five gates have a node input for expansion. The remaining three gates can be expanded by using one of their diode inputs as a node. (When used, the noise margins on expanded inputs are reduced by 0.3 volt.)

Each NAND gate performs the NAND function for negative voltage logic (ONE = -6 V) or the NOR function for positive voltage logic (ONE = 0 V). The gates operate on levels, pulses, or with combinations of both.

Two DI-30 NAND gates form a flip-flop when their inputs and outputs are cross-coupled.

CIRCUIT FUNCTION

Each DI-30 circuit (figure 3-4.3) consists of a two-input diode gate followed by a transistor inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to 0 volt. When an input goes to ZERO (0 V), the transistor is turned off and the output falls to the clamp voltage of -6 volts.

NOTE

In all applications of the DI-30, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)

0.1 μsec (max)

0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

1.4 watts

Polarization

Pins 28 and 32

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 80 ma

-6 V 42 ma (reverse current into supply)

+12 V 5 ma

Handle Color Code

Long: Red

Short: Yellow

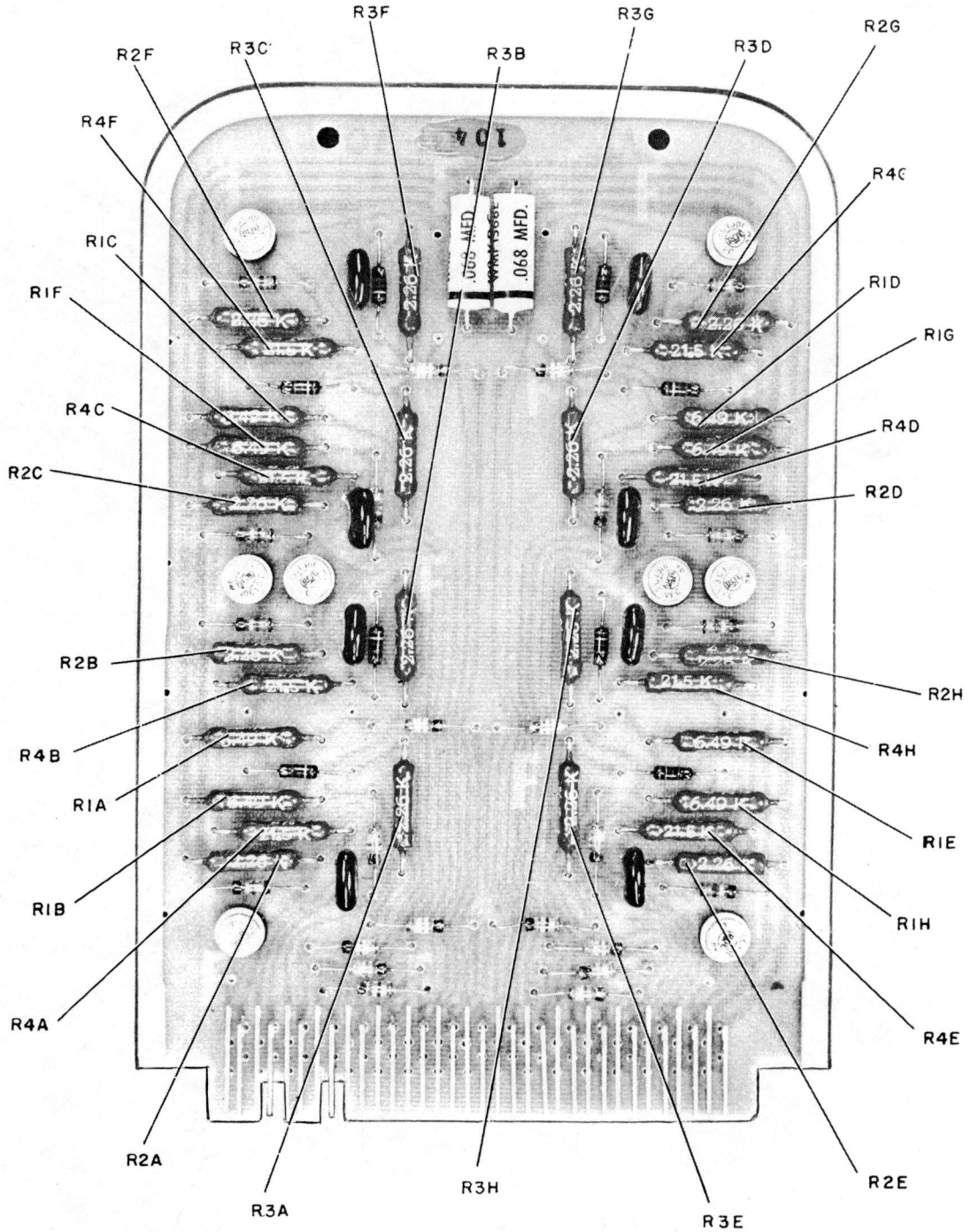


Figure 3-4.1. NAND PAC, Model DI-30, Parts Location (Resistors)

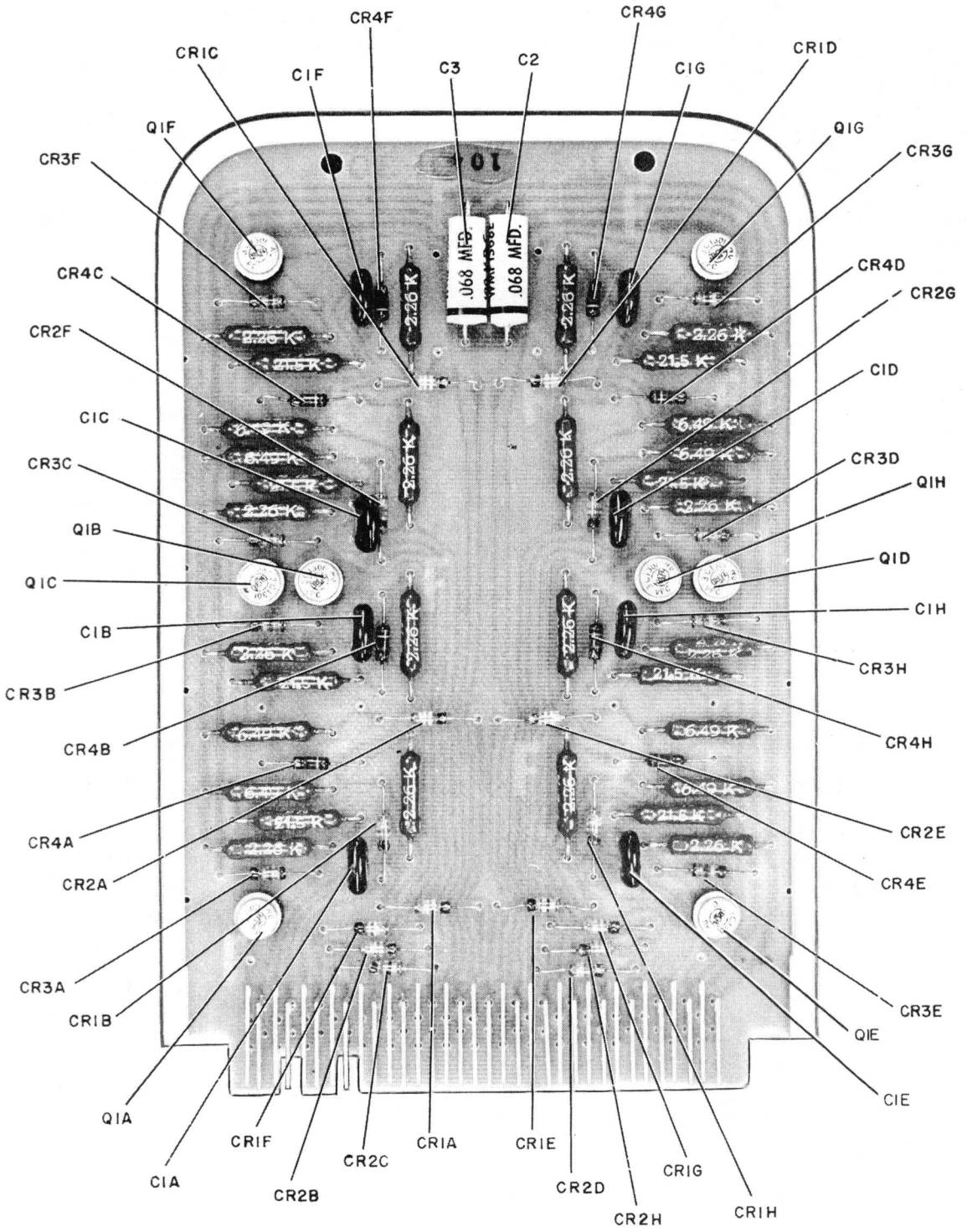


Figure 3-4.2. NAND PAC, Model DI-30, Parts Location
(Capacitors, Diodes, and Transistors)

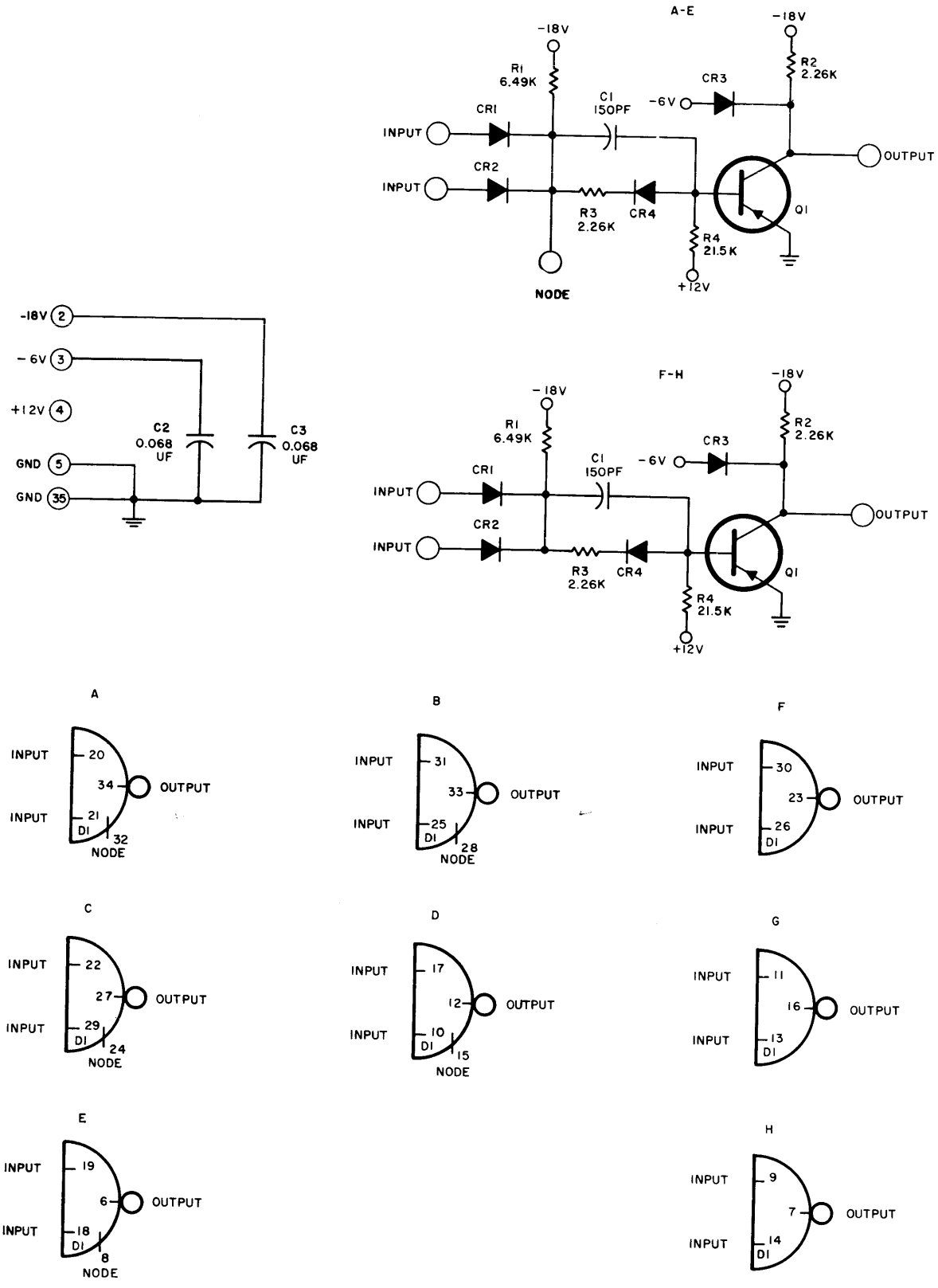


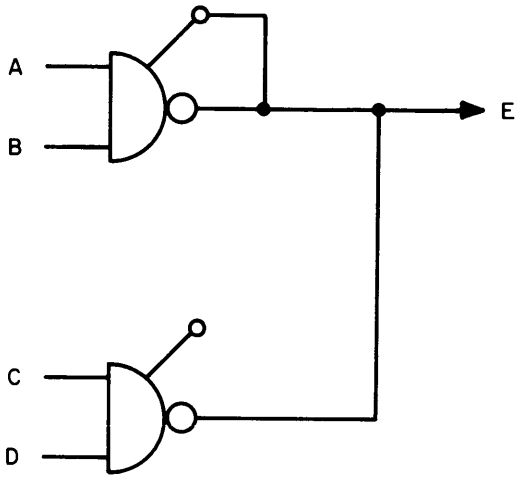
Figure 3-4.3. NAND PAC, Model DI-30, Schematic and Logic Diagram

3-5 PARALLEL NAND GATE PAC, MODEL DJ-30

GENERAL DESCRIPTION

The Parallel NAND Gate PAC, Model DJ-30 (figure 3-5.1), contains six 2-input NAND gates with nodes. The circuits allow the connection of NAND gates in parallel without decreasing the output drive capability (fanout). The diode clusters can be used to expand the number of inputs to the NAND gates and to other S-PACs. The gates operate on levels, pulses, or with a combination of both.

NAND gates with parallel collectors can perform logic functions as shown in the following illustration.

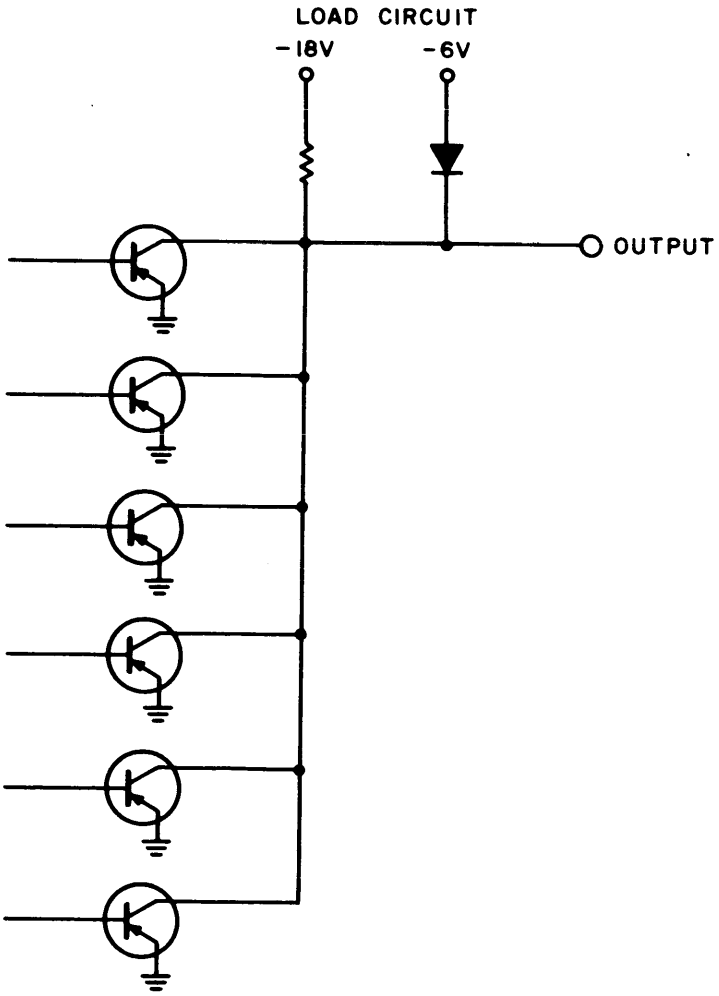


$$E = \overline{AB + CD} = (\overline{AB}) \cdot (\overline{CD})$$

At the point where the outputs are tied together, an OR operation with logic ZEROs (AND operation with logic ONEs) is performed.

CIRCUIT FUNCTION

The DJ-30 (figure 3-5.2) contains six 2-input NAND gates with separate collector load circuits. These load circuits consist of a resistor to the -18 volt supply and a clamp diode to the -6 volt supply. Each collector load can be jumpered to a corresponding gate circuit to form a standard NAND gate; however, a single load circuit can be tied to the output of several parallel-connected gate circuits without affecting the fanout. If the inputs are such that one or more transistors are conducting, the output will be at 0 volt. The maximum drive capability with up to 10 collector outputs jumpered in parallel is 7 unit loads. The following illustration shows all DJ-30 gates on a PAC tied in parallel.



Model DJ-30, Parallel Gate Configuration

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)

0.1 μsec (max)

0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

1.0 watt

Polarization

Pins 20 and 30

Frequency of Operation

DC to 1 MC (max)

Number of Outputs in Parallel

Limited only by total fall time acceptable

Fall time increases 0.015 μsec per paralleled DJ-30.

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 60 ma

-6 V 32 ma (reverse current into supply)

+12 V 4 ma

Handle Color Code

Long: Red

Short: Brown

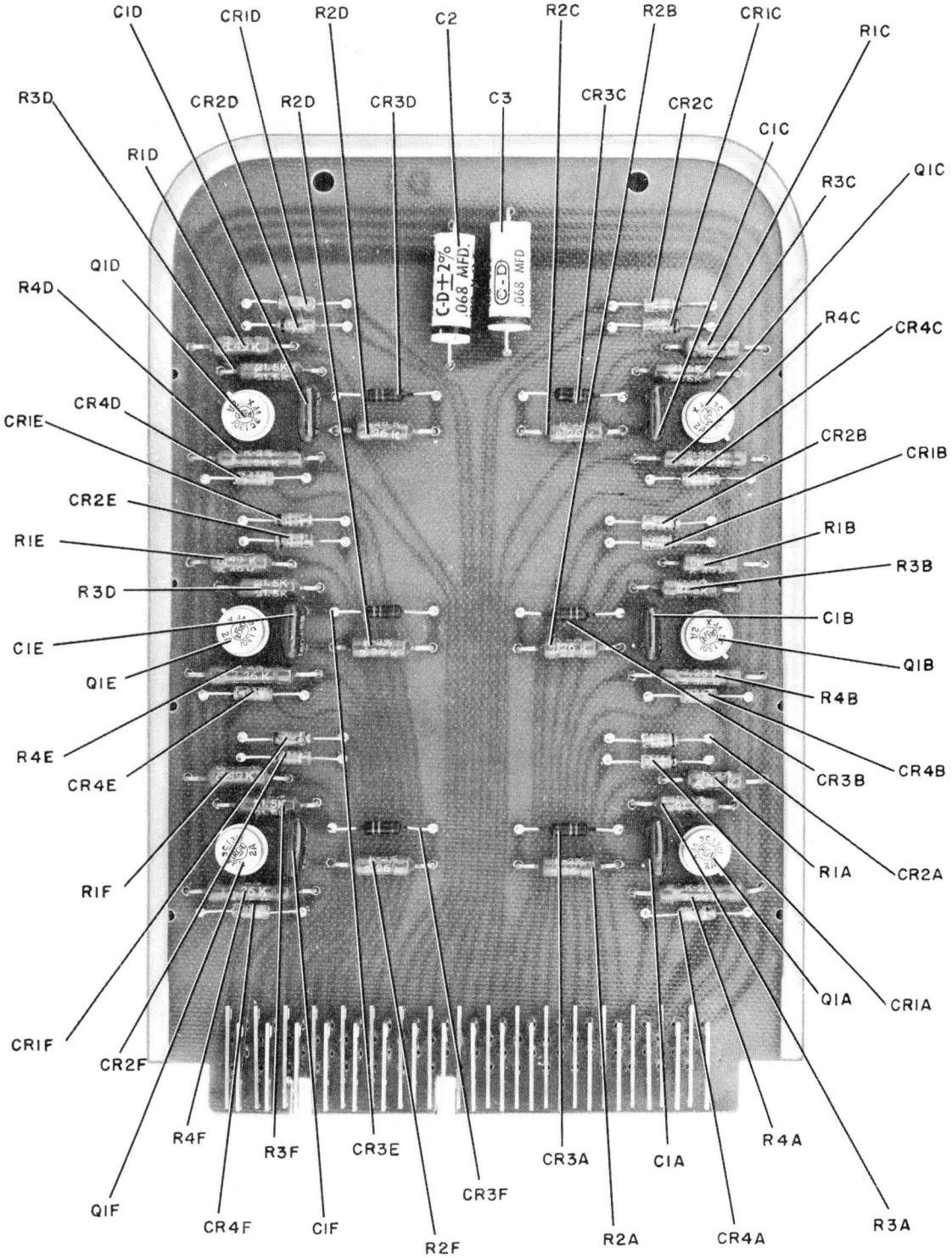


Figure 3-5.1. Parallel NAND Gate PAC, Model DJ-30, Parts Location

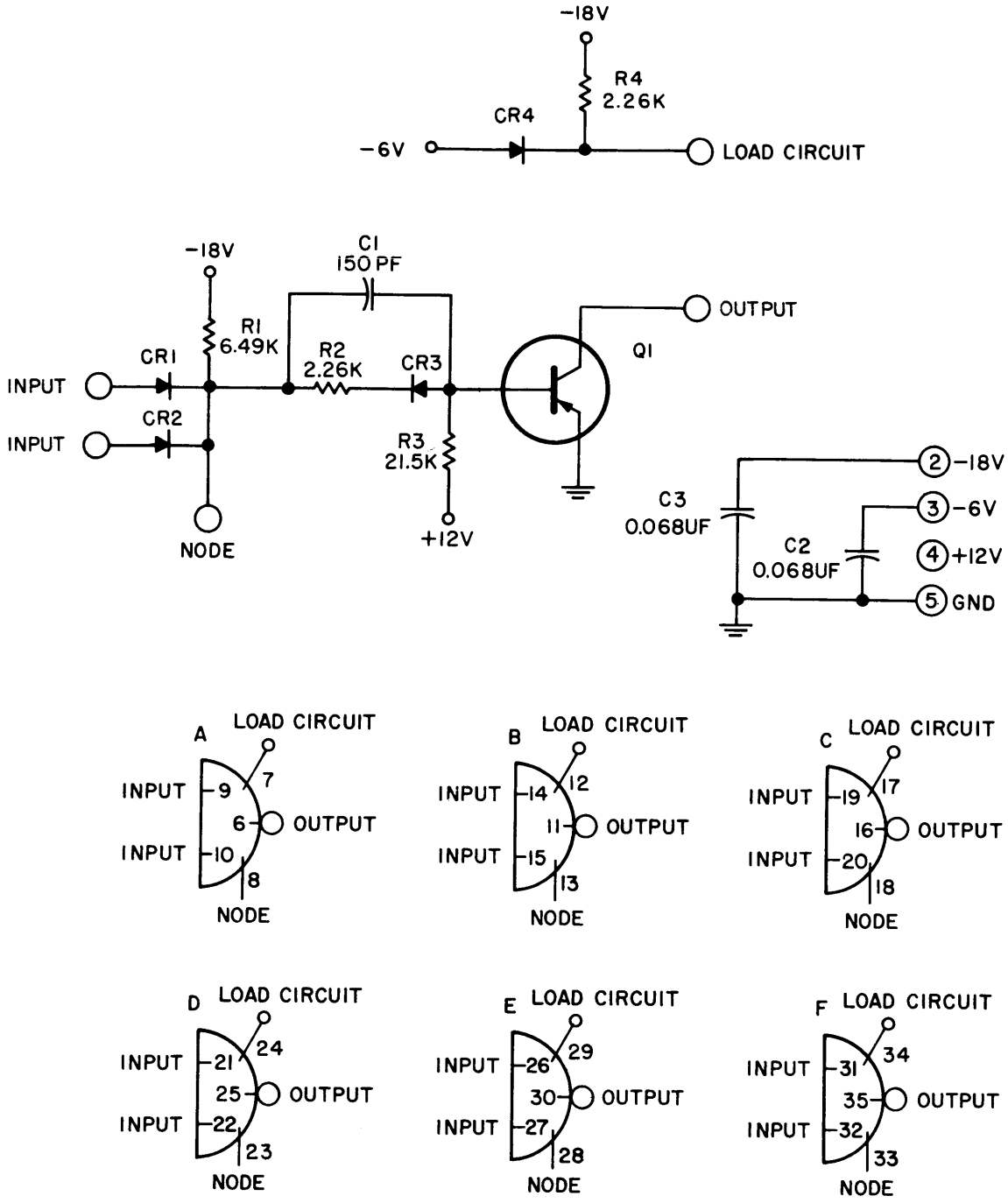


Figure 3-5.2. Parallel NAND Gate PAC, Model DJ-30, Schematic and Logic Diagram

3-6 NAND PAC, MODEL DL-30

GENERAL DESCRIPTION

The NAND PAC, Model DL-30 (figures 3-6.1 and 3-6.2), contains five 3-input and three 2-input NAND gates without nodes. These gates can be expanded by using one of the diode inputs as a node and connecting diode clusters from a DC, DN, or DF S-PAC. However, the use of a diode input as a node slightly reduces the noise margins on the expanded inputs (from the S-PAC noise margin minimum of 1.5 volts to 1.2 volts).

Each NAND gate performs the NAND function for negative voltage logic (ONE = -6 V) or the NOR function for positive voltage logic (ONE = 0 V). The gates operate on levels, pulses, or with combinations of both.

Two DL-30 NAND gates form a flip-flop when their inputs and outputs are cross-coupled.

The DI-30 and DL-30 are similar PACs with identical input and output connector pins. These PACs are therefore interchangeable in S-BLOC installations with the exception of polarization; the S-BLOC polarization must be modified to agree with the particular PAC. The difference between the PACs is where the DI-30 contains gates with two-diode and one-node inputs and the DL-30 contains gates with three-diode inputs.

CIRCUIT FUNCTION

Each DL-30 PAC (figure 3-6.3) consists of five 3-input and three 2-input diode gates followed by a transistor inverter amplifier. When all inputs to a gate are at ONE (-6 V), the transistor is turned on and the output is clamped through the transistor to 0 volt. When an input to a gate goes to ZERO (0 V), the transistor is turned off and the output falls to the clamp voltage of -6 volts.

NOTE

In all applications of the DL-30, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)
0.1 μsec (max)
0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

1.4 watts

Polarization

Pins 16 and 20

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 80 ma
- 6 V 42 ma (reverse current into supply)
+12 V 5 ma

Handle Color Code

Long: Orange

Short: Red

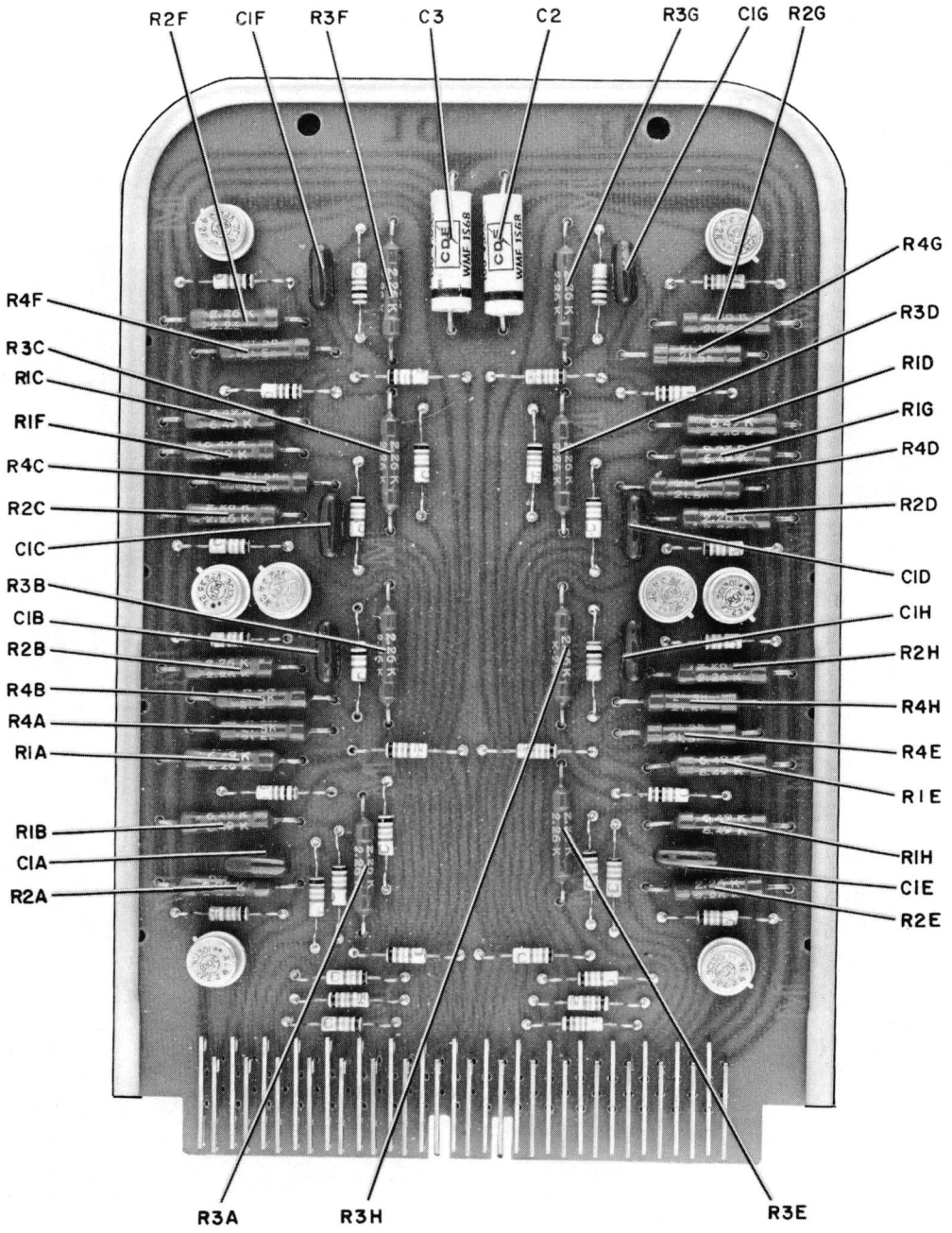


Figure 3-6.1. NAND PAC, Model DL-30, Parts Location (Resistors and Capacitors)

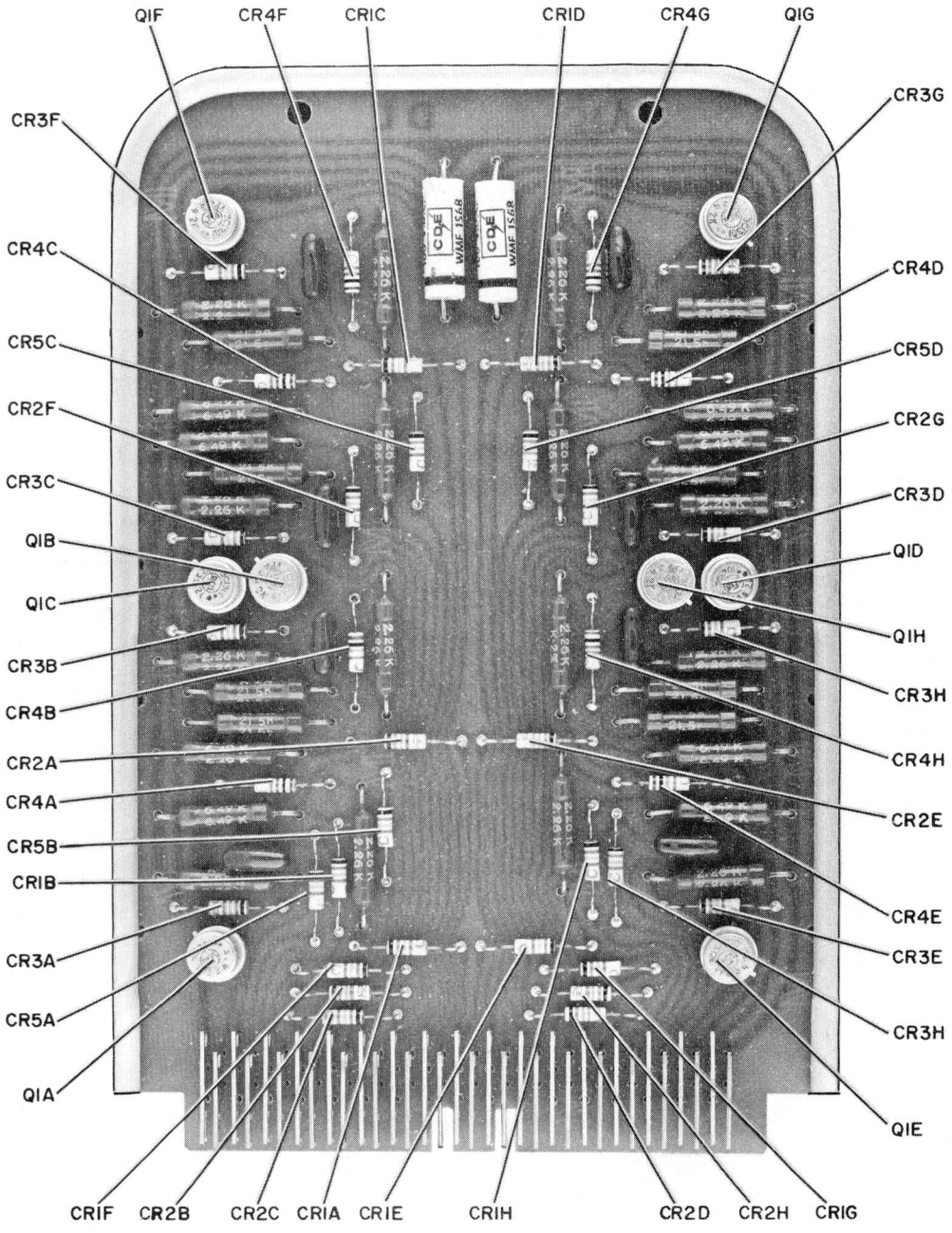


Figure 3-6.2. NAND PAC, Model DL-30, Parts Location (Diodes and Transistors)

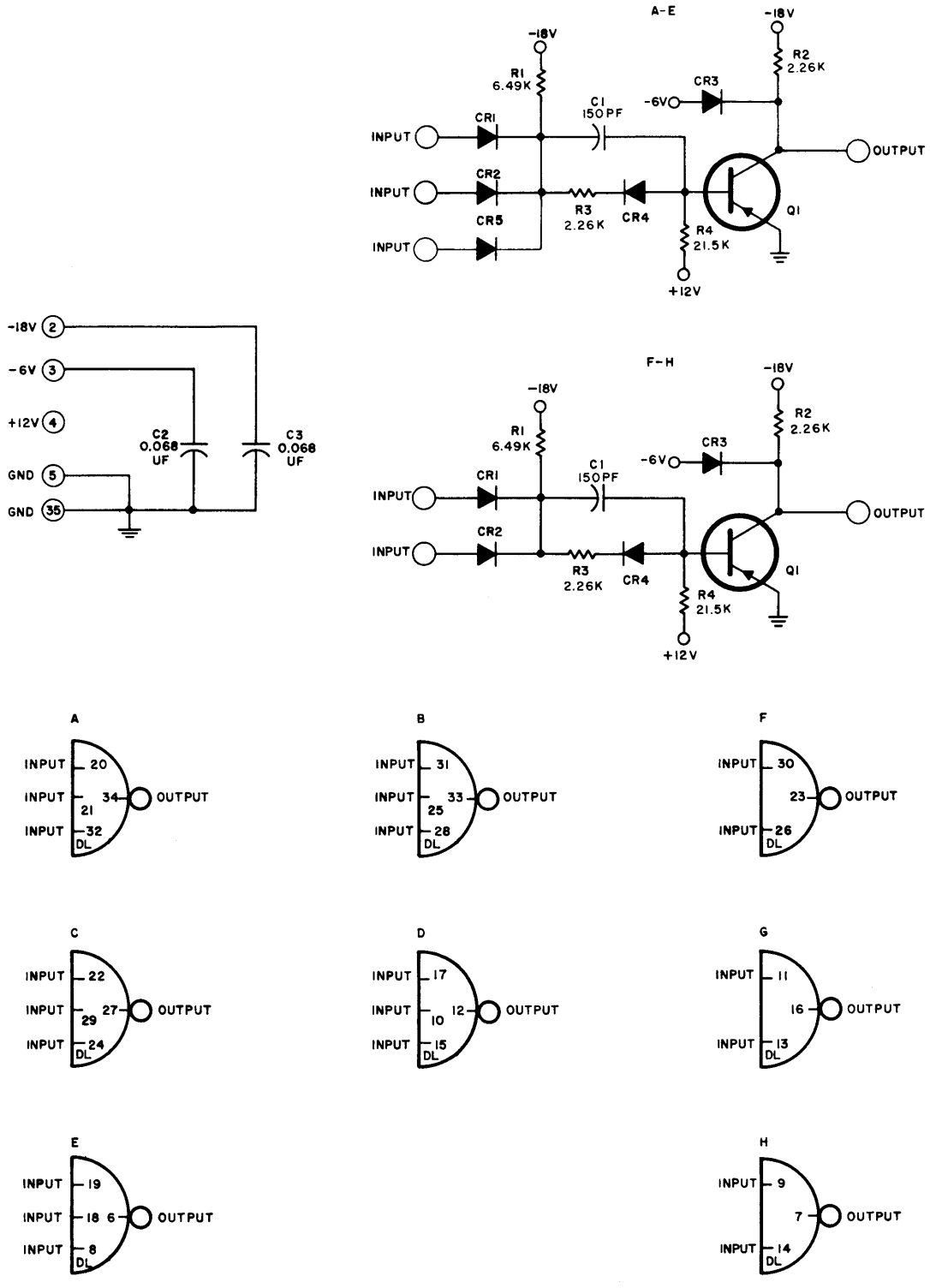


Figure 3-6.3. NAND PAC, Model DL-30, Schematic and Logic Diagram

3-7 DELAY MULTIVIBRATOR/PULSE SHAPER PAC, MODEL DM-30

GENERAL DESCRIPTION

The Delay Multivibrator/Pulse Shaper PAC, Model DM-30 (figures 3-7.1 and 3-7.2), contains three independent and identical one-shot multivibrators capable of generating pulses in a variety of widths. The capacitors provided with each circuit can be wired for pulse widths of 0.7 to 200 microseconds. In addition, externally connected capacitors can be used to obtain pulse widths up to several seconds. An AC trigger input, an input node, and assertion and negation outputs are available on each multivibrator. Each output is capable of driving four unit loads. The DM-30 is useful in applications requiring delayed levels or pulse shaping and standardizing.

CIRCUIT FUNCTION

Each DM-30 circuit (figure 3-7.3) consists of a single input gate (expandable to 10 inputs using the input node) which is AC-coupled to a monostable multivibrator. A delay cycle is initiated by a positive-going transition at the input. The triggering input must remain positive for at least 0.25 microsecond and negative for at least 0.6 microsecond prior to the triggering action.

The pulse width is controlled by precision resistors, stable mica and film capacitors, and a zener diode reference element. Pulse width is essentially independent of temperature, power supply variations, ripple, etc. The required recovery period for the delay multivibrator is less than 80 percent of the pulse width and begins immediately after the delay period, regardless of the state of the input signal. The delay multivibrator can be triggered during the 50 to 80 percent of pulse width portion of the recovery period, but yields a narrower than normal output signal (figure 3-7.4). The delay multivibrator should not be triggered during the recovery period from 0 to 50 percent of the pulse width. For example, if successive 10-microsecond delays are required, the time between triggering should be a minimum of 18 microseconds. Retriggering during the active pulse time does not affect circuit operation or cause any additional output.

The pulse width is controlled by connecting the appropriate capacitors to the delay node as indicated in the schematic portion of figure 3-7.3. Two or more of the internally provided capacitors can be connected simultaneously and the resulting pulse has a width equal to the sum of the pulse widths indicated in the logic diagram portion of figure 3-7.3. For other delays, external capacitors should be connected across the delay node and external delay node (terminals 7 and 8, 16 and 11, or 27 and 18, depending upon which of the three circuits is used).

The value of the external capacitor is calculated from the following equation:

$$C = 360 \ (PW - 0.7 \ \mu sec)$$

where C is capacitance in picofarads and PW is pulse width in microseconds.

Table 3-7.1. Delay Multivibrator Output Delay Widths and Proper Jumper Connections at the PAC Connector

Delay Width	Circuit A Jumper Connections	Circuit B Jumper Connections	Circuit C Jumper Connections
0.7 μsec	No jumper connections required	No jumper connections required	No jumper connections required
2 μsec	Pins 12 and 8	Pins 20 and 11	Pins 32 and 18
5 μsec	Pins 13 and 8	Pins 21 and 11	Pins 33 and 18
10 μsec	Pins 14 and 8	Pins 24 and 11	Pins 34 and 18
200 μsec	Pins 15 and 8	Pins 23 and 11	Pins 35 and 18
For all other delay widths	Connect an external capacitor between pins 7 and 8	Connect an external capacitor between pins 16 and 11	Connect an external capacitor between pins 27 and 18

SPECIFICATIONS

Circuit Delay

0.25 μsec (max) negation output

0.15 μsec (typ) negation output

0.15 μsec (max) assertion output

0.10 μsec (typ) assertion output

Width Accuracy

10% from circuit to circuit

Frequency of Operation

DC to $\frac{1}{1.8 \times PW}$ or 600 KC, whichever is less, where PW is pulse width in μsec

Internally Provided Nominal Pulse Widths

0.7 μsec, 2 μsec, 5μsec, 10 μsec, and 200 μsec

Pulse Width Variations

(All independently specified)

Short-term stability (8 hours): <1%

Jitter (pulse-to-pulse): <0.1%

Long-term stability (reproducibility over three months): <2%

Temperature variation:
-20° to +25°C: -7%
+25° to +55°C: +8%

Input Loading

2 unit loads each

Recovery Time

<80% of pulse width (figure 3-7.4)

Output Waveform Characteristics

Assertion Output (negative pulse measured from -0.6 to -4.5 V)

Rise time: 0.15 μsec or 0.2% of pulse width, whichever is longer

Fall time: 0.15 μsec (typ)

NOTE

A positive-going edge, adequate for triggering of another DM-30, is assured on the trailing edge of DM-30 assertion pulses up to 1 millisecond wide. For wider pulses (longer delays), inversion of the negation output is recommended for triggering of AC inputs and DM-30s.

Negation Output (positive pulse)

Rise time: 0.06 μsec(typ)

Fall time: 0.15 μsec(typ)

SPECIFICATIONS (Continued)

Output Drive Capability

4 unit loads and 200 pf stray capacitance

Total Power

1.4 watts

Polarization

Pins 18 and 20

Current Requirements

-18 V 90 ma

-6 V 25 ma (reverse current into supply)

+12 V 1.8 ma

Handle Color Code

Long: Yellow

Short: Yellow

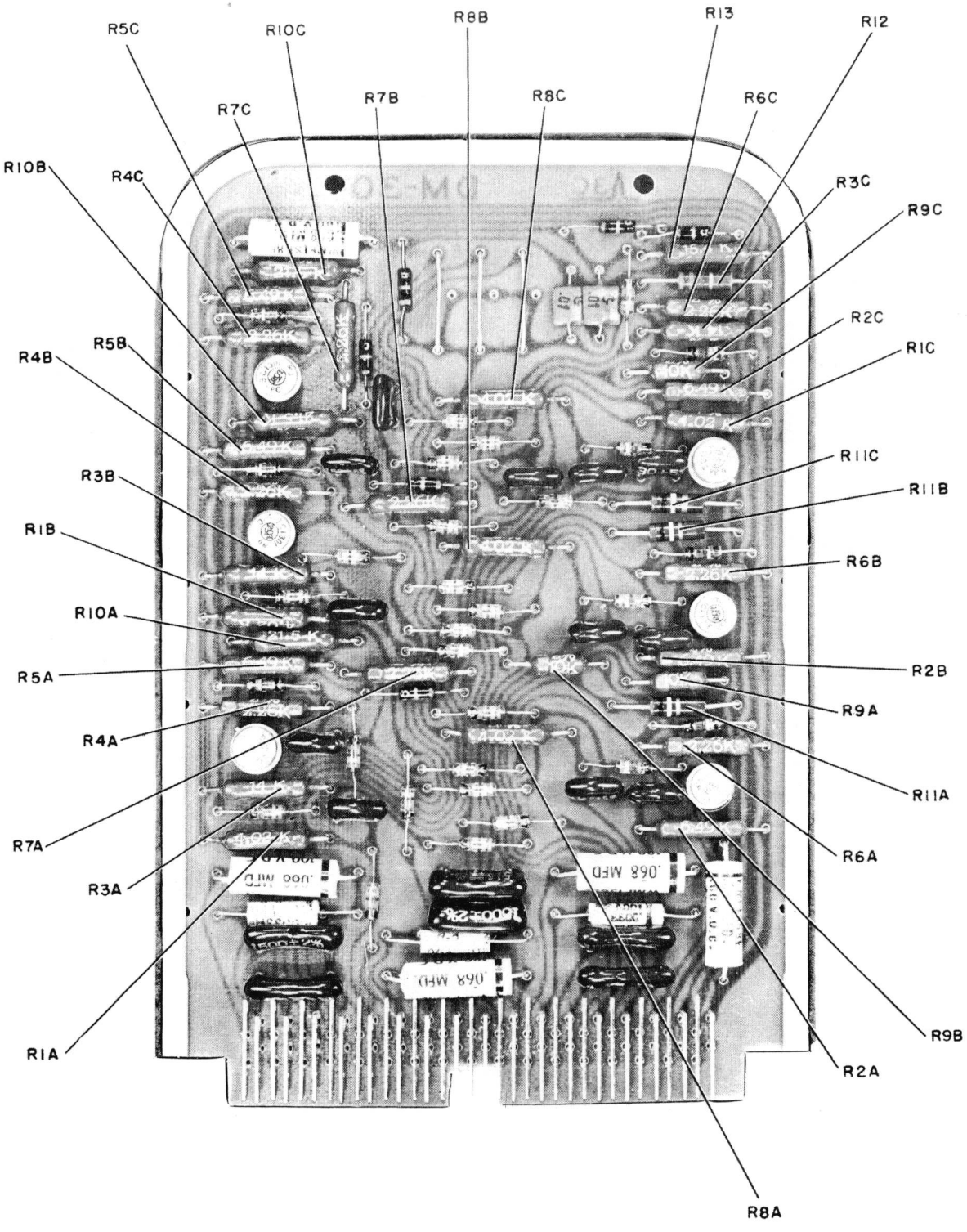


Figure 3-7.1. Delay Multivibrator/Pulse Shaper PAC, Model DM-30, Parts Location (Resistors)

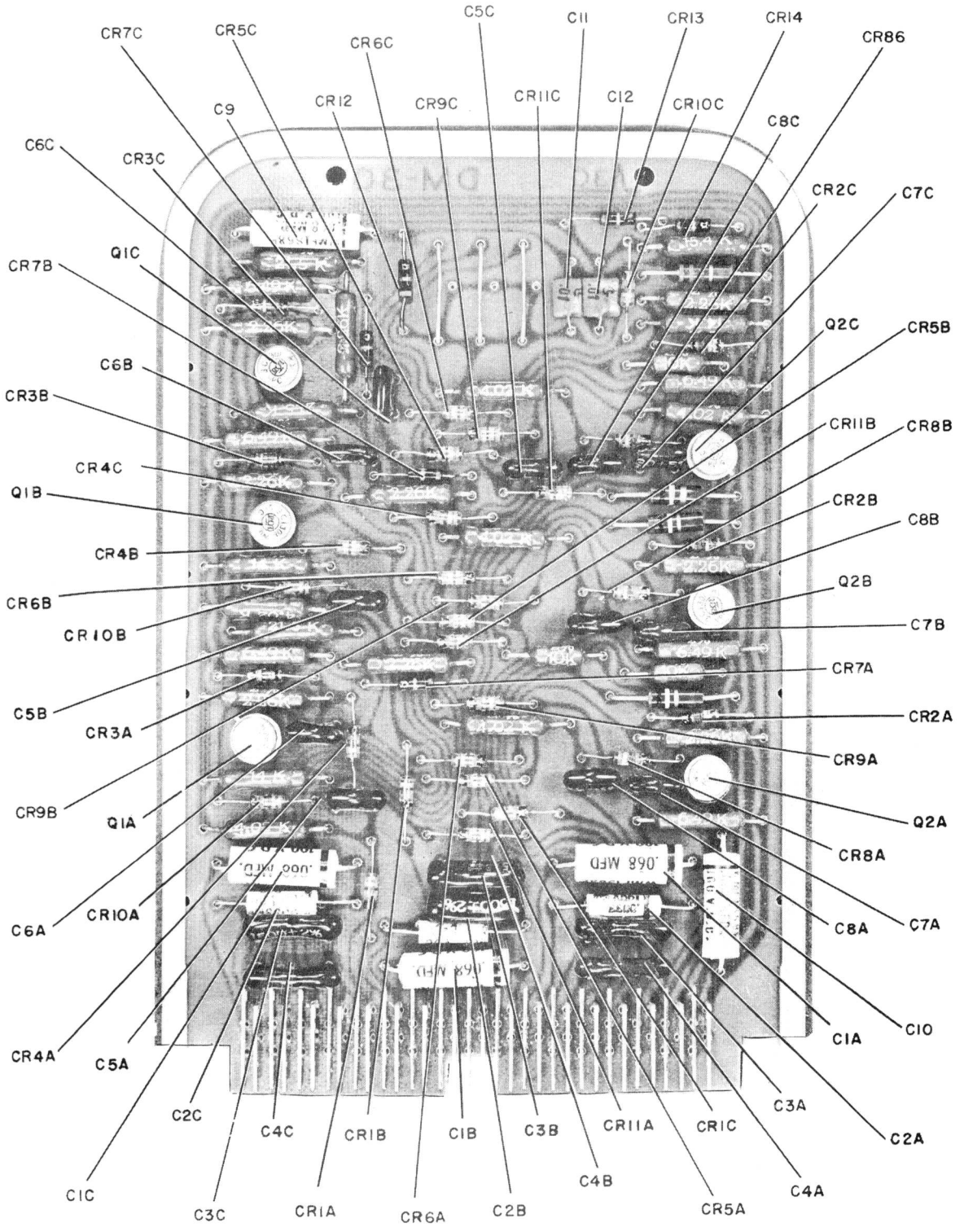


Figure 3-7.2. Delay Multivibrator/Pulse Shaper PAC, Model DM-30, Parts Location (Capacitors, Diodes, and Transistors)

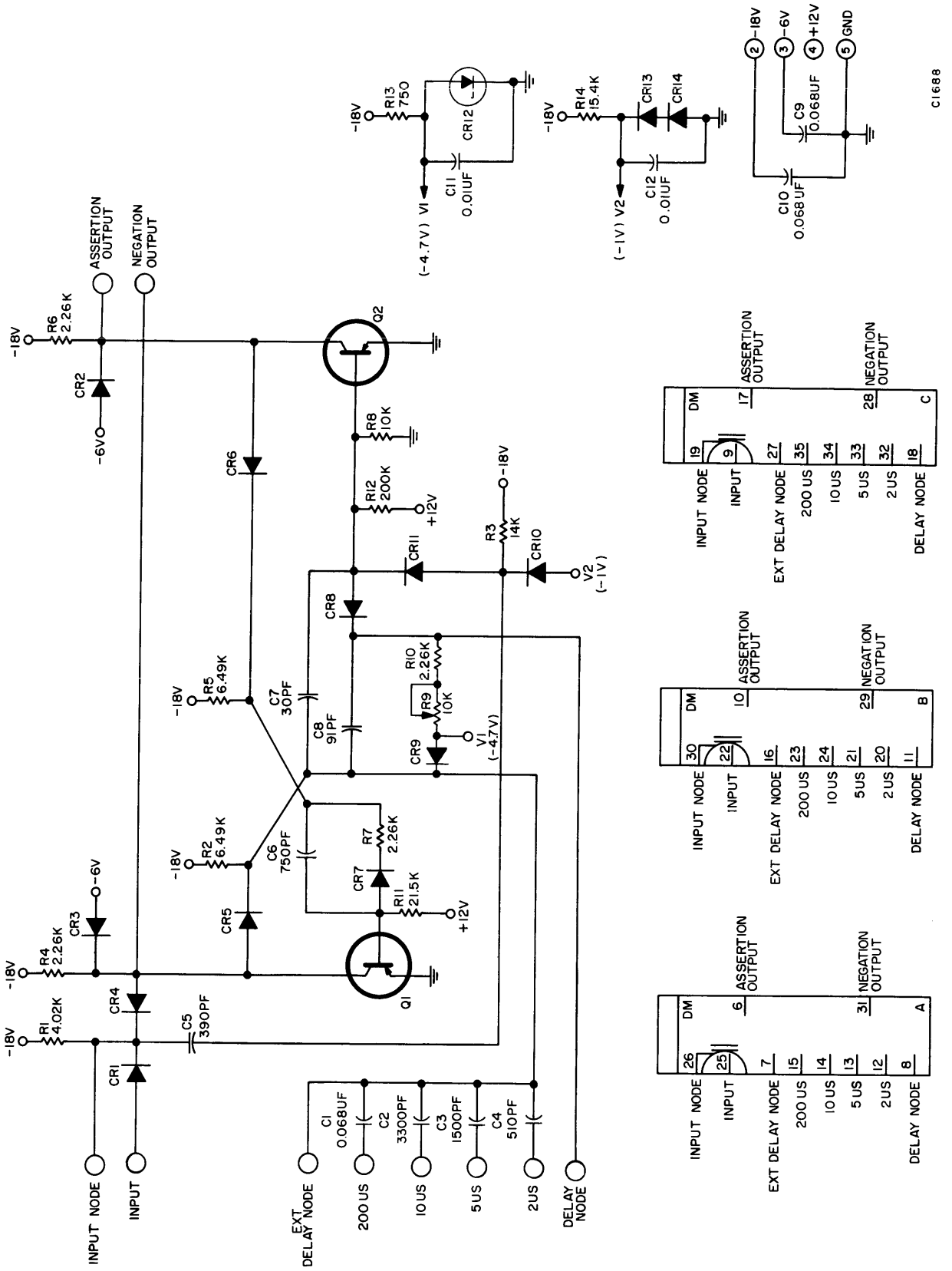


Figure 3-7.3. Delay Multivibrator/Pulse Shaper PAC, Model DM-30, Schematic and Logic Diagram

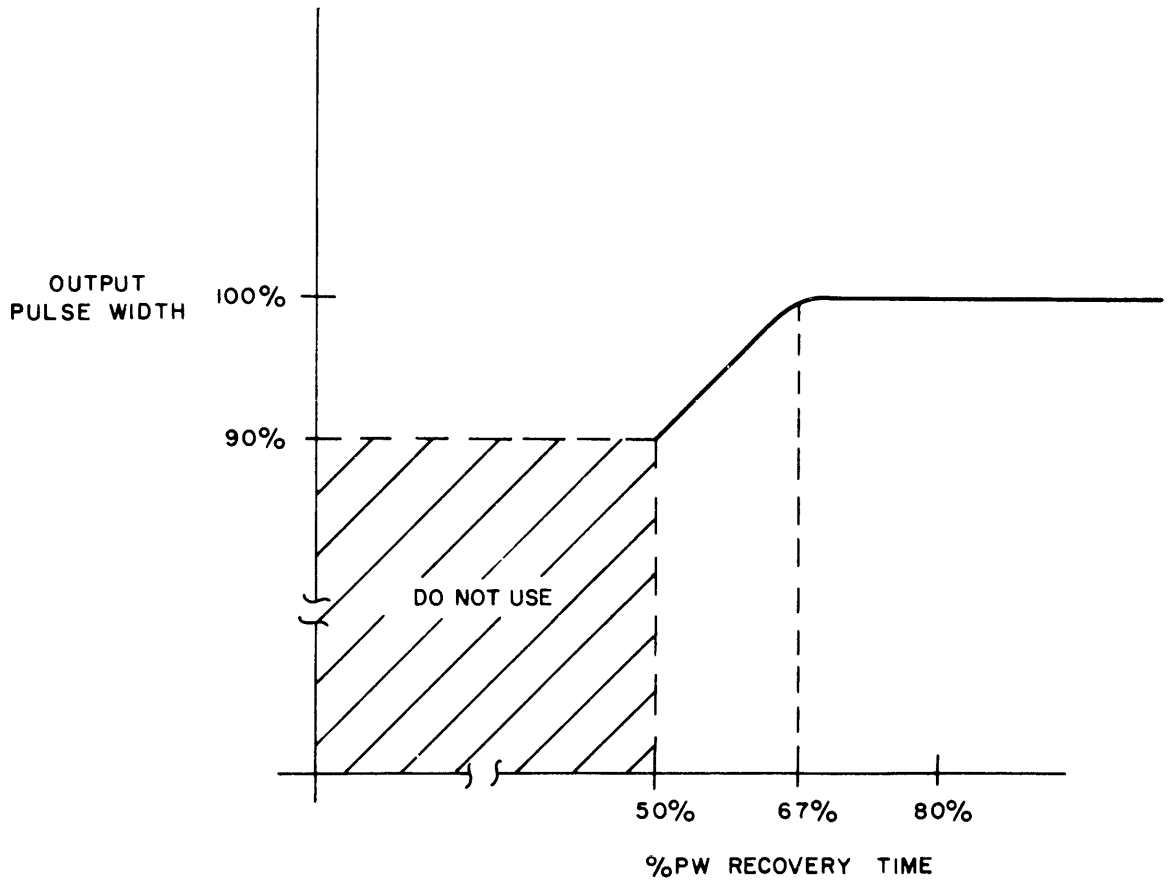


Figure 3-7.4. Typical DM-30 Recovery Curve

3-8 ADJUSTABLE DELAY MULTIVIBRATOR PAC, MODEL DM-30A

GENERAL DESCRIPTION

The Adjustable Delay Multivibrator PAC, Model DM-30A (figures 3-8.1 and 3-8.2), contains three independent and identical variable one-shot multivibrators. The delays available from each circuit are nominally the same as the DM-30 and each pulse width is variable from 60 percent of nominal to 3 times the nominal width. Externally connected capacitors can be used to obtain pulse widths up to several seconds. An AC trigger input, an input node, and assertion and negation outputs are available on each circuit. The negation output is capable of driving four unit loads and the assertion output of driving one unit load.

CIRCUIT FUNCTION

The circuit function of the DM-30A (figure 3-8.3) is essentially similar to that of the DM-30. Three potentiometers are mounted on the DM-30A to allow independent pulse-width variation of each circuit. The required recovery period for the adjustable delay multivibrator is less than 80 percent of the pulse width and begins immediately after the delay period, regardless of the state of the input signal. The delay multivibrator can be triggered during the 50 to 80 percent of pulse width portion of the recovery period, but yields a narrower than normal output signal (figure 3-8.4). The delay multivibrator should not be triggered during the recovery period from 0 to 50 percent of the pulse width. For example, if successive 10-microsecond delays are required, the time between triggering should be a minimum of 18 microseconds. Retriggering during the active pulse time has no affect on circuit operation.

The pulse width is controlled by connecting the appropriate capacitors to the delay node as indicated in the schematic portion of figure 3-8.3. Two or more of the internally provided capacitors can be connected simultaneously and the resulting pulse has a width equal to the sum of the pulse widths indicated in the logic diagram portion of figure 3-8.3. For other delays, external capacitors should be connected across the delay node and external delay node (terminals 7 and 8, 16 and 11, or 27 and 18, depending upon which of the three circuits is used).

The value of the external capacitor can be calculated from the following equation:

$$C = 360\ (PW - 0.7\,\mu sec)$$

where C is capacitance in picofarads and PW is pulse width in microseconds.

Table 3-8.1. Delay Multivibrator Output Delay Widths and Proper Jumper Connections at the PAC Connector

Delay Width	Circuit A Jumper Connections	Circuit B Jumper Connections	Circuit C Jumper Connections
0.7 μsec	No jumper connections required	No jumper connections required	No jumper connections required
2 μsec	Pins 12 to 8	Pins 20 to 11	Pins 32 to 18
5 μsec	Pins 13 to 8	Pins 21 to 11	Pins 33 to 18
10 μsec	Pins 14 to 8	Pins 24 to 11	Pins 34 to 18
200 μsec	Pins 15 to 8	Pins 23 to 11	Pins 35 to 18
For all other delay widths	Connect an external capacitor between pins 7 and 8	Connect an external capacitor between pins 16 and 11	Connect an external capacitor between pins 27 and 18

SPECIFICATIONS

Circuit Delay

0.25 μsec (max) negation output

0.15 μsec (typ) negation output

0.15 μsec (max) assertion output

0.10 μsec (typ) assertion output

Frequency of Operation

DC to $\frac{1}{1.8 \times PW}$ or 500 KC (max) whichever is less, where PW is pulse width in μsec

Internally Provided Nominal Pulse Widths

0.7 μsec, 2 μsec, 5 μsec, 10 μsec, and 200 μsec

Pulse Width Variations

(All independently specified)

Short-term stability (8 hours): < 1%

Jitter (pulse-to-pulse): < 0.1%

Long-term stability (reproducibility over three months): <2%

Temperature variation:
-20°C to +25°C: -7%
+25°C to +55°C: +8%

Input Loading

2 unit loads each

Recovery Time

80% of pulse width (figure 3-7.4)

Output Waveform Characteristics

Assertion Output:

Rise time: 0.2 μsec or 0.3% of pulse width, whichever is longer.

Fall time: 0.15 μsec (typ)

NOTE

A positive-going edge, adequate for triggering another DM-30A, is assured on the trailing edge of DM-30A assertion pulses up to 1 millisecond wide. For wider pulses (longer delays), inversion of the negation output is recommended for triggering of AC inputs and DM-30As.

Negation Output:

Rise time: 0.06 μsec (typ)

Fall time: 0.15 μsec (typ)

Pulse Width Control

Fully CW: 60% of nominal PW

Fully CCW: 3 times nominal PW

Clockwise rotation decreases pulse width

SPECIFICATIONS (Continued)

Output Drive Capability

Assertion Output (negative pulse):
1 unit load

Negation Output (positive pulse):
4 unit loads

Total Power

1.3 watts

Polarization

Pins 18 and 20

Current Requirements

-18 V 80 ma

-6 V 25 ma (reverse current into supply)

+12 V 1.8 ma

Handle Color Code

Long: Yellow

Short: Black (with silver character A)

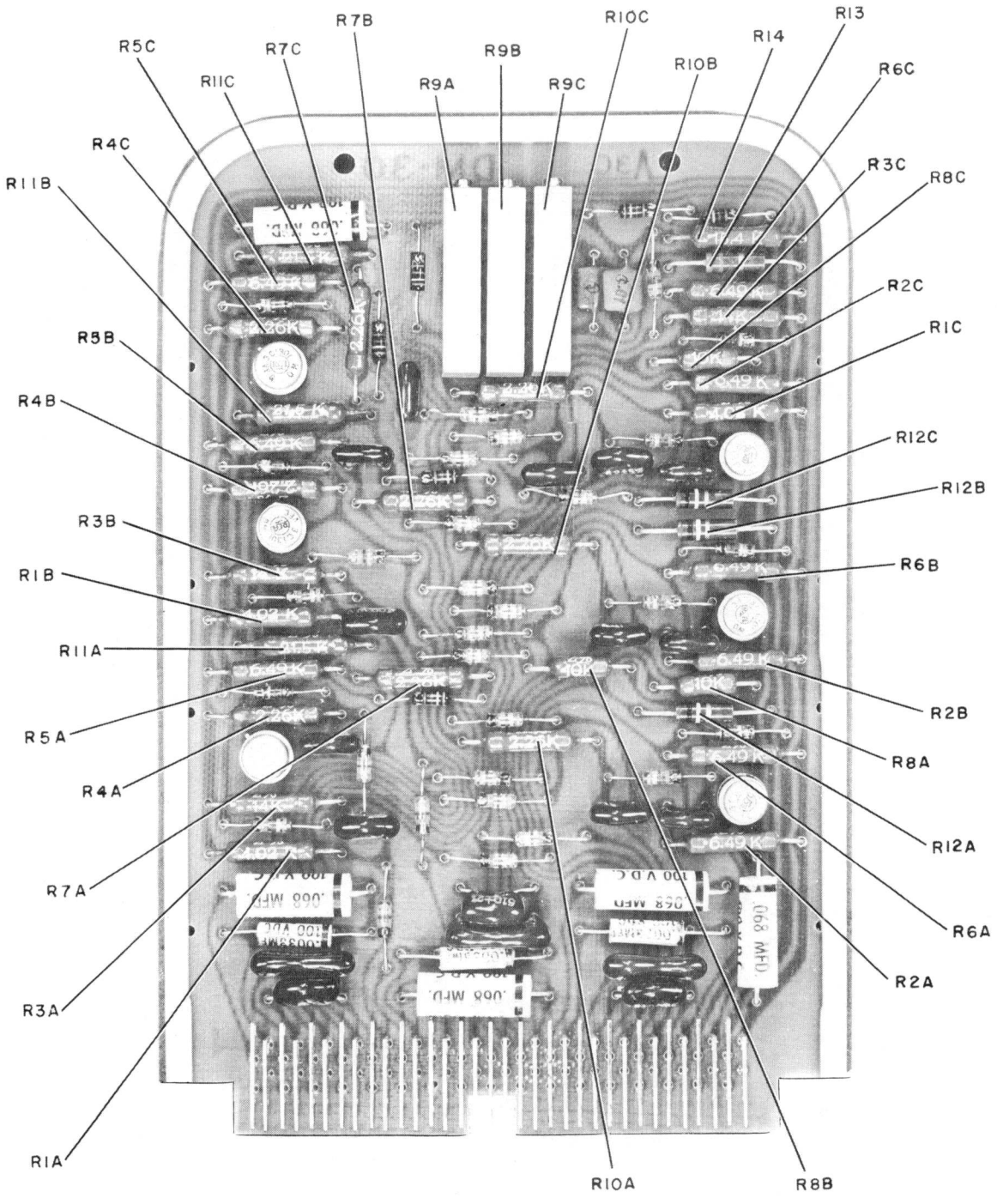


Figure 3-8.1. Adjustable Delay Multivibrator PAC, Model DM-30A, Parts Location (Resistors)

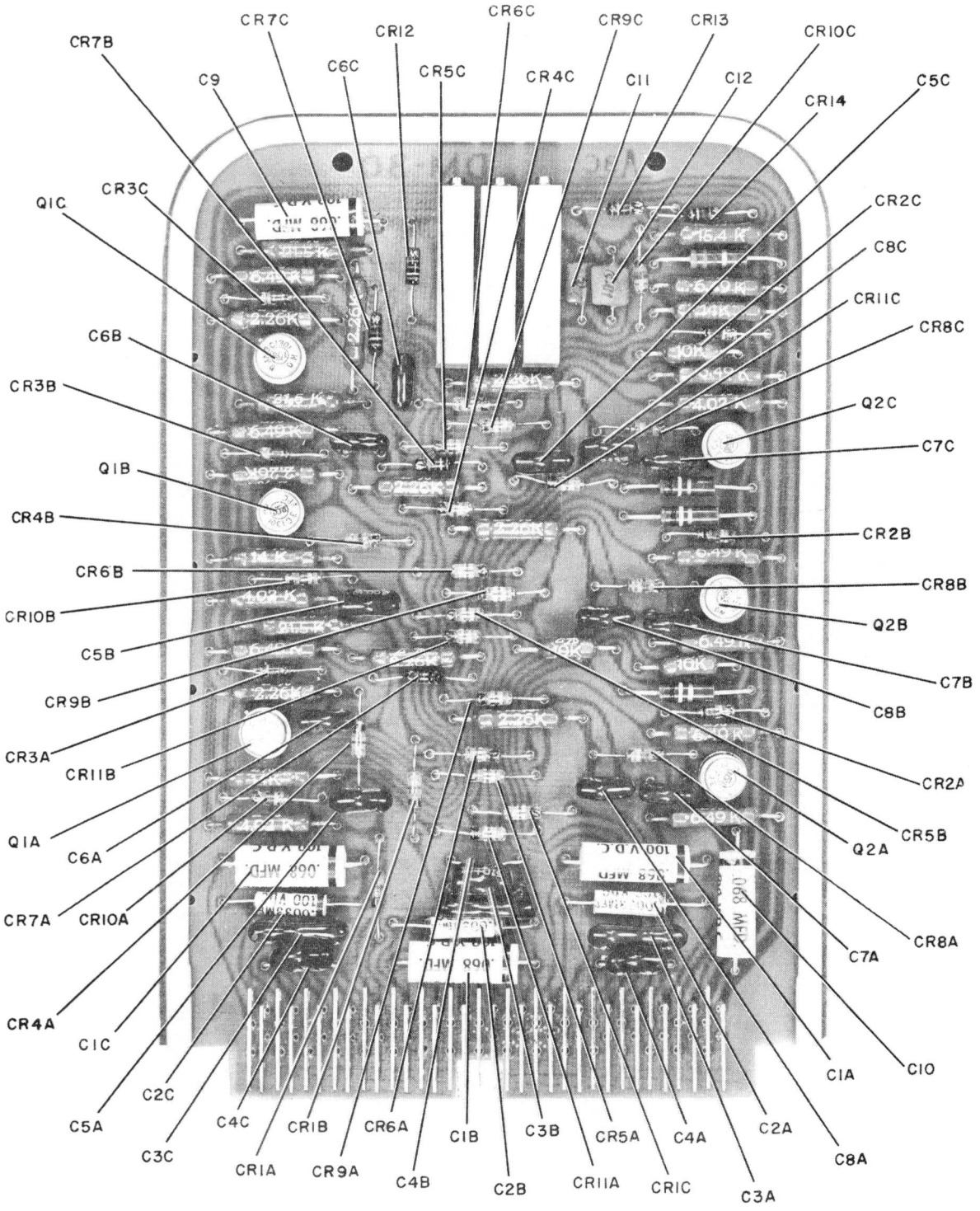


Figure 3-8.2. Adjustable Delay Multivibrator PAC, Model DM-30A, Parts Location (Capacitors, Diodes, and Transistors)

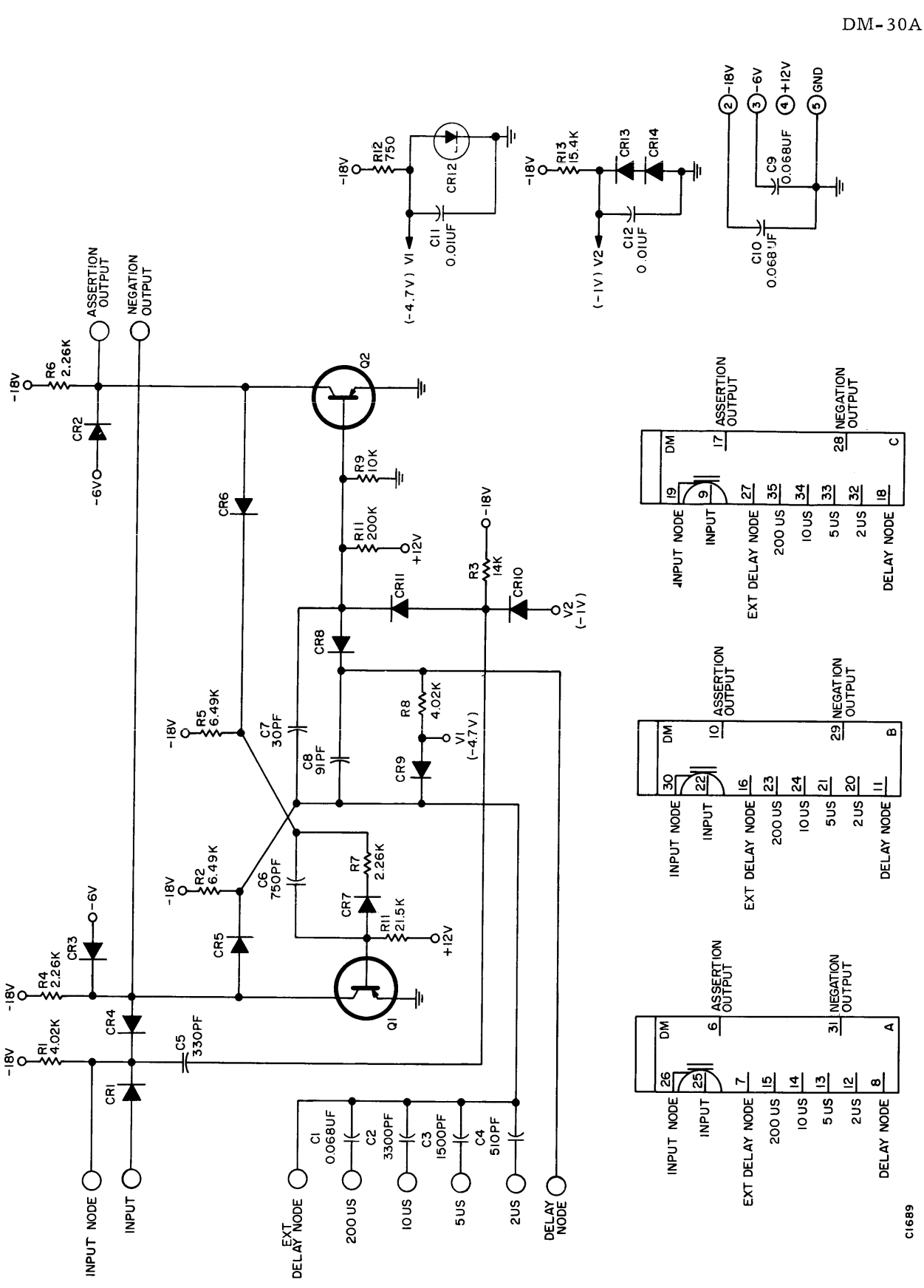


Figure 3-8.3. Adjustable Delay Multivibrator PAC, Model DM-30A, Schematic and Logic Diagram

3-9 GATE PAC, MODEL DN-30

GENERAL DESCRIPTION

The Gate PAC, Model DN-30 (figure 3-9.1), contains four 2-input NAND gates, two 3-diode clusters, and two 2-diode clusters. These diode clusters can be used to expand the number of inputs to the NAND gates or to other S-PACs.

Each NAND gate performs the NAND function for negative voltage logic (ONE = -6 V) or the NOR function for positive voltage logic (ONE = 0 V). The gates operate on levels, pulses, or with combinations of both.

CIRCUIT FUNCTION

Each DN-30 PAC (figure 3-9.2) consists of a 2-input diode gate followed by a transistor inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the transistor on and the output is clamped through the transistor to 0 volt. When an input goes to ZERO (0 V), the transistor is turned off and the output falls to the clamp voltage of -6 volts.

The diode clusters can be wired to the node input of any S-PAC for expansion of its inputs up to a maximum of 10. Care should be taken to insure that diode cluster connections are made to local PACs and that the interconnecting leads are not cabled. The recommended maximum lead length is 1-1/2 feet.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V, averaged over two stages)

0.1 μsec (max)

0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

Total Power

0.7 watts

Polarization

Pins 6 and 8

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise Time: 0.1 μsec (typ)

Fall Time: 0.15 μsec (typ)

Current Requirements

-18 V 40 ma

-6 V 21 ma (reverse current into supply)

+12 V 3 ma

Handle Color Code

Long: Red

Short: Red

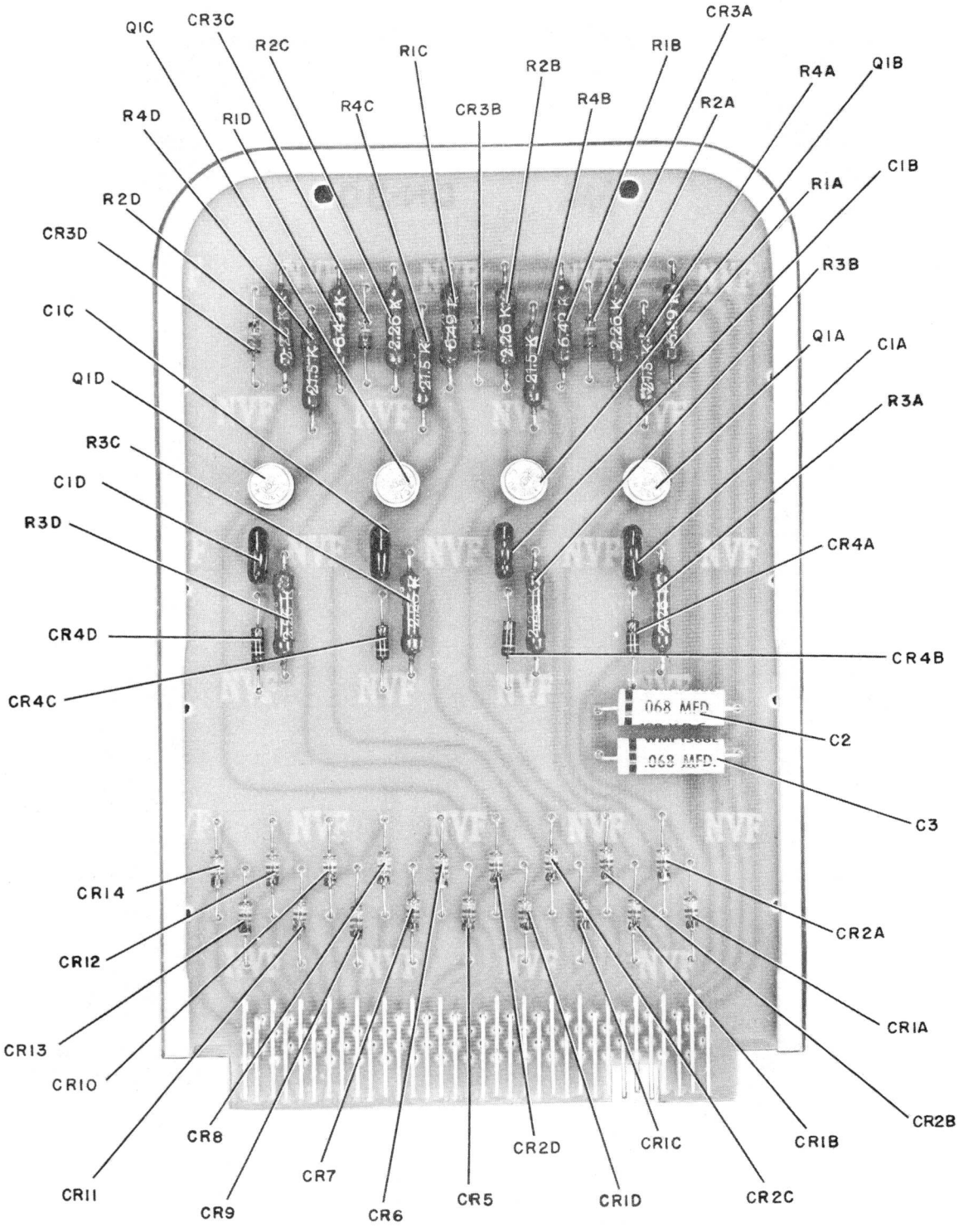


Figure 3-9.1. Gate PAC, Model DN-30, Parts Location

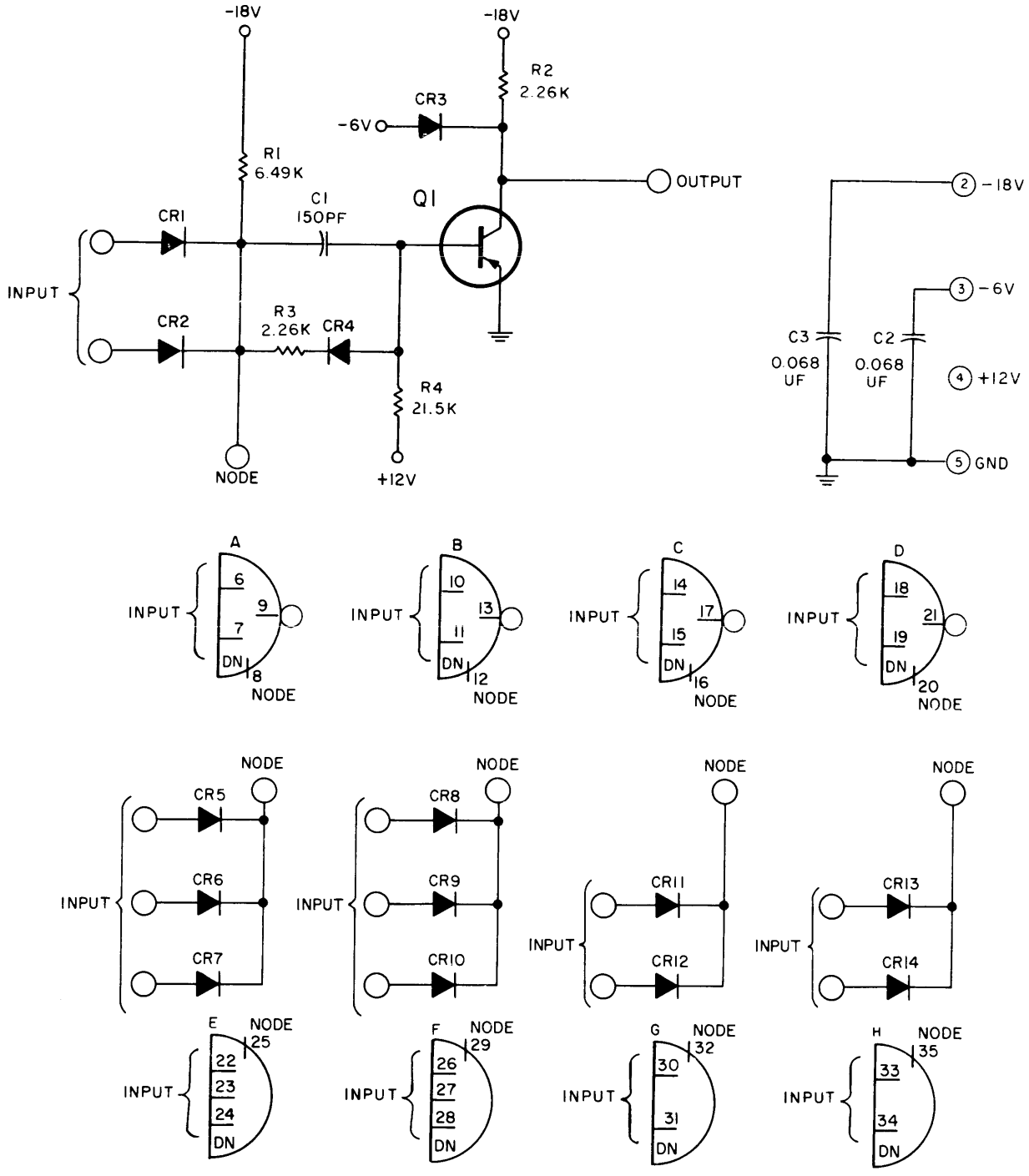


Figure 3-9.2. Gate PAC, Model DN-30, Schematic and Logic Diagram

3-10 DELAYED PULSE PAC, MODEL DS-30

GENERAL DESCRIPTION

The Delayed Pulse PAC, Model DS-30 (figure 3-10.1), contains two monostable multivibrators which generate delays in a variety of widths and two pulse shaper circuits. Each monostable multivibrator drives a pulse shaper which delivers a pulse at the end of the delay. Therefore, the PAC provides pulses delayed relative to an input signal and performs both pulse shaping and standardization functions. Each pulse shaper has two inputs. One input is internally connected to the assertion output of an associated multivibrator, while the other, in conjunction with the multivibrator output, can be used to implement various logic forms for delaying and timing applications.

The monostable multivibrator provides both assertion and negation delay pulse widths of 0.7, 2, 5, 10, or 200 microseconds. Other delay widths can be obtained by means of external components.

The pulse shaper provides a 0.6-microsecond assertion pulse; however, wider pulse widths can be achieved through the use of external components. In normal operation, the pulse shaper circuit is triggered on the trailing edge of the delay multivibrator assertion output signal, thus providing a pulse at the end of the delay.

CIRCUIT FUNCTION

The DS-30 PAC (figure 3-10.2) contains two independent and identical pairs of circuits. Each pair, identified as circuit A and circuit B, consists of a delay multivibrator driving a pulse shaper. The following discussion is limited to circuit A.

Delay Multivibrator. Each delay multivibrator circuit contains a single AC input and a node for expansion to 10 inputs. A positive-going transition at the input triggers the multivibrator. The triggering input must remain positive for at least 0.25 microsecond and all inputs must be negative for a minimum of 0.6 microsecond prior to the triggering action.

The delay pulse width is controlled by precision resistors, stable mica and film capacitors, and a zener diode. The delay width is essentially independent of temperature, power supply variations and ripple.

The required recovery period for the multivibrator is less than 80 percent of the delay width and begins immediately after the delay period, regardless of the state of the input signal. The multivibrator can be triggered during the 50 to 80 percent pulse width portion of the recovery period (figure 3-10.3), but yields a narrower than normal output signal. The multivibrator should not be triggered during the 0 to 50 percent delay width portion of the recovery period. For example, if successive 10-microsecond delays are required, the time between triggering should not be less than 18 microseconds. Retriggering during the active delay time does not affect circuit operation.

The circuit provides for the selection of five fixed delays: 0.7, 2, 5, 10, and 200 microseconds. The output delay width is controlled by connecting the appropriate PAC connector pins as outlined in table 3-10.1. These conditions essentially parallel capacitors. Other delays can be obtained by connecting an external capacitor to the PAC connector as indicated in the same table.

Table 3-10.1. Delay Multivibrator Output Delay Widths and Proper Jumper Connections at the PAC Connector

Delay Width	Circuit A Jumper Connections	Circuit B Jumper Connections
0.7 μsec	No jumper connections required	No jumper connections required
2.0 μsec	Pins 19 and 12	Pins 32 and 17
5.0 μsec	Pins 21 and 12	Pins 33 and 17
10.0 μsec	Pins 22 and 12	Pins 34 and 17
200.0 μsec	Pins 23 and 12	Pins 35 and 17
For all other delay widths	Connect an external capacitor between pins 15 and 12*	Connect an external capacitor between pins 25 and 17*

*The value of the external capacitor can be calculated from the following equation:

$$C = 360\ (DW - 0.7)$$

where DW is the delay width in microseconds and C is the capacitance in picofarads (pf). For example: when a 300-microsecond delay is required:

$$C = 360\ (300 - 0.7) = 108,000\ \text{pf} = 0.11\ \mu\text{f}$$

Pulse Shaper. The pulse shaper circuit is an AC-coupled inverter which provides a standard 0.6-microsecond assertion pulse output. The circuit is triggered on the positive transition of the input signal and the pulse width is determined by an RC network. The pulse width can be increased by adding a parallel capacitor to the capacitor provided on the PAC as shown in table 3-10.2. The value of the parallel capacitor required for a specific output pulse width can be calculated from the following equation:

$$C = (PW - 0.6) \times 1.07 \times 10^3$$

where PW is the pulse width in microseconds and C is the capacitance in picofarads (pf). For example, if a 10-microsecond pulse is required:

$$C = (10 - 0.6) \times 1.07 \times 10^3 = 9.4 \times 1.07 \times 10^3 = 10,058\ \text{pf} = 0.01\ \mu\text{f}$$

The parallel capacitor can be added in two ways: installed in a space provided on the PAC referred to as CX or externally connected to the PAC connector. Refer to table 3-10.2 for applicable connections and to figure 3-10.4.

Table 3-10.2 Pulse Shaper, Jumper Connections at the PAC Connector to Change Pulse Width

Method	Circuit A Jumper Connections	Circuit B Jumper Connections
Add parallel capacitors in space marked CX	Pins 10 and 8	Pins 24 and 29
Add external capacitor	Connect capacitor between pins 6 and 8	Connect capacitor between pins 31 and 29

Both inputs to the pulse shaper must conform to the following general rules:

a. The input waveform must be positive for a time equal to or greater than the required output pulse width.

b. The input waveform must be negative, prior to going positive, for a time equal to or greater than the desired output pulse width.

As the preceding rules imply, minimal cases require that the input waveform be symmetrical. Examples of the input waveforms required are shown in the a and b portions of figure 3-10.5.

The input leads to the pulse-shaper input circuit should be as short as possible to prevent noise and spurious transients. In normal operation, the pulse-shaper circuit is triggered on the trailing edge of the delay multivibrator assertion output signal, thus providing a pulse at the end of a delay. In most applications, the available input to the pulse shaper is used to inhibit the circuit (c, figure 3-10.5); that is, an applied logic ZERO (0 V) at the available input prevents triggering of the pulse shaper. The additional pulse-shaper input can be used to generate output pulses during the active delay period (d, figure 3-10.5).

SPECIFICATIONS

Multivibrator Specifications

Input Loading

2 unit loads each

Frequency of Operation

DC to $\left(\frac{1}{1.8 \times DW}\right)$ or 600 KC, whichever is less, where DW is delay width in μsec

Circuit Delay

Negation output: 0.25 μsec (max)
0.15 μsec (typ)

Assertion output: 0.15 μsec (max)
0.10 μsec (typ)

Output Drive Capability

Assertion: 2 unit loads each

Negation: 4 unit loads each and 200 pf stray capacitance

Output Waveform Characteristics

Assertion Output (negative pulse measured from -0.6 V to -4.5 V)

Rise time: 0.15 μsec or 0.2% of pulse width, whichever is longer

Fall time: 0.15 μsec typ

NOTE

A positive-going edge, adequate for triggering of other DS-30s, is assured on the trailing edge of assertion output up to 1 millisecond wide. For wider pulses (longer delays), inversion of the negation output is recommended for triggering of AC inputs and other DS-30s.

Negation Output (positive pulse)

Rise time: 0.06 μsec (typ)

Fall time: 0.15 μsec (typ)

SPECIFICATIONS (Continued)

Multivibrator Specifications (Cont)

Delay Width Specifications:

Internally Provided Delay Widths
0.7, 2, 5, 10 and 200 μsec

Delay Width Accuracy

±10%

Recovery Time

80% of delay width (figure 3-10.3)

Delay Width Variations

(All independently specified)

Short term stability (8 hours): <1%
Jitter (delay to delay): <0.1%
Long term stability (reproducibility over three months): <2%
Temperature variation:
-20° to +25°C: -7%
+25° to +55°C: +8%

Pulse Shaper Specifications

Input Loading

3 unit loads each

Standard Output Pulse Width

0.6 μsec

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Pulse Width (max)

Limited only by the general rules listed in table 3-10.2

Output Drive Capability

Assertion: five unit loads and 100 pf stray capacitance each output

DS-30 PAC Specifications

Current Requirements

-18 V 110 ma
- 6 V 35 ma (reverse current into supply)
+12 V 11 ma

Total Power

1.7 watts

Polarization

Pins 14 and 32

Handle Color Code

Long: Yellow

Short: Green

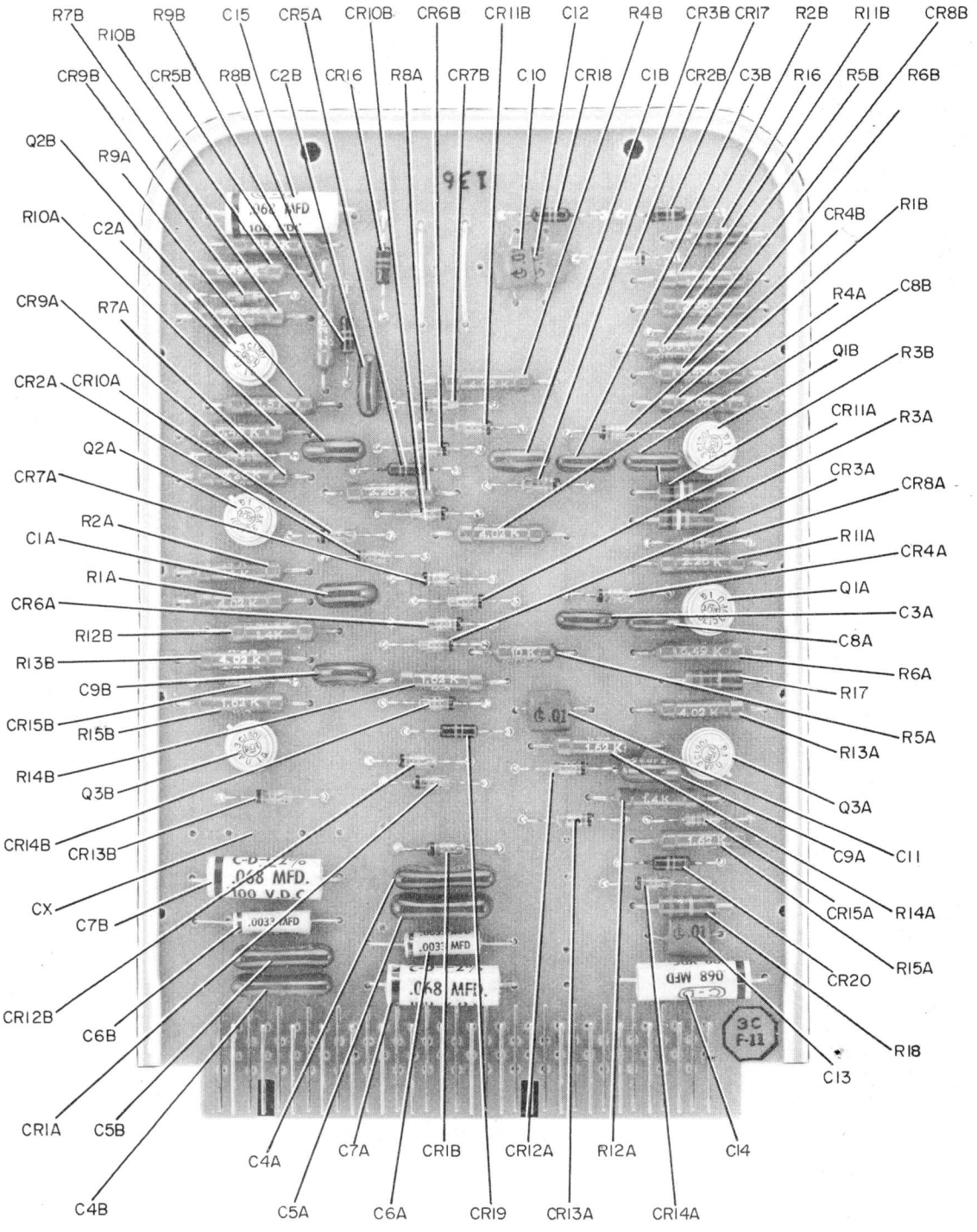


Figure 3-10.1. Delayed Pulse PAC, Model DS-30, Parts Location

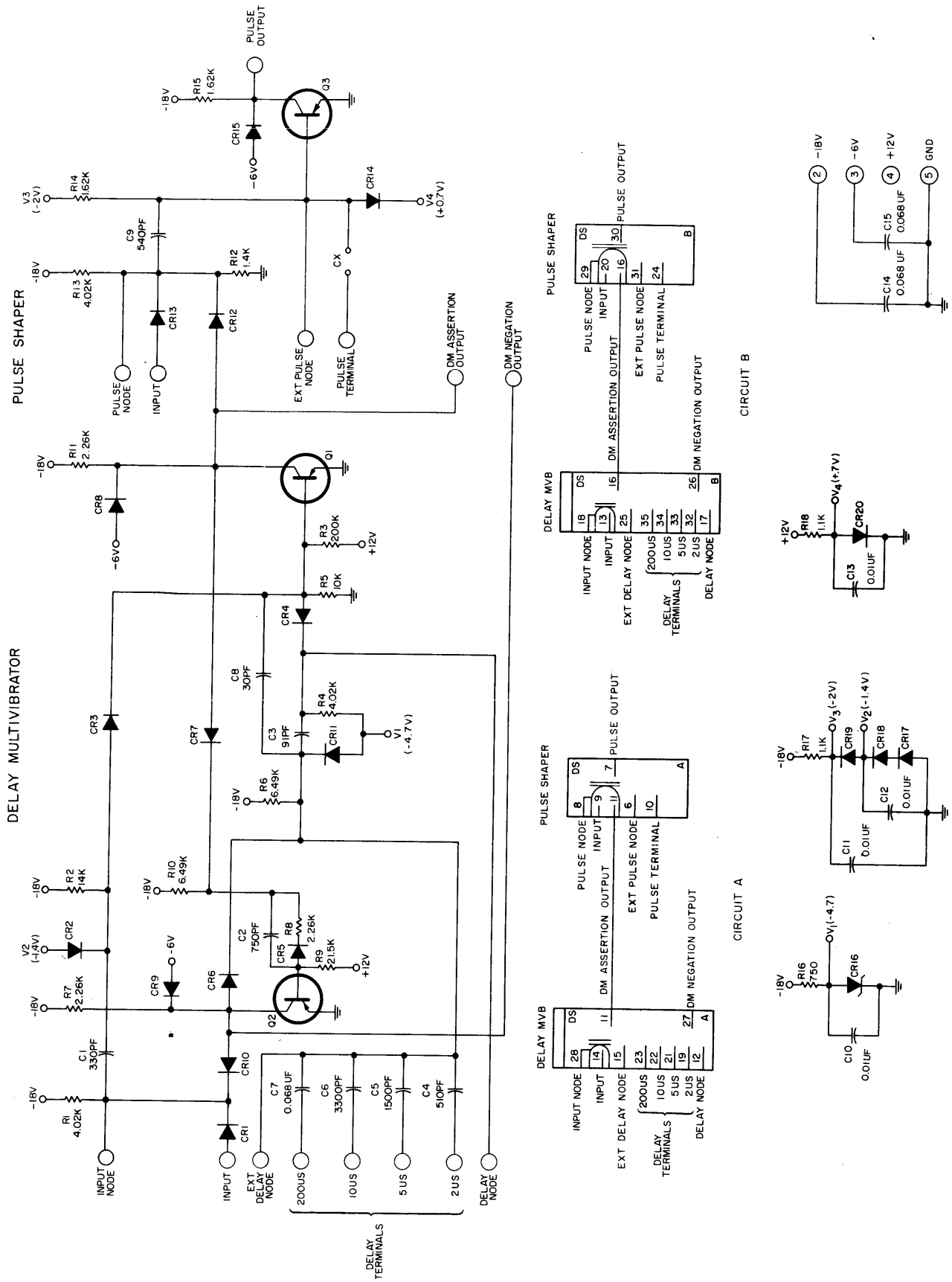


Figure 3-10.2. Delayed Pulse PAC, Model DS-30, Schematic and Logic Diagram

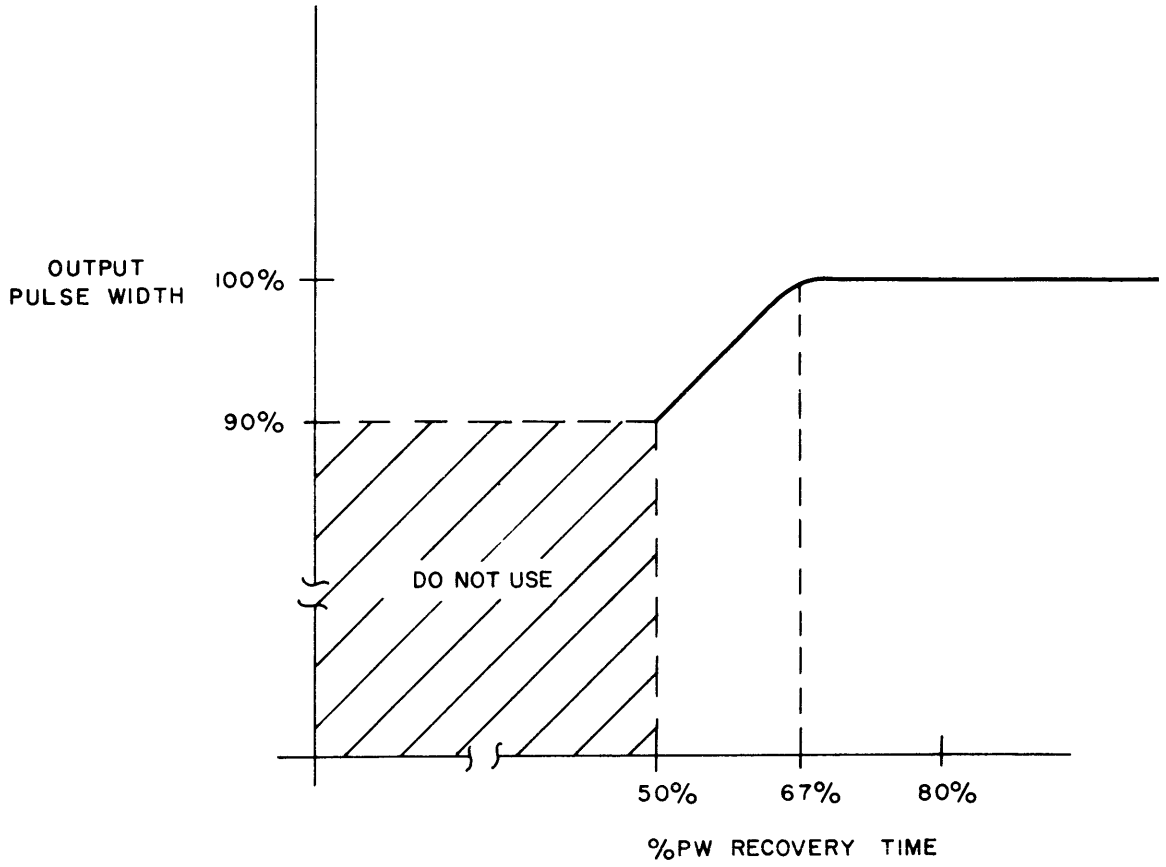
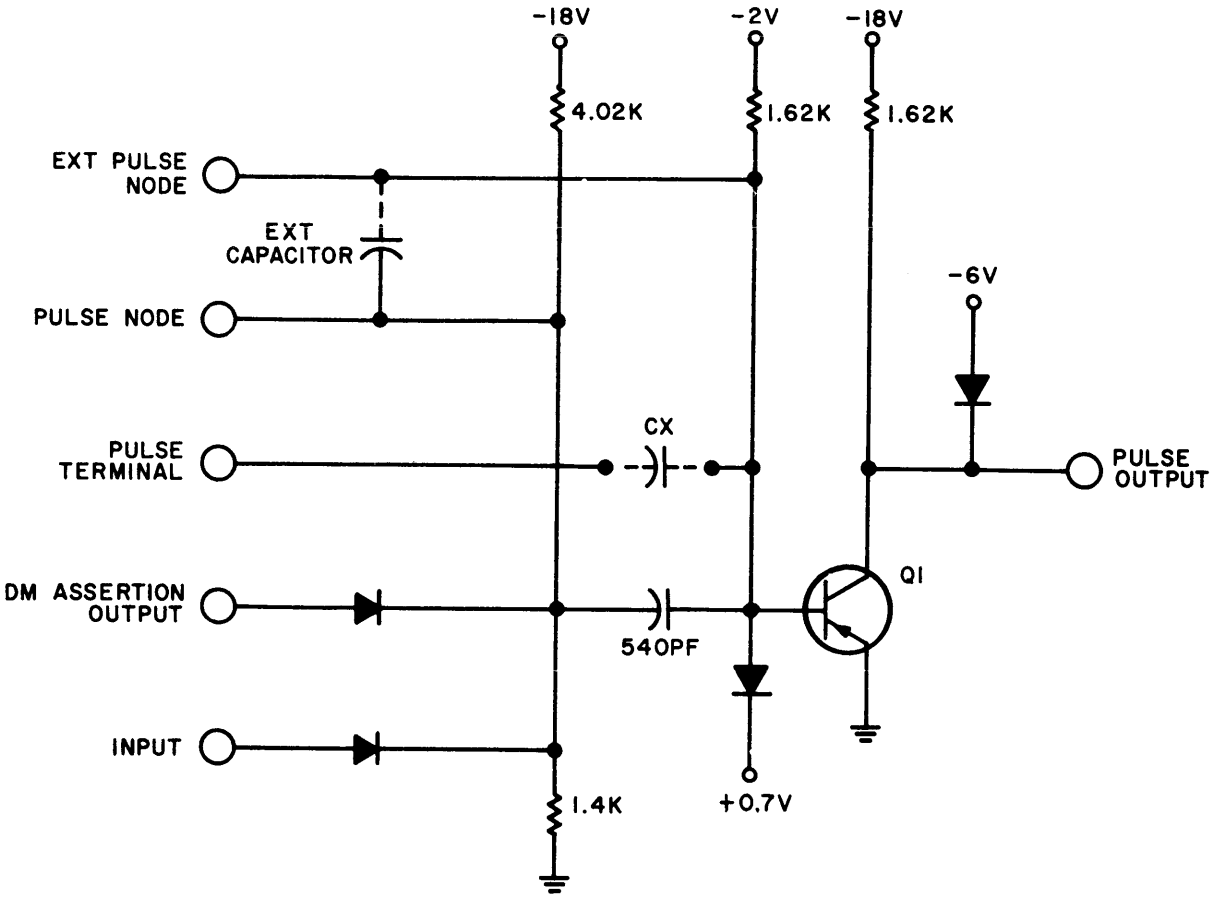


Figure 3-10.3. Typical Delay Multivibrator Recovery Curve

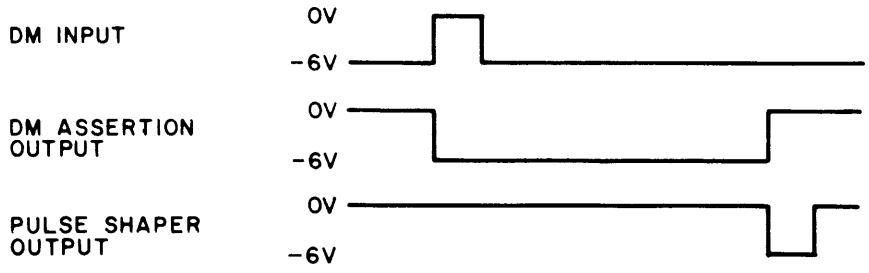


THE VALUE OF THE EXTERNAL CAPACITOR OR CX CAN BE CALCULATED FROM THE FOLLOWING FORMULA $C = (PW - 0.6) \times 1.07 \times 10^3$

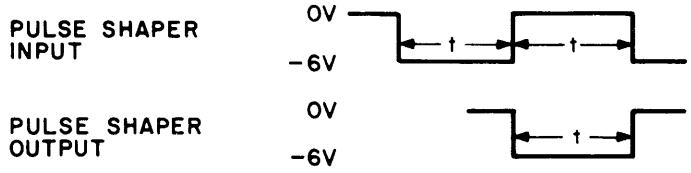
WHERE : PW IS THE PULSE WIDTH IN US AND C IS THE CAPACITANCE IN PF

EXAMPLE: A 10 US PULSE IS REQUIRED $C = (10 - 0.6) \times 1.07 \times 10^3 = 9.4 \times 1.07 \times 10^3$
$= 10{,}058$ PF $= 0.01$ UF

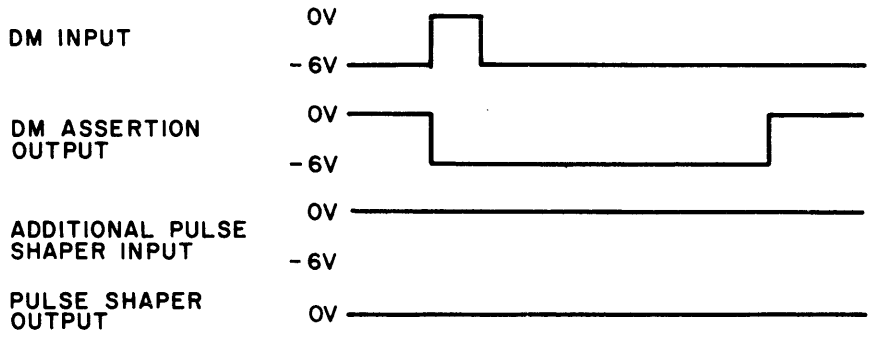
Figure 3-10.4. Pulse Shaper Using External Capacitor



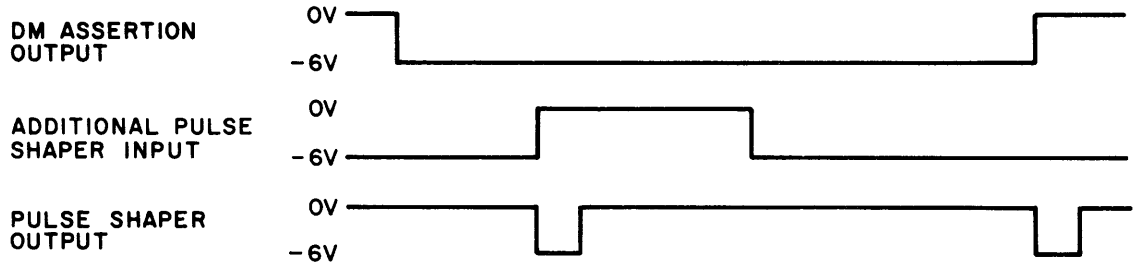
a. Normal Operation



b. Minimum Input For An Output Pulse Width t



c. Using Additional Pulse Shaper Input To Inhibit Pulse Shaper



d. Using Additional Pulse Shaper Input To Generate Output Pulses

Figure 3-10.5. Model DS-30 Waveforms

3-11 ADJUSTABLE DELAYED PULSE PAC, MODEL DS-30A

GENERAL DESCRIPTION

The Adjustable Delayed Pulse PAC, Model DS-30A (figure 3-11.1), is similar to the DS-30 PAC with one exception. The delay multivibrator circuit on the DS-30A PAC contains a variable resistor to provide additional adjustment of the output delay width from 60 percent of the nominal width to three times the nominal width as indicated in the DS-30A specifications. For a general description and a discussion of the circuit function of the DS-30A, refer to paragraph 3-10 covering the DS-30.

SPECIFICATIONS

Multivibrator Specifications

Input Loading

2 unit loads each

Output Waveform Characteristics

Assertion Output:

Rise time: 0.2 μsec or 0.3% of DW, whichever is greater
Fall time: 0.15 μsec (typ)

NOTE

A positive-going edge, adequate for triggering another DS-30A, is assured on the trailing edge of the DS-30A assertion pulses up to 1 millisecond wide. For wider pulses (longer delays), inversion of negation output is recommended for triggering of AC inputs and DS-30As.

Negation Output:

Rise time: 0.06 μsec (typ)
Fall time: 0.15 μsec (typ)

Delay Width Specifications:

(All independently specified)

Internally Provided Delay Widths (nominal)

0.7, 2, 5, 10 and 200 μsec

Delay Width Adjustment

0.6 of nominal to 3 times nominal

Delay Width Accuracy

(All independently specified, assuming a fixed potentiometer setting)

Short term stability (8 hours): <1%
Jitter (delay to delay): <0.1%
Long term stability (reproducibility over three months): <2%
Temperature variation
-20° to +25°C: -7%
+25° to +55°C: +8%

Output Drive Capability

Assertion: (negative pulses) 1 unit load

Negation: (positive pulse) 4 unit loads

Frequency of Operation

DC to $\left(\frac{1}{1.8 \times DW}\right)$ or 500 KC, whichever is less, where DW is delayed pulse width in μsec.

Recovery Time

80% of delay width (figure 3-11.1)

Potentiometer Rotation

CW rotation increases delay width

SPECIFICATIONS (Continued)

Pulse Shaper Specifications

Input Loading

2 unit loads

Standard Output Pulse Width

0.6 μsec

Output Drive Capability

Assertion: 5 unit loads and
100 pf stray capacitance

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Pulse Width (max)

Same as DS-30

DS-30 Specifications

Current Requirements

-18 V	100 ma
- 6 V	35 ma (reverse current into supply)
+12 V	11 ma

Total Power

1.5 watts

Polarization

Pins 14 and 32

Handle Color Code

Long: Yellow
Short: Green

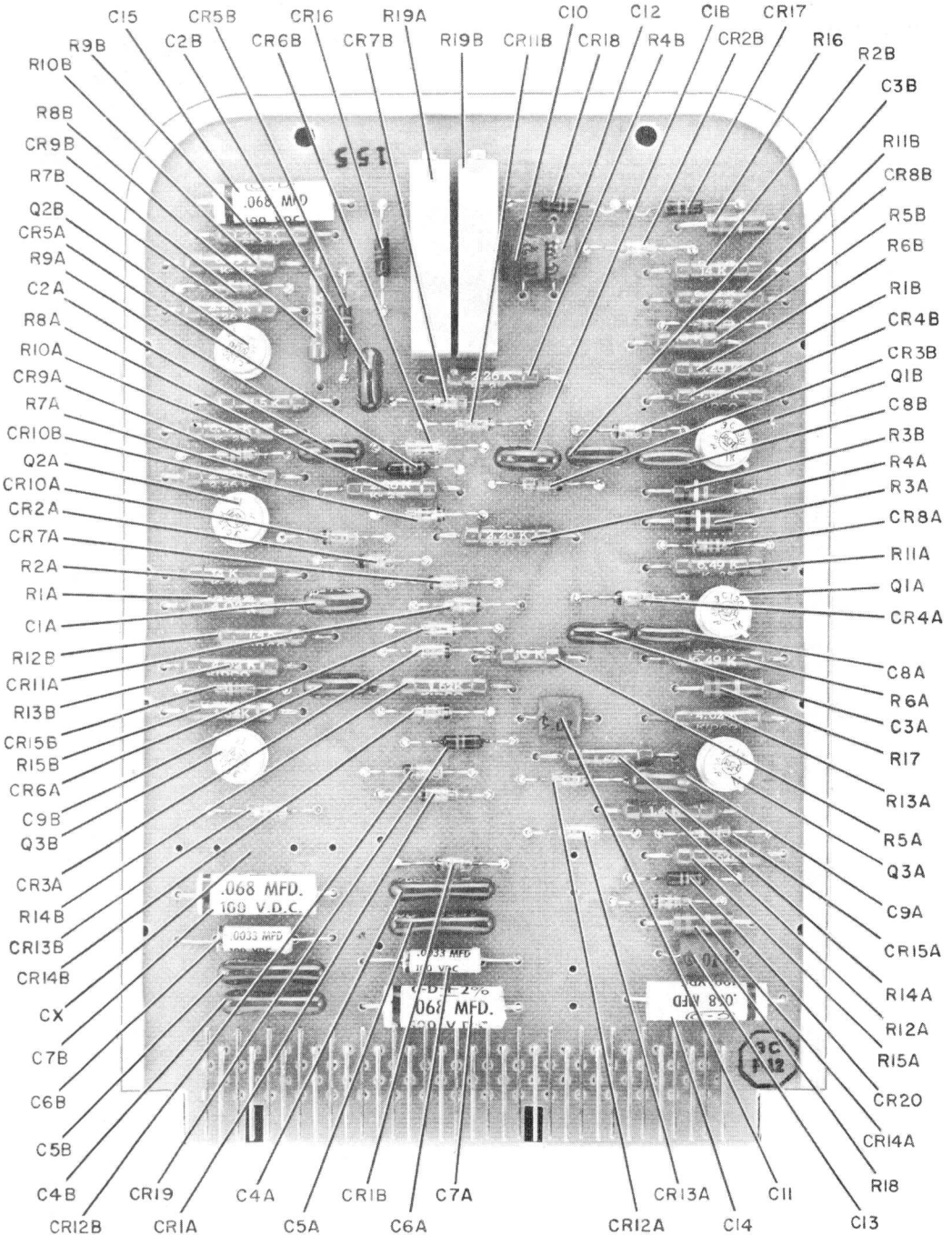


Figure 3-11.1. Adjustable Delayed Pulse PAC, Model DS-30A, Parts Location

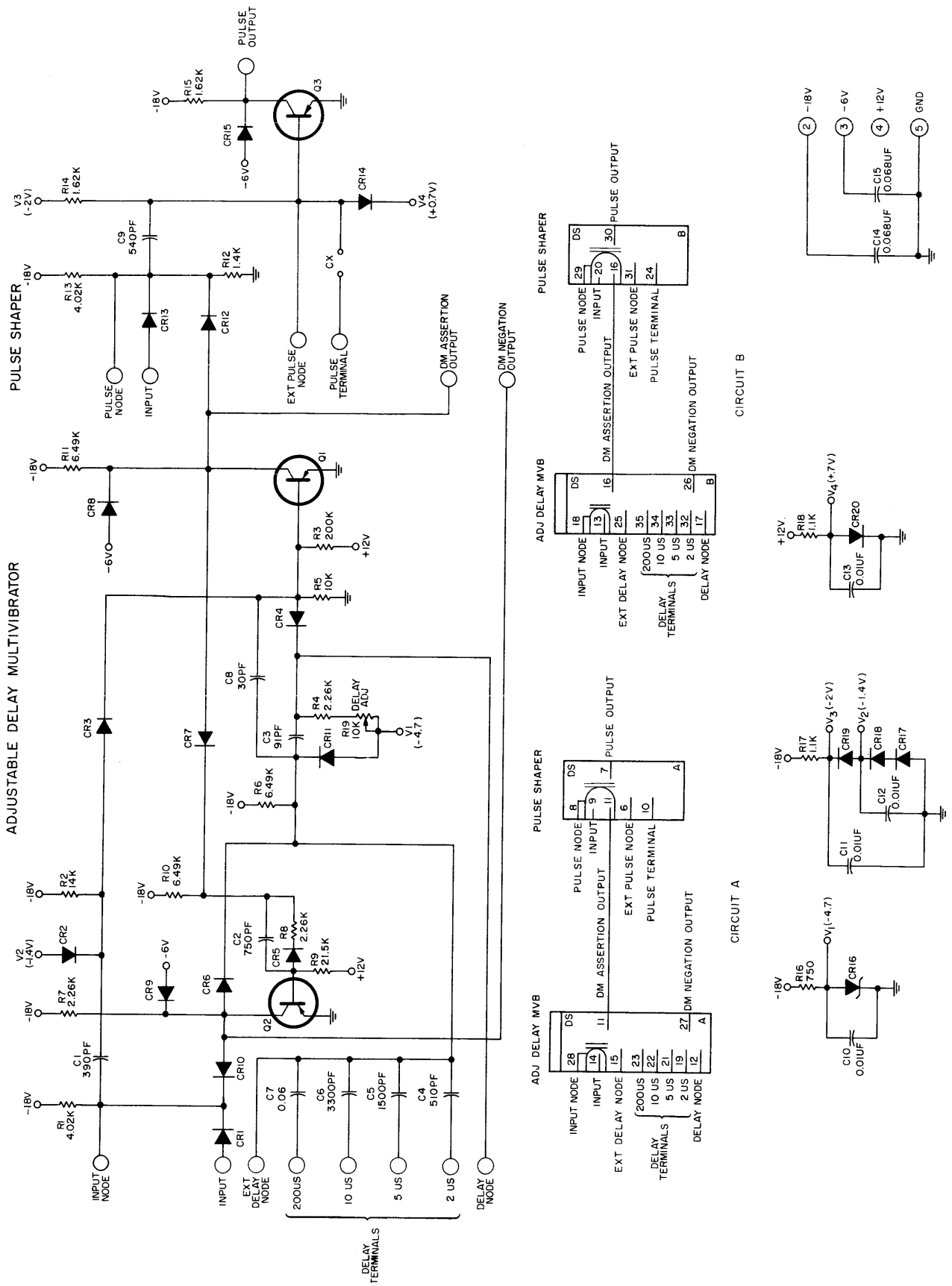


Figure 3-11.2. Adjustable Delayed Pulse PAC, Model DS-30A, Schematic and Logic Diagram

3-12 GATED FLIP-FLOP PAC, MODEL FA-30

GENERAL DESCRIPTION

The AC Gated Flip-Flop PAC, Model FA-30 (figures 3-12.1 and 3-12.2), contains four identical, independent, bistable circuits which respond to transitional input signals. These circuits can be wired to perform any logic function required of a flip-flop, such as counting, shifting, accumulating, etc. Each stage has three independent, AC-coupled inputs composed of a reset input and two set inputs. Level control inputs are provided with the AC reset input and one of the AC set inputs to permit gating of set and reset information. The AC set and reset inputs can be wired separately in applications requiring independent setting and resetting of the flip-flop. The inputs can also be tied together to implement logic functions, such as shifting, complementing, parallel information drop-in, etc. These applications are described under Circuit Function. A DC reset input common to the four flip-flop circuits is provided to permit simultaneous clearing of all four stages.

CIRCUIT FUNCTION

The four FA-30 circuits (figure 3-12.3) are identical. Each stage consists of two cross-coupled NAND gates with AC-coupled inputs.

AC Set (Reset) Input and Level Control. The AC set (reset) input and associated level control form a two-input AC gate which, when properly activated, causes the flip-flop to assume the set (reset) state. Proper activation of the gate requires that the level control be a ZERO (0 V) and a positive-going 6-volt step be applied to the AC input as described under Timing. The 6-volt step is differentiated and applied to the flip-flop input through a biased diode. If the level control is a ONE (-6 V), the differentiated step is blocked. The additional AC set input also forms a two-input AC gate with the level control internally wired to the set output. The flip-flop is unconditionally set each time a positive-going 6-volt step is applied to this AC set input.

Timing. There are two modes of operation for an AC input with a level control. The first is the pulse mode of operation, which is defined as the condition where the level control signal switches negative when the AC input signal is positive. The required AC input signal for this mode of operation is a negative pulse with a minimum pulse width of 0.4 microsecond.

The second mode of operation is the step mode, which is defined as the condition where the level control switches negative when the AC input signal is negative. This mode requires that the AC input signal remain negative for a minimum of 1.4 microsecond after the level control switches negative. Figure 3-12.4 illustrates the waveforms associated with both modes of operation for single pedestal gates.

Shifting. Each stage of the FA-30 can be wired to perform the function of shifting. The AC reset inputs and the AC set inputs with a level control are connected to form the shift input. The level control inputs and the outputs of the four stages are then connected in a shift register configuration as illustrated in figure 3-12.5. Input information to the register is applied to the level control inputs of the first stage and must conform to the specifications outlined under Timing. The shift input is sensitive to positive-going, 6-volt

steps and incorporates trailing edge triggering for negative shift pulses (figure 3-12.6). This allows the output of the register to be gated with the shift signal without the need for delay circuits or two-phase clocks.

Complementing. Each stage of the FA-30 can be wired to perform the function of complementing. This is accomplished by connecting the AC reset input to either of the two AC set inputs, thus forming the complement input. The reset level control is connected to the reset output. If the AC set input with a level control is used to form the complement input, the set level control must be connected to the set output. However, if the other set input is used, no connection is required since its level control is internally wired to the set output. The complement input is sensitive to positive-going, 6-volt steps. For trailing edge triggering of the flip-flop, negative signals with a minimum duration of 0.4 microsecond should be used. For leading edge triggering, positive signals of 0.25 microsecond minimum duration are required. Figure 3-12.7 illustrates the FA-30 wired as a binary counter with each stage performing the complementing function.

Parallel Information Drop-In. Each stage of the FA-30 can be wired to accept information in parallel with the advantages of built-in pulse dodging and no additional gating required. Parallel information drop-in is accomplished by connecting the AC reset input to the AC set input with a level control. The combined inputs of each stage are then tied together to form a common input. The input information should be in the form of complementary logic signals, such as the outputs of any S-PAC flip-flop, and should be connected to the level control inputs. A level control input at ZERO causes the flip-flop to assume the state associated with that level control when the common input becomes positive; that is, the flip-flop becomes set if the set level control is 0 volt. If the input data is presented from the output of a gate (signal-ended), an inverter must be provided between the set and reset level control inputs.

The set and reset level controls should be connected to the reset and set outputs, respectively, of the driving flip-flop. With both level controls at -6 volts or disconnected, the common input is disabled. If both level controls are at ZERO when the common input becomes positive, the flip-flop assumes an indeterminate state. Information is placed in the FA-30 register on each positive transition of the common input signal. Figure 3-12.8 illustrates the FA-30 wired to accept information in parallel. The input waveform requirements are presented in the discussion under Timing.

Common Reset. A 1-microsecond positive pulse applied to the common reset input clears (resets) the four counter stages simultaneously.

NOTE

In all applications of the FA-30, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

AC set or reset inputs: 2 unit loads each used separately
Level control input: 1/2 unit load each
Common (DC) reset input: 4 unit loads

Input Waveform Requirements

Common reset: 1 μsec min at logic ZERO

Circuit Delay

(Measured at -3 V)
0.15 μsec (typ) Reset input to set output
0.25 μsec (max) or set input to reset output.

0.06 μsec (typ) Set input to set output or
0.10 μsec (max) reset input to reset output.

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Total Power

2.7 watts

Polarization

Pins 4 and 32

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 137 ma
-6 V 64 ma (reverse current into supply)
+12 V 5 ma

Handle Color Code

Long: Blue

Short: Brown

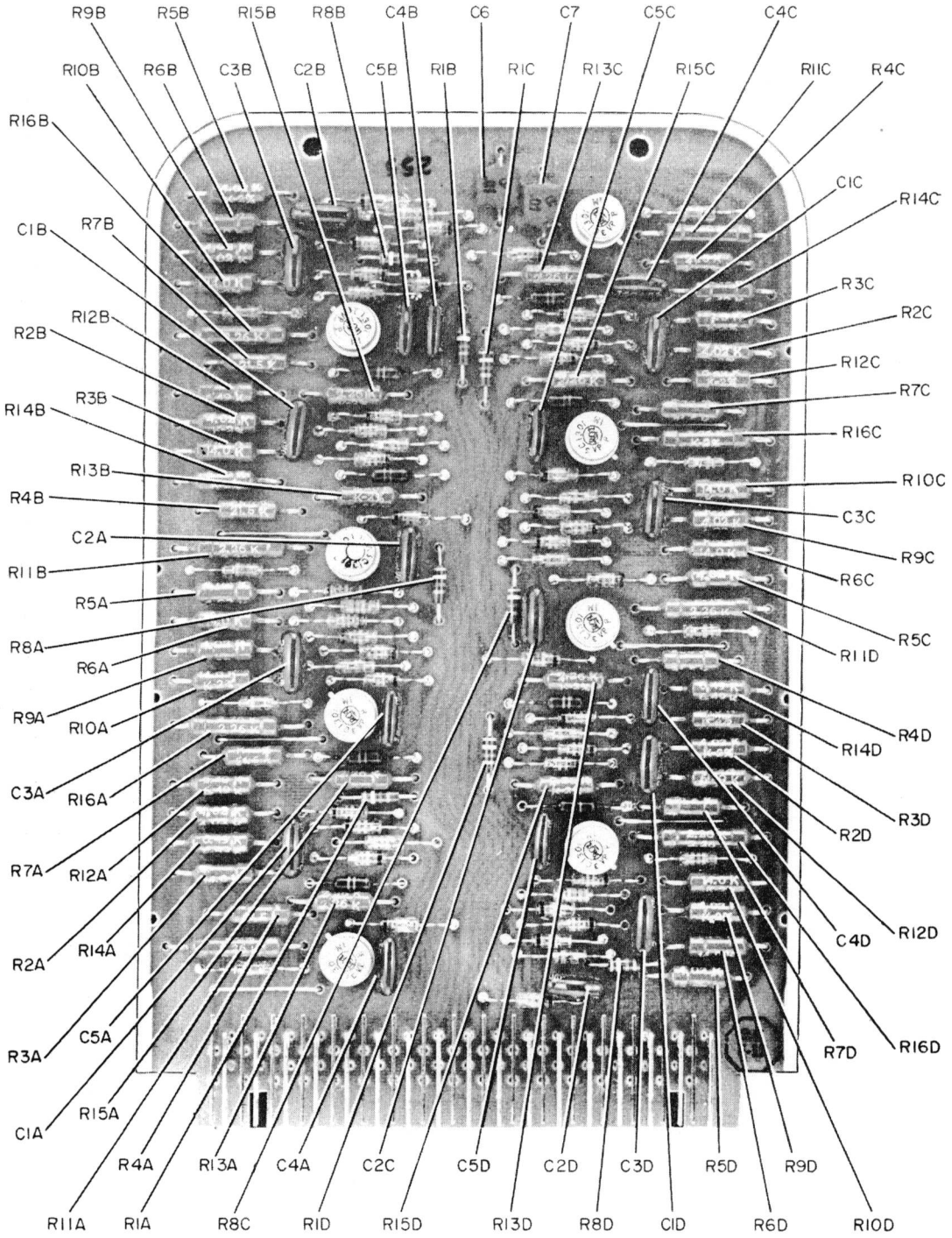


Figure 3-12.1. Gated Flip-Flop PAC, Model FA-30,
Parts Location (Capacitors and Resistors)

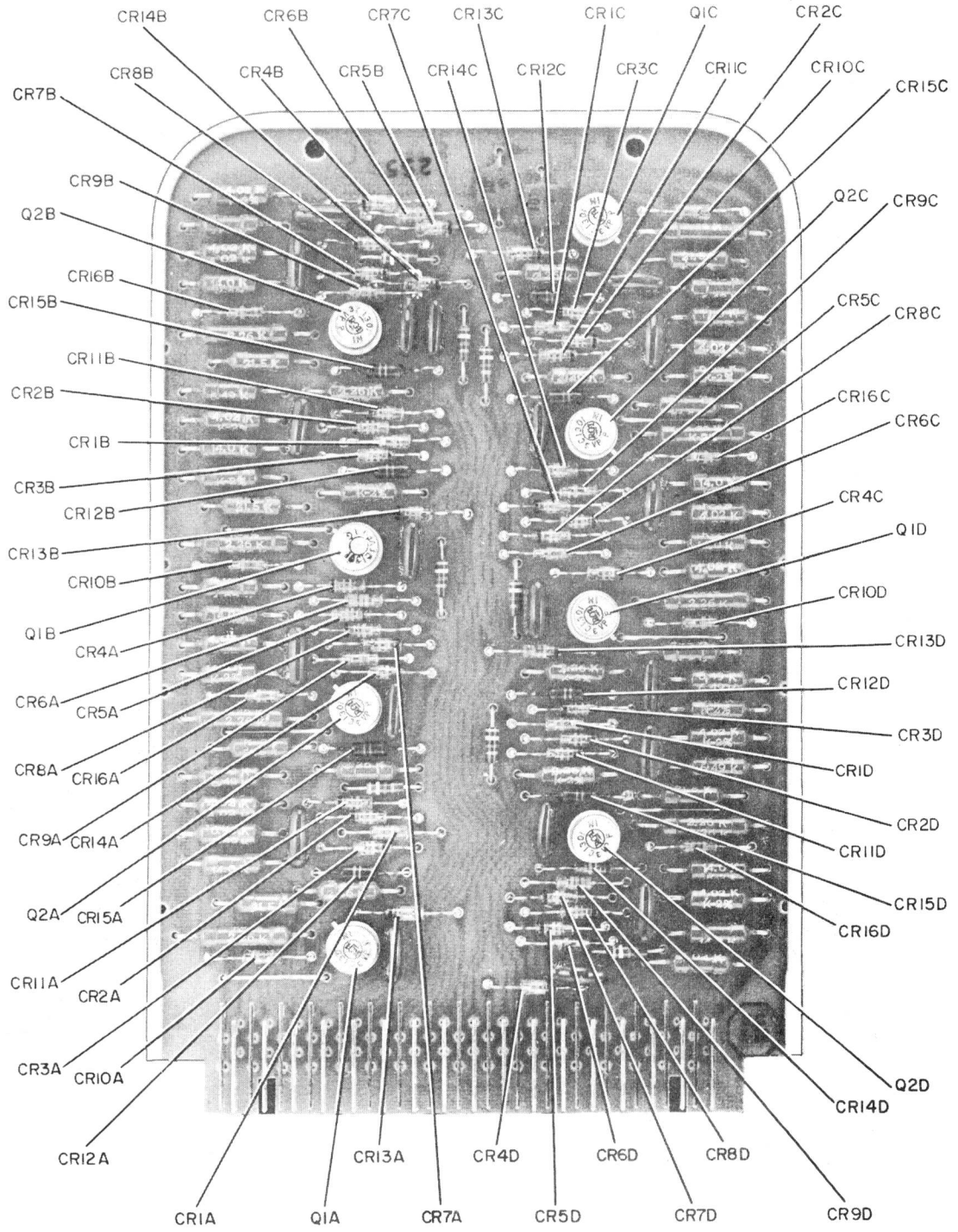


Figure 3-12.2. Gated Flip-Flop PAC, Model FA-30,
Parts Location (Diodes and Transistors)

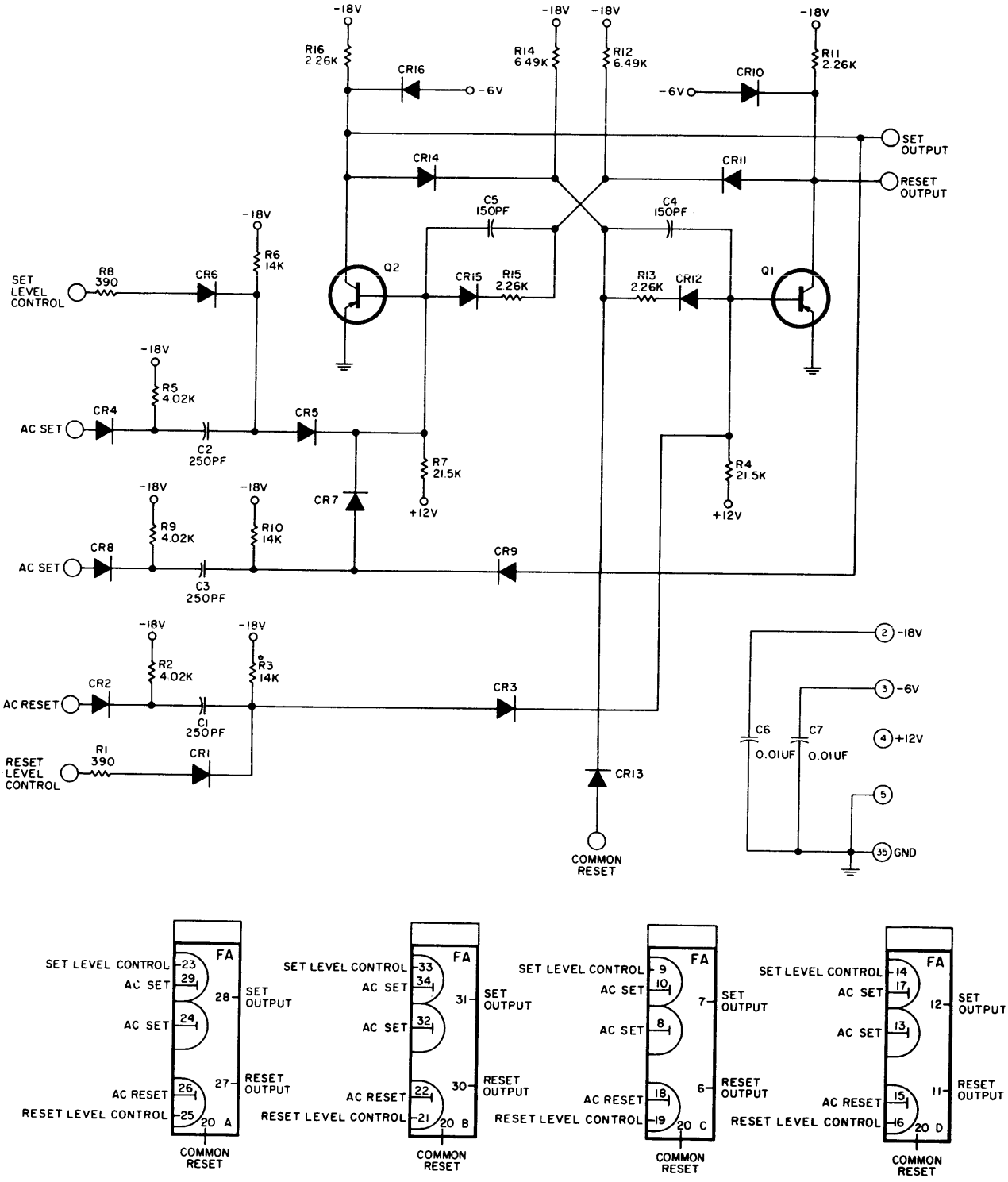


Figure 3-12.3. Gated Flip-Flop PAC, Model FA-30, Schematic and Logic Diagram

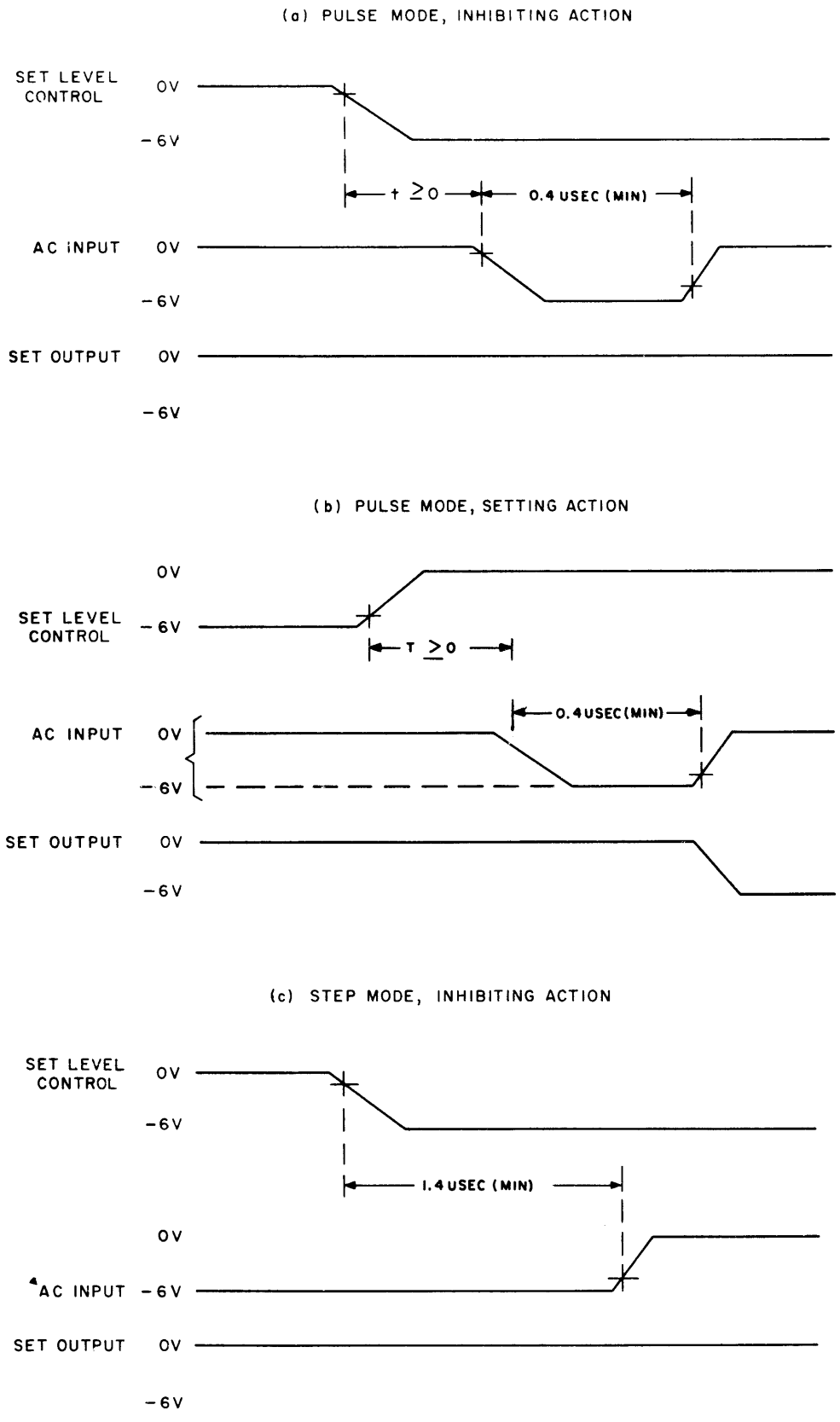


Figure 3-12.4. Timing for a Single Pedestal Gate

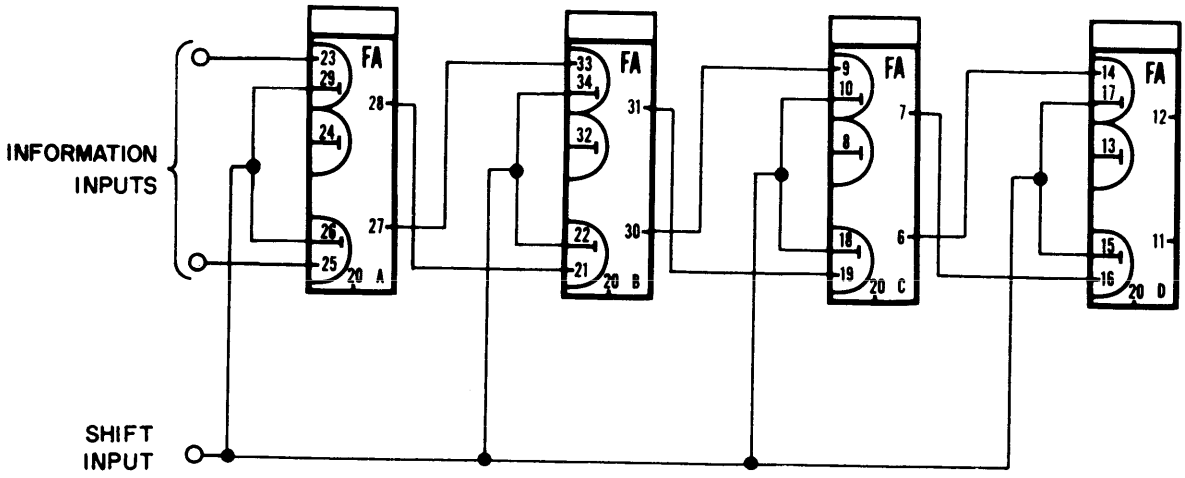


Figure 3-12.5. Model FA-30 Wired as Shift Register

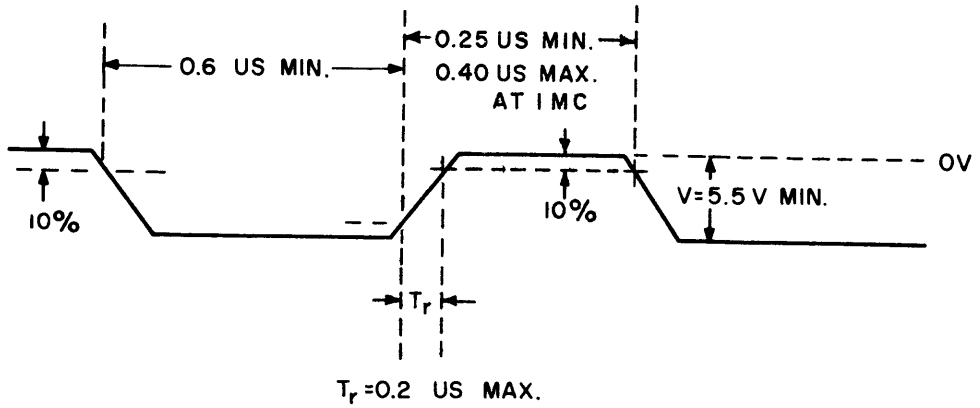


Figure 3-12.6. Trailing Edge Trigger Mode Signal Requirements

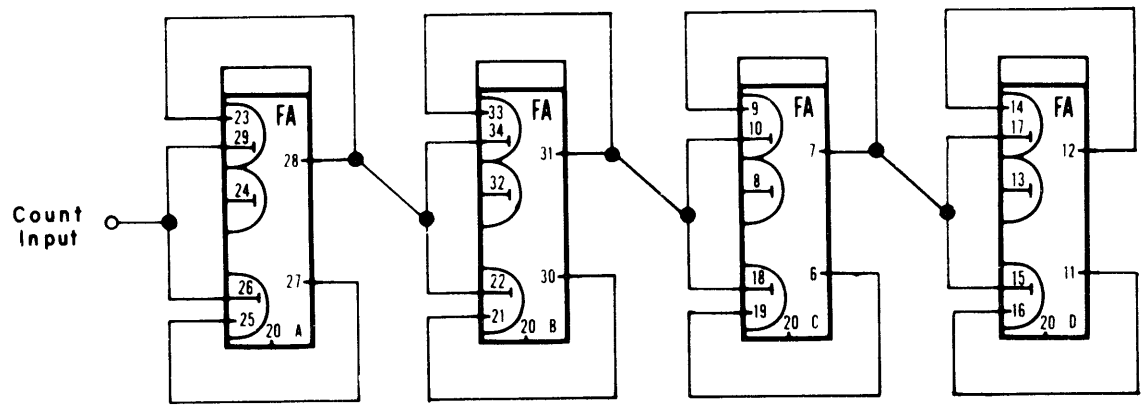


Figure 3-12.7. Model FA-30 Wired as Binary Counter

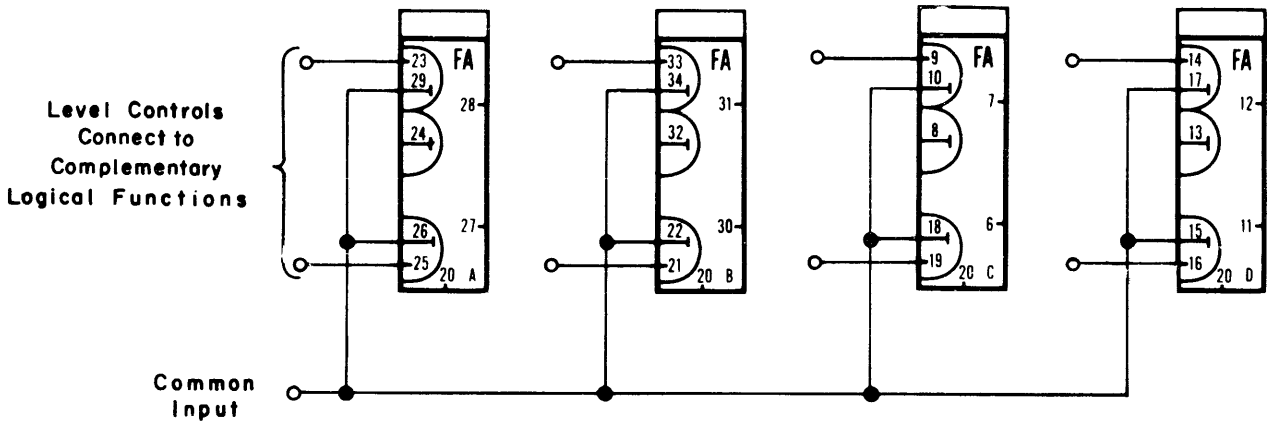


Figure 3-12.8. Parallel Information Drop-In

3-13 BASIC FLIP-FLOP PAC, MODEL FF-30

GENERAL DESCRIPTION

The Basic Flip-Flop PAC, Model FF-30 (figures 3-13.1 and 3-13.2), contains four identical, independent, bistable circuits for use as input-output registers or for any logic application in which complementing, shifting, etc., is not required. One DC set and two DC reset inputs are provided. Each input is expandable to 10 by connecting diode clusters to the appropriate node.

CIRCUIT FUNCTION

The basic flip-flop circuit (figure 3-13.3) consists of two cross-coupled NAND gates. When all DC inputs are at ONE (-6 V), the flip-flop assumes one of its bistable states. Applying ZERO (0 V) to a DC set or reset input for 0.25 microsecond or longer causes the flip-flop to assume the set or reset stage, respectively, unless already in that state. The flip-flop may be both set and reset in a 1-microsecond interval.

If both set and reset DC inputs are held at ZERO, a third state (unstable) exists in which both set and reset outputs are at ONE.

NOTE

In all applications of the FF-30, pin 35 should be connected to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

(Measured at -3 V)

0.15 μsec (typ) Reset input to set output
0.25 μsec (max) or set input to reset output.

0.06 μsec (typ) Set input to set output or
0.10 μsec (max) reset input to reset output.

Output Waveform Characteristics

Rise Time: 0.1 μsec (typ)
Fall Time: 0.15 μsec (typ)

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Total Power

1.3 watts

Polarization

Pins 16 and 18

Current Requirements

-18 V 75 ma
-6 V 23 ma (reverse current into supply)
+12 V 5 ma

Handle Color Code

Long: Blue
Short: Blue

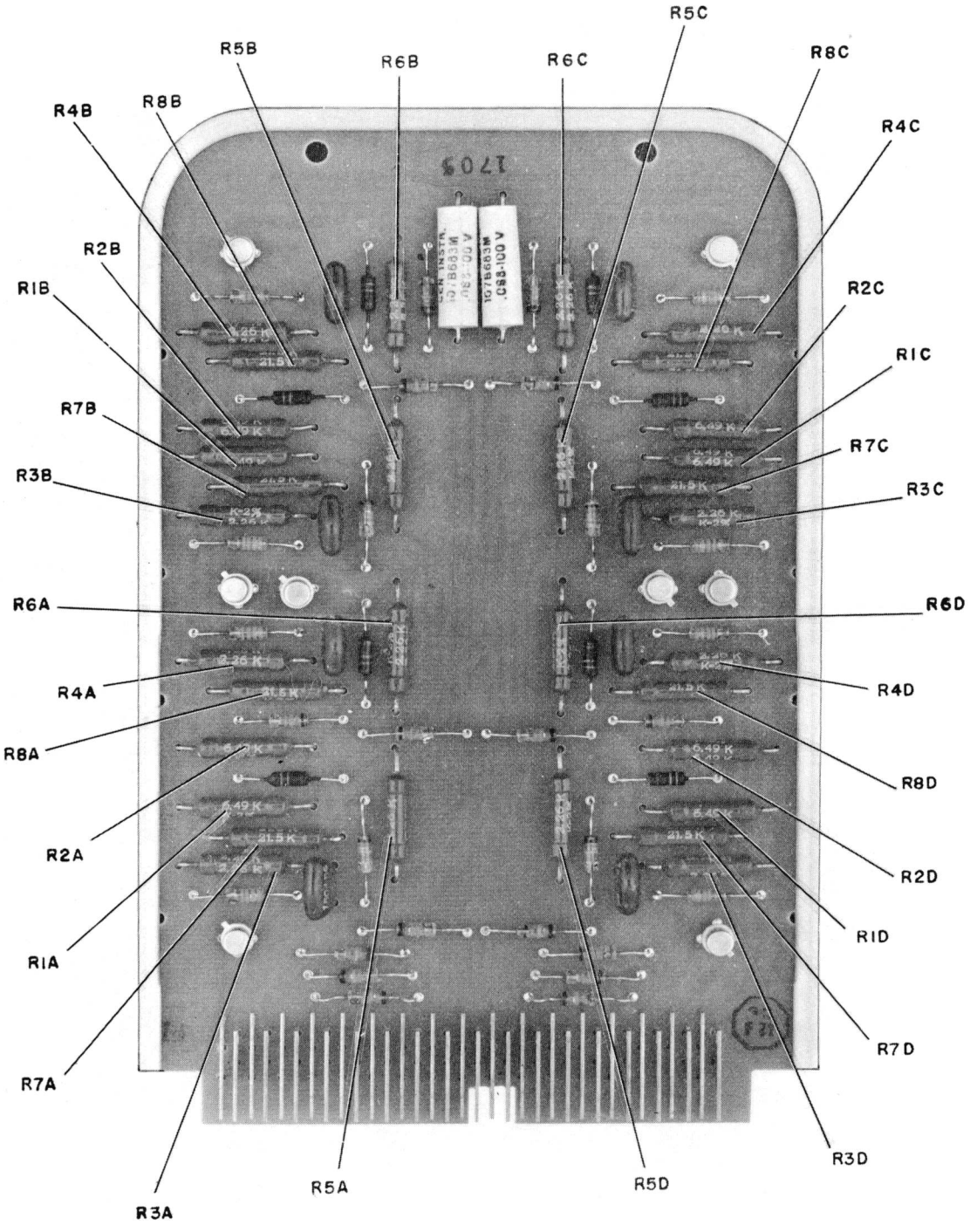


Figure 3-13.1. Basic Flip-Flop PAC, Model FF-30, Parts Location (Resistors)

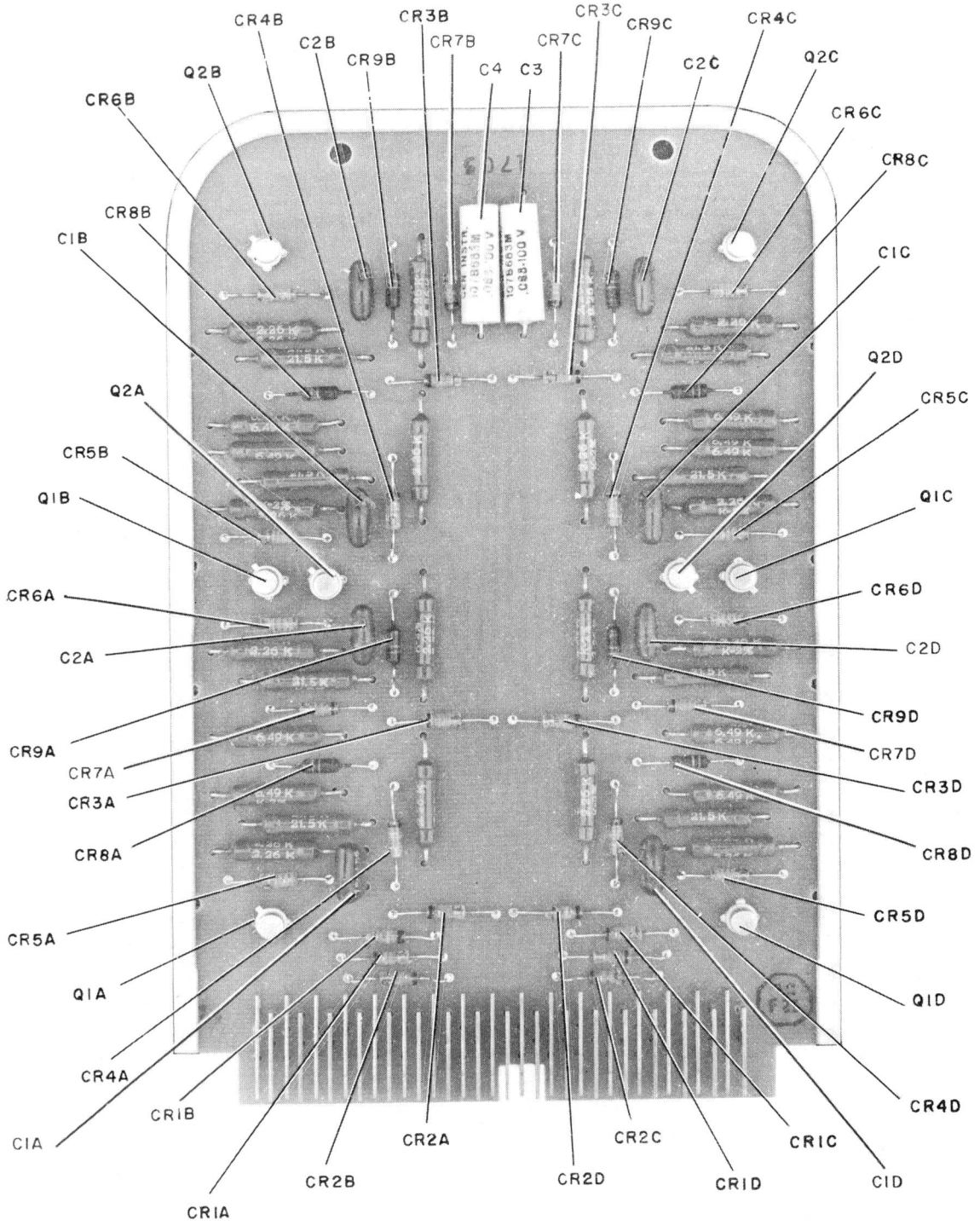


Figure 3-13.2. Basic Flip-Flop PAC, Model FF-30, Parts Location (Capacitors, Diodes, and Transistors)

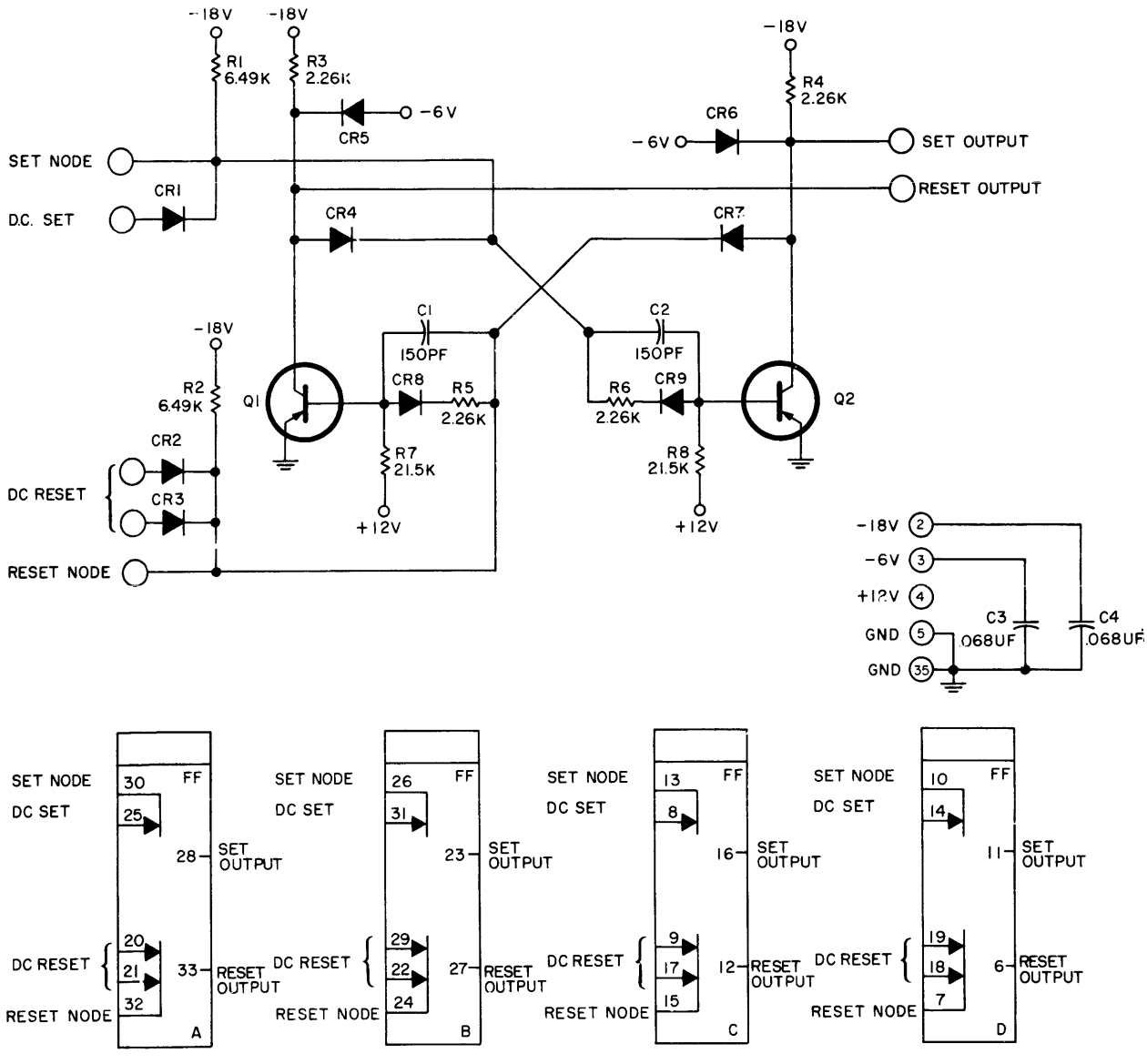


Figure 3-13.3. Basic Flip-Flop PAC, Model FF-30, Schematic and Logic Diagram

3-14 MASTER CLOCK PAC, MODEL MC-30

GENERAL DESCRIPTION

The Master Clock PAC, Model MC-30 (figure 3-14.1), contains a crystal-controlled oscillator, a level restorer, a pulse shaper, and a pulse amplifier. The standard operating frequency of the MC-30 is 1 megacycle, but this PAC can be modified to operate at any specified frequency between 100 kilocycles and 1 megacycle upon request. The MC-30 PAC has both assertion and negation pulse outputs set for a duration of 0.6 microsecond. The output pulse width can be expanded to 2 or 5 microseconds by jumper connections at the PAC connector.

Additional control of the MC-30 is provided by the shaper inhibit input which inhibits the output pulse train. Connections for external crystal and external frequency control and a sync output are also available at the PAC connector. The basic purpose of the external frequency input is to permit the MC-30 to be triggered by an external clock source. The external crystal input is provided to permit off-PAC mounting or oven placement for the crystal and is located at pins 13 and 15 of the PAC connector.

CIRCUIT FUNCTION

The circuit functions (figure 3-14.2) of the oscillator circuit, pulse shaper, external frequency input, and synchronous clock control are discussed in the following paragraphs.

Oscillator Circuit. The frequency generating section of the MC-30 is a parallel-resonant, 1-megacycle crystal oscillator. An external frequency source can drive the MC-30 PAC, provided the crystal is removed. Following the crystal oscillator is an inverter circuit which clamps the oscillator output to S-PAC signal levels. The inverter output (sync) is gated with the shaper inhibit input to drive the pulse shaper. The sync output at pin 12 of the PAC connector can be used for synchronous clock control. A ONE (-6 V or no connection) applied to the shaper inhibit (pin 28) allows every positive transition of the sync output to trigger the pulse shaper. A ZERO applied to pin 28 inhibits the pulse shaper.

Pulse Shaper. The pulse shaper is a one-shot multivibrator circuit which produces the desired pulse width. The pulse width can be changed by jumper connections at the PAC connector. To set the pulse width to 2 microseconds, pin 16 should be connected to pin 30. For a 5-microsecond pulse width, pin 14 should be connected to pin 30. An external capacitor can be connected to pins 17 and 30 for other pulse widths. The value of the external capacitor may be derived from the following equation:

$$C = 370\,(PW - 0.64) \qquad PW\ Max = \frac{1}{1.6 \times Freq}$$

where:

PW = pulse width in μsec
C = capacitance in pf
Freq = crystal frequency in mc

For example, if a 3-microsecond pulse is needed:

$$C = 370 (3 - 0.64) = 870 \text{ pf}$$

The maximum frequency of operation is 210 kilocycles.

The outputs from both sides of the pulse shaper (collectors of Q3 and Q4) are used to drive the pulse amplifiers. The amplifier outputs appear as assertion (negative) and negation (positive) pulses at pins 10 and 8, respectively.

External Frequency Input. To drive the MC-30 with an external frequency, crystal Y1 should be removed and the external frequency source connected to pin 18 of the PAC connector.

Synchronous Clock Control. Synchronous starting and stopping of the MC-30 prevents pulse-splitting at the outputs of the pulse amplifier and requires one stage of a UF-30 or an FA-30. These additional circuits, used in conjunction with the inverter sync output, synchronously start and stop the MC-30 as shown in figure 3-14.3.

To start, a ZERO should be applied to the AC set level control input. The flip-flop is then set on the next positive transition of the sync output and applies a ONE to the shaper inhibit input. The next positive transition of the sync output triggers the pulse shaper.

To stop, a ZERO should be applied to the AC reset level control input of the flip-flop. The leading edge of the next negation pulse then resets the flip-flop. The set output of the flip-flop applies a ZERO to pin 28 which inhibits the pulse shaper. Since the leading edge of the negation pulse initiates this action, the last pulse is a complete pulse.

SPECIFICATIONS

Input Loading

Shaper inhibit: 6 unit loads

External frequency: 70 pf to ground

Frequency of Operation

100 KC to 1 MC

Frequency Accuracy

0.005%

Frequency Stability

0.01%

Current Requirements

-18 V 53 ma

-6 V 5 ma

+12 V 15 ma

External Frequency Input Signal Requirements

Pulse amplitude (min): 1.8 V

Pulse width (min): 0.15 μsec

Total Power

1.3 watts

Polarization

Pins 22 and 32

Output Drive Capability

Assertion (negative pulse): 12 unit loads and 1000 pf of stray capacitance

Negation (positive pulse): 12 unit loads and 1000 pf of stray capacitance

Sync: 1 unit load or 1 AC input

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.14 μsec (typ)

Handle Color Code

Long: Brown

Short: Brown

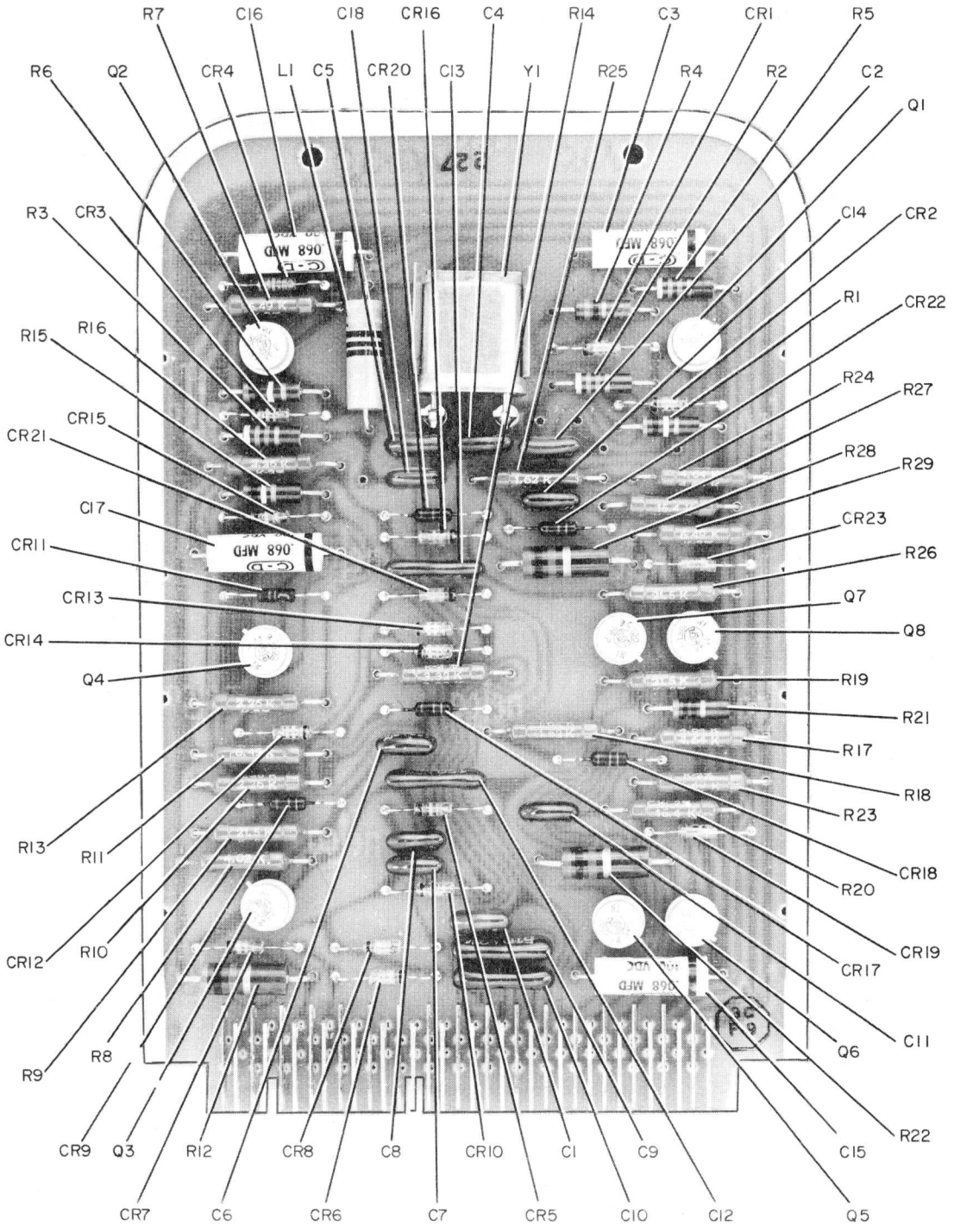
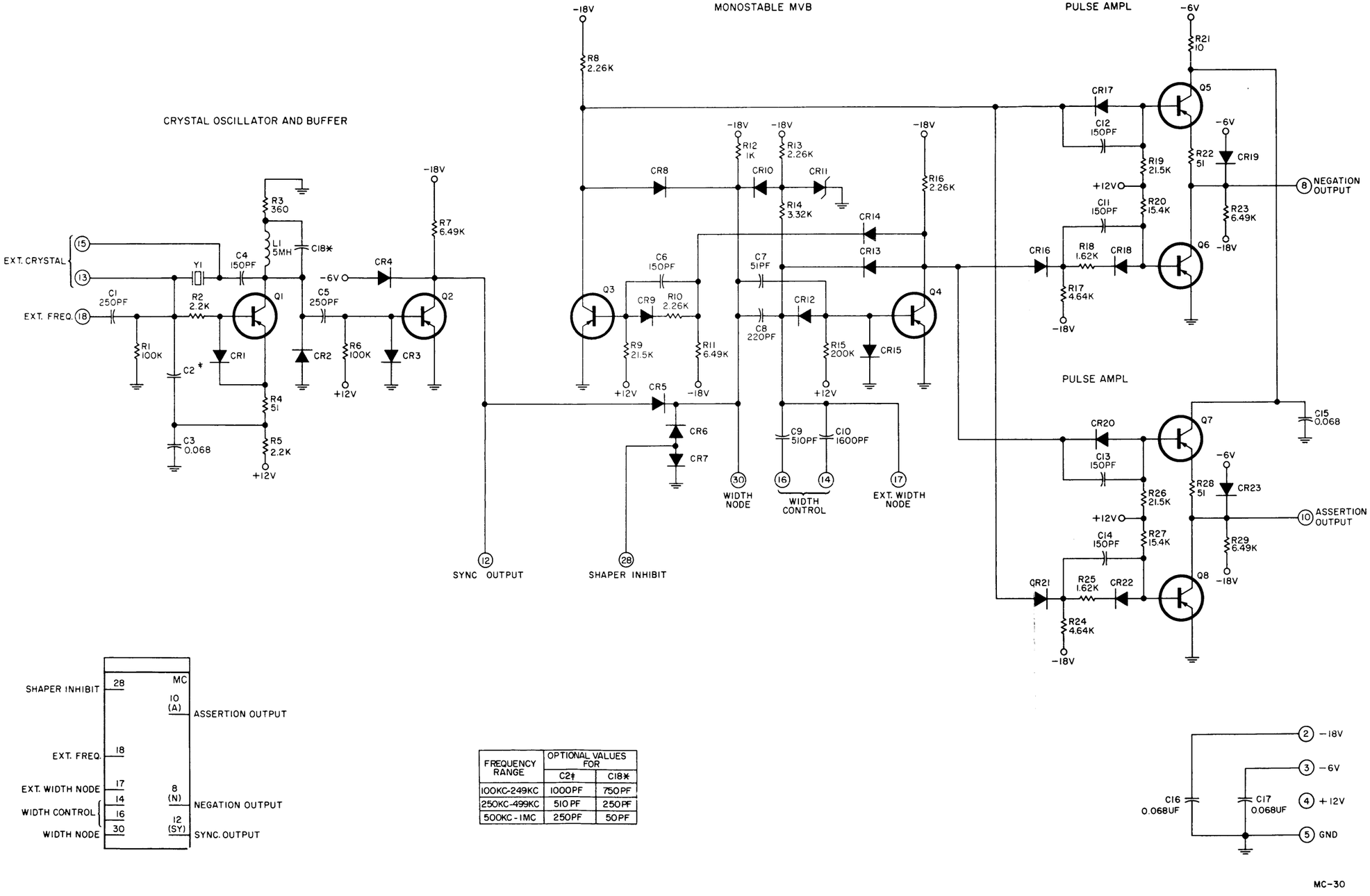
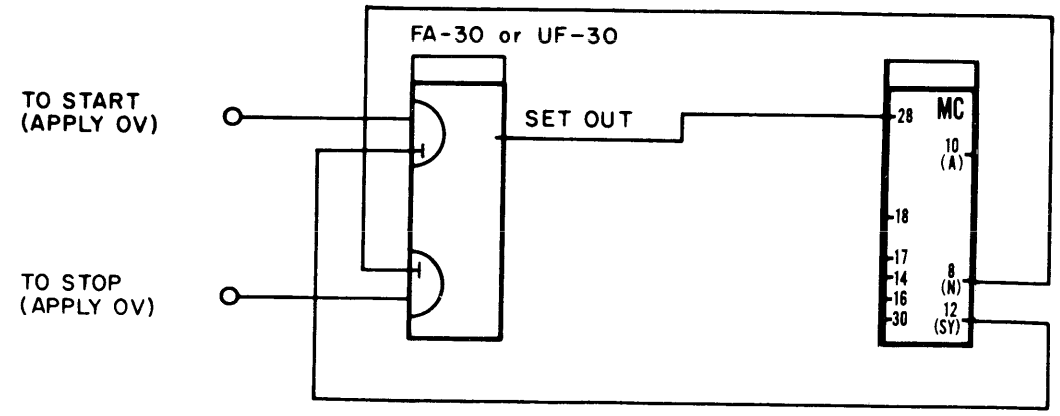


Figure 3-14.1. Master Clock PAC, Model MC-30, Parts Location



FREQUENCY RANGE	OPTIONAL VALUES FOR	
	C2‡	C18*
100KC-249KC	1000PF	750PF
250KC-499KC	510 PF	250PF
500KC - 1MC	250PF	50PF

Figure 3-14.2. Master Clock PAC, Model MC-30, Schematic and Logic Diagram



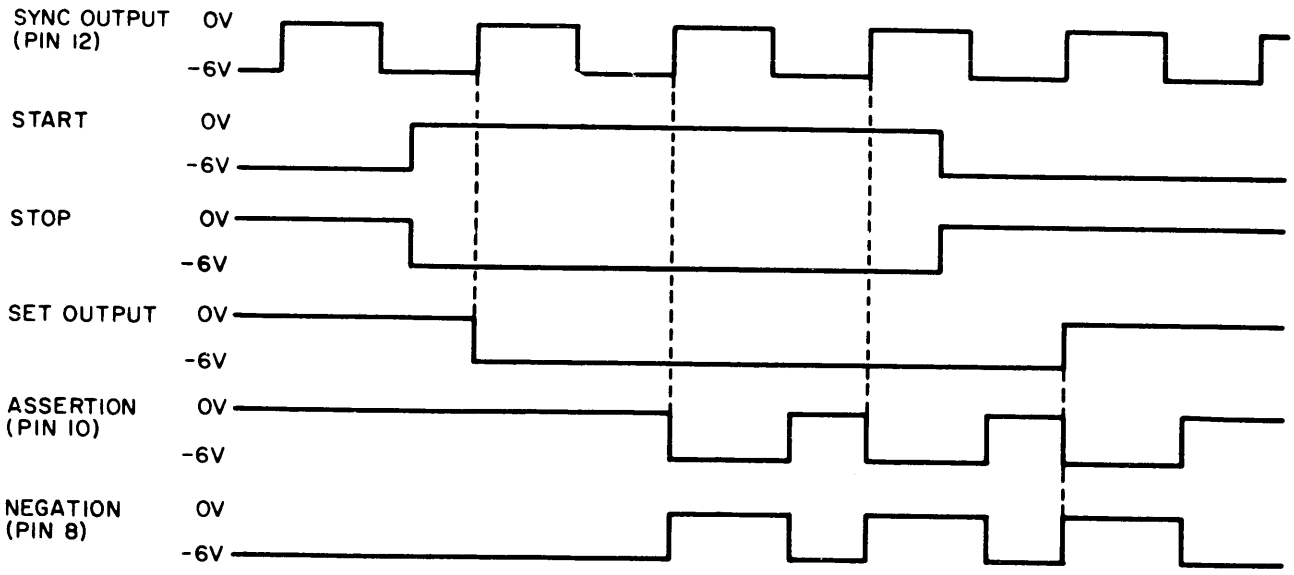


Figure 3-14.3. Synchronous Clock Control, Simplified Logic Diagram

3-15 MASTER CLOCK PAC (SPECIAL PRECISION), MODEL MC-30X

GENERAL DESCRIPTION

The Master Clock PAC, Model MC-30X (figure 3-15.1), is similar to Master Clock PAC MC-30. However, the MC-30X uses a special crystal (Y1) that insures the overall stability and accuracy of the PAC to 0.002 percent. In addition, frequency tuning capacitors C2, C4, and C18 (figure 3-15.2) provide the MC-30X with a higher degree of frequency accuracy.

The MC-30X contains a crystal-controlled oscillator, a level restorer, a pulse shaper, and a pulse amplifier. The standard operating frequency of the MC-30X is 1 megacycle, but this PAC can be modified to operate at any specified frequency between 100 kilocycles and 1 megacycle upon request. The MC-30X PAC has both assertion and negation pulse outputs set for a duration of 0.6 microsecond. The output pulse width can be expanded to 2 or 5 microseconds by jumper connections at the PAC connector.

Additional control of the MC-30X is provided by the shaper inhibit input which inhibits the output pulse train. Connections for external crystal and external frequency control and a sync output are also available at the PAC connector. The basic purpose of the external frequency input is to permit the MC-30X to be triggered by an external clock source. The external crystal input is provided to permit off-PAC mounting or oven placement for the crystal and is located at pins 13 and 15 of the PAC connector.

CIRCUIT FUNCTION

The circuit functions (figure 3-15.2) of the oscillator circuit, pulse shaper, external frequency input, and synchronous clock control are discussed in the following paragraphs.

Oscillator Circuit. The frequency generating section of the MC-30X is a parallel-resonant, 1-megacycle crystal oscillator. An external frequency source can drive the MC-30X PAC, provided the crystal is removed. Following the crystal oscillator is an inverter circuit which clamps the oscillator output to S-PAC signal levels. The inverter output (sync) is gated with the shaper inhibit to drive the pulse shaper. The sync output at pin 12 of the PAC connector can be used for synchronous clock control. A ONE (-6 V or no connection) applied to the shaper inhibit input (pin 28) allows every positive transition of the sync output to trigger the pulse shaper. A ZERO applied to pin 28 inhibits the pulse shaper.

Pulse Shaper. The pulse shaper is a one-shot multivibrator circuit which produces the desired pulse width. The pulse width can be changed by jumper connections at the PAC connector. To set the pulse width to 2 microseconds, pin 16 should be connected to pin 30. For a 5-microsecond pulse width, pin 14 should be connected to pin 30. An external capacitor can be connected to pins 17 and 30 for other pulse widths. The value of the external capacitor may be derived from the following equation:

$$C = 370\,(PW - 0.64) \qquad PW\ Max = \frac{1}{1.6 \times Freq}$$

where:

PW = pulse width in μsec
C = capacitance in pf
Freq = crystal frequency in mc

For example, if a 3-microsecond pulse is needed:

$$C = 370 (3 - 0.64) = 870 \text{ pf}$$

The maximum frequency of operation is 210 kilocycles.

The outputs from both sides of the pulse shaper (collectors of Q3 and Q4) are used to drive the pulse amplifiers. The amplifier outputs appear as assertion (negative) and negation (positive) pulses at pins 10 and 8, respectively.

External Frequency Input. To drive the MC-30X with an external frequency, crystal Y1 should be removed and the external frequency source connected to pin 18 of the PAC connector.

Synchronous Clock Control. Synchronous starting and stopping of the MC-30X prevents pulse-splitting at the output of the pulse amplifier and requires one stage of a UF-30 or an FA-30. These additional circuits, used in conjunction with the inverter sync output, synchronously start and stop the MC-30X as shown in figure 3-15.3.

To start, a ZERO should be applied to the AC set level control input of the flip-flop. The flip-flop is then set on the next positive transition of the sync output and applies a ONE to the shaper inhibit input. The next positive transition of the sync output triggers the pulse shaper.

To stop, a ZERO should be applied to the AC reset level control input of the flip-flop. The leading edge of the next negation pulse then resets the flip-flop. The set output of the flip-flop applies a ZERO to pin 28 which inhibits the pulse shaper. Since the leading edge of the negation pulse initiates this action, the last pulse is a complete pulse.

SPECIFICATIONS

Input Loading

Shaper inhibit: 6 unit loads
External frequency: 70 pf to ground

Frequency of Operation

100 KC to 1 MC

Frequency Accuracy

0.002%

Frequency Stability

0.002%

Current Requirements

-18 V	53 ma
-6 V	5 ma (reverse current into supply)
+12 V	15 ma

External Frequency Input Signal Requirements

Pulse amplitude (min): 1.8 V
Pulse width (min): 0.15 μsec

Total Power

1.3 watts (max)

SPECIFICATIONS (Continued)

Polarization

Pins 22 and 32

Output Drive Capability

Assertion: 12 unit loads and 1000 pf of stray capacitance

Negation: 12 unit loads and 1000 pf of stray capacitance

Sync: 1 unit load or 1 AC input

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Handle Color Code

Long: Brown

Short: Brown

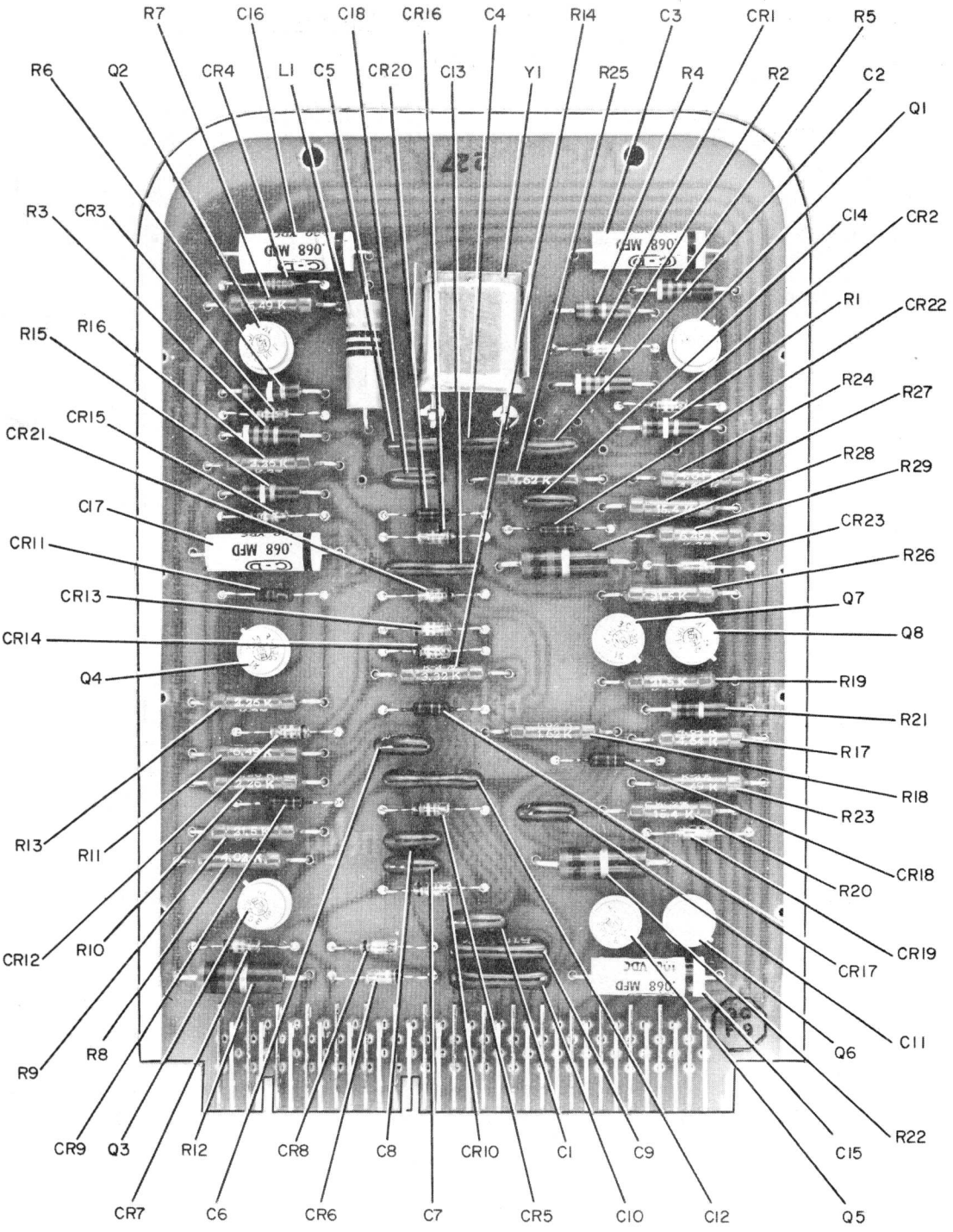
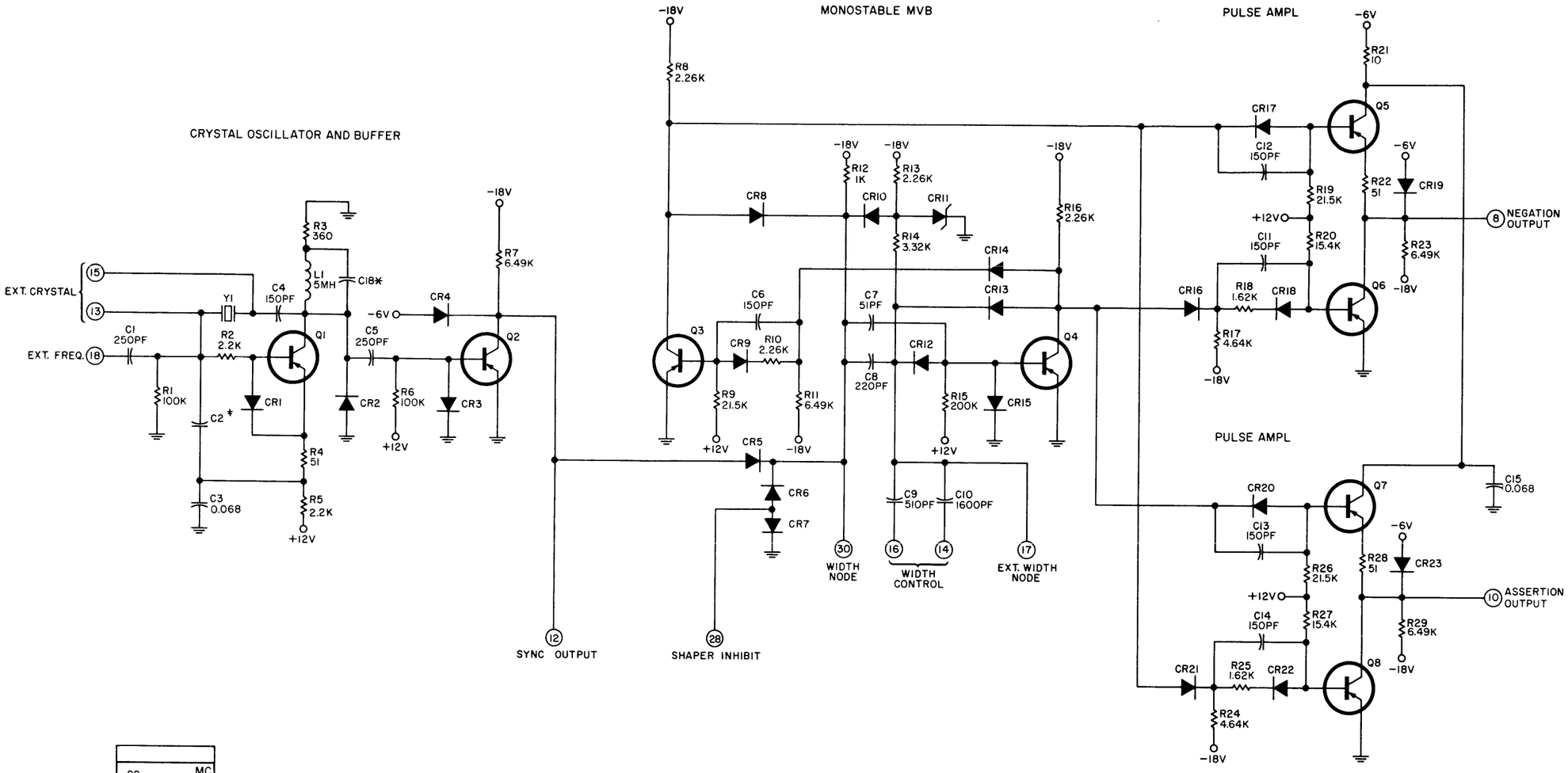
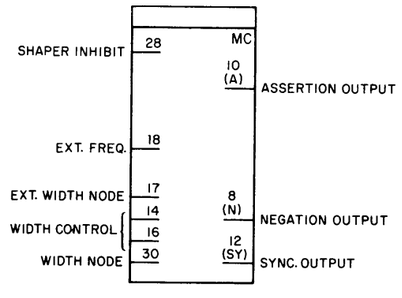


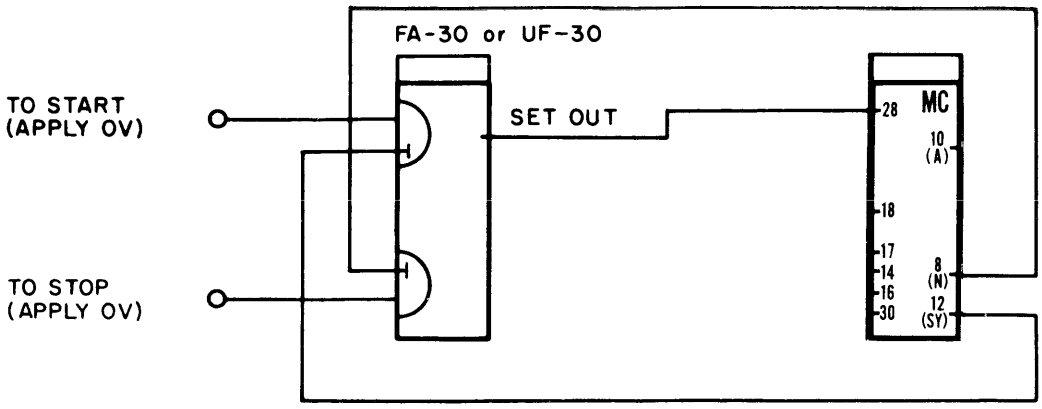
Figure 3-15.1. Master Clock PAC (Special Precision), Model MC-30X, Parts Location





FREQUENCY RANGE	OPTIONAL VALUES FOR	
	C2†	C18*
100KC-249KC	1000PF	750PF
250KC-499KC	510 PF	250PF
500KC - 1MC	250PF	50PF

Figure 3-15.2. Master Clock PAC (Special Precision) Model MC-30X, Schematic and Logic Diagram



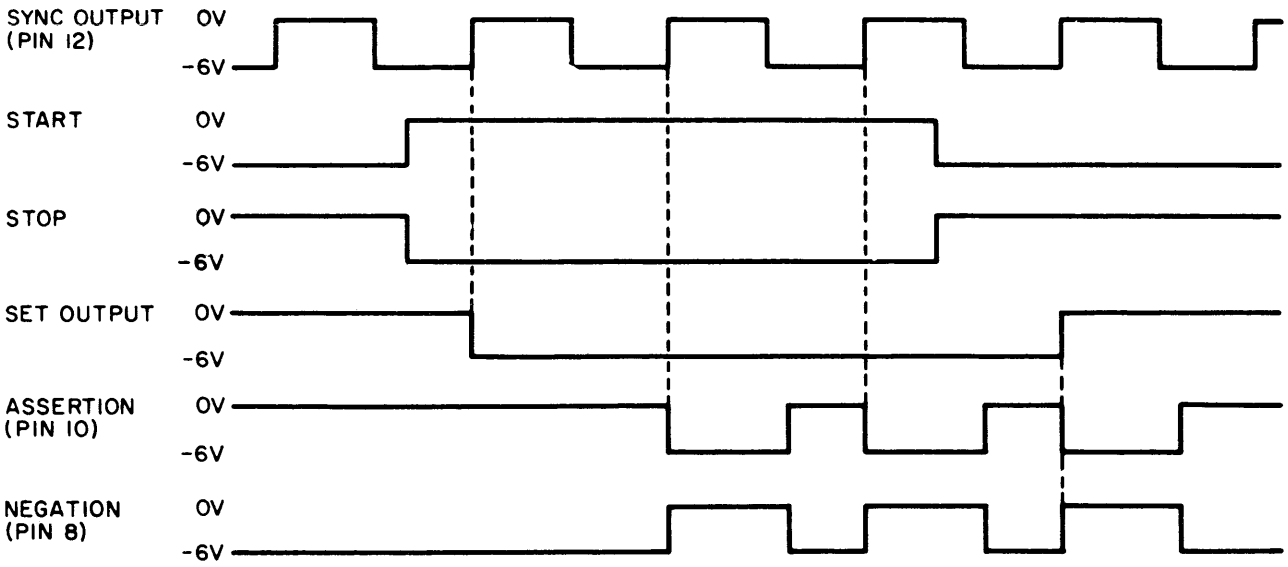


Figure 3-15.3. Synchronous Clock Control, Simplified Logic Diagram

3-16 MULTI-PURPOSE FLIP-FLOP PAC, MODEL MF-30

GENERAL DESCRIPTION

The Multi-Purpose Flip-Flop PAC, Model MF-30 (figures 3-16.1 and 3-16.2), contains four identical, independent flip-flops which can be used for storage, counting, and shifting functions. Each flip-flop has DC set and reset inputs which permit the parallel loading of information and each has a common AC input and associated set and reset level control inputs for shifting and counting. In addition, a common reset input is provided for the simultaneous clearing of all four flip-flops. The basic flip-flop circuit (figure 3-16.3) of the MF-30 is functionally identical to that of the UF-30, except that the MF-30 does not have the AC set and reset inputs.

CIRCUIT FUNCTION

The four MF-30 circuits are identical. Each circuit consists of two cross-coupled NAND gates with AC and DC inputs.

DC Set and Reset Inputs. When a ZERO (0 V) is applied to the DC set or reset input for 0.25 microsecond or longer, the flip-flop assumes the set or reset state, respectively. The flip-flop can be set and reset within a 1-microsecond interval.

Common AC Input. The common AC input is associated with two level controls which steer signals applied to the common AC input to the set or reset side of the flip-flop. Thus, when the associated level control inputs are connected to another flip-flop to form a shift register, the common AC input serves as the shift input. When the level control inputs are properly connected to the flip-flop outputs, the MF-30 functions as a binary counter. Refer to tables 3-16.1 and 3-16.2.

Timing. There are two modes of operation for AC inputs with level controls. The first is the pulse mode of operation, which is defined as the condition where the level control signal switches negative when the AC input signal is positive. The required AC input signal for this mode of operation is a negative pulse with a minimum pulse width of 0.6 microsecond.

The second mode of operation is the step mode, which is defined as the condition where the level control switches negative when the AC input signal is negative. This mode requires that the AC input signal remain negative for a minimum of 1.4 microseconds after the level control switches negative. Waveforms associated with both modes of operation are illustrated in figures 3-16.4 and 3-16.5.

Common Reset Input. A 1-microsecond positive pulse applied to the common reset input clears (resets) all four flip-flops simultaneously.

SPECIFICATIONS

Input Loading

DC inputs: 1 unit load each

AC inputs: 2 unit loads each

Level controls: 1/2 unit load each

Input Waveform Requirements

Common reset: 1 μsec (min) at logic ZERO

Circuit Delay

(Measured at -3 V)

0.15 μsec (typ) Reset input to set output or
0.25 μsec (max) set input to reset output.

0.60 μsec (typ) Set input to set output or
0.10 μsec (max) reset input to reset output.

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 103 ma

-6 V 42 ma (reverse current into supply)

+12 V 5 ma

Total Power

1.8 watts

Polarization

Pins 14 and 20

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Handle Color Code

Long: Green

Short: Orange

Table 3-16.1. MF-30 Connections For Use as Complementing Stages

Input Used	Connect			
	Circuit A	Circuit B	Circuit C	Circuit D
Common AC Input	Pin 8 to 9 Pin 7 to 6	Pin 12 to 13 Pin 11 to 10	Pin 31 to 30 Pin 32 to 33	Pin 27 to 26 Pin 28 to 29

Table 3-16.2. MF-30 Connections For Use as Shift Stages

Input Used	Connect			
	Circuit A	Circuit B	Circuit C	Circuit D
Common AC Input	Pin 8 to reset output of previous stage Pin 7 to set output of previous stage	Pin 12 to reset output of previous stage Pin 11 to set output of previous stage	Pin 31 to reset output of previous stage Pin 32 to set output of previous stage	Pin 27 to reset output of previous stage Pin 28 to set output of previous stage

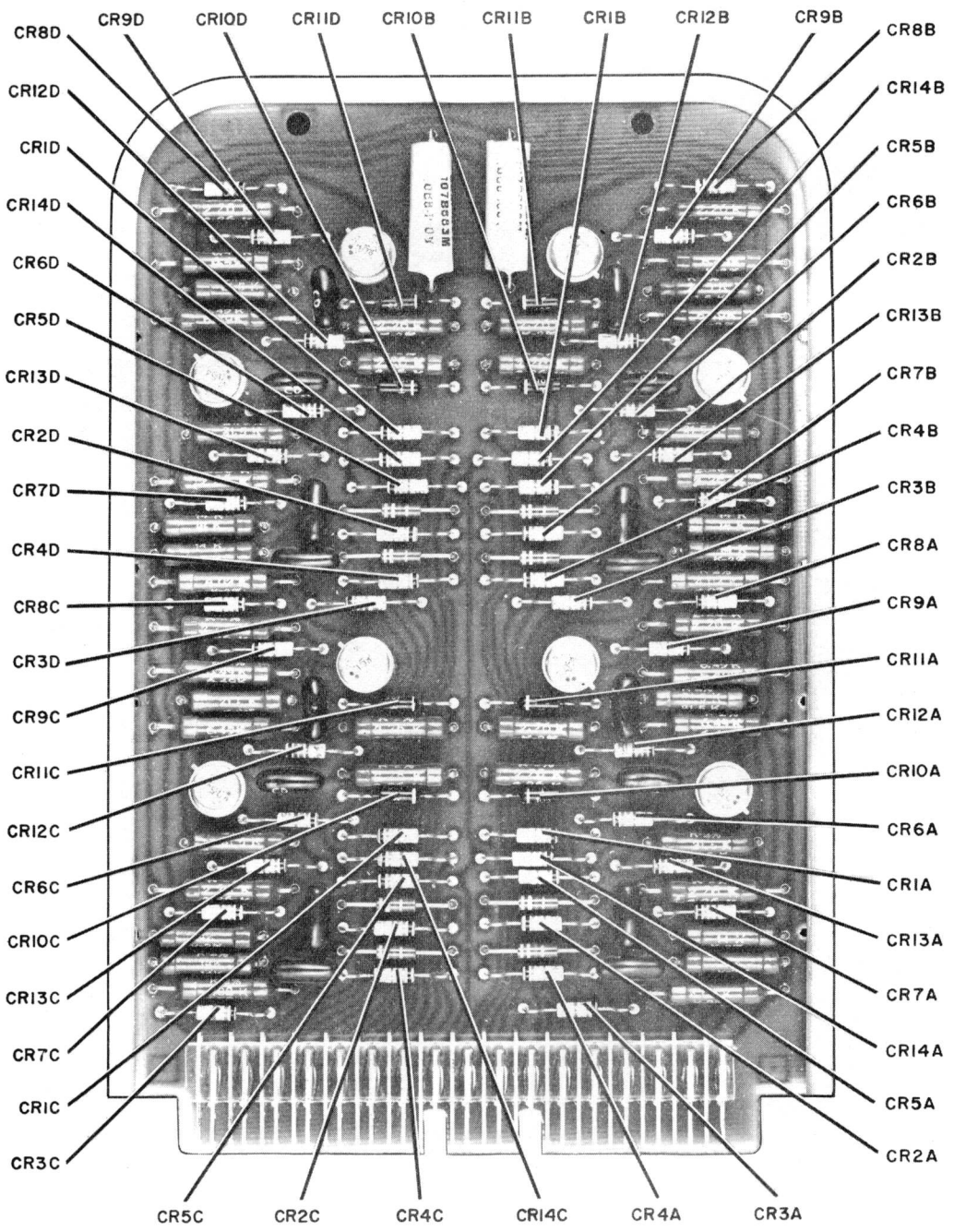


Figure 3-16.1. Multi-Purpose Flip-Flop PAC, Model MF-30, Parts Location (Diodes)

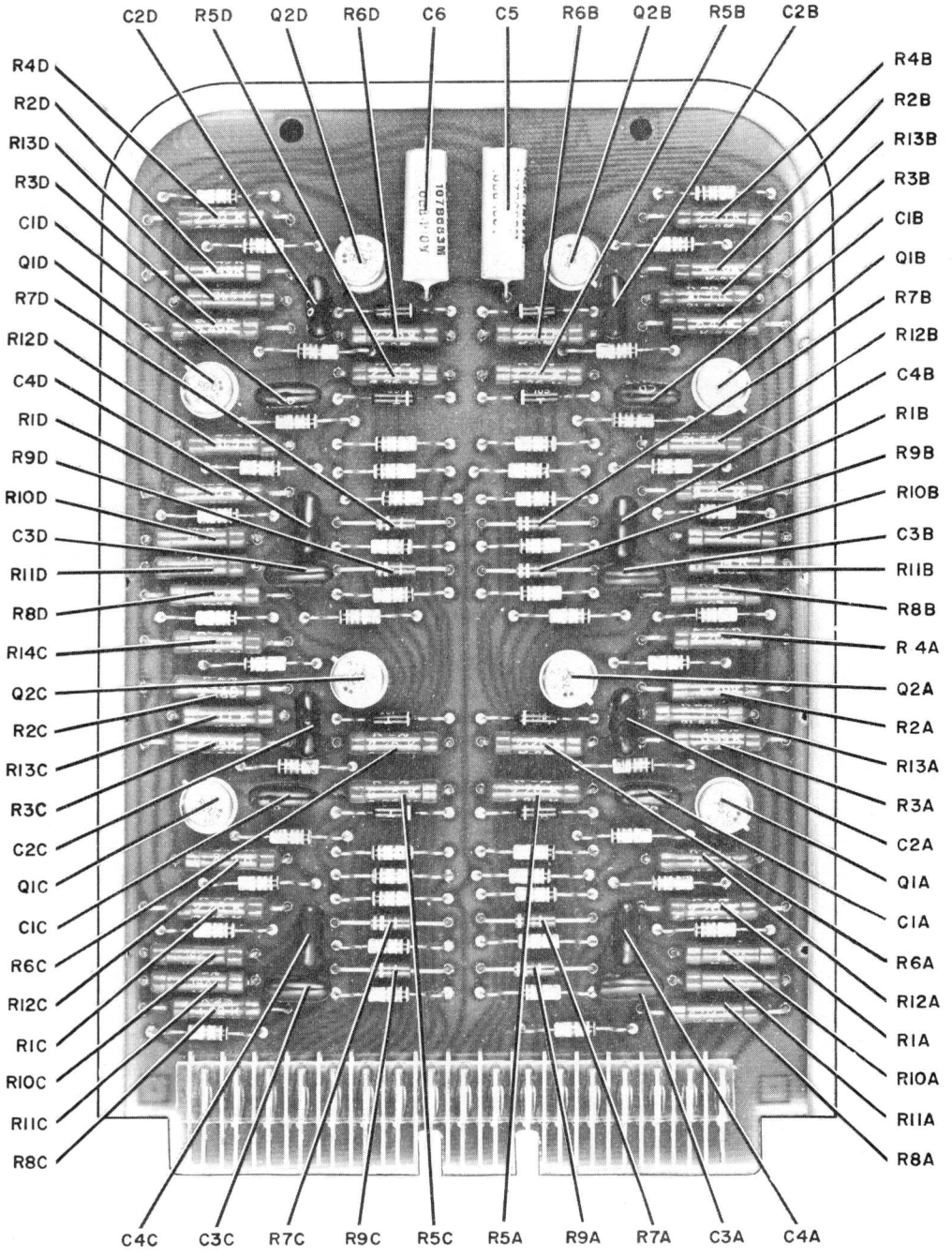


Figure 3-16.2. Multi-Purpose Flip-Flop PAC, Model MF-30
Parts Location (Resistors, Capacitors, and Transistors)

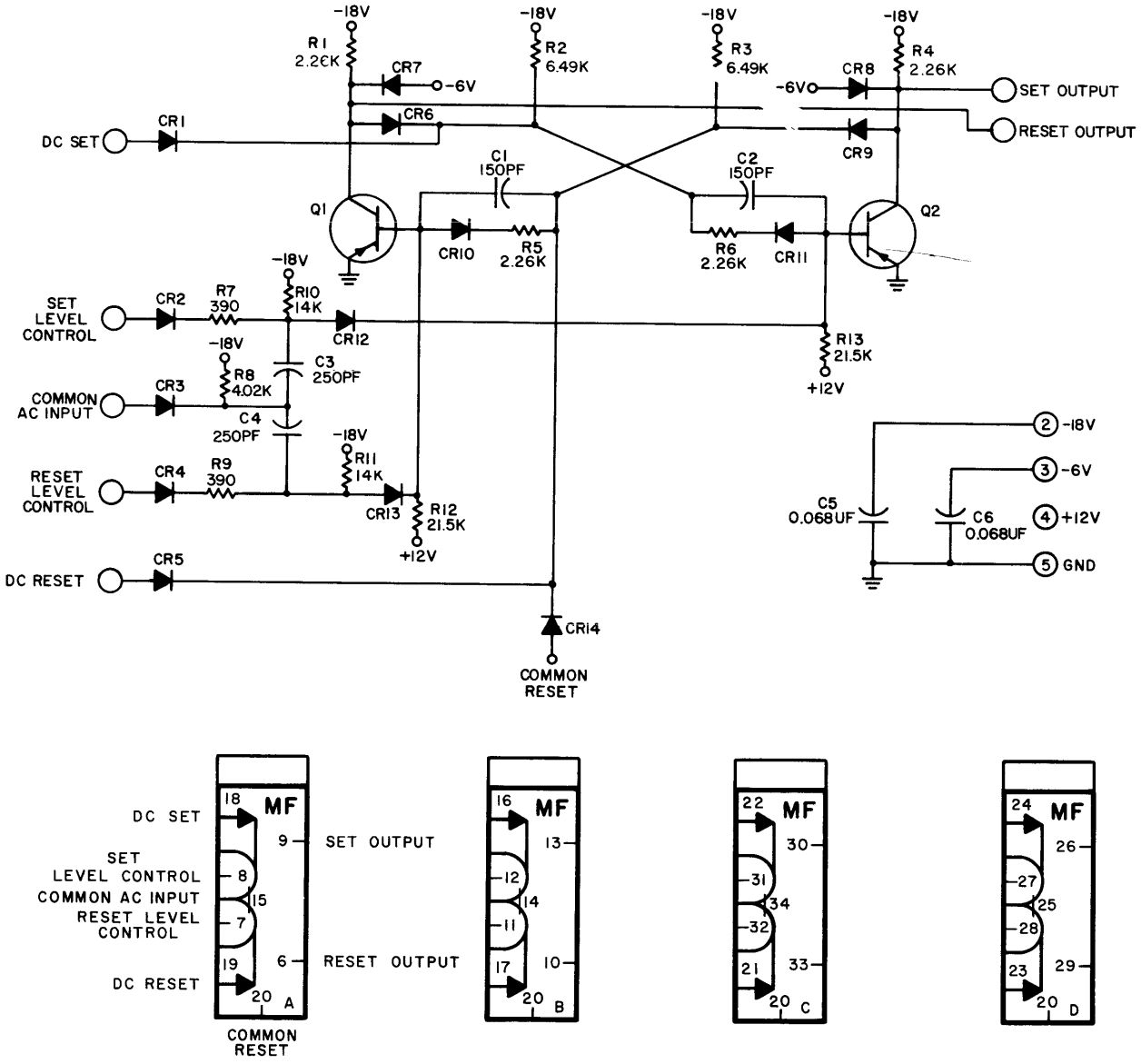
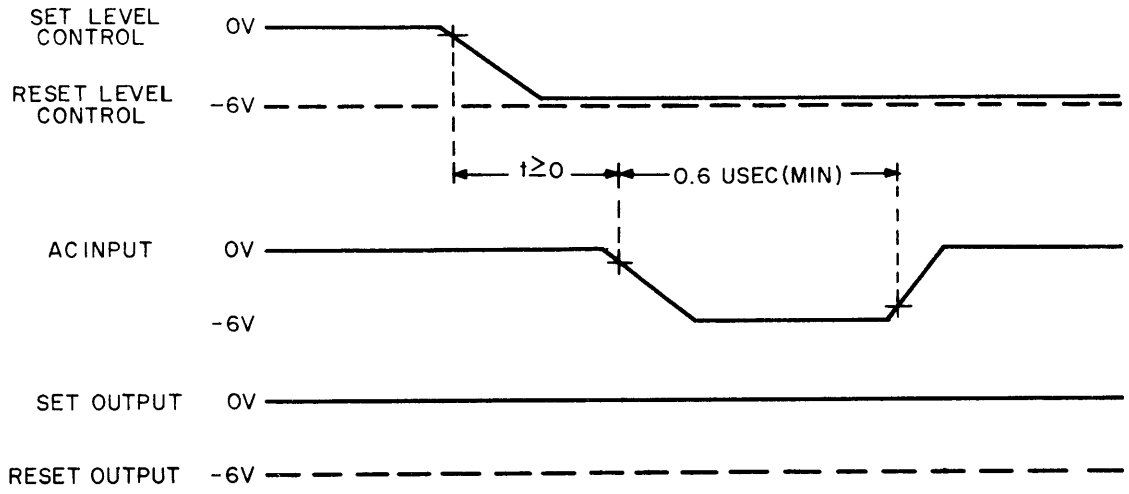


Figure 3-16.3. Multi-Purpose Flip-Flop PAC, Model MF-30, Schematic and Logic Diagram

(a) INHIBITING ACTION



(b) PROPER SWITCHING ACTION

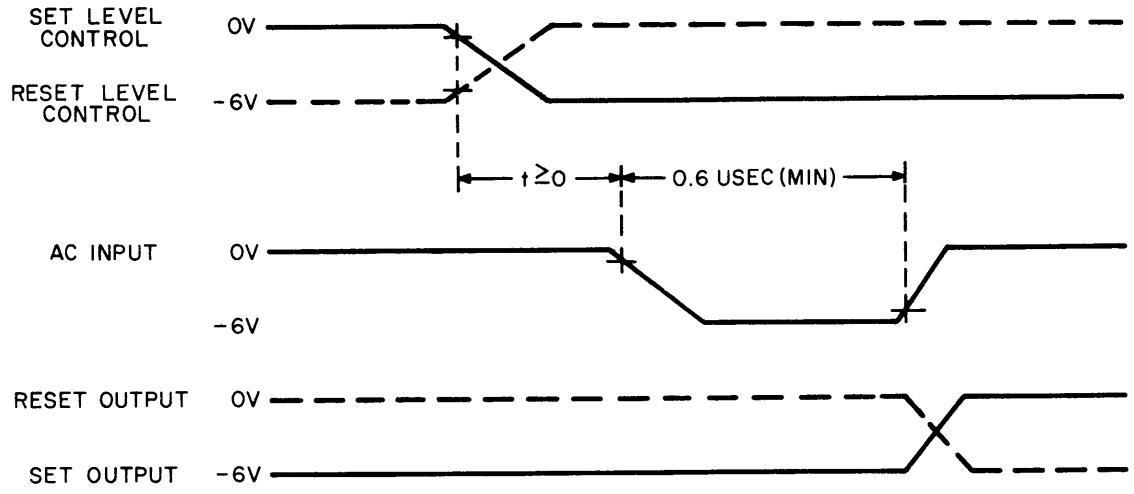
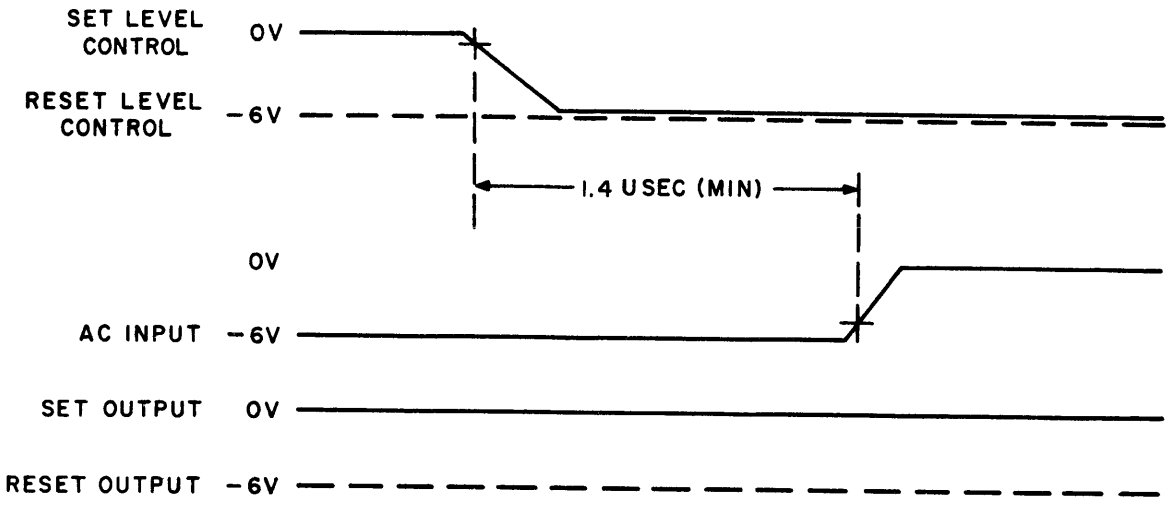


Figure 3-16.4. Pulse Mode Timing

(a) INHIBITING ACTION



(b) PROPER SWITCHING ACTION

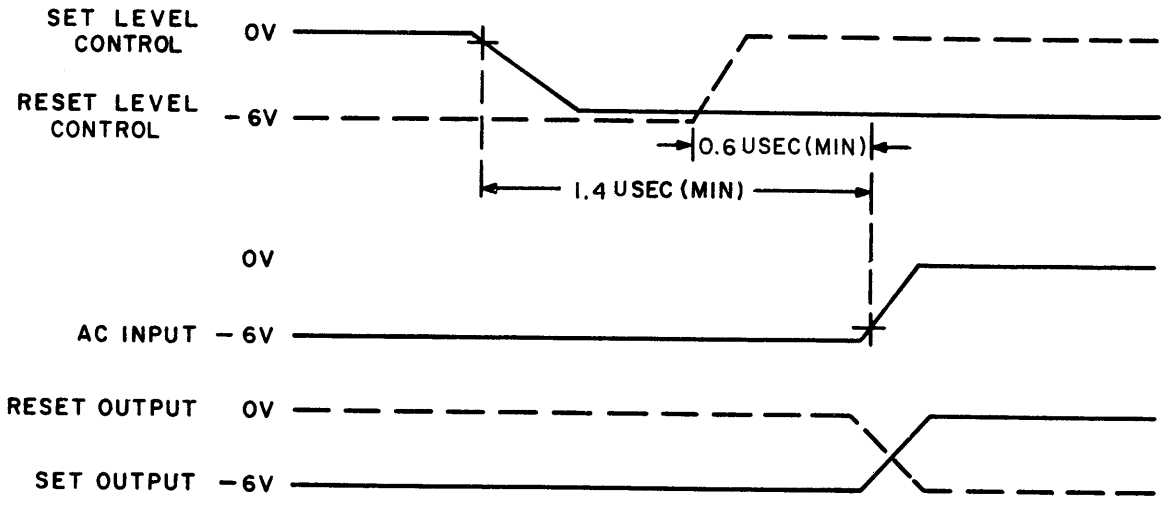


Figure 3-16.5. Step Mode Timing

3-17 MULTIVIBRATOR CLOCK PAC, MODEL MV-30

GENERAL DESCRIPTION

The Multivibrator Clock PAC, Model MV-30 (figure 3-17.1), contains a self-starting, free-running multivibrator circuit, a pulse shaper, and pulse amplifier circuits. The MV-30 functions primarily as a variable frequency clock source. The frequency of operation is from 50 cps to 1 megacycle in five overlapping ranges; however, lower frequencies are obtainable with the addition of external capacitors.

The MV-30 provides assertion and negation pulse outputs and square-wave outputs. The PAC provides separate inputs to inhibit the free-running multivibrator circuit and the pulse shaper. In addition, the output pulse width is adjustable to either 2 or 5 microseconds using a jumper connection. The output pulse width is further variable to any desired pulse width by the connection of an external capacitor to the proper PAC connector pins.

CIRCUIT FUNCTION

The circuit functions of the MV-30 (figure 3-17.2) are discussed in the following paragraphs.

Multivibrator Circuit. The multivibrator is a free-running, astable, and self-starting circuit. The operational frequency range of the multivibrator is dependent upon the parallel capacitance selected by jumpering specified terminals at the PAC connector. The basic frequency of the multivibrator is 1 megacycle adjustable to 150 kilocycles without making any additional connections. This basic frequency can be reduced progressively by making connections to terminals 27 and 29 as indicated in table 3-17.1. Potentiometer R6, mounted on the PAC, permits variation of the frequency within the selected range. The frequency variation of the range also can be controlled remotely by disconnecting the potentiometer from the PAC and connecting an external potentiometer (15K) to pins 12 and 14 of the connector.

Table 3-17.1. Frequency Range and Pin Connections at the PAC Connector

Multivibrator Frequency Range	Connect Terminal No. 27 to Terminal or Terminals Below	Connect Terminal No. 29 to Terminal or Terminals Below
1 MC to 155 KC	None	None
165 to 23 KC	34	16
25 to 3.3 KC	32, 34	18, 16
3.5 KC to 410 cps	30, 32, 34	20, 18, 16
430 to 50 cps	28, 30	20, 24
Below 50 cps	Connect two external capacitors;* one across terminals 27 and 33 and the other across terminals 29 and 22.	

*The value of each external capacitor is determined by the following equation:

$$C = \frac{220}{f}$$

where: C = capacity in microfarads

f = midrange frequency in cps

The extremities of each frequency range are approximately 8:1.

For example: Assume a frequency of 2 cps is required. Using the above equation,

$$C = \frac{220}{2} = 110\ \mu f$$

NOTE

When two 110-microfarad capacitors are used in conjunction with potentiometer R6, the frequency range becomes 0.71 to 5.6 cps.

Pulse Shaper Circuit. The pulse shaper circuit is a standard one-shot multivibrator activated by negative transitions from free-running multivibrator output pin 35. RC networks determine the pulse widths. A standard 0.6-microsecond pulse width is provided. Pulse widths of 2 and 5 microseconds are obtainable by jumpering the PAC between pins 10 and 11 and between pins 10 and 19, respectively. Any pulse width can be obtained by connecting an external capacitor between pins 10 and 13 on the connector. The value of the external capacitor can be derived from the following equations:

$$C = 370\ (PW - 0.64) \qquad PW_{Max} = \frac{1}{1.6 \times freq.}$$

where: C = capacitance in pf

PW = pulse width in μsec

freq = crystal frequency in megacycles

For example: If a 3-microsecond width is required, the value of the external capacitor is obtained by:

$$C = 370\ (3 - 0.64) = 870\ pf$$

Pulse Amplifier Circuit. The outputs of both sides of the one-shot multivibrator pulse shaper drive the pulse amplifiers to provide the assertion and negation output pulse trains. The pulse amplifiers enable the assertion and negation outputs (pins 9 and 6, respectively) to drive 12 unit loads and 1000 pf of stray capacitance each.

Controls. Two inputs are provided on the MV-30 for controlling the operation of the PAC. These inputs are discussed in the following paragraphs.

a. Oscillator Inhibit Input (Pin 26). The oscillator inhibit input controls the stopping of the free-running multivibrator. A logic ZERO (0 V) applied to pin 26 stops oscillation of the circuit. A logic ONE (-6 V) applied to pin 26 allows the circuit to free-run. No connection to pin 26 is equivalent to the application of a ONE. The ZERO input results in a ONE output at pin 17 and a ZERO output at pin 35.

b. Shaper Inhibit Input (Pin 25). The shaper inhibit input is gated with the output from the astable multivibrator (pin 35) to drive the pulse shaper. A ZERO applied to pin 25 inhibits the functioning of the pulse shaper. If the pulse shaper is inhibited through the pulse shaper input, the astable multivibrator continues to free-run and yields square-wave output signals to pins 35 and 17, inhibiting the assertion and negation output pulses at pins 9 and 6.

Synchronous Start and Stop. Synchronous start and stop of the MV-30 PAC prevents possible pulse splitting at the outputs of the astable circuit and the assertion and negation outputs of the PAC. Synchronous start and stop is accomplished through the oscillator inhibit input or the shaper inhibit input.

If the oscillator inhibit input is used, no external circuits are required to synchronously start the astable multivibrator. If a ONE is applied to pin 26, the circuit will free-run. Square waves will thus be produced at the astable multivibrator outputs (pins 35 and 17) as well as pulses at the assertion and negation outputs (pins 6 and 9). Stopping the operation of the MV-30 by applying a ZERO level directly to the oscillators inhibit input can produce pulse splitting. To prevent this, one section of a UF-30 or FA-30, connected as shown in figure 3-17.3, performs the stop function without incurring pulse-splitting.

If the shaper inhibit input is used, synchronous starting and stopping is achieved by using one section of a UF-30 or FA-30 as shown in figure 3-17.4. The astable circuit will then continue to free-run when synchronous starting and stopping is controlled by the shaper inhibit input.

SPECIFICATIONS

Input Loading

Oscillator inhibit: 6 unit loads

Shaper inhibit: 3 unit loads

Frequency of Operation

50 cps to 1 MC (5 overlapping ranges)

DC to 50 cps (with addition of external capacitors)

Current Requirements

-18 V	115 ma
-6 V	28 ma (reverse current into supply)
+12 V	5 ma

Total Power

2.0 watts

Polarization

Pins 16 and 32

Output Drive Capabilities

Assertion (negative pulse): 12 unit loads and 1000 pf stray capacitance

Negation (positive pulse): 12 unit loads and 1000 pf stray capacitance

MV Output: 4 unit loads

$\overline{MV}$ Output: 6 unit loads

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Handle Color Code

Long: Brown

Short: Yellow

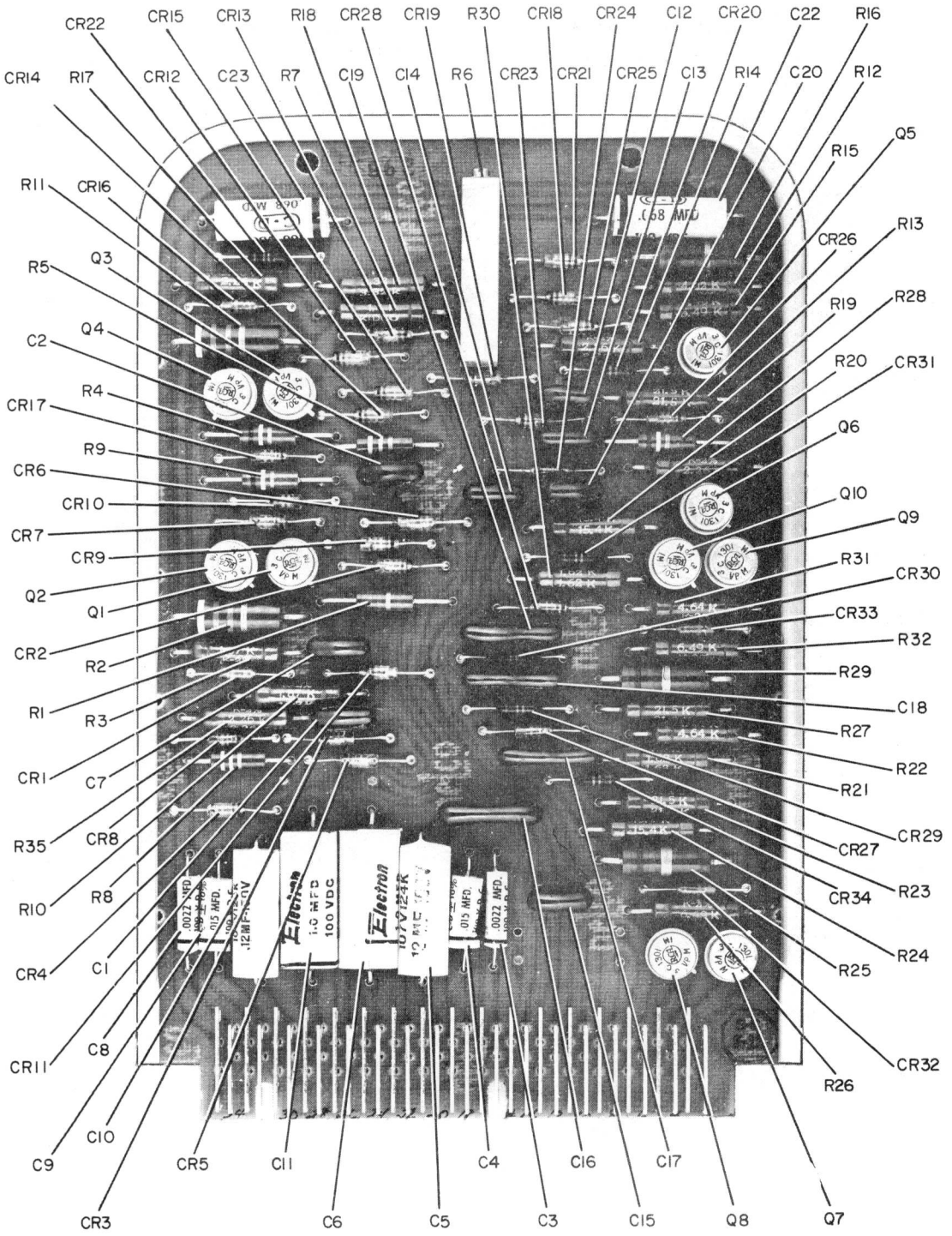


Figure 3-17.1. Multivibrator Clock PAC, Model MV-30, Parts Location

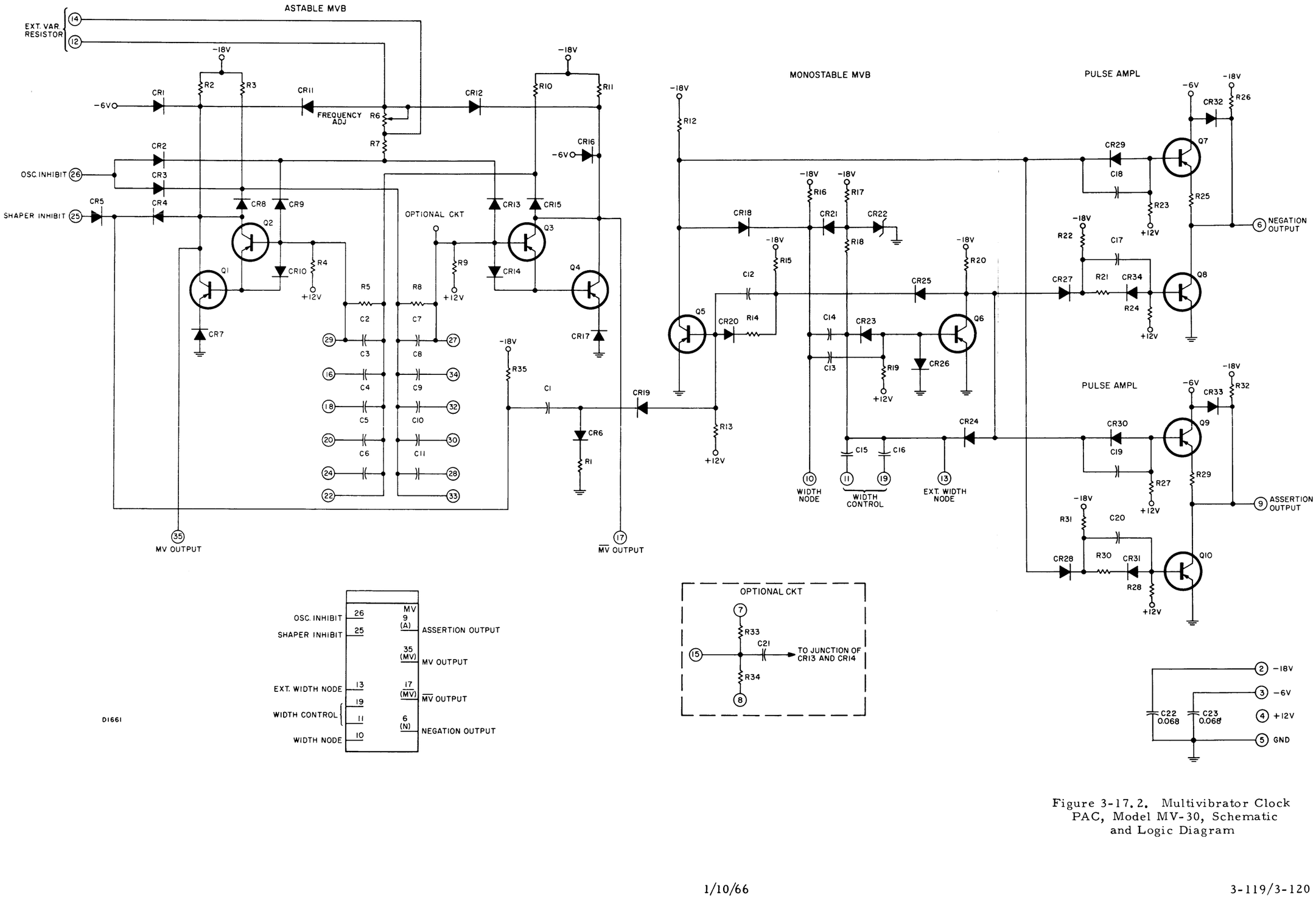


Figure 3-17.2. Multivibrator Clock PAC, Model MV-30, Schematic and Logic Diagram

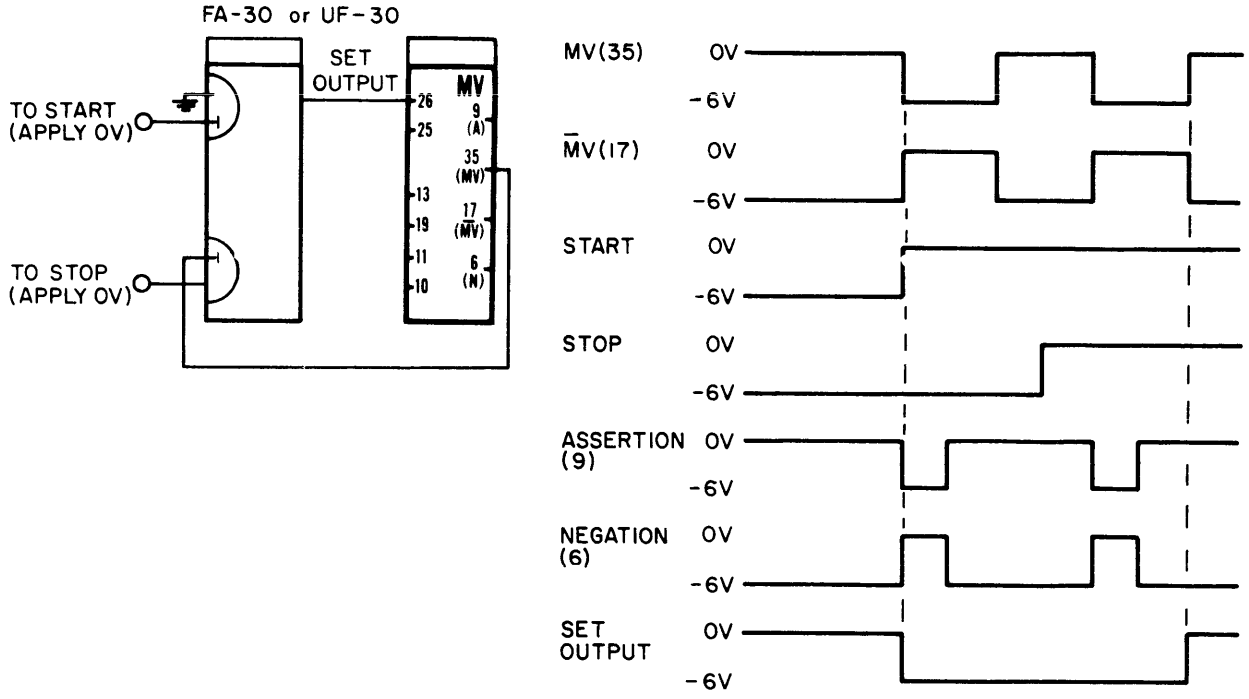


Figure 3-17.3. Start Control Input, Synchronous Operation

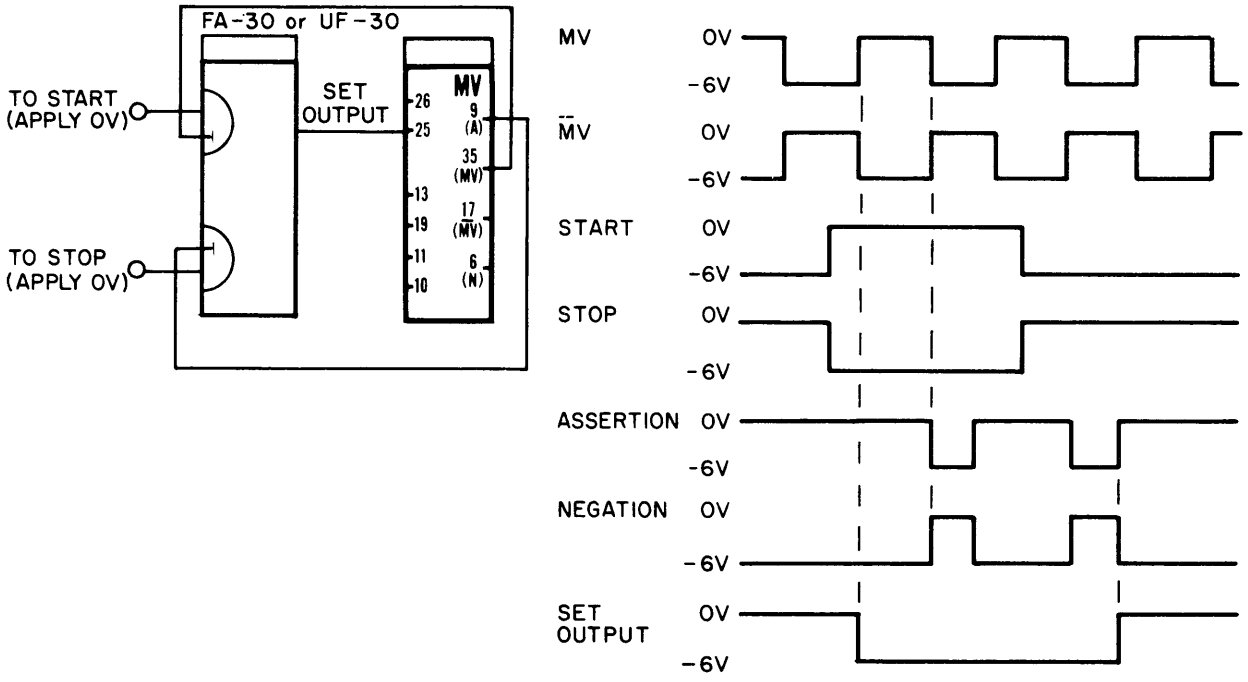


Figure 3-17.4. Gate Control Input, Synchronous Operation

3-18 OCTAL/DECIMAL DECODER PAC, MODEL OD-30

GENERAL DESCRIPTION

The Octal/Decimal Decoder PAC, Model OD-30 (figures 3-18.1 and 3-18.2), contains a prewired binary-to-octal decoder and additional circuits to expand the matrix for BCD-to-decimal decoding. The octal matrix has nine input lines and eight output lines. Of the nine inputs, six are wired to activate one of the eight outputs. The three additional input lines are provided to permit the matrix to be expanded to 16, 32, or 64 outputs by connecting additional OD-30s in parallel. If a 64-output matrix is not required, one or more of these additional input lines can be used for strobing or sampling of the matrix.

The BCD-to-decimal decoder uses the octal matrix for the zero through seven output lines and two additional independent gates, included on the S-PAC, for output lines eight and nine. The two independent gates are standard NAND gates which can be used as such when BCD-to-decimal decoding is not required.

CIRCUIT FUNCTION

The circuit functions of the OD-30 (figure 3-18.3) are discussed in the following paragraphs.

Octal Matrix. The octal matrix has nine input lines which drive eight NAND gates (figures 3-18.3 and 3-18.4). Six of the nine input lines (pins 15 through 20) are driven by the assertion and negation levels of a three-bit binary number. These six input lines are prewired to three inputs of each of the eight gates. The three inputs then become discrete combinations of the three binary bits and their negations. As an example, the gate driving output line six (pin 9) has $\bar{2}^0$, 2^1, and 2^2 as the three inputs.

Each of the eight gates has a total of six inputs. Three of these inputs recognize a discrete binary number from 000 through 111 as described previously. The remaining three inputs are common to all eight gates and are distributed to pins 12, 13, and 14 on the connector. The six inputs to any gate must be a ONE (-6 V) to activate the gate output. Since pins 12, 13, and 14 form three common and direct inputs to all eight gates, these inputs must all be ONEs to have one of the eight output lines activated. An output line is activated when it is at ZERO (0 V).

Making no connection to pins 12, 13, or 14 is equivalent to having the input at ONE. Applying ZERO to any one of these common input lines inhibits the octal matrix. This feature is useful in applications requiring multioctal matrices, BCD-to-decimal decoding, and strobing.

Multioctal Matrices. Matrices with 16, 32, or 64 outputs are formed by driving multiple octal matrices in parallel. All but the one matrix containing the significant output line must be inhibited. As as example, in a 64-output matrix eight octal matrices are used and seven of these must be inhibited for unique activation of one of the 64 output lines. The seven octal matrices are inhibited by applying ZERO to either pin 12, 13, or 14 as discussed previously. For example, if binary bits 2^3, 2^4, and 2^5 are true (ONE), the seven matrices containing outputs 0 through 55 inclusive are inhibited and only one output from 56 to 63 is activated, depending upon the state of bits 2^0, 2^1, and 2^2. Figure 3-18.4 shows the logic connection for multioctal matrices.

BCD-to-Decimal Decoder. The BCD-to-decimal decoder consists of the octal matrix, in conjunction with the two additional NAND gates, as indicated by the logic connections illustrated in figure 3-18.5. If the OD-30 is connected in this manner, four binary-coded-decimal bits and their negations are required to drive the decimal decoder. Only the most and least significant digits are required as inputs to gates eight and nine if binary numbers 10 through 15 are forbidden, or if ambiguous outputs resulting from these numbers are permitted.

Strobing. Provision is made to permit strobing or sampling of the matrix. Strobing is accomplished by applying a negative pulse to pin 12, 13, or 14. Prior to the pulse, when the input is a ZERO (0 V), the matrix is inhibited and all output lines are ONEs. During the negative pulse, one of the output lines is activated (0 V). The three input lines to the octal matrix (pins 12, 13, and 14) can be used as separate strobe lines to gate a strobing function.

The OD-30 decodes any combination of binary bits and their negations. As the inputs to the OD-30 change, one or more of the outputs can be transiently selected. For example, a binary counter in changing from 0111 to 1000 passes briefly through states 0110, 0100, and 0000. These transitory states cause brief positive spikes at the corresponding output lines of the OD-30. Typically, the spikes are 0.1 microsecond in width. To eliminate the spikes, the decoder should be inhibited during the transition of the driver register.

One method of eliminating spikes when the input is driven from an S-PAC register is to strobe the decoder with the signal that triggers the register. This method takes advantage of trailing edge triggering inherent in S-PAC flip-flop modules. Figure 3-18.6 presents logic and timing diagrams for a typical case.

SPECIFICATIONS

Input Loading

Binary to Octal and Multioctal Matrices

8 output decoder (3 bits): 3 unit loads each

16 output decoder (4 bits): 4 unit loads each

32 output decoder (5 bits): 7 unit loads each

64 output decoder (6 bits): 14 unit loads each

BCD-to-Decimal Decoder

Binary bits 2^0, and $\overline{2}^0$: 4 unit loads each

Binary bits 2^1, $\overline{2}^1$, 2^2, and $\overline{2}^2$: 3 unit loads each

Binary bit 2^3: 2 unit loads

Binary bit $\overline{2}^3$: 5 unit loads

Frequency of Operation

DC to 1 MC

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Circuit Delay

0.06 μsec (typ)

0.1 μsec (max)

Output Drive Capability

7 unit loads and 400 pf stray capacitance each

SPECIFICATIONS (Continued)

Total Power

1.7 watts

Polarization

Pins 8 and 32

Current Requirements

-18 V 108 ma

-6 V 58 ma (reverse current into supply)

+12 V 7 ma

Handle Color Code

Long: Purple

Short: Yellow

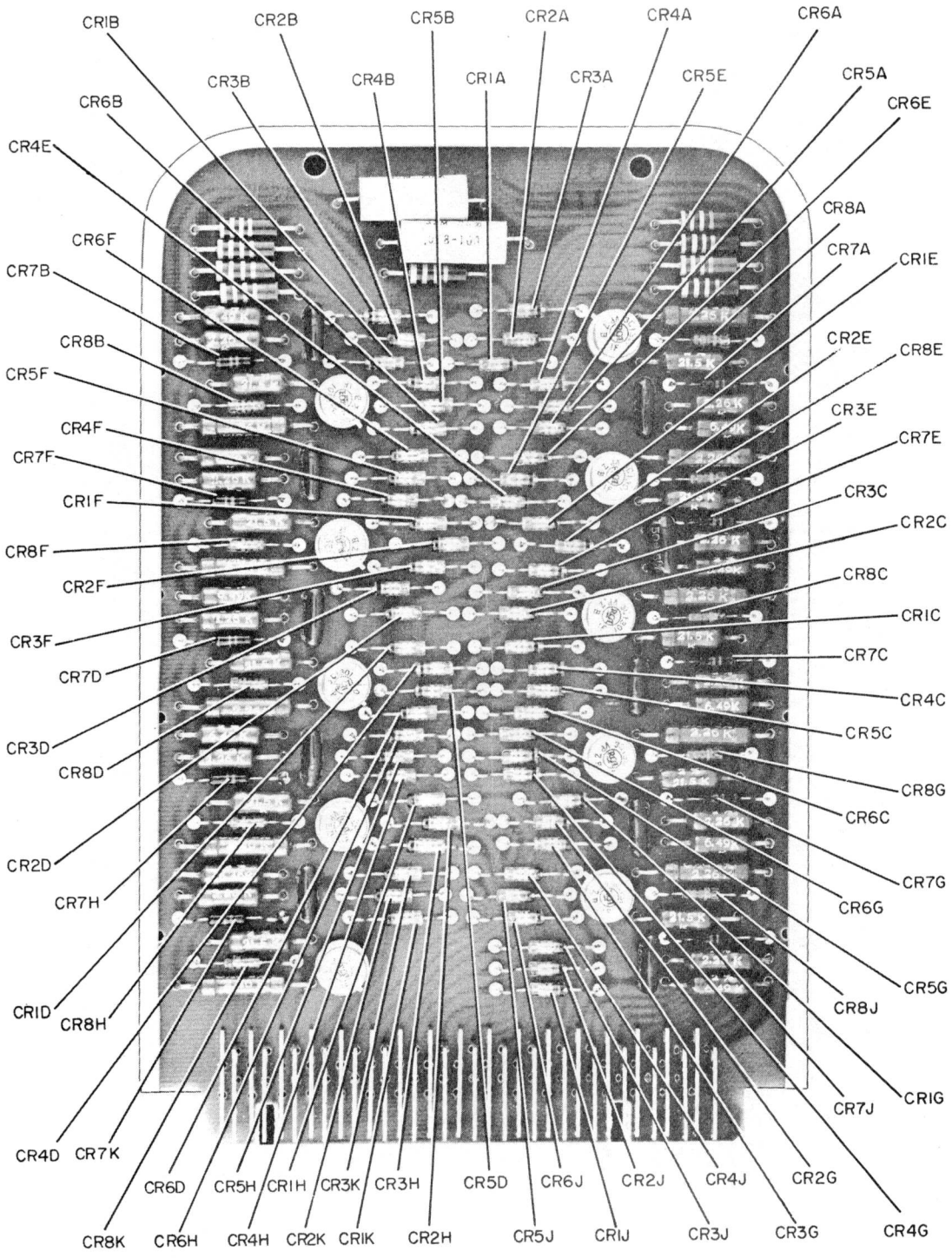


Figure 3-18.1. Octal/Decimal Decoder PAC, Model OD-30, Parts Location (Diodes)

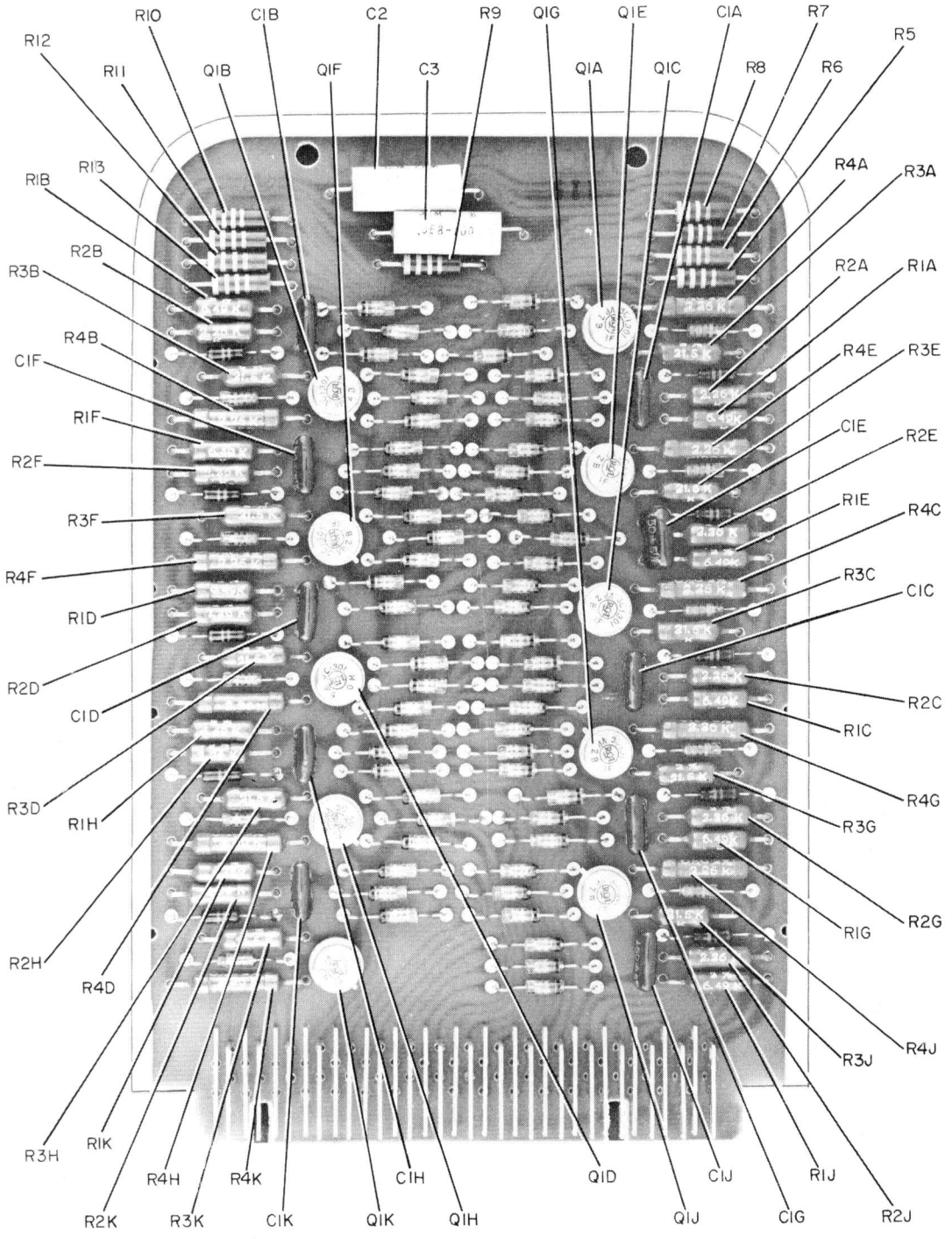


Figure 3-18.2. Octal/Decimal Decoder PAC, Model OD-30, Parts Location (Capacitors, Resistors, and Transistors)

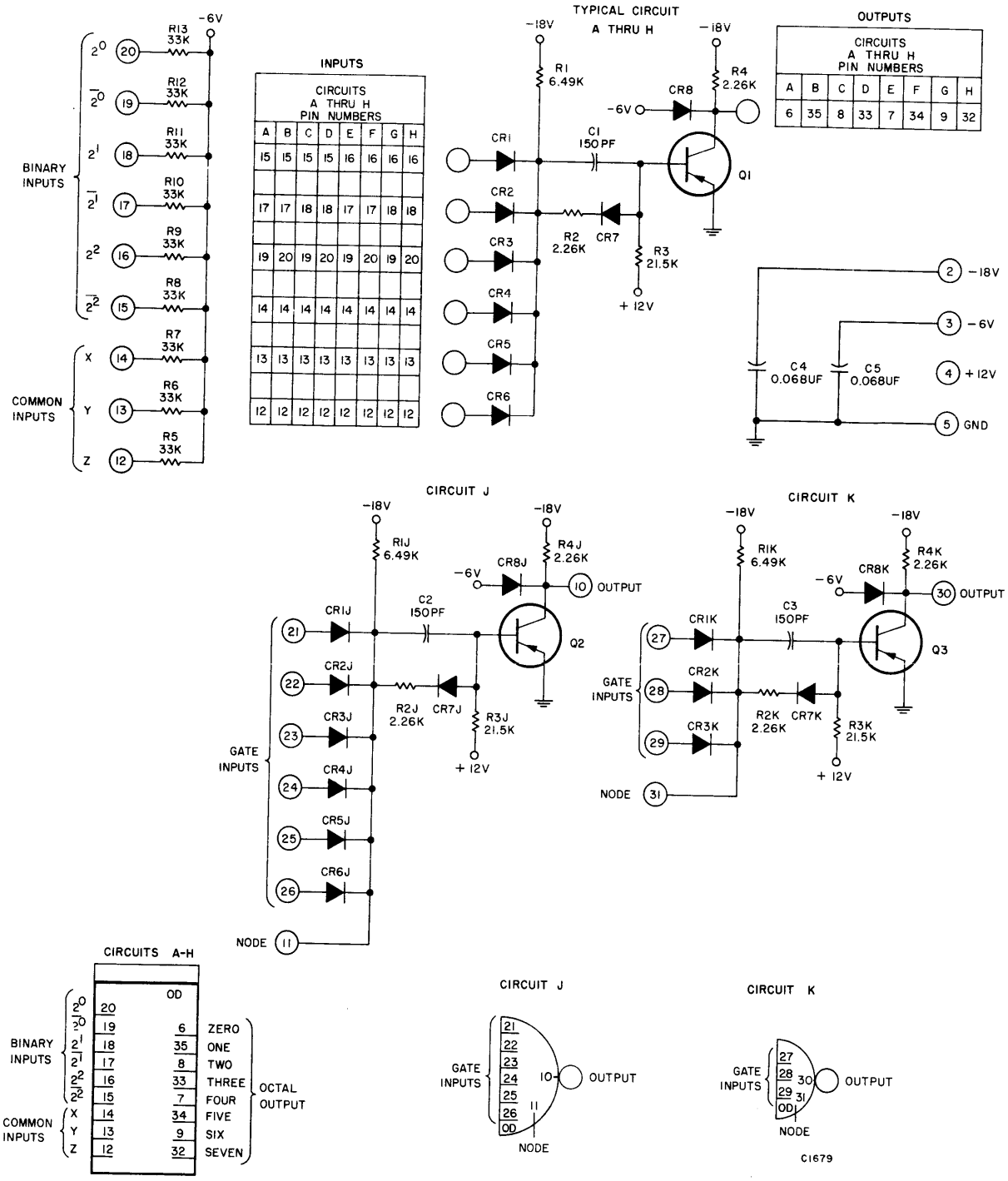


Figure 3-18.3. Octal/Decimal Decoder PAC, Model OD-30, Schematic and Logic Diagram

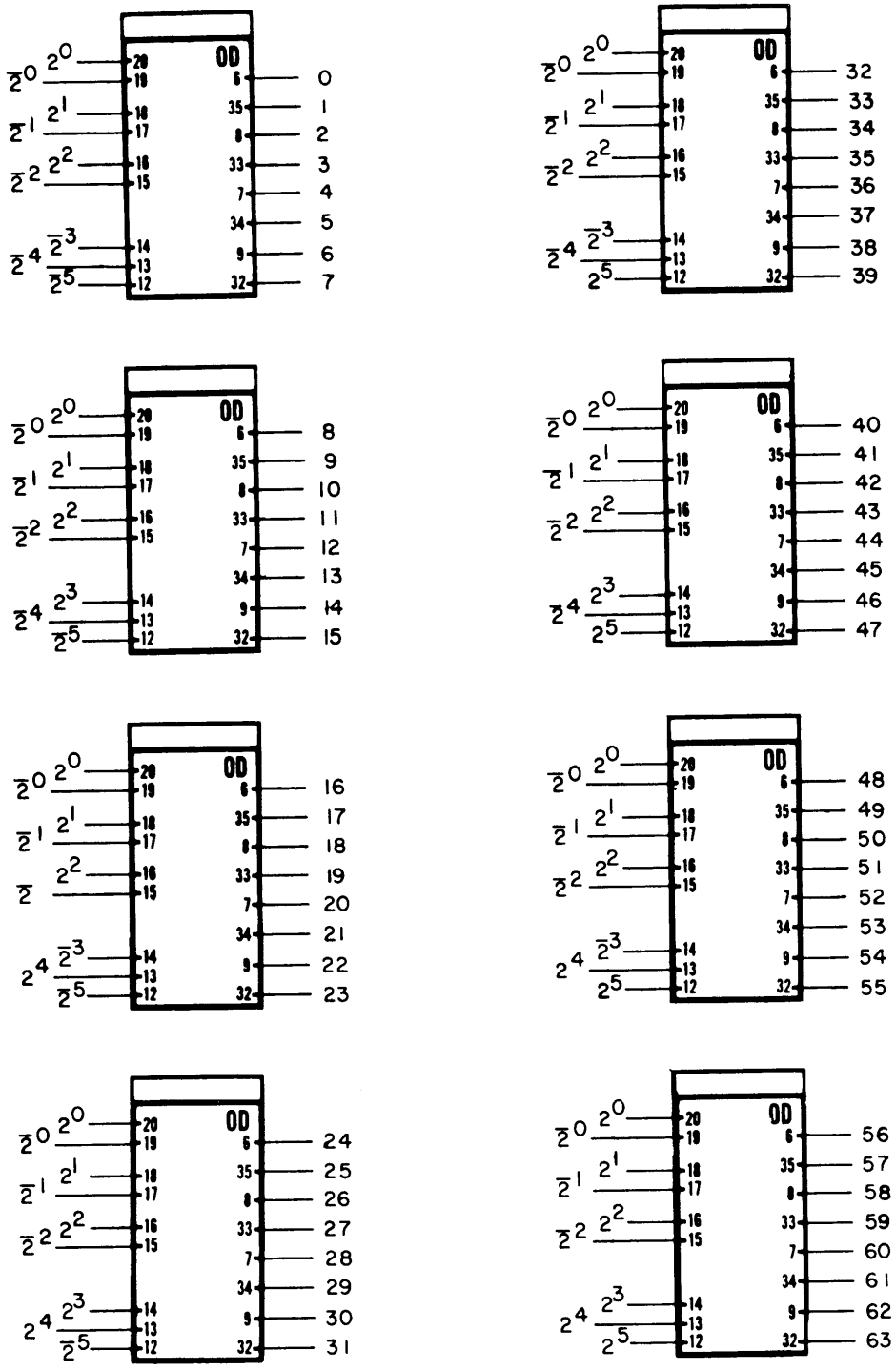


Figure 3-18.4. Multioctal Matrices

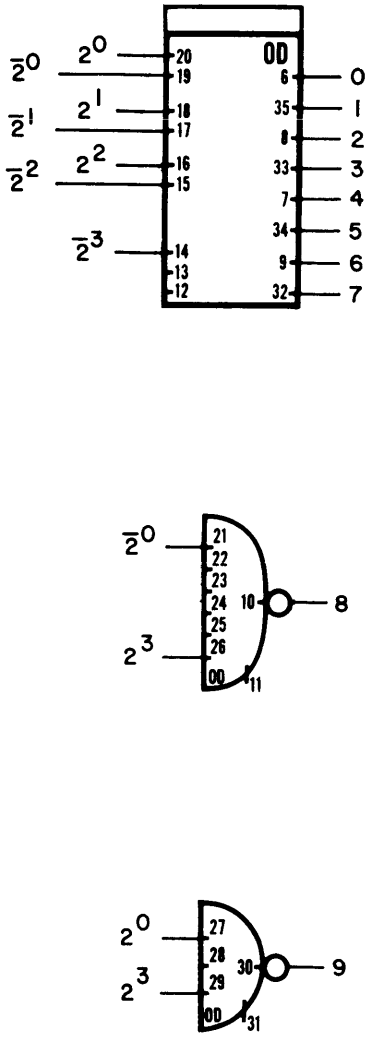


Figure 3-18.5. BCD-to-Decimal Decoder

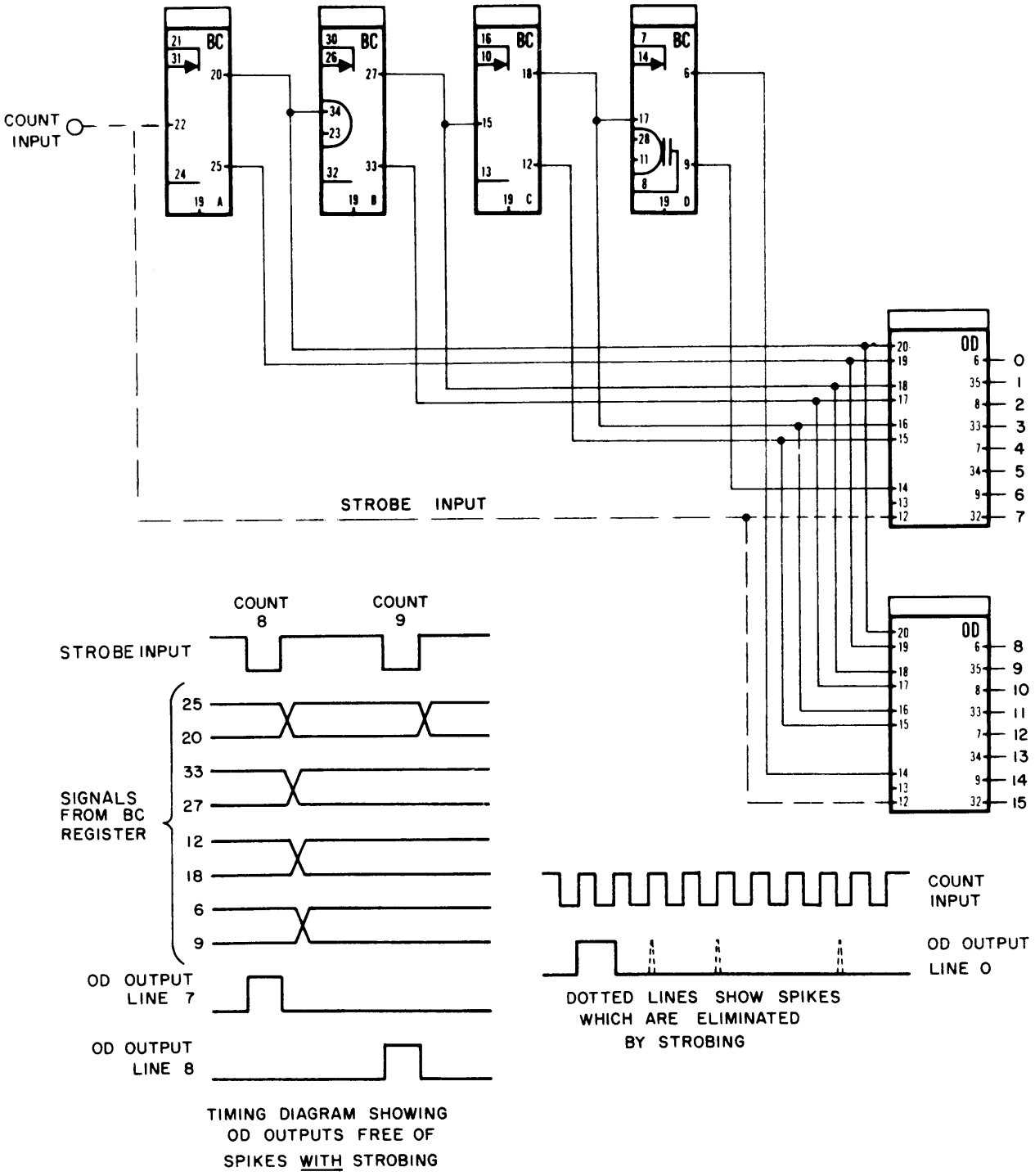


Figure 3-18.6. Logic and Timing Diagram

3-19 POWER AMPLIFIER PAC, MODEL PA-30

GENERAL DESCRIPTION

The Power Amplifier PAC, Model PA-30 (figure 3-19.1), contains four independent power inverters. Each power inverter circuit has a single diode input plus node and two isolated outputs, with each output capable of driving 14 unit loads and stray capacitance. The number of inputs is expandable to a maximum of 10 by connecting diode clusters contained in the DC or DN S-PACs to the node input. The PA-30 amplifiers are logic equivalents of S-PAC NAND gates. The PA-30 is used to drive heavy loads, such as common reset lines, shift lines, long information loads, clock buses, etc.

CIRCUIT FUNCTION

Each PA-30 circuit (figure 3-19.2) consists of a single input diode gate, with gate node expandable to 10 inputs, followed by a dual power inverter amplifier. When all inputs are at ONE (-6 V), the gate turns the two output transistors on and each output is clamped through a transistor to 0 volt. When an input goes to ZERO (0 V), all but one transistor is turned off. This transistor clamps both outputs through isolating diodes to a -6 volt level.

SPECIFICATIONS

Input Loading

3 unit loads each

Circuit Delay

0.25 μsec (max)
0.15 μsec (typ)

Output Drive Capability

14 unit loads and 1000 pf stray capacitance each (28 unit loads per circuit)

20 unit loads and 2000 pf stray capacitance, with both outputs tied in parallel

Current Requirements

-18 V 58 ma
- 6 V 22 ma (reverse current into supply)
+12 V 9 ma

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Total Power

1.3 watts

Polarization

Pins 20 and 22

Handle Color Code

Long: Green
Short: Green

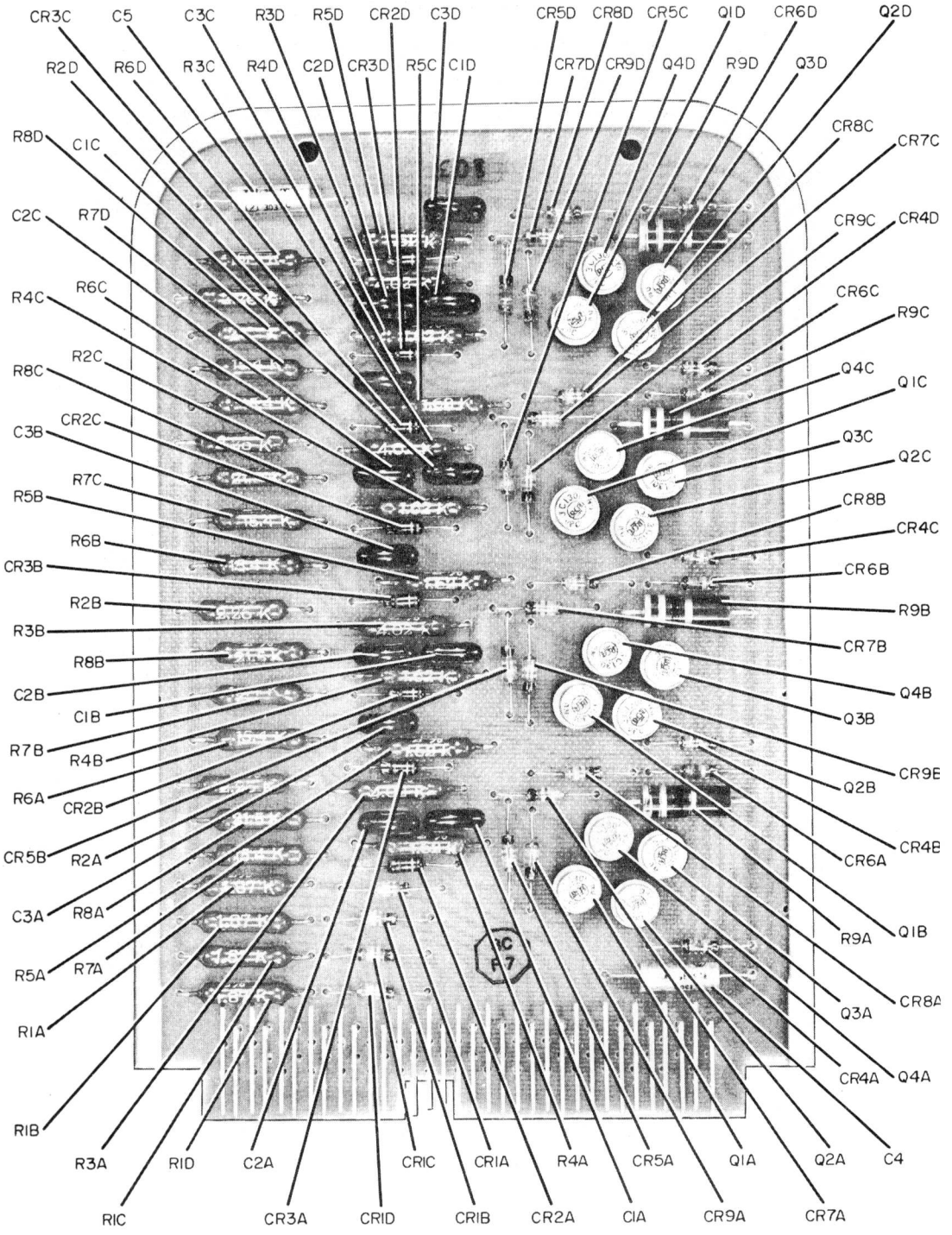


Figure 3-19.1. Power Amplifier PAC, Model PA-30, Parts Location

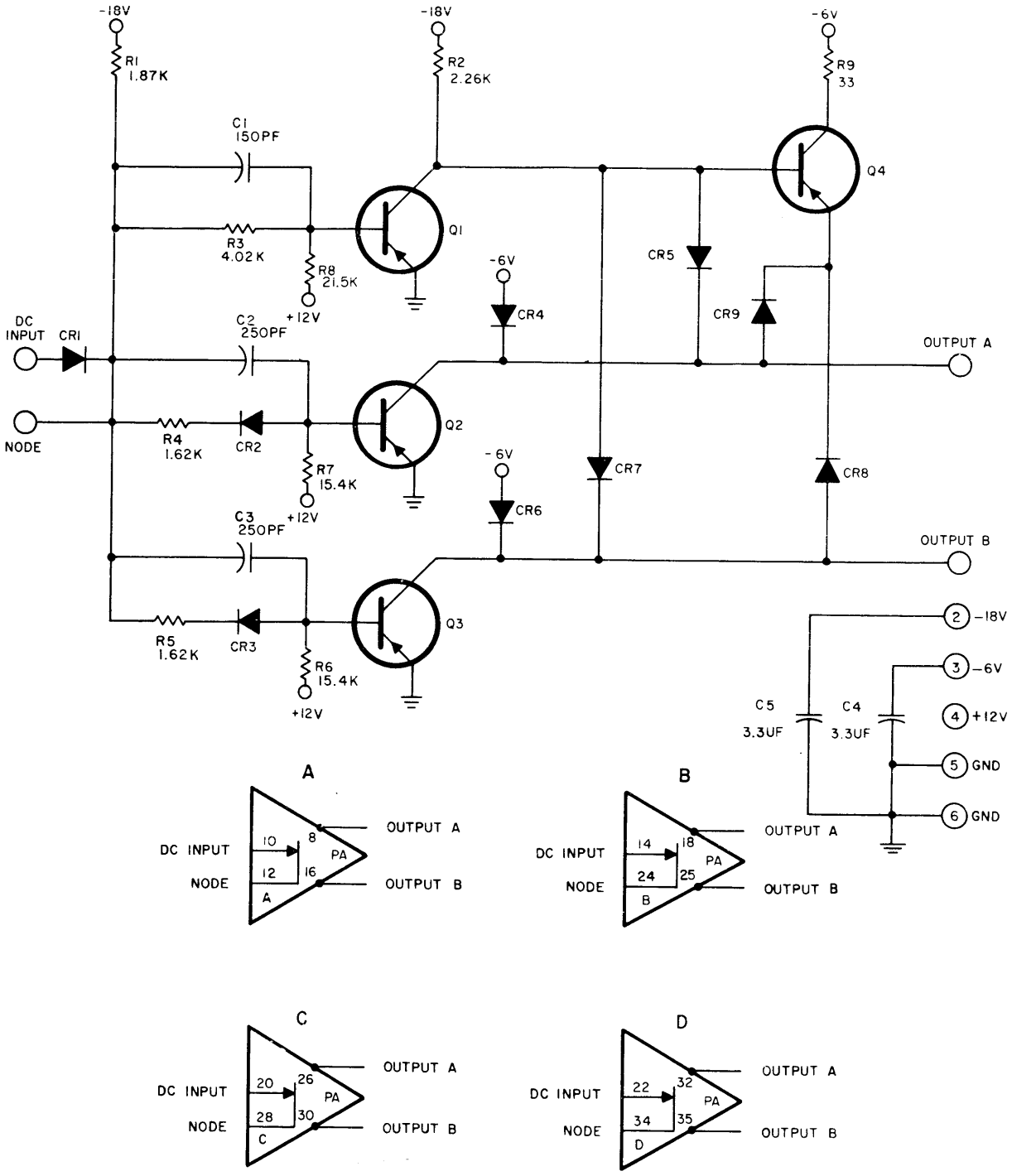


Figure 3-19.2. Power Amplifier PAC, Model PA-30, Schematic and Logic Diagram

3-20 NON-INVERTING POWER AMPLIFIER PAC, MODEL PN-30

GENERAL DESCRIPTION

The Non-Inverting Power Amplifier PAC, Model PN-30 (figures 3-20.1 and 3-20.2), contains four independent non-inverting power amplifiers. Each power amplifier has two diode-coupled inputs, an input node, and a single output. A two-stage amplifier, each inverting the logic level, produces the non-inverted output.

Logically, the circuit acts as an AND gate with conventional S-PAC negative logic inputs. For a single input signal, the amplifier output is the same as the input. For more than one input, the output is ZERO when any of the inputs is ZERO and logic ONE only when all inputs are ONE.

Non-inverting power amplifier PACs are useful for combining the AND gating function with power amplification. These PACs can also drive heavy loads without logical inversion.

CIRCUIT FUNCTION

The PN-30 circuit (figure 3-20.3) consists of a two-input gate, expandable to 10 inputs, followed by a non-inverting power amplifier. High logic gain is achieved by two cascaded, grounded emitter amplifiers. A fast output transition is attained by using the "totem pole" configuration. The common output pins provide additional output connections for load distribution.

SPECIFICATIONS

Input Loading

1 unit load each

Circuit Delay

0.20 μsec (max)
0.12 μsec (typ)

Output Drive Capability

40 unit loads and 2000 pf stray capacitance

Total Power

1.6 watts

Polarization

Pins 6 and 28

Current Requirements

-18 V	103 ma
- 6 V	37 ma (reverse current into supply)
+12 V	7 ma

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time:	0.10 μsec (typ)
Fall time:	0.15 μsec (typ)

Handle Color Code

Long:	Green
Short:	Yellow

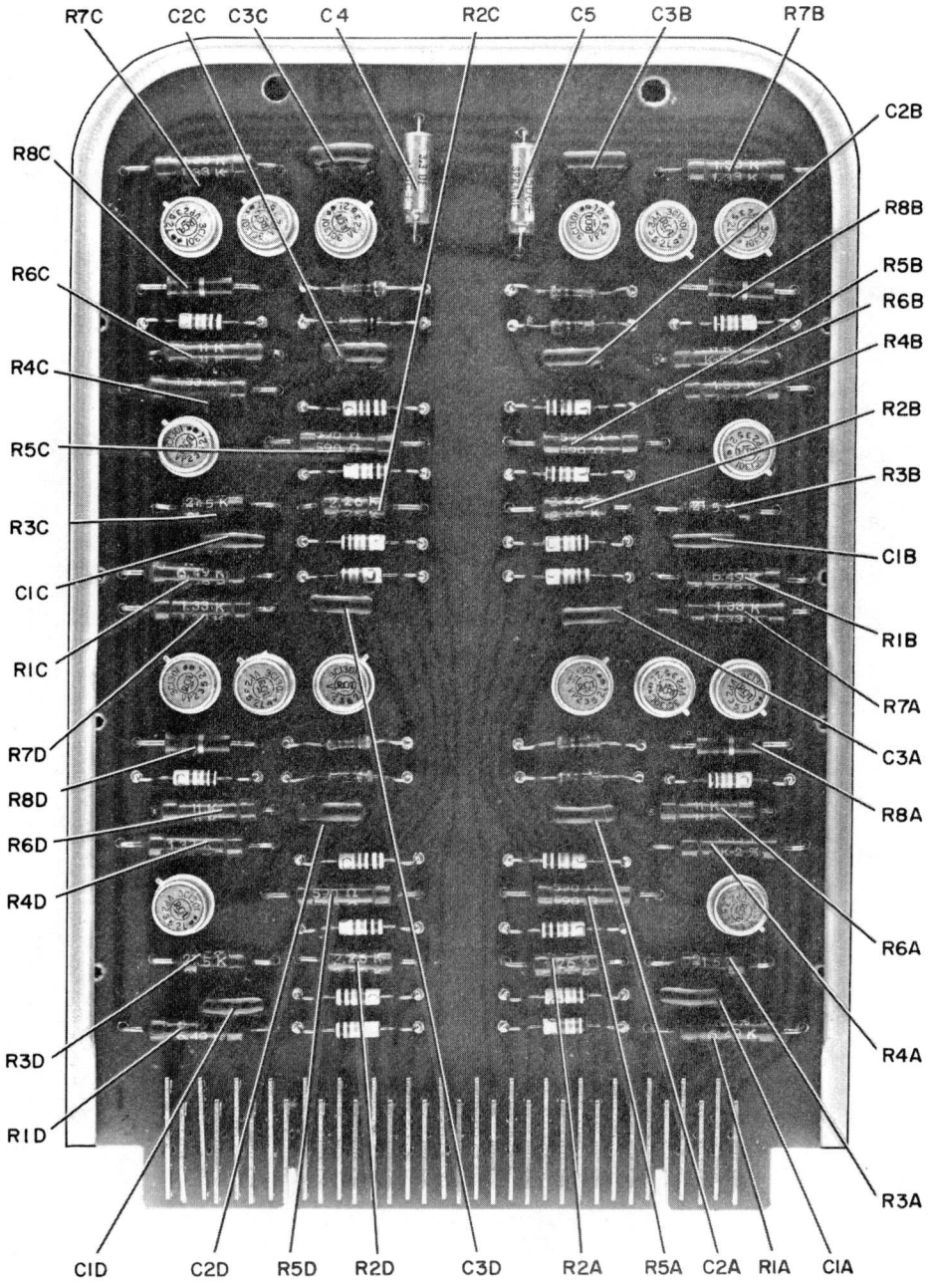


Figure 3-20.1. Non-Inverting Power Amplifier PAC, Model PN-30, Parts Location (Resistors and Capacitors)

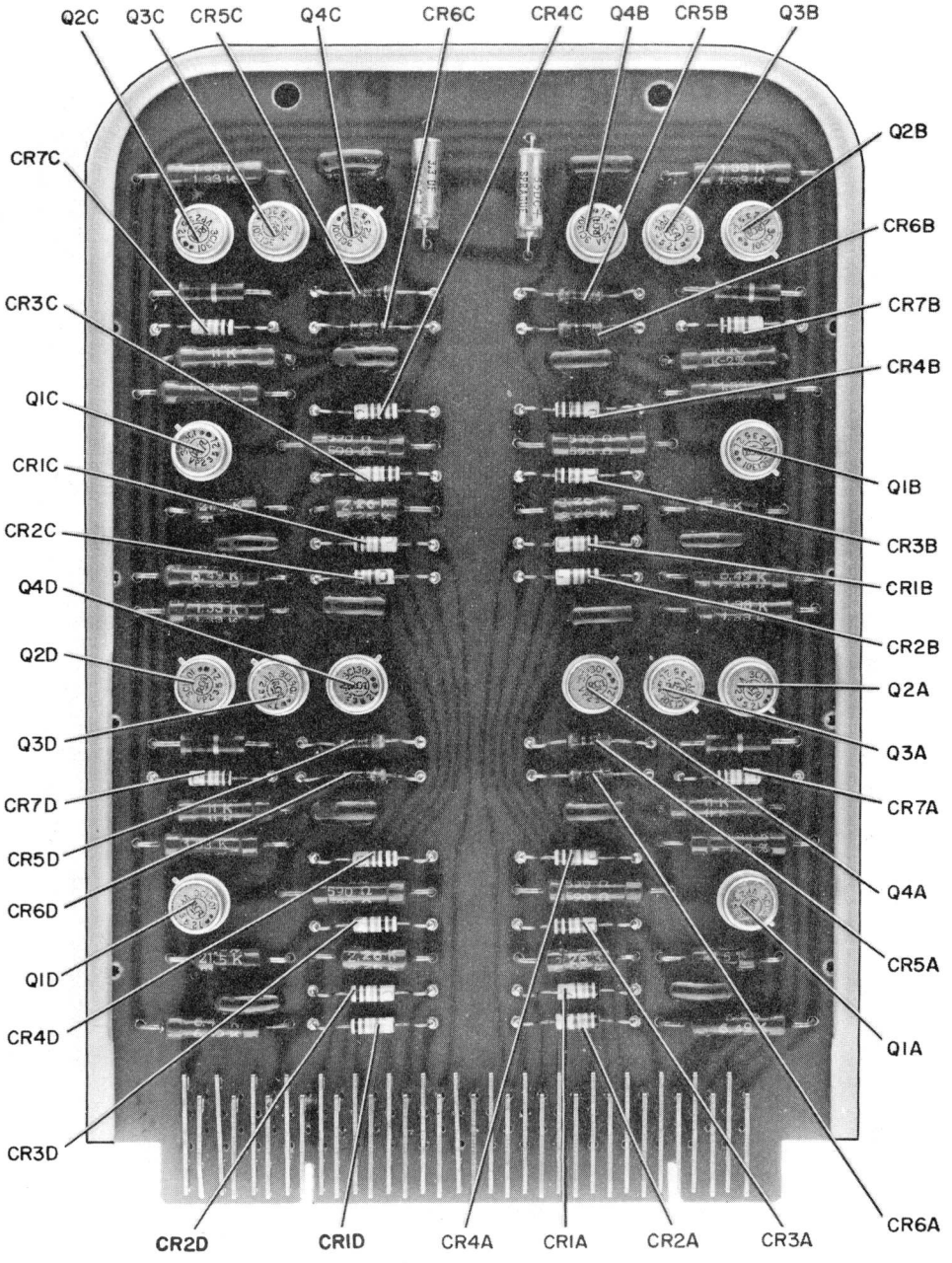


Figure 3-20.2. Non-Inverting Power Amplifier PAC, Model PN-30, Parts Location (Diodes and Transistors)

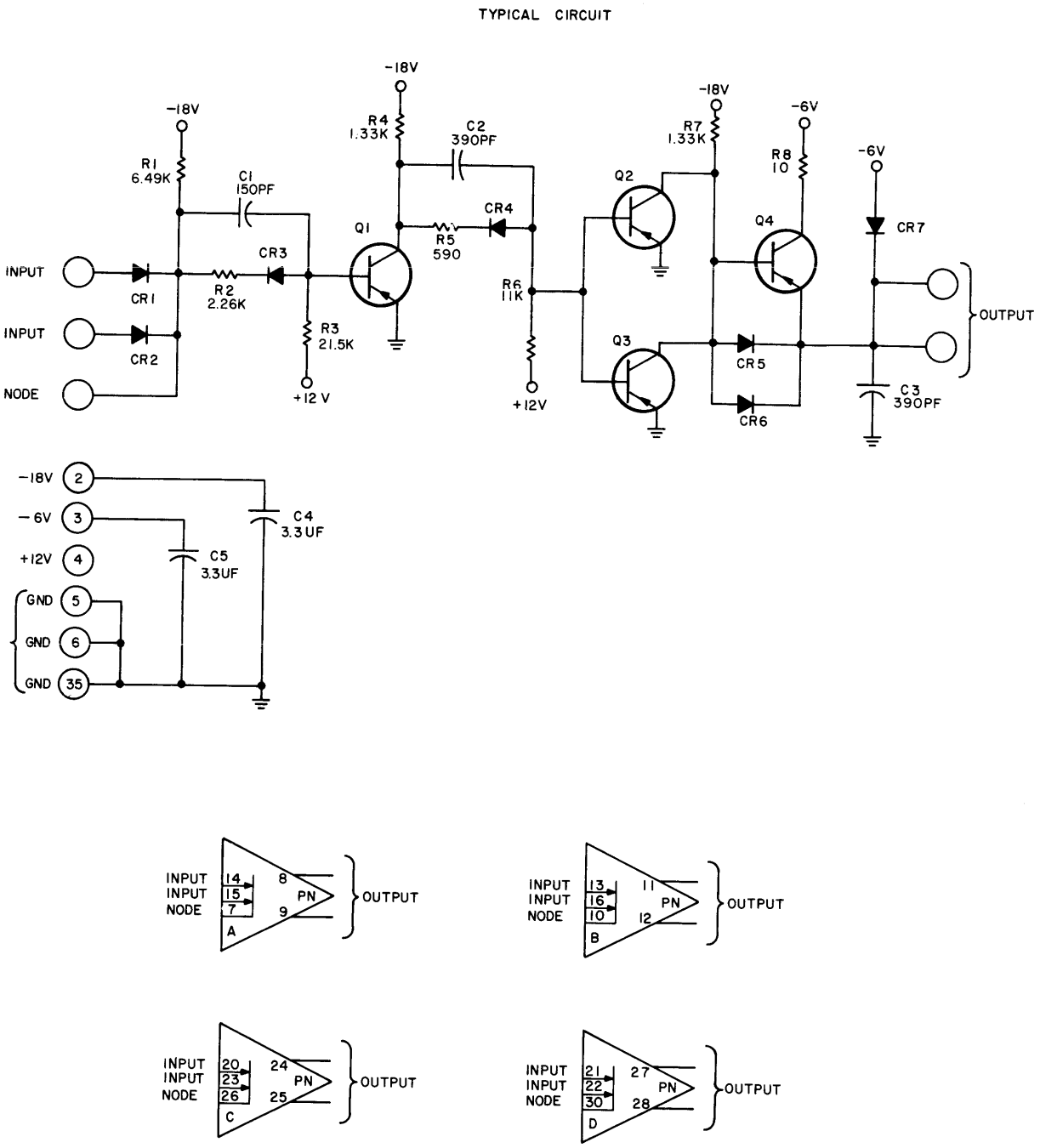


Figure 3-20.3. Non-Inverting Power Amplifier PAC, Model PN-30, Schematic and Logic Diagram

3-21 SERIAL MEMORY PAC, MODEL SM-30

GENERAL DESCRIPTION

The Serial Memory PAC, Model SM-30 (figures 3-21.1 and 3-21.2), is an integral element of S-PAC systems which stores serial binary data. The SM-30 can store data up to 2048 microseconds at any clock rate up to and including 1 megacycle. Longer delay lines are available on the SM-30L PAC. Customer specifications always govern the length of each delay line installed in every SM-30 PAC.

The delay line element is a magnetostrictive delay line with nickel alloy input-output transducers. This element offers a temperature coefficient of less than 10 PPM/°C.

The SM-30 PAC is driven by standard S-PAC signal levels and system clock pulses and provides properly delayed standard S-PAC signal levels as outputs. The SM-30 consists of input logic gating, a pulse shaper (triggered by an AC clock input), a delay line driver, a delay line element, two high-gain amplifiers, an emitter follower, a detector, and a flip-flop output.

The SM-30 plugs into a standard S-BLOC in a single connector. In a high-density BLOC (BL-32 or BL-33), the SM-30 requires two card slots for delays up through 1500 μsec and three slots for delays from 1501 to 2048 μsec. In a low-density BLOC (BL-30 or BL-31), two card slots are required for delays up to 2048 μsec. The delay line is connected to the etched side of the card and, as such, will result in the unused connectors being on the low-order side of the slots allocated for the SM-30.

CIRCUIT FUNCTION

Signals for the SM-30 (figure 3-21.3) are applied to the PAC through four input AND gates. Each of these gates has a node connection by which the gate can be expanded up to 10 inputs. Each gate is expanded by connecting diode clusters, such as those on the DC-30 PAC, to the appropriate node. In addition, the OR gate structure of the input circuits has a node input with an OR function diode which expands the input capacity of the SM-30 when connected to external AND gates. Application of all ONEs (-6 V) to an AND gate input results in a sequential pulse excursion through the pulse shaper, delay line driver, delay line, both high-gain amplifiers, the emitter follower, and the difference amplifier (detector). This sets the output flip-flop. The application of a ZERO (0 V) inhibits the entire circuit chain and resets the output flip-flop.

An unused AND gate must be tied to a ZERO level. All four gate outputs are connected to an OR structure to drive a standard inverter. The output of the inverter activates a clock gate level control.

With the coincidence of logic ONEs on the input gate, the inverter is turned on, activating the level control of the AC clock gate. In the presence of a ONE, the positive-going trailing edge of the clock pulse triggers the pulse shaper and converts the standard S-PAC NRZ (nonreturn-to-zero) levels into RZ (return-to-zero) levels for insertion into the delay line. The pulse is shaped to approximately a 9-volt amplitude and 500-nanosecond bandwidth, independent of clock rate, data rate, and delay.

The input signal to the delay line is differentiated twice, once by the input transducer and again by the output transducer. The delayed and attenuated output signal from the delay line is amplified by two high-gain, iterative amplifiers. The output from the first amplifier, available at test point TP1 is approximately 0.25 volt in amplitude. The output from the second amplifier, available at test point TP2, is approximately 2.5 volts in amplitude, and, through an isolating emitter follower, triggers the detector circuits.

The detector is an emitter-coupled difference amplifier with a transistor switch which shunts the difference amplifier emitter current source. In the quiescent state, the transistor switch conducts, shunting the difference amplifier current. Application of any clock pulse to the switch turns it off, permitting current to flow through the difference amplifier. The set and reset outputs from the detector are connected to the set and reset sides of a standard flip-flop FF-30 output circuit.

When there is coincidence between the system clock pulse and the double differentiated output from the delay line, the emitter current is conducted through the set side of the difference amplifier. In the absence of a signal from the delay line, the emitter current is conducted through the reset side of the difference amplifier and the output flip-flop is reset.

Logically, the SM-30 operates like a shift register whose length is equal to the specified number of digits of the delay. However, the SM-30 shifting occurs precisely at the clock rate. Consequently, when data enters the delay line element, it cannot be inhibited, slowed, or stopped.

SPECIAL FEATURES

A special DC clear input to the SM-30 permits the clearing of all data from the delay line. When a 0-volt signal is applied to this input, all ZEROs enter the line.

Recirculation of data in the delay line is accomplished by direct feedback from the flip-flop outputs to the input logic. Recirculation can serve in the system control, troubleshooting, and adjustment of the delay line element. Each SM-30 is factory adjusted to customer specifications. However, if it becomes necessary to adjust the SM-30 for any system timing discrepancies, data can be recirculated and observed comparatively while the timing adjustment is performed. A screwdriver adjustment is at the rear of the delay line element.

Turret lugs are connected to the collectors of output amplifiers Q6 and Q8 to provide test point facilities for monitoring and troubleshooting. These lugs are readily accessible from the rear of the S-BLOC and are indicated as TP1 and TP2 in figure 3-21.3.

NOTE

One leg of any unused AND gate must be tied to ground to prevent a continuous ONE input.

SPECIFICATIONS

Input Loading

DC inputs: 1 unit load each
AC inputs: 4 unit loads each
DC clear: 4 unit loads

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each output

Total Power

3.6 watts

Polarization

Pins 20 and 28

Timing for AC Inputs

Standard S-PAC pulse (figure 2-1.1)

Current Requirements

-18 V 165 ma
-6 V 60 ma (reverse current into supply)
+12 V 22 ma

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Handle Color Code

Long: Green
Short: Black

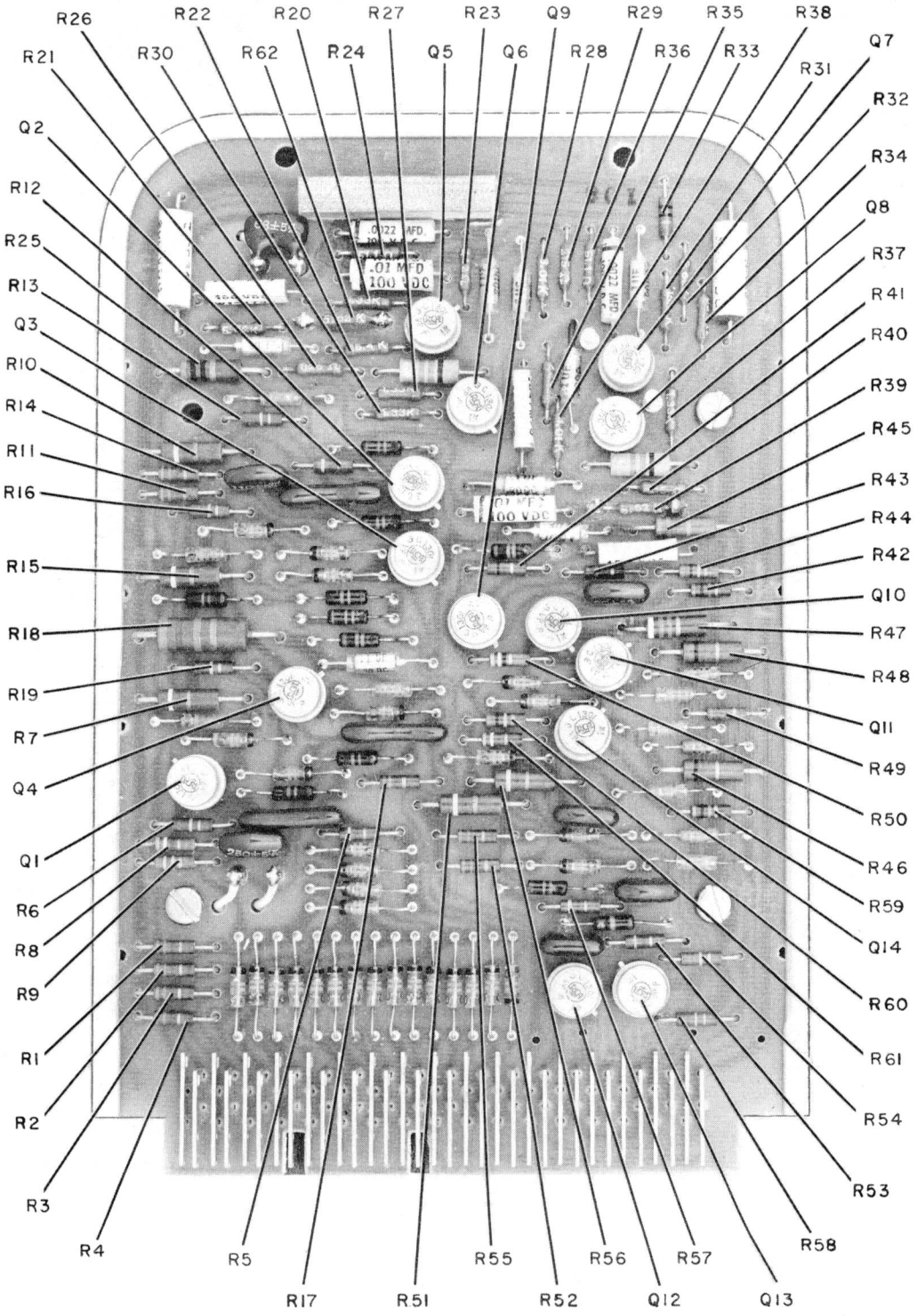


Figure 3-21.1. Serial Memory PAC, Model SM-30,
Parts Location (Resistors and Transistors)

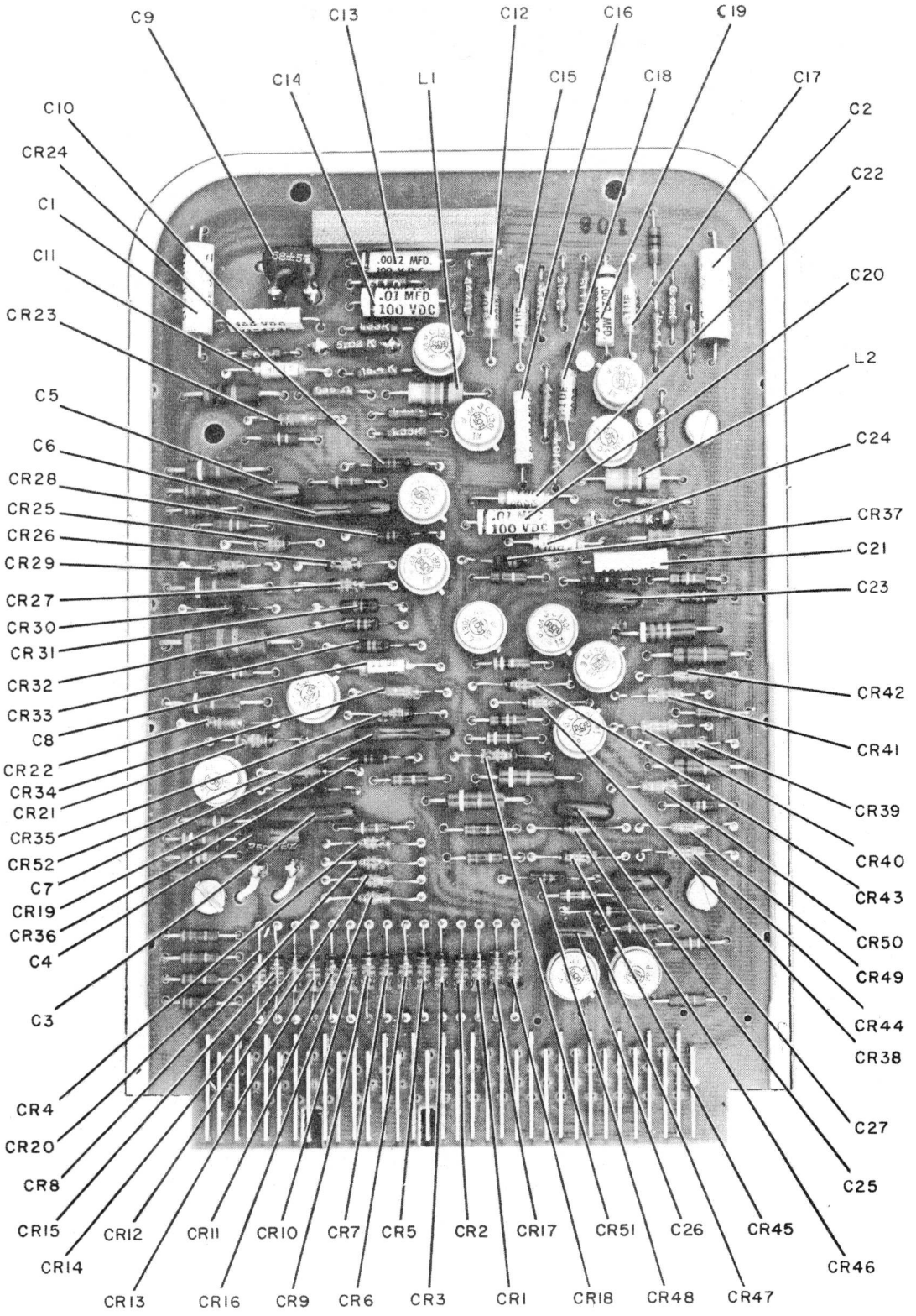
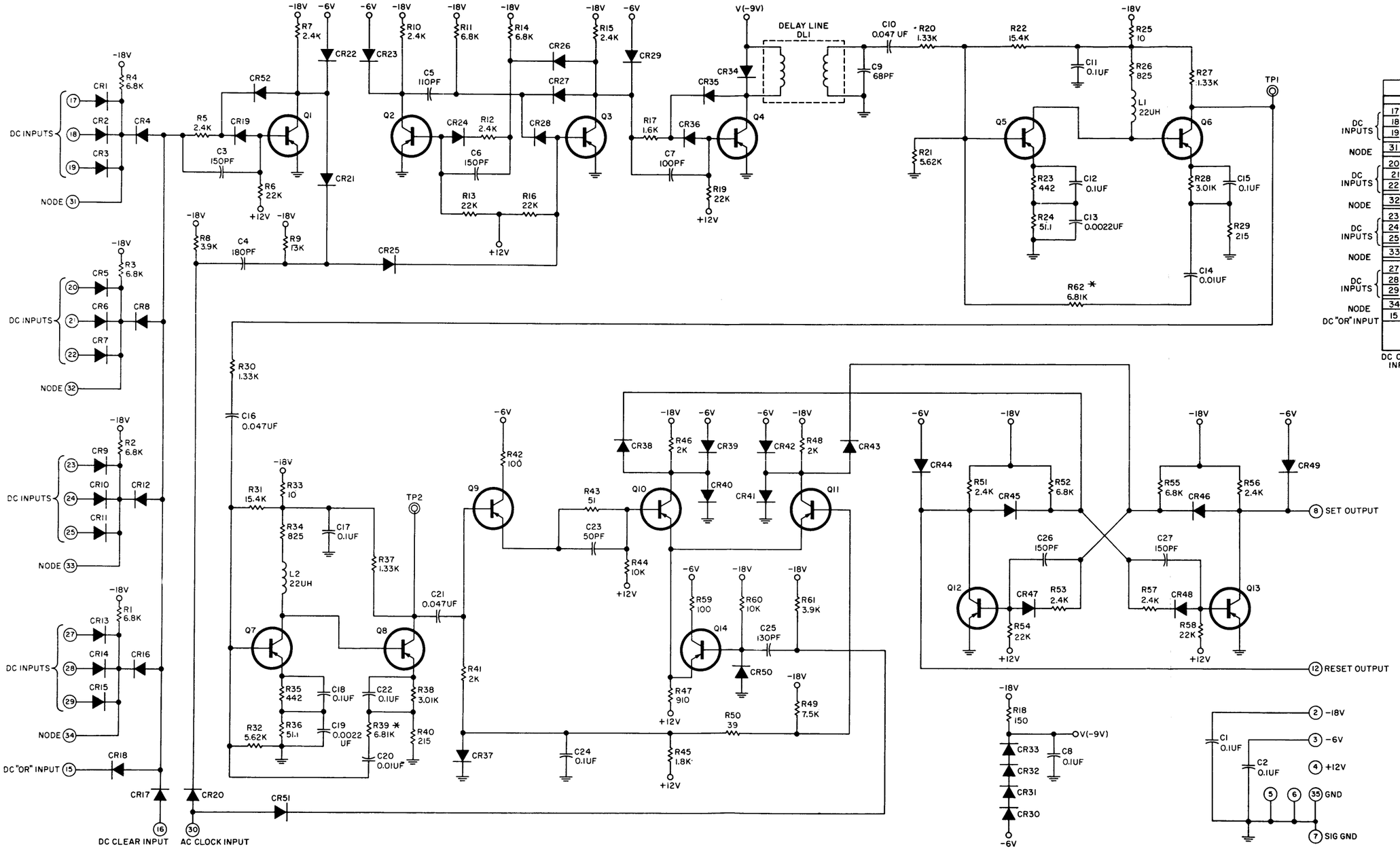


Figure 3-21.2. Serial Memory PAC, Model SM-30, Parts Location (Capacitors, Diodes, and Inductors)



* R39 AND R62 ARE TRIMMER RESISTORS

Figure 3-21.3. Serial Memory PAC, Model SM-30, Schematic and Logic Diagram

3-22 SERIAL MEMORY PAC, MODEL SM-30L

GENERAL DESCRIPTION

The Serial Memory PAC, Model SM-30L (figures 3-22.1), is an integral element of S-PAC systems which stores serial binary data. The SM-30L can store data up to 5,000 microseconds at any clock rate up to and including 1 megacycle. Customer specifications always govern the length of each delay line installed in every SM-30L PAC.

The delay line element is a magnetostrictive delay line with nickel alloy input-output transducers. This element offers a temperature coefficient of less than 10 PPM/°C.

The SM-30L PAC is driven by standard S-PAC signal levels and system clock pulses and provides properly delayed standard S-PAC signal levels as outputs. The SM-30L consists of input logic gating, a pulse shaper (triggered by an AC clock input), a delay line driver, a delay line element, two high-gain amplifiers, an emitter follower, a detector, and a flip-flop output.

CIRCUIT FUNCTIONS

Signals for the SM-30L (figure 3-22.3) are applied to the PAC through four input AND gates. Each AND gate has a node connection by which the gate can be expanded up to 10 inputs. Each gate is expanded by connecting diode clusters, such as those on the DC-30 PAC, to the appropriate node. In addition, the OR gate structure of the input circuits has a node input with an OR function diode which expands the input capacity of the SM-30L when connected to external AND gates. Application of all ONEs (-6 V) to an AND gate input results in a sequential pulse excursion that passes through the pulse shaper, delay line driver, delay line, both high-gain amplifiers, the emitter follower, and the difference amplifier (detector). This sets the output flip-flop. The application of a ZERO (0 V) inhibits the entire circuit chain and resets the output flip-flop.

An unused AND gate must be tied to a ZERO level. All four gate outputs are connected to an OR structure to drive a standard inverter (Q1). The output of inverter Q1 activates a clock gate level control.

With the coincidence of logic ONEs on the input gate, the inverter is turned on, activating the level control of the AC clock gate. In the presence of a ONE, the positive-going trailing edge of the clock pulse triggers the pulse shaper and converts the standard S-PAC NRZ (nonreturn-to-zero) levels into RZ (return-to-zero) levels for insertion into the delay line. The pulse is shaped to approximately an 18-volt amplitude and 500-nanosecond bandwidth independent of clock rate, data rate, and delay.

The input signal to the delay line is differentiated twice, once by the input transducer and again by the output transducer. The delayed and attenuated output signal from the delay line is amplified by two high-gain, iterative amplifiers. The output signal from the first amplifier (Q5 and Q6), available at test point TP1, is approximately 0.25 volt in amplitude. The output signal from the second amplifier (Q7 and Q8), available at test point TP2, is approximately 2.5 volts in amplitude. The signal is coupled through an isolating emitter follower (Q9) and triggers the detector circuits.

The detector is an emitter-coupled difference amplifier (Q10 and Q11) with a transistor switch (Q14) which shunts the difference amplifier emitter current source. In the quiescent state, the transistor switch conducts, shunting the difference amplifier current. Application of a clock pulse to the switch turns it off, permitting current to flow through the difference amplifier. The set (Q10) and reset (Q11) outputs from the detector are connected to the set and reset inputs, respectively, of a standard flip-flop FF-30 output circuit.

When there is coincidence between the system clock pulse and the output from the delay line, the emitter current flows through the set side of the difference amplifier and the output flip-flop is set. In the absence of a signal from the delay line, the emitter current flows through the reset side of the difference amplifier and the output flip-flop is reset.

Logically, the SM-30L operates like a shift register whose length is equal to the specified number of digits of the delay. However, the SM-30L shifting occurs precisely at the clock rate. Consequently, when data enters the delay line element, it cannot be inhibited, slowed, or stopped.

SPECIAL FEATURES

A special DC clear input to the SM-30L permits clearing of all data from the delay line. When a 0-volt signal is applied to this input, all ZEROs enter the line.

Recirculation of data in the delay line is accomplished by direct feedback from the flip-flop outputs to the input logic. Recirculation can serve in the system control, troubleshooting, and adjustment of the delay line element. Each SM-30L is factory adjusted to customer specifications. However, if it becomes necessary to adjust the SM-30L for any system timing discrepancies, data can be recirculated and observed comparatively while the timing adjustment is performed. A screwdriver adjustment is at the rear of the delay line element (figure 3-22.4).

Turret lugs are connected to the collectors of output amplifiers Q6 and Q8 to provide test point facilities for monitoring and troubleshooting. These lugs are readily accessible from the rear of the S-BLOC and are indicated as TP1 and TP2 in figure 3-22.3.

NOTE

One leg of any unused AND gate must be tied to ground to prevent a continuous ONE input.

SPECIFICATIONS

Input Loading

DC inputs: 1 unit load each
AC inputs: 4 unit loads each
DC clear: 4 unit loads

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each output

Total Power

3.6 watts

Polarization

Pins 20 and 28

Timing for AC Inputs

Standard S-PAC pulse (figure 2-1.1)

Current Requirements

-18 V: 165 ma
- 6 V: 60 ma (reverse current into supply)
+12 V: 22 ma

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Handle Color Code

Long: Green
Short: Black

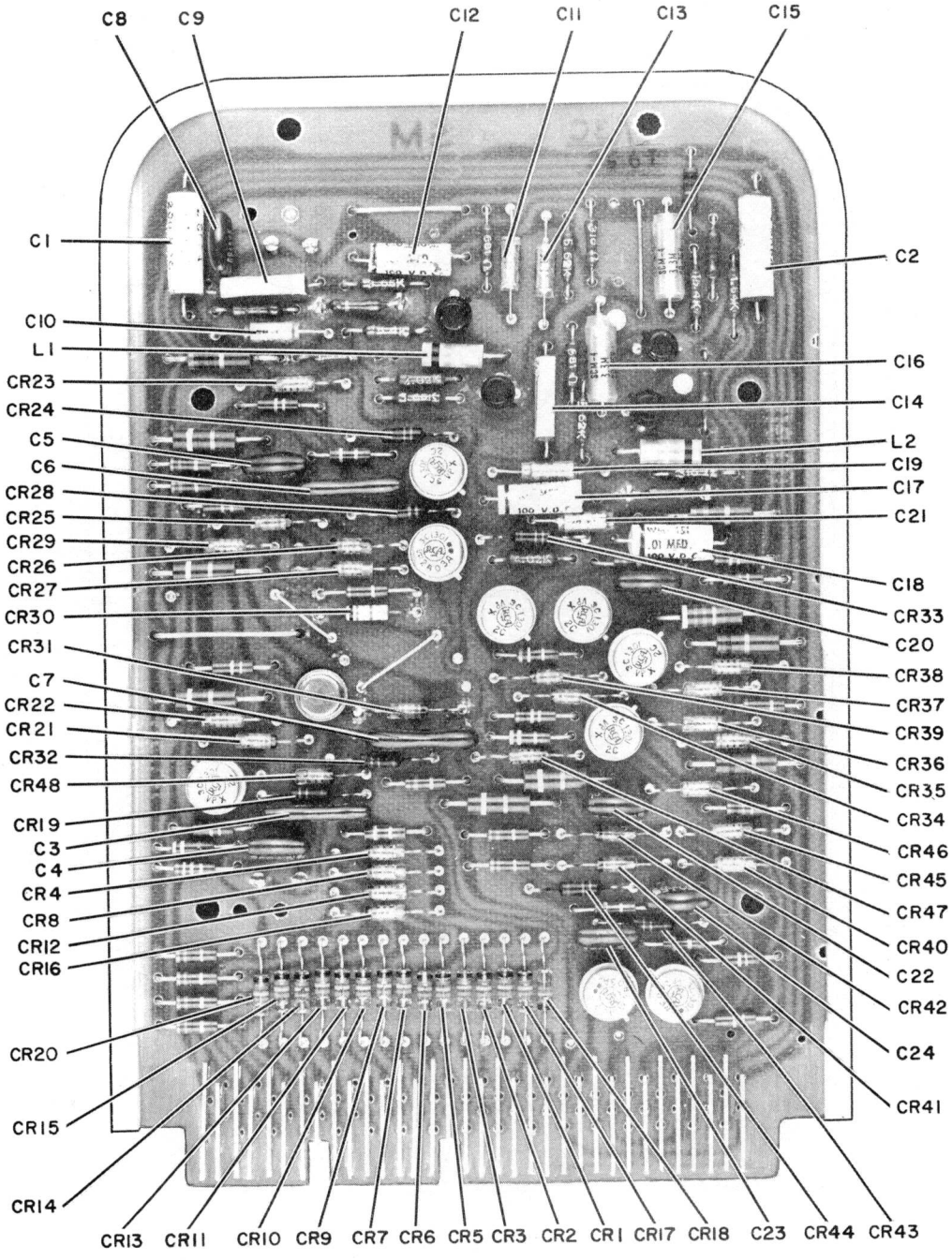


Figure 3-22.1. Serial Memory PAC, Model SM-30L, Parts Location (Capacitors, Diodes, and Inductors)

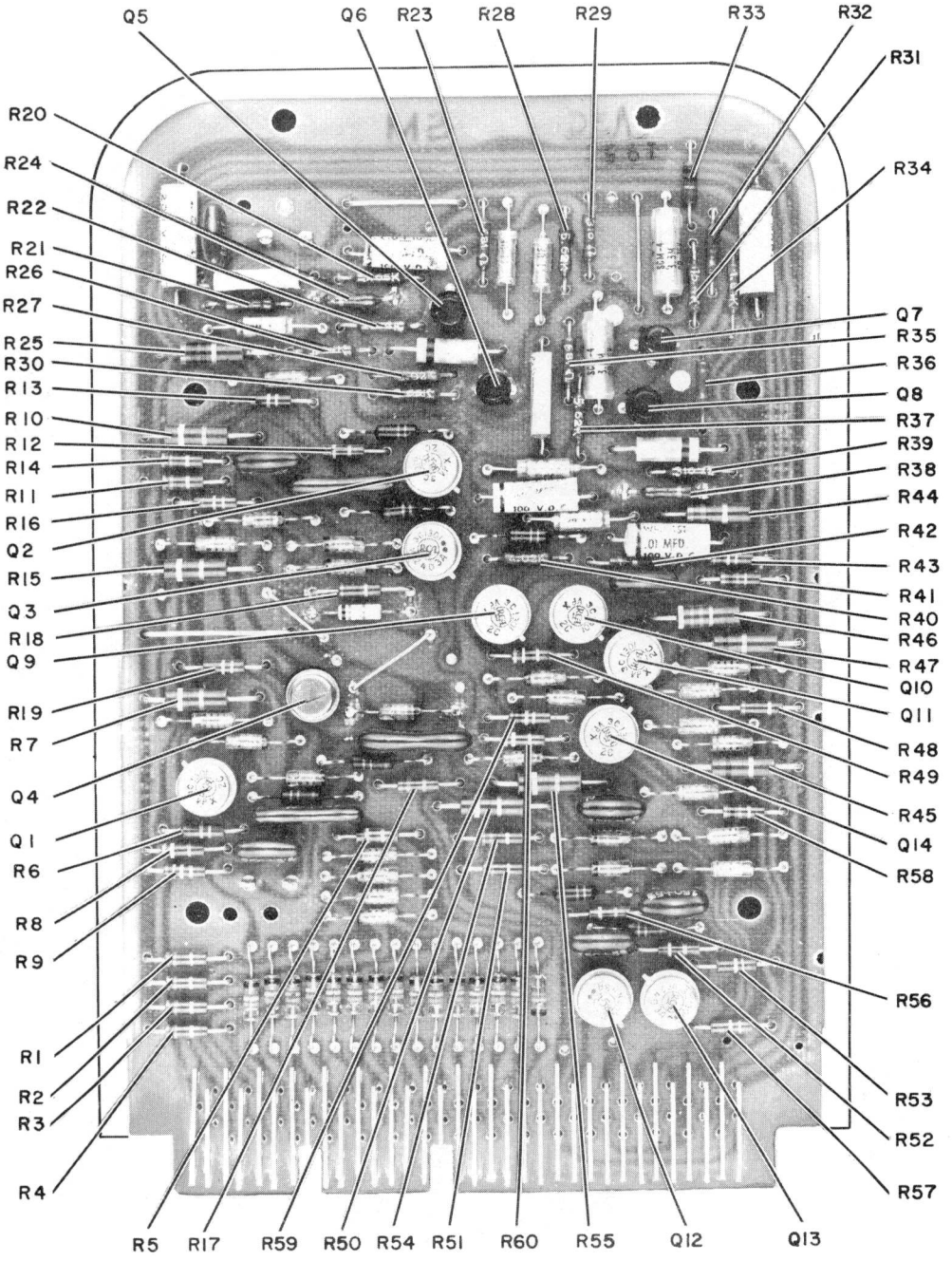


Figure 3-22.2. Serial Memory PAC, Model SM-30L, Parts Location (Resistors and Transistors)

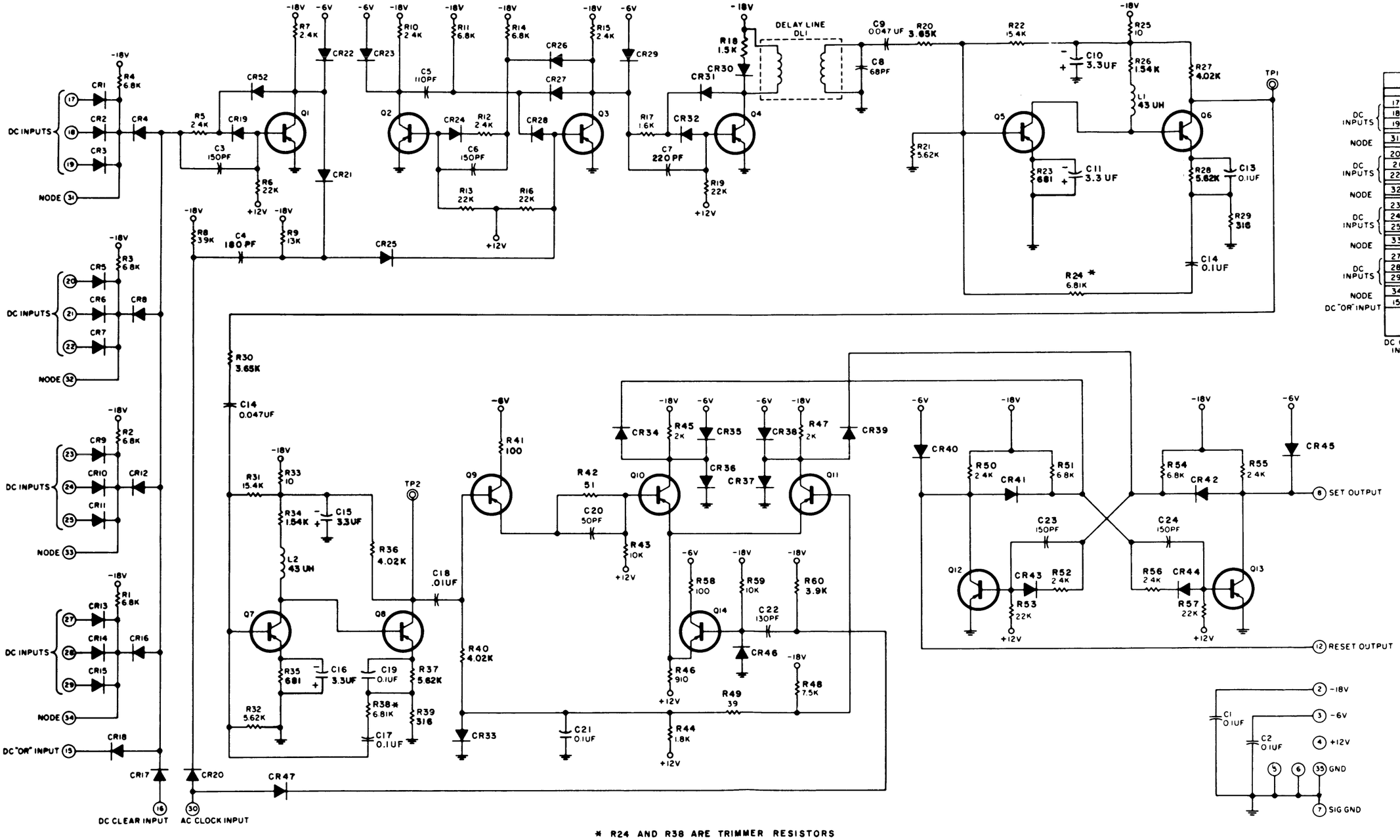


Figure 3-22.3. Serial Memory PAC, Model SM-30L, Schematic and Logic Diagram

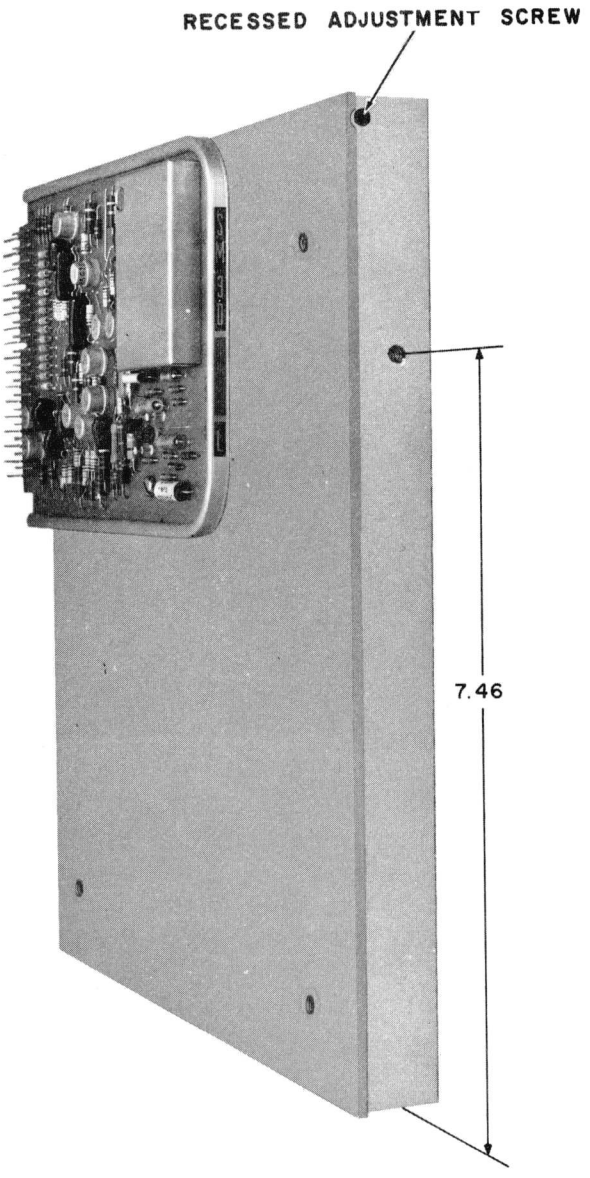


Figure 3-22.4. Serial Memory PAC, Model SM-30L, Recessed Adjustment Screw Location

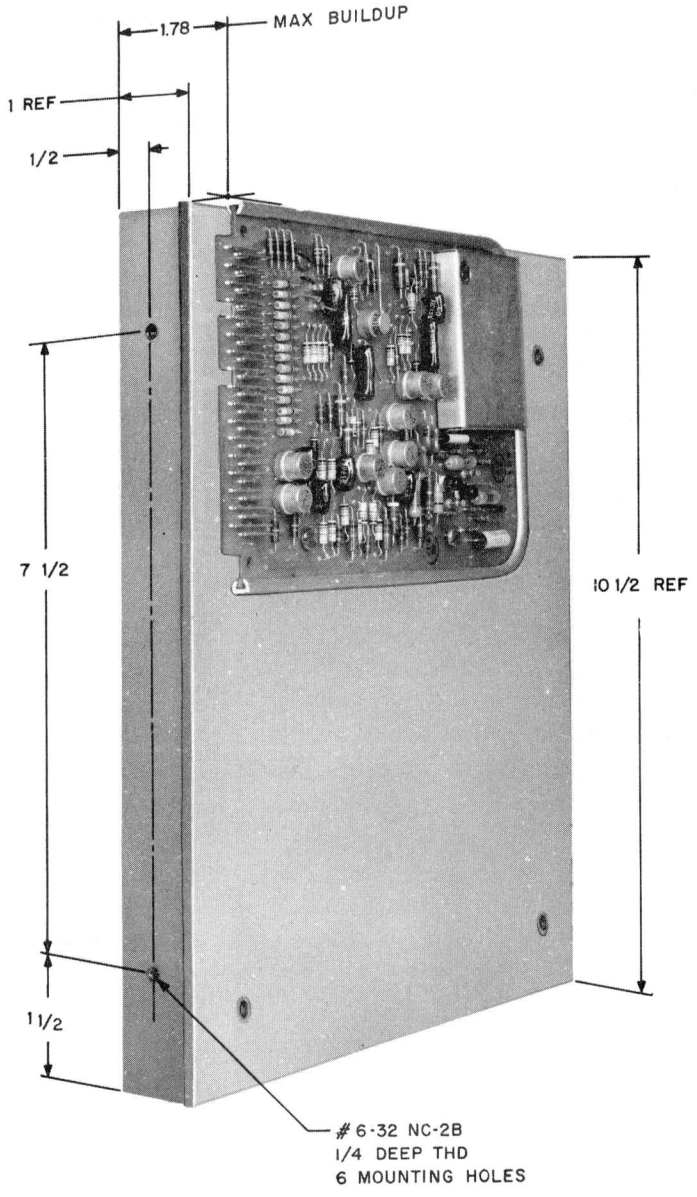


Figure 3-22.5. Serial Memory PAC, Model SM-30L, Assembly Reference Dimensioning

3-23 SHIFT REGISTER PAC, MODEL SR-30

GENERAL DESCRIPTION

The Shift Register PAC, Model SR-30 (figures 3-23.1 and 3-23.2), contains four prewired flip-flops capable of operating in serial-parallel, parallel-serial, and serial-serial modes. DC set and reset inputs permit the parallel-loading of information. A common reset input is provided for clearing all stages simultaneously. The shift input incorporates trailing edge triggering. This allows the output of the register to be gated with the shift signal without the use of delay circuits or two-phase clocks. The first stage of each register has DC set and reset information inputs for serial entry of information and cascading shift registers.

CIRCUIT FUNCTION

The basic circuit (figure 3-23.3) of each stage consists of two cross-coupled NAND gates with the addition of the shift-gating circuit.

DC Set and Reset. The DC set and reset inputs are used to preset the register stage to a desired condition (parallel entry).

Common Reset. The common reset input is direct-coupled to the reset side of each stage. This permits the four stages to be cleared simultaneously by a single positive signal with a minimum width of 0.25 microsecond.

Shift-Gating Circuits. These circuits are common AC inputs with their level controls cross-coupled back to the outputs of the preceding stage. Thus, the set and reset level controls of each stage are conditioned by the state of the preceding stage and, when the shift line is activated by a positive-going signal, information is shifted to the next stage in the register.

Information Inputs (Set and Reset). The information inputs are level controls (set-pin 24, reset-pin 23) of the first stage of the SR-30 which determine what information is shifted into the SR-30. The level control inputs must be driven from complementary logic signals, such as the outputs of any S-PAC flip-flop. If the input data is presented from the output of a gate (single-ended), an inverter must be provided between the set and reset information inputs. Level controls are active when at ground potential, therefore the set and reset level controls should be connected to the reset and set outputs, respectively, of the driving flip-flop. Leaving both level controls open will disable the shift input, while having both controls at 0 volt at the time the shift input goes positive causes the first stage to assume an indeterminate state. When information is not being entered serially through the information inputs, tying the set and reset level control inputs to -6 volts and 0 volt, respectively, will cause the first stage to clear to reset when the shift line is activated.

NOTE

In all applications of the SR-30, pin 35 should be connected to pin 5 (ground). This jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Input Loading

DC set (reset) inputs: 1 unit load each

Shift input: 7 unit loads (common to four stages)

Common reset: 4 unit loads

Set (reset) level controls: 1/2 unit load each

Shift Rate

DC to 1 MC (max)

Shift Timing

Negative-going pulse: (trailing edge trigger) 0.6 μsec minimum width, -6 V amplitude

Positive-going pulse: 0.25 μsec minimum width, 6 V amplitude, 0.4 μsec maximum at 1 MC. In all cases, 0.6 μsec at -6 V is required preceding positive transition.

Total Power

1.7 watts

Polarization

Pins 4 and 6

Circuit Delay

(Measured at -3 V)

0.15 μsec (typ): DC reset input to set output or

0.25 μsec (max): DC set input to reset output

0.10 μsec (typ): DC set input to set output or

0.15 μsec (max): DC reset input to reset output

Setting time after shift: 0.25 μsec (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)

Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 100 ma

-6 V 41 ma (reverse current into supply)

+12 V 5 ma

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Handle Color Code

Long: Blue

Short: Red

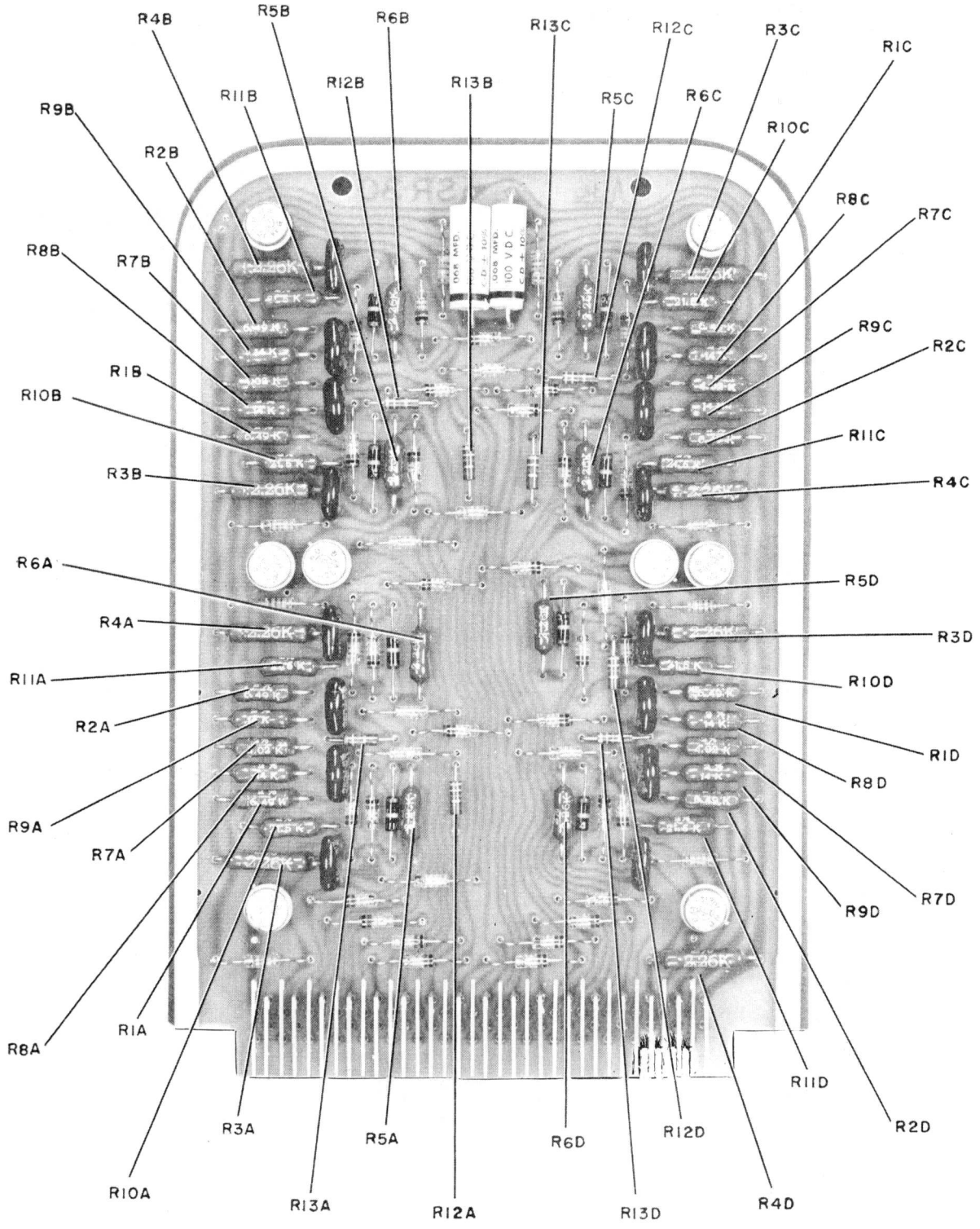


Figure 3-23.1. Shift Register PAC, Model SR-30,
Parts Location (Resistors)

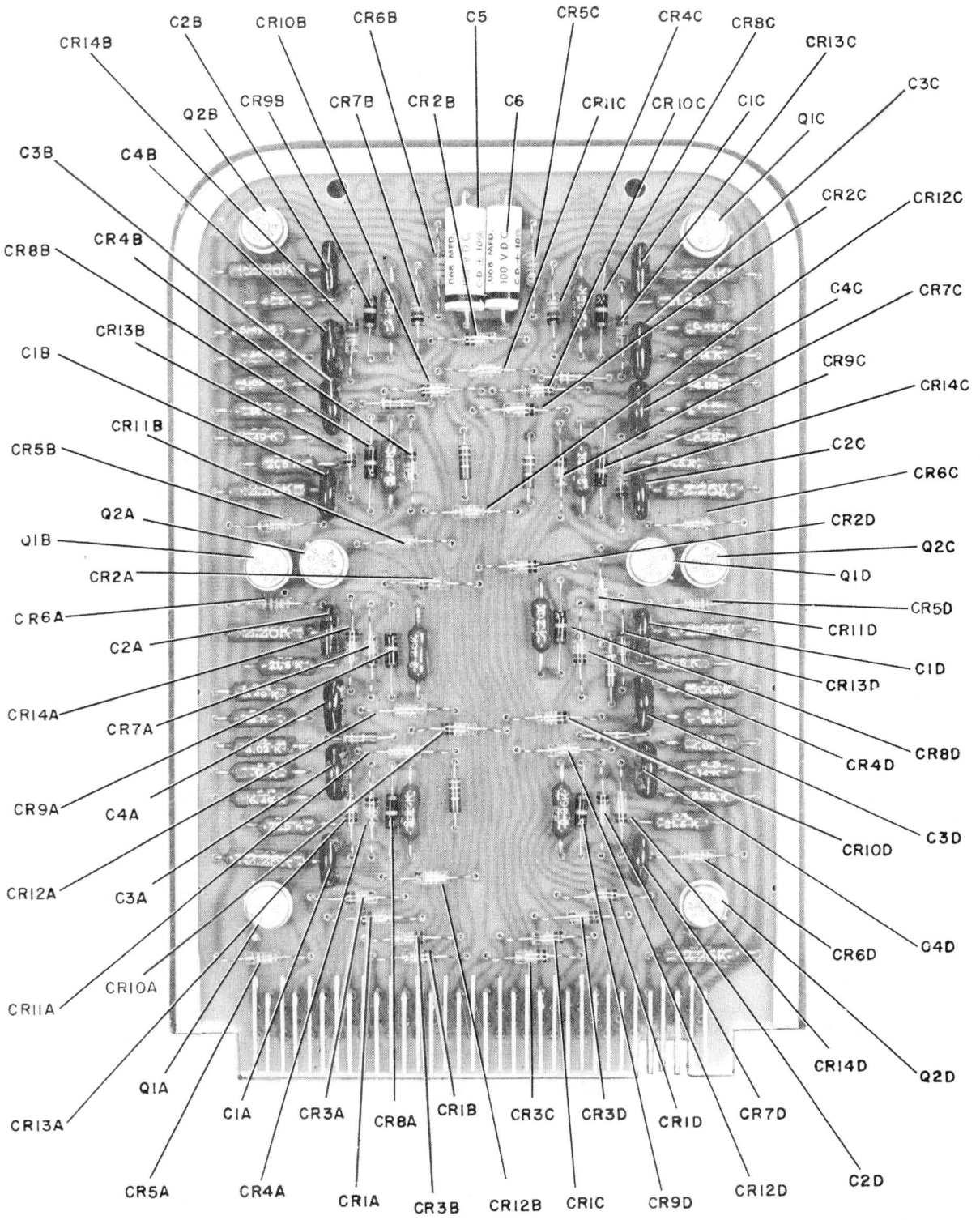
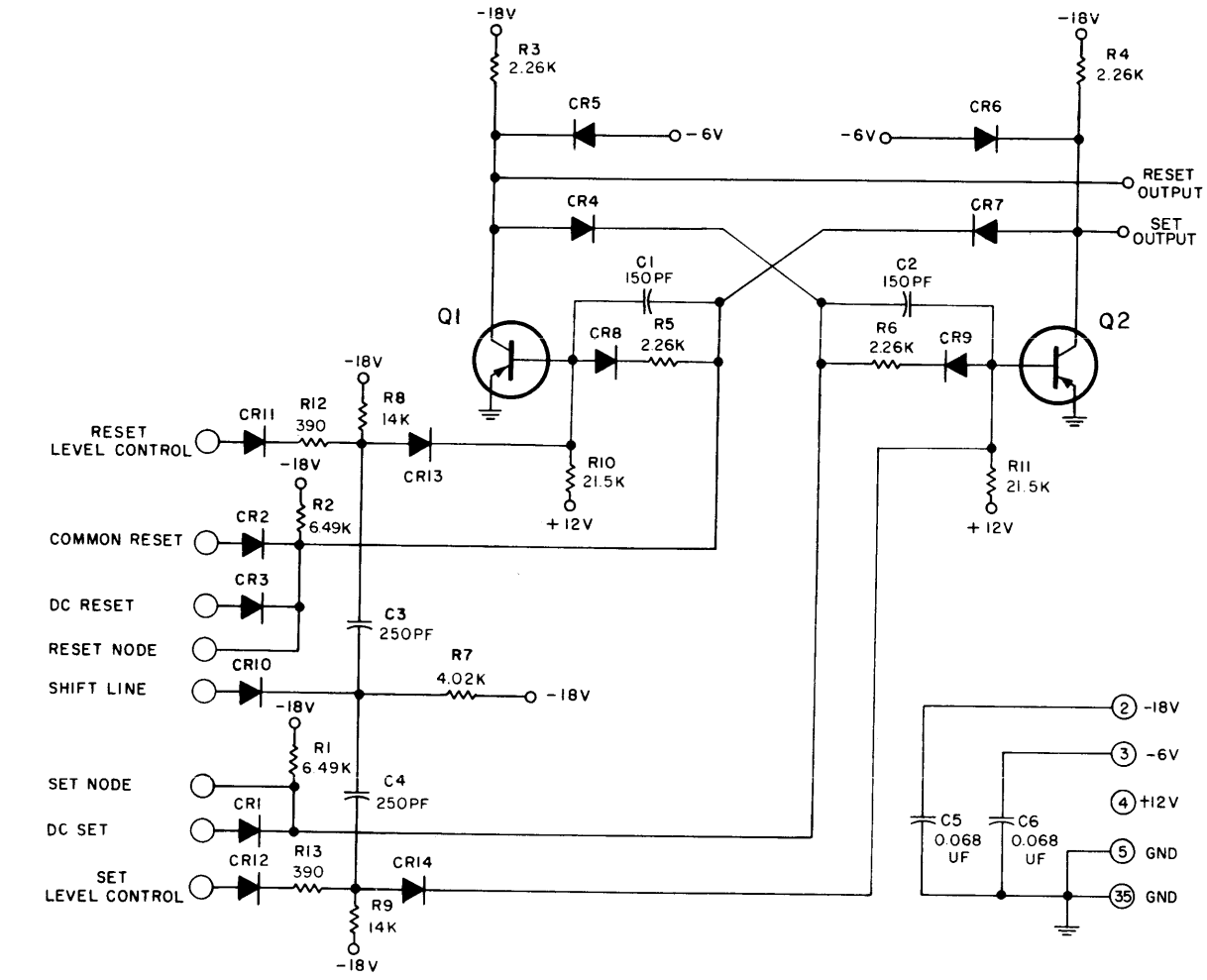


Figure 3-23.2. Shift Register PAC, Model SR-30, Parts Location (Capacitors, Diodes, and Transistors)



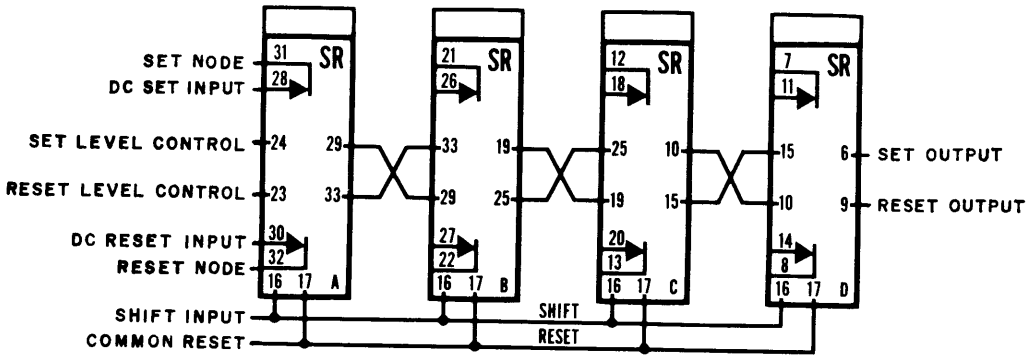


Figure 3-23.3. Shift Register PAC, Model SR-30, Schematic and Logic Diagram

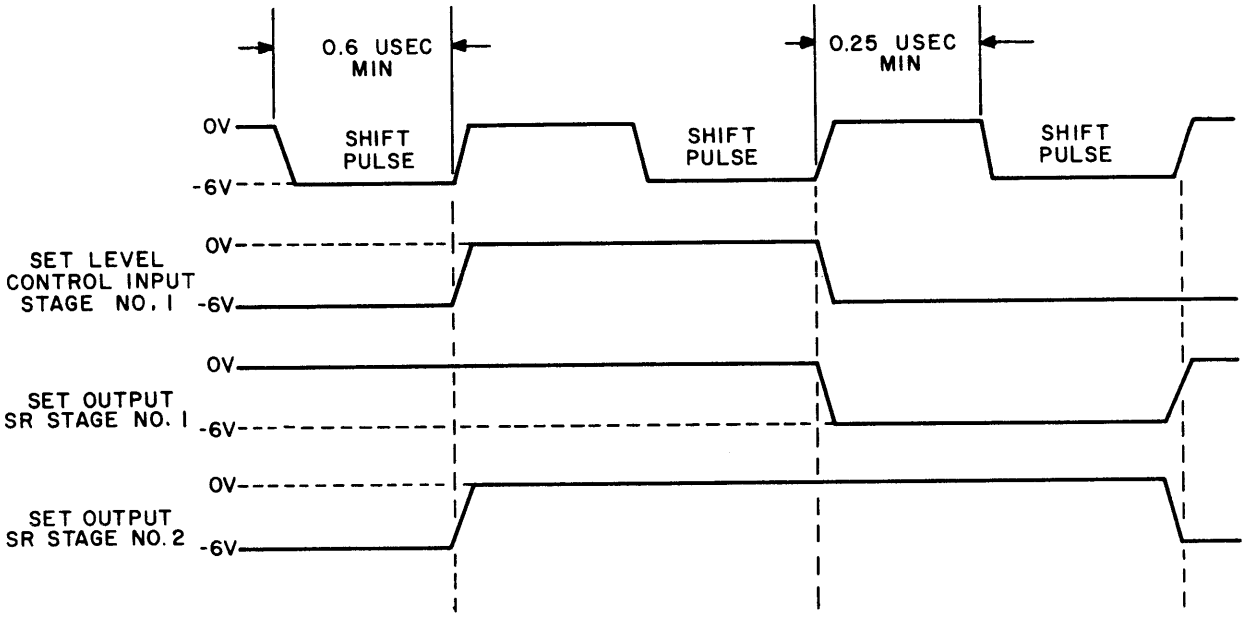


Figure 3-23.4. Shift Register Timing Diagram

3-24 UNIVERSAL FLIP-FLOP PAC, MODEL UF-30

GENERAL DESCRIPTION

The Universal Flip-Flop PAC, Model UF-30 (figures 3-24.1 and 3-24.2), contains two identical, independent flip-flops which can perform all functions of the other S-PAC flip-flops as well as additional logic functions. For example, the UF-30 can be wired as a left-right shift register or as a combined binary counter shift register.

Each stage has DC set and reset inputs which can be used for parallel-loading of information. Each stage also has three AC-coupled inputs. One AC input is common to both set and reset inputs and can be wired for shifting or complementing. The remaining two AC inputs and their associated level control inputs provide independent set and reset gates on each stage.

CIRCUIT FUNCTION

The two UF-30 circuits (figure 3-24.3) are independent and identical. The basic circuit of each stage consists of two cross-coupled NAND gates.

AC Set (Reset) Input and Level Control. The AC set (reset) input and associated level control form a two-input gate which, when properly activated, causes the flip-flop to assume the set (reset) state. The change of the state of the flip-flop results from applying a positive-going, 6-volt step on the AC set (reset) input with the level control input at ground. The circuit function is that of a pedestal gate in which the step is differentiated and applied to the flip-flop input through a biased diode. The level control input conditions are such that when a ONE (-6 V) control signal is applied, the differentiated step is blocked. However, when a ZERO (0 V) is applied, the differentiated step is gated into the flip-flop and causes the change of state.

Common AC Input. The common AC input is associated with two level controls which are essentially similar in function to those associated with the AC set and reset inputs. These level controls serve to steer signals applied to the common AC input to either the set or reset side of the flip-flop. Thus, when the associated level control inputs are connected to another flip-flop to form a shift register, the common AC input serves as the shift input. When the level control inputs are tied back to their own outputs, the UF-30 functions as complementary stages for pulses applied at its AC input. Refer to tables 3-24.1 and 3-24.2.

When the AC set and reset inputs are connected, their function becomes identical to that of the common AC input, except that DC loading is doubled (four loads rather than two).

Timing. There are two modes of operation for AC inputs with level controls. The first is the pulse mode of operation, which is defined as the condition where the level control signal switches negative when the AC input signal is positive. The required AC input signal for this mode of operation is a negative pulse with a minimum pulse width of 0.6 microsecond.

The second mode of operation is the step mode, which is defined as the condition where the level control switches negative when the AC input signal is negative. This mode requires that the AC input signal remain negative for a minimum of 1.4 microsecond after the level control switches negative. Figures 3-24.4 and 3-24.5 illustrate the waveforms associated with both modes of operation.

SPECIFICATIONS

Input Loading

DC inputs: 1 unit load each
AC inputs: 2 unit loads each
Level controls: 1/2 unit load each

Circuit Delay

0.25 μsec (max): Carry propagation delay as binary counter
0.15 μsec (typ): Carry propagation delay as binary counter

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Current Requirements

-18 V 74 ma
-6 V 36 ma (reverse current into supply)
+12 V 3 ma

Total Power

1.3 watts

Polarization

Pins 30 and 32

Frequency of Operation

DC to 1 MC (max)

Output Drive Capability

6 unit loads and 400 pf stray capacitance each

Handle Color Code

Long: Blue
Short: Yellow

Table 3-24.1. UF-30 Connections for Use as Complementing Stages

AC Input Used	Connect		AC Input Loading
	Circuit A	Circuit B	
Common AC input	Pin 30 to 26 Pin 31 to 35	Pin 11 to 15 Pin 10 to 6	2 unit loads
AC set and reset inputs tied together	Pin 25 to 26 Pin 21 to 35	Pin 16 to 15 Pin 20 to 6	4 unit loads

Table 3-24.2. UF-30 Connections for Use as Shift Stages

AC Input Used	Connect		AC Input Loading
	Circuit A	Circuit B	
Common AC input	Pin 30 to reset output of previous stage Pin 31 to set output of previous stage	Pin 11 to reset output of previous stage Pin 10 to set output of previous stage	2 unit loads
AC set and reset inputs tied together	Pin 25 to reset output of previous stage Pin 21 to set output of previous stage	Pin 16 to reset output of previous stage Pin 20 to set output of previous stage	4 unit loads

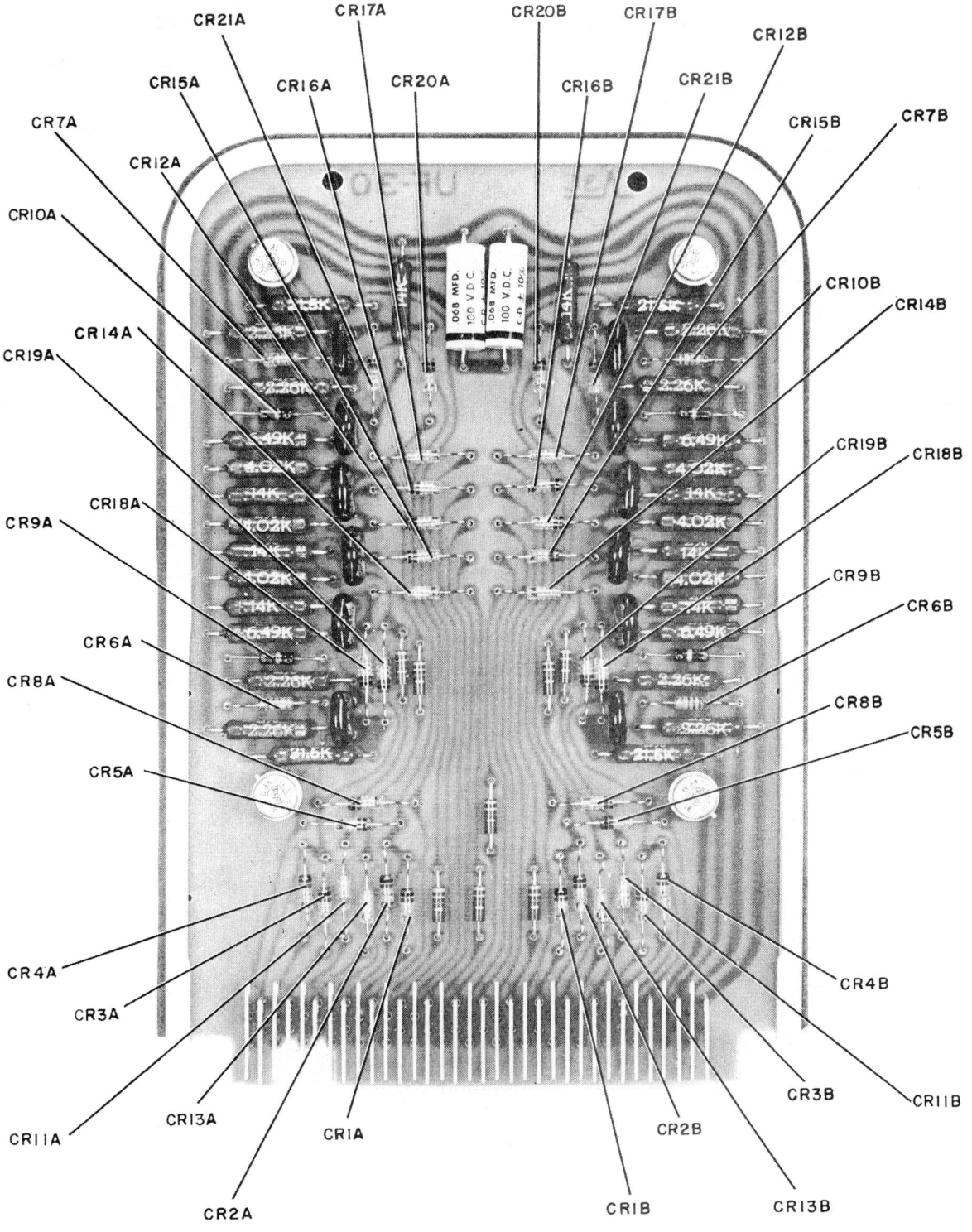


Figure 3-24.1. Universal Flip-Flop PAC, Model UF-30, Parts Location (Diodes)

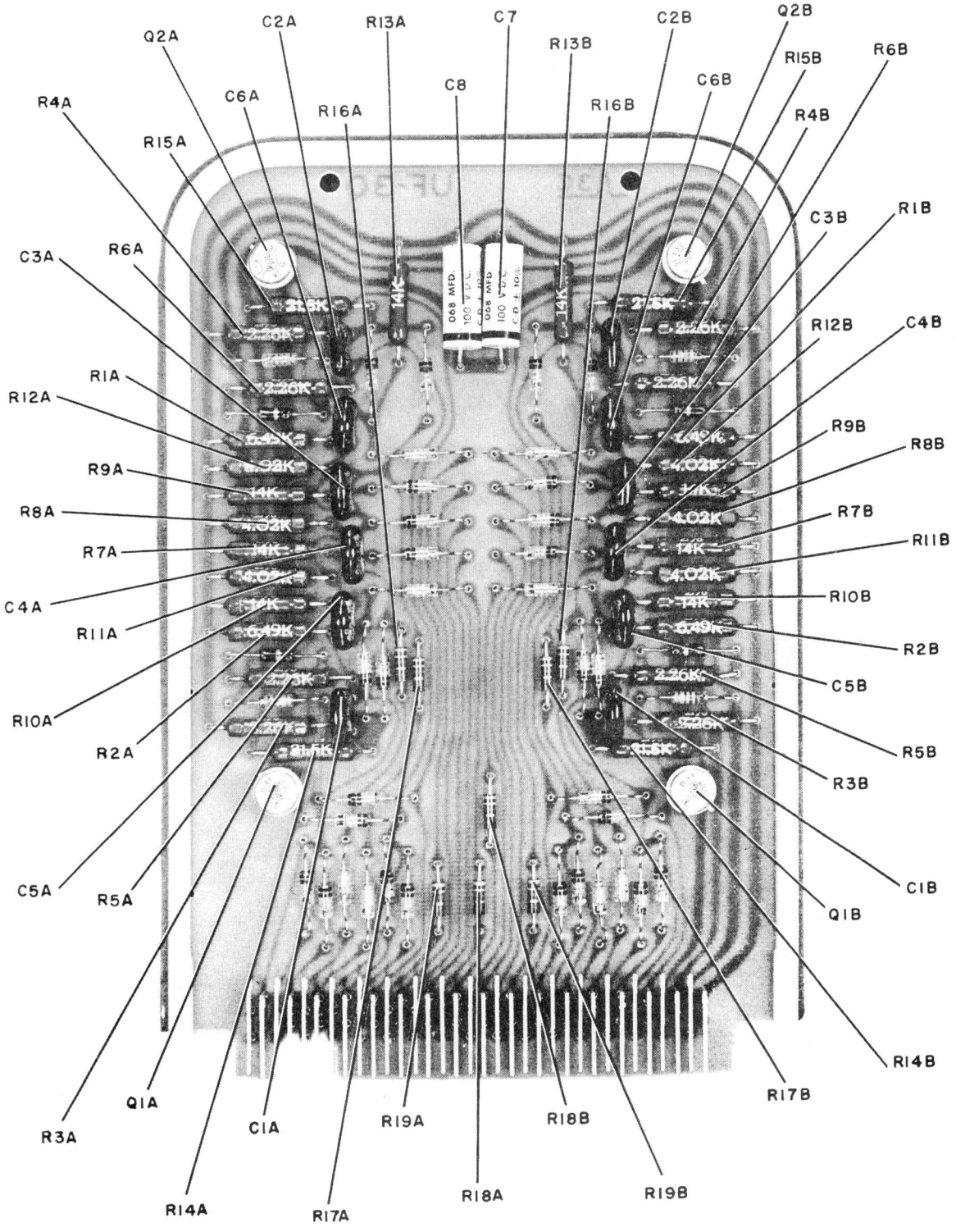


Figure 3-24.2. Universal Flip-Flop PAC, Model UF-30, Parts Location (Capacitors, Resistors, and Transistors)

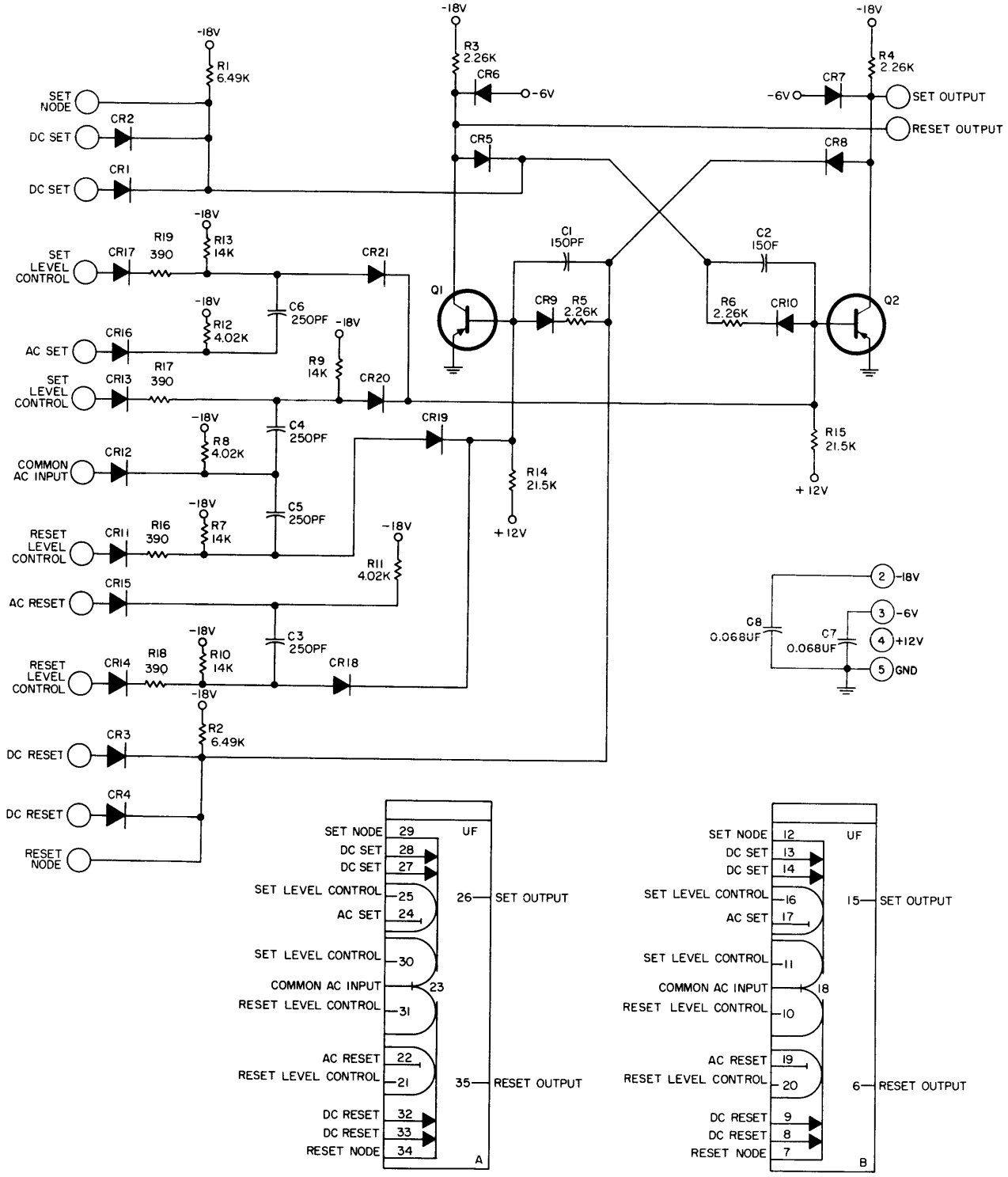


Figure 3-24.3. Universal Flip-Flop PAC, Model UF-30, Schematic and Logic Diagram

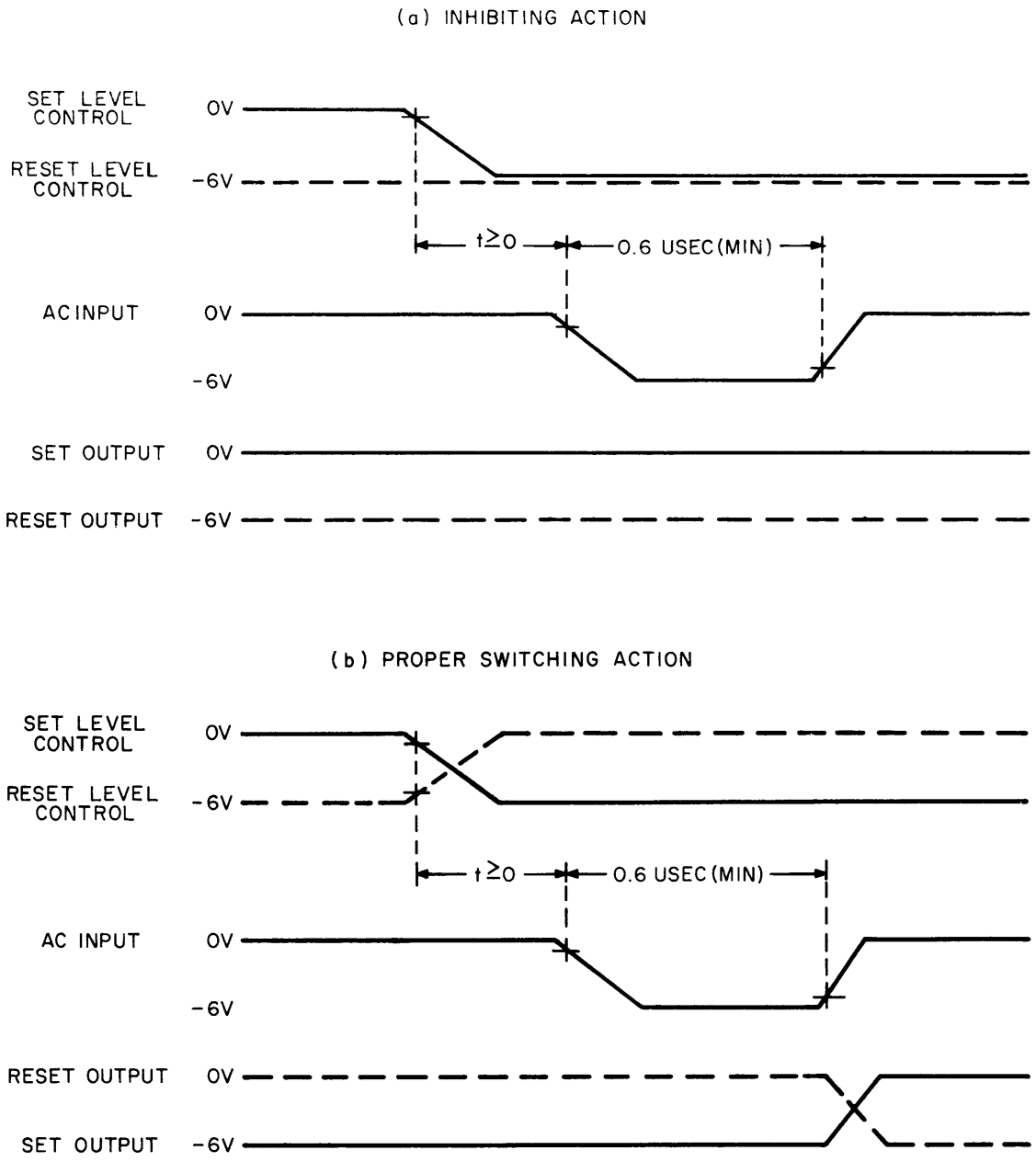
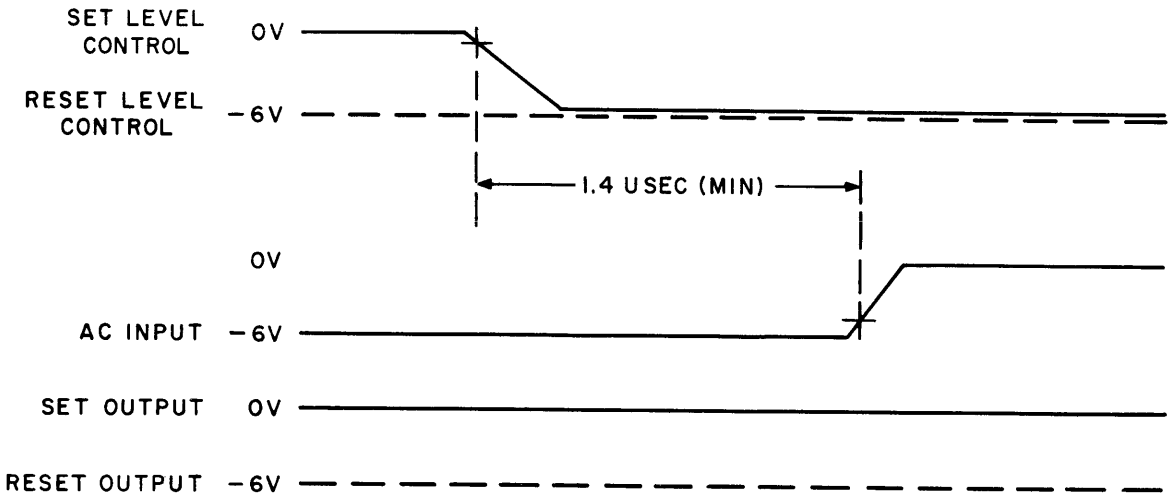


Figure 3-24.4. Pulse Mode Timing

(a) INHIBITING ACTION



(b) PROPER SWITCHING ACTION

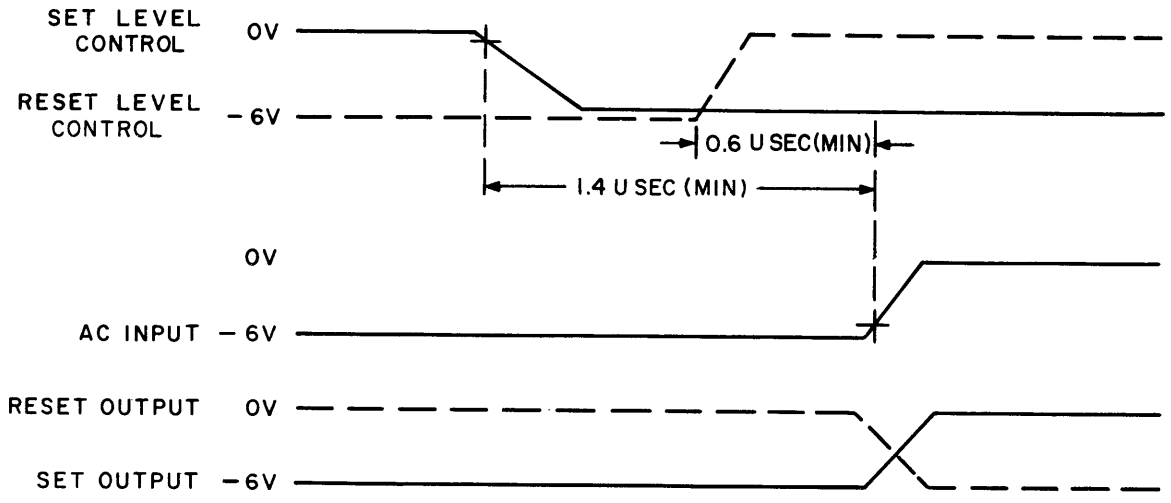


Figure 3-24.5. Step Mode Timing

3-25 TRANSMISSION LINE DRIVER PAC, MODEL XD-30

GENERAL DESCRIPTION

The Transmission Line Driver PAC, Model XD-30 (Figures 3-25.1 and 3-25.2), contains six circuits which drive standard 50-ohm, 75-ohm, and 93-ohm coaxial cables, and twisted-pair cables up to 1-MC repetition rates. The transmission line termination should be a high impedance. A standard S-PAC gate is recommended.

The design principle requires minimum DC currents from the PAC, only unit load current on the line, halved transient currents (60 ma max), no terminating resistor at the receiving end, and a 6-volt signal at the end of the line. Since the line is lightly loaded, only small currents are incident on the receiver thereby simplifying the grounding techniques at the receiver. The PAC output is short circuit protected.

CIRCUIT FUNCTION

Each driver, which performs a NAND function, consists of a two-diode input gate followed by a transistor inverter (Figure 3-25.3). A second transistor in a "totem pole" arrangement provides a fast transition from ground to -6 volts. Two series resistors and standoff terminals for a shunt resistor are provided with each circuit to match most transmission line impedances (Table 3-25.1). Each output has an adjacent pin (ground) to be used as a signal return from the transmission line.

The principle of operation of the XD-30 is to match the transmission line characteristic impedance at the driver end and open-circuit the receiving end. A 3-volt signal is sent down the line which results in a 6-volt signal at the receiving end due to the +1 reflection coefficient. The reflected 3-volt signal travels back to the driver and is completely absorbed in the termination of the driver with no multiple reflections. (Refer to Figures 3-25.4 and 3-25.5.)

Table 3-25.1. Transmission Line Impedance Match

Line Z_o	Connections Between Standoffs on PAC
93 ohms (and twisted pair*)	None
75 ohms	33 ohms, 5%, 1/2 W
50 ohms	Jumper

*See Applications

APPLICATIONS

Since one XD-30 PAC can introduce 0.36 amp transients with 80 ns transition times into the ground and -6-volt supply, all PACs should be as close as possible to the system power supply to minimize intercoupling through ground or power connections.

For best operation, the transmission line should be connected directly to the PAC at its connector and run continuously to the receiver (a DI-30 or equivalent). Whenever a different cable is used to couple the driver to the main transmission line, reflections are inherent. However, if the line impedance mismatch is minimal, signal degradation may be tolerable. In general, open wire lines should never be used for coupling, and a twisted pair should not be used to couple the driver to a 50-ohm coaxial cable. Usually a twisted pair coupling the driver to another twisted pair will be satisfactory.

The general limitations upon the length of the transmission line to be driven are the rise time, attenuation, and crosstalk peculiar to the cable. Actual experimental results show that 100 ft of standard coaxial cables (50-ohm, 75-ohm, 93-ohm), a 100-ft cable of 24 twisted pairs (#24 wire, PVC covered), and a 10-ft length of twisted-pair cable joined to 100 ft of 93-ohm coaxial cable can easily be driven at up to 1-MC repetition rates.

Twisted-pair cables are heterogeneous, and some experimental manipulation may be necessary to determine the optimum total series resistance on the PAC. For many twisted-pair cables, no modifications will be required. The recommended procedure to find the optimum series resistance is to monitor the signal at the PAC output and trim the series resistance until the initial transitions (not to be confused with the reflections) from -6 volts or 0 volt are 2.7 to 3.0 volts in amplitude. Alternatively, the resistors may be trimmed to yield the optimum signal at the end of the line.

Generally, twisted-pair cables with an increasing number of pairs require correspondingly less total series resistance on the PAC. Unfortunately, each individual pair in larger cables may require substantially different optimum total series resistance. Experimenting on a cable containing 24 pairs, the individual optimum total series resistance varied between 50 and 70 ohms.

The termination of twisted-pair cable should normally be a single S-PAC gate. However, more than one gate may be driven which results in DC attenuation, and a lower impedance termination which is detrimental. Low impedance cables can more easily drive more than one gate, but in all cases other gates being connected to the end of a single transmission line should be adjacent with short connecting wires.

If desired, lines may be terminated (at the receiving end) with a resistor equal to the Z_o of the particular transmission line. The result is a 3-volt signal at the output, but the line will be then terminated at both ends by the characteristic impedance (with no reflections). A special 3-volt-sensitive line receiver, such as the DI-31 S-PAC, is now necessary in this application. (Refer to Figure 3-25.6.)

The PAC may be used to achieve almost any output signal, between ground and -6 V, by selecting various terminating resistors at the receiving end. If the line is properly terminated on the PAC by R_0 (equal to the line impedance Z_o) and by R_1 at the receiver, then the output signal is:

$$e_o = \frac{R_1}{R_0 + R_1} (-6\ V)$$

The maximum DC current from any circuit is 60 ma (refer to Figure 3-25.7).

SPECIFICATIONS

Input Loading

2.0 Unit loads

Circuit Delay

60 ns (typ)

100 ns (max)

Frequency of Operation

DC to 1 MC

Output Waveform Characteristics*

Rise time: 80 ns (typ)

Fall time: 140 ns (typ)

Output Drive Capability

50-ohm, 75-ohm, 93-ohm coaxial cables and twisted-pair cables

Current Requirements

-18 V:	72 ma
- 6 V:	360 ma transient 30 ma (reverse) DC**
+12 V:	6 ma

Power

1.3 watt

Color Code

Long: Orange

Short: Blue

Recommended Cable Termination

50-ohm cable: two gates

73-ohm, 93-ohm and twisted pairs: one gate

Polarization

Pins 30 and 32

*Measured before series resistor.

**If the receiving end is terminated, a total of 360 ma (forward current) will be required.

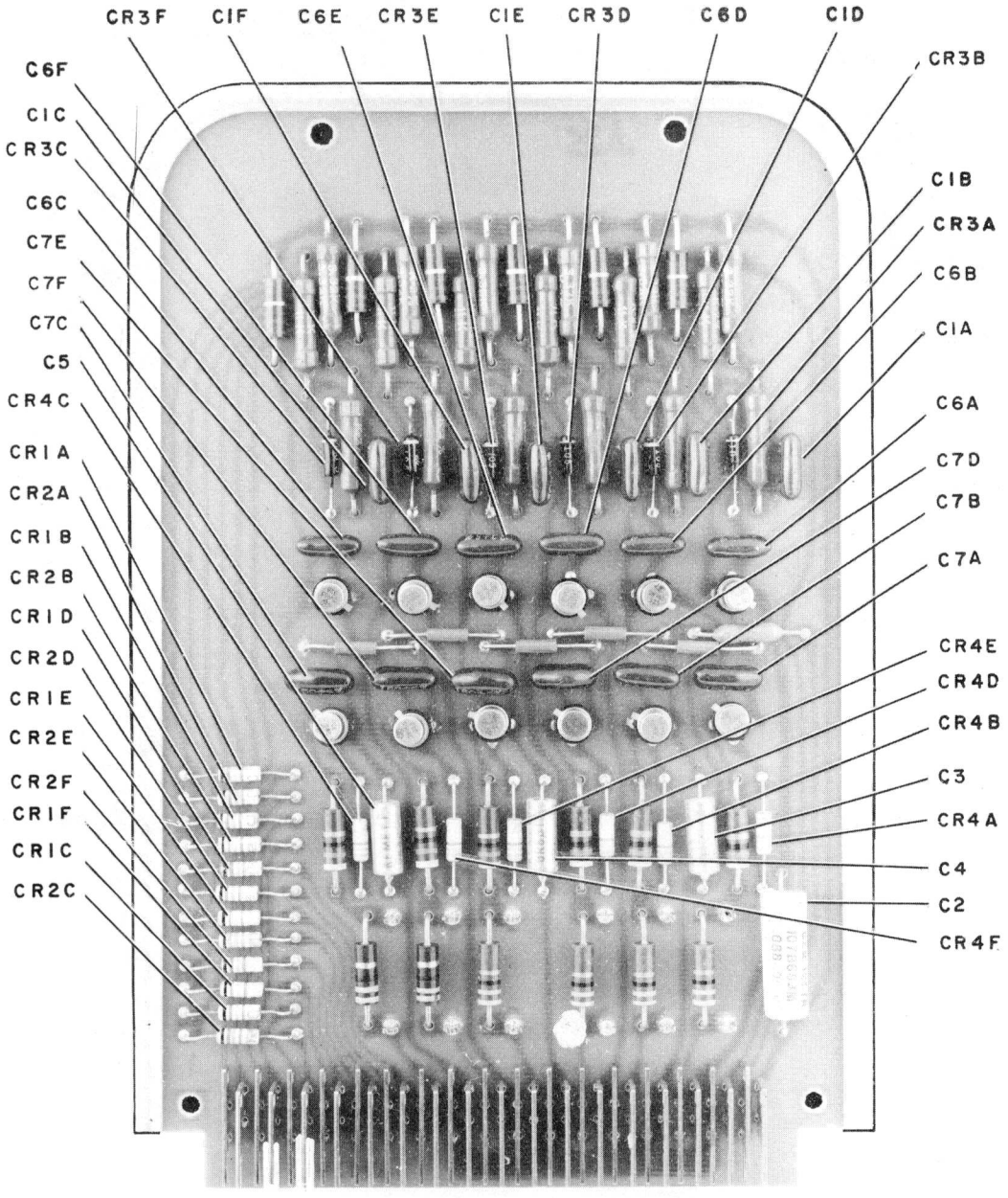


Figure 3-25.1. Transmission Line Driver PAC, Model XD-30, Parts Location (Capacitors and Diodes)

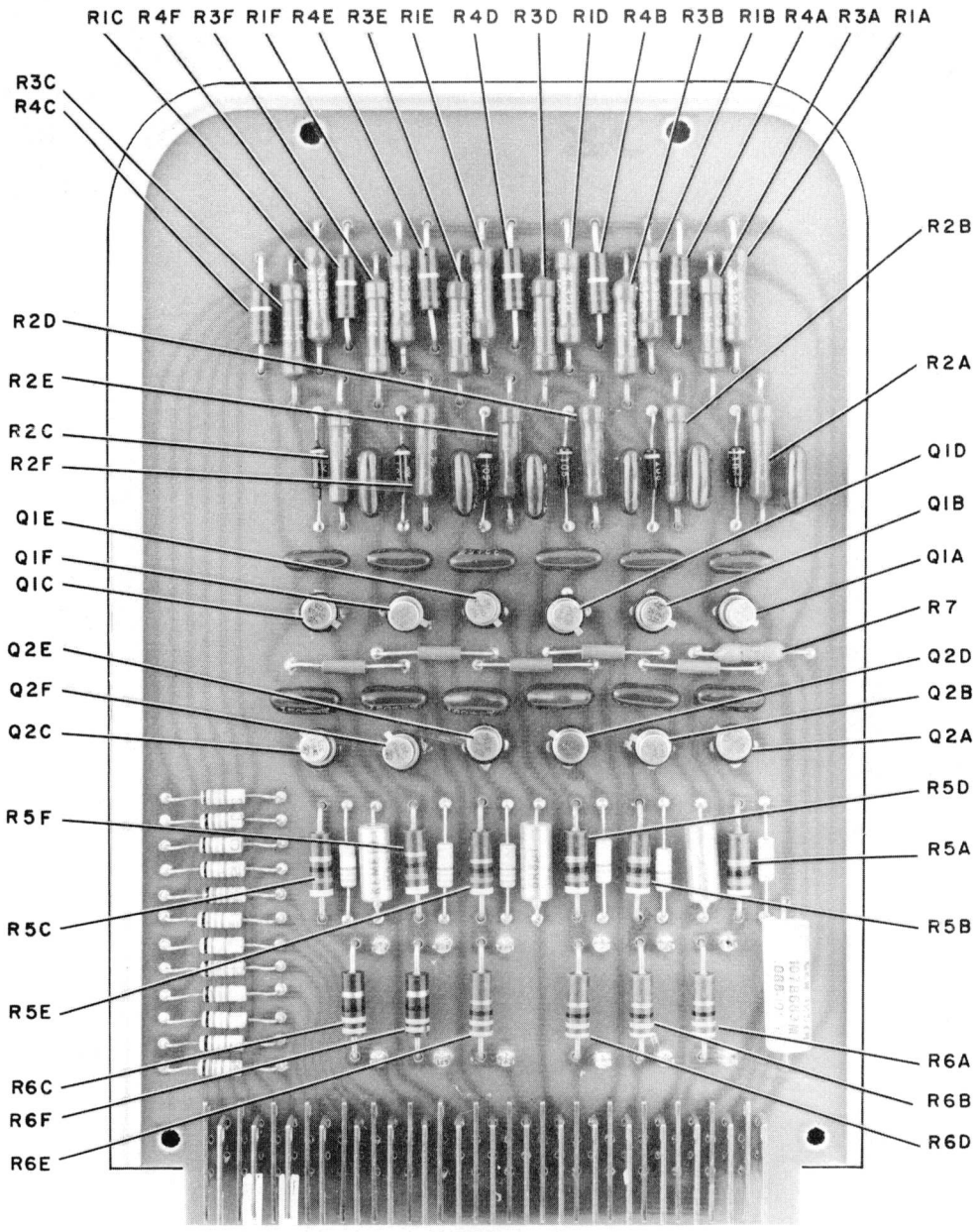


Figure 3-25.2. Transmission Line Driver PAC, Model XD-30, Parts Location (Resistors and Transistors)

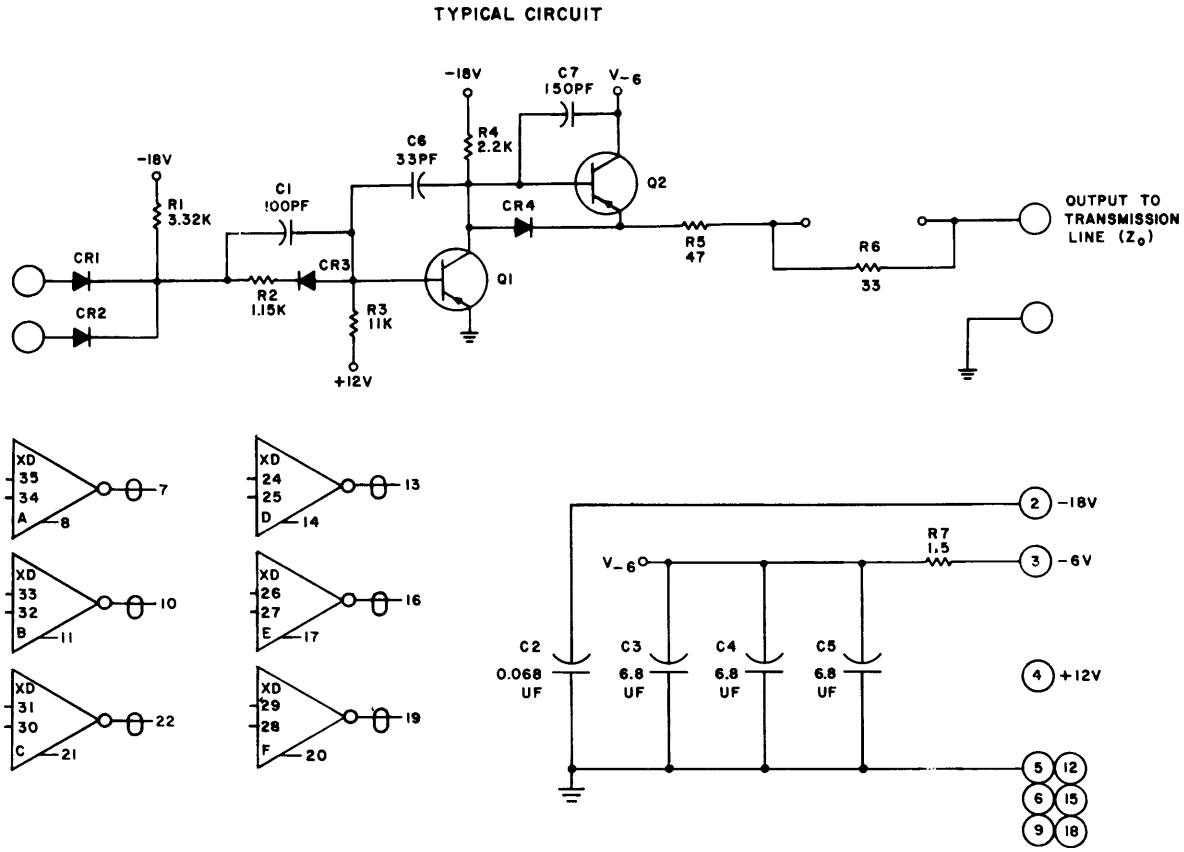


Figure 3-25.3. Transmission Line Driver PAC, Model XD-30, Schematic and Logic Diagram

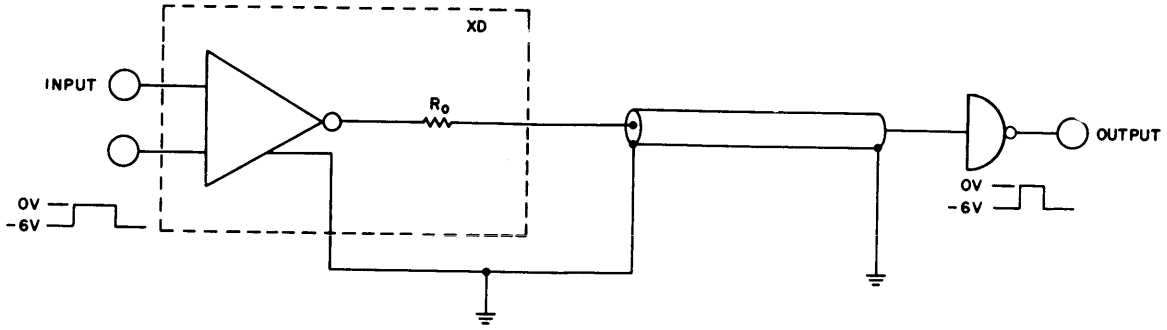


Figure 3-25.4. XD-30 PAC Signal Transmission

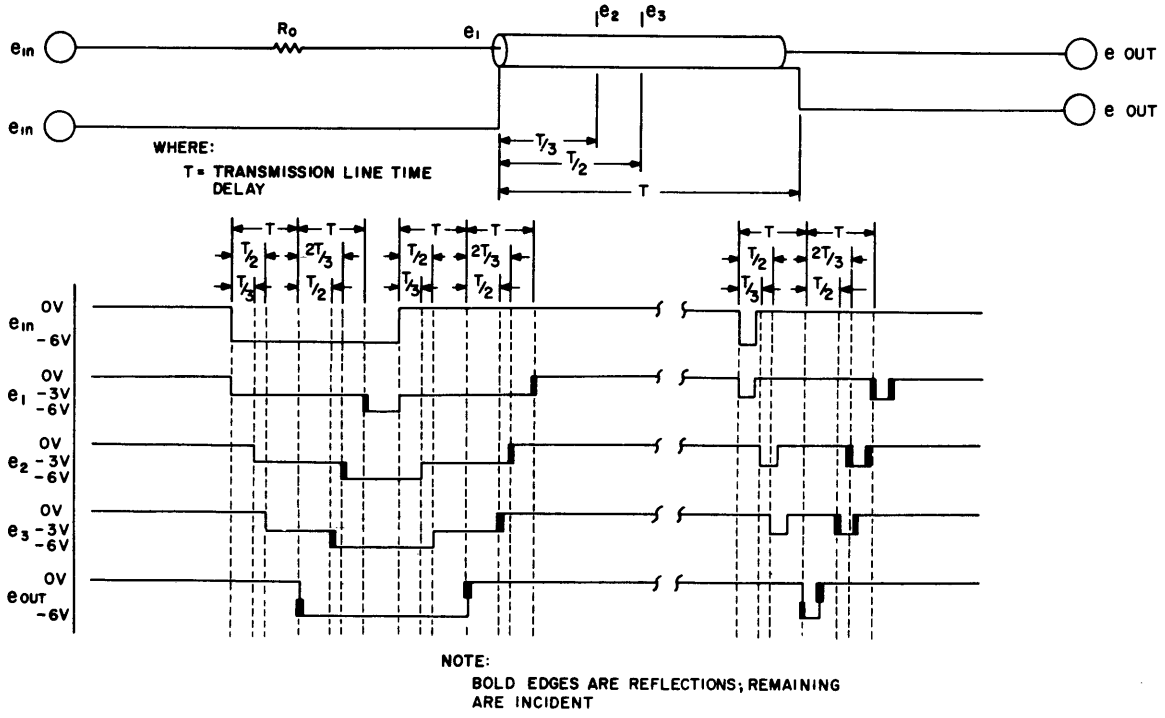


Figure 3-25.5. Transmission Line Waveform Characteristics

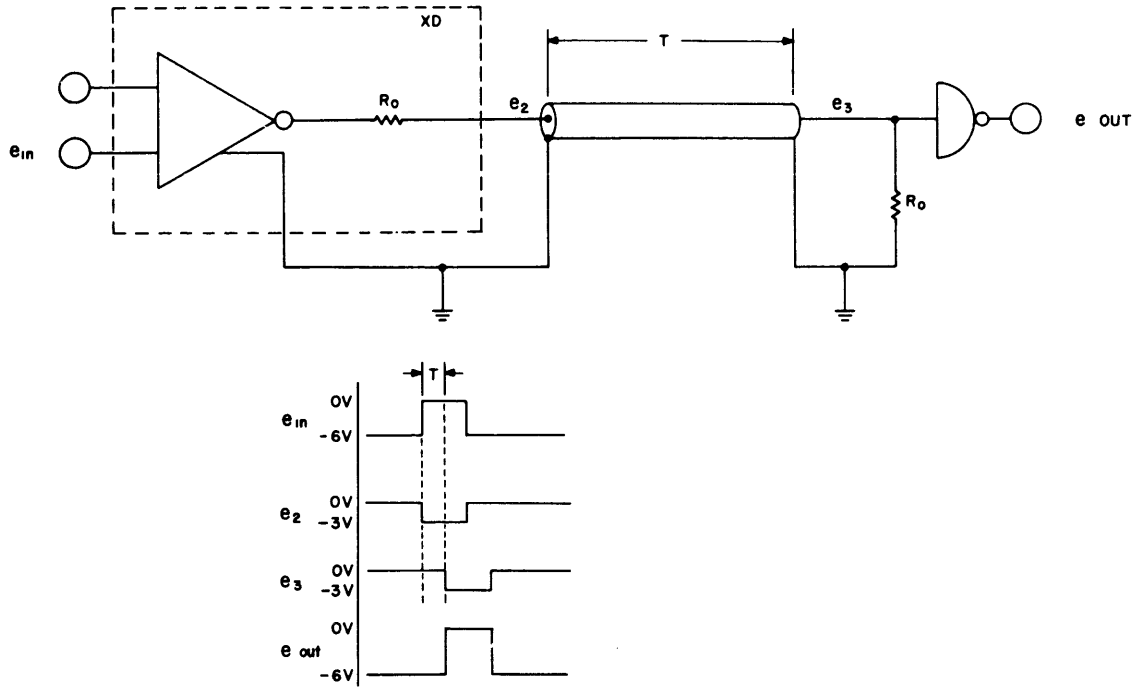


Figure 3-25.6. Line Terminated with Matched Impedance

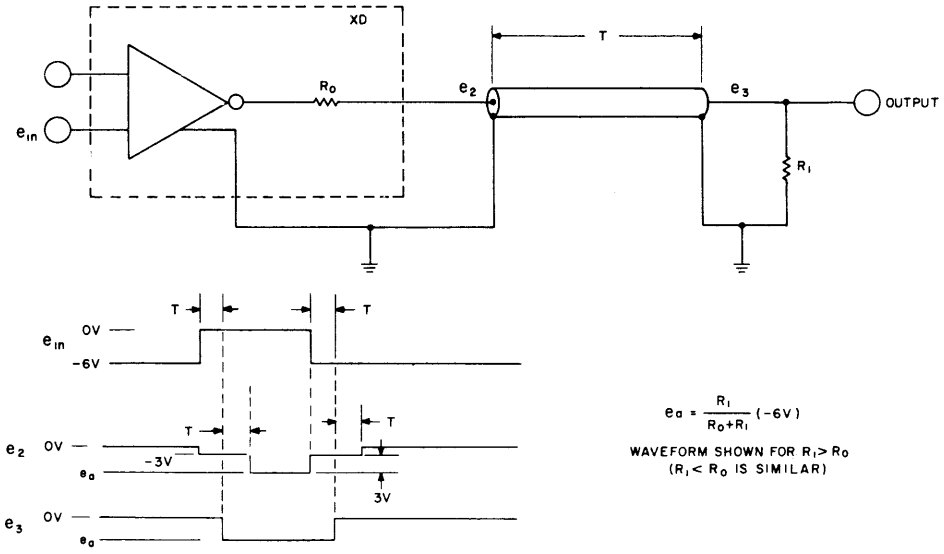


Figure 3-25.7. Selection of Output Terminating Resistors

SECTION IV
PARTS LISTS FOR 1-MC S-PACS

The parts lists below are applicable to the S-PACs in Section III.

COUNTER PAC, MODEL BC-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C3-C5	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15	930 011 137
C6, C7	CAPACITOR, FIXED, MICA DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR6, CR9-CR17	DIODE: Replacement Type 1N276	943 023 001
CR7, CR8	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R2	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/4 W	932 102 240
R3, R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R5, R6	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R7, R12	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/4 W	932 102 230
R8, R9, R13	RESISTOR, FIXED, FILM: 14 K ±2%, 1/4 W	932 102 308
R10, R11	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317

DIODE PAC, MODEL DC-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR3, CR5-CR23	DIODE: Replacement Type 1N276	943 023 001
CR4	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR; Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R2, R3	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R4	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

PARALLEL GATE PAC, MODEL DF-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1, CR2, CR4-CR11	DIODE: Replacement Type 1N276	943 023 001
CR3	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2% 1/2 W	932 103 240
R2, R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R3	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

NAND PAC, MODEL DI-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR3	DIODE: Replacement Type 1N276	943 023 001
CR4	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R2, R3	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R4	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

PARALLEL NAND PAC, MODEL DJ-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1, CR2, CR4	DIODE: Replacement Type 1N276	943 023 001
CR3	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/4 W	932 102 240
R2	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R3	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317
R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218

NAND PAC, MODEL DL-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC	930 301 015
CR1-CR3, CR5	DIODE: Replacement Type 1N276	943 023 001
CR4	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R2, R3	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R4	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

DELAY MULTIVIBRATOR/PULSE SHAPER PAC, MODEL DM-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 315
C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 3300 pf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 305
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 1500 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 257
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 330 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 140
C6	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 150
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 113
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 91 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 126
C9, C10	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type WMF	930 301 015
C11, C12	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.01 µf, 75 VDC; Glenco Type K-6000	930 156 301
CR1-CR6, CR8-CR11	DIODE: Replacement Type 1N276	943 023 001
CR7, CR13, CR14	DIODE: Replacement Type 1N816	943 105 001
CR12	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R8	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R2, R5	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R3	RESISTOR, FIXED, FILM: 14 K ±2%, 1/2 W	932 103 308
R4, R6, R7	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R9	RESISTOR, FIXED, FILM: 10 K ±2%, 1/4 W	932 102 301
R10	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

DELAY MULTIVIBRATOR/PULSE SHAPER PAC,
MODEL DM-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R11	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R12	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/2 W	932 004 046
R13	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310

ADJUSTABLE DELAY MULTIVIBRATOR PAC, MODEL DM-30A, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 315
C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 3300 pf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 305
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 1500 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 257
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 390 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 142
C6	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 150
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 113
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 91 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 126
C9, C10	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
C11, C12	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.01 µf GMV, 75 VDC; Glenco Type K-6000	930 156 301
CR1-CR6, CR8-CR11	DIODE: Replacement Type 1N276	943 023 001
CR7, CR13,CR14	DIODE: Replacement Type 1N816	943 105 001
CR12	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R2, R5, R6	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R3	RESISTOR, FIXED, FILM: 14.0 K ±2%, 1/2 W	932 103 308
R4, R7, R10	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R8	RESISTOR, FIXED, FILM: 10 K ±2%, 1/4 W	932 102 301
R9	RESISTOR, VARIABLE, COMPOSITION: 10 K ±20%, 1/4 W	933 003 007

ADJUSTABLE DELAY MULTIVIBRATOR PAC, MODEL DM-30A, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R11	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R12	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R13	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/2 W	932 004 046
R14	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310

GATE PAC, MODEL DN-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 µf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1, CR2, CR3,CR5-CR14	DIODE: Replacement Type 1N276	943 023 001
CR4	DIODE, SILICON: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R2, R3	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R4	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

DELAYED PULSE PAC, MODEL DS-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 330 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 140
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 150
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 91 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 126
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 1500 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 257
C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 3300 pf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 305
C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 315
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 113
C9	CAPACITOR, FIXED, MICA DIELECTRIC: 540 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 154
C10-C13	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.01 μf GMV, 75 VDC; Glenco Type K-6000	930 156 301
C14, C15	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR4, CR6-CR15	DIODE: Replacement Type 1N276	943 023 001
CR5, CR17-CR20	DIODE: Replacement Type 1N816	943 105 001
CR16	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1-Q3	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R4, R13	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R2	RESISTOR, FIXED, FILM: 14 K ±2%, 1/2 W	932 103 308
R3	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R5	RESISTOR, FIXED, FILM: 10 K ±2%, 1/4 W	932 102 301

DELAYED PULSE PAC, MODEL DS-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R6, R10	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R7, R8, R11	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R9	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R12	RESISTOR, FIXED, FILM: 1.4 K ±2%, 1/2 W	932 103 208
R14, R15	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R16	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/2 W	932 004 046
R17, R18	RESISTOR, FIXED, COMPOSITION: 1.1 K ±5%, 1/2 W	932 004 050

ADJUSTABLE DELAYED PULSE PAC, MODEL DS-30A, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 390 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 142
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 150
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 91 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 126
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 1500 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 257
C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 3300 pf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 305
C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±2%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 315
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 113
C9	CAPACITOR, FIXED, MICA DIELECTRIC: 540 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 154
C10, C11, C12, C13	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.01 μf GMV, 75 VDC; Glenco Type K-6000	930 156 301
C14, C15	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR4, CR6-CR15	DIODE, GERMANIUM: Replacement Type 1N276	943 023 001
CR5, CR17-CR20	DIODE: Replacement Type 1N816	943 105 001
CR16	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1-Q3	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R13	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R2	RESISTOR, FIXED, FILM: 14.0 K ±2%, 1/2 W	932 103 308
R3	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R5	RESISTOR, FIXED, FILM: 10 K ±2%, 1/4 W	932 102 301

ADJUSTABLE DELAYED PULSE PAC, MODEL DS-30A, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R6, R10, R11	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R4, R7, R8	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R9	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R12	RESISTOR, FIXED, FILM: 1.4 K ±2%, 1/2 W	932 103 208
R14, R15	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R16	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/2 W	932 004 046
R17, R18	RESISTOR, FIXED, COMPOSITION: 1.1 K ±5%, 1/2 W	932 004 050
R19	RESISTOR, VARIABLE, COMPOSITION: 10 K ±20%, 1/4 W	933 003 007

GATED FLIP-FLOP PAC, MODEL FA-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2, C3	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C4, C5	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C6, C7	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.01 μf GMV, 75 VDC; Glenco Type K-6000	930 156 301
CR1-CR11, CR13, CR14, CR16	DIODE: Replacement Type 1N276	943 023 001
CR12, CR15	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R8	RESISTOR, FIXED, COMPOSITION: 390 ohms ±5%, 1/4 W	932 007 039
R2, R5, R9	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/4 W	932 102 230
R3, R6, R10	RESISTOR, FIXED, FILM: 14 K ±2%, 1/4 W	932 102 308
R4, R7	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317
R11, R16	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R12, R14	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/4 W	932 102 240
R13, R15	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218

BASIC FLIP-FLOP PAC, MODEL FF-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C3, C4	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR7	DIODE: Replacement Type 1N276	943 023 001
CR8, CR9	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R2	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R3-R6	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R7, R8	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317

MASTER CLOCK PAC, MODEL MC-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C5	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C3, C15-C17	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
C4, C6, C11, C14	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 51 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 120
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 220 pf ±2%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 235
C9	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C10	CAPACITOR, FIXED, MICA DIELECTRIC: 1600 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 258
C12, C13	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-16	930 006 131
	FREQUENCY RANGE	
	100 KC to 249 KC	
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 1000 pf ±5%, 100 VDC; Elmenco Type DM-15 Cornell-Dubilier Type CD-15	930 011 153
C18	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell Dubilier Type CD-15	930 011 150
	250 KC to 499 KC	
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 146
C18	C APACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
	500 KC to 1 MC	
C2	CAPACITOR, FIXED, MICA. DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C18	CAPACITOR, FIXED, MICA DIELECTRIC: 50 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 119

MASTER CLOCK PAC, MODEL MC-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
CR1-CR8, CR10, CR12-CR16, CR19, CR20, CR23	DIODE: Replacement Type 1N276	943 023 001
CR9, CR17, CR18, CR20, CR22	DIODE: Replacement Type 1N816	943 105 001
CR11	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1-Q8	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R6	RESISTOR, FIXED, COMPOSITION: 100 K ±5%, 1/2 W	932 004 097
R2, R5	RESISTOR, FIXED, COMPOSITION: 2.2 K ±5%, 1/2 W	932 004 057
R3	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/2 W	932 004 038
R4	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/2 W	932 004 018
R7, R11, R23, R29	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R8	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R9, R19, R26	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2W	932 103 317
R10, R13, R16	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R12	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1 W	932 005 049
R14	RESISTOR, FIXED, FILM: 3.32 K ±2%, 1/2 W	932 103 226
R15	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R17, R24	RESISTOR, FIXED, FILM: 4.64 K ±2%, 1/2 W	932 103 233
R18, R25	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R20, R27	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310
R21	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/2 W	932 004 001
R22, R28	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1 W	932 005 018

MASTER CLOCK PAC, MODEL MC-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
Y1	CRYSTAL UNIT, QUARTZ	FREQ. DEP.
L1	COIL, RF: 5 mh; Replacement Type DELEVAN 2500-62	939 205 032

MASTER CLOCK PAC (SPECIAL PRECISION), MODEL MC-30X, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C5	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C3, C15-C17	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
C4, C6, C11, C14	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 51 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 120
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 220 pf ±2%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 235
C9	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 246
C10	CAPACITOR, FIXED, MICA DIELECTRIC: 1600 pf ±2%, 100 VDC; Elmenco Type DM-16	930 006 258
C12, C13	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-16	930 006 131
	FREQUENCY RANGE	
	100 KC to 249 KC	
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 1000 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 153
C18	CAPACITOR, FIXED, MICA DIELECTRIC: 750 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 150
	250 KC to 499 KC	
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 146
C18	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
	500 KC to 1 MC	
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C18	CAPACITOR, FIXED, MICA DIELECTRIC: 50 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 119

MASTER CLOCK PAC (SPECIAL PRECISION), MODEL MC-30X,
PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
CR1-CR8, CR10-CR16, CR19, CR21, CR23	DIODE: Replacement Type 1N276	943 023 001
CR9, CR17, CR18, CR20, CR22	DIODE: Replacement Type 1N816	943 105 001
CR11	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1-Q8	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R6	RESISTOR, FIXED, COMPOSITION: 100 K ±5%, 1/2 W	932 004 097
R2, R5	RESISTOR, FIXED, COMPOSITION: 2.2 K ±5%, 1/2 W	932 004 057
R3	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/2 W	932 004 038
R4	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/2 W	932 004 018
R7, R11, R23, R29	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R8	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R9, R19, R26	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R10, R13, R16	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R12	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1 W	932 005 049
R14	RESISTOR, FIXED, FILM: 3.32 K ±2%, 1/2 W	932 103 226
R15	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R17, R24	RESISTOR, FIXED, FILM: 4.64 K ±2%, 1/2 W	932 103 233
R18, R25	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R20, R27	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310
R21	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/2 W	932 004 001
R22, R28	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1 W	932 005 018
Y1	CRYSTAL UNIT, QUARTZ	FREQ. DEP.

MASTER CLOCK PAC (SPECIAL PRECISION), MODEL MC-30X,
PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
L1	COIL, RF: 5 mh; Replacement Type DELEVAN 2500-62	939 205 032

MULTI-PURPOSE FLIP-FLOP PAC, MODEL MF-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC	930 011 131
C3, C4	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC	930 011 137
C5, C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC	930 301 015
CR1-CR9 CR12-CR14	DIODE: Replacement Type 1N276	943 023 001
CR10, CR11	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R2, R3	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R5, R6	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R7, R9	RESISTOR, FIXED, COMPOSITION: 390 ohms ±5%, 1/4 W	932 007 039
R8	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R10, R11	RESISTOR, FIXED, FILM: 14 K ±2%, 1/4 W	932 102 308
R12, R13	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317

MULTIVIBRATOR CLOCK PAC, MODEL MV-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15	930 011 137
C2, C7	CAPACITOR, FIXED, MICA DIELECTRIC: 330 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 140
C3, C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.0022 μf ±10%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 104
C4, C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.015 μf ±10%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 110
C5, C10	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.12 μf ±10%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 118
C6, C11	CAPACITOR, FIXED, METALIZED PAPER: 1.0 μf ±10%, 100 VDC; Electron Products Type W 150	930 400 001
C12, C20	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C13	CAPACITOR, FIXED, MICA DIELECTRIC: 51 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 120
C14	CAPACITOR, FIXED, MICA DIELECTRIC: 180 pf ±2%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 233
C15	CAPACITOR, FIXED, MICA DIELECTRIC: 510 pf ±2%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 246
C16	CAPACITOR, FIXED, MICA DIELECTRIC: 1600 pf ±5%, 100 VDC; Elmenco Type DM-16	930 006 158
C17, C18, C19	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-16	930 006 131
C22, C23	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 pf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type CD-15	930 301 015
CR1-CR19, CR21, CR23-CR28, CR32, CR33	DIODE: Replacement Type 1N276	943 023 001
CR20, CR29, CR30, CR31, CR34	DIODE: Replacement Type 1N816	943 105 001
CR22	DIODE, ZENER: Replacement Type 1N705	943 102 002
Q1-Q10	TRANSISTOR: Replacement Type 2N1301	943 535 002

MULTIVIBRATOR CLOCK PAC, MODEL MV-30,
PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R1	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/2 W	932 004 042
R2, R11	RESISTOR, FIXED, COMPOSITION: 910 ohms ±5%, 1 W	932 005 048
R3, R10	RESISTOR, FIXED, FILM: 1.87 K ±2%, 1/2 W	932 103 214
R4, R9, R19	RESISTOR, FIXED, COMPOSITION: 200 K ±5%, 1/2 W	932 004 104
R5, R8	RESISTOR, FIXED, COMPOSITION: 24 K ±5%, 1/2 W	932 004 082
R6	RESISTOR, VARIABLE, COMPOSITION: 15 K ±20%, 1/4 W	933 103 208
R7	RESISTOR, FIXED, FILM: 1.4 K ±2%, 1/2 W	932 103 208
R12, R14, R17, R20, R35	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R13, R23, R27	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R15, R26, R32	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R16	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1 W	932 005 049
R18	RESISTOR, FIXED, FILM: 3.32 K ±2%, 1/2 W	932 103 226
R21, R30	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R22, R31	RESISTOR, FIXED, FILM: 4.64 K ±2%, 1/2 W	932 103 233
R24, R28	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310
R25	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1 W	932 005 018
R29	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1 W	932 005 025

OCTAL/DECIMAL DECODER PAC, MODEL OD-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR6, CR8	DIODE: Replacement Type 1N276	943 023 001
CR7	DIODE: Replacement Type 1N816	943 105 001
Q1	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/4 W	932 102 240
R2	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R3	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317
R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R5-R13	RESISTOR, FIXED, COMPOSITION: 33 K ±5%, 1/2 W	932 004 085

POWER AMPLIFIER PAC, MODEL PA-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C2, C3	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	932 011 137
C4, C5	CAPACITOR, FIXED, ELECTROLYTIC: 3.3 μf ±20%, 35 VDC; Sprague Type 150D	930 217 018
CR1, CR4-CR9	DIODE: Replacement Type 1N276	943 023 001
CR2, CR3	DIODE: Replacement Type 1N816	943 105 001
Q1-Q3	TRANSISTOR: Replacement Type 2N1301	943 535 002
Q4	TRANSISTOR: Replacement Type 2N404A	943 519 003
R1	RESISTOR, FIXED, FILM: 1.87 K ±2%, 1/2 W	932 103 214
R2	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R3	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R4, R5	RESISTOR, FIXED, FILM: 1.62 K ±2%, 1/2 W	932 103 211
R6, R7	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/2 W	932 103 310
R8	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R9	RESISTOR, FIXED, COMPOSITION: 33 ohms ±5%, 1/2 W	932 004 013

NON-INVERTING POWER AMPLIFIER PAC, MODEL PN-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC	930 011 131
C2, C3	CAPACITOR, FIXED, MICA DIELECTRIC: 390 pf ±5%, 100 VDC	930 011 142
C4, C5	CAPACITOR, FIXED, ELECTROLYTIC TANTALUM: 3.3 μf ±20%, 35 VDC	930 217 018
CR1, CR2, CR7	DIODE: Replacement Type 1N276	943 023 001
CR3, CR4	DIODE: Replacement Type 1N816	943 105 001
CR5, CR6	DIODE: Replacement Type Clevite CGD-956	943 024 002
Q1-Q3	TRANSISTOR: Replacement Type 2N1301	943 535 002
Q4	TRANSISTOR: Replacement Type 2N404A	943 519 003
R1	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R2	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R3	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317
R3, R7	RESISTOR, FIXED, FILM: 1.33 K ±2%, 1/2 W	932 103 207
R5	RESISTOR, FIXED, FILM: 590 ohms ±2%, 1/2 W	932 103 138
R6	RESISTOR, FIXED, FILM: 11 K ±2%, 1/4 W	932 102 303
R8	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/2 W	932 004 001

SERIAL MEMORY PAC, MODEL SM-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.1 μf ±20%, 200 VDC; Potter Company Z3064	930 304 001
C3, C6	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-16	932 006 131
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 180 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 133
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 110 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 128
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 100 pf ±5%, 100 VDC; Elmenco Type DM-16	930 006 127
C8, C11, C12, C15, C17, C18, C22, C24	CAPACITOR, FIXED, ELECTROLYTIC, TANTALUM: 0.1 μf ±20%, 35 VDC; Sprague 150D	930 217 009
C9	CAPACITOR, FIXED, MICA DIELECTRIC: 68 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 123
C10, C16, C21	CAPACITOR, FIXED, METALIZED PAPER: 0.047 μf ±10%, 100 VDC; Electron W-150	930 400 002
C13, C19	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 2200 pf ±10%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 104
C14, C20	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.01 μf ±10%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 109
C23	CAPACITOR, FIXED, MICA DIELECTRIC: 50 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 119
C25	CAPACITOR, FIXED, MICA DIELECTRIC: 130 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 130
C26, C27	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
CR1-CR18, CR20-CR23, CR25-CR27, CR29, CR34, CR35, CR38-CR46, CR49, CR50,	DIODE: Replacement Type 1N276	943 023 001
CR19, CR24, CR28, CR30-CR33, CR36, CR37, CR47, CR48	DIODE: Replacement Type 1N816	943 105 001

SERIAL MEMORY PAC, MODEL SM-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
Q1-Q14	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1-R4, R11, R14, R52, R55	RESISTOR, FIXED, COMPOSITION: 6.8 K ±5%, 1/4 W	932 007 069
R5, R12, R53, R57	RESISTOR, FIXED, COMPOSITION: 2.4 K ±5%, 1/4 W	932 007 058
R6, R13, R16, R19, R54, R58	RESISTOR, FIXED, COMPOSITION: 22 K ±5%, 1/4 W	932 007 081
R7, R10, R15, R51, R56	RESISTOR, FIXED, COMPOSITION: 2.4 K ±5%, 1/2 W	932 004 058
R8, R61	RESISTOR, FIXED, COMPOSITION: 3.9 K ±5%, 1/4 W	932 007 063
R9	RESISTOR, FIXED, COMPOSITION: 13 K ±5%, 1/4 W	932 007 076
R17	RESISTOR, FIXED, COMPOSITION: 1.6 K ±5%, 1/4 W	932 007 054
R18	RESISTOR, FIXED, COMPOSITION: 150 ohms ±5%, 1 W	932 005 029
R20, R27, R30, R37	RESISTOR, FIXED, FILM: 1.33 K ±2%, 1/8 W	932 105 207
R21, R32	RESISTOR, FIXED, FILM: 5.62 K ±2%, 1/8 W	932 105 237
R22, R31	RESISTOR, FIXED, FILM: 15.4 K ±2%, 1/8 W	932 105 310
R23, R35	RESISTOR, FIXED, FILM: 442 ohms ±2%, 1/8 W	932 105 132
R24, R36	RESISTOR, FIXED, FILM: 51.1 ohms ±2%, 1/8 W	932 105 035
R25	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/2 W	932 004 001
R26, R34	RESISTOR, FIXED, FILM: 825 ohms ±2%, 1/8 W	932 105 145
R28, R38	RESISTOR, FIXED, FILM: 3.01 K ±2%, 1/8 W	932 105 224
R29, R40	RESISTOR, FIXED, FILM: 215 ohms ±2%, 1/8 W	932 105 117
R33	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/4 W	932 007 001
R39, R62	RESISTOR, FIXED, FILM: 6.81 K ±2%, 1/8 W	932 105 241
R41	RESISTOR, FIXED, COMPOSITION: 2 K ±5%, 1/4 W	932 007 056
R42, R59	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4 W	932 007 025

SERIAL MEMORY PAC, MODEL SM-30, PARTS LIST (Cont)

Ref. Desig.	Description	3C Part No.
R43	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/4 W	932 007 018
R44, R60	RESISTOR, FIXED, COMPOSITION: 10 K ±5%, 1/4 W	932 007 073
R45	RESISTOR, FIXED, COMPOSITION: 1.8 K ±5%, 1/2 W	932 004 055
R46, R48	RESISTOR, FIXED, COMPOSITION: 2 K ±5%, 1/2 W	932 004 056
R47	RESISTOR, FIXED, COMPOSITION: 910 ohms ±5%, 1/2 W	932 004 048
R49	RESISTOR, FIXED, COMPOSITION: 7.5 K ±5%, 1/4 W	932 007 070
R50	RESISTOR, FIXED, COMPOSITION: 39 ohms ±5%, 1/4 W	932 007 015
L1, L2	COIL, RF: 22 μh ±10%: Replacement Type, Delevan 1537-44	939 204 023

SERIAL MEMORY PAC, MODEL SM-30L, PARTS LIST

Ref. Desig.	Description	3C Dwg. No.
C1, C2, C14, C17	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.1 μf ±20%, 200 VDC	930 304 001
C3, C6	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC	930 006 131
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 180 pf ±5%, 100 VDC	930 011 133
C5	CAPACITOR, FIXED, MICA DIELECTRIC: 110 pf ±5%, 100 VDC	930 011 128
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 220 pf ±5%, 100 VDC	930 006 235
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 68 pf ±5%, 100 VDC	930 011 123
C9	CAPACITOR, FIXED, METALIZED PAPER: 0.047 μf ±10%, 100 VDC	930 400 002
C10, C11, C15, C16	CAPACITOR, FIXED, ELECTROLYTIC, TANTALUM: 3.3 μf ±20%, 35 VDC	930 217 018
C12, C18	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.01 μf ±10%, 200 VDC	930 301 109
C13, C19, C21	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 0.1 μf ±20%, 25 VDC	930 171 007
C20	CAPACITOR, FIXED, MICA DIELECTRIC: 50 pf ±5%, 100 VDC	930 011 119
C22	CAPACITOR, FIXED, MICA DIELECTRIC: 130 pf ±5%, 100 VDC	930 011 130
C23, C24	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC	930 011 131
CR1-CR18, CR20-CR23, CR25-CR27, CR29-CR30, CR34-CR42, CR45, CR46	DIODE: Replacement Type 1N695	943 023 001
CR19, CR24, CR28, CR32, CR33, CR43, CR44	DIODE: Replacement Type 1N276	943 105 001
R1-R4, R11, R14, R51, R54	RESISTOR, FIXED, COMPOSITION: 6.8 K ±5%, 1/4 W	932 007 069
R5, R12, R52, R56	RESISTOR, FIXED, COMPOSITION: 2.4 K ±5%, 1/4 W	932 007 058
R6, R13, R16, R19, R53, R57	RESISTOR, FIXED, COMPOSITION: 22 K ±5%, 1/4 W	932 007 081
R7, R10, R15, R50, R55	RESISTOR, FIXED, COMPOSITION: 2.4 K ±5%, 1/2 W	932 004 058

SERIAL MEMORY PAC, MODEL SM-30L, PARTS LIST (Cont)

Ref. Desig.	Description	3C Dwg. No.
R8, R60	RESISTOR, FIXED, COMPOSITION: 3.9 K ±5%, 1/4 W	932 007 063
R9	RESISTOR, FIXED, COMPOSITION: 13 K ±5%, 1/4 W	932 007 076
R17	RESISTOR, FIXED, COMPOSITION: 1.6 K ±5%, 1/4 W	932 007 054
R18	RESISTOR, FIXED, COMPOSITION: 1.5 K ±5%, 1/4 W	932 007 053
R20, R30	RESISTOR, FIXED, FILM: 3.65 K ±2%, 1/8 W	932 105 228
R21, R28, R32, R37	RESISTOR, FIXED, FILM: 5.62 ±2%, 1/8 W	932 105 237
R23, R35	RESISTOR, FIXED, FILM: 681 ohms ±2%, 1/8 W	932 105 141
R24, R38	RESISTOR, FIXED, FILM: 6.81 K ±2%, 1/8 W	932 105 241
R25	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/2 W	932 004 001
R26, R34	RESISTOR, FIXED, FILM: 1.54 K ±2%, 1/8 W	932 105 210
R27, R36, R40	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/8 W	932 105 230
R29, R39	RESISTOR, FIXED, FILM: 316 ohms ±2%, 1/8 W	932 105 125
R33	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1/4 W	932 007 001
R41, R58	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4 W	932 007 025
R42	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/4 W	932 007 018
R43, R59	RESISTOR, FIXED, COMPOSITION: 10 K ±5%, 1/4 W	932 007 073
R44	RESISTOR, FIXED, COMPOSITION: 1.8 K ±5%, 1/2 W	932 004 055
R45, R47	RESISTOR, FIXED, COMPOSITION: 2 K ±5%, 1/2 W	932 004 056
R46	RESISTOR, FIXED, COMPOSITION: 910 ohms ±5%, 1/2 W	932 004 048
R48	RESISTOR, FIXED, COMPOSITION: 7.5 K ±5%, 1/4 W	932 007 070
R49	RESISTOR, FIXED, COMPOSITION: 39 ohms ±5%, 1/4 W	932 007 015
Q1-Q3, Q9-Q14	TRANSISTOR: Replacement Type 2N1301	943 535 002

SERIAL MEMORY PAC, MODEL SM-30L, PARTS LIST (Cont)

Ref. Desig.	Description	3C Dwg. No.
Q4	TRANSISTOR: Replacement Type 2N1065	943 513 001
Q5-Q8	TRANSISTOR: Replacement Type 2N965	943 543 014
L1, L2	COIL: 43 μh ±5%: Replacement Type Delevan 1537-38	939 204 030

SHIFT REGISTER PAC, MODEL SR-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C3, C4	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C5, C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR7, CR10-CR14	DIODE: Replacement Type 1N276	943 023 001
CR8, CR9	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R2	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/4 W	932 102 240
R3, R4	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R5, R6	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/4 W	932 102 218
R7	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/4 W	932 102 230
R8, R9	RESISTOR, FIXED, FILM: 14 K ±2%, 1/4 W	932 102 308
R10, R11	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/4 W	932 102 317
R12, R13	RESISTOR, FIXED, COMPOSITION: 390 ohms ±5%, 1/4 W	932 007 039

UNIVERSAL FLIP-FLOP, MODEL UF-30, PARTS LIST

Ref. Desig.	Description	3C Part No.
C1, C2	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 131
C3-C6	CAPACITOR, FIXED, MICA DIELECTRIC: 250 pf ±5%, 100 VDC; Elmenco Type DM-15; Cornell-Dubilier Type CD-15	930 011 137
C7, C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf ±20%, 100 VDC; Pyramid Type 107; Cornell-Dubilier Type WMF	930 301 015
CR1-CR8, CR11-CR21	DIODE: Replacement Type 1N276	943 023 001
CR9, CR10	DIODE: Replacement Type 1N816	943 105 001
Q1, Q2	TRANSISTOR: Replacement Type 2N1301	943 535 002
R1, R2	RESISTOR, FIXED, FILM: 6.49 K ±2%, 1/2 W	932 103 240
R3-R6	RESISTOR, FIXED, FILM: 2.26 K ±2%, 1/2 W	932 103 218
R7, R9, R10, R13	RESISTOR, FIXED, FILM: 14 K ±2%, 1/2 W	932 103 308
R8, R11, R12	RESISTOR, FIXED, FILM: 4.02 K ±2%, 1/2 W	932 103 230
R14, R15	RESISTOR, FIXED, FILM: 21.5 K ±2%, 1/2 W	932 103 317
R16-R19	RESISTOR, FIXED, COMPOSITION: 390 ohms ±5%, 1/4 W	932 007 039

TRANSMISSION LINE DRIVER, MODEL XD-30 PARTS LIST

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, MICA DIELECTRIC: 100 pf, ±5%, 100 VDC	930 011 127
C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.068 μf, ±20%, 100 VDC	930 301 015
C3-C5	CAPACITOR, FIXED, ELECTROLYTIC TANTALUM: 6.8 μf, ±20%, 35 VDC	930 217 020
C6	CAPACITOR, FIXED, MICA DIELECTRIC: 33 pf, ±5%, 100 VDC	930 011 114
C7	CAPACITOR, FIXED, MICA DIELECTRIC: 150 pf, ±5%, 100 VDC	930 011 131
CR1, CR2	DIODE: Replacement Type 1N276	943 023 001
CR3	DIODE: Replacement Type 1N816	943 105 001
CR4	DIODE: Replacement Type CGD-935	943 024 001
Q1	TRANSISTOR: Replacement Type 2N965	943 543 004
Q2	TRANSISTOR: Replacement Type 2N3250	943 724 001
R1	RESISTOR, FIXED, FILM: 3.32 K ±2%, 1/2 W	932 103 226
R2	RESISTOR, FIXED, FILM: 1.15 K ±2%, 1/2 W	932 103 204
R3	RESISTOR, FIXED, FILM: 11 K ±2%, 1/2 W	932 103 303
R4	RESISTOR, FIXED, COMPOSITION: 2.2 K ±5%, 1/2 W	932 004 057
R5	RESISTOR, FIXED, COMPOSITION: 47 ohms ±5%, 1/2 W	932 004 017
R6	RESISTOR, FIXED, COMPOSITION: 33 ohms ±5%, 1/2 W	932 004 013
R7	RESISTOR, FIXED, WIREWOUND: 1.5 ohms ±10%, 1 W	932 208 003