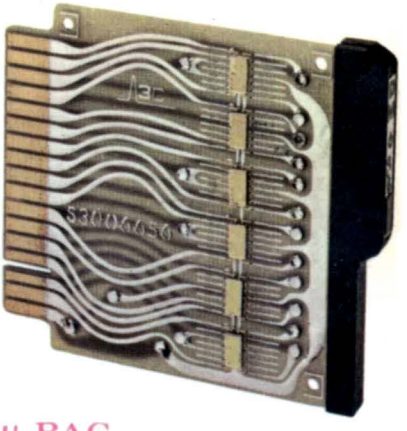

μ-PAC
integrated
circuit modules
Instruction Manual

HONEYWELL
INC.
COMPUTER CONTROL DIVISION

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M-135

Instruction Manual

μ-PAC INTEGRATED CIRCUIT MODULES

September 23, 1966

Honeywell

COMPUTER CONTROL DIVISION

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PREFACE

MANUAL REVISION

To ensure continued usefulness of this manual, each revised page of technical material (text, schematic, photo assembly, and parts list) is identified with the date of revision. A revision bar is also provided to facilitate the location of the change. Undated pages are unchanged pages of the original issue (8/1/65).

COMPONENT REPLACEMENT

Some components supplied in the equipment have slightly different specifications than more readily available commercial equivalents. All parts manufactured by or specifically for Computer Control should be ordered directly from Computer Control. These parts are assigned a 3C 9-digit part number only. In cases where the supplied components are interchangeable, the type numbers of the commercial equivalents are listed in the parts list.

SECTION I
INTRODUCTION

1-1 SCOPE

This instruction manual provides complete descriptive and reference material for the μ-PAC digital modules and auxiliary equipment of Computer Control. The manual is divided into three sections. Section I contains a general description of the equipment, capabilities and design of the module line. Section II contains the product line specification and detailed descriptions of the basic logic circuits. Section III contains specific information on each μ-PAC product, including specifications and applications data.

1-2 μ-PAC PRODUCT LINE

μ-PAC is a complete product line of logic modules (PACs), mounting assemblies (BLOCs), power supplies, and other supporting equipment that together provide a complete capability for the design and fabrication of computers and data processing systems. A list of the products appears in Tables 1-1 and 1-2.

While incorporating the reliability and economic advantages of integrated circuits, the μ-PAC product line retains the versatile logic flexibility of S-PAC, a product line of Computer Control that has received wide customer acceptance.

The μ-PACs are compact, functionally efficient modules using standard types of integrated circuits interconnected on an etched board. This approach simplifies design and allows more logic to be included on each PAC. Some special-purpose PACs of moderate or low usage are hybrid in construction, being composed of integrated circuits and discrete components. All PACs use static logic, and in general have an operating frequency range between dc and 5 mc.

Table 1-1.
Product Line Summary (Modules)

Functional Type and Color Code	Model No.	PAC Type	Contents
PACs with Independent Gates (Red)	DC-335	Multi-Input NAND	Four 3-input diode clusters; Two 6-input NAND gates with nodes
	DI-335	NAND type 1	Eight 2-input NAND gates; Two 2-input NAND gates with separate load circuits
	DL-335	NAND type 2	Four 4-input NAND gates; Two 4-input NAND gates with separate load circuits

Table 1-1. (Cont)
Product Line Summary (Modules)

Functional Type and Color Code	Model No.	PAC Type	Contents
PACs with Independent Gates (Cont) (Red)	DN-335	Expandable NAND	Four 3-input NAND gates with nodes; Two 3-input NAND gates with nodes and separate load circuits
PACs with Independent Flip-Flops (Blue)	BC-335	Counter	Six flip-flops for binary counting or complementing operations
	BR-335	Buffer register	Six flip-flops with prewired common clock and common reset
	FA-335	Gated flip-flop	Four flip-flops with independent dc, clock and control inputs. A prewired common reset is also provided
	FF-335	Basic flip-flop	Eight flip-flops with dc input gating
	FF-335	Basic flip-flop	Eight flip-flops with dc input gating
	SR-335	Shift register	Eight to 16-bit shift register
	UF-335	Universal flip-flop	Three flip-flops with multiple clocked and dc inputs
Functional Gating PACs (Purple)	DG-335	Selection gate type 1	Four selection gate structures each having three 2-input selection gates
	DG-336	Selection gate type 2	Two selection gate structures. One has four 3-input gates; the other has four 4-input selection gates
	EO-335	Exclusive OR	Five exclusive OR gate structures and a single-input NAND circuit
	OD-335	Octal/Decimal decoder	One prewired binary-to-octal decoder plus two independent NAND gates for expanding the matrix for BCD-to-decimal conversion
	TG-335	Transfer gate	Four transfer gate structures each having a common input
Functional Flip-Flop PACs (Blue)	BC-336	Binary counter	Eight to 20 flip-flops prewired for binary counting
	BC-337	Fast carry counter	Eight flip-flops for BCD or binary counting
Power Amplifier PACs (Green)	PA-335	Power amplifier	Six 3-input inverting amplifiers
	PN-335	Non-inverting power amplifier	Six 3-input non-inverting power amplifiers
Delay Multivibrator PAC (Yellow)	DM-335	Delay multivibrator	Two monostable multivibrators with step-adjustable pulse widths

Table 1-1. (Cont)
Product Line Summary (Modules)

Functional Type and Color Code	Model No.	PAC Type	Contents
Delay Multivibrator PAC (Yellow) (Cont)	DM-336	Adjustable delay multivibrator	Two monostable multivibrators with continuously adjustable pulse width
Clock PACs (Yellow)	MC-335	Master clock	One crystal-controlled clock with variable pulse shaper output
	MV-335	Multivibrator clock	One free-running multivibrator with adjustable frequency and pulse widths and also synchronous start/stop capability
Input/Output PACs (Orange)	DD-330	Display driver	BCD-to-decimal converter, 10 lamp-driver circuits
	LC-335	Negative logic level converter	Ten converter circuits
	LD-330	Lamp driver	Twelve lamp driver circuits
	LD-331	High-drive lamp driver	Eight lamp driver circuits
	LD-335	Negative logic level driver	Eight converter circuits
	SD-330	Solenoid driver	Three 2-input solenoid driver circuits plus an additional gate
	ST-335	Schmitt trigger	Two Schmitt trigger circuits
	ST-336	Adjustable Schmitt trigger	Two Schmitt trigger circuits with adjustable threshold and sensitivity
	XD-335	Transmission line driver	Six 2-input transmission line drivers
	XD-336	Transmission line driver	Six 2-input transmission line drivers
Special Purpose PACs (Black)	AS-330	Copper clad PAC kit	Unetched card with separate handle
	BP-330	Blank PAC	Blank PAC with etched power lines
	TP-330	Test Point PAC	For access to μ-BLOC connector pins from μ-PAC side
	XP-330	Extender PAC	Used for access to μ-PAC in operation

Table 1-2.
Product Line Summary (Auxiliary Equipment)

General Type	Model No.	Description		
Power Supplies	PB-330	Regulated supply rated for 2.5 amp at +6v and 0.25 amp at -6v		
	PB-331	Regulated supply rated for 10 amp at +6v and 1 amp at -6v		
	RP-330	Regulated supply rated for 25 amp at +6v and 2.5 amp at -6v		
BLOCs		Connector Type	μ-PAC Capacity	Provisions for Power Supply
	BL-330	Solderless wrap	96	PB-331
	BL-331	Taper pin	48	PB-331
	BL-332	Solderless wrap	144	None
	BL-333	Taper pin	72	None
	BM-330	Solderless wrap	24	PB-330
	BM-335	Taper pin	24	PB-330
	BM-337	Taper pin	36	None
Indicators	UI-110	Transistorized unit indicator		
	UI-330	Transistorized unit indicator		
Mounting panels	PM-330	Mounting panel for use with BM-335 and BM-337 BLOCs		
	PM-331	Mounting panel for use with BM-330 μ-BLOC		
Jumper lead set	JT-330	Assorted taper pin jumper leads		

1-3 MICROCIRCUITS

The monolithic integrated circuits are packaged in standard 14-lead 1/8 in. by 1/4 in. flat packs. (See Figure 1-1.) Up to 22 flat packs can be soldered to the etched wiring of a single μ-PAC card for high-density logic. Resistance soldering methods enable simple replacement of components. Production techniques proven by major integrated circuit manufacturers and Computer Control Company's own facility guarantee quality control and environmental stability consistent with military standards. At present the μ-PAC line employs four standard microcircuit types:

a. F-01, dual NAND gate, two 3-input gates with input nodes
b. F-02, quad NAND gate, four 2-input gates
c. F-03, power amplifier, two 3-input power gates
d. F-04, flip-flop, one J-K flip-flop

Detailed microcircuit descriptions appear in Section II.

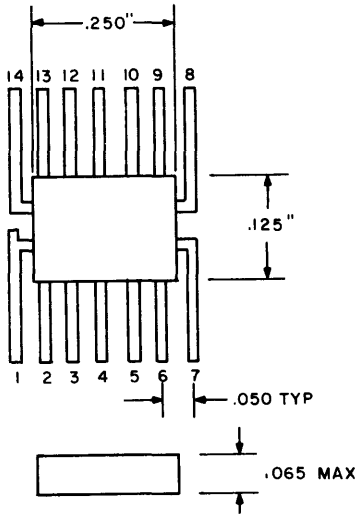


Figure 1-1. Dimensions of Standard Microcircuit

1-4 μ-PAC MODULES

The μ-PAC modules contain integrated circuit assemblies and some discrete hybrid combinations mounted on glass-impregnated epoxy cards with 1-ounce copper-clad printed circuits. Dimensions are shown in Figure 1-2. The PAC type is clearly indicated on the molded nylon handle by model number. Color coding on the handle indicates functional type (see Table 1-1). All PACs feature gold-plated etched fingers to guarantee reliable electrical contact with a 34-pin polarized connector.

1-5 AUXILIARY EQUIPMENT

1-5.1 μBLOCs

Several types of μ-BLOCs are available for μ-PAC installation flexibility. All models use the same basic structure, but differ in dimensions, number of μ-PAC connectors, power supply provisions, and the use of taper-pin or solderless-wrap connectors.

The BL-series is directly mountable in standard 19-inch rack panels. BM-335 and BM-337 BLOCs can be adapted to mount in a 19-inch rack by using a mounting panel. If desired, this panel can then be used as a control panel. The BM-335 and BM-337 BLOCs can also be coupled for side-by-side mounting in a 19-inch rack.

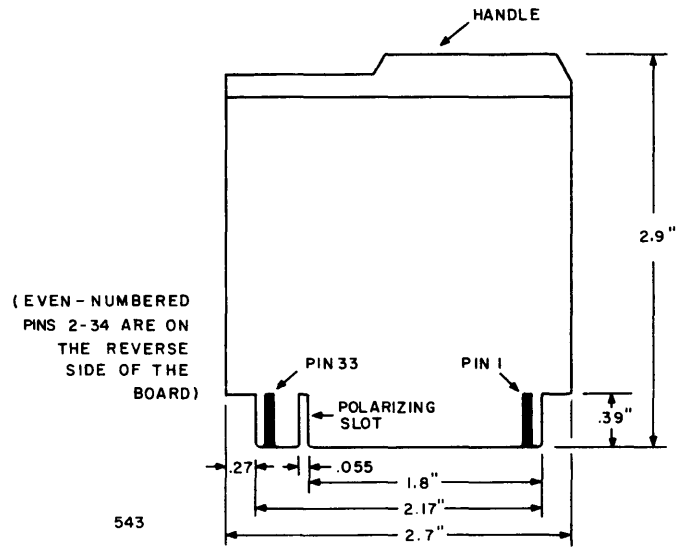


Figure 1-2. Dimensions of a Standard μ-PAC

Solderless-wrap or taper-pin connectors are mounted in BLOCs with ground and power prewired. The connector plane is easily removable for convenient wiring.

Mounting ears are detachable and allow front or back mounting of the connector plane.

Built-in cooling units are contained in each BLOC. When two BL-series BLOCs are used together, the fans can be utilized in a push-pull manner.

1-5.2 Power Supplies

Plug-in Power Supplies, Models PB-330 and PB-331, are integrally packaged units that can be mounted directly into BLOCs. PB-330 mounts in BM BLOCs; PB-331 mounts into BL BLOCs. They supply current at both μ-PAC voltage levels, +6v and -6v, and are designed to drive all modules contained in their respective BLOCs. By making the necessary internal connections, these supplies can accommodate input voltages of 115 or 220v ac at standard input frequencies of 50, 60 and 400 cps.

Front panels include the following features: on/off switch, power on indicator, three fuses, and voltage adjustment potentiometers.

1-5.3 Jumper Lead Set

Jumper Lead Set, Model JT-330, provides an assortment of taper-pin connectors in a variety of lead lengths and colors for system wiring of taper pin μ-BLOCs.

1-5.4 Logic Symbol Stickers

To aid in the use of μ-PACs, individual sheets of logic symbol stickers are available for all PAC types. The stickers are printed on precut sections of transparent mylar for direct application to a reproducible drawing base. The stickers simplify system logic design and generation of wire lists, and minimize drafting requirements for final engineering drawings. The logic symbol, pin numbers, and logic function are printed directly on each sticker. In addition, space is provided for designating the physical location of the PAC in the μ-BLOC.

1-5.5 Accessories

μ-PAC accessories include the Model XP-330 Extender PAC, automatic wire-wrap kits, wire-wrap and taper-pin wiring tools, and a module extractor.

1-6 PRODUCT LINE FEATURES

The integrated circuit designs were developed at Computer Control Company to meet the specific needs of a versatile 5-megacycle product line. Emphasis in design was on reliable systems operation and on efficient interconnection of logic functions. Types of logic circuits suitable for fabrication in monolithic form were investigated; certain types, including resistance-coupled transistors, transistor-coupled transistors, diode-coupled emitter followers, and transistor-coupled emitter followers, operated in very high speed systems but at a sacrifice in ease of logical or electrical interconnection. Their stability in a noisy system environment often proved to be marginal. These factors led to the selection of DTL, or diode gating followed by an inverting saturated transistor, as the basic μ-PAC gating element. DTL logic combines a high immunity to noise with an operating speed in excess of 5 mc. On critical inputs, such as clock inputs to the flip-flop, μ-PAC noise thresholds compare favorably with discrete component circuitry. Other inherent features of DTL, such as input gate expansion and output cascading, have been exploited in the design.

Several features not normally available in integrated circuit products have been included. Power amplifiers employ a technique for switching to an idling mode when the output is short-circuited. The unique flip-flop circuit has negligible set-up time, low dc input loading, low transient input loading, a short clock pulse-width requirement, J-K and R-S operation, dc control independent of clock input level, and a highly versatile input gating structure.

Design and specification of the equipment are conservative. For example, the flip-flop will toggle at rates greater than 10 mc under moderate loading conditions, but this capability is not logically useful except in limited applications. At the specified frequency limit of 5 mc, data can be transferred from one register to another through three gates (up to five or six logic functions) in one clock period. Additionally, all applicable circuitry has been laboratory-tested under full load over the temperature range at frequencies up to 8 mc.

SECTION II
PRODUCT LINE SPECIFICATIONS AND MICROCIRCUIT CHARACTERISTICS

2-1 INTRODUCTION

This section contains general specifications for the μ-PAC digital module line and detailed technical data on the four basic integrated circuit types used throughout the product line for digital logic functions. The detailed descriptions of each module type, in Section III of this manual, make reference to these general specifications.

2-2 GENERAL μ-PAC SPECIFICATIONS

All performance specifications listed below are guaranteed minimums based on worst-case tolerances. Actual performance will invariably exceed these guaranteed minimums. The following specifications apply to all μ-PAC types. Any exceptions are listed in the individual specifications.

2-2.1 Input Switching Thresholds (Refer to Figure 2-1.)

a. NAND gate and flip-flop dc inputs

ZERO level: +1.1v (min), +1.35v (typ)

ONE level: +3.0v (max), +1.55v (typ)

b. Power Amplifier and flip-flop clock and control inputs

ZERO level: +1.2v (min), +1.6v (typ)

ONE level: +3.0v (max), +1.8v (typ)

2-2.2 Output Logic Levels (Guaranteed for all circuit types)

Logic ONE: +4.0v (min) to +6.3v (max)

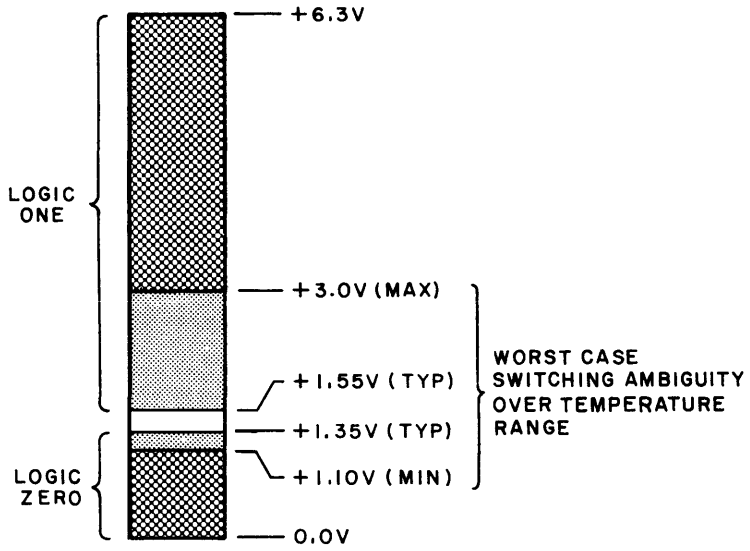
Logic ZERO: 0v to +0.35v (max)

When referring to the outputs of circuits, the terms "set" and "reset" denote level outputs and "assertion" and "negation" denote pulse outputs. Flip-flops produce level outputs; one-shots and clocks produce pulse outputs.

2-2.3 Frequency Range (DC to 5 MC)

One common way of describing the speed of a digital circuit is to state the highest frequency square or rectangular wave that can be applied to the input of a circuit and still reliably produce a specified output. Applied to a flip-flop, this method specifies the highest toggling or complementing rate possible; and for a gate, an input discrimination capability dependent on its circuit delay. Of course, these circuits would be driving light loads. Such

a. NAND GATE AND FLIP-FLOP DC INPUTS



b. POWER AMPLIFIER AND FLIP-FLOP CLOCK AND CONTROL INPUTS

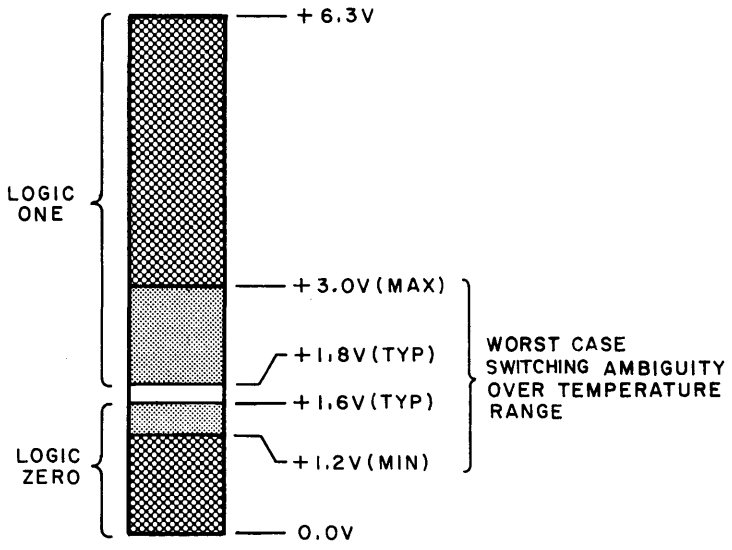


Figure 2-1. Switching Thresholds

an approach is often misleading and unusable for the systems designer. When many of the same types of circuits are used in a system, the system capability or operating frequency depends on accumulated circuit delays. There must also be a reasonable fanout from any logic circuit; otherwise extra circuits would be needed in parallel or series in order to drive a moderate amount of logic. Rise and fall times of individual circuits are primarily meaningful only to the extent that they affect circuit delay.

An alternate measure of the efficiency of a system is the number of stages or levels of logic through which a signal can pass during a clock period. Computer Control Company, Inc. has chosen to specify the μ-PAC digital circuit line from this standpoint of system operating frequency. The standard flip-flop can actually toggle at 10 mc, but is specified as having an operating frequency of 5 mc. The flip-flop requires only 40 nsec set up time before triggering. At a 5 mc clock rate, 160 nsec is available for going through logic, enough time for the initial clocked flip-flop delay plus three gate delays. All logic circuits in the chain have a fanout of eight at this frequency.

2-2.4 Temperature Range

Operating ambient (System): $0^{o}C$ to $+55^{o}C$
Storage: $-65^{o}C$ to $+150^{o}C$

2-2.5 Power Supplies

a. Positive voltage

Nominal:	+6.0v
Operating range:	+5.1v to +6.3v
Absolute maximum rating:	+8.0v

b. Negative voltage (used on hybrid modules only)

Nominal:	-6.0v
Operating range	-5.7v to -6.3v
Absolute maximum rating:	-8.0v

Absolute maximum voltage ratings cannot be exceeded without the risk of circuit damage.

2-2.6 Loading Rules

Loading specifications for μ-PACs are expressed in terms of "unit loads," both for input loading and output drive capability. The unit load concept simplifies calculation of total loading imposed on a driving stage that is fanned out to a number of different circuit types. For μ-PAC, a unit load is defined as the power required to drive the input circuit of a NAND gate (nominally 1.6 ma dc). Unit load ratings apply to the logic ZERO (ground) signal condition at a gate input. (Gates require no input power when all inputs are at logic ONE or are not connected.)

2-2.7 Current Requirements

Current requirements are listed in the specifications for each individual μ-PAC. The requirements are calculated on a nominal worst-case basis, in which the circuit inputs are assumed to be in the condition capable of causing the maximum current drain for a particular voltage. The nominal worst-case is selected instead of the extreme worst-case to provide a more realistic figure for power requirements and therefore permit more equipment to be driven by a power supply. Since it is very unlikely that all gates in a system would be on at the same time, the nominal worst-case calculations provide a considerable safety factor.

The current specifications include only the current used in the specific μ-PAC and do not include the current going to external loads. Since the input load current is included in the specification, total system current requirements can be calculated by adding the rated currents for all μ-PACs in the system.

2-2.8 Worst Case Delays

In the detailed μ-PAC descriptions of Section III, worst-case delays are specified over the full temperature range and under loading conditions which result in the longest propagation delay. (Eight dc gate loads are assumed for turn-on and one active dc gate load is assumed for turn-off.) For a gating circuit, the delay is specified as the average of the turn-on and turn-off delays. The total capacitance driven under the specified worst-case condition is 15 pf of wiring capacitance plus the capacitance accumulated in a μ-BLOC system when driving eight unit loads. This capacitance may be present during turn-off as well as turn-on, since it is possible to fan out to eight unit loads and yet have only one gate active. (The other seven loads may be inhibited by inputs at ground.) The effect of additional wiring capacitance on gate delays is discussed in Paragraph 2-2.9.

The preceding conditions apply to all gate and flip-flop circuits. Power amplifier delay specifications assume the condition of driving 25 active dc gate loads plus a total of 250 pf of capacitance.

2-2.9 Typical Delay Characteristics

The curves in Figure 2-2 show typical circuit delays of the basic NAND gate, plotted against variations in temperature, system wiring capacitance, and dc and capacitive loading conditions. For example, the "5 loads, 1 active" curve shows the delay characteristic of a gate output that fans out to five gates, four of which are inhibited by logic ZERO signals on other inputs. Connector, printed circuit, and input capacitance when fanning out to 5 unit loads are taken into consideration. The worst-case condition is also plotted. This is the "8 loads, 1 active" curve, where 1 active load is being driven from an output that fans out to 8 unit loads. In this situation, the maximum stray capacitance is being driven by the minimum charging current, resulting in longer turn-off delays.

Although the curves are plotted beyond 40 picofarads of additional wiring capacitance, that amount of wiring capacitance is unlikely to appear on any output in a μ-BLOC

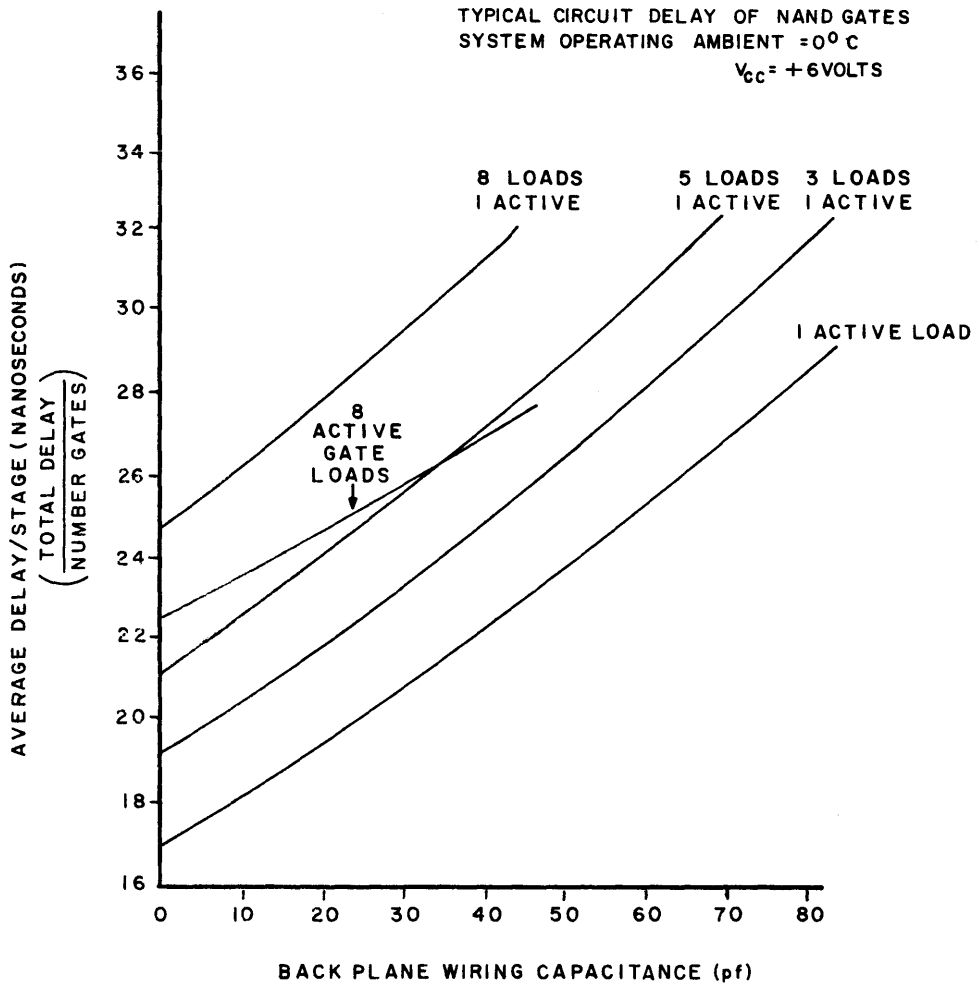


Figure 2-2. Typical NAND Gate Circuit Delays (Sheet 1 of 3)

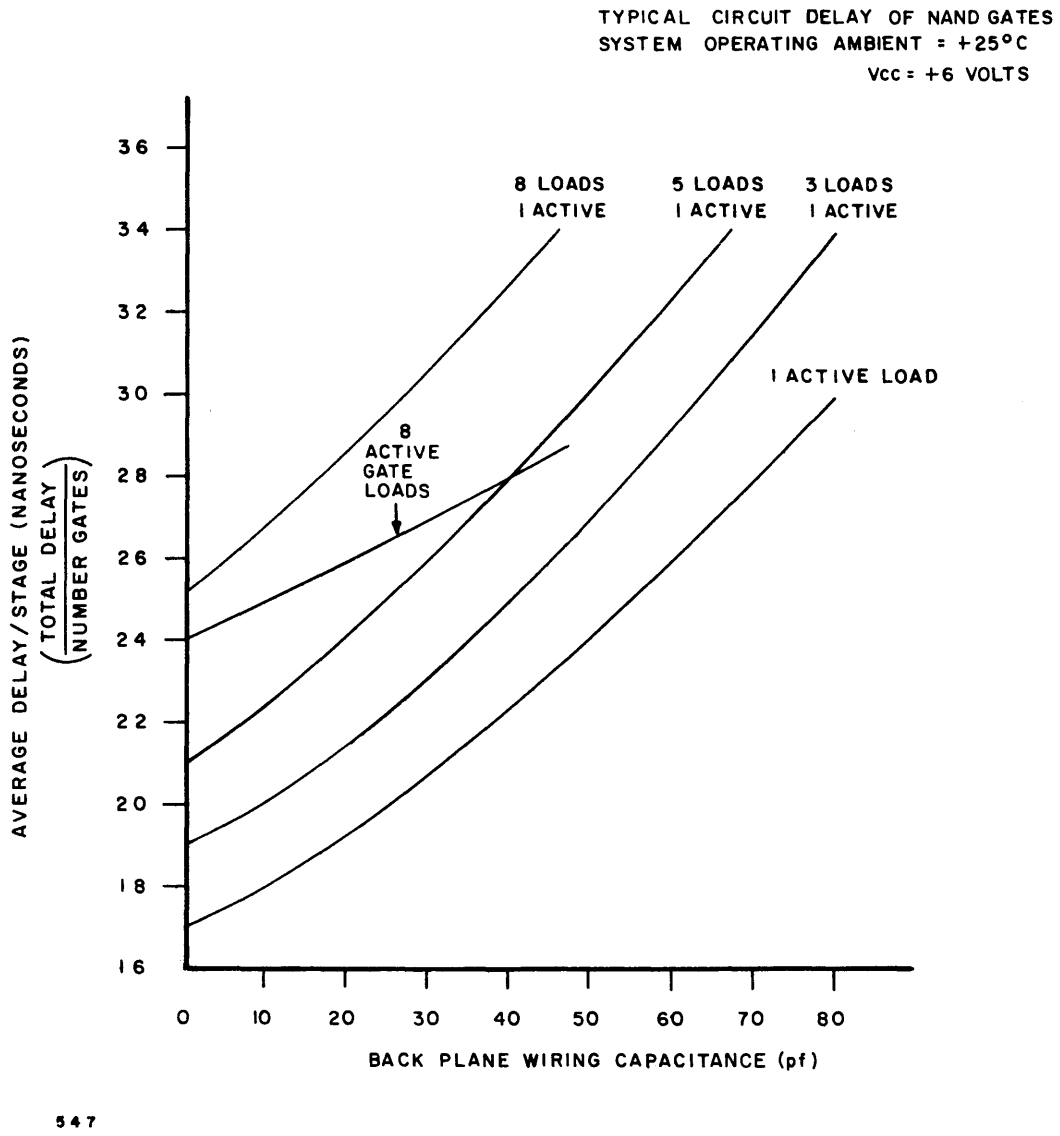


Figure 2-2. Typical NAND Gate Circuit Delays (Sheet 2 of 3)

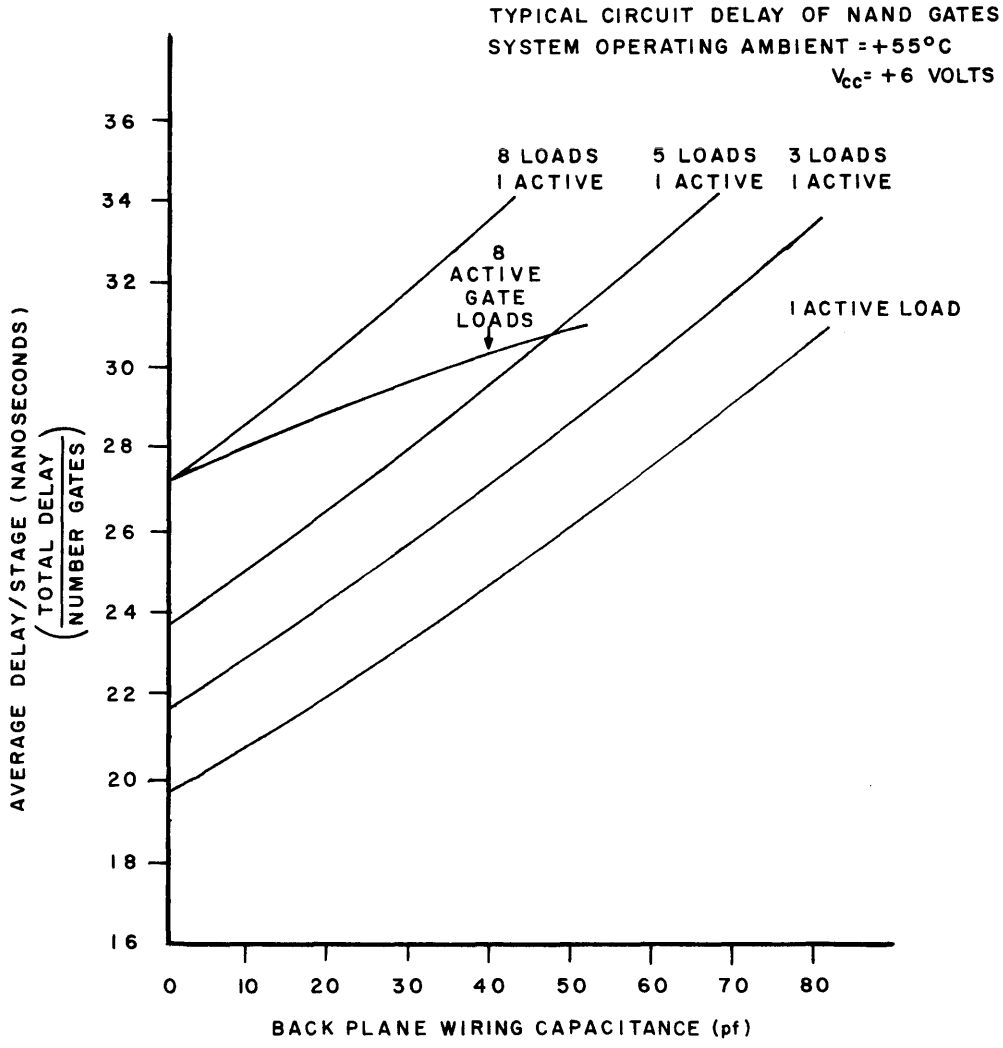


Figure 2-2. Typical NAND Gate Circuit Delays (Sheet 3 of 3)

system. The stray wiring capacitance will vary between 6 and 12 picofarads per foot, depending on the system wiring density. Due to the relatively small size of a μ-BLOC the wiring runs are minimized.

2-2.10 Typical Waveform Characteristics

The waveforms shown in Figure 2-3 are typical of a Model MC-335 clock driving a flip-flop, power amplifier, and two NAND gates in a series chain, with all logic elements operating at one-half their rated full load.

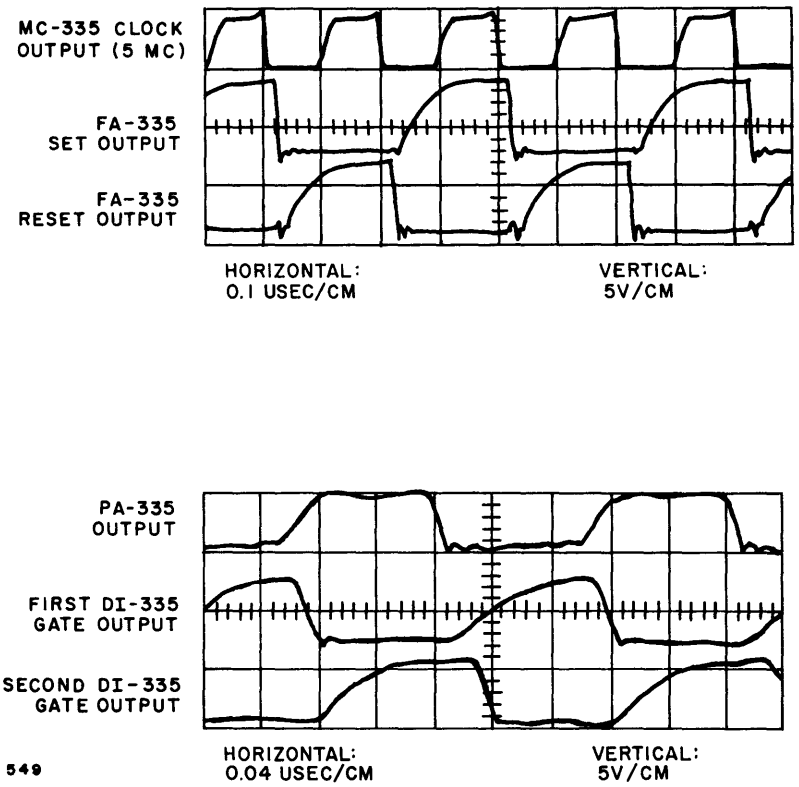


Figure 2-3. Typical μ-PAC Waveforms

2-3 NAND GATE F-01 AND F-02 CHARACTERISTICS

2-3.1 Basic NAND Circuit

The standard μ-PAC NAND gate is a grounded-emitter, inverter amplifier. All inputs are diode-buffered, and the output is either the voltage of a saturated transistor or the supply voltage. Accidental grounding of the output will not damage the circuit.

The gate performs the NAND function with conventional positive logic (+6v = ONE, 0v = ZERO). For negative logic, the gate performs the NOR function. (See Figure 2-4.)

When all inputs are at logic ONE (+6v) or open, the output transistor is turned on, and the output is logic ZERO (ground). If any input is at ground, the transistor is turned off, and the output is logic ONE (the supply voltage, +6v).

2-3.2 F-01 and F-02 NAND Microcircuits

In order to obtain maximum logic flexibility two types of NAND gate microcircuits are used, the F-01 dual NAND gate and the F-02 quad NAND gate. The two NAND gate types have similar specifications and differ only in logic capability. (See Figure 2-5.)

The F-01 dual NAND gate microcircuit contains two 3-input gates, each with an input node and a separate load resistor. The number of inputs to any gate can be expanded by tying the node of a gate to the node of a diode cluster. Outputs of gates with separate load resistors can be tied together as shown in Figure 2-6, to perform the AND-OR-INVERT function without loss of output drive capability.

The F-02 quad NAND gate microcircuit contains four 2-input NAND gates. Pairs of gates can be wired back to back to form a dc set-reset flip-flop.

2-3.3 Loading

Input Loading:	1 unit load
Output Drive Capability:	8 unit loads (capable of also driving 75 pf total capacitance with delays as specified)

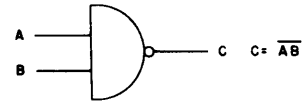
Outputs of gates with separate load resistors can be tied together to 1 load resistor with no loss in output drive capability.

2-3.4 Fan-In Expansion Using Nodes

12 at 5 mc

24 at 1 mc

Maximum fan-in is limited primarily by the maximum tolerable delays. The average propagation delay increases 3 nsec with each diode cluster that is tied to a node. The wire between nodes should be kept as short as possible by locating the PACs as close as possible to one another.



A. LOGIC FUNCTION

B. TRUTH TABLE

INPUT 1	INPUT 2	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

0 = GROUND
1 = +6V

550

Figure 2-4. Basic NAND Gate Logic

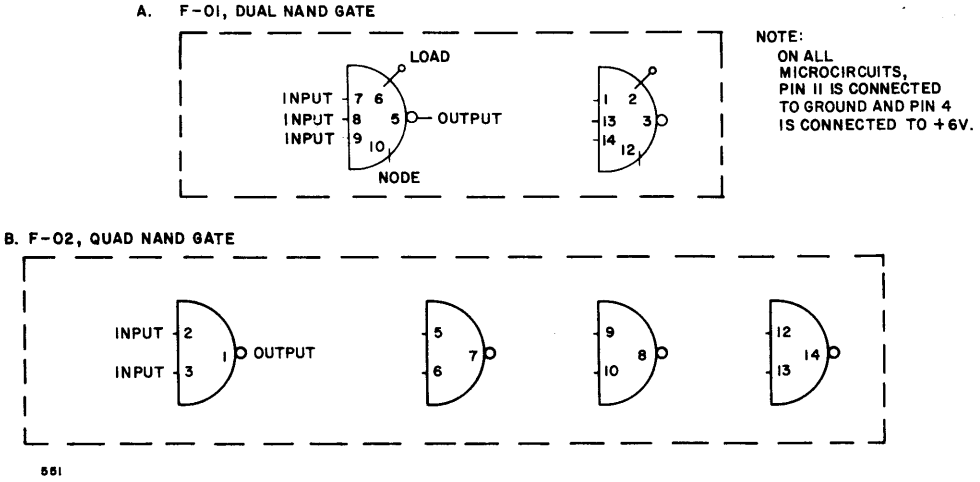


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Figure 2-5. Types F-01 and F-02 NAND Gate Equivalent Logic Symbols

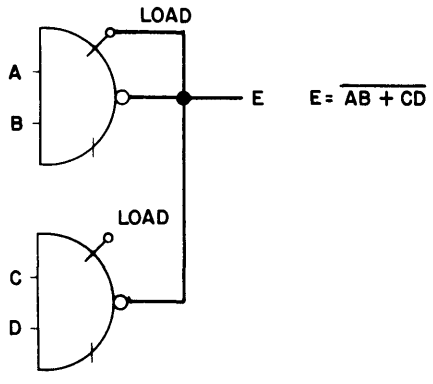

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Figure 2-6. Paralleled NAND Gates with Common Load Resistors

2-3.5 Circuit Delay

(Measured at the +1.5v level, and averaged over 2 stages)

24 nsec (typ)

30 nsec (max)

The maximum delay specifications stated in the detailed μ-PAC descriptions in Section III are based on worst-case loading conditions for both turn on and turn off. Typical delays are based on one-half maximum rated loading. (See paragraph 2-2.8.)

2-3.6 Load Resistors in Parallel

When the outputs of two type F-02 NAND gates are tied together, the structure has a fanout capability of 4 unit loads (two load resistors are in parallel.) When the outputs of three type F-02 NAND gates are tied together, the structure has a fanout of 1 unit load (three load resistors are in parallel).

Load Resistors in Parallel	Output Drive Capability
1	8
2	4
3	1

2-3.7 Paralleling Outputs with One Load Resistor

The maximum number of type F-01 NAND gate collector outputs that can be connected to one load resistor is limited by the maximum tolerable delay. The average propagation delay increases 3 nsec for each additional collector output that is jumpered through a connector to a standard output.

2-4 TYPE F-03 POWER AMPLIFIER CHARACTERISTICS

The type F-03 power amplifier microcircuit has two 3-input inverter amplifiers with nodes for input gating expansion. (See Figure 2-7.) The power amplifier circuit is logically equivalent to the NAND gate but has about three times the output drive capability. It has a short circuit protection network such that accidental grounding of the output will not damage the circuit.

2-4.1 Input Loading

2 unit loads

2-4.2 Output Drive Capability

25 unit loads (capable of also driving 250 pf total capacitance with delays as specified)

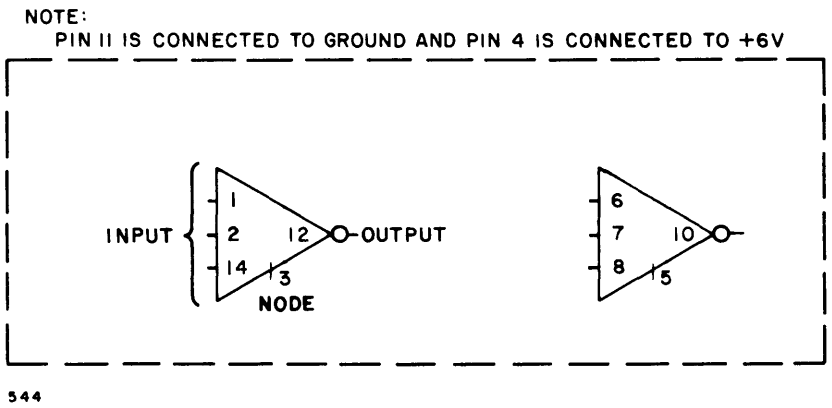


Figure 2-7. Type F-03 Power Amplifier Equivalent Logic Symbol

2-4.3 Circuit Delay

(Measured at the +1.5v level, averaged over two stages)

24 nsec (typ)

30 nsec (max)

The maximum delay is specified with a total of 250 pf capacitance and a dc current equivalent to 25 input gates.

2-5 TYPE F-04 FLIP-FLOP CHARACTERISTICS

The standard μ-PAC integrated circuit flip-flop, type F-04, is a double-rank, J-K flip-flop with dc set and reset capability. Figure 2-8 shows the logic symbol and equivalent logic circuit.

The clock gate portion of the flip-flop is composed of the clock and the set and reset control inputs. The control inputs are energized by logic ONEs. A ZERO-ONE-ZERO pulse on the clock will cause the flip-flop to assume the state determined by the condition of the control inputs. With J-K circuitry, no combination of the control input signals can cause an ambiguous state.

The set and reset control inputs may be used as follows.

a. To gate clock pulses

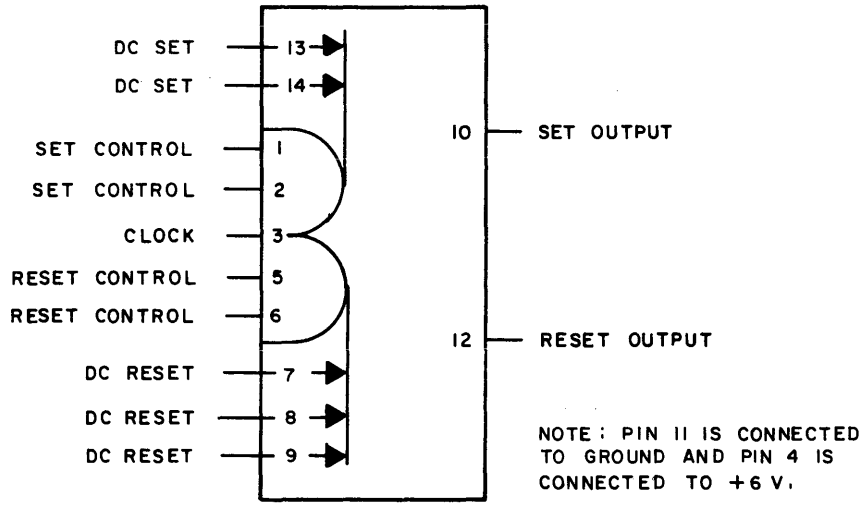
b. As direct set and reset inputs

c. As another clock input when a set and a reset control are tied together.

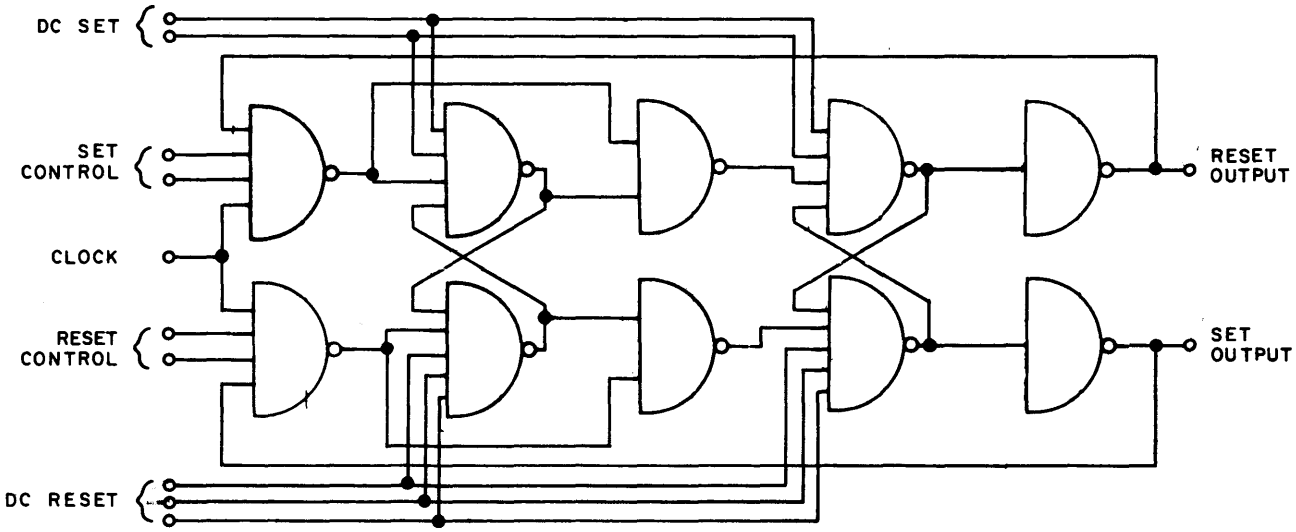
For dc operation, voltage levels are used on the dc inputs. Signals applied to the dc set and reset inputs take precedence over any ac gating. However, output spikes may occur when the reset clock gate is activated during a dc set, or vice-versa. Such spikes can be eliminated by tying the dc set input to a reset control input and tying the dc reset input to a set control input.

2-5.1 Pulse Dodging

The flip-flop utilizes the double-rank technique of pulse dodging (Figure 2-9). When the clock input makes the transition from ZERO to ONE, the state of the input flip-flop



A. LOGIC SYMBOL



B. EQUIVALENT LOGIC CIRCUIT

Figure 2-8. Type F-04 Flip-Flop Logic Symbol and Equivalent Logic Circuit

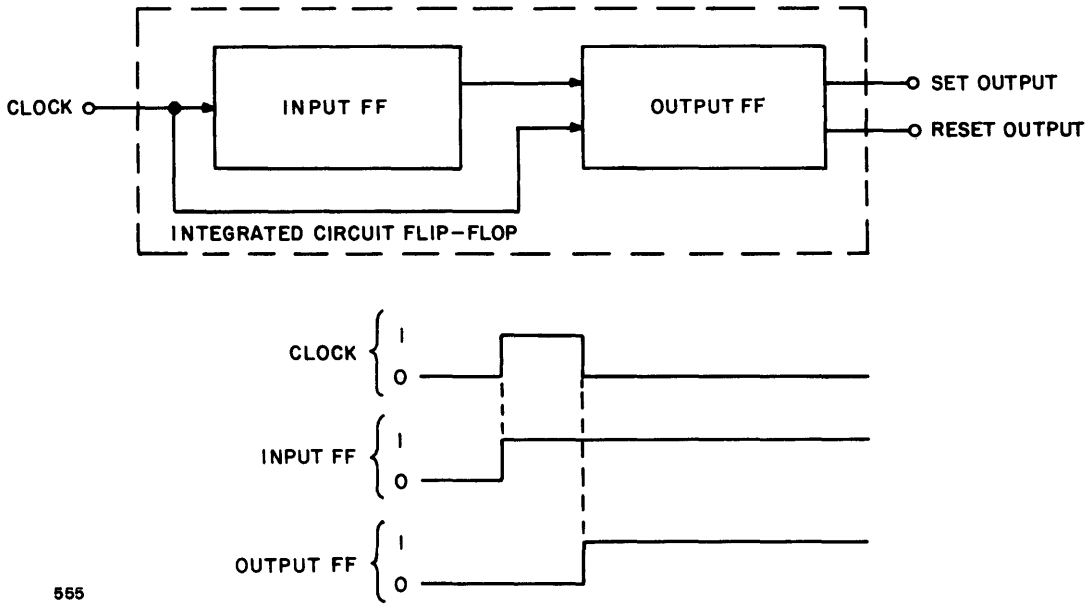


Figure 2-9. Double-Rank Flip-Flop Pulse Dodging, Timing Diagram

is fixed and data transfer from the input flip-flop to the input of the output flip-flop is inhibited. On the ONE to ZERO transition of the clock input, data from the input flip-flop is shifted to the output flip-flop and the inputs to the input flip-flop are inhibited. Thus the clock provides intrinsic pulse dodging by means of trailing edge triggering. This feature permits strobing of the flip-flop output with input triggering signals.

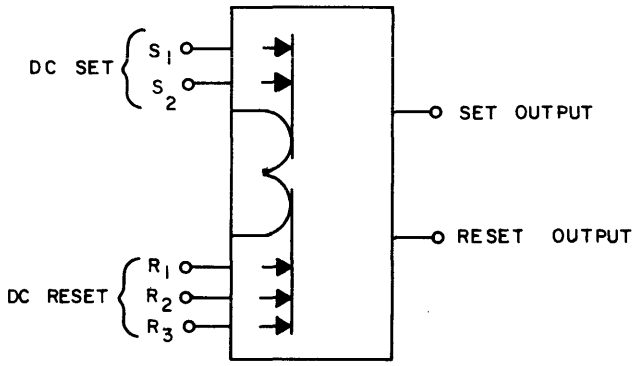
2-5.2 DC Operation

If either dc set goes to logic ZERO, the flip-flop will assume the ONE state; if any dc reset goes to ZERO, the flip-flop will assume the ZERO state. If both a dc set and a dc reset go to ZERO at the same time, both the set and the reset outputs will go to logic ZERO. Figure 2-10 contains diagrams and equations describing this mode of flip-flop operation.

2-5.3 Control Inputs Used to Steer Clock Pulses

If both the set controls (S_C) and the reset controls (R_C) are logic ONES, the flip-flop will be complemented by the application of a clock pulse. If only S_C or R_C is a ONE, the state of the flip-flop will be a ONE or ZERO, respectively, after the clock is energized. If both S_C and R_C are ZERO, the flip-flop will remain in its previous state. One restriction is that when a control input is used to gate the clock, the control input cannot change from the ONE to the ZERO state while the clock is a ONE. Figure 2-11 contains diagrams and equations describing this mode of flip-flop operation.

A.) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_D - AND result of the dc set inputs. $S_D = S_1 \cdot S_2$

R_D - AND result of the dc reset inputs. $R_D = R_1 \cdot R_2 \cdot R_3$

F - state of the flip-flop (set output)

F' - previous state of the flip-flop

S_D	R_D	F
0	0	(Both set and reset outputs are 0's.)
0	1	1
1	0	0
1	1	F' (no change)

$$F = R_D (\overline{S}_D + F')$$

C.) TIMING DIAGRAM

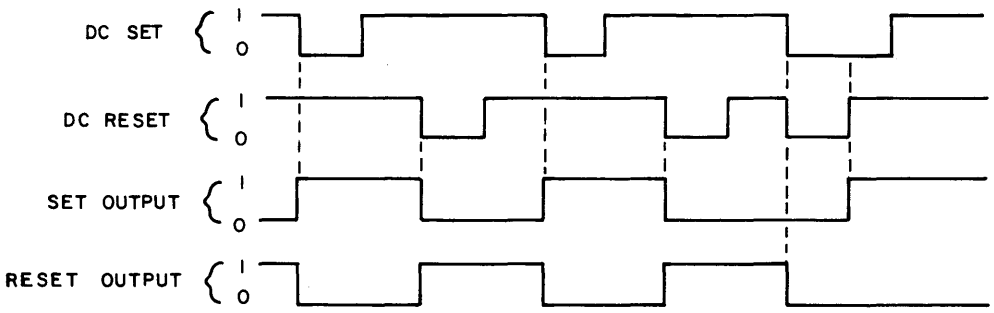


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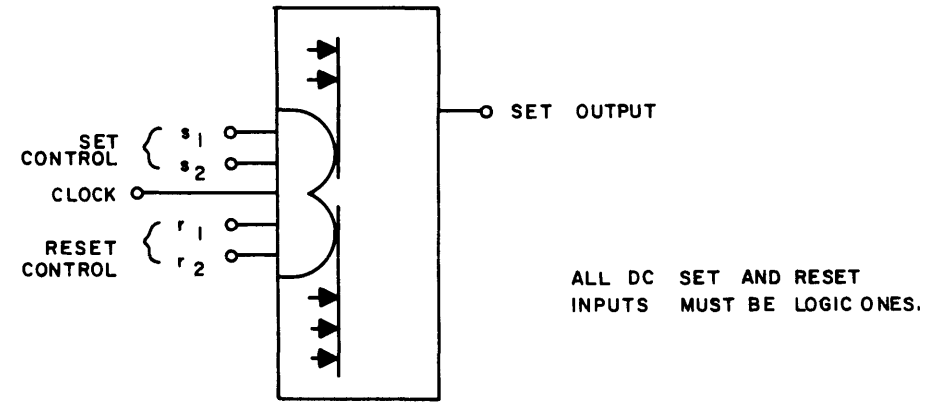
Figure 2-10. DC Operation

A) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_C - AND result of the set control inputs, $S_C = s_1 \cdot s_2$

R_C - AND result of the reset control inputs, $R_C = r_1 \cdot r_2$

F' - previous state of the flip-flop

F - state of the flip-flop after the clock pulse

S	R	F'	F	
0	0	0	0	NO CHANGE
0	0	1	1	
0	1	0	0	RESET
0	1	1	0	
1	0	0	1	SET
1	0	1	1	
1	1	0	1	COMPLEMENT
1	1	1	0	

$$F = S_C \overline{F'} + \overline{R}_C F'$$

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Figure 2-11. Control Inputs Used to Gate Clock Pulses (Sheet 1 of 2)

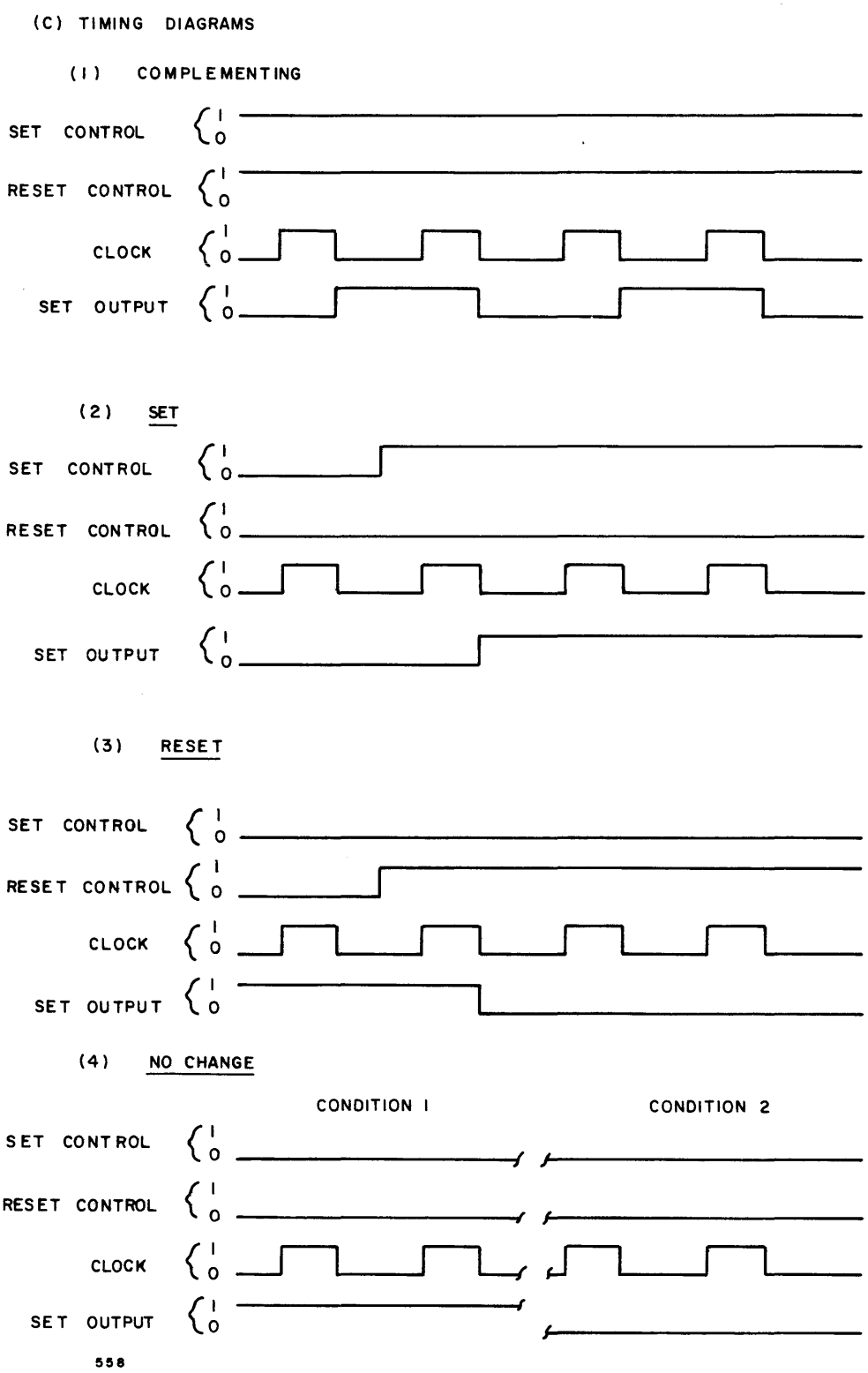


Figure 2-11. Control Inputs Used to Gate Clock Pulses (Sheet 2 of 2)

2-5.4 Control Inputs Used as a Second Clock

A set and a reset control can be tied together and used as another clock input. In this case, the resultant clock is the ANDed result of both clocks. Figure 2-12 contains diagrams describing this mode of flip-flop operation.

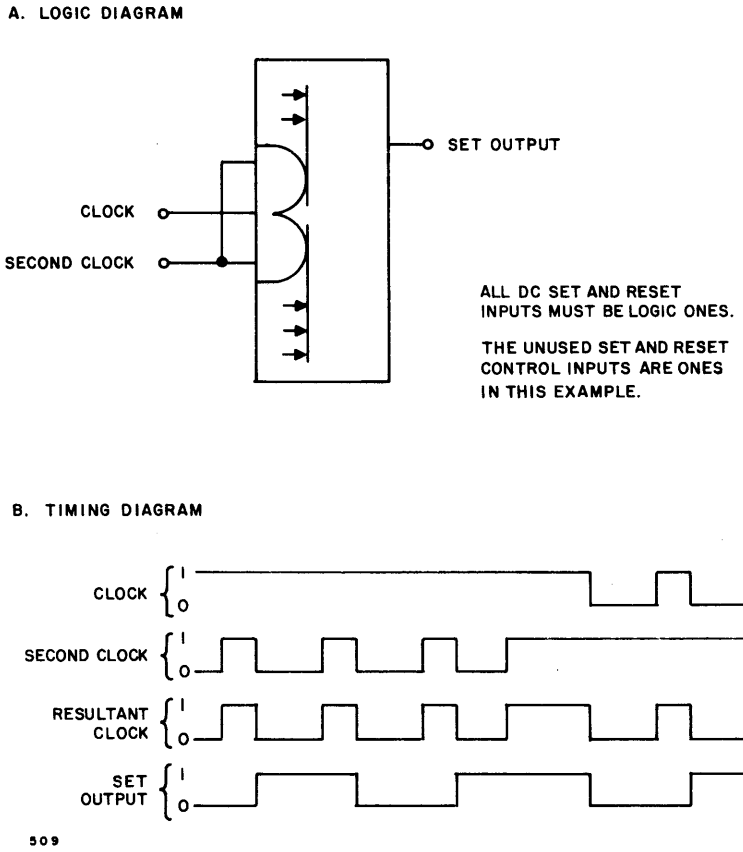


Figure 2-12. Control Inputs Used As a Second Clock

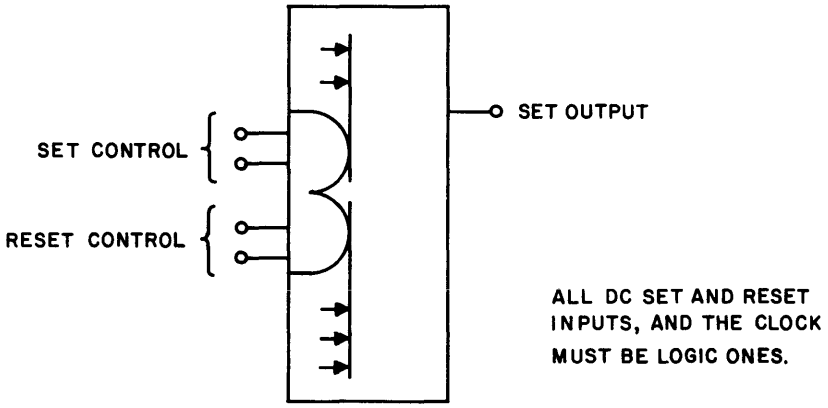
2-5.5 Control Inputs Used Directly to Set or Reset

The set and the reset control inputs can also be used separately to change the state of the flip-flop. When the clock is a ONE, the first control input that goes from ONE to ZERO acts as the clock input. After a set control changes from ONE to ZERO, the flip-flop will be in the ONE state. After a reset control changes from ONE to ZERO, the flip-flop will be in the ZERO state. Figure 2-13 contains diagrams and equations describing this mode of flip-flop operation.

2-5.6 Input Loading

DC inputs:	2/3 unit load
Clock input:	1 unit load
Control inputs:	1 unit load

A. LOGIC DIAGRAM



B) Boolean Equations

S_C - AND result of the set control inputs

R_C - AND result of the reset control inputs

F - state of the flip-flop

primes (') - previous state of a signal

$$F = S'_C \cdot \overline{S}_C \qquad \text{(setting operation)}$$

$$\overline{F} = R'_C \cdot \overline{R}_C \qquad \text{(resetting operation)}$$

C. TIMING DIAGRAM

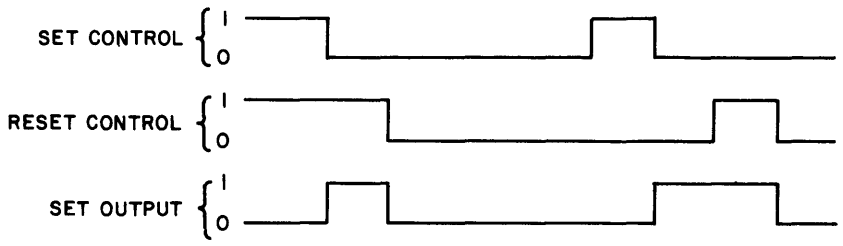


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Figure 2-13. Control Inputs Used Directly to Set or Reset

2-5.7 Output Drive Capability

8 unit loads (both outputs)

(Capable of also driving 75 pf total capacitance with delays as specified.)

2-5.8 Circuit Delay

The following circuit delays are specified from the +1.5v level of the input signal to the +1.5v level of the output signal.

Clock input (ONE to ZERO transition) to latest output	45 nsec (typ) 60 nsec (max)
DC set input to set output or DC reset input to reset output	65 nsec (typ) 80 nsec (max)
DC set input to reset output or DC reset input to set output	45 nsec (typ) 60 nsec (max)

2-5.9 Clock and Control Input Timing Requirements

To trigger the flip-flop at the clock or control inputs, pulses must meet the requirements shown in Figure 2-14.

2-5.10 DC Input Timing Requirements

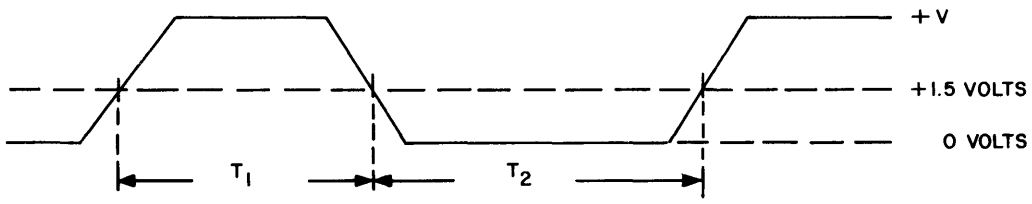
To activate a dc input, signals must meet the requirements of Figure 2-15.

2-5.11 Control Inputs

Figure 2-16 shows the timing requirements of the set and reset control inputs when they are being used to steer the triggering clock input to set the flip-flop. The reset control input must be completely switched to logic ZERO before the clock starts positive. No control input should go from logic ONE to ZERO while the clock is positive. The set control input must be switched to logic ONE at least 40 nsec before the clock starts towards logic ZERO. The clock must be a positive pulse of 40 nsec minimum duration. The flip-flop changes state on the trailing edge of the positive clock pulse. Reset timing is the same, except that the time relations and logic levels of the set and reset input must be interchanged.

2-5.12 Maximum Allowable Clock Skew

In cases where a register is being driven by clock (shift) signals from different sources, the output of one stage may arrive at the next stage before late clock signal. If the delay between the early and late clock signals is more than 30 nsec, erroneous data transfer may occur. To guarantee proper operation the allowable clock skew must be as shown in Figure 2-17. Note that the triggering signal to flip-flop B is S_A rather than C_B. This situation is not detrimental to the operation of the shift register. Either S_A or C_B may trigger flip-flop B, depending on which occurs first.



T_1 (POSITIVE TIME) = 40 NSEC. (MIN)

T_2 (NEGATIVE TIME) = 60 NSEC. (MIN)

+V (INPUT ONE LEVEL) = +3.0 VOLTS (MIN)

T_{RISE} AND T_{FALL} REQUIREMENT – ANY μ-PAC OUTPUT SIGNAL WILL RELIABLY TRIGGER THE FLIP FLOP.

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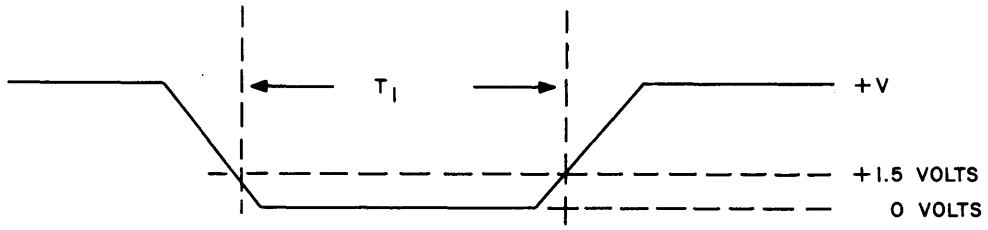
Figure 2-14. Flip-Flop Input Pulse Requirements



T_1 (TIME AT LOGIC ZERO) = 80 NSEC. (MIN.)

V (INPUT ONE LEVEL) = +3.0 VOLTS (MIN.)

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Figure 2-15. DC Set and Reset Input Signal Requirements

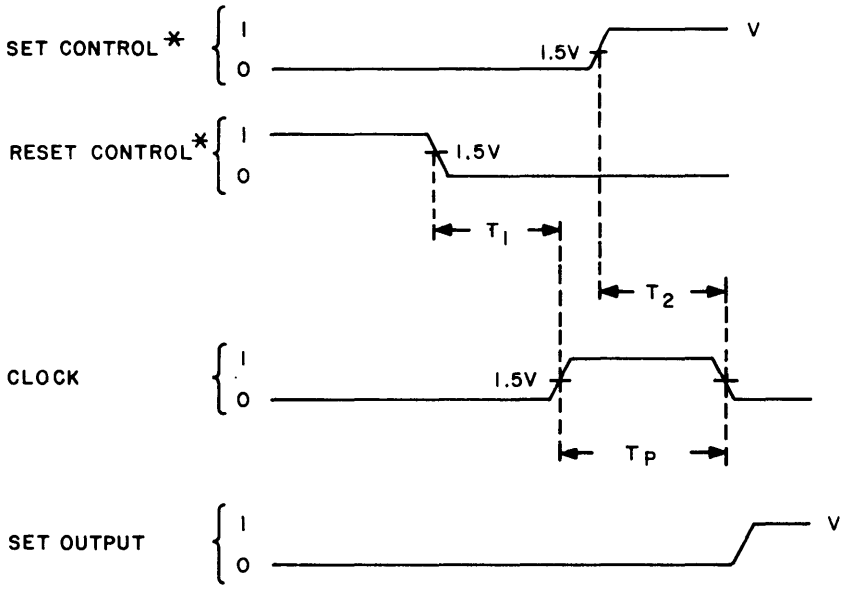


Figure 2-16. Timing Requirements for Control Inputs, Using Clock Triggering

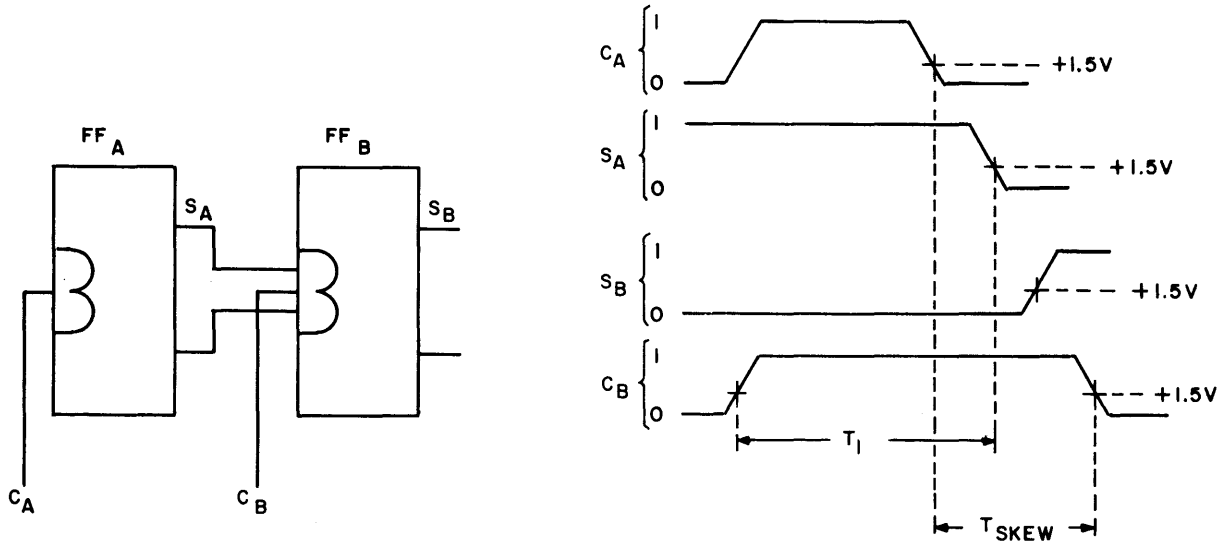


Figure 2-17. Allowable Clock Skew, Logic and Timing

SECTION III
DESCRIPTIONS OF μ-PAC MODULES AND EQUIPMENT

CAUTION

If replacement type is not specified in the parts list, for a component which appears to be standard, order by 3C part number only. Such components have been selected for certain critical parameters.

3-0 COPPER CLAD PAC KIT, MODEL AS-330

The Copper Clad PAC Kit, Model AS-330 (Figure 3-0.1), consists of a standard μ-PAC card and a separate handle and retaining roll pins. The μ-PAC card has gold-plated etched connector fingers attached to approximately 5.5 sq in. of copper on both sides of the PAC. Registration marks are provided so that double-sided etching from photographic negatives can be accomplished. It is recommended that the etchant for the copper be a solution of 100 lb ammonia persulphate/60 gallons of water with a maximum etching time of 6 minutes, otherwise the gold plating will be removed from the fingers.

The maximum allowable height of components on the AS-330 when the PAC is mounted in a solderless-wrap μ-BLOC is 0.115 in. on the component side and 0.080 in. on the etch side. For a taper-pin μ-BLOC, the maximum heights are 0.36 in. and 0.32 in. However, if the adjacent PAC slots of either BLOC are left vacant, any component height can be attained.

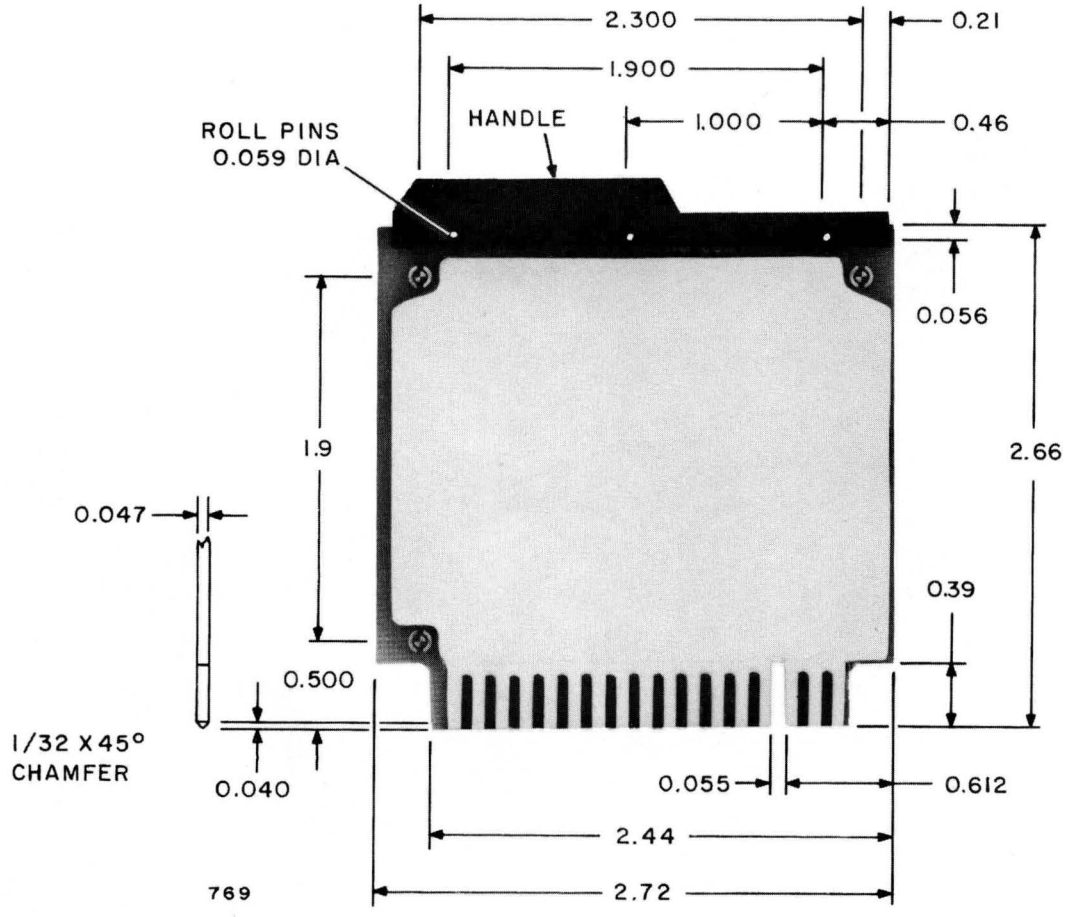


Figure 3-0.1. Copper Clad PAC Kit, Model AS-330, Dimensions (Etch Side View)

3-1 COUNTER PAC, MODEL BC-335

The Counter PAC, Model BC-335 (Figures 3-1.1 and 3-1.2), contains six independent flip-flops that can be used for counting, frequency division, and buffer storage. Each stage has a complement input, dc set and dc reset inputs, and set and reset outputs. There is also a common reset input for clearing all stages simultaneously. Application of a signal to the complement input causes the flip-flop to change state. (Toggling action is accomplished without additional wiring.) A detailed description of the basic flip-flop circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

DC Set and Reset. -- A signal at logic ZERO for 80 nsec or longer on the dc set (or reset) input will set (or reset) the flip-flop.

Common Reset. -- A signal at logic ZERO for 80 nsec or longer on the common reset input will clear the six counter stages simultaneously.

Complement. -- The output changes state on the negative (ONE to ZERO) transition of the complement input. This input is the same as the clock input of the integrated circuit flip-flop. Waveform requirements are shown in Section II.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Common reset:	4 unit loads
Complement:	1 unit load each

Output Drive Capability

8 unit loads each

Handle Color Code

Blue

Circuit Delay

Complement input to flip-flop outputs (counter propagation stage delay):
60 nsec (max)

DC set input to set output, or dc reset input to reset output:
80 nsec (max)

DC set input to reset output, or reset input to set output:
60 nsec (max)

Current Requirements

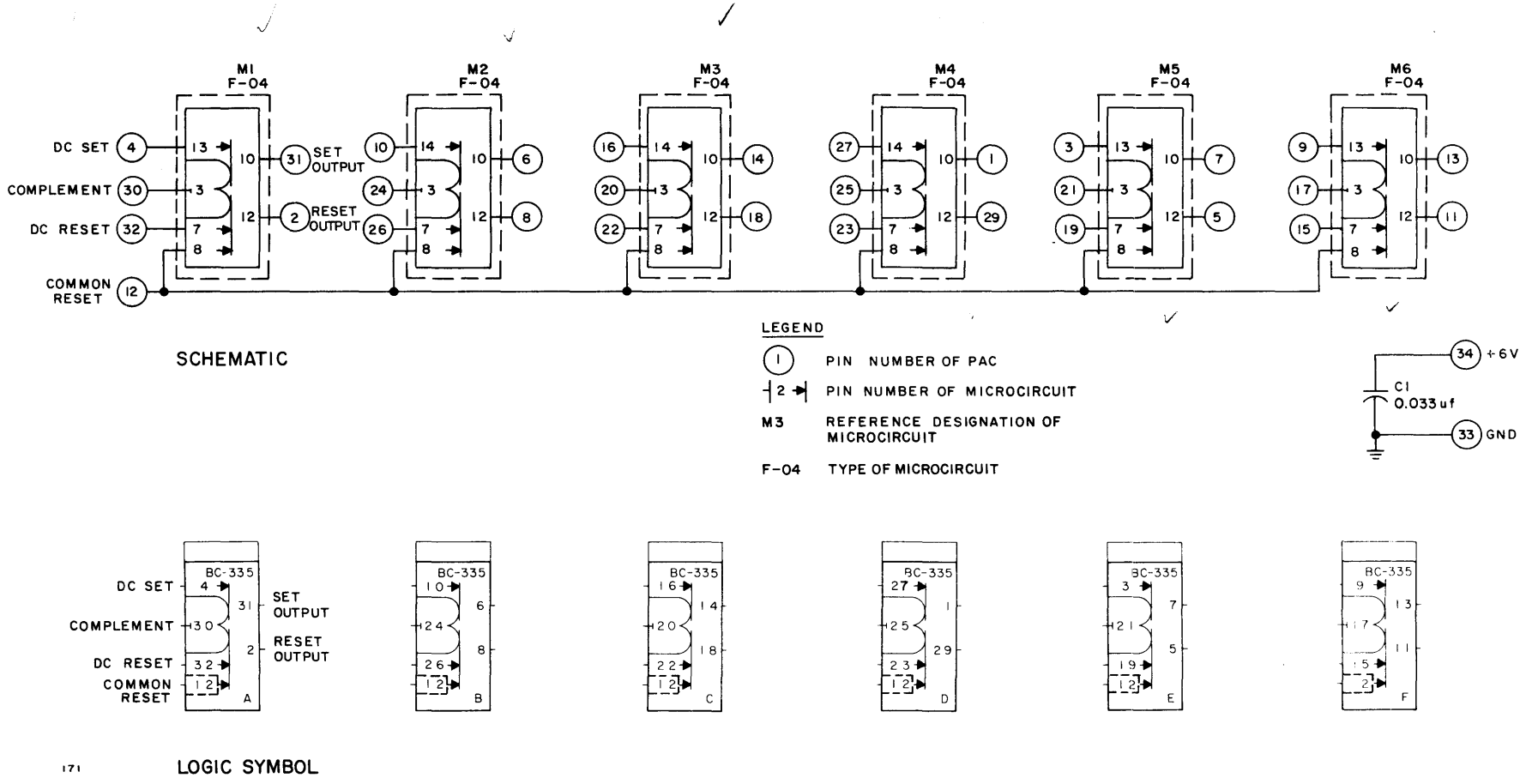
+6v: 150 ma (max)

Power Dissipation

0.90w (max)

APPLICATIONS

Each of the stages can be used separately for divide-by-two, complementing operation. Successively connecting the set output of one stage to the complement input of another stage (Figure 3-1.3) results in frequency division by factors of 4, 8, 16, 32 or 64. In this configuration, the PAC has a capacity as a counter of 0 through $2^6 - 1$, a total of 64 states.



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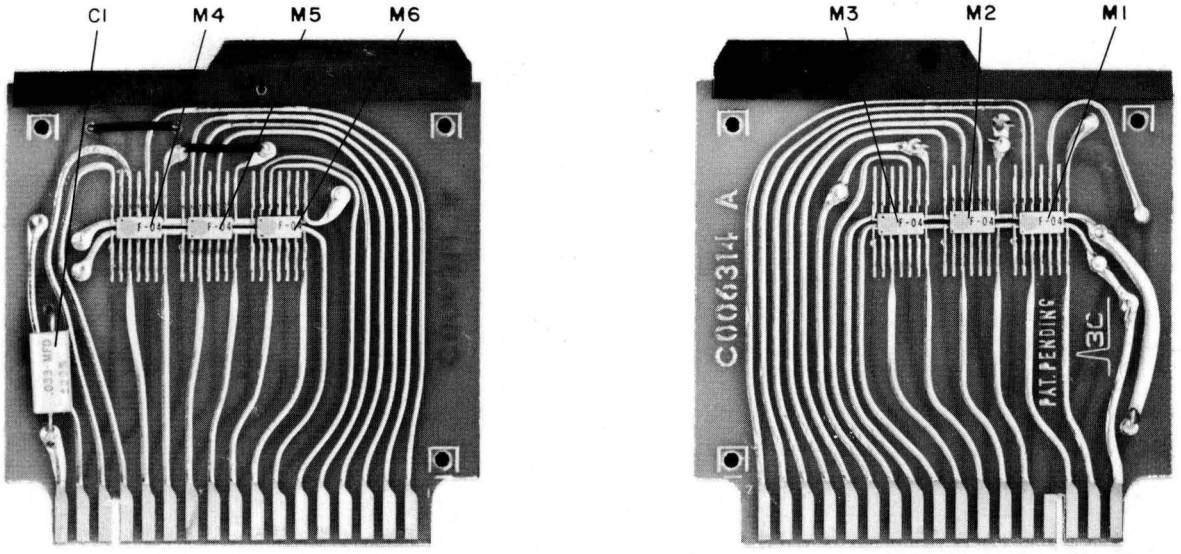
| Note: For Ser. No. up to and including 978.

Figure 3-1.1. Counter PAC, Model BC-335, Schematic Diagram and Logic Symbol
Note: Refer to Figure 3-1.1A for PACs with Ser. Nos. 979 and beyond

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

| Note: Refer to Figure 3-1.2A for PACs with Ser. Nos. 979 and beyond.

Figure 3-1.2. Counter PAC, Model BC-335, Parts Location and Identification

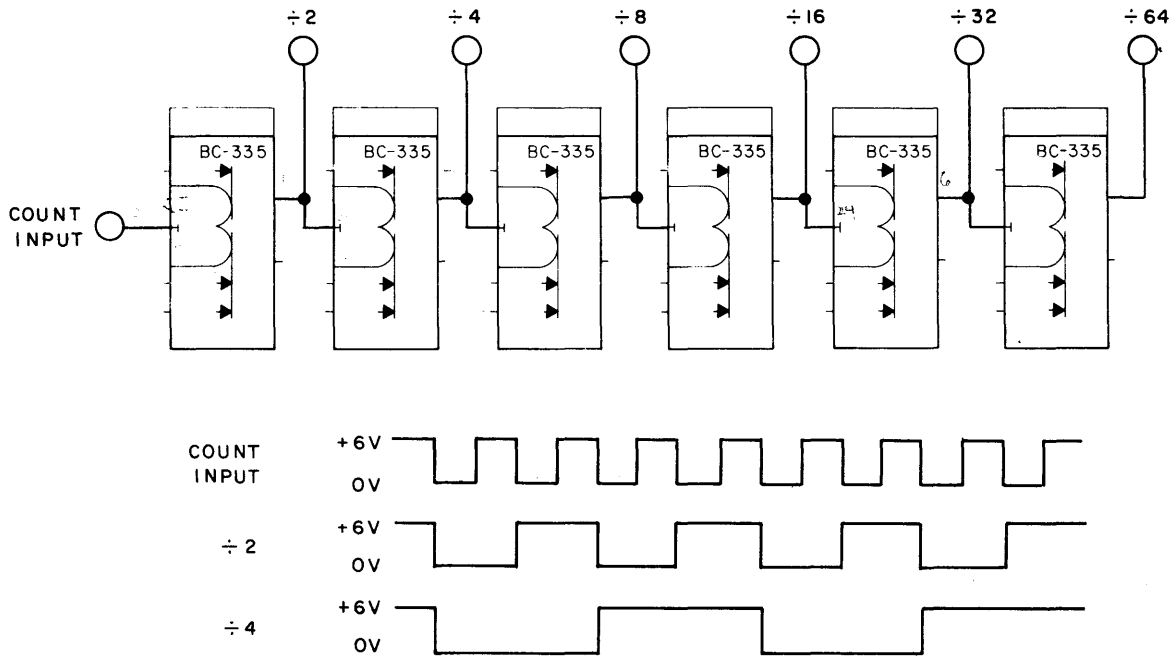

Figure 3-1.3. Counter PAC, Model BC-335, Operation As a Frequency Divider

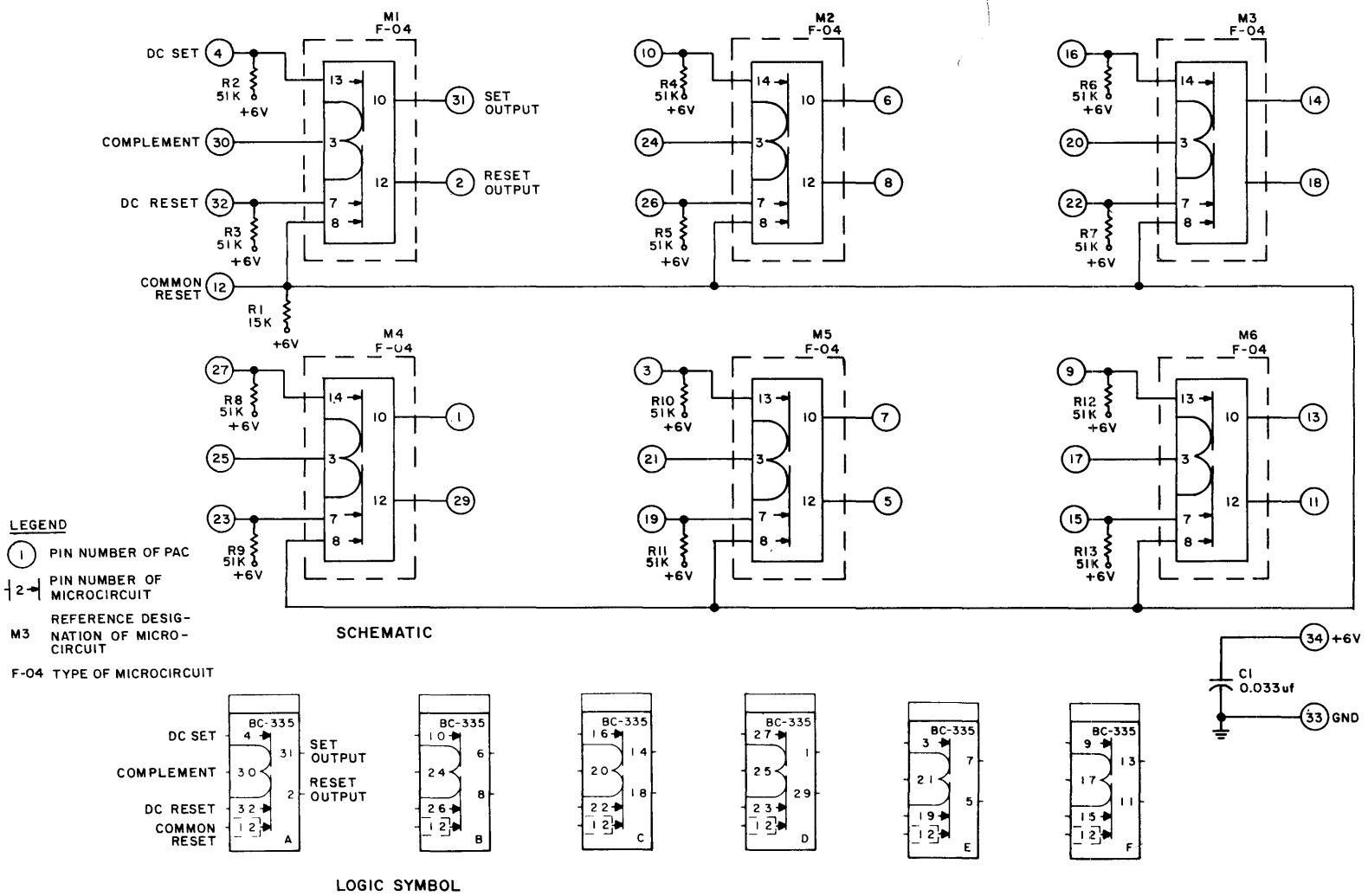

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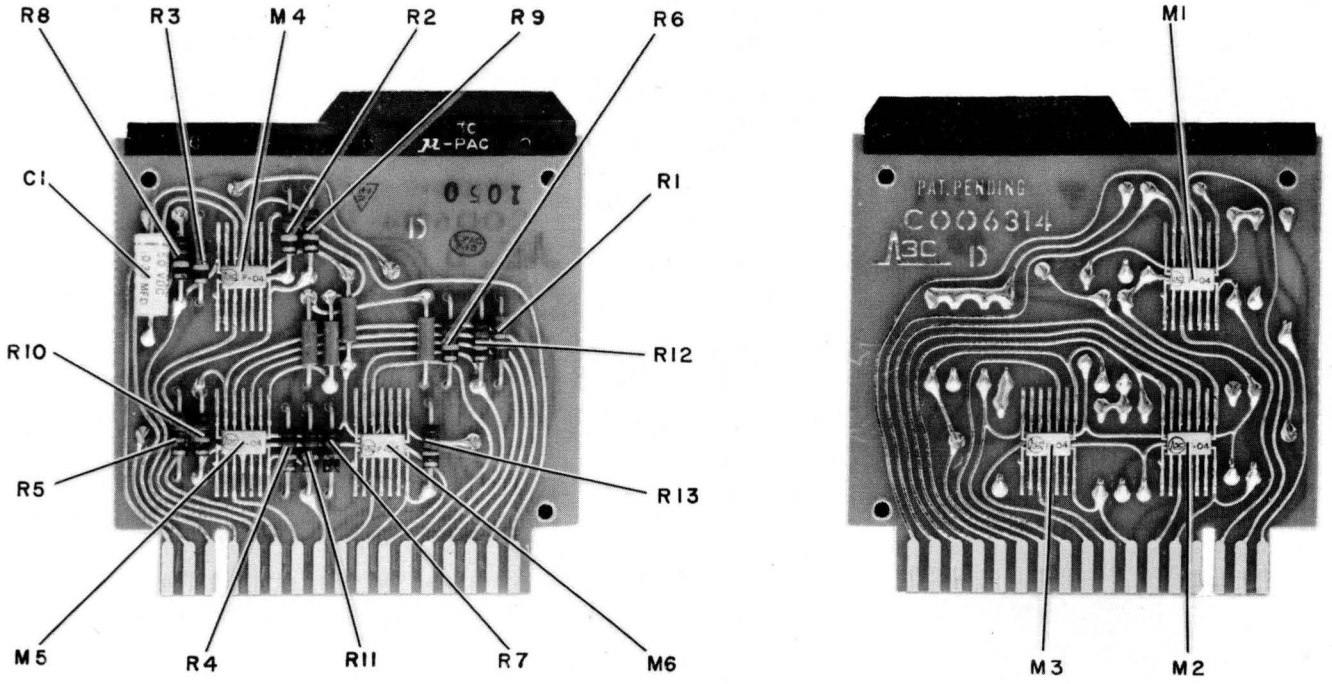
Figure 3-1.1A. Counter PAC, Model BC-335 (Ser. No. 979 and beyond), Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15K ±5%, 1/4 w	932 007 077
R2-R13	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4 w	932 007 090

Figure 3-1.2A. Counter PAC, Model BC-335 (Ser. No. 979 and beyond)
Parts Location and Identification

3-2 BINARY COUNTER PAC, MODEL BC-336

The Binary Counter PAC, Model BC-336 (Figures 3-2.1 and 3-2.2), is built to order, with 8 to 20 prewired binary counter stages. The set output of each stage is accessible at the PAC terminals. The counter can be cleared by gated or ungated reset signals. Each count-input pulse increases the binary content of the counter by one bit. The PAC also contains one independent NAND gate.

INPUT AND OUTPUT SIGNALS

Reset. -- Two reset inputs are provided, each capable of resetting up to 10 stages. A signal at logic ONE for 80 nsec or longer will reset all connected stages. (One or both of the gated reset inputs must be at ground.) The reset inputs can be tied together, allowing a single input signal to clear all counter stages.

Gated Reset. -- A signal at logic ZERO for 100 nsec or longer on either gated reset input will clear all counter stages. These inputs are operative only if both reset inputs are at logic ONE or disconnected.

Count. -- The count input is the same as the clock input of the integrated circuit flip-flop. Waveform requirements are shown in Section II. The counter changes state on the negative (ONE to ZERO) transition.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

Count:	1 unit load
Reset:	1 unit load each
Gated reset:	1 unit load each
Input (NAND gate):	1 unit load each

Reset Timing

Reset:	80 nsec (min) at logic ONE to reset
Gated reset:	100 nsec (min) at logic ZERO to reset

Output Drive Capability

Counter:	7 unit loads each stage
NAND gate:	8 unit loads

Circuit Delay

Counter propagation delay per stage:	60 nsec (max)
Clearing counter from reset input:	100 nsec (max)
Clearing counter from gated reset input:	120 nsec (max)
NAND gate delay (Measured at +1.5v, averaged over 2 stages):	30 nsec (max)

Current Requirements (20 counter stages)

+6v: 533 ma (max)

Power Dissipation (20 counter stages)

3.2w (max)

Handle Color Code

Blue

APPLICATIONS

The BC-336 can be used as a binary counter or power-of-2 frequency divider. A 20-stage PAC can accumulate numbers from 0 to $2^{20}-1$ (1,048,575) or divide the input frequency by a factor of up to 2^{20} (1,048,576).

8-20 STAGES, BUILT TO ORDER

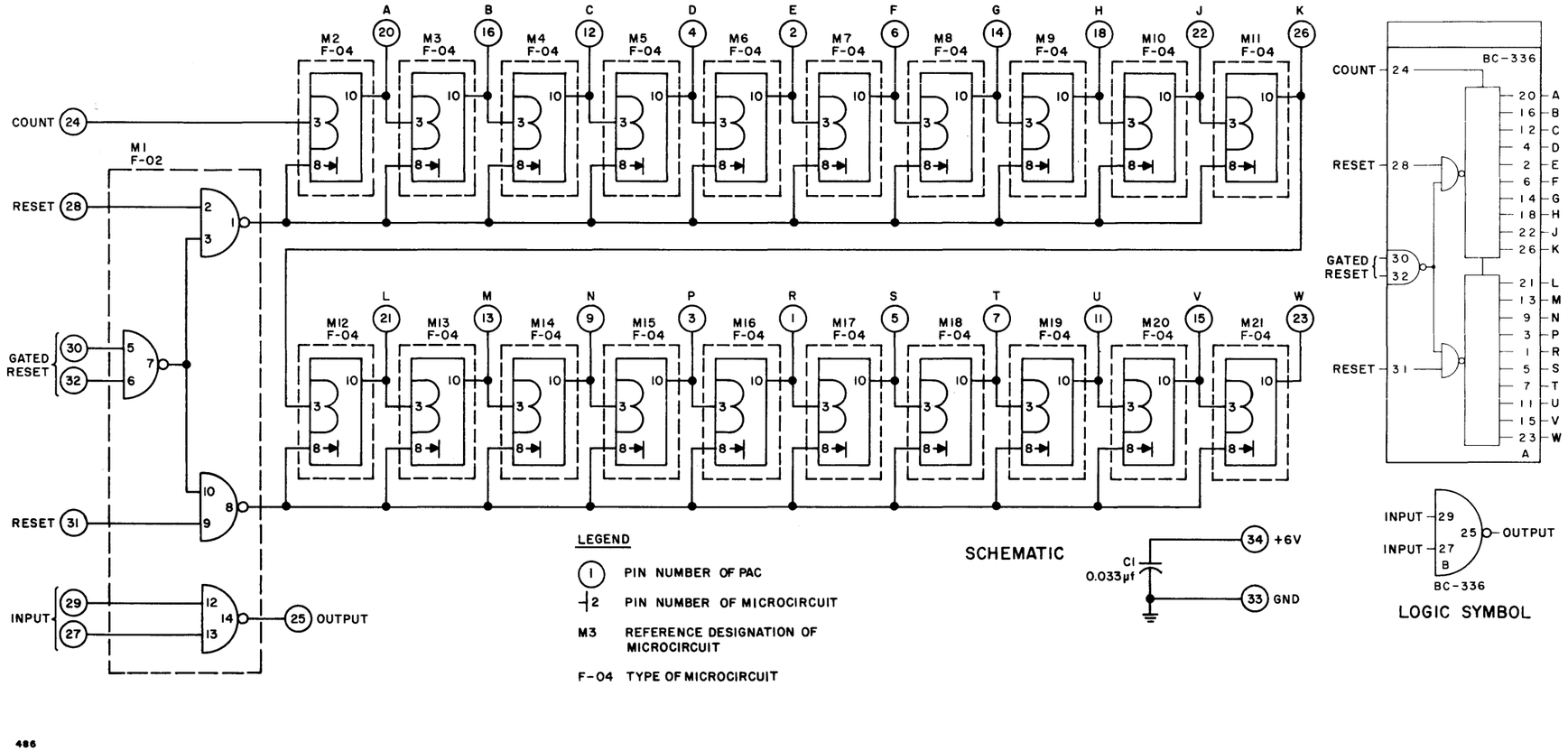
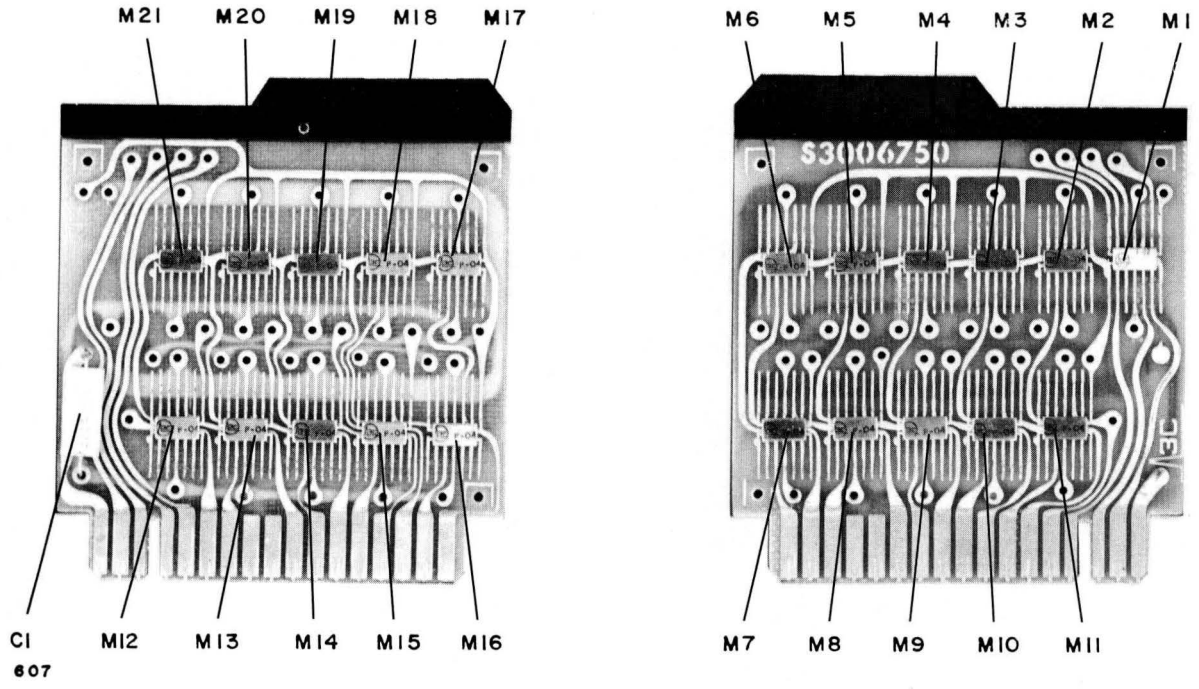


Figure 3-2.1. Binary Counter PAC, Model BC-336, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M2 - M21	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-2.2 Binary Counter PAC, Model BC-336,
Parts Location and Identification

3-3 FAST CARRY COUNTER PAC, MODEL BC-337

The Fast Carry Counter PAC, Model BC-337 (Figures 3-3.1 and 3-3.2) contains eight pre-wired counter stages that can be set up by a few PAC connector jumpers to operate as an eight-stage binary counter or a two-digit BCD counter. In either configuration, carries are anticipated by gating structures, to reduce counter propagation delays.

Each stage has a dc set input for presetting a starting count, and a common reset input for clearing all eight stages simultaneously.

INPUT AND OUTPUT SIGNALS

Count. -- The contents of the counter increase by 1 on the negative (ONE to ZERO) transition of the count input. This input is the same as the clock input of the integrated circuit flip-flop. Waveform requirements are shown in Section II.

Common Reset. -- A signal at logic ZERO for 80 nsec or longer on the common reset input clears all eight counter stages simultaneously.

BCD and BIN inputs. -- These points are to be connected as shown in Figure 3-3.3 for binary counting or as shown in Figure 3-3.4 for BCD counting.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC set inputs: 2/3 unit load each
Common reset: 5 unit loads
Complement: 2 unit loads

Output Drive Capability

Output	Binary Mode	BCD Mode
A and E	5 unit loads each	5 unit loads each
$\overline{A}$ and $\overline{E}$	8 unit loads each	8 unit loads each
B and F	5 unit loads each	6 unit loads each
$\overline{B}$ and $\overline{F}$	8 unit loads each	8 unit loads each
C and G	6 unit loads each	7 unit loads each
$\overline{C}$ and $\overline{G}$	8 unit loads each	8 unit loads each
D	6 unit loads each	6 unit loads each
H	8 unit loads each	8 unit loads each
$\overline{D}$ and $\overline{H}$	8 unit loads each	6 unit loads each

Circuit Delay

Counter propagation delay per group of 4 stages:	100 nsec (max)
Counter propagation delay for the 8 stage counter:	200 nsec (max)
DC set input to set output, or common reset input to reset output:	80 nsec (max)
DC set input to reset output, or common reset input to set output:	60 nsec (max)

Current Requirements

+6v 200 ma (max)

Power Dissipation

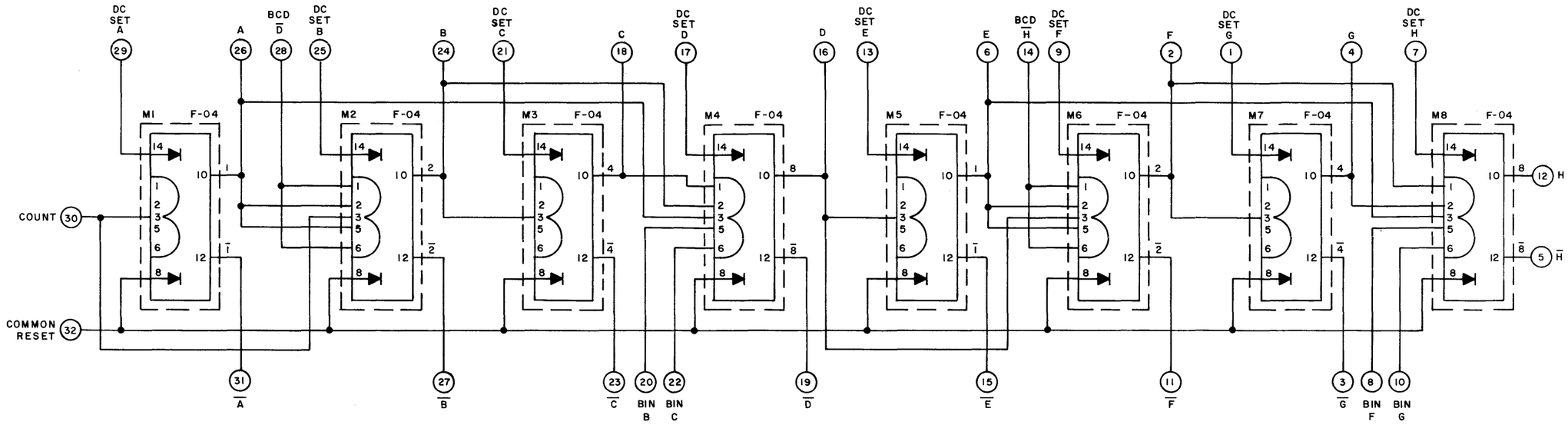
1.2w (max)

Handle Color Code

Blue

APPLICATIONS

Figure 3-3.3 shows the μ-PAC wired as an 8-bit binary counter. Frequency division by multiples of 2, up to 256, may be attained. Figure 3-3.4 shows the μ-PAC wired as a 2-decimal digit BCD counter. The counter can be preset to a number by first resetting all stages, then setting only the appropriate ones.



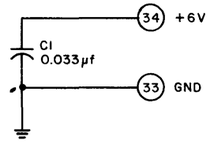
LEGEND

(1) PIN NUMBER OF PAC

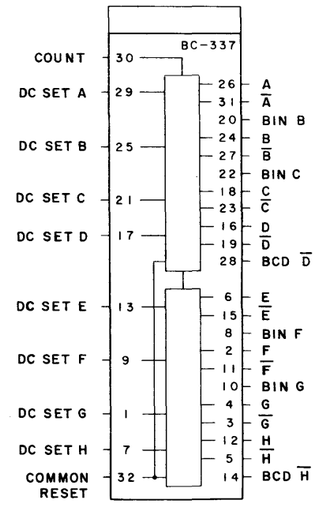
2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT



SCHEMATIC

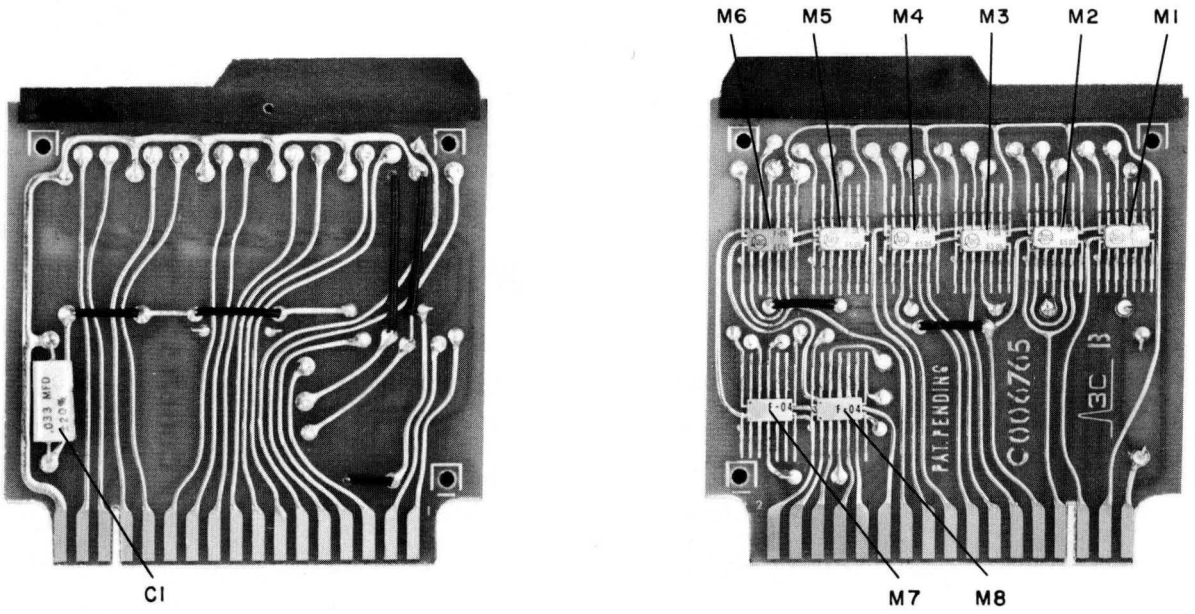


LOGIC SYMBOL

Note: Refer to Figure3-3.1A for PACs with Ser. No. 800 and beyond.

Figure 3-3.1. Fast Carry Counter PAC, Model BC-337, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M8	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

| Note: Refer to Figure 3-3.2A for PACs with Ser. No. 800 and beyond.

Figure 3-3.2. Fast Carry Counter PAC, Model BC-337, Parts Location and Identification

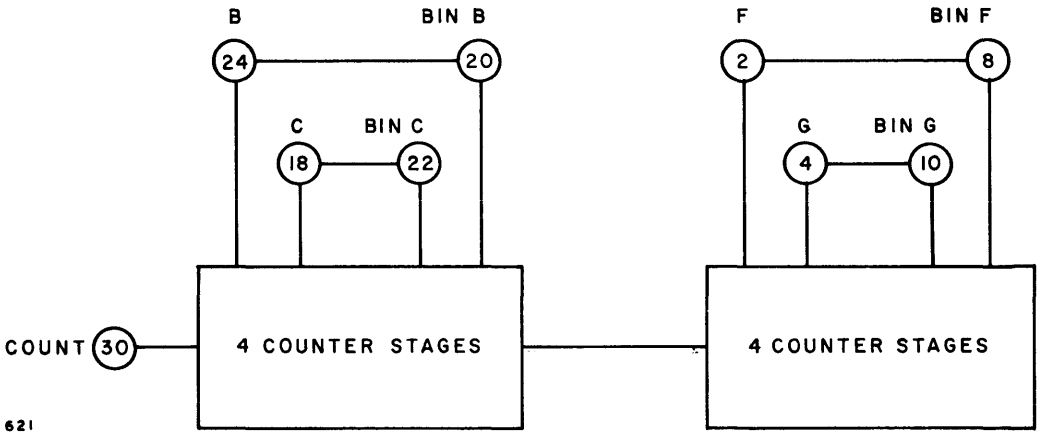


Figure 3-3.3. Fast Carry Counter PAC, Model BC-337, Jumper Connections for Binary Counting

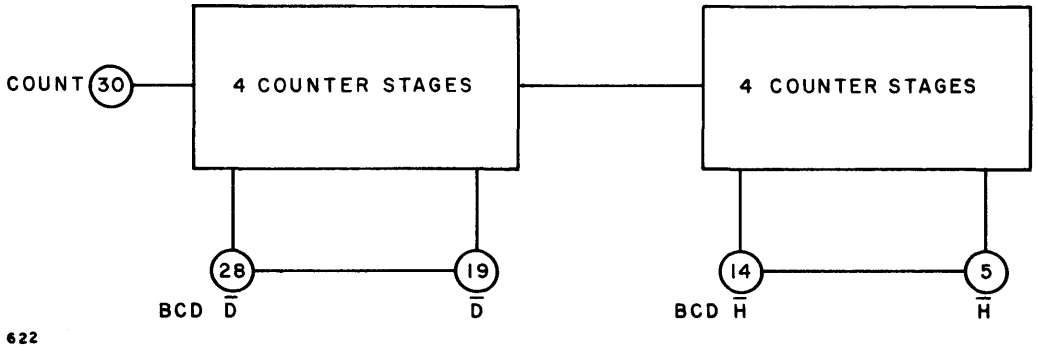
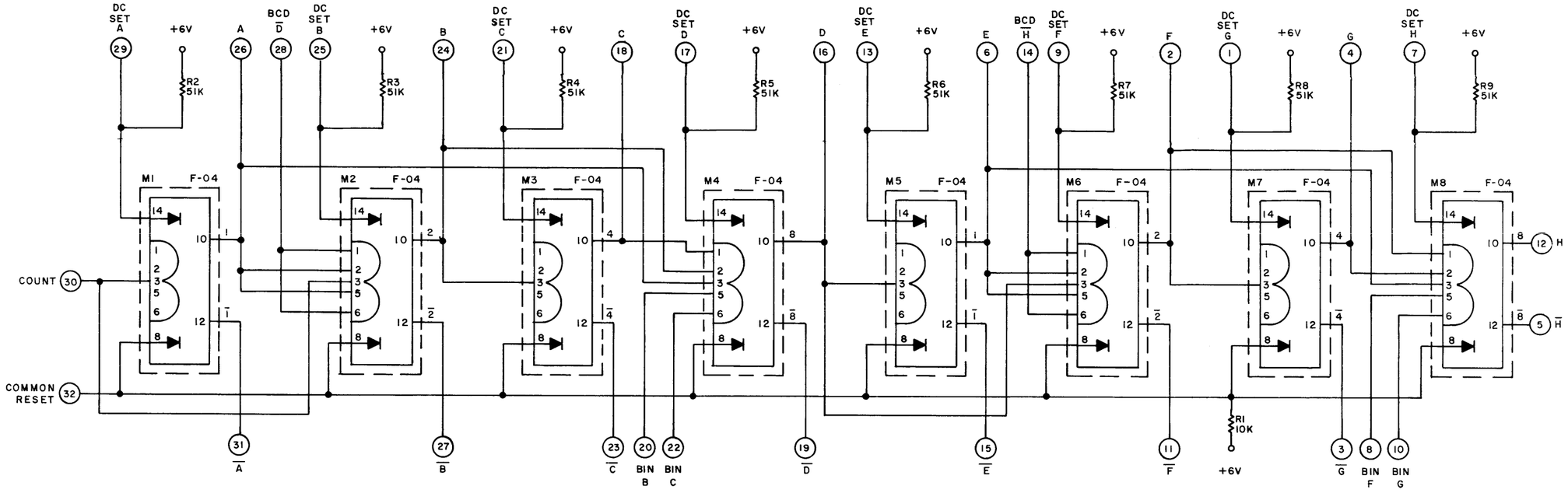


Figure 3-3.4. Fast Carry Counter PAC, Model BC-337, Jumper Connections for BCD Counting



LEGEND

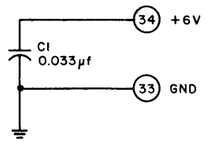
(1) PIN NUMBER OF PAC

2 PIN NUMBER OF MICROCIRCUIT

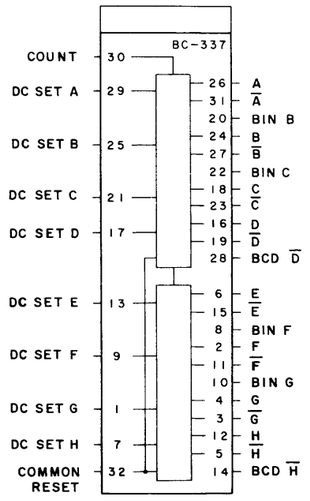
M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

622A



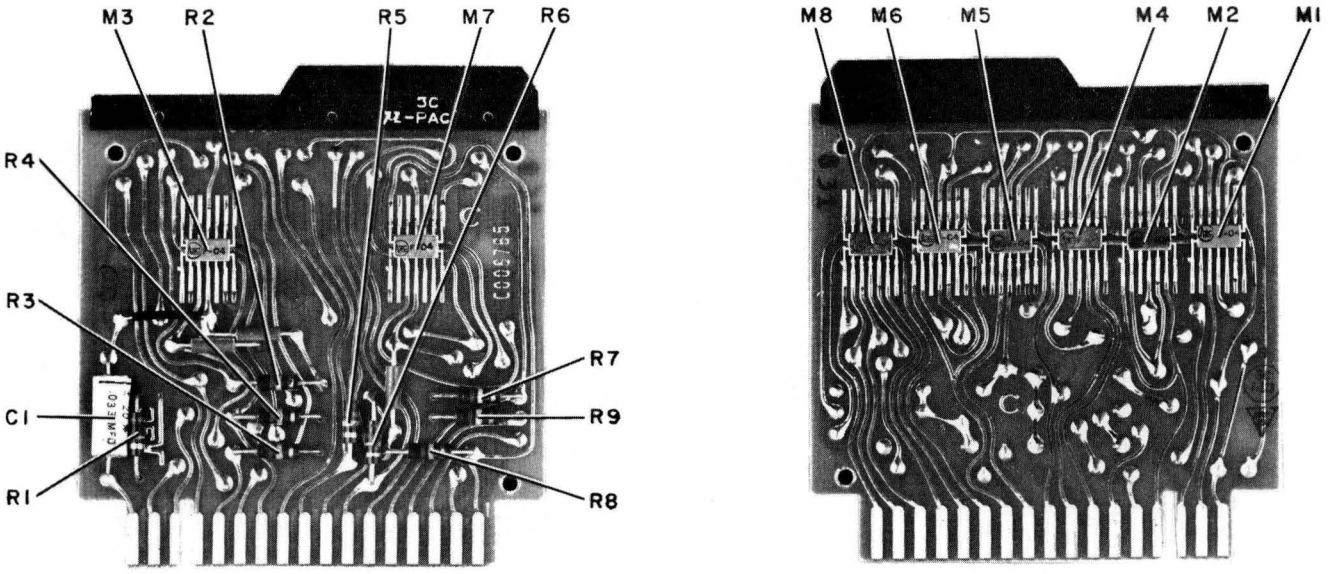
SCHEMATIC



LOGIC SYMBOL

Figure 3-3.1A. Fast Carry Counter PAC, Model BC-337 (Ser. No. 800 and beyond), Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M8	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 10 K ±5%, 1/4 w	932 007 073
R2 - R9	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4w	932 007 090

Figure 3-3.2A. Fast Carry Counter PAC, Model BC-337 (Ser. No. 800 and beyond), Parts Location and Identification

3-4 μ-BLOCS, MODELS BL-330, BL-331, BL-332, and BL-333

Four standard BL-series μ-BLOCs are available for mounting μ-PACs. The μ-BLOCs offer a choice of either solderless-wrap or taper-pin connectors, and are equipped with cooling units. Detachable mounting brackets permit direct installation in a 19-inch relay rack. The mechanical housing for the BL-330 and BL-331 μ-BLOCs accommodates a Model PB-331 Plug-in Power Supply. Table 3-4.1 summarizes the main characteristics of each μ-BLOC.

Table 3-4.1 BL-Series μ-BLOC Characteristics

Model	PAC Capacity	Connector Type	Dimensions (In.)			No. of Connector Assemblies	Housing for Power Supply
			Height	Depth	Width		
BL-330	96	Solderless wrap	12-7/32	5-1/8	16-11/18	12	PB-331
BL-331	48	Taper pin				12	PB-331
BL-332	144	Solderless wrap				18	None
BL-333	72	Taper pin				18	None

MECHANICAL FEATURES

All of the BL-series μ-BLOCs use modular connector assemblies for holding groups of μ-PACs. The solderless-wrap connector assembly is a single piece of molded glass-filled phenolic, capable of holding eight μ-PACs. Solderless-wrap connectors are spaced 1/4 in. apart on centers. The taper-pin connector assembly is a set of four molded plastic connectors spaced 1/2 in. apart on centers. Figure 3-4.1 shows the mechanical arrangement of the BL-330.

Each 34-pin connector slot is polarized to prevent upside-down insertion of μ-PACs. A reliable electrical contact is assured between the gold-plated etched μ-PAC terminal finger and a gold dot welded to the phosphor-bronze connector terminal. Solderless-wrap terminals accept three levels of wrap (three connections); the taper-pin terminal accepts two connections each. An instruction manual (Doc. No. 71-371) on solderless-wrap techniques is available.

The BLOCs feature many mechanical options and mounting flexibility. All of the μ-BLOCs have detachable rack-mounting ears, permitting the wiring side to be mounted facing either the front or the back. The connector plane is removable from the wiring side as a complete assembly. The power supply is also removable from the wiring side. Cooling unit fans are removable from the PAC side. The cooling unit (105-120v at 50/60 cps) is equipped with a washable filter.

ELECTRICAL FEATURES

Power supply voltages are distributed within the BL-series μ-BLOCs by a prewired power distribution system. All PAC connectors are prewired for +6v and ground. Connectors can be wired individually for -6v when required.

The BL-330 and BL-331 contain an integral mechanical housing for mounting the PB-331 Plug-in Power Supply, which can nominally supply all the power required by each configuration. A common ac line cord for the power supply and the cooling unit extends from the cooling unit housing on the PAC side. Filtering of power supply voltages in these BLOCs is accomplished mainly by local filtering on each PAC.

The BL-332 and BL-333 μ-BLOCs have provision for obtaining power supply voltages from an external power supply such as the RP-330. Filtering of the power supply voltage input leads on the BL-332 μ-BLOC is accomplished by a decoupling module (3C Part No. B011516702) that contains two 15-microfarad capacitors. The module is located between the top and middle solderless-wrap connector assemblies of the left-hand row as viewed from the wiring side. When the user deems necessary, additional decoupling modules may be utilized on the BL-330 and BL-332 by temporarily removing the appropriate PAC guides and inserting the module into the molded spacer. When viewed from the wiring side, the left hand pin of the module is for -6v, the center pin is for ground, and the right hand pin is for +6v.

Filtering of the power supply voltage input leads on the BL-333 μ-BLOC is accomplished by 15-microfarad capacitors mounted adjacent to the power supply input terminals on the connector plane. If it is necessary to provide additional filtering on the connector plane, capacitors should be connected between the appropriate PAC terminal and any convenient ground terminal.

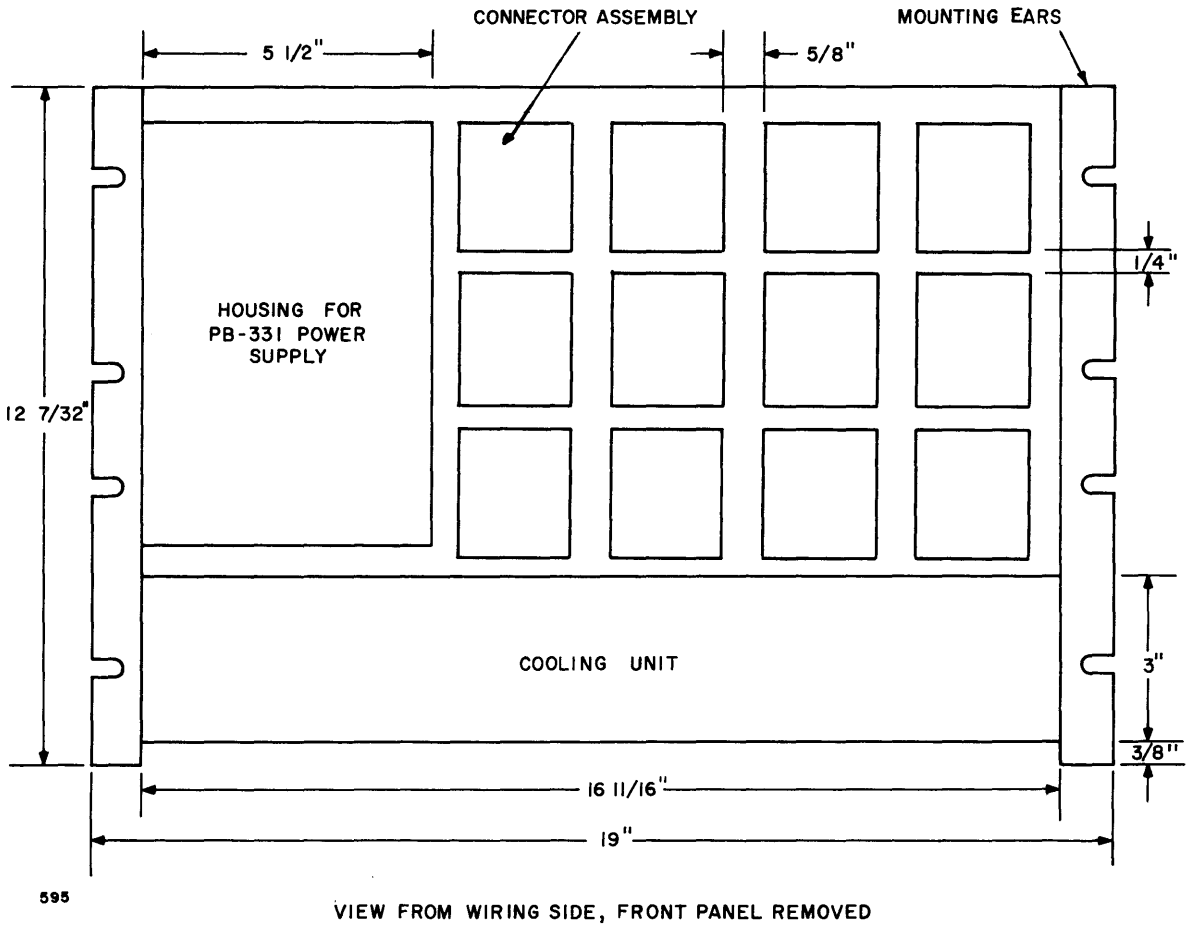


Figure 3-4.1. Mechanical Arrangement of BL-330

3-5 μ-BLOCS, MODELS BM-330, BM-335, and BM-337

Three standard BM-series μ-BLOCs are available for mounting μ-PACs in custom housings or, with optional adapter panels, in standard 19-inch relay racks. The BLOCs offer a choice of either solderless-wrap or taper-pin connectors, and are equipped with cooling units. The mechanical housing for the BM-330 and BM-335 μ-BLOCs accepts a Model PB-330 Plug-in Power Supply. Table 3-5.1 summarizes the main characteristics of the BM-series μ-BLOCs.

Table 3-5.1 BM-Series μ-BLOC Characteristics

Model	PAC Capacity	Connector Type	Dimensions (In.)			No. of Connector Assemblies	Housing for Power Supply
			Height	Depth	Width		
BM-330	24	Solderless wrap	12-7/32	5-1/8	5-11/16	3	PB-330
BM-335	24	Taper pin	12-7/32	5-1/8	8-7/16	6	PB-330
BM-337	36	Taper pin	12-7/32	5-1/8	8-7/16	9	None

MECHANICAL FEATURES

All of the BM-series μ-BLOCs use modular connector assemblies for holding groups of μ-PACs. The solderless-wrap connector assembly is a single piece of molded glass-filled phenolic capable of holding eight μ-PACs. Solderless-wrap connectors are spaced 1/4 in. apart on centers. The taper-pin connector assembly is a set of four molded plastic μ-PAC connectors spaced 1/2 in. apart on centers. The BM-series μ-BLOCs are constructed so that connector assemblies are arranged in vertical columns of three. Figure 3-5.1 shows the mechanical arrangement of the BM-337 from the wiring side, front panel removed. The other side is the PAC side.

Each 34-pin connector slot is polarized to prevent upside-down insertion of a μ-PAC. A gold dot welded to each phosphor-bronze connector terminal mates with the gold-plated, etched μ-PAC contact finger for reliable electrical interconnection. Solderless-wrap terminals can accept three levels of wrap (three connections), while taper-pin terminals accept two connections each. An instruction manual (Doc. No. 71-371) on solderless-wrap techniques is available.

The BLOCs feature many mechanical options and mounting flexibility. Detachable rack-mounting ears permit the wiring side to be mounted facing either the front or the back. The connector plane is removable from the wiring side as a complete assembly. The PB-330 power supply is also removable from the wiring side. Cooling unit fans are removable from the PAC side. The cooling unit (105-120v at 50/60 cps) is equipped with a washable filter.

All BM-series BLOCs have a quick-release front panel covering the μ-PAC connectors and the power supply housing.

ELECTRICAL FEATURES

Power supply voltages are distributed within BM-series μ-BLOCs by a prewired distribution system. All PAC connectors are prewired for +6v and ground. Connectors can be wired individually for -6v when required.

The BM-330 and BM-335 μ-BLOCs contain an integral mechanical housing for mounting the PB-330 Plug-in Power Supply, which can nominally supply all the power required by each configuration. A common ac line cord for the power supply and the cooling unit extends from the cooling unit housing on the PAC side. Filtering of power supply voltages in these μ-BLOCs is accomplished mainly by local filtering on each PAC.

The BM-337 has provision for obtaining power supply voltages from an external power supply such as the RP-330. Filtering of the power supply voltage input leads is accomplished by 15-microfarad capacitors mounted adjacent to the power supply input terminals on the connector plane. If the user deems it necessary to provide additional filtering on the connector plane, capacitors should be connected between the appropriate PAC terminal and any convenient ground terminal.

Additional filtering of the power supply voltages is also possible on the BM-330 and BM-335 BLOCs. Additional decoupling capacitors may be added to the BM-335 in the same manner as indicated for the BM-337.

On the BM-330 additional decoupling may be utilized by temporarily removing the appropriate PAC guide and inserting a decoupling module (3C Part No. B011516702) into the molded spacer beneath the solderless-wrap connector. When viewed from the wiring side, the left-hand pin of the decoupling module is for -6v, the center pin for ground, and the right-hand pin is for +6v.

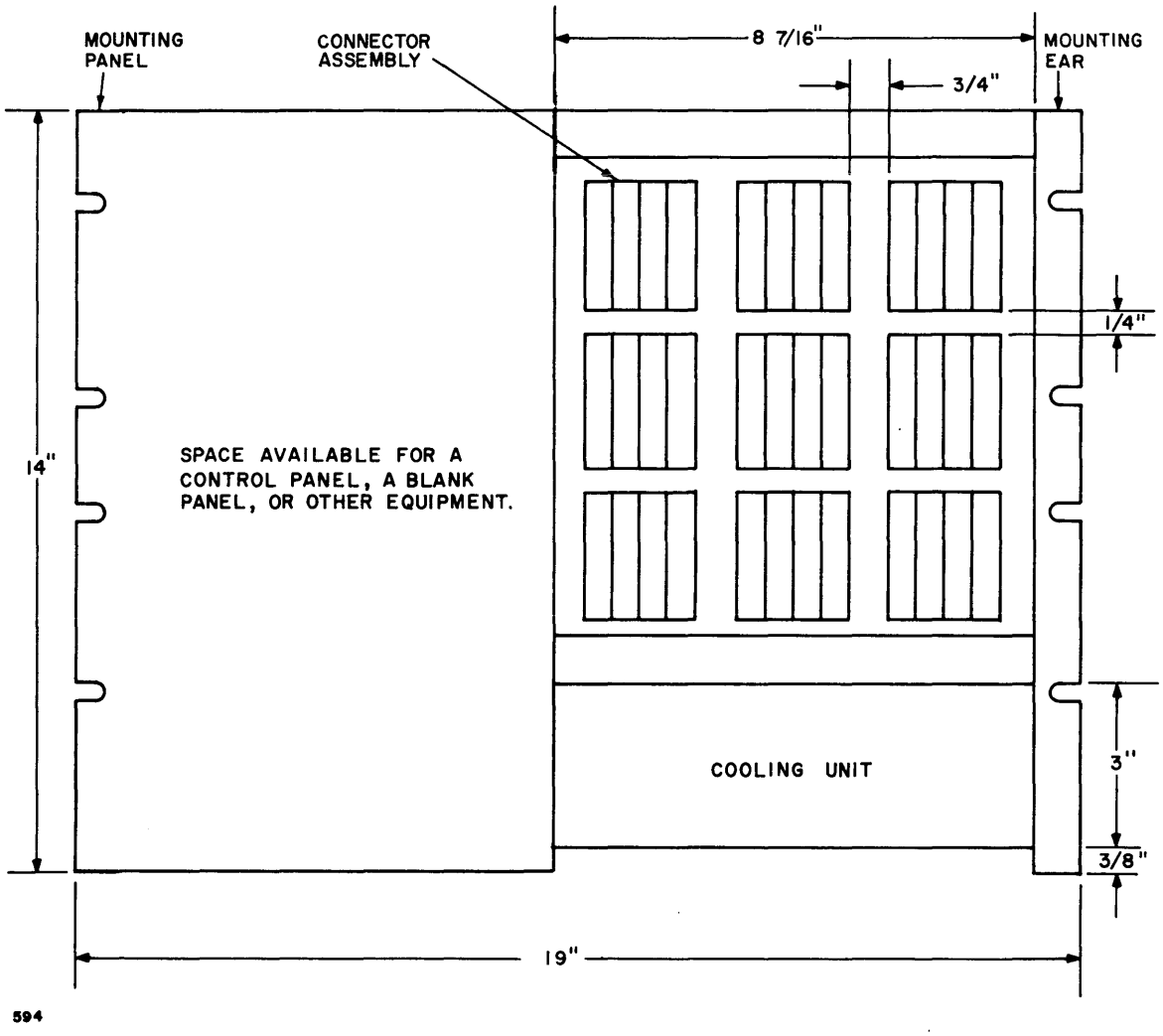
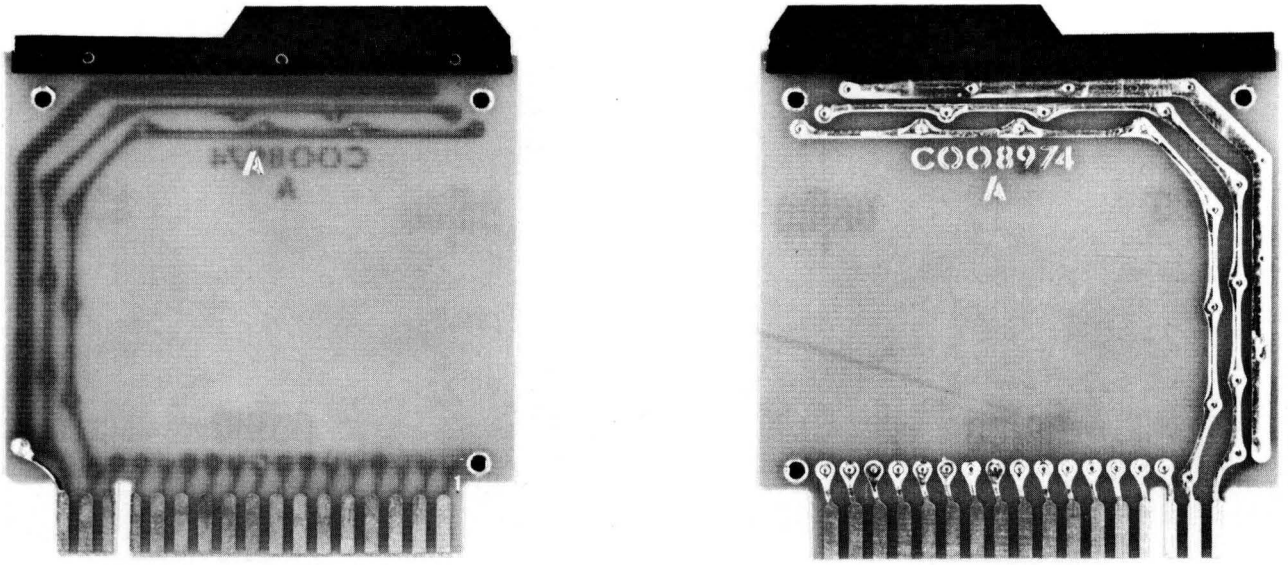


Figure 3-5.1. μ-BLOC, Model BM-337, with Adapter Panel

3-5A BLANK PAC, MODEL BP-330

The Blank PAC, Model BP-330 (Figure 3-5A.1), is a standard μ-PAC card with etched power and ground buses stemming from the appropriate connector terminals about its periphery. Most of the card is blank to facilitate the mounting of any special circuits or components using standard lugs and point-to-point wiring. Fifteen connector terminals are provided for circuit input and output connections. The usable area is approximately 3.5 sq in.

The maximum allowable height of components on the BP-330 when the PAC is mounted in a solderless-wrap μ-BLOC is 0.115 in. on the component side and 0.080 in. on the etch side. For a taper-pin μ-BLOC, the maximum heights are 0.36 in. and 0.32 in. However, if the adjacent PAC slots of the BLOC are left vacant, any component height can be attained.



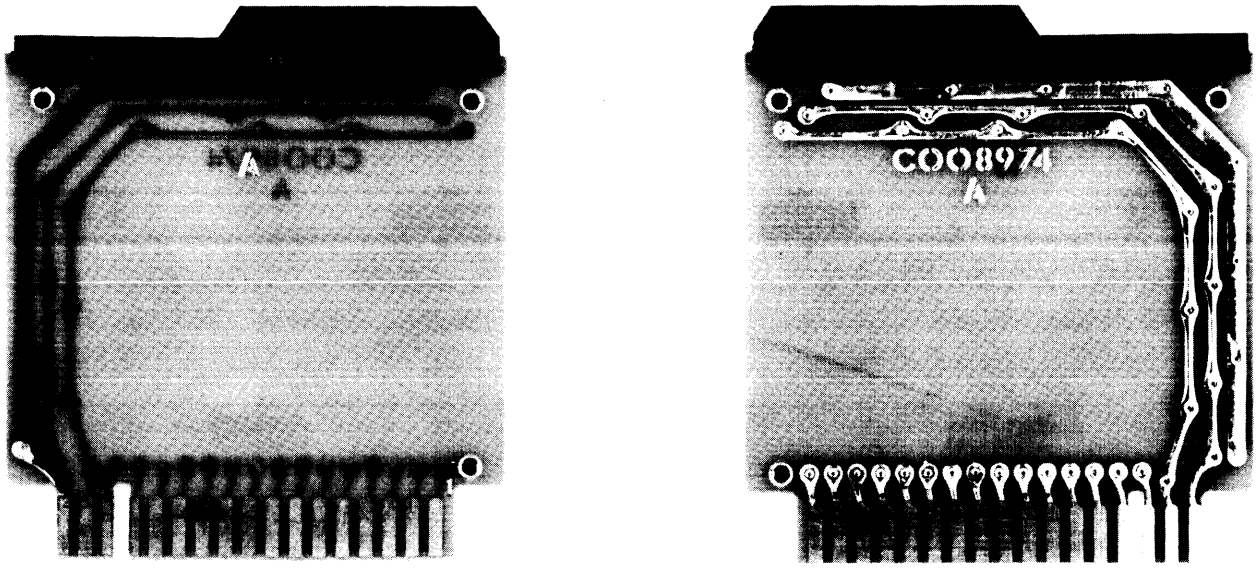
768

Figure 3-5A.1. Blank PAC, Model BP-330

3-5A BLANK PAC, MODEL BP-330

The Blank PAC, Model BP-330 (Figure 3-5A.1), is a standard μ-PAC card with etched power and ground buses stemming from the appropriate connector terminals about its periphery. Most of the card is blank to facilitate the mounting of any special circuits or components using standard lugs and point-to-point wiring. Fifteen connector terminals are provided for circuit input and output connections. The usable area is approximately 3.5 sq in.

The maximum allowable height of components on the BP-330 when the PAC is mounted in a solderless-wrap μ-BLOC is 0.115 in. on the component side and 0.080 in. on the etch side. For a taper-pin μ-BLOC, the maximum heights are 0.36 in. and 0.32 in. However, if the adjacent PAC slots of the BLOC are left vacant, any component height can be attained.



768

Figure 3-5A.1. Blank PAC, Model BP-330

Parts Location

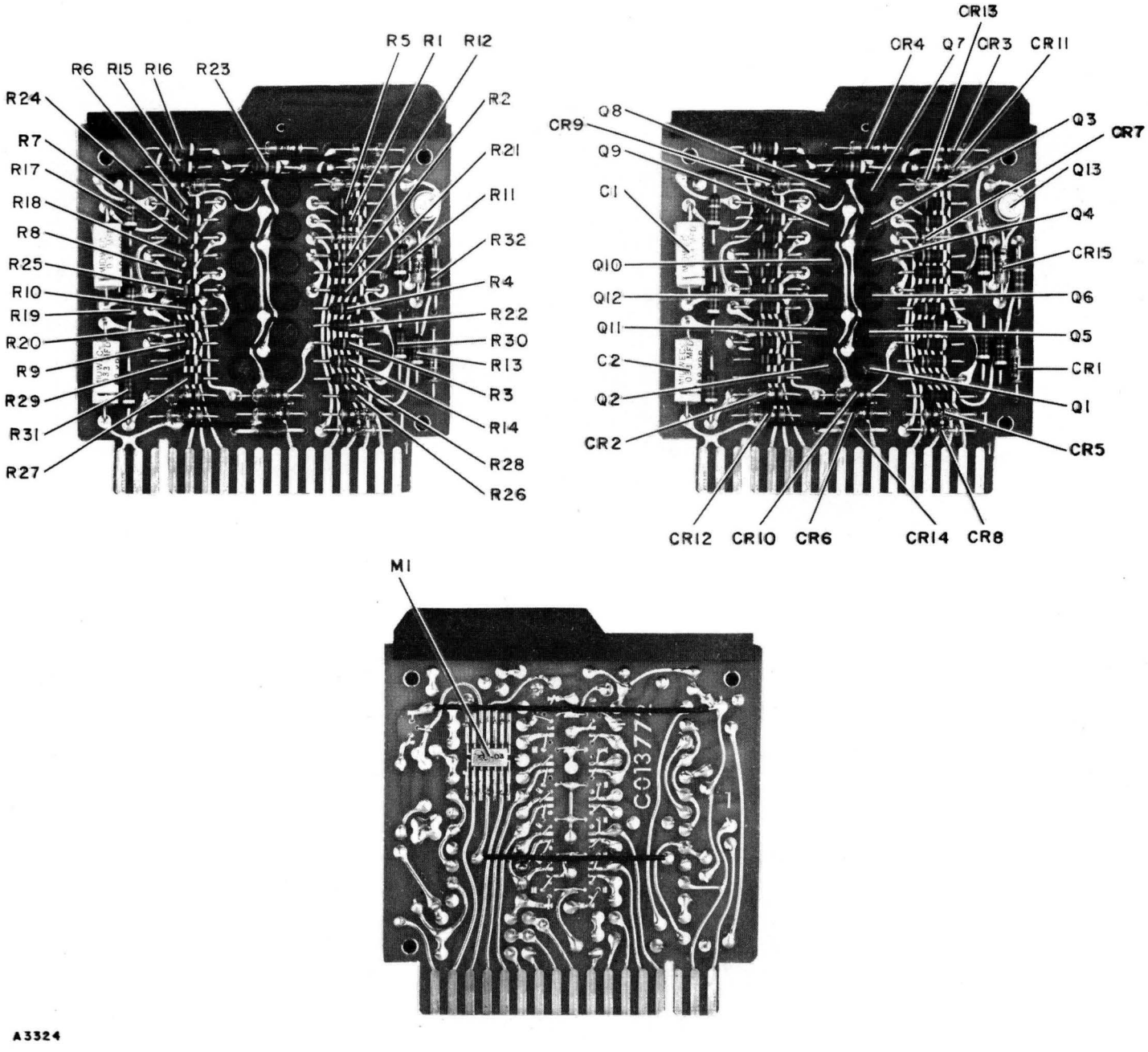


Figure 3-7A. 2. Display Driver PAC, Model DD-330,
Parts Location and Identification
(Sheet 1 of 2)

3-6 BUFFER REGISTER PAC, MODEL BR-335

The Buffer Register PAC, Model BR-335 (Figures 3-6.1 and 3-6.2), contains six flip-flops. Common clock and common reset inputs make simultaneous operations possible on all stages. Typical uses include shifting, accumulating, and clocked parallel transfer.

A detailed description of the basic flip-flop circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

DC Set. -- A signal at logic ZERO for 80 nsec or longer on dc set input will set the flip-flop.

Set Control and Reset Control. -- Logic ONE (+6v) is the enabling level on the control inputs. Refer to Section II for general information on flip-flop timing and control.

Common Clock. -- The flip-flops change state on the negative (ONE to ZERO) transition of the clock input.

Common Reset. -- A signal at logic ZERO for 80 nsec or longer on the common reset input clears all the six stages simultaneously.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC set:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	4 unit loads
Common clock:	6 unit loads

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output: 60 nsec (max)

DC set input to set output, or common reset input to reset output: 80 nsec (max)

DC set input to reset output, or common reset input to set output: 60 nsec (max)

Current Requirements

+6v: 150 ma (max)

Power Dissipation

0.90w (max)

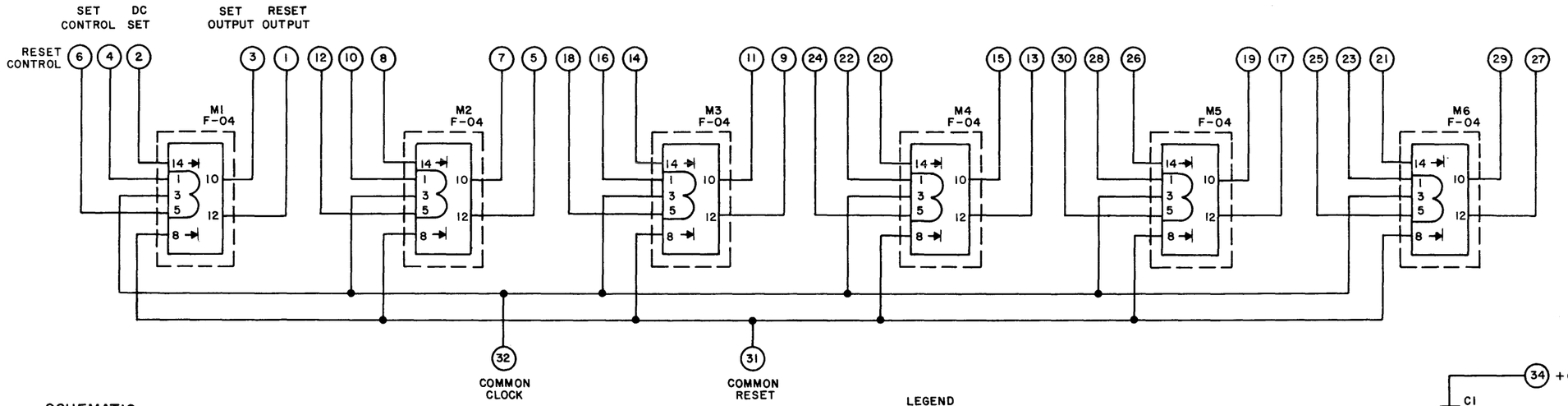
Handle Color Code

Blue

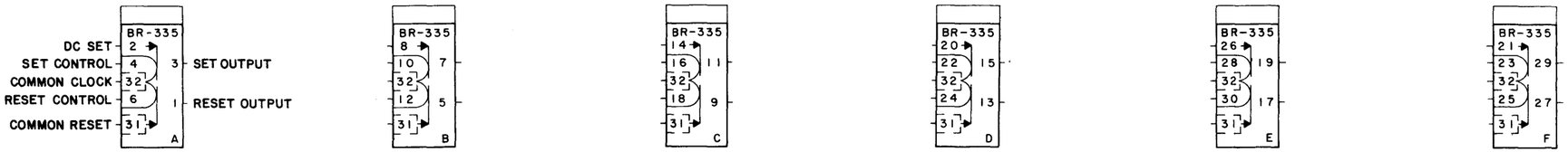
APPLICATIONS

The BR-335 can be used as a shift register in the configuration of Figure 3-6.3. The method of parallel information drop-in is shown in Figure 3-6.4.

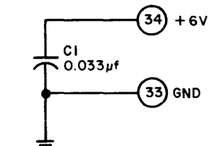
For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation. Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones.



SCHEMATIC



LOGIC SYMBOL



LEGEND

(1) PIN NUMBER OF PAC

-|2|- PIN NUMBER OF MICROCIRCUIT

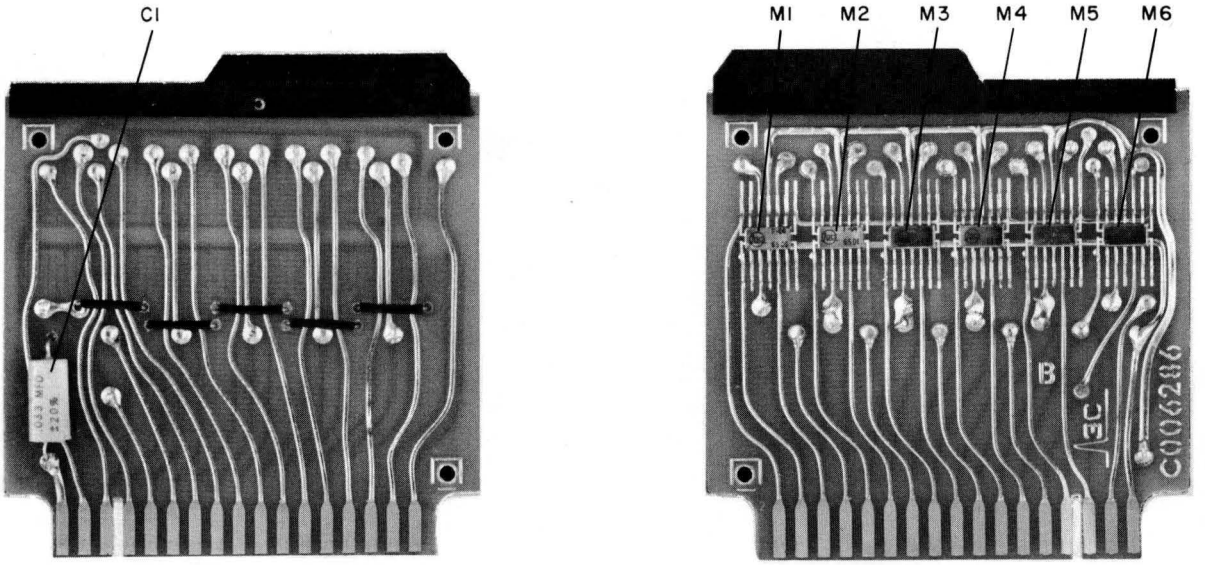
M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

Note: Refer to Figure 3-6.1A for PACs with Ser. No. 1186 and beyond.

Figure 3-6.1. Buffer Register PAC, Model BR-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

| Note: Refer to Figure 3-6.2A for PACs with Ser. No. 1186 and beyond.

Figure 3-6.2. Buffer Register PAC, Model BR-335, Parts Location and Identification

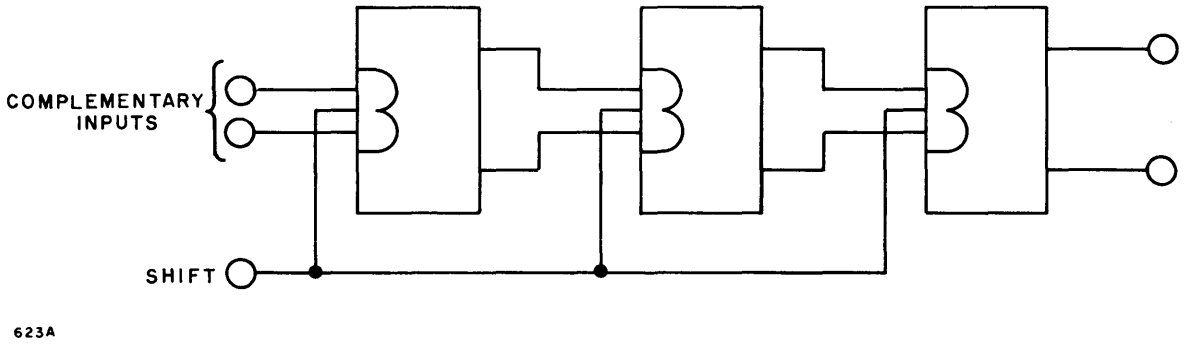


Figure 3-6. 3. Buffer Register PAC, Model BR-335,
Shift Register Operation

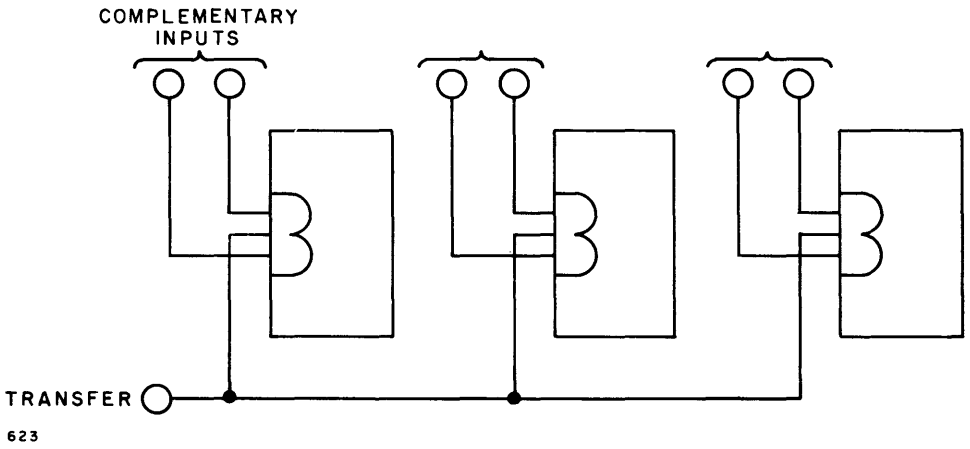
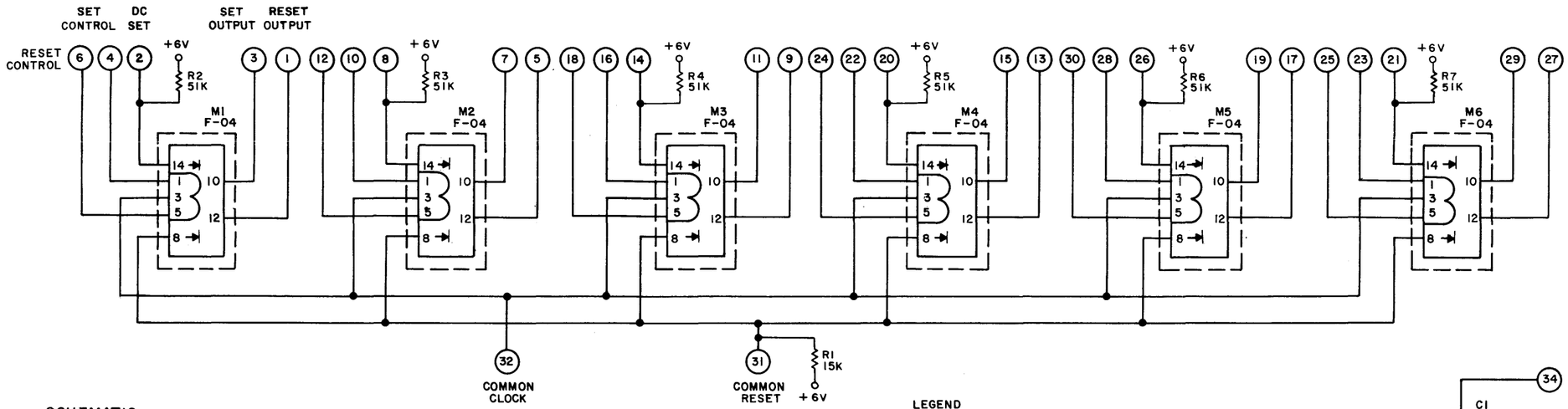


Figure 3-6. 4. Buffer Register PAC, Model BR-335,
Parallel Information Drop-In



SCHEMATIC

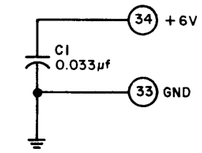
LEGEND

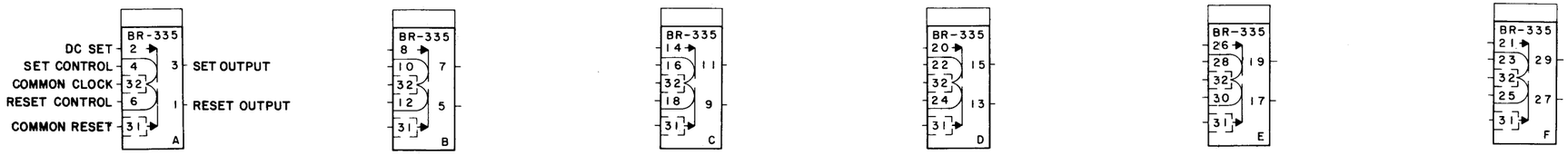
(1) PIN NUMBER OF PAC

2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT



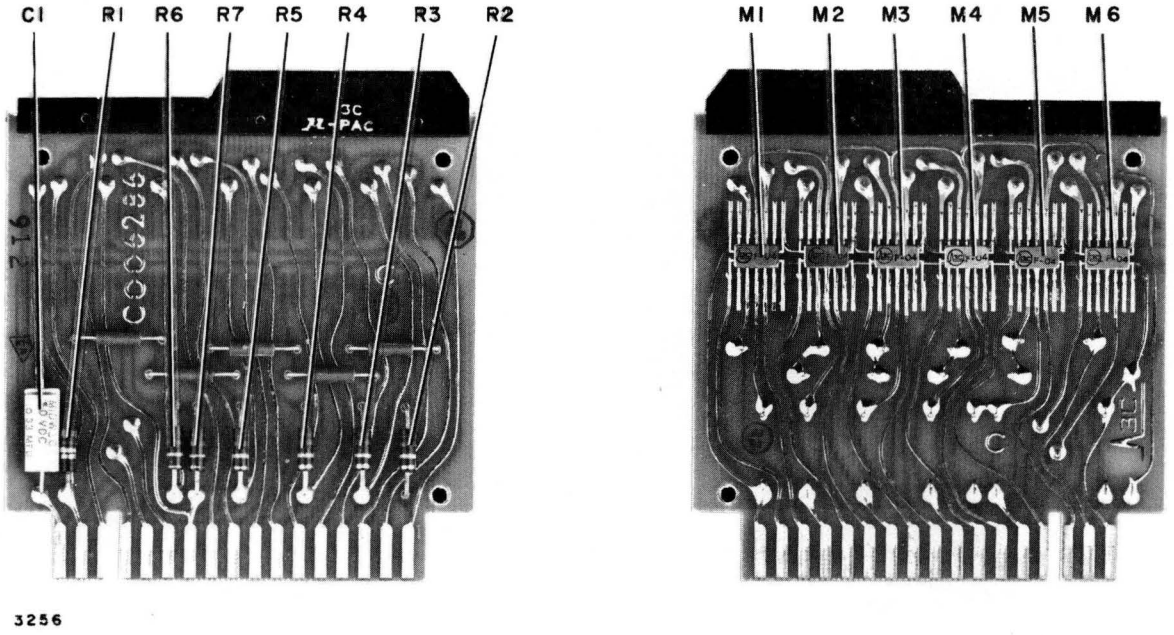


LOGIC SYMBOL

488A

Figure 3-6.1A. Buffer Register PAC, Model BR-335 (Ser. No. 1186 and beyond), Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M6	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 15 K ±5%, 1/4w	932 007 077
R2 - R7	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4w	932 007 090

Figure 3-6.2A. Buffer Register PAC, Model BR-335 (Ser. No. 1186 and beyond), Parts Location and Identification

3-7 MULTI-INPUT NAND PAC, MODEL DC-335

The Multi-Input NAND PAC, Model DC-335 (Figures 3-7. 1 and 3-7. 2), contains two 6-input NAND gates with nodes, and four 3-diode clusters. The diode cluster nodes can be connected to the gate nodes of this or other PACs to expand the number of gate inputs (Figure 3-7. 3). A detailed description of the NAND gate appears in Section II.

INPUT AND OUTPUT SIGNALS

Gate Node.--This point may be connected to diode cluster nodes to expand the number of logic inputs. The connecting wire between nodes should not be cabled, and should have a maximum lead length of 3 in.

Gate Inputs. --Each gate performs the NAND function for positive logic (+6v = ONE, 0v = ZERO). For negative logic, it becomes a NOR gate. When all inputs to a gate are at +6v or not connected, the output is ground. When any input is at ground, the output is +6v.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Fan-In

Refer to Section II.

Output Drive Capability

8 unit loads each

Circuit Delay

(Measured at +1. 5v, averaged over two stages)

33 nsec (max)*

Current Requirements

+6v: 25 ma (max)

Power Dissipation

0. 150w (max)

Handle Color Code

Red

APPLICATIONS

Two NAND gates can be cross-coupled to form a dc set-reset flip-flop.

The diode clusters, which are composed of discrete components, can be used to expand the number of gate inputs as shown in Figure 3-7. 3.

The dc-coupled gates operate on levels, pulses, or combinations of both.

*30 nsec for gate plus 3 nsec for diode cluster

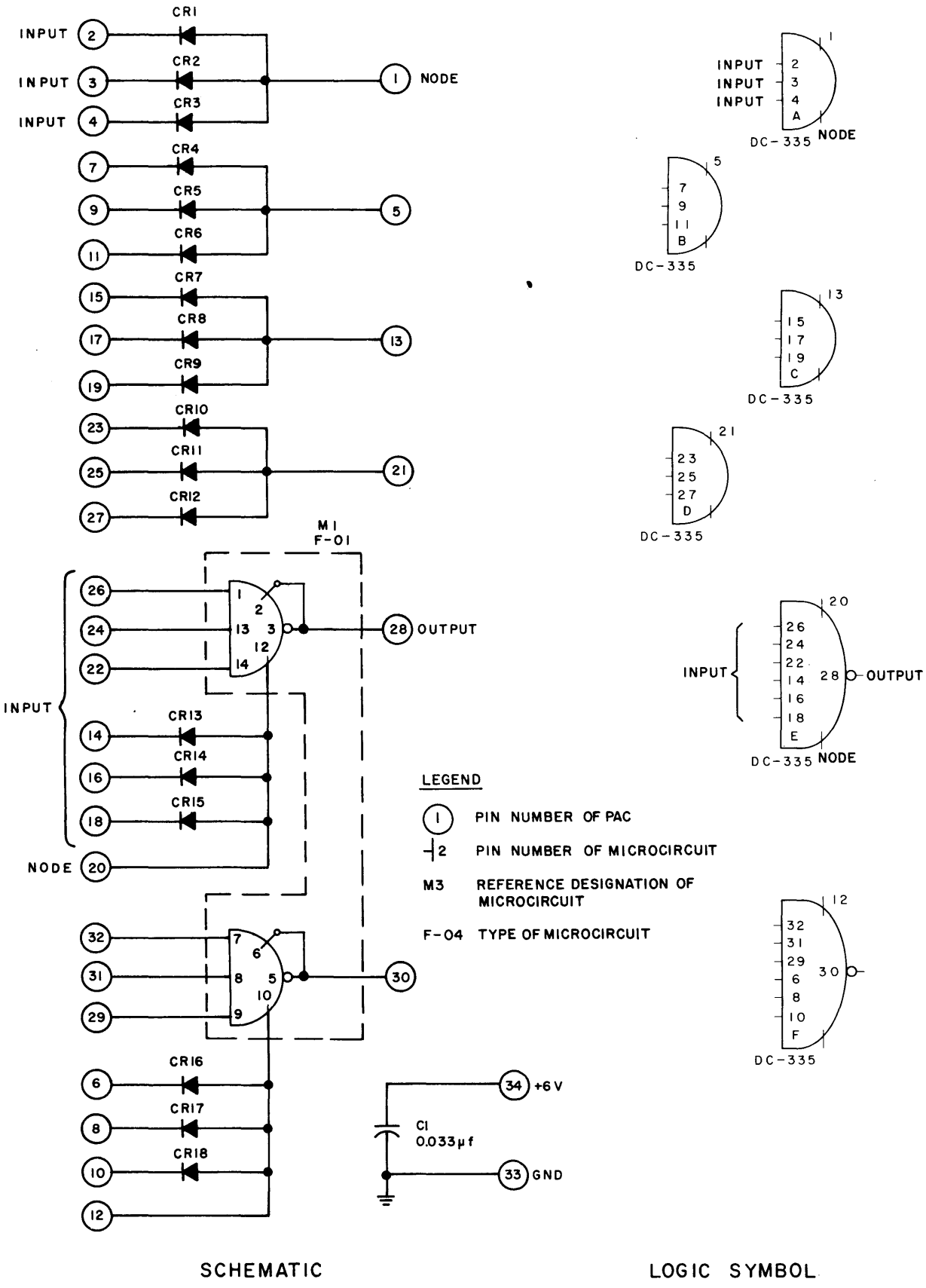
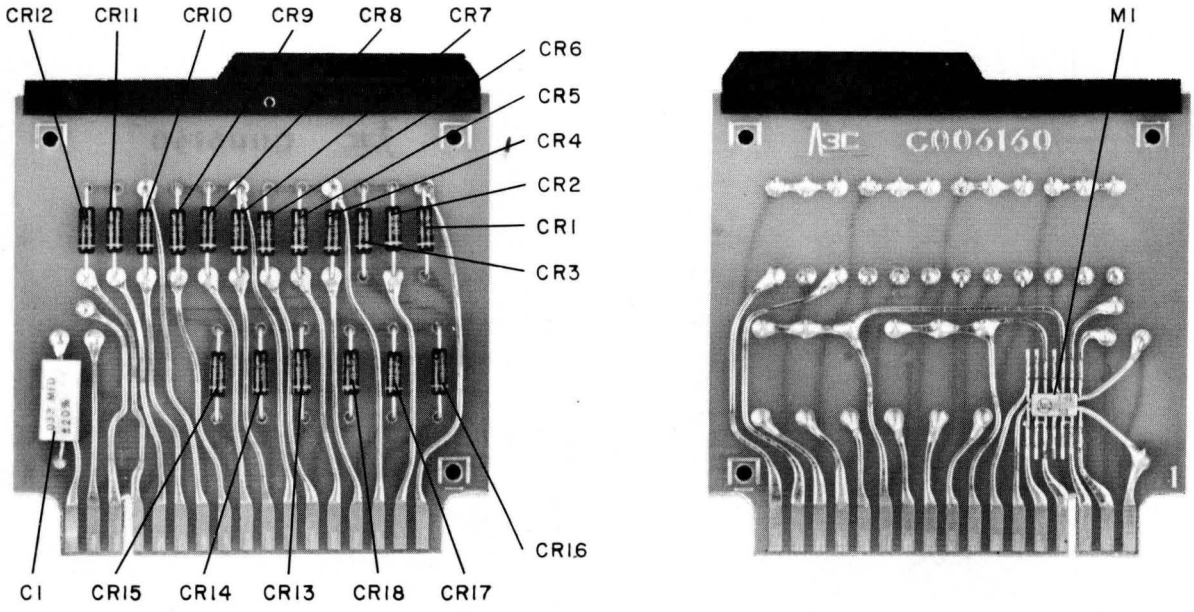


Figure 3-7.1. Multi-Input NAND PAC, Model DC-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR18	DIODE: Replacement Type 1N914	943 083 001

Figure 3-7.2. Multi-Input NAND PAC, Model DC-335, Parts Location and Identification

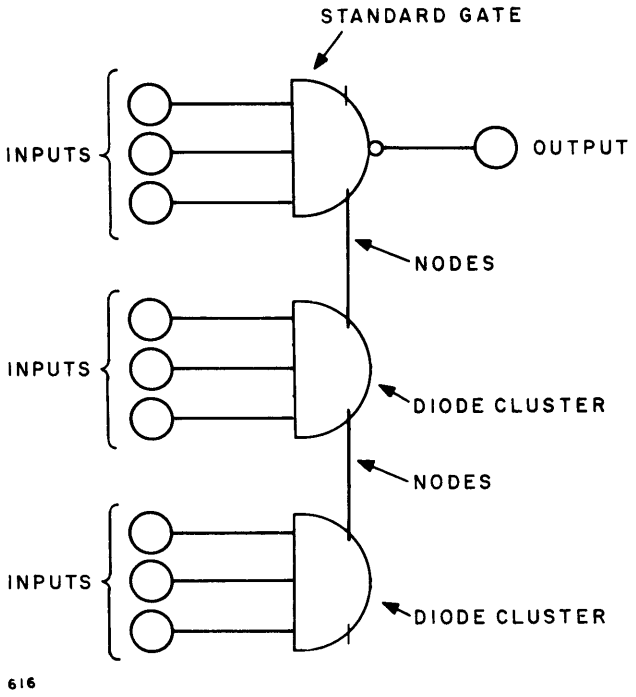


Figure 3-7.3. Multi-Input NAND PAC, Model DC-335, Expansion of Gate Inputs

3-7A DISPLAY DRIVER PAC, MODEL DD-330

The Display Driver PAC, Model DD-330 (Figures 3-7A. 1 and 3-7A. 2), is designed to decode a four-bit, binary-coded-decimal (BCD) input, store the result, and drive a projection-type digital display device. The BCD input information is applied to the PAC, decoded, and then strobed. The result is stored and retained until a clear signal is applied.

The circuit is designed around a silicon-controlled switch (SCS) which provides both storage and power amplification.

The use of an ac supply voltage for the incandescent lamps of the display unit is essential for the proper operation of the circuit, since resetting of the SCS is accomplished during the negative half-cycle of this supply voltage.

INPUT AND OUTPUT SIGNALS

BCD Data Input. -- The DD-330 uses biquinary diode gating to select one of the ten output SCSs in accordance with BCD input data. Both polarities of the BCD inputs, set and reset, are required. The decoding is accomplished as follows: The least significant bit is the binary portion and the remaining three bits are the quinary portion. The quinary portion selects one of five pairs of adjacent odd and even numbers, and the binary portion controls odd (Q2) or even (Q1) selection.

Output. -- There are ten identical output circuits each associated with one of the decimal numbers, 0 through 9. An SCS and its associated number is turned on when its control gate is positive from the quinary gate structure, its cathode has a path to ground through a binary control SCS (Q1 or Q2), and the strobe signal is activated.

The anode of each SCS is connected to its associated lamp filament. The common side of the lamp filaments is connected to pin 14 of the PAC. The ac supply voltage is connected between pins 31 (ground) and 20 and reaches the lamp common through a single diode. This diode acts as a half-wave rectifier when any SCS is on. The voltage of the ac supply depends upon the requirements of the display device. Equation 1 is used to calculate the specific requirement.

$$V_S \leq 2\ V_L + 2 \text{ volts} \qquad (1)$$

where V_S is the supply voltage needed and V_L is the rated lamp voltage.

Clear Input. -- The clear circuit controls the holding current of the conducting SCSs during the negative half-cycle of the ac supply voltage. The circuit includes an F-03 power amplifier to minimize input signal requirements. The clear input is active at +6v and inactive at 0v. When the clear signal is not synchronized (externally) with the ac lamp supply voltage, it must be active for 10 milliseconds (min). If it is synchronized, the clear signal need only be active for a minimum of 25 microseconds.

Strobe Input. -- The strobe circuit controls the current for the decoding gate structure and includes an F-03 power amplifier to minimize input signal requirements. The strobe signal is active at 0v and inactive at +6v.

SPECIFICATIONS

Input Loading

BCD data: 1 unit load each

Strobe signal: 2 unit loads

Clear signal: 2 unit loads

Signal Requirements

	Active	Inactive
BCD data:	+6v	0v
Clear signal:	+6v (10 msec) +6v (25 μsec)	0v (not synchronous) 0v (synchronous)
Strobe signal:	0v (2 μsec)	

AC Supply Requirements	Current Requirements
(Refer to equation 1.)	+6v: 45 ma
	-6v: 2 ma

Handle Color Code	Power Dissipation
Orange	0.3w

NOTE

This PAC occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

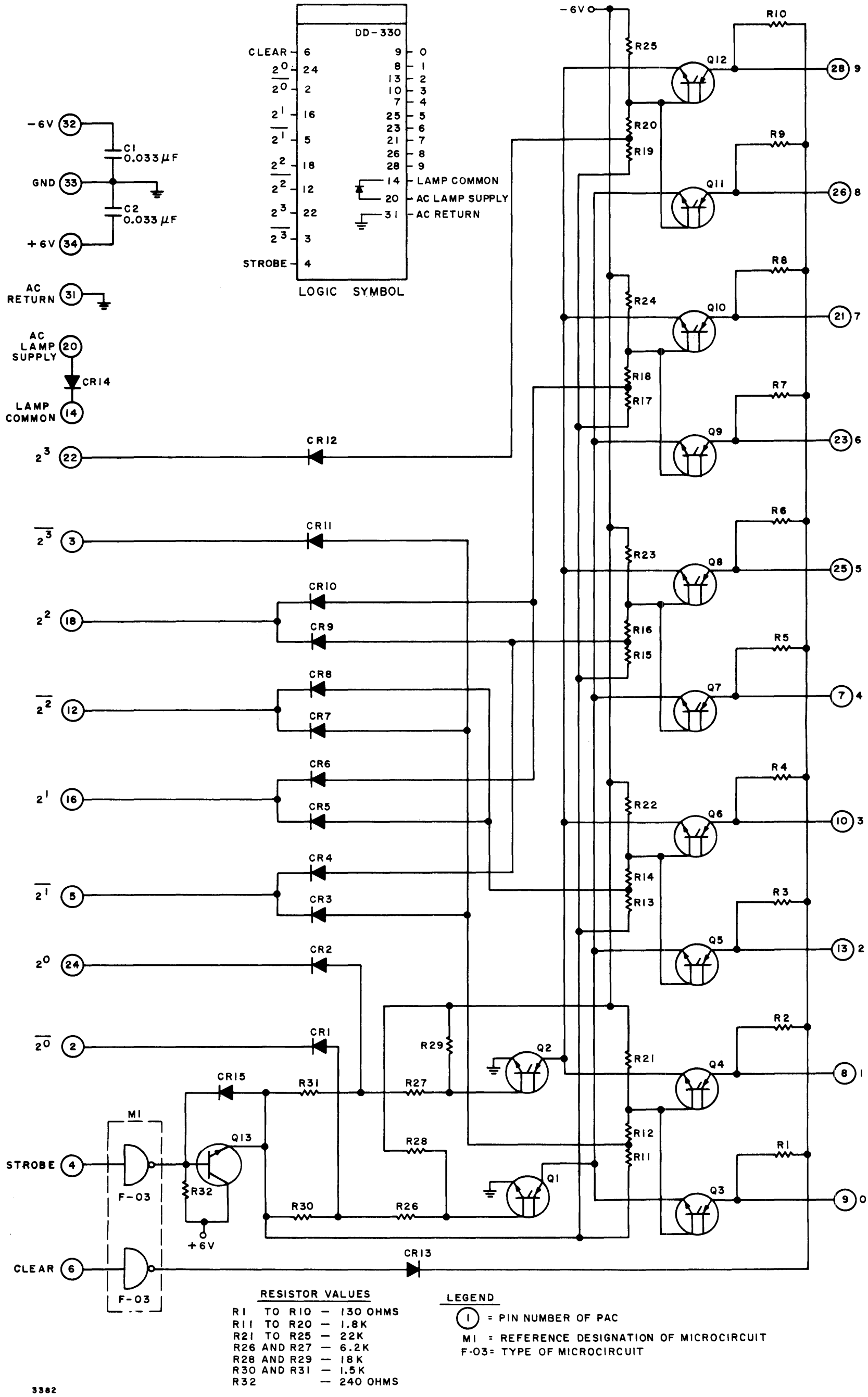


Figure 3-7A.1. Display Driver PAC, Model DD-330, Schematic Diagram and Logic Symbol

Parts Location

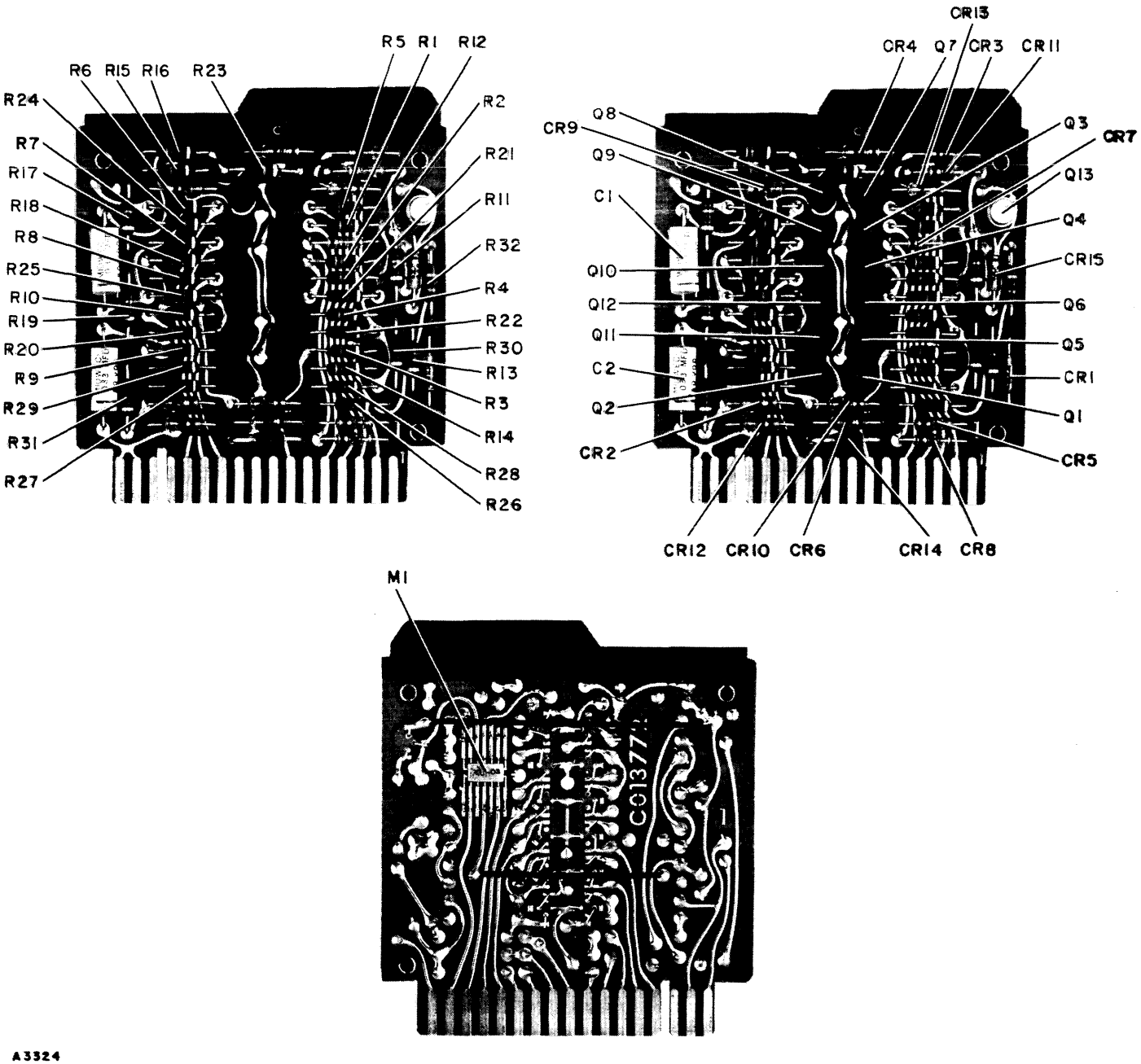


Figure 3-7A. 2. Display Driver PAC, Model DD-330,
Parts Location and Identification
(Sheet 1 of 2)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1 - 13,15	DIODE: Replacement Type 1N914	943 083 001
CR14	DIODE: Replacement Type 1N4001	943 313 001
Q1 - Q12	SILICON CONTROLLED SWITCH: Replacement Type 3N81 General Electric	943 404 001
Q13	TRANSISTOR: Replacement Type 2N3011	943 722 002
R1 - R10	RESISTOR, FIXED, COMPOSITION: 130 ohms ±5%, 1/4w	932 007 028
R11 - R20	RESISTOR, FIXED, FILM: 1.8 K ±2%, 1/4w	932 114 055
R21 - R25	RESISTOR, FIXED, FILM: 22 K ±2%, 1/4w	932 114 081
R26, R27	RESISTOR, FIXED, FILM: 6.2 K ±2%, 1/4w	932 114 068
R28, R29	RESISTOR, FIXED, FILM: 18 K ±2%, 1/4w	932 114 079
R30, R31	RESISTOR, FIXED, FILM: 1.5 K ±2%, 1/4w	932 114 053
R32	RESISTOR, FIXED, FILM: 240 ohms ±2%, 1/4w	932 114 034

Figure 3-7A.2. Display Driver PAC, Model DD-330, Parts Location and Identification (Sheet 2 of 2)

3-8 SELECTION GATE TYPE 1 PAC, MODEL DG-335

The Selection Gate Type 1 PAC, Model DG-335 (Figures 3-8.1 and 3-8.2), contains four independent functional gate structures. Each structure has three 2-input NAND gates that perform the AND-OR-INVERT function. Gate structures may be connected to a common load for transfer selection of up to 12 data signals. The data when transferred is inverted in polarity. Refer to Section II for a detailed description of the basic μ-PAC NAND gate.

INPUT AND OUTPUT SIGNALS

Inputs. -- When all inputs to one NAND gate are at logic ONE (+6v) the collector output is at ground.

Load. -- This point is internally connected through a collector load resistor to +6v. One load must be connected to each group of gates with common collector outputs.

Collector Output. -- The collector output of every active gate structure must be connected to its own load, to the collector output of another loaded gate structure, or to a standard gate output.

SPECIFICATIONS

Frequency of Operation (System)	Circuit Delay
DC to 5 mc	(Measured at +1.5v, averaged over two stages)
Input Loading	30 nsec (max)
1 unit load each	Current Requirements
Output Drive Capability	+6v: 100 ma (max)
8 unit loads per output line	Power Dissipation
Outputs in Parallel	0.60w (max)
Refer to Section II.	Handle Color Code
	Red

APPLICATIONS

Logical operation of one gate structure used for selective transfer of three input signals is shown in Figure 3-8.3. By tying collector outputs together, with a common load termination, up to 12 input lines may be gated to a common output. (See Figure 3-8.4.) Only one gate per group should be enabled during a transfer interval.

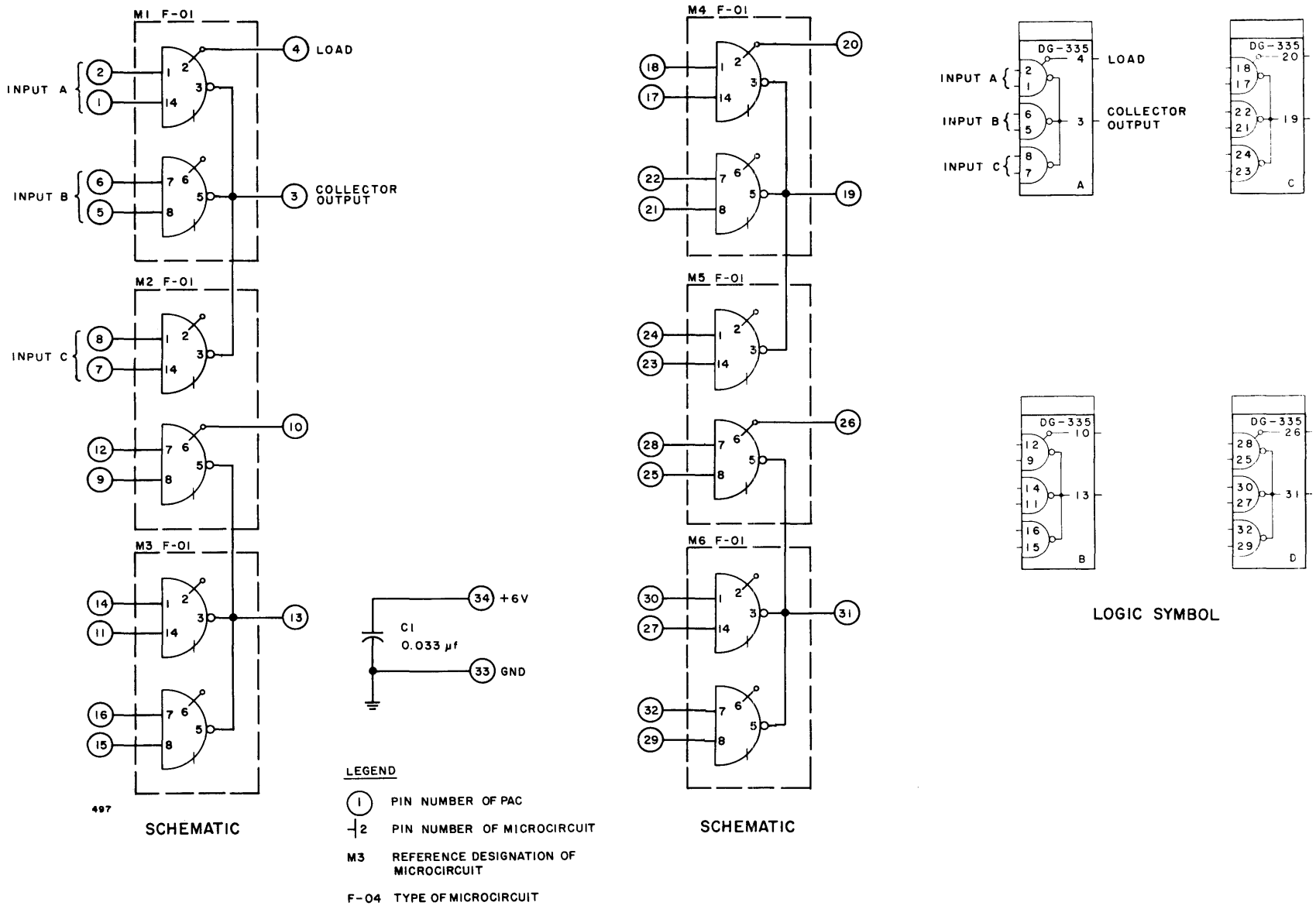
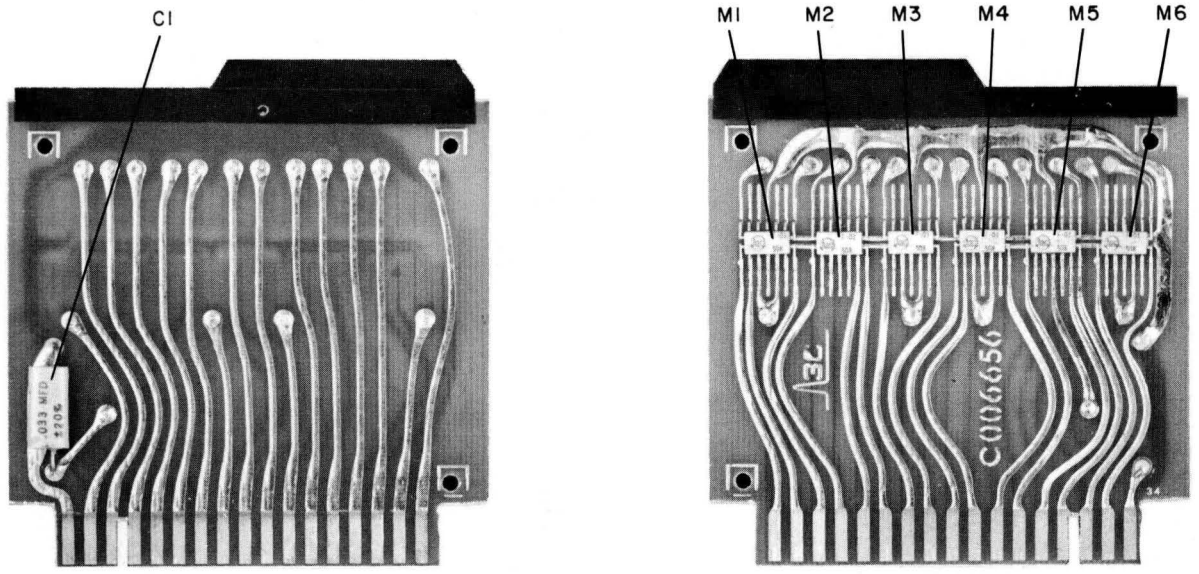


Figure 3-8.1. Selection Gate Type 1 PAC, Model DG-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M6	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-8.2. Selection Gate Type 1 PAC, Model DG-335, Parts Location and Identification

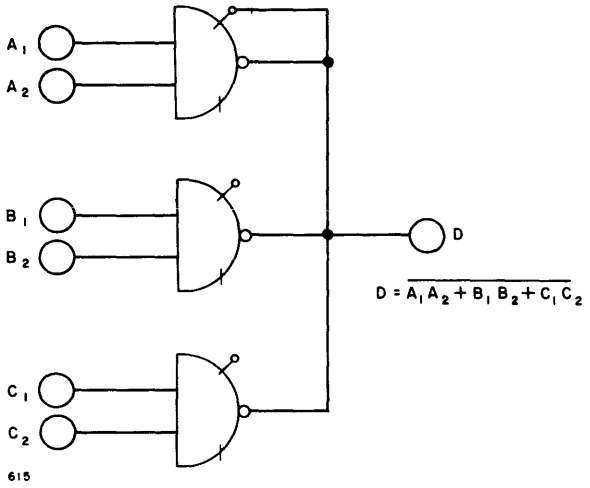


Figure 3-8.3. Selection Gate Type 1 PAC, Model DG-335, Logic of Gate Structure

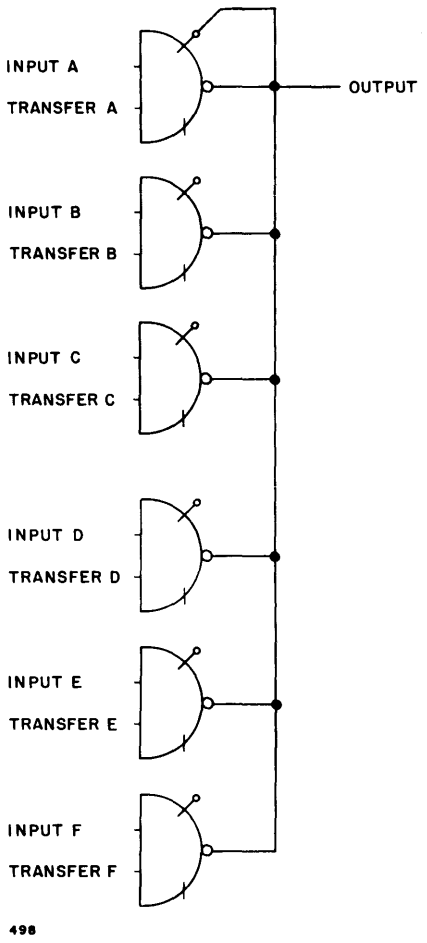


Figure 3-8.4. Selection Gate Type 1 PAC, Model DG-335, Paralleling Gate Structures

3-9 SELECTION GATE TYPE 2 PAC, MODEL DG-336

The Selection Gate Type 2 PAC, Model DG-336 (Figures 3-9.1 and 3-9.2), contains two independent functional gate structures. Each structure has four sets of gates that perform the AND-OR-INVERT function. Section A has three inputs per gate and section B has four inputs per gate. Any gate in a structure may be selected independently. Refer to Section II for a detailed description of the basic μ-PAC NAND gate.

INPUT AND OUTPUT SIGNALS

Inputs.--When all inputs to one NAND gate are at logic ONE (+6v), the common collector output is at ground.

Load.--This point is internally connected through a collector load resistor to +6v.

Collector Output.--The collector output of every active gate structure must be connected to its own load, to the collector output of another loaded gate structure, or to a standard gate output.

SPECIFICATIONS

Frequency of Operation (System)	Circuit Delay
DC to 5 mc	(Measured at +1.5v, averaged over two stages)
Input Loading	30 nsec (max)
1 unit load each	Current Requirements
Output Drive Capability	+6v: 60 ma (max)
8 unit loads each	Power Dissipation
Outputs in Parallel	0.36w (max)
Refer to Section II.	Handle Color Code
	Red

APPLICATIONS

Each gate structure can be used for control or data transfer operations as shown in Figure 3-9.3. By tying collector outputs together, with a common load termination, up to 8 sets of inputs may be gated to a common output. (See Figure 3-9.4.)

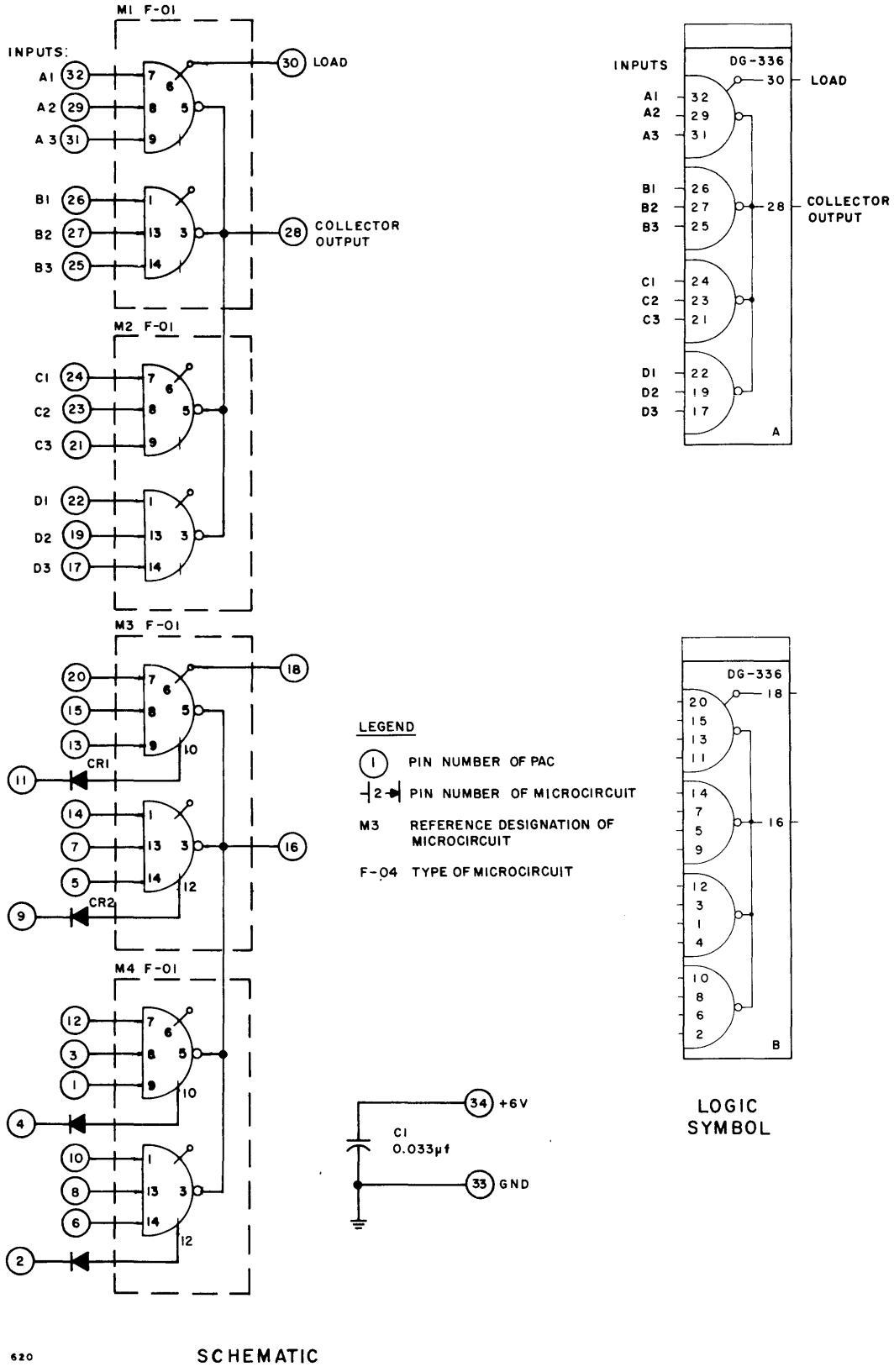
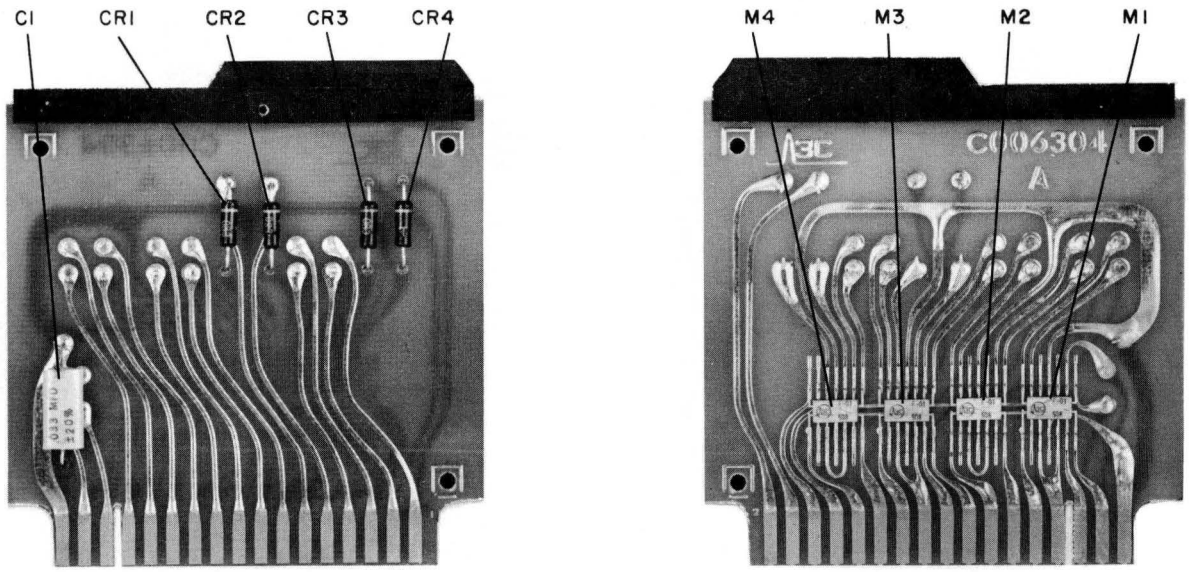


Figure 3-9.1. Selection Gate Type 2 PAC, Model DG-336, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR4	DIODE: Replacement Type 1N914	943 083 001

Figure 3-9.2. Selection Gate Type 2 PAC, Model DG-336, Parts Location and Identification

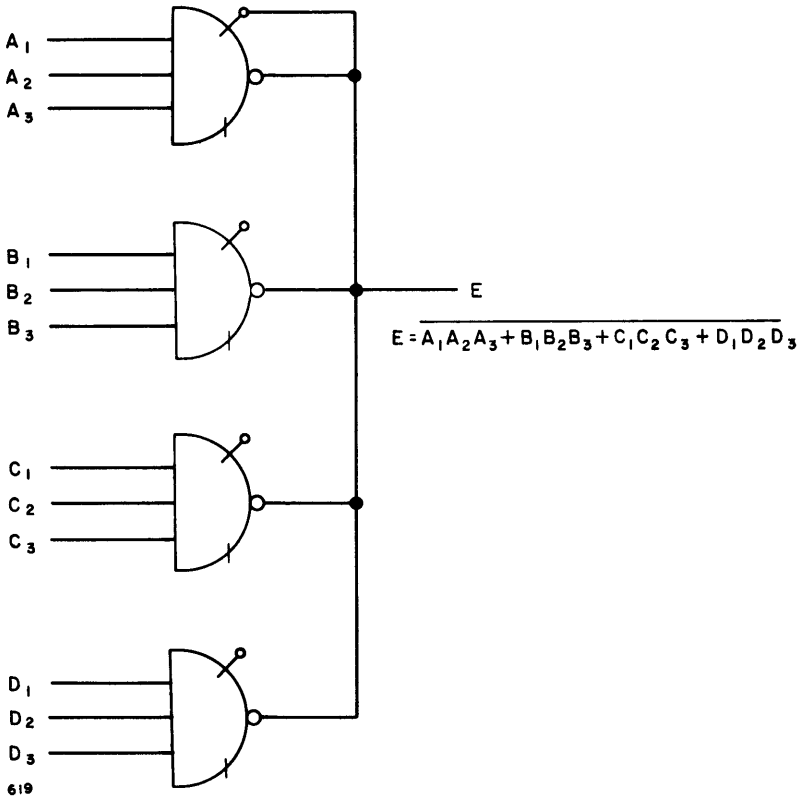


Figure 3-9.3. Selection Gate Type 2 PAC, Model DG-336, Logic of Gate Structure

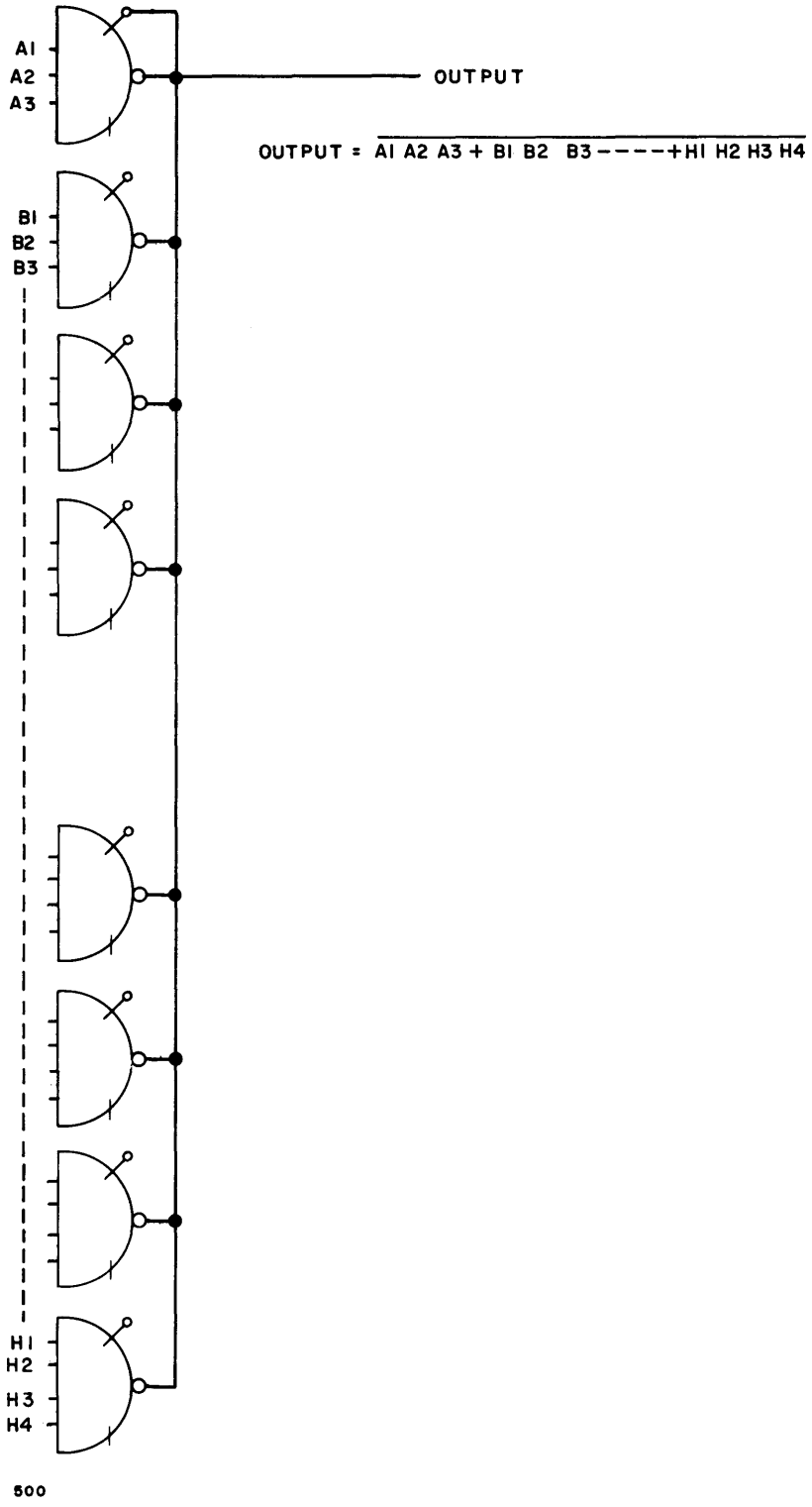


Figure 3-9.4. Selection Gate Type 2 PAC, Model DG-336, Paralleling Gate Structures

3-10 NAND TYPE 1 PAC, MODEL DI-335

The NAND Type 1 PAC, Model DI-335, Figures 3-10. 1 and 3-10.2), contains 10 independent 2-input NAND gates. Each gate performs the NAND function for positive logic (+6v = ONE, 0v = ZERO). For negative logic, it becomes a NOR gate.

Two of the 10 gates have separate load connections available at the PAC terminals. Outputs of these gates can be tied together, using a single load resistor, without loss of output drive capability.

A detailed description of the basic NAND circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

Inputs. -- When both inputs to a gate are +6v or not connected, the output is at ground. When any input is at ground, the output is +6v.

Load. -- This point is internally connected through a collector load resistor to +6v.

Collector Output. -- The collector output must be connected to at least one load resistor, either internal or external to the module.

Output. -- Each output terminal is internally connected to a collector load resistor. If an output is connected to load points or other outputs, the output drive capability of the structure is reduced.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Fan-In

Refer to Section II.

Output Drive Capability

8 unit loads each

Outputs in Parallel

Refer to Section II.

Circuit Delay

(Measured at +1. 5v, averaged over two stages)
30 nsec (max)

Current Requirements

+6v: 110 ma (max)

Power Dissipation

0. 67w (max)

Handle Color Code

Red

APPLICATIONS

The NAND gates operate on levels, pulses, or combinations of both. Two gates can be wired back-to-back to form a dc set-reset flip-flop.

The two gates with separate load outputs form standard NAND gates when the load and collector output terminals are connected. When the collector outputs of gates are connected in parallel as in Figure 3-10. 3, the AND-OR-INVERT function is performed. At the point where the outputs are tied together, an AND operation with logic ONES (OR operation with logic ZEROs) takes place.

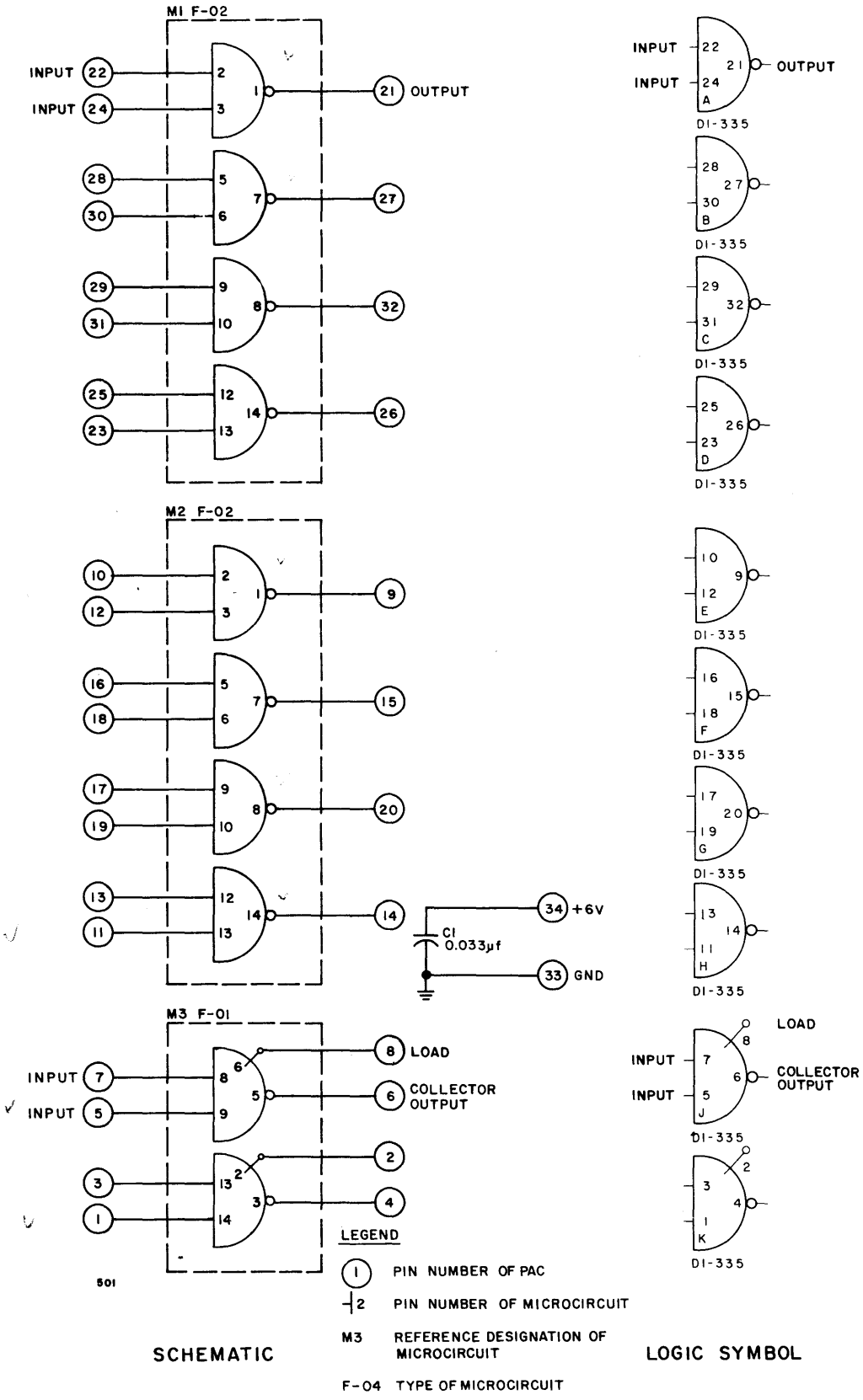
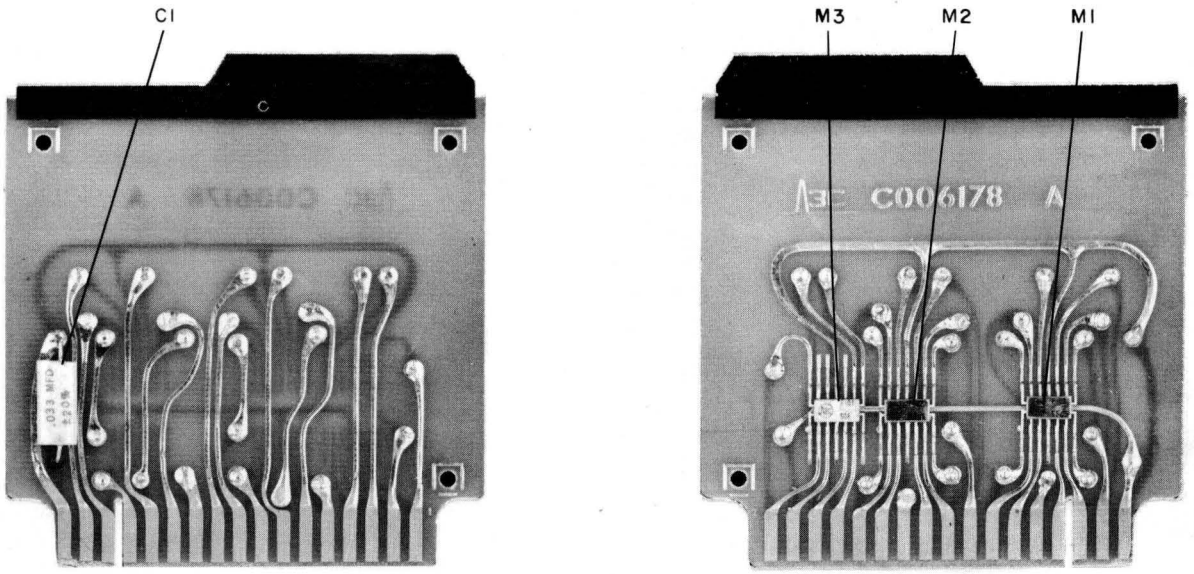


Figure 3-10.1. NAND Type 1 PAC, Model DI-355, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M3	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-10.2. NAND Type 1 PAC, Model DI-335,
Parts Location and Identification

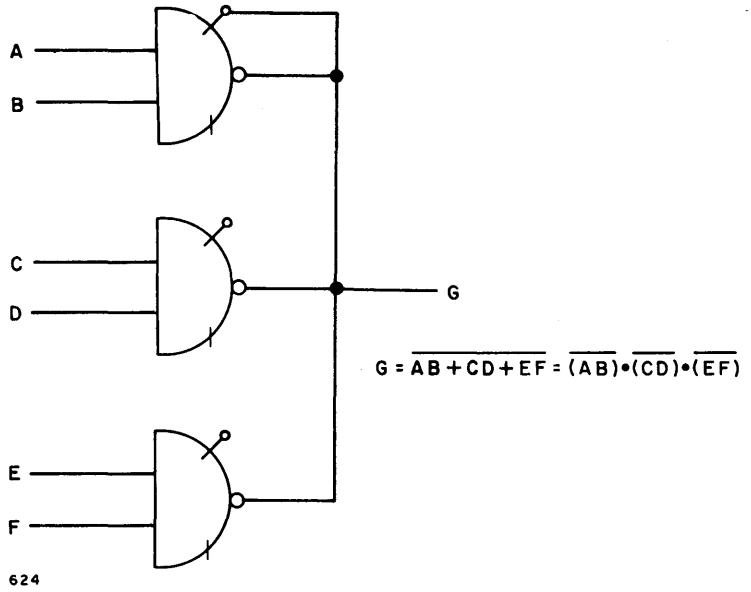


Figure 3-10.3. NAND Type 1 PAC, Model DI-335, Gates Used in Parallel

3-11 NAND TYPE 2 PAC, MODEL DL-335

The NAND Type 2 PAC, Model DL-335 (Figures 3-11.1 and 3-11.2), contains six 4-input NAND gates. Each gate performs the NAND function for positive logic, (+6v = ONE, 0v = ZERO). For negative logic, it becomes a NOR gate.

Two of the six gates have separate load connections available at the PAC terminals. Outputs of these gates can be tied together, using a single load resistor, without loss of output drive capability.

A detailed description of the basic NAND circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

Inputs. -- When all inputs to a gate are at +6v or not connected, the output is at ground. When any input is at ground, the output is at +6v.

Load. -- This point is internally connected through a collector load resistor to +6v.

Collector Output. -- The collector output of any gate must be connected to at least one collector resistor, either internal or external to the module.

Output. -- Each output terminal is internally connected to a collector load resistor. If an output is connected to load points or other outputs, the output drive capability of the structure is reduced.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Fan-In

Refer to Section II.

Output Drive Capability

8 unit loads each

Outputs in Parallel

Refer to Section II.

Circuit Delay

(Measured at +1.5v, averaged over two stages)
30 nsec (max)

Current Requirements

+6v: 75 ma (max)

Power Dissipation

0.45w (max)

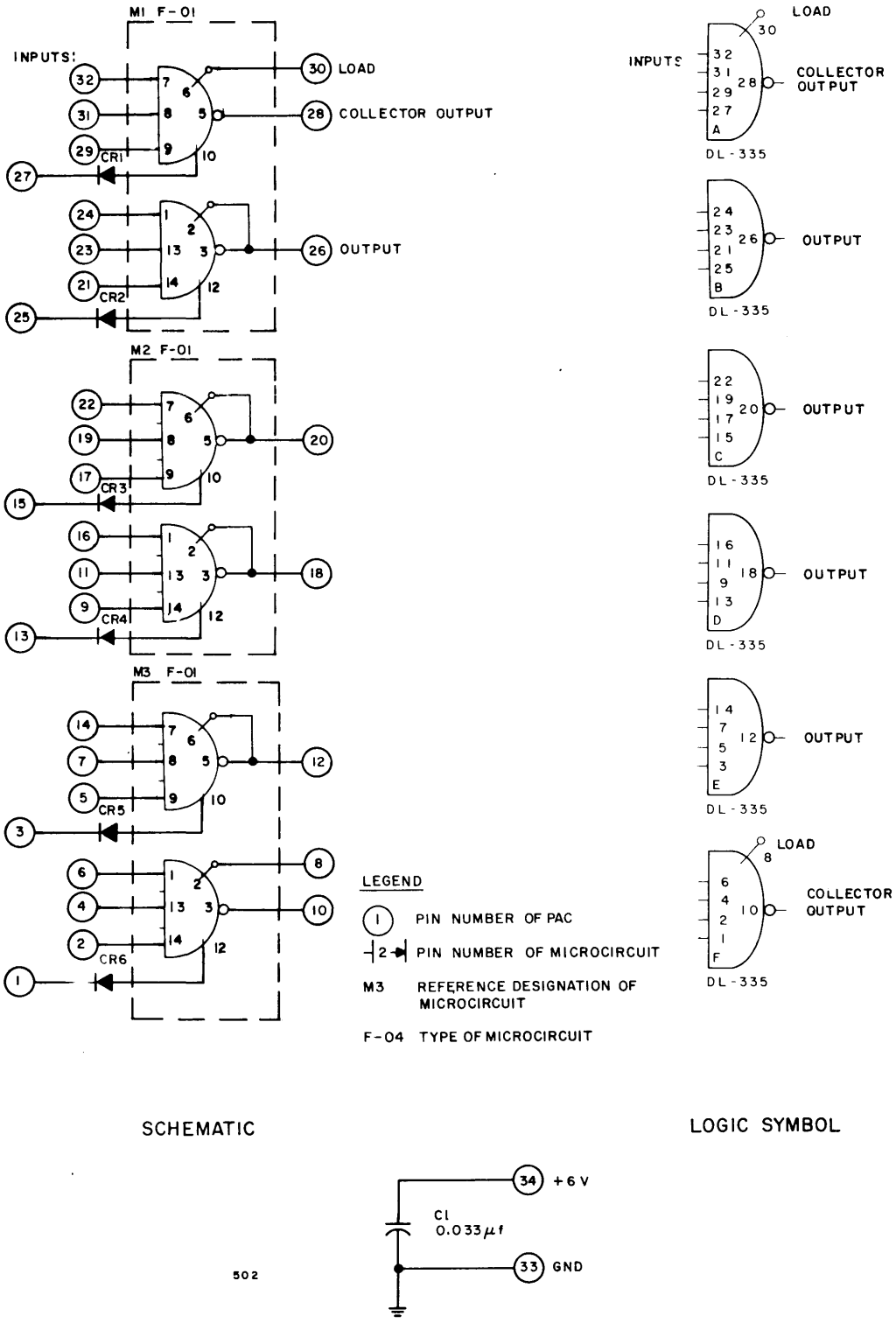
Handle Color Code

Red

APPLICATIONS

The NAND gates operate on levels or pulses, or combinations of both. Two gates can be wired back to back to form a dc set-reset flip-flop.

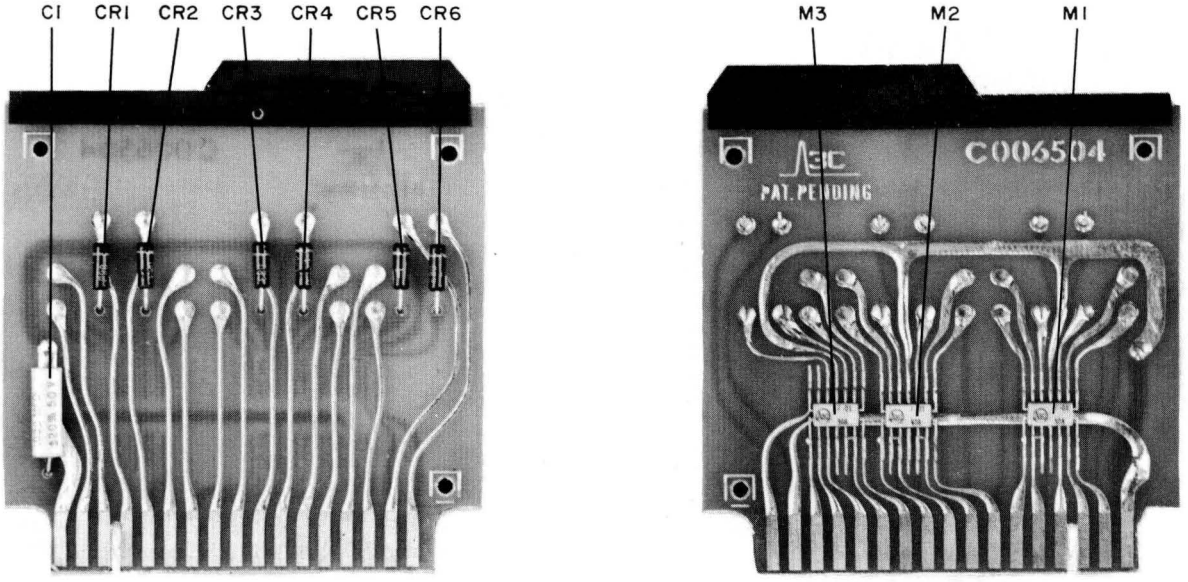
The two gates with separate load outputs form standard NAND gates when the load and collector output terminals are connected. When the collector outputs of such gates are connected in parallel as in Figure 3-11.3, the AND-OR-INVERT function is performed. At the point where the outputs are tied together, an AND operation with logic ONEs (OR operation with logic ZEROs) takes place.



SCHEMATIC LOGIC SYMBOL

Figure 3-11.1. NAND Type 2 PAC, Model DL-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR6	DIODE: Replacement Type 1N914	943 083 001

Figure 3-11.2. NAND Type 2 PAC, Model DL-335,
Parts Location and Identification

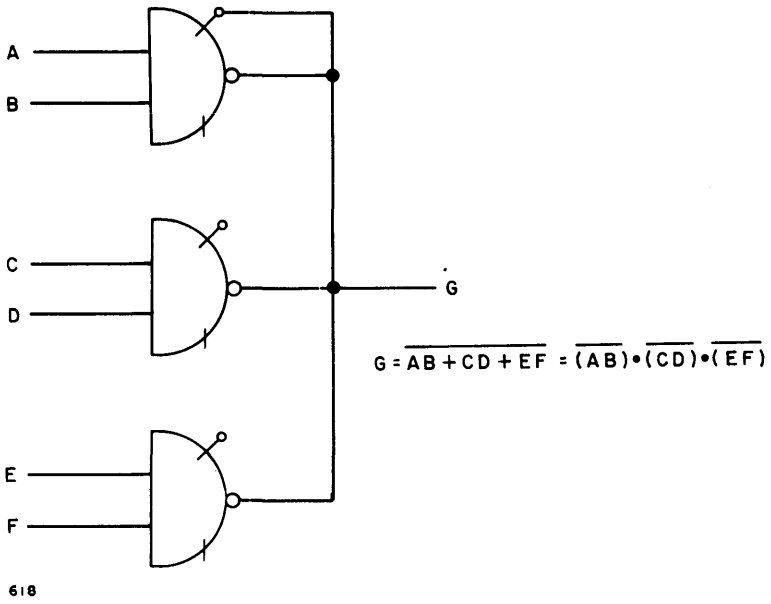


Figure 3-11.3. NAND Type 2 PAC, Model DL-335, Gates Used in Parallel

3-12 DELAY MULTIVIBRATOR PAC, MODEL DM-335

The Delay Multivibrator PAC, Model DM-335 (Figures 3-12.1 and 3-12.2), contains two independent delay multivibrator circuits (one shots). In response to an input signal, the circuit will produce both a positive and a negative output pulse. If no external connections are made, the pulse width will be 500 nsec. Pulse widths between 100 nsec and 500 μsec may be attained by wiring jumpers at the PAC connector. External capacitors may be used to obtain any pulse width up to several seconds. A significant feature of the PAC is that the output transition times are independent of the input signal and the output pulse width.

CIRCUIT FUNCTION

The delay multivibrator circuit is activated by a positive (ZERO to ONE) transition on an input (Figure 3-12.3). The output of the NAND gate will drop sharply from +6v to 0v, and couple through CR1 and C6 to the base of Q1. The base of Q1 going negative will turn off that transistor, which will then turn on another NAND gate to lock up the junction point of CR1 and C6 at ground. The input signal can then drop from a positive voltage to ground without affecting the pulse delay operation.

After the base of Q1 is driven negative, it tries to go positive towards +6v through R3. The basic timing is derived from the resistor-capacitor combination of R3 and C6. When the base of Q1 becomes about +0.7v, Q1 turns on and the output pulse ends. Resistor R2 aids the recovery time by pulling C6 towards +6v.

The pulse width may be changed by connecting different capacitors in parallel with C6. Additional pulse width variation may be obtained by connecting R1 in parallel with R3. The negation and assertion outputs are taken from two NAND gate microcircuits in series.

INPUT AND OUTPUT SIGNALS

Input. -- Each delay circuit has two standard microcircuit NAND gate inputs. A positive-going signal at either input triggers an output pulse. If either input is held at ground, triggering by the other input is inhibited.

Enable. -- If the enable input is held at logic ONE or is not connected, the circuit can produce output pulses. If logic ZERO (ground) is applied, no output pulses will occur, and if applied during an output pulse, the pulse will end.

Assertion Output. -- For the duration of the delay, a positive pulse appears at the assertion output.

Negation Output. -- For the duration of the delay, a negative pulse appears at the negation output.

Delay Selection Terminals. -- Additional capacitors and a resistor are provided in each delay circuit. Table 3-12. 1 lists the external jumper connections required for various delay intervals.

Table 3-12. 1.
Connections for Internally Provided Pulse Widths

Assertion Output Pulse Width	Pin Connections	
	Circuit A	Circuit B
100 nsec	6-3	21-27
500 nsec	None	None
1 μsec	2-3 and 6-3	20-27 and 21-27
5 μsec	2-3	20-27
10 μsec	4-3 and 6-3	11-27 and 21-27
50 μsec	4-3	11-27
100 μsec	1-3 and 6-3	25-27 and 21-27
500 μsec	1-3	25-27

External Capacitors. -- An external capacitor may be connected to the delay node and external capacitor terminals, or mounted on the PAC standoffs, to produce any pulse width between 100 nsec and several seconds.

NOTE

For installation on PAC standoffs, capacitor dimensions cannot exceed 0. 115 in. high and 0. 550 in. long.

The value of the external capacitor (with the range control and delay node terminals jumpered) can be determined from the following equation:

$$C = PW\ (470) - 36$$

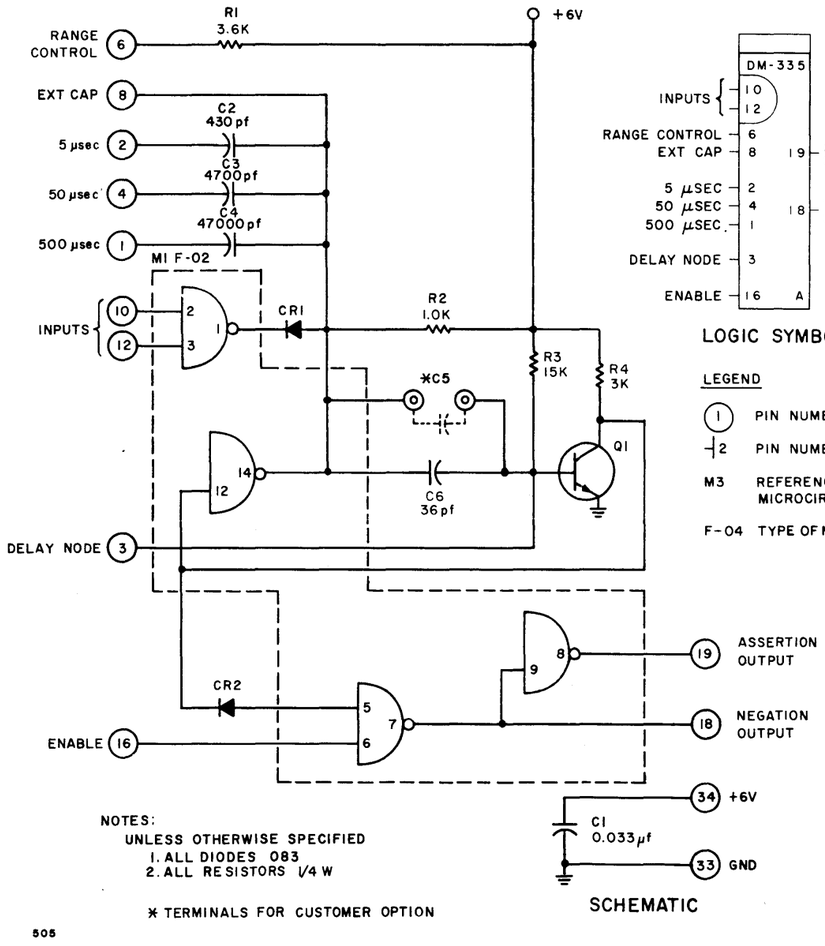
where C is the required capacitance in picofarads and PW is the desired pulse width in microseconds. Make the following connections when installing capacitors:

Circuit A

Connect pins 6 and 3; mount external capacitor (C5) between pins 3 and 8 or between the standoffs.

Circuit B

Connect pins 21 and 27; mount external capacitor(C10)between pins 27 and 23 or between the standoffs.



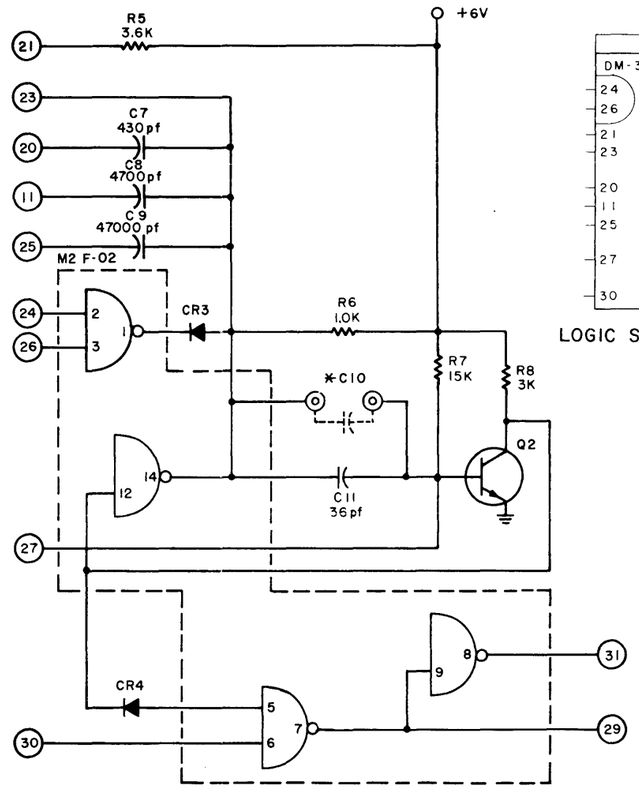
LEGEND

(1) PIN NUMBER OF PAC

2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

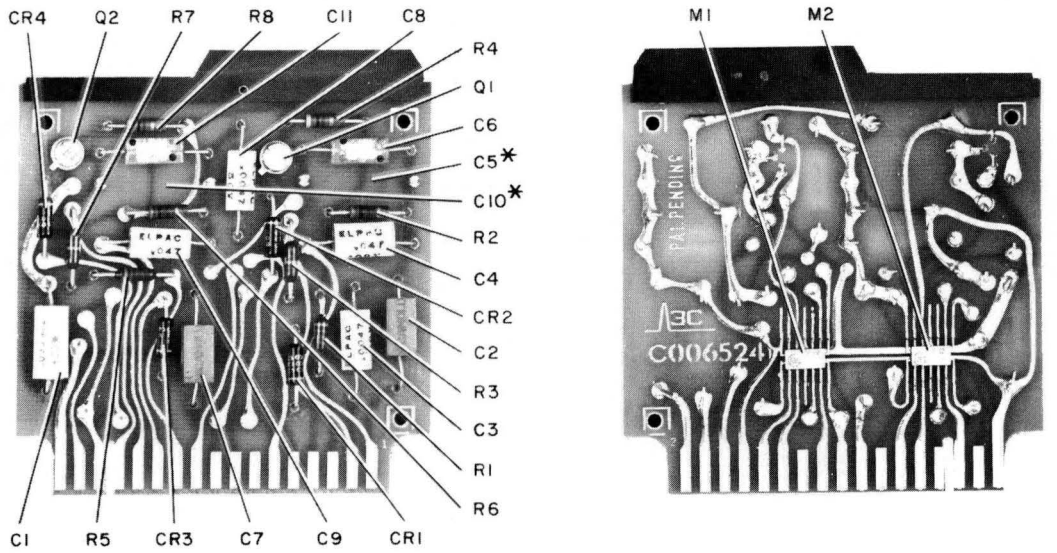
F-04 TYPE OF MICROCIRCUIT



505

Figure 3-12.1. Delay Multivibrator PAC, Model DM-335, Schematic Diagram and Logic Symbol (Ser. No. 1 through 999)

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C2, C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 430 pf ±2%, 50 vdc	930 313 318
C3, C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 4700 pf ±2%, 50 vdc	930 313 309
C4, C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 47,000 pf ±2%, 50 vdc	930 313 317
C5, C10	Customer option, listed for reference only	
C6, C11	CAPACITOR, FIXED, MICA DIELECTRIC: 36 pf ±2%, 500 vdc	930 005 512
R1, R5	RESISTOR, FIXED, FILM: 3.60 K, ±2%, 1/4w	932 114 062
R2, R6	RESISTOR, FIXED, COMPOSITION: 1.0 K, ±5%, 1/4w	932 007 049
R3, R7	RESISTOR, FIXED, FILM: 15.0 K, ±2%, 1/4w	932 114 077
R4, R8	RESISTOR, FIXED, COMPOSITION: 3.0 K, ±5%, 1/4w	932 007 060
Q1, Q2	TRANSISTOR: 2N3011	943 722 002
CR1-CR4	DIODE: Replacement Type 1N914	943 083 001

Figure 3-12.2. Delay Multivibrator PAC, Model DM-335, Parts Location and Identification

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc or $\frac{0.75}{\text{Pulse Width}}$ whichever is lower

Input Timing

50 nsec (min) pulse at logic ONE (+1.5v or more positive)

Assertion Output

Positive pulse, activated on the positive (ZERO to ONE) transition of the input. Pulse width is 500 nsec without external connections.

Circuit Delay (See Figure 3-12.3).

Assertion: 60 nsec (typ)

Negation: 30 nsec (typ)

Pulse Width Accuracy (Assertion Output)

Pulse widths between 100 nsec and 1000 nsec: 12% (max)

Pulse widths longer than 1000 nsec: 6% (max)*

Jitter

0.1% of pulse width (typ)

Recovery Time

(for 5% reduction in pulse width)

100 nsec or 50% of pulse width, whichever is greater

Input Loading

1 unit load each

Negation Output

Negative pulse, activated on the positive (ZERO to ONE) transition of the input. Pulse width is 500 nsec without external connections.

Output Drive Capability

Assertion: 8 unit loads each

Negation: 7 unit loads each

Pulse Width Variation

Pulse widths are not affected by supply voltage variation between +5v and +6v.

Pulse Width Variation over Temp. Range (0°C to 55°C)

Pulse widths between 100 nsec and 1000 nsec: ±4% (typ), ±10% (max)

Pulse widths 1000 nsec and greater: ±2% (typ), ±5% (max)*

Current Requirements

+6v: 100 ma (max)

Power Dissipation

0.60w (max)

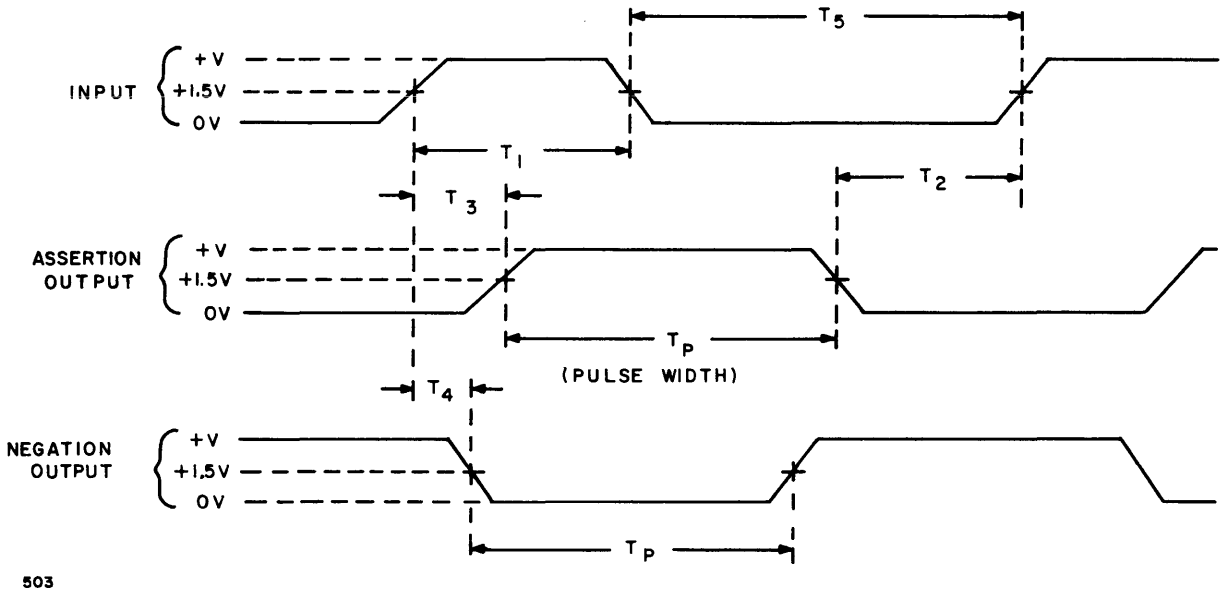
Handle Color Code

Yellow

APPLICATIONS

Several DM circuits can be connected in series to produce a sequence of pulses. Figure 3-12.4 shows two circuits used to produce a short (100 nsec) positive pulse after a longer delay interval determined by the first circuit. The short positive pulse is well suited for driving flip-flop clock inputs.

* For pulses of 300 μsec and over, a tantalum capacitor is recommended for maximum pulse width accuracy and temperature stability.



Pulse Width (T_1)	=	50 nsec (min)
Recovery Time (T_2, T_5)	=	Refer to specifications.
Assertion Circuit Delay (T_3)	=	60 nsec (typ)
Negation Circuit Delay (T_4)	=	30 nsec (typ)
Voltage (V)	=	3.5 volts (min)

Figure 3-12.3. Timing of the Delay Multivibrator PAC, Model DM-335

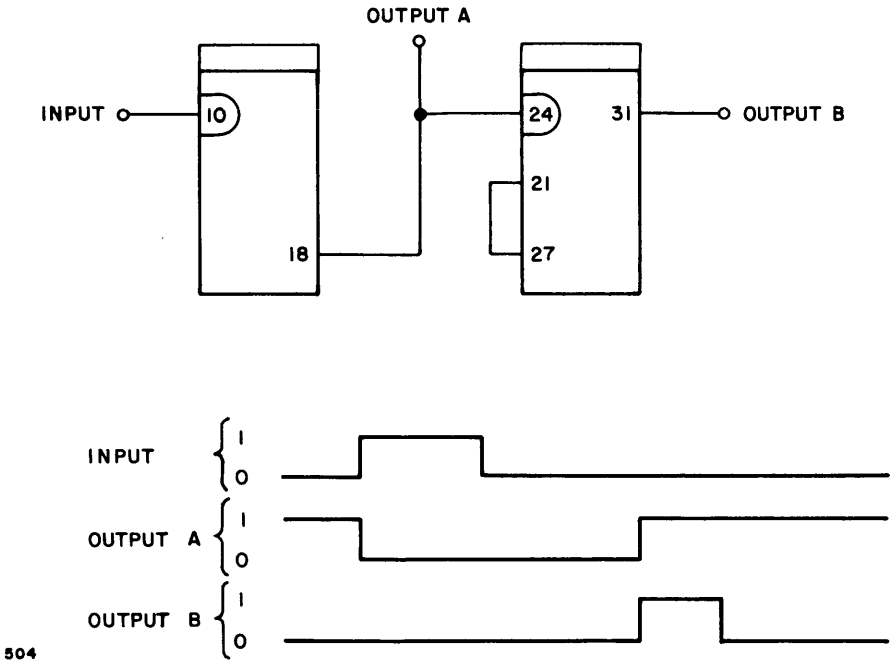


Figure 3-12.4. Delay Multivibrator PAC, Model DM-335, Delayed Pulse Generator

3-12A DELAY MULTIVIBRATOR PAC, MODEL DM-335*

The Delay Multivibrator PAC, Model DM-335 (Figures 3-12A.1 and 3-12A.2), contains two independent delay multivibrator circuits (one shots). In response to an input signal, the circuit will produce both a positive and a negative output pulse. If no external connections are made, the pulse width will be 100 nsec. Pulse widths between 50 nsec and 100 μsec may be attained by wiring jumpers at the PAC connector. External capacitors may be used to obtain any pulse width up to several seconds. A significant feature of the PAC is that the output transition times are independent of the input signal and the output pulse width.

CIRCUIT FUNCTION

The delay multivibrator circuit is activated by a positive (ZERO to ONE) transition on an input (Figure 3-12A.3). The output of the NAND gate will drop sharply from +6v to 0v, and couple through CR1 and C6 to the base of Q1. The base of Q1 going negative will turn off that transistor, which will then turn on another NAND gate to lock up the junction point of CR1 and C6 at ground. The input signal can then drop from a positive voltage to ground without affecting the pulse delay operation.

After the base of Q1 is driven negative, it tries to go positive toward +6v through R3. The basic timing is derived from the resistor-capacitor combination of R3 and C6. When the base of Q1 becomes about +0.7v, Q1 turns on and the output pulse ends. Resistor R2 aids the recovery time by pulling C6 toward +6v.

The pulse width may be changed by connecting different capacitors in parallel with C6. Additional pulse width variation may be obtained by connecting R1 in parallel with R3. The negation and assertion outputs are taken from two NAND gate microcircuits in series.

INPUT AND OUTPUT SIGNALS

Input. -- Each delay circuit has two standard microcircuit NAND gate inputs. A positive-going signal at either input triggers an output pulse. If either input is held at ground, triggering by the other input is inhibited.

Enable. --If the enable input is held at logic ONE or is not connected, the circuit can produce output pulses. If logic ZERO (ground) is applied, no output pulses will occur, and if applied during an output pulse, the pulse will end.

Assertion Output. -- For the duration of the delay, a positive pulse appears at the assertion output.

Negation Output. -- For the duration of the delay, a negative pulse appears at the negation output.

*This PAC is the same as Model DM-335 as discussed in paragraph 3-12 except for certain component values and specifications. Paragraph 3-12 covers only DM-335 PACs, Serial No. 1 through 999.

Delay Selection Terminals. -- Additional capacitors and a resistor are provided in each delay circuit. Table 3-12A.1 lists the external jumper connections required for various delay intervals.

Table 3-12A.1
Connections for Internally Provided Pulse Widths

Assertion Output Pulse Width	Pin Connections	
	Circuit A	Circuit B
50 nsec	6-3	21-27
100 nsec	None	None
500 nsec	2-3 and 6-3	20-27 and 21-27
1 μsec	2-3	20-27
5 μsec	4-3 and 6-3	11-27 and 21-27
10 μsec	4-3	11-27
50 μsec	1-3 and 6-3	25-27 and 21-27
100 μsec	1-3	25-27

External Capacitors. -- An external capacitor may be connected to the delay node and external capacitor terminals, or mounted on the PAC standoffs, to produce any pulse width between 50 nsec and several seconds. If a polarized capacitor is used, the positive lead should be connected to pin 8 (circuit A) or 23 (circuit B).

NOTE

For installation on PAC standoffs, capacitor dimensions cannot exceed 0.115 in. high and 0.550 in. long.

The value of the external capacitor (without the range control and delay node terminals jumpered) can be determined from the following equation:

$$C = PW\ (470) - 43$$

where C is the required capacitance in picofarads and PW is the desired pulse width in microseconds. Make the following connections when installing capacitors:

Circuit A

Mount external capacitor (C5) between pins 3 and 8 or between the standoffs.

Circuit B

Mount external capacitor (C10) between pins 27 and 23 or between the standoffs.

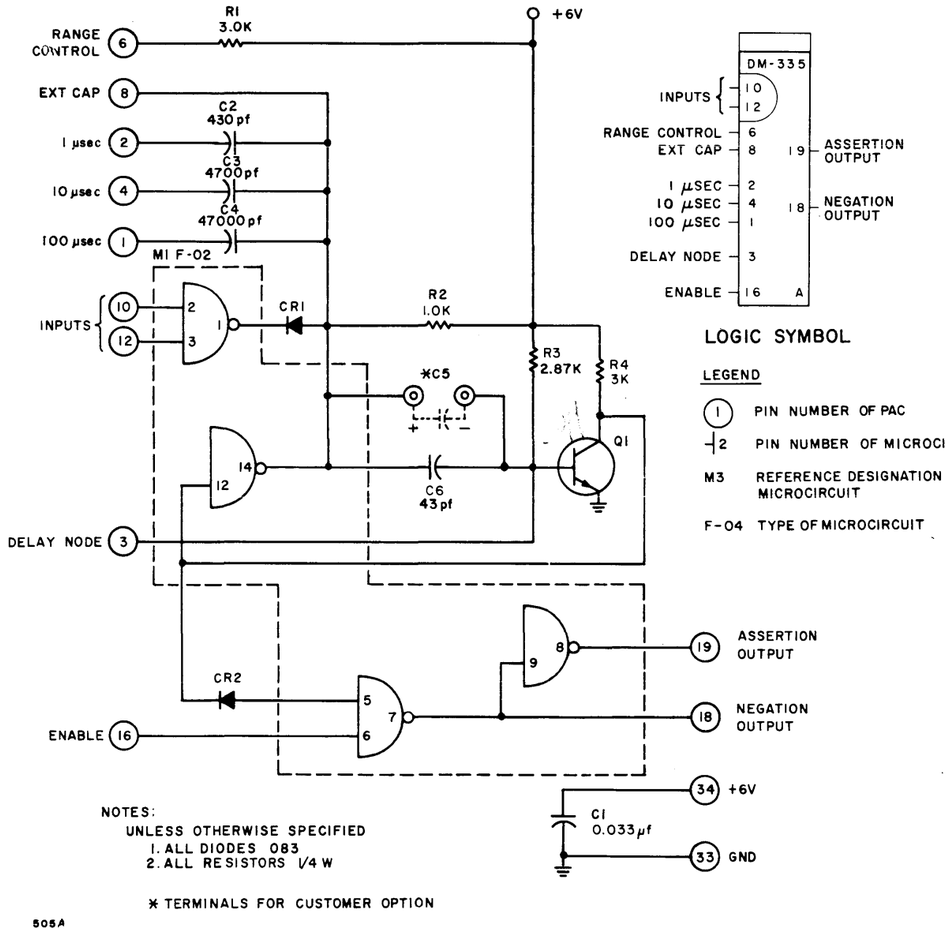
The value of the external capacitor with range control and delay node terminals connected (pin 6 to pin 3 for circuit A; pin 21 to pin 27 for circuit B), can be determined from the following equation:

$$C = PW\ (918) - 43$$

where C is the required capacitance in picofarads and PW is the desired pulse width in microseconds.

NOTE

If leads used to jumper external capacitors exceed 3 inches, they should be twisted pair with one wire terminated to ground.



LOGIC SYMBOL

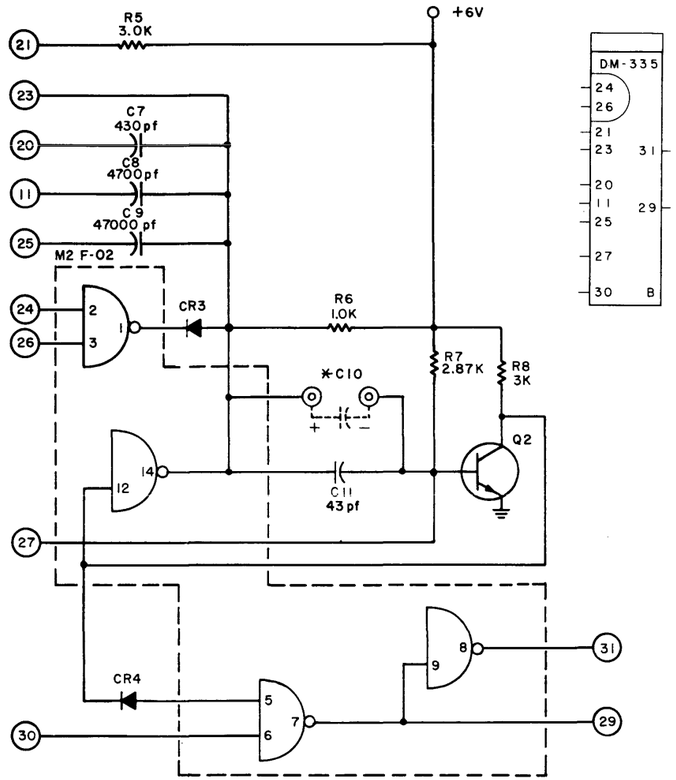
LEGEND

(1) PIN NUMBER OF PAC

2 PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

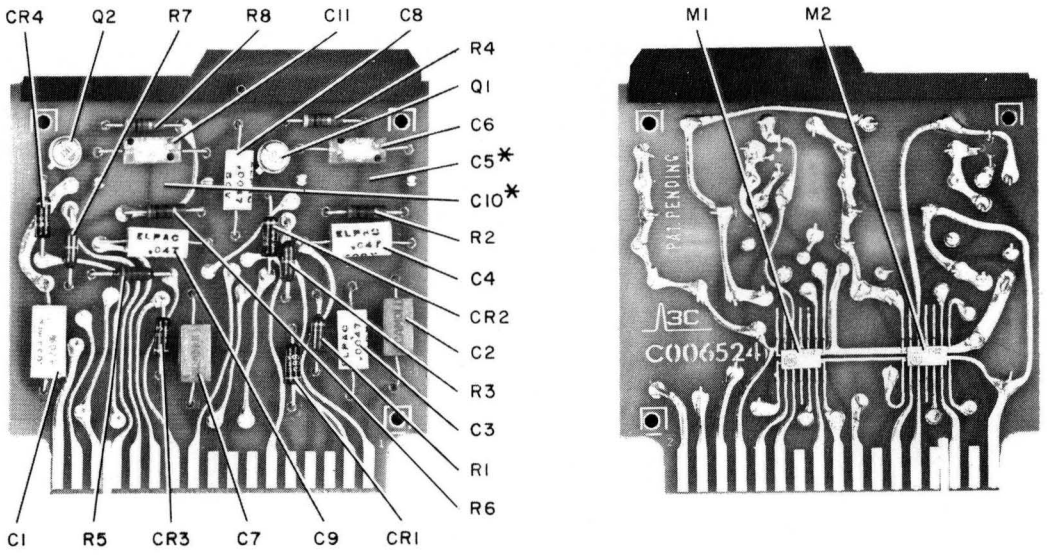
F-04 TYPE OF MICROCIRCUIT



SCHEMATIC

Figure 3-12A. 1. Delay Multivibrator PAC, Model DM-335, Schematic Diagram and Logic Symbol

Parts Location



*CUSTOMER OPTION

530

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C2, C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 430 pf ±2%, 50 vdc	930 313 318
C3, C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 4700 pf ±2%, 50 vdc	930 313 309
C4, C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 47,000 pf ±2%, 50 vdc	930 313 317
C5, C10	Customer option, listed for reference only	
C6, C11	CAPACITOR, FIXED, DIELECTRIC: 43 pf ±2%, 100 vdc	930 005 514
R1, R5	RESISTOR, FIXED, FILM: 3.0 K, ±2%, 1/4w	932 114 060
R2, R6	RESISTOR, FIXED, COMPOSITION: 1.0 K, ±5%, 1/4w	932 007 049
R3, R7	RESISTOR, FIXED, FILM: 2.87 K, ±2%, 1/8w	932 113 223
R4, R8	RESISTOR, FIXED, COMPOSITION: 3.0 K, ±5%, 1/4w	932 007 060
Q1, Q2	TRANSISTOR:	943 722 002
CR1-CR4	DIODE: Replacement Type 1N914	943 083 001

Figure 3-12A.2. Delay Multivibrator PAC, Model DM-335, Parts Location and Identification

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc or $\frac{0.75}{\text{Pulse Width}}$ whichever is lower

Input Timing

50 nsec (min) pulse at logic ONE (+1.5v or more positive)

Assertion Output

Positive pulse, activated on the positive (ZERO to ONE) transition of the input. Pulse width is 100 nsec without external connections.

Circuit Delay (See Figure 3-12A.3)

Assertion: 60 nsec (typ)

Negation: 30 nsec (typ)

Pulse Width Accuracy (Assertion Output)

Pulse widths under 100 nsec: ±10 nsec

Pulse widths between 100 nsec and 1000 nsec: 12% (max)

Pulse widths longer than 1000 nsec: 6% (max)*

Jitter

0.1% of pulse width (typ)

Recovery Time
(Refer to Figure 3-12A.3)

Without Range Control:
125 nsec or 70% of output pulse width, whichever is greater (for 5% reduction in output pulse width)

200 nsec or 100% of output pulse width, whichever is greater (for 1% reduction in output pulse width)

Input Loading

1 unit load each

Negation Output

Negative pulse, activated on the positive (ZERO to ONE) transition of the input. Pulse width is 100 nsec without external connections.

Output Drive Capability

Assertion: 8 unit loads each

Negation: 7 unit loads each

Pulse Width Variation

Pulse widths are not affected by supply voltage variation between +5v and +6v.

Pulse Width Variation over Temp. Range (0°C to 55°C)

Pulse widths between 50 nsec and 1000 nsec: ±4% (typ), ±10% (max)

Pulse widths 1000 nsec and greater: ±2% (typ), ±5% (max)*

Current Requirements

+6v: 100 ma (max)

Power Dissipation

0.60w (max)

Handle Color Code

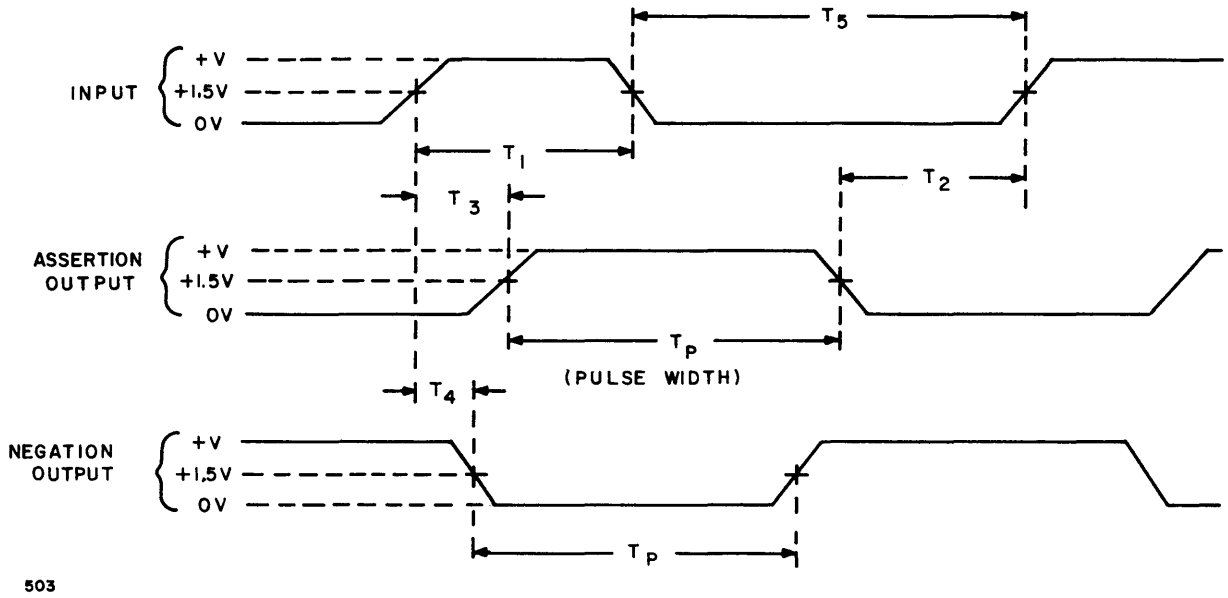
Yellow

*For pulses of 300 μsec and over, a tantalum capacitor is recommended for maximum pulse width accuracy and temperature stability.

Recovery Time (Cont)

With Range Control:
150 nsec or 125% of output pulse width, whichever is greater (for 5% reduction in output pulse width)

200 nsec or 200% of output pulse width, whichever is greater (for 1% reduction in output pulse width)



Input Pulse Width (T_1)	= 50 nsec (min)
Recovery Time (T_2, T_5)	= Refer to specifications.
Assertion Circuit Delay (T_3)	= 60 nsec (typ)
Negation Circuit Delay (T_4)	= 30 nsec (typ)
Voltage (V)	= 3.5 volts (min)

Figure 3-12A.3. Timing of the Delay Multivibrator PAC, Model DM-335

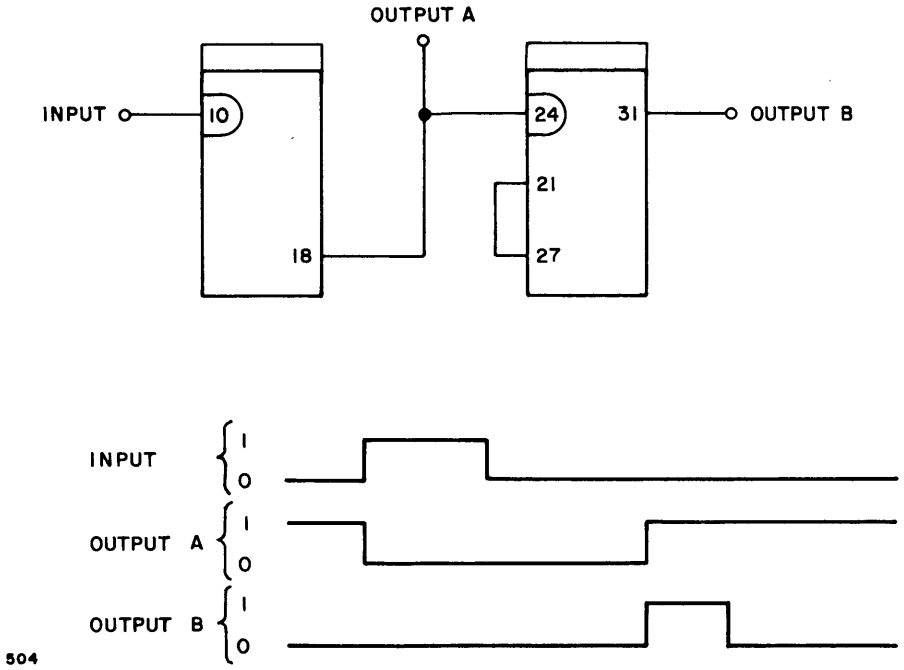


Figure 3-12A. 4. Delay Multivibrator PAC, Model DM-335
Delayed Pulse Generator

3-12B ADJUSTABLE DELAY MULTIVIBRATOR PAC, MODEL DM-336

The Adjustable Delay Multivibrator PAC, Model DM-336 (Figures 3-12B.1 and 3-12B.2), contains two independent adjustable delay multivibrator circuits (one shots). In response to an input signal, the circuit will produce both a positive and a negative output pulse. If no external connections are made, the pulse width is adjustable from 50 to 300 nsec. Pulse widths between 300 nsec and 300 μsec may be attained by wiring jumpers at the PAC connector. External capacitors may be used to obtain any pulse width up to several seconds. A significant feature of the PAC is that the output transition times are independent of the input signal and the output pulse width.

CIRCUIT FUNCTION

The adjustable delay multivibrator circuit is activated by a positive (ZERO to ONE) transition on an input (Figure 3-12B.3). The output of the NAND gate will drop sharply from +6v to 0v, and couple through CR1 and C6 to the base of Q1. The base of Q1 going negative will turn off that transistor, which will then turn on another NAND gate to lock up the junction point of CR1 and C6 at ground. The input signal can then drop from a positive voltage to ground without affecting the pulse delay operation.

After the base of Q1 is driven negative, it tries to go positive toward +6v through R1 + R3. The basic timing is derived from the resistor-capacitor combination of R1, R3 and C6. When the base of Q1 becomes about +0.7v, Q1 turns on and the output pulse ends. Resistor R2 aids the recovery time by pulling C6 toward +6v.

The pulse width may be changed by connecting different capacitors in parallel with C6. Continuous pulse width variation can be obtained by varying R1 in series with R3. The negation and assertion outputs are taken from two NAND gate microcircuits in series.

INPUT AND OUTPUT SIGNALS

Input. -- Each delay circuit has two standard microcircuit NAND gate inputs. A positive-going signal at either input triggers an output pulse. If either input is held at ground, triggering by the other input is inhibited.

Enable. -- If the enable input is held at logic ONE or is not connected, the circuit can produce output pulses. If logic ZERO (ground) is applied, no output pulses will occur, and if applied during an output pulse, the pulse will end.

Assertion Output. -- For the duration of the delay, a positive pulse appears at the assertion output.

Negation Output. -- For the duration of the delay, a negative pulse appears at the negation output.

Delay Selection Terminals. -- Additional capacitors are provided in each delay circuit. Table 3-12.1A lists the external jumper connections required for various delay intervals.

Table 3-12.1A
Connections for Internally Provided Pulse Widths

Assertion Output Pulse Width	Pin Connections	
	Circuit A	Circuit B
50 nsec to 300 nsec	None	None
0.3 μsec to 3 μsec	2-3	20-27
3 μsec to 30 μsec	4-3	11-27
30 μsec to 300 μsec	1-3	25-27

External Capacitors. -- An external capacitor may be connected to the delay node and external capacitor terminals, or mounted on the PAC standoffs, to produce any pulse width between 300 μsec and several seconds. If a polarized capacitor is used, the positive lead should be connected to pin 8 (circuit A) or 23 (circuit B).

NOTE

For installation on PAC standoffs, capacitor dimenstions cannot exceed 0.115 in. high and 0.550 in. long.

The value of the external capacitor (with the pulse width control fully clockwise) can be determined from the following equation:

$$C = PW(155) - 43$$

where C is the required capacitance in picofarads and PW is the desired pulse width in microseconds. Make the following connections when installing capacitors:

Circuit A

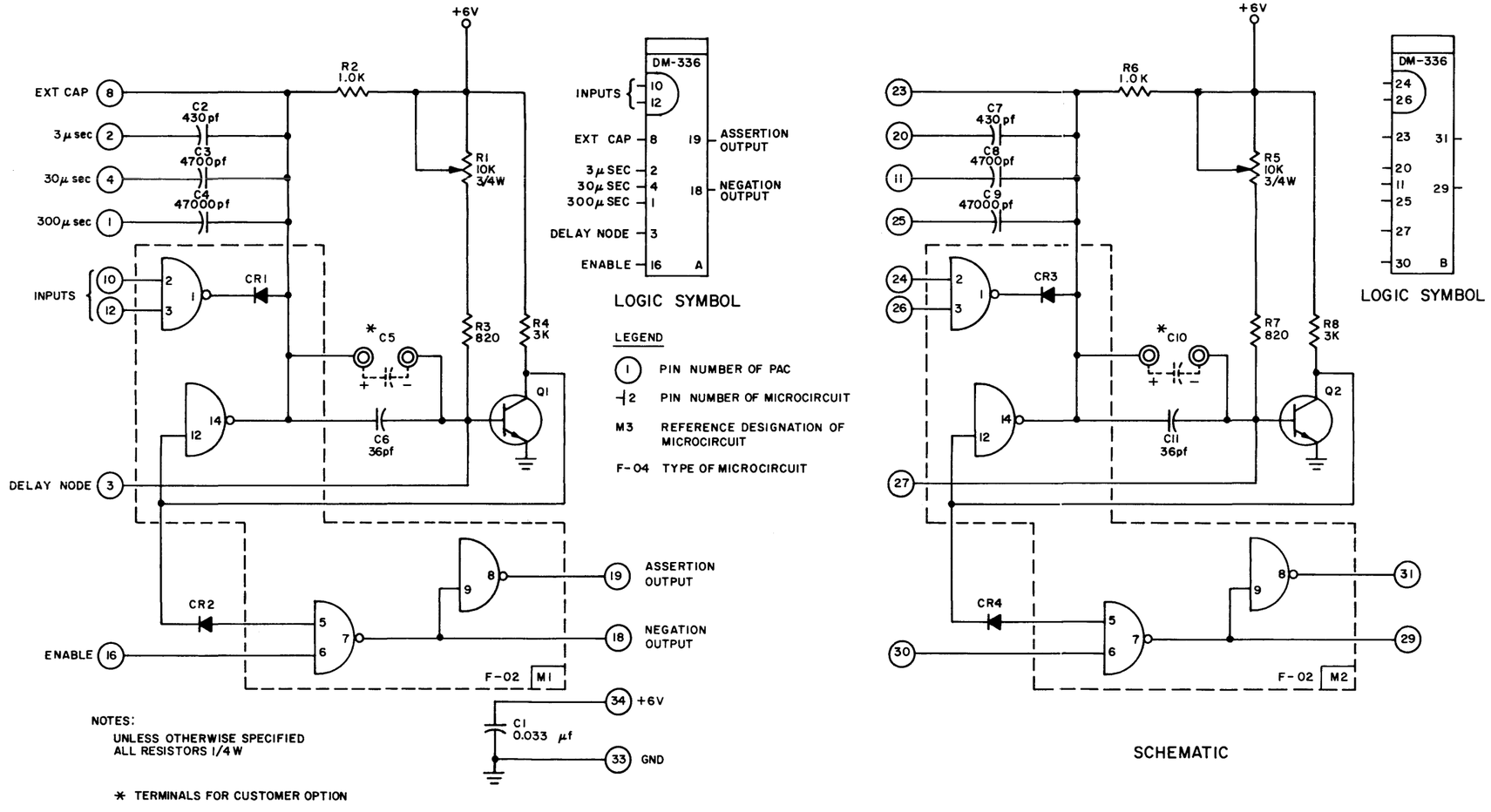
Mount external capacitor (C5) between pins 3 and 8 or between the standoffs.

Circuit B

Mount external capacitor (C10) between pins 23 and 27 or between the standoffs.

NOTE

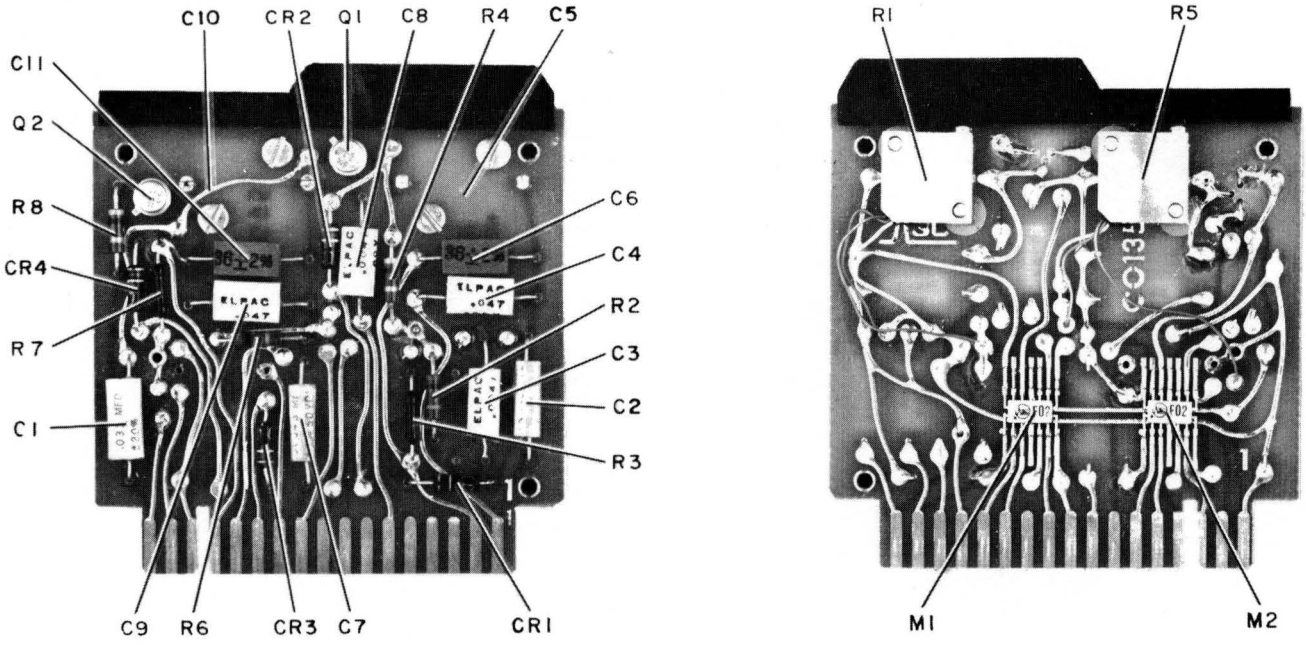
This PAC occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.



SCHEMATIC

Figure 3-12B.1. Adjustable Delay Multivibrator PAC, Model DM-336, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033μf ±20%, 50 vdc	930 313 016
C2, C7	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 430 pf ±2%, 50 vdc	930 313 318
C3, C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 4700 pf ±2%, 50 vdc	930 313 309
C4, C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 47000 pf ±2%, 50 vdc	930 313 317
C5, C10	Customer option, listed for reference only	
C6, C11	CAPACITOR, FIXED, MICA DIELECTRIC: 36 pf ±2%, 500 vdc	930 005 512
CR1-CR4	DIODE: Replacement Type 1N914	943 083 001
Q1, Q2	TRANSISTOR: Replacement Type 2N3011	943 722 002

Figure 3-12B.2. Adjustable Delay Multivibrator PAC, Model DM-336, Parts Location and Identification (Sheet 1)

Electrical Parts List (Cont)

Ref. Desig.	Description	3C Part No.
R1, R5	RESISTOR, VARIABLE, FILM: 10 K ±10%, 3/4w	933 300 107
R2, R6	RESISTOR, FIXED, COMPOSITION: 1.0 K ±5%, 1/4w	932 007 049
R3, R7	RESISTOR, FIXED, FILM: 820 ohms ±2%, 1/4w	932 114 047
R4, R8	RESISTOR, FIXED, COMPOSITION: 3.0 K ±5%, 1/4w	932 007 060

Figure 3-12B.2. Adjustable Delay Multivibrator PAC, Model DM-336, Parts Location and Identification (Sheet 2)

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc or $\frac{0.75}{\text{Pulse Width}}$ whichever is lower

Input Timing

50 nsec (min) pulse at logic ONE (+1.5v or more positive)

Assertion Output

Positive pulse, activated on the positive (ZERO to ONE) transition of the input.

Circuit Delay (See Figure 3-12B.3)

Assertion: 60 nsec (typ)

Negation: 30 nsec (typ)

Pulse Width Accuracy (Assertion Output)

Pulse widths under 100 nsec: ±10 nsec

Pulse widths between 100 nsec and 1000 nsec: 12% (max)

Pulse widths longer than 1000 nsec: 6% (max)*

Jitter

0.1% of pulse width (typ)

Input Loading

1 unit load each

Negation Output

Negative pulse, activated on the positive (ZERO to ONE) transition of the input.

Output Drive Capacity

Assertion: 8 unit loads each

Negation: 7 unit loads each

Pulse Width Variation

Pulse widths are not affected by supply voltage variation between +5v and +6v.

Pulse Width Variation over Temp. Range (0°C to 55°C)

Pulse widths between 50 nsec and 1000 nsec: ±4% (typ), ±10% (max)

Pulse widths 1000 nsec and greater: ±2% (typ), ±5% (max)*

Current Requirements

+6v: 100 ma (max)

Recovery Time

Refer to Figure 3-12B.3.

*For pulses of 300 μsec and over, a tantalum capacitor is recommended for maximum pulse width accuracy and temperature stability.

Recovery Time

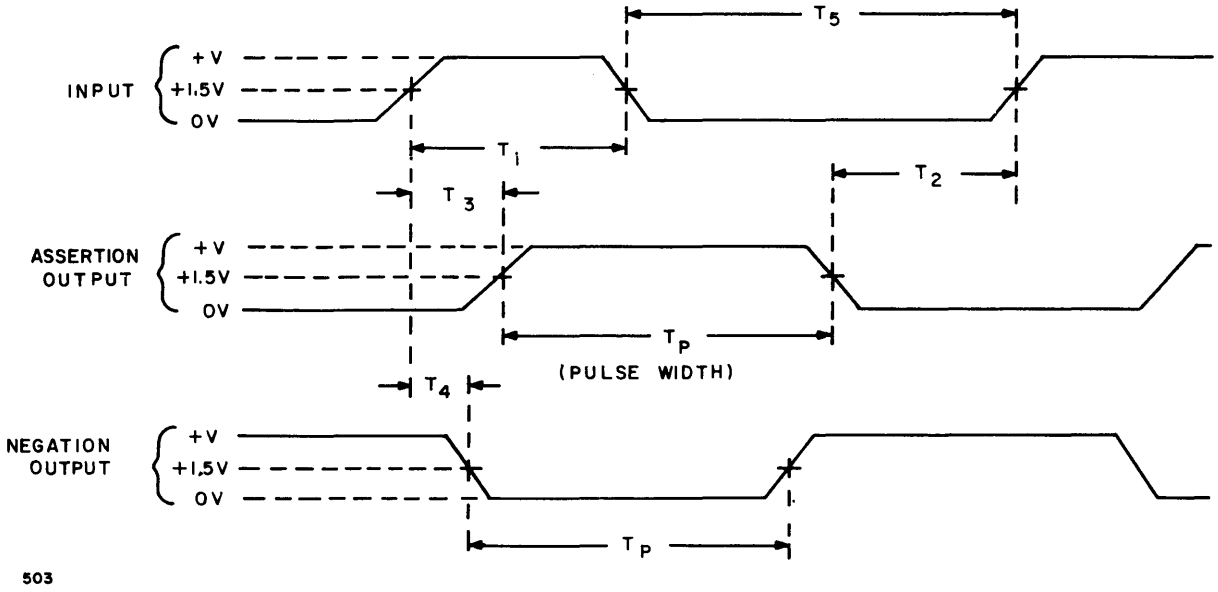
(Refer to Figure 3-12B.3)

Handle Color Code

Yellow

Power Dissipation

0.60w (max)



Input Pulse Width (T_1)	= 50 nsec (min)
Recovery Time (T_2, T_5)	= With Range Control: 150 nsec or 125% of output pulse width, whichever is greater (for 5% reduction in output pulse width) 200 nsec or 200% of output pulse width, whichever is greater (for 1% reduction in output pulse width)
Assertion Circuit Delay (T_3)	= 60 nsec (typ)
Negation Circuit Delay (T_4)	= 30 nsec (typ)
Voltage (V)	= 3.5 volts (min)

Figure 3-12B.3. Timing of the Delay Multivibrator PAC, Model DM-336

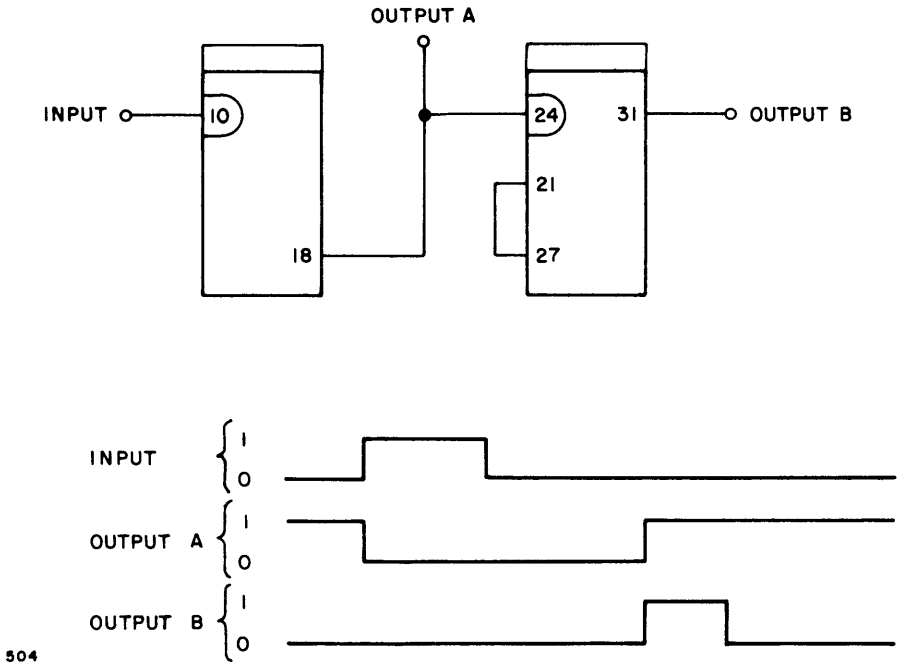


Figure 3-12B.4. Delay Multivibrator PAC,
Model DM-336 Delayed Pulse Generator

3-13 EXPANDABLE NAND PAC, MODEL DN-335

The Expandable NAND PAC, Model DN-335 (Figures 3-13. 1 and 3-13. 2), contains six 3-input NAND gates with nodes. Gate nodes can be connected to the diode cluster nodes of a DC-335 to expand the number of gate inputs.

Each gate performs the NAND function for positive logic, (+6v = ONE, 0v = ZERO). For negative logic, it becomes a NOR gate.

Two of the six gates have disconnected collector load resistors which are available at the PAC terminals. Outputs of these gates can be tied together, using one load resistor, without decreasing the output drive capability.

A detailed description of the basic NAND circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

Inputs. -- When all inputs to a gate are at +6v or disconnected, the output is at ground. When any input is at ground, the output is +6v.

Node. -- By connecting this point to the nodes of diode clusters, the number of gate inputs can be expanded. The connecting wire between nodes should not be cabled, and lead length should be kept under 3 inches.

Load. -- This point is internally connected through a collector load resistor to +6v and is a collector termination for a collector output.

Collector Output. -- Every active collector output must be connected to a load or a standard gate output.

Output. -- Each output terminal is internally connected to a collector load resistor. If an output is connected to load points or other outputs, the output drive capability of the structure is reduced.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Fan-In

Refer to Section II.

Output Drive Capability

8 unit loads

Outputs in Parallel

Refer to Section II.

Circuit Delay

(Measured at +1. 5v, averaged over two stages)

30 nsec (max)

Current Requirements

+6v: 75 ma (max)

Power Dissipation

0. 45w (max)

Handle Color Code

Red

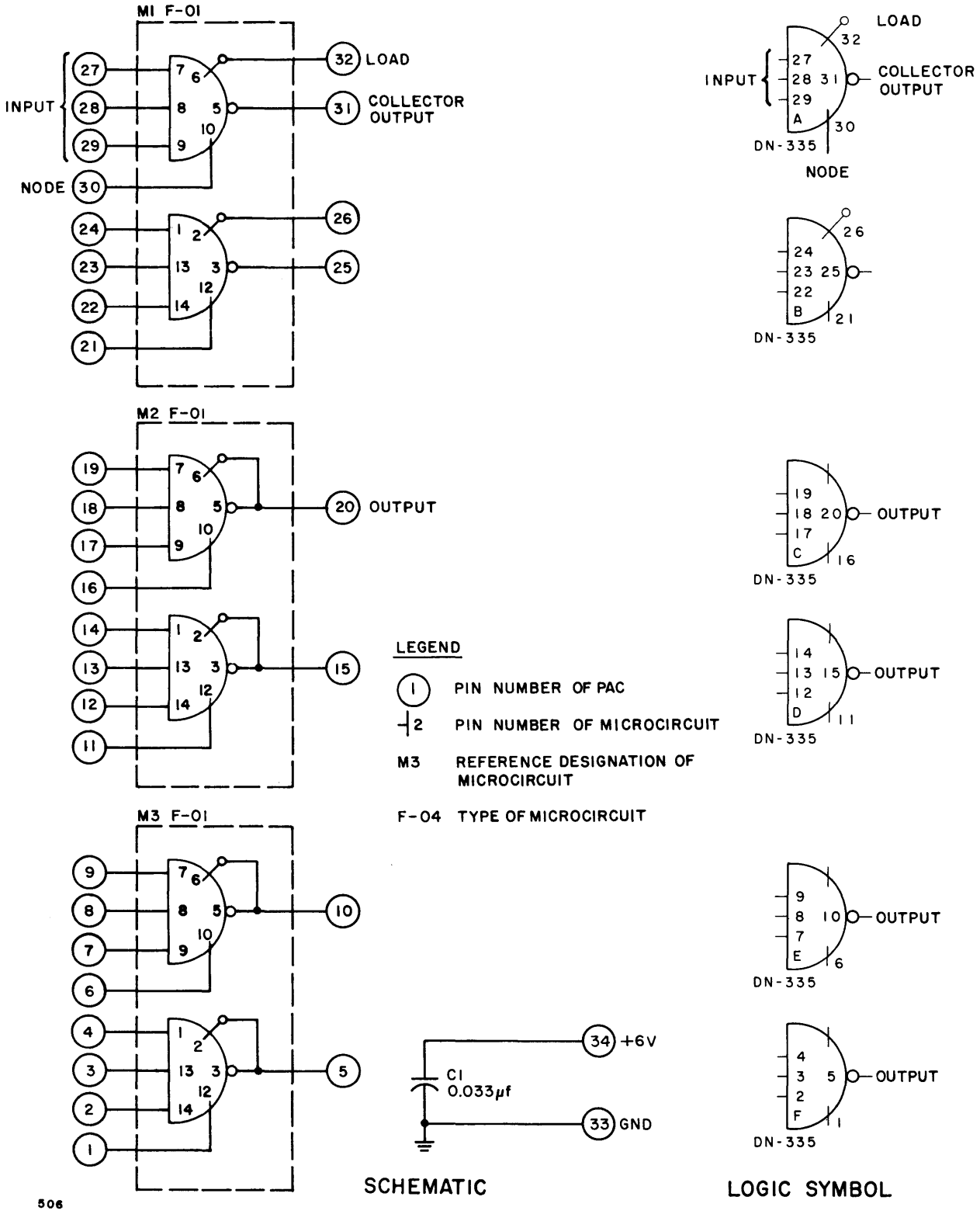
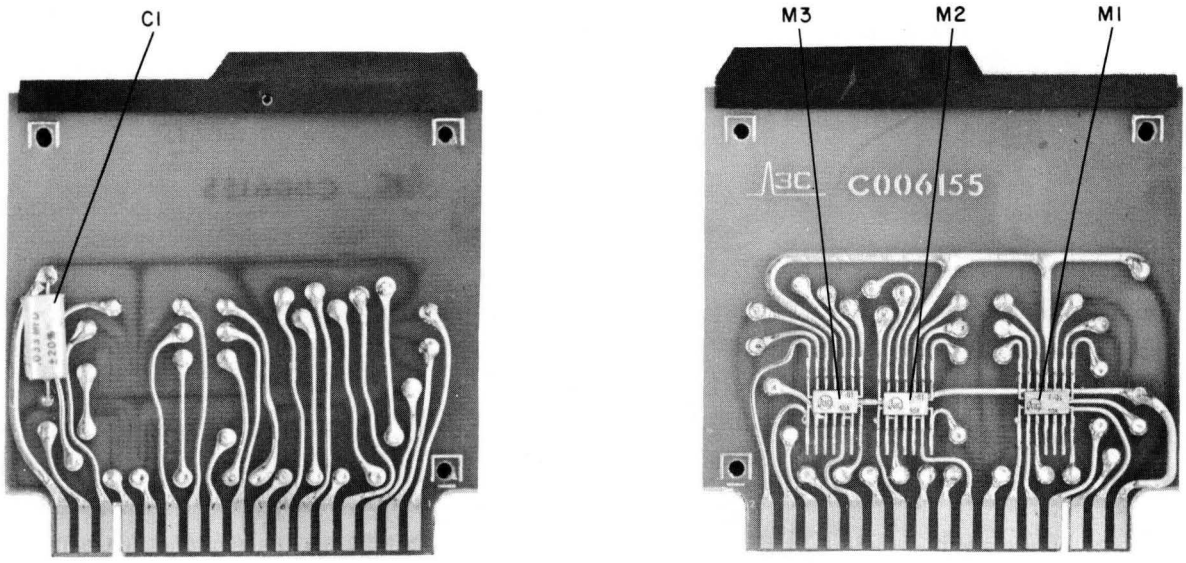


Figure 3-13. 1. Expandable NAND PAC, Model DN-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M3	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-13.2. Expandable NAND PAC, Model DN-335, Parts Location and Identification

APPLICATIONS

The NAND gates operate on levels, pulses, or combinations of both. Two gates can be wired back-to-back to form a dc set-reset flip-flop.

The two gates with separate load outputs form standard NAND gates when the load and collector output terminals are connected. When the collector outputs of these gates are connected in parallel as in Figure 3-13.3, the AND-OR-INVERT function is performed.

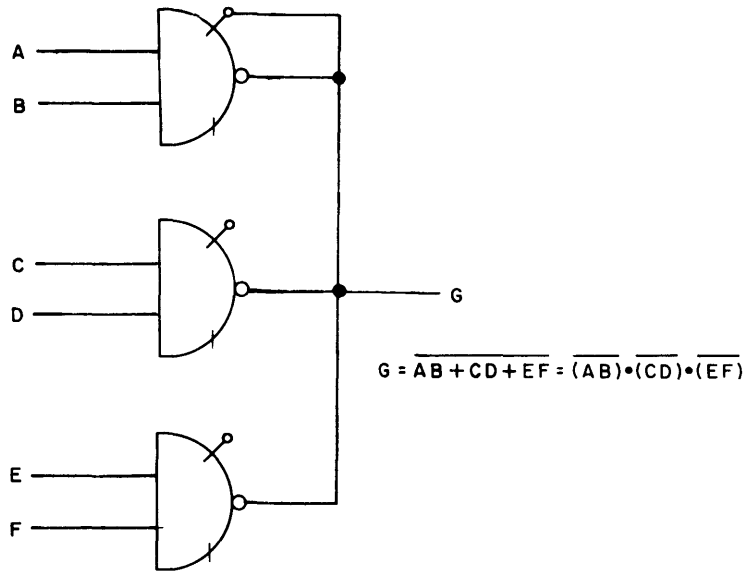


Figure 3-13.3. Gates Used in Parallel

3-14 EXCLUSIVE-OR PAC, MODEL EO-335

The Exclusive-OR PAC, Model EO-335 (Figures 3-14. 1 and 3-14. 2), contains five independent gate structures and one NAND gate. Each gate structure, consisting of a pair of two-input NAND gates and an inverter, performs the AND-OR and the AND-OR-INVERT functions. Gate structures may be used to sense the exclusive-OR and equality functions of two double-ended binary inputs.

INPUT AND OUTPUT SIGNALS

Inputs. -- The logical response of a gate structure to input combination is illustrated in Figure 3-14. 3.

Output 1 and Output 2. -- The two outputs from each gate structure are always opposite in polarity.

Output. -- The output of the single NAND gate is opposite in polarity to the input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Output Drive Capability

Output 1:	8 unit loads each
Output 2:	3 unit loads each
Output (NAND gate):	8 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

Output 1:	60 nsec (max)
Output 2:	30 nsec (max)
Output (NAND gate):	30 nsec (max)

Current Requirements

+6v: 130 ma (max)

Power Dissipation

0. 78w (max)

Handle Color Code

Purple

APPLICATIONS

Two logical configurations for sensing the exclusive-OR and equality of two inputs are illustrated in Figure 3-14. 4.

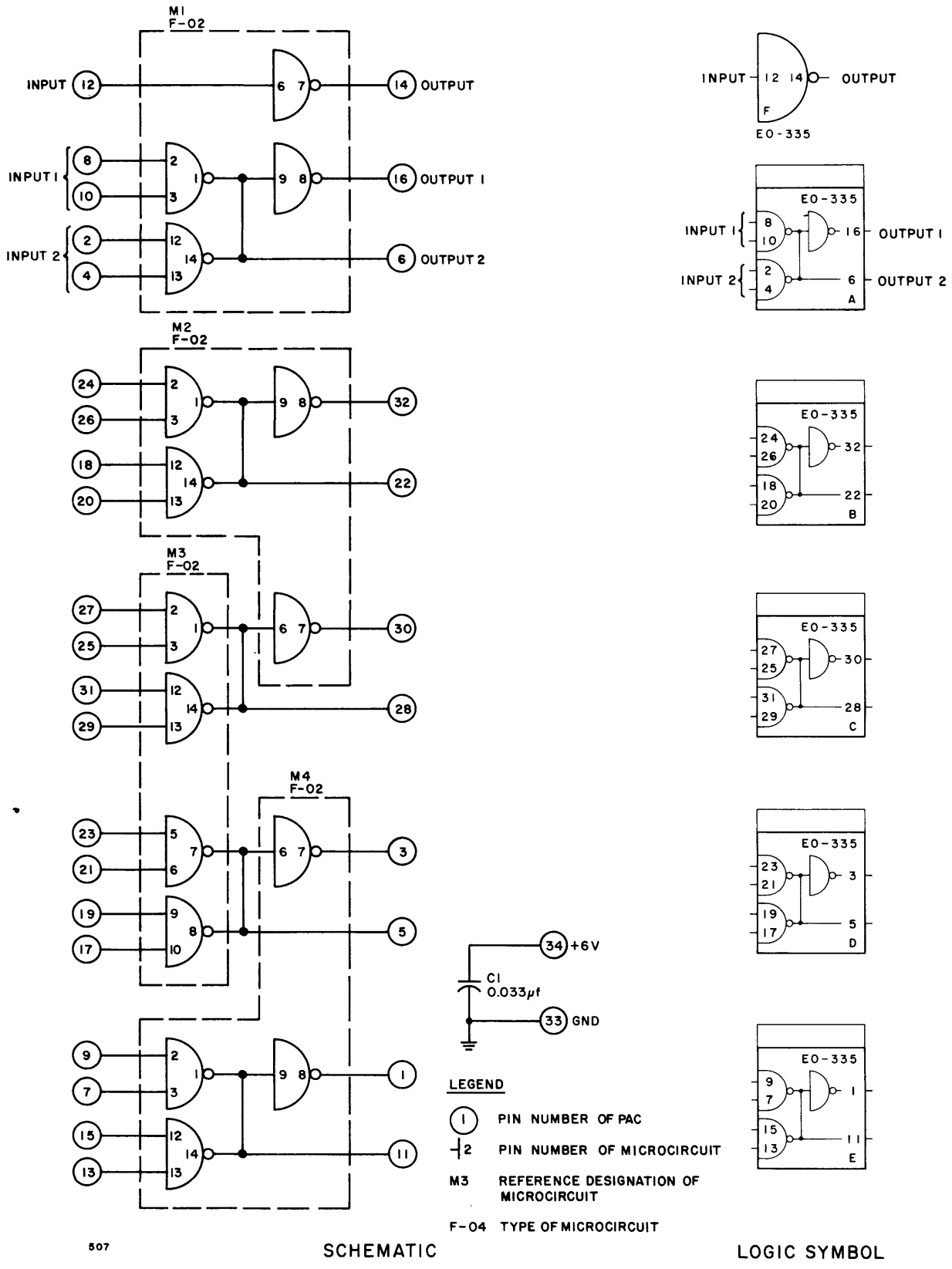
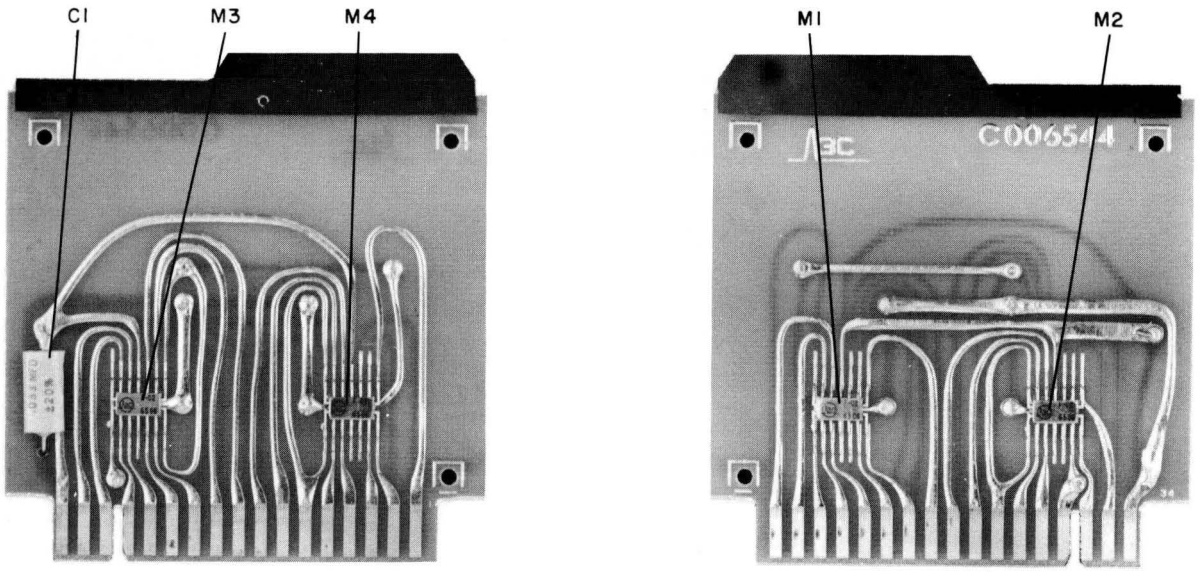


Figure 3-14.1 Exclusive OR PAC, Model EO-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M4	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-14.2. Exclusive OR PAC, Model EO-335,
Parts Location and Identification

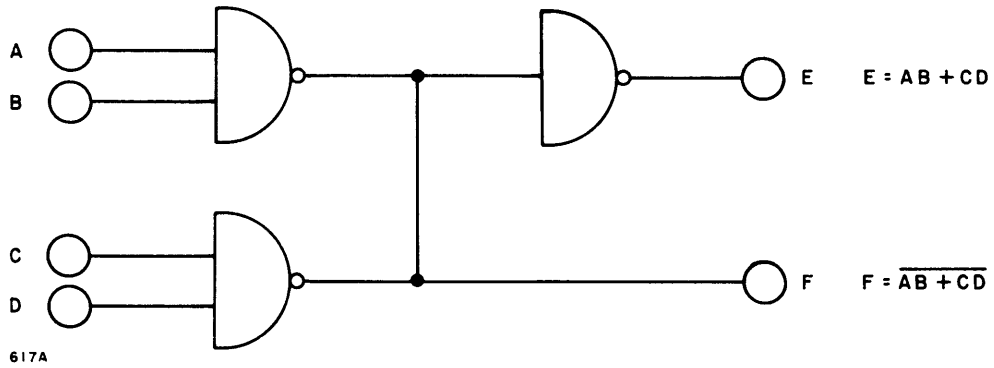


Figure 3-14.3. Logic of EO-335 Gate Structure

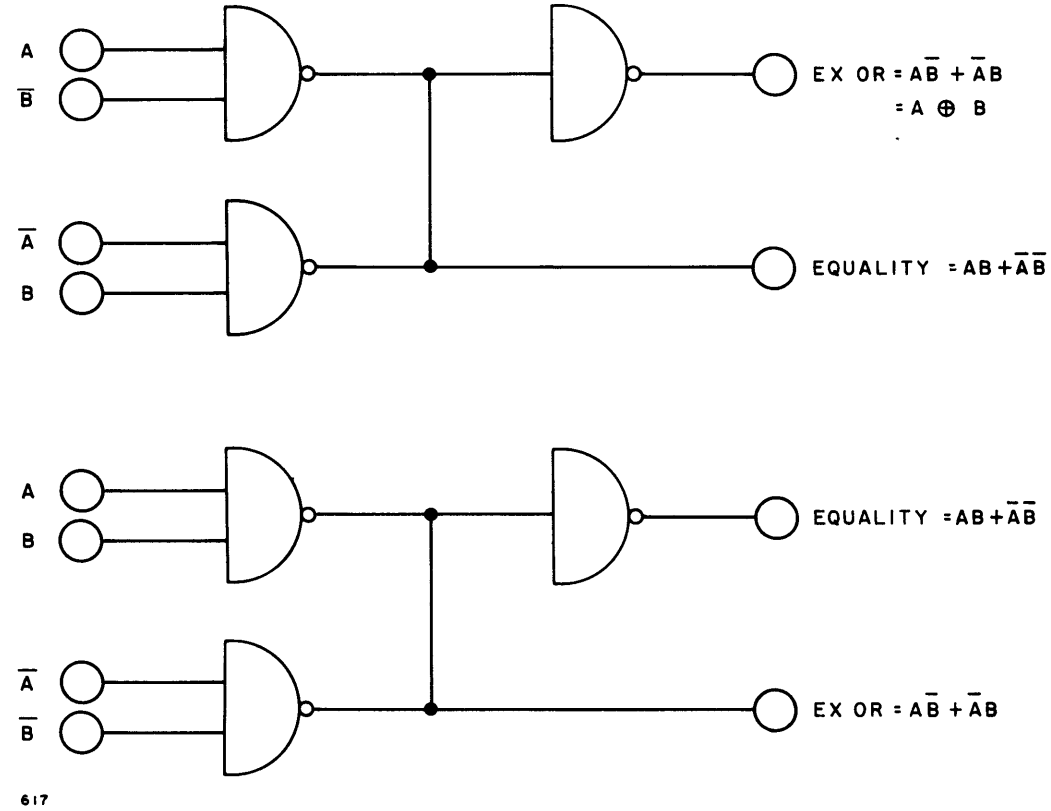


Figure 3-14.4. Exclusive OR and Equality Functions

3-15 GATED FLIP-FLOP PAC, MODEL FA-335

The Gated Flip-Flop PAC, Model FA-335 (Figures 3-15. 1 and 3-15. 2) contains four independent flip-flops. A versatile input structure allows control from a variety of levels and pulses. Typical applications are storage, counting and shifting, and control.

A detailed description of the basic μ-PAC flip-flop circuit appears in Section II.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset. -- A signal at logic ZERO for 80 nsec or longer on a dc set (or reset) input will set (or reset) the flip-flop.

Common Reset. -- A signal at logic ZERO for 80 nsec or longer on the common reset input clears all four stages simultaneously.

Set Control and Reset Control. -- Logic ONE is the enabling level on the control inputs. Refer to Section II for detailed information on flip-flop timing and control.

Clock. -- The flip-flop changes state on the negative (ONE to ZERO) transition of the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Control inputs:	1 unit load each
Common reset:	3 unit loads
Clock:	1 unit load each

Output Drive Capability

8 unit loads each

Circuit Delay

Clock input to set or reset output
60 nsec (max)

DC set input to dc set output, or dc reset input to reset output
80 nsec (max)

DC set input to reset output, or dc reset input to set output
60 nsec (max)

Current Requirements

+6v: 100 ma (max)

Power Dissipation

0. 60w (max)

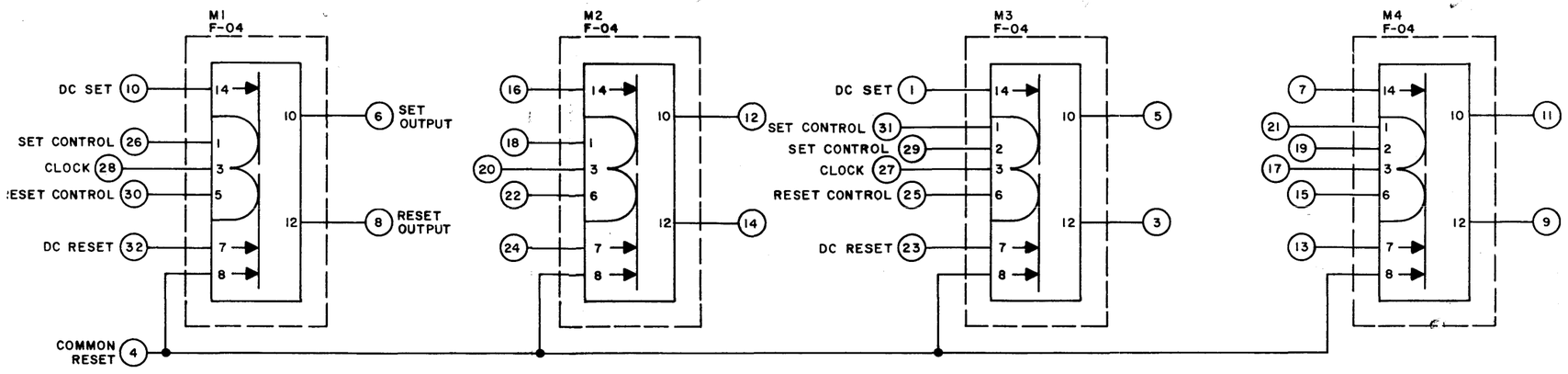
Handle Color Code

Blue

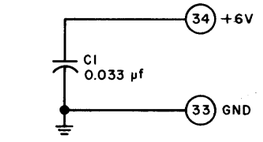
APPLICATIONS

The FA-335 can be used as a counter (Figure 3-15. 3) or as a shift register (Figure 3-15. 4) The method of parallel information drop-in is shown in Figure 3-15. 5.

Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones. For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation.



SCHEMATIC



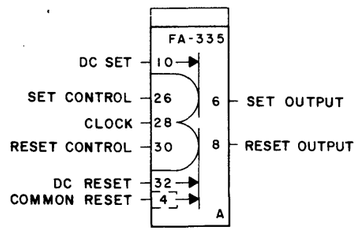
LEGEND

(1) PIN NUMBER OF PAC

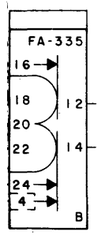
2 PIN NUMBER OF MICROCIRCUIT

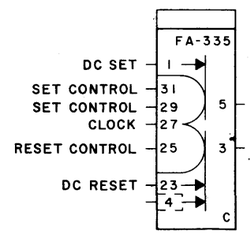
M3 REFERENCE DESIGNATION OF MICROCIRCUIT

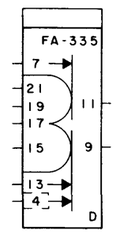
F-04 TYPE OF MICROCIRCUIT



LOGIC SYMB



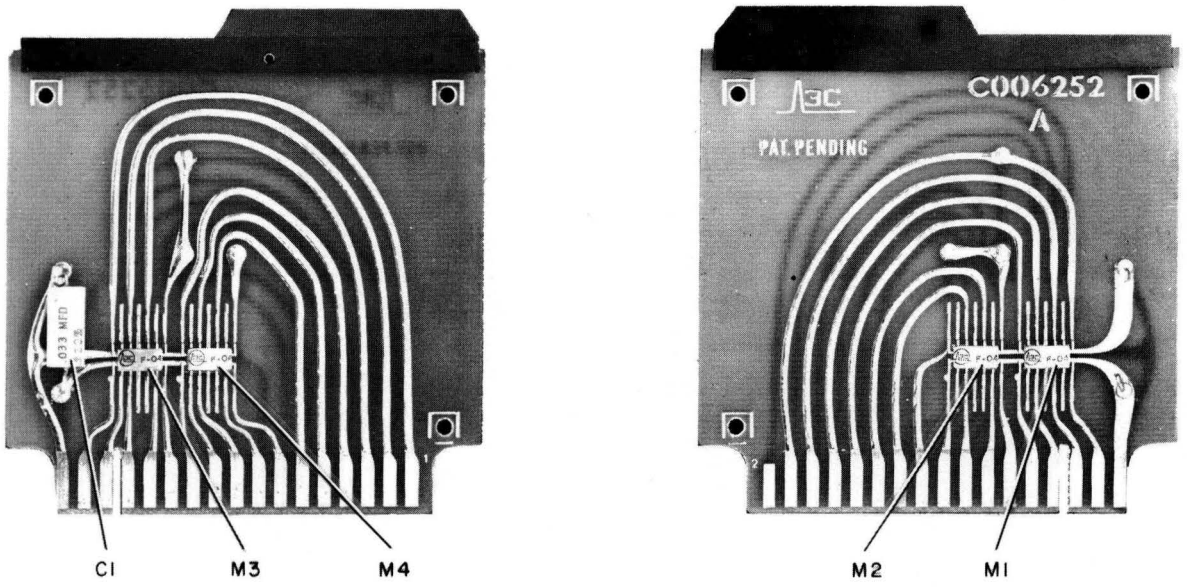




Note: Refer to Figure 3-15.1A for PACs with Ser. Nos. 831 and beyond

Figure 3-15.1. Gated Flip-Flop PAC, Model FA-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-15-2. Gated Flip-Flop PAC, Model FA-335, Parts Location and Identification

| Note: Refer to Figure 3-15.2A for PACs with Ser. Nos. 831 and beyond

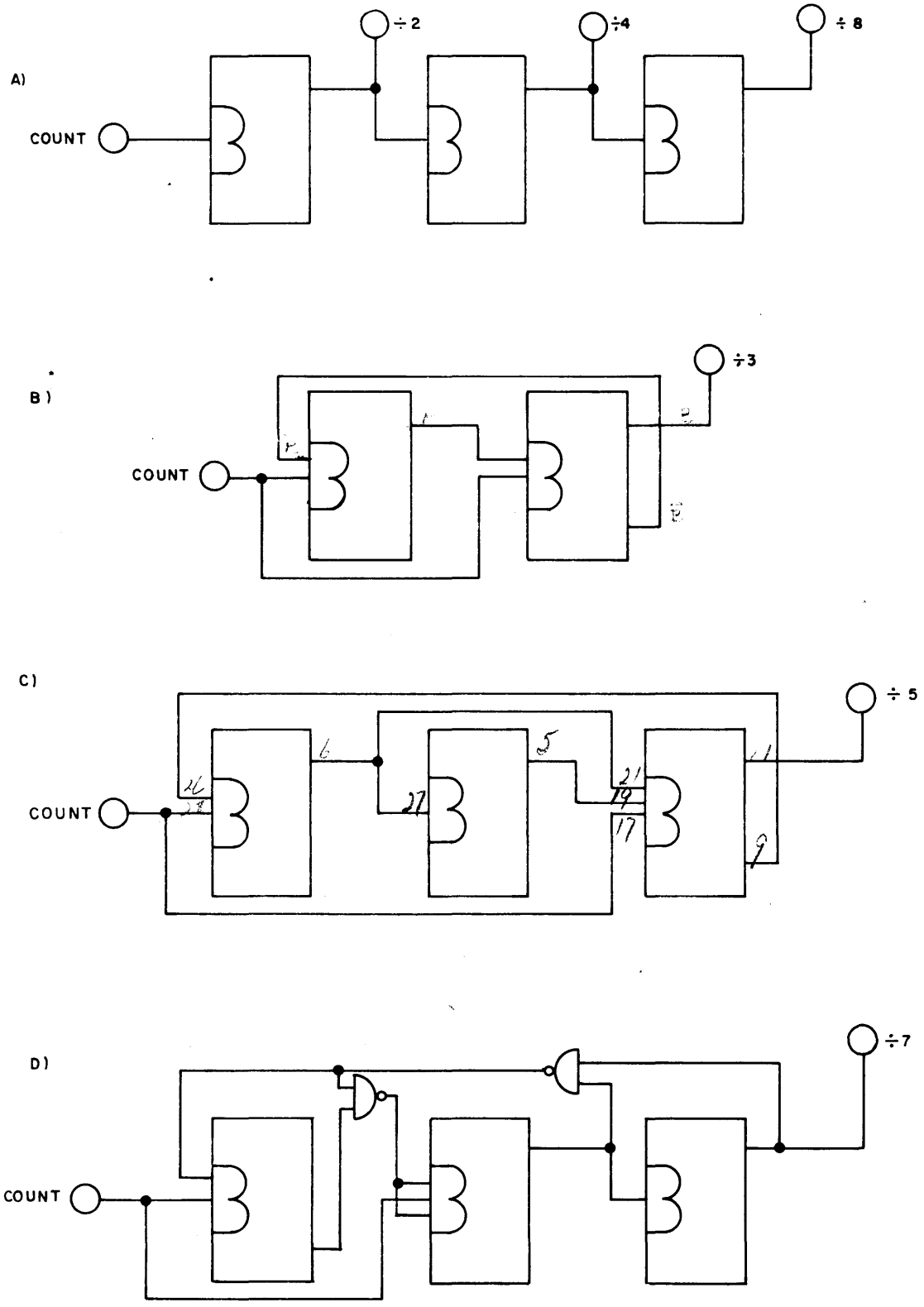


Figure 3-15.3. Gated Flip-Flop PAC, Model FA-335, Counter Operation

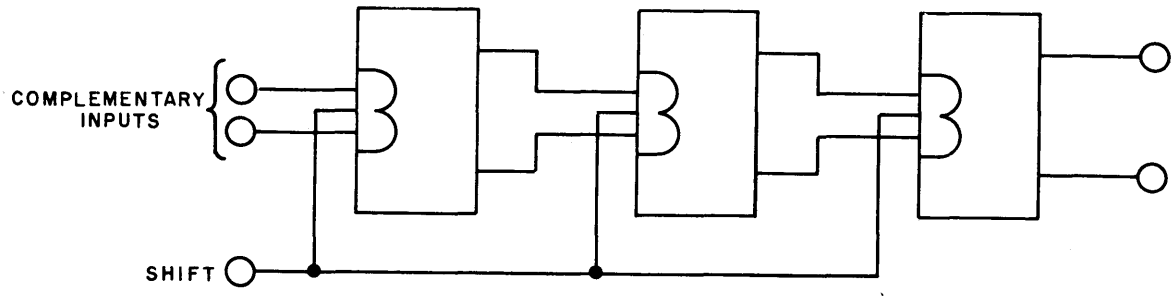


Figure 3-15.4. Gated Flip-Flop PAC, Model FA-335, Shift Register Operation

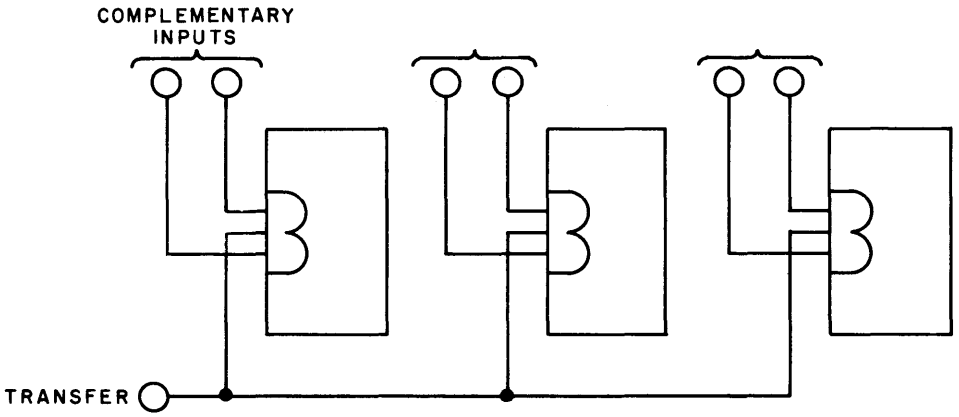


Figure 3-15.5. Gated Flip-Flop PAC, Model FA-335, Parallel Information Drop-In

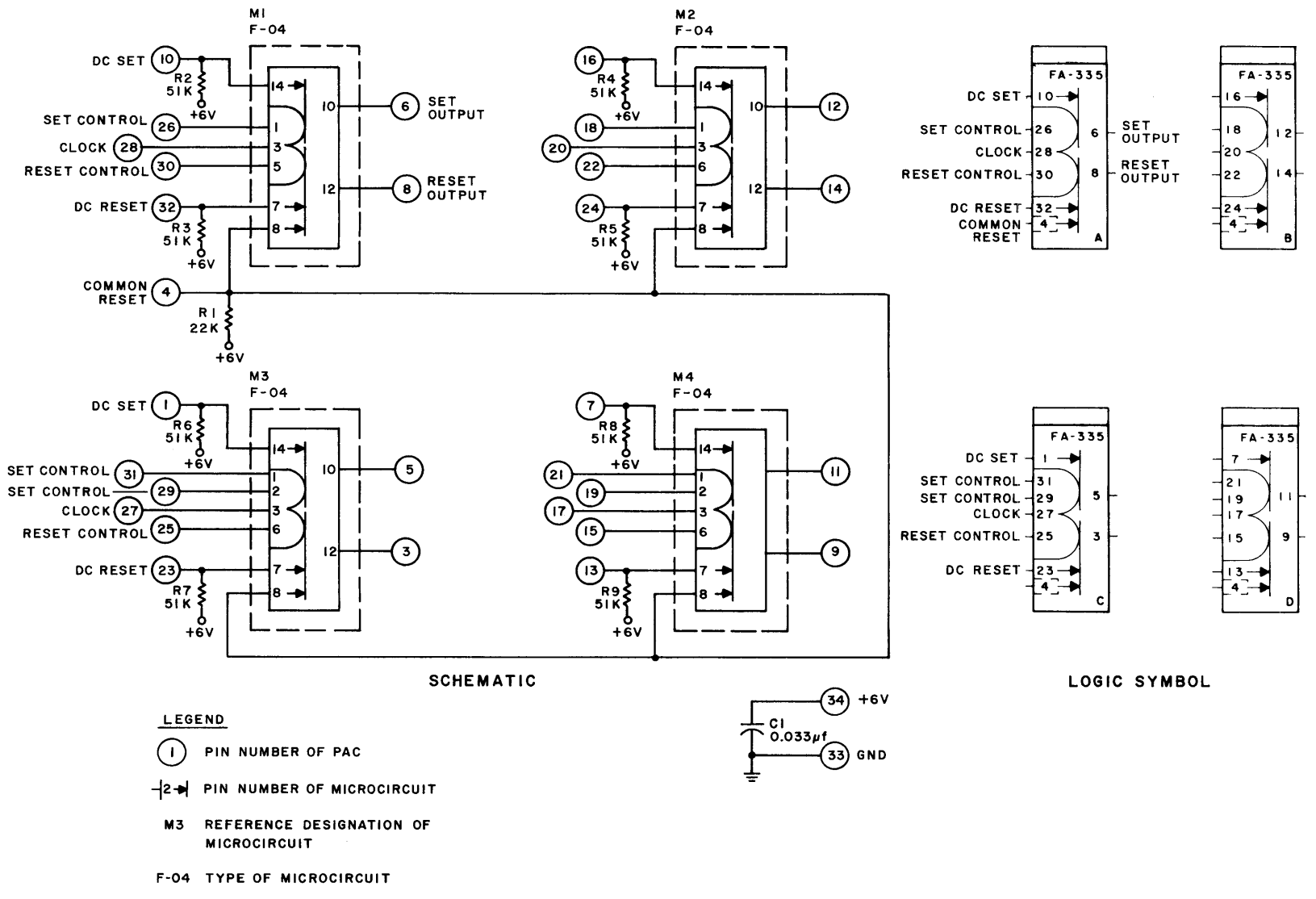
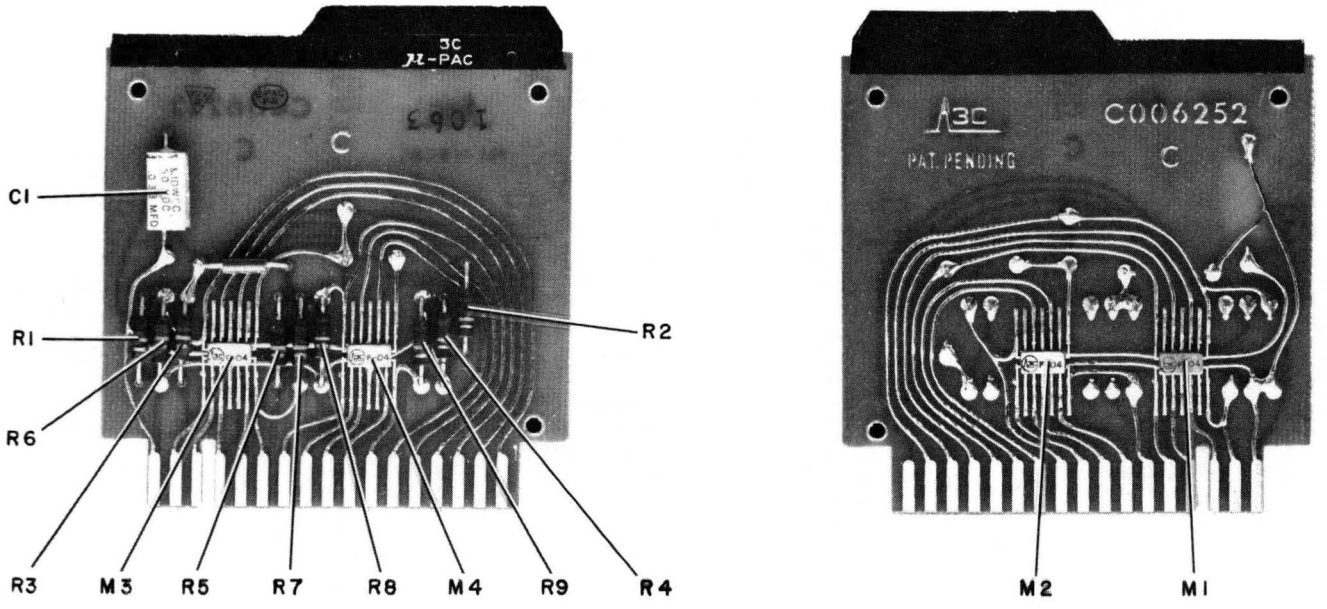


Figure 3-15.1A. Gated Flip-Flop PAC, Model FA-335 (Ser. No. 831 and beyond), Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4 w	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4 w	932 007 090

Figure 3-15.2A. Gated Flip-Flop PAC, Model FA-335 (Ser. No. 831 and beyond)
Parts Location and Identification

3-16 BASIC FLIP-FLOP PAC, MODEL FF-335

The Basic Flip-Flop PAC, Model FF-335 (Figures 3-16.1 and 3-16.2), contains eight independent flip-flop circuits. Each circuit is formed by two separate NAND gates wired back to back internally. The output of one gate is connected to the input of the other. A detailed description of the NAND circuit is contained in Section II. Figure 3-16.3 illustrates the logic operation. Each stage of the FF-335 has a dc set and a dc reset input, and a set and reset output.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset. -- A signal at logic ZERO (ground) for 60 nsec or longer on either input will set or reset the flip-flop.

SPECIFICATIONS

Frequency of Operation (System)	Output Drive Capability
DC to 5 mc	7 unit loads each
Input Loading	Circuit Delay
DC inputs: 1 unit load each	60 nsec (max)
DC Set and Reset Timing	Current Requirements
60 nsec (min) at logic ZERO to set or reset	+6v: 100 ma (max)
Handle Color Code	Power Dissipation
Blue	0.60w (max)

APPLICATIONS

The FF-335 PAC is used for economical implementation of logic operations, such as input-output registers, storage and buffering applications. Control of data into and out of the register can be easily accomplished by using gating PACs in the μ-PAC line. Figure 3-16.4 illustrates how an FF-335 stage can be used for data storage, with inputs and outputs from several locations.

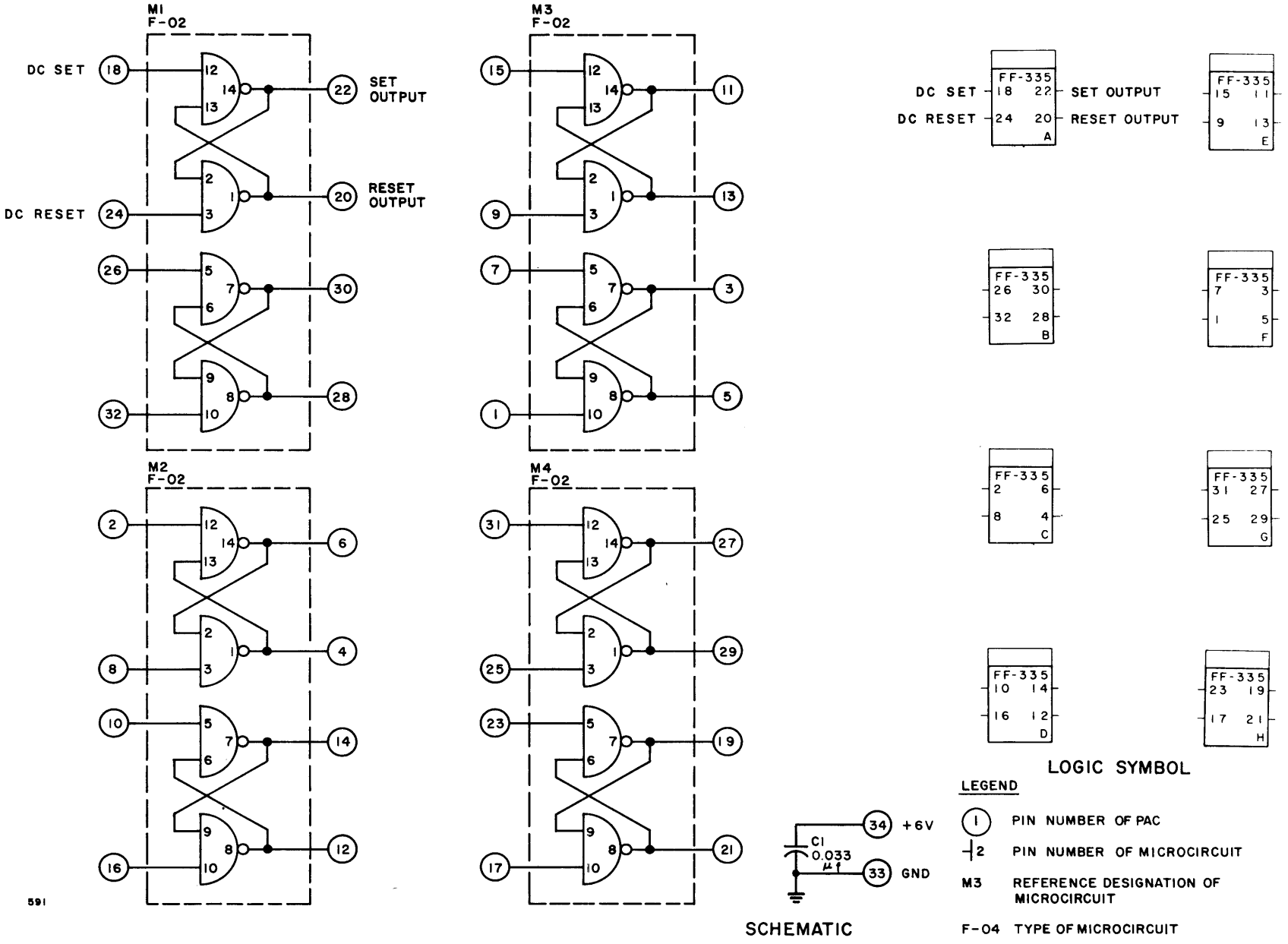
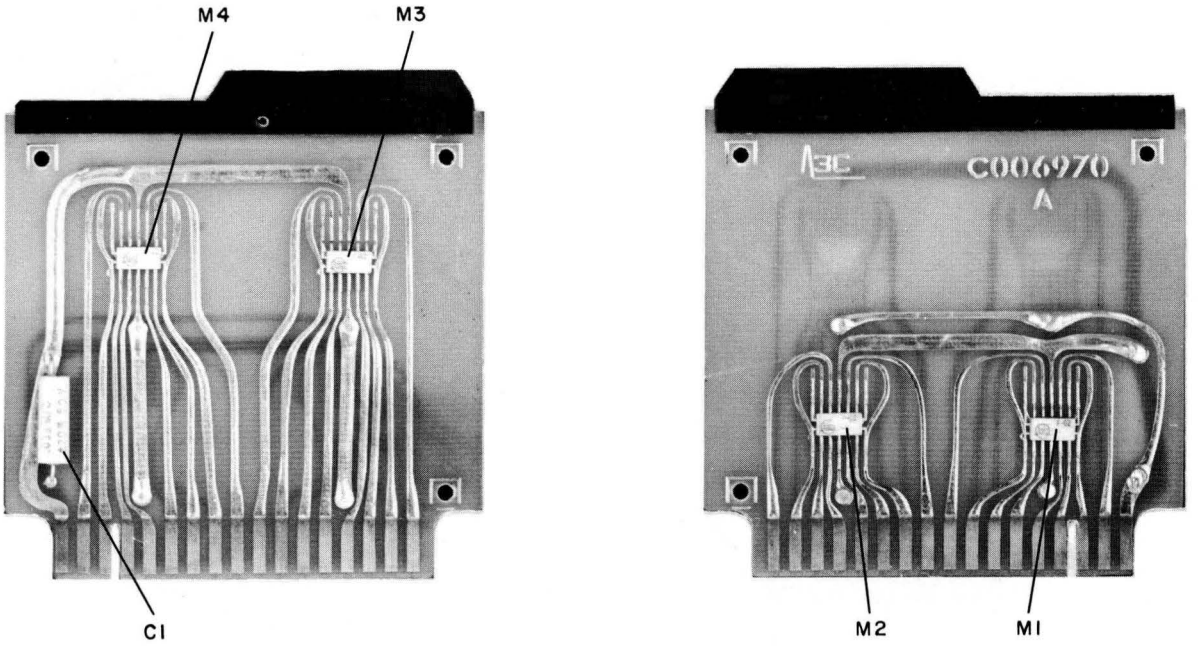


Figure 3-16.1. Basic Flip-Flop PAC, Model FF-335, Schematic Diagram and Logic Symbol

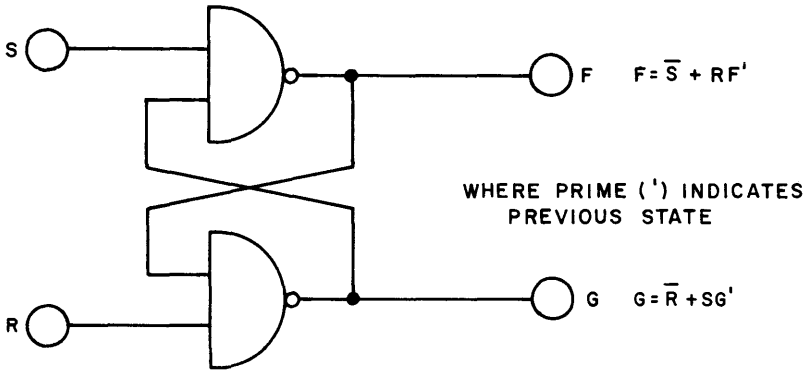
Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-16.2. Basic Flip-Flop PAC, Model FF-335, Parts Location and Identification



TRUTH TABLE

S	R	F	G
0	0	1	1
0	1	1	0
1	0	0	1
1	1	*	*

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*REMAIN IN PREVIOUS STATE

Figure 3-16.3. Basic Flip-Flop PAC, Model FF-335, Logic Operation

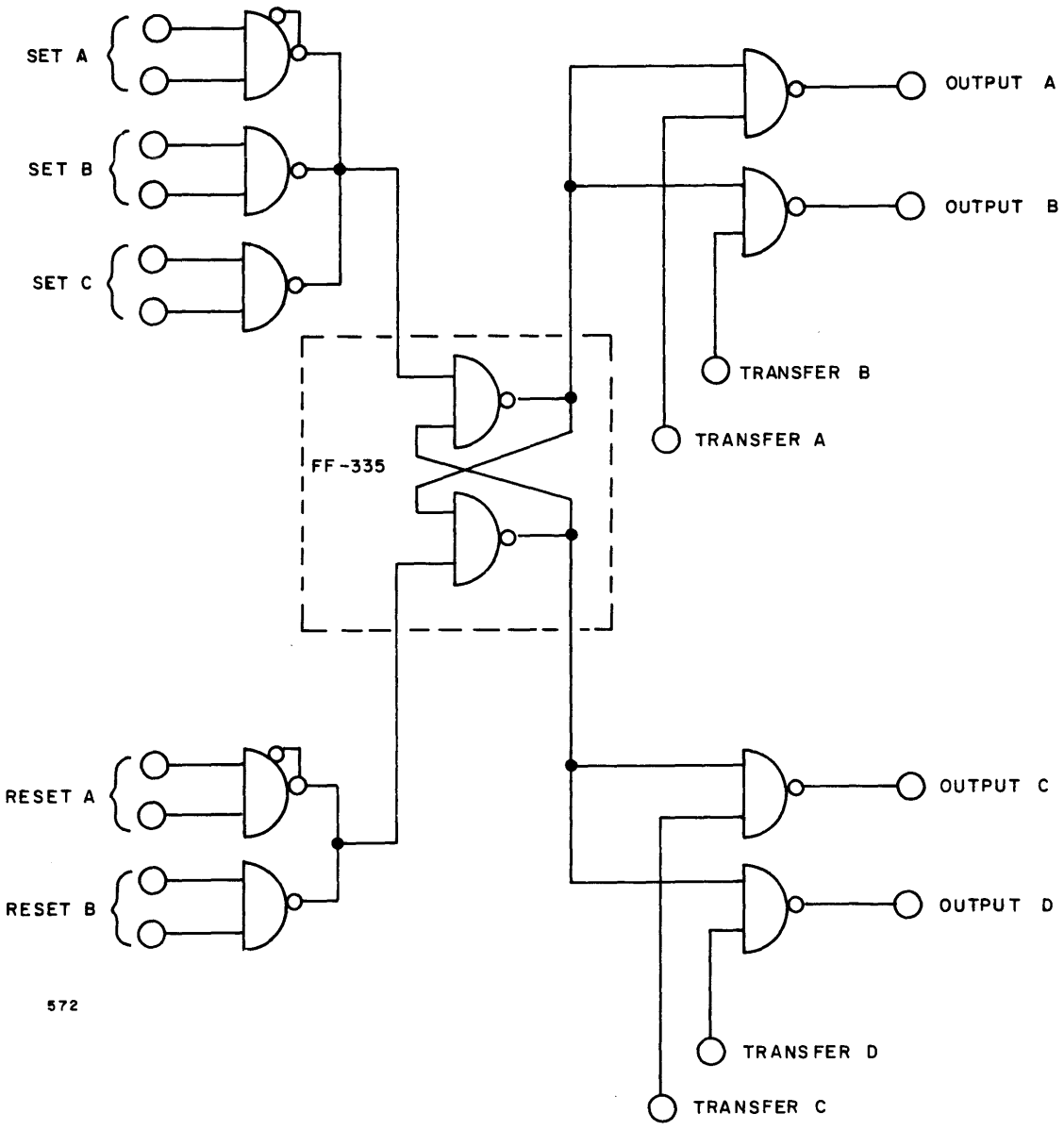


Figure 3-16.4. Basic Flip-Flop PAC, Model FF-335, Input and Output Logic

3-17 TAPER PIN JUMPER LEAD SET, MODEL JT-330

The Taper Pin Jumper Lead Set, Model JT-330, contains 420 assorted jumper leads for use on μ-BLOCs with taper pin connectors. The leads are composed of plastic insulated No. 24 AWG stranded wire with gold-plated AMP No. 53 series taper pins at each end.

The selection of lead lengths and colors is based upon experimentation in wiring, tracing signals, and troubleshooting digital equipment.

Assorted jumper leads are described in Table 3-17.1 along with a recommended color code for each PAC type. The colors apply to the PAC outputs.

Table 3-17.1.
Jumper Lead Set

Wire Color	Quantity (Per Lead Length*)				Quantity (Per Color)	Recommended PAC Type
	2 in.	3-1/2 in.	5 in.	6-1/2 in.		
Blue	35	35	30	15	115	Flip-flops
Red	35	35	30	15	115	Gates
Yellow	25	25	20	10	80	Amplifiers, input/ output circuits
Orange	10	10	5	5	30	Clocks, one-shots
White	10	10	5	5	30	Miscellaneous
Black	30	20	-	-	50	(Ground)
Total	145	135	90	50	420	

*Length is from tip to tip of taper pins

3-17A NEGATIVE LOGIC LEVEL CONVERTER PAC, MODEL LC-335

The Negative Logic Level Converter PAC, Model LC-335 (Figures 3-17A.1 and 3-17A.2), contains 10 independent converter circuits. The N-input accepts a negative logic signal (i.e., logic ONE is a negative voltage) for conversion into a standard μ-PAC positive logic signal. The μ-input uses a μ-PAC signal to control or gate the negative logic signal. When the circuit is enabled, there is no logic inversion from the converting input to the output. The operation of the circuit is summarized in Tables 3-17A.1 and 3-17A.2.

Table 3-17A.1.
Logic Truth Table

Negative Logic		Positive Logic
N	μ	Output
0	0	1
0	1	0
1	0	1
1	1	1

For the N-input: Logic ZERO = 0.0v to -1.5v
Logic ONE = -2.8v to -15v (or not connected)

For the μ-input: Logic ZERO = 0.0v to +1.2v
Logic ONE = +3.0v to +6.3v (or not connected)

Table 3-17A.2.
Voltage Truth Table
(With Nominal Voltages)

N	μ	Output
0v	0v	+6v
0v	+6v	0v
-6v	0v	+6v
-6v	+6v	+6v

CIRCUIT FUNCTION

Each level converter consists of a standard NAND gate microcircuit and a level shifter. The converting input (N) drives the emitter of a common base transistor whose base is referenced to -2v. When a logic ZERO (0v) is applied to this input, the emitter of transistor Q1 becomes more positive than the base and Q1 is turned off. This is interpreted as a logic ONE at the NAND gate input. When the converting input is a ONE (negative voltage or not connected), Q1 is turned on, causing the NAND gate output to be +6v.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Logic Levels

Refer to Table 3-17A.1

Input Loading

N-input: 2 ma

μ-input: 1 unit load

Current Requirements

+6v: 125 ma (max)

-6v: 35 ma (max)

Power Dissipation

0.96w (max)

Output Drive Capability

8 unit loads each

Conversion Circuit Delay

(measured from -1.5v of the input to +1.5v of the output)

Positive-going input: 65 nsec (max)

Negative-going input: 45 nsec (max)

Handle Color Code

Red

APPLICATIONS

The LC-335 PAC can be used when converting signals from an S-PAC or H-PAC system to a standard μ-PAC system. This is accomplished by applying the external signal to the N-input; a μ-PAC signal will appear at the output. A control signal from within the μ-PAC system can be applied to the μ-input to gate the external signal (a ONE enables and a ZERO inhibits). If no control is required, the μ-input should be left disconnected.

Each circuit can be used as an inverter for μ-PAC signals by using the μ-input and grounding the N-input.

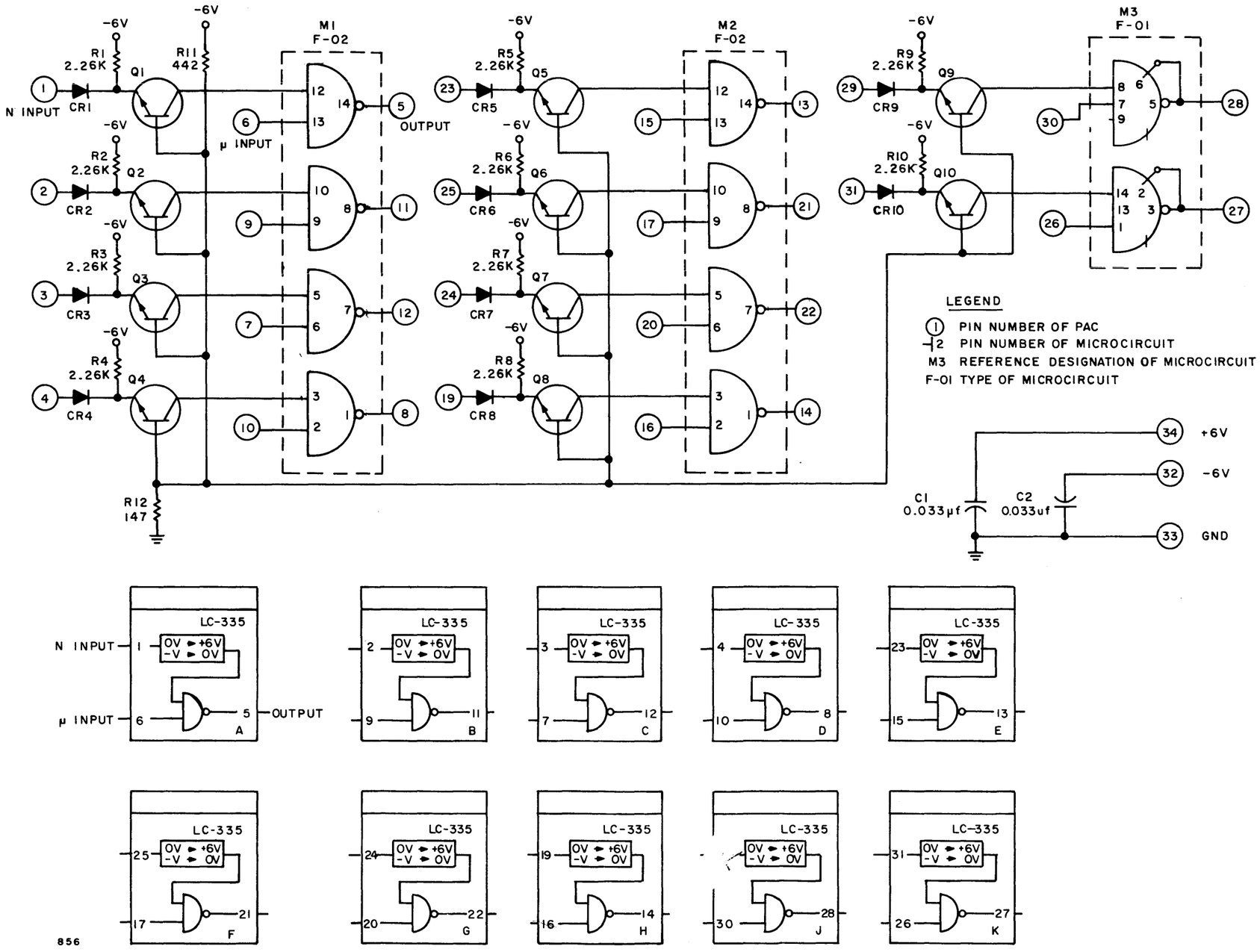
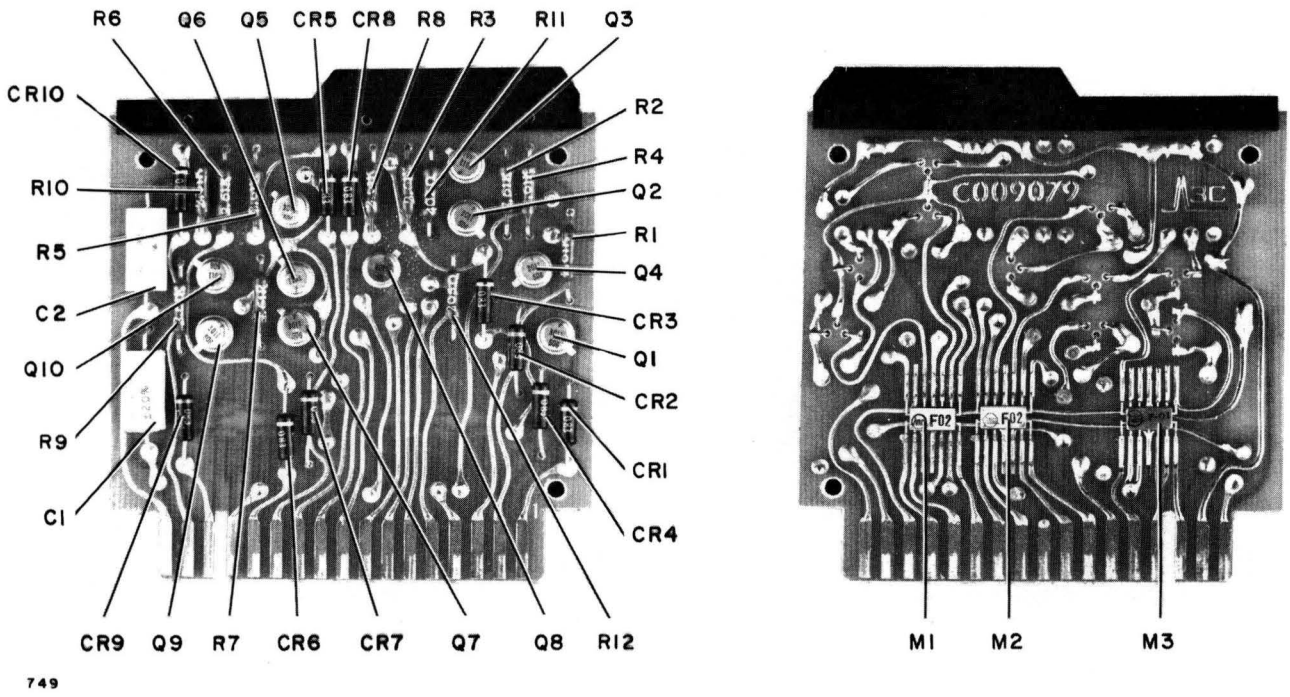


Figure 3-17A.1. Negative Logic Level Converter PAC, Model LC-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M3	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 002
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 006
CR1-CR10	DIODE: Replacement Type 1N914	943 083 001
Q1-Q10	TRANSISTOR	943 722 002
R1-R10	RESISTOR, FIXED, FILM: 2.26 K±2%, 1/8w	932 113 218
R11	RESISTOR, FIXED, FILM: 442 ohms ±2%, 1/8w	932 113 132
R12	RESISTOR, FIXED, FILM 147 ohms ±2%, 1/8w	932 113 109

Figure 3-17A.2. Negative Logic Level Converter PAC, Model LC-335, Parts Location and Identification

3-18 LAMP DRIVER PAC, MODEL LD-330

The Lamp Driver PAC, Model LD-330 (Figures 3-18.1 and 3-18.2), contains 12 independent transistor-driver circuits. The circuit operates from standard μ-PAC signals. Each circuit is capable of switching up to 70 ma of current from a positive supply of up to 20v.

CIRCUIT FUNCTION

Each driver circuit is composed of a single-input NAND gate microcircuit which drives an output transistor. When the input to the circuit is a ZERO (0v), the transistor is turned on and the output will be at ground. When the input is a ONE, the transistor is turned off, and the output will be the same as the external positive supply voltage. The operation is summarized in Table 3-18.1.

The peak or maximum in-rush current on the output transistor must be limited to 150 ma. If the load (such as a lamp) does not limit the initial current, then an external series resistor must be used between the driver and the external voltage source.

Table 3-18.1
Truth Table

Input	Output	External Lamp
0v	0v	Lamp on
+6v	External supply voltage	Lamp off

INPUT AND OUTPUT SIGNALS

Input. -- This point is a NAND gate input.

Output. -- This point is connected to the positive terminal of an external load.

Return. -- This point should be connected to the negative side of the external supply voltage.

SPECIFICATIONS

Frequency of Operation

DC to 100 kc (max)

Input Loading

1 unit load

Current Requirements

+6v: 130 ma (max)

Power Dissipation

0.78w (max)

Output Drive Capability

70 ma at 20v (quiescent)
150 ma at 20v (peak)

Handle Color Code

Orange

APPLICATIONS

Figure 3-18.3 illustrates a typical application, using the LD-330 to drive a remote lamp. The circuit is shown operating at 10v with approximately 40 ma. An external 200-ohm resistor limits the peak in-rush current to 90 ma when the lamp is cold. As the lamp draws current, it heats up until the filament reaches its quiescent resistance of 250 ohms.

NOTE

When a circuit is being used to drive an indicator lamp, an external series resistor must be used to limit the peak current to 150 ma.

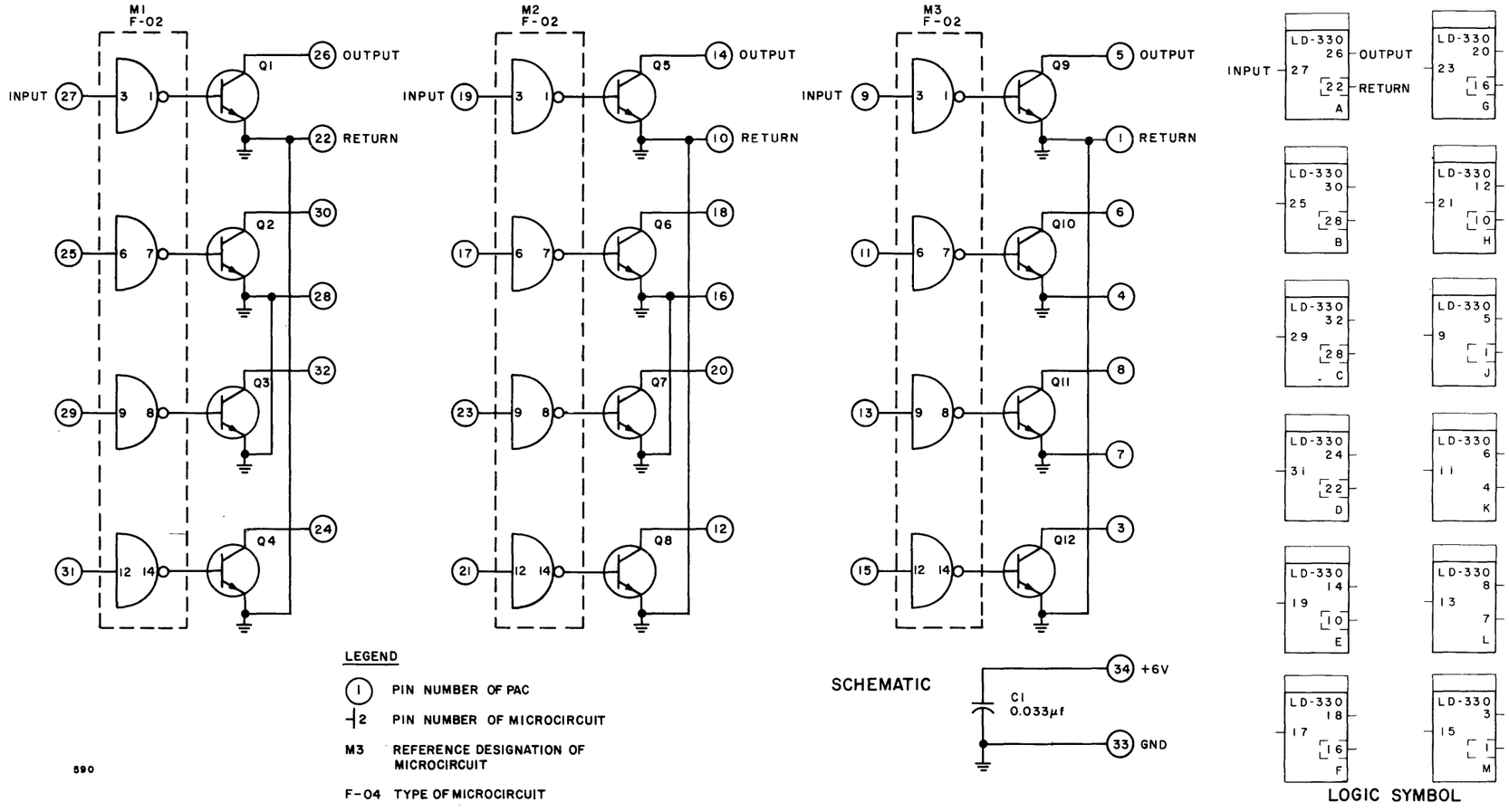
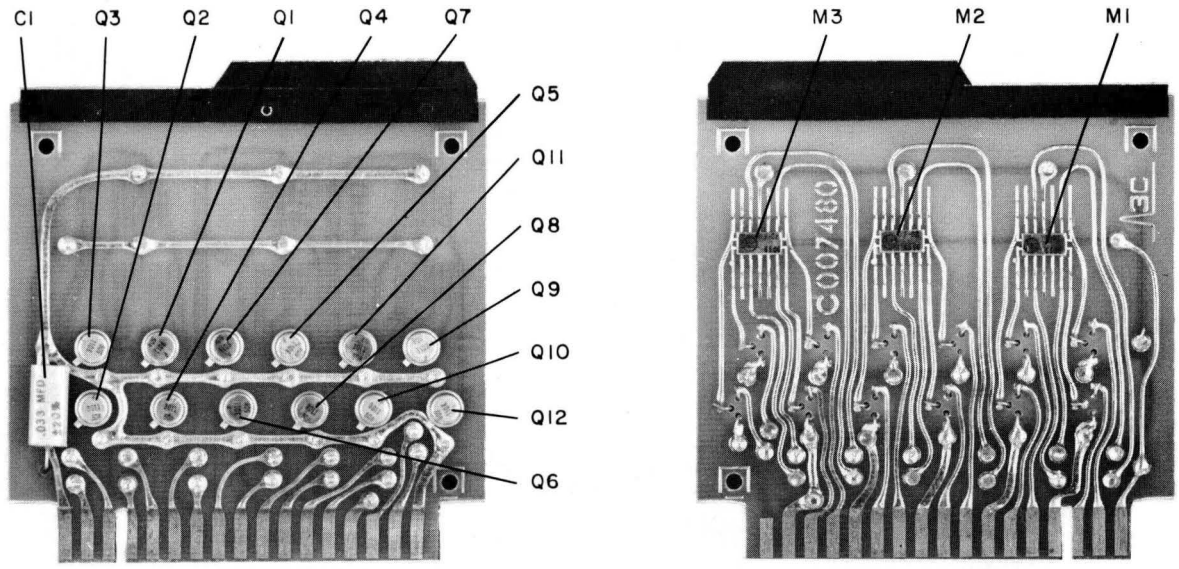


Figure 3-18.1. Lamp Driver PAC, Model LD-330, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
Q1-Q12	TRANSISTOR	943 722 002

Figure 3-18.2. Lamp Driver PAC, Model LD-330, Parts Location and Identification

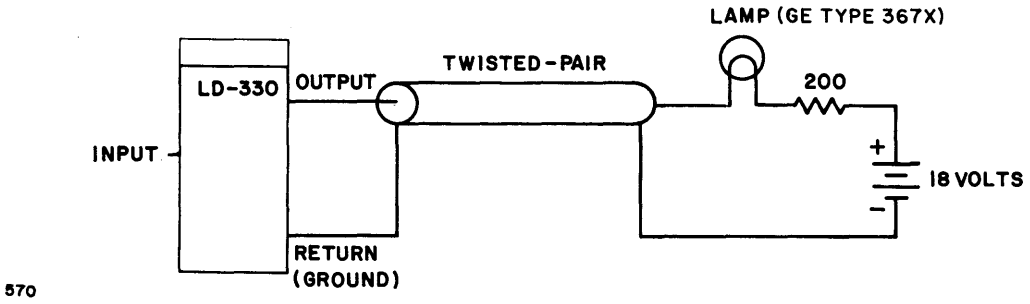


Figure 3-18.3. Lamp Driver PAC, Model LD-330, Driving a Remote Lamp

3-18A HIGH-DRIVE LAMP DRIVER PAC, MODEL LD-331

The High-Drive Lamp Driver PAC, Model LD-331 (Figures 3-18A.1 and 3-18A.2), contains eight independent lamp driver circuits, each of which is capable of switching up to 300 ma of current from a positive supply of up to 35v. The circuit operates from standard μ-PAC signals.

CIRCUIT FUNCTION

Each driver circuit is composed of a microcircuit dual-input NAND gate which drives a discrete output transistor. The filament lamp is connected in series between the collector of the transistor (Output) and the external positive supply voltage.

When the output of the NAND gate is a ONE (+6v), the transistor is turned on and the lamp illuminated. When the output of the NAND gate is a ZERO (0v), the transistor is turned off and the lamp extinguished.

INPUT AND OUTPUT SIGNALS

Input. -- This point is a NAND gate input.

Output. -- The external lamp is connected in series between this point and the positive terminal of an external supply.

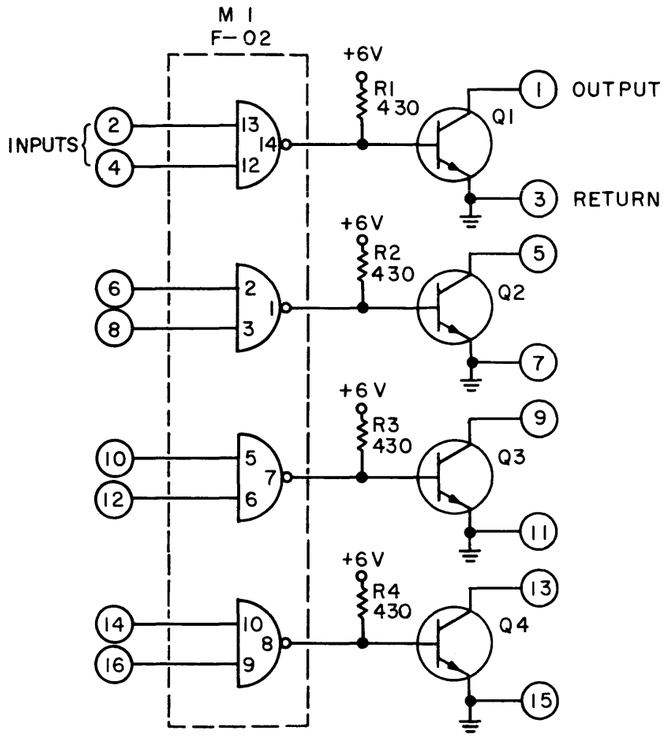
Return. -- This point should be connected to the negative side of the external supply voltage.

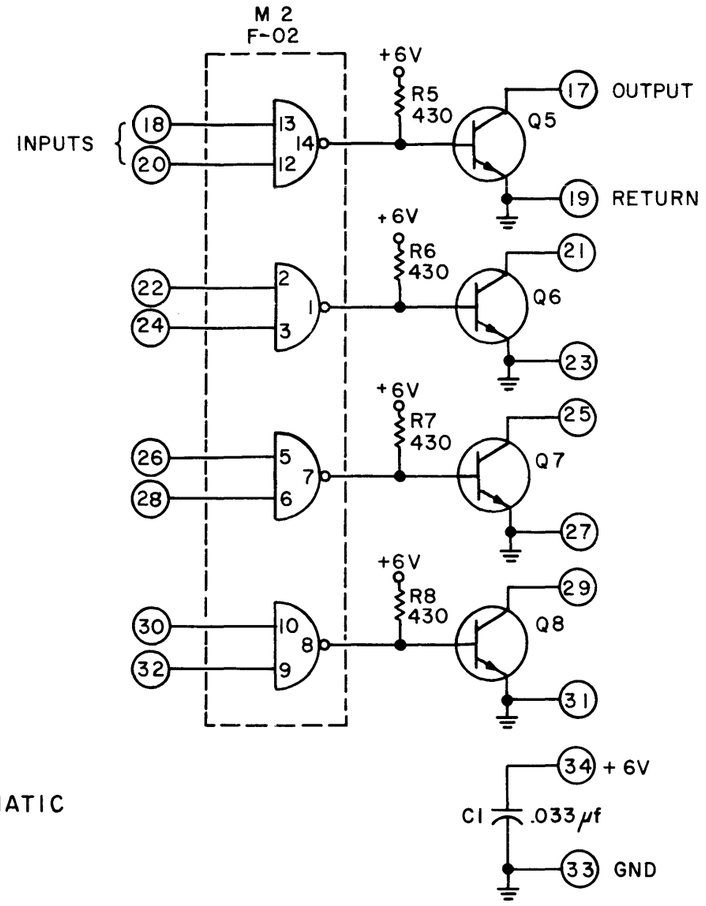
SPECIFICATIONS

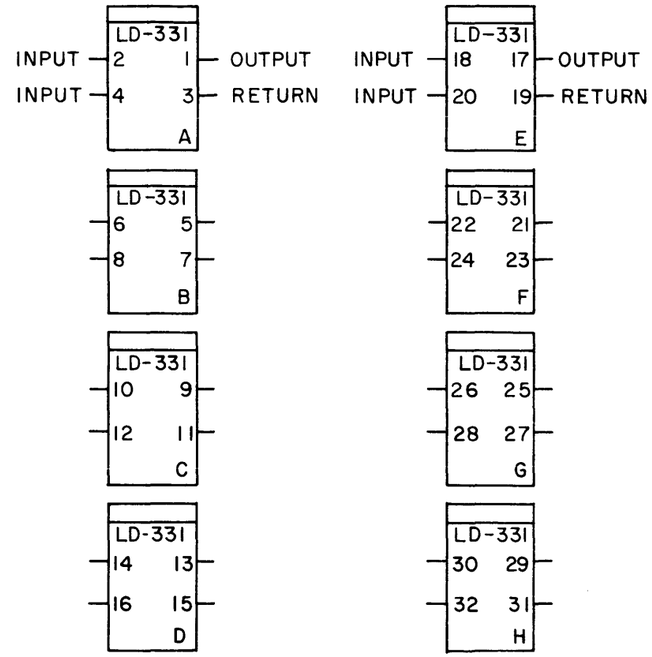
Frequency of Operation	Output Drive Capability
DC to 10 kc (max)	300 ma at 35v
Input Loading	**Current Requirements**
1 unit load each	+6v: 200 ma (max)
Handle Color Code	**Power Dissipation**
Orange	1.2w (max)

APPLICATIONS

The LD-331 can be used to drive remote lamp or resistive loads up to 300 ma from a positive external supply of up to 35v.







NOTE:
ALL RETURNS COMMON TO PIN 33 (GND)

LEGEND

(1) PIN NUMBER OF PAC

—12 PIN NUMBER OF MICROCIRCUIT

M2 REFERENCE DESIGNATION OF MICROCIRCUIT

F-02 TYPE OF MICROCIRCUIT

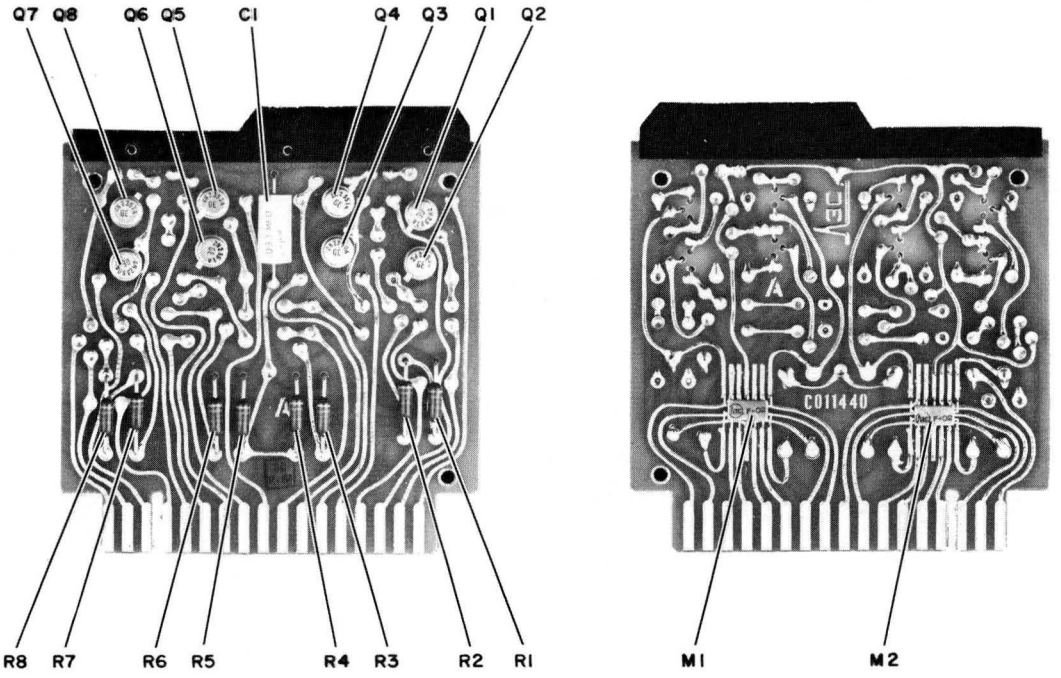
B3075

SCHEMATIC

LOGIC SYMBOL

Figure 3-18A.1. High-Drive Lamp Driver PAC, Model LD-331, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref Desig	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
Q1 - Q8	TRANSISTOR: Replacement Type 2N2351A	943 745 002
R1 - R8	RESISTOR, FIXED, COMPOSITION: 430 ohms ±2%, 1/4w	932 114 040

Figure 3-18A.2. High-Drive Lamp Driver PAC, Model LD-331, Parts Location and Identification

3-18B NEGATIVE LOGIC LEVEL DRIVER PAC, Model LD-335

The Negative Logic Level Driver PAC, Model LD-335 (Figures 3-18B. 1 and 3-18B. 2),contains eight identical circuits that convert standard μ-PAC signal levels (+6v and 0v) to negative logic levels (0v and -v). The negative voltage output is -25v at 60 ma maximum per circuit, and the voltage input is common to all circuits. Logically, each circuit acts as a two-input AND gate followed by a level shifter (+6v and 0v to 0v and -v).

CIRCUIT FUNCTION

Each driver circuit is composed of a microcircuit dual-input NAND gate which drives a discrete output transistor. When the output of the NAND circuit is a ZERO the transistor is turned on, and the output will be at ground. When the output of the NAND is a ONE the transistor is turned off and the output will be the same as the external negative supply.

NOTE

The LD-335 PAC occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

SPECIFICATIONS

Frequency of Operation (system)

DC to 4 mc

Input Loading

1 unit load each

Output Drive Capability

60 ma each at 25v

Output Timing

Rise time (positive slope): 2 ns/v (typ)
Fall time (negative slope): 200 ns (typ)

Current Requirements

+6v: 200 ma (max)

-6v: 40 ma (max)

(plus external voltage supply of -25v (max) at 0. 6 amp (max))

Power Dissipation

1. 44w (max)

Handle Color Code

Orange

APPLICATIONS

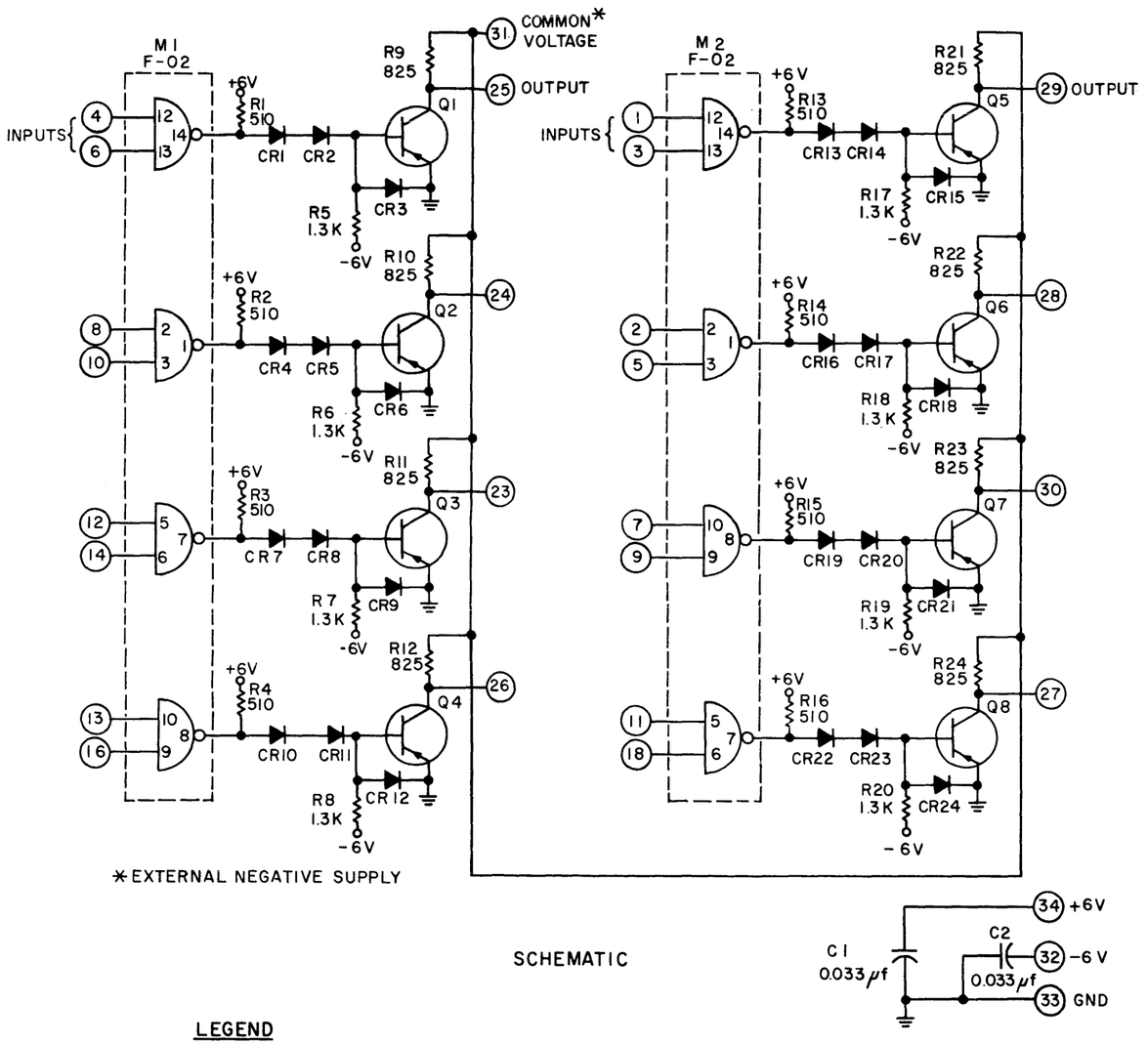
The LD-335 PAC can be used as follows.

a. To convert signals from a μ-PAC system to an S-PAC or an H-PAC system.

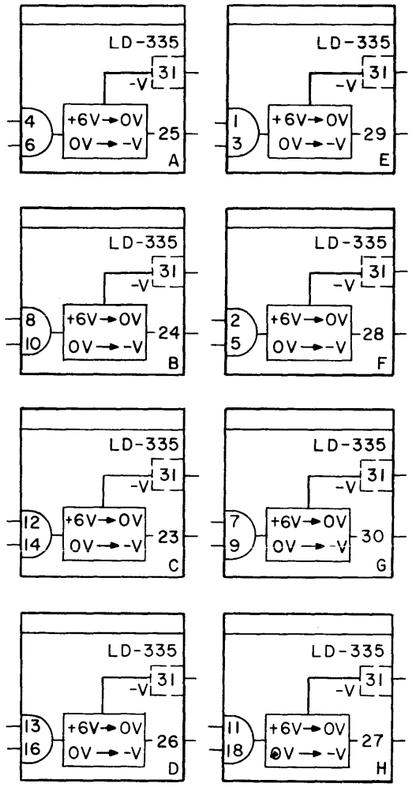
b. To drive low current filament lamps with ratings up to 40 ma

NOTE

When the LD-335 is driving S-PAC or H-PAC systems or any system which uses clamped logic, it is recommended that pin 31 be connected to the collector pull-up voltage rather than the lower logic voltage. This will improve the fall time for 5 MC operation.



SCHEMATIC



LOGIC SYMBOL

LEGEND

(1) PIN NUMBER OF PAC

—12 PIN NUMBER OF MICROCIRCUIT

M2 REFERENCE DESIGNATION OF MICROCIRCUIT

F-02 TYPE OF MICROCIRCUIT

B3074

Figure 3-18B.1. Negative Logic Level Driver PAC, Model LD-335, Schematic Diagram and Logic Symbol

Parts Location

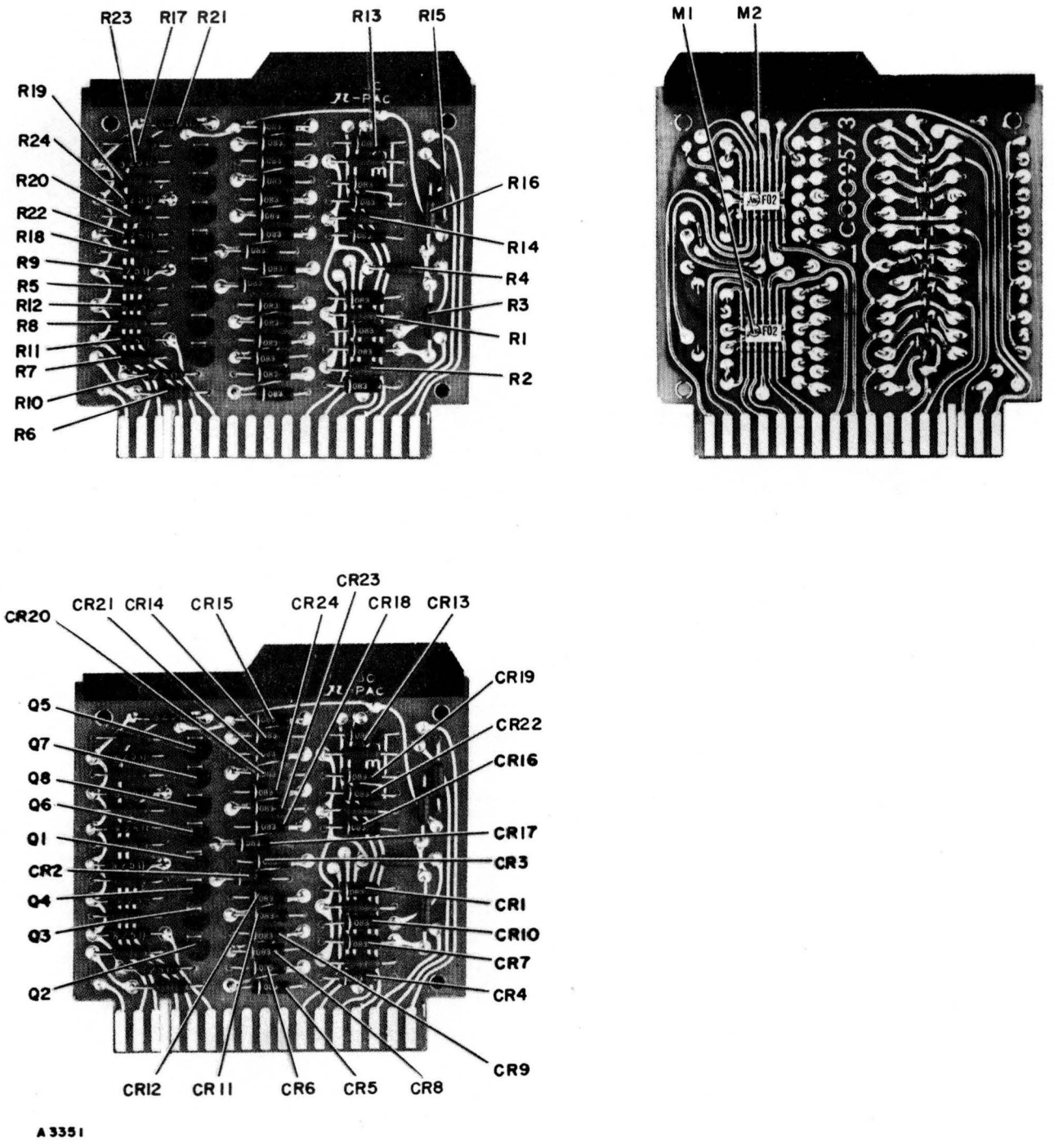


Figure 3-18B.2. Negative Logic Level Driver PAC, Model LD-335, Parts Location and Identification (Sheet 1)

Electrical Parts List

Ref Desig	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
CR1-CR24	DIODE: Replacement Type 1N914	943 083 001
Q1 - Q8	TRANSISTOR: Replacement Type 2N3906	943 746 001
R1 - R4, R13 - R16	RESISTOR, FIXED, FILM: 510 ohms ±2%, 1/4w	932 114 042
R5 - R8, R17-R20	RESISTOR, FIXED, FILM: 1.3 K ±2%, 1/4w	932 114 052
R9-R12, R21-R24	RESISTOR, FIXED, WIREWOUND: 825 ohms ±3%, 1/2w	932 209 145

Figure 3-18B.2. Negative Logic Level Driver PAC, Model LD-335, Parts Location and Identification (Sheet 2)

3-19 MASTER CLOCK PAC, MODEL MC-335

The Master Clock PAC, Model MC-335 (Figures 3-19.1 and 3-19.2), contains a crystal-controlled oscillator, a pulse shaper, and a pulse amplifier. The standard operating frequency of the MC-335 is 5 mc but this PAC can be modified to operate at any specified frequency between 200 kc and 5 mc. The MC-335 is prewired to provide negation pulse outputs through one section of a power amplifier microcircuit. The other section may be connected in series with the negation output to provide an assertion pulse. The assertion output pulse is continuously adjustable between 45 and 200 nsec.

Additional control is provided to inhibit the shaper outputs. Connections for an external frequency source and a sync output are available at the PAC connector.

CIRCUIT FUNCTION

Oscillator Circuit. -- The frequency generating section of the MC-335 is a two-transistor series mode circuit. An external frequency source can drive the PAC, provided the crystal is removed. The oscillator is dc-coupled to the pulse shaper.

Pulse Shaper. -- The pulse shaper is a nonsaturating current mode circuit which produces the desired pulse width. The pulse shaper can vary pulse width between 45 and 200 nsec by means of a built-in potentiometer-capacitor network. The potentiometer allows continuous pulse width adjustment over a 5:1 range. Increased pulse width can be obtained by replacing the capacitor with various values indicated in Table 3-19.1. The minimum pulse width is 45 nsec, and the maximum is 50 percent of the oscillator time period.

Table 3-19.1.
Pulse Widths with Replacement Capacitors

Pulse Width Range*	Value of Capacitor (Replacing C4)
45 nsec to 200 nsec	None
200 nsec to 1 μsec	130 pf
1 μsec to 5 μsec	680 pf
5 μsec to 25 μsec	3600 pf
25 μsec to 125 μsec	0.018 μf

*There will be a 5 percent minimum overlap on both ends of all ranges.

External Frequency Control. -- The MC-335 may be driven with either sine wave or pulse signals from an external source. For this mode of operation, crystal Y1 and capacitor C5 must be removed. Connect a sine wave input signal to external input 2 (pin 10). For pulse operation, connect the pulse input signal to external input 1 (pin 14), and connect a jumper across pins 12 and 10. Refer to the PAC specifications for input signal requirements.

Synchronous Clock Control. -- Synchronous start/stop control of the MC-335 prevents pulse-splitting at the pulse amplifier outputs and requires a clocked flip-flop. The flip-flop used in conjunction with the synchronous output will synchronously start and stop the MC-335 (refer to Figure 3-19.3).

Gated Input. -- This point is a power amplifier microcircuit input. When both gated inputs are at logic ONE or not connected, the pulses from the clock appear at the output. When either gated input is at logic ZERO, output pulses are inhibited.

NOTE

The MC-335 occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

SPECIFICATIONS

Oscillator Circuit

Frequency of Operation

200 kc to 5 mc

Input Loading

Gated input: 2 unit loads each

Frequency Accuracy

0.01%

Frequency Stability

0.005%

External Frequency Input

External input 2 (sine wave):	200 kc to 5 mc	
	±1.5v (min)	
	±3.0v (max)	
	input impedance 500 ohms	
External input 1 (pulse):	less than 1 cps to 5 mc	
	3v (min)	
	pulse width	50 nsec (min)
	fall time	30 nsec (max)

Output Drive Capability

Negation output:	25 unit loads
Sync output:	2 unit loads

Pulse Width Stability

Temperature: 0°C to +55°C

Voltage: 5.1v to 6.3v

Assertion pulse > 200 nsec: ±2% (typ)

For 50 nsec pulse: ±3 nsec (typ)

Power Amplifier Circuit

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Output Drive Capability

25 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

30 nsec (max)

MC-335 PAC

Current Requirements

+6v: 80 ma (max)

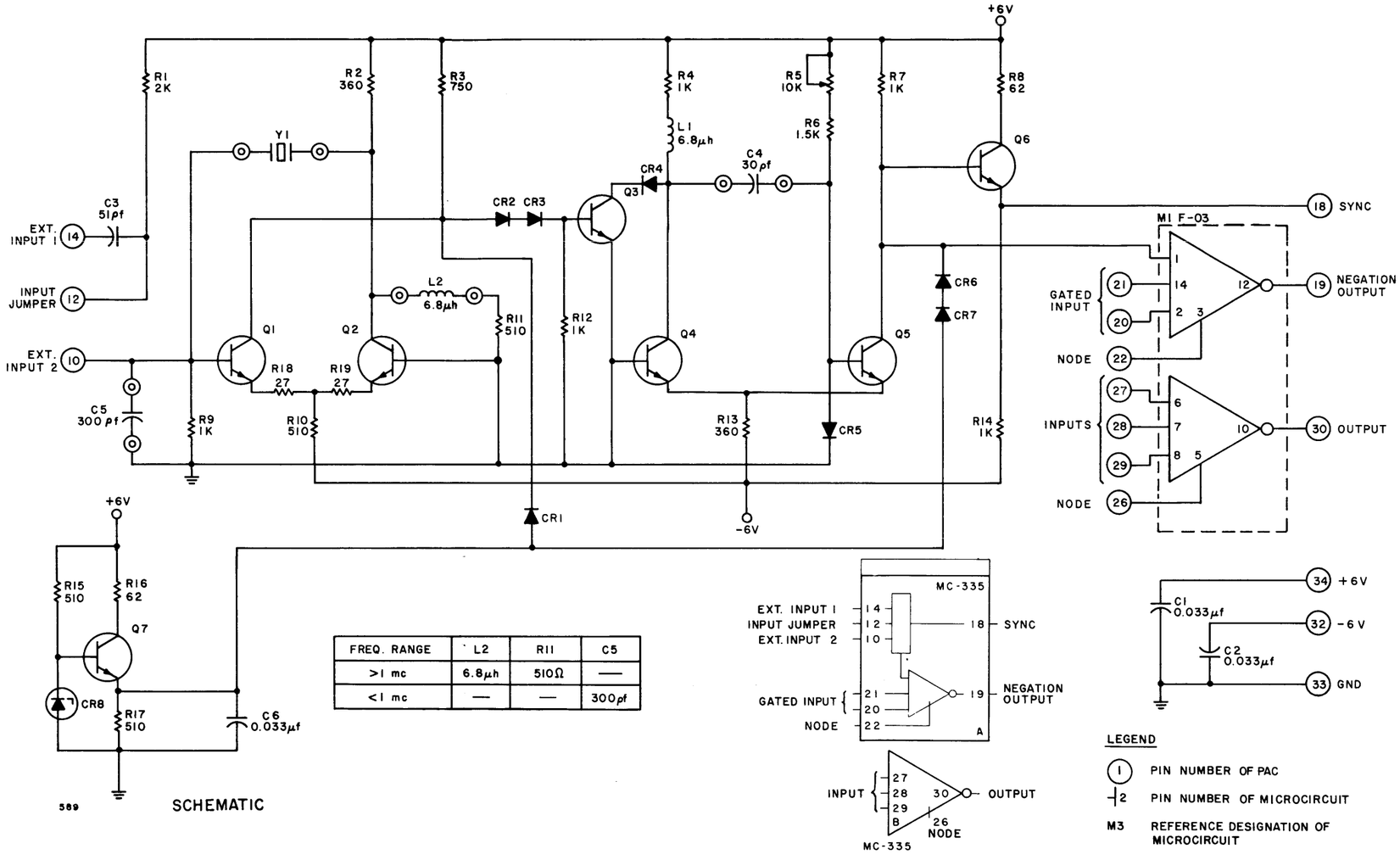
-6v: 40 ma (max)

Power Dissipation

0.72w (max)

Handle Color Code

Yellow

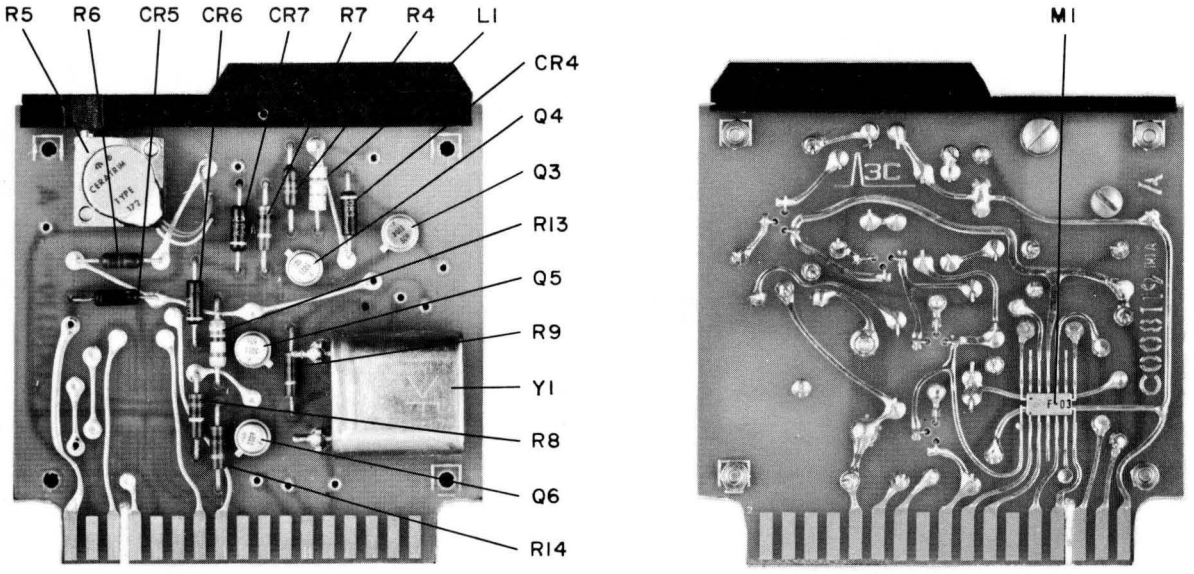


FREQ. RANGE	L2	R11	C5
>1 mc	6.8μh	510Ω	—
<1 mc	—	—	300pf

Figure 3-19.1. Master Clock PAC, Model MC-335, Schematic Diagram and Logic Symbol

Parts Location

Board A



Board B

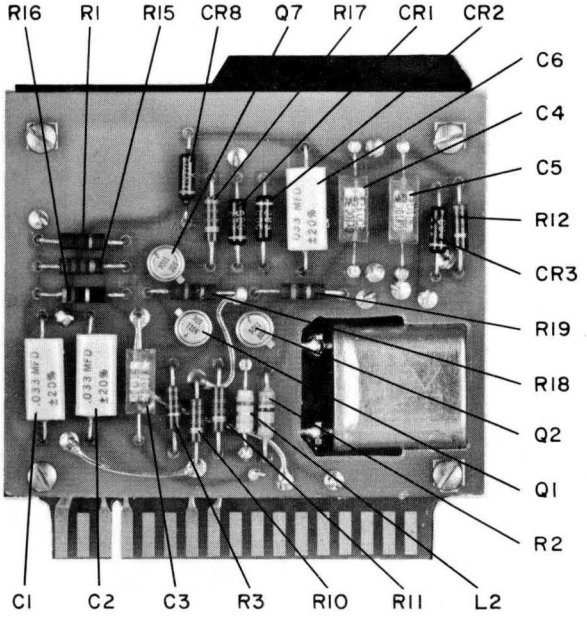


Figure 3-19.2. Master Clock PAC, Model MC-335, Parts Location and Identification (Sheet 1 of 2)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1, C2, C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 51 pf ±5%, 500 vdc	930 005 616
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±2%, 500 vdc	930 005 510
C5	CAPACITOR, FIXED MICA DIELECTRIC: 300 pf ±2%, 500 vdc	930 005 534
CR1-CR4, CR6, CR7	DIODE: Replacement Type 1N914	943 083 001
CR5	DIODE: Replacement Type FD777	943 088 001
CR8	DIODE: Replacement Type 1N702A	943 102 004
L1, L2	COIL, R.F.: 6.8 μh, ±10%	939 207 023
Q1-Q7	TRANSISTOR	943 722 002
R1	RESISTOR, FIXED, COMPOSITION: 2 K ±5%, 1/4w	932 007 056
R2	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/4w	932 007 038
R3	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/4w	932 007 046
R4	RESISTOR, FIXED, FILM: 1 K ±2%, 1/4w	932 114 049
R5	RESISTOR, VARIABLE: 10 K ±10%, 3/4w	933 300 107
R6	RESISTOR, FIXED, FILM: 1.5 K ±2%, 1/4w	932 114 053
R7, R9, R12, R14	RESISTOR, FIXED, COMPOSITION: 1 K ±5%, 1/4w	932 007 049
R8, R16	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4w	932 007 020
R10, R11, R15, R17	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4w	932 007 042
R13	RESISTOR, FIXED, FILM: 360 ohms ±2%, 1/4w	932 114 038
R18, R19	RESISTOR, FIXED, COMPOSITION: 27 ohms ±5%, 1/4w	932 007 011
Y1	CRYSTAL, UNIT QUARTZ: 200 kc to 5 mc	961 002 204

Figure 3-19.2. Master Clock PAC, Model MC-335, Parts Location and Identification (Sheet 2 of 2)

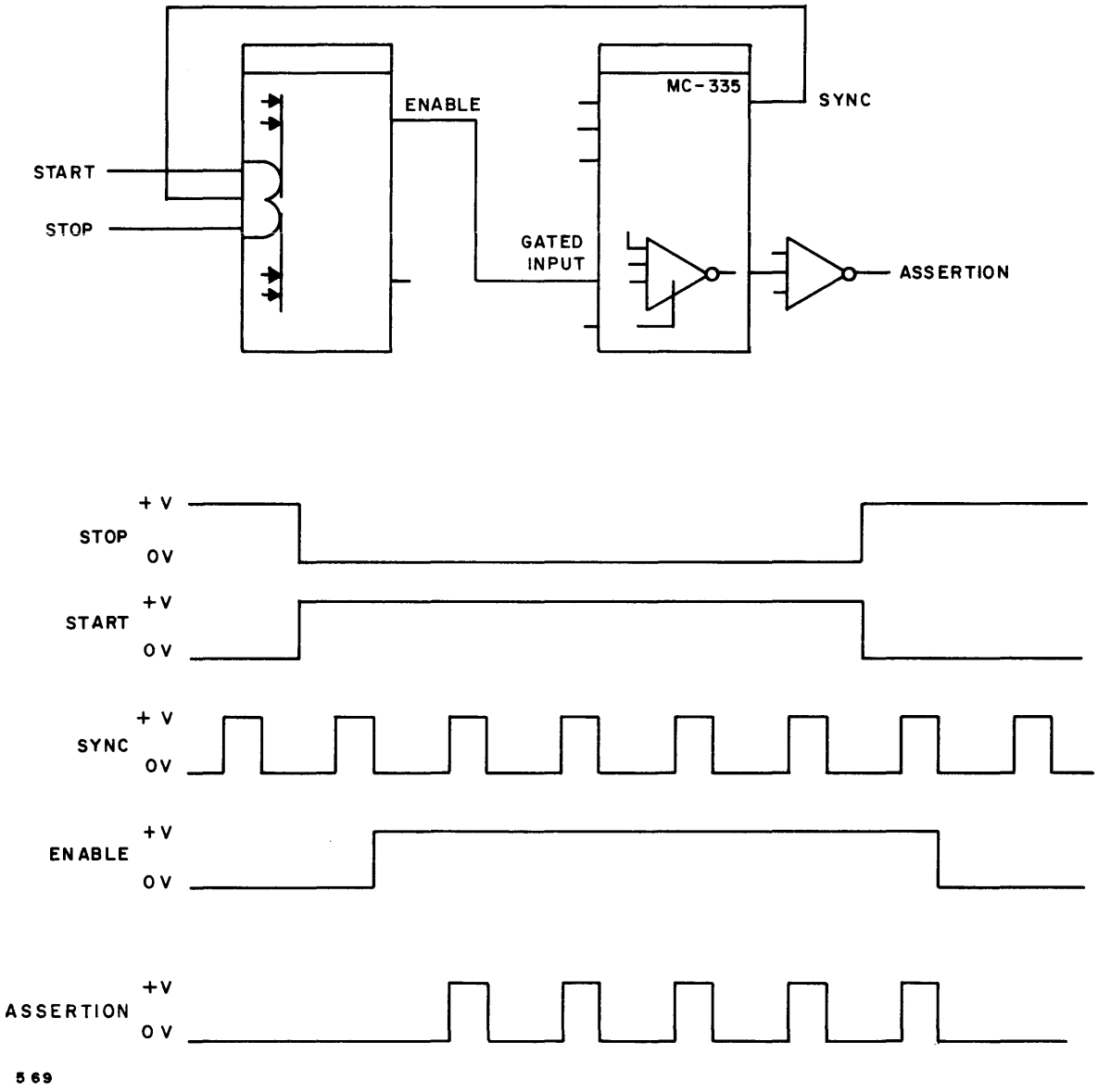


Figure 3-19.3. Master Clock PAC, Model MC-335, Synchronous Clock Control

3-20 MULTIVIBRATOR CLOCK PAC, MODEL MV-335

The Multivibrator Clock PAC, Model MV-335 (Figures 3-20.1 and 3-20.2), contains a self-starting, free-running multivibrator, a pulse shaper and a pulse amplifier. The MV-335 functions primarily as a variable frequency clock source. The frequency of operation is from 200 kc to 5 mc in two overlapping ranges. Lower frequencies are obtainable with the addition of external capacitors on standoff terminals located on the PAC.

The MV-335 is prewired to provide negation pulses through a standard power amplifier microcircuit. In addition, the PAC provides an oscillator inhibit which is internally wired to provide synchronous start/stop capability from external asynchronous signals. A logic ONE level will inhibit the oscillator, and a ZERO level will enable the oscillator.

NOTE

The OSC INHIBIT input, pin 9, must be at GND in order to generate pulses.

The PAC also contains an independent power amplifier.

CIRCUIT FUNCTION

Multivibrator Circuit. -- The multivibrator is a free-running, self-starting circuit with an operating frequency dependent upon the value of the timing capacitor C4. The basic frequency range of the multivibrator is 1 mc to 5 mc. Jumpering pin 2 to pin 4 will place C5 in parallel with C4 and reduce this range from 1 mc to 200 kc. Additional ranges are obtainable by replacing C4 with other values listed in Table 3-20.1. Potentiometer R10, mounted on the PAC, permits continuous variation of frequency within the selected range.

Pulse Shaper Circuit. -- The pulse shaper is a current mode nonsaturating circuit which is dc-coupled to the multivibrator by transistor Q6. Pulse widths can be varied by means of a built-in potentiometer-capacitor network. Potentiometer R17 allows continuous pulse width adjustment between 45 nsec and 200 nsec. The pulse width minimum is 45 nsec and the maximum is 50 percent of the time period. Increased pulse width, beyond that standard range, may be obtained by replacing capacitor C8 with associated values listed in Table 3-20.2.

Gated Input. -- This point is a power amplifier microcircuit input. When the gated input is at logic ONE, or not connected, the pulses from the oscillator appear at the output. When the input is at logic ZERO, output pulses are inhibited.

NOTE

The MV-335 PAC occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

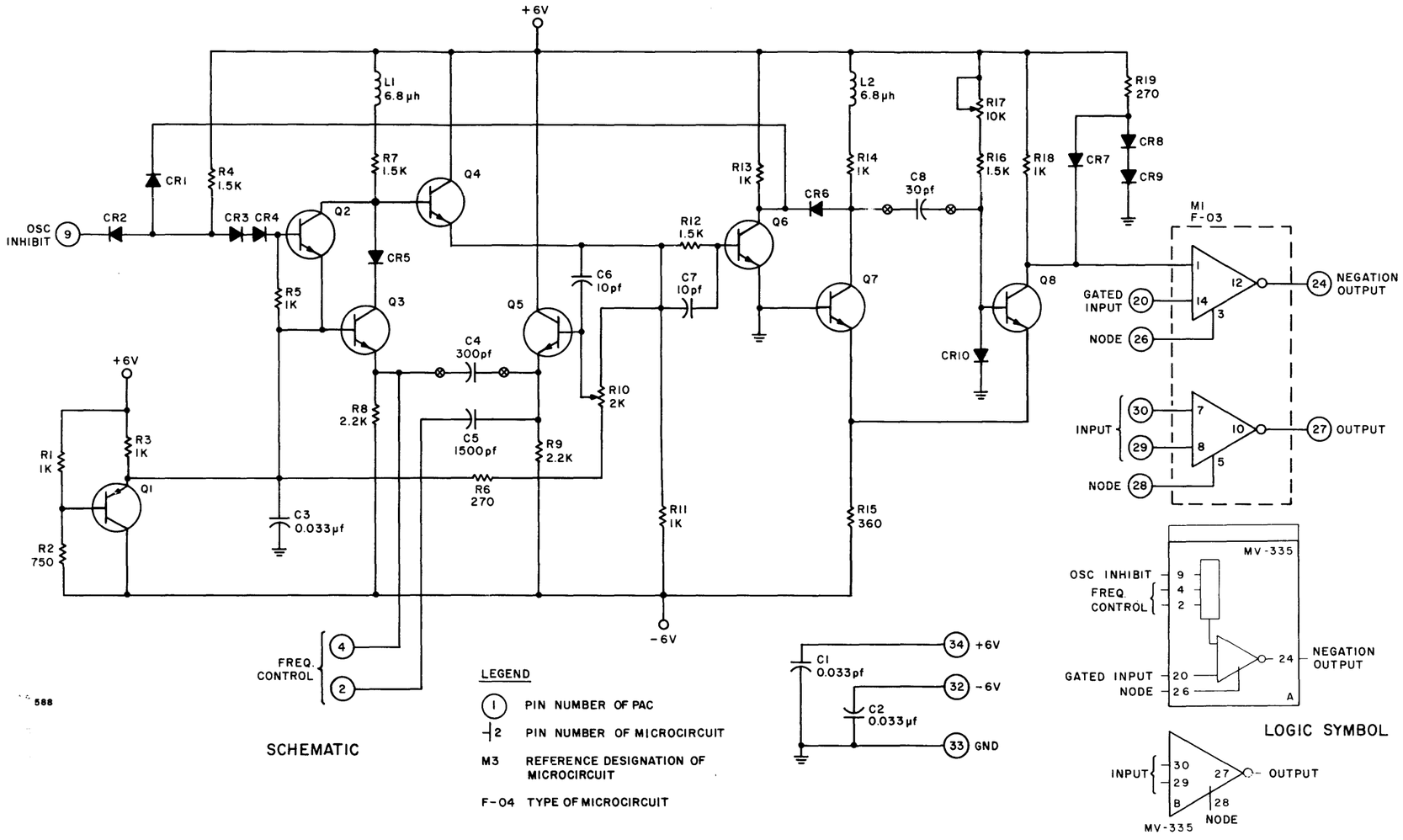
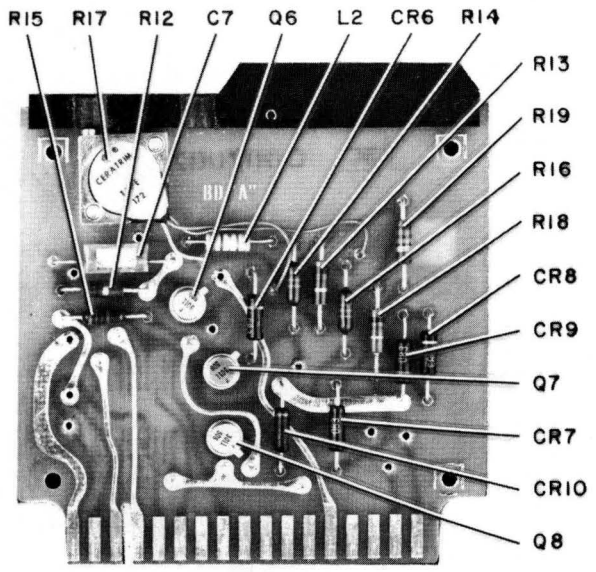
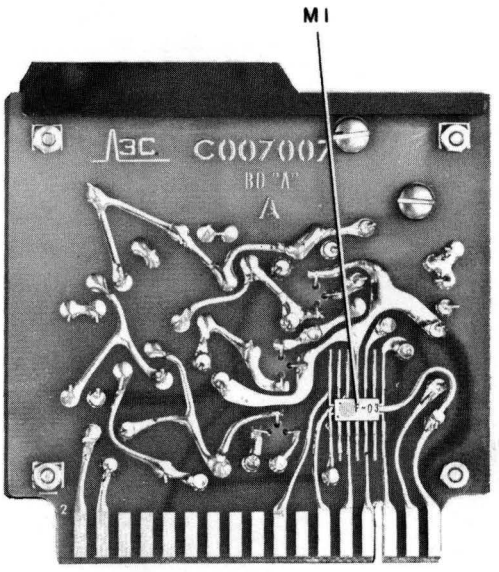


Figure 3-20.1. Multivibrator Clock PAC, Model MV-335, Schematic Diagram and Logic Symbol

Parts Location

Board A





Board B

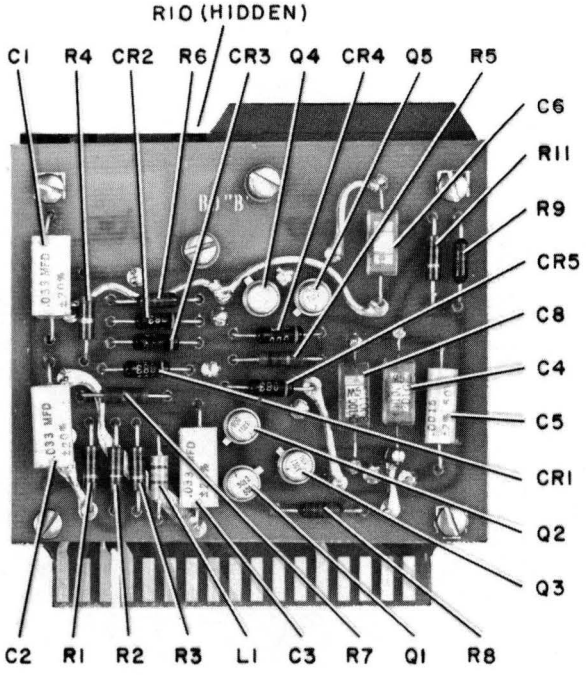


Figure 3-20.2. Multivibrator Clock PAC, Model MV-335, Parts Location and Identification (Sheet 1 of 2)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1-C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 300 pf ±2%, 500 vdc	930 005 534
C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1500 pf ±5%, 50 vdc	930 313 205
C6, C7	CAPACITOR, FIXED, MICA DIELECTRIC: 10 pf ±5%, 500 vdc	930 005 602
C8	CAPACITOR, FIXED, MICA DIELECTRIC: 30 pf ±2%, 500 vdc	930 005 510
CR1-CR9	DIODE: Replacement Type 1N914	943 083 001
CR10	DIODE: Replacement Type FD777	932 088 001
L1, L2	COIL, R.F.: 6.8 μh ±10%	939 207 023
Q1	TRANSISTOR	943 721 002
Q2-Q8	TRANSISTOR	943 722 002
R1,R3,R5, R11,R13,R18	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049
R2	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/4w	932 007 046
R4,R7,R12	RESISTOR, FIXED, COMPOSITION: 1.5K ±5%, 1/4w	932 007 053
R6	RESISTOR, FIXED, FILM: 270 ohms ±2%, 1/4w	932 114 035
R8,R9	RESISTOR, FIXED, FILM: 2.2K ±2%, 1/4w	932 114 057
R10	RESISTOR, VARIABLE: 2K ±10%, 3/4w	933 300 105
R14	RESISTOR, FIXED, FILM: 1K ±2%, 1/4w	932 114 049
R15	RESISTOR, FIXED, FILM: 360 ohms ±2%, 1/4w	932 114 038
R16	RESISTOR, FIXED, FILM: 1.5K ±2%, 1/4w	932 114 053
R17	RESISTOR, VARIABLE: 10K ±10%, 3/4w	933 300 107
R19	RESISTOR, FIXED, COMPOSITION: 270 ohms ±5%, 1/4w	932 007 035

Figure 3-20.2. Multivibrator Clock PAC, Model MV-335, Parts Location and Identification (Sheet 2 of 2)

Table 3-20.1.
Frequency Ranges with Replacement Capacitors

MV-335 Frequency Range*	Value of Capacitor (Replacing C4)
5.5 mc to 1.25 mc	None
1.25 mc to 200 kc	None (Jumper pin 2 to 4)
200 kc to 40 kc	0.012 μf
40 kc to 8 kc	0.056 μf
8 kc to 1.5 kc	0.33 μf
1.5 kc to 0.3 kc	1.5 μf
370 to 45 cps	6.8 μf**
54 to 6 cps	56 μf**
132.5	220 μf **

Table 3-20.2.
Pulse Widths with Replacement Capacitors

Pulse Width Range*	Value of Capacitor (Replacing C8)
45 nsec to 200 nsec	None
200 nsec to 1 μsec	130 pf
1 μsec to 5 μsec	680 pf
5 μsec to 25 μsec	3600 pf
25 μsec to 125 μsec	0.018 μf

SPECIFICATIONS

Multivibrator Circuit

Input Loading

Gated input: 2 unit loads

Frequency Range

5 mc to 200 kc in two overlapping ranges

200 kc to less than 5 cps with capacitor changes

Potentiometer range, 5:1

Output Drive Capability

25 unit loads

Temperature Stability

Oscillator frequency from 0°C to +55°C: 4% (typ)

Pulse width stability of assertion pulse 0°C to +55°C: 4% (typ)

50 nsec pulse: ±3 nsec (typ)

Voltage Stability

Oscillator from 5.1v to 6.3v:	10%
Pulse width for 50 nsec pulses:	20%
Pulse width > 200 nsec pulses:	5%

* There will be a 5 percent minimum overlap on both ends of all ranges.

** The frequency range can be extended down to as low as 2.5 cps, but the capacitor required will probably require additional PAC slot spaces due to the component height restriction.

Power Amplifier

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Output Drive Capability

25 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

30 nsec (max)

MV-335 PAC

Current Requirements

+6v: 110 ma (max)

-6v: 50 ma (max)

Power Dissipation

0.96w (max)

Handle Color Code

Yellow

3-21 OCTAL/DECIMAL DECODER PAC, MODEL OD-335

The Octal/Decimal Decoder PAC, Model OD-335 (Figures 3-21.1 and 3-21.2), contains a prewired binary-to-octal decimal decoder and two additional independent NAND gates to expand the matrix for BCD-to-decimal decoding. The octal matrix is composed of eight NAND gates and has nine input lines and eight output lines. Of the nine inputs, six accept both polarities of a three-bit binary number. The three additional input lines expand the matrix from 8 to 16, 32, or 64 outputs by using additional OD-335 PACs (Figure 3-21.3). If a 64-output matrix is not required, one or more of these additional input lines can be used for strobing or sampling of the matrix.

The BCD-to-decimal decoder uses the octal matrix for the output lines 0 through 7 and two independent NAND gates, included on the PAC, for output lines 8 and 9. The two independent gates can be used when BCD-to-decimal decoding is not required.

Octal Matrix. -- Each of the gates in the octal matrix has a total of six inputs. Three of these inputs recognize a discrete binary number from 000 through 111. For an example, the three inputs, $\overline{2^0}$, 2^1, and 2^2 would drive output line 6 (pin 16). The remaining three inputs are common to all eight gates. The six inputs to any gate must be a ONE to activate the gate output. An output line is activated when it is at ZERO (ground). Since inputs X, Y, and Z form three common and direct inputs to all eight gates, these inputs must be ONEs (+6v or disconnected) to have one of the eight output lines activated.

BCD-to-Decimal Decoder. -- The BCD-to-decimal decoder consists of the octal matrix and the two additional NAND gates (Figure 3-21.4). If the OD-335 is connected in this manner, four binary-coded-decimal bits with both polarities are required. If binary numbers 10 through 15 are forbidden, or if ambiguous outputs resulting from these numbers are permitted, then only the most and least significant bits are required as inputs to gates 8 and 9.

Strobing. -- Provision is made to permit strobing or sampling of the matrix. Strobing is accomplished by applying a positive pulse to input X, Y, or Z. Prior to the pulse, when the input is a ZERO, the matrix is inhibited and all output lines are ONEs. During the positive pulse, one of the lines is activated and becomes a ZERO. The three common inputs to the octal matrix can be used as separate strobe lines to gate a strobing function.

The OD-335 decodes any combination of binary bits. As the inputs to the PAC change, one or more of the outputs can be transiently selected. For example, a binary counter in changing from 0111 to 1000 passes briefly through states 0110, 0100, and 0000. These transitory states can cause brief negative spikes at the corresponding output lines of the PAC. To eliminate the spikes, the decoder should be inhibited during the transition of the driving register.

A detailed description of the NAND circuit is given in Section II.

INPUT AND OUTPUT SIGNALS

Binary Inputs $\overline{2}^0$ through 2^2. -- These six input lines are driven by the assertion and negation levels of a three-bit binary number.

Common Inputs X, Y, and Z. -- Applying ZERO to any one of these common inputs inhibits the octal matrix. This feature is useful in applications requiring multioctal matrices, BCD-to-decimal decoding, and strobing.

Outputs 0 through 7. -- An output is active or selected when at ground.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

Binary-to-Octal and Multioctal Matrices

8 output decoder (3 bits):	3 unit loads each
16 output decoder (4 bits):	4 unit loads each
32 output decoder (5 bits):	7 unit loads each
64 output decoder (6 bits):	14 unit loads each

BCD-to-Decimal Decoder

Binary bits 2^0 and $\overline{2}^0$:	4 unit loads each
Binary bits 2^1, $\overline{2}^1$, 2^2, and $\overline{2}^2$:	3 unit loads each
Binary bit 2^3:	2 unit loads
Binary bit $\overline{2}^3$:	5 unit loads

Independent NAND Gates

1 unit load each

Output Drive Capability

8 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)
33 nsec (max)(30 nsec for gate plus 3 nsec for diode cluster)

Current Requirements

+6v: 125 ma (max)

Power Dissipation

0.75w (max)

Handle Color Code

Purple

APPLICATIONS

Matrices for decoding 16, 32, or 64 outputs are formed by using two, four, or eight OD-335 PACs, respectively. All but the one matrix containing the significant output line must be inhibited. In a 64-output matrix, seven of the eight octal matrices must be inhibited for unique activation of one of the 64 output lines. The seven matrices are inhibited by applying a ZERO to input X, Y, or Z. For example, if binary bit 2^3, 2^4, and 2^5 are ONEs, the seven matrices with outputs 0 through 55 are inhibited and only one output from 56 to 63 is activated, depending upon the state of bits 2^0, 2^1, and 2^2. Figure 3-21.3 illustrates the logic connections for multioctal matrices.

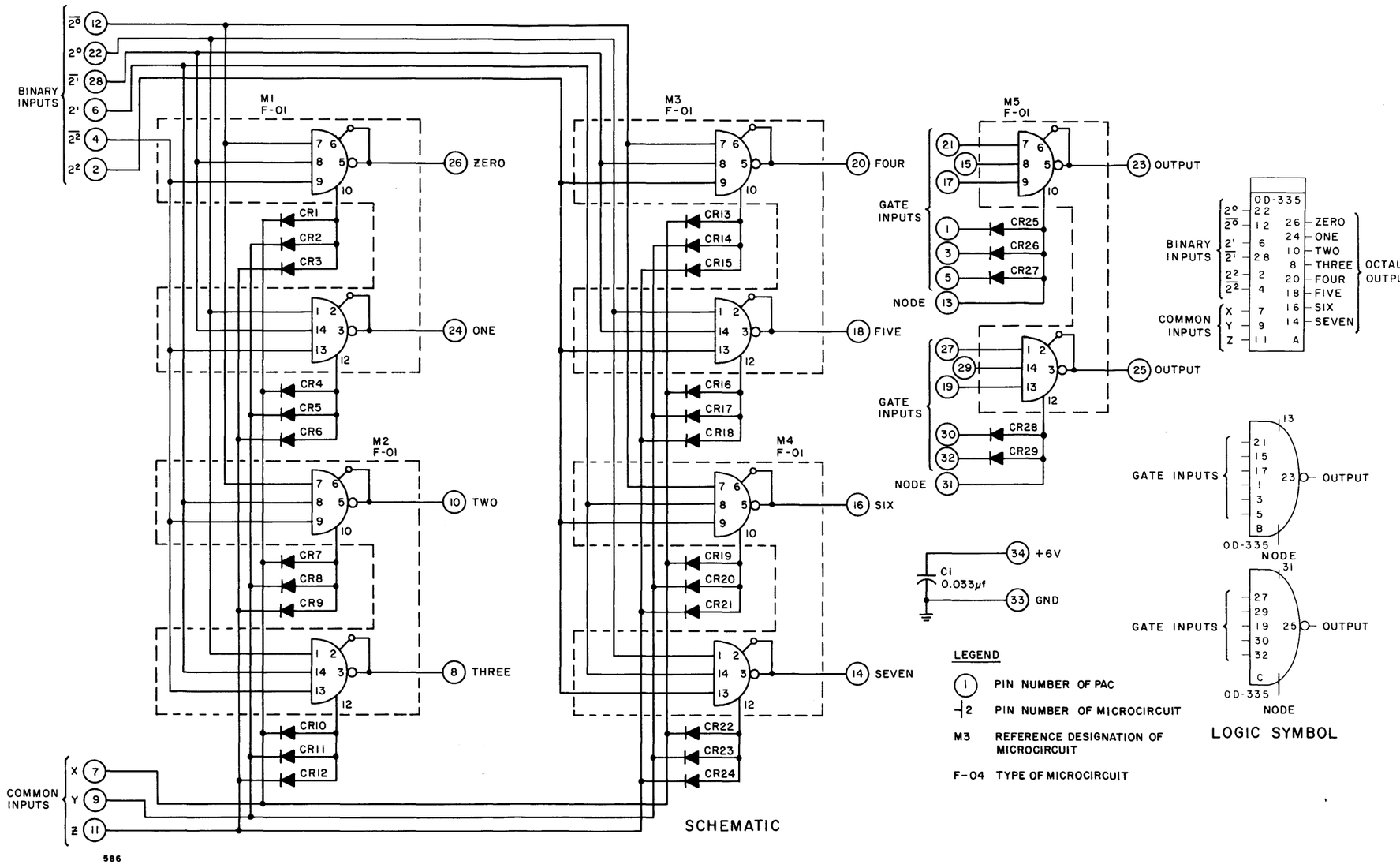
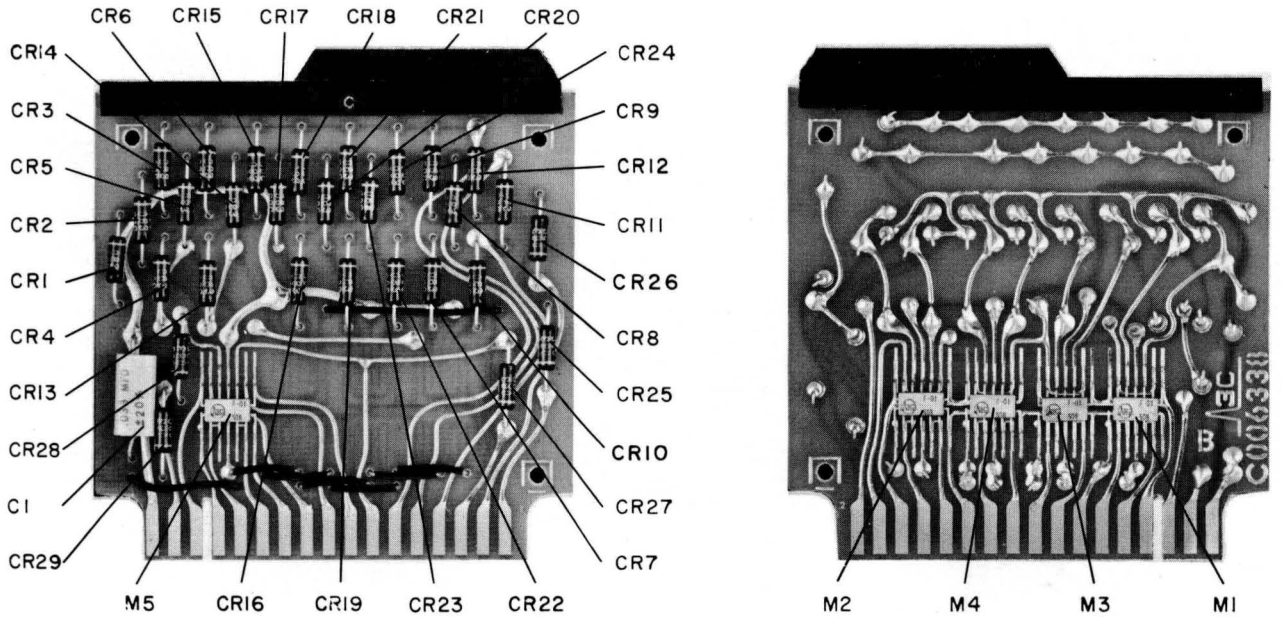


Figure 3-21. 1. Octal/Decimal Decoder PAC, Model OD-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M5	MICROCIRCUIT: F-01, dual NAND gate integration circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR29	DIODE: Replacement Type 1N914	943 083 001

Figure 3-21.2. Octal/Decimal Decoder PAC, Model OD-335, Parts Location and Identification

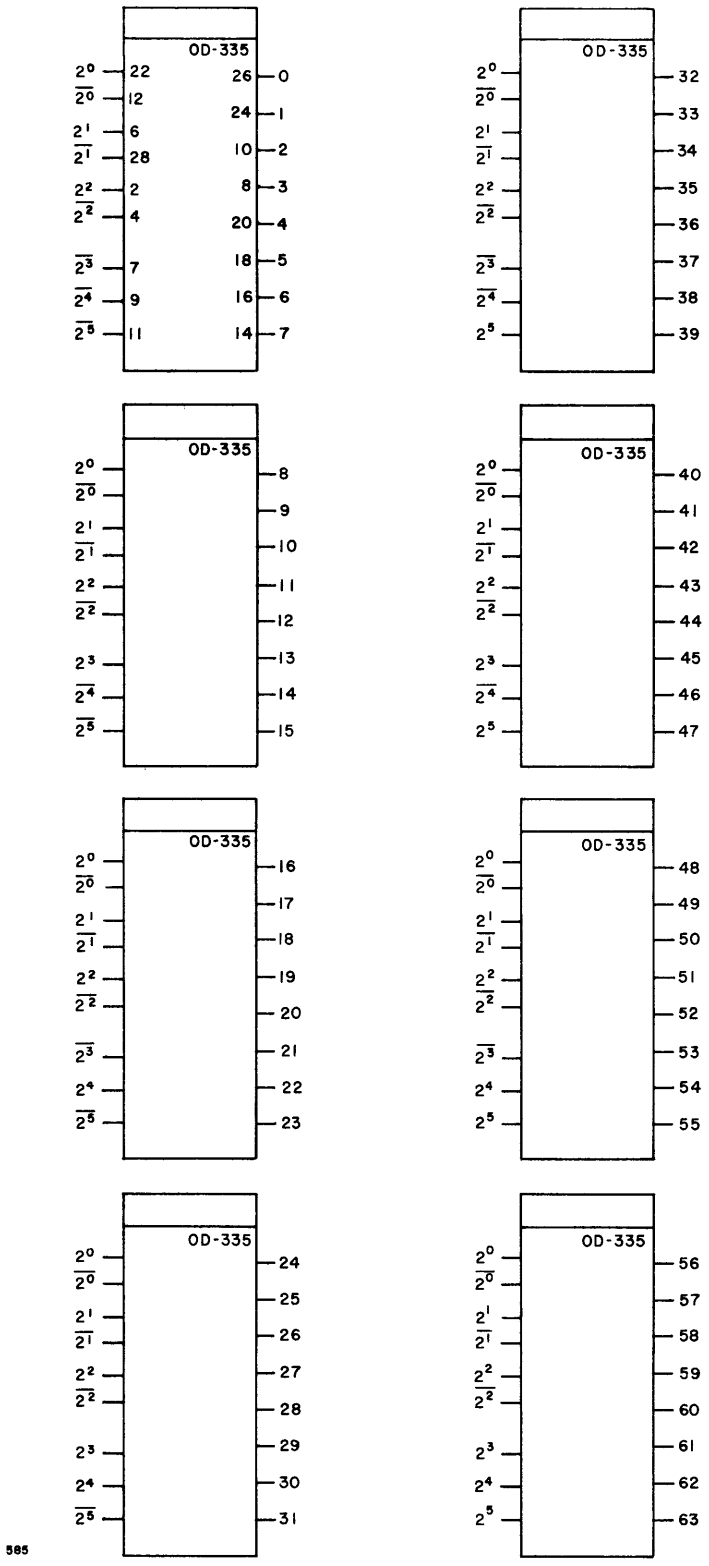


Figure 3-21.3. Octal/Decimal Decoder PAC, Model OD-335, Multioctal Matrices

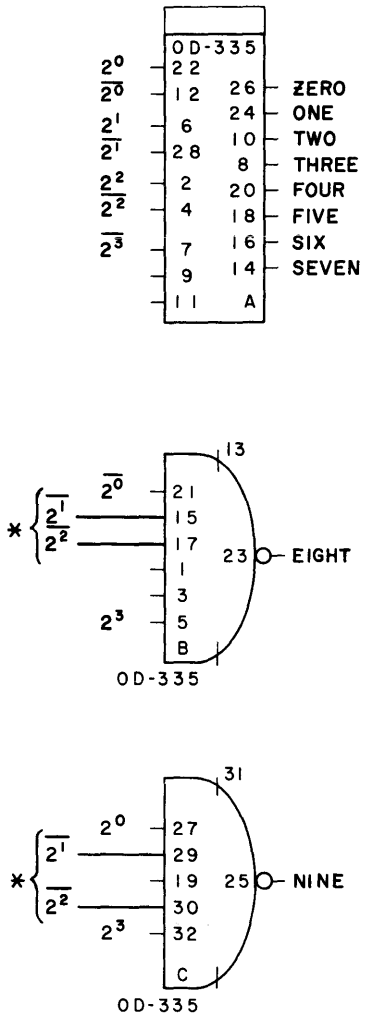


Figure 3-21. 4. Octal/Decimal Decoder PAC, Model OD-335 BCD-to-Decimal Decoder

3-22 POWER AMPLIFIER PAC, MODEL PA-335

The Power Amplifier PAC, Model PA-335 (Figures 3-22.1 and 3-22.2), contains six 3-input NAND gates that can be used for driving heavy loads. Each gate has two electrically common outputs to reduce load distribution current on any single wire. Built-in short-circuit protection limits output current if the output is accidentally grounded.

Each gate performs the NAND function for positive logic (positive voltage is a ONE and 0v is a ZERO). For negative logic, it becomes a NOR gate. When all inputs to a gate are at positive or not connected, the output goes to ground. When any input is at ground, the output goes to a positive voltage.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Current Requirements

+6v: 80 ma (max)

Power Dissipation

Static: 480 mw
Dynamic: 780 mw

Handle Color Code

Green

Output Drive Capability

25 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

30 nsec (max)

APPLICATIONS

The power gates operate on levels, pulses, or with combinations of both. Two gates can be wired back to back to form a dc set/reset power flip-flop.

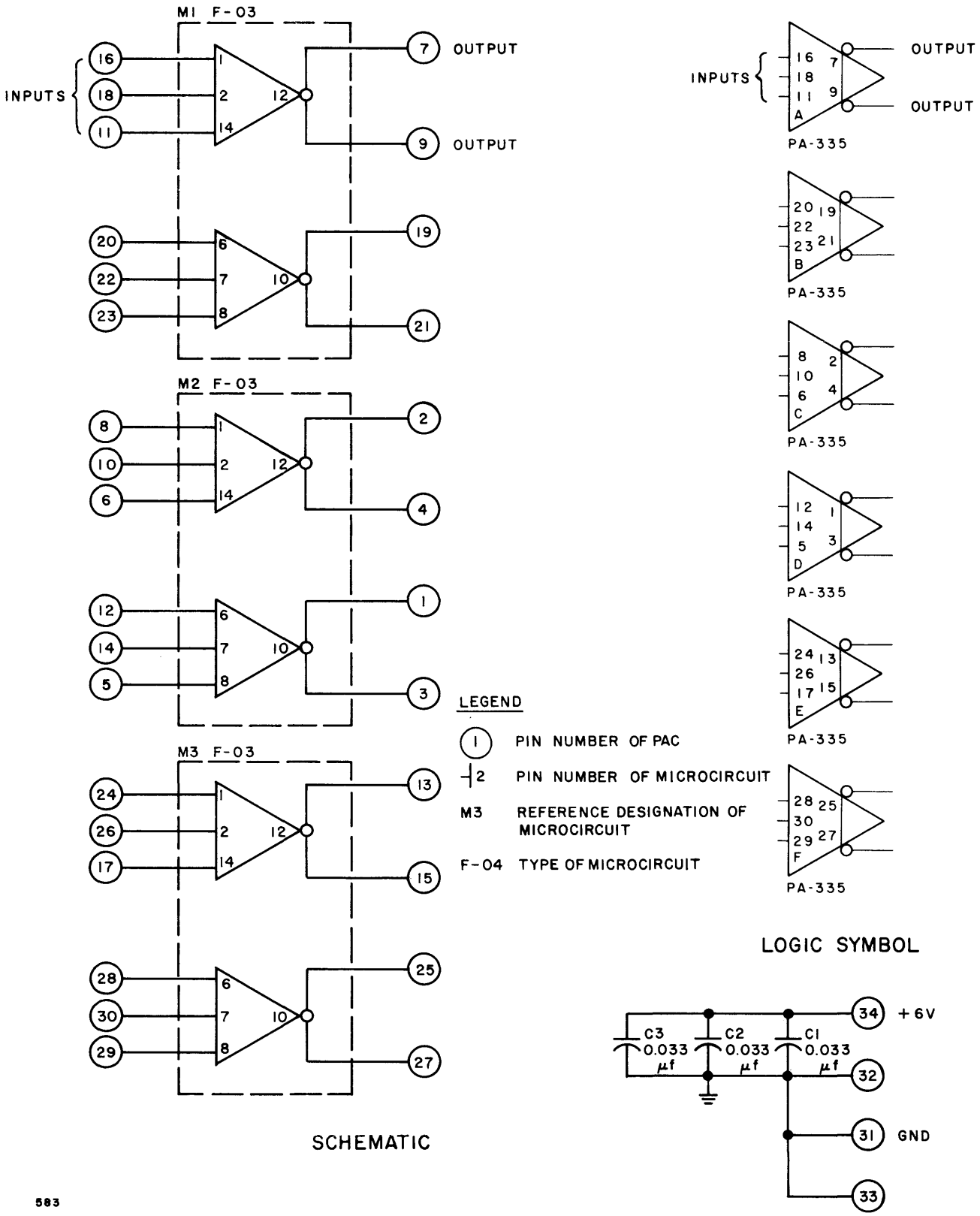
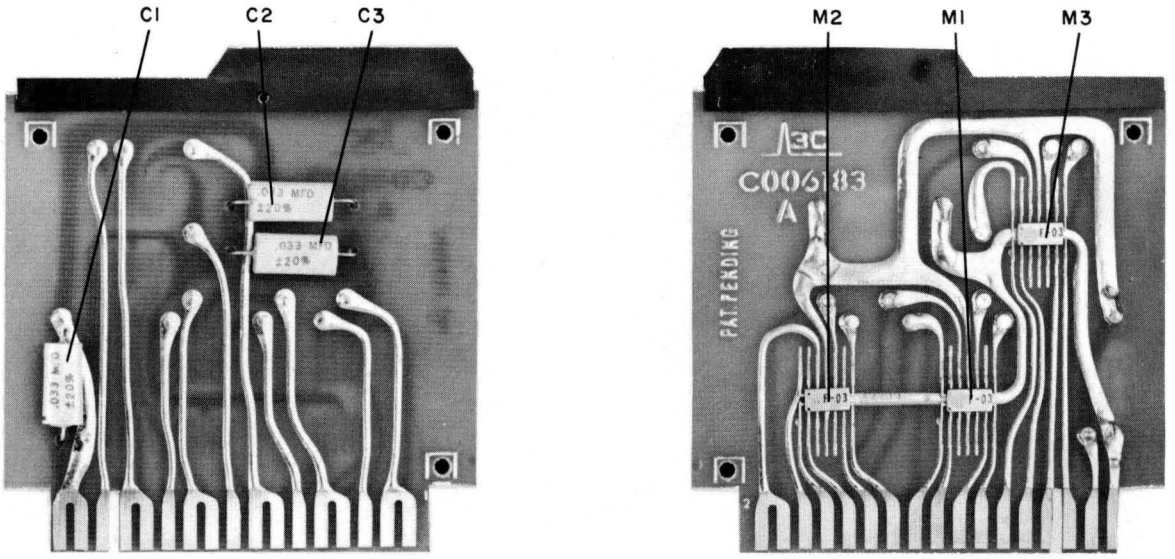


Figure 3-22.1. Power Amplifier PAC, Model PA-335, Schematic Diagram and Logic Symbol

Parts Location



537

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1-C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-22.2. Power Amplifier PAC, Model PA-335, Parts Location and Identification

3-22A POWER AMPLIFIER PAC, MODEL PA-336

The Power Amplifier PAC, Model PA-336 (Figures 3-22A.1 and 3-22A.2), contains six 3-input NAND gates that can be used for driving heavy loads. Built-in short-circuit protection limits output current if the output is accidentally grounded.

CIRCUIT FUNCTION

Each gate performs the NAND function for positive logic (positive voltage is a ONE and 0v is a ZERO). For negative logic, it becomes a NOR gate. When all inputs to a gate are at positive or not connected, the output goes to ground. When any input is at ground, the output goes to a positive voltage.

NOTE

The following pins must be jumpered together on the connector into which a PA-336 is inserted. These jumpers should be made as short as possible.

Pin 1 to pin 33
Pin 4 to pin 31
Pin 13 to pin 32
Pin 9 to pin 32
Pin 21 to pin 31

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Current Requirements

+6v: 80 ma (max)

Power Dissipation

0.48w (max) static,

0.78w (max) at 5 mc and with 250 pf stray capacitance

Handle Color Code

Green

Output Drive Capability

25 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

30 nsec (max)

APPLICATIONS

The power gates operate on levels, pulses, or with combinations of both. Two gates can be wired back to back to form a dc set/reset power flip-flop.

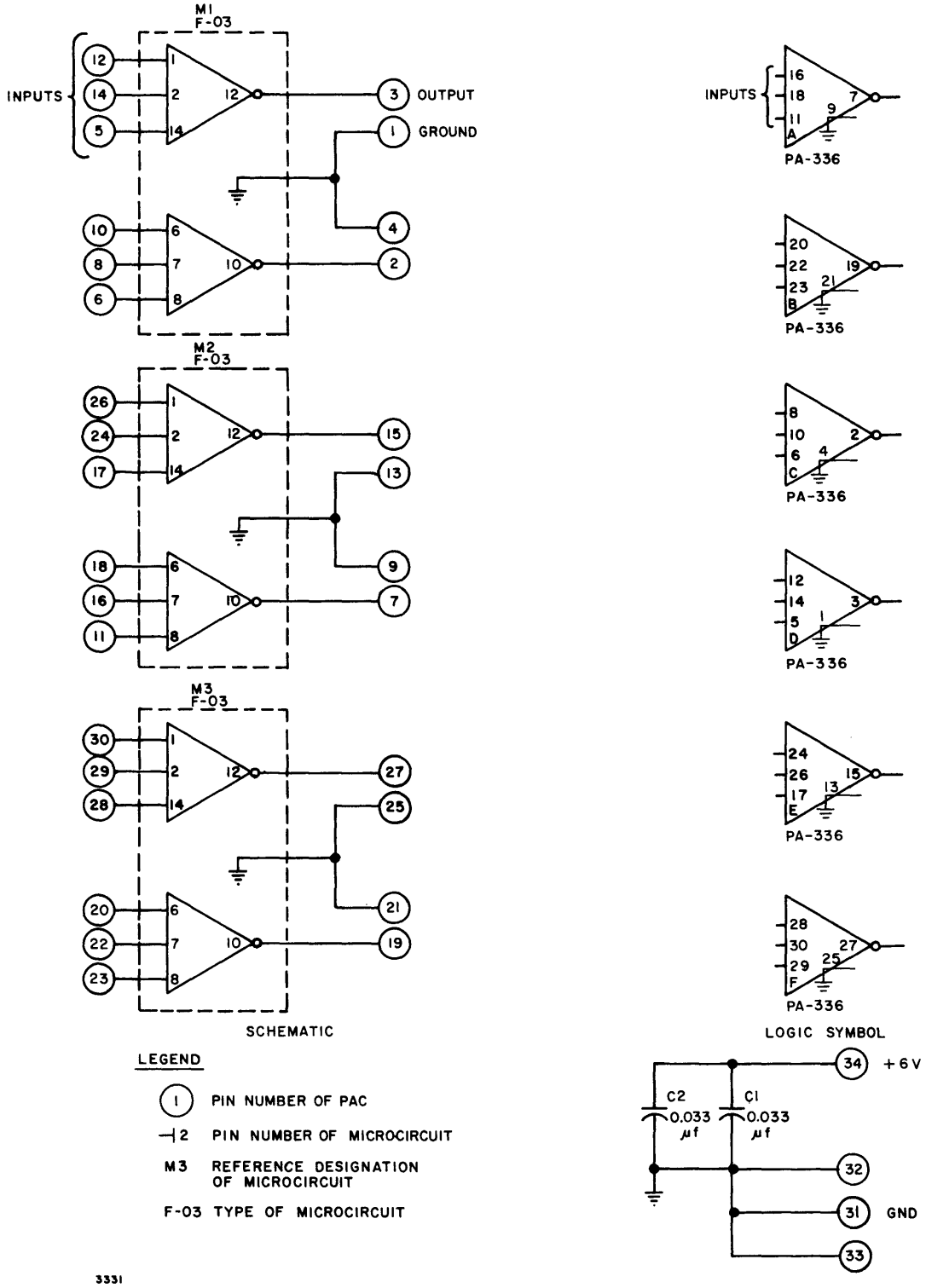
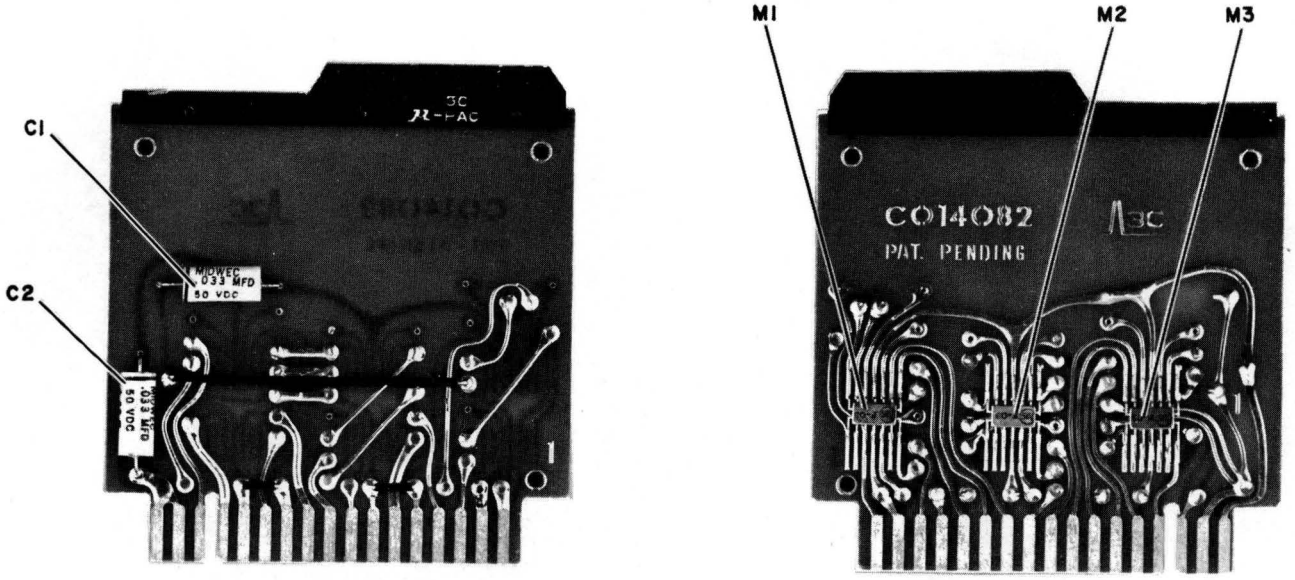


Figure 3-22A.1. Power Amplifier PAC, Model PA-336, Schematic Diagram and Logic Symbol

Parts Location



3329

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1, C2	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-22A.2. Power Amplifier PAC, Model PA-336, Parts Location and Identification

3-23 PLUG-IN POWER SUPPLIES, MODELS PB-330 AND PB-331

The Plug-In Power Supplies, Models PB-330 and PB-331 (Figures 3-23.1 and 3-23.2), are integrally packaged units that can be mounted directly into their respective μ-BLOCs. Both models supply current at the two μ-PAC voltage levels, +6v and -6v. The PB-330 can drive approximately 24 μ-PACs, and the PB-331, approximately 96 μ-PACs. The number of PACs that can be powered from the supplies depends on the current requirements of the PACs used.

Line voltage is applied to the power supplies through connectors mounted in the fan housing area of the μ-BLOC. μ-PAC voltages are brought out the side of the supplies adjacent to the wiring side of the μ-PAC connectors and are connected to the power distribution on buses by means of push-on connectors.

The following features are recess-mounted on the front panel of the supply and are concealed when the front panel of the μ-BLOC is in place.

1. ON/OFF AC power switch
2. Power ON lamp
3. Three fuses. Protection is provided for the ac input voltage and the two voltage outputs.
4. Access to the voltage adjustment potentiometers for the +6-v and -6-v outputs (PB-331). For the PB-330, access is on the rear panel.

CIRCUIT FUNCTION

The PB-330 and PB-331 contain two dynamically regulated circuits which combine to provide the two μ-PAC voltage levels. The rated currents for each output are proportional to the relative currents required in a system.

The +6-v and -6-v supplies are Zener-regulated circuits which consist of a full-wave rectifier, error detector, differential amplifier, and pass transistors (refer to Figures 3-23.3 and 3-23.4). The power transformer is provided with two-primary windings and a series of taps to facilitate operation from 100 vac to 240 vac at any frequency between 47 and 420 cps, single phase. These primary taps are brought out to terminal boards TB1 and TB2 to allow ac line input and jumper connections for operation at various line voltages (refer to Table 3-23.1).

Table 3-23.1.
Transformer Primary Connections for Different Input Voltages

Input Voltage, VAC (RMS)	Connect Input Line Voltage to Terminals	Connect Jumper Wire Between Terminals
100	TB1-1 and TB1-2	TB1-1 and TB2-1 TB1-2 and TB2-2
115	TB1-1 and TB1-3	TB1-1 and TB2-1 TB1-3 and TB2-3

Table 3-23.1. (Cont)
Transformer Primary Connections for Different Input Voltages

Input Voltage, VAC (RMS)	Connect Input Line Voltage to Terminals	Connect Jumper Wire Between Terminals
120	TB1-1 and TB1-4	TB1-1 and TB2-1 TB1-4 and TB2-4
127	TB1-1 and TB1-5	TB1-1 and TB2-1 TB1-5 and TB2-5
200	TB1-1 and TB2-2	TB1-2 and TB2-1
220	TB1-1 and TB2-4	TB1-2 and TB2-1
230	TB1-1 and TB2-3	TB1-3 and TB2-1
240	TB1-1 and TB2-4	TB1-4 and TB2-1

SPECIFICATIONS

Input Power Requirements

Input Voltage: 100, 115, 120, 127, 200, 220, 230, and 240 vac ±10%

Frequency: 47 to 420 cps, single phase

Current: PB-330: 0.30 amps (max)
PB-331: 1.75 amps (max)

Output

Model	Voltage and Load Current
PB-330	+6v, 0 to 2.5 amp (max)
	-6v, 0 to 0.25 amp (max)
PB-331	+6v, 0 to 10 amp (max)
	-6v, 0 to 1.0 amp (max)

Voltage Adjustment

±2% for both voltages

Regulation

Better than ±1% for line and load

Stability

Better than 0.05%/°C over temperature range

Ripple

+6v: 100 mv (max)

-6v: 100 mv (max)

Operating Temperature Range

0°C to +55°C at full load

NOTE

If the PB-330 or PB-331 is operated out of a μ-BLOC, air must be supplied to the heat sink at a minimum rate of 50 cu ft/min.

Size

PB-330: 8-3/4 in. high x 2-3/4 in. wide x 4-1/2 in. deep

PB-331: 8-3/4 in. high x 5-1/2 in. wide x 4-1/2 in. deep

Weight

PB-330: 8 lb (max)

PB-331: 17 lb (max)

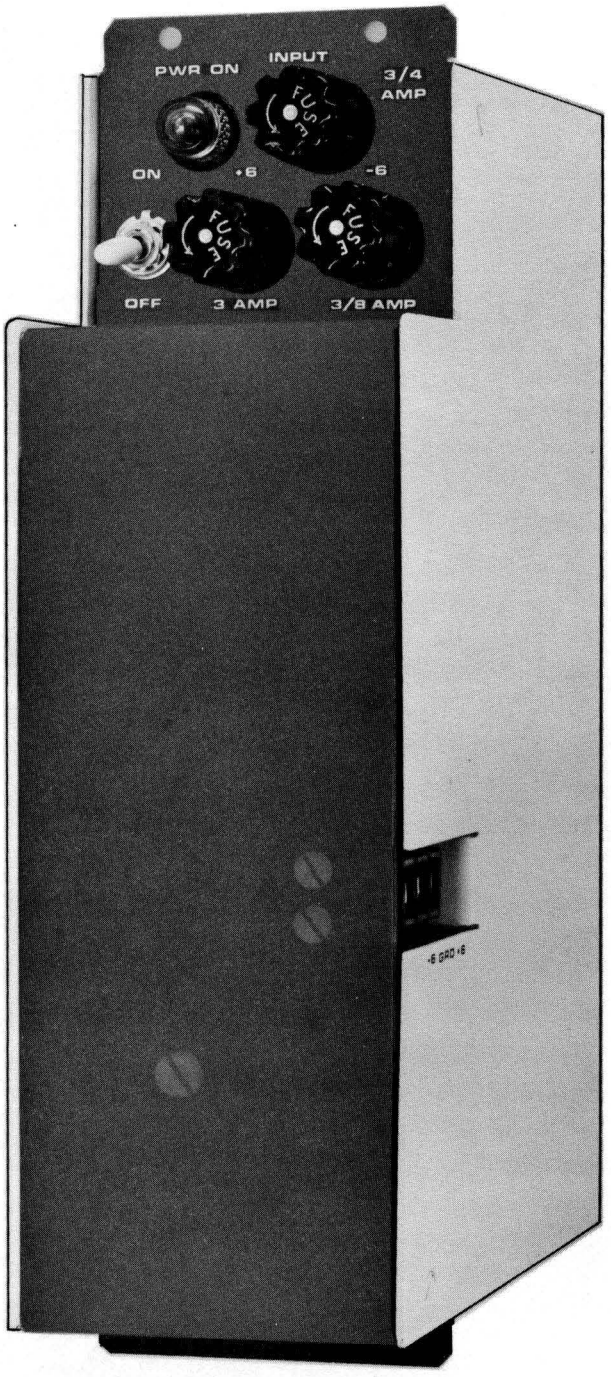


Figure 3-23.1. Plug-In Power Supply, Model PB-330

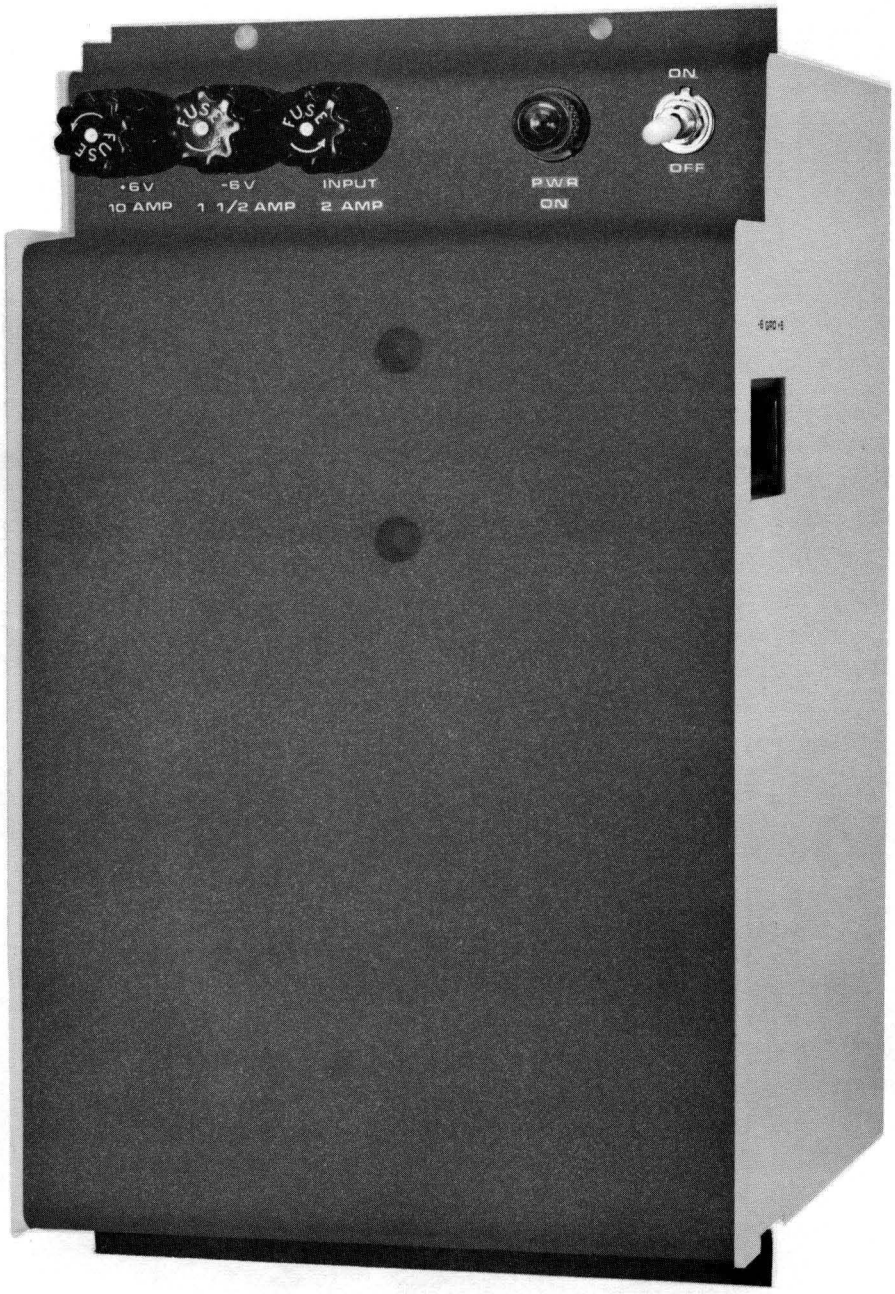


Figure 3-23.2. Plug-In Power Supply, Model PB-331

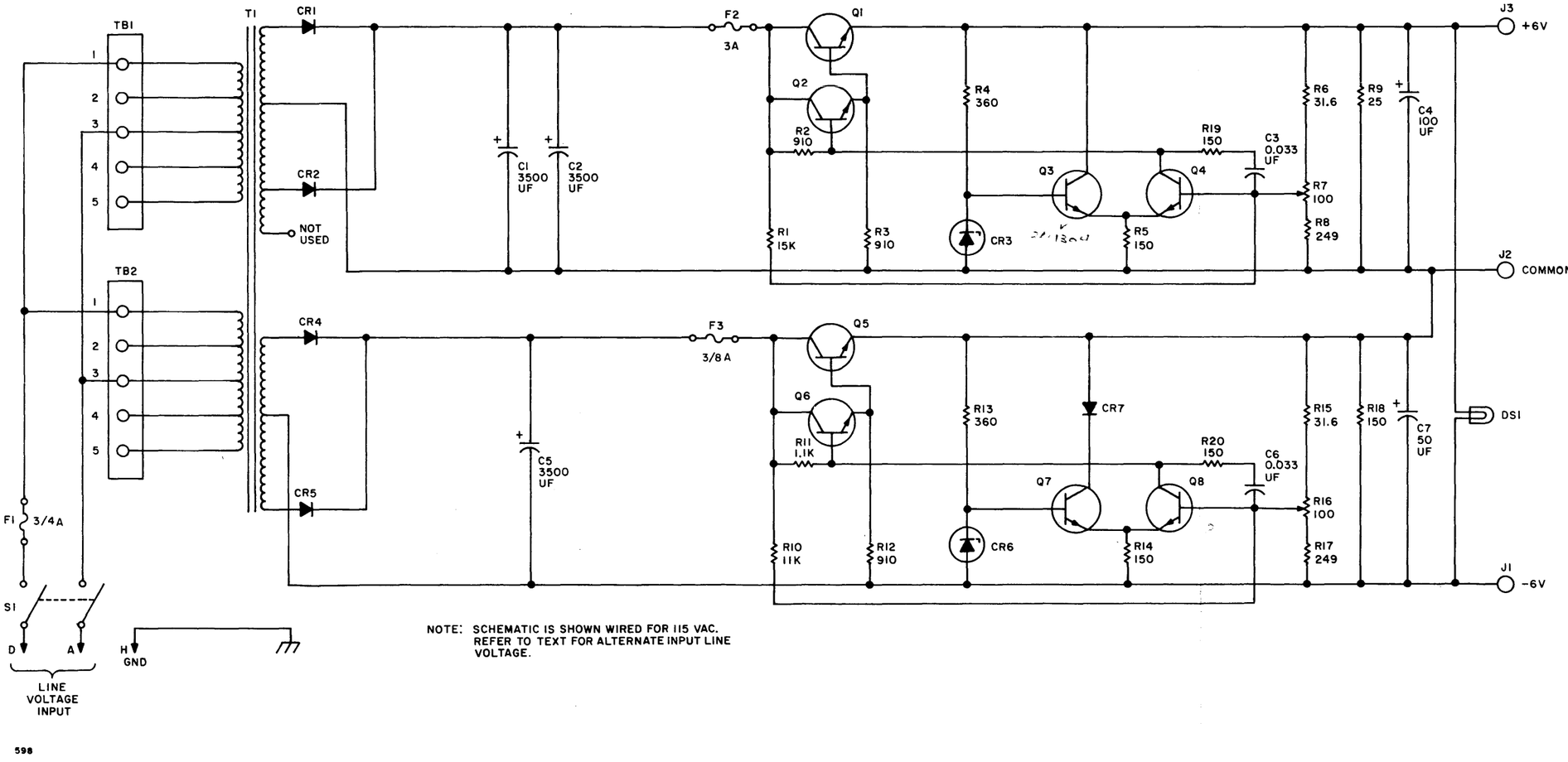


Figure 3-23.3. Plug-In Power Supply, Model PB-330, Schematic Diagram

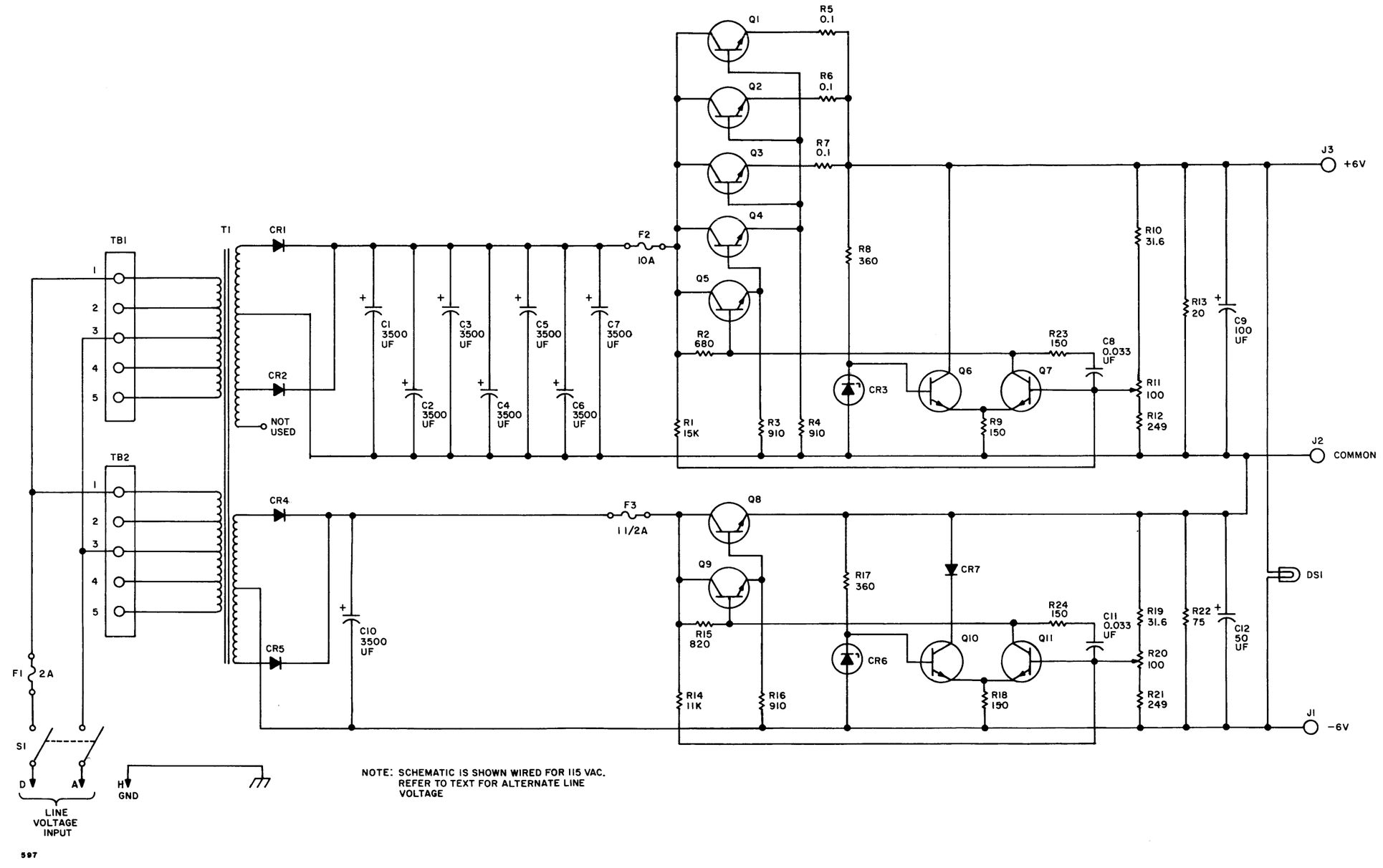


Figure 3-23.4. Plug-In Power Supply, Model PB-331, Schematic Diagram

Table 3-23.2.
Plug-In Power Supply, Model PB-330, Parts List

Ref. Desig.	Description	3C Part No.
C1, C2, C5	CAPACITOR, FIXED, ELECTROLYTIC: 3500 μf - 10% to +100%, 20 vdc	930 229 002
C3, C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C4	CAPACITOR, FIXED, ELECTROLYTIC: 100 μf -10% to +75%, 12 vdc	930 220 215
C7	CAPACITOR, FIXED, ELECTROLYTIC: 50 μf -10% to +75%, 12 vdc	930 220 213
CR1, CR2	DIODE: Replacement Type 1N1613	943 306 001
CR3, CR6	DIODE: Replacement Type 1N750A	943 110 005
CR4, CR5	DIODE: Replacement Type 1N3193	943 311 001
CR7	DIODE: Replacement Type 1N914	943 083 001
DS1	LAMP, INCANDESCENT	945 002 001
F1	FUSE, CARTRIDGE: 3/4 amp, 125v Replacement Type Bussman MDL Series or equivalent	960 001 017
F2	FUSE, CARTRIDGE: 3 amps, 250v Replacement Type Bussman AGC Series or equivalent	960 002 010
F3	FUSE, CARTRIDGE: 3/8 amp, 250v Replacement Type Bussman AGC Series or equivalent	960 002 004
J1	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 612
J2	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 012
J3	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 212
Q1	TRANSISTOR: Replacement Type 2N3055	943 732 003
Q2	TRANSISTOR: Replacement Type 2N3053	943 732 001
Q3, Q4, Q6-Q8	TRANSISTOR: Replacement Type Sprague Elec. TN-61	943 733 002
Q5	TRANSISTOR: Replacement Type 2N3054	943 732 002
R1	RESISTOR, FIXED, COMPOSITION: 15 K ±5%, 1/2w	932 004 077
R2, R3, R12	RESISTOR, FIXED, COMPOSITION: 910 ohms ±5%, 1/2w	932 004 048
R4, R13	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/2w	932 004 038
R5, R14, R18, R19, R20	RESISTOR, FIXED, COMPOSITION: 150 ohms ±5%, 1/2w	932 004 029

Table 3-23.2. (Cont)
Plug-In Power Supply, Model PB-330, Parts List

Ref. Desig.	Description	3C Part No.
R6, R15	RESISTOR, FIXED, FILM: 31.6 ohms ±2%, 1/4w	932 111 025
R7, R16	RESISTOR, VARIABLE, WIREWOUND: 100 ohms ±5%, 1w	933 207 004
R8, R17	RESISTOR, FIXED, FILM: 249 ohms ±2%, 1/4w	932 111 120
R9	RESISTOR, FIXED, WIREWOUND: 25 ohms ±3%, 3w	932 206 208
R10	RESISTOR, FIXED, COMPOSITION: 11 K ±5%, 1/2w	932 004 074
R11	RESISTOR, FIXED, COMPOSITION: 1.1 K ±5%, 1/2w	932 004 050
S1	SWITCH, TOGGLE, DPST	934 006 001
T1	TRANSFORMER	938 160 001

Table 3-23.3.
Plug-In Power Supply, Model PB-331, Parts List

Ref. Desig.	Description	3C Part No.
C1-C7, C10	CAPACITOR, FIXED, ELECTROLYTIC: 3500 μf -10% to +100%, 20 vdc	930 229 002
C8, C11	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C9	CAPACITOR, FIXED, ELECTROLYTIC: 100 μf -10% to +75%, 12 vdc	930 220 215
C12	CAPACITOR, FIXED, ELECTROLYTIC: 50 μf -10% to +75%, 12 vdc	930 220 213
CR1, CR2	DIODE: Replacement Type 1N1613	943 306 001
CR3, CR6	DIODE: Replacement Type 1N750A	943 110 005
CR4, CR5	DIODE: Replacement Type 1N3193	943 311 001
CR7	DIODE	943 083 001
DS1	LAMP, INCANDESCENT	945 002 001
F1	FUSE, CARTRIDGE: 2 amp, 125v Replacement Type Bussman MDL Series or equivalent	960 001 024
F2	FUSE, CARTRIDGE: 10 amp, 250v Replacement Type Bussman AGC Series or equivalent	960 002 015
F3	FUSE, CARTRIDGE: 1.5 amp, 250v Replacement Type Bussman AGC Series or equivalent	960 002 008
J1	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 012
J2	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 212
J3	CONNECTOR, RECEPTACLE, ELECTRICAL	941 307 612
Q1-Q3, Q8	TRANSISTOR: Replacement Type 2N3055	943 732 003
Q4	TRANSISTOR: Replacement Type 2N3054	943 732 002
Q5-Q7, Q9-Q11	TRANSISTOR: Replacement Type Sprague Electric TN-61	943 733 002
R1	RESISTOR, FIXED, COMPOSITION: 15 K ±5%, 1/2w	932 004 077
R2	RESISTOR, FIXED, COMPOSITION: 680 ohms ±5%, 1/2w	932 004 045
R3, R4, R16	RESISTOR, FIXED, COMPOSITION: 910 ohms ±5%, 1/2w	932 004 048
R5-R7	RESISTOR, FIXED, WIREWOUND: 0.1 ohm ±5%, 2w	932 213 001
R8, R17	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/2w	932 004 039

Table 3-23.3. (Cont)
Plug-In Power Supply, Model PB-331, Parts List

Ref. Desig.	Description	3C Part No.
R9, R18, R23, R24	RESISTOR, FIXED, COMPOSITION: 150 ohms ±5%, 1/2w	932 004 029
R10, R19	RESISTOR, FIXED, FILM: 31.6 ohms ±2%, 1/4w	932 111 025
R11, R20	RESISTOR, VARIABLE WIREWOUND: 100 ohms ±5%, 1w	933 207 004
R12, R21	RESISTOR, FIXED, FILM: 249 ohms ±2%, 1/4w	932 111 120
R13	RESISTOR, FIXED, WIREWOUND: 20 ohms ±3%, 3w	932 206 207
R14	RESISTOR, FIXED, COMPOSITION: 11K ±5%, 1/2w	932 004 074
R15	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, 1/2w	932 004 047
R22	RESISTOR, FIXED, COMPOSITION: 75 ohms ±3%, 3w	932 206 212
S1	SWITCH, TOGGLE, DPST	934 006 001
T1	TRANSFORMER	938 161 001

3-23A MOUNTING PANELS, MODELS PM-330 and PM-331

Mounting Panels, Models PM-330 and PM-331, are designed to adapt the BM series of μ-BLOCs for mounting on standard 19-in. RETMA relay racks. The PM-330 is designed for use with 5-11/16-in. wide μ-BLOCs (BM-330), while the PM-331 is used for 8-7/16 in. wide μ-BLOCs (BM-335 and BM-337).

The mounting panels may be attached to either the PAC end or the connector end (Figure 3-23A. 1) of the μ-BLOC and on either side of the BLOC. The panel is secured to the BLOC with three 8/32 x 3/8 in. flat head screws. These screws are the same as those used for the 1-in. mounting flanges normally on the BLOC.

When mounted, the panels can also be used as control panels for indicator lamps, switches, and other uses.

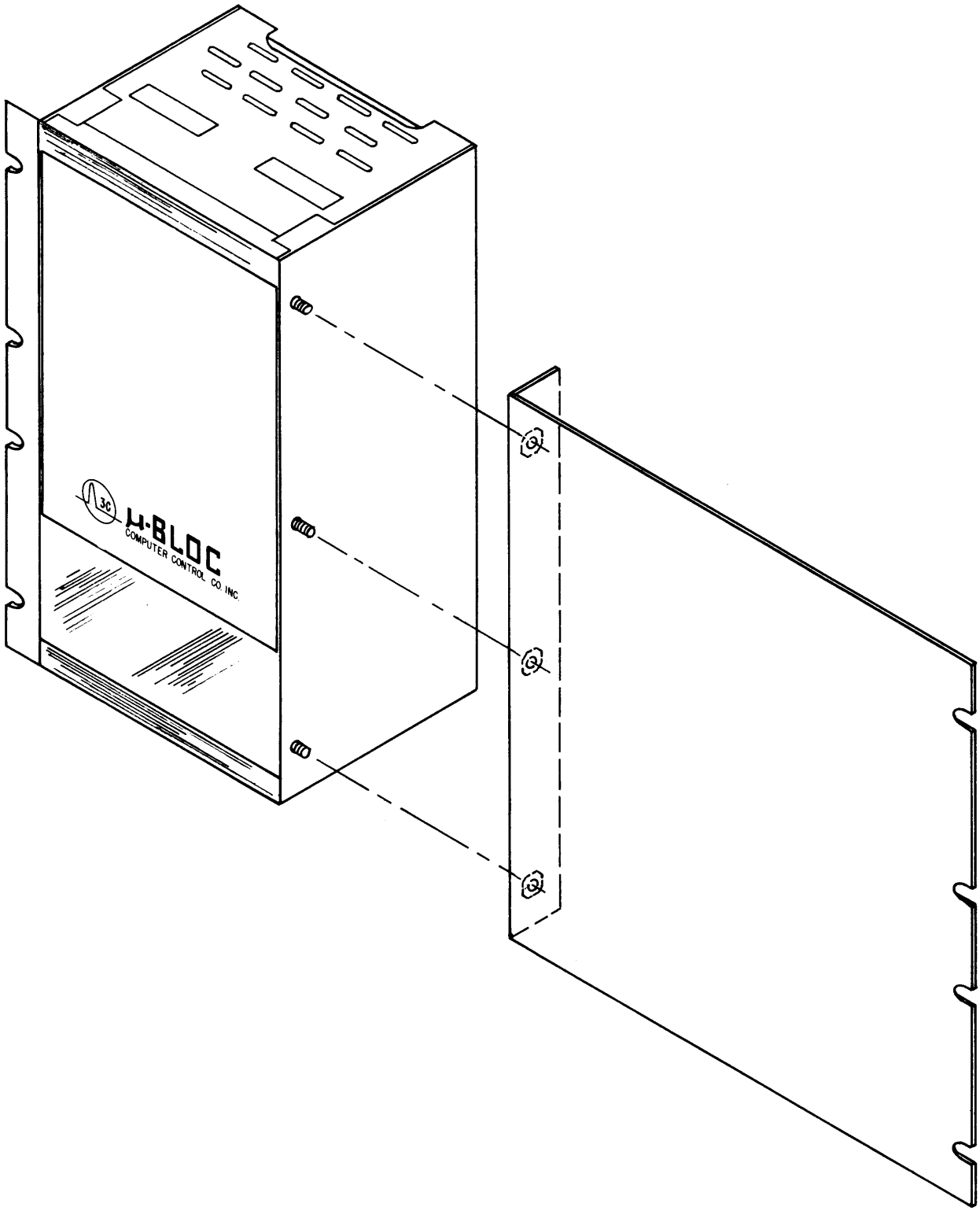


Figure 3-23A. 1 μ-BLOC and Mounting Panel Assembly

3-23B NON-INVERTING POWER AMPLIFIER PAC, MODEL PN-335

The Non-Inverting Power Amplifier PAC, Model PN-335 (Figures 3-23B. 1 and 3-23B. 2), contains six microcircuit 3-input AND gates that can be used for driving heavy loads. Each gate contains two inverting amplifiers so that the output has the same polarity as the input. Built-in short-circuit protection limits output current if the output is accidentally grounded.

CIRCUIT FUNCTION

Each gate performs the AND function for positive logic (positive voltage is a ONE and 0v is a ZERO), or an OR function for negative logic. When all inputs to a gate are at positive or not connected, the output goes to +6v. When any input is at ground the output goes to ground.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Circuit Delay (measured at +1. 5v)

50 nsec (max)

Output Drive Capability

25 unit loads

Current Requirements

+6v: 110 ma (max)

Power Dissipation

Static: 660 mw

Dynamic: 960 mw at 5 mc
with 250 pf stray capacitance

Handle Color Code

Green

APPLICATIONS

The power gates operate on levels, pulses, or with combinations of both.

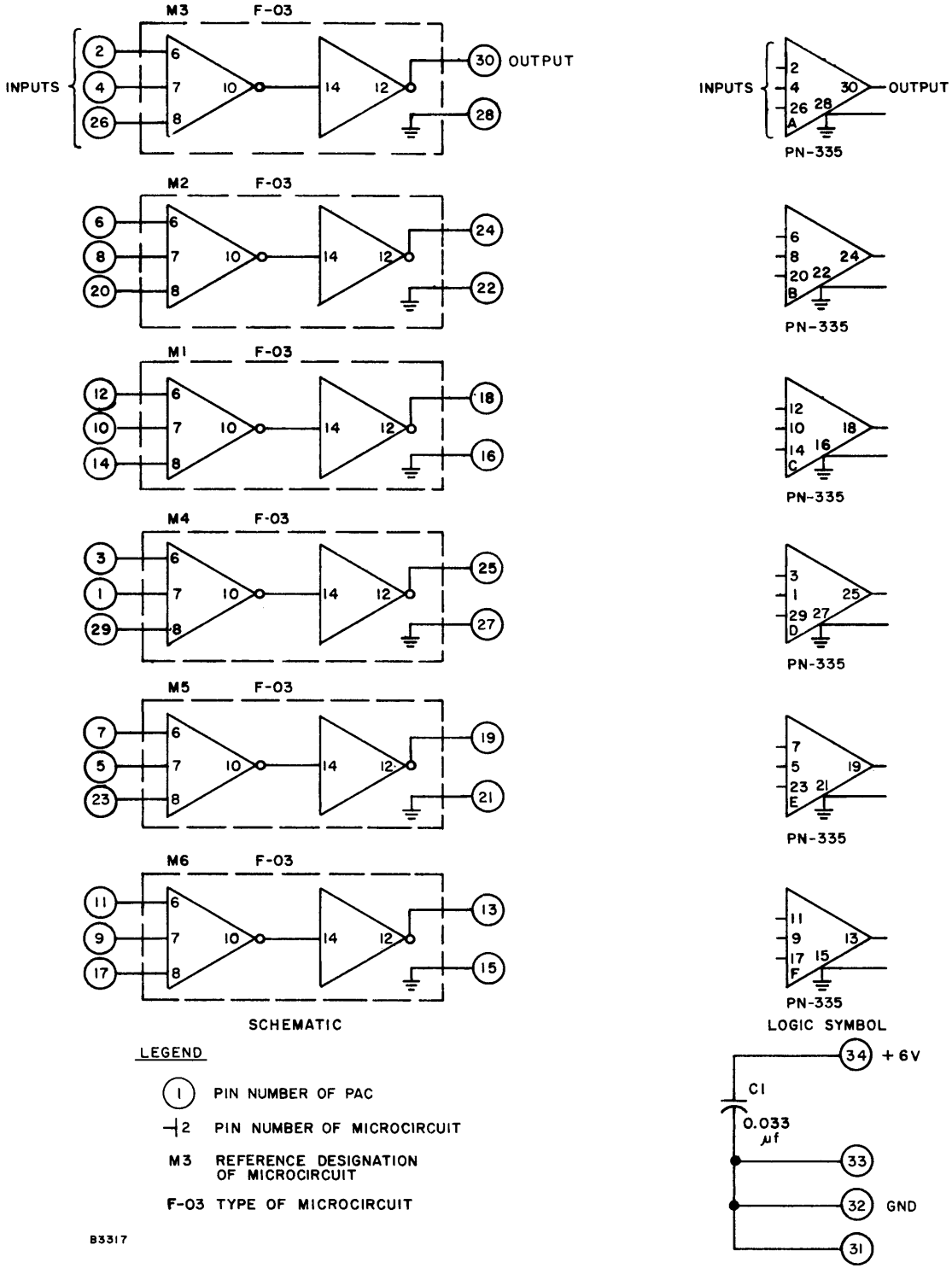
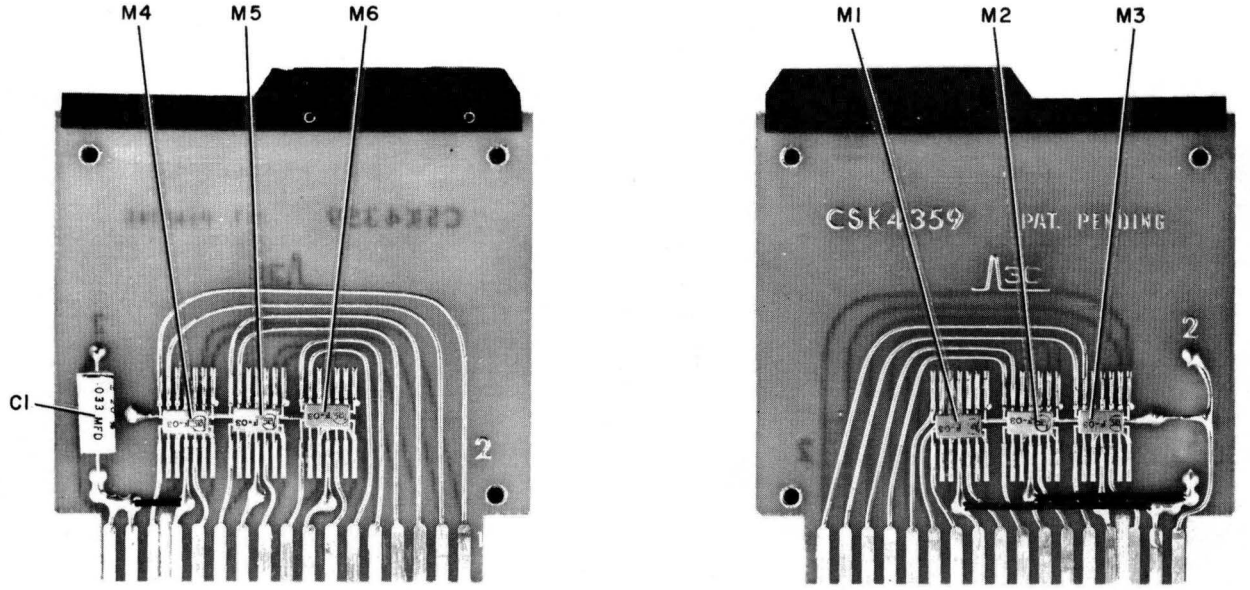


Figure 3-23B.1. Non-Inverting Power Amplifier PAC, Model PN-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref Desig	Description	3C Part No.
M1 - M6	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-23B.2. Non-Inverting Power Amplifier PAC, Model PN-335, Parts Location and Identification

3-24 POWER SUPPLY, MODEL RP-330

The Power Supply, Model RP-330 (Figure 3-24.1), is an integrally packaged, regulated power source that supplies two μ-PAC voltages (+6v and -6v) with proportioned current capability. The supply is substantially derated at maximum specified load and can be operated safely at full load over its specified environmental temperature range. In specific cases it may be possible to operate the supply slightly beyond its ratings, when used in an air-conditioned laboratory environment. The supply employs a ferroresonant transformer to minimize the effects of the line voltage variations, and uses high-gain, solid-state regulator circuits to achieve excellent ripple regulation and stability.

The schematic shown in Figure 3-24.2 is wired for 115-v, 60-cycle operation. Alternate transformer primary and secondary connections for input voltage and frequency of operation are listed in Tables 3-24.1 and 3-24.2.

The RP-330 can be mounted in a standard 19-in. relay rack. Power supply features include an ac power ON indicator light, and dc outputs which are protected by fast-acting circuit breakers. An indicator light is also provided to show a dc power failure. All supplies are factory preset for the proper value of voltage. A screwdriver adjustment is provided for recalibration if necessary. (Range of adjustment is 2%.) The supply is floating with respect to ground; a chassis ground terminal is provided.

SPECIFICATIONS

Input Power Requirements

Input voltage and frequency:

a) 100, 115, and 120v rms ±10%, 60 cps, single phase

b) 100, 115, 120, 127, 200, 220, 230, and 240v rms ±10%, 50 cps, single phase

Current: 5 amp (max) at 100v and less for higher voltages

Output	Ripple
+6v, 0 to 25.0 amp (max)	+6v: 75 mv (max)
-6v, 0 to 2.5 amp (max)	-6v: 75 mv (max)
Voltage Adjustment	**Operating Temperature Range**
±2% for both voltages	-20°C to +55°C at full load
Regulation	**Size**
Better than ±0.75% for load (0 to max) and ±10% line change	5-1/4 in. high x 19 in. wide x 15 in. deep (relay rack mounting)
Stability	**Weight**
Better than ±0.03%/°C over the temperature range	60 lb (max)

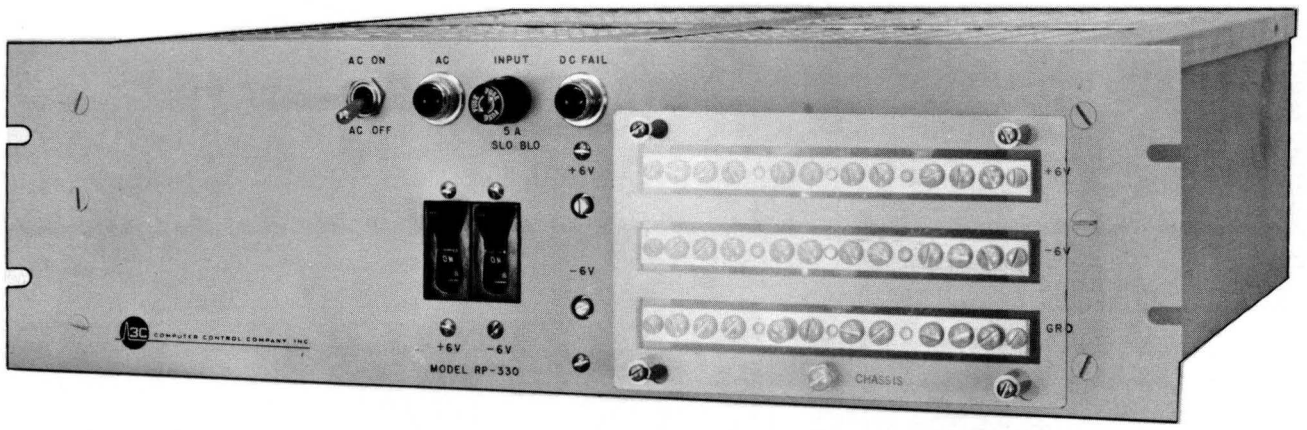


Figure 3-24.1. Power Supply, Model RP-330

Table 3-24.1.
Transformer Primary Connections for Alternate Input Voltage and Frequency

Input Voltage	Connect Input Line Voltage to Terminals	Connect Jumper Wire Between Terminals
100 vac, 60 cps	1 and 2	1 and 6; 2 and 7
115 vac, 60 cps	1 and 3	1 and 6; 3 and 8
120 vac, 60 cps	1 and 3	1 and 6; 3 and 8
100 vac, 50 cps	1 and 3	1 and 6; 3 and 8
115 vac, 50 cps	1 and 4	1 and 6; 4 and 9
120 vac, 50 cps	1 and 4	1 and 6; 4 and 9
127 vac, 50 cps	1 and 5	1 and 6; 5 and 10
200 vac, 50 cps	1 and 7	4 and 6
220 vac, 50 cps	1 and 8	4 and 6
230 vac, 50 cps	1 and 11	3 and 6
240 vac, 50 cps	1 and 9	4 and 6

Table 3-24.2.
Transformer Secondary Connections for Alternate Frequency

50-Cycle Operation Terminal	60-Cycle Operation Terminal
12	13
16	15
17	18
21	20
22	23
24	25
28	27
30	29

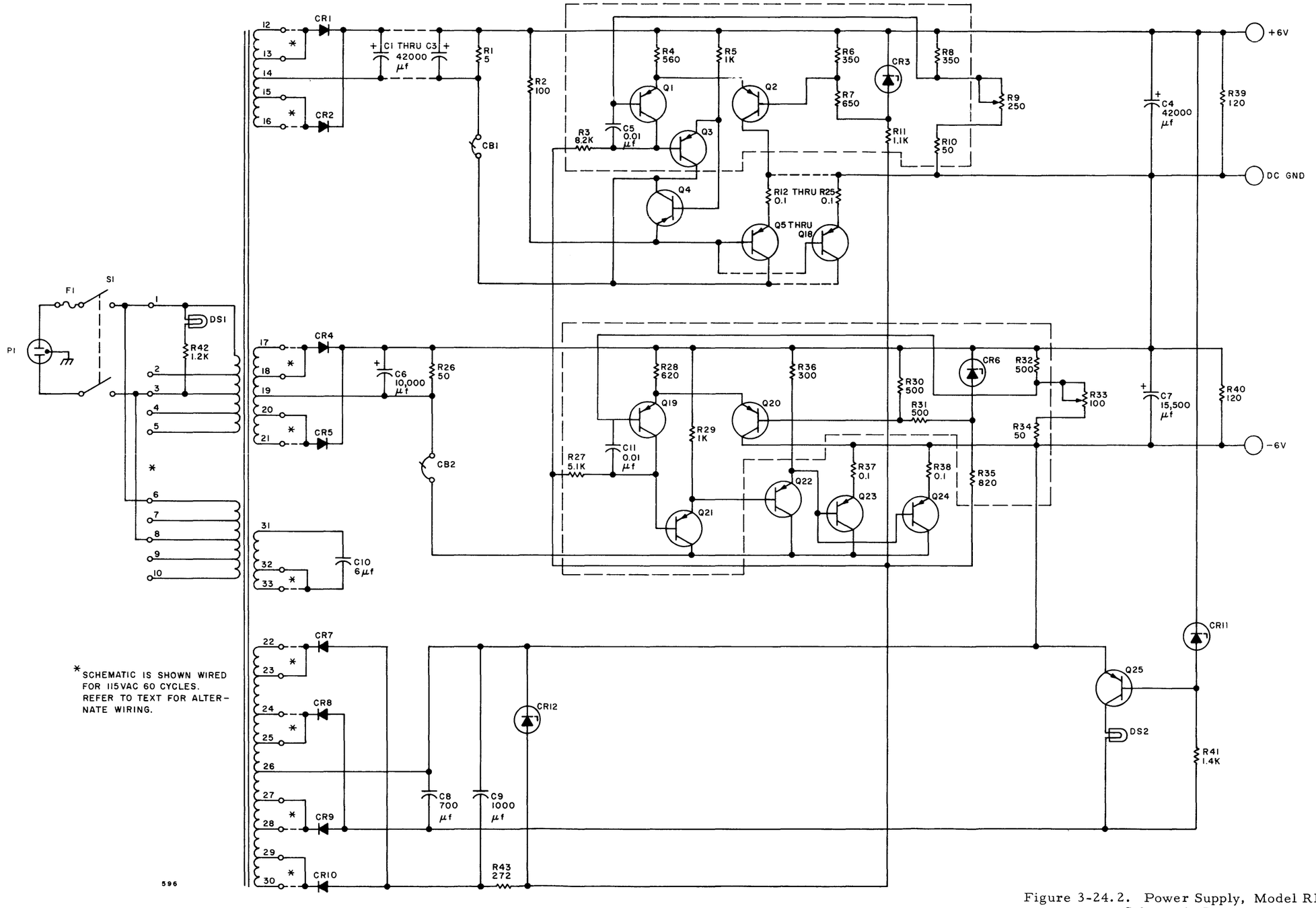


Figure 3-24.2. Power Supply, Model RP-330, Schematic Diagram

Table 3-24.3.
Power Supply, Model RP-330, Parts List

Ref. Desig.	Description	Part No.
C1-C4	CAPACITOR, FIXED, ELECTROLYTIC: 42,000 μf, 15 vdc	3041099
C5, C11	CAPACITOR, FIXED, ELECTROLYTIC: 0.01 μf, 100 vdc	3040716
C6	CAPACITOR, FIXED, ELECTROLYTIC: 10,000 μf, 15 vdc	3040690
C7	CAPACITOR, FIXED, ELECTROLYTIC: 15,500 μf, 10 vdc	3040742
C8	CAPACITOR, FIXED, ELECTROLYTIC: 700 μf, 35 vdc	3040963
C9	CAPACITOR, FIXED, ELECTROLYTIC: 1000 μf, 45 vdc	3040834
C10	CAPACITOR, FIXED 6 μf, 660 vac	3041007
CB1	CIRCUIT BREAKER: 28 amp	3050204
CB2	CIRCUIT BREAKER: 3 amp	3050118
CR1, CR2	DIODE: Replacement Type 1N1183	3371205
CR3, CR6	DIODE, Zener	3371230
CR4, CR5	DIODE	3371185
CR7, CR10	DIODE: Replacement Type 1N4003	3371279
CR8, CR9	DIODE: Replacement Type 1N4001	3371266
CR11	DIODE, Zener: Replacement Type 1N757	0535833
CR12	DIODE, Zener: Replacement Type 1N1778A	0529748
DS1	LAMP, INDICATOR, POWER ON	3220048
DS2	LAMP, INDICATOR, DC FAILURE	3220037
F1	FUSE	3150146
P1	CONNECTOR, ELECTRIC	3330123
Q1-Q3, Q19-Q21, Q25	TRANSISTOR: Replacement Type 2N527	3700029
Q4	TRANSISTOR: Replacement Type 2N1544	3700044

Table 3-24.3. (Cont)
Power Supply, Model RP-330, Parts List

Ref. Desig.	Description	Part No.
Q5-Q18, Q23, Q24	TRANSISTOR: Replacement Type 2N2082	3700103
Q22	TRANSISTOR: Replacement Type 2N1038	3700028
R1	RESISTOR, FIXED: 5 ohms ±10%, 25w	3407405
R2	RESISTOR, FIXED: 100 ohms ±5%, 2w	3400824
R3	RESISTOR, FIXED: 8.2 K ±5%, 1/2w	3400175
R4	RESISTOR, FIXED: 560 ohms ±5%, 1/2w	3400147
R5, R29	RESISTOR, FIXED: 1 K ±5%, 1/2w	3400153
R6, R8	RESISTOR, FIXED: 350 ohms ±1%, 3w	3405112
R7	RESISTOR, FIXED: 650 ohms ±1%, 3w	3405147
R9	RESISTOR, VARIABLE: 250 ohms ±5%, 2w	3410523
R10, R34	RESISTOR, FIXED: 50 ohms ±1%, 3w	3405126
R11	RESISTOR, FIXED: 1.1K ±5%, 2w	3400849
R12-R25, R37, R38	RESISTOR, FIXED: 0.1 ohm ±5%, 3w	3405158
R26	RESISTOR, FIXED: 50 ohms ±5%, 10w	3407216
R28	RESISTOR, FIXED: 620 ohms ±5%, 1/2w	3400148
R30-R32	RESISTOR, FIXED: 500 ohms ±1%, 3w	3405013
R33	RESISTOR, VARIABLE: 100 ohms ±5%, 2w	3410573
R35	RESISTOR, FIXED: 820 ohms ±5%, 2w	3400846
R36	RESISTOR, FIXED: 300 ohms ±5%, 1/2w	3400140

Table 3-24.3. (Cont)
Power Supply, Model RP-330, Parts List

Ref. Desig.	Description	Part No.
R39, R40	RESISTOR, FIXED: 120 ohms ±5%, 1w	3400603
R41	RESISTOR, FIXED: 1.4 K ±1%, 3w	3405186
R42	RESISTOR, FIXED: 1.2 K ±5%, 5w	3401673
R43	RESISTOR, FIXED: 272 ohms ±1%, 3w	3405123
S1	SWITCH, TOGGLE, DPST	3660251
VR1	TRANSFORMER, REGULATED, FERROMAGNETIC	6113837

3-25 SOLENOID DRIVER PAC, MODEL SD-330

The Solenoid Driver PAC, Model SD-330 (Figures 3-25.1 and 3-25.2), contains three independent circuits for driving heavy resistive, capacitive or inductive loads. Each circuit is capable of switching up to 1 amp of current from a positive supply of up to 28v. The PAC also contains one independent two-input NAND gate. A detailed description of the NAND circuit is given in Section II.

Logically, each driver circuit acts as a two-input NAND gate. When both inputs are at logic ONE (positive voltage or disconnected), the output is high (solenoid supply voltage) and the solenoid is de-energized. When either or both of the inputs are at logic ZERO (ground), the output is low (ground) and the solenoid is energized. The operation is summarized in Table 3-25.1.

CIRCUIT FUNCTION

Each solenoid circuit is composed of a two-input NAND gate microcircuit, which drives a transistor amplifier-inverter. If either or both inputs to the NAND gate are 0v, the output transistor of the gate will be off, causing current to flow into the base of Q1. When Q1 and Q2 are on, the solenoid is energized, and the current from the external supply flows through the solenoid to ground through Q1 and Q2. If both inputs are positive, the output of the NAND gate will be ground, biasing Q1 and Q2 off. When these transistors are turned off, the solenoid is de-energized and the energy stored in the coil is damped by the diode-resistor combination CR1 and R3. This is necessary to protect the output transistors from excessive overshoot voltage.

INPUT AND OUTPUT SIGNALS

Input. -- This point is a NAND gate input.

SD Output. -- This output is connected to the negative terminal of an external load.

External Supply. -- This point is connected to the positive terminal of an external load. It should also be connected to the positive side of the external supply voltage.

External Return. -- This point should be connected to the negative side of the external supply voltage.

SPECIFICATIONS

Solenoid Driver Circuits

Frequency of Operation	Circuit Delay (switching 1 amp)
DC to 500 cps (max)	Turn on: 150 nsec (typ) Turn off: 400 nsec (typ)

Input Loading

1 unit load each

Output Drive Capability

1 amp at 28v*

Output Levels

Energizing solenoid: 0v to +1.5v

De-energizing solenoid: solenoid supply voltage

SD-330 PAC

Current Requirements

+6v: 50 ma (max) less loading

Power Dissipation

0.30w (max) not including effects of load current

Handle Color Code

Orange

NAND Gate

Frequency of Operation (System)

DC to 500 cps (max)

Input Loading

1 unit load each

Output Drive Capability

8 unit loads

Circuit Delay

Turn on: 400 nsec (typ)

Turn off: 150 nsec (typ)

APPLICATIONS

Figure 3-25.3 illustrates a typical application, using the PAC to drive a solenoid coil.

NOTE

The SD-330 occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

Table 3-25.1.
Truth Table

Input 1	Input 2	Solenoid Output
0v	0v	0v } Solenoid
0v	+6v	0v } is
+6v	0v	0v } energized
+6v	+6v	External voltage supply } Solenoid is de-energized

*Solderless-wrap connectors are rated at 1/3 amp (max) per wire (3 wraps permissible per terminal). Taper-pin connectors can carry full load on one wire. Because of high currents and inductive loading, leads should be kept separated from logic signal wiring.

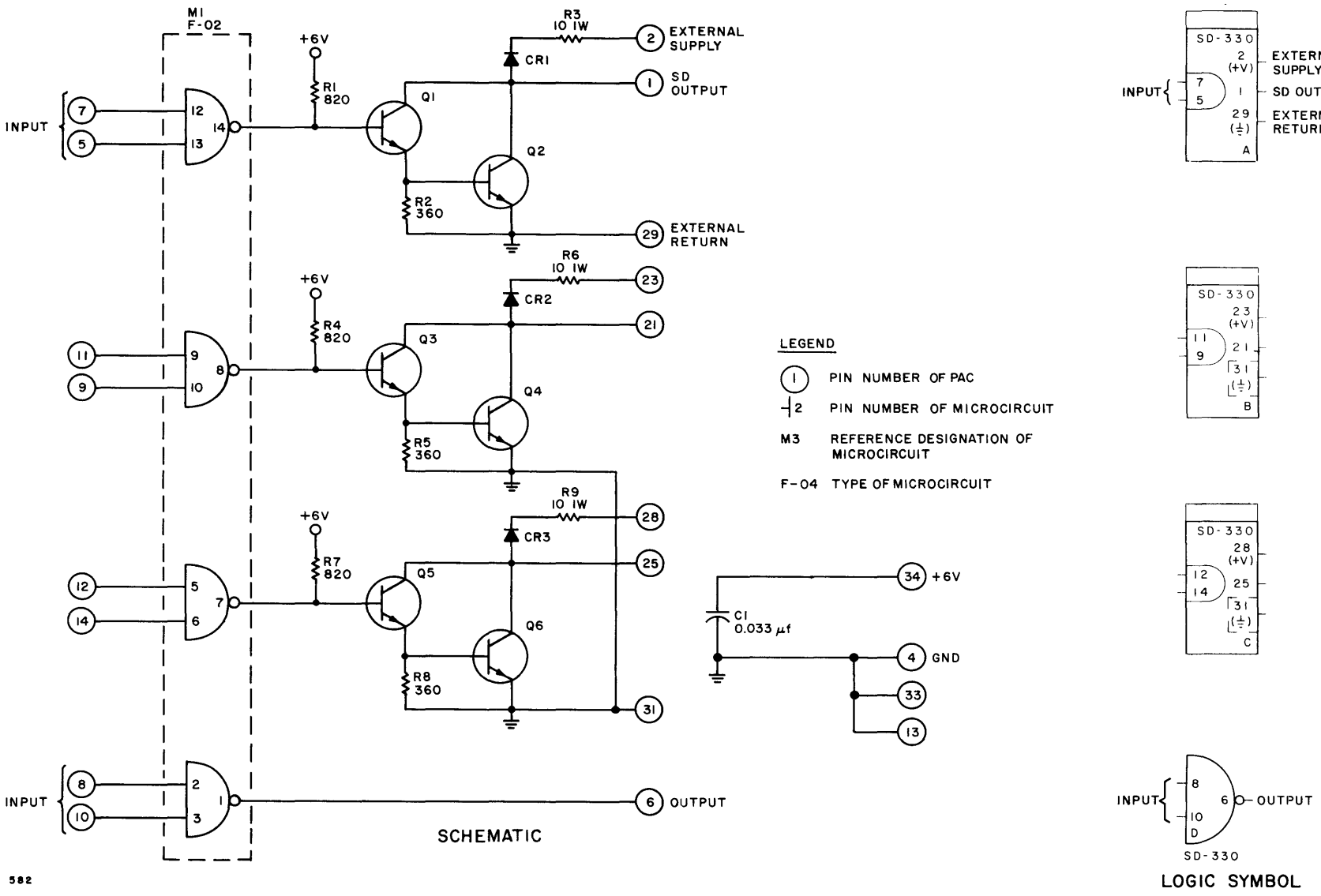
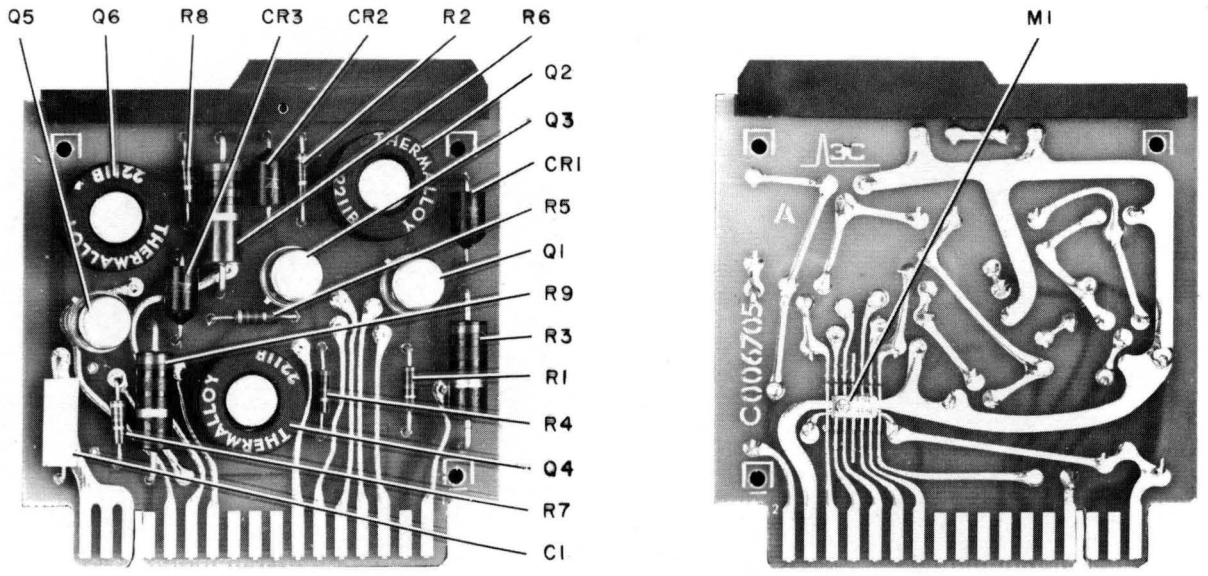


Figure 3-25. 1. Solenoid Driver PAC, Model SD-330, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR3	DIODE: Replacement Type 1N2069	943 303 001
Q1-Q6	TRANSISTOR: Replacement Type 2N2297	943 728 001
R1, R4, R7	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, 1/4w	932 007 047
R2, R5, R8	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/4w	932 007 038
R3, R6, R9	RESISTOR, FIXED, COMPOSITION: 10 ohms ±5%, 1w	932 005 001

Figure 3-25.2. Solenoid Driver PAC, Model SD-330, Parts Location and Identification

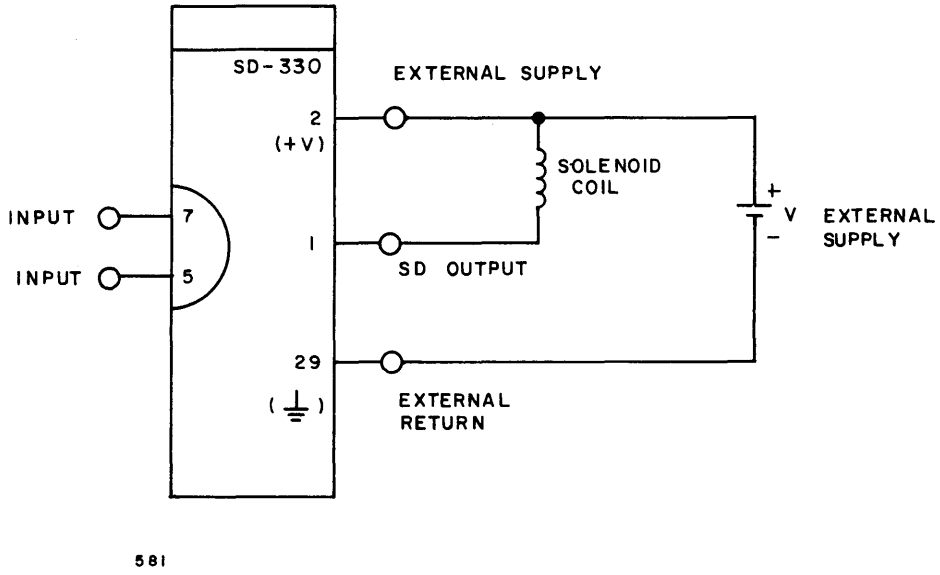


Figure 3-25. 3. Solenoid Driver PAC, Model SD-330, Driving a Solenoid Coil

3-25A SHIFT REGISTER PAC, MODEL SR-335

The Shift Register PAC, Model SR-335 (Figures 3-25A.1 and 3-25A.2), is built to order, with 8 to 16 prewired shift register stages. The set output of each stage and the reset outputs of the eighth and sixteenth stages are accessible at the PAC terminals. The shift register can be cleared by a reset signal that is applied to all stages simultaneously. Complementary input information is required at the first shift register stage. Information within the register is transformed one bit position after each shift pulse input. DC set inputs are provided for the first eight stages.

INPUT AND OUTPUT SIGNALS

Common Reset. -- A signal at logic ZERO for 80 nsec or longer on the common reset input clears all shift register stages.

Information Inputs. -- These inputs are the same as the control inputs of the integrated circuit flip-flop. Waveform requirements are shown in Section II. The inputs must be driven from complementary logic signals, such as the output of any μ-PAC flip-flop. If the input data is presented from the output of a gate (single-ended), an inverter must be provided between the set and reset control inputs.

Shift. -- The shift input is the same as the clock input of the integrated circuit flip-flop. Waveform requirements are shown in Section II. Information within the shift register is shifted on the negative (ONE to ZERO) transition.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC set: 2/3 unit load

Inputs: 1 unit load each

Common reset: 5 unit loads (8 stages, 2/3 unit load per stage)
10 unit loads (16 stages)

Shift: 8 unit loads (8 stages, 1 unit load per stage)
16 unit loads (16 stages)

Output Drive Capability

7 unit loads each

Circuit Delay

60 nsec (max)

Current Requirements (16 stages)

+6v: 400 ma (max)

Power Dissipation (16 stages)

2.4w (max)

Handle Color Code

Blue

APPLICATIONS

The SR-335 can be used for processing serial or serial/parallel information. Information may be entered into the shift register in serial and read out in parallel, or the information may be entered in parallel (after having first cleared the register) and then shifted out serially.

The 16-bit shift register may be loaded in the following manner:

1. Clear the register by using the common reset input.
2. Enter the first 8 bits of information in parallel by using the dc set inputs.
3. Shift 8 ZEROs into the register, moving the first 8 bits of information into the other half of the register.
4. Enter the second 8 bits of information in parallel by again using the dc set inputs.

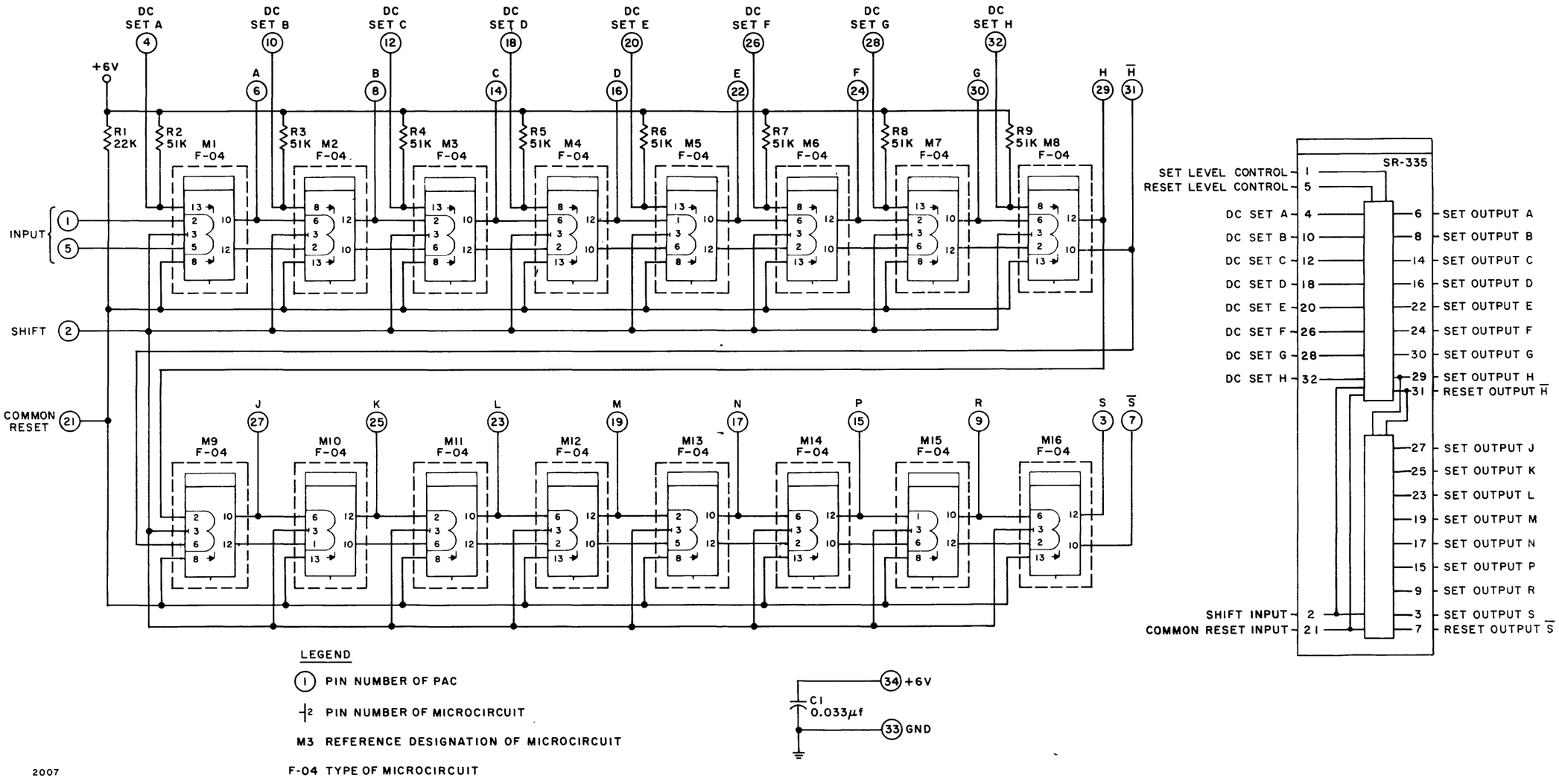
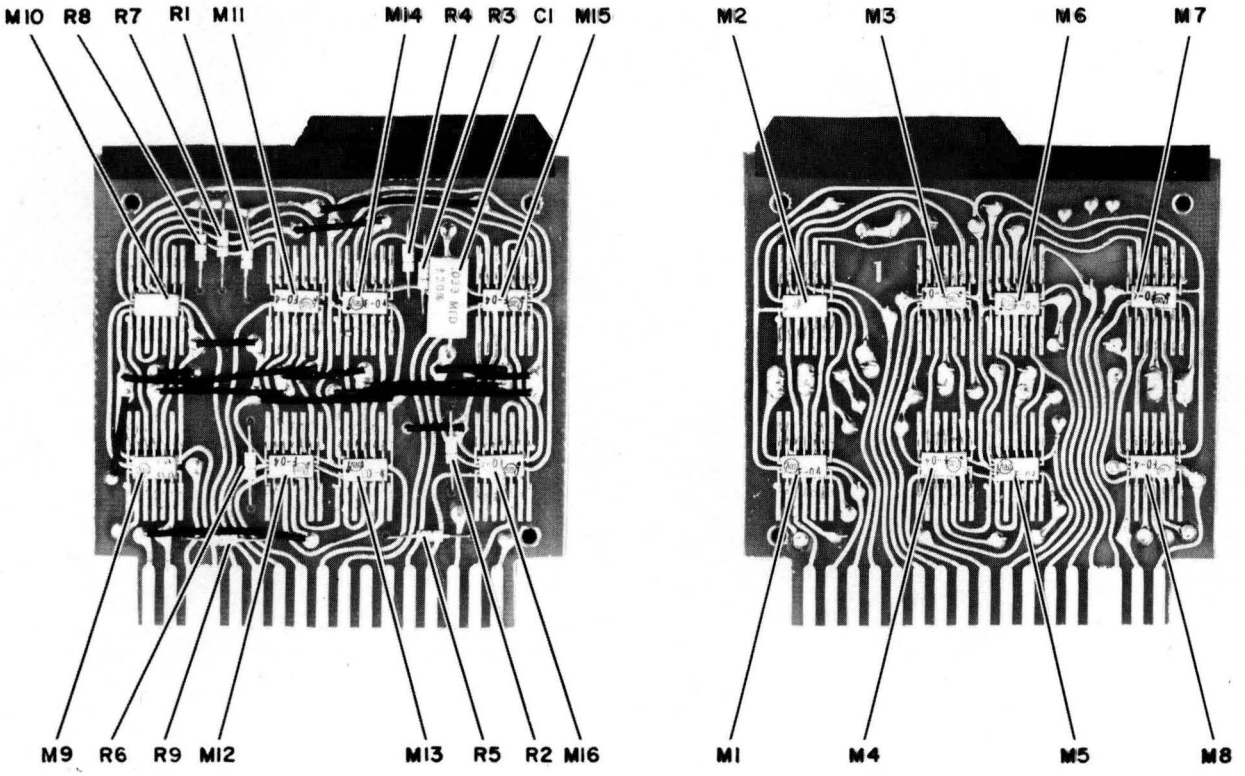


Figure 3-25A.1. Shift Register PAC, Model SR-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M16	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4w	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51K ±5%, 1/4w	932 007 090

Figure 3-25A.2. Shift Register PAC, Model SR-335, Parts Location and Identification

3-26 SCHMITT TRIGGER PAC, MODEL ST-335

The Schmitt Trigger PAC, Model ST-335 (Figures 3-26.1 and 3-26.2), contains two independent trigger circuits, each capable of converting arbitrarily shaped inputs to μ-PAC compatible outputs. The Schmitt trigger is versatile and can be used for such applications as pulse shaping, signal level shifting, level detecting, and level comparing. In addition, each circuit can perform signal attenuation, differentiation and integration by use of available resistor-capacitor networks.

Provisions are made at the input, whereby the input signal may be attenuated before it is applied to the base of the first transistor stage. The attenuating network will be needed only when the input signal exceeds the positive voltage supply of the PAC (usually +6v, or when the input signal is more negative than -20v).

CIRCUIT FUNCTION

Each circuit has a single input and output. The only amplitude restriction is that the input signal, which appears at the base of the input transistor, must not exceed the positive voltage supply to prevent input clipping. However, the signal may be as low as -20v with no detrimental effect. These input restrictions are independent of the switching levels. The output of each trigger circuit is directly compatible with the μ-PAC product line.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Output Drive Capability

8 unit loads and 40 pf stray capacitance each

Circuit Delay

20 nsec (typ)

Switching Levels

(Refer to Table 3-26.1)

Variation of Switching Levels Over Temperature

50 mv (max)

Input Signal at Base of Input Transistor

+6v (max positive)
-20v (max negative)

Current Requirements

+6v: 90 ma (max)
-6v: 60 ma (max)

Power Dissipation

0.90w (max)

Handle Color Code

Orange

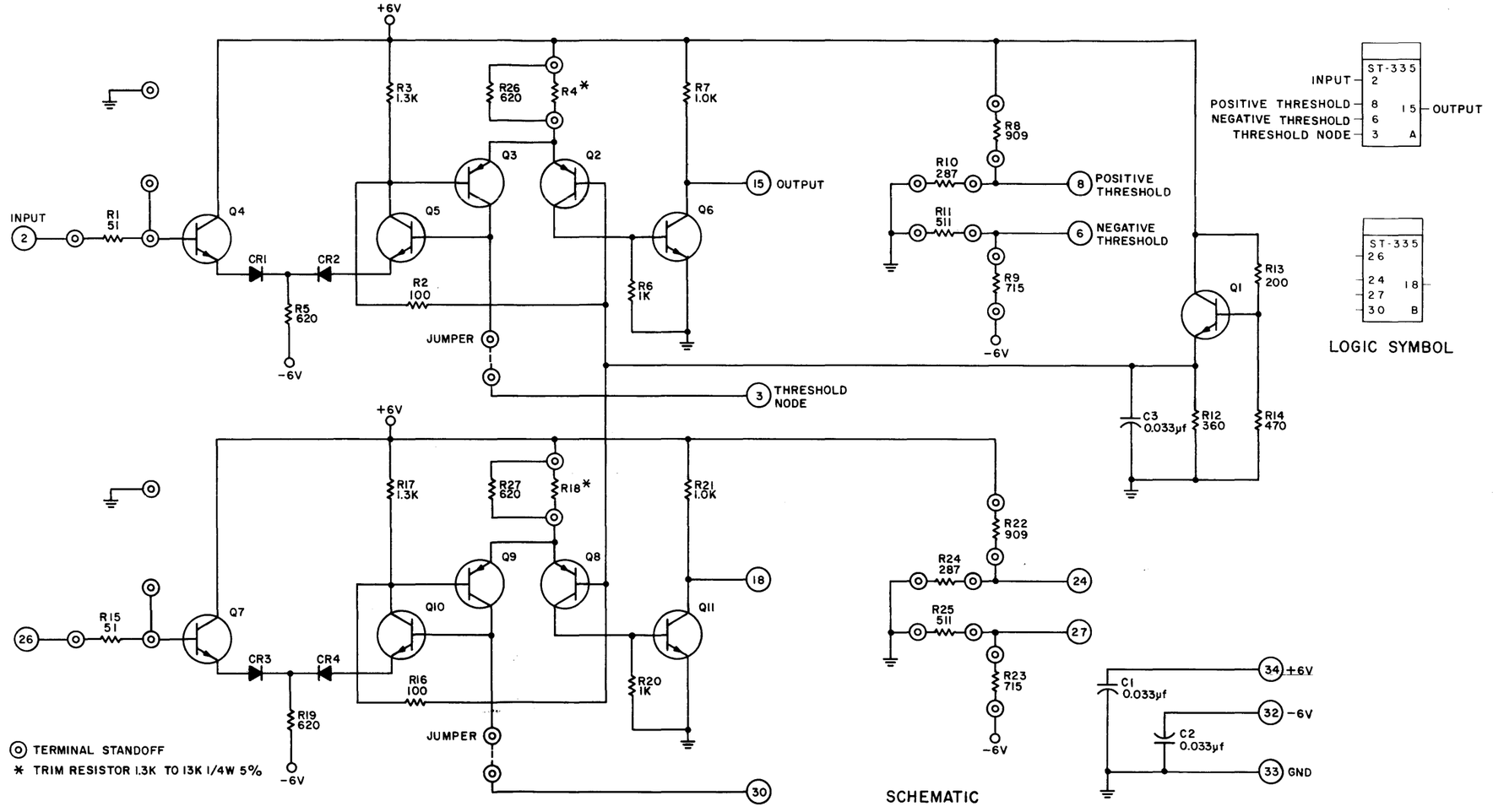
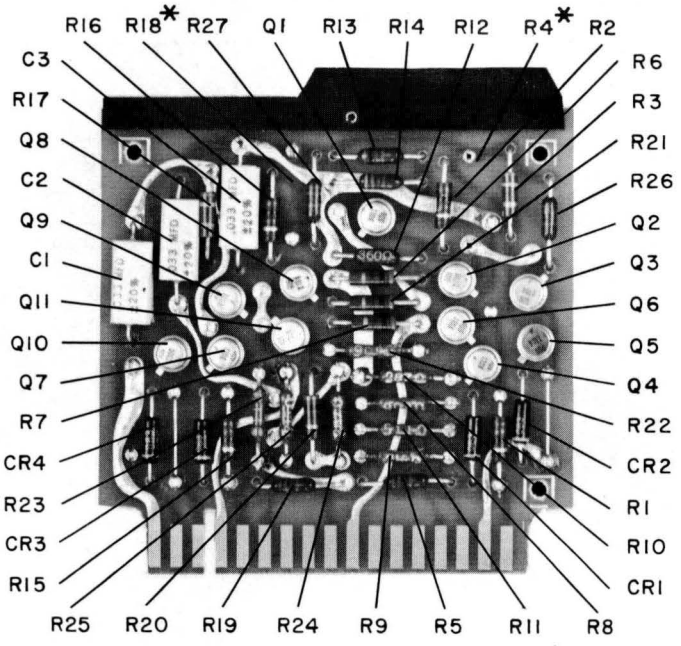
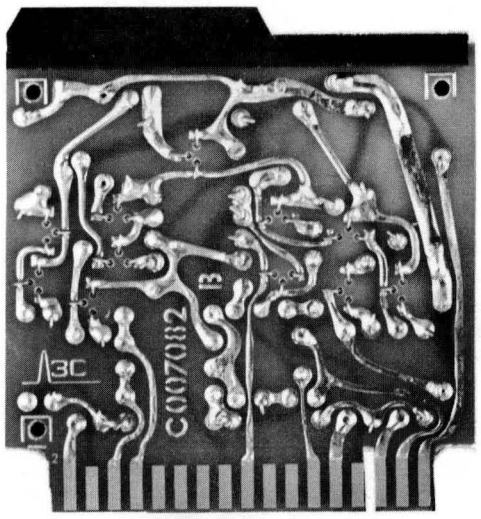


Figure 3-26.1. Schmitt Trigger PAC, Model ST-335, Schematic Diagram and Logic Symbol

Parts Location





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*CUSTOMER OPTION

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1-C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR4	DIODE: Replacement Type 1N914	943 083 001
Q1, Q4-Q7, Q10, Q11	TRANSISTOR	943 722 002
Q2, Q3, Q8, Q9	TRANSISTOR	943 721 002
R1, R15	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/4w	932 007 018
R2, R16	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4w	932 007 025
R3, R17	RESISTOR, FIXED, COMPOSITION: 1.3 K ±5%, 1/4w	932 007 052

Figure 3-26.2. Schmitt Trigger PAC, Model ST-335, Parts Location and Identification (Sheet 1 of 2)

Electrical Parts List (Cont)

Ref. Desig.	Description	3C Part No.
R4, R18	RESISTOR, FIXED, COMPOSITION: (Tailored item)	
R5, R19, R26, R27	RESISTOR, FIXED, FILM: 620 ohms ±2%, 1/4w	932 114 044
R6, R7, R20, R21	RESISTOR, FIXED, COMPOSITION: 1.0 K ±5%, 1/4w	932 007 049
R8, R22	RESISTOR, FIXED, FILM: 909 ohms ±2%, 1/8w	932 113 147
R9, R23	RESISTOR, FIXED, FILM: 715 ohms ±2%, 1/8w	932 113 142
R10, R24	RESISTOR, FIXED, FILM: 287 ohms ±2%, 1/8w	932 113 123
R11, R25	RESISTOR, FIXED, FILM: 511 ohms ±2%, 1/8w	932 113 135
R12	RESISTOR, FIXED, COMPOSITION: 360 ohms ±5%, 1/4w	932 007 038
R13	RESISTOR, FIXED, FILM: 200 ohms ±2%, 1/4w	932 114 032
R14	RESISTOR, FIXED, FILM: 470 ohms ±2%, 1/4w	932 114 041

Figure 3-26.2. Schmitt Trigger PAC, Model ST-335, Parts Location and Identification (Sheet 2 of 2)

APPLICATIONS

Input Level Options. -- Two separate switching levels and sensitivities can be selected for either circuit by making the appropriate pin connections. Switching levels can be varied from +2.5v to -2.5v. Table 3-26.1 gives two standard variations that can be contained with the various input options. Refer to Figure 3-26.3 for the typical ST-335 waveform characteristics.

Table 3-26.1.
Typical Input Variations

Option	Pin Connections		Switching Levels	
	Circuit A	Circuit B	Positive-Moving Input	Negative-Moving Input
1	8 and 3	24 and 30	+2.5v	+1.6v
2	6 and 3	27 and 30	-1.6v	-2.5v

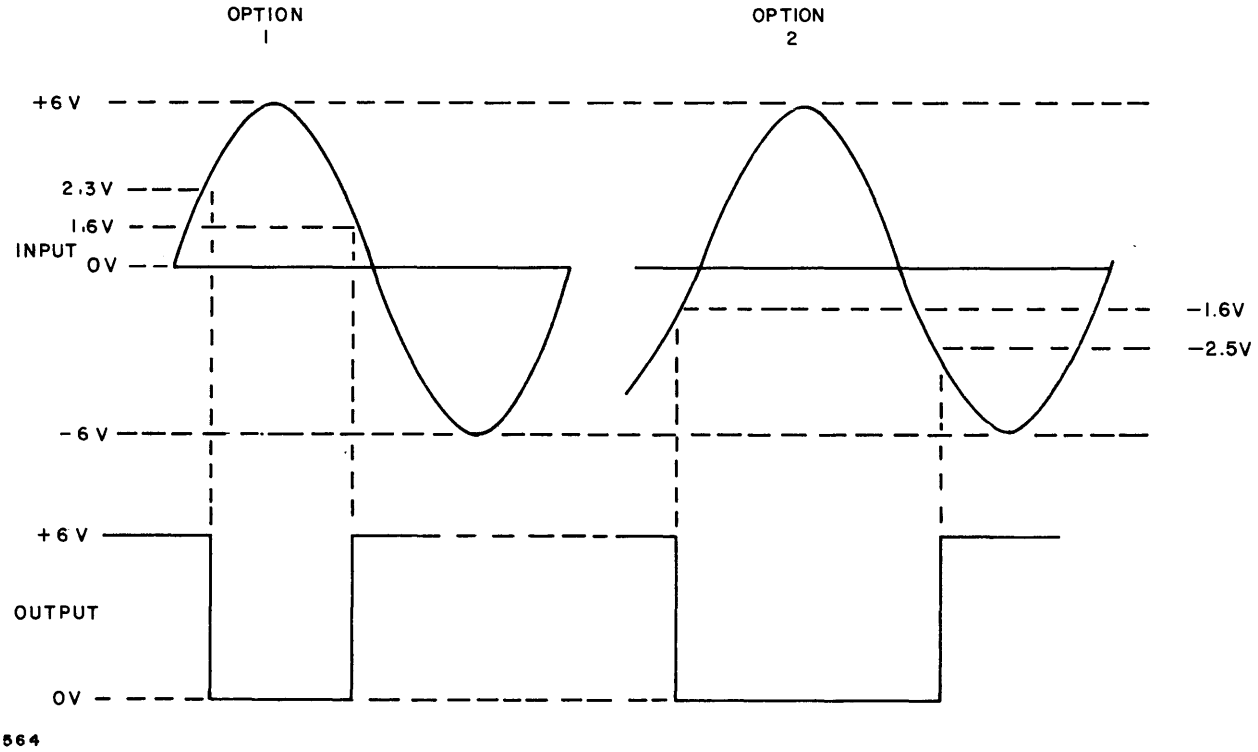


Figure 3-26.3. Schmitt Trigger PAC, Model ST-335, Typical Waveforms

Switching Levels. -- When different switching levels are desired, the following equations will determine the approximate value of resistance which will replace the designated resistors on the PAC. For example, V_1 is the desired switching level for a positive-moving input, and V_2 is the desired switching level for a negative-moving input; if V_2 is positive with respect to ground then,

$$R8' \text{ (in K ohms)} = \frac{V_1 - V_2}{V_2 (0.7 + 0.05 V_2)} , \quad (1)$$

$$R10' \text{ (in K ohms)} = \frac{V_2 R8'}{6 - V_2} , \quad (2)$$

where R8' and R10' will replace R8 and R10 on the PAC, respectively.

If V_2 is negative with respect to ground, then the resistor network (R9 and R11) is used and R9' and R11' are determined from the following equations:

$$R9' \text{ (in K ohms)} = \frac{-(V_1 - V_2)}{V_2 (0.7 + 0.05 V_2)} , \quad (3)$$

$$R11' \text{ (in K ohms)} = \frac{V_2 R9'}{-6 - V_2} . \quad (4)$$

If V_2 is ground, then jumper J1 is removed and replaced by a resistor R_x, and pin 3 is connected to ground (pin 30 for circuit B). The value of resistance for R_x is determined from Equation (5).

$$R_x \text{ (in K ohms)} = \frac{V_1}{4.15} . \quad (5)$$

A graphic presentation of the Equations (1) through (4) is given in Figures 3-26.4 and 3-26.5, Graphs I and II, respectively. The following steps demonstrate proper use of the graphs.

a. To determine the replacement resistor value, use Graph I if V_2 is more positive than 0v, or Graph II if V_2 is more negative than 0v.

b. Select the line radiating from the origin which corresponds to the desired V_2.

c. Among the lines sloping downward from left to right, find the line which corresponds to the desired difference between V_1 and V_2.

d. The coordinates of the intersection of the two lines will give the desired resistor value.

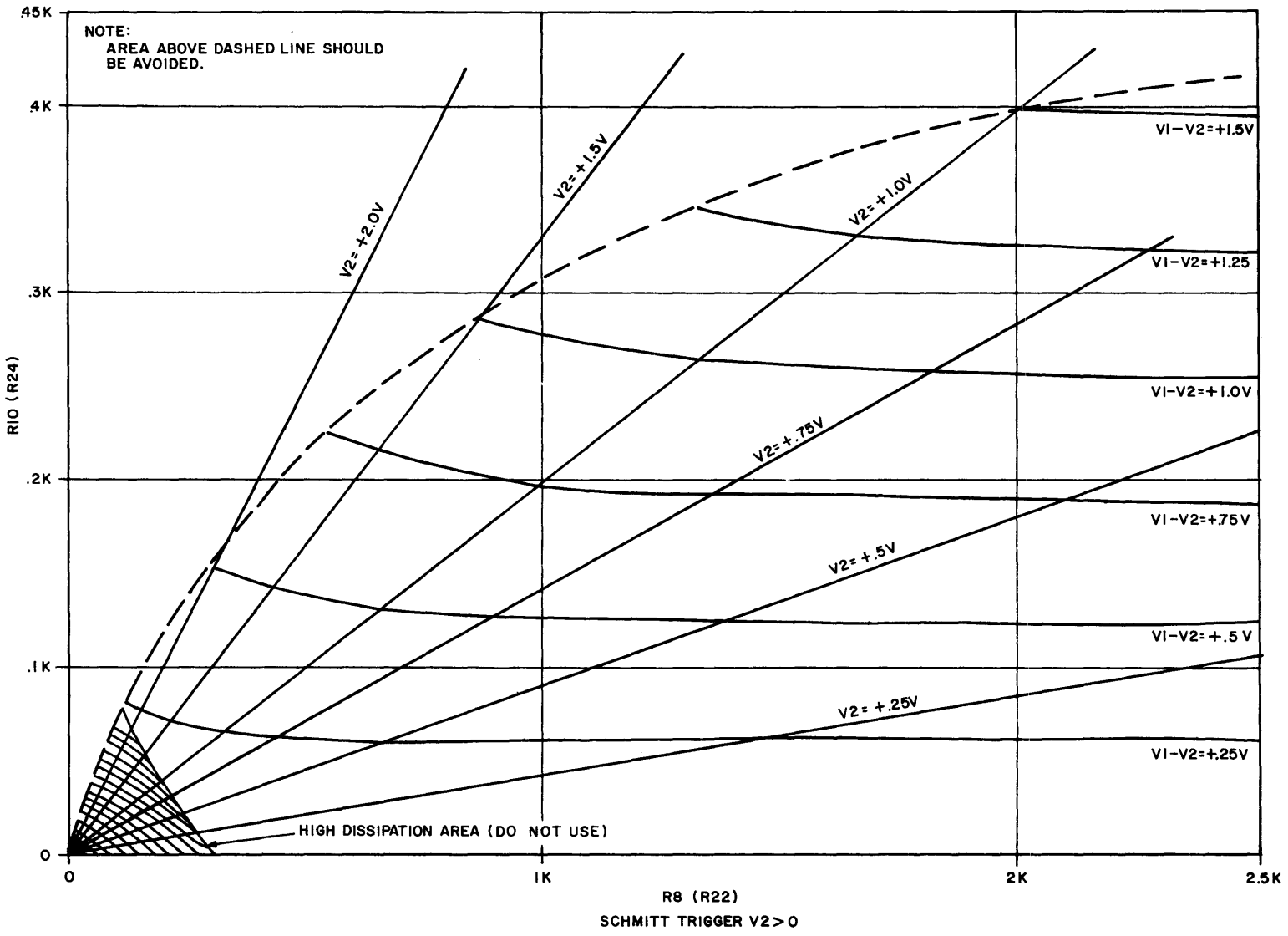


Figure 3-26.4. Schmitt Trigger PAC, Model ST-335, Graph I

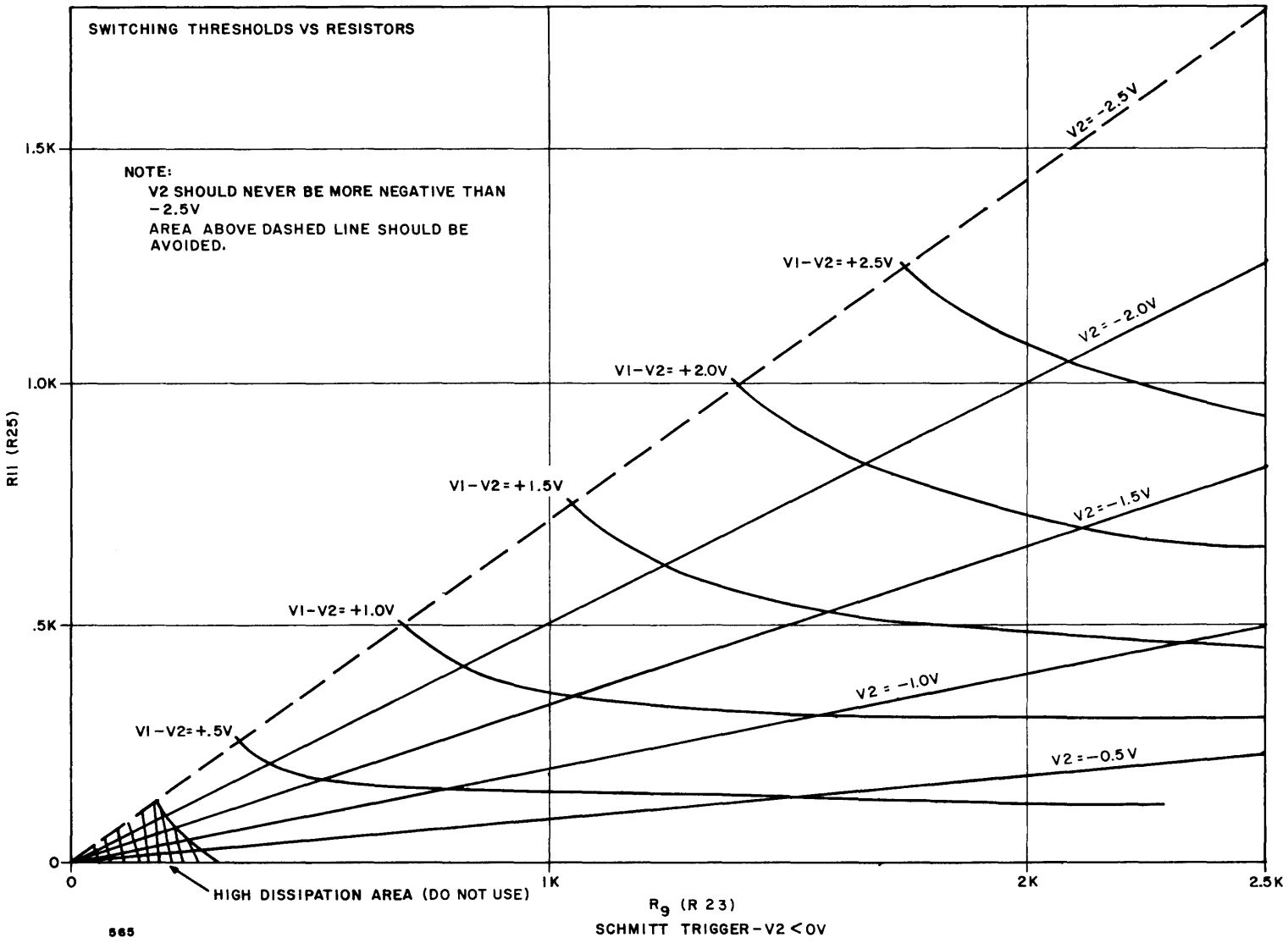


Figure 3-26.5. Schmitt Trigger PAC, Model ST-335, Graph II

e. Linear interpolation and extrapolation is permissible.

For example, given

$$V_2 = -2.5v,$$

$$V_1 = 0v,$$

$$V_1 - V_2 = +2.5v,$$

then, looking at Graph II, the line marked $V_2 = -2.5v$ is the uppermost sloping line radiating from the origin. The uppermost line sloping downward corresponds to $V_1 - V_2 = +2.5v$ and the resulting intersection is at R11 = 1.25 K, and R9 = 1.75 K (R25 = 1.25 K and R23 = 1.75 K for circuit B).

If $V_2 = -2.5v$ and $V_1 = +2.5v$, then $V_1 - V_2 = +5.0v$. The corresponding resistors would be (by linear extrapolation) double those previously found, i.e., R11 = 2.5 K and R9 = 3.5 K.

When the operating voltage (+6v) is reduced to +5v, then Graphs I and II are modified as follows.

(1) The maximum input is now reduced to +5v.

(2) Graph I must be modified by multiplying each labeled value of V_2 by (5/6), and each labeled value of $(V_1 - V_2)$ must be multiplied by (2/3).

(3) Graph II must be modified by multiplying $(V_1 - V_2)$ by (2/3). V_2 remains unchanged.

External Level and Sensitivity Control. -- If Equations (1) through (5) yield unrealistic resistance values (e.g., requiring excessive power dissipation), then an external power supply must be used and jumper J1 is replaced by an appropriate resistor. Using the same definitions for V_1 and V_2, the external supply will be equal to V_2 and the value of resistance replacing J1 is determined from Equation (6).

$$R = \frac{V_1 - V_2}{4.15 + 0.3\ V_2} . \qquad (6)$$

Switching Level Measurement. -- Switching levels may be measured in the following manner.

a. Select and connect the appropriate network (internal or external) to pin 3 (pin 30 for circuit B).

b. Connect a well-filtered dc supply to the input.

c. Set the dc supply to +6v. The output should be 0v.

d. Lower the dc input until the output switches to +6v. This is the dc negative-going switching level, V_1.

e. Raise the dc input until the output switches to 0v. This is the dc positive-going switching level, V_1.

If an accurate threshold is desired, an external supply should be used, and a resistor of the correct value should replace J1. Then an external potentiometer should be used as a fine trim. The switching levels should be measured as above. To determine the switching levels more accurately, they should be measured at the operating frequency of the PAC. If the input signal waveform reveals sharp edges, this condition should be duplicated when setting up the ST-335. Switching levels will not remain constant if the input signal changes frequency. If the frequency varies from dc to 5 mc (sine wave), thresholds will change by 100 mv (typical).

Restrictions upon the switching levels and components determined by calculation are as follows.

a. The maximum switching level for a positive-moving input at the base of the first input transistor is +2.5v.

b. The maximum negative switching level for a negative-moving input at the base of the first input transistor is -2.5v.

c. If the difference between switching levels is 0.2v or less, the equivalent driving signal source impedance should be low to avoid multiple triggering.

d. The maximum dissipation of any resistor used with the ST-335 must not exceed 125 mw. All of these resistors should be a metal film type.

Shifting Input Signal. -- To condition the input signal, a network may be inserted on the standoff terminals provided between the input pin and the base of the first transistor.

The usual network will consist of two resistors to attenuate the input signal. The limits of the signal appearing at the base of the input transistor are +6v and -20v, and resistive attenuators will only be needed if these levels are exceeded. Combinations of resistors and capacitors to provide differentiation and integration can be used. Figure 3-26.6 illustrates the use of the network, R1 and R_x. Standard configuration provides R1 = 50 ohms and $R_x = \infty$ (open circuit).

NOTE

When an input signal is to be attenuated, R_1 and R_x should be chosen to provide suitable attenuation and input impedance.

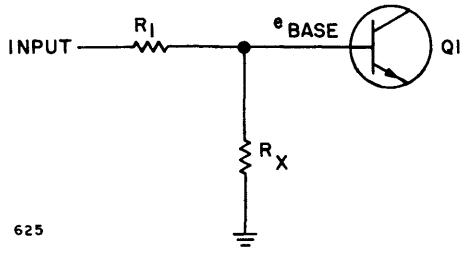


Figure 3-26.6. Schmitt Trigger PAC, Model ST-335, Shifting Input Signal Network

3-26A ADJUSTABLE SCHMITT TRIGGER PAC, MODEL ST-336

The Adjustable Schmitt Trigger PAC, Model ST-336 (Figures 3-26A. 1 and 3-26A. 2), contains two independent trigger circuits, each capable of converting arbitrarily shaped inputs to μ-PAC compatible outputs. The Schmitt trigger is versatile and can be used for such applications as pulse shaping, signal level shifting, level detecting, and level comparing. In addition, each circuit can perform signal attenuation, differentiation and integration by use of external resistor-capacitor networks.

Provisions are made at the input, whereby the input signal may be attenuated before it is applied to the base of the first transistor stage. The attenuating network will be needed only when the input signal exceeds the positive voltage supply of the PAC (+6v) or when the input signal is more negative than -20v.

CIRCUIT FUNCTION

Each circuit has a single input and output. The only amplitude restriction is that the input signal, which appears at the base of the input transistor, must not exceed the positive voltage supply to prevent input clipping. However, the signal may be as low as -20v with no detrimental effect. These input restrictions are independent of the switching levels. The output of each trigger circuit is directly compatible with the μ-PAC product line. Switching levels and sensitivities are selected by variable resistors mounted on the PAC.

NOTE

This PAC occupies two slots in a solderless-wrap BLOC and one slot in a taper-pin BLOC.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Output Drive Capability

8 unit loads and 40 pf stray capacitance each

Circuit Delay

20 nsec (typ)

Input Signal at Base of Input Transistor

+6v (max positive)

-20v (max negative)

Sensitivity

100 mv max
1 volt min

Current Requirements

+6v: 90 ma (max)

-6v: 60 ma (max)

Switching Level Range

+2. 5v to -2. 5v

Variation of Switching Levels Over Temperature

50 mv (max)

Power Dissipation

0. 90w (max)

Handle Color Code

Orange

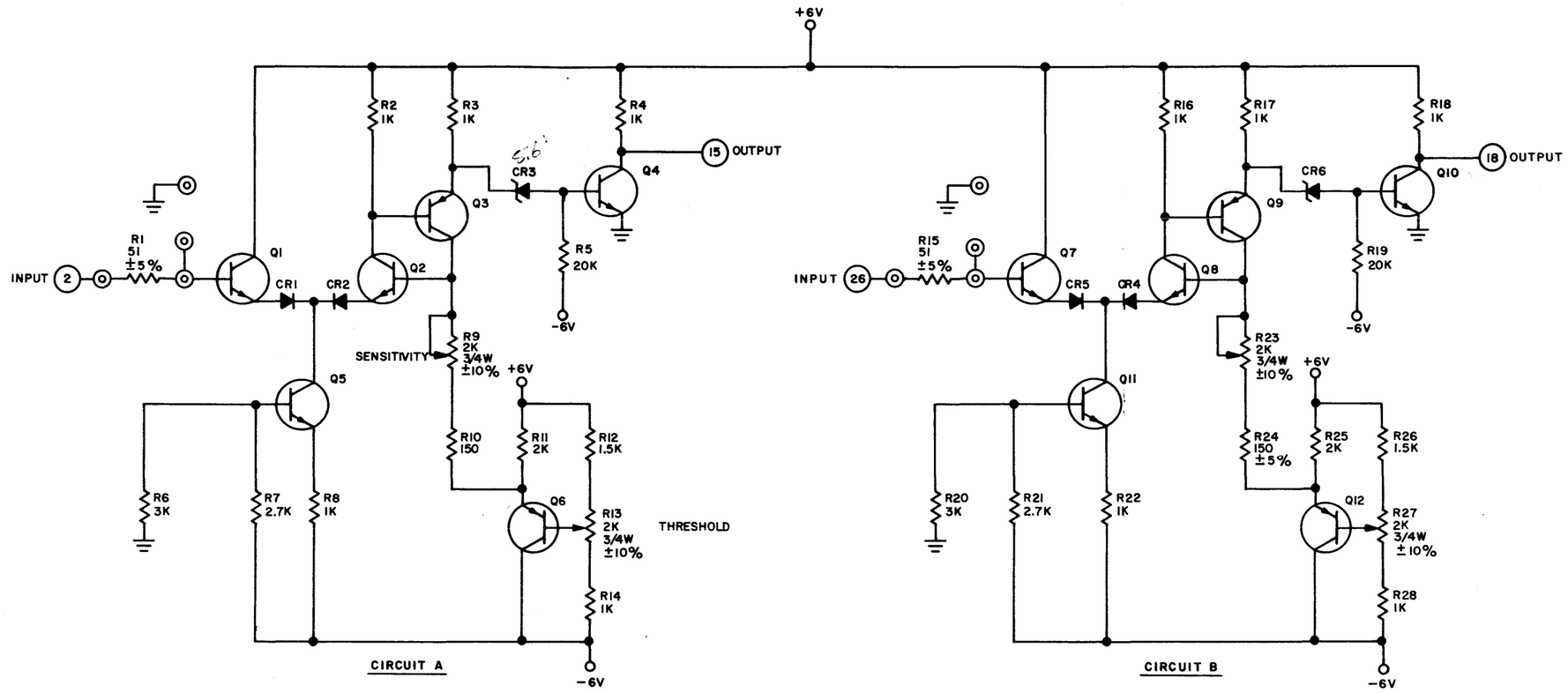
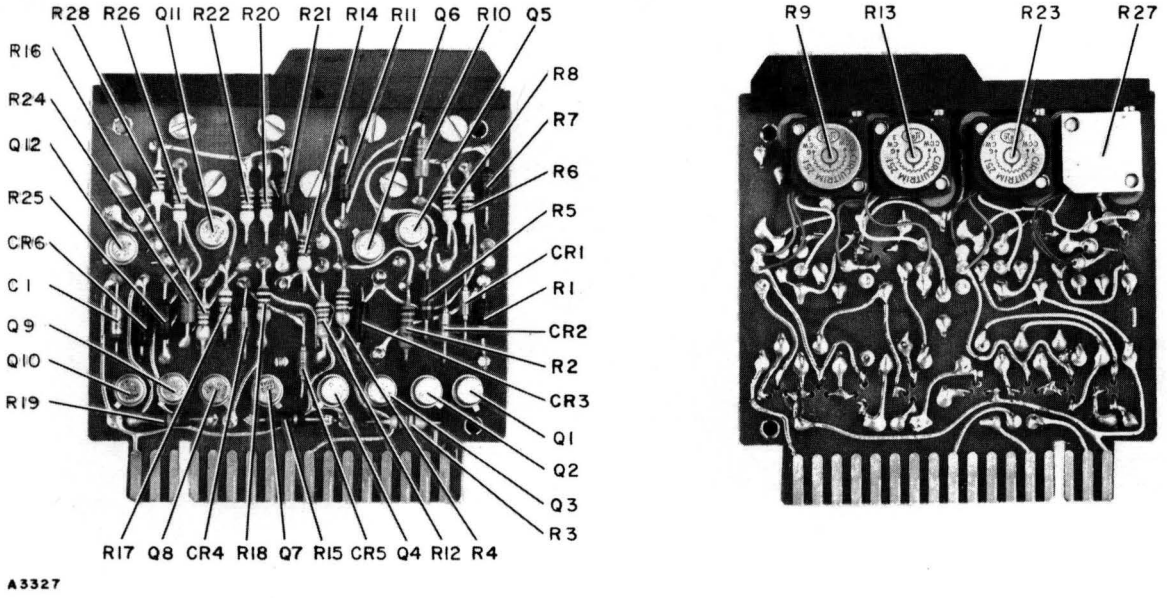


Figure 3-26A.1. Adjustable Schmitt Trigger PAC, Model ST-336, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC: 0.1 μf ±20%, 35v	930 227 003
CR1, CR2, CR4, CR5	DIODE: Replacement Type 1N914	943 083 001
CR3, CR6,	DIODE: Replacement Type 1N708A	943 102 015
Q1, Q2, Q4, Q5, Q7, Q8, Q10, Q11	TRANSISTOR: Replacement Type 2N3011	943 722 002
Q3, Q6, Q9, Q12	TRANSISTOR: Replacement Type 2N3012	943 721 002
R1, R15	RESISTOR, FIXED, COMPOSITION: 51 ohms ±5%, 1/4w	932 007 018
R2-R4, R8, R14, R16-R18, R22, R28	RESISTOR, FIXED, FILM: 1K ±2%, 1/4w	932 114 049
R5, R19	RESISTOR, FIXED, FILM: 20K ±2%, 1/4w	932 114 080
R6, R20	RESISTOR, FIXED, FILM: 3K ±2%, 1/4w	932 114 060
R7, R21	RESISTOR, FIXED, FILM: 2.7K ±2%, 1/4w	932 114 059
R9, R13, R23, R27	RESISTOR, VARIABLE, FILM: 2K ±10%, 3/4w	933 300 105
R10, R24	RESISTOR, FIXED, FILM: 150 ohms ±2%, 1/4w	932 114 029
R11, R25	RESISTOR, FIXED, FILM: 2K ±2%, 1/4w	932 114 056
R12, R26	RESISTOR, FIXED, FILM: 1.5K ±2%, 1/4w	932 114 053

Figure 3-26A.2. Adjustable Schmitt Trigger PAC, Model ST-336, Parts Location and Identification

APPLICATIONS

Input Level Options. -- The switching levels and sensitivities can be selected for either circuit by making the appropriate potentiometer adjustments. Switching levels can be varied from +2.5v to -2.5v. Refer to Figure 3-26A.3 for the typical ST-336 waveform characteristics.

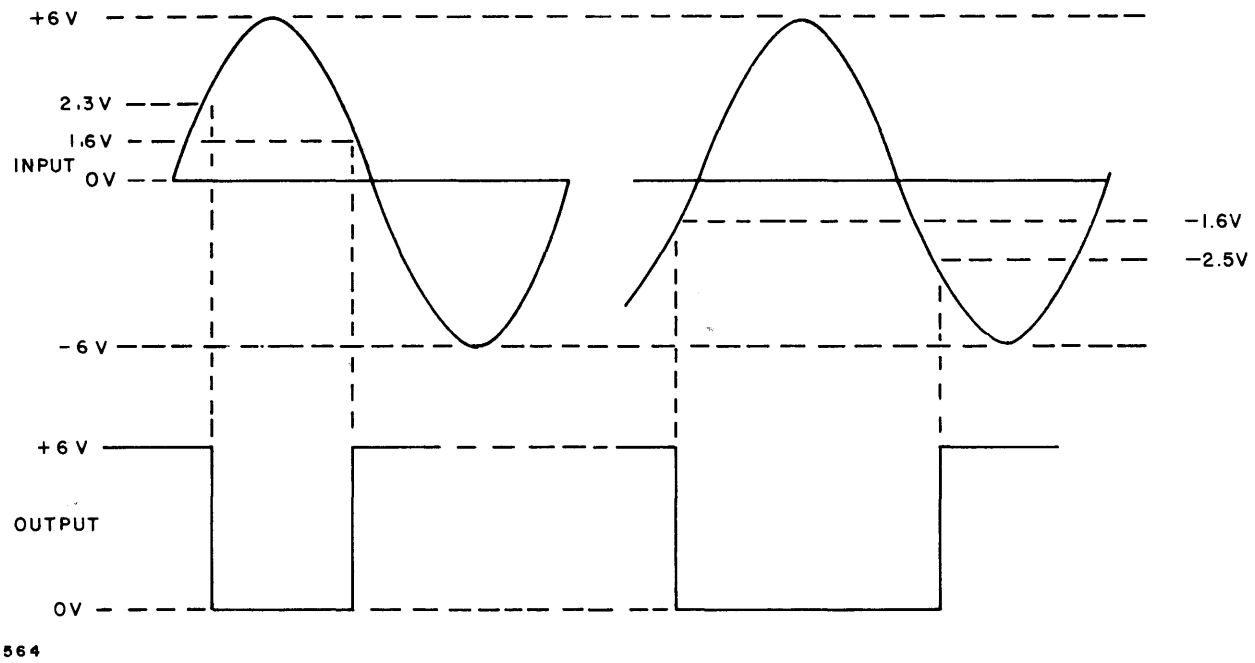


Figure 3-26A.3. Adjustable Schmitt Trigger PAC, Model ST-336, Typical Waveforms

Switching Level Measurement. -- Switching levels may be measured in the following manner.

a. Connect a well-filtered dc supply to the input.

b. Set the dc supply to +6v. The output should be 0v.

c. Lower the dc input until the output switches to +6v. This is the dc negative-going switching level.

d. Raise the dc input until the output switches to 0v. This is the dc positive-going switching level.

e. The voltage difference between the switching levels noted in steps c. and d. is the sensitivity.

To determine the switching levels more accurately, they should be measured at the operating frequency of the PAC. If the input signal waveform reveals sharp edges, this condition should be duplicated when setting up the ST-336. Switching levels will not remain constant if the input signal changes frequency. If the frequency varies from dc to 5 mc (sine wave), thresholds will change by 100 mv (typical).

Restrictions upon the switching levels are as follows.

a. The maximum switching level for a positive-moving input at the base of the first input transistor is +2.5v.

b. The maximum negative switching level for a negative-moving input at the base of the first input transistor is -2.5v.

c. If the difference between switching levels is 0.2v or less, the equivalent driving signal source impedance should be low to avoid multiple triggering.

Shifting Input Signal. -- To condition the input signal, a network may be inserted on the standoff terminals provided between the input pin and the base of the first transistor.

The usual network will consist of two resistors to attenuate the input signal. The limits of the signal appearing at the base of the input transistor are +6v and -20v, and resistive attenuators will only be needed if these levels are exceeded. Combinations of resistors and capacitors to provide differentiation and integration can be used. Figure 3-26A.4 illustrates the use of the network, R_1 and R_x. Standard configuration provides R_1 = 50 ohms and R_x = ∞ (open circuit).

NOTE

When an input signal is to be attenuated, R_1 and R_x should be chosen to provide suitable attenuation and input impedance.

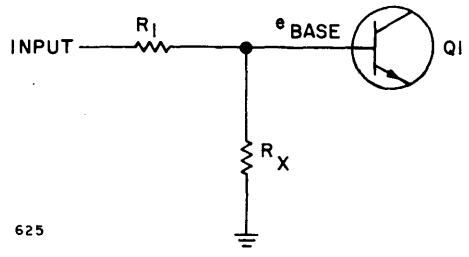


Figure 3-26A.4. Adjustable Schmitt Trigger PAC, Model ST-336, Shifting Input Signal Network

3-27 TRANSFER GATE PAC, MODEL TG-335

The Transfer Gate PAC, Model TG-335 (Figures 3-27.1 and 3-27.2), contains four independent functional gate structures. Two of the structures have four 2-input NAND gates, one input on each gate being common to the four gates. The remaining two structures have three 2-input NAND gates, one input being common to the three gates. (See Figure 3-27.3.)

The PAC can be used for the common transfer control of up to 14 data signals, the data when transferred is inverted in polarity.

INPUT AND OUTPUT SIGNALS

Common Input. -- This input acts as a control or strobe input to each gate in the structure. The signal is active when at logic ONE.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

Input:	1 unit load each
Common input:	3 or 4 unit loads (equal to the number of gates in the structure)

Output Drive Capability

8 unit loads

Circuit Delay

(Measured at +1.5v, averaged over two stages)

30 nsec (max)

Current Requirements

+6v: 155 ma (max)

Power Dissipation

0.95w (max)

Handle Color Code

Red

APPLICATIONS

Each gate structure can be used for the common transfer control of three or four signals (Figure 3-27.4). A separate line is provided for each output signal. The gates may be used separately as inverters when the common inputs are disconnected.

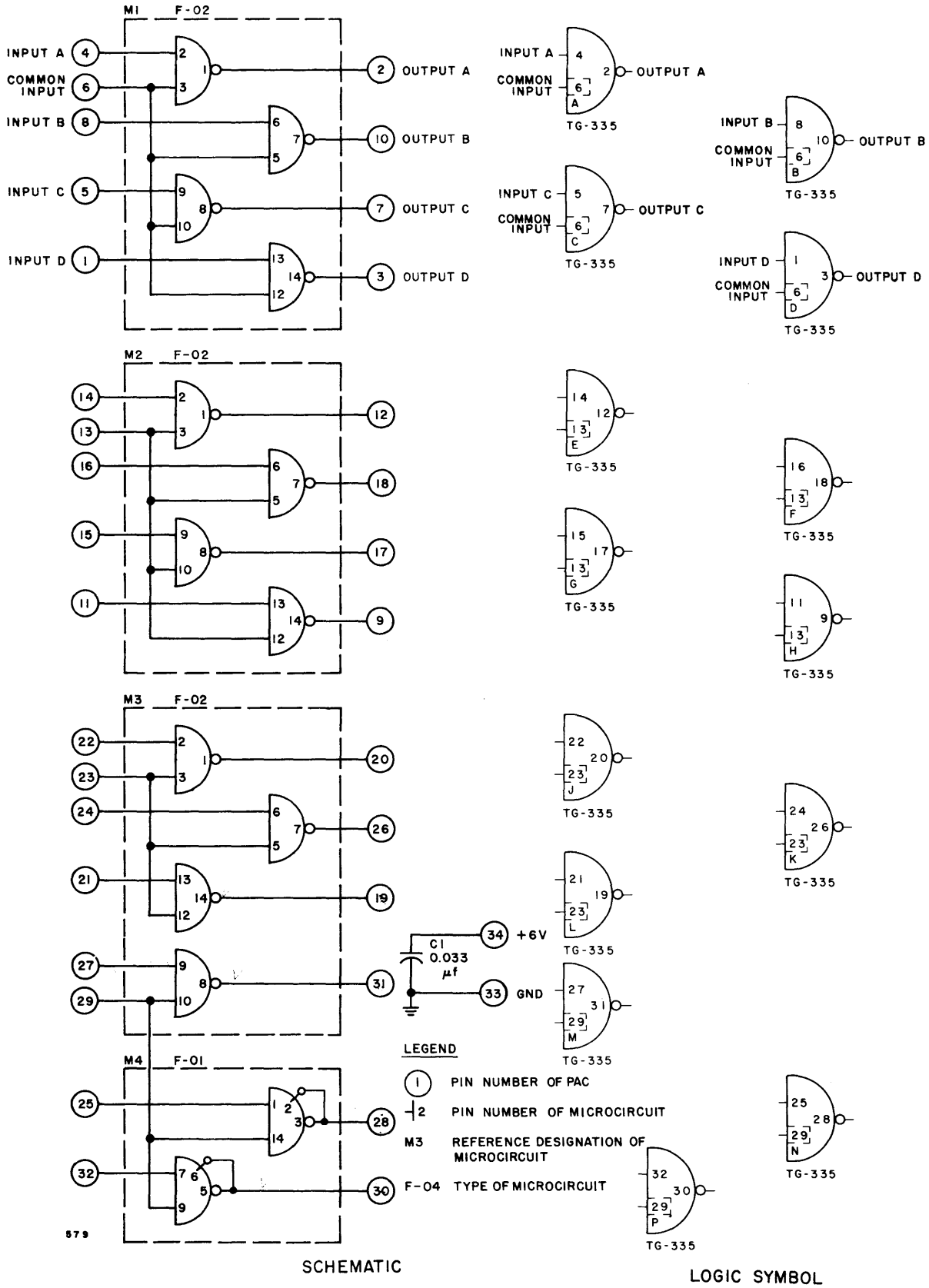
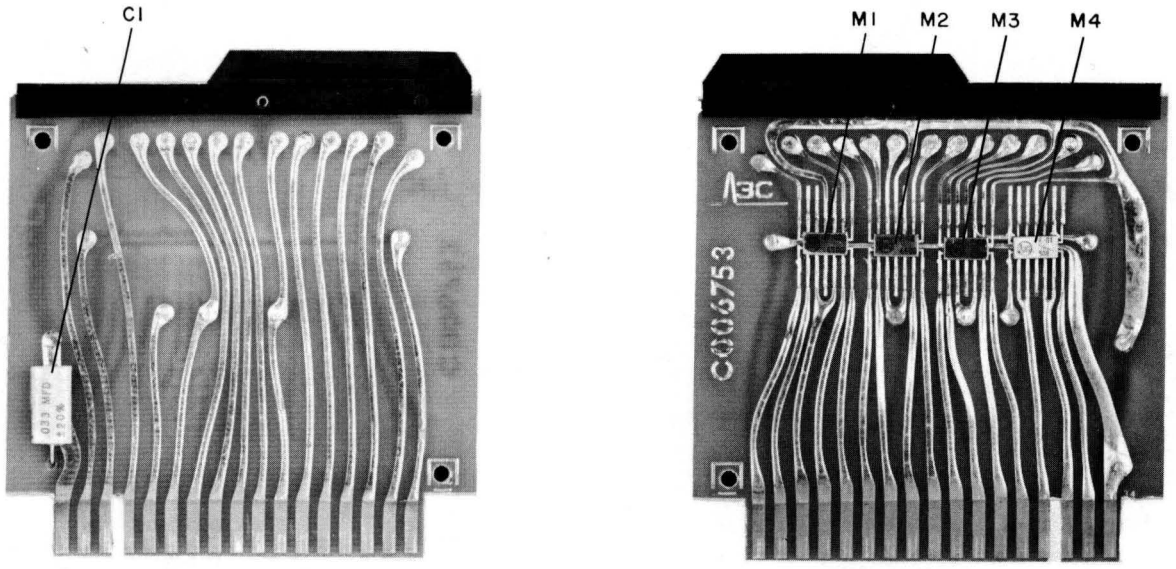


Figure 3-27. 1. Transfer Gate PAC, Model TG-335, Schematic Diagram and Logic Symbol

Parts Location



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Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M4	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Figure 3-27.2. Transfer Gate PAC, Model TG-335, Parts Location and Identification

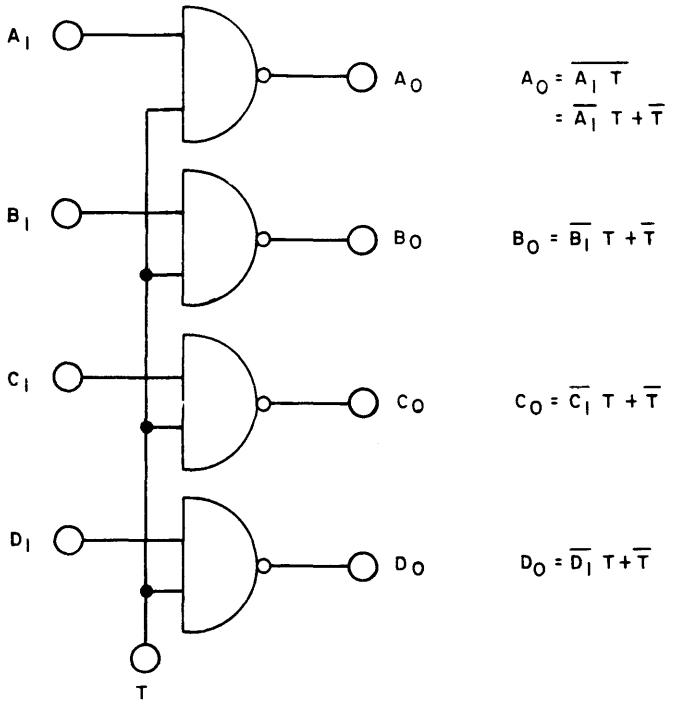


Figure 3-27.3. Transfer Gate PAC, Model TG-335, Gate Structure Logic

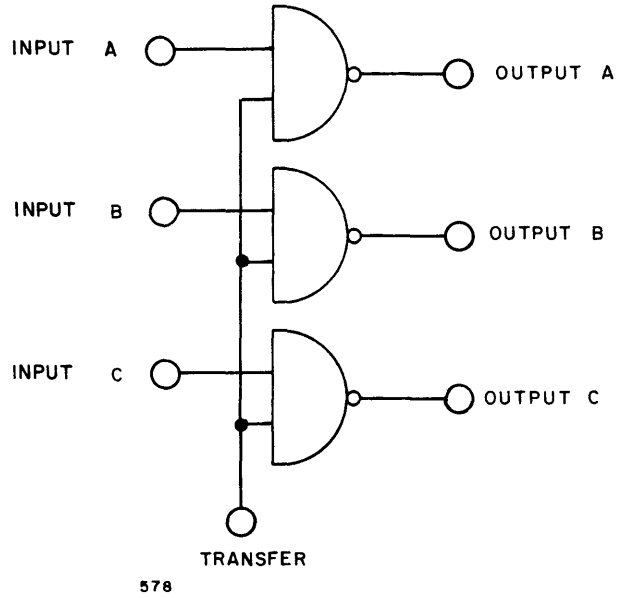


Figure 3-27.4. Transfer Gate PAC, Model TG-335, Controlling Transfer of Three Signals

3-27A TEST POINT PAC, MODEL TP-330

The Test Point PAC, Model TP-330 (Figure 3-27A.1), contains 34 test points, each of which is prewired to a connector terminal. Each test point is identified with the terminal number to which it is connected.

The TP-330 is 2-3/8 inches longer than the standard μ-PAC card. This additional length allows easy access to the test points. A standard μ-PAC handle is provided for PAC identification and ease of extraction.

APPLICATIONS

The TP-330 is intended for use in a given system to facilitate the observation of waveform characteristics. The PAC can be mounted in a prewired plug-in connector of a μ-BLOC.

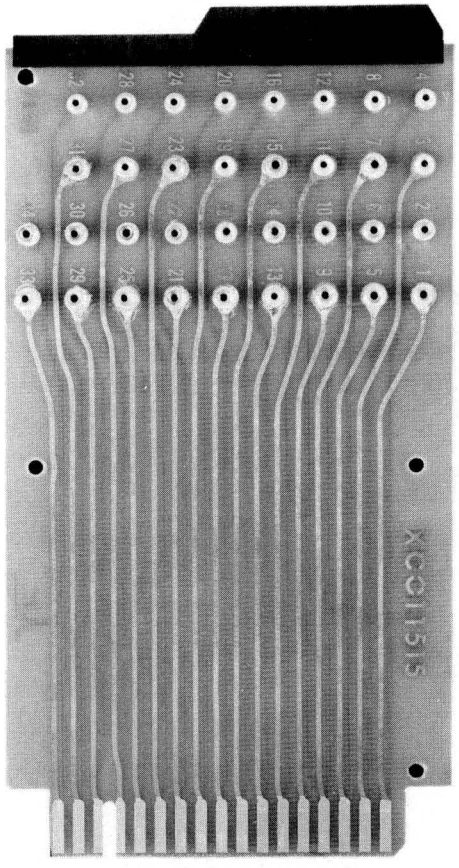


Figure 3-27A.1. Test Point PAC, Model TP-330

3-28 UNIVERSAL FLIP-FLOP PAC, MODEL UF-335

The Universal Flip-Flop PAC, Model UF-335 (Figures 3-28. 1 and 3-28. 2), contains three versatile, independent flip-flops which can perform the functions of storage, counting, shifting, and control. Each flip-flop circuit has a comprehensive input structure which allows control of the flip-flop from a variety of level and pulse inputs. Each stage has two dc set and two dc reset inputs, set control and reset control inputs, a clock input, and set and reset outputs. There is also a common reset input for clearing all stages simultaneously.

A detailed description of the flip-flop circuit is given in Section II.

INPUT AND OUTPUT SIGNALS

DC Set and DC Reset.--A signal at logic ZERO for 80 nsec or longer on any dc set or reset input will set or reset the flip-flop, respectively.

Common Reset.-- A signal at logic ZERO for 80 nsec or longer on the common reset input clears the three stages simultaneously.

Set Control and Reset Control. -- Logic ONE (+6v) is the enabling level on the control inputs. Refer to Section II for complete information on flip-flop operation.

Clock. -- The flip-flop can change state on the negative (ONE to ZERO) transition on the clock input.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

DC inputs:	2/3 unit load each
Control inputs:	1 unit load each
Clock input:	1 unit load each
Common input:	1 unit load each
Common reset:	2 unit loads

Output Drive Capability

8 unit loads

Circuit Delay

Clock input to set or reset output:
60 nsec (max)

DC set input to set output, or dc reset input to reset output:
80 nsec (max)

DC set input to reset output, or dc reset input to set output:
60 nsec (max)

Current Requirements

+6v: 75 ma (max)

Power Dissipation

0. 45w (max)

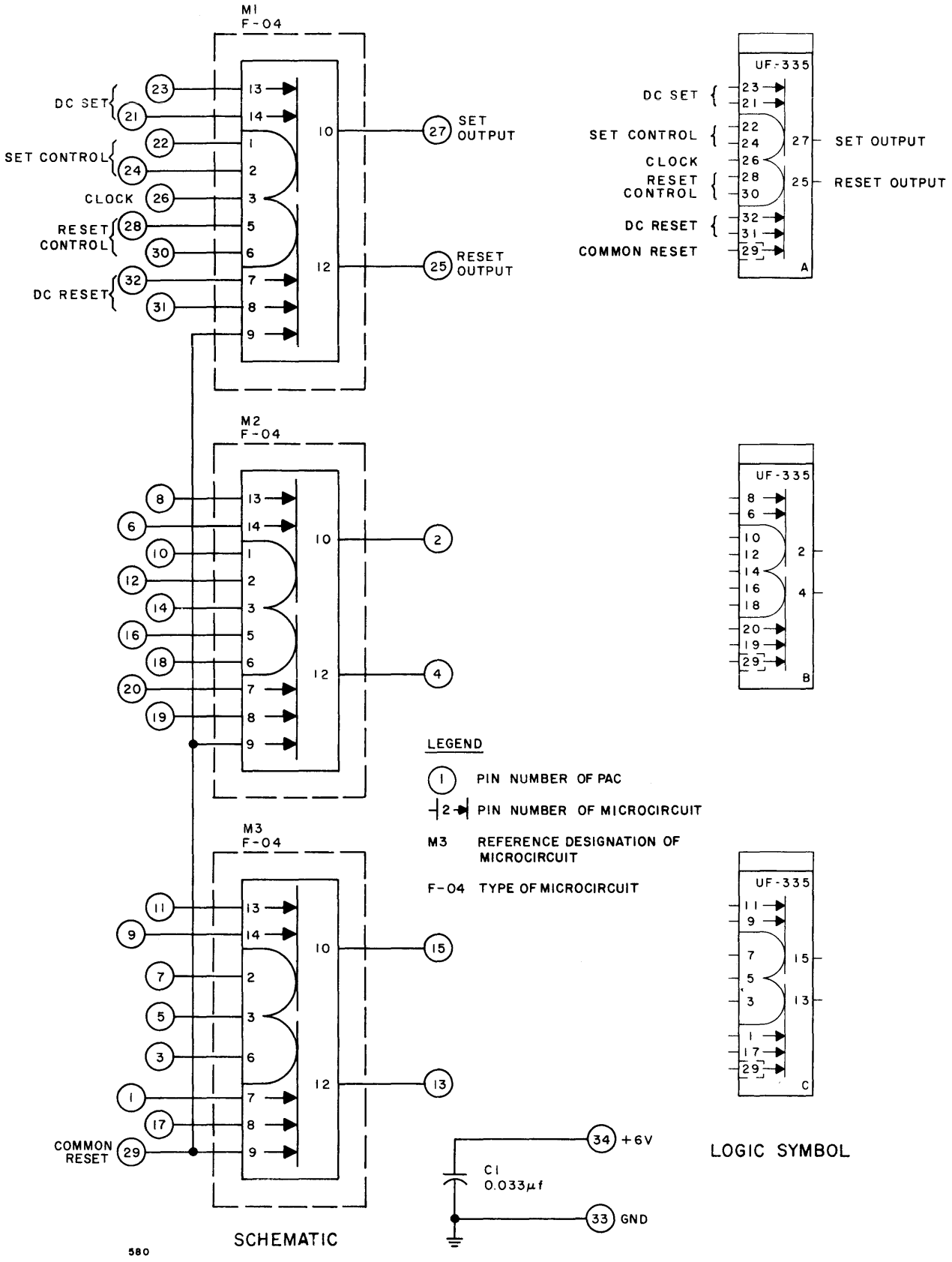
Handle Color Code

Blue

APPLICATIONS

The UF-335 PAC can be used as a counter (Figures 3-28. 3 and 3-28. 4) or as a shift register (Figure 3-28. 5). The method of parallel information drop-in is illustrated in Figure 3-28. 6.

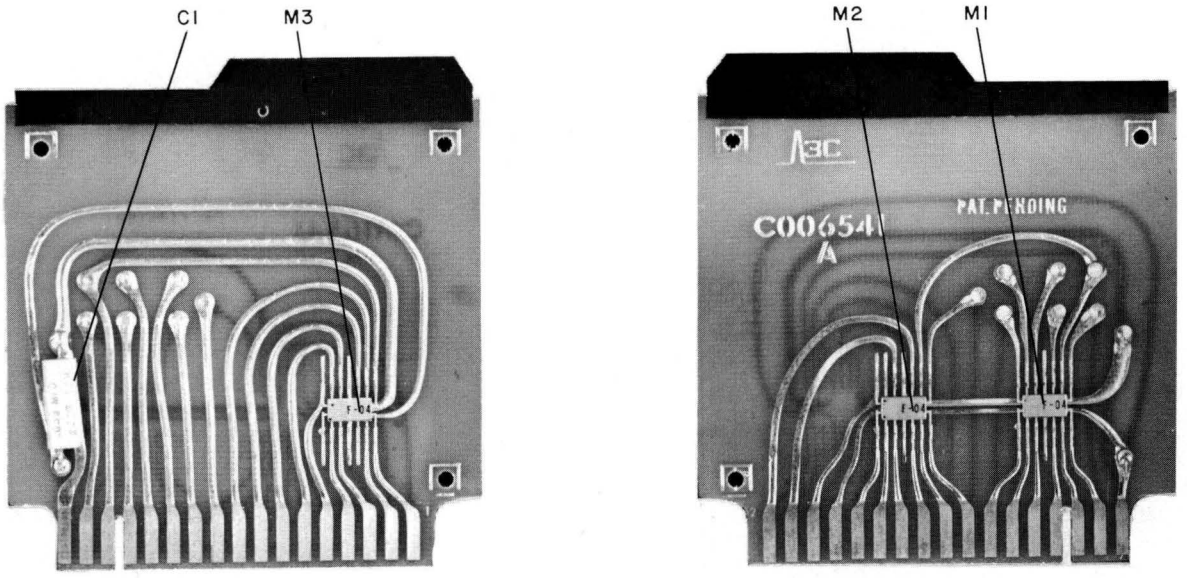
Data may be transferred to the flip-flop with single-ended signals by first resetting all stages, then setting only the appropriate ones. With double-ended data transfer, complementary signals are applied to the dc set and dc reset inputs for putting the flip-flop in the appropriate state in one operation.



Note: Refer to Figure 3-28.1A for PACs with Ser. No. 825 and beyond.

Figure 3-28.1. Universal Flip-Flop PAC, Model UF-335, Schematic Diagram and Logic Symbol

Parts Location



540

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M3	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016

Note: Refer to Figure 3-28.2A for PACs with Ser. No. 825 and beyond.

Figure 3-28.2. Universal Flip-Flop PAC, Model UF-335, Parts Location and Identification

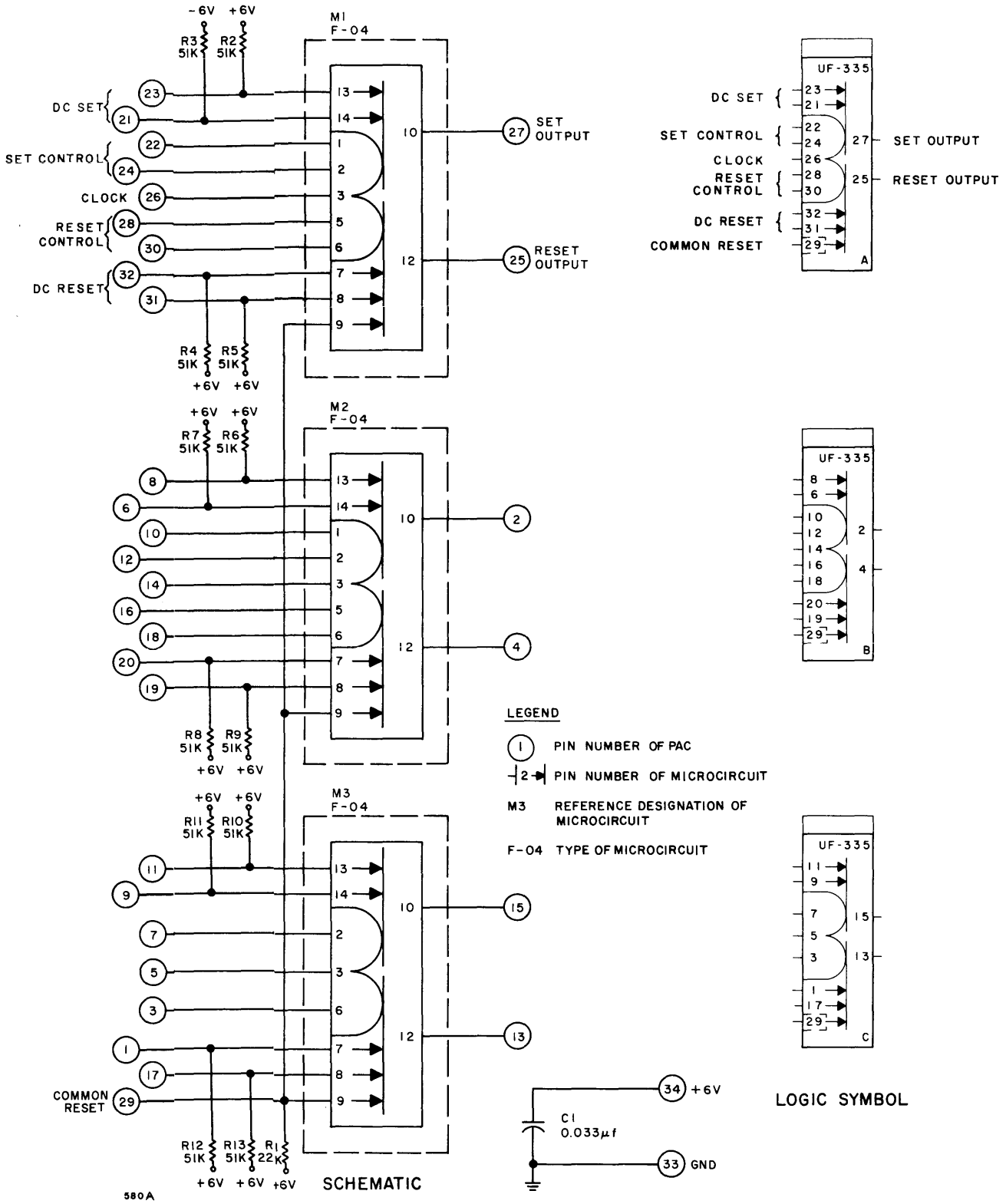
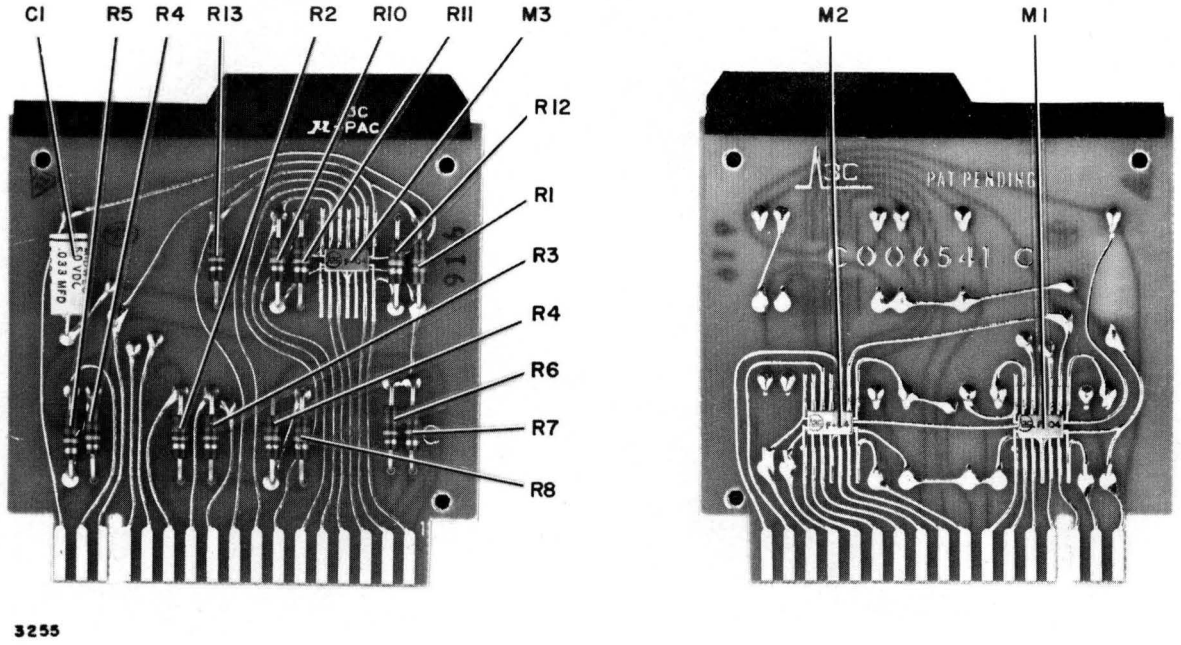


Figure 3-28.1A. Universal Flip-Flop PAC, Model UF-335 (Ser. No. 825 and beyond), Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-04, flip- flop integrated circuit	950 100 044
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf, ±20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22 K ±5%, 1/4w	932 007 081
R2-R13	RESISTOR, FIXED, COMPOSITION: 51 K ±5%, 1/4w	932 007 090

Figure 3-28.2A. Universal Flip-Flop PAC, Model UF-335 (Ser. No. 825 and beyond), Parts Location and Identification

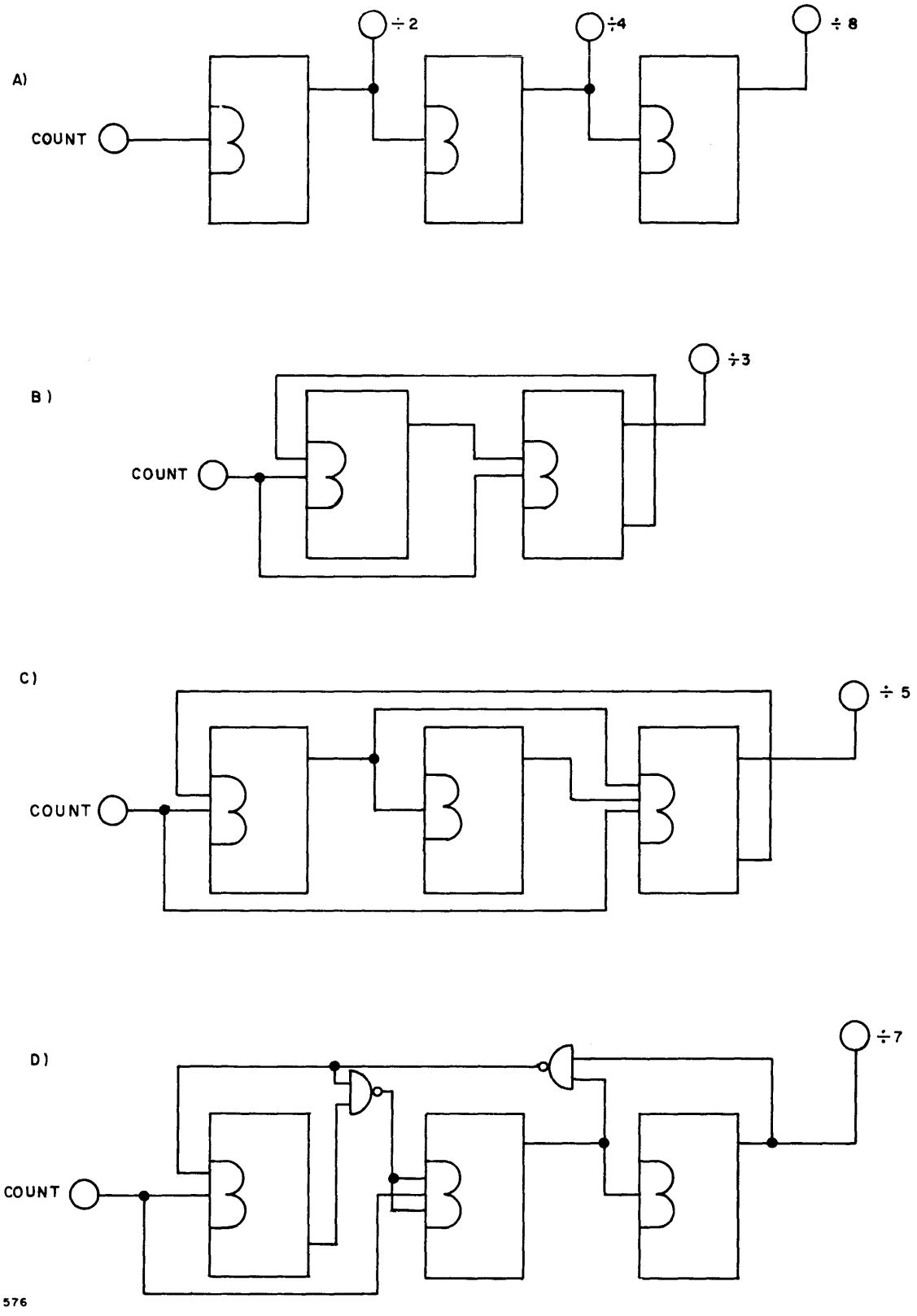


Figure 3-28.3. Universal Flip-Flop PAC, Model UF-335, Counter Operation

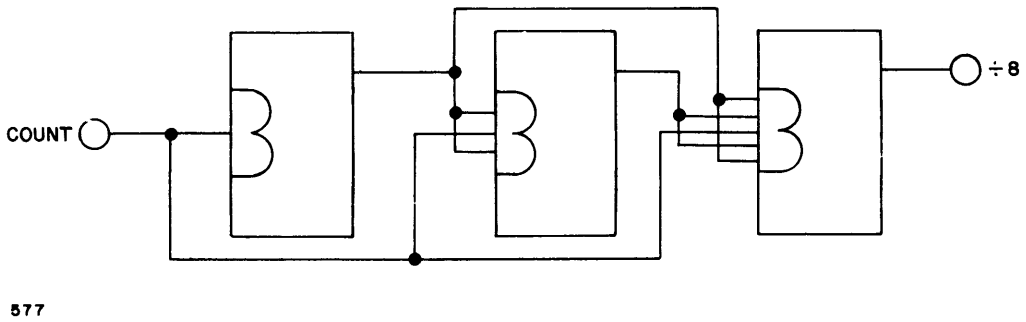


Figure 3-28.4. Universal Flip-Flop PAC, Model UF-335, Three-Stage Instantaneous Carry Operation

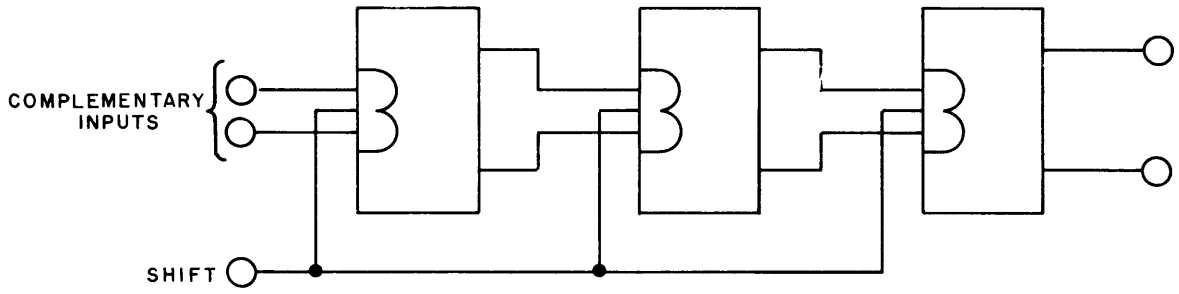


Figure 3-28.5. Universal Flip-Flop PAC, Model UF-335, Shift Register Operation

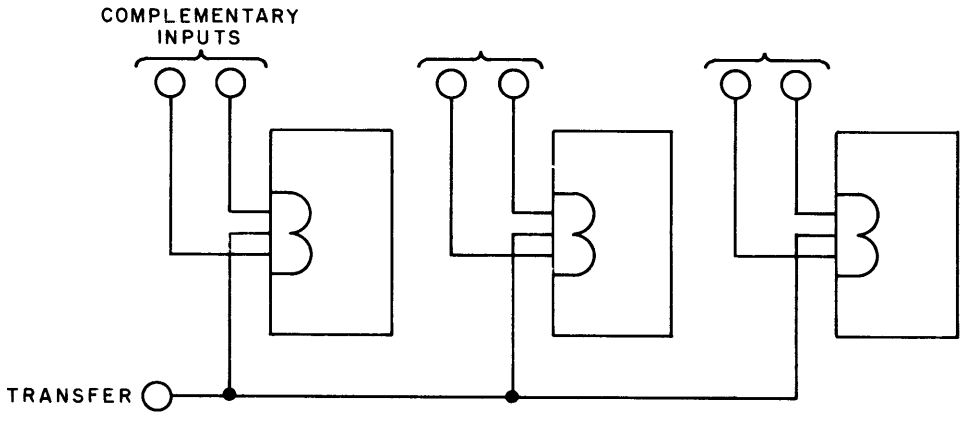


Figure 3-28.6. Universal Flip-Flop PAC, Model UF-335, Parallel Information Drop-In

3-28A TRANSISTORIZED UNIT INDICATOR, MODEL UI-110

The Transistorized Unit Indicator, Model UI-110 (Figure 3-28A.1), is a low power visual indicator that monitors positive voltage logic levels such as in the μ-PAC and Silicon S-PAC lines. The UI-110 contains a transistorized neon indicator circuit. When a ONE (+6v) is applied to the input circuit, the neon indicator ignites. The UI-110 is powered from a +90-v supply, and is driven by standard μ-PAC or Silicon S-PAC logic signals.

Each standard UI-110 is equipped with a clear plastic lens and taper-pin connections. The UI-110 has provision for driving an external indicator.

The UI-110 mounts in a 3/8-in. hole, 5/8 in. on center, and projects 1-15/16 in. maximum behind the panel.

CIRCUIT FUNCTION

During normal operation, the transistor is biased to cutoff. Application of a +6-v level permits the transistor to light the indicator lamp.

Input logic levels are applied either to pin 2 or pin 3 of the UI-110 connector. The internal 68K resistor between pin 3 and the base of the transistor provides effective circuit isolation between the UI-110 and the driving source. Pin 2 is provided for the application of dynamic assertion signals to the indicators.

CAUTION

Do not apply power to a UI-110 unit unless pin 2 is connected to an appropriate input signal or ground.

SPECIFICATIONS

Frequency of Operation

DC to 50 kc

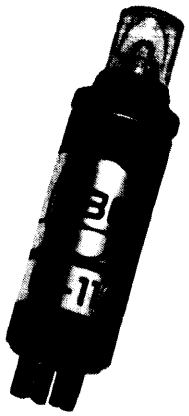
Input Loading

1 unit load each

Input Voltage Margins

		Indicator ON	Indicator OFF
Pin 2	Voltage:	+0.8v to +1.5v	+0.4v to -5.0v
	Current:	0.1 ma to 1.0 ma	0 ma
Pin 3	Voltage:	+3.5v to +20v	+1.6v to -5.0v
	Current:	0.2 ma to 1.0 ma	0 ma

Current Requirements	Power Dissipation
+90v: 2.3 ma with remote lamp	162 mw
1.8 ma without remote lamp	



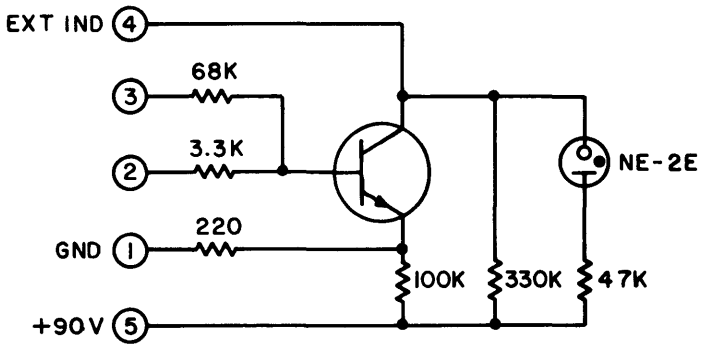


Figure 3-28A.1. Transistorized Unit Indicator, Model UI-110

3-28B TRANSISTORIZED UNIT INDICATOR, MODEL UI-330

The Transistorized Unit Indicator, Model UI-330 (Figure 3-28B.1), is a low power visual indicator that monitors μ-PAC logic levels. The UI-330 contains a neon indicator and a transistor blocking oscillator circuit that functions as a high-voltage ac generator. When a ONE (+6v) is applied to the input circuit, the oscillator ignites the neon indicator. The UI-330 is powered from the +6-v line of any μ-PAC power supply, and is driven by standard μ-PAC logic signals.

Each standard UI-330 is equipped with a clear plastic lens and taper-pin connections. However, colored plastic lenses and solder-pin connections are available by special order.

The UI-330 mounts in a 3/8-in. hole, 5/8 in. on center, and projects 2-1/8 in. maximum behind the panel.

CIRCUIT FUNCTION

During normal operation, the blocking oscillator is biased to cutoff. Application of a +6-v level permits the blocking oscillator to generate a large ac voltage through the secondary winding of the transformer to light the indicator lamp.

Input logic levels are applied either to pin 2 or pin 3 of the UI-330 connector. The internal 10K ohm resistor between pin 3 and the base of the blocking oscillator provides effective circuit isolation between the UI-330 and the driving source. Pin 2 is a direct connection to the base of the blocking oscillator, and provides a connection for a 10K ohm base current-limiting resistor located at the output terminals of the driving source. This arrangement isolates any circuit wiring capacitance.

NOTE

If pin 2 is used, a 10K ohm resistor must be connected in series with the driver.

SPECIFICATIONS

Frequency of Operation

DC to 50 kc

Input Loading

1 unit load each

Current Requirements

+6v: 20 ma (max)

Input Voltage Margins

Neon ON: +5v to +10v

Neon OFF: +1.5v to -3v

Power Dissipation

180 mw

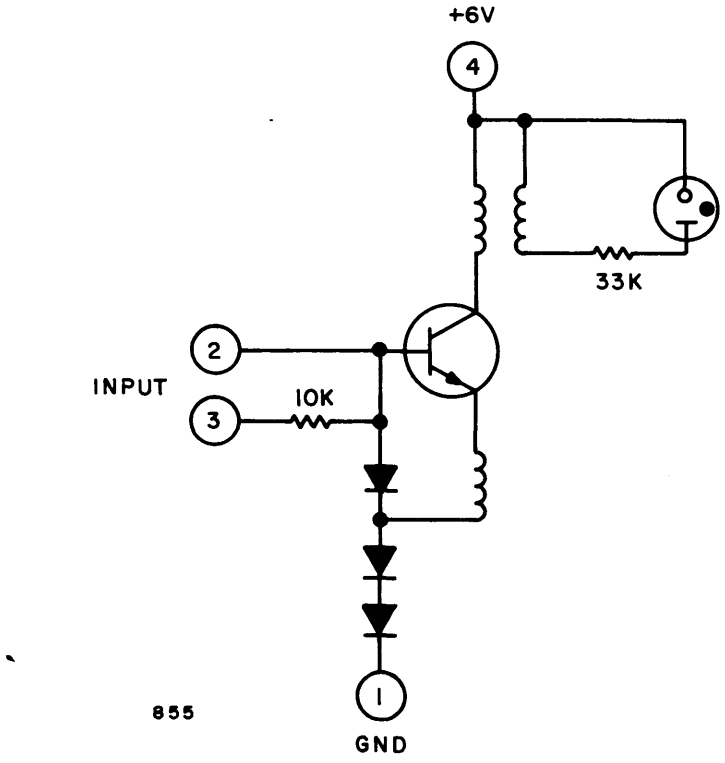


Figure 3-28B.1. Transistorized Unit Indicator, Model UI-330

3-29 TRANSMISSION LINE DRIVER PAC, MODEL XD-335

The Transmission Line Driver PAC, Model XD-335 (Figures 3-29. 1 and 3-29. 2), contains six identical circuits which drive standard 50-ohm, 75-ohm, and 93-ohm coaxial cables, or twisted-pair cables at up to 5-mc repetition rates. The transmission line termination should be a high impedance. A standard NAND gate is recommended.

The design principle is such that there is a small amount of current in the PAC, only one unit load of static current (1. 6 ma) on the line, one-half the amount of transient current (50 ma max) as with normal terminating methods, no terminating resistor at the receiver end, and a 5-v signal at the end of the line. Since the line is lightly loaded, only small currents are incident on the receiver, thereby simplifying the grounding techniques at the receiver. The outputs of the driver are short-circuit protected.

CIRCUIT FUNCTION

Each driver circuit, which performs a NAND function, contains a 2-input power amplifier microcircuit. Of the two output pins which are provided with each circuit, one is connected through a 62-ohm resistor. Standoff terminals are provided with the other output pin for mounting a resistor when a transmission impedance other than 62 ohms is used. The standoff terminals are spaced to accept an Allen Bradley 1/4-w, 5 percent resistor.

In addition, each circuit has a ground pin adjacent to the output terminals for the signal return from the transmission line.

The principle of operation of the XD-335 is to match the transmission line characteristic impedance at the driver end and open-circuit the receiving end. A 2.5-v signal sent down the line results in a 5-v signal at the receiving end due to the +1 reflection coefficient. The reflected 2.5-v signal travels back to the driver and is completely absorbed in the termination at the driver with no multiple reflections. (Refer to Figures 3-29. 3 and 3-29. 4.)

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

2 unit loads each

Output Drive Capability

50-ohm, 75-ohm, or 93-ohm coaxial cables or twisted-pair cables

Output Waveform Characteristics

(Deleted)

Circuit Delay

24 nsec (typ)
30 nsec (max)

Current Requirements

+6v: 80 ma (max)

Power Dissipation

0. 48w (max)

Handle Color Code

Green

APPLICATIONS

Since one XD-335 PAC can introduce 0.3-amp transients with 10-nsec transition time into the ground and +6-v supply, all PACs should be as close as possible to the system power supply to minimize intercoupling through ground or power connections.

For best operation, the transmission line should be connected directly to the PAC at its connector and run continuously to the receiver (a NAND gate or equivalent). Whenever a different cable is used to couple the driver to the main transmission line, reflections are inherent. However, if the line impedance mismatch is minimal, signal degradation may be tolerable. Open wire lines should never be used for coupling, and a twisted-pair should not be used to couple the driver to a 50-ohm coaxial cable. A twisted-pair can be used for coupling the driver to another twisted-pair cable.

Twisted-pair cables are heterogeneous and some experimentation may be necessary to determine the optimum total series resistance on the PAC. For many twisted-pair cables, no modifications will be required. The recommended procedure to find the optimum series resistance is to monitor the signal at the PAC output and trim the series resistance until the initial transitions (not to be confused with reflections) are one-half the total transition in amplitude. Alternatively, the resistors may be trimmed to yield the optimum signal at the end of line.

Generally, twisted-pair cables with an increasing number of pairs require correspondingly less total series resistance on the PAC. Each individual pair in larger cables may require substantially different optimum total series resistance. For a cable containing 24 pairs, the individual optimum total series resistance varies between 50 and 70 ohms.

The termination of any line driver should normally be a single NAND gate. If more than one gate is driven, the result will be dc attenuation (resulting in lower noise protection from ground) and a lower impedance termination.

The maximum length of transmission line to be driven is determined by the length of time the driving source behaves as a low impedance. The length of time for this low impedance is 30 nsec and, therefore, the maximum length of transmission line is:

$$L_T = \frac{30}{2t} = \frac{15}{t} \text{ ft},$$

where L_T is the total length of transmission line in feet and t is the delay of transmission line in nanoseconds per foot. For twisted-pair cables, the delay is approximately 1.5 nsec per foot and, therefore, the maximum length to be driven is 10 ft.

For desired lengths of transmission line, which are longer than the low impedance limitation, a terminating resistor may be used at the receiver end. When this is done, the output from the standoff terminals of the respective circuit is utilized. A jumper wire is connected between the standoff terminals. The terminating resistor should be tied to the positive supply voltage (refer to Figure 3-29.5). The maximum current to the driver when e_2 is 0v should not exceed 50 ma. When used in this mode of operation, the maximum length of the line that can be driven at 5-mc rates is 50 ft.

The XD-335 PAC is capable of driving long lines when used in the following manner.

1. On the XD μ-PAC, coaxial cable, twisted pair, etc., is connected to output pins 25, 32, 15, 20, 3 and 9 as in normal operation for short line lengths (less than 10 feet).

2. On the standoffs provided, a 150-ohm ±5%, 1/2 watt resistor is inserted for R2, R4, R6, R8, R10 and R12.

3. Auxiliary output pins 21, 30, 11, 17, 1 and 6 are returned to +6v (pin 34 or any other convenient power supply source).

The 150-ohm resistors add an additional pull-up current, nominally 38 ma, and provide a partial termination to the transmission line when the XD output is at the ONE level. As in normal short line operation, the fanout is limited to two or three unit loads at the far end of the line due to the voltage shift across the series terminating resistor (R1, R3, etc.). The XD-335 is supplied with a series terminating resistor of 62 ohms, which may be used for most transmission cables, including twisted pair.

The minimum ONE level output at the far end of the line will be as follows:

Cable Impedance	Output After One Cable Length Delay Time	Output After Three Cable Length Delay Times
65 ohms	3.0v	4.4v
75 ohms	3.4v	4.8v
93 ohms	4.0v	5.3v

For a long line, on successive reflections, the output will step up to 6.0v in an exponential manner. If the upper input threshold limit on the receiving circuit is 3.0v, the receiver will be fully switched when the signal has propagated once down the transmission cable. To provide operating margins, transmission line impedances should be equal to or greater than 62 ohms so that there will be no restrictions on repetition rate. This is adequate for most twisted pair and coaxial cables.

In any event, for both normal short line operation and the above-described long line operation, the 62-ohm terminating resistor should be trimmed to the specific characteristic impedance of the transmission cable. The repetition rate is then restricted only by the bandwidth of the cable. If care is not taken to match the line, the following rule should be used: the transmitted pulse width in nsec divided by the line length in feet should be greater than 6. This allows two reflections of one input transition to die out before a second transition occurs. For example, a 5-mc square wave may be transmitted down a line 16 feet long and a 1-mc square wave may be transmitted down a line 83 feet long. Trimming the terminating resistor value requires inserting a resistor at the standoffs provided and using the auxiliary output for normal short line operation. For long line operation the 62-ohm resistor is unsoldered and replaced with the appropriate value.

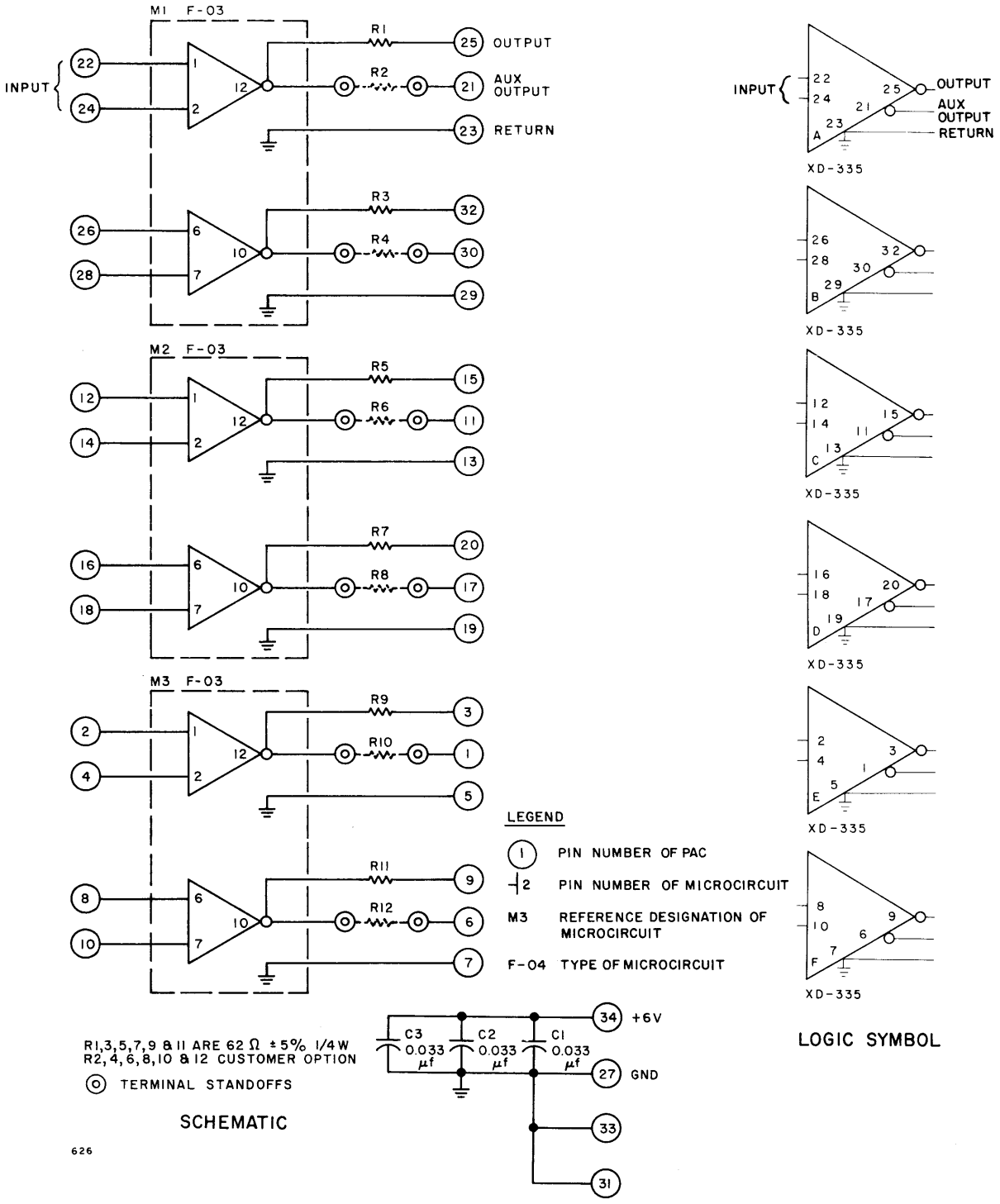
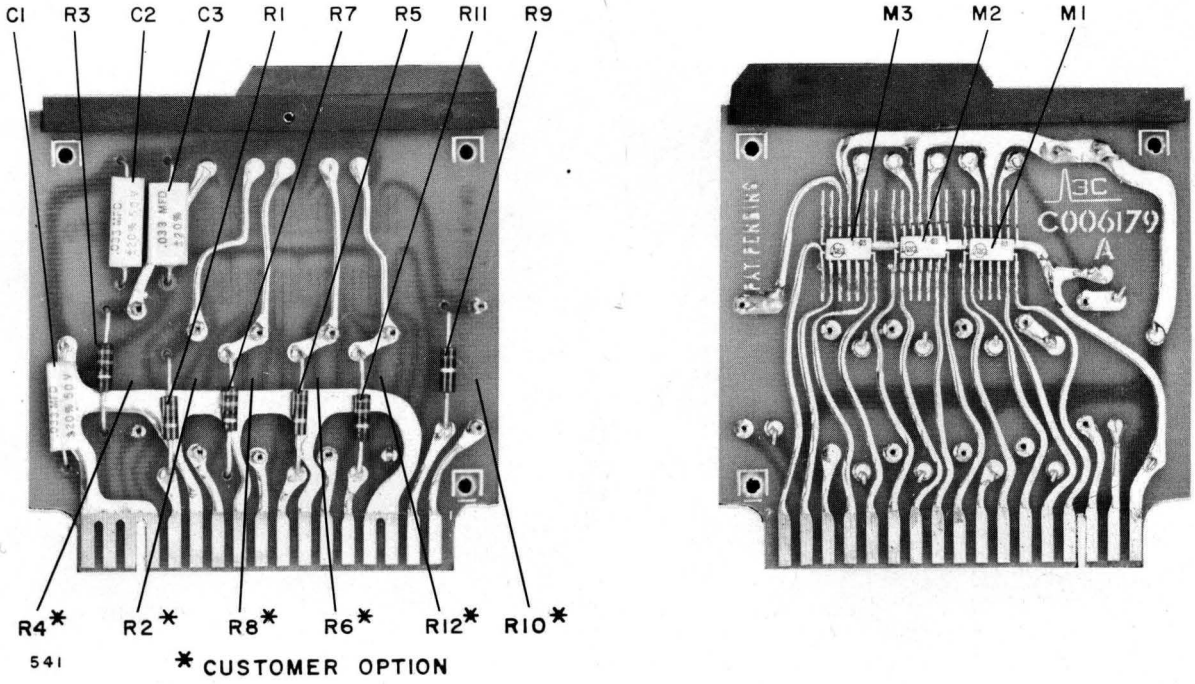


Figure 3-29.1. Transmission Line Driver PAC, Model XD-335, Schematic Diagram and Logic Symbol

Parts Location



Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1 - M3	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1 - C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
R1, R3, R5, R7, R9, R11	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4w	932 007 020
R2, R4, R6, R8, R10, R12	RESISTOR (Customer option)	

Figure 3-29.2. Transmission Line Driver PAC, Model XD-335, Parts Location and Identification

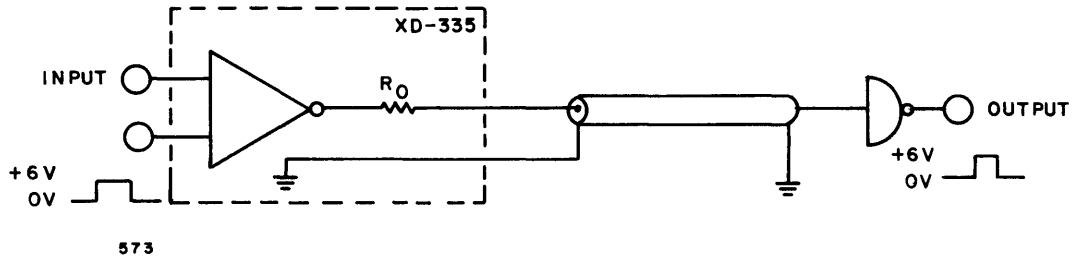


Figure 3-29.3. Transmission Line Driver PAC, Model XD-335, Line Termination at the Driving End with Matched Impedance

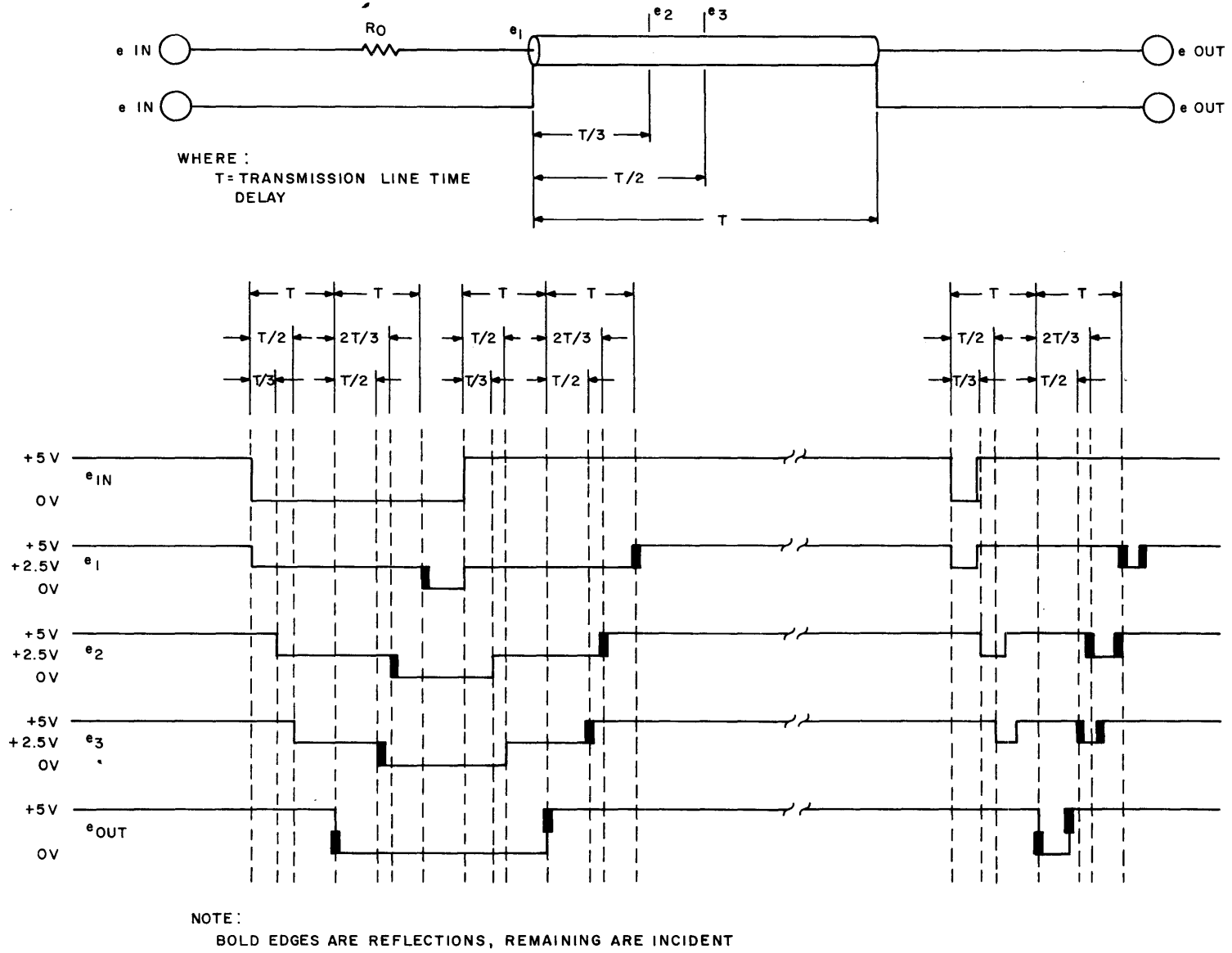


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Figure 3-29.4. Transmission Line Driver PAC, Model XD-335, Transmission Line Waveform Characteristics

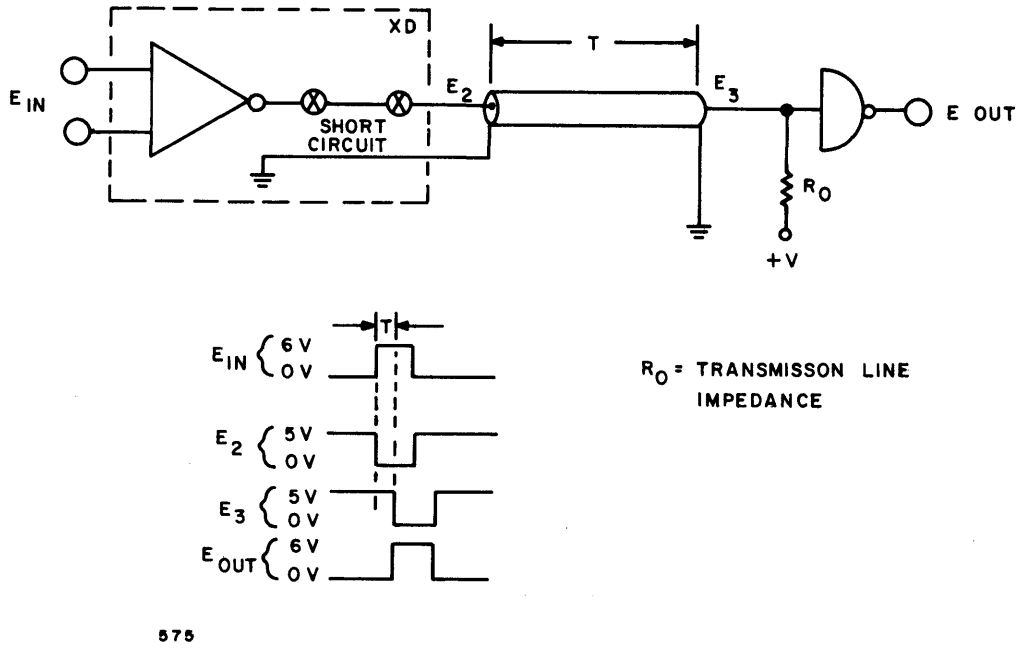


Figure 3-29.5. Transmission Line Driver PAC, Model XD-335, Line Terminated with Matched Impedance

3-29A TRANSMISSION LINE DRIVER PAC, MODEL XD-336

The Transmission Line Driver PAC, Model XD-336 (Figures 3-29A.1 and 3-29A.2), contains six identical circuits which drive standard 50-ohm, 75-ohm, and 93-ohm coaxial cables, or twisted-pair cables at up to 5-mc repetition rates. The transmission line termination should be a high impedance. A standard NAND gate is recommended.

The design principle produces the following: a small amount of current in the PAC, only one unit load of static current (1.6 ma) on the line, one-half the amount of transient current (50 ma max) as with normal terminating methods, no terminating resistor at the receiver end, and a 5-v signal at the end of the line. Since the line is lightly loaded, only small currents are incident on the receiver, thereby simplifying the grounding techniques at the receiver. The outputs of the driver are short-circuit protected.

CIRCUIT FUNCTION

Each driver circuit, which performs a NAND function, contains two 2-input micro-circuits. Of the two output pins which are provided with each circuit, one is connected through a 62-ohm resistor. Standoff terminals are provided with the other output pin for mounting a resistor when a transmission impedance other than 62 ohms is used. The standoff terminals are spaced to accept an Allen Bradley 1/4-w, 5 percent resistor.

In addition, each circuit has a ground pin adjacent to the output terminals for the signal return from the transmission line.

The principle of operation of the XD-336 is to match the transmission line characteristic impedance at the driver end and open-circuit the receiving end. A 2.5-v signal sent down the line results in a 5-v signal at the receiving end due to the +1 reflection coefficient. The reflected 2.5-v signal travels back to the driver and is completely absorbed in the termination at the driver with no multiple reflections. (Refer to Figures 3-29A.3 and 3-29A.4.)

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 mc

Input Loading

1 unit load each

Output Drive Capability

50-ohm, 75-ohm, or 93-ohm coaxial cables or twisted-pair cables up to 50 ft long

Circuit Delay

35 nsec (typ)
40 nsec (max)

Current Requirements

+6v: 80 ma (max)

Power Dissipation

0.48w (max)

Handle Color Code

Green

APPLICATIONS

Since one XD-336 PAC can introduce 0.3-amp transients with 10-nsec transition time into the ground and +6-v supply, all PACs should be as close as possible to the system power supply to minimize intercoupling through ground or power connections.

For best operation, the transmission line should be connected directly to the PAC at its connector and run continuously to the receiver (a NAND gate or equivalent). Whenever a different cable is used to couple the driver to the main transmission line, reflections are inherent. However, if the line impedance mismatch is minimal, signal degradation may be tolerable. Open wire lines should never be used for coupling, and a twisted-pair should not be used to couple the driver to a 50-ohm coaxial cable. A twisted-pair can be used for coupling the driver to another twisted-pair cable.

Twisted-pair cables are heterogeneous and some experimentation may be necessary to determine the optimum total series resistance on the PAC. For many twisted-pair cables, no modifications will be required. The recommended procedure to find the optimum series resistance is to monitor the signal at the PAC output and trim the series resistance until the initial transitions (not to be confused with reflections) are one-half the total transition in amplitude. Alternatively, the resistors may be trimmed to yield the optimum signal at the end of line.

Generally, twisted-pair cables with an increasing number of pairs require correspondingly less total series resistance on the PAC. Each individual pair in larger cables may require substantially different optimum total series resistance. For a cable containing 24 pairs, the individual optimum total series resistance varies between 50 and 70 ohms.

The termination of any line driver should normally be a single NAND gate. If more than one gate is driven, the result will be dc attenuation (resulting in lower noise protection from ground) and a lower impedance termination.

The maximum length of transmission line to be driven by the XD-336 is 50 ft.

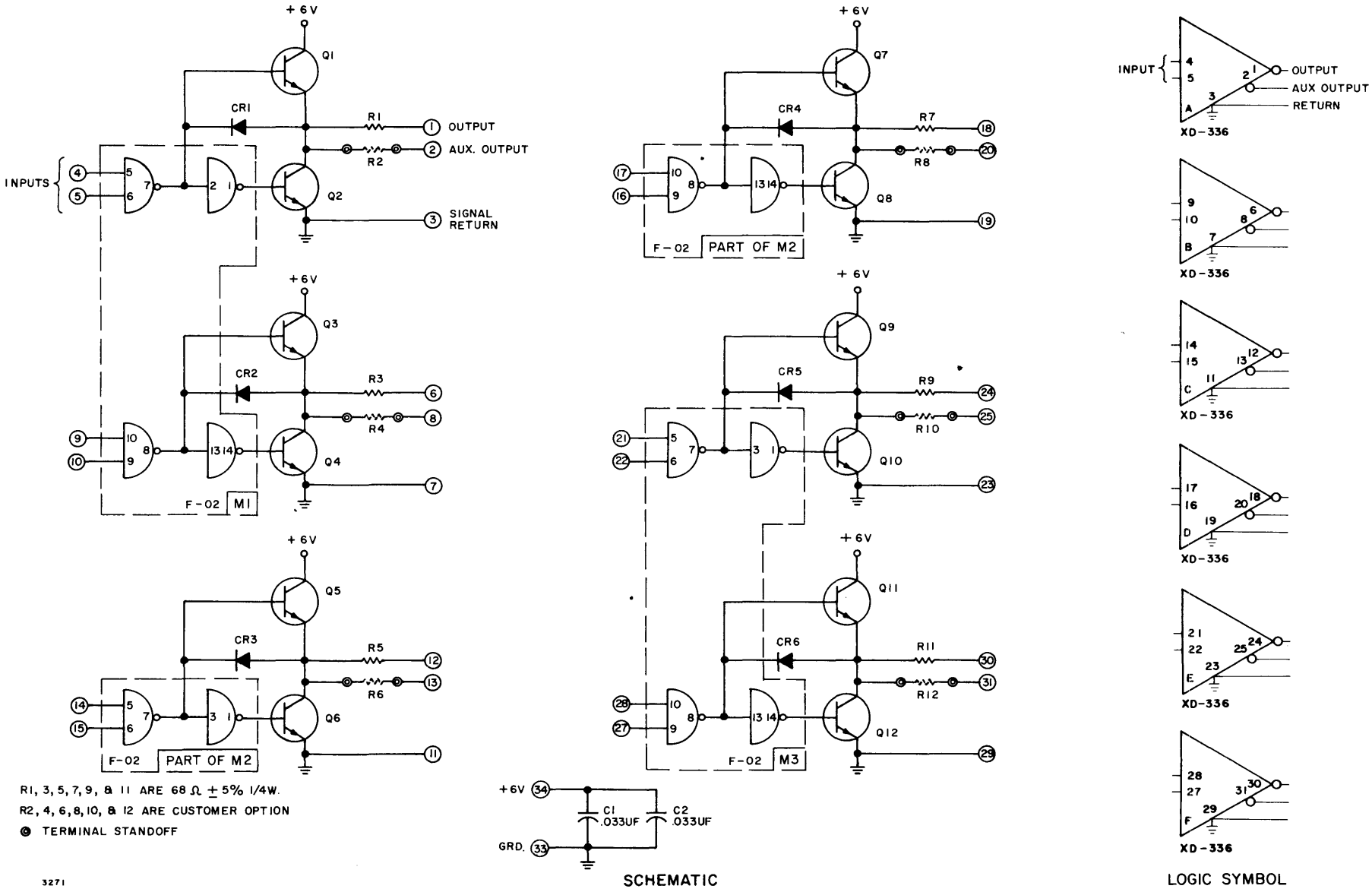
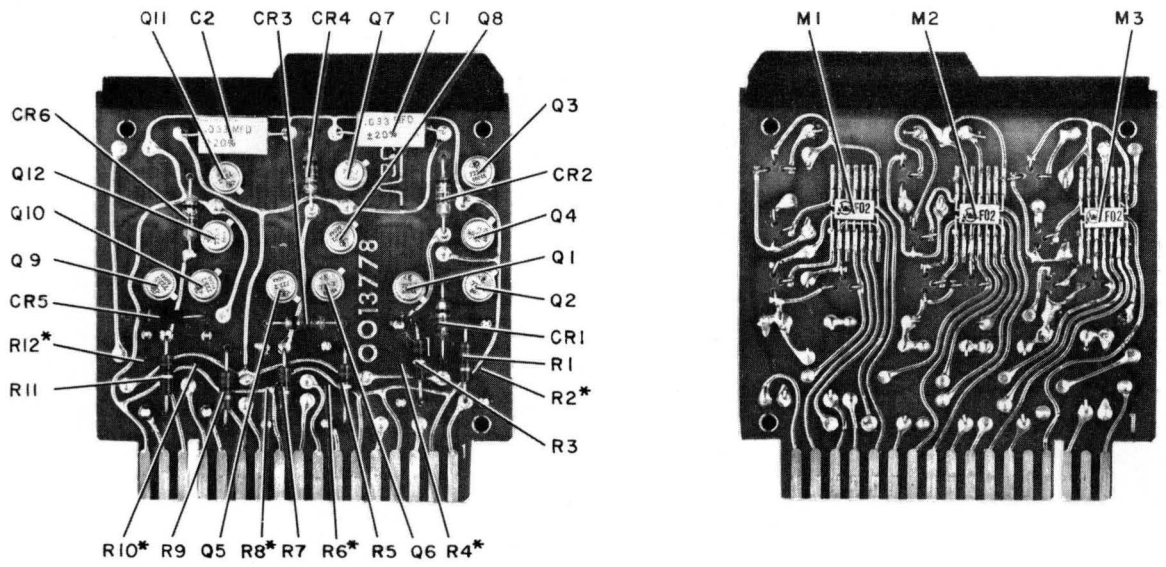


Figure 3-29A.1. Transmission Line Driver PAC, Model XD-336, Schematic Diagram and Logic Symbol

Parts Location



*CUSTOMER OPTION- CAN BE MOUNTED BETWEEN STANDOFF TERMINALS

A3325

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±5%, 50 vdc	930 313 216
CR1-CR6	DIODE, SILICON	943 083 001
R1, R3, R5, R7, R9, R11	RESISTOR, FIXED, COMPOSITION: 68 ohms ±5%, 1/4w	932 007 021
R2, R4, R6, R8, R10, R12	RESISTOR* (Customer option)	
M1-M3	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
	*NOTE: These items not included unless specified by customer	

Figure 3-29A.2. Transmission Line Driver, Model XD-336, Parts Location and Identification

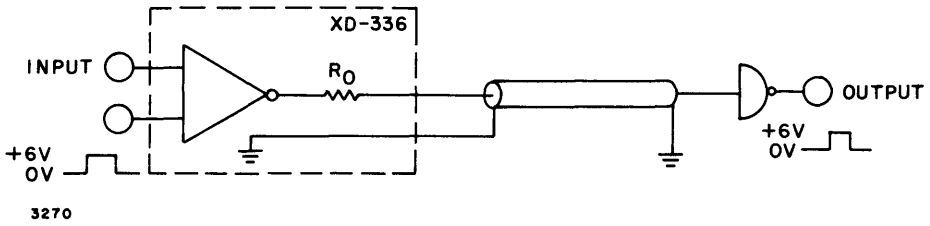


Figure 3-29A.3. Transmission Line Driver PAC, Model XD-336, Line Termination at the Driving End with Matched Impedance

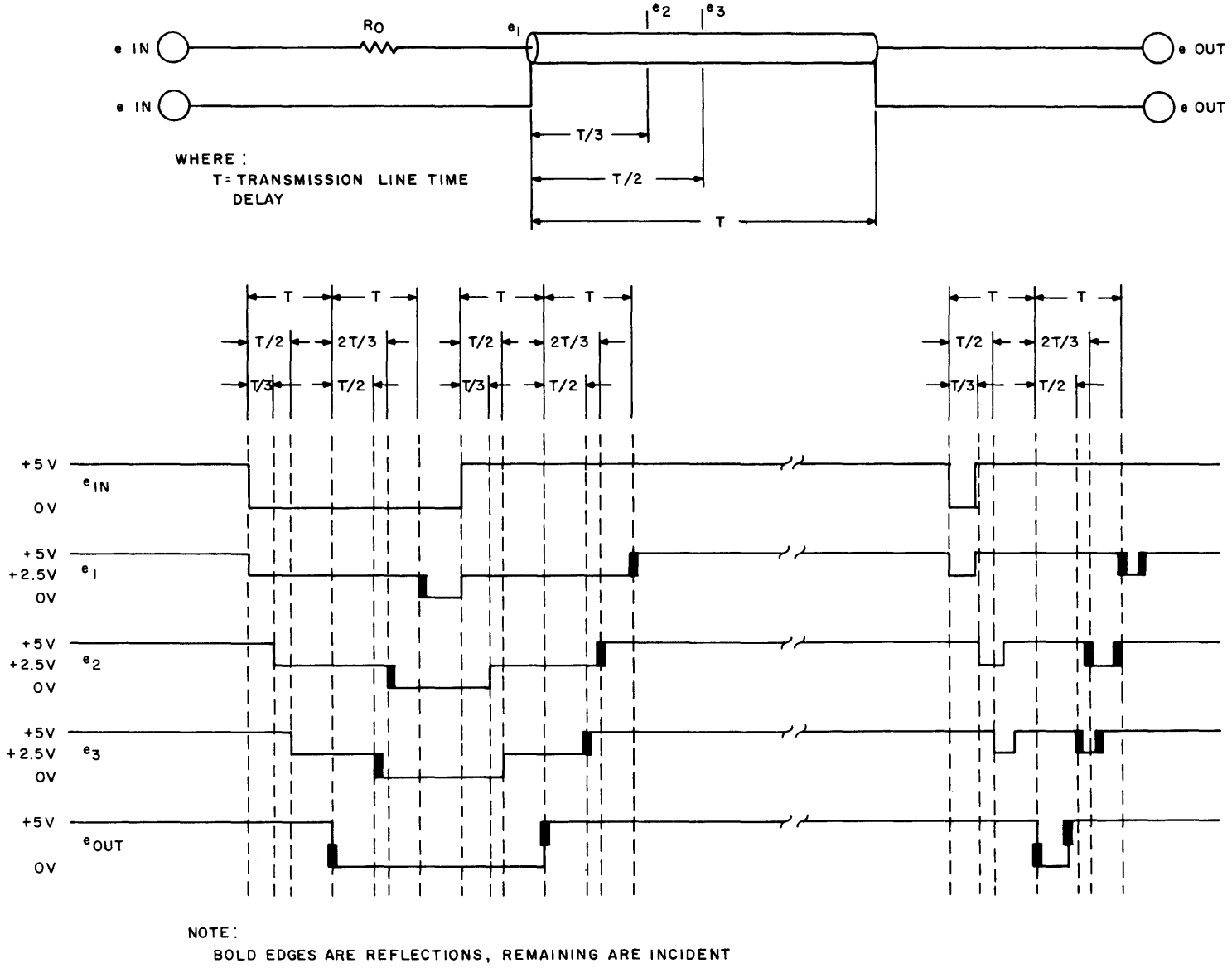


Figure 3-29A.4. Transmission Line Driver PAC, Model XD-336, Transmission Line Waveform Characteristics

3-30 EXTENDER PAC, MODEL XP-330

The Extender PAC, Model XP-330 (Figure 3-30.1), provides unobstructed access to any μ-PAC while it is electrically mounted in its appropriate μ-BLOC connector. The connector terminals at the front end of the XP-330 mount into any μ-BLOC connector and the connector at the rear accepts the μ-PAC it is displacing. Front and rear terminals are directly tied together electrically.

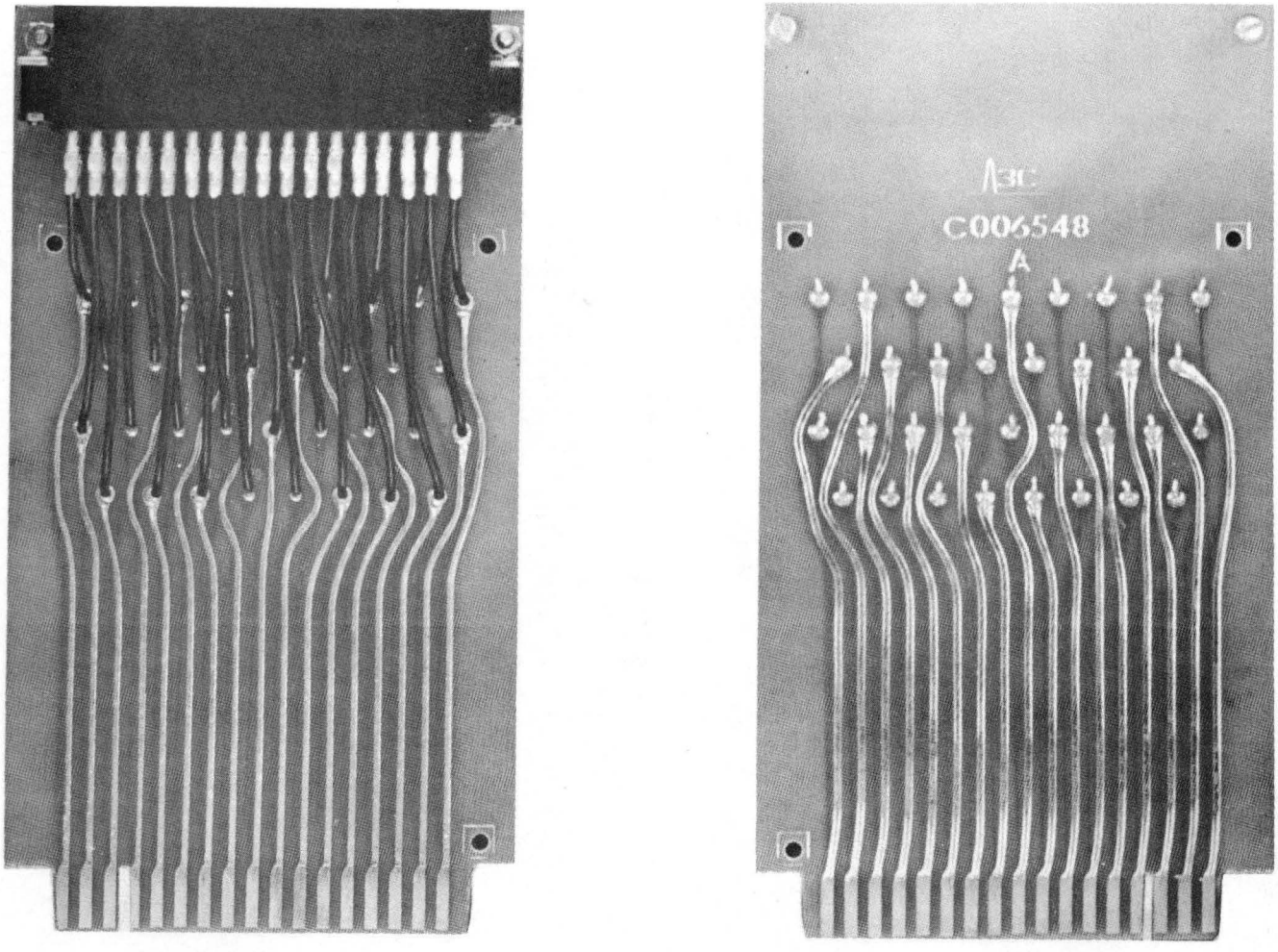


Figure 3-30.1. Extender PAC, Model XP-330

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