COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

OCTOBER 1967

1967 FALL JOINT COMPUTER CONFERENCE


AR
DR
ICM-500 I/C CORE MEMORY

New I/C 500-600 nsec Memory System . . .

. . . Stores 1/4 million bits in single 5-1/4″ high unit, features MTBF of 12 years under normal 40-hour week operation

The ICM-500 Series* is the newest addition to Honeywell's broad line of μ-STORE magnetic core memory systems. It combines high speed, large capacity, flexible packaging, high reliability, and maximum use of integrated circuits in a compact, economical system. Plus, you get a choice of standard model configurations to meet your special design requirements.

Speed — Standard Systems: 600 nanoseconds full cycle time. Special systems: available with cycle times as low as 500 nanoseconds.

Capacity — Standard models now up to 16,384 words with 54 bits/word; or up to 4096 words with 72 bits/word. (Over ¾ of a million bits in little more than 15″ of vertical rack space, including power supply). Special memory systems are available with larger capacities.

Packaging — Model ICM-500E is designed for pull-out rack mounting; Model ICM-500 for flexible mechanical mounting. All circuit modules, core stack, and interconnections are easily accessible from the front of the rack.

Integrated Circuits — Used for all major functions, including X-Y current drivers, resulting in a highly compact and reliable unit. Circuit organization has drastically reduced system interconnections and lead lengths.

Reliability — MTBF exceeds 25,000 hours.

Temperature Range — 0° to 50°C

If you've drawn a block marked "core memory system" recently, let us tell you the full ICM-500 story. You'll find our eight years' experience has again produced a standard product designed to solve your memory problems.

Write today for our new brochure. It gives all the details. Honeywell, Computer Control Division, Old Connecticut Path, Franmingham, Massachusetts 01701.

*Patent applied for.

Honeywell

COMPUTER CONTROL DIVISION

CIRCLE NO. 1 ON INQUIRY CARD

Editorial Notes

URBAN PROBLEMS AND THE COMPUTING PROFESSION

During the relatively short lifetime of the "computer business," we have seen the applications of our systems spread in all directions and into nearly all aspects of the nation's activities. Only a few years ago, our applications were wholly in scientific calculation and business processing, with a few venturesome souls investigating such "futures" areas as industrial control and real-time banking. Occasional voices in the wilderness called to us to take notice of and tend to the social implications of our advancing technology, but our direction has been of necessity determined by the availability of money to finance the development of new machines and systems, and that money has been abundant only for space/military systems, business, and industrial machines.

With public problems rising exponentially, they are finally reaching the level where responsible authority is joining the wilderness voices in calling for action, and public attention is being drawn to such problems as pollution, electrical power service, automobile safety, conservation of natural resources, and the functioning of urban areas. Public money follows public attention, and sufficient incentive now exists that private companies can consider the development of machines and systems aimed at solving these problems.

Of particular attention to us in the business of developing, marketing, and producing digital systems is a forthcoming symposium, sponsored by the four New York City area chapters of The Association for Computing Machinery, on the subject "Application of Computers to the Problems of Urban Society." This second annual one-day symposium will be held on November tenth at the New York Hilton, and is designed to promote the exchange of ideas, information, and experiences among professionals from industry, government, and universities. Registration is $18.

Five well-known authorities will address the Symposium in the morning — Deputy City Administrator Emmanual Savas of New York (who is also General Chairman of the Symposium), Edward Hearle of Booz Allen, Professors Russell Ackoff and Britton Harris of the University of Pennsylvania and Commissioner Austin Heller of New York City. Following the luncheon address by Undersecretary Robert C. Wood of The Department of Housing and Urban Development, fifteen contributed papers will be given in three parallel sessions. One session will be concerned with school planning, forecasting, and an operations research approach to racial desegregation, optimization of municipal fiscal policies, and a model for allocating urban activities in a state. The second session will be devoted to urban and state planning, data banks, and problems in public transportation systems. The third session includes papers on air and water pollution, sewage system design, transportation, and traffic control.

The Editors of Computer Design believe that our readers would be well advised to become aware of the state-of-the-art in the application of computing equipment to urban problems. We feel that the most dramatic progress will be made when government and industry officials are fully aware of one another's problems and capabilities, and this Symposium promises to be a mechanism for accomplishing such a dialogue. We commend the New York area ACM for its efforts and recommend the Symposium to our readers. Further information can be obtained from the Symposium Registration Chairman, Mr. Arthur Hutt, Bowery Savings Bank, 110 East 42nd Street, New York City.

S. Henry Sacks

S. Henry Sacks, Editor

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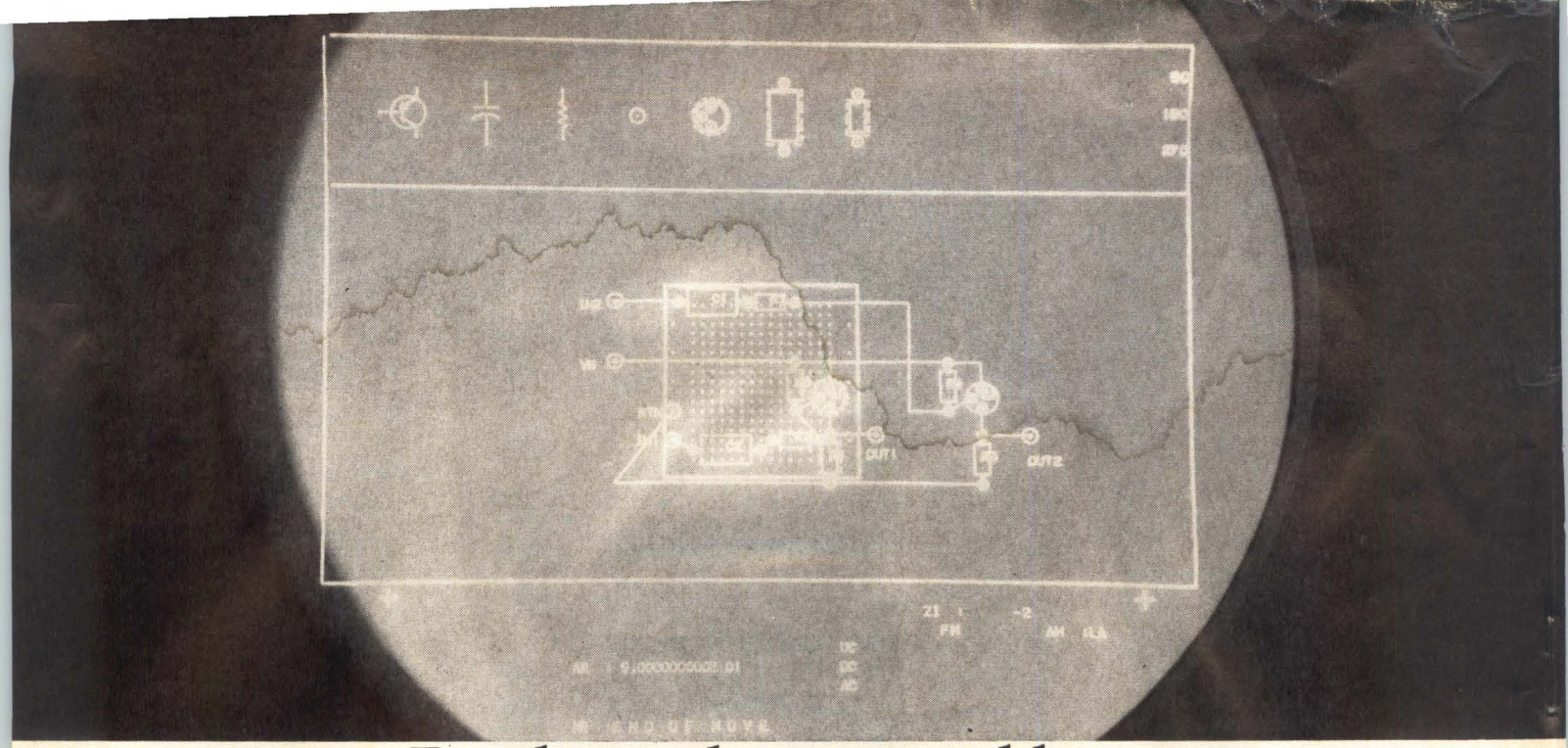
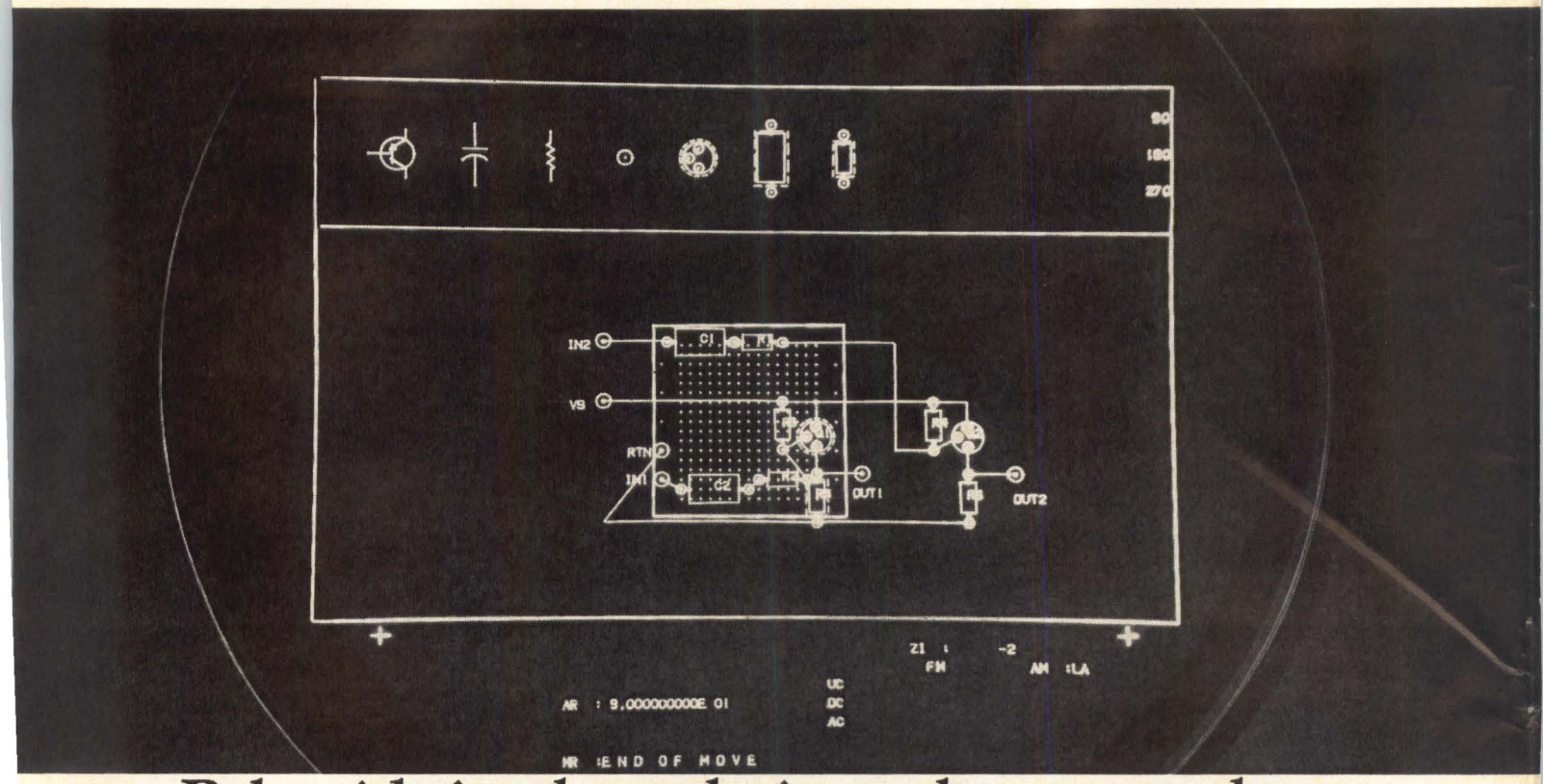


Readouts clear up problems.



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It's never a problem to read readouts if they're equipped with Polaroid circular polarizers. Our polarizers improve readability from every angle by increasing contrast. In daylight. Or even in brightly lighted rooms.

But now you don't have to take our word for it. Send for our new brochure, and we'll include 3 samples of our circular polarizers (amber, neutral, and green). They'll help you see very clearly why many major display and instrument manufacturers are now using Polaroid circular polarizers.

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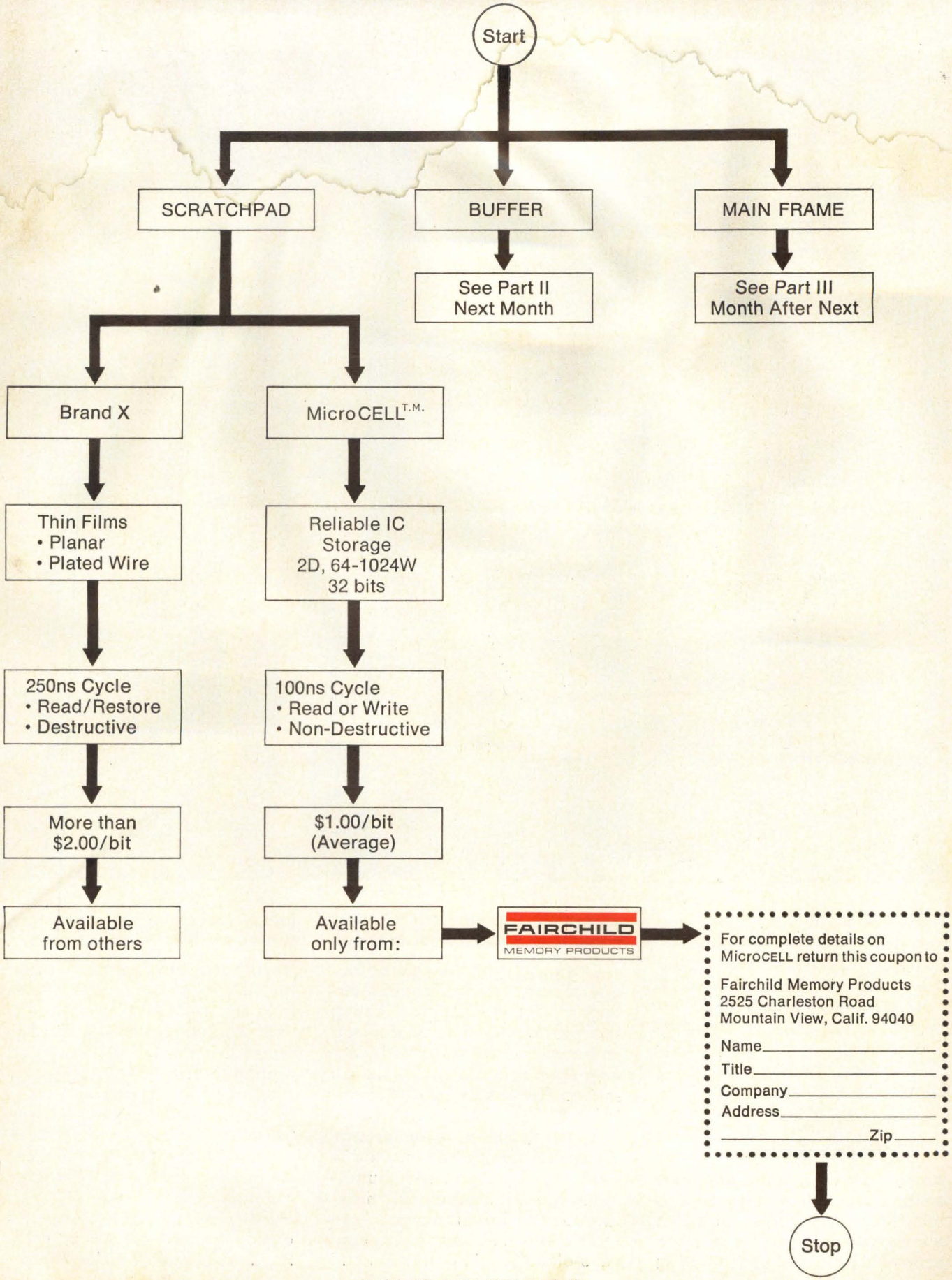
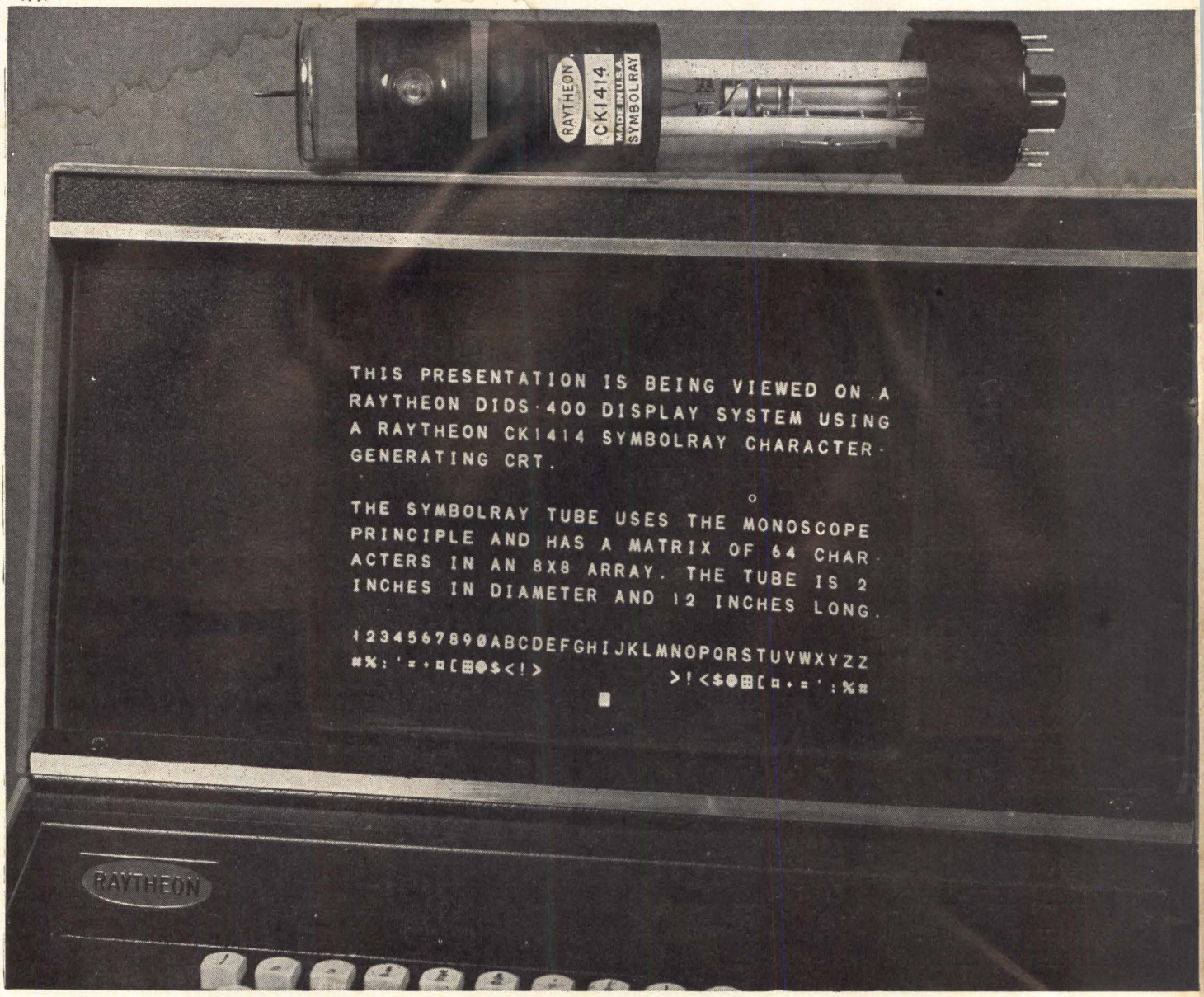
Polaroid®

How to improve your memory: Part I



Data Display Devices from Raytheon



The presentation you see above was generated by a Symbolray* Cathode Ray Tube identical to the one lying on the console. A new type of monoscope, the Symbolray can generate alphanumerics from electrical signals for cathode-ray display or for hard copy print-out. The presentation here is shown on a Raytheon tube (CK1415) used in a Raytheon DIDS-400 display system.

An economical method of generating characters. Priced at less than $100 in quantities of 1,000, the Symbolray provides a more economical method of generating electronic displays than using large numbers of circuit cards.

The output of the Symbolray operating as a monoscope is obtained by electrically deflecting the electron beam to desired characters on the target and scanning them sequentially with small raster. The display cathode ray tube on which this output is viewed is scanned in synchronism. When the Symbolray method is used in conjunction with buffer-memory techniques, full messages can be displayed—as shown above. The Symbolray tube uses electrostatic deflection and focus, and is available in designs with 64 and 96 character matrices.

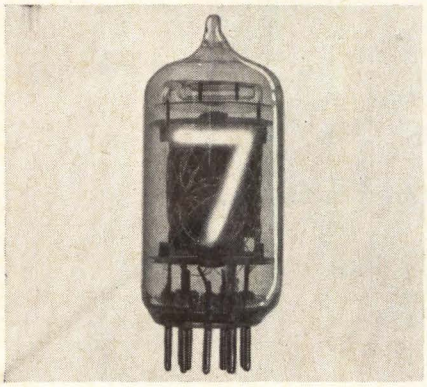
Raytheon's wide range of Dataray* CRTs cover the screen sizes from 7 to 24". Electrostatic, magnetic and combination deflection types are available for writing alphanumeric characters while raster scanning. Raytheon also offers combination deflection or "diddle plate" types and all standard phosphors. Or, Raytheon can meet your special CRT design requirements.

For more information—or a demonstration—call or write your Raytheon regional sales office.

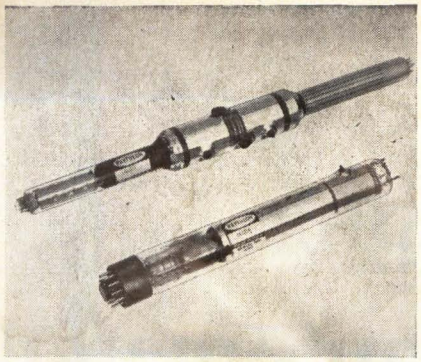
New Raytheon Projectoray* Tube produces more than double the light output of standard projection-type cathode ray tubes. The tube's light output is 30,000 foot lamberts, which results in a light level of 15-foot lamberts on a 3′ x 4′ lenticular screen.

The tube's expected minimum operating life is 500 hours — 20 times the life of a standard projection tube.

The Projectoray's high light output and long life are due to its novel design. The design incorporates liquid cooling of the phosphor backplate. This allows the phosphor to be energized with a very intense electron beam. At high beam levels, very high peak light output is obtained. The light image is projected through a 5″ optical window in the face of the tube. The electron gun is set at an angle to the phosphor and the deflection system compensates for keystone effects.



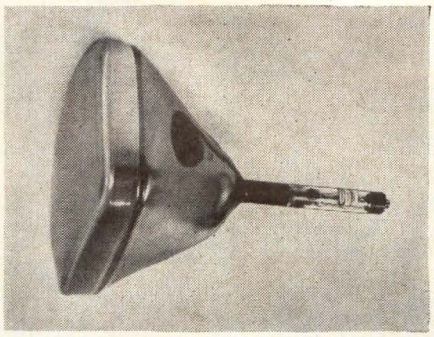
Datavue* Side-View Tubes. New Type CK8650, with numerals close to the front, permits wide-angle viewing. These side-view, in-line visual readout tubes display single numerals 0 through 9 or preselected symbols such as + and − signs. Their 5/8″-high characters are easily read from a distance of 30 feet. Less than $5 each in 500 lots, they also cost less to use because the bezel and filter assembly can be eliminated and because their mating sockets are inexpensive.



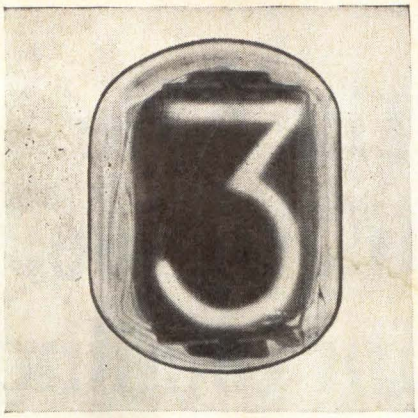
Recording Storage Tubes. The miniature tubes shown here are Raytheon's single-gun (CK1516) and dual-gun (CK1519). They provide high resolution, long storage, and fast erase capability.

Raytheon electronic input-output storage devices feature the above capabilities and immediate readout. Information can be written and stored by sequential techniques or by random-access writing. Complete, gradual or selective erasure is possible.

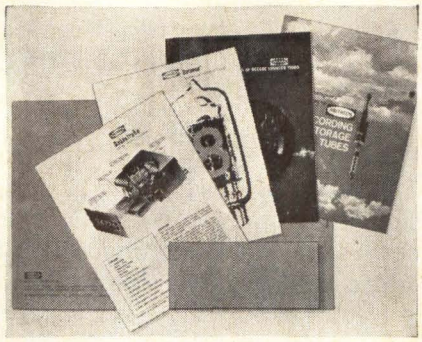
Raytheon storage tubes are readily available for applications in radar scan conversion, slow-down video, signal processing, signal enhancement, time delay, and stop motion.



Dataray* Cathode Ray Tubes. Raytheon makes a wide range of industrial CRTs —including special types—in screen sizes from 7″ to 24″. Electrostatic, magnetic, and combination deflection types are available for writing alphanumeric characters while raster scanning. All standard phosphors are available and specific design requirements can be met. Combination deflection or "diddle plate" types include CK1395P (24″ rectangular tube), CK1400P (21″ rectangular), and CK1406P (17″ rectangular).



Datavue* End-View Tubes. These tubes are easily read in high ambient light — do not wash out like other displays. Erroneous readings due to segment failure do **not** occur because the characters are fully formed. Raytheon Datavue End-View Tubes fit existing sockets and conform to EIA ratings. Models include round (CK8421) and rectangular (CK8422). Ultra-long-life types are designed for 200,000 hours or more of dynamic operation.



Send Reader Service Card for literature on the:

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Or call your Raytheon regional sales office. Or write to *Raytheon Company, Components Division, Quincy, Mass 02169.*

*Trademark of Raytheon Company

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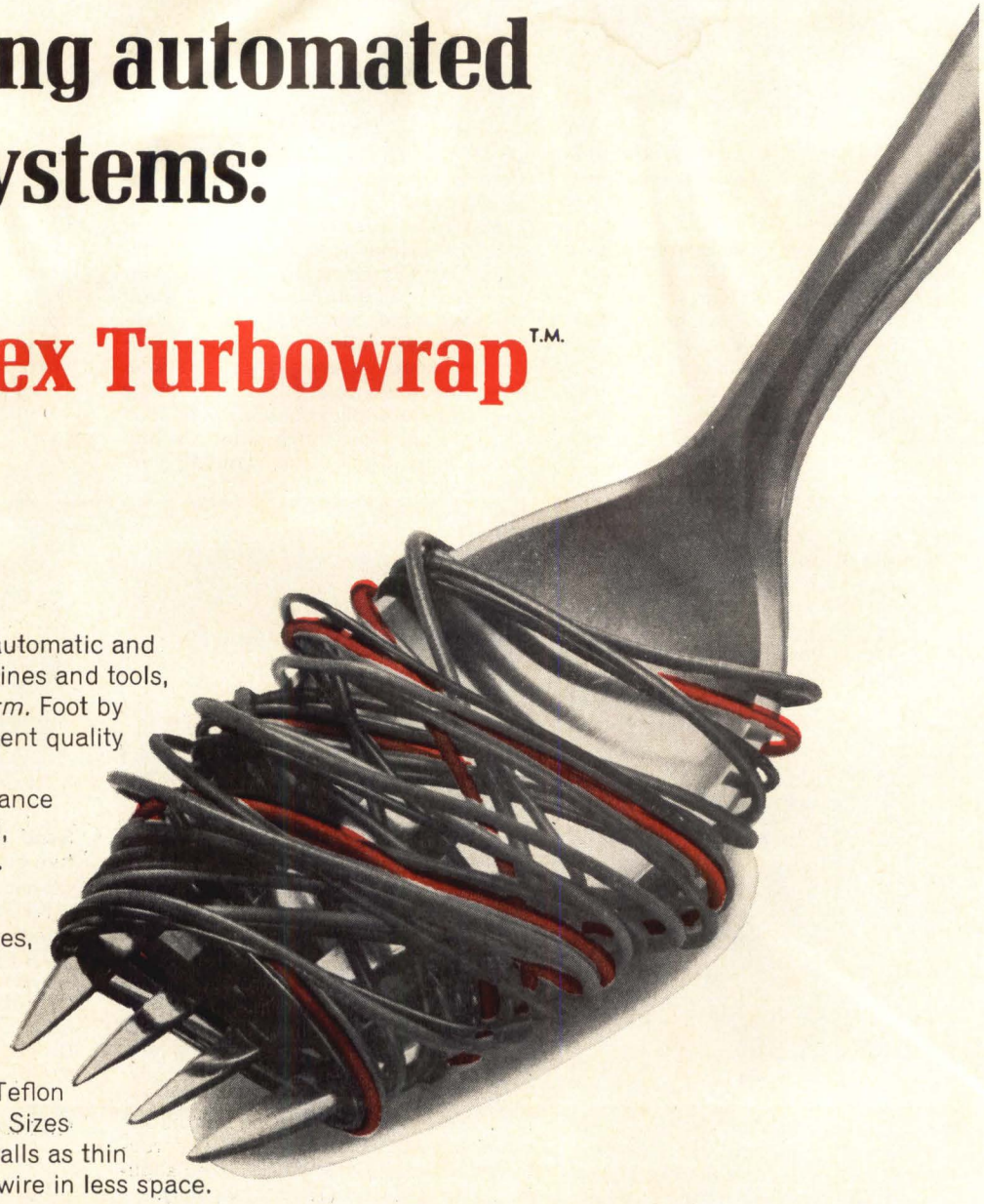
The wire that's specially-made for feeding automated wiring systems:

Brand-Rex Turbowrap™



Turbowrap runs like silk in automatic and semi-automatic wiring machines and tools, because it's *unusually uniform.* Foot by foot, and lot by lot — consistent quality in electricals, physicals and mechanicals reduces the chance of jammed or erratic feeding, nicks, strains, cuts or shorts.

And Turbowrap, in a broad choice of insulations and sizes, gives you almost unlimited design freedom. Standard insulations include semi-rigid PVC and PVC/nylon, Teflon FEP and FEP/nylon, Teflon TFE, Kynar and Polysulfone. Sizes as small as #30 AWG, and walls as thin as .004", help you put more wire in less space.

Various Turbowrap types have been expressly engineered for the world's leading manufacturers of computers and business machines. They're one reason why Brand-Rex has chalked up more UL approvals for business machine wire than any other company.

Want to get more out of automated, high-density wiring? Write us for details on Turbowrap.

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BRAND-REX DIVISION
WILLIMANTIC, CONNECTICUT 06226
PHONE 203 423-7771

BRAND REX

CIRCLE NO. 9 ON INQUIRY CARD

Need data storage capacity from 1K to 131K bits? We've got it made (and so have you).

We've got it made—literally. All the combinations you see here and hundreds of variations on our FX-12 and FX-14 core memory systems have been in mass production. They're available on dependable delivery schedules. We can ship tomorrow morning if you like.

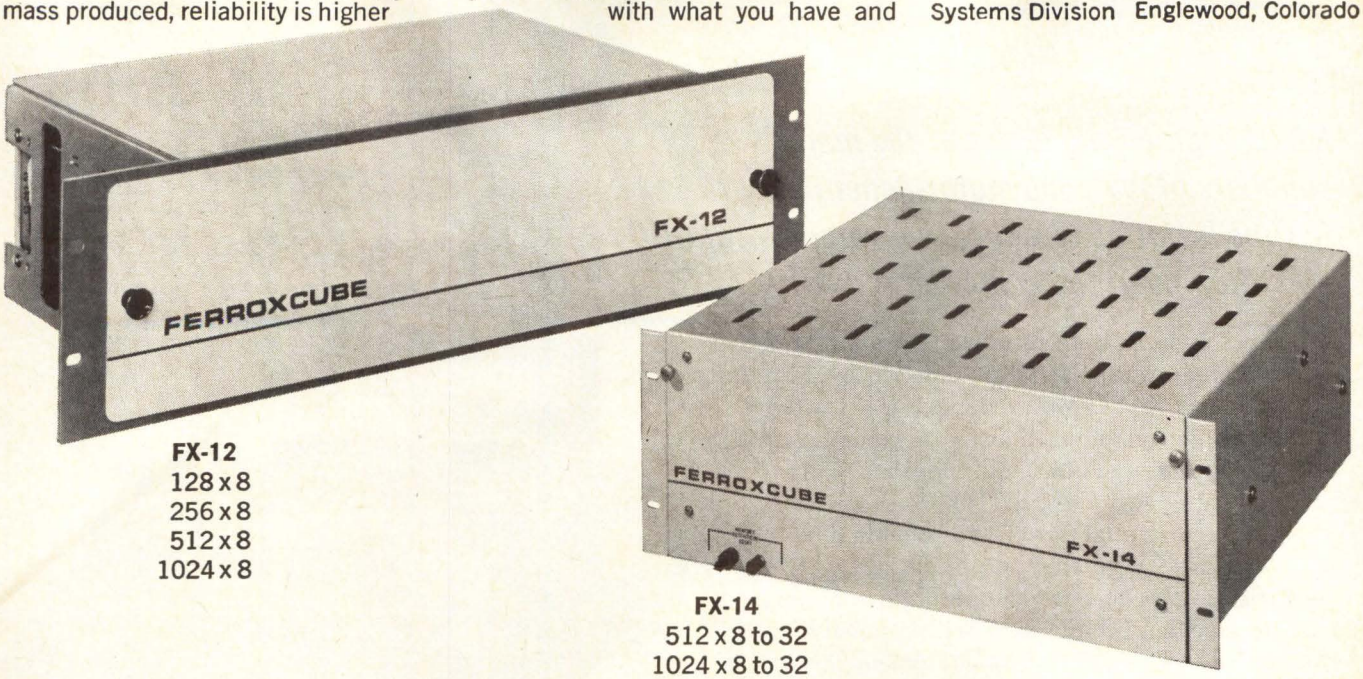
You've got it made because these are core memories with all the advantages of core storage over electromechanical techniques: speed, random access, non-dissipative, non-volatile... to name a few. And, because they're mass produced, reliability is higher than core storage systems built on a onesy-twosy basis.

You've even got it made on cost. Remember, all the engineering is done. You specify; we produce and ship. That alone narrows the cost between Ferroxcube core memories and less versatile types. Example: you can buy a Ferroxcube 1024 x 8 FX-12 system complete with stack electronics and timing for $1,990.

But that's not all. With so many models to choose from, interfacing is flexible: buy what you need to interface with what you have and save some more money.

For details on all this performance and economy, write for Bulletin MS670, "Ferroxcube Catalog-Standard Coincident-Current Memory Systems." It describes 513 ready-to-go models—with prices. Not so incidentally, we're the only manufacturer to publish a price list on memory systems. Reason: production experience; we know our costs in advance. You will too.

Ferroxcube
Systems Division Englewood, Colorado



FX-12
128 x 8
256 x 8
512 x 8
1024 x 8

FX-14
512 x 8 to 32
1024 x 8 to 32
2048 x 8 to 32
4096 x 8 to 32
8192 x 8 to 16
16,384 x 4 to 8

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CIRCLE NO. 10 ON INQUIRY CARD

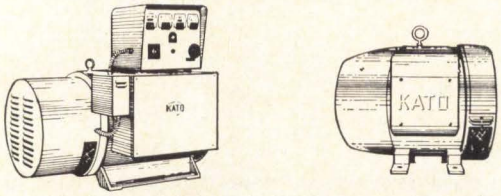
For the kind of clean power it takes to keep computers efficient, Control Data Corporation calls on KATO

KATO Engineering is one of the major suppliers of matched motor-generator sets for line isolation and cycle conversion...at CDC and throughout the computer industry.

When precision equipment demands *pure* power, free from line transients, phase unbalance and frequency fluctuations, a KATO Motor-Generator Set is the answer. In the computer industry, in communications, ground-support operations and industrial process-control functions, KATO M-G Sets take imperfect commercial power and provide the exact, balanced, regulated output desired, with continuing efficiency and absolute minimum maintenance. KATO offers the widest possible range of M-G Sets and control equipment *plus* 40 years of power engineering experience. Why not get the details?

Free 8-page folder gives complete information on KATO M-G Sets. Write for your copy today.

Typical KATO M-G Set supplied to CDC—common-frame, common-shaft construction. Motor is 30 H.P., 220/440 volt, 3-phase, low-slip, squirrel-cage induction type. Generator delivers 20 KVA, 120/205 volt, 400-cycle, 3-phase and features brushless excitation. Free-standing cabinet houses both motor and generator controls.



KATO makes many power products...
AC Generators • DC Motors and Generators

KATO

KATO ENGINEERING COMPANY
1403 First Avenue • Mankato, Minnesota 56001

CIRCLE NO. 11 ON INQUIRY CARD

General Instrument proudly announces

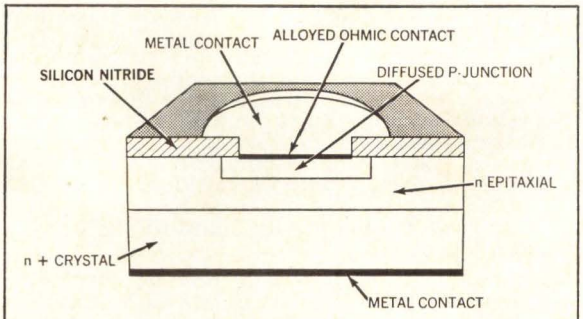
the industry's first silicon nitride computer diodes

now in production

It has long been generally recognized that semiconductor devices passivated with silicon nitride rather than with silicon dioxide would demonstrate unprecedented reliability.

Until now, however, the problem to be overcome was the difficulty of adequately handling and controlling the nitride process in mass production. General Instrument has solved that problem and is producing the industry's first line of silicon nitride passivated diodes.

The inherent reliability of silicon nitride is derived from its total imperviousness to the movement of sodium ions and extreme chemical inertness. Therefore, many of the most common modes of diode failure are eliminated. Unstable reverse breakdowns, excessive leakage currents and contamination occurring during chip handling and packaging no longer present reliability problems.



CUT-AWAY VIEW OF SILICON NITRIDE PASSIVATED COMPUTER DIODE

Superior electrical characteristics are now combined with this built-in reliability in General Instrument's line of high-speed silicon nitrided diodes in miniature DO-35 or DO-7 packages for computer applications.

Write for full information. (In Europe, to: General Instrument Europe, Via Turati 28, Milano, Italy).

GENERAL INSTRUMENT

GENERAL INSTRUMENT CORPORATION · 65 GOUVERNEUR STREET, NEWARK, NEW JERSEY

CIRCLE NO. 12 ON INQUIRY CARD

Your memory need improvement? Ampex makes cores, planes, stacks, transports and complete memory systems. Check this list for your needs.

a A data system or computer is only as good as its memory, so it pays to get the most reliable memory components and systems. Here are some examples—from a company which is a leader in the development of core and tape memories and has the technology and experience to improve your system's memory—Ampex.

Core Memories

b **START WITH FERRITE CORES...** We offer a full line of ferrite cores ranging in size from 18 to 80 mils (outside diameter). If your application involves a wide temperature range, we can supply you with lithium ferrite cores in 18- to 30-mil sizes. Chart "B" shows typical switching times.

For more information on Ampex cores, circle number 15 on Reader Card.

c **OR WITH ARRAYS OR STACKS...** We have a full line of commercial and military arrays for memory designers, and we're glad to take on design assignments for special stacks and arrays.

Our 2½D stack family has expanded and now includes 18-, 22-, and 30-mil cores. Ruggedized stacks for military applications are designed to satisfy such requirements as MIL-E-5400 and MIL-E-16400 in both 3-wire 3D and 4-wire 3D configurations.

More stack or array info? Circle 16 on Reader Card.

d **OR BUY THE COMPLETE MEMORY!** We design and build all kinds of core memory systems for commercial and military use. They begin with our widely known and used RF series, and range in size up to 20 million bits. Here is a brief view of our core memory line.

RF series is a modular family of reliable memories which offer large ranges of "store" sizes and options. Integrated circuits and "Master Board" construction cut their size and cost, increase reliability. All feature high MTBF, easy maintenance, non-destructive power shutdown.

RF-1, RF-2, RF-3 give you 1.5 microsecond cycle time. Capacities from 512 to 16,384 words, in word lengths from 4 to 72 bits. Each includes power supply. Over 4000 hours MTBF for 4K x 12 RF-1; proportional for RF-2 and RF-3.

New RF-4 memory has faster cycle time of 1 microsecond. Capacity: up to 4K x 20. Available with or without power supply.

RS memory system is a large capacity (up to 32K x 80) 1-microsecond system with a variety of options that let you tailor it to your exact needs.

For more core memory details, circle 17 on Reader Card.

e **MASS MEMORY** consists of 4 modular stacks of 5 megabits each. Cycle time is 2.7 microseconds, but unique 4-way interleafed operation with two-port entry into the four stacks results in *effective cycle time of 675 nanoseconds.*

For more core memory details, circle 17 on Reader Card.

NEW! RG MEMORY

Our brand-newest system, the RG memory packs big capacity into very small size by using integrated circuits throughout. Some features:

- 900 nanosecond full cycle
- modular (16K x 40 max. per 5¼" panel unit), can expand to 32K x 80
- operating temperature 0 to 50°C
- standard TTL positive true logic interface levels
- uses advanced IC's throughout
- low cost yet reliable and simple to maintain
- options: data parity generation and check, built-in tester, indicator panel, zone transfer; many other options

For more core memory details, circle 17 on Reader Card.

Single Capstan Tape Transports

Our tape transports meet all your requirements with data transfer rates up to 120 kHz. All offer at least 2,000 hours MTBF, at least ONE BILLION start/stop operations before replacement parts may be needed in the drive mechanism. All units are interface interchangeable. Write and read IBM compatible 7- or 9-track formats. All contain the Ampex patented single capstan electronic servo control.

f **NEW! TM-16 TRANSPORT** is the newest member of the Ampex single capstan family. It is a direct plug-compatible replacement for any IBM 729 or 2400 series transport. Besides offering higher data reliability at high speeds (60-150 ips), the TM-16 features a number of human design improvements: push-button power window for faster access and easier loading; straight-line threading for operator convenience and faster loading; optional automatic threading; and a modular design that makes maintenance simple.

For additional data circle 18 on Reader Card.

TM-7, -9, -11, -12 transports are the original single capstan transports specifically designed for digital data transfer. Over 1,000 of these Ampex tape drives are now in use around the world.

For complete and up-to-date information on transports, circle 18 on Reader Card.

g **BUFFERED TAPE MEMORIES (BTM SERIES)** incorporate an Ampex single capstan tape memory, an RF core memory and integrated circuit control logic to achieve a highly flexible digital data recording system. A functionally integrated, easy-to-use unit, the BTM buffered tape memory, can accept asynchronous digital data over a wide range of character rates, format the incoming information and record the data in blocked and gapped form on computer-compatible magnetic tape.

For more core memory details, circle 19 on Reader Card.

h **SHARED TAPE MEMORY SYSTEMS** let you save both money and floor space. They time-share the 7- or 9-track data (read/write) electronics between up to four TM-series single capstan tape transports.

TAPE CONTROL UNITS FOR COMPUTERS

The convenience and low cost of digital magnetic tape recording can now be inexpensively obtained for various medium and small size digital computers. By combining an Ampex TM-series single capstan digital tape memory with our Ampex-designed tape control unit (TCU) you have a versatile, compact, low price magnetic tape system. The TCU plugs directly into a computer's input/output interface and decodes standard magnetic tape unit program instructions for tape transport selection and data transfer control.

Sound interesting? Circle 19 on Reader Card for tape memory info.

i **HOSTILE ENVIRONMENT DIGITAL TAPE MEMORY SYSTEMS** Our ATM-13 and GTM-14 memories are designed and constructed to take the extremes of pressure, humidity, temperature, shock and vibration found in airborne, shipborne, geophysical and ground mobile applications.

The ATM-13 high performance memory system is IBM-compatible to 75 ips (60 kHz character transfer rate at 800 cpi). Continuous (gapless) to 112.5 ips. Fast start/stop times of 6 milliseconds maximum at 75 ips. Can operate continuously at maximum program rates up to 160 start/stop cycles per second. Environmental Class: MIL-E-5400-G, Class 1A; RFI: MIL-1-6181D; Source Power: MIL-STD-704. Weight: less than 150 lbs.

NEW! GTM-14 memory is IBM-compatible to 45 ips. Continuous (gapless) to 105 ips. Weighs less than 150 pounds. Low power requirements. Will operate on battery power. Capable of operation within the environment of MIL-E-5400, Class 1A.

If you're especially interested in this tough breed of memory, circle 20 on Reader Card.

a

AMPEX

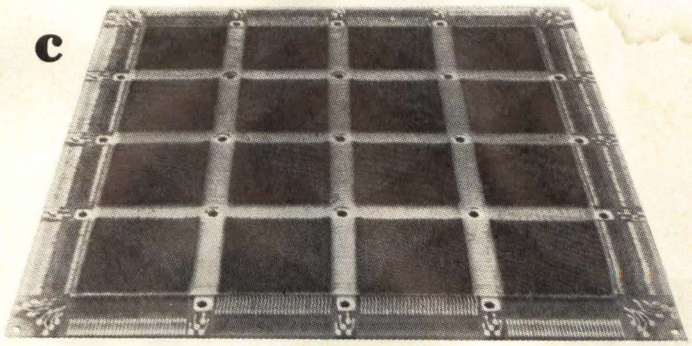
Typical switching times for Ampex Ferrite Cores

b

Core #	*Switching time*
184-06*	175 nanoseconds
204-06*	230 nanoseconds
303-03	360 nanoseconds
304-07*	380 nanoseconds
304-06*	440 nanoseconds
501-10	850 nanoseconds
504-10	1300 nanoseconds
506-15	1500 nanoseconds
802-40	3000 nanoseconds

*Wide temperature range

c



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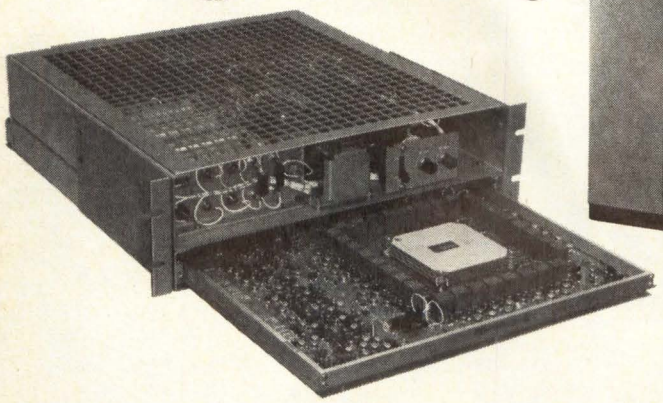

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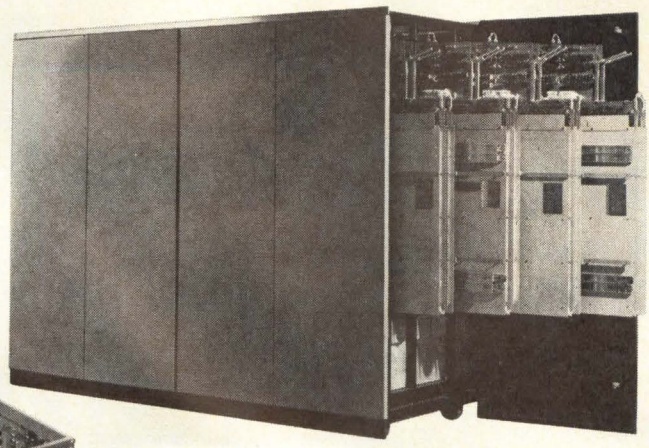

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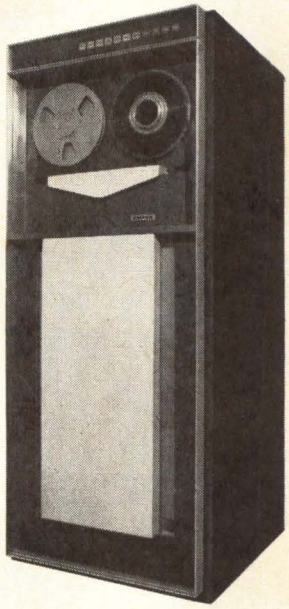

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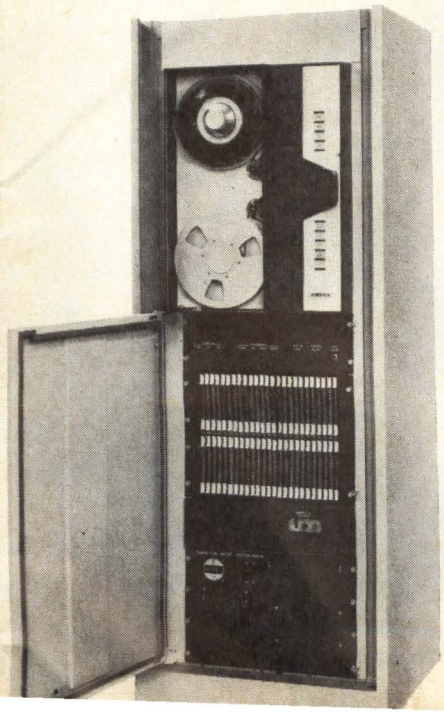

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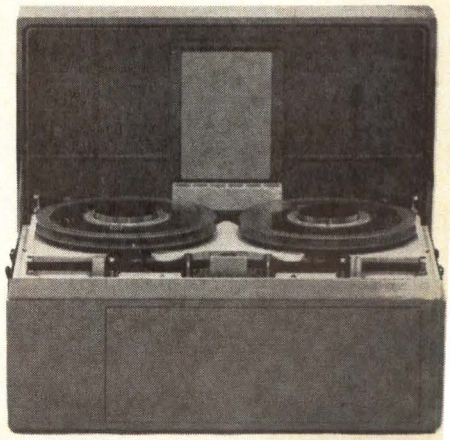


See many of these components and systems in our Booth "G" at FJCC, Anaheim, Nov. 14-16. You can't miss us—we're in the center of the hall.


SEL
SEL

The SEL 810A flies again at the Fall Joint.

Remember us at the Spring Joint Computer Conference? We were the ones with the highly popular CRT "airplane" demonstration. Look for us again at Anaheim. We'll be back with the SEL 810A High Speed Digital Computer controlling our new CRT display. Our new Computer Graphics System is a CRT display with high-speed line drawing capability. This permits image display with a minimum number of program instructions.

Another brand-new product to look for is the SEL 810B submicrosecond Digital Computer. This new unit has everything the highly regarded SEL 810A, 16-bit computer has. Plus twice the speed. Yet it's only about 20% more in price.

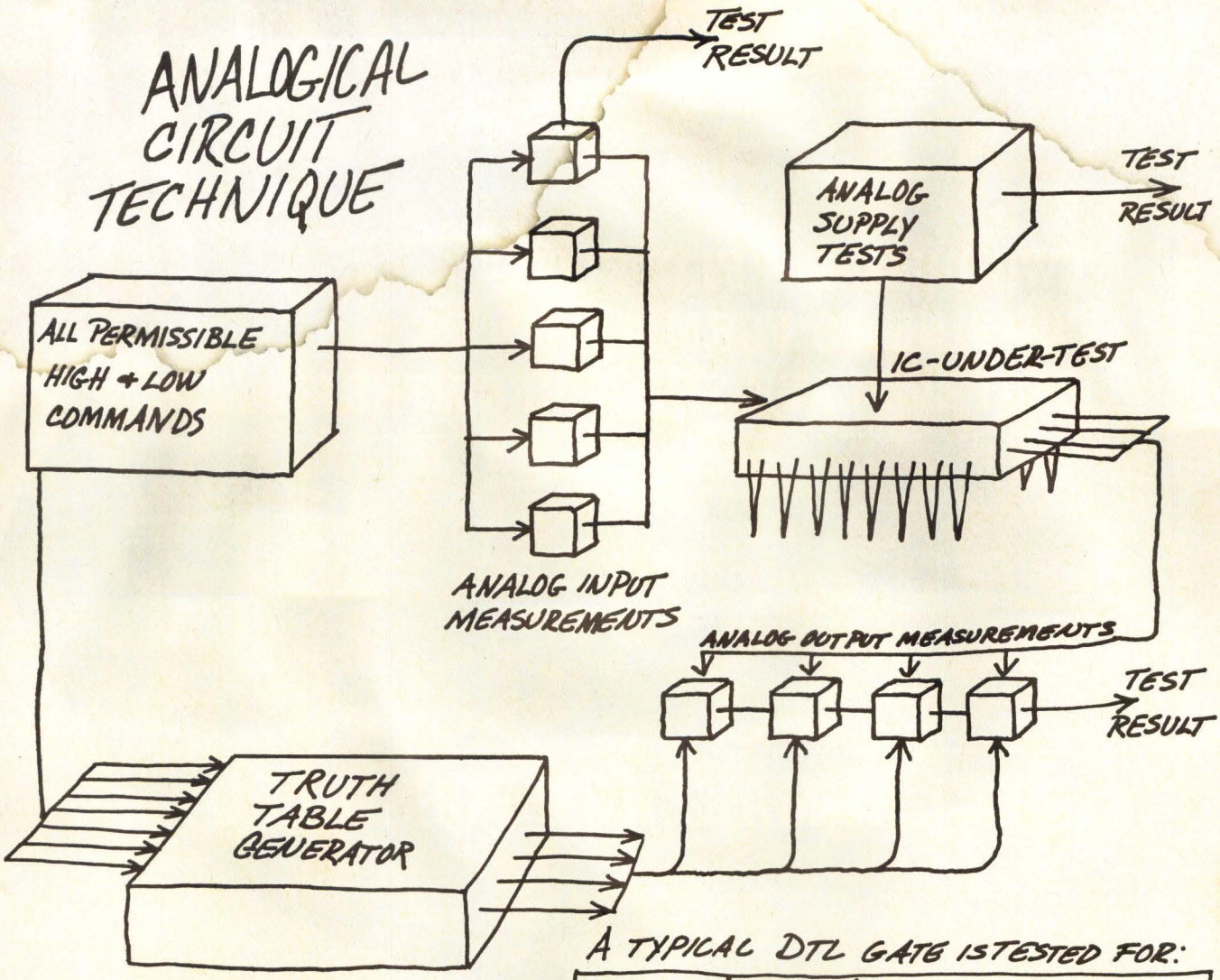
And, of course, in addition to these products, we'll be showing the SEL 840A 24-bit computer. So drop by our booth* and fly our "airplane". While you're there we'll tell you something about us. How our strengths in standard computers, computer systems, and engineering creativity, make us *the* full systems capability company.

Can't make the show? Write for details on any of the products mentioned above. Systems Engineering Laboratories, Inc., 6901 West Sunrise Blvd., Fort Lauderdale, Florida. Or call Area Code 305 587-2900.

Systems Engineering Laboratories

*Booths D1, 2, 3, 4.

CIRCLE NO. 13 ON INQUIRY CARD



A TYPICAL DTL GATE IS TESTED FOR:

$I_{IN\ HI}$	5.1 μA MAX @ 4.1 V
$I_{IN\ LO}$	1.1 mA MAX @ 1.1 V
$V_{OUT\ HI}$	2.6 V MIN @ 0.12 mA
$V_{OUT\ LO}$	0.45 V MAX @ 12.0 mA
I_{CC}	16 mA MAX @ 5.0 V

Intriguing, isn't it, this new way of testing digital integrated circuits?

Now you can make sure ALL of your ic's will work — because you can make both parameter and functional tests simultaneously, and for all permissible combinations of inputs. □ It's done by exercising all the LOGICAL inputs on the ic-under-test and selecting the appropriate ANALOG measurements that should be made. 5,000 such measurements are made in 1/100 of a second.

TERADYNE

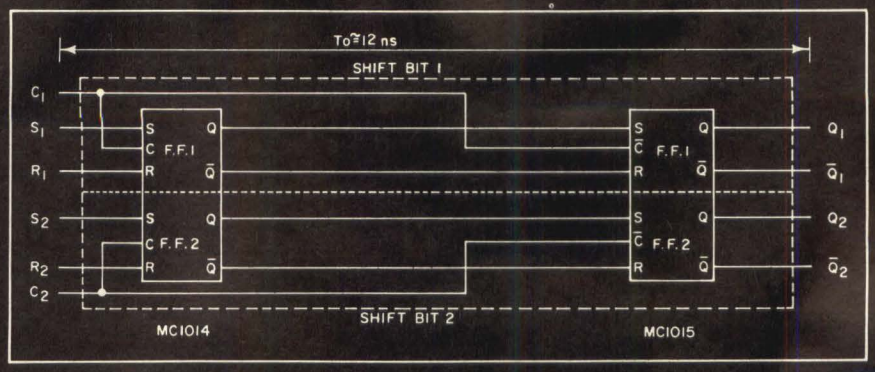
□ Even more exciting, our Analogical Circuit Technique is available on a little machine that weighs only 25 lbs. It's a cinch to program, and costs only about $5,000. □ We call it ACT 1 (because of the fortunate acronym). □ *To learn more about analogical testing, just write: ACT 1, Teradyne, 183 Essex Street, Boston, Massachusetts 02111.*

SEE YOU AT NEC, BOOTH 749

CIRCLE NO. 91 ON INQUIRY CARD

MECL II High-Speed LOGIC DESIGN IDEAS ... one of a series

TWO DUAL R-S FLIP-FLOPS COMBINE TO FORM A 6 ns MASTER-SLAVE SHIFT REGISTER!



(MECL II MAKES IT POSSIBLE!)

Two new additions to the growing MECL II line of integrated circuits, MC1014P and MC1015P, can be used as positive-gated and negative-gated R-S flip-flops, respectively. Two levels of gating are accomplished with only 2 ns increase in propagation delay. As a result, a single phase, clocked Master-Slave type of shift register with a 6 ns total propagation delay may be obtained as shown.

The MC1014P, in addition to teaming with MC1015P for shift register functions, is also useful as a dual storage element. It contains two dc Set-Reset flip-flops with a positive clock input provided for each flip-flop. MC1015P operates with a negative clock input.

Both new circuits exhibit typical propagation delays of 5.0 ns, operating over the 0 to +75°C temperature range. Both provide typical power dissipation of 125 mW at an operating frequency of 80 MHz. Minimum dc fan-out of 25 for each output is guaranteed!

Available in the 14-pin Unibloc* plastic package, these circuits bring to 27 the total number of MECL II functional elements – in the fastest, most flexible logic line available. All are fully compatible with the MECL 300/350 series; and, have the same logic levels and power supply requirements as the coming, ultra-high-speed MECL III line.

For data sheets and application notes, circle the reader service number or write to us on your company letterhead.

*Trademark of Motorola Inc.

MOTOROLA Semiconductors
-where the priceless ingredient is care!

MOTOROLA SEMICONDUCTOR PRODUCTS INC. / P. O. BOX 955 / PHOENIX, ARIZONA 85001

CIRCLE NO. 21 ON INQUIRY CARD

I, Digital, take thee, Analog...

We'll give it five years.

That's a long, happy life for a hybrid computer.

We've performed more digital-analog marriages than anybody. So many that we're able to guarantee them.

We will join an SDS digital computer to any brand of analog and guarantee to the user that the system will work and that he will know how to run it before we leave the hybrid alone in its new home.

We've hybridized all the leading brands of analogs, we've solved the interface problems, we've developed reams of hybrid software, and we make the fastest, most versatile and economical digital computers for hybrid applications.

We support analog computer manufacturers in the design and installation of hybrid systems, and we install SDS digital computers in simulation laboratories which already have analog computers, providing interface equipment, software, and system integration.

The simulation community is a small one, but it plays a vital role in science, aerospace, and the process industries. Our people are active members of this community, helping to advance the hybrid and digital state of the art.

They're also licensed to perform marriages, so if you have a lonesome analog...

SDS

Scientific Data Systems, Santa Monica, California

CIRCLE NO. 22 ON INQUIRY CARD

Why do AMI's MOS arrays travel with NASA?

High reliability is the reason.

When you send a system aloft, there are no repair men in space. You make it or break it on reliability. That's why NASA moved into the forefront of MOS applications. And, that's why NASA is using AMI's 3-Input NAND Gate and 3-Input NOR Gate for space flight. The case for reliability is plain: ask any AMI representative or distributor for a copy of our life test data on these NASA parts.

The case for reliability on down-to-earth systems is just as plain: the same type parts that NASA sends out of this world pay off in PFM telemetry, count-down chains, and analog commutators. Beyond that, AMI's complete line of MOS building blocks offers you the greatest low-cost versatility in integrated microelectronics today, including capacity to interface with bi-polar devices. Wait and see? Why? Application data, available on request, opens new opportunities in systems design.

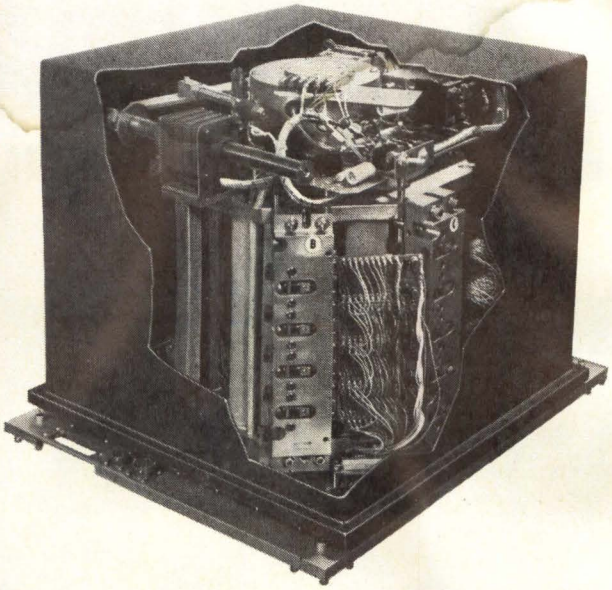
HI REL MOS ARRAYS	
Part Nos.	
L103G	3-Input NAND Gate
L203G	3-Input NOR Gate
B002E	Binary Element
BG002	Gated 2-Stage Binary
B2002	2-Stage Binary
R0002	2-Stage Shift Register
R0008	8-Stage Shift Register
L4SSG	Stream Select Gate

American Micro-systems, Inc.
3800 Homestead Road, Santa Clara, California 95051 (408) 246-0330

CIRCLE NO. 23 ON INQUIRY CARD

DRUMS • MODULES • SYSTEMS

A Page from the Vermont Research MEMORY FACT BOOK



Fact:

Computer Downtime Can Be Reduced

● Are your peripherals as reliable as your computer? VRC's drum memories are. Design life is 100,000 hours of operation . . . MTBF is 15,000 hours . . . error rate is 1 in 10^{13} bits. And these are just the standards to which all VRC drums are built.

Take our new 116CP, for example. It packs more than 16,000,000 bits on a 10-inch diameter, nickel-cobalt plated drum. The shock-mounted, hermetically sealed enclosure locks out dust, dirt, and fumes. This drum operates dependably at 0°C . . . at 45°C . . . at 100% humidity. For rugged application, this compact, 17¾" square x 20" high unit offers proven, lasting reliability.

There's really no secret behind VRC product reliability. Just a great deal of solid experience in dependable, standard modular design. Like standard track head pads connected to standard rotary actuators connected to standard polynoids. With simple, standard adjustments for peaking head pads . . . standard, top grade bearings . . . standard electronics . . . and standard failsafe features in event of power failure.

And if the 116CP won't fit your particular needs, another VRC drum or system will . . . using the same standard, reliable, modular approach. You'll find more details in our standard, reliable, modular new brochure.

See reliability in action at our booth #155 at FJCC

Computers are known by their MEMORIES

. . . so is

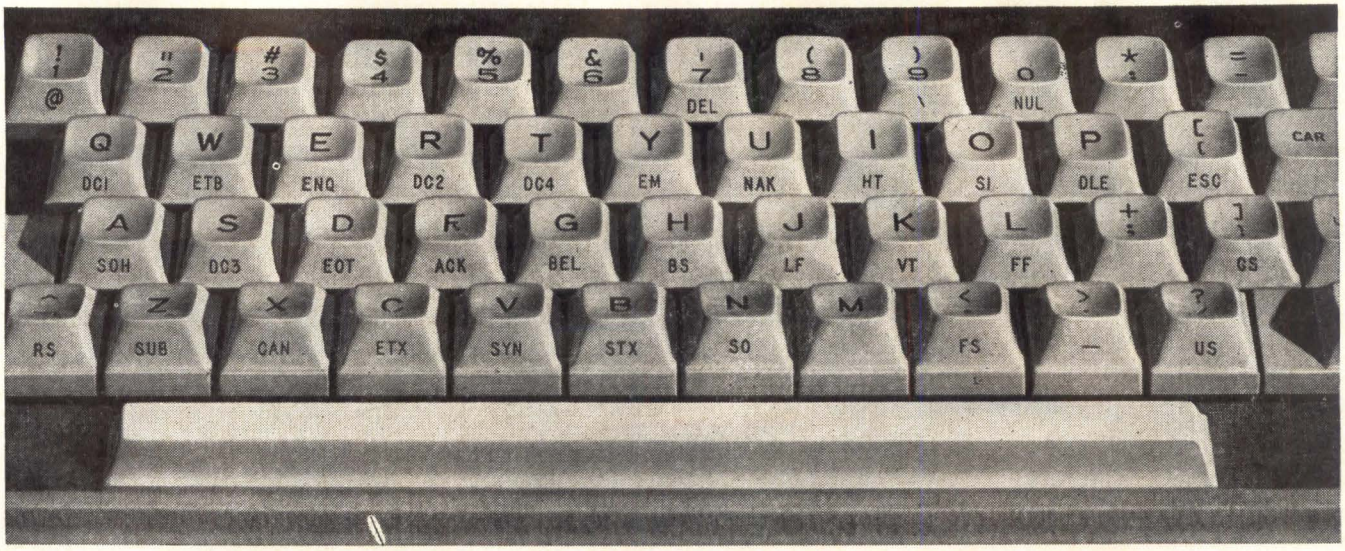
Vermont Research CORPORATION

Box 20a • Precision Park • North Springfield • Vermont

Who will help conceive, engineer, manufacture and market VRC's future memory products? You? Get the facts on openings, advancement opportunities and the many rewards of North Country living from:
RICHARD A. STOVER
Vice-President, Engineering

CIRCLE NO. 24 ON INQUIRY CARD

USASCII spoken here.



So here is the one terminal now available that can begin to match the input-output potential of a modern computer: the new 7100 Conversational Mode Terminal by Friden.

The 7100 has the same, easy-to-use keyboard as an electric typewriter. But with one major addition.

The USASCII code!

USASCII puts 128 characters at your command. You can use them to write your own computer program. And when you're done, the 7100 neatly prints out your program for later use — saving costly computer storage.

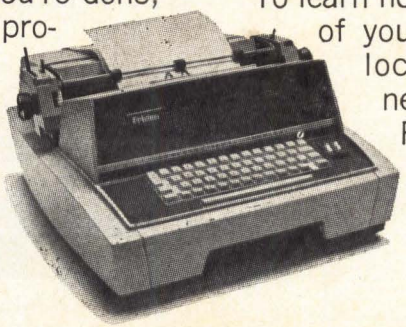
Nice? Just the beginning.

The 7100 is the only USASCII terminal with upper and lower case. The only terminal with a 13" writing line. And the only terminal that will reproduce a facsimile of all USASCII codes (except space and carriage return).

It even has a color shift. When you talk to the computer, it prints in red. When the computer talks to you, it prints in black.

The 7100 brings new ease and efficiency to time-sharing, on-line programming, information retrieval, and documentation.

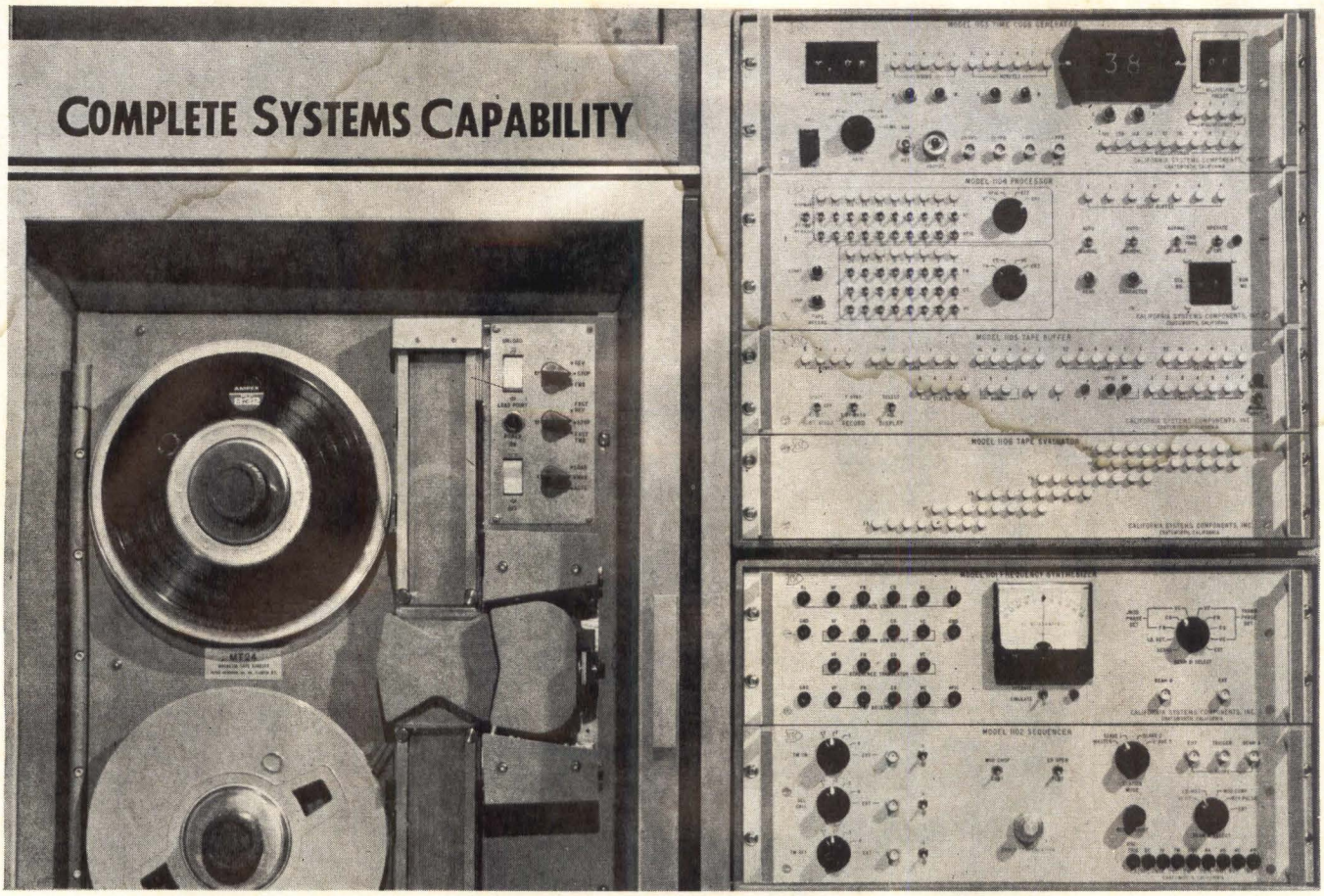
To learn how easily it can let any corner of your company use a centrally located computer, call your nearest Friden office. Or write Friden, Inc., San Leandro, California 94577. Sales and service throughout the world.



Friden
DIVISION OF SINGER
DIVERSIFIED · WORLDWIDE

CIRCLE NO. 25 ON INQUIRY CARD

Reader's Choice



CALIFORNIA SYSTEMS COMPONENTS HAS PRODUCED THE WORLDS MOST ACCURATE MINIATURIZED GEODETIC SURVEYING SYSTEM

The SECOR system can measure distances up to 800 miles to an accuracy of 9" without requiring line of sight between the points. SECOR, as other sophisticated military and industrial systems use CSC off the shelf Integrated Circuit Digital Logic and Analog Cards.

ANALOG AND DIGITAL INTEGRATED CIRCUIT LOGIC CARDS • A/D & D/A CONVERTERS • POWER SUPPLIES • MOUNTING HARDWARE

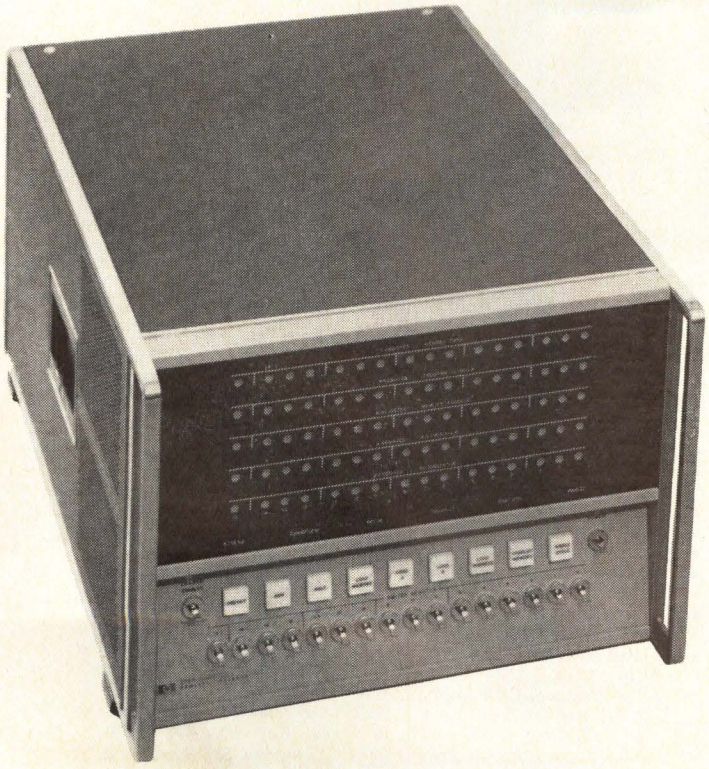
For information on IC logic for your next system write to:

CALIFORNIA SYSTEMS COMPONENTS, INC.

9176 INDEPENDENCE AVENUE • CHATSWORTH, CALIFORNIA 91311 • (213) 341-1050

CIRCLE NO. 27 ON INQUIRY CARD

the new name in high-performance, low-priced computers



This new computer is the easiest to program and interface of all high-speed computers. It has 16-bit words, 4K expandable memory, 2 microsecond cycle time, plug-in I/O cards, multichannel priority interrupt, relocatable software and both FORTRAN and ALGOL compilers. Plug-in options including direct memory access and hardware multiply and divide are available. Peripherals such as high-speed disc memory and magnetic tape are standard. The price, with 4K memory and ASR-33 teletype: $16,500.

To find out how easy the 2115A is to use—and its big brother, the 2116A, write to Hewlett-Packard, Palo Alto, California 94304; Europe: 54 Route des Acacias, Geneva.

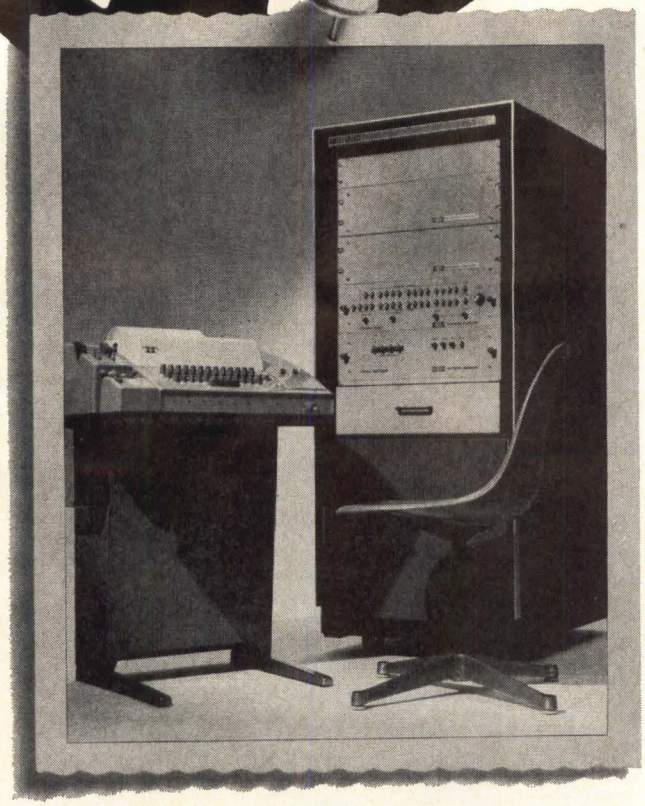
06714

HEWLETT hp PACKARD

SEE HP COMPUTERS AT BOOTHS 705-707 FALL JOINT COMPUTER CONFERENCE

CIRCLE NO. 28 ON INQUIRY CARD

Price & Power



The new Raytheon 703 IC systems computer—$15K.

RAYTHEON

Raytheon Computer is expanding its data systems product line of Integrated Circuit modules, multiplexers and conversion equipment with a new low-cost 16-bit IC digital computer. The 703 is designed to replace core buffers and special logic as the central element in data acquisition, processing and control systems.

FOR $15,000, YOU GET:

- ASR 33 with paper-tape reader and punch
- 16-bit word length
- 2's complement arithmetic
- 71 hardware instructions
- Direct and indexed addressing
- 4K memory
- Byte and word addressing
- Byte manipulation
- Register entry and display control panel
- Programmed word transfer via 16-bit I/O bus
- 2 μsec cycle time
- software-diagnostics, assembler and executive routine

YOU CAN HAVE:

- Up to 32K memory
- Direct memory access channel
- High-speed hardware multiply/divide
- Real time clock
- Peripherals including mag tape, disk and Raytheon Computer's exclusive Multiverter®.

WE WILL SEND YOU FREE:
Bulletin SP-244 with all you need to know. Raytheon Computer, 2700 S. Fairview St., Santa Ana, Calif. 92704. (714) 546-7160.

SEE THE 703 AT FJCC BOOTHS 601-604

CIRCLE NO. 29 ON INQUIRY CARD

CIRCLE NO. 30 ON INQUIRY CARD →

6 new off-beat 2½ D stacks.

1 HEATED STACK— Built for a process control application, this has an extremely large bit length. (16K x 25 bits). Heaters keep the temperature a constant 55°C ±3°C; but the whole stack with heaters and large capacity only takes up 750 cubic inches.

2 FOLDED STACK — We've built hundreds of these for SDS computers over the past year. With a 4K x 9 bit capacity, the stack uses our 20 mil cores, and turns out a cycle time of 830 nanoseconds.

3 HIGH/LOW TEMP STACK— This 8K x 18 bit 2½ D, built for RCA, uses our special lithium cores. They have a low temperature coefficient and excellent stability over a 10°C to 55°C range. The beauty of this is that the customer doesn't have to bother with temperature compensation.

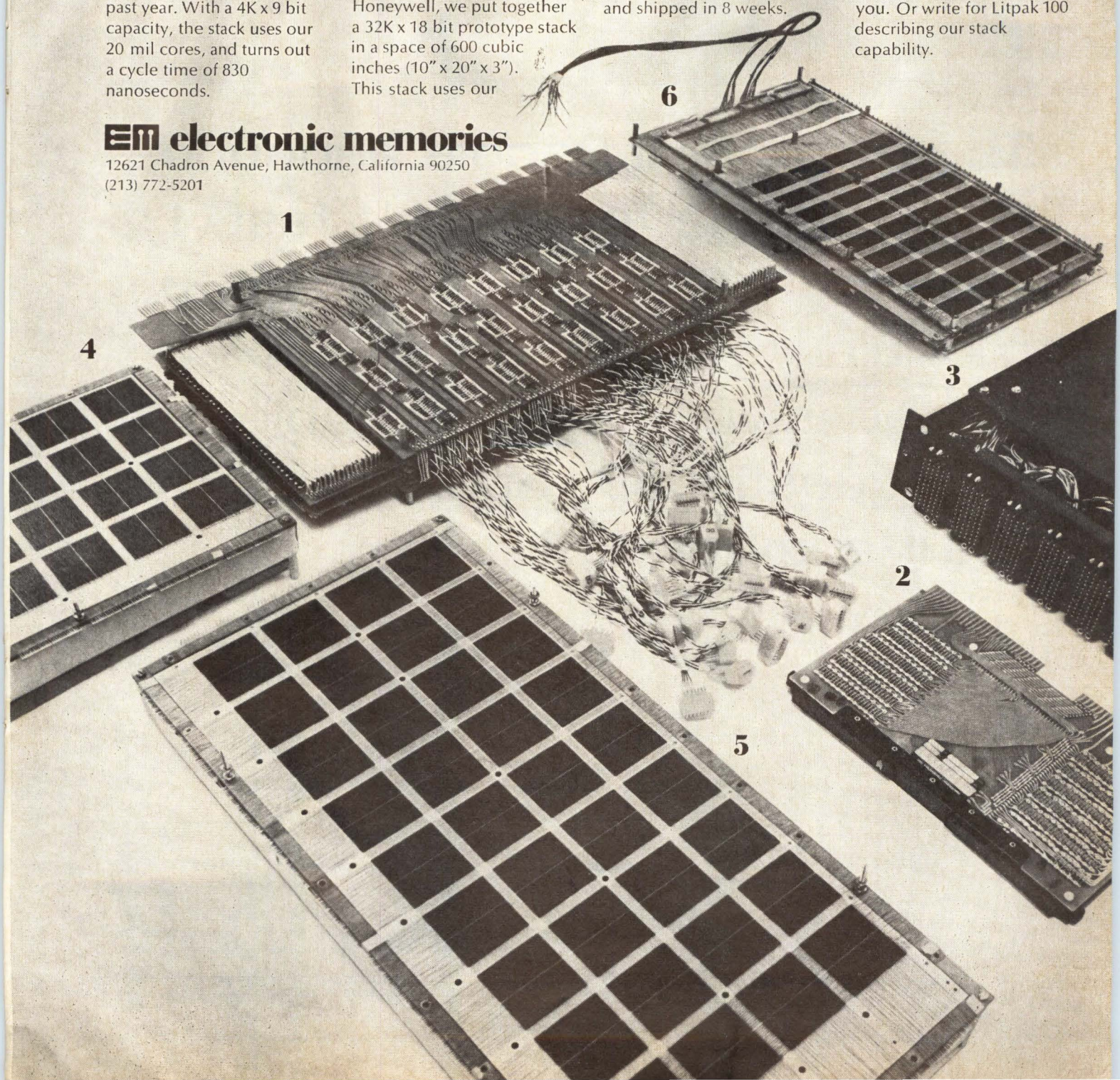
4 COMPACT STACK WITH LARGE CAPACITY— For Honeywell, we put together a 32K x 18 bit prototype stack in a space of 600 cubic inches (10" x 20" x 3"). This stack uses our 20 mil cores and has a cycle time of less than 650 nanoseconds.

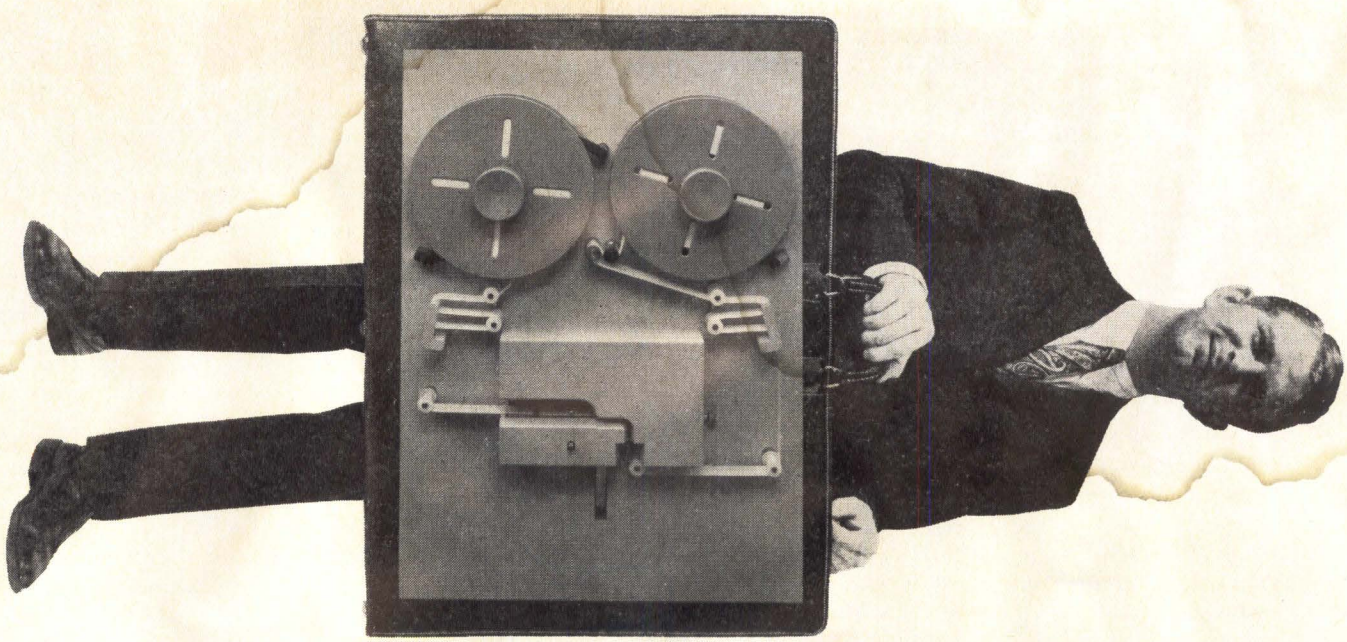
5 SPLIT MODULE STACK— This was a tricky one for Raytheon. It was a special 16K x 18 bit stack, and two sets of diode modules in the word direction had to be placed on each side of the stack. (Usually, they're all on one side.) The whole stack was designed, built, and shipped in 8 weeks.

6 NANOSTACK™— We use this one in our large capacity NANOMEMORY system, but we've also been making a modified version for over a year and a half for Digital Equipment Corp. The stack has an 8K x 18 bit capacity and measures only 10½" x 20½" x 2".

If your 2½ D requirements are off-beat, call us, and we will see what we can do for you. Or write for Litpak 100 describing our stack capability.

EM electronic memories
12621 Chadron Avenue, Hawthorne, California 90250
(213) 772-5201





The Peripheral People announce a 200 cps perforator. It's fast (1) reliable (2) easy to maintain (3) modular (4) accurate (5) inexpensive (6) and available (7). Any questions? Speak, demand, we'll answer (8).

(1) Asynchronous. (2) So good, we use it ourselves. NCR knows electro-mechanics. (3) Two moving parts per punch channel. No moving parts when unit is on but not punching. (4) Available in three sections: perforator, media handler, electronics with validity check. (5) Validity rather than parity check inhibits media movement and will not punch if power is lost. (6) Lowest cost, most reliable high performance perforator on the market. (7) From three to six months. After August, two to four months. (8) Macbeth, Act IV, Scene 1.

NCR®

THE PERIPHERAL PEOPLE

Card Readers, Tape Punches, Tape Readers, Printers, MICR Readers, CRAM (Card Random Access Memory)

THE NATIONAL CASH REGISTER COMPANY • INDUSTRIAL PRODUCTS DIVISION • DAYTON, OHIO 45409

CIRCLE NO. 31 ON INQUIRY CARD

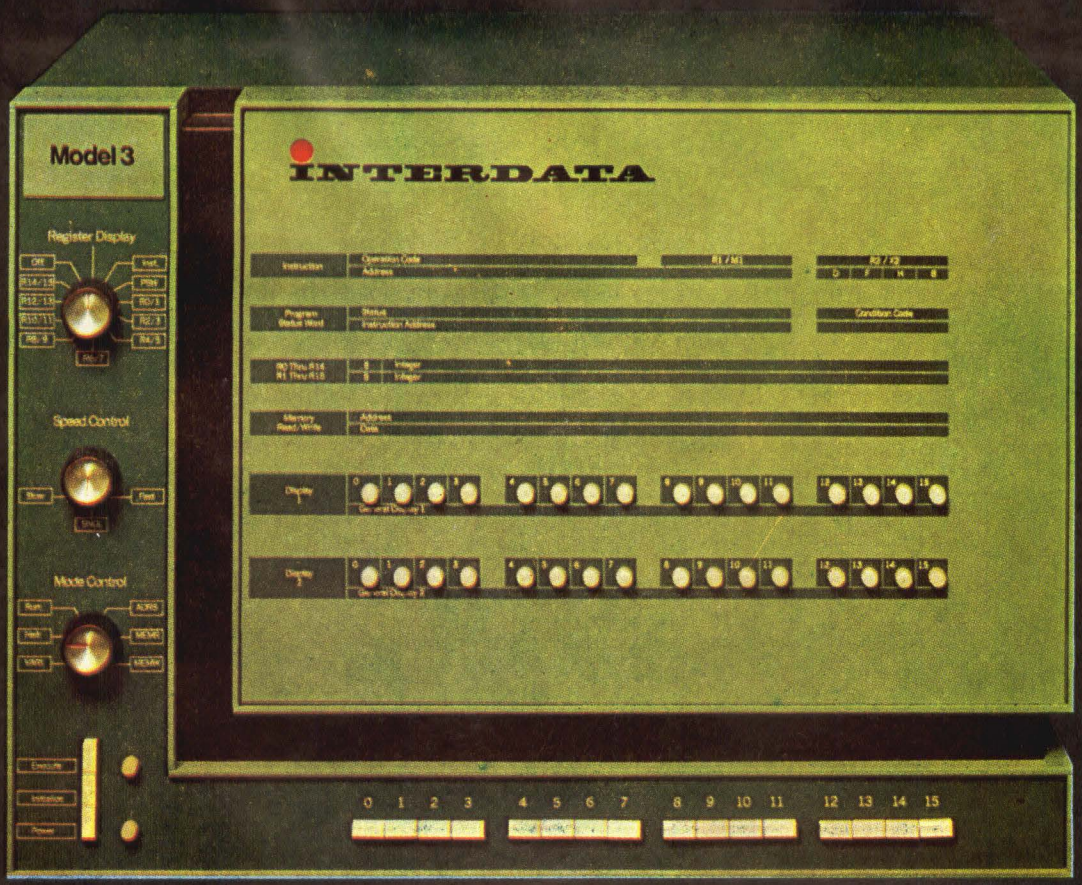
A communications computer for $6,000. The Interdata Model 3.

The Interdata Model 3 digital computer has unique firmware capability for multi-unit low speed data concentration with simultaneous high speed processor-to-processor transfer.

16 and 32-bit instruction word length.

Modular structure with integrated circuits.

1024 8-bit bytes (expandable to 65,536) all directly addressable. Fast cycle time of 2.0 microseconds.



Powerful instruction repertoire with register-to-register and register-to-indexed memory operations.

16-bit arithmetic and 16 general registers to simplify programming.

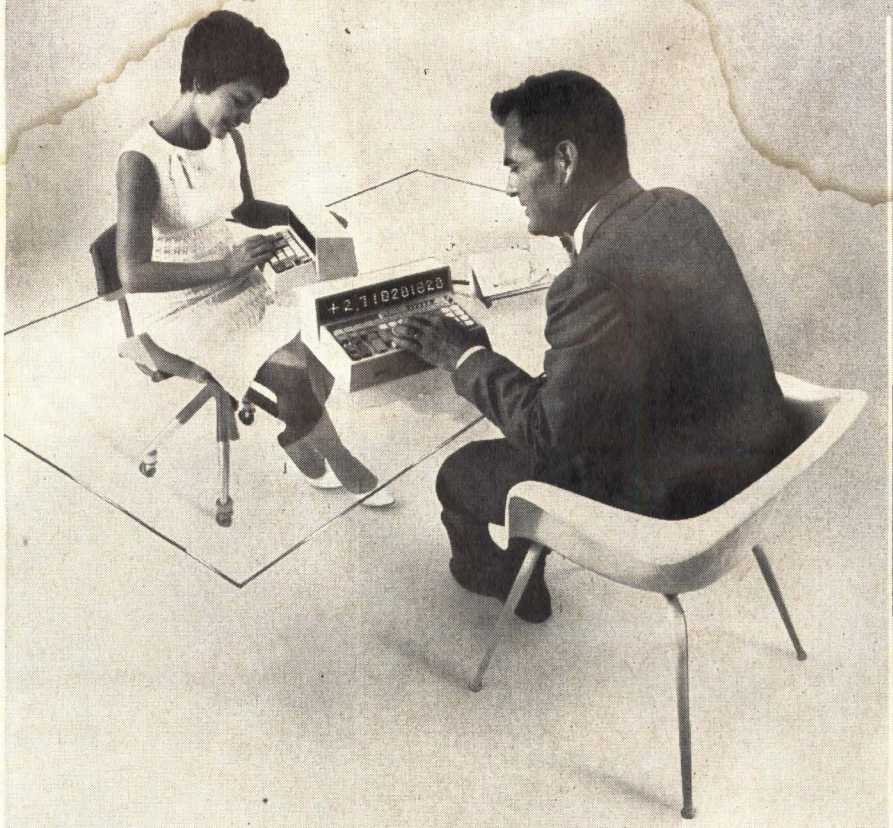
Software system includes assembler and debugging package.

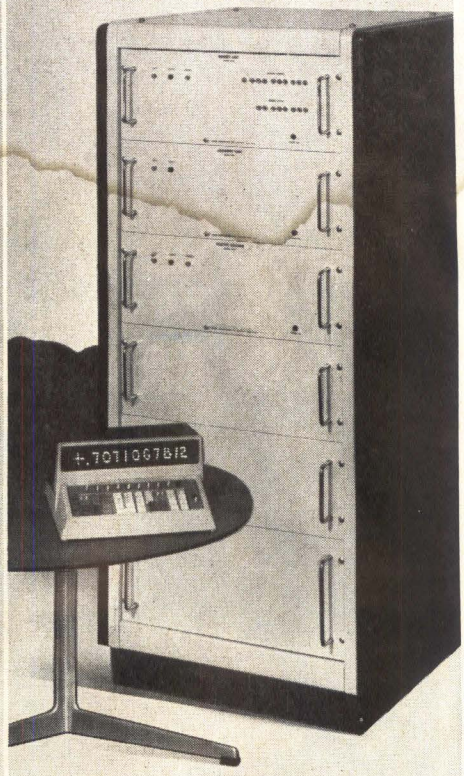
Write for details: Interdata, 2 Crescent Place, Oceanport, N.J. 07757 (201) 229-4040

FJCC BOOTH 130

CIRCLE NO. 32 ON INQUIRY CARD

NUMBER 1
IN NUMBERS





Wang products tend to be friendly.. ..but calculating

Take our Series 300 calculator . . .

It's small, quick, quiet and very easy to get along with. You'd never guess, till you get to know it, that inside this trim little keyboard console lurks the most versatile, most advanced electronic desk-top calculating capability ever developed. Among other things, these vital statistics:

- Petite keyboard and large display
- Silent, fast, and easy to use
- Maximum economy — 4 keyboards can share the cost of 1 "brain"
- 2 adders, and 2 more registers for each keyboard
- Automatic invoice extensions and line counts
- Special keys for Log_eX, e^X, $\sqrt{X}$, and X^2, SIN (θ), COS (θ), ARCSIN (X) and ARCTAN (X)

. . then there's the brand new Series 370 programmable calculator

Although it looks like its little Series 300 brother, this new, absolutely unique instrument can do things no other electronic calculator in the world can handle.

- Attaches to the 300 Series
- Same calculating keys
- Program capacity from 80 steps up
- Only 8½" page printed output on a calculator
- Complete programming features including decisions and loops
- Extensive program library
- Additional data storage up to 64 registers (with 10 digits, decimal point and sign)
- Communication with telephone lines and data acquisition equipment
- Fully programmable for long or iterative calculations

. . . and while you're here, meet the Series 4000 on-line data system

Actually a series of compatible "black-box" data modules, this unusual "system" can be custom-assembled, at low cost and virtually on a plug-in basis, to handle any of a broad variety of on-line data acquisition and reduction tasks.

- Completely modular for versatility and expandability
- Fully programmable multiple inputs and outputs
- Data and program storage in modules of 1024 — 10 digit numbers plus decimal point and sign
- Economy of calculator with power of computer

When your calculations are beyond an adding machine and below a computer, call

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LABORATORIES, INC

DEPARTMENT CA-10. 836 NORTH STREET. TEWKSBURY. MASSACHUSETTS 01876 — TELEPHONE: (617) 851-7311

CIRCLE NO. 33 ON INQUIRY CARD

Contemporary Electronics is one of the largest producers of computer pulse transformers in the U.S.

SO?

So, maybe you're missing a bet if you haven't checked Contemporary Electronics for *quality, service* and *price.*

Contemporary Electronics *specializes* in pulse transformers. It's not a sideline, but a principal part of our business. Well over 100,000 pulse transformers are produced each month in 75 different designs.

Advantages? Here are some.

Technical Capability. Contemporary Electronics engineering staff knows computers and can design any special product for any application.

High Quality. Most transformers have special high quality design features. All pulse transformers are 100% inspected as many as three times before shipment. QC system meets MIL-Q-9858, and has been approved for use on the Apollo program.

Fast Sample Service. Samples, small production lots and specials are normally shipped 24 to 72 hours after receipt of request.

Interested in what can be done in terms of performance, size, delivery, or MIL-specs? Get to us—we've got lots more to tell.

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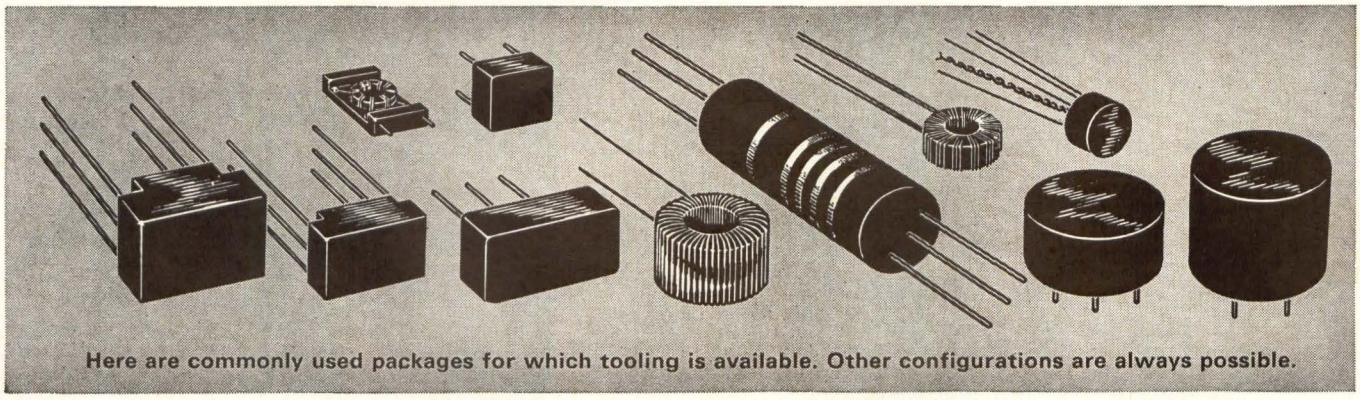

Here are commonly used packages for which tooling is available. Other configurations are always possible.

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CIRCLE NO. 34 ON INQUIRY CARD

Letters to Editor

FIBER OPTICS

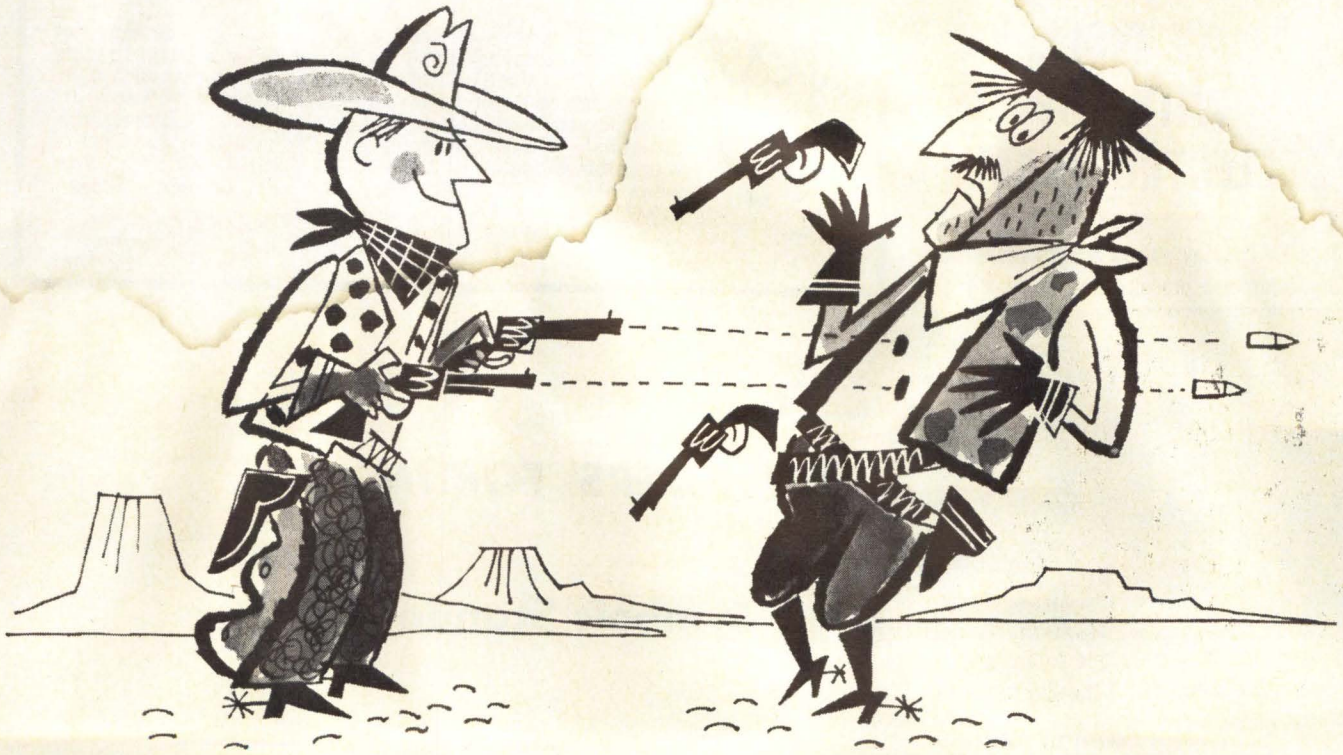
To the Editor:

I was happy to see Corning fiber optics well represented in your July coverage on Fiber Optics; an informative article of this sort is of benefit to the entire fiber optics industry. But, I was dismayed to see no mention of the most significant advance so far in flexible fiber optics technology.

The industry's first continuous length flexible fiber optics made of glass were introduced by Corning Glass Works on February 3, 1967. The flexible, non-coherent fiber optic bundles, jacketed in polyvinyl-chloride (PVC), are available in single lengths up to 10,000 feet — almost two miles. The glass fibers can be twisted and flexed without degradation of light transmission. A unique process of drawing hundreds of glass fibers simultaneously made the development economically feasible. Initial selling price is 10 cents per foot in quantities of 50,000 feet, but as volume increases, the price will fall to five cents or less per foot, depending on quantity and specifications. Continuous lengths of environmentally stable glass fibers are ideal for high volume, automated process applications. The jacketed fibers can easily be cut, terminated, end finished, and installed to light source and output devices. PVC jacketed fibers withstand sustained temperatures up to 220°F. Because glass fibers will transmit light efficiently up to 600°F, high temperature applications using other jacketing materials are possible.

The claims of the plastic fiber manufacturers that glass can't be manufactured in "almost unlimited lengths and at lower cost" are not true:

Robert B. Parker
Product Program Manager
Corning Glass Works
Corning, New York



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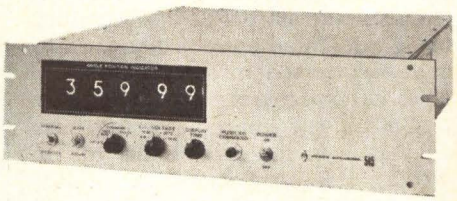

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CIRCLE NO. 36 ON INQUIRY CARD

what do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

Logic Symbols Standard

. . . "no longer a vital issue" . . .
A Statement From
The Editors Of Computer Design

In September, 1965 The Editors of Computer Design aligned themselves with those persons within our industry who deplored the lack of a generally-accepted standard for logic symbols, and offered the pages of the CD Readers' Forum for the presentation of comments, opinions, and enlightening information. We felt that a free presentation of views from concerned persons may help resolve the contest between USASI Y32.14 and MIL-STD-806B, and lead to a single generally-accepted standard.

Toward this end we have published twenty letters from interested readers; we have also published articles on MIL 806B and Y32.14, plus extracts from standards in use by IBM, Sandia, and Airborne Instrument Laboratories. We have been praised by some for our efforts; we have also been publicly and privately excoriated by some adherents of one standard who accuse us of favoring the other standard. For the benefit of the latter, we repeatedly have stated that our single purpose has been to assist in the acceptance of one standard for logic symbology, and that we have neither vested interest in, nor bias toward, the content of that standard.

We think that the following statements summarize the present status with respect to logic symbols standards.

- Most responsible people support the desirability of a single universally-accepted standard.

- Within the past three to six years, most companies have reached the point where it was imperative to adopt a logic symbol standard for company-wide use. Had there been, at that time, a single standard with the backing of the major organizations the predominant decision would probably have been to live with that standard for company purposes. The fact that there were two major competing standards forced the companies to follow one of three courses: (1) Delay a decision and thus invite company chaos; (2) Choose sides in the ASA vs. USAF quarrel by choosing Y32.14 or MIL-806B; (3) Create a company standard either based on one of

the two competing standards, or a combination thereof, or in combination with past company practices. Most companies have established a standard in one of the above two ways.

• The dispute between the two competing standards has not made any perceptible progress toward resolution in the past few years.

The most significant fact which we now face is that all of the companies who have need of a logic symbol standard have already established an internal standard because NO INDUSTRY-WIDE STANDARD EXISTED AT THE TIME WHEN IT WAS NEEDED. These companies have made a substantial investment in the design, promulgation, and implementation of their internal standards. Even in the unlikely event that the 806B/Y32.14 dispute were to be resolved, it is doubtful that this investment would be discarded and a new investment made in the universal standard.

A second important fact is that our industry and technology are advancing at a rapid pace and we are rapidly passing the point where a universal logic symbol standard is a very important issue. Logic circuitry has given way to integrated circuits which may soon give way to integrated functions or subunits: LSI. The question of how to represent an OR gate assumes less importance with each passing month. It seems likely that LSI may breed a new form of representation which will obsolete the logic symbol as we know it. IN AN INDUSTRY WHOSE LEVEL OF ACTIVITY DOUBLES EVERY FIVE YEARS, WE CANNOT AFFORD TO SPEND TEN YEARS DISCUSSING ONE RELATIVELY-MINOR PROBLEM.

The Editors of Computer Design conclude that, although a universal logic symbol standard would have been desirable, it appears that it is no longer a realizable goal, and, further, that it is no longer a major disaster that this is so. Our industry has many more interesting and important endeavors to which we can devote our time and energy than the continuation of a ten-year-old quarrel. The CD Readers' Forum continues to invite readers' comments on this subject, but we no longer consider it to be a vital issue to our industry.

from our man in Washington

Can computer technology help solve the growing demands of the information explosion — especially in the area of scientific literature which doubles in size every 8 to 10 years. The U.S. Office of Education has announced a new $3.5 million Library and Information Sciences Research Program to help libraries efficiently meet the demands of the information boon. Thirty-three projects have been approved by the Office of Education including one to Hampshire College, Amherst, Mass., for the design of a program for student use of computers and "dial access" communication systems to bring library services to dormitory rooms, and to develop a better accommodation between copyright law and information technology.

.....

Demand in the highly industrialized countries of Western Europe, Canada, and Japan remained buoyant for U.S. computers and parts, according to the Commerce Department. These exports averaged $37 million per month during the first five months of 1967 and were nearly 40 percent more than that from July to December 1966.

.....

Copyrighting computer programs is a major issue in overall copyright legislation now under consideration in the U.S. Senate. Under existing legislation it is not possible to copyright computer programs. Two doubts have been expressed about the ability to copyright computer programs. First, whether they are the "writing of an author" rather than mere mechanical operation of a methodology, process, or idea, and, second, whether punched cards or tapes, and especially magnetic tapes, can be considered as "copies" for the purpose of registration. Another basic problem, and an even more sharply-contested one, is the extent to which uses of copyright material of all sorts in computers should require permission and payment. Many people think the area of computer copyright is not yet ready for detailed legislative action. Many computer manufacturers and users fear that if the general copyright bill revision is enacted in the present form, the door will be closed for future Congressional action on computers for the years to come. A group may be established by Congress soon to study the entire matter and report back to Congress as soon as possible.

.....

The risks and dangers of relying too heavily on computer analysis in defense and foreign policy matters are being investigated by the Senate National Security and International Operations Subcommittee under the Chairmanship of Senator Henry M. Jackson (D. Wash.). The group will hold closed-door hearings on the wisdom of using advanced analytical techniques throughout the Government in place of human experience and intuition.

.....

A Joint Congressional Subcommittee on Economic Statistics has called for the development of a National Data Center by the Budget Bureau to serve as a clearinghouse for government statistics. The Congressional group concluded that further integration of Government statistics "can and should be attained without sacrificing principles of personal privacy. Modern technological capabilities for data association, storage, and retrieval, like most technological changes, present new possibilities for use and misuse. The rational approach to these new capabilities is not fear to act, but

DC Output continued on page 38

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Data 620/i was designed from scratch as a powerful systems computer. That's why it so efficiently solves problems previously considered too difficult or expensive for computer solution. Data 620/i has a bigger instruction set, one-half the components, and costs less than any computer in its class.

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DC Output *continued from page 36*

rather action to control technology for man's use." From this standpoint, the Congressional report concludes, the problem of safeguarding privacy should be treated seriously. The data center would force a more explicit consideration of pressing issues of our electronic age, the Subcommitte concludes.

Recent Government Contracts

BENDIX CORP., Teterboro, N. J., has received a $3,636,600 firm, fixed-price contract for modification of airborne computers. Work will be done at Wilkes-Barre, Penn. The Oklahoma City Air Material Area, Tinker AFB, Okla., is awarding the contract.

SYSTEMS DEVELOPMENT CORP., Santa Monica, Calif., has been awarded a $14,389,265 cost-plus-incentive fee contract for computer program updating and preparation of system training programs. The contract is being awarded by the Sacramento Air Material Area (Air Force Logistics Command), McClellan AFB, Calif., following competition in which 33 bids were solicited and four were received.

HONEYWELL, Cambridge, Mass., has been awarded a contract by the Naval Ordnance Systems Command to lease 15 computers (10 H1200's and 5 H2200's) for the Naval Ordnance management system.

WESTINGHOUSE ELECTRIC CORP., Pittsburgh, Pa., has been given a $27,933 contract by the Atomic Energy Commission's New York Operations Office for a computer development program.

DIGITAL EQUIPMENT CORP., Maynard, Mass., has been awarded a $46,200 contract for an on-line computer by the San Francisco Operations Office of the Atomic Energy Commission.

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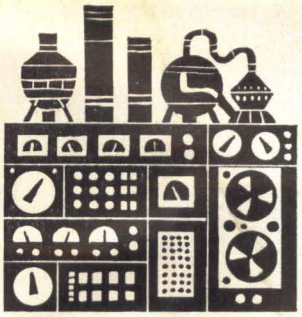

INDUSTRY NEWS

PITNEY-BOWES, INC., ANNOUNCED THAT IT IS ENTERING THE FLUIDICS FIELD WITH FIVE NEW COMPONENTS, INCLUDING A "FLOWBOARD" WHICH IT CALLS "A SIGNIFICANT BREAKTHROUGH IN FLUID LOGIC CONTROLS." Fluidics is a new market for Pitney-Bowes, the company which originated the metered mail system and which up to now has been exclusively a business machines manufacturer.

The Flowboard, on which patents are pending, is "The simplest and least time-consuming device now known for setting up digital circuit applications," according to Fred T. Allen, PB's executive vice president for products.

"This unique device thus saves substantial technical and engineering time, both in breadboarding and in production."

The Flowboard is the result of five years of research into fluidics by Pitney-Bowes, which has successfully tested it in actual applications. The standard Flowboard, which has 22 fluidic amplifiers, can be easily and quickly programmed to meet most control needs. Integrated Flowboards, without external intraconnections, can also be designed by PB to meet special needs.

Along with the new Flowboard, Pitney-Bowes is offering connectors, a filter, an air pulse generator without moving parts, and a self-contained control unit, the F-132, which contains 132 fluidic amplifiers, a filter, a regulator and a pressure indicator.

In the near future, the company will also offer input sensors and output transducers (converters) so as to provide complete systems compatibility.

SCIENTIFIC DATA SYSTEMS WILL ESTABLISH A TIME SHARING SERVICE CENTER USING AN SDS 940 COMPUTER at its El Segundo facility this Fall. The center will be used by SDS programmers and system development engineers as well as by subscribers at other local companies. The primary objective of the center is to increase the company's experience in the use of SDS 940's for time sharing service center operations. SDS has no plans to establish additional company-owned centers. The El Segundo center will be established to provide the company with the actual experience needed to increase the efficiency and reliability of time sharing hardware and software provided to 940 customers. Because the SDS service center will devote more than half the available computer capacity to SDS personnel, and because it will be available to outside subscribers only during limited time periods, it is not expected to compete directly with other SDS 940 time sharing centers.

A SYSTEM WHICH WILL ALLOW A COMPUTER TO RECOGNIZE HAND-PRINTED CHARACTERS IS BEING DESIGNED by System Development Corporation, Santa Monica, California. The system is being developed through funding provided by the National Aeronautics and Space Administration (NASA) and the Advanced Research Projects Agency (ARPA) of the Department of Defense. The goal of the project is to permit a computer user to communicate with a computer in a form he is most familiar—his own written characters, letters, and symbols.

When operational, the user will draw a character on the surface of a graphic input device (such as a RAND tablet or a GRAFACON 1010A) connected on-line to a time-shared computer. A recognizer program will identify the character as an "A," a "9," or the Greek symbol for pi, for example.

Working on the assumption that no one writes a character the same way twice, the program will have sufficient flexibility built into it to recognize later versions of the same character.

According to Morton I. Bernstein, a computer systems specialist and head of the research project, the program being developed "will provide the means of creating the kind of computer support that mathematicians and scientists have been requesting for years—to have the computer perform the time-consuming, straightforward manipulation of equations presented to both the computer and the user in their most natural form." The system is being designed to function in real-time, either under time-sharing or a stand-alone computer environment. SDC, an independent not-for-profit corp., specializes in design and development of information systems.

Production rates of interconnect components, such as computer back-planes and printed circuits, are out-stripping the ability to inspect them using long-established methods. Mechanical fixtures, providing a quick-access to all tested nodes, coupled with the highest-speed wiring analyzers available, are shown to be the best answer yet to this problem.

RAPID VALIDATION

PRICE WICKERSHAM,
V. P., Engineering,
Brooks Research & Mfg., Inc.,
Kansas City, Missouri

Computers, data acquisition systems, and other digital electronic machines involve a wide variety of interconnect subsystems, ranging from small printed circuit boards to large logic wiring matrices or back-planes. A single-sided PC board can have 50-500 terminations, a multilayer board 300-10,000 terminations, and a logic back-plane 1,000-20,000 terminations. The probability of wiring errors existing in these assemblies is far from being insignificant and is a major problem in the manufacture of digital systems.

In fabricating these assemblies, manufacturers have attempted to automate their processes as much as possible. This effort is aimed at two principal objectives, both of which have an ultimate cost reduction target:

- Improvement in quality through reduction in wiring errors
- Increase in volume at the same or lower unit costs.

Logic Back-Planes

The use of automatic punched-card-controlled back-plane wiring systems has done much toward reaching the above objectives, but has left a residual population of defects that must be corrected before the over-all system will function. Although card-controlled wire-wrapping machines have dramatically improved the quality of back-plane wiring in comparison to manual methods, errors due to broken wires or pins, shorted pins, or program-deck card omissions, result in error rates running 1%, 2% or even as high as 5%.

A common checking technique in the past has involved a manual point-by-point check of the wired back-plane against the wire-list, correcting errors as they are found. This is rather a time-consuming and expensive method, and it is generally recognized that a manual check of this type usually does not eliminate all errors, but merely reduces their population. The final validation of the back-plane is done at the system test level, where it is hoped that existing wiring errors will be found by functional testing.

Checkout technicians will testify to the difficulty of diagnosing back-plane wiring errors. Hours may be spent, using rather sophisticated diagnostic procedures, to locate the one source of a malfunction. Others may be found easily. In some cases, the checkout procedures may not in-

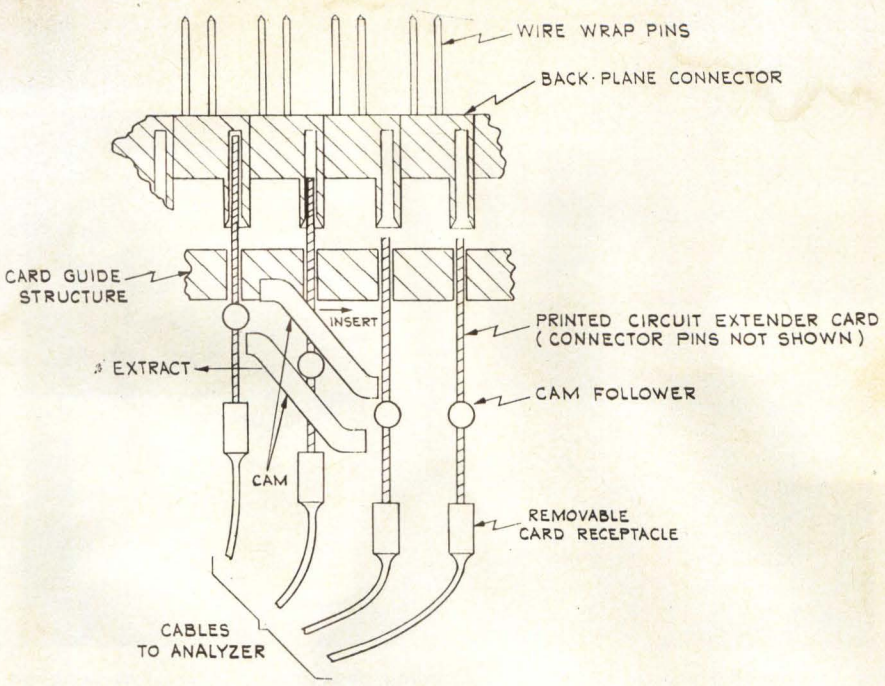

Fig. 1. Schematic of cam-card access fixture. Cam excursion is a right-left movement under control of lead screw. In multi-row fixtures, cams in each row move in synchronism.

OF INTERCONNECT SYSTEMS

dicate that a wiring error even exists, because the test may not establish a particular logic level pattern where a wiring error would produce a failure of the desired function.

This procedure has been used for a number of years. Now, under increasing pressures to ship more systems in less time, production managers are realizing the true costs and inadequacy of this type of de-bugging. Where a few years ago, one or perhaps two, automatic wire-wrapping machines could handle the throughput of a computer assembly plant, now installations of four to five machines of this type are common, with plans afoot to double or triple this level. With the de-bugging load implied by this increase in volume, automatic back-plane validation appears to be the only economic and practical answer.

Although the probability of shorted lands, open lands, or separated pads on PC boards is fairly low in a carefully-controlled fabrication operation, some reject boards are usually found. Most of these are screened out in a visual inspection process, leaving a residual of undetected, faulty boards which enter the component assembly phase. When the existence of a faulty board is detected during functional testing of the complete assembly, quite often the components assembled thereto are in jeopardy and the entire assembly is scrapped. The economics of this condition parallel that of the back-plane, i.e., there is strong justification for automatic validation of these units where the volume is sufficiently high and the repair process is impractical.

The Validation Problem

The requirements for automatically validating a wiring system are relatively simple and straightforward:

- Access — the test equipment must be given simultaneous electrical access to every node in the wiring system;
- **Continuity Resistance** — the test equipment must be capable of determining if the resistance between any two points in the wiring system is below an established maximum;
- **Insulation Resistance** — the test equipment must be capable of determining if the resistive isolation of any point or multiple-terminal group (circuit) from all other points is greater than an established minimum;
- **Insulation Error Identification** — in the event of an insulation test reject condition, the test equipment must be able to identify the particular terminals involved in this error condition;
- **Automatic Test Program** — the test equipment must be able to proceed, unattended, through a complete test sequence to provide 100%

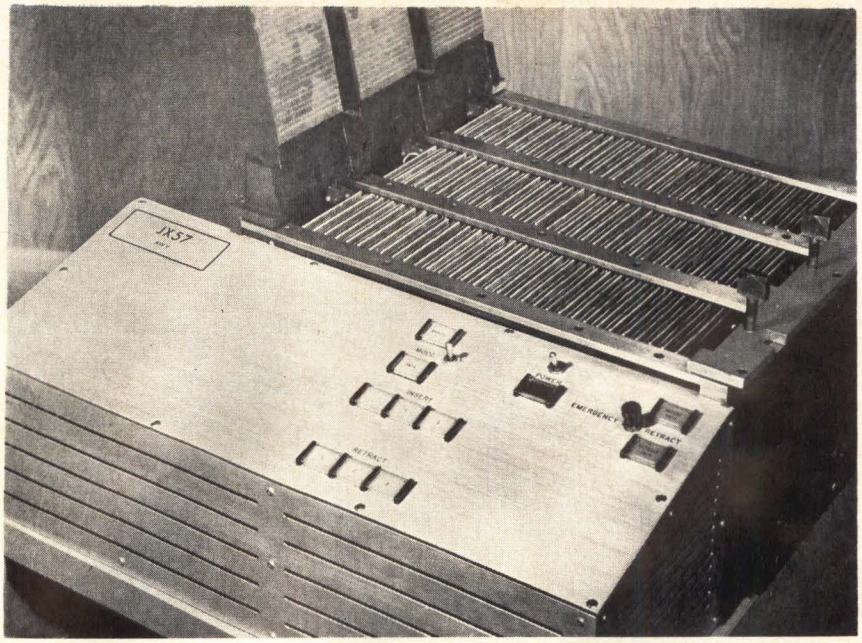

Fig. 2. Cam-card access fixture before inserting back-plane. Fixture was designed for accessing up to 3-row back-planes having up to 32 cards per row for a total of 4992 terminations.

validation of the wiring system and do so at the fastest possible test rate.

These are the general requirements for automatic proof testing of any complex interconnect system. Consideration of inductive and capacitive parameters is of concern in some instances. In addition, wired-in components of various types may be included in wiring systems. This discussion, however, is limited to validation of wiring complexes comprised of low-resistance jumper wires or printed circuit lands. Interconnect systems of this class are often termed "homogeneous." Homogeneous wiring systems can be tested with only a single pair of continuity resistance and insulation resistance limits, e.g., 5 ohms continuity maximum, 10 megohms insulation minimum.

THE ACCESS PROBLEM

For many years, cable systems have been tested automatically by a variety of commercially-available test equipments. The test equipment interfaces with the cable or harness system via a set of what are termed "adapter cables," which make connections to the receptacles or plugs of the harness being tested. With back-planes or multi-layer boards, however, electrical access to the entirety of the system wiring is not as easily made.

PC Board Access Fixtures

With a PC board, the test equipment must be connected directly to each and every circuit node in order that continuity and insulation resistance tests can be made. This requires what is usually referred to as an access fixture. Typical characteristics of access fixtures that have been designed for PC and multi-layer boards are listed below.

- **Termination Capacity** — minimum usually about 100; maximum effectively unlimited.
- **Node Contact Method** — spring-pin.
- **Spring-Pin Matrix** — spring-pins are located in a matrix on a rigid plane comprised of a suitable insulating material such as Lexan. Center distances may be as low as 0.050".
- **Spring-Pin Design** — spring-pins have a 60° conical end, gold-plated with rhodium flash. Continuity from contact-to-board is continuous and does not rely on sliding contact. Pins are designed to be push-fitted into metal sockets in the insulating matrix for ease of replacement. Pin sizes will vary depending on minimum center-to-center distance.
- **Engagement Force** — typically 1-2 oz./pins.
- **Contact Surface** — a ring is preferable between the PC board pad hole and the conical surface of the pin, although a point contact will suffice.
- **Engagement** — PC multi-layer boards may be engaged from one or both sides; engagement power is pneumatic.
- **Contact Resistance** — typically, 30 milliohms maximum.

Because of the infinite variety of possible artwork patterns, the pin matrix for PC board access fixtures is a special tooling design job. In most cases, however, the basic fixture and engagement mechanism can be designed to accommodate a number of interchangeable pin matrix assemblies. In these cases, the adapter cables are designed in two sections, one captive to the pin matrix, the other section leading to the test equipment.

Back-Plane Access Fixtures

Back-planes, usually consisting of a rectangular matrix of PC board con-

TABLE 1

CHARACTERISTICS OF WIRING ANALYZERS

Characteristic Feature	System 611 General-Purpose Analyzer	System 6120 Back-Plane/PCB Validation
Max. Termination Capacity	50,000	50,000
Max. Test Voltage	1500VAC	500VDC
Max. Test Current	2.5 amp DC	1.0 amp DC
Max. Insulation Limit	1,000 megohms	100 megohms (usually run at 5-10 megohms)
Min. Continuity Limit	1 ohm	1 ohm
Continuity/Insulation Test Rate (tests/minute)	400/300	3000/2400

nectors, present a somewhat different problem. Adapter cables between the test equipment and the back-plane can be provided with the back-plane end of these cables having a plug for each back-plane receptacle. However, the task of manually plugging all these cables into a back-plane of the usually-encountered size is impractically long and subject to error. To bypass this problem, a machine-aided access to all points of a back-plane must be provided. Back-plane access fixtures are available in two types:

- **Cam-Card Type** — access is made on the connector side of the back-plane;
- **Spring-Pin Type** — access is made on the wiring side of the back-plane.

The cam-card fixture technique is shown in the mechanical schematic of Fig. 1. Fig. 2 is a photograph of a cam-card fixture designed for accessing 1-, 2-, or 3-row back-planes having up to 32 receptacles per row, before insertion of the back-plane. Hinged swing-clamps (upper left, Fig. 2) come down over the back-plane providing resistance to the upward engagement force. Fig. 3 shows a back-plane (un-wired) in position on the fixture before clamping; wire-wrap pins up, connectors down.

Each row in the fixture has a horizontally-driven cam (see Fig. 1), which causes PC board extender cards, located in the fixture, to engage sequentially (left-to-right cam motion) or disengage (right to left) with the receptacles of the back-plane. The engagement occurs at a rate of about 0.6 second per card, taking nearly 20 seconds to engage the back-plane of Fig. 3. Adapter cables to the test equipment are plug-connected to each cam card. The cam-card design is usually symmetrical so they may be inverted to compensate for long-term wear effects, if necessary. Fixtures of this type have been built in several sizes up to 13,000 terminations, with no practical limit inhibiting the design size. The fixture is adaptable to a wide variety of back-planes of the same "family", i.e., back-planes having common connector types, inter-row, and interconnector spacings. This is often the case in any particular installation such as a computer assembly plant where back-planes are of varying sizes having a

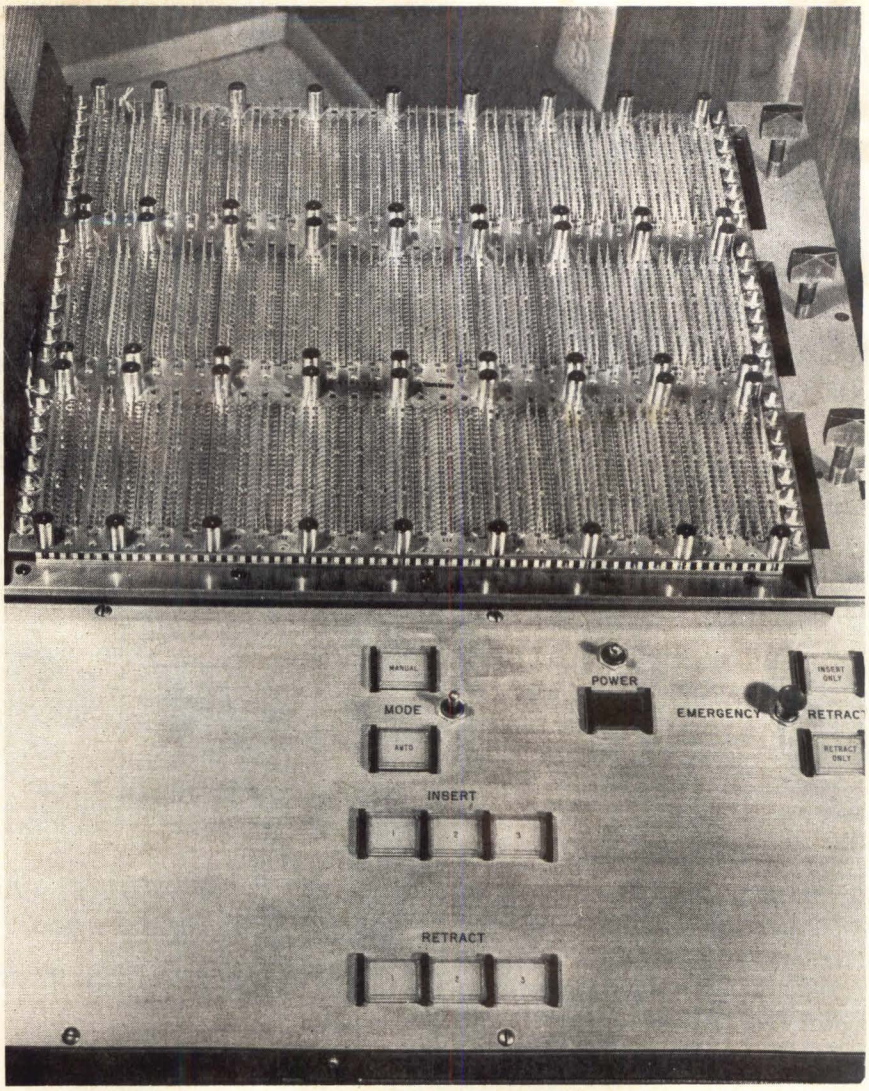

Fig. 3. Cam-card access fixture with back-plane located in position, unclamped.

common mechanical design configuration. There is one major restriction to the use of cam-card fixtures: the back-planes to be accessed must be uniform and all connectors must be identical and on constant center-to-center spacings.

Cam-card access fixtures are considered to be more economical and reliable than spring-pin types, but cannot be used where non-uniform back-planes are to be tested. Non-uniform back-planes are characterized by inclusion of receptacles in each row that vary in type along the row. The design of a family of back-planes in this category usually respects the wire-wrapping machine requirement that wire-wrapping pins appear on definite grid coordinates, but on the other side the receptacles may differ along any row.

With back-planes of this type, it is almost mandatory that contact be made to each pin on the wiring side. Fig. 4 is a photograph of a 6-row spring-pin fixture of 16,000 termination capacity. A 1-row back-plane is shown in a partially-inserted position, connectors down, wire-wrapping pins up. When the back-plane to be tested is translated fully into the fixture and located properly on a supporting bed, the bed carrying the back-plane raises by screw-jack action. Each wire-wrapping pin then engages with a mating 60° conical-socket spring-pin. In this particular fixture, 16,000 spring-pins are located in a fixed-position, horizontal matrix, comprised of six separate row assemblies. Fig. 5 shows a side view of one of these rows with a back-plane (bottom) engaged with the spring-pins (top). Each spring-pin (see Fig. 6) is a removable assembly; removal of the spring-pin does not require the associated ma-

trix termination to be unwired. Engagement force is approximately 3 oz./pin, or 3,000 lbs. total for the fixture when loaded with a maximum-sized back-plane. Maximum contact resistance is typically 25 milliohms.

Due to occasional rough handling of wired back-planes in a production operation, or because of wire bulk build-up, the wire wrapping pins are often bent away from their nominal centerline location. This particular fixture will make reliable contact to bent pins up to a total displacement from nominal of ±0.070". This degree of bend is detectable by eye and is usually corrected before inserting the back-plane for engagement.

Test Equipment System

Fixtures of the types described above permit suitable electrical access to all terminals of the interconnect system to be tested, for use by a test system designed specifically for the validation of homogeneous wiring systems. The term "wiring analyzer" has been applied to test systems of this type, although in fact, no analysis in the usual sense is done. An appropriate but more unwieldy term is "program-sequenced resistance comparator". We will use the term "wiring analyzer", since it is probably more familiar to most readers. Equipment of this type has been commercially available for some 11 years, and has principally been applied to the validation of a wide variety of cable and harness systems, frequently having wired-in components. In a typical present-day installation, a wiring analyzer may be applied to the test of many different kinds of wiring systems. For these applications, the emphasis has been on flexibility, with test parameters (voltage, current, dwell, limits, etc.) usually programmed via punched tape. These test parameters will vary considerably in the test sequence for a particular wiring system.

Wiring analyzers intended for these applications might be classified as general purpose, where flexibility of application is emphasized, and test speed is secondary. General-purpose wiring analyzers exhibit test rates ranging from about 100 to 600 tests per minute, even slower if extensive insulation test dwell intervals are programmed. These relatively-

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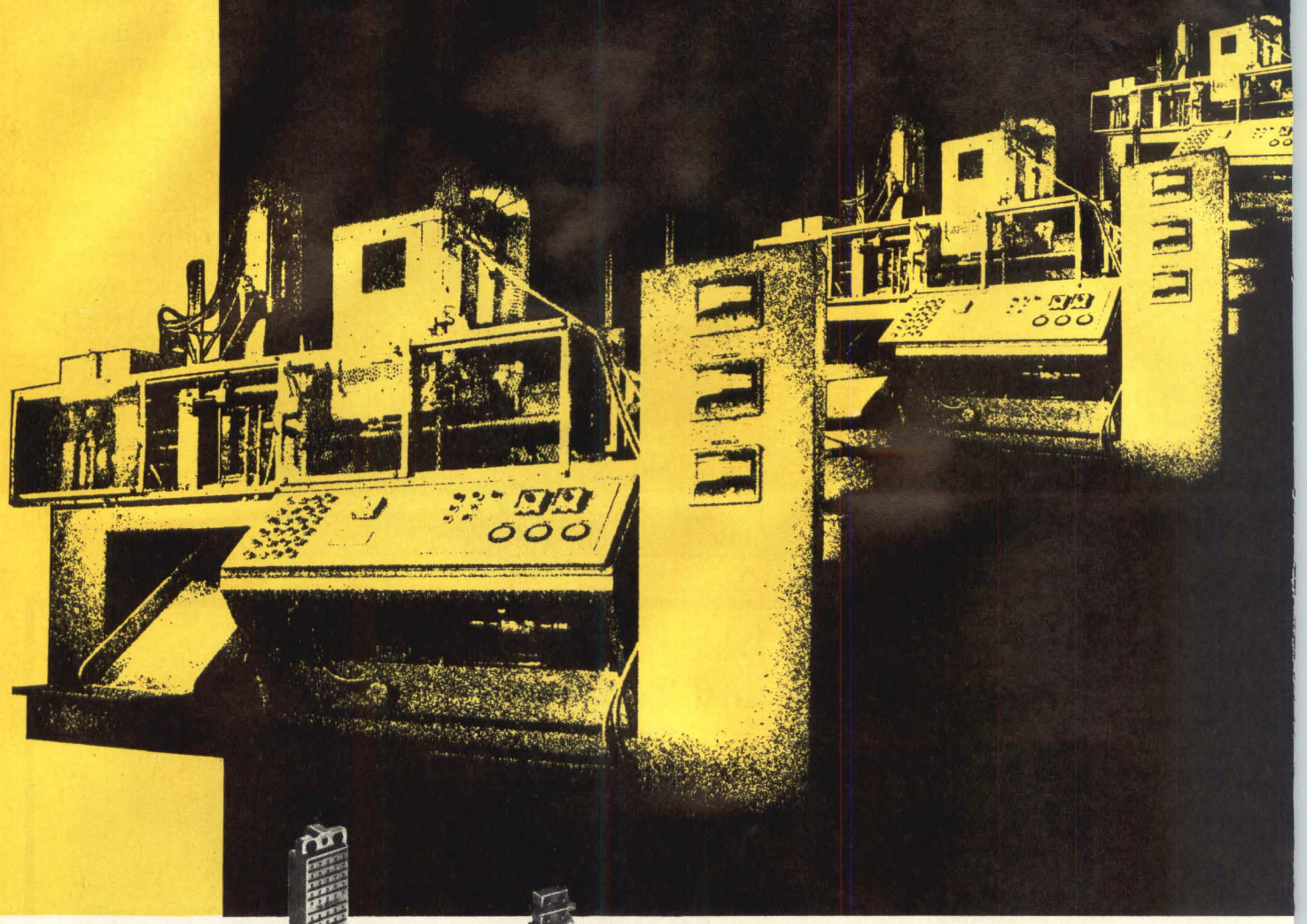

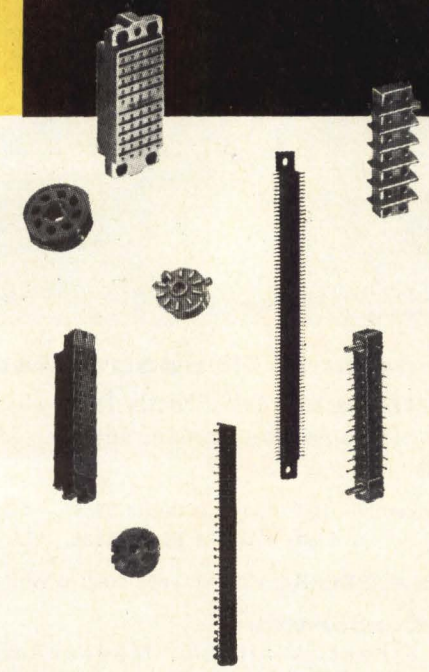

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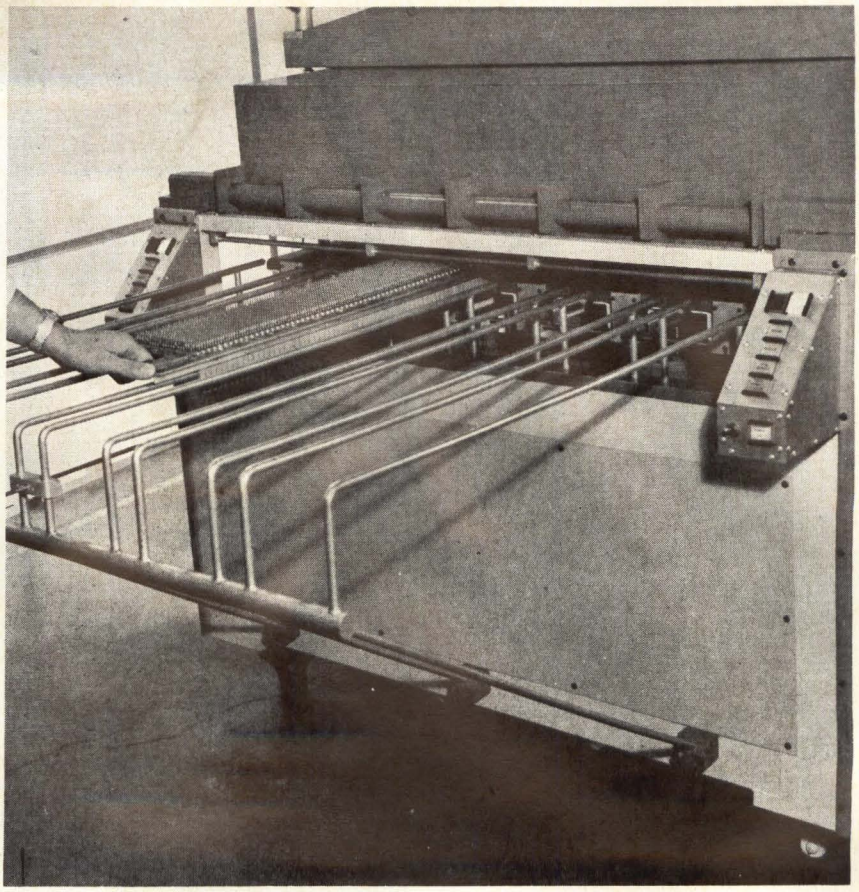

Fig. 4. Spring-pin type back-plane access fixture — 6 rows, 16,000 termination.

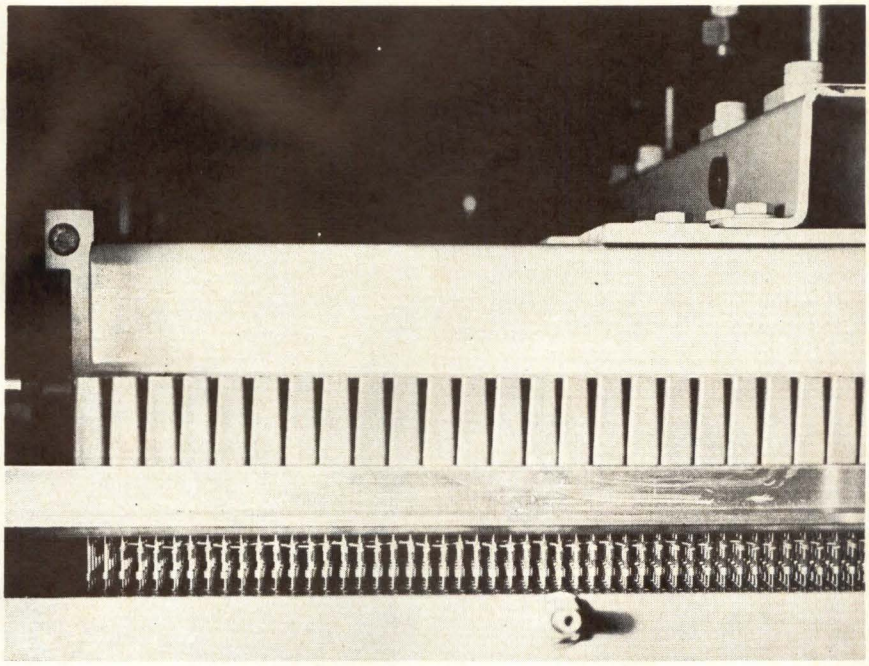

Fig. 5. Side view of spring-pin access fixture with back-plane in engaged position.

slow speeds reflect the irreducible operating times of the high-voltage relays included in the switching portion of the analyzer.

In designing a wiring analyzer for the test homogeneous interconnect systems, where insulation resistance limits and maximum test voltages are relatively low, advantage can be taken of this reduced requirement to design a system that is about an order-of-magnitude faster than the

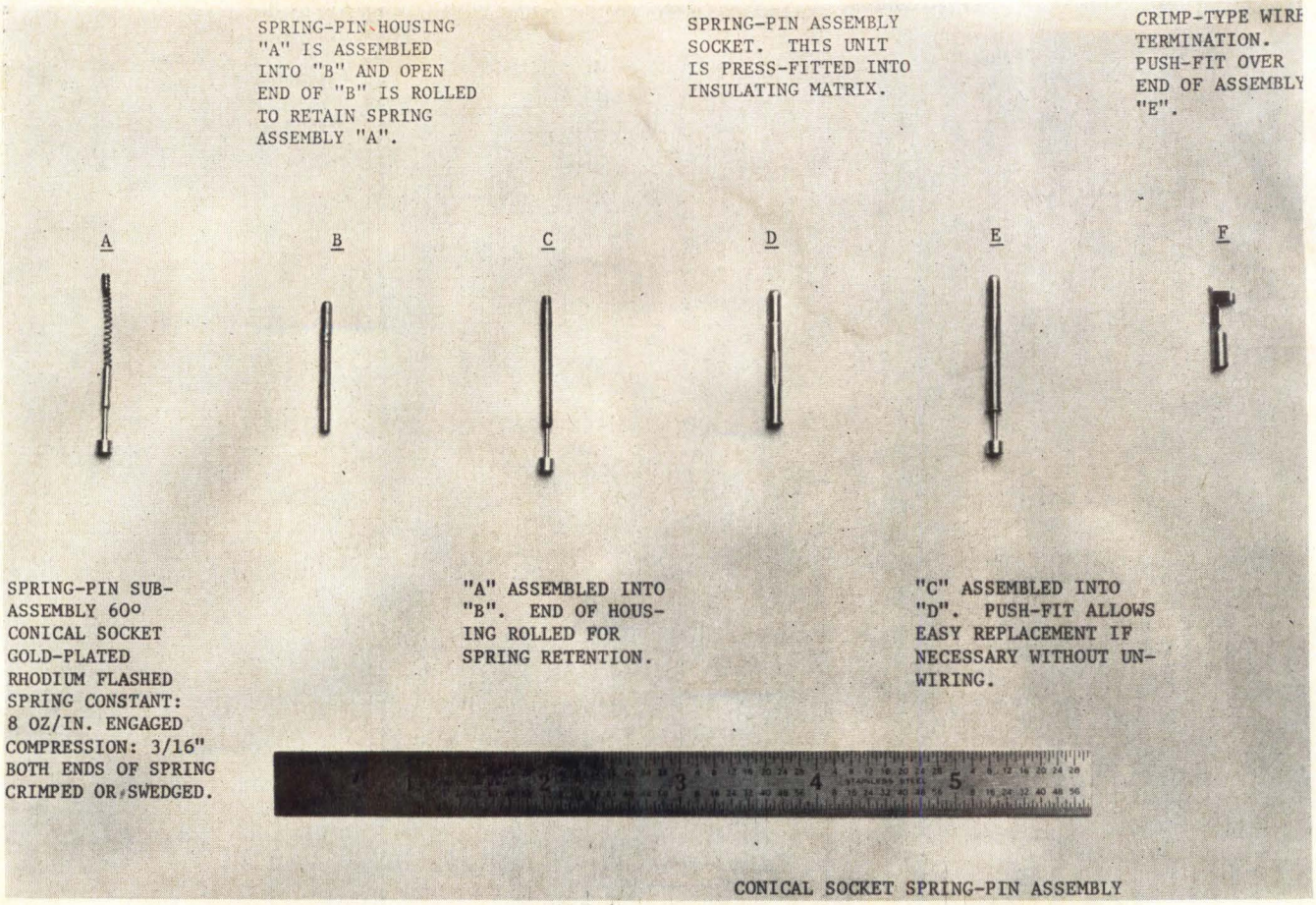

Fig. 6. Conical socket spring-pin assembly.

general-purpose system. In this type of testing, speed (and of course, reliability) is paramount, as the user is looking for the maximum throughput for capital dollar invested. With the requirements of high voltage (slow relays) and high insulation resistance limits (long test dwell times) removed, a much faster system can be produced. A wholly-adequate validation test of logic interconnect systems can be obtained at reduced voltage and insulation levels. To illustrate this point, characteristics of two wiring analyzers presently available from the DIT-MCO are compared as shown in Table 1.

Fig. 7 is a photograph of the control portion of the 6120 wiring analyzer with its logic section extended. Fig. 8 is a switching console sized for 9,000 termination capacity. Connections are made between these front face connectors and the access fixture via adapter cables. Each horizontal connector row in Fig. 8 corresponds to one 500 termination switching module, any number of which may be added to expand the system. All test instructions are entered via a 300 cps photoelectric tape reader (or, if desired, with a com-

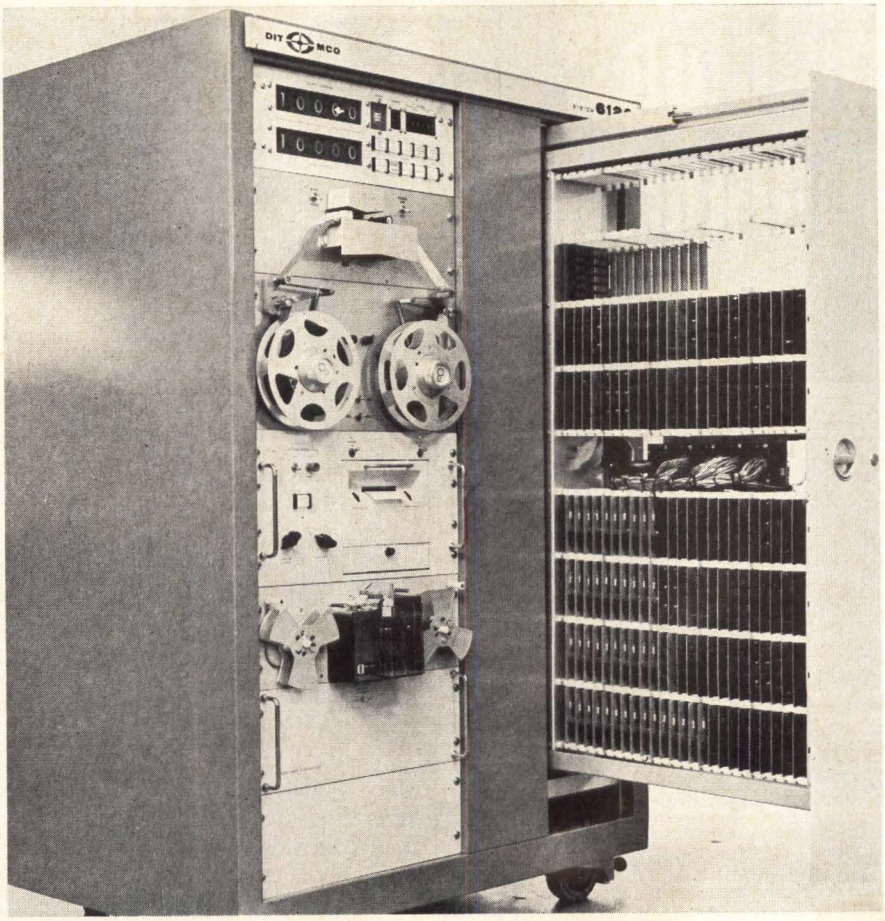

Fig. 7. Control console of DIT-MCO's System 6120 wiring analyzer.

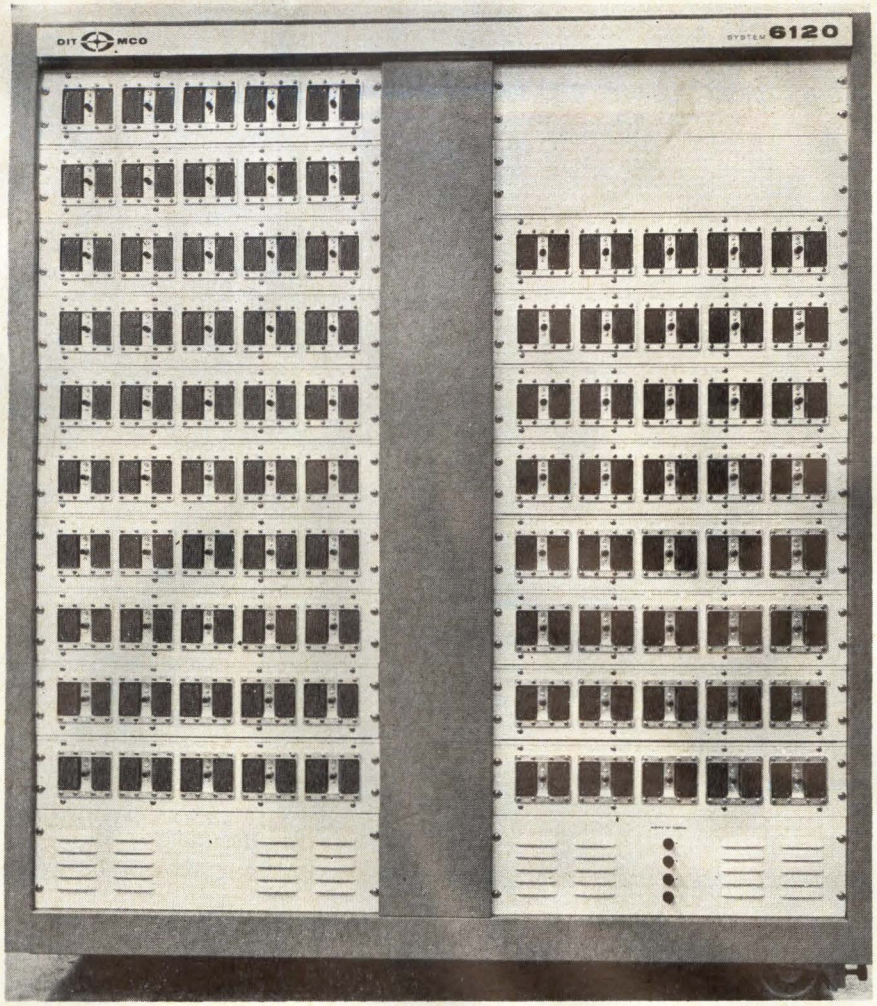

Fig. 8. Switching console (9,000 terminations) of DIT-MCO's System 6120 wiring analyzer.

puter or card reader). Programming is extremely simple and may be prepared manually by computer or by the wiring analyzer itself when operated in its self-programming mode. The self-programming technique is particularly useful when a computer conversion program is not available. To prepare a program tape in the self-programming mode, the analyzer is connected to a "known-good" wiring system, and will automatically punch out an entire test program which may then be used to validate identical systems.

The analyzer has several features useful in diagnosing wiring errors. For example, it will distinguish between shorts that occur to the frame or the copper sheet of a back-plane from those between back-plane wires. This omits redundant error printouts of the many ground terminal addresses accessed by the fixture. Certain other disturbed busses such as collector supply, bias, or logic ground that have many repeated terminations may also be handled in this way. Also, when continuity errors occur in back-plane testing, usually it is not that the wire is broken or missing, but that it has simply been wired to the wrong point. If so enabled, and in the event of a continuity error, the analyzer will scan for the existence of an erroneous wire routing and identify where the wire was actually terminated.

Summary

Production rates in the computer industry, measured by any of a number of criteria, such as total quantity of point-to-point connections, have expanded rapidly in the past few years. In order to keep pace with this growth, quality control procedures must be upgraded. The combination of rapid-access fixtures and high-speed wiring analyzers provides for these needs. ■

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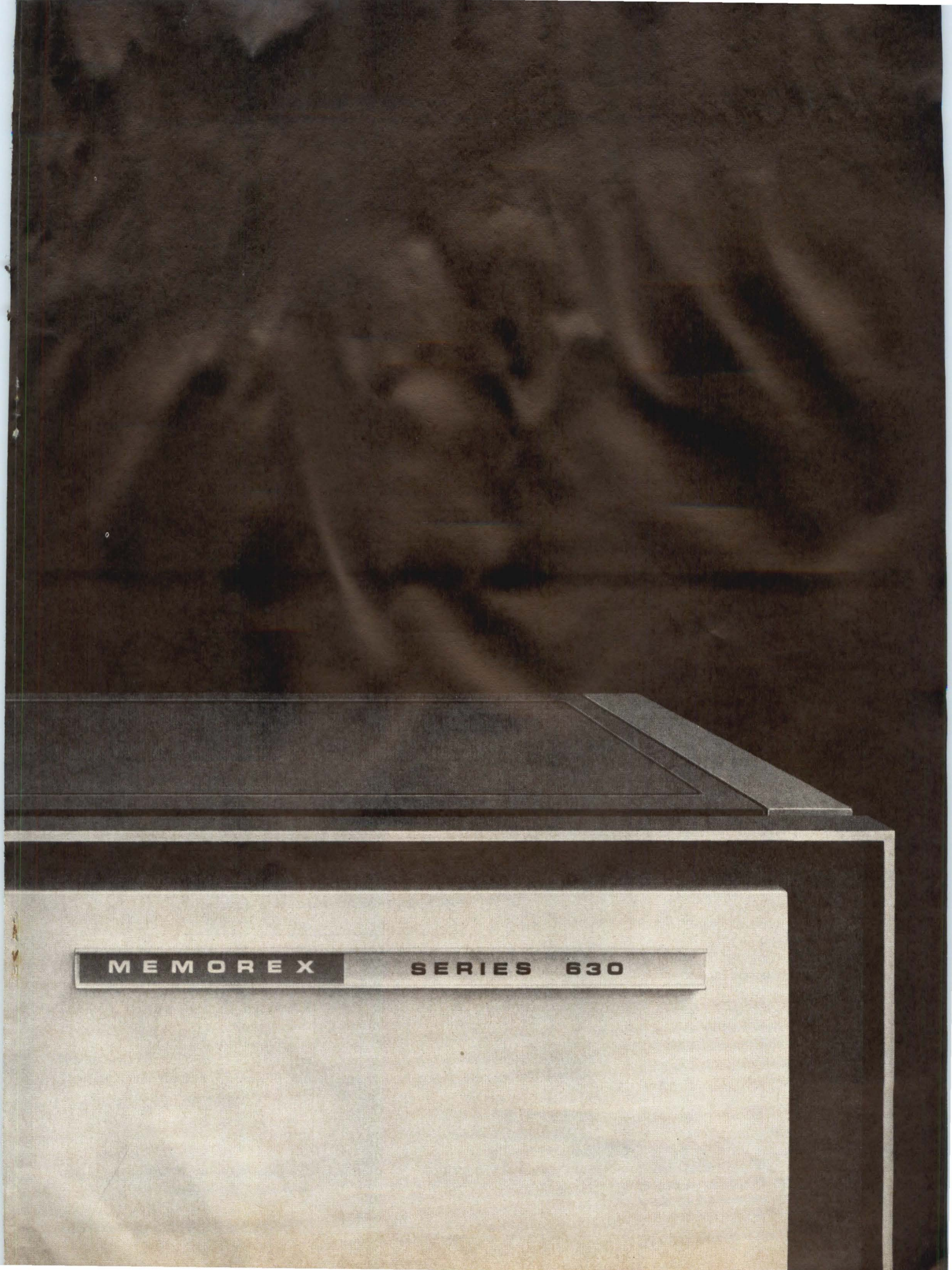
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A ONE-STEP PROCESS FOR OBTAINING FLIP-FLOP INPUT LOGIC EQUATIONS

Through the use of a table of simple rules, a new method provides the flip-flop input equations directly from the application equation, eliminating the usual step of considering the characteristic equations.

JONAS BERARU,
TRW Systems,
Redondo Beach, Cal.

There are several commonly-used methods for deriving flip-flop input logic equations through the combination of the application equations and the characteristic (or difference) equations for flip-flops.[1,2,3] The usual procedure is to generate the application equations for a desired logical design (e.g., a binary counter), to develop the characteristic equations for a given type of flip-flop, and to combine these to obtain a set of input logic equations which describe the logical interconnection of the flip-flops which will realize the application equations. Any of several available techniques may be employed to reduce or minimize the number of logic elements necessary for the final design.

In a new book devoted to digital computer design methods that are practical, straightforward, and largely self-working,[4] a method of writing flip-flop input equations directly from the application equation is presented. This method eliminates the step of considering the characteristic equations of flip-flops through the use of a table in which the equations are embedded. The table is shown here as Table 1 and contains modification rules for each of the six kinds of flip-flops in common use. To utilize the table, the application equation is plotted on a Karnaugh map (although the method is not dependent on the use of the Karnaugh map; any of the Boolean simplification methods can be used).

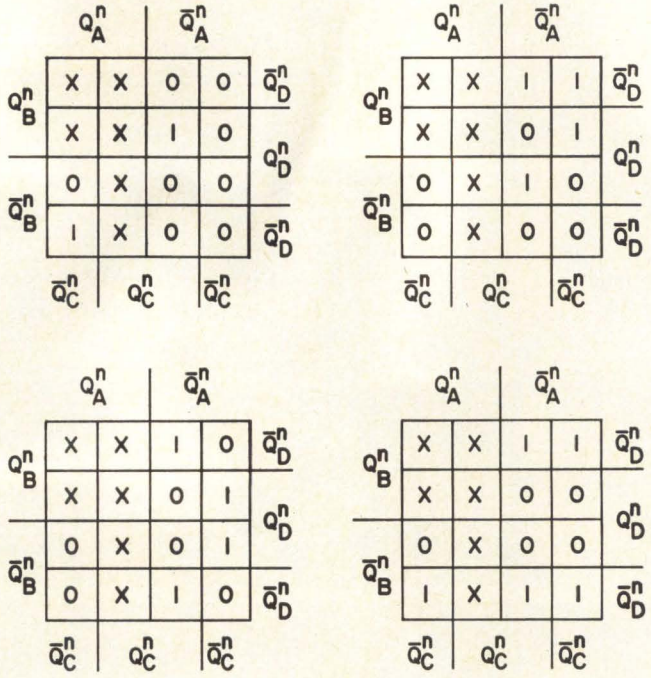

Fig. 1 BCD counter application equations.

After mapping the desired application, a particular flip-flop type is selected and appropriate variable columns (or rows) of the Karnaugh map are modified in accordance with the rules of Table 1. The resulting Karnaugh map is now a map of the flip-flop input equations and may be simplified by combining minterms. The intermediate step of using flip-flop characteristic equations has been completely eliminated.

BCD Counter

To illustrate the design process, we shall use a binary-coded decimal

TABLE 1

FLIP-FLOP CHARACTERISTIC TABLE

		FLIP-FLOP TYPE					
		D	T	R	S	J	K
State of Q^n	In Application Equation	0 1 X	0 1 X	0 1 X	0 1 X	0 1 X	0 1 X
	In Input Equation	0 1 X	1 0 X	1 0 X	0 X X	X X X	1 0 X
State of $\bar{Q}^n$	In Application Equation	0 1 X	0 1 X	0 1 X	0 1 X	0 1 X	0 1 X
	In Input Equation	0 1 X	0 1 X	X 0 X	0 1 X	0 1 X	X X X

counter example. This counter, which is described in Table 2, counts sequentially from 0 through 9 (10 through 15 being "don't care" states), however the actual pattern of count is immaterial as long as an application equation describing it can be written. This particular example was selected because such counters are common in practice, because it contains don't-care minterms, and because it will illustrate the rules of Table 1 on a D, T, R-S, and J-K flip-flop in a single example. R-S-T flip-flops are not considered at all because of their low frequency of use and because they do not yield a single final answer using the table. As usual, Q^n represents the present state of a flip-flop and Q^{n+1} represents its state at the next bit or clock pulse time. Also, Q is a general flip-flop type; we will designate specific types by D, T, R-S, or J-K.

The application equations and their Karnaugh maps for Q_A^{n+1}, Q_B^{n+1}, Q_C^{n+1}, and Q_D^{n+1} are shown in Fig. 1. At this point we are at liberty to select any of the flip-flop types in Table 1. We are free to select one type of flip-flop for Q_A, Q_B, Q_C, and Q_D or we can mix the types. All we need do is take care that we use the proper columns in Table 1 and that we modify the appropriate columns in the Karnaugh map. For the purpose of illustration, let us use one of each type of flip-flop. Arbitrarily, let us select a D for Q_A, a T for Q_B, an R-S for Q_C, and a J-K for Q_D.

By changing the 1's, 0's and X's in the Karnaugh maps of Fig. 1, in ac-

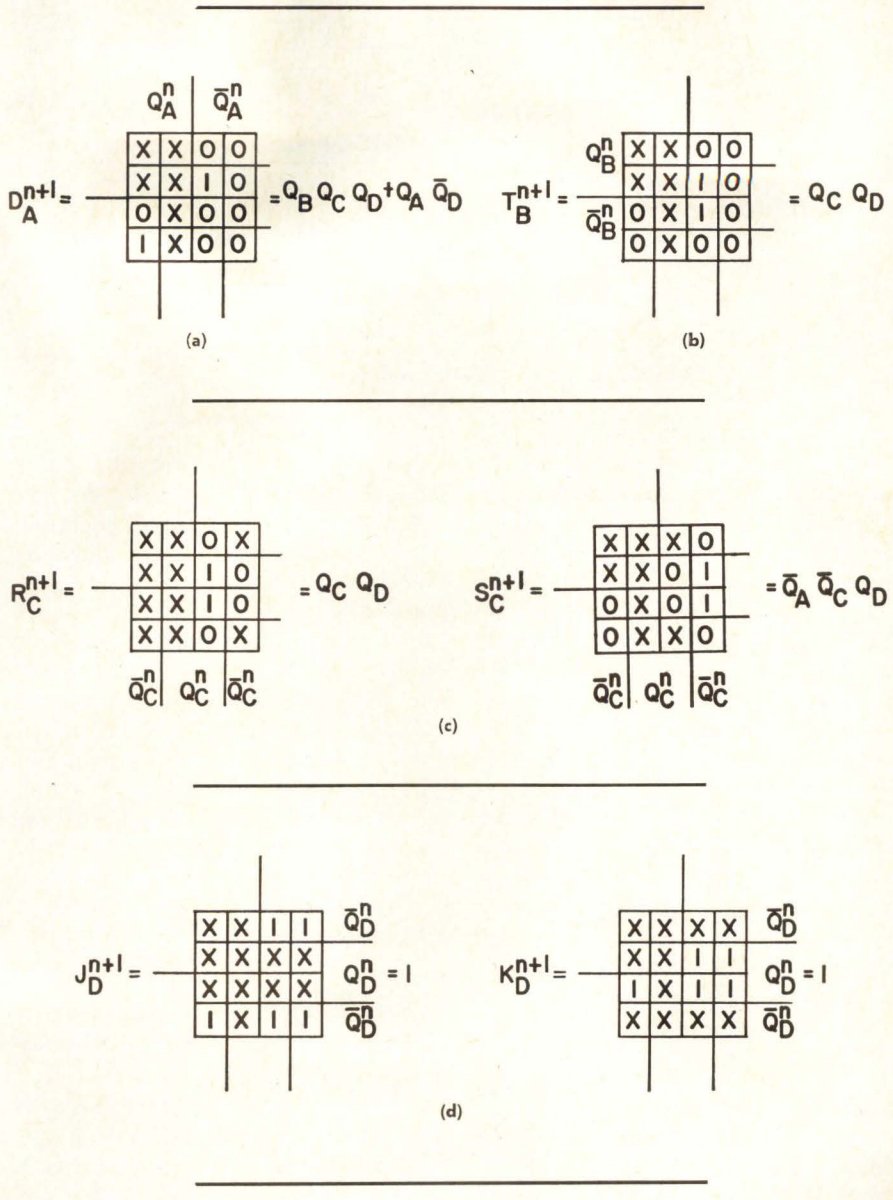

Fig. 2 BCD counter input equations.

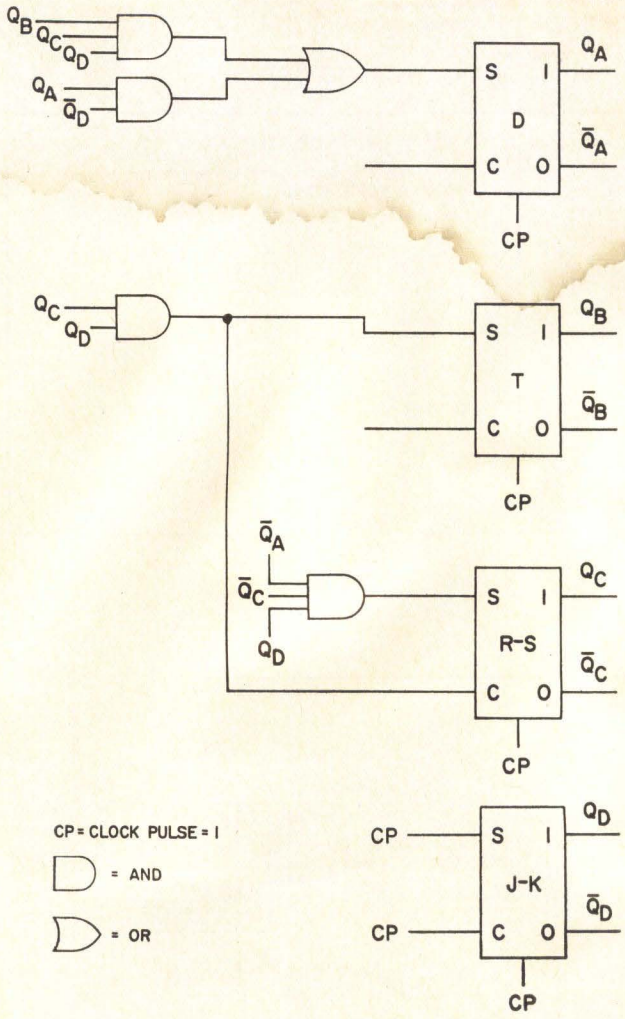

Fig. 3 Mechanization of the BCD counter.

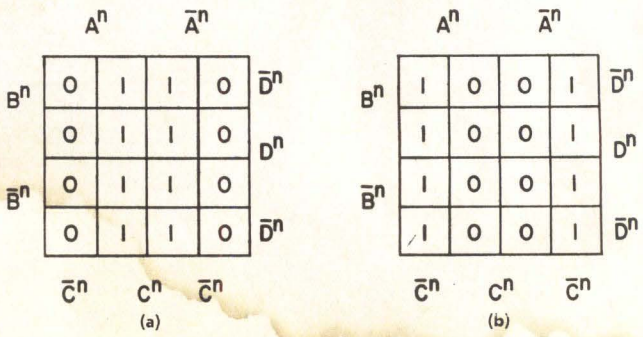

Fig. 4 Karnaugh maps for a T flip-flop.

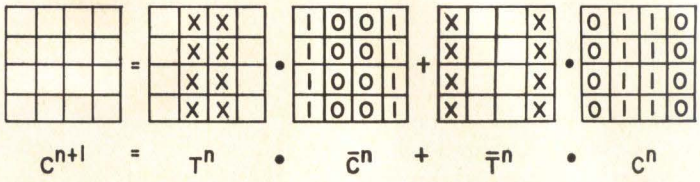

Fig. 5 C^{n+1} map for T flip-flop.

cordance with the rules of Table 1, we will have generated the Karnaugh maps of the flip-flop input equations directly. We can then simplify these input logic equations by the usual simplification methods. The maps of Fig. 1, as modified by the rules of Table 1, are shown in Fig. 2. To emphasize the rules of Table 1, only those rows or columns being modified by the rules in Table 1 are indicated by their flip-flop designations. For example, in Fig. 2 (a), only the Q_A and $\overline{Q}_A$ are indicated since we are solving for D_A^{n+1}. In 2 (b), we only indicate the Q_B and $\overline{Q}_B$ rows since we are interested in T_B^{n+1} and no other of the flip-flops. Fig. 3 is a schematic representation of the mechanized logic input equations.

Derivation of Table 1

Since Table 1 is designed to allow input logic equations to be written directly from application equations, and since each type of flip-flop is characterized by a specific characteristic (or difference) equation, these distinctive equations must be incorporated into the table. For the case of D flip-flops, Table 1 shows that no transformation of the Karnaugh map is necessary; this might be expected since a D flip-flop is nothing more than a single bit time-delay. The other types, T, R-S, and J-K, are more complicated. We shall show the derivation specifically for the T flip-flops; the R-S and J-K are quite similar in nature.

The characteristic equation of a T flip-flop is:

$$Q^{n+1} = T^n \overline{Q}^n + \overline{T}^n Q^n$$

We know Q^{n+1}, $\overline{Q}^n$, and Q^n because Q^{n+1} is the application equation we started with and $\overline{Q}^n$, Q^n are particular T-type flip-flops. Fig. 4 shows the Karnaugh maps for Q^n and $\overline{Q}^n$, for a four-variable case, where C is the flip-flop to be described. Our unknown quantities are T^n and $\overline{T}^n$. Similar maps can be drawn for both the complemented and uncomplemented variables A, B, and D.

We know that Karnaugh maps can be multiplied or added by the usual rules of Boolean algebra. By these operation rules, we know that any maps multiplied (ANDed) by (a) of Fig. 4 must result in a map with 0's where (a) has 0's; the rest of the resulting map depends on what the 1's of (a) are being ANDed with. Fig. 4(b) will have the same kind of effect in multiplication except that the 1's and 0's are in different columns from (a). Since we know Q^{n+1}, Q^n, and $\overline{Q}^n$ (C^n and $\overline{C}^n$ in this derivation), we must now find either T^n or $\overline{T}^n$; either will suffice since they are complements of each other. We can immediately fill in the C^n columns of T^n and the $\overline{C}^n$ columns of $\overline{T}^n$ with X's. This is because these columns will be multiplied by 0's and it is immaterial whether they had 0's or 1's; the final product will always be 0's. Fig. 5 shows our Karnaugh maps at this state of the derivation. Without knowing the application we cannot proceed beyond this point.

Once we decide on an application equation, we can fill in the C^{n+1} maps and calculate what went into the T^n map to generate the $\overline{C}^n$ columns of C^{n+1}. When we have this,

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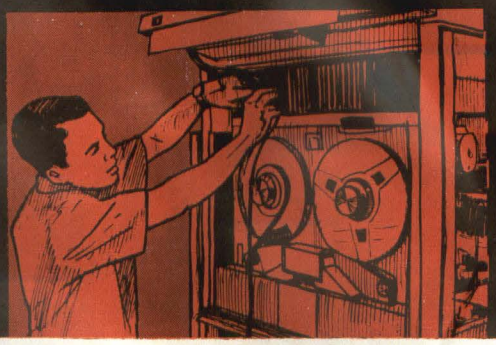

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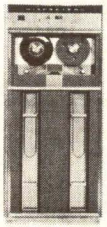

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TABLE 2

BCD COUNTER SEQUENCE

Q_A^n	Q_B^n	Q_C^n	Q_D^n	Q_A^{n+1}	Q_B^{n+1}	Q_C^{n+1}	Q_D^{n+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

TABLE 3

SEQUENCE WITH NO DEPENDENCE ON Q_D^n

Q_A	Q^n Q_B	Q_C	Q^{n+1} Q_D	Q_C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

we can determine $\overline{T}^n$ immediately by taking the complement of T^n. From this reasoning, we can determine the rules as set forth in Table 1. For example, X's remain X's in both the C^n and $\overline{C}^n$ columns of C^{n+1}. We see that 0's and 1's are interchanged in the C^n column of C^{n+1}; we also note that 0's and 1's remain unchanged in the $\overline{C}^n$ columns of C^{n+1}. Similar reasoning was applied to R-S and J-K flip-flops to complete Table 1.

An Extension To The Method

Table 2 illustrated the case where the state of a flip-flop at time $(n+1)$ depended on the state it had at time

n and the state of the other flip-flops at time n, i.e., Q_B^{n+1} is a function of Q_A^n, Q_C^n, and Q_D^n as well as Q_B^n. Our method is easily extended to cases where a flip-flop at time $(n+1)$ is not dependent on the states of other flip-flops at time n. A common example of this is the case of a flip-flop in the circulating path of a binary adder. Its present state, as Table 3 shows, does not depend on the previous state of flip-flop Q_D. We cannot write input equations using Table 1 rules since there is no explicit Q_D in our Karnaugh maps. To remedy this, we use the Boolean identity:

$$X \cdot D + X \cdot \overline{D} = X$$

This has the effect of adding an additional column to Table 3; this column represents Q_D. There are now twice as many entries in our table as before but the use of the Boolean identity assures us that nothing has really changed. We readily see that this creates a table in which the following are the first few entries:

Q^n				Q^{n+1}	
Q_A	Q_B	Q_C	Q_D	Q_D	Q_C
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	0
etc.				etc.	

We now proceed as we did for our example of the counter, since the maps for the input equations of Table 3 now contain Q_D, and we can use Table 1 directly to find input logic equations.

REFERENCES

1. Phister, M., Jr., *"Logical Design of Digital Computers,"* John Wiley and Sons, Inc., New York, 1958.

2. Ledley, R. S., *"Digital Computer and Control Engineering,"* McGraw-Hill Book Company, Inc., New York, 1960.

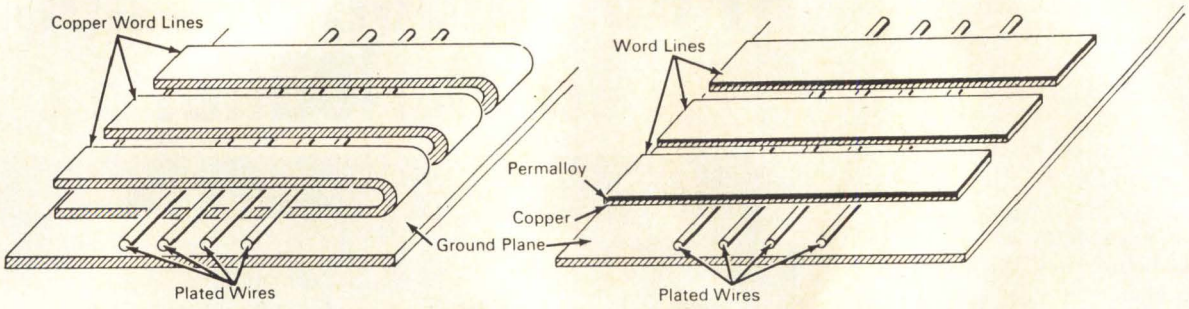
3. Bartee, T. C., Lebow, I. L., and Reed, I. S., *"Theory and Design of Digital Machines,"* Lincoln Laboratory Publications, McGraw-Hill Book Company, Inc., New York, 1962.

4. Beraru, J. and Hartman, S., *"Fundamentals and Design Concepts of Digital Computers,"* John Wiley and Sons, Inc., New York (to be published).

NASA TECH BRIEF

A SUMMARY OF A SPECIFIC TECHNICAL INNOVATION DERIVED FROM THE SPACE PROGRAM. ISSUED BY THE TECHNOLOGY UTILIZATION DIVISION OF NASA.

Improved Memory Word Line Configuration Allows High Storage Density



FULL TURN CONFIGURATION

HALF-TURN CONFIGURATION

THE PROBLEM:

To design a plated wire memory word drive line configuration which allows high storage density, good plated wire transmission characteristics, and a simplified memory plane configuration. Prior art used a plain copper full-turn word line to obtain word field uniformity. With the plain copper word line the word field spread to the extent that the desired high storage density could not be obtained. Also, with this configuration the connections have to be made to both ends of the word line to obtain efficient selection of the word lines. With both ends of the word line available at the same side of the plane, the connections are complicated, particularly since the two ends are in different layers of the plane construction. The full turn construction does not allow good plated wire transmission characteristics because of the presence of the copper word line between the plated wire and the ground line return path.

THE SOLUTION:

A half-turn word drive line with a magnetic keeper. The ground plane provides the return path for both the word current and the plated wire transmission line.

HOW IT'S DONE:

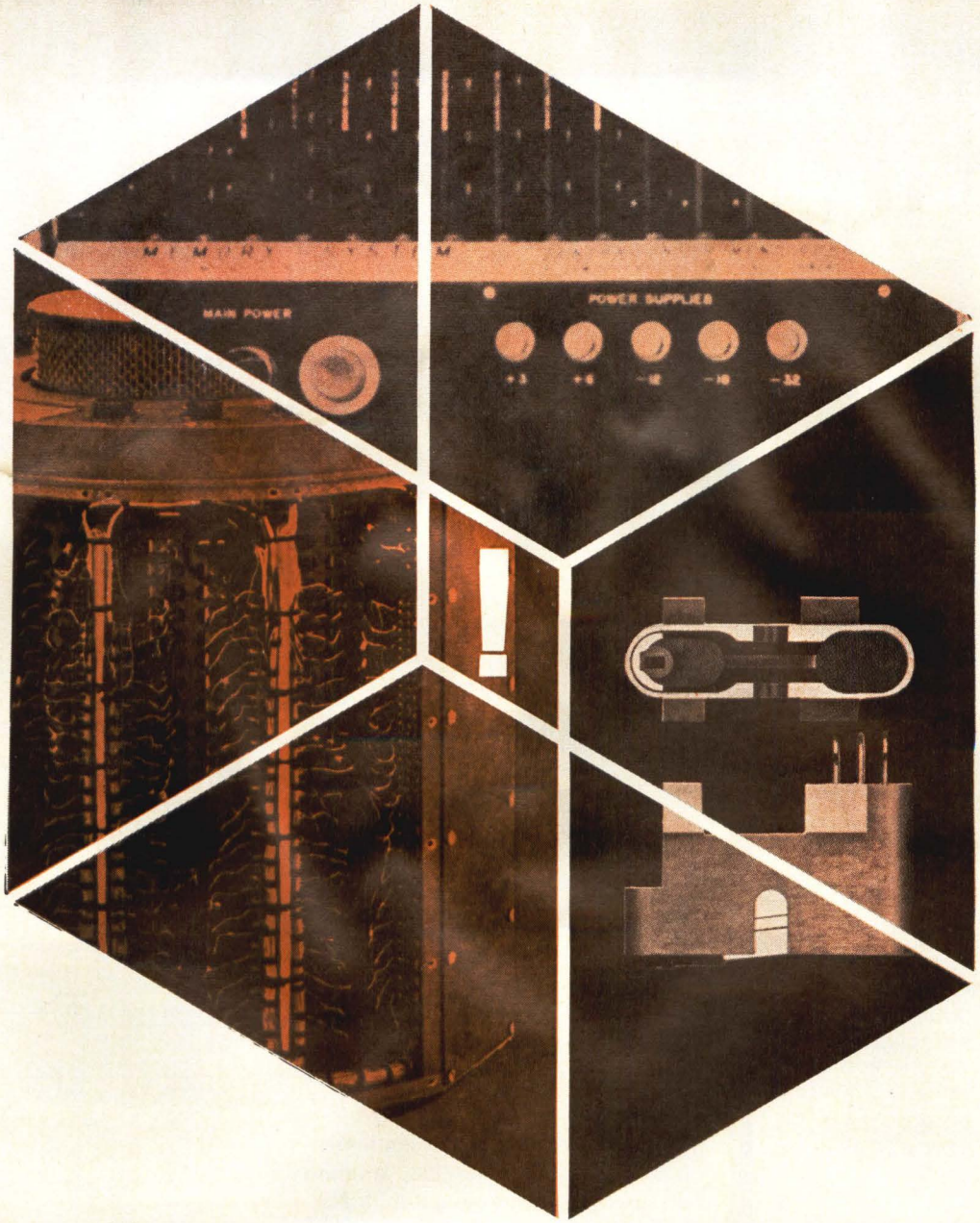
The half-turn word line structure is made by copper plating a thin magnetic sheet which is cemented to a supporting dielectric. This composite is then photo-etched leaving the desired word line pattern. The copper and the magnetic material are etched away at the same time. High storage density is achieved by having magnetic strips slightly wider than the word lines on top of the word lines. These strips provide a low reluctance path for the word field and inhibit it from spreading.

NOTE:

Inquiries concerning this invention may be directed to: Technology Utilization Officer, Goddard Space Flight Center, Greenbelt, Maryland 20771. Reference: B66-10617

PATENT STATUS:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546. **END**



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CIRCLE NO. 54 ON INQUIRY CARD

NEW PRINTED CIRCUIT PROCESS

Simplified production technique permits highly-reliable plated-through boards for packaging integrated circuits

Photocircuits Corp. of Glen Cove, N. Y. recently announced the development of a new, low-cost printed circuit production process called NT-1. The simplicity of the process is achieved by the elimination of the costly electroplating process. Reliability is assured since all the performance characteristics produced by conventional techniques are retained, while many of the inherent limitations of electroplated boards are eliminated. Photocircuits claims that the three following developments provide the essential elements for this improved lower cost process.

- **Catalytic copper-clad laminate** — conventional copper-clad laminates are used in the manufacture of NT-1 circuits, with one notable modification. The resin is impregnated with a small amount of inert catalyst to make all exposed surfaces, after etching and hole fabrication, susceptible to copper deposition.

- **Electroless deposited copper** — Photocircuits' CC-4 electroless copper process produces a fine-grain, pure, ductile copper which can be deposited with exceptional uniformity upon laminates and within punched or drilled holes in any required thickness. Because of its purity and grain structure, the CC-4 copper is said to exhibit very favorable solderability characteristics.

- **Permanent, non-registered solder mask** — the permanent, non-registered solder mask used on NT-1 circuit boards is a high-grade protective

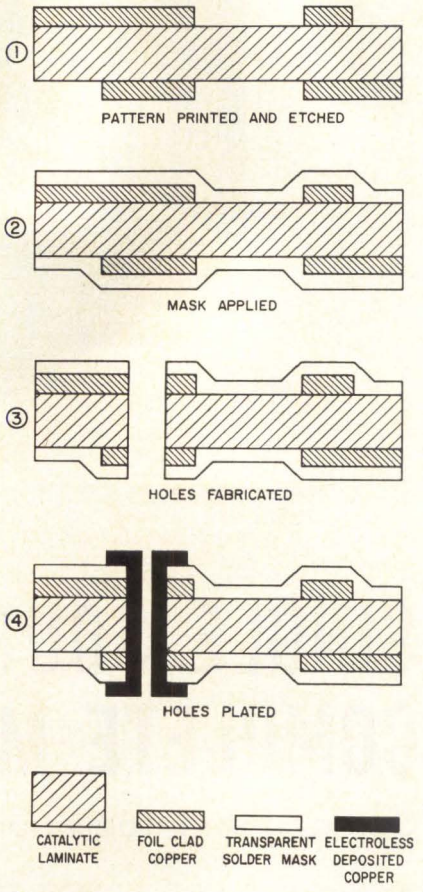

Fig. 1. The simplicity of the NT-1 process is indicated by the above procedure. (1.) The conductor pattern is printed on both sides of the copper-clad catalytic laminate. The patterns are then etched and the resist is stripped off. (2.) A thin, non-registered, transparent solder mask of non-catalytic epoxy resin is applied to the surface. (3.) Holes are drilled or punched through the mask, conductor pattern, and laminate. (4.) Copper is deposited on the walls of the holes by electroless deposition. The board is then ready for fabrication.

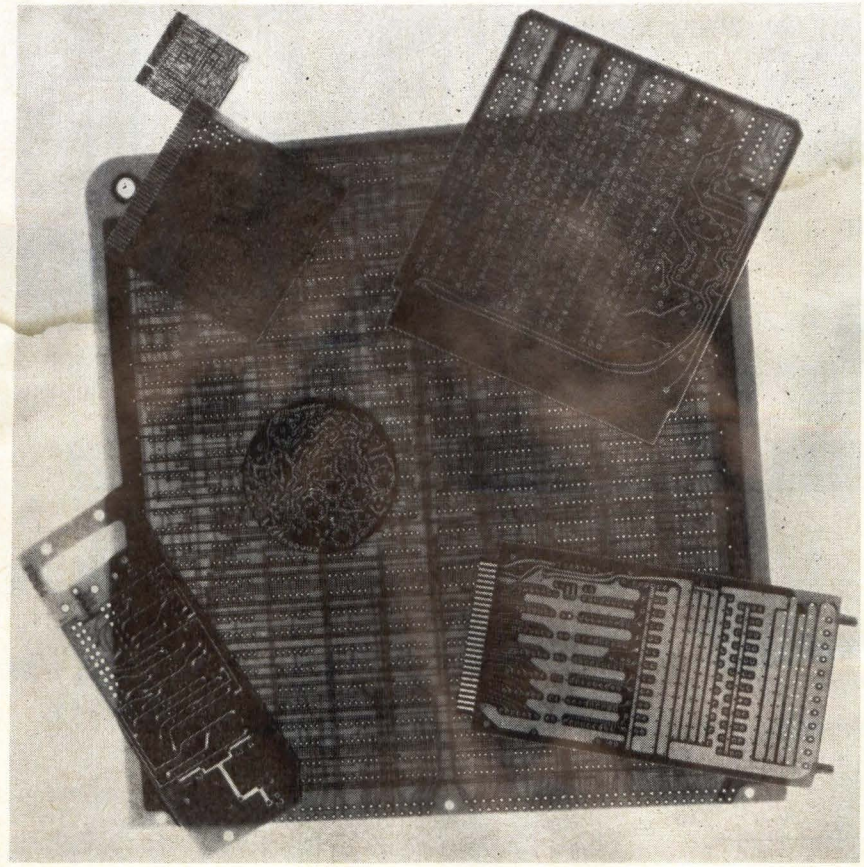

Fig. 2. A sampling of NT-1 printed circuit boards produced for a variety of dense pattern packaging applications.

coating impervious to any of the normally-used cleaning solutions. It encapsulates and protects the surface conductors from electrical leakage under high humidity conditions, eliminates bridging during soldering, and prevents damage during field repair.

Steps in the NT-1 manufacturing process are shown in Fig. 1. The pattern of conductors is printed and etched from the foil of two-sided base laminates in the first step. The patterns on both sides of the board are then protected with a permanent, transparent epoxy coating (non-registered solder mask). Thereafter, the holes are drilled or punched through, and copper is deposited in them, interconnecting the patterns on both sides of the board.

The two prime advantages of NT-1 over conventional techniques, according to Photocircuits, are economy and design flexibility. The most significant cost-saving benefit is the elimination of the expensive electroplating process. Specific advantages claimed for the NT-1 boards are:

- Fine lines and spacing (for example, small diameter holes on 50-mil centers with conductors between the holes);
- Virtually no limitation on hole diameter to depth ratio (for example, 10:1 ratios are easily attained).

In addition, NT-1 boards are said to eliminate solder bridging and slivers from plating overhang, while providing "built-in" conformal coating.

A sampling of NT-1 circuit boards are shown in Fig. 2.

For more information on this new printed circuit board technique:

Circle No. 105 on Inquiry Card

negative radix arithmetic

M. P. deRegt

Part 6: MANUAL DIVISION

The Magnitude Test

Editor's Note: In this month's article of this pioneering series on negative radix number systems, Mr. deRegt continues his study of the division operation, the first two parts of which appeared in the August and September issues.

In the introduction to negative decimal division presented in Part 4 (August, 1967), we covered the first three steps of manual division: locating the initial quotient digit, estimating the initial quotient digit, and computing the new remainder. The procedure for these steps is very similar to that for normal division, except for the different multiplication tables and the strangeness of the number lengths. The next step, testing the remainder, is quite different from the corresponding test in normal decimal division, and it is quite involved. The principal reason for this is related to the fact that we are using a non-restoring division algorithm.

The use of a non-restoring algorithm was first mentioned in Part 4, and the basis for its use was established in Part 5 (September), where several candidate algorithms were explored in detail. In Part 5, we also developed a polarity test for the remainder, using a non-restoring mechanical algorithm. Although a polarity test is quite appropriate in a mechanical algorithm, it is not suitable for a manual algorithm. In manual decimal division, we almost never formally test the remainder. A simple comparison between the partial dividend and digit product is usually sufficient, and this is done before computing the remainder. (See Table 3, Part 4 for a refresher on division nomenclature.) Even when the remainder is computed, such as when the quotient digit is too small, it is compared with the divisor for magnitude, which is, of course, a magnitude test.

Magnitude comparisons are much more difficult to make in negaradix notation than conventional, as we have observed. Even so, magnitude comparisons will generally be found to be more natural than a polarity test and will save much computation. As we shall see in this article, the magnitude test for non-restoring division is quite different from that for restoring; some clues as to its nature emerged toward the end of the last article. It is also much more interesting.

Numerical Values Of Test Limits

Referring to the first pass of example 3 presented last month, we note that a very small interim dividend, 515 (+495), relative to weighted divisor, 28300 (+12300), occurs just before the polarity change when the corresponding quotient is 600 (+600). The result of the next operation is an interim dividend of 192215 (−11805) which is correspondingly close in magnitude to the weighted divisor. The quotient at that point is 700 (+700). Since the weighted divisor for the next pass is 2830 (−1230), it takes ten operations to complete the second pass, which ends up with an interim

TABLE 1

NEGADECIMAL REPEATING RADIX FRACTION SPECIAL FORMS

Repeating Radix Fraction	Limiting Decimal Values
.	.
.	.
.	.
1.8888. . .	+3/11
1.9999. . .	+2/11
1.9090. . .	+1/11
0.0909. . .	+1/11
0.0000. . .	0
0.1111. . .	−1/11
0.2222. . .	−2/11
0.3333. . .	−3/11
.	.
.	.
.	.
0.9999. . .	−9/11
0.9090. . .	−10/11
19.0909. . .	−10/11
19.0000. . .	−1
19.1111. . .	−12/11
.	.
.	.
.	.

dividend of 515 (+495) and a quotient of 600 (+600) — the same values we found after the next-to-last operation of the first pass. Clearly, we might have skipped the second pass altogether by not performing the final or polarity-changing operation of the first pass.

We see that such a situation will arise, before the polarity change, whenever the magnitude of the interim dividend becomes less than about one-tenth of the magnitude of the weighted divisor. If the polarity-changing operation is performed in such a situation, the resulting quotient digit q_i will be incorrect — it will be too large by unity — and the next quotient digit, q_{i-1}, will also be too large, being in effect 190 (−10), which corresponds to ten operations in that pass. Therefore, in order to make sure that no more than nine operations will be required in the next pass, it is necessary to test the interim dividend, so that the polarity-changing operation will not be performed when its magnitude is less than about one-tenth of the weighted divisor.

To obtain the exact values of the magnitudes of the test limits, we must examine the radix-fraction equivalent of the fraction formed by the interim dividend and the weighted divisor at the end of pass i to develop q_i. The relationship is derived as follows:

$$\frac{\text{Interim Dividend}}{\text{Divisor}} = (q_{i-1})\ (q_{i-2})\ (q_{i-3})\ldots(q_0)\ (q_{-1})\ldots$$

$$\frac{\text{Interim Dividend}}{10^1\ (\text{Divisor})} = \frac{(q_{i-1})\ (q_{i-2})\ (q_{i-3})\ldots(q_0)\ (q_{-1})\ldots}{10^1}$$

$$\frac{\text{Interim Dividend}}{\text{Weighted Divisor}_i} = (0)\ (q_{i-1})\ (q_{i-2})\ (q_{i-3})\ldots(q_0)\ (q_{-1})\ldots$$

At the beginning of pass i-1, this relationship becomes:

$$\frac{\text{Interim Dividend}}{\text{Weighted Divisor}_{i-1}} = (q_{i-1})\ (q_{i-2})\ (q_{i-3})\ldots(q_0)\ (q_{-1})\ldots$$

and obviously q_{i-1} must not be greater than 9. Therefore, the maximum magnitude of the fraction at the end of pass i is 0.909090. . . . An insight as to why this is so may be obtained from Part 2, pages 58 and 59 of the June issue. Table 4 of that article presented certain special number forms for negabinary; Table 1 in this article gives a similar set of special forms for negadecimal.

Note, as we did in Part 2, that upper and lower limits in the box of Table 1 have limiting values identical to the adjacent limits in the adjoining boxes. The bottom limit-pair, 0.9090. . ./19.0909. . . , is of special interest to us. Its limiting value is −10/11, and we note that 0.9090. . . is the maximum permissible magnitude of the above ratio. If this ratio is less than $|-10/11|$, then the quotient digits up to and including q_i are correct, and the rest of the quotient will be $10^1(0.9090\ldots)$ to some number of digits. However, we note from the table that if this ratio is greater than $|-10/11|$, the "rest" of the quotient will be $10^1(19.0909\ldots)$ to some number of digits. The integral portion, 19 (−1), of this radix fraction will have the effect of diminishing the quotient digit q_i by unity, which is the effect we noticed as the result of the tenth operation at the end of the second pass of example 3 in Part 5.

Thus, if q_{i-1} is not to exceed 9, the interim dividend magnitude at the end of pass i must not exceed:

$$|\ (-10/11)\ (\text{weighted divisor})\ |.$$

This situation can be prevented by terminating pass i

negative radix arithmetic continued

before the polarity change, whenever the interim dividend magnitude is less than:

$$|(+1/11)\ \text{(weighted divisor)}|.$$

If the ratio is exactly $+1/11$, then both quotients, and hence both procedures, are technically correct, although failure to observe the test rule would result in extra operations.

The test is readily demonstrated by referring again to example 3 from Part 5. The interim dividend just prior to the polarity change in the first pass was 515 (+495), when the weighted divisor was 28300 (+12300). One-eleventh of the weighted divisor is +1118 2/11, which is much larger than the interim dividend. The test, therefore, indicates that the final diminishing operation should not be performed; instead, the pass should be terminated with a quotient digit of 6, the next quotient digit should be set to zero, i should be reduced by 2, to 0, and the next pass, for i = 1, should be skipped. This would leave us with a quotient of 600 (+600), and an interim dividend of 515 (+485) to start the i = 0 pass, which is identical to the third pass of the example.

If the remainder had been 19299 (+1119), which is larger than one-eleventh of the weighted divisor, the test would have indicated that the polarity-changing operation should be taken. If it had been 19298 (+1118), then as in the example, the polarity-changing operation should be skipped.

The Magnitude Test For Decimal Non-Restoring Division

We stated in the introductory comments that the reason for the more involved testing procedure required for negadecimal division was due primarily to use of a non-restoring algorithm. This assertion is borne out when we perform the analysis to determine the test limits for a decimal non-restoring mechanical algorithm.

Referring to Fig. 3 of Part 5, the flow chart for non-restoring division incorporating only the polarity test, we note that the diminishing operation stays the same for negadecimal, but alternates for decimal (assuming k does not change in the weighting factor, $(-1)^k(r^i)$). This is because in non-restoring division using positive radix, as in negative radix, the polarity of the interim dividend changes with each pass, but unlike negaradix, the polarity of the weighted divisor does not. This is shown in Fig. 3 of Part 5 by means of the dotted line which causes the procedure to oscillate from one branch to the other. Thus, subtraction must be used for passes in which the interim dividend and weighted divisor are of the same polarity, and addition when they are opposite. This action is confirmed by the decimal half of example 3 of Part 5, in which the weighted divisor is subtracted in the first and third passes, but is added in the second. Similarly, the weighting factor is added to the quotient in the first and third passes, and subtracted from it in the second.

Suppose, instead of doing arithmetic on the entire quotient using the weighting factor, we generated each quotient digit, starting from zero, by adding or subtracting the weighting factor coefficient $(-1)^k$. We should then find that some digits are positive, and some negative, and we could do the arithmetic on the quotient all at one time, after division is complete, by subtracting the negative component from the positive. If now we refer to example 1 of Part 1 (May), we find that such a quotient would actually be one expressed in special decimal, and the arithmetic we do on the quotient components after division is complete is simply the procedure for converting from special decimal to normal decimal.

Non-restoring division is thus seen to be arithmetically identical, step for step, in negative radix and positive radix notation, including the numerical limits of the magnitude test. This identity is emphasized in the flow chart for non-restoring division, Fig. 1(a). Fig. 1(b) shows the flow chart for restoring division, arranged to be symmetrical with Fig. 1(a) to emphasize both the similarities of and the differences between the two procedures. In Part 5, the flow charts for non-restoring and restoring division using the polarity test each showed two separate branches for negaradix and posiradix division. These separate branches have been combined in the flow charts of Fig. 1, so that the symmetrical comparison of non-restoring and restoring division could be made. Note that these charts apply to any positional scale of notation, with k or the dividend-diminishing operation arbitrarily selected.

The Division Algorithms Using The Magnitude Test

Referring to Figs. 1(a) and 1(b), the procedures constitute another transition step between the primitive counting algorithm of Part 4 and the final manual algorithm to be presented next month. The transition it illustrates is, of course, the use of a magnitude test rather than the use of a polarity test to test for the end of a pass, since this is how a human being divides. We have made few other changes over the flow charts of Part 5 for division using the polarity test; specifically, we are still generating the entire quotient by operating upon it at every step with the weighting factor, $(-1)^k(r^i)$, using the operation opposite to that used on the interim dividend by the weighted divisor, $(-1)^k(r^i)D$.

The changes over the flow charts of Part 5 include the substitution of box 2 in Figs. 1(a) and (b) for the first decision box, which compares the polarities of A and WD. This substitution permits combining the two branches of last month's flow chart into one branch, providing the more compact display we need for comparing the non-restoring and restoring algorithm. This compactness is achieved by the small price of the added complexity caused by the use of the compound signs in blocks 2, 3, 4, and 5. These compound signs are used in the usual way: the upper signs are used if the polarity obtained in block 2 is +, and the lower signs if this polarity is negative. The interim dividend (ID) is used, rather than the dividend (A), because in Part 5 the test was not in the loops, whereas in Figs. 1(a) and 1(b)

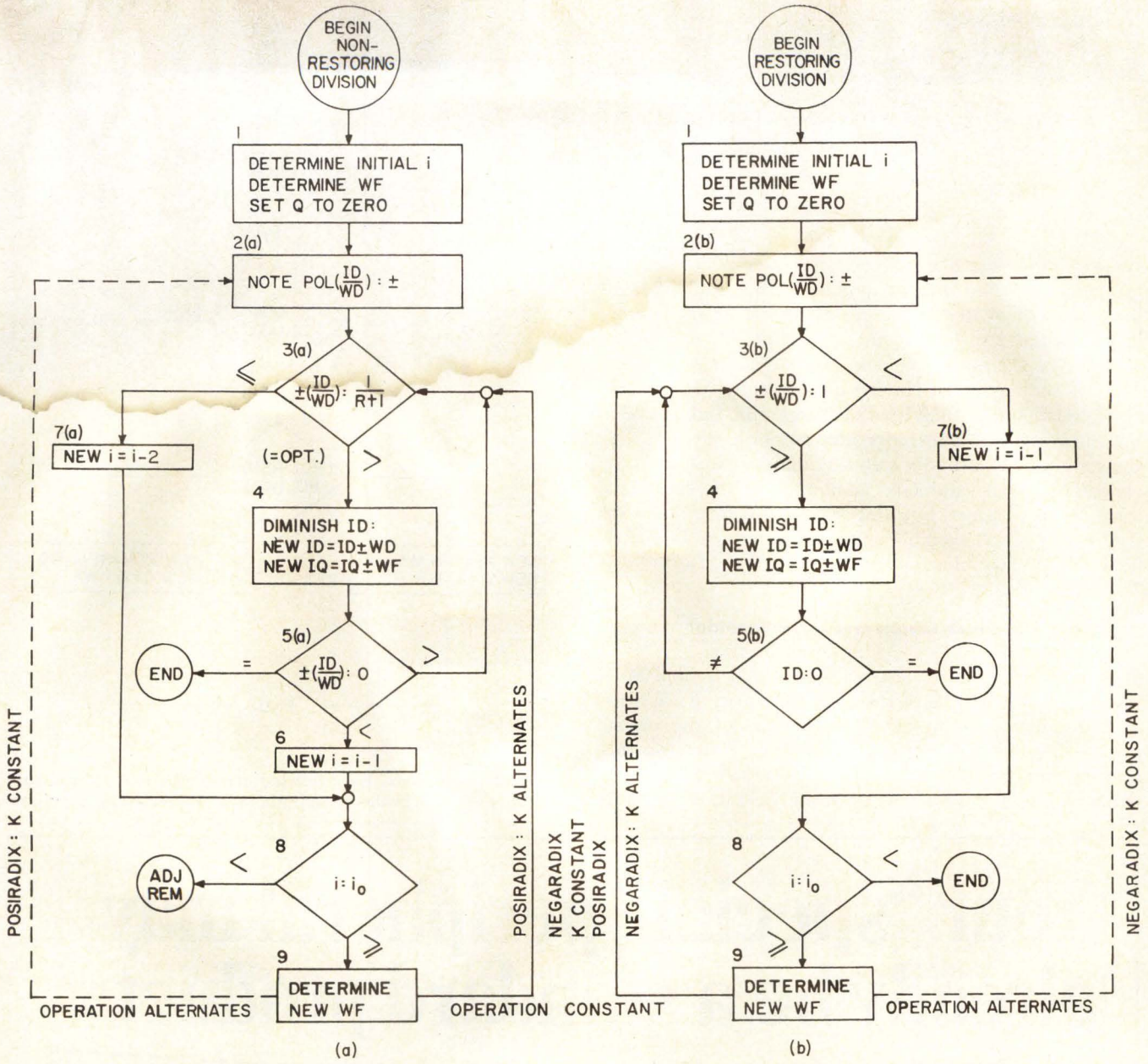

Fig. 1 Flow charts for (a) non-restoring and (b) restoring division using the magnitude test. "Natural" division is the situation in which the diminishing operation is constant, e.g., always subtraction, and k in the weighting factor, $(-1)^k$ (r^i), is constant, e.g., always zero. This is possible in negaradix non-restoring division and posiradix restoring division.

it is. Since the polarity of the ID changes with each pass, it must be used in the non-restoring algorithm. In the restoring algorithm, either A or ID could be used; we used ID to minimize essential differences.

We have also placed the polarity test before the diminishing operation, reversing the procedure used for the polarity test in Part 5. The reason for this, of course, is that the purpose of the magnitude test is to **avoid** the redundant step, so we **must** test first, whereas using the polarity test, the redundant step must be taken in order to be able to perform the polarity test. Note that the same thing holds true for restoring division: use of the magnitude test obviates the "restore" operation. In the non-restoring algorithm, however, we must still test the polarity after the diminishing operation, since the terminal interval (marking the end of the pass) into which the ratio $\pm(\mathrm{ID}/\mathrm{WD})$ must fall, $+1/(\mathrm{R}+1)$ to $-\mathrm{R}/(\mathrm{R}+1)$, straddles zero, and the magnitude test applies only to the positive portion. In the restoring algorithm, the terminal interval is R to 0, so the analogous test is a simple test for a zero interim dividend.

We have used the ratio $\pm(\mathrm{ID}/\mathrm{WD})$ to indicate the magnitude test, rather than ID as a fraction of WD, in order both to minimize the size and complexity of the two flow charts, and to preserve the significance of the polarities of the test magnitudes. Although expressing the test of block 2(a), for example, as $\left|\mathrm{ID}\right| : \left|\frac{\mathrm{WD}}{\mathrm{R}+1}\right|$ would make it more authentically a "magnitude" test, considerable "feel" for the essence of the magnitude test itself is lost by the use of the absolute symbols.

There is some value in presenting perfectly general flow charts such as Figs. 1(a) and 1(b). The almost complete duality of non-restoring and restoring division, and of negaradix and posiradix notation, is clearly re-

negative radix arithmetic continued

vealed, emphasizing that negaradix non-restoring and posiradix restoring division are both "natural," that is, the exponent of the coefficient of the weighting factor, k, is constant (such that the weighting factor can be a power of the radix, r^i), and the operation is constant (always subtraction). Having demonstrated these interesting relationships, and provided a graphic link between the elusiveness of negaradix non-restoring division and the certainty of posiradix restoring division, we can leave generality behind and take advantage of the simplicity that can be obtained by being specific. Before doing so, however, we shall examine one final important difference between the flow charts of Part 5 and Fig. 1(a).

Adjusting The Final Quotient And Remainder

With only the polarity test, we know that a final non-zero remainder will be of the correct polarity if we have an even number of quotient digits, and of the wrong polarity for an odd number. The flow chart for this rule is given in Fig. 4 of Part 5; it shows that if the remainder is not proper, a restoring operation on both

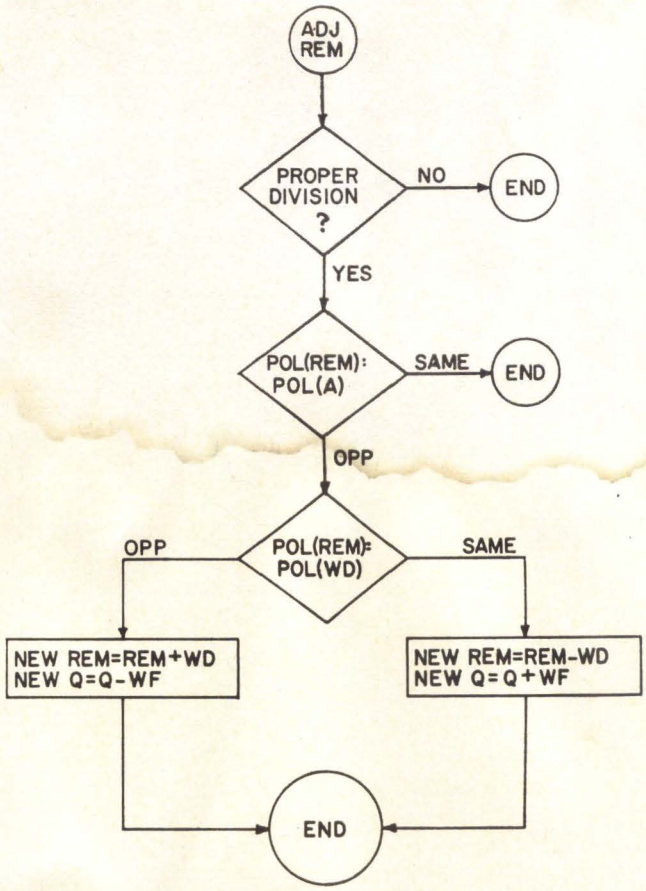

Fig. 2 Flow chart for adjusting remainder and quotient for proper division in the magnitude test, non-restoring algorithm.

TABLE 2

FINAL OPERATION TO PERFORM PROPER DIVISION

Remainder	Dividend	Weighted Divisor	Adjusting Operation On: Remainder (Using Wtd. Divisor)	Adjusting Operation On: Quotient (Using Wtg. Factor)
+	+	+	None	None
−	+	+	Add	Sub
+	−	+	Sub	Add
−	−	+	None	None
+	+	−	None	None
−	+	−	Sub	Add
+	−	−	Add	Sub
−	−	−	None	None

remainder and quotient will make it proper. However, if we include the magnitude test in the algorithm, the polarity of a final non-zero remainder is not predictable, and so neither is the adjusting operation, which must be determined by the polarities of remainder, dividend, and the weighted divisor. The operations required to obtain a proper quotient and remainder is given by the truth table, Table 2; the weighting factor and weighted divisor of the final pass are used as operands. The procedure is shown in the flow chart of Fig. 2.

While it is desirable to be able to perform an adjusting operation on an improper division, it may not always be desirable to do so. Although the results of such a division are not, by definition, proper, they are, nevertheless, arithmetically correct, and from a computer point of view it may be more advantageous to leave the results of an improper division in improper form. The results of an improper division can be used to develop additional quotient digits which can simply be appended to the more significant part without doing arithmetic, whereas the adjusted proper result cannot be so used. This is especially true in many digital computers and computer applications, where extended-precision results are often required. It would seem reasonable in a computer to provide one instruction for unadjusted division and a second instruction either for the adjustment only or for adjusted division.

Easy adjustment and extended precision are important features of negative radix division. In a digital computer using conventional complementary notation, the result of a division may be not only improper, but arithmetically incorrect. A rather elaborate little subroutine may be required in such a computer, to obtain results which are arithmetically correct, which may then easily be adjusted to be proper.

It should be noted that the correction to the quotient must be made upon the entire quotient, adding or subtracting the weighting factor. The adjustment cannot be made to the least significant quotient digit alone, since carries (or borrows) are possible.

Next month, we shall conclude this extended treatment of the division operation and reach our goal of a manual algorithm for negaradix division.

MASS CORE STORAGE

A multi-million bit ferrite core memory system is seen to fill the speed gap between the extremes of nanoseconds-per-access and milliseconds-per-average access.

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The recent installation of a Fabri-Tek MT mass core storage system at the Massachusetts Institute of Technology points up a significant development in computer memory usage techniques. Ten years ago, a capacity of several hundred thousand bits of high-speed main memory was sufficient for most computer systems. Neither hardware nor software was sophisticated enough that more capacity was economically feasible. During the past decade this has changed rapidly. First, the cost of basic storage elements has been reduced. Second, manufacturing and testing techniques and procedures have been improved greatly. Third, there has been an improvement in semiconductors and their cost is much lower. Fourth, new organizational innovations have been devised. Fifth, and probably most important, system designers and programmers have been demanding additional memory at an economical price.

The results of these demands are various. Planar thin-film and plated-wire memories show hope as the primary devices for very high-speed main memories. However, for small storage requirements, integrated circuits are making inroads. Moreover, the ever-present ferrite core is proving a worthwhile element even in the 500 nanosecond cycle time range of operation. High-speed memories are still quite costly when compared to the storage media used for the other extreme of the cost/speed spectrum where demands are for billions of bits at significantly lower costs. At this end of the spectrum, advanced drum and disc systems have been developed.

A third concern is with memories that accommodate the speed gap between the extremes of nanoseconds-per-access and milliseconds-per-average access. Here, Fabri-Tek foresaw a need in mid-1964. The industry had slow memories that were about 10^4 times cheaper than the fastest memories available; however, these devices had an average access time of 10^5 times slower. What was needed were capacities of up to 20 or 30 million bits of storage, operating at one quarter to half as fast as main memory, but at a sufficiently lower cost. Just what is this cost, and, is the economically-required cost of the device technically feasible? Fabri-Tek believed at that time that such a memory could be built and sold for two to three cents per bit and that a market existed at that price. Experience showed that the ferrite core was a satisfactory memory element and that production techniques were enough advanced to attain these goals. The development program at Fabri-Tek has proved this to be true. A 65,536 word by 20 bit prototype, operating at 5.5 microseconds per cycle, resulted from initial development efforts. Discrete components were used throughout the electronics and the stack was constructed of 30 mil O.D. ferrite cores. The memory was two-wire, 2½D in organization which proved to be economical to produce in very large arrays. The system was described in the April 1966 issue of *Computer Design*.

An order for a 262,144 word by 40 bit mass core store was received in the fall of 1965 and this memory is now installed and operational at MIT (see Fig. 1). During the acceptance testing period this memory was available to the customer 98.9 percent of the time (measured over a 30-day period). The full-cycle time of this memory is 2.75 microseconds. To meet the speed requirement, fast switching complementary transistor integrated circuits are used for a majority of the logic functions of the memory. Also, integrated circuits are used for the final sense amplifiers. All drive circuits consist of integrated circuit decoding inputs and discrete transistor high-current drivers.

This particular memory is designed to interface as an extension of main memory with Digital Equipment Corp.'s PDP-6 computer. However, the basic design of the memory is such that the interface is easily redesigned for use with other families of computers. The design of the MT series allows for several word capacity and word length configurations. Memories are available with word lengths from 20 to 120 bits and total bit capacities from 2.5 to 20 million.

Just what comparative advantages mass core storage has over other bulk storage devices is not entirely known as yet. The factors that are most evident are the absence of latency and addressability at either the word or byte level. However, what must really be considered is: What possible improvements (lower costs and faster, more efficient computer system operation) result from incorporating an intermediate speed memory with main memory and peripheral bulk

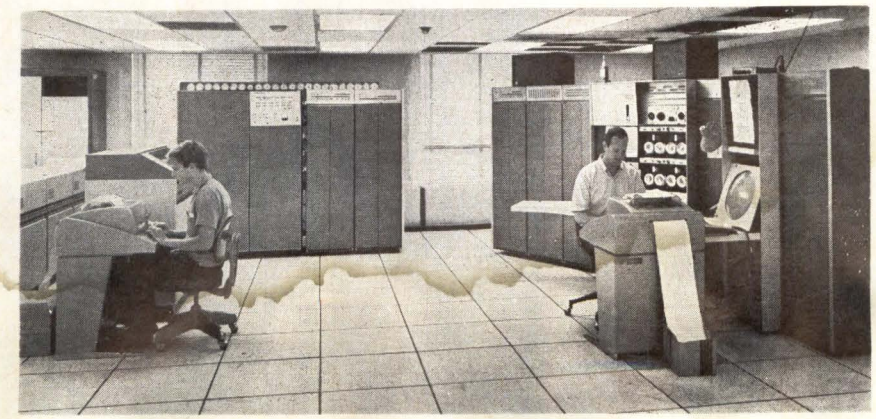


Fig. 1. Fabri-Tek's MT Mass Core Memory is shown in the left background as it relates to the total system configuration of the PDP-8 computer at M. I. T.

storage? According to computer systems designers, main memory need only be large enough to feed the central processor continually with instructions and data. Entwined in making an evaluation of how much memory is needed are considerations of the rate at which main memory is accessed (the execution rate) and how fast main memory information can be exchanged with peripheral memory information.

Computer systems designers are beginning to believe that the real answer for cost/speed/performance optimization is the creation of a memory hierarchy. Fabri-Tek feels its MT mass core memory system is the tool that allows the "tailoring" of this hierarchy for a number of large data processing configurations. The MT will eventually establish itself as a specific product, much the same as tape decks and rotating devices have. Systems designers will incorporate mass core storage in a number of ways resulting in the optimum solution for various data processing applications. Fabri-Tek's optimism is based on success in making cost reductions, and on the encouraging results of several experiments using mass core memories with two different large computer systems. These experiments project probable job time savings of from 30 percent to 60 percent in large job stack situations. The savings are largest when job priorities are well defined and when a large variety of data handling requirements exist. Job priority is dependent on frequency of use and urgency.

The mass core store can be used to extend the computing power of a large system. By relating the expected job loading profile to cost and speed, the configurations giving the desired performance can be determined. These configurations may use mass core storage for extension of main memory, block transfer interchange of main memory information, data collection and distribution for small remote processors, sharing of storage for multiple processors, or data buffering between main memory and peripheral bulk storage devices. Furthermore, one system may even use several combinations of these configurations. Several large time sharing computer installations have done this. A number of additional features are possible through logic design. For example, interleaving of several mass core memories and multiple-word read-out, and sophisticated priority schemes such as first-come-first-served, ordered priority, and automatic assignment of priority allow considerable increases in throughput. These features can be designed into the memory controller which may, in some cases, be only a re-design of an existing I/O controller.

Most advances in ferrite core and thin-film technology have been directed towards increasing the operational speed of memories. When the need arose for low per-bit costs, some of the same technological improvements could be employed. In addition, a new memory organization and very large magnetics module configurations were required to achieve the desired cost goals. However, these requirements result in operation at slower speeds because of increased back voltages, increased stack delays, and more sophisticated sense amplification and strobing. The design objective of the mass core storage system was to make the trade-off between memory cycle time and per-bit cost which would most satisfactorily fit the needs that are developing in the speed gap between very high-speed main memories and the very slow rotating peripheral memories.

Third generation medium-to-large computers have normally from one to 20 million bits of internal main storage. Cycle times are from 0.5 to 2.0 microseconds per cycle. Maximum module size is in the order of 65,536 words by 72 bits (approximately 5×10^6 bits). From these guidelines, a minimum mass core memory of 2.5×10^6 bits was chosen as the lower size limit. With cycle times of two to eight microseconds as a goal (a speed differential of one quarter to one half as fast as main storage units), the maximum low-cost single memory unit feasible was 20×10^6 bits (262,144 words by 80 bits). Units of this size appeared to fit the market that was developing. Since the initiation of this development program, the practical speed of operation of the resulting Fabri-Tek mass core memory has increased to two to three microseconds per cycle

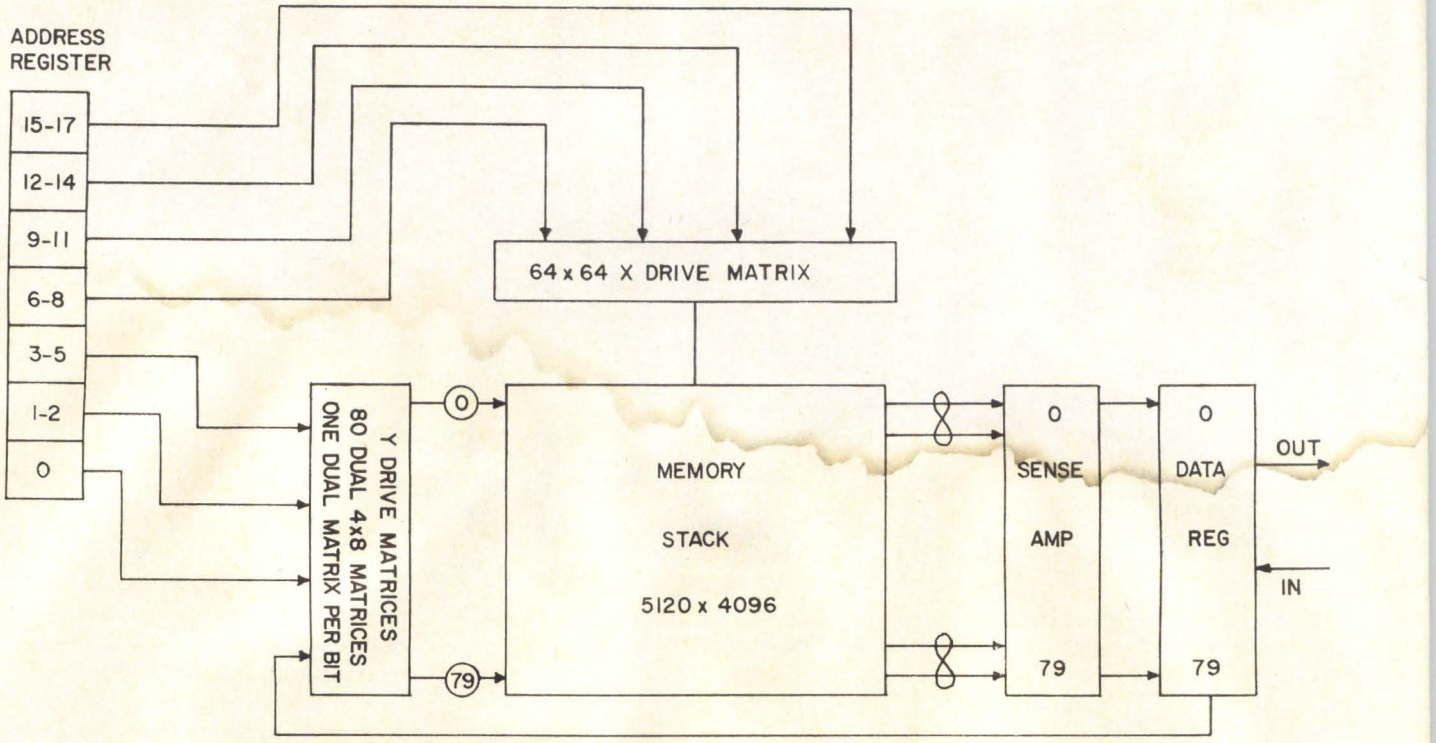


Fig. 2. Block diagram of Fabri-Tek's mass core memory.

TABLE 1

GENERAL SPECIFICATION OF THE MIT MASS CORE MEMORY

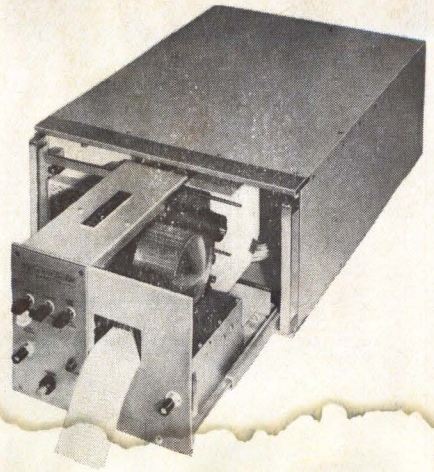
MEMORY TYPE	COINCIDENT CURRENT, FERRITE CORE 2½D SELECTION.
CAPACITY	262,144 WORDS AT 40 BITS PER WORD.
MEMORY CAPABILITIES	FULL CYCLE, RANDOM ACCESS DURING NORMAL OPERATION. SEQUENTIAL ACCESS DURING SELF-TEST.
MEMORY CYCLES	CLEAR-WRITE (FULL CYCLE LOAD) READ-RESTORE (FULL CYCLE UNLOAD) READ-PAUSE-WRITE (FULL CYCLE MODIFY)
CYCLE TIME	CLEAR-WRITE 2.75 USEC MAX. READ-RESTORE 2.75 USEC MAX. READ-PAUSE-WRITE 2.75 USEC PLUS MODIFY TIME.
ACCESS TIME	65% OF CYCLE TIME
OPERATING TEMPERATURE	60°F TO 90°F
STORAGE TEMPERATURE	−20°C TO +65°C
RELATIVE HUMIDITY	10 TO 90 % WITHOUT CONDENSATION
DIMENSIONS	LENGTH — 50 INCHES HEIGHT — 69¼ INCHES WIDTH — 26¼ INCHES
WEIGHT	1500 POUNDS

at no cost increase over original design goals.

From an analysis of four-wire coincident current memories, it can be shown that a majority of the costs are in the core stacks. At very large sizes (10^7 bits and above), core stacks account for about 80 percent of the total cost. It became evident that stack costs must be reduced to obtain any significant cost improvement. Thus, an organization which allows a trade-off between stack costs and circuitry costs would be beneficial.

Therefore, the Fabri-Tek mass core design approach, first developed in 1964, employs a two-wire stack design and a 2½D electronics organization capable of sensing, as well as current driving, on one of the two wires. A cost breakdown of a memory shows that four major criteria are involved, and the two-wire design using a large memory plane allows cost reductions in three of these criteria:

• Ferrite Core — since the memory speed is relaxed, core peaking time and switching time are not as critical. The elimination of the inhibiting function improves current margins and, hence, relaxes delta noise requirements. Each of the above-mentioned factors improves core yield and, hence, reduces core cost.



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. . . with a reliability that hasn't been matched yet . . . maintenance free, economical operation after thousands of hours in use.

And there are seven basic printer types to choose from. In each printer type, there's a wide range of models to fit almost any requirement—even for ticket printing. Here are some basic models:

TYPICAL PRINTER MODELS

Basic Model No.	Maximum No. of Columns	Print Rate In Lines Per Sec.	Printable Characters	
			Numeric	Alpha-Numeric
120A	1	20		√
812D-4	4	12	√	
812D-6	6	12	√	
812D-8	8	12	√	
812D-10	10	12	√	
1200	12	20	√	
1600	16	20	√	
1600	16	30	√	
1600	16	40	√	
2200	22	20	√	
2200	22	30	√	
2200	22	40	√	
2200	22	20		√
3200	32	20	√	
3200	32	30	√	
3200	32	40	√	
3200	32	20		√

Request Engineering Data Sheets for complete specifications. For basic application information, request Engineering Guide 2041B.

FRANKLIN electronics, inc

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CIRCLE NO. 59 ON INQUIRY CARD

• Wire Stringing and Terminating — because only two wires are used rather than four, and because the first two wires are easier to place than the last two, a reduction of greater than 50 percent is obtained in stringing cost. The use of large planes reduces the number of connections, or wire terminations, per bit. For example, a plane of 256 x 1280 would have about 10 connections per 1000 cores, but a 64 x 64 array would have about 62 per 1000. The economic advantage of large planes is evident.

• Test and Rework — testing can be automated quite readily. There is benefit with larger planes in reducing testing costs, because the time needed to install the plane in the tester, measured on a per-bit basis, is reduced. With larger planes, rework tends to be increased, somewhat. However, the simplicity of the two-wire scheme and the good margins obtained, as mentioned above, greatly alleviate the need for substantial rework. Memory system testing for 2½D organization is very similar to that of 3D memory systems.

• System Organization — the system organization used in Fabri-Tek's mass core memory allows for a simplified memory stack at some increase in circuitry cost. However, in a large-capacity memory, the circuitry cost-per-bit attained is still quite low. The principal reason for this is that the 2½D selection scheme allows the use of an efficient near-square stack array and yet takes advantage of the economies of coincident current read selection. This technique, combined with a sensing design which allows one sense amplifier and data register to serve up to 262,144 bits, makes the design of a 20-million bit memory practical. The block diagram shown in Fig. 2 is an organizational breakdown of a full-sized Fabri-Tek MT mass core memory. The memory contains 262,144 words of 80 bits. Table 1 lists the general specifications for the 262,144 word by 40 bit memory which is in operation at MIT.

This discussion does not cover all of the possible applications for a mass core memory. Fabri-Tek believes that computer system designers will be finding many applications and new configurations for which a mass core memory will prove to be the best storage device available.

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VARO

CIRCLE NO. 60 ON INQUIRY CARD

NEW PRODUCTS

DIGITAL LINE RECEIVER

New integrated circuit is a digital line receiver for military/industrial logic applications requiring high noise immunity. Designed primarily as a signal discriminator at the end of a coax transmission line in digital data systems, this circuit is also useful as a voltage comparator. Consisting of two gates driven by a differential amplifier, it has a TTL input and complementary outputs compatible with DTL and TTL logic. Input threshold is set by the differential amplifier reference voltage which may be adjusted over a 3 to 4.5 volt range. Propagation delay time is typically 40 nsec at 25C. Nominal supply voltages are 3.6 volts bias, +5 volts gate supply, and +12 volts differential amplifier supply. Typical power dissipation is 100 mw. Siliconix Inc., Sunnyvale, Cal.

Circle No. 260 on Inquiry Card

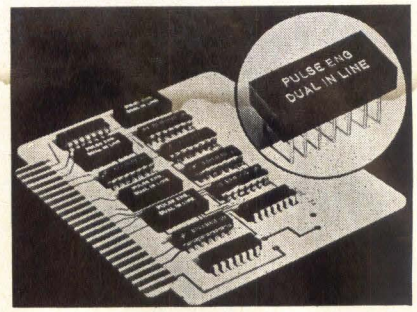
OPTICAL CODE READER

Optical code readers will produce punched card EDP input records at speeds up to 15 times faster than manual keypunching, according to the manufacturer. The unit reads information in bar code language recorded from plastic cards and variable keyboards on source documents and automatically converts the numerical values to Hollerith Code. Converted input data is punched into a separate output tab card. An alphanumeric keyboard permits manual entry of information into the punched card to supplement the automatically scanned numeric data. Tab cards are fed from a 500-card shuttle feed hopper into the read station, operating in a "demand" mode from the card punch. Addressograph Multigraph Corp., Cleveland, Ohio.

Circle No. 268 on Inquiry Card

DUAL IN-LINE TRANSFORMERS

A new approach to packaging pulse transformers to be compatible with integrated circuits has been introduced. The dual-in-line module consists of three transformers which can provide DC isolation, impedance matching, signal inversion, current or voltage gain, and common-mode rejection. The modules, which utilize the same board space and pin



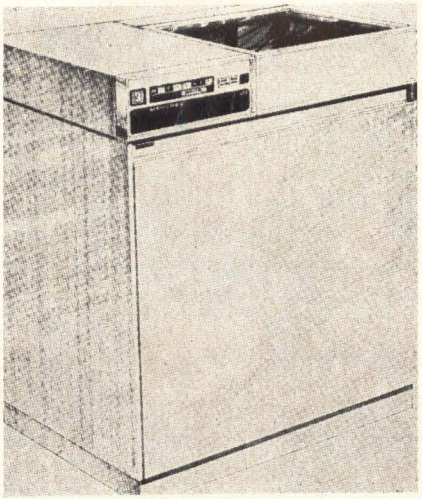
layout as a dual in-line integrated circuit, find applications as memory line drivers, common-mode chokes, floating switches, and for general purpose coupling. The new transformer modules are priced at $14.00 in quantities of 1 to 9. Delivery of prototype quantities is from factory stock. Pulse Engineering Inc., Santa Clara, Cal.

Circle No. 234 on Inquiry Card

CABINET COOLING BLOWER

Cabinet blowers for cooling electronic cabinets and consoles are self-contained, comprising a cabinet housing the blower mechanism, an efficient, washable filter, and a satin-chrome grille. The units may be installed easily in a standard electronic cabinet. Typical model is capable of delivering 310 cfm at 0″ s.p., and 220 cfm at 0.5″ s.p., in a cabinet occupying only 5.25 inches of panel space. The same unit is also available in a recess model occupying only 3.50″ of panel with the same air delivery. All ratings are made with the filter and grille installed. Features of the units include the use of force-cooled thermal-overload-protected ball-bearing motors that are fungus, moisture, and corrosion resistant; stainless steel shafts are used exclusively. Electronic Cooling Devices, Inc., Van Nuys, Cal.

Circle No. 258 on Inquiry Card



AN OEM DISC DRIVE

Designed to be compatible with the IBM 2311, a new OEM disc drive combines an economical drive mechanism with read/write electronics. The unit will read/write IBM's 1316 or Memorex's Mark 1 disc packs. One, two, or more drives can be connected to a computer depending on the size, speed, and controller design. A separate magnetic head is provided for each of the ten recording surfaces. Double frequency read/write circuitry is provided and the user's I/O controller can communicate with the device at the first level interface using standard logic levels. The data format allows for variable length records. The drive unit is designed to be connected in "chain" fashion. Supplied with the exact adapter interface required for systems integration, the unit, designated the 630 Disc Drive, can be specified in any configuration from console to relay rack mounting. Peripheral Systems Corp., Subs. of Memorex Corp., Sunnyvale, Cal.

Circle No. 201 on Inquiry Card

Anything the 810A can do,

the new 810B can do twice as fast.

Over 50 SEL 810A, 16-bit computers have been supplied for data acquisition and control. Now meet the SEL 810B, with twice the speed of the A. Yet only about 20% more in price. Same great features: all integrated circuits, 2 levels of priority interrupt, memory expandable to 32K, I/O typewriter, high-speed hardware multiply and divide, and real-time I/O structure. And the software package of the 810B has been proven in the A.

Fixed point execution times of the B are: add/subtract—1.58 microseconds; multiply—4.74 microseconds; divide—6.32 microseconds; cycle time—790 nanoseconds. If you don't need the speed of the SEL 810B, buy the A. For either, call or write: Systems Engineering Laboratories, 6901 West Sunrise Blvd., Fort Lauderdale, Fla. 33310. Area Code 305 587-2900.

Systems Engineering Laboratories

See the 810B at FJCC Booth D1-2-3-4.

CIRCLE NO. 61 ON INQUIRY CARD

NEW PRODUCTS

TELEMETRY DATA HANDLING

A new signal conditioner was designed to prepare time-multiplex telemetry signals for computer entry. Signal conditioning may be performed manually or under complete computer control through a unique interface permitting direct communication and control by a computer. The unit recovers time-multiplexed serial PAM or PDM pulse trains in the presence of noise, automatically generates pulse and frame synchronization, and converts each incoming data sample to a 12-bit parallel digital word. Output data include synchronization and status information to allow simultaneous routing to quick-look facilities and real-time computer. It can handle PAM channel rates from 1.0 Hz to 50 kHz and PCM rates from 10 Hz to 10 kHz. Electro-Mechanical Research, Inc., Sarasota, Fla.

Circle No. 219 on Inquiry Card

PC CARD FRAMES

PC card frames feature ½" spacing and ease of assembly which was designed primarily for circuit cards which are not "profiled," i.e., having connector tongue the same width as the rest of the card. A special feature is the method of connector retention; recesses are provided at the rear of the mouldings in which the ear of the connector is positioned. Two bars are used to retain all connectors thus reducing assembly time. Where it is necessary to use profiled cards, separate connector rails are available. A single tier 3½" unit (19" or 22" mounting standard) accepts a card 2. 495 x 4. 75. A 7" high unit accepts cards 6⅛ x 4¾ with direct connector mounting. Double tier racks and split racks accepting both card sizes are available. Vero Electronics, Inc., Farmingdale, N.Y.

Circle No. 224 on Inquiry Card

MILITARY FLATPACK IC's

Linear integrated circuits offering full commercial electrical parameters are now available for military use in low-cost FLATPAK units. These monolithic circuits, the U3H7702313 (uA702B) and U3H7710313 (uA-710B), feature the complete range of commercial electrical properties in the 0 to 70 degree centigrade range, plus additional specifications over the full −55 to +125 degree centigrade military range. All units are 100 per cent tested at both temperature extremes. The units will be priced in quantities of 100 to 999 at $9 for the uA702B and $16.80 for the uA710B. The prices are said to represent a considerable reduction from standard military grade prices. This special line was developed for those customers working on military projects where components must meet full temperature requirements although the equipment involved will operate in the 0 to 70 degree temperature range. Additional applications for the uA702B and uA710B stem from equipment operating over the full temperature range, with less stringent electrical performance requirements. These devices are now available. Fairchild Semiconductor, Mountain View, Cal.

Circle No. 245 on Inquiry Card

PROGRAMMABLE PULSE GENERATOR

Programming of a new pulse generator is accomplished by inserting diode pins into a sixteen by twelve program matrix board. The model SQ-250 operates at stepping rates from 10 mc to 1 kc and has twelve parallel output channels. Sixteen time steps constitute a single pass through the program. The cycle may be started again by means of an external control pulse or by a built-in cycle initiate clock. As a clock and controller for memory testers, the SQ-250 accommodates any system which requires sequencing. The new programmable pulse generator is said to be particularly useful in testing logic networks for hazards and investigating the consequences of irregular duty cycles. Adar Assoc., Inc., Somerville, Mass.

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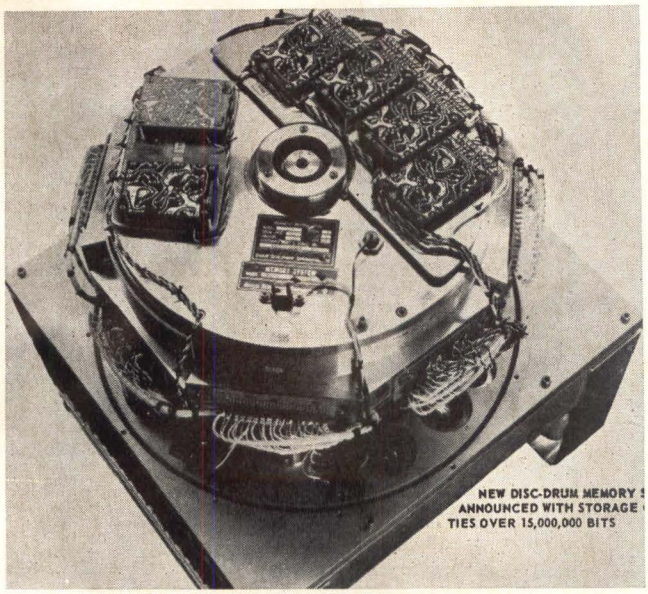
NEW PRODUCTS

RECORDING LENSES

CRT relay lens transfers a flying spot scanner raster to a copy station. Reflected energy, modulated by the object copied, is recorded and stored in a computer. The data is played back to modulate the flying spot and recreate the copy on other medium. The lens (P/N34489) is corrected for a P16 phospher and produces a two times magnification at a 39″ total track length. Resolving power exceeds 85 1/ppm. Pacific Optical, L. A., Cal.

Circle No. 222 on Inquiry Card



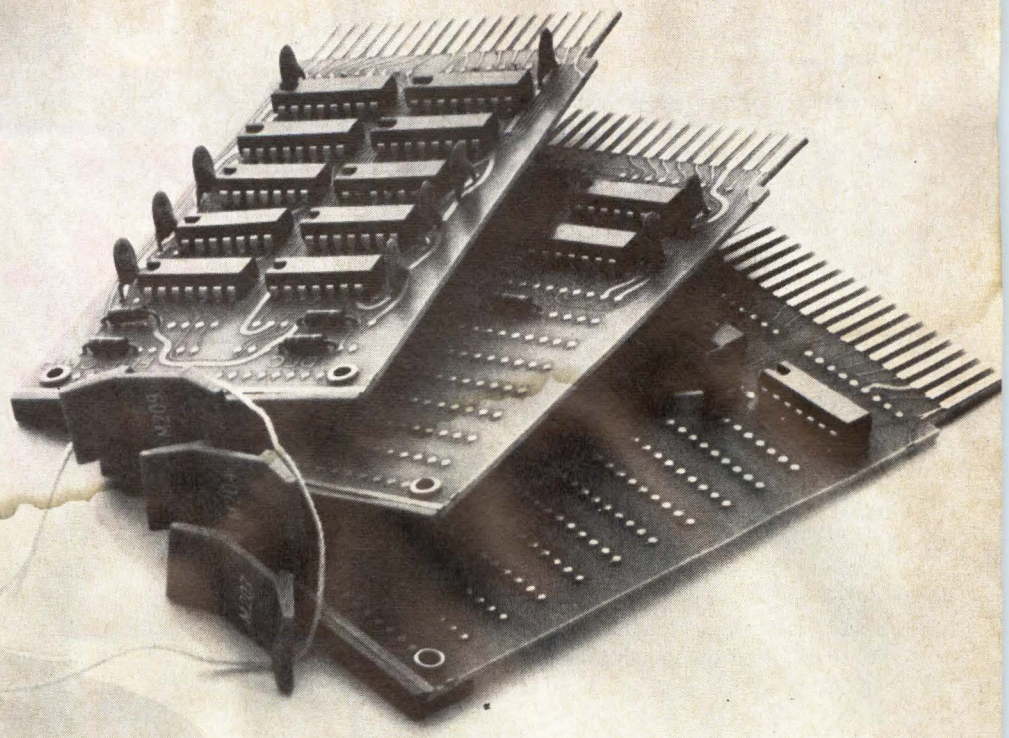
DISC-DRUM MEMORIES

An improved series of disc-drum memories was designed to increase the efficiency of mass storage and random-access computer applications. The new systems, designated the DDC 7300, is rated at up to 15.36 million bits with an average access time of 8.5 milliseconds. The new series 7300 is said to combine the high storage capacity of magnetic discs with the speed and reliability of magnetic drums. Volumetric efficiency of the disc unit allows maximum data density in a package less than ½ of conventional drum size and weight. Each disc has a rated capacity of 3.84 million bits on its 128 data tracks of recording surface. With four discs, up to 512 data tracks are available in a single unit.

The entire drum is shock-mounted in a hermetically-sealed enclosure which provides a controlled environment protected from dust, moisture, and other forms of contamination. The unit is designed for mobile, airborne and mil spec applications. Recording heads are organized into groups of 64 and each group services one disc surface. The heads never touch the recording surfaces and require no field adjustments. Digital Development Corp., San Diego, Cal.

Circle No. 226 on Inquiry Card

CIRCLE NO. 65 ON INQUIRY CARD →



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And the prices. Lowest cost per gate in the industry. And we're not afraid to publish them.

M Series Price List

Type	Function	Price
M050	12 — Lamp Driver	$31.00
M113	10 — 2 Input Nand	23.00
M115	8 — 3 Input Nand	24.00
M117	6 — 4 Input Nand	24.00
M121	6 — And/Nor Gates	25.00
M161	BCD to DEC/BIN to Octal Decoder	60.00
M203	8 — R/S Flip Flops	32.00
M204	4 JK Flip Flops, General Purpose Counter	36.00
M206	6 D Type Flip Flops	42.00
M207	6 JK Flip Flops	42.00
M208	8 Bit Shift Register	84.00
M209	8 Bit Up/Down Counter	84.00
M302	Dual Delay Multi	46.00
M401	Variable Clock	55.00
M502	2 — Negative Input Conv.	26.00
M602	2 — Pulse Amplifiers	28.00
M617	6 — 4 Input Power Nand	27.00
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Circle No. 230 on Inquiry Card

FLAT PACK IC CARRIER & CONTACTOR

A protective carrier and contactor for 14 lead ⅜″ x ⅜″ flat-pack integrated circuits, has been developed to allow long period aging and burn-in applications for environmental and ambient testing of flat-packs over −65C to 150C temperature ranges. The carrier has index notches for simple and positive error-free alignment with the polarization studs of the contactor. Although leads are fully protected by the carrier, precise designing allows them to be exposed to the probing test contacts of the 029-302-01 contactor. Continuous, reliable contact is ensured by the support provided by the contactor lid across the entire surface of the carrier during tests. The contacts are wiping type Ni/Au plated Beryllium copper with a typical service life in excess of 50,000 insertions. Once placed in the carrier by the manufacturer, the flat pack remains in the unit through all phases of environmental testing, marking and shipping. Similarly, when received by the user, the IC undergoes incoming inspection, testing and fabrication in the carrier, thus speeding up all phases of production. Price: Depending on quantity — Model 029-258 — $.055 to $0.15; Model 029-302-01 — $3.30 to $6.25. Barnes Development Company, Lansdowne, Pa.

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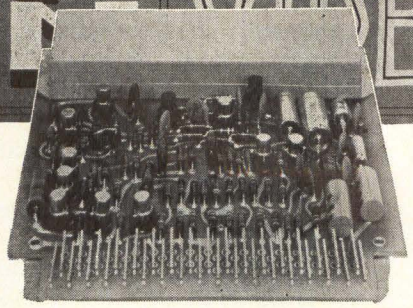

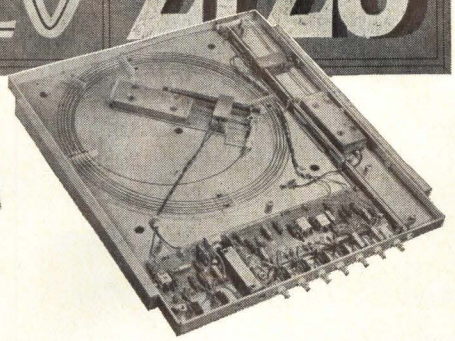

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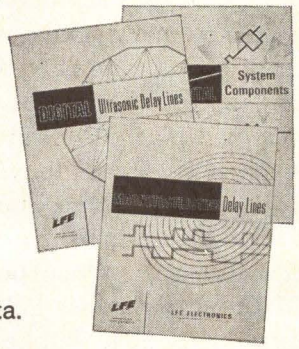

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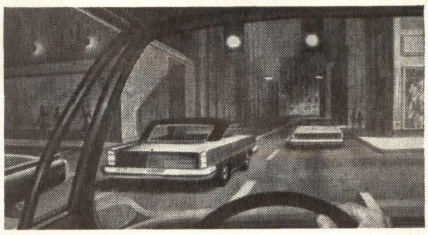

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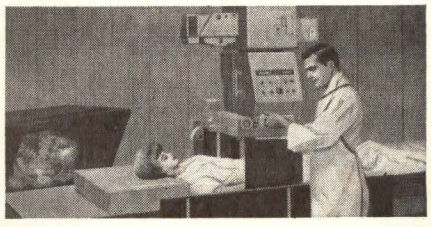

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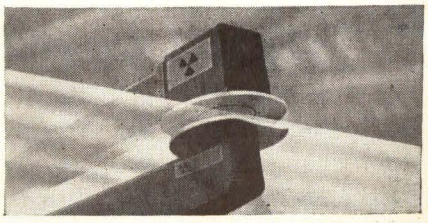
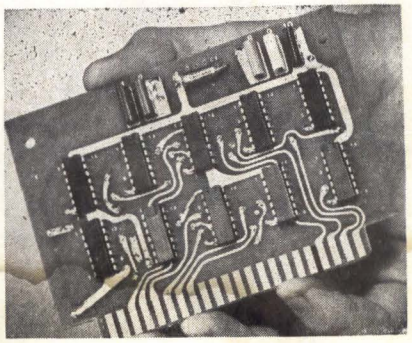


LABORATORY FOR ELECTRONICS, BOSTON, MASS.

NEW PRODUCTS



DTL I/C LOGIC CARDS

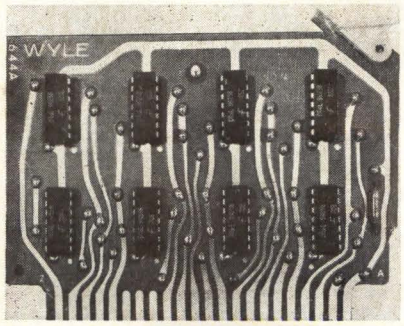
Available in both commercial and military versions, the new series 5000 logic cards provide high noise immunity, DC to 5 MHz operating speed and high circuit density. Monolithic integrated circuits and discrete hybrid combinations are mounted on a single 4.50 inch by 3.25 inch glass epoxy board for highest packaging density. Cards are fitted with 44-pin gold-plated card-edge contacts on standard 0.156 centers. Cards and connectors are keyed to prevent insertion errors, and color coded test points are provided to permit inspection of circuit functions. Test points accept a standard 0.080 inch probe. High noise immunity, typically 1.2 volts, over a 0°C to 70°C temperature range, is achieved by use of diode-transistor logic elements and local power line filtering. Fan-out up to 9 unit loads is typical with power stages available for driving up to 25 unit loads and up to 1000 pfd capacitive loading. A variety of standard cards are available including flip-flops, gates, high voltage and/or current drivers, extended time delays, wave shaping and wave generation, as well as interface capability with non-standard voltage level logic elements. All accessories, power supplies and hardware are offered. A standard card file accepts 39 logic cards for highest circuit density. Typically, a J-K flip-flop is priced at $9.50 and a gate at $2.50 in single board quantity. Normal delivery is from stock. The Roback Corporation, Huntingdon Valley, Pa.

Circle No. 210 on Inquiry Card

TAPE SPOOLER

All solid state, RS-1000 high speed punched tape spooler operates at 1000 characters per second with a full 2000 feet of tape on 10½ inch reels. Rewind speed is 2000 characters per second in either direction or while in reverse rewind without spilling or breaking the most fragile 5 channel tape. This is made possible through the use of full proportional servo controlled torque motors. Operational temperature range is 0° to 70°C. Any input line frequency from 50 to 400 cycles at 115 volt can power the unit with 230 volt optionally available. The Remex RS-1000 is priced at $2,195.00 with quantity discounts available. Deliveries are eight weeks after receipt of order. Remex Electronics, Hawthorne, Cal.

Circle No. 208 on Inquiry Card



REVERSIBLE COUNTER

Two new reversible counter cards have been added to a line of integrated circuit logic modules. One card contains one reversible BCD decade counter and the other card contains one reversible 4-bit binary counter. Both cards use DTL dual-in-line integrated circuits and operate at up to 5MHz. Operating from a single counting input, the counters are equipped with "enable" gates for forward or reverse control. Carry outputs are provided for tandem connecting of several counters which are completely presettable. Voltage levels are 0 and 4 volts ±1 volt. Ambient operating temperature range is 0°C to 70°C with storage temperatures from −55°C to +125°C. Overall board dimensions are 3¼" by 4½". Wyle Products Division, El Segundo, Cal.

Circle No. 232 on Inquiry Card

NEW PRODUCTS

DIGITAL CALENDAR CLOCK

Immediate delivery is offered for a new electromechanical digital calendar/clock which provides visual readout continuously and remote electrical readout on command of date and time information in classical six-figure form. The calendar/clock is designed for use in data reduction systems, to control batching, to aid in computing piece rates in all production processes, and in all types of data or material handling where a date/time base is required. Manual set-up switches on the front panel are provided to establish initial date and time information upon installation, or to enable swift corrections to be made in case of power failure or plant shutdown. In operation, the time level advances automatically and resets automatically on reaching midnight. Also at midnight (24:00:00), the date level automatically advances to the next day, to the next month, to the next year — all functions are completely automated. Each digit in both date and time levels has an insolated 11 line readout. This remote electrical readout capability can be made available to computers, printers and controls. The calendar/clock is available as a standard model with or without a time base generator, with a cabinet for desk mounting or without cabinet for 19" relay rack mount — or for 9½" panel mounting. Durant Manufacturing Co., Milwaukee, Wis.

Circle No. 225 on Inquiry Card

WORD GENERATOR

New generator supplies complete digital words composed of a combination of pulses, up to 100 bits long. By operating switches on the front panel of the unit, the content of the word is completely controlled. By using identical circuitry wherever possible in different pulse generators, necessary stocks of circuit cards and parts for repair and maintenance are substantially reduced. Extensive use of integrated circuits in the new word generators allows a lightweight, compact design (only 7 inches high, with width suitable for mounting in a standard rack). The word generators feature 100 bit capability in single or multiple channels. Bit repetition rate is variable to 10 MHz, with word lengths available as the product of any two integers from 1 to 10. Multiple channels with independent controls are available within the 100 bit limit, and programs can be set up with front panel switches. The series has the capability of bit programming, direct from a computer. Models available include single bit, single word, and gated outputs. Output amplitude is variable to 5 volts, positive or negative, with rise and fall times less than 6 nsec. Both RZ and NRZ outputs are available, and delay between RZ and NRZ channels can be supplied from 20 nsec to 80% of bit width. Bit width for RZ is variable from a 20 nsec minimum. Selectable bit synch output allows synchronization of an oscilloscope at any desired point in a full 100-bit word. Industrial Products Group, Texas Instruments Inc., Houston, Texas.

Circle No. 279 on Inquiry Card

MEMORY PLANE AND STACK TESTER

Automatic memory plane and stack test system features a built-in temperature chamber to provide a controlled environment for a core plane or memory stack under test. The system, designated M-205, is designed to test standard 2D, 2½D and 3D memories and is also capable of testing a wide range of sophisticated memories employing complex sense and digit wire geometries. Memory stack dimensions that can be accommodated with the M-205 range up to 256 x 256 x 128. In operation, the M-205 checks memory performance by subjecting it to its ultimate system environment. Memory response is measured at each address under imposed "worst case" electrical and logical conditions and the capability of each bit to store data with prescribed reliability is verified. The temperature chamber is mounted on top of a pedestal rack which houses all current drivers, termination panels, current and sense switches, and amplifiers. Temperature range is from −25°C to +80°C. Heating is provided by nichrome wire elements and CO_2 is ued to achieve sub-ambient temperatures. Additional features of the M-205 system include integrated circuit logic, decimal address control and direct digital readout, 75 volt current drivers, 50 MH_z sense amplifier, interchangeable solid state or reed relay switch modules. Pre-wired programming plugs supplied with the M-205 speed production testing by permitting rapid setup of the most commonly used "worst case" storage patterns. Computer Test Corp., Cherry Hill, N.J.

Circle No. 223 on Inquiry Card

NEW PRODUCTS

HIGH-SPEED TELEPRINTER

Providing high through-put with speeds up to 640 characters per second, a new flexible terminal printer interfaces with 201A, 201B, 202A, and 202B Data Sets. Customer options include automatic answering and a variety of "receive" and "transmit" supervisory control functions employing simplex, reverse channel, or full-duplex operation. Printing format is 32 columns using any code with up to 11 units. An exclusive non-ribbon ink roller is said to give 10 times the inking capacity of a conventional ribbon. Other features include all silicon circuits, a through-hardened steel type-drum, electronic vertical alignment adjustment, self-cleaning printing elements, and complete modular construction throughout, Di/An Controls, Inc., Boston, Mass.

Circle No. 233 on Inquiry Card

PHOTOELECTRIC ROTARY

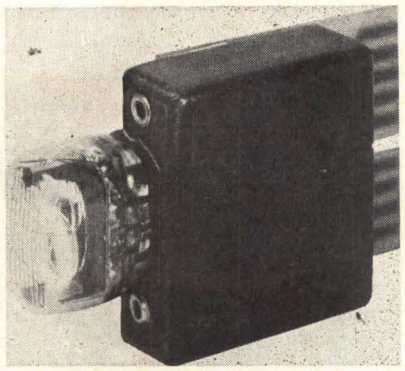
A new incremental solid state, photoelectric rotary encoder in a synchro size 11 package has been developed for applications as an electronic tachometer, or angular measurement device in computer, process control, machine tool control, and aerospace guidance systems. The compact unit (1.062" diameter by 1.125" length), packaged in a rugged all-metal case, incorporates Gallium Arsenide light sources for maximum reliability over a temperature range of $-55°C$ to $+100°C$ and shock in excess of 50 G's. Standard accuracy is ± 1 minute with pulse counts up to 1024 pulses per revolution. The encoder can fulfill the requirements of MIL-5272C and MIL-E-5400 Class 2. Priced from $348 each, the new encoder is available within 60 days after receipt of order. W. & L. E. Gurley, Troy, New York.

Circle No. 236 on Inquiry Card

AUTOMATIC FREQUENCY COUNTER

A new integrated circuit counter features automatic measurements from 300 MHz to 12.4 SHz and a direct 100 MHz counting range. This range and fully automatic operation was achieved by combining a built-in automatic computing transfer oscillator with a 100 MHz frequency counter. Readout of measurements in the 0.3 to 12.4 GHz range appear instantaneously in 8 digits (9 digits optional). Designed principally of integrated circuits, the Model 6316 has a 1¾ inch panel height, slide switches, an optional super high stability oscillator (5 parts in 10^{10} per 24 hrs), 9-digit readout, and other features that permit continuous remote operation in systems applications. Systron-Donner Corp., Concord, Cal.

Circle No. 227 on Inquiry Card



DISPLAY MODULE

A digit display module for use in high speed electronic counters and readouts accepts four-line BCD input code for single digit display on a neon glow tube. It is said to be readily adaptable as a building block for computer input/output, numerical control displays, and a wide range of digital instrumentation requirements. Offering monolithic integrated circuitry, an encapsulated package, and printing wiring with etched connections, the unit is said to be physically and electronically interchangeable with competitive models. It operates on the supply of 4.75 to 7 volts, and 200 volts for tube anodes. Integrated Circuit Electronics, Incorporated, Waltham, Mass.

Circle No. 231 on Inquiry Card

INTEGRATED CIRCUIT SOCKETS

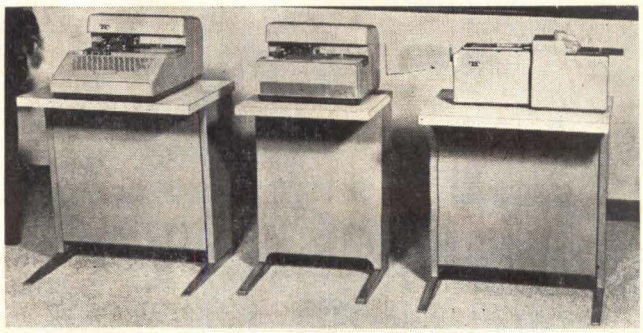
A new series of six dual in-line integrated circuit sockets has been designed for low cost mass production use. The new M-1000 Series of integrated circuit sockets, called "Uni-Pac", have universal mounting and packaging capabilities. They can be printed circuit board mounted with standard .100 x .300 pin spacing and have special snap-in features for mounting into punched aluminum or epoxy glass panels to ⅛" thick. The sockets are made for 14 and 16 pin dual in-line integrated circuits. Three types of terminations are available. They are designed with printed circuit type, .025" square wrap post type, and .008 conventional wiring type terminations. The one piece molded 14 pin socket body is approximately .850" long, .450" wide and .250" high, not including termination length. The 16-pin socket body is .100" longer. Two ejection holes molded into the body permit easy IC removal. Each "Uni-Pac" body is also molded with visual index slot which matches that of the indexing slot of the IC. Delivery of the M-1000 "Uni-Pac" Series is three to four weeks from receipt of order. Price range is dependent upon unit quantity, pin number (14 or 16), type of contact finish. Prices range as low as 15¢ each for a standard 14 pin unit with printed circuit terminations in large production quantities. Methode Manufacturing Corp., Rolling Meadows, Ill.

Circle No. 204 on Inquiry Card

NEW PRODUCTS

PUNCHED CARD DATA TERMINAL

Data can be accurately prepared, transmitted, or received in edge-punched card form with three new companion machines introduced by Teletype. The new CARData equipment has a variety of data communications applications, particularly where repetitive, fixed information is involved. Designed to supplement the uses of punched paper tape, the compact CARData equipment consists of a keyboard typing punch, a card reader and hopper feed, which automatically supplies individual cards into the reader. The punch and reader operate at 100 words per minute (10 characters per second) or less and utilize an 8-level code compatible with the United States of America Standard Code for Information Interchange (USASCII). The units are especially designed for use in systems where: data transmissions are of relatively short lengths; transmitted data must be subsequently separated for storage or other manipulation, such as stock withdrawal authorizations; individual cards have to be updated or replaced from



among many; data must accompany a shipment of goods; and where data byproducts, such as billing, inventory or accounting cards are needed to prepare business forms. The keyboard punch provides both typing and punching on the upper portion of single or fanfold cards in either an on-line or local condition. The keyboard punch is also capable of punching paper tape in on-line or local applications. The unit features a four-row keyboard similar to that of an ordinary typewriter and punches 10 characters an inch. Printing is along the upper edge above and six spaces behind the corresponding perforations. Cards in continuous form are automatically aligned in the correct punching position. The CARData reader, including a card collector, can be employed independently for transmitting data or mounted directly on a Teletype Model 35 ASR set if desired. In this latter application, it can be actuated from the keyboard of the ASR set to permit combining fixed data from the cards with variable data entered manually by the ASR set operator. Teletype Corp., Skokie, Ill.

Circle No. 202 on Inquiry Card

MICRO ZENER DIODES

Temperature compensated zener diodes in micro size have been developed which are electrically interchangeable with standard JEDEC types. Measuring only 0.075" in diameter and 0.125" long, these reference elements, designated the MTC series, are encapsulated in high temperature epoxy. Standard units cover the voltage range from 5.0 volts to 12.0 volts with similar electrical characteristics to EIA types 1N821, A through 1N935, A, B through 1N946, A, B. They are constructed on a unique, high strength "unibody" principle which according to the manufacturer, takes advantage of the best properties of alloyed and diffused construction. Standard units contain up to four integrated silicon junctions. Non-standard units can be provided to customer specifications to meet any voltage requirements up to 200 volts or higher. All units are said to meet the mechanical and environmental requirements for industrial and most military applications. They are supplied with either 0.020" diameter silver leads, ½" long, or with 0.004" by 0.020" gold plated weldable ribbon leads, ¾" long. Computer Diode Corporation, Fair Lawn, New Jersey.

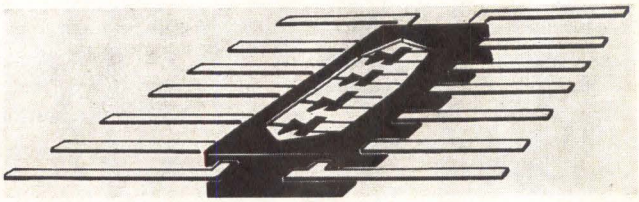
Circle No. 212 on Inquiry Card

HALF-WATT RESISTOR

A new flame-proof half-watt resistor, the FP half-watt, extends singular line of flame-proof tin-oxide film resistors in 2, 3, 4, 5, 7, and 10-watt sizes. The units won't burn under overloads of as much as 100 times rated power. Instead, they open, protecting the circuitry and system. Even with this singularity, prices of the flame-proof film resistors are only at the high end of the carbon composition resistor price range or just above. Resistance range of the half-watt addition to the FP line is 10 ohms to 470K ohms. Case size is 0.360-inch length and 0.138-inch diameter. Standard purchase tolerances are two percent and five percent. The half-watt has an especially favorable load life characteristic. Maximum resistance change after 1000 hours is only 1.5 percent. Except for the half-watt, the flame-proof resistor line exhibits a maximum load life resistance change of three to five percent after 1000 hours. Temperature coefficient of the complete line is 200 parts per million between −55 and 150C. In replacing wirewound units FP resistors provide required power, stability, low ohmic values and size. Their unique difference over silicone-coated wirewounds is their non-flammability, and they beat vitreous enamel wirewounds on price, according to manufacturer. FP resistors have won acceptance in printed circuitry because of their excellent hot spot characteristic. Because of this feature, the resistors don't require crimping to keep them off the board, and are ready as shipped for automatic insertion. In some equipment, they have been inserted 10 times faster than rectangular resistors, manufacturer said, at about 1100 per minute. The new half-watt FP is available in production quantities from the manufacturer. Electronic Products Division, Corning Glass Works, Raleigh, N. C.

Circle No. 215 on Inquiry Card

NEW PRODUCTS



FOUR JUNCTION FETS

Eight new 4-channel junction FET switches, designed primarily for switching applications, are also useful in amplifiers, voltage-controlled-resistor (VCR) and constant-current applications. Packaged four to a TO-84, the series offers a choice between separate or common-drain configurations, four r_{ds} and two V_P ranges in each configuration. Maximum pinch-off voltages are 5 and 10 volts; maximum ON resistances are 500, 250, 90, and 45 ohms. They feature low I_{GSS}, 0.1 and 0.2 nA max. depending on device type, and 0.05 and 0.1 nA max. $I_{D(OFF)}$ and $I_{S(OFF)}$. These n-channel junction devices provide several advantages: very low ON resistance per unit capacitance, trade off between V_P and $r_{ds(on)}$ to lessen the drive swing requirement, and low leakage. On special order, the manufacturer will package any of its junction FETs in a flat package. Immediately available from distributors, this G125F-G125F series is priced from $20.00 to $34.80 in 100 quantities. Siliconix Incorporated, Sunnyvale, Cal.

Circle No. 217 on Inquiry Card

HIGH-SPEED CARD READER

A new card reader with a 1500-card-per-minute reading speed reads standard 80-column punched cards in either Extended Binary-Coded Decimal Interchange Code (EBCDIC) or binary code. The Model 7140 reads cards serially by columns. The serial method is said to offer three advantages over parallel reading: (1) higher reliability because fewer components are needed, (2) greater accuracy because the card is guided by its long edge, and (3) faster availability of data because the reader need not read the entire card to obtain data punched in the first few columns. The Model 7140 consists of a photoelectric reader mechanism with its associated transducer electronics, housed in a free-standing cabinet, and a controller that provides the necessary interface between the reader and the computer input/output channel. Two program-selectable stackers facilitate card-stacking operations and afford a convenient means of separating cards that contain errors. This high-speed card reader is said to be especially useful in large, high-volume batch processing installations. Deliveries on Model 7140 Card Reader will begin in the fourth quarter of 1967. The unit sells for $24,000 and leases for $540 per month. Scientific Data Systems, Santa Monica, Cal.

Circle No. 206 on Inquiry Card

SERIAL MEMORIES FOR VIDEO DISPLAYS

A series of magnetostrictive serial memories, designated Type 3790, have been designed for video display application in computer terminal or peripheral equipment. Intended to function as CRT refresh memories for the storage of graphics and data in commercial or non-military applications these serial memories are self-contained packages including complete electronics and are said to operate well under wide environmental conditions including shock vibration, low or high temperatures and high altitudes. The casing consists of an aluminum casting fitted with a cold rolled steel cover, fully gasket sealed. Since terminals are arranged on one side only, a series of Type 3790 serial memories may be stacked. Per bit storage cost is approximately 1 cent. Deliveries range from 2 to 3 weeks dependent upon quantity. Cost is approximately $285 each. Andersen Laboratories, Inc., Bloomfield, Conn.

Circle No. 211 on Inquiry Card

DISC CAPACITORS

An improved line of Ultra-Kap disc capacitors that provide higher capacitance but smaller in size are said to out-perform the 3, 10 and 20V Ultra-Kaps which feature 100 times the capacitance of conventional ceramic dielectrics. Units are available with capacitance values of 0.01, 0.022, 0.033, 0.05, 0.068 and 0.1 MFD. Rated at 16V and 25V, these new disc capacitors offer outstanding capacitance versus temperature change stability (X5R) and can readily replace larger or more costly devices such as monolithic ceramic, low voltage ceramic discs and certain plastic film capacitors. Leakage resistance of the 16V and 25V units is 10 megohms — from 16 to 33 times greater than before. The maximum dissipation factor is 5% at 1 kHz. Disc diameters vary from 0.290″ to 0.760″ and all units have a maximum thickness of 0.156″. The low cost and compact size of these improved units make the Ultra-Kap most useful in a variety of bypass and coupling applications in the communications, military, medical, instrumentation and computer markets. Centralab, Electronics Division of Globe-Union Inc., Milwaukee, Wisc.

Circle No. 250 on Inquiry Card

BINARY TO BCD CONVERTER

Self-contained converter module capable of accepting pure binary data or the cascaded output of a prior BBC affords a 1-2-4-8-BCD output and the required number of decimals may be cascaded with no special circuitry additions. Conversion rate is dependent upon clock rate. Total conversion period is equal to the number of binary bits multiplied by the clock frequency in units of time. For example, a 10 bit binary work (sample) would require four cascaded BBC modules, each BBC representing a BCD digit. The module is 3½ inches by 2¼ inches by 1/16 inch and uses a 36-pin connector. Digital Data Systems, Chatsworth, Cal.

Circle No. 228 on Inquiry Card

NEW PRODUCTS

MILITARY CORE MEMORY

Random access core memory systems designed specifically for operational ship and shore based weapons systems are organized to be expandable from 512 words to 8,192 words, and from 4 bits to 2 bits. The memory is organized as a four-wire coincident current system and employs 22 mil lithium ferrite cores. It can be operated in any of the following four modes: clear/write; read/restore; read/modify/write; and read-only. Full cycle times of under 1.5 usec. are achieved over an operating temperature range of −30C to +85C. The memory has been designed in full accordance with MIL-E-4158C and is shock and vibration qualified according to MIL-STD-810A. Interface characteristics are compatible with DTL and TTL integrated circuit output voltages. Proprietary techniques have been employed to minimize the prime power required; for example, an 8K x 10-bit memory utilizes less than 100 watts of prime power. Designed to minimize maintainability problems in the field, the memory is packaged in functional plug-in assemblies, measuring 7¼" x 9¼". All modules, including the stack and power supply are designed to plug into a connector plate via an 82-pin and socket connector. A color-coded test strip is mounted across the top of each module, permitting access to all significant memory signals. A built-in exerciser is included in the memory system which allows testing of the memory under conditions of all ones, all zeroes, worst pattern, and worst pattern prime. Abacus Div., Information Control Corp., El Segundo, Cal.

Circle No. 283 on Inquiry Card

STANDARD DECODING DISPLAYS

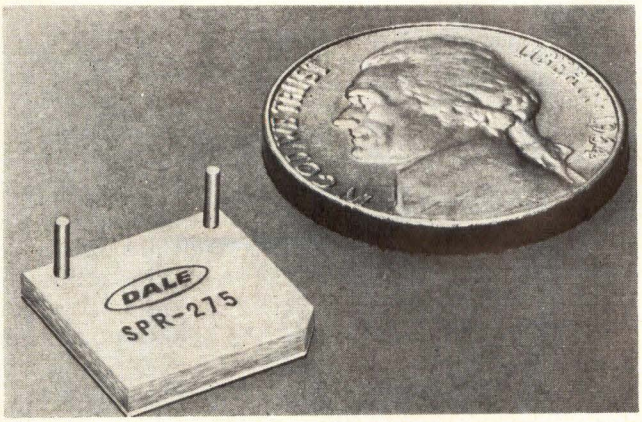
Decoding readouts are now available from stock in 2 to 6 decade assemblies. Said to be the brightest, most legible projection displays available on the market, the units come complete with decoding circuitry and memory and require only two connectors and a 6.3 volt transformer. They are delivered ready for panel mounting — already interwired, and feature direct interface with integrated circuits. The modules are based upon a tiny electronically-pulsed stepping motor that rotates an optical disc on which the numerals 0 through 9 appear. The light source, a high-power bulb, is always on. Pulsing the motor rotates the disc, causing different numerals to be projected in sequence on a brilliant, high contrast screen. All drive, decoding, and encoding circuits are included. Modules are assembled to customers' requirements and are normally panel mounted. Back apron electrical connections are included, eliminating all inter-decade wiring. Numex Corporation, Waltham, Mass.

Circle No. 203 on Inquiry Card

PC LAMINATES

A new line of copper-clad laminates can be fabricated into printed circuits at lower cost and with greater reliability, according to the manufacturer. The new laminate is tradenamed Catabond and is intended for the production of double-sided or multi-layer printed circuit boards which utilize plated through-holes. With a Catabond laminate, copper can be reduced directly on the substrate hole surface, completely eliminating the need for the customary steps of catalytic seeding and subsequent sanding. Further production economies are made possible by the fact that costly hole drilling can often be replaced by punching. Consisting of two sides of copper foil bonded to an insulating substrate, Catabond laminates are produced by a patented process which provides for the dispersion of a special catalytic agent throughout the substrate. This agent effects the bonding of copper to the non-metallic substrate. Since it is incorporated directly in the substrate, there is no need for an additional catalytic seeding operation. Five grades of Catabond laminates are presently available. These are produced to correspond with existing NEMA grades such as XXXPC, FR-2, FR-4, or G-10. Properties of Catabond grades are the same as the traditional grades. NVF Company, Wilmington, Del.

Circle No. 281 on Inquiry Card



POWER RESISTOR

Thinner than a nickel and smaller than a dime the SPR-275 twenty-one watt resistor with a resistance of .025 to 1K, within 5% tolerance has been designed to isolate line drive impulses and terminate lines within the demanding space requirements of a computer. Finer resistance tolerances are available, down to 1%. Mounted to a heat sink maintained within the computer at 75°C, its maximum temperature on the other side is 110°C at 21 watts. Terminals are 0.031 copperweld wire, 0.09 inch high for easy soldering. Optional configurations are numerous; the SPR-275 can take almost any shape to fit design requirements. Tested for ten days in accordance with MIL-STD-202, the SPR-275 had no failures in moisture resistance. Temperature coefficient is 100 parts per million. Dale Electronics, Inc., A subs. of The Lionel Corp., Columbus, Neb.

Circle No. 246 on Inquiry Card

NEW PRODUCTS

MICROMINIATURE P-C CONNECTORS

Two series of microminiature printed circuit card-edge connectors — the 600-2 for 1/32″ P-C boards and 600-6 for 1/16″ P-C boards feature the exclusive "Bellowform" contacts. Both types have 0.050″ center-to-center contact spacing, dual readout and terminations for soldering, welding, and conductive adhesives. Series 600-2 can be supplied with 20, 30, 50, or 64 dual contacts (40, 60, 100, or 128 terminals respectively); series 600-6 with 10, 14, 22, 40, 55, or 64 dual contacts (20, 28, 44, 80, 110, or 128 terminals respectively). Contact material is Beryllium copper with gold plate. Single piece body moldings are glass reinforced diallyl phthalate Type GDI-30 per MIL-P-19833 (Series 600-2) and Type SDG per MIL-M-14 (Series 600-6). Continental Connector Corporation, Woodside, N. Y.

Circle No. 216 on Inquiry Card

X-Y RECORDER

Human engineering techniques applied to the development of new X-Y recorder have resulted in a multipurpose instrument suitable for many different installations. Plug-in "function modules" permit the recorder to be quickly converted for use in a variety of applications. The manufacturer states that use of proven solid-state servo systems already in production and application of enclosed infinite-resolution slidewires instead of helical-wound resistance elements, high precision is insured, while deadband problems are eliminated. Either vertical or horizontal mounting of the recorder is possible, without special fittings or accessories. In addition, when the instrument is used as a tabletop unit, the recording surface may be angled to 45 or 90 degrees from the horizontal to allow visibility of the recording even when the operator is seated. Both 8½ x 11 inch and 11 x 17 inch charts can be used. Either X or Y axes may be geared to time function, while the interchangeable "function modules" permit quick and easy modification for the job at hand. Three modules are presently available: a single range signal-input module, a time-sweep/signal attenuator module and a multirange attenuator module. Terminal for remote control of time sweep are standard, as are pen lifters. Inking is provided by disposable plug-in ink cartridges. The vacuum hold-down system is exceptionally quiet, due to the use of controlled volume techniques. A nonconductive case of mar-resistant fiberglass enclosed the recorder. Instruments are now available for demonstration. Delivery is 90 days after receipt of order, price is in the $1,600 range. Industrial Products Group, Texas Instruments, Inc., Houston, Texas.

Circle No. 248 on Inquiry Card

LAMP HOLDERS

A unique family of R-lites — relampable holders and lens caps for the midget flange based T-1 ¾ incandescent and T-2 neon lamps — make it possible to replace and lens caps from the front of a panel without use of special tools. Five groups within the R-Lite Series are available, each for a wide range of applications and with a wide variety of special features. Eldema, Compton, Cal.

Circle No. 240 on Inquiry Card

CORE MEMORY

Small, high-speed 2½D core memory system is designed for OEM and non-severe military applications. The NANOMEMORY trademark 2650 is packaged in a 7″ high sliding drawer (including power supply and optional tester) which mounts into a standard EIA 19-inch wide cabinet. According to the Company, the new system is the smallest for its speed and capacity on the commercial market. A combination of integrated circuit electronics with a unique 2½D drive system gives the NANOMEMORY 2650 a cycle time of 650 nanoseconds and an access time of 350 nanoseconds. Silicon integrated circuits are used for all logic, addressing, decoding, timing, control, and sensing functions. The proprietary drive scheme for which a patent is pending is said to enhance system reliability and storage density. The system can handle up to 16,384 words x 18 bits, 8,192 words x 36 bits or 4,906 words x 36 bits, without any modification of the 7″ high x 19″ wide x 21″ deep configurations. For greater word capacity and extended word lengths, NANOMEMORY 2650's can be conveniently stacked. Use of a new magnetic selection technique enables stack connections to be significantly reduced — to the extent that all magnetics and system electronics are mounted on plug-in printed circuit boards. Core stacks as well as accompanying circuitry are therefore readily accessible for maintenance and can be quickly removed and replaced if necessary. All modules of a common type are directly interchangeable with each other and no module selection or adjustments are required to ensure stable performance over the operating temperature range of 5°C to 45°C. For further reliability, the use of a double keying technique prevents misorientation of printed circuit modules or insertion into an incorrect location. The 2650 also includes protection circuitry to ensure that no stored data is lost during power turn-on, turn-off or failure, and no damage can be caused by excessive internal temperature or DC voltage conditions. Front of rack access is provided to all system modules and wiring.

The NANOMEMORY 2650's high operating speed and compact packaging make it well suited for all applications where high reliability and simplified maintenance are required. Electronic Memories, Inc. introduced the first submicrosecond 2½D commercial memory system in 1964. This unit offers full cycle times down to 650 nanoseconds and capacities up to 16,384 words x 84 bits. Electronic Memories, Hawthorne, Cal.

Circle No. 249 on Inquiry Card

LITERATURE

Multi-purpose Keyboard Display

A self-contained input/output device that provides keyboard input and CRT display for SDS Sigma computers is described in a new data sheet. The multi-purpose keyboard display is designed to replace the teleprinter and provide a greater degree of flexibility for time-sharing, text-editing, and inquiry/response systems. Features of the keyboard display unit include high-speed character generation, a complete set of ASCII codes, simultaneous send/receive capability, and the ability to interface with standard communications services at speeds from 15 cps to 180 cps. Scientific Data Systems, Santa Monica, Cal.

Circle No. 316 on Inquiry Card

Magnetic Core Press

The Multipak Model 1104 Magnetic Core Press is described in detail in a new technical brochure. The Model 1104 is a multi-station press that was designed specifically for the production of memory cores and related ferrite devices. It can press up to 57,600 cores per hour. The unique single-action tool set design eliminates the need for an upper punch, which in turn reduces cost, improves dimensional stability, and simplifies maintenance. The six page brochure includes a description and photographs of both press and tool set. Operation is illustrated with cross-sectional drawings. Complete specifications are given. Computer Test Corp., Cherry Hill, N. J.

Circle No. 305 on Inquiry Card

Core Memories

Portfolio of miniature core-memory "Fact Sheets" provide specifications as well as descriptions of salient features and applications. An entire spectrum of core memories are covered ranging from miniature to rack mounted units, and encompassing random access, sequential access, and bit serial configurations for a wide variety of high-rel aerospace, airborne, and hydrospace applications. Di/An Controls, Boston, Mass.

Circle No. 314 on Inquiry Card

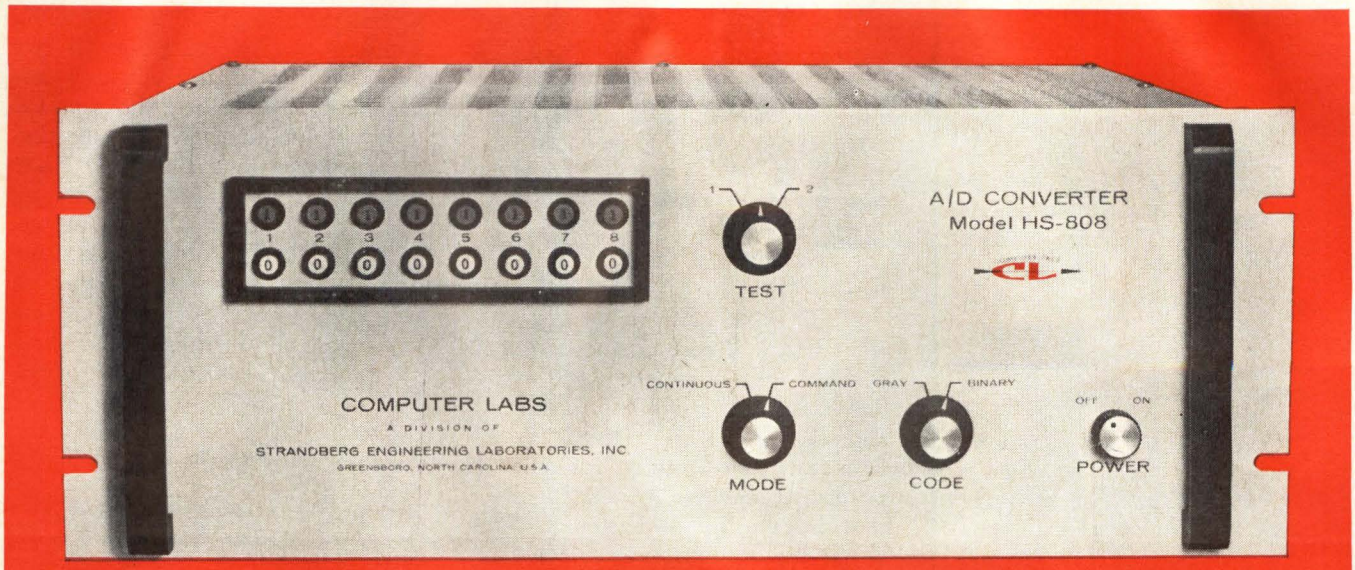
Pulse Generator

A 5 MHz pulse generator and six separate plug-in output units which provide varied output characteristics are described in a technical bulletin. Combinations provide outputs to ±25V, rise times to 0.8 ns, single or double pulses, and 2 ns to 50 ms durations. Datapulse Inc., Culver City, Cal.

Circle No. 313 on Inquiry Card

Would you believe

Speeds to 10 nanoseconds per bit.
Aperture time low as 0.2 nanoseconds.
Internal sample-and-hold and power supplies.
Prompt delivery.



HS-808 A/D Converter 8-bit Conversion at 8 MHz

BITS	MODEL NO.	CONVERSION RATE (MAX.)	APERTURE	WEIGHT OF LSB.	ACCURACY	ANALOG BW FOR RATED ACCURACY	MAX. ANALOG BANDWIDTH	PRICE
4	HS-425	25 MHz	1.0 ns	128 mv	64 mv	12.5 MHz	15 MHz	$5800
4	HS-406	6 MHz	3.0 ns	128 mv	64 mv	3 MHz	5 MHz	$4200
5	HS-520	20 MHz	0.8 ns	64 mv	32 mv	10 MHz	15 MHz	$6400
5	HS-505	5 MHz	2.5 ns	64 mv	32 mv	2.5 MHz	5 MHz	$4800
6	HS-615	15 MHz	0.6 ns	32 mv	16 mv	7.5 MHz	15 MHz	$7490
6	HS-604	4 MHz	2.0 ns	32 mv	16 mv	2 MHz	5 MHz	$5500
7	HS-710	10 MHz	0.4 ns	16 mv	8 mv	5 MHz	15 MHz	$7950
7	HS-703	3 MHz	1.5 ns	16 mv	8 mv	1.5 MHz	5 MHz	$5900
8	HS-808	8 MHz	0.35 ns	8 mv	4 mv	4 MHz	10 MHz	$8650
8	HS-802	2 MHz	1.0 ns	8 mv	4 mv	1 MHz	3 MHz	$6400
9	HS-905	5 MHz	0.2 ns	4 mv	2 mv	2.5 MHz	10 MHz	$9660
9	HS-901	1 MHz	0.5 ns	4 mv	2 mv	0.5 MHz	3 MHz	$6800

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CIRCLE NO. 88 ON INQUIRY CARD

LITERATURE

Photoelectric Keyboard

A two-page data sheet describes the new Photoelectric Keyboard, Series PK-200. This data sheet lists the various format and function options available with the keyboard which make it applicable to data handling and communication systems requiring unique or customized keyboard capability. Custom coding (up to 14 bits) and the use of photoelectric techniques to eliminate contact bounce and minimize RFI/EMI are also covered in the data sheet. Invac Corporation, Waltham, Mass.

Circle No. 325 on Inquiry Card

Ferrite Cores

A summary of core characteristics is available in a two-page sheet which lists sizes, pulse drive characteristics, and output signals. Described are 15 major ferrite core types including coincident current, coincident current lithium for wide temperature range applications, coincident current for 2D applications, switch, and linear. It also defines terms commonly used in core technology. Electronic Memories, Incorporated, Hawthorne, Cal.

Circle No. 331 on Inquiry Card

Disc Storage Unit

Bulletin describes a fixed-head, disc storage unit that provides random-access bulk storage of 227, 328 16-bit words. The unit consists of a disc storage assembly and a control and interface logic controller. Both of these assemblies are contained in one cabinet. Data is recorded on two recording surfaces. Each surface contains 64 tracks. Each track is divided into 16 sectors and each sector provides storage for 111 16-bit data words. Average access time for data recording or retrieval is 8.3 milliseconds. The word transfer rate is 112.5 KHz. Systems Engineering Labs, Ft. Lauderdale, Florida.

Circle No. 315 on Inquiry Card

DC Voltage Regulators

Bulletin illustrates and describes a new line of miniature DC voltage regulators. These regulators may be installed in any convenient location, and will operate from any available DC source—unregulated brute force supply, inverter-rectifier, battery, or a regulated supply—capable of furnishing the requisite voltage and current. DC input voltage may vary over as much as a 7-to-1 range; the device attenuates these variations (including ripple and noise) by at least 80db. Load regulation is of the order of 0.01%. Thirteen output voltage levels are available from 2 to 33vdc each adjustable $\pm 10\%$ about the nominal (without derating) by connection of an external resistor of appropriate value. The regulator occupies no more space than a pack of matches, and may be employed as an integral element of a master regulated DC power supply, or as a point-of-load-regulator operating from a remote source. Trio Laboratories, Inc., Plainview, L. I., N. Y.

Circle No. 318 on Inquiry Card

Shaft Encoder

A new four-page engineering bulletin, No. 66-14B, describes the details of 3-digit BCD shaft encoders and associated electronics. The bulletin details twelve of modular electronics that are optionally available with the encoder for performing such tasks as data display and printout, computer interface, and simplified digital control of motors and processes. Complete specifications, prices and application details are given. Theta Instrument Corp., Fairfield, N.J.

Circle No. 300 on Inquiry Card

One-Ounce Relay

Latest technical data on a general-purpose, one-ounce relay, quantity-priced at less than one dollar and rated to switch 1-ampere loads at least one million times from 90-milliwatt signals, is available. Sigma Instruments, Inc., Braintree, Mass.

Circle No. 332 on Inquiry Card

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LITERATURE

Test Equipment For Rent

This new 28 page illustrated catalog contains thousands of different items of instrumentation equipment such as digital computers, X-Y recorders, tape recorders, oscillographs, D. C. amplifiers, power supplies, frequency counters—all for rent. The 1967 Instrumentation "FOR RENT" catalog lists weekly and monthly rental rates together with manufacturer's specifications on all equipment offered. Datacraft, Inc., Gardena, Cal.

Circle No. 308 on Inquiry Card

EDP Accessories

A 16-page catalog contains full specifications, prices, and descriptions of a complete line of tape winders, rewinders, unwinders, continuous loop tape handling systems, perforated tape and magnetic tape splicers, splicing patches, data encoders, bulk tape erasers, head demagnetizers, tape reels, tape storage canisters and mailing boxes, data processing filing accessories, and perforating tapes. Robins Data Devices, Flushing, N. Y.

Circle No. 321 on Inquiry Card

IC Digital Instruments

A new eight-page condensed catalog describes digital equipment based on integrated circuit techniques without "hybrid" compromise. Equipment listed includes digital frequency synthesizers, counter/timers, clocks, and pulse generators. In all instruments extensive use of integrated circuits is said to reduce size, weight, and power dissipation, and to contribute new functional capabilities unobtainable through other means. Monsanto Electronics Technical Center, W. Caldwell, N.J.

Circle No. 307 on Inquiry Card

Integrated Circuits

Among the products listed in a reference guide are bipolar linear and digital integrated circuits, MOS integrated circuits, epoxy transistors, and MOS field-effect transistors. The brochure also contains instructions for logic diagrams, packaging, and basic parameters are given for all integrated circuits. Philco-Ford Corp. Microelectronics Div., Santa Clara, Cal.

Circle No. 310 on Inquiry Card

Core Application Note

How to determine optimum sizes for a given ferrite core is described in a two-page applicate note. Since stack drive and sense line impedances are a major parameter in memory stack design, the application note outlines a method of selecting the largest possible wire size for stringing cores. Electronic Memories, Hawthorne, Cal.

Circle No. 303 on Inquiry Card

Microelectronics

Integrated circuits manufactured by Radiation Incorporated are listed in a bulletin issued by the firm's Microelectronics Division. Typical characteristics, schematics and logic diagrams, for electrically isolated DTL circuits, operational amplifiers, and diode matrices are presented in a bulletin issued by Microelectronic Division, Radiation, Inc., Melbourne, Fla.

Circle No. 329 on Inquiry Card

Digital Printer Application

Thirty-six page tech manual, 2041B, is a comprehensive presentation of the theory and application of digital printers. Illustrated with photographs, block diagrams, timing charts, schematics and a logic diagram. Section III of the manual contains an illustrated, in-depth discussion of elementary digital techniques. Franklin Electronics, Inc., Bridgeport, Penna.

Circle No. 304 on Inquiry Card

Rotary Power Switches

New 12-page catalog no. E 5000-2 describes over 400 standard Series 100 quick-snap switches in four sizes, for loads from 3 to 200 amperes a-c or d-c; single-pole to 12-pole single-throw and to 8-pole 4-throw. Gives details of dimensions, mounting, terminal arrangements, weights, torques, handle-positions, accessories, and optional features. Explains "Erectorset" principle, whereby off-the-shelf components can be combined in customized configurations for a variety of switching, control, and data handling functions. Electro Switch Corp., Weymouth, Mass.

Circle No. 326 on Inquiry Card

DTL-TTL Reference Chart

Compatibility, interfacing and performance characteristics of DTL and TTL integrated circuit logic modules are covered in a new quick-reference chart. The chart lists propagation time, power dissipation (maximum and typical), fan in-fan out, and all other important operating parameters of DTL-TTL modules, including DTL-TTL interface. The four page, full color chart folds to a standard 8½ x 11 booklet for easy filing or inclusion in a notebook. Data Technology Corporation, Mountain View, Cal.

Circle No. 306 on Inquiry Card

Memory Exerciser

Designed for laboratory development and production testing of magnetic core memory systems, an exerciser, described in a 12-page brochure, addresses of 40-bit words at variable cycle times from 400 nanoseconds to 500 milliseconds. The system's variable timing can be substituted for the fixed timing of a memory to detect and investigate sense amplifier strobing, gating, and driver timing characteristics. The brochure gives design, operation, specification, and interface data. Honeywell Inc., Computer Control Div., Framingham, Mass.

Circle No. 311 on Inquiry Card

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(maybe we've generated a homonym!)

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- Problem Analysis
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- Automatic Test Equipment
- Diagnostic Problems
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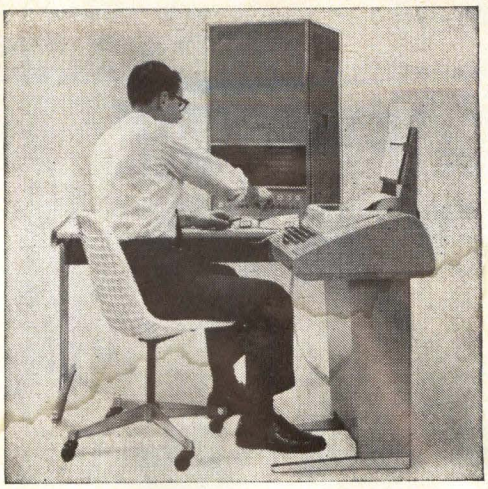

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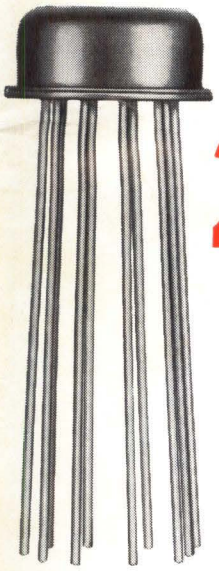

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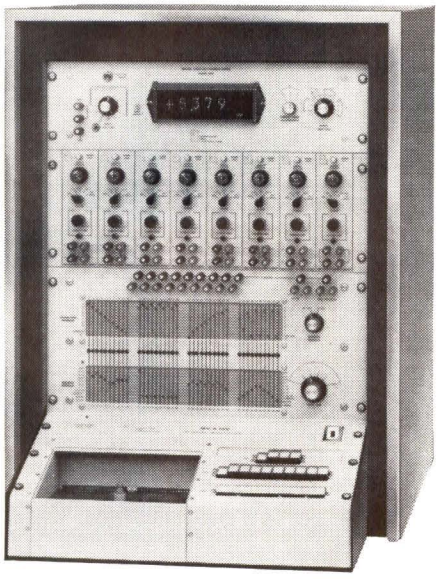

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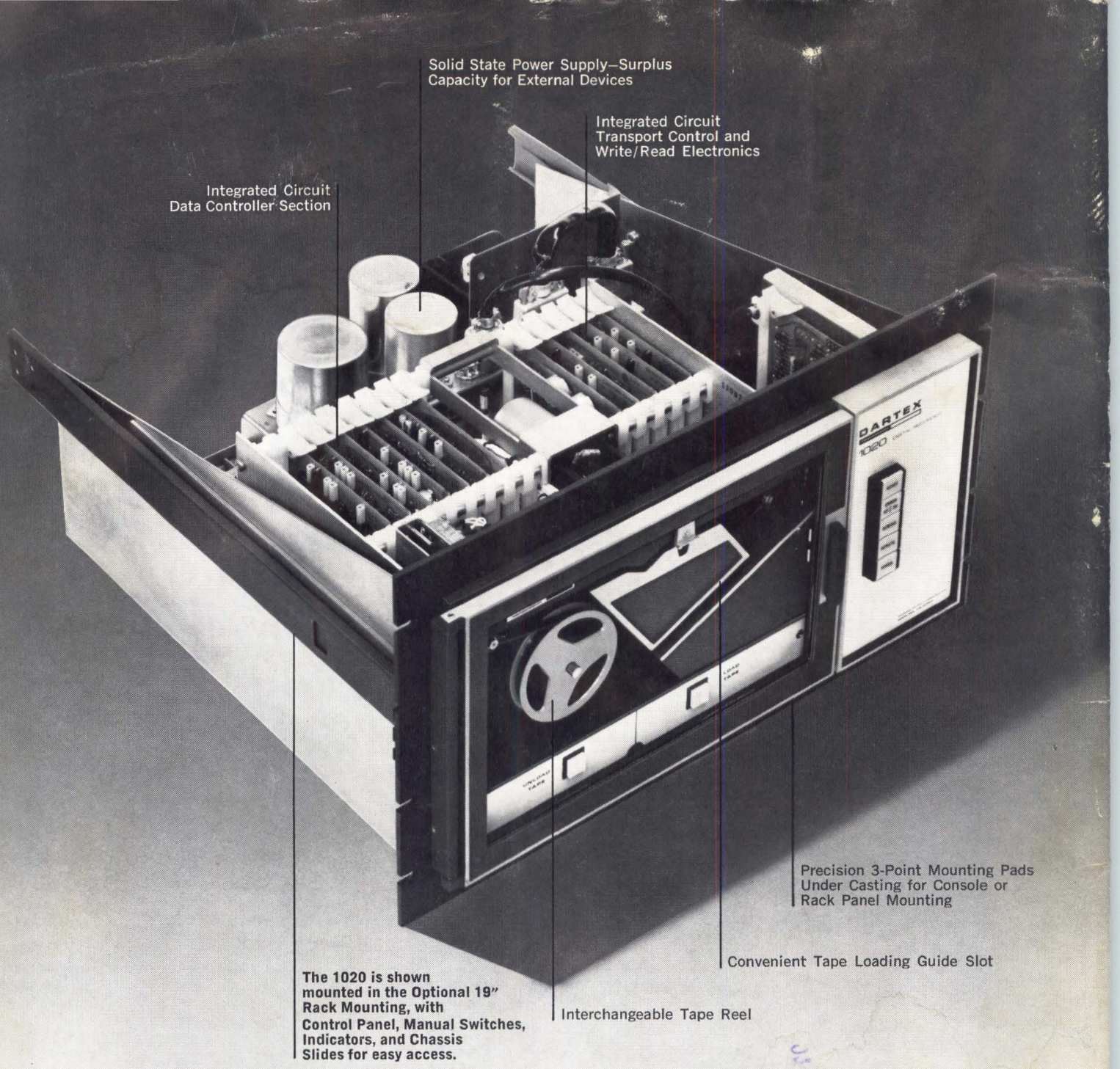

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