# COMPUTER DESIGN

## THE MAGAZINE OF DIGITAL ELECTRONICS

MAY 1978

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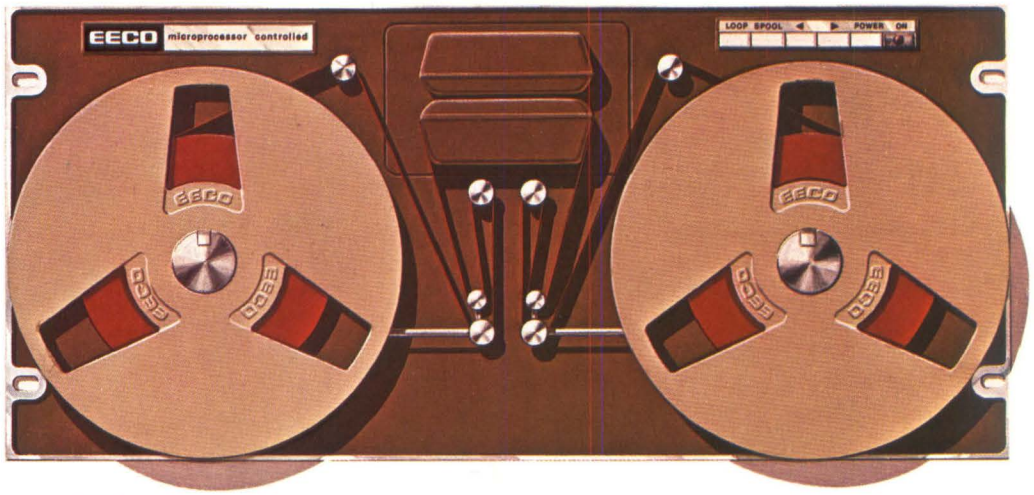


# This new microprocessor controlled

reader/spooler will read
1000 characters per second,
and still provide *stop on character.*
All of its reader/spooler functions,
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stopping,
rewind speed (1500 c/s),
data output,
and interface timing
are controlled by a program
stored in
its microprocessor memory.
Its other advantages lie in the areas of
reading reliability,
high speed stopping,
programmed soft stopping,
the spooler system,
and equipment reliability.
It also includes
step and slew modes, and
a priority interrupt mode.
And like other EECO readers
it boasts LED
and phototransistor optoelectronics,
a step motor drive,
a full tape-width barrel sprocket,
handshake interface logic,
and TTL and DTL compatible electronics.
But wait, we can't sell you one now,
because it won't be shippable until
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just so you
can make plans.
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*First public showing.

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# They weren't born yesterday.

Being first doesn't happen overnight. The Series 9000 synchronous tape transports are the result of 16 years experience in designing and building digital tape transports. We've learned a few things along the way — the many unique features of Series 9000 prove it. Features such as:

- A position arm anticipatory sensing system. An exclusive Kennedy feature, the linear, non-contact (Mag Pot) position sensor requires no lamp source and assures performance for the life of the machine.
- Interchangeable electronics on all Series 9000 transports, to reduce stocking costs and down time.
- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick-release hubs.
- All models are available with either 7 or 9 track, 800 NRZI, 1600 PE or 800/1600 NRZI/PE.
- 7 and 9 track NRZI and PE format/control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available.

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**TALLY**

**CIRCLE 3 ON INQUIRY CARD**

THE MAGAZINE OF DIGITAL ELECTRONICS

# COMPUTER DESIGN

MAY 1976 • VOLUME 15 • NUMBER 5

## FEATURES

**104 NATIONAL COMPUTER CONFERENCE**

Celebrating the 25th anniversary of Joint Computer Conferencing, this year's NCC has "something for everyone." The technical program, made up of 128 sessions divided into three major areas, addresses societal issues in computing, systems design and management, and computer and data base architecture. More than 266 organizations will display the latest in EDP technology on three floors of the Coliseum

**159 ARCHITECTURE OF AEROSPACE COMPUTER SIMPLIFIES PROGRAMMING**

**by H. Clifford Kancler**

By concentrating complex design features in the microprogram rather than in software or hardware, the effects of developmental changes on hardware have been minimized and the use of micro-diagnostics optimized

**169 MOVING INVERSIONS TEST PATTERN IS THOROUGH, YET SPEEDY**

**by J. Henk de Jonge and Andre´ J. Smulders**

Because the MOVI program requires fewer tests than other time-consuming methods, it is particularly useful for testing large memories

**175 ADAPTER SIMPLIFIES DEVELOPMENT OF MICROPROCESSOR SYSTEMS**

**by Robert L. Morrison and Claude A. Wiatrowski**

An adapter board simplifies microprocessor system development by simulating special characteristics of nonstandard ROMs, allowing reprogrammable ROMs to be substituted for specialized mask-programmed versions

**179 AUTOMATIC ERROR CORRECTION IN MEMORY SYSTEMS**

**by Bryan Rickard**

Understanding underlying principles of failure rate analysis allows the decision on whether or not to include error-correction and/or detection techniques in a system to be made on a firm base

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**by San-Yen Shi**

Combining logarithm computation with table lookup simplifies overall procedures

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**by Suresh Vasa**

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**212 MEDIUM SCALE COMPUTER FEATURES SIX MICROPROCESSOR CHIPS IN CPU**

Price/performance ratio obtained by use of MPUs allows 24-bit capability at prices competitive with 16-bit machines

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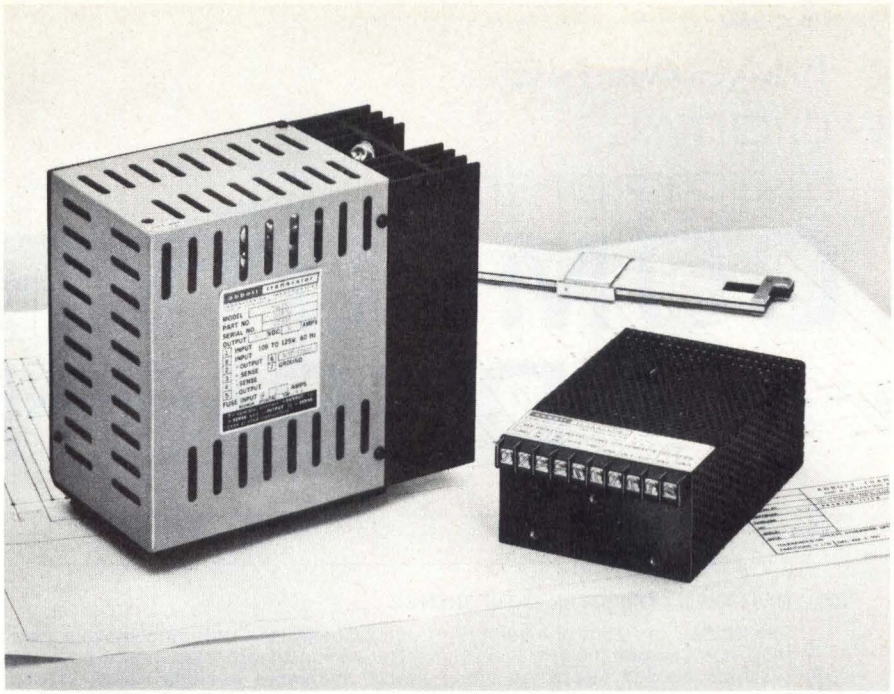

# Reduce Your Power Supply Size and Weight By 70%

A new way has been found to substantially reduce power supply size and weight. Consider the large power supply shown at left in the above photo – it uses an input transformer, into a bridge rectifier, to convert 60 Hz to 5 volts DC at 5 amperes. This unit measures 6½"x4"x7½" and weighs 13 pounds. Abbott's new model Z5T10, shown at right, provides the same performance with 70% less weight and volume. It measures only 2¼"x4"x6" and weighs just 3 pounds.

This size reduction in the Model Z5T10 is primarily accomplished by eliminating the large input transformer and instead using high voltage, high efficiency, DC to DC conversion circuits. Abbott engineers have been able to control the output ripple to less than 0.02% RMS or 50 millivolts peak-to-peak maximum. This design approach also allows the unit to operate from 100 to 132 Volts RMS and 47 to 440 Hertz. Close regulation of 0.15% and a typical temperature coefficient of 0.01% per degree Celsius are some of its many outstanding features. This new Model "Z" series is available in output voltages of 2.7 to 31 VDC in 12 days from receipt of order.

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**Please see pages 1037-1056 Volume 1 of your 1975-76 EEM (ELECTRONIC ENGINEERS MASTER Catalog) or pages 612-620 Volume 2 of your 1975-76 GOLD BOOK for complete information on Abbott Modules.**

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**Editorial & Executive Offices**
**221 Baker Ave,**
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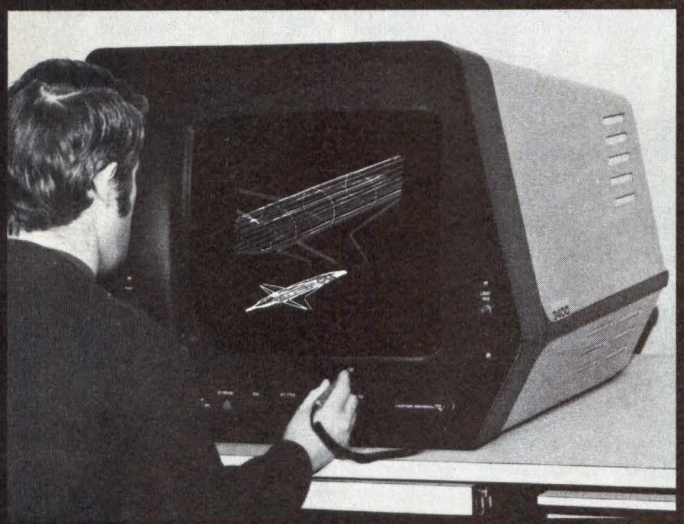
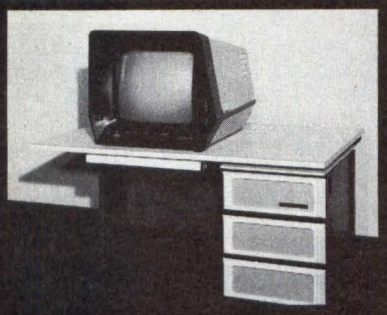
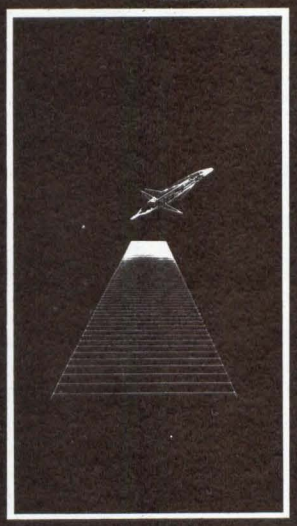
# Announcing the 3400

## Interactive Graphics Display...







## Welcome to 1980.

Introducing a totally new graphics display system with years-ahead performance at years-ago prices: the Vector General 3400.

Featuring a new standard of hardware modularity and firmwear flexibility, the 3400 has a system organization designed to keep pace with advances in minicomputer hardware and operating systems technology.

The 3400 hardware features 3D Digital Transformations, a 1,600-to-1 Dynamic Range, Clip/Zoom/Window, Perspective, unique user aids (Hit/Select/Pick/Edit), and an internal refresh buffer that yields a dramatic reduction in host computer loading.

Complementing the 3400's advanced hardware and firmwear, there is a powerful new software system featuring VGAM (Vector Graphics Access Method) a macro-oriented handler with facilities for efficient graphics resources management.

The technology of the 3400 will be commonplace in the 1980's; with Vector General's 3400, you can have it today.

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# CALENDAR

## CONFERENCES

**June 8-10—FIRST NORTHEAST PRODUCTIVITY CONF,** Hartford Hilton Hotel, Hartford, Conn. INFORMATION: D. A. Vincent, Asst Mgr, Tech Activities Dept, Soc of Manufacturing Engineers, 20501 Ford Rd, Dearborn, MI 48128. Tel: (313) 271-1500

**June 15-18—FIRST JOINT INTERNAT'L MAGNETICS, AND MAGNETISM AND MAGNETIC MATERIALS CONF,** Hilton Hotel, Pittsburgh, Pa. INFORMATION: Conf Chm, E. W. Pugh, IBM Research Ctr, PO Box 218, Yorktown Heights, NY 10598

**June 16-20—INTERNAT'L FEDERATION OF AUTOMATIC CONTROL SYM ON LARGE SCALE SYSTEMS,** Udine, Italy. INFORMATION: G. Guardabassi, Istituto di Elettrotecnia ed Elettronica, Politecnico di Milano, 32 Piazza Leonardo da Vinci, 20133 Milano, Italy

**June 17—15TH ANNUAL ACM TECHNICAL SYM,** Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Dr Robert S. Butler, Nat'l Bureau of Standards, A247 Technology Bldg, Washington, DC 20234. Tel: (301) 921-3485

**June 21-23—MODEL CURRICULA IMPLEMENTATION TECHNIQUES,** Illinois State U, Bloomington-Normal, Ill. INFORMATION: Earl Ecklund, Regional HELP Subcomm, Computer Science Dept, Illinois State U, Bloomington-Normal, IL 61761. Tel: (303) 436-6681

**June 21-23—IEEE COMPUTER SOC INTERNAT'L SYM ON FAULT-TOLERANT COMPUTING,** Pittsburgh, Pa. INFORMATION: Gen'l Chm, Prof Daniel P. Siewiorek, Computer Science Dept, Carnegie-Mellon U, Pittsburgh, PA 15213

**June 21-23—34TH ANNUAL DESIGN RESEARCH CONF,** U of Utah, Salt Lake City. INFORMATION: Dr E. I. Gordon, Bell Telephone Laboratories, Rm 2A-330, Murray Hill, NJ 07974

**June 21-24—INTERNAT'L SYM ON INFORMATION THEORY,** Ronneby Brunn, Ronneby, Sweden. INFORMATION: Robert W. Lucky, Bell Laboratories, Rm 1F-532, Holmdel, NJ 07733

**June 24-25—NORTHWEST 76, ACM-CIPS PACIFIC REG SYM,** Seattle Pacific College, Seattle, Wash. INFORMATION: Ms Patricia Crockett, Gen'l Chm, PO Box 88063, Tukwila Branch, Seattle, WA 98188. Tel: (206) 773-9823

**June 28-30—13TH ANNUAL DESIGN AUTOMATION CONF,** Palo Alto, Calif. INFORMATION: D. J. Humcke, Bell Laboratories, Holmdel, NJ 07733. Tel: (201) 949-6253

**July 12-16—CONF ON COMPUTER TECHNOLOGY—MICROPROCESSORS/COMPUTERS,** Iowa State U, Ames, Iowa. INFORMATION: Conf Director, Roger Camp, 332 Coover Hall, Iowa State U, Ames, IA 50011. Tel: (515) 294-2663

**July 14-16—SIGGRAPH 76 (CONF ON COMPUTER GRAPHICS, INTERACTIVE TECHNIQUES, AND IMAGE PROCESSING),** Philadelphia, Pa. INFORMATION: SIGGRAPH 76, Gen'l Chm, Dr Thomas Johnson, Dept of Decision Science, U of Pennsylvania, Philadelphia, PA 19174

**Aug 10-12—4TH SYM ON THE SIMULATION OF COMPUTER SYSTEMS,** Nat'l Bureau of Stds, Boulder, Colo. INFORMATION: Arthur F. Chantker, Nat'l Bureau of Standards, Technology Bldg, Rm A247, Washington, DC 20234

**Aug 24-27—1976 INTERNAT'L CONF ON PARALLEL PROCESSING,** Waldenwoods Resort and Conf Center, Waldenwoods, Mich. INFORMATION: Tse-yun Feng, Conf Chm, 1976 Internat'l Conf on Parallel Processing, College of Engineering, Wayne State U, Dept of Electrical and Computer Engineering, Detroit, MI 48202

**Aug 31-Sept 2—1976 INTERNAT'L OPTICAL COMPUTING CONF,** Capri, Italy. INFORMATION: Sam Horvitz, Gen'l Chm, Naval Underwater Systems Center, New London, CT 06320

**Sept 7-10—COMPCON 76 (13TH IEEE COMPUTER SOCIETY INTERNAT'L CONF)** Mayflower Hotel, Washington, DC. INFORMATION: Paul L. Hazan, Program Chm, The John Hopkins U, Applied Physics Lab, John Hopkins Rd, Laurel, MD 20810. Tel: (301) 953-7100, X449

**Sept 14-17—WESCON (WESTERN ELECTRONIC SHOW AND CONV),** Los Angeles Conv Center, Los Angeles, Calif. INFORMATION: William C. Weber, Jr, WESCON Gen'l Mgr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

## SHORT COURSES

**May 22—MICROPROCESSORS AND THEIR APPLICATION TO INDUSTRIAL CONTROL OF DATA ACQUISITION SITUATIONS,** Whittemore Hall, VPI & SU Campus, Blacksburg, Va. **June 4-5—MICROPROCESSORS,** Engineering and Science Building Auditorium/Lecture Hall, U of Pittsburgh, Johnstown, Pa. INFORMATION: Educational Registrar, IEEE, 445 Hoes Lane, Piscataway, NJ 08854

**June 6-11—MICROPROCESSORS AND MINICOMPUTERS—INTERFACING AND APPLICATIONS,** Virginia Polytechnic Institute and State U, Blacksburg, Va. INFORMATION: American Chemical Soc, Educational Activities Div, 1155 16th St NW, Washington, DC 20036. Tel: (202) 872-4508

**June 7-11** (Madison)**—MINICOMPUTERS IN INSTRUMENTATION AND CONTROL, June 14-25** (Madison)**—COMPUTER TECHNIQUES—POWER SYSTEMS, June 21-25** (Milwaukee)**—POWER SUPPLY DESIGN WITH INTEGRATED CIRCUIT REGULATORS, July 19-23** (Milwaukee)**—HUMAN FACTORS IN ENG AND THE DESIGN OF ELEC EQUIP, Aug 16-20** (Milwaukee)**—CRT AND MATRIX DISPLAY SYSTEMS DESIGN,** U of Wisconsin—Ext. INFORMATION: U of Wisconsin—Extension, Dept of Engineering, 432 N Lake St, Madison, WI 53706. Tel: (608) 262-2061

**June 20-23—IEEE WORKSHOP ON IMPLEMENTING THE MODEL CURRICULA,** Illinois State U, Bloomington. INFORMATION: Prof David Rine, Workshop Chm, Computer Science Div, West Virginia U, Morgantown, WV 26506. Tel: (304) 293-3196

**June 21-25—STRUCTURED PROGRAMMING AND SOFTWARE ENGINEERING; MODERN DATA COMMUNICATIONS; ADVANCES IN ELECTRONICS TECHNOLOGY,** George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

**June 28-July 2—DATA BASE DESIGN METHODOLOGY, July 19-23—LOGICAL DESIGN FOR DIGITAL, COMPUTER, AND INSTRUMENTATION SYSTEMS,** U of Michigan, Ann Arbor. INFORMATION: Continuing Engineering Education, 300 Chrysler Center—North Campus, The U of Michigan, Ann Arbor, MI 48105

**July 12-23—OPERATING SYSTEMS; STRUCTURED PROGRAMMING, July 19-30—DATA BASE MANAGEMENT, July 26-30—SIMULATION USING GPSS, July 26-Aug 6—COMPILER CONSTRUCTION, Aug 2-13—PRACTICAL COMPUTER GRAPHICS; USING MICROCOMPUTERS,** U of California, Santa Cruz. INFORMATION: Joleen Kelsey, U of California Ext, Santa Cruz, CA 95064. Tel: (408) 429-2761

## SEMINARS

**July 14-16** (London), **July 19-21** (Munich)**—MINICOMPUTERS.** INFORMATION: Ms Heidi E. Kaplan, New York Mgmt Center, Dept 14NR, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

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# MICROPHOTOS

**Your IC lead frames look like this** at 30X enlargement (unretouched). Because they are punched out of metal, the edges are rough, jagged and irregular. In contrast, the flat sides of the lead frame are smooth, even and perfectly plated.

Arrows indicate scars and abrasions made by rough edge of lead frame.

22X magnification, unretouched.

## THEIRS

**An ordinary edge-bearing socket contact** after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. Notice how the contact has scars and abrasions from *rough, irregular edge of IC lead frame.* Electrical contact is degraded and resistance is increased. Reliability is obviously reduced.

*Lead frame in place in an ordinary edge-bearing contact.*

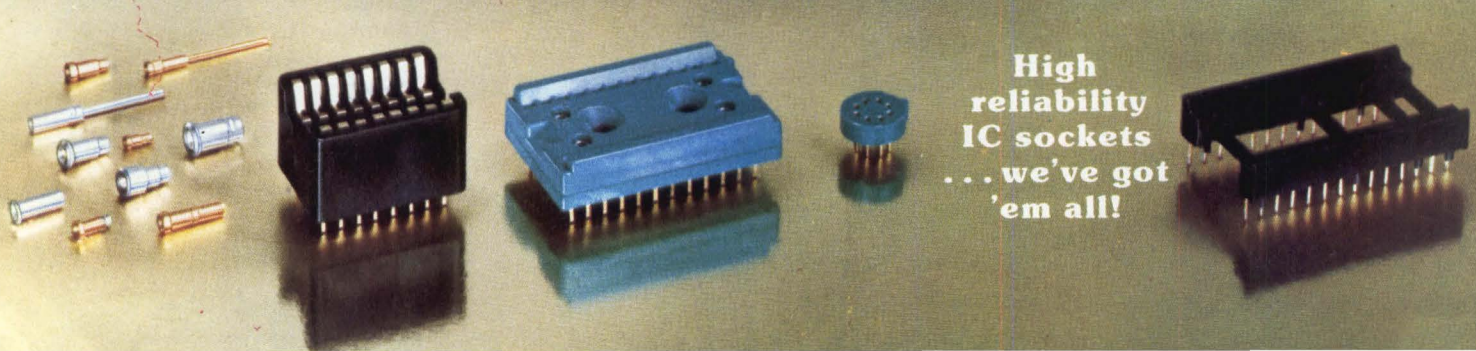
Arrows indicate contact surface still smooth, clean, free from abrasions.

22X magnification, unretouched.

## OURS

**ROBINSON-NUGENT "side-wipe" socket contact** after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. See how the RN contact—because it mates with the *smooth, flat side of the IC lead frame*—retains its surface integrity. This 100% greater lead frame contact results in continued high reliability.

*Lead frame in place in RN "side-wipe" contact.*

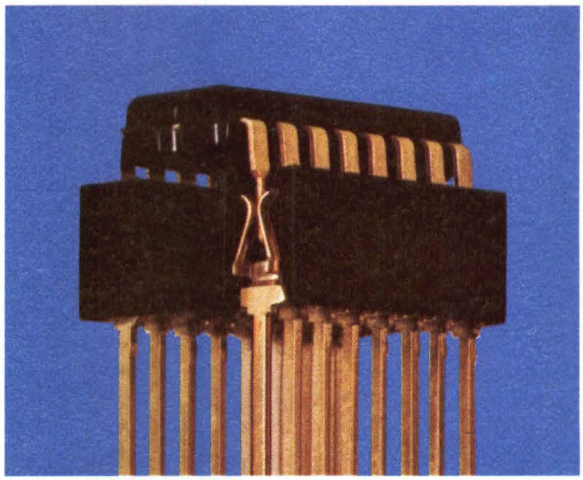


**High reliability IC sockets . . . we've got 'em all!**

# expose 'junk' socket problems

## Secret of RN high reliability 'side-wipe' DIP sockets revealed by microphotos

Here's microscopic proof that high reliability Robinson-Nugent "side-wipe" DIP sockets make 100% greater contact than any edge-bearing socket on the market. This advance design provides constant low contact resistance, long term dependability—trouble-free IC interconnects. Yet RN high reliability DIP sockets cost no more than ordinary sockets!



**Get the high reliability that eliminates trouble.** RN "side-wipe" DIP sockets make contact with the wide, flat sides of your IC leads. You get 100% greater surface contact for positive, trouble-free electrical connection.

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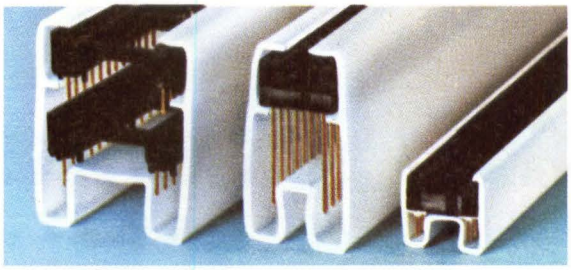
for catalog and informative book "What to Look for in IC Interconnects." Free from Robinson-Nugent—the people who make more kinds of high reliability IC sockets than anyone.



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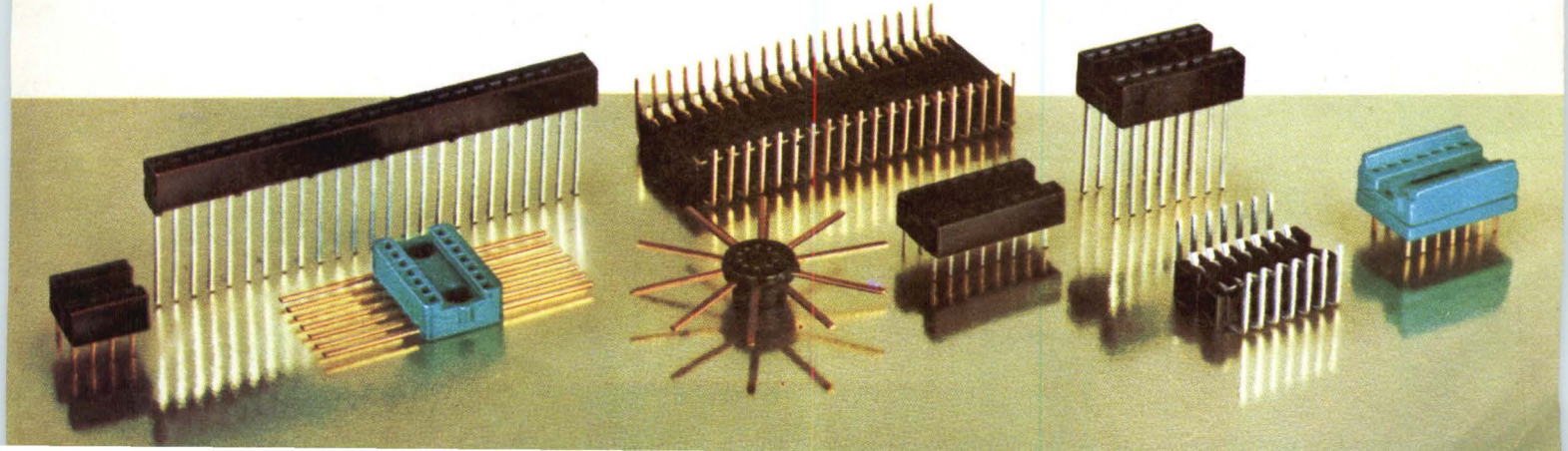

# LETTERS TO THE EDITOR

To the Editor:

Re Mr Whitby's letter in this column (Feb 1976) concerning the originality of Pandeya and Cassa's work ("Parallel CRC Lets Many Lines Use One Circuit," Sept 1975):

My article "Implementation of a Parallel Cyclic Redundancy Check Generator," *Computer Design*, Mar 1974, is based on an idea conceived in early 1970.

The article also contains references to two papers presented at the Spring and Fall Joint Computer Conferences in 1971.

While I do not claim that I was the first to conceive the idea, I maintain that to my knowledge I designed and built the first working parallel CRC generator in 1970-71.

Karl M. Helness
Tandbergs Radiofabrikk A/S
Oslo, Norway

To the Editor:

In his article "Trends in Computer Hardware Technology" (Feb 1976), David Hodges suggests that it is unlikely that the cost per instruction executed can continue to be reduced by building larger, faster computers such as the 1000-MIPS CPU predicted by the Rand Corp.

It is true that Control Data Corp cancelled its 8600 development project, whose goals were a machine in the 1000-MIPS area. The project was cancelled primarily for economic reasons, though the technical problems were indeed formidable.

The 1000-MIPS processor, however, is still on the horizon. Its immediate predecessor, the Cray-1 computer, is already operational in the laboratories of Cray Research, Inc. This machine delivers peaks of throughput up to 200 MOPS (roughly analogous to the MIP) and sustained performance in the 60 to 80 MOPS range. This peak performance is delivered at an approximate cost of $40,000 per MOPS.

Simple examination of the Cray-1 architecture reveals that it can be extended in the not too distant future to an approximately 1000 MIPS machine with little effort. Coupled with decreases in memory cost predicted by Mr Hodges, an educated guess says that such performance could be delivered at an approximate cost of $8500 per MOPS.

In reading Mr Hodges' final paragraphs, it is interesting to note that in the cases of all but the ILLIAC IV and STAR-100, each of the computers shown on the curve of Fig. 11 started out as a special-purpose processor for solving scientific problems, and evolved into a somewhat general-purpose processor later in its life. Mr Cray seems to be betting that such is still the case.

Richard E. Reeves
Consultant
Huntsville, Ala


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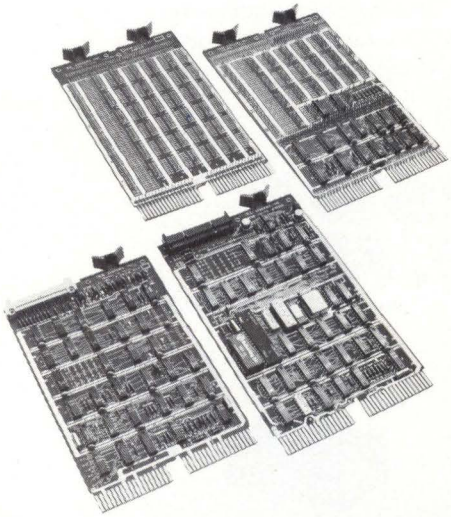

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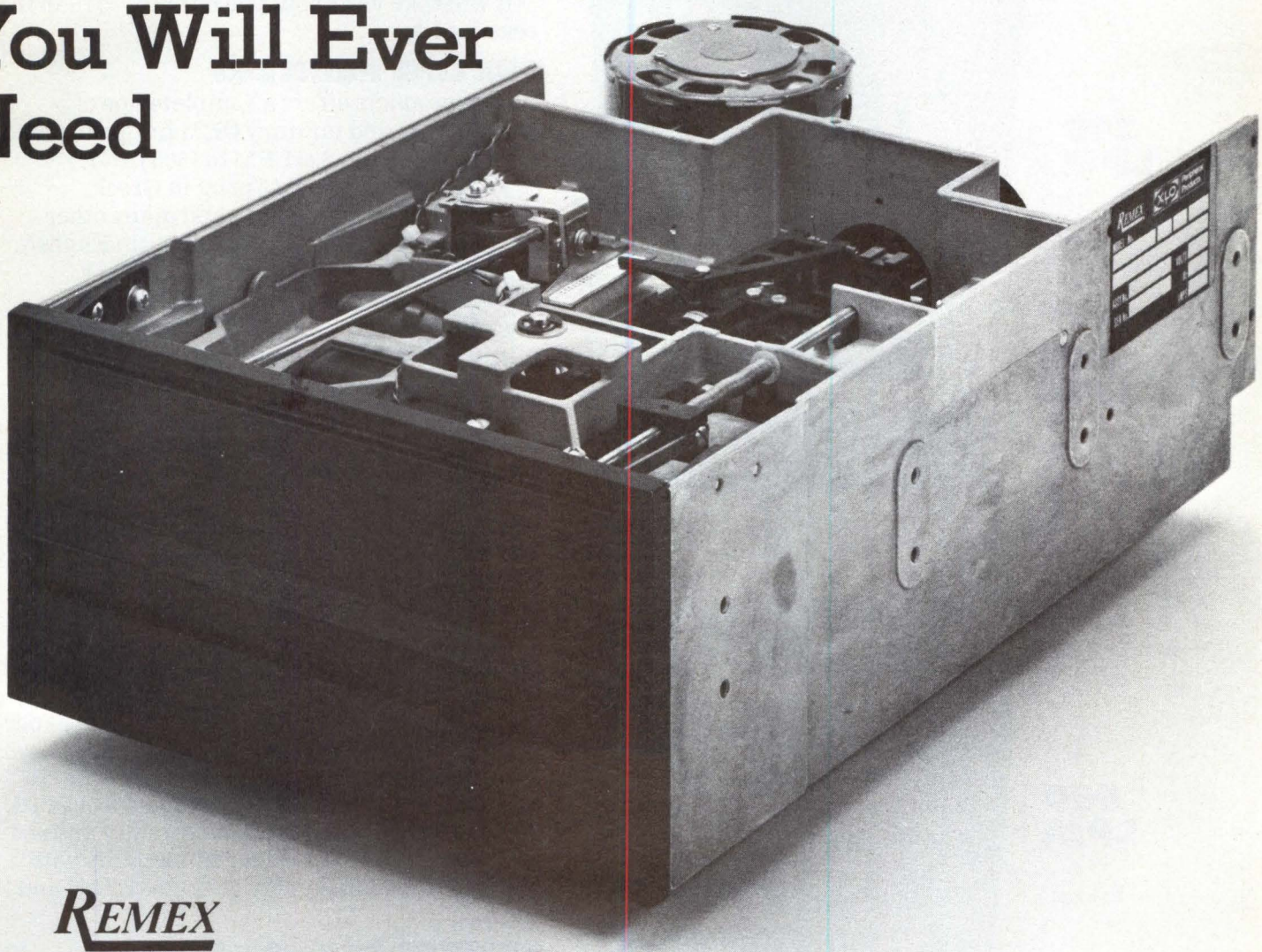

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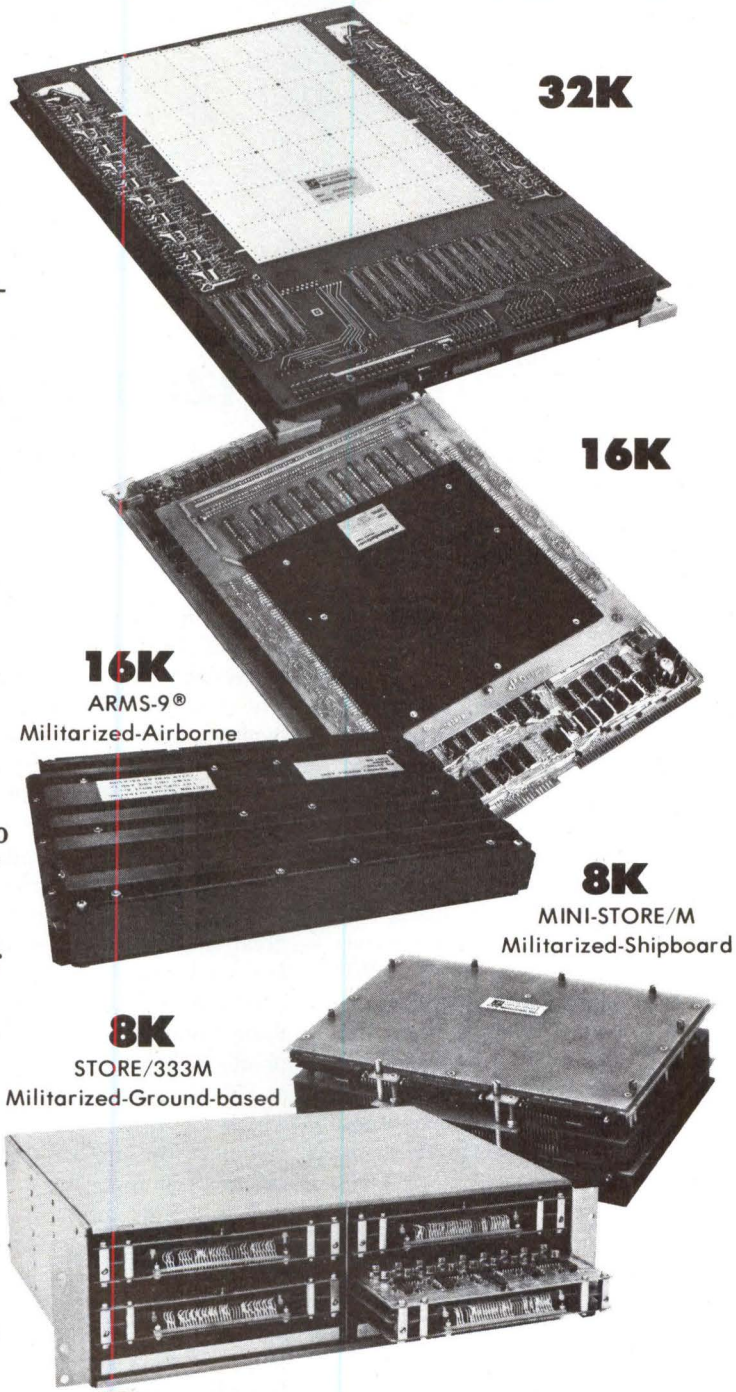


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COMMUNICATION CHANNEL

**by John E. Buckley**
Telecommunications Management Corp
Cornwells Heights, Pa.

# Computerized PBX Systems

This past March 10th, the telecommunications community observed the centennial anniversary of the basic telephone patent awarded to Alexander Graham Bell. However, in contrast to the ever expanding application of new technologies in the data communications segment of the telecommunications environment, the basic transmission of informational energy and the operation of the nationwide telephone systems still encompass many engineering principles and, in many cases, the equipment design originally conceived and developed by Mr Bell and his contemporaries. During almost 90 years following the first telephone patent, if Alexander had been able to visit virtually any telephone system or transmission center, he would have found himself in familiar surroundings. Only since the mid-60's have we experienced rapid and innovative developments in the use of the basic telephone network for the exchange of data or computer communications. Yet, even during that period, the use of the telephone system for voice applications was uniquely compatible with traditional telephone techniques and principles.

Only now are we seeing the first major deviation from traditional practices in the area of voice communications, developments which are now merging the requirements of voice communications with data processing principles and techniques. These new telephone switching systems for individual business requirements provide voice switching capabilities by using stored program data processing devices, that is, digital computers.

Most organizations today employ a digital computer to perform technical and business computations, and a great number of those organizations use a telephone system to communicate the required data. Yet, often these companies have internal telephone switching systems referred to as Private Branch Exchanges (PBXs) which reflect the traditional telephone principles in cumbersome electromechanical devices.

A major deviation from the traditional is the application of the digital computer to the telephone switching system requirement. The resulting product is known as a computerized-PBX or a Computerized Branch Exchange (CBX). Three major CBXs have been introduced recently in the U.S.: Western Electric, wholly owned subsidiary of AT&T, is promoting its Dimension Telephone System through the various Bell System Operating Companies; Rolm Corp of Cupertino, Calif is presently installing its CBX: Business Switch; and IBM is marketing its 3750 Switching System.

Although commonplace to the data processing community, these examples are revolutionary in the previously staid telephone environment. All systems operate under a stored program environment including an operating system and a series of utility programs or routines which control and interact on a series of application programs. All three vendors isolate the area of program development from the actual user; they provide, in effect, turnkey systems. However—consistent with the background of each company—application programs from Rolm and IBM tend to be flexible and user-oriented, while those from Western Electric tend to be rigidly defined.

Both Rolm and Western Electric use time division multiplexing (TDM) to perform the switching functions. The usual switching matrix of a telephone PBX system is replaced by a TDM bus in which time slots are defined and addressable. IBM continues to use the discrete crosspoint switching concepts, but the crosspoints are solid-state rather than mechanical. In all systems per-

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CIRCLE 13 ON INQUIRY CARD

# New Intel microcom system costs, increase

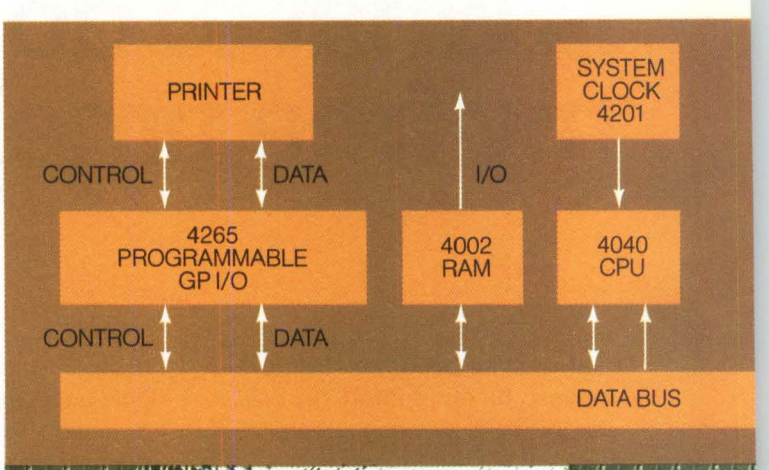
Intel has two new LSI components for the MCS-40™ microcomputer system which will help you cut system costs, increase throughput and reduce the number of components you have to stock for I/O interface requirements. The new Intel 4269 Programmable Keyboard Display and the 4265 Programmable General Purpose I/O devices eliminate the large number of discrete SSI/MSI components previously required for keyboard, control panel, indicator array, alphanumeric display, printer, communications and other I/O interfaces. These new LSI parts increase system throughput up to 50%, and make it easy to add standard Intel memory and system peripherals.

The 4269 Keyboard Display can be software programmed to interface to various keyboard and display elements and makes it possible for you to eliminate fifteen or more discrete components.

It significantly increases system throughput since it performs the scan, storage, refresh, and other simultaneous keyboard/display tasks previously required of the 4004 or 4040 CPU.

When programmed as a keyboard or line sensor input interface, the 4269 can scan up to 64 key closures or lines. When a key closure is detected, the 4269 generates a system interrupt and stores up to eight characters in its first-in/first-out buffer before requiring CPU service.

In alphanumeric applications, the 4269 eliminates the need to use the CPU



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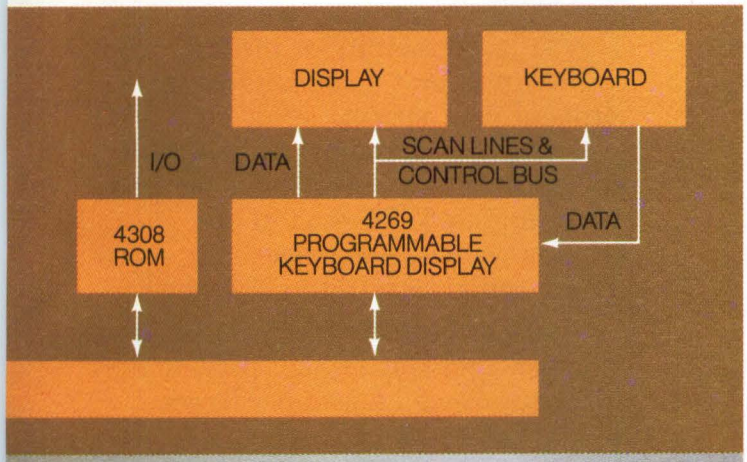
# puter I/O devices cut throughput up to 50%



and system memory for display refresh since the necessary memory and control are built in. One 4269 can operate and refresh alphanumeric displays or indicator arrays with up to 32x4 digits, 16x8 characters or any configuration of 128 elements or lights, including a 20-character Burroughs Self-Scan* Display.

The 4265 General Purpose Programmable I/O is ideally suited to implement custom interface requirements. Up to four devices can be controlled by the CPU. Each 4265 has 16 I/O lines organized into four ports which can be used in 14 different data transfer and control/interface organizations. The 4265 provides synchronous/asynchronous control, buffer inputs and outputs, bit set and bit reset capability on output port lines and byte transfer control. It can be used to add industry standard RAM memory such as Intel's 5101 CMOS RAM. And the 4265 lets you use system peripherals such as the 8251 Programmable Communications Interface (USART), the 8253 Programmable Interval Timer or the 8214 Priority Interrupt Control Unit.

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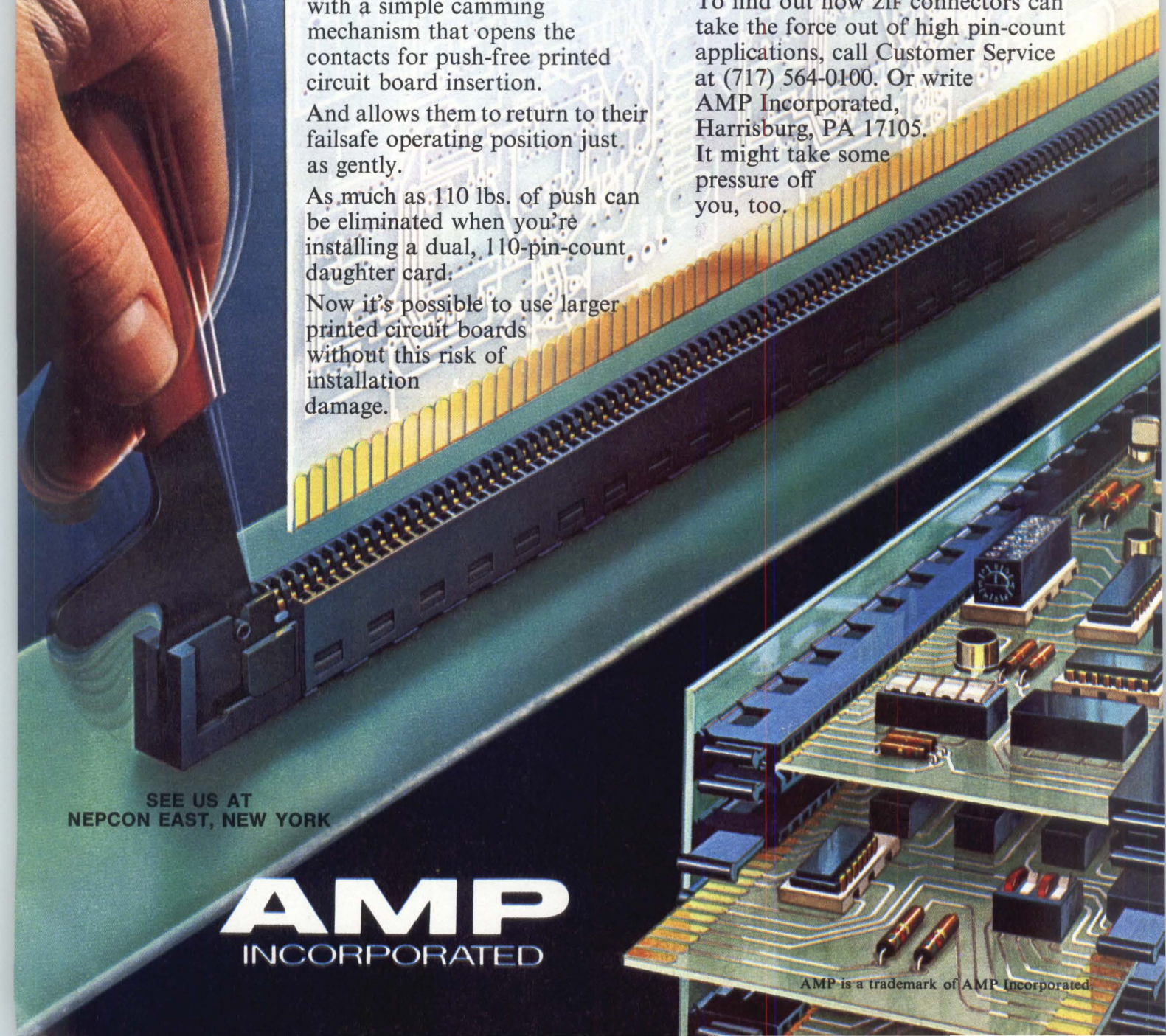

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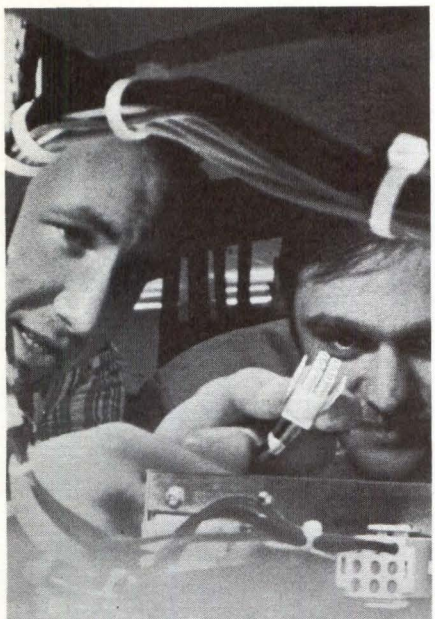

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formance of specific functions, recognition of addressing digits (dialed telephone number), and the decisions required to establish authorized connections are performed under program control interacting with user-defined stored tables.

The 3750 descriptions clearly link this product to existing IBM data processing installations. It can support a number of peripherals such as teletypewriters, CRT terminals, magnetic tapes, line printers, or audio response units. Although it is continually discussed in terms of an IBM computer system, connected and accessible via a communications adapter, the associated computer is not mandatory for the 3750 operation and is necessary only if full automation of the information environment is desired. The 3750 is supported under a modified version of the IBM Customer Information Control System/Virtual Storage which provides a transaction-oriented multi-application data base/data communications interface to the System/370 operating system. IBM even suggests that the name of the telephone set be changed to "information station" when it is used with the 3750.

Under its consent decree, AT&T is prohibited from entering into business areas that are not directly communications. Therefore, Western Electric's Dimension System is carefully defined as only a voice telephone switching system. Data can be transmitted through the system with minimal limitations but under no circumstances does the system become aware of the data content or attempt to perform functions based on that content. Availability of data collection of calling activity or automatic routing of calls, which would typically be expected to be available from a computerized-PBX, is precluded and is available only through existing tariffed offerings of the specific telephone central office connected to the customer-located Dimension System. No peripheral devices can be connected other than standard telephone sets and attendant consoles. The market strategy carefully limits the potential capability of the system to functions that can be uniformly programmed and controlled and that are representative of functions that have typically been provided to a traditional PBX user. In addition, system support appears to be structured to keep the user dependent on the same services and extra cost offerings presently offered in a controlled environment by the operating telephone companies.

The Rolm CBX: Business Switch is also defined as primarily a voice telephone switching system but the "door is left open" for utilizing its program capabilities as a data sensitive system. While the company does not provide any data processing programs, this limitation is presented in terms of its current status only. The ability to implement an interface to a peripheral data processing system is presently provided and a minicomputer system with typical peripherals can be provided. This minicomputer system can be programmed to collect and process the call activity data and statistics occurring within the system. The resulting computer reports analyze the calling characteristics and costs generated through the system for network optimization and cost allocation purposes. Rolm is not attempting to either promote more data processing applications or increase dependency on the existing telephone system services.

These three different and yet similar computerized-PBX systems mark the beginning of the second 100 years of telephone technology. The blending of telephone and computer technologies has long been predicted, but is now a reality. It is interesting to note that the two sources from the traditional environments present their systems in terms that will continue supporting their interests, while the third, a product of the merger of technologies, tends to focus on the unique requirements of the new computerized-PBX user.

The existing electromechanical-PBX population is almost 250,000 in the U.S. Therefore, it is reasonable to expect additional entries into this new application area. In addition, the growing demand by users for greater operational flexibility and management control of their total communications environment will necessitate introduction of systems that solve existing and new problems. □

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And now the EXORciser has additional company . . . options to make it even more flexible, even more versatile.

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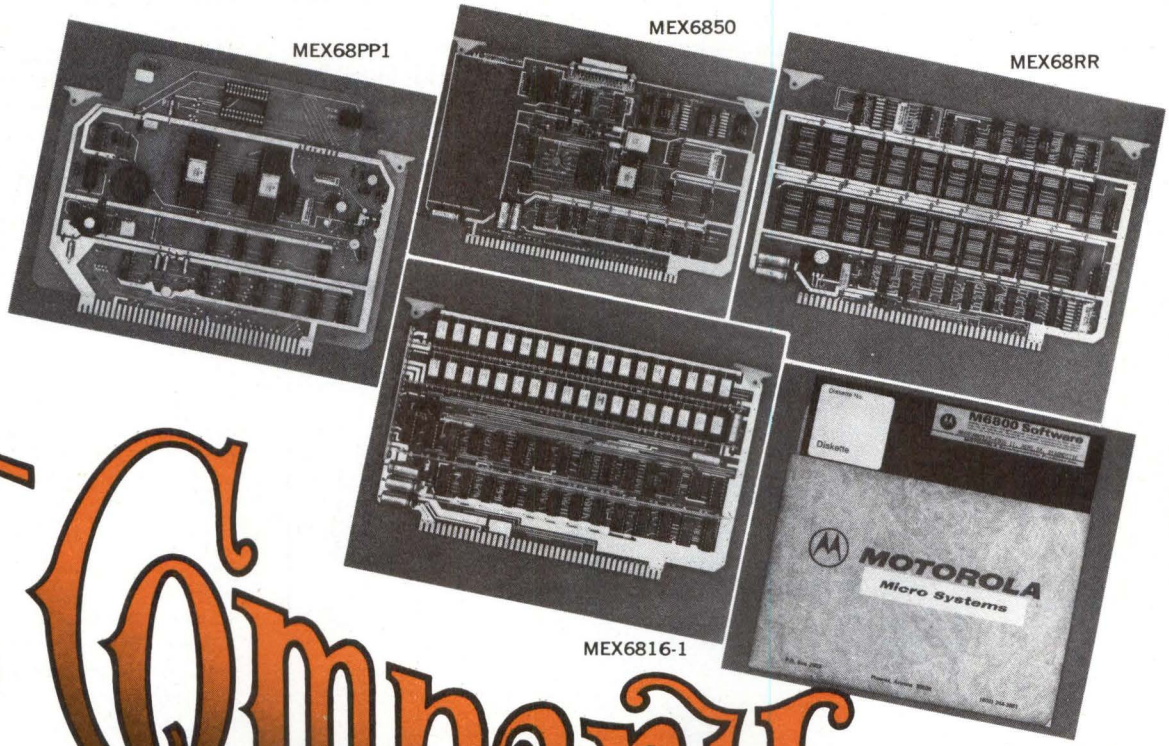


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There they are, **EXORciser et Company,** some of the tools so vital to trouble-free M6800 systems development. There are others, of course. M6800 software: from commercial time-sharing, to host computer packages, to the EXORciser resident packages, to the high-level language MPL compiler. The hardware: from the EXORtape* paper tape reader to the EXORdisk* floppy disk system. Before you design anything with microprocessors, know all you can about Motorola's total product approach. Write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number for copies of the latest data. All Motorola data sheets are also now available from VSMF Data Centers.

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## Bulk Core System Bridges Gap Between Main Memory and I/O Devices

An unusual approach to secondary or bulk storage, a core memory module, offered by Modular Computer Systems, 1650 W McNab Rd, Fort Lauderdale, FL 33309, combines the speed of conventional core memory subsystems with the major data transfer characteristics of traditional secondary memories, at low cost and with some advantages distinctly its own. Providing from 256K to 4M bytes of storage capacity, the Memory + system operates with effectively zero latency, and achieves word transfer rates of 1.25 to 5M bytes/s while eliminating the need for battery backup associated with semiconductor memories.

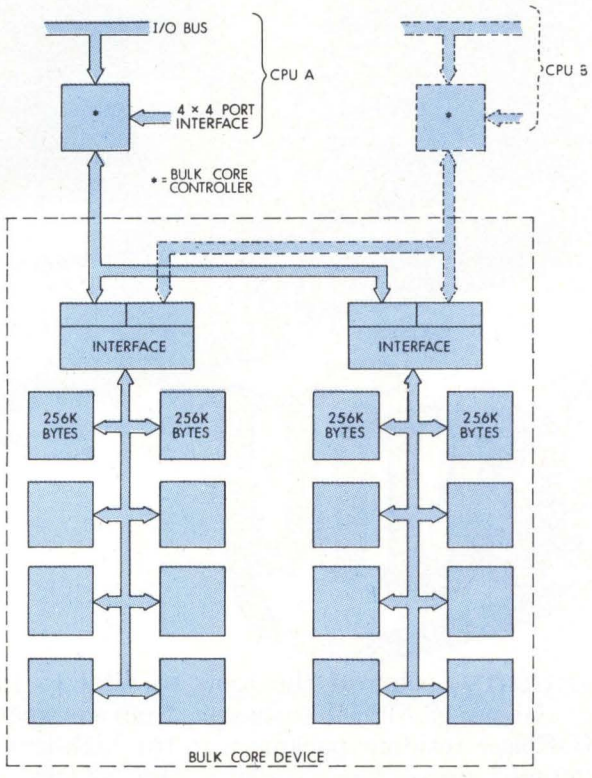
Traditionally secondary memories have taken the form of magnetic tapes or discs where large quantities of data could be stored at a very low cost per bit, and brought to main memory in large chunks under program control. Where speed was important, preferred technology was the fixed-head disc, which was subject only to the rotational delay of waiting for the desired data block to arrive under the read head, but not to the delay imposed by moving a read head from one track to another. More recently, all-solid-state systems based on such technologies as charge-coupled devices and magnetic bubbles have been proposed, which would eliminate the mechanical disadvantages of discs.

Now however, Memory + developed in a joint effort between Dataram Corp, Cranbury, NJ and Modcomp, takes another approach. This system is described by Bernard F. Hellrigel, chief engineer at Dataram, and Thomas A. Hughes, director of hardware development for Modcomp, as returning to an old technology to achieve secondary storage at costs competitive with those of fixed-head discs, yet providing the capability of transferring data in large blocks at high speed but with essentially zero latency, which even CCDs and bubbles do not have.

Memory + is a bulk core sytem which provides I/O storage, offering throughput commensurate with main memory and without the latencies associated with rotating mechanisms. Furthermore, Modcomp main memory porting (DMA) architecture permits high transfer rates with minimal impact to I/O bus availability for other I/O devices.

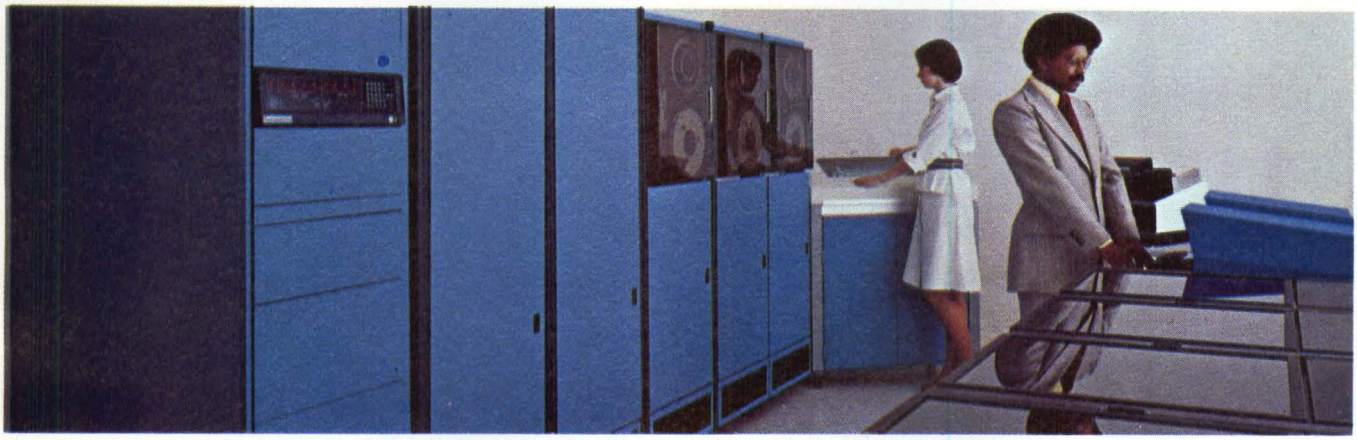
Instead of being implemented on the main memory bus, where the large 256K-byte module would cause greater user interaction, resulting in less effective system performance, the modules are employed on the I/O bus; the system is organized for compatibility with the company's fixed-head disc system to minimize necessary changes to operating system software. When used as an I/O storage system in block address mode with the high speed data path to one of the main memory ports, up to 4-way interleaving of 256K-byte modules provides throughput in the 5 megabyte/s range; with only one 256K module, the rate is about 1.25 megabyte/s. A software I/O handler similar to a fixed-head disc handler makes the implementation functionally transparent to operating system software.

Basic storage element is a random-access core memory—the same technology currently used in most core main memory. However, while current state-of-the-art core memories use 32K- and 64K-byte modules, this system has a 256K-byte module that is organized as 128K 16-bit words, plus parity. According to Hellrigel




256K-byte modules are used in Modular Computer System's Memory + bulk core storage system to permit cost savings, increased reliability, reduced power consumption, and improved packaging density. The system is implemented over the I/O bus and is organized for block transfers to provide compatibility with fixed-head disc subsystems

# INTERDATA 8/32 MEGAMINI LIFE SUPPORT



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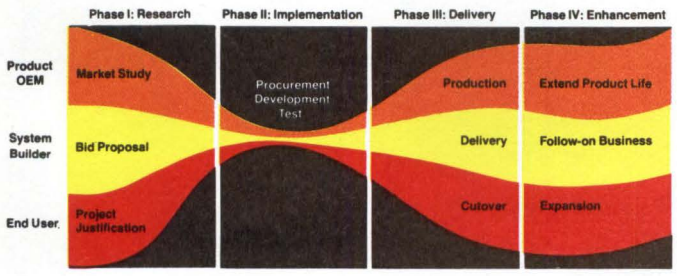


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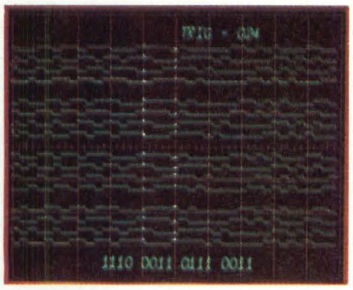
# TEKTRONIX logic analyzers

# for the digital domain



Timing and binary information together with intensified trigger marker and cursor displayed by the 7D01 Logic Analyzer. The number of sample intervals from the trigger point to the cursor appears at the top of the display; data stored at the cursor position is displayed in binary across the bottom of the crt.

## New Plug-ins with Expanded Capabilities

For digital design and testing applications, you'll find that Tektronix Logic Analyzers and Oscilloscopes are literally made for each other. To expand your digital analysis capabilities, choose either the 7D01 Logic Analyzer (a new plug-in for our 7000-Series laboratory oscilloscope family) or the LA 501 Logic Analyzer and its new companion plug-in, the WR501 Word Recognizer (these two are packaged as modular TM 500-Series instruments to work with almost any oscilloscope).

Features these analyzers have in common include:

- **16 Channel Operation**
- **15-ns Asynchronous Timing Resolution**
- **4k Memory to Store Pretrigger Data**
- **Word Recognition**
- **High Z Probes**

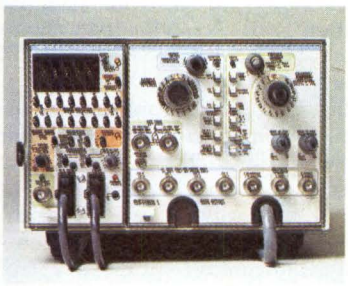
For versatile data acquisition, these logic analyzers let you select the number of channels and the resolution best suited to specific applications:

**16 Channels, 20 MHz, 256 Memory Bits**

**8 Channels, 50 MHz, 512 Memory Bits**

**4 Channels, 100 MHz, 1024 Memory Bits**

You'll like what we've done to **reduce circuit loading problems** associated with testing high-speed and high-impedance logic families. With our new P6451 active probes, which have an input impedance of **1 MΩ paralleled by 5 pF at the probe head,** you'll be able to test virtually any logic family.



## LA501/WR501, Members of the TM 500 Series

Take your logic analyzer right to the problem with the LA 501 Logic Analyzer and its new companion word recognizer, the WR 501. Packaged as modular TM 500 test instruments, this pair works with any oscilloscope or X-Y monitor. Now you've got versatile logic analysis capabilities to complement the oscilloscope you probably already own.

**Word recognition with digital delay** gives you fast access to almost any location in the data stream.

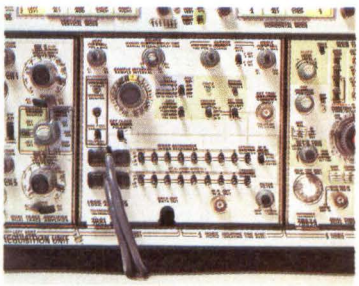
For **channel-to-channel timing comparisons,** you can select any trace and position it next to any other. And **timing tic marks** on each channel enhance visual analysis.

No matter what your application—design, production testing, or service we've got a TM 500 logic analysis configuration for you.

On the bench, power the LA 501 and WR 501 with the TM 503 mainframe or the TM 504 mainframe (now you've got room for another TM 500 module like the DMM 502 Digital Multimeter).

In a rack, use the RTM 506—there's room enough for the LA 501, the WR 501, the SC 502 Oscilloscope, and one more module. Or you can mount the LA 501 and WR 501 in a TM 503 side by side with a 604 Monitor. The 6½-in. display is easy to read.

For **field portability,** try the TM 515 Traveler Mainframe. It's rugged and durable, yet as attractive as carry-on luggage. You can pack the LA 501, the WR 501, and the SC 502 and have a complete logic analysis system in a suitcase.



## 7D01, A Member of the 7000 Series

Turn any 7000-Series laboratory oscilloscope into a versatile 16-channel logic analyzer with the new 7D01 dual-wide plug-in. Now, gaining logic analysis capability is as simple as adding a plug-in.

With a four-compartment 7000-Series mainframe and plug-ins, you get a truly powerful logic design tool: **a logic analyzer and a real-time oscilloscope in one unit.** Use the 7D01 Logic Analyzer to locate a digital domain problem, then zero in for detailed analysis by using the 7D01's word recognizer to trigger the analog portion of your oscilloscope. Now you can do it with one instrument and display your digital and analog information on the same crt.

With the 7D01 you also get **timing and binary information displayed simultaneously** on the crt. You do it with a cursor. And because the cursor can be moved in single clock intervals, **timing comparisons are faster, easier and more error-free than visual estimates.** When the cursor is moved to a given clock position, the binary word at that point is read out across the bottom of the display.

The LA 501/WR 501 and the 7D01 Logic Analyzers will be on display at ELECTRO76. Stop by our booth for all the details and a hands-on demonstration. If you can't make it to the show, call your nearby Tektronix Field Engineer or write Tektronix, Inc., P.O. Box 500, Beaverton OR 97077.

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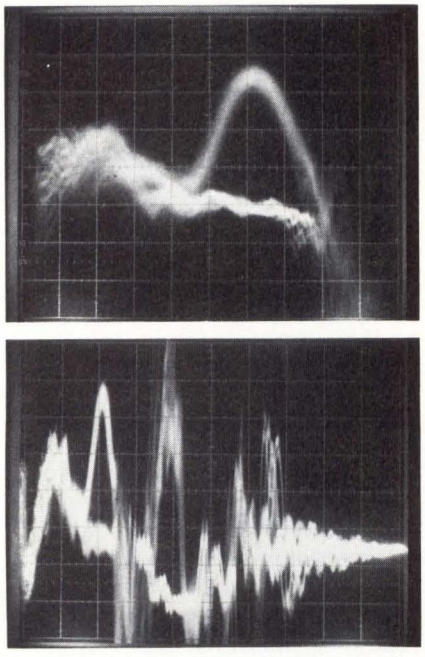
and Hughes, using this size module instead of four 64K-byte modules permits approximately a 2:1/bit cost savings, results in greater than 2:1/bit MTBF enhancement, significantly improves per bit packaging density, and achieves more than 2:1/bit power consumption savings. The resulting cycle and access degradation is about 25 to 50%.

The storage module, designated DR-128, consists of an electronics board and core stack assembly. Core memory stack consists of a continuously strung 128K x 18-bit core array which is folded around the four surfaces of two PC boards that are hinged together to allow easy access to any core area. Industry standard 18-mil, medium temperature range, ferrite cores with 780-mA nominal drive and 100/200-ns peaking/switching times are used. 3D/3-wire organization achieves access and cycle time specifications of 600 and 1500 ns, respectively.

Sensing and inhibiting of 32K cores are performed on a single sense/inhibit line. By choice of a non-square aspect ratio (64 Y x 512 X) for each sense line, the signal-to-noise ratio during strobe time is optimized. Under worst pattern conditions, delta noise consists of Y delta pair contribution and X delta pair contribution. The aspect ratio presents 255 Y delta pairs and 31 X delta pairs, making the Y pair contribution very large compared to that of a normal 8K sense line. To overcome this, the read Y current source is turned on 200 ns earlier than the read X current source, settling out the Y noise contribution prior to strobe time, leaving only the X delta pair noise contribution.



To illustrate the effect of strobe modulation on 32K sense waveform worst pattern core signals, the sense amplifier strobe was used as the oscilloscope sync. Upper photo has 50-ns strobe; the lower photo, 200 ns

For optimum flexibility, the storage module has a TTL-compatible asynchronous "handshake" interface. The electronics/stack assembly includes data and address registers which make it completely self-contained. Low power Schottky-TTL circuits are used extensively to minimize power consumption and input signal loading. Total power consumption is 18 W (7.8 $\mu$W/bit) in standby and 95 W (40.4 $\mu$W/bit) when operating "all zeros" at a 1500-ns cycle time.

Capable of driving one device, the system controller is similar to that used with most high speed devices with two exceptions: data buffering is not required, since there are no overflow implications in the core memory; and the interface for data transfers to and from main memory requires the controller to have virtual mode addressing for managing main memory greater than 64K words. If a main memory port is not available, data are transferred via the I/O bus, at a rate limited only by I/O throughput ability.

A second identical controller, connected to the second port of the interface, allows a second computer to access the device. Controller-to-device interface provides for requesting priority or taking exclusive use between controllers.

Circle 140 on Inquiry Card

## CPU Implemented With Cache, Control Store To Speed Execution

Claimed to rival the performance of a PDP-11/70, the model 400 central processor with up to 8M bytes of MOS main memory, announced as part of the TEMPUS line by Prime Computer, Inc, 145 Pennsylvania Ave, Framingham, MA 01701, offers 512M bytes of virtual memory to each of 64 simultaneous users, supports up to 1.2G bytes of online disc storage, and provides a data transfer rate of up to 2M bytes/s. Performance is attributed to the design and implementation of three interrelated features: cache memory, high speed arithmetic unit, and microprogrammed control store. Cache memory increases the apparent speed of the main memory, while the arithmetic unit and control store speed instruction times by reducing the number of steps and the time for each step in instruction execution cycles.

Implemented as 2K bytes of bipolar, Schottky-logic memory, cache memory uses a complex algorithm to store whatever information is most likely to be used next in program execution. The 80-ns access time for the next instruction substantially increases the apparent memory speed. In typical applications, the cache "hit rate" will be about 85%, giving main memory an apparent speed approaching that of the central processor.

Working in conjunction with cache memory to increase effective memory speed and system throughput, main memory is interleaved. Consecutive memory locations are on separate memory modules, permitting the processor to read or write two 16-bit words at a time, for a 32-bit effective data transfer. Speed and reliability are effectively balanced by the use of 2-way interleaving.

Use of segmented virtual memory addressing and paged memory mapping allows each of up to 64 simultaneous users to access a virtual address space of up to 512M bytes (4K, 128K-byte segments). Segmented memory management resources, a combination of hardware, software, and microcode, automatically and transparently perform the physical mapping of main memory and the allocation and sharing of memory resources among all active users and tasks.

An "embedded" PRIMOS IV operating system, implemented partially in memory resident software and partially in microcode, makes all operating system functions immediately available to all users simultaneously. Since the operating system supervisor is embedded in each user's virtual address space, it can behave as a subroutine or program module callable by the user. Other operating system features include dynamic linking, which permits program modules to be linked as needed during run-time, rather than being statically linked at load time; process exchange, which minimizes operating system overhead and maximizes re-

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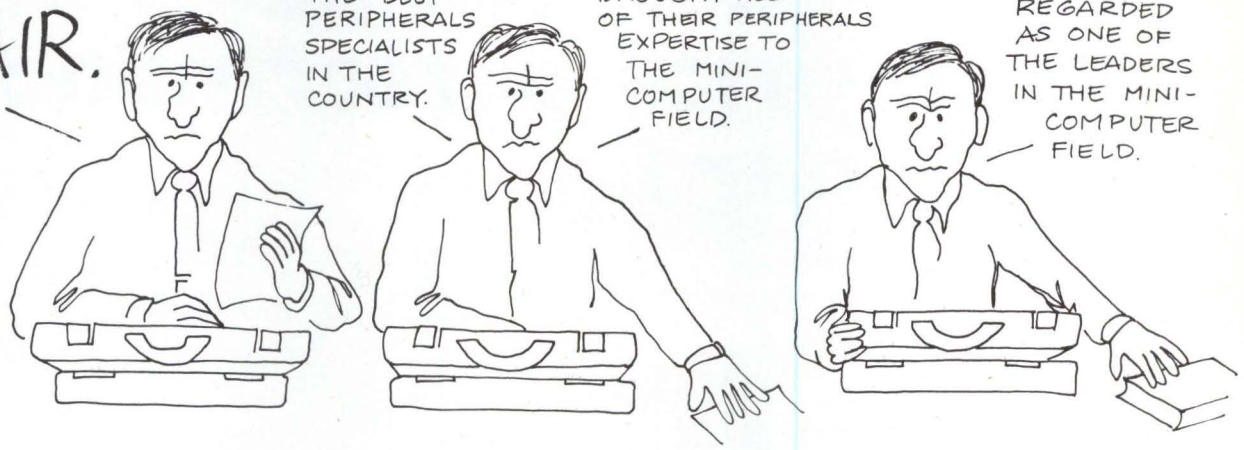


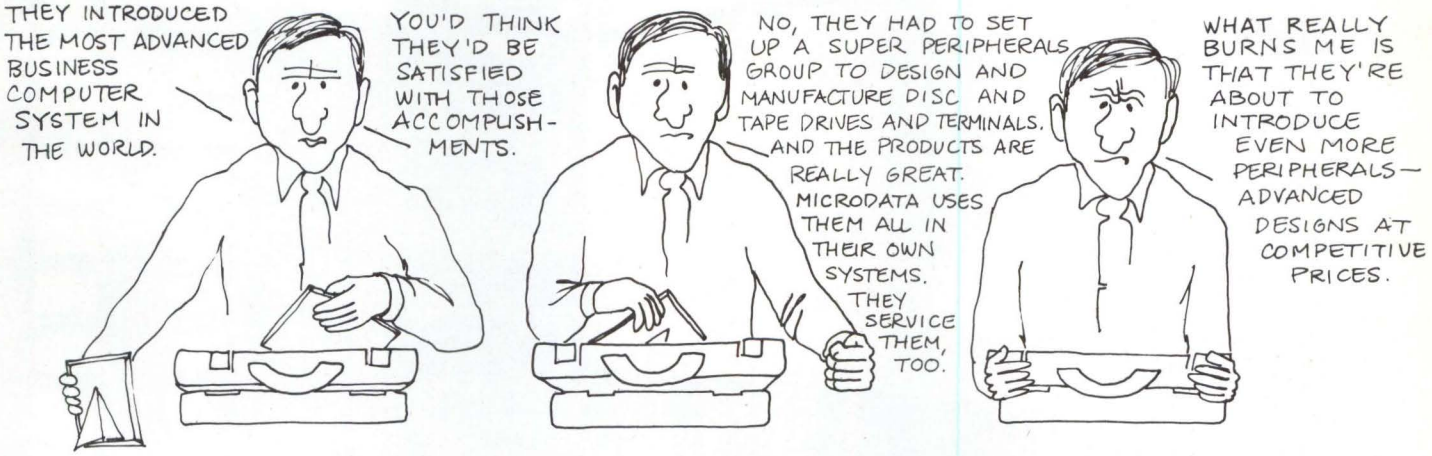

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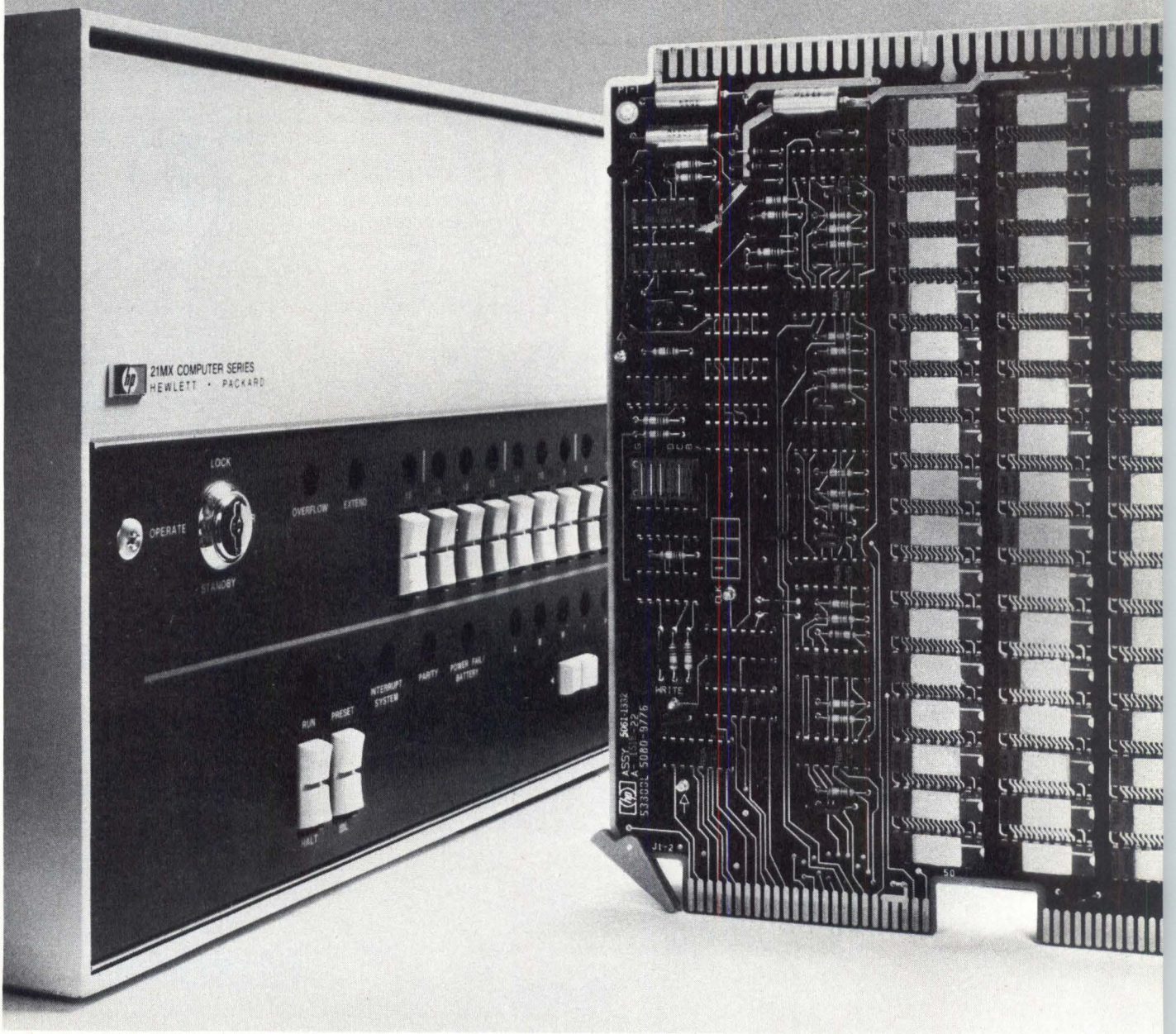
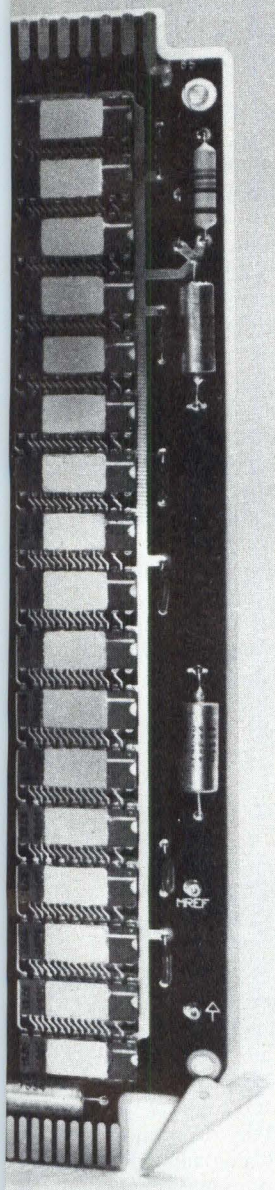
# The Hewlett-Packard 21MX minicomputer sets a new price/performance standard.



# Announcing 16K word memory with parity for $1386.*



Because the majority of a minicomputer's cost is its memory, the $1386 price for HP's new 16K word parity memory module is a significant price/performance breakthrough. And when you consider the low-cost memory along with the other features of the 21MX, it's a combination that's hard to beat. At any price.

**Proven 4K RAM Reliability.** Hewlett-Packard pioneered minicomputers with 4K RAM memory. Our unequalled field experience with more than 250,000 4K RAMS has proven their reliability. Solidly.

**Doubled Memory Capacity.** Now pack double the memory into your dynamic 21MX minicomputer. Put up to 32K words in 5¼" of space, or up to 128K in 13", without giving up a single powered I/O slot.

**21MX Performance Extras.** Each HP 21MX gives you more of what you buy a minicomputer for. Standard features that often are extra-cost options from others include floating point and extended arithmetic, brownout-proof power supply, ROM bootstrap loader, power-fail interrupt capability, and a full front display panel.

**HP's Worldwide Service and Support.** We're on the spot to provide installation, service and support for you and your customers throughout the world.

**We're Shipping Now.** The 21MX minicomputer family with the new 16K memory board is available and being shipped today.

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**Today's Price/Performance Leader.**

| | 16K Add On Parity Memory | Computer† with 64K Word Memory |
|---|---|---|
| HP 21MX | $1386.* | $11,038.* |
| DEC 11/34 | $2046.* | $12,995.* |
| Nova 3/12 | $2368.* | $14,528.* |

†Includes CPU, parity memory, memory management, EAU and battery backup. Source: Datapro
*U.S. domestic price. OEM quantity 50.

**There's More.** Every HP minicomputer and peripheral is designed from the start for easy, "building block" integration. Spend less time on design, and put your system to work faster. Other HP benefits range from installation and software to providing the level of service you specify. Or HP training, if you prefer to do it yourself. If you want more, call your nearest HP field office. Hewlett-Packard, the leader in 4K RAM minicomputers — and a lot more.

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sponse time; a procedure call mechanism, which permits recursive or reentrant coding; and a fast subroutine call for automatic argument transfer.

System integrity is tested using built-in byte parity checking, provided throughout the processor and main memory. Microverification routines, invoked automatically or under program control, test validity of the CPU logic, indicating the cause of a malfunction through a diagnostic status word. Operation in machine-check mode permits the user to determine what remedial action is to be taken for various error conditions; eg, record error but continue processing, stop processor immediately, or initiate automatic restart.

The 400 processor is priced at $71,200 with 256K bytes of main memory. Additional memory is offered in 64K-byte modules for $12,000 or in 256K-byte increments at $30,000 for the first and $24,000 for all subsequent modules. A full configuration, composed of P400 processor with 256K bytes of memory, 100M-bytes disc storage, 30-char/s printer, 75-in./s, 1600-bit/in. tape drive, eight communication lines, and PRIMOS IV software, is priced at $140,000.

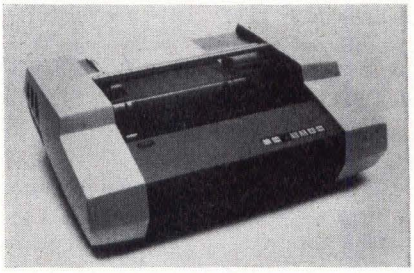
Circle 141 on Inquiry Card

## Systems, Peripherals Incorporate Cost-Cutting Features

A portable computer system and a disc workstation for use in multiprocessor systems, 120-char/s serial matrix impact printer, and a microprocessor-controlled drum plotter were among the products announced recently by Wang Laboratories, Inc, 836 North St, Tewksbury, MA 01876. Each was designed with primary emphasis on producing a low cost product for the small standalone and distributed processor markets. In the case of the printer and plotter, this was accomplished by incorporating some unusual design features.

Design features of the 120-char/s model 2231W series printer include the use of a ribbon that is shaped into a Möbius band and is contained in a lightweight cartridge. Rather than feeding past the printhead from one end to the other and then reversing automatically, this ribbon feeds continuously in one direction, making a half-twist within the cartridge to provide even wear across its width, without requiring that the operator turn the cartridge.

Printer is a dot-matrix unit that prints nine dots in a vertical column, allowing the descenders on lower case letters to be clearly shown. To lengthen the life of the printhead, the wires that print the dots are staggered in two columns of five and four; increasing the amount of bearing structure around each wire and the point of impact and permitting vertically adjacent dots to overlap for a clean print image.



Featuring a dual-axis design bearing plate for greater reliability and a lightweight ribbon cartridge with "Möbius strip" for long ribbon life, Wang Lab's 2231W 120-char/s printer produces from 40 to 250 lines/min.

The printhead is driven by a stepping motor and its position is controlled with a microprocessor, thus eliminating the analog portion of the control loop and the adjustments required by analog controls. Wires in the printhead are driven by solenoids with hollow armatures; solid armatures, frequently used in such printers, although much heavier, are no more effective, since at high operating frequencies they have a skin effect that restricts the magnetic flux paths to a zone near the armature surface.

Designed with a drum that does not rotate, the 2272 series "virtual drum" plotter, is designed such that the end sprocket mechanisms which secure the plotting paper rotate, making plots faster, allowing the use of smaller motors, and resulting in lower power dissipation. As in the printer, stepping motors control the position of the paper and of the plotting pen, moving parallel to the drum axis. Analog servomotors and linearizing circuitry commonly used in drum plotters are eliminated by sending X,Y coordinates directly into an Intel 8080-type microprocessor which digitally linearizes the motion by controlling the stepping motors. Addition of a ROM permits the processor to generate a 64-character ASCII set, allowing plots to be labeled without adding overhead to the central processor.

The 2200 PCS portable computer systems are directly competitive with IBM's model 5100 (see *Computer Design*, Nov 1975, pp 130-131). Completely contained within a 55-lb desktop console that can plug directly into a wall socket, the unit consists of a 2200 central processor with 8K bytes of semiconductor RAM (expandable to 32K) and 42.5K bytes of ROM, a 9" CRT display with full alphanumeric keyboard, plus a tape cassette for data storage and program loading. The unit is programmed in an extended version of BASIC. Asynchronous and synchronous telecommunications options will be available in June for use in tying the system into large central computers for distributed processing applications.

Attaching to multiplexers on 5- and 10-megabyte discs, the 2200 WS disc workstations include a complete minicomputer with 12" CRT display/keyboard and 8K-bytes memory (expandable to 32K bytes). Intended for use as components in multiuser, multitask, multiprocessor systems, up to three workstations can be multiplexed to one system; the central processor console can serve either as a fourth workstation or as a system monitor. A typical multiprocessor configuration consists of 2200 CPU with 5-megabyte disc, 16K-byte memory, 200-char/s printer, removable diskette, three workstations, and a disc multiplexer.

Circle 142 on Inquiry Card

## Data Entry System Combines Local Storage with Intelligent Terminal

Combining intelligent terminals with local storage media, hardcopy printers, and comprehensive applications software, model 200 provides the flexibility to handle a range of applications. Announced by Computek, Inc, 143 Albany St, Cambridge, MA 02139, CDES configurations concurrently perform I/O tasks such as printing or file management, with-



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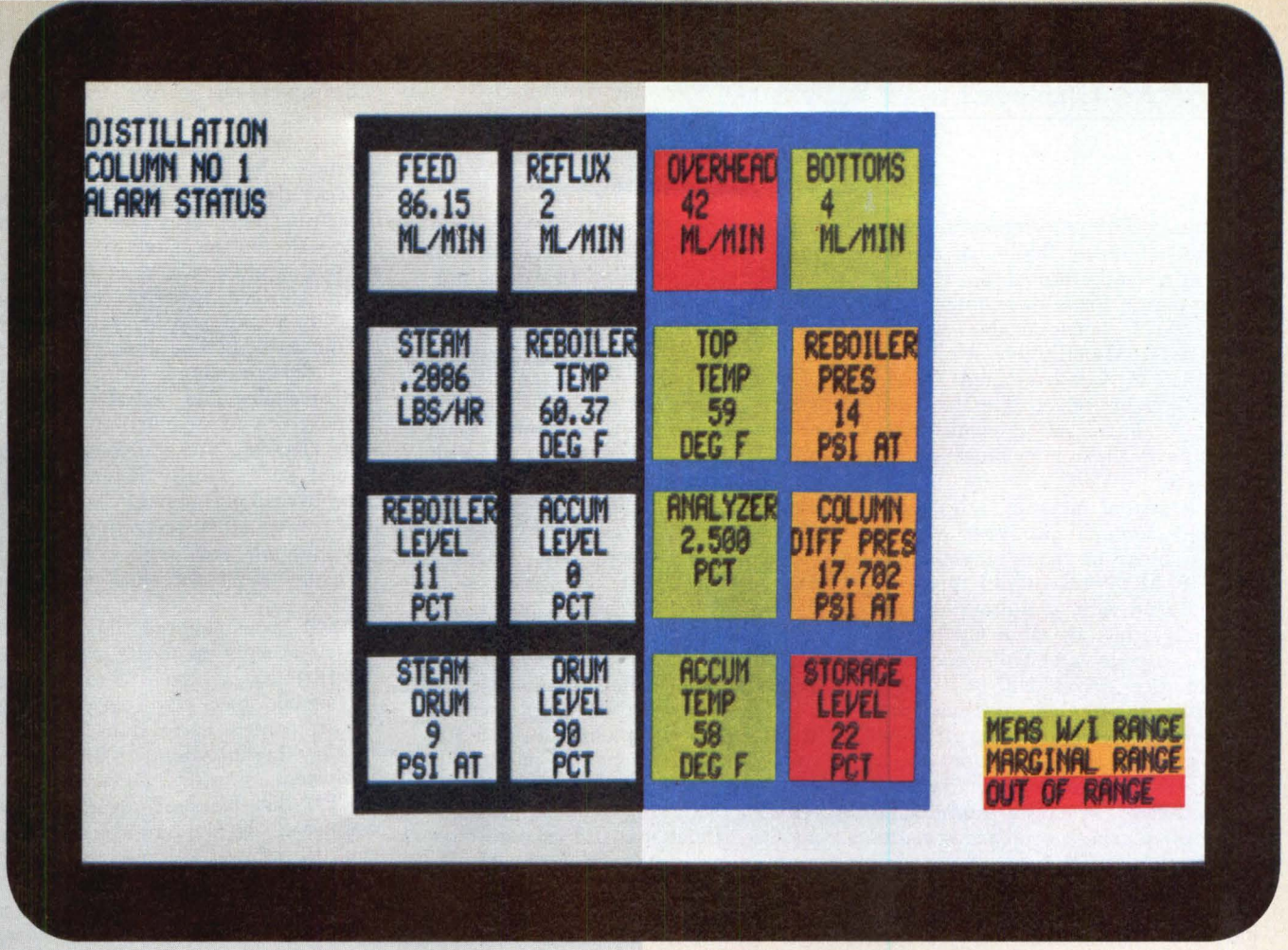


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For the black and white side, take the MRD 380 or the MRD 980. The 380 is a basic teletypewriter compatible unit; the 980 is more advanced. Both are in a class by themselves, packaged to fit in anywhere. ADDS developed them specifically for the process control industry.

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MRD 380, $1195 MRD 980, $1995.

There's another side to the story. The MRD 460—a real show-off. Put it where you need it, and it'll show you what's what in eight snappy colors. If rapid visual indentification of information is important, the 460 is for you. It features graphics, formatting and extensive remote controls. ADDS developed it specifically for the process control industry.

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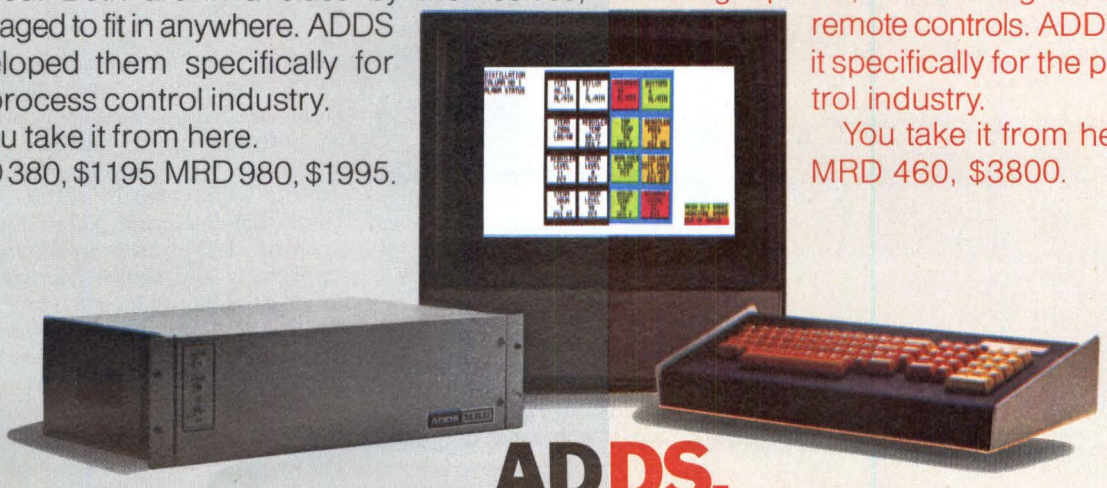
MRD 460, $3800.



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out halting data entry operation; provide 480-, 960-, or 2000-char screens with characters formed on a 20 x 14 dot-matrix for high legibility; and use 3740-compatible flexible diskettes for IBM compatibility. Units are available in self-contained single-station systems which operate stand-alone, or in clustered workstations which share the system processor and peripherals.

Each system includes a high performance terminal processor with up to 32K bytes of memory (combination of MOS read/write programmable, read-only, or programmable read-only), one or more CRT workstations, up to six 3740-compatible flexible disc drives with 240K-byte capacity for program and local data storage, 165-char/in. or 220-line/min. printer, communications interface, and terminal-resident data entry software. Processor architecture provides a single-source/destination transfer bus which uses 10-bit data words and 16-bit instruction words, permitting 2-address moves, and allowing an effective 650-ns processor cycle time.

The system's master console may be housed in a desk along with the terminal processor and diskette drives or may be used as a workstation. Other workstations are keyboard/displays located up to 50 ft from the system processor. The system communicates with an IBM host processor using binary synchronous discipline at speeds to 9600 baud.

CDES operating software consists of a forms creation program (EASY-FORM), supervisor program, and one or more data entry programs. Each module is operated under a real-time operating system which schedules tasks and allocates system resources; each is executed right at the terminal without host processor intervention.

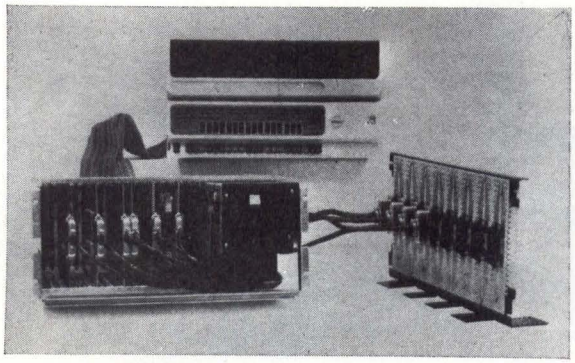
The supervisor controls and monitors system use, permitting terminals to be opened and closed, data programs to be loaded, and initialization programs to be implemented. It also makes available detailed statistics on operator performance. Data entry programs initiate and control terminal activities, provide file management functions, and execute communications with the host. All file formatting is done on-the-fly as data are actually being stored; thus, no reformatting need be done.

Typical configuration prices are: model 200/D10, with single workstation—$15,625; model 200/D20 with two stations—$17,960; and 200/D40 with four stations—$19,990.

**Circle 143 on Inquiry Card**

## Sensor Subsystem Eases Computer Interfacing for Automation Systems

For industrial automation systems builders who need comprehensive I/O support for many lines, the data acquisition and control subsystem handles more than 1000 lines and features a comprehensive I/O function card library as well as designed-in dual porting capability. Developed by Data General Corp, Southboro, MA 01772 to ease interface problems between Nova® and Eclipse® computers, and sensors and control devices, the DG/DAC (Data General/Data Acquisition and Control) subsystem features modular design for simple installation, service, and expansion, and rugged packaging to ensure reliable operation in rugged environments.



Data Acquisition and Control subsystem eases interface of sensors, actuators, and associated electrical circuits to Data General's Nova and Eclipse computers. Chassis and power supply are shown on left with several function cards; subsystem hardware includes terminal board (right) with capacity for 128 signal lines

Subsystem chassis are accessed and controlled by computers through a chassis control card which provides interface electronics between chassis backpanel and the computer's I/O bus; using two cards allows the subsystem to be accessed by two separate computers for critical applications. Thirteen types of printed circuit input and output control cards handle a variety of analog and digital industrial signals. Any combination of analog and digital cards may be mixed in any configuration in the same chassis. Card-addressing is slot-related with priority determined by the physical position of the card in the chassis; this serves to simplify configuration and reduce the hardware necessary for smaller applications.

Each rack-mounted model 4300 chassis accepts up to 16 plug-in I/O function cards. Each card handles 16 signal lines. By daisy-chaining chassis control cards, multiple chassis may be incorporated in a single subsystem.

CPU line-handling overhead encountered in larger configurations can be reduced through use of the optional Data Control Unit (DCU) for interfacing chassis to computer. The DCU is a dedicated I/O processor that converts programmed I/O for data acquisition and control into data channel transfers.

Four A-D converter cards (models 4280, -A, -B, and -C) provide a selection of high level voltage ranges. One card controls up to 15 analog input multiplexer cards, each handling up to 16 channels. Model 4085 wide range subsystem allows A-D conversion of low level analog signals, including thermocouples; it is a separate chassis interfaced through the 4300 chassis; separation of chassis ensures accuracy and increases the number of lines handled.

Two digital input cards (4290 and 4291) interface all common digital input signals. The 4290 accepts 16 inputs from 6 to 55 Vdc or 15 to 135 Vac in any mix. The 4291 TTL digital input card handles up to 16 TTL input lines and an external interrupt trigger line.

Software support for the subsystems in single- or dual-computer environments is provided by a library of device handlers and subroutines that control I/O transfers between user programs and sensor hardware. The sensor access manager (SAM) works with the computer's real-time multitasking operating systems (RTOS, RDOS, or MRDOS) and FORTRAN compilers to simplify sensor monitor and control programming.

**Circle 144 on Inquiry Card**



*(Continued on p 67)*

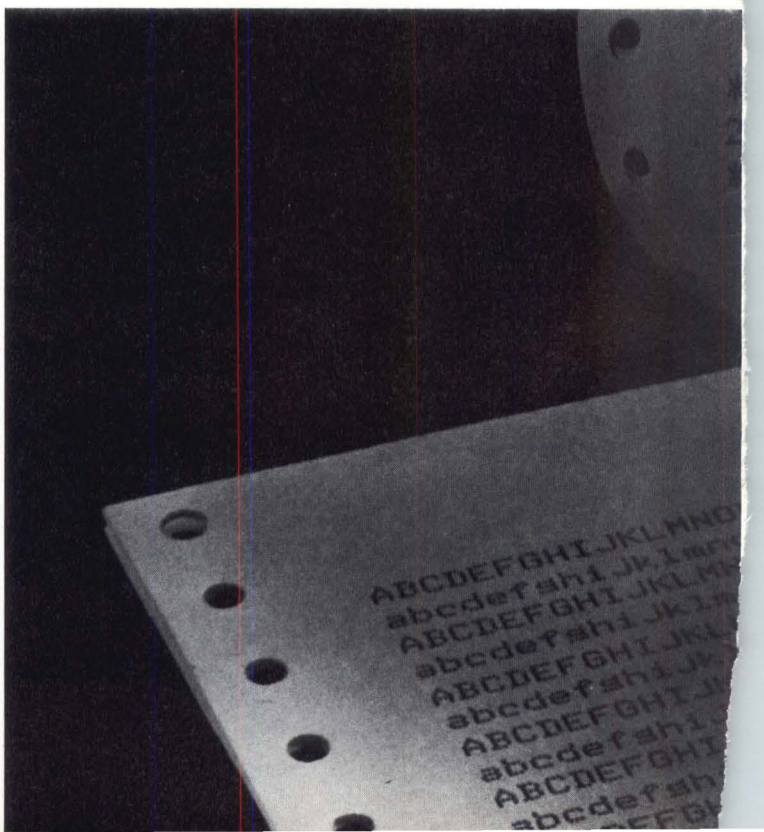
# DECprinter

DECprinter is a small, quiet line printer for use with computer systems requiring a low price, low operating costs, exceptional reliability, and high throughput.

# DECprinter–Digital's LA180 line printer–performs better and more reliably than any second-generation, 180cps printer terminal.

Compare DECprinter's user-benefiting features:

- ☐ 60 to 400 lpm, depending on line length.
- ☐ Lowest price, best reliability in its class
- ☐ Parallel interface, serial line interface option
- ☐ Full ASCII 128-character set–96 upper and lower case letter, numeral, and symbol printing set
- ☐ Full 132-character line length capability (10 characters per inch) allows use of standard line printer forms
- ☐ Positive tractor feed advances paper precisely without slipping or misalignment of multipart forms
- ☐ Movable left tractor lets you position forms horizontally for precise column alignment with preprinted forms
- ☐ Movable right tractor lets you use forms as narrow as 3 inches and as wide as 14-7/8 inches
- ☐ 11 Switch-settable form lengths
- ☐ Manual print gap adjustment for uniform image density with single or multipart forms
- ☐ Multipart forms can be up to 20 thousandths of an inch thick, with up to five copies plus the original
- ☐ Vertical vernier adjustment allows exact print head/form registration
- ☐ Unique print head design offers excellent readability and print quality over long product lifetimes with heavy duty cycles
- ☐ Backspacing capability for strikeover character formation

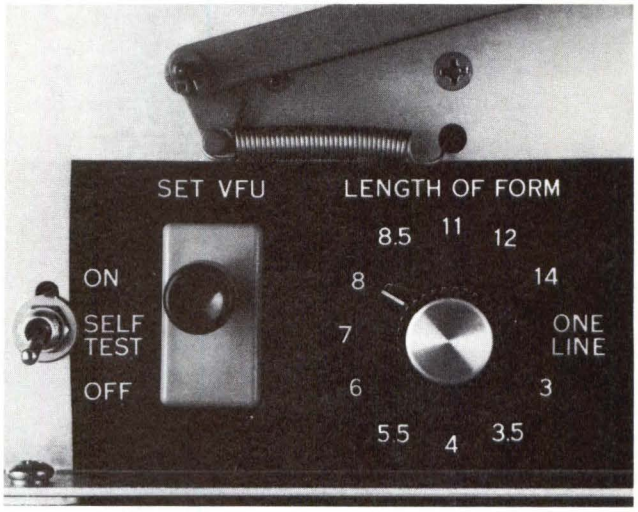


DECprinter prints easily read upper and lower case characters formed in a 7-by-7 dot matrix positioned precisely by a proprietary new carriage system.

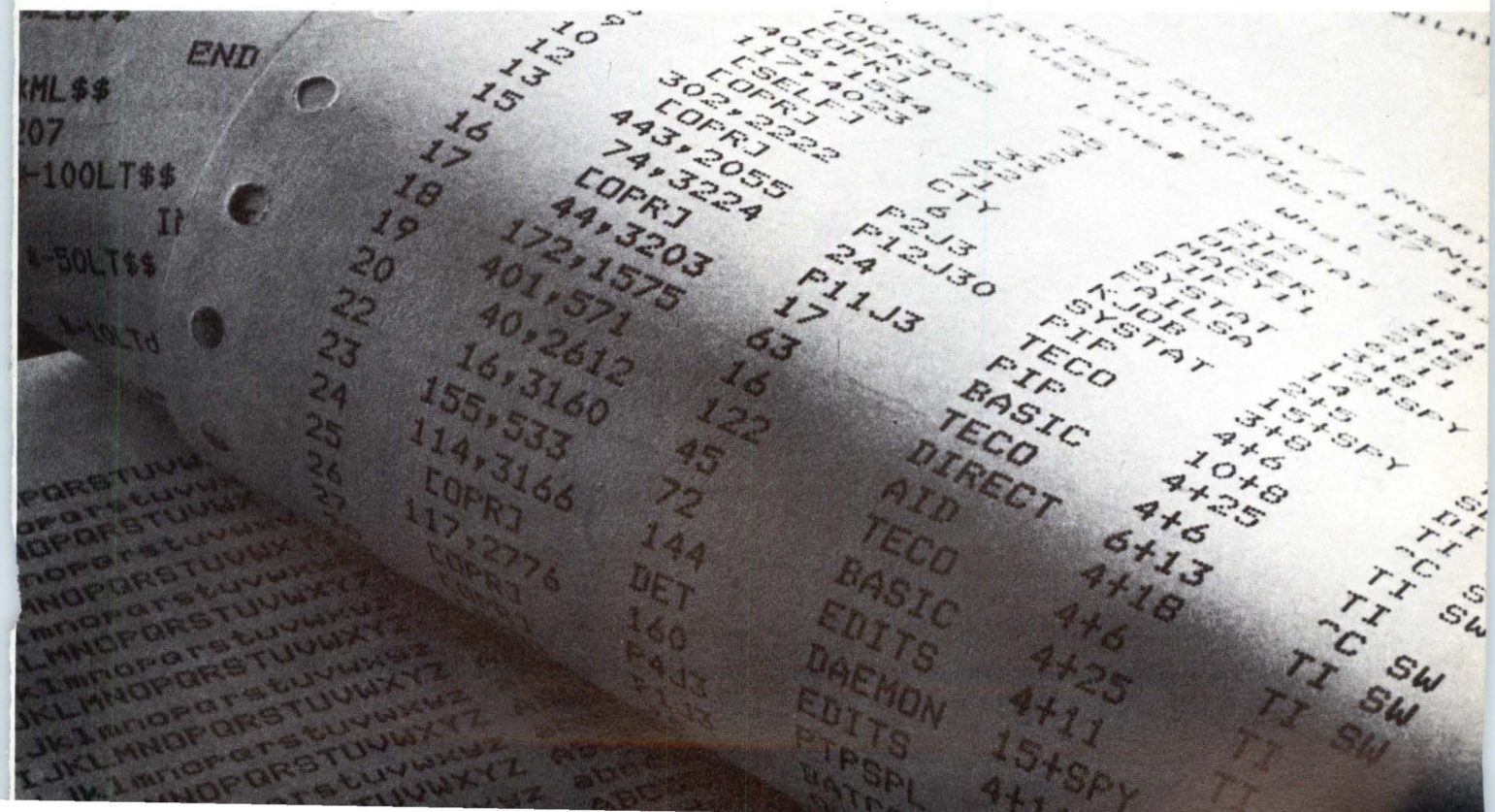
# Introducing DECprinter, the low-cost, reliable line printer.

DECprinter, the LA180, is a fast, small, quiet, and reliable printer for use as an economical hard-copy device in remote or local output applications. A parallel transfer device, DECprinter offers improved throughput, reliability, print quality, and form-handling versatility at a price well below other comparable printers.

It's quiet, fast, and reliable. Form-handling versatility and exceptionally good print quality make it an ideal choice for applications in which xerography or carbon copies are distributed. Its design is based on Digital's LA36 DECwriter II keyboard printer terminal, which has become an industry standard. Several of its key components and operating mechanisms incorporate Digital's extensive experience with the keyboard terminal.



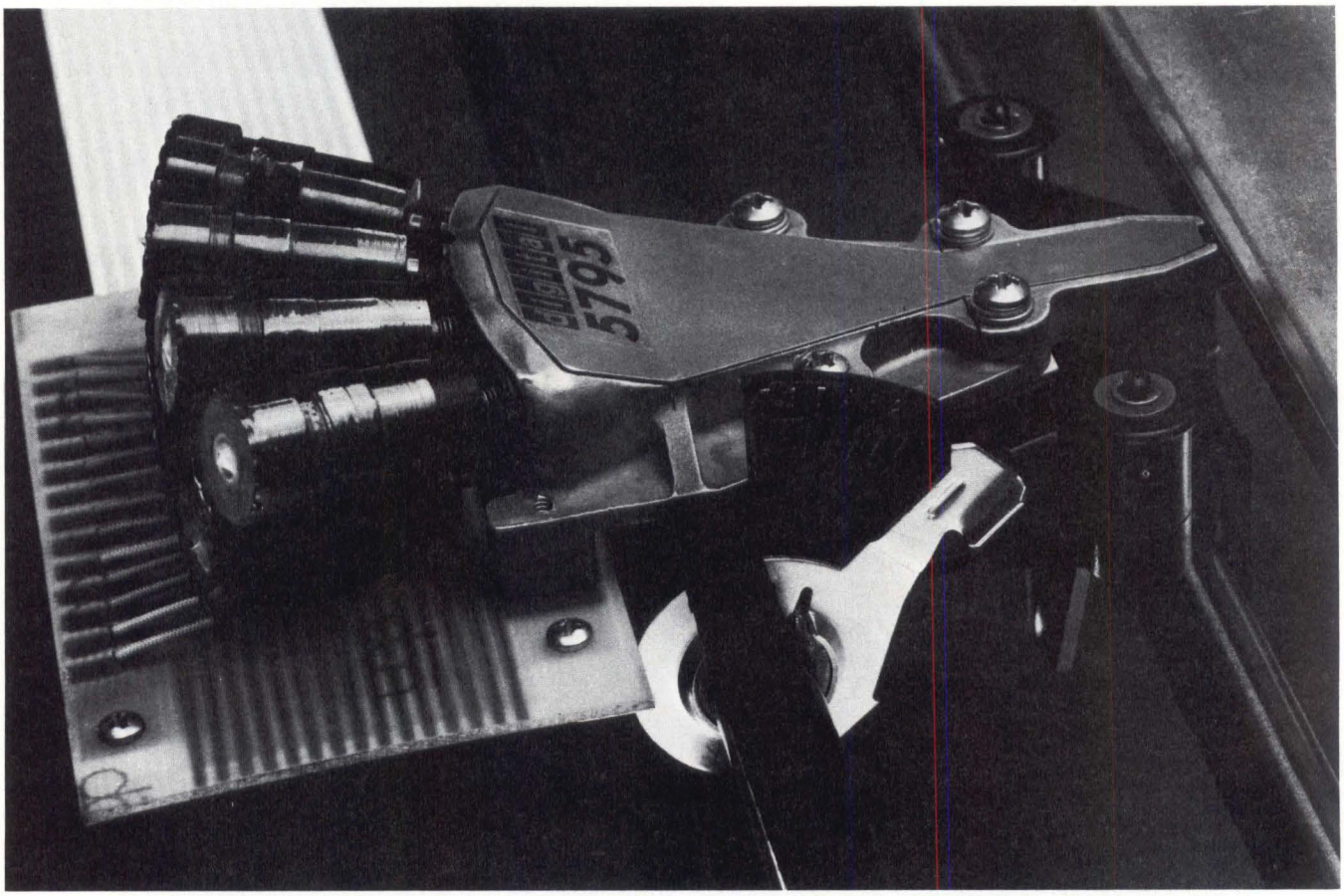

The self-test provision of the DECprinter enables the user to check the printer's operation simply by throwing one toggle switch. The printer can be made to initialize at the top of the next form, and various form lengths can be selected with a rotary switch.



# DECprinter is fast and versatile.

DECprinter makes 132-column printing standard, so that you can use the same forms on keyboard printers, large line printers, and small line printers. Different forms and paper are no longer needed, saving you the inconvenience and cost problems of special papers and special sizes.

Six-part form printing is a standard DECprinter feature, resulting from the use of extremely reliable tractors like those used on large line printers. The left tractor can be adjusted from side to side to provide precise horizontal placement of the printed image within preprinted formats. The right tractor can be moved to accept any paper width between 3 and 14-7/8 inches. A vernier adjustment of the paper feed mechanism knob permits precise vertical positioning.




The detent-secured lever at the right center allows the user to produce uniform print image density with from one to six pieces of paper in the form pack. Total pack thickness can be up to 0.020 of an inch.

# Design is based on a new industry standard.

DECprinter's print head—the crucial element in any matrix printer—is based on that used in Digital's DECwriter II. Extensive field experience has proven the DECwriter print head the most reliable and longest-lived available.

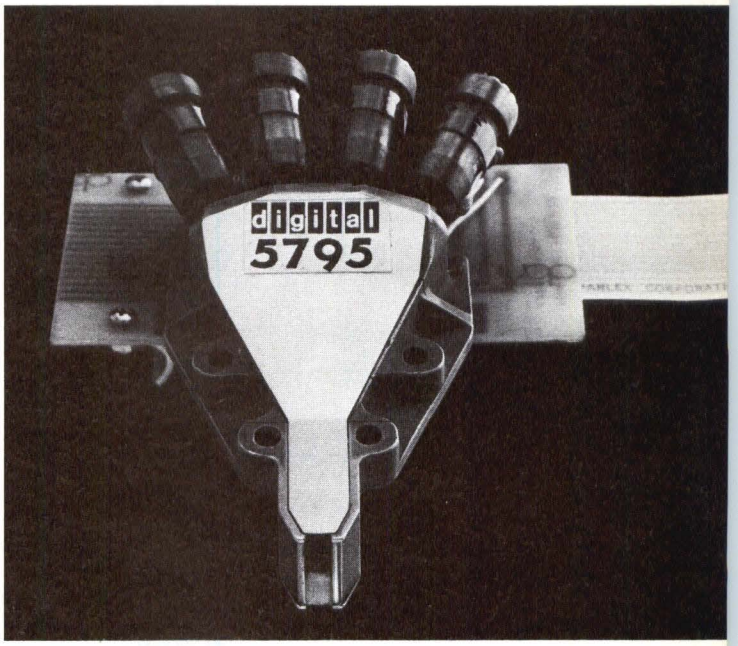
More than 20,000 DECwriter IIs—the LA36—were delivered in the product's first year, and the LA36 quickly became the new standard of performance in the keyboard printer market place.

The impact wire curvature and design of the wire support structure in the head are derived from a computer simulation program to minimize fatigue and wear. A sink protects the head from overheating.

The wires are permanently lubricated to reduce wear in the head, and material was chosen for most effective resistance to wear by the ink ribbon. To further reduce tip wear, as well as eliminate image blurring, the ribbon advances while the head is printing, and the ribbon is nonabrasive.

A constant-current drive circuit—not the more common constant-voltage method—controls wire motion. This technique eliminates motion variations produced in other printers by heat-caused resistance changes and resulting current changes. The effect is uniform impression density, from first character to last.

Motion of the impact wires in controlled by a constant current through the driving solenoids, making the consistency of the printed image independent of variations in temperature and resistance. Wire wear is minimized by a ruby-sapphire bearing at the print head tip.



20-times magnification of the tip bearing.

# DECprinter is designed with the user's needs foremost.

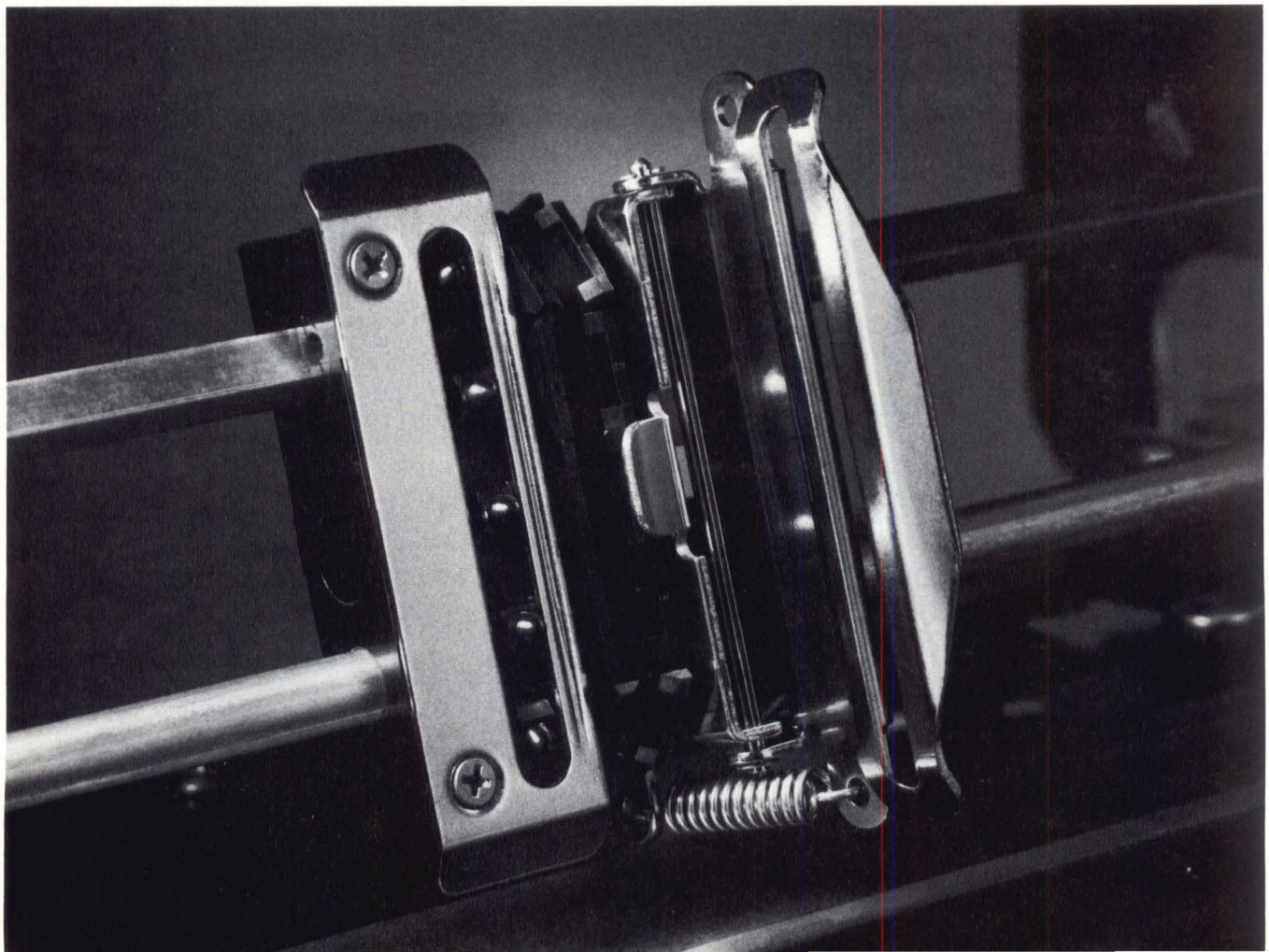
DECprinter's mechanisms eliminate the noise problems typical of line printers. The print head design is a key factor. An adjustable print gap, for example, minimizes print wire travel and resultant noise. And small, quiet fans provide all the cooling needed, due to extensive heat-sinking and low power consumption.

You can reproduce with confidence from DECprinter's output. Its 7 x 7 dot matrix prints a far more legible image than conventional 5 x 7 designs. In addition, the DECprinter carriage subsystem is designed and engineered for precise dot placement, eliminating incomplete, smeared, or unreadable characters.

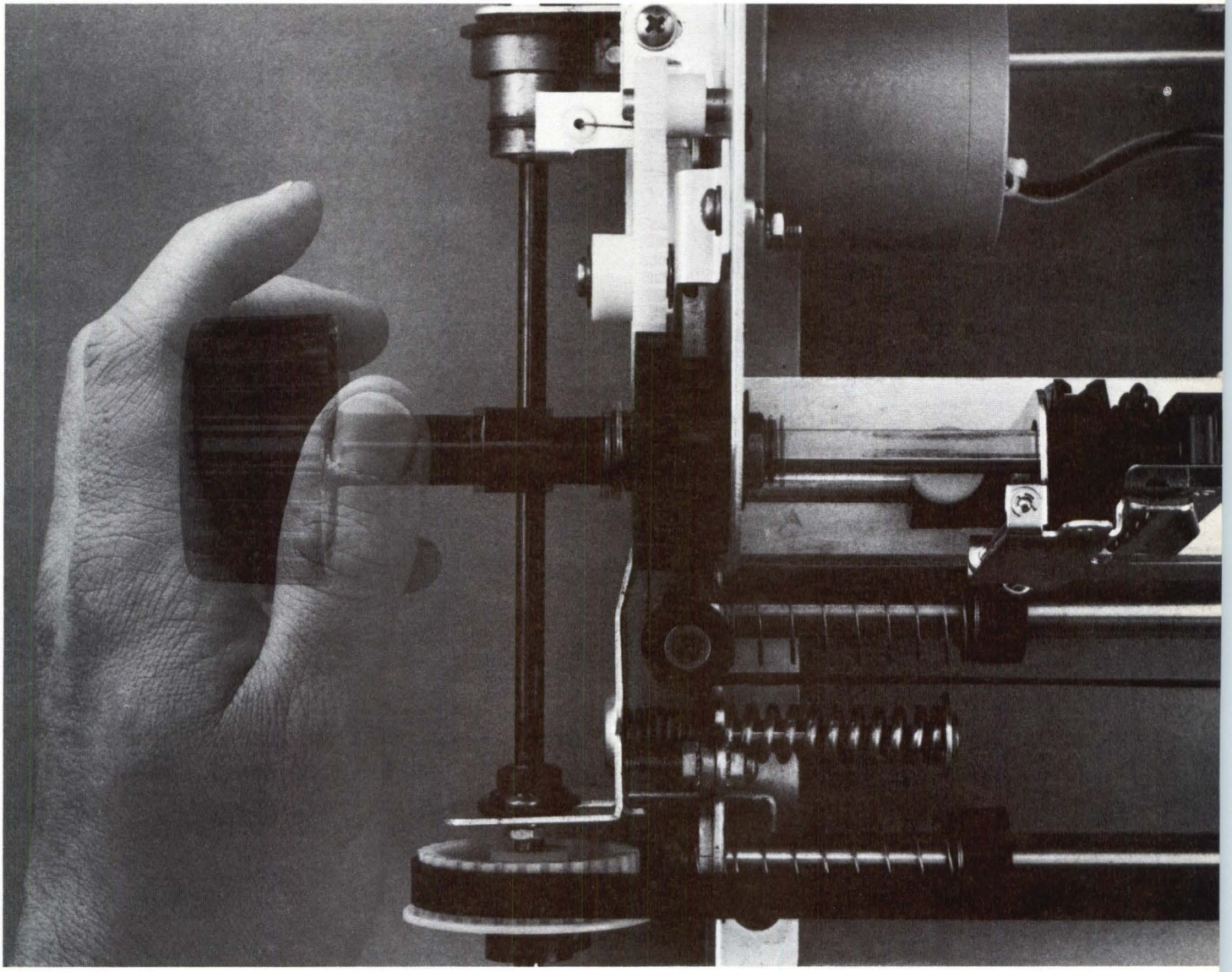
Several design refinements make it easier to read the printout while it is being produced. The ribbon is positioned back from the paper, and the cabinet top is beveled for easy viewing of the current line.

DECprinter offers several convenience features, all available separately. One is a paper stacker/ holder that mounts at the rear; another is a caster attachment for the pedestal for moving DECprinter easily.

A spring-loaded pressure plate on each tractor holds the paper in engagement with three driving pins.



Pushing in the platen knob the distance shown in this dual-exposure disengages the drive clutch, enabling the operator to locate the printing within the vertical spacing of preformatted paper. Moving the left tractor enables the operator to position characters in precise horizontal alignment on preprinted forms.



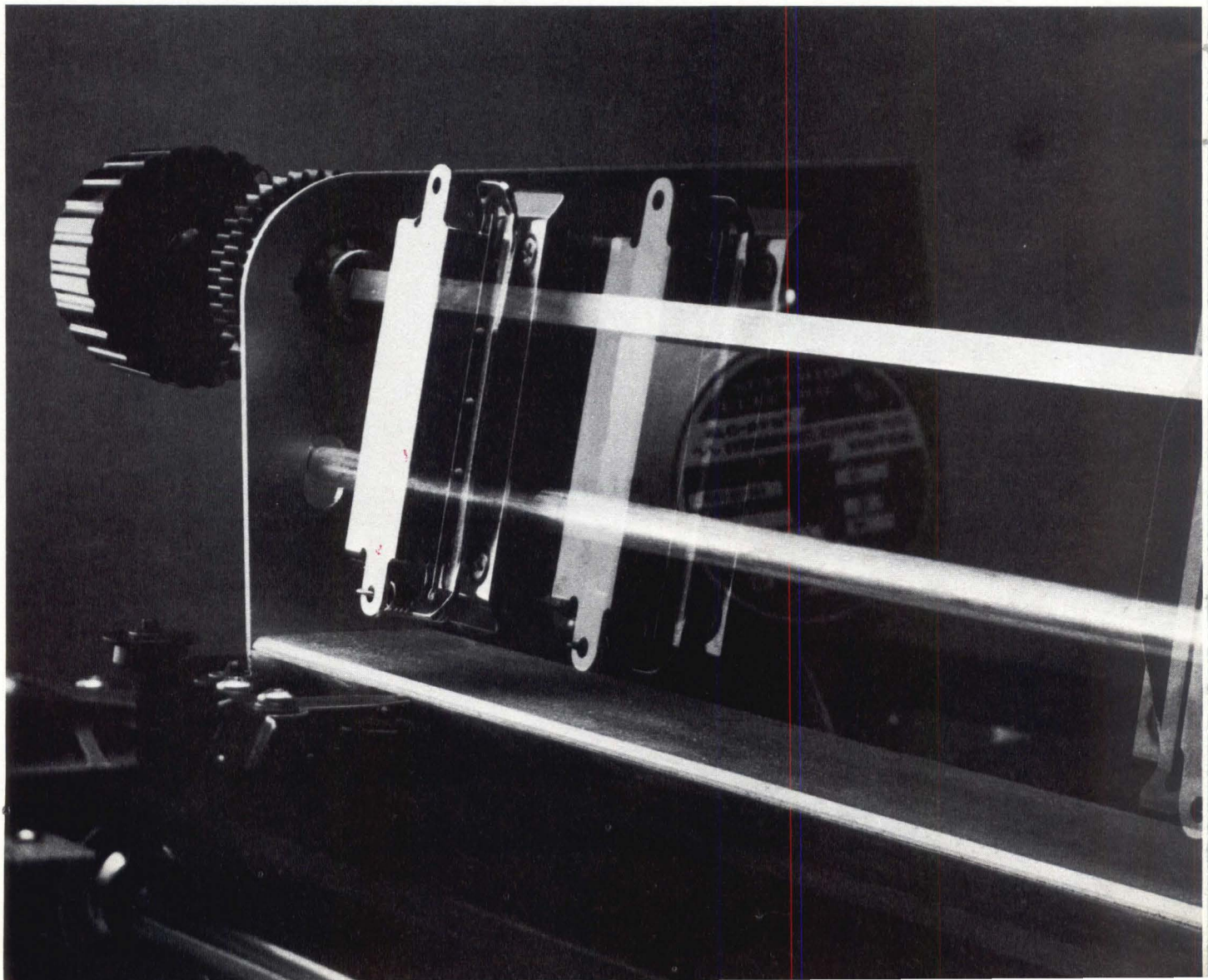
# Carriage design reflects sophisticated simplicity.

A combination of design features ensures precise dot placement and long service life by the carriage subsystem.

Carriage motion is controlled by a dc servo mechanism consisting of a dual-channel encoder and a dc motor. The head is positioned exactly for printing each dot in the character cell, and rough, jerking motion is eliminated. Noise, vibrations, and wear are minimized. A circuit in the servo system protects the carriage system against jam.

A manual print gap adjustment allows the user to vary the gap to accommodate single-part or multipart forms, with a total thickness of up to 0.020 of an inch.

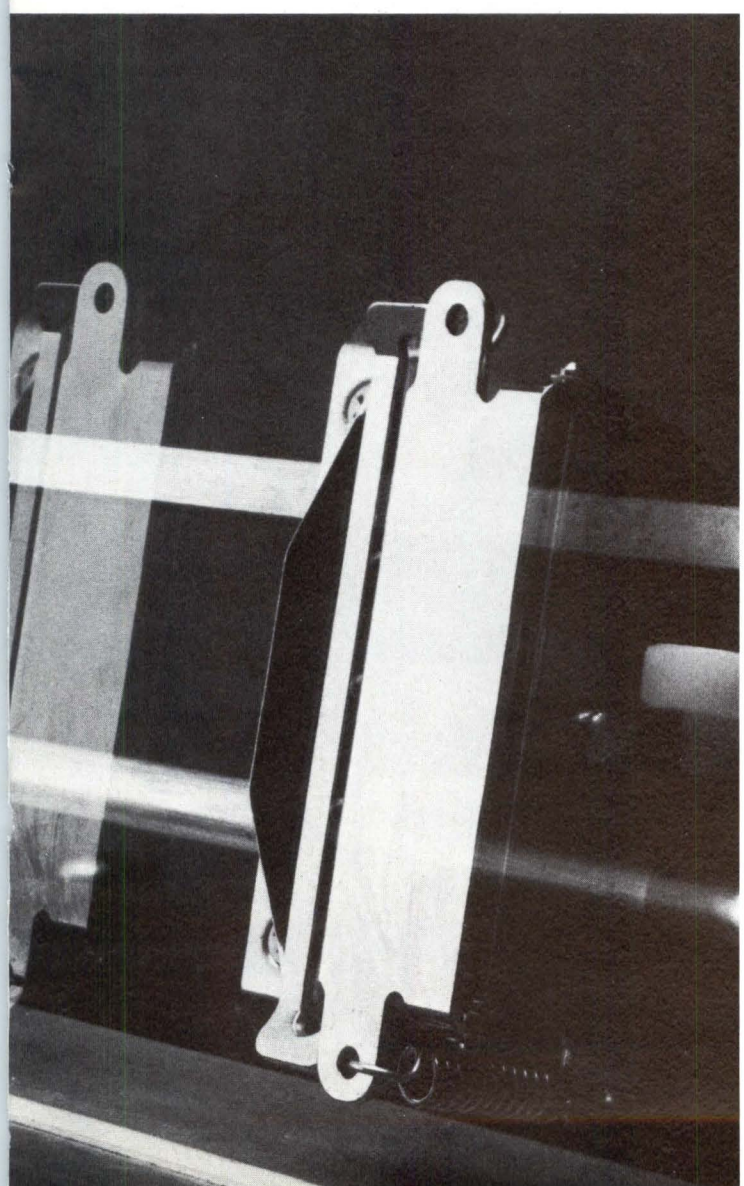
Carriage motion drives the ribbon feed mechanism, eliminating character smudging as well as eliminating separate drive and control elements.



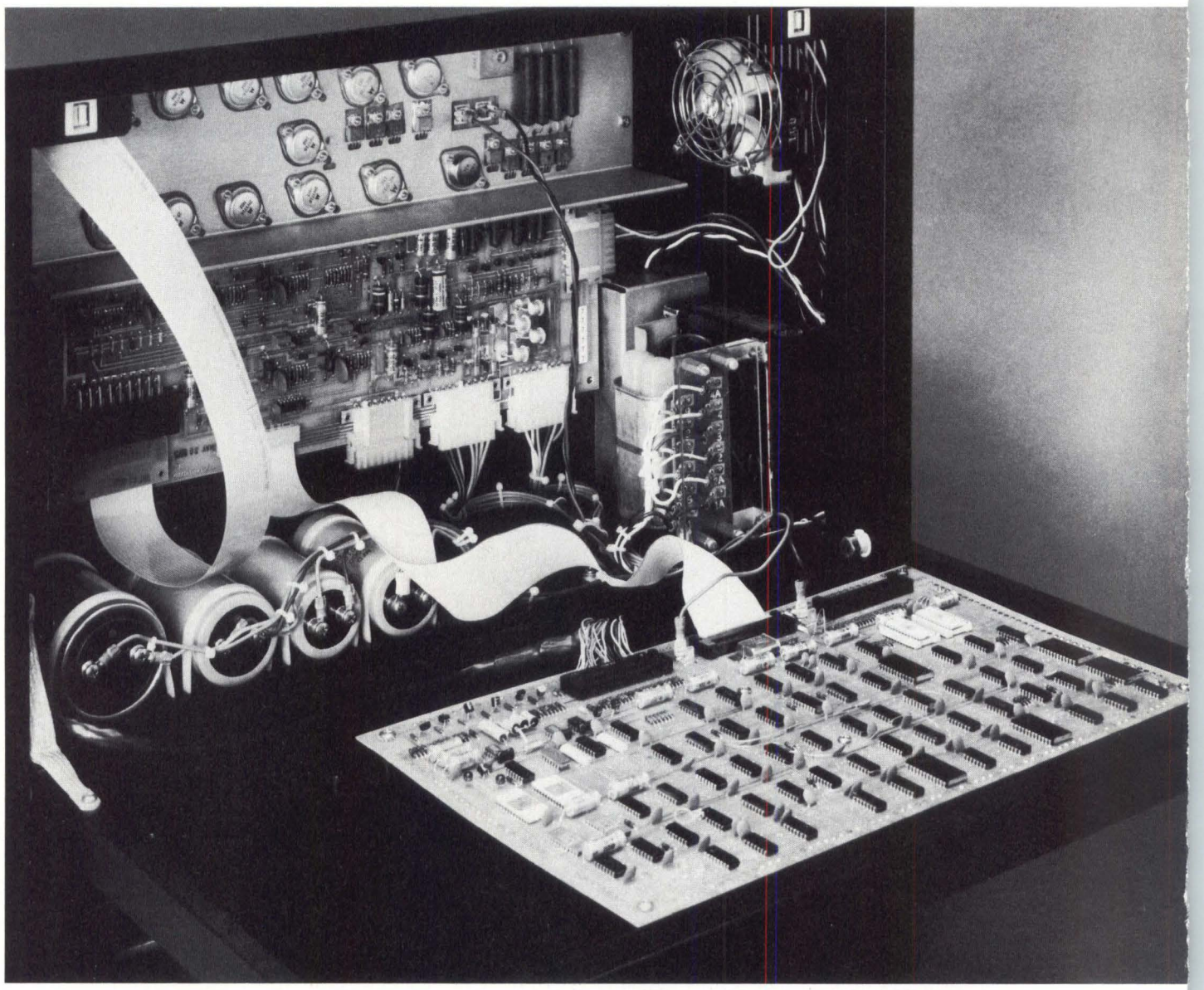
# DECprinter feeds paper positively, precisely, and quietly.

A stepping motor drives the dual-tractor, pin-feed paper advance mechanism. Paper always initializes on an integral line and feeds quietly but positively under equal and consistent tension. Working from a flat feeding surface, with six tractor pins constantly engaged, the mechanism advances multiple-part forms without slippage or misregistration.

Both tractors can be moved along the support bars, as this double exposure indicates. The right tractor is moved to accommodate different paper widths ranging from 3 to 14-7/8 inches. The left tractor is moved to position preprinted forms in precise horizontal alignment with print areas.



The rear door gives access to all electronic components. All logic functions are mounted on the door, analog and power circuitry, driver circuits, and controls on the inner board. Some large power components are mounted directly on the cabinet.

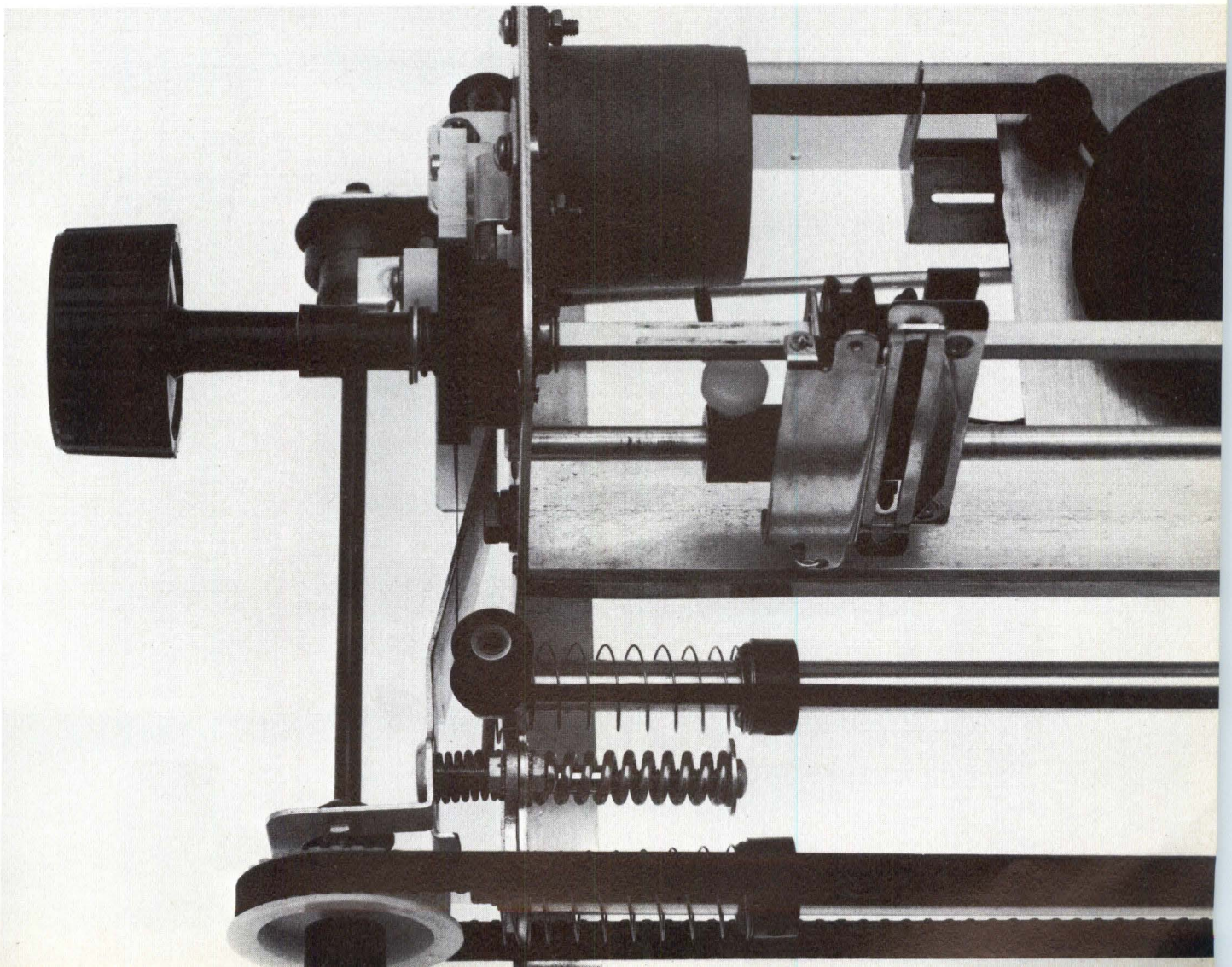


# High-uptime results from accessibility and maintainability.

By removing four screws you can remove the entire mechanical assembly or the print head. All logic control functions are concentrated on a single printed circuit board, mounted on the cabinet rear door. Analog and power circuitry, drive circuits, and controls are mounted on another easily accessible board. Some large power components mount on the cabinet.

Voltage taps on the power supply simplify and speed conversion from 115- to 230-volt operation.

The stepping motor advances paper by driving a pair of pin-feed tractors, each engaging three teeth. Pushing in the platen knob allows the operator to disengage the drive clutch, initializing the printing in the proper vertical position of preformatted paper.

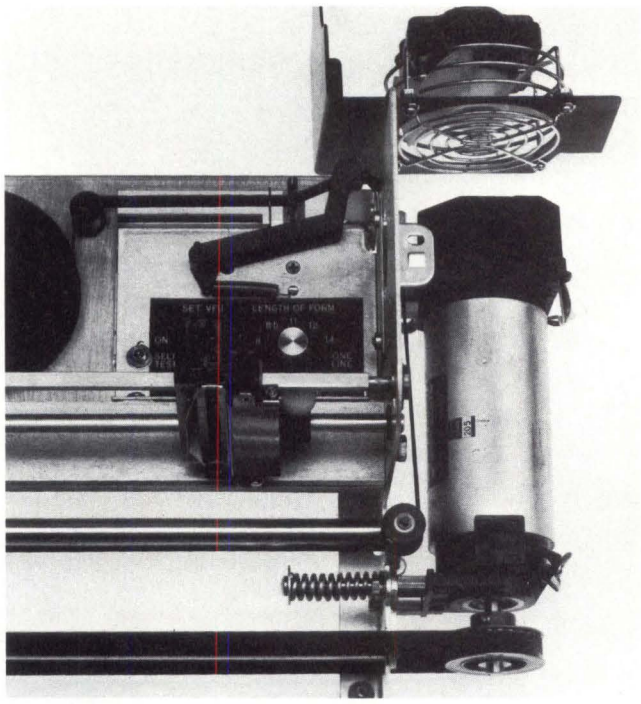


# Reliability proven in the field.

The DECprinter head is rated at 100,000,000 characters. It is designed to be the most reliable in the printer industry.

# Parity.

DECprinter is shipped with no parity. The user can select even parity or odd parity, with parity error printout, by changing jumpers.



A dc servo motor, driven by a dual-channel encoder, uses a belt to position the print head horizontally along the carriage. Loosening the locking knob at the upper center allows the operator to slide the right tractor along its support bars to accommodate a wide range of paper sizes.

# Reference data

How DECprinter operates
- Character set
- Printing
- Character operation
- Bell
- Line interface
- Control logic
- Microprogram control
- Program description
- Character ROM
- Ribbon drive
- Carriage drive
- Printing
- Carriage return
- Power supply
- ASCII code assignments
- DECprinter specifications

Digital's Components Group
Service and warranty
How to order DECprinter

DECprinter

# How DECprinter operates.

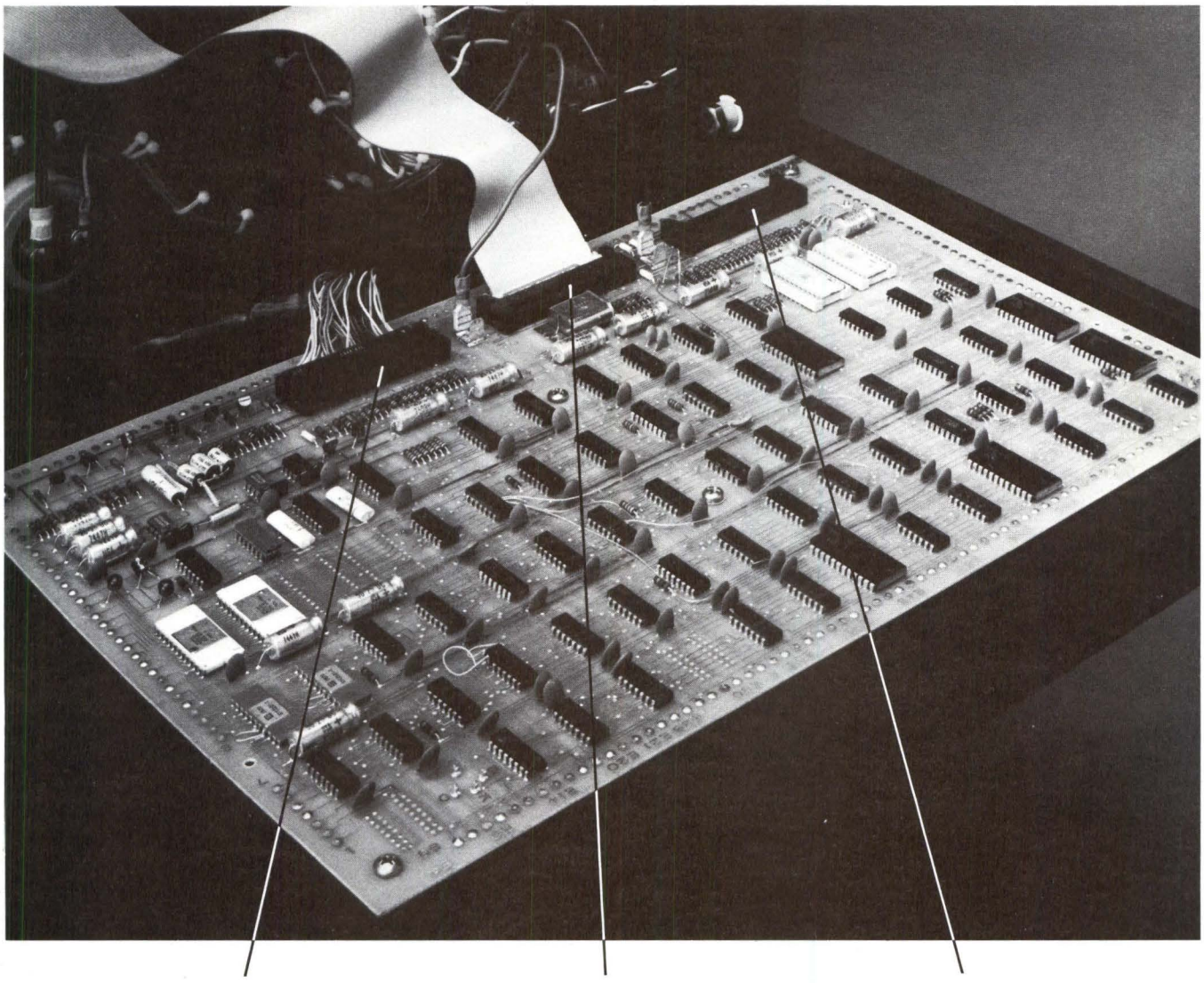
**Character set and code**
The full, 96-character, upper and lower-case set is standard with the LA180. Data is interpreted in a read-only memory (ROM). Changing the ROM enables the user to print nonstandard characters. The standard ASCII set, shown in Table 1, consists of 10 numerics, 26 upper-case alphas, 26 lower-case alphas, and 34 special characters, including DELETE, a nonprinting, nonspacing control code. The total character and control code count is 128.

**Printing**
The LA180 character cell is a seven-by-seven dot matrix measuring 0.18 cm wide (0.07 in.) by 0.25 cm high (0.10 in.) Horizontal spacing is ten characters per inch. Vertical spacing is six lines per inch. Maximum printable line length is 132 characters.

**Character operation**
DECprinter is a 180-character-per-second printer.

**Bell (BEL)**
Receipt of 007 (BEL) causes an audible tone to be sounded. A separate tone is sounded from each of up to eight BEL codes in succession.

**DECprinter Logic Board Connections.**

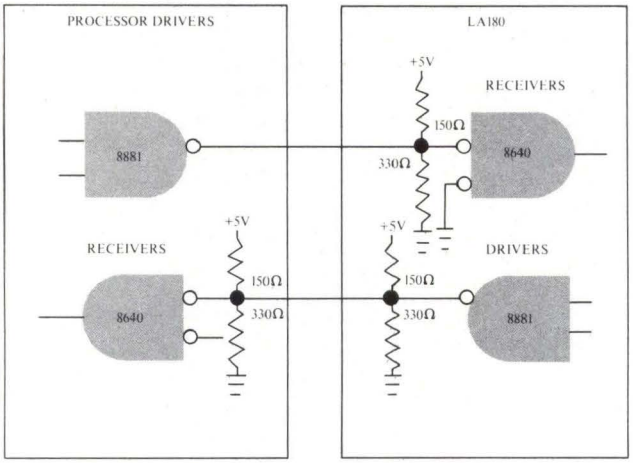


# Line interface.

**Cable**
BC11-S connects to a 40-pin Berg connector on the LA180 logic module. (See the Logic Board Connection photograph.) The cable can be any length up to 100 feet.

**Line interface**
The accompanying diagram identifies the drivers and receivers that are recommended for maximum noise rejection.

**LA180 Interface Diagram**




**Interface connector**
The accompanying table identifies the pin assignments for the 40-pin Berg connector (Digital Equipment Corp. Number 1209941-00) supplied with the LA180.

**Interface Connector Pin Assignments**

| Pin No. | Signal |
|---|---|
| A | Data Strobe |
| M | Data 1 |
| K | Data 2 |
| U | Data 3 |
| P | Data 4 |
| C | Data 5 |
| E | Data 6 |
| S | Data 7 |
| SS | Parity* |
| Y | Demand |
| PP | Busy* |
| EE | Paper Fault |
| HH | On Line |
| MM | +12 Vdc* |
| LL | 1200 baud*<br>DC ground<br>Chassis Ground |
| KK | +5 Vdc* |
| B | Data Strobe Ret |
| N | Data 1 Ret |
| L | Data 2 Ret |
| V | Data 3 Ret |
| R | Data 4 Ret |
| D | Data 5 Ret |
| F | Data 6 Ret |
| T | Data 7 Ret |
| TT | Parity Ret |
| Z | Demand Ret |
| RR | Busy Ret |
| FF | Paper Fault Return |
| JJ | On Line Ret |
| W | +5 Vdc* |
| UU | -12 Vdc* |

*Optional signal at interface (jumper must be added)

# The LA180 is microprogrammed, not hardware-controlled.

**Microprogram control**

Functions once performed by printers under hardware control are handled in the LA180 under the control of a 512-instruction microprogram. These instructions are divided into routines, each dedicated to a specific machine function. Microprogram control (MPC) initiates a machine function, senses the performance of the function, and, based on that performance, determines which routine is to be performed next.

The simplified block diagram shows the primary data and program paths and identifies the functions performed by the microprogram.

Because the LA180 allows the user to monitor machine functions and operator controls, he can design his software to modify specific routines and to change the printer's responses as desired to meet changing operational requirements.

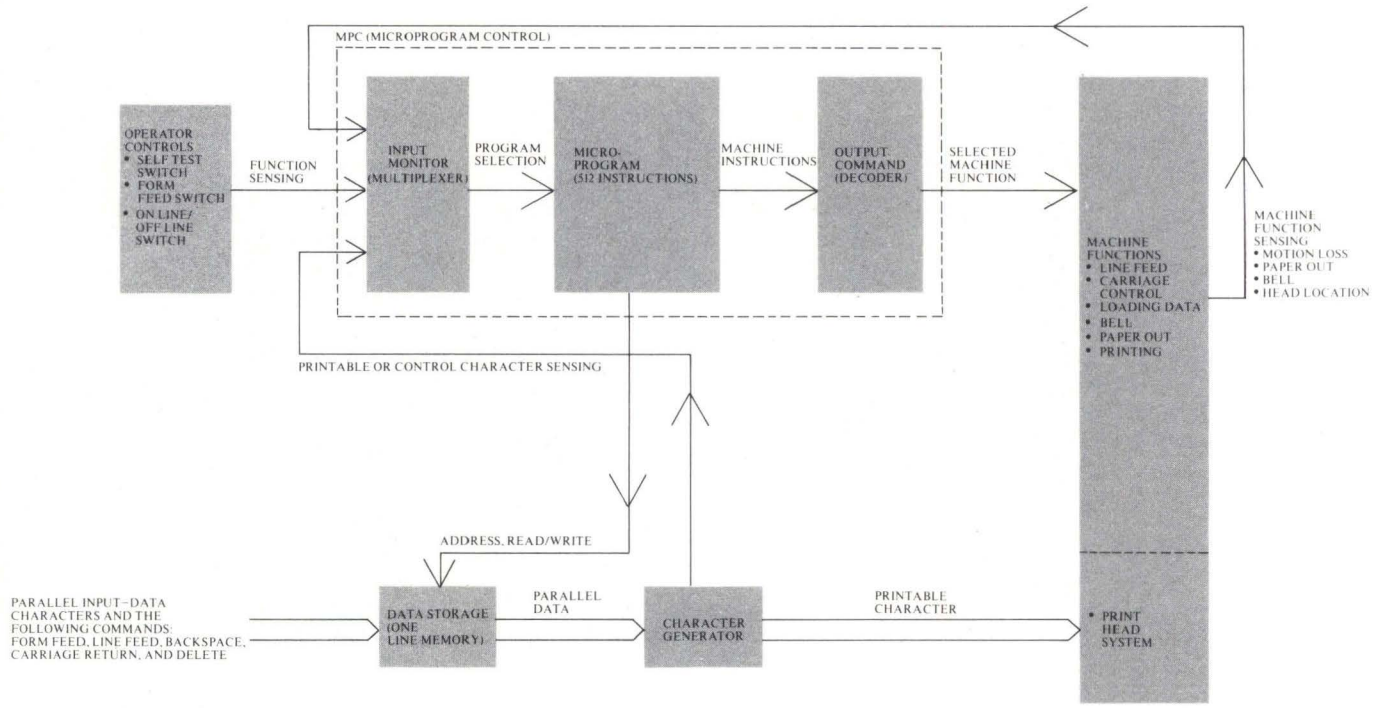
**Control logic**

Eight-bit characters reach the LA180 from the user's interface and are processed through the single-character buffer under MPC, loading the character-buffer RAM with a line of data. From the RAM, characters are presented on a FIFO basis to the character-generator ROM, which generates the firing matrix through which the print head forms the printable characters. The ROM also contains decoding information for the nonprintable command characters.

The carriage servo and print head subsystems are activated under MPC to move the print head through the character cell and print the commanded dots in each of the seven rows.

A CR (carriage return) character causes the MPC to move the print head to the left margin. A BS (back space) character causes the MPC to move the print head one column to the left. An LF (line feed) character causes the MPC to activate the stepper motor drive and advance the paper one line. An FF (form feed) character advances the paper to the top of the next form.

## Simplified Block Diagram



The structure of the MPC is shown in the control logic block diagram. Each of the 512 instructions in the control ROM consists of an eight-bit word. The upper four bits define the general class of instruction. the lower four bits, the specific operation to be performed.

Selection of an instruction is performed by the program address register, which generally acts as a counter, causing instructions to be executed sequentially at the rate of one every 1.182 microseconds.

The sequential instruction clock can be interrupted by jump and skip instructions when the user desires to modify the normal order of instruction execution.

The **JUMP1** instruction causes the address control logic to be activated to load the lower four bits of the instruction (on the ROM data bus) into the lower four bits of the program address register. Any transfer of control which does not change the upper five bits of the address can use this instruction. JUMP1 is thus limited to jumps within one of the 32 16-word pages of the microprogram.

**JUMP2** produces the same effect as JUMP1, but with the added effect that the 4-bit register data bus is used to load the next four bits of the program address register. Thus, the combination of an instruction that loads the register (described below) and a JUMP2 instruction can effect a transfer within one of the two 256-word halves of memory.

**JUMP3** produces the same effect as JUMP2, but with the added effect that the most significant bit of the address register is toggled. This causes the jump to be to the opposite half of memory from the instruction being executed.

**JUMP4** causes a jump from one to the next of the 32 16-bit pages of the micro-program.

CLR resets the contents of the program address register to zero. The program address register is reset to zero on power-up.

**SKIP1** and **SKIP2** are conditional skip instructions. The conditions are the inputs to multiplexers 1 and 2. The lower four bits of the skip instruction specify which of 16 inputs to sample. If the selected input is asserted when the skip instruction occurs, then the address control logic causes the address to increment by two rather than by one during a single instruction cycle. Input signals to the skip multiplexers are data available, servo control data (CARRY, BORROW, INC), bits 1, 2, 3, and 4 of register (REG), control character indications (CR, FF, LF, BS, and BEL), the printable-character indication, the REG-0 indication, and a clock.

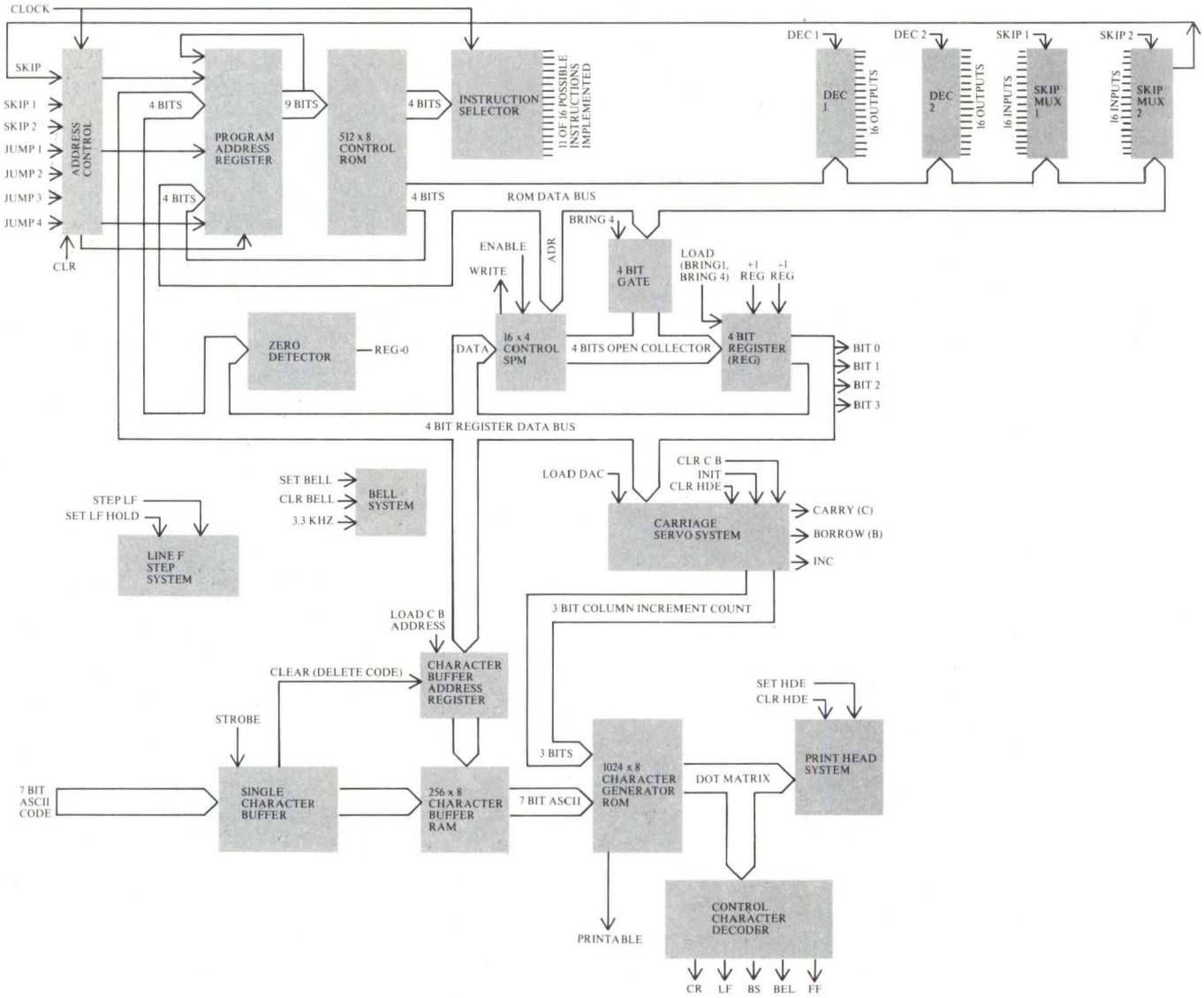
Instructions which do not modify the normal sequential flow are BRING1, BRING4, DEC1, DEC2, and STORE1.

**BRING1** is used to bring data from one of 16 4-bit memory locations in the control RAM to the 4-bit register REG. The lower 4 bits of the instruction select the memory location.

**BRING4** loads the lower 4 bits of the instruction in the 4-bit register REG.

**DEC1** and **DEC2** enable the MPC to transmit commands to the systems it is controlling. The lower 4 bits of the instruction specify which of 16 outputs of the decoder will be pulsed.

## Control Logic Block Diagram



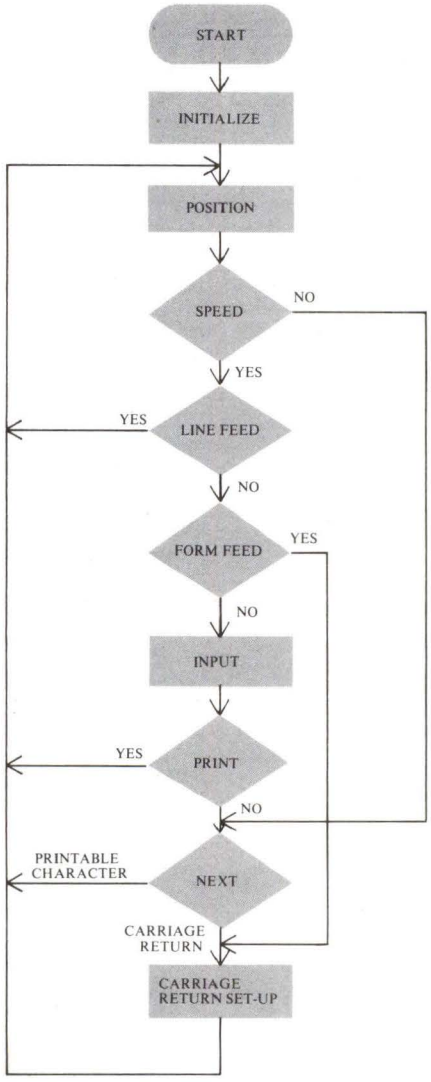
# Program description.

The microprogram consists of several instruction sequences connected by major decision nodes as shown in the flow diagram.

The first sequence is the initialize routine. This routine initializes all the scratch pad locations and moves the print head to the left margin.

The next sequence is the position routine. Requests for print head position changes (such as for print or carriage return) are processed. All position information is in units of character cells and is stored in locations of the control ROM. In addition, indications of print head position change are processed (CARRY is a one-column advance; BORROW, a one-column reverse).

## Microprogram Flow Diagram




Speeds are 18 inches per second for normal printing, -65 inches per second for carriage return, slower negative speeds for carriage return slow-down, and 0 inches per second for idle.

The input routine increments the line buffer address register by one count for each character received and stores the character in the line buffer. It resets the buffer address register upon receiving an LF, FF, or CR character.

The bell routine activates the bell subsystem and times the duration of the audible tone bursts.

The print routine requests print head motion and activates the print head solenoids to form the dot matrix characters.

The line feed routine times the four steps and the settling time for the line feed stepper system.

The character-processing routine is the mate to the input routine. It processes characters as they come from the line buffer and sets up conditions in the control ram for executing them.

If a character is printable, the print routine is activated.

If the character is carriage return, then the desired print head position change is entered in the control RAM. The position and speed routines complete the execution of carriage return. Backspace is processed in a similar manner.

If the character is line feed, then the line feed step timing sequence is initiated.

If a bell character is received, the bell sounding routine is notified.

Other characters cause no action.

# Character ROM features.

**Character ROM**
The character generator ROM converts the seven-bit 7-bit ASCII character code to the 7 x 7 dot matrix pattern.

The 7-bit character code (inverted) forms the most significant seven bits of the ROM address. The 3-bit column increment count forms the least significant three bits of the 10-bit ROM address.

Seven of the eight outputs of the ROM select the seven solenoids in the print head. The eighth output provides the printable/nonprintable indication for the microprogram.

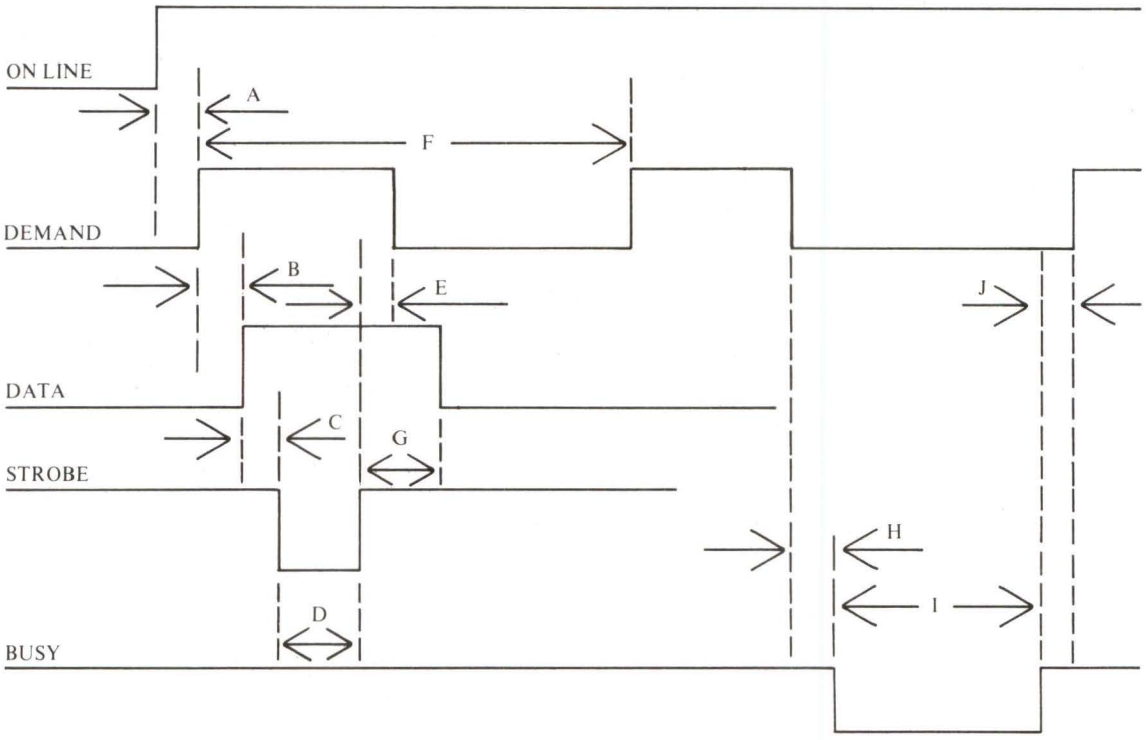
For each nonprintable character, a unique pattern is coded in the printing cell which provides for economical decoding of the printer control characters for the microprogram.

**Ribbon drive**
Power to move the ribbon is taken from the carriage drive motor through a one-way clutch and a reversing mechanism. The clockwise motion during printing is used to drive the ribbon. No ribbon motion occurs during carriage return. The drive is connected to one spool at a time. As one spool empties, a rivet near the end of the ribbon pushes a lever into the path of a shift tab which flips the driving ratchet from the driving reel to the follower. Spring-loaded disk brakes maintain a drag of three ounces on the follower.

**Carriage drive**
The carriage is driven by a dc servo mechanism containing a power amlifier, a conventional permanent-magnet dc motor, and a timing belt. An optical incremental encoder determines carriage position by detecting motor shaft movement, generating one pulse for each 0.01 inch of carriage travel. A one-decade up-down BCD counter records carriage position within a character cell. The overflow of this counter is captured by the ROM processor to determine carriage position and for other functions.

Motor speed during printing and carriage return is controlled by the ROM processor through a register which controls the output of the power amplifier feeding the drive motor.

## Timing in the LA180




A = 0 SEC MIN, 1 SEC MAX
B = 0 SEC MIN
C = 50 N SEC MIN
D = 100 N SEC MIN
E = 50 N SEC MAX
F = 8.26 U SEC MIN
G = 100 N SEC MIN
H = 100 U SEC MAX
I = 60 M SEC MIN, 700 M SEC MAX
J = 1.2 U SEC

**Printing**
Printing is performed by moving the print head from left to right across the character cell, sensing dot position columns with the BCD counter, and energizing the solenoids selected by the character generator ROM outputs.

If the carriage is to the right of the character starting position, the carriage is moved to the left of the starting dot column before printing starts. When the complete line is printed, the carriage returns to the left margin and halts. Printing starts only upon receipt of a line terminator (CR, LF, FF).

**Carriage return**
A carriage return command causes the carriage to return to the left margin. Its speed in return depends on its distance from the margin. Maximum time for return is 275 msec. Minimum time is 100 msec.

**Power supply**
The basic power supply provides nominal output voltages of +21, -21, and +10 dc.

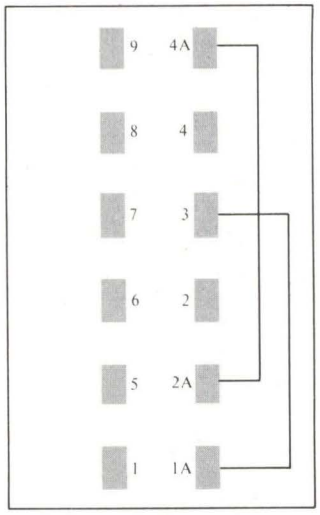
The 5-volt supply for the logic is derived from a linear regulator. Regulation is 5 percent, with ripple of 200 mv P-P.

Regulation of the ±12-volt supply is also 5 percent.

Special voltage levels for MOS circuitry are controlled on the logic boards.

The power transformer is normally configured for 115 Vac operation, with jumpers in the positions shown in the accompanying diagram. For 240 Vac operation, remove the two jumpers and replace them with one from 2A to 3.

**Transformer Strapping**




The power transformer, filter capacitors, and the other large parts are mounted individually on the base of the electronics compartment. The input line cord enters the printer electronics compartment in a metal enclosure in which a line filter is mounted. The off-on switch is located at the right front of the cabinet. Low-voltage, high-energy terminals are protected against accidental shorts.

Fifty and sixty Hz models have different power transformers.

The following table lists the 7-bit ASCII codes and the response of the LA180 to each code.

| ASC II Code | Character | Character Print | Action/Description |
|---|---|---|---|
| 000 | NUL | None | None |
| 001 | SOH | None | None |
| 002 | STX | None | None |
| 003 | ETX | None | None |
| 004 | EOT | None | None |
| 005 | ENQ | None | None |
| 006 | ACK | None | None |
| 007 | BEL | None | Sound Alarm Bell |
| 010 | BS | None | Backspace one position |
| 011 | HT | None | None |
| 012 | LF | None | Print contents of line buffer, return print head to left margin, advance paper one line. |
| 013 | VT | None | None |
| 014 | FF | None | Print contents of line buffer, return print head to left margin, advance paper one line. |
| 015 | CR | None | Move print head to left margin |
| 016 | SO | None | None |
| 017 | SI | None | None |
| 020 | DLE | None | None |
| 021 | DC1 | None | None |
| 022 | DC2 | None | None |
| 023 | DC3 | None | None |
| 024 | DC4 | None | None |
| 025 | NAK | None | None |
| 026 | SYN | None | None |
| 027 | ETB | None | None |
| 030 | CAN | None | None |
| 031 | EM | None | None |
| 032 | SUB | None | None |
| 033 | ESC | None | None |
| 034 | FS | None | None |
| 035 | GS | None | None |
| 036 | RS | None | None |
| 037 | US | None | None |
| 040 | SP | Blank Space | Receive character and store in memory. |
| 041 | ! | ! | Receive character and store in memory. |
| 042 | " | " | Receive character and store in memory. |
| 043 | # | # | Receive character and store in memory. |
| 044 | $ | $ | Receive character and store in memory. |
| 045 | % | % | Receive character and store in memory. |
| 046 | & | & | Receive character and store in memory. |
| 047 | ' | ' | Receive character and store in memory. |
| 050 | ( | ( | Receive character and store in memory. |
| 051 | ) | ) | Receive character and store in memory. |
| 052 | * | * | Receive character and store in memory. |
| 053 | + | + | Receive character and store in memory. |
| 054 | , | , | Receive character and store in memory. |

| ASC II Code | Character | Character Printed | Action/Description |
|---|---|---|---|
| 055 | - | - | Receive character and store in memory. |
| 056 | . | . | Receive character and store in memory. |
| 057 | / | / | Receive character and store in memory. |
| 060 | 0 | 0 | Receive character and store in memory. |
| 061 | 1 | 1 | Receive character and store in memory. |
| 062 | 2 | 2 | Receive character and store in memory. |
| 063 | 3 | 3 | Receive character and store in memory. |
| 064 | 4 | 4 | Receive character and store in memory. |
| 065 | 5 | 5 | Receive character and store in memory. |
| 066 | 6 | 6 | Receive character and store in memory. |
| 067 | 7 | 7 | Receive character and store in memory. |
| 070 | 8 | 8 | Receive character and store in memory. |
| 071 | 9 | 9 | Receive character and store in memory. |
| 072 | : | : | Receive character and store in memory. |
| 073 | ; | ; | Receive character and store in memory. |
| 074 | < | < | Receive character and store in memory. |
| 075 | = | = | Receive character and store in memory. |
| 076 | > | > | Receive character and store in memory. |
| 077 | ? | ? | Receive character and store in memory. |
| 100 | @ | @ | Receive character and store in memory. |
| 101 | A | A | Receive character and store in memory. |
| 102 | B | B | Receive character and store in memory. |
| 103 | C | C | Receive character and store in memory. |
| 104 | D | D | Receive character and store in memory. |
| 105 | E | E | Receive character and store in memory. |
| 106 | F | F | Receive character and store in memory. |
| 107 | G | G | Receive character and store in memory. |
| 110 | H | H | Receive character and store in memory. |
| 111 | I | I | Receive character and store in memory. |
| 112 | J | J | Receive character and store in memory. |
| 113 | K | K | Receive character and store in memory. |

| ASC II Code | Character | Character Printed | Action/Description |
|---|---|---|---|
| 114 | L | L | Receive character and store in memory. |
| 115 | M | M | Receive character and store in memory. |
| 116 | N | N | Receive character and store in memory. |
| 117 | O | O | Receive character and store in memory. |
| 120 | P | P | Receive character and store in memory. |
| 121 | Q | Q | Receive character and store in memory. |
| 122 | R | R | Receive character and store in memory. |
| 123 | S | S | Receive character and store in memory. |
| 124 | T | T | Receive character and store in memory. |
| 125 | U | U | Receive character and store in memory. |
| 126 | V | V | Receive character and store in memory. |
| 127 | W | W | Receive character and store in memory. |
| 130 | X | X | Receive character and store in memory. |
| 131 | Y | Y | Receive character and store in memory. |
| 132 | Z | Z | Receive character and store in memory. |
| 133 | [ | [ | Receive character and store in memory. |
| 134 | \ | \ | Receive character and store in memory. |
| 135 | ] | ] | Receive character and store in memory. |
| 136 | ^ | ^ | Receive character and store in memory. |
| 137 | – | – | Receive character and store in memory. |
| 140 | ' | ' | Receive character and store in memory. |
| 141 | a | a | Receive character and store in memory. |
| 142 | b | b | Receive character and store in memory. |

| ASC II Code | Character | Character Printed | Action/Description |
|---|---|---|---|
| 143 | c | c | Receive character and store in memory. |
| 144 | d | d | Receive character and store in memory. |
| 145 | e | e | Receive character and store in memory. |
| 146 | f | f | Receive character and store in memory. |
| 147 | g | g | Receive character and store in memory. |
| 150 | h | h | Receive character and store in memory. |
| 151 | i | i | Receive character and store in memory. |
| 152 | j | j | Receive character and store in memory. |
| 153 | k | k | Receive character and store in memory. |
| 154 | l | l | Receive character and store in memory. |
| 155 | m | m | Receive character and store in memory. |
| 156 | n | n | Receive character and store in memory. |
| 157 | o | o | Receive character and store in memory. |
| 160 | p | p | Receive character and store in memory. |
| 161 | q | q | Receive character and store in memory. |
| 162 | r | r | Receive character and store in memory. |
| 163 | s | s | Receive character and store in memory. |
| 164 | t | t | Receive character and store in memory. |
| 165 | u | u | Receive character and store in memory. |
| 166 | v | v | Receive character and store in memory. |
| 167 | w | w | Receive character and store in memory. |
| 170 | x | x | Receive character and store in memory. |
| 171 | y | y | Receive character and store in memory. |
| 172 | z | z | Receive character and store in memory. |
| 173 | { | { | Receive character and store in memory. |
| 174 | ¦ | ¦ | Receive character and store in memory. |
| 175 | } | } | Receive character and store in memory. |
| 176 | ~ | ~ | Receive character and store in memory. |
| 177 | DEL | None | Clear buffer. |

# DECprinter specifications.

| Specification | Standard |
|---|---|
| Printing | Speed: 180 char/sec<br>Columns: 132<br>Characters: 96 ASCII printing set; 32 ASCII control set<br>Character Size: 0.175 x 0.25 cm (0.70 x 0.10 in)<br>Horizontal Spacing: 10 char/in<br>Vertical Spacing: 6 lines/in<br>Character Formation: impacting wires, 7 x 7 dot matrix<br>Carriage Return: 275 msec max, 100 msec min<br>Line Feed: 32 msec<br>Slew Speed: 7.5 in/sec (45 lines/sec) |
| Paper Handling | Tractor feed, both tractors engaging four pins; movable right tractor for 3 to 14-7/8-in forms; movable left tractor for precise horizontal placement of pre-printed forms; paper advance mechanism disengages for precise vertical placement of pre-printed forms; print gap adjustment for 1 to 6-part forms; top-of-form with 11 form lengths |
| Paper | Single-part form: 15-pound min; card stock, 0.010-in max<br>Multipart form: 2 to 6 parts, 0.020-in max (card stock can be used for only last part)<br>Note: NCR or 3M paper, must use ribbon on original.<br>First-surface impact paper not recommended.<br>Continuous-feed, fan-fold business forms with 3- or 4-prong margin crimps on both margins (multi-part). Stapled forms not recommended, since they may damage tractors. Line-glued margin on one side acceptable, not acceptable on both margins. Dot-glued acceptable on both margins. |
| Modes of Operation | On-line, off-line, self-test ripple test pattern. |
| Parity | Odd, even, or none. |
| Interface | 8-bit parallel, bit asynchronous. |
| Power | 90–264 Vac (selectable):<br>50 or 60 Hz ± 1 Hz<br>400 W printing max peak<br>100 W nonprinting |
| Mechanical | Mounting: free-standing pedestal unit<br>Size: 32.2 in (84.3 cm) H x 27.5 in. (69.8 cm) W x 21.0 in (50.8 cm) D<br>Weight: 102 lb (224.4 kg) approx |
| Environment | Temperature: 10° to 40° C (50° to 104° F) operating<br>–40° to 66° C (–40° to 151° F) nonoperating<br>Humidity: 10 to 90%, noncondensing, operating<br>5% to 95%, noncondensing, nonoperating<br>28° C max wet bulb |
| Ribbon | Digital-specified nylon fabric, spool assembly 0.5 in (1.27 cm) W x 60 yards (54.68 m) L |

| Option | |
|---|---|
| LAXX-LJ | Compressed font (kit of five) |
| LAXX-NW | RS232C serial line interface with 256-character buffer |
| LAXX-MW | Kit of five RS232C interfaces |
| LAXX-NX | 20mA interface |
| LAXX-MX | Kit of five 20 mA interfaces |
| LAXX-NY | RS232C serial line interface with EBCDIC-to-ASCII converter |
| LAXX-MY | Kit of five |
| **Accessory, Supply** | |
| LAXX-KB | Casters |
| LAXX-KD | Deep wire basket |
| 3612153-01 | Ribbons (dozen) |
| LAXXK-S1 | Extended supply kit |
| LAXXK-S2 | Basic supply kit |

# Digital's Components Group. Unbundling the most popular minicomputers.

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Now, if you buy through this group, you can get these components completely unbundled. Volume buying will earn you steep discounts and enable us to deliver your orders off the shelf. Our entire manufacturing capability–more than two million square feet–stands behind this commitment to deliver.

# Service and Warranty

You get a simple, straightforward warranty: DEC-printer is warranted for 90 days. Return any defective subassembly to us during this period and we will repair or replace it without charge.

Post-warranty service can be provided in a variety of ways: a traditional priority service contract with various coverage hours, an on-site per-call service on a time and materials basis, and depot maintenance.

Depots are located at the Canadian Regional Office in Kanata, the Chicago Regional Office in Rolling Meadows, the Northeast Region in Maynard, the Western Regional Office in Sunnyvale, and major European cities.

Service training is available at DIGITAL.

# How to order DECprinter

Call DIGITAL's Components Group free for a full discussion of your application. The hot line number to reach an LA180 specialist is 800-225-9480 toll-free from 8:30 a.m. to 5 p.m. Eastern time in the United States. Massachusetts residents should dial (617) 481-7400. Or use the accompanying reply card and we will call you after analyzing your application and requirements.

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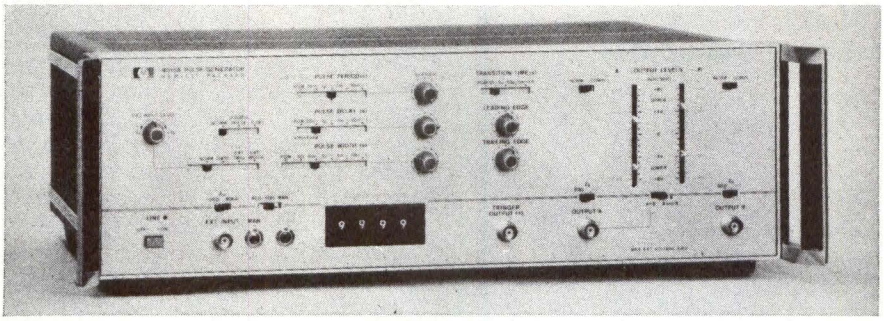
## Pulse Generator Options Speed Testing of MOS/CMOS Circuits



Hewlett-Packard's 8015A pulse generator is now available with power supply tracking, external amplifier access, extra TTL output, and remote control options to speed and simplify testing of MOS and CMOS circuitry

Enhancing the usefulness of the 8015A pulse generator in testing MOS/CMOS circuits, four options, introduced by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, provide an extra sensing level connection, make internal amplifiers externally accessible, provide an extra third output connection, and allow remote control of pulse parameter ranges. The options serve to protect the devices under test, allow TTL outputs to be amplified to CMOS levels, and permit testing of mixed TTL and CMOS circuits.

Option 006, a tracking function, assures that test pulses fed to MOS circuits will not exceed power supply voltage levels—thus destroying the device under test. This extra sensing connection, when tied to the power supply, permits the output level of the pulse generator to automatically track the power supply voltage.

By means of option 004, the two linear internal amplifiers of the 8015A are made externally accessible. Either channel will put out a signal up to 16 V peak-to-peak, operated asymmetrically; the two channels may be used separately. Rise time is 6 ns or better. External accessibility allows the output of experimental TTL circuits to be amplified to CMOS levels, as well as the mixing of external and internal signals to produce test signals consisting of noise spikes on sine waves.

Also useful when testing mixed TTL and CMOS circuits is an isolated, third output connection, option 005. In-phase with channel A, this connection puts out signals at fixed TTL level and is a precise 50-Ω resistive source (such a source has the advantage of absorbing reflections caused by external mismatches). While the level is fixed at ≥4.5 V into open circuit for logic 1, all other pulse parameters are variable in concurrence with channel A.

Option 003 provides remote control of pulse parameter range and of the pulse burst option (if included). Pulse parameter ranges may be remoted digitally by external contact closure to ground or by applying TTL-compatible signals (negative-true logic). Vernier control is available by combining external currents or voltages and resistances.

Circle 145 on Inquiry Card

## Minicomputer System Cuts Costs of Applications Programming

Designed to sharply reduce costs of developing transaction-oriented business accounting and inventory control systems, DASL (for Data Access System Language)™ is a multiterminal computer system which provides a powerful language for applications programming, operating system and data base management software, and a 16-bit minicomputer and full range of peripherals. Developed by Ball Computer Products, Inc, 5601 College Ave, Oakland, CA 94618, the system provides a set of more than 250 precoded routines in metacompiler format to handle common business and data management functions; these are combined to develop online business programs, saving up to 90% of the work ordinarily required.

Because routines are written in assembly language, resulting system throughput is several times greater than that of equivalent COBOL or BASIC systems. The ability to specify system parameters for each transaction type, along with the formalized system structure, provides the programmer with all the tools he needs to build a system that exactly matches the end-user's needs.

A minimum operating configuration for an online multiterminal operation includes 16-bit minicomputer with 64K bytes (32K words) of core memory, two CRT terminals operating in page mode with maximum screen size of 20 lines (80 char/line), disc drive providing storage for 5.8M bytes, magnetic tape drive, and control console with hardcopy printer. This basic system can be expanded in stages to a total of 16 CRT terminals and 400M bytes of disc storage; other options include high speed tape drives, printers, card readers, multiplexers, and controllers.

System software includes a file-oriented disc operating system for high level I/O management and system control and a real-time subsystem for multiprogramming of user applications in a multilevel priority interrupt environment. This permits data entry and inquiry to occur uninterrupted at terminals, concurrent with processing and high speed I/O. Different transactions may be processed concurrently at each terminal, or groups of terminals may handle the same task.

Among the system's features are online data entry, with detailed error messages; online data bases for instant access and immediate transaction posting; batch control of data entry, and multiple levels of operator and station security. Error checking keeps untested transactions from undermining system integrity.

Circle 146 on Inquiry Card

## Optical Page Reader Combines Low Price with Editing Capability

Context's model 103 optical page reader incorporates a correction/editing terminal which allows typewritten copy to be converted directly to corrected, edited typesetting tape, ready to run on a typesetting machine

Offering high throughput plus powerful correction and editing capabilities via an integral correction/editing terminal, the model 103 optical page reader converts typewritten copy directly to typesetter tape, eliminating the need for perforating keyboards, video terminals, or typesetting computers. It reads copy prepared on a standard IBM Selectric™ typewriter, equipped with a special typeball which imprints a human-readable character over a tiny machine-readable bar code, resulting in what is claimed, by Context Corp, 4 Ray Ave, Burlington, MA 01803, to be one of the lowest system costs obtainable.

The unit includes a 200-char memory, programmable via typed "header sheet," which permits the user to store repetitive phrases, typesetting format strings, or titles for insertion at any designated point in the text. A separate dedicated read-only memory stores typesetting codes and characters not normally found on a standard office typewriter. These are called by a 2-keystroke code.

Copy can be deleted or inserted on the typewritten page using a variety of keyboard or manual codes, permitting copy to be edited prior to scanning. After scanning, necessary editing is accomplished by means of a keyboard display module attached to the scanner. This module allows the operator to access the 1-page (4000-character) buffer memory, permitting insertion, deletion, or substitution of copy. It also allows automatic searching for any "can't read" character in the copy, and display of the character, in context, on a 32-character display for quick correction. Each page can be reviewed, or the machine can operate in a fully automatic mode, processing up to 50 pages in an unattended mode.

The unit is capable of providing 1000 words/min. to a punch, or 4000 words/min. to a computer. Accuracy is specified to be less than one error in 25,000 characters with controlled copy. The scanner tolerates typed skew of up to ±0.070" in line, and up to ±0.070" of vertical character misalignment.

Circle 147 on Inquiry Card


# ACOUSTIC COUPLER
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**FEATURES**
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## Electronic Typing System Communicates at Speeds to 120 Char/s

Combining high speed document creation with immediate electronic document transmission, the model 800 communicating electronic typing system sends information eight times faster than most competitive units and can communicate directly with computers as well as other word processing systems. Developed by the Office Products Div of Xerox Corp, 701 S Aviation Blvd, El Segundo, CA 90245, the system is claimed to offer a viable alternative to mail service, sending and receiving more than two pages of double-spaced text per minute.

Data are sent and received over ordinary telephone lines at speeds to 120 char/s, using standard telephone company data sets. Receiving units can operate unattended with single or dual, high capacity tape cassettes which accommodate more than 20 pages of double-spaced text each. Cassettes can be played back on the receiving typing system, or on a standard model 800 electronic typing system. Copy is typed out at 350 words/min. □

Circle 148 on Inquiry Card

# Monitor or generate at any level or speed, economically... Using RTP.

RTP is a family of standard products that allows the direct input and output of analog signals to your digital computer, regardless of which computer you select. All are self-contained, plug-compatible, designed for local or remote applications, and delivered virtually off-the-shelf.

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Measuring a lot of high-level signals at high speed? You'll be interested in the RTP High-Level Controller.

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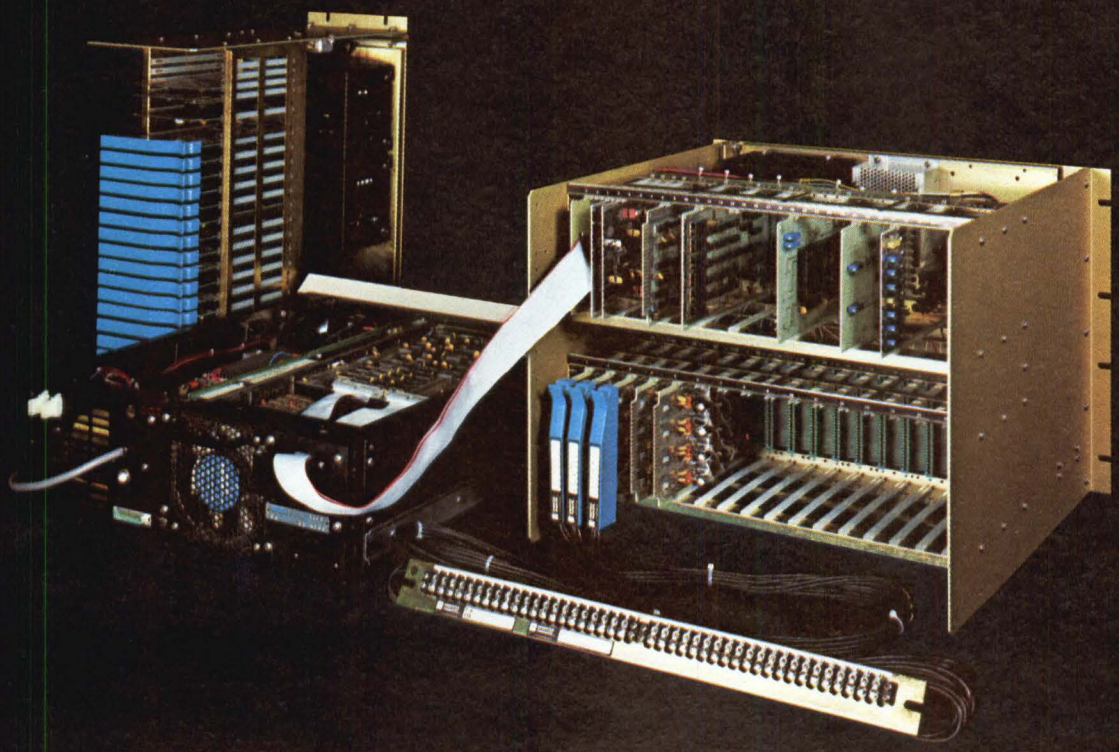
**Computer Products, inc.**

# Analog Signals



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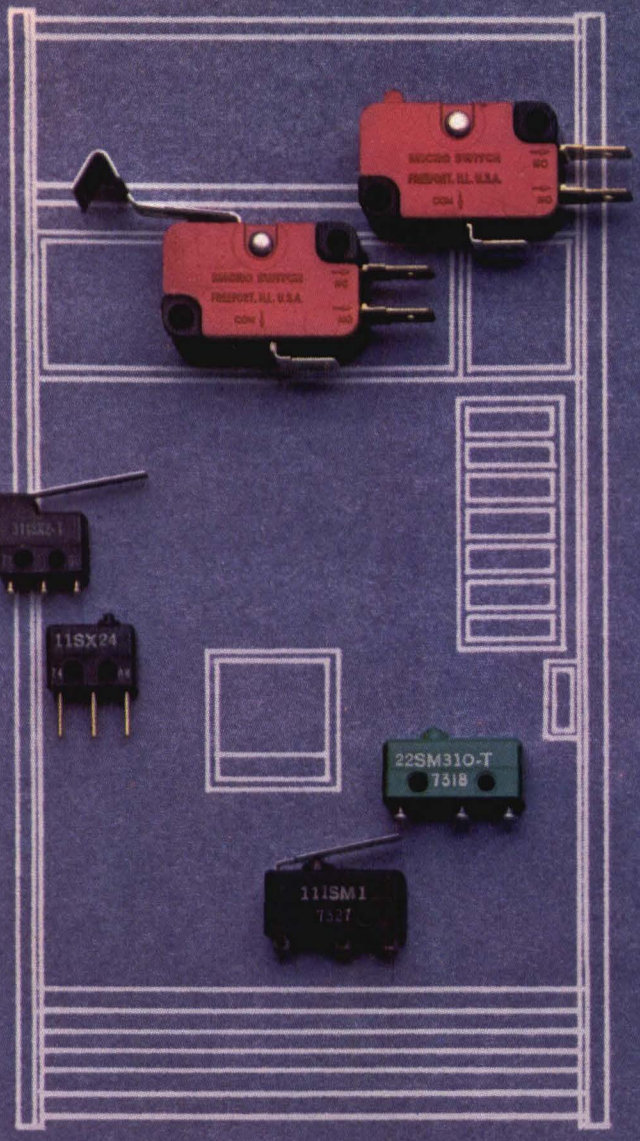
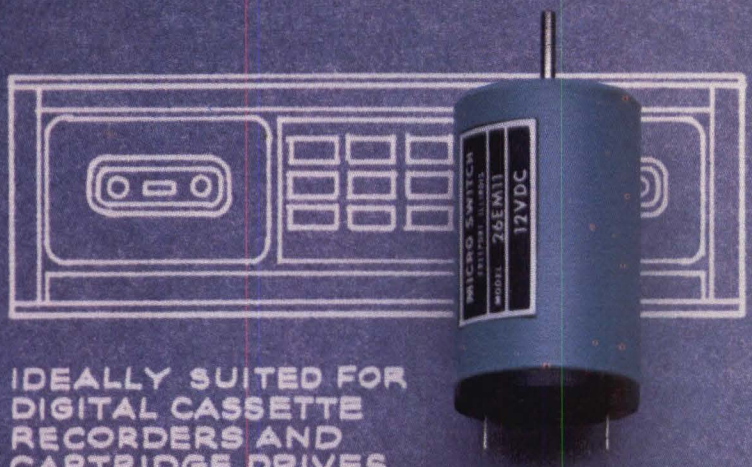
Japanese Distributor: Tamagawa Seiki Co., Ltd. 3-19-9 Shin-Kamata, Ohta-Ku, Tokyo, Japan 144. Phone: 03-731-2131.

CIRCLE 24 ON INQUIRY CARD

# Some of these components will probably




SNAP-ACTION V3, SM AND SX SWITCHES PROVIDE HIGH RELIABILITY AND ARE CAPABLE OF HANDLING HIGH OR LOW ENERGY CIRCUITS; PROVIDE OUTSTANDING PERFORMANCE FOR SELECTION, TIMING AND DISPENSING FUNCTIONS IN VENDING MACHINES.

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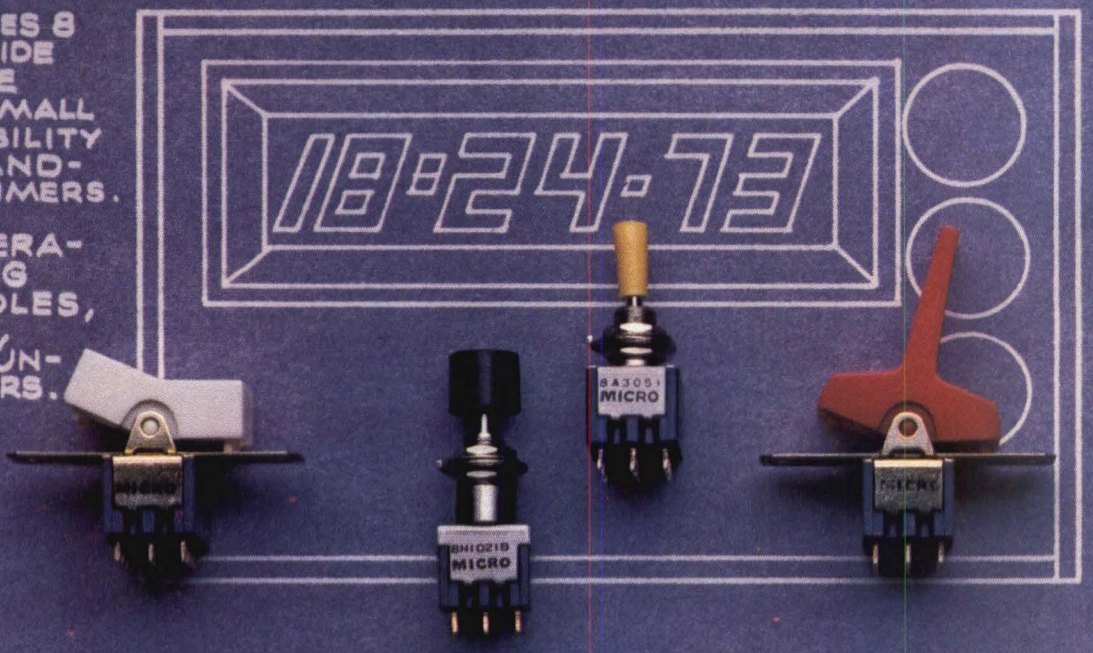
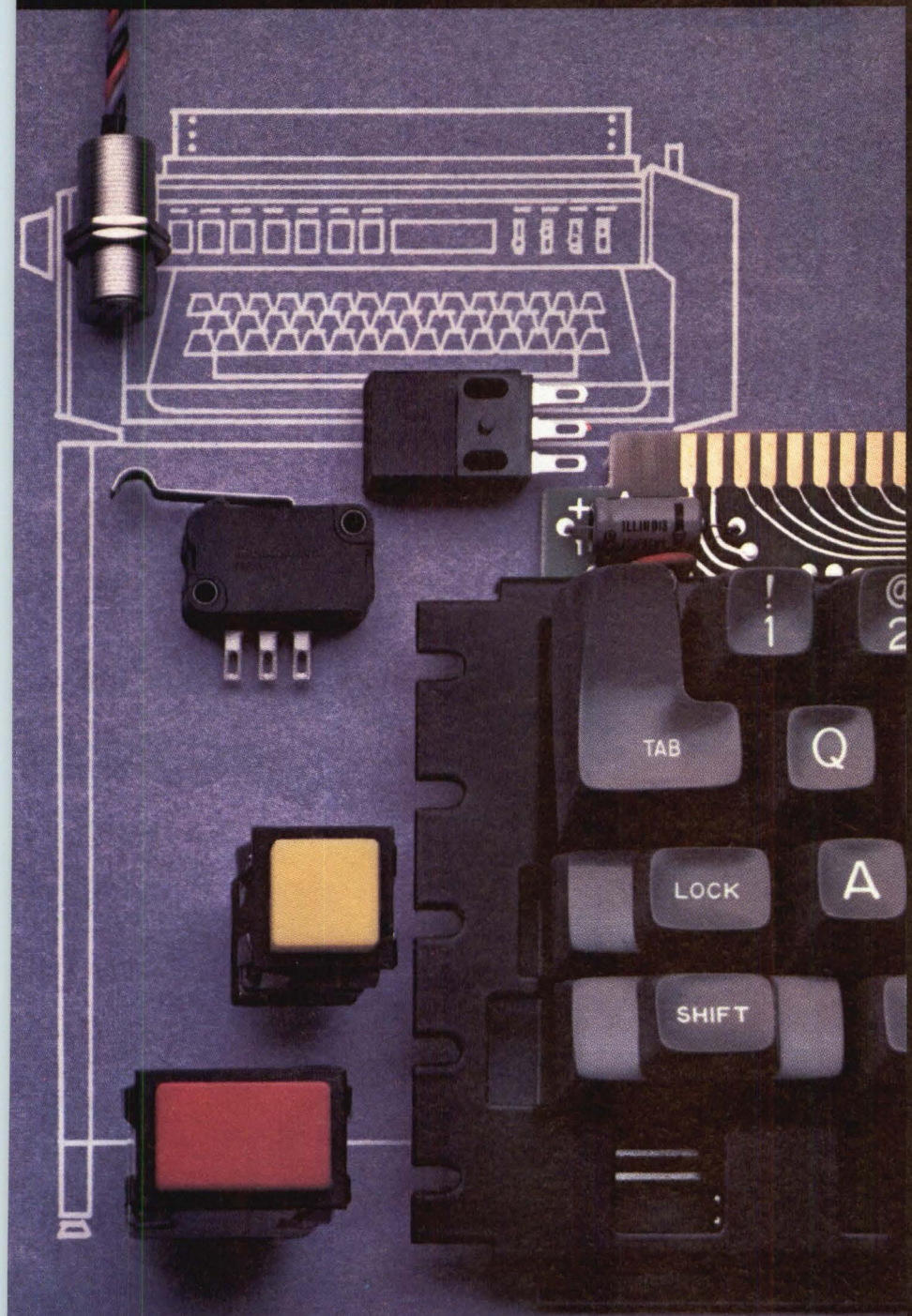


# never wear out. The others will just come close.

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## CCDs Are Potential Replacements for Moving Magnetic Memories

Charge-coupled devices (CCDs) are being considered as solid-state replacements for moving magnetic memories and to bridge the gap between high cost random access memories and the slow access magnetic memories. One such device, the MN2.5, has been developed by Mnemonics, Inc of Cupertino, Calif in a 22-pin ceramic package. As recently discussed at a scientific conference[1] and in a society journal,[2] the 64K-bit block-addressed charge-coupled serial memory uses an offset-gate CCD electrode structure to obtain small cell size and an adaptive system approach to utilize nonzero defect memory chips.

This memory chip is organized as 64K words x 1 bit in 16 blocks of 4K bits (Fig. 1), with each block organized as a serial-parallel-serial array. The chip is fully decoded with write/recirculate control and 2-dimensional decoding to permit memory matrix organization with X-Y chip select control. All inputs and outputs are TTL compatible.

Each of the 16 CCD blocks in the memory chip, shown in Fig. 1, can be independently accessed by applying appropriate address signals. Four address buffers receive address bits $A_0$, $A_1$, $A_2$, and $A_3$ at TTL voltage levels and generate the addresses and their complements at MOS voltage levels. Four row and four column address decoders generate the appropriate row-select (RS) and column-select (CS) signals to select one of the CCD blocks.

An input-data buffer and a write-enable buffer receive the input-data (IN) and write-enable (WE) signals at TTL voltage levels and generate IN and $\overline{WE}$ signals: IN is sent to the input/recirculate circuit of the 16 CCD blocks; $\overline{WE}$ is sent to the row decoders to inhibit the RS signals when no new input data are to be written into the memory. A chip-enable buffer receives two chip-select signals, $\overline{CE}_X$ and $\overline{CE}_Y$ at TTL voltage level and generates a complementary chip-enable signal, $\overline{CE}$. This signal inhibits IN, $\overline{WE}$, RS,

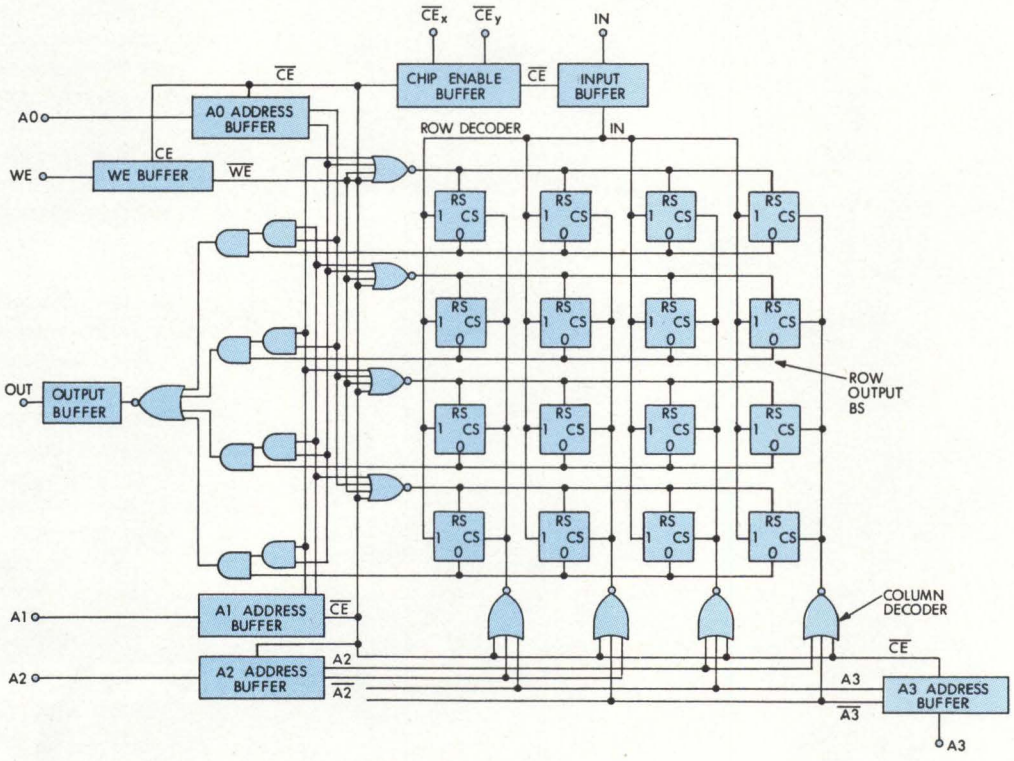


Fig. 1 Block diagram of Mnemonics MN2.5, a 65,536-bit block-addressed charge-coupled memory chip. Organization is in 16 independent recirculating CCD registers of 4096 bits each. Blocks are organized as serial-parallel-serial arrays, and any one of the blocks can be addressed by applying an appropriate 4-bit address input

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and CS signals when the chip is not selected.

CS signals gate the outputs of the charge-detection circuits to the row output buses. A second set of RS signals generated from the addresses route the appropriate row output to the chip output buffer.

The chip output data buffer receives the information from the CCD block selected by the row and column decoders and drives an open-drain output transistor. This device is capable of sinking 3 mA at 0.4 V and 100°C and driving a 50-pF output load at frequencies as high as 10 MHz. When the memory chip is not selected, the output transistor is turned off, thereby providing OR-tie capabilities of the memory chips. Two dc power supplies, 12 V and −7.5 V with ±10% tolerance, are required.

CCD blocks recirculate data automatically as long as the clocks are continuously applied and no write command is given. Ten clocks are required to operate the memory chip. Four clocks—P1, P2, P3, and P4—operate the chip peripheral circuits. The CCD arrays operate with two fast overlapping serial clocks, P1S and P2S (Fig. 2); two fast gating clocks, PB and P2PF, which interface the serial registers with the parallel CCD array; and the two parallel slow overlapping clocks, P1P and P2P.

Although parallel clocks P1P and P2P drive a large capacitance, their drive requirements are reasonable since they are about 64 times slower than the serial clocks. All inputs are sampled and latched at the beginning of each clock cycle. Output data change at the beginning of each clock cycle and remain valid until the next clock cycle. Any bit can be accessed with a maximum of 4287 clock cycles.

Average latency time of the CCD device is 2 ms to 400 $\mu$s and serial data rate is 1M to 5M bits/s over a 0 to 70°F temperature range. Full block address decode is onchip. Because of thermal leakage currents, the charge-coupled storage mechanism is dynamic in nature. To satisfy the refresh requirements and maintain the data integrity, the minimum clock frequency is 1 MHz. Power dissipation is 1 $\mu$W/bit at the 1-MHz output data rate including reactive power in clock drivers.

Access to the recirculating blocks is performed in a random access mode. A 4-bit address selects one of the blocks for read, write, or read/write operations. Information is written into and read out of the memory in a line format consisting of 64 bits of data separated by three cycle times. One whole line of data can be read from one or more of the 16 blocks by applying the appropriate 4-bit addresses.

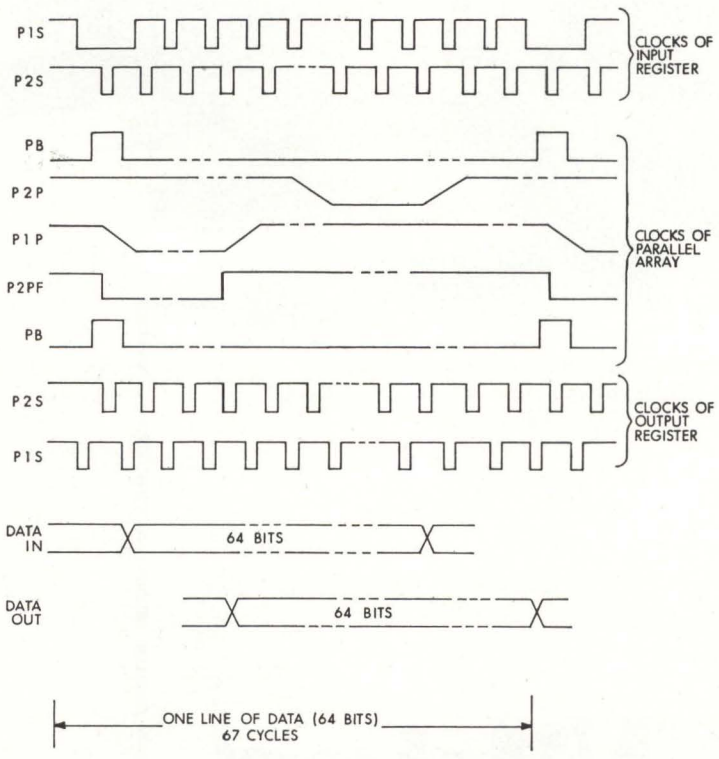


Fig. 2 CCD memory input/output and charge-transfer timing diagram. Arrays operate with a set of 2-phase fast serial clocks, two other fast clocks which interface the serial registers with the parallel array, and two slow parallel clocks

### References

1. A. M. Mohsen, R. W. Bower, M. Wilder, and D. Erb, "A 64K-Bit Block-Addressed Charge-Coupled Memory Device," *Digest of Technical Papers*, 1976 IEEE International Solid-State Circuits Conference, pp 180-181

2. A. M. Mohsen, R. W. Bower, E. M. Wilder, and D. M. Erb, "A 64-kbit Block Addressed Charge-Coupled Memory," *IEEE Journal of Solid-State Circuits*, Feb 1976, pp 49-58

## Schottky Diodes Match Computer Power Supply Rectifier Requirements

Although the basic family is one of the oldest in the solid-state field, and despite their capability to convert ac to dc with 50 to 80% lower losses than by pn junctions, Schottky diodes have not been commonly used for power devices. Chief reasons have been the difficulty of obtaining performance reproducibility, and the problem of attaining a reasonable value of reverse breakdown voltage.

Both problems have been solved by a fabrication method in which platinum is sputtered onto the silicon base and by utilizing a mesa structure. According to the developer, General Electric's Research and Development Center in Schenectady, NY, platinum silicide is formed in a reliable, reproducible manner with

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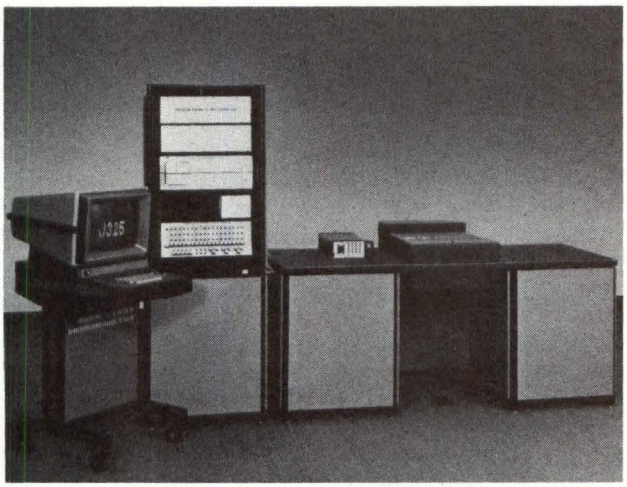

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a barrier height of 0.80 eV. The mesa structure eliminates the problem of premature low voltage breakdown.

Devices made by this process can operate at ratings up to 150 V. (This is four times higher than that of Schottky rectifiers now on the market.) Power rectifiers have been made that have forward drop of <0.70 V at 50 A, switching time of <50 ns, and reverse breakdown voltage of >100 V.

This research was supported in part by the NASA Lewis Research Center which also provided guidance on goals and specifications. Dr Linus F. Cordes, Ernest A. Taft, and Dr Marvin Garfinkel are responsible for the actual research effort. The resultant power rectifiers are reproducible and have suitable performance characteristics for use in computer power supplies and other low voltage applications.

## Military Tests BORAM Module as Replacement For Discs and Drums

What may eventually be a replacement for electromechanical disc and drum secondary memories in severe environment military applications is now being operationally tested at the Naval Air Center, Patuxent River, Md. Later it will undergo additional testing at the Army Electronics Command, Fort Monmouth, NJ. A partially populated, general-purpose nonvolatile semiconductor computer memory, the block-oriented random-access memory (BORAM) uses a metal nitride oxide semiconductor (MNOS), a drain-source protected gate, memory transistor, as its basic storage component.

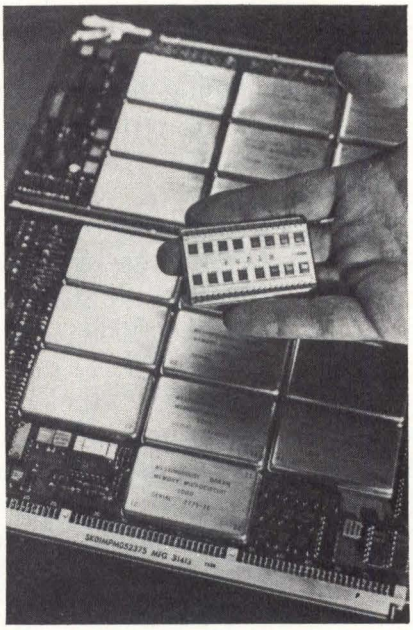
A 2K-bit memory, including read/write circuitry, is achieved on a 154- x 170-mil chip by large scale integration (LSI). When fully populated, a module will store 16.8M bits of information.

The memory module was developed by the Westinghouse Defense & Electronic Systems Center, Baltimore, Md, with joint Army/Navy funding. Military organizations supporting the development effort include the U.S. Army Electronics Command, Army Tactical Data Systems, the Naval Air Systems Command, and the Naval Air Test Center.

A block of data in the BORAM module can be accessed in <30 $\mu$s, about 100 times faster than fixed-head drum or disc storage. Also, the all-electronic memory will have reduced volume, weight, and power requirements. Physical storage densities for the module are 476 bits/cm$^3$ and 366 bits/g—about one-fourth the volume and two-thirds the weight of a moving-head disc system currently being used by the military. Cost is expected to be competitive with militarized electromechanical storage.

The device provides memory by storing or removing charge from deep trap sites located near the oxide-nitride interface. Retention times exceeding 4000 hr are possible because a relatively large amount of energy is required to lift the charge out of the traps. Data are retained in memory if power is shut down or interrupted.

Since the memory chips need be powered only when data transactions take place and electrical stress is thereby removed from the chip, power is conserved and the failure rate is reduced. This reliability advantage becomes dramatic for larger systems or longer mission times.



Density of 2K bits on a 154- x 170-mil chip, including R/W circuitry, has been achieved using MNOS transistors and LSI. A single memory unit contains 16 such chips (shown held in hand); each memory card contains 304 memory chips packaged in 19 units

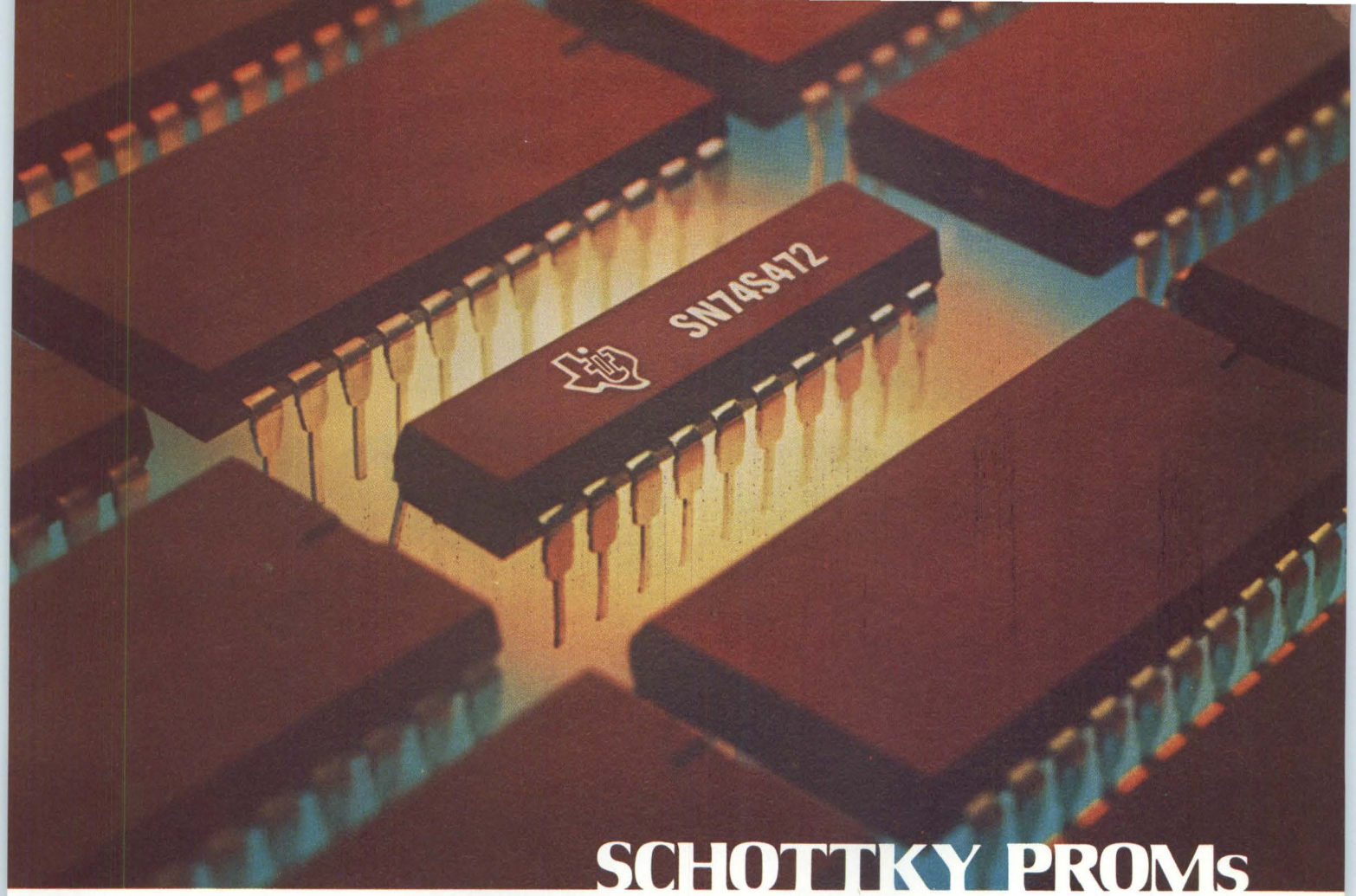
Memory cells can be extremely small because the storage component is a single transistor. BORAM chips are currently being laid out (using conservative line widths and spacings) which have cell sizes of about 0.5 mil$^2$. As photolithographic capabilities improve, MNOS densities will improve even further. BORAM chips with 100K bits of memory are being projected.

BORAM-type chips can efficiently transfer blocks of data at high rates using onchip, parallel transfer of data to shift registers. The shift registers can be operated at data speeds of 5 MHz. Also, much of the offchip electronics required by other memory technologies can be avoided. Other advantages for secondary memories include reliability in severe environmental conditions, temperature stability, radiation resistance, no computer logic interface problems, and the potential for low-cost batch fabrication.

The present memory module contains a circuit board for input/output (I/O) and self-test, a board for memory control, a power section mounted behind the front panel, and up to 32 PC cards, each with 304 MNOS memory chips and card power control. All functions which could change if BORAM is used with a different computer are located on the I/O board. Changing that board can make BORAM compatible with almost any computer system.

The BORAM module contains circuitry which checks the accuracy of data and provides an alarm in case of errors. A Hamming single error correction code is used. When data are read from storage, they are checked and decoded. Any single bit errors are corrected before being transmitted to the computer. Single bit errors, which are the most likely type of data failure, can be tolerated without interrupting system operation.

Each MNOS memory chip contains a fully decoded 64-word x 32-bit random-access memory (RAM) and two dynamic 16-bit shift registers. All data I/O flow serially through the two shift registers. To read data from the BORAM memory chips, data are accessed from the RAM, transferred in parallel to the shift registers, and then shifted out serial-

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# New 4K PROMs from Texas Instruments slice pc board area by 54%.

TI has placed its newest, high-complexity, 512-word by 8-bit PROMs into compact, 300-mil width, 20-pin dual-in-line packages. These new 4K PROMs are the latest addition to TI's space-saving, cost-effective Schottky PROM family. The result: Improved system density with savings as much as 54% in PC board area. A space-saving package is just one of the benefits TI offers.

First, you have a choice of a three-state bus-driving PROM (SN74S472). Or, an open-collector output PROM (SN74S473).

Second, Schottky-clamping gives these PROMs superior speed/power characteristics. Typical access time from address, 50ns – from chip select, 20ns. Both new PROMs feature low-current, MOS-compatible, pnp inputs as do all TI's Schottky PROMs.

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| SN74S470N<br>SN74S471N | 256 W x 8 B, O-C, 20 Pins<br>256 W x 8 B, 3-S, 20 Pins | 8.37<br>8.37 |
| SN74S287N<br>SN74S387N | 256 W x 4 B, 3-S, 16 Pins<br>256 W x 4 B, O-C, 16 Pins | 3.95<br>3.95 |
| SN74S188N<br>SN74S288N | 32 W x 8 B, O-C, 16 Pins<br>32 W x 8 B, 3-S, 16 Pins | 2.55<br>2.55 |
| MILITARY – 55°C to 125°C (Ceramic) | | |
| SN54S472J<br>SN54S473J | 512 W x 8 B, 3-S, 20 Pins<br>512 W x 8 B, O-C, 20 Pins | $37.20<br>37.20 |
| SN54S470J<br>SN54S471J | 256 W x 8 B, O-C, 20 Pins<br>256 W x 8 B, 3-S, 20 Pins | 16.74<br>16.74 |
| SN54S287J<br>SN54S387J | 256 W x 4 B, 3-S, 16 Pins<br>256 W x 4 B, O-C, 16 Pins | 7.88<br>7.88 |
| SN54S188J<br>SN54S288J | 32 W x 8 B, O-C, 16 Pins<br>32 W x 8 B, 3-S, 16 Pins | 5.61<br>5.61 |

Third, these new devices are made with TI's unique titanium-tungsten fuse links for fast, low-voltage, reliable programming. The same metallurgy used for over five years to fabricate all TI's patented Schottky-clamped PROMs and TTL. Thus, by using these new 4096-bit PROMs, you can upgrade old designs and improve new ones.

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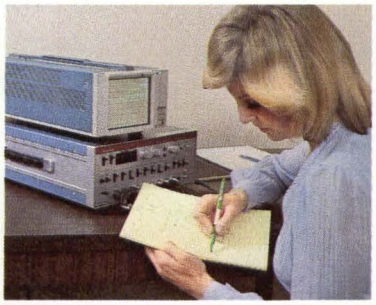

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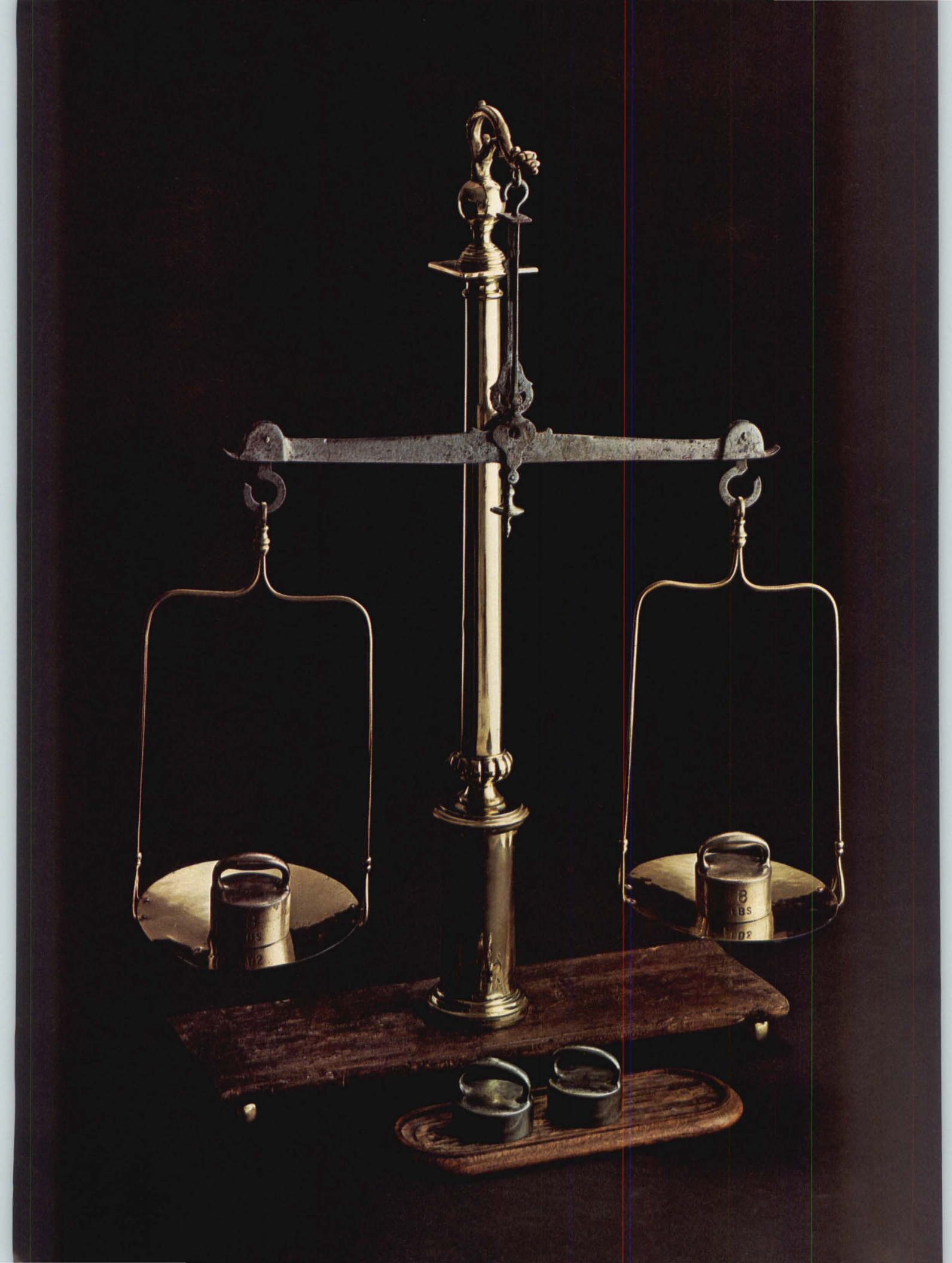

# The SEL Mini keeps its balance, to help you keep yours.

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On the hardware side of the scale, we'd like to say a few brief words about obsolescence, throughput, and I/O.

The SEL 32 Mini's powerful CPU architecture is proof against obsolescence. Want to upgrade? Just change a board or two.

Throughput? The SEL Bus is capable of transferring data and commands at a continuous throughput of 26 megabytes per second. Based on a 150 nanosecond clock, this has established the industry standard for bus speed.

Lastly, I/O. The SEL 32 is the only 32-bit mini that employs micro-programmable, independent processor-based I/O, so it doesn't have to steal cycles.

That's all quite nice, but so far, it's just iron. Let's take a look at the other side of the scale: software.

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But there's more to software than a super track record.

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One of those tasks, the new SEL Terminal Support Subsystem, allows up to 16 CRT operators to develop programs, debug, or activate tasks... concurrently. Result? Increased flexibility.

Another SEL software bonus is our highly optimizing FORTRAN IV Compiler, which reduces the amount of memory and execution time required for a program. In addition to its full ANSI-standard capabilities, several extensions are available which enhance its real-time applications even further.

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ly from the two registers. While data are being shifted out, the RAM is free to access a new data word. To store information, the entire chip is first set to a logic 1 state; then the information is serially shifted into the chip and written into the memory transistors word by word.

The partially populated BORAM module, which has been delivered to the Naval Air Test Center for initial test and evaluation, contains 152 MNOS chips on one memory board. The I/O board uses the Navy standard NTDS interface. After completion of tests at Patuxent River, the memory with another I/O board for the Army TACFIRE interface will be tested at Fort Monmouth.

## Analogic NC Programming Eases Transition of Job Shops to Computer Use

Need for computer expertise by machinists programming numerically controlled (NC) tools is circumvented by use of a computer in a system developed at the Massachusetts Institute of Technology, Cambridge, Mass. Formulated as part of David C. Gossard's PhD thesis in the Dept of Mechanical Engineering, the "analogic part programming" process allows "a machinist with no knowledge at all of computers to program an NC machine tool—and after only a couple of hours of practice."

Reportedly, programmer training time is dramatically reduced, programming efficiency is increased, and some persistent programming problems are solved. In essence, it eliminates physical verification of NC tapes, lowers psychological barriers built up against computers and NC devices in small to medium sized job shops, and enables use of unskilled programmers.

The system provides an interactive graphic display of the working area of an NC machine tool that permits "part programming by doing." In operating the system, a machinist sits in front of a display of a workpiece, tool, and fixturing which appears on a cathode-ray tube. By using hand cranks, he then guides the tool through the movements required to machine the desired part, watching the tool movement and changes in the workpiece on the display as he goes along.

Mistakes and corrections can be made freely, in effect permitting the operator to "ruin" a part without ruining it. As he enters each tool movement, the system creates a part program on tape for an NC tool.

Instead of selecting only the best machinists in a shop for training as programmers, and then spending six to nine months in training those persons and teaching them one or more of the many possible part-programming computer languages, skilled machinists—after a half hour of explanation and an hour of unstructured practice—can set up an analogic part program. The machinists are able to use their years of on-the-job training and their inherent skills since they can "see" the results.

Verification, one of the major problems in setting up an NC tape, is eliminated. Instead of cutting dummy parts or even running a tape through the machine with no workpiece, "verification" is now accomplished by playing back the tape and watching a display scope. The system can also verify tapes prepared by conventional programming. Prof Gossard believes that the optimal programming procedure may lie somewhere between the analogic and symbolic methods, taking advantage of the best features of both.

## Large Screen Laser Display Has High Speed Graphics Capability

Laser-Scan HRD-1, a computer-controlled laser display/plotter, produces clear and detailed graphics for design applications and can draw a map defined by 350,000 bytes of data in less than 2 min. The unit can reproduce more than 5000 x 3500 resolvable lines on a screen measuring about 39 x 26″ (100 x 70 cm). Fine line drawings in various styles and shaded drawings are reproducible to within one-tenth of a line width. Among its potential applications are the display of detailed subjects such as dimensioned engineering drawings, PC artwork, and command and control information.

Developed by Laser-Scan Ltd, Cambridge Science Park, Milton Rd, Cambridge CB4 4BH, England, the system displays large amounts of high resolution graphical information in a stored display mode. It uses no core storage; refresh information is superimposed on the stored picture and used to effect changes and additions to this picture. A tracker ball and cursor, 16 illuminated function buttons, and a keyboard are provided for this interactive mode.

When microfiche hardcopy is required, the argon ion laser beam is directed through the optimized doublet lens onto diazo film which can be developed immediately, producing a permanent negative image suitable for reproduction or enlargement.

Used as a simple plotter, the unit can draw digitally-coded information to the same standards of resolution and precision as a flatbed plotter in a fraction of the time. The map can be brought up to date or the profile altered by editing in the display mode.

A complete software package will provide full computer control of plotting, display, and interaction based on FORTRAN. With the interactive use of the refresh mode, an enlarged view of a small area on the screen can be produced.

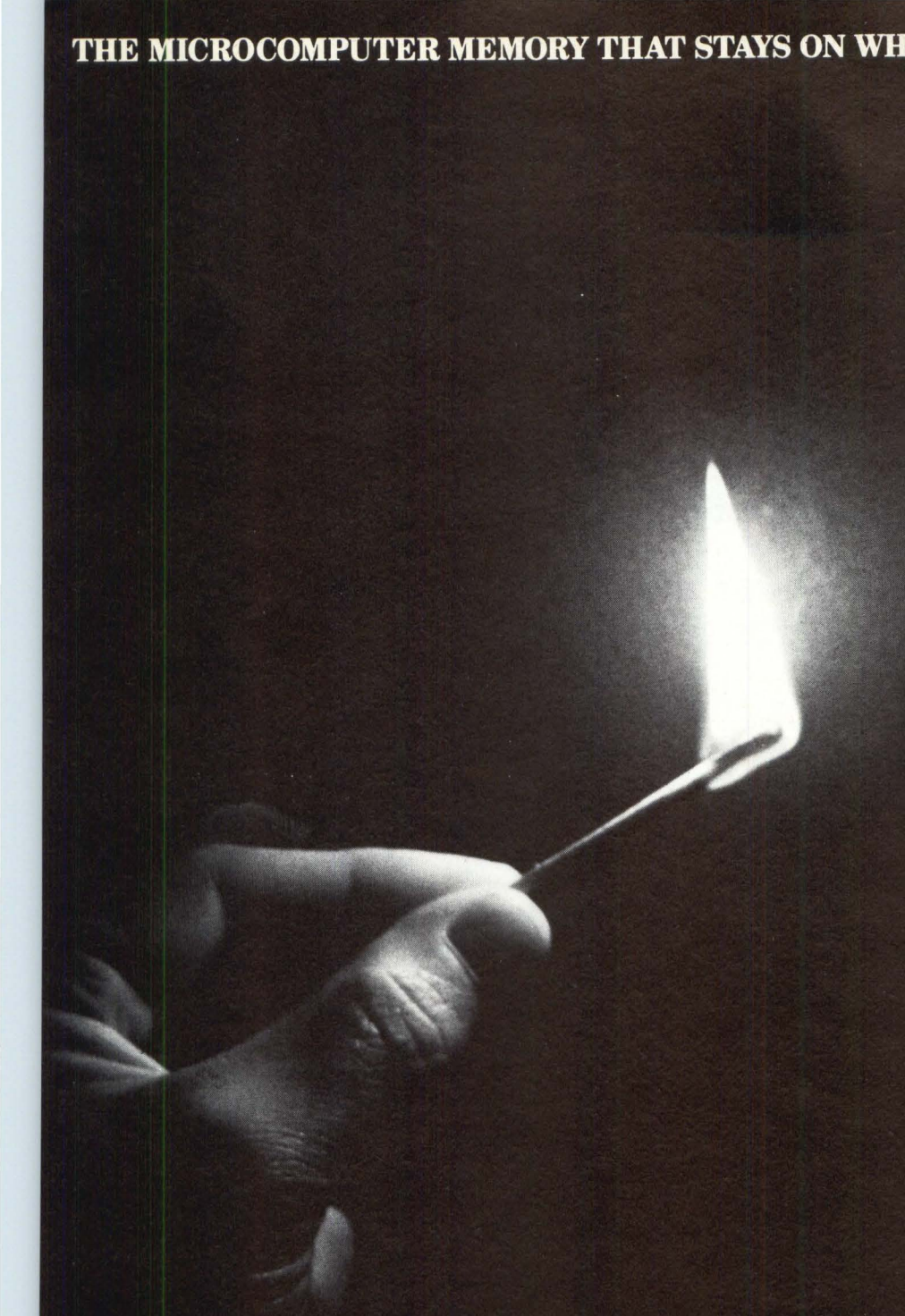
## Proven Insulation Adaptable to Computer Cabling Applications

In use for several years for insulation applications such as power generating plants, rapid transit vehicles, and military aircraft, Tefzel fluoropolymer is now being used to insulate power and signal cables in computer systems. For one example of the material in use, single or double flat conductors carry power while ribbon cables with 60 coplanar conductors carry signals.

Although the material has for some time held a UL listing as a wire extrusion insulation, DuPont Co of Wilmington, Del has now also been granted a UL "yellow card" on series 200 and 280 Tefzel for relative thermal index recognition of 170 electrical and 155 mechanical for molding applications. This recognition also places the resins in the 94 V-0 flammability classification.

The melt-processible thermoplastic has excellent resistance to most solvents and chemicals as well as to high energy radiation. It is usable from −190 to 155°C (−310 to 310°F) and has good low loss dielectric properties. □

# THE MICROCOMPUTER MEMORY THAT STAYS ON WHEN THE POWER GOES OFF.

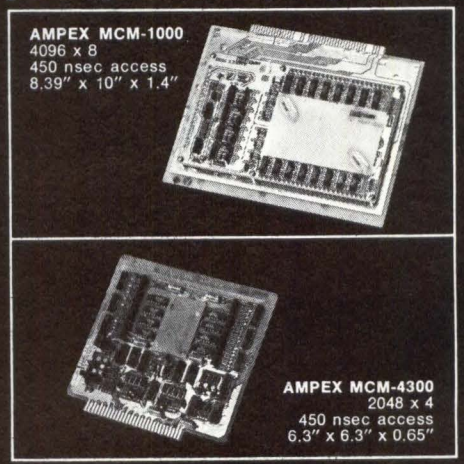


Ampex MCM. Microcomputer Core Memory. It retains everything, even in the event of a total power failure. No batteries or other tricks, just the unflappable reliability of magnetic core technology.

Ampex MCM comes complete, with all timing and control, data and address registers, decoding and drive circuits and, of course, your choice of core capacity. You can specify the word length you need from 4 to 18 bits, and storage for 256 to 4096 words, in all popular binary increments.

Modest-capacity MCM modules are complete on a single board; use as many as required to achieve the total capacity you desire. All of them are available with a single connector strip, with pinouts to suit your design.

Ask yourself if your microcomputer-based system can afford a program loss due to power interruption. If you answer "no" to that question, then you'll answer "yes" to Ampex MCM modules. They offer the least expensive protection you can buy. When the power goes off, they stay on.

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# Professional Group Conference Stresses Microprocessor Applications for Process Control

**Sydney F. Shapiro**
Managing Editor

Organized and presented by working engineers and scientists for their counterparts, this year's annual meeting of IEEE's Industrial Electronics and Control Instrumentation Group was held in Philadelphia, Pa on March 8 to 10. Theme of IECI '76 was "Industrial Applications of Microprocessors, Process Measurement, and Failure Mode Analysis." However, nearly all papers presented during the first two days of regular sessions concerned applications of microcomputers and, occasionally, minicomputers. An evening panel session on March 9 covered programmable controllers. Only the last day's papers discussed transducers, process measurement, and reliability.

## Where Microprocessors Are Used

If there is any clear distinction between types of control processes where microprocessors (MPUs) can be used and where they are not practical, that separation was not evident from the subjects of the papers presented at IECI '76. Applications ranged in scope from true control or automation to monitoring and data acquisition. Actual processes involved were as diverse as a nuclear power generating station and an aisle stacker crane, liquid natural gas transfer and telemetry, and a "teachable" robot and automotive traffic control. The only common element among most of the many processes was the inclusion of some type of MPU as controller, with accompanying random-access or read/write memory (RAM) (R/W), and read-only memory (ROM) and/or programmable ROM (p/ROM). The following are only samples of the many MPU-controlled systems discussed at the conference, but indicate the wide range of MPUs being used.

## Nuclear Reactor Core Monitoring

Although the hardware included is similar to that which might be incorporated in minicomputer systems, a microprocessor was used instead in an out-of-core detection and monitoring system.[1] According to the speaker who described the system, an MPU was chosen "because of needed reliability." Function of the system is continuous monitoring of the axial power distribution within a reactor using 4-section excore detectors. Rapid time response as well as high accuracy and total system reliability and security are attained for one phase of a pressurized water reactor nuclear power plant.

The self-contained microcomputer system is based on an Intel 8080 MPU that is housed with clock and power on/auto restart circuitry on a single card (Fig. 1). Program storage is on ROM and RAM. The MPU bus is buffered for use by system interface cards. System components include a 4-channel multiplexed A-D converter (ADC) for detector current inputs, digital displays and annunciators, and a single-channel D-A converter (DAC) for system output.

UV-erasable p/ROMs were used for system development and checkout. These were replaced by ROMs in the final system for required security. A single-chip 128 x 8 RAM device supplies the necessary 75 bytes of temporary storage.

The MPU performs online testing and internal diagnostics of ROM, RAM, and ADC during each calculation cycle. A ROM test detects single-bit or whole-word errors, data or address lines stuck high or low, or missing ROMs. Each RAM location is tested for both read and write functions. Diagnostic software locates and specifies the actual RAM or ROM device that is in error. If a fault is detected, the system will attempt to reset itself.

## Warehouse Stacker Crane Control

Although developed for controlling motion of a captive aisle stacker crane, this microcomputer-based system is also relevant to many industrial systems both within and outside the material handling field.[2] Predecessor systems were built around a programmable controller in one case and TTL logic cards in a second. The first was programmable but not sufficiently modular. In addition, its programs were written as relay ladder

# The reign of the PMOS UART is over.

## Long live the king. Intersil's new IM6402 CMOS UART.

It's the CMOS/LSI Universal Asynchronous Receiver/Transmitter (UART) for interfacing computers or microprocessors to serial data channels. The IM6402 operates with Intersil's IM6100 family of microprocessor peripheral circuits. It's pin compatible and price competitive with the AY-5-1013, TR1602 and TMS6012 PMOS UARTs, but far superior, making it the new ideal for use in modems, printers, peripherals and remote data acquisition systems.

Because it's CMOS, it provides data transfer rates up to 200,000 Baud (3.2 MHz clock frequencies) with data word length from 5 to 8 bits. That's a *ten-to-one* improvement over previous PMOS UARTs. And because it's CMOS, power is reduced from the 300mW typical with PMOS, to only 10mW for the IM6402, at supply voltages from 4 to 11 volts.

The IM6402 is packaged in a 40 pin DIP, available off-the-shelf from Intersil distributors in a military (−55° to +125°C) version for $26.50 (100+ quantities) or a commercial (0° to +75°C) version for $6.95 (100+).

## Talking to a TTY? Try the IM6403.

The IM6403 version of this CMOS UART contains an on-chip 4/11 divider stage; this, plus on-chip oscillator, allows use of inexpensive crystals—for example a commercial color-TV crystal—resulting in an appropriate Baud rate for easy teletype interface.

Both of them. IM6402 and IM6403, the new king of UARTs. Only from Intersil. 10900 North Tantau Ave., Cupertino, CA 95014.

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CIRCLE 30 ON INQUIRY CARD

# When it comes to computer networks, MODCOMP offers you a big advantage.

# Experience.

At MODCOMP, we were pioneers in making the concept of resource-sharing computer networks a practical reality. The tieing together of multiple computers in distributed processing systems whereby several computers work together, sharing the work load.

Putting the computing power out where the work is, yet allowing each computer in the network to do not only its own job, but also draw upon the resources of every other computer in the system.

We developed MAXNET as a standardized operating system exclusively for this purpose. And MODCOMP systems using our network software have been in operation for more than two years.

We now have over forty network systems in the field, with another fifteen or so being readied for early delivery. Which means that we have more experience—both in length of time and in numbers of systems installed—than all our competitors combined.

In addition to traditional "host-satellite" networks, we have systems in operation that include so-called "ring" networks, "star" networks, and many more. The important thing is that you can link your computers together in any format you want. Provide each computer with whatever peripherals are best suited to your purpose. And leave the rest to MAXNET.

We figure the best way to give you an idea of what MAXNET can do is to give you some examples showing how other people are now using it.

We invite you to study these case histories. More important, we invite you to get in touch with us so you can get a first-hand look at how well they work. Which is a lot more convincing than just listening to us brag about them.

Meanwhile, we have a couple of brochures you should send for.

Our MAXNET brochure deals with computer networking, and how MAXNET makes it all happen.

The other is a thirty-two page booklet that explains in detail exactly what we mean by MODCOMP "TSP." The Total Systems Performance that has made MODCOMP first choice of many of the world's toughest computer buyers.

If you're into computers at all, the TSP brochure is "must" reading. If you're into resource-sharing networks (and if you're not, you soon will be), the MAXNET brochure is equally compulsory.

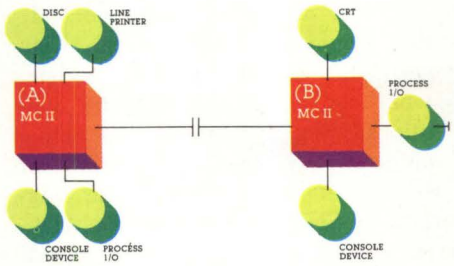
Write Modular Computer Systems, 1650 West McNab Road, Ft. Lauderdale, FL 33309. Phone (305) 974-1380.

European Headquarters:
Export House, Woking,
Surrey, England
Phone (04862) 71471

**Case History No. 1**
A giant aluminum company chose MODCOMP for this simple two-computer "network."
Computer A is at one of the Company's plants in Pennsylvania. Computer B at a research facility in Tennessee, several hundred miles away. The two computers communicate with each other over ordinary dial-up telephone lines. Using MAXNET, operators at either location have full access to all the resources of both computers. Data, programs, peripheral services can be freely exchanged.

For example, suppose a research engineer at Computer B needs to compile a new program. By a simple terminal request, he can call down language processors from Computer A, compile and edit his program on his own computer, and transmit his listing outputs back to Computer A for printing.

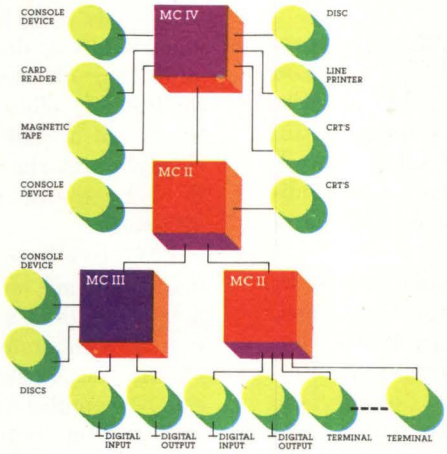
Alternatively, a programmer at Computer A can prepare a program and load it directly down to Computer B. Even though it's the break of day in Tennessee, and the computer is all alone in the office.




This relatively simple system illustrates the flexibility of MAXNET, whether the computers in your network are in adjoining rooms, or a thousand miles apart. It would work just as well if they were on different planets, but nobody's asked us to do that. Yet.

**Case History No. 2**
This MODCOMP Network is in operation at the central R&D facility of a major oil company. It's a good example of how MAXNET, coupled with across-the-board compatibility of MODCOMP hardware, allows you to start as small as you want to, and grow as big as you need to. Without a heavy initial investment. And without costly re-programming as your system expands.

It started, as part of a long-range plan, with the installation over two years ago of a MODCOMP III. Although this model has now been superseded in our line by later models of the MODCOMP II, it is indicative of the long-term compatibility of MODCOMP systems that the III remains today a vital part of this network.




As the system has since evolved, a 32-bit MODCOMP IV now acts as host computer. Replacing (at a fraction of the cost) the company's former stand alone IBM 1800, the MODCOMP IV is expected to provide 10 to 25 times the throughput of the big machine, which had long since reached its saturation point.

A MODCOMP II acts as communications controller between the host and satellite computers.

The satellites consist of 16-bit MODCOMP II's performing various data acquisition and control functions for a series of pilot plants. The MODCOMP III handles analytical instrumentation, providing simultaneous service to over 80 instruments of various types.

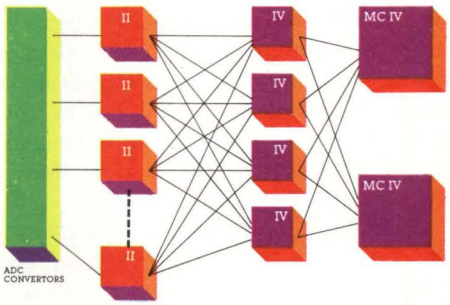
The advantages of this system are, firstly, it's computing power—many times that of the old stand-alone system. It's reliability (the MODCOMP system has had an overall availability of 99.3% of prime time over the past two years). It's expandability, which allows virtually unlimited future growth. And last, but far from least, it's economy and ease of operation.

**Case History No. 3**
A NASA prime contractor has installed this highly sophisticated MODCOMP hierarchical network to handle complex stress and fatigue test analyses.

Dual redundant 32-bit MODCOMP IV's at the "host" level communicate with an intermediate level of several smaller 32-bit MODCOMP IV's, screening data received from the satellite computers. A large number of 16-bit MODCOMP II satellites interface directly to the various processes. The entire system has built-in redundancy at each level.

Among minicomputer vendors, only MODCOMP has the capability to build a network of this size and complexity, using standard hardware and software products. At a small fraction of the cost for a single stand-alone computer large enough to perform the same multiple tasks. And with far greater efficiency.

It clearly illustrates the unlimited expandability of MAXNET in setting up any kind of network system you need to do your particular job.




For clarity, peripheral devices omitted from this diagram.

*Note: The MAXNET systems shown here are all resource-sharing networks of the type commonly used in laboratory and industrial measurement and control systems. For dedicated telecommunications applications, MODCOMP offers a separate software system called MAXCOM. For more information, send for our Data Communications brochure.*

# MODCOMP® TSP*

## *TSP=Total Systems Performance.

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diagrams, not convenient for a sophisticated system. The second was modular but not programmable. Logic additions or corrections required either wirewrapping or more circuit boards.

An Intel 8008 MPU, 3.5K bytes of p/ROM for program storage, and 256 bytes of RAM for program scratchpad are packaged as a Control Logic L series microcomputer. Processing of input commands, control of crane motion, and implementation of other controller features are handled by software logic. In addition, several functions normally associated with hardware are implemented with software.

For operation of the crane, nine commands can be entered into a file. If no error conditions are met, the crane executes those commands sequentially without intervention by the operator or the warehouse's master computer. However, if an error occurs, the system enters an idle mode during which a corrective command can be entered from a keyboard. After the crane completes that command it resumes execution of the remaining commands in the file.

The operator can view contents of the command file as a sequential LED numeric display when the crane is not in motion. Undesirable commands can be canceled or replaced by the operator.

By pressing a button, the operator can place the system in idle mode—after completion of any command the crane is executing at the moment. Then the operator may key in one command which the crane will execute immediately. After that, execution of the file commands will resume.

Plans for future crane controllers call for use of the Intel 8080 MPU rather than the 8008. Superior interrupt capabilities, easier power-on initialization, expanded instruction set, and higher speed were listed as some of the reasons for this change.

### LNG Transfer Measurement

Designed specifically for modern cryogenic gas carriers, such as liquified natural gas (LNG) transport ships, this custody transfer system measures LNG levels and monitors critical cargo conditions.[3] The controller is a 16-bit National Semiconductor IMP-16C/300 MPU which offers microprogrammed multiply, divide, and double-precision add, subtract routines. A single PC card contains MPU, 256 words of R/W memory, and 512 words of p/ROM. An auxiliary memory card provides address decoding and mounting space for an additional 4K words of ROM or p/ROM. As shown in Fig. 2, other elements of the digital processing subsystem are an ADC, teleprinter, and displays. These elements interface with sensors at the LNG tanks through several analog multiplexers and signal conditioners.

LNG levels are measured, displayed, and recorded before, during, and after transfer of cargo to or from a port facility. Also, the system monitors and records critical temperatures, pressures, and liquid densities of the cargo in each of five insulated tanks. Data can be supplied to the ship's ballast and cargo control and transfer system which controls actuation of LNG valves and pumps. Overall system accuracy meets stringent requirements on all parameters.

System sensors connect to their respective conditioners which output signals as dc voltages and/or 4- to 20-mA currents. Voltages are multiplexed, digitized, and forwarded for digital processing.

Online self tests, offline diagnostic programs, and a field calibration program are under MPU control; these are features that would have been prohibitively expensive in an equivalent hardwired logic system. With the MPU system, they are implemented in software and require little additional memory. The online self-test program automatically checks operation of the ADC and the MPU stack register; the offline diagnostic program permits a field engineer to test ADC, multiplexers, displays, memories, and individual signal conditioners via commands from the teleprinter keyboard.

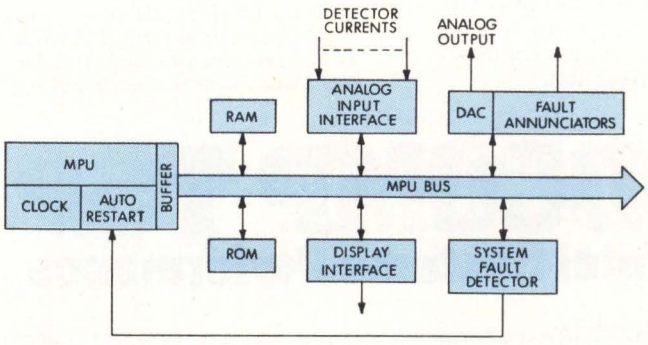
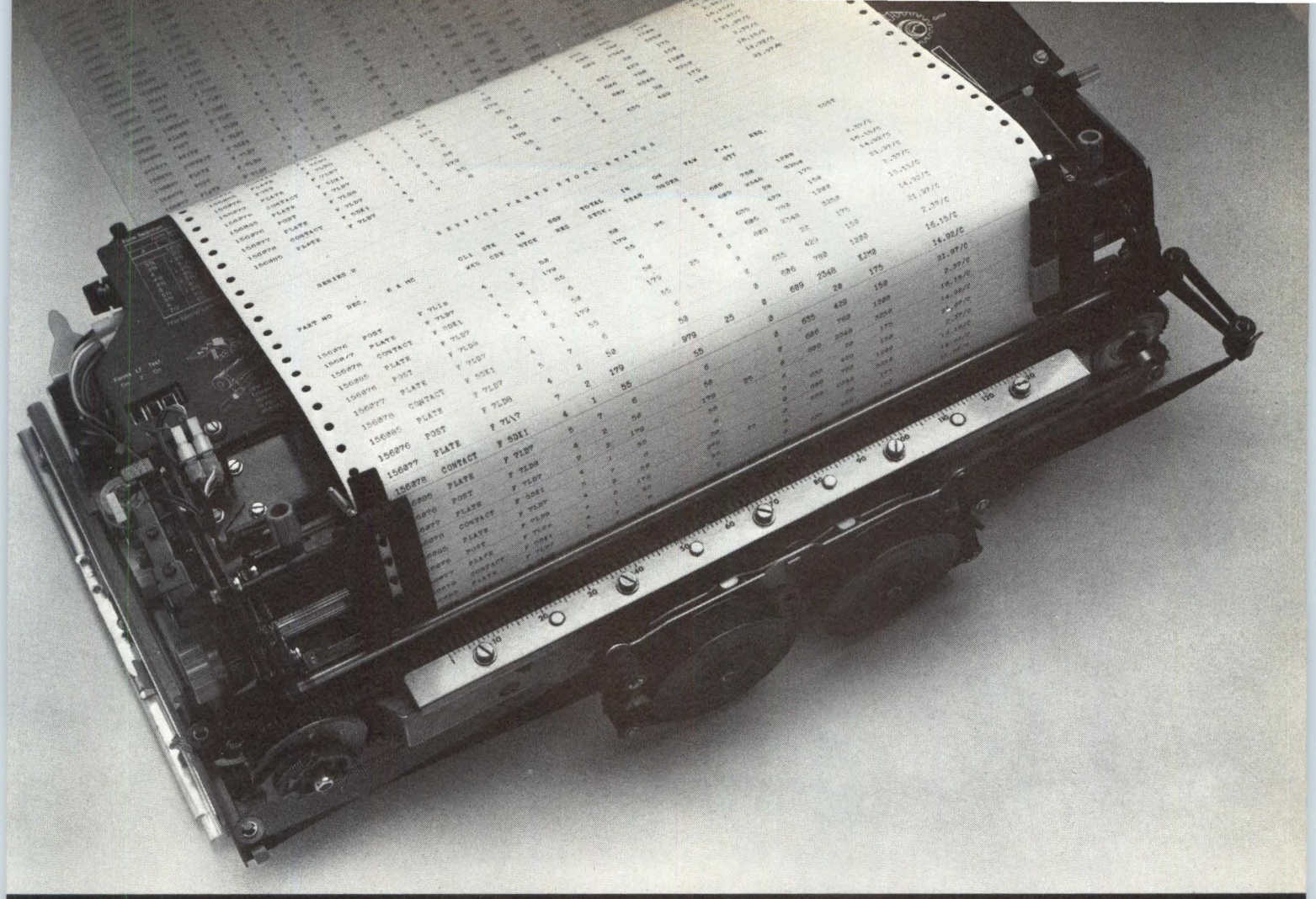



Fig. 1 Westinghouse Electric's excore detector system is controlled by an 8-bit microprocessor. Clock, auto restart, and buffer circuits are on single board with the MPU. Interface with system components is maintained via the buffered MPU bus



(Continued on p 92)



# The Teletype® model 40 OEM printer. When you look at it from price and performance, you'll find it difficult to look at anything else.

The fact of the matter is simply this:
We don't think any other printer can even come close to the model 40.

And that's no idle boast. Not when you consider the facts.

Consider: Where else can you get a 132-column, heavy-duty impact printer that delivers over 300 lines per minute for less than $2000, or an 80-column printer for under $1400?

The big reason behind the model 40's price/performance advantage is our unique design. Even though it operates at speeds of more than 300 lpm, wear and tear is less than you'd find in a conventional printer operating at considerably slower speed. Fewer moving parts and solid-state components add up to greater reliability and reduced maintenance.

Here's something else to consider: Where else can you get a printer that delivers the kind of flexibility and reliability the model 40 offers?

For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE

## The Teletype model 40 OEM printer. Nothing even comes close.

**CIRCLE 32 ON INQUIRY CARD**

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# Very expensive.

You're looking at a superbly engineered disk drive: The Pertec D3000.

In its class of disk drives, the D3000 is expensive. (There *are* less expensive drives available.)

The D3000 is the best-engineered disk drive. (35/40 msec average seek time; internal power supply; exclusive "Power Save" feature; 100 tpi, 2200 bpi; 200 tpi, 4400 bpi; Air-Purge Cycle during start-up; etc.; etc.)

The D3000 is a superbly-tested disk drive. (Ave. burn-in: 49 hours; MTBF: 5865.96 hours.)

## You don't have to be a snob to buy one. You don't have to be rich to keep one.

The Pertec D3000 series disk drives have a capacity range of 3 to 25 megabytes. Three series models and 25 variations provide this range.

The D3000's recoverable-error rate of less than 1 X $10^{10}$ bits transferred offers OEMs superior data reliability over the entire range of specified environmental conditions. Each with a ± 1% spindle speed control.

Parts commonality throughout the Pertec series (no need to stock parts for every model. Spare parts inventories are absolutely minimal), top *and* front loading, easy-to-service "Flip-Top" boards, and interface compatibility with other disk drives make the D3000 an owner's dream. (*And* a

# Not very costly.

serviceman's dream: Only two *hinged* printed-circuit boards. No need to use an extender card.)

## Simplify your new controller design: Use our formatter.

Pertec's F3000 Series Disk Formatter saves the cost and effort of designing (and building) a special formatter/controller. The F3000 performs all formatter functions required to control and transfer data to and from up to *four* drives.

## Turn good money into safe money.

The D3000 costs you less to own. (It's true.)
And it costs less to service.
And it costs less to carry in your inventory.
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So put your money on an expensive disk drive: The Pertec D3000.
And watch good money turn into safe money.

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**CIRCLE 33 ON INQUIRY CARD**

This system is fully programmable, can be customized at low cost, can be altered or expanded in the field, and can simplify and automate manufacturing and field service testing. In addition, it reduces hardware design and development while increasing reliability and maintainability, can be used for jobs that range from simple to very complex, and is potentially adaptable to many other applications.

### Preprocessor for Telemetry System

By including a pipelined microcomputer system as a preprocessor for a larger data acquisition system, the rate capability is extended from approximately 100K to 8M bits/s.[4] The preprocessor system, known as Spacepipe, uses two Scientific Microsystem model 300-40 Schottky bipolar microcomputers.

Primary communication path between Spacepipe and host computer—a DEC PDP-11/40—is implemented by two dual port PDP-11 Unibus compatible memories, one dedicated to each microcomputer. Data from both microcomputers are placed in these memories for access by the host computer. Secondary path is a high speed, 16-bit duplex interface which directly connects each microcomputer to the Unibus.

Motives inherent in developing this system were the desire to extend processing capabilities of general real-time data processing systems, and the need to increase overall system reliability. High speed and LSI packaging of the microcomputers provided solutions to basic problems.

The 300-40 has an instruction speed of 300 ns; each instruction can perform a useful operation in data control. Interface to the microcomputer is through an internal bus which can provide control for up to 28 separate I/O ports.

Although only 90% completed at the time the paper was prepared, the authors reported that preliminary results indicated that design goals had been satisfied. In their opinions, "the addition of modularized microcomputer elements can be used to efficient advantage in real-time data acquisition systems."

### Industrial Robot

Although a number of industrial manipulators or robots are in use, most are driven point-to-point or through continuous paths by instructions pre-stored in some form of memory. By using a microprocessor as the basic controller, however, a manipulator has been developed which can be "taught" by a skilled worker who leads the manipulator through the task using manual controls.[5] Stored commands then permit the manipulator to repeat the task by inputs from stored-position data, sensory feedback, and external status signals (Fig. 3).

Initially designed with minicomputer control,[6] the system configuration was later modified as a stand-alone controller built around an Intel 4004 MPU. At present it contains 1K 8-bit words of p/ROM and 320 4-bit words of RAM.

The manipulator has one translational and five rotary joints, all powered hydraulically. (Prime mover, however, is a pneumatic pump.) Its end effector consists of parallel gripping fingers, a palm that moves along the surface of the fingers, and clutching prongs to grasp non-rectangular objects. An extension thumb in one of the fingers can be used as a mechanical probe or to press pushbuttons.

Position feedback, obtained from direct coupled potentiometers on the joints, is sampled asynchronously through an analog multiplexer. Analog position signals are digitized by a 12-bit ADC which is multiplexed to a 4-bit I/O port in three bytes.

Choice of the 4004 MPU was based on its low cost and availability at the time this project started. Since much student labor was involved in the development, the extra manhours required to organize the system around this MPU were not critical. Presenters of the paper, however, stated that an 8-bit processor would now be justified because it would lower software development costs. It is also likely that a CMOS processor would be desirable in the high noise environment in which an industrial robot is likely to be used.

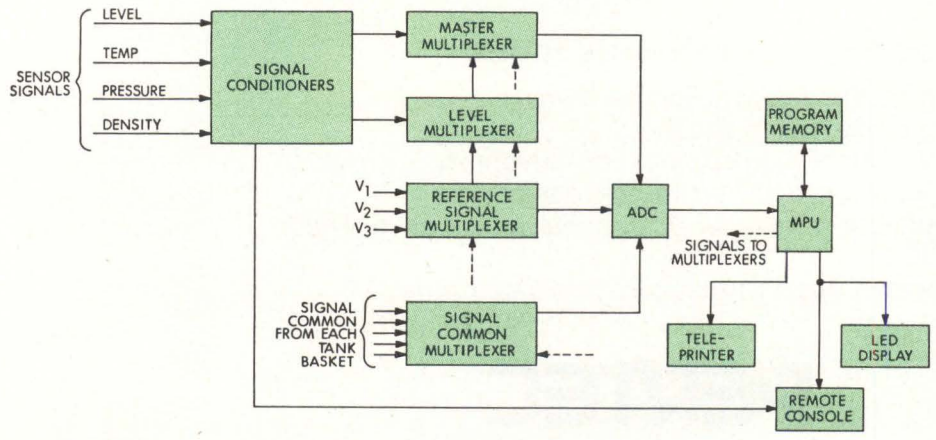
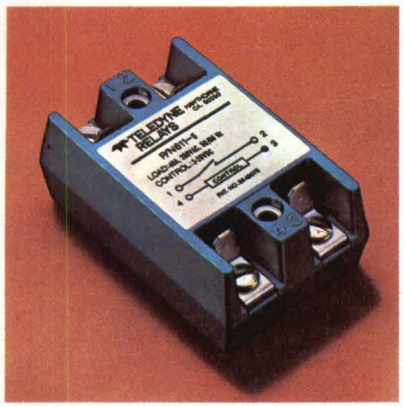



Fig. 2 System designed by Simmonds Precision Products uses 16-bit microprocessor to measure liquid natural gas levels in five tanks of an LNG transport ship, and to monitor critical temperature, pressure, and liquid density parameters. A self test online program controlled by the MPU automatically checks the ADC; an offline program permits the MPU to test the several analog multiplexers



(Continued on p 96)

# The 600V Solid State Relay: the true answer to false triggering.



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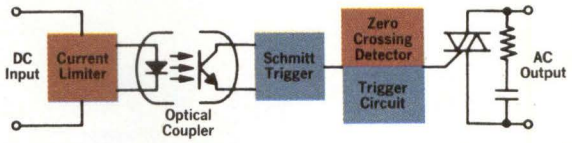
We now offer AC solid state relays specifically designed to prevent false triggering by high voltage transients — the Teledyne 611 "H" version. These relays feature a 600-volt peak blocking capability that provides a high margin of transient immunity. In addition, this feature permits the effective use of external MOV transient suppressors for 240 VRMS line applications. MOV's designed specifically for this use can be ordered direct from Teledyne Relays (Part Number 970-2).




Typical Functional Diagram

Our full line of Teledyne 611 relays listed below includes ac and dc input ranges, with load ratings of 10, 15, 25 and 40 amps. They feature optical isolation, zero voltage turn-on, and a typical dv/dt rating of 200V/$\mu$sec. What's more, we employ a rugged, flame-retardent high-impact package with recessed connections that include both quick-disconnect and screw terminals.

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| INPUT (CONTROL) VOLTAGE | OUTPUT VOLTAGE RATING | | OUTPUT CURRENT RATING AND PART NUMBERS | | | |
|---|---|---|---|---|---|---|
| | CONTINUOUS (RMS) | TRANSIENT (PEAK) | 10 AMP | 15 AMP | 25 AMP | 40 AMP |
| 3-28 VDC | 140 | 200 | 611-7 | 611-3 | 611-1 | 611-5 |
| | 250 | 400 | 611-8 | 611-4 | 611-2 | 611-6 |
| | 250 | 600 | 611-8H | 611-4H | 611-2H | 611-6H |
| 90-250 VAC | 140 | 200 | 611-17 | 611-13 | 611-11 | 611-15 |
| | 250 | 400 | 611-18 | 611-14 | 611-12 | 611-16 |
| | 250 | 600 | 611-18H | 611-14H | 611-12H | 611-16H |


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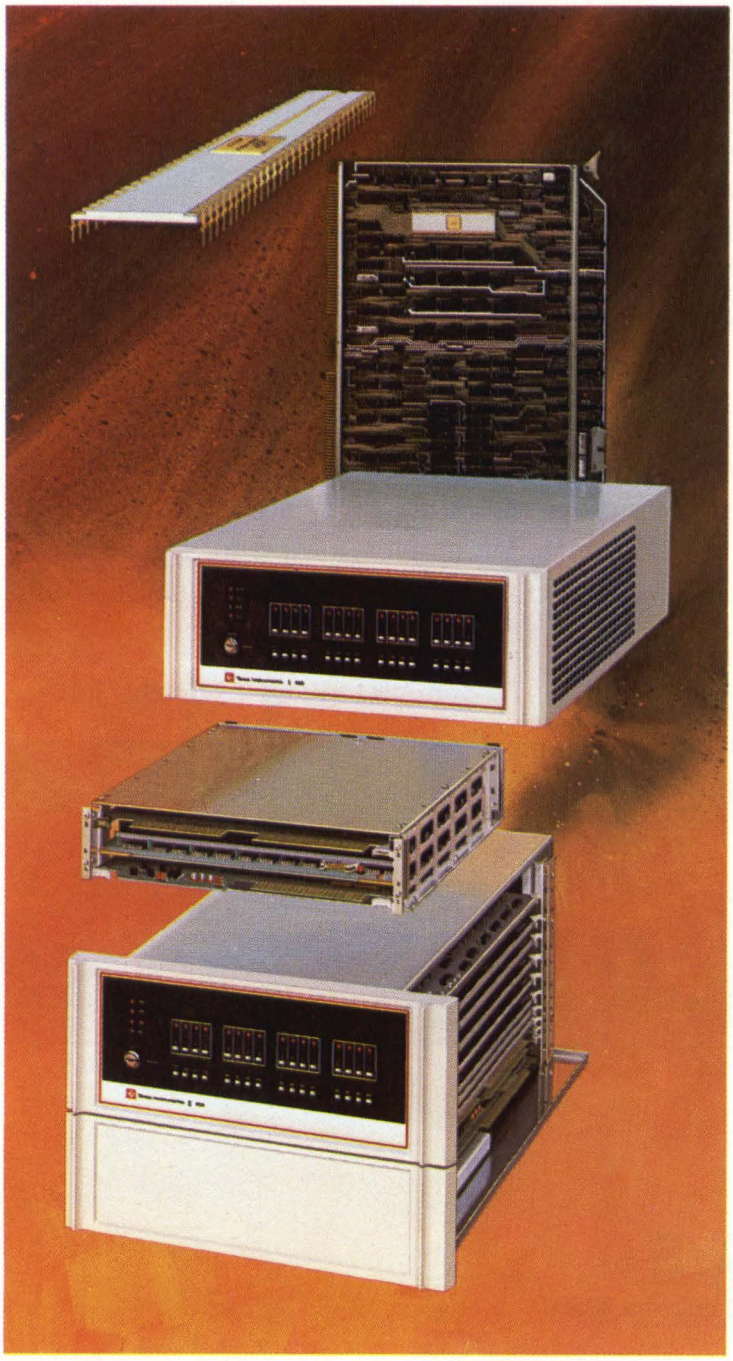

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# UMENTS HAS RE AND HARDWARE.

ble for application software.

The 990/10 Disc System Software accents the mass-storage, random-access features of the disc with extensive file management and the multi-tasking features of the DX10 Operating System. The system software package includes a multi-pass 990 assembler, link editor, interactive source editor, and numerous other utilities that support easy implementation of application programs.

**Flexible Packaged Systems**

TI offers two packaged program development systems and a prototyping system for the user who needs his own stand-alone system for software and firmware development of application programs.

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### Automotive Traffic Control

Although major systems have only recently been placed online for control of automotive traffic by minicomputer (see *Computer Design,* June 1975, pp 40-46), the microcomputer is already being designed into systems for the future (see *Computer Design,* Aug 1975, p 50). The Federal Highway Administration is, of course, involved in many such systems.

Since no calculations except very simple multiplication in a volume density controller are necessary in a traffic controller, MPUs are ideal for the job. The system described at IECI '76 is intended for use at isolated intersections. The controller is an MCS-8008 microcomputer simulator.[7]

### Minicomputer Applications

Although stress at IECI '76 was on microprocessors, as clearly stated in its theme, several important papers were on systems under minicomputer control. In some cases, a speaker referred in his talk to a microprocessor while by common definition his system was using a minicomputer. This does not lessen the importance of MPUs for process control. It does point out, however, that neither have minicomputers decreased in importance for this purpose. There will be adequate room for both in future systems, each handling requirements it can meet better. Likely, in future years, there will be less and less mention of "minicomputer" or "microcomputer" for process control projects; instead, the term will be "computer."

### Sugar Refinery Control

As the result of developments that went through two prior stages in the 1960's and early 1970's, the Kinuura Sugar Refinery, built at Hekinan City, Japan in 1974 adopted a completely centralized control system and man-machine interfaced computer control.[8] It has been operating successfully with a staff of seven persons per shift—and daily production of up to 800 tons, including liquid and dry sugar.

A sugar refinery requires a combination of batch and continuous processes, with a very complicated material flow involving both recycle and bypass lines. The processes have many constraints for control variables such as flow rates and buffer tank levels. In addition, there are a number of quality constraints such as purity and color as well as quantity considerations. Because of the involvement, a simple mathematical form cannot be formulated.

In this plant, a hierarchical system was adopted which divided the control system into two main levels. The higher level determines the optimum flow of materials for the entire process; the lower level gives the references and scheduling parameters of control to the individual batch processes.

Although the computer determines the optimized references to the control systems in the lower level, for the higher level the computer presents a set of feasible solutions of control to the operators who then select which they consider to be the best. This results from the previously mentioned inability to formulate performance criteria mathematically. Because of the possibility of computer failure, an online computer system has not been adopted. Information from computer to processes passes through the operators.

System computer control is maintained by a minicomputer and disc memory (Fig. 4). A color CRT display provides man-machine interface. Overall, the system has proven to be highly efficient and labor saving.

### Batch Mixing of Dry Pet Foods

Until relatively recently the control systems used in automatic mixing of dry pet foods were quite crude and inaccurate—even to the degree of measuring vat content by the numbers of knots remaining on a rope dropped into that vat. In the past 15 years, a move-

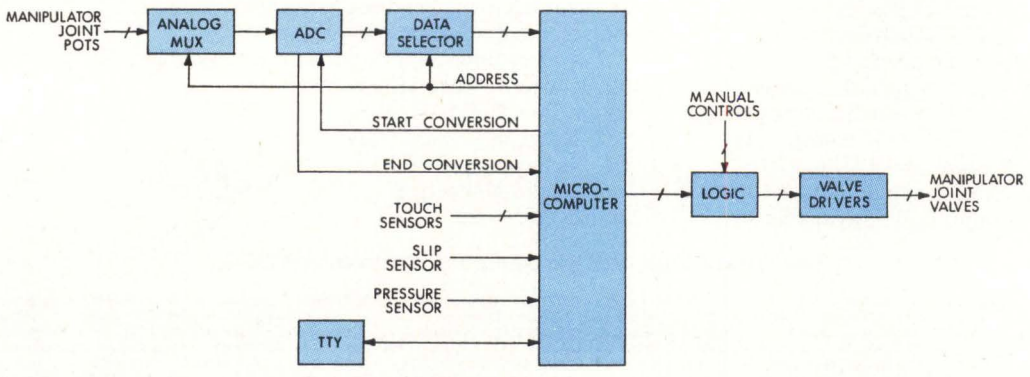


Fig. 3 As experimental "teachable" robot is led by manual controls through the steps required in performing a desired task, the joint positions and commands are stored in memory. The 4-bit MPU controller then can perform the task by executing the stored commands. Stored-position data, tactile feedback, and external status signals are used

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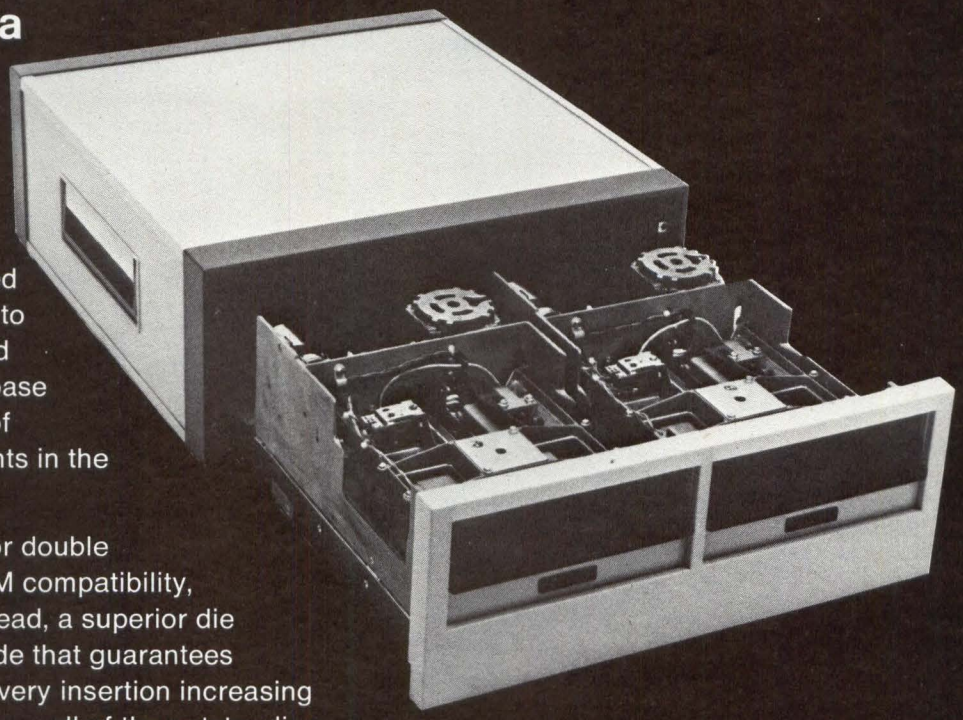

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ment began with resistor packages and progressed to card punches and readers to programmable controllers, and now to minicomputers.[9]

First of the "new" trend began in 1972 with a system based on a programmable controller with 8K memory, an online CRT monitor, and ASR-33 operator interface. Data storage was resident in core memory. Software was set up and dedicated by the vendor. Peripherals, by today's standards, were slow and cumbersome.

A 1975 model, several times faster than the 1972 version, incorporated a General Automation minicomputer and allowed six remote terminals for data acquisition. Approximately three times as many reports were generated, covering additional supplies required by the plant as well as the basic raw materials. Memory was 16K, a keyboard was supplied with the CRT, and data storage was in a mag tape cassette. Online editing was now possible. Software, however, was still vendor-dedicated.

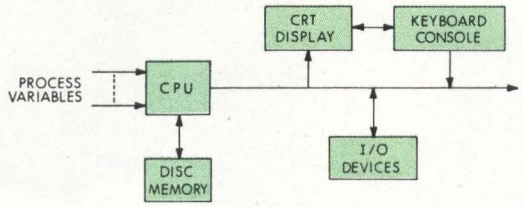



Fig. 4 Minicomputer control of a sugar refinery permits output of up to 800 tons/day with a staff of only seven operators. This is achieved by a completely automated control system and centralization of all controls and operations

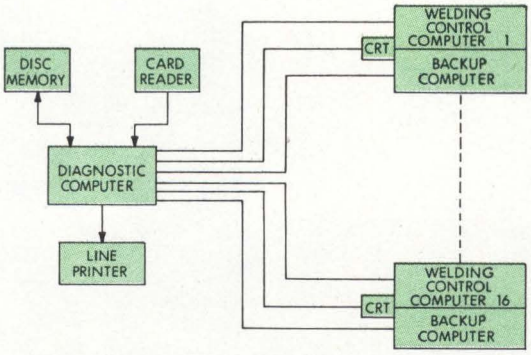



Fig. 5 Diagnostic minicomputer monitors all welding control minicomputers to be certain each is running properly. CRTs, one on each welding line, are used by maintenance personnel to locate problem in a "down" line. Line printer and card reader are used with diagnostic computer instead of a teleprinter because of their high speeds

The 1976 version has 28K core memory and 256K of data storage on a fixed head disc, permitting far more extensive data acquisition than was possible before. A Foxboro minicomputer is used as controller. Software now is developed by the user.

### Truck Cab Welding

At the Chevrolet truck manufacturing plant in Flint, Mich, cabs are fabricated from their sheet metal components in an automatic cab shop comprised of six multi-station welding lines.[10] Whereas robot-type automatic welders can handle only one spot-welding gun, and press welders require cab components to be previously tack-welded, the automatic cab shop applies 1087 welds from 470 welding guns with all movement, positioning, and transfer of components and all welds made automatically under control of a series of minicomputers. No tack-welding is required. As many as 80 cabs can now be processed per hour to feed production lines that run at 55 trucks per hour; in a manual shop, the maximum was 25 cabs per hour.

Main welding lines are connected by accumulating conveyor systems which absorb the differences in welding machine cycle times. Each stores semi-completed cabs from one line until the next line, which may operate slower because it does more positioning and produces more welds, is ready to handle another cab. In addition, the accumulators allow a line to be shut down for repairs or minor maintenance, such as replacement of welding electrodes, without affecting other lines.

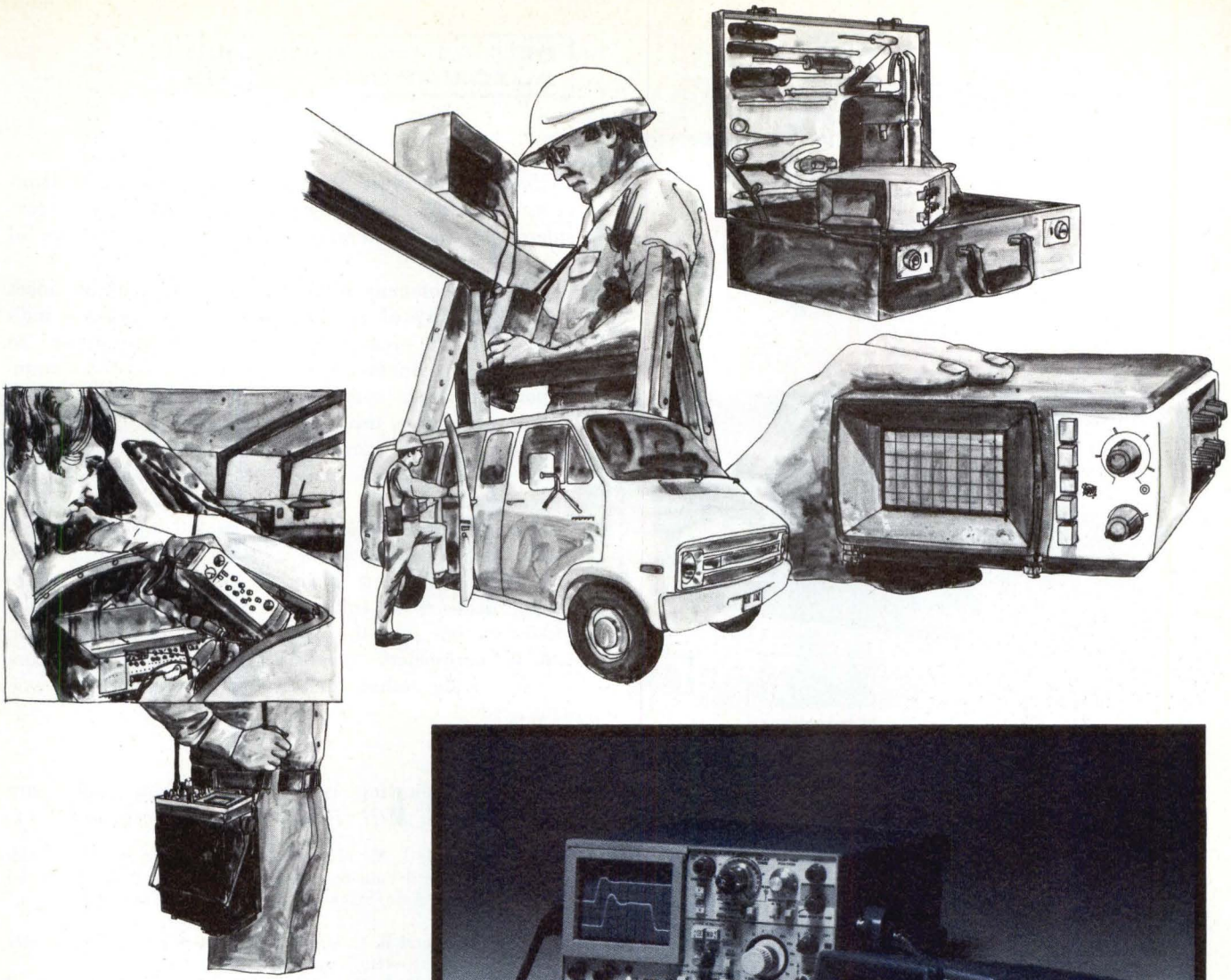
The welding line minicomputers, each a Computer Automation Alpha 16 with 32K memory (Fig. 5), monitor 3900 nonredundant limit switches and control 2100 solenoid valves. Each computer can handle 1024 inputs and an equal number of outputs. To assure continuous operation, a backup computer is included for each control computer on each welding line.

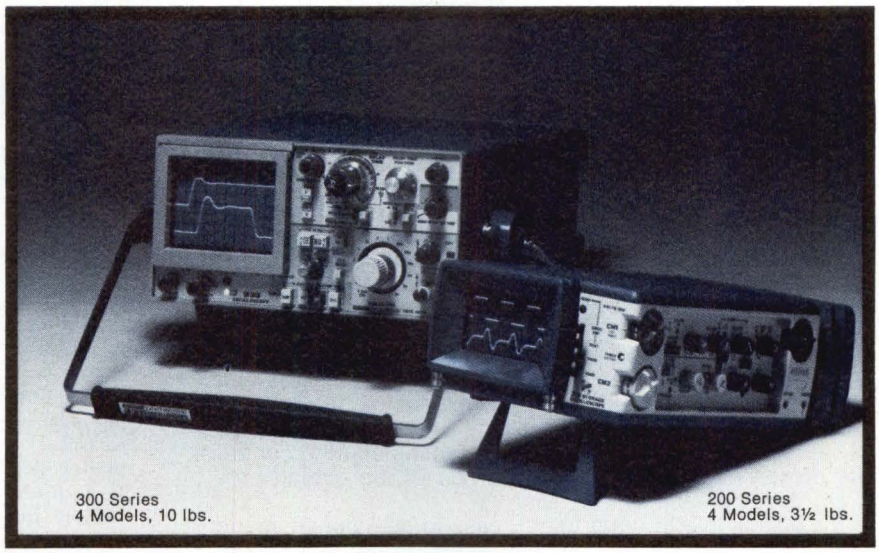
Operation of all control computers and their backups is monitored by a separate diagnostic computer (also on Alpha 16). Notice of a defective line can be sent to maintenance personnel in less than 30 s after a malfunction occurs. (Previous to initiation of this system, such detection and notification of a malfunction might require 5 to 10 min.) Notification of a malfunction is provided on a CRT display at the relevant welding line.

This system has proven to be effective despite the especially noisy environment (caused by the large number of spot-welding operations), and even though some transmission lines are as long as 500 ft (152 m). Signal-to-noise ratio of the 24-V, 60-Hz input signal is maintained at a good level. Problems found in the system have been more mechanical than electrical. Despite inconsistency of size among sheet metal components received from other fabricating plants, finished cabs are maintained within tolerances of less than 30 thousandths.

### Summary

Not yet a "major" conference, IECI '76 showed promise for expansion in future years to that status. Despite little publicity, nearly 200 persons attended this year's annual meeting, a larger number than registered in



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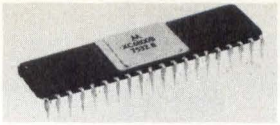
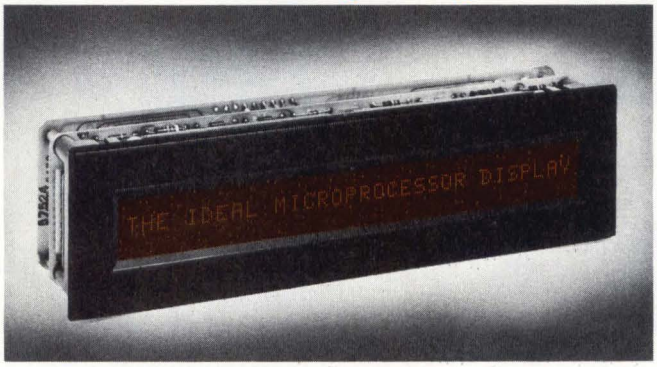


# Your microprocessor, our displays...

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MC6800 chip photo courtesy of Motorola Corporation.

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## DIGITAL CONTROL AND AUTOMATION SYSTEMS

1975, the first year the conference was held. However, even this relatively small attendance was considered by the conference committee to be a sign of success.

Both the company affiliations and titles of attendees and the quality of papers presented by speakers indicated that the program met its intended purpose: to show working engineers and scientists how their counterparts in other companies or laboratories have put microprocessors to use in process control. Although most speakers reported successes, there were also occasional discussions of failures, and what was considered to be the cause of each.

Most failures seemed to be caused by decisions—made several years ago—to start design of process control systems that included microprocessors before microprocessors of sufficient capability were available. Designers fell into the only too easy trap of making system parameters meet what the microprocessors could provide rather than what the users of the systems needed.

### References

All of the following items, except where noted, are included in the *IECI '76 Conference Proceedings.*

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2. G. Caplan, "Auto/Stack-L Microcomputer Crane Controller," pp 25-27
3. D. L. Sharp and R. C. Unger, "A Cryogenic Custody Transfer Measurement System," pp 5-10
4. S. K. Brede, R. L. Gonyea, and M. L. Harvey, "High Speed Data Preprocessing System Using Bipolar Microcomputers," pp 62-66
5. K. Goksel, K. Knowles, and L. Kitis, "A Microprocessor Controlled Industrial Manipulator Programmable-By-Teaching," pp 78-80
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7. J. E. Roehl, "Implementing Vehicle Control Algorithms for Isolated Intersections with Microprocessors," Unbound insert
8. K. Yamaguchi *et al,* "Instrumentation and Man-Machine Interfaced Computing Control System for Sugar Refinery," pp 18-24
9. R. W. Fuerst, "Advancement of Minicomputer Technology As Applied to Batch Mixing of Dry Pet Foods," Unbound insert
10. V. F. DeCrausoz, "Automatic Truck Cab Welding Facility," presented at Conference but not included in Proceedings. Also presented at Society of Automotive Engineers Automotive Engineering Congress and Exposition, Detroit, Mich, Feb 24-28, 1975

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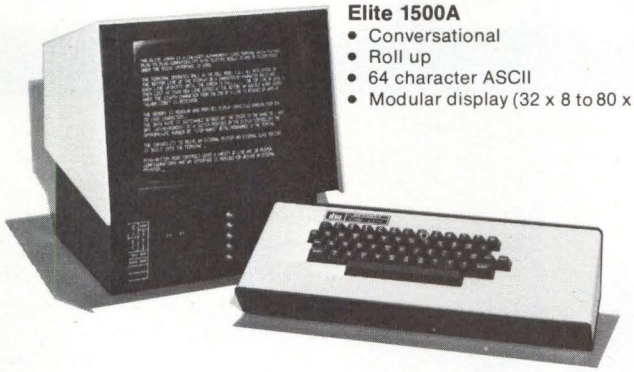
Copies of *IECI '76 Conference Proceedings* containing papers presented at most sessions, but not the evening panel, are available from the Institute of Electrical and Electronic Engineers, Inc, 345 East 47th St, New York, NY 10017. Price is $15 per copy, less 25% for IEEE members.

The 1977 conference will be held in Philadelphia on March 21 to 23. A call for papers and further information will be available at proper intervals in advance of the conference dates. **For details on IECI '77 Circle 160 on Inquiry Card.** □

# See things your way



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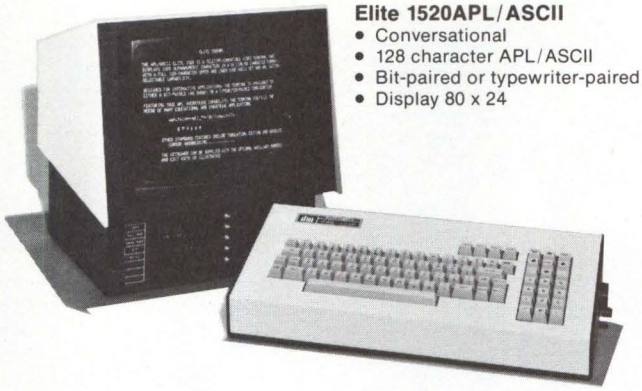
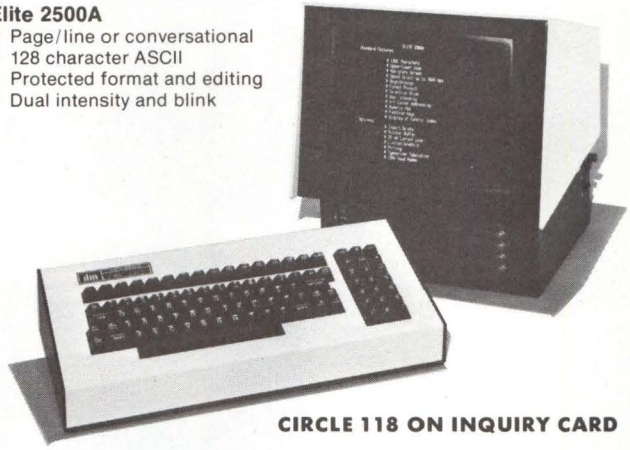
- Display 80 x 24

CIRCLE 116 ON INQUIRY CARD



**Elite 1520APL/ASCII**
- Conversational
- 128 character APL/ASCII
- Bit-paired or typewriter-paired
- Display 80 x 24

CIRCLE 117 ON INQUIRY CARD



**Elite 2500A**
- Page/line or conversational
- 128 character ASCII
- Protected format and editing
- Dual intensity and blink

CIRCLE 118 ON INQUIRY CARD

## with Datamedia Elite Video Terminals

If you're with an OEM firm or a system house, and look at peripherals with one eye on cost and the other on performance, you'll want to take a long look at these proven products from Datamedia.

Their modular design makes troubleshooting a breeze, and facilitates conformance to your system needs, and their quality workmanship assures that those needs will be met longer than you thought possible.

And if you believe in service after the sale the way Datamedia does, you'll appreciate the new dimension we've given to the word "responsive."

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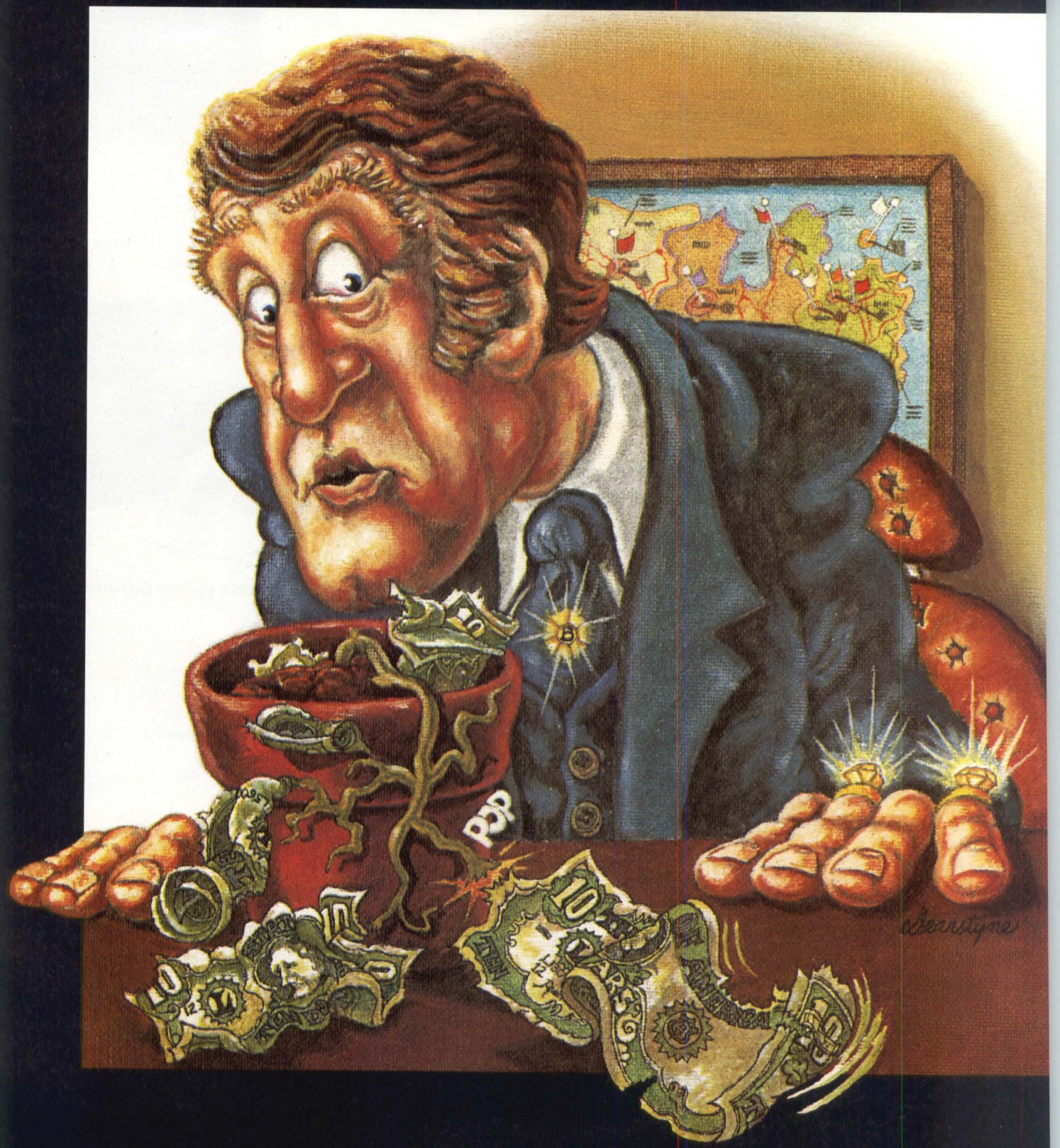
CIRCLE 119 ON INQUIRY CARD

# "Big Bucks" Buckley shade with peripherals



# had it made in the from the mini OEM.

Buckingham Buxton Buckley III.

Born with a Silver Cloud Rolls in his garage. Bought everything, including his mini peripherals, on price: the highest.

But one day, Big Bucks' bubble burst. His boss (Buckingham Buxton Buckley II) said:

"Cut costs, or heads will roll!"

Now, Big Bucks may have been a high-roller, but he wasn't dumb. He could see the handwriting on the wall.

It said: *"We're the largest independent supplier of minicomputer add-on core memories and have a complete line of mini peripherals to expand your DEC, Data General or Interdata mini without putting the bite on your wallet.*

*"Plessey Microsystems.*

*"P.S.: And all the support you need, too, because we're part of an international billion dollar corporation."*

"Hmm," thought Big Bucks. "Largest independent. Won't bite my budget. Billion dollar corporation."

He *liked* that.

So he picked up his phone (French Provincial) and called Plessey (collect).

He found out all kinds of wonderful, money-saving things about Plessey add-on core memories, Plessey single and dual disc drives and Plessey infrared punched tape readers.

From that day on, Big Bucks Buckley bought his mini peripherals from the mini expander, Plessey Microsystems.

## The easy street special

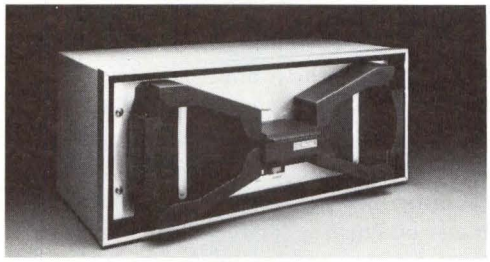
Plessey infrared punched tape readers are an exceptional bargain in mini and micro peripherals.

They're the most advanced punched tape readers available today. A pinch roller/capstan drive improves reliability and lowers tape wear. Advanced electronics permit *asynchronous* operation at any speed from 0 to 1000 characters per second. Infrared optics read tapes with up to 60% transmissivity. And the fine Plessey touch eliminates all mechanical, electrical and photo-optic adjustments.

They're available as an OEM transport, in rack mounts and cabinets, with or without fanfold handlers, in a portable carrying case and as a reader/punch combo.

All with your choice of interfaces for DEC and Data General minis, and many of the popular microprocessors.

And all at prices that, while they might not quite put you on Easy Street, will definitely be a comfort.



He saved his company a bundle.

And he kept his head.

If you'd like to find out how to expand your mini without emptying your wallet, give the people at Plessey Microsystems a call today.

**CIRCLE 123 ON INQUIRY CARD**

Plessey Microsystems
(714) 540-9945

'76 NCC
June 7-10

# 1976 National

## New York Hilton and Americana Hotels,

Celebrating the 25th anniversary of the first Joint Computer Conference—predecessor of the now familiar annual National Computer Conference—in a year that marks both the bicentennial of the United States and the 25th anniversary of the electronic digital computer as a commercial reality, this year's NCC—Landmarks in Data Processing—is planned as an outstanding event. With Dr Carl Hammer, director of computer services for Sperry Rand, serving as Conference Chairman, and Dr Stanley Winkler, manager of applied technology for IBM's Systems Development Div, as Program Chairman, the NCC technical program focuses special attention on the fundamentals of computer science and technology, and attempts to analyze data processing methods and applications, management concerns, societal issues, international relations, and the impact of economic trends on the computer industry. The Conference is sponsored by the American Federation of Information Processing Societies, the Association for Computing Machinery, Data Processing Management Association, IEEE Computer Society, and the Society for Computer Simulation.

Comprising 128 sessions, including five special plenary sessions, the technical program, to be held at the New York Hilton and Americana Hotels, has been divided into three major areas: Computers and People, Systems, and Science and Technology; each area contains approximately 40 sessions within four key topics.

*Computers and People* addresses the key topics of societal concerns, the computer profession, issues in computing, and important applications serving people. Mini-symposia within this area include data security, public access to computers, and industrial and university relationships.

*Systems* deals with computer systems as well as systems management, networking, and business and industrial systems. Within this core are groups of sessions concentrating on microprocessors, minicomputers, system performance and evaluation, and system design.

*Science and Technology* focuses on computer and data base architecture, software, and computer science and its applications. Within this program, mini-conferences cover programming languages, artificial intelligence, mathematical programming, and software design and engineering.

Of special interest is the Pioneer Day Program, which will honor the Moore School of Electrical Engineering at the University of Pennsylvania and participating individuals for pioneering contributions to the development of the electronic digital computer. Three panel discussions on Tuesday June 8 will review events leading to development of the ENIAC, its development, and the technology transfer that occurred in the immediate post-ENIAC time period.

In addition to the regular program, a series of full-day extra-cost Professional Development Seminars will be held each day of conference week. On Tuesday, Structured Programming in COBOL, with Robert G. Abbott of Yourdon, Inc in charge, and Computer Networks, lead by Marshall D. Abrams of the National Bureau of Standards, will be given. Wednesday's schedule includes Design of Online Systems, under the direction of Walter E. Simonson, US Bureau of Census; Management Auditing of Computer Operations, conducted by Harold J. Podell, US General Accounting Office; and Micrographics and Data Processing, headed by John H. Mitchell and Terrence H. Coyle of Eastman Kodak. To be presented on Thursday are Structured Design, lead by Edward Yourdon of Yourdon, Inc; Management of Software Engineering, under the direction of W. E. Simonson and Paul D. Oyer, president-elect of the ADP Users' Group; and Computer Applications for Learning Technology, conducted by Raymond G. Fox of IBM Federal Systems Div. Seminars are restricted to a maximum of 100 individuals; fees are $50 per registrant in addition to at least partial registration for the Conference Program. An additional no-charge seminar, How to Benefit from Attendance at the NCC, will be given on Sunday, preceding the conference opening, and on Monday morning, to provide answers to questions on the program, special features, and exhibits.

# Computer Conference

## New York Coliseum, New York City

**Dr Carl Hammer**
Conference Chairman

**J. Paul Lyet**
Keynote Speaker

**Dr Stanley Winkler**
Program Chairman

## Special Activities

J. Paul Lyet, Chairman of the Board of Sperry Rand Corp, will deliver the Keynote Address at the Conference Keynote Session, beginning at 10:15 am on Monday in the Grand Ballroom of the New York Hilton Hotel. In his address, Mr Lyet will explore the challenges that lie ahead of this industry, which by the end of the next 25 years is expected to be the world's largest. Monday's program will also feature a special International Plenary Session, chaired by Bob O. Evans, president of IBM Systems Communications Div. Mr Evans will be joined by authorities from Japan, the United Kingdom, the Soviet Union, Austria, and Central Europe in reviewing developments that have taken place in computing during the past 25 years.

Highlight of a special plenary session on Tuesday is the AFIPS Presidential Address given by Dr Anthony Ralston, chairman of the Dept of Computer Science, State University of New York in Buffalo. Starting at 12:30 pm in the Grand Ballroom of the Hilton Hotel, Dr Ralston's address will center on the topic of Computing, Politics, and Professional Societies. Following his address, the AFIPS Harry Goode Memorial Award will be presented as will prizes to the winners of the National Student Computer Fair Competition. On Wednesday and Thursday, beginning at 1:15 pm, plenary sessions will focus on computers and government, and on industry and commerce, respectively.

Also on the list of special events are the annual Conference Reception, Monday from 6 to 8 pm, the NCC Student Computer Fair Exhibit, 4th International Computer Art Festival, and Computer Science Film Theater.

A demonstration of interactive computing and network communications will be presented by the program committee in conjunction with the Telenet Communications Corp. Several dozen interactive terminals, installed in the Coliseum and connected through access controllers to the nationwide packet-switching network, will have access to approximately 75 computers. Representatives from each host computer site will demonstrate its capabilities.

## Exhibits

More than 275 organizations will take part in the exhibit which will occupy three floors of the New York Coliseum. Products dealing with virtually every aspect of data processing will be on display, providing attendees with an opportunity to evaluate and compare the industry's latest offerings. Exhibit hours are 11 am to 7 pm on Monday and 10 am to 6 pm on Tuesday, Wednesday, and Thursday. Information on many of the products which will be on display can be found on the pages following the "Technical Program Excerpts." Although products being shown for the first time are given emphasis, others are included for the reader's convenience. Information is necessarily limited to that available at press time.

## Registration

Conference attendees may register at the New York Hilton between 5 and 8 pm on Sunday, 8 am and 7 pm on Monday, 8 am and 6 pm on Tuesday and Wednesday, and 8 am and 1 pm on Thursday; or at the Coliseum between 10:30 am and 7 pm on Monday, and 9 am and 6 pm on Tuesday, Wednesday, and Thursday. Registration fees are

| | |
|---|---|
| Full-Conference (4-day program plus exhibits) | $75 |
| 1-Day Program and Exhibits | 25 |
| Full-Conference Students | 10 |
| 4-Day Exhibits Only | 25 |

Full-conference registration includes a copy of the *Conference Proceedings;* post-Conference price is $50. Bus transportation will be provided between major conference hotels and the Coliseum. Travel information may be obtained by calling the NCC Travel Information Service—(800) 433-2897. Other information on NCC can be obtained by writing AFIPS, 210 Summit Ave, Montvale, NJ 07645; or by calling (201) 391-9810.

# TECHNICAL PROGRAM EXCERPTS

## Computers and People

### Monday Afternoon

Session B1 2:30-4 pm

**25 Years of Joint Computer Conferencing**

(Information not available at press time.)

Session B2 4:15-5:45 pm

**Information Processing in the Year 2000**

Chairman: Walter L. Anderson, United States General Accounting Office

Intended to stimulate thinking about long-range planning, which through consideration of longer term trends and attempts to forecast beyond normal bounds of extrapolation may reveal useful information, this session may provide early warnings on important long-range effects as well as broadening planning viewpoints. Panel members, resident in the year 2000, present information gained from personal experience, extrapolations, long-range forecasts, and intuitive projections.

Session C1 2:30-4 pm

**Role and Obligations of the Trade Press**

Chairman: Ronald A. Frank

(Information not available at press time.)

### Tuesday Morning

Session B3 8:30-10 am

**Computing in Europe**

Chairman: Anita J. Cochran

(Information not available at press time.)

Session B4 10:15-11:45 am

**Origins of ENIAC**

Chairman: John G. Brainerd, Emeritus Professor, University of Pennsylvania

The interconnected string of events that led to development of ENIAC, in which almost every link was vital to its initiation, will be discussed by the panel, who review the problems of realizing a very fast computer, putting together the largest electronic network in existence, and assuring a reasonable reliability.

### Tuesday Afternoon

Session A5 2:30-4 pm

**Data Cryptography**

Chairman: Rein Turn, The Rand Corp

Cryptographic techniques are becoming increasingly important for providing data security in computer systems and networks. Although important progress has been made in algorithms for communication links, questions remain to be answered. Speakers explore the areas of distribution of keys in computer networks, suitability of various algorithms for use in computer systems, applications of cryptographic techniques in data bases, and methods of tailoring cryptographic techniques to specific protection needs.

Session A6 4:15-5:45 pm

**Security in Computer Networks**

Chairman: Dennis K. Branstad, National Bureau of Standards

Speakers alert the audience to threats to data security in computer networks, considerations involving cryptography in the engineering of computer networks, details of one approach to controlling access to data and services of computer networks, and specifications and rationale of an LSI implementation of the NBS Data Encryption Standard.

Session B5 2:30-4 pm

**Development of ENIAC**

Chairman: Herman Goldstine, Institute for Advanced Study

ENIAC was developed between 1942 and 1946 by staff members of the Moore School of Engineering, with effort involving administration, design, construction, and programming. Speakers discuss the process involved in building the machine, which contained 15,000 vacuum tubes and performed useful computations both at the University of Pennsylvania and later at the Aberdeen Proving Grounds.

Session B6 4:15-5:45 pm

**Post-ENIAC Transfer of Technology**

Chairman: Richard E. Merwin, USA BMD Program Office

Completion and demonstration of electronic computing speeds of the ENIAC sparked the birth of the computer revolution. Participants in these beginnings went on to spawn the Eckert and Mauchley Corp, which later became the Univac Div of Sperry Rand, and establish a group at the Institute for Advanced Studies, which built a machine that became the prototype for later scientific computers. Some participants in this technology transfer will describe their experiences during this period of computer technology development.

### Wednesday Morning

Session C7 8:30-10 am

**Industry Needs and Views of Computer Science Graduates**

Chairman: Marshall C. Yovits, Ohio State University

In addition to examining the way industry perceives computer science graduates and how it uses them, this session will determine the shortcomings and problems that have been identified by industry, and suggest corrective measures.

Session C8 10:15-11:45 am

**Computer Science Graduates and Industry**

Chairman: Marshall C. Yovits, Ohio State University

Discussing programs at community college, BS, MS, and PhD levels, in an attempt to determine characteristics of graduates of each type and how they can be of value to industry, this session identifies possible problems, discusses them, and suggests corrective measures.

### Wednesday Afternoon

Session C9, 10 2:30-4 pm

**Industry and University— Problems and Solutions**

Chairman: Marshall C. Yovits, Ohio State University

Considering the problems and mismatches that have occurred between what the universities provide and what industry needs, panelists will offer some potential solutions that will provide graduates endowed with more suitable characteristics.

## Thursday Morning

Session A11 — 8:30-10 am

### Data Communication Policy

Chairman: Neal Gregory

(Information not available at press time.)

Session C11 — 8:30-10 am

### Productivity Payback from Package Application Software

Chairman: Lloyd Baldwin, Lloyd Baldwin & Associates

The frequently encountered "make-or-buy" dilemma is examined in terms of its impact on overall corporate productivity decisions. Speakers discuss the particular relevance of software that relates to data bases in this regard.

Session C12 — 10:15-11:45 am

### High Level Languages for Software Development

Chairman: Eugene I. Lowenthal, MRI Systems Corp

Participants will present two high level program development environments, each with its own domain of applicability. The first is oriented to production and continuing development of applications software, the second to development of systems software, providing the use of a PL/1 subset instead of assembly language.

## Thursday Afternoon

Session C13, 14 — 2:30-5:45 pm

### Quality and Performance Measurements for Software

Chairman: Larry A. Welke, International Computer Programs, Inc

Focusing on the problems of measuring a programming organization's productivity and evaluating the quality of its output, this session covers isolation of basic metrics, techniques for collecting raw data, reduction and interpretation of statistics, and guidelines for instituting remedial steps. Presentations are pragmatic in tone, based on in-depth experience, live data, and specific automated techniques.

# Systems

## Monday Afternoon

Session E1, 2 — 2:30-5:45 pm

### Storage Systems

Chairman: John C. Davis, Dept of Defense

Various aspects of storage systems, including technology, hierarchy, and intelligent memory, are explored in this session to determine which technologies show promise for the future, how they will affect system performance, and what their impact on intelligent memories will be.

Session F1, 2 — 2:30-5:45 pm

### Long Range Planning for Computer Usage in Large Organizations

Chairman: John V. Soden, McKinsey & Co

Session profiles approaches to and guidelines for long range strategic planning for use of information systems technology. Experienced practitioners present three differing viewpoints, stressing a means for securing a link between information systems and overall corporate planning.

Session G1 — 2:30-4 pm

### Legal and Regulatory Trends in Computer Communication

Chairman: Peter E. Jackson

(Information not available at press time.)

Session G2 — 4:15-5:45 pm

### Protocols for Computer Networks

Chairman: Ira W. Cotton, National Bureau of Standards

Although a common interface to packet-switching systems would greatly benefit users, controversy has developed over what approach to take—whether the interface should operate on a virtual call or a datagram basis. Papers argue both sides of this technical and political controversy; an opportunity for rebuttal is provided.

Session H2 — 4:15-5:45 pm

### Air Traffic Control

Chairman: Greg E. Mellen, Sperry Univac

In the past, air traffic controllers performed their task aided only by skin-tracking radar; today they have beacon-transponder radar, whose replies are processed and analyzed in a digital system. Whys and wherefores of the need for automated air traffic control systems are described, and what they will do is detailed by speakers and panel members.

## Tuesday Morning

Session E3 — 8:30-10 am

### Interactive Systems

(Information not available at press time.)

Session E4 — 10:15-11:45 am

### Computer Systems Reliability and Maintainability

Chairman: Stephen S. Yau, Northwestern University

Panelists discuss various approaches to attaining reliable and easily maintainable computer systems, emphasizing both hardware and software design and development, considering structured programming, data abstraction, testing and validation, redundancy, computer architecture, hardware-software interaction, and fault-tolerant systems.

Session G3 — 8:30-10 am

### Packet Radio and Satellite Networks

Chairman: Franklin F. Kuo, Dept of Defense and University of Hawaii

Speakers present some design issues for packet-switching networks having both satellite and terrestrial components, discuss a branching broadcast communication system for transporting digital data packets among locally distributed computing stations, and deal with issues in the implementation of gateways between ARPA's packet radio network and ARPANET.

Session G4 — 10:15-11:45 am

### Progress in Packet Network Intercommunications

Chairman: Robert E. Kahn

(Information not available at press time.)

Session H3 — 8:30-10 am

### Communications, Computers, and Word Processing

Chairman: Harvey L. Poppel, Booz, Allen & Hamilton

Highlighting current integration opportunities, and attempting to forecast the coming telecommunications environment, session emphasizes technology, user impact, and competitive vendors, and considers management considerations that include organizational impact, controls, and planning.

Session H4 — 10:15-11:45 am

### Computer Message Systems

Chairman: David J. Farber, University of California

Computer-based message systems for information interchange offer a nondisruptive entry point for computers in the office environment, and provide the potential for rapid interpersonal communication between geographically separated groups. Session exam-

ines both technical issues and organizational and economic implications of the technology in forming automated offices.

## Tuesday Afternoon

Session E5, 6 — 2:30-5:45 pm

### Modular Computer Design

Chairman: Gerald Estrin, University of California

Although modularity has been accepted intuitively as desirable in computer system design, there have been many abuses of good design when the concept is reduced to practice. Panelists will clarify their concept of modularity, describe cases exemplifying its advantages or disadvantages, and discuss their experience with support systems purporting to support modular design.

Session F5 — 2:30-4 pm

### Economics of Software Quality Assurance

Chairman: David S. Alberts, The MITRE Corp

Bringing together papers addressing the potential performance of quality assurance and control methods and techniques, ranging from automated tools to development and management approaches, session addresses the relationship between error rates and development costs, and examines the software life-cycle phases to assess the role and impact of quality assurance on each.

Session F6 — 4:15-5:45 pm

### Future Directions of Quality Assurance

Chairman: David S. Alberts, The MITRE Corp

Panel focuses on the relative effectiveness of current approaches being suggested for improving software quality and investigating the causes of poor quality. Approaches and subjects covered include selection and use of specific program structures and technologies, defect detection, allocation of development and test resources, and planning.

## Wednesday Morning

Session E7, 8 — 8:30-11:45 am

### Understanding and Using Microprocessors

Chairman: Reg P. Kaenel, AMF Inc

Session compares significant architectural differences of microprocessors, discusses tools that greatly facilitate development of microprocessor-based systems, outlines significant considerations associated with microprocessor software, and describes and demonstrates a major new use of microprocessors.

Session F7, 8 — 8:30-11:45 am

### Computer Performance Measurement

Chairman: Philip J. Kivit, FEDSIM/CA

Concepts and facilities, procedures, and reports that should be included in a good performance management system are discussed, forming the basis for a description of specific uses for such a PMS. An open panel discussion on performance management concludes the session.

Session G8 — 10:15-11:45 am

### Network Architecture

(Information not available at press time.)

Session H7, 8 — 8:30-11:45 am

### Computer-Aided Manufacturing and Design

Chairman: Thomas L. Boardman, University of Michigan

In discussing the trend toward convergence of computer-aided manufacturing and computer-aided design into a single unified discipline, papers present recent advances in the end-user to computer system interface in both areas. A panel discussion of trends toward unification of technologies is planned.

## Wednesday Afternoon

Session E9, 10 — 2:30-5:45 pm

### Microprocessor Systems

Chairman: Barry R. Borgerson, Sperry Research Center

Panel will examine both strengths and weaknesses of multimicroprocessor implementation of mainframe systems. To assure a cohesive discussion, each panelist will first answer a set of questions and, after committing himself, will accept questions from the floor.

Session F7 — 2:30-4 pm

### Measures of Performance

Chairman: Gerald Estrin, University of California

In the decade that serious attention has been paid to measuring computer system performance, enough experience has been gained to sift out the more meaningful measures of performance. Session discusses how the usage of current systems can be influenced, development of future measurement methods can be clarified, and design of future systems can be changed.

Session F8 — 4:15-5:45 pm

### Performance Information Systems

Chairman: Stephen T. Swift

(Information not available at press time.)

Session G9, 10 — 2:30-5:45 pm

### Network Operating Systems

Chairman: Stephen R. Kimbleton, University of Southern California

Papers structure objectives implicit in network operating system design, requirements dictated by these objectives, and current approaches toward partial achievement of these requirements. Emphasis is placed on discussion of mechanisms required for effective user interaction with a network environment.

## Thursday Morning

Session E11, 12 — 8:30-11:45 am

### Minis vs Maxis

Chairman: S. Ron Oliver, University of Kansas

As capabilities of computers and requirements of users have increased, the distinction between minis and maxis has been lost. This panel discusses four areas where growth and development have contributed to this blurring—communications and networks, microprogramming, operating systems, and programming languages—in an attempt to discover the direction mini applications will take in the next decade.

Session F11 — 8:30-10 am

### Issues in Computer Systems Performance

Chairman: Jeffrey P. Buzen, BGS Systems

Panel examines concepts, trends, and controversies that have emerged in the area of computer system performance. Topics to be considered include the relevance of performance evaluation theory to real-world problems, recent breakthroughs in performance evaluation theory, and new problems in the practical areas of computer performance evaluation.

Session F12 — 10:15-11:45 am

### Markov Performance Models

(Information not available at press time.)

Session G11, 12 — 8:30-11:45 am

### Network Measurements

Chairman: Susan Poh, The MITRE Corp

# LOGIC BOARD TESTING DOES NOT DEMAND SOFTWARE PROGRAMMERS, AND LOTS OF MONEY.

There is a foolish notion in logic board test circles that says, "Plan on spending all the budget you have, plus a lot more, to get logic board testing results."

What nonsense.

Why, that's as bad as the arguments for testing in the end product. Is there no middle ground? You know, a good testing system for a fair price.

Of course there is. And we built it.

It's our 3000 Series Logic Testers. The 3020A is a console for high-volume production applications. It comes complete with 128 pins for under $30,000*. The 3010A is a compact version for field service and low-volume production at less than half the price.

O.K. So why no high cost?

Most testers share one major shortcoming: the cost and complexity of programming. As logic boards become larger and more complex, test engineers anxiously reach for more computer power and more software.

It just isn't necessary.

The fact is that tediously developed, bit-by-bit sequences are now past history. Instead, we provide powerful groups of general-purpose sequences with various duty cycles and frequencies. Boards respond to them. Their mathematical qualities honor the constraints of your circuits and the laws of logic.

Specifically, the 3000 Series Testers have seven classes of signals. Over 350 unique bit streams and their complements are available to exercise the most complex boards.

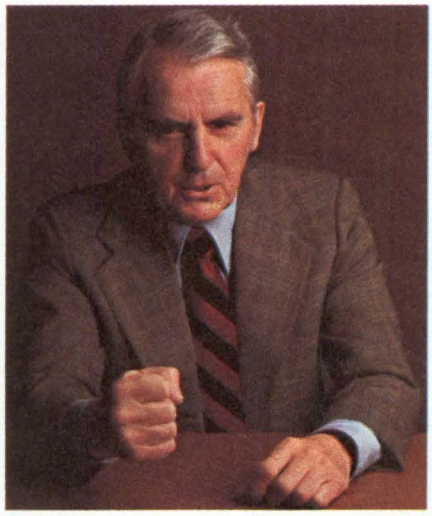
And, where a specific sequence is needed, it is easily added.

The test engineer doesn't program in the conventional sense. He simply develops a test plan which consists of selecting the appropriate stimulus algorithm for each input.

We've pre-programmed the CPU, simplified the peripherals, and eliminated 80% of the programming. That's what keeps the cost down.

The beautiful part is that test confidence ends up higher.

And fault isolation is just as practical as the price. It's hard to imagine



*"Prove it."*

any other tester making more common sense.

Test program assignments and editing are made on-line by pushbutton. Program debugging is simple. Whenever a pin number is entered, the sequence assignment is displayed. Sequences can be changed simply by depressing the appropriate pushbutton.

Again, there are no assemblers or compilers to fuss with. Highly comprehensive programs are completed in hours, not days or weeks.

And once the test program is entered into memory, you can record it easily on a handy little magnetic credit card that looks exactly like those credit cards in your wallet. The programmed card will function interchangeably with the production Model 3020A, or the field service 3010A.

Maybe we've made our point.

You can get a tester that offers four million tests per second, test sequences to 40 million words, and programmable logic levels without subsidizing a computer center and staff of programmers.

We'll prove it to you in dollars and cents.

Write and ask for "The Economics of Logic Board Testing." Everything you need is there to get you into logic board testing. Economically, for a change.

For data out today, dial (415) 965-0350.
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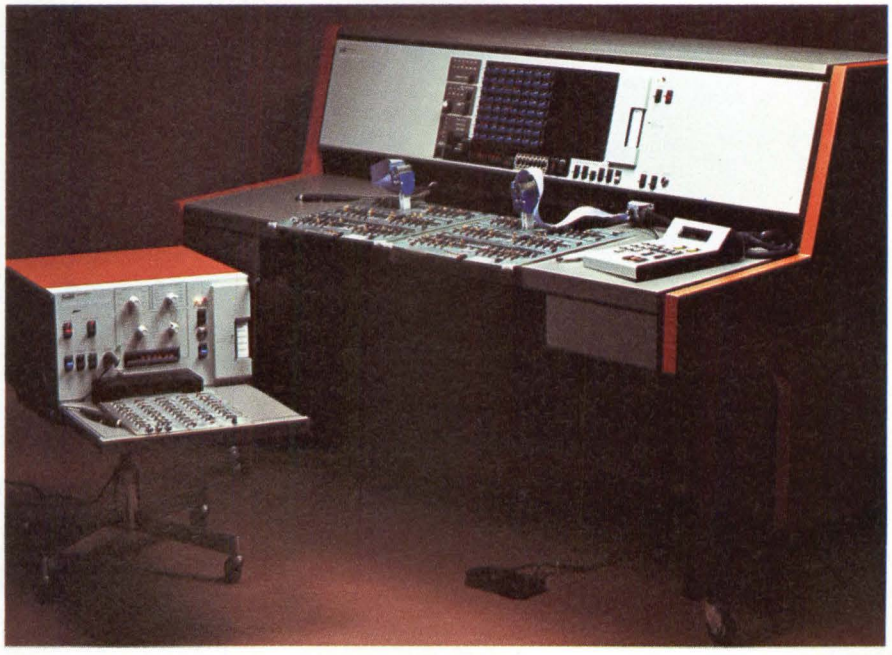

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CIRCLE 41 ON INQUIRY CARD

# Why more engineers than all other microcom

The 8080 system comes with four CPU options, twenty-five performance matched peripheral, I/O and memory components, and the industry's most useful software and hardware development systems. We've had the 8080 in volume production since April 1974 and there are now major second sources. These are just a few of the reasons why more engineers use the Intel 8080 system than all other microcomputers combined. Join them and you'll eliminate complex random logic, save design time, and get your products to market faster and at lower cost.

Start by replacing hundreds of TTL packages with the three LSI circuits in the MCS-80™ CPU Group—the 8080A CPU, 8224 Clock Generator and 8228 System Controller. Built into the Intel 8224 and 8228 are many of the extra functions that most designs require, such as TTL & MOS clocks, auxiliary timing functions and current sinking capability that keeps memory and I/O interfaces simple.

**MCS-80™ SYSTEM COMPONENTS**

| | Part No. | Description |
|---|---|---|
| **CPU GROUP** | 8080A | 8-bit Central Processor Unit, 2μs cycle |
| | 8224 | Clock Generator |
| | 8228 | System Controller |
| **CPU OPTIONS** | 8080A-1 | 1.3μs cycle |
| | 8080A-2 | 1.5μs cycle |
| | M8080A | 2 μsec cycle (−55 to +125°C) |
| **I/O** | 8212 | 8-bit I/O Port (15 mA drive) |
| | 8251 | Programmable Communication Interface |
| | 8255 | Programmable Peripheral Interface |
| **PERIPHERALS** | 8205 | 1 out of 8 Binary Decoder |
| | 8210 | Dynamic RAM Driver (8107B) |
| | 8214 | Priority Interrupt Control Unit |
| | 8216 | Bidirectional Bus Driver, Non-Inverting (50 mA) |
| | 8226 | Bidirectional Bus Driver, Inverting (50 mA) |
| | 8222 | Dynamic RAM Refresh Controller (8107B) |
| | 8253* | Programmable Interval Timer |
| | 8257* | Programmable DMA Controller |
| | 8259* | Programmable Interrupt Controller |
| **PROMs** | 8604 | 512 x 8, 100 ns |
| | 8702A | 256 x 8 Erasable, 1.3 μs |
| | 8704 | 512 x 8 Erasable, 450 ns |
| | 8708 | 1K x 8 Erasable, 450 ns |
| **ROMs** | 8302 | 256 x 8, 1μs |
| | 8308 | 1K x 8, 450 ns |
| | 8316A | 2K x 8, 850 ns |
| **RAMs** | 5101 | 256 x 4 Static CMOS, 650 ns |
| | 8101A-4 | 256 x 4 Static, 450 ns |
| | 8102A-6 | 1K x 1 Static, 650 ns |
| | 8102A-4 | 1K x 1 Static, 450 ns |
| | 8107B | 4K x 1 Dynamic, 420 ns |
| | 8111A-4 | 256 x 4 Static Common I/O, 450 ns |

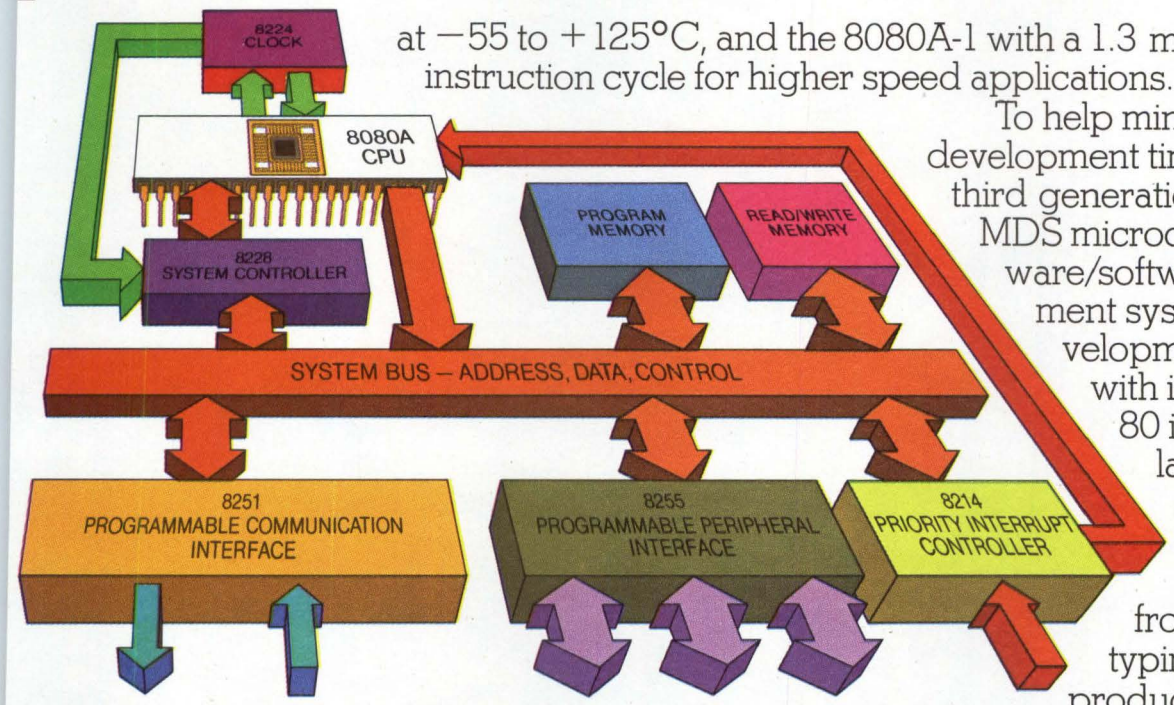
*Available 2nd quarter 1976.

A dozen I/O and peripheral circuits that attach directly to the system bus make it easy to add on peripheral subsystems. Five are programmable LSI devices. These operate under software control in numerous modes and can often replace up to 75—or more—TTL packages each. For example, the Intel 8251 Programmable Communication Interface provides virtually all serial data transmission protocols in use today, including IBM Bi-Sync. Or, for easy interface to printers, keyboards, displays and motor drives, use the 8255 Programmable Peripheral Interface. You can reorganize its 24 I/O lines with software as your needs change.

You have thirteen options in performance matched standard memory circuits, such as 16K ROMs, 8K erasable PROMs and 4K RAMs for high density at low cost, plus CMOS RAMs for lowest power.

You also get four CPU choices, including the M8080A for operation

# use the Intel 8080 system puters combined.




at −55 to +125°C, and the 8080A-1 with a 1.3 microsecond instruction cycle for higher speed applications.

To help minimize system development time use the third generation Intellec® MDS microcomputer hardware/software development system. This development system with its unique ICE-80 in-circuit emulator lets you simultaneously debug software and hardware, from initial prototyping right through production. The Intellec MDS is supported by six comprehensive software packages including a macro-assembler, ICE-80 interactive software driver and a diskette operating system.

In addition to the software packages in the development system, three cross product software packages are available on magnetic tape and on several time share networks. The Intel 8080 system is also supported by the industry's largest user's library, training courses and field applications assistance.

Start now with the new SDK-80 System Design Kit. It's a complete system for only $350 and includes: An 8080A CPU, Clock Generator, System Controller, Programmable Communications Interface and a Programmable Peripheral Interface. You also get two 1 of 8 binary decoders, 256 bytes of static RAM, two kilobytes of erasable PROM (with the system monitor supplied in one kilobyte), a PC board, clock crystal, connectors, other assembly parts, plus a user's manual and programming manuals.

To order the SDK-80 kit, contact our franchised distributors: Almac/Stroum, Component Specialties, Components Plus, Cramer, Elmar, Hamilton-Avnet, Industrial Components, Liberty, Pioneer, Sheridan or L.A. Varah.

For your free copy of the new 8080 system brochure and our Intellec MDS brochure, write: Intel Corporation, 3065 Bowers Ave., Santa Clara, Calif. 95051. For $5.00 we'll send you a copy of our new 236 page 8080 Microcomputer Systems User's Manual that includes complete hardware, software and interfacing data for all 8080 systems.

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CIRCLE 42 ON INQUIRY CARD

# Rolm launches its most compact computer

## The 1650: rugged, lightweight, ½ ATR size

The 1650 smashes the size barrier . . . especially in critical applications that have to meet Mil-E-5400 and Mil-E-16400 Environmental Specs.

It's about one-third the physical size of the Rolm 1602, yet has equivalent computing power through the use of the latest bipolar LSI technology. A microprogrammed 1650 CPU with an instruction set identical to the 1602 is packaged as a single folded-board module. The ½ ATR chassis also holds two 16K core memory modules (1 μsec cycle time) and a +28 Vdc power supply. Total weight — less than 30 pounds.

You can choose from a variety of cooling configurations including natural convection, external forced air or a Rolm-supplied blower. Single-sided access makes maintenance and service easy. Cap it off with optional floating point firmware, extensive I/O capabilities and complete software support . . . and you've got a compact computer system that can't be beat. Call (408) 257-6440, TWX 910-338-0247 or write ROLM Corp., 18922 Forge Drive, Cupertino, CA 95014. In Europe: 06181 15011, TWX 841-418-4170, 645 Hanau, Muehlstrasse 19, Germany.

ROLM CORPORATION

**The Rugged Computer Company**

CIRCLE 43 ON INQUIRY CARD

Session explores measurement facilities that are appropriate to satisfy the measurement goals in packet radio systems; new techniques for network user monitoring; and the performance of a new type of host interface; in an attempt to define goals and apply the measurements in the evolving technology of computer communications networks.

## Thursday Afternoon

Session E13, 14 — 2:30-5:45 pm

### Use of Minicomputers in Large Organizations

Chairman: Carol Brown, Winthrop, Brown

By exploring the use of small business computers and minis in large organizations, participants attempt to determine how a large company decides what kind of system to use, and the advantages and disadvantages of their decision. Also explored are software development, language alternatives, and system maintenance and documentation.

Session F13, 14 — 2:30-5:45 pm

### Computer Systems Auditability and Control

Chairman: William E. Perry, Institute of Internal Auditors

Discussing approaches and techniques for auditing and control based on the experience of organizations that are leaders in this area, the session focuses on auditors' concerns about advanced EDP systems, together with the skills and techniques needed to manage these systems.

Session G13, 14 — 2:30-5:45 pm

### Network Access Techniques

Chairman: Thomas N. Pyke, Jr, National Bureau of Standards

Problems of learning to use and then remembering awkward and lengthy procedures for remotely accessible network-based computer and information services are compounded when a user must access multiple network-based resources. Techniques are presented to alleviate this problem, including consideration of both functional and implementation considerations.

# Science and Technology

## Monday Afternoon

Session I2 — 4:15-5:45 pm

### Computer Structure

(Information not available at press time.)

Session J1 — 2:30-4 pm

### Software Sharing

Chairman: Margaret Butler

(Information not available at press time.)

Session J2 — 4:15-5:45 pm

### Transferability of Application Programs and Data Bases

Chairman: Alan G. Merten, University of Michigan

Presents practical and formal approaches to the inherent incompatibilities between dissimilar information systems hardware/software. By proper design of programming languages, job-control languages, and data structures and formats, the problems encountered in having to move an information system from one machine to another can be lessened considerably.

Session K1, 2 — 2:30-5:45 pm

### Computer Arithmetic and Numerical Methods

Chairman: Nathaniel Macon, The American University

Concerned with numerical methods which have immediate design implications, this session presents a design for a fast parallel multiplier, describes the advantages of using residue systems of modulus $2^b - 1$ in developing simple algorithms with high storage efficiency, and details an approach to interval arithmetic in terms of its applicability to symbolic and algebraic manipulation.

## Tuesday Morning

Session I3, 4 — 8:30-11:45 am

### High Level Language Computer Architecture

Chairman: Yaohan Chu, University of Maryland

High level language computer architecture is potentially capable of reducing software costs. This session presents some of the latest work in computer architectures for executing high level language programs.

Session J3, 4 — 8:30-11:45 am

### Structured Design

Chairman: Edward Yourdon, Yourdon, Inc

Although the ideas behind structured design have been known for several years, they have received widespread attention only in the last two years. Speakers present an overview of the subject, then discuss current research in some of its more important aspects, and present points of disagreement between their individual approaches to structured design.

Session K3 — 8:30-10 am

### Forecasting Technology

Chairman: James S. Ketchel, University of Puget Sound

Speakers review the state-of-the-art of technological forecasting methods, including Delphi, Bayesian statistics, and computer conferencing. They are joined by discussants for a critique of current applications.

Session L3, 4 — 8:30-11:45 am

### Inference and Speech Recognition and Understanding

Chairman: Iris Kameny

(Information not available at press time.)

## Tuesday Afternoon

Session I5 — 2:30-4 pm

### Multiprocessing

Chairman: Anne M. Gulick

(Information not available at press time.)

Session I6 — 4:15-5:45 pm

### Developing Application-Oriented Computer Architecture

Chairman: Tomlinson G. Rauscher, NCR Corp

Session addresses several techniques for improving a computer's problem-solving efficiency by developing computer architectures to support particular applications. Discussion of the techniques of specialized hardware design, microprogramming, and microprocessor-based systems cover the spectra of performance improvement, flexibility, and cost.

Session J5, 6 — 2:30-5:45 pm

### Software Engineering—What to Expect in the Next Decade

Chairman: Raymond T. Yeh, The University of Texas at Austin

To assess the impact of software engineering in the next decade, speakers discuss what is to be expected with compilers, hardware/software interaction, impact of software engineering on data processing, and automatic programming, and what effect software engineering will have on data base systems.

Session K5, 6 — 2:30-5:45 pm

### Implementation of Computerized Conferencing Systems

Chairman: Murray Turoff, New Jersey Institute of Technology

# Our incred

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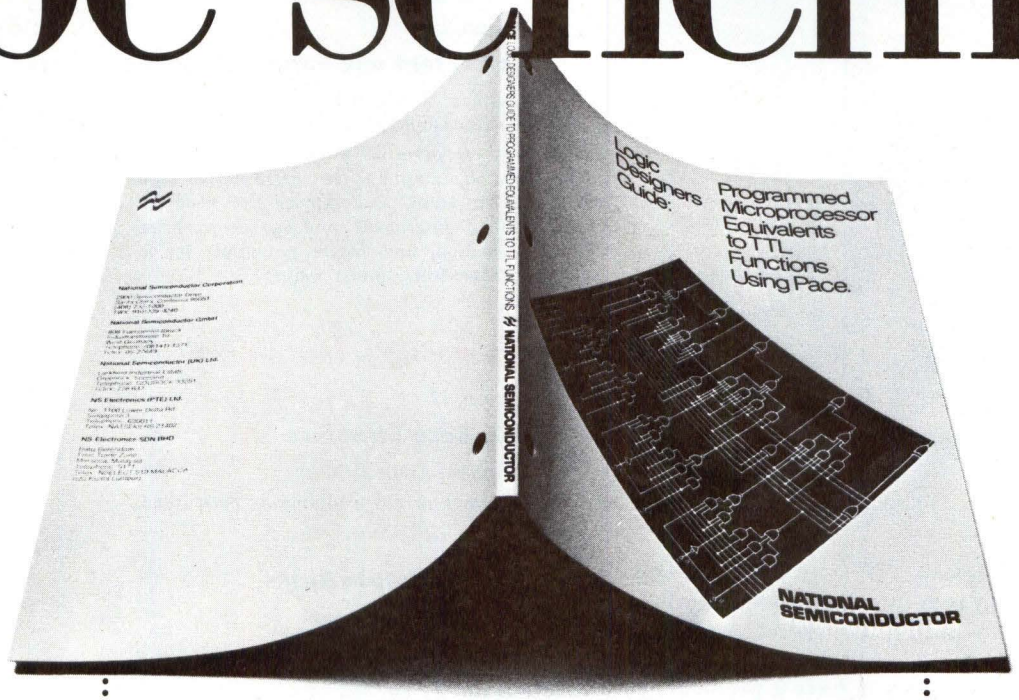


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I think this whole thing is a scheme to get *you* rich. But here's my $5.00, anyway.
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Company_____ Address_____

City_____ State_____ Zip_____

It's the "Logic Designer's Guide to Programmed Microprocessor Equivalents to TTL Functions Using Pace." And it's intended to help system designers make the transition from design in hardware to design in software. Thus saving your company a lot of money, which they will probably turn over to you. Or will they?

See us at NCC Booth 3220.

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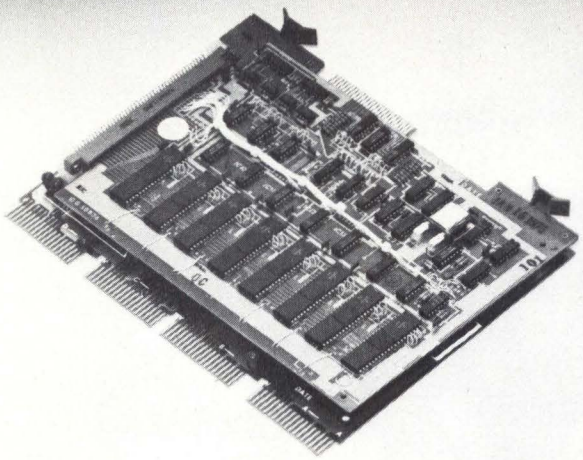
If Your Question Is...

# PDP-8 Data Collection At Less Than $300 Per Channel...



**Your answer is Telcon TDP-8. It's the only 8-channel serial data interface (or communication multiplexer, if you prefer) anywhere! And, it's protected by the industries only 36 month unconditional warranty. Should you have a problem... Telcon will provide a new board at no cost. Right from stock.**

**Plug compatible with your PDP-8, the high-density TDP-8 board features a temporary memory that buffers up to 64 words.**

**Multiple boards? Of course. Your system can be expanded to provide the most economical configuration for your data collection / distribution requirements.**

**Get in our communication loop. Call or write Telcon Industries. Direct your inquiries to Al Tonnessen... he will provide you with all the details. Our complete 3-ring catalog is available upon request.**

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in Canada contact:
ROR Associates Scarboro, Ontario
(416) 291-7121

Concerned with systems software design and implementation problems associated with computerized conferencing systems, panel session provides insight into the design characteristics, crucial problems encountered, and solution to other problems encountered in using FORTRAN approaches on the PDP-11/45 and Interdata 7/32, APL on a time-sharing service, and a systems programming language on the Interdata 7/32.

Session L5 2:30-4 pm

### Artificial Intelligence and Education

Chairman: Marvin Minsky and Seymour Papert, Artificial Intelligence Laboratory

Artificial intelligence indicates a new way of thinking about thinking and about learning and cognitive phenomena. Panel discusses ongoing research in enhancing the growth of intelligence in people, particularly children.

Session L6 4:15-5:45 pm

### The Present and Future of Mobile Robots

Chairman: Leonard Friedman, California Institute of Technology, Jet Propulsion Laboratory

Speakers describe work on an intelligent robot, under development to determine the feasibility of constructing a rover for exploring Mars, and explore the needs for a free-swimming, unmanned intelligent underwater explorer, robots for coal mine automation, and future potentials for a TV-vehicle system that navigates freely under water.

## Wednesday Morning

Session I7 8:30-10 am

### Data Base Structure

Chairman: Etelle Grinoch

(Information not available at press time.)

Session I8 10:15-11:45 am

### Relational Data Bases

Chairman: Susan Brewer

(Information not available at press time.)

Session J7, 8 8:30-11:45 am

### Programming Language Design

Chairman: Herbert Maisel, Goergetown University

Providing a forum for discussion of the design of programming languages that will serve to stimulate the development of languages needed by the computer community, session presents design considerations relating to hardware, software physics, programming methodology, and applications. These are discussed by a computer scientist, supervisor of programming, and an executive of a software development firm.

Session K7, 8 8:30-11:45 am

### Approximate Reasoning

Chairman: Enrique Ruspini

(Information not available at press time.)

## Wednesday Afternoon

Session I9, 10 2:30-5:45 pm

### Data Base Decisions

Chairman: John L. Berg, National Bureau of Standards

Panel composed of representatives of government agency, large centralized company, large decentralized company, and a medium-sized company describe their current status with respect to data base system implementation and answer previously prepared questions about the role that issues in auditing, standards, regulations, user experience, and technology played in making their decisions.

# Point by point, line by line:

# See why our lowest-cost Graphics package has no competition.

**Our 1024 X by 780 Y viewable points separate Graphics from mere graphing.** The price has never been lower. But Tektronix' new 4006-1 provides the same superior information capacity that has made us the company for all your graphics needs.

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**Graphics to gain. Nothing to lose.** Add the graphics extra at an everyday price: $2995 or $150 a month on a two year lease. Alphanumerics? Up to 2590 on screen characters. Plus a spectacular package that includes confirmed compatibility with most mainframes through proven interfaces and time-tested software packages. And expert maintenance that follows you all over the world.

**Plug-in peripherals standing by.** Like our 4631 Hard Copy Unit for up to four 4006-1's with 8½"x11" copies, or 4923 Digital Cartridge Tape Recorder for low-cost, off-line storage.

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Graphics $2995

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GENERAL ELECTRIC
TERMINET 340

# GE puts it on the line with a new family of TermiNet® line printers

## Four value-packed true line printers with real 90-340 lines per minute throughput at practical, low prices

Small size. Compact design. Modern styling. Quiet operation. Low prices.

At the same time this new space-saving family of GE TermiNet line printers is big on performance. They're big on throughput. Gives you a range of speeds from 90 lpm to 340 lpm, depending on the number of printable characters per line and the size (64 or 96) of the ASCII subset. And that's *real* throughput (see graph).

They're big on reliability backed by years of proven electronics and rotating belt technology. (Over 75,000 GE belt printers installed worldwide.) Big on versatility. 67% of the parts are common to TermiNet 300, 1200 and 120 printers. For resellers this means a minimal spare parts investment. For users it means improved service and less downtime due to a lack of spare parts. You can modify or upgrade quickly and at modest cost. They're big on interfaces. Serial and parallel, buffered and unbuffered.

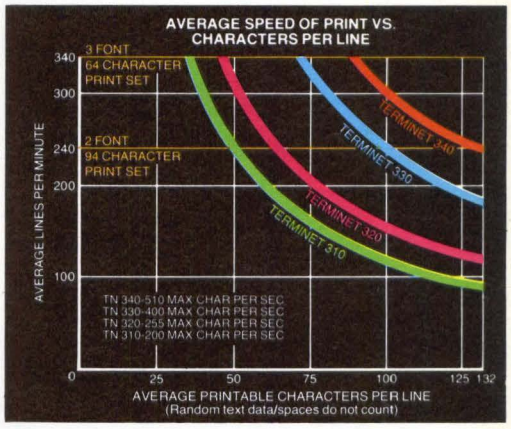
Big on quietness. They're a welcomed addition to any office or computer room. Big on value-packed features. Both front (recommended for multi-part forms) and rear loading. 132 columns. Original and 5 copies. A unique ribbon cartridge. With a life span of 50 million print characters. Operators can replace in less than a minute. Easily. Cleanly.

And, they're big on troubleshooting. 14 light emitting diodes (LED's) located on the outside of five printed circuit boards quickly indicate malfunctions. A test button on the control panel provides rapid checkout of printer action. Staggered or "ripple" test patterns print continuously as long as TEST is activated.

This big new family of TermiNet line printers are *true* line printers.

In fact, the only thing you'll find small about this new family of line printers is their size and price. In these days of spiraling costs, GE is putting it on the line with practical, low prices. From $3900 for the TermiNet 310 printer to $5130 for the TermiNet 340 printer (user quantity 1). That could well be the best cost/performance in line printers available today.

Let us prove it. Write General Electric Company, TermiNet 794-17, Waynesboro, VA 22980.




*The print rate for TermiNet line printers varies with the number of printable characters per line and the size of the ASCII subset used. Analysis of the typical rate curve shows that TermiNet 340 throughput for the 64 character ASCII subset is an average of 340 lines per minute when there are 90 or fewer characters printed on a line. This includes one line feed per line. Minimum throughput is 231.8 lines per minute when printing characters in all 132 columns, faster if there are spaces in the print line.*

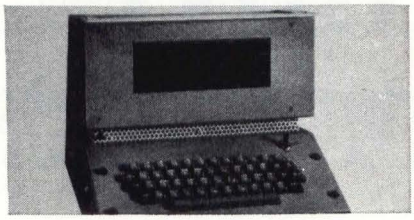
## For your special kind of needs-A special kind of printer

GENERAL ELECTRIC

CIRCLE 47 ON INQUIRY CARD

# NCC PRODUCTS

## DATA COMMUNICATIONS TERMINALS

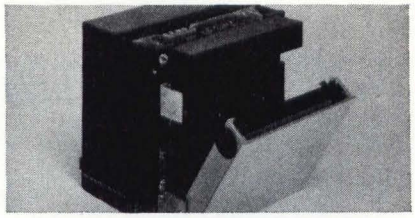


Three-unit family permits user to select device which meets specific requirements. Depending upon version selected, alphanumerics and graphics are possible at data rates up to 9600 baud. Plasma display provides easy-to-read characters with virtually no eye fatigue in 8-line x 42-char/line format. AG 90 is simple terminal for data communications featuring typewriter style keyboard. Primary application is in 2-way communications between individuals or between individual and computer. AG 91 is direct replacement for Teletype® terminal in many applications; AG 95 can be used for both data communications and graphics. Char set consists of full 64 char. For graphics applications, display matrix size is 80 x 256 points with resolution of 33 points/in. **Applications Group Inc,** PO Box 444, Maumee, OH 43537.

***See at Booth 2127***

Circle 330 on Inquiry Card

## DIGITAL CASSETTE TRANSPORT SYSTEM

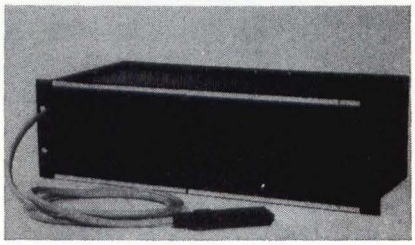


Small, lightweight CS-400 features Auto Sync™ decoding scheme which recovers previously lost data. Density of data handled is 800 bits/in. (other densities optional); data rate is 8000 baud at 10 in./s; data capacity is 5.76M bits (for a 300-ft tape). System contains CD 200 transport with following features: R/W speed 10 to 20 in./s, start time 10 to 25 ms, stop time 10 to 40 ms, start and stop distances 0.05 to 0.25 in. (all at 10 in./s); search speed 75 in./s avg, start time 60 to 100 ms, stop time 100 to 150 ms, start distance 2.5 to 5 in., stop distance 1.5 to 4.5 in.; search/rewind time (for 300-ft tape) 40 s; and speed accuracies ±5% short term, ±2% long term at 10 in./s. Operating modes are bidirectional search and R/W. **Braemar Computer Devices, Inc,** 11950 Twelfth Ave S, Burnsville, MN 55337.

***See at Booth 2745***

Circle 331 on Inquiry Card

## COMMUNICATIONS PATCHING SYSTEM

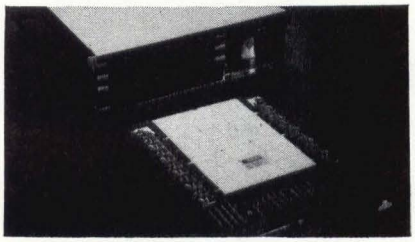


A modular system that allows the network controller to access data circuits at the RS-232/V.24 interface, Data-Patch is used to connect or "patch" modems, multiplexers, terminals, and computers where rapid service restoral or diagnostic testing is required. When using the monitor access patch position, test equipment may be inserted without interrupting the circuit or causing "hits." A typical system consists of a rackmounted assembly equipped with up to 16 patch modules and an adapter module. Inserting the patch cord in the computer position breaks all 24 leads of the circuit and provides access to these leads toward the computer. In modem position, access is gained to the circuit toward the modem; monitor position provides access without breaking the circuit. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

***See at Booth 1542***

Circle 332 on Inquiry Card

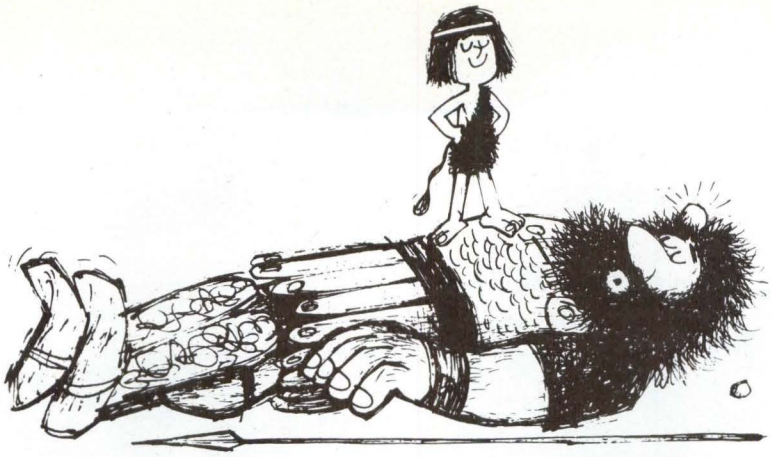
## 32K-WORD CORE MEMORY SYSTEM



A singleboard 3-wire, 3-D planar system organized as 32,768 words x 20 bits, Store/3220 features 750-ns cycle time and 300-ns access time. It is expandable to 131,072 words in a 5¼" chassis which includes a power supply option. Up to eight 32K modules can be daisy-chained to form a system with a capacity up to 262K x 20 in two 5¼" chassis. Core arrays and all electronics are housed in a module that measures 11.7 x 15.4 x 0.98". The low power 32K modules consume <100 W in worst-case conditions. Voltage requirements are 5 and ±15 Vdc. No temperature compensation is required for the power supply voltages for operation from 0 to 55°C. Complete, tested, and assembled systems are said to sell in OEM quantities for less than semiconductor memory components. **Dataproducts Corp,** 6219 De Soto Ave, Woodland Hills, CA 91364.

***See at Booth 1329***

Circle 333 on Inquiry Card



# The best floppy disk for your Intellec MDS*. iCOM or Intel?

## 16K vs 32K of RAM

At first glance it might seem that the best floppy disk system for the Intellec MDS-800* microcomputer would be Intel's own. Take another look. iCOM's Floppy Disk Operating System, FDOS-II, runs circles around Intel's. Take memory requirements for example. Intel's disk software is RAM resident, takes up 12K and leaves only 4K in the standard 16K system. Think how quickly you'll run out of label storage when running the assembler in only 4K. On the other hand, iCOM's FDOS-II is disk-resident and leaves nearly all of the 16K of RAM available for the assembler, etc.

## Save over $1000

The price tag for both floppy disk systems is about the same. Again, until you look more closely, You'll need a 32K RAM to support Intel's disk. With iCOM you can use the standard 16K RAM. You save about $1000. And less hardware too!

## Easier to use

iCOM makes your job easier. iCOM's commands are easier to use. File search is faster. We're IBM compatible. FDOS-II loads hex format directly. No conversion to binary required. Easier access to the file structure. Error messages in English. And iCOM is ICE-80 compatible.

## Just plug in to Intellec MDS*

iCOM is fully hardware & software compatible with the MDS-800. It can be installed in 5 minutes. It contains the most powerful FDOS available anywhere. Software is supplied on a ready to use diskette. You get features like variable length files, auto file create, open & close, multiple file merge & delete, auto disk repacking. Plus lots more.

## iCOM's track record

We've already delivered hundreds of floppy disk systems for microcomputers. We have plug-in interfaces to the 8080, 8008, Intellec* 8, MDS-800, PCS Micropac™ 80A, M6800 and others. With this track record, you can be sure you'll get service after the sale.

Contact iCOM today.
iCOM gives you the answers.

Intellec MDS*

iCOM FD 360-53

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# The AMI 6800 Micro

**We started by redesigning a CRT. And ended with the fastest, easiest way to build microcomputer systems.**

The AMI 6800 MDC architecture is so far ahead of the competition they'll have to change their whole development philosophy to catch up.

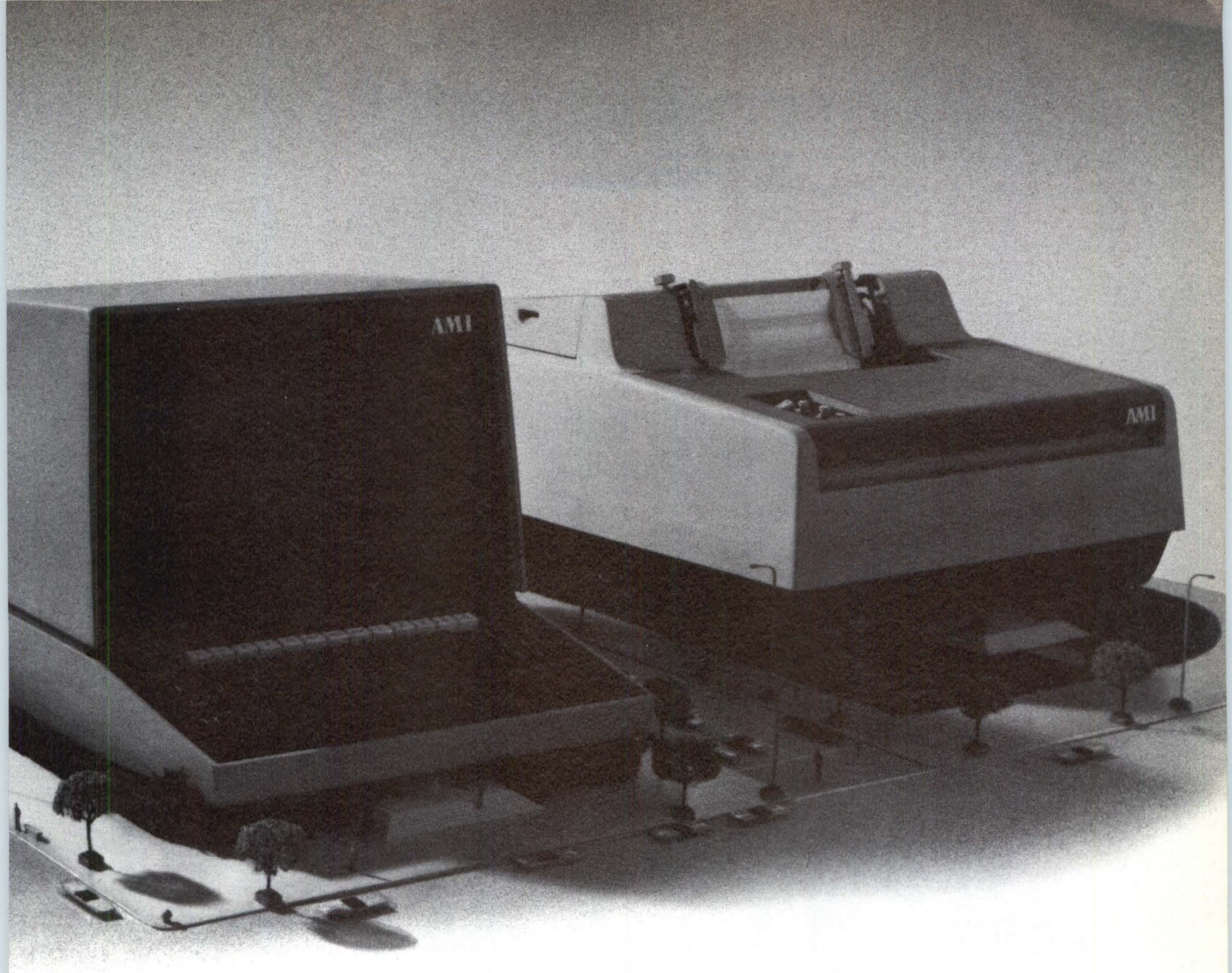
Unlike their multiple box approach, with lights and switches, our grand plan is centered around a very smart CRT, with full debug software.

There's a 6800 system in the terminal, so the processor you're working with is the same one you're developing. That cuts your learning time in half.

And you can forget about those long hassles with paper tape, front panels, teletype or cassettes. Put your hands on our keyboard and you never have to let go. You modify information instantaneously. Interrupt a program after every instruction, and get a complete snapshot of the state of the machine. Look at all the registers and change their values, simply by pressing a key. And you never have to translate addresses into binary to get information.

Our 6800 MDC not only cuts programming time in some cases from hours to minutes, it can also be configured as a test center for incoming 6800 parts. And it adapts easily to a powerful, one megabyte microcomputer for a variety of uses, such as inventory control.

The standard AMI Microcomputer Development Center consists of the 80 char. x 25 line CRT, the dual floppy disk with disk operating system, S6834 EPROM programmer,




# computer Development Center.

RS232 interface and 16K words of RAM memory. The many options will include a character printer, an in-circuit emulator so you can use the CRT like a front panel, EPROM and RAM memory modules.

So now the most flexible, easiest-to-use microprocessor family, the AMI 6800, has taken another giant step ahead of the others. The AMI 6800 Microcomputer Development Center can get you to the market faster, with a better product. Ask your AMI sales office, distributor or representative for our brochure. Or write to AMI, 3800 Homestead Road, Santa Clara, CA 95051. Then see how fast things develop.

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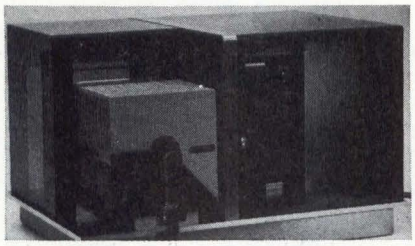
CIRCLE 49 ON INQUIRY CARD

# NCC PRODUCTS

## FLEXIBLE DISC SUBSYSTEM MASS MEMORY

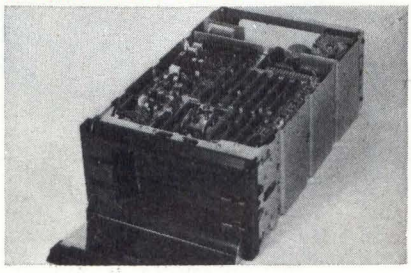


Up to 102.4M bytes of direct access memory for flexible disc drive subsystems are provided by the Random-Access Mini-Mass Memory (RAM³) system which automatically loads and unloads up to 32 IBM-equivalent diskettes from a magazine into GSI-110 double/single density flexible disc drive. Diskettes are selected randomly under control of the host system. Total time for selection and load of a diskette can be as low as 2.5 s (avg 3.9 s). Feeding mechanism assures precise diskette centering and careful media handling. Max data capacity of each system in IBM format is 7.7M data bytes; in unformatted double density on 32 diskettes, capacity is 25.6M bytes. Up to four systems can be daisy-chained to provide a total system capacity of 102.4M bytes. **General Systems International, Inc,** 1440 Allec St, Anaheim, CA 92805.

***See at Booth 3410***

Circle 334 on Inquiry Card

## FLEXIBLE DISC DRIVE

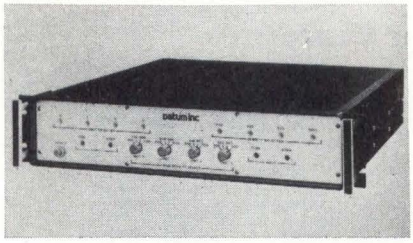


Said to be one of the most compact units on the market, the model 4231 is available in both single and dual versions and is IBM 3740 compatible, with a track-to-track access time of 4 ms max. Its loading mechanism gives exact disc positioning but assures gentle handling and full protection against disc damage; self-adjusting core moves perpendicular toward the axially fixed spindle holding disc such that disc is adjusted accurately at proper position. One loading, rotation, and access mechanism and a single drive electronic board are used in the dual version. Transfer rate is 250K bits/s; max bits/disc is 3.2M unformatted, 1.98M IBM-formatted. Recording mode is fm (double frequency). Diskette max times are 1.0-s start, 4-ms track-to-track, 20-ms settling, and 25-ms head load. **Facit-Addo, Inc,** 66 Field Point Rd, Greenwich, CT 06830.

***See at Booth 1615***

Circle 335 on Inquiry Card

## FOUR-DENSITY MAG TAPE CONTROLLER



Interface for all operating, formatting, and control signals is provided between industry-standard drives and minicomputers of 11 companies by the model 5191 controller. Called Quad-Density because it handles four separate data densities with a single controller, the unit has individually driven ports for up to four transports in any combination of 7 or 9 tracks, NRZ or PE encoded data density from 200 to 1600 bits/in., and tape speed from 12.5 to 200 in./s. It has separate, parallel outputs for each drive, which allow a mix of different tapes on one formatter. The NRZ section generates and checks VRC, LRC, and CRC error detecting codes; the PE section contains logic for generating preamble, postamble, file marks, and I/D bursts. **Datum, Inc, Peripheral Products Div,** 1363 S State College Blvd, Anaheim, CA 92806.

***See at Booth 2741***

Circle 336 on Inquiry Card

## DUAL MAGNETIC TAPE MICROPROCESSOR PERIPHERAL

Designed to interface with any MPU system, the model 31-001 features an internal MPU which controls operation of two tape transports, one for writing and one for reading. Asynchronous interface provides full data buffering and is independent of tape read or write speeds. Peripheral can be used as a complete program development system for the Intel 8080 and as an incremental recorder for nonvolatile data storage with any MPU that has an 8-bit, bidirectional data bus. Continuous-loop wafer cartridges for data storage are available in 5-ft tape increments from 5 to 50 ft. A 50-ft wafer stores a max of 48K bytes. Prewritten wafers containing monitor, editor, and assembler in Intel 8080 object code and requiring 4K RAM for execution are available. **Micro Communications Corp,** 80 Bacon St, Waltham, MA 02154.

***See at Booth 1829***

Circle 337 on Inquiry Card

# When you choose DATUM mag tape or disc systems You get performance... but We get system responsibility!

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Off-the-shelf controllers for these computers:

**Computer Automation** Alpha LSI • **Data General** Nova and Eclipse • **DCC** 112, 116 • **DEC** PDP-8, -8e, -8i, -8l, -9, -9l, 11, 12, 15 • **Harris Communications** Slash 4, Slash 7 (Datacraft) • **HP** 21MX, 2100, 2114, 2116 • **Honeywell** 316, 416, 516 • **IBM** 1130 • **Interdata** 716, 832 • **Lockheed** SUE • **Micro Systems** 810 • **Rolm** 1602, 1603 • **Varian** 620i, 620l, 620f, V73, V74, V75, V76.

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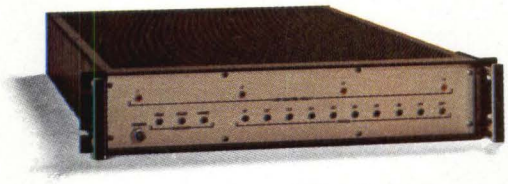

Series 4091 Disk Controller

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expertise given by cooperating in-house divisions that design and build custom data acquisition systems and sophisticated micro-programmed minicomputers.

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(UC) EXPANDED (LC) CHARACTERS

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Standard character sets included are in ASCII or 5 Level Code. TTS (6 Level) Code available at extra cost.

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STANDARD LINE INTERFACES: EIA RS 232C. DC Loop. MIL 188C.

## THESE ADDED SMALL-COST OPTIONS MAKE THIS OUTSTANDING PRINTER A SELF-STANDING R/O TERMINAL:

BUILT-IN MODEMS WITH 103 OR 108 OR 113 COMPATABILITY.

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A 20 CHARACTER ANSWER BACK.

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NATIONAL OR SPECIAL CHARACTER SETS - INCLUDING LOWER CASE DESCENDERS.

IN A COMPACT; COMPLETELY SELF-CONTAINED UNIT - 12-5/8" WIDE; 17-3/8" DEEP; AND 5" HIGH (WITHOUT PAPER ROLL); 25 LBS.

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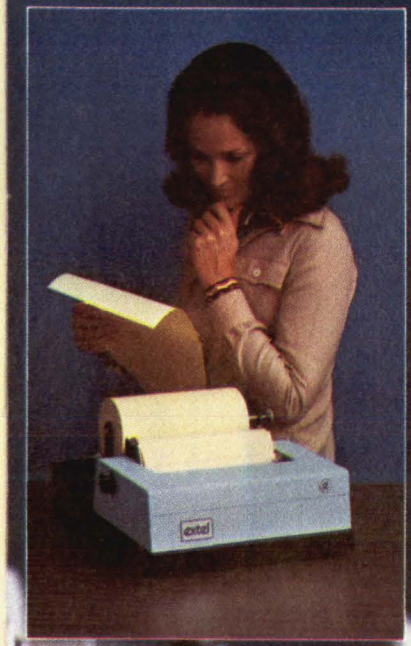


**EXTEL CORPORATION**
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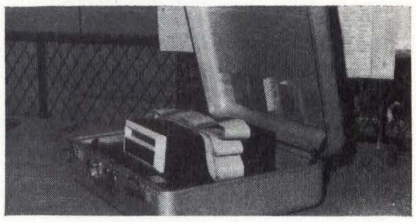
**CIRCLE 51 ON INQUIRY CARD**

# NCC PRODUCTS

## PORTABLE PROGRAM LOADER/LOGGER



Model 2710 offers performance approaching ½" mag tape with 48K bits/s transfer. 3M data cartridge medium, guaranteed at 5K passes, provides an order of magnitude improvement in reliability compared to cassette systems. Data loss through media failure is virtually eliminated. For program loading applications, the data transfer rate is 6K bytes/s. Built-in CRCC provides data integrity. Three minicomputer interfaces are offered as std; others are optionally available. For diagnostic applications, a typ test program can be loaded with only a 10-instruction bootstrap and operates at 600 times the rate of paper tape. For data logging applications, the unit will operate with field-available voltages. **North Atlantic Industries, Inc, Qantex Div,** 200 Terminal Dr, Plainview, NY 11803.

***See at Booth 2831***

Circle 338 on Inquiry Card

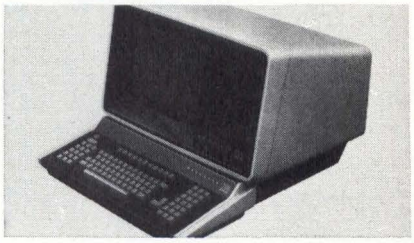
## DUAL HEAD SERIAL PRINTER

Matrix printhead on the model 5703 is rated at 150M char of continuous use without special adjustment except to coil after printing 50M char. Printhead consists of seven vertical printwires and solenoids. Operating noise level is <65 dB. Print speed is 330 char/s, 80 lines/min. on a 132-char line. Max 132 char for one line are stored in buffer memory composed of four shift registers in 132 x 2 format. Print format is 6 lines/in., 10 char/in. Data transmitting speed is 75K char/s. Data input form is parallel. Print matrix is 7 x 9. Input code is std ASCII, 64 char; special code and char sets are available. Paper slew is 45 ms/line. Temp ranges are 5 to 40°C operating, −20 to 60°C storage. Dimensions are 22 x 29.5 x 11.8" (56 x 75.5 x 30 cm); weight is 121 lb (55 kg). **Tokyo Juki Industrial Co, Ltd,** Kabuki-cho, Shinjuku-ku, Tokyo, Japan.

***See at Booth 3240***

Circle 339 on Inquiry Card

## PROGRAMMABLE INTELLIGENT TERMINAL

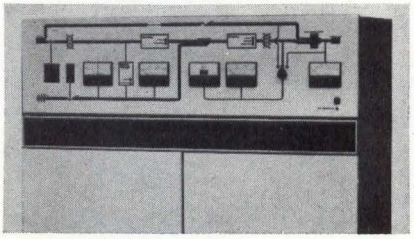


System 700 has full 12-bit minicomputer capability with up to 64K words of program and data storage in p/ROM and RAM. DEC PDP-8/E type architecture permits assembly language programming. Up to 71 program controlled function keys and 12 status lights on a 126-key keyboard simplify complex data processing operations. Data are preprocessed at the terminal, eliminating most input errors and need for lengthy verification. The unit communicates in virtually any format, protocol, and line discipline, at speeds up to 13,500 baud serial or 20,000 baud parallel. Std display format on 15" diagonal screen is 80 char x 24 lines (128 x 32 optional). Std char are 7 x 8 dot matrix; 7 x 9, 8 x 10, 8 x 12, 10 x 15, 12 x 15, and 10 x 23 are options. **Megadata Computer and Communications Corp,** 35 Orville Dr, Bohemia, NY 11716.

***See at Booth 1005***

Circle 340 on Inquiry Card

## UNINTERRUPTIBLE POWER SYSTEMS

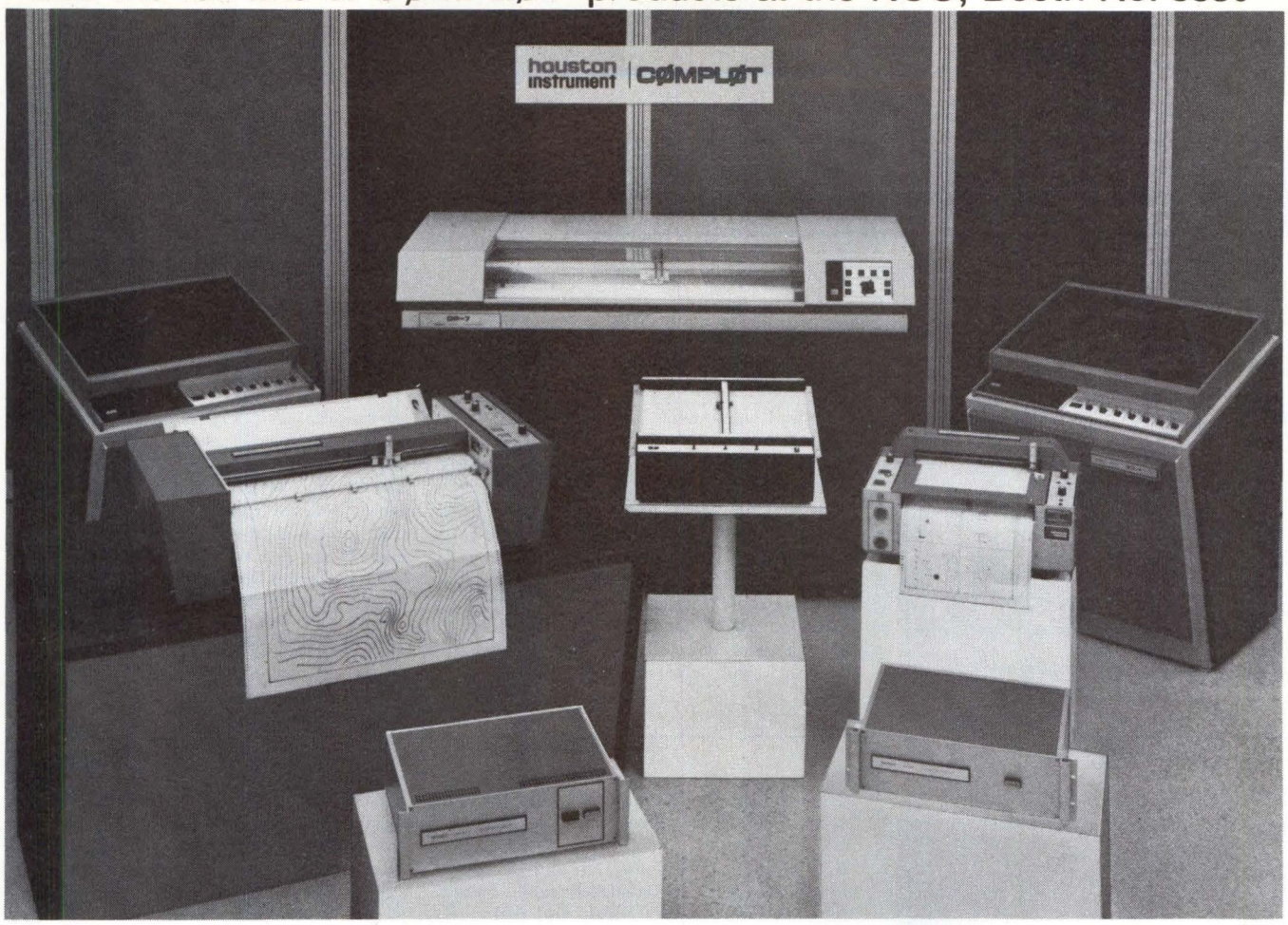


81000 series UPS protects critical loads against ac power line disturbances and loss of commercial ac power. Loads are protected from instantaneous and subcycle power losses as well as from longer term power outages. Features include fast battery recharge and excellent noise suppression. Std models have 1$\phi$ outputs and are available in 3-, 5-, 10-, and 15-kVA ratings. With the commercial ac line present, the UPS protects the load from brownouts and short term transients or interruptions resulting from switching in the transmission system, clearing of line faults, starting of loads, or lightning strikes. When the line is not present, the UPS continues to supply the load from power stored in the system's batteries. The unit will deliver 150% of rated power for 10 s and 125% for 10 min. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.

***See at Booth 1036***

Circle 341 on Inquiry Card

See the full line of CØMPLØT® products at the NCC, Booth No. 3330




## NEW! PTC-5 Universal Time Sharing Plotter Controller

- Drives any CØMPLØT Digital Plotter
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- Firmware character and vector generation
- Circular buffering system
- Low cost

## NEW! DP-1H Digital Plotter

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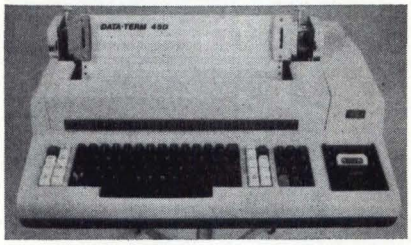
# NCC PRODUCTS

## DATA COMMUNICATIONS TERMINALS



Standard equipment on every Data-Term includes impact printing, 132-col print width, portability (weighs <45 lb), high speed (up to 45 char/s is std with 60, 120, and 180 char/s optional), IBM Selectric™ configured keyboard with tactile feedback, 30-key alphanumeric "gear-shifted" keypad, horizontal tabs, vertical tabs, variable forms control, and a user programmable char set. Options include an APL/ASCII char set, IBM 2740-41 compatibility, and company's Intercette® micro-cassette. For expanded capability an additional micro-cassette unit may be added. Terminal's 8080 microprocessor memory may be expanded up to 65K bytes, thereby allowing the user to run numerous high level software packages which may be loaded into the terminal via the tape device. **Intertec Data Systems Corp,** 1851 Interstate 85 S, Charlotte, NC 28208.

***See at Booth 2807***

Circle 342 on Inquiry Card

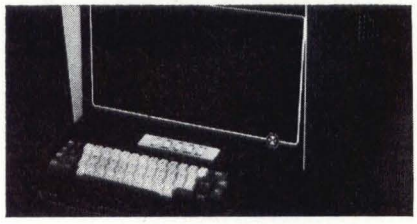
## BRIEFCASE CRT TERMINAL

TeleComputer™ II features switch-selectable 40- or 80-char line length (1280-char display), built-in acoustic coupler, EIA RS-232 and current-loop (20- and 60-mA) interfaces, and 15 switch-selectable baud rates from 50 to 9600. Half and full duplex, page and roll mode, and local and remote switch are std; blinking character or field, parity select, "here is" coding, cursor addressability, protected formats, and batch transmit are optional. Maximum installation flexibility is provided for interfacing up to 10 video monitors of any size, and attaching through dual RS-232 interfaces to peripherals. Printer output is std feature. With built-in acoustic coupler, 5" CRT, and case, weight is 23 lb; full unit, with case, measures 6.25 x 15.5 x 20.75". **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.

***See at Booth 2014***

Circle 343 on Inquiry Card

## CURSOR CONTROL AND X-Y ADDRESSABLE CRT

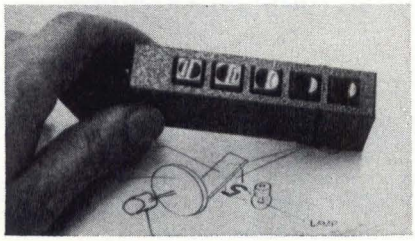


Cursor-addressable model 3811 Teleray is characterized by switchable wide/narrow character display, plug-in ICs throughout, RS-232 and current-loop interfaces, and silent operation (no fan). The cursor is fully controllable from keyboard or computer. X-Y addressing is accomplished by ESC sequences, in which a series of four characters instantly moves the cursor anywhere on its 12" screen. All interface codes (CR, LF, parity) and choice of 15 speeds to 9600 baud are set by DIP switches. The unit operates in scroll or page mode, offers erase to end-of-line and screen erase, and displays a nondistracting, low brightness blinking block cursor. It measures 18 x 14 x 24", weighs 50 lb, consumes only 80 W, and has a full-screen anti-reflective faceplate. **Research Inc,** Box 24064, Minneapolis, MN 55424.

***See at Booth 2022***

Circle 344 on Inquiry Card

## HAND-HELD OCR WAND



Electronic eye in model KT3 Datawand allows reading rates of 100 char/s, including alphanumerics, in eight printed fonts and hand print. Buttons on the back duplicate keys on the keyboard, permitting such operations as tab, return, backspace, and caps, and selection of different fonts. In operation, wand is placed in contact with paper or other surface on which data are printed, then moved across data line at speeds to 10 in./s. Small "displacement wheel" on underside of wand steps off wand travel, allowing for different or uneven scanning speeds. When wand encounters degraded printing, or incorrect type style, its associated recognition circuitry emits an audible beep to alert the operator. OCR converts human-readable data into computer-recognizable codes automatically, **Key Tronic Corp,** Bldg 14, Spokane Industrial Park, Spokane, WA 99216.

***See at Booth 1706***

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# MINICOMPUTER MEMORY... Buy 1/2...Get 1/2 Free

You get up to twice as much memory for your money from EMM. It's like only paying for half, and getting the other half free. And that's just one of the reasons why it pays to do business with the memory experts. You get the choice of core or semiconductor, the latest advances in memory system design, and a full one-year warranty.

Come to EMM for add-in/add-on memory for most major mini-computers — DEC, Data General, Interdata, General Automation and others. You'll get more bits for your buck — and proven performance too — when you deal directly with the memory experts at EMM.

**TYPICAL PRICES***

| Minicomputer Model | Capacity | Minicomputer Company Price | EMM Price |
|---|---|---|---|
| Data General Nova 1200 | 8K Words | $2,000 | $ 860 |
| | 16K Words | $3,500 | $ 1,230 |
| | 32K Words | Not Avail. | $ 2,400 |
| Interdata 7/16, 7/32 | 32K Bytes | $5,000 | $ 2,000 |
| General Automation SPC-16 | 16K Words | $4,600 | $ 2,000 |
| DEC PDP-11 Core Add-On Unibus | 32K Words | $9,800 | $ 5,190 |
| DEC PDP-11 NMOS Add-On Fast Bus | 64K Words | Not Avail. | $19,000 |
| DEC PDP-11 Core Add-In | 16K Words | $4,500 | $ 1,825 |
| DEC LSI-11 Add-In | 16K Words | Not Avail. | $ 1,590 |

*All prices for single unit quantities.

## Check The Green Tag Values At Your Local EMM Minicomputer Memory Market:

**BFA CORPORATION**

| | |
|---|---|
| Scottsdale, Arizona | (602) 946-4215 |
| Las Cruces, New Mexico | (505) 523-0601 |
| Denver, Colorado | (303) 344-3800 |
| Albuquerque, New Mexico | (505) 292-1212 |
| Salt Lake City, Utah | (801) 466-6522 |

**ELECTRONIC MARKETING SPECIALISTS**

| | |
|---|---|
| Sherman Oaks, California | (213) 990-4244 |
| San Diego, California | (714) 566-1000 |
| Sunnyvale, California | (408) 245-9291 |

**HARVEY J. KRASNER ASSOC., INC.**

| | |
|---|---|
| Great Neck, New York | (516) 487-0690 |

**TECHNOLOGY MARKETING, INC.**

| | |
|---|---|
| Dallas, Texas | (214) 358-1307 |
| Houston, Texas | (713) 461-0038 |

**VICTOR ASSOCIATES**

| | |
|---|---|
| Framingham, Massachusetts | (617) 879-5710 |
| Manchester, Connecticut | (203) 646-6448 |
| | 647-9203 |

**CANTEC**

| | |
|---|---|
| Ottawa, Ontario, Canada | (613) 225-0363 |

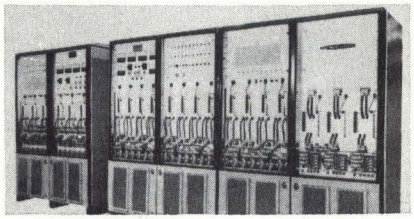
**EMM ELECTRONIC MEMORIES**
***COMMERCIAL MEMORY PRODUCTS***

A Division of
Electronic Memories & Magnetics Corp.
12621 Chadron Avenue
Hawthorne, California 90250
(213) 644-9881

CIRCLE 53 ON INQUIRY CARD

# NCC PRODUCTS

## UNINTERRUPTIBLE AC POWER SUPPLY SYSTEM



A 400-kW UPS added to the SuperGuardian line uses a digitally-controlled stepped wave inverter with subcycle current control to provide "no-break" power to real-time computers and other critical loads. Transient recovery is accomplished within 50 ms for complete recovery to within ±1% band. Variations in computer load requirements, such as those caused by in-rush loads and faults, are corrected every 700 μs. When an electrical fault occurs, protection is provided against crashdown by feeding max available fault clearing current, instantaneously supplied by the continuously monitored subcycle current control in conjunction with the all-digital logic control. **Exide Power Systems Div, ESB Inc,** Rising Sun & Adams Aves, Philadelphia, PA 19120.

***See at Booth 1100***

Circle 346 on Inquiry Card

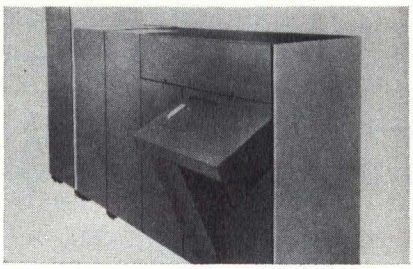
## DIGITAL RECORDER

Unireel concept combines two products: a single reel mag tape package and a companion small, self-threading tape drive. The package is a conventional reel with an enclosing, protective leader. Model 150 package is 2⅛" in dia, weighs 1 oz, and contains approximately 140K bytes of information. Reels are loaded into the tape drive with a straight line "slot loading" motion. The drive automatically threads the tape onto a captive takeup reel and positions the tape at BOT. The IC 1300 has an avg transfer rate of 1.2K bytes/s; tape speed is 12 in./s forward and reverse with an optional search speed of 60 in./s. Recording format is serial biphase with a velocity tolerant decoding technique. Control logic protects against inadvertent reel removal and tape run-off, and handles power interruptions. **Interdyne,** 14761 Califa St, Van Nuys, CA 91411.

***See at Booth 2635***

Circle 347 on Inquiry Card

## LASER MASS MEMORY



System 190 permanently records and stores up to 1T bits of user data. It can interface to a host computer providing online mass storage or operate in a standalone mode. Recording media are Data Strips™, each of which contains over 1.6G user bits and has an estimated shelf life in excess of 50 yr. Data are recorded by using a precisely focused laser beam to form patterns in the surface of the medium. Basic system consists of a 191 control unit, a 192 R/W data storage unit, and a 191-4 channel I/O control unit. A single storage unit provides online data storage capacity of 128G bits. Since media are removable, the total data storage capacity is virtually unlimited. A single control unit can handle up to eight read/write or read-only units in any combination. **Precision Instrument Co,** 2323 Owen St, Santa Clara, CA 95051.

***See at Booth 2021***

Circle 348 on Inquiry Card

## BAR CODE READER

Model 9106 reads bar code tags or labels for subsequent data transmission or input to a minicomputer or data terminal system. Reader includes Ruby Wand® lightpen and presently reads 2-out-of-5 code and the company's Code 39, an alphanumeric bar code that features additional human-readable text in the area immediately above the code. It is switch programmable to read min lengths from 1 to 16 char. Bar code can be bidirectionally scanned at 3 to 25 in./s with the hand held lightpen. An audio signal confirms that a label has been read correctly. The unit's communications interface is compatible with asynchronous bit serial rates of 110, 150, 300, 600, 1200, or 2400 baud. Optional baud rates are available up to 9600. Parity checking and stop bits are switch programmable. **Interface Mechanisms, Inc,** 5503-232nd St S W, Mountlake Terrace, WA 98043.

***See at Booth 1022***

Circle 349 on Inquiry Card

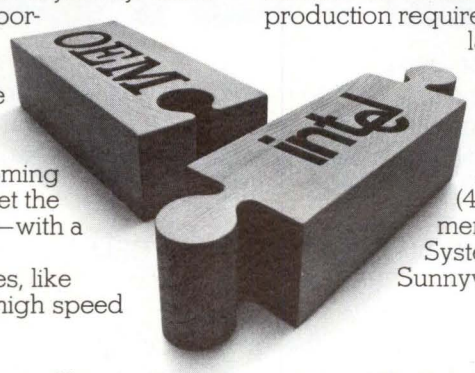
# Who is the largest supplier of OEM semiconductor memory systems?

If you're in the computer or systems business you probably already know that it's Intel. You also know the importance of getting your systems out of engineering and into the marketplace. Nothing happens until you get an order.

If the semiconductor memory part of your system is delaying things or if you have two important memory projects but only one design team, then you should talk to us. Chances are we may already have just the memory system you need. That's why more and more computer companies and system houses are coming to Intel for help. We're helping them get the competitive jump in the marketplace—with a memory as good as their own.

We're talking about big memories, like 8 megabytes in a single frame. And high speed memories as fast as 150 ns access time, 300 ns cycle time. And memories to interface with your TTL or ECL logic, with or without error correction.

We're already shipping over 50 multi-megabit systems, plus thousands of single board memories every month. That means we'll be able to support your volume production requirements. And because we're the world's largest manufacturer of both semiconductor memory systems and components you get the best possible price/performance package.




It's easy to get started. Call Gary Andersen, OEM Marketing Manager, (408) 734-8102 Ext. 451, or send your memory specifications to Intel Memory Systems, 1302 N. Mathilda Avenue, Sunnyvale, California 94086.

intel memory systems
A DIVISION OF INTEL CORPORATION

CIRCLE 54 ON INQUIRY CARD

# What large OEM's need today:

# a short cut into microcomputing

**...that's easier to get, easier to use, easier to expand at will.**

You've got it. With the new LSI member of our Solution Series. The GA-16/110. A full-fledged 16-bit computer on a single plug-in board. Specifically designed for dedicated computer applications, such as remote data collection and control, terminals, and communications concentrators.

Dollar for dollar, spec for spec: the fastest, most flexible, lowest cost microcomputer *with* full software support and dozens of I/O controllers, now available off the shelf.

Performance twice as fast as the nearest competitor. Powerful repertoire of 120 basic instructions. Memory expansion from 512 words to 64K words. And this "load-and-go" worker, the GA-16/110 system, shares software and I/O compatibility with all Solution Series family members, right up to the GA-16/440 super mini with 2 mega-bytes of memory.

Terrific price/performance tradeoff too. From $474 for a fully-operational 512-word computer. To $1692 for a complete 8K packaged system. (OEM quantities of 200.)

Say you need still more: our GA-16/220 will do the job. By adding more I/O capability, more interactive controls, more displays, you get full minicomputer performance and features at microcomputer prices.

And the rich GA-16/220 software includes: batch operating systems; foreground/background real-time operating systems; indexed file management systems. FORTRAN IV; COBOL; multi-user BASIC; macro assembler; and a lot more. *All* are off-the-shelf software, currently in the field working in applications such as yours.

Compared to any computer family in production today, the Solution Series meets your requirements with the largest variety of configurations and range of performance, backed by the broadest software and I/O support. Hands down, the shortest distance to your microcomputer product is the new Solution Series family from a real solution systems company—General Automation.

For product info, write General Automation, 1055 South East Street, Anaheim, California 92805. (714) 778-4800.

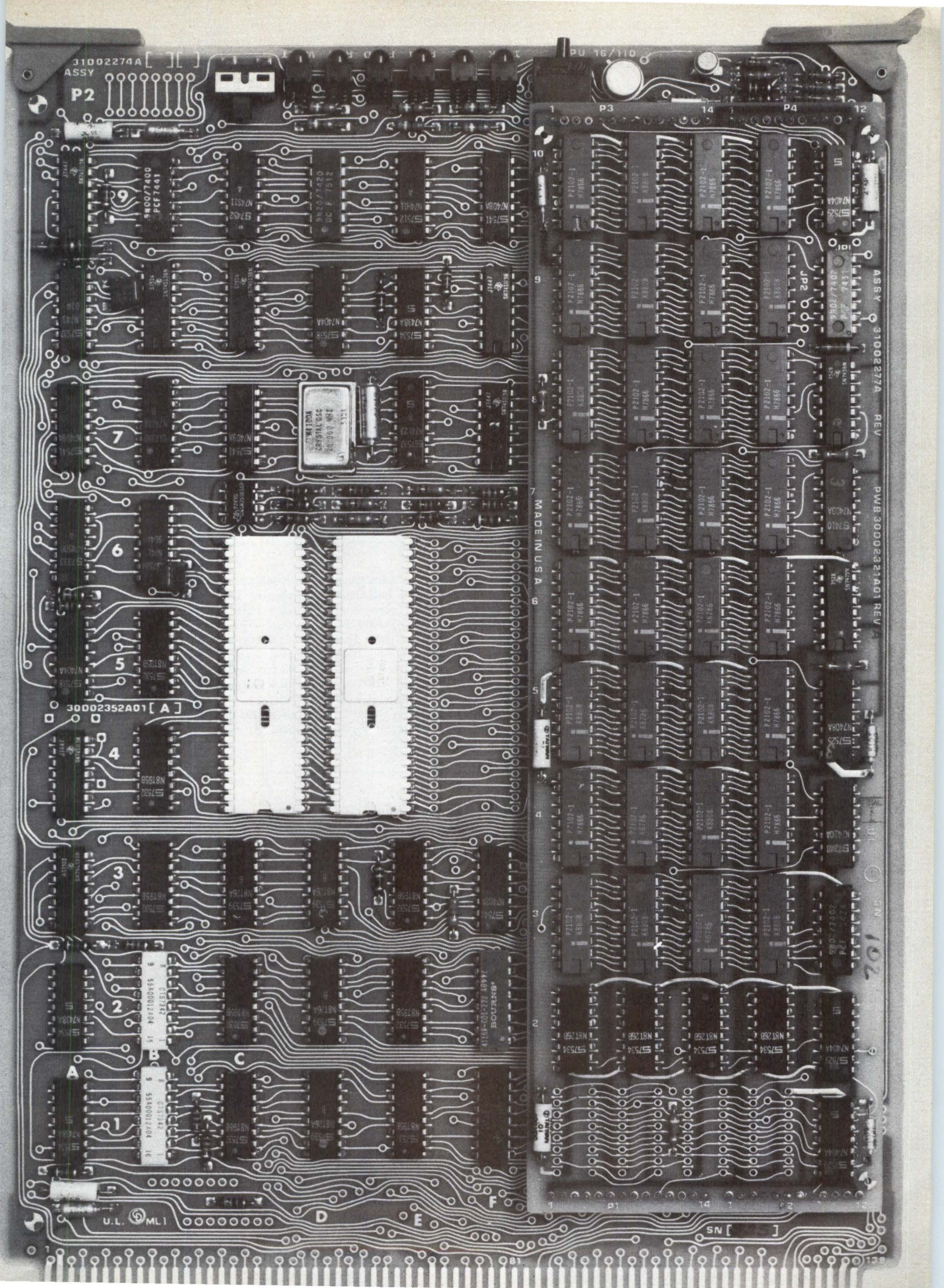
Also General Automation, Paris, France and G.A. Computer Ltd., Ontario, Canada.

# GENERAL AUTOMATION

**SEE GENERAL AUTOMATION AT NCC, BOOTH 2501.**

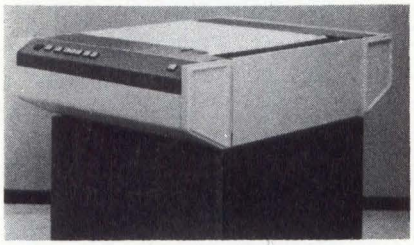


**CIRCLE 55 ON INQUIRY CARD**


31002274A
ASSY
P2
P3
P4
P1
P2
30002352A01 [ A ]
31002277A REV
PWB30002321A01 REV
MADE IN U.S.A.
SN 102
SN [ ]
U.L.
ML1
BOURNS
CRYSTAL OSC

# NCC PRODUCTS

## ELECTROSTATIC PRINTERS



Choice of 22 or 24" paper width, vertical plotting speed of 1 or 2 in./s, resolution of 100 or 200 dots/in., char generator, and simultaneous print/plot option for display of captions, legends, and other alphanumeric data while plotting are offered in four models of printers. Plotting a raster scan of data at a time, they can shade, tone, draw variable line widths, and draw a continuous plot of up to 500 ft in length. Shaft encoder and servomotor drive maintain an accumulated vertical accuracy of 0.2% or 15 mils (whichever is greater) while operating at max speed. Shaft encoder determines timing and writing location; the servomotor drives the paper. Servo paper drive gradually decelerates and stops paper movement without overshooting. **Versatec,** 2805 Bowers Ave, Santa Clara, CA 95051.

***See at Booth 2720***

Circle 350 on Inquiry Card

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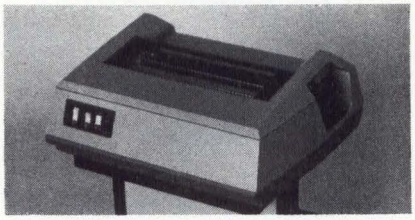
## DOT MATRIX SERIAL PRINTER



In addition to operational features such as 120-char/s operation, 9 x 7 half-space matrix printing, and control electronics based on an 8-bit MPU, the T-1200 includes an acoustically designed cover that provides a noise signature of <55 dBA under NC45 profile. It also allows the option of a 2-channel VFU reader that functions only when initially loading a VFU tape. Information on the tape is stored in RAM and retrieved for subsequent forms positioning operations. Power is automatically removed from the photo-optic reader until it is required to load a new format. Space is reserved on the control electronics card for 2K bytes of RAM although only 256 bytes are needed for the 132-char buffer and for program stack. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.

***See at Booth 2543***

Circle 351 on Inquiry Card

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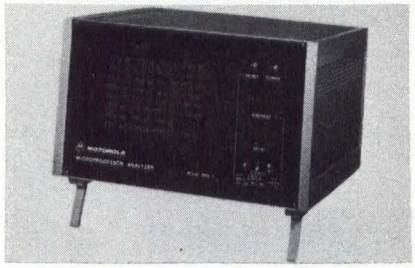
## MICROPROCESSOR ANALYZER



Claimed to be the first digital diagnostic instrument created specifically for convenient testing and debugging of MPU hardware and software, the MPA-1 provides a "window" into actual MPU operation. Words are displayed in hexadecimal to allow direct comparison with written program instructions. Basic operating modes are Start Display, which monitors program execution starting with the trigger-word address and adding the next 31 words in order of their execution; End Display, which works backward in negative-time format from "illegal operations" to track down the source of hardware and software errors; and Free Run, in which continuous address and data information are displayed to locate hardware faults and program hang-ups. **Motorola Data Products,** 455 E North Ave, Carol Stream, IL 60187.

***See at Booth 1228***

Circle 352 on Inquiry Card

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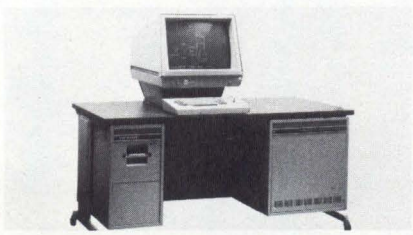
## INTERACTIVE GRAPHIC SYSTEM



A computer-based terminal that combines both refresh and storage graphics in a single display for sophisticated applications of interactive computer graphics, the 4081 enables users to incorporate picture manipulation with highly detailed picture display having up to 45,000 in. of total image. This technology is achieved by use of two computers, one general-purpose and the other a special display processor. Both are housed in a desk-style unit which includes 19" display, tape cartridge drive, ASCII keyboard, 12 function keys, joyswitch, and RS-232-C communications interface. Std software includes a 4014 emulator. Up to 40M bytes of additional local data storage are available with optional flexible and hard discs. The system is supported by 32K bytes of standard memory; main memory is expandable to 64K bytes. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

***See at Booth 2101***

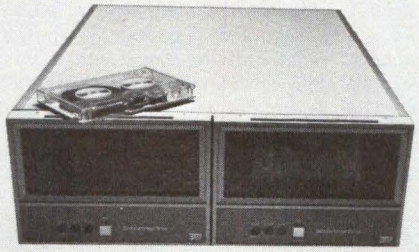
Circle 353 on Inquiry Card

# Once you make up your mind not to be a follower, there's only one alternative.

**You lead.** It's that simple. As 3M did back in 1971 when we introduced the "Scotch" Brand ¼" Data Cartridge. You know the changes it caused in the industry.

Then, in '73, we introduced the people-proof, jam-proof, wear-resistant DCD-3 Drive. It wasn't the first on the market, it was simply the best, with design features that confirmed 3M's engineering leadership. But if you're committed to this business, as we are, you're a slave to constant discontent.

So now, we'd like to introduce you to our new DCS-3000 series, an ANSI-formatted system that allows one formatter to operate up to 8 drives. The media is our standard DC300A Cartridge with a total capacity of 23 million bits. Perhaps its greatest advantage is the ease with which you can integrate it into a system. Only one cable to the user's logic is required. And the complete set of status flags is available to indicate readiness to perform a given function. There's an error check during both read and write operations, and an error flag to indicate errors. There's an automatic search (90 ips) to tape mark, and a variable-length erase function.



It adds up to this: now the system designer has a reasonably-priced peripheral that delivers both data reliability and data interchange capability. We're certain our competitors are going to be very interested in this new system. And if you are too, just write 3M Company Data Products, Dept. 129, Mincom Division, Bldg. 223-5E, 3M Center, St. Paul, Minnesota 55101.

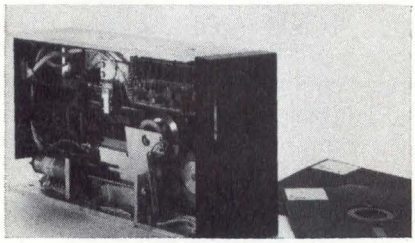
**All our competitors can do is follow us.**

DATA PRODUCTS
**Mincom Division 3M COMPANY**
3M CENTER • SAINT PAUL, MINNESOTA 55101

CIRCLE 56 ON INQUIRY CARD

# NCC PRODUCTS

## DUAL DISKETTE DRIVE

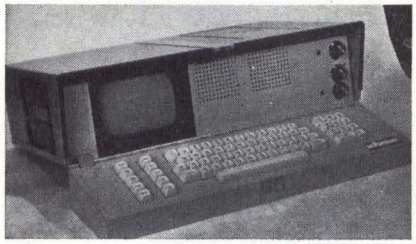


Smaller in size than many single diskette drives and offering faster access to data than two independent drives of most manufacturers, model 270 incorporates two read/write/erase head assemblies but measures only 8.6 x 4.4 x 15.0". Two horizontal or four vertical units can be housed in a 19" rack. Drive is fully IBM 3740 compatible and can accommodate a total of 3.8M bits of data (1.9M bits/diskette) in IBM format. In non-IBM hard or soft sectored formats, the drive will store up to 6.4M bits of data on the two media. With addition of a double density option, storage capacity can be increased to 12.8M bits/drive. Voice coil positioning system facilitates a random avg seek in 33 ms and a full stroke 76-track seek in 100 ms. **Per-Sci, Inc,** 4087 Glencoe Ave, Marina del Rey, CA 90291.

***See at Booth 1642***

Circle 354 on Inquiry Card

## PORTABLE TERMINALS

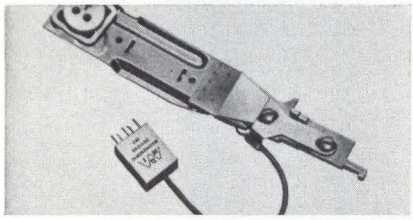


Family of small, lightweight devices are designed for communicating with a computer. P series terminals may be equipped with 301 control which provides full char interactive RS-232 capability at data rates up to 9600 baud, 302-pollable daisy chainable control unit, 301 or 302 control units, and 300-baud acoustic coupler, or 306 control unit including cassette tape recorder and acoustic coupler. This last model can place formats on the screen for operator entry of data, store that data on the tape, and transmit the data via telephone line to a computer at end of entry cycle. Each keyboard contains full numeric pad as well as function keys. Terminals display 512 char on 6" screen in 16 lines of 32 char each. Acoustic coupler is Bell 103 compatible. **Informer, Inc,** 2218 Cotner Ave, Los Angeles, CA 90064.

***See at Booth 2000***

Circle 355 on Inquiry Card

## MAGNETIC DISC HEAD FOR 2314 DRIVES

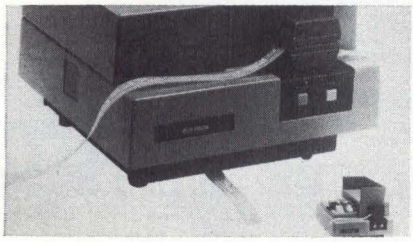


Series A 2000 "flying heads" are designed for use with IBM 2314 disc drives and other equivalent OEM units operating with disc packs. The heads are for read and write applications and are available in single, double, and quadruple densities. They are designed for either 1500- or 2400-rpm applications except for the quadruple series which is available for 2400-rpm speeds only. Quadruple density version can be supplied to furnish a min signal output of 1.2 mV with stable flying characteristics. Also exhibited are 6250 series digital mag tape heads designed to read and record up to 6250 bits/in. on ½" magnetic tape in ANSI tape-compatible format (9042 flux reversals/in.). Heads will operate in either GCR or PE modes. **Magnusonic Devices, Inc,** 290 Duffy Ave, Hicksville, NY 11801.

***See at Booth 1420***

Circle 356 on Inquiry Card

## PHOTOELECTRIC PAPER TAPE READER/PUNCH



Designed for NC, graphic arts, data communications, and computer peripheral applications, the series 1560 is an asynchronous combination desktop unit. It features a LED-type, 150-char/s photoelectric reader housed with a 60-char/s Roytron punch. The unit will punch and read metallized Mylar; sandwich, colored, and standard paper; and 5-, 6-, 7-, or 8-level code tapes; and can accommodate 1, ⅞, or 11/16" widths. A soundproof housing assures quiet operation. Overall dimensions are 10¼ x 15¾ x 15¾". Weight is approx 40 lb. Also on exhibit are two basic series of multimedia, multistation printers for a wide variety of applications. Model SV alphanumeric printers can simultaneously print different data at each of three independently controlled stations, at 2 lines/s. **Sweda International, Div of Litton Industries, OEM Products Div,** 34 Maple Ave, Pine Brook, NJ 07058.

***See at Booth 1000***

Circle 357 on Inquiry Card

# 3M got there first. Again.

We put the features of our ¼" DC300A cartridge into a shirt-pocket size. Then we designed a drive—small in size, small in price, for applications where high data reliability must be combined with compact size.

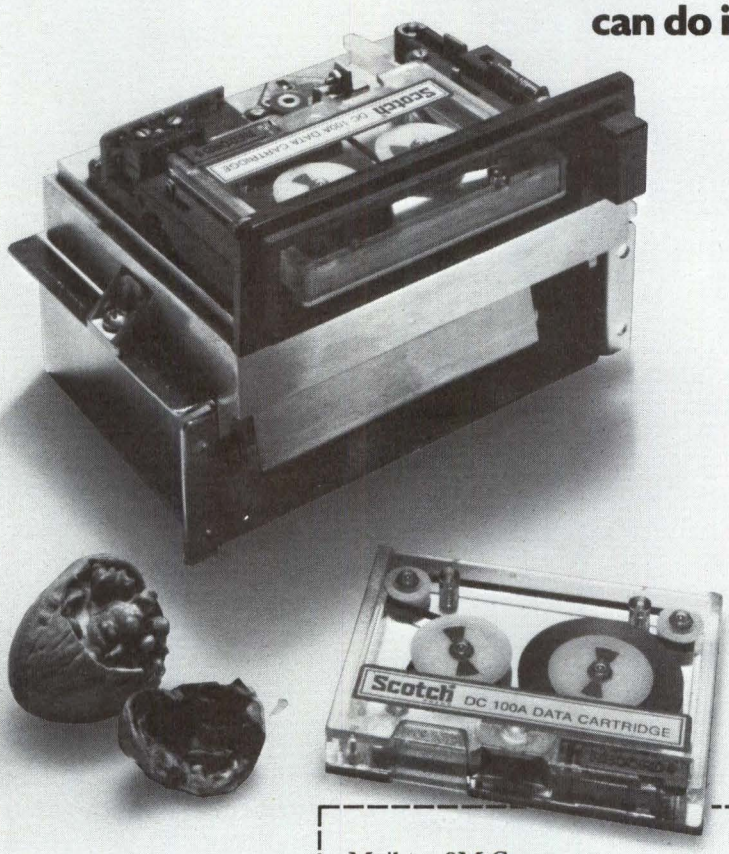
The new DCD-1 system will fit in a 5 inch cube—the cartridge alone measures just 2.4 x 3.2 x .5 inches. Enough about size, let's talk performance.

The drive records *full width* across the entire tape, which virtually eliminates errors. It has an encoding method virtually independent of tape speed, and control logic that prevents the drive from accepting any command that might harm the cartridge.

The electronics are designed to give the system engineer the greatest application flexibility—has byte oriented data input and output and 100,000 byte storage capacity. It's also designed to permit battery operation.

This new system will change the industry much like our ¼" cartridge. So it's time for our competitors to play follow the leader again—if they can. That's the story in a nutshell. Just send the coupon for more details.

**All our competitors can do is follow us.**




Mail to: 3M Company
Data Products, Dept. 125
Mincom Division, Bldg. 223-5E
3M Center, St. Paul, Mn. 55101

I'm interested in receiving information on your DCD-1 Drive.

Name_____
Title_____
Firm_____
Address_____
City_____ State_____ Zip_____
Phone_____

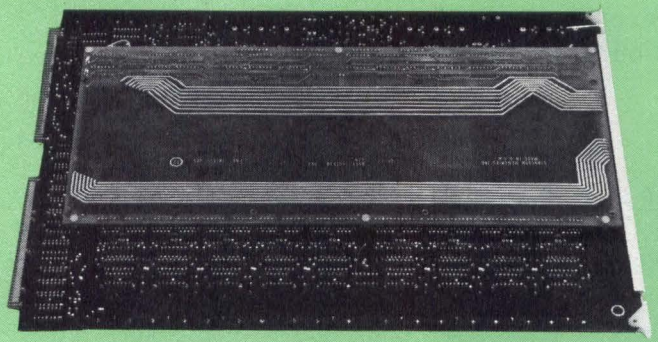
DATA PRODUCTS
**Mincom Division** 3M COMPANY
3M CENTER · SAINT PAUL, MINNESOTA 55101

CIRCLE 57 ON INQUIRY CARD

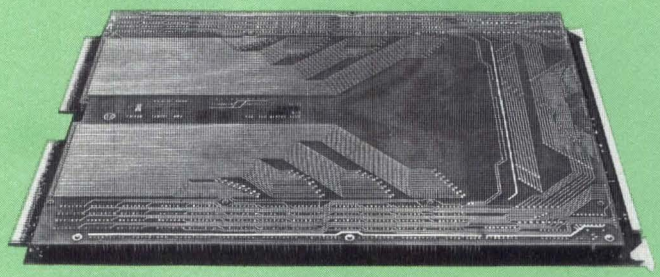
O.E.M.

# TWO MORE *STANDARDS*
## from the Leader in the Memory Industry...

NOW . . . from ***STANDARD MEMORIES*** . . . the new single board ECOM® H 16K and the ECOM® R 32K Core Memory Systems with specifications that meet or beat any others in the industry! And you get a total upward compatibility to 32K. The basic ECOM® Memory System was introduced in 1968 and has established a time-proven record for reliability at a competitive price. Today, for low-cost, off-the-shelf and custom memory systems, there is only one ***STANDARD*** THROUGHOUT THE WORLD!



**ECOM® H MEMORY MODULE H16K18MM**



**ECOM® R MEMORY MODULE R32K18MM**

### SPECIFICATIONS

| MODEL | SERIES H | SERIES R |
|---|---|---|
| MEMORY SIZE | 16K | 32K |
| CYCLE TIME | 650 | 750 |
| ACCESS TIME | 250 | 300 |
| PHYSICAL SIZE | 11.5 x 16 x .75 | 11.5 x 16 x .75 |
| COMPATIBILITY 16K to 32K | YES | YES |

STANDARD MEMORIES

AN APPLIED MAGNETICS COMPANY

4120 Birch Street, Suite 105
Newport Beach, CA 92660
Phone: 714-752-8455
TWX: 910-595-2533

## *SEE US AT BOOTH #2032 During 1976 NCC*

CIRCLE 58 ON INQUIRY CARD

# NCC PRODUCTS

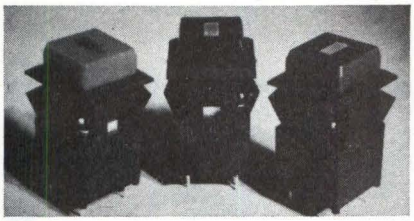
## INTELLIGENT TERMINAL

Portable display terminal has std uc ASCII keyboard with optional numeric pad. Char size is 0.28 x 0.20″ in 5 x 7 dot matrix. Display is neon-orange plasma with 256 char in eight 32-char lines on 3.3 x 8.7″ screen (128 char in four lines on 0.8 x 7.1″ screen optional). Operating modes are full- or half-duplex or local. Block mode is optional. Transmission code is 7-bit ASCII plus 1-bit parity (switch-selectable even, odd, 1, or 0). Transmission speeds are 110 or 300 baud, with options to 9600 baud. Cursor control is optional. Optional intelligence for formatting, editing, or special communications protocols is provided by microprocessor. Unit is available in 18 x 22″ briefcase (14 x 8″ optional). **Applied Systems Corp,** 26401 Harper Ave, St. Clair Shores, MI 48081.

***See at Booth 2100***

Circle 358 on Inquiry Card

## LED LIGHTED PUSHBUTTON SWITCHES

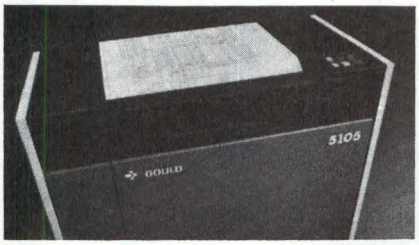


Series offers seven different background button colors with red, yellow, and green LEDs. Centered in a ½″ button, the 0.100 x 0.250″ window displays the LED at a 150-deg viewing angle. Added reliability is provided by stationary LEDs that remain fixed during switch operation. Switch also features 2M cycles at logic level loads using bifurcated contacts and is practical where low contact resistance, bounce, or noise prevail—both audible and electrical. 1- or 2-pole N.O. momentary switching or indicator is optional. Maintained latching logic circuit is available upon request. Also exhibited are series 54 Superswitch II standard, tactile, alternate action, double depression, incandescent, and LED keyswitches. **Licon, Div Illinois Tool Works Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.

***See at Booth 1127***

Circle 359 on Inquiry Card

## ELECTROSTATIC PRINTER/PLOTTER

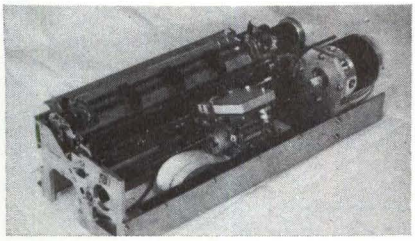



Writing system on the 5105 wide-bed electrostatic printer/plotter produces clean, high density images and smooth line contours from computer-generated graphics and alphanumerics. The device is especially suited for high speed plotting of computer graphics in scientific and engineering applications. It can completely plot standard 22 x 34″ drawings in approx 11 s. 22″-wide coated paper is in 400-ft rolls and has a printing and plotting resolution of 100 dots/in. vertically and horizontally. Graphics are plotted at up to 3 in./s; and 264 alphanumeric characters are printed per line at a speed of 1200 lines/min. with a 128 ASCII u/lc char set. Stylii selectively put dot charges on the electrostatic paper in two rows with the second row offset laterally. **Gould Inc, Instrument Systems Div,** 3631 Perkins Ave, Cleveland, OH 44114.

***See at Booth 2813***

Circle 360 on Inquiry Card

## TYPOGRAPHIC ACTION SERIAL PRINTER



Designed for high speed, heavy duty applications, Shinko M-60 Helianthus has avg printing speed of 60 char/s (50 min). 128-char circular printwheel has operator-replaceable individual char. Entire font can be replaced in minutes without tools. Option permits viewing last char printed. Print lines available are pica, 132 col, 10 char/in., and elite, 158 col, 12 char/in. Forms width is 15″ (38.1 cm) max. Carriage return time is 300 ms for full 15″ page. Paper feed is bidirectional with friction feed, forward feed with sprocket feed, manual set using typewriter declutching knob. Feed speed is 30 ms/line at 6 lines/in. Each section of split platen is individually controlled. Passbook and ticket book inserters are available. Dimensions are 8 x 24.4 x 14.4″ (20 x 61 x 36 cm); weight is 44.1 lb (20 kg). **Mitsui and Co, Inc,** 200 Park Ave, New York, NY 10017.

***See at Booth 3509***

Circle 361 on Inquiry Card

## NCC PRODUCTS

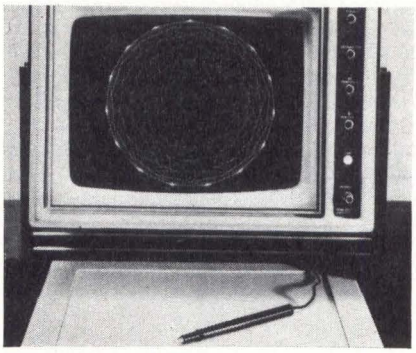
### DUAL CASSETTE RECORDERS

Family of single and dual cassette recorders with high density storage, selectable speeds, high speed search and edit, and online/offline capability, units are RS-232-plug-compatible with keyboard printers, CRTs, minicomputers, and data loggers. 8410 is a single transport unit for use in store and forward operations; 8400 has high speed search and edit. 8420 and 8421 are dual transport units, the latter with high speed search on both decks, and edit. **Techtran Industries, Inc,** 580 Jefferson Rd, Rochester, NY 14623.

***See at Booth 2825***
Circle 362 on Inquiry Card

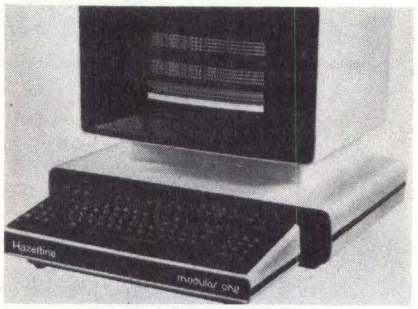
### GRAPHIC PROCESSOR

Capable of flicker-free refreshing of >4000 vectors, points, or char with full screen resolution of ±0.05%, the 76X adds semiconductor and microprocessor technology to the company's earlier graphic products. The unit refreshes from internal memory to essentially eliminate CPU loading. Features include dynamic graphic capabilities, real-time clock, and ASCII keyboard. **Megatek Corp,** 1055 Shafter St, San Diego, CA 92106.



***See at Booth 1807***
Circle 363 on Inquiry Card

### VIDEO DISPLAY TERMINALS




Microprocessor techniques are used with p/ROMs to permit modular expansion of the Modular One. Basic configuration provides 1920-char display (80 x 24) on a 12" bonded screen, incremental and absolute cursor positioning, dual video intensity, 10-key numeric pad on a movable keyboard, eight transmission rates up to 9600 baud, communication interfaces switchable between EIA RS-232 and current loop, and white-on-black or black-on-white display presentation. **Hazeltine Corp,** Greenlawn, NY 11740.

***See at Booth 3418***
Circle 364 on Inquiry Card

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# SUB-MINI Computer Systems - Series 70

**Microprocessor technology integrated into computer systems**

**One Board Computer**

- Intel 8080
- ROM - 1K to 4K bytes
- RAM - 4K to 16K bytes
- Async I/O Controller
- DMA Bus
- Optional:
  - Memory to 64K
  - Operator front panel
  - Peripherals*

**Integrated Computer/Mini Peripheral Systems with IBM Compatible Floppy Disk or 3M Tape Cartridge**

- RS232 Storage System
- Intelligent Terminal
- Complete Software/Hardware Development System
- Tester - Intelligent Floppy Disk Test System
- Sub-Mini Computer System with Peripherals*

**OEM Hardware Systems**

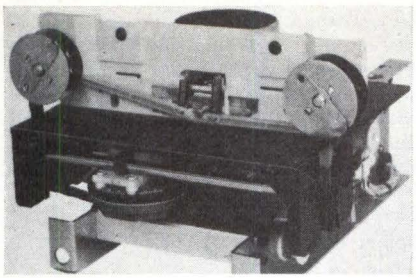
*Complete peripheral support - enclosures, desks, floppy disk, tape cartridge, printers, 9 track tape, communication controllers, 5 and 10 megabyte disks, general purpose controller, clock, paper tape, ROM programmer.

ADC APPLIED DATA COMMUNICATIONS

1509 East McFadden Avenue
Santa Ana, California 92705
Telephone: (714) 547-6954

Also Add-on Mini Peripherals for DEC PDP-11, Data General DEC PDP-8

## ALPHANUMERIC SERIAL INPUT DATA PRINTER



Designed for panel or base mounting and for data recording first line down, with first line visible after printing, the 35-, 60-, or 80-col unit uses ordinary paper up to 8½" wide and ribbon or impact sensitive paper rolls. Input is serial with proprietary dot-matrix head as printing medium. Input rate is 110 char/s. Char pitch is variable; 12/in. is normal. Char enhancement can be obtained through optional electronic controls. **Practical Automation, Inc,** Trap Falls Rd, Shelton, CT 06484.

***See at Booth 1631***

Circle 365 on Inquiry Card

## ADD-ON MEMORY SYSTEM

Designed to expand or replace any of the DEC family of PDP-11 memories, the BUSCOMM® H-11 interfaces directly to the DEC Unibus® cable. All interface logic drivers and receivers are fully compatible with the Unibus transmission line characteristics. The 5¼" enclosure may be expanded to a max of 65K words; an optional 12¼" enclosure may be expanded to 124K words. The system offers parity and interleaving. **Standard Memories Inc,** 4120 Birch St, Suite 105, Newport Beach, CA 92660.

***See at Booth 2032***

Circle 366 on Inquiry Card

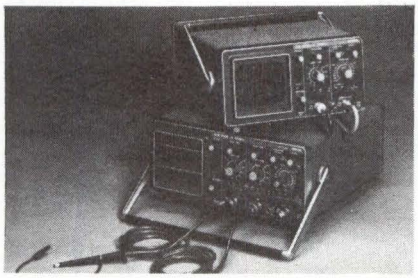
## SMALL BUSINESS SYSTEM

Available with 32K, 49K, or 65K bytes of MOSFET memory, System/4 configurations can accept either punched card or flexible disc input. 96-col data recorders read at 300 and punch at 60 to 120 cards/min., while card readers operate at 300 to 1200 cards/min. From two to six diskettes can be used in the system, each able to access 500K bytes of data. Console screen displays messages two lines at a time, 16 char/line. **Decision Data Computer Corp,** 100 Witmer Rd, Horsham, PA 19044.

***See at Booth 2527***

Circle 367 on Inquiry Card

## LIGHTWEIGHT OSCILLOSCOPES

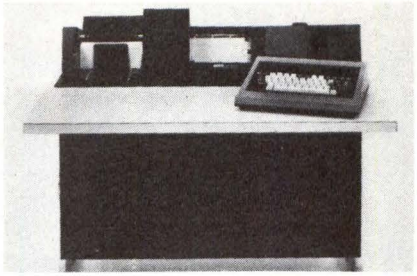


The single trace PM3225 weighs 8 lb 2 oz, and measures 4.72 x 9 x 12.5"; the dual 3226 weighs 9 lb 10 oz, and measures 4.72 x 10.8 x 12.5". Both offer adjustable level, automatic, line, and automatic TV line and frame sync pulse triggering. External triggering is also possible. Input impedance of vertical and horizontal channels is 1 MΩ/25 pF, and risetime is 25 ns. Dynamic range is 24 div for sinewave signals up to 1 MHz. **Philips Test & Measuring Instruments, Inc,** 400 Crossways Pk Dr, Woodbury, NY 11797.

***See at Booth 1033***

Circle 368 on Inquiry Card

## INTERPRETING PUNCH/VERIFIER



For use in 80-col card production, the 501 is equipped with a versatile microprocessor, which provides intelligence; is fully buffered; and has chained-program selectivity, memory storage for constant data, check digit, accumulate, and computation functions. An interface has been added to the unit to allow the full range of capabilities to be used online in RS-232 serial, parallel, or TTY-compatible modes. **Tab Products Co,** 2690 Hanover St, Palo Alto, CA 94304.

***See at Booth 2707***

Circle 369 on Inquiry Card

## GRAPHIC COMPUTER TERMINAL

Offering selective erase of single char or vector, bright high resolution display, and intermixed display of vectors, text, and video frames, the 801's capabilities include X-Y plotting of vectors and points, full ASCII alphanumeric text, and exclusive intermix of video live action or single frames with computer-generated graphics. Specs include a matrix of 1024 x 1024 addressable points, 32 linear-level gray scale, and writing at 4K char/s or 11K vectors/s std. **Princeton Electronic Products, Inc,** PO Box 101, North Brunswick, NJ 08902.

***See at Booth 2018***

Circle 370 on Inquiry Card

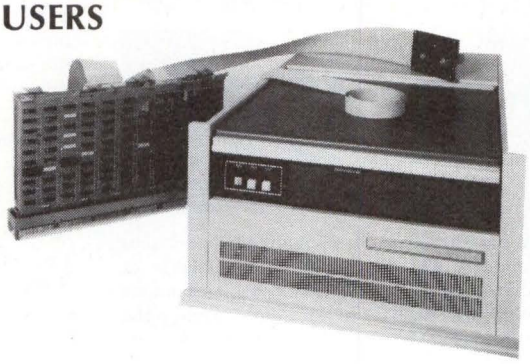

**PDP-11 and NOVA USERS of disk storage systems**

If you are a

- Chief Engineer
- Financial Officer
- Marketing Manager
- Field Service Manager

of a PDP-11 or NOVA-type OEM or end user, you should be talking to Xylogics about our Phoenix Series of disk controllers.

WHY?



Xylogics

XYLOGIC OEM COMPONENTS GROUP, INC.
42 Third Ave., Burlington, Massachusetts 01803
617/272-8140

BECAUSE we know what you are interested in . . .

The Xylogics Phoenix 211 controls up to 4 CDC storage modules

- with DMA throttle control
- variable sectoring
- exclusive command queuing
- and more - call us for details

EXCLUSIVE – Microprocessor self-test isolates disk subsystem problems in minutes without fear of crashes or burned-out units

DOCUMENTATION – Far exceeds industry standards in detail and completeness

PERFORMANCE – Proven faster throughput and reduced CPU overhead

COMPATIBILITY – Media and software compatible with RK-11, 4046, 4234

PRICE – Call us and see how we can help you achieve better margins

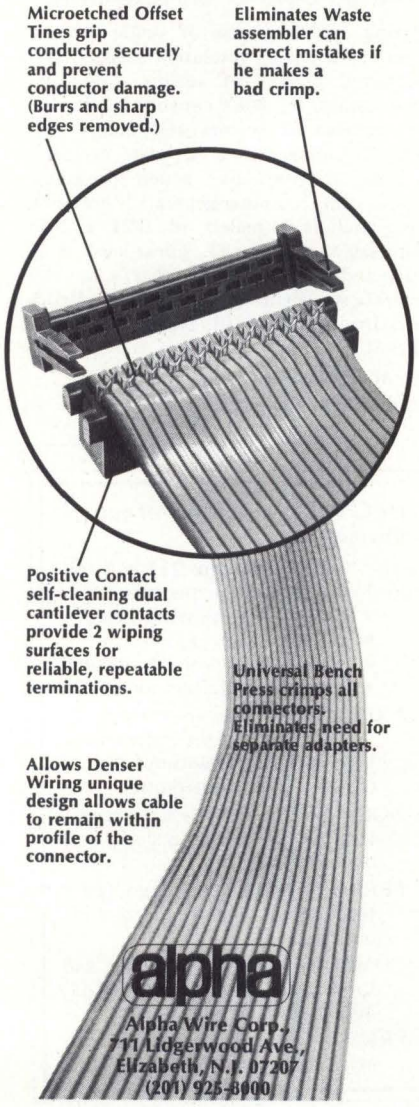
CIRCLE 61 ON INQUIRY CARD

# New ideas from a new source for flat cable and connectors

The source: Alpha Wire, one of the oldest full-line wire and cable manufacturers.

Our cable is compatible (matches all flat cable connectors designed for 0.050 in. conductor spacing). It has excellent teardown characteristics, is ultra-flexible, and UL listed. Exclusive footage indicator on the reel shows how much cable is left.

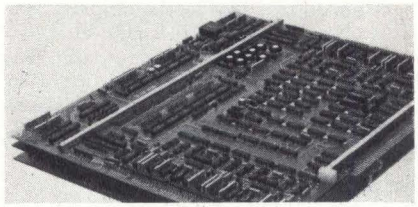
Our complete line of connectors (female sockets, headers, DIPs and PCBs) also offer some new ideas:





## NCC PRODUCTS

### SINGLE-BOARD CORE SYSTEM



Containing 2.4M bits, the DR-128 is claimed to be the industry's largest capacity single-board core memory system. While providing speeds in the main memory range, its capacity makes it suitable for high performance peripheral applications. A 19" chassis can contain up to eight systems or 2M bytes of storage. Cycle time is 1.3 $\mu$s; access time is 650 ns. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512.

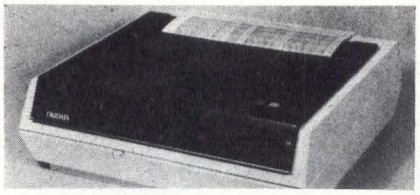
***See at Booth 1117***
Circle 371 on Inquiry Card

### 10½" REEL TAPE DRIVES

Three models of large drives that hold 2400 ft of ½" mag tape permit data storage of >25M char. Model 9554 has 800-bit/in. density, 9 tracks, and NRZI recording; while the 9555 has seven tracks. 9583 has 1600-bit/in. density, 9 tracks, and PE recording. All operate at 12½ in./s. Also exhibited is an MPU-based communications interface. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.

***See at Booth 3250***
Circle 372 on Inquiry Card

### 132-COL MATRIX PRINTER



A desktop or pedestal-mounted model that produces 132 col of 5 x 7 matrix char at 125 lines/min. or 265 char/s continuous with no limitation on duty cycle, the printer has a proprietary printhead composed of 22 pin drivers instead of the std seven or nine, and uses state-of-the-art constant current drivers to more than triple head life. Available with OEM parallel and RS-232 serial interfaces, unit includes u/lc ASCII set, 6 or 8 lines/in. spacing switch-selectable, and double-height or width char. **Okidata Corp,** 111 Gaither Dr, Moorestown, NJ 08057.

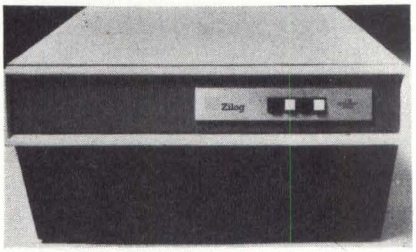
***See at Booth 2301***
Circle 373 on Inquiry Card

### INTELLIGENT TERMINAL

Dual MPU-based system 70 is preprogrammed for immediate use. Built-in terminal command language allows operator to instruct terminal using std English commands. Unit can automatically edit data input, manipulate data files, and control printer output. Workstation consists of CRT and keyboard, diskettes, and communications interface. **Applied Digital Data Systems Inc,** 100 Marcus Blvd, Hauppauge, NY 11787.

***See at Booth 1219***
Circle 374 on Inquiry Card

### MICROCOMPUTER DEVELOPMENT SYSTEM

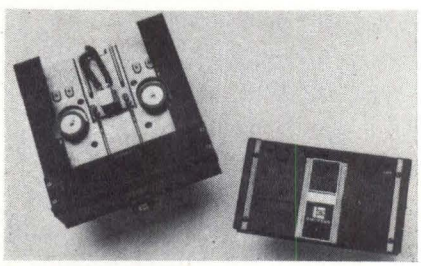


Z-80 microcomputer line consists of an LSI component set with CPU and I/O controllers, full software support utilizing high level languages and featuring 158 instructions (including all 8080A instructions), floppy-disc based development system with real-time debug capability, and support services. The CPU, programmable parallel I/O controller, programmable serial I/O controller, and DMA controller are provided in std 40-pin DIPs; a counter-timer circuit is in a std 28-pin DIP. **Zilog, Inc,** 170 State St, Suite 260-A, Los Altos, CA 94022.

***See at Booth 1442***
Circle 375 on Inquiry Card

### MAGNETIC TAPE SYSTEM

Superior tape handling and greatly improved media protection are claimed for the 2000 series Tape Pac® system. Dual-differential capstan drive uses no reel motors or associated servos. Tape pack totally protects tape; 600 ft (1000 ft optional) of tape is stored in a reel-to-reel configuration mounted to bearings in the unit. Integral tape guides result in no oxide contact for long tape life. **Emerson Electric Co, Industrial Controls Div,** 3300 S Standard St, Santa Ana, CA 92702.



***See at Booth 1218***
Circle 376 on Inquiry Card

## BUFFERED DATA TERMINAL SYSTEM

Built around the model 250 tape cassette transport system, the model 5000 uses a microcomputer for control and efficiency. Providing programmed high speed search and edit functions as well as full communications capability, the unit conforms to ANSI/ECMA stds (industry defined) with tape speeds of up to 120 in./s on cassettes capable of holding 155K char of formatted data. The compact system weighs <10 lb. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.

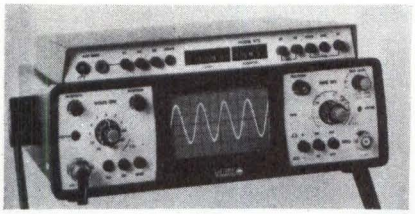
***See at Booth 2044***
Circle 377 on Inquiry Card

## LINE PRINTER SYSTEMS

Four basic configurations of the D-3000 family have 240-, 300-, 436-, and 600-line/min. rated print speeds. Each prints 136 col/line. Two have 64- and two have 96-char/col char sets. Models 3240 and 3300 have passive ribbon tracking; 6436 and 6600 have active tracking. On all, char spacing is 10/in. and line spacing is switch-selectable 6 or 8/in. **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.

***See at Booth 1709***
Circle 378 on Inquiry Card

## DMM/COUNTER/OSCILLOSCOPE



PS915/975 includes DMM, frequency counter, and oscilloscope in a single 3½ x 8½ x 12½" unit with all three devices having individual displays. All can be used simultaneously as complements, or independently at the same time. The unit can be operated from normal ac power, from a 12-Vdc source, or from an optional battery pack. The 975 DMM/counter includes 3½-digit digital multimeter as well as 4-digit 20-MHz frequency counter. Scope is a 20-MHz bandwidth, triggered sweep, single trace unit. **Vu-data Corp,** 7170 Convoy Ct, San Diego, CA 92111.

***See at Booth 2019***
Circle 379 on Inquiry Card


# MAG TAPE SYSTEMS FOR MINICOMPUTERS

**Compatible** with PDP-11, PDP-8, NOVA, and HP 2100.

**Reliability** backed by a full one-year warranty.

**Prices** from **$4,750** for a complete system which includes transport, controller cables and diagnostics.

DIGI-DATA CORPORATION

*Supplier of magnetic tape transports and systems.*

8580 Dorsey Run Road, Jessup, Md. 20794 (301) 498-0200
831 S. Douglas St., El Segundo CA 90245 (213) 640-2060
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**CIRCLE 63 ON INQUIRY CARD**

NCR

**TERMINAL SYSTEMS DIVISION**
**CAMBRIDGE, OHIO**

## COMPUTER SYSTEMS ENGINEERS [2]
## ESSP

**To begin the evaluation of total P.O.S. computer system as it relates to incorporating *ESSP — ENVIRONMENT — SAFETY — SECURITY — POWER MANAGEMENT.***

These engineers will have a major input for defining the scope and direction of this program and then defining a system to implement it. They will analyze, select, and specify specialized sensor and control equipment to interface with P.O.S. systems for Supermarket applications. They will interface with software analysts and hardware designers in assuring overall system performance objectives are met.

A BS or MS degree in applicable areas of Engineering Science and competence in both hardware and software design, with emphasis on product/system definition. Since ESSP is a new area of attention, we are looking for a well rounded hardware/software background that can be brought to bear on these new areas of emphasis.

**We invite you to respond at your earliest convenience.**

**Robert W. Donovan**
**Terminal Systems Division**
**NCR Corporation**
**Cambridge, Ohio 43725**
**Phone: 614/439-0398**

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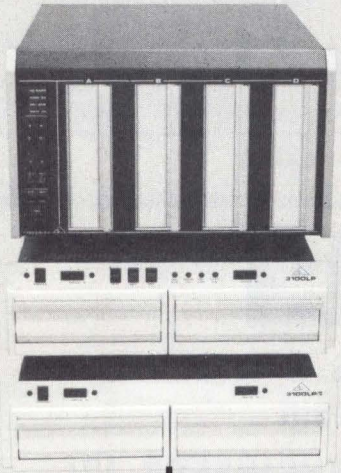
**CIRCLE 900 ON INQUIRY CARD**

# THE OS FLOPPY

**FOR OS/8 . . . RT-11 . . . RDOS . . . DOS AEDOS-11 . . . AEDOS-NOVA . . . IRIS . . . YOU NAME IT!**

Now AED offers the choice of either IBM-compatible or Double Density floppy disk subsystems to run your Operating System. The table below indicates the byte capacity of Double Density (MFM) storage compared to conventional storage. All AED subsystems are available with up to four drives in either standard cabinets or low-profile cabinets. And the list of interfaces goes on and on. AED . . . the world's most flexible floppy disk subsystems.

| Recording | Words/ Sector | Sectors/ Track | Tracks/ Diskette | Bytes/ Diskette | μs./ Byte |
|---|---|---|---|---|---|
| IBM Compatible 3100 Series | 128 | 26 | 77 | 256,256 | 32 |
| Double Density 6200 Series | 64-512 | 128-16 | 77 | 630,784 | 16 |



VARIAN — PDP-11
INTEL — NOVA/ECLIPSE
CAI — LOCKHEED
INTERDATA — MICRODATA
HP — PDP-8A, E, F, L, M

**PRICES**

| Qty. 1 | Configuration | Qty. 100 |
|---|---|---|
| $2,950 | ONE DRIVE | $1,770 |
| $3,650 | DUAL DRIVE | $2,320 |
| $4,550 | TRIPLE DRIVE | $3,152 |
| $5,250 | QUAD DRIVE | $3,540 |

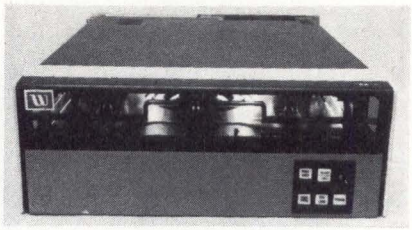
**Telephones: (408) 733-3555 and (213) 889-6312**

**FROM AED**

**Advanced Electronics Design,** 754 N. Pastoria Sunnyvale, California 94086 Telex 357498


## NCC PRODUCTS

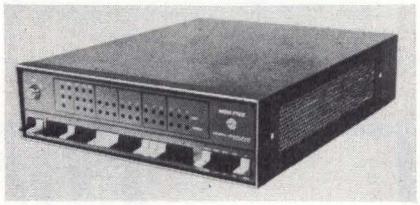
### CARTRIDGE DISC DRIVES



Super F front-loading drives take only 7″ of vertical space in a std 19″ rack; the units use IBM 2315-type cartridges, record 50M bits/disc at 2200-bit/in. density, and provide 33-ms avg access time. Features include brushless dc spindle, tachless positioner, zero spindle-speed sensor, fault detection logic, and end of travel interlock. **Wangco Inc,** 5404 Jandy Pl, Los Angeles, CA 90066.

***See at Booth 1521***
Circle 380 on Inquiry Card

### MICROPROGRAMMED COMPUTER



Upward and downward compatible with other computers in the 16 series, Mod Five features single CPU board, eight general-purpose registers, up to 16K words of core and up to 32K words of MOS memory on one board, memory expansion to 128K words, stack processing, and full software support. Available speeds are 800, 1000, and 1200 ns; configurations can be with 4, 7, 10, or 17 slots. **Digital Computer Controls Inc,** 12 Industrial Rd, Fairfield, NJ 07006.

***See at Booth 2407***
Circle 381 on Inquiry Card

### CORE MEMORY SYSTEM

Featuring full cycle time of 650 ns with 250-ns access time, the 16,384 word x 18-bit model 696 is field expandable to 256K x 9, 128K x 18, or 64K x 36, and is pin-compatible with the Micro 3000 core memory. Model 698 has basic capacity of 32K words x 18 bits, and expands to 512K x 9, 256K x 18, or 128K x 36. Also shown is the Q9/MP, which provides 1-μs full cycle across the −55 to 95°C temp range, and has a 300-ns access time. **Fabri-Tek Inc,** 5901 S County Rd 18, Minneapolis, MN 55436.

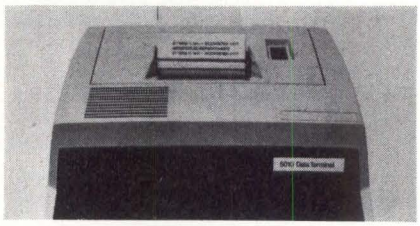
***See at Booth 2445***
Circle 382 on Inquiry Card

### EMULATOR-p/ROM PROGRAMMER MODULE

Extending the MICROKIT-8/16's debugging monitor directly into the user's 8080 system, the module provides a 40-pin DIL plug to connect into the 8080 socket. The p/ROM programmer is usable with 2708 and 2704 EPROMs. Logic analysis features include emulation of the 8080 microprocessor in the user system, hardware and software breakpoints, DMA within user system, and single- and slow-step modes with register and 168-byte memory display at each instruction step. **Microkit Inc,** 2180 Colorado Ave, Santa Monica, CA 90404.

***See at Booth 1034***
Circle 383 on Inquiry Card

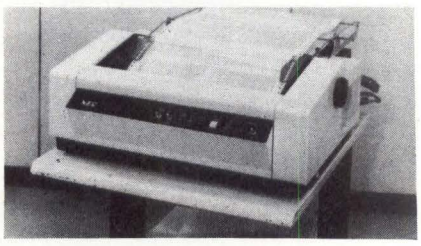
### DATA TERMINAL



The 5010 series terminal includes an IPM 130 print mechanism and the electronics to drive it from an ASCII input. Input may be either serial (bit serial) or parallel (bit parallel, char serial). Printing mechanism is a wire-matrix dot printer with a strobe track for detecting the printhead position. Strobe signals are used to form a 5 x 7 dot char. Printing rate is 110 char/s. Line rate is 1.5 lines/s for a full 34-char line or 4.2 lines/s for line feed only. **Victor Comptometer Corp, Business Products Group,** 3900 N Rockwell St, Chicago, IL 60618.

***See at Booth 2010***
Circle 384 on Inquiry Card

### INTELLIGENT PRINTER



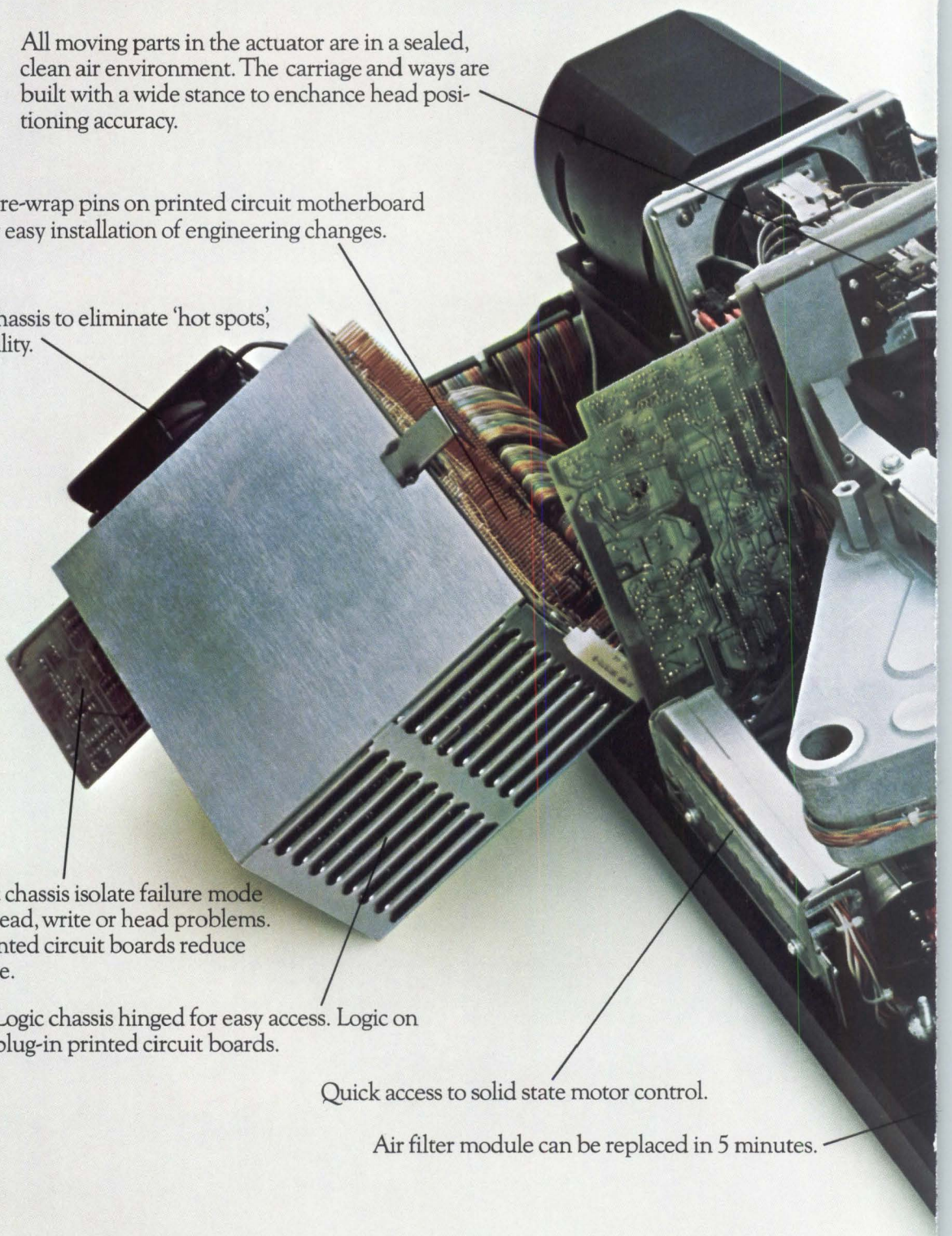
Capable of operation as terminal of either computer or communication system, the NH3000 "High" printer is a serial 9 x 7 dot matrix impact device with speed of up to 180 char/s. Up to 132 char can be printed per line. Spacing is 10 char/in., 6 and 3 lines/in. Carriage return time is 330 ms for a full line. Line feed time is 32 ms. Acoustic noise is <60 dB. **NEC America, Inc,** 277 Park Ave, New York, NY 10017.

***See at Booth 3415***
Circle 385 on Inquiry Card

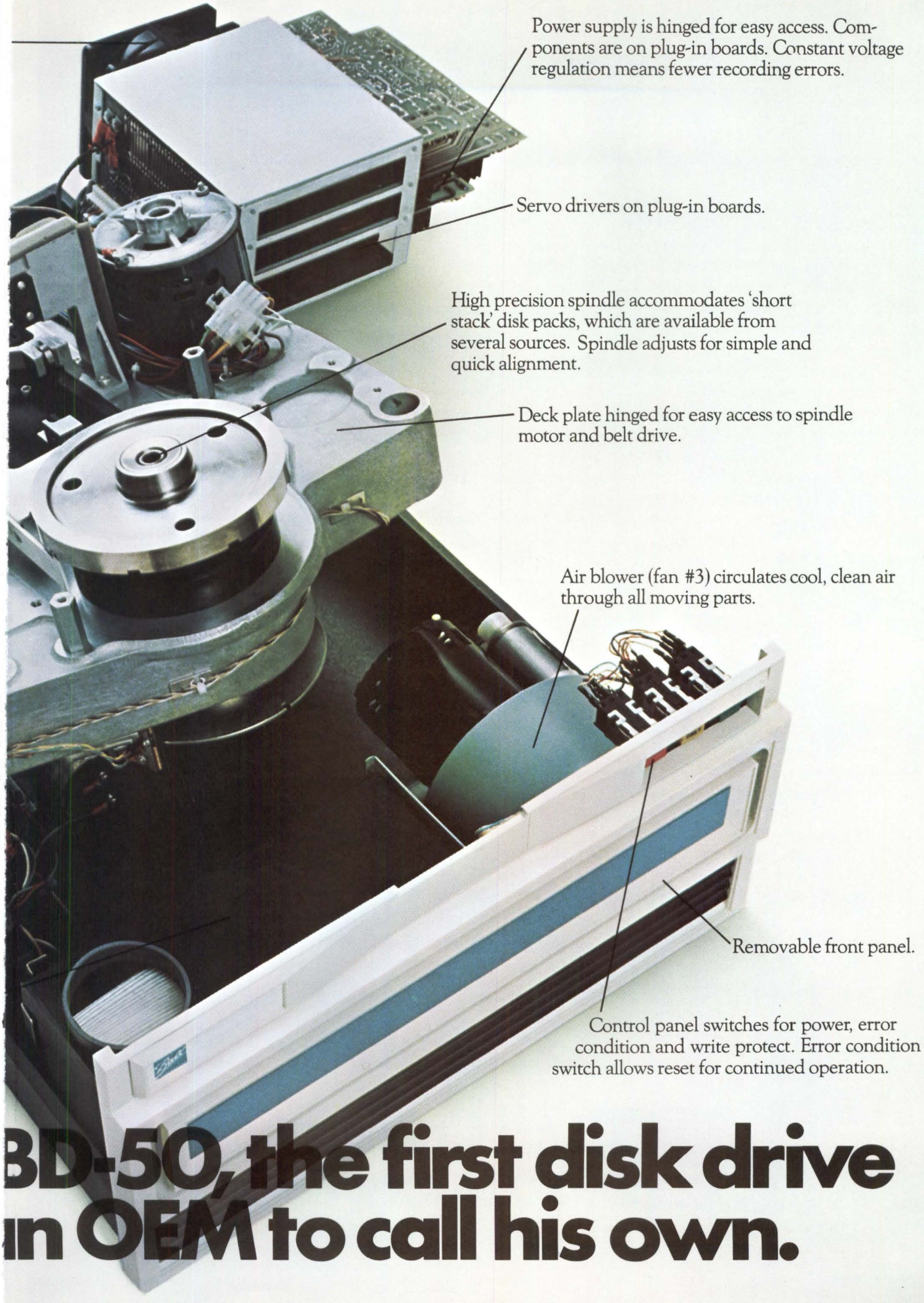
"It's bad enough when the disk drive fails. It's even worse when it takes half the weekend to find the trouble and fix it."

"What I need is a more reliable disk drive; one that's easier to maintain. And when a problem does occur I want to be able to find it and replace the part in minutes—not hours."

"In the systems business, customers demand trouble free performance. It's that simple."




# Announcing the Ball I
# that's good enough for a




# BD-50, the first disk drive an OEM to call his own.

## BD-50 Specifications

**Description:** The Ball Computer Products model BD-50 Disk Drive provides a new standard of reliability and maintainability for the OEM. The BD-50 accommodates a removable 3330-type 'short stack' disk pack with 50 megabytes of data storage. The BD-50 satisfies the OEM's requirement for large capacity disk files to interface with small and medium size computers in applications where trouble-free performance is critical. The BD-50 combines reliable, proven drive technology with features that ensure high reliability, maintainability, and ease of repair.

**Reliable:** To provide the highest possible reliability, the BD-50 has the industry's first triple cooling system in a compact design, an actuator mechanism that is sealed in a clean air environment, and a constant-voltage power supply. Together, these features eliminate or greatly reduce the most common disk drive problems: dust and dirt accumulation on precision mechanisms, head crashes caused by contamination, hot spots in circuitry that cause premature component failures, and susceptibility to recording errors resulting from line-power variations.

A track-following servo system is employed, requiring no external reference, nor any reference temperature compensation. A servo track surface on the disk provides reliable operation at all operating temperatures.

**Maintainable:** The BD-50's maintainability features are organized to speed preventive maintenance, simplify trouble-shooting and repair in the field if a failure should occur, and prevent an operator from inadvertently using the system when maintenance is needed.

Since the most frequent maintenance requirement is clean-air filter replacement, the BD-50 has a quick access filter. The system is fully modular using separate chassis for actuator and motor control mechanisms, power supply and logic. All electronic circuitry including servo-drivers is on plug-in cards, arranged in functional groupings and provided with built-in test points. Deck plate, logic, and power chassis are hinged for easy access.

When a problem is detected, internal latches monitor operation and light LED indicators on the chassis next to the corresponding circuits. The operator can reset the drive from the front panel but the latches can only be over-ridden by opening the cover and pressing the release buttons next to the LED indicators.

All critical electronic parts, including voice coils and heads are readily available from several sources. You're not tied to one source for replacement parts. Disk packs are also available from several suppliers.

**Features**

**Capacity**
50 million 8-bit bytes

**Transfer Rate**
6.45 megahertz
806 Kbytes/sec

**Access Time**
Track to Track—5 milliseconds max.
Average Positioning—30 milliseconds
Full Stroke—55 milliseconds max.
Average latency—8.3 milliseconds

**Pack Start/Stop Time**
Start—20 seconds
Stop—20 seconds (Dynamic Braking)

**Densities**
Track Density—370 tracks/inch
Recording Density—4040 bits/inch
(unformatted) 13,440 bytes/track
67,200 bytes/cylinder
815 cylinders/pack

**Disk Pack Characteristics**
Disk Pack—IBM 3336-11 Components
Recording Surfaces—5 plus 1 servo surface
Cover Disks—2

**Operating Methods**
Recording Method—Modified Frequency Modulation
Positioning Method—Track-following Servo

**Controls & Indicators**
Start/Stop Switch
Ready Indicator
Read Only Indicator/Switch (write protect)
Fault Indicator/Reset Switch

**Interface (all digital)**
Control & Address Lines—Single Open Ended Collector
Clock & Data Lines—Differential ±0.6 Volts

**Physical (Self contained power supply)**
17.5" wide x 10.5" high x 31" deep
Weight—185 pounds

**Power**
Input Voltages—115 ± 15% VAC, 60 Hz, single phase
225 ± 15% VAC, 50 Hz, single phase
Power Cable Included

**Environmental Conditions**
Operating Temperatures—60° to 90°F
15.6° to 32.2°C
Humidity—10% to 80% noncondensing
Altitude—(−) 1000 feet to (+) 6000 feet

**Additional Standard Features**
Address Mark Detection
Variable Sector Sizes
Sector Address/Cylinder Address Read Commands
Uniform cooling with individual fans per electronic chassis

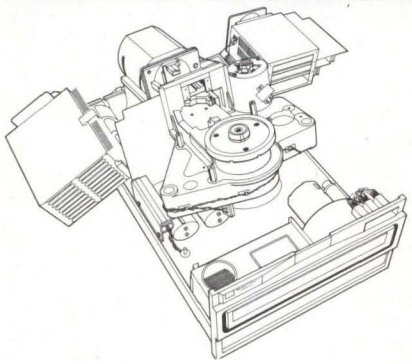
**Options**
Rack or Pedestal Mounting
NRZ Data Interface
VFO & Encoder/Decoder Functions
Differential Control & Address Lines
Signal Cables; 7, 10, 15 or 25 feet
Read/Write Cables; 7, 10, 15 or 25 feet

**Also Available**
Ball Model 3300 Comprehensive Formatter with error correction, variable record length and multiple drive capability
CPU Interfaces for various minicomputers

**Ball Computer Products, Inc.**
SUBSIDIARY OF BALL CORPORATION

Ball Computer Products, Inc., 860 East Arques Avenue, Sunnyvale, California 94086
**Regional Offices** Los Angeles, (213) 822-1419; New York, (201) 224-2332; Chicago, (312) 593-3450; Boston, (617) 482-0101; Atlanta, (404) 289-0101; San Francisco, (408) 733-6700

# The first disk drive that's good enough for an OEM to call his own.



If our four-page disk drive announcement is missing from the opposite page, then you can't read why Ball Computer Products' BD-50 sets a new standard in disk drive reliability and maintainability.

If you select disk drives, you should know about the 50 megabyte BD-50. Use the reader service number below, or call our nearest sales office.

Either way, we'll show you why the BD-50 is the first disk drive that's good enough for an OEM to call his own.

**Ball Computer Products, Inc.**
SUBSIDIARY OF BALL CORPORATION

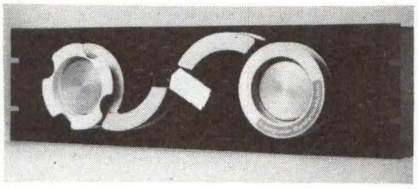
Ball Computer Products, Inc., 860 East Arques Avenue, Sunnyvale, California 94086

Regional Offices: Los Angeles, (213) 822-1419; San Francisco, (408) 733-6700; New York, (201) 224-2332; Chicago, (312) 593-3450; Boston, (617) 482-0101; Atlanta, (404) 289-0101.

See us at COMPDESIGN/76 in Los Angeles, May 4-6, and San Francisco, May 11-13.


# NCC PRODUCTS

## MINICOMPUTER TAPE SYSTEM



A bidirectional direct-access mass storage system, the CO-3000N Linc tape is designed for use with Data General Nova and Eclipse processors. Features include 8400-byte/s transfer rate, 335K bytes/reel capacity, software operating system, up to four transports on one controller for 1M bytes capacity, redundant 10-track recording, and immunity to wide power variations. **Computer Operations, Inc,** 9700-B George Palmer Hwy, Lanham, MD 20801.

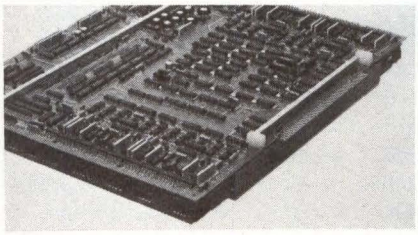
***See at Booth 2007***
Circle 386 on Inquiry Card

## PEN DIGITIZERS

NT series Graf/Pen digitizers use a sonic ranging technique to determine the location of a point on a plane. NT-101 is an OEM version without timing and logic circuitry; -201 is a single-bar, 2-sensor model that provides digital triangular-coordinate output in binary or BCD format; and -211 has built-in compensation for variations in the speed of sound with varying temp. **Science Accessories Corp,** 970 Kings Hwy W, Southport, CT 06490.

***See at Booth 1803***
Circle 387 on Inquiry Card

## BULK CORE STORAGE SYSTEM



From 256K to 4M bytes of I/O storage are provided in 256K-byte increments by the Memory Plus system. Throughput ability is in the 6M-byte/s range (1.5M bytes with one 256K module). As many as eight modules can be packaged in each 19" rack-mountable card file. Each file also accommodates a dual-ported interface which includes an offline test feature for modes and a power supply. **Modular Computer Systems, Inc,** 1650 W McNab Rd, Fort Lauderdale, FL 33309.

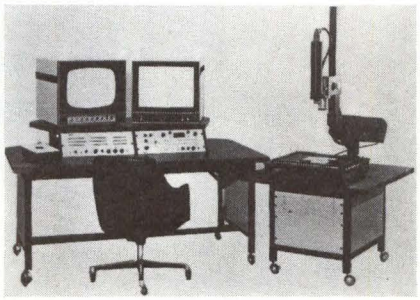
***See at Booth 1203***
Circle 388 on Inquiry Card

## VISUAL DISPLAY SYSTEM

GD-1 provides the flexibility to meet changing demands of communications protocols and systems requirements by programming changes into the microprocessor. Peripherals include printers and disc drives; the system has graphics plotting capability, self-checking features, double-width char, and two char generators to provide a second language. **Lynwood Scientific Developments Ltd,** Caker Stream Rd, Mill Lane, Alton, Hampshire GU34 2QF, England.

***See at Booth 3100***
Circle 389 on Inquiry Card

## IMAGE PROCESSING SYSTEM



The Computer Eye Image Station, a digital picture processing terminal, enhances and measures all types of pictures including aerial photos, radiographs, and microscope images. It provides standalone capabilities or acts as an intelligent terminal to larger host computers. Major components consist of image scanner, analog enhancement and measurement system, image digitizer, and storage tube display. **Spatial Data Systems, Inc,** Box 249, 508 S Fairview, Goleta, CA 93017.

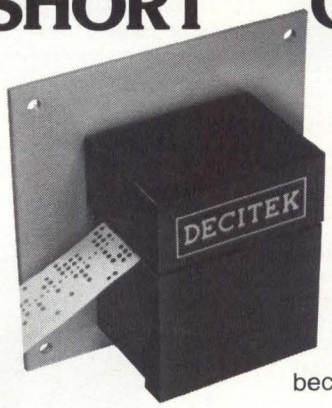
***See at Booth 1111***
Circle 390 on Inquiry Card

## ALPHANUMERIC DISPLAY TERMINALS

Teletypewriter-compatible Vistar/GTX features 1920 (80 x 24) char display, EIA RS-232-C and selectable (up to 9600) baud rates, and a solid-state detachable keyboard for reliability and operator convenience. Convection cooling allows quiet operation. The /SATELLITE incorporates the same std features plus cursor control cluster, numeric keypad, function keys, addressable cursor, u/lc (switchable), and char/block mode transmission. **Infoton,** Second Ave, Burlington, MA 01803.

***See at Booth 3005***
Circle 391 on Inquiry Card

# SAM® IS THE LOWEST PRICED READER YOU CAN BUY. BUT YOU DON'T GET SHORT CHANGED.




You could spend a lot more for a tape reader and still not get all of SAM'S quality features. SAM clips along at 300 cps, has our sure-footed dual sprocket drive and our state-of-the-art fiber optic light source and photo transistor read head. We can make SAM do all this *and* save you money because we do things differently.

This is the plain, brown wrapper SAM comes in.

The more you know about punched tape equipment, the better you read us.

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CIRCLE 66 ON INQUIRY CARD

# The LINEAR DISC.....

■ LINC TAPE expands your program development, editing, loading, and data acquisition capabilities through direct, block addressible "disc like" format in a convenient and inexpensive medium ■ Reduces access time because searching can be performed in either direction ■ High reliability is ensured by a redundant recording capability ■ Simple, rugged reel-to-reel drive without capstan ■ Storage — 335,872 bytes/reel ■ Transfer Rate — 8400 bytes/second.

APPLICATIONS
- DISC BACKUP
- BOOTSTRAPPING
- DIAGNOSTICS
- SOFTWARE DISTRIBUTION

Interfaces and Operating Systems for NOVA®, PDP®-11, HP 2100, INTERDATA, and VARIAN.

LINC TAPE for PDP®-11 is DECtape® and RT-11 compatible.

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LINC TAPE

CIRCLE 67 ON INQUIRY CARD

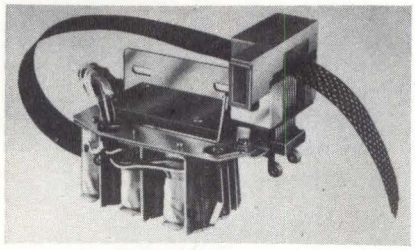

## NCC PRODUCTS

### TEXT EDITING TERMINAL

"Edit-Bee" is programmed with editing features and may be custom programmed for modifications or additional features. Offline viewing allows review and editing of data before it is output to computer. Unit displays up to 256 char in 7 x 9 dot matrix on 15" CRT, 25 lines at a time with up to 80 char/line. **Beehive Terminals, Beehive Medical Electronics, Inc,** Box 25668, Salt Lake City, UT 84125.

***See at Booth 1211***
Circle 392 on Inquiry Card

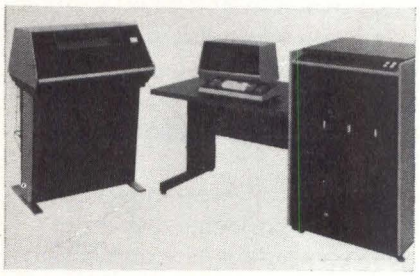
### PAPER TAPE PUNCH



Features of Moduperf 75 include field-replaceable modules that allow operator to make adjustment-free replacements of the die block and/or data selector in less than 1 min. Quiet device operates by making the data selection directly on the punch pins and advancing the tape with a stepping motor, eliminating need for intermediate levers, links, clutches, ratchets, and pawls. **Data Specialties, Inc,** 3455 Commercial Ave, Northbrook, IL 60062.

***See at Booth 2117***
Circle 393 on Inquiry Card

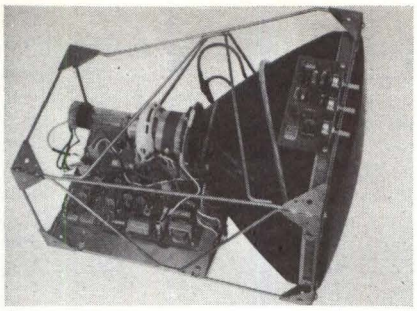
### REMOTE DATA ENTRY SYSTEM



Flexible disc storage medium in the model 77 allows data entry, edit, storage, and transfer under data entry and communications software control. System is programmed key-to-diskette/communications product for use in distributed processing applications. Also exhibited are OEM line printers, disc drives, magnetic tape transports, card reader, and card punch. **Data 100 Corp,** PO Box 1222, Minneapolis, MN 55440.

***See at Booth 2327***
Circle 394 on Inquiry Card

## CRT MONITOR



Offering 1000-line resolution, the 15" series 500 has a digital interface, and can be used for data transmission systems, computers, graphic arts, and graphical displays. Designed with a wire-frame chassis, the monitor can be mounted either horizontally or vertically; other features include dual video and separate blanking, adjustable background resolution without visible retrace, and 50/60-Hz squarewave for line synchronization of vertical frame rate to local line frequency. **Redactron Corp,** 100 Parkway Dr S, Hauppauge, NY 11787.

***See at Booth 3411***
Circle 395 on Inquiry Card

## LINE PRINTERS

Model CT-6644, -6643, -2324, and -2323 ChainTrain™ printers are among the number of heavy-duty chain devices exhibited. Print speeds range from 200 to 760 lines/min., and char sets are 48 to 96 char/line. All print 132 col/line. Typ -2323 unit has single line memory buffer, ASCII char set and coding, modified OCR-B char style, control panel, and self test. **Data Printer Corp,** 600 Memorial Dr, Cambridge, MA 02139.

***See at Booth 2727***
Circle 396 on Inquiry Card

## VOICE DATA ENTRY TERMINAL

Automatically recognizing spoken words, the model 500 can replace or complement intelligent CRT/keyboard stations by allowing data to be entered by voice. Output is in the same format and code as that of a std keyboard terminal, allowing multiterminal voice data entry systems to be used in all applications formerly requiring intelligent CRT/keyboard input stations. **Threshold Technology Inc,** 1829 Underwood Blvd, Delran, NJ 08075.

***See at Booth 1013***
Circle 397 on Inquiry Card


# If low cost and high performance are criteria... our new 82000 Series permanent magnet steppers are the answer.

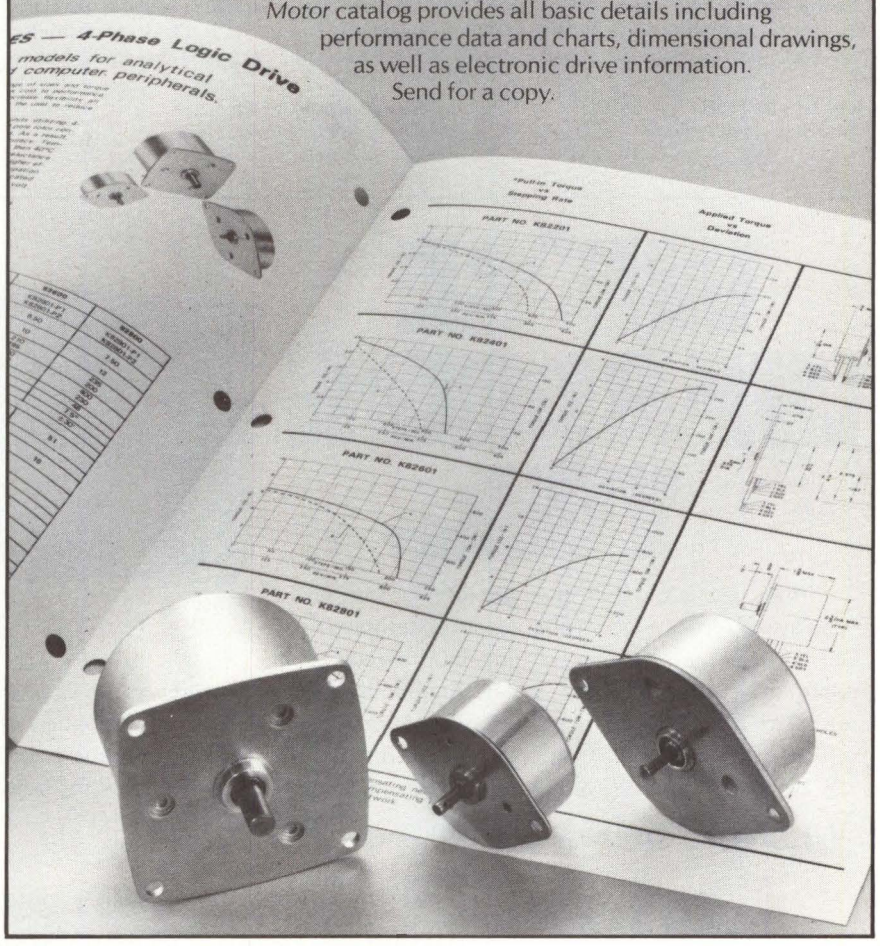
Here's a new permanent magnet stepper motor line created to meet the design needs of analytical instrumentation and computer peripherals. Applications include tape drives, printer and chart drives and optical disc drives. Both 5 volt and 12 volt models are available.

All utilize 4-phase stators and permanent magnet rotors. Most have 24-pole rotor construction. As a result, they offer excellent pull-in rates and good stepping accuracy. Another advantage is low temperature rise...over 50% lower than comparable variable reluctance stepper motors operating on a similar duty cycle. Gear boxes can be furnished to meet varying torque and speed requirements.

*Write for information today!*

Available pull-in torques from .750 oz-in. to 7.50 oz-in.
Available stepping rates from 210 steps/sec to 440 steps/sec.

Our 4-page *Permanent Magnet Logic Stepper Motor* catalog provides all basic details including performance data and charts, dimensional drawings, as well as electronic drive information. Send for a copy.




A.W. HAYDON CO. PRODUCTS

NORTH AMERICAN PHILIPS CONTROLS CORP.

Cheshire, Conn. 06410 • (203) 272-0301

## NCC PRODUCTS

### SYNCHRONOUS TAPE TRANSPORT

Dual-density (45 in./s, 9 track, 800 and 1600 bit/in., NRZI and PE) model 1730 is fully IBM-compatible. Max reel size is 10½"; std tape velocity is 45, 37½, or 25 in./s; max speed variations are ±3% instantaneous, ±1% long term; start/stop distance is 0.19 ±0.02"; and start/stop time is 8.0 ±0.55 ms at 45 in./s. Available configurations include read, write, read/write, and read-after-write. **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, MD 20794.

***See at Booth 1416***
Circle 398 on Inquiry Card

### MEMORY SYSTEM FOR DIGITAL DATA RECORDING

Perifile 6000C provides data I/O with storage facilities capable of interfacing, via a bidirectional data and control bus with handshake, to most minicomputers as well as software drivers and diagnostics. Each unit is a single or double cartridge tape transport system, each cartridge having four independent serial data tracks. Track selection is by logic command. Storage capacity is 2M 8-bit bytes/cartridge. Data transfer is up to 5K 8-bit bytes. **Sintrom Electronics Ltd,** 2 Arkwright Rd, Reading, Berkshire RG2 OLS, England.

***See at Booth 3100***
Circle 399 on Inquiry Card

### DATA MANAGEMENT SYSTEM

An IBM version 2.70 of the System 2000, system provides 2:1 to 4:1 improvement in general processing, both batch and online. Features include multiple virtual storage compatibility, new buffer manager, extended-where clause, enhanced self-contained language processing in multithread environments, additional DBA statistical aids, and an extended procedural language interface COBOL and PL/1 precompiler. **MRI Systems Corp,** PO Box 9968, Austin, TX 78766.

***See at Booth 1115***
Circle 400 on Inquiry Card

### LARGE CAPACITY DISC DRIVE

Capacity of 300M bytes is provided on the Trident T-300 IBM 3330-type drive. Specs include 20K bytes/track, 815 cylinders/pack, 6K-bit/in. and 370-track/in. densities, 1M-byte/s transfer rate, 3600-rpm rotational speed, 8.3-ms avg latency time, 10-ms track-to-track access time, 30-ms avg and 55-ms max access times, and 25-s start/stop times. **California Computer Products, Inc,** 2411 W La Palma, Anaheim, CA 92801.

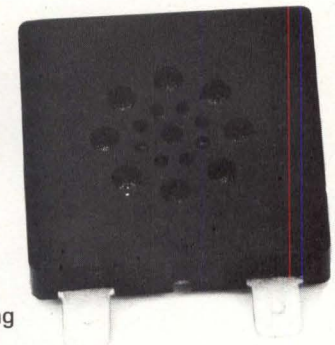
***See at Booth 2243***
Circle 401 on Inquiry Card

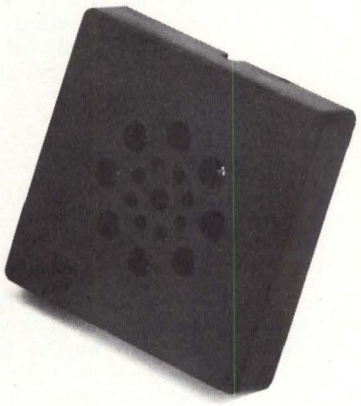
### SEMICONDUCTOR MEMORY SYSTEMS

OEM designs for mini, micro, or custom applications range from 1K x 10 to 32K x 22 planar systems and modular systems with up to 3.5M bits, and include nonvolatile CMOS, in commercial and military versions. Add-in/on systems for DEC PDP-8 computers include a single board, single-slot 8K x 12 memory and a nonvolatile CMOS memory that provides 8K x 12 capacity and has 1-A max power consumption. Both are directly compatible with any /A, /E, /F, or /M. **Monolithic Systems Corp,** 14 Inverness Drive E, Englewood, CO 80110.

***See at Booth 2637***
Circle 402 on Inquiry Card


# WE'RE WARNING YOU...





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Series X-10 Continuous
Series X-11 Pulsing

. . . these new audio indicators are just right for letting you know something's wrong. Ideal for computer terminals, remote control warning, fault detection and alarm devices. Six models . . . featuring 35mm diameter piezo crystal . . . rated to 85 dbA at 3.3 kHz . . . 3 to 16 vdc, drawing just 10 mA maximum current. Supplied with .187 quick disconnect tabs, wires or PC mounting pins. Black . . . 40mm square x 10mm high (X-10), or 15mm high (X-11). Life-tested for at least 1000 hours. Ask for free catalog.

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**OHIO,** CLEVELAND
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**OHIO,** COLUMBUS
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**TEXAS,** DALLAS
K. A. Electronics

**UTAH,** SALT LAKE
Newark Electronics

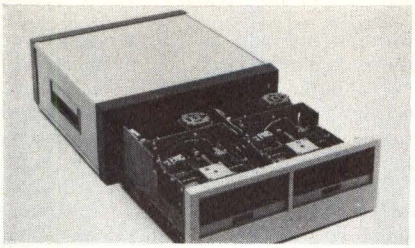
**WASHINGTON,** SEATTLE
Frank Jackson & Associates

**WISCONSIN,** MILWAUKEE
Taylor Electric

**ONTARIO,** WILLOWDALE
Electro Sonic, Inc.

**B. C.,** VANCOUVER
Deskin Sales Corp.

## FLOPPY DISC DRIVES



Model SA800R, the Skinny Floppy, has a redesigned, thinner drive chassis that allows two drives to be mounted side-by-side in a std 19" RETMA rack. A pair of drives can be mounted either vertically or horizontally, or can be used in a desktop version. Basic drive mechanism is the SA800; drives feature single- or double-density recording capability, IBM compatibility, proprietary ceramic R/W recording head, and positive diskette registration system. **Shugart Associates,** 435 Indio Way, Sunnyvale, CA 94086.

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## PORTABLE DATA TERMINAL

Weighing only 13 lb, the model 745 provides true "briefcase mobility" for field access to a central computer. Design includes MPU, MOS/LSI ICs, solid-state printhead, and min moving parts. Std features are selectable 10- or 30-char/s print speed, 5 x 7 dot matrix with print contrast control, built-in acoustic coupler, and half- or full-duplex operation. **Texas Instruments Inc,** PO Box 1444, Houston, TX 77001.

***See at Booth 2115***
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## HEAD-PER-TRACK DISC MEMORIES

Series 700 random-access disc drive is offered in increments of 32 tracks up to 128 tracks. Avg access time is 8.5 ms, nom rotational speed is 3600 rpm, data rate is up to 4.5 MHz, and capacity is up to 19.2M bits. Options include 256 tracks; 38M bits; 2-, 4-, or 8-bit parallel; 150K bits/track; and 1800 or 2400 rpm speed. **General Instrument Corp, Rotating Memory Products,** 13040 S Cerise Ave, Hawthorne, CA 90250.

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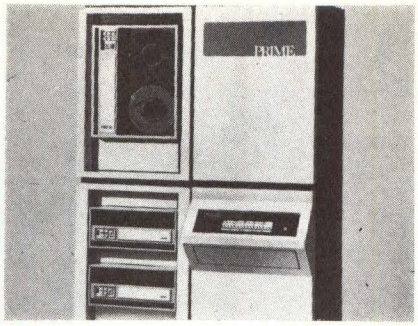
## HIGH LEVEL PROCESSOR

Part of the TEMPUS family of upward and downward compatible computers, the model 400 processor offers 512M-byte virtual memory for each of up to 64 simultaneous users, and is claimed to be competitive with the PDP-11/70 in performance. System features include up to 8M bytes of MOS main memory, 2K bytes of 80-ns bipolar cache memory, and support for online disc capacity up to 1.2G bytes. CREATE IV series configuration to be shown includes a 16-user CPU with 256K-bytes main memory, operator terminal, and communications controller. **Prime Computer, Inc,** 145 Pennsylvania Ave, Framingham, MA 01701.

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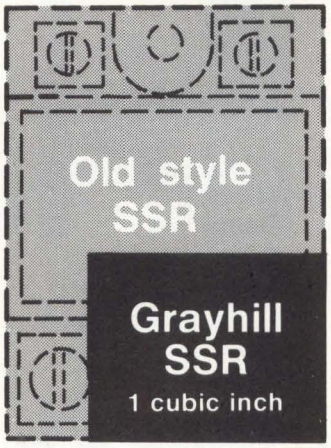
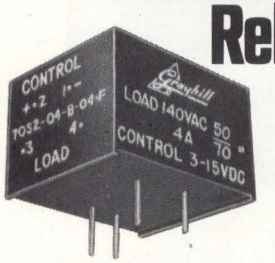



# Grayhill Mini Cube 4 amp Solid State Relays

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# NCC PRODUCTS

## VIDEO TERMINAL

Packaged in separate modules the ADM-2 Executive provides max installation flexibility. Electronics package mounts beneath a desk or countertop, allowing keyboard and screen to be placed for most efficient use; 9" video screen displays 1920 char from the 128-char u/lc ASCII set in a 24-line, 80-char/line format. Keyboard module, top-mounted or recessed, is a 119-key unit with 63 alphanumeric keys, a 10-key numeric pad, 16 function keys, cursor control, and four transmission control keys. **Lear Siegler Inc, Electronic Instrumentation Div,** 714 N Brookhurst St, Anaheim, CA 92803.

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## UNINTERRUPTIBLE POWER SYSTEM

To protect critical process equipment against all types of ac line failures (blackouts, brownouts, flickouts), the 125-kW UPS acts as a continuous monitor/buffer (with reserve battery plant) between the commercial ac power source and the computer. Design guarantees precise, regulated voltage and frequency to the load despite changes on the supply. Std capacities accommodate loads from minicomputers to large data processing installations. **Reliance Electric, Power Systems Div/ Lorain UPS,** 1122 F St, Lorain, OH 44052.

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## COMMUNICATIONS CENTER

Permitting a data communication network to be monitored and controlled from a central facility, tech control centers can be tailored to specific requirements by combining std modules such as EIA and VF patch panels, data line monitors, status displays, and communication test equipment. The center incorporates data line monitor, multipoint tester for diagnostic capability, and eye pattern generator for online monitoring of transmission link. **International Communications Corp,** 8600 NW 41st St, Miami, FL 33166.

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## INTELLIGENT DISPLAY AND STORAGE SYSTEM

Program load and store, information retrieval, and other data entry applications are handled by Delta 4700 system which includes video display terminal and floppy disc, each under microprocessor control. Display terminal with up to 16K bytes of R/W memory is programmable from the keyboard. Keyboard with set of programmable function keys is std. **Delta Data Systems Corp,** Woodhaven Industrial Pk, Cornwells Heights, PA 19020.

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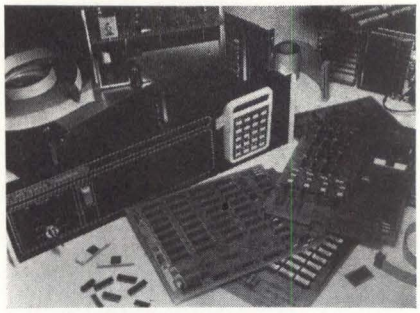
## MICROPROCESSOR-BASED MINICOMPUTER SYSTEM



Built around a company-manufactured single-chip n-MOS microprocessor, the microNova family is made up of mN601 CPU chip sets, CPU/4K single-board computers with 4K-word memory, and fully packaged 9- or 18-slot minicomputer with up to 32K-word memory—plus support and software. An intelligent I/O controller chip addresses up to 61 devices. Full memory cycle speed is 960 ns. Battery backup for MOS RAM data protection is available. **Data General Corp,** Southboro, MA 01772.

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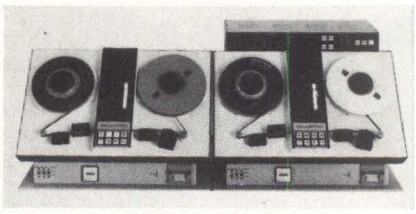
## TAPE EVALUATOR AND COPIER



Upgraded to clean and test computer grade tapes at 6250 bits/s, the evaluator enables tape libraries to certify all tapes for high density applications. The copier is composed of two std 1600 bit/in. evaluators plus an electronic interface linking the two units together. It can copy any 1600-bit/in. tape from one drive to the other, requiring <10 min. to duplicate a 2400-ft reel. **Recortec, Inc,** 777 Palomar Ave, Sunnyvale, CA 94086.

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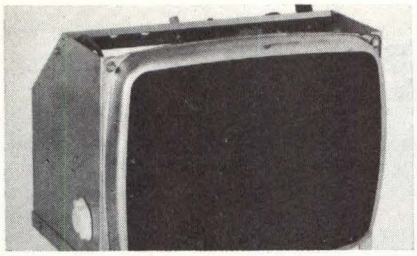
## CRT DATA DISPLAY



Designed specifically for critical display applications, with plug-in circuit boards to reduce downtime and MTTR, the C-925 has a calculated MTBF of >20,000 h. All versions comply with DHEW regulations relating to X-radiation, and components are designed to meet UL stds. The CRT has a 15″ diag, 100-in.² area, 110-deg deflection angle, and center spot resolution of 1000 lines. Power input is 105 to 135 V rms, 50/60 Hz, 60 W nom. **SC Electronics, Inc,** 530 5th Ave NW, New Brighton, MN 55112.

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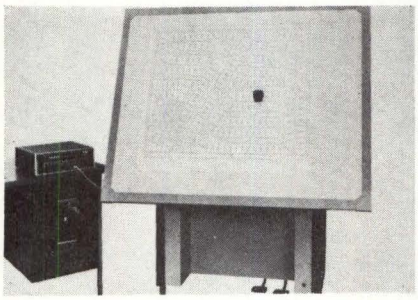
## INTELLIGENT DIGITIZER



This self-calibrating model includes a built-in microprocessor which continuously monitors the digitizing process, assuring high linearity and accuracy. All modes—point, stream, and remote—may be operated incrementally, providing X-Y data output only when values change. A front panel switch permits user selection of origin anywhere on the tablet surface. The microprocessor also permits stand-alone operation of the unit. **Summagraphics Corp,** 35 Brentwood Ave, Box 781, Fairfield, CT 06430.

***See at Booth 1826***
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## LINE PRINTER

Rated at a speed of 2250 lines/min. (single spaced, using std 48-graphic char set), the DOC 2250 is TTL/DTL compatible. Std line width is 132 print positions (150 optional). Vertical spacing is 6 or 8 lines/in. Four std bands with 0.095 x 0.083″ char use 48-char commercial or scientific, 60-char PL/1, and 63-char ASCII fonts. Other graphics and char arrangement are optionally available. Sound level is 74 dBA. **Documation Inc,** PO Box 1240, Melbourne, FL 32901.

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## DIGITAL CASSETTE

Critical dimensions of the H-series cassette are controlled over wide ranges in environmental conditions through use of appropriately matched materials. Lexan™ polycarbonate used in cassette shells provides protection from cracking from thermal or mechanical shock. Tape guides are precision-machined for friction-free tape motion, and a patented ribbed slip sheet assures controlled tape winding, uniform tension, and optimum tape guidance. **Information Terminals Corp,** 323 Soquel Way, Sunnyvale, CA 94086.

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## INTELLIGENT TERMINAL SYSTEMS

Software-controlled SPD 20/20 multistation display system is built around a 32K-byte processor powering a flexible combination of video terminals, printers, and other peripherals, and is compatible with the IBM 3270. System stores forms at the data entry site available for retrieval at all times by a terminal operator. Users can add components as needs grow and alter functions as the environment changes. **Incoterm Corp,** 6 Strathmore Rd, Natick, MA 01760.

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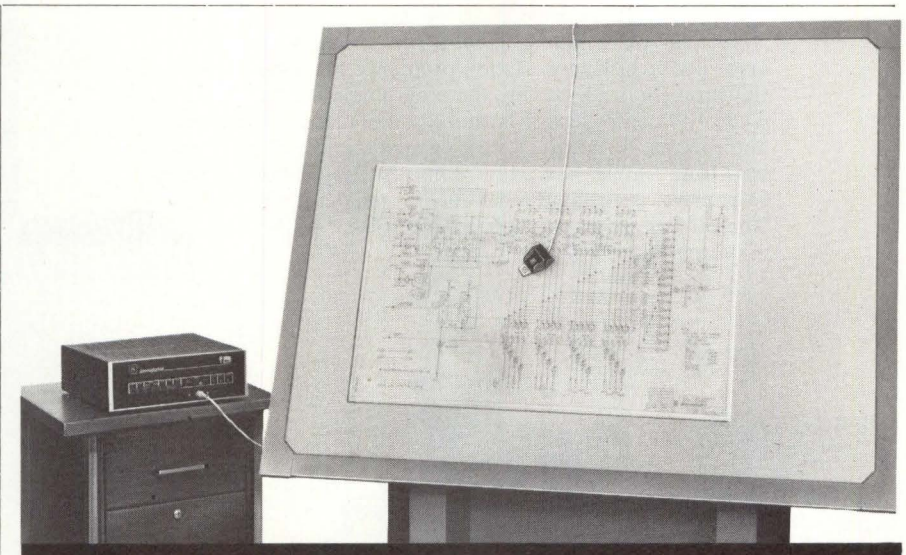

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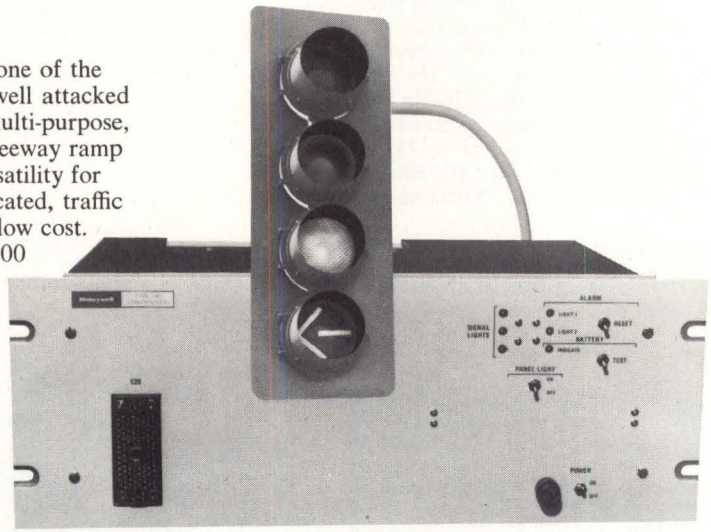
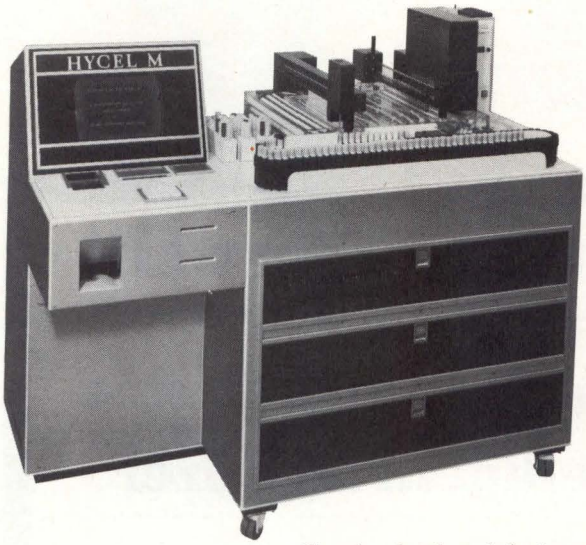
# They mastered new design concepts with Motorola's M6800 Family.

## HONEYWELL

Vehicular traffic management is recognized as one of the great practical transportation problems. Honeywell attacked this problem head-on, with the programmable, multi-purpose, Type 140 controller for both intersection and freeway ramp applications. It has the speed, capacity, and versatility for uses from simple, fixed, time control to sophisticated, traffic responsive, centrally directed operation, yet it's low cost. The central processing unit is Motorola's MC6800 microprocessor.



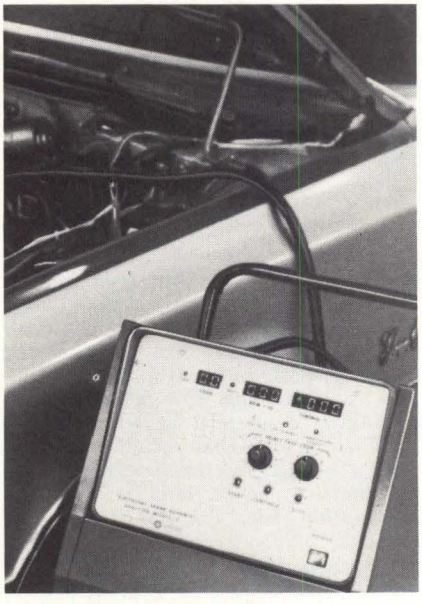



## HYCEL

It's a desk-size, 30-channel, automated blood analyzer for medical laboratories. It performs over 3,000 tests per hour, selectively and sequentially, while continuously tracking patient identity and sample status. It's fast. Maximum test time is ten minutes, from sample pickup to completion. The HYCEL M is big news in the medical test instrument field, and HYCEL calls it the "ultimate analyzer." All machine functions are automatically controlled by the instrument's Motorola's MC6800 microprocessor.

## CHRYSLER

Chrysler developed the lean burn system to permit engines operating in their cars to meet emission standards without catalysts, while giving improved fuel economy on either leaded or unleaded gas. Servicing this innovative system also called for an innovative new concept in diagnostic testing. Chrysler has called the MC6800 microprocessor based portable diagnostic tester they designed to meet this challenge "an ideal service tool," for its versatility and economy.



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***Engineers more familiar with applications than with computers depend less on expert assistance to computerize their designs when a microprogram-based architecture is available to them***

# Architecture of Aerospace Computer Simplifies Programming

**H. Clifford Kancler**

Lockheed Missiles and Space Company
Sunnyvale, California

An unusual architecture, developed in conjunction with the design of an aerospace computer for missile control, offers a method of designing a problem- or programmer-oriented instruction set for a variety of applications, while allowing more concurrency in developing different subsystems within the architecture. The approach gives the microprogrammer responsibility for all hardware interfaces, on the assumption that he is best qualified to design them; while the user-level program can develop almost independently.

The computer is conceptually simple—a considerable advantage in an engineering organization where the primary concern is the design of autopilots. The design was purposely made so that systems engineers conversant with a high level language could understand it. Details of programming the machine do not transcend the problem to be solved.

The machine's application is to control events and stabilize a missile through many diverse modes of flight. It receives digital attitude and timing information serially from a guidance and navigation computer and rate gyro information from analog-to-digital (A-D) converters. It provides serial digital information to a number of packages, parallel information to thrusters, and analog information to various servos. Sampling frequency for control purposes is 100 Hz; during the 10-ms interval between real-time interrupts, approximately 2500 instructions are executed. Control algorithms are complex, using digital filters, integrators, optimum gain selection, and various types of limiting and compensation.

Efficiency and simplicity were important initial considerations in the design. It was essential to retain maximum flexibility as late in the development phase as possible.

Key aspect of the design is a microprogrammed processor that executes variable-length instructions composed of strings of 4-bit bytes. (Although the term byte generally implies eight bits, it is used here to denote a unit of information larger than a bit—in this case four bits.) This approach has two advantages: it permits a programming language containing equation-like, problem-oriented instructions, instead of symbolic abbreviations, to be defined; and, because of the general nature of the instruction register mechanization, it does not require any aspect of the instruction repertoire, including its format, to be committed to hardware until the microprogram is supplied. The instruction set is expandable and each instruction uses an amount of memory proportionate to the information it contains.

A second aspect of the design makes the hardware's logical construction invisible to the programmer. Instruction set and input/output (I/O) are memory oriented and transparent to each other. No particular hardware is implicit in any instruction. This is analogous to a high level language; the programmer who uses it does not know how the compiler will create and

execute code. With the language defined in this machine, the programmer has exact knowledge of the compiled code, yet does not need to understand the machine's construction in order to solve his problem efficiently.

## Hardware Architecture

The microprogrammer, on the other hand, must know how the machine is constructed, what major hardware components are under microprogram control, and their connectivity (Fig. 1). Each microinstruction is encoded only to the level where it can directly drive medium-scale devices such as multiplexers, but nevertheless is wide enough (48 bits) to allow considerable parallel activity.

One of the most important registers is the instruction register. It is 24 bits, or six bytes, long; can shift left either one or three bytes; and can load the upper, middle, or lower four bytes from memory while preserving the two remaining bytes. The byte counter indicates the number of null bytes by counting the number of shifts. It is driven by the same signals that shift or load the instruction register. A typical microprogram sequence can be thought of as removing information from the left end of the register in 1- or 3-byte chunks and inserting null bytes at the right. When the register contains four or more null bytes, as indicated by the byte counter, a fetch sequence inserts four valid bytes and decrements the byte counter by four, if enabled by the microprogram. Thus, the instruction register supplies an apparently endless string of bytes to the microprogram.

The microprogram may temporarily inhibit the fetch sequence, if its execution would disturb an operation in progress. Most operations, including the fetch sequence, utilize one or more of eight processor registers, including the program counter, in accordance with microprogram assignments. Therefore, when such operations are underway, the fetch sequence is disabled.

The program counter and two other functions are given fixed register-file assignments by the microprogram. The other five have no dedicated function but

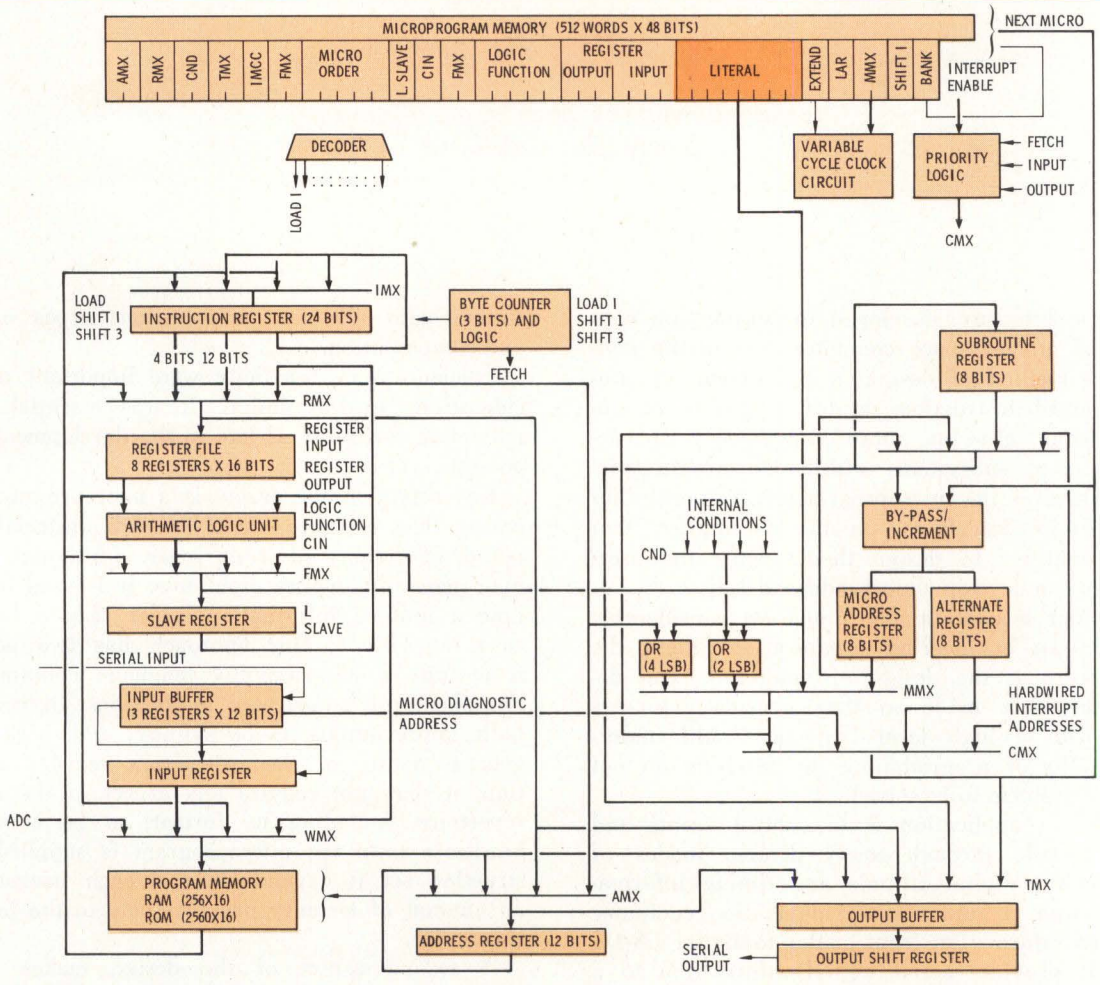


Fig. 1 Aerospace processor. Data flow along paths indicated here, in widths of 4 to 16 bits. Routing and sequence are controlled by microinstructions, which control use of register file (not accessible to problem program). Literal micro-operand (dark color) in microprogram memory (top block) tests conditions arising during instruction execution, controlling sequence of operations accordingly. Coded blocks control flow of data between registers; eg, AMX (first two bits of micro-operand) admits address to address register, TMX (bits 7 and 8) gates data to output buffer, etc

are used as temporary storage locations by different instructions, pending transfer of the instruction's result to memory at the instruction's end. This temporary nature is quite important, because the I/O mechanization requires extensive processing capability. For example, the digital input is a 48-bit serial word from which three 12-bit words must be parsed, converted from 1's to 2's complement, and stored in locations specified by the remaining 12 bits. This type of activity can be accomplished at an instruction's end in the temporary registers.

Memory contains only semiconductor elements, organized in 16-bit words—256 words of read/write memory and 2560 words of read-only. The total, 2816 words, requires a 12-bit memory address register with a range of 4096, only part of which is occupied. The 1280 invalid addresses lie between the two memory areas.

Logic that controls microinstruction sequencing consists of a microaddress register, the source of microaddresses for executing instructions; an alternate register, the source of microaddresses for executing I/O; and a microsubroutine register, which establishes a hierarchy for using microsubroutines, as shown in Fig. 2. Microprograms can be two levels deep in executing instructions and one level deep in I/O.

An alternative source of microaddresses is the literal field of the microinstruction (dark color in Fig. 1). This field may be used directly as a jump address, or may test internal conditions with a logical OR, producing multiway jumps depending on their statuses.

The rightmost four bits of this literal field test the most significant byte of the instruction register at the start of every new instruction, and occasionally in the midst of more complex instructions. This test takes place just as the previous instruction concludes. At this moment, the most significant byte of the instruction register contains either the operation code for the next instruction, or a generic code that identifies the class of the next instruction. One such class, for example, is that of logical operators AND, OR, exclusive-OR, and so on. Generic code is followed by a series of bytes used as operands, along with a byte that distinguishes or further isolates the class.

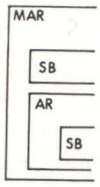


Fig. 2 Microsubroutine nesting. Microinstructions can call two levels of nested subroutines in any kind of operation except input/output, where one level is available

## Microdiagnostics

Microprogrammed design lends itself particularly well to microdiagnostic testing. One serial input word creates a real-time jammed interrupt to start the mission program. This word contains an incrementing time field, six bits of which specify one of 64 jammed microaddresses. Each of the 64 starts a microdiagnostic, which runs just prior to the mission program and puts a hardware test result into the output buffer. This is entered serially into a telemetry channel. The probability of running a diagnostic and getting a meaningful result is quite high, since very little of the processor is inaccessible to this type of testing.

## Input/Output

Input/output connects the program with the outside world entirely through memory. There are no instructions related to I/O. Instead, incoming data go directly and automatically to certain prescribed locations in the scratchpad area of memory, while output data are placed by the program anywhere in the scratchpad area and directed to their external destinations by instruction-like definitions stored in an area of memory called the output list.

Any I/O interrupts are processed by the microprogram between instructions. There are three types of interrupts. One is a housekeeping interrupt at 4800 Hz; this is internally generated by counting down an external clock, which is the time reference for all communication. The other two, derived from serial inputs, are data interrupts to memory and jump interrupts which jam the program counter. Data interrupts received in flight have preassigned addresses at the digital input area and at the real-time program start location (Fig. 3). Data interrupts, received on the ground before launch, are more general, and can load or jump to any location. The real-time jump interrupt, which is repeated at 100 Hz, synchronizes the 4800-Hz housekeeping interrupt to the program. Certain of its functions, such as sequencing the A-D converter, are preassigned; others can be defined by the programmer in the output list, which has a capacity of 48 words. As shown in Fig. 3, words on the output list consist of an operation and an address. Of the 48, 47 are instructions telling the interrupts where to send their data. Output of the last interrupt in the list is the memory sum, which is replaced in the serial output stream by a diagnostic word if the real-time interrupt occurs. The programmer places these instructions in the output list to send data placed in scratchpad memory to external devices. His only real constraint is timing the output list so that critical data are sent out soon after they are computed. The timer word, which is in memory location 50, aids this process by indicating the interrupt which last occurred (1 to 48 repetitively). The programmer temporarily includes provisions in his program to sample the timer word at the worst-case end of every critical computational path. This sample specifies the lowest numerical position which the variable can occupy on the list, if it is to be output immediately.

Although the A-D converter sampling schedule is automatic, its mode can be controlled by setting bits in the discrete word (location 49). In self-test mode, all 32 inputs are analog. In flight mode, there are only five analog inputs; the other 27 are received directly

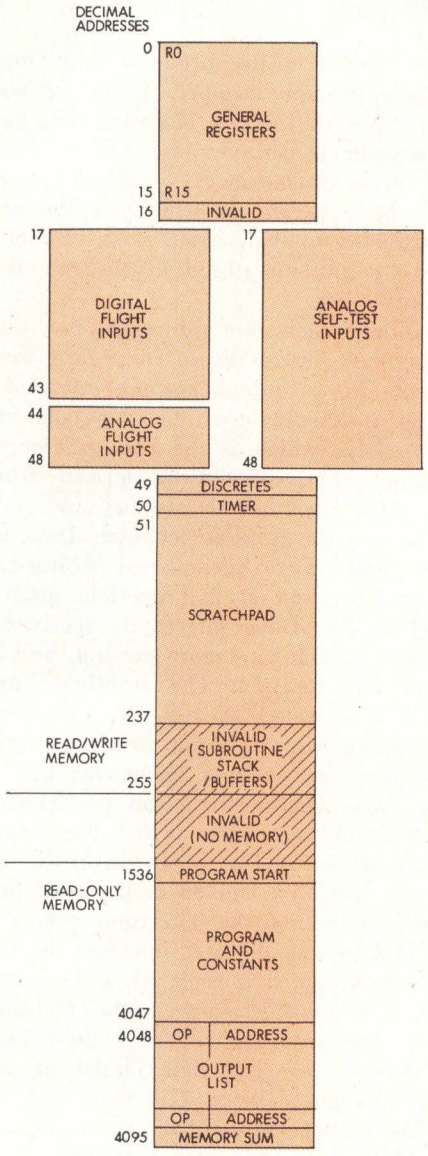


Fig. 3 Memory map. Locations are dedicated to their respective functions by the microprogram; the programmer is constrained to use them this way. Words 17 through 48 are used one way during testing, and another way during missile flight, as described in text

in digital form. The discrete word is another means of external communication. Some of its bits are sampled from external conditions and may be tested by the program; others, set by the program, control outputs and are latched by the 4800-Hz interrupt.

## Software Architecture

The programmer's view is of a virtual computer, specified by the memory map (Fig. 3) and a list of allowable operations in symbolic form. On the map, the first 16 memory locations are general registers in which all arithmetic operations and comparisons are performed. All programs move data from other memory areas to the registers and operate on them there. The simplest (dyadic) instructions move data by equating two symbolic identifiers that point to the data register. More complex forms use subscript notation to reference registers used as indirect addresses or indices. There are also vector instructions for economical and rapid transfer of arrays between registers and memory, and immediate instructions with operation code and operand in the same word.

Because of the symbolic source-code input, the program which converts source to object code is called a compiler rather than an assembler, even though, unlike most compilers, it inserts no extra code. It is a cross-compiler written in FORTRAN and running on a Univac 1110. Cross-compilation is important in developing an instruction set of this sort, as it is doubtful that self-compilation would be possible with the small memory available.

The requirement to perform arithmetic operations in registers and to use dyadics to get data there encourages the programmer to optimize his registers. Dyadics could have been inserted by the compiler; however, having the programmer do it makes him aware of his overhead. Thus, he develops a tendency to consolidate variables in the registers and to map this information from one program segment to the next. Sixteen general registers seem to be sufficient to contain the variables pertinent to routines we have encountered.

Very general operations are allowed on data in the registers. Instructions have two formats: short fixed-length formats, which include logical operations, and the variable-length arithmetic string, which is limited to purely arithmetic operations.

Five kinds of fixed-format functional instructions (Fig. 4) (a) transfer data from one register to another while incrementing or decrementing it; (b) complement or change the sign of data being moved; (c) shift data within a single register a prescribed number of bit positions; (d) perform conventional arithmetic and logical operations on the contents of two registers and move the result into a third; or (e) sum or difference a product.

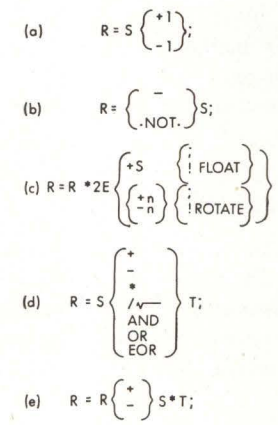


Fig. 4 Fixed-format instructions. Most of the instruction set is represented in this diagram and in Figs. 5 and 6. R, S, and T are shorthand for any general registers

Arithmetic string format (Fig. 5) is very powerful. It can show operations on any register (designated R), on a specified number between 0 and 15, or on an element of a numerical array. Such an element of a one-dimensional array is designated in the form R(S), where S is a subscript, as in FORTRAN. Effective address of R(S) is the address of R plus the contents of address S. Operations that can be performed include addition, subtraction, and multiplication, along with arithmetic shifts to left and right.

The format's only significant limitation is the lack of a hardware stack, as indicated by the first example in Fig. 5, which shows the formation of the sum of two products. To perform that instruction, a single instruction would require a stack register for temporary storage of an intermediate result, p (one of the products); since a stack is not available, the compiler rejects the instruction as invalid. In a real application, it would have to be replaced by instructions that form products and sum separately.

Fig. 5 also illustrates two valid examples. The first illustrates bit packing; it shifts a word four places to the right, then left four places, zeroing the rightmost bits, then setting those bits to 0101 (5). The other multiplies an element of array X(I) by the contents of register S, subtracts the resulting product from the contents of register R, shifts that result to the left as many bit positions as are specified by element T(J) in another array, and, finally, stores the shifted number as element P(K) of a third array.

In a program, the minus operator is always written between the two operands upon which the subtraction is performed, as in conventional algebraic notation (a — b). In the assembled code it may appear following the two operands in two forms, depending on whether or not a multiply is more deeply embedded. In the example, a reverse representation appears.

Although the short forms could all have been implemented in the variable-length arithmetic string format, which requires from six to eight bytes, 4- or 5-byte fixed-length formats were chosen for efficiency. Short forms are used frequently, since one or two bytes of

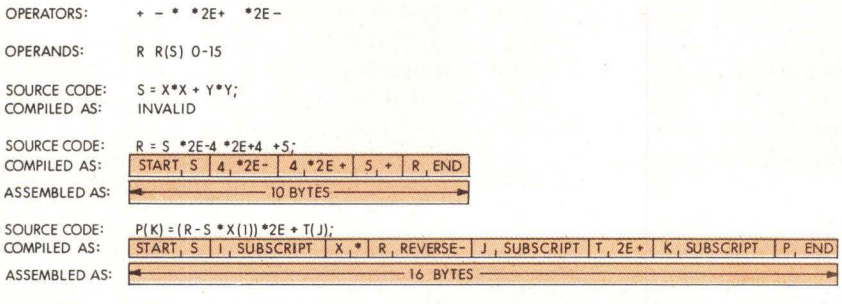


Fig. 5 Arithmetic string format. Any arithmetic expression that can be expressed as a chain calculation (ie, without implied or explicit un-nested parentheses) is valid. Each operator must be paired with an operand; minus operator may appear before or after its operand. These three examples are described in the text

memory, as well as fetch and execution time, are saved over the long form each time one is used. Furthermore, in the IF instruction, which says

"IF 'condition' THEN 'operation' ELSE 'operation',

the short form fixes the two operation fields at five bytes, while still covering the most frequently used operations, including dyadics. These two factors represent about a 10% saving in instruction memory.

The IF instruction has a number of possible variations (Fig. 6). All compare the contents of two registers, or the contents of one register with a specified number between 0 and 15, for equality or inequality, in either direction.

Other instructions are the 4-byte GO TO and CALL, which can have any address, and IDLE; a 1-byte instruction is RETURN.

## Choice of Instruction Set

Implementable repertoire is completely a function of the microprogram, not the word length of the memory. For our application, the 16-bit, single-precision, fixed-point number system dictates a number of attributes of the instruction set. One, for instance, is good shift capability for scaling. Another is the use of single instructions to cover a variety of arithmetic needs; eg, the inverse-square-root which combines division and root extraction without overtly performing either operation. Although its normal function is

$$Z = \frac{Y}{\sqrt{X}}$$

by proper choice of operands, the same instruction can compute the square root or the quotient.

With the IF instruction, variables can be compared directly to other variables, rather than being subtracted from them and the difference tested against 0. Direct comparison is important in fixed-point arithmetic, because it avoids testing for an occasional overflow, which could occur when subtracting two large, oppositely signed numbers. It also avoids the need for a temporary register to contain the result of the subtraction.

Because less hardware and memory are needed when only whole-word addresses are used, the variable-length instruction set requires a 1-byte no-op instruction. This is useful in a transfer or branch, where the target instruction immediately follows an instruction that does not end on a word boundary. No-ops must be inserted between them so that the first byte of the target instruction is at the next whole-word boundary. Similarly, no-ops are useful after a CALL statement, which branches to a subroutine, so that the RETURN from the subroutine is directed to a whole-word boundary. Also, the compiler inserts no-ops to insure that the THEN and ELSE clauses of the IF instruction are a full five or six bytes long. No-ops are wasteful because they occupy memory and take time to fetch and "execute"; but in our flight program they take up less than 4% of the instruction memory and save more than they use.

## Implementation of Instructions

Some considerations in design and implementation of instructions are illustrated by the IF. The compiler produces and assembles an IF instruction in memory from the initial source code in a straightforward way (Fig. 7), substituting bytes that supply information about the instruction's format, shown as hexadecimal characters in the assembled string. Bytes specifying general registers are shown as X, Y, or Z, but are assigned a particular hexadecimal value at assembly time. The either/or character implied by the reserved words THEN/ELSE is achieved by interpreting the ELSE (hexadecimal E) as a 5-byte skip whenever it is encountered. This interpretation produces execution sequences for both a TRUE and a FALSE condition, shown in the lower portion of Fig. 7.

Aspects of formatting and implementation of instructions demonstrated by the IF include assignment of formats and their mapping into microprogram memory, ordering of operands with regard to their sequence of use, commonality with other sequences to conserve microcode, and optimization of frequently used instructions (Fig. 8). In the flowchart of the IF (Fig. 8), boxes represent microinstructions. The colored portion is an instance where the condition is found to be TRUE and the THEN clause Z = X is to be executed. Consequent instruction register activity is also shown. Hexadecimal microaddresses are shown above each box. If a logic condition is required to invoke a particular microinstruction, it is shown underlined at the top of the box.

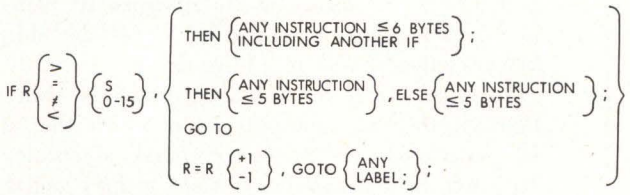


Fig. 6 IF-THEN format. Conditional instruction may be the basis for another instruction, a choice of two others, or a branch with or without indexing

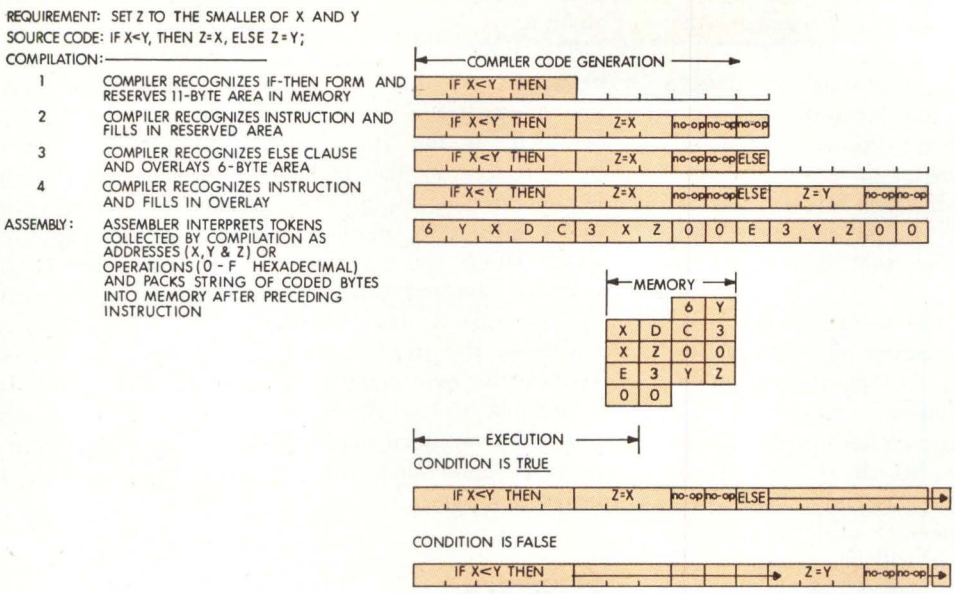


Fig. 7 Typical instruction compilation. Instruction is converted from high level non-mnemonic form to string of bytes in step-by-step fashion. When executed, any step based on an unfulfilled condition is simply skipped

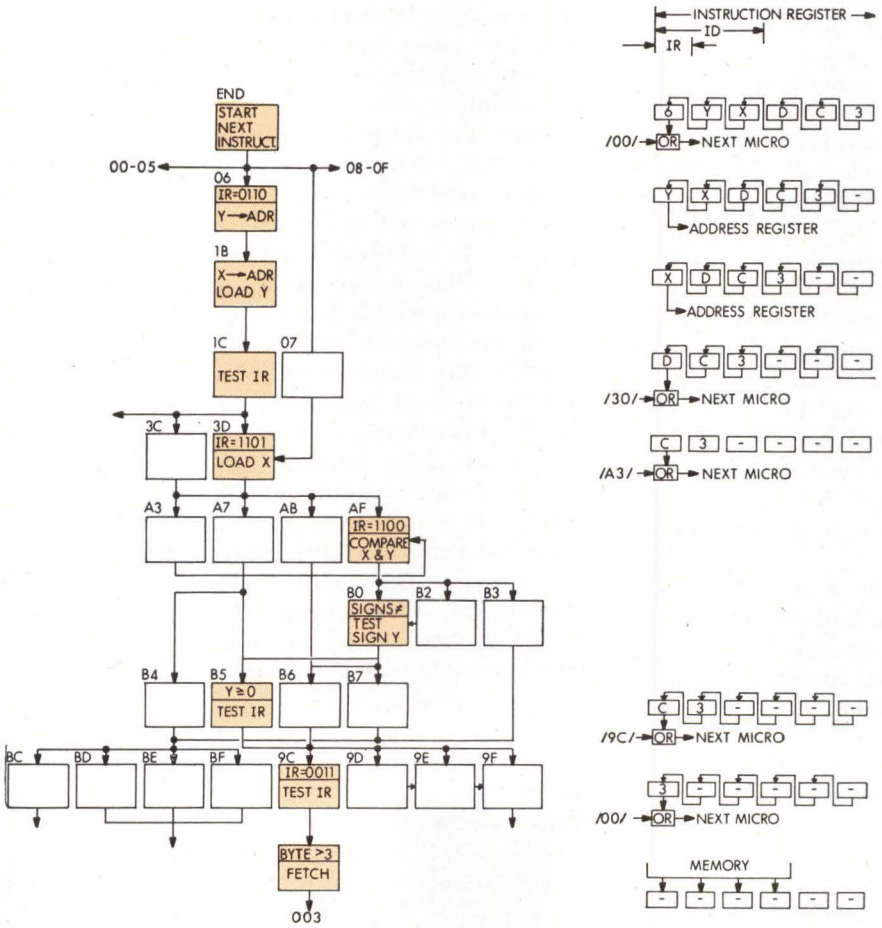


Fig. 8 How microprogram controls execution. Bytes of instruction are inspected one by one as they arrive at high order end of instruction register. They cause certain steps to be taken by processor. If a branch is implied, the byte is tested against the current microinstruction's literal field to specify the correct sequence

Each instruction is responsible for removing its own string of bytes from the instruction register and starting the next instruction. This is done by testing the most significant byte of the instruction register (the op code) with the literal field of the current microinstruction, using an OR gate, as mentioned previously. When an instruction is ending, the terminating microinstruction's literal field is always $00_{16}$ (a string of eight binary 0's); therefore, the OR of this literal and the op code is simply the op code. This forces a branch to one of the first 16 locations in the microprogram, which contains the first step for that instruction or that class of instructions.

In the example, op code for the IF instruction is 6; therefore, the first step in executing this instruction is in microprogram location 06. (All microprogram locations are in hexadecimal notation.) As this microinstruction is picked up, the instruction register shifts left, bringing in the next byte, which is the address of Y, one comparand of the IF. The microinstruction transfers this address to the memory address register, and a memory cycle begins; it will place the actual number Y in one of the file registers, which are not accessible to the programmer. Again the instruction register shifts; the address of X appears and is transferred to the memory address register. These three microinstructions, in locations 06, 1B, and 1C, are common to all instructions that use two operands.

At this point, 16 different things could happen. In our example, the byte following X is a hexadecimal D (binary 1101). This means that the two preceding bytes have specified registers whose contents are to be compared. If, for instance, X were followed by C, it would mean that location X contains a number to be compared against the number Y. The other 14 possibilities specify arithmetic operations. To establish what action is to occur, the byte following X is tested as before. This time the test is against $30_{16}$, and, as the outcome of the test is 3D, a branch takes place in the microprogram. The microinstruction in 3D places the contents of X in one of the file registers.

As shown in the flowchart, 3D can be reached by another route, which is followed when the first byte of the instruction is 7 (and the microprogram sequence begins at 07). This is the instruction that compares the contents of a register with 0; it is used frequently enough to justify its own shorter, faster format. The separate sequence saves memory and time, and illustrates the type of optimization that is possible with this design.

Following the D is a C, which again is tested. This byte specifies the kind of comparison to take place—equal, unequal, less than, or greater than—and what to do if the comparison succeeds—branch immediately, branch after incrementing or decrementing a register, or execute another instruction (the THEN part of the IF instruction). The test is against a hexadecimal A3, or binary 1010 0011, which effectively masks the two lower bits of the byte and tests only the two upper bits to establish the comparison. Here the test of C by A3 yields AF; the microinstruction in location AF calls for the "less than" comparison. Byte C remains in the instruction register so that its other two bits can be tested in due time. Since, in our example, the comparison shows that X is indeed less than Y, the microprogram proceeds to check their signs, and then to look at the other two bits of C (by a test against hexadecimal 9C) to find out what to do about it.

The remainder of the microprogram sequence is not shown in the diagram. However, in the long run, it sets a register Z with the contents of register X, as specified in the programmer's instruction. The last byte it sees in the immediate sequence is 3, which is the op code calling for the contents of a register to be moved to another register; however, before it knows which two registers are involved, it has to fetch more of the instruction from main memory, because the op code 3 was the sixth byte and the only one left from the previous fetch. This fetch is necessary because the byte counter contents are more than 3; it is possible because the relation between X and Y, which previously occupied part of the file register, has been determined, and they may now be overlaid with new instruction bytes.

## Summary

Our approach was to concentrate the most complex design features in the microprogram, rather than in software or hardware. Instruction set, I/O, and diagnostic tests each occupy about one-third of the microprogram memory and are approximately equal in complexity. Very few developmental changes in software have affected the hardware, or vice versa, because the microprogram is more representative of the architecture than any other part of the machine. Changes in the outward conception of the machine have consequently been absorbed there.

From the software viewpoint, coding is painless. Production programs approach high level languages in their readability. The intensive nature of the general registers and the dyadic overhead force the programmer to route his data and argument passing in the most efficient way. As a result, he is usually aware of possible tradeoffs between time and memory, which would be masked in a high level language. One difficulty has been visualizing all the data in the general registers at any point in the program; indeed, this has been the major source of program bugs. Visualization has been improved and bugs reduced by a documentation program that presents the data in the registers in signal-flow-graph form.

Microdiagnostics have been valuable in hardware development. They give a degree of fault isolation unobtainable with instruction tests, particularly since the instruction set purposely makes no express reference to any hardware except memory.

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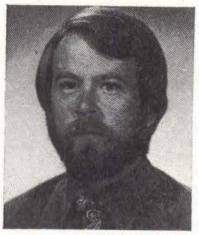

*Clifford Kancler received a BSEE from Rensselaer Polytechnic Institute and an MSEE from the University of Santa Clara. He is currently responsible for software and firmware development within the Guidance and Controls Dept at Lockheed Missiles and Space.*

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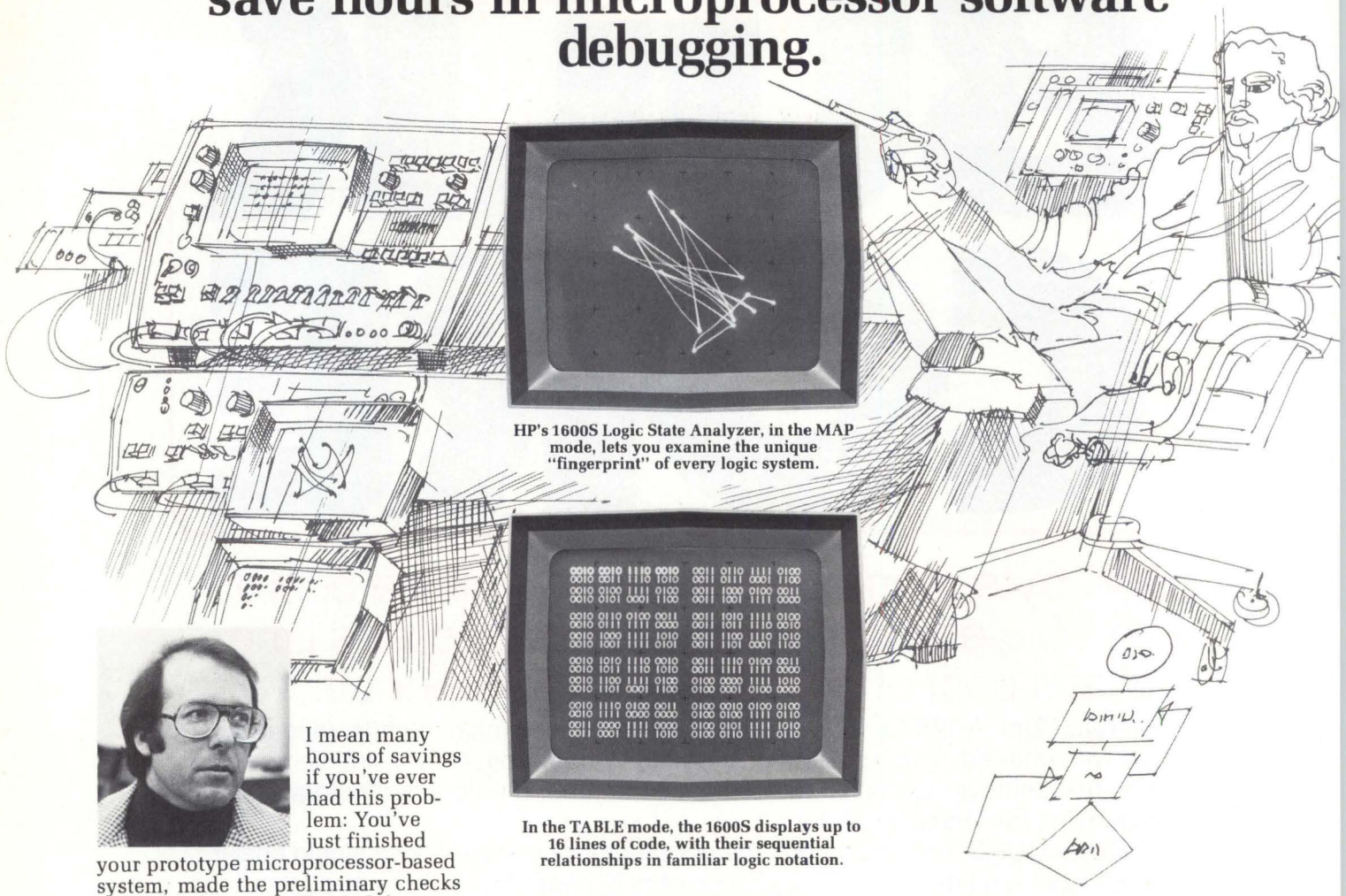

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***Memory tests are often time-consuming, especially when a "map" of the cell layout is not available. This approach to testing locates many serious faults in a reasonable time***

# Moving Inversions Test Pattern Is Thorough, Yet Speedy

**J. Henk de Jonge and Andre´ J. Smulders***

Philips Data Systems
Apeldorn, The Netherlands

To be certain that potential weaknesses are uncovered by a memory test, the internal structure of the device must be known and test patterns must be devised to exercise any weak points that exist. If the internal structure is unknown, using a wide variety of patterns may locate the weaknesses,[1] but may require a substantial amount of time. In the event that few or no faults are located by the test patterns, that time is wasted.

A moving inversions (MOVI) test pattern is a good compromise since it has the best features of many previously devised patterns, but does not require an inordinate amount of execution time. MOVI includes both functional and dynamic tests. Functional tests insure that no memory bit is disturbed by a read or write action on another unrelated memory bit; dynamic tests calculate the worst and best access times, and require the knowledge of which address changes impose these times. Because the data pattern in the memory area may influence performance and functional reliability, it can also be important to both tests.

The MOVI program uses fewer tests to check possible interactions as much as, if not more than, other test patterns, such as the walking zero/one and the galloping test patterns. Its name is derived from its internal process, in which a field of 0's is inverted to become a field of 1's, and vice versa. This inversion is caused by a sequential selection of the addresses and the write action at those addresses. Main characteristics of the MOVI program are placing each write action between two read actions, and generating the addresses in different sequences.

## Program Description

In principle, the MOVI program inverts the data of each address sequentially, thus creating an access time by the jump from one address to another which contains different information. To measure access times, the data of each address are read before and after inversion. This requires three operations on each address: a read, a write, and another read.

However, inversion by itself is not sufficient to create the correct address jumps. Therefore, the read/write/read operations are performed with both forward and backward address sequences, and also with n orders of the address-bit significance (where n is the number of address bits).

Total number of tests performed by the MOVI program is $12 \times B \times n \times 2^n$, where n = number of address bits, and B = number of data bits in each word. A program is started after loading the memory with 0's. The n address bits indicate up to $2^n$ words in the memory, each of which is cycled three times: first the word at each address is read and verified to be all 0's; then a single 1 is substituted in one bit position and the altered word is written back into the same location; and finally the word is reread to verify that the newly entered 1 is still there. This procedure is repeated for each of the B bits per word, accounting thus far for $3 \times 2^n \times B$ cycles, leaving

*Mr Smulders is currently employed by Famatra and Mr de Jonge is with Big Dutchman International.

the memory filled with 1's. This again is repeated, plugging 0's back into the memory; and repeated twice more with 0's and 1's but reading the words in reverse order from $2^n - 1$ down to 0. At this point the number of cycles taken is $12 \times 2^n \times B$.

The remaining factor of n is accounted for by repeating this whole series of tests n times, using a different bit of the address each time as the least significant bit for incrementing through all possible addresses. This has the effect of incrementing through all the addresses by 1's, by 2's, by 4's, by 8's, and so on; every overflow generates an end-around carry, so that all addresses are tested once in each sequence.

Some of these sequences are addresses illustrated in Fig. 1; the whole test sequence is outlined in the colored part of the flowchart (Fig. 2). A similar sequence, if desired, can insure that all previously altered locations retain their revised contents and that locations not yet specifically altered retain their original contents (uncolored blocks in the flowchart).

The MOVI program has fewer cycles per test than the galloping test pattern (Galpat) for addresses of more than four bits. Galpat requires $(2 \times 2^{2n} - 2^n) \times B$ cycles, of which some $(2 \times 2^n) \times B$ are write cycles. Reduction in the number of cycles comes about because the MOVI program uses a method of address generating that creates a number of fundamental jumps and tests them. These fundamental jumps are created by switching each address bit with all states of the other address bits. Switching is performed by counting the addresses with each order of significance, and by generating fundamental jumps in a backward direction—whereas, with the galloping program, all possible jumps are tested.

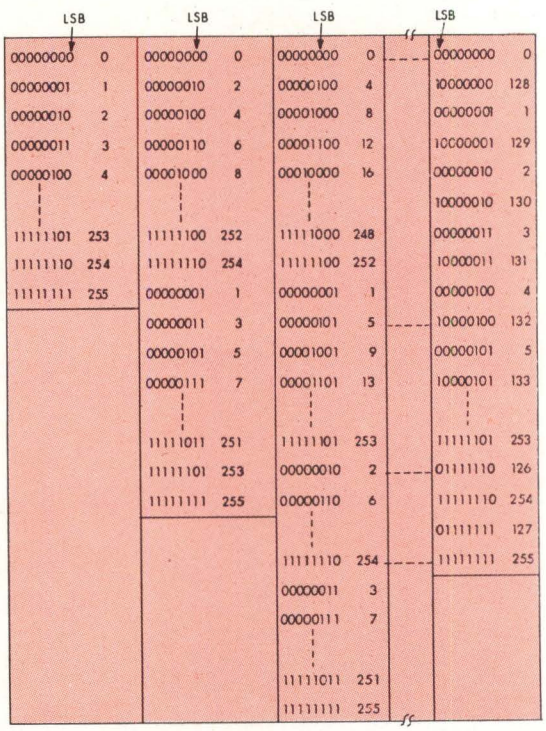


Fig. 1 Address sequences. By cyclically rotating the identity of the least significant bit (LSB), different sequences are created

## Test Strength of the MOVI Program

*Functional.* MOVI can test for address selection failures caused by a fixed address bit, uni- or bidirectional coupling between address bits, or an address bit that does not work in one state. It also tests for fixed memory bits, uni- or bidirectional coupling between different bits, and uni- or bidirectional coupling between rows or columns in the memory matrix. Both of these are functional tests. Whatever stage the test program is in, the memory bit under test is the inverse of the previous bit before the write action, and of the following bit after the write action. Thus, if all addresses are sequentially selected, any of the previously mentioned failures will aways be detected. Construction of the MOVI program ensures that address or memory bits are not connected in one direction (eg, via a diode). Once the test program is running, the addresses are selected in the reverse sequence as well as the normal sequence, thus detecting any incorrect connection.

*Dynamic Behavior.* The read/write/read pattern provides two sequential read operations at different addresses with different data. This measures the access time with the transition from one address to another (Fig. 3). No other test program, such as walking 1, contains this feature. Access times can be distinguished for four situations, because addresses are generated in the forward and backward sequence for both 1's and 0's (Fig. 4).

An arbitrary access time is determined in a particular memory cell by the delays of the different paths in the address decoder. This means that each bit has to be "least significant" once, a condition achieved by shifting the order of significance of the address bits. The resultant number of necessary tests is unavoidably doubled since a regular sequence must be maintained.

Also important are coincidence times, which include address setup and hold times, data setup and hold times, and pulse width of the write enable signal. By inverting all addresses and data just before and after the write operation, the MOVI program can check all coincidence times. In normal operation, address and data are stable for a specified period before the write pulse; changing them suddenly can be instructive in disclosing defective address circuitry. After the write action, address signals revert to normal for the succeeding read operation (Fig. 5).

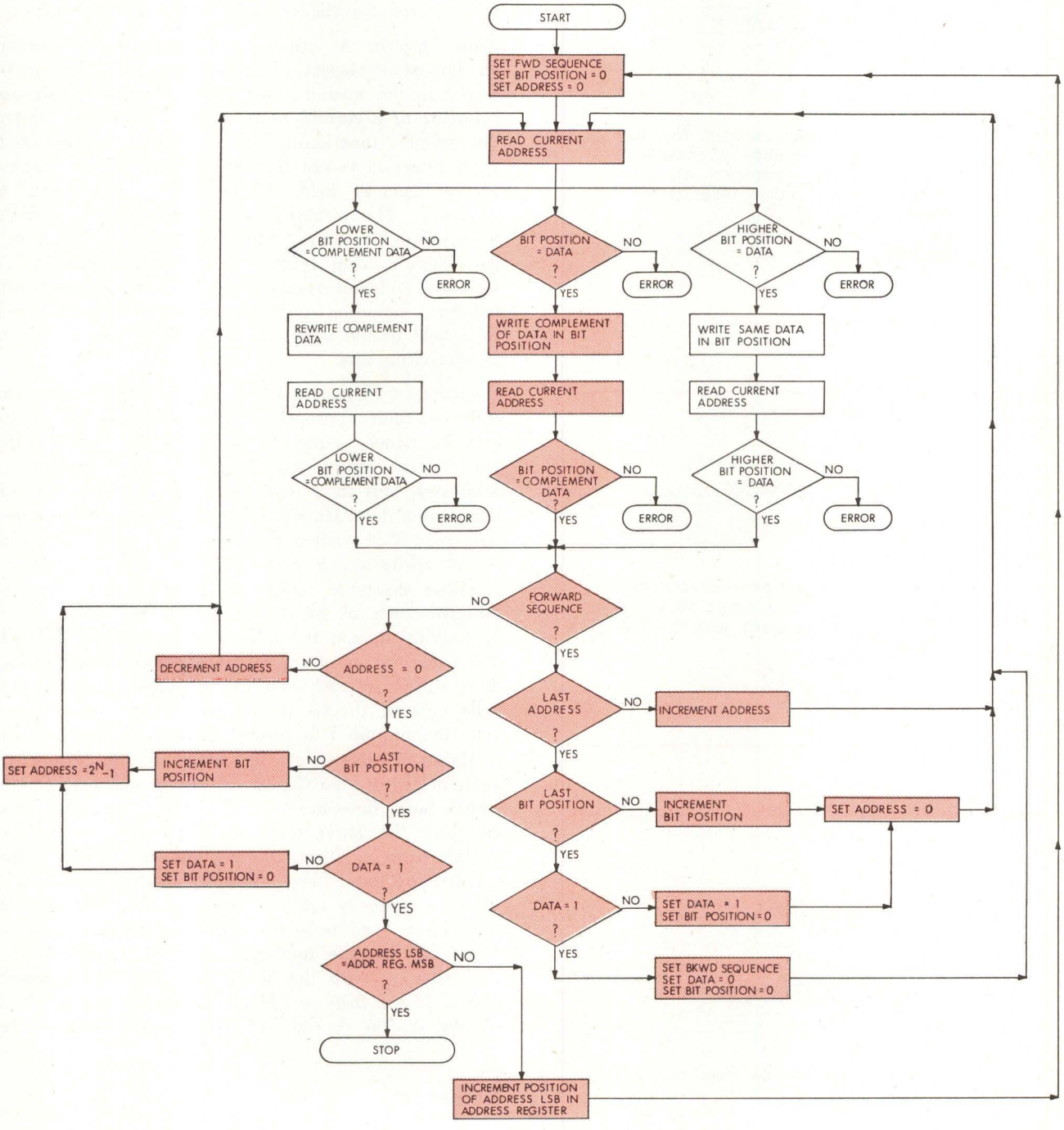


Fig. 2 Moving inversion sequence. The test can be applied to a single bit (color blocks) or to multiple bit positions (color and black). In the latter case the three parallel streams are executed concurrently

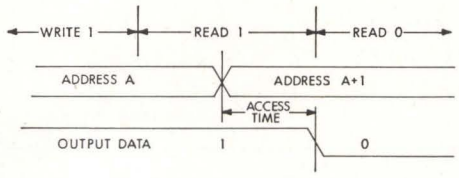


Fig. 3 Access time measurement. This is possible in MOVI because successive read operations are performed at addresses that always contain different information

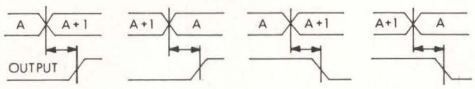


Fig. 4 Four cases. Access time measurement is made four ways during a single MOVI sequence—forward and backward, with the output rising and falling

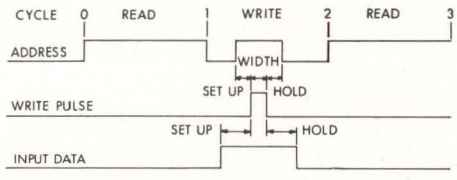


Fig. 5 Coincidence test. By inverting the address bits just before and just after the write pulse, setup times and hold times can be checked. Although the trace of only one address bit is shown here, it represents a multiplicity of lines, some of which are positive and some negative, in general. All of them are inverted in the coincidence check

This procedure can also check for any discrepancy in output information during a read cycle, when the address is changed from normal to inverse and information contained at the address remains constant. The check takes place before the write action for the first half of a sequence of addresses, and after the write action for the second half of this sequence.

*Data Pattern.* A suitable data pattern is sometimes an important aspect of a test program. Information stored in the memory field can influence the dynamic behavior of a certain location, or it may even obstruct the proper functioning of a location. Whereas the MOVI program is not intended to test all data patterns of the memory field, it does offer some useful test situations. The memory field is generally in a matrix of rows and columns. Although the MOVI program in its simplest form replaces a continual series of 0's with 1's, and vice versa, it can also be used with other patterns, including a single row or column of one bit in a field of the other, or succeeding rows or columns of alternating bits.

*Comparison With Other Test Programs.* Test programs differ in their approach as to which data are written, and in which sequence the write and read actions take place. Many test programs first write to all addresses, and then read from all addresses, verifying the written data. Others, having written to all addresses, first read this written data and then write the inverse to all addresses, a procedure known as MARCH.

These sequences can be combined with various data patterns such as all 1, all 0, checkerboard, walking 1, walking 0, and the address bits as input data. The galloping test program is more complicated; a single 1 is stored in each cell of an array while all other cells contain 0. All the 0 cells are rechecked every time the unique 1 is moved from one cell to another.

Main characteristics of several test programs[2] are summarized in the Table. Where a memory must be tested both functionally and dynamically, the galloping and the MOVI test patterns appear to be most useful. However, the galloping pattern involves a large number of tests.[3] For example, to test one data bit of a 4K memory cell requires $2 \times 2^{2N} - 2^N$, or over 33 million read tests for the galloping 1. If one test takes 250 ns, the total galloping test time would be 8 s, whereas with the MOVI test, the time is only $12 \times N \times 2^N \times 250$ ns = 144 ms. The difference is a factor of almost 100 shorter, a considerable saving of time.

## Summary

The MOVI program is a test pattern which has good functional and dynamic test features. A galloping pattern can test the effects on dynamic behavior, caused by certain address jumps which do not occur in the MOVI program. However, research has shown that these effects are not significant in bipolar or static metal-oxide semiconductor (MOS) memory. The MOVI test can be applied to dynamic MOS memories, but they

**Test Program Characteristics**

| Program (R/W Mode) | Data Pattern | Functional Strength | Dynamic Strength |
|---|---|---|---|
| Write all addresses | All 1 | Very poor; no check on all bits | Very poor; no transitions |
| Read all addresses | All 0 | | |
| | Checkerboard | Poor; address decoding is hardly checkable unless address bit significance is changed | Insufficient; some access times can be measured. Considerable improvement by changing the address bit significance |
| | Walking 1<br>Walking 0 | Good; all address selection and bit failures can be checked<br>Disadvantage: too many tests | Better than all 1 and 0. Gives access times from a particular address to the next one in the counter sequence. Improved by change of address bit significance |
| Write all addresses<br>Read all addresses | Address bits used as input data | Diagnostics of selection failure is simple, but requires many unnecessary tests | Insufficient; a little better than checkerboard |
| Read/write the inverse on each address | Combined with preceding data patterns | Much improved compared to the R/W all addresses technique | Very poor; no address jumps with access time |
| Galloping | | | |
| Write | 1 in field of 0's | Good | Good |
| Read addresses in galloping manner | 0 in field of 1's | Disadvantage: too many tests; twice as many as walking technique | All address access times can be measured |
| MOVI | | | |
| Read/<br>Write/<br>Read | Moving inversions | Good; considerably fewer tests than the galloping test program. More data patterns | Good; all fundamental address access times can be measured |

usually require very specific test procedures in addition to the MOVI program and other standard test programs.

Good test features and the small number of tests required with the MOVI program provide a solution in many cases. MOVI is particularly useful where larger memories require testing.

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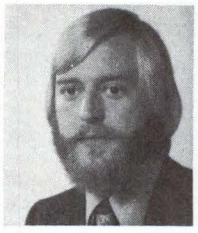
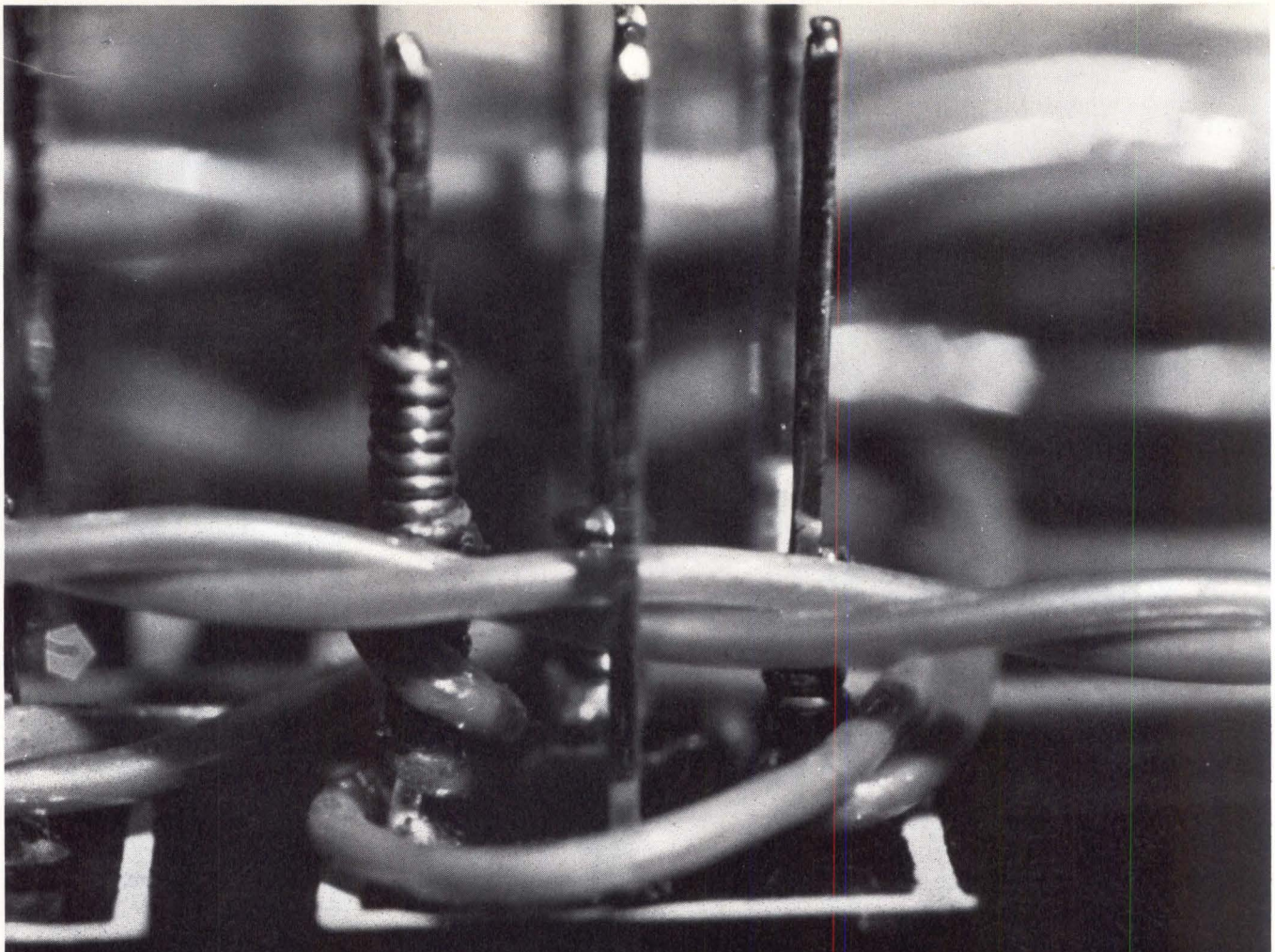
3. R. Nevala and C. Pelletier, "Testing of Static Bipolar RAMs," *Digest, IEEE Symposium on Semiconductor Memory Testing*, 1974, p 72


*J. Henk de Jonge holds an ingenieur degree from the Technical School of Groningen, The Netherlands. As an electronic engineer within the Memory Development Group of Philips Data Systems, he developed test programs and equipment for memory circuitry to be applied in future systems.*

*André J. Smulders holds an ingenieur degree from the Eindhoven University of Technology, The Netherlands. At the time this article was written, he worked in the Memory Development Group of Philips Data Systems.*



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***Programmable-ROMs can be substituted for the masked variety, even when the latter have unusual features, with the aid of a board that simulates the masked ROMs special characteristics***

# Adapter Simplifies Development of Microprocessor Systems

**Robert L. Morrison and Claude A. Wiatrowski***

Burr-Brown Research Corporation
Tucson, Arizona

Many aids for writing and debugging programs are available from microprocessor manufacturers. Although these are useful for preliminary testing of the software modules, final testing must be done in conjunction with the special hardware interfaces developed for the system. Particularly in larger systems, specialized hardware can be made similar enough to the microprocessor's development system to allow the special interfaces to be used with the development system for final testing. Alternatively, if the system uses compatible read-only memories, programmable read-only memories that are generated by the microprocessor development system can be used for final testing before specifying masks.

In small systems that can not justify the cost of over-specialized hardware, or that require specialized read-only memories (ROMs) that are not compatible with standard parts, an adapter can be built to allow the use of programmable ROMs (p/ROMs) in the system. Systems based on 4-bit processors such as the Intel 4004 or 4040 or the Rockwell PPS-4 or -4/2 are among the latter. These microprocessors are most economical with their own specialized ROMs that are available only in mask-programmed versions.

A p/ROM adapter (Fig. 1) allows up to four reprogrammable ROMs to be substituted for four mask-programmable Intel 4001 ROMs. The reprogrammable units used are Intel 1702s, which are programmed using the Intellec 4 microprocessor development system. Each ROM has a capacity of 256 x 8; up to 16 of them can be used in a system. However, because the microprocessor and its associated circuits have a data path only four bits wide, the contents of any addressed location must be multiplexed in two parts onto that path, and the address itself must be multiplexed in three parts—two for the location in an individual ROM (eight bits) and one to select a particular ROM (four bits). Each ROM carries a permanent identification, 0 through 15, established by metallization, and is supplied in a 16-pin package; four pins carry both the multiplexed address in and the multiplexed data out, during the first five of eight cycles that follow a synchronizing pulse from the microprocessor.

Although the 1702 p/ROM is also a 256 x 8 device, it comes in a 24-pin package of which eight pins are used for data and eight others for address, without multiplexing. Therefore, to enable the adapter to simulate the 4001, its inputs and outputs must be made to resemble the multiplexed connections of the system. These functions are performed by the Intel 4008 and 4009 interface circuits.

The adapter is connected to the system by cables that plug into the sockets that would be occupied by 4001s. One of these cables picks up the sync pulse and the three multiplexed address words, which are demultiplexed in the 4008 and forwarded to the p/ROMs. Data from the latter, eight bits wide, are multiplexed by the 4009 and returned to the ROM

*Now with the University of Colorado, Colorado Springs

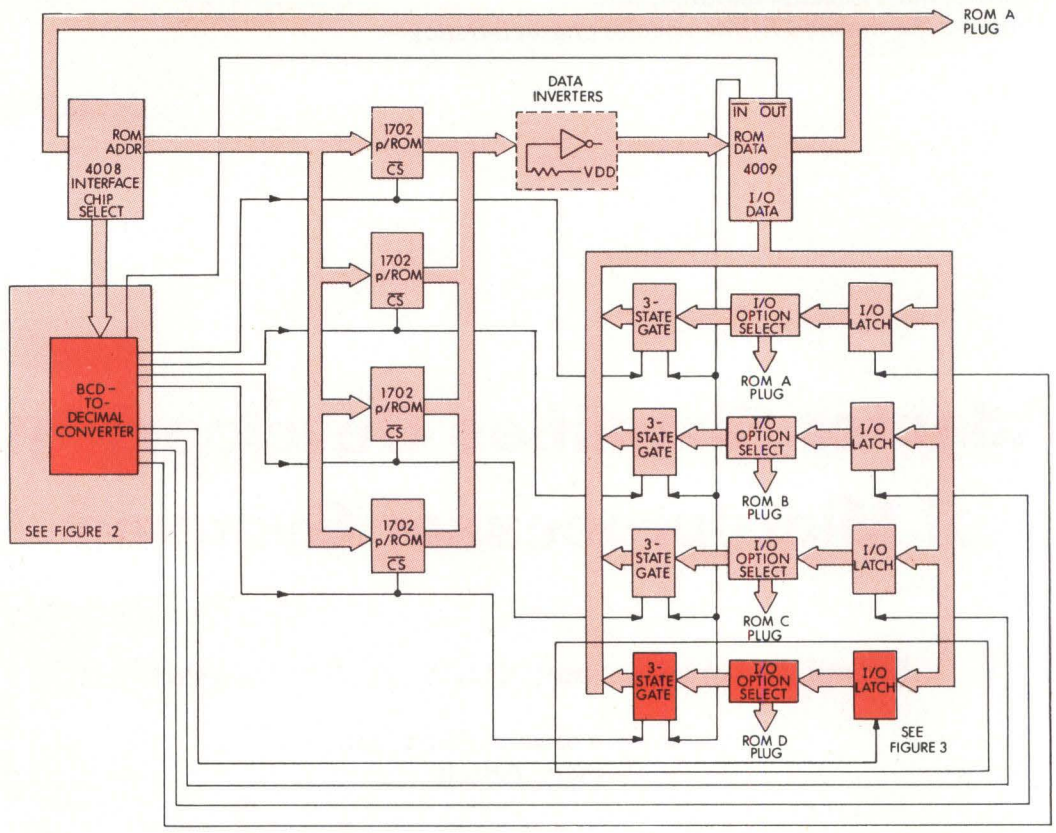



Fig. 1 p/ROM adapter. Four programmable ROMs can be used in place of four fixed ROMs in microcomputer development, with the aid of additional circuits detailed here

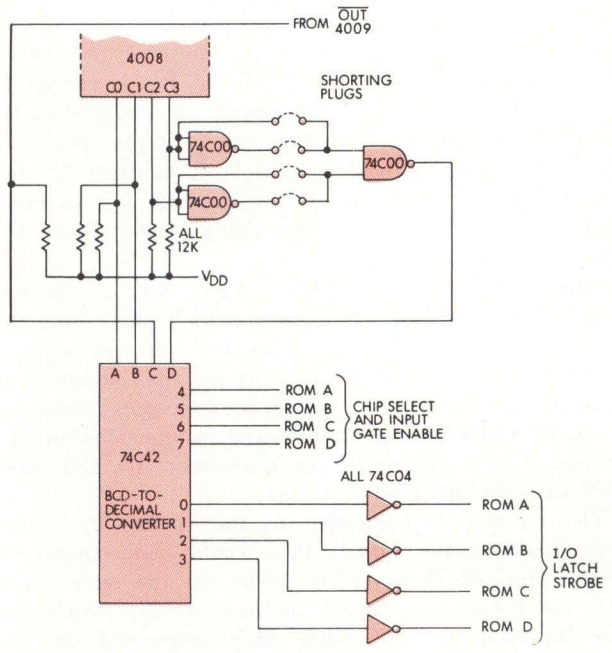



Fig. 2 Address decoding. Only two of four bits in third address word are needed in this adapter. Shorting plugs define the other two bits, and a line from an interface circuit establishes whether input/output portion of simulated ROM is used during a cycle

sockets along the same cable. One cable is sufficient because all of the ROMs are normally connected to the same bus.

One of 16 ROMs is selected by the third address word with its four bits. However, in the adapter, the maximum number of ROMs is four, so that only two of the four bits in the third word are needed. These are decoded in a BCD-to-decimal converter (Fig. 2) to select one of the four p/ROMs and enable its input gate. The two bits for this purpose enter the converter through its inputs weighted 1 and 2; the input with weight 8 defines the remaining two address bits so that the board's p/ROMs can be placed anywhere within the microprocessor's memory field. By this means, programs written for any memory locations can be executed.

The converter's input with weight 4 is used in connection with an additional complication in adapter design, encountered because the 4001 ROM has a mask-specified input/output (I/O) interface in addition to and separate from its ROM function. The interface consists of four lines, each of which is defined as either input or output by metallization, at the same time that the ROM contents and chip address are defined. When operating in I/O mode, the 4001 requires the same three multiplexed addressing cycles, but it uses only six of the 12 bits—two for the I/O line and four for the chip.

Thus, when an I/O cycle is called for, the converter's weight-4 input brings in a signal from the

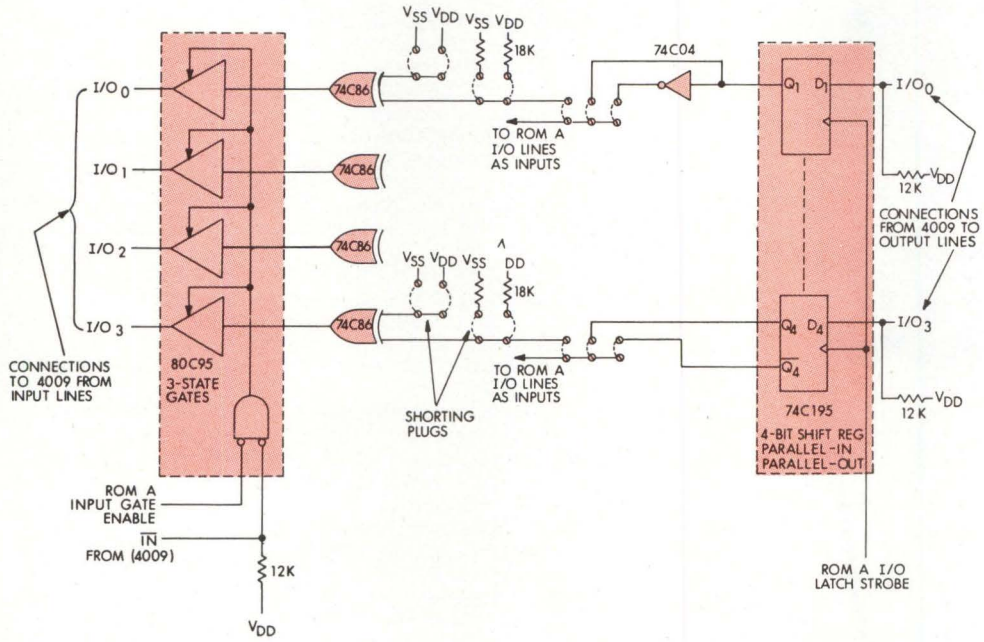


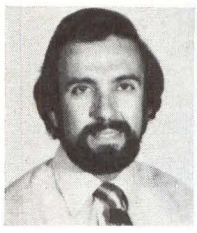

Fig. 3 Interface simulation. I/O latches (far right) route output data through adapter to peripheral device; shorting plugs (right) select true or complement output data. Other shorting plugs (center) select pull-up or pull-down, and (left) true or complement input data. All input data pass through 3-state gates (far left)

4009, which designates whether the upcoming cycle is input or output. If an output cycle is specified, the signal prevents the p/ROMs from being enabled and instead gates one of four sets of I/O latches (Fig. 3) through which output data are routed from the 4009. Shorting plugs are used again here to connect the true or complemented outputs of these latches to appropriate lines in the system, through the cables that plug into the ROM sockets. Separate cables are necessary because the I/O lines from the sockets are separate. Similarly, if the lines are input instead of output, shorting plugs make the appropriate connection to pull-up or pull-down voltages and, with the aid of exclusive-OR gates, establish whether direct or complemented input signals enter the system. The plugs duplicate the metallization in the ROM. Three-state drivers connect these to the I/O lines via the 4009; drivers are gated by signals from the 4009 and by the chip-enable lines from the BCD-to-decimal converter.

The adapter was constructed using CMOS logic so that it would need only one power supply (the 15-V microprocessor supply) and to simulate more closely the electrical characteristics of the I/O interface that is part of the 4001 ROM. TTL logic would require a separate 5-V power supply.

Only one adapter may be connected to the microprocessor bus, because the 4009's outputs are not 3-state. However, for memory expansion, an adapter has been built that replaces the data inverters in Fig. 1 with NOR gates. Additional NOR inputs are connected through an expansion cable to other adapters from which the 4009s have been removed. For the same reason, this adapter can not be used simultaneously with ROMs.

To date, these adapters have been in use successfully for several months and have not caused any timing or bus loading problems in rather complex Intel microprocessor systems.



*Robert L. Morrison holds a BSEE degree from Arizona State University and an MSEE degree from Colorado State University. As a product design engineer at Burr-Brown, he designed analog data acquisition and distribution systems for several microcomputer development systems. His experience also includes development of mini- and microcomputer-based systems.*

*Claude A. Wiatrowski, an assistant professor of electrical engineering at the University of Colorado, has designed several mini- and microcomputer systems, including some for use in harsh environments. He received a BS degree in physics from the Illinois Institute of Technology and a PhD in electrical engineering from the University of Arizona.*

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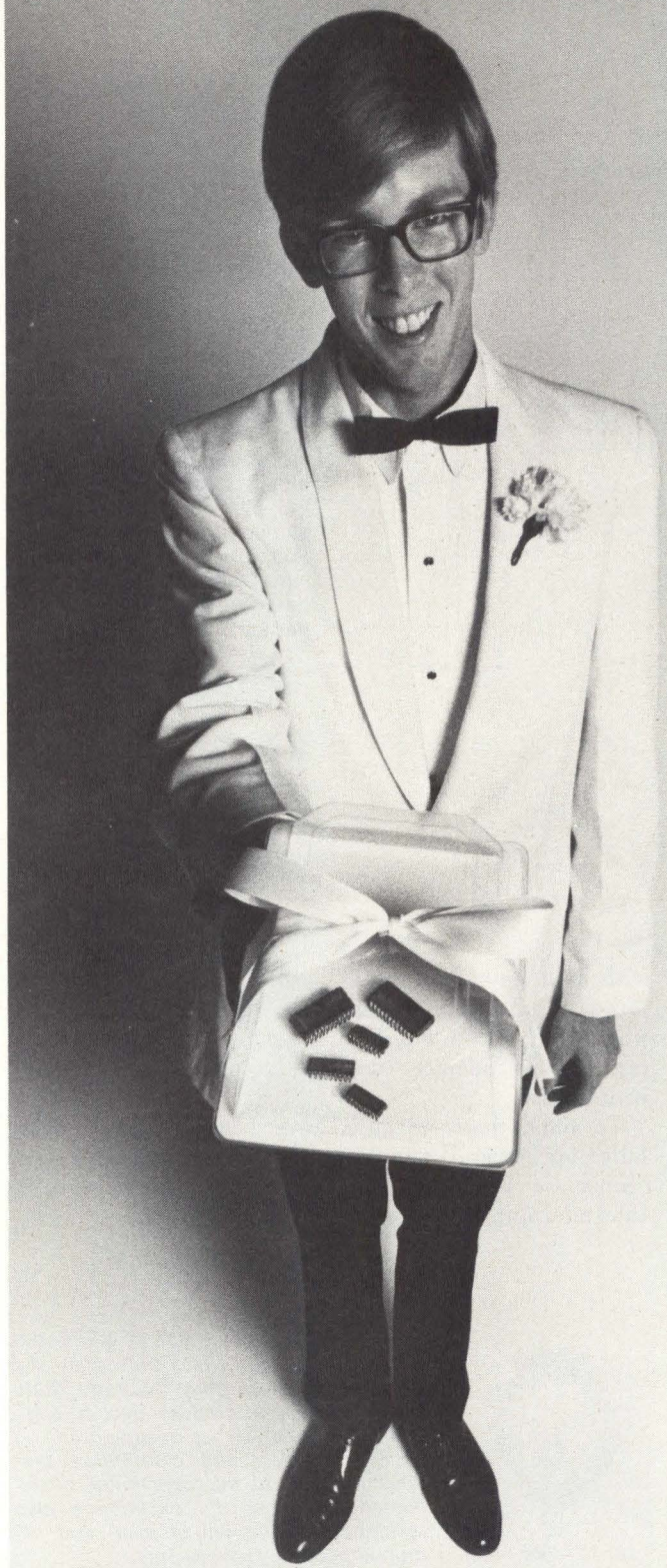

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| HM-7611 (three state) | 1024 | 256x4 | 16 | 60ns | 75ns | $4.95 | $9.95 |
| HM-7620 (open coll) | 2048 | 512x4 | 16 | 70ns | 85ns | $9.95 | $19.95 |
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| HM-7642 (open coll) | 4096 | 1024x4 | 18 | 70ns | 85ns | $19.95 | $39.95 |
| HM-7643 (three state) | 4096 | 1024x4 | 18 | 70ns | 85ns | $19.95 | $39.95 |
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***Transparent error-correction systems enhance the reliability of memory systems, but impose a cost in terms of system complexity and reduced speed***

# Automatic Error Correction in Memory Systems

**Bryan Rickard**

Electronic Memories & Magnetics Corporation
Hawthorne, California

First to use semiconductor mainframe memory in a major product line, International Business Machines Corp introduced the System/370 model 145 in 1971. As the reliability of semiconductor memory had not yet been firmly established, IBM used an automatic error-correction scheme in this memory. With that scheme, one fault in any word being read out had no effect on processor operation; the faulty readout was corrected within the memory system prior to transmission of the word to the central processing unit.

Similar error-correction schemes are now widely used in large mainframe semiconductor memories. In smaller computers, they are available for use when long periods of error-free operation must be achieved. It is worthwhile, therefore, to review how such a system operates; to examine the cost, both in components and system access time; and to analyze the reliability improvement that can be achieved by using error-correction.

Error-correction systems are simply an extension of the familiar parity principle. They use multiple parity checks on certain subsets of the bits comprising the data word. Several parity bits are generated and written into memory as additional bits on the end of the data word. The simplest system corrects only single-bit errors in any word. Addition of one more parity bit allows double errors to be detected, but not corrected.

## Debit Side

Parity checks significantly increase the word length (Table), raising power dissipation, cooling requirements, and board area. In addition, other circuits are required for control purposes. These include parity generation and check circuits, memory output buffers (most metal-oxide semiconductor memories cannot fan out into the several parity check circuits required), decoders for the parity circuit outputs, exclusive-OR circuits to complement the memory output if an error is detected, and flag latches to advise the central processing unit (CPU) that an error has been corrected or detected.

A third disadvantage of error-correction systems is their effect on memory speed. When writing, parity bits must be generated by adding all the 1's in several combinations of bits before the memory-write operation can begin. When reading, parity bits must be checked and necessary corrections made before data

**Increase in Word Length With Error Detection and Correction**

| Data Word Length | Single-Error Correction | | Single-Error Correction and Double-Error Detection | |
|---|---|---|---|---|
| | Extra Bits | Increase (%) | Extra Bits | Increase (%) |
| 4 | 3 | 75.0 | 4 | 100.0 |
| 8 | 4 | 50.0 | 5 | 62.5 |
| 10 | 4 | 40.0 | 5 | 50.0 |
| 12 | 5 | 41.7 | 6 | 50.0 |
| 16 | 5 | 31.25 | 6 | 37.5 |
| 18 | 5 | 27.8 | 6 | 33.3 |
| 20 | 5 | 25.0 | 6 | 30.0 |
| 24 | 5 | 20.8 | 6 | 25.0 |
| 32 | 5 | 15.6 | 6 | 18.75 |
| 48 | 5 | 10.4 | 6 | 12.5 |
| 60 | 6 | 10.0 | 7 | 11.7 |
| 64 | 6 | 9.4 | 7 | 10.9 |
| 72 | 6 | 8.3 | 7 | 9.7 |
| 96 | 6 | 6.25 | 7 | 7.3 |

can be released to the CPU. Depending on word length and circuit design, these operations can add 30 to 150 ns to memory access and cycle time.

## Credit Side

However, reliability can be significantly increased by use of single-bit error correction. To accurately evaluate the increase, it is necessary to distinguish between "hard" and "soft" errors, complete and partial chip failures, and bit- and word-related system faults. It is also necessary to examine just what is meant by "failure rate," to discard the concept of an invariant mean time between failures (MTBF), and to consider what action is taken when the memory is observed to be automatically correcting a permanent error.

First, some types of error will not be corrected or detected. For example, faulty system input or output circuits may garble data before parity is generated or after it is checked, power failures or refresh circuit malfunctions (when using dynamic random-access memories) can destroy all stored data, or failure of address decoding circuits can cause the wrong words to be read from memory or words to be written into wrong locations. In any failure rate analysis, these and similar word-related failure modes must be identified and their contribution to the overall failure rate added to those results obtained from analyzing bit-related failures.

Second, bit-related failures, which are corrected by the parity circuits, must be analyzed according to the number of system words they affect. In a 32K-word system, using 4K-bit memory integrated circuits (ICs), a gross failure of one IC (eg, putting its output permanently into the 0 state) could affect 4K words, or whatever number should contain 1 in the bit position corresponding to the failed IC. Failure of a buffer between the memory array and the parity check circuits affects all 32K words in the same way. On the other hand, a localized contamination problem in a chip may affect only one or a few words.

All such errors are corrected, as long as the rest of memory is error-free. However, if a second failure occurs, the chance that it will appear in a word that is already affected is clearly greater if the first error is common to many words. When this happens, a double noncorrectable error results.

## Failure Rate Analysis

To illustrate some unique considerations of failure rate analysis on a memory with error correction, consider

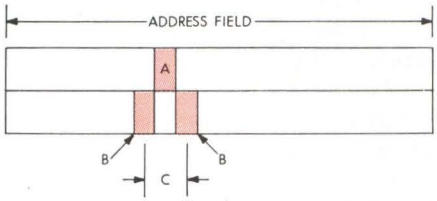


Fig. 1 Single-failure overlap. Region A represents the probability that a single failure (5%) will occur during the first 1000 hours of operation. Points marked B are limits of allowable second failures. If the part of the memory that is affected by a second failure is centered in region C, a double error is observed

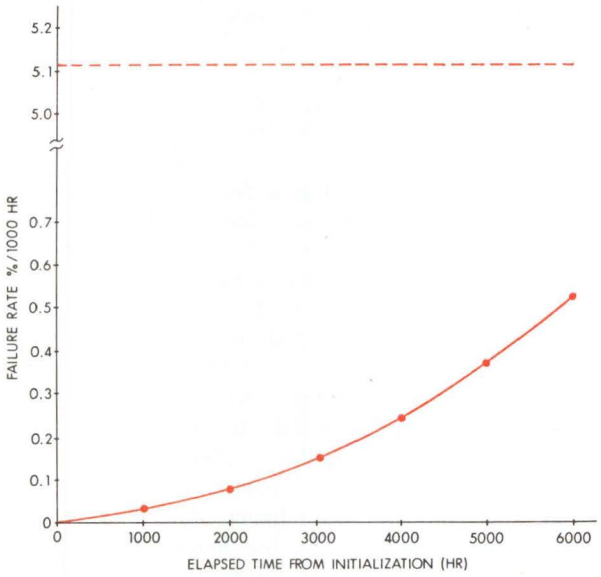


Fig. 2 Variable failure rate. Rate of bit-related failures apparent to the processor in a memory system that has error correction is a function of the length of time since any permanently defective components were last replaced. Dashed line represents failure rate of system without error correction

a system with a data capacity of 128K words of 16 bits each, assembled from 4K-bit chips.

Assume temporarily that all failures are "hard errors," which, once they appear, are permanent; that a failure typically affects 5% of the words in the system; and that the component failure rate is 0.01% per 1000 hours.

Without error correction, the chance that a failure will occur in any 1000-hr period is 0.01% times the number of memory chips, which is 512. This comes to 5.12%, and is also expressed as an MTBF of 19,531 hours.

With single-error correction, the physical memory word length is increased to 21 bits, increasing the chance of getting a single error in the first 1000 hours to 21/16 x 5.12%, or 6.72%. However, an error will be visible to the computer only if a second error occurs in the same word. Since typical errors affect only 5% of the memory words, the chance that two such errors will overlap is only 10% (Fig. 1). (An implicit assumption is made that any error affects a contiguous block of memory addresses. Other assumptions would slightly alter the 10% figure.)

The chance that the second failure will occur is only 6.4%, or 20/16 times the probability of a single error in an uncorrected system (only 20 bits remain that can fail). Therefore, the chance of two independent failures in the same word in the first 1000 hours is 6.72% x 6.4% x 10% = 0.043%. Inclusion of second-order effects (based on the possibility that three or more errors will occur in this time period) increases this figure to 0.048%, which is still equivalent to an MTBF of over 2 million hours—100 times better than without error correction.

This analysis is quite sensitive to the size and distribution of those words affected by the projected failures. Clearly, if a failure affects all of a memory's words, a subsequent failure in a different bit will cause a noncorrectable error. In this case, after the first failure, the subsequent failure rate is worse than that without error correction, because there are 20 more bits which can fail instead of 16. While the assumption that typical failures affect 5% of the memory words is a convenient simplification, and may even be true, in a practical situation, atypical failures must also be considered. Furthermore, this analysis is valid only for the first 1000 hours, ie, when it is known that no errors are present (and being transparently corrected) initially. (Without error correction, an MTBF calculation is valid for any period.)

With the passage of time, the probability that a hard error has occurred and is being corrected by the system increases exponentially, along a curve $y = 1 - a^x$, where a is between 0 and 1. This curve is

asymptotic to 1, because failure is never certain, although continued operation without failure is highly unlikely after a sufficiently long time. Since a second error has a constant probability of occurring, the likelihood of a double error resulting in an observable malfunction also increases exponentially with time. Thus, if the hypothetical system, with a 1000-hr failure rate of 6.72%, has been running for 5000 hours, the chance that a transparent fault has already developed is approximately $[1 - (1 - 0.0672)^5] = 0.294$ or 29.4%. Given these initial conditions, the chance of failing in the next 1000 hours is 29.4% x 6.4% x 10% = 0.188%. Thus, the expected failure rate increases, and the MTBF correspondingly decreases by a factor of 0.188/0.048 or nearly four over this period of time.

In fact, there is also a substantial chance that two or more faults will have developed in different words. Although these faults will be transparently corrected by the system, they increase the chance that a subsequent fault will cause an observable error. Taking this effect into account, a curve of system failure rate versus elapsed time may be plotted (Fig. 2), since operation was known to be error-free. This curve shows a slight increase of slope with time, instead of the exponential decrease obtained when only one undetected fault is considered. Applying this correction to the previous calculation, the failure rate after 5000 hours is 0.38%/1000 hr, or more than seven times the rate for the first 1000-hr period. Eventually, the failure rate will exceed that of the system without error correction. This occurs when the population of permanent single-bit errors is so high that double errors are more likely among the 21 bits including error correction than single errors are among the 16 uncorrected bits, when they are known to be initially good. Of course, this state of affairs is most unlikely, since double errors would probably already have occurred and the faults repaired.

Therefore, to gain maximum benefit from an error-correction system, the system should be checked periodically for permanent faults that are being systematically corrected. These should be repaired before they become implicated in a double error. Error-correction systems are usually equipped with indicators to show when errors are being corrected. Repairs can then occur "on demand," if considered necessary. More elaborate systems include counters and registers to collect statistical data about the incidence of soft and hard errors.

This increase in the failure rate for a system using automatic error correction leads to another paradox. If a period other than the 1000-hr span is used as the base time for calculating failure rates, the rate is different. As an extreme case, any attempt to calculate the number of failures per $10^9$ hours fails, because the expected number of single failures is always greater than unity. (This corresponds to the case where the failure rate eventually exceeds that of a system without error correction.) The time period must be short enough that the individual failure rate is much less than unity. However, if the base time is too short (say a few minutes), the chance of two independent failures in the same word is so low that the MTBF approaches infinity. In practice, the base period for the determination of MTBF should approximate the planned period between routine checks for single errors.

Perhaps the chief advantage of automatic error-correction lies in its ability to correct soft errors. These elusive faults, which often occur in dynamic random-access memories (RAMs), are thought to result from worst-case relationships between refresh timing and access of marginal cells. In manufacturing these RAMs, it is not possible to exhaustively test each cell at the maximum specified time since it was previously refreshed. In the field, however, a program may catch a weak cell in that situation, resulting in an error. Repetition of the program may not repeat the error, since refresh timing is usually asynchronous with respect to program execution.

By nature, the chance that two soft errors will occur simultaneously in the same word is negligible. The only way that they can cause a fault in a system with error correction is if they occur in coincidence with a hard error. Therefore, it is necessary to consider the soft error rate in a dynamic RAM system when establishing criteria for periodic checking of such a system for hard errors.

## Conclusion

Clearly, a substantial reliability improvement results from use of error-correction systems. Quantification of this improvement, however, is tricky, and depends on several factors not usually considered in reliability calculations. Even when numerical results are obtained, their usual expression as an MTBF or a failure rate is ambiguous; these numbers vary with time and can be improved by preventive maintenance.

The information presented here should clear some of the mystery away from error-correction techniques and provide a structure on which to base analyses of failure rates and preventive maintenance policies. A decision on whether or not to use error-correction and/or detection techniques in any particular situation can be made on the basis of these analyses. It can be effective only if the underlying principles and tradeoffs are thoroughly understood.

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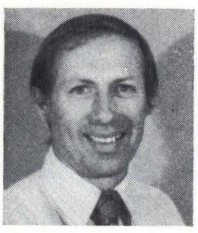

*After graduation from Cambridge University in England, Bryan Rickard worked with core memories for several years, then joined Electronic Memories & Magnetics, where he has worked extensively with both core and semiconductor memories. He is currently sales training manager for the company.*

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TECH NOTE

# Shortcut to Logarithms Combines Table Lookup and Computation

**San-Yen Shi**

NCR Corporation
Dayton, Ohio

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When a computer programmer requires his system to obtain the logarithm of a quantity, he generally has two ways of going about it: he can compute the logarithm, for example from the first few terms of an infinite series, or he can insert a table of logarithms in the computer's memory and have the system look up the number in much the same way as it is looked up in manual computation. Both methods have disadvantages; the computation takes time, particularly if it must be repeated and if it must be carried out to high precision, while the log table occupies a large area of memory.

However, the computation can be simplified by combining the two methods. This combination is based on a table of nine rows and n + 1 columns, where n is the required number of decimal places in the result. The first column contains the first nine powers of the base, which are the characteristic values of those logarithms. Other columns succes-

**Reference Table for Base e With N = 6**

| | $e^e$ | $(e^{0.1})^{m_1}$ | $(e^{0.01})^{m_2}$ | $(e^{0.001})^{m_3}$ | $(e^{0.0001})^{m_4}$ | $(e^{0.00001})^{m_5}$ | $(e^{0.000001})^{m_6}$ |
|---|---|---|---|---|---|---|---|
| 1 | 2.7182818 | 1.1051709 | 1.0100502 | 1.0010005 | 1.0001000 | 1.00001 | 1.000001 |
| 2 | 7.3890561 | 1.2214028 | 1.0202013 | 1.0020020 | 1.0002000 | 1.00002 | 1.000002 |
| 3 | 20.0855370 | 1.3498588 | 1.0304545 | 1.0030045 | 1.0003000 | 1.00003 | 1.000003 |
| 4 | 54.5981500 | 1.4918247 | 1.0408108 | 1.0040080 | 1.0004001 | 1.00004 | 1.000004 |
| 5 | 148.4131591 | 1.6487213 | 1.0512711 | 1.0050125 | 1.0005001 | 1.00005 | 1.000005 |
| 6 | 403.4287935 | 1.8221188 | 1.0618365 | 1.0060180 | 1.0006002 | 1.00006 | 1.000006 |
| 7 | 1096.633158 | 2.0137527 | 1.0725082 | 1.0070246 | 1.0007002 | 1.00007 | 1.000007 |
| 8 | 2980.957987 | 2.2255409 | 1.0832871 | 1.0080321 | 1.0008003 | 1.00008 | 1.000008 |
| 9 | 8103.083928 | 2.4596031 | 1.0941743 | 1.0090406 | 1.0009004 | 1.00009 | 1.000009 |

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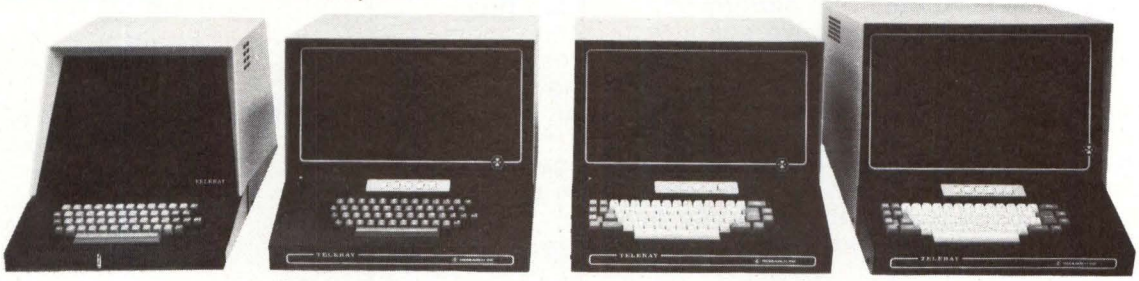

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sively contain decimal fractions of the same powers. Thus, if the base is e, the first column contains e, $e^2$, $e^3$, and so on; the second column contains $e^{0.1}$, $e^{0.2}$, $e^{0.3}$, . . ., and other columns contain powers of $e^{0.01}$, $e^{0.001}$, $e^{0.0001}$, and on out to the desired number of decimal places.

After the table has been precalculated, it is used according to the following algorithm. To calculate the logarithm of x to the base b:

(1) The characteristic is determined from the basic definition

$$x = (b^c) \times (b^m)$$

The characteristic is c; it is an integer with a value such that m is a fraction between 0 and 1, so that $b^m$ is between 1 and b. There is only one such integer; it may be 0, if x is less than b. The number $b^m$ is $P_0$, for use in finding the first digit of the mantissa.

(2) From the table, determine successive digits of the mantissa. Each digit $m_{i+1}$ is the largest integer for which

$$P_{i+1} = P_i/(b^{0.00\ldots1})^{m_{i+1}} > 1$$

when the exponent of b has i + 1 digits. This integer may be 0.

(3) Repeat this process until the desired accuracy is achieved. The logarithm is

$$\log_b(x) = c.m_1m_2m_3\ldots m_n$$

*Example*: Find $\log_e(361)$ to six places. From the table,

$$1 < b^m = 361/e^4 = 361/54.5981500 = 6.611946 > e$$

$$1 < b^m = 361/e^5 = 361/148.4131591 = 2.432399 < e$$

$$b^m = 361/e^6 = 361/403.4287935 = 0.894830 < 1$$

Thus c = 5.

To find the first digit of the mantissa, calculate $P_1$ such that

$$1 < P_1 = P_0/(b^{0.1})^{m_1} = b^m/(e^{0.1})^7 = (2.432399)/(2.0137527) = 1.2078936$$

$$1 < P_1 = P_0/(b^{0.1})^{m_1} = b^m/(e^{0.1})^8 = (2.432399)/(2.2255409) = 1.0929473$$

$$1 > P_1 = P_0/(b^{0.1})^{m_1} = b^m/(e^{0.1})^9 = (2.432399)/(2.3495031) = 0.9889396$$

Thus the largest possible integer value for $m_1 = 8$.

In the same way, $P_2$ is calculated from $P_1$, using $(b^{0.01})^{m_2}$ in the denominator of the fraction:

$$1 < P_2 = P_1/(b^{0.01})^{m_2} = P_1/(e^{0.01})^8 = (1.0929473)/(1.0832871) = 1.0089175$$

Successive integers of the logarithm are calculated in the same way:

$$1 < P_3 = P_2/(b^{0.001})^{m_3} = P_2/(e^{0.001})^8 = (1.0089175)/(1.0080321) = 1.0008783$$

$$1 < P_4 = P_3/(b^{0.0001})^{m_4} = P_3/(e^{0.0001})^8 = (1.0008783)/(1.0008003) = 1.0000779$$

$$1 < P_5 = P_4/(b^{0.00001})^{m_5} = P_4/(e^{0.00001})^7 = (1.0000779)/(1.00007) = 1.0000079$$

$$1 < P_6 = P_5/(b^{0.000001})^{m_6} = P_5/(e^{0.000001})^7 = (1.0000079)/(1.000007) = 1.0000009$$

Successive integers of the logarithm are the successive largest powers of $e^{0.00\ldots1}$ (or $b^{0.00\ldots1}$) that permit $P_1$ to be larger than 1. Thus $\log_e(361) = 5.888877$

To implement the scheme, the precalculated table is stored in memory and a program is written to execute the successive steps. If the logarithms must be frequently calculated, the table can be stored in a read-only memory installed in the system. □

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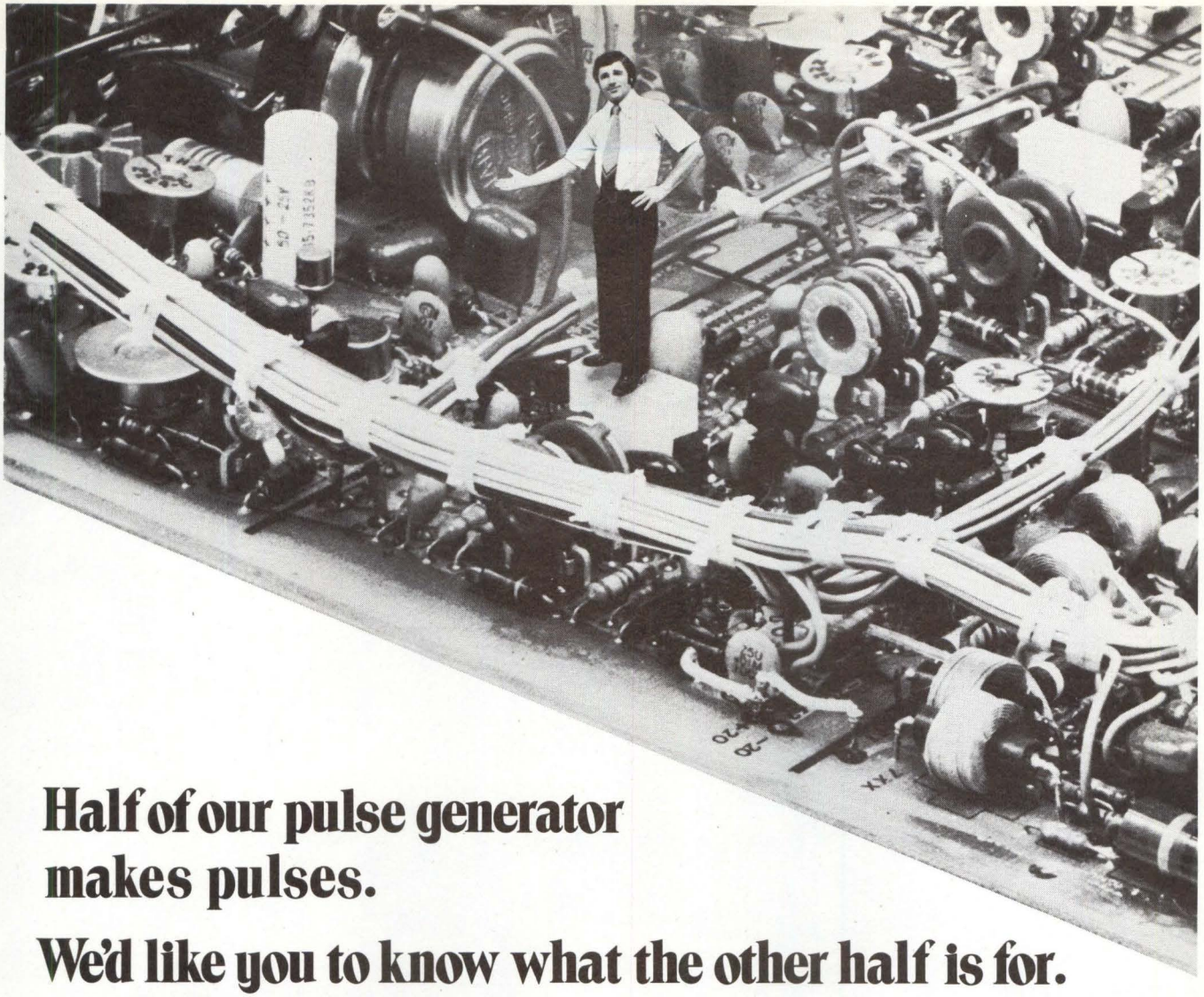

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APPLICATION NOTE

# Calculating an Error Checking Character in Software

**Suresh Vasa**

Fairchild Micro-Systems
San Jose, California

*CRC characters, which follow the blocks of data to be transmitted, although usually generated in a hardware shift register with feedback loops, can be created quickly by software in microprocessor-based system*

A software approach is used in the F8 microprocessor to generate a cyclic redundancy check (CRC) character for a block of data. The character provides a means of detecting the occurrence of bursts of errors in the block that it follows. The technique can be used for any cyclic code, including that used for the IBM synchronous data link control (SDLC) communication protocol.

To form the CRC, the binary value is premultiplied by $x^{16}$ and is divided by an appropriate polynomial, which for SDLC is

$$x^{16} + x^{12} + x^5 + 1$$

In many digital systems these operations are performed in a feedback shift register (Fig. 1). Assume that the initial content of this register is represented by A15, A14, A13, . . . , A0, and that an 8-bit character is received, represented by B7, B6, B5, . . . , B0 (A15 and B7 are the most significant bits). The CRC generation process is performed by

**CRC Generation Routine**

```
XS  1      Exclusive-OR scratchpad 1 and accumulator
LR  2,A    Store result in scratchpad 2
SR  4      Shift accumulator right four places;
             (accumulator contains 0000IJKL)
XS  2      Exclusive-OR scratchpad 2 and accumulator
LR  2,A    Result is IJKLMNOP; store in scratchpad 2
SL  4      Shift accumulator left four places; contains MNOP0000
XS  0      Exclusive-OR scratchpad 0 and accumulator
LR  1,A    Store result in scratchpad 1
LR  A,2    Bring back IJKLMNOP to accumulator
SR  1
SR  1
SR  1      Shift accumulator right three places; contains 000IJKLM
XS  1      Exclusive-OR scratchpad 1 with accumulator
LR  1,A    Store result in scratchpad 1
LR  A,2    Again bring back IJKLMNOP to accumulator
SL  4
SL  1      Shift left five places; contains NOP00000
XS  2      Exclusive-OR scratchpad 2 with accumulator
LR  0,A    Store in scratchpad 0
```

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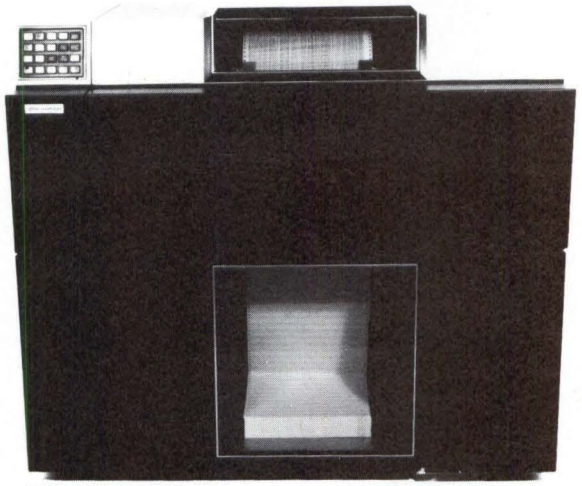

DOC 2250 OR DOC 1800

DOC 1800 (printing 1800 lpm). Either model can appear to your system as either an IBM 3211 or 1403. With some extra advantages thrown in.

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The 1403 compatibility feature allows both models to operate in the 1403 mode. This feature includes: paper tape loop; operator selection of line spacing (6-8 lines per inch); dualing; manual indexing with rotary dial; use of 1403 UCSB feature or other standard non-UCSB character arrays. Your CPU will think it's working with a 1403. You'll know you're getting a 2250 or 1800 lpm printer for just about the cost of an 1100 lpm printer.

The read/punch side of the Subsystem (the PC 6000 Reader and the PC 50 Punch) recognizes the same command set as the IBM 2540. All data and control signals transferred between the host and the PC 50 and PC 6000 pass through a subsystem microprocessor controller built into the PC 6000. Utilizing Documation's own patented riffle-air pick and stack system, the PC 6000 reads 1000 cards per minute and stacks them in one of two stackers. The input hopper holds 6000 cards and can be loaded on the fly. Stacker 1 card capacity is 5500; Stacker 2 holds 3000 cards. PC 6000 options include 51 Column Card Read, Optical Mark Read and Read Column Eliminate.

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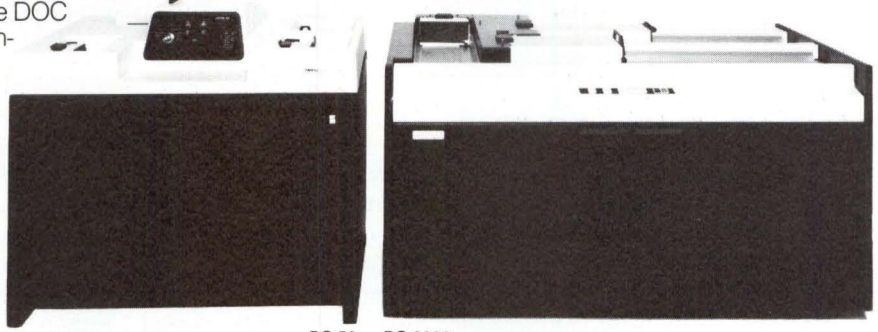

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| X15 | X14 | X13 | X12 | X11 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | INITIAL VALUE |
| A14 | A13 | A12 | A11⊕I | A10 | A9 | A8 | A7 | A6 | A5 | A4⊕I | A3 | A2 | A1 | A0 | I | B7 RECEIVED |
| A13 | A12 | A11⊕I | A10⊕J | A9 | A8 | A7 | A6 | A5 | A4⊕I | A3⊕J | A2 | A1 | A0 | I | J | B6 RECEIVED |
| A12 | A11⊕I | A10⊕J | A9⊕K | A8 | A7 | A6 | A5 | A4⊕I | A3⊕J | A2⊕K | A1 | A0 | I | J | K | B5 RECEIVED |
| A11⊕I | A10⊕J | A9⊕K | A8⊕L | A7 | A6 | A5 | A4⊕I | A3⊕J | A2⊕K | A1⊕L | A0 | I | J | K | L | B4 RECEIVED |
| A10⊕J | A9⊕K | A8⊕L | A7⊕M | A6 | A5 | A4⊕I | A3⊕J | A2⊕K | A1⊕L | A0⊕M | I | J | K | L | M | B3 RECEIVED |
| A9⊕K | A8⊕L | A7⊕M | A6⊕N | A5 | A4⊕I | A3⊕J | A2⊕K | A1⊕L | A0⊕M | I⊕N | J | K | L | M | N | B2 RECEIVED |
| A8⊕L | A7⊕M | A6⊕N | A5⊕O | A4⊕I | A3⊕J | A2⊕K | A1⊕L | A0⊕M | I⊕N | J⊕O | K | L | M | N | O | B1 RECEIVED |
| A7⊕M | A6⊕N | A5⊕O | A4⊕I⊕P | A3⊕J | A2⊕K | A1⊕L | A0⊕M | I⊕N | J⊕O | K⊕P | L | M | N | O | P | B0 RECEIVED |

I = A15⊕B7
J = A14⊕B6
K = A13⊕B5
L = A12⊕B4
M = A11⊕B3⊕I
N = A10⊕B2⊕J
O = A9⊕B1⊕K
P = A8⊕B0⊕L

Fig. 1 Feedback shift register. CRC characters are conventionally generated in devices like this one, shown connected for IBM SDLC protocol

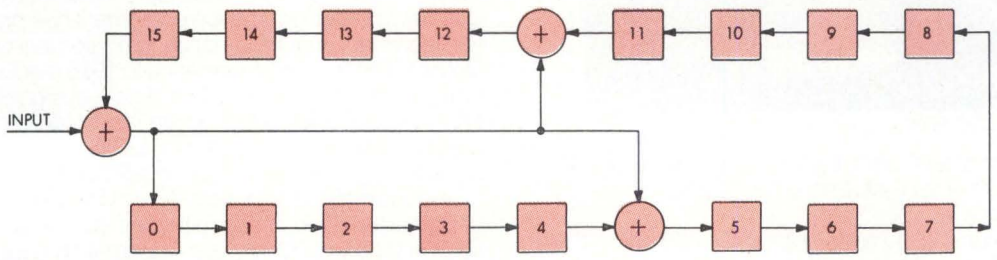


Fig. 2 CRC generation. As input character B arrives serially at shift register, its contents change step-by-step. It contains proper CRC character for B after last bit is in

these eight bits one at a time as they arrive serially at the shift register (Fig. 2). The last line of the figure indicates the result, after the last bit of character B has been received.

To generate the CRC with software would require more instructions and more time than is usually available, unless the system's instruction set includes commands such as exclusive-OR and 4-bit left and right shifts that can be executed in one machine cycle. The F8 includes such instructions.

To use these instructions, assume that scratchpad registers 0 and 1 together contain a 16-bit remainder (A15 - A0), and that character B is in the accumulator register. Scratchpad register 2 is available for temporary storage.

A routine that generates the CRC (see listing) consists of five exclusive-OR instructions interspersed with various shifting steps that align the bits for the successive exclusive-ORs, corresponding to the shifting and feedback steps in the hardware generation of the CRC. The exclusive-OR is performed bit-for-bit on the contents of the accumulator and a specified scratchpad register, of which the F8 contains 64; the result of the operation replaces the input bits in the accumulator. A shift in either direction leaves 0's in its wake; a subsequent exclusive-OR, of course, simply moves the bits from the other register into the positions containing 0 in the accumulator, and inverts the remaining bits.

At the end of the sequence, scratchpad registers 1 and 0 (in that order) contain the same data as the feedback shift register after receipt of character B; the lower eight bits of this result are also found in the accumulator. Register 2 contains an intermediate result that is no longer needed.

The sequence contains 19 instructions, each of which occupies one byte of memory; its total execution time is 38 $\mu$s. □

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# Generating Input/Output Device Select Pulses For Microcomputer Interfacing

**David G. Larsen**
Virginia Polytechnic Institute & State University

**Jonathan A. Titus**
Tychon, Inc

**Peter R. Rony**
Virginia Polytechnic Institute & State University

Last month's column on microcomputer interfacing discussed the 16-bit OUT instruction contained within the 78 instruction set of the Intel 8080 microprocessor chip. That instruction comprises two successive 8-bit bytes, and can be written in binary notation, $11010011_2$ $XXXXXXXX_2$; in 8-bit octal code, $323_8$ $YYY_8$; or in 8-bit hexadecimal code, $D3_{16}$ $ZZ_{16}$. A discussion of how to convert 8-bit binary code into either octal or hexadecimal code can be found in Ref. 1. In the above notations, $XXXXXXXX_2$ represents an 8-bit byte that can range in value from $00000000_2$ to $11111111_2$; $YYY_8$ represents a 3-digit octal code that can range from $000_8$ to $377_8$; and $ZZ_{16}$ represents a 2-digit hexadecimal code that can range from $00_{16}$ to $FF_{16}$. A quick calculation demonstrates that $11111111_2$, $377_8$, and $FF_{16}$ represent the same 8-bit binary word. Choice of coding system is up to the user.

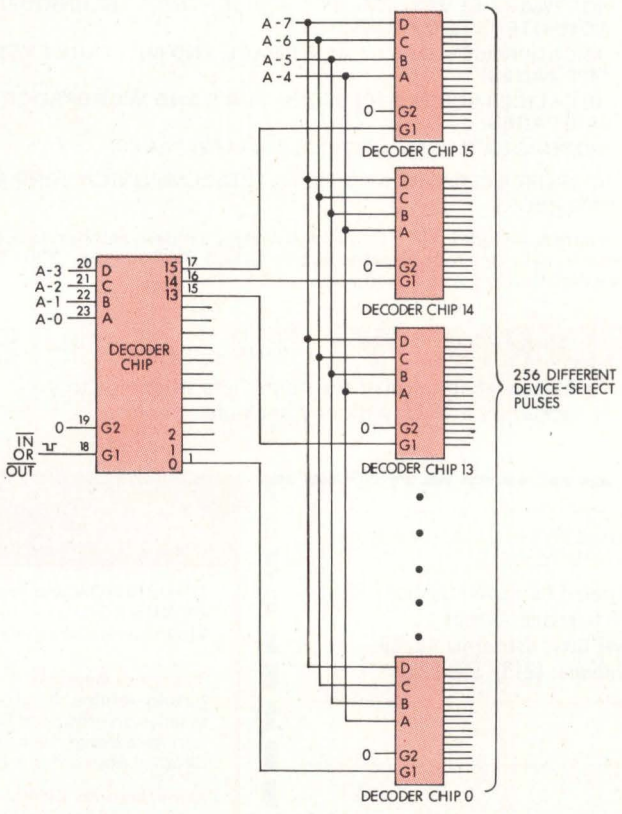


Fig. 1 Circuit permits generation of $256_{10}$ device-select pulses for output devices. Similar circuit permits generation of $256_{10}$ device-select pulses for input devices. Owing to the relatively large power consumption, SN74L54 decoder chips are recommended

Binary code is awkward to write and difficult to remember. Octal code is used in Digital Equipment Corp's PDP-8 and -11 minicomputer software, and is easy to remember. Hexadecimal code is more natural for an 8-bit binary word; it is currently quite popular among microprocessor manufacturers. We should emphasize that the manner in which the code is written on paper will not affect the way in which the microcomputer will execute a program. Both octal and hexadecimal codes eventually must be converted back to binary, which is stored in successive 8-bit memory locations. Conversion can be accomplished several ways, eg, by hand or by computer program.

The second 8-bit byte, $XXXXXXXX_2$, in the 16-bit OUT instruction is the device code for the output device. As indicated in previous columns,

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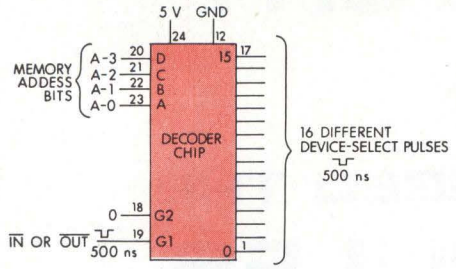


Fig. 2 Simpler circuit allows generation of 16 device-select pulses, either for input or output devices, but not for both simultaneously

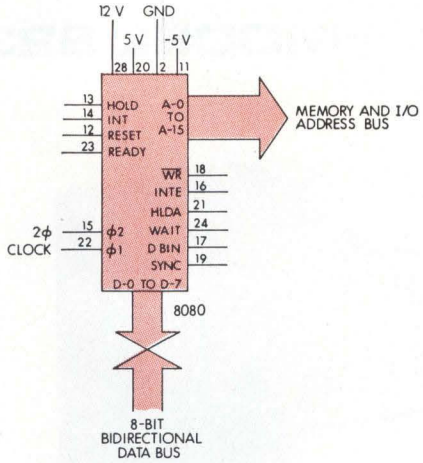


Fig. 3 Block diagram of Intel 8080-based microprocessor chip. Note 16-bit memory and I/O address bus shown at top right; bus provides two identical sets of 8-bit device codes during the OUT and IN instructions

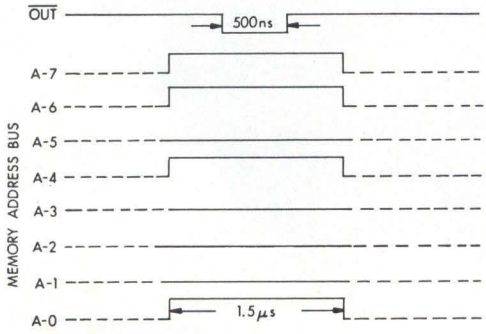


Fig. 4 Set of timing diagrams depicting the relationship of the OUT function pulse and the device code information appearing on the memory address bus. Information is applied to SN74-154 decoder circuits such as those in Figs. 1 and 2

$256_{10}$ different devices can be addressed with the aid of such a code. This procedure is shown in detail in Fig. 1, which provides a device decoding circuit comprising 17 SN74154 integrated circuit (IC) chips. Since this is a rather complicated circuit, we will first discuss the simpler decoding circuit shown in Fig. 2.

SN74154 IC chips are 4-line-to-16-line decoders that allow any 4-bit binary word ranging from $0000_2$ to $1111_2$ to be input, and any single output from among 16 channels labeled 0 to $15_{10}$ to be selected. G1 and G2 are the strobe or gating inputs to this chip; when they are both at logic 0, the chip is said to be enabled (ie, it is operative), and the output channel (one of 16) that corresponds to the binary input at pins 20 to 23 is at logic 0. When either G1 or G2 is at logic 1, the chip is disabled (ie, it is inoperative), and all output channels are at logic 1, irrespective of the binary input at pins 20 to 23.

Basic trick employed by the 8080-based microcomputer is to enable the chip for a very short period of time—500 ns to be exact. This is done with the aid of a negative clock pulse at G1. This pulse, called IN or OUT in Ref. 1, or I/O R or I/O W by Intel,[2] is generated by the microprocessor chip with the aid of some additional circuitry. IN and I/O R refer to the 16-bit IN instruction, whereas OUT and I/O W refer to the 16-bit OUT instruction. During this 500-ns period, the device code appears on the memory address bus and can be used as input to the SN74154 chip to select a desired output channel.

The memory address bus is a group of 16 output pins on the 40-pin 8080 microprocessor chip (Fig. 3). A bus can be defined as a path over which digital information is transferred, from any of several sources to any of several destinations. Only one transfer of information can take place at any one time. While such transfer is taking place, all other sources that are tied to the bus must be disabled.[1] An important point here is that two types of information can appear on the 16-bit memory address bus: the 16-bit memory address for a memory location addressed by the 8080, or the 8-bit device code present in the second 8-bit byte of an IN or OUT microprocessor instruction; but both may not appear at the same time. IN or OUT microprocessor instructions require 5 $\mu$s for execution, and the device code appears only during the last 1.5 $\mu$s of this time. When the device code appears on the memory address bus, the bus is subdivided into two 8-bit bytes, each containing the address code. Thus, there is a choice of bits A-0 through A-7 or A-8 through A-15 for the device code. This 8-bit device code is connected directly to one or a group of decoder chips, as shown in Figs. 1 and 2. In Fig. 2, only four of the eight device code bits are used whereas in Fig. 1, all eight device code bits are decoded into $256_{10}$ different output or input device code negative clock pulses. Each output device is addressed uniquely by the OUT function pulse and by a corresponding 8-bit device code. The same is true for each input device, except the IN function pulse is employed instead of the OUT function pulse at the gating input G1 to the decoder chip. Each device-select pulse lasts for only 500 ns, the time that the decoder chip is gated at G1.

Fig. 4 provides a set of timing diagrams that summarizes the ex-

ternal consequences of the OUT instruction:

(1) An 8-bit device code appears on the memory address bus for a period of 1.5 $\mu$s, in this case the code for device $11010001_2$ or $321_8$

(2) During this 1.5 $\mu$s, an OUT function pulse is generated for a period of 500 ns

(3) These nine output lines are used as inputs to the 17-chip circuit shown in Fig. 1. This circuit generates a 500-ns negative device-select pulse for device $321_8$. All the remaining $255_{10}$ outputs from the decoders remain at logic 1

This device-select pulse can be used to turn on the solid-state relay shown in the circuit presented last month.[3] The program listing, which is analogous to the previous one, is given below.

So far, we have discussed the interfacing technique called accumulator I/O, which is also known as isolated I/O.[2] A much more exciting interfacing technique is memory I/O, also known as memory mapped I/O,[2] in which an I/O device appears to the microcomputer CPU as a simple memory location. Without question, memory I/O will be the most popular interfacing technique among all of the different microprocessor families. One important advantage of this technique is the considerable number of IC chips that already have been designed for memory I/O applications. Included among such chips are the 8255 programmable peripheral interface, the 8251 universal synchronous/asynchronous receiver/transmitter (USART), the MC6820 peripheral interface adapter, and the XC6850 asynchronous communications interface adapter. We will discuss this alternative I/O technique in next month's column.

| Memory address | Octal instruction | Description |
|---|---|---|
| 0 | 323 | Send device-select pulse to device given by the following 8-bit device code |
| 1 | 321 | Device code for clear input to SN7474 flip-flop |
| 2 | 166 | Halt the microcomputer |

## References


1. *Bugbook III. Microcomputer Interfacing Experiments Using the Mark 80[R] Microcomputer, an 8080 System,* E & L Instruments, Inc, Derby, Conn, 1975
2. *Intel 8080 Microcomputer Systems User's Manual,* Intel Corp, Santa Clara, Calif, 1975
3. D. G. Larsen, P. R. Rony, and J. Titus, "Microcomputer interfacing: The 8080 microcomputer output instruction," *American Laboratory,* Dec 75, pp 75-77



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CIRCLE 85 ON INQUIRY CARD

## µComputer System Package Eases User Development Problems

Manufacturers of the Abacus Microware™, a complete package of hardware, software, development tools, and technical support, claim that its use will result in savings of both money and time in developing applications-oriented microcomputer-based systems. Key elements are Abacus Microsystem™ hardware and logic modules, Commander MDS™ development system, and p/ROM programmer. Users may purchase systems either in preassembled kits or fully assembled and tested.

Modules required by every Microsystem include:

*MPU*—contains Intel 8080 central processor with all 40 pins brought to a module connector

*System, Clock, and Control*—contains major support functions such as bidirectional 3-state buffer for MPU data lines, I/O and memory control, phase 1 and 2 clocks for MPU, and Schmitt input to a latch to provide reset for the 8080

*System I/O Logic*—provides general-purpose logic functions, in particular that necessary for the priority interrupt control module

*Dual 8-Bit I/O Port*—has two major functions: serves as address buffer for lines from MPU module and is used as data I/O module of an 8-bit parallel I/O structure

I/O modules used in addition to the dual 8-bit port include:

*Single 8-Bit I/O*—used as data input or output of an 8-bit parallel I/O structure

*Priority Interrupt Control*—sets priority of interrupts entering the system and provides other functions associated with I/O port

*Extended Priority Interrupt Control*—priority encoder for eight interrupts

*Programmable Serial I/O*—creates serial output data from parallel data on the MPU bus and parallel data from serial data input to the bus

*Baud Rate Generator*—provides clock for the serial I/O module

Memory modules are 512-byte RAM, and 512-, 1K-, 1.5K-, and 2K-byte p/ROM. An address decode module, containing three 1-of-8 decoders, selects RAM and p/ROM when multiple modules are used, and in addition decodes I/O addresses. System checkout modules include step control, address compare logic, status latch, display module, and MDS I/O logic.

Chassis are available with 10-, 19-, and 38-card slots to handle most systems. Power supplies provide 5, 12, and −5 V at various current ratings depending on size of the system. An extender module is available for aid in hardware debugging.

Commander MDS hardware elements consist of:

*Central Processor*—is built around an 8080 MPU and has eight I/O ports; memory is in 8K increments

*Keyboard*—53-key, ASCII format for operator communications

*CRT Display*—standard, commercial, B/W TV set which displays 24 lines of information at 40 char/line; displays all system operational messages

*Cassette Tape Units*—one performs read, the other write functions

*Printer*—optional; a bidirectional, matrix unit rated at 110 char/s or 65 lines/min.

Five major software packages are supplied:

*System Monitor*—composed of program loader for communication with cassette tape units; interactive debugger which allows programmer to display data in development system memory and store changes or connections; and I/O subroutines that provide interfaces to the development system's I/O devices

*Communications Monitor*—includes all functions of system monitor but also permits communication with Microsystem

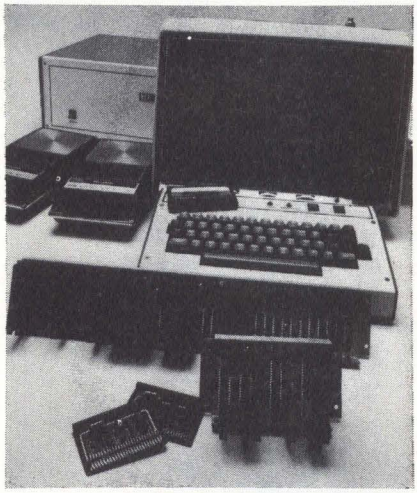
*Editor*—provides means for preparing and updating symbolic data stored on cassette tapes

*Assembly*—allows user to write all programs in Intel 8080 symbolic assembly language

*p/ROM Programming*—reads binary object tapes into user area

The p/ROM programmer may be purchased as a complete system made up of a series of modules in a 10-position card cage, connected by cable to an 8-bit parallel I/O port of the Commander MDS. Alternatively, the user may choose to have the programmer module within the prototype version of the Microsystem. According to Information Control Corp, 9610 Bellanca Ave, Los Angeles, CA 90045, its system debug package allows a user to test his microcomputer completely before committing his program to p/ROM.

Circle 170 on Inquiry Card



Abacus Microware™ package consists of all items needed to develop a microcomputer-based system. It contains hardware, software, development tools, and technical support and is available either in kit form or fully assembled and tested

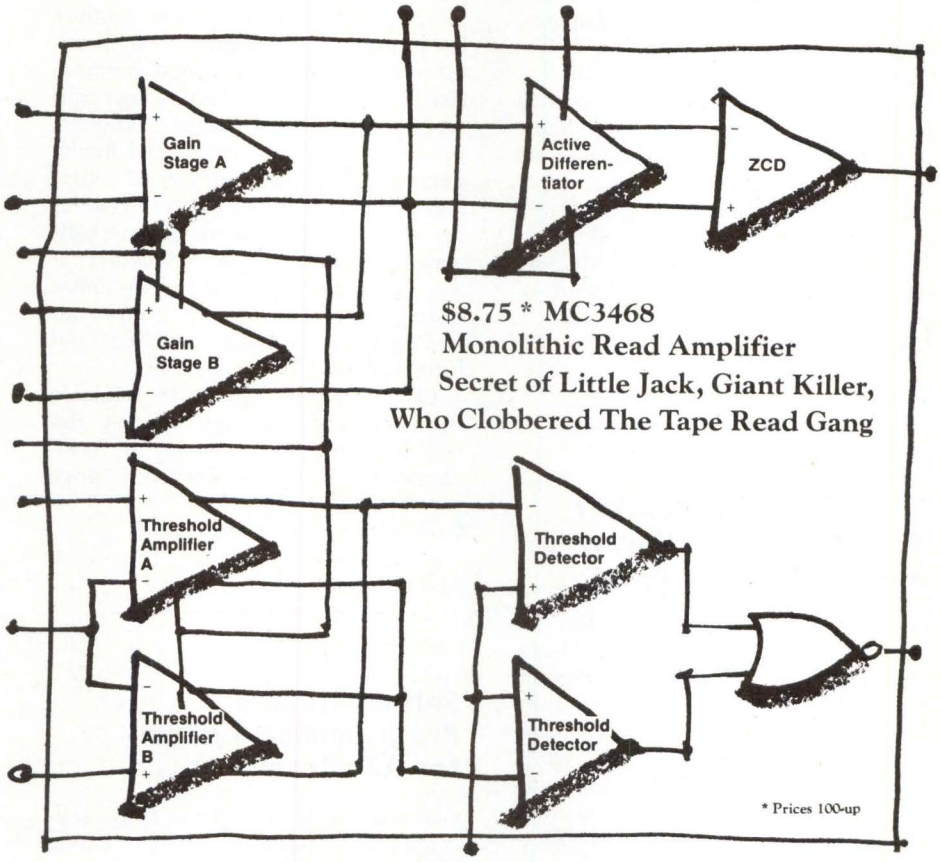
## Two Devices Extend Capabilities of 4-Bit µProcessor Systems

Software programmable LSI devices —a keyboard/display unit and a general-purpose I/O unit—have been added to the MCS-40 microcomputer systems by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. These systems are based on 4004 and 4040 4-bit CPUs and components that may be used with either.

Both units allow MCS-40 systems in most applications to be built with fewer components and to achieve significant increases in CPU throughput. Built-in logic functions simplify program routines and take care of local control functions for the CPU. In addition, the I/O device provides an interface between MCS-40 and MCS-80 systems based on the 8080A 8-bit processor unit.

Model 4269 keyboard/display unit is a general-purpose interface and control unit for "man-machine" communications devices such as keyboards, displays, panel switch arrays, sensor arrays, lamps, and indicators. As an input, for example, it can interface keyboards up to full teletypewriter size; as an output,

# Jack, The Giant Killer




In Peripheraland, there lived 5 terrible giants. The Tape Read Chain Gang some called them.

Anyone traveling through their forest with a bit of this or that wandered torturous paths. For it was vastly overgrown with componentry which boggled the mind and scratched the head. And the giants exacted much tribute from the unwary.

Many champions from the Valley had battled them. They always lost.

One day Jack arrived.

I am the giant killer, here to free you from the primitive bondage of the ogres for under 9 bucks, list.

You are small, cheap, and have a monolithic look, laughed the people. You will never function effectively in that tangled maze.

We'll see about that, said Jack. I have a secret. And he set off.

From behind a great clump of ICs sprang Input Multiplex, the first terrible giant.

Your NRZI or your life! he roared.

Let me go and I'll tell you a secret, said Jack.

Tell it at once, growled the giant.

Well, I not only handle phase, group and NRZI coding from 9-track but cartridges and cassettes as well, cried Jack, dancing about. And I can digitally select between two of these formats!

O, no! cried the giant and ran crashing off through the wood.

Soon Gaynstage, the second giant, confronted him.

Halt, he frothed.

Control yourself and I'll tell you my secret, said Jack.

Do so, grunted Gaynstage.

My EGC (Electronic Gain Controlled) amplifier provides differential outputs for the active differentiator and a single output is available for threshold function.

AAAGH! screamed the giant. How awful! and fell backward into a wayside pool and drowned.

The third giant, Threshold Amplifier/Detector, leaped from the undergrowth. He shook Jack till his teeth rattled and he could hardly explain his secret.

Tell it! the giant bellowed.

My threshold amp gives an output signal whenever it exceeds the setting in pos or neg direction, replied Jack.

The bully turned red and choked on his own phase jitter.

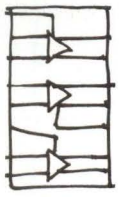
Much the same happened with the fourth and fifth giants, Active differentiation and ZCD. Jack revealed his ensured linearity, optimum zero-crossing detection for excellent noise rejection and strict avoidance of timing distortion.

He laughed at the giants' horrorstruck faces as they took off.

When he returned the elated people cut down the forest and made him king, as he deserved.

Now it's no secret with a little jack you can go out and kill some giants of your own.

But you already concluded that.



MC3467, advance man and partner of Jack. Has 3 EGC preamps, diff inputs/outputs and 15 MHz BW. Operates near mag heads for less than 4 bucks.

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it can control and refresh either numeric or alphanumeric displays, including Burroughs Self-Scan® displays.

Model 4265 general-purpose I/O unit provides four software-configurable I/O ports (16 I/O lines) and a variety of peripheral control capabilities. The four ports can operate in 14 software-selectable modes, enabling the unit to interface MCS-40 systems with virtually any kind of peripheral equipment.

Circle 171 on Inquiry Card

## Study of μP/μC Market Delves Into User/Buyer Satisfaction and Plans

Orders are now being accepted for the "Survey of Microprocessor/Microcomputer Buyers," a market research report prepared jointly by the publishers of *Computer Design* magazine and International Data Corp, an industrial market research company. Basis of the report is data obtained from a survey of those *Computer Design* readers who are specifically associated with microprocessors/microcomputers (μPs/μCs).

Of the 40,000 readers who buy or use μPs/μCs, 18% completed lengthy questionnaires that delved deeply into their experiences and preferences. For instance, they were asked how many μPs/μCs they used, where they used them, and what functions were served by them. They were also asked to identify which μPs/μCs they were using (by manufacturer and model number), what technical and nontechnical criteria were decisive in making choices, and how well these devices served their intended purposes.

Further questions were based on memory, peripherals, and software—with room for the users to specify manufacturers, models, and reasons for making their choices. In particular, the questionnaire gave users the opportunity to point out and discuss both advantages and deficiencies of the μPs/μCs that they had in their systems. They also were asked to list recommendations of how manufacturers could better serve their customers.

This study was designed to aid manufacturers of μP/μC and all related devices or systems in tracking μP penetration into existing product lines and in developing new products. Authors of the report summarized data into the following content areas: μP/μC usage, function, product status, and vendor and model selected; suitability of μP/μC offerings; vendor, model, and reasons for choosing specific memories; software incorporated and whether it was purchased or developed in-house; testing methods; use of peripherals and opinions of those available; and future plans for using μP/μC.

Copies of the report are available from Computer Design Market Research Group, 143 Swanton St, Winchester, MA 01890. Per copy price is $395.

Circle 172 on Inquiry Card

## Self-Contained Programming System for All μProcessors

Claimed to be the first, fully self-contained, portable programming system which can be universally applied to all microprocessors now on the market, μScope model 8000 contains a full alpha keyboard, 10-key numeric pad, control keys, CRT display for instantaneous program viewing, full alpha printer for documentation, magnetic tape cartridge device for program storage, and expandable memory with up to 57K of user space. Users have everything needed to write and document programs for any programming objective. In many cases they can reportedly double their programming output over traditional programming methods.

The software package is resident in ROM and consists of three parts: monitor, editor, and assembler. Editor and assembler are interrelated since the software assembles the program as it is entered.

Monitor reads, writes, and verifies magnetic tapes, copies and compares blocks of memory, allows direct entry or modification of any memory location, and has the capability for multiple traps or breakpoints in the program. Entries are via numeric key pad rather than toggle switches, and control keys are provided to set address, examine, backspace, clear, deposit, and run.

Editor features control keys which facilitate program entry, enabling the user to set, increment, and decrement program addresses and label, list, move, assemble, and disassemble programs. Programmers can alter or rework existing or in-progress programs as the need arises, and can selectively list the entire program or portions thereof on the printer as required.

Assembler is designed to convert user entries into object codes; the only additional memory required is for labels. Typically, object code and labels will consume equal amounts of memory space, resulting in 50% efficiency of memory use. Thus, 2K of object codes can be generated with only 4K of user memory.

Introduced by Tranti Systems, Inc, 1 Chelmsford Rd, North Billerica, MA 01862, the system is priced at $6995. Delivery is within 30 days from date of order after June 1.

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## KPRAM Emulates p/ROM, Reduces Program Development Costs

For use in development of microprocessors, minicomputers, and other digital systems, the keyboard programmable random access memory (KPRAM), developed by Sunrise Electronics, 228 N El Molino, Pasadena, CA 91101, can be used in place of the p/ROM, thereby significantly reducing costs. The KPRAM allows the user to alter memory contents in-circuit. It is coupled with a 16-key keyboard and is directly circuit interchangeable with p/ROM through the normal p/ROM socket.

Hexadecimal byte data are in-circuit, byte alterable, and are entered by keyboard. Memory address is selected by toggle switches. The 3-state data bus is active only when the data key or display memory button is depressed. Eight LEDs above the keyboard continuously display information on the data bus, or will

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| | 17.0 | EC2N17 | 101.00 | 82.00 | 78.00 |
| | 25.0 | EC2N25 | 137.00 | 112.00 | 106.00 |
| 5 V. | 3.0 | EC5N3 | 31.00 | 24.95 | 22.95 |
| | 6.0 | EC5N6 | 51.00 | 41.50 | 39.00 |
| | 9.5 | EC5N9.5 | 63.00 | 51.00 | 48.50 |
| | 12.0 | EC5N12 | 80.00 | 65.50 | 62.00 |
| | 17.0 | EC5N17 | 101.00 | 82.00 | 78.00 |
| | 25.0 | EC5N25 | 137.00 | 112.00 | 106.00 |
| 6 V. | 2.6 | EC6N2.6 | 31.00 | 24.95 | 22.95 |
| | 5.4 | EC6N5.4 | 51.00 | 41.50 | 39.00 |
| | 8.5 | EC6N8.5 | 63.00 | 51.00 | 48.50 |
| | 11.0 | EC6N11 | 80.00 | 65.50 | 62.00 |
| | 15.0 | EC6N15 | 101.00 | 82.00 | 78.00 |
| | 23.0 | EC6N23 | 137.00 | 112.00 | 106.00 |
| 12 V. | 2.2 | EC12N2.2 | 31.00 | 24.95 | 22.95 |
| | 3.5 | EC12N3.5 | 51.00 | 41.50 | 39.00 |
| | 6.0 | EC12N6 | 63.00 | 51.00 | 48.50 |
| | 7.5 | EC12N7.5 | 80.00 | 65.50 | 62.00 |
| | 10.0 | EC12N10 | 101.00 | 82.00 | 78.00 |
| | 16.0 | EC12N16 | 137.00 | 112.00 | 106.00 |
| 15 V. | 1.8 | EC15N1.8 | 31.00 | 24.95 | 22.95 |
| | 3.0 | EC15N3 | 51.00 | 41.50 | 39.00 |
| | 5.0 | EC15N5 | 63.00 | 51.00 | 48.50 |
| | 6.5 | EC15N6.5 | 80.00 | 65.50 | 62.00 |
| | 9.5 | EC15N9.5 | 101.00 | 82.00 | 78.00 |
| | 14.0 | EC15N14 | 137.00 | 112.00 | 106.00 |
| 20 V. | 1.5 | EC20N1.5 | 31.00 | 24.95 | 22.95 |
| | 2.5 | EC20N2.5 | 51.00 | 41.50 | 39.00 |
| | 4.2 | EC20N4.2 | 63.00 | 51.00 | 48.50 |
| | 5.3 | EC20N5.3 | 80.00 | 65.50 | 62.00 |
| | 8.0 | EC20N8 | 101.00 | 82.00 | 78.00 |
| | 11.0 | EC20N11 | 137.00 | 112.00 | 106.00 |
| 24 V. | 1.3 | EC24N1.3 | 31.00 | 24.95 | 22.95 |
| | 2.4 | EC24N2.4 | 51.00 | 41.50 | 39.00 |
| | 4.0 | EC24N4 | 63.00 | 51.00 | 48.50 |
| | 5.0 | EC24N5 | 80.00 | 65.50 | 62.00 |
| | 7.5 | EC24N7.5 | 101.00 | 82.00 | 78.00 |
| | 10.0 | EC24N10 | 137.00 | 112.00 | 106.00 |

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|---|---|---|---|---|---|
| ±12/15 | 0.5 | EC12D0.5 | $ 45.00 | $ 38.00 | $ 35.00 |
| ±12/15 | 1.5 | EC12D1.5 | 69.00 | 57.00 | 53.00 |
| ±12 | 3.0 | EC12D3 | 89.00 | 72.00 | 67.00 |
| ±15 | 3.0 | EC15D3 | 89.00 | 72.00 | 67.00 |
| ±12 | 5.0 | EC12D5 | 122.00 | 99.00 | 92.00 |
| ±15 | 5.0 | EC15D5 | 122.00 | 99.00 | 92.00 |

## TRIPLE OUTPUT POWER SUPPLIES

| Nominal Output Voltage (amps) | Max. Current | Model Number | Price 1 | 100 | 250 |
|---|---|---|---|---|---|
| 5V | 6.0 | ET401 | $113.00 | $ 92.00 | $ 85.00 |
| ±12/15 | 1.0 | | | | |
| 5V | 12 | ET601 | 165.00 | 135.00 | 125.00 |
| ±12 | 3 | | | | |
| 5V | 12 | ET602 | 165.00 | 135.00 | 125.00 |
| ±15 | 3 | | | | |

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| 12 to 25 Amps | 12.00 | 10.50 | 10.00 |

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display contents of memory on command. KPRAM is compatible with MOS, TTL, and CMOS interfaces.

Four standard memory sizes are available: 256 x 4, 256 x 8, 512 x 4, and 512 x 8, with standard pinouts or customer wired adapter cable. An optional power supply with rechargeable battery pack permits out-of-circuit programming and power failure backup. Unit measures 8.25 x 5.25 x 1.60"; weight is 12 oz.

Circle 174 on Inquiry Card

## Adjustable Output Power Supplies Prevent Logic Circuit Interaction

Multiple-output, IC-regulated supplies for OEM use with microprocessors, offered by Sola Electric Div of Sola Basic Industries, 1717 Busse Rd, Elk Grove Village, IL 60007, feature fully isolated, independent outputs to prevent interaction between microprocessor logic circuits. Four dual- and four triple-output models provide most often required voltage combinations; several units have adjustable outputs. Output power levels will also accommodate accessories such as RAMs, ROMs, FPROMs, clocks, and I/O devices.

Input voltage range is 104 to 127 or 208 to 254 Vac and frequency range is 50 to 400 Hz, in conformance with Appendix B of ANSI C84.1 –1975. Outputs are regulated to within 0.05% of rated voltage throughout line voltage variations of up to ±10%.

All models are equipped with automatic current limiting, short circuit protection, and reverse voltage protection. Overvoltage protection is standard on all 5-V outputs, and available as an option on all others. Components are mounted on an open heatsink frame for effective convection cooling and serviceability. The package allows either horizontal or vertical mounting.

Circle 175 on Inquiry Card

## Triple-Output Microprocessor Power Supply

Model μPS-35 may be used to power Intel 8080, TI TMS 8080, AMD 9080, Mostek F8, Motorola M6800, and other microprocessors with similar power requirements. Three outputs provided are 5 V/3 A (0.1% regulation); 5 V/0.6 A (0.3% regulation); and 12 V/0.3 A (0.3% regulation). Full rated current is delivered over the entire temperature range from 0 to 55°C with 115/230-V, 47- to 63-Hz inputs.

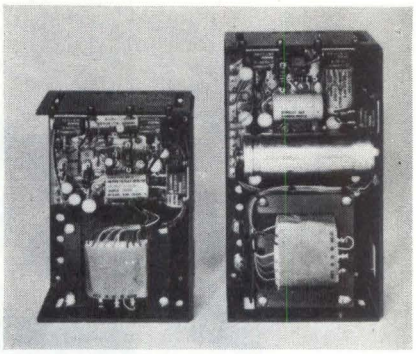
Standard features of these supplies from Elexon Power Systems, 3131 S Standard Ave, Santa Ana, CA 92705 include IC regulation, isolated outputs for positive or negative operation, remote sensing, foldback current limiting, and spike suppression. Overvoltage protection can be provided for all outputs, and the supply can be certified to meet UL requirements.

Circle 176 on Inquiry Card

## Triple Output Power Supplies Control μProcessors

MPU-1 and -2, designed for laboratory, breadboard, engineering prototype, pilot production, and limited production systems, can power any microprocessor and its associated clock, ROMs, FPROMs, RAMs, p/ROMs, memories, and I/O chips. Outputs for the -1 are 5 and 12 V ±5% adjustable, and 9 to 12 V ±5% adjustable; outputs for the -2 are 5 and 12 V adjustable and 9 V fixed.

All of the MPU power supplies introduced by Lambda Electronics, 515 Broad Hollow Rd, Melville, NY 11746 contain three hybrid overvoltage protectors that can maintain



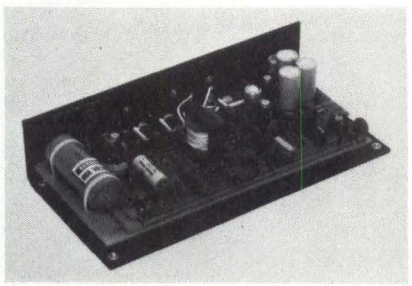
triple voltage tolerance over 71°C temperature range. Features include dual input voltage for domestic and overseas use (105 to 125 or 210 to 250 Vac), electrolytic capacitors for reliability, hermetically sealed IC regulators, Darlington silicon power transistors, hermetically sealed semiconductors, and vacuum impregnated magnetics.

Electrical specifications include line and load regulation, 0.15% each; ripple and noise, 1.5 mV rms, 5 mV pk-pk; temperature coefficient, 0.03%/°C. Supplies are convection cooled; no heat sinks or forced air is required. There is no overshoot under conditions of power turn-on, turn-off, or failure.

Circle 177 on Inquiry Card

## Switching Power Supply

Model 0L80, from Boschert Associates, 1031 E Duane, Suite C, Sunnyvale, CA 94086, is a 4-output, 2 lb switching-type power supply designed to power microprocessor systems. Its output voltages are 5 V at 10 A max, ±12 V at 2 A max, and either −9 or −5 V at 2 A max. Total power output is 80 W max. Overvoltage, overcurrent, and reverse voltage protection is standard.



Circle 178 on Inquiry Card

# Spend less and get a PROM Programer you can talk to.

Using plug-in personality modules, the inexpensive Series 90 can program almost any AMD, Harris, Fairchild, Intel, Intersil, Monolithic Memories, Motorola, National, Signetics or Texas Instrument bipolar or MOS PROM made. Contact us for information on the specific module you need. Series 90 shown with personality module installed and with optional MOS PROM erase light.

Close-up of Series 90 control panel.

**Pro-Log's Series 90 simplifies the interface between man and machine.**

Pro-Log's Series 90 PROM programer gives you a simple, straightforward method of programing, duplicating or verifying MOS or bipolar PROMs. You program straight from a hexadecimal keyboard so there's no need to learn computer talk. The Series 90 interacts with you and leads you through the programing process so there's less chance for error. Addresses and data appear on a six digit hexadecimal display. Thanks to our plug-in personality modules, display and formatting adjust automatically to accommodate PROM type or size.

The Series 90 can also duplicate PROMs directly from pre-programed master PROMs, with corrections if necessary.

It has a light indicator to tell you whether or not a PROM is completely blank and will automatically indicate an unprogramable PROM.

It weighs less than 15 pounds and comes in an attache case. An optional bench top model is available.

**Guards against MOS PROM data loss.**

Pro-Log's field-proven programing technology protects against MOS PROM data dropout caused by improper or inadequate programing pulses.

**Tailor it to your needs.**

We have standard options to interface it with TTY, paper tape readers and punches, or computers.

**Low-priced.**

A Series 90 control unit costs $1,800. Personality modules range from $350 to $550.

**We have other microprocessor-based instruments and microprocessor subsystems, too.**

Our instruments include analyzers for systems using 4004, 4040, 8008, 8080 and 6800 microprocessors.

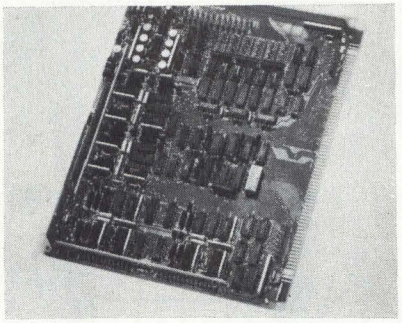
Our microprocessor subsystems include 4004 and 4040 logic processors and 8008, 8080, and 6800 microcomputers.

For more information on the Series 90, including a complete list of the many personality modules currently available, send for a copy of our PROM User's Guide.

**PRO-LOG CORPORATION**
**2411 Garden Road**
**Monterey, CA 93940**
**Telephone (408) 372-4593**
**TWX 910-360-7082**

## Non-Volatile Add-On Memory Functions as RAM, p/ROM

PM-MP8, a complete standalone core memory system, has been introduced by Plessey Microsystems, 1674 McGaw Ave, Irvine, CA 92714 to fulfill the functions of both RAM and p/ROM in a microprocessor system. It can be used as a 16K x 8-bit or 8K x 16-bit memory. Fully compatible with National Semiconductor's IMP-16C, -16P, -8C, -8P, and Pace microprocessors, it can also be used to replace the IMP-16P/004A RAM or as an add-on memory module, and features a separate I/O data bus, 3-state outputs, access time under 450 ns, and programmable address select.



An optional memory control card which enables the memory system to be used with the IMP-16L and other 16- and 8-bit microprocessors provides write protect to prevent inadvertent program modification, data protect for memory contents during power-up and power-down sequences, address partitioning with up to 16 pages/memory, memory expansion up to 65K 16-bit words, and a flexible I/O that allows the memory to interface with a separate or common I/O data bus and synchronous or asynchronous controls.

Circle 179 on Inquiry Card

## Multifunction I/O Controller Operates Under Software Control

A versatile high performance I/O controller which replaces five or more regular 8080/8080A support circuits, the TMS 5501 is compatible with TI's TMS 8080, and 8080A's furnished by others. An important feature of the circuit is its programmability—it operates under 8080 or 8080A software control. Five timers are programmable to generate interrupts after counting intervals of up to 16 ms; they also can be cascaded for longer intervals. Versatility is increased since the programmable baud rate allows communication with equipment of different speeds.

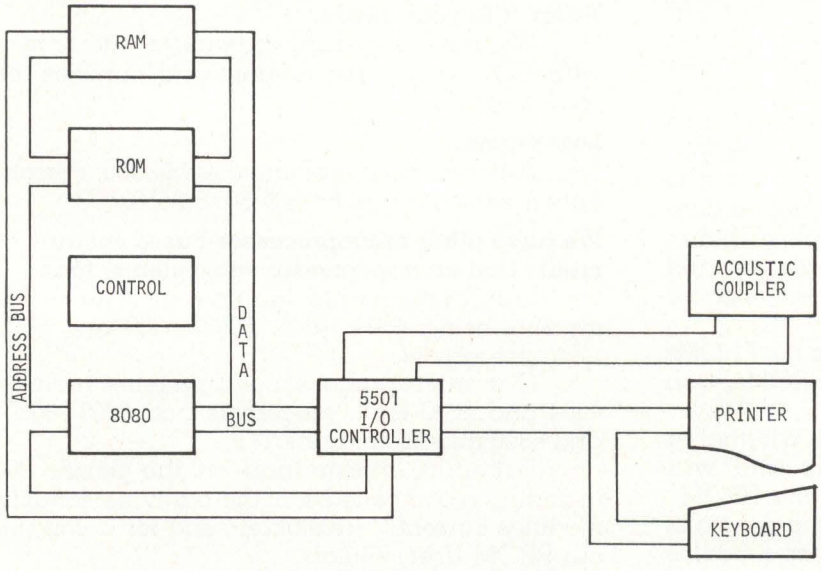
The controller was announced by Texas Instruments Inc, PO Box 5012 M/S-84, Dallas, TX 75222. It combines on one circuit the functions which normally require several devices. This provides for transmission of serial data, 8-bit parallel data I/O, efficient interrupt servicing, and interval timing.

Asynchronous serial data are handled at baud rates of 110, 150, 300, 1200, 2400, 4800, and 9600, selectable by software. Eight-bit output and input ports transfer data to and from the TMS 8080 and other components.

Eight interrupts are ranked by priorities, and the appropriate RST instruction is generated for the 8080. Interrupts are individually maskable by software; they can be accepted as they occur or can be polled. Applications include data terminals, POS equipment or any system requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous data.

Packaged in 40-pin ceramic, TMS 5501 JL is available immediately. TMS 5501 NL (plastic-packaged version) will be available soon. Unit price is $32.80; quantity prices are also available.

Circle 180 on Inquiry Card




Use of an I/O controller as direct interface eliminates need for six 8080 support circuits. In addition to cost savings, the system gains increased versatility through programmability

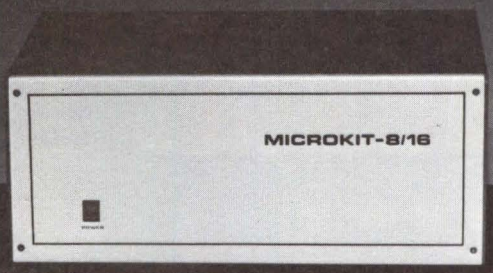
## µComputer NC

A microcomputer numerical controller announced by Aivex, Inc, 6 Preston Court, Bedford, MA 01730 has digital ramping for drift-free operation and program storage in nonvolatile read-only memory. Floating zero point, 3-speed manual jog, mirror image, and single-step mode are standard. Tape is either EIA or ASCII with both absolute and incremental commands. Step and repeat function allows sections of the control tape to be automatically repeated. Options include manual data input via digital thumbwheel switches, sequence number and coordinate displays, and in./mm conversion.

Circle 181 on Inquiry Card

# A Complete 8080 Microcomputer Development System for

# $3,850.00




## If you use microcomputers, you are probably paying too much for a Microcomputer Development System.

An effective microcomputer development system must have the capability for convenient editing, assembling, and rapid interactive debugging. To achieve this, the system should not only have adequate memory and software, but it should also include a CRT display terminal and high performance mass storage.

You might pay as much as $12,000.00 to get these features. The MICROKIT-8/16 offers them all for only $3,850.00.

The MICROKIT-8/16 is a complete stand alone system for writing, debugging and executing programs on the 8080 microprocessor. The MICROKIT-8/16 comes with an 8K memory, an alphanumeric CRT display, an ASCII keyboard and two cassette tape units. Its superior software includes a monitor/debugger, editor and assembler designed to take full advantage of the high-speed multi-line CRT display and the tape I/O.

The MICROKIT-8/16 has been designed to make effective use of standard television sets and audio cassette recorders as I/O devices. The system's overall cost is lowered by the use of these peripherals, which have proven to be reliable and easily serviced. Because of MICROKIT's proprietary recording technique, data is transferred to audio cassettes at the rate of 2000 bps with data reliability comparable to digital cassette units.

Program development time is significantly reduced by the unique MICROKIT hardware/software package.

The 8080 is only the first of a series of processors to be supported by the basic MICROKIT-8/16 system. The modular nature of the system makes it adaptable to other popular 8 and 16 bit processors.

The MICROKIT-8/16's superior features at a low cost make it an obvious choice for the designer requiring a microcomputer development system. Write or call MICROKIT INC. today, (213) 828-8539, to see how well the MICROKIT-8/16 fits your present microcomputer development requirements.

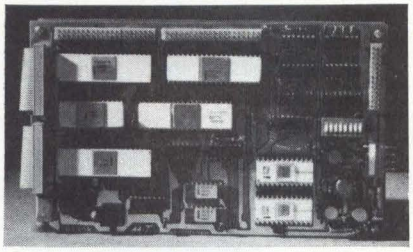
# MICROKIT INCORPORATED

2180 COLORADO AVENUE □ SANTA MONICA, CALIFORNIA 90404 □ (213) 828-8539

**NCC Booth No. 1034 — Circle 89 On Inquiry Card**

## Single-Card Microcomputer

MT 80, a single-card microcomputer designed for the OEM, contains an 8080 CPU, 2K bytes of EPROM, 256 bytes of RAM, 48 programmable



I/O bits, and an RS-232 port. An optional oncard converter gives single 5 V only operation. If the converter is not used, a ±12-V and 5-V supply is required.

Other features of the device introduced by Mycro-Tek, Inc, 216 N Washington, Wichita, KS 67201 include a switch-selectable RS-232-C clock rate to give most standard rates from 110 to 9600 baud, and power-on reset that can be expanded to a larger configuration using add-on cards. Memory can be increased by adding 4K bytes of RAM and 2K bytes of EPROM.

Circle 182 on Inquiry Card

## Microcomputer System Cards Satisfy OEM Needs

OEM microcomputer system cards, announced by Microcomputer Associates Inc, 2589 Scott Blvd, Santa Clara, CA 95050, are designed as low cost, standalone cards with full microcomputer capability including p/ROM, RAM, and I/O. The series consists of four cards based on the 8080A, 6502, 6800, and 2650 microprocessors. Card features include crystal-controlled clock; 1K x 8 static RAM, 2K x 8 p/ROM, or 4K x 8 masked ROM sockets; 24 bidirectional I/O lines; and fully buffered address/data lines. An interconnection technique minimizes the cost of card cages and backplanes for additional cards.

The cards, offered with several microprocessors, can replace a wide range of existing designs. To further support this series, 4K x 8 RAM cards; 2K, 4K, or 8K x 8 p/ROM cards; I/O cards; power supplies; and software applications support are available. Prices start at $375 per single unit; $295 per 100. Delivery is 30 to 45 days.

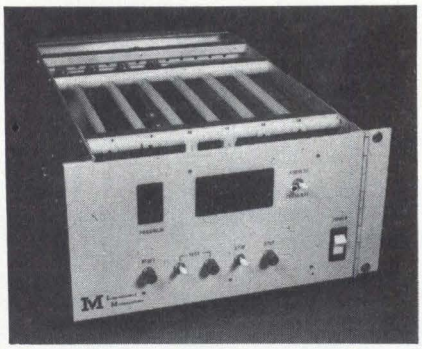
Circle 183 on Inquiry Card

## Ready-to-Use µComputer Adaptable as Center of Control System

Featuring a versatile I/O structure, the 4060 microcomputer is designed around a half- or full-size Cambion bin card cage which has 13 slots for 4.5 x 9.25" cards. The swingout front panel is divided into two sections: one half for 4060 function controls and the other half for the users' displays and switches.

International Microsystems, Inc, 122 Hutton St, Gaithersburg, MD 20760, claims that this 4-bit microcomputer can be adapted as the center of a control system. Useful to system engineers for control and measurement applications, it increases performance capability and reduces system development time and costs. Various communication links available in the system provide solutions to custom interface designs. Interfaces can be to RS-232 or current loop terminals.

The unit comes ready to use with a prewired backplane, terminal I/O connectors, and a triple voltage power supply which provides 5 V at 5 A and ±12 V at 1 A. Also included are 4041 CPU board, 4050 terminal control board, front panel PC board (supporting all control switches), specially designed extender card, and 2K x 8 of program memory on the CPU card.



Packaged in standard Cambion bin, the 4060 microcomputer incorporates the Intel 4040 with 1K of RAM and 1K of p/ROM. The system (shown in half-rack configuration) includes CPU board with fully decoded TTL-compatible I/O structure, RS-232 and 20-mA current loop TTY interface card, and front panel driver board

Terminal interface card and software system monitor allow simple program development. The microcomputer is supported with two software packages and is documented with five manuals: 4041 CPU board, 4050 terminal interface board, series 4000 system monitor, series 4000 test p/ROM, and 4060 microcomputer system.

Hardware debugging software is provided as preprogrammed test p/ROM allowing easy testing of external system components and custom interfaces by use of front panel controls. The 4000 system monitor permits software in RAM memory to be loaded and modified before the program is committed to p/ROM memory. System cost is $1195 (single quantity); delivery is 15 days ARO.

Circle 184 on Inquiry Card

## Cross-Assemblers Feature MACRO Assembly Software

Claimed to provide great cost and time savings, a series of microprocessor cross-assemblers, developed by Boston Systems Office, Inc, Waltham Mass, features assembly software written completely in MACRO. This allows the creation of macro routines, has complete conditional capabilities, produces object code for the target device, and is said to be faster than cross-assemblies with FORTRAN programs available from hardware manufacturers.

Assemblers are available on a commercial timesharing network. The series is for the Intel 4000 and 8000 series, Fairchild F8, Motorola 6800, Mostek 6500 series, Texas Instruments 9900 and 1100, and National Semiconductor Pace microprocessor. Assemblers also are available for TI 8080, NEC 8080, and Mostek F8; plans are to develop similar software for other microprocessors. Software is for sale or lease on DEC-system-10 and PDP-11 computers from Sofco Inc, 4 Lakeside Office Pk, Wakefield, MA 01818.

Circle 185 on Inquiry Card

# FULLY INTERFACED TAPE & DISC SYSTEMS for the PDP-11

**See these and other WANGCO tape and disc products at the NCC, June 7 through 10, Booth 1521.**

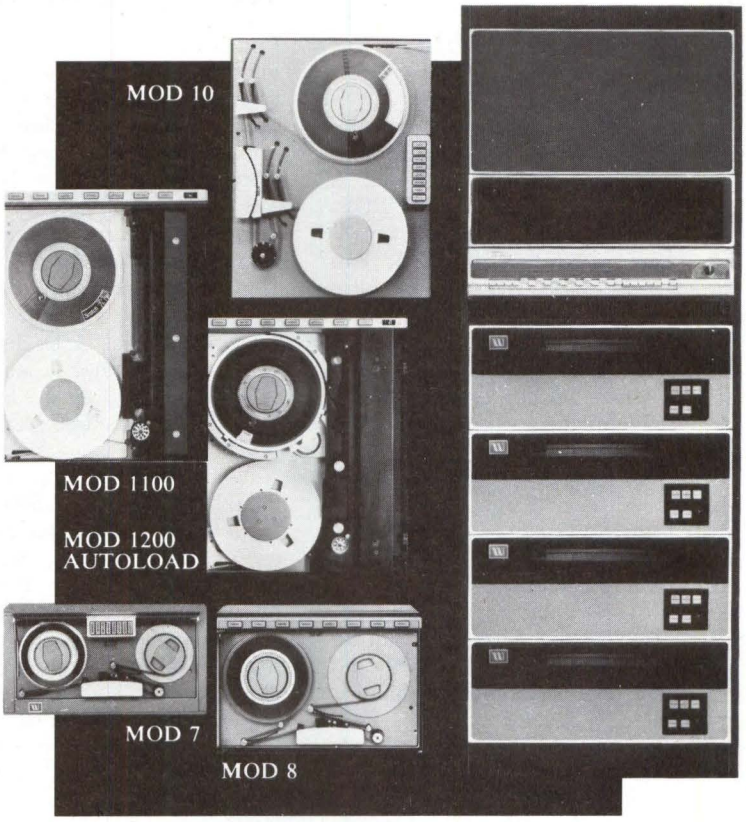
## High capacity, low cost...from a SINGLE SOURCE!

WANGCO's new disc and tape controllers for the PDP-11 *(following our successful NOVA systems)*, give you expanded capacities not presently available, and at significantly lower cost.

Up to four WANGCO disc drives can be daisy chained to a single WANGCO controller to achieve a maximum of *40 million bytes of storage.*

WANGCO tape systems provide up to four times more tape flexibility than any other manufacturer. Systems include WANGCO's widely accepted, dependable magnetic drives, configured to meet your system requirements.

Expand your PDP-11's capability, with increased disc or tape capacity, at many times the operating flexibility presently available.




*Phone or write for your WANGCO SINGLE SOURCE DATA PACKAGE, for the PDP-11 and NOVA.*

**WANGCO** INCORPORATED

SETTING THE PACE IN PERIPHERALS

5404 JANDY PLACE — LOS ANGELES, CALIFORNIA 90066 ■ (213) 390-8081, TWX-910/343-6246

*Offices in principal U.S. cities.*

*In Europe:* WANGCO Incorporated, The Lodge, 362 Cranford Lane. Harlington, Middlesex, England. Telephone 897-0202. *Offices in* France, Germany, Spain, Sweden, Norway, Finland, Switzerland, Australia, Canada, Israel, Japan, New Zealand and the Philippines.

## Companies Agree to Alternate Sourcing for Microcomputer Products

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, and Siemens, Munich, Germany, have agreed to a cooperation agreement encompassing microcomputer semiconductor products and related software and support systems. The agreement, covering both present and future systems, will establish alternate sourcing of each others' products, and is expected to help both companies develop and promote the use of microcomputer products and technology.

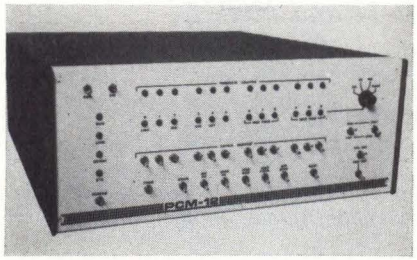
Circle 186 on Inquiry Card

## Kit Computer Is Software Compatible With DEC PDP-8/E

A general-purpose minicomputer designed around the Intersil IM6100 microprocessor chip, the PCM-12 is software-compatible with DEC PDP-8/E. The 12-bit static device is available from PCM, PO Box 215, San Ramon, CA 94583, either in kit form or preassembled and tested. Completed, the kit can execute nearly all PDP-8 software, including assemblers, editors, debug routines, advanced languages (eg, BASIC and FORTRAN), and DEC's OS-8 operating system. Much of this software, which is written, debugged, and documented by DEC, is available on an unlicensed, over-the-counter basis.

Bus-oriented architecture provides identically-operating card slots. TTL-compatible 80-line bus holds up to 15 cards for device interfaces and additional memory. The machine is equipped with a 4096-word by 12-bit memory card, and is expandable up to 32K words.

Flexibility ensures future expansion through provision for a vectored, priority interrupt system, and direct memory access. The control panel provides essentially all PDP-8/E functions, plus a built-in binary bootstrap loader, and decrement-address function.



Complete minicomputer kit contains CPU, control panel, 4K-word static memory card, cabinet, and power supply. Assembly requires loading five PC boards. TTY, cassette recorder, and other interfacing modules are available. Basic kit price is $799; assembled and tested it is $1224.

Circle 187 on Inquiry Card

## Measuring/Recording System Monitors Terminal Networks

Consisting of standard company microprocessor products plus a teletypewriter unit, the RTM-3000 response time measuring and recording system, introduced by Heurikon Corp, 700 W Badger Rd, Madison, WI 53713, is designed to aid efficiency monitoring of interactive terminal networks. An MLP-8080 card contains the processing element, program memory, random access memory, and serial I/O interface (for the teletypewriter); an MLP-8030 I/O interface card communicates with the MLP-8080 via a universal bus board.

The device to be monitored is linked to the MLP-8030 I/O card by a cable and monitor channel interface (MCI) unit, which isolates the RTM-3000 from the unit being monitored. One to 30 MCI units can be connected to a system. Devices may be added or removed without changing the control program. If no inputs are received over an input channel, no report is generated for that channel.

Response time data are accumulated by the system from devices connected to MCI units. Each device is monitored continually and is handled independently from the others. Response times are categorized into eight adjustable time windows; report summaries are generated automatically at user designated intervals.

Operator inputs consist of initialization requests for single device channel or the entire system, adjustment of internal real-time clock, request for printout of accumulated data in one of several formats, and input of miscellaneous limits and other data. Outputs consist of printout of real-time clock on request or when response time exceeds present limit and reports of accumulated data for each device and averages for all devices. The system's standard configuration has a resolution of 50 ms with max timing count of 10.9 min., but it can also be configured for longer or shorter timing count resolutions.

Circle 188 on Inquiry Card

## Microprocessor Programming Module Is Digitally Operated

A programming module using microprocessor techniques is offered as a standard option by Tenney Engineering, Inc, 1090 Springfield Rd, Union, NJ 07083 as a substitute for cam, 2-point, or punched tape programmers. The module interfaces with all of the company's environmental test chambers which simulate temperature, humidity, and altitude in any combination. It is particularly useful in programming MIL-spec tests, including those required by AGREE procedures.

Containing programmable memory, the instrument is digitally addressed in English terms. After the operator introduces temperature and humidity set-points, times and rates of change, and time of program completion, the solid-state device automatically takes over. Activated modes are displayed digitally.

Circle 189 on Inquiry Card

## CTL to Support Users of Motorola Microprocessor

Computer Technology Limited, Eaton Rd, Hemel Hempstead, Hertfordshire HP2 7EQ, England, and Motorola Semiconductor Group, PO Box 20294, Phoenix, AZ 85036, have agreed that CTL is to give total support to existing and future microprocessor users. This agreement was developed in collaboration with Motorola distributors. CTL will provide support of the M6800 microprocessor covering all aspects of design, manufacture, and maintenance; the services range from initial exploratory consultancy through total system responsibility.

Circle 190 on Inquiry Card

# Announcing a giant reduction in the Nova line.

You're looking at a whole new family of NOVA® computers. microNOVA. A microprocessor chip, a microcomputer board and a complete MOS minicomputer. All based on the little thing on the tip of the finger.

mN601. The microNOVA CPU.

It's a full-blown, 16-bit NOVA computer. Manufactured by Data General. And fully supported by NOVA software.

And it's not a NOVA computer in name only. This chip has all the NOVA registers, internal data paths and computational elements. The NOVA multifunction instruction set. The NOVA multiple addressing modes. And the NOVA 3 hardware stacking. Plus things that used to be NOVA options: multiply/divide, real-time clock and power fail/auto restart. All standard at no additional cost.

The difference is, all that NOVA has been reduced to a single chip that measures only 225 mils by 244 mils.

Which was no small accomplishment.

For those who need more than a chip, there's the microNOVA computer-on-a-board. A complete, fully-buffered microcomputer that comes with 2K or 4K words of RAM on a single 7½" by 9½" board. You can add on more RAM in either 4K or 8K increments, or PROM boards with up to 4K words. Plus terminal interfaces, general purpose interfacing boards, card frame, power supply and PROM burner.

And for those who need more than a board, there's a fully-packaged 4K word MOS microNOVA mini. It comes with power supply and turnkey console. In 9 and 18 slot versions. Into which you can place as much as 32K words of RAM or PROM. And still have plenty of room left over for I/O.

There's even a microNOVA system specifically for program development. A complete system, with dual diskette drive, terminal and our RDOS-compatible Disc Operating System. Or you can use a Nova 3 system with RDOS. The best development software you can get.

And no matter which microNOVA product you get, you get to use NOVA software like FORTRAN IV. Software that's in use in over 20,000 installations all over the world. So you know it's going to work right the day you get it.

Want to know something else?
Call our toll free number.
800-225-9497.

**microNOVA**

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Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361/Sydney (02) 908-1366.

CIRCLE 91 ON INQUIRY CARD

PRODUCT FEATURE

# Medium Scale Computer Six Microprocessor

Designed to meet continuing expansion requirements of growing organizations, the Slash 6 medium scale computer provides exceptional flexibility for a system of its size. It may be expanded from a minimum configuration of three plugboards, including CPU, 16K MOS memory, and channel board, to a maximum multiboarded configuration of up to 256K words of memory, 32 I/O channels, scientific arithmetic unit, and CPU option boards including features such as interval timer and bit processor.

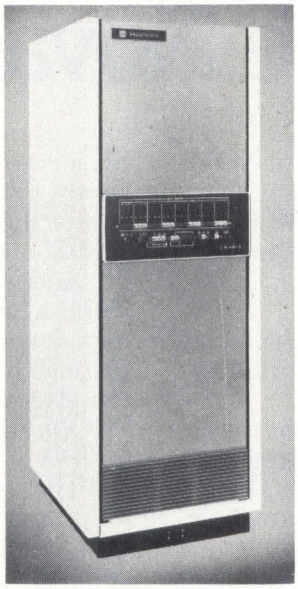
Price/performance value is maintained by use of six 4-bit bipolar microprocessor chips in the CPU. This architecture features direct memory address channels for high speed devices such as discs and magnetic tape equipment and a programmed I/O channel for devices of lower speeds. According to Harris Corp, Computer Systems Div, this processor offers 24-bit capability at prices competitive with 16-bit machines. It is fully software compatible with Slash 4, 5, and 7 computers. The entire CPU with p/ROM bootstrap and eight priority interrupts is packaged on a single 15.7 x 16.5″ multilayer PC board.

## Features

Microprogrammed architecture with a high degree of parallelism provides a superior level of performance which is further enhanced with block oriented direct-to-memory I/O operation for high speed devices. This I/O system also offers command and data chaining for scatter-write or gather-read requirements. An 8-bit programmed I/O channel is available for slow speed character-oriented devices. I/O system design allows peripheral controllers and their associated devices to be shared by multiple processors.

Basic processor architecture is oriented about a single system bus which has 48 data and 18 address lines. All major system elements communicate through this bus. A universal block channel transfers 48 bits to and from memory.

Use of 18-pin 4K RAMs on the semiconductor memory allows packaging of 48K bytes on a single board. A full system can contain 768K bytes, organized in 48K-byte increments. Single-bit error correction using a 5-bit code is a standard feature. Battery backup is optional.



*See at NCC Booth 2217*

Hardware add, subtract, multiply, divide, and square root functions are standard features. Data are represented in 2's complement binary, with fixed-point word lengths of 24 and 48 bits. Floating-point numbers have a 39-bit mantissa and an 8-bit exponent. Overflow, negative, zero, or positive status are determined after each operation with condition register bits set accordingly. All of the products and dividends are 48 bits long.

Over 120 generic instructions yield a set of up to 658 individual operations. Some of the operations include byte, word, and double-word; memory-to-register and register-to-register transfers; priority and I/O control; memory execution; and algebraic and logical comparison.

Effective cycle time is 600 ns. Transfer rates are 4.9M bytes/s input, 3.9M bytes/s output (both with one port active). Power requirements are 115 Vac ±10%, 16 A; or 320 Vac ±10%, 8 A; at 47 to 63 Hz. All equipment is mountable in standard 19″ RETMA cabinets with all cable and repair accesses from the front.

## Optional Features

In addition to those already mentioned, a number of options are available with this processor. For instance. two types of control panels are available. A full function programmers' panel supplies all of the switches and displays necessary to monitor and modify the contents of registers and memory. In addition, a turnkey panel is offered for those system applications not requiring the full functional programmers' panel.

A program restrict option allows areas of memory to be protected from unauthorized access. This system is enabled or disabled by a key switch on either of the panels. When enabled, the instruction trap

## Features

## Chips in CPU

causes an executive trap to be triggered when the processor attempts to execute privileged instructions.

The scientific arithmetic unit (SAU) is a hardware floating-point option. All floating-point operations are carried out in double precision format. Resultant exponent ranges are $2.94 \times 10^{-39}$ and $1.7 \times 10^{38}$. Forty-seven SAU operation codes are provided, including full mathematical functions and various branch and transfer operations. The unit has its own accumulators and condition register and is autonomous with respect to the processor. Data and condition information are displayed on the programmers' panel as a function of selectable shared indicators. An executive trap is provided for overflow/underflow conditions. Typical SAU instruction execution times are add/subtract, 2.58 $\mu$s; multiply, 5.58 $\mu$s; and divide, 10.98 $\mu$s.

Eight standard priority interrupt levels may be expanded to a maximum of 24 in groups of eight. External interrupts may be individually armed, disarmed, enabled, inhibited, or triggered under program control.

### Price and Delivery

Slash 6 with 48K bytes of MOS memory will be priced at approximately $14,500. Volume discount agreements will be available. First customer shipments will begin in August. Harris Corp, Computer Systems Div, 1200 Gateway Dr, Fort Lauderdale, FL 33309. Tel: (305) 974-1700.

**For additional information circle 199 on inquiry card.**


# CHECK DIGITAL IC'S FASTER THAN A SCOPE, SAFER THAN A VOLTMETER

You're looking at the most convenient and efficient way developed to check digital IC's: CSC's Logic Monitor. It speeds digital design and testing by accurately and automatically displaying static and dynamic logic states of DTL, TTL, HTL and CMOS DIP IC's. All in a compact, self-contained 16-pin circuit-powered unit.

Use it to effortlessly trace signals through counters, shift registers, gating networks, flip-flops, decoders...even entire systems made up of mixed logic families. It's a great way to cut minutes, even hours all along the line from design through debugging.

Nothing could be simpler: just clip it over any DIP IC up to 16 pins, and the Logic Monitor does the rest. Precision plastic guides and unique flexible web insure positive connections between non-corrosive nickel-silver contacts and IC leads. Each contact connects to a single "bit" detector with high-intensity LED readout, activated when the applied voltage exceeds a fixed 2V threshold. Logic "1" (high voltage) turns LED on; Logic "0" (low voltage or open circuit) keeps LED off. A power-seeking gate network automatically locates supply leads and feeds them to the Logic Monitor's internal circuitry.

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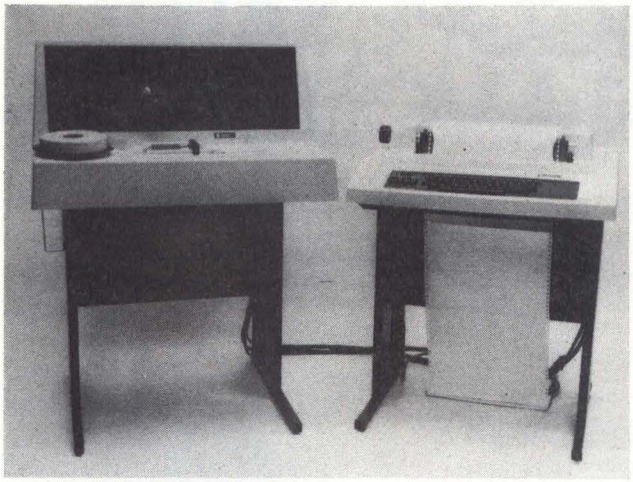
*Manufacturer's suggested price. Prices and specifications subject to change without notice.

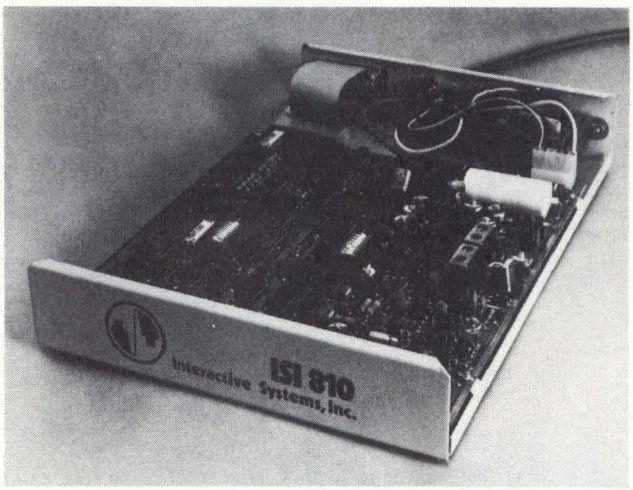
CIRCLE 92 ON INQUIRY CARD

# PRODUCTS



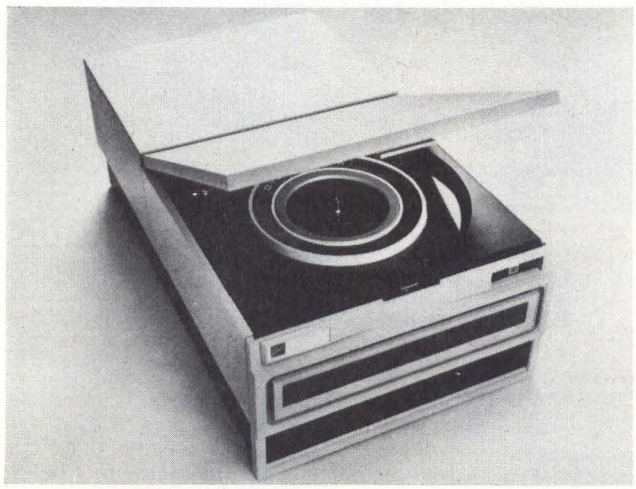
## Tape Preparation System Produced for Numerical Control Industry

Intended to replace the Flexowriter[R], the basic MPS-2000 consists of an operating system that handles both ASCII and EIA codes; 125-char/s reader; 33-char/s perforator; 30-char/s keyboard impact printer; interface to 110- or 300-bit/s data sets; and 4K bytes of internal EXEC operating system program storage. Options permit upgrading to include 4K buffer data storage modules; faster I/O and auxiliary devices; flexible diskette drive; read-after-punch station for absolute verification of correct punching; internal modems for direct communications to a central site computer; and interface for direct communications with programmable machine tools. The unit can create, edit, duplicate, verify, transmit, and store metallized, aluminized, and paper tapes. **Unitech, Inc,** 1005 E St. Elmo Rd, Austin, TX 78745.
Circle 200 on Inquiry Card




## Intelligent/Addressable Modem Interfaces Parallel Device to Coax Cable System

A single address, CMOS logic data modem developed for full-duplex, coax cable digital communication systems using TDM techniques, model 810 interfaces a single digital device, such as a CRT, line printer, or teleprinter, to a coax cable communication system at data transmission rates up to 48,000 baud in both directions, full-duplex. It accepts eight bits of CMOS, TTL, or switch-sense parallel inputs, and supplies eight output bits of open-collector or TTL logic levels. In addition, it offers an optional eight programmable latched output bits. All required rf transmitting and receiving, logic functions, and serial/parallel conversions take place on a single integrated card, keeping both modem size and cost down. **Interactive Systems, Inc,** 3980 Varsity Dr, Ann Arbor, MI 48104.
Circle 201 on Inquiry Card



## Disc Pack Drive Supports Systems Requiring High Speed, Random-Access Storage

Online data storage of 50M bytes is provided on a std IBM 3330-type short stack disc pack by the model BD-50 drive. A track-following servo system requires no external reference or reference temperature compensation. The drive has triple cooling systems, actuator mechanism sealed in a clean-air environment, and constant-voltage power supply. Quick-access filter can be replaced in approx 5 min. Drive system is fully modular; separate chassis are used for actuator and motor control mechanisms, power supply, and logic. All electronic circuitry is on plug-in cards. Internal latches which prevent operation can be overridden only by opening cover and pressing release buttons. Basic drive contains dynamic braking, std digital I/O, and ac power cable and power supply. **Ball Computer Products, Inc,** 860 E Arques Ave, Sunnyvale, CA 94086.
Circle 202 on Inquiry Card

Our modular dc supplies have always been UGLY™ because we're designers, not stylists.

But we may have outdone ourselves with our new SOLV-15.

Like all our other single and multiple-output dc supplies, our 15-watt SOLV-15 delivers its full rated output all the way up to +55°C. And its standard features include: a choice of 16 voltages from 5-24V, currents from 3-0.75A; ±0.1% regulation, ripple-and-noise; foldback current limiting; and a 1-year warranty.

But even with all this, it still looked stark.

So we took a stab at making it more attractive by getting it UL-listed and adding sense protection (free), reverse diode protection (free) and a fixed OVP (free). We wrapped it all up in a new low-profile package that uses the same mounting holes as the supplies you're probably using now.

And then priced it all a couple of bucks under the nearest competition ($23.50, 100-pieces).

We just figured that since it was so UGLY, it was really going to have to deliver.

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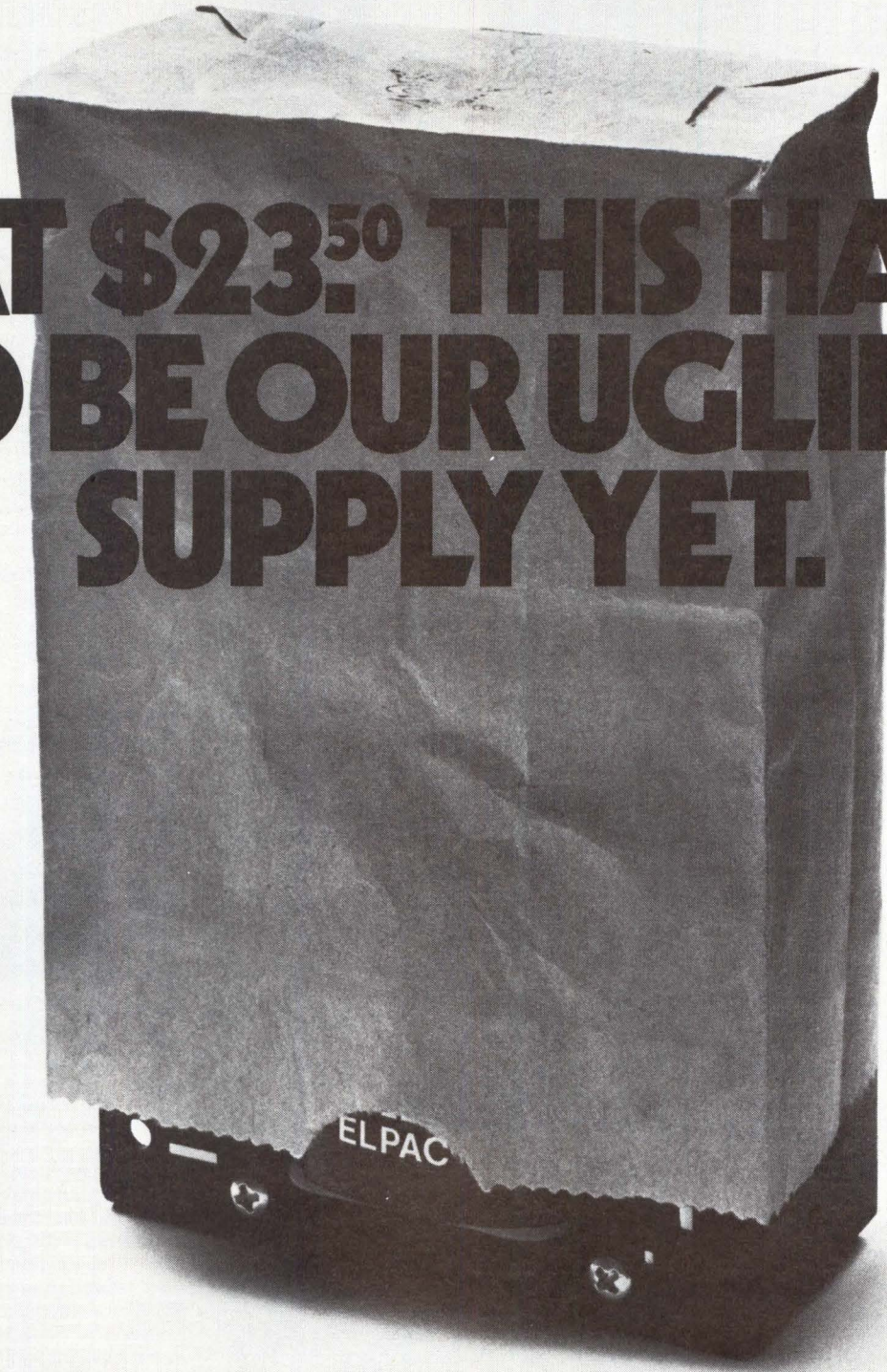
# AT $23.50 THIS HAS TO BE OUR UGLIEST SUPPLY YET.




## Elexon: the ugliest dc supplies on earth.

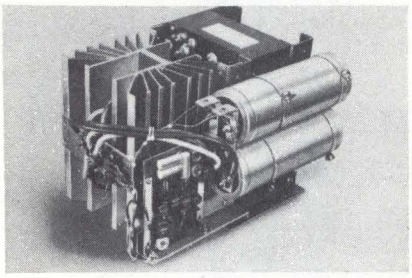
Get UGLY at Cramer, Newark, MIL-COMM, QPL and Utronics. Or call 714/979-4440.

CIRCLE 93 ON INQUIRY CARD

## PROGRAMMABLE CALCULATING SCOPE OPTIONS

Options for use with NI 2001 oscilloscope include serial asynchronous digital I/O for communications between scope and terminal; file with serial asynchronous digital I/O for locating information on mag tape cassettes; X-Y plotter for recording waveform data appearing on CRT; computer link for communication via RS-232-C interface; 8-bit parallel digital I/O for communication via binary port; and 12-bit DAC output for generation of analog voltage. **Norland Instruments,** PO Box 47, Fort Atkinson, WI 53538.
Circle 203 on Inquiry Card

## MODULAR DC POWER SUPPLIES

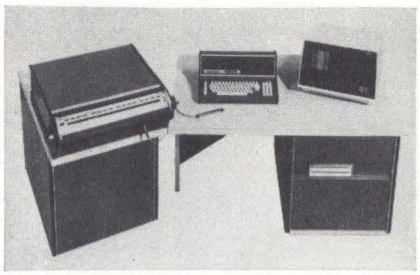


Thirty models of HR series dc supplies have been recognized as components by Underwriters Laboratories. File numbers are 478 (data processing) and 14 (office equipment). Low cost enclosed supply is interchangeable with Lambda LM series and other units. Six case sizes, and wide range of outputs, from 5 to 28 Vdc at up to 20 A, are offered. Input requirements are 105 to 125/210 to 250 V, 47 to 63 Hz. Line and load regulation is $\geq \pm 0.05\%$, and ripple is $\leq 1$ mV rms. **Tele-Dynamics, Div of Ambac,** 525 Virginia Dr, Fort Washington, PA 19034.
Circle 204 on Inquiry Card

## 12-BIT D-A CONVERTERS

Self-contained DAC-80 series includes internal reference supplies and output amplifiers. Binary or BCD versions are pin for pin replacements for Burr-Brown DAC-80 and are provided to same specs. Series incorporates functionally laser trimmed precision thin film resistor networks. Units are packaged in hermetically sealed glass 24-pin DIPs. Converter outputs, selectable by external pin connections, are 0 to 5, 0 to 10, $\pm 2.5$, $\pm 5$, and $\pm 10$ V in voltage mode. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01606.
Circle 205 on Inquiry Card

## PROGRAMMABLE DIGITAL BOARD TESTER



Configured as program development and test or test-only station, Datatester 5800 computer-driven system features high volume testing capability. Pattern generation is from fixed and programmed stimuli; response evaluation is by programmed response or transitional redundancy check. Both allow tests of low and high density logic configurations. Bidirectional 64-pin (TTL/DTL levels—0 to $\pm 5$ V) and 32-pin (multilevel—0 to $\pm 30$ V) groups are expandable. **Data Test Corp,** 2450 Whitman Rd, Concord, CA 94518.
Circle 206 on Inquiry Card

## MINICOMPUTER INTERFACE CONNECTOR MODULE

General-purpose wirewrap Nova module has four ribbon cable edge connectors with up to 50 conductors each. Board provides over 200 IC or socket positions and takes 14-, 16-, 18-, 22-, 24-, and 40-pin ICs or sockets, accommodating 0.400″ center devices. Pads are provided for discrete components at each IC position. Double-sided with plated-through holes, board takes only one slot in Nova chassis. Power and ground are prewired for each socket position. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.
Circle 207 on Inquiry Card

## AUTOMATIC ID BADGE READER

Having remotely-actuated contacts and improper-card lockout protection, SCR 1010-B accepts std plastic ID badges. Full wiping contacts, remote from read area, are protected from card-carried dirt. Proper card position and presence of hole in Hollerith pattern actuate read sensor solenoid, causing activated contacts to remain closed. Once information acquisition is complete, feedback signal breaks circuit, ejecting card. **Sealectro Corp,** 225 Hoyt St, Mamaroneck, NY 10543.
Circle 208 on Inquiry Card

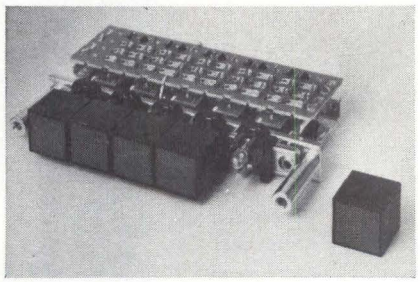
## AUTOMATIC PCB PROBER

A guided-probing unit for use on L100 series circuit board test systems, the M150 is expected to save time and increase fault-diagnosis throughout. Only three plug-ins are required to connect prober to system. Device-pin positioning information for each board is written into test plan and prober receives commands directly from system. User commands prober through terminal keyboard. PC boards up to 19.5 in.$^2$ can be tested. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.
Circle 209 on Inquiry Card

## PC BOARD CONNECTORS

For vertical board to backplane interconnection, Qiklatch is a zero entry, single sided type PC connector with solder tail termination. Tin/lead contact forms gas-tight connection with soft base metal target to prevent formation of oxides at point of contact. Available on 0.156″ centers in 8- to 24-contact position sizes, connector is designed for 0.062″ component boards and 0.062 or 0.093″ backplane. Connector body is constructed of 94V-0 flammability rated thermoplastic. **Burndy Corp,** Norwalk, CT 06852.
Circle 210 on Inquiry Card

## LIGHTED PUSHBUTTON SWITCHES



Series 1300 switches are available in low power or power-rated versions. Low power models offer up to 10-pole switching capability/button. Contacts are rated at 1 A, 28 Vdc, with brass silver plate. Power-rated type has 2-pole, double-throw switching/button, with single-sided stator; or 4-pole, double-throw switching with double-sided stator. Contacts are rated at 6 A, 125 Vac, with coin silver material. Lamp replacement is from front. Several button operations are available. **Oak Industries Inc, Switch Div,** Crystal Lake, IL 60014.
Circle 211 on Inquiry Card

# Mini-Raycorder: The first miniature data cassette recorder for micro-computers.

The Raymond Model 6409 Mini-Raycorder is the first tape recorder available to use the new Information Terminals MI-50 Mini Data Cassette. The only peripheral of its type specifically designed for use with microprocessors and in other applications where size, weight, power consumption and cost are major considerations. Small in size, its performance more than meets the needs of today's reliable data processing equipment.

Precision engineered and manufactured to the same exacting standards long recognized the world over, the Mini-Raycorder is the newest of a line of superior quality tape recorders from Raymond Engineering.

FEATURES:

- End of Tape and Load Point Sensing
- Write Inhibit
- Switch Closures — Cassette in Place and Side A/B
- TTL Compatible Interface
- Unique Reel Drive Servo for Constant Tape Speed
- ANSI Proposed Standard Compatibility

SPECIFICATIONS

Transport size: *3.0" x 3.0" x 1.8"*

Electronics: *Single PC board 3.5" x 5.75" (attaches to transport or remote mounting)*

Power: *Less than 1 watt @ 5.0V DC*
*Less than ¼ watt standby.*

Weight: *16 ozs. (including electronics).*

Capacity: *64 K bytes/side unformatted.*

Data Transfer Rate: *2400 bits per second.*

Tape speed: *3" per second.*

Rewind: *20" per second.*

Packing density: *800 bits per inch.*

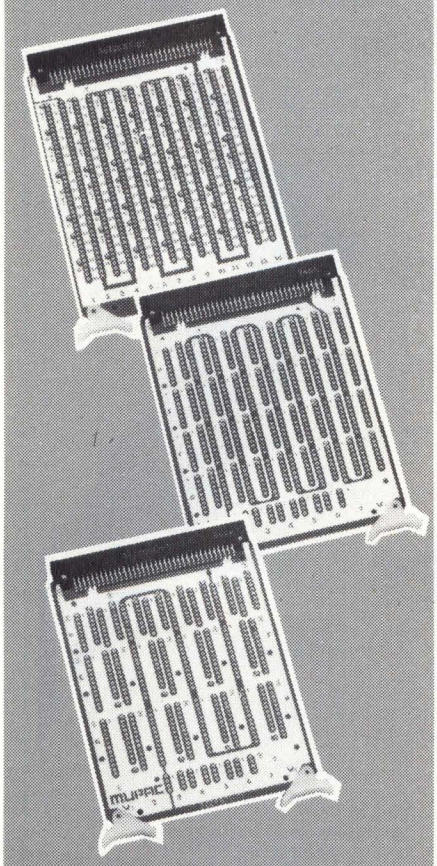
Call — or write — ask for complete details regarding Mini-Raycorder Model 6409.

**RAYMOND ENGINEERING INC.**
217 Smith Street, Middletown, Connecticut 06457
Telephone: (203) 632-1000

CIRCLE 44 ON INQUIRY CARD

# They're Here!!

**Wire Wrap* Panels for MICROPROCESSORS RAMs, ROMs, PROMs, CPUs**



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MUPAC® offers a family of multiple voltage panels, multiple voltage connector backplanes and rack assemblies for these integrated circuits.

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# PRODUCTS

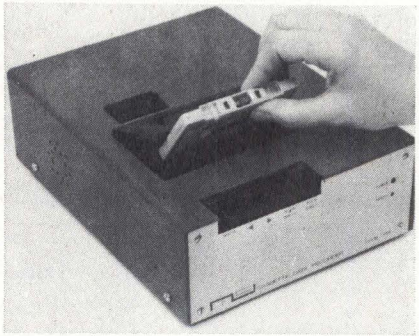
## CMOS COUNTER ICs

CMOS counters are programmable 4-bit circuits; two are decade counters and two are 4-bit binary (hexadecimal) units, both with asynchronous or synchronous clear. Std features are 3- to 18-V limits and parameters specified for 5-, 10-, and 15-V operation, and ability to drive low power Schottky TTL load. Two available temp ranges are −55 to 125°C and −40 to 85°C. In addition to the two 16-pin DIP types, the counters are available as tested dice. **Motorola Semiconductor Products Inc,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 212 on Inquiry Card

## HIGH SPEED ROM EMULATOR

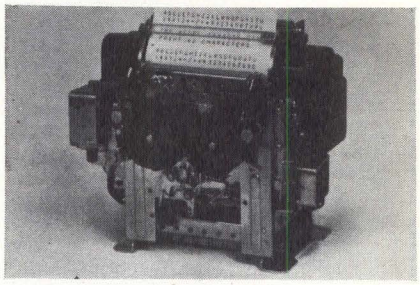
Providing direct connection capability to ROM socket up to 1024 x 8, GENRAM RE8192 can be configured to emulate ROM or p/ROM with access time of 50 ns at emulator attachment point. Units may be ganged to emulate multiple ROMs. Emulators are loaded and operated from RS-232/current loop at rates up to 19,200 baud. Individual locations or entire unit can be loaded or read for display. Entry control logic recognizes only address and data field control char. **Genesys,** 11120 Roselle St, San Diego, CA 92121.
Circle 213 on Inquiry Card

## DATA CASSETTE RECORDER



To alleviate reinstating or interchanging program problems in mini- and microcomputers, model 715 MK2 feeds into std teletypewriter interface and is similar in operation to audio recorder. Data recorder utilizes std audio or 300-ft computer grade cassette, both with breakout lugs for overwrite protection. Although max data rate is 2.4K baud, unit can load assembler or program quickly. Turns indicator and speaker help determine program starting position. **MS Instruments Ltd,** Rowden Rd, Beckenham, Kent BR3 4NA, England.
Circle 214 on Inquiry Card

## ALPHANUMERIC PRINTER UNIT



Suitable for computer printout, data logging, and electronic cash register OEM applications, AN-101F is parallel-entry 21-col line printer with 42-char font consisting of full alphabet, numerical digits, and six symbols. Print speed is 72 lines/min. Printing mechanism consists of rotating print drum and 21 print hammers. Unit is guaranteed for MTBF of 5M lines continuous operation. Dimensions are 6 x 6.4 x 4.4″; weight is 6.7 lb. **C. Itoh Electronics, Inc, Systems and Components Div,** 280 Park Ave, New York, NY 10017.
Circle 215 on Inquiry Card

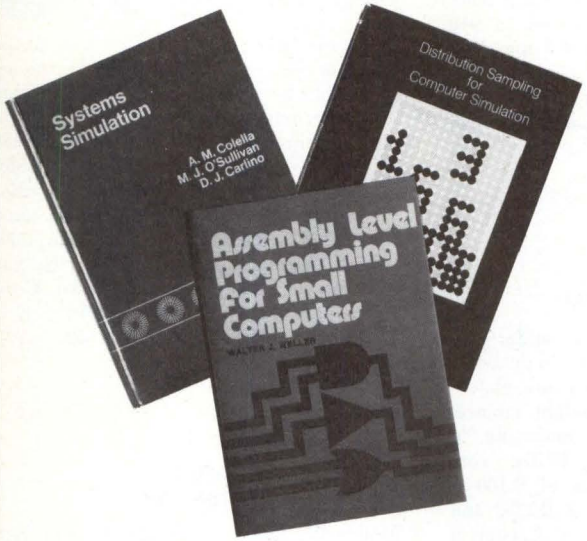
## DUAL-IN-LINE RESISTOR NETWORK

Family includes 14- and 16-pin hermetically sealed resistor networks conforming to MIL-R-83401 environmental requirements. Std in-out and pull-up circuits are offered. Resistors can handle 0.1 to 0.2 W at 70°C; networks are rated at 1.3 to 1.6 W at 70°C and derated linearly to 0 at 125°C. Networks are offered with resistors in equal or any value, tempcos of 100, 50, or 25 ppm/°C, and tolerances of 1.0, 0.5, and 0.1%. **American Components, Inc,** Eighth Ave at Harry St, Conshohocken, PA 19428.
Circle 216 on Inquiry Card

## TRIPLE OUTPUT SWITCHING POWER SUPPLY

MM series 930 ECL-PLUS regulated power supply combines three independent, single output supplies in package measuring 14 x 10 x 6.1″ and weighing <26 lb. Std outputs are −5.2 Vdc at 100 A, −2 Vdc at 75 A, and 15 Vdc at 48 A. Input voltage is 208 ±10% Vac, 1φ. Up to 80% efficient, unit features 1% pk-pk or 50-mV pk-pk ripple and noise on output, line and load regulation of 0.4%, and response time of 200 μs to 1% after 25% load change. **LH Research, Inc,** 1821 Langley Ave, Irvine, CA 92714.
Circle 217 on Inquiry Card

# 3 aspects of computer programming from




## LEXINGTON BOOKS.

### Techniques for random number generation . . .

Covering both traditional and new techniques, **Distribution Sampling for Computer Simulation** deals with the programming and generating of pseudo-random numbers.

The author, T.G. Lewis, presents several new techniques for sampling and makes extensive investigation into n-dimensional properties of pseudo-random numbers and generalized sampling from arbitrary distributions. 176 pp.

Lewis is associate professor of computer science at the University of Southwestern Louisiana and general editor of Lexington Books' new computer science series.

### simulation . . .

**Systems Simulation,** an overall view of the simulation process, provides the user with the detail and command of simulation necessary to select an optimum approach.

Principal computer representations—analog, digital, and hybrid—are discussed together with their various implementations. The authors document a set of basic steps common to nearly all simulation studies and describe the development, organization, and management of simulation programs including executive and software. 320 pp.

A. M. Colella is with the U.S. Department of Transportation; M.J. O'Sullivan and D.J. Carlino are with Northeastern University.

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### and minicomputer software.

**Assembly Level Programming for Small Computers** is a unique guide for anyone dealing with minis. It's got all the nuts-and-bolts details needed to do assembly level programming.

**Assembly Level Programming for Small Computers** lets you write your own ticket:

* Start out with the basics—the counting process, components of a computer, classification of instructions—and build from there...
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Walter J. Weller, the author, is a mini-computer software consultant based in Chicago, working in industrial, medical, and educational applications of small computers.

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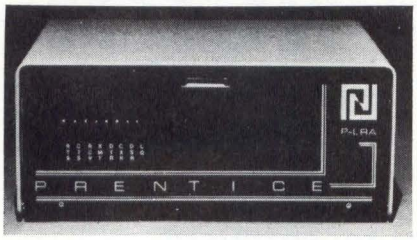
## PRODUCTS

### SYNCHRONOUS DATA LINE DRIVER/ADAPTERS




High speed limited range adapters, P-LRAs are synchronous line drivers for phase shift transmission of serial data over two pairs of twisted wires. Units can transmit data up to 10 cable miles, or further through use of repeaters. Units do not require dc continuity, although they can be installed on unloaded telephone company circuits (metallic continuity) in areas where they are tariffed. Five models operate at switch-selectable rates from 600 to 160K bits/s. **Prentice Electronics Corp,** 795 San Antonio Rd, Palo Alto, CA 94303.
Circle 218 on Inquiry Card

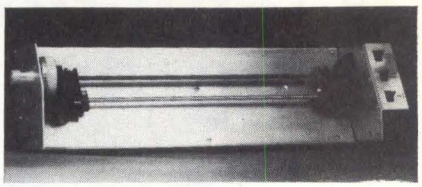
### ARRAY PROCESSOR HIGH SPEED MEMORY

AP-120B array transform processor, with high speed data memory, is peripheral arithmetic processor optimized for efficient execution of vector/matrix operations. The 167-ns data memory allows dramatic reduction of times required to perform certain types of algorithms. A 256-point complex FFT can now be performed in 940 $\mu$s, a 1024 complex FFT in 4.7 ms. Processor interfaces to several types of common minicomputers. **Floating Point Systems, Inc,** 10520 SW Cascade Blvd, Portland, OR 87223.
Circle 219 on Inquiry Card

### PRESS-FIT INTERCONNECT SYSTEM

Variboard™ eliminates need to solder connectors into PC back panels; single beam bifurcated contacts are swaged into plated-through holes providing gas-tight connection. Designed for press-fit mounting in double-sided or multilayer PCBs, connectors offer contact spacing of 0.100 x 0.200, 0.125 x 0.250, 0.125 x 0.125, and 0.156 x 0.200". Ratings are 5 A/contact with resistance of 7 m$\Omega$ max, PC card to back panel, and 0.5 m$\Omega$ max, contact to back panel. **Elco Corp, A Gulf + Western Manufacturing Co,** 2250 Park Pl, El Segundo, CA 90245.
Circle 220 on Inquiry Card

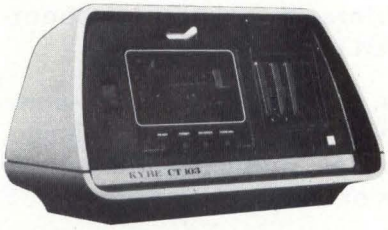
### PAPER TRANSPORT MECHANISM SYSTEM



Quiet operation, electronic vernier adjustment to 1/8 line, and adjustable tractors highlight low cost system which eliminates ratchets, levers, pawls, and need for clutches through simple design. Line feed, 1/4 line feed forward and reverse, and slew are executed at 25 lines/s. Controls allow forward slew of paper, inhibition of paper feed, and adjustment of print line registration. Various speeds of line spacing, slew, and stepping can be supplied. **Computer Transceiver Systems, Inc,** E 66 Midland Ave, Paramus, NJ 07652.
Circle 221 on Inquiry Card

### DUAL RESETTABLE BAR GRAPH DISPLAY

Model BG12203-2, dual 203-element Self-Scan® display, presents bar graphs independently from top and/or bottom of each bar, and can be operated in several modes. Information is presented with 0.5% resolution in flicker-free, easy-to-read, neon orange. Each bar has 203 segments (0.15"

# The beauty is more than skin deep.

Introducing the first low cost digital cassette subsystem that's pretty on the outside and downright beautiful on the inside where it counts. Precision performance with the flexibility to serve as a read/write or read-only memory, baud rate multiplier or terminal text/data buffer.

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The CT-103 was designed and built for long life and error-free operation by KYBE—the #1 name in magnetic media maintenance. More than a decade of tape handling experience went into making the CT-103 the best (as well as the most beautiful) digital cassette subsystem on the market today. Find out for yourself. Contact:

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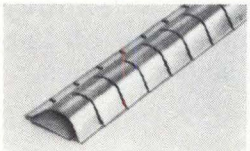
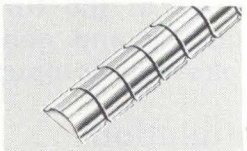
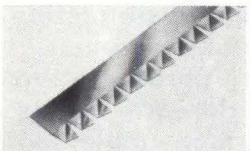
**Attaches faster, shields better than anything else!**



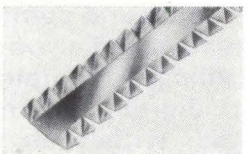
**SERIES 97-500** The original Sticky Fingers with superior shielding effectiveness.



**SERIES 97-520** A smaller size strip; highly effective in less space.



**SERIES 97-555** New Single-Twist Series for use when space is at a premium. Measures a scant 3/8" wide.



**SERIES 97-560** New 1/2" wide Double-Twist Series, ideal for panel divider bar cabinets.

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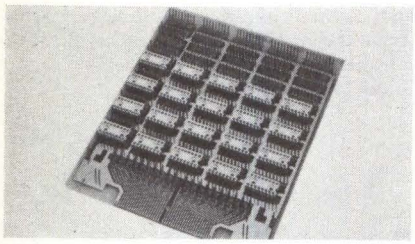
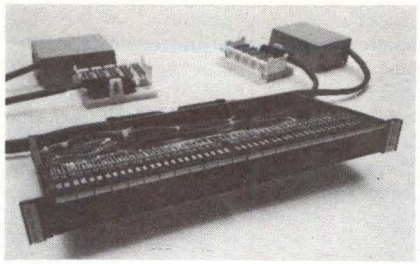
wide on 0.020″ spacing), allowing glow to blend into continuous bar at normal viewing distances. Unit measures 1.4 x 4.8 x 0.25″. **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 222 on Inquiry Card

## SINGLE-SIDED IC BOARD



Wirewrappable IC packaging panel allows boards to be mounted with close board-to-board spacing (0.500″ centers). Boards, available with std DIP low profile header assemblies or individual lead sockets, have both sockets and wrappable pins on same side. Thickness of other boards with sockets and pins on opposite sides is reduced. Further advantages are compatibility with 2-sided PC board, and direct interfacing with existing card panels or cage assemblies. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 223 on Inquiry Card

## MODEM PATCH/ACCESS SYSTEM

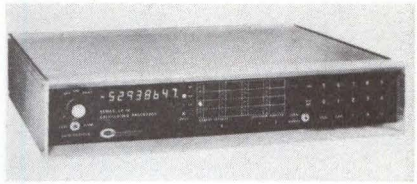


Engineered for data networks and located at junction of modem and telephone lines, system pinpoints problems within seconds by patching to backup phone line or spare modem. Convenient access for level or noise measurements is provided. Connector organization eliminates rearranging of existing cables, unsoldering, unwrapping, or reconnecting wires. Same system may be used for 4- or 2-wire circuits. Package includes jackfield, two modems, cables, and terminations. **ADC Telecommunications,** 4900 W 78th St, Minneapolis, MN 55435.
Circle 224 on Inquiry Card

## HIGH SPEED 4K RAMs

An n-channel silicon gate device, the MB 8215 is reported to be the first dynamic MOS 4K RAM to offer bipolar-like typ access time of only 70 ns (100 ns max) and power dissipation as low as 500 mW/chip. Speeds are guaranteed over 0 to 70°C op temp range. Differential outputs with OR-tie capability are provided; bipolar sense amps for high speed access time are available. **Fujitsu California, Inc, Laboratory Div,** 1280 E Arques Ave, Sunnyvale, CA 94086.
Circle 225 on Inquiry Card

## DIGITAL DATA PROCESSOR



Using equations stored in plug-in EPROM, the CP70A accepts and operates on data from up to three sources. Equations have data from external sources or constants stored in RAM. Std or optional series of equations are selected by use of front panel program address thumbwheel switches. Values of constants can be changed by front panel keyboard. Eight-digit readout contains polarity and decimal indications, displays results, and indicates value of constants being programmed. **California Instruments Div of Aiken Industries, Inc,** 5150 Convoy St, San Diego, CA 92111.
Circle 226 on Inquiry Card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CIRCLE 97 ON INQUIRY CARD

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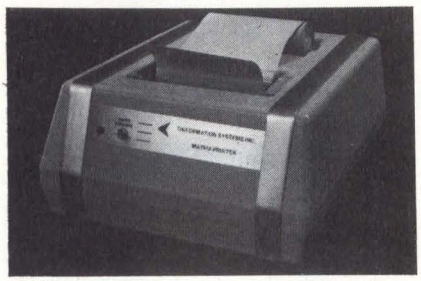
## PRODUCTS

### HIGH SPEED ELECTROSTATIC PRINTER



Designed as replacement for teleprinters, the TRI-80 provides real-time printouts, on command, from ASCII video terminals at 8 to 16 times the speed of teletypewriters. The microprocessor-directed printhead can print up to 80 char/s in 40-col widths, or up to 160 char/s in 80-col widths. Nonimpact printhead has 5 x 7 dot matrix and 64 alphanumeric char, and produces high contrast printout. Printer is fed by 240-ft rolls of electrosensitive paper. **Triformation Systems Inc,** PO Box 2433, Stuart, FL 33494.
Circle 227 on Inquiry Card

### 8- AND 16-CHANNEL DATA ACQUISITION MODULES

Featuring 12-bit resolution and 75-kHz min throughput rate, two modular systems offer 16-channel single ended or 8-channel differential operation. Total accuracy is ±0.025%. Hybrid 12-bit A-D converter has 8-μs max conversion time and performs data conversion. System uses monolithic sample-hold and CMOS multiplexer. Channel address register is for sequential or random selection of channels up to full capacity. Input voltages are externally selected. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 228 on Inquiry Card

### ALPHANUMERIC DOT MATRIX THERMAL PRINTHEAD

The DM1150 10-col printhead contains one row of 10 groups of five heater dots for printing up to 10 columns of 5 x 5 or 5 x 7 matrix char, and uses close dot spacing for dense, legible printout. Design allows stacking printheads edge-to-edge to expand column capability. Head is interconnected for multiplexed operation with on-board chip isolation diodes. Paper is stepped in continuous contact across printing surface which leads to simplified mechanism. **Gulton Industries, Inc, Electronic Components Div,** Metuchen, NJ 08840.
Circle 229 on Inquiry Card

### HIGH PERFORMANCE DATA ACQUISITION MODULE

Containing 16-channel multiplexer, buffer and high speed sample/hold amplifiers, 12-bit A-D converter, and all control and programming logic, the DT5701 is designed for use with microcomputers. Outputs are 3-state TTL buffered for direct connection to buses. Unit features 12-bit resolution, ½ LSB linearity from 0 to 70°C, and system accuracy of 0.03% of full-scale range. Built-in elements include zero and gain adjustments, input multiplexer protection, and break-before-make switching. **Data Translation Inc,** 109 Concord St, Framingham, MA 01701.
Circle 230 on Inquiry Card

### FLOPPY DISC CONTROLLER

High speed microprocessor-based design provides functions implemented in ROM. FDC-1 is flexible disc drive controller for up to four drives. Features include drive write protect, automatic CRC generation and check, full IBM 3740 compatible soft sector formatting, automatic track seek verify, and head retraction after eight idle disc rotations. Disc is TTL implemented and compatible. Eight-bit parallel input and output buses for control information provide interface. **Digital Systems,** 754 Carmel Ave, Livermore, CA 94550.
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Gears are sintered iron to precision tolerances, providing low backlash for computer peripheral, instrumentation and other demanding applications. Gearbox design strength limit is 1,000 oz.-in. Many possible variations in armature windings permit tailoring of outputs to a wide range of performance requirements.

GM 9213 Gearmotors ensure value and reliability at a moderate price. 123

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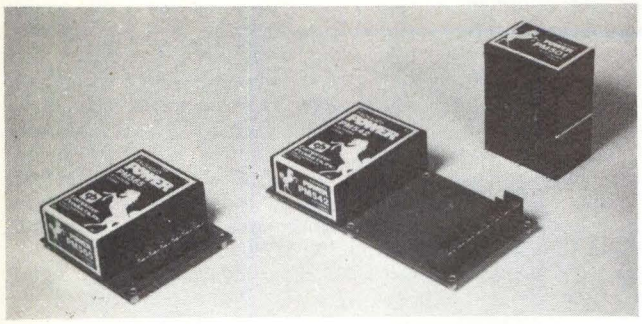
## MODULAR POWER SUPPLY MATING SOCKETS



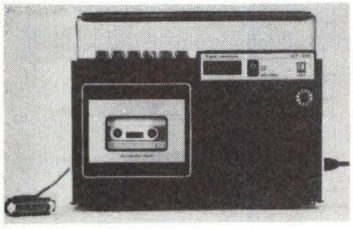
Plug-in type sockets with barrier terminal strip connections, model MS-148-0 accepts one power supply and -149-0 accepts two. The sockets are made of glass-epoxy type PC material and have standoff spacers for mounting. Applications include product prototyping and elsewhere that plug-in capability is desirable. Single- and dual-output supplies in 23 models are compatible with these sockets. **Computer Products,** 1400 NW 70th St, PO Box 23849, Fort Lauderdale, FL 33307.
Circle 232 on Inquiry Card

## MEDIUM/HIGH CURRENT DARLINGTON ARRAYS

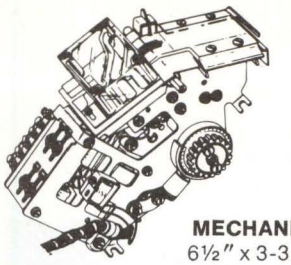
SG2001/2/3 and SG3851/2/3 families, medium and high current transistor arrays, respectively, consist of seven silicon npn Darlington pairs on common monolithic substrates. Each device features low saturation voltage, high speed switching, and closely matched parameters. 2001/2/3 offers peak inrush currents to 600 mA; 3851/2/3, to 750 mA. 2001 and 3851 interface with DTL and TTL signals, 2002 and 3852 are p-MOS-compatible, and 2003 and 3853 use either CMOS or TTL drive signals. All are available in hermetically sealed 16-pin ceramic DIPs. Units feature common emitter configuration with open collector outputs and integral suppression diodes for inductive loads. Darlington pair collector current rating is 600 mA for 3851/2/3, and 500 mA for 2001/2/3. Outputs can be paralleled for higher current load capability. Max collector output voltage is 50 V. **Silicon General Inc,** 7382 Bolsa Ave, Westminster, CA 92683.
Circle 233 on Inquiry Card

## 3M-BIT PORTABLE STORAGE UNIT

Designed primarily for field testing and program loading small computers, the ACT-1200 contains 4-ft cable and connector that store within the 12.1 x 7.7 x 3.3″ unit for travel. Unit plugs into std serial asynchronous port of any computer or terminal, and can record and playback at std rates up to 1200 baud. It is aimed at OEM dedicated minicomputers that have to be loaded occasionally with new programs for upgrading. Need for on-site interfacing or hardware for program loading is eliminated. Most minicomputers can use existing paper tape oriented software with the unit. With editing-type programs, the unit can record source programs following a punch command and re-enter following a read command. Similarly, the output of an assembler or compiler can be recorded for future loading via std object loader programs. **Digital Laboratories,** 377 Putnam Ave, Cambridge, MA 02139.
Circle 234 on Inquiry Card



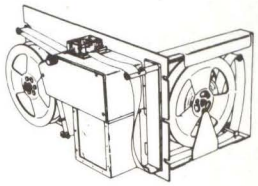

Punched Tape



**MECHANISM ONLY**
6½″ x 3-3/16″ x 4½″

# ROYTRON™

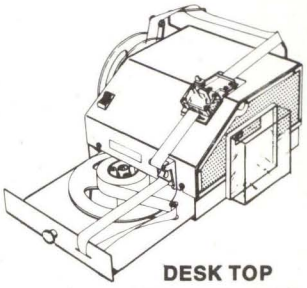
ROYTRON Readers, Punches and Combination Reader/Punches are offered in over 20 standard configurations.



**RACK MOUNTED**
12″ x 19″ x 10½″

**Paper Tape/ Edge Punch Card**
Punches (50-60 cps)

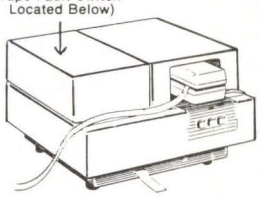
**Paper Tape/ Edge Punch Card**
Readers (50 cps)



**DESK TOP**
14½″ x 15″ x 9½″

**Combination Paper Tape Reader/Punch**
Reader (50/150/250 cps)
Punch (60 cps)

PUNCH COVER (Punch Mechanism and Tape Fault Switch Located Below)



**PHOTOELECTRIC READER/PUNCH**
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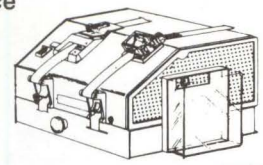

**COMBINATION READER/PUNCH**
16″ x 16″ x 10″

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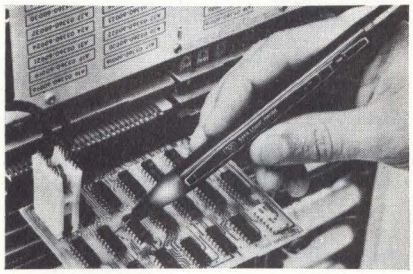
## PRODUCTS

### MULTI-FAMILY LOGIC PROBE



Simplifying logic circuit testing, model 545A indicates digital states and pulses in high and low level logic. Single lamp indicator displays levels or detects open circuit conditions. CMOS/TTL operation is selected with slide switch. Automatically set CMOS logic threshold levels are variable. One probe can sense positive logic up to 18 Vdc. Features include built-in pulse memory, pulse stretching, and pulse trains to 80 MHz in TTL, 40 MHz in CMOS. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.
Circle 235 on Inquiry Card

### DATA DISTORTION ANALYZER

DAL-100 Analyzer/BERT permits LED display of average, end, or peak distortion readings of up to 50% in 1% increments on char or bits. Frequency synthesizer allows rate selection from 10 to 9990 bits/s. Inputs can be high or low level. Alarm lamp displays odd or even parity errors on 8-level codes. Optional programmable EIA interface adapter provides connection to equipment for testing TDM and FDM channels, modems, or data terminals. **International Creative Data Industries, Inc,** PO Box 451, Danbury, CT 06810.
Circle 236 on Inquiry Card

### BIDIRECTIONAL OPTICALLY COUPLED ISOLATOR

OPI 2500 features input of two LEDs connected in inverse parallel to enable operation from bidirectional inputs. Guaranteed min current transfer ratio in either direction of the isolator is 12.5% at an input of 16 mA. Typ current transfer ratio is 30%. Providing 1500-Vdc input-to-output isolation, it is available in 6-pin DIP. Isolator is designed for applications requiring interface isolation between ac line and dc logic circuitry. **Optron, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.
Circle 237 on Inquiry Card

### CRT DATA TERMINAL

The PE9000 conversational CRT terminal features baud rates from 50 to 9600 selectable by operator, 103 and 202 modem protocol, destructive or nondestructive backspace, "break" key, and printer port. Keyboard is detachable with 5-ft cord, and has separate 11-key numeric pad and N-key rollover. Terminal is available with either 16- or 24-line x 80-char display. Display has 12″ diag CRT, scroll or page display mode, and 60-Hz refresh rate. **Perry Electronics, Inc,** PO Box 10217, Raleigh, NC 27605.
Circle 238 on Inquiry Card

### SYNCHRO/RESOLVER TO DIGITAL CONVERTER MODULE

Available with 14- or 15-bit output, model SD552 has accuracies up to 0.03 deg at tracking rate of 3600 deg/s with transformer isolation. Occupying half of previous converter volume, low profile module requires only one card slot, 0.5″ center to center, in computer or CRT card cage assemblies. CMOS circuitry is used, reducing 5-Vdc current consumption. Unit is supplied with Hi-Rel components to MIL-883 level B and JANTX. Dimensions are 0.42 x 2.6 x 3.1″. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.
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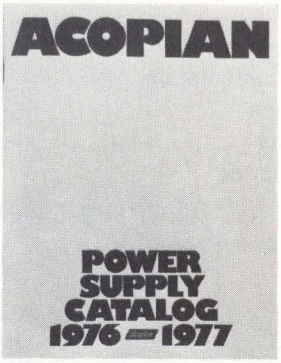


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Total U.S. shipments of process control equipment in 1973 had a sales volume of $1.54 million — which will increase to $2.1 billion in 1977 and $2.55 billion in 1980 (in constant dollars). During the next ten years, measuring instruments will continue to be the largest equipment category in sales, while digital controllers will be the principal growth segment.

Frost & Sullivan has completed a 200-page analysis and forecast of the process control market through 1984, by product and end user industry. Applications, technology developments, the competition and catalysts and limitations to growth are explored. Product categories covered include: measuring instruments, analog controllers, control valves & actuators and digital controllers.

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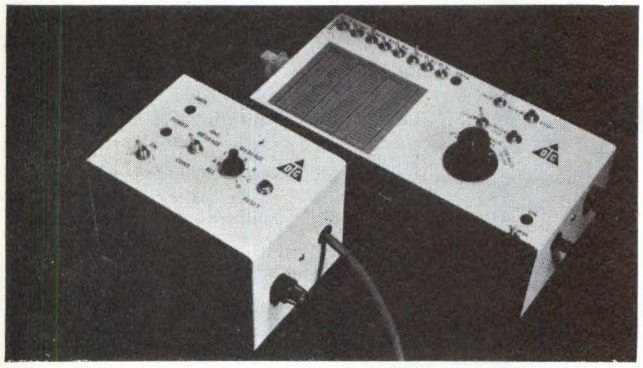
## HI-REL HYBRID D-A CONVERTER

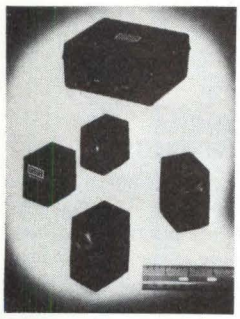
A true 12-bit binary DAC, model 4058 operates over the −55 to 125°C full-MIL temp range, has max nonlinearity of ±½ LSB, and requires only ±15-V power. Current settling time to within ±0.01% of final value for a full scale step is <200 ns; voltage settling is <2.5 μs. Max full scale tempco is ±10 ppm/°C. Zero stability is ±1 ppm/°C for current outputs and ±5 ppm/°C for voltage ranges. Max versatility results from externally programmable current and voltage outputs. Programmable full scale outputs include ±2 and 4 mA, and ±10, −10, ±5, −5, and ±2.5 V. The device is housed in a 24-pin hermetically sealed metal DIP. Model 4058-83 has 100% screening to MIL-STD-883, Method 5004, Class B, including stabilization bake, fine and gross leak, constant acceleration, burn-in, and temp cycling. **Teledyne Philbrick,** Allied Dr at Rt 128, Dedham, MA 02026.
Circle 240 on Inquiry Card

## ASCII PROGRAMMER

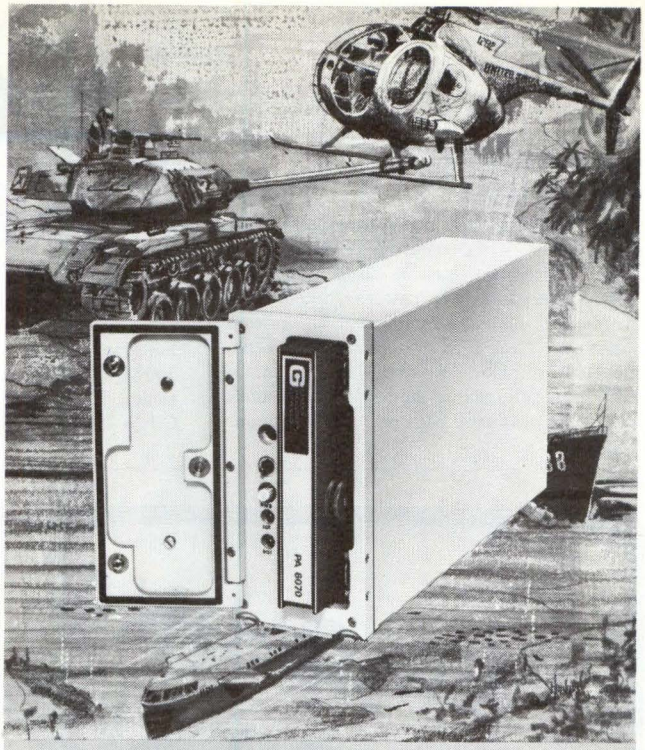


Model 954 expands repertoire of ASCII char for the company's 900 series ASCII char generators and generator/receivers. Field replaceable p/ROM permits preprogramming one message of up to 128 char, two messages of 64 char each, four messages of 32 char, or any combination. To change a message, the p/ROM can be removed, and a new one inserted. Programmer can be shared by several ASCII char generators. Speed control, insertion of start and stop bits, sequencing, and interfacing are performed by generator being used. Message can run once or continuously. Programmer can be used for simulation of sign-on procedures, storage of subroutines, repetitive test messages, and generation of tape header information for cassette tapes. Power supply is self-contained, and logic circuits are enclosed. **Terminal Data Corp of Maryland,** 11878 Coakley Circle, Rockville, MD 20852.
Circle 241 on Inquiry Card

## LED PHOTOELECTRIC SCANNERS



Four models of Visolux sender-receiver/amplifier scanning heads cover the primary photoelectric applications. Retro-reflecting model MCS-625 has 15-ft operating range, 0.002-s on/off response time, and 15K-cycle/min. max rate; reflective model MCS-626 has 12″ operating range (off an 8½ x 11″ sheet of white paper) that can be adjusted down to 1½″, 0.005-s on/off response time, and 6K-cycle/min. max rate; MCS-626-1 has adjustable 1- to 4-ft reflective range. A 2-part MCS-627 model has 30-ft typ and 50-ft max operating range; its response time is 0.002 s on/off, and max cycle rate is 15K/min. An optional power supply (MCS-149) for use with any of the scanners can operate up to four units simultaneously. All scanners have 10-ft cable; both scanners and power supply are packaged in NEMA enclosures. **Warner Electric Brake & Clutch Co,** 449 Gardner St, Beloit, WI 53511.
Circle 242 on Inquiry Card

**COMPACT MAGNETIC TAPE CARTRIDGE RECORDER/REPRODUCER**

...for Cost Effective, Reliable Operation in Severe Environments.

**The Model ECR-10 features:**

- Qualification to Army/Navy/Air Force environmental requirements.
- Complete recorder/reproducer with electronics and power supply in 3/8 ATR short case or standard rack mount (8.75"x4.0"x13.75").
- Record and playback speeds up to 60 ips; search and wind speeds up to 120 ips.
- Parallel 7, 8 or 9-track computer-compatible digital or analog recording.
- Up to 600 feet of 1/2-inch tape in a unique, environmentally capable, self-tensioning cartridge.
- Easy cartridge insertion and removal with positive positioning and locking in the transport.
- No reel motors required – tape directly driven by servo-controlled capstan motor.
- Large reel recorder operational capabilities, including bi-directional Read After Write and Erase functions.
- Very fast Start and Stop for bilateral inter-changeability with computer generated tapes.

For complete ECR-10 details, call Les Turner at (213) 537-4750

An Equal Opportunity Employer M/F

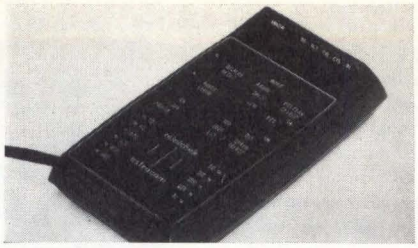
**GENISCO TECHNOLOGY CORPORATION**
**Systems Division**

18435 Susana Road, Compton, CA 90221 (213) 537-4750

SEE THE ECR-10 AND OUR OTHER NEW RUGGEDIZED PERIPHERALS AT THE NCC–BOOTH NO. 1605

## PRODUCTS

### DATA TRANSMISSION LINK TESTER



Pocketsize Minichek tester attaches to any synchronous or asynchronous modem to help isolate transmission link problems. Tester generates four patterns, checks for errors, and displays number of errors and status of RS-232 interface signals. Technical specs include random (511 pattern), all space, all mark, and alternate mark and space transmit patterns; asynchronous speeds of 300 and 1200 bits/s; and two digit error count LED displays. Two 9-V batteries supply power. **Astrocom Corp,** 15012 Minnetonka Industrial Rd, Minnetonka, MN 55343.
Circle 243 on Inquiry Card


SWITCHING POWER SUPPLY

LOW COST

DESIGNED TO POWER

★ QUME/DIABLO PRINTERS
★ MICROPROCESSOR SYSTEMS
★ COMPUTER TERMINALS
★ MINI COMPUTERS
★ BURROUGHS DISPLAYS

60 to 300 WATTS 4 OUTPUTS

TYPICALLY 1/4 SIZE, 1/9 WEIGHT AND 1/5 HEAT OF A LINEAR SUPPLY

If you can't live with the heat, weight and size of linear supplies and can't afford the high prices of switching supplies, look at our line of low cost, high efficiency open frame switching power supplies.

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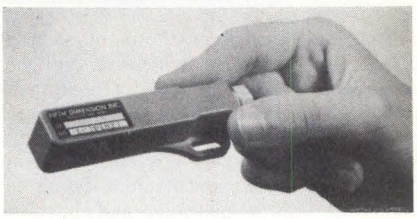
### SINGLE, DUAL, AND TRIPLE OUTPUT POWER SUPPLIES

Supplies are available in three basic configurations: single output 5 V (500 to 1200 mA), ±12 or ±15 V (150 mA) dual output, and triple output 5 V and ±12 or ±15 V. Mounted on a PC card, each type utilizes monolithic IC regulators that provide 2% load and 1% line regulation. Full short circuit protection, low ripple (10 mA), and low internal impedance are other features. **Elcom Industries, Inc,** 79R Terrace Hall Ave, Burlington, MA 01803.
Circle 244 on Inquiry Card

### FLOPPY DISC

Improved performance and durability are features of model FD-3200S's newly developed binder system that allows very fine dispersion of magnetic powder for highly accurate recording. Smooth surface of disc permits improved durability. Disc can be used for 10M passes/track without error. Recording density is 3200 bits/in. Memory capability of 8" disc is 243K bytes on seven tracks. Disc is packed in square jacket. **Maxell Corp of America,** 130 W Commercial Ave, Moonachie, NJ 07074.
Circle 245 on Inquiry Card

### BOUNCE FREE LIMIT SWITCH

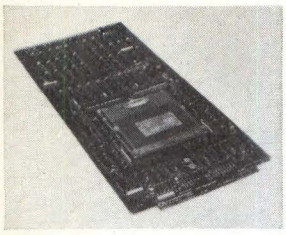


LC2P-1823, an epoxy encapsulated switch package, has tested reliability of over 2G cycles between failures, and is rated at over 500M operations. Unit is built around LC2 mercury film switch which is welded steel capsule carrying film of mercury. Patented system circulates mercury, renewing stationary contacts. Contacts provide stable resistance of 150 mΩ at microampere levels; at power loads, to 2.0 A. Shock and vibration levels exceed 30 G. **Fifth Dimension Inc,** 707 Alexander Rd, Princeton, NJ 08540.
Circle 246 on Inquiry Card

### MAG TAPE CLEANER/ RETENSIONER/REWINDER

Utilizing dual high efficiency cleaning system which eliminates >90% of permanent R/W errors, TC-225 has electronically controlled retensioning, rewinding system, which prolongs life of tape. Features include 225-in./s throughput speed; IBM-compatible self-seating hubs, front-mounted controls, and loading system to simplify operation; "Enduron" sapphire jewel cleaning blade; and four auto-advancing tissue cartridges. **Kybe Corp,** 132 Calvary St, Waltham, MA 02154.
Circle 247 on Inquiry Card

## MINICOMPUTER 1K AND 4K CORE MEMORY MODULES



Nonvolatile core memories in 1K and 4K 16-bit word packages are offered on half cards, the same size as used for semiconductor memories. Because the 1K and add-on model 11761-04 4K memories are compatible with all other Naked Mini core and semiconductor memories, the user can choose from among RAM, ROM, p/ROM, and EPROM for the configuration that best suits his requirement. 4K cards can be configured into systems as large as 32K words. Three versions of the Alpha LSI-3/05 series are available with the 1K memory, five with the 4K; the memories are also available with the LSI-2 series. A 1K core card with a Naked Milli LSI-3/05 CPU card provides a model 10320-01 minicomputer; the same CPU with 4K card is a model 10320-04. **Computer Automation,** 18651 Von Karman, Irvine, CA 92664.

Circle 248 on Inquiry Card

## LARGE LED DISPLAY MODULES

A 0.8″ high LED display digit, reported to be the largest single digital display available in the industry, is readable at 30-ft distances, permitting use in applications requiring "across-the-room" monitoring of readouts. Common cathode types are the FND800 which has right-hand decimal, and the -850, with left-hand decimal; common anode types are the -807, right-hand decimal, and the -847, left-hand decimal. Supply voltage is 1.7 V; avg current is 5 mA/segment; avg intensity is 0.15 mcd/segment. A single LED is used per segment to reduce supply voltage requirements. Digits are assembled in 1.03 x 0.77″ package. **Fairchild Camera and Instrument Corp, Optoelectronics Div,** 464 Ellis St, Mountain View, CA 94042.

Circle 249 on Inquiry Card

## AUTORANGING DMM PROBE

A 3½-digit, 14-range device that combines thermometer and digital multimeter in a hand-held probe body, the model 12T features autoranging, autopolarity, and 0.1% Vdc accuracy. When the probe tip is pressed to a surface, temperature can be read with 0.1°C resolution. In addition, the probe measures ac/dc voltages from 1 mV to 750 V and resistance from 1 Ω to 19.99 MΩ. Readout is a monolithic 7-segment LED display. Overrange in all modes is indicated by blinking of two horizontal segments in front of the most significant digit. Up to 4-h continuous operation can be obtained from std NiCd rechargeable size AA batteries. When the probe is not in use, power can be turned off. Batteries can be recharged overnight from a 117-Vac source. **Logical Technical Services Corp,** 71 W 23rd St, New York, NY 10010.

Circle 250 on Inquiry Card


# THIS MAKES 40,000 CASSETTE RECORDERS. WHEW!

When it comes to cassette recorders, who you buy them from is as important as what you buy.

And when you buy the Sycor Model 135, you're dealing with a company that already has 40,000 recorders in service worldwide.

The popularity of our cassette recorder isn't really surprising.

The Sycor 135 is the ANSI compatible cassette drive with record overwrite capacity that lets you edit a whole data block without disturbing so much as a character on adjacent records.

The recorder that reads/writes at a fast 12.5 ips with quick starts and stops for high throughput. With a dual-gap head for Read-After-Write verification.

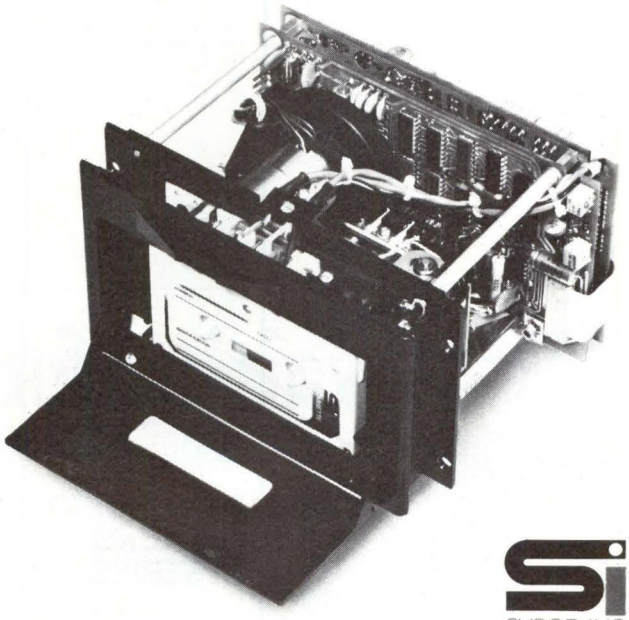
The recorder that accesses data at a clip of 60 ips.

For more information on our Model 135, or for help on any design or application problem, give us a call.

A company that's made 40,000 cassette recorders ought to be pretty good at finding solutions.

**SYCOR**

Contact Dick Conner, OEM Department, Sycor, Inc.,
100 Phoenix Drive, Ann Arbor, Michigan 48104, Telephone: (313) 995-1381

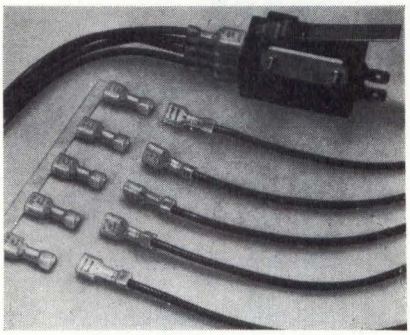


SYCOR INC

*Sales offices in major metropolitan areas throughout the world.*

**Circle 105 for data only.**
**Circle 124 for salesman.**

## PRE-INSULATED QUICK-DISCONNECT TERMINAL

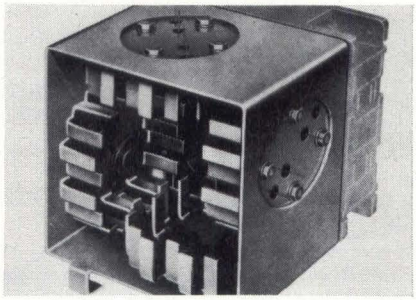


Rated at 600 V and 105°C, fully-insulated FASTON terminal has no protruding metal parts and can be machine applied at rates up to 7600 terminals/hr. One-piece nylon insulator is color-coded to indicate wire range and translucent to permit visual inspection. Tin-plated brass terminals can be used with 0.187 or 0.250" wide quick-disconnect tabs. Lead-in features are designed into terminal and insulator, which has funnel entry wire barrel. **AMP Inc,** Harrisburg, PA 17105.

Circle 251 on Inquiry Card

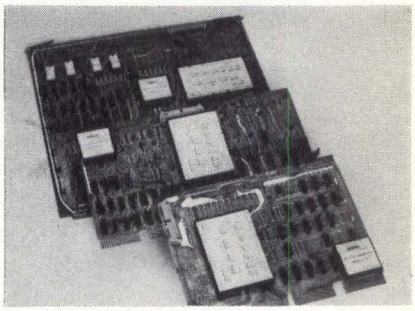
## LIGHTWEIGHT SEMICONDUCTOR COOLING PACKAGE

Series FAHP4 units use four std HP3 staggered finger heat sinks to dissipate 450 W in 25°C ambient with semiconductor case temp rise of <95°C. Semiconductor hole pattern in dissipator allows unit to be assembled from std heat sinks mounted to shrouds. Hole patterns can accommodate single or dual mounting, allowing up to eight TO-3 or TO-66 semiconductors; shroud opening holds dual mounting with sockets for TO-66s and TO-3s. **International Electronic Research Corp,** 135 W Magnolia Blvd, Burbank, CA 91502.



Circle 252 on Inquiry Card

## DATA ACQUISITION AND CONTROL SYSTEMS



Economy Series, single-card, A-D and D-A converters and sample and hold systems are software and mechanically compatible and fit into CPU or expansion boxes of minicomputers: 535-DGC is Nova and Eclipse compatible, 635-11 is for PDP-11, and 635-8E is for PDP-8/E, /F, /M, and /A series. Basic configuration consists of 16 single-ended, 16 pseudodifferential, or 8 differential channels of multiplexer input, 12-bit successive approximation ADC, sample and hold, bus interface, dc/dc converter, and cable. **Adac Corp,** 118 Cummings Park, Woburn, MA 01801.

Circle 253 on Inquiry Card

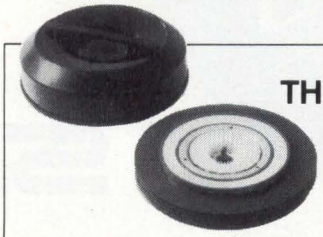

# We have your Disc Media answers.

**Q.** _____? **A.** You can be sure of that, sir! Nashua has a planned program specifically designed to service the needs of both O.E.M.'s and systems houses. We are geared to service your present *and* future needs.

**Q.** _____? **A.** Let me name just a few: 5440 (top loader) with Multi-Sector disc size .050 & .075. Current State-of-the-Art Winchester Media (aligned & lubricated). 3336 type 100, 200, 300, & 400 MB. CDC type Disc Packs 100 & 200 MB... I could go on and on.

**Q.** _____? **A.** Don't worry about that. Nashua makes memory devices for every known drive on the market: Calcomp (Trident), CDC (Storage Modules and Disc Packs), Diablo, Pertec, Ampex, ISS, Wangco, etc.

# We're waiting for your questions.



THE NEW TRIDENT DISC PACKS. 4460 SERIES

(T25, T50, T80 type)
another memory answer from Nashua

We can come up with the answers to all your memory requirements. Just phone:

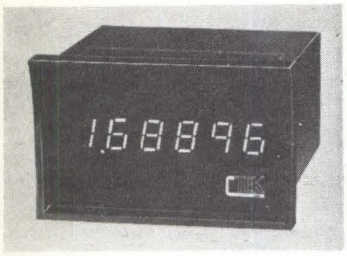
**(415) 655-9361** Chet Mielcarz

**(603) 880-2769** Dave McGuckin

NASHUA CORPORATION
Nashua, New Hampshire 03060.

## PANEL MOUNTING COUNTER/DISPLAY

From two to five full decades of decimal display or counting functions, plus optional overrange "1" and polarity symbol, are provided on the series AN540. Operation is from BCD data 8-4-2-1 parallel inputs. Serially, the counter will respond to count frequencies up to 10 MHz. Features include 0.43" high planar LED digits, user-programmable decimal point position, BCD outputs, optional decade counter and storage register outputs at read connector, DTL/TTL-compatible inputs, and buffer amplifiers for driving storage and reset lines. Each output can drive 10 TTL loads. Case size is 2.0 x 3.8 x 2.75" (50.8 x 88.9 x 70 mm). All circuitry may be removed from the front for servicing. The unit can operate from existing 5-V supplies or optional built-in 115-Vac supply. Op temp range is −10 to 70°C. **C-Tek, Inc,** 4 Railroad Ave, Wakefield, MA 01880.




Circle 254 on Inquiry Card

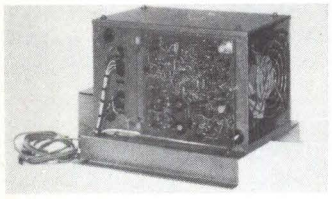
## STANDARD MINICOMPUTER SYSTEM

Configuration incorporating PDP-11T34 processor consists of PDP-11/34 CPU with 32K words (64K bytes) of parity memory, memory management, bootstrap, and clock; dual-drive disc-pack subsystem; and dot-matrix terminal printer and control. System can run RT-11, RSX-11M, MUMPS, and RSTS/E. CPU is upward-compatible with PDP-11/04 minicomputer. Both use same memories, peripherals, chassis, cabinets, and options, and have same UNIBUS® architectures; only processors differ in functional scope. 64K words of 16-bit parity memory plus options can be put in 5¼" high chassis. Std features include memory management unit, extended instruction set, and "virtual console." Console control can be effected from ASCII terminal. Self-testing console permits machine-level diagnoses to be performed remotely, via communication line hookups. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 255 on Inquiry Card

## CRT DISPLAY DEFLECTION AMPLIFIER

Designed for alphanumeric/vector type display systems, the DA3000 is ultra-linear deflection system which provides 3-MHz bandwidth while conserving power. Beam deflection is achieved through proportional splitting of current between positive and negative half-axes of deflection coil, so that difference in current is always proportional to sine of deflection angle. Stability and very low noise are assured. Sampling of deflection currents at output of coil windings, providing negative feedback to input, guarantees linearity. All deflection is accomplished in one major-axis system. Functional simplicity and accuracy are achieved with high frequency signals processed by same feedback amplifiers and driven through same deflection windings as larger signals. Amplifier is applicable to most random-write or fixed-raster display systems. **Discom Display Components Inc,** 550 Newtown Rd, Box 488, Littleton, MA 01460.



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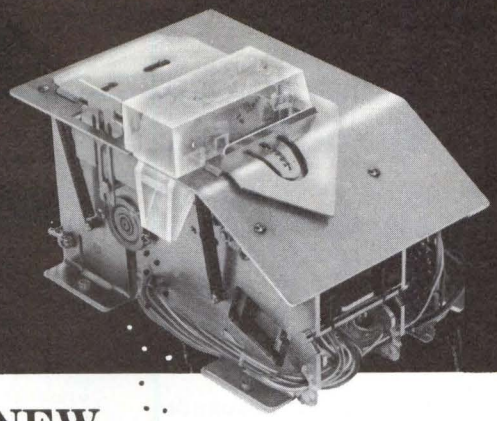


NEW FOR OEM

**6110**

**PAPER TAPE PUNCH**

**Lowest cost, highest reliability, easiest to maintain in operation**

Epson's precision manufactured, miniature 6110 Paper Tape Punch mechanism offers high reliability *and* low unit cost to OEM.

Compare these value features:

- Long life steel punchblock warranted to process 500 9" reels MTBF.
- Simple design that allows compact size only 4" high, 4" wide and 6" long.
- Brushless motor for high reliability and low power consumption.
- Operation at 50 characters per second.
- Adjustable tape guide for 5, 6 and 8 channels.
- Easy to design control circuit.
- Price in OEM quantities less than $200.00.

Complete factory parts, repair and customer training located at our Torrance main office.

**Write or call for complete information**

At NCC (1128), also see our new paper tape reader, card reader, line printers, and micro drum memory.

**EPSON**

EPSON AMERICA, INC.

2990 W. Lomita Blvd., Torrance, CA 90505
(213) 530-6533

CIRCLE 107 ON INQUIRY CARD

## SURVEY OF MICROPROCESSOR/ MICROCOMPUTER BUYERS

The publishers of COMPUTER DESIGN and the leading industrial market research company INTERNATIONAL DATA CORPORATION announce a significant new market research report entitled:

**Survey of Microprocessor/ Microcomputer Buyers**

**7000 COMPUTER DESIGN readers were surveyed to determine:**

- the type of equipment using μPs/μCs they are currently designing.
- the μP/μC models selected and the criteria for the selection
- the memories selected and the criteria for the selection.
- peripherals used with the equipment.
- various aspects of software and test.
- opinions on current μPs/μCs and peripherals.
- recommendations for their improvement.
- future plans for using μPs/μCs

and much more.

The 150 page report contains more than 50 tabulations of data from the survey, many of them correlating use factors and selection criteria with type of equipment. Each table is accompanied by an explanation of its meaning and an interpretation of its significance.

For a more detailed description of the report, circle 120 on the Reader Inquiry Card,

**or write**

Survey of Microprocessor/
Microcomputer Buyers

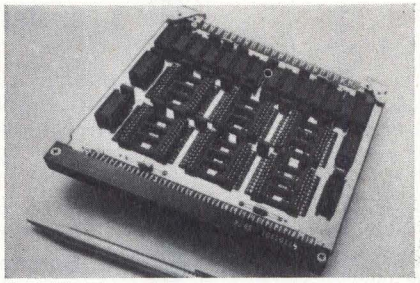
Computer Design
Market Research Group
143 Swanton St.
Winchester, MA 01890

# PRODUCTS

### TUBE-AXIAL FAN

The TA1000, 10″ dia x 3.5″ deep, consists of impeller, housing, and motor; is interchangeable in dimensions, mounting hole configuration, and plug attachment with other 10″ fan models; and outperforms them with less input power and lower winding temp. Recommended range of operation at 60 Hz is from 310 cfm at 0.165″ $H_2O$, static pressure to 490 cfm at 0.05″ $H_2O$, with current and power constant throughout. Two models are available for 115- or 230-V power at 50/60 Hz. **Torin Corp,** Torrington, CT 06790.
Circle 257 on Inquiry Card

### INLINE SOCKET CARDS

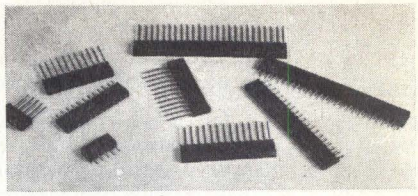


Up to six 42-pin quad-in-line and 18 16-pin dual-in-line packages can be installed in these 3D5019 wirewrap socket cards. Included for reduction of power noise are 27 ceramic and four tantalum capacitors. Power is connected on four of 16-pin sockets; remaining sockets can be custom connected with power clips furnished with card. Cards feature 96-pin pin and socket edge connector and fit company's std 3D files. The 5.82 x 6.25″ card is available for 2- and 3-level wirewrap. **EECO,** 1441 E Chestnut Ave, Santa Ana, CA 92701.
Circle 258 on Inquiry Card

### LOW PROFILE KEYBOARD SWITCH

Model DI-104, companion piece to Double Cross Point, has <½″ profile and is designed for high quality terminal keyboard applications. Switch features double set of crosspoint gold alloy contact, rugged construction, and low contact bounce. Switching elements are enclosed to prevent foreign particle contamination. Terminals are sealed to allow soldering. Switch life is specified for 20M operations; >4G test operations have been accumulated without failure. **Data Interfaces Inc,** 12 Cambridge St, Burlington, MA 01803.
Circle 259 on Inquiry Card

### SINGLE INLINE IC SOCKETS



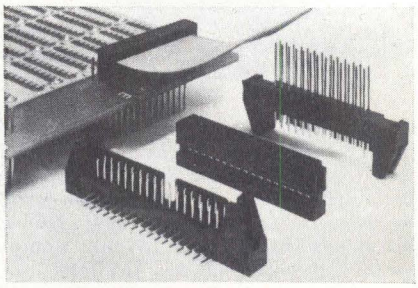
Line of SIP sockets in 5-, 11-, 12-, 14-, 20-, and 25-pin lengths are both side- and end-stackable. When combined, they can be used for unusual width or length requirements. Use of open area on PC board between sockets is also obtained. Available with solder tail or three lengths of wirewrap pins, sockets can be supplied in right angle configuration for use at end of board. Contacts are 0.010″ leaf spring phosphor bronze, except solder tail which is 0.008″. **Circuit Assembly Corp,** 3169 Red Hill Ave, Costa Mesa, CA 92626.
Circle 260 on Inquiry Card

### FAST INFRARED LIGHT EMITTING DIODE

Suited for high power color video or data transmission via fiber or air, IR emitters (GaAlAs/GaAs) have high figure of merit, $F \geq 10^6$ W/s in pulsed operation. Features include typ response time of 50 ns, radiation frequency at or near fiber optics absorption min, and CW-operation over 10 mW. Several mounts are available (eg, TO-5, power stud) with different lens types for wide angle and beamed power. **International Audio Visual, Inc,** 15818 Arminta St, Van Nuys, CA 91406.
Circle 261 on Inquiry Card

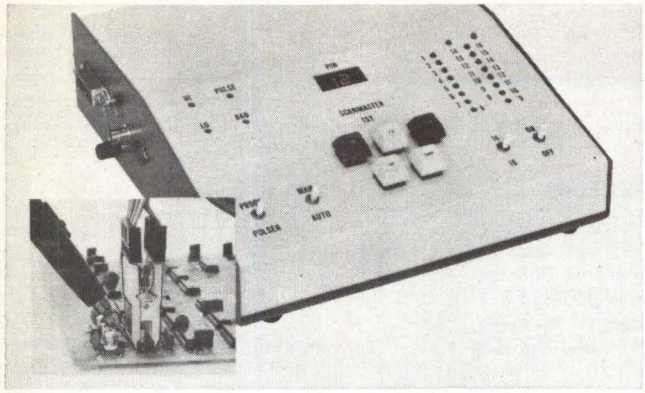
### FLAT RIBBON CONNECTORS

Designed for fast, low cost installation on logic panels, PC boards, and backplanes, Multi-Term line consists of series 6200 male (with protected pins), 6600 male (with unprotected pins), 6300 female, 6400 DIP, and 6700 card edge connectors—all on 0.100″ contact centers. Line includes 1-piece header connectors in 10 to 60 contacts in straight-through or right-angle configurations, and those featuring preassembled construction with optional strain reli f. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.



Circle 262 on Inquiry Card

## AUTOMATIC LOGIC TESTER



Scanmaster—combining logic probe, logic clip, pulser, and circuitry for detecting pin-levels—automatically checks every pin in 14- or 16-pin logic modules for high, low, and bad levels of TTL, DTL, HTL, RTL, CMOS, or other positive logic families. After scanning the module, the tester stores and displays its static-state truth table in a panel LED array. If bad level—ie, a logic state that is either not high enough or not low enough (or both) to be a proper logic signal—is detected, the unit stops its scan at the bad pin and identifies the number of the display. A universal pulser-probe can be used to check for more details or to inject a single pulse into the circuit under test. For dynamic circuit conditions, a second LED panel shows pin voltage conditions. **Information Scan Technology,** 3650 Charles St, Santa Clara, CA 95050.

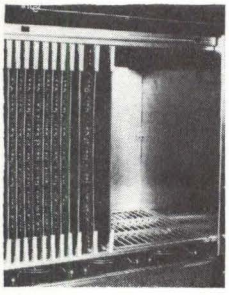
Circle 263 on Inquiry Card

## PROGRAMMABLE LOGIC CONTROLLER

Features of the model 1001 include simplified direct entry of relay ladder diagrams into the controller without converting to computer language, programming and editing of a CRT, extra programming card for adding functions not normally included with PLCs, and optional test panel for go/no-go check of program and processor. 8-bit MPU, up to 64 I/O circuits, programmable digital timers, shift registers, pre-adjustable counters, built-in fault monitoring system, individually isolated I/Os with status lights, and patented isolation circuit are included in the design. Std units has 1K words of light erasable reprogrammable memory. Timers and counters can be entered and monitored online. Options include data entry panel for entering timer/counter presets and program loader with 1K R/W memory for testing programs. **Struthers-Dunn, Inc, Systems Div,** PO Box J, Bettendorf, IA 52722.

Circle 264 on Inquiry Card

## CCD MEMORY SYSTEM



The in-65 Megachassis provides high density, solid-state memory system with up to 2M bytes stored in a unit measuring 19 x 17.5 x 14". Additional chassis may be used for system expansion. Basic storage element is 16K-bit CCD. Chassis houses system boards which include MU-65 memory units to store 128K x 8 or 9 bits; CU-65 control unit to operate up to 1M bytes or words (up to eight memory boards); and BU-65 buffer unit, required only in systems with word lengths of $\geq$ 2 bytes. Number of bytes/word ranges up to eight. The 1M 18-bit word unit is popular size for replacement of small disc and drum memories. Chassis can also be organized 512K x 36 or 256K x 64. System is used as block-oriented RAM and can transfer data at rates up to one word every 550 ns, or up to 14.5M bytes/s. **Intel Memory Systems,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.

Circle 265 on Inquiry Card

**I/O Data Transmission Cable**

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# LITERATURE

### OEM Microcomputer

Details on MM1 microcomputer system featuring Poly-Buss™, address spaces, and design options are provided in descriptive brochure which includes software information. **Control Logic, Inc,** Natick, Mass.
Circle 300 on Inquiry Card

### Synchro/Resolver Converters

Capsule descriptions, specs, and applications of angle position indicators and synchro-resolver data converters are provided in short-form catalog. **C & A Products, Inc,** Woodside, NY.
Circle 301 on Inquiry Card

### Optional Programmer

Features of 954 programmer available for 900 series char generators and for use in systems engineering, field service, and minicomputer software checkout are covered in leaflet which includes applications information. **Terminal Data Corp of Maryland,** Rockville, Md.
Circle 302 on Inquiry Card

### Wirewrap Hardware

Short-form catalog describes wiring services, wirewrap cards, files, panels, CAD/CAM software, and modular hardware for microprocessor applications; also offers full-line catalogs. **EECO,** Santa Ana, Calif.
Circle 303 on Inquiry Card

### DC-to-DC Power Supplies

Details of supplies necessary to activate readouts for users of gas discharge displays are available in product data sheets, application notes, and spec sheets contained in data file folder. **Endicott Coil Co,** Binghamton, NY.
Circle 304 on Inquiry Card

### n-MOS 1K RAM

Complete with schematic diagrams, graphs, and tables, data bulletin and application note furnish further systems considerations of MW7001ID static RAM. **RCA Solid State Div,** Somerville, NJ.
Circle 305 on Inquiry Card

### Lighted Pushbutton Switches

Comprehensive catalog points out aesthetic, performance, and versatility advantages of EAO series lighted pushbutton switches. **Unimax Switch Corp,** Wallingford, Conn.
Circle 306 on Inquiry Card

### Miniature DIP Slide Switches

Catalog sheet details electrical, environmental, and operational specs, plus mechanical data, pin and contact interconnections, features, and applications of submini, dual-in-line, multislide switches. **Minelco, div of General Time,** Thomaston, Conn.
Circle 307 on Inquiry Card

### Digital Cassette Tape Transport

Operation and interface manual provides information on general performance; mechanical, electrical, and technical specs; schematics; and engineering definitions for Model 250B tape transport. **MFE Corp,** Salem, NH.
Circle 308 on Inquiry Card

### Switches

Outlined in 32-page selection guide are detailed specs, electrical ratings, circuitry, and technical diagrams for complete line of switches, including new LED display pushbutton and programmable DIPs. **Licon, Div Illinois Tool Works Inc,** Chicago, Ill.
Circle 309 on Inquiry Card

### Aperture Time for A-D Conversion

Graphs in application note allow circuit designers and systems engineers to find quickly the amount of error in aperture time required for A-D conversion, simplifying selection of converter or sample-hold circuit. **Datel Systems, Inc,** Canton, Mass.
Circle 310 on Inquiry Card

### Illuminated Pushbutton Switches

Catalog highlights features of 554 series switches presenting electrical and mechanical ratings and dimensional diagrams for panel or bezel mounting units. **Dialight, a North American Philips Co,** Brooklyn, NY.
Circle 311 on Inquiry Card

### Precision Electronic and Electromechanical Products

Full range of products, including communications terminal and test equipment, displays, printers, potentiometers, modules, and keyboards, is covered in brochure which provides general descriptions, data, and photos. **Bowmar Instrument Corp,** Phoenix, Ariz.
Circle 312 on Inquiry Card

### Graphics Display Terminals

Colorful, illustrated brochure describing line of interactive computer terminals presents technical features enabling hardware to do work of software, and advantages resulting in reduction of required data. **Hughes Aircraft Co, Industrial Products Div,** Carlsbad, Calif.
Circle 313 on Inquiry Card

### I/O Typewriter

Model 735, a replacement for the IBM Selectric® in I/O applications, is described in technical bulletin covering features, applications, specs, schematics, and baseplate characteristics. **Tycom Systems Corp,** Fairfield, NJ.
Circle 314 on Inquiry Card

### p/ROM and FPLA Programming Systems

*PROMBiTS,* a bimonthly newsletter designed to furnish info on programmable logic encompassing p/ROMs and FPLAs, features paper tape preparation, calibration techniques, generic card set, and new products in this issue. **Data I/O Corp,** Issaquah, Wash.
Circle 315 on Inquiry Card

### Universal Data Converter

Introducing the DC-6 parallel-to-serial converter, a flexible, programmable communications interface with OEM adaptions available, pamphlet outlines features, operation, specs, and applications. **Science Accessories Corp,** Southport, Conn.
Circle 316 on Inquiry Card

### DC Mini Motors

Showing many combinations of motors from ⅞ to 2¼" dia, with std planetary gearboxes, easy-to-read wall chart indicates torque, speed, voltage, reduction ratios, and armature windings. **TRW Globe Motors, an Electronic Components Div of TRW, Inc,** Dayton, Ohio.
Circle 317 on Inquiry Card

### Thermoset Plastic Knobs

Catalog supplies photos, descriptions, and necessary information for engineering specs of full line of std instrument and mechanical knobs, as well as information on custom knobs. **Kurz-Kasch, Inc,** Wilmington, Ohio.
Circle 318 on Inquiry Card

### PC Board Bus Bars

Literature kit includes product folder, design sheets, schematic drawings, and series of technical articles emphasizing cost savings and technical advantages of Mini/Bus® line of PCB bus bars. **Rogers Corp,** Chandler, Ariz.
Circle 319 on Inquiry Card

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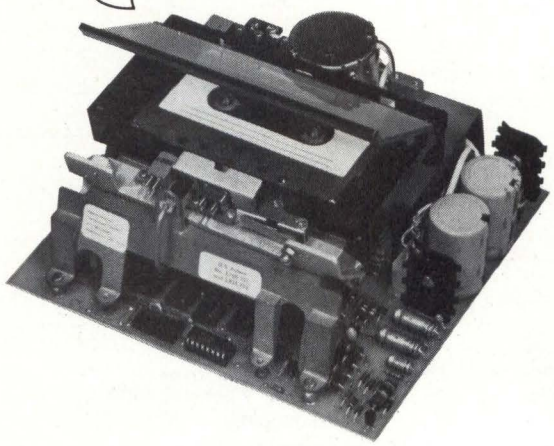

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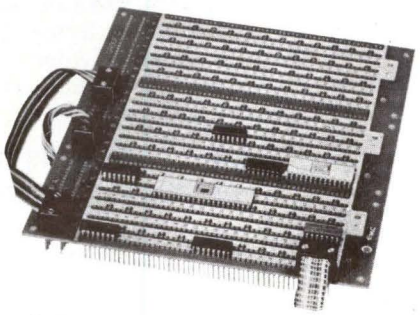

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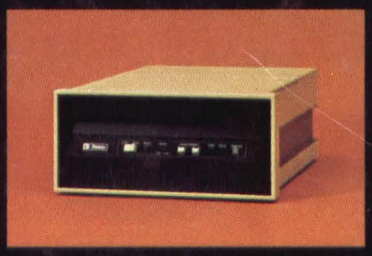

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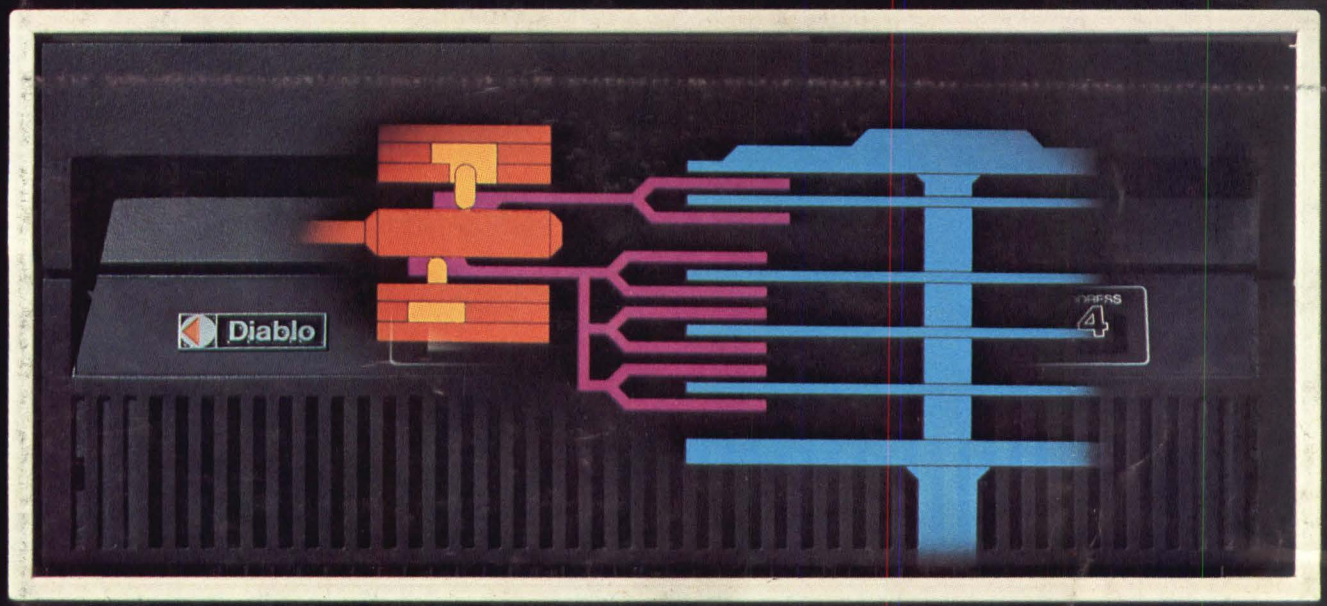


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