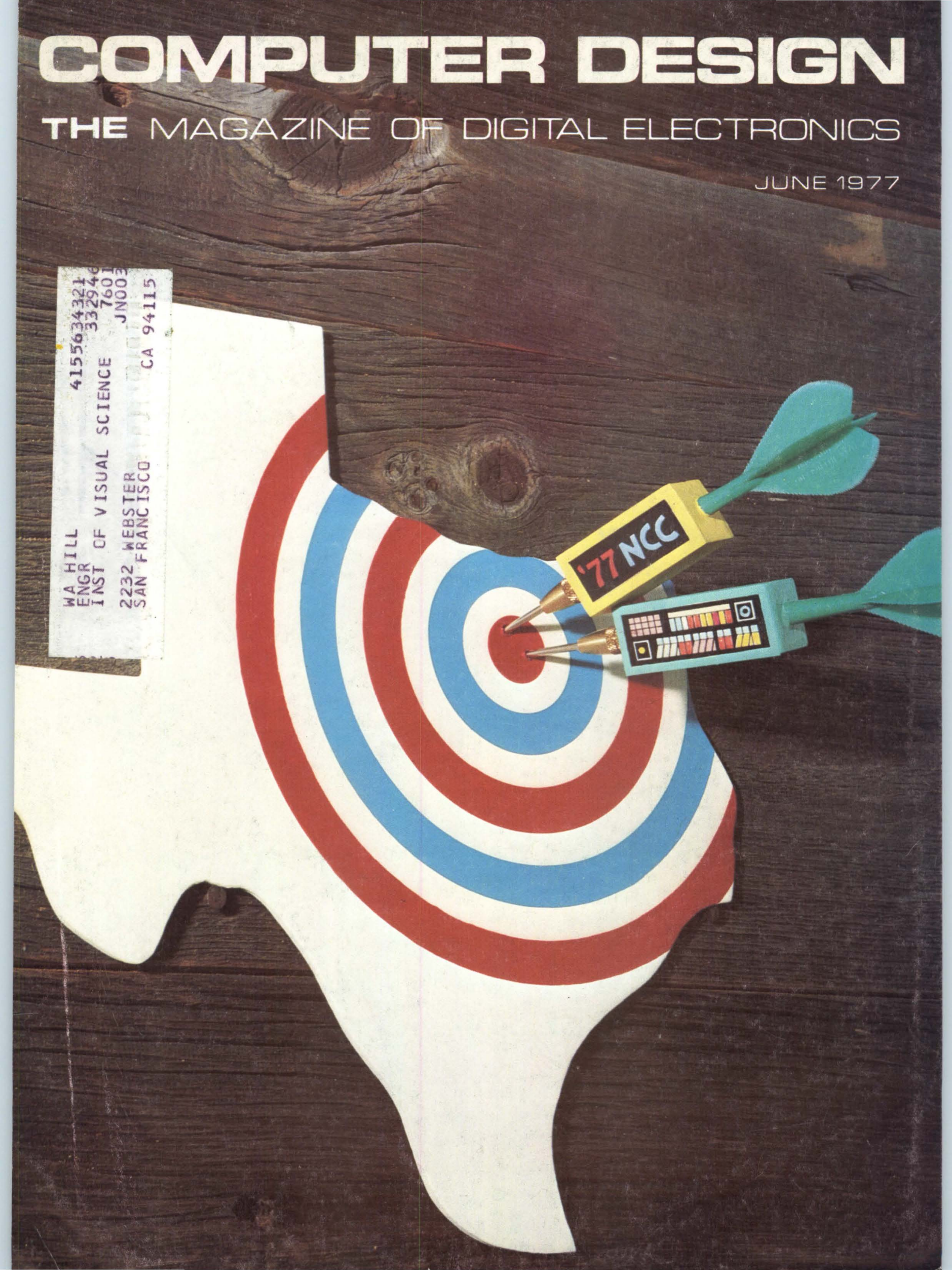
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JUNE 1977



New! DATUM Tape or Disc Systems for IBM Series 1!

Series 1 users can now add mag tape memory capability to their Series 1 (Models 3 or 5) installation! The new DATUM seven- or nine-track system permits recording densities of 200 bpi NRZ through 1600 bpi, phase-encoded. Speeds: from 12.5 ips through 125 ips. As many as four transports can be used.

A 5440 removable-media disc system that is software-compatible with the IBM 4962 Disk Storage Unit is also available.

Both systems incorporate the new DATUM "Universal User's Adapter," a device that allows connection of external devices to the Input-Output bus of Models 3 or 5 of the IBM Series 1 computers. The Adapter operates in the "cycle -steal" mode while exchanging 16-bit words with the computer. With this Adapter, Series 1 users can tailor their system to their own exact requirements, even to the extent of interconnecting several computers.

Diagnostic and operational software is included with each system. Color-coordinated cabinets can be ordered. Service and installation is offered throughout the U.S. Deliveries are 90 to 120 days ARO.

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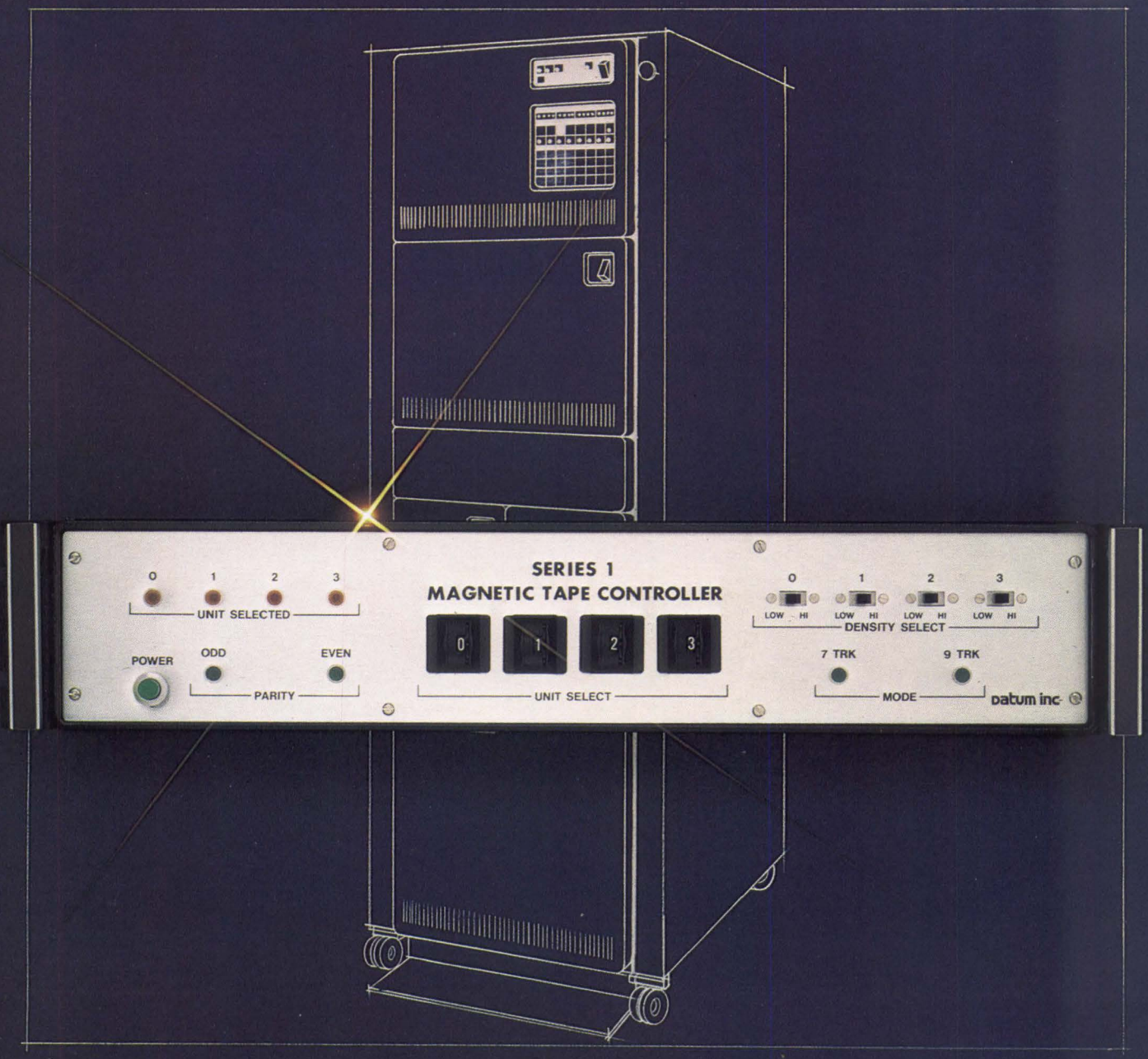
CIRCLE 1 ON INQUIRY CARD

datum inc



Series 9000...

Still the hottest series around.

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- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick-release hubs.
- All models are available with either 7 or 9 track, 800 NRZI, 1600 PE or 800/1600 NRZI/PE.
- 7 and 9 track NRZI and PE format/ control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available.

Series 9000's performance is as impressive as its features, with data transfer rates to 72KHz, and tape speeds from 10 to 45 ips.

Series 9000 is the hottest digital tape transport series around, and we plan to keep it that way, with constant improvements, rigid quality control and greater service capabilities. That should give you a warm feeling if you have a requirement for digital tape transports.

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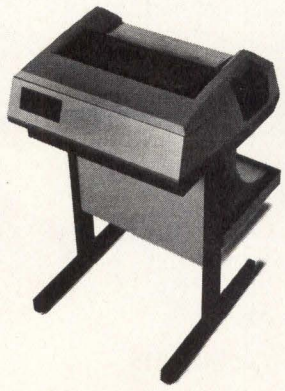
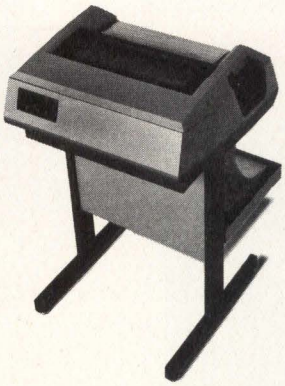
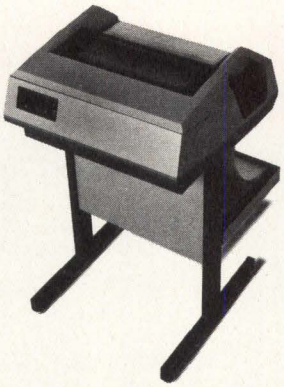


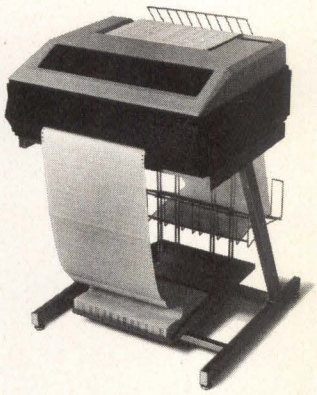
40 to 100 lpm



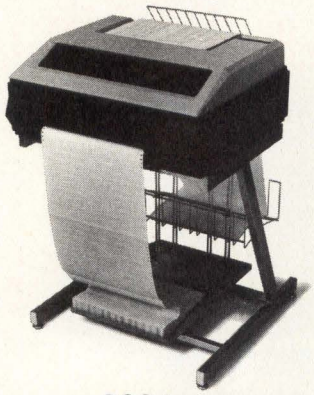
55 to 150 lpm



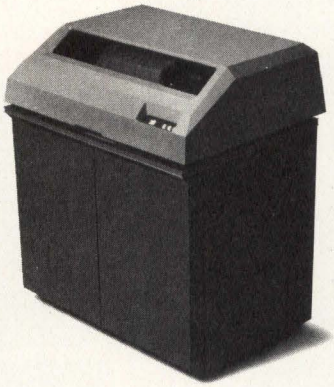
70 to 200 lpm



125 lpm



200 lpm



300 lpm

375 lpm

500 lpm

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THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

JUNE 1977 • VOLUME 16 • NUMBER 6

FEATURES

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BPA **CIRCULATION OVER 55,000**

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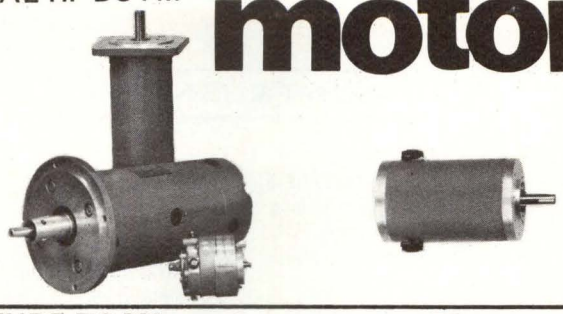
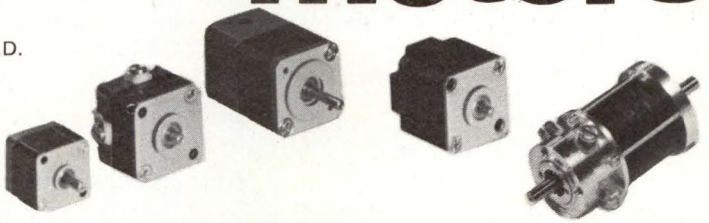
APPLICATIONS	FEATURES
TAPE TRANSPORT DRIVES	Torques from 10 to 120 lb-ft
DISK MEMORY DRIVES	2 inch to 5.5 inch O.D.
PRINTER CARRIAGE DRIVES	Advanced magnetic materials
MACHINE TOOL DRIVES	Cartridge brushes
CONVEYOR DRIVES	



MINIATURE DC PM INSTRUMENT motors

APPLICATIONS	FEATURES
DAISY WHEEL DRIVES	Torques from 2 to 50 oz-in.
PRINT HEAD DRIVES	.75 inch cube to 1.25 inch O.D.
INSTRUMENT RECORDERS	Cartridge brushes
LABORATORY INSTRUMENTS	Alnico or rare earth magnets

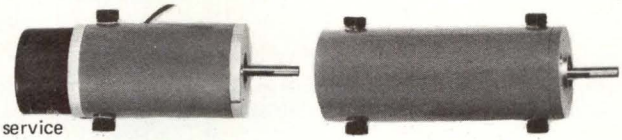


PM STEPPER motors

APPLICATIONS	FEATURES
PRINTER RIBBON DRIVES	Step angles 7.5°, 15°, 30°, 45°, 90°
PRINTER PLATTEN DRIVES	1.1 inch to 2.8 inch O.D.
CARD SORTERS	Ceramic or rare earth magnets
OFFICE COPIERS	

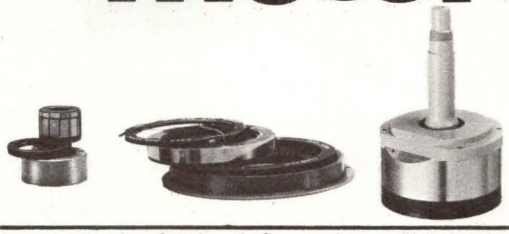
INTEGRAL ENCODER AND MOTOR-TACHOMETER ASSEMBLIES motors

APPLICATIONS	FEATURES
PRINTER CARRIAGE DRIVES	Optical encoder resolution to 1000 cycles
COPYING MACHINES	Solid state gallium arsenide light source
SPEED CONTROLS	Integral assemblies — no assembly or alignment necessary
MACHINE TOOL CONTROLS	Single source for motor/encoders eliminates costly assembly & simplifies service



DC PM HOLLOW SHAFT TORQUE motors

APPLICATIONS	FEATURES
INERTIAL NAVIGATION PLATFORMS	Torques from 6 to 500 oz-in.
AIRCRAFT INSTRUMENTS	1.1 inch to 5.2 inch O.D.
AIRCRAFT CONTROLS	Precision tolerances Gold commutators High reliability



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CALENDAR

CONFERENCES

JUNE 20-24—1977 Internat'l IEEE/AP-S, USNC/URSI, URSI Internat'l Electromagnetic Sym, Stanford, Calif. INFORMATION: IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 644-7500

JUNE 20-24—3rd Microprocessor Conf, Ames, Iowa. INFORMATION: Roger Camp, 332 Coover Hall, Iowa State University, Ames, IA 50011. Tel: (515) 294-2663

JUNE 21-23—4th Sym on Machine Processing of Remotely Sensed Data, Purdue U, West Lafayette, Ind. INFORMATION: Dr John C. Lindenlaub, Laboratory for Applications of Remote Sensing, Purdue University, 1220 Potter Dr, West Lafayette, IN 47906. Tel: (317) 749-2052

JUNE 21-23—31st Annual Convention of Armed Forces Communications and Electronics Assoc (AFCEA), Washington, DC. INFORMATION: Judith H. Shreve, Editor, AFCEA, Skyline Ctr, 5205 Leesburg Pike, Falls Church, VA 22041. Tel: (703) 820-5028

JUNE 22-24—Joint Automatic Control Conf, San Francisco, Calif. INFORMATION: Prof J. Meditch, Dept of Electrical Engineering, U of Washington, Seattle, WA 98195. Tel: (206) 543-2170

JUNE 27-29—35th Annual Device Research Conf, Cornell U, Ithaca, NY. INFORMATION: Conf Chm, George E. Smith, Bell Telephone Labs, Murray Hill, NJ 07974

JUNE 28-30—Internat'l Sym on Fault-Tolerant Computing, Los Angeles, Calif. INFORMATION: Prof A. D. Friedman, Dept of Electrical Engineering and Computer Science, U of Southern California, Los Angeles, CA 90007

JULY 18-19—Special Interest Group in Computer Graphics 4th Annual Conf (SIGGRAPH 77), San Jose, Calif. INFORMATION: Steve Levine, Lawrence Livermore Laboratory, PO Box 808, Livermore, CA 94550

JULY 24-29—ISA Sym for Innovation in Measurement Science, Hobart/Smith College, Geneva, NY. INFORMATION: Peter Vestal, Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

JULY 28-29—AMC-Pacific 77, San Jose, Calif. INFORMATION: Peter Szego, Ampex Corp, Mailstop 3-22, 401 Broadway, Redwood City, CA 94063. Tel: (415) 367-3126

AUG 8-12—IFIP Congress 77 (Internat'l Federation for Information Processing), Toronto, Canada. INFORMATION: Robert C. Speiker, U.S. Committee for IFIP Congress 77, Registration and Accommodations, Western Electric Co, 222 Broadway, New York, NY 10038

AUG 23-26—Internat'l Conf on Parallel Processing, Bellaire, Mich. INFORMATION: Dr Charles S. Elliot, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812

SEPT 6-8—7th Internat'l Congress on Instrumentation in Aerospace Simulation Facilities, Royal Military College of Science, Shrivenham Wiltshire, England. INFORMATION: Gen'l Chm, 7th ICIASF, P. W. W. Fuller, R31 RARDE, Fort Halstead, Sevenoaks, Kent, England

SEPT 6-9—COMPCON FALL, Washington, DC. INFORMATION: COMPCON Fall '77, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

SEPT 19-21—WESCON (Western Electronic Show and Convention), San Francisco, Calif. INFORMATION: William C. Weber Jr, Gen'l Mgr, WESCON, 999 N Sepulveda Blvd, El Segundo, CA 90245

SEPT 26-28—Internat'l Electrical Electronics Conf and Exhibition, Toronto, Canada. INFORMATION: Internat'l Electrical Electronics Conf and Exposition, 1450 Don Mills Rd, Don Mills, M3B 2X7, Canada

SEPT 26-28—Distributed Computer Control Systems Internat'l, University of Aston, Birmingham, England. INFORMATION: IEE, Savoy Place, London, WC2R OBL England

SEPT 27-29—Military Electronics Defense Expo 77, Wiesbaden, W Germany. INFORMATION: Joseph Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

OCT 3-6—EUROMICRO Sym, Amsterdam, The Netherlands. INFORMATION: Ted Holtwijk, Philips Elcoma, Bldg BAE 2, NL-Eindhoven, The Netherlands

OCT 6-8—3rd Internat'l Conf on Very Large Data Bases, Tokyo, Japan. INFORMATION: James Gabbert, MIT Sloan School, 50 Memorial Dr, Rm E53-330, Cambridge, MA 02139

OCT 6-12—Stockholm Internat'l Technical Fair, Stockholm, Sweden. INFORMATION: Radley Communications Ltd, 509 Madison Ave, New York, NY 10022. Tel: (212) 838-9215

OCT 18-20—Internat'l Conf on Modeling Semiconductor Devices, Lausanne, Switzerland. INFORMATION: Secrétariat des Journées d'électronique, Dept d'électricité-EPFL, 16 chemin de Bellerive, CH-1007 Lausanne, Switzerland

SEMINARS

JUNE 21-23—IOSA 8th Annual U.S. I/O Systems Seminar, New York, NY. INFORMATION: Input/Output Systems Assoc, PO Box 1333, Stamford, CT 06904. Tel: (203) 323-3143

JULY 20-22—Computer Networks; JULY 27-29—Understanding Performance Evaluation, Los Angeles, Calif. INFORMATION: Technology Transfer, Inc, PO Box 49765, Los Angeles, CA 90049. Tel: (213) 476-1331

OCT 25-27—IFAC Workshop on Information and Systems, Compiègne, France. INFORMATION: Prof B. Dubuisson, Université de Technologie de Compiègne, Département MAI, BP 233, 60206 Compiègne Cedex, France

SHORT COURSES

JUNE 20-24—Microprocessors and Microcomputers: Theory and Applications; JULY 5-8—Computer Communications Networks; JULY 6-8—Microcomputer Interfacing Workshop; JULY 11-12—Minicomputer Programming and Interfacing Techniques; JULY 13-15—Engineering Applications of Minicomputers; and JULY 20-22—Microprocessors, Washington, DC. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

JULY 11-13—Surge Protection of Electronic Equipment, Madison, Wisc. INFORMATION: Willis F. Long, Dept of Engineering, U of Wisconsin-Extension, 432 N Lake St, Madison, WI 53706. Tel: (608) 262-2061

JULY 11-15—Digital Communications in Spread-Spectrum, Data Bus, Optical Fibers, and Common-Carrier Systems; JULY 18-22—Logical Design for Digital Computer and Instrumentation Systems; Database: Distributed, Systems, Models, Reorganization; JULY 25-29—Mini and Microcomputers: Their Structures, Characteristics and Applications; and Database Design Methodology, Ann Arbor, Mich. INFORMATION: Continuing Engineering Education, U of Michigan, 300 Chrysler Center, N Campus, Ann Arbor, MI 48109. Tel: (313) 764-8490

JULY 12-15 and 25-27—Digital Image Processing, JULY 18-21 and 27-29—Computer Techniques in Image Pattern Recognition and Analysis, Los Angeles, Calif and Washington, DC. INFORMATION: Enrollment Secretary, Integrated Computer Systems, Inc, 4445 Overland Ave, Culver City, CA 90230. Tel: (213) 559-9268

JULY 18-22—Current Issues in Information Systems Research, MIT, Cambridge, Mass. INFORMATION: C. Lawrence Meador, Ass't Director, CISR, E53-311, Sloan School of Mgmt, MIT, 50 Memorial Dr, Cambridge, MA 02139. Tel: (617) 253-2930

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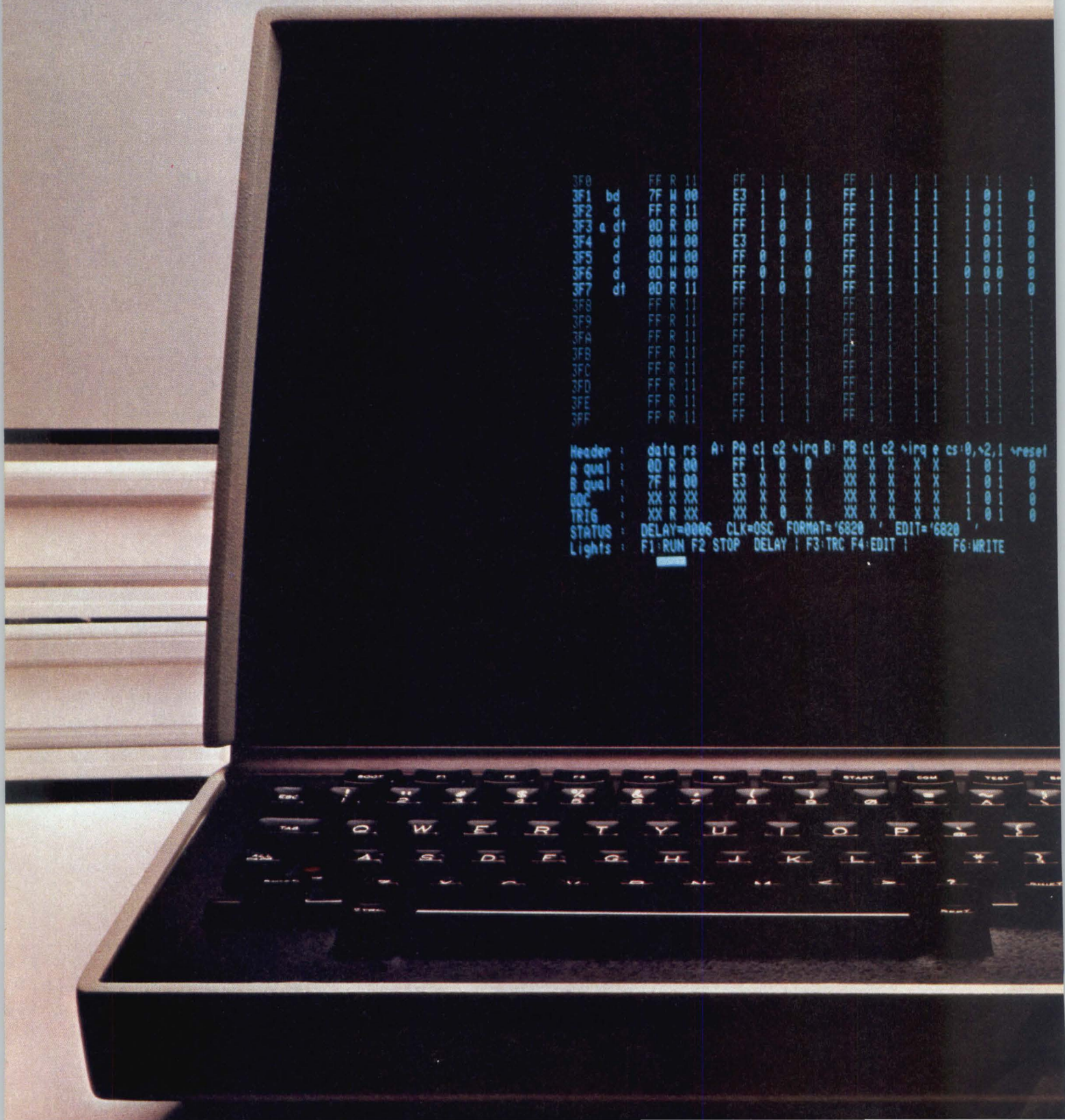

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COMMUNICATION CHANNEL

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Shared User Networks

A major and continuing objective of data communications system users is to achieve and maintain the lowest possible monthly cost for leased lines connecting their remote terminals to centralized processing centers. The growth and success to date of the specialized communications common carriers has been stimulated totally by this unending quest of lower communications costs. Many design techniques have been implemented in data communications networks for this sole purpose. Use of multipoint leased circuits as well as implementation of time division and frequency division multiplexers are examples of these traditional techniques.

In the past there has existed an unofficial source of lower cost communications networks for central processing site access, beyond the availability of leased data channels from traditional communications common carriers such as AT&T and Western Union, and the more recent availability of offerings from specialized carriers, such as MCI, USTS, SPCC, etc. The ability of independent users of data communications networks to pool their line requirements and share a common network has become increasingly more commonplace. This has been permitted under applicable tariffs (ie, FCC260) to allow nonaffiliated users to share a communications leased line network to achieve access to a centralized location. Guidelines under which this sharing has been permitted have not been defined clearly other than the requirement that the communications costs must be shared by some equitable allocation method to all shared users of a particular network. Use of network management fees as well as the shared cost of multiplexers and other network equipment has not been clearly defined or enforced in the past history of shared user environments.

Under the present private line tariff structure, the appeal for the shared user environment basically is limited to lower speed remote terminals geographically clustered in metropolitan areas that are populated by similiar data rate terminals of other potential shared users. The only communications channel that is presently subject to sharing, and promises any significant economic advantage by sharing, is the typical voice grade channel. Usually the type 3002 channel, using AT&T's FCC260 tariff nomenclature, is the only long distance private line which realistically can be considered for shared usage. Its sharing can be achieved on either a time or frequency allocation basis; both methods automatically imply the inclusion of multiplexing techniques. The exception to this premise is a type 3002 channel which is exclusively assigned to each shared user for defined contiguous time periods. For example, a user may require the use of a private line during business hours and then may make the line available by a transfer switching arrangement at the private line's terminations to another user for usage during nonbusiness hours.

In practice, this continuous time allocation example is not the usual shared user arrangement. Typically a time (TDM) or frequency division (FDM) multiplexer is associated with the shared private line at its terminations. Each of the users is assigned a defined portion of the private line's available frequency spectrum through the use of FDMs. A more common configuration is to implement TDMs at each end of the private line and to assign each shared user terminal a portion of the data rate capacity of the common private line's data rate.

In order to realize any practical economics, a shared user terminal, and hence its allocated portion of the private line's capacity in frequency or data rate, must be kept relatively small. If a remote terminal that operates at 2400 bits/s attempts to share a private line through TDM that is clocked at 4800 bits/s, the resulting economics anticipated by sharing is lost. Assume that the shared private line cost $1000 per month and that the two multiplexers and modems cost an additional $2000 per month in equipment rentals. The allocated monthly cost for this 2400-bit/s remote terminal would be approximately $1500 per month. If a direct private line were installed for only this remote terminal, the monthly communications cost would only approximate the $1000 per month. If the remote terminal, however, only operated at 150 bits/s, and this shared private line were fully utilized, the allocated cost would only be $93.75 per month. This is considerably less than the cost of a direct voice grade channel. Typically, shared usage rapidly loses its economic advantage if the remote terminal's data rate is beyond 300 bits/s.

(*Continued on p 14*)

DATAPRODUCTS FOR A NEW ERA

SETS THE STAGE IN PRINTERS.

The date: June 13 to 16, 1977.
The place: the National Computer Conference.
The place to be at NCC: Booth #1273.
The Printer Company's booth.

When something new happens in printers, it happens at Dataproducts.

But don't take our word for it, come to booth #1273 and see for yourself.

This year, we will be announcing and exhibiting some exciting new printers at exciting prices.

They make use of the latest technologies to meet today's needs.

They are high-quality, high-dependability, low-cost machines.

And since they're from Dataproducts, you can be sure that they're reliable.

We have a complete line of commercial and military printers, from 300 LPM to 1500 LPM.

And we're expanding our line to meet the growing needs of OEMs and their customers.

Our printers are performing the world over in every type of application, from remote terminals and small business systems, to large general purpose computer systems.

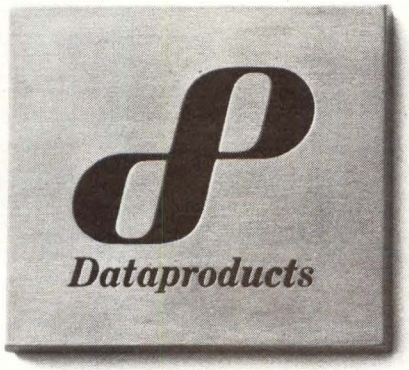
To better serve our world-wide market, we have manufacturing facilities in the U. S. and in Europe.

A commitment to R&D, a determination to design and produce highest-quality printers, and a dedication to customer satisfaction, have helped make Dataproducts The Printer Company.

If you want to know what's new in printers, the place to be is booth #1273.

And if you can't make it to the show, call or write us.

We'll be more than happy to tell you how Dataproducts' New Era in Printers can expand your horizons.



THE PRINTER COMPANY

NORTH AMERICAN SALES HQ: 6219 DE SOTO AVE., WOODLAND HILLS, CA. 91365, TEL: (213) 887-8451, TELEX: 69-8492.
EUROPEAN SALES HQ: DARMSTAEDTER LANDSTRASSE 199, FRANKFURT, W. GERMANY, TEL: 681-034, TELEX: 841-416344.

Unless the remote terminals which are to operate in a shared environment are geographically clustered, the economics can again be significantly impacted. Today's private line tariff rates, as illustrated by AT&T's FCC 260 Tariff, provide a high initial monthly cost and a declining per mile IXC charge as the mileage of the communications channel increases without interruption. If a remote terminal is a great number of miles from the nearest shared multiplexing location, the cost of that remote terminal's "local" line to the shared mutiplexer plus its allocated cost of the shared network may approach and possibly exceed the monthly cost of a direct line between that remote terminal and its intended destination.

The shared user network environment evolved without any major direction from regulatory bodies until January 1977. At that time the Federal Communications Commission (FCC) directly addressed this business area and established guidelines under which sharing of private line capacity may be permitted without infringing on the domain of a regulated communications common carrier. Prior to this FCC ruling, shared usage had evolved its own application area encompassing everything from the joint sharing of a common communications channel to pseudo-common carriers which were realizing profit from the sharing, or more accurately, the brokering and management of data communication networks. The objective of the FCC order was to clarify the shared user environment to permit data communications users to legitimately share channels so as to collectively reduce their monthly communications cost. The FCC also intended by its ruling to clearly isolate and prohibit any organization from realizing the economic benefits of acting as a communications common carrier without the responsibility and accountability required of a legitimate communications common carrier.

The actual initiating step in bringing this matter to a definitive position was the July 1, 1976 action of the FCC adopting a policy which instructed communications common carriers to remove from their private line tariffs any provisions that would not permit unlimited resale and shared use of their private line offerings and services. That policy resulted in a number of filings to the FCC and was also subject to court appeals which resulted in the policy's not being immediately reflected in various private line tariffs. In its January 6, 1977 Resale and Shared Use decision, the FCC made two key rulings. It restated that the existing tariff restrictions relating to this area were unlawful. The FCC did not specify exactly what the new tariffs must contain but established only general guidelines and intents. The new private line tariffs were to be filed in March 1977 with scheduled effectiveness in 90 days. AT&T filed their tariff on March 23, 1977 to be effective in June 1977. This new private line tariff while reflecting AT&T's interpretation of the FCC's guidelines also revises the MPL rates and discontinues the TELPAK service. (See *Computer Design*, June 1977, p 19, 22.)

The January 6th position of the FCC established conditions for the legitimate shared use of common data communications networks in an unregulated environment. In general, any organization or group of organizations may share common networks without the imposition of FCC regulation if the sharing is not implemented as a business objective. Shared use of private lines and associated network equipment for the purpose of reducing all such users' communications costs in a uniform and peripheral manner is clearly encouraged by the FCC's ruling and generally reflected in the March tariff filings. The FCC was quite clear that it did not intend to establish a business environment that would permit the emergence of pseudo-communications common carriers.

The FCC stated that an organization providing communications services on a shared user basis *cannot* show any profit from their communications activity, including revenue realized from fees for the management of the network. In the past, some shared user participants would directly allocate the regulated costs such as for the private line or modems as billed by the associated common carrier; they would then add a significant charge for the use of the nonregulated equipment such as multiplexers, and/or a management fee for a great variety of intangible and generally unspecified services and benefits. As long as the total amount was less than a direct line cost, the shared user was content to pay the unsubstantiated and generally inflated charges thereby providing a profit from shared communications services to the sharing organization. Under the January decision, such accounting manipulations are not acceptable. The governing criterion is the intent of the sharing organization. If it is merely to reduce all its shared users' costs without generating a profit, it will be considered within the scope of this ruling. If the sharing organization is attempting to develop a self-substantiating business activity from sharing, then it is clearly outside the definition of the shared user decision.

In this same context of profit, the use of nonuniform cost allocation methods are considered as contrary to the intent of this ruling. If a sharing organization establishes a 2-tier allocation policy in which its own terminals receive a much lower proportional cost allocation than a similiar terminal associated with an outside user, this can be considered as a means of creating indirect profit by significantly reducing the sharing organization's internal costs at the expense of the outside shared user. While the FCC did not specify exact limits for such tiered allocation methods nor explicitly prohibit such arrangements, such a situation would most likely be interpreted as contrary to the intent rather than the letter of that FCC ruling.

The FCC, in concert with this emphasis on intention, prohibited a sharing organization from actively and publicly soliciting outside shared users. It is reasonable to expect public notices of available network capacities to be issued by interested parties. This solicitation activity, however, would be considered overt if a nationwide advertising and promotion campaign were initiated by such a sharing organization. An additional criterion that may be applied by the FCC would be the extent to which a sharing organization has expanded its data communications network beyond its internal needs to accommodate outside shared user requirements.

The shared user liberalization of present and proposed tariff filings increase this opportunity for lowest possible communications costs. Nework designers who are considering shared usage as a reliable means of lowering communications costs must be familiar with the provisions of the January 1977 FCC ruling and tariff filings. To become involved with a legitimate shared use association would provide reliable increased communications value; to commit vital data communication needs to a pseudo-communications common carrier would result in continued subsidization of the sharing organization's communications cost, and upon eventual discovery by regulatory agencies, discontinuation of your data communications capability in that shared environment.

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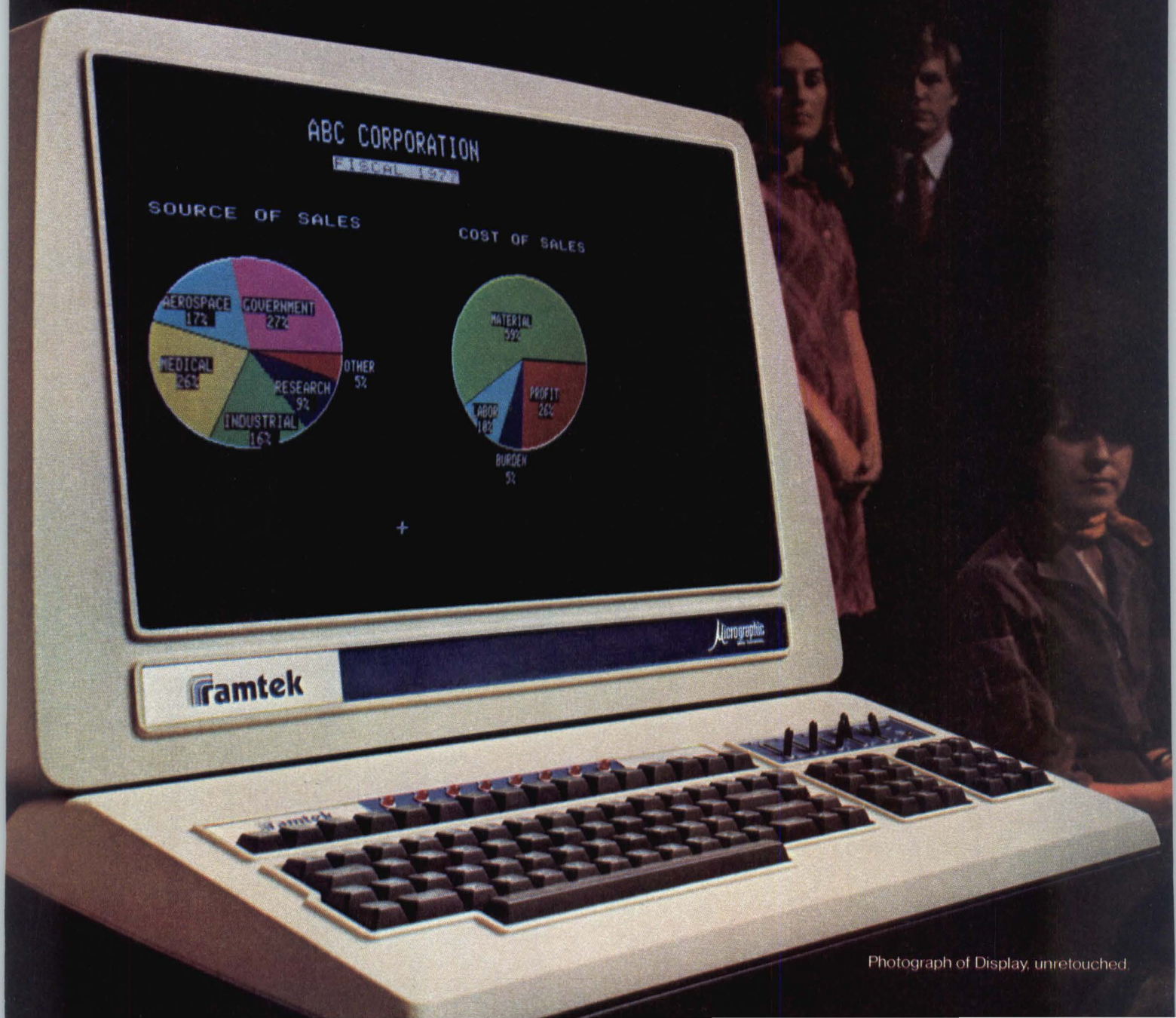
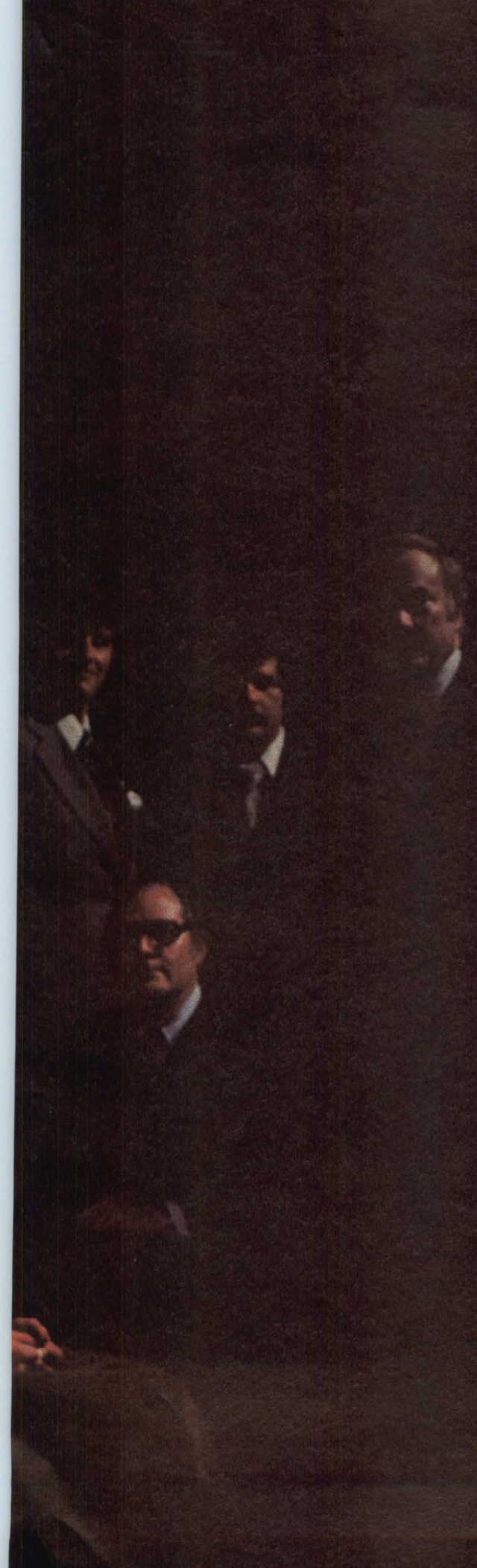
Look what Ramtek has done to graphic terminals.

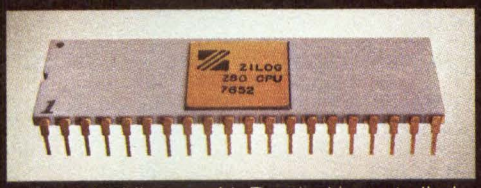


Photograph of Display, unretouched.



Now you can get quality resolution and a combination of true graphics and true alphanumerics at an affordable price.

Ramtek introduces the new Micrographic Terminal. No longer do you have to settle for poor resolution or give up color in economy priced display terminals. Ramtek gives you a high resolution, flicker-free display on a resolvable matrix of 512 elements by 256 lines. And you get a choice of black and white or any 8 of 64 colors as well as split or dual screen capability. The independent alphanumeric refresh offers you single character addressibility within a visible matrix of 25 rows of 80 characters that are crisp, sharp and well defined.



Ramtek's Micrographic Terminal is controlled by a powerful Zilog Z-80 with 28K bytes of PROM and 16K bytes of RAM.

In addition you can program the Ramtek Micrographic Terminal and give it the dedicated capability and intelligence you need for your application. Ramtek's software gives you TTY compatibility and high level graphic functions commanded by ASCII text strings. You can choose from an extensive list of options such as floppy disc interface, additional serial I/O ports, alphanumeric overlays, user defined fonts, color selections and packaged software.

More good news: prices for a black and white basic system begin at just $4,700 and for color at only $5,400.

But to fully appreciate the contribution the Ramtek Micrographic Terminal can make to your application, you'll need to know more details. Just call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale CA 94806. If you're really in a hurry call us at (408) 735-8400 and ask for Todd Martin.

ramtek

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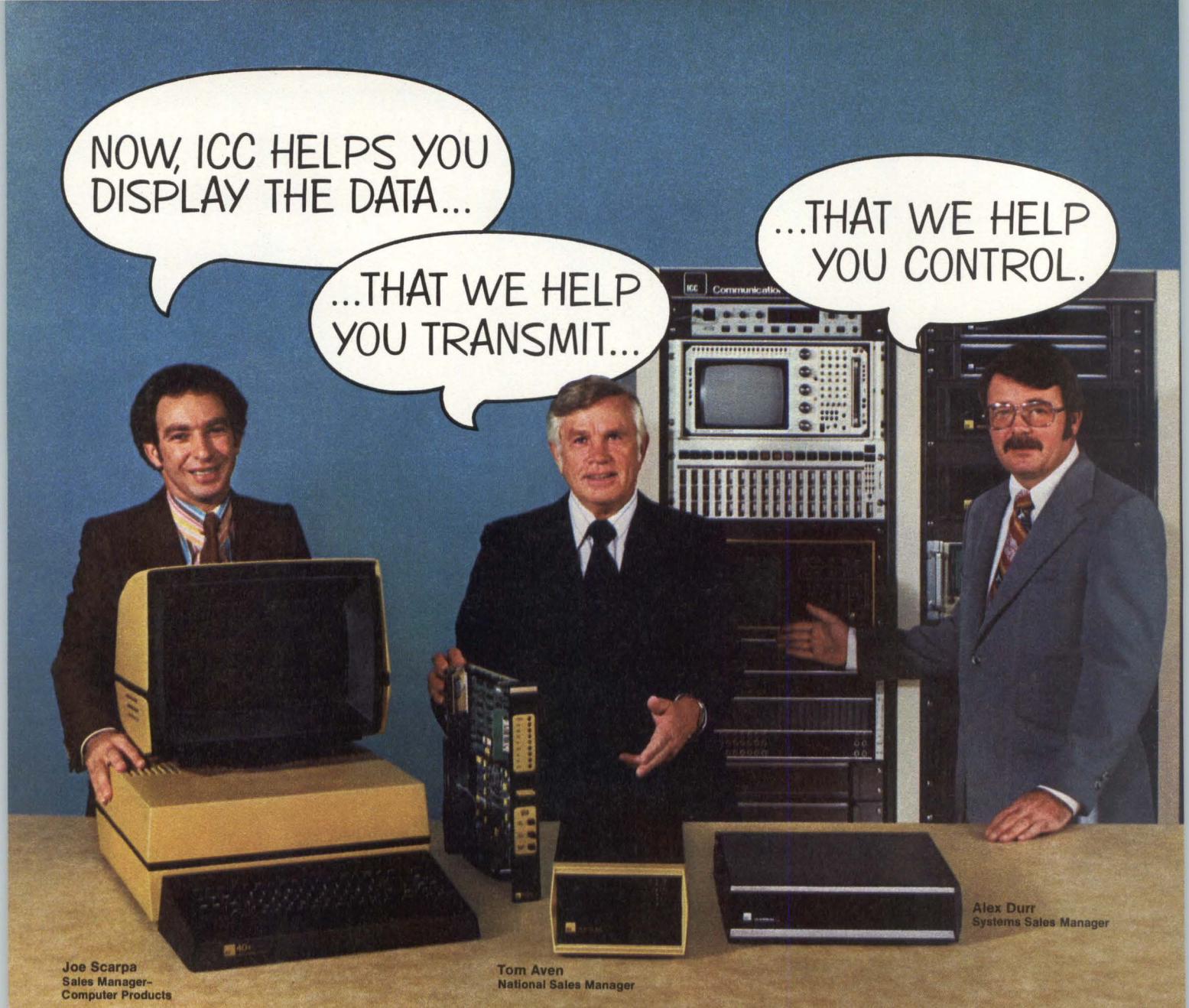
CIRCLE 9 ON INQUIRY CARD



Your data—where you want it, when you want it, in the form you want it. Now you can get it all from ICC. Dependable ICC data display terminals give you superior visual displays with optional hard copy printouts. Our full line of modems transmits your data at speeds up to 9600 bps. And ICC system monitoring and controls can improve the efficiency of your entire data network.

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Remote Batch Terminal Communicates With Two Companies' Computers

A computer-based remote data communications terminal for Control Data and IBM computers, and the worldwide CYBERNET data services, the Cyber 18-5 also expands remote data handling applications for the Cyber 18 family of standalone minicomputer equipment. The batch terminal contains special computer logic for communicating with the computers as though it were any of several models of terminals supplied by these companies.

Basic terminal includes computer processor, 16k bytes of memory, visual display and keyboard operator console, one terminal emulation program, communications control capabilities, peripheral controller, interface logic, card reader, and line printer.

According to Control Data Corp, PO Box O, Minneapolis, MN 55440, a key advantage is overall lower operating costs. Addition of an optional magnetic unit to the basic configuration allows transfer of more data, thereby reducing charges for communications line use and connect time. Online batch and local utility functions can be performed concurrently; this includes intercommunication among the terminal's display, card, printer, or tape units while data are transferred to and from the terminal and host computer system.

The processor is a microprogrammed computer that includes 16k bytes of 750-ns core memory. Expansion is possible up to 64k bytes in 16k-byte increments to support data transfer applications and optional magnetic tape units. The keyboard-visual display, a version of the company's 751-10 microprocessor-controlled display, functions as the terminal operator's information and control station.

Terminal communications are conducted with a host computer system in half-duplex synchronous mode. Switches allow selection of data transmission rates ranging from 1200 to 9600 bits/s. Standard interface compatibility is provided for RS-232-C and CCITT V.24 communications protocols.

One of a series of three controlware programs also is included. These enable the terminal to emulate operations of the company's 200 user terminal with the 3000, 6000, Cyber 70, or 170 system as host computer; or an IBM 2780 or 3780 remote batch terminal.

Up to three model 1860 magnetic tape transports can be added to the terminal to support higher speed batch entry applications. Drives operate at 25 in/s (63.5 cm/s), record at 800 bits/in (315 bits/cm) NRZI, and come in 7- and 9-track models. The controller is contained on a single PC board.

Model 1829 card readers are available in 300- and 600-card/min versions, each housed in a desktop unit. Optional line printers (1827-30 and -60) provide 300- and 600-line/min print output.

Other software available with the terminal is the CYBER 18 RTOS (real-time operating system). RTOS, a compatible subset of the Mass Storage Operating System (MSOS) used with other systems, requires no mass storage disc devices. It occupies a minimum of 3k bytes of main memory.

Prices range from $28,345 for the basic unit with 300-card/min card and 300-line/min printer peripherals, to $59,915 for a terminal configuration including two magnetic tape transports plus 600-card/min card and 600-line/min printer units. Monthly leases on a 1-year contract, including maintenance, for these configurations are $1084 and $2482, respectively.

Circle 166 on Inquiry Card

Tariffs Filed to Alter and Reduce Rates of Private Line Services

In response to orders by the Federal Communications Commission (FCC), the American Telephone and Telegraph Co (AT&T), Long Lines Dept, Bedminster, NJ 07921 has filed tariffs to permit sharing and resale of its private line services and to eliminate Telpak—its bulk private line service offering. Simultaneously, the company filed reductions in some of its voice grade private line rates in an effort to lessen the impact of higher rates that customers would pay when Telpak is no longer available. These reductions—to coincide with the elimination of Telpak on June 8—would lower rates for individual voice grade private line services generally 100 miles or longer. Rates for shorter distances would remain unchanged.

A private line is a circuit leased at a fixed monthly rate; with Telpak, users with large communications needs can purchase 60 or 240 private lines at a time. AT&T feels that a bulk service replacement for Tel-


POWER
LINE

You get more than 125 IPS in the Number One Tape Drive

Wangco Mod 14 – the first "no compromise" 125 ips tape transport with 500 ips rewind speed for OEM systems, gives you:

1.

EXTRA LENGTH VACUUM COLUMNS.
For the first time a 125 ips tape transport is *designed* to give speed plus reliability. Extra vacuum column length eliminates the need for a high powered reel servo system and power supply such as that used in "short column" designs, therefore, no cooling of the reel motor is required. The Mod 14 configuration allows high performance operation with no program restrictions.

1.

115 VAC POWER OPERATION AND LOWEST POWER CONSUMPTION.
Due to Mod 14's unique design, only 10.5 Amps of standard 115 VAC power are required, reducing operating cost and complexity. At 230 VAC the Mod 14 uses only 6.5 Amps.

1.

AUTOMATIC LOAD.
The Mod 14 will accept IBM Easy Load I* and II* cartridges permitting fully automatic tape load, and rewind and unload by software control.

*Trademarks of IBM Corporation

1.

UNIQUE TAPE PATH LAYOUT.
A straightforward tape path configuration eliminates unsupported lengths of tape and does away with air bearing guides, air compressors and application of vacuum on the capstan. The simplified drive design results in greatly increased reliability.

1.

CONSERVATIVE DESIGN.
All components and subassemblies of the Mod 14 are built and tested to meet "worst case" requirements assuring highest reliability in all applications including high duty cycle mainframe systems with ample operating margins.

1.

FRONT ACCESSIBLE SUBASSEMBLIES.
All adjustments and test points of the Mod 14 are accessible from the front of the unit. Subassemblies, including the card cage, are modular for instant replacement.

1.

DUAL DENSITY WITH EMBEDDED FORMATTERS AVAILABLE.
Data densities to 800 cpi NRZI and 1600 cpi PE are provided, individually or in switch selectable dual density (NRZI/PE). Wangco's embedded formatters, an optional feature, reduce cost and power requirements in system operation.

These No. 1 features plus long life, hard coated heads, four drive daisy chain with unit select capability and RFI/EMI criteria design – add them all up and you get the Wangco Mod 14. For information contact Wangco, Inc., 5404 Jandy Place, Los Angeles, CA 90066. (213) 390-8081. In Europe: P.O. Box 7754, Building 70, 1st floor, Schiphol-OOST, Netherlands. Phone: (020) 458269. TWX: 844-18822 WANGCO NL.

WANGCO
PERKIN ELMER DATA SYSTEMS

CIRCLE 11 ON INQUIRY CARD

pak would not be viable due to the sharing and resale provisions for private line services ordered by the FCC.

Effective June 21, the shared use and resale tariff would enable users to share a private line service or—subject to FCC certification—resell it to third parties. The tariff is in response to FCC decisions directing all carriers to remove existing restrictions against sharing and resale of private line service.

This filing does not apply to international private line services, the company's interstate message telecommunications service, or Wide Area Telecommunications Service (WATS). Opposing the sharing and resale order, AT&T has asked the U.S. Court of Appeals for the Second Circuit in New York City to review the order.

Low Speed Terminal Receives AUTODIN Category II Approval

Having passed the Defense Communications Agency's AUTODIN (Automatic Digital Network) Category II test requirements, the system 2407-T20 low speed AUTODIN terminal from Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054 is now a complete TEMPEST-approved system which can be marketed to various government agencies utilizing the network. Category II is one of three categories involved in the acquisition of AUTODIN terminals. The acceptance was approved by the Data Communications TEMPEST Working Group as a result of evaluation of satisfactory test data by the National Scientific Laboratory.

The secure, worldwide electronic communications network provides subscribers with compatibility in areas of codes, speeds, and formats. It provides automatic error detection service by levels of precedence, alternate routing capability, message accounting, and protection. TEMPEST is an unclassified name referring to investigation and studies of compromising emanations.

Draft Standard Covers Improved Communications Link Control Procedures

The proposed 6th draft of the American National Standard (ANSI) Advanced Data Communication Control Procedures has been accepted for public comment by Standards Committee X3. The X3S34 Task Group, chaired by David E. Carlson, Bell Telephone Laboratories, developed the standard, which is informally referred to by the initials "ADCCP." ANSI identification is BSR X3.66.

As the culmination of development work which began in 1969, the standard embodies improved ways to perform communications link control functions, providing desirable capabilities inherently unavailable in the earlier standard X3.28-1976, "Procedures for the Use of the Communications Control Characters of ASCII in Specified Data Communications Links." That standard is character-oriented, using 7-bit ASCII characters or sequences of characters for the link control functions; the ADCCP standard is based on a bit-oriented approach for link control, and an independent/dual numbering per frame.

Basic objectives of the standard are to provide full transparency and code independence; efficient interactive and batch operation; a high level of reliability; 2-way alternate and 2-way simultaneous operation between computers, concentrators, and terminals which are normally buffered; and a high level of modularity. It also covers data link configurations, such as full- and half-duplex, multipoint, point-to-point, switched, or nonswitched.

The standard establishes procedures to be used on synchronous communications links using ADCCP. It does not define any single system and should not be regarded as a specification for a data communications system.

Its development was accomplished in close liaison with corresponding international standards body, ISO/TC97/SC6 where the basic technique is identified as HDLC (High-level Data Link Control) and also with the European Computer Manufacturers Association (ECMA). The document may be obtained for $4 per copy from the X3 Secretariat, Computer and Business Equipment Manufacturers Association (CBEMA), Standards Dept, 1828 L St, NW, Washington, DC 20036.

Joint Agreement Provides Overseas Packet-Switched Service

An interconnection agreement for the provision of packet-switched data communication service between the United States and overseas points has been announced by Telenet Com-

AMP's CR connectors prevent damage to pc board traces.

They mate with Zero Insertion Force.

AMP 40 position CR connectors assure excellent connections. Because they apply over 150 grams of force to each contact with just a turn of the cam. The wipe backwipe motion of the contacts precleans the surfaces for full electrical continuity. And contact wear is virtually nonexistent for well over 5,000 insertion cycles.

The 40 position CR connector is designed specifically for input/output functions in today's high density pc board applications such as those used in microprocessors. Its modular design means extra economy because it can be loaded with as few or as many contacts as you'll actually use. And it will accept either crimp snap-in or insulation displation modules.

There are other sizes of AMP CR connectors including the 120 and 156 position types. All have positive lock and keyed housings with contacts on .100" centers. And all come with AMP's assurance of experienced technical aid whenever and wherever you need it.

For more information on CR Series connectors, call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

AMP has a better way.

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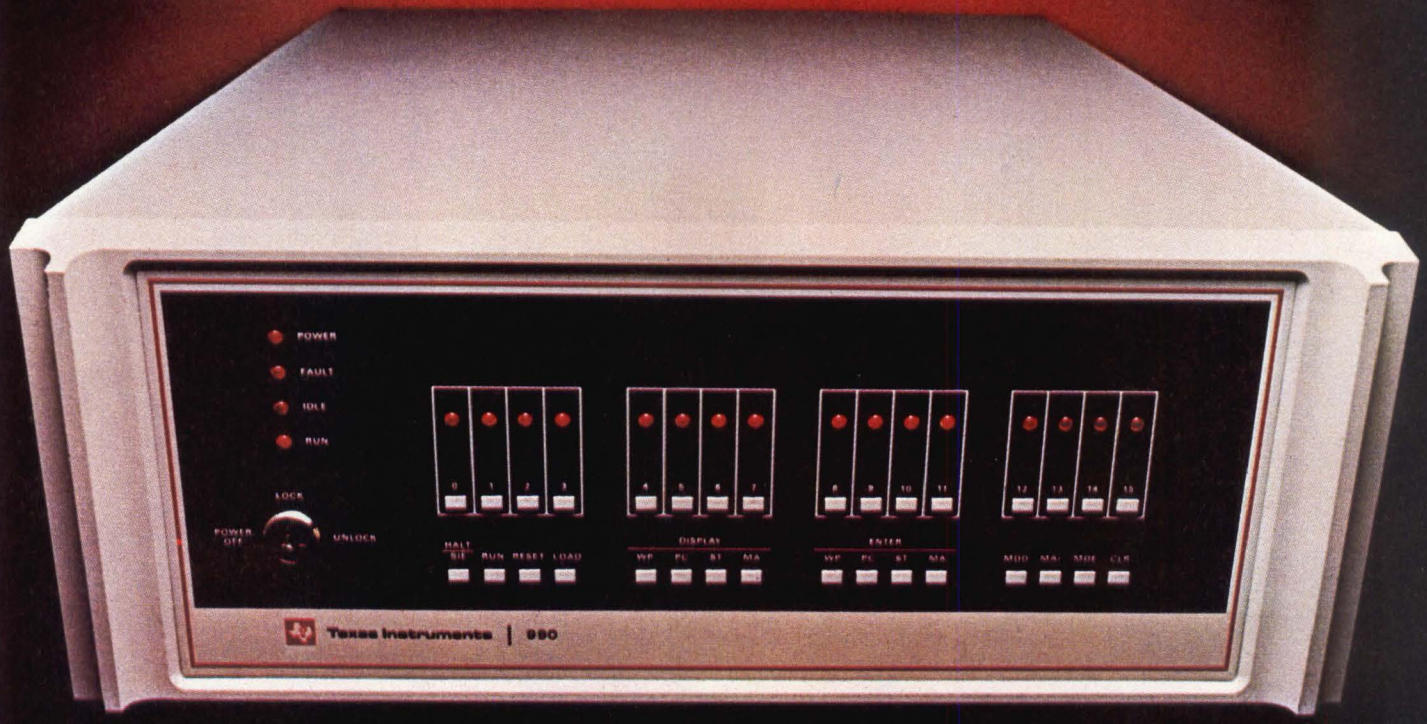
CIRCLE 12 ON INQUIRY CARD

990/10 OEM minicomputers.



Built, backed and priced to sharpen your competitive edge.

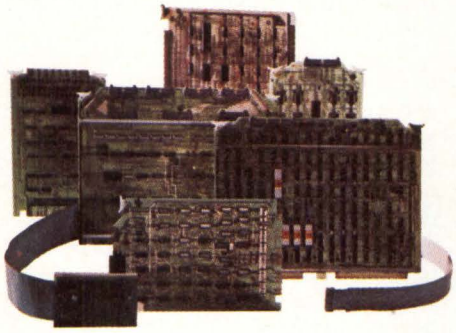
TEXAS INSTRUMENTS.

The 990/10 minicomputer from TI brings superior value to both you and your customers.

Starting with field-proven hardware, the 990/10 delivers the reliability you expect from TI. And all the off-the-shelf support you need for user applications. You get standard software languages, a broad choice of peripherals and nationwide service.

Built for more processing power.

The 990/10 is the most powerful member of the 990 computer family. Its architecture provides features that give you maximum processing power for your money. Like hardware multiply and divide. A 16-level hardware



Peripheral Interface Modules

interrupt structure. 16 registers arranged in a workspace concept. I/O that's directly programmable through the Communications Register Unit (CRU) and autonomously through a high-speed data bus. And bit, byte and word addressing of memory.

Built for system flexibility.

In small or large configurations, the 990/10 design provides surprising flexibility for a small investment.

The CRU, with up to 4096 I/O lines, reduces interfacing costs by keeping controller complexity to a minimum. The TILINE* asynchronous high-

Model 913 Video Display Terminal

speed data bus can support both high- and low-speed devices and takes advantage of design simplicity for simultaneous data transfer between peripherals, the CPU and memory.

With the 990/10, you get a powerful instruction set with an extended operating feature that allows hardware to take over operations that software would normally execute. An optional mapping feature provides memory protection and memory expansion to 1 million words. And, optional error-correcting memory corrects single-bit errors for increased system reliability.

DS 25/50 Disc Drives

Full peripheral support.

As well as a range of standard peripherals, disc storage to 90 million 16-bit words and magnetic tape with 800 and 1600 bpi options are available for low-cost mass storage and back-up.

A choice of software.

With common higher level languages, FORTRAN IV, COBOL and Multiuser BASIC, plus the 990/10 assembly language, you have all the tools you need for an efficient application program.

Both the disc-based and memory resident operating systems give you modularity and flexibility for system generation to meet application de-

Model 979 Tape Drive

mands. We offer program development aids for creating and testing software, and communications software to support synchronous or asynchronous data transmission.

Backed with nationwide service.

Our responsibility to you doesn't end with the sale. We follow through with complete system training, plus a nationwide factory service network.

The TI 990/10 minicomputer. We build it, back it and price it the way you and your customers want it. You can start configuring a system now with our 990 Computer Systems Handbook on the upward-compatible family of the TMS 9900 microprocessor, 990/4 microcomputer and 990/10 minicomputer. For your free copy, send a letterhead request to Texas Instruments Incorporated, P.O. Box 1444, M/S 784, Houston, Texas 77001.

CIRCLE 13 ON INQUIRY CARD

TEXAS INSTRUMENTS
INCORPORATED

*Trademark of Texas Instruments

See Texas Instruments products at the NCC.

munications Corp, 1050 17th St, NW, Washington, DC 20036 and ITT World Communications, Inc, a subsidiary of International Telephone and Telegraph Corp, 67 Broad St, New York, NY 10004. The service is designed as an economic means of communications between computers and various terminals operating at low and medium speed. ITT Worldcom will furnish the overseas data transmission facilities and gateway switching equipment linking the Telenet network and its users in the U.S. with packet-switching facilities abroad.

In operation since 1975, Telenet was the first FCC-regulated common carrier to utilize packet-switching technology. Local access to the network is available in 47 cities in the U.S., Canada, and Mexico, and will be available in 38 other cities during 1977. This is the second overseas service agreement signed by Telenet; the first was with RCA Global Communications, Inc (see *Computer Design*, May 1977, p 14).

ITT Worldcom provides a variety of record communications to more than 170 countries throughout the world. The company has also introduced the Universal Data Transfer Service (UDTS), using packet-switching data communications techniques for initial operation with France and Puerto Rico. Extensions of the service to other countries are planned for later this year.

The service is intended as a highly reliable means of communications between a variety of terminals and data base and timesharing-oriented computers. Users in the U.S. can access UDTS by means of domestic data networks such as TYMNET, Inc and Telenet Communications Corp, with whom the company has agreements.

Plans for the service include expansion to accommodate data transfer requirements at speeds up to 56k bits/s. Additional features would include automatic translation of varying codes, protocols, and formats; and the ability to connect with terminals such as teleprinters, CRTs, facsimile machines, batch terminals, and word processors.

Terminals Operate on Packet Network and In Concurrency Mode

CRT terminals that can operate on a public packet network while emulating IBM 3270 functions have been demonstrated by Raytheon Data Systems Co, Communications Dept, 1415 Boston-Providence Tpk, Norwood, MA 02062, along with a software system that allows its PTS/1200™ distributed processing system to perform 3270-emulation tasks concurrently with local batch processing, file updating, printing, and other online communications tasks. Both capabilities serve to extend the functional range and cost-effectiveness of applying terminals of the 3270 class to information systems tasks.

Implementation of PTS-100™ intelligent terminals on public packet networks is made possible by two software packages and the use of the international CCITT X.25 device protocol. This capability permits devices other than teleprinters and ASCII-based products to connect through packet modes.

Software packages include DMEP-II which replaces control and emulation programs in IBM 3704 or 3705 front-end processors, and RAYPAC which is loaded into local-site PTS-100 terminal controllers. They convert 3270-type messages into line, device, and address modes required for packet networks. When installed on any of the company's 32k-byte PTS-100 intelligent controllers operating in 3270-emulation mode, the software packages allow such systems to access immediately public packet networks in the U.S. and abroad using the worldwide X.25 and HDLC protocols.

Four major modules of DMEP-II are the line protocol, which replaces conventional bisynchronous protocol with HDLC protocol; the X.25 device protocol, which permits direct connection and disconnection of local devices within a public packet network; the PPX packet protocol extension, which converts conventional 3270 device addresses to suitable packet network addresses; and an operating system. DMEP-II allows the user to run existing applications programs and operate existing communications.

Both packages can be loaded in minutes, without disrupting existing 3270s or other applications; users can therefore create CRT-terminal networks without significant systems development. Advantages obtained are lower transmission costs, fewer line delays, improved error rates, and line speeds up to 56k bits/s (five times faster than current speeds).

Benefits of the 3270-concurrency capability, which allows a single system to operate concurrently in 3270 emulation mode and local processing mode, are said to be obtaining more work from one system, eliminating unnecessary equipment, obtaining

Now there's an alternative to the high cost of mainframe disc storage. DIVA's Computroller V.

If you've decided to buy your minicomputer system from DEC, DG or Interdata, you already know the facts about their disc storage systems. They're well designed. They're also expensive.

Now, you can get the same high performance, reliability and software transparency of the mainframe product at a price that makes sense. With Diva's Computroller V line of disc systems.

The Computroller V matches the mainframer's system feature-for-feature, but costs up to 50 per cent less to purchase, install and maintain. With no shortcuts in design or service support.

The reason? Unlike the mainframer, we specialize in the development of disc storage systems to help you cope with the continuous expansion in information processing. The Computroller V has an amazing capacity range of 25-300 megabytes per spindle. Plus compatibility with the mainframe system and total software transparency.

No other disc storage system can interface, adapt and self-test like the Computroller V. Make your own comparison and see how the Computroller stacks up against other mainframe products.

	DIVA Computroller V	Mainframer
Complete Software Transparency	YES	YES
ECC Error Correction	YES	YES
Complete Customer Services	YES	YES
Resident Self-Checking Diagnostics	YES	YES
Microprocessor Technology	YES	YES
Dual Processor Support	YES	YES
Interface to Most 3330 Technology Drives	YES	NO

From now on, this may be the only system your company will need for mass storage. For more information, fill in the coupon or call Toll-Free at 800-631-2141.

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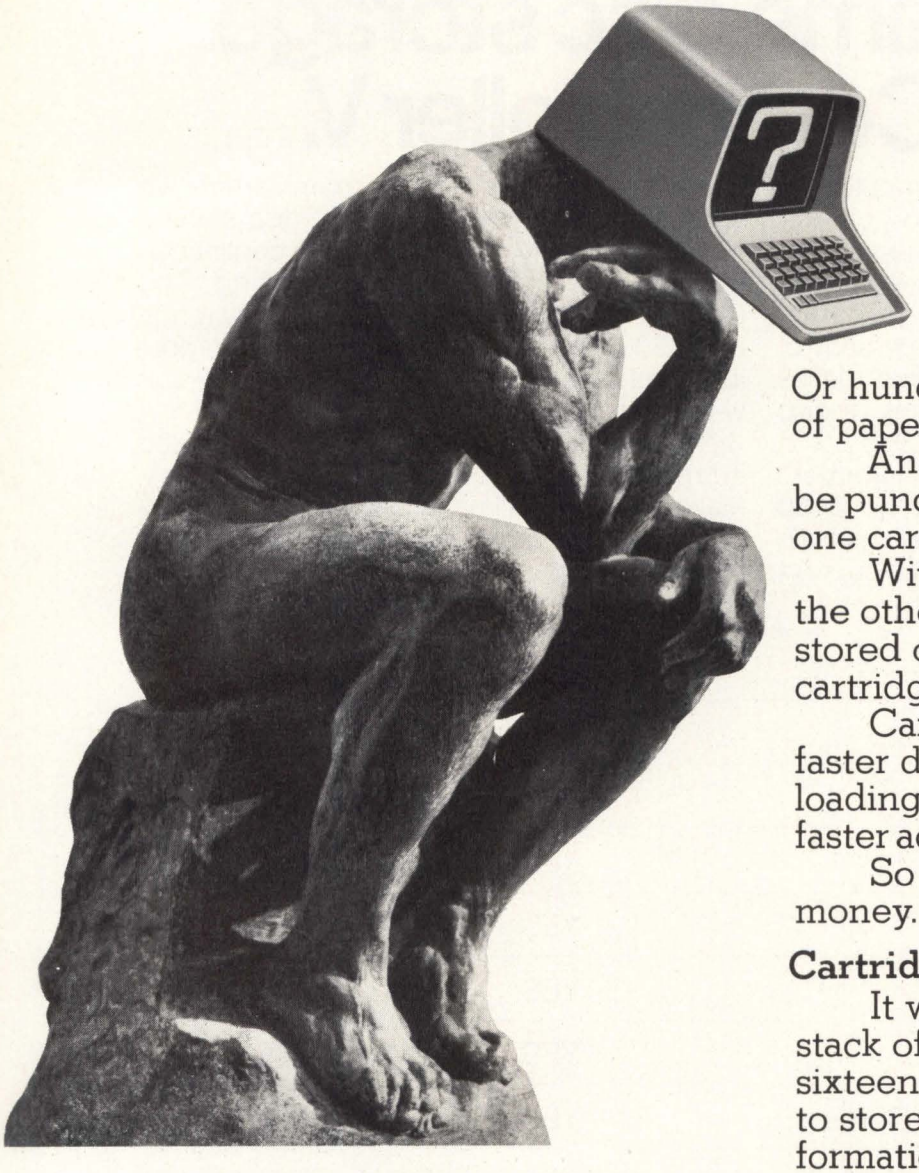
Is your computer smart enough



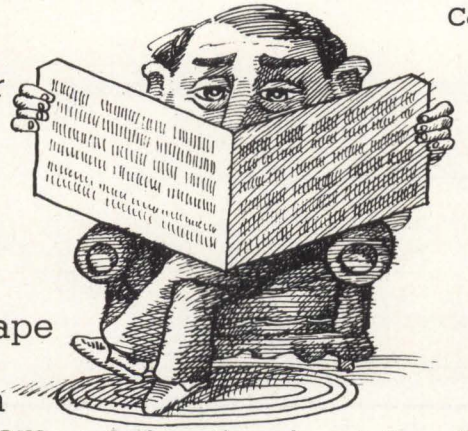
A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

And, if you'd take the time to ask it, your computer would probably tell you so.

It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



Cards must be read one at a time.

Or hundreds of feet of paper tape.

And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

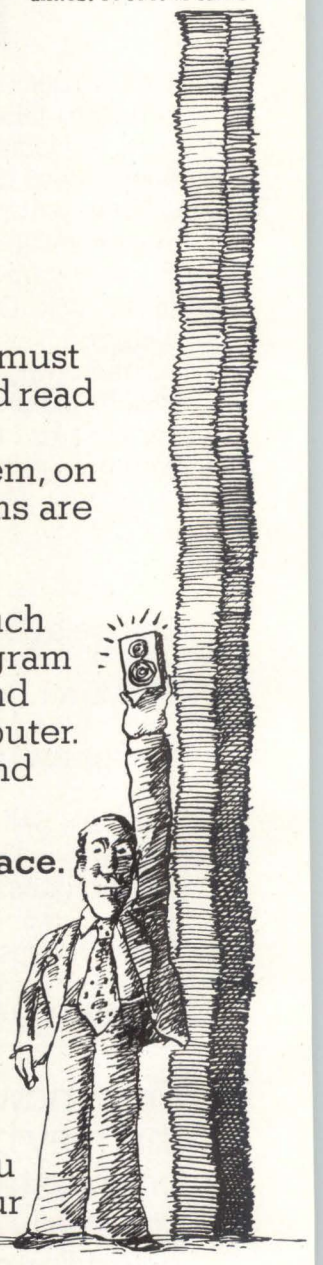
Cartridges take less space.

It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3M DC-300A data cartridge.

With cartridges, you can store all of your programs in a fraction of the space you'd need for cards or paper tape.

Your filing system is simplified and overhead is greatly reduced.

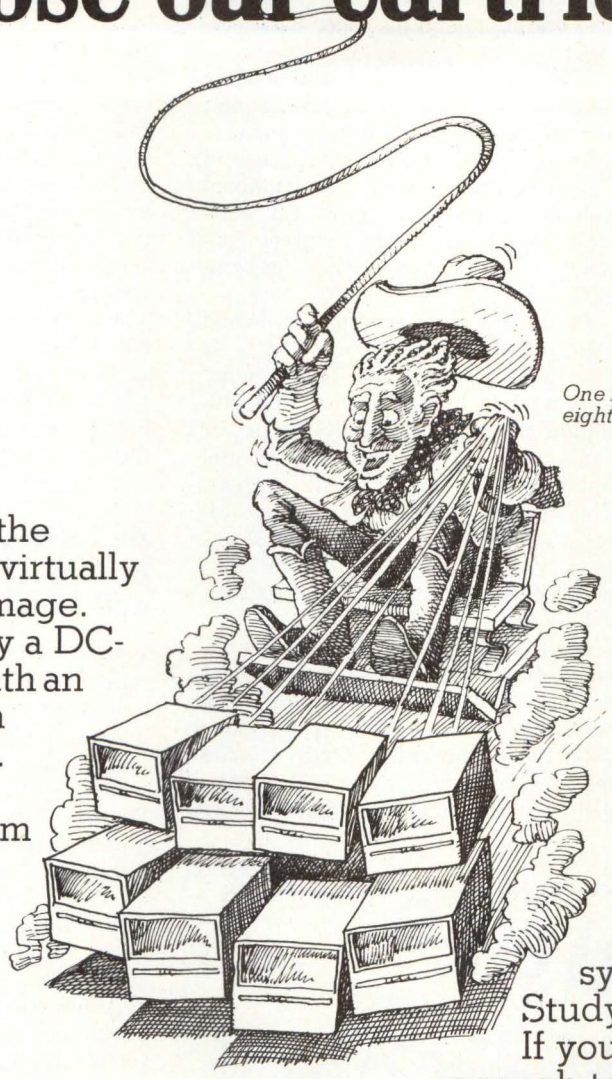
One DC-300A cartridge equals almost 16 feet of cards.



Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need never touch the media. It's well

to choose our cartridge drive?



One formatter can control eight drives at once.

protected inside the cartridges, so it's virtually impossible to damage.

You can carry a DC-100A cartridge with an entire program in your shirt pocket.

Even if you drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards.

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

We'll bet your computer will prefer ours.

Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our unique DCD-1. It offers many of the features of our bigger systems, yet it will fit inside a five-inch cube.

The cartridge alone measures just 2.4 x 3.2 x .5 inches.

See for yourself.

Send us the coupon. There's much more we can tell you about our drive systems.

Study the information carefully. If your computer isn't smart enough to choose our drive systems, we'll bet you will be.

Send me more information.

Name _____ Title _____

Firm _____ Address _____

City _____ State _____

Zip _____

Phone _____

3M COMPANY

Mail to: 3M Company
Data Products, Dept. 125
Mincom Division, Bldg. 223-5F
3M Center
St. Paul, Minnesota 55101

CIRCLE 34 ON INQUIRY CARD

single-vendor support, and improving control and efficiency of information handling at each local site. Both packet network packages and 3270-concurrency capability are available within 90 days under monthly license fees.
Circle 167 on Inquiry Card

Communications Satellite Serves as Backup for Indonesian System

The Palapa 2 satellite has been launched as part of a system to link the Republic of Indonesia with modern communications. That country is the first in Southeast Asia to own and operate its own telecommunication satellite system. The satellite will be in synchronous orbit 22,300 mi (35,000 km) high over the Indian Ocean, serving as a spare to Palapa 1, launched July 8, 1976 and activiated Aug 17.

Hughes Aircraft Co, PO Box 90515, Los Angeles, CA 90009 built the satellite using the same technology as the Anik and Westar satellites developed for Canada and the U.S. Each Palapa provides capacity for 5000 2-way telephone circuits or 12 television channels, or combinations of telephone, TV, radio, telegraph, and data services.

Hughes also designed and built a master control station in Jakarta and nine of the 40 ground stations currently in operation. Ford Aerospace and Communications and International Telephone and Telegraph Co each built 15 stations under separate contracts with the Indonesian government.

Perumtel, the government-owned telecommunications company, is directing operation of the satellite system, which consists of the 40-station network, studio links, power equipment, civil works, personnel training, maintenance, and support. The Palapa system is rapidly expanding the nation's communications services via the 40-ground-station network strategically placed throughout the islands.

Single-channel-per-carrier equipment, controlled by a demand-assignment system, has been installed at each earth station, enabling telephone users to call any other city by dialing the area code. When the call is completed, the circuits are immediately released and become available to the central control station for reassignment to other call stations.

At launch the satellite weighed 1268 lb (573 kg); in-orbit weight after firing of the apogee motor is approximately 645 lb (293 kg). The drum-shaped body measures 61.5″ (156 cm) high and 75.1″ (191 cm) in diameter. The solar drum is covered with 23,000 solar cells which charge an onboard battery system to provide the spacecraft with power when the earth intersects the sun during the spring and autumn eclipse season. The solar cells provide a minimum of 259 W of power for the life of the satellite (seven years or more). A 60″ (152-cm) wide parabolic antenna reflector extends 73.5″ (187 cm) above the spacecraft.

Audio Response System Provides Multiline Output and Touch-Tone™ Input

Votrax LVM-70 is a compact solid-state multiplexed audio response system which can service 64 telephone lines and store vocabulary in digital pattern form in amounts up to 128 seconds of speech. Vocal Interface Div of Federal Screw Works, 500 Stephenson Hwy, Troy, MI 48084 developed the system to provide multiline audio output and Touch-Tone™ input handling capabilities for microcomputers, minicomputers, and large business mainframes. Business machine users are now able to take advantage of Touch-Tone audio response applications.

Features include variable word and message length for maximum flexibility, custom vocabulary of words and phrases, excellent voice quality, and customer's choice of voice. The system supports many communications data sets including the Bell 407A, 407B, and several commercially available 403-type units, plus the Bell Transaction Telephone™, Automatic Call Distributor, and Call Director.

The system controller, containing a microprocessor, can simulate operation of an asynchronous terminal (RS-232-C) on the host computer's communications adapter. Transactions between the controller and host computer are conducted using standard data formats. No special support software or interfacing hardware is required.

Optional program modules offer additional capabilities of synchronous or asynchronous data communications support, local or remote connection to host computer, buffered communications, and transaction time-out. □
Circle 168 on Inquiry Card

The keyboard switch with a heart of gold

...keeps your product WORKING year after year...after year.

In your keyboard or ours, Cherry key switches just don't fail. The knife-edge contact area is so small (9 millionths of a square inch)... the contact pressure so great (about 5,000 psi) ... the gold alloy so pure and film-free... that you are assured of positive contact every time. For 50 million operations and beyond. (Which is probably beyond the life expectancy of your product!)

Cherry "heart of gold" keyboard switches are available as part of a fully encoded Cherry Electronic Keyboard or individually, with or without two-shot molded keycaps. *We have keycaps*... in more legends, sizes, type faces than you're likely to find anywhere else. Sculptured keycaps? We've got 'em. Smooth or matte finish? We've got *both.* Colors? Lighted? Specials? Sure! Some "off the shelf"... all at prices that make it obvious why the *Cherry* way is the *economical* way to put a heart of gold in any keyboard.

SEE US AT NATIONAL COMPUTER CONFERENCE
Dallas Convention Center
June 13-16
BOOTHS 1768-1744

For free test sample switch and catalog, just TWX 910-235-1572... or PHONE 312-689-7700.

CHERRY®

Cherry switches now available locally from distributors.

CHERRY ELECTRICAL PRODUCTS CORP., 3614 Sunset Avenue, Waukegan, IL 60085

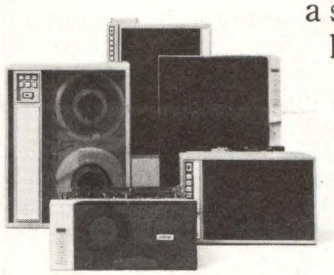
GET YOUR ACT TOGETHER:

It takes a lot of drive to make ends meet today.

We hate to see OEM frustration—the kind caused when you can't close the gap between advancing computer technology, and your peripherals' ability to fit in with your plans. Just coming "sort of close" won't do anymore.

Getting things together is a specialty at Pertec. We're industry-watchers, as well as seasoned participants—trust us to pinpoint exactly what you're going to need...often even before you do. To help you realize the full potential of state-of-art CPUs. With much greater cost-effectiveness.

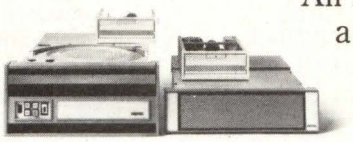
Take our tape drives. (Please.) Already available in more than 400 line-variations—but we didn't stop there. Not Pertec. We anticipated your need for a super-fast, sophisticated tape transport, to handle high volume dp throughput.



The result: our new T1000 family, a *new-generation* in vacuum column drives. 75 to 125 ips; dual density for now, but designed to handle GCR high density recording.

We're devoted to your disk demands too. Rigid or flexible. Both fixed-and-removable. From 0.25 Mb to 50 Mb.

And we didn't give you 50 megabytes by forcing a switch in technology. We simply *expanded* our D3000 Series to include 25-50 Mb units. As extensions to an *existing* line. With technology and parts commonality you're already used to. 50 Mb, without major logistic support changes...without special pre-recorded media.



All Pertec drives are built to *stay* together too. Reliability's a big number with us. Like testing at every manufacturing stage, with 40-hour burn-ins. Like setting up the biggest direct sales and service organization of any independent peripherals manufacturer. Like our toll-free 800 line, for 24-hour, 7-day emergency assistance from strategically located parts-and-repair depots around the world.

Pertec's product families are ready when you are. With on-target solutions—regardless of capacity, speed and performance specs...it's a snap with Pertec.

Get together with Pertec peripherals: write Pertec, 9600 Irondale Avenue, Chatsworth, California 91311. Or call the Pertec regional sales office nearest you: Los Angeles (213) 996-1333. Ann Arbor (313) 668-7980. Hudson, New Hampshire (603) 883-2100. London (Reading) 582-115.

PCC PERTEC

a division of Pertec Computer Corporation

See us at NCC Booth 1415.

CIRCLE 21 ON INQUIRY CARD

DIGITAL TECHNOLOGY REVIEW

Expanded Computer Series Lowers Entry Cost and Increases Performance

Cyber 171 and 176 are medium and large scale additions to the Cyber 170 family from Control Data Corp, Box O, Minneapolis, MN 55440, which serve to lower cost and increase performance range. The 171, an entry level, medium scale system, and the 176, in a class with the largest commercially available equipment, share NOS operating systems and distributed network processing architecture with the other four models in the series (see *Computer Design*, June 1974, pp 26, 30), providing high levels of multiprogramming and multiprocessing support.

Architectural design of the 171 centers on the distributed processing concept. Input/output, system monitoring, and control are performed independently through a set of peripheral processing units.

The system can be configured with one or two central processors, each with an arithmetic unit having 24 registers. Instruction control section of the CPU directs all arithmetic operations and provides the interface between the arithmetic section and the central memory control unit. In large configurations, it also manages character manipulation activities of a standard compare/move unit, allowing movement of data characters from one memory location to another.

Central memory is available in five incremental sizes ranging from 65k to 262k 60-bit words. Organized in eight or 16 banks of interleaved storage to minimize access conflicts, the MOS memory includes single-bit error correction and double-bit error detection capability.

One or two peripheral processor subsystems direct operation of all disc, tape, card, printer, and display peripherals. Basic are 10 processors, each with 4k 12-bit words of memory supporting a repertoire of 64 arithmetic and I/O instructions.

The Cyber 176 incorporates technologies that differ from those of the other systems, but serve to enhance upward compatibility and improve price/performance and reliability. Central memory consists of high speed bipolar semiconductor elements and ranges from 131k to 262k 60-bit words in size. This is complemented by an extended memory subsystem with capacities of 0.5M, 1M, or 2M words.

Two architectural elements which contribute to central processor speed are its 12-word instruction stack and its nine independent functional units. Instruction words are read from central memory into the stack on a 2-word lookahead basis. After the 15- or 30-bit instructions are issued for execution, they flow through the remaining 10 words of the stack. If the program sequence is such that any of these instructions still in the stack are to be re-executed, they are issued from the stack, thereby reducing access time and minimizing memory references. An address register associated with each word in the stack allows noncontiguous sequences to operate totally from the instruction stack.

Instructions are issued from the stack at a maximum rate of one per system clock period (27.5 ns) to any of the nine functional units. Each functional unit is independent of the others, permitting significant parallelism of operation to occur. Additionally, most functional units are segmented (or pipelined) so that several operations can be at various stages of completion within a single functional unit.

A set of 10 to 20 peripheral processors drive the peripheral equipment and perform many system software functions. High performance peripheral processors are used to support high speed model 819 disc storage units. Available only on this model, the units each contain 400M data characters and have a transfer rate of approximately 40M bits/s. Concurrent operation of system elements and CPU, combined with ECL circuitry, provide performance 18 times that of the 171.

Configured with hardware and software to support entry-level timesharing requirements, a basic Cyber 171 can be purchased for $790,778. This system includes central processor, 65k memory, disc and tape subsystems, 18-05 remote batch terminal, and communications hardware. A typical 176 with 196k-word main memory, 524k-word extended memory, disc, tape, printer, and card equipment to support high speed batch processing has a price of $6,969,475.

Circle 150 on Inquiry Card

Distributed Systems Integrate Data Collection and Process Control

Distributed plant management system (DPM) offers both factory data collection and process control in an integrated network. The system comprises factory data collection terminals, local and remote process monitor and control subsystems, and a data link that serves as a common data path between host computer and remote stations. System components are designed to promote management efficiency by enabling single source reporting of management information, large reductions in wiring expense for remote stations, and simplified installation of total systems.

Digital Equipment Corp, Maynard, MA 01754 plans a phased introduction of the components over the next 18 months. Phase 1, with deliveries in October, includes DPM 60 and 80 host systems based on the PDP-11/34 and -11/70 computers. Other components are three user-oriented factory data collection terminals; IP11, a local measurement and test subsystem, for interfacing I/O modules with the PDP-11's UNIBUS™; and DECdataway™, an inexpensive data link for interconnection of a host with remote collection points up to 15,000 ft (4.6 km) distant.

A basic DPM 60 configuration would include an -11/34 processor with 192k bytes of main memory, floating-point arithmetic, RK05 or RK06 cartridge disc drives, and two serial bus ports. Typically an 80 series would have an -11/70 processor with 256k bytes of memory, floating-point arithmetic, RK06 or RP06 disc pack drive, and four data link controllers. Both systems are supplied with COBOL and FORTRAN IV languages running under the RSX-11 operating system.

Terminals for use with the system are time and attendance station RT-801 for employee exit/entry recording; this wall-mounted unit includes time of day display and badge reader. A basic work-station, RT-803, includes card and badge reader, alphanumeric display, numeric keypad, one transaction key, and five function keys for single activity reporting. An area work station (RT-805), for entry of transactions and values, accepts punched cards, marked cards, and plastic badges. It features 12-key nu-


The system builder's sensible display.
Everything you need and not one piece more.
Tektronix

We've combined refresh with storage in a new modular graphics display.

You build from there.

Suddenly state-of-the-art display technology comes built for the OEM.
Tektronix' new GMA display modules let you integrate into your system our most impressive display capabilities ever. Including refresh and storage graphics in one tube. Complete character and vector generators. Big 19" screen and fine resolution.

It's exactly what you need, because you can specify exactly what you want. Order CRT and power supply only, or select from a range of performance and packaging options in our extensive product line.

You can integrate other products from our graphics family, like hard copy modules. Or talk to us about other special product configurations, like our 11" storage-only components.

No other package lets you pick such comprehensive graphic display capability at anywhere near the price.
It figures, because Tektronix has been the worldwide low-cost graphics leader for years. No matter what unique and unusual systems you're working with, we can help with manufacturing flexibility, engineeering assistance, and a passion for excellence.

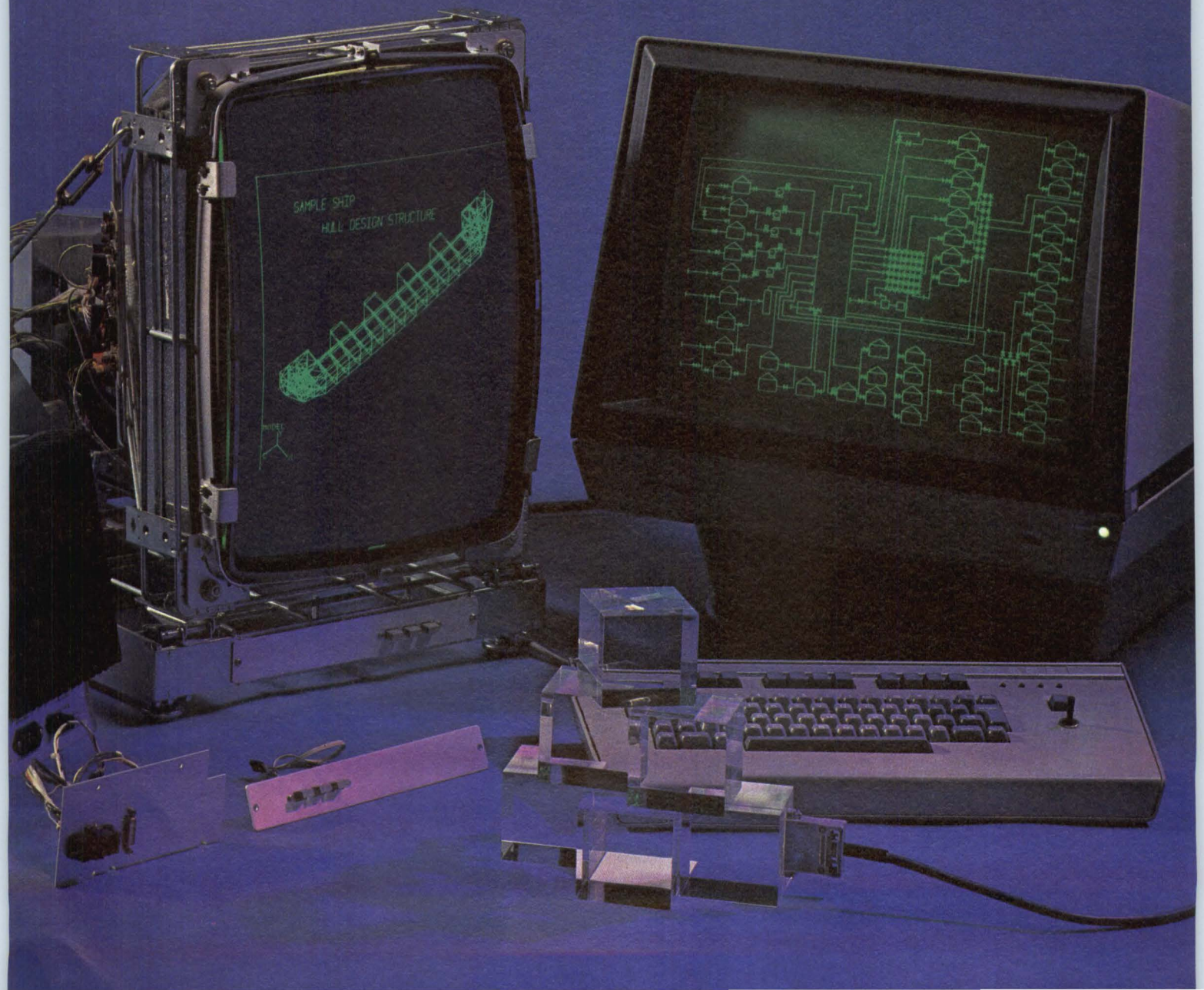
Get capability you can build with. From a supplier you can work with. Get your Tektronix OEM Sales Engineer on the phone today. Or write us for more information.

Tektronix, Inc.
Information Display Group
OEM Components
P.O. Box 500
Beaverton, OR 97077

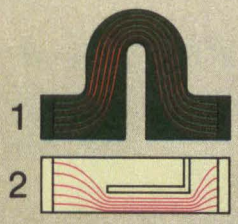
CIRCLE 22 ON INQUIRY CARD

Tektronix OEM components: the perfect fit.

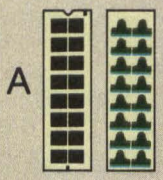
Tektronix®
COMMITTED TO EXCELLENCE



A revolutionary idea. Stackpole "top-hat" networks prove you can get more resistance on less real estate.



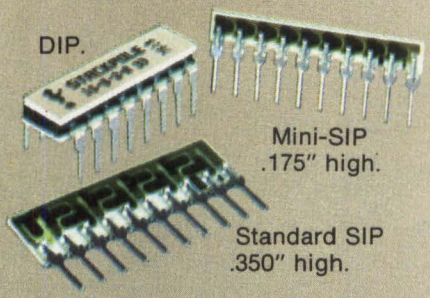
Compare (1) our "top hat" to (2) a standard "L"-cut and you see why ours dissipates more heat, faster. On a much longer resistance path.



(A) Standard thick-film networks have more hot spots, current crowding higher capacitance than (B) our "top-hat" network.

Flip our network's lid and you can see why. It's revolutionary.

The more our unit is trimmed, the better your resistance. So ratings of 200 watts/in² are very realistic.



The secret is in the simple laser cut in the middle of each "hat." In this and its horizontal geometry you get lower capacitance without hot spots, current crowding, or the other power-robbing things built into conventional networks.

Now you can get equal resistance in less space. Or greater resistor network performance in the same space.

We're out to tip our "hat" to you. With a full range of values, tolerances, sizes. In single or dual in-line networks, custom designs and even mini-SIPs that are only .175 inch high.

Ask for a free sample of a revolutionary idea. Stackpole Components Company, P.O. Box 14466, Raleigh, N.C. 27610. (919) 828-6201.

STACKPOLE

The revolutionary resistor people.

CIRCLE 23 ON INQUIRY CARD

meric keypad, eight transaction keys, guidance panel, and alarm. All are ruggedized for use in factory environments and offer block mode communication for high throughput and data integrity.

Central to each system is the DECdataway, a 2-conductor twisted cable extending more than 15,000 ft from the host computer. The 56-kHz line serves as a bidirectional data path for host and up to 63 multidrop nodes in a factory environment. A data link controller manages data handling and bus protocol through firmware, relieving the host processor. Because each device address is contained in the interface, the data link permits true position independence for all remote devices, allowing them to be freely interchanged or moved to other locations in the factory.

During phase 2 (early 1978), a terminal concentrator for connecting keyboard video display and hardcopy terminals to the data link is planned. Future releases will include intelligent microcomputer-based subsystems with digital and analog I/O capability for remote monitoring and process control, and transaction processing software for development of factory management applications.

Circle 151 on Inquiry Card

Relays Achieve Time-Delay Function With Hybrid Module

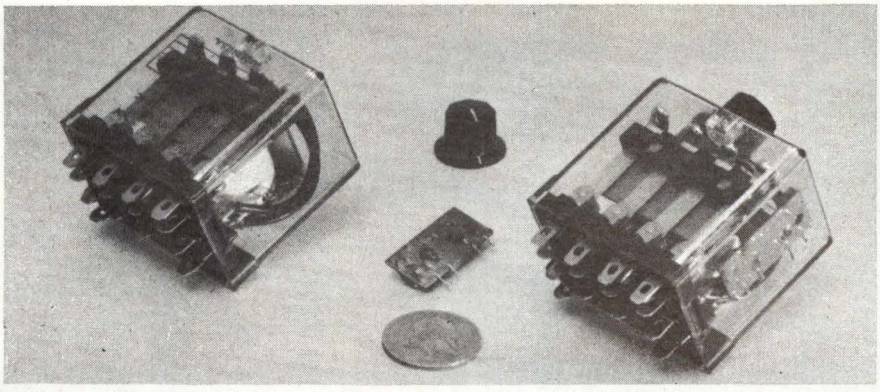
Virtually every line of relays produced by Struthers-Dunn, Inc, Pittman, NJ 08071 is now available with an integral timer function. The preset or adjustable function is achieved by adding a solid-state device called a hybrid thick-film module to standard relays. This module can be incorporated as an integral part of any relay to form an inexpensive, reliable time-delay relay. In most cases, the timing module fits within the existing relay cover, and does not affect unit size or ease of mounting.

Expected to have a major impact on machine tool controls, energy conservation systems, and the development of consumer products, the TDRs will cut costs in applications that currently use a conventional electromechanical timer and a separate relay. In this application the designer can use a single component, cutting that cost almost in half, and at the same time reduce the cost of mounting and wiring the components. Other advantages are that there are no motors to wear out, no clutches to slip, no actuators to come loose, and no grease in gear trains to solidify at low temperatures. Users can attain high packaging density and a wide range of ac and dc voltages.

Offered in some 6000 different relay configurations, the units are basically standard general-purpose relays with an electronic module wired to the coil circuit to provide a time function. The electronic module is a 4-terminal encapsulated device, small enough to be attached to most relays without increasing the relay package size. Fixed TDRs (non-adjustable) require only the module and the relay and are completely interchangeable with the basic relay.

If needed, the delay period can be remotely adjusted over a 10 to 1 range by a 1-MΩ potentiometer on the front panel of the control console. However, the most common unit consists of the relay in its standard case with an added solid-state module and integral potentiometer. Unlike conventional timers, the units are available in any ac or dc voltages normally used in relay applications. Preset time intervals range from 0.1 s to 5 min; adjustable models can be set for a similar range of times.

Circle 152 on Inquiry Card



A solid-state, hybrid thick-film timing module (center) is incorporated into standard relays to form a time-delay relay. The function, available on virtually every line offered by Struthers-Dunn, fits inside existing relay cover and does not affect unit size or ease of mounting

Scientific Processor Performs Processing and System Management

Going beyond 'super computers' that only perform high speed mathematical processing, the Burroughs Scientific Processor (BSP) employs a large-scale B 7800 as its system manager, to provide automatic management capabilities for controlling the entire system's operation. Introduced by Burroughs Corp, Detroit, MI 48232, the system performs numerical computations at up to 50M operations/s and has sufficient capacity to handle massive and time-critical applications. In addition to economic benefits derived from simultaneous scientific computation and general-purpose data processing, the system provides a degree of automatic self-regulation and simplicity of operation believed to be unique in the "super computer" class.

The system uses multiple processing units operating in parallel. This arrangement constitutes an array processor architecture which enables large vector-oriented problems to be solved at very high speed. To achieve the operating speeds necessary to make its architecture fully efficient, the system incorporates an LSI circuit implementation of Burroughs Current Mode Logic (BCML), and makes extensive use of charge-coupled device (CCD) circuitry.

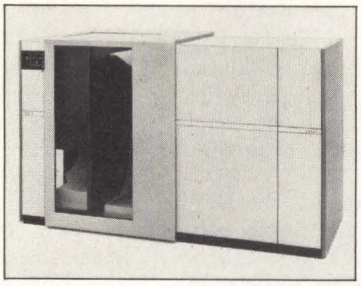
Three asynchronous sections make up the balanced system: control processor, multi-element parallel processor, and file memory. Operating at 12 MHz, the control processor has two principal functions. It acts as the interface for transfer of supervisory information from the system manager, and controls the parallel processor and file memory.

Consisting of 16 arithmetic elements, 17 memory modules, and an

New data-hungry peripherals from Siemens

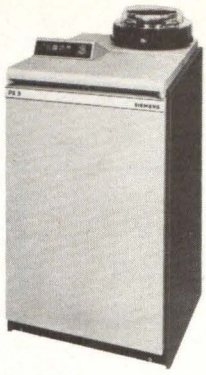
For OEM requirements demanding high throughput from reliable I/O devices, Siemens introduces the data-hungry peripherals.

Siemens ND 2 is the ultimate in hardcopy peripheral systems. It uses a laser and electrophotography to print up to

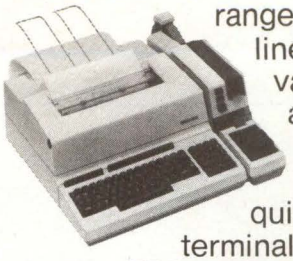


21,000 lines/min. on plain paper, and outputs approximately 8,800 12-inch sheets/hour. A forms overlay feature, that eliminates the need to preprint computer paper, is available.

The life of ND 2's photoconductor drum is an unparalleled three million copies...and the drum is user replaceable.



Siemens PS 5 disk storage drive, with an average positioning time of 23 ms, is expandable from 72 to 144 to 300 to 500 MB without cabinetry changes. Users can upgrade easily and your parts inventory stays small. The PS 5 is extremely rugged and reliable with a proven MTBF of 2500 hours, including the first hour of operation. At 500 MB it's the largest capacity disk unit available and the most economical per MB.



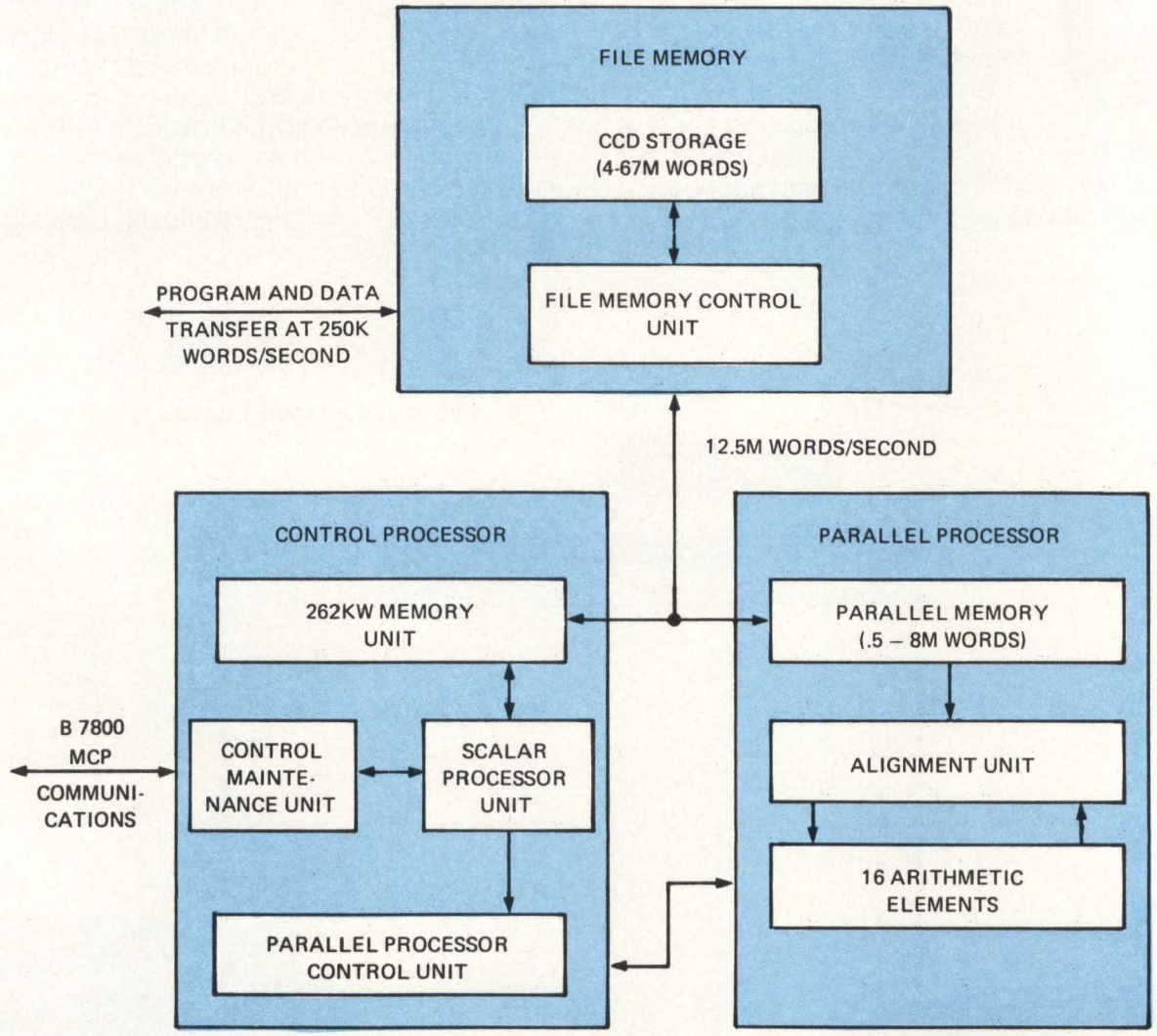
The PT 80 terminal features printing speeds of 30 to 90 characters/second and a range of 72 to 132 characters/line. In addition, it offers a wide variety of type faces and the ability to adjust to all common paper sizes.

Its compact design and quiet operation make the PT 80 terminal ideal for use in offices, banks, EDP centers, etc.

To learn more about how Siemens can satisfy your growing data appetite, call or write Richard Mizrahi, Siemens Corporation, 3 Computer Drive, Cherry Hill, N.J. 08034 (609) 424-2400.

SIEMENS

CIRCLE 24 ON INQUIRY CARD



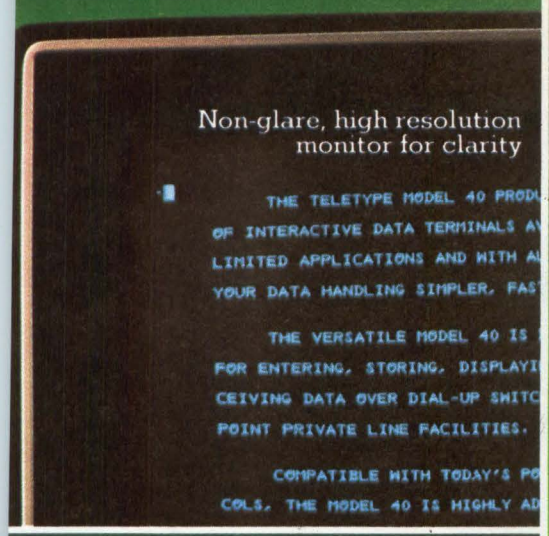
Utilizing multiple processing units operating in parallel, Burrough's Scientific Processor is capable of solving large vector-oriented problems at very high speed. LSI circuit implementation of current mode logic and extensive use of CCD storage technology achieve operating speeds which make the architecture efficient

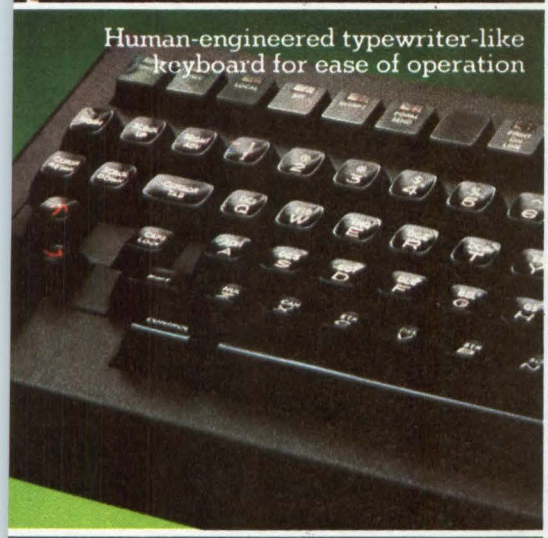
alignment unit, the parallel processor performs vector-oriented computations. It operates on data loaded into its memory modules under control of the control processor. Arithmetic elements operate in lock step, all executing the same instruction on distinct data values at the same time. Operating at 6.25 MHz, the elements complete most operations in two clock periods; for example, the processor can perform 16 floating-point multiplications every 320 ns.

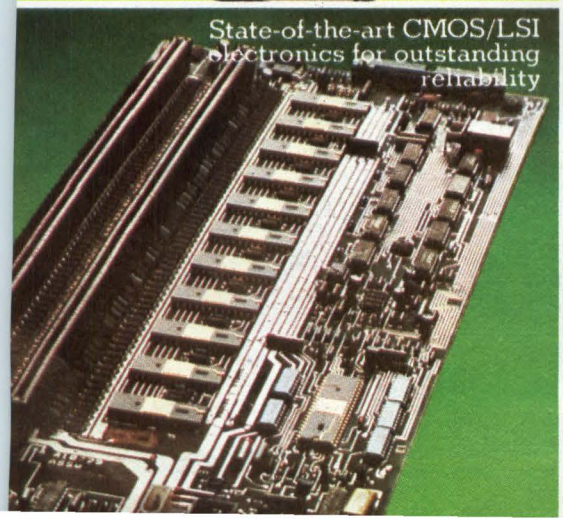
File memory is composed of CCDs and has a 500-μs access time, 75M-byte/s transfer rate, and basic capacity for 4M words, expandable to 67M words. It is loaded with tasks and data files through a channel connecting it to the system manager's I/O processor; once a task is initiated, code files are transferred to control processor memory, and data arrays are transferred to the parallel processor's memory. File memory serves as the overlay device for files and arrays that exceed the processor's memory capacities.

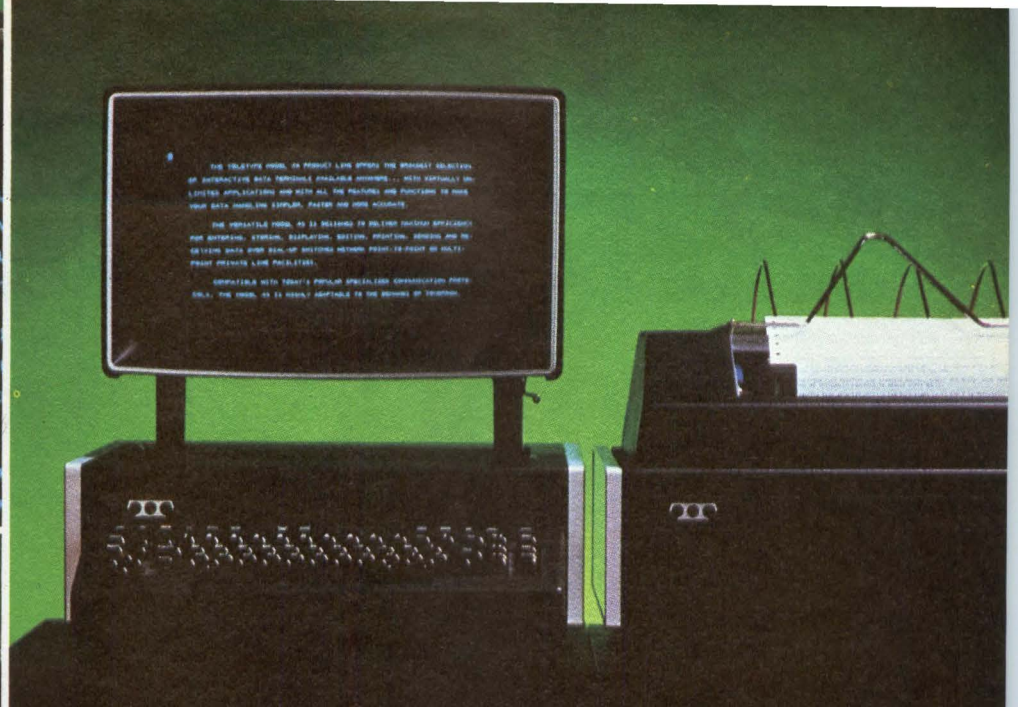
Three models of the system will be available: the basic BSP, using the B 7800, and the BSP/7811 and BSP/7821, which include large-scale 7811 and 7821 computer systems as the system manager. The processor is being developed at the Burroughs' Great Valley Laboratories. Customer deliveries are expected to start in 1979.

Circle 153 on Inquiry Card









THE MODEL 40 IS SO GOOD, NOTHING EVEN COMES CLOSE. AND WE CAN PROVE IT, COMPONENT BY COMPONENT.

We're convinced the Teletype® model 40 product line matches—if not exceeds—any data terminal system on the market today. Because on a cost/performance basis, nothing even comes close.

The 40 printer, using a unique design, is incredibly dependable. And its CMOS/LSI drive electronics are so advanced and compact, they fit inside the printer itself on a single circuit card.

Our keyboard is anything but ordinary, too. Naturally, all controls are grouped according to function. But more importantly, the entire unit is human engineered to provide the most in throughput. Not only do the keys impart a typewriter feel, they're also contoured to the shape of the operators' fingers.

We admit we could have cut corners when we designed and built our display tube. But good enough wouldn't have been good enough. So we used a glare reducing screen. Even the display type is specially designed for legibility, with a flicker-free refresh rate of 60 times/second. Character separation and clarity are insured by a large 7 x 9 dot matrix. And the whole unit tilts through 20° for the best viewing angle.

As good as the individual components are, added together they put the model 40 product line in a class by itself. For more information, write or call: Teletype, 5555 Touhy Ave., Skokie, IL 60076. Phone 312/982-2000.

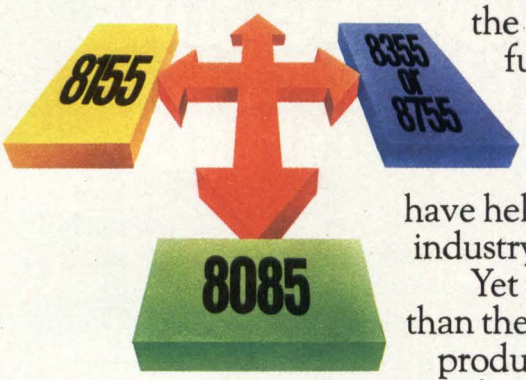
TELETYPE

CIRCLE 25 ON INQUIRY CARD

Intel delivers a unique the 8085. It's like the

Introducing the 8085, a unique new microcomputer that is part of a new Intel® microcomputer system—the MCS-85.™

The 8085 is both software and bus compatible with the 8080. So you can take full advantage of the wealth of software, peripherals and development tools that have helped make the 8080 the industry standard.



Yet the 8085 is 50% faster than the 8080. So your 8085-based products will enjoy a new level of performance at even lower cost.

All components in the MCS-85 system have higher level integration, making it possible to replace a 10-chip 8080 system with three MCS-85 chips. Components of the MCS-85 system include the 8085 CPU, the 8155 256-byte RAM with I/O and timer, and the 8755 16K EPROM with I/O and interchangeable 8355 ROM with I/O. All these components, including the 8755 EPROM, operate from a single +5V TTL supply enabling you to go from prototype to production without board or power supply changes.

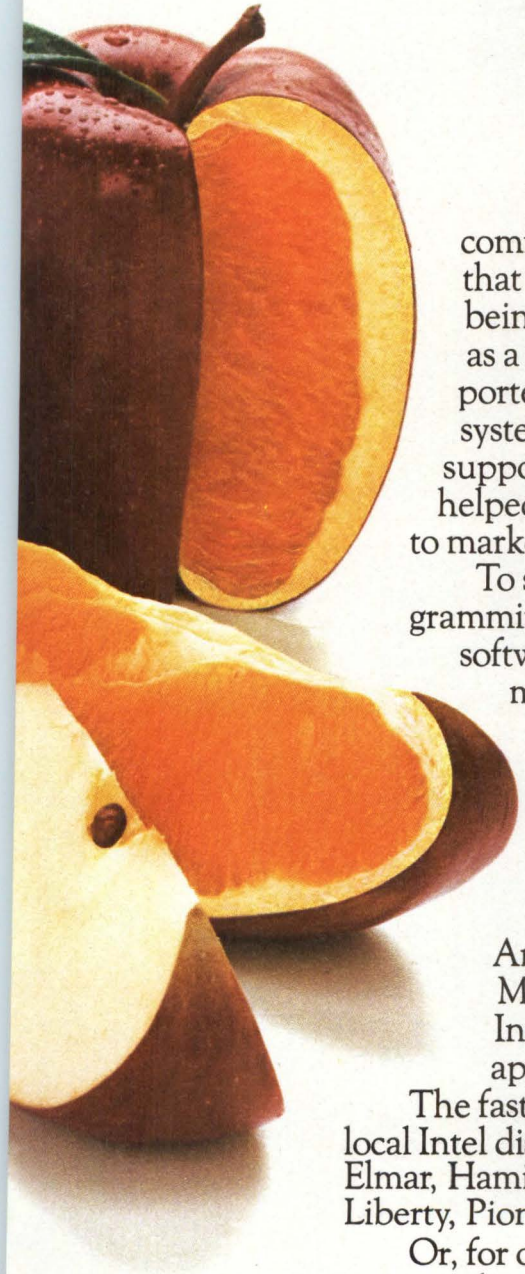
It all adds up to faster, easier, more economical—and better—system design.

The 8085 is more than a faster, more efficient microcomputer. It's the newest example of Intel's total system commitment. Here's what that means for existing 8080 users and new microcomputer users.

Because the 8085 is fully compatible with 8080 software and 8200 series peripheral components, it protects your investment in existing designs and allows you to implement new designs without starting the development cycle all over again.

And now you can design your 8085 and 8080 systems around four new advanced peripheral controllers: the 8271 Floppy Disc Controller, the 8273 Synchronous Data Link Controller, the 8275 CRT Controller and the 8279 Keyboard/Display Interface. Like the other 8200 series peripherals, these new devices are fully programmable, single chip solutions to system interface requirements.

new microcomputer, 8080. Only better.



Intel's total system commitment means that the MCS-85 is being introduced as a fully supported, complete system. All the support that has helped 8080 users get to market sooner now gives 8085 users a head start too.

To speed programming we provide PL/M, the high level programming language for microcomputers that can cut months off software development. The Intellec® microcomputer development system, with ICE-85™ in-circuit emulation and symbolic debugging, helps reduce system integration and debug time. Then there's application assistance worldwide. Training classes and seminars to help you get the most from the MCS-85 system. And a comprehensive development software library at your disposal.

Total system commitment. It protects your investment. And gives you the jump in a competitive world. Because MCS-85 is a complete and fully supported system, comparing Intel with any other microcomputer supplier becomes an apples to oranges comparison.

The fastest way to get started is to order MCS-85 products from your local Intel distributor. Almac/Stroum, Component Specialties, Cramer, Elmar, Hamilton/Avnet, Harvey Electronics, Industrial Components, Liberty, Pioneer, Sheridan, L.A. Varah, or Zentronics.

Or, for our detailed MCS-85 brochure, use the reader service card or write us directly. Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

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Circle 27 for technical information and a demonstration.

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CIRCLE 29 ON INQUIRY CARD

Laboratory Recorder Uses Microprocessor For Tape Handling Functions

SABRE X, in addition to recording and reproducing a wide range of analog or digital signals, handles tape in many modes and monitors its own operating points. An all-band laboratory magnetic tape recorder/reproducer, the unit may be configured with 0.5 or 1" heads and may contain up to 32 tracks of dual channel electronics. All channel electronics are completely interchangeable within the system and capable of IRIG bandwidth changes without manual change of components.

Sangamo's Data Recorder Div, PO Box 3347, Springfield, IL 62714 built into the system capability for 10 speeds of operation from 240 to 15/32 in/s with signal electronics electrically switchable for all speeds. Direct, FM, or HDR electronics may be used in any combination to ensure maximum flexibility. With 1-mil tape and 16" reels at 15/32 in/s, nearly 89 hours of continuous recording or reproducing time can be attained from a single tape. The unit accepts 10.5, 14, 15, or 16" reels, and can use 0.5 or 1" tape.

Microprocessor-controlled tape handling capabilities enable end of tape and shuttle modes to be programmed to meet specific applications. Beginning and end of data points are entered directly from the control panel and the points are stored in microprocessor memory, allowing shuttle action to occur between the two points automatically. Variations to the standard shuttle sequence that may be programmed include automatic record/reproduce in both directions, sequential record/reproduce, and two systems alternately recording and rewinding for operation without loss of data from a continuous data source.

Tape drive system consists of a low mass capstan operating in conjunction with a vacuum-tensioning subsystem, thus eliminating the need for tension arms and pinch rollers. Tape speed is accurately controlled by coupling a quick response servo system to a capstan motor. The servo compares a crystal oscillator reference to one of two speed-dependent signals for frequency and phase relationships. One of these signals is generated by a tachometer, mounted within the capstan motor resulting in a tape speed accuracy of ±0.10% of nominal tape speed. The second signal may be reproduced from tape for tape speed accuracy of ±0.001% referenced to record speed.

Circle 154 on Inquiry Card

Multiple Workstation Computer System Uses 2-Sided Diskettes

System/34 is a disc-oriented system that supports multiple workstations, consisting of display station and tabletop character printing units, and allows display system operators to execute the same or different programs concurrently with other batch or workstation-oriented programs. With the system, International Business Machines Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301 also announced the 5251 display station, a CRT display with keyboard; 5256 printer, a tabletop matrix printer; 5211 printer, a standalone line printer; and Distributors Management Accounting System II (DMAS II), an application program designed to provide online billing, inventory control, accounts receivable, and sales analysis.

The 5340 system unit contains CPU, diskette drive, disc storage, and workstation controllers. Multiple processors/controllers in the CPU are capable of operating in parallel. The main storage processor directly executes most instructions stored in main memory. A microprocessor supports a portion of the supervisor program and I/O control and controllers are used to drive specific I/O devices. 32k, 48k, or 64k bytes of MOSFET memory has 600-ns storage time. LSI and MSI circuitry form the logic.

Either 1- or 2-sided removable diskettes are supported by the diskette drive. When double-density, double-sided diskettes are used, the unit stores up to 7696 records in basic format or 9472 128-char records in extended format. A nonremovable disc store functions as the prime processing file, and provides 8.6M, 13.2M, or 27.1M bytes of capacity, with average access time of 40 ns and data transfer rate of 889k bytes/s.

Workstation controller allows direct attachment of up to eight workstation devices—one within 20 ft (6 m) of the CPU, and the others at a maximum distance of 5000 ft (1524 m). All keyboard polling is done by the controller without CPU interference. Keyboard depressions are handled stroke-by-stroke; screen buffering for each station is up to 127 fields.

The cable connected keyboard of the 5251 display station has familiar typewriter layout, with a 10-key proof keypad and system function keys. Display consists of 1920 u/lc characters in an 8 x 16 dot matrix. Twin axial cabling provides capability to wire each display station directly to the controller or to short-wire one or more stations to each other in a cluster and long-wire the whole cluster to the controller.

A tabletop bidirectional serial printer that uses an upper/lower case 96-char set with a 4 x 8 dot matrix, the 5256 provides 40, 80, or 120 char/s. Attached to the system via a 20 ft (6 m) cable, the 5211 is a standalone, separately powered, 132-col line printer that provides 160 or 300 lines/min with 48- or 64-char set. Operation is fully buffered under direction of the printer controller.

Both SDLC and BSC data communications capabilities are supported to allow communications with other systems. The system support program (SSP) is designed to handle a multiprogramming workload.

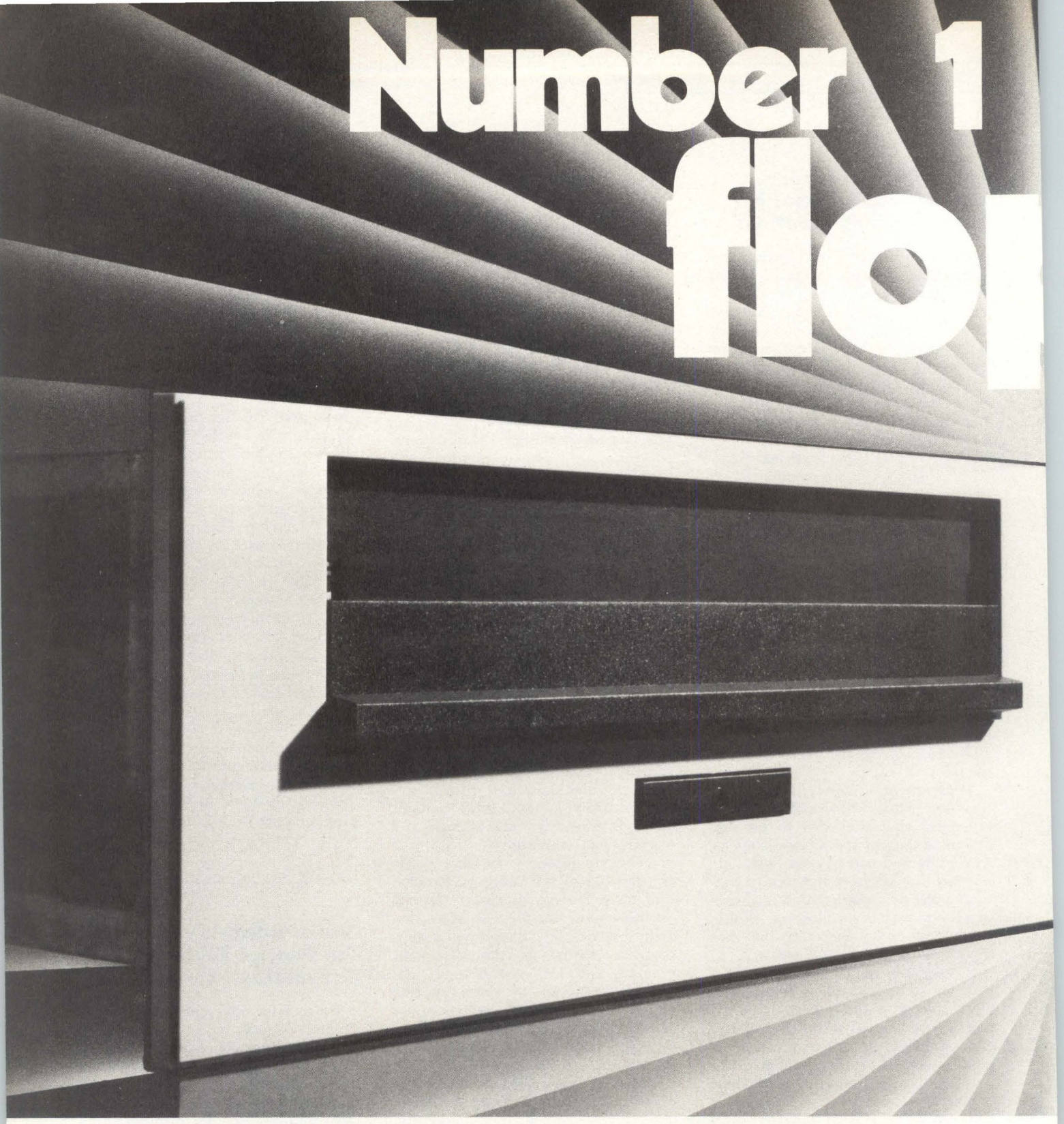
Circle 155 on Inquiry Card

Pressure-Sensitive Termination Replaces Conventional Connectors

A concept for interconnecting flexible printed wiring type of flat cable without using conventional connectors approaches the problem with a pressure-sensitive termination that integrates the pluggable interconnection into the cable manufacturing process. Called the Gold Dot interconnection system, it utilizes gold "buttons" plated directly onto the flat flexible circuitry that is to be connected to a standard PC board conductor pad.

According to James E. Wittmann, military products manager for the Connecting Devices Div of Hughes Aircraft Co, 17150 Von Karman Ave, Irvine, CA 92714, the concept meets changing technical and economic requirements of airborne electronics sys-

Number 1 flo



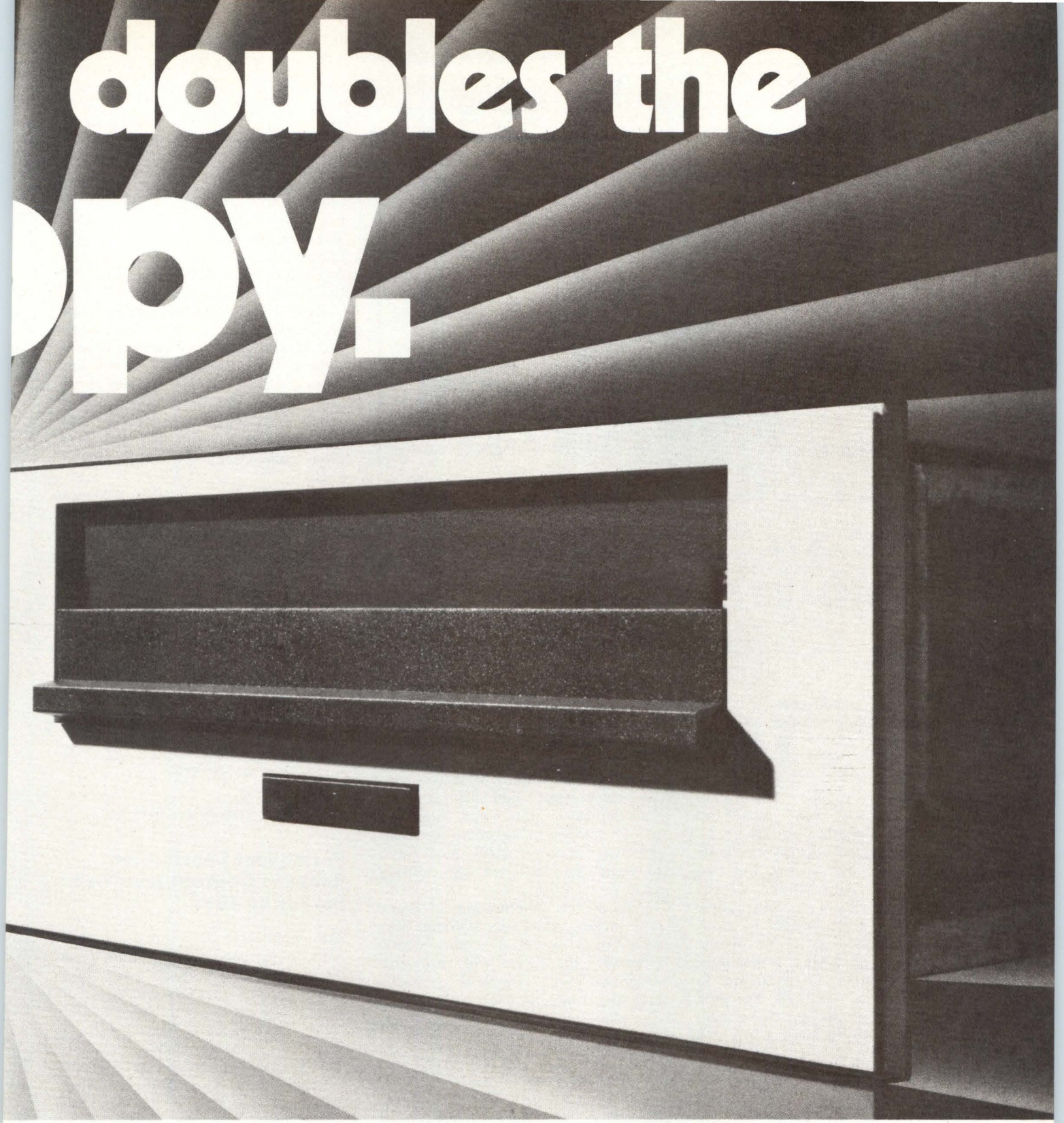
Doubled data storage capacity. Doubled access speed. Doubled floppy media selection. Get it all with the new Shugart double-sided single/double density floppy disk drive. All this for only 25% more than a single-sided floppy.

Data. Data. The new SA850 double-sided floppy packs twice as much data as a standard unit—up to 1600 K bytes (unformatted). Yet the SA850 is identical in physical interface, mechanical outline and package size to the industry-standard—our SA800/801. It's plug-compatible, cabinet-compatible.

Faster. Faster. Access time is more than twice as fast. The SA850 moves from track-to-track in 3 milliseconds, with an average access time of less than 100 milliseconds. The secret is a proprietary Fasflex™ actuator that delivers positive, low-friction head movement.

Media. Media. One drive reads and writes them all. Single or double density. Single or double-sided disks. Industry standard diskettes and IBM Diskette 2, too.

Features. Features. The head carriage assembly allows loading of the two read/write heads simultaneously on both sides of the disk. (No more head load pads!)



Plus this head can be replaced without an alignment disk, scope, or special tool—and it's totally self-aligning.

Lower heat dissipation and better PCB packaging promise even better reliability. A new I/O controlled programmable door lock strengthens data security.

And there's more, more. So before you look at another floppy, see the SA850 twice. See it in our brochure. Then watch it perform in a demonstration with your own system.

The SA850. The doubled floppy from number 1.

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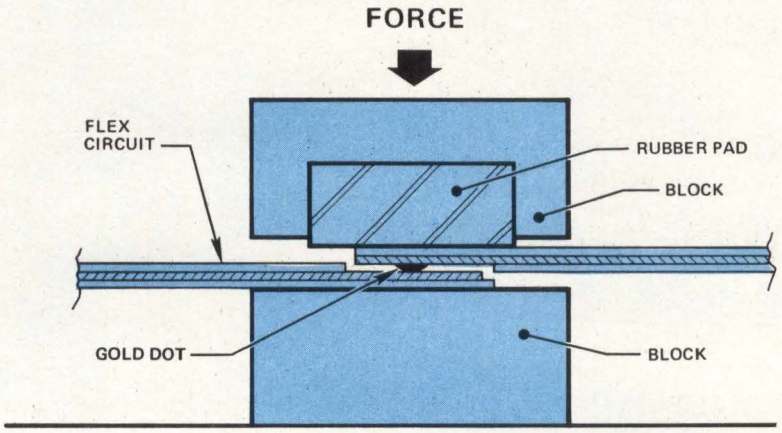
Number 1 in low cost disk storage.

Shugart Associates®

CIRCLE 30 ON INQUIRY CARD



Gold buttons plated directly on circuitry to be connected to a standard conductor pad form the basis of Hughes Aircraft's pressure sensitive termination technique. Planned for use in high density wiring systems, the concept uses a simple clamping force to join two mating faces and produce a gas-tight joint

tems. Replacing conventional "friction mating" contact interfaces such as the standard pin socket or blade tuning fork variety, it can be used in high density wiring systems to connect/disconnect flex circuits to flex circuits and flex circuits to printed wiring boards.

The technique utilizes a simple clamping force for joining the two mating faces. Application of the proper force causes a microscopic layer of the gold button to flow, filling in irregularities in the mating surfaces and producing a gas-tight joint. Approximately 5 to 10 mils in diameter by 1.5 mils thick, the gold buttons are deposited on the circuit, using a proprietary plating process, in a pattern identical to that of a PC board. Necessary pressure is created by tightening an engagement screw until the pressure plate butts against the PC board. A silicon rubber compression pad assures even distribution of the force and acts as a spring to maintain constant pressure. Stainless steel pins serve to align and polarize the mating surfaces.

The contact juncture can be made and broken repeatedly without degradation. Absence of wiping action eliminates the severe wear problems associated with standard contacts, and the contacts' high static force can penetrate resistive surface films.

Circle 156 on Inquiry Card

Disc Cartridges Use Single-Function Handle to Reduce Costs

A System 3 disc cartridge offers improved durability and ease of operation in addition to reduced weight and cost. Designed by Nashua Corp, Computer Products, Nashua, NH, the unit incorporates a single-function handle and an efficient disc holding device which ensures a smooth uniform pull across the cartridge when opened and provides an effective seal when closed.

In an effort to reduce cost while improving reliability, a study was made to determine how disc cartridges were actually used and what problems were encountered in use. Although the traditional double-function handle was designed to allow users to carry a cartridge by the handle without accidentally opening the unit, it was discovered that they were seldom carried by the handle; rather they were held under the arm. This negated the need for the complex handle, allowing it to be replaced by the single-function handle. The user can open the unit by simply raising the handle, instead of the raise and slide action required by the double-function unit.

Further simplification removed operational problems encountered with the double-function handle. Loose screws often caused a disc to improperly align on the computer drive unit; the latch and internal spring mechanisms could break, making disc removal difficult; and dirt and dust often gummed up the handle mechanism.

The redesigned handle achieves low cost, durability, and reliability through the use of LEXAN® polycarbonate resin to form internal parts. The resin, from General Electric Co's Plastics Div, Pittsfield, MA, provides sufficient dimensional stability and overall toughness for use as mechanical parts, permitting the 12 metal parts of the original design to be replaced by three parts molded of the resin. This provides significant savings in cost and weight and, through the reduction in parts, a higher level of durability.

Circle 157 on Inquiry Card

Permanent Lubrication Reduces Contact Insertion Forces By 40%

Now applicable to a range of contacts, a permanent lubrication technique increases contact wear life, significantly reduces insertion and withdrawal forces, and has potential for a "more perfect" contact surface —all in a cost-effective manner. Gold-plated hermaphroditic contacts with graphite coatings produced using this technique bridge the gap between pin and socket and zero entry-force connectors.

Where organic or liquid lubricants have sometimes been used to reduce insertion force, they are not permanent and evaporate with time or at elevated temperatures. To solve this problem Amp Inc, Harrisburg, PA 17105 developed an approach that uses all solid material and involves solid-state bonding of lubricant to contact surfaces. This permanent lubrication can actually improve the surface properties of gold.

(Continued on p 55)

Data General. A la carte.

Now, you can buy our DASHER™ terminals, even if you don't own a Data General computer system. Select our fast impact printer and our user-oriented video display. Both are interface-compatible with any standard computer system.

Choose either 60 or 30 cps versions of the DASHER printer, which has a standard typewriter keyboard, u/l case, 132 columns.

DASHER display features a 1920 character screen, u/l case, convenient detached keyboard, programmable function keys, and a monitor that tilts and swivels.

Just as DASHERS' features make them easy to use, their attractive appearance makes them easy to fit into any environment. And of course they are solidly reliable and easy to maintain, a Data General trademark. For more details call your Data General sales office or nearest independent supplier of Data General terminals. Or send the coupon. Even a bit of Data General in your computer system is better than none.

Send details on ☐ DASHER printers ☐ DASHER displays
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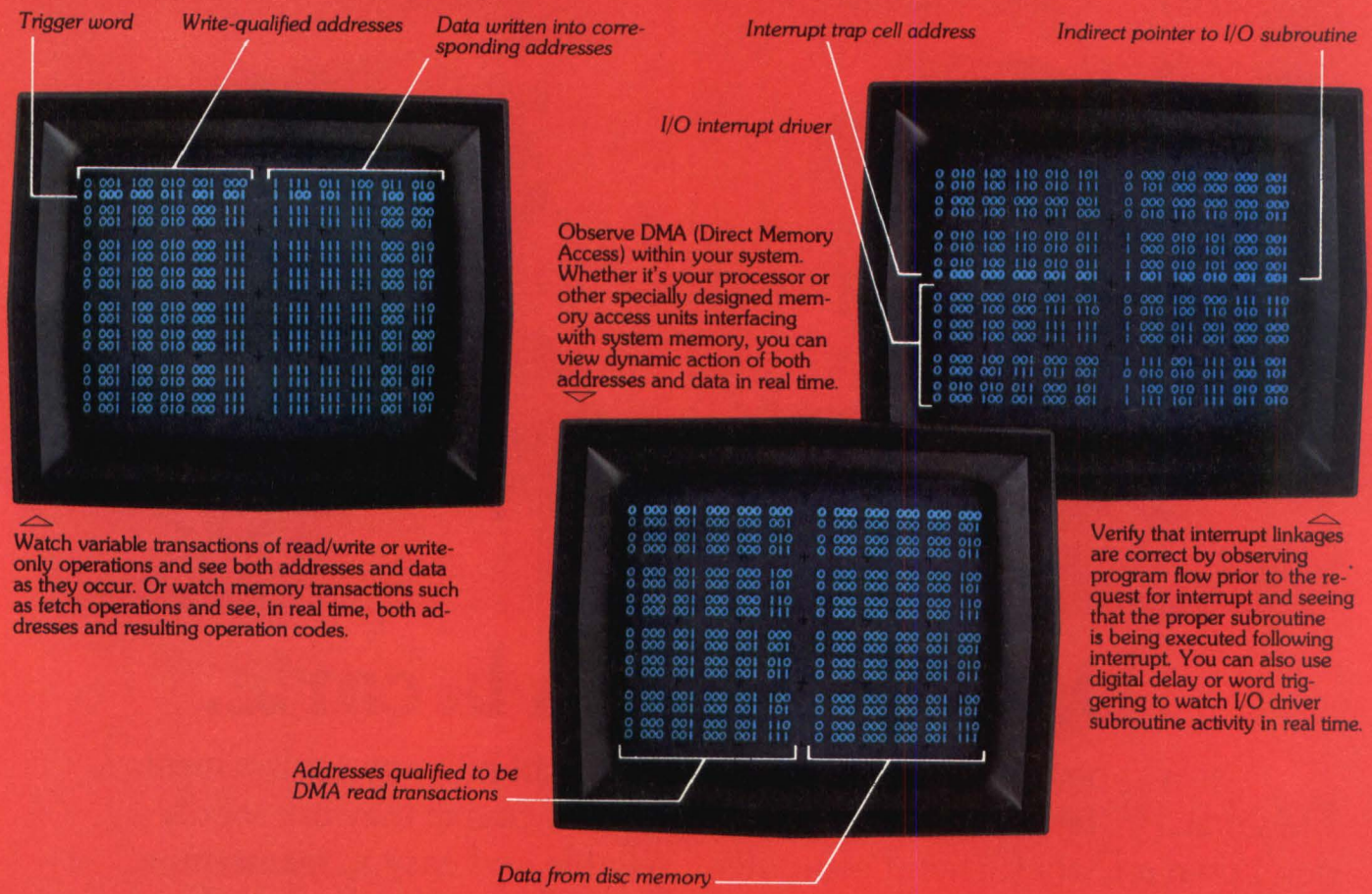
CIRCLE 31 ON INQUIRY CARD



If you're designing minicomputer based systems,

only HP Logic State Analyzers show you real time like this.

Logic State Analyzers effectively put you inside your operating minicomputer system for faster design and debugging. Here's the difference HP's real-time view makes.

HP's 1600S Logic State Analyzer (priced at $7100*) plus 10254A Serial-to-Parallel Converter (priced at $975*) gives you a better way to spot and diagnose intermittent system operation. They give you greater insight for better understanding of your system's capability. The combination can mean earlier product introduction, lower development costs, a faster return on the development investment.

Your local HP field engineer has all the technical details. Give him a call today. And also ask him about HP's FREE seminars—An Introduction to the Data Domain.

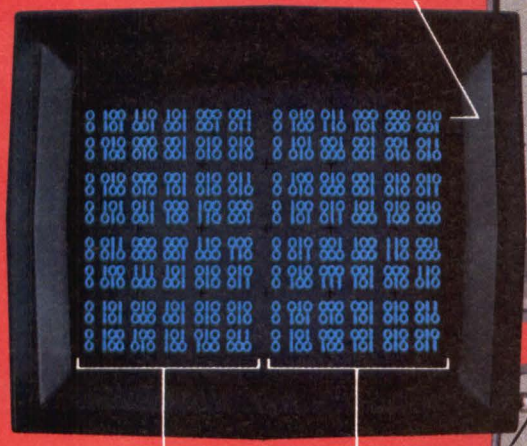
*Domestic U.S.A. prices only

Cursor

Dynamic real time photograph (time exposed) of incrementing counter used as system clock

Get a system overview with this memory map. It shows how your memory is being utilized in an operating program. If you know how your memory is organized, the map tells you at a glance what your program is doing and the relative time being spent in any one memory location. That makes it easy to spot things that shouldn't be happening, or to determine that part of your program isn't being implemented.

Disc address (cylinder, head, sector)



Parallel data inside computer

Serial data from 10254A

ASCII code

View I/O transactions in real time. Straddle an interface with the 1600S and you can evaluate handshake signals and compare input and output data directly—even if the clock rates differ and you're comparing serial data to parallel.

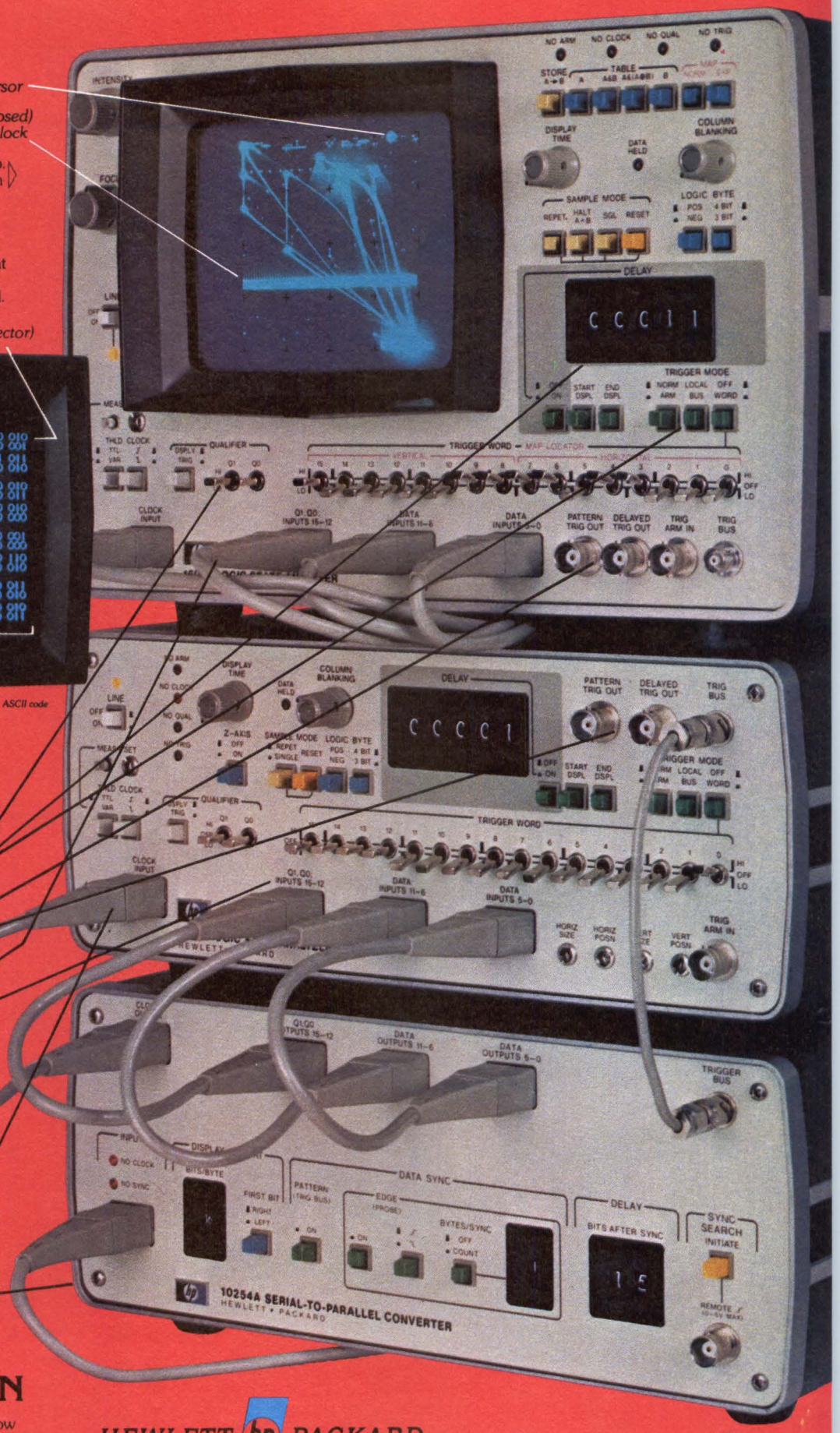
Qualifiers, *digital delay and various local or bus-triggering modes give you pinpoint selection of data flow for effective program tracing.*

Output triggers *drive your scope—at the right instant—for making electrical measurements in the time domain.*

Up to 32 channels *let you see all the action on a 16-bit system main bus plus 16 bits in the control section, I/O, or any other logic section in your minicomputer system.*

Dual clock *means you can easily relate bus activity to events occurring elsewhere at a different clock rate—in system peripherals, for example.*

Serial-to-Parallel Converter *(HP's 10254A) lets you directly view serial data in relation to parallel data on the system bus.*



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CIRCLE 32 ON INQUIRY CARD

Why Toggle?

(when you can turnkey)

Power-on-start means automatic program execution when computing with the Altair™ Turnkey Models from MITS. Both highly acclaimed Altair mainframes, the 8800b and 680b, are obtainable in easy-to-implement turnkey versions—offering the same capabilities as their full front panel counterparts—and then some.

Our 8800b Turnkey Model incorporates a Module Board complete with CPU, serial I/O channel, 1K of RAM, and provisions for 1K of PROM. All 8800 hardware and software are compatible with the 8800b Turnkey Model.

In addition to the 8800b Turnkey, we are introducing these new 8800 system peripherals. The Altair 88-AD/DA converter is our eight channel analog I/O system for applications where analog to digital and digital to analog conversion is necessary. For economical mass storage, the Altair Minidisk System (88-MDS) provides a fast access storage capacity of over 71K bytes per minidiskette.

A big computer in a small package—the Altair 680b Turnkey Model—is a low cost mainframe capable of home, business and process control applications. The 680b CPU module contains all the logic circuitry needed for immediate computing plus 1K of RAM, serial I/O port and provisions for 1K of PROM.

You may expand your 680b Turnkey with these new additions to the 680b line. Load and save programs on audio cassette with the 680b-KCACR. This inexpensive mass storage device is highly reliable under widely varying conditions and requires no circuitry adjustments. Interface your 680b Turnkey to the practical world of process control with the 680b-PCI. Monitor and compensate for changes in any operation, from tracking the sun to watering the lawn.

mits

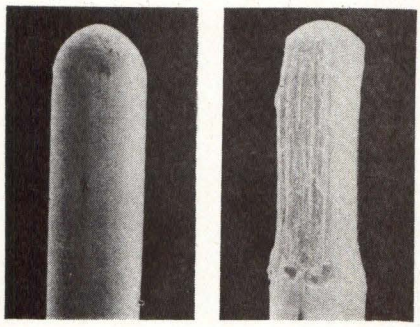
See all of these Altair Computer products and more at the MITS booth #1733, June 13-16 at the NCC in Dallas.

MITS 2450 Alamo SE Albuquerque, N.M. 87106

CIRCLE 33 ON INQUIRY CARD

Gold is too soft to use in pure form as a connector plating, thus it is used in combination with various hardeners and brightening agents. These elements, however, must be considered as impurities which detract from the nobility of the gold surface; permanent lubrication reduces the need for hardeners, permitting the use of pure gold. The ability to use as little as 50 μin of pure gold instead of the 200 μin currently being used provides another significant benefit because of the considerable savings achieved.

Graphite particles are applied to the surface of plated materials by spraying. When the fine graphite powder is projected against the surface with sufficient velocity, particles will shear and either adhere or rebound from the surface. If the contact surface struck by the particles is clean, a bond can occur. Once applied in this manner the graphite cannot be effectively removed by rubbing, handling, or cleaning.



Comparison of contact experimentally mated 2000 times illustrates benefits derived from Amp's permanent lubrication technique. Graphite coating on the pin on left has protected pin from wear, while conventional pin on right has been virtually destroyed

The resultant coating lowers the coefficient of friction at the mating surfaces. Since insertion or extraction force is related to the coefficient of friction and the normal force that is applied to the contact, high contact forces can be maintained with a lower coefficient of friction, thereby reducing the insertion/extraction force in connectors. It also improves the durability or wear life of the contact, allowing in some instances 50,000 mating cycles to be attained. This is achieved with a lower incidence of damage by dust and dirt than when using wet lubricants.

These desirable characteristics are accomplished with essentially no increase in contact resistance of the mating surfaces over that of untreated clean metal plating. Currently available on gold-graphite plated contacts, the lubrication will soon be offered on palladium, silver, and possibly on tin plating.

Circle 158 on Inquiry Card

Shorts Detection System Expands Capacity of PC Board Test System

An in-circuit test system designed to expand the capacity of installed functional PC board test systems, the L429 Shorts Detection System locates all shorts on a board. Because shorts frequently comprise the majority of faults on a board, their removal can improve the yield reaching board test, and can decrease the average time required to diagnose faults on each board. Major elements of the tester, developed by Teradyne, Inc, 183 Essex St, Boston, MA 02111, are shorts detector with system controller, and a board handler, which uses bed-of-nails test plates that the user builds up from fixturing kits.

To detect shorts, the system makes an electrical contact to each circuit stripe or component pad through the test fixture. The system can have up to 760 points of test electronics, and will test a board in less than 1 s. Each short will add 1 s for fault location and print out on a strip printer. Continuity tests are performed at a 200-mV level to a 10-mA current limit with a 3-Ω short point and a 15-Ω open point. Therefore, both active and passive components on the board under test appear as opens during testing.

With this capability, the unit detects all common types of shorts—solder blobs, slivers, and whiskers between stripes and pads, and internal shorts within semiconductors or passive components—but does not force enough current to turn on semiconductors or damage them. System controller provides the operator access to system controls, error-message printout, and self-test of the test plate.

Key feature of the board handler is the test plate that contains spring-loaded tulip-head probes. Each is assembled by the customer using a fixturing kit and a bare PC board as a template. The board handler provides the means for handling the board under test and making electrical contact. The handler will accept virtually any loaded PC board up to 14 x 17.5″ (35.6 x 44.4 cm) regardless of complexity or component mix, without platens or vacuum pumps. Only the test plate is changed for each individual board layout.

Circle 159 on Inquiry Card

Air Fireable Materials Cut Cost of Manufacturing Gas Discharge Displays

An air-fireable materials system for producing planar dc gas discharge displays, the Nicyl system eliminates the need for inert or reducing atmospheres, thereby lowering costs and simplifying the manufacturing process. Developed by the Electronic Materials Div of the DuPont Co, Wilmington, DE 19898, the thick film system includes Nicyl 9530 nickel electrode composition, silver conductor 7713 for glass seal feedthroughs, crossover dielectric 9740, and contrasting dielectric 9741. All compositions are designed for compatibility with soda lime glass substrates.

"Nicyl" nickel electrode composition 9530 has low resistivity, typically 50 to 60 mΩ/square/25 μm, depending on firing conditions. When properly processed, the composition fires to a smooth, dense nickel film that eliminates potential high current density sites and cathode sputtering problems. It is fired at 570 to 600°C; its electrical characteristics are not degraded by multiple air firing cycles in conjunction with dielectric and silver compositions.

For feedthroughs, silver conductor 7713 can be used to provide hermetic seals with both vitreous and crystalizable sealing glasses. Conductors can be printed up to and over the electrode material under the designated seal region and co-fired, eliminating the presence of silver within the tube.

Crossover and contrast dielectric compositions are also fired at 570 to 600°C. Their insulation resistance at 100 Vdc is greater than 10^{11} Ω and dc breakdown voltage is greater than 500 V.

Circle 160 on Inquiry Card

Our first SBC 80 compatible systems for 1977!

4K to 64K RAM Up to 8K EPROM on one board

Now you can have RAM and EPROM on the same board and buy as much or as little memory as you need. And because our memories use 16 pin memory element sockets you can change your memory when you change your mind.

Speaking of changing your mind, when you want to change address locations of either RAM or EPROM, it's done with two, on-board switches—providing 16 possible start locations for each memory.

Compare these features with our much improved read, write and refresh cycle times and you'll choose MSC first.

16K RAM Version

Up to 16K × 8 of RAM and up to 8k × 8 of EPROM on the same board.

RAM expandable in 4K × 8 increments and EPROM expandable in 1K × 8 or 2K × 8 increments.

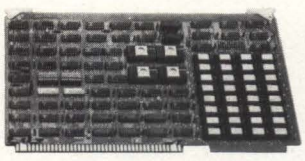
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

Delivery 30 days ARO.



MSC 4502
May

64K RAM version

Up to 64K × 8 of RAM and up to 8K × 8 of EPROM on the same board.

RAM expandable in 16K × 8 increments and EPROM expandable in 1K × 8 or 2K × 8 increments.

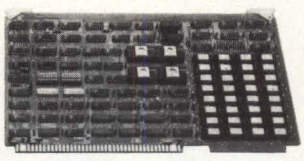
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

Delivery 30 days ARO.



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Data Base Software Modules Integrated Into Comprehensive Package

Data Management-IV (DM-IV), a comprehensive data management package for large-scale computer system users, provides flexibility, data independence, and ease of use. Personnel work directly with the computer on remote terminals using simple transaction and inquiry through any of the four modules that make up the package.

The modules—data manager, transaction processor, query and reporting processor, and procedural language processor—yield a high level of data independence and allow concurrent batch, transaction, and interactive processing. Data manager controls the structure of and directs access to online data bases used by the processor subsystem. Integrated data store (I-D-S/II) performs those management functions necessary to describe, create, and maintain an integrated or indexed data base that reflects real-world requirements.

Transaction processor provides high volume I/O to a data base through remote terminals. Pertinent updating of online data base is triggered and the resulting reply message is returned to the terminal.

Allowing each user to converse directly with the system and data base, the query and reporting processor performs data base inquiry using a "what if" style of questions designed to answer many spontaneous data reporting needs. Module features include flexibility to accommodate data bases for existing applications without conversion, language compatibility with other DM-IV functions, and a data base interface with other modules that offers data independence and a virtual or application view of the information.

An option to the query and reporting processor, the procedural language processor offers an alternative to COBOL-74 or FORTRAN and increases productivity by requiring fewer statements to describe a procedure. Procedures written in this language can be debugged online and made operational faster; through similar online routines, program maintenance costs can be reduced.

Operating on all series 60/level 66 computer systems, DM-IV is available from Honeywell Information Systems, Inc, PO Box 6000, Phoenix, AZ 85005 as a package or as individual modules. It can also be used on Series 6000 systems with extended instruction sets.

Circle 161 on Inquiry Card

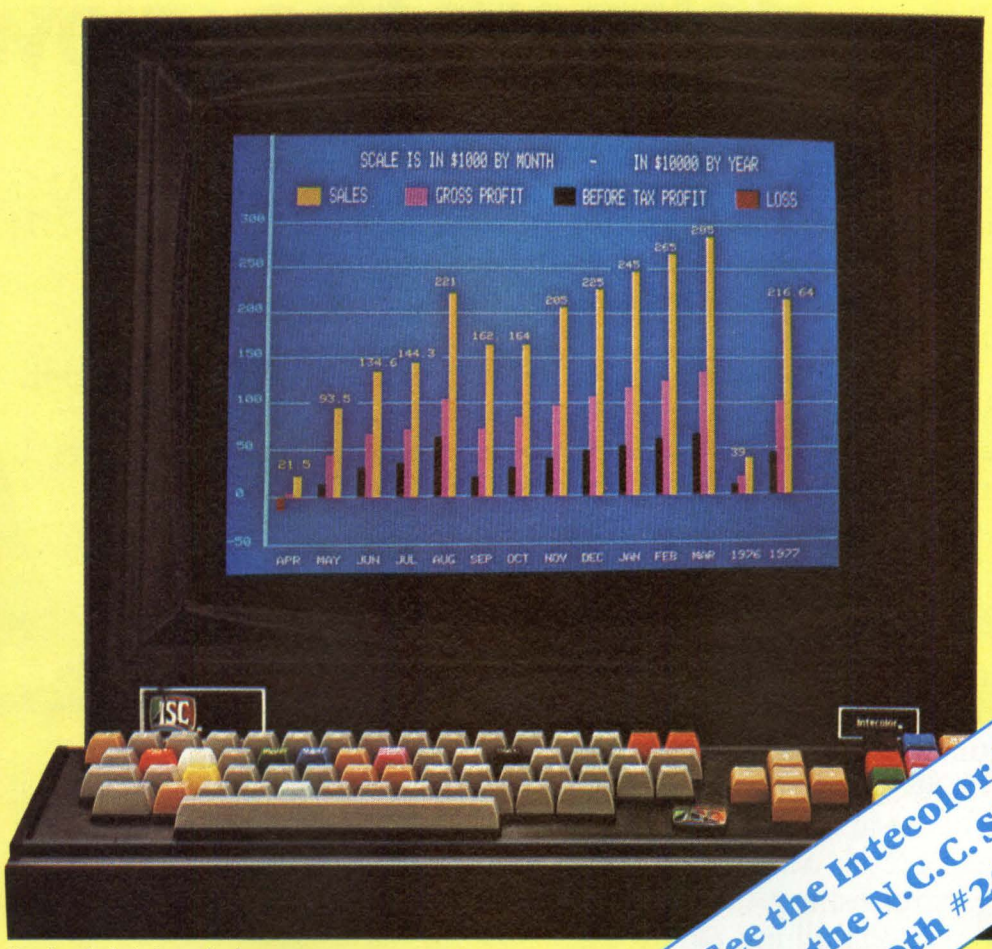
Cost-Effective "Recycling" Process Restores Disc Heads

Effecting dramatic savings in computer parts replacement costs, a process has been developed to permit the heads of virtually all commercially available disc drives to be restored. The proprietary process brings crashed or damaged heads back to original manufacturers' specifications at savings of 50% over replacement costs.

Developed by Trans Datacorp, 612 Bayport Ave, San Carlos, CA 94070, the recycling process consists of a combination of resurfacing techniques, adjusting and measuring processes, and online testing. Critical air bearings are resurfaced, components are replaced if necessary, all settings are adjusted, and each unit is fully tested.

The service covers all makes of 2314- and 3330-compatible disc heads. Adherence to original manufacturers specifications and performance criteria is guaranteed. Static and dynamic electrical tests are performed on every head, sliders are relapped to millionths of an inch curvature tolerances, load force is set for head stability in flight, and attitude for proper landing conditions is set. Final step is to test each head in flight under operating conditions, run performance evaluation data, and enclose resulting data with the returned unit. □

Circle 162 on Inquiry Card



Unretouched photograph of screen.

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Evaluation unit price—$1495, Limit one to a customer, cash with order
Domestic U.S.A. prices

Intel delivers the growing

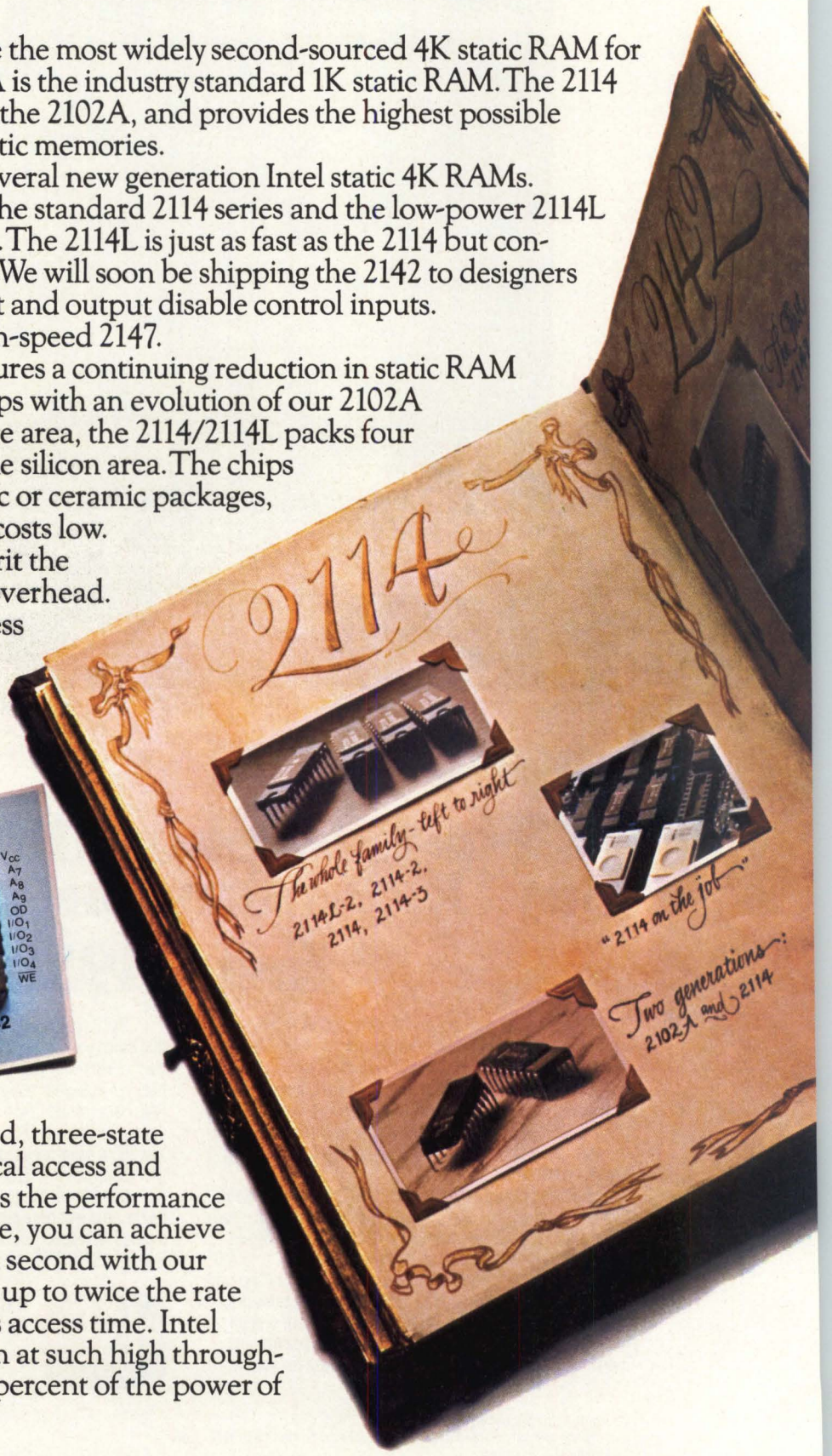
Our 2114 has already become the most widely second-sourced 4K static RAM for the same reason Intel's 2102A is the industry standard 1K static RAM. The 2114 simplifies system design, like the 2102A, and provides the highest possible density and modularity in static memories.

The 2114 is the first of several new generation Intel static 4K RAMs. We are now delivering both the standard 2114 series and the low-power 2114L series in production volumes. The 2114L is just as fast as the 2114 but consumes 30 percent less power. We will soon be shipping the 2142 to designers who want an extra chip select and output disable control inputs. Next, we'll add the super high-speed 2147.

This new generation assures a continuing reduction in static RAM costs. We fabricate the 4K chips with an evolution of our 2102A technology. At 181 mils square area, the 2114/2114L packs four times the bits in only twice the silicon area. The chips fit into standard 18-pin plastic or ceramic packages, keeping volume production costs low.

Our 4K RAMs also inherit the 2102A's ease of use and low overhead. You don't need a clock, address setup timing, or refreshing. You don't even need pullup resistors or output gating. These RAMs operate at TTL levels on a single

+5v supply and have buffered, three-state outputs. We guarantee identical access and cycle times, so you can surpass the performance of clocked RAMs. For instance, you can achieve a data rate of 20 million bits a second with our 200-nanosecond parts. That's up to twice the rate of clocked RAMs with 200-ns access time. Intel specs also guarantee that even at such high throughput you'll need only 25 to 50 percent of the power of first-generation static RAMs.



4K static RAM family.

As for board density, look at the pinouts. The 18-pin 2114/2114L configuration provides the highest density possible in 4K static RAMs.

Our 20-pin 2142 adds a second chip select—so you can go to 4K without external decoders—and an output disable for direct control of the output buffers. And since it is a simple modification of the 2114, it promises similar production economies.

You can minimize package count at any number of kilobytes since these new RAMs store 1Kx4 bits. With our compatible 256x4-bit static RAMs, you now have the widest range of modular design options. They are all listed in our new Static RAM Family Album.

Intel's 4K Static RAMs		
1K x 4	Access Time (max) Cycle Time (min) 0-70°C	I_{CC} (max) 0-70°C
2114-2 2114L2 2142-2	200 ns	100 mA 70 mA 100 mA
2114-3 2114L3 2142-3	300 ns	100 mA 70 mA 100 mA
2114 2114L 2142	450 ns	100 mA 70 mA 100 mA
4K x 1 with low power standby		
2147	70 ns	160 mA Active 20 mA Deselected

The 2114/2114L series is already as easy to get from stock as the 2102A. The 2142 soon will be. Contact any Intel franchised distributor: Almac Stroum, Component Specialties, Cramer, Elmar, Hamilton/Avnet, Harvey Electronics, Industrial Components, Liberty, Pioneer, Sheridan, L.A. Varah or Zentronics.

For your copy of our Static RAM Family Album, write: Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

In Europe, contact Intel International Corporation S.A., Rue du Moulin a Papier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814. In Japan, contact Intel Japan Corporation, Flower Hill-Shinmachi East Building 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Data Acquisition System Automatically Monitors Steel Rolling Mill

Much like many other relatively small areas within a very large processing complex made up of many seemingly unrelated domains, the rolling mill at a fully integated steel mill is an important cog in the work flow. If, for instance, a bearing on one of the generators in the rolling mill were to fail while a batch of steel was being processed, the entire batch might be ruined and have to be scrapped. In any case, the unscheduled downtime would be quite costly.

Before automatic monitoring of key parameters was initiated operators had to visually check rolling mill bearing temperatures, oil flow rates, and oil pressures. Despite precautions, human errors occurred, especially when the number of critical points to be watched increased. Problems sometimes developed unnoticed and, in time, caused unscheduled shutdowns.

As an attempt to improve this potentially costly situation, an automatic monitoring system was installed on the rolling mill at U.S. Steel's Geneva Works in Utah. This fully integrated steel mill processes iron ore, coal, limestone, and scrap through various stages into finished or semifinished products. Principal output items are plates, hot-rolled sheets, coils, structural shapes, welded pipe, pig iron, and byproducts.

The automated system monitors temperatures, oil flow rates, and oil pressures in 42 bearings; monitors a water recycling system to be certain it remains operative and warns of any trouble; and performs linear regression calculations of the plant's natural gas allocation in order to distribute gas efficiently over a 24-h period. If the temperature on a bearing begins to rise or if oil flow is impaired, the system provides sufficient warning to permit emergency procedures to be initiated, enabling either that the bearing be kept in use until the regular maintenance period or at least that the mill be cleared so that the product in process need not be scrapped.

Monitoring System Components

Major constituent of the maintenance monitoring system is an HP 9600 automatic measurement system (Fig 1) formulated by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304. It is rugged enough to function satisfactorily in the ambient temperatures of a steel mill which can be as high as 110°F (42°C). Key elements (Fig 2) are an HP 2116A computer with DACE (data acquisition control executive) software and RTE-II (real-time executive) operating system, HP 2911B crossbar scanner controller, HP 2911A crossbar scanner, HP 2401C digital voltmeter, HP 12925A tape reader, and ASR 35 teletypewriter.

The HP 2116A computer supervises the data acquisition system and interacts with all sensors (thermocouples). It also communicates with a second computer, an HP 2100A, via an RS-232-C interface (Fig 3). This second computer handles all data storage tasks for the system. Associated equipment includes a disc drive for the operating system, a Beehive Mini Bee CRT terminal which provides engineers access to the system for solving engineering problems, and a tape reader.

At present two teletypewriters are used to print out sensor alarms and hourly reports on the natural gas usage progression. A Tektronix 4008 graphics CRT shows what the power demand has been during any past 15-min interval and a projection of what it should be over the remainder of the 24-h period. Eventually this CRT will also be used to show alarms and to present the

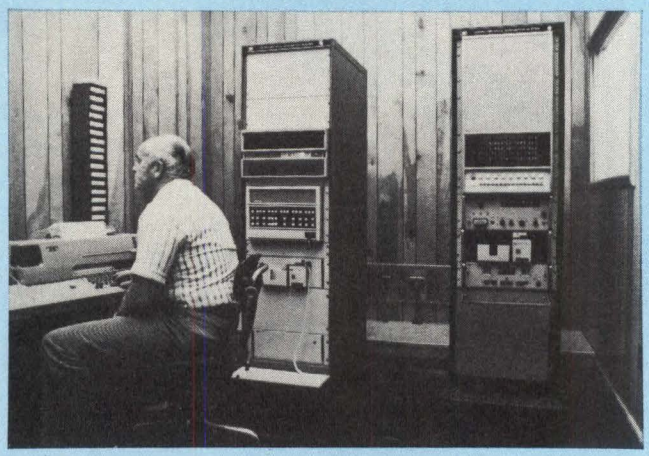

Fig 1 Hewlett-Packard 9600 automatic measurement system at load dispatch center of U.S. Steel's Geneva Works in Utah. For past four years system has monitored conditions of motor and generator bearings as well as operation of water recycler and has calculated natural gas usage within daily allocations. Capacity remains for enhancement to handle other duties still in planning stages

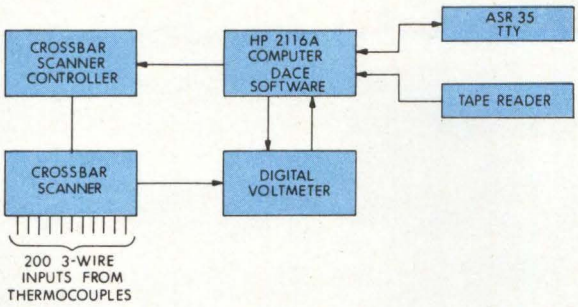

Fig 2 Interconnection of HP 2116A computer and other components for monitoring sensors at bearings and at water clarifier. DACE software controls data acquisition tasks for periodic temperature, oil flow, and oil pressure readings

natural gas usage progression over a graph of that usage. The second RS-232-C interface indicated on the diagram is for an 8080 microprocessor that will provide control of electrical energy usage.

Other elements include high and low level multiplexers, relay multiplexer, and analog-to-digital converters (ADCs). The high level multiplexer can handle up to 1056 channels with an accuracy of 0.09%. Each ADC handles as many as 44 channels with ±0.025% accuracy. In all, the system can scan 45,000 channels/s over a ±10.24-V range.

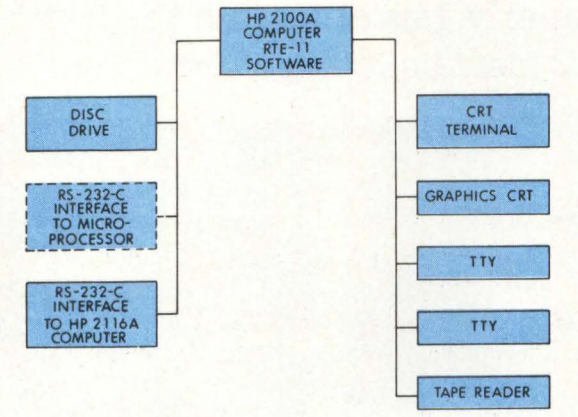

Fig 3 HP 2100A central computer system showing interface to HP 2116A. RTE-II software enables concurrent multiterminal operation. Microprocessor interface is for added subsystem that will go online for computer control of electrical power consumption

DACE is a core-based multitask scheduler which controls data acquisition tasks to periodically monitor bearing temperatures. Also disc-based, the RTE-II multiprogramming operating system schedules multiple programs to run concurrently on a priority basis. Foreground, background, checkpoint swapping, and multi-user swapping partitions enable multiterminal access to the data base and all other system resources.

The original system was set up for real-time maintenance monitoring as well as online program development, testing, editing, and linking. Main memory consisted of 32k words of core and basic disc drive capacity was 2.5M bytes. However, the system can be enhanced to access 118M bytes of disc storage for file management, program storage, and fast access data base.

DACE and RTE-II support input/output spooling to disc to speed throughput without excessive use of main memory for buffering, online interactive editing for program development, and management of a distributed multiprocessor network. FORTRAN was adopted as the language for concurrent processing and program development.

System Tasks

Most of the bearings monitored by the system are located in the slab rolling mill motor room. There, an 8000-hp wound-rotor ac motor is shaft-connected to four 2250-kW dc generators (Fig 4) which supply power to two 5000-hp dc roll motors. The system monitors the temperatures of 42 bearings ranging from 4 to 14 in (10 to 36 cm) in diameter and also monitors oil flow rates and oil pressures to those bearings.

Each bearing temperature is scanned once every minute. If a temperature reaches 178°F (82°C), an audible alarm sounds in the load dispatch center and the number of the problem bearing, its temperature, and the time of scan are simultaneously displayed on a CRT terminal. The load dispatcher then calls a maintenance operator by telephone and instructs him on what action to take.

Alternatives to shutdown include adding forced air or increasing the oil flow to the bearing to keep the temperature down and coax the bearing through to a normal shutdown. The load dispatcher can request a scan of the bearing as well as a hardcopy printout from a teletypewriter as often as necessary to remain aware of any changes in bearing condition. If the temperature rises too rapidly and the problem becomes serious, the operator notifies mill operations in time to permit work schedules to be revised.

Another system task is keeping track of the water temperature and level in a liquid slip regulator for the 8000-hp ac motor. This regulator acts as a heat exchanger and power dissipator across the secondary of the huge motor. Water is treated to give it a fixed resistance to the current in the motor's secondary and, therefore, water level and temperature are critical. Too high a temperature or too low a level could cause motor problems.

In addition, the monitoring system keeps track of the position of sweeps (paddles) and the operation of pump motors in the clarifiers (Fig 5), where water is cleared for reuse in the rolling mill. These clarifiers are huge tubs, 90 ft (27.4 m) across and about 40 ft (12.2 m) deep, into which sludge containing scale washed from rolled steel is drained. The sweep moves at about 6 revolutions/h through the sludge, stirring it until the scale

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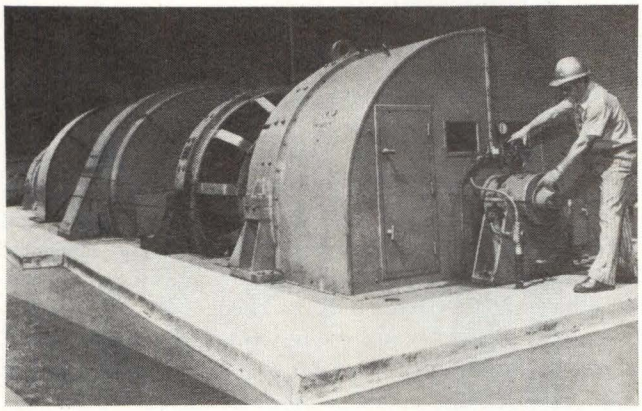


Fig 4 Two 2250-kW dc generators in mill's motor room. Four such generators are driven by an 8000-hp ac motor and, in turn, supply power to two 5000-hp dc roll motors. Computer checks sensors which continually measure bearing temperature as well as oil flow rate and pressure to those bearings

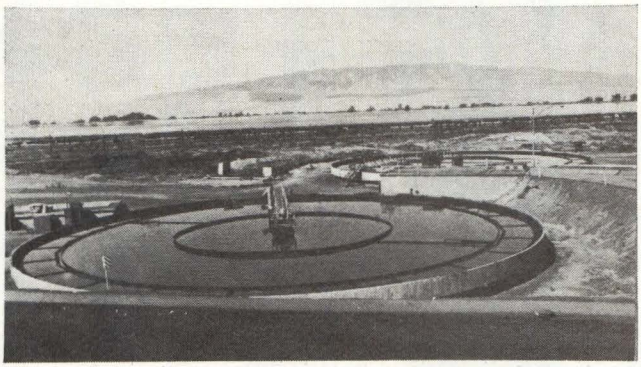


Fig 5 Water clarifier. Automatic monitoring warns of any trouble with slow sweep which stirs recycling water. Once sweep stops, scale and sludge can prevent it from restarting

settles to the bottom and sludge pumps remove it. If a sweep stops, the sludge can freeze the sweep in place, making it necessary to drain the clarifier and remove the sludge manually.

If the sweep stops, the monitoring system notifies the load dispatcher, who in turn notifies maintenance operators. If a circuit breaker has tripped, the maintenance operators try to restart the sweep; or if shear pins on the sweep shaft have broken, the operators replace them. If necessary, sludge-bearing water can be pumped to another clarifier while one is being worked on.

As with all large consumers of natural gas (see *Computer Design*, Feb 1977, pp 46-55) the Geneva Works is allocated a predetermined amount for each 24-h period. Any usage over that allocation is billed by Mountain Fuel Supply at a surcharge of \$10/1000 ft^3 (\$10/30 m^3). Therefore, up-to-the-minute knowledge of gas usage rate is critical, particularly in the winter when the allocation is low.

The automatic measurement system keeps track of the gas usage rate and distributes the allocation over the full 24-h period. To do so, it performs linear regression calculations and gives updates every minute on the current usage rate and the permissible rate for the remainder of the current period.

Reliability and Payback

In four years of operation, there have been only two problems with the system, both minor. Reportedly, the system has paid for itself several times over, both in greater monitoring reliability and in reduced lost-labor costs for unscheduled downtime.

Probably the most critical potential problem discovered and prevented by the system involved a 14-in (36 cm) babbit bearing on the shaft connecting the 8000-hp ac motor to the dc generators. Sensors detected a dangerous rise in temperature and alerted the local dispatcher before the bearing was damaged. If not detected, the high temperature would have ruined the bearing, the rolling mill would have had to be shut down for repair, and there would have been heavy losses in labor and product costs.

Future Applications

When first designed and placed online this measurement system contained provisions for enhancement—even to include certain phases of computer process control. For instance, an interface has been designed that will enable computer control of electrical power consumption, another area where penalties for peak usage are costly. An 8080 microprocessor (see Fig 3) will be interfaced to the HP 2100A computer to permit controlled allocation of power to the rolling mill by adjusting the rate at which ingots are removed from the soaking pits (where they are heated to rolling temperature) and rolled. The electrical energy needed to roll the ingots cannot be reduced, but the rate at which ingots arrive for rolling can. In addition the computer will be able to shut down unneeded electrical equipment, including lights.

Geneva Works also plans to add maintenance monitoring of the structural and blooming mills this year. Within the next two years it is anticipated that the plate mill will be added to the monitoring system.

As budget permits, considerable use of the measurement system is planned for programs outside the monitoring field, such as maintenance planning. Data captured in monitoring would automatically be used to determine when maintenance should be scheduled. There are also plans to use the computer to control inventory of the several thousand spare parts used in maintenance.

Circle 163 on Inquiry Card

Chromatography System Provides Continuous Analysis of Gas Supply

Energy content, specific gravity, and composition of gas are critically important to gas producers, transporters, and users—although this last group may not realize it. Highly accurate online measurement of all three, therefore, is a necessity; and Electronic Associates, Inc, W Long Branch, NJ 07764 has designed a system to meet the requirements. ProPACE™ 250 provides 24-h, unat-

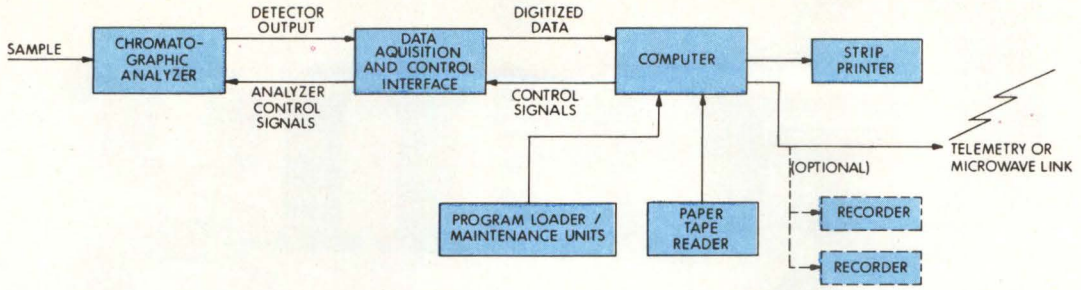
tended operation for remote stations as well as terminals and plants. It measures and reports gas energy content in British thermal units (Btu) to an accuracy of ±0.5 Btu in the 1000 Btu/ft³ range. Specific gravity (SG) measurement of accuracy is ±0.003 units at an average SG of 0.6100.

Major components of the system are an industrial-type digital computer and an all-weather process chromatographic analyzer. Other units include data acquisition/control interface, strip printer, program loader/maintenance unit, power supplies, two A-D converters, paper tape reader, detector, and optional recorders. Analysis can be performed on compositions of either natural or synthetic gas containing up to 15 components, including combustibles, noncombustibles, and saturated and nonsaturated hydrocarbons.

System outputs are both digital and analog. Continuous 0- to 10-Vdc analog outputs may be used locally to record Btu and SG and/or as input to telemetry for transmission to central monitoring stations. British thermal units and specific gravity, along with time of day and other sample information are recorded on a local strip printer, to the nearest 0.1 Btu/ft³ and 0.0001 SG unit.

Diagnostics built into the computer program constantly monitor fidelity of the results and flag any malfunctions. If there is a power failure the system shuts down by itself, with automatic, orderly restart after restoration of power. Calibration checks are automatically performed every 24 h under commands issued by the computer program; complete, fully-labeled composition reports may be issued as frequently as needed.

Computer and related equipment are mounted in a metering house or control room and operate over a



Chromatographic analysis system, under control of industrial computer, provides full-time, unattended, online measurement of gas energy content and specific gravity as well as composition

temperature range of 50 to 104°F (10 to 40°C). The chromatographic analyzer is in a self-contained housing; its operating temperature range is 0 to 130°F (−18 to 55°C). Circle 164 on Inquiry Card

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And to celebrate, we're having a "sale."

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To get 10% off Intel's 80/10, don't buy Intel's 80/10. Buy National's 80/10.

We're able to sell the 80/10 for less because of our improved board layout which permits automated assembly (such as using axial leaded components)...the fact that we make not only the 8080, but also—unlike Intel—most of the rest of the ICs on the board...and, of course, National's legendary competence in efficient manufacturing doesn't hurt either.

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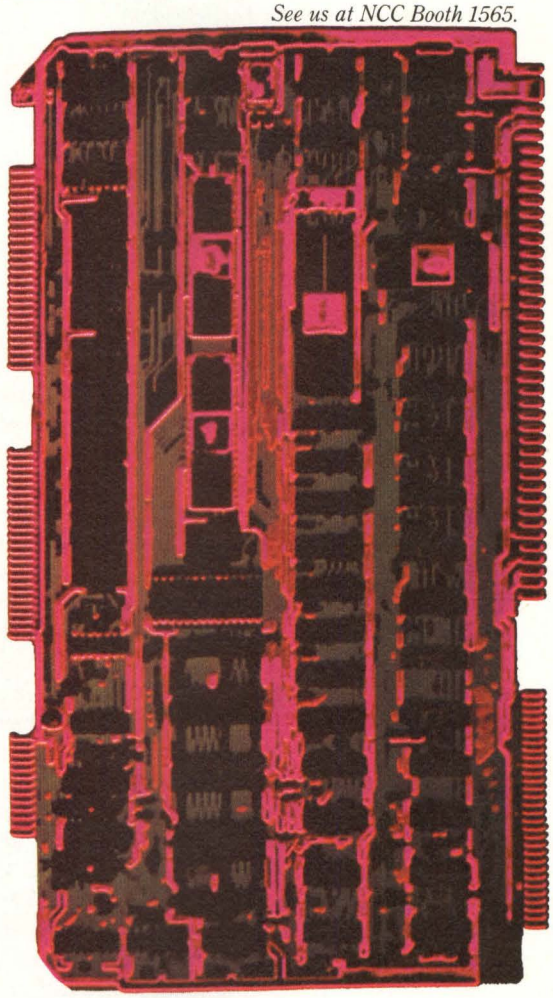

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National Semiconductor

Program and Extensive Data Base Alert Physicians to Possible Adverse Drug Reactions

Any patient admitted to a hospital today undergoes extensive questioning that covers far more than his hospitalization insurance number. A large part of the questioning concerns the names of prescription drugs he may be taking and known adverse reactions to other drugs.

Hospitals are becoming very concerned about such adverse reactions and particularly about the possibility of interaction among two or more drugs. Since the per capita annual average for written prescriptions is said to be 10, since many prescriptions are multicomponent medications, and since many drugs remain potentially active for significant periods after the person stops using them, the possibility of adverse reaction is high. One source estimates that billions of dollars are lost each year in the U.S. as a result of death, additional illnesses, extended hospital stays, and time lost from work caused by adverse drug reactions. Another source estimates that 22% of such reactions are due to interactions that produce clinical results not attributable to any one drug used by itself.

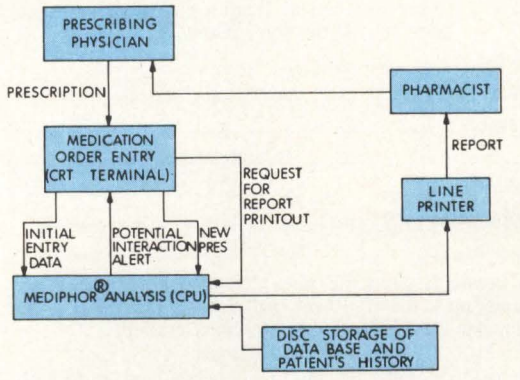
Therefore, many farsighted hospitals either have installed computerized drug interaction prediction schemes or have tied packages onto existing computer systems in order to carefully review each patient's drug therapy regime. One relevant arrangement developed at Stanford University School of Medicine and in use there since 1973 consists of a program tied to a data base. The latter contains information on clinically documented interactions and a mechanism for comparing those data with medication requests and patient drug profiles. The scheme automatically screens a patient's drug therapy to detect specific combinations of drugs that could negate or reduce their individual values or even cause harm to the patient.

Called Mediphor® (for monitoring and evaluation of drug interactions by a pharmacy-oriented reporting system) the program and data base have been integrated by B-D Spear Medical Systems, 123 Second Ave, Waltham, MA 02154 to its Pharmacy System 830. Medication orders and other appropriate information are entered on a CRT and simultaneously transmitted to the computer file. The computer immediately searches the patient's drug profile and, if a drug/drug interaction potential is indicated, automatically provides audible and visual warnings. If requested by the pharmacist, the system can print a documenting report noting interaction, severity, immediacy, and clinical significance. The package is scheduled to be installed this year in several other hospitals including those at the Universities of Kentucky and Wisconsin.

There is no intent to interfere with physicians' decisions on prescribing drugs. The system instead provides information on which the physician may act.

Early evaluation results at the Stanford University Medical Center show that, at the point at which over 77,000 patients had been screened, the probability of administering two potentially interacting drugs was 3% for patients receiving five drugs, 10% for 10 drugs, and 30% for 20 or more drugs. Valid drug interaction reports were issued for 7 to 8% of hospitalized patients. There has been a 10% decrease in drugs administered per patient, 14% fewer drug interactions, and a 33% drop in multiple drug interactions.

Circle 165 on Inquiry Card



Information flow for evaluating drug interaction with Mediphor program and data base. Preliminary evaluation of 3-year period indicates up to 33% reduction in multiple drug interaction

DC&AS BRIEFS

Australian Traffic Controlled by Minicomputer-Based Systems

A computerized system designed by Eagle Signal of Australia Pty, Ltd is being installed in Brisbane to control traffic. Based on a Data General Corp Nova minicomputer, the system combines data collection and communications equipment to provide online coordination of traffic signals. It is believed to be among the most advanced of its kind in the world.

In another Brisbane system which has been controlling 20 intersections in Fortitude Valley since April 1974, calculations based on savings in vehicle operating costs alone show that all installation costs were recovered in about eight months. These benefits are said to be augmented by savings from reductions in accidents, noise and air pollution, and traveling time. There are three levels of control: the minicomputer controls the traffic master, which controls intersection traffic signals, which control traffic.

In the Fortitude Valley system, approximately 30 vehicle detectors located at intersection and midblock points supply information on traffic flow over communication links to the minicomputer. Preselected patterns for coordination of traffic lights are stored in a digital memory unit. The minicomputer is programmed to examine the vehicle detector information and to issue automatic instructions for the application of the preselected patterns to the interface equipment.

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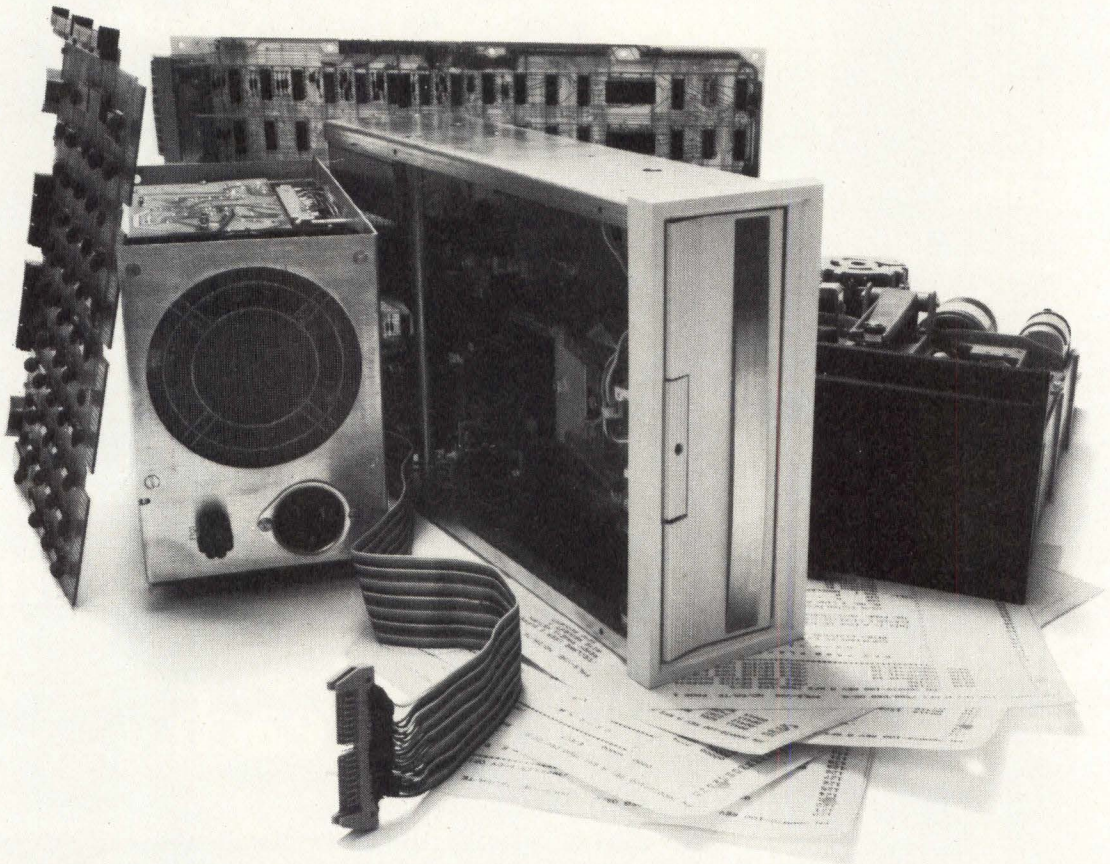
THEIR PARTS



An OEM flexible disk subsystem is more than the sum of its parts. Getting optimum performance at a low unit price requires design control to eliminate redundancy and volume production to reduce cost.

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The RFS7500 is comprised of one to four RFD1000 Flexible Disk Drives, a microprocessor based controller/formatter, interface and software for most major minicomputers plus power supply cabling and rack mountable chassis. Because it is a fully integrated subsystem, the RFS7500:

☐ expands data capacity through implementation of IBM3740 format or a user selectable 1, 2, 4, 8, 16, 26 or 32

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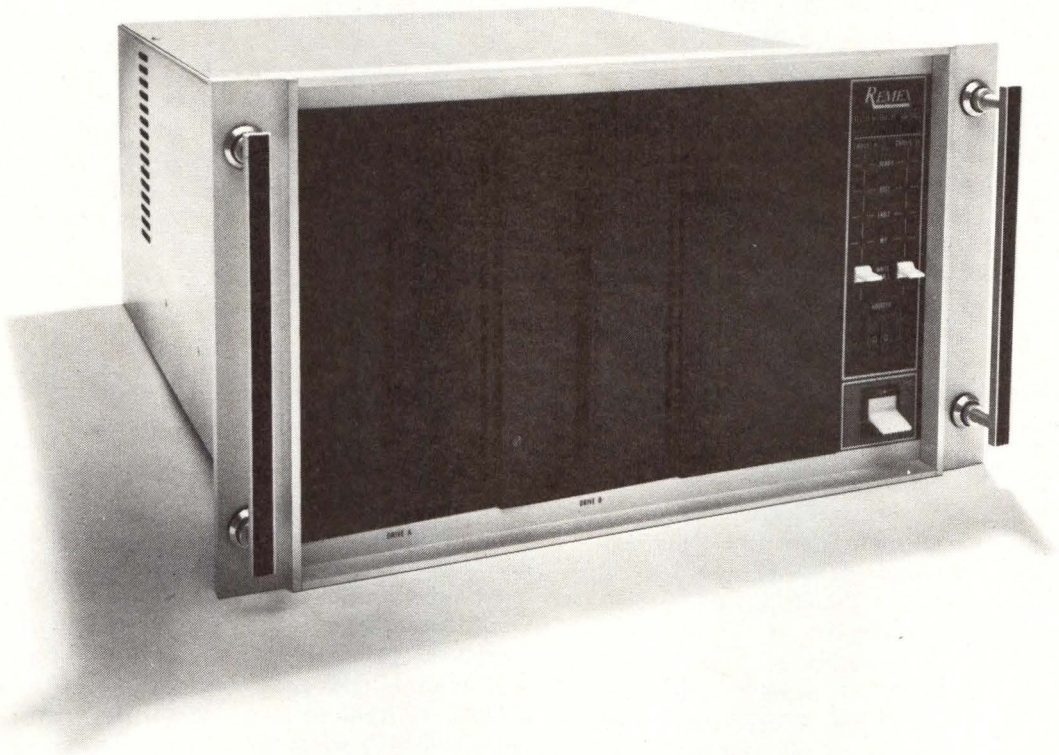

sector format. ☐ saves computer time by data block transfer of from one to 65K 2-byte words on a single command from the host. ☐ reduces core memory requirements due to automatic track and sector search and auto-initializing without software. ☐ simplifies operation and system integration by 8-command structure. ☐ saves space by housing interface card in the system chassis in some configurations. ☐ speeds access through 6 ms track to track speed plus unit select.

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DC&AS BRIEFS

Computer-Controlled System Automates DIP Assembly

A minicomputer-controlled reflow solder system for automated assembly of surface-mounted components on PC modules, the HPS-300 automatic flat pack assembly system, has been introduced by Hughes Aircraft Co's Industrial Products Div, Carlsbad, Calif. It is designed primarily for electronic manufacturers using large quantities of flat packs or surface mounted DIPs in their PC board assembly operations with component usage exceeding 30,000 per month, and is the first time that computer control has been combined with the company's reflow solder stations. Control computer is a Hewlett-Packard 21MX.

Under program control, the system automatically performs all functions from selecting and extracting a component from a magazine to positioning and soldering it on a PC board. Assembly rates exceed 350 components/h, with the program formatted on punched tape.

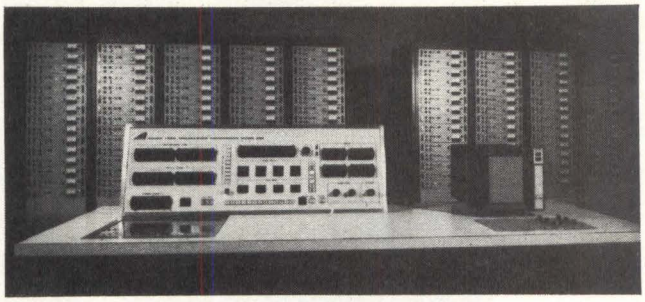
The system selects a component carrier and deposits it in a transfer mechanism which opens the carrier, centers the part, and presents it to the head assembly. The part is then extracted with a vacuum quill, rotated to programmed position, and moved down to alignment height over the PC board which has been positioned to proper X-Y coordinates. Final alignment is monitored by closed circuit TV, and a dwell feature permits the operator to make fine adjustments.

Reflow soldering is performed according to five program-selectable "time-at-temperature" schedules with each heater element equipped with separate power supplies and digital switch controls. The control programs, consisting of ASCII characters, determine the magazine selected, rotation of the part, X-Y position of the PC board, and selection of the proper solder schedule for each power supply.

Two of the systems are operating in a production environment for the assembly of avionic systems at the company's El Segundo division. A component verification system, available as an option, consists of an inline probing station that performs a limited functional test to insure that the selected component is correct, operational, and positioned properly in the carrier.

Closed-Loop Servo Controller Maintains Computer Input Setpoints

A dual-loop supervisory control and data acquisition system, capable of handling from three to several hundred load controllers, can apply up to 16 hydraulic loaded



functions. System accuracy through control loops is said to be typically ±1%.

Instructions to the HSCADA system, made by Avco Electronics Div, 4807 Bradford Dr, Huntsville, AL 35805, are provided through setpoints input through an operator's panel. Digital function generator control is provided by a computer and then converted to analog as an input to the closed-loop servo amplifier controller. That device then compares the difference between required and actual loads. The resultant error signal excites the controller to activate servo valves, repositioning the hydraulic cylinder so that applied load equals required load.

Applied load is monitored by a digital control loop, built around the company's DATA-ACQ, and measured via a strain gage mounted on a load cell. A transducer signal conditioner and multiplexer uses the amplifier-per-channel concept for exceptionally high common-mode rejection ratios even with very large common-mode voltages. Corrections are computed and the forcing function is modified to automatically correct any errors.

System Programs NC Machine Tools by Voice Commands

A system now in use by Calabrese & Sons, a Mechanicsburg, Pa producer of machined parts, programs machine tools by voice command and prepares tapes for the numerically-controlled devices. VNC-200, manufactured by Threshold Technology Inc, 1829 Underwood Blvd, Delran, NJ 08075, is a complete standalone, 2-axis, continuous path system with third axis control, rotary axis control, and an easy to use lathe programming module. It features 10M-byte cartridge disc, minicomputer with 32k words of memory, line printer/console/reader/punch, 22″ (56 cm) plotter, and voice input module which includes a 16-character visual display readout for verification of the spoken machining commands.

Programmers speak to the system in everyday shop terms. If programming errors occur, the system displays them as they happen for on-the-spot correction. The plotter graphically develops each part as programming proceeds, so that the NC programmer sees the exact part prior to machine operation.

Currently the system prepares tapes for two 8-15 and two 12-30 Pratt & Whitney Star Turn lathes, two Mazak lathes with 20A control, Seiki 6 MC horizontal machining

Hughes' low-cost C-9 display terminal makes a minicomputer work like a giant.

Here's an interactive graphic terminal that does with hardware what most terminals need software to do. It needs only a mini-computer or telecommunications coupler and a 110-volt outlet to give you a ready-to-work system. And it costs less than $10,000.

More for your money

The new C-9 terminal offers high resolution, selective erase, serial interface (standard), and several other features otherwise offered only by units costing almost twice as much—like 17-inch diagonal, 1029-line-scan, cathode-ray-tube video monitor with high light output screen for easy daylight viewing....computer independent zoom and pan....a joystick for graphics and alpha-numerics interaction....a hardware graphic processor for scaling and rotating graphics and alpha-numerics.

The architecture of the terminal embodies a micro-processor driven by micro-programs contained in read-only memories. A serial interface connecting the detached keyboard to the CRT display eliminates restrictions imposed by parallel interfaces used in other models.

Optional features

You can extend the C-9's capability even further with options like enhanced graphic hardware package with rotations, reflections, and line-texturing features or programmable gray levels for graphics (16 levels) and digital raster continuous tone images (256 levels). We also offer parallel interfaces for a variety of minicomputers and interfaces to popular digitizers for local data input and control of the interactive CRT cursor.

The new C-9 offers a continuous writing mode and a new capability which guarantees that writing occurs only during vertical retrace time.

Smoother curves and lower costs

The patented Conographic™ generator, using conic curves to plot curvilinear information, produces smoother curves from much less data, thus requiring less computer memory, simpler software, less computer or telecommunications time. Result: The lowest *total cost of ownership* of any graphic terminal available today.

Many FORTRAN IV software programs are available, including a new set of Tektronix-compatible subroutines. The basic software package, called CONO-PAC, is available at no extra cost.

To find out how your minicomputer can work like a giant for much less cost, contact your local representative, or Hughes Image and Display Products, 6155 El Camino Real, Carlsbad, California 92008. Or call (714) 438-9191.

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DC&AS BRIEFS

center with Fanuc 3000C control, and Giddings & Lewis horizontal machining center with G&L CNC control. Postprocessors are included for each machine tool. Additional machines or new formats can be added.

Modules Add Logic Circuit Test Capability to Automatic Device

Addition of recently developed modules to the established Pegamat automatic test system, used for a number of years in the measurement of communications parameters, now enables the device to be used for testing analog and digital circuit board components and complete units. The added equipment allows analog electronic circuits using dc techniques and ac techniques up to 100 kHz to be tested and combined. It also allows hybrid circuits and sequential logic circuits such as those employing TTL, ECL, and MOS to be checked. An adapted version of Standard Atlas is used as the test language.

Introduced by Siemens AG, Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany, the system includes a patch panel with up to 320 terminals for connecting analog test specimens. (A version is available for switching a maximum of 220 V at 5 A.) This patch panel is designed as an 8-layer circuit in order to isolate input, output, and control signals and thus reduce crosstalk to a minimum. A software package for supervising the patch panel automatically controls and monitors all signals and also has a protective function; eg, it prevents two power supplies from being connected in parallel.

A digital module with up to 360 terminals is used to test digital circuits. Complex tests can be carried out with the aid of various high power drivers (up to ±25 V/80 mA sink and source), four receivers (up to ±75 V), load resistors which can be connected by means of a program, and a time unit. Two clock-pulse generators, which are synchronized in phase and which can be connected to each terminal by means of a program, must be set so that 2-phase shift clock pulses with different frequencies can be produced. In order to test hybrid modules, a multiplexer connects either the analog patch panel or the digital module to the terminal on the test specimen so that the analog and digital test sections can be fully exploited without adversely affecting one another.

Automatic fault-finding employs a probe with highly sensitive microelectronics. It detects high and low states of digital circuits as well as short circuits to chassis and to the operating voltage and breaks and shorts in conductor paths. A fault-storing circuit receives wanted and interference pulses, thereby allowing faulty components to be detected in loop circuits by locating the point at which the fault first appears. □

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We've won our dominant position at the end of the semiconductor production line and at the beginning of the electronics assembly line through hard work and understanding. What we start, we stay with, but you can see that every time you walk through your production-test or incoming-inspection area.

We've come to think of those places as our turf, and we intend to keep it that way.

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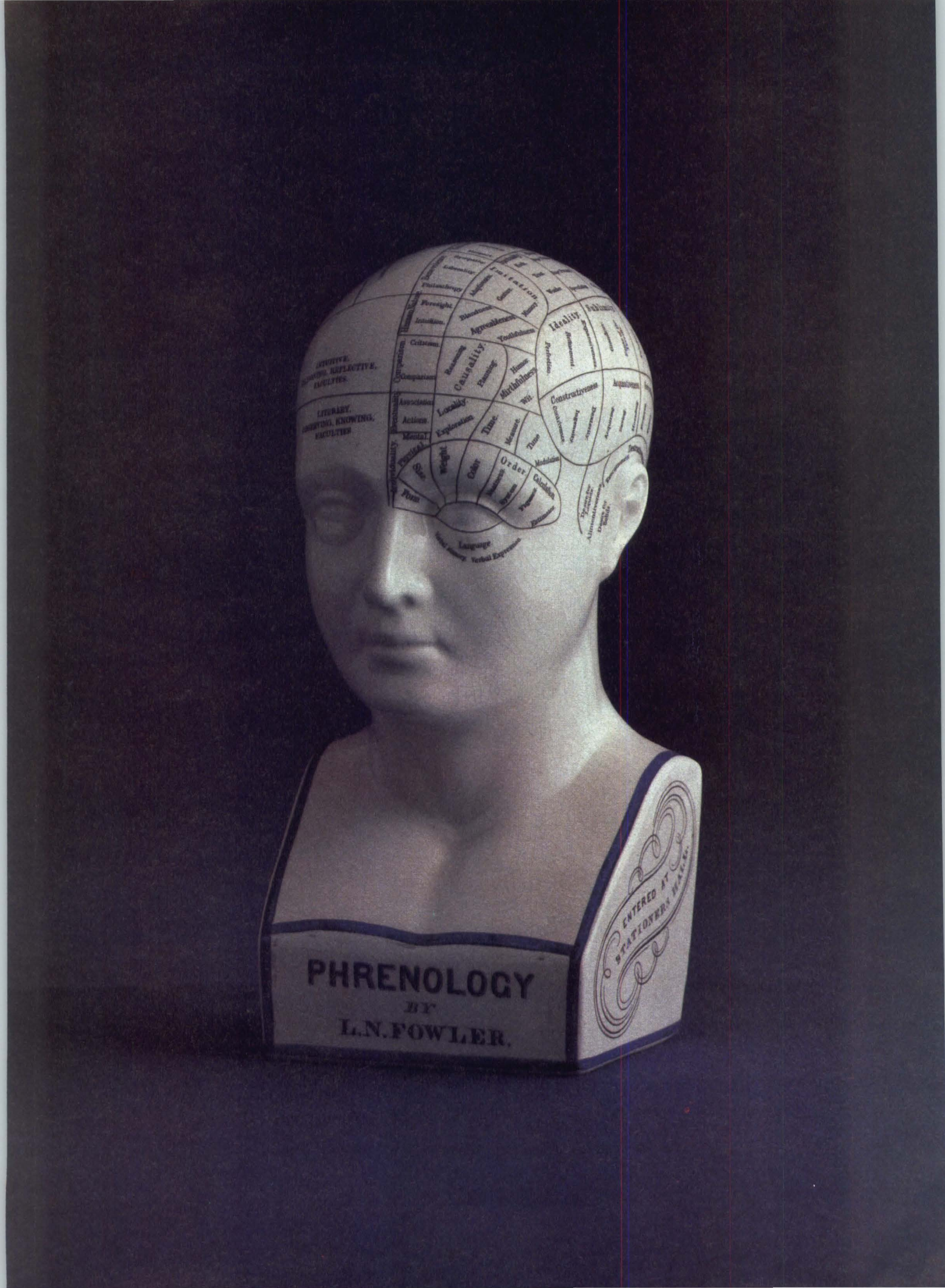
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The Computer with a Subconscious.

Your eyes blink 25 times a minute. You don't realize it because this routine, like thousands of other vital routines, is handled by your subconscious.

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This is also a good description of how the new SEL Regional Processing Units operate within the SEL 32/75 System. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating Point Hardware, Writable Control Storage, and flexible interleaving.

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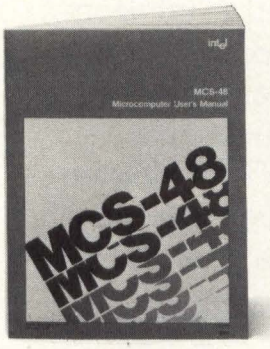

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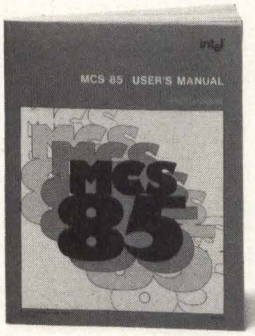

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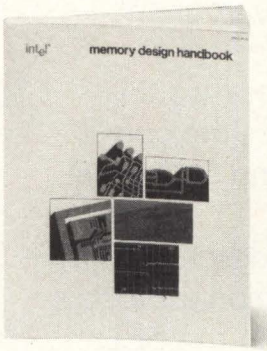
288 pages
We designed our new 8085 to give you a high performance microcomputer with a built-in head start—bus and software compatibility with the industry standard 8080. User's manual details MCS-85 system operation, data sheets and application notes, plus specs on compatible peripherals and standard memories.



3. 1977 Intel Memory Design Handbook 288 pages
For the facts on efficient memory system design, come to the source: Intel. We're the pioneers and leading suppliers of semiconductor memory. Our new design handbook is the definitive compendium of memory applications. Covers system design using RAMs, PROM/ROMs, CCD and memory support circuits. Includes actual PC board layouts for many applications.

4. 1977 Intel Data Catalog
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Here are 928 pages detailing *what* Intel delivers. Complete electrical specs on 286 Intel memory components, systems and support circuits, microcomputer systems, peripherals and development aids. Includes data sheets and comprehensive information on our MCS4/40, MCS 48, MCS 80/85 and Series 3000 microcomputer families. Provides an index of available software and workshop programs.

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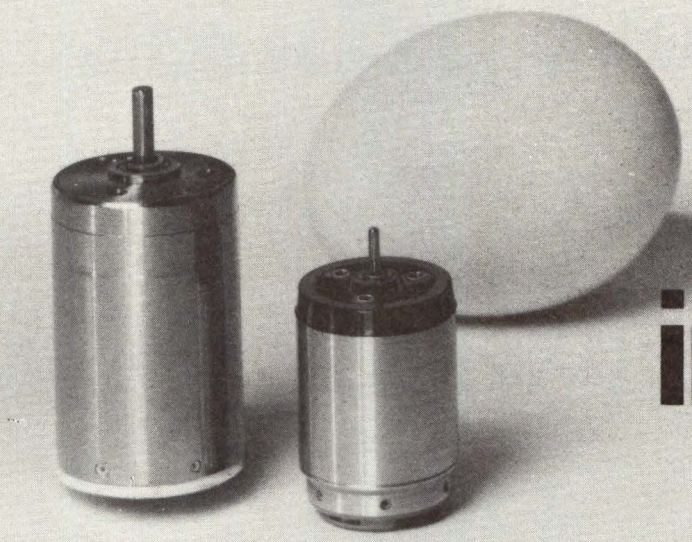

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No other micromotor on the market today offers the high reliability and optimum performance efficiency of an escap® miniature dc servomotor. We earned our reputation by building a quality line of motors that not only deliver superior performance, but superior cost effectiveness as well. We're ahead of our competition in such areas as space-saving design, low current consumption, high efficiency, and ripple-free torque, just to name a few, because for over 15 years we have made a continuous investment in new product development, as well as product line reliability and performance.

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CIRCLE 46 ON INQUIRY CARD

The complete $655 line printer.

It's ready to plug in, has an 80-column format, a remarkable MTBF and is 14 times faster than a teletype!

Breaking the hardcopy barrier

It's finally happened! The Axiom EX-800 provides full performance hardcopy at a price compatible with today's low cost micros. This little 80-column machine zips along at 160 characters per second (14 times faster than a teletype)—at a breakthrough single quantity price of $655 for a complete printer.

When we say complete we mean it

The EX-800 is a stand-alone unit with case, power supply, 96 character ASCII generator and interface, paper roll holder, infra-red low paper detector, bell, and multi-line asynchronous input buffer. You won't find these standard features on any other printer, regardless of price!

Our only option

Our printer is so complete, that we offer only one option. A serial interface (RS 232C or current loop) good for 16 baud rates from 50 to 19,200 and thoughtfully provided with a switch for either Centronics or Tally compatibility. Might we call it a Tally-whacker? At $85.00 it certainly should be!

Built-in LSI microprocessor

The heart of the EX-800 is a printed circuit card, containing a custom LSI chip made by Intel to Axiom specifications, which controls all printer functions. Microprocessor power means flexibility. Such as the built-in self test routine and variable character size. It also means reliability. Several industry surveys have shown LSI to be many times more reliable than equivalent conventional circuitry.

THIS LIFE-SIZE SAMPLE SHOWS THE 80-COLUMN PRINTOUT FROM AXIOM'S EX-800 PRINTER

There are 3 character sizes (upper and lower case) which can be MIXED.

This can have the same effect as UNDERLINING or changing COLOR.

The advantages of electrosensitive printing

The EX-800 can print 80, 40, or 20 characters across the five inch wide electrosensitive paper. Under software control, single characters or words may be printed larger for emphasis. The permanence of the hardcopy is archival, because once the aluminum coating has been removed, there is no way to put it back. It's unaffected by sunlight, moisture or heat. Although the printer doesn't provide multiple copies, excellent quality photocopies can be made from the high contrast printout. Also, the paper is inexpensive and readily available, costing about 1¢ for an 8½ x 11" equivalent.

Light, small, quiet, reliable, and versatile

Our EX-800 weighs in at 12 pounds, is just 9½ inches wide, 4 inches high, and 11 inches deep, and is delightfully quiet which makes it ideal for office and other low noise environments. The simple print mechanism is virtually maintenance free. In fact, tests show an incredible MTBF, many times greater than impact printers. This versatile printer is the ideal mate for micros, minis, CRTs, instruments and systems.

Just unbox and plug it in

That's all you have to do to the Axiom EX-800 — apart from pay for it, and at $655 that's <u>almost</u> a pleasure.

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- ☐ Send lit including sample of printout

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CIRCLE 47 ON INQUIRY CARD

COMPUTER DESIGN

PREVIEWS THE 1977 NATIONAL COMPUTER CONFERENCE

1977
National Computer Conference

Dallas Convention Center
Dallas, Texas
June 13-16

Addressing the issues of technology, applications, management, and the individual in relation to computing, the 1977 National Computer Conference will seek to solicit involvement, while also inspiring and educating attendees. The Great Computer Roundup is aimed at the consumer-oriented role of computers. Approximately 100 sessions contained in the Technical Program—summarized in last month's issue of *Computer Design*—examine topics which range from design, evaluation, and operation of systems; programming; hardware; networking; and architecture, to the roles, responsibilities, management, and education of people involved with computers. The inclusion of the Personal Computing Fair and Exposition further reflects the rise, continued growth, and future promise of the field.

The Conference at a Glance outlined on the following pages lists the separate program sessions and hours.

Exhibits

Every area of data processing technology will be covered by over 300 organizations, with exhibits on digital, analog, and hybrid systems; data communications equipment; components; microprocessors; minicomputers; mainframes; CRT displays; memory systems; printers and plotters; software and timesharing services; and test equipment. Items will be on display in the Convention Center from 11 am to 7 pm on Monday and 10 am to 6 pm on Tuesday, Wednesday, and Thursday.

Information on many of the products to be shown is contained on the pages following the Conference at a Glance. Only items for which data were available at press time are included. Emphasis is placed on those products being exhibited for the first time; a review of other products is included for the convenience of our readers.

CONFERENCE AT A GLANCE

MONDAY

	2:00 - 3:30	3:45 - 5:15
COMPUTER SCIENCE AND TECHNOLOGY	DATA BASE ADMINISTRATION *Peter Scheuermann*	DATA MODELS AND THEIR APPLICATIONS *Peter P. S. Chen*
	COMPUTER SYSTEMS ARCHITECTURE *Yih-Wu Han*	TOWARD THE COMPUTER OF TOMORROW: A MULTI-FACETED CHALLENGE *Lowell Amdahl*
	SECURITY OF COMPUTER SYSTEMS *Richard E. Merwin*	COMPUTER SECURITY RISK ASSESSMENT *Rein Turn*
	COMPUTER GRAPHICS *Nancy Storch*	SYMBOLIC EVALUATION *Edward F. Miller, Jr.*
MANAGEMENT AND APPLICATIONS	DEVELOPMENTS IN COMPUTER OUTPUT MICROFILM (COM) AND MICROGRAPHIC TECHNOLOGY — PRESENT AND FUTURE *Don M. Avedon*	
	HOW TO SELL, SERVICE AND SUPPORT CUSTOMER NEEDS WITH SMALL BUSINESS COMPUTERS *Donald W. Fuller*	SMALL BUSINESS INFORMATION SYSTEMS *Frederick F. Newpeck*
	CLINICAL APPLICATIONS OF THE COMPUTER *Lynn Peterson*	AGE OF COMPUTER BASED MEDICAL CONSULTATION: WILL IT BE FAIR? *John Lackmann*

Separate registration will be required for each seminar. ▶

TUESDAY

	9:00 - 10:30	10:45 - 12:15	2:00 - 3:30	3:45 - 5:15
COMPUTER SCIENCE AND TECHNOLOGY	SELF-ORGANIZING/SELF-OPTIMIZING DATA BASES *Gene Altschuler*	ADVANCED CONCEPTS IN DATA BASE MANAGEMENT *Gene Altschuler*	USER EXPERIENCE WITH RELATIONAL DATA BASE SYSTEMS *Michael Stonebraker*	DATA BASE DESIGN METHODOLOGY *Philip Y. Chang*
	SELECTION METHODS FOR A FAMILY OF COMPUTER ARCHITECTURES *Y. S. Wu*		THE ENGINEERING OF COMPUTER SYSTEMS *William P. Summers*	GOVERNMENT PANEL ON RESEARCH IN COMPUTER ARCHITECTURE *Jimmie R. Suttle*
	MICROPROCESSOR ARCHITECTURE *Charles R. Vick*		DEVELOPMENTS IN OUTPUT DEVICES *James O. Matous*	MAN-MACHINE INTERACTION *Seymour Jeffrey*
	SOFTWARE MANAGEMENT: HOW TO START A SOFTWARE DEVELOPMENT PROJECT *Richard Thayer*		DATA STRUCTURES *Julie Landstein*	MINI AND MICRO DESIGN MISTAKES *Helmut E. Thiess*
MANAGEMENT AND APPLICATIONS	SYSTEMS STRATEGIC PLANNING — A VIEW FROM THE TOP *Harvey L. Poppel*	THE MANAGEMENT OF DISTRIBUTED COMPUTING IN LARGE ORGANIZATIONS *Larry D. Woods*	ICCP AND CERTIFICATION MOVE FORWARD *Fred H. Harris*	CERTIFICATE IN DATA PROCESSING/PROGRAMMER CERTIFICATION EXAM *William W. Cotterman, William J. Horne*
	HUMANISTIC PERSPECTIVES ON COMPUTER CENTER MANAGEMENT *Jack Stone*	GUIDELINES FOR COST ACCOUNTING PRACTICES FOR DATA PROCESSING *Norman Statland*	COMPUTING AT LOS ALAMOS IN THE 40'S AND 50'S *J. B. Harvill*	
	COMPUTER SYSTEMS IN HEALTH CARE DELIVERY AND MEDICAL LABORATORIES *William J. McClain*	EDUCATION FOR MEDICAL INFORMATION SCIENCE *Richard Pogue*	CODASYL VS. MUMPS FOR MEDICAL DATA BASE MANAGEMENT *Gio Wiederhold*	COMPUTER TECHNOLOGY IN THE INFORMATION/LIBRARY FIELD *Marilyn Johnson*
	SOCIETY LOOKS AT THE COMPUTER *Gordon R. England*	PRIVACY AND SOCIAL ISSUES *Herbert B. Safford*	UNETHICAL CONDUCT IN COMPUTER SCIENCE AND TECHNOLOGY *Donn B. Parker*	

PROFESSIONAL SEMINARS	COMPARING DATA BASE SYSTEMS *William E. Linn and Thomas F. Meurer* CULLINANE CORPORATION
	MICROPROCESSORS *Adam Osborne* OSBORNE & ASSOCIATES, INC.
	SOFTWARE DESIGN TECHNIQUES *Peter Freeman and Anthony Wasserman* SOFTWARE ENGINEERING CONSULTANTS
	INTRODUCTION TO COMPUTER NETWORKS *Ira W. Cotton* COMPUTER NETWORK ASSOCIATES

The new DAC standard. Analog Devices' complete 10-bit monolithic DAC.

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You can pay at least twice as much for a 10-bit IC D/A converter and still not get the degree of accuracy and stability of our new AD561. Selling for less than $10, the AD561 sets a new standard of price and performance for the other guys to shoot for.

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And the AD561 joins the industry's 12-bit IC DAC standard, AD563.

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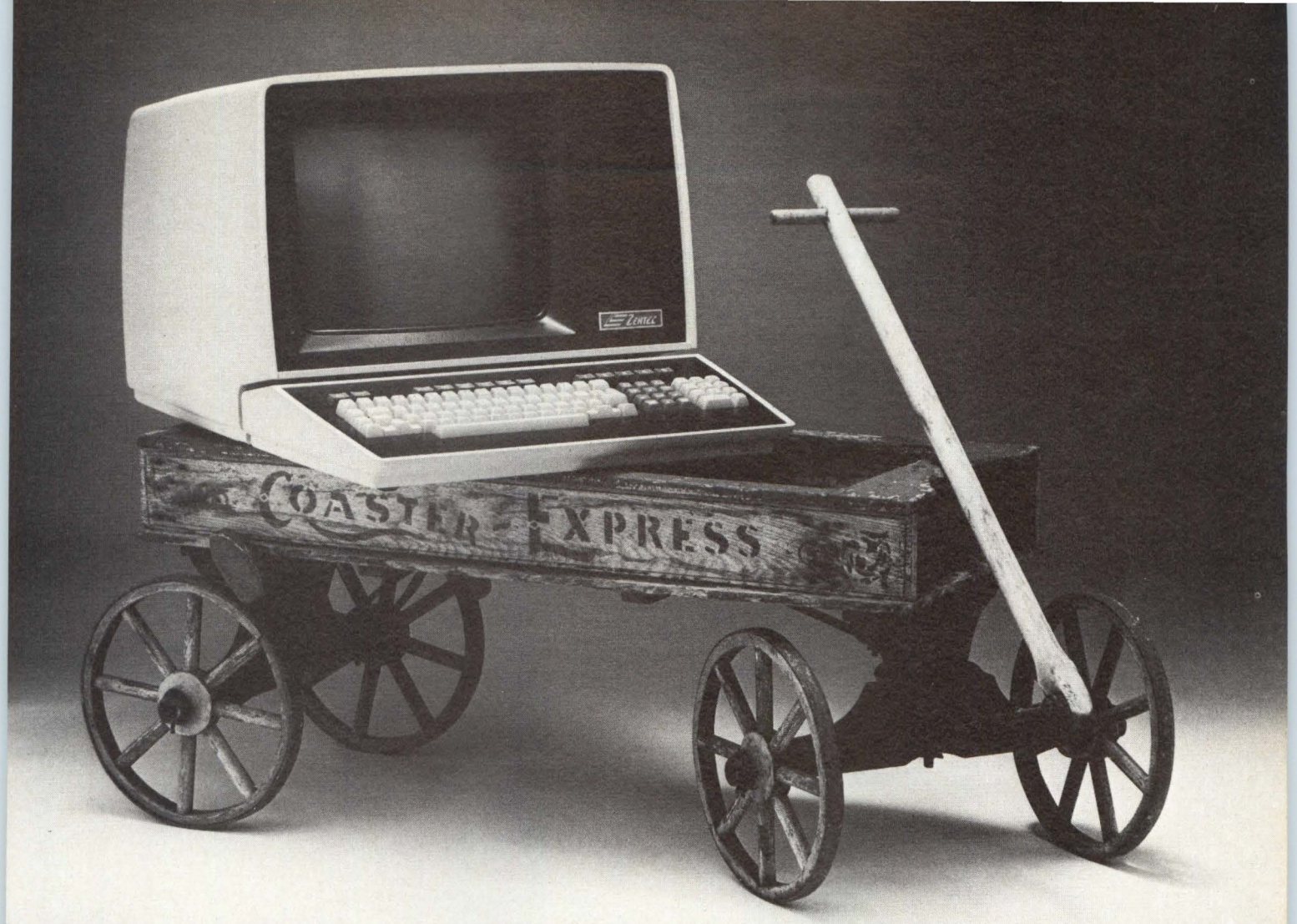
CONFERENCE AT A GLANCE (continued)

WEDNESDAY

	9:00 - 10:30	10:45 - 12:15	2:00 - 3:30	3:45 - 5:15
COMPUTER SCIENCE AND TECHNOLOGY	ANSI/SPARC DATA BASE MANAGEMENT SYSTEM FRAMEWORK *Beatrice Yormark*	DATA BASE STRUCTURE AND ORGANIZATION *Margaret Butler*	DATA BASE APPLICATIONS *J. Shirley Henry*	DATA BASE MANAGEMENT AND THE FUTURE *Lorraine Duvall*
	ARCHITECTURE FOR PATTERN RECOGNITION APPLICATIONS *Tadao Ichikawa*		DISTRIBUTED FAULT-TOLERANT MICRO-PROCESSOR SYSTEMS *Stephen S. Yau*	CM*: A MULTI-MICRO-PROCESSOR COMPUTER SYSTEM *Samuel H. Fuller*
	APPLICATIONS OF COMPUTER NETWORKS *Susan Poh*	DATA COMMUNICATION POLICY AND ITS IMPACT ON THE CONSUMER *Robert R. Korthage*	PACKET-SWITCHED NETWORKS *Saroj Kar*	INTERNATIONAL DATA COMMUNICATIONS — A MANAGEMENT PERSPECTIVE *Noel Zakin*
	COMPUTER SYSTEMS: A GLOBAL VIEW *Roger M. Firestone*	SOFTWARE VALIDATION *Edward V. Resta*	PROGRAMMING LANGUAGES: HIGH-LEVEL PROGRAMMING FOR LOW-LEVEL MACHINES *Dennis J. Frailey*	PROGRAMMING LANGUAGE: THEORY *Nancy Betz*
MANAGEMENT AND APPLICATIONS	AUDITING THE DATA CENTER: A MANAGEMENT APPROACH *John R. Kennedy*	WHY MANAGERS FAIL *James F. Towsen*	EXECUTIVE SEARCHES IN THE DATA PROCESSING INDUSTRY *Nat Turner*	DATA BASE DESIGN FOR DECISION SUPPORT SYSTEMS *Howard L. Morgan*
	EMERGING LEGAL ISSUES AND IMPACTS OF ELECTRONIC DATA PROCESSING	COMPUTER TECHNOLOGY FORECAST THROUGH 1985	PROGRAMMABLE CALCULATORS IN BUSINESS *Julius S. Aronofsky*	
	CONTINUING EDUCATION FOR THE COMPUTER SPECIALIST *Ben Knowles*	EDUCATION FOR SPECIALISTS IN THE INFORMATION AGE *Della T. Bonette*	COMPUTER SCIENCE PROGRAM ARTICULATION *Ronald P. Rhoten*	COMPUTERS IN THE PETROLEUM INDUSTRY *Olin G. Johnson*
	PERSONAL COMPUTING: HISTORY AND FORESEEABLE FUTURE *James Warren*		HARDWARE OF THE COMPUTER HOBBY MARKET *Adam Osborne*	

PROFESSIONAL SEMINARS	THE DATA BASE ADMINISTRATOR *John K. Lyon and Harold S. Schwenk* BGS SYSTEMS, INC.
	INTRODUCTION TO SOFTWARE PHYSICS *Kenneth W. Kolence* INSTITUTE FOR SOFTWARE ENGINEERING
	STRUCTURED DESIGN *Edward Yourdon* YOURDON, INC.
	EDP PROFESSIONAL DEVELOPMENT *Larry K. Grodman* Q.E.D. INFORMATION SCIENCES, INC.



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The 9003 offers you assurance of a system that just won't be obsoleted. Because of special features like user programmability and flexible bus architecture. A system that does exactly what you want, the way you want it done. User customized functions may even be added... in either software or firmware.

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CIRCLE 144 ON INQUIRY CARD

CONFERENCE AT A GLANCE (continued)

THURSDAY

	9:00 - 10:30	10:45 - 12:15	2:00 - 3:30	3:45 - 5:15
MANAGEMENT AND APPLICATIONS	ARCHITECTURE FOR DATA BASE MANAGEMENT *Gerald T. Capraro*	TEXT PROCESSING SYSTEMS *Michael J. McGill*	INFORMATION SYSTEMS: PERFORMANCE ORIENTED DESIGN AND EVALUATION *Alfred G. Dale*	
	FAULT-TOLERANT COMPUTING — I *Francis Mathur*	FAULT-TOLERANT COMPUTING — II *T. R. N. Rao*	COMPUTER ARCHITECTURE DESIGN *James E. Brown*	
	REMOTE TERMINAL EMULATION *Marshall D. Abrams*	PERFORMANCE EVALUATION *Anita Cochran*	SPECIAL MEMORY ARCHITECTURES *William E. Cantrell*	
	SOFTWARE FOR USERS AND MANAGERS *William Burns*	THEORY OF COMPUTING *Ranan Banerji*		
COMPUTER SCIENCE AND TECHNOLOGY	NATIONAL COMMISSION ON ELECTRONIC FUND TRANSFERS REPORT *William A. Fenwick*			
	LEASING, CONTRACTS AND INVESTMENT *Louis J. Brocato*	MANAGEMENT VIEW OF DATA BASE SYSTEMS *Andrew Whinston*	THE COMPUTER IN MANAGEMENT AND BUSINESS *Art Dubnow*	
	OPTICAL CHARACTER RECOGNITION: IMPACT OF MATURING TECHNOLOGY ON FUTURE APPLICATIONS *Herbert F. Schantz*	INDUSTRIAL APPLICATIONS OF COMPUTER SYSTEMS	SIMULATION METHODS	
	PERSONAL COMPUTING SOFTWARE *William Gates*		PERSONAL COMPUTING SYSTEMS *Roger L. Mills*	TRENDS IN COMPUTER STORES *David Wilson*

PROFESSIONAL SEMINARS	DISTRIBUTED DATA BASE NETWORKS *Leo J. Cohen* PERFORMANCE DEVELOPMENT CORPORATION
	STRUCTURED INFORMATION *Robert B. Ware* WARE ASSOCIATES
	HOW TO DEVELOP A LONG-RANGE DATA PROCESSING PLAN *Ben Knowles* BRANDON SYSTEMS INSTITUTE, INC.

Compare the new Sanders Graphic 7 with other interactive terminals.

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CIRCLE 43 ON INQUIRY CARD

Moving into microprocessor-based product development...

doesn't have to be a costly, time-consuming business.

Now Tektronix introduces the 8002 Microprocessor Lab, to help you meet your project deadlines and save on some of the spending.

Featuring an innovative multiple-processor architecture, the 8002 software development system supports a variety of microprocessors: at introduction, the 8080 and the 6800; next the Z-80 (available late summer 1977); then an expanding selection. Assembler software for two components is provided from those available at the time of purchase, and software for each additional microprocessor may be added optionally with a minimum of added expense.

Follow Your Own Direction

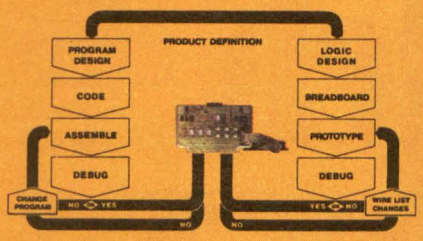
Now it is no longer necessary to buy a new microprocessor development aid each time you decide to use a different microprocessor chip. You and your team don't need to go through a new learning cycle with your equipment each time, either.

The 8002 can also save you time with several features that ease the task of program creation: a text editor that simplifies software entry and revisions, an assembler with macro capability, and dynamic trace for software debugging.

Integrate As You Go Along

Since microprocessor-based program creation and prototype design typically go hand in hand, the 8002 offers three progressive option levels for program emulation and debugging, prototype emulation and debugging, and real-time prototype analysis.

The 8002 Program Emulation and Debugging System, which adds an emulator processor and software for a selected microprocessor, enables the developmental software to be run, tested, changed, traced, and debugged on the desired microprocessor. The emulator microprocessor is identical to the microprocessor in the designer's



prototype; if the software is to be executed on an 8080 in the prototype, for example, an 8080 micropressor chip is used in the emulator processor.

The 8002 Interactive Prototype Emulation and Debugging System adds a Prototype Control Probe for a selected microprocessor. With the probe inserted into the prototype, developmental software and hardware may be tested, traced, and debugged together.

The 8002 Real-Time Prototype Analyzer System adds real-time trace and an 8-channel Analyzer Probe. At this level bus transactions and events external to the microprocessor may both be monitored.

From the Instrument Company

One final advantage: the Tektronix name. Tektronix has always been responsive to the instrumentation needs of the design engineer . . . and the 8002 Microprocessor Lab is no exception. Its ability to deal with a number of different microprocessors, its many convenience features for software development, and its capabilities for software/hardware debugging, make it a unique design tool.

As a leading electronics instrument company, Tektronix offers you a full line of options and peripherals, from the three 8002 option levels . . . to PROM programming facilities for the 1702 or the 2704/2708 MOS PROMs . . . to a line printer and choice of system terminals.

Backed by years of experience, Tektronix also offers you a rare commodity in the field of microprocessor development tools: local Field Engineers and local service. A nation-wide network of Field Offices and Service Centers is ready to help you realize the full benefits of the 8002.

For more information or a demonstration of this new software development tool, write Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077.

For availability outside the U.S., please contact the nearest Tektronix Field Office, Distributor, or Representative.

The 8002... with multiple microprocessor support.

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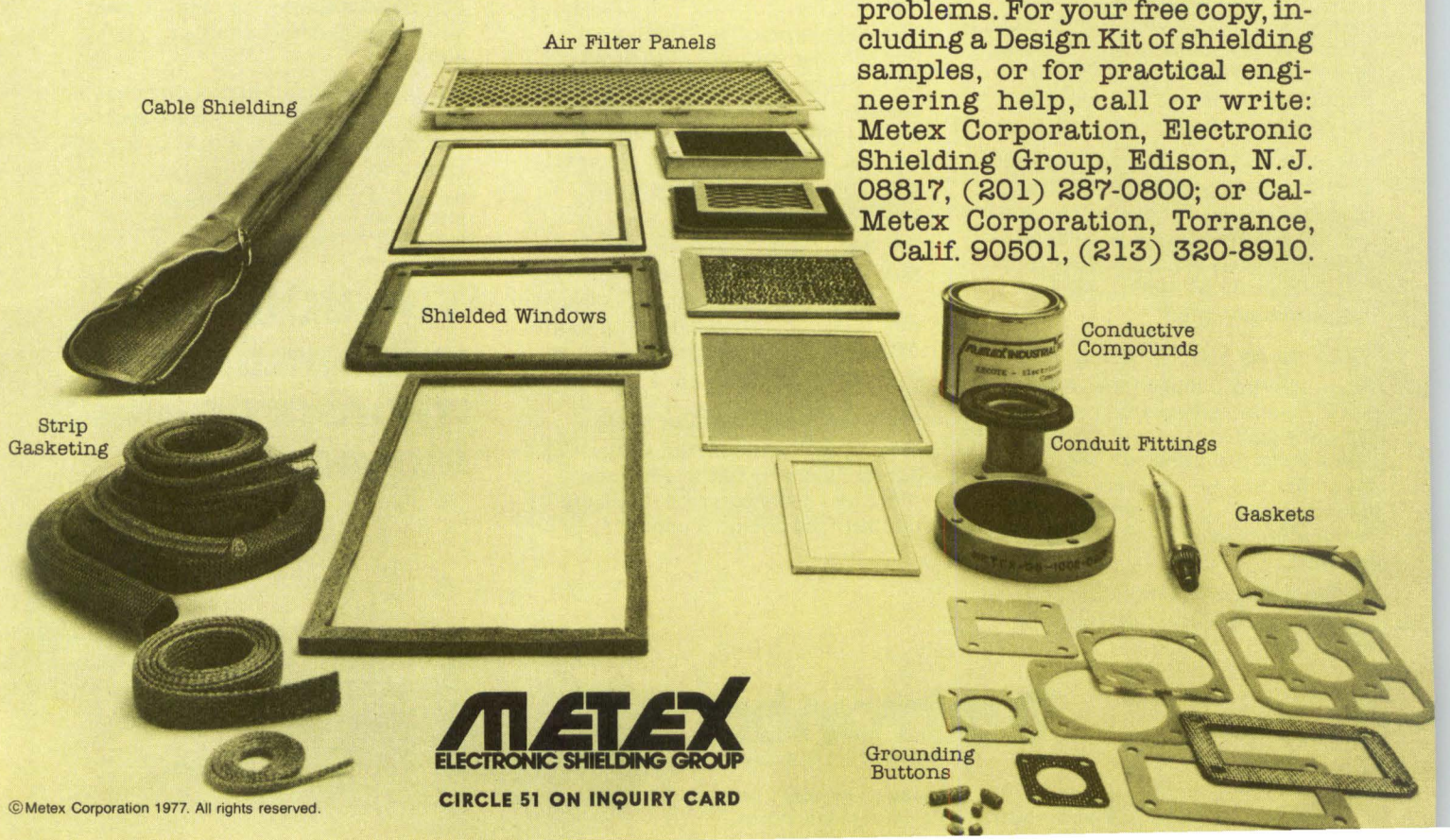
We've packed a wealth of EMI/RFI shielding information into an application brief covering practical solutions to all electromagnetic interference problems. For your free copy, including a Design Kit of shielding samples, or for practical engineering help, call or write: Metex Corporation, Electronic Shielding Group, Edison, N.J. 08817, (201) 287-0800; or Cal-Metex Corporation, Torrance, Calif. 90501, (213) 320-8910.



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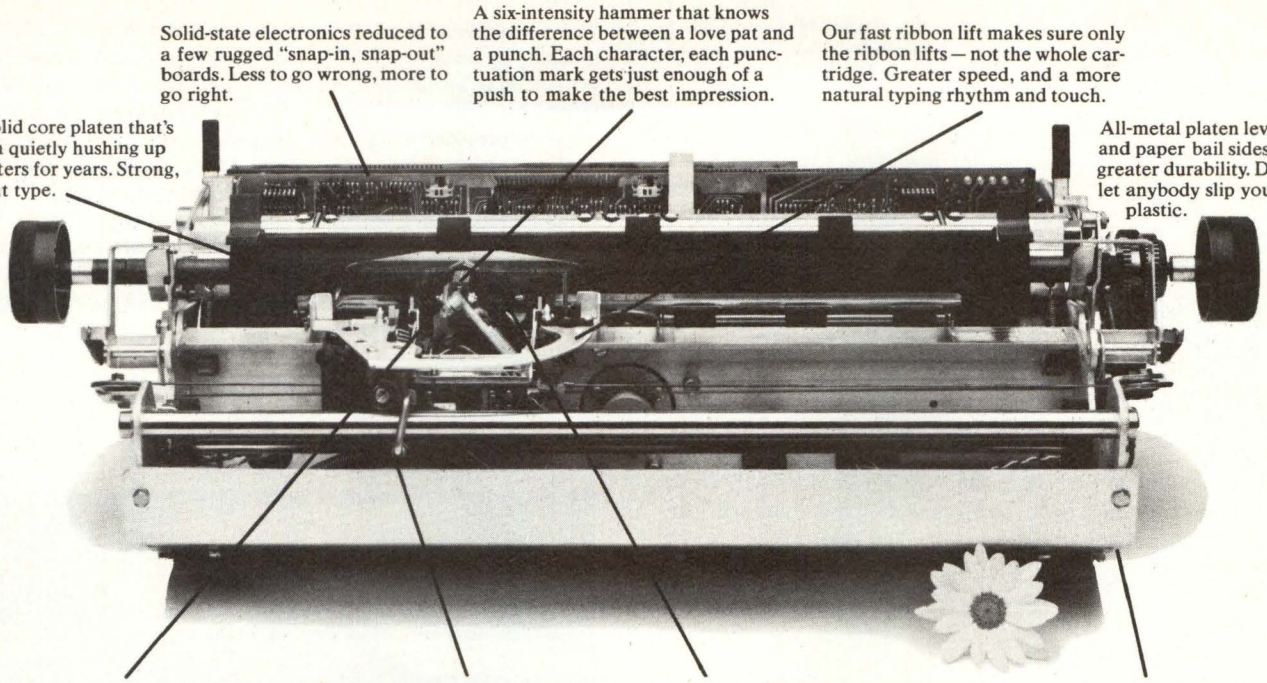

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Qume just believes continuity of product is everything. Savings in design, spares provisioning, training. So all Qume products are part of a continuing family. Not a designer-gone-berserk whim factory.

That's why the brand new 1976 Sprint Micro 3 pictured above is basically the same as the first Qume character printer we ever built. Each and every mechanical part is retrofittable, from the six-intensity hammer to the smooth-sailing carriage ball bearings.

So that any computer, terminal, or word processing system builder can buy Qume printers with the comforting knowledge that he'll face no printer-switching in midstream.

It's an interesting philosophy. (Made a big name for a small German car manufacturer a while back.)

And it's a sound philosophy we're committed to. Whether it's the industry's first true microprocessor-controlled character printer, our Sprint Micro 3. Or Qume's new WideTrack™ — 26 inches of bi-directional printing power.

All well and good, you might observe, but why buy Qume?

Because our unobsolescence philosophy is part of The Plan. A plan built on one simple rule: We don't compete with our customers. We don't make WP systems. We don't make terminals. We don't make computer systems. We have only one business — the printed word. And you get the best product we'll ever make.

Which leads us to believe, the only thing obsolete about Qume is its competition.

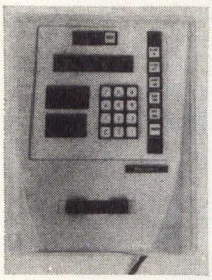
Qume®
the printed word

2323 Industrial Parkway West, Hayward, CA 94545 415/783-6100

CIRCLE 18 ON INQUIRY CARD

NCC PRODUCT REVIEW

DATA ENTRY TERMINALS



A multipoint line data entry terminal—called a data action tracker—and its associated EIA RS-232-C system interface unit provide a link between data source and computer. The basic unit accepts punched badges or cards but more than 25 options are available. It can accept variable numeric and sensor data from BCD scale interfaces, monitor inventory and material control, and keep accurate time and attendance records. Bus architecture utilizes plug-in PC boards for convenient servicing. A static optical badge reader and CMOS logic allow operation in rugged environments. The interface can be optionally configured with a time and attendance master clock and a secondary port. **Panasonic Co,** 2960 Hart Dr, Franklin Park, IL 60131.

See at Booth 1044

Circle 345 on Inquiry Card

LINE PRINTER FAMILY

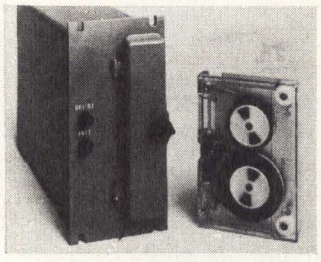
6000 series fully-formed character line printer models have speeds of 75, 150, 300, and 600 lines/min, respectively, but share an 85% parts commonality. A 1-piece lightweight print band in choice of 48, 64, 96, and 128 characters is operator changeable within 1 min. Std features include non-shifting hammer mechanism, modular 2-part mechanism design, compact size, universal power supply, test print, automatic motor control, forms-feed control, single-line feed control, out-of-paper sensor, and 2-channel direct access VFU. Optional features include electronic VFU for automatic recording and utilization of 2, 8, or 12 channels of format instructions; paper jam sensor to automatically terminate printing in unattended operation; line counter for monitoring printer usage; and 136-col capacity for specialized applications. **Centronics Data Computer Corp,** Hudson, NH 03051.

See at Booth 1238

Circle 346 on Inquiry Card

DATA CARTRIDGE TAPE DRIVE

Model 6413 Cartridge Raycorder, for use with 0.25" (0.64 cm) data cartridges, features a patented direct-drive system, together with associated electronics, which provide high data integrity. Conductive heat flow to the chassis eliminates hot spots for longer operating life and eliminates the need for forced air cooling. In addition, components are hard-mounted to a cast aluminum chassis for precision alignment and superior performance. The unit is fully ANSI/ECMA compatible. Modular packaging provides a variety of configurations to meet varying requirements. The unit records on the 3M DC300A cartridge at 1600 bits/in PE to store 23.04 x 10^6 bits (unformatted). **Raymond Engineering Inc,** Middletown, CT 06457.



See at Booth 1820

Circle 347 on Inquiry Card

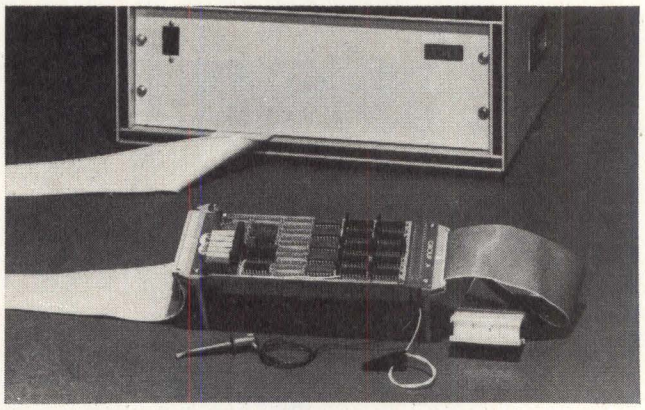
DISC STORAGE UNIT

With capacities from 72M to 500M bytes and a transfer rate of 806k bytes/s, the PS 5 uses an exchangeable disc pack with 9 data surfaces and one surface for servo information to provide 72M- and 144M-byte capacity; expansion to 500M bytes is provided by a fixed disc pack with 19 data surfaces and one surface for servo data. Made up of cabinet, disc pack drive mechanism, voice coil positioning systems, read/write heads, and associated electronics, power supply, and device interface electronics, the unit simultaneously positions all read/write heads to one of the possible positions using an electromechanical positioner. **Siemens Corp,** 3 Computer Dr, Cherry Hill, NJ 08002.

See at Booth 1199

Circle 348 on Inquiry Card

COMPUTERIZED LOGIC ANALYZER



Functioning as a peripheral to the company's microcomputer development system, which provides both full computer power and an interactive operating system, the 40-channel MDC-140 analyzer allows 1024 steps to be traced and formatted under total software control. Connection to the digital circuit to be analyzed is via either a set of 40 probes or a 40-pin DIP-clip. Probe thresholds can be adjusted in groups of 10 for any level in the ±15-V range. Four different qualifiers can be specified, combined with the analyzer's clock source or with either edge of an incoming clock signal, after which 1024 captured steps are displayed in pages of 16 lines. Line format can be binary, ASCII, hex, or symbolic—brought in from a floppy disc file and modified as needed. **American Microsystems, Inc,** 3800 Homestead Rd Santa Clara, CA 95051.

See at Booth 1051

Circle 349 on Inquiry Card

DATA ANALYZER

Rapidly pinpointing system problems, the Comtest intelligent microprocesor-based network analyzer is suited to verifying data integrity of communications systems. The portable unit weighs 24 lbs (10.8 kg) and measures 7 x 18.25 x 16.5" (17.78 x 46.36 x 41.91 cm). It normally stores both EBCDIC and ASCII disciplines in integral p/ROM modules; SDLC is available as an option. Keyboard input allows modification of std disciplines to accommodate specific system checkout needs. Containing half- or full-duplex modes, it also serves as an emulator for CPU or other terminal devices. Loop testing capability permits verifying of modem and line performance. Other features include built-in self-test, 12 commands, and 16-line, 512-char CRT display in hex pairs or English text. **Universal Data Systems,** 4900 Bradford Dr, Huntsville, AL 35805.

See at Booth 1601

Circle 350 on Inquiry Card

Now you can get our disk systems within 30 days ARO at the industry's lowest prices:

• 80 Mbytes for under $12K*
• 300 Mbytes for under $20K*

Field-proven reliability, total software support and 30-day delivery. You've come to expect them all from us. And that's why we've become the world's largest independent supplier of minicomputer disk storage systems.

Now add low price. Lower than the minicomputer manufacturer, lower than any other independent—*the lowest in the industry*. Why? Because we buy more disk drives than anyone else, and we can afford to pass the OEM discounts on to you.

The prices listed above are for complete disk systems ready to plug into your minicomputer. Each system includes our high-performance controller, an appropriate minicomputer interface and the software of your choice.

When you buy disk systems from us, you'll save a lot more than a lot of money on the purchase price. You'll save precious time. Beginning with our 30-day delivery and continuing with our responsive, customer/software support, we'll get your system up quickly—and keep it up. For complete OEM pricing information and technical details, contact the System Industries representative in your area.

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An equal opportunity employer.

535 Del Rey Avenue
Sunnyvale, California 94086
(408) 732-1650, Telex 346-459

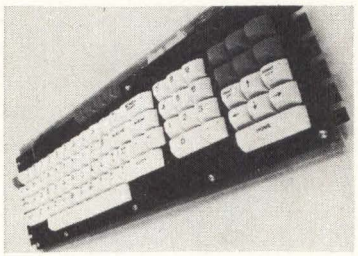
* OEM prices: 40-69 systems.

Sales/Service Representatives
Boston: (617) 492-1791. **New York:** (201) 461-3242; (716) 385-3021; (516) 299-4272; (201) 694-3334.
Washington, D.C.: (202) 337-1160. **Cincinnati:** (513) 661-9156. **Los Angeles:** (714) 752-8904. **Houston:** (713) 465-2700.
Sunnyvale HQ: (408) 732-1650. **Canada:** (416) 624-0320. **United Kingdom:** (4862) 70725.
Germany: 211-407542. **Sweden:** 08-236640. **Spain:** 45-7-5312.

NCC PRODUCT REVIEW

CAPACITIVE SOLID-STATE KEYBOARD

Low profile keyboard incorporates an n-MOS ROM keyboard encoder chip which handles either mechanical or capacitive inputs and requires only a 5-Vdc supply. The entire 110-key keyboard can be scanned in 1.1 ms. Built-in noise rejection circuit and built-in hysteresis enable the keyboard to offer a high degree of noise immunity and protection from key "teasing." Encoding capability is up to 10 bits for 110 keys and four modes per key. Selectable codes include ASCII, USASCII, Baudot, BCD, or EBCDIC. Scan time is externally adjustable from 10 to 80 μs/key. N-key lockout or N-key rollover are available without additional components. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.



See at Booth 1768

Circle 351 on Inquiry Card

ONLINE MULTIPLE PROCESSOR SYSTEM

T16/210 and T16/240 system modules consist of 22-slot card cages capable of supporting two T16 processors with up to 320k bytes of semiconductor or 128k bytes of core memory. Dual interprocessor DYNABUS™, processor boards, memory boards, I/O channels, cooling fans, and power supply are included. Up to eight device controllers can be installed in the system. Two system modules can be configured side by side to obtain a 4-processor system without program changes. The system can continue in operation while parts of it are replaced, repaired, or expanded. I/O structure is a microcoded processor controller, with block-multiplexed channels which can handle variable length transfers to buffered dual I/O port controllers. **Tandem Computers Inc,** 20605 Valley Green Dr, Cupertino, CA 95014.

See at Booth 1642

Circle 352 on Inquiry Card

BUBBLE MEMORY DATA TERMINALS

Silent 700™ model 765 portable memory terminal and model 763 send-receive terminal come with 20k bytes of nonvolatile TBM 0103 bubble memory storage, expandable to 80k bytes in 20k-byte increments. Units can access any indexed record in memory in <15 ms; if the data location in 765 memory is not known (not indexed), the character string search speed is 1000 char/s, about four times the speed of a cassette search. The 765 has a full ASCII keyboard, built-in numeric cluster, thermal printer, acoustic coupler, carrying case, and powerful editing capability, and includes ASR functions. The 763 offers all capabilities for a fixed location. Data transmission speeds can be 9600 baud. **Texas Instruments Inc, Digital Systems Div,** M/S 784, PO Box 1444, Houston, TX 77001.

See at Booth 1305

Circle 353 on Inquiry Card

COMPUTER SYSTEM

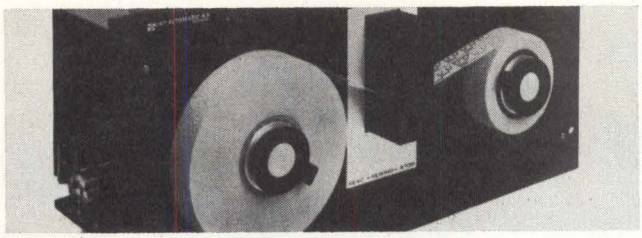
In its basic configuration, the 1400 series handles small to medium-sized business requirements, and can function as a standalone host or satellite processor. Hardware capabilities of the system 1400-2 include a high speed CPU; 16k char of user memory with system-dedicated main memory for a resident operating system; two interactive video terminals with 1728-char display; and sealed, fixed media, random access disc drive with 25M char of storage. Also included are a 300-line/min printer, and a large reel, 45-in/s (114.3 cm) magnetic tape unit with 1600 bits/in (629.9/cm). Expansion space is built-in to accommodate additional plug-in main memory and I/O devices. **Qantel Corp,** 3525 Breakwater Ave, Hayward, CA 94545.

See at Booth 1285

Circle 354 on Inquiry Card

PAPER TAPE READER STATION

Designed to meet requirements of the numerical control industry, model 27 consists of reader, spooling equipment, and electronics in an integral unit. Buffer arms and capstans have been eliminated—the spooling equipment is the sole source of tape movement, thereby minimizing tape wear. Data are read automatically into the semiconductor memory when it is less than half full; even at reading speeds of 250 char/s the memory will not normally be emptied. The station will always provide an effective stop-on-character capability even when reading at 1500 char/s and a built-in counter ensures that no characters are ever skipped or read twice. **G N T Automatic, Inc,** 440 Totten Pond Rd, Waltham, MA 02154.

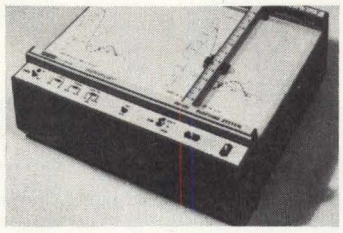


See at Booth 1176

Circle 355 on Inquiry Card

FLATBED TIMESHARE PLOTTER

Model DP-101, designed for remote timeshare applications, combines flatbed digital plotter with microprocessor controller. The 11 x 17" (28 x 43 cm) unit operates at 2" (5 cm)/s with a step size of 0.005" (0.01 cm). The controller element features vector and character generation and 16 special centered symbols in addition to the company's previously available std character set. It also offers circle generation, enhanced vector length, and the ability to perform with an offline tape cassette. Operation is at 110, 300, and 1200 baud with total interruption capability without loss of origin. Also on display are three models of the 36" (91 cm) wide DP-8, the DP-1, and the 22" (56 cm) wide DP-3 digital plotters, the MTR-4 magnetic tape reader, the PTC-5A-1 and 5A-3 controllers, and BTC-7 batch terminal controllers. **Houston Instrument,** 8500 Cameron Rd, Austin, TX 78753.



See at Booth 1193

Circle 356 on Inquiry Card

Measuring both Low-Level & High-Level Analog Signals with any Mini... Using RTP.

Let's say you have to measure signals that originate from low level transducers, like thermocouples, and some higher level signals that have been pre-conditioned by a transducer amplifier. These signals may range from ±2.5mV to ±10.24V, full scale.

This application can be handled by an RTP Bus Converter for your mini, an RTP Wide-Range Analog Input Controller, and sufficient 8-channel gate cards to accommodate the signals to be measured.

The RTP Bus Converter interfaces the Wide-Range Controller to your mini by converting your mini's parallel I/O bus to the standard RTP parallel bus. Appearing transparent to your computer, it allows the Wide-Range Controller to be directly programmed, as if it were one of the computer's peripherals. Best of all, RTP Bus Converters are available for all popular minicomputers.

The Wide-Range Controller provides the logic, power, and space for up to 16 gate cards, or 128 channels of input. Need more? With expansion chassis, you can handle up to 512 channels with one controller. Still more? Simply daisy-chain controllers with the RTP parallel bus.

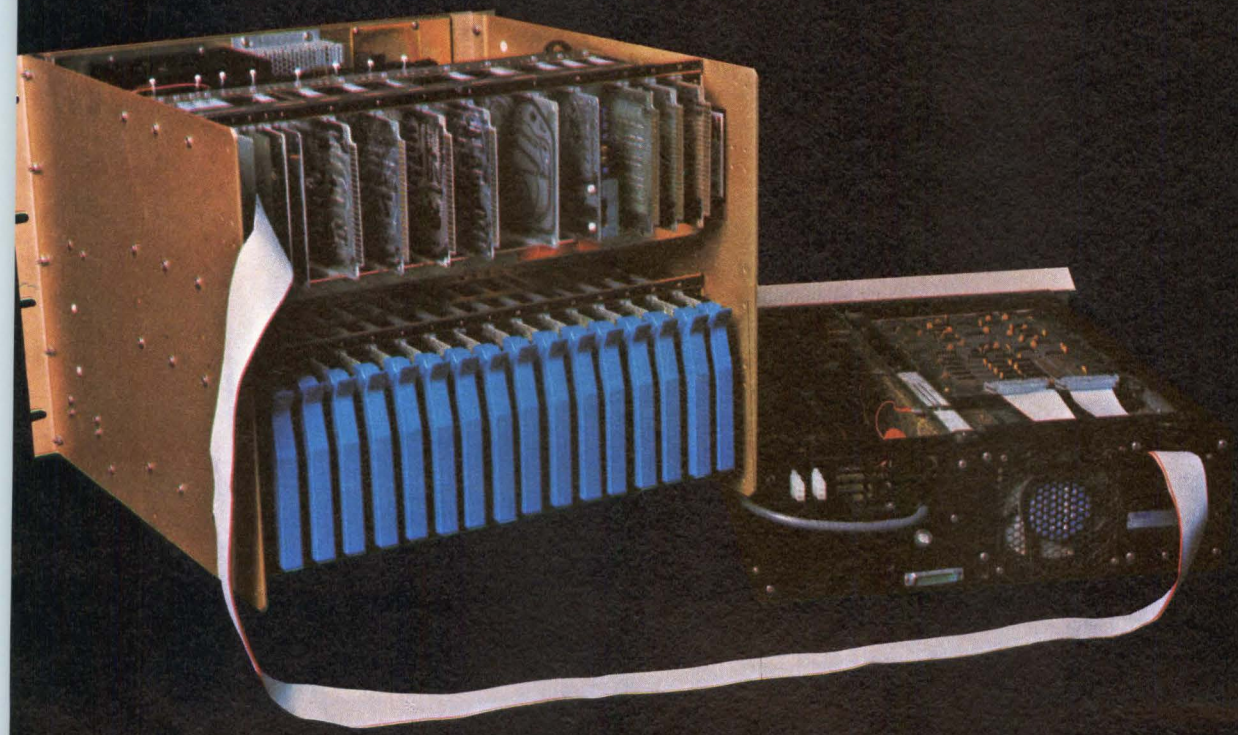
The Wide-Range Controller also allows random selection of both channel and gain at rates up to 200 sps, and uses proven reed relay scanning techniques.

There's more to RTP than our Wide-Range, though. RTP is a complete line of standard products that allows direct input and output of analog and digital signals to any popular minicomputer.

Just circle our number on the Reader Service Card, and we'll send you "Using RTP"...a concise RTP subsystem design overview.

Computer Products, inc.

Your Mini & RTP

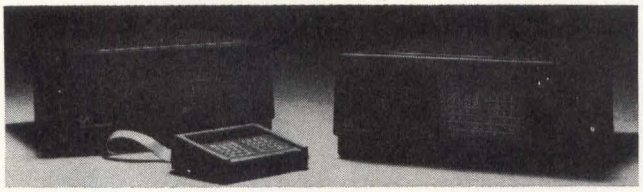


Computer Products, inc.
1400 N.W. 70th Street, Fort Lauderdale, Florida 33309 • (305) 974-5500, TWX (510) 956-9895

CIRCLE 53 ON INQUIRY CARD

NCC PRODUCT REVIEW

16-BIT MINICOMPUTER FAMILY

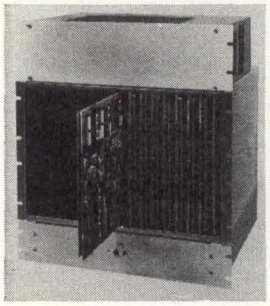


Common bus architecture enables flexibility of configuration, ease of interface, and family compatibility among the LSI 4/10, 4/30, and 4/90 Naked Mini-4 computers. Instruction repertoires are 89, 106, and 119, respectively, and optional expanded instruction sets are available. Core add-ons are available in 1k-, 4k-, 8k-, and 16k-word modules. Semiconductor memories with battery backup include combinations of RAM, ROM, p/ROM, and EPROM devices that range from 256 to 32k words/module. A distributed I/O system permits a half-card distributor to control up to eight programmed I/O or four DMA devices. Multiple distributors can be included. **Computer Automation, Inc,** 18651 Von Karman, Irvine, CA 92713.

See at Booth 1465

Circle 357 on Inquiry Card

PDP-11 COMPATIBLE CORE MEMORY



Offering significant performance enhancement for PDP-11/70 computers, the ARM 1170 is a totally transparent alternative to, or replacement for, the MJ 11 memory as used in -11/70 computers. Available in 128k-byte (32k words of 36 bits each) increments, the memory is capable to expanding computers to their maximum 4M-byte capacity. All components required to achieve expansion to the maximum can be accommodated within two computer cabinets. Throughput is enhanced by 2- or 4-way interleaving features in the memory. Using 4-way interleaving, effective cycle time is 350 ns as compared with 800 ns for the basic memory, or 1 μs for DEC memory. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.

See at Booth 1444

Circle 358 on Inquiry Card

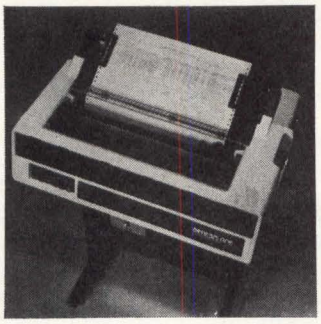
FLOPPY DISC SYSTEM

Model 3700C permits up to eight model 4000, 4300E, or 4500 video display terminals and two serial read-only printers to share access to as much as 1.5M bytes of storage. Up to six flexible drives of 242,900 characters each are available. The system is compatible with IBM 3780 terminals and Teletype® typewriters and is available as a compact single-drive cabinet or as a full-capacity pedestal unit. The pedestal may be further expanded to include a complete workstation. Recorded data are compatible with IBM 3740 data entry equipment. A BASIC programming capability will be provided to permit the system to be used in applications such as data and order entry. **Delta Data Systems Corp,** Woodhaven Industrial Pk, Cornwells Heights, PA 19020.

See at Booth 1276

Circle 359 on Inquiry Card

IBM-COMPATIBLE PRINTER



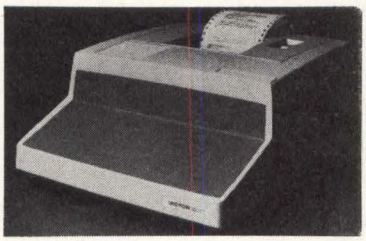
An interchangeable replacement for IBM 3284 printers, G060 interfaces directly with IBM 3271 and 3272 Mod 2 controllers and System/3 device adapters. Std features include 9 x 7 dot matrix, serial, impact character structure (approximates 10-pt type), 64-char set; 3270-compatible interface, with all electronics housed in pedestal base; 1920-char buffer; 132-char/line, 6-line/in format (40, 64, 80, or variable char/line can be programmed); and top of form positioning and vertical tabulation control of forms movement. Operation is at 60 char/s. An automatic alarm sounds when paper runs out or an operator is needed. **Genesis One Computer Corp,** 300 E 44th St, New York, NY 10017.

See at Booth 1866

Circle 360 on Inquiry Card

LABEL AND TICKET PRINTER

Designed for OEMs, the standalone 5000 series of sprocket-fed terminals are compatible with most systems. Each unit is equipped with a microprocessor controller and double line buffer for incoming data, which may be received at up to 9600 baud. ASCII inputs are parallel for the model 5010-463, RS-232 for the 5011-463, and current loop for the 5012-463. Terminals have either 115-V, 60-Hz, or 230-V, 50-Hz power requirements. Units print up to 26 char/line on labels, tickets, or multipart forms. Sprocket feed assures exact registration. A command code enables characters to be expanded and/or printed in red for highlighting and headlining. Device is packaged in a 12 x 18 x 6" (30.48 x 45.72 x 15.24 cm) desktop case. **Victor Comptometer Corp,** 3900 N Rockwell St, Chicago, IL 60618.



See at Booth 1771

Circle 361 on Inquiry Card

BUFFERED TAPE CASSETTE TERMINAL

Featuring an Intel 8080A microprocessor for control of buffering, editing, and communications, the model 5000 features high speed search and powerful edit functions as well as full communications capability. It uses read-after-write and CRC for error detection and has extensive data correction routines. It conforms to ANSI/ECMA standards, with tape speeds up to 120 in/s (305 cm/s) on cassettes which hold 221k char of formatted data. Transmission is half- and full-duplex, asynchronous serial-by-bit-by character. Speeds are switch selectable at six points from 110 to 2400 baud. The unit connects directly to CRT terminals, keyboard printers, and other send/receive serial data interface devices. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.

See at Booth 1753

Circle 362 on Inquiry Card

WHEN IT'S FINALLY ON THE SCREEN, YOU DESERVE FAST HARD COPY.

Gould's electrostatic printer/plotter is the fastest graphic hard copy peripheral available today for your Tektronix 4000 Series interactive graphic terminal. You get permanent graphics direct from the terminal in as little as 4 seconds, regardless of image complexity. In an on-line CPU configuration, you can plot at up to 3.25 paper in./sec. and print at up to 1600 lines per minute.

Yet Gould's hard copy still possesses exceptional resolution and extremely high contrast. Only Gould offers you both unmatched speed and unsurpassed image quality.

And Gould lets you select a 0° or 90° image orientation at will. In 90° mode, images are enlarged up to 72%. You are able to select 1024 or 2048 point sampling and high or low speed graphic operation, letting you optimize image size, resolution and speed.

As with all Gould systems, your software is all-Gould. You never need worry about third party variables.

Gould images don't deteriorate. The system requires no warm-up. Gould paper costs a fraction of silver paper. Up to 2 interfaces are accommodated in the plotter, allowing you to use it with up to 8 Tektronix terminals or 4 terminals and a minicomputer, or 2 minicomputer CPU's.

Your CRT work deserves the best hard copy you can get. You get it from Gould.

For more information and a sample graphic output, contact Gould Inc., Instrument Systems Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Or Gould Advance Ltd., Raynham Road, Bishop Stortford, Herts, United Kingdom.

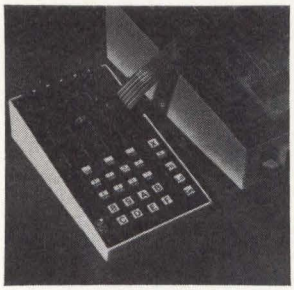
FOR FREE BROCHURE CALL GOULD TOLL-FREE AT (800) 325-6400 Ext. 77.
In Missouri: (800) 342-6600

CIRCLE 54 ON INQUIRY CARD

GOULD
The product development company

NCC PRODUCT REVIEW

MINICOMPUTER DATA ENTRY/DISPLAY DEVICE



Developed as a general-purpose, microcomputer device for users who prefer hexadecimal coding, the Hex Keypad can be used either with the company's MMD-1 or as a separate I/O device. The keyboard section generates 4-bit hex code corresponding to the legends. If two or more keys are struck simultaneously, the value of the highest order will be output, thereby preventing generation of false codes and simplifying the processing of data. The keypad can also be jumper selected for device codes 0 through 7. The display section of the keypad provides for three separate pairs of displays, each fully decoded and latched, which can be individually jumper selected for device codes 0 through 7, or wired to any decoding hardware of your construction. **E & L Instruments, Inc,** 61 First St, Derby, CT 06418.

See at Booth 1268

Circle 363 on Inquiry Card

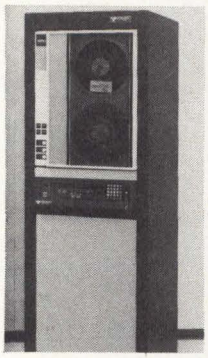
MATRIX PRINTER TERMINAL

Model 1660 features a 1200-baud transmission rate, 200-char/s print speed, 100% duty cycle 9-wire ballistic matrix head with extra wide head to paper gap, microprocessor control to provide incremental and bidirectional printing, 7 x 9 dot matrix u/lc print capability, and versatile forms handling. The terminal communicates in and is compatible to ASCII code devices. Functional capabilities reside in preprogrammed ROMs. A front control panel allows the operator to select baud rate, parity, duplex, automatic carriage return, reverse channel select, and diagnostic test. Indicators on the panel allow error detection and terminal operating modes. **Diablo Systems Inc,** 24500 Industrial Blvd, Hayward, CA 94545.

See at Booth 1479

Circle 364 on Inquiry Card

OFFLINE PLOTTING SYSTEM



System translates vector plot data to raster format for fast electrostatic plotting on any company plotter. Data can be in the form of vector, intermixed vector, and raster or simultaneous print/plot information. Components include an intelligent vector processor with operator panel and display, magnetic tape deck, one plotter or printer/plotter, and Versaplot-PPEP (pen plotter emulation program) software which provides a set of FORTRAN-callable subroutines. Tape decks handle 9-track, either 800- or 1600-bits/in (315 or 630/cm) formats. Both operate at tape speeds of 45 in/s (114 cm) and rewind speed of 150 in/s (381 cm). At speeds up to 2 in/s (5.08 cm), plotters plot areas up to 34 ft²/min (3.16 m²). All models use dual array writing heads. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.

See at Booth 1165

Circle 365 on Inquiry Card

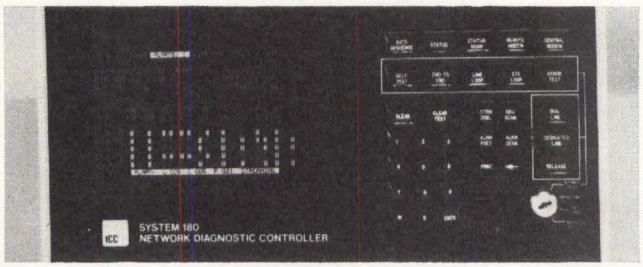
INTERACTIVE GRAPHICS TERMINAL

A microcomputer and display memory increase local performance and reduce host computer support for this intelligent device in the display and manipulation of computer graphics output. Functions such as pan, zoom, cursor tracking, grid generation, black on white and white on black display, alphanumeric display, and write-through (erase and add) are enabled. Basic configuration is a processor, display screen, RS-232-C interface, and full ASCII keyboard which includes function and cursor controls. Supporting software handles display features, keyboard, cursor pad, and the RS-232-C interface control. Optional Plot 10 compatible software is available as well as various compatible software for selected host computers. **California Computer Products, Inc,** 2411 W LaPalma Ave, Anaheim, CA 92801.

See at Booth 1233

Circle 366 on Inquiry Card

NETWORK DIAGNOSTIC CONTROLLER



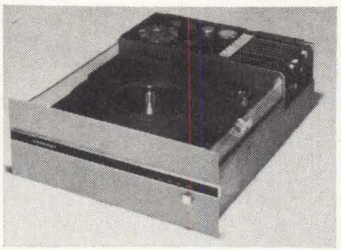
System 180, a simplified central site monitoring and diagnostic system, operates without highly trained technical personnel or specialized programming. It provides real-time information and status on malfunctions or abnormal situations in data lines, modems, power, or terminal controllers located at remote sites. All monitoring operations can be performed at the central site console without involving personnel at the remote sites. English language instructions displayed on a video screen lead the operator through a step-by-step testing procedure with results displayed on the screen. An alarm message in the screen and an audio tone signal abnormal conditions. The system is available for rack or console mounting or as a desktop unit. **International Communications Corp,** 8600 NW 41st St, Miami, FL 33166.

See at Booth 1360

Circle 367 on Inquiry Card

MOVING-HEAD DISC DRIVES

Up to 70M bytes of data can be stored at rates of 1M bytes/s by the series 5300 fixed-cartridge disc drives. They have unformatted capacities ranging from 14M bytes in the 1-disc version up to 70M bytes in the 3-disc model. Each surface has two 350-track/in (138/cm) cylinders with a recording density of 6000 bits/in (2362/cm). A sealed enclosure eliminates expensive filters and blowers, yet allows operation in locations previously considered unsuitable for disc drives. Using the "Winchester" technique, a dual-head carriage is driven in an arc by a d'Arsonval-type actuator which rapidly and accurately positions the heads. Head positioning is controlled by prerecorded servo-tracks on the bottom of one disc. **Kennedy Co,** 540 W Woodbury Rd, Altadena, CA 91001.

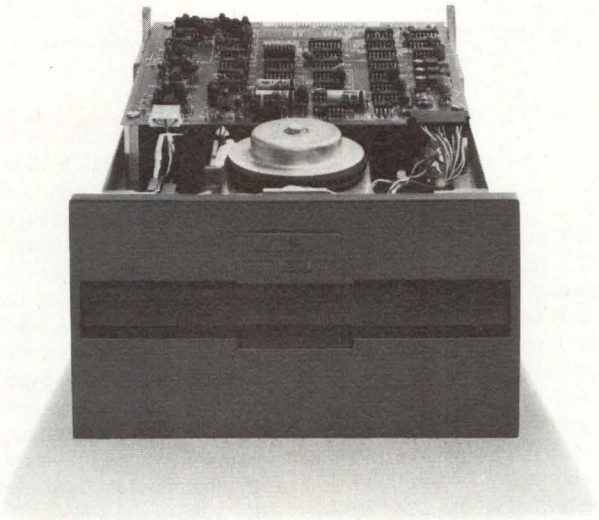


See at Booth 1785

Circle 368 on Inquiry Card

FLEXIBLE DISK DRIVES:

GSI THE WINNER: PRICE
GSI THE WINNER: DELIVERY
GSI THE WINNER: QUALITY



The flexible disk drive winner—GSI's FD 110. Our price in production quantities starts in the low $300 range per unit. Unlike others we deliver in 30 days, not 90.

But GSI has more going for it than just price and delivery.

While other makers have been toying with bells and whistles, we've put together all the high quality features you'll need in an advanced flexible disk drive.

It accommodates up to 6.4M bits of information using MFM or M²FM encoding techniques.

It is fully IBM compatible and will read and write IBM 3740 formatted diskettes.

It also has up to 8 drive daisy-chaining ability, select separation of clock and data, track "00" photosensing, automatic diskette ejection as well as a fail-safe interlock.

Quality features come from experience. We're the only flexible drive maker who over the years designed systemized equipment for some of the world's largest computer system manufacturers. More than 2,000 GSI system configurations are working worldwide and better GSI peripherals for those systems have been developed simultaneously. Maybe that's why we're recognized the world over as second to none.

So now that you know, go with the winner, it sure makes a difference.

Send for our new peripherals brochure. FREE.

NAME_____ DATE_____

COMPANY_____

ADDRESS_____

CITY/STATE/ZIP_____

G.S.I., 1440 Allec Street, Anaheim, California 92805

GENERAL SYSTEMS INTERNATIONAL, INC.

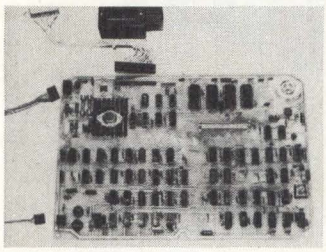
1440 Allec Street, Anaheim, California 92805, (714)956-7183, Telex 69-2488

CIRCLE 55 ON INQUIRY CARD

NCC PRODUCT REVIEW

PRINTER INTERFACE BOARD

C-40 converts Teletype® model 40 SSI interface to that of a Centronics® printer with plug-to-plug compatibility without software or hardware changes. Type -A supplies power and is mounted inside the model 40 cabinet beneath the printer mechanism; -B requires an external source of dc power and can drive a remote printer from as far as 2000 ft (610 m). Std features of both include full line buffer for burst mode load operation (up to 500 kHz), continuous or automatic turn-off motor control, up to 190 printable characters (with extended font), and strap-selectable parity. Effective print rates vary from 500 lines/min with 48-character set to 220 lines/min with 96-character set. **Innovative Electronic Systems,** 5951 NW 151 St, Miami Lakes, FL 33014.



See at Booth 1781

Circle 369 on Inquiry Card

REFRESH GRAPHIC TERMINALS

Std features of the Megagraphic 500 series include 12-bit (4096 x 4096) screen resolution, 21″ (53 cm) electromagnetic monitor, hardware blink, translation, dashed lines, and sharp constant intensity vectors. Std screen spot size is 15 mils with a 10-mil option. Also included are general-purpose Nova 3 minicomputer, expandable to 128k words, u/lc keyboard with 20 function keys, and operator workstation/desk. A high speed microprocessor-based graphic display unit occupies two computer slots and provides digital to graphic conversions, control, and display functions. Std and user definable hardware character sets are available. **Megatek Corp,** 1055 Shafter St, San Diego, CA 92106.

See at Booth 1216

Circle 370 on Inquiry Card

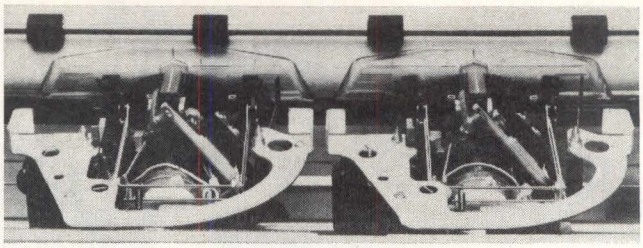
PRINTING RESPONSE TIME MONITOR

A hardware monitor designed to measure response time of terminals, PRTM 102 is capable of measuring and recording response time information on two separate terminals (expandable to four with options). Response time information is printed, automatically or on command, on a built-in 20-col alphanumeric printer to give a permanent sequential record. Front panel switches allow users to set a response time threshold which, when exceeded by a transaction, causes printing of transaction time and time of day that it occurred. The monitor uses optical couplers to pick up the transaction time information. The printer is a dot matrix alphanumeric impact printer that uses ordinary 2.25″ (5.72 cm) adding machine paper. **Questronics, Inc,** 3596 S 300 W, Salt Lake City, UT 84115.

See at Booth 1645

Circle 371 on Inquiry Card

2-HEADED CHARACTER PRINTER



The Micro 3 TwinTrack is designed to solve complicated printing problems by providing two daisywheel printheads operating independently, thereby doubling the character sets or number of online characters available. The unit can print with both heads over a print area of 15.3″ (38.9 cm) wide, which permits legal-sized sheets to be used. With two different wheels and the max of 192 char, up to 45 char/s can be achieved; two identical printwheels can generate 75 char/s. Usable print area can be increased to a full 26.3″ (66.8 cm) width by using identical printwheels. 10- or 12-pitch or proportional spacing daisy wheels can be used. **Qume Corp,** 2323 Industrial Pkwy W, Hayward, CA 94545.

See at Booth 1754

Circle 372 on Inquiry Card

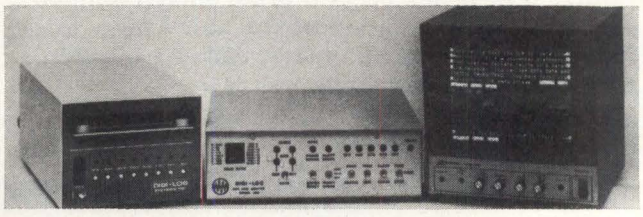
ADD-IN MEMORY STORAGE CARD

NS-11 series, 32k x 18-bit, double-density cards plug directly into PDP-11/04, /05, /10, /34, /40, /45, /50, and /55 computers. Each card replaces two 16k DEC memory cards in the backplane assembly, resulting in space savings, increased reliability, and lower cost. Each card provides up to 64k bits and occupies one system unit slot. The memory has a 375-ns access time and 500-ns cycle time. I/O device addresses are switch-settable to 1k or 2k, expanding the addressable memory space to 31k, or with memory management to 127k. All memory devices are in sockets for simplified field maintenance or memory expansion. 100% burn-in at both component and system level assures reliability. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

See at Booth 1565

PROGRAMMABLE DATA COMMUNICATION STORAGE UNIT

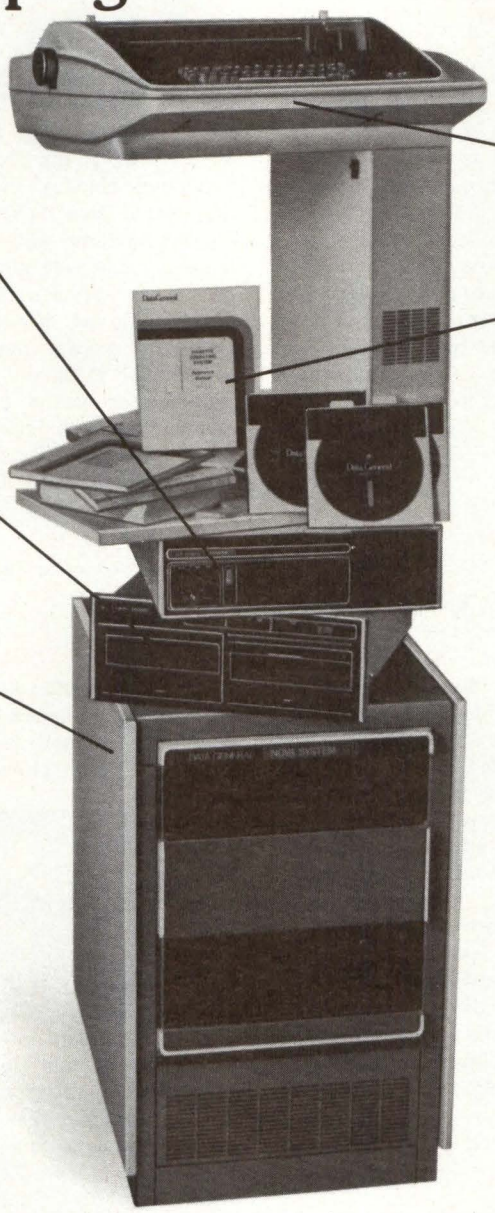
A 1M-byte storage device, Tapetrap provides programmable, unattended monitoring techniques for fast fault isolation. It is operator settable to record one track (250k characters) and stop, record the whole tape (1M characters) and stop, or record continuously on an endless loop. The last option provides a constant record of the last 1M characters monitored. A trap sequence of up to 16 characters can be entered via an integral keypad. The user-programmed sequence can either start tape recording or stop recording upon detection; in either case special flags are automatically recorded on the tape at the point where the match took place. Flags can also be set manually. **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.



See at Booth 1700

Circle 373 on Inquiry Card

Here's how Data General's microNOVA system stacks up against the competition.



microNOVA Processor:
Fully packaged 9-slot microcomputer, 16K words MOS memory, 2.4-microsecond arithmetic operations, hardware stack facility, multiply/divide, DMA capability. Includes RTC, PF/AR and APL. Supports up to 32K words RAM/PROM memory.

Dual-diskette subsystem:
Integral DMA controller, compact 630KB capacity.

Cabinet:
37 inches high, holds all rack mounted components.

DASHER terminal printer:
30 cps, 132-columns, typewriter keyboard, upper/lower case.

Systems Software:
Multitasking Disc Operating System, Real-Time Operating System, FORTRAN IV, Extended BASIC, Macro Assembler, Utilities.

$10,970
List*

The facts speak for themselves. For $10,970, Data General's new microNOVA gives you more system, software availability and support than any other comparable computer. And we deliver in 60 days.

Any way you look at it, it all stacks up in your favor. For more information and our brochure, call our toll free number, 800-225-9497, or, fill out and return the coupon.

*Additional software fees apply to first system only. Quantity and OEM discounts available.

Data General, Westboro, MA 01581
Sounds like smart business. Send me more information.

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COMPANY

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Data General, Westboro, MA 01581, (617) 485-9100. Data General (Canada) Ltd., Ontario. Data General Europe, 15 Rue Le Sueur, Paris 75116 France. Data General Australia, Melbourne (03) 82-1361.

NCC PRODUCT REVIEW

SBC 80 SERIES COMPATIBLE MEMORY

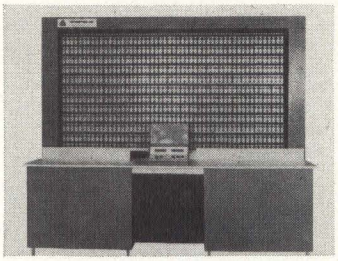
Totally hardware and software compatible with the Intel SBC 80 family of single-board computers and the Intellec MDS systems, the MSC 4502 can provide both high density RAM and EPROM on the same board. Use of 16-pin sockets allows the RAM section to be expanded in 4k increments up to 16k x 8. Four EPROM sockets can be used to expand in 1k x 8 or 2k x 8 increments up to 8k x 8, allowing the addition of nonvolatile memory for control or monitor programming. The unit provides 16 switch-selectable address start locations each for RAM and EPROM, permitting address location changes to be made without wiring charges. Distributive refresh time is 500 ns, read cycle time is 350 ns, and write cycle time is 500 ns. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80110.

See at Booth 1240

Circle 374 on Inquiry Card

MICROFICHE STORAGE AND RETRIEVAL SYSTEM

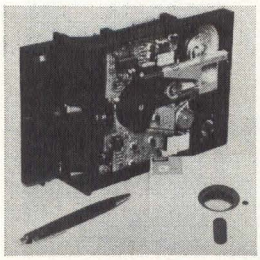
A closed-loop system that is controllable by computer or by local or remote inquiry terminals such as teletypewriters, CRT devices, Touch-Tone® telephones, or other keyboard devices, the 410/50 provides compact storage and high speed retrieval, distribution, and display of up to 150k microfiche/module for as many as 5M microfiche/system. All communication control, priority assignment, indexing, and search are provided by the computer. Information can be presented automatically as video display, duplicate microfiche, or hard copy printout. Several users can have simultaneous access to the information store. Once filed, all microfiche are secured within the storage module; all handling is automated. **Infodetics Corp,** 1341 S Claudina St, Anaheim, CA 92805.



See at Booth 1049

Circle 375 on Inquiry Card

MINI FLOPPY DISC DRIVE

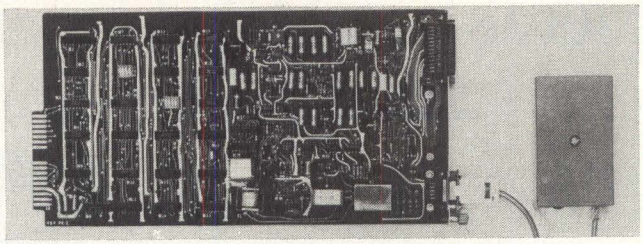


Compatible with std 5.25-in (13.34 cm) flexible disc media, model 6106 measures 5.75 in (14.6 cm) wide by 3 in (7.62 cm) high and 7.5 in (19.1 cm) deep. The drive rotates mini-diskettes at 300 rev/m and records at 2581 bits/in on 35 tracks. Tracking density is 48 tracks/in in 0 to 16 sectors. The unit allows transfer of up to 125k bits/s on an average track-to-track access time of about 220 ms. The single-density disc has track-to-track access time of 20 ms, with head loading time of 35 ms. Rated at 5000 h under heavy usage, it can perform for more than 8000 h with regular usage. Drive has read/write and control electronics, all on a single PC board. **BASF Systems,** Crosby Dr, Bedford, MA 01730.

See at Booth 1795

Circle 376 on Inquiry Card

FCC-REGISTERED DIRECT CONNECT MODEM



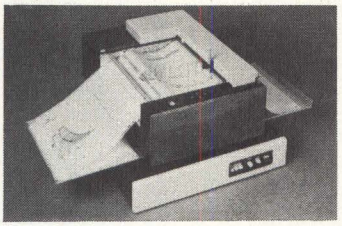
Registered under the FCC ruling which eliminates the need for a Bell DAA, the VA317S modem connects to the switched telephone network through the telephone company's programmable Data Jack. The jack provides a std Bell miniature 8-pin connector with "key way" design; the modem provides a cable with keyed data plug. Jacks may be mounted on the wall or in cabinets; they are configured in multiples of 16 up to 64 modems. Device operates at 300 bits/s in automatic answer mode and is a direct replacement for Bell model 113B. Full-duplex transmission is provided over switched or leased 2-wire telephone circuits. Features include protective circuitry, analog and digital loopback, 8-LED interface display, and built-in data source for online testing. **Vadic Corp,** 505 E Middlefield Rd, Mountain View, CA 94043.

See at Booth 1835

Circle 377 on Inquiry Card

PLOTTER CONTROLLERS

Combining Graphic Machine Language (GML) software with microcomputer-based controllers, series 50 provides systems which are claimed to operate from two to ten times faster than other drum plotting systems. Model 51 provides online RS-232-C service; model 52 offers remote interface to terminal/modem in addition to the RS-232-C. GML relative vector commands provide for transmission of significant digits. Three annotation vectors provide 128 char, plotted at virtually every size and angle. This reduces data transmission load. Features include low host CPU operating costs, high speed on curves, USASCII code, and baud rates of 110 through 9600 asynchronous. Systems include the high speed 1252 and the 3651 36" (91.44 cm) plotter. **Zeta Research, a div of Nicolet Instrument Corp,** 1043 Stuart St, Lafayette, CA 94549.



See at Booth 2053

Circle 378 on Inquiry Card

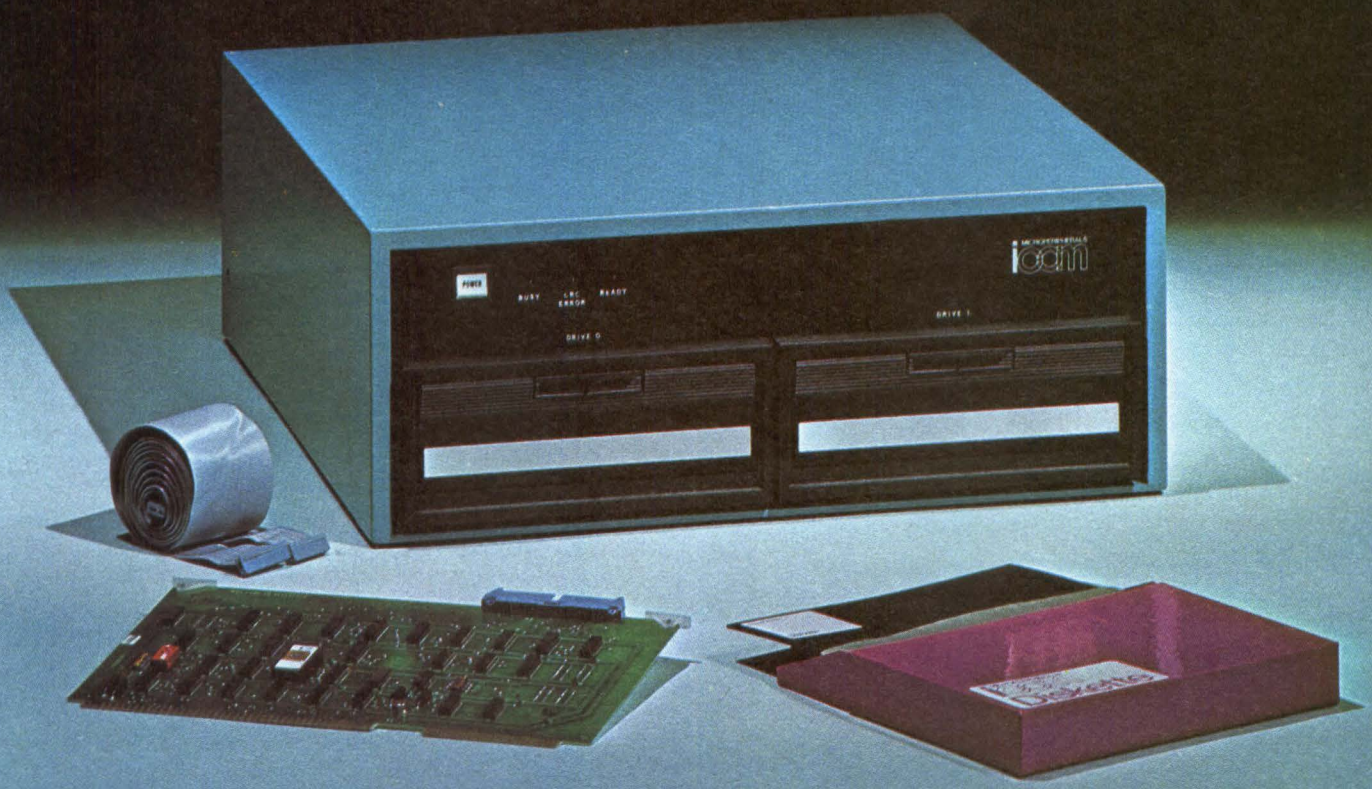
WIRELESS DATA ENTRY MICROPHONE

Combining all advantages of voice data entry with operator mobility, wireless input system consists of transmitter, battery, and volume control packaged in a 1-piece, heavy duty leather belt pack. The miniature FM transmitter transmits each voice entry to a companion receiver which is connected to a voice data entry terminal. Belt pack and a lightweight microphone are all that are required to enter data within an operating range of from 50 to 1000 ft (15 to 305 m). General specifications are ±1.5 dB, 100 Hz to 10 kHz frequency response, and better than 55-dB signal to noise ratio. Frequency stability is crystal-controlled to 0.0025% and modulation is narrow band fm, 40 F3 emission. **Threshold Technology, Inc,** 1829 Underwood Blvd, Delran, NJ 08075.

See at Booth 1017

Circle 379 on Inquiry Card

Save $650 on iCOM's New Dual Floppy Disk System.



At the regular price of $3,300, our new dual floppy is a great buy. It's priced less than competitive models, with features found on no other machine.

At the special $2,650* single quantity price, it's a super value.

Why the low introductory price?

Quite frankly, to make your buying decision easy. We're betting you'll design the iCOM® dual floppy into your system. Many of the largest companies have. And by the way, our OEM quantity prices are right, too. Even more savings.

Here's what you get

The $2,650 price includes the iCOM Dual Floppy and your choice of interface to any of these microcomputers: Intellec 8, Intel SBC-80/10 or 80/20, Intellec-800 or Motorola's EXORciser. You also get our powerful FDOS-II development software with macro assembler and string text editor. And for only $50 more, our new Disk BASIC-M is available for most models.

Another savings

iCOM's software is disk resident, requiring virtually no dedicated computer memory. Most dual floppies require 16K or more of RAM. You could save as much as $1,000 on computer memory alone.

A comforting thought

iCOM® is the world's largest supplier of peripherals for microcomputers. And, being a division of Pertec Computer Corporation, we'll be around whenever and wherever you need us.

This offer ends July 31, 1977. So don't procrastinate. Phone us, or mail the coupon. Right now!

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See iCOM at NCC - Dallas - Booth 1415

CIRCLE 57 ON INQUIRY CARD

NCC PRODUCT REVIEW

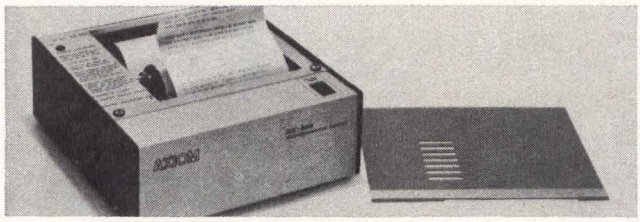
CORE EMULATION OF FIXED-HEAD DISC SYSTEMS

BC-201, -202, and -301 bulk core modules, offered as alternatives to fixed-head discs, have complete interfaces to emulate DEC and Data General systems. A 15.75" (40 cm) high rack-mountable chassis can hold up to eight 128k-word modules for a max of 2M bytes (1M words). The microprocessor-controlled interfaces have access times of 750 ns for DEC and 2 μs for Data General systems. All offer parity generate-and-check, built-in offline test capability, 0 to 55°C operation, and operational fault indication. With 128k-word (256k-byte) modularity and fault indication, MTTR is <15 min. MTBF for the min 128k-word (256k-byte) configuration is >15,000 h. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512.

See at Booth 1025

Circle 380 on Inquiry Card

STANDALONE LINE PRINTER



A complete unit, including case, power supply, ASCII interface, character generator, and paper roll holder, the EX-800 is a compact 80-col, 160-char/s printer which plugs into almost any system. It prints on 5" (12.7 cm) wide electrosensitive paper with black 5 x 7 dot-matrix characters on an aluminum background. Std features include infrared low paper detector, bell, 96-char ASCII set, programmable character size, built-in self-tester, and multiline asynchronous input buffer. Typefaces can be mixed on the same line; the printhead is self-adjusting. A custom LSI chip on the single electronics PC card controls all printer functions. Size is 9.625 x 3.875 x 10.875" (24.45 x 9.84 x 27.62 cm); weight is 12 lb (5.44 kg). **Axiom Corp,** 6932 San Fernando Rd, Glendale, CA 91202.

See at Booth 104

Circle 381 on Inquiry Card

REMOTE GRAPHICS PROCESSOR

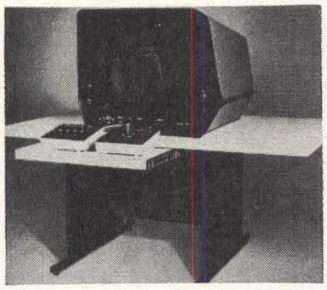
High speed graphics capability is added to remote alphanumeric data display terminals when they are coupled to a graphics processor and the company's 5000 series electrostatic printer/plotter. Charts, graphs, and engineering drawings can be printed at paper speeds averaging 0.5" (1.3 cm)/s when the serial data rate is 9600 Hz. Actual instantaneous paper speed varies from 0.04 to 1.0" (0.1 to 2.54 cm)/s depending on plotter model, baud rate at which data are received, and plot complexity. Using PLOT graphics software and RGP option software on the host computer, input data are processed and transmitted over the communication line in highly encoded char form. **Gould Inc, Instrument Systems Div,** 3631 Perkins Ave, Cleveland, OH 44114.

See at Booth 1015

Circle 382 on Inquiry Card

INTERACTIVE GRAPHICS DISPLAY

High speed 3300 series displays can provide refresh graphics for any minicomputer with a standard I/O configuration writing up to 16,667 short vectors and 6000 char. Model 3301 displays 2-dimensional graphics and alphanumerics; 3302 adds image transformation and rotation to these basics. The microprogrammed units feature font and 2-dimensional digital transformations, variable speed vector and font generators, programmable graphic instructions, optional refresh buffer, and full subroutine stack capability. Display I/O control unit accepts 16-bit data and control. Other hardware features include 256 intensity levels, four vector modes, and 4096 x 4096 addressable locations. Full range of input devices are available. **Vector General,** 21300 Oxnard St, Woodland Hills, CA 91364.



See at Booth 1115

Circle 383 on Inquiry Card

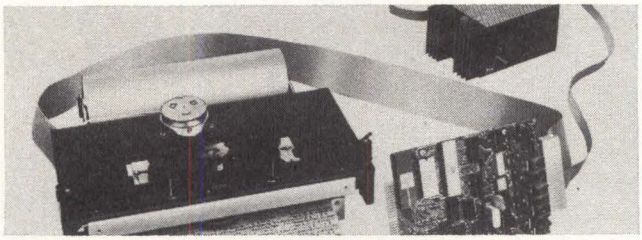
SHARED-MEMORY MULTIPROCESSOR SYSTEM

GA-16/550, based upon the architecture of and upward compatible from the /440 computer, is expandable to eight central processors with 2M bytes of common memory. Data transfers on the 32-bit memory bus exceed 7M bytes/s. Dual-port memories and dual-bus structures provide flexible multiprocessor configurations. The microprogrammed central processor uses high speed TTL (Schottky) and bipolar control store. Basic microcycle execution time is 240 ns. Two sets of eight general-purpose registers and a full range of arithmetic and logical functions enhance the power. An integral 1024-word cache memory acts as a buffer between processor registers and main memory with a 120-ns access time. **General Automation, Inc,** 1055 S East St, Anaheim, CA 92803.

See at Booth 1393

Circle 384 on Inquiry Card

DATA PRINTER AND CONTROLLER

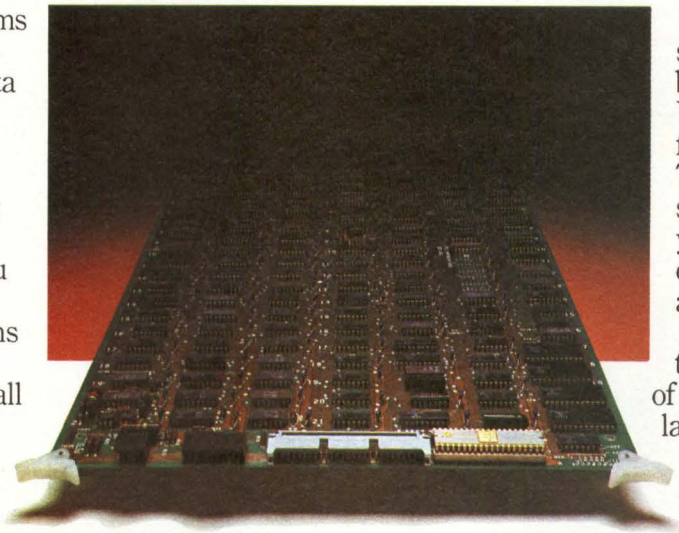


Three sizes of DMTP-6 series printers produce max lines of 36, 66, and 96 characters, respectively, at 12 char/in (4.7/cm) on 3.4375, 6, and 8.5" (8.73, 15.2, and 21.6 cm) wide paper. Heads are driven by synchronous motors at 10 in/s (25 cm/s) for 60 Hz. Since character generation is dependent on this constant, pitch is variable—programmable at 8, 10, or 12/in (3, 4, or 5/cm), single stroke or enhanced. Printing technique is 7 x 5 impact dot matrix; character height is 0.110" (0.279 cm). Print speed is 120 char/s. Data input is synchronous; entry is serial. Interface memory and control circuitry options are offered as either discrete packages or part of standalone instruments. **Practical Automation, Inc,** Trap Falls Rd, Shelton, CT 06484.

See at Booth 1743

Circle 385 on Inquiry Card

Varian's new mainframe-on-a-board: What you do with it is your business.



Whether your systems business is scientific, instrument control, or data communications, know this:

Our new V77-200 delivers more computing power than any other computer-on-a-board you can buy. Handling up to 32K/16-bit words of 660ns MOS memory.

Reason enough to call it the world's first mainframe-on-a-board. But there's more.

Because our new V77-200 comes loaded with "big machine" features. Like 8 programmable registers with byte, word and double word manipulation. Up to 32-bits of arithmetic precision. A powerful set of 187 instructions. Hardware multiply/divide. Direct memory access. Programed I/O. Multi-device automatic program loaders. A real-time clock. And a teletype/CRT controller. All standard. And all on a single 10.8" x 17" board.

There's even Virtual Console Logic that eliminates the need for a programmer's console by allowing you to control the V77-200 from a teletype or CRT keyboard.

You get "big machine" performance, too. Example: a microinstruction cycle time of 165ns that allows multiplication functions to be handled in just 4.9 microseconds—divide in just 8.

Plus your choice of OEM-tailored options. Like a variety of connector planes and general purpose interface boards for custom I/O designs. Three different 660ns memory boards (in 8K, 16K, and 32K-word modules). An operator's console. Power-fail detect and data save. Memory parity. Hardware for up to 64 priority vectored interrupts. An integral or modular power supply. And, of course, a system chassis. All the "unbundled" pieces you need for quick and easy system integrations.

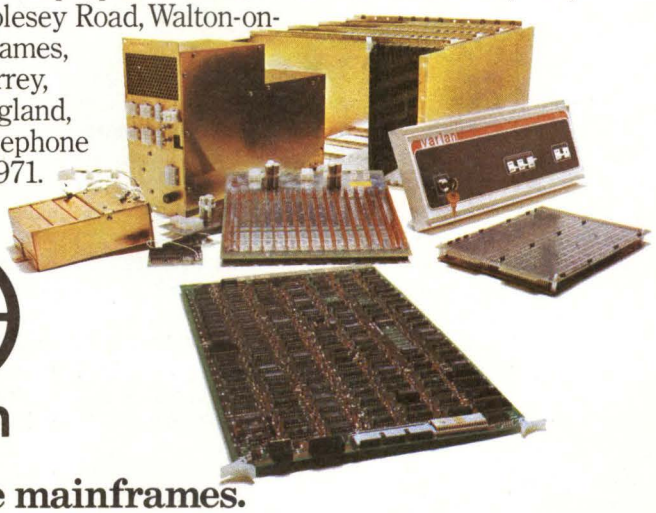
The new V77-200 also saves you time and money by allowing you to use Varian's well-established floppy or disk-based VORTEX real-time operating system. In effect, allowing you to concentrate on the development of your application software.

And giving you access to Varian's extensive library of software subsystems, language processors, and system utilities.

Best of all, the world's first mainframe-on-a-board has a base price of just $1200. Plus a discount plan designed to give even modest-volume OEM buyers a big break. And you can take delivery in a matter of days—not months.

No matter how you configure it, the new V77-200 is the most economical Varian yet. Delivering the kind of price/performance value that just makes good sense. No matter what business your systems are in.

For more information on the world's first mainframe-on-a-board, please contact: Varian Data Machines, 2722 Michelson Drive, P.O. Box C-19504, Irvine, California 92713, Telephone (714) 833-2400. In Europe, please contact: Varian Associates, Ltd., Molesey Road, Walton-on-Thames, Surrey, England, Telephone 28971.



varian

Mini's that think like mainframes.

NCC PRODUCT REVIEW

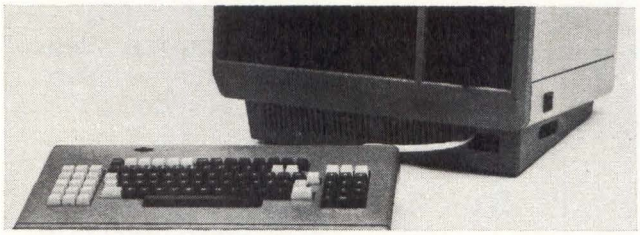
MICROFLOPPY CONTROLLER

Small enough to stack on top of the microfloppy's PC board, the 8201 employs Intel MCS 8048 with ROM, RAM, and I/O ports and Western Digital 1771-1 floppy controller chip to form a preprogrammed intelligent controller for the company's model 82 disc drives. It performs all functions necessary to transfer data between one to four disc drives and a host system and to format discs according to the modified IBM-type format specs. Commands received from the host are interpreted by internal microcode and implemented by TTL and MOS LSI, providing a compromise between flexibility and simplicity. Operating features include three instruction sets—DUP, a copy diskette instruction; two self-test diagnostics; and a 128-byte sector buffer. **Wangco Inc, a unit of Perkin-Elmer Data Systems,** 5404 Jandy Pl, Los Angeles, CA 90066.

See at Booth 1483

Circle 386 on Inquiry Card

INTELLIGENT TERMINAL



TDV 2114 is a CRT display unit which can serve as a teleprinter replacement, standalone processing system, or intelligent terminal. It contains a microprocessor to facilitate change from one mode of operation to another by merely loading a program from cartridge or diskette. The terminal may be equipped with up to four digital cartridge recorders or up to four IBM-compatible diskette units, which may be integrated in the unit itself, providing operator convenience and min space requirements for small systems. A minimum configuration consists of display hardware with 12″ (30 cm) diag CRT faceplate and a microprocessor with 2k bytes of RAM and sockets for 8k bytes of ROM/erasable p/ROM (expandable to 64k bytes of total memory). **Tandberg Data Inc,** 4060 Morena Blvd, San Diego, CA 92117.

See at Booth 1065

Circle 387 on Inquiry Card

COLOR PLOTTING SYSTEM

An area-oriented software system (COLOR), a plotter with three ink jets, and an offline magnetic tape unit comprise a color plotting system which can produce pictures up to 22 x 34″ (59 x 86 cm) or eight page-size units in 8.5 min. The three primary colors (red, yellow, blue) can be plotted alone or superimposed to create seven solid colors, including black, and >15,000 shades on ordinary paper or on a special clear film for producing transparencies. No drying time is needed. When color separation offset plates are required for printing large quantities of a plot, the system can produce separate plots of the three color components. The ink jets plot a uniform resolution of 125 points/in (49/cm) in both dimensions; a full plot contains nearly 12M picture elements. **Applicon Inc,** 154 Middlesex Tpk, Burlington, MA 01803.

See at Booth 2042

Circle 388 on Inquiry Card

VISUAL DISPLAYS/KEYBOARDS

Monitors for model 303 units are std TV rasters with video data synchronized to horizontal and vertical timing pulses. Keyboard sections require input power of 5 V at 35 mA max (typ 20 mA) for the encoder and an additional 315 mA max (typ 200 mA) for the parallel to serial converter. Self-contained data entry keyboards with numeric pad have std 0.75″ (1.9 cm) typewriter spacing and feel. Alternate miniature keyboards, with converter logic mounted on the display monitors, have keys spaced 0.625″ (1.6 cm) apart. Both are available with a number of different character configurations. Output signal from the std keyboard is 7-bit ASCII plus parity, upper case only. **Informer, Inc,** 2218 Cotner Ave, Los Angeles, CA 90064.

See at Booth 1577

Circle 389 on Inquiry Card

INTELLIGENT TERMINAL

Key features of the model 216, the first member of the Display 16 terminal family, include a 16-bit LSI microcomputer; up to 128k bytes of internal memory for data and programs; high storage efficient memory structure; compact display stations with flicker-free screens and movable solid-state keyboards; and communications interfaces for asynchronous, synchronous, BSC, and SDLC protocols. Peripherals include hard and floppy discs, magnetic tape drives, and character and line printers. Terminal-resident software includes a development system, a real-time operating system, and text editing and data entry applications packages. **Computek Inc,** 63 Second Ave, Burlington, MA 01803.

See at Booth 1393

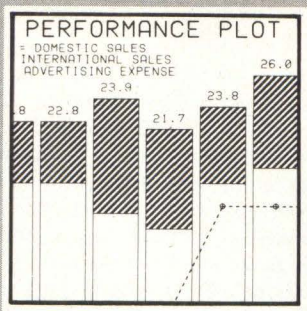
Circle 390 on Inquiry Card

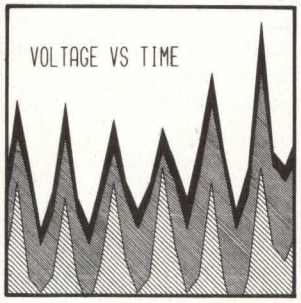
INTERACTIVE GRAPHICS DISPLAY TERMINAL

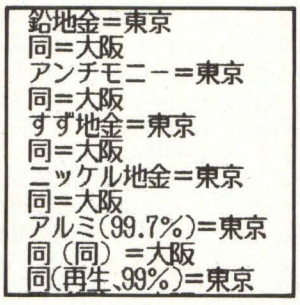
The fully interactive Graphics C-9 terminal provides the user with a complete electronics package that can be unpacked and simply plugged directly into a 110-V outlet and a telecommunications coupler, with no additional hardware options required. Std features include 17″ (43 cm) 1029-line scan video monitor with high screen light output, built-in zoom/pan, joystick for graphics interaction, and hardware graphics processor for scaling graphics and alphanumerics. Microprograms contained in ROM drive a microprocessor controller. A serial interface connecting the detached keyboard to the CRT display eliminates restrictions imposed by parallel interfaces used in other models. Curvilinear information is displayed by converting all contour data to conic curves. **Hughes Aircraft Co, Industrial Products Div,** 6155 El Camino Real, Carlsbad, CA 92008.

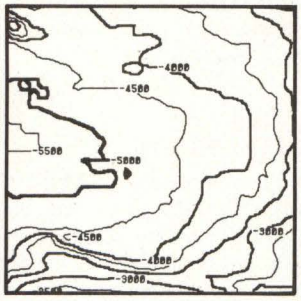
See at Booth 1190

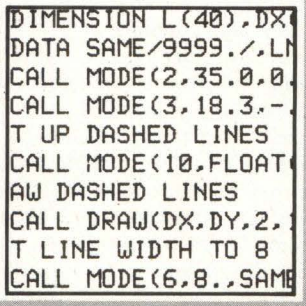
Circle 391 on Inquiry Card

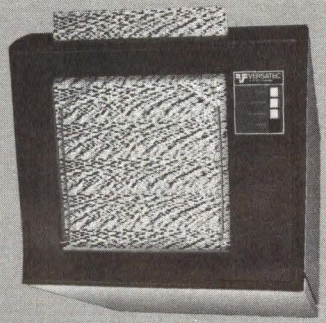












Don't print. Write.

Versatec printer/plotters don't print. They write. And that difference means more useful, reliable, quiet output from your minicomputer.

While impact printers hammer ink on paper with a limited font, Versatec electrostatics write anything—alphanumerics in any size, style or language, graphics ranging from simple bar charts and line drawings to complex maps and geophysical plots. They give you words and pictures simultaneously without changing hardware or reducing speed.

Here is a way to compact pages of printout into a single graph. A way to isolate variables you might never see in print. A way to visualize data for better presentation.

And you can depend on continuing output. Writing is electronic, not mechanical. No impact. No type wear. No alignment problems. No vibration. And no noise. Just quiet reliability measured in thousands of hours.

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Versatec has the optimum writer for your application. Thirty-six plotters and printer/plotters (more models than all competitors combined) offer the widest range of speeds, formats and resolution. Interfacing is simple with on-line controllers to match popular computers, CRTs or video sources.

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- ☐ The 360/370 plotting system

Please send samples:
- ☐ Print samples
- ☐ Plot samples

computer model and operating system

application

name telephone

organization

address

city, state & zip

50-MHZ, 4-CHANNEL PORTABLE OSCILLOSCOPE

Based on cold-switching techniques, the PM3244 has four identical 50-MHz channels with 5-mV sensitivities. Two differential signals can be displayed at the same time as the four input signals on an 8 x 10 cm display. A direct-conversion power supply allows operation from any ac supply between 100 and 240 V ±10% and any frequency between 46 and 440 Hz is possible; any dc supply between 100 and 200 V is accepted. Power consumption is 29 W. **Philips Test & Measuring Instruments, Inc,** 400 Crossways Pk Dr, Woodbury, NY 11797.

See at Booth 2061

Circle 264 on Inquiry Card

LINE PRINTER

Compact, medium speed, impact printer model 5100 uses a swing drum printing method to produce the 64-char ASCII code, 136 char/line at 350 lines/min. Horizontal and vertical spacing are 2.54 ± 0.13 mm and 6 or 8 lines/in, respectively, selectable by toggle switch. Line advance time is 40 ms (6 lines/in), 30 ms (8 lines/in). Std fanfold and edge-punched paper, 4 to 6.75" (10 to 17 cm) wide is used. Measuring 108.0 x 77.0 x 55.0 cm, the unit uses 110/115/220-V, 50/60-Hz power, single-phase, 600 VA. **Tokyo Juki Industrial Co, Ltd,** 23 Kabukicho, Shinjuku-ku, Tokyo, Japan.

See at Booth 1086

Circle 265 on Inquiry Card

LIGHTED SWITCH PC TERMINAL OPTION

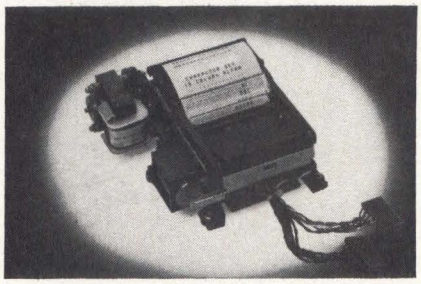
PC terminals have been added as an option to the series 01-700 switches featuring 1-piece housing with the Butterfly® double-break basic switch. Switches are offered with two optional bushing sizes, a 0.469" (1.19 cm) to accept a T-1¾ screw base lamp, or 1.6" (4.064 cm) to accept a T-1¾ flange base lamp. The 1- and 2-pole momentary or alternate action units have gold-plated contacts. Option eliminates costly wiring and harnessing because switches can be directly inserted into mother and daughter boards. **Licon, div of Illinois Tool Works, Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.

See at Booth 1139

Circle 266 on Inquiry Card

ALPHANUMERIC/NUMERIC IMPACT PRINTER

PR1500 series, 15-col impact printers are capable of speeds up to 3 lines/s for numeric, and 1.5 lines/s for alphanumeric data, and offer a full 54-char set and multicopy capabilities. Characters for every three columns are formed by "spanning hammers," a construction feature designed to cut drive electronics costs and increase reliability by reducing the number of moving parts. Devices offer a 500-ms start-up time, with subsequent line feed of up to 10 lines/s. **Sheldon-Sodeco Div, Landis & Gyr, Inc,** 4 Westchester Plaza, Elmsford, NY 10523.



See at Booth 1128

Circle 267 on Inquiry Card

DUAL CHANNEL DATA SET

Design 100 is a 0- to 300-baud dual-channel, direct-access, originate and automatic answer data set that interfaces I/O devices to both the TWX and the DDD switched telephone dial-up network. Control panel configurations include a remote control head, or integral with teleprinters such as Teletype® and LA36 DECwriter®. Both rotary dialers and numeric keypad controls with automatic redial capability are offered. The electronics package mounts inside or at the rear of most terminals, or can be wall mounted. **MI² Corp,** 1212 Kinnear Rd, Columbus, OH 43212.

See at Booth 1583

Circle 268 on Inquiry Card

DISTRIBUTED INFORMATION SYSTEMS

Designed for distributed processing applications are two versions of the series 21, available in multiple-unit configurations. Basic systems consist of an operator station with 1920-char CRT and keyboard, and a processor with one diskette drive. System 21/20 is preprogrammed for data entry and validation under control of user supplied formats; the 21/40 is fully programmable by the user via MOBOL. Both are expandable to four operator stations. **Mohawk Data Sciences Corp,** 1599 Littleton Rd, Parsippany, NJ 07054.

See at Booth 1460

Circle 269 on Inquiry Card

HIGH ISOLATION TRANSFORMERS

Available in ratings from 1 kVA, the line of transformers comes in three versions: 0.005, 0.001, and 0.0005 pF. Devices provide low cost isolation of sensitive equipment from noisy power lines with rejection of both common and transverse mode noise caused by common mode input transients >125 dB. Rated 50 or 60 Hz, models are connectable for 120- or 240-Vac input or output for use as a combination step-down transformer and noise isolation device. **Elgar Corp,** 8225 Mercury Ct, San Diego, CA 92111.

See at Booth 1008

Circle 270 on Inquiry Card

FLOPPY DISC MICROCOMPUTER SYSTEM

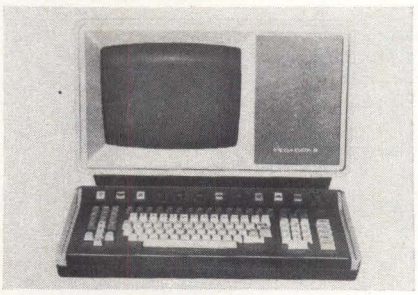
Based on the 6800 microprocessor set, system 68 can accept any WINCE micromodules with MPU, RAM, ROM, serial and parallel I/O, and EROM programmer. It is expandable to 65k in addition to one or more floppy disc drives. Basic system includes 1k ROM with FANTOM II, a monitor/diagnostic program that allows the user to enter programs and data, single-step through programs, and set breakpoints. Editor, assembler, and BASIC are also available. **Wintek Corp,** 902 N 9th St, Lafayette, IN 47904.

See at Booth 1023

Circle 271 on Inquiry Card

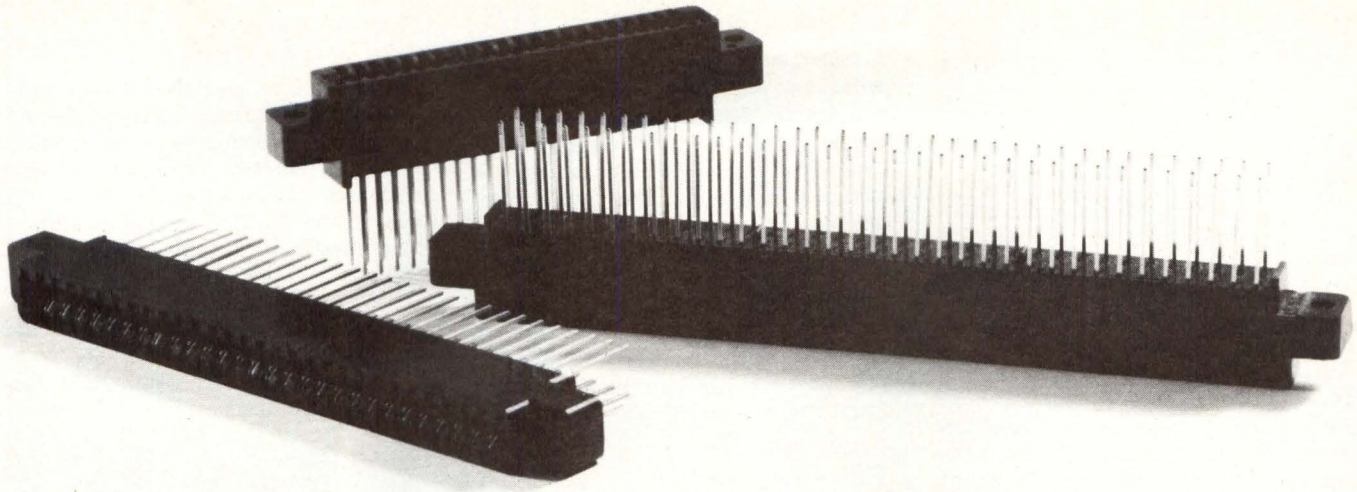
EMULATING TERMINAL SYSTEM

Containing a full-scale 12-bit microprocessor, 15" (38.1 cm) diag display screen, and 126-station keyboard, model 700/UETS is a minicomputer configured as a terminal which emulates many types of terminals and protocols. Programmable unit contains data line discipline and protocol, plus forms and data handling software routines to make it plug-for-plug compatible with different mainframes. Program storage system consists of MOS, p/ROM devices, or RAM loaded from diskette; it stores all operating parameters and telecommunications routines. **Megadata Corp,** 35 Orville Dr, Bohemia, NY 11716.



See at Booth 2029

Circle 272 on Inquiry Card



Presenting our better-mouse-trap line. No frills at all.

When you cut price without cutting quality, soon no one thinks of it as a cut price. That's where our Norsman line of Wire-Wrap* P/C connectors is headed. Here's why:

The insulator — it's tough, resilient, non-conductive — everything you need in a Wire-Wrap body. And it's made out of low cost phenolic, not the higher cost diallyl phthalate (if you need to meet mil specs, we have that in one of our other lines).

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The whole Norsman idea is as simple as it is old: keep performance up and cost down. It works.

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*Wire-Wrap — registered trademark of Gardner-Denver Company.

Tell me everything. ☐ Send me detailed literature.

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Company _____ Telephone _____

Address _____

City _____ State _____ Zip _____

Viking CONNECTORS

Viking Industries, Inc./21001 Nordhoff St./Chatsworth, Calif. 91311/(213) 341-4330

CIRCLE 60 ON INQUIRY CARD

3-WAY OPTICAL SCAN CAPABILITY

Providing flexibility for electronic ordering, an enhancement to the SOURCE 2200 portable data terminal optically scans three bar code systems with a single unit. Optional 3-way selector enables reading of UPC, Monarch's CODABAR, and the company's bar code. Also available is the SOURCE 7600 programmable offline data terminal, incorporating an Intel 8080 microprocessor, cassette drive, keyboard, 10-key numeric touchpad, and 32-position LED display. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92627.

See at Booth 1180
Circle 273 on Inquiry Card

ROTARY PRINTER

Mechanism of the series 1100 is designed to provide printing speeds above 2k char/s on moderately-priced, electrosensitive paper. The unit provides 40, 80, or 132 char/line on 24 lines. Character set is the std 64-char ASCII set. Characters are formed from a 5 x 7 dot matrix with 70 line/in resolution. Power requirements are 5 W standby, 55 W operating. Drive unit life is 8 billion char; printhead has life of 25M char. **SCI Systems, Inc,** 8600 S Memorial Pkwy, PO Box 4000, Huntsville, AL 35802.

See at Booth 1172
Circle 274 on Inquiry Card

COMMUNICATIONS TERMINAL

Delivering 30-char/s throughput, upper/lower case printing, and 132-col capability on 11" wide fanfold paper, the model 43 has a 9-wire matrix impact printhead mechanism that permits true descenders for increased legibility. The terminal sends or receives at 10 or 30 char/s in half- or full-duplex mode with even parity detection on or off. Its solid-state keyboard is buffered to allow users to type as fast as possible. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60076.

See at Booth 1505
Circle 275 on Inquiry Card

MATRIX LINE PRINTER

A raster matrix line printer capable of producing 132-char lines at 300 lines/min, model 300 forms characters one dot at a time with sufficient hammer energy to produce clear copy on the last of 6-part forms. The shuttle hammer assembly overlaps dots both horizontally and vertically to produce near solid lines. Std features include plotting capability, electronic VFU, double-height characters, and underlining. 8-pin engagement tractors assure accurate paper movement. **Printronix, Inc,** 17421 Derian Ave, Irvine, CA 92714.

See at Booth 1817
Circle 276 on Inquiry Card

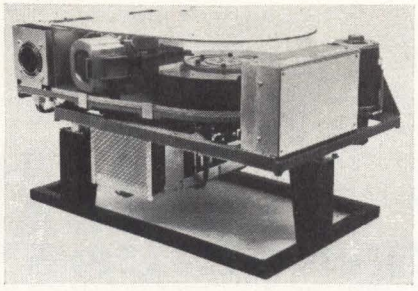
VIDEO DISPLAY TERMINAL

Interfacing directly with std computer systems using its 132-col output format, model 132A eliminates data reformatting of 80-col displays. Display is 132 col x 30 lines, with 60-cycle refresh of images. Features include Charactron® CRT for instant alphanumeric char and symbol generation, 96-char ASCII set, 60- or 120-line buffer, cursor control, single line editing, 110- to 9600-bit/s transmission in full- or half-duplex modes, and RS-232 output. **DatagraphiX,** PO Box 82449, San Diego, CA 92138.

See at Booth 1887
Circle 277 on Inquiry Card

75M-BYTE SMALL SYSTEM DISC DRIVE

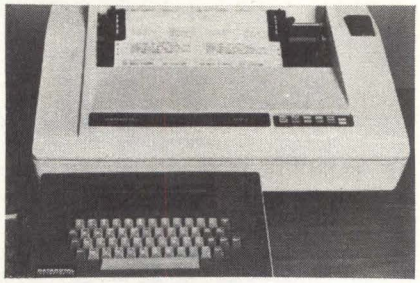
A fixed-media storage drive designed for use with small computer systems, model 601 has storage capacities of 25M, 50M, and 75M bytes and a data transfer rate of 885k bytes/s. Average access time is 32 ms. System consists of two assemblies, the deck plate and frame. Use of proximity recording provides max reliability and performance, as does the disc coating technique and surface shield. Optional feature provides 500k or 1000k bytes of fixed head storage. **Memorex Corp, Equipment Products Group, OEM Div,** San Tomas at Central Expwy, Santa Clara, CA 95052.



See at Booth 1661
Circle 278 on Inquiry Card

PROGRAMMABLE PRINTING SYSTEMS

Combining a compact data input station with a 120-char/s printer configured around a programmable microcomputer, IPS-7/KD consists of a 32-char gas discharge display, 64-char ASCII keyboard, and RS-232 or 20-mA current loop interface. Microcomputer has eight I/O registers and 10k bytes of memory. Users communicate directly with a central computer; system operates online in either local or remote mode, or in standalone mode. **Dataroyal, Inc,** Nashua, NH 03060.



See at Booth 1295
Circle 279 on Inquiry Card

INTELLIGENT DATA TERMINAL

Outpost 7, the MC6800 microprocessor-oriented intelligent data terminal, operates on its own or online. It handles many distributed data processing functions and stores data on tape. Online, it transmits tape-stored data in batch mode or communicates in real-time. Components include a 12" (30 cm) diag screen display, full communications keyboard, company's tape drive, RAM expandable to 64k bytes, and selectable baud rates of 110 to 9600. BASIC compatibility is included on the unit. **Tano Corp,** 4521 W Napolean Ave, Metairie, LA 70001.

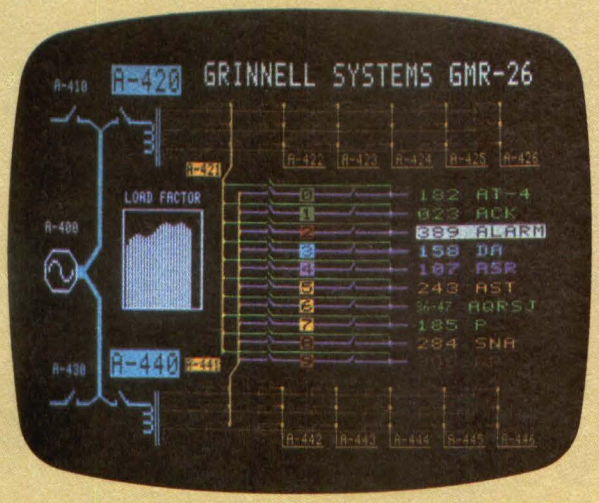
See at Booth 1126
Circle 280 on Inquiry Card

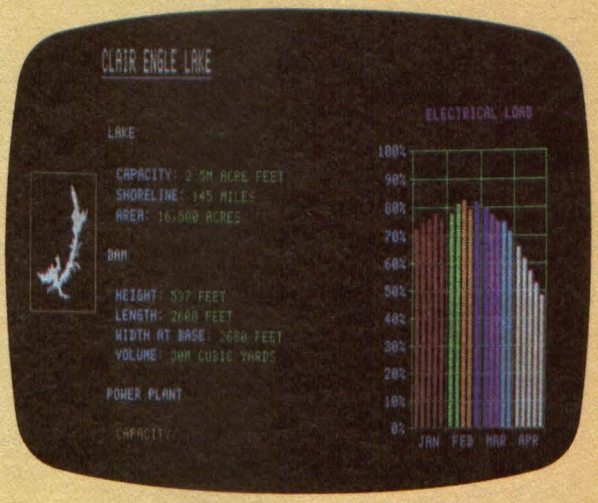
RAM BUFFER OPTION

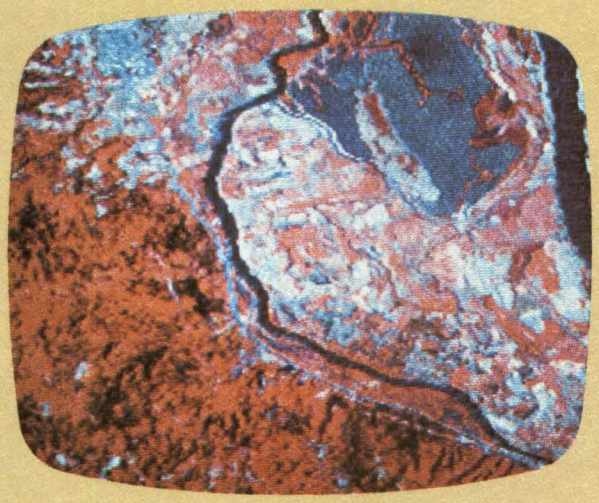
The 9107-1 CMOS p/ROM programmer option provides a 1024 x 8 workspace where p/ROM code can be accumulated and manipulated prior to programming a blank p/ROM. Buffer can be loaded from the series 90 keyboard or from master p/ROM, and the copy p/ROM programmed directly from any part of the buffer. A data displacement feature during buffer input and output operations provides editing capability. Power to the programmer can be switched off for up to 60 s without losing buffer data. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

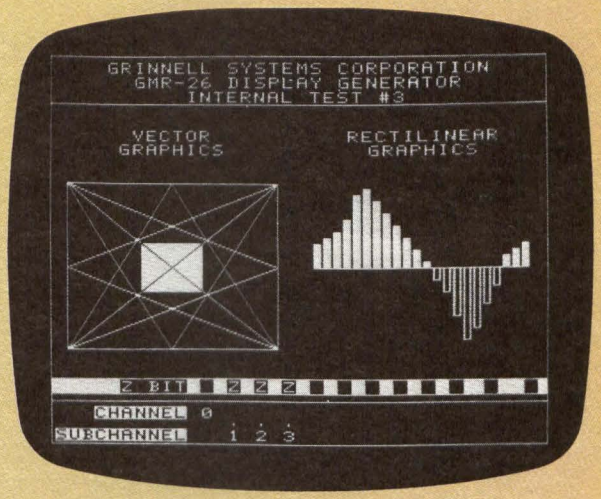
See at Booth 1089
Circle 281 on Inquiry Card

GRINNELL DISPLAYS:









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So, before you make any decision about computer display systems, talk to the Grinnell experts. Our engineers have been in the display picture longer than most, and their experience shows. Complete operating systems start at $5,700, and quantity discounts are available. For detailed specs and/or a quotation, call or write.

GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

CIRCLE 61 ON INQUIRY CARD

IMAGE PROCESSING SYSTEM

Providing automatic input of grey-tone pictures, line drawings, and OCR numerals, the EyeCom picture digitizer and display terminal also has keyboard data entry and full alphanumeric and graphic capabilities. Pictures are input to the computer by means of a digitizer, processed, and displayed on the TV screen. Graphical data are drawn and input using a joystick controlled cursor, and generated by the computer for display. Full typewriter keyboard allows alphanumeric input and subsequent display. **Spatial Data Systems, Inc,** PO Box 249, 508 S Fairview Ave, Goleta, CA 93017.

See at Booth 2013

Circle 282 on Inquiry Card

LINE DRAWING COMPUTER GRAPHICS SYSTEM

A standalone computer graphics package, PICTURE SYSTEM 2 is a high performance system which presents dynamically-moving pictures of 2- and 3-dimensional objects. Basic hardware consists of a picture controller (a DEC PDP-11 minicomputer), direct I/O and DMA interface, processor, dual-port MOS memory in 16k increments, generator, display, and interactive devices. Capabilities include rotations, translations, changes in scale, and segmented refresh buffering. **Evans & Sutherland Computer Corp,** 580 Arapeen Dr, Salt Lake City, UT 84108.

See at Booth 1097

Circle 283 on Inquiry Card

DATA COLLECTION TERMINALS AND CONTROLLERS

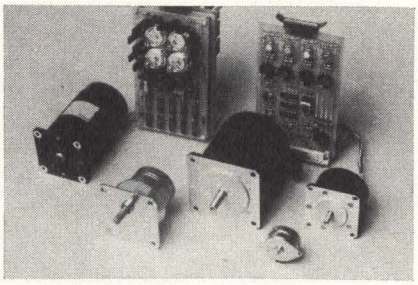
Three programmable data collection terminals and two communications controllers meet MIL-STD-810 tests for reliable operation in hostile environments. Model 1647-1, an 8080 microprocessor-based terminal, electro-optically reads punched badges and has five LEDs for prompting. The 1647-2 in addition reads 80-col ANSI cards and has 20 user-defined input keys; 1647-3 provides 40 user-defined keys and up to 10 LEDs. The 8080-based 1648-1 SCU controls up to 30 terminals on one party line; the 1648-2 controls up to 100 terminals on four separate lines. **Epic Data Corp,** 12728 15th Place NE, Bellevue, WA 98005.

See at Booth 1057

Circle 284 on Inquiry Card

MOTORS

RDM series 5-phase stepping motors have step angle of 0 to 72/0 to 36 deg with low oscillation amplitude. The Quintronic drive provides smoothness of rotation through its inherent damping. Harmonic distortion is approx 5%. The unit has no pronounced resonance regions and no zero torque point at high speed, resulting in high start/stop and slew frequencies. Corresponding to 500 steps/rev the 0- to 72-deg step can be electrically divided to give 1000 steps/rev. **Berger-Lahr Corp,** Peterborough Rd, Jaffrey, NH 03452.



See at Booth 2066

Circle 285 on Inquiry Card

SWITCHING POWER SUPPLY

The 9E5-50C-17 is a 5-V ±10%, 50-A switching regulated power supply in a 2.25 x 4.94 x 15.88″ (5.72 x 12.55 x 40.33 cm) package yielding 1.4 W/in^3 (86 mW/cm^3). Packaging allows it to fit crosswise in a std 5.25″ (13.34 cm) Retma rack while using only 2.25″ (5.72 cm) of rack depth; it may also be mounted to the cabinet alongside, above, below, or behind the rack drawers. Input voltage range is 115/230 Vac 10/−20% with a 20-ms hold-up allowing it to work under abnormal line conditions. **Powertec Inc,** 9168 DeSoto Ave, Chatsworth, CA 91311.

See at Booth 2030

Circle 286 on Inquiry Card

DMM/COUNTER/SCOPE

PS935/975 DMM-counter-miniscope is a dual-trace instrument which includes digital multimeter (DMM), frequency counter, and oscilloscope in a single unit; each device has a dedicated display. Bandwidth is 35 MHz, vertical sensitivity is 5 mV/div, sweep resolution is 10 ns/div, and scope trigger range extends from dc to 50 MHz. Counter frequency range is 50 MHz. CRT acceleration voltage is 5 kV, resulting in greater brightness; display area is 8 x 10, 0.25″ (0.64 cm) divisions. **Vu-Data Corp,** 7170 Convoy Ct, San Diego, CA 92111.

See at Booth 1624

Circle 287 on Inquiry Card

MODEMS

Model 232D2-42, a 1200-baud PC card modem, mounts in the series 330 basic unit allowing 300- and 1200-baud ports to be mixed in the same enclosure. The modem provides asynchronous 1200-baud service compatible with Bell Series 202, including 5-baud reverse channel. Other reverse channel options include 150 baud. The modem operates full-duplex on 4-wire, half-duplex on 2-wire. 330 series modems provide integral power supply, auto answer, and display of four control and two data functions. **ComData Corp,** 8115 N Monticello, Skokie, IL 60076.

See at Booth 1739

Circle 288 on Inquiry Card

SMALL BUSINESS SYSTEMS

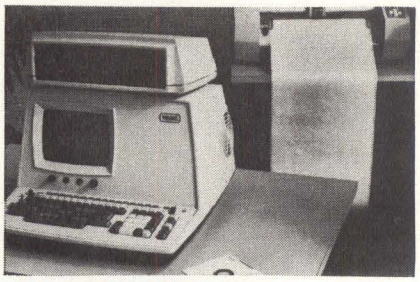
Comprised of Nova-compatible microprocessor and video display, the video computer system is based on the B 800, and features a full line of peripherals, communications controllers, and software. Its 16-bit processor permits maximum operator interface and functions, high data throughput, ease of programming, and configuration flexibility. Extensive use of firmware allows user functions to be integrated as an integral part of the system architecture. **Beehive International,** 4910 Amelia Earhart Dr, Box 25668, Salt Lake City, UT 84125.

See at Booth 1265

Circle 289 on Inquiry Card

DESKTOP COMPUTER

PCS-II "deskette" computer makes direct access computing affordable by small users. Implementing minidiskette storage devices, the computer includes a 1k-char CRT screen and typewriter-like keyboard with numeric keypad and 32 data entry and control function keys. High speed processor has two memories: 8k bytes of user memory and one or two 5.25″ (13.4 cm) minidiskettes holding up to 89k bytes of programs or data. Information is stored in 350 sectors. **Wang Laboratories, Inc,** One Industrial Ave, Lowell, MA 01851.

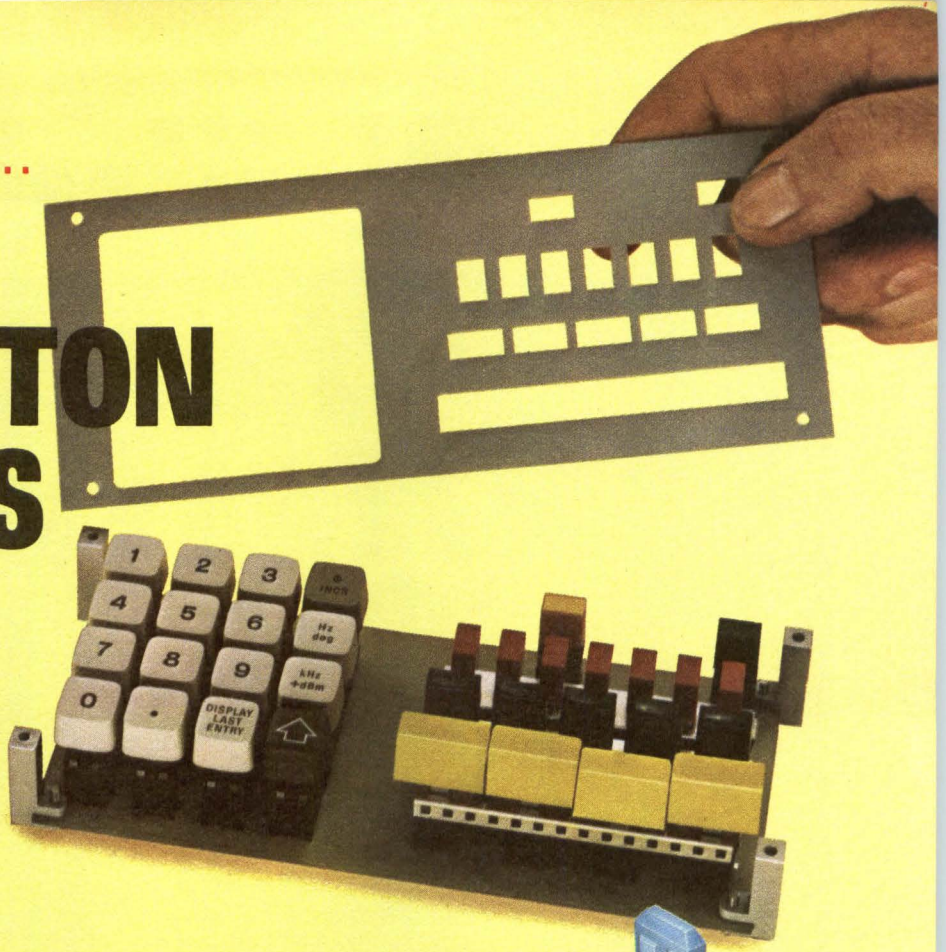


See at Booth 2049

Circle 290 on Inquiry Card

New from Centralab...

IMPS PUSHBUTTON SWITCHES

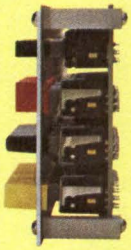


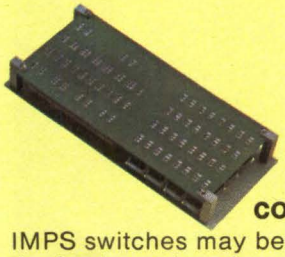
A new miniature modular building block system that offers microprocessor control designers more of what they need.

To meet the special digital and analog needs of today's μP-based controls, Centralab offers design engineers a whole new system of modular pushbutton switch building blocks. We call it IMPS — Integrated Modular Panel System. IMPS saves PC board and panel area and simplifies front panel design, cuts assembly costs, reduces back-panel space requirements, and meets the digital-analog needs of μP-based controls. Check these space saving, cost-cutting features.

Simplify front panel interface.

All IMPS switches regardless of function, are uniform in size, simplifying design and selection of front panel hardware. They have high volumetric efficiency, occupying .505" x .388" PC board area and require only .608" of space between PC board and front panel.





Cut assembly costs.

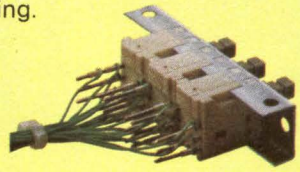
IMPS switches may be mounted on the front panel, and are designed for automatic wave soldering installation and PC board cleaning. Insert molded terminals prevent flux and solder wicking and contact contamination. Integral PC board stand-offs provide for efficient board cleaning.

Meet analog and digital needs.

IMPS switches are available with momentary, push-push and interlocking actions, with a long-life contact system that switches both digital and analog signals. To accommodate critical signal requirements, housings are high-insulation molded plastic with UL 94V-0 rating.

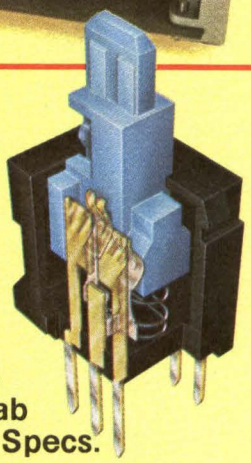
Available options.

Optional installations include ganged assemblies, front-panel mounting and wire-wrapping.



All IMPS pushbutton switches are built to Centralab's highest quality standards (see specifications at right). They're priced as low as 41 cents in 1,000 quantity. For full technical details, samples and quotation, call (515) 955-3770, or write to the address below.

CENTRALAB
Electronics Division
GLOBE-UNION INC.
P.O. BOX 858
FORT DODGE, IOWA 50501

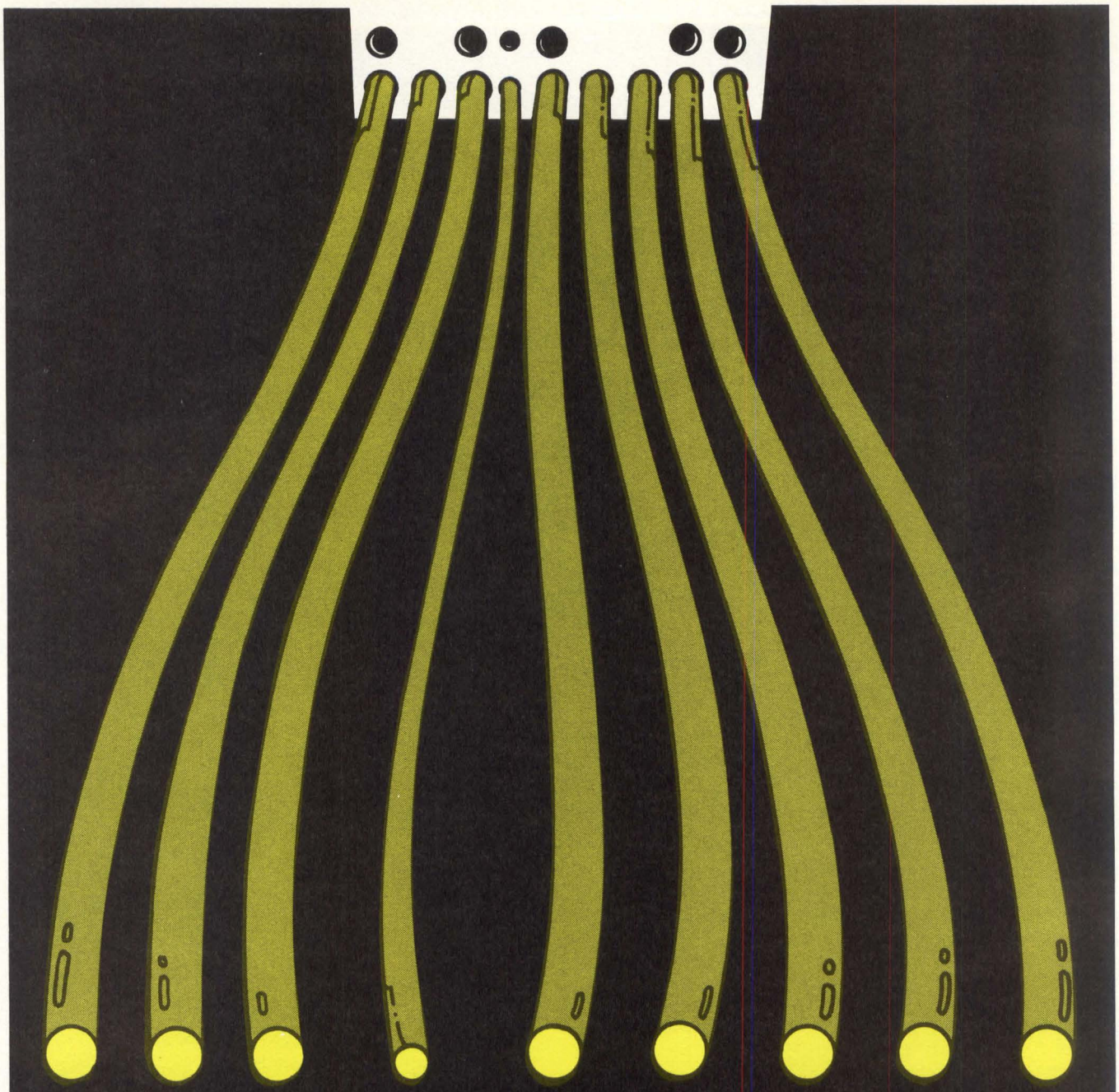


Built To Centralab Quality Specs.

IMPS Pushbutton Switches combine compact size, low cost and highest quality throughout.

- Silver or gold inlay wiping contacts for long-life and low-contact resistance.
- Less than 2 milliseconds contact bounce.
- SPST, SPDT, DPST, and DPDT switch contacts.
- Printed circuit, DIL socket or wire-wrap terminations available.
- 2.5 to 3.5 oz. actuation force (momentary).
- Choice of button interface — square or blade shaft (shown) — permits use of a variety of Centralab and industry standard buttons and keycaps.
- 10, 15, 20 or 25mm center-to-center spacing.

CIRCLE 62 ON INQUIRY CARD



Our readers make light work.

Decitek photoelectric punched tape readers were all designed with state-of-the-art reliability — a fiber optic light distribution system and a beautifully simple patented dual-sprocket drive, which eliminates the need for level switches, tape guides and keepers. Since fewer actual parts go into our readers, greater performance comes out. It also gives us the lowest spare parts volume in the business. Decitek has, in a few years come from nowhere to such a strong penetration of the market that we are now the number one supplier to the photo-typesetting OEM industry and gaining in the machine control and mini-micro computer field. We got where we are purely because of performance, quality, reliability and price.

We will work with you to make your equipment work better.

The more you know about punched tape equipment, the better you read us.

DECITEK

A DIVISION OF JAMESBURY CORP.
250 CHANDLER STREET, WORCESTER, MASSACHUSETTS 01602, U.S.A. (617) 798-8731

CABINETRY AND ENCLOSURES

Line of Specialty I, II, and III desks, chairs, and CRT work stations, as well as cubes, mounts, and printer stands are offered. The computer cabinetry, electronic enclosures, and related furniture support units vary in size, weight, and description depending upon customer requirements. Both std and custom-made products conform to government and business specs. **Systems Furniture Co,** 13900 S Figueroa St, Los Angeles, CA 90061.

See at Booth 1077
Circle 291 on Inquiry Card

COMPUTER DISPLAY MONITOR

Combining IC and CRT storage, the 19-in TEK 19/10 storage refresh graphics monitor stores more than 8500 alphanumeric characters in 3200 in (8100 cm) of vector. Store, store-refresh, and nonstore modes are provided and a direct view storage tube displays high density graphics at low computer overhead. Basic modules—CRT, low voltage power supply, and card cage—are mounted on a wire-form chassis. Display functions include view, erase, and copy. **Tektronix, Inc, Information Display,** PO Box 500, Beaverton, OR 97077.

See at Booth 1358
Circle 292 on Inquiry Card

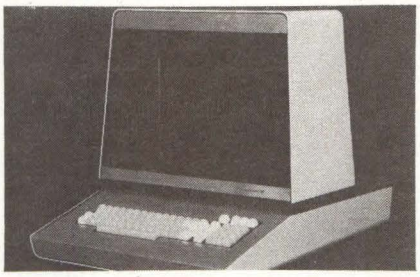
AUTOMATIC SEND/RECEIVE TERMINAL

Incorporating both a mini-cassette magnetic tape unit with 68k chars of removable storage and an 8k RAM, the Miniterm 1204 allows offline data preparation, editing, and reporting, providing complete simultaneous transmit/receive capability. Tape, memory, or keyboard to line transmissions occur at 1200 baud. The 3-mode keyboard has TTY, APL, or integral 16-key numeric cluster, and provides 35-char/s printing speed on the u/lc typewriter. **Computer Devices, Inc,** 25 North Ave, Burlington, MA 01803.

See at Booth 1513
Circle 293 on Inquiry Card

STANDALONE GRAPHICS TERMINAL

Desktop configuration is an upgraded ORION-60 series with resident BASIC containing graphics extensions, disc drive, and up 56k expandable RAM or ROM. The flexible 8080 microcomputer-based unit features touch panel option, ability to perform rear projection of film images through the screen, 2k-byte RAM for down loading special char, ability to emulate other terminals via firmware, and the ability to upgrade into intelligent standalone terminal. **Magnavox Display Systems,** 2131 S Coliseum Blvd, Fort Wayne, IN 46808.



See at Booth 1277
Circle 294 on Inquiry Card

MAGNETIC MEDIA

Designed for data and word processing applications, Verbatim™ media is a formulation of ferric oxides in a macromolecular binder system that adheres it to a polyester base film. Line includes removable magnetic data storage, discs, cards, and tape. With high density and parallel recording formats, cartridges are fully compatible with ANSI, ECMA and ISO stds. With long life and low abrasion, mag cards are interchangeable and compatible with IBM MC/ST cards; flexible discs offer 78 tracks and fit a variety of drives. **Information Terminals Corp,** 323 Soquel Way, Sunnyvale, CA 94086.

See at Booth 1032
Circle 295 on Inquiry Card

DATA CARTRIDGE SYSTEMS

DCS-100 packages two drives for the mini DC100A data cartridge with control, interface, and power circuitry in a self-contained unit. It is designed to require only mounting, power connection, and plugging into host circuitry. System allows single or double drive configurations; the interface cable permits up to four drives to be individually selected by control circuitry. For OEM users, basic system DCD-1B includes drive with built-in servo control and R/W circuitry. **3M Co, Mincom Div,** PO Box 33600, St Paul, MN 55133.

See at Booth 1621
Circle 296 on Inquiry Card

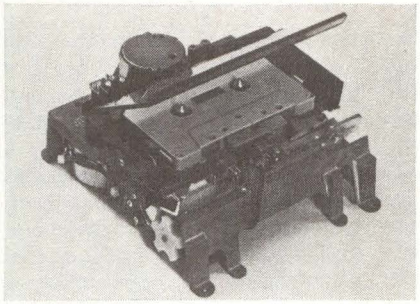
BAR CODE READER

Model 9210 offers dual connectors for ease of interface to allow tandem operation with online RS-232-C terminals and is designed for plug compatibility with most CRTs. With external switches for selection of baud rate, parity, and half- or full-duplex, unit is compatible with bit-serial rates from 110 through 9600 baud. Included is RUBY WAND® light pen for hand scanning codes. Variable length messages up to 32 char std or 64 char optional can be read. **Interface Mechanisms, Inc,** 5503 232nd St SW, Mountlake Terrace, WA 98043.

See at Booth 1845
Circle 297 on Inquiry Card

VARIABLE SPEED CASSETTE TAPE TRANSPORT

Phil-Deck model 3 features 4-motor control, remote control capabilities, fast start/stop, <30-s rewind, and ac or battery operation. Four separate motors control take-up, rewind, play or record, and head engagement, allowing complex tape deck functions to be accomplished by remote control. Flutter and wow and jitter are minimal because the capstan drive motor only moves the capstan. Control boards contain all circuitry for proper control of the transport. **Triple I, a div of The Economy Co,** 4605 N Stiles, PO Box 25308, Oklahoma City, OK 73125.



See at Booth 2015
Circle 298 on Inquiry Card

TELEPRINTERS

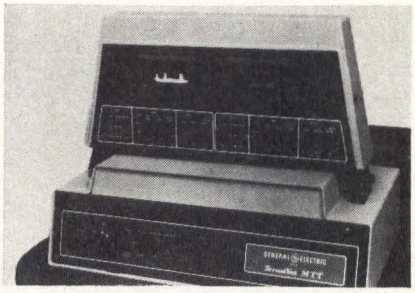
Featuring paper tape/memory ASR, 5-level code, 30-char/s speed, and Telex/private line, the model B 305 PS printer includes Telex controller, printer, paper tape punch and reader, editable memory, answerback, and keyboard. Impact 5 x 7 dot matrix printing is 69, 72, 74, or 80 char/line. RAM contains 4000 char minimum, expandable to 8000. Power is optional 115 or 115/230 V (strappable) 20 to −30%, 46 to 64 Hz; operating temp range is 0 to 50°C. **Extel Corp,** 310 Anthony Trail, Northbrook, IL 60062.

See at Booth 1654
Circle 299 on Inquiry Card

NCC PRODUCT REVIEW

MAGNETIC TAPE TERMINAL

Featuring character string search, high speed data transfer, and flexible editing, the TermiNet® MTT is equipped with two RS-232-C interfaces to accommodate a data set and printer, CRT, or auxiliary device. Available in single or dual cassette configurations, terminal also features extended search and block recording. Specs include ANSI compatible 2.5 x 4" (6.4 x 10.2 cm) twin-hub coplanar digital cassette with 300' (90 m) of 0.150" (0.38 cm) wide magnetic tape. **General Electric Co, Data Communication Products Dept,** Waynesboro, VA 22980.



See at Booth 1585
Circle 392 on Inquiry Card

PROGRAMMABLE DIGITIZER

Intelligent digitizer incorporates an 8080 microprocessor for accuracy and performance, enabling data to be preprocessed. The device can be modified for development of custom firmware. "Board level" firmware includes relocatable origin, binary/BCD conversion, metric output, incremental operation, scaling, rotational correction, area and angle calculation, and distance measurement. **Summagraphics Corp,** 35 Brentwood Ave, PO Box 781, Fairfield, CT 06430.

See at Booth 1170
Circle 393 on Inquiry Card

DATA LINK

Remote peripherals can now communicate with 360 or 370 mainframes via SDLC protocol without the need for NCP or VTAM software, as if connected locally. The PIX-II virtual data link consists of two minicomputer-based controllers. Local control unit plugs directly into the mainframe's byte multiplexer channel, and one of several remote control units are available for peripherals attachment. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33540.

See at Booth 1616
Circle 394 on Inquiry Card

COMPUTER TAPE

Universally adaptable to 556/800- and 1600/6250-bit/in drives, "G" tape is coated with 360-μin thick oxide for optimum electrical performance in both ranges. A specially formulated lubricant is dispersed through the magnetic coating to reduce static and alter the coefficient of friction by providing the slip characteristics necessary to assure trouble-free tape handling at any speed. The binder system adapts to wide extremes of temperature and humidity. **Wabash Tape Corp,** 2700 Des Plaines Ave, Des Plaines, IL 60018.

See at Booth 1255
Circle 395 on Inquiry Card

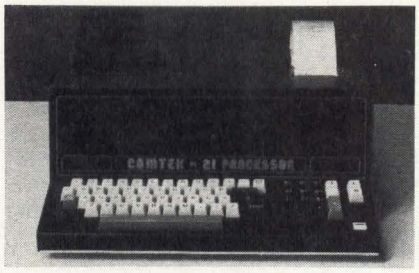
MULTIPLE FLOPPY DISC SYSTEM

TD-1 TermiDisk is equipped with one to four std IBM-compatible diskette devices with a 1M-byte storage capacity. Intended as a peripheral accessory for on-site or remote data terminals, basic system provides resident programs for file management and editing. Communication is by means of two serial ports (expandable to four), each capable of communication with 5-, 6-, 7-, and 8-bit data at 50 to 19,200 baud. Unit measures 10.2 x 11.2 x 20" (25.90 x 28.45 x 50.80 cm). **International Computer Products, Inc,** 2925 Merrell Rd, Dallas, TX 75229.

See at Booth 1511
Circle 396 on Inquiry Card

INTELLIGENT PROCESSOR

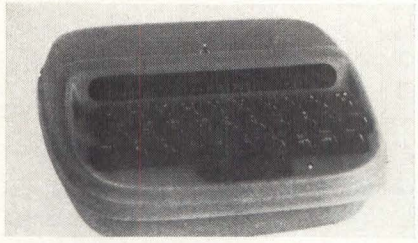
Featuring a mini floppy disc, model 21 processors contain an 8k RAM (12k optional), and a 1200-baud communications modem. Information is displayed on a 16-char alphanumeric prompting display. Other features include an alphanumeric keyboard, plus 10-key numeric pad; and a 25-col hardcopy alphanumeric printer which operates at 420 lines/min. Options are a 132-col, 125-line/min printer; light pen scanner; floppy disc; and parallel interface. **Comtek, Inc,** 4216 McCullough, San Antonio, TX 78212.



See at Booth 2045
Circle 397 on Inquiry Card

COMPUTER TERMINAL

Allowing 2-way data communications between user and RS-232 interface device, KDM/1 terminal with built-in 32-char alphanumeric LED display utilizes advanced semiconductor devices to provide reliable performance with digital systems, computer-controlled test equipment, and devices such as bar code readers and OCR scanners. It combines full ASCII keyboard, ac power supply, and RS-232 interface in single unit. KDM/2 has a 16 x 64-char display terminal and operates on a TV set; KDM/3 provides 24 x 80-char display on a video monitor. **Micon Industries,** 252 Oak St, Oakland, CA 94607.



See at Booth 1352
Circle 398 on Inquiry Card

FLOATING-POINT ARRAY PROCESSORS

Interfaced to work in parallel with most computers, the high speed programmable AP-120B processor typically increases throughput of minicomputers by a factor from one to 200. It is comprised of fast registers (with a 167-ns clock cycle), program source memory, data memory, and floating-point adder and multiplier; all are interconnected by seven parallel synchronous data buses. Parallel/pipelined units simplify programming process. **Floating Point Systems, Inc,** 11000 SW 11th St, Beaverton, OR 97005.

See at Booth 1571
Circle 399 on Inquiry Card

UNINTERRUPTIBLE POWER SUPPLIES

Intended for smaller applications, three static inverters provide 30, 60, and 100 kW. Digitally controlled, the step-wave inverter 3-phase, 60-Hz system allows 208 to 480 V in or out; 50-Hz systems allow 380 V. Also included are subcycle current control to correct voltage every 700 μs; steady-state voltage regulation; instant fault clearing current; and overload capacity 125% of rated kVA for 10 min, or as high as 300% line-to-neutral current for 10 cycles. **Exide Power Systems Div, ESB, Inc,** Rising Sun & Adams Ave, PO Box 5723, Philadelphia, PA 19120.

See at Booth 2050
Circle 400 on Inquiry Card

Zero RPM. The Disk that doesn't Spin.

Megastore goes where a disk drive used to go.

More to the point, Megastore keeps going long after a disk drive quits. Without motors, bearings, heads or platters, there's nothing to wear out, burn out or crash. No moving parts.

Megastore is the astonishing new fixed-head disk memory replacement from Ampex that uses reliable cores instead of rotating media. In the long run it saves a lot of money.

Megastore provides increased throughput, increased system availability, increased system uptime and reduced maintenance costs. A vastly better return on investment.

Unplug your disk and plug in Megastore. You'll get a half-million to four million bytes of capacity (in half-megabyte increments) that your existing software can't tell from the disk it was designed for. The only difference you'll see is a major improvement in throughput, because Megastore has a data access time that's anywhere from 1000 to 3000 times faster than the disk it replaces.

Megastore. Ready now as a software-transparent replacement for Novadisk (Megastore 1223) and DEC's RJSO3/RJSO4 Disk (Megastore 11). Also available as Megastore 4666 for users who wish to provide their own controller. Other versions on the way. Contact Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Phone (213) 640-0150. Ask for Megastore. The disk that doesn't spin.

AMPEX

Novadisk is a trademark of Data General Corp.

Visit the Ampex Memory Store, NCC Booth 1444.

CIRCLE 64 ON INQUIRY CARD

SYNCHRONOUS 16k MEMORY BOARD

Fast access units for use with Altair bus, 8080-based microcomputers combine synchronous operation without wait states and 16k bytes of low power Mostek 4096-15 RAM. Refresh circuitry is located onboard and timing signals are received from CPU. Power ratings for model 88-S16K are 5 V at 282 mA, −5 V at 9.25 mA, and 15 V at 72 mA. Permitting simultaneous access, Altair Timesharing BASIC supports four users although eight can be active with an increase in response time. It is configured as a partitioned system where all users have a fixed area of memory space. **MITS, Inc,** 2450 Alamo SE, Albuquerque, NM 87106.

See at Booth 1733

Circle 401 on Inquiry Card

ONLINE RETRIEVAL AND ANALYSIS SYSTEM

Used from an online terminal or in batch mode, the BASIS system contains a storage and retrieval module designed to search large files of textual or numeric information by subject area or data value, and retrieve information satisfying the search criteria. Other modules allow users to perform data analysis and data management tasks. The software operates on CDC 6000 series, DECsystem 10 and 20, IBM 360/370, Univac, and Sigma computers. **Battelle, Columbus Laboratories,** 505 King Ave, Columbus, OH 43201.

See at Booth 1116

Circle 402 on Inquiry Card

DISTRIBUTED PROCESSING SYSTEM

System 7000 permits concurrent data entry, data processing, file management, and data communications functions at local or remote locations. A 16-bit microcomputer, capable of high speed multitasking operations, provides intelligence for model 7115 standalone and 7110 master control terminals. System employs an interactive COBOL compiler enhanced for data entry. Master terminal with 64k bytes of memory supports up to seven local or remote terminals, four mass storage units, and 45-char/s to 600-line/min output printers. **Inforex Inc,** 21 North Ave, Burlington, MA 01803.

See at Booth 1691

Circle 403 on Inquiry Card

CRT TERMINAL

By means of microprocessor architecture, the 1500 is able to offer as standard features a built-in numeric cluster, cursor addressing, printer interface, u/lc, a display of 24 lines of 80 col, insert/delete line, dual intensity, and speeds up to 19.2k bytes/s. These features and capabilities were previously found only in CRTs of buffered or editing variety. At the networking level, the Modular One family has been expanded to include mainframe protocol compatibility for Burroughs (/b), Honeywell (/h), and Univac (/u) computers. **Hazeltine Corp,** Greenlawn, NY 11740.

See at Booth 1791

Circle 404 on Inquiry Card

120-CHAR/S TELEPRINTER

EDT 1232 keyboard send-receive (KSR) has a 1024-char buffer which permits effective character throughput of 120 char/s, eliminating the need for carriage return/line-feed fill characters. The unit's expanded carriage permits a full 132 print positions per line. Its std ANSI 4-row keyboard is capable of generating all 128 ASCII characters, including u/lc. The terminal transmits and receives data at 10, 30, and 120 char/s, switch selectable, in serial form. **Western Union Data Services Co,** 70 McKee Dr, Mahwah, NJ 07430.

See at Booth 2008

Circle 405 on Inquiry Card

MINIATURE CARTRIDGE DRIVE

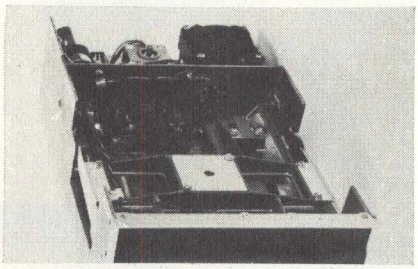
A microprocessor-compatible drive, model 200 MINIDRIVE™ uses 3M's DC100A cartridge. The 3 x 4 x 4.125" wide (7.6 x 10.2 x 10.48 cm) unit features design simplicity. An aluminum base plate provides mechanical integrity with automatic and positive cartridge positioning. A solid-state optical tachometer in the servo loop permits precise speed control of the low inertia dc motor. Available with 800-bit/in or optional 1600-bit/in packing density, resulting in a transfer rate of 24k or 48k bits/s at 30 in/s, the unit stores from 168k bytes to 772k bytes of data. **Qantex, Div of North Atlantic Industries,** 200 Terminal Dr, Plainview, NY 11803.

See at Booth 1842

Circle 406 on Inquiry Card

DOUBLE-SIDED FLOPPY DISC DRIVE

Offering twice the online storage of std drives, and 3-ms access time, the SA850/851 double-sided single/double density drive is the same physical size as the SA800 floppy (4.62 x 9.50 x 14.25", 11.73 x 24.13 x 36.20 cm); and is media interchangeable with the IBM 3740, S/32 single-sided, as well as IBM series/1 (model 4964) and 3600 series 2-sided, drives. The units read and write on any industry std diskette as well as the IBM 2-sided diskette 2. A dual index sensor differentiates between single and 2-sided diskettes. **Shugart Associates,** 415 Oakmead Pkwy, Sunnyvale, CA 94086.



See at Booth 1085

Circle 407 on Inquiry Card

DUAL DISKETTE DRIVE

Model 270 records and retrieves data on two removable flexible diskettes, providing 6.4M bits of data storage unformatted, or 3.8M bits in IBM 3740 format. Double density capability increases capacity to 12.8M bits. The drive is the size of most single diskette drives: 8.6 x 4.4 x 15.0" (21.8 x 11.2 x 38.1 cm), and has 33-ms random average seek; track to track access is 10 ms, including head settle time. The unit has 28-W power consumption; heat dissipation is only 109 BTU/h. **PerSci, Inc,** 4807 Glencoe Ave, Marina del Rey, CA 90291.

See at Booth 2014

Circle 408 on Inquiry Card

CRT TERMINAL

Intelligent terminal combines alphanumeric and graphics display capabilities and allows users to choose between color and black and white in a single unit. Internal operations are controlled by a Z80 microprocessor. Keyboard is made up of 61-key typewriter layout, 12-key cursor/function pad, and 12-key numeric/function pad. Communications capabilities are synchronous or asynchronous, 110 to 9600 baud program-selectable. Three serial ports are provided. **Ramtek Corp,** 585 N Mary Ave, Sunnyvale, CA 94086.

See at Booth 2039

Circle 409 on Inquiry Card

NOW DELIVERING

A Half Million Word Computer

THE ROLM 1666. Memory expansion to 576K words. Transparent mapping into 64K blocks for six users. Four-way memory protection. Privileged instructions with I/O allocation & protection.

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THE PACKAGE. Complete selection of peripherals. Both military & commercial specs. Fully integrated & documented. Supported by a wide range of systems software including RMX/RDOS.

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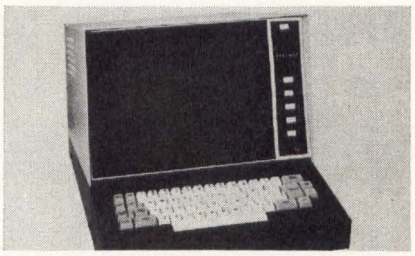
4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

In Europe: 645 Hanau, Muehlstrasse 19, Germany, 06181 15011, TWX 418-4170.

CIRCLE 65 ON INQUIRY CARD

CRT TERMINAL

Model 4041 has a full edit keyboard; the 119 keys include CRT function keys, editing keys, and system function keys. Optionally available are 15 function keys and eight additional editing keys. Also shown will be the Teledisk 2020 microfloppy disc terminal that is designed with two independent baud rates—one for the remote teleprinter or CRT and the other for a modem. **Teleray, Div of Research, Inc,** Box 24064, Minneapolis, MN 55424.



See at Booth 1847

Circle 410 on Inquiry Card

MINICOMPUTERS

Model 5116 single-board minicomputer in a floppy-disc-configured system contains 16 g-p registers, direct addressing to 64k bytes of memory, a microbus, and 256k-byte disc drive. Three other systems are the 8/16 16-bit program development system with a 2.5M-byte disc and 30-char/s printer; the 8/32 32-bit scientific system operating FORTRAN IV on 500k-byte memory with two 80M-byte disc drives; and a 7/32 32-bit commercial business system with 256k-byte memory and two 300M-byte discs. **Interdata Inc, a unit of Perkin-Elmer Data Systems,** 106 Apple St, Tinton Falls, NJ 07724.

See at Booth 1483

Circle 411 on Inquiry Card

INTELLIGENT TERMINAL SYSTEM SOFTWARE

Maximizing the use of data gathering networks to increase throughput, Level II Data Entry System (IDES) is a powerful general-purpose package developed for use with series 30 and 40 intelligent terminals. The application-oriented software consists of custom forms-generation procedures and data entry programming. This provides data entry, editing, and control with local data storage, concurrent local printing, and batch or interactive data transmission. **Incoterm Corp,** 65 Walnut St, Wellesley Hills, MA 02181.

See at Booth 1870

Circle 412 on Inquiry Card

AUDIO/DATA COMMUNICATIONS UNIT

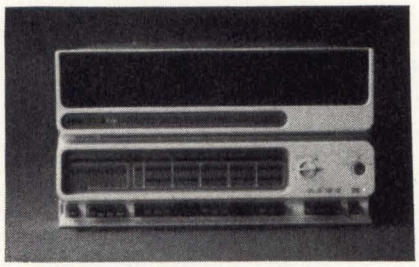
As a general-purpose controller, the ADC1500 is linked between the computer and telephone system to provide computer, voice, and FSK response to remote terminal devices. The unit multiplexes terminals through a single, serial communications channel. It handles up to 32 I/O lines with receiver data sets in 2-line increments, and provides up to 123 words (32-word increments). Other features include ASCII speeds of 110, 150, and 300 baud; and simultaneous operation of multiple I/O lines. **Wavetek Data Communications,** PO Box 651, San Diego, CA 92112.

See at Booth 1253

Circle 413 on Inquiry Card

MID-RANGE MINICOMPUTER

Eclipse S/130 features a user-microprogrammable control processor for high speed and supports concurrent timesharing, batch, and real-time operations. Packed in a 12-slot chassis with up to 256k bytes of MOS, core, or mixed main memory, the unit has bit, byte, word, and block instructions, as well as hardware interrupt vectoring and stack facility, multiply/divide, and automatic program load. Writable control store of 1k 56-bit words or p/ROM control store of 2k 56-bit words are available for custom instructions. **Data General Corp,** Southboro, MA 01772.



See at Booth 1215

Circle 414 on Inquiry Card

TAPE MESSAGE DISPLAY SYSTEM

A specialized message display system that provides key information about tape and disc mounts/dismounts directly at each peripheral unit, the 9850 display system uses the 20-char Burroughs Self-Scan II as the display device. Each display unit is microprocessor controlled, eliminating system downtime due to failure of a central control unit, and allowing each display unit to perform its own diagnostic self-testing to identify failure. **Texas Digital Systems, Inc,** PO Box 3701, Bryan, TX 77801.

See at Booth 2075

Circle 415 on Inquiry Card

HANDHELD TERMINALS

Interactive alphanumeric terminals include the HT/3 which displays a single line of 12 char and the HT/4 with 24 char in two lines. HT/5 has an annunciator display of 12 labeled lights which the computer system can turn on, off, or blink. The HT/8 provides display buffer capacity for 80 letters, numbers, and symbols, and operates at 10, 15, 30, or 120 char/s in full- or half-duplex mode. All provide 2-way, bit-serial, asynchronous communication of ASCII codes, and are RS-232-C compatible. **Termiflex Corp,** 17 Airport Rd, Nashua, NH 03060.

See at Booth 1600

Circle 416 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEMS

Providing precisely conditioned power for critical data/communications requirements, series 75/415-Hz system is based on a 75-kVA, 415-Hz frequency converter which may be used singly or in parallel for system redundancy or increased power capacity. The unit converts 60-Hz input power to conditioned 415-Hz output. Efficiency is 86% at full load. Standard features are output voltmeter and ammeter, battery voltmeter and ammeter, system fault alarms, and line drop compensation, 0 to 5%. **Teledyne Inet,** 711 W Knox St, Gardena, CA 90248.

See at Booth 1254

Circle 417 on Inquiry Card

EXPANDABLE p/ROM PROGRAMMER

The portable model 7, which is the basis of a versatile programming station, contains a 1k x 8 RAM (expandable in 1k increments) in its basic configuration. The universal p/ROM duplicator is capable of programming all commercially available p/ROMs. Options add serial or parallel data communications in interchangeable data formats; remote control by TTY, CRT terminal, or computer; and emulation of over 200 p/ROMs. Addition of a front panel converts it into a model 9. **Data I/O Corp,** PO Box 308, Issaquah, WA 98027.

See at Booth 1143

Circle 418 on Inquiry Card

Alumax Mic-6 cast aluminum plate. All it needs are your finishing touches.

By the time our Mic-6 cast plate reaches you, the tough work has already been done. It's been stress-relieved, precision-machined and cut to size. All you do is finish it.

What can you do with it? Almost anything. Mic-6 can be sawed, drilled, tapped or milled. And it can be welded or anodized. All at speeds compatible with today's processing equipment.

Mic-6 is held to exceedingly close tolerances. Plate thickness is ±.005". And its fine, precision-machined surface finish (typically 25 micro-inch) eliminates the high costs of in-plant surface machining.

All in all, it's the "answer material" for computers, printing systems, instrumentation, electronics and other high-spec OEM industries. It saves you the costs of permanent mold castings. And frees you from the eccentricities of wrought plate.

See your nearby Alumax distributor. Or write for the Mic-6 brochure that gives you complete information and specs.

Mic-6 cast aluminum plate from Alumax. We started it, you finish it.

ALUMAX
MILL PRODUCTS INC.

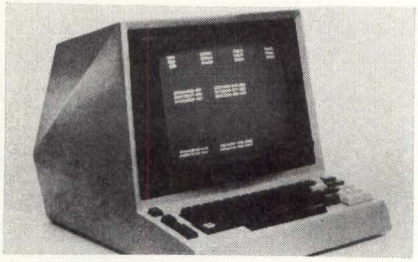
A subsidiary of Alumax Inc. 5555 E. Highway 6, Morris, Ill. 60450
West Coast office: 1495 Columbia Avenue, Riverside, California 92507

CIRCLE 66 ON INQUIRY CARD

NCC PRODUCT REVIEW

VIDEO DATA TERMINAL

Teletype-compatible VC303A features RS-232-C interface, 12″ nonglare CRT (displaying 1920 char), keyboard with auto-repeat and cursor control key cluster, direct cursor addressing, eight switch-selectable data rates from 110 to 9600 baud, and composite video output for up to 30 slave monitors. Lower case, switched serial and parallel auxiliary interfaces, and special character fonts including APL and French are optional. **Volker-Craig Ltd,** 266 Marsland Dr, Waterloo, Ontario N2J 3Z1, Canada.



See at Booth 1095
Circle 419 on Inquiry Card

SOLID-STATE MASS MEMORY

Organized to look like a rotating head/track magnetic disc memory, the solid-state semiconductor disc memory uses CCDs as memory elements. Providing capacity for up to 1M-bytes in one 8-board system, the unit has an average access time of 500 ns, transfers data at 2 to 4 MHz, and requires <100-W operating power. Plug-in memory boards carry CCD chips; capacity is field expandable in 128k-byte increments. **Alpha Data Inc,** 20750 Marilla St, Chatsworth, CA 91311.

See at Booth 2071
Circle 420 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEMS

Rack mount 82000 series, 500 VA to 1500 VA, single-phase output systems feature high reliability, rugged construction, external batteries, and excellent noise suppression. Output voltage variations do not exceed 20% of the steady-state value for step-load changes of 50%. Low level battery contacts are provided with optional audible alarm and acknowledge switch; transfer alarm relay contacts are provided with optional transfer switch. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.

See at Booth 1177
Circle 421 on Inquiry Card

The new generation of Diskette Drives is here and under control.

PerSci has it–a family of diskette drives "design-years" ahead of competitive drives–now available in complete low cost subsystems for interface to 8080, 6800 and other major microprocessors.

The Highest Performance Diskette Drives:

PerSci diskette drives, both single and dual head units, offer a combination of performance features unique in the marketplace while still maintaining compatibility in existing systems:

- ☐ Voice coil positioning for access speeds seven times faster than competitive drives (76 tracks in 100 ms)
- ☐ A low power all DC system reduces cost and assures high reliability
- ☐ Automatic electric loading simplifies operation and protects media
- ☐ Small size permits 5 single drives or 4 dual drives to be mounted vertically in a 19 in. rack

The Most Powerful Diskette Drive Controller

The PerSci Model 1070 Diskette Drive Controller puts the advanced performance of PerSci drives to work in microprocessor based systems. An IBM format compatible, "intelligent" controller, the Model 1070 will handle from 1-4 drives with minimum demand on the host system.

In fact, with addition of a power supply and keyboard to the PerSci subsystem, the user can perform many floppy disk routines without additional hardware or software. Controller features include:

- ☐ 8080 microprocessor
- ☐ Formatter/control IC
- ☐ 4K disk operating system
- ☐ 1K data buffer
- ☐ 8080 or 6800 microprocessor interfaces
- ☐ RS-232 serial interface optional
- ☐ IBM data format

An Economical Diskette Drive Subsystem

A complete subsystem including a single diskette drive (Model 70), the Model 1070 controller with interface and a controller-to-disk-drive cable is available in single units or OEM quantities. For double capacity, a dual diskette drive (Model 270) subsystem is also available. Don't settle for yesterday's diskette drive. Get the new generation under control from PerSci, 4087 Glencoe Avenue, Marina Del Rey, CA 90291 (213) 822-7545.

PERSCI

Peripherals a Generation Ahead.

NCC PRODUCT REVIEW

DISTRIBUTED PROCESSING SYSTEM

Mainframe architecture of the 1600 allows maximum concurrent processing, modularity, and balanced cost/performance. The disc-based ECOS operating system permits a multitask environment featuring interactive processing, batch processing, media conversion, and remote batch transmission sharing the same files and peripherals. The system supports model 1675 CRT keystation terminals displaying up to 1920 char, located locally or remotely. **Harris Corp, Data Communications Div,** 11262 Indian Trail, PO Box 44076, Dallas, TX 75234.

See at Booth 1333

Circle 422 on Inquiry Card

FIXED DISC DRIVE

Providing up to 74M bytes of memory in a 7 x 23.5 x 19" (17.8 x 58.7 x 48 cm) package, the 3300 series includes six moving-head models in capacities starting at 12.4M bytes. Two fixed-head-only models provide capacities of 2.97M and 5.94M bytes. Fixed heads can be added to moving-head models to a max of 2.2M bytes; they have an avg access time of 10.1 ms and can be accessed while positioning the moving heads. The drives feature compact rotary positioner, IBM 3340 Winchester-type heads, and media. Max weight is 65 lb (29.5 kg) including power supply. **Okidata Corp,** 111 Gaither Dr, Mt Laurel, NJ 08054.

See at Booth 1533

Circle 423 on Inquiry Card

OCR DOCUMENT TRANSPORT AND READER

When used with the company's M9 electronic module, the Datareader provides high level character resolution and front panel sensitivity adjustments for tuning or detuning recognition circuits. Vertical adjustment of read heads allows scanning of forms from a min of 1 x 2.5" (2.54 x 6.35 cm) to a max of 6 x 8.75" (15.24 x 22.225 cm). Unit can read and process up to 3900 documents/h in a variety of fonts. Additional features include a jam detection device and autofeed mechanism to ensure single document selection. **Key Tronic Corp,** Bldg 14, Spokane Industrial Park, Spokane, WA 99216.

See at Booth 1354

Circle 424 on Inquiry Card

32-BIT PROFITABILITY

Profit from our 32-bit experience.

Scores of customers are taking advantage of our lead in 32-bit design right now, because we were there first . . . with the first mini with true 32-bit architecture. Hundreds of Interdata Megamini® computers have been working throughout the world since 1973.

Interdata's 8/32 computer processes data at one-half the speed of the IBM 370/158, for about one-tenth the cost. And the Model 7/32 offers even greater economies. With our Multiport Memory System, up to 14 processors can share a single memory bank, increasing throughput and processor-to-processor operation even further.

And, although they cost as little as the 16-bit DEC 11/70 or DG Eclipse, Interdata's Megaminis are the only low-priced computers with no constraint on program size. That's just one benefit of 32-bit architecture.

You also get 219 IBM-like standard instructions, and can create even more of your own with up to 512 words of Interdata Writable Control Store, raising throughput by a factor of five. And for still greater throughput, Interdata's exclusive Hardware Floating Point option improves the speed of scientific calculations ten times faster than software-bound minis.

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Send me 1977 specs on your 7/32 and 8/32 Processors and field proven software.

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CIRCLE 70 ON INQUIRY CARD

NCC PRODUCT REVIEW

GRAPHICS DISPLAY TERMINAL

The AG-60 graphics/alphanumerics terminal offers a choice of functional capabilities, including three char sets, two graphics sets, and alphanumeric cursors. A 12″ (30.48 cm) diag plasma panel presents a 512 x 512 dot matrix. Selection of input devices includes two keyboards, touch panel for menu selection, or sonic pen for interactive graphics. Others may be added. Ten control functions and EIA RS-232 interface are std. **Applications Group, div of Eprad, Inc,** PO Box 4712, Toledo, OH 43620.

See at Booth 1759

Circle 425 on Inquiry Card

INTELLIGENT DISPLAY SYSTEMS

Online data entry is possible with 250 series user-programmable, IBM 3270-compatible remote display stations, standalone terminals, and printers. Screen capacities are 480 or 1920 char; also available are two keyboard arrangements, printers from 66 to 180 char/s, and binary synchronous communications from 1200 to 4800 bits/s. Each station has a microprocessor with 8k bytes of ROM and 6k bytes of programmable memory connected to a control unit. **Sycor, Inc,** Ann Arbor, MI 48104.

See at Booth 1205

Circle 426 on Inquiry Card

INTELLIGENT NETWORK PROCESSOR

The 6030 provides advanced data management functions at the nodes of a communications network. Based on microprocessor architecture, and designed modularly for growth in size and capabilities, the unit functions as a statistical multiplexer, combining signals from a number of terminal devices so that there is a finite probability that a device will be allocated a subchannel on the high speed link. **Codex Corp,** 15 Riverdale Ave, Newton, MA 02195.

See at Booth 2062

Circle 427 on Inquiry Card

YOU CHOOSE THE WINNER

PROCESSOR	6/16	NOVA 3/4	PDP-11/04
Data Type Lengths (bits)	4,8,16,	16	1,8,16
Instruction Word Length (bits)	16,32	16	16,32,48
General-Purpose Registers	16	4	8
Hardware Index Registers	15	2	8
Maximum Memory Available (KB)	64	64	56
Directly Addressable Memory(KB)	64	2	56
Automatic Interrupt Vectoring	Standard	N/A	Standard
Parity	Optional	Optional	N/A
Cycle Time (nanoseconds)	600	800	725

PRICE	6/16	NOVA 3/4	PDP-11/04
8KB Processor	$2200	$2600	N/A
16KB Processor	$2800	$3200	$3795
32KB Processor	$4000	$4400	$4995
Multipy/Divide Hardware	$ 950	$1400	$1820

Interdata's 6/16 wins the battle of the specs.

Not only do we cost less than the Nova 3/4 and the PDP-11/04, we have more features. Just compare: 16 general purpose registers on the 6/16 to simplify programming and reduce fetches . . . only 4 in the Nova and 8 in the 11/04; 15 hardware index registers on the 6/16 against 2 for the Nova and 8 for the 11/04; 64 KB of directly addressable memory instead of just 2 KB for the Nova 3/4 and 56 KB for the PDP11/04.

What's more; all these hardware features enhance the nimble 6/16's performance. Its cycle time is only 600 nanoseconds, compared to 800 for the Nova and 725 for the 11/04.

Interdata's comprehensive software drives this powerful hardware full out. You get the field-proven OS/16 MT2, a real-time, multi-tasking operating system providing instantaneous response to events, while allowing the user to minimize memory by storing non-critical functions on disks. And the 6/16 can be programmed in your choice of FORTRAN, BASIC or MACRO CAL.

All this and save money too, as much as one-third less than a PDP-11/04 and substantially less on a Nova 3/4 . . . with OEM discounts saving even more.

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Get the whole story. Just fill in the coupon or call (201) 229-4040.

Send me 1977 specs on your Model 6/16

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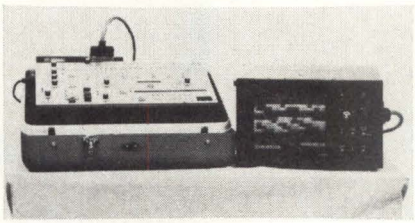
Oceanport, New Jersey 07757, U.S.A. CD-6

CIRCLE 72 ON INQUIRY CARD

NCC PRODUCT REVIEW

DATA COMMUNICATIONS MONITOR

INTERVIEW, a CRT monitor for displaying data communications transmissions, when used with INTERSHAKE® I or II, provides a clear display of all data traffic, or traffic from a selected terminal or location. Allowing visual observation of up to 1024 char in either text, hex, or octal, the unit aids in isolating hardware or software faults in data communications systems. Operation is full- or half-duplex at data rates up to 56k bits/s. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.



See at Booth 1067

Circle 428 on Inquiry Card

LINE PRINTER CONTROLLERS

Operating several printer models, the H-P 2100 controller is transparent to the host computer. Completely compatible with diagnostics, drivers, and operating systems, it is a single PC board requiring one slot in the H-P chassis. Also offered are LSI-11 modules, which configure to DEC 11/03 equivalent operation, and the 8063 multiplexer for Nova computers which provides an RS-232 interface for four or eight asynchronous data sets or local terminals. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.

See at Booth 1081

Circle 429 on Inquiry Card

LSI MODEM

Advanced LSI design of the 4196 data set enables bridging up to 2 s of transient line impairments without retraining, and elimination of analog drift. Transmission rates of 4800, 7200, or 9600 bits/s are selectable by switch or at the direction of DTE equipment connected to the RS-232-C interface cable. Operation is full-duplex, synchronous, binary, serial over a 4-wire 3002-type channel. LED status indicators provide visual monitoring of equipment and line operations. **Western Union Information Systems,** Mahwah, NJ 07430.

See at Booth 1166

Circle 430 on Inquiry Card

THE NEW SPINWRITER PRINTERS. THE BETTER PERCENTAGE MACHINES: 20% FASTER. 30% MORE CHARACTERS. 50% LONGER LIFE. 10% QUIETER...

...AND 10% LESS COSTLY.

Systems builders and OEM buyers today can select from several good character printers. That's why NEC built the Spinwriter printers to be better than today's best.

The five models in the Spinwriter series operate in every application at up to 55 characters per second — which is a faster effective rate than competitive models. They can store 128 characters on a print wheel — 36% more than the usual 94 characters others provide. Major components use the most advanced technologies for added durability; the reinforced plastic in the Spinwriter's unique "thimble" print element lasts three million impressions. And the Spinwriter is quiet — 60 dbs or less — so it can be used without special deadening in almost any application.

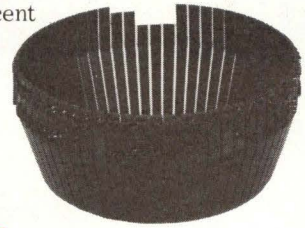
Since printers are an increasing percentage of total systems costs, the Spinwriter is priced better too. In moderate OEM quantities, you save 10 percent or more — savings that can make your product more competitive or your business more profitable.

Select from five Spinwriter models to meet your exact needs. The Model 5510 is a receive-only (RO) printer ideal for applications in which keyboard input is not required. The Model 5520 has a full built-in keyboard to perform keyboard send-receive (KSR) functions. For word processing usage, the Model 5530 is available with impeccable print quality, no change in mechanism and full 55 cps print speed. Special-purpose units include the Model 5540 split-platen printer, and the low-cost Model 5500, a components kit for OEM buyers wishing to add their own electronics and housing.

Every Spinwriter printer comes with LSI and microprocessor control-oriented architecture, up to five optional interfaces, full ASCII-code compatibility, 10- or 12-pitch characters, many typefaces, RS-232-C compatibility and numerous reliability features and operator aids.

But those are just the beginning of the Spinwriter's capabilities.

Spinwriter printers. They are big percentages better for your printing needs — today and tomorrow.



NEC NEC INFORMATION SYSTEMS, INC.
5 Militia Drive, Lexington, Massachusetts 02173
(617) 862-3120

CIRCLE 75 ON INQUIRY CARD

NCC PRODUCT REVIEW

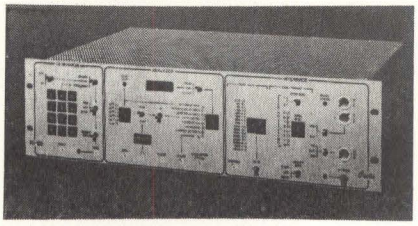
DATA COMMUNICATIONS TERMINAL

Utilizing microprocessor control, SuperTerm 120-char/s printer-terminal features an RS-232-C interface, IBM Selectric-configured keyboard, 22-key numeric pad, 132-col print width, cartridge ribbon system, and 7 x 7 matrix impact printing. Text-optimized printing increases throughput by automatically tabbing over white space to next printable character. Automatic reverse printing option enables bidirectional printing. **Intertec Data Systems Corp,** 1851 Interstate 85 S, Charlotte, NC 28208.

See at Booth 1765
Circle 431 on Inquiry Card

DATA COMMUNICATIONS TEST SET

The microprogrammed TC-100 simulates and tests components as well as system hardware and software with keyboard entry feature. Portable version provides RS-232 control signal breakout. Set is divided into three sections—generator with keyboard, transmit control and patterns, single error, and test points; analyzer with display, analysis modes, and test points; and interface with data rate and format, panel check, monitor select, and connectors. **Dynatech Laboratories, Inc, Cooke Engineering Div,** 900 Slaters Ln, Alexandria, VA 22314.



See at Booth 1595
Circle 432 on Inquiry Card

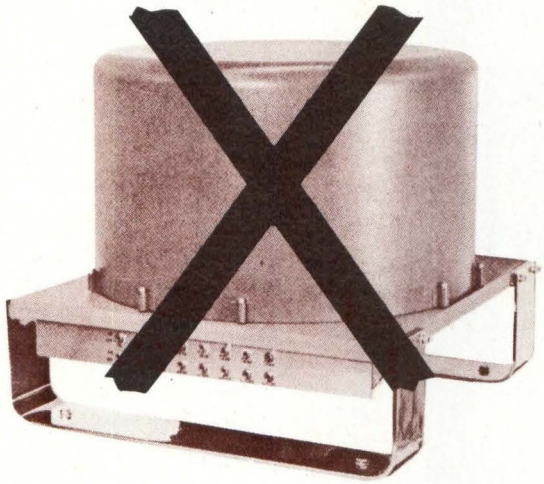
CRT TERMINALS

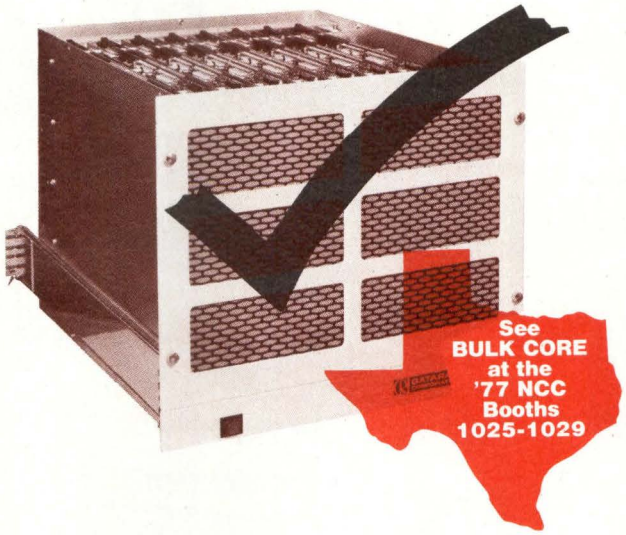
A microprocessor-oriented CRT with full array of editing features, the Micro-Tec™ includes user-definable function keys, programmable video presentations, and adjustable viewing angles. A 12" (30.48 cm) screen displays the 128-char set. The 7 x 9 dot matrix chars measure 0.20 x 0.08" (0.508 x 0.203 cm). Further specs include half/full-duplex, buffered modes, 15 operator-switchable speeds, and max baud rate of 9600. Options include data panel, printer interface, and polling. **TEC, Inc,** 2727 N Fairview Ave, Tucson, AZ 85705.

See at Booth 1838
Circle 433 on Inquiry Card

DEC® RC-11 and RF-11 fixed-head disc...and
Data General Novadisc® users:

Replace Fixed-Head Disc with Dataram BULK CORE





Now, all the remarkable features of Dataram's BULK CORE memory system are available to you in a unique storage peripheral with complete interfaces to emulate DEC and Data General fixed-head discs.

Basic building block of this dramatic, new peripheral is Dataram's BULK CORE module, which provides 256 kilobytes of storage on a single board. Eight of these modules can be packaged in a standard 19" chassis to provide two megabytes of storage.

To give you more of what you can't get from fixed-head discs. BULK CORE gives you microsecond-range access time, high reliability, and greatly improved maintainability. And at a price unheard of for core or semiconductor memory. Until now.

Until Dataram made its BULK CORE memory system plug-compatible with PDP-11 and Nova® minicomputers. To provide:

- Access time 1/10,000 of FHD
- High Throughput
- Zero Error Rate
- Self-Test for Fault Isolation
- Hardware & Software Transparent
- LED-spotlighted Fault Isolation
- 256 KB Modularity
- Non-Volatile
- Non-Mechanical
- High MTBF/Low MTTR
- Low Power
- Parity Check

Reasons enough to find out more about BULK CORE. If you use a DEC or Data General minicomputer—or any kind—and want to move ahead in performance, move a BULK CORE into your system.

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PRINCETON-HIGHTSTOWN ROAD
CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

I'd like to learn more about BULK CORE for my
☐ PDP-11 ☐ Nova ☐ _____
☐ Please send information.
☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

☐ Please send me information about Dataram's ADD-ON/ADD-IN memory for minicomputers.

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Nova and Novadisc are registered trademarks of Data General.

CIRCLE 77 ON INQUIRY CARD

PORTABLE TAPE UNIT

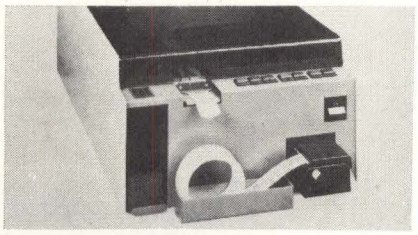
The high speed T-511 aids data communications diagnostics by recording all traffic on both sides of a data link for instant replay and analysis. Weighing 25 lb (11.34 kg), the instrument provides full-duplex data stream tape recording, records line speeds from 50 to 56k bits/s, and accommodates all codes and disciplines. Unit stores 2.4 to 60 min of traffic. Tapes are produced at speeds below 44k bits/s for replay on the D-601 Datascope. **Spectron Corp,** Church Rd and Roland Ave, Mt Laurel, NJ 08057.

See at Booth 2043

Circle 444 on Inquiry Card

PAPER TAPE READER/PUNCH

This 58-dB combination reader/punch attaches to any terminal through an RS-232 or current-loop connector. Full/half-duplex, line/local, search/edit control, back space, tape feed, and selectable baud rates of 110 and 300 are std features. The 12" (30.48 cm) wide SRP-300 may be remotely controlled from line or terminal through std DC1-DC4 codes. MODUPERF tape punch mechanism cuts paper, mylar, rolled, and folded tapes. **Data Specialties, Inc,** 3455 Commercial Ave, Northbrook, IL 60062.



See at Booth 1525

Circle 445 on Inquiry Card

PERIPHERAL SWITCHES

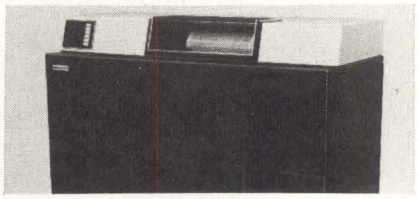
Family of switching equipment is specifically compatible with several mainframes, with switches for most minicomputer suppliers. Intended primarily for use in distributed data processing and online inquiry response applications, each switch is compatible with a specific computer; however, all feature the capability to switch peripherals quickly and all are suited to remote control via manual instruction or by direct computer drive or address. **T-Bar, Inc,** 141 Danbury Rd, Wilton, CT 06897.

See at Booth 1811

Circle 446 on Inquiry Card

LINE PRINTER

A high speed line printer, the DOC 2000 contains an integrated microprocessor controller and can print 2000 lines/min, single-spaced, using a 48-char set with fully buffered print line of 132 char. Controller communicates with host, decodes commands, controls printer hardware, and reports errors and status. Std features are interchangeable char arrays, and universal char set buffer. In-depth fault locating and hardware timing diagnostic panel is optional. **Documation, Inc,** PO Box 1240, Melbourne, FL 32901.

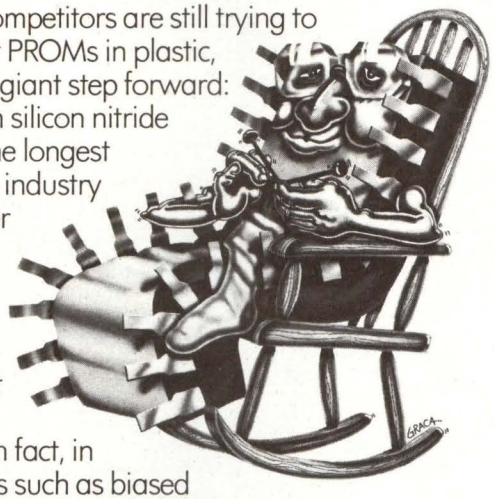


See at Booth 1643

Circle 447 on Inquiry Card

BIPOLAR MEMORIES

FAIRCHILD INTRODUCES PLASTIC PROMS THAT WILL LIVE TO A RIPE OLD AGE.



While many of our competitors are still trying to figure out how to put PROMs in plastic, we've taken another giant step forward: Plastic packages with silicon nitride protection to make the longest lasting PROMs in the industry about six times longer lasting.

That's because silicon nitride inhibits latent device failure by holding out moisture and ionic contamination. In fact, in accelerated tests such as biased 85/85, MTBF on industry standard plastic PROMs was 2,000 hours, while MTBF on our plastic PROMs was 13,000 hours. And, in the real world of systems applications, they're equivalent to hermetic packages.

WE HOLD ALL THE RECORDS FOR FAST.

For all their reliability, Fairchild PROMs don't sacrifice a nanosecond in speed. They're still the fastest on the market. Up to 30% faster than most.

And the simplest to program. The breadth of our line pretty much speaks for itself, so we'll let it:

PROM Part No.	Organization	Output	0-70°C T_{AA}
93417	256 x 4	OC	45 ns
93427	256 x 4	3S	45 ns
93436	512 x 4	OC	50 ns
93446	512 x 4	3S	50 ns
93438	512 x 8	OC	55 ns
93448	512 x 8	3S	55 ns
93452	1024 x 4	OC	55 ns
93453	1024 x 4	3S	55 ns

STEP RIGHT UP, THERE'S NO WAITING.

If you need fast, reliable, simple-to-program PROMs, and you need them now, you're in luck. Because all ours are available now.

To place an order, or to learn more, write or call your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to call our BIPOLAR MEMORY people direct. Fairchild Camera and Instrument Corporation, 464 Ellis St., Mountain View, California 94042. Tel: (415) 962-3951. TWX: 910-373-1227.

FAIRCHILD

CALL US ON IT. (415) 962-3951

CIRCLE 79 ON INQUIRY CARD

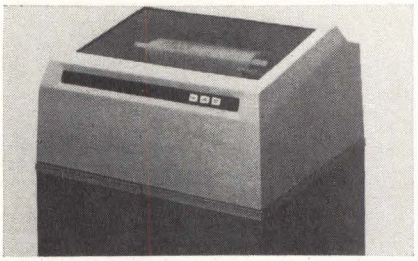
DISC STORAGE SYSTEM

Flexible DD-50 system permits interfacing disc controllers to mass memory peripherals to form cost-effective mass memory disc systems. Computroller V series is designed for PDP-11, Data General Nova or Eclipse, and Interdata minicomputers. Hardware compatibility and software transparency are std, enabling operating systems to run without changes. Features include ECC error correction, microprocessor technology, emulation, and increased throughput. **Diva, Inc,** 607 Industrial Way W, Eatontown, NJ 07724.

See at Booth 2012
Circle 448 on Inquiry Card

MATRIX LINE PRINTERS

With print speeds of 375 and 500 lines/min, T-5000 series features 9 x 7 half-space matrix font, full line buffering, 64-char set, 11-in/s (27.94-cm/s) slew speed, 132 print positions at 10 char/in (4/cm), and dual adjustable tractors for widths of 4 to 16.75" (10.16 to 42.55 cm). Units use the helix printing principle. All functions and characters are controlled by a microprocessor. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.



See at Booth 1283
Circle 449 on Inquiry Card

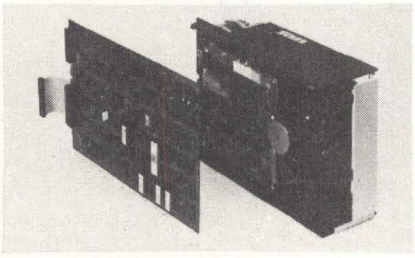
MAGNETIC HEADS

IBM-compatible 7- and 9-track magnetic tape heads feature ferrite erase heads and long life characteristics. They come in all speeds and densities, including GCR. Magnetic disc heads include type 2314, with 100 and 200 tracks/in (39.3 and 78.7/cm); and 2200 and 4400 bits/in (866.1 and 1732.3/cm); 3330 type with 192 and 370 tracks/in (75.6 and 145.7/cm); plus Winchester. All types of floppy disc heads and cassette and cartridge heads are also available. **Magnusonic Devices, Inc,** 290 Duffy Ave, Hicksville, NY 11801.

See at Booth 1725
Circle 450 on Inquiry Card

FLOPPY DISC SYSTEM KIT

Kit consists of a microprocessor-based disc controller (for IBM-compatible or dual-density formats); one to four floppy disc drives; interconnecting cable from controller to disc drives; and an 8-bit bidirectional hardware I/O interface for connection to microcomputers. The 1-board controller provides hardware for functions generally done in software. Additional disc drives are daisy chained from the first. **Sykes Datatronics, Inc,** 375 Orchard St, Rochester, NY 14606.



See at Booth 1722
Circle 451 on Inquiry Card

Anode lead wire for impressed current anodes for use in deep ground beds, sea water and other severe cathodic protection environments.

Jackets for use as cladding over glass fiber bundles in transportation applications utilizing fiber optics.

Electrical heat tracing systems maintain process temperatures in liquid-handling systems (pipes, valves and fittings). Also used to freeze-protect pipes under extreme climatic conditions.

Heat shrinkable tubing protects critical diodes and capacitors, carbon deposited resistors and provides support for butt-welded connections.

Solder sleeves provide electrical solder connections for wires, cables, cable shields and coaxial cables.

Insulated terminals for nuclear power plant, aircraft, aerospace and pipeline installations.

Cable ties for nuclear and other tough environmental applications.

Jacket cable constructions for aerospace, electrical and electronic systems, airframe wiring, outerspace environments, high density wiring and other complex circuitry.

KYNAR® Resin protects your wiring system end to end.

It's the unique balance of these properties that enables KYNAR to perform in many tough applications:

Kynar can be marked, printed, striped, or hot stamped for identification. It can also be pigmented for color coding.

Kynar has high dielectric strength and good insulation resistance.

Kynar has a temperature range from −80° to +300°F.

Kynar is nondripping, self-extinguishing (UL STD 94 V-0) and has an LOI (Limiting Oxygen Index) of 45.

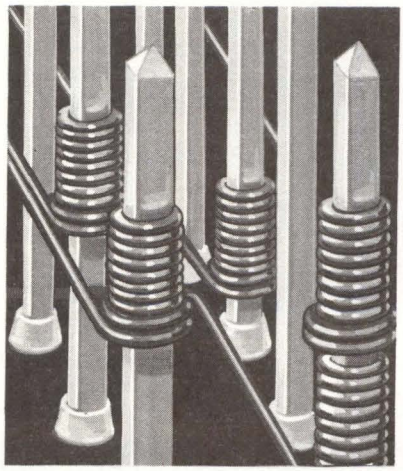
Kynar has good chemical resistance, low permeability.

Kynar has a tensile strength of 7000 psi. It is mechanically strong and has good abrasion and cut-through resistance.

Kynar has low-moisture absorption (0.04%), excellent radiation and UV resistance.

For list of fabricators, more technical data, specifications (UL and military), write or call Joe Michaud. Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7520.

*KYNAR is Pennwalt's registered trademark for its polyvinylidene resin.



Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels.

PENNWALT
CHEMICALS ■ EQUIPMENT
HEALTH PRODUCTS

CIRCLE 81 ON INQUIRY CARD

TELEPRINTER TERMINAL

A 60-char/s desktop terminal, the 860 is designed for interactive operation with host mainframe timesharing or transaction processing applications. Features include a 9-wire dot matrix print element, which provides high resolution 9 x 5 dot matrix u/lc chars in a 12 x 9 character cell; full last line visibility during operator input activity; and 132-col printing at recovery speeds of up to 90 char/s. Keyboard includes a 17-key numeric pad, n-key rollover, and auto repeat features. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.

See at Booth 1780

Circle 452 on Inquiry Card

NETWORK ADAPTER

Series A adapters interconnect computing equipment of any manufacturer into a long distance, high performance network. They provide communication between installation equipment from 50M bits/s at 1000 ft (304.8 m) to 1.5M bits/s at 1 mi (1.609 km) on a single coaxial cable. Serial data transmission and buffering of control and data allow effective interconnection. Each data path features multiple drops. **Network Systems Corp,** 6820 Shingle Creek Pkwy, Brooklyn Center, MN 55430.

See at Booth 1178

Circle 453 on Inquiry Card

MAGNETIC RECORDING HEADS

Long life "Thrift" heads for financial and credit card applications are constructed with DURACORE™. This high permeability magnetic alloy provides a wear ratio at least 10 times greater than Hi-Mu 80 materials. Long wear properties are provided without changes in head electrical characteristics. Workable alloy can also be used to form case shields and cores. Track 2 is a read track; track 3 is write/read. **Nortronics Co, Inc,** 8101 10th Ave N, Minneapolis, MN 55427.

See at Booth 1266

Circle 454 on Inquiry Card

FLOPPY DISC SYSTEM

Consisting of controller, DMA interface, and up to four IBM 3740-compatible disc drives, an option for PDS-1G and PDS-4 graphic display systems includes FDOS, a macro editor, assembler, and debugger. FORTRAN IV with graphic extensions is also supported. Minimum requirements for application development are 16k core memory and a 2-drive floppy system. IBM 3740 hardware compatibility allows media transfer. Application software can be written to provide data format and program compatibility. **Imlac Corp,** 150 A St, Needham Heights, MA 02194.

See at Booth 1581

Circle 455 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEMS

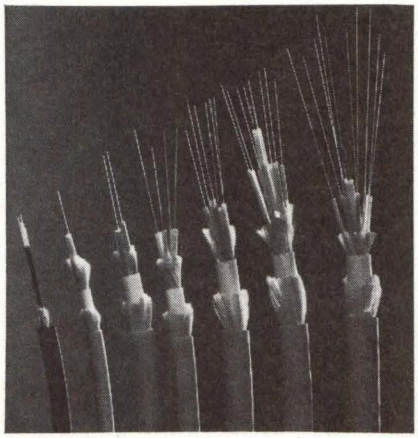
In three sizes—375 kVA/300 kW, 75 kVA/415 Hz, and 15 kVA—the systems utilize pulse-width modulation techniques to synthesize ac inverter output. Uninterruptible power devices have improved efficiency and reliability, and superior dynamic voltage regulation in comparison to earlier devices. **International Power Machines Corp,** 3328 Executive Blvd, Mesquite, TX 75149.

See at Booth 1626

Circle 456 on Inquiry Card

OPTICAL CABLE

Step-index (model 1300) and graded-index (1302) cables incorporate seven Corguide™ fibers in a rugged urethane cable structure suited to indoor and outdoor use. In addition to wide bandwidth and low attenuation (20 dB/km max), the cable is small in diameter, lightweight (25 kg/km max), and flexible. It is not susceptible to electromagnetic interference or pulses, and provides high degree of intercept security and dielectric isolation. **Corning Glass Works, Telecommunications Products Dept,** Corning, NY 14830.



See at Booth 2002
Circle 457 on Inquiry Card

BUSINESS PROCESSOR

Featuring 120k user memory, internal memory speed of 600 ns, advanced memory space handling, and enhanced instruction set, the 6600 advanced business processor incorporates a microprogrammable controller which executes a 16-bit microinstruction in 150 ns. Processor includes keyboard, video display, and dual cassette tape decks and is designed for use with disc-based systems. It can support up to 24 display terminals. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.

See at Booth 1005
Circle 458 on Inquiry Card

WORD PROCESSING SYSTEM

The OP-1 intelligent terminal performs editing and test manipulation functions. Large display, terminal keyboard processor logic, memory, and five slots for peripheral controllers are combined into a standalone desktop unit. The terminal can be programmed for on/offline use in synchronous or asynchronous modes, or for emulation. Device contains three microprocessors for CPU functions, I/O handling, and display control. **Ontel Corp,** 250 Crossways Park Dr, Woodbury, NY 11797.

See at Booth 1197
Circle 459 on Inquiry Card

FLOPPY DISC

Designed for use on IBM 3740 or equivalent drive and data entry systems, the FD-3200S conforms to specs of ISO, ECMA, and ANSI and IBM diskette standards. Device incorporates super-fine magnetic material and is capable of high density recording of 3200 bits/in (1259.8/cm). It has a media life of 10M passes/track without error. The 8″ (20.32 cm) disc's memory capability is 243k bytes on seven tracks. **Maxell Corp of America,** 130 W Commercial Ave, Moonachie, NJ 07074.

See at Booth 1697
Circle 460 on Inquiry Card

PAPER TAPE READER/PUNCH

Serial interface compatibility via an RS-232-C is available in the model 1560-S, a combination desktop, self-contained unit with integral electronics, power supply, and asynchronous serial interface. It connects between a terminal device and its modem or data coupler. Punch operates at up to 60 char/s, perforating all commercial tapes. Internal DIP switches allow reader data rates from 50 to 2400 baud. **Sweda International, OEM Products,** 34 Maple Ave, Pine Brook, NJ 07058

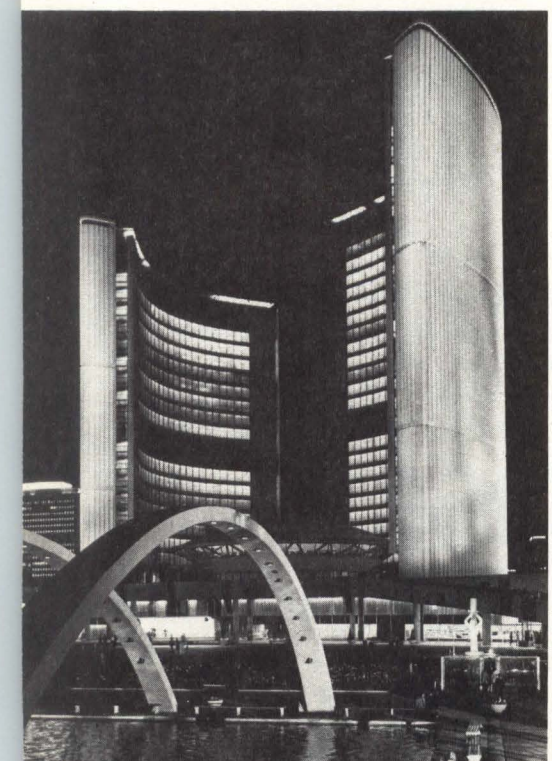
See at Booth 1000
Circle 461 on Inquiry Card

IFIP Congress 77

Toronto, Canada
August 8-12

Gathering computer scientists, managers, and professionals from all over the world, the 7th IFIP Congress 77 is a forum to bring together users and developers of information processing techniques and systems to share their knowledge and experience, while discussing, analyzing, and evaluating the state of computer sciences on the international level. Centering on the theme "The Maturing Profession—Perspectives and Prospects," the Congress will feature a week of presentations on technical state-of-the-art developments in technology, equipment, and applications. Complementing this technical program will be exhibits of the products and services of international companies, as well as the traditional series of special events and entertainment which has become an integral ingredient of these Congresses.

James H. Finch of Canada as Chairman of the Organizing Committee and Prof Wlad M. Turski of Poland as Program Committee Chairman have been instrumental in arranging this year's Congress. The sponsoring organization is the International Federation for Information Processing (IFIP) which is a multinational federation of professional/technical societies concerned with the science and technologies of information processing. Organized in 1960, it currently includes national societies from 35 countries. The principal event in IFIP's program of activities is its Congress, held every three years in a different part of the world.



The technical program, consisting of six parallel sessions to be held in the Sheraton Centre and the Royal York Hotel from Monday afternoon through Friday afternoon, has been devised to cater to specialists in many fields, as well as to those interested in obtaining an overview of developments in all aspects of information processing. Applications of many kinds will be highlighted, with special emphasis placed on computer-aided design, education, and management. A special effort has been made to ensure the relevance of the program to business users of computers, while bringing together the views of computer scientists. The diversified program places greater emphasis on verbal presentations of panels rather than on formal papers. Divided into three types of presentations, the program includes 24 invited speakers, giving keynote and review papers; over 140 contributed papers of original work in information processing; and approximately 35 panels/minisymposia which discuss the progress and practical implications of this work, and the social issues relating to the use of computers. The official Congress language is English.

The program is organized into eight major areas, with many sessions covering fundamentals of hardware and software technology, and computer networking. *Theoretical Foundations of Information Processing* covers the formalization of concepts in program verification, methodology, data bases, and artificial intelligence; mathematical theory; and representation, semantics, optimization, and complexity. *Computer Hardware* highlights parallel processing, microprocessors, special purpose processors, large memories, and the evolution of information processing technology. Means of improving software's technical integrity will be discussed in the *Computer Software* sessions, touching on operating and programming systems, data management, tools, engineering, reliability, and performance.

Computer Networks will be devoted to aspects of the merger between telecommunications and computer technologies, considering distributed processing, packet switching, protocols, and the impact of minicomputers and microprocessors. *Applications in Science and Engineering* presents numerical computation and packages; symbol manipulation, and parallel algorithms, among several other aspects. Case studies provide a means of appraising *Computer Aided Design;* methods, applications, hardware considerations, and economics are ex-

amined, with the importance of management awareness emphasized.

Applications in Management and Administration will attempt to explore changes, applications, cost effectiveness, security, minicomputers, and telecommunications in an effort to help management come to grips with problems brought about by advances in information handling technology. *Information Processing and Education* consists of user, industry, and science needs, and computer education systems.

Special Activities

Opening ceremonies for the IFIP Congress 77 are to be held at 9:15 am Monday morning in the O'Keefe Centre for the Performing Arts. This session will be highlighted by an address by Dr Josef Kates, Chairman of the Science Council of Canada.

The second championship of the world for chess playing computer programs will be held in the Hotel Toronto, with ample room for spectators. The tournament will consist of 12 programs competing in four rounds under the Swiss pairing system. Two rounds will be played on Sunday, and one round each on Monday and Tuesday evenings. Expert commentary will be provided on the game in progress.

The Science Theatre program which will also focus on the theme "The Maturing Profession—Perspective and Prospects" will consist of movies and video tapes grouped into special interest areas, representative of the state of information processing today. Hours will be Monday, 12 noon to 4 pm, and Tuesday through Friday, 10 am to 4 pm.

A social program has also been planned for the enjoyment of attendees. At 6 pm on Sunday in the Royal York Hotel, the Organizing Committee is hosting a welcoming reception to greet arriving delegates. On Monday evening, the Government of Ontario and the Congress Organizing Committee are holding a Wine and Cheese Social at the Ontario Science Centre.

Optional activities offer visitors a view of Canadian celebrations and hospitality. Picnics on Tuesday and Wednesday evenings on Toronto Island will have a Western flavor with a barbeque and square dancing. The cost will be $7 per person. As an alternative, a harbor cruise and dance on the "Trillium" will also take place Tuesday and Wednesday evenings. Price is $4 per person.

The IFIP Congress 77 banquet on Thursday evening will commence with a reception at 6 pm in the Ontario Room of the Royal York Hotel. The banquet will begin at 7 pm in the Canadian Room, followed by a period of entertainment. The cost per person of $25 includes dinner, wines, entertainment, and dancing.

Registration

Registration will take place at the Royal York Hotel, headquarters for the Congress. The fee of $145 includes all Congress materials, admission to technical sessions and Exhibition 77, and a copy of the proceedings which will be distributed at the Congress.

Registration and accommodations are being handled by the IFIP Congress 77, Canadian Information Processing Society, 212 King St W, Suite 214, Toronto, Ontario M5H 1K5, Canada, or in the U.S., by the U.S. Committee for IFIP Congress 77, Registration and Accommodations, 444 Hoes Lane, Piscataway, NJ 08854, tel: (201) 463-6589.

Detailed technical information may be obtained from the U.S. Committee for IFIP Congress 77, Bowery Savings Bank, 110 E 42nd St, New York, NY 10017. Official U.S. travel agent is Garber Travel, Congress and Convention Dept, 1406 Beacon St, Brookline, MA 02146. Tel: 800-225-4570 (outside Mass) or (617) 734-2100, X213/214/215.

Exhibits

A major attraction of the Congress is the 4-day exhibit of computing equipment and services. Many international companies will present products, systems, and services that represent the leading edge of developments and techniques to the international information systems industry. Viewers will see the latest developments in large- and medium-scale CPUs and smaller processors, as well as highly developed systems for business, government, science, and communications. Paralleling the technical sessions, the Exhibition will be held at the Sheraton Centre on Monday from 11 am to 6 pm, and Tuesday through Thursday from 9 am to 6 pm.

Only sessions of particular interest to readers of *Computer Design* are included in the following Technical Program Excerpts. Information is limited to that available at press time.

Technical Program Excerpts

Monday Afternoon

Session 13A 13:30-15:00

Future Directions In Computer Architecture

Chairman: F. Sumner, U.K.

"Beyond Today's Computers," M. V. Wilkes, U.K.

"Direct-Execution Computer Architecture," Y. Chu, U.S.A.

Session 13C 13:30-15:00

Software Studies 1

"On Generation of Test Data and Minimum Cover of Directed Graphs," R. K. Deb, U.S.A.

"An Experiment in Modular Program Design," J. L. Cheval, F. Christian, S. Krakowiak, J. Montue Ilw, J. Messiere, France

"A Debugging Machine: An Approach to an Adaptive Computer," K. Sakamura, H. Kitafusa, Y. Takeyari, H. Aiso, Japan

Session 13D 13:30-15:00

Pattern Recognition and Artificial Intelligence

"A Feature Concentration Method For Character Recognition," K. Komori, T. Kawatani, K. Ishii, Y. Iida, Japan

"Recognition System for Handprinted Characters," K. Iwata,

M. Yoshida, E. Yanamoto, T. Masui, Y. Kabuyama, S. Shimizu, Japan

"The Hierarchical Synthesis of LISP Scanning Programs," A. W. Biermann, D. R. Smith, U.S.A.

Session 14B 15:30-17:30

The Impact of Microcomputers on Computing

Chairman: I. M. Barren, U.K.

Panelists: E. W. Dijkstra, The Netherlands; T. K. Iliffe, U.K.; A. W. Holt, R. L. Petritz, U.S.A.

Session 14D 15:30-17:00

Theories of Programs and Languages

"Automatic Construction of Complete Sample System for Program Testing," J. M. Barzdin, J. J. Bicevskis, A. A. Kalninsh, U.S.S.R.

"Data-Flow-Analysis in Weakly Interpreted Program Schemes," P. Bachmann, German Democratic Republic

"A Theory of Syntactic Monoids for Context-Free Languages," J. F. Perrot, J. Sakarovitch, France

Session 14E 15:30-17:00

New Methods For Information Systems Development

"Utilization of New Information Systems Development Methods in Practice—Perspectives and Prospects," M. Lundeberg, Sweden

"Principles of Computer-Assisted Conception for Automatic Elaboration of a Computerized Information System," J. P. Anton, C. Y. Chrisment, J. B. Crampes, M. F. Debaisieux, J. H. Luguet, France

"A Managerial Decision-Making Tool—Computer Assisted Problem-Solving System (CAPSS)," T. Ishiketa, T. Yokoyama, S. Mandai, N. Takeshima, Japan

Session 14F 15:30-17:00

Finite Elements Methods

"Conforming Finite Element Methods for Shell Problems With Numerical Integration," M. Bernadeu, France

"A Family of Finite Elements With Penalization for the Numerical Solution of Stokes and Navier-Stokes Equation," M. Bercovier, Israel

"On a Graphical Package for Nonlinear Partial Differential Equation Problems," O. Axelsson, U. Navert, Sweden

Tuesday Morning

Session 21B 8:30-10:00

Programming Languages

"An Implementation-Oriented Method for Describing Algorithmic Languages," A. P. Ershov, V. V. Grushetsky, U.S.S.R.

"A Formal Approach to Translator Specification," M. C. Dendien-Gaudel, France

"Optical Code Generation for Expressions Containing Binary and Unary Operators," T. Kameda, H. M. Abdel-Wahab, Canada

Session 21D 8:30-10:00

Distributed Processing

Chairman: E. G. Manning, Canada

"Interprocess Communication in the Pattern Information Processing System," M. Maekawa, Japan

"Distributed Systems—Towards a Formal Approach," G. LeLann, France

"The KUIPNET In-House Computer Network," T. Sakai, T. Hayashi, S. Kitazawa, K. Tabata, T. Kanade, Japan

Session 21E 8:30-10:00

Graphics

"An Interactive Geometrical Design System With Handwriting Input," M. Hosaka, F. Kimura, Japan

"The Intermediate Language for Pictures," T. Hagen, P. J. W. Ten Hagen, P. Klint, H. Neet, The Netherlands

"Multiple Colors and Image Mixing in Graphics Terminals," E. D. Carlson, G. M. Gidding, R. Williams, U.S.A.

Session 21F 8:30-10:00

Numerical Analysis

"Computing the Frequency of a Sampled Sinusoidal Function," G. Frosini, F. Viterbo, Italy

"Inexact Step Lengths and Quasi-Newton Methods," D. F. Shanno, U.S.A.; K-H Phua

"On Bayesian Methods for Seeking the Extremum and Their Application," J. Nockus, U.S.S.R.

Session 22B 10:30-12:00

Computer Aided Instruction

"Trends in Computerized Education Systems," J. Hebenstreit, France

"Introduction of Computer Aided Design in an Educational System," Ph. Masse, J. C. Sabonnadiere, France

Session 22C 10:30-12:00

Impact of Information Systems On Organizations 1

"Impact of Information Systems Organization Thinking," R. I. Tricker, U.K.

"Information Systems and Organization: Empirical Findings Regarding the Introduction of the Computer in Manufacturing Firms," E. Bartezzaghi, C. Ciborra, A. De Maio, P. Maggiolini, P. Romano, Italy

Session 22D 10:30-12:00

Modeling and Analysis of Data Networks

"A Unified Method for the Specification and Verification of Protocols," G. Bochmann, J. Gecsei, Canada

"The Complexity of Computer Network Design Problems," K. M. Chandy, India; L. Van Sickle, U.S.A.

"A Recursive Algorithm for Deadlock Preemption in Computer Networks," D. A. Hutchison, A. Mahmoud, J. S. Riordon, Canada

Session 22E 10:30-12:00

Which Way In Computer Graphics?

Chairman: A. van Dam

Panelists: Evans, U.S.A.; Krammer, Hungary; Guedj, France; Sancha, U.K.

Session 22F 10:30-12:00

Pattern Recognition and Process Control

"The Discriminant Function Approach to Classification of Incomplete Pattern Vectors," J. Kittler, U.K.

"Validation Problems in Pattern Recognition: Study of a Particular Case," M. Borillo, L. Farinas del Cerro, J. Virbel, France

"Problems of Plating-Line Scheduling," V. M. Gluskov, A. I. Nikitin, I. V. Sergienko, U.S.S.R.

Tuesday Afternoon

Session 23A 13:30-15:00

Effects of Information Technology On Organization Structures

Chairman: R. L. Nolan, U.S.A.

Panelists: T. J. Lincoln, R. I. Tricker, U.K.; I. Sitkin, S. Kahn, U.S.A.

Session 23B 13:30-15:00

Trends and Developments In CAD

"Trends and Developments in CAD," J. Hatvany, Hungary

"Focusing on the Internal Model in CAD and CAM Systems," F. M. Lillehagen, J. Oian, J. F. Mack, Norway

Session 23C 13:30-15:00

Technological Aspects of CAI

Chairman: J. Nievergelt, Switzerland

Panelists: D. L. Bitzer, T. Brown, H. L. Morgan, U.S.A.; A. Schmitt, German Federal Republic

Session 23E 13:30-15:00

Software Studies 2

"An Allocation Algorithm for Multi-Microcomputers Using Array Structured Data," Galtier, France

"Software for Speech Output," I. H. Witten, U.K.

"Program Generation and Transformation—Tools for Mathematical Software Development," J. M. Boyle, K. W. Dritz, U.S.A.; O. B. Arushanyan, Y. V. Kuchevskiy, U.S.S.R.

Session 23F 13:30-15:00

Routing and Congestion Control in Switched Data Networks

"Adaptive Routing in Store-and-Forward Networks and the Importance of Load Splitting," W. L. Price, U.K.

"Analysis of Congestion Control in Switched Data Networks," T. W- N. Wong, Hong Kong; M. Unsoy, Canada

"On Alternate Routing in Circuit-Switched Data Networks," H. Rudin, Switzerland

Session 24D 15:30-17:30

Mathematical Theory of Data-Flow Analysis

Chairman: T. D. Ullman, U.S.A.

Panelists: P. Couser, France; K. Kennedy, B. N. Rosen, R. E. Tarjan, U.S.A.

Session 24E 15:30-17:00

Process Control

"Control Under Incomplete Information," N. N. Krasovskii, U.S.S.R.

"Realizations of Two-Dimensional Recursive Filters," M. Clerget, France

Session 24F 15:30-17:00

Techniques In CAD 1

"The Analysis of Cams by Computer-Aided Algebraic and Symbol Manipulation," J. N. Hanson, U.S.A.

"A Computer System for the Synthesis of Reinforced Concrete Frames," A. Golka, Poland

"Using a Conversational Translator Writing System for Generating CAD Systems," G. Courtieux, D. Giubert, France

Wednesday Morning

Session 31B 8:30-10:00

Fault Tolerance

"Fault-Tolerant Computing," A. Avizienis, U.S.A.

"Model For Concurrent Diagnosis in a Microprogrammable System Using a Dynamic Test Scheme," K. Subramanian, India

Session 31C 8:30-9:30

Distributed Data Switching

"Design of Network Access Arrangements," P. Mockapetris, M. Lyle, D. J. Farber, U.S.A.

"MLMA: A Collision-Free Multi-Access Method," E. H. Rothauser, D. Wild, Switzerland

Session 32B 10:30-12:00

Data Networks: Past, Present and Future

"Perspectives On Networks: Past, Present and Future," P. Baran, U.S.A.

"The CYCLADES Experience—Results and Impacts," H. Zimmermann, France

Session 32E 10:30-12:00

Performance Evaluation

"Performance Measurements of the MU5 Primary Instruction Pipeline," N. A. Yannacopoulus, Greece; R. N. Ibbett, U.K.; R. W. Holgate, Australia

"Assessing the Power of an Order Code," S. H. Lavington, A. E. Knowles, U.K.

"A Multi-Class Network Model of a Multiprogramming Time Sharing Computer System," A. Krzesinski, S. Gerber, P. Teunissen, South Africa

Session 32F 10:30-12:00

Computational Algorithms

"Approximation With a Class of Rational Functions," J. A. Van Hulzen, R. P. Hettich, The Netherlands

"Fast Algorithm for Rational Function Integration," D. Y. Y. Yun, U.S.A.

"An Application of a Component by Component Splitting Up Scheme to the Hamilton-Jacobi Equation," S. Maurin, France

Wednesday Afternoon

Session 33A 13:30-15:00

Organizational Productivity: The Role of Information Technology

Chairman: P. Strassman, U.S.A.

Panelists: I. P. Sharp, H. Gellman, Canada; G. Glaser, R. H. Brandon, R. F. Hespos, U.S.A.

Session 33B 13:30-15:00

Packet Networks: Issues, Experiences, Choices

"Datapac: Start-up of a Public Packet-Switched Network," C. I. McGibbon, H. Gibbs, Canada

"Packet Networks: Issues and Choices," L. Pouzin, France

Session 33E 13:30-15:00

Program Translation

"An Approach to Compile-Time Type Checking," P. Henderson, U.K.

"Error Recovery for LR(K) Parsers," G. Poonen, U.S.A.

"Automatic Generation of Optimizing Multipass Compilers," H. Ganzinger, K. Ripken, R. Wilhelm, German Federal Republic

Session 34A 15:30-17:00

Software Reliability

Chairman: D. Gries, U.S.A.

Panelists: E. Dijkstra, The Netherlands; J. Goodenough, S. Gerhart, M. Shooman, U.S.A.

Session 34B 15:30-17:00

Future Potentials In Computer Communication

"The Future Potentials of Packet Switching," L. Roberts, U.S.A.

"Performance of Distributed Multi-Access Computer Communication Systems," L. Kleinrock, U.S.A.

Session 34C 15:30-17:30

Very Large Memories

Chairman: A. S. Hoagland, U.S.A.

Panelists: A. Gibson, U.K.; D. Colton, Canada; J. Harker, G. Kenney, T. Ratchman, U.S.A.

Session 34E 15:30-17:00

System Performance

"Task Scheduling With Critical Section Constraints," D. G. Kafura, U.S.A.

"Customer Classes and Closed Network Models: A Solution Technique," G. Balbo, S. C. Bruell, H. D. Schwetman, U.S.A.

"Priority Scheduling Disciplines in Queueing Network Models of Computer Systems," K. Sevcik, Canada

Thursday Morning

Session 41A 8:30-10:00

Programming Support Systems

"A Support for Program Design With Abstract Machines," E. A. Jordan, France

"Language Design for Modular Software Construction," K. Jackson, U.K.

"Pseudo-Languages and Their Preprocessors," S. Shinozawa, H. Ikeda, A. Nakashima, M. Watanade, Japan

Session 41D 8:30-10:00

Specification and Verification of Communication Protocols

Chairman: C. Sunshine, U.S.A.

Panelists: B. Bochmann, H. Gouda, Canada; S. Crocker, U.S.A.; V. Stenning, U.K.

Session 41E 8:30-10:00

Soft Hardware

"Logical Systems Design Using PLAs and Petri Nets: Programmable Hardwired Systems," K. C. Leung, P. Le Beux, C. Michel, France

"A Multilingual High Level Processor," E. Luque Fadon, L. Moreno Ruiz, J. F. Tirado Fernandez, Spain

"Linear Checking Equations and Error-Correcting Capability for Computation Channels," M. G. Karpovsky, E. A. Trachtenberg, Israel

Session 42A 10:30-12:00

Graphics In Software Engineering

"The Computer 'Scientist' as Toolsmith," F. P. Brooks, U.S.A.

"Making Pointed Queries with a Light Pen," M. E. Senko, U.S.A.

Session 42C 10:30-12:00

Hardware Aids to Software

"Performance of a Parallel Hash Hardware with Key Deletion," T. Ida, E. Goto, Japan

"Putting Supervisory Routines into Hardware," J. L. Bondy, D. N. Freeman, U.S.A.

"Multidimensional Array Accessing in the MU5 Computer," G. Thomas, U.K., A. Necula, Romania

Thursday Afternoon

Session 43A 13:30-15:00

Electronic Mail 1: Design

Chairman: R. Taylor, U.S.A.

Panelists: J. C. R. Licklider, T. Meyer, J. Vallee, U.S.A.; D. Yates, U.K.

Session 43B 13:30-15:00

CAD: Perspectives and Prospects

"Means and Levels of Knowledge Representation in the CAD System GERMINAL," J. Foisseau, R. Jacquart, F. R. Valette, France

"On Being Creative in CAD," N. Negroponte, U.S.A.

Session 43D 13:30-15:00

Logic and Proofs For Programs

"Intermittent Assertion Proofs in LUCID," E. A. Ashcroft, Canada

"Program Proving: Expression Languages," P. Pritchard, Australia

"A Constructive Programming Logic," R. L. Constable, U.S.A.

Session 43F 13:30-15:00

System Programming

"A Microprogram Generating System: MPG," T. Baba, Japan

"Parallelism in Loop-Free Microprograms, S. Dasgupta, Canada

"On the Efficiency of Some List Marking Algorithms," J. L. Baer, M. Fries, U.S.A.

Session 44A 15:30-17:00

Electronic Mail 2—User Needs

Chairman: G. Edwards, Canada

Panelists: K. Samuelson, Sweden; J. Carlisle, R. Panko, R. Uhlig, U.S.A.

Session 44C 15:30-17:00

Automated Design in Electronics

"Automation of Electronic and Microelectronic Design," M. A. Gavrilov, U.S.S.R.

"NOPAL: Automated Design and Programming of Testing," N. S. Prywes, Y. Chang, C. Tinaztepe, U.S.A.

Friday Morning

Session 51A 8:30-10:00

Operating Systems

"Machine-Independent Operating Systems; Portable Operating Systems," D. Morris, U.K.

"Managers Versus Monitors," A. Jannel, H. Stiegler, German Federal Republic

Session 51D 8:30-10:00

Complexity Theory

"A Nonlinear Lower Bound for the Formula Complexity of Certain Boolean Functions," G. Wechsung, German Democratic Republic

"Natural Complexity Measures and a Subrecursive Speed-Up Theorem," D. A. Alton, U.S.A.

"Probabilistic Machines Can Use Less Running Time," R. Freivalds, U.S.S.R.

Session 51E 8:30-10:00

Parallel Architectures

"A Multimicroprocessor: CYBA," E. L. Dagless, U.K.

"A Computer Capable of Exchanging Processors for Time," M. Arvind, Italy; K. P. Gostelow, U.S.A.

"Hardware Organization of a Low Level Parallel Processor," S. Tomita, K. Shibayama, S. Oyanagi, H. Hagiwara, Japan

Session 52A 10:30-12:00

Programming Methodology

Chairman: W. M. Turski, Poland

"Using Precise Specifications in the Development of Software," D. Parnas, German Federal Republic

"The Narrowing Gap Between Language Systems and Operating Systems," A. K. Jones, U.S.A.

Session 52E 10:30-12:00

Techniques in CAD 2

"How To Design Variants of Flats Using Programming Language PROLOG based on Mathematical Logic," Z. Markusz, Hungary

"Algorithmic Macro Design System for Shift Registers," H. G. Marchand, France

"LSI by CAD out of DAISY," D. B. Jarvis, U.K.

Friday Afternoon

Session 53B 13:30-15:00

New Approaches to Systems Integrity

"System Quality Through Development Audit," D. J. Lewis, U.K.

"A New Approach for Risk Analysis and Control—The U.K. Experience," K. K. Wong, U.K.

"ACL: A Conversational Language for Audit Intelligence," H. J. Will, H. Brussel, Canada

Session 53C 13:30-15:00

Numerical Methods In Mathematical Physics and In Control Theory

"Numerical Methods for Variational Inequalities: Applications in Physics and in Control Theory," J. L. Lions, France

"Computational Aspects for a Control Problem," C. L. Simionescu, Romania

Session 53E 13:30-15:00

Design Automation For LSI—Practical or Painful?

Chairman: W. Rosenbluth, U.S.A.

Panelists: J. Manchon, France; E. Kozenchak, B. Gogos, W. Shorter, U.S.A.; D. B. Jarvis, U.K.

Session 54C 15:30-17:00

Programming Systems

"SIGMA 76," J. Reinfelds, Australia; C. E. Vandoni, Switzerland

"Single-Language Small Processor Systems," R. G. Hamlet, U.S.A.

"PL4: A Low Level Language With Class," J. Vaucher, N. Rochon, Canada

Session 54D 15:30-17:00

Concepts In Parallel Programs

"Towards Autonomous Descriptions of Synchronization Modules," P. Robert, Canada; J. P. Verjus, France

"Laws for Communicating Parallel Processes," C. Hewitt, H. Baker, U.S.A.

"Coroutines and Networks of Parallel Processes," G. Kahn, France; D. MacQueen, U.K.

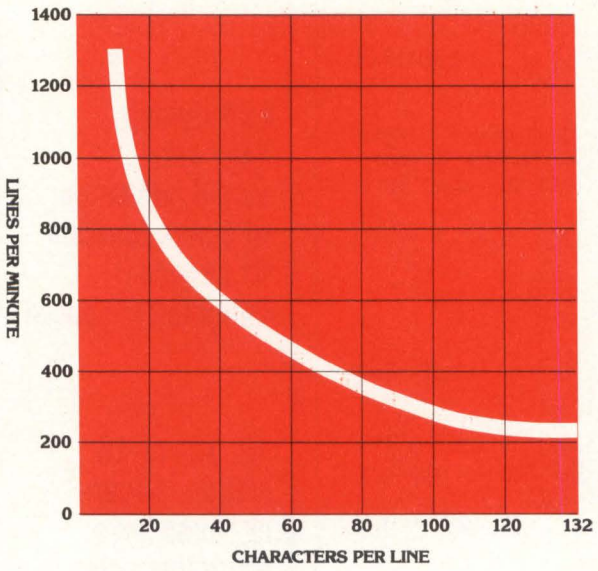
Session 54E 15:30-17:00

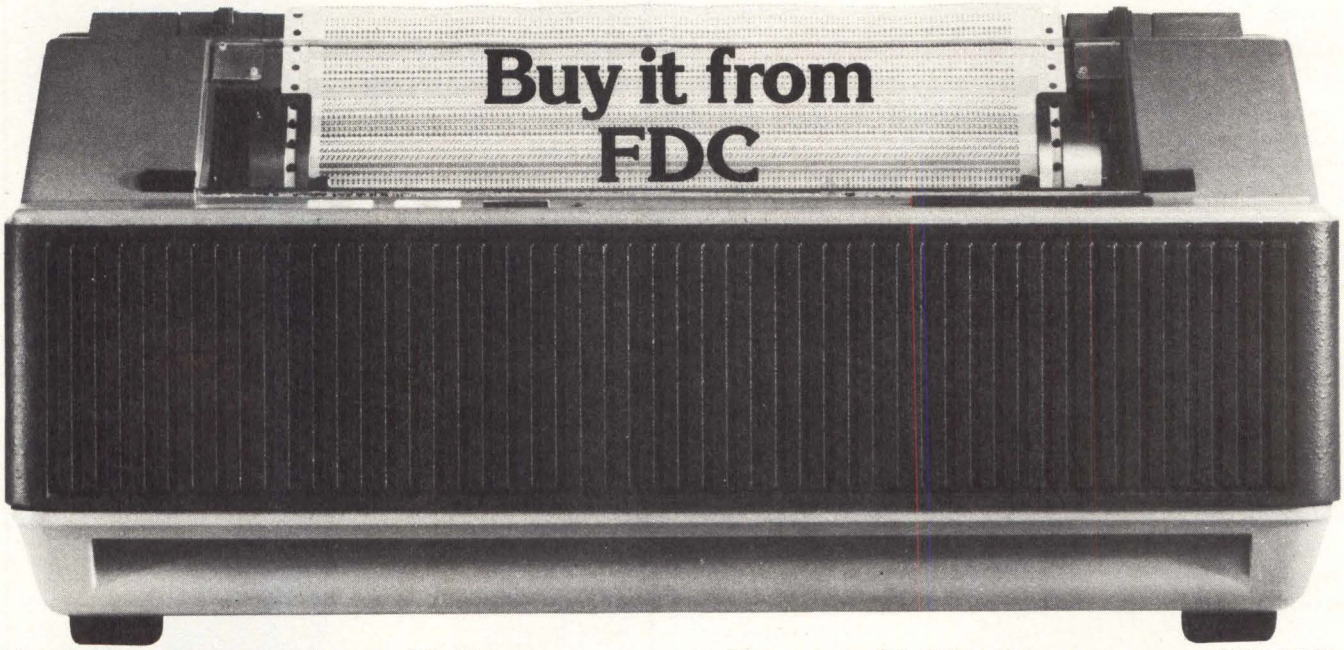
Economics, Organizational, and Social Implications of CAD

Chairman: A. I. Llewelyn, U.K.

Panelists: J. J. Allan III, U.S.A.; F. Lillehagen, Norway; C. de Vannsay, France; V. Stams, German Federal Republic □

Line printer speed at serial printer prices





Florida Data Corporation's new PB-600 gives you line printer speed at serial printer prices. It's rated at 600 characters per second. And, as the graph indicates, that translates into line outputs from 240 to well over 1200 lines per minute, depending on line length.

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FDC

Specific operating and architectural requirements for workable multiple microprocessor systems result from a detailed analysis of current LSI microprocessor organizations

Analysis of Multiple-Microprocessor System Architectures

Alan J. Weissberger

Signetics Corporation
Sunnyvale, California

Current low cost large-scale integrated microprocessors offer the potential of cost-effective multiple microprocessor systems. Advantages that can be gained by these systems include high throughput, improved real-time response, better availability/reliability, and modular expansion. Unfortunately, the design techniques, structures, and organizations of multiprocessor systems are not well defined. A host of problems, including process partitioning into parallel tasks, allocating tasks, sequencing and interaction between processors, controlling system resources, and overcoming the physical and architectural limits of microprocessors must be thoroughly researched before implementation progress can be made.

To provide solutions and design guidelines for multiprocessor and distributed processor systems incorporating available large-scale integrated (LSI) microprocessors, existing microprocessor architectures, organizations, and strategies have been analyzed to derive those characteristics deemed mandatory for workable multiple microprocessor systems. Based on the analyses, recommendations are made on specific architectures, interconnection structures, desirable features, and special LSI control chips.

LSI Microprocessors

Microprocessors are now available in a wide spectrum of performance classifications. Calculator oriented processors, dedicated controllers, general-purpose and high performance units, microcomputer boards, bipolar bit slices, and sequencers have emerged to potentially fulfill the requirements of many control and real-time processing applications. Characteristics of some available units are listed in the Table. These various microprocessor organizations have been analyzed to enumerate the problems of parallelism. This provides a means of defining favorable properties for implementing a sound microprocessor system.

Organization Definitions

There is great divergence in the acceptable meanings of terms describing parallel processor/multiple processor systems. The following definitions are presented to alleviate this ambiguity. *Parallel processing* is the concurrent* processing of two or more portions of the same system algorithm by two or more processing units. This can occur at the task, subtask, instruction stream, or data set level. The result is a *multiple processor system.*

Two organizations of multiple processors are analyzed; these are the single instruction multiple data (SIMD) and the multiple instruction multiple data (MIMD) organizations.

SIMD Architecture

In SIMD architectures (sometimes called parallel processor systems), a single control unit fetches and decodes instructions. The instruction is executed in the control unit itself (eg, jump, conditional branch) or is broad-

*Concurrent refers to the same interval of time; simultaneous refers to the same instant of time.

LSI Processor Classification

Manufacturer	Model Number	Characteristics
Calculator Oriented Processors		
National Semiconductor	5781, 82, 99, 140	Lowest cost controller with ROM, RAM, I/O, clock, and CPU on chip. Primitive instruction set and addressing modes. Used in appliance controls, radio tuners, scales, simple instruments, and cash registers
Rockwell	MM76, MM77	
Texas Instruments	TMS 1000, 1100, 1200	
General Instrument	PIC 1650	
Dedicated Function Controllers		
Intel	8048, 8041	Control-oriented architecture with limited processing capabilities. Several I/O ports and timer on chip. Instruction set includes BCD operations, table lookup, and conditional branch capability. Used in equipment controllers, gas pumps, telephone dialers, and point of sale terminals
Mostek	3870	
Fairchild	F8/1, 2	
National Semiconductor	SC/MP I, II	
Texas Instruments	9940	
General-Purpose Units		
Intel	8080	Intermediate processing power, fair to good instruction set and addressing modes, flexible, special-function I/O chips. Greatest range of applicability—smart instruments, smart terminals, process control, measurement and test, data collection, peripheral control, communication control, and games
Motorola	6800	
Signetics	2650	
MOS Technology	6502	
Rockwell	PPS-8	
Texas Instruments	9980	
RCA	1802	
Intersil	6100	
National Semiconductor	PACE	
General Instruments	1600	
High Performance Units		
Zilog	Z80	Minicomputer-like instruction set, register configuration and addressing modes, clock, bus control, multiple interrupt circuitry on chip. Higher speed operation. Programmable and combination function support chips. Used in applications requiring high speed and performance
Intel	8085	
Texas Instruments	TMS, SBP9900	
Microcomputer Cards		
Digital Equipment	LSI-11	Complete computer with clock, CPU, memory, I/O, and interrupt circuitry on one PC card. Good performance. Easy to design with. Some cards offer extended arithmetic functions; others offer flexible I/O through programmable LSI I/O chips. Special function cards for memory and I/O expand system capabilities. General-purpose minicomputer applicability
Data General	μNOVA	
Intel	SBC 80/10, 20	
Zilog	Z80 MCB	
Mostek	SDB, OEM 80	
Motorola	Monoboard	

Bipolar LSI Processor Elements

	Bit Slice	Sequencer	
Intel	3002	3001	Bit slice is a segment of an ALU + register file. Control sequencer is for microinstruction next address function. Latches, buffers, transceivers, and carry look-ahead logic are required to complete a microprogrammed CPU. Highest speed and throughput, most flexible, but large component count and difficult to develop and test system. Used for minicomputer construction, special-purpose computers, disc controllers, and communication frontends
American Micro Devices	2901	2909, 2911	
Motorola	10800	10801	
Fairchild	9405	9408	
Signetics		8X02	

cast to other processing elements. The SIMD computer is shown in Fig 1. Three subclasses of SIMD are

Array Processors—where instructions manipulate vectors of data simultaneously and the control unit has limited capability (eg, ILLIAC IV)

Processing Ensembles—where the control unit is a full-fledged computer and processing elements communicate by passing messages through it (eg, PEPE)

Associative Processors—which access and operate on data by its content rather than address (eg, STARAN)

Of the three organizations, the array processor (sometimes called vector processor) is the only one that appears to be cost-effective, and then only for very specific applications. This configuration is shown in Fig 2. Rationale for this organization is the tremendous throughput obtained by simultaneous (parallel) operation of processors on different data streams. To obtain this parallelism, the array processor system must have three specific characteristics. Computations must be describable by vector instructions with many identical operations in

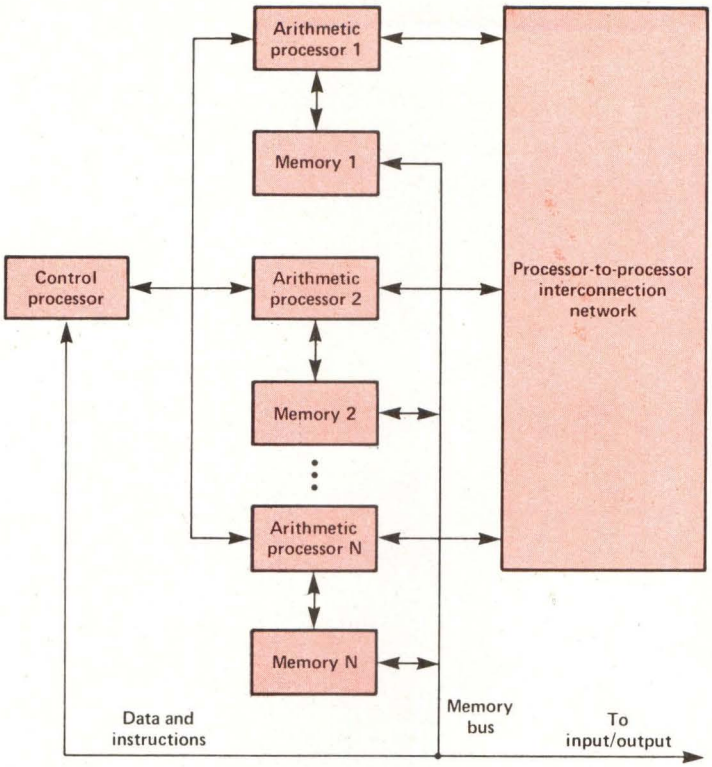


Fig 1 Block diagram of an SIMD computer. Each of N independent arithmetic processors has own private memory. These memories are connected to a high speed data bus whose bandwidth is compatible with both processors and I/O devices capable of DMA. This permits data sharing between individual processors and DMA devices

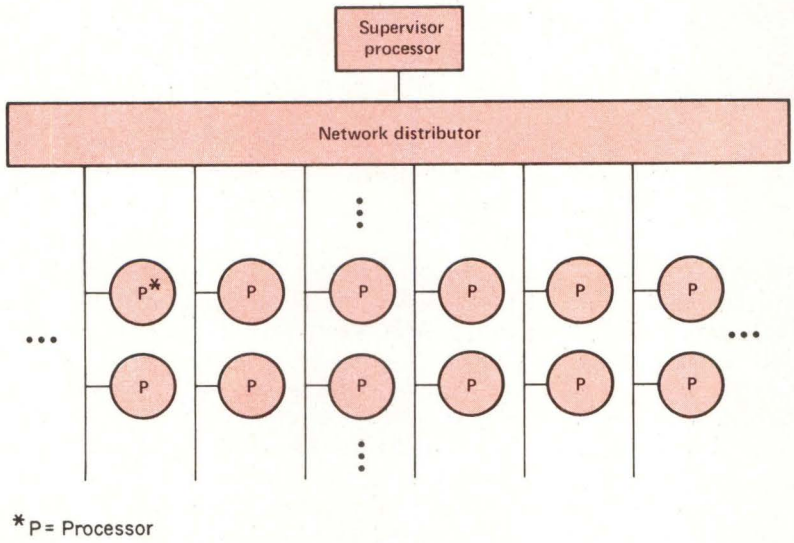


Fig 2 Block diagram of an array processor. The array processor is a specific implementation of an SIMD computer. Simultaneous operation of processors on different data streams provides very high system throughput

action simultaneously on different data; high speed data routing between processors is necessary; and operands that are manipulated simultaneously must be fetched simultaneously. If any condition is not satisfied, the computation may run serially, thereby idling processors and negating the throughput advantage of parallel execution.

Examples of this type of computation are the solution of systems of partial differential equations, linear equations, matrix multiplication, or grid problems. Applications may be in weather prediction, air traffic control, radar signal processing, or any high speed vector computation.

Bipolar bit-slice microprocessors would necessarily be used as processing elements in an LSI array processor. Bit slices achieve lower cost per function than medium-scale integrated (MSI) circuits, permit application-dependent configurations and feature built-in fault tolerance. These advantages accrue from custom tailoring the slices to the application. Techniques for attaining high performance with bit slices include fast technology (eg,

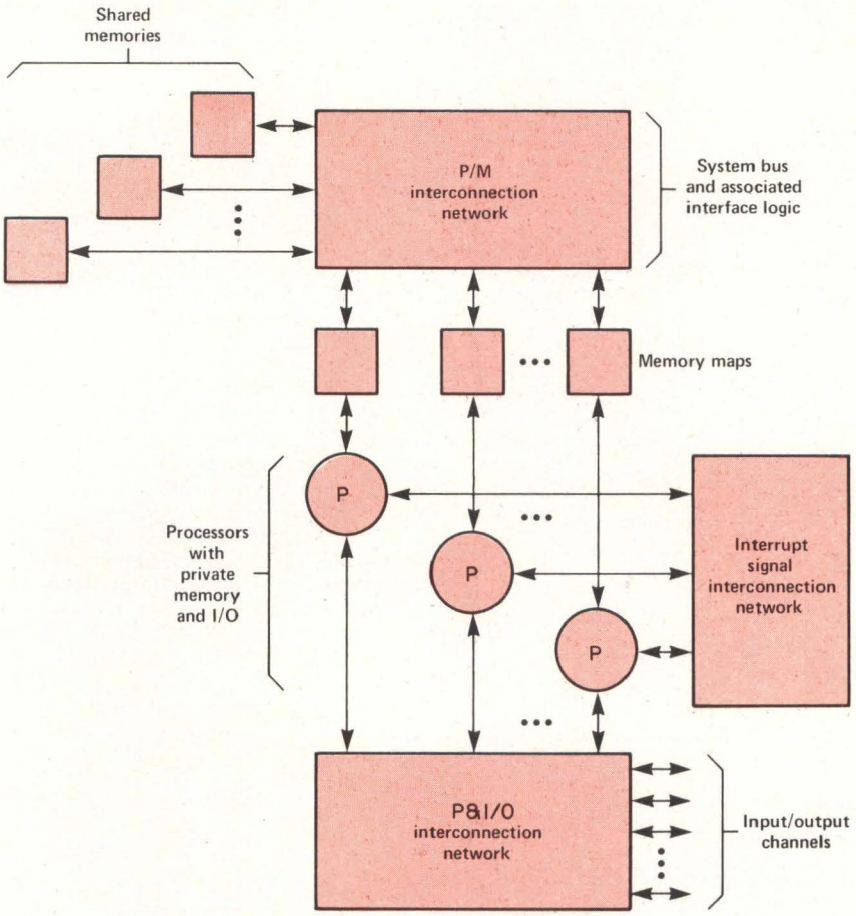


Fig 3 Block diagram of an MIMD computer. Flexibility inherent in an MIMD computer necessitates extensive interconnections between processors, shared memories, and I/O channels. To maintain high efficiency in this environment, computations on different processors must be properly synchronized and tasks must be carefully allocated

Motorola M10800 ECL), horizontal microinstructions, prefetch microinstructions (pipelining), overlapped microinstruction execution (2-stage pipeline), carry lookahead logic, external hardware for multiply/divide and multibit shifts, microlevel interrupt capability, different microcycle times for different microinstructions, and pipelining at the macroinstruction level in the central control unit.

MIMD Architecture

Architecture of the MIMD is not meant for vector or iterative computations. This organization (Fig 3) achieves parallelism by performing independent tasks on separate data sets concurrently, and combining results of the execution of the independent tasks. To attain high efficiency in this environment, proper synchronization of processors and allocation of tasks is necessary to balance the processing load. This contrasts sharply to SIMD organization, where synchronization is done automatically when each instruction is executed, and there is no task allocation problem because all processors perform the same tasks (but on different data). The two subcategories of MIMD are the distributed system and the multiprocessor system.

Distributed System—In this system multiple processors perform dedicated functions as part of a single partitioned system. Processors can be locally distributed (eg, factory) or geographically distributed (eg, communication network). Tasks and their actions must be completely known in advance so that the system functions can be subdivided among the individual processing elements. This includes segmentation of software into dedicated program segments for each processor and assignment of controlled variables and devices to each processor. Such static allocation of tasks minimizes program interaction, which permits simplified development and debugging of individual program segments.

Interprocessor communication is usually restricted to passing messages or data blocks through shared peripherals or serial communication links as opposed to a shared main memory. When secondary storage (such as disc or tape) is used to pass messages, the system is called a multicomputer.

Distributed systems have three serious disadvantages. System load characteristics are rarely known explicitly. This can result in inefficient utilization of processors and awkward segmentation of system software. System expansion through the addition of controlled variables, tasks, or processors may require extensive offline sys-

tem reconfiguration. Failure of any processing module (PM)* may seriously degrade system performance, as the system can not dynamically shift tasks that have been assigned to the defective PM.

Process control, numerical control, factory automation, HP Instrument Bus (IEEE 488) instrumention, and data communications are examples of distributed function microprocessor architectures. No special microprocessor features are required other than a link for interprocessor communications.

Multiprocessor System—A system in this category employs a single integrated operating system to dynamically allocate tasks as they are received. The operating system can run on each PM (floating executive), or a resource allocation processor (master) can allocate tasks to PMs (slaves) through a resource request table.[1] PMs may be identical and capable of executing any task (symmetric) or may be preassigned to handle special functions (asymmetric).

The symmetric multiprocessor is used in a general-purpose environment where processing requirements are constantly changing. Since PMs are equivalent, a given task can be assigned to any idle PM and tasks can be reassigned in the event of PM failure. By contrast, the asymmetric multiprocessor is composed of PMs specially configured for a set number of tasks. Incoming tasks must be queued to assigned PMs even though other PMs may be idle. Although this may decrease throughput, it greatly simplifies the operating system, which becomes a task scheduler and is relieved from the identification and disbursement of parallel tasks. As a system becomes more asymmetric, more tasks must be allocated to specific PMs and portions of the operating system become more individualistic. Under these conditions, a multiprocessor system moves toward a distributed system.

Coupling

Multiprocessor systems (MPS) are further classified according to the degree of interaction between PMs (often called coupling). Two such classifications are tightly coupled processors and loosely coupled processors.

Tightly coupled processors operate under the jurisdiction of a strict control scheme, generally implemented in a self-contained hardware unit. Examples include the CDC 6600, CDC 7600, IBM 360/91, CDC STAR-100, and Texas Instruments ASC. This trend is only evident in "super computers" whose viability is questionable. However, Bowra[2] has proposed a multiple function unit processor with MSI and LSI building blocks. (It should be noted that processors passing data through shared memory are sometimes considered to be tightly coupled, although this author disagrees with that classification.)

There is no program interaction between loosely coupled processors, although they may share read/write memory to pass information. When the system is to consist of numerous small modules for general-purpose applications, the connections are necessarily of the loose type.[3] In this case, the processors should be able to access memory with as much concurrency (sharing) as possible, communicate with one another through shared resources with minimum contention problems, and be capable of dynamic reconfiguration in the event of PM failure.

Selection of Architecture

The loosely coupled MPS is the microprocessor system architecture for general-purpose applications requiring high throughput and/or high availability. This author predicts that these systems will eventually replace many minicomputers and mainframes in data base inquiry/response and in real-time control applications. This prediction is corroborated by reasoning that (1) inherent flexibility permits small increments of growth with minimum system redesign (sometimes called extensibility); (2) ability to dynamically allocate tasks to balance the processing load improves throughput and real-time response; (3) ability to dynamically reconfigure PMs in the event of failure provides fault-tolerant operation if extra PMs are available, or graceful degradation by reassigning the most important tasks to working PMs; LSI is cost-effective, particularly the low incremental cost/performance achieved when adding an LSI PM; and an MPS can overcome the ultimate physical limits of LSI for high performance applications. One or more of these items will be chosen as design goals for the microprocessor-based MPS (μMPS).

Examples of μMPS consist of data base management for online interactive systems (air reservations, credit authorization, banking, inventory control, and hospital patient recordkeeping), or in real-time applications such as industrial control, data communication, speech recognition, and hospital patient bedside monitoring. Any system where processes can be partitioned into small individual tasks is a candidate for μMPS implementation.

Design Consideration for µMPS

Functional design of μMPS must consider at least six important variables: allocation of tasks, control of system resources, characteristics of PMs, interconnection structure, interaction between PMs, and failure recovery. The approach taken for each variable has a pronounced effect on system performance, cost, reliability, and flexibility.

Allocation and Synchronization

Allocation of tasks and synchronization of microprocessors are the most serious problems in the design of a multiple microprocessor operating system. They involve identification of a parallel process, partitioning the process into subprocesses or tasks, establishing a priority scheme for the tasks, assigning or scheduling the tasks among various microprocessors, synchronizing microprocessors so that the process can be carried out correctly, and providing a means to dynamically reassign a task in the event of PM failure (graceful degradation).

Although solutions to these problems have been proposed,[4,5,6,7] none has been implemented successfully. Three non-mutually exclusive approaches to attainment of a concurrent operating system have been suggested: (1) design algorithms that take advantage of the parallel architecture; (2) expressing potential parallelism in the coding via FORK-JOIN or WAIT-SIGNAL[5]; and (3) detect-

*In this context, a PM is a microprocessor-based central processing unit or input/output channel.

ing parallelism during compilation, primarily at the instruction level.[8,9]

For a small number of microprocessors, about two to four, the process partitioning/synchronization problem is not as overwhelming as it is with 16 or more processors. Processes are seldom so complex that there are 16 distinct subprocesses all being executed concurrently. An exception might be an online interactive system where simultaneous users create similar demands on system resources. Each such demand can be thought of as a task.

Control of System Resources

Processes or tasks operating in a μMPS share a pool of resources to improve performance. Resources include hardware (processors, memory, I/O channels, registers, buses, bulk storage) and software (programs, data files, buffers, queues, variables). The more shared resources that are available, the greater the control that is required for allocation and resolution of access conflicts (contention). Too much sharing results in complex control structures and increased contention. This can produce low throughput or deadlock, a situation in which two or more tasks are waiting for resources that have already been assigned to each other. When this occurs, the wait state must be broken by external control and the deadlocked tasks reinitiated. Arbitration, flag test-and-set, and interrupts are the most common methods of hardware resource control.

Arbiters—An arbiter accepts requests from PMs (active elements), resolves contention, and alerts the elements of its decision. A centralized arbiter consists of a single self-contained hardware unit. Intel has designed a custom "bus controller" chip for this function on the SBC 80/20 microcomputer board,[10] Widdows has developed an "IBUS arbiter" for the MINERVA system,[11] and Reyling has proposed a resource allocation microprocessor.[1]

A decentralized arbiter is one in which control logic is distributed throughout the active elements connected to a shared resource. This necessarily complicates each PM, but improves system integrity in the event of failure.

Both schemes use the same methods for arbitration. These include daisy chaining, priority encoding, and polling asynchronous requests (flags and interrupts). Choice of method depends on simplicity, device servicing requirements, expandability, susceptibility to failure, control line limitations, interconnect cabling, and controller speed.[12] Arbiter speed should be such that the overhead to access a device is only a fraction of the time spent using that device. For example, a high speed cycle-shared memory requires a hardware arbiter, while a block of shared memory can be allocated by a microprocessor arbiter.

Status Flags—Conflicts over shared memory and input/output (I/O) can be resolved via the flag test-and-set (TAS) procedure. The requesting processor tests the status of the flag, which is simply a resource busy indicator. If busy, the microprocessor must wait before obtaining the resource. If not busy, the flag is set to busy during resource access and then reset when the microprocessor is finished with the resource.

Simultaneous requests for a resource must result in only one processor gaining access. Since requests for a shared resource occur asynchronously, care must be taken that more than one processor does not gain control of the resource. For this reason, the TAS operation must be indivisible.

If memory is used for the status flag, it must be capable of a read-modify-write cycle before permitting further accesses. This requires a lock on the memory address. Although it is easier to lock a block of memory (memory module) than a specific address,[12] in that case the remainder of the module is unavailable to other processors. For this reason, status bits are sometimes implemented as a set of dedicated external registers that perform the read-modify-write cycle themselves.

Assume that each status flag within an external status flag register is individually addressable. When the addressed flag is read by an interrogating processor, that flag immediately sets itself to busy. If the flag indicates resource busy, the processor must wait before accessing the resource, and setting the flag has done no harm; if the flag indicates resource not busy, access is permitted and further requests are denied until the flag is reset. A dual-rank register is required for this implementation and some priority scheme is needed to control access to the register. However, no hardware lock is required, memory is not disturbed, and only one bus cycle is necessary to determine resource access.

Interrupts—Interrupts can be used to service internal processor errors (parity, invalid op code, address out of range), clock signals (interval time-out, real-time clock), external devices (character ready, channel transfer complete, device acknowledge), or to synchronize interprocessor communications (shared memory mailboxes, reassignment of tasks or devices). There are several methods used to service interrupts in μMPSs.

Service of the first two classes is usually assigned to the originating microprocessor. External devices may be preassigned to individual processors or dynamically directed to whatever processor is best equipped for service. This real-time assignment can be done through a centralized hardware arbiter (an interrupt switch), a dedicated high speed processor, or by individual microprocessors. Assignment is made on the basis of servicing capability, availability, task allocations, and software priorities of each processor. Interprocessor communications (discussed later) can be synchronized by passing an interrupt request signal from one processor to another, such that requests for each can be wire-ORed onto one interrupt level dedicated to interprocessor communications. A prioritized vector, corresponding to the highest priority processor requesting the bus, can be placed on the data bus when the interrupt has been acknowledged.

Handling external device interrupts is perhaps the most critical decision in implementing the device interface to the μMPS. Dedicated assignment is the most straightforward, but limits flexibility and prohibits graceful degradation. LSI interrupt controller chips (eg, Intel 8214, 8259) can provide fixed priorities, rotating priorities (based on last occurrence), polling, and masking. Alternatively, MSI or small-scale integrated (SSI) based interrupt controllers can be constructed. Some microprocessors (Zilog Z80, Rockwell PPS-8) have a built-in serial interrupt priority mechanism (daisy chaining).

If a centralized switch is used, the interrupt must be quickly directed to the appropriate microprocessor;

otherwise service may not occur in time. This is particularly true if the switch is heavily loaded with interrupt requests. Interrupt assignment by individual processors can be done with external hardware to store information about the state of an interrupt.[11] For example, if a processor receives an interrupt of type A, it can assign the next type A interrupt to the best available processor. This method is less effective than the centralized design because scheduling of interrupts is made well in advance of actual occurrence. However, the method works well if interrupts are periodic and occur with known frequency. High processor speed is not required for interrupt assignments because scheduling is distributed among all processors. Graceful degradation is possible through interrupt reassignment in the event of failure.

Characteristics of PMs

Composition of PMs depends to a large extent on system bus structure (interconnection topology), interprocessor communications, and the number and type of shared resources. In general, the PM includes a central processor unit (microprocessor chip plus clock, bus control, and buffers as required), local or private memory for instructions and data storage, system bus interface circuitry, memory map hardware, interrupt handling logic, and I/O device controllers for private I/O. It is also possible for each PM to have a portion of its memory that can be shared with other PMs.[13] If instruction memory is shared, a cache containing frequently executed instructions is useful.[14] In cases where system bus width is significantly greater than microprocessor word length, an instruction stack[11] can be used to lighten system bus loading.

One critical area of the PM is the system bus interface logic. Flexibility and performance of the interconnection topology (subsequently examined) are directly proportional to the complexity and expense of this interface logic. If heterogeneous microprocessors are used in PMs, interface logic will be unique for each unique processor. In particular, 8- and 16-bit processors may communicate over the same bus, requiring distinct interfaces for each microprocessor.

Memory map hardware is used to translate addresses provided by the microprocessor into addresses in physical memory (both private and shared). In a parallel computation environment, precise memory requirements for a group of concurrently executing programs can not be predicted ahead of time. As a result, programs and data must be moved and/or compacted to make room for additional items. The memory map facilitates dynamic variation of physical locations during program execution without actually moving the locations. If data are to be moved, the map function is changed to reflect a new physical address assignment. The memory map also provides a convenient means for two or more programs to share data. References to shared data are mapped onto the same physical addresses, while references to private data are mapped into distinct locations for each PM.

It is sometimes possible to use software to achieve the memory map function. To do this, extensive use is made of indirect addressing through indirect pointers in microprocessor registers or in read/write memory, and indexed addressing. Presently, only the Zilog Z80 and the Signetics 2650 have the addressing modes and the required number of internal registers to make software mapping feasible.

Interconnection of Functional Modules

Three organizations for interconnection of PMs, shared memory, and shared I/O are the time-shared common bus, multibus/multiport memory, and crossbar switch.[15] Chosen structure is called the system bus.

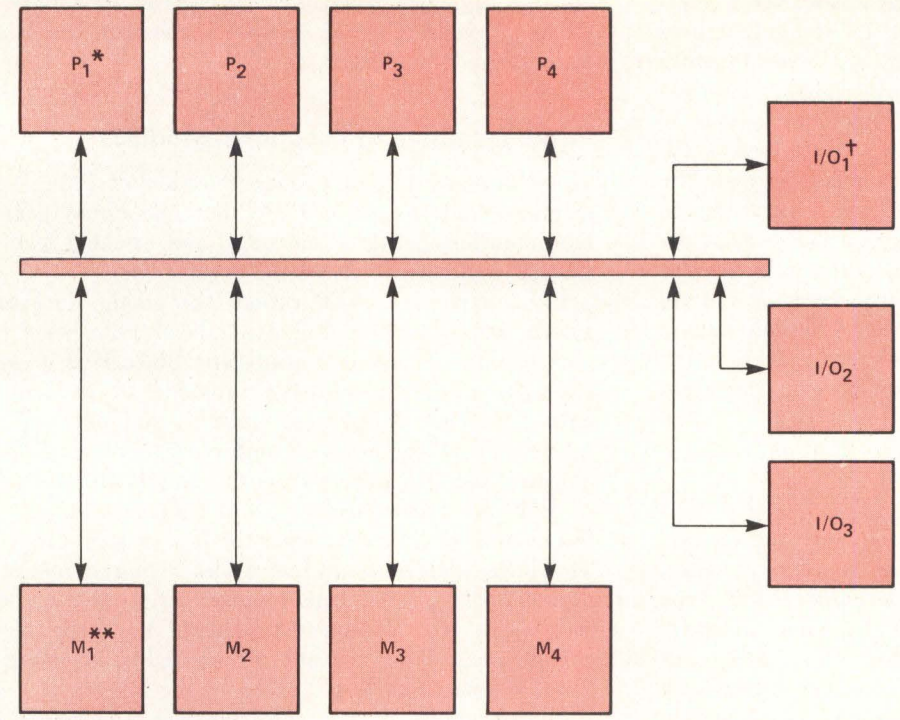
Least expensive organization, the single time-shared system bus, shown in Fig 4(a), is also the least complex and the easiest to reconfigure. Since it is a shared resource, a means must be provided to resolve contention (fixed priorities, first-in first-out (FIFO) queues, daisy chaining). Interference between PMs requesting the bus depends on the length and frequency of PM bus cycles, memory and I/O cycle times, and the number of PMs that share the bus (system capacity). The lower the ratio of bus cycles required by an individual PM to the total number of cycles available, the higher the system throughput. For this reason, private memory and private I/O are highly advantageous. Total system capacity is limited by the bus transfer rate.

Disadvantages of this bus structure are that system expansion (additional PMs) increases contention which degrades throughput and increases arbitration logic; lower priority PMs on the bus may never gain control; and, worst of all, failure of the bus is catastrophic for the system.

Multiported systems, as depicted in Fig 4(b), employ multiple dedicated buses that are connected between PMs, shared memory, and shared I/O. Each of the latter two (passive) elements is said to have multiple ports, one for each connection to a PM. Although this arrangement provides excellent throughput, contention logic must be built into each passive element to acknowledge or hold PMs competing for the resource (alternatively, TAS status flags can be used). Major disadvantages are the high cabling and connector costs that accrue from multiple connections, and the limits placed on size and number of configuration options by the restricted number of ports. For this reason, the maximum system configuration must be clearly defined prior to fabrication.

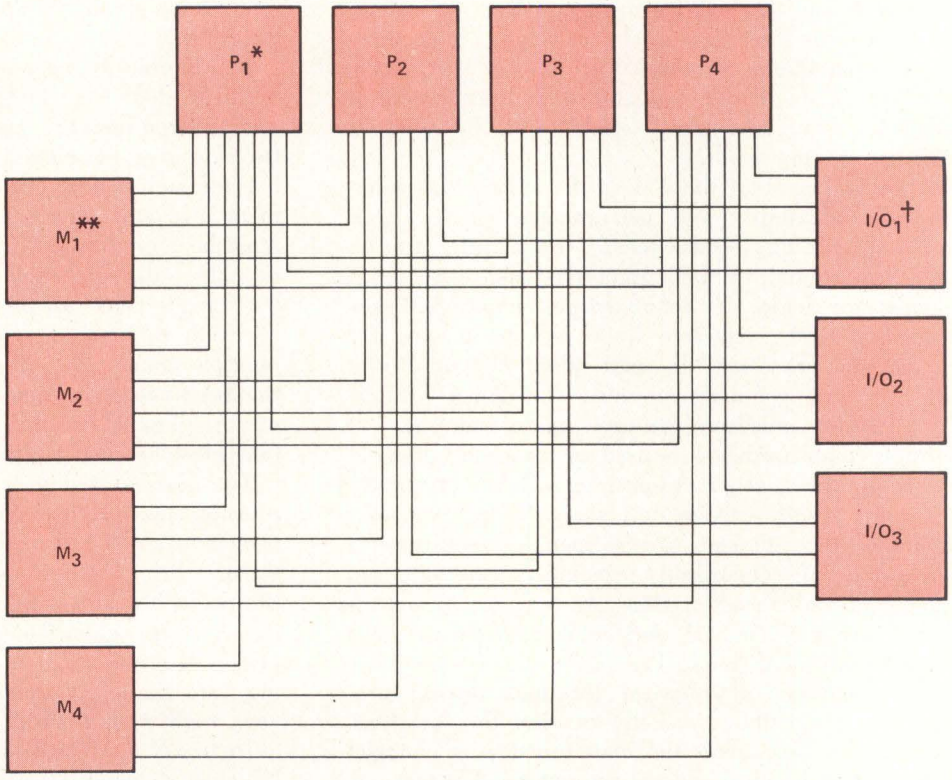
The crossbar switch is sometimes referred to as space division multiplexing. Any passive element can be connected to any PM for the complete duration of a data transfer through the crossbar matrix. System size is not limited by access capabilities of the functional units, since they are all connected by a single crosspoint [see Fig 5(a)]. Multiple simultaneous connections are possible if they are mutually exclusive. This scheme can produce very high system throughput.

In the N x M crossbar switch [Fig 5(b)], there are N active elements (P and I/O) and M passive memory elements (M). Three simultaneous connections are denoted by X in the diagram. Functional units in such a system need minimal bus interface logic since they perform neither conflict resolution nor recognition of which data are directed toward them. These functions are done by the switch matrix which is necessarily complex, costly to control, and physically large. Note that one line in the crossbar consists of address, data, and control bus signals, corresponding to 32 to 64 wires in a real



* P= Processor
** M= Memory
† I/O= Input/Output

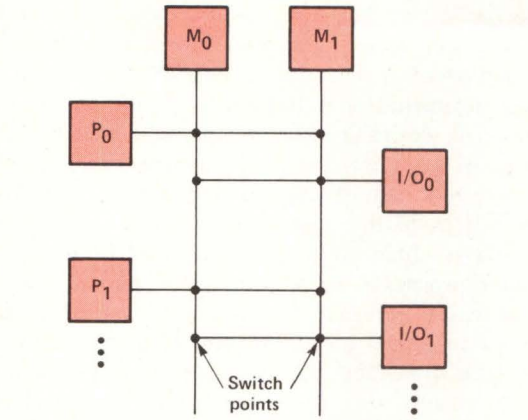
(a)



* P= Processor
** M= Memory
† I/O= Input/Output

(b)

Fig 4 Functional module interconnection. Single time-shared bus (a) is simplest means of interconnecting processors, memories, and I/O channels. Being a shared resource, a means must be provided to resolve bus contention. Multiported system bus configuration (b) is characterized by permanent connections between each system element. This permits simultaneous bus operation for each processor



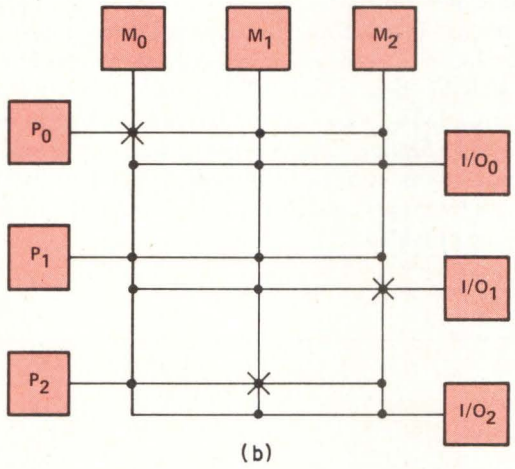


Fig 5 Crossbar switch organizations. Any memory or I/O channel can be connected to any processor through the crossbar switch matrix (a). A crossbar switch enables multiple simultaneous connections (b), if they are mutually exclusive. Three simultaneous connections (M_0 to P_0, I/O_1 to P_1, and M_1 to P_2) are denoted by Xs in the diagram

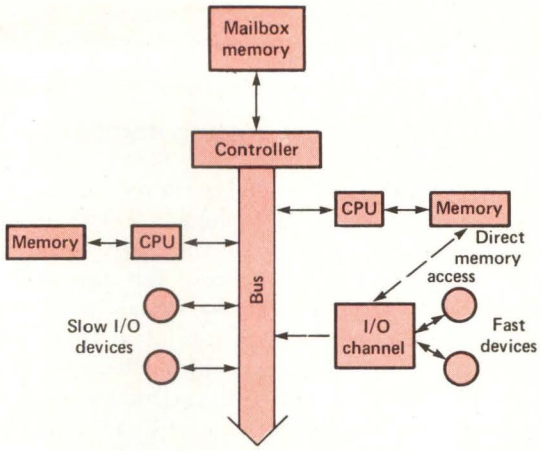


Fig 6 Mailbox memory. Processors and I/O channels communicate through mailbox memory, a shared resource consisting of messages, data files, request blocks, or I/O queues. Sending processor places information in mailbox for receiving processor or I/O channel

implementation. The complexity becomes enormous as N and M become large. Cost of the crossbar dominates the cost of N active elements and the M passive memory elements for sufficiently large N.

Reliability of the system depends on valid operation of the N x M different bus sets and each crosspoint connection. Duplication or segmentation of the matrix into autonomous blocks is necessary to ensure some degree of fault-tolerance.

Other bus structures are possible. The multiple time-shared bus is a combination of single time-shared system and the multiported system, while multiple sets of single time-shared buses are a combination of the single time-shared system and the crossbar switch. For simplicity, a single bus or a restricted multiported memory (two or four ports) will be most prevalent in μMPSs.

Interprocessor Communications

In the MIMD environment, principal interprocessor communication media is the mailbox memory. Processors in this context are central processing units (CPUs) or I/O direct memory access (DMA) channels. Mailbox memory, shown in Fig 6, is a shared resource consisting of messages, data files, request blocks, or queues. The sending processor structures information and places it in the mailbox. The receiving processor "looks" in the mailbox, or the sending processor "rings a doorbell" to indicate that there is something in the mailbox for the recipient processor.[15] Polling, flags, jump conditions, interrupts, or special instructions can be used to alert the receiving processor of information to be taken. A status bit, residing in memory or external hardware, is generally used to indicate the condition of the mailbox (whether it has meaningful information or not). These bits are similar to the test-and-set status flags discussed earlier. Ford[16] has proposed PUT and GET instructions for a mailbox controller with BLOCK and WAKEUP signals from the controller to processors on the system bus. This controller can process only one PUT or GET signal at any time; thus competition for mailbox memory must be resolved by arbitration.

Failure Detection and Recovery

Ability to identify and isolate failures to achieve fail-safe/failsoft capabilities is often the prime motivation for a multiprocessor design. The degree of fault detection, task reassignment, and duplexing of functional units depends on the application's integrity requirements. Failures can be detected using various mechanisms: (1) parity on the system bus for both address and data, (2) local diagnostics for each PM in private read-only (ROM) or programmable read-only memory (p/ROM),

hardware failsafe timers to monitor the operation of PMs and requests for shared resources, (4) protected memory to detect address out of range, and (5) invalid op code or other invalid condition detection.

Microprocessor Chip Requirements

Based on this investigative study, microprocessor chips that are desirable for μMPS should provide machine cycle status information (instruction fetch cycle, memory read/write cycle, valid address, interrupt acknowledge) and appropriate bus strobe signals as dedicated pins. This is required for bus control and failure detection. A READY control input which allows the microprocessor to enter WAIT state is necessary for cases when the device to be accessed does not respond (due to bus contention or previous allocation). The chip should also provide a HOLD input that halts the microprocessor and places address, data, and control buses in 3-state operation at the conclusion of the instruction being executed and activates a HOLD ACKNOWLEDGE output. When the hold signal is removed, the processor begins execution at the next sequential instruction. The 3-state feature is useful only for small μMPS sharing read/write memory. In such a system, the processor bus and system bus are the same. Larger systems require buffers, data bus controllers, or bus conversion interface logic, which must be put into 3-state operation before another microprocessor or DMA controller can gain bus access. For this reason, the interface logic that converts the processor bus to the system bus must have a 3-state control input.

In addition, a BUS REQUEST output to a bus arbiter chip that resolves bus access conflicts and sends back acknowledgements to a BUS GRANT input on the microprocessor is desirable. BUS IN and BUS OUT signals are alternatives if daisy-chain bus arbitration is used. In that case, BUS OUT of each microprocessor is connected to the BUS IN of the next lower priority microprocessor in the daisy chain. When BUS REQUEST becomes active, the microprocessor is automatically put in the WAIT state, and an external (or internal) failsafe timer is triggered to begin a count down. If a BUS GRANT or a READY ACKNOWLEDGE has not been received when the counter reaches zero, the processor is awakened via an interrupt that indicates failure to gain control of the system bus or device not available (busy or failure).

System bus utilization will be improved by provision of a DELAY instruction for internal time loops while waiting for a shared resource without accessing buses. An indivisible test-and-set instruction with memory lock or external self-locking flags will allow control of shared resources. Effective interprocessor and processor I/O communications will be achieved if good indirect, indexed addressing capabilities using internal 16-bit registers are provided.

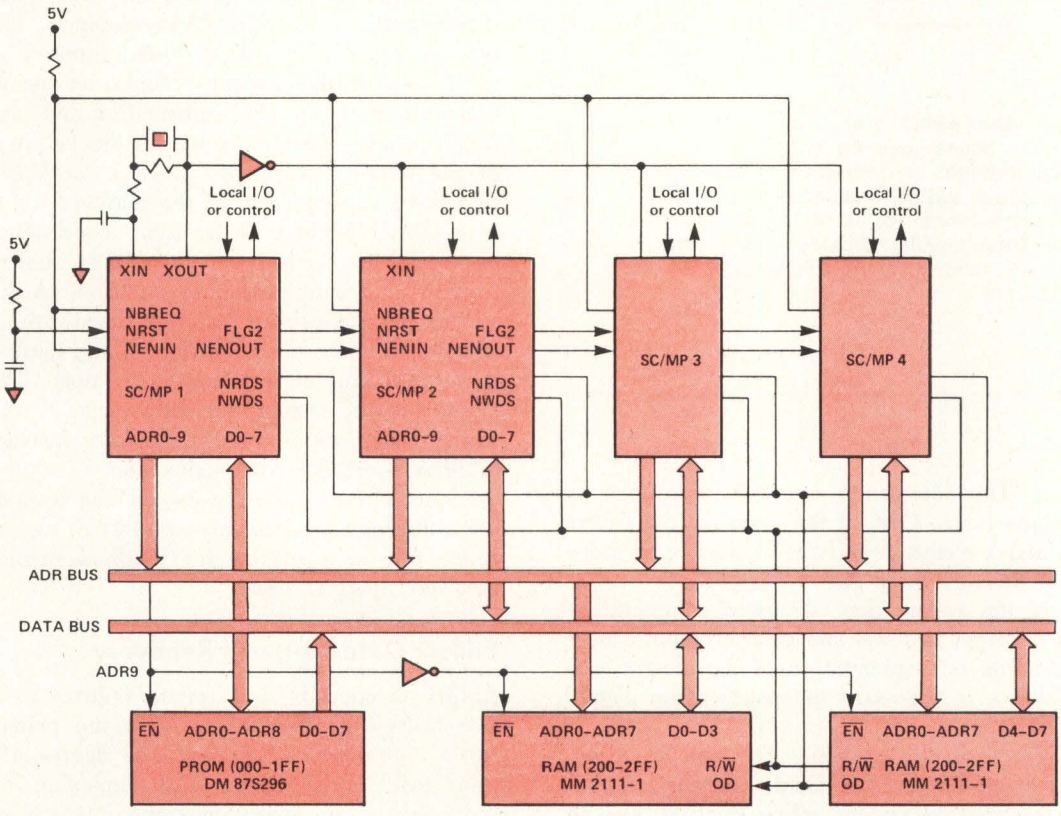


Fig 7 SC/MP-based multiprocessor. One crystal provides clocks for four SC/MP microprocessors that are interconnected through daisy-chain bus

Features of Available Microprocessors

Among the various microprocessors available for use in multiprocessing, many provide some or all of the functions described previously. Features of some individual microprocessors are summarized here.

National Semiconductor SC/MP

(1) NBREQ, NENIN, NENOUT pins for bus control in DMA and multiprocessor applications. Daisy-chain or prioritized bus control are possible (see Fig 7).

(2) Delay (DLY) instruction for built-in software delay when accessing a shared peripheral or memory. There are no instruction fetches during the duration of the delay, permitting other microprocessors to access a single system bus.

(3) Indivisible TAS instructions in the form of ILD and DLD (increment load and decrement load)

(4) Internal oscillator that permits a single crystal to drive all SC/MPs in a system for a low cost μMPS.

Motorola 6800

(1) Since each machine cycle is composed of two phases (ϕ 1 = address/control signal set-up followed by ϕ 2 = data transfer), a time-multiplexed dual-6800 system is possible. One microprocessor can be setting up its address and control signals while setting up its data bus for 3-state operation during ϕ 1, while a second processor is sending or receiving data with its address and control signals in 3-state operation. During ϕ 2, the roles of the microprocessors are reversed. A single clock generator (6875) supplies ϕ 1 and ϕ 2 to both processors. Three-state buffers (6885-8) are used on the address and control signal while a bus switch (6881) is used for the data bus (see Fig 8).

(2) TSC signal is available to hold processor and to place address and control signals in 3-state mode. DBE, or a signal to a bus transceiver, is necessary to put the data bus in 3-state operation.

(3) HALT input is provided to allow suspension of the processor.

Signetics 2650

(1) Static design permits PAUSE input to be activated or CLOCK to be stopped for indefinite suspension of a 2650. Dynamic microprocessors specify a maximum suspension time, after which the processor will not operate properly due to loss of information that is capacitively stored. Suspension is useful for block transfer DMA or when waiting for a shared resource.

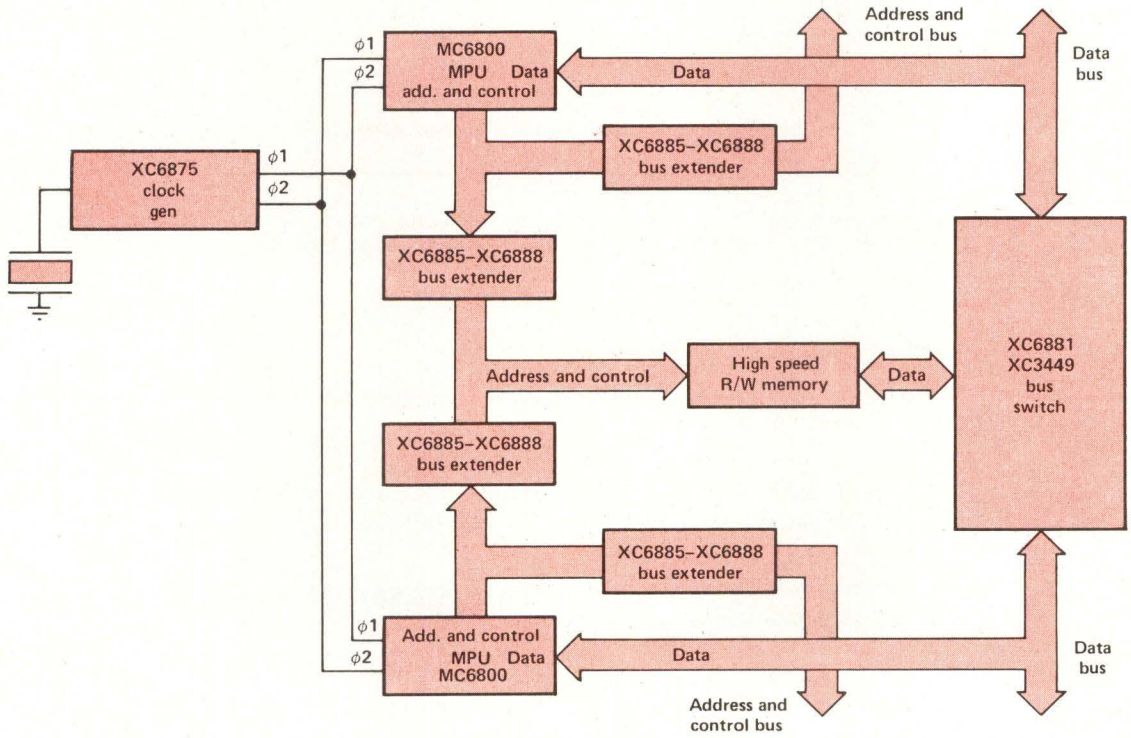


Fig 8 6800-based multiprocessor. Two 6800 microprocessors share common read/write RAM memory through bus switch which creates two ports

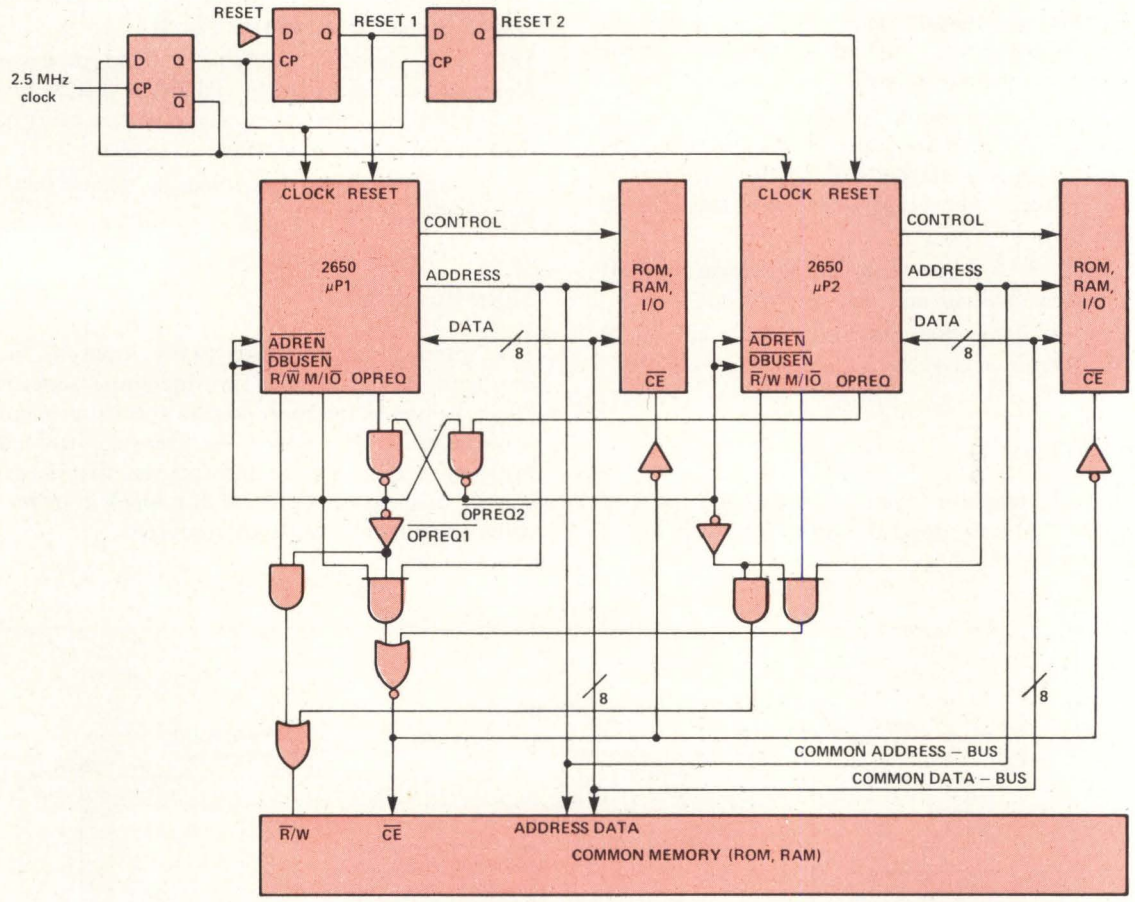


Fig 9 2650-based multiprocessor. Two 2650 microprocessors can access shared instruction and data memories (ROM and RAM respectively) through time-shared address and data bus

(2) OPACK can be used to stretch an I/O or memory cycle if the peripheral device or memory is busy.

(3) Low time of OPREQ can be used by a second 2650 for system bus access. This technique is shown in Fig 9, and is similar to the 6800 time-multiplexing dual-microprocessor system.

(4) Three clock periods per instruction cycle could be used as shortened OPREQs in a 3-processor system

(5) Versatile addressing modes, particularly indirect and indexed, permit software memory mapping

Intel 8080

(1) RDY "handshake" input with WAIT ACKNOWLEDGE

(2) HOLD input with HOLD ACKNOWLEDGE (equivalent to 6800 HALT)

Intel SBC 80/20 Microcomputer Board

(1) Custom bus arbiter chip for up to four daisy-chained active elements (SBC 80/20s or I/Os) or up to 16 prioritized active elements with external priority resolver logic.

(2) Failsafe timer to detect inability of accessed device to lower READY input. This indicates failure to gain control of system bus, device busy, or device failure.

(3) System bus override feature guarantees that the 80/20 does not lose control of the system bus. Invoked

by an OUTPUT instruction to set or to reset an override flip-flop.

LSI Peripheral Chips

In conjunction with the microprocessor chip requirements, various LSI peripheral chips are needed for μMPS. These should include a bus arbiter with fixed/rotating priorities, a microprocessor bus/system bus interface, multi-failsafe timer, and test-and-set status register with self-lock mechanism. Also desirable are dynamic writable field-programmable logic arrays (FPLAs) for use in memory mapping of addresses and interrupt switching to "best" microprocessor, and possibly a crossbar matrix system bus.

Summary

The main problems of μMPSs are independent of microprocessors. At this point in time, technology is considerably ahead of software and architecture.

Specific operating system issues that remain to be effectively solved are:

(1) Identification of parallelism and subdivision of a process into tasks

(2) Allocation of tasks

(3) Scheduling processors to operate concurrently on a process

(4) Interprocessor communications

(5) Prevention of deadlock when accessing shared resources

(6) Failure identification, isolation, and task reassignment

Architectural problems (combined hardware/software) to be resolved include:

(1) Choice of interconnect method for system bus

(2) Interrupt assignment strategy

(3) Memory mapping technique

(4) Evaluation or monitoring tools for system development and debug

Unless progress is made in these areas, the trend toward multiprocessing will be significantly delayed, despite the availability of low cost microprocessors, LSI input/output, programmable read-only memories, and semiconductor read/write memories.

Conclusion

The architecture most likely to be employed in the near future will consist of asymmetric PMs, a single bus with centralized arbiter or a multiport bus, dedicated assignment of interrupts, interprocessor communication through shared memory mailboxes, TAS hardware flags, and limited failure recovery. The operating system will structure tasks into request blocks and queue them to a preassigned PM. Two to four microprocessors with the same number of I/O channels are a reasonable number for prototype μMPS. Colon[17] has proposed an interesting quasi-μMPS architecture that may be quite practical. Outstanding features of commercially available microprocessors for implementation into multiprocessing systems are itemized within this article.

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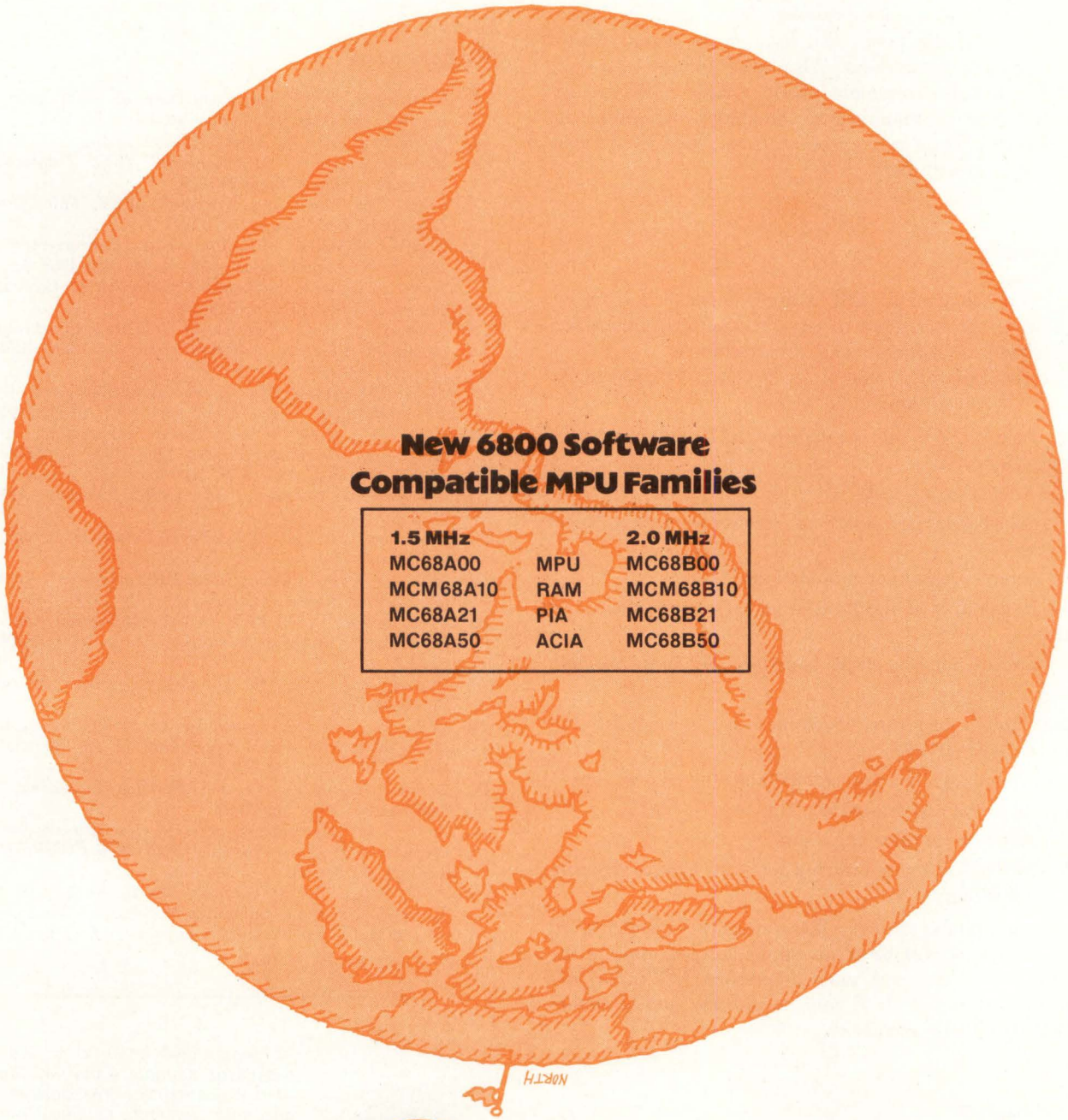

New 6800 Software Compatible MPU Families

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MCM68A10	RAM	MCM68B10
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MC68A50	ACIA	MC68B50

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The new families also offer a 20% reduction in power consumption and several clock specification changes that significantly reduce the complexity of clock generator/driver circuitry. System speed advantages are insured because the new families include RAMs, Peripheral Interface Adapters, and Asynchronous Communications Interface Adapters.

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Motorola's Introducing More Than 100 New Microprocessor Family Devices This Year.

The list spans all manner of MPU family functions from several new microprocessors and a couple of new single-chip microcomputers to new LSI peripheral interface devices and memories. All will be available by year's end.

Motorola's 1977 MPU Family Introductions.

	Device	Function
□	MC6400P	Microcontroller
□	MC6400CP	Microcontroller
□	MC6400L	Microcontroller
□	MC6400CL	Microcontroller
■	MC6800P	Microprocessor
□	MC6800CP	Microprocessor
□	MC6800MTL	Microprocessor
□	MC6800ML	Microprocessor
■	MC68A00P	Microprocessor
■	MC68B00P	Microprocessor
■	MC68A00L	Microprocessor
■	MC68B00L	Microprocessor
□	MC6802P	Microprocessor + RAM & Clock
□	MC6802CP	Microprocessor + RAM & Clock
□	MC6802L	Microprocessor + RAM & Clock
□	MC6802CL	Microprocessor + RAM & Clock
■	MCM6810P	Byte Organized RAM
□	MCM6810CP	Byte Organized RAM
■	MCM68A10P	Byte Organized RAM
■	MCM68A10L	Byte Organized RAM
■	MCM68B10P	Byte Organized RAM
■	MCM68B10L	Byte Organized RAM
□	MCM6810MTL	Byte Organized RAM
□	MCM6810ML	Byte Organized RAM
■	MC6821P	Periph. Interface Adapter
□	MC6821CP	Periph. Interface Adapter
■	MC6821L	Periph. Interface Adapter
□	MC6821CL	Periph. Interface Adapter
■	MC68A21P	Periph. Interface Adapter
■	MC68A21L	Periph. Interface Adapter
■	MC68B21P	Periph. Interface Adapter
■	MC68B21L	Periph. Interface Adapter
□	MC6821MTL	Periph. Interface Adapter
□	MC6821ML	Periph. Interface Adapter
□	MC6840P	Programmable Timer
□	MC6840CP	Programmable Timer
□	MC6840L	Programmable Timer
□	MC6840CL	Programmable Timer
□	MC68A40P	Programmable Timer
□	MC68A40L	Programmable Timer
□	MC68B40P	Programmable Timer
□	MC68B40L	Programmable Timer
□	MC6840MTL	Programmable Timer
□	MC6843P	Floppy Disk Controller
□	MC6843L	Floppy Disk Controller
□	MC6844P	DMA Controller (1.0 MHz)
□	MC6844L	DMA Controller
□	MC6845P	CRT Controller
□	MC6845L	CRT Controller
□	MC6846P	MC6802 Combo
□	MC6846CP	MC6802 Combo
□	MC6846L	MC6802 Combo
□	MC6846CL	MC6802 Combo
■	MC6850P	Asynch. Comm. Interface Adapter
□	MC6850CP	Asynch. Comm. Interface Adapter

	Device	Function
■	MC68A50P	Asynch. Comm. Interface Adapter
■	MC68A50L	Asynch. Comm. Interface Adapter
■	MC68B50P	Asynch. Comm. Interface Adapter
■	MC68B50L	Asynch. Comm. Interface Adapter
□	MC6850MTL	Asynch. Comm. Interface Adapter
□	MC6850ML	Asynch. Comm. Interface Adapter
■	MC6852P	Synch. Serial Data Adapter
□	MC6852CP	Synch. Serial Data Adapter
□	MC68A52P	Synch. Serial Data Adapter
□	MC68A52L	Synch. Serial Data Adapter
□	MC6852MTL	Synch. Serial Data Adapter
□	MC6854P	Adv. Data Link Controller
□	MC6854CP	Adv. Data Link Controller
□	MC6854L	Adv. Data Link Controller
□	MC6854CL	Adv. Data Link Controller
□	MC68A54P	Adv. Data Lini Controller
□	MC68A54L	Adv. Data Link Controller
□	MC68B54P	Adv. Data Link Controller
□	MC68B54L	Adv. Data Link Controller
□	MC6854MTL	Adv. Data Link Controller
■	MC6860P	0-600 bps Modem
■	MC6862P	2400 bps Modulator
□	MC6875P	Clock Oscillator/Driver—
□	MC6875L	Clock Oscillator/Driver—
□	MC68488P	Gen. Purp. Interface Adapter
□	MC68488CP	Gen. Purp. Interface Adapter
□	MC68488L	Gen. Purp. Interface Adapter
□	MC68488CL	Gen. Purp. Interface Adapter
□	MC68A488P	Gen. Purp. Interface Adapter
□	MC68A488L	Gen. Purp. Interface Adapter
□	MC68B488P	Gen. Purp. Interface Adapter
□	MC68B488L	Gen. Purp. Interface Adapter
□	MC68488MTL	Gen. Purp. Interface Adapter
■	MCM6830P	1K ROM
□	MCM6830CL	1K ROM
□	MCM68A30P	1K ROM
□	MCM68A30L	1K ROM
□	MCM68B30P	1K ROM
□	MCM68B30L	1K ROM
■	MCM68308P	8K ROM
■	MCM68308L	8K ROM
□	MCM68308CL	8K ROM
□	MCM68A308P	8K ROM
□	MCM68A308L	8K ROM
□	MCM68316AP	16K ROM
□	MCM68316AL	16K ROM
■	MCM68316EP	16K ROM
■	MCM68316EL	16K ROM
□	MCM68A316EL	16K ROM
■	MCM68708L	8K EPROM
■	MCM68A708L	8K EPROM

1st Quarter 1978

□	MC6801	Microprocessor

Legend:

Frequency Range
MC68XX = 1.0 MHz
MC68AXX = 1.5 MHz
MC68BXX = 2.0 MHz

Temperature
MC68XX = 0°C to +70°C
MC68XXC = −40°C to +85°C
MC68XXMT = −55°C to +125°C
MC68XXM = MIL 883

Package
MC68XXP = Plastic
MC68XXL = Ceramic
Pin-Out Variations
Suffix A, Suffix E

■ **Denotes Introduced to date.**

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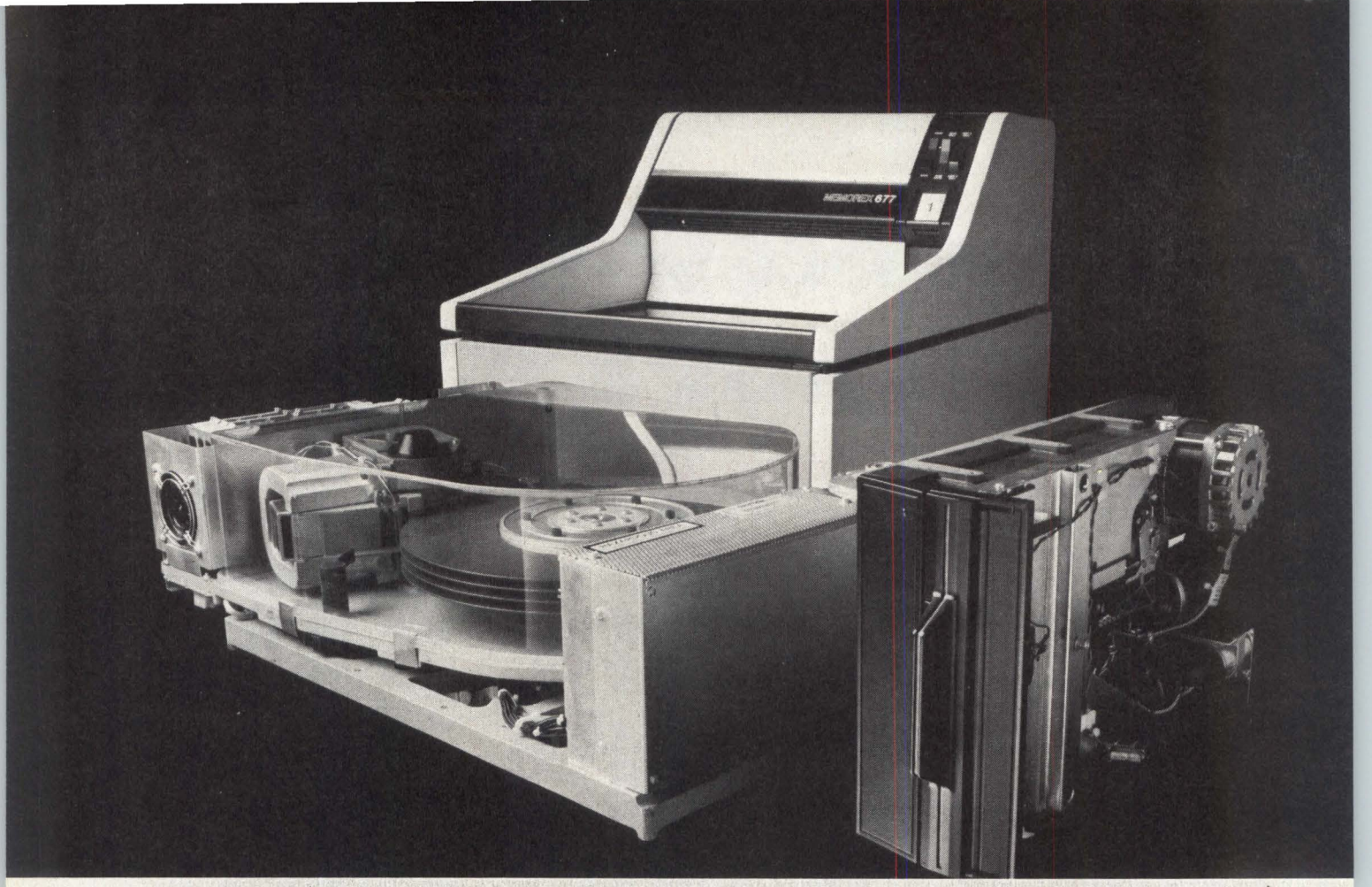

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A 16-terminal minicomputer interface is designed around the universal asynchronous receiver transmitter (UART) after hardware and software design considerations are developed

Design Constraints For a UART-Based Minicomputer Communication Interface

Abraham Hirsch

Data General Corporation
Westboro, Massachusetts

Compared with other techniques, the large-scale integrated universal asynchronous receiver transmitter (UART) provides the easiest method of interfacing minicomputers with terminals. It exploits the benefits of large-scale integration (LSI), including reduced circuit size and increased reliability, and also offers more flexibility. Proper design of terminal interfaces, however, must include functions that the UART alone does not provide, since it does not constitute a complete minicomputer communications interface.

Design of a single-terminal interface is not even as simple as connecting the UART to the input/output (I/O) bus of the minicomputer. Timing and signals of the I/O bus must be translated to those necessary for the minicomputer. A multiterminal interface is a much more complex design problem because, in addition to the basic functions, a multiplexing function must be included for transfer of data from several UARTs. Implementation is important because of its impact on the software that will use the interface. By taking advantage of the UART's 3-state bus capability, a multiterminal multiplexer design can be efficient in both hardware and software.

Design of the communication subsystem of a minicomputer begins with evaluation of constraints which will affect the interface's structure. Specific functional goals must then be defined. It is also necessary to describe the constraints imposed by the minicomputer's I/O structure and the UART's functionality. Required interface information for a multiterminal communications subsystem is analyzed to provide for efficient hardware and software. Finally, the hardware configuration for a 16-terminal multiplexer with an easily expandable structure is presented.

General Design Constraints

A communication subsystem designer must work within the framework of several design constraints. One of the most important is the minicomputer's I/O structure. This structure determines the method by which software communicates with interface hardware. The number of addressable I/O devices and I/O instruction capabilities, such as interface register addressing and programmable strobes, are defined by the I/O system.

Another consideration is the timing constraints of the I/O bus. In general, the bus is relatively fast compared with the timing necessary for the UART. A method of translating the signals and timing of the I/O bus to those of the UART must be devised.

Additional hardware constraints include the amount of space available on the printed circuit (PC) board and the number of I/O pins that are available. These constraints limit the number of terminals that can be interfaced on one PC board.

Functional Design Goals

As a design example, details of the development of a 16-line asynchronous multiplexer are presented. This number of lines allows easy addressing and makes maximum use of available board space. Although this design does not include modem interfaces, future designs should be capable of implementing them within the constructed software/hardware framework. Similarly, the design should allow synchronous multiplexers to make use of a similar software format and to be inter-

UART Functions

The asynchronous multiplexer is based upon use of a UART for each asynchronous communication line. The UART is basically a serial/parallel converter that contains both receiver and transmitter functions. The transmitter takes up to eight bits in parallel from the I/O bus interface and shifts them out serially; the receiver operates in the reverse order.

Control and error detecting bits are added by the UART to each transmitted character and are stripped from each received character. A serial character consists of a start bit, five to eight data bits, an optional parity bit, and one or two stop bits (some UARTs supply one and one-half stop bits on 5-bit characters). Bits per character, parity mode, and number of stop bits may be externally set with the control strobe. These parameters determine the characteristics of both receiver and transmitter. Baud rate is determined by clocks supplied to the receiver and to the transmitter. Because of its internal timing chain, the UART requires that these clocks be 16 times the desired baud rate. Signals to and from a typical UART are listed in "Representative I/O Signals of Available UARTs."

Double buffering in the transmitter consists of a holding register and a separate shifting register; this allows the interface a character time to supply the next character. The transmitter buffer empty (TBMT) signal is used to indicate that the transmitter holding register is available for another character. Data are written into the holding register with data strobe (DS). End of character (EOC) is used to signify the end of each transmitted character. Transmitter timing is demonstrated in Fig A. For specific timing values, consult the manufacturer's specifications.

The receiver is also double buffered. Data available (DAV) is used to indicate that a completed character is available in the receiver holding register. The 3-state holding register outputs are enabled by received data enable (RDE). These outputs will enter a high impedance state when disabled. This third state allows outputs from several UARTs to share a common signal line if only one output is enabled at any instant. The interface acknowledges the receipt of a character with the reset data available (RDAV) signal. If data available is still asserted when the next character is completed, the over run (OR) flag will be set. Receiver timing is demonstrated in Fig B. Consult manufacturer's specification sheets to determine specific time intervals.

The receiver checks parity and stop bits of the received character against those specified by control strobe (CS). Errors are indicated by parity error (PE) and/or framing error (FE) flags. These three flags have 3-state outputs and are enabled by status word enable (SWE). SWE also enables DAV and TBMT. SWE and RDE permit easy multiplexing of the UART outputs on a bus to the interface.

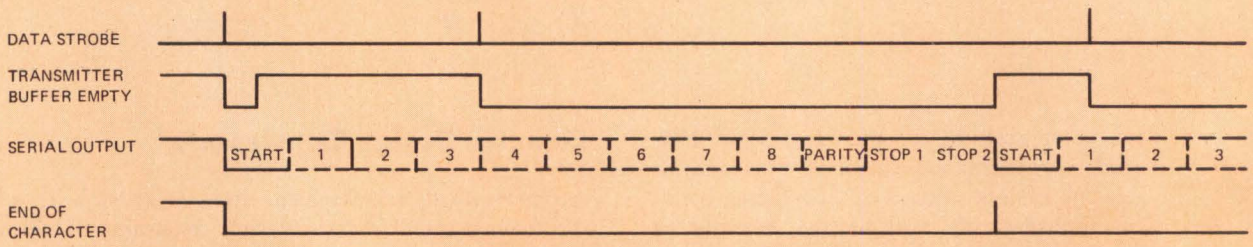

Fig A Transmitter timing. UART transmitter timing for 8-bit character with parity and two stop bits. Data strobe can occur at any time when transmitter buffer is empty

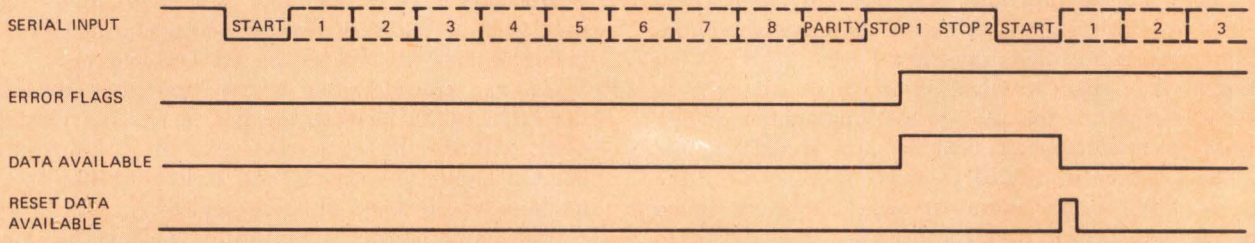

Fig B Receiver timing. UART receiver timing for 8-bit character with parity and two stop bits. Overrun error will occur if data available is not reset before completion of next character

mixed with the asynchronous multiplexers. The interface scheme should be flexible enough to allow for easy expansion of the communication subsystem to include a large number of lines of a variety of types. A reasonable limit on the number of lines required for most applications and consistent with binary addressing is 256.

Specific goals for the interface include:

(1) Capability of addressing up to 256 lines.

(2) In order to preserve I/O address space, the communication subsystem should be addressed as a single device.

(3) The software interface word format should include provisions for the following information: transmit data, receive data, receiver status, modem control and status, synchronizing (SYN) and data-link escape (DLE) characters for binary synchronous interfaces,

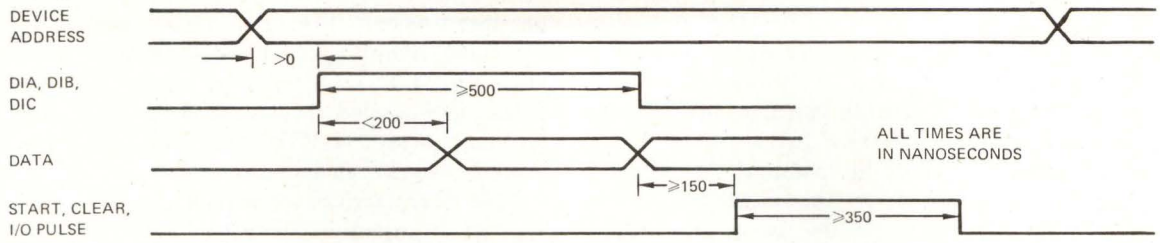

Fig 1 Programmed data input on I/O bus. Diagram shows times for point of physical connection to bus. Timing within interface circuits must account for additional propagation delays and access times

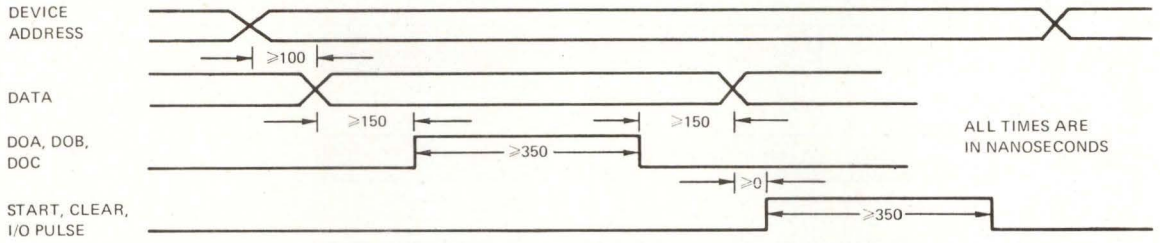

Fig 2 Data output instruction execution. Timing diagram illustrates write operation performed by data out instruction on I/O bus

and line characteristics, such as baud rate, character size, and parity type.

(4) Capability of implementing a basic 16-terminal interface on a 15-in (38.1-cm) square PC board.

I/O Bus Constraints

For this design, the interface is connected to the I/O bus of the NOVA® and ECLIPSE® minicomputers. Bus structure allows the addressing of 64 device codes. Therefore, the communication subsystem has a single device code instead of one for each communications line.

The I/O instruction is capable of reading three input registers, labeled A, B, and C, from a single device code; and the minicomputer can output data to three registers, also labeled A, B, and C, in the interface. In addition, there is a choice of three programmable strobes that may be activated by the instruction. Two of these strobes have specific functions: the start pulse is used to start the device by setting its busy flag to 1 and its done flag to 0, and the clear pulse is used to idle the device by setting both busy and done flags to 0. The third strobe is available to the interface designer for use as desired.

When the device finishes its operation, it resets the busy flag and sets the done flag. The minicomputer processor has the capability of testing the busy and done flags of a device under program control. Setting the done flag generates an interrupt to the processor if the done flag has not been masked by a previous mask out instruction, and if the processor has enabled the interrupt requests. The interrupting device can be identified by using the interrupt acknowledge instruction; this places the device code of the interrupting device in the specified accumulator. Since the interrupt line is daisy-chained from one device to the next, priority is given to the interrupting device on the chain that is closest to the processor.

Timing of an I/O read operation performed by a data in instruction is shown in Fig 1. A write operation performed by a data out instruction is shown in Fig 2. A considerable length of time is allowed for accessing the device's I/O registers to account for maximum propagation delays through bus drivers and receivers.

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Interface Data

Four types of information must be conveyed between the software and the communication subsystem. The first is line addresses. For line initializing and setup purposes, the software must be able to specify a particular line with which it wants to communicate. When responding to an interrupt from the communication subsystem, software first must be able to quickly and efficiently identify the particular line that generated the interrupt and then prepare the interface for data transfers with that line.

A second type of information is the actual data to or from the communication lines. These data consist of transmit and receive characters. Because of its effect on the transmit line, the ability to provide a programmed line break on an asynchronous line is included in this category. On lines with modem interfaces, data needed to control the modem, such as data terminal ready (DTR) and request to send (RTS), should also be included.

Line characterization parameters comprise the third type of information. These include transmitter enable, receive enable, line speed, number of bits per character, and parity mode. For asynchronous lines, the number of stop bits must be included; for synchronous lines, the SYN and DLE characters must be provided.

Status information, the fourth type, identifies the nature of the interrupt, whether caused by receiver,

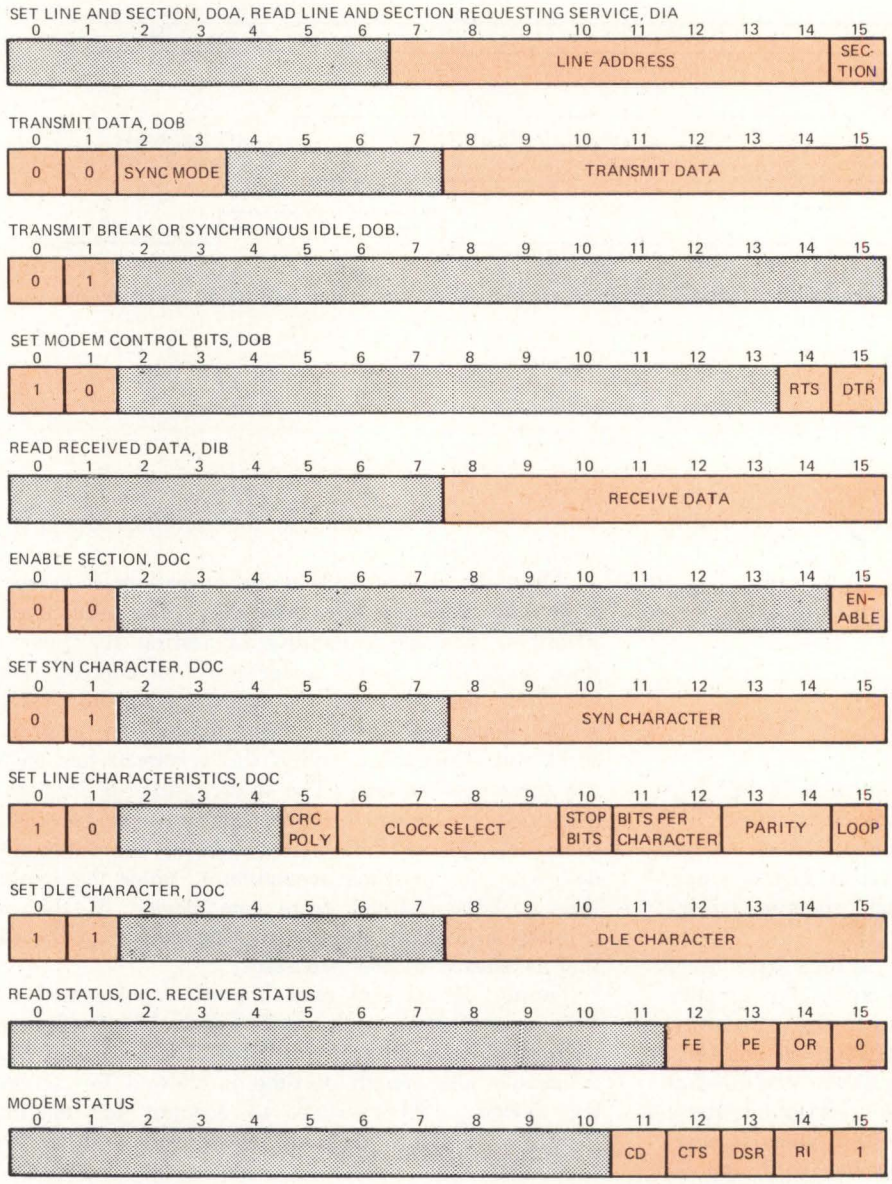


Fig 3 Interface data word formats for communication subsystem. Although primary focus is an asynchronous multiplexer, word formats for modem interfaces and synchronous multiplexers are included for completeness

transmitter, or modem. If caused by the receiver when a character becomes available, the information should include the state of the parity error (PE) and over run (OR) [and framing error (FE), if asynchronous] flags. (The Table contains a list of UART signals and their functions.) If caused by the modem, the state of the inputs from the modem, such as clear to send (CTS), data set ready (DSR), carrier detect (CD), and ring indicator (RI), should be included.

Addressing and data categories are both bidirectional. Parameter information is always output from the minicomputer; and status and error information are always input to it. Since three input and three output registers are allowed for every device code, each can be assigned naturally to an information type. A registers can be used for addressing or identifying a particular line, B registers for passing data characters. The C output register can be used for parameter initialization, while the C input register can be used for status and error information. This allocation of registers reduces the building of new I/O instructions by the software since a register is assigned a function generally utilized by a particular subroutine.

Word Format

Within an information category it may not be neces-

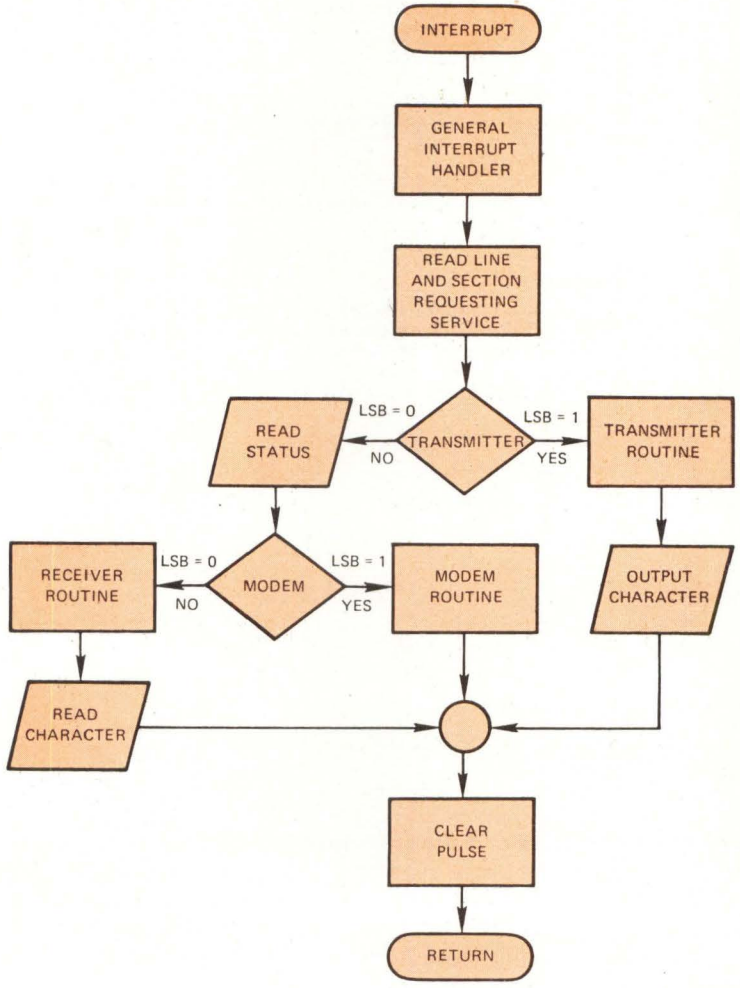
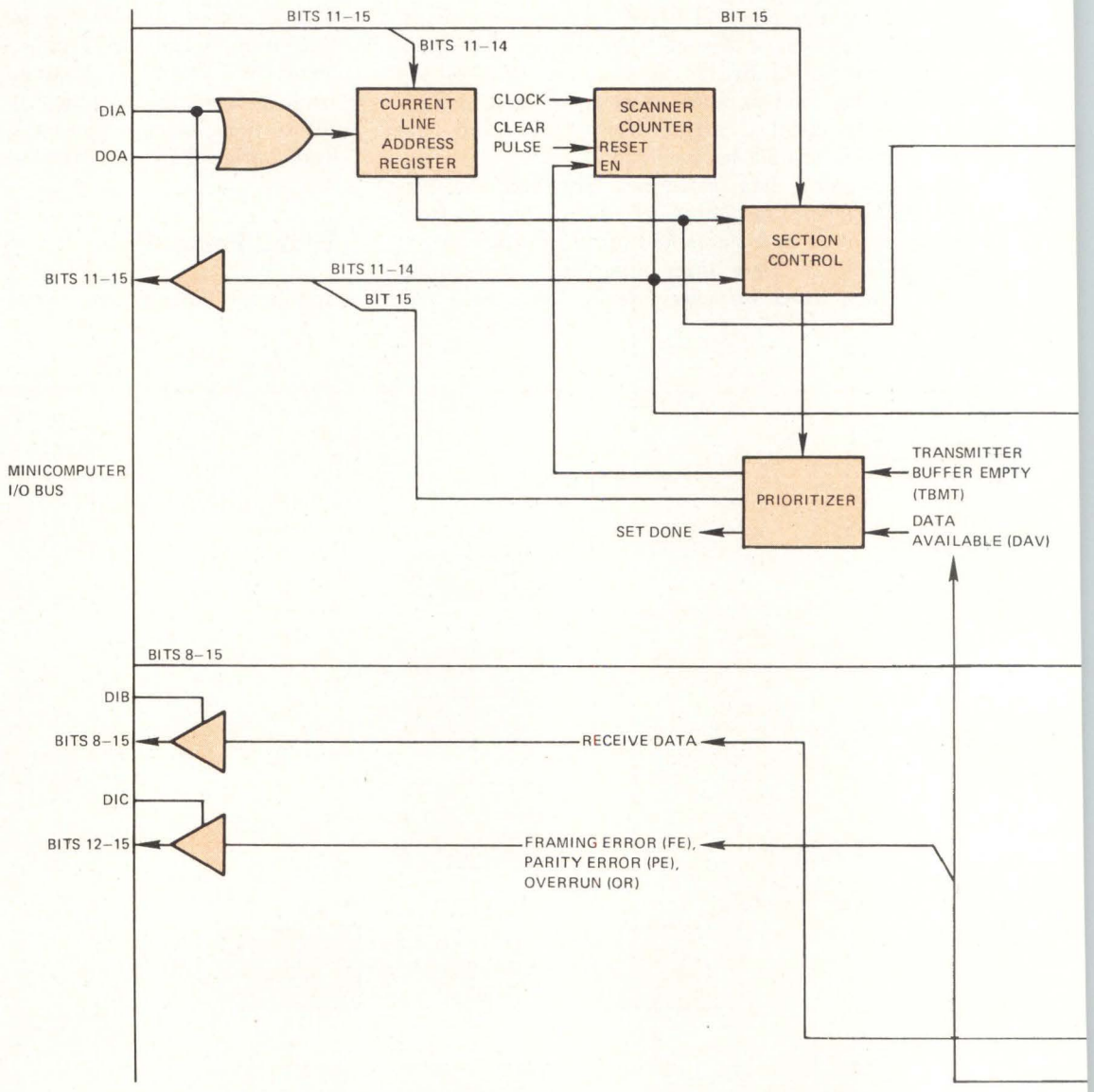


Fig 4 Status determination. Efficient determination of nature of interrupt is accomplished by using section bit as LSB of line address. LSB of status word differentiates between receiver status and modem status



sary to fit all information to be transferred into a 16-bit data word. It is also inefficient to place it all within a single data word if the desired functions are incompatible. For example, although there is sufficient space to include modem control bits with each transmit character transferred, these two types of information are not required simultaneously, either in software or hardware. It is more reasonable to provide a specific word transfer for each type of information.

This is possible for output operations by allowing the most significant bits of the data word to specify a register. Software cannot specify any more than one of the three registers for input. If the hardware is allowed to choose and specify, the number of input registers can be increased. The hardware sets bits within the input word to identify its type. Using these two techniques, the data formats chosen for the communication subsystem are shown in Fig 3.

Line addressing is performed through use of the A register. Eight bits are provided allowing up to 256 lines to be addressed. An additional least-significant bit (LSB) is used to specify the receiver or transmitter

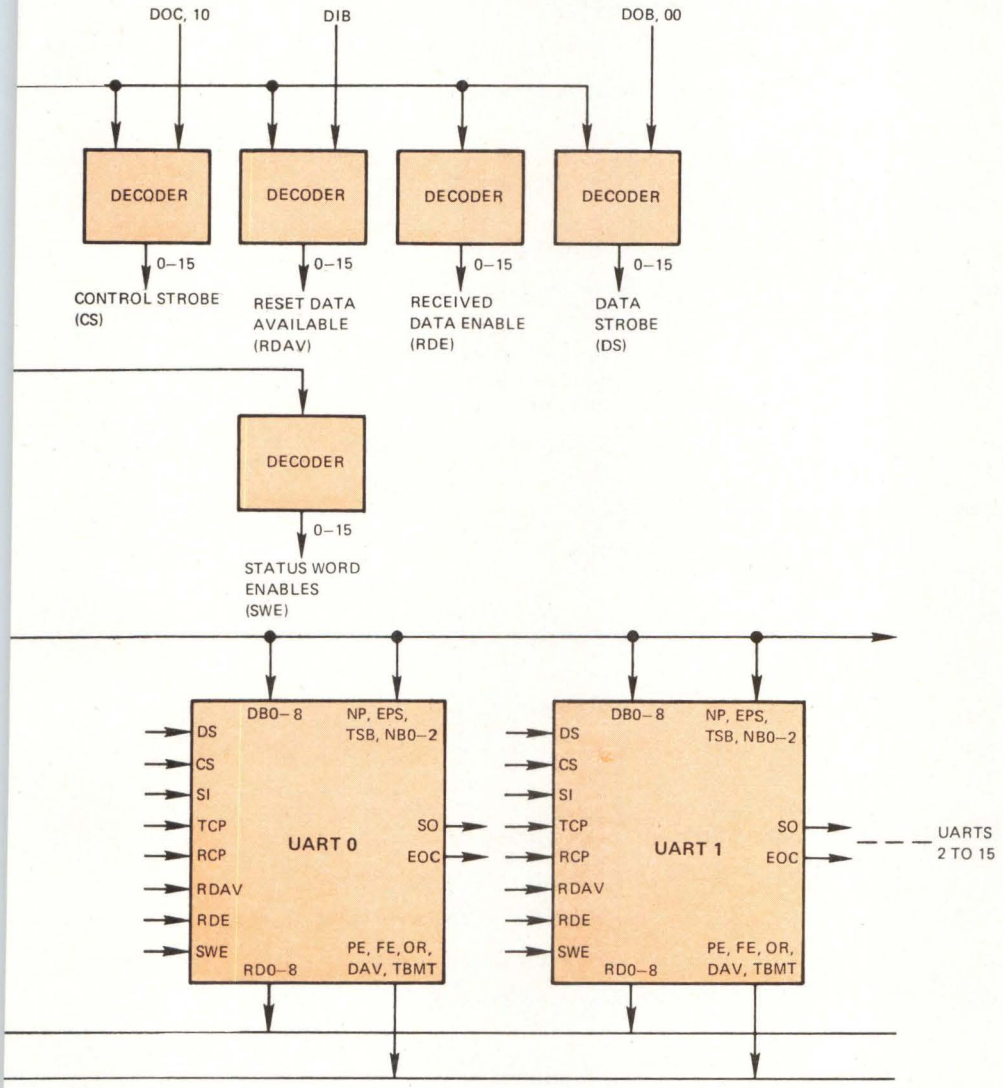


Fig 5 Hardware configuration. 3-state buses are provided for received data and for status word. Scanner counter and current line address are decoded to provide enables and strobes for each UART

section of a line. This is useful because it permits easy identification of the nature of the interrupt, while also identifying the interrupting line by executing a read line and section requesting service (DIA) instruction. The resulting nine bits can be used to locate a line handling routine in software (Fig 3).

Three different output functions are performed through the B register: transmit data, transmit break for asynchronous lines or idle for synchronous lines, and modem control. Receive data, an input function, is obtained by reading the B register (see Fig 3).

Four output functions and two input functions are served by the C registers. One output function is used to enable and disable the addressed line and section. Two more are allocated for the SYN and DLE characters, and the last is used for specifying line characteristics. Modem and receiver status, the two input functions, are obtained by reading the C register, with the LSB serving to differentiate between the two status types. Thus the necessary handling routine is easily found. A flowchart for locating the proper handler is shown in Fig 4.

Representative I/O Signals of Available UARTs

Symbol	Name	Function
RDE	Received Data Enable	Places received data onto data output lines
RD1 to RD8	Received Data Bits	Data output lines from the receiver holding register provide 3-state outputs and are enabled by RDE
PE	Parity Error	3-state output which is asserted if the received character parity does not agree with the selected parity
FE	Framing Error	3-state output is asserted if the received character has no valid stop bit
OR	Over Run	3-state output is asserted if the previously received character has not been read before the present character is ready to be transferred to the receiver holding register
SWE	Status Word Enable	Line enables status bits PE, FE, OR, DAV, and TBMT
RCP	Receiver Clock	Clock is 16 times desired baud rate
RDAV	Reset Data Available	Resets the data available output
DAV	Data Available	3-state output is asserted when a complete character has been received and transferred to the receiver holding register
SI	Serial Input	Line accepts bit serial input stream
XR	External Reset	Resets all registers, DAV, and error flags. Asserts SO, EOC, and TBMT
TBMT	Transmitter Buffer Empty	3-state output is asserted when the transmitter holding register is ready to accept the next character
DS	Data Strobe	Strobe enters data into the transmitter holding register
EOC	End of Character	Output is asserted at the end of each transmitted character
SO	Serial Output	Transmitted characters are serially output on this line
DB1 to DB8	Data Bit Inputs	Data inputs to the transmitter holding register
CS	Control Strobe	Strobe enters control bits EPS, NB1, NB2, TSB, and NP
NP	No Parity	Control bit which eliminates the parity bit from transmitted and received characters
TSB	Number of Stop Bits	Control bit selects two stop bits instead of one
NB1, NB2	Number of Bits Per Character	Two control bits which determine the number of data bits per character
EPS	Even Parity Select	Control bit selects even parity instead of odd parity which is then appended to the transmitted character and checked on the received character
TCP	Transmitter Clock	This clock is 16 times the desired baud rate

Hardware Configuration

The crux of the multiplexer is the method by which each line interface is given an opportunity to communicate with the software. In this design there can be at most 256 lines with no more than 16 per board; as few as one per board is possible. Interboard priority can be handled in the same manner as done for other peripheral interfaces.

Intraboard priority on the 16-line asynchronous multiplexer can take advantage of the UART's capabilities. A fixed combinational priority requires that the TBMT and DAV signals (see Table) be always available from each UART. These 3-state signals are enabled by SWE. Unfortunately, SWE also enables OR, FE, and PE. These latter three signals have to be multiplexed to supply the proper status for the DIC instruction (see Table).

An easier method is to sequentially scan each of the UARTs by decoding the outputs of a 4-bit counter. A block diagram illustrating this scheme is shown in Fig 5. The SWE for each UART would be activated in turn. The DAV and TBMT signals could be sampled after allowing for settling time. If an active DAV or TBMT is detected, the scanning stops and an interrupt is generated. Priority is given to the receiver rather than to the transmitter. This is done because the interval between transmitted characters is unspecified and there is no consequence in allowing the transmitter to wait. However, the receiver may overrun if the received character is not read before the completion of the next receive character.

Bits 7 to 10 of the A register are determined by the address of the board on which the interrupt is generated. Bits 11 to 14 are the contents of the scanner counter. Bit 15 is 1 if TBMT is set and DAV is not set. This 9-bit value (bits 7 to 15) becomes the current line address and section (see Fig 3). All I/O instructions to the communication subsystem device code then reference this line and section until another DOA or DIA instruction is executed. The current line address and section is decoded to provide RDE and the enable for DS, CS, and RDAV for each UART. For a receive interrupt, RDE gates the receive character from the interrupting UART onto a bus internal to the board. The DIB instruction reads the contents of this bus and causes RDAV to be sent to the UART. For a transmit interrupt, the transmit data DOB instruction causes DS to be sent to the interrupting UART. Similarly, for initialization, CS is generated for the selected UART. Following an interrupt, the clear pulse is used to reset the scanner counter to 0 and to permit it to begin scanning again. In this manner, line 0 has the highest priority and line 15 the lowest.

Enhancements

This design scheme may be improved. One improvement gives even greater priority to the receivers by providing a single receiver-only scan before allowing a transmitter interrupt to be generated. When a true TBMT is found, all receivers would first be scanned before the transmit interrupt is generated.

Another improvement allows the scanner to reset and restart after generating a transmit interrupt; this serves to minimize the delay due to the scanner intervals between interrupts. Once the interrupt has been acknowledged by the software with the execution of the DIA instruction, the clear pulse may be issued to reset and restart the scanner before the requested transmitter character is transferred. A special flag is set within the multiplexer under these circumstances. Since the current line address and section is set by the DIA, it can be used with the flag to mask further interrupts from this particular transmitter while the scanner continues to cycle. After the data are transferred, the flag is reset. In this manner, the scanner is capable of locating the next interrupt. Most likely the new interrupt is disabled while the previous one is serviced, but there is no delay in assertion of the next interrupt once the interrupt request is enabled.

Summary

An efficient hardware configuration for a multiterminal interface which exploits the 3-state bus capabilities of the UART has been demonstrated. By analyzing the information transfer required by the interface, the software process which will operate the interface has also been optimized. A combined hardware/software structure is developed to allow for easy expansion into a subsystem with many line interfaces of various types. This basic structure forms the basis for a complete communications interface product family. Providing a comprehensive framework also permits the easy development of both hardware and software products by eliminating a multiplicity of individual interface formats.

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Presently employed as a communication system engineer at Data General Corp, Abraham Hirsch is involved in the development of communications products for minicomputers. His experience includes design of military data communications interfaces. He holds a BS degree and MEE degree from Cornell University.

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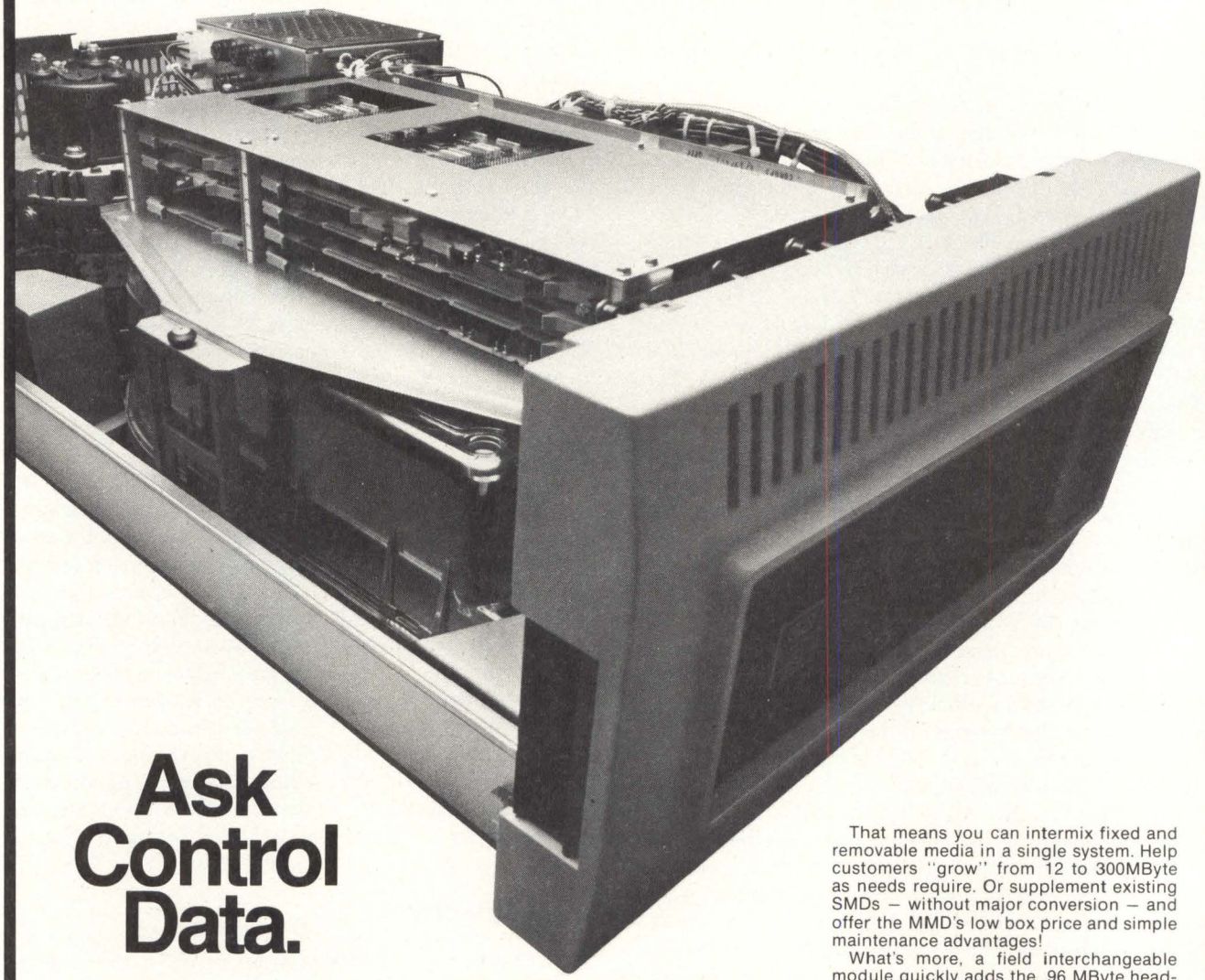

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A Distributed Computer System For Laboratory Automation

Granino A. Korn*

Max-Planck-Institut für Biophysikalische Chemie
Göttinen, West Germany

Computer-controlled instrumentation has become indispensable for research experiments and production or safety tests that require large numbers of measurements. Laboratory automation often is combined neatly with computer processing of measured data. Over the years, such instrumentation systems have used large time-shared computers, minicomputers (which were first called "laboratory computers"), programmed desk calculators, and special-purpose logic. Computers can be dedicated to specific experiments or instruments, or they can be time-shared. In either case, communication links between instruments, computers, and peripheral devices, such as printers and tape drives, are important components of a complete instrumentation system.

More recently, costs of powerful small processors (microprocessors), solid-state memory, and interface and communication circuits have been reduced so dramatically that a complete reassessment of laboratory-automation design is now necessary. Dedicated microprocessors, which can associate substantial processor power with each instrument at very low cost, allow computer programming to replace the design and redesign of special-purpose logic (not only electronics, relays, but also cams, gears, etc). Nevertheless, nondedicated laboratory computers, and even central computers serving several laboratories, still have a place justified by the cost of duplicating expensive peripherals (line printers, large disc and tape systems) and/or by large-scale data processing requirements. For the same reason, reliable, inexpensive communication links continue to be important.

Functions of an Instrumentation System

To be specific, an instrumentation system (Fig 1) provides certain general functions.

Timing and control of experiments—Resetting, scale setting, calibration, setting temperatures, and test voltages; timing and supervising measurement sequences; and alarm and abort operations

Data acquisition—Measurements produce numerical data from selected sensors or transducers. Typically, successive measurements produce arrays of data, such as time histories or frequency, energy, or mass spectra

Data processing—This may be as simple as zero suppression and scaling, or more complicated (statistics computation, integration, Fourier transformation, or filtering with subsequent display, printout, and/or storage of results

Data storage and data-base management—Typically in the form of files labeled with codes designating the experiment, investigator, time, and instruments used for easy retrieval and cross-reference

Data display and/or hardcopy preparation—Directly and/or from stored files

These functions can involve a processor per instrument, no processor at all, a laboratory minicomputer time-

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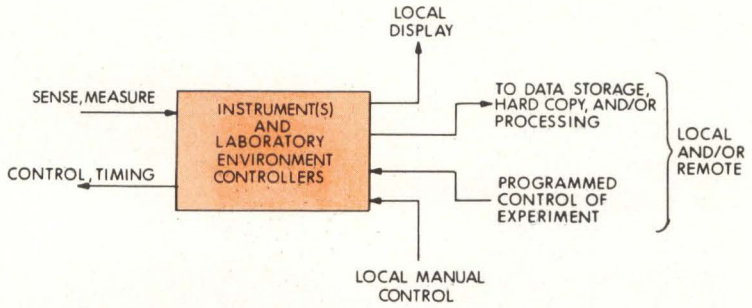

Fig 1 Functions of an instrumentation system include timing and control of experiments, data acquisition, data processing, data base management, and display and hardcopy preparation

shared among several instruments or among several experiments, or a hierarchy of computers, each performing some system functions.

Many different systems can do a given job. Aside from the obvious demands for system reliability, convenience, and acceptable cost, more subtle requirements must be satisfied.

Especially in research organizations, a wide variety of professionals with different requirements and individual tastes must be served. Some of them may want a maximum of local autonomy (eg, local files, hard copy, free-form data and command formats).

Although computer hardware is relatively inexpensive (and getting cheaper), programming is expensive. While some users must be freed from any programming and allowed to simply push buttons, others will accept (and need) higher order languages like FORTRAN or BASIC, plus file-manipulation commands. Routines or programs that require more efficient execution must be written in assembly language (or machine language) by qualified programmers. If at all possible, standard system programs (operating system, language translators, file manipulation) should be used that are supported by a viable manufacturer or systems house on a continuing basis, rather than by "homemade" software.

Some researchers will have computer programs that have already been developed for use on a specific type of micro- or minicomputer.

Hard-to-get data from critical experiments must be safe (local buffer storage or magnetic storage, safe communications with redundancy checks and retry capability).

Physical and electrical standards for interfaces between instruments and computers reduce hardware and design costs (eg, CAMAC, IEC-bus standards).

Optimum design will maximize the use of low cost mass-produced LSI (large-scale integration) chips to replace not only conventional processor and interface logic, but also to reduce the need for overly complex real-time operating systems.

To reduce maintenance problems as well as initial costs, electromechanical peripherals (disc and tape drives, printers, plotters) should be restricted to a few central locations.

Simple, standard communications links among computers, instruments, and terminals should be used as much as possible (serial links, standard communications protocols).

The system must work even when some component power supplies are shut off.

Finally, efficient laboratory automation requires a complete review of experiment design, not simply automation of existent procedures. Therefore, this discussion of instrumentation-computer hierarchies will emphasize modularity, flexibility, and expandability.

Modular Distributed-System Concept

Computer-related functions of instrumentation systems will be distributed over a hierarchy of modular laboratory computers (Fig 2). Each computer can, if desired, be made to stand alone with suitable plug-in memory and peripherals; however, it will usually be joined to the next computer in the hierarchy through a simple plug-in communication interface.

Built-in Instrument Microcomputers—Consisting of microprocessor, memory, input/output (I/O) ports, these devices will be built into individual instruments mainly to replace conventional logic. Other functions may con-

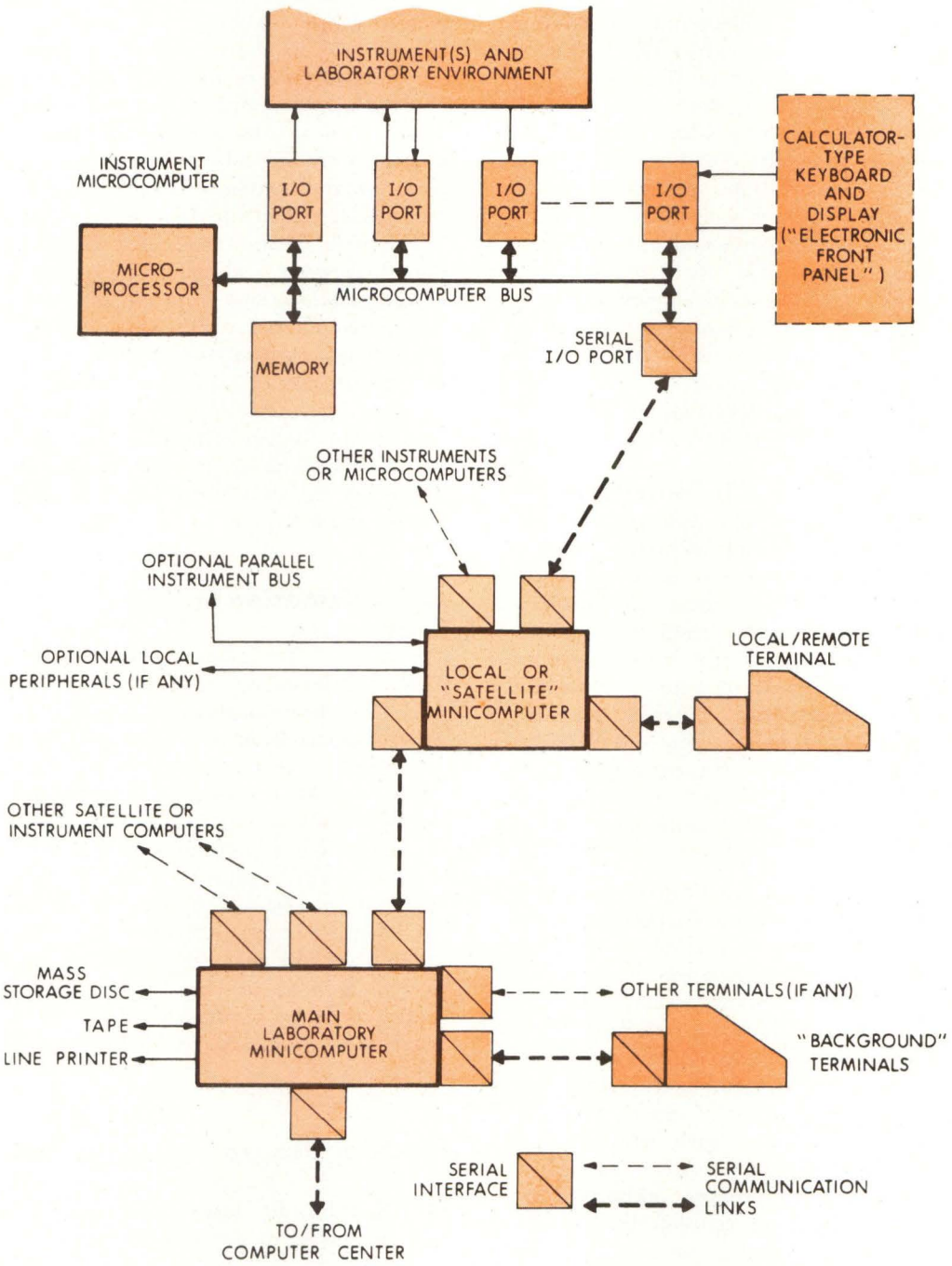

Fig 2 Laboratory computer hierarchy includes instrument microprocessors, satellite minicomputers, and a central laboratory minicomputer whose "remote operating system" can be accessed by satellite computer terminals to provide them with disc and printer services, remote program translation, and a laboratory data base. Point-to-point serial communication links shown may be replaced by a single multidrop bus as software becomes available. Each satellite can have a keyboard and television-raster CRT display for alphanumeric text, data, and simple graphics. Plug-in interface cards connect the minicomputer to rest of system, and also to optional local mass storage and hardcopy peripherals

sist of measurement control, timing, calibration, and simple data-processing operations, such as scaling, zero suppression, and scale linearization.

Typical instrument microcomputers will use 8-bit n-channel metal-oxide semiconductor (n-MOS) microprocessor chips (8080, 6800, 2650) or 16-bit n-MOS or integrated injection logic (IIL) processors (LSI-11, 9900). The slightly lower price of a 4-bit processor does not justify its extra programming (and memory) costs in most instrumentation applications. Within the instrument, instrument microprocessors will utilize the microprocessor manufacturer's I/O ports and bus hardware. Thus, a 6800-based system would use a parallel 8-bit data bus, while a 9900 system could employ its "communications-register" (CRU) I/O hardware (serial data, parallel addresses), as well as its parallel TILINE bus. It is usually best to employ mass-produced LSI chips and "programmed logic" rather than specially designed hardware. Instrument microcomputers will usually be supplied by the instrument manufacturers.

Automated instruments should be designed so that any and all communication with the instrument, including function and scale settings and calibration, is done through the instrument microcomputer via an "electronic front panel" consisting of an inexpensive calculator-type keyboard and display interfaced directly to a microprocessor I/O port. This will make the instrument more suitable for computer-supervised laboratory systems and may save much mechanical adjusting hardware. Above all, the absence of direct manual controls will ensure that all measurement conditions can be automatically recorded and documented. This feature is more important than the mere convenience of an automatic measurement procedure.

Local or "Satellite" Minicomputers—Probably also built from microcomputer (LSI) components, these units can control experiments that involve multiple instruments and can do respectable data processing. Although intended to supplement instrument microcomputers, they may also replace them, especially in research-type instrumentation. Satellite minicomputers will be standalone, general-purpose units frequently combined with cathode-ray tube (CRT)/keyboard terminals,* which may also serve as simple graphic displays. Such minicomputers can also support plug-in modular peripherals, such as local printers or floppy discs; however, initial cost and maintenance considerations favor concentration of electromechanical peripherals around a central laboratory minicomputer. Satellite minicomputers will be tabletop size and will be either checked out of a stock room or built into an experiment setup.

Local minicomputers will be low-end to medium-size members of a family that is software-compatible with the main laboratory minicomputer, if any (eg, LSI-11, PDP-11/04, 990/4, up to PDP-11/34 or 990/10).

Main Laboratory Minicomputer—The "central" minicomputer of a laboratory or research group can be time-shared among tasks associated with different experiments and communicated by their associated minicomputers or microcomputers. This "central" minicomputer can do more extensive data processing, possibly using a floating-point processor option. More important, however, is the operation of all major computer peripherals (mass storage on disc, tape, or printer with software support, program preparation, and data-base management for all the laboratory's smaller computers. The main laboratory minicomputer may also communicate with a larger computer center if extremely large data processing tasks are required or if extra peripherals are needed.

The main laboratory minicomputer will then be time-shared between real-time foreground tasks associated with communications from the smaller computers and a "background" task, such as program development or general-purpose computation. Depending on the amount of data processing needed, a top-end, medium, or even a small minicomputer that is software-compatible with the satellite computers may be used. In the future, various tasks will again be distributed over two or three processors, eg, data processor, task scheduler/communications processor, and I/O processor.

Communication Between Processors

Most instrumentation-system communications (mainly data from instruments to computers and mass storage, and programs from main computer to satellites and instrument microcomputers) can be accommodated with 2400- to 9600-bit/s asynchronous serial links, which use simple twisted-pair or coaxial lines and inexpensive LSI interfaces. While "multidrop" serial links, including loop systems, slightly reduce the number of interfaces needed, standard interfaces and software are not yet generally available. Point-to-point serial links (two interfaces per individual link) that can be flexibly added or replaced by synchronous or parallel data links as needed for higher speed are recommended. Above all, standard communications protocols, redundancy checks, and software exist.

Modular Programming System

Our distributed-computer system will be designed so that each level or any two levels of the computer hier-

*Some users prefer teleprinters to CRT terminals, because, in addition to the local hard copy of their data, the device provides printed-out commands which serve as a primitive record of past operations. However, local teleprinters must be supplied with paper and inked ribbons and break down much more often than CRT terminals. With a good overall system design, complete experiment records can be kept automatically on a tape or disc, to be displayed and/or printed out on demand. If a local printer is needed, it is best to provide a small keyboardless matrix printer as a movable plug-in accessory for CRT/keyboard terminals.

archy can, if desired, also stand alone and implement suitably restricted laboratory-automation functions. This modularity is also expressed by a flexible programming system, which supports a variety of computer languages, language translators, utility programs, and a file manipulation system together with intercomputer communications.

Built-in Instrument Microcomputers—In their simplest form, these devices only read read-only memory (ROM) programmed by the manufacturer to support simple front-panel operations (eg, scale setting, calibration, and function and scale switching) selected through the calculator-type keyboard/display. The same functions can, however, also be called by simple ASCII-code commands through a serial communications link that is connected to a CRT terminal or minicomputer. Data can be similarly output as ASCII-character sequences, which can comprise file identification characters.

The next higher programming level employs either similar "canned" instrument commands, user-written machine language, or block-diagram language.** This is either keyboard- or computer-entered with the aid of a ROM-implemented monitor program.

Note that, up to now, the instrument microcomputer appears to any higher up member of the hierarchy simply as another teleprinter-like terminal, which accepts and transmits ASCII character strings through a simple serial interface. Such communications are best restricted to simple programs and slow data rates, but they can be supported easily in any desired computer language.

For more sophisticated programs, the instrument microcomputer must execute assembly-language, block-diagram, PL/M, or FORTRAN programs translated and downloaded by a higher-up computer. An alternative is to use a BASIC interpreter either in the microcomputer (ROM-resident or down loaded) or in the higher-up computer (multi-user BASIC). At this point, the instrument microcomputer's functions become exactly those envisaged for the local minicomputer, and a software-compatible member of a 16-bit computer family (eg, LSI-11) would be used.

Local or Satellite Minicomputer—This unit is likely to be the workhorse of the computer hierarchy, especially in research-type installations. To permit interactive experiment control and reprogramming for such installations, programming ought to be done in interpreted BASIC whenever execution speed permits. BASIC is easily learned, supports graphic displays, and permits interactive editing and file manipulation; simple versions do not need a disc. To speed execution and to accommodate new I/O interfaces, "extended" BASIC can call assembly language subroutines written by expert programmers. One such system (MICRODARE[1]) permits the user to call complete block diagram-language subprograms which can operate instruments and perform digital filtering, function generation, and statistical operations at assembly language speed. The extended-BASIC interpreter can again be ROM-canned, downloaded, or loaded from a plug-in mass storage device. Typical memory requirements vary between 8k and 16k 16-bit words.

With an extended-BASIC interpreter, a keyboard, and a TV-raster display for alphanumerics and simple graphics, the local minicomputer can be used as a very powerful scientific calculator, which can control instruments (with or without instrument microcomputers) through efficient block-diagram language routines. However, local/satellite minicomputers can also execute FORTRAN and assembly language programs, including file operations and other programmed operating system requests. Such programs will normally be edited, translated, and linked on the main laboratory minicomputer, using either the main computer or a satellite terminal. Object programs are then downloaded in response to requests from satellite terminals or from programs currently running in a satellite. Similar typed or programmed requests move data to the main computer, which has suitable mass storage and other peripherals.

Main Laboratory Minicomputer—This system has a real-time disc operating system incorporating "remote software" for remote (satellite-actuated) file manipulation, program translation, and downloading. This allows each remote terminal and/or minicomputer to access the main computer's operating system and peripherals like its own.

In addition, the main minicomputer can handle program preparation, listing, copying, or batch data processing as a background task which is interrupted by real-time demands. The complexity of the operating system is related to its responsiveness to simultaneous satellite requests. If at all possible, a standard system supported on a continuing basis by a viable computer manufacturer or software house should be utilized.

Data and File Formats and Data Base Management

Instrumentation system data formats handled by communication links and file manipulation programs include the usual 16-bit signed integers, 32-bit floating-point numbers, and ASCII character bytes† employed by BASIC

**Block-diagram languages implement an analog computer-like block diagram by calling successive block-operator macros or subroutines (eg, addition, multiplication, analog-digital conversion) which have been written previously by an expert programmer. Such languages produce very efficient code without any need to learn assembly language. ROM-canned block-operator subroutines (or microprograms) are especially suitable for microcomputer programming. Such programming systems are described in detail in Ref 1.

†Again recall that a BASIC or FORTRAN program can communicate with sufficiently slow instruments or instrument microcomputers entirely in terms of ASCII character strings, ie, exactly as if the instrument or microcomputer were a teleprinter; simple ASCII command strings may call ROM-canned instrument microcomputer routines. Operation of graphic terminals is a good example. Transmission of instrument data through ASCII strings, however, is not very efficient because of the conversion routine overhead.

and FORTRAN. It is desirable to add 16-bit signed fractions (between −1 and +1), which are ideal for representing scaled analog data in assembly language and block diagram programs.[1,2] Double precision data, needed to reduce roundoff errors in integration and averaging operations, typically occur only within a computer program. Finally, instrument microcomputers and interface logic may require plain binary (or hexadecimal) command words.

Instrumentation data must be formatted into retrievable files identified by codes for experimenter, program, data, and run number. These files will comprise numbers (eg, scale settings, ambient temperature), arrays of numbers (eg, time histories, spectra), and, if possible, plain language comments for future reference and report generation. It is vital that file formats be easily accessed by computer programs and, in particular, by standard BASIC and FORTRAN programs. This fact alone determines the preferred file format for an instrumentation system. Similarly, retrieval of an experimenter's files from mass storage (typically on a disc or tape associated with the main laboratory minicomputer) ought to employ the file name, extension, user number, date, and file-protection conventions of a standard minicomputer operating system. It will then be possible to retrieve all files complied on a certain date or by a certain user or project in one operation. Unfortunately some current BASIC file designations identify files only by a logical-unit number; the same is true for many FORTRAN systems.

Software Requirements

A complete instrumentation system with instrument-level micro/minicomputers (satellites), local keyboard terminals, and a central laboratory minicomputer will require system software. Typically this will comprise

Real-Time Disc Operating System for Main Laboratory Minicomputer—A foreground/background system will permit simultaneous instrument operation and program preparation; a true multitask system will also provide memory protection for different users' I/O buffers. The distributed multiprocessor system will, however, tend to simplify operating system tasks.

"Remote Software" for Satellite Computers—Program downloading, remote operation of peripherals and file manipulation programs, remote editing, debugging, and program preparation functions are desirable. All this requires communications routines with redundancy checks and retry capability.

Macroassembler—This can also be used for cross-assembly of microprocessor code.

Higher Order Language Translation and Loading For Satellite Programs—Cross-translation on the central minicomputer is satisfactory. Desirable languages are FORTRAN with reentrant real-time procedures and file manipulation capability; BASIC with real-time procedures, file manipulation capability, and optional double-precision operations (needed for averaging, integration); and block-diagram language or other macro language, with runtime and graphics package (eg, DARE, MICRODARE). This is especially efficient for satellite microprocessors.[1]

Summary

The proposed laboratory-automation scheme distributes the computer functions of an instrumentation system over three levels of micro/minicomputers. Built-in instrument microcomputers replace conventional logic, do simple data processing and control, and permit replacement of manual controls with computer-documented control through a calculator-type "electronic front panel." Local or "satellite" micro/minicomputers can control multiple experiments and do respectable data processing, but do not usually need expensive peripheral or mass storage. These are supplied by a central laboratory minicomputer via remote computer access to its operating system (remote software). Most intercomputer communications are handled through simple serial links, although parallel links can be accommodated. The entire system is modular, and any level in the hierarchy may be omitted in simpler systems. A modular programming system, permitting such modular operation with a variety of programming languages, and a simple data base management system, are described. All hardware and software components of the proposed system currently exist; on-going LSI developments will reduce hardware costs further.

Acknowledgements

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Granino A. Korn received the BA degree from Brown University, the MS from Columbia University, and the PhD degree from Brown University. A professor of electrical engineering at the University of Arizona, his interest is research on digital computation and on random-process simulation and measurements. He is currently on leave to the Max-Planck Institute.

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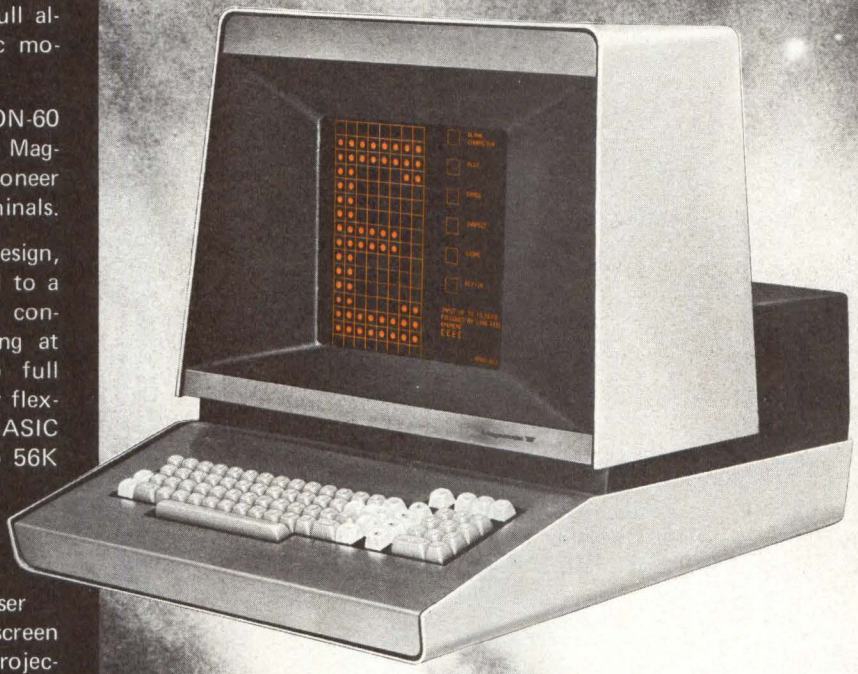

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In agricultural applications, a major requirement in achieving optimum crop yields is the accurate spacing of seeds during sowing. Utilization of a seeder controlled by a microcomputer could fulfill this requisite, and greatly improve the reliability of today's mechanically-controlled seeders.

A conventional seeder consists of anywhere from one to 12 seed distribution units (one unit per row of crops). Each unit has a bucket shaped container for the seeds. At the bottom of the container is a toothed disc which rotates proportionally to the forward speed of the seeder. The space between the teeth of the disc is large enough for a single seed. At one point below the toothed edge of the disc is a hole. Rotation of the disc moves the seeds trapped between the teeth of the disc. As the seeds pass over the hole, they fall through it to the ground (Fig 1).

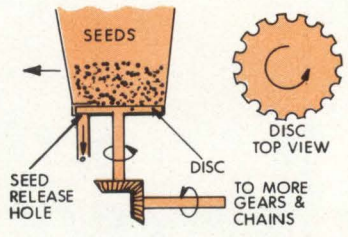
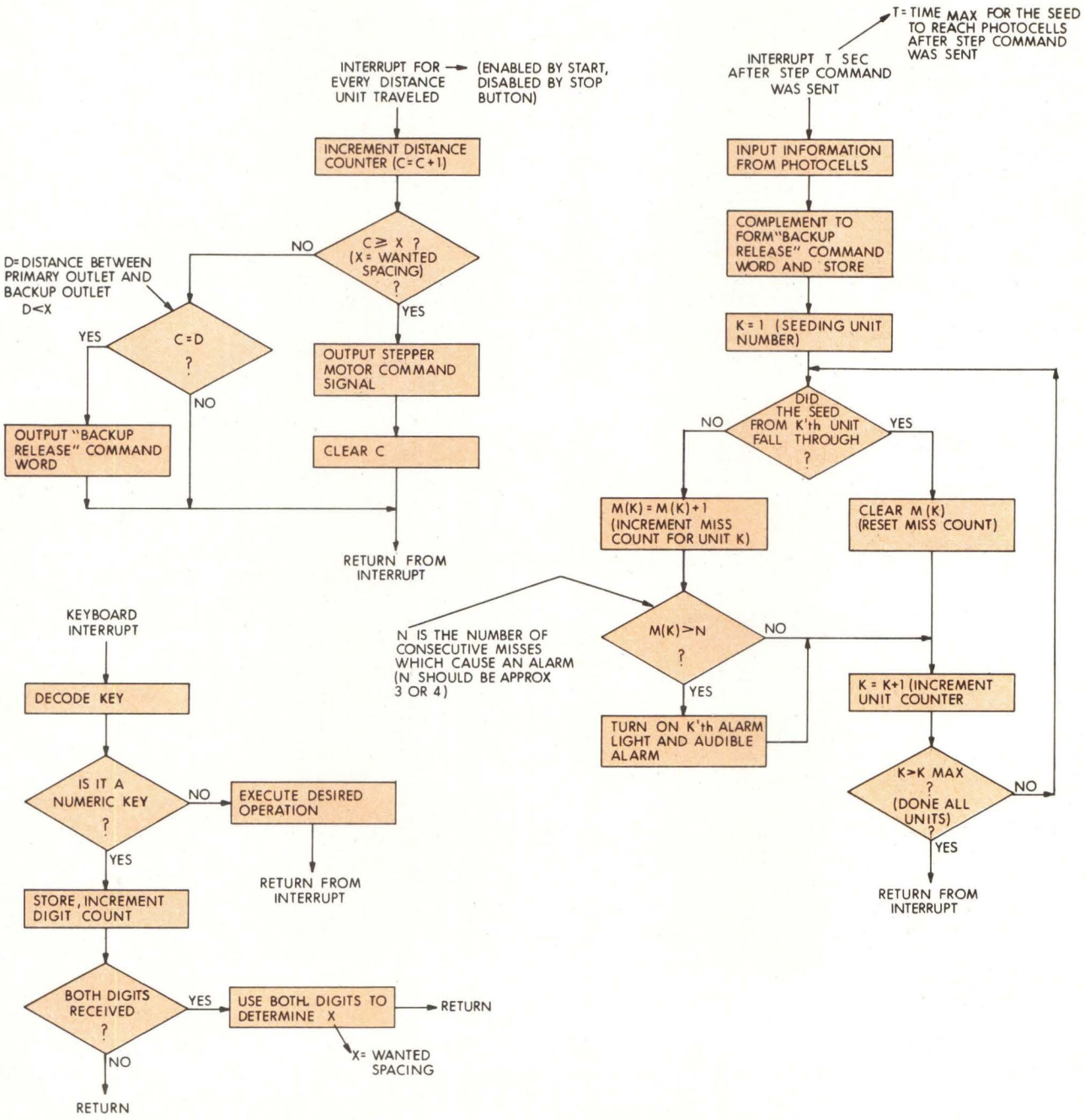


Fig 1 Conventional seeding units contain own chains and gears. Seeds are released through teeth on disc; to alter spacing between seeds, a gear must be changed

Flowchart


INTERRUPT FOR EVERY DISTANCE UNIT TRAVELED
(ENABLED BY START, DISABLED BY STOP BUTTON)
INCREMENT DISTANCE COUNTER (C=C+1)
C ≥ X ? (X = WANTED SPACING) ?
NO
YES
D=DISTANCE BETWEEN PRIMARY OUTLET AND BACKUP OUTLET D<X
C=D ?
YES
NO
OUTPUT "BACKUP RELEASE" COMMAND WORD
OUTPUT STEPPER MOTOR COMMAND SIGNAL
CLEAR C
RETURN FROM INTERRUPT
T = TIME MAX FOR THE SEED TO REACH PHOTOCELLS AFTER STEP COMMAND WAS SENT
INTERRUPT T SEC AFTER STEP COMMAND WAS SENT
INPUT INFORMATION FROM PHOTOCELLS
COMPLEMENT TO FORM "BACKUP RELEASE" COMMAND WORD AND STORE
K = 1 (SEEDING UNIT NUMBER)
DID THE SEED FROM K'th UNIT FALL THROUGH ?
NO
YES
M(K) = M(K) + 1 (INCREMENT MISS COUNT FOR UNIT K)
CLEAR M(K) (RESET MISS COUNT)
N IS THE NUMBER OF CONSECUTIVE MISSES WHICH CAUSE AN ALARM (N SHOULD BE APPROX 3 OR 4)
M(K)>N ?
NO
YES
TURN ON K'th ALARM LIGHT AND AUDIBLE ALARM
K = K+1 (INCREMENT UNIT COUNTER
K>K MAX ? (DONE ALL UNITS) ?
NO
YES
RETURN FROM INTERRUPT
KEYBOARD INTERRUPT
DECODE KEY
IS IT A NUMERIC KEY ?
NO
YES
EXECUTE DESIRED OPERATION
RETURN FROM INTERRUPT
STORE, INCREMENT DIGIT COUNT
BOTH DIGITS RECEIVED ?
YES
NO
USE BOTH DIGITS TO DETERMINE X
RETURN
X= WANTED SPACING
RETURN

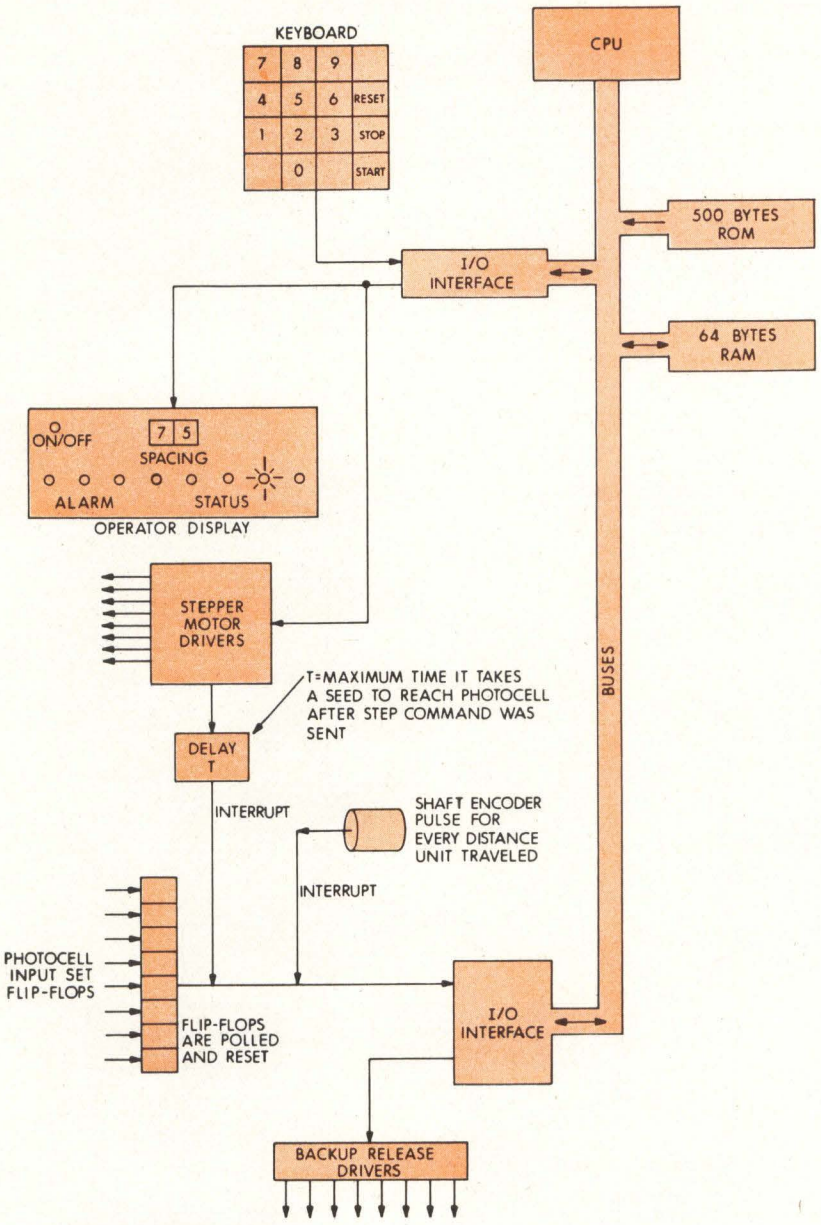


Fig 2 Block diagram of microcomputer-controlled seeder illustrates components and operations involved in determining spacing and release of seeds, as well as backup seeds if miss should occur

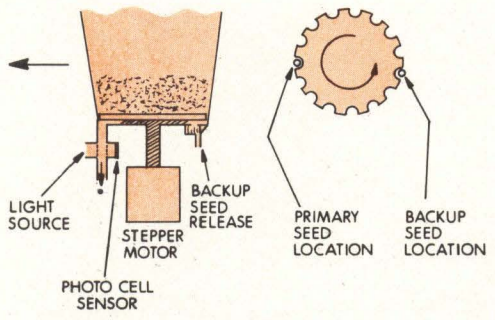


Fig 3 Microcomputer-controlled seeder operates with stepper motor. Photocell senses seeds, enabling release of backup seed if there is a miss

To change spacing between the seeds on these seeders, the farmer must remove one gear and replace it with another, on every seeding unit. Each unit also has its own chain.

The seeder is pulled by a tractor, necessitating a tractor driver plus at least one other observer to monitor the seeder. This person ensures that none of the holes become plugged and that none of the chains fall off.

A microcomputer-controlled seeder would have the following features: an operator keyboard with numerical display, stepper motor driven seeding units, photocell monitoring of primary seed outlets, and backup seed outlets. It would be controlled by an 8-bit microprocessor, containing 500 bytes of ROM and 64 bytes of static RAM.

The operator would set the desired spacing between seeds via a keyboard. The distance, X, is measured in units of inches or centimeters. The value X is displayed on a 2-digit numerical display (Fig 2). After the Start button is pressed, the controller begins monitoring the distance traveled. Every X distance units, the stepper motors are rotated one step angle, moving the seeds to the seed release holes, where they fall through the outlet tubes (Fig 3) and are sensed by the photocells. Pulses from the photocells set flip-flops. The microcomputer reads in the outputs of the flip-flops and resets them in the process.

As the Flowchart indicates, the input word is used to determine to which units to send backup seed release commands. Consecutive misses by the primary seed release are counted. If the count reaches N (N is approximately three or four), the controller sounds an audible alarm, and lights an alarm status LED corresponding to the guilty seeding unit. The backup release hole can be opened when it is exactly over the spot where the seed from the primary outlet should have fallen. The backup seed release fills incidental misses from the primary outlet.

Requiring only one operator, the microcomputer seeder offers the advantages of greater reliability and accuracy, with a reduction in the number of moving parts. A problem area to be taken into consideration is use of the device under very rough environmental conditions including vibrations, temperature, and electrical noise. □

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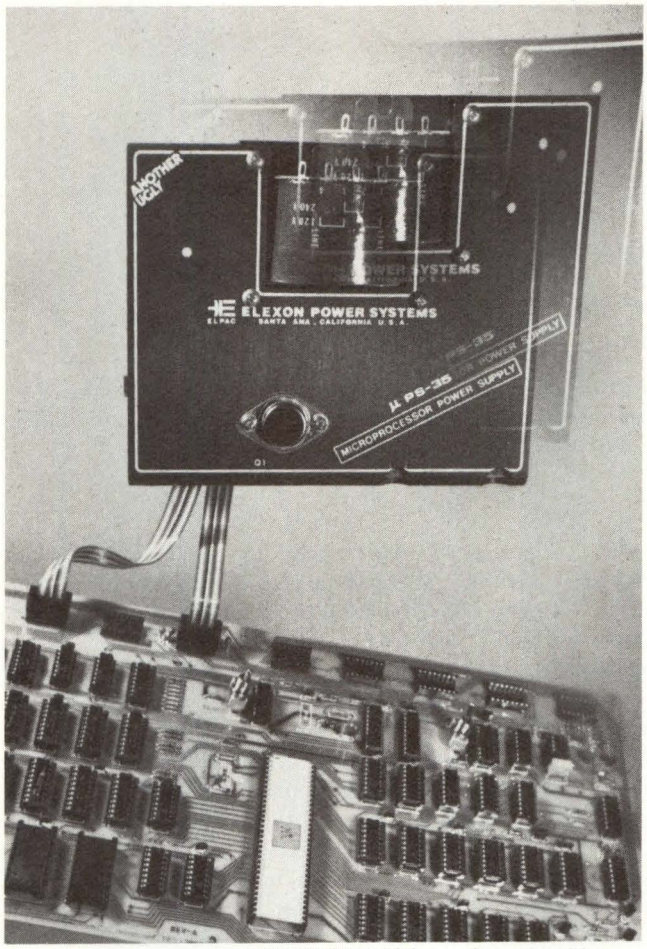

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TECH NOTE

Understanding Logic Analyzers

Robert L. Down

Tektronix, Incorporated
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The evolution of logic analyzers has brought with it the need for defining associated terminology, basic concepts, and differing capabilities for both the novice and veteran user

To meet the complex digital development and service requirements of the microprocessor and microcomputer design engineer, and to complement the traditional oscilloscope, logic analyzers have evolved as important test instruments with increasing capability, versatility, and applicability. These instruments do for the analysis of complex digital equipment what the oscilloscope has long done for real-time signal analysis by providing views of multiple channels of sequential data even if the data are nonrecurring, providing true simultaneous acquisition of multiple data channels, and providing data sequence displays that occur *before* a trigger.

Logic analyzers are described by terms which either are new or take on special meaning when applied to these instruments. Beginning logic analyzer users can obtain from this note a basic understanding of what the terms mean, what the instruments are, and what they can do. For experienced logic analyzer users, a clearer understanding of the capability differences among various models will be gained.

What is a Logic Analyzer?

Basically, the logic analyzer is an instrument for acquiring and displaying information from the digital domain, as opposed to the familiar time domain of real-time oscilloscopes or the frequency domain of spectrum analyzers. Digital domain information consists of data (ones and zeros or high and low states) simultaneously present on a parallel set of signal lines, the sequence of changing data on each of the lines, the timing of sequential data changes, and the clock and other control signals used to govern the processing and flow of data in a digital machine. At any given time, a single channel of digital domain information can, of course, take on only one of two values rather than the continuous range of values available in analog information.

Note that the logic analyzer does not actually analyze data. Rather, it displays machine data in a convenient form for analysis by the operator. Some models do, however, have an output port for stored data. This permits the possibility of data transfer to a computer for automated analysis.

Devices as simple as the familiar logic probe are often thought of as tools for performing logic analysis. The term logic analyzer has, however, come to mean a more sophisticated instrument which generally includes multiple data channels, memory, trigger, and display.

Multichannel probes enable logic analyzers to look simultaneously at parallel data words ranging from four to 16 bits, or even up to 32, as opposed to the one to four channels (not usually acquired simultaneously) which are commonly associated with an oscilloscope. A logic analyzer stores parallel data acquired *on a single pass* so that they can be dis-

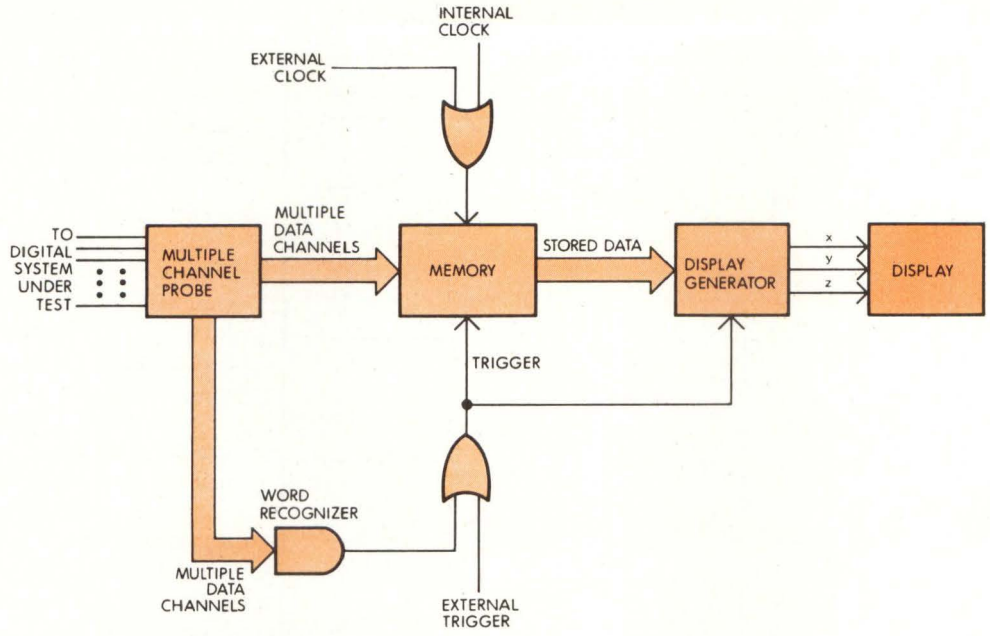

Fig 1 Simplified block diagram of typical logic analyzer

played indefinitely. In present logic analyzers there is sufficient memory capacity to store from 16 to several thousand bits of sequential data for each acquired channel. Memory allows the logic analyzer to capture and display a nonrepetitive sequence of parallel data for analysis at leisure and to provide a display of sequential data preceding the trigger. The trigger is the logic pulse or transition that initiates stable display of data stored in memory during an operator-selected time period or "window." In an analyzer, a trigger stops the acquisition of data and initiates a display of data stored at that time.

Display medium (normally a CRT) presents stored data to the operator. In some logic analyzers it is built-in, while in others it can be any available oscilloscope or CRT monitor with X-Y inputs.

How It Works

A simplified block diagram of a typical logic analyzer is shown in Fig 1. Parallel data from the system under test are acquired via a multiple channel probe, and are written into a random-access memory* (RAM) under control of a clock from the system under test or internal to the logic analyzer. As long as there is no trigger, sequential data continue to be clocked into memory; when memory is full, the first data written in are overwritten by new data. Thus, the logic analyzer memory stores a constantly changing time slice or window of sequential digital information. The "Display Generator" block in Fig 1 converts stored data and control information into signals necessary to produce displays.

Data Acquisition

From four up to 32 data channels are acquired simultaneously by a logic analyzer. While this can be done with single-channel probes, it is generally less confusing to the user if as many channels as practical are combined in a single multiple lead probe (a short set of color-coded leads from the probe head). It is important that both dc and ac loading of the logic circuits under test be minimized. High dc input impedance is achieved in most quality probes on the market. The best probes for high speed logic analyzers minimize capacitive loading by using active electronic probes.

Most logic analyzers convert incoming analog pulses to ones and zeros by using a single voltage threshold. This threshold must be operator-selectable to match the threshold of the logic family under test. Some logic analyzers employ dual thresholds (set to the minimum high state and maximum low state levels of the logic family under test) to detect and store data imperfections due to low amplitude glitches, pulse ringing, or slow transitions. A possible drawback of the latter technique is that the logic analyzer display may reproduce low amplitude glitches which the logic under test did not actually see. Sequential data entering the logic analyzer are constantly changing. To determine what logic state is to be stored in each bit of memory, incoming data are sampled at periodic intervals using a clock.

If the sampling clock is taken from the system under test, sampling is said to be synchronous. The logic

*Memory of a logic analyzer acts, in effect, as a shift register with multiple parallel channels. For reasons of economy and design efficiency, however, nearly all available models use random-access IC memories.

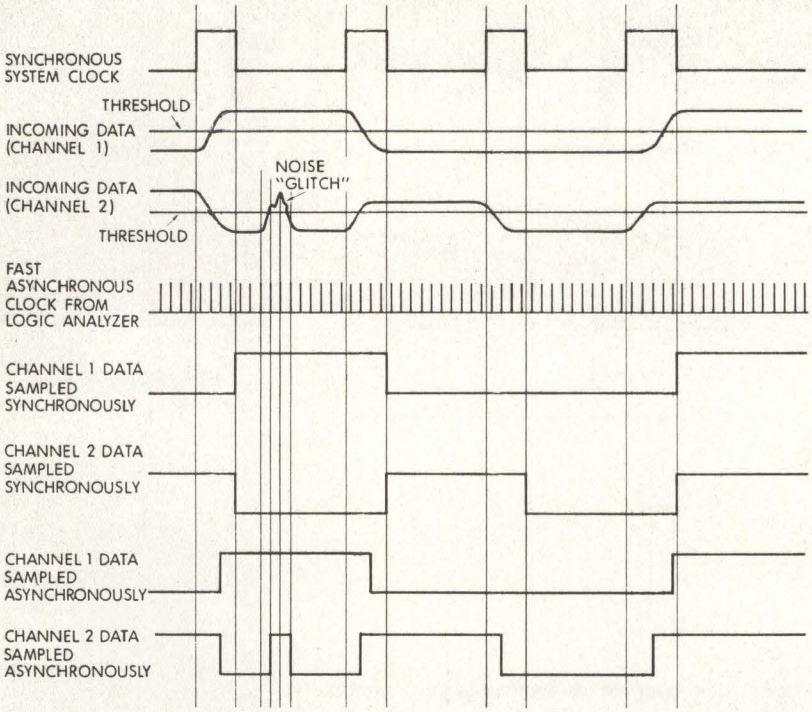

Fig 2 Data input to logic analyzer can be synchronously sampled by system clock or asynchronously sampled by fast clock from analyzer itself. Using first technique, state information is stored and displayed; second technique adds timing information to stored data. Note, for instance, that asynchronously sampled data clearly show that last transition on channel 2 occurs before last transition on channel 1. Also, noise glitch on channel 2 is recorded

analyzer stores (and ultimately displays) state changes only at the time of the system clock. Content of the stored and displayed data is that of a system state table, regardless of whether the displayed data are an actual table of ones and zeros or a reconstructed waveform showing a sequence of high and low states.

To store timing as well as state information, the incoming data are sampled by an asynchronous clock generated by the logic analyzer and unrelated to the system clock. Normally, the asynchronous clock is run much faster than the system clock, so that timing of the data (pulse widths, delays between channels, glitches, etc) can be studied in detail. In fact, timing resolution (minimum detectable time between state transitions) of the logic analyzer is equal to the sampling interval plus the finite setup time required to detect and store a new logic state. Thus, a logic timing analyzer with a 100-MHz asynchronous clock (10-ns sample interval) and a 5-ns setup time has a timing resolution of 15 ns. Fig 2 shows reconstructed ladder diagram displays for an incoming data channel as sampled by both synchronous and fast asynchronous clocks.

Storage

Most available logic analyzers accomplish the storage function with solid-state RAMs. Since the trigger does not have to precede the events to be viewed, another valuable capability of the analyzer is that a logic fault condition can be used to trigger a display of events which led up to it (see Fig 3).

For added versatility, delay counters are built into logic analyzers to allow selection of displays of events before (pre-trigger), after (post-trigger), or centered around (center-trigger) the trigger event. For optimum usage, a logic analyzer must be capable not only of acquiring multiple data channels, but also of storing a large number of sequential data bits for each channel, enabling thorough examination of complex logic problems.

Storage format refers to the division of memory capacity into a certain number of channels with a certain number of sequential bits for each channel. A 256-bit memory could be formatted as 16 channels with 16 bits/channel or as eight channels with 32 bits/channel. Some logic analysis applications are better served by one format than by another. Transfer of serial data (plus a few control channels) between instruments can best be examined using a format having perhaps four channels with 1024 bits/channel. For a parallel data transfer, the same 4096 bits would better be formatted as 16 channels with 256 bits/channel. Some logic analyzers offer front panel selection of storage formats.

Triggering

A useful form of triggering, called word recognition, is almost always included in current logic analyzers. Word recognizers produce a trigger by comparing incoming data words against a specific word (a known error condition or an instruction word for instance) preset by the operator. Whenever there is a match, a trigger is produced.

Some logic analyzers provide trigger delay by a number of digital events selected by the operator. Another feature sometimes included is a qualifier. This is an additional condition (clock pulse high, for instance) which must be met simultaneously with a recognized word before a trigger can be generated. The qualifier can also be used to gate the sampling clock, and hence give the operator control of the data to be stored in memory.

Display

Stored data can be presented to the operator in the form of a logic state table, a logic timing diagram, or a "map" of the logic words stored. Typical displays are shown in Fig 4. The state table, as its name implies, is a table of states present for a set of parallel channels at each of a sequence of clock times. Binary, octal, or hexadecimal notation may be employed in the display. Many logic analyzers offer the ability to

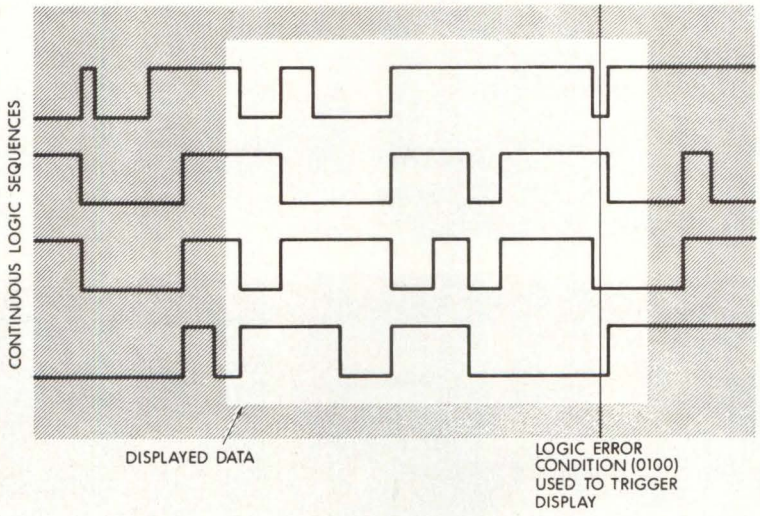

Fig 3 Because data are stored by logic analyzer, it is easy to stop data recording by triggering on an error condition and then displaying data that preceded trigger

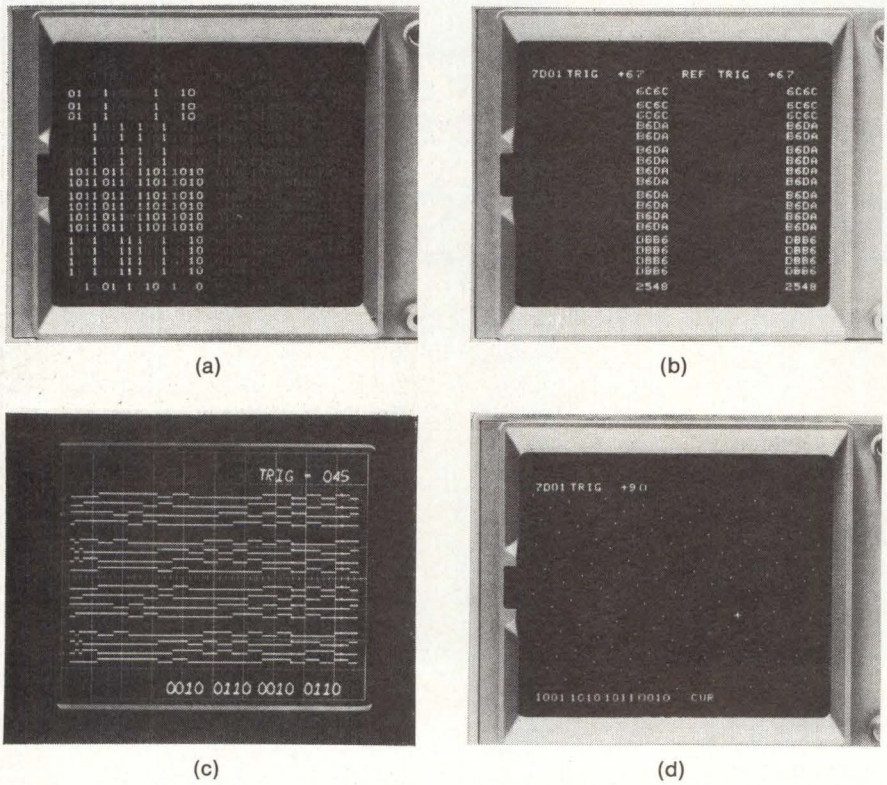

Fig 4 Various logic analyzer displays. State table display (a) in binary format contains two tables of 16 parallel words of 16 sequential bits each; same table is also displayed in hexadecimal notation (b). Timing diagram (c) shows sequence of state changes on 16 parallel channels; logic mapping display (d) provides unique "signature" for specified block of stored data

display simultaneously two state tables (sampled at two occurrences of the trigger) and compare them, showing differences between the two as intensified characters [see Fig 4(a)]. Additional words at the top and bottom of the table represent the position of a movable display cursor and the parallel logic word on which the display is triggered. In Fig 4(b), a state table is displayed in hexadecimal notation.

In the timing diagram display, parallel channels are displayed as reconstructions of real-time waveforms. For the reconstruction to truly approximate the time sequence of state changes in the original data, the data must be sampled by a clock faster than the clock of the system under test. This is usually done with a fast asynchronous clock built into the logic analyzer. Timing diagram displays, in addition to yielding time information, are typically used to display longer sequences of data than those contained in a state table display. Note that timing diagram displays, such as the one in Fig 4(c) are capable of portraying state as well as timing information, although the operator must translate the high and low states at a given time into ones and zeros.

Map displays, such as the one shown in Fig 4(d), portray each stored logic word as a separate dot. Vertical position of the dot is proportional to the most significant half of the word. Horizontal position is proportional to the least significant half. The combination of dots for a given sequence of data words forms a signature that is unique for that data block. With practice, the user can utilize the map for an overview of a data sequence without performing a detailed analysis. It enables fast detection of logic errors whose precise source can then be determined using state and timing display modes. Movable cursors and sometimes on-screen binary, octal, or hexadecimal readout of selected words help in interpreting maps. Photographic records of maps for known good and bad versions of the data sequence also assist in quickly locating error conditions.

State, timing, and map displays each have applications where they are the most appropriate portrayals. The most versatile logic analyzers, however, offer operator selection of all three. □

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TECH NOTE

A Task-Scheduling Executive Program for Microcomputer Systems

David A. Townzen

Kaye Instruments, Incorporated
Bedford, Massachusetts

A task-scheduling program allows a high performance microcomputer to execute concurrently up to eight levels of software priority in a real-time operating system

If a microcomputer is designed for real-time processing and control, it is often desirable to have it perform many software tasks at the same time. Since the CPU can execute only one task at any given time, the classic dilemma of scheduling CPU time must be resolved by the microcomputer system designer. In minicomputers and in larger machine systems, this task-scheduling function is achieved by the executive portion of a real-time operating system. A task-scheduling executive program, developed for a microcomputer based on the Intel 8080 CPU, allows tasks on eight levels of software priority to be executed concurrently by the CPU, and offers many of the features of a minicomputer real-time operating system.

Multitask System

This microcomputer system demonstrates the usefulness of such a task-scheduling program. The microcomputer is used as the control center of a data-logging system with remote scanning digital voltmeters communi-

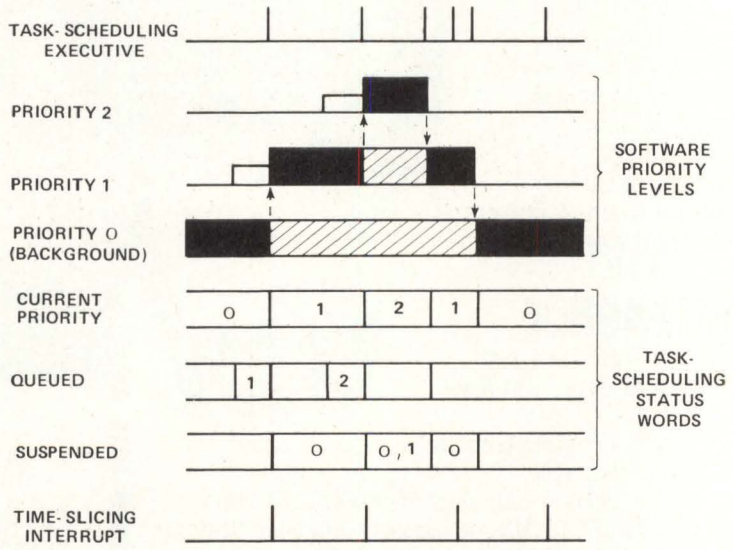

Fig 1 Task-scheduling executive program shares control of CPU among three priority levels. Execution of task is indicated by solid black, suspended task is indicated by shading, and queued task is indicated by line at middle height. Time-slicing interrupt enables queued tasks of higher priority than current priority to take control of CPU. When high priority task is completed, control of CPU falls to lower priority task. For simplicity, the diagram does not show that priority 0 (background) always has task queued

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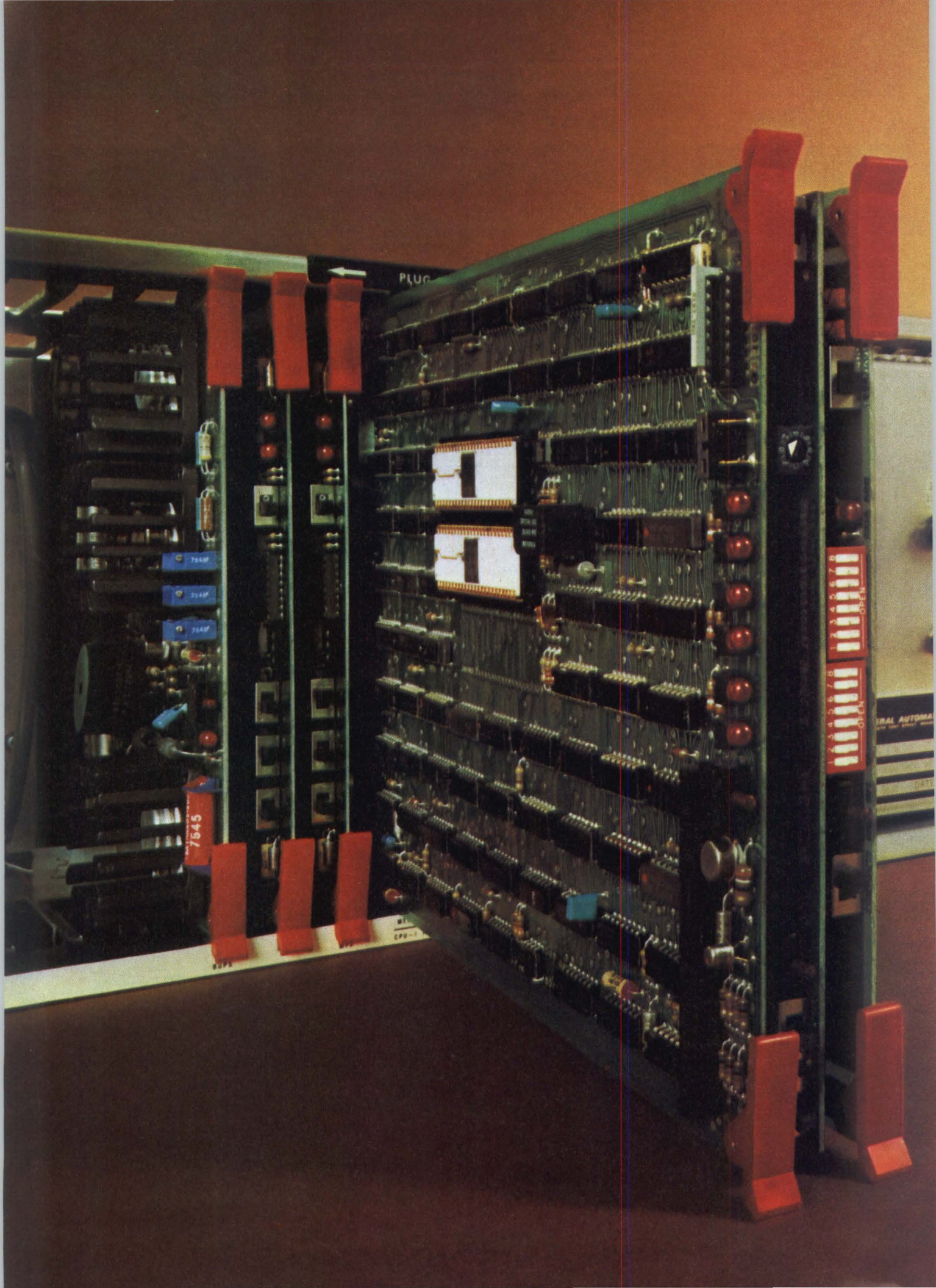
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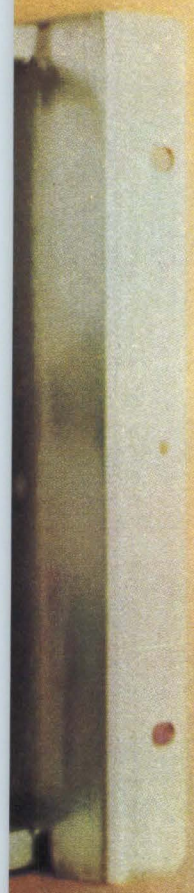

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cating via serial data lines. Each scanner asynchronously sends messages with the channel numbers and voltage measurements made by the digital voltmeters. The microcomputer receives data from the scanners, converts the measurements from voltages to engineering units (temperature, pressure, etc), compares them with preset threshold values, displays the measurements on a front panel, and logs the data on a printer at periodic intervals.

In this context, a "task" is a program to be executed by the CPU to perform a function. Each task has a definite beginning and end. For instance, the data conversion task takes "raw" data from a scanner, performs the required linearization to obtain the engineering units, and stores the processed data in memory.

Some tasks require immediate execution by the CPU, such as a data character received from a scanner which must be read by the CPU before the next data character is received. Such tasks are handled most conveniently as interrupt-driven routines. However, many tasks do not require such immediate use of the CPU, but do require the ability to take CPU time from lower priority tasks. For example, the data conversion task has higher priority than the front panel display task, so the former must be allowed to take CPU time from the latter.

A task is "active" if the CPU has executed the beginning of it but has not reached the end. A task is "suspended" if another task has taken use of the CPU while the first task is active. A task is "queued" if its beginning has not been executed by the CPU, but is due to be executed as soon as the CPU becomes available.

Fig 1 illustrates three tasks being executed concurrently by the CPU. The task-scheduling program is triggered by the "time-slicing" interrupt and also by the end of each task. A task must be queued before it can be made active by the task-scheduling program.

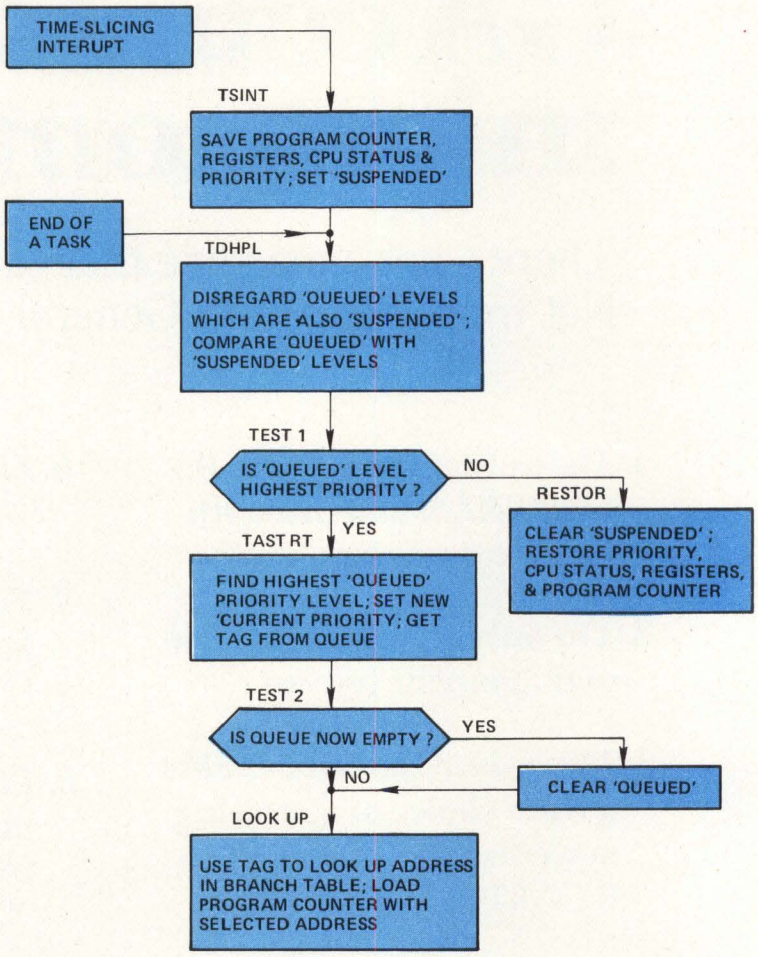


Fig 2 Flowchart of decisions and processing performed by task-scheduling executive program. Labels appearing above boxes correspond to labels in the source listing (see Fig 3)

Task-Scheduling Executive

Since the data word length of the 8080 microprocessor is eight bits,[1] the task-scheduling executive program is designed to allow up to eight levels of software priority. Each priority level may have more than one task assigned to it; therefore, a buffer (queue) is provided for each level. The size of each queue is sufficient to allow all possible tasks on a given priority level to be queued at the same time.

Queues operate in a first-in, first-out (FIFO) manner. When a task is to be made active, a symbolic reference (tag) is loaded into the queue, and the task-scheduling program is notified that a task has been queued. The tag is used by the task-scheduling program to look up the address of the beginning of the task.

The time-slicing interrupt causes the program counter, register contents, and CPU status to be loaded onto the "stack,"[1] corresponding to the point in the task where the interrupt occurred. Also, the priority level of the task is stored on the stack, and the task is recorded as being suspended. The task-scheduling program then determines the highest priority level that is either queued or suspended. If the highest priority level is suspended, the task-scheduling program clears the "suspended" record; restores the priority level, program counter, registers, and CPU status from the stack; and resumes the suspended task. If the highest priority level is queued, the tag is taken from the queue and the priority level of the new task is recorded; then, the task corresponding to the tag is started. If the highest priority level has both queued and suspended tasks, the queued task is ignored, and the suspended task is resumed. At the end of a task, the task-scheduling program again searches for the highest priority level

that is either queued or suspended, making the same decisions as for the time-slicing interrupt.

Lowest priority level is the "background," which is occupied by tasks that have the least critical time constraints. The background is always queued—that is, when one task has ended, another task must be started. The background task-scheduling program is therefore a special case, and must be tailored to suit the particular application of the microcomputer system. In some cases, a simple "chain" of tasks may be sufficient; in other cases, a queue may be required as well. A flowchart of the task-scheduling decision process is shown in Fig 2.

Implementation Details

The task-scheduling executive program has three status words which are used to determine how tasks are to be scheduled. The current priority status word (TCURP) represents the priority level of the task that is currently active; each bit represents a priority level, with bit 7 (most significant bit) as the highest priority level. The suspended status word (TSUSP) represents priority levels of any tasks that are currently suspended; the bit relationship is the same as for TCURP. The queued status word (TQUED) represents priority levels that have tasks queued and ready to be activated; the bit relationship is the same as for TCURP.

Each queue consists of an input pointer, output pointer, and data storage area. The input pointer is used by a program to load a tag into the queue; the output pointer is used by the task-scheduling program to take a tag from the queue. Pointers are incremented each time a tag is loaded into or taken from the queue; the queue is considered empty when the pointers are equal. In order to have the pointers "wrap around" the data storage area, the size of the data storage area is constrained to a power of 2; a mask $(2^N - 1)$ is ANDed with the pointers after they are incremented, which guarantees that they will stay within the proper range of values. All queues have the same size data storage area for simplicity.

The procedure for loading a tag into a queue is as follows. The queue input pointer is incremented, masked, and then added to the start address of the data storage area. Using the resulting address, the tag is loaded into the selected data storage location, and the corresponding bit in TQUED is set to "1" to notify the task-scheduling program that a task has been queued on that priority level.

When the task-scheduling program takes the tag from the queue, it increments the queue output pointer, masks it, adds it to the start address of the data storage area, and reads the tag from the selected data storage location. If the queue input and output pointers are equal, the corresponding bit in TQUED is set to "0" to indicate that no additional tasks are queued on that priority level.

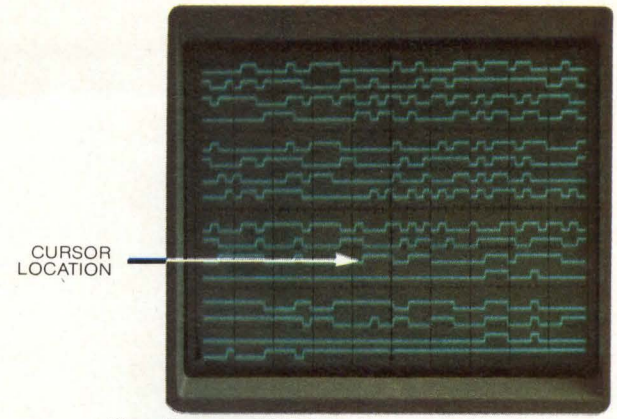
The table of addresses corresponding to tags in a queue is called the

```
;TASK-SCHEDULING EXECUTIVE
;PROGRAM FOR 8080.
;
;PARAMETER DEFINITIONS
QLNTH   EQU     4
QMASK   EQU     3
TBLNTH  EQU     4
TBLMSK  EQU     3
;
;TIME-SLICE INTERRUPT
;ENTERS HERE.
;
;SAVE REGISTERS ON STACK.
TSINT:  PUSH    H
        PUSH    D
        PUSH    B
        PUSH    PSW
;SAVE CURRENT PRIORITY.
        LDA     TCURP
        PUSH    PSW
;SUSPEND CURRENT TASK.
        LXI     H,TSUSP
        ORA     M
        MOV     M,A
;
;ENTER HERE TO DETERMINE
;HIGHEST PRIORITY LEVEL.
;
;GET SUSPENDED TASKS.
TDHPL:  DI
        LDA     TSUSP
        MOV     B,A
;DISREGARD QUEUED TASKS
;ON SAME PRIORITY LEVEL.
        CMA
        LXI     H,TQUED
        ANA     M
;IS SUSPENDED TASK THE
;HIGHEST PRIORITY LEVEL?
TEST1:  CMP     B
;YES, RESUME IT.
        JC      RESTOR
;NO, FIND HIGHEST QUEUED
;PRIORITY LEVEL.
        RLC
        JC      ACTIV7
        RLC
        JC      ACTIV6
        RLC
        JC      ACTIV5
;BACKGROUND IS ALWAYS QUEUED.
        JMP     ACBACK
;
;SAMPLE ROUTINE TO ACTIVATE
;A TASK ON A PRIORITY LEVEL.
;
;SET BIT FOR CURRENT PRIORITY.
ACTIV7: MVI     A,80H
;SET MASK TO CLEAR 'QUEUED'.
        MVI     B,80H XOR OFFH
;SET POINTER TO BRANCH TABLE.
        LXI     D,BTBL7
;SET POINTER TO QUEUE POINTER.
        LXI     H,Q7OUT
        JMP     TASTRT
;
;ROUTINE TO START A TASK AT
;SELECTED PRIORITY LEVEL.
;
;STORE NEW 'CURRENT PRIORITY'.
TASTRT: STA     TCURP
;GET QUEUE OUTPUT POINTER.
        MOV     A,M
;INCREMENT & MASK IT.
        INR     A
        ANI     QMASK
        MOV     M,A
;COMPARE WITH INPUT POINTER.
        INR     L
;ARE POINTERS NOW EQUAL?
TEST2:  CMP     M
;NO, SKIP NEXT PART.
        JNZ     LOOKUP
;YES, CLEAR 'QUEUED' BIT
        MOV     C,A
        LDA     TQUED
        ANA     B
        STA     TQUED
        MOV     A,C
;GET TAG FROM QUEUE.
LOOKUP: INR     L
        ADD     L
        MOV     L,A
        MOV     A,M
;GET ADDRESS FROM BRANCH TABLE.
        ANI     TBLMSK
        ADD     A
        XCHG
        ADD     L
        MOV     L,A
        MOV     A,M
        INX     H
        MOV     H,M
        MOV     L,A
;BRANCH TO START OF TASK.
        EI
        PCHL
;
;ROUTINE TO RESTORE REGISTERS
;AND RESUME INTERRUPTED TASK.
;
;RESTORE PRIORITY LEVEL.
RESTOR: POP     PSW
        STA     TCURP
;CLEAR 'SUSPENDED' BIT.
        CMA
        LXI     H,TSUSP
        ANA     M
        MOV     M,A
;RESTORE REGISTERS & RESUME.
        POP     PSW
        POP     B
        POP     D
        POP     H
        RET
;
;SIMPLE-MINDED BACKGROUND
;TASK SCHEDULER.
;
;SET CURRENT PRIORITY.
ACBACK: MVI     A,08H
        STA     TCURP
;BRANCH TO START OF TASK.
        EI
        JMP     BKGRND
;
;SAMPLE ROUTINE TO QUEUE A TASK.
;
;SET 'QUEUED' BIT.
QTSK7:  DI
        LXI     H,TQUED
        MOV     A,M
        ORI     80H
        MOV     M,A
;GET QUEUE INPUT POINTER.
        LXI     H,Q7INP
        MOV     A,M
;INCREMENT INPUT POINTER.
        INR     A
        ANI     QMASK
        MOV     M,A
;LOAD TAG INTO QUEUE.
        INR     L
        ADD     L
        MOV     L,A
        MVI     M,TAG
;
;STATUS WORDS & SAMPLE QUEUE.
;
;CURRENT PRIORITY LEVEL.
TCURP:  DB      0
;SUSPENDED PRIORITY LEVELS.
TSUSP:  DB      0
;QUEUED PRIORITY LEVELS.
TQUED:  DB      0
;
;QUEUE OUTPUT POINTER.
Q7OUT:  DB      0
;QUEUE INPUT POINTER.
Q7INP:  DB      0
;QUEUE BUFFER AREA.
        DS      QLNTH
;
;SAMPLE BRANCH TABLE.
;
BTBL7:  DW      TASK0
        DW      TASK1
        DW      TASK2
        DW      TASK3
```

Fig 3 Assembly language listing of task-scheduling executive program. Sample routines for queueing and activating tasks on priority level 7 are provided as models for routines required for other priority levels

time domain.

data domain.



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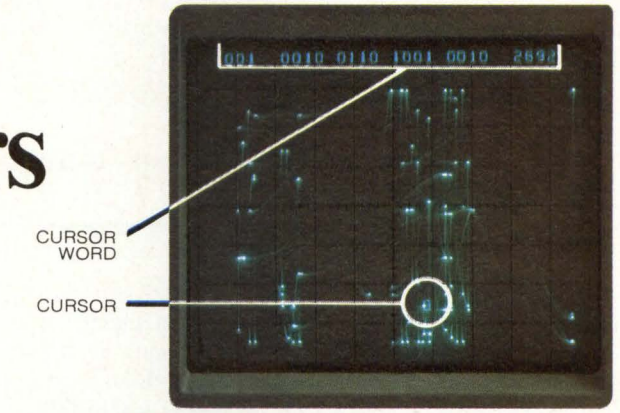
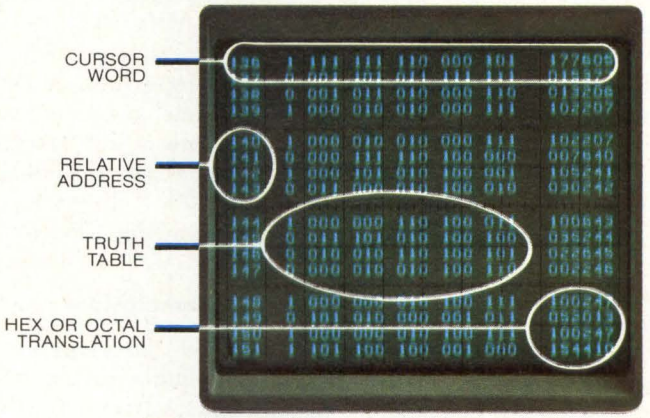


Map—each word in memory is transformed via two DAC's to form a unique dot which characterizes that word. All 512 words of the 1650's memory can be accessed for mapping. The cursor word is circled in the map as well as displayed at the top of the screen in alphanumeric form. The cursor may be moved to any of the points in the map for positive identification of that word. In addition, a map of only 16 words may be selected.



Logic state—provides memory address location, binary output of the 16 channels and selectable octal or hexidecimal translation. 16 words are displayed at one time with the cursor address location at the top of the screen. Movement of the cursor control allows accessing any 16 words of the entire 512 words stored in the 1650-D. The display control memory can store 16 words while a different set of 16 is selected from the 1650's main memory (or a new recording is made). These two sets of 16 words can then be overlayed on the CRT. *Any differences will blink* and be easily identified.

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Task-Scheduling Operations	Execution Time (μs)
Interrupt Task; Start Higher Priority Task	181.5 to 223.5
Interrupt Task; Clear "Queued"; Start Higher Priority Task	201.5 to 243.5
Interrupt Task; Resume It	135.5
End Task; Start Another Task	125.0 to 167.0
End Task; Clear "Queued"; Start Another Task	145.0 to 207.0
End Task; Resume Suspended Task	79.0

Fig 4 Execution times for 8080 CPU with 2-MHz clock. Minimum and maximum times are provided for those operations that determine highest priority level

"branch table" for that queue. Each address consists of a 16-bit number stored in two consecutive memory locations.[2] The tag is used as an offset from the start of the branch table, with the task-scheduling program loading the program counter from the table. In order to avoid possible illegal branches, the number of addresses in the branch table is constrained to a power of 2, and again a mask $(2^N - 1)$ limits the value of the tags. If the number of tasks on a given priority level is less than the number of addresses allowed in the branch table, the table should be filled with "dummy" addresses. All branch tables have the same number of addresses for simplicity.

An assembly language source listing of the task-scheduling executive program appears in Fig 3. In the interest of brevity, redundant portions have been omitted. (See "Sample Routine to Activate a Task on a Priority Level" and "Sample Routine to Queue a Task.") All tasks end by branching to the task-scheduling program (TDHPL).

Whenever any program modifies any of the status words associated with the task-scheduling executive program, *interrupts must be disabled.* Failure to disable interrupts will result in faulty operation, since the time-slicing interrupt could occur during the time that a status word is being modified.

Like any computer program, the task-scheduling executive program requires time to perform its functions. Fig 4 is a table of execution times for various task-scheduling operations. Times are based on a 2-MHz CPU clock with no "wait" states required by the CPU.[1] Using 150 μs/task as an average execution time, and assuming a task-scheduling rate of 100 tasks/s, the overhead of the task-scheduling function is 150 x 100 = 15,000 μs/s, or 1.5% of the available CPU time.

Conclusions

By incorporating this task-scheduling executive program into a high performance microcomputer system, designers may obtain some of the flexibility and performance features of a minicomputer real-time operating system. The microcomputer CPU can execute up to eight levels of software tasks concurrently, with only a moderate amount of CPU overhead required.

References

1. *8080 Microcomputer Systems User's Manual,* Intel Corp, Sept 1975
2. *8080 Assembly Language Programming Manual,* Intel Corp, 1976

Microcomputer Interfacing: Interfacing a 10-Bit DAC

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This month's discussion concerns interfacing an Analog Devices AD7522 monolithic complementary metal-oxide semiconductor (CMOS) 10-bit multiplying digital-to-analog converter (DAC), a 28-pin chip which is a recent example of a generation of inexpensive DACs that can be interfaced directly to 8-bit microcomputers. A typical converter consists of an arrangement of weighted resistors, each controlled by a single bit of input data, that develops varying output analog voltages or currents in accordance with the digital input code.[1] A DAC is used to provide a small analog error signal from a microcomputer that is utilized in a feedback control circuit; to convert a sequence of bytes in memory into analog-vs-time data and thus simulate the output from an analog instrument such as a gas chromatograph or UV-visible spectrophotometer; to provide analog data for the two channels of an X-Y recorder; or, in general, to operate any device that requires an analog voltage or current and is interfaced to a digital device, such as a microcomputer.

For a general discussion of the principles of analog-digital conversion, we suggest Analog Devices' conversion handbook[1] or a series of small pamphlets distributed by National Semiconductor Corp.[2] Important concepts associated with DACs include resolution, accuracy, scale error, gain error, offset error, linearity, differential linearity, monotonicity, settling time, slew rate, overshoot and glitches, temperature coefficient, supply rejection, conversion rate, and output drive capability.[2] A few such terms are summarized in the Listing.

Both an interface circuit to an 8080A-based microcomputer (Fig 1) and a functional diagram of the DAC (Fig 2) are provided to explain how to interface the AD7522

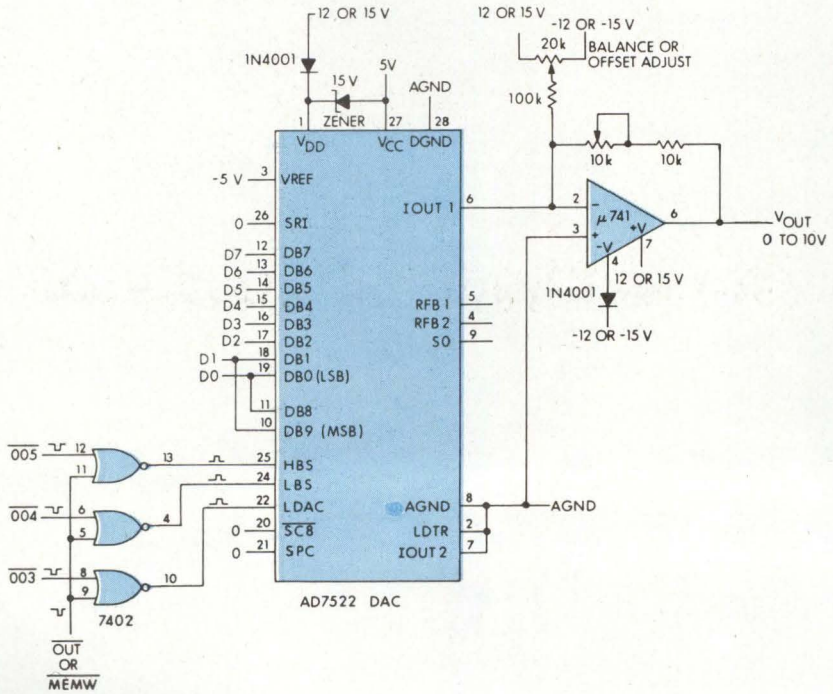

Fig 1 Interface circuit between 8080A-based microcomputer and Analog Devices AD7522 DAC chip

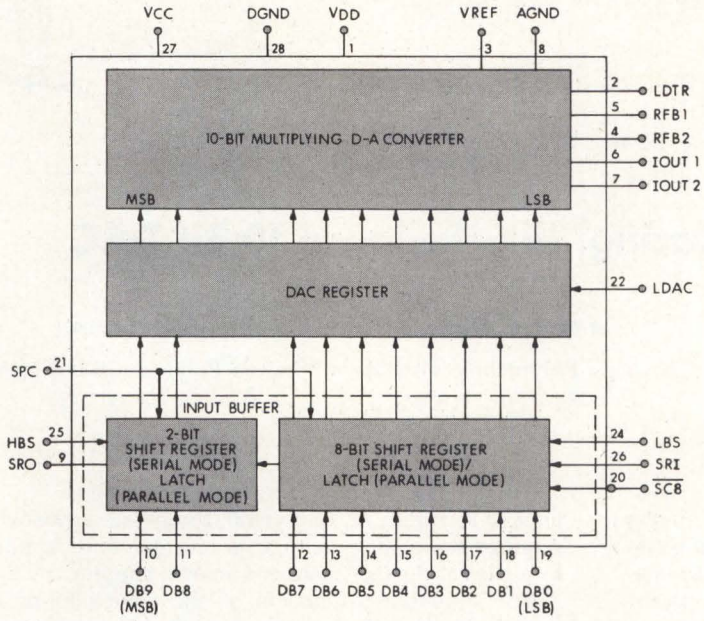

Fig 2 Functional diagram of AD7522 chip (Courtesy of Analog Devices, Inc. All rights reserved)

DAC to an 8-bit microcomputer. An important feature of this specific DAC is that it is double buffered; within the device there are two independent 10-bit registers—the DAC register and the 2-bit and 8-bit shift registers noted as the input buffer (Fig 2). A DAC is an output device for a microcomputer, and thus data are strobed from the

TABLE 1

Memory I/O Program to Generate a Slow Linear Ramp

Execution starts at HI = 003 and LO = 000

	LO Address Byte	Instruction Byte	Mnemonic	Comments
Start:	000	042	SHLD	Strobe ten bits of digital data into AD7522 DAC shift registers. Ten input data bits are contained in register pair H. Address select code for the LBS input is HI = 200 and LO = 004; address select code for the HBS input is HI = 200 and LO = 005
	001	004	004	
	002	200	200	
	003	062	STA	Strobe ten bits of digital data from input buffer into DAC register within the AD7522 DAC. Address select code for the LDAC input is HI = 200 and LO = 003
	004	003	003	
	005	200	200	
	006	043	INX H	Increment register pair H
	007	315	CALL*	Call 10-ms time delay routine, DELAY
	010	277	277	LO address byte of DELAY
	011	000	000	HI address byte of DELAY
	012	303	JMP	Unconditional jump to START, where input of new data into DAC occurs
	013	000	000	LO address byte of START
	014	003	003	HI address byte of START

*On the 8080-based microcomputer used in our courses, a 10-ms time delay subroutine is located in EPROM starting at HI = 000 and LO = 277. Such a routine can be located anywhere in memory

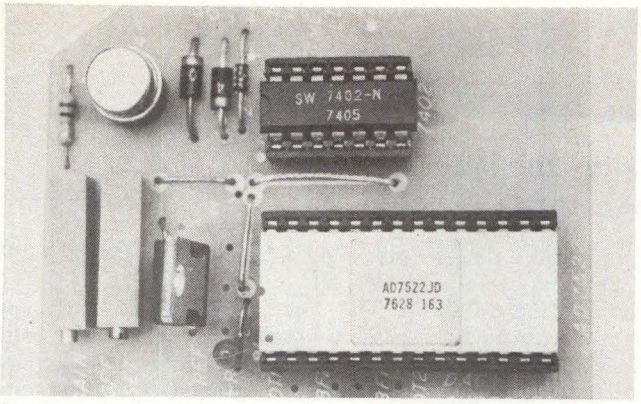

Fig 3 Photograph of DAC Outboard® containing interface circuit shown in Fig 1

microcomputer data bus into the internal registers or latches of the DAC. Fig 1 shows the connections to the 8-bit bidirectional data bus, D0 through D7; the 8080A control signals OUT or MEMW, used with accumulator I/O or memory I/O data transfers;[3] and the channel select outputs 003 through 005 that are generated by a decoder tied to the microcomputer address bus.[4]

Since the AD7522 is a 10-bit DAC, it is not possible to load all ten bits simultaneously into the input buffer (Fig 2) of the DAC from an 8-bit microcomputer. The sequence that actually occurs can be summarized as follows: DAC input bits DB0 through DB7 are first strobed into the 8-bit shift register/latch in parallel using a positive device-select pulse[5] applied at input pin 24, LBS or Low Byte Strobe. The two most significant bits (MSB), DB8 and DB9, are then strobed into the 2-bit shift register/latch via the use of a device-select pulse applied at pin 25, HBS or High Byte Strobe. Finally, a device-select pulse applied at pin 22, LDAC or Load DAC, transfers the ten bits of input data, DB0 through DB9, into the second buffer within the DAC chip, the DAC register, from which the D-A conversion is performed. The output current appears at IOUT1 and IOUT2 and is converted into a voltage with the aid of a μ741 operational amplifier (Fig 1). The two MSBs are loaded from the 8-bit microcomputer bus using any two bits. Generally, bits D0 and D1 are chosen since this makes data formatting easy. Thus, ten bits are transferred as eight bits, D0 to D7, and as two additional bits, D0 and D1.

A simple program that exercises the DAC over its full operating range is provided in Table 1. The program generates a slow linear ramp as the analog voltage output from the AD7522 DAC. This can be observed on a VOM (volt-ohm milliammeter), digital multimeter, or oscilloscope. The ramp output is subdivided into 1024 small steps, each step being approximately 5 mV in magnitude. Total time required to change from 0.0 to 5.12 V is 10.24 s. The SHLD <B2> <B3> instruction outputs two data bytes in succession from register pair H into the input buffer registers of the DAC. Contents of register L are input into the 8-bit shift register/latch and the least significant two bits in register H are input into the 2-bit shift register/latch (Fig 2). Note that the address is automatically incremented and a second MEMW control pulse is generated by the 8080A when it executes a SHLD instruction. The STA <B2><B3> instruction provides only a strobe pulse at the LDAC input to the DAC; no data transfer occurs between the accumulator and DAC.

Additional small monolithic and hybrid DAC systems are available from other manufacturers. The Analog Devices converter was chosen here because of the on-chip latches and double buffering registers. Use of a reference potential is common to many DAC modules. Perhaps in the future, it, too, will be included in the module.

The reader is referred to the specification sheets for additional information concerning use of the AD7522 DAC. Since the input buffer is a shift register, it is possible to serially load the DAC. Less expensive 8-bit versions of the DAC are available. Output from the DAC can be either unipolar or bipolar. We have developed a DAC Outboard® that contains everything in Fig 1, including the 5-V reference source (Fig 3). A copy of the PC layout for the board is available to those who send a self-addressed stamped envelope to Dr Christopher Titus, PO Box 715, Blacksburg, VA 24060.

Concepts Associated With DACs

Resolution	The smallest standard incremental change in output voltage of a DAC. A converter with n input bits can resolve one part in 2^n
Accuracy	Describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors
Settling Time	Elapsed time after a code transition for a DAC output to reach a final value within specified limits
Conversion Rate	The speed at which a DAC can make repetitive data conversions
Nonlinearity	Error contributed by a deviation of the DAC transfer function from a best straight line function (normally expressed as a percentage of full-scale range)

References

1. *Analog-Digital Conversion Handbook*, Analog Devices, Inc, Norwood, Mass (Copies are available for $3.95)
2. "Specifying A-D and D-A Converters," publication AN-156; "Data Acquisition System Interface to Computers," publication AN-159; and data sheets on the DA1200/1201/1202/1203 monolithic DACs, National Semiconductor Corp, Semiconductor Div, Santa Clara, Calif
3. P. R. Rony, J. A. Titus, and D. G. Larsen, "Microcomputer Interfacing: Accumulator I/O vs Memory I/O," *American Laboratory*, Feb 1976, p 119
4. *Bugbook V, Module Six. Introductory Experiments in Digital Electronics, 8080A Microcomputer Programming, and 8080A Microcomputer Interfacing*, E & L Instruments, Inc, Derby, Conn, 1976
5. D. G. Larsen, P. R. Rony, and J. A. Titus, "Microcomputer Interfacing: Generating Input/Output Device Select Pulses," *American Laboratory*, Jan 1976, p 77

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Programmable General-Purpose Keyboard/Display Device and Floppy Disc Controller Interface Microprocessors

A floppy disc controller contained on a single chip and a general-purpose keyboard and display I/O device are both programmable units designed by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 as interfaces for 8-bit microprocessors such as the 8080. The 8271 floppy disc controller interfaces from one to four floppy disc drives to the 8080 microcomputer system; its powerful control functions minimize both hardware and software overhead normally associated with floppy disc interface. The 8279 keyboard/display is designed for general use with microprocessors.

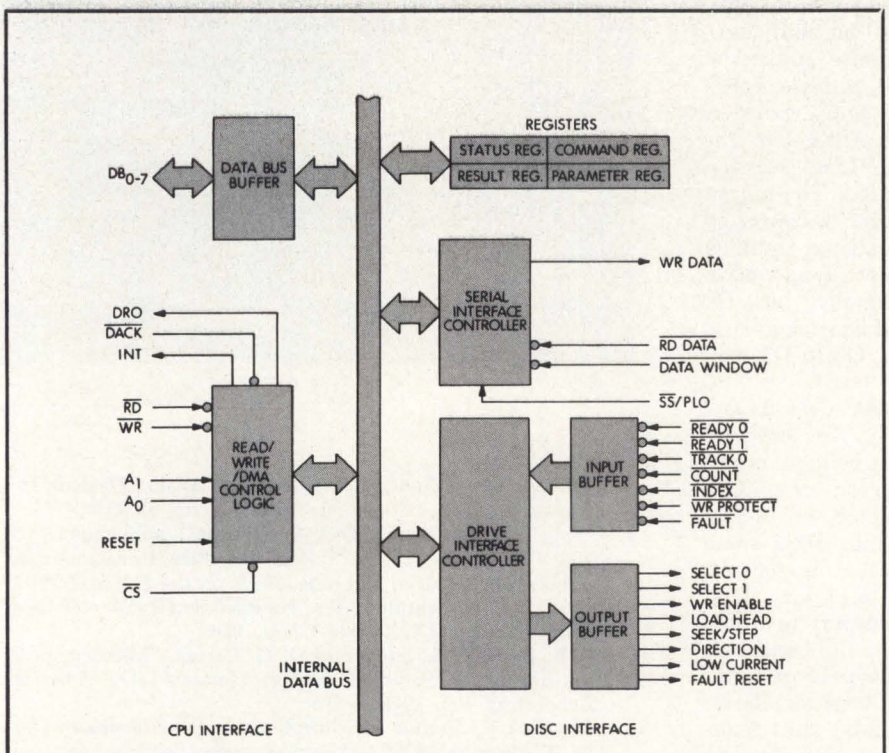
The floppy disc controller is an LSI component which supports a soft-sectored format that is IBM 3740 compatible. This high level controller relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disc interface. A variety of high level instructions are supported which allow the user to store and retrieve data on a floppy disc without dealing with low level details of disc operation.

Features of the controller are programmable record lengths, multi-sector capability, and dual drives which are expandable to four drives. Automatic read/write head positioning and verification; internal CRC generation and checking; and programmable step rate, settle-time, head load time, and head unload index count are all included.

Fully compatible with the 8080 CPU, the 40-pin DIP controller requires a single 5-V supply. As an 8080 peripheral device, the controller during operation accepts and executes commands from the CPU, providing a result to the 8080 CPU at the end of execution.

The controller can accept many powerful software commands from the CPU. In addition to standard read/write commands, a scan command is supported which allows the user program to specify a data pattern and instructs the controller search for that pattern on a track. Once the scan is initiated, no CPU intervention is required.

Circle 179 on Inquiry Card



Block diagram of Intel's single-chip 8271 programmable floppy disc controller illustrates CPU and disc interfaces. Device interfaces from one to four floppy disc drives to 8080 microcomputer systems. Hardware and software are minimized with use of powerful control functions

Keyboard/Display Interface

Since data input and display are integral to many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 programmable I/O device contains two sections: keyboard and display. The keyboard portion which interfaces to regular typewriter-style keyboards, or random toggle or thumb switches, can provide a scanned interface to a 64-contact key matrix, expandable to 128. This part also interfaces to an array of sensors or a strobed interface keyboard, such as the Hall effect and ferrite variety.

Key depressions can be 2-key or N-key rollover. Keyboard entries are debounced and stored in an 8-character FIFO. If more than eight characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display section provides a scanned display interface for LED, incandescent, and other display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The interface has a 16 x 8 display RAM which can be organized into a dual 16 x 4; RAM can be loaded or interrogated by the CPU. Right entry, calculator, and left entry typewriter display formats are possible. Read and write of the display RAM can be done with auto-increment of the display RAM address.

The 40-pin DIP interface features simultaneous keyboard display operations, programmable scan timing, and interrupt output on key entry. The device directly connects to the 8080 bus. The CPU can program all operating modes for the interface.

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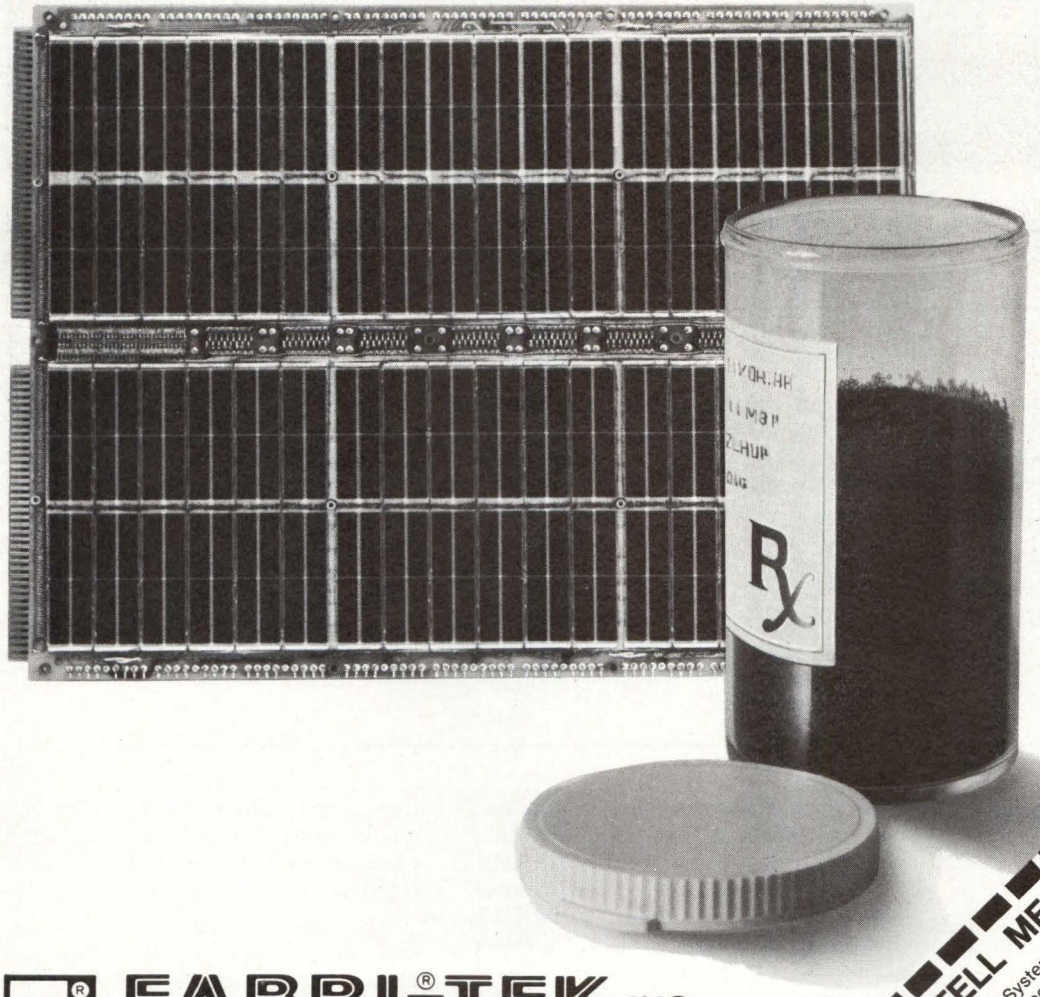

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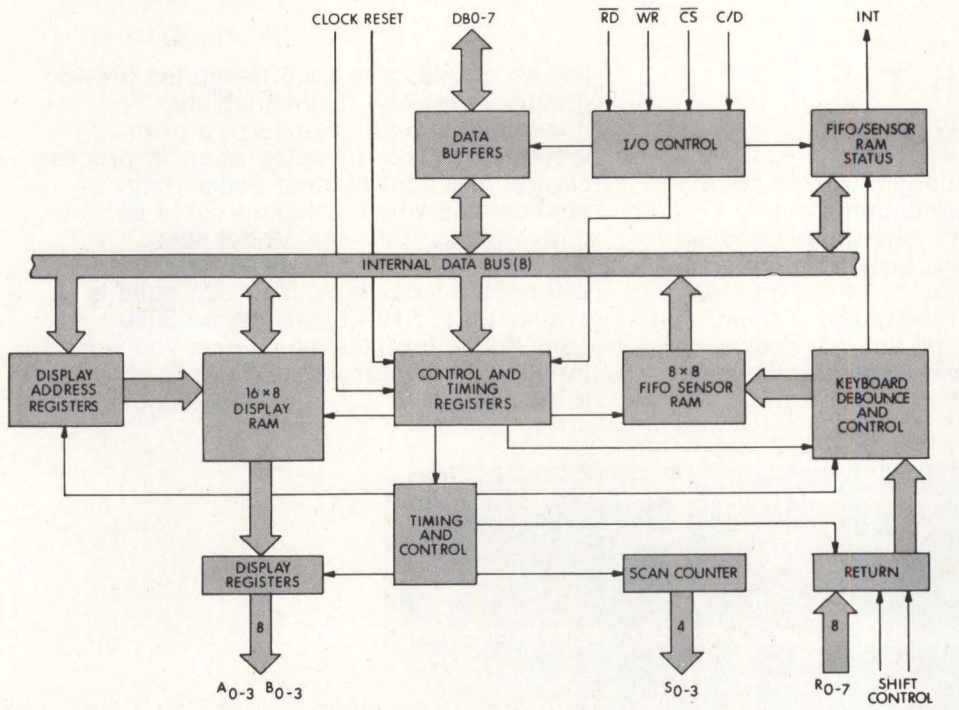

Major components involved in operation of Intel's 8279 programmable keyboard/display I/O interface are displayed in block diagram. Device controls input and display for 8-bit microprocessors without placing large load on CPU

Input modes include scanned keyboard and scanned sensor matrix, both with encoded or decoded scan lines; and strobed input. Software commands program the interface's various operating modes.

A programmable clock matches scan times to the CPU cycle time. Interrupt output signals the CPU when keyboard or sensor data are available.

Major components are I/O control and bidirectional data buffers; control and timing registers, and timing control; scan counter; return buffers, and keyboard debounce and control; FIFO/sensor RAM and status; and display address registers. Registers store keyboard and display modes, as well as other operating conditions programmed by the CPU. Display address registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed.

Absolute maximum ratings are ambient temperature, 0 to 70°C, and storage temperature, −65 to 125°C. Voltage on any pin with respect to ground is −0.5 to 7 V; power dissipation is 1 W.

Circle 180 on Inquiry Card

Microcomputer Products Feature Speed and Multiprocessing Ability

A 16-bit microcomputer with high speed asynchronous bus and data controller that allows DMA data transfers at rates to 16M bits/s, as well as a family of compatible microprocessor CPU and memory application cards featuring on-card memory, small size, and low price, have been developed by the Microcomputer Systems Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. The IMP-16L, which can be used as a process or machine-tool controller, is a fully assembled unit that includes an IMP-16 CPU board with DMA control, 4k by 16 bits of RAM expandable to 64k, a standard TTY interface module, and program control panel. Optional cards provide interface for a Centronics 306 printer, a Documation 300 card reader, and the company's IMP-16/805 p/ROM programmer card.

The programmer's panel, which is removable to prevent unauthorized operation, has an array of data switches, data and address indicators, and function switches. The operator uses this to address, load, and examine memory controls or CPU registers.

The microcomputer has 60 general-purpose instructions which include time saving single-word commands. It accommodates either arithmetic or POWRI/O control read-only memory (CROM) devices. Arithmetic CROM has 10 addition instructions that speed calculation involving high accuracy fractional data and floating point numbers. POWRI/O CROM, with 11 instructions, provides block transfer and peripheral I/O commands

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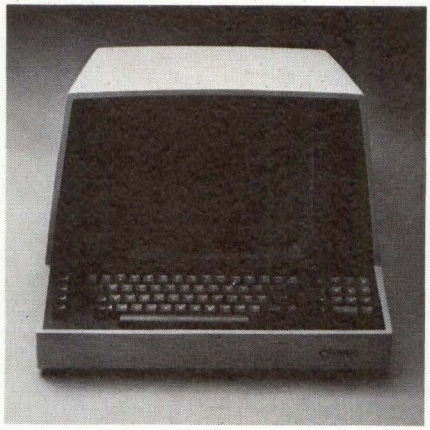

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Other than that, it's pretty standard.

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We aren't so dumb.

CIRCLE 97 ON INQUIRY CARD

National Semiconductor's IMP-16L microcomputer system offers CPU board with DMA control, 4k RAM, TTY interface module, programmer's front control panel, and software support. It provides DMA data transfers at rates to 16M bits/s

allowing data transfers of up to 97k words/s.

Combining DMA capability with special instructions gives the computer power to handle data processing tasks traditionally in the minicomputer domain. Flexibility allows a wide variety of applications. Up to three CPU cards can be used with the system's architecture for multiprocessing.

The computer has four general-purpose registers and a 16-word LIFO stack. I/O lines include eight general-purpose flags, one general interrupt, one vectored interrupt, and four general-purpose jump condition inputs.

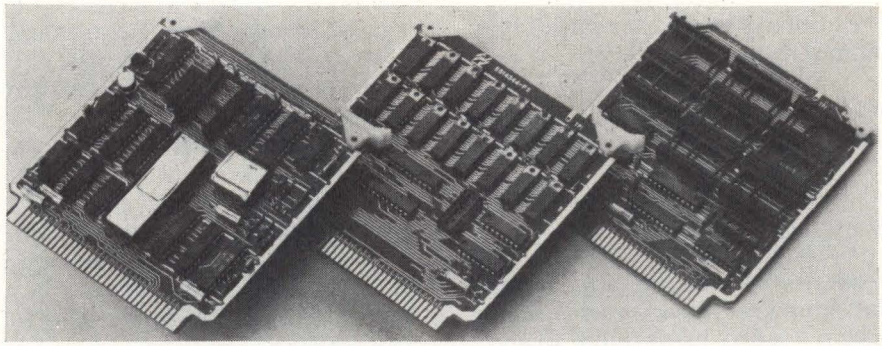
With a 1.4-μs microcycle time, the computer has typical register-to-register addition times of 4.9 μs and memory-to-memory addition times of 8.4 μs. Time required for DMA transfer is 1.05 μs.

Measuring 12 x 17 x 24" (30.48 x 43.18 x 60.96 cm), the microcomputer has 12 connectors for CPU, memory, and interface cards. For expansion, additional 6-connector card cages may be installed. Required input power is 105 to 125 V at 60 Hz; 220 V at 50 Hz is optional.

Software support includes CPU, memory, and peripheral diagnostic routines; software DEBUG, resident assembler; IMP-16 to PACE or SC/MP cross assemblers; absolute and linking loaders; and an IMP/FORTRAN cross assembler.

Microprocessor Board Family

Small size, together with the capability of page addressing, multiprocessing, and DMA, produce a microcomputer suited to physically confined situations. Based on the 8-bit, single-chip SC/MP microprocessor (see *Computer Design*, April 1976, pp 134, 136, 138, and July 1976, pp 128, 137), the cards reduce development time in applications ranging from games to industrial controls.



Providing multiprocessing capability, family of low cost compatible cards, also available from National Semiconductor, includes the SC/MP-based ISP-8C/100 CPU card with 256 x 8-bit RAM; and the /002 2k x 8-bit RAM card, /004P 4k x 8-bit p/ROM card, and /004B 4k x 8-bit ROM/p/ROM socket card for applications requiring increased memory capacity

Basic CPU card is the ISP-8C/100 application module with SC/MP microprocessor, timing and control circuits, 256 x 8 bits of RAM, a socket for 512 bytes of either p/ROM or pin-compatible ROM, and buffer circuits. Measuring 4.375 x 4.862" (11.113 x 12.349 cm), the card has an 8-bit Tri-State® data/control bus and latched 16-bit address bus. Expanded address busing permits selection of up to 16 memory pages as well as specific locations within the page.

Two separate ports allow input and output of RS-232-type serial data. Three program-controlled flag output signals and two program-controlled sense inputs allow single-line peripheral control.

In small applications, a single CPU card supplies complete control capability. In larger applications up to three cards, combined with additional memory cards to 64k words, give multiprocessing capability. ROM, p/ROM, and RAM can be intermixed in any configuration.

For increased memory capacity, there are also size- and bus-compatible RAM and p/ROM/ROM application modules. The ISP-8C/002 RAM card provides 2k x 8 bits of static read/write memory and all control circuits required for address decoding and bidirectional data transmission over the Tri-State buses. For applications using less than 64k words of memory, unassigned addresses are used for peripherals, enabling all SC/MP memory instructions to be used for peripheral control.

The ISP-8C/004P application card has 4k x 8 bits of unprogrammed erasable p/ROM supplied by eight 512 x 8-bit chips. The ISP-8C/004B ROM/p/ROM card has sockets for up to eight 512 x 8-bit erasable p/ROMs or pin-compatible ROMs. Both cards contain complete control circuits, module-select logic, and I/O buffers.

System software includes ROM resident assemblers, IMP-16 and PACE cross assemblers, FORTRAN cross assemblers, ROM-resident NIBL, and ROM-resident loaders and debug programs. System aids include SC/MP, PACE, and IMP-16 development systems.

The /002 CPU card has a 2-μs/microcycle instruction execution speed. Power supply requirements are 5 and −12 V for the CPU and ROM/p/ROM cards, 5 V for the RAM card. Packaging accessories are readily available; mating connectors, compatible card cages, extender cards, and wrapped-wire and interface cards are available from various sources.

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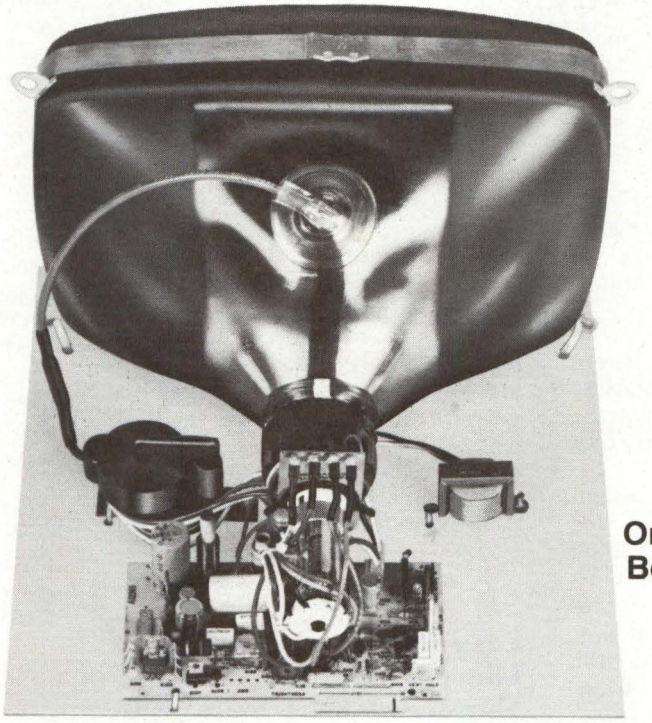

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Ball Electronic Display Division

CIRCLE 98 ON INQUIRY CARD

Hex/Octal-Based 8080 Editor/Assembler Is Co-Resident

Useful in simplifying the preparation of assembly language programs for 8080 systems, the co-resident editor/assembler program (TEA) is a development package incorporating both octal and hexadecimal codes. The program can be used to create, modify, and assemble symbolic or source programs.

The assembler accepts both octal and hexadecimal address and data values intermixed in the same program. Final assembled listings may also be in either code. A single keyboard command allows switching between octal and hexadecimal output at any time.

The editor portion contains full editing commands, character string search commands, and commands to list sections or entire contents of the current text buffer. A punched paper tape may also be created.

The source program can be assembled at any time from paper tape or memory. The assembler identifies the type and location of errors, allowing immediate editing. The program can then be reassembled.

Once errors are eliminated, the assembler punches a binary paper tape, and produces a source program listing of addresses, instructions, and data. The paper tape can be loaded into the microcomputer system to begin the debugging process.

Programs which are too large to be contained in memory at one time may be prepared in sections which are reread back into the 8080 using TEA. A binary tape is produced during the second reading, and the third time a teleprinter listing is produced.

Tychon, Inc, PO Box 242, Blacksburg, VA 24060 has developed the program to require only 5k of memory (R/W or p/ROM). It is completely I/O independent relying upon its own I/O software or I/O routines already available in a user's system.

The editor/assembler is relocatable using a special relocator within the program which places TEA anywhere in the 8080's memory space. The program is available in 1702A or 2708 p/ROMs and on paper tape; listings are also available. Two versions are the standard one starting at address 000 000 (hexadecimal 00 00), and the special one starting at user specified addresses.

Circle 181 on Inquiry Card

Simulator/Debugger Is Interactive Programming Tool

An integrated simulator-debugger simulates a virtual Texas Instruments TMS1000 system on a host computer. The product from Boston Systems Office, Inc, 400-1 Totten Pond Rd, Waltham, MA 02154 allows users to interactively examine and modify programs in a symbolic manner. It can also be used in conjunction with the company's CA1000 cross-assembler, producing a powerful programming tool for developing software for the TMS1000 system.

The simulator-debugger is available on national timesharing as well as for use on inhouse host computers. It is written in the assembly language of the host computer, resulting in high processing speed while requiring less than 16k of memory. The software is cost-effective as it is claimed to run 20 times faster and require one-quarter to one-third the memory of others.

Circle 182 on Inquiry Card

Easy to Assemble Microcomputer Kit Features n-MOS 8-Bit MPU

With a simple PC board layout enabling kit construction in one evening, the Educator II 8-bit microcomputer system contains everything necessary to assemble and operate the microcomputer. It includes an n-MOS 8-bit MPU, PIA, 128 x 8-bit static RAM, two TTL 512 x 4-bit ROMs, and a TTL clock circuit. Clock frequency is approximately 625 kHz. A separate power supply is required.

The HEP/MRO Operations Group of Motorola Semiconductor Products, Inc, PO Box 20924, Phoenix, AZ 85036 uses n-MOS components that are HEP versions of the M6800 microcomputer products. The kit utilizes the full M6800 MPU instruction set and address modes.

An executive program, residing in ROMs, contains routines for examining and modifying memory locations and MPU registers, servicing interrupts, transferring programs to and from cassette tapes, searching tapes, and testing the finished kit. The executive uses 14 bytes of RAM for scratchpad; the remaining 114 bytes are for user programs. An optional 128 x 8-bit RAM can be added to the PC board for larger user programs.

The microcomputer is housed in an aluminum case. Entry and display of machine code is through front panel toggle switches and LEDs. Edge connectors on the board provide an interface to the PIA and address, data, and control buses for system expansion. Accessories which are planned include a keyboard kit, video display kit, module card rack and power supply, memory modules, and applications programs on cassettes.

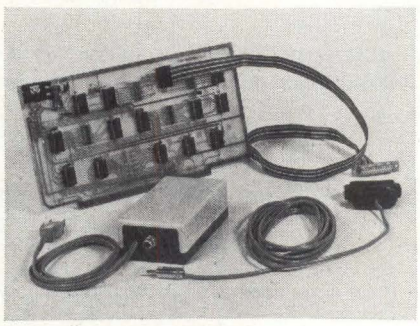
A construction/instruction manual covering theory of operation, application programs, and a test-as-you-build feature is included with the kit, which retails for $169.95. Optional RAM is priced at $19.04.

At the same time, the HEP/MRO Operations Group announced a complete power supply kit designed for the Educator II. Priced at $29.95, the power supply provides a regulated 1.0-A, 5-Vdc ±5% output. A 60-Hz real-time clock signal (approximately 5.1 V pk-pk) is also available. Kit requires 117-V rms, 60-Hz input power.

Circle 183 on Inquiry Card

System Concept for Power Allows Distributed Control for S-100 Bus

Many applications have been opened up for S-100 bus microcomputers with the introduction of the PC3200 power control system from Comptek, PO Box 516, La Canada, CA 91011. System components—the PC3216, a 16-channel logic interface (CLI), and the PC3202, a 400-W 120-Vac power control unit (PCU)—combine to form a high quality ac power switching system to enable microcomputer control of lights, small motors, ap-



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Infotek's FAST BASIC ROMS add to the machine instruction set where HP left off. These ROMS provide spectacular increases in the work throughput of your 9830A/B. For example, you can process arrays at speeds of 40,000 words per second, attain an I/O capability of 10,000 bytes per second, greatly increase the power of a 9880A/B disk system, and print from a buffer while computing.

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RS-30 High Speed RS 232C Interface	750
TC-30 Real Time Clock	825
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pliances, and tools. They are designed around a system concept developed to meet demanding needs from personal systems to light and medium industrial control.

The concept behind this design is that since real world power control applications are external to the microcomputer, power switching devices also should be located externally. Lengths of ac power cabling to and through the microcomputer chassis are eliminated.

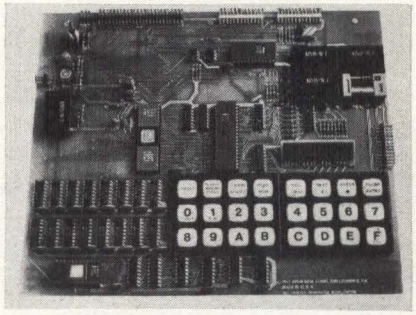
The CLIs that are located on S-100 compatible circuit boards and the PCUs that can be remotely located at the desired point of control allow this type of distributed processing. Control outputs from the CLIs are low voltage, current limited signals routed to various PCUs. Optical isolation is provided at both ends of the control signal providing maximum noise immunity and short-circuit protection.

CLIs contain up to 32 independently addressable control channels, yet require only one output port address. A single byte output from the processor selects an individual channel, turning it on or off without affecting the state of any other channels. Program control of the system's channels is straightforward, and usually can be accomplished with a single BASIC statement.

Circle 184 on Inquiry Card

Control Computer and 1M-Byte Memory System Developments Announced

A single-board control computer based on Intel's 8048 microcomputer chip and a megabyte memory system for microcomputers have been introduced by IMSAI Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577. The 8.5 x 10" (21.6 x 25.4 cm) 8048 control computer is a programmable computer and hardware control system. Components include an 8-bit CPU, 2.5-μs instruction cycle, 96 instructions, BCD arithmetic capability, 1k words of ROM or compatible EPROM program memory, 64 words of internal register memory, and 27 I/O lines.



Single-board control computer using Intel 8048 microcomputer chip allows tools, instruments, and appliances to be directly connected and controlled. Programs are input through onboard keyboard, device is attached, and immediate control of device is obtained

Other features are an internal timer/event counter, oscillator and clock driver, a 24-pad hexadecimal keyboard, 9-digit LED hexadecimal display, reset circuit, and interrupt circuit. The computer uses a single 5-V supply and is TTL-compatible.

Claimed to be the first single-chip control computer to contain all of those features, the system's capabilities enable it to operate as a user-programmable controller for diverse applications. Components include cassette interface; serial I/O (RS-232, current loop); five relays capable of handling 2 A at 220 V, 3 A at 110 V, or 5 A at 24 Vdc; 1k (optional additional 1k) of user-programmable program memory; and dc power supply or battery operation.

The 8048/8748 microcomputer chip is designed to accommodate three memory spaces: program memory, internal register memory, and external RAM. Program memory consists of 1k bytes of ROM/EPROM on the chip itself, and is expandable to 4k with additional ROMs/EPROMs. With memory banking techniques, the space can be expanded to 65k or more. This is the only memory space from which instructions can be fetched and executed.

Internal register memory can be divided into four separate, contiguous areas. Provisions exist for 2k of external RAM; the instruction set allows for direct access of 256 bytes expandable by use of memory banking to any level in 256-byte increments. Internal and external memory are RAM, and can be written into and read from by the user. Both external RAM and program memory are mapped into the same memory space.

Two versions of the computer are available, either assembled or in kit form. A ROM version contains the system monitor on the 8048 chip itself. The other contains the system monitor on an Intel 8716 2k EROM.

Circle 185 on Inquiry Card

Megabyte Memory System

The complete memory system for the company's 8080 and other S-100 bus computers consists of the RAM-16, -32, and -65 low power dynamic memory boards of 16k, 32k, and 65k bytes respectively, and an intelligent memory manager (IMM) controller board. It may be implemented in a variety of configurations requiring very large memories; larger multiprocessor systems can be implemented using multiple mainframes and shared memory facility.

Shared memory blocks can be up to 65k bytes and each processor can address up to one megabyte total of shared and local memory. If desired, the user can specialize the system by selecting an added cost 8755 option and modifying the program.

Modules, offered in kit form or assembled, may be used alone or in combination to form a conventional memory system of up to 65k bytes. With 400-ns access time and hidden refresh, no wait states are required when accessed by the MPU. The address of each 16k-byte block is individually selectable.

The IMM is implemented with an 8048 microcomputer, an 8155 memory I/O and 8255 ROM I/O timer chips to provide 2k bytes of program and 320 bytes of data storage. It provides for memory expansion to one megabyte, write protect for each 1k block in the extended space, read protection, fully vectored interrupts, time of day clock, and real-time clock. It also maintains a table of process control words.

Memory expansion is implemented by increasing the number of address lines from 16 to 20, and using a form of block switching to control the four added lines. Extended address space is divided into 64 16k-byte blocks of which four may be online at any one time.

The read/write protect function is implemented at two levels. The first level, always in effect, divides the extended space into 1024 1k blocks which may be write protected or enabled individually or in larger blocks, under software control or individually from front panel switches. The second level is a read/write protect mask which defines a segment in memory which is enabled with all

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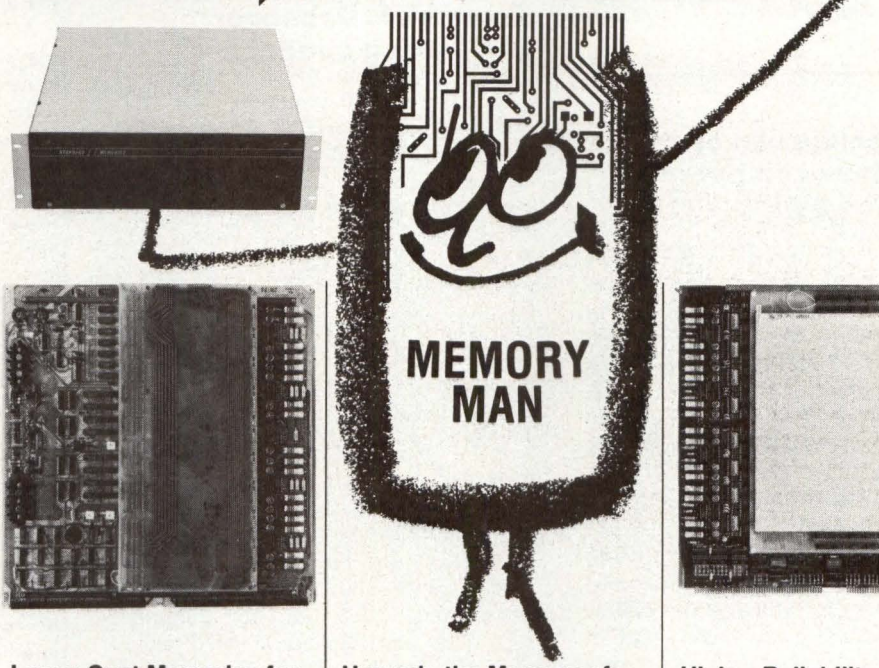

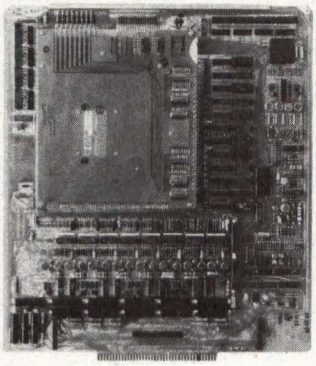

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CIRCLE 101 ON INQUIRY CARD

other memory protected. When this level is switched in, a memory location is accessible only when enabled at both levels.

Interrupt control functions include eight interrupt request lines, each with its own PCW. Interrupts can be selectively masked at the IMM, or programmed to be non-maskable at the MPU.

The real-time clock can generate interrupts at software selectable rates from 200 μs to 1600 s. The IMM maintains 16 4-bit nibbles which may be written or read by the system MPU. These nibbles are also multiplexed to a connector for use by an optional display. When the feature is selected, the bottom 10 nibbles are maintained as a BCD time of day clock.

Circle 186 on Inquiry Card

Bipolar Emulation of 8080A Microcomputer Is Speeded By Kit

Bipolar emulation of the Intel 8080A microcomputer system, with execution speed improvements of up to nine times, is possible with the 8080 emulator kit (3000KT8080SK). It is a microprogrammed microprocessor using Schottky LSI components to implement the 8080A emulation at speeds that allow expansion of existing 8080A-based systems with no change in software.

Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 has manufactured the emulator to provide a 150-ns microinstruction cycle time and a 150-ns RAM access time. All components required for construction, including the preprogrammed microcontrol store and PC board, are included. The emulator is equivalent in function to systems containing the Intel 8080A, 8228, 8224, and 8212; it executes all 8080A instructions with performance improvements on individual instructions ranging from two to nine times that of the 8080A system.

Features of the kit are fully static operation (dc to 150 ns), a single 5-V power supply, hardware multiply and divide, and full vectored interrupt to any location within 64k of memory. It is also microprogram expandable so that the user can utilize 12 unused instruction locations in the 8080 for expanding the instruction set. Over 150 spare locations are available in the control store for this expansion.

Bipolar LSI elements permit a single phase clock instead of the 2-phase nonoverlapping clock of the 8080A. In addition, the system does not provide signals which emanate from the 8080 during sync time; instead it generates status signals normally provided by the 8228 system controller. The kit provides standard address, data, status, and control buses as defined in the Intel 8080 microcomputer system manual.

Circle 187 on Inquiry Card

8080 Compiler Combines Assembler, Debugger, and Linking Loader

The FORTRAN-80 compiler for the 8080 microcomputer is a full implementation of ANSI Standard FORTRAN with the exception of the double precision and complex data types. It provides three data types—logical (1-byte), integer (2-byte), and real (4-byte floating point). An extended version with double precision and complex data types is forthcoming.

The compiler generates pure, relocatable code which may be placed in ROM; the runtime package may also be placed in ROM. The 1-pass compiler requires less than 12k bytes of memory, and the runtime system less than 6k bytes.

A relocating linking loader is included with the package. Subprograms may therefore be compiled separately and linked at load time. Only the specific subprogram required (including system subprograms) are loaded.

The package also has a relocating assembler and assembly language debugging program. The assembler may be used to produce FORTRAN compatible subprograms; the debugging system may be used with the load map produced by the loader to debug FORTRAN or assembly language programs.

Additional features of the compiler available from Microsoft, 819 Two Park Central Tower, Albuquerque, NM 87108 are multistatement code optimization, mixed mode expressions, and all standard FORTRAN library functions for reals and integers.

Circle 188 on Inquiry Card

Process Control Interface Boards Offer Unlimited Potential

Both the Altair 88-process control interface (PCI) board and the similarly designed Altair 680b-PCI enable Altair computers to communicate with relays, switches, motors, fans, contacters, alarms, solenoids, lights, heaters, and other electromechanical devices. With the addition of these boards, the computers also can be used in a greater variety of scientific and industrial applications, where the computer must control large amounts of power.

MITS, 2450 Alamo SE, Albuquerque, NM 87106 has equipped each board with eight relay outputs with spst operation, capable of switching 1 A at 120 Vac. The addition of relays allows an essentially unlimited amount of power to be controlled. Both boards also have optically-isolated inputs, configurable to accept a wide range of input signals.

Two optically-isolated, software-controlled "handshake" lines are also provided for interfacing with external devices. All lines are isolated and balanced for operation in electrically noisy environments.

Each board is also equipped with a complete interrupt structure under software control. For relay control, the boards require only an 8-bit word to be output from the computer to the relay control channel once board initialization is complete.

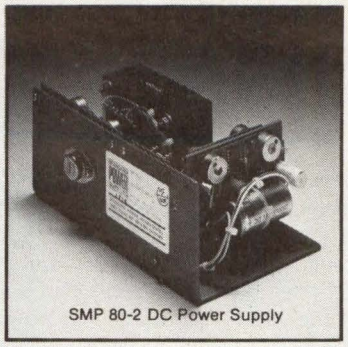
Lines set to a logic 1 by this method energize their respective relays; those set to 0 de-energize. Input from the opto-isolator input channel reads data from the opto-isolated input lines.

Circle 189 on Inquiry Card

Low Cost Software Operates on 8080 Microcomputer Systems

Previously available only to OEMs, the CP/M low cost advanced disc operating system has been in existence for over three years in various manufacturers' products and has undergone extensive field testing. It is now available to small computer users with IBM-compatible diskette-based computer systems employing the Intel 8080 microcomputer.

(Continued on p 218)



SMP 80-2 DC Power Supply

When you have to engineer for microprocessor-based systems

Our new SMP Series DC power supplies is just the ticket you need for those tough microprocessor-based system applications. And there are several reasons.

First, it interfaces *directly* with the power requirements of virtually all microprocessor ICs. No expensive custom design work is needed.

Too, you can get four independent and isolated outputs. You can power logic, memory and displays, for example, from one simple power source.

For extra flexibility, we give you 115/230 V ac universal input. And we've designed in all the little extras for top performance: well regulated, overvoltage protection, highest quality components and low ripple.

Our SMP 80-2 also features temperature compensated circuitry. So if the temperature goes up, your output stays right on track.

But most importantly, it embodies a reliable design proven in more than 10,000 units now in use.

For detailed specs, price schedule, and product arrival times, telephone your local stocking distributor, or contact Standard Power, Incorporated, 1400 South Village Way, Santa Ana, California 92705. Telephone: (714) 558-8512.

STANDARD POWER

CIRCLE 102 ON INQUIRY CARD

Functions of this software package from Digital Research, PO Box 579, Pacific Grove, CA 93950 include named dynamic files, program editing, assembly debugging, batch processing, and instantaneous program loading, resulting in facilities similar to timesharing services. Overall operation of the software closely resembles standard features of the DECsystem-10. Components include a basic disc operating system, console command processor, peripheral interchange program, batch processing features, editor, assembler, dynamic debugging tool, loader, dump utility, and system generation utility.

An "unbundled" software package, it can be adapted easily to any 8080 or Z80 computer system with at least 16k of main memory and one or two IBM-compatible disc drives. Although the standard system operates on an Intel MDS, a field-modification manual explains how to alter it for other hardware configurations.

The system is distributed on an IBM-compatible diskette in machine code form only (source programs are available for internal use, or distribution with custom hardware at additional cost). Complete documentation covers system operation and programming in the CP/M environment.

Circle 190 on Inquiry Card

Proprietary Software Is Available for 6800 Development

MICRO BASIC is a complete resident software development system which includes a compiler, editor, loader, debug, and runtime support routines. This product, previously available only to 8080 microcomputer users, offers efficient interactive software development for 6800 microcomputer users.

Programs can be developed in BASIC. Fast integer arithmetic and powerful string manipulation features are suited to many microcomputer applications. In addition, external subroutines can be incorporated to accommodate special interface requirements.

To use the system, all that is needed is a 6800 microcomputer with at least 24k bytes of memory, and an I/O device. Announced by Ryan-McFarland Corp, Rolling Hills Estates, Calif, MICRO BASIC is available in paper tape, cassette, or diskette form exclusively from Hamilton/Avnet Electronics.

Circle 191 on Inquiry Card

Dual Output DC Supplies for Microprocessors Meet Universal Applications

A series of UL recognized dual output power supplies for microprocessors are designed for universal applications. Designated the "Gold Dust Twins" and "Big Red" series, the units measure 4 x 2.75 x 4.87" (10.16 x 6.99 x 12.37 cm) and 7 x 3.4 x 4.87" (17.78 x 8.64 x 12.37 cm), and have gold and red irridite finished chassis, respectively.

The entire line has primary ac input capabilities to operate over a range of 115/230 V, ±10%, 47 to 63 Hz at a temperature up to 50°C ambient with no derating. Units may be operated up to 65°C with derating.

In the Gold Dust series, four models have output ratings of ±5 Vdc, 0.8 A; ±12 Vdc, 0.75 A; ±15 Vdc, 0.6 A; and 5, −12 Vdc, 1.0, 0.5 A. The Big Red series of three models has outputs of ±12 Vdc, 1.5 A; ±15 Vdc, 1.3A; and 5, −12 Vdc, 3.0, 1.5 A.

Adtech Power, Inc, 1621 S Sinclair St, Anaheim, CA 92806 has designed the units to have high reliability; MTBF using MIL-HDBK-217A guidelines is over 60,000 hours. Devices are constructed on an open aluminum chassis with approximately 20% more heat sink area than other supplies. Mounting may be accomplished in various orientations with optional fasteners available.

Electrostatically shielded transformers provide lower high frequency noise experience. Units are regulated by hermetically sealed IC regulators in metal enclosures. All transistors used are hermetically sealed TO-3 can types.

Units may be connected in series or parallel to provide higher output voltages and currents. Overvoltage protection is available with either one on each output or a single one to protect both outputs. Regulation is ±0.05% for line, ±0.1% for load. Ripple is 1 mV rms (3 mV peak-to-peak maximum).

Circle 192 on Inquiry Card

SELF-STUDY MICROCOMPUTER SOFTWARE/HARDWARE TRAINING COURSE

COURSE 126

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INTEGRATED COMPUTER SYSTEMS, INC.

THE FINEST UNBIASED MICROCOMPUTER TRAINING

- In your home or office
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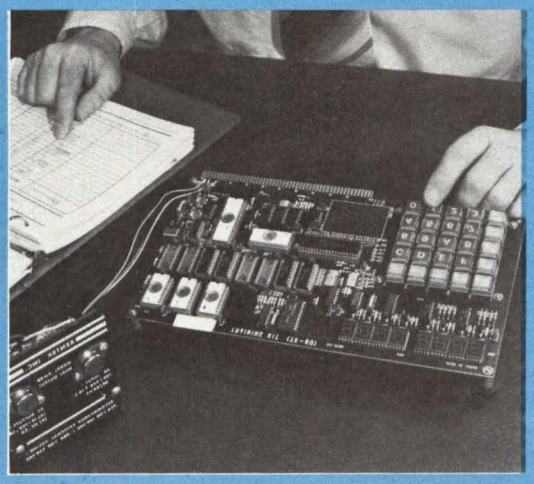
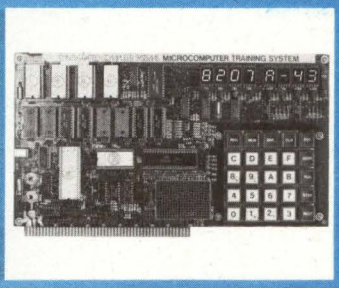


The new ICS Hands-On Training System is the first and only *SOFTWARE/HARDWARE* SELF-STUDY COURSE. The ICS Training System includes a fully-assembled 8080A microcomputer and built-in educational monitor program together with a coordinated **650 page Workbook/text.** The System is ready to use in your office or home (with its built-in keyboard/display, no expensive teletype or CRT terminal is required)! You will learn the details of both programming and interfacing by actually performing scores of exercises on your own microcomputer — at your own pace.

The Training Computer itself includes: the 8080 microprocessor, .5K CMOS RAM, 1K PROM, three parallel I/O ports, two serial ports, one DMA channel, and the on-board 8-digit display and 25-key keyboard. The ICS Monitor program is specifically designed to be easy to use. It provides many unique functions essential for efficient learning. Furthermore, many Monitor routines are available for use in your own programs, including display and keyboard I/O, timing, cassette interfaces, etc.



Using the ICS Training System, you will first learn each 8080 instruction through simple exercises which illustrate its effective use. These exercises, which also teach you basic programming, then progress to more and more advanced techniques. Other exercises specifically teach how to debug your programs quickly and effectively. Furthermore, throughout the course, hardware interface design and implementation projects are coordinated with programming problems. (For example, as your first project you will build a simple interface to an audio-cassette recorder.) Thus, you will learn both hardware and software design techniques and how to make software/hardware tradeoffs by actual hands-on experience.

KEY TOPICS

• Introduction to the training system • Hardware fundamentals • Software fundamentals • The 8080 instructions — one by one • Using the keyboard/display to load and check programs • I/O programming — parallel/serial • Using a programmable I/O device • Interrupt handling (vectored/priority) • Organizing data in program (PROM) and data (RAM) memory • Subroutine structures • Real-time program design • Interfacing to a TTY, audio cassette, CRT • Advanced math routines (trig, logs, floating point, etc.) • Advanced I/O — block data and DMA use • Interfacing with analog devices • Annotated work sheets for designing and implementing your own application

$495.00 TOTAL PRICE

INCLUDES: 8080A training microcomputer, educational monitor, coordinated 650-page training text with exercises, software, flowcharts, block diagrams and schematics.
Optionally, a separate power supply(+5V-1.5A, +12V-0.8A) is also available for $95.00.

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Integrated Computer Systems, Inc.
Self-Study Training Dept.
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CIRCLE 104 ON INQUIRY CARD

Integrated Minifloppy/ Microcomputer System Increases Throughput

Featuring single or dual minifloppy disc drives with controller and interface, the System 8 is a powerful microcomputer for both applications and development. A single minifloppy disc has storage capacity of 80k bytes of formatted data in single density.

Hardware includes a 1.3-μs 8080A processor, 16k/64k RAM module, serial/parallel I/O, and front panel for control and display. Utilization of the higher speed of the 8080A results in a 30% increase in throughput over other 8080A systems.

Software includes resident p/ROM monitor, complete disc operating system with file management, editor, assembler, and dynamic debugger. PLM, BASIC, FORTRAN, and other high level languages are available.

As part of the GNAT-PAC series from GNAT Computers, 7895 Convoy Ct, Unit 6, San Diego, CA 92111, the system comes assembled and tested in a 5.25" (13.34 cm) high cabinet. It is compatible with the series' line of memory and I/O support modules.

Circle 193 on Inquiry Card

Floating Point Chip Gives Arithmetic Powers to 8080 Microcomputers

Designed to interface with Intel 8080-based microcomputer systems, the FP708 is a single-chip floating point arithmetic package. Novonics, 602 Sciandro Dr, Greensburg, PA 15601 developed the chip for the Intel SBC 80/10 or SDK 80 systems; it plugs into one of the 8k p/ROM sockets located on the 80/10 board. The chip is also compatible with the 8708 EPROM.

Faster than a calculator chip, this device is accurate up to five digits and requires no scratchpad memory. It performs 16-bit binary floating point arithmetic, and executes (16-bit) binary-to-BCD (5-digit), BCD-to-binary, floating-to-fixed point, fixed-to-floating point conversions, and utility operations. Typical execution times for the most common routines are 0.4 ms for addition, subtraction, floating-to-fixed and fixed-to-floating point conversions; 1.2 ms for multiplication and squares; 1.8 ms for division; and 6.5 ms for square roots.

No additional memory overhead is required to support the chip except for a maximum 26 bytes of stack memory. The package is designed for OEM applications where both software density and speed of execution are important. The FP702, a 4-chip set designed for use with the 1702A EPROM, will be available soon.

Circle 194 on Inquiry Card

Analog Input Component Is Bus-Compatible Solution for µProcessors

Providing microprocessor system designers with a solution for analog data acquisition tasks, the MP20 analog input microperipheral is a hybrid 80-pin quad-in-line package. It consists of a 16-channel analog multiplexer, high gain instrumentation amplifier, and 8-bit A-D converter, plus all necessary address, data, and control bus interfaces.

The device is timing and logic level compatible with 8080A and 8008 type microprocessors. No external logic is needed. Gain and offset are internally laser-trimmed, eliminating the need for external adjustments while providing absolute accuracy better than ±0.4% (1 LSB) on the ±5-V or 0- to 5-V ranges. Other compatible devices are the 8085, 8048, Z80, and SC/MP.

Low level signals such as thermocouple outputs can also be handled directly with reduced accuracy. The instrumentation amplifier can be programmed with a single external resistor to provide input signal ranges as low as ±10 mV FS.

Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734 has simplified programming and allowed for unlimited channel expansion by treating the component as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used to access data. Thus, one LDA instruction will input data from one channel to the accumulator. Two adjacent input channels can even be acquired with one LHLD instruction. Alternately, the peripheral can be interfaced as I/O.

Housed in a 1.7 x 2.1 x 0.15" (4.3 x 5.3 x 0.38 cm) ceramic package, the system is specified over a 0 to 70°C temperature range. Power requirements are ±15 and 5 Vdc.

Circle 195 on Inquiry Card

8080 Instruction Timing Reference Card Saves Design/Debugging Time

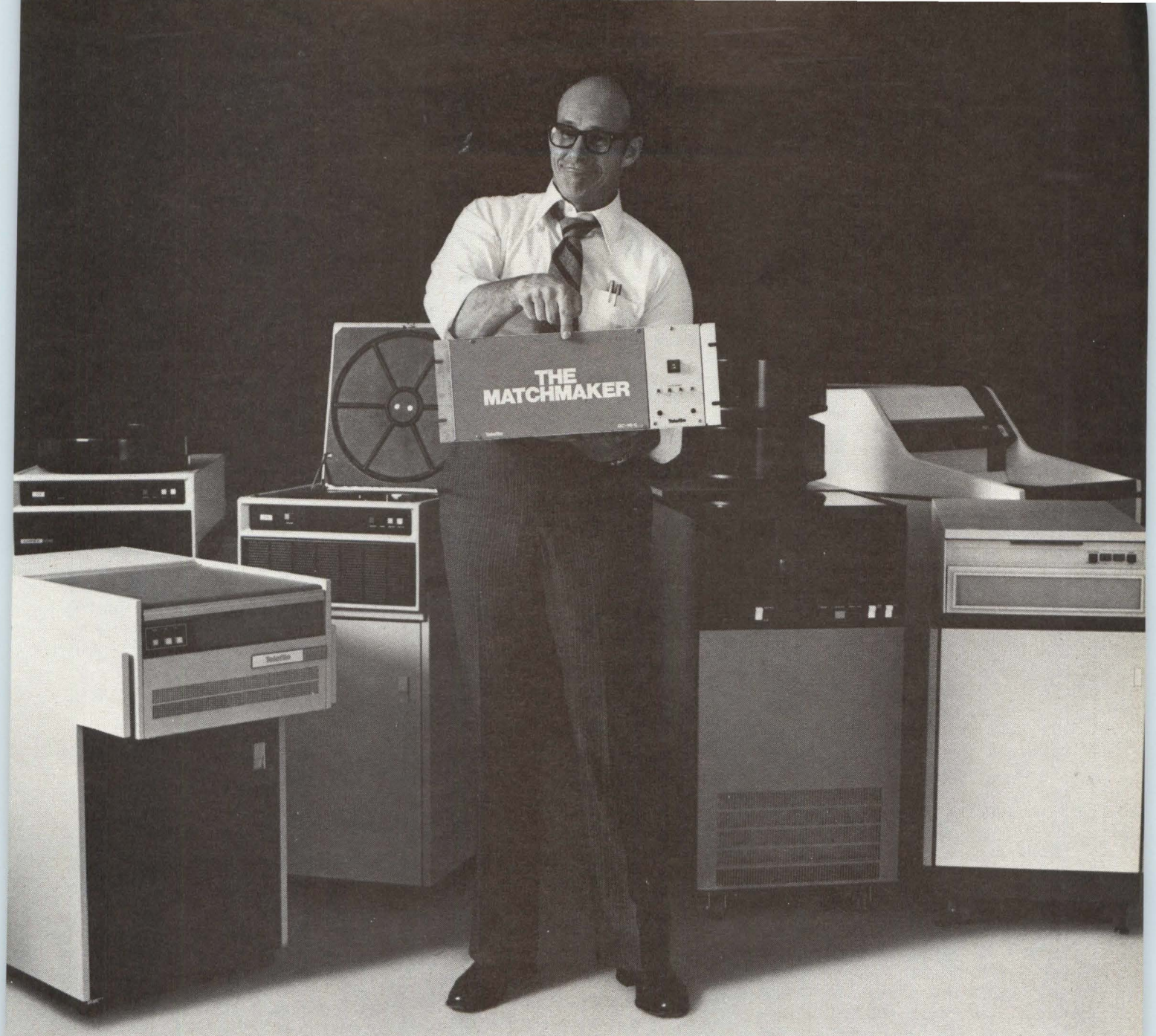
Microcomputers are commonly used in applications where program execution speeds must be accurately known. This analysis has been accomplished by approximation or by trial and error. A software design aid has been introduced by Pragmatic Systems, PO Box 43, Mountain View, CA 94042 to simplify this analysis, helping 8080 users compute execution times for speed critical program sections.

The 8.5 x 11" (21.6 x 27.9 cm) 8080 instruction timing reference card presents instruction execution times and characteristics of all 8080 instructions in an easy-to-use format. General timing equations are included along with precomputed execution time columns for 8080 systems with a 2-MHz clock and memory access times from 0 to 1500 ns.

One specific problem involved with microcomputer applications is timing analysis of systems with different speed memories. This often occurs when programs are stored in ROM and data are stored in RAM. Failure to account for these speed differences can result in timing errors of over 40%. The card simplifies this analysis by indicating the number of accesses each instruction makes to both read-only and read/write memory, and by providing precomputed execution times for these split-speed memory applications.

The back of the card contains instructions and equations for computing execution times of existing programs in any 8080 system. It also shows how to use the card to design program delay loops with specific execution times. Small sample programs are included as examples. □

Circle 196 on Inquiry Card



Very little stands between your mini and the disk drives of your choice.

Just Telefile's little Matchmaker disk controller. With it, we can put your minicomputer together with *any* of the latest 3330-type disk drives: Ampex, Memorex, CalComp, Control Data, or Diablo. You'll have a system no one else can match.

Greater flexibility.

Special tailor-made, compatible interface modules make changing minicomputers a snap.

To change drives, simply switch circuit boards. Capacity can grow from 13.3 million to 1.2 *billion* bytes per system.

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Telefile even provides handlers that make the Matchmaker software transparent to the operating systems of most major minicomputers.

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100 fact-filled pages on the universal Matchmaker concept including operation, functional specs, features, diagnostics, installation, and maintenance. Get it free by writing: Telefile Computer Products, Inc., 17131 Daimler St., Irvine, CA 92714. Or call toll-free (800) 854-3128. In Calif., (714) 557-6660.

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CIRCLE 105 ON INQUIRY CARD

AROUND THE IC LOOP

Low Power 4k and 16k Dynamic RAMs Have Standard Pinouts

Low power, 16k and 4k dynamic RAMs and custom memory board design and manufacturing services have been introduced by NEC Microcomputers, Inc, 5 Militia Dr, Lexington, MA 02173. Addition of the uPD416 16k x 1 dynamic RAM and the 18-pin uPD418 4k x 1 dynamic RAM allow the company to offer all standard pinouts—16, 18, and 22—of 4k dynamic RAMs and the standard 16-pin 16k RAM.

The 16k RAM is available in both plastic and ceramic packages. It uses non-latched outputs. Maximum access times are 150, 200, 250, and 300 ns for the four units in the family. Operating current is 35 mA, and the 12- and ±5-V power supplies have 10% margins.

The 18-pin uPD418 4k x 1 RAM has access times of 150, 200, 250, and 300 ns. It requires an operating current of only 28 mA and 12- and −5-V power supplies, which have 10% operating margins. It is available in both plastic and ceramic packages.

Customized memory boards using 4k and 16k components will be custom designed, built, and tested for customers. Board size will be a minimum of 4k words and may range to 64k or 128k words depending on requirements. This service will reduce design development and testing time for companies that require various sized memory boards. Turnaround time for a test board will depend on accurate definition of the board to be built.

5-V 16k UV-EPROM Has Improved Specs Over 2k and 8k Predecessors

A 16,384-bit ultraviolet-erasable programmable read-only memory (UV EPROM) with 5-V supply is said by its manufacturer to be the industry's densest as well as the easiest to use in both read and programming modes. An extension of a family of EPROMs based on floating-gate, avalanche-injection, metal-oxide semiconductor (FAMOS) technology, the 2716 is organized as 2048 x 8 bits. It is a double layer polysilicon n-channel MOS device.

For normal read operations, the device requires only one 5-V supply. In the programming mode, a 26-V supply is still required, but TTL level input, control, and output levels have been implemented to greatly simplify programming procedures. In addition, there is no requirement for externally switching the 26-V supply to obtain the pulsed signal necessary for programming storage cells. The high level pulsed signal required to induce charge transport of electrons to the floating gate in the cell via avalanche injection is generated on-chip.

Access time is 450 ns, power dissipation in the read mode is 525 mW, and per bit power dissipation is 0.03 mW—in all cases equal to or better than the ratings for respective specification of 2k and 8k UV EPROMs. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 also states that the single power supply feature in the read mode makes this EPROM more compatible with the single-supply advanced microprocessors and microprocessor-based systems. A unique standby power mode enables the device to be deselected for operation at one-fourth its normal power dissipation when not in the read mode—about 125 mW, or 0.007 mW/bit.

The device features single location programming as well as single pulse programming. Programming time for all words is about 100 s; programming time for one word is 50 ms.

The 24-pin package is plug-compatible with the company's 2316E mask-programmable 16k ROM. Users can debug systems with the 2716 and, as soon as the data pattern is firm, order ROMs to plug directly into the 2716/2316E socket. In addition, the initial systems can be shipped with EPROMS and field-fitted with ROMs when they become available.
Circle 169 on Inquiry Card

QA Program Assures High Level of Functional Logic Circuit Devices

Buyers and specifiers of Schottky TTL, standard TTL, low power Schottky, ECL, and interface logic components are now offered a no-cost quality assurance program. Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 claims that its SUPR II commercial upgrading program will guarantee that 999 out of 1000 units will be functional, a high for functional acceptable quality level (AQL) guarantees on logic circuits.

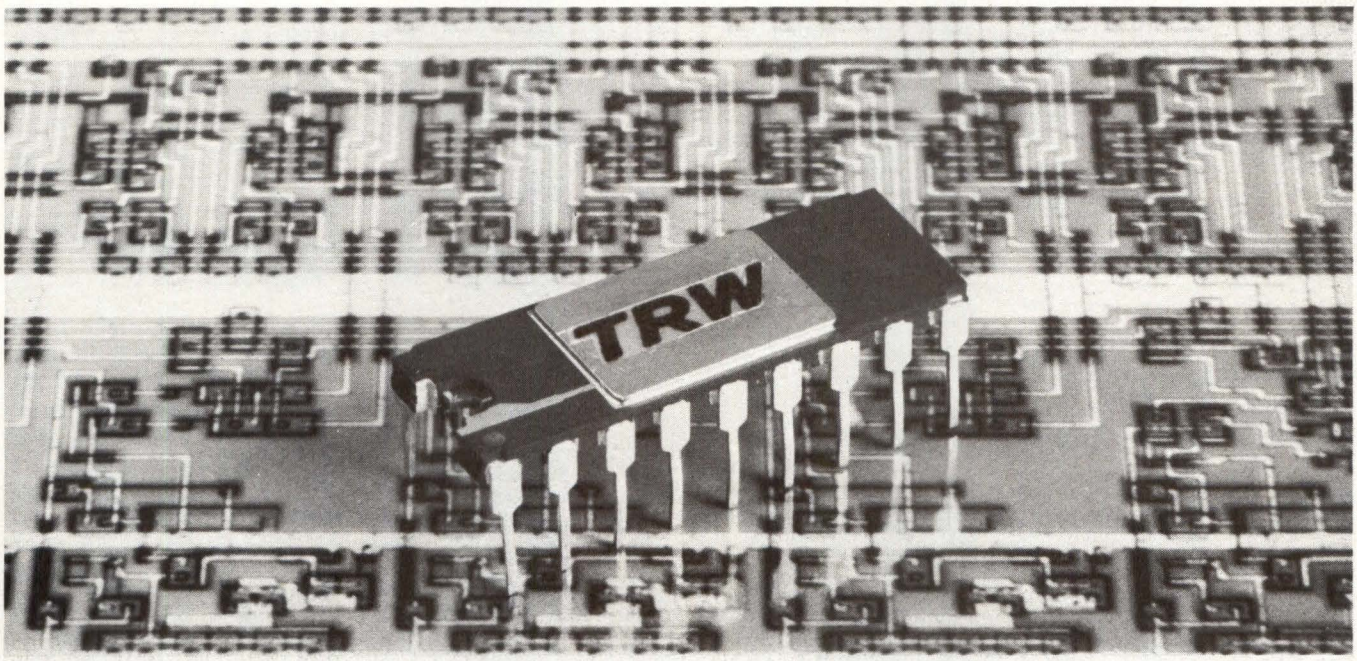
Two program levels are designed to cut user costs in inspection, outside testing laboratories, board rework, warranty repairs, and field service. Level A, standard on all IC products, includes SEM wafer quality monitor, MIL-STD-883 die and preseal visual inspection criteria, MIL-STD-883 thermal shock preconditioning, 100% testing, 100% high temperature testing, and tight commercial outgoing criteria. Level B, an optional program for maximum reliability, includes level A processing plus a 100% burn-in to MIL-STD-883A method 1015. This program also applies to analog, bipolar memory, and MOS products. It specifies AQL guarantees for hot opens, dc and ac parametric testing, mechanical testing, and sealing (for ceramic and metal packages).
Circle 170 on Inquiry Card

LSI Chip Controls and Interfaces Dot Matrix Printer

An LSI printer controller chip which controls and interfaces to a dot matrix printer made by LRC, Inc, Riverton, Wyoming, P/N RC7000 replaces 40 TTL SSI packages, otherwise required to implement the printer's control logic, as well as an MSI ROM character generator, reducing the cost of materials and assembly by about 60%, or from approximately $50 to under $20 for comparable quantities.

In addition to interfacing the printer with PPS-4 and -8 microprocessor systems, Rockwell International, Microelectronic Device Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803 designed the LRCC controller chip for use directly with other host microcomputers, and to be TTL or CMOS compatible. The chip accepts 64 ASCII characters via either serial or parallel data channels from the host system, with each 8-bit byte representing either a printable character or one of eight instruction codes. Upon receiving a print command, the LRCC initiates a print cycle, empties its line buffer, and prints out in the left to right direction up to forty 5 x 7 dot matrix characters per line. (The character generator is internal.) If a double-width character print is re-

8-Bit high-speed monolithic A/D



Priced under $100

TDC-1002J	**1000 ns**	**$75 in 100's**
TDC-1001J	**400 ns**	**$175 in 100's**

Two performance ranges—400 and 1000 ns conversion times: two price ranges for a wide variety of high-speed A/D applications.

Linearity is ± 1/2 of LSB. Nine clock periods per conversion. All output bits are ready one clock period after the status signal indicates "ready to convert." There are no missing codes — ever!

TDC-1001J and TDC-1002J are supplied in an 18-pin ceramic DIP package designed to operate at a commercial temperature range of 0° to 70° C.

For more information and complete specifications, call (213) 535-1831, or use this coupon.

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CIRCLE 106 ON INQUIRY CARD

quired, up to 20 double width characters are generated per line, and a mix of single- and double-width characters is allowed.

By taking advantage of the operational timing of the LRC printer, the chip allows a continuous print mode that utilizes 100% of the printer's print time. It also provides control over the paper-form hold solenoid, and senses top of form, print head, and paper feed switches for proper operation of the printer. Four straps (pins) allow variable/programmable solenoid on-time.

Circle 171 on Inquiry Card

4k Static RAM Offers 310-ns Cycle Time, 27-mW Standby Power

With 200-ns access and 310-ns cycle time and 165-mW active and 27-mW standby power dissipation, the MK 4104P-3 is claimed to have the industry's lowest speed/power product for a 4k x 1 static RAM. The unit is directly TTL-compatible with an input 1 level of 2.0 V and 0 level of 0.8 V. Output will drive four TTL loads in addition to 100 pF.

Automatic standby power is achieved by forcing chip enable to an inactive state and reducing standby power to 27 mW max. Further reduction occurs when V_{cc} is reduced. With this mode of operation, data retention is maintained at less than 0.3 μW/bit (type), allowing a true battery backup static RAM system.

The MK 4104 is available from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 in the industry standard 18-pin ceramic package; price in quantities of 100 or more is $18.75 each.

Circle 172 on Inquiry Card

Low Cost Hybrid ADC Performs 12-Bit Conversion in 20 µs

Model ADC-HX12BGC analog-digital converter is claimed by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 to include many performance features found only in higher priced modular converters. It performs a 12-bit conversion in 20 μs while maintaining a $\pm\frac{1}{2}$ LSB linearity and 20-ppm/°C maximum temperature coefficient.

Universal performance features include: five pin-selectable input voltage ranges (0 to 5, 0 to 10, ±2.5, ±5, and ±10 V), binary or offset binary output coding with 2's complement coding also user-selectable in bipolar operation, varied input impedance depending on the voltage range selected, and high impedence internal buffer providing 100-MΩ input impedance. The device can be short-cycled for lower resolution conversions at higher speed; eg, it can be connected for a 10-bit conversion in 15 μs and an 8-bit conversion in 10 μs.

Successive approximation is used for conversion. Matched quad current switches are combined with laser trimmed nichrome thin film resistors to give optimum linearity and a 2-ppm/°C differential linearity tempco. There are no missing codes over the operating temperature range.

The 1.1 x 1.7 x 0.2" (2.78 x 4.32 x 0.51 cm) device is manufactured in a 32-pin, hermetically sealed glass package. Power supply requirement is ±15 and 5 V; operating temperature range is 0 to 70°C. Extended temperature range models are also available. Pricing in 1 to 24 quantity is $85.

Circle 173 on Inquiry Card

Laser-Trimmed Voltage Reference Has Only 1% Output Variation

A stable 2.5-V reference source, MC1403/1503 is designed for critical instrumentation and D-A converter applications. The low cost monolithic circuit features a maximum output voltage variation of only 1% (±25 mV) and a typical tempco ($\Delta Vo/\Delta T$) of 10 ppm/°C.

Laser trimming of resistive networks as a routine process during normal manufacture provides a high yield to a very tight tolerance specification. The laser trimming process adds to the probing time and requires a small amount of additional real estate (compared with untrimmed chips), but effectively increases the tight-tolerance yield to the point where the small cost increase is insignificant compared to the overall cost reductions made possible.

The chip represents the first utilization of a p-channel J-FET in a linear IC at Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Ion implantation technology provides the capability. Circuit specifications include line regulation of 3 mV (max) at input voltage from 4.5 to 15 V, 4.5 mV (max) at input voltages from 15 to 40 V; and load regulation of 10 mV (max) at output currents from 1 to 11 mA.

Units are available in both plastic and ceramic packages. Typical prices in 100 to 999 quantities range from $1.50 to $4 for a commercial temp range device in a plastic package; and from $5 to $12 for a military temp range device in a ceramic package.

Circle 174 on Inquiry Card

4k-Byte Memory Cards Meet Low Cost Needs for µP Applications

NS 400-N series self-contained 4k-byte n-MOS memory cards, incorporating MM2102 1k-bit static RAMs, are offered as alternatives to eliminate the usual design-prototype-test cycles. According to National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, the cards do not require clocks or refresh signals. They are available in 8-, 9-, or 10-bit versions and with 550- or 330-ns access times.

The only requirements for use with the cards are memory enable, address, read-and-write, and data (all TTL-compatible) and a single 5-V power supply with 1 A for each card. Independent 3-bit addressing for each card permits plug-in expansion to an 8-card, 32k-word memory system. The card address is programmable via the connector wiring.

Data in and data out have the same polarity and the read operation is nondestructive. Tri-State® outputs simplify busing by keeping impedance high when the card is not being addressed, and allow easy expansion of bus interfacing.

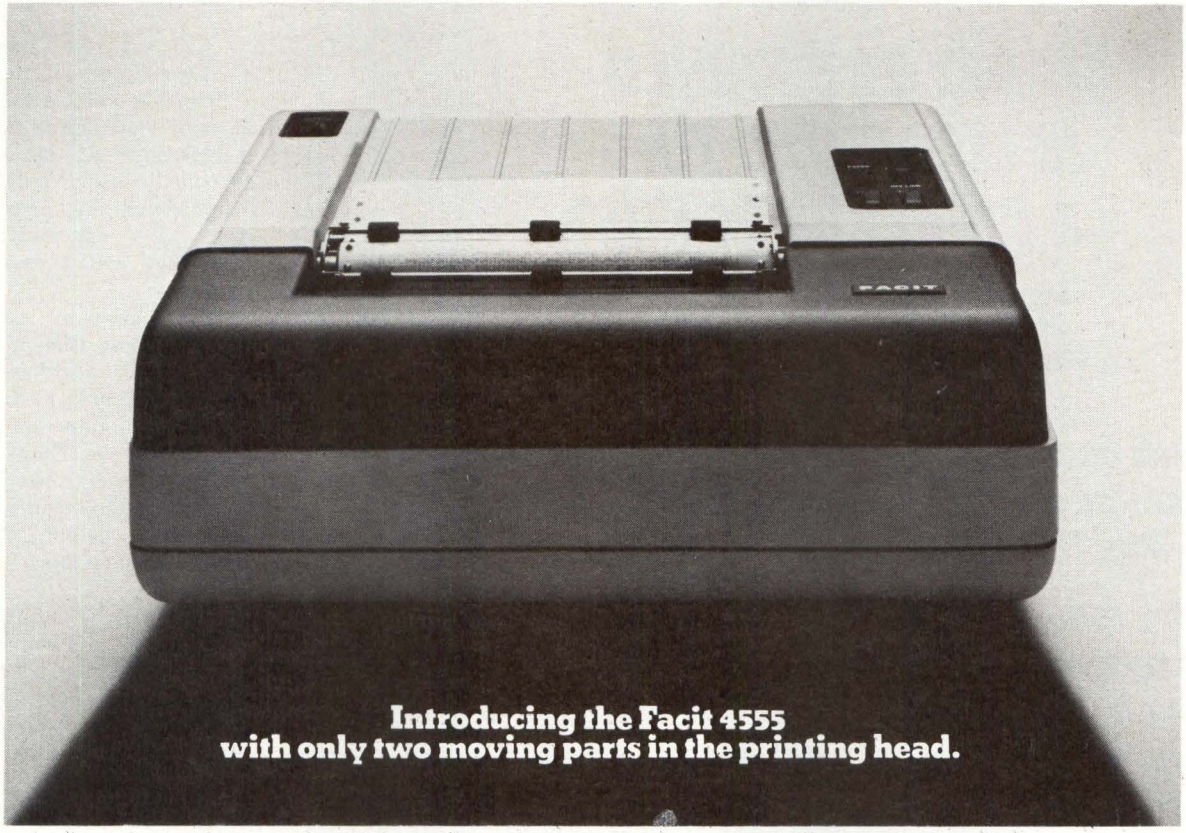
The 4k x 10-bit, 550-ns version, on a 3.93 x 6.3 x 0.5" (9.98 x 16 x 1.27 cm) card sells for $200 in 100 quantities. Simple interface and low cost are said to target the memory cards for microprocessor system applications.

4-Channel Optical Coupler Achieves 300% CTR With 0.5-mA Input Current

HPCL-2770 has four GaAsP LEDs, each optically coupled to a corresponding high gain photon detector,

The Facit 4555 Page Printer.

Fewer moving parts are a moving argument.



Introducing the Facit 4555 with only two moving parts in the printing head.

The rationale: fewer parts moving around means fewer parts wearing out.

But we didn't stop there.

We also gave considerable thought as to how well our page printer should produce a print-out.

So, unlike most page printers, our 4555 uses a character by character (asynchronous) print-out and an automatic ribbon control to give you big, easy-to-read characters at 6 or 60 characters per second.

And whether you need one, two or even three copies, your print-out will always come out crystal clear.

Our 4555 is even less trouble to hook up than most page printers. That's because we give you several interface versions. Among them are: The Facit SPI interface for bit parallel data transfer, and the EIA, RS 232C.

All things considered, the Facit 4555 page printer is one of those rare instances where less for your money is really more for your money.

Facit-OEM Division,
66 Field Point Road,
Greenwich, Connecticut
06830.

FACIT
Dedicated to Efficiency

See us at the N.C.C. Show in Dallas, Booths 1670-72-74

CIRCLE 107 ON INQUIRY CARD

in a single, hermetically-sealed package. Current transfer ratio (CTR) of 300% is achieved at an input current of only 0.5 mA. Output saturation voltage is typically 0.1 V.

Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, designed the units for use in MOS, CMOS, and low power interfacing, or RS-232-C data transmission systems. The devices assure compatibility with high voltage CMOS by the 18-V supply voltage and guaranteed maximum output leakage of 18 V. Low input current requirement adapts to use in portable equipment where low power consumption is necessary.

Use of a common V_{cc} pin for the photodiodes and the first stage of each detector results in lower output saturation voltage and higher speed operation than conventional photoDarlington type optocouplers. Also, the separate V_{cc} pin can be strobed low as an output disable or operated with supply voltage as low as 1.6 V without affecting performance.

Use of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage current to ground results in high temperature performance. Performance is guaranteed from −55 to 100°C ambient. The 4-channel optocoupler is priced at $44 each in quantities of 100.

Circle 175 on Inquiry Card

High Performance 6-Bit DAC Has ½ LSB Accuracy

DAC-01D is a complete monolithic digital-to-analog converter, which includes a precision voltage reference, current steering logic, current sources, resistor ladder network, and an operational amplifier. This addition to the DAC-01 series from Precision Monolithics, Inc, 1500 Space Park Dr, Santa Clara, CA 95050 has ½ LSB accuracy.

Power consumption of 250 mW max and fast settling time make the unit useful in servo positioning controls, digitally programmed power supplies, pulse generators, and data sets. The device is specified over the 0 to 70°C commercial temperature range. Maximum nonlinearity, specified over that range is ±0.78% of full scale, and full scale tempco is ±160 ppm/°C.

Concurrent with this addition, the DAC-01A ⅛ LSB grade has been dropped. All grades having ¼ LSB accuracy have been retained. In a 14-pin hermetic package the unit is priced at $6.50 ea in 100 to 999 quantity.

Circle 176 on Inquiry Card

Dual Differential Comparator Now Second Sourced

A second source for the National Semiconductor Corp LM2903 dual differential comparator has been announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. Devices operate over 2- to 36-V and −40 to 85°C ranges. They are compatible with TTL, DTL, MOS, and CMOS and are available in 8-pin plastic and ceramic DIPs as well as in 8-pin metal can packages. Prices are $0.96 each for the plastic version and $1.39 for the others in 100-piece quantities.

Circle 177 on Inquiry Card

Trade Association Formed by Semiconductor Manufacturers

Spurred by the growing array of government and regulatory problems being encountered, major semiconductor manufacturers have formed the Semiconductor Industry Association as a trade organization for their industry. The founders described the association's initial focus as gathering reliable industry statistics and examining critical government relations at both State and Federal levels.

Executive committee of the association will include W. J. Sanders, III, president of Advanced Micro Devices, Inc; Wilfred J. Corrigan, president of Fairchild Camera and Instrument Corp; Robert N. Noyce, chairman of Intel Corp; John R. Welty, vice president, Motorola, Inc; and Charles E. Sporck, president of National Semiconductor Corp. Bernard T. Marren, former president of American Micro Systems, Inc, was named executive director. Headquarters offices will be located in Santa Clara County, California.

High Speed Op Amp Performs Over Wide Bandwidth

Offering wide bandwidth performance, fast slewing rate, and well behaved dynamics for use in high speed applications, the 9912 is intended for use in data acquisition and graphics systems. Packaged in a standard 14-pin DIP, the device is specified to provide a min $\pm 600\text{-V}/\mu\text{s}$ slewing rate and an 800-MHz min gain bandwidth product.

Settling time is given as 150 ns max to 0.1% error with a 200-ns max overload recovery time. Standard output swing is ± 10 V at ± 20-mA load current. Minimum open loop gain at dc is 60 dB. Operating temperature range is -55 to 125°C. Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734 is offering the devices for $41 each (1 to 2), $37 each (3 to 9), and $33.50 each in 10 to 29-piece quantity.

Circle 178 on Inquiry Card

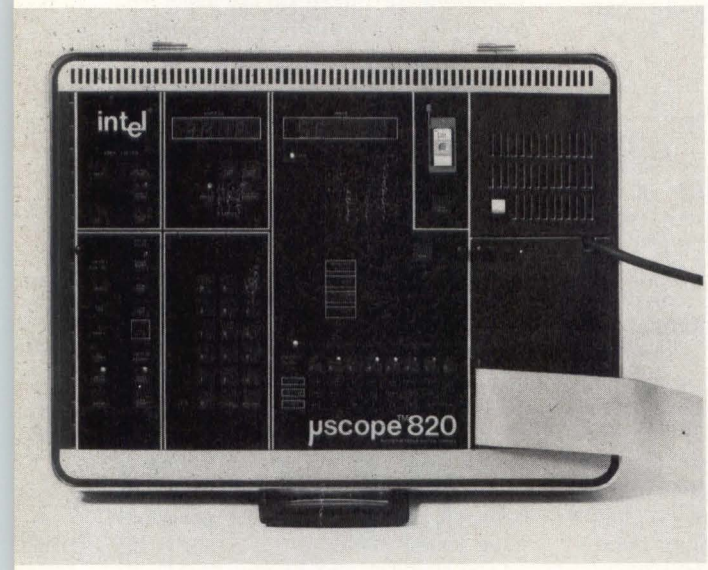
Semiconductors Will Maintain Historic Price/Performance Trends

Technical achievements in logic circuits, main memories, and mass storage will pace continued improvements in large computer system price/performance ratios, according to Dr. Warren Gaines, director of advanced marketing programs for Honeywell Information Systems, PO Box 6000, Phoenix, AZ 85005. Speaking before the Canadian Information Processing Society's March symposium, in Toronto, Canada, Dr. Gaines said denser and faster semiconductors will allow the historic 12 to 15% annual price/performance ratio to continue into the 1980s. He also predicted similar trends for data storage devices, where rotating magnetic media retain the potential for substantial density increases that should lower cost per stored bit.

"Higher levels of integration and attendant lower costs per gate in logic circuitry are now being combined with new methods of packaging faster semiconductors," Gaines said. "Experience in developing Honeywell's Model 66/85 computer system proved that very fast current mode logic chips, when placed in dense micropackages, can deliver speed increases up to 500% from less than 1/15th the space." These densities are important as designers work with nanosecond processing speeds, he said, and added: "Equally as dramatic are memory chip trends. The semiconductor industry has been able to develop MOS enhancements to support a 25% plus improvement per year in the cost/bit for large system main memories."

Transition from core memories through various MOS memory sizes to current 4k bit chips has been accompanied by a substantial reduction in the physical size of memories by 20 to 1. "Where core memories required 40 ft^3 for 256k words of memory, 4k technology allows packaging 1M words in only 8 ft^3 today." That trend continues with some semiconductor manufacturers delivering prototype quantities of 16k-bit chips today. Projections are for 64k and even 128k-bit offerings by the end of this decade. "By the 1980s, these trends will result in substantial changes in memory use," Gaines predicted. "As the price of 256k words of memory approaches the monthly salary of a programmer, data processing managers will be re-evaluating the tradeoffs between memory use and programming time." □

PRODUCT FEATURE



Portable System Enables Online Debugging of Microprocessor-Based Equipment

Both service personnel who are relatively unfamiliar with microprocessors and those who have had extensive experience have been considered in the design of the μScope™ 820 microprocessor system console. This portable, self-contained instrument from Intel Corp provides the critical control, monitoring, and interaction required for maintenance and repair of microcomputer-based systems. Although human-engineered for the laboratory, production line, or field technician to the extent that it will prompt the operator, it also serves as a powerful analytical tool when used by sophisticated test personnel for troubleshooting difficult problems.

In principle, it is similar to the in-circuit emulation approach to system debugging for use with Intellec® microcomputer development systems. However, the microprocessor system console is a standalone, self-contained maintenance processor. It requires only a personality probe—specifically designed for the particular microprocessor in the system under test. At present the only probe available is for use with 8080A microprocessors, but other probes will be available for systems using other microprocessors.

Maintenance Console

Complete control over operation of the microprocessor (CPU) in the system under test (SUT) is maintained at all times by the maintenance console. The console can force the CPU to halt, single step, reset, run real-time, or run real-time with periodic display data collection (10 times/s). All such CPU commands are given without interference to other operational parameters or diagnostic sequences that have been set up.

Address information is shown in a 4-hexadecimal-digit display. Included are address of any memory location the user wishes to examine, number of any I/O port defined in the SUT, addresses of any overlay memory location and of overlay memory origin assignment, address at which breakpoint is to occur, address portion of breakpoint mask, and address of given trace record element. Once the operator has initiated a given memory, trace, or I/O examination, the examination can continue sequentially in either ascending or descending address value.

Hardware breakpoint allows the operator to alter normal SUT program flow without any throughput degradation of the SUT. All 32 bits of the breakpoint condition word are maskable, and the condition can therefore be as specific or as general as desired.

Occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or recording of a single cycle of trace data. All such options are key-selectable prior to enabling the breakpoint.

Following a breakpoint match, the operator can select a number of diagnostic operations by pressing an action key and then entering on the hexadecimal keypad the assigned value of the specific action desired. Further keypad entries specify parametric value of the selected action (such as number of breakpoint pass counts or start address of a subroutine call following a breakpoint). Trace control logic is used to record a single cycle of trace data when a breakpoint occurs.

An overlay memory enables the test unit to map its memory onto SUT memory space, and to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. Resident subroutines are executed without SUT wait states; subroutines can be entered through either the hexadecimal keypad or a ROM-p/ROM socket on the front panel. The operator can set the SUT to execute special maintenance or troubleshooting programs.

A full 32-bit trace memory records 256 cycles of CPU operation without delays in SUT processing. It provides information about CPU operation just prior to a CPU halt or the start of a panel freeze initiated through a panel key.

Data can be recorded on all CPU

cycles or only when CPU program execution generates a breakpoint match. Once data are recorded, sequential examination of those data is possible via a panel key.

Selection of information, such as address or control variable entry that the operator may want to change or examine, can be made through orders on the hexadecimal keypad. The operator then can either enter further data or discontinue the display if only an examination was wanted. The operator is prompted by the console with indications of the specific information expected if multiple value data entries are needed.

Value displays, with the address display, provide simultaneous readout of trace vectors, breakpoint conditions and mask values, memory location, and I/O port contents. Other selectable readouts include all single and double register values, state of CPU pins and flags, information on course of action following occurrence of a breakpoint, and information on the breakpoint pass count. Information displayed is selected through the hexadecimal keypad and any of 11 dedicated examine keys, and is shown either statically or continually updated 10 times/s.

A reset key allows breakpoint and overlay memory to be disabled, clears registers, and aborts specific examine modes, resetting the instrument for another test sequence. The operator also can initiate self-test sequences via a panel key. These sequences check proper operation of most of the instrument.

ROMs or p/ROMs storing preprogrammed test subroutines fit into a front panel socket. Of the 2048 available bytes of ROM, 128 identify up to 16 separate subroutines and define specific instrument states and conditions under which the subroutine will be called; the remaining 1920 bytes, along with 128 bytes of RAM contained in the console, are usable program space. Each subroutine is enabled by a select key and the hexadecimal keypad.

For situations where operator recognition will be enhanced by a binary presentation, a binary display shows all 8-bit values in parallel with the hexadecimal display. Selection procedures are the same for both. Once a selection has been made, the operator can alter values by making further hexadecimal keypad entries or by changing binary states through binary data switches.

Personality Probe

Although standardized interface logic which transmits and receives various address, data, and control signals between maintenance console and circuitry of a particular probe is intended to function with many of the available microprocessors, the only probe now available is for use with 8080A-based systems. This probe comprises a 6-ft (1.82-m) flat cable, connector, buffer box, personality p/ROM, and particular overlay for the console. A 50-pin mating connector plugs into a board-edge connector in the power card compartment of the console and into a flat-cable connector on the buffer box.

The user unplugs the CPU from the SUT, plugs it into the probe, and then plugs the probe into the CPU socket on the SUT. The probe provides complete control over the SUT, yet causes minimal interference.

Specifications

Electrical requirements for the maintenance console are 100, 120, 220, or 240 V −10% +5%, 110 VA max; 48 to 63 Hz. Power to the probe is supplied by the console. Environmental conditions for both are 0 to 55°C (32 to 130°F) operating temperature, −40 to 75°C (−40 to 167°F) storage, at 95% relative humidity at 15 to 40°C (59 to 104°F) non-condensing. Console dimensions are 18.875 x 15.5 x 6.625″ (47.9 x 39.4 x 16.8 cm); weight is 20 lb (9.1 kg).

Price and Delivery

Price of a μScope 820 microprocessor system console and probe is under $2500. Delivery is 90 days ARO. Intel Corp, Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051. Tel: (408) 246-7501.

For additional information circle 199 on inquiry card.

See at NCC Booth 1605

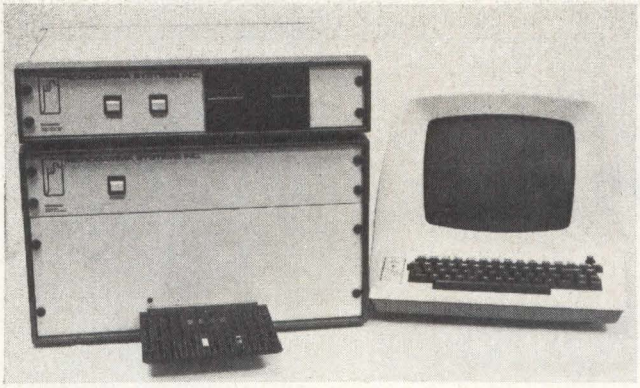
PRODUCTS

Intelligent Magnetic Card Terminal Family Interfaces With Most Computer Systems

Modular intelligent terminals incorporate an ID card reader/encoder with 1- or 2-track head, intelligent controller (8080A) with memory, buffered interface between controller and internal peripherals, V.24 user interface, and power supply. Operating with most computer systems via the standard interface, the units handle ISO, IATA, ABA, and IBM standard magnetic cards, embossed or unembossed, measuring 86 x 54 mm and up to 1 mm thick. Five standard configurations are a simple read/write station (IDT-10) operating strictly under program control, station with three function keys (-20), station with three function keys plus 8-digit numeric display (-30), station with 16-key numeric pad (-40), and -50, complete station with additional 16-point position, alphanumeric printer. The microcode-oriented controller has p/ROM and ROM capability, allowing the terminal to be used as a standalone unit together with external data storage which can be cassette, cartridge, floppy disc, or printer. **Steinmetz•Krischke•Systemtechnik-GmbH,** 75 Karlsruhe 41, Maybachstrabe 10, Germany.

Circle 200 on Inquiry Card

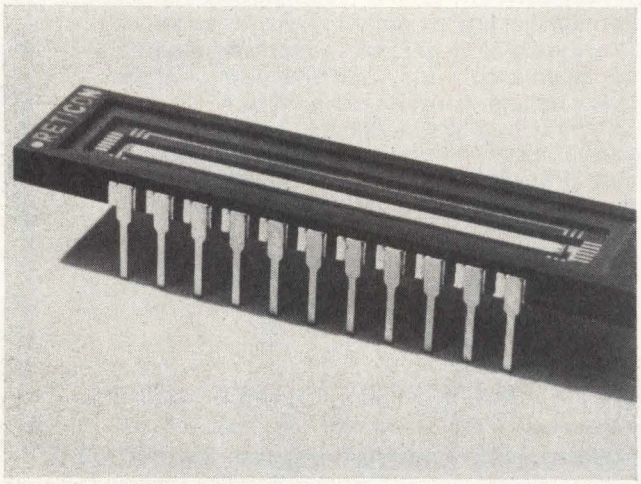
Semiconductor Memory Test System Incorporates Pattern Simulation Feature



MG 3000, designed for production testing of semiconductor memory devices, boards, or systems, incorporates pattern simulation, a hardware aid which simplifies the task of test pattern generation and verification, to give the programmer a means of verifying that the test pattern is actually exercising the memory as intended. Consisting of a microprocessor-based controller and one or more memory test stations, the unit can be modularly expanded. Each station is a versatile pattern processor capable of generating address and data patterns at a 10-MHz test rate. A 16-bit address generator can be expanded to 24 bits and features dynamic field-length definition. A full adder with independent carry-propagation control between each bit allows the address to be segmented into two or more independent fields. Standard 16-bit data word is expandable to 64 bits and can be complemented, shifted, swapped with a standby pattern, or loaded from an external source. Hardware board error mapping allows real-time error logging without affecting test speeds. **Microgamma Systems, Inc,** 260 N Rock Rd, Suite 225, Wichita, KS 67206.

Circle 201 on Inquiry Card

Solid-State Image Sensors Combine Features of CCDs and Photodiode Arrays



While the CCPD's actual sensing aperture is made up of a series of diffused photodiodes, interdigitated on 16-μm centers, readout is provided by CCD analog shift registers. The photogenerated charge integrated on the odd and even elements of this photodiode structure are side-dumped on application of a transfer pulse into two CCD registers which then transfer the charge to an on-chip output charge detection circuit. Since this output has a small capacitance, output signal voltage and S/N ratio are high. Outputs of the two CCD registers are then multiplexed off-chip to obtain a full wave "boxcar" type sampled and held video output. The arrangement offers low capacitance, low noise output of CCDs, along with high quantum efficiency, freedom from blooming, and uniform response of photodiode arrays. They can be used at low clock rates corresponding to integration times as long as 40 ms at room temperature. The devices are designed with 256, 1024, and 1728 elements on 16-μm centers and are mounted in gold ceramic DIPs sealed with an optical quality quartz window. **Reticon Corp,** 910 Benicia Ave, Sunnyvale, CA 94086.

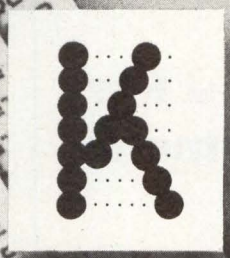
Circle 202 on Inquiry Card

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

Like 300 lpm print quality others can't match.

The Printronix 300 is unlike any other impact matrix printer. Its elegantly simple printing mechanism gives it a greater MTBF than others. Modular design cuts MTTR to minimize downtime. And the basic concept enables it to put a single dot anywhere on the paper, providing full plotting capability — at no extra cost — plus print quality unattainable by any other line printer. All-in-all, it's rather remarkable.

It forms characters by printing one dot row at a time. And it overlaps the dots to produce a solid appearing character, as shown below. Uniform hammer energy dot-by-dot produces clear, crisp dots on the first to last copy of a six-part form, as the actual form pictured demonstrates. No ghosting, smearing or misregistration as often occurs with mechanical font drum/chain/belt printers. And no embossed periods or faint "W"s, either. Just clear, first-to-last copies. After all, printing ought to be easy to read.



The ability to form characters one dot at a time yields another advantage. Simply by plugging in different ROM sets, optional character styles can be accommodated. Various foreign language sets are already available, such as Katakana and Farsi, or you can easily program your own. Send for literature. You'll learn why it prints so well, why it's your best buy, and why we've felt comfortable offering a one-year warranty from the beginning.

Printronix Inc., 17421 Derian Ave., Irvine, California 92714. (714) 549-8272.

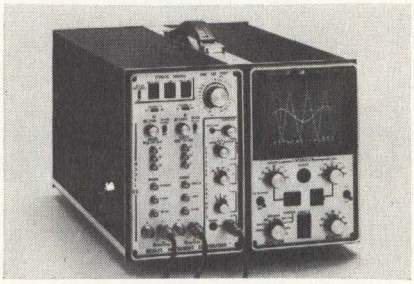
PRINTRONIX 300

It's your best buy!

CIRCLE 111 ON INQUIRY CARD

PRODUCTS

HIGH PRECISION DIGITAL SCOPE



EXPLORER II is designed to replace low frequency analog oscilloscopes, either storage or nonstorage types. Features are nonfading high capacity storage with writing rate equivalents up to 100 cm/μs, depending on plug-in unit; and precision of from 0.4 to 0.025% of full scale. Time resolution is 0.025%. Normalized voltage and time values are displayed for any selected point, true values with respect either to zero or to time and voltage corresponding to any other selected point. Stored waveforms may be displayed superimposed on live waveforms. **Nicolet Instrument Corp, Oscilloscope Div,** 5225 Verona Rd, Madison, WI 53711.
Circle 203 on Inquiry Card

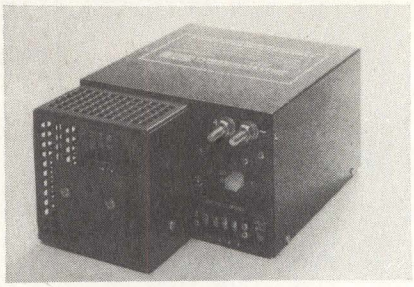
FIELD MULTIPLEXER SYSTEM

A microprocessor-based data acquisition and control unit for serial interface with any computer or ASCII terminal, the series 1500 understands FORTRAN read-write statements. It is ruggedly constructed and light isolated, with hermetically-sealed IC packages for operation in hostile environments. Other features include a range of analog inputs from 10 mV to 10 Vdc, thermocouples and RTD elements, digital I/O circuits, optional dc backup power supply, alarm panels, and a modular design to permit system expansion. **The IPAC Group, Inc,** 3047 Industrial Blvd, Bethel Park, PA 15102.
Circle 204 on Inquiry Card

100-W SWITCHING MINIATURE REED RELAYS

Capable of switching up to 100 W, 1 A, and 200 Vdc, Powermite reed relays are suited for applications such as switching gates of power-switching thyristors, or handling greater lamp and reactive loads. Devices are available in 1- through 4-pole form A open-line and totally sealed encased-line body styles with 0.100 x 1.00" (0.254 x 2.54 cm) or 0.150 x 1.00" (0.381 x 2.54 cm) industry standard terminal spacing. Options include magnetic and electrostatic shielding. **Elec-Trol, Inc,** 26477 N Golden Valley Rd, Saugus, CA 91350.
Circle 205 on Inquiry Card

HIGH POWER SWITCHING REGULATED POWER SUPPLIES

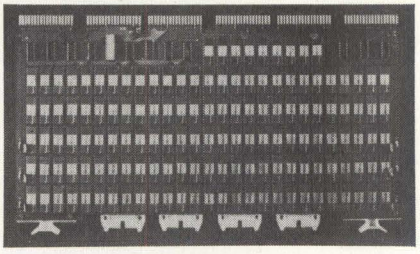


Family of power supplies delivers 25% more power than previous models with voltages ranging from 2 to 28 V and current ratings to 150 A. Operating at 70 to 80% efficiency, the 5 x 8 x 11" (12.7 x 20.3 x 27.9 cm) devices weigh less than 14 lb (6.35 kg), and deliver up to 1 kW power. Units feature dual wide range inputs, 85 to 132 Vac and 170 to 264 Vac at 47 to 63 Hz, and maintain regulation down to 78 and 156 Vac for 10 minutes thus providing complete brownout protection. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 206 on Inquiry Card

LOW PROFILE PCB RELAYS

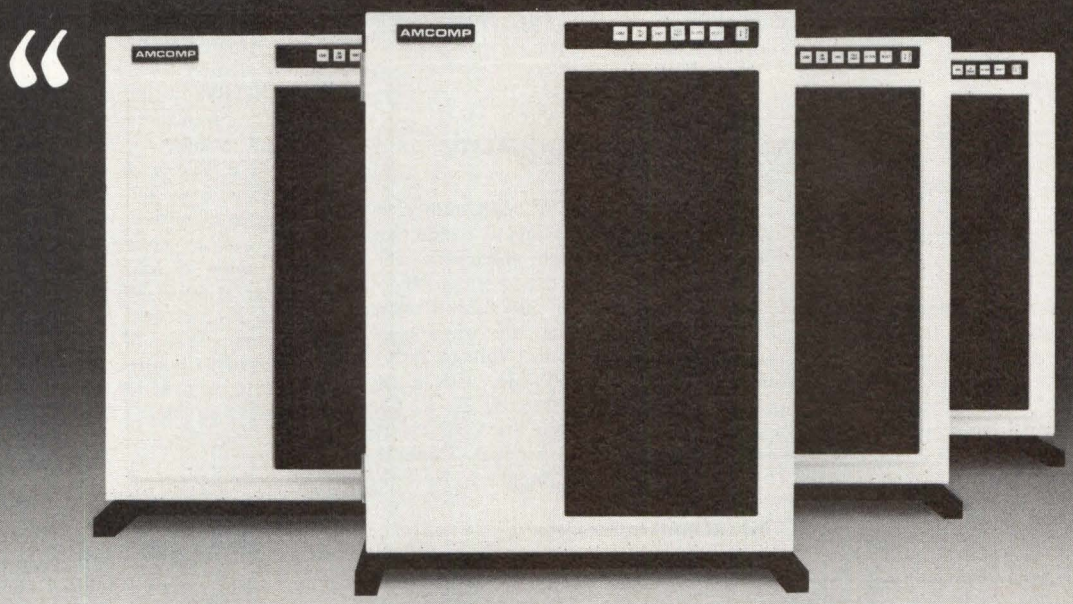
Claimed to have a life of more than 1M electrical operations at 1 A, 30 Vdc and a mechanical life of more than 30M operations, the 0.5" (1.27 cm) high relays feature bifurcated contacts to insure high reliability with both standard and dry circuit capability. Devices are available in dpdt and 4pdt with power consumptions of approximately 0.45 and 0.6 W, respectively. **Impact Electrical Products, Inc,** 7 Westchester Plaza, Elmsford, NY 10523.
Circle 207 on Inquiry Card

MINICOMPUTER ADD-IN FASTBUS MEMORY



The SCAT/45 cuts computer run time up to 60% for PDP-11/45, /50, and /55 users. Minimum configuration consists of one hex-wide 32k-word memory board and control module which monitors FASTBUS and UNIBUS, and derives the timing, multiplexing, and cycle definitions performed by memory modules. It is expandable in 32k-word increments to max of 128k with each increment requiring one board. Switch selectable from 0 to 128k in 4096-word increments, device can be used across entire 124k-word range of the computer. **Able Computer Technology,** 1616 S Lyon St, Santa Ana, CA 92705.
Circle 208 on Inquiry Card

Our commitment to the tape drive market can be summed up this way:



We make four basic tape drives. One of them is just the one you want.

Because the options we've engineered for our basic four effectively give you a choice of over 400 configurations.

Speeds from 12.5 to 125 ips. Tension arm or vacuum column. A variety of electronics options. And more.

Yet with all the differences from drive to drive, there are a number of things the same in every drive.

Simple one-hand loading, dynamic braking, linear sensors and servos, and other engineering advantages.

A near 80% parts commonality. Which makes your spares stocking, training, and servicing a lot easier. An industry-unsurpassed commitment to quality—given meaning by our industry-unsurpassed 13 month warranty. And backed by 24 hour a day, 7 days a week field service.

AMCOMP Tape Drives. Giving you exactly what you want rather than selling you just what we have.

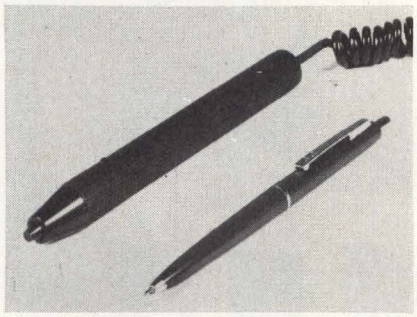
To find out more about the tape drives, or other products and services we have, please contact your nearest AMCOMP office, or AMCOMP, INC., 686 West Maude Avenue, Sunnyvale, CA 94086, phone (408) 732-7330.

AMCOMP. Our strength is our commitment. And our commitment is strong.

AMCOMP

PRODUCTS

ADJUSTABLE LIGHT PEN



Spot brightness sensitivity, which is operator adjustable over a 3 to 1 ratio, is available as an option on the std TTL-compatible light pen which provides "light pen switch" and "light pen hit" signals for interface with the subsystem control logic. Mid-range is set by the factory according to customer specs. Two other options are a coiled cord or non-CRT contact via a "No-Touch" switch option. The latter fingertip switch allows activation of the light pen without having to touch the CRT faceplate. **HEI, Inc,** Jonathan Industrial Ctr, Chaska, MN 55318.
Circle 209 on Inquiry Card

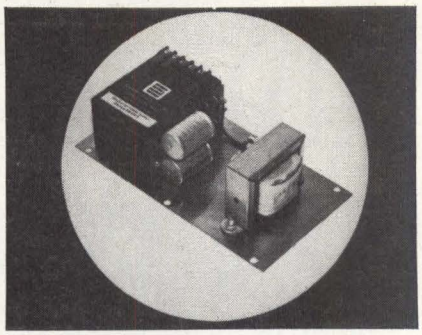
MODULAR VIDEO ADCs

Designed for video digitization, model MATV-0811 converts high bandwidth video signals to parallel digital format with 8-bit accuracy at random or periodic word rates of dc through 11 MHz. Encased in 5.5 x 4.38 x 0.85" (13.97 x 11.13 x 2.16 cm) metal module, unit contains internal 30-ps track-and-hold, encoder, and TTL-compatible output data latch. Analog input is industry std 1 V at 75 Ω. Power requirements are <8 W when unit is operated from ±12, 5, and −5.2 V. It has a relative accuracy of ±0.2% of full scale (±½ LSB). **Computer Labs, Inc,** 505 Edwardia Dr, Greensboro, NC 27409.
Circle 210 on Inquiry Card

SMALL COMPUTER-QUALITY CAPACITORS

Type WHB Computamite® aluminum electrolytic capacitors are welded, computer-grade devices with high volumetric efficiency. Operating in the −40 to 85°C temperature range, the miniature devices offer extensive operating life when used within rated specifications. Voltage rating range is 3 through 450 Vdc, with a capacitance range of 1 through 18 F. Capacitors are polarized but are available in semi- and non-polarized versions. **Cornell-Dubilier Electric,** 150 Avenue L, Newark, NJ 07101.
Circle 211 on Inquiry Card

MICROPROCESSOR AND MEMORY POWER SUPPLIES



Line operated power supplies employ ripple regulation to achieve 70% efficiencies with MTBFs >100 kh and immunity to input line transients of >60 dB. Consisting of four models, the OE series offers outputs of 5 Vdc at 4 A, 5 Vdc at 6.5 A, 12 Vdc at 2 A, and 12 Vdc at 3.5 A—all regulated to within 0.5%, line and load. Units can be user-connected to operate from inputs of 105 to 125 Vac or 210 to 250 Vac at 50 to 440 Hz. Features include output short-circuit protection and operating temp range of −25 to 60°C. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.
Circle 212 on Inquiry Card

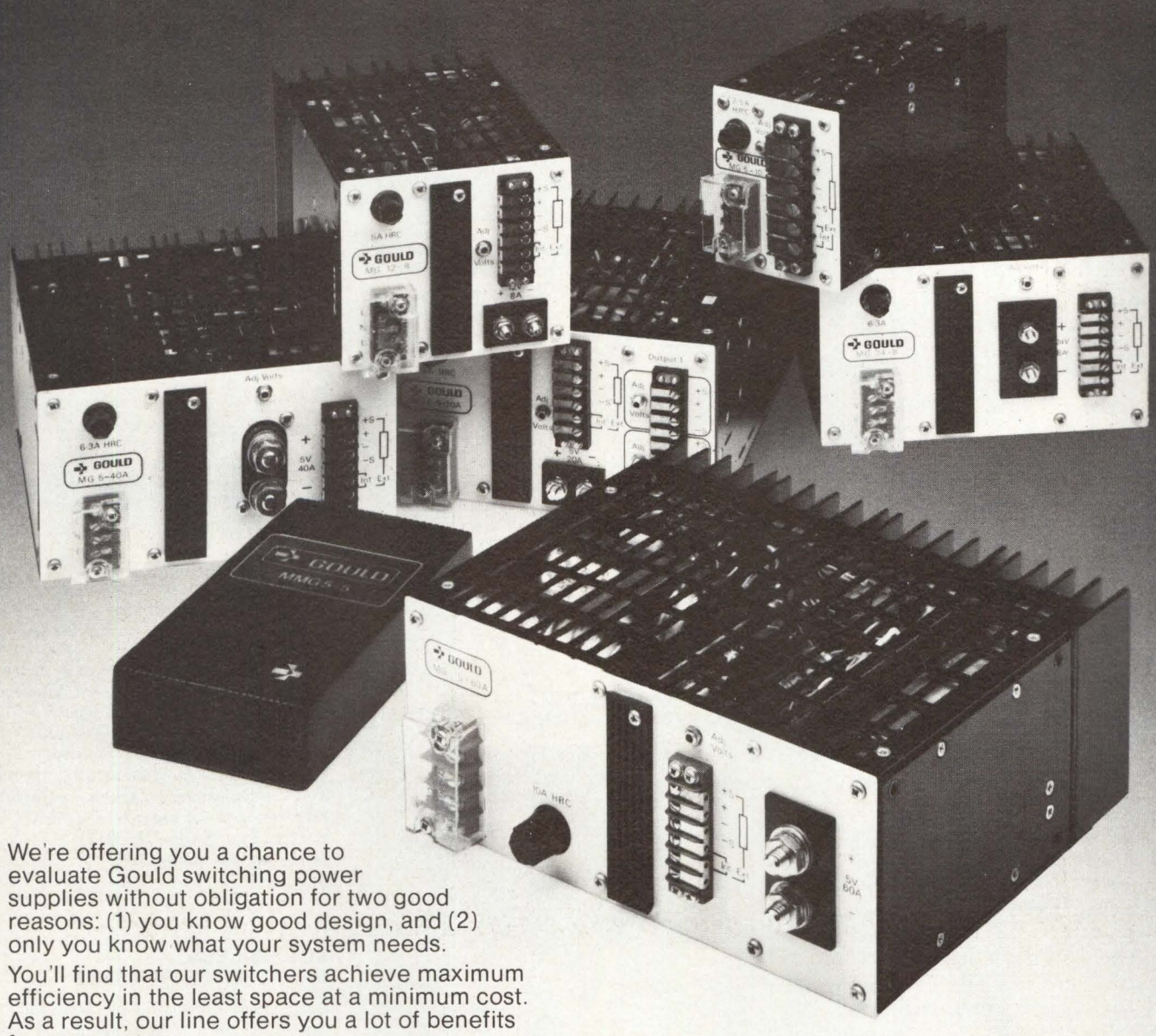
COMPLEMENTARY POWER TRANSISTORS

Two series of triple-diffused epitaxial npn and pnp devices have large signal and medium power characteristics for industrial control applications, alone or as complementary pairs. The 2N5091 series of four pnp devices, and 2N5092 of six npn devices respectively exhibit collector-base voltages of 350 to 500 V and 400 to 800 V with 100 μA collector current; collector-emitter voltages of 300 to 450 V and 350 to 550 V with collector currents of 50 mA; and emitter-base voltage of 6 V. Continuous power dissipation for both is 2 W at 100°C with linear derating factor of 26.7 mW/°C above 100°C. **Solid State Devices, Inc,** 14830 Valley View Ave, La Mirada, CA 90638.
Circle 213 on Inquiry Card

OCR VIDEO CAPTURE OPTION

An option for the Laser OCR-ONE optical character recognition system permits capture of a variety of information not recognizable in terms of the basic definition of OCR equipment. Raw video or image information is captured, processed, and then reconstructed during a later processing step. Video information can be captured from a maximum area 1" H x 4" W (2.54 x 10.16 cm) per output record. Multiple records can be generated for each document scanned enabling a whole document to be captured. Minimum area will be 0.3525" (0.895 cm) with variable width. **Optical Business Machines, Inc,** 804 W New Haven Ave, Melbourne, FL 32901.
Circle 214 on Inquiry Card

TRY ONE ON GOULD AND YOU DECIDE.



We're offering you a chance to evaluate Gould switching power supplies without obligation for two good reasons: (1) you know good design, and (2) only you know what your system needs.

You'll find that our switchers achieve maximum efficiency in the least space at a minimum cost. As a result, our line offers you a lot of benefits for your system:

- off-the-shelf delivery
- 36,000 hours MTBF
- switching at 33 kHz
- 5 year warranty
- 28 m/sec hold-up time
- 0.1% line/load regulation
- full output at 50°C ambient
- remote sensing and voltage programming
- less than 50 mV peak to peak ripple

But the truth is, you really have to test one of our switching power supplies yourself to appreciate how well our switcher works with your design.

So tell us what you need to fully evaluate our capabilities. Our salesman will deliver the appropriate unit from stock without any obligation to buy.

For information contact Gould Inc., Power Supply Dept., 3631 Perkins Ave., Cleveland, Ohio 44114.

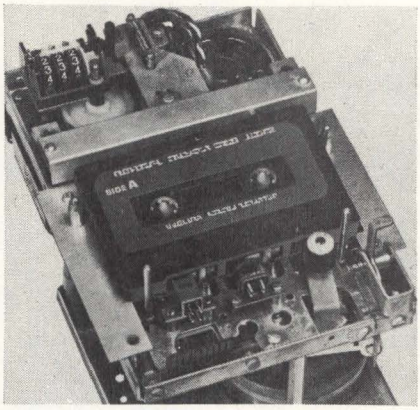
For brochure call toll free at (800) 325-6400 Extension 77
In Missouri: (800) 342-6600

GOULD

CIRCLE 115 ON INQUIRY CARD

PRODUCTS

DIGITAL CASSETTE TRANSPORT MECHANISM



Model A7, a compact, high performance transport, features one reel motor and one capstan motor. The concept eliminates back tension due to the unused motor as well as motor bearing frictions which cause tape stretching and slipping. Designed for compatibility with ANSI, ECMA, and ISO standards, the unit has mechanical and electrical interlocks to prevent improper cassette insertion or usage. Other features include fail-safe braking, front loading with full cassette visibility, precision machined head mount, single or dual direction read/write, and self-aligning pinch roller. **Amilon Corp,** 49-12 30th Ave, Woodside, NY 11377.
Circle 215 on Inquiry Card

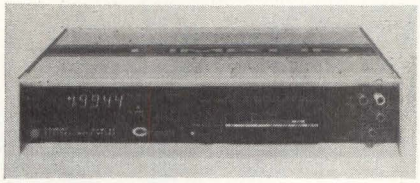
CUSTOM MOLDED CABLE ASSEMBLIES

VIKORD units feature miniature, rugged thermoplastic-shelled Thorkom circular connectors. Any cable that can mate with these connectors can be used in the unit. Right-angle or straight backshells are moisture resistant and suitable for applications in dirty environments. Offering quick connect/disconnect capability, connectors are corrosion resistant and come with 7, 12, or 24 No. 22 contacts, accepting 22 to 26 AWG wire. Operating temperature range is −55 to 125°C. **Viking Industries, Inc,** 21001 Nordhoff St, Chatsworth, CA 91311.
Circle 216 on Inquiry Card

MODULAR DISC SWITCHES

Reliability is >10M operations without failure for these switches which are totally sealed through insert molding and ultrasonic welding. Applying pressure to the upper dome collapses the device momentarily making instant positive 3-point contact with the lower diaphragm. Features include self-cleaning, and switching power from a few milliwatts to 30 W with low bounce (<10 μs). Adaptations are the model MD disc, an extra-flat momentary-contact module; model ED disc element, a basic contact element; model DMB modular rocker disc switch with momentary contact; and model TFD alphanumeric data entry keyboard-style switch with low profile. **IEE/Schadow, Inc,** 8081 Wallace Rd, Minneapolis, MN 55343.
Circle 217 on Inquiry Card

MULTIMETER G-P INTERFACING OPTION



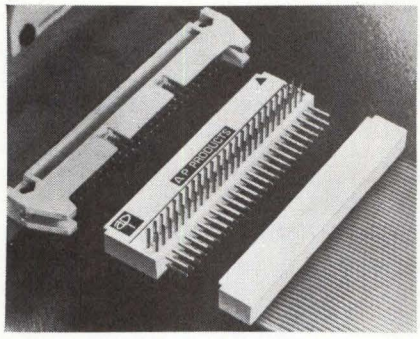
GPIB IEEE-488 is now optionally available on Cimron^R model DSM 44. The 4½-digit systems multimeter is no longer limited to fixed software. The bus is implemented with an 8-bit microprocessor under p/ROM control which allows a variety of program formats. Opening the input measurement bus to the multimeter and requesting service from the controller whenever a false program combination is received protects the option until the error has been cleared. **Aiken Industries, California Instruments Div,** 5150 Convoy St, San Diego, CA 92111.
Circle 218 on Inquiry Card

SOLDERLESS BREADBOARD SOCKETS

Designated EXPERIMENTOR 300 and 600, the 1-piece sockets both provide 94 5-point terminals, plus two 40-point bus strips, for a total of 550 solderless tie-points. The 600 has a 0.6" (1.524 cm) center channel, with full 4-terminal fanout for microprocessors, clock chips, and larger DIPs. The 300 has a 0.3" (0.762 cm) center channel for smaller DIPs. Sockets feature an interlocking system permitting them to be snapped together vertically or horizontally for optimum configurations. Both measure 0.375" deep x 6" long (0.95 x 15.24 cm). The 600 is 2.4" (6.096 cm) wide; 300 is 2.1" (5.334 cm). **Continental Specialties Corp,** 44 Kendall St, PO Box 1942, New Haven, CT 06509.
Circle 219 on Inquiry Card

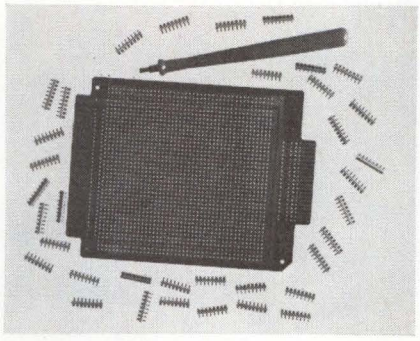
←CIRCLE 116 ON INQUIRY CARD

FLAT RIBBON CABLE CONNECTORS



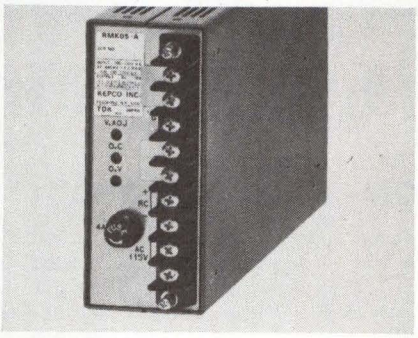
Intra-Connector™, consisting of std female double-row socket connector and two sets of mating male contact pins at right angles, can be used as a through-line connector with a redundant set of male pins to facilitate signal tracing and measurement of flat cable systems, thus making it a valuable testing tool. Available in five flat ribbon cable line widths (20, 26, 34, 40, and 50 contacts), the device can also expand existing systems by residing as a line tap, enabling daisy chains to be built into the systems. **AP Products, Inc,** Box 110, 72 Corwin Dr, Painesville, OH 44077.
Circle 220 on Inquiry Card

PC CARD BREADBOARD KIT



The "Scotchflex" 3383 kit contains a prototype PC card and 36 8-terminal breadboard contact strips. As many strips as needed may be wave-soldered to the card, together with discrete components or IC sockets. The upper edge of each solder strip has exposed U-contacts into which connecting wires are inserted with a special hand tool. Wires are also removable, permitting changes. The 4.5 x 6.375" (11.43 x 16.19 cm) card is printed with buses and floating multiple connections on 0.1" (0.25 cm) centers. It mates with "Scotchflex" 40- and 44-position edge card connectors. **3M Co, Electronic Products Div,** PO Box 33600, St Paul, MN 55133.
Circle 221 on Inquiry Card

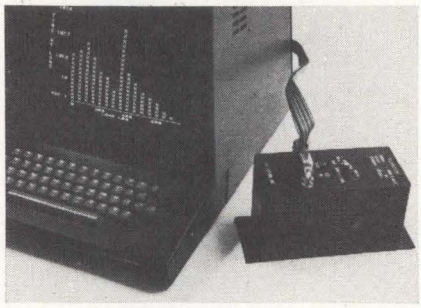
SWITCH-MODE POWER SUPPLIES



RMK series A consists of five models: 5 V at 0 to 12 A, 9 V at 0 to 7.6 A, 12 V at 0 to 6.3 A, 15 V at 0 to 5 A, and 24 V at 0 to 3.2 A. All models may be factory set in the −30 to 10% range of nominal voltage. With an operating temp of 0 to 71°C, the 2.1875 x 5.125 x 7.5" (5.56 x 13.02 x 19.05 cm) units feature 25-kHz switching for 68% efficiency, low loss TDK ferrites, and low parts population through integration. They also provide remote error sensing, adjustable current limiting logic level on/off, and ac/dc power input. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
Circle 222 on Inquiry Card

PRODUCTS

SOLID-STATE DATA RECORDER



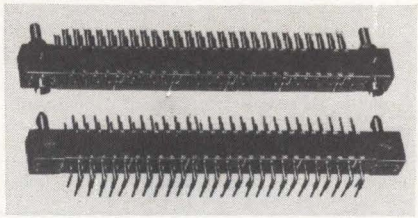
Containing no moving parts, the self-powered, self-contained ADASTOR obsoletes tape, strip charts, and other methods of data recording as it accumulates and organizes data as a direct histogram which can be read out onsite when interfaced to a computer terminal with minimal graphics capability, or to any std plotter. For monitoring purposes, unit reduces data storage need in real-time and turnaround time to interpret results. Capable of storing $>10^{10}$ bits of data, the recorder accepts information from all typical transducer devices and from electronic instruments which generate voltages, currents, or pulses. **Sun Systems,** PO Box 182, Sun Valley, ID 83353.
Circle 223 on Inquiry Card

POWER SWITCHING TRANSISTORS

With high energy capabilities, series 2N6582 npn silicon devices for offline switching regulators feature switching times of 250 ns. Collector-emitter sustaining voltage ranges from 350 to 450 V with continuous collector current of 10 A. $V_{CE(SAT)}$ is <1.5 V at I_C of 7 A while transistor dissipation is rated at 125 W at 25°C. Junction operating and storage temp range is −65 to 200°C. Transistors are available in TO-3 or -61 (isolated) packages. **TRW Power Semiconductors,** 14520 Aviation Blvd, Lawndale, CA 90260.
Circle 224 on Inquiry Card

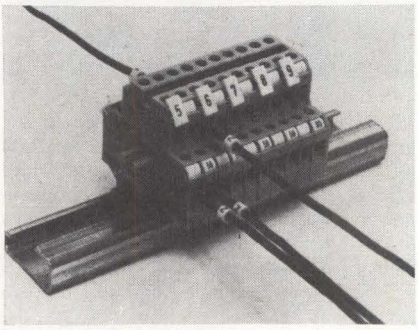
LOW MATING FORCE PC CONNECTORS

Line of 2-piece high density SI-TAC connectors features a socket design which provides 80 to 90% reduction in contact mating forces over conventional contacts.



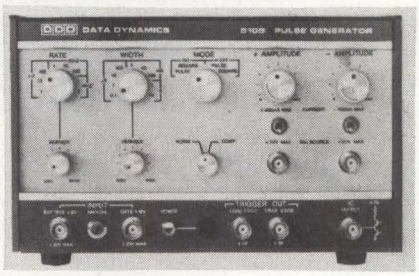
Current ratings are 2.5 to 5 A, contact resistance is <5 mΩ, and a 1- to 2-oz (28.3- to 56.6-g) insertion/withdrawal force is required per contact pair. The hyperbolic shaped sleeve is formed by a number of gold-plated wires extended through a tubular wire carrier at an angle to the axis of the tube. When a pin is inserted, the wires form a helical wrap along the pin, producing a large contact area and redundant electrical circuit paths. **Smith Industries, Inc, Connector Div,** PO Box 5389, Clearwater, FL 33518.
Circle 225 on Inquiry Card

DOUBLE-DECK CONNECTOR TERMINAL



Modular terminal block allows high density wiring while maintaining access to clamping devices and providing spaces between wires. The DK4 is UL-recognized for industrial applications up to 300 V for wire sizes AWG 22 to 12. Width of the terminal is 0.24" (0.61 cm), enabling a 1-foot assembly to accommodate 48 blocks, each with four vibration-proof screw clamp connections. The molding is made from Polyamid 6.6, to comply with UL 94V2. **Weidmuller Terminations, Inc,** 4326 Eubank Rd, Richmond, VA 23231.
Circle 226 on Inquiry Card

CMOS-COMPATIBLE PULSE GENERATOR



DDD model 5105 pulse generator is compatible with many logic families, particularly CMOS. Positive output is CMOS-compatible, providing pulses continuously variable to 20 V. Variable pulse repetition rate aids direct measurement of dynamic dissipation increases due to higher speed of operation. Negative amplitude pulses to −20 V are simultaneously available from the negative output, satisfying requirements for other MOS families. Both outputs may also be operated as current sources (to 400 mA) by means of a front panel switch. **Electronic Counters, Inc,** 240 Humphrey St, Englewood, NJ 07631.
Circle 227 on Inquiry Card

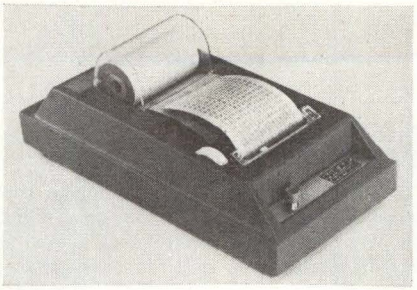
FLOPPY DISC SYSTEM

Vortex provides V-77 series minicomputer users with a low cost approach to program and data distribution between host computer and remote processors. Vortex II (64k main memory) operates in full fore/background modes with diskettes providing medium for transporting generated systems or program load modules to multiprocessor network locations. System consists of single or dual disc drives, formatter, and interface controller. Diskettes are formatted at 120 16-bit words/sector, providing 295k and 590k words for single and dual drives, respectively. **Varian Data Machines,** 2722 Michelson Dr, Irvine, CA 92713.
Circle 228 on Inquiry Card

18-BIT DAC

Packaged in 2 x 4 x 0.4" (51.18 x 101.98 x 10.41 mm) module, 18-bit DAC1138 and a 16-bit DAC are available in J and K versions, with 18-bit resolution. They are pin compatible with QM series 14- and 16-bit DACs. J has 1 LSB linearity; K has ½ LSB linearity. Both feature offset tempcos of 0.5 ppm/°C with differential linearity tempcos of 0.4 ppm/°C. Each operates at specified resolution over the 5 to 50°C temp range; accuracy in the K version is maintained ±10°C from operating temp. **Analog Devices, Inc,** PO Box 280, Norwood, MA 02062.
Circle 229 on Inquiry Card

80-CHAR/S MATRIX LINE PRINTER



All electronics for direct interfacing such as from I/O ports of microprocessor to high voltages and currents of printhead and motors are included in the NMP-420 medium speed printer. Unit comes in a case with power supply from 110 to 220 V. Electrosensitive matrix printer uses low cost metallized paper eliminating the need for ink ribbons. A 25-m x 60-mm roll of paper has capacity for 5000 lines. Depending on format, character spacing, and column update timing, 40, 32, 21, or 16 char/line are possible. **NIEAF,** Jutfaseweg 205, Utrecht, Holland.
Circle 230 on Inquiry Card

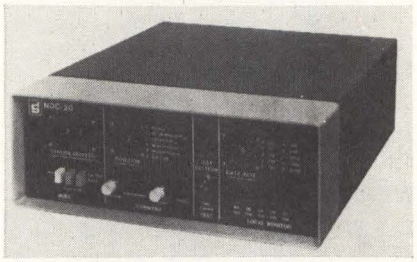
SUBMINIATURE PLUNGER PUSHBUTTON SWITCHES

A variety of plunger/actuator switches (models 8531, 32, 33, and 34) include three basic styles: large—with a 0.330" (8.38 mm) dia, flatted top, and 0.250" (6.35 mm) height; short—0.250" (6.36 mm) dia, convex top, and 0.150 to 0.173" (3.81 to 4.39 mm) height; and long—0.250" (6.35 mm) dia, convex top, and 0.210 to 0.233" (5.33 to 5.92 mm) height. Short and long are available in red or black; large is available in white, black, red, yellow, or green. All plungers are made of Phenolic, and feature an electrical life of 1M make-and-break cycles. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 231 on Inquiry Card

WIREWRAP MODULE BOARD

The WW-1 is based on the std 44-pin, 3.25 x 4.5" (8.16 x 11.43 cm) microcomputer and digital logic module configuration. Module contains 14 rows of 20 pins each with rows spaced on 0.3" (0.76 cm) centers for direct insertion of any combination of IC chips, from 8 to 40 pins. Power and ground are bused throughout board for connection to specific pins. Also selectable for user wiring are 12 card edge test points and 44 module I/O pin connections. Since no chip sockets are used and pin wiring is user defined, unit can accept a variety of chip types and configurations. Board is supplied with decoupling capacitor installed. **Wyle Computer Products, Div of Wyle Laboratories,** 3200 Magruder Blvd, Hampton, VA 23666.
Circle 232 on Inquiry Card

DATA NETWORK DIAGNOSTIC CONTROL SYSTEM



NETCON™-2 extends test, control, and diagnostic functions from a central location to remote terminals via multipoint and multiline modem networks, DDS networks, and other links. Remote testing is accomplished in-band, within data path, eliminating equipment costs of parallel or secondary transmission channels. System can address up to 32 remote stations on unlimited multipoint lines. Diagnostic commands, which are insensitive to noise, and remote site addresses are switch-selectable on NDC-20. Control technique includes positive response from each addressed modem. **General DataComm Industries Inc,** 131 Danbury Rd, Wilton, CT 06897.
Circle 234 on Inquiry Card

3-DIMENSIONAL DISPLAY IMAGE MULTIPLEXER

Model 6154 allows superimposition of two graphic type images on the same CRT display screen. Time multiplexing is used to switch between two different image generation signals. Packaged in 2 x 2 x 0.4" (5.08 x 5.08 x 0.102 cm) module, the unit features dc to 5-MHz signal bandwidth, internal switching clock set at 350 Hz nom, external provision to vary switching duty cycle to control relative image intensity, and ±10-V full scale signal voltage. Operating temp range is −55 to 100°C. **Optical Electronics, Inc,** PO Box 11140, Tucson, AZ 85734.
Circle 235 on Inquiry Card

PEAK-DETECTING A-D CONVERTERS

Capable of digitally tracking and storing (using no capacitors) the peak value of an analog input signal without degradation or droop, the PD855 series is available with 3-decade BCD or 12-bit binary coding. It can detect and read peak signals from 0 to 10 V at a tracking rate of 40 V/ms for BCD and 10 V/ms for binary code. Devices are recommended for use in applications where peak analog signals interface with computer, microprocessor, or digital display. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.
Circle 236 on Inquiry Card

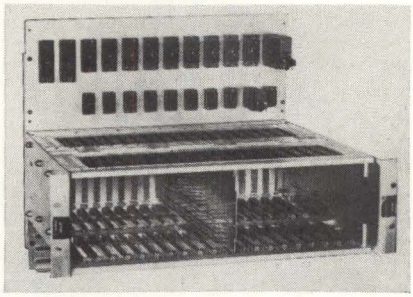
SUBMINIATURE SWITCHES

Offering a variety of function, actuation, electrical, and mounting options, line of switches consists of three series: 571 toggle switches with solder blade, wirewrap, or straight PC terminals; 572 with rocker and lever actuators; and 573 toggle switches with right angle PC terminals. Each offers spdt and dpdt options and three contact ratings: for low level application, up to 0.4 VA at 20 V max ac or dc resistive load; for higher levels, 5 A at 120 Vac or 128 Vdc, resistive load, or 2 A at 250 Vac; and a single item to meet either requirement. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 237 on Inquiry Card

ADD-ON MEMORY

A memory expansion system is completely self-contained in a rack mountable 5.25" (13.34 cm) high chassis, which houses as much as 128k words by 20 bits of core memory. The company designs and manufactures the interface between almost any manufacturer's computer and the expansion memory. Interface module is also enclosed in the expansion chassis. Entire memory includes memory modules, power supply, chassis, and interface. **Digital Data Systems,** 5975 W Sunrise Blvd, Sunrise, FL 33313.
Circle 238 on Inquiry Card

ADJUSTABLE PC CARD ENCLOSURE SYSTEM



Available in 24" (60.96 cm) model, Varipak II[R] expandable enclosure system's design is suited to packaging rows of cards and connectors using almost any card spacing. Design also offers good air flow for long component life. Basic construction is of rigid aluminum. Available in 32 sizes, system has single and double tiers, holding 54 and 107 cards, respectively. Polycarbonate guides are 0.093" (0.236 cm) deep. Accessories include marker strips, reinforcement bars, and standard or custom front panel. **Elco Corp,** a Gulf + Western Mfg Co, 2250 Park Pl, El Segundo, CA 90245.
Circle 239 on Inquiry Card

HIGH SPEED BUFFER MEMORY

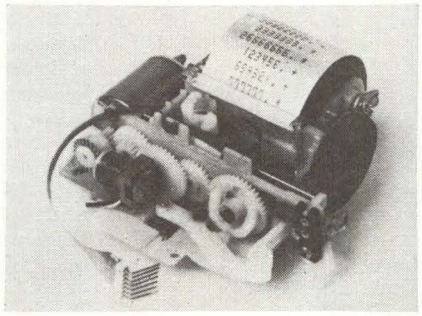
MEM1108-100/2560 allows users to buffer ultra-high speed analog data conversions. With a storage capacity of 2560 words accumulated at input rate of 100M words/s, memory readout (output) rate is 4M words/s when using the internal buffer clock. Unit is suited for use with A-D converter systems employing up to 6-bit resolution and ECL interface logic. Approximately 8 x 8 x 3″ (20.32 x 20.32 x 7.62 cm) in size, memory also features TTL logic and load operation synchronized with ADC end of conversion pulse. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017.
Circle 240 on Inquiry Card

REMOTE STATION TERMINALS

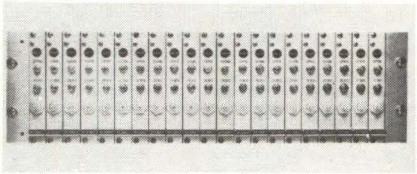
Units in the 5500 MICROPLEX series are designed for supervisory control and data acquisition systems where remote stations have fewer points. Completely self-contained, they include power supply, modem, and a max of four functional point modules. Devices can be equipped with as many as five different types of point functions in various combinations, economically configured in increments as small as four points. Available plug-in modules are four and eight control points; 16 indication points, with eight accumulator points; four setpoints; and 4-, 8-, or 16-point isolated A-D modules. **Harris Corp, Controls Div,** PO Box 430, Melbourne, FL 32901.
Circle 241 on Inquiry Card

ELECTRONIC DISCHARGE PRINTER

Adding permanent recording to portable instrumentation, battery operable model DC 31206 is reliable, mechanically simple, and low powered (requiring no standby power). With high speed operation of 12 col of alphanumerics at minimum rate of 5 lines (60 char)/s, 5 x 7 dot matrix characters are printed by current from electrodes in printhead passing to standard 1.4″ (3.6 cm) roll of aluminum coated paper. Printer measures 3.65 x 3.2 x 1.7″ (9.27 x 8.13 x 4.32 cm) and weighs 5.25 oz (147 g). **Hycom, Inc,** 16841 Armstrong Ave, Irvine, CA 92714.
Circle 242 on Inquiry Card



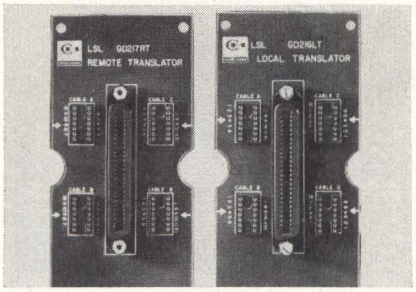
MULTICHANNEL P-I CONVERTER SYSTEMS



Systems provide current or voltage signal from a standard 3- to 15-lb/in² pneumatic line for computer interface. Up to 21 plug-in P-I modules containing solid-state amplifiers and IC sensors can be mounted on single 19″ (48 cm) rack adapter. Both 2- and 4-wire systems and self-contained consoles with 100 or more channels are available. Accepted inputs are 3 to 15, 3 to 27, 20 to 30 lb/in²; outputs of 0 to 10 V or 4 to 20 mA are offered. Accuracy is 0.25% FRO and repeatability is better than 0.1%. **Kulite Semiconductor Products, Inc,** 1039 Hoyt Ave, Ridgefield, NJ 07657.
Circle 243 on Inquiry Card

PRODUCTS

INDUSTRIAL CONTROL SYSTEM I/O BOARDS



Flexibility has been added to Ladder Static Logic (LSL) solid-state industrial control systems with local and remote 48-point I/O plug-in circuit boards for materials handling, sequencing, timing, and synchronizing operations. Working in combination, the additions accept a 50-wire communications cable and four DIP receptacles to accommodate flat ribbon cable connections from logic boards. This reduces costs of initial wiring and virtually eliminates the high time/cost factors of reconnecting wire bundles when equipment arrives at the job site. **Cutler-Hammer, Inc, Logic Device and Systems Div,** 4201 N 27th St, Milwaukee, WI 53216.
Circle 244 on Inquiry Card

COAXIAL FIBER OPTIC SCANNER

Capable of detecting a 0.005" (0.0127 cm) wide mark at 0.100" (0.254 cm) with a repeatability of ±0.001" (0.0025 cm) and amplifying output of phototransistor in the scanner to an open collector output, the C32101 is a complete electronic amplifier in a combination unit. Its high level signal output allows transmittal over long distances without loss of quality or signal strength. Schmitt trigger circuit insures positive switching of output from on to off. Units are available in lamp or LED versions with power requirements of 5 Vdc, and a 15-turn potentiometer for sensitivity adjustment. **Skan-A-Matic Corp,** PO Box S, Rt 5 W, Elbridge, NY 13060.
Circle 245 on Inquiry Card

LOW PROFILE LSI SOCKETS

Including 14-, 16-, 24-, 28-, 40-, and 42-pin versions on 0.1" (0.25 cm) centers, the SI-2440 series with glass-filled nylon bodies are designed to withstand soldering temperatures to 350°C for 3 seconds. Available with tin plating, selective gold contact plating, or gold flash, units are designed to be flush mounted end-to-end maintaining the 0.1" (0.25 cm) center-to-center pin spacing. **SMK Electronics Corp of America,** 118 E Savarona Way, Carson, CA 90746.
Circle 246 on Inquiry Card

DIP OSCILLATORS

Crystal-controlled miniature oscillators feature a frequency range of from 20 kHz to 25 MHz. They drive up to 10 TTL loads with an overall stability of ±0.01% (model DT1-121) or 0.005% (model DT1-221), over the temperature range of 0 to 70°C. Package size is 0.50 x 0.80 x 0.37" (1.27 x 2.032 x 0.94 cm). Extended frequency range and low temperature models are also available. **Ovenaire Div, Walter Kidde & Co, Inc,** 706 Forrest St, PO Box 1528, Charlottesville, VA 22902.
Circle 247 on Inquiry Card

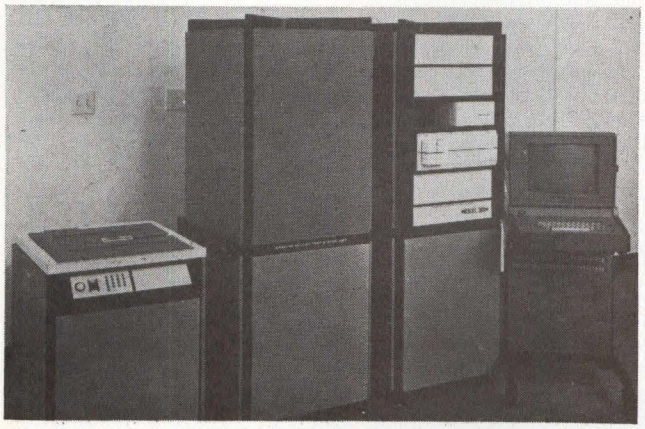
6-PIN OPTICAL COUPLERS

Two photodarlington devices, models 4N45 and 4N46, feature low input current with high gain and current transfer ratio of 1000% typ. For use in low input applications such as MOS, CMOS, and low power logic interfacing, 4N46 has input current at 350% CTR, as low as 0.5 mA; output voltage is −0.5 to 20 V. 4N45 has minimum CTR of 250% at 1.0 mA, and −0.5- to 7-V output. Both include internal base-emitter bypass resistor which minimizes output leakage. Gain-bandwidth adjustment pin allows access to second stage base for better noise rejection. Performance is guaranteed over temp range of 0 to 70°C. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.
Circle 248 on Inquiry Card

8-BIT D-A CONVERTER

DAC 82 is a self-contained multiplying DAC that provides ±1 LSB accuracy at room temperature with no external adjustments, and ±½ LSB linearity over the full temperature range. Complete with internal reference, scaling resistors, and an output amplifier, the unit is claimed to be the first 8-bit DAC for use with either an internal reference for normal operations or with an external reference for 2-quadrant multiplying applications. Reference input is a summing junction, which allows use of any positive value reference voltage with an appropriate input resistor. Two versions, both hermetically sealed in metal packages, are the BM version with a temp range of −25 to 85°C, and the SM version covering the full military temp range of −55 to 125°C. **Burr-Brown,** International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734.
Circle 249 on Inquiry Card

PAGE-MODE MEMORY TEST STATION



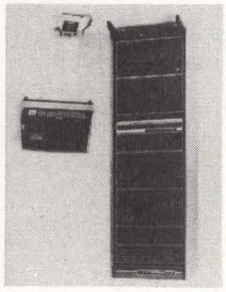
In addition to address multiplexed devices, the H712 station tests 4k and 16k page-mode memories with multiplexed input and output terminals, on its J387 memory test system. Basic station includes nine independently programmable, double-edge clock phases, 16 address drivers, four data drivers, and four dual-limit comparators. These can be expanded to nine data drivers and 12 comparators for testing RAMs with up to nine input and output terminals and ROMs with up to 12 output terminals. Because timing constraints must be changed during testing without interrupting the functional test, unit is designed so that multiple values for clock widths and clock delays can be established in the test program before the test is initiated. These times, as well as a test rate oscillator, can be changed "on-the-fly" under microprogram control. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.
Circle 250 on Inquiry Card

MULTIPROCESSOR AUTOMATIC TEST SYSTEM

Capable of simultaneous linear/digital testing at multiple sockets or at one socket with up to 232 pins, the multiprocessor controlled model 6000 automatic test system is designed for linear, digital, or hybrid circuit boards. Diagnosed faults are printed on an adhesive ticket or displayed on a CRT error map. All connections to the circuit under test are via a high performance full Kelvin universal switching matrix, eliminating the need for patched socket adapters. Testing operations are governed by a DEC PDP Super-8 minicomputer with 16k core memory. Linked to it is a second 32k PDP-8 for digital simulation or program preparation. An additional microprocessor controls a Mirco digital test subassembly, complete with RAM, control unit, and pin electronics. High speed disc files are central to all processors, with magnetic floppy disc as backup memory. Two high speed line printers serve for listing and data logging. **Optimized Devices, Inc,** 220 Marble Ave, Pleasantville, NY 10570.
Circle 251 on Inquiry Card

PRODUCTS

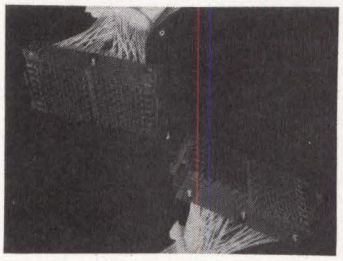
COMPUTER VOICE-RESPONSE SYSTEM



A voice response telecommunications system that makes any Touch-Tone® telephone a computer terminal, Nucleus 4000 allows direct data retrieval from a computer. The system stores recorded human speech and has unlimited vocabulary capability. Using industry standard ports, the system can service up to 48 lines and more with special configurations. Voice response can function concurrently with CRTs, printers, and other telecommunications devices; it can be provided for any type CPU. Configurations are as an intelligent front-end to IBM systems and as standalone systems. Networks can be configured under the ASI/NET packet-switching software system. Basic front-end teleprocessing system includes data sets, I/O multiplexer, central minicomputer processors, disc for vocabulary storage, interface to applications computer, and software. **American Systems, Inc,** 123 Water St, Watertown, MA 02172.
Circle 252 on Inquiry Card

LOW MATING FORCE CONNECTORS

The B³ bristle brush bunch line of connectors for PC board designers provides a 70 to 90% reduction of conventional mating/unmating forces. The need for external board supports is reduced and high circuit count interconnections are practical. Line includes mother and daughter board connectors, PC receptacles, as well as I/O styles, in 2-, 3-, and 4-row versions on 0.1 in² (0.645 cm²) grid spacing. They are available in row lengths of from 10 to 100 contacts. Termination options include solderless wrap, PC stud, straight and 90-deg mount, and crimp removable contacts. Featuring a modular building block connector for "build your own" connector needs, the modules are stackable in both X- and Y-axis combinations. Replaceable contacts, modular connector bodies, hardware, and accessories are packaged with instructions in prototyping kit. **Bendix Electrical Components Div,** Sidney, NY 13838.

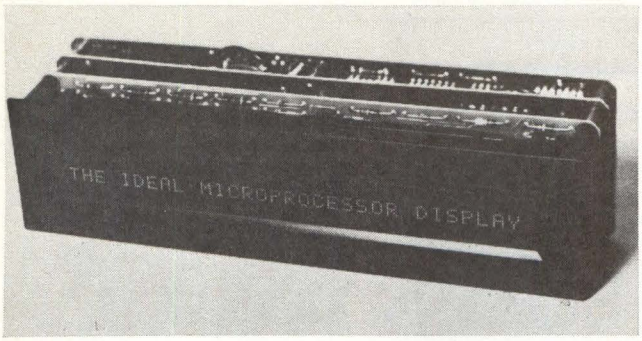


Circle 253 on Inquiry Card

MICROFICHE READER/PRINTER

Sharp copies in an infinitely adjustable range of page sizes from 4 x 5" (10.2 x 12.7 cm) to 12 x 12" (30.5 x 30.5 cm) are attainable from the "21st Century" microfiche reader/printer. Copy costs are claimed to be as little as a penny a print. All controls are located on the front panel. Paper flow is from side to side, easing servicing, and paper loading is very simple. A magnetic-drive pump continually agitates toner and pumps it evenly over the paper to assure uniform print intensities. The toner tray can be removed for filling or cleaning. Paper is cut to size before being exposed, and a vacuum system pulls the paper flat against the platen during exposure. Each fiche is viewed on a 12" (30.5 cm) sq blue screen; actual copy size is shown by vertical lines on the screen. A rotator positions the image to align a skewed fiche. Interchangeable lenses give 24X to 54X magnification. The quartz-halogen lamp is rated at 600/1000-h life (high/low brilliance). **Micro Information Systems,** 467 Armour Circle NE, Atlanta, GA 30324.
Circle 254 on Inquiry Card

PROGRAMMABLE ALPHANUMERIC DISPLAY

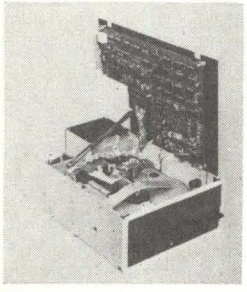


SELF-SCAN model SSD0132-0081 is a programmable 32-char alphanumeric display module, which permits selection of an unlimited number of different characters and symbols for display in a 5 x 7 dot matrix format. A 64-char repertoire version of the unit uses a pair of p/ROMs for easy programming of any desired character set. The p/ROMs may be reprogrammed as desired to display any combination of letters, symbols, or numbers after initial programming. The system can also be used with a 128-char repertoire by populating the display module with 64 std characters in a metal-masked ROM plus a custom 64-char set generated by two p/ROMs. Maximum character entry rate is 13 times faster than typical units (max rate of 166k char/s). Gas discharge panels display 0.2 x 0.14" (0.508 x 0.356 cm) char with a high contrast, steady neon-orange glow, readable at distances up to 15 ft (4.57 m). **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 255 on Inquiry Card

HYBRID DIP DATA ACQUISITION SYSTEMS

The MN7100 and 7110 combine to form a complete 8-bit, 24-channel data acquisition system in two DIPs requiring <5 in² (32.26 cm²) of board space. These thin film hybrids are available for operation over the full −55 to 125°C military temperature range. The 7100 contains the basic 8-bit, 8-channel DAS including multiplexer, sample/hold, A-D, and controlling and addressing logic. Each 7110 adds the multiplexers and logic for an additional 16 analog input channels. Std 7400 TTL ICs allow expansion to over 256 analog input channels. Devices are hermetically packaged in 32-pin DIPs. Input channels may be randomly addressed or controlled from the internal sequential address counter, and both channel address inputs and outputs are provided. Digital inputs and outputs are TTL-compatible and internal or external clock can be used. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01606.
Circle 256 on Inquiry Card

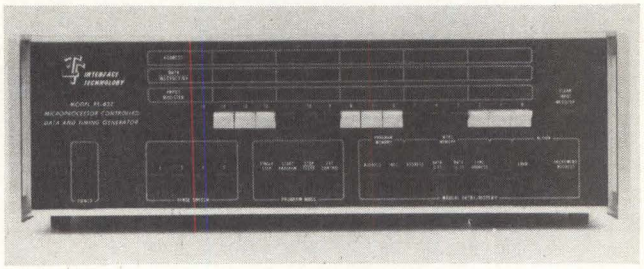
FLOPPY DISC DRIVES



Series 400 diskette drives feature automatic head-unload and stepper motor timeouts, bidirectional write-protect, radial stepping ability for overlapping seeks, host power failure detector, six different LED activity indicators, and 50-pin ribbon cable or twisted pair interfacing compatibility. Both the model 410 (soft-sectored, IBM-compatible) and the 420 (hard-sectored) provide single and double density recording capability. A proprietary data separator design, coupled with a digital noise filter and unique handling of recorded signals, results in 35% greater data integrity margins than other units. Additional features include filtered air operating environment, single-side accessibility for maintenance, mechanical door interlock with manual override button, targeted media loading, and a patented "wear-free" diskette hub rated for over 100,000 insertions. **Innovex Corp,** 75 Wiggins Ave, Bedford, MA 01730.
Circle 257 on Inquiry Card

PRODUCTS

BUS TESTER/EXERCISER



Specifically designed for IEEE Std 488-1975 bus/device testing, exercising, and simulation, the model RS-432-IB is designed around the company's microprocessor-controlled data and timing generator. The programmable tool simulates the bus control function and allows the user to control and exercise the end device under test, thereby aiding reduction of development time. All testing can be accomplished at full dynamic bus speed or at user programmed rates, with memory for storing and transmitting up to 512 bytes of end device dependent message data. A basic exerciser program is included with the unit. User programs may also be generated. Interface circuit debugging is enhanced with LED readout of all bus signal states. **Interface Technology,** 852 N Cummings Rd, Covina, CA 91724.

Circle 258 on Inquiry Card

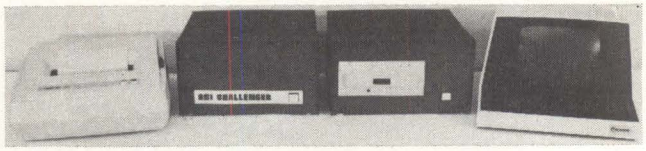
300-W UPS

Model 2700 Mini-UPS mainframe and three user selectable dc-dc supply slots furnish continuous dc power during an ac interruption or brown-out. Standby power is supplied from a backup battery; diode switches allow instantaneous change-over. Unit is designed for applications where only a few hundred watts of uninterruptible dc power are needed to supply critical data circuitry such as memories and/or timing logic, data recording, or alarm circuitry. Sequential logic programming can be designed to extract and permanently record memory data, put the system in a hold mode, shut it down, or activate an alarm. Modules are user selected as add-ons, with ratings of 1, 3, 5, 10, or 25 W. They are installed at the factory in three uncommitted slots built into the mainframe. Features include custom outputs, replaceable modules, and burn-in at full load for 100 h or more. **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.

Circle 259 on Inquiry Card

SMALL INTEGRATED COMPUTER

This integrated computer system is based on the Challenger 65 mainframe computer, featuring 16k of RAM, system monitor, disc bootstrap p/ROMs, and serial interface. Also included is the Challenger single drive floppy disc based on the GSI 110 drive, plus a standalone CRT terminal and Sanyo monitor. System comes complete with software—the company's disc operating system, disc-based 6502 resident assembler/editor, extended monitor, 8k disc BASIC by Microsoft, and BASIC program library. Options allow system expansion. Dual floppy disc drives are offered, as are 13 accessory boards giving up to 192k of RAM and 16k of I/O and ROM, DACs, ADCs, parallel and serial I/O cassette interfaces, video graphics display, and advanced multiprocessor capabilities. Hard copy is obtained from two Okidata dot matrix line printers with 80- or 132-char lines. **Ohio Scientific Instruments,** 11679 Hayden St, Hiram, OH 44234.



Circle 260 on Inquiry Card

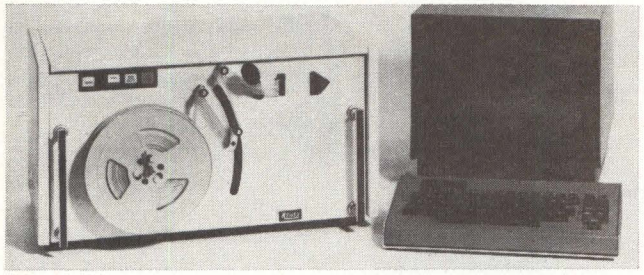
LSI MODEM TERMINALS

Two modems, which convert analog waves into machine-readable form and vice versa, rely entirely on LSI technology, enabling them to adapt to any line conditions with a processor-type automatic equalizer that compensates line amplitude and delay distortion. FACOM 1915A transmits and receives at a data signaling rate of 4800 bits/s, and the 1911A at a rate of 2400 bits/s. Units feature differential 8- and 4-phase modulation, respectively. Both satisfy recommended guidelines of the CCITT, and are therefore compatible with existing international data communications networks. Available as options are a loop checking device, an error checker, and an eye-pattern generator which immediately detect and signal errors or malfunctions. Measuring 8.3 x 6.7 x 17.7″ (21.08 x 17.02 x 44.96 cm), the devices require 100 V, 50 to 60 Hz, 35 W. **Fujitsu Ltd,** 6-1 Marunouchi 2-chome, chiyoda-ku, Tokyo 100, Japan.
Circle 261 on Inquiry Card

PORTABLE SOURCE DATA ENTRY TERMINAL

Suited for wholesale and retail order entry, the Scorepad™ series of data entry and communications terminals feature solid-state design in a portable, handheld unit. It is used to record source data and transmit it using normal voice-grade telephone lines. The terminal uses a standard 8-bit ASCII code and is fully industry compatible, interfacing with most existing computerized order entry systems; it also has an optional MSI compatibility feature. Contained in the 9 x 13 x 0.5″ (22.86 x 33.02 x 1.27 cm) impact resistant clipboard-style package weighing 1.5 lb (680.4 g) is a microprocessor, half-duplex transmission modem, program storage ROM, 8k RAM, rechargeable battery pack, LED display, and keyboard. Three attachments are a transmitter muff, battery charger, and scanning wand. **Azurdata, Inc,** 1100 Jadwin Ave, Richland, WA 99352.
Circle 262 on Inquiry Card

1200-BAUD TAPE PERFORATOR



Claimed to be the first tape perforator system capable of a 1200-baud rate for communications applications, the RQS 6120 with RS-232-C interface has a 120-char/s punch speed asynchronous bidirectional. Baud rate is selectable to 110, 134.5, 150, 300, 1050, and 1200. The punch can be connected directly to any modem with RS-232-C output and operates online as a data collection device. Other user-selectable features are character length of 5-, 6-, 7-, or 8-levels with 6-level advance feed available; stop bit selection of 1, 1½, or 2 bits between words; odd or even parity selection; and parity error inhibit selection. High speed perforator mechanism features motor driven tape feed and sprocket drive design for control of longitudinal registration. Life expectancy is >8.4 x 10^7 char. **Remex Div, Ex-Cell-O Corp,** 1733 Alton St, Irvine, CA 92713.
Circle 263 on Inquiry Card

LITERATURE

Miniature Switches

Listings for toggle, slide, rotary, DIP, pushbutton, keylock, rocker, and power switches can be found in catalog which contains specifications. **Alco Electronic Products, Inc,** North Andover, Mass.
Circle 300 on Inquiry Card

Minicomputer Media

A 16-page brochure lists media such as discs, tape cassettes, and ribbons available for minicomputer users. **Associated Computer Products, Inc,** Monroe, Conn.
Circle 301 on Inquiry Card

D-A Converters

Application note consists of tutorial section on multiplying DAC basics, detailed circuit examples, and list of applications such as algebraic digital computation. **Precision Monolithics, Inc,** Santa Clara, Calif.
Circle 302 on Inquiry Card

Backpanel Interconnect Systems

Describing both press-fit and metal-plate systems, catalog consists of descriptions, advantages, design criteria, illustrations, and technical data. **Elco Corp, A Gulf + Western Mfg Co,** El Segundo, Calif.
Circle 303 on Inquiry Card

Optical Fiber Components

Contained within catalog are optical fibers, fiber cables, laboratory accessories, source/detector systems, and research and development needs for fiber investigations. **Math Associates, Inc,** Great Neck, NY.
Circle 304 on Inquiry Card

CAMAC Equipment

Describing over 90 products which conform to IEEE Std 583 for Modular Instrumentation and Digital Interface Systems, illustrated catalog is divided into sections which focus on such areas as binary and analog I/O, controllers, processors, and memory. **KineticSystems Corp,** Lockport, Ill.
Circle 305 on Inquiry Card

Remote Display System

Model 82 interactive visual display system is discussed in 6-page folder which lists features and configurations, and gives photos and diagrams. **Data 100 Corp,** Minnetonka, Minn.
Circle 306 on Inquiry Card

Communications Components

Jacks, plugs, patch cords, terminal blocks, and hybrid transformers are some of the components listed in revised catalog featuring schematics, specs, selection charts, product descriptions, and photos. **ADC Products, div of Magnetic Controls Co,** Minneapolis, Minn.
Circle 307 on Inquiry Card

Pushbutton Switches

Color catalog with photos includes detailed specs, dimensional drawings, and assembly options on integrated modular panel system (IMPS) pushbutton switches for microprocessor applications. **Centralab Electronics Div, Globe-Union, Inc,** Milwaukee, Wis.
Circle 308 on Inquiry Card

Minicomputer Family

Covering software, services, and support for the NOVA[R] 3 minicomputer family, brochure describes operating systems, high level languages, peripherals, and configurations for applications ranging from intelligent terminals to distributed inventory systems. **Data General Corp,** Southboro, Mass.
Circle 309 on Inquiry Card

Digital Data Systems

Encompassing functional operations, engineering considerations, installation, and maintenance, illustrated bulletin supplies features on DDS station equipment consisting of the L500A data service and L550A channel service units. **GTE Lenkurt, Inc,** San Carlos, Calif.
Circle 310 on Inquiry Card

Indicator Lights

Data sheet gives complete specs and dimensional drawings of the UL and CSA approved Mini-Dot 4700 series indicator light assemblies which require minimal back-of-panel space. **Industrial Devices, Inc,** Edgewater, NJ.
Circle 311 on Inquiry Card

Single Output Switching Power Supplies

Single output switching power supply brochure covers specs, output and input ranges, and features of approximately 100 combinations of both convection and fan cooled units. **Trio Labs, Inc,** Plainview, NY.
Circle 312 on Inquiry Card

Power Line Module

Folder with photos covering series 7100 filtered and unfiltered power line modules shows capability data, operating specs, engineering interconnection drawings, and case dimensions. **The Potter Co, div of Pemcor, Inc,** Wesson, Miss.
Circle 313 on Inquiry Card

Cable Connector System

Colorful 24 x 34" (60.96 x 85.36 cm) wall chart includes cable and connector specs, and details selection and use of mass termination connectors, cables, and tools. **T & B/Ansley Corp,** Los Angeles, Calif.
Circle 314 on Inquiry Card

Time Delay Relays

Advantages, applications, features, specs, and outline dimensional diagrams for the JT series PC board relays are detailed in data sheet. **Warren G-V Communications, div of Sola Basic,** Livingston, NJ.
Circle 315 on Inquiry Card

Data Acquisition Equipment

Fully illustrated catalog points out specs and applications pertaining to line of converters, amplifiers, and systems for data acquisition and signal conditioning. **Burr-Brown,** Tucson, Ariz.
Circle 316 on Inquiry Card

Headers

Brochure describes line of male and female, single and double row headers defining specs on std items as well as options for custom configurations. **AP Products,** Painesville, Ohio.
Circle 317 on Inquiry Card

Digital Patch Units

Bulletin details features and operating information on digital patch units which rearrange interconnections between modems, multiplexers, terminals, and computers. **Spectron Corp,** Mt Laurel, NJ.
Circle 318 on Inquiry Card

Plug-In Oscilloscope

Application note with charts, drawings, and graphs supplies information on capabilities, procedures, and applications for mechanical measurements. **Tektronix, Inc,** Beaverton, Ore.
Circle 319 on Inquiry Card

Fiberoptic Communication Cable

Specs, graphs, and drawings highlight data sheets for line of single-channel fiberoptic communication cables including step index, graded index, and single mode types. **Valtec Corp,** West Boylston, Mass.
Circle 320 on Inquiry Card

Memory Systems

Divided into three sections which identify the range of standard and add-in/on products, and custom design capabilities, catalog includes specs, applications, and a "make vs buy" discussion. **Intel Memory Systems,** Sunnyvale, Calif.
Circle 321 on Inquiry Card

Switches

Complete with engineering and specification data, charts, options, photos, and dimensional diagrams, switch selection guide describes line of single and double break, DIP pushbutton, and industrial and sealed limit switches. **Licon, a div of Illinois Tool Works, Inc,** Chicago, Ill.
Circle 322 on Inquiry Card

Synchro Converters and Encoders

Detailed catalog provides specs, applications, and features for synchro converters, displays, and encoders, as well as multispeed digital-to-synchro and synchro-to-digital converters. **Computer Conversions Corp,** East Northport, NY.
Circle 323 on Inquiry Card

A-D Converters

Two technical bulletins with tables, diagrams, and outline drawings consider construction, performance specs, operation and PC board layout for series 873-78 and -88 ADCs. **Beckman Instruments, Inc, Helipot Div,** Fullerton, Calif.
Circle 324 on Inquiry Card

MOS/LSI 1-Chip Microcomputers

Data manual describing the TMS1000 series MOS 4-bit microcomputers covers applications, product and design support data, and electrical and mechanical specs, including flowchart, tables, and diagrams. **Texas Instruments, Inc,** Dallas, Tex.
Circle 325 on Inquiry Card

Mass-Terminated Connectors

Full-color brochure with photos, drawings, tables, and charts indicates performance data, assembly procedures, and mechanical and electrical features of cable connectors and headers, plus specs for ribbon cables. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 326 on Inquiry Card

Network Design Tools

Guidebook entitled "Software Tools for Network Design and Analysis" examines use of computer-aided techniques, provides background material on network architectures, and offers practical guidelines. **Network Analysis Corp,** Glen Cove, NY.
Circle 327 on Inquiry Card

SC/MP Microprocessor

A microprocessor users manual is available describing the SC/MP (PACE) PROM Programmer (publication number 420305 306-001A). For copy write to **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Interactive Data Processing

Explaining how systems fit into business applications without disrupting existing procedures, brochure details data base management software (DBMS) and provides configurations. **Prime Computer, Inc,** Framingham, Mass.
Circle 329 on Inquiry Card

8-Bit MOS Microprocessor

In addition to complete descriptions of CPU and major support circuits, the *8080A/9080A MOS Microprocessor Handbook* details timing diagrams, memory and interface circuit descriptions, and applications. Price is $7.95. **Advanced Micro Devices, Inc,** Sunnyvale, Calif.
Circle 330 on Inquiry Card

Image Digitizer and Display Terminal

Theory, operation, and specs of the Eye-Com picture digitizer and display are furnished in handbook illustrated with block diagrams, tables, curves, and actual digitized pictures. **Spatial Data Systems, Inc,** Goleta, Calif.
Circle 331 on Inquiry Card

A-D Signal Converter

Illustrated data sheet features descriptions, applications data, specs, and mechanical drawings on the CYAD-14QM successive approximation analog-to-digital signal converter. **CPS, Inc, Converter Products,** Sunnyvale, Calif.
Circle 332 on Inquiry Card

Power Transistors

Series IR 708 and 709, 900-V power transistors, are described in data sheet which presents features, specs, dimensional drawings, sample test circuits, and five rating curves. **International Rectifier, Semiconductor Div,** El Segundo, Calif.
Circle 333 on Inquiry Card

Flat Cables

Summarizing electrical and physical properties of bonded and laminated cables and termination techniques, catalog discusses crosstalk data and applications. **Belden Corp, Electronic Div,** Richmond, Ind.
Circle 334 on Inquiry Card

CRT Terminals

Separate brochures describe two low cost CRT terminals with built-in microprocessors—the Fox-1100, a sophisticated basic terminal, and the Owl-1200, an intelligent editing terminal. **Perkin-Elmer Data Systems, Terminal Div,** Randolph, NJ.
Circle 335 on Inquiry Card

Data Communications Backup

Folder with photos and specs details information on backup measures and restoral techniques for private lines and modems and explains considerations for real-time online systems. **Intertel,** Burlington, Mass.
Circle 336 on Inquiry Card

Alphanumeric Display Subsystems

Characteristics, power requirements, filter information, character fonts, and installation drawings can be found in brochure describing ARGUS gas discharge dot matrix display subsystems. **Industrial Electronic Engineers, Inc,** Van Nuys, Calif.
Circle 337 on Inquiry Card

CMOS Digital Logic ICs

Basics of the B-series of COS/MOS high voltage ICs are examined in guide which furnishes function classification and selection charts, electrical characteristics, and function diagrams. **RCA/Solid State Div,** Somerville, NJ.
Circle 338 on Inquiry Card

Solid-State Relays

Full electrical and mechanical specs, operating parameters, features, block diagram, and package dimensions are provided in technical data sheet pertaining to series 7500 panel mounted relays. **Hamlin Inc,** Lake Mills, Wis.
Circle 339 on Inquiry Card

Miniature dc-dc Converter

Flyer on high power (5 V at 1 A) fully isolated dc-dc converter includes input and output specs, functional schematic case dimensions, and terminal arrangement drawings. **Powercube Corp,** Waltham, Mass.
Circle 340 on Inquiry Card

MOS/LSI Circuits

Cross-reference table and second-source listings are mentioned in short-form catalog which features such products as multiprotocol synchronous and async/sync receiver-transmitters, and controllers. **Standard Microsystems Corp,** Hauppauge, NY.
Circle 341 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

GUIDE TO PRODUCT INFORMATION

CIRCLE 130 ON INQUIRY CARD

CIRCLE 131 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

CIRCLE 133 ON INQUIRY CARD

CIRCLE 134 ON INQUIRY CARD

ADVERTISERS' INDEX

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Gotcha, DEC!

SuperTerm™

Yes, we gotcha DECwriter and we did it with such standard features as: matrix impact printing, 132 column print width, microprocessor electronics, portability (SuperTerm weighs less than 50 lbs.), high speed (10, 15, 30, 45 and 60 characters per second are standard with 120 and 200 CPS being optional), an IBM Selectric configured keyboard, a "gear shifted" alphanumeric key pad, a quick loading cartridge ribbon system, horizontal tabs (variable *and* fixed), vertical tabs, programmable keyboard lockout, text-optimized printing and forms control—all standard.

In addition, SuperTerm's unique "ballistic" printhead design is warranted for an entire year. This means that during the warranty period, should you ever encounter defects in printhead workmanship, Intertec will replace or repair the defective component *free!*

It's really just that simple and that super — a printhead warranty 4 times longer than DEC's.

End users will be pleased to learn that the Intertec SuperTerm provides all of this capability and more at a price of only $1995 — quantity one.

Low cost options available on every SuperTerm include: 200 CPS printing, super and subscripting, variable vertical pitch, pagination (automatic top of form), direct X/Y addressing, adjustable left and right margins, automatic reverse printing, double-width characters, automatic CR on end of line, a font programmable character set, and a 1200 baud communications package consisting of 120 CPS printing, dynamic buffer control, 202C interface compatibility (w/reverse channel) and automatic reverse printing.

If your application calls for APL/ASCII, Super Term has that too. In fact, Super Term has got just about everything — except competition.

Want more? You've got it! A built-in micro-cassette (Supercette™) is available for only $900 in single quantities with OEM discounts available.

In addition to unparalleled price and performance, every SuperTerm is backed by Intertec's nationwide factory trained service network with over 160 service centers strategically located coast to coast.

For more information on the total performance and unparalleled low price that make the Intertec SuperTerm the very best buy for your terminal dollar, just call Intertec Data Systems, the only company with international sales, service and the revolutionary SuperTerm.

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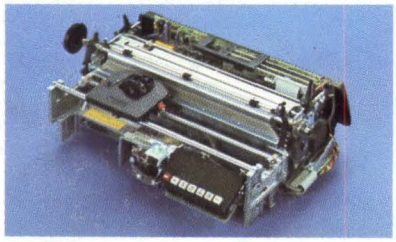
See Us at Booth 1765

CIRCLE 142 ON INQUIRY CARD

Matrix Horsepower

A 100% Duty Cycle Makes Ours The Workhorse of Matrix Printers!

Inherent Diablo ruggedness and reliability and our unique ballistic head design give our Matrix printer a 100% duty cycle. Add to that, bidirectional printing, high speed tabbing, skip-over spacing and vertical forms control and the result is greater throughput. Our wide-gap ballistic head means paper clearances are never a problem and field head change requires only an allen wrench – no alignment! (All this plus incremental printing capability make our printer an ideal component for a workhorse terminal.) For a complete product demonstration, Diablo Systems, Inc., 24500 Industrial Blvd., Hayward, California 94545, Diablo Systems, S.A., Avenue de Fre 263, 1180 Brussels, Belgium, or Mitsui & Company, Ltd., 2-1 Otemachi 1-Chome, Chiyoda-ku, Tokyo.



Diablo

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CIRCLE 143 ON INQUIRY CARD