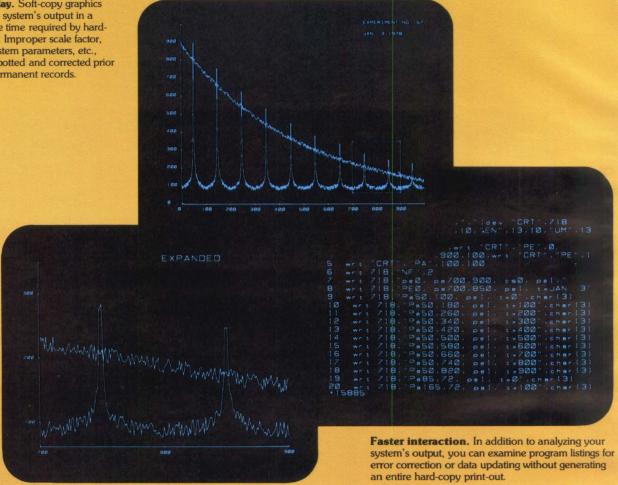
# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS



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- \* HP's implementation of IEEE Standard 488-1975.
- \*\* Domestic U.S.A. price only.



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# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

**MAY 1978** 

**VOLUME 17, NUMBER 5** 

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### **DIGITAL TECHNOLOGY REVIEW**

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### DIGITAL CONTROL AND **AUTOMATION SYSTEMS**

Five distributed microcomputers in Five distributed microcomputers in Texas Federal Center have reduced electrical demand by 38% and electrical consumption by 49%—while also controlling HVAC equipment, providing smoke and fire detection, and preventing unauthorized entry. In another system, engineers at a California amusement park designed a lighting and air conditioning control system around three microcomputer kits

### MICRO PROCESSOR/ 214 COMPUTER DATA STACK

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Ink-jet printer for mini and microcomputer based systems achieves low cost and high reliability through use of "drop on demand" ink dispensing technique

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### FLOPPY DISC-BASED EMULATOR REPLACES PAPER TAPE READER 192

To replace and update original equipment paper tape readers used in factory test sets for checking telephone switching units, a microcomputer-based disc-storage emulator has been designed for direct substitution, resulting in substantial test time and maintenance cost savings

### LOW COST DATA ACQUISITION SYSTEM **USING STANDARD DIPs** 200

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Four dual-in-line packages can be designed onto a small printed circuit card to obtain a low cost, high performance data acquisition system that includes all interfacing

## CONFERENCE

### 1978 NATIONAL COMPUTER CONFERENCE 66

This year's conference will include a technical program of over 100 sessions, exhibits representing more than 330 organizations, and special events including a personal computing festival, professional development series of seminars, and an energy symposium

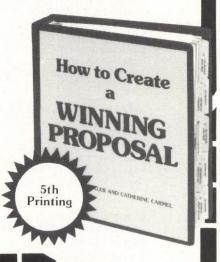
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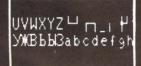
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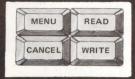
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# CALENDAR

# CONFERENCES

- MAY 22-23—Lightwave Communication Trade Show, Park Plaza Hotel, Boston, Mass. INFORMATION: Fiber Optic Con, c/o Conventures, Inc, 11 Newbury St, Boston, MA 02116. Tel: (617) 267-0055
- MAY 22-25—2nd Minnesota Electronics Manufacturing and Assembly Conf and Expo (Minnex II), St Paul Civic Ctr, St Paul, Minn. INFORMATION: Kevin Miller, Society of Manufacturing Engineers, 20501 Ford Rd, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500, X417
- MAY 22-26—7th Annual Sym on Incremental Motion Control Systems and Devices, Hyatt Regency O'Hare, Chicago, III. INFOR-MATION: Prof B. C. Kuo, Dept of Electrical Engineering, U of Illinois at Urbana-Champaign, Urbana, IL 61801. Tel: (217) 333-4341
- MAY 23-25—ELECTRO '78, Boston-Sheraton, Hynes Auditorium, Boston, Mass. INFORMATION: W. C. Weber, Jr, IEEE ELECTRO, 31 Channing St, Newton, MA 02158. Tel: (617) 527-5151
- MAY 24-26—8th Internat'l Sym on Multiple Valued Logic, Sheraton O'Hare Motor Hotel, Chicago, III. INFORMATION: A. S. Wojcik, Dept of Computer Science, Illinois Institute of Technology, Chicago, IL 60616. Tel: (312) 567-5153
- JUNE 4-7—Internat'l Conf on Communications, Sheraton Hotel, Toronto, Ontario, Canada. INFORMATION: F. J. Heath, Power System Operation Dept, Ontario Hydro Electric Power System, 700 University Ave, Toronto M5G 1X6, Canada
- JUNE 5-7—Conf on Pattern Recognition and Image Processing, Chicago, III. INFORMA-TION: K. Preston, Jr, Dept of EE, Carnegie-Mellon U, 5000 Forbes Ave, Pittsburgh, PA 15213
- JUNE 5-8—1978 Nat'l Computer Conf (NCC), Anaheim Conv Ctr, The Disneyland Hotel Comp, Anaheim, Calif. INFORMATION: AFIPS, 210 Summit Ave, Montvale, NJ 07645. Tel: (201) 391-9810
- JUNE 12-13—Microcomputer-Based Instrumentation Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Bradford M. Smith, Rm A130 Technology, National Bureau of Standards, Washington, DC 20234. Tel: (301) 921-2381

- JUNE 15—17th Annual Technical Sym of ACM and NBS, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: U.S. Dept of Commerce, National Bureau of Standards, Washington, DC 20234
- JUNE 19-21—Design Automation Conf, Caesar's Palace, Las Vegas, Nev. INFOR-MATION: Steven A. Szygenda, Dept of Electrical Engineering, U of Texas, Austin, TX 78712. Tel: (512) 471-7365
- JUNE 19-22—Distributed Data Processing, Jack Tar Hotel, San Francisco, Calif. IN-FORMATION: AIIE Seminars, Dept PR, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500
- JUNE 21-23—Internat'I Sym on Fault Tolerant Computing, Toulouse, France. INFOR-MATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901
- JUNE 26-28—36th Annual Device Research Conf, U of California, Santa Barbara, Calif. INFORMATION: James C. McGroddy, 1978 DRC Chm, IBM T. J. Watson Research Ctr, Yorktown Heights, NY 10598. Tel: (914) 945-1228
- AUG 6-9—3rd Jerusalem Conf on Information Technology (JCIT), Jerusalem, Israel. INFORMATION: Anthony Ralston, SUNY at Buffalo, 4226 Ridge Lea Rd, Amherst, NY 14226
- AUG 21-25—4th Internat'l Congress of Cybernetics and Systems, Amsterdam, The Netherlands. INFORMATION: Dr J. Rose, c/o College of Technology, Feilden St, Blackburn BB2 1LH, Lancashire, England
- AUG 22-25—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: Dr Charles S. Elliott, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812
- AUG 28-SEPT 1—8th Australian Computer Conf, Canberra, Australia. INFORMATION: ACS-8 Programme Committee, PO Box 448, Canberra, ACT 2601, Australia
- SEPT 4-6—5th Nat'l Systems Conf, Punjab Agricultural U, Ludhiana, India. INFORMA-TION: Dr R. K. Varshney, Organizing Secretary, NSC 78, Dept of Electrical Engineering, PAU Ludhiana 141004, India
- SEPT 5-8—COMPCON Fall '78, Capital Hilton, Washington, DC. INFORMATION: COMPCON Fall, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

- SEPT 6-8—Internat'l Optical Computing Conf, Imperial College, London, England. INFORMATION: S. Horvitz, Box 274, Waterford, CT 06385. Tel: (203) 442-0771
- SEPT 12-14—Western Electronic Show and Convention (WESCON), Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: W. C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965
- SEPT 19-22—Conf on Microprocessors in Automation and Communications, U of Kent at Canterbury, England. INFORMATION: Conf Secretariat, Institution of Electronic and Radio Engineers, 99 Gower St, London WC1E 6AZ, England
- SEPT 26-29—4th Internat'l Conf on Computer Communication (ICCC-78), Kyoto Internat'l Conf Hall, Kyoto, Japan. INFORMATION: ICCC-78 Executive Committee, c/o Internat'l Affairs Bureau NTT, 1-6, Uchisaiwai-cho, 1-chome, Chiyoda-Ku, Tokyo 100, Japan
- OCT 17-19—EUROMICRO 78, 4th Sym on Microprocessing and Microprogramming, Munich, Germany. INFORMATION: Dr Helmut Berndt, Siemens AG, Dv WS PZ1, Postfach 70 00 78, D-8000 Munichen 70, West Germany

# SEMINARS

- JUNE 19-23—Charge-Coupled Devices: Operation and Applications, Northeastern U, Burlington, Mass. INFORMATION: Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: (617) 964-1412
- JUNE 21-23—Sym on Machine Processing of Remotely Sensed Data, West Lafayette, Ind. INFORMATION: D. Morrison, LARS-Purdue U, 1220 Potter Dr, West Lafayette, IN 47906

# SHORT COURSES

- MAY 31-JUNE 2—Software Design for Data Communications Systems, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106
- JUNE 5-9—Microcomputer Workshop, Carnegie-Mellon U, Pittsburgh, Pa. INFORMATION: Post College Professional Education, Carnegie Institute of Technology, Carnegie-Mellon U, Schenley Pk, Pittsburgh, PA 15213. Tel: (412) 578-2207
- JUNE 19-30—Computer Techniques for Real-Time Control and Monitoring of Power Systems, U of Wisconsin, Madison, Wis. IN-FORMATION: Willis F. Long, Dept of Engineering, U of Wisconsin-Extension, 432 N Lake St, Madison, WI 53706. Tel: (608) 262-2061

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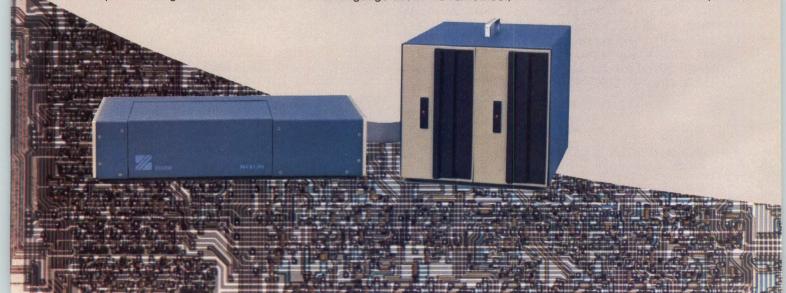
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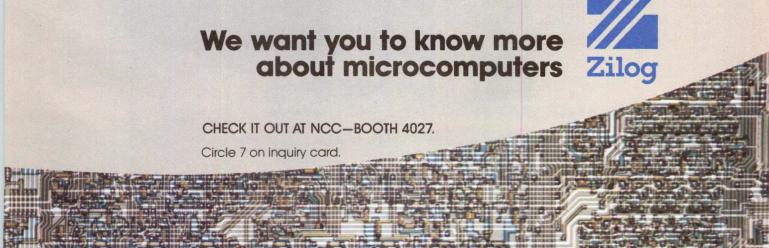
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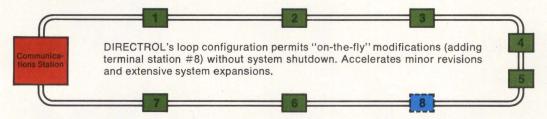






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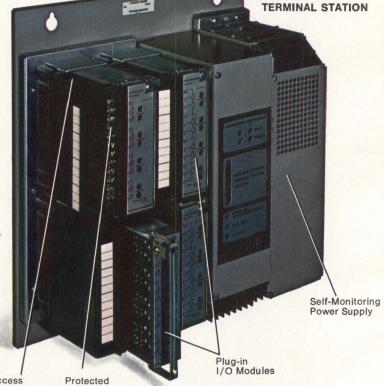
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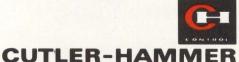
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# MANAGEMENT AUTOMATION APPLICATIONS

John E. Buckley

Telecommunications Management Corporation Cornwells Heights, Pennsylvania

Beginning as specific interactive applications in the late 1960s, information management systems strove to provide the management of a diverse, complex organization with more meaningful timely information concerning the dynamics of their operating environment. These initial endeavors addressed primarily the material control and financial aspects. As successes were realized, additional dimensions of these and other peripheral application areas became subject to the advantages of interactive processing using database management technology.

Four elements or phases—data collection, data reporting, data modification, and data reaction—were always planned with these development activities, regardless of the specific application. The objective was to fully automate each phase so that its execution would always be compatible with its purpose. To delay or handicap that purpose because of inherent automation activities resulted in a less than ideal application system.

Data collection was the timely gathering of the application's associated source data from the numerous locations at which they would be expected to occur. Development of display terminals, particularly in cluster configurations, was stimulated and directed by the necessity to automate this data collection phase.

Data reporting was contingent upon the development and refinement of database systems, and the refinement of exception reporting and interactive software capabilities. To merely collect source data was only a partial step toward an information system; it was also necessary to compile the assimilated data into timely reports for management evaluations and decisions. Traditional data reporting consisted of periodic computer printouts on a weekly or daily basis. Gradually it was refined to present only exception and trend data. Exception reports typically identify deviations from pre-entered norms or from nominal parameters that have been compiled from data previously processed by the system. Trend reporting also

uses historical data to show management the characteristic flow of the application with respect to time, and in some cases attempted to use this data to project future conditions.

It was not until the early 1970's that data modification and reaction phases were introduced and became significant elements of an information system. Even then they were applied only in a batch environment without the same time characteristic inherent in the first two phases.

Data modification permitted an organization's management to introduce variations as temporary or permanent changes to an accumulated data base. Every information system directed to the collection, manipulation, and dissemination of real data has been confronted with the management question of "what if this should change?" Thus, this phase modified the database content to provide a proper, timely response to that inquiry.

Data reaction was the ability of an information system to accept these hypothetical or real data modifications and react immediately; to wait hours or days would destroy any human analytical or response capabilities. For example, with batch program coding and compilation as opposed to interactive programming, a programmer would prepare the coding in a void for the former case, submit it for batch data entry, wait for compilation or program test time on the computer, and wait again for the results to determine its correctness. The magnitude of elapsed time can be such that the programmer will have lost the sense and flow of his original thought processes. Development of a management decision that must be formulated by multiple manipulations of a data base can result in the same ineffectiveness if similar time delays are encountered.

A possible fifth phase, considered part of data modification, is data inquiry activities. Management must be able to access specific record(s) in a data base to deter-

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Computer model and operating system

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City, State and Zip

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mine and verify the required modifications. Multiple and selective record accesses and summations are also permitted.

These aspects of an information system are present in automated environments today, since all the necessary technology exists. A true management automation system, however, is still to be fully attained. The missing elements are the development of appropriate data collection and management terminals, together with a product area referred to as interactive concentrators.

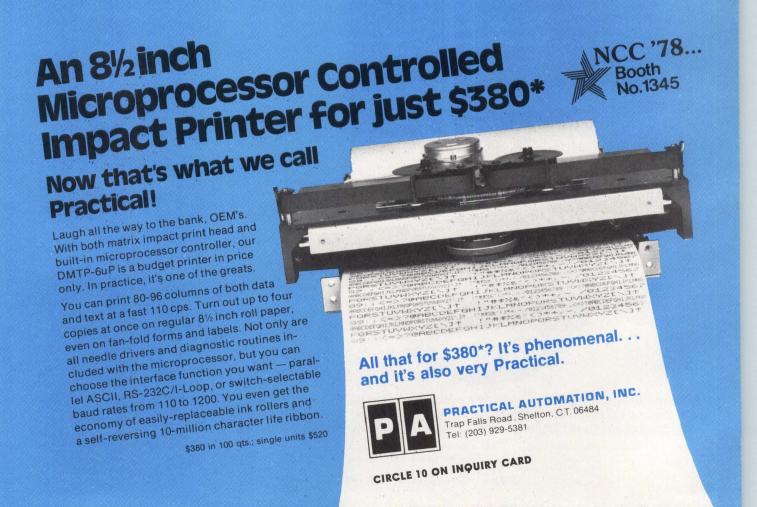
It has not been universally implemented that each source of data be equipped with an online data collection device so that every management employee would have access to a terminal permitting data inquiry, modification, reporting, and reaction. In most information system applications, source data are gathered manually to a point where it is economically feasible to automate their entry into a centralized database and processing system. The majority of data terminals have been designed for a computer-type operating environment and are not intended specifically for the management office operational environment. Information systems have been and are currently focused on the hardware and software developments resident at the centralized computer processing center.

Dependent upon the present capabilities of an information system, the ability to extend and multiply its accessibility to all facets of an organization will provide a true management automation capability. A meaningful analogy can be found in the evolution of the telephone system. The early telephone system was totally manual; the end subscriber verbally provided the telephone number to the local operator who verbally requested the de-

sired connection from other intermediate operators. The ability of the local telephone operator to directly dial the desired connection to the destination local operator was the first step in automation. The final step of telephone network automation permitted the end subscriber to dial the telephone number directly. Management automation's final step, in comparison, will permit the management employee to directly store, interact, modify, and receive the desired data.

A management automation application can be segmented into five equipment and facility areas: centralized processing center, long distance communications facility, local interactive concentrator, local communications network, and management terminals. The centralized processing center and long distance communications facility already exist with today's information systems. The local data communications network also exists in the form of an organization's internal telephone system controlled by a traditional private branch exchange (PBX) or the newer computerized branch exchange (CBX). The local interactive concentrator and management terminal areas require finalized development of application specifications and actual products.

Continual access and interaction with a centralized database management and processing system usually are unnecessary with a management automation system. Unless the geographic distribution of potential terminals and the centralized processing center are in close proximity, the long distance communications cost coupled with the expected interactive traffic loadings would economically impact the desired system. Since the management automation system is dedicated to collection, demand manipulation, and transient modification and processing of data,



What the world needs now is a real-time microcomputer system you can program and debug in a simple, high level, interactive language.

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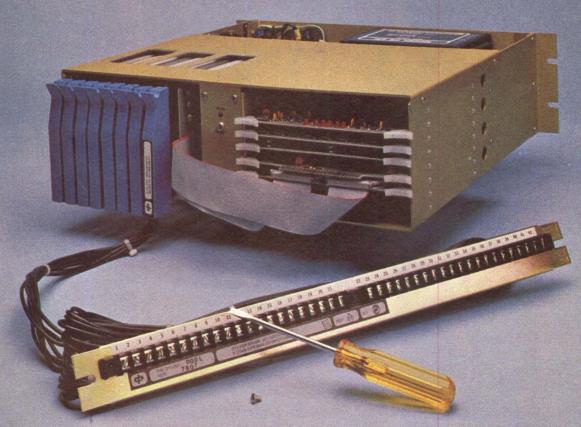
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the need to operate with a totally merged data base is minimal. Therefore, each functional area such as a plant location or a department can be considered as an entity. The processing would encompass only source data collected during a recent interval from this contained environment. The existence of historical data and events would also be necessary, and the centralized processing center would still have to merge the data from all environments to produce periodic reports.

Once a specific operating environment is defined and functional allocations assigned, the determination may be made as to whether the communications facility between the centralized processing center and contained environments warrants the use of leased or switched communications. Ideally, the various functions should be assigned so that a switched communications facility could be employed. The inherent redundancy with switched facilities should offset the lower data rate. The centralized processing center should access each of its contained environments several times each day to collect current source data and update any historical parameters. This center must also be capable of a demand access request from a contained environment.

Control and intelligence residing in a contained environment are the local interactive concentrators that communicate directly with the centralized processing center. Basically, a local interactive concentrator consists of a mini or microcomputer-controlled storage. Concentrators must have high speed data transmission capability for communications with a centralized processing center, and multiple low speed data access for communications with the environment's management terminals. A multiplicity of concentrators could be placed at a single location, with each one dedicated to a specific application



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area, such as accounting, personnel, inventory, manufacturing, sales, customer service, and office management.

The interactive concentrator's role would be to collect its application's source data from within its associated environment, store them, and then use them for processing of pre-established parameters, limited status, and exception reports. The concentrator must respond to inquiry and demand access, data modification entries, and specialized processing requests from a management terminal. If the requested processing was beyond the capability of the interactive processor or if it required data from other locations or applications, a request for access to the centralized processing center would be generated. The centralized processing center would perform the actual processing and return it to the concentrator, which would deliver it to the requesting management terminal. The majority of the terminal's interaction should involve only a concentrator.

For a true management automation system, the local data communications network must be controlled by a CBX ("Office Automation," Computer Design, Nov 1977, pp 14, 20). The CBX would recognize the type of transaction desired by a management terminal and select the associated interactive processors that should be accessed. Feasibly, the CBX could also recognize whether the transaction involved more than one concentrator, and could obtain and assimilate the various application information from the different concentrators into a combined response to the requesting management terminal. A concentrator requesting access to the centralized processing center would notify the CBX to accomplish the access. Conversely, if the centralized processing center performed data collection and updating with the remote concentrators, the processing center would interrogate only the associated CBX.

The management terminal would replace the primary telephone instrument associated with the CBX. During nondata activities, this terminal would be used to place and receive normal telephone calls; in the data environment, primary input capability would be keyboard entry with a display output. An additional output advancement would be to have an audio response capability associated with the CBX. Digital response from an interactive concentrator could then be converted into an audio response by the CBX for delivery to the management terminal. Peripheral devices such as media readers, printers, displays, and expanded keyboards could also be connected to the management terminal, further adapting the terminal to its operating environment.

Application development of products directed to management automation systems is necessary. Although the CBX was introduced to the marketplace less than four years ago, there are now estimated to be over 6000 in operation. In addition, interactive concentrators in the form of microcomputer disc systems driven by p/ROMS are available from several manufacturers. Such a system with a 256k-byte disc has a list price of less than \$2200; a larger disc capacity system from another manufacturer lists at under \$3000. The missing link has been the management terminal. Such a terminal was presented by a West German manufacturer at the May 1977 Hanover Fair in Hanover, West Germany; and a U.S. manufacturer of computerized telephone systems recently announced an electronic telephone set that encompasses a microprocessor, RAM, and p/ROM-operated display, comparable in price to a traditional 10-button telephone set.

As with all new applications, both technological and user maturity must occur. The technological component is available. With meaningful examples of management automation being implemented, the users' desire can be expected to develop rapidly.

# Now you can solve your data communications problems at super-high baud rates.

These two new 2650 LSI peripherals interface with any microprocessor, and offer on-chip performance which shrinks hardware/software costs.

Whether you're designing data communications systems for a byte-control protocol like BISYNC, or for one of the newer bit-oriented disciplines like SDLC, you won't find a more cost-effective, higher performance interface

capability than you get with the newest LSI additions to the Signetics 2650 family.

These two data communications
ICs can satisfy virtually every
interface requirement. They
help speed data flow between
CPUs or between CPU and terminals. The 2651 Programmable Communications Interface
(PCI) combines USART functions
with an on-chip baud-rate generator, modem controls and BISYNC
support. The 2652 Multi-Protocol Communications Controller (MPCC) handles
many popular line protocols and can interface with either a microprocessor or minicomputer data bus. Both devices are TTL-

compatible and operate from a single +5V power supply. Move Data at 800,000 Baud. With the 2651 PCI, you can serialize and deserialize data at rates up to 800,000 baud. Interfaced with any microprocessor, this versatile IC can be used in a polled or interrupt-driven system—count on it to support many serial data disciplines, both synchronous and asynchronous, in the full- or half-duplex mode.

Moreover, the 2651 PCI can be programmed either to accept an external clock or to generate an internal transmit/receive clock. In the internal mode, you can program any of 16 different baud rates, from 50 to 19,200 baud.

2651/2652 SELECTION GUIDE 2651 (PCI) 2652 (MPCC) Rcv/Xmt Modes Synchronous and Asynchronous | Synchronous SDLC, HDLC, ADCCP, DDCMP, **Protocol Compatibility** BISYNC, DDCMP BISYNC (limited). Baud Rate DC to 800,000 baud DC to 1,500,000 baud, typical External or On-chip **Baud Rate Generation** External (16 internal rates) Microprocessor or Minicomputer Microprocessor Data Bus Compatiblity (8-bit tri-state) (8- or 16-bit tri-state) Modem Controls None Odd/Even VRC, CRC-16, **Error Controls** Odd/Even VRC CRC-CCITT Local/Remote Loop Back Self-test Local Loop Back 28-pin DIP 40-pin DIP Package \$13.70 Price (100 Qty) \$24.90 Availability Immediate Immediate

Link With 8- or 16-Bit Bus. The 2652 MPCC works with either an 8-bit or 16-bit data bus, and handles both bitoriented and byte-control protocols. That means you can use it with microprocessors or minis, and with almost any discipline, including SDLC, HDLC, ADCCP and DDCMP.

When you design in the 2652 MPCC, you design in flexibility. It gives you high-speed operation — up to 1,500,000 baud — plus on-chip features which reduce hardware and software costs. This LSI device contains programmable circuitry for performing CRC generation/checking and zero insertion/deletion, as well as SYNC or secondary address comparison.

If you're designing data communications systems, you need to know all about the new 2651 PCI and 2652 MPCC cir-

cuits from Signetics. To get the full story, use the coupon below or contact your local Signetics Distributor.



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	☐ I have an urgent requirement. Ple specialist phone me at once: (	The second secon
9	Name	Title
-	Company	Division
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	City State	Zip

# Controllers Expand Distributed System, Adding Peripherals, Source Data Entry, Network Productivity Aids, and Protocol

Introduction of the low cost, limited capacity MARK I and the extended, higher speed MARK II to expand the PTS/1200™ distributed processing system is regarded by Raytheon Data Systems Co, 1415 Boston-Providence Tpk, Norwood, MA 02062 as the start of the second generation of distributed processing technologymarked by improved equipment and network performance coupled with the maintenance of existing investments in data communications and host processing software. Totally compatible with existing PTS/1200 systems, both models can perform intelligent 3270-type emulation tasks, local format storage, and local printing concurrently with the processing, file handling, and communications functions of the current system.

MARK I consists of a central processor with 64k bytes of main memory (expandable to 128k bytes) and a self-contained 10M-byte disc storage drive. Up to eight 1920-character video display stations and moderate speed, medium capacity peripherals such as printers, mag tape drives, and card reader equipment can be supported. A typical 4-terminal MARK I system leases for under \$850/month, including maintenance, on a 3-year lease term.

With a faster central processing subsystem, the MARK II has 128k of main memory and supports up to 24 1920-character visual display stations. Large capacity peripherals and up to 20 1/0 device connections, in addition to terminal stations, can be accommodated. Peripheral products announced include the model 3820 disc storage module, an 80M-byte toploading drive with removable 20surface disc cartridge; the model 3306 high speed printer, a 600-line/min, 132-column drum device; and the model 3910 magnetic tape transport, a 9-track format, 1600-bit/in (630/ cm) drive with a 120k-byte/s transfer rate. A typical 16-station system leases for \$2625/month on a 3-year basis.

Among 20 capabilities to be incorporated in the products are synchronous data link control (splc) communications protocol, source data entry, and communications network productivity enhancements. The features will be deliverable in PTS/1200 equipment shipped in July.

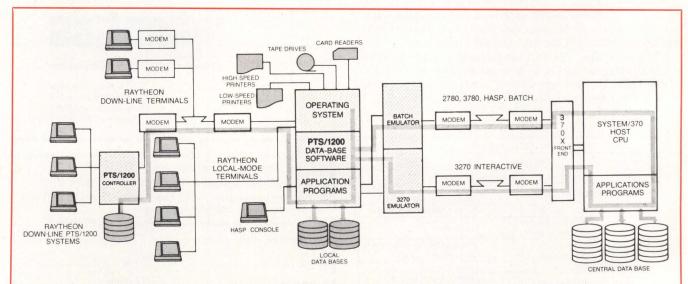
Communications interconnect options offer binary synchronous protocols for 3270 interactive communication, 2780 and 3780 batch, and hasp multileaving for remote job entry. SDLC protocol supports batch

and interactive transmissions simultaneously on a single communications line (to be available on the system in the fourth quarter of this year).

Five network aids also have been added. A downline terminal control feature permits any PTS/1200 system to monitor and control, independent of and transparent to a host mainframe, either a network of PTS-100 terminals or other PTS/1200 systems under IBM 3270 protocols.

A teleprinter concentrator consisting of hardware and software allows users with large teleprinter networks to consolidate such message traffic on the same lines used to support PTS/1200 communications, providing high speed autoanswer capabilities. Key to the capability are microprogrammed general-purpose communications adapters, each of which controls four half-duplex lines; five adapters can be attached to each controller.

Containing IBM TSO software facilities, an enhanced editor performs pre-editing on PTS/1200 systems to assist in program development for host computers. Code is developed and stored locally, and is then batched and sent to the host for analysis, editing, and debugging. Downline program loading permits transmission of programs from central to remote sites;



PTS/1200 MARK I and II systems of Raytheon Data Systems feature enhanced capabilities, communications protocols, and more peripherals. Video display terminals can operate in local mode connection to controller at distances up to 5000 ft (1.5 km). Independent of the user, applications program decides which data base to access

# WE JUST PUT TWO BIG HAMMERS IN ONE SMALL PACKAGE WITHOUT DRIVING COSTS UP.

If you're looking for higher current and higher voltage without paying higher prices, Fairchild's new SH3011 Dual 5-amp Hammer Driver hits the nail on the head.

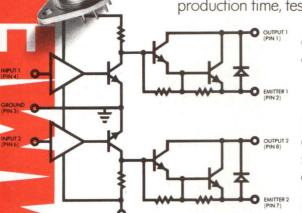
# **BIG SAVINGS.**

Our new dual hammer driver was designed as an alternative to  $2\frac{1}{2}$  x  $2\frac{1}{2}$  circuit boards that end up costing you a small fortune in time and parts.

So now whenever you need high-power for driving impact printer heads, solenoids or motor controls, you can plug in a SH3011 and save about half the TTL gates, darlingtons and transistors you'd need otherwise.

Which, in turn, saves you insertion time, production time, test time, labor and inventory.

And all those savings added together can greatly reduce your overall system cost.



# **BIG PERFORMANCE.**

Each of the SH3011's two independent hammers is capable of sinking 5-amps of current. Each output is designed to withstand 80 volts between the collector and emitter. And each driver is TTL compatible.

The SH3011 comes compactly and hermetically sealed in a steel, 8 lead TO-3

package to improve reliability and eliminate heat sink.

For details on our newest Hybrid (or on any of our other Hybrid products), just contact your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to reach our Hybrid Division.

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CALL US ON IT. (415) 962 - 3771 remote debug facilitates program patching of software routines operating on terminals at sites remote from the PTS/1200 central controller.

Edit, arithmetic, and logical functions in the parameter-driven source data entry package permit nonprogrammers to set up data entry jobs. An interactive program is used to define job parameters through simple conversational dialogue; maximum record size supported by the system is 1600 characters.

Interactive cobol, to supplement the MACROL language, and Videotype<sup>™</sup> word processors with resource sharing capabilities are currently under development for the MARK I and II systems. Also, 3274/3276 capabilities will soon be supported on the PTS-100 and /1200 lines. Circle 290 on Inquiry Card

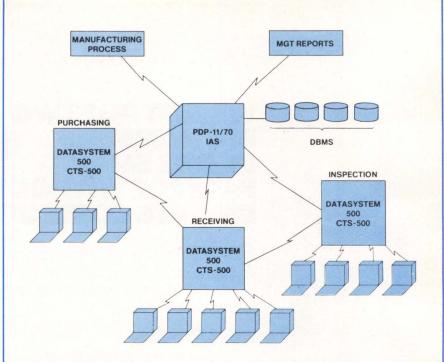
# Network Software Items Introduce Online Distributed Processing

A second phase of DECnet software permits configurations of distributed processing networks encompassing a wide selection of hardware and operating systems. The new and enhanced products of Digital Equipment Corp, Maynard, MA 01754 enable communication among most of the company's major operating systems and computers, ranging from the LSI-11 microcomputer to the VAX-11/780 (see *Computer Design*, Dec 1977, pp 27-28).

The user can link real-time systems for industrial and scientific monitoring and control, timesharing systems for commercial and educational applications, and interconnect timesharing, real-time, and multifunction nodes for broad-based management information systems.

DECnet comprises software modules, protocols, hardware, and support services that facilitate construction of distributed computer networks among the computers. It is intended to extend resources of local computer systems, not to enlarge the dependence on central systems. Products thus support general system interconnectability and permit such network configurations as hierarchical, "star," "ring," and random topology structures.

Introduced are the DECnet-VAX, a network software interface for VAX-



As typical installation, commercial network for manufacturers includes remote Datasystem 500s that perform terminal-oriented transaction processing, exchange data among themselves using DECnet/E, and update an inventory data base residing on PDP-11/70 system running IAS and DBMS-11. PDP-11/70 also supports local users for management reporting and program development. Second phase of software products, introduced by Digital Equipment Corp, are optimized for nature and size of task to be done, eliminating use of "all-purpose" operating system

11/780 computers running under the VMS operating system; DECnet-RT for PDP-11 computers running under the RT-11 real-time operating system; and DECnet/E for the PDP-11/34 to -11/70 systems operating under RSTS/E. Enhanced versions were announced for systems using the real-time executives RSX-11D, RSX-11M, and core-only RSX-11S, and for the multifunction IAS operating system.

The network's remote resource access permits programs or users at one node to utilize mass storage peripherals and I/O devices at another node. It allows a program to open files at a remote node and to perform sequential input or output of data in that file. Updates conform to modifications in three protocols that make up the digital network architecture—the network service protocol (NSP), data access protocol (DAP), and digital data communication message protocol (DDCMP)—to support future product developments.

Common features are full point-topoint interconnect capability for taskto-task communication, by which programs running on separate network nodes can exchange 8-bit ASCII data, and for file transfer, which allows ASCII sequential files to be copied from one node to another on user command. Also included are greater network throughput, simplified network configuration and generation procedures, dynamic reconfiguration, and ability to switch lines without interruption of service.

License fees are \$1500 for the DECnet-RT and -S systems; \$2700 for -M, /E, and -VAX; and \$3500 for -D and -IAS. This includes warranty and support services.

Circle 291 on Inquiry Card

# Video System Transmits TV Pictures and Data Via the Telephone

Designed for use with normal dialup telephone networks, leased lines, radio links, microwave, or satellite channels to provide low cost visual communications, the model 260B video compressor accepts signals from



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Good product, the 4014.™ So good, in fact, that we designed our MEGRAPHIC 5014 Refresh Graphics System to do everything the 4014.™ does, and more.

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But, best of all, the MEGRAPHIC 5014 costs substantially less than comparable systems. For the OEM, that means better margins. And, for the sophisticated end

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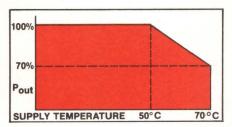
ICEMAN's here with heat-busting

ICEMAN's here with correct balance between hardware and performance.

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# What Others Say

Every MPU power supply source says the same thing—"at 50°C, our supply will operate at 100% of rated output power." And many show, or describe, a derating curve like this on their data sheet:



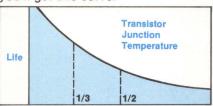
But shown or described, the curve doesn't really tell you anything about the unit. Because the devices inside that unit may be operating a whole lot hotter than the supplier, or you, thinks. Even at 50% efficiency, 50% of input power will be dissipated by the supply itself.

As industry observers have noted, many manufacturers aren't even able to meet their own derating curves. At least for extended periods. And their supplies may not be able to deliver 100% of multiple rated voltages and currents simultaneously at rated temperatures.

That 100% looks reassuring. But 100% of what? 5 V @ 6 A? 12 V @ 1 A twice? Some? All? None?

# **What Motorola Says**

Run it cooler and run it longer. All power transistors have a maximum TJ. Usually, it's 200°C for discrete, series-pass hermetics. And, if you plot device life vs T<sub>J</sub>, you'll get this curve:



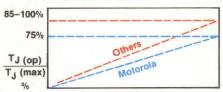
It's obvious. The cooler the device, the longer it lasts.

Where the supply designer operates on this curve is up to him.

But the secret of our success is conservative guardbanding—and we know no device should operate continuously at more than 75% of its maximum T<sub>J</sub> to meet customers' reliability expectations. A 200°C-rated TO-3 or TO-66 should be no hotter than 150°C. A 150°C-rated plastic unit should run at 110°C or lower.

And that's where we design them to operate in ICEMAN supplies.

At 100% of Pout (all outputs simultaneously) our power transistors will be at 75% of their maximum T<sub>J</sub>. No ifs, ands or buts.

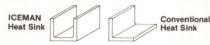


Transistor Pout

Units in other supplies will be at 85%, 95%, 100% . . . or even higher. And you can't do that to a power transistor and expect it to live long.

Our pedal's not to the metal.

# How We Keep 'Em Cool



ICEMAN supplies furnish 50% to 100% more square inches of heat sink area than comparables. Power transistor locations are spread over a much greater area, heat is dissipated faster, more efficiently, the supply runs cooler and more reliably.

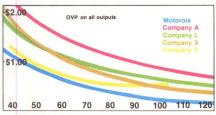
ICEMAN design furnishes power devices with more of what they're looking for—enough heat sink to take care of heat dissipation and keep T<sub>1</sub> out of catastrophe.

Vendor	Pout (Watts)	Sq. In. Per Watt	% of Motorola
Motorola	17.2	5.33	100
Company A	17.5	2.48	46.5
Motorola	36.8	3.13	100
Company A	46.0	1.65	52.7
Company B	39.0	2.14	68.3
Motorola	54.0	3.18	100
Company B	70.8	1.49	46.9
Company C	60.0	1.51	47.5

# **Better, Standard OVP**

Besides standard foldback current protection with the MC1723, ICEMAN supplies furnish the latest OVP technology using Motorola's MC3423 and the 2N6504 SCR. The '3423 senses overage, rapid-fires the SCR and shorts the supply output forcing it into current limiting or opening fuse or breaker. Turn-on propagation is just 0.5ms preventing SCR failure from incomplete firing. Threshold is resistor-adjustable.

# **ICEMAN's Bottom Line**



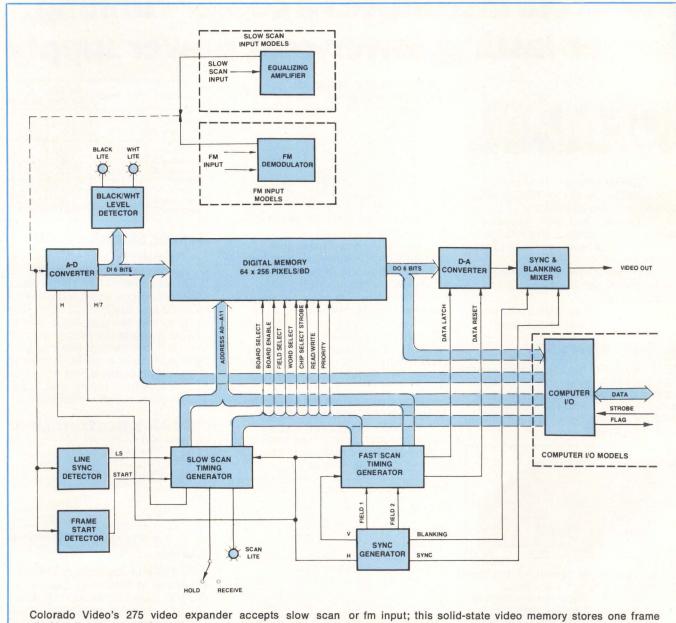
**Total Watts** 

Quality and technology are not expensive at Motorola. Our PLT800, 810, 820, 840/841, 2, 4, 6 and 15 A supplies are lower-priced-per-watt than any other nationally-known manufacturer based on latest published data.

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MOTOROLA INC.



Colorado Video's 275 video expander accepts slow scan or fm input; this solid-state video memory stores one frame of video information and builds up continuously refreshed image for display on standard TV monitor screen. Computer I/O option permits interconnection with TTL level minicomputers or digital processing devices

a conventional CCTV camera and reduces the bandwidth by a factor of several thousand for coupling to the telephone system. Still pictures are transmitted, with a typical frame time of 78 s/image for medium resolution of 256 x 512 picture elements. An optional 35-s mode with lower resolution is available.

The third generation system from Colorado Video, Inc, PO Box 928, Boulder, CO 80306 has a small remote control panel included with the compressor to allow the user to select from three video input signals to initiate or terminate a transmission at any time, and to pause in the middle of a transmission for split screen effects. Control of an optional frame freezing device is also incorporated.

Other features are a vertical cursor and a setup aid that provides a video waveform display superimposed over the TV image. The compressor also may be interconnected with audio sources for sequential voice/video transmission. Either simplex or duplex configurations are available.

At the receiving location, a model 275B video expander with solid-state picture memory reconverts signals to normal TV standards for viewing, distribution, or video tape recording. Capable of storing one frame of video information, the unit accepts data at

a slow rate, using them to build up a continuously refreshed image. The resulting display has no fadeout or image degradation.

The expander can be used as a computer output display device or as a slow scan video communications receiver. The output signal can be displayed on a TV monitor or used with other standard TV equipment. Output capability of units with the computer I/O option provides easy interfacing with TTL level minicomputers or other digital processing devices.

Circle 292 on Inquiry Card

# Language and Software Packages Add Further Communications Functions

The RPG II business data processing language for DS990 systems and a 3780 communications emulator for models FS990 and DS990 have been introduced by the Digital Systems Div of Texas Instruments, Inc, PO Box 1444, Houston, TX 77001. Based on a predetermined sequence that reads a record, processes the data, and outputs the results, 990 RPG II is suited to applications requiring file maintenance or report generation. A programmer uses a series of six basic spec formats to input the specific actions to be taken with the language's sequence of execution.

The language is similar to the IBM System/3 RPG II. A utility program is provided to copy System/3 or /32 source programs or files from diskette to DS990 disc files. Entry-level system for the language is the DS990 model 4 commercial system that includes a 990/10 minicomputer, 128k-byte memory, 10M-byte disc drive, the company's 911 VDT, and DX10 disc operating system software object license.

The package includes an RPG II screen-oriented text editor for program creation or modification. To aid program debugging, a trace feature prints each major item during program execution. A System/3 compatible sort/merge capability is optional, as is communication of RPG II files.

The one-pass compiler features run-time trace, right or lefthand sign handling, and ASCII or EBCDIC in-

ternal character set. It produces over 500 diagnostic messages; alphabetic summary listing of fields, labels, arrays, and tables; and listing of all specified indicators.

The 3780 emulator package provides the floppy disc-based FS990 and larger disc-based DS990 packaged system families with remote job entry communications to an IBM host, between other FS990 and DS990 systems, or between series 700 distributed processing systems. Systems equipped with a communication interface module, synchronous modem, and optional autocall unit can operate with the emulator as unattended central or satellite stations in distributed networks. Their operation is implemented by auto answer, auto disconnect, and auto call software capabilities, and any system 1/0 device or file may be selected for data transmission or reception.

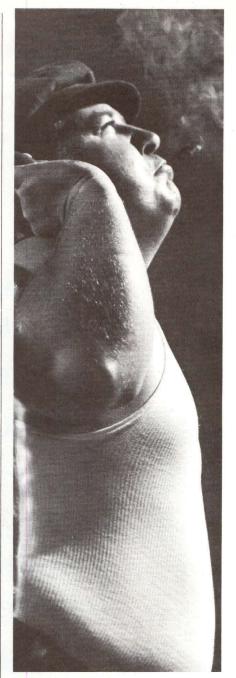
Circle 293 on Inquiry Card

# Powerful Networking Systems Family Performs Source Data Processing

The 220 DPS distributed processing series of networking systems that provide mainframe computing power for source data processing applications has been introduced by General Automation Inc, 1055 S East St, Anaheim, CA 92803. The systems are based on the 16-bit GA-16/220 LSI computers, with 128k bytes of 400ns access semiconductor memory and 10M bytes of online disc storage. They provide 2780 communications capability for access to remote host computer systems. Each cpu/cluster processor supports up to four online video display terminals operating in a multitasking environment up to 2000 ft (610 m) away.

The family provides easy forms generation, efficient data entry, mainframe cobol/fortran computing, comprehensive ISAM/PSAM file management, and remote batch communication capabilities for corporate online distributed processing. Software includes CDEs comprehensive data entry software containing supervisory functions for efficient use of system resources, as well as Easyform, a forms generation package for creating screen formats online without compilation.

Circle 294 on Inquiry Card



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HM-6518B 1K RAM	1024 x 1	18	140 ns	25 μW	74C930 Equivalent
HM-6518 1K RAM	1024 x 1	18	200 ns	250 μW	
HM-6518D 1K RAM	1024 x 1	18	250 ns	5 mW	<b>兴</b> 。李素是
HM-6501B 1K RAM	256 x 4	22	170 ns	25 μW	5101/2101 Pinout
HM-6501 1K RAM	256 x 4	22	240 ns	250 μW	
HM-6501D 1K RAM	256 x 4	22	300 ns	5 mW	
HM-6551B 1K RAM	256 x 4	22	170 ns	25 μW	74C920 Equivalent
HM-6551 1K RAM	256 x 4	22	240 ns	250 μW	
HM-6551D 1K RAM	256 x 4	22	300 ns	5 mW	
HM-6561B 1K RAM	256 x 4	18	170 ns	25 μW	2111 Pinout
HM-6561 1K RAM	256 x 4	18	240 ns	250 μW	
HM-6561D 1K RAM	256 x 4	18	300 ns	5 mW	
HM-6562B 1K RAM	256 x 4	16	170 ns	25 μW	2112 Pinout
HM-6562 1K RAM	256 x 4	16	240 ns	250 μW	
HM-6562D 1K RAM	256 x 4	16	300 ns	5 mW	

<sup>\*</sup>Access Time and Standby Power Specified at 5.0v, 25°C Maximum

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# Intelligent µProcessor System Automates **Electronic Mail**

Designed for the high document volume electronic mail user, the microprocessor-controlled high speed system 50 offers fully automated, unattended hardcopy communications with confirmed document delivery for up to 50 satellite terminals over standard voice grade telephone lines. Multiple transmission speeds are 35, 50, and 90 s. Components of the system consist of a programmable controller and satellite terminals.

The controller automatically dials up to 50 telephone numbers stored in memory, transmits documents to satellite units, and polls single satellite terminals or groups for documents on a periodic basis or at specific times. WATS or other telephone lines may be used during evening hours or when rates are lowest. Each controller or satellite can receive up to 500 documents in unattended operation and each has an automatic document feeder, which can be preloaded with up to 50 documents for unattended transmission.

Shorthand programming assigns a code to each satellite's telephone number, which is used for transmit or polling functions. Group codes can also be designated. A priority function, which interrupts any programmed task for immediate transmission, prevents the system from being locked out in continual use.

Developed by Rapifax Corp, 7 Kingsbridge Rd, Fairfield, NJ 07006, the system has an automatic dialing mode which causes the controller to

Key component of Rapifax's intelligent electronic mail system is programmable controller containing microprocessor and 32-char alphanumeric display, providing overall corporate mail network

redial a number twice at 5-min intervals when a busy signal is received; a job record review shows the entire day's send and poll tasks at any time. Added features are multiple resolutions and digital handshaking.

A 32-character alphanumeric display on the controller's panel exhibits keypad entries, instructions, and programming errors during programming mode; otherwise, a 24-h real-time clock appears. Two built-in security systems protect accessing of data and polling with special codes. Built-in battery backup prevents memory loss during a power failure.

Circle 295 on Inquiry Card

# **Discount Plan Slices Costs of Communications Network Charges**

A volume discount plan permitting lower hourly communications costs for the public packet network of Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 covers such key items as traffic charges for the amount of data sent; monthly charges for private dial and leased channel ports, including multiple connection, rotary, and private network features; and usage of local public dial-in ports. Effective February 1, monthly billings over \$5000 will have a reduced rate above that amount ranging from 20% on billings between \$5000 and \$9000, to 50% on those over \$18,000. Incremental cost of public dial-in service in major cities, for example, will be approximately \$1.90/h at the 20% level to \$1.20/h at the 50% level. Circle 296 on Inquiry Card

# Conference Focuses on Fiber-Optic Technology, Design, and Applications

The Fiber Optic Con Trade Show to be held at the Park Plaza Hotel, Boston, Mass on May 22 and 23 will combine technical sessions with exhibits from over 20 companies to provide an open forum for the exchange of ideas and applications relating to fiber optics. The sessions to be held concurrently on Monday afternoon, May 22 will deal with a basic tutorial covering various considerations and benefits of fiber-optic technology (Allen B. Kasiewicz, Rank Optics); individual hardware components of light sources, connectors, fiber types, detectors, and ancillary items; and communications applications involving telecommunications, CATV, and computer data transmission (Richard Cerny, Valtec).

On Tuesday morning, May 23, financial and economic matters will relate actual and projected growth, capital requirements, government policy considerations, and conversion to mass production (Phillip Leigh, First Boston); in addition, specific products on the market, and military applications (Bruce Metcalf, Mitre Corp) will be detailed. The final sessions on Tuesday afternoon will highlight systems design involving the selection of components to maximize overall system performance (Ken Fenton, ITT Cannon); products-continued from the morning briefs; and general applications in areas such as high stress or high voltage environments.

Further information concerning the show and exhibitors may be obtained from the sponsoring organization-Fiber Optic Communications and Information Society (FOCIS), 94 Charles St, Boston, MA 02114, tel:

617-367-4734.

# Contracts Are Assigned for Canadian Digital **Radio Route**

The first major contracts for large capacity digital radio in Canada, covering a 1100-mi (1770-km) system running from the Manitoba-Ontario border to Calgary, Alberta, have been awarded to Northern Telecom Canada Limited, 304 The East Mall, Islington, Ontario M9B 6E4, Canada. Alberta Government Telephones, Saskatchewan Telecommunications, and Manitoba Telephone Systems gave the contract following evaluation of proposed digital and microwave radio systems.

When completed and in service in late 1979, the system will link up with another in Ontario, thus stretching 2300 mi (3702 km) from Toronto to Calgary and Edmonton. This route in turn will be linked to the LD-4 high capacity coaxial cable digital system that runs between Toronto, Ottawa, and Montreal.

The company's DRS-8 system, developed and designed in Canada to meet Canadian operating telephone requirements, will use existing microwave route facilities that include buildings, towers, and antennas. There are 40 such locations over the route in the prairies. The system can handle voice or data traffic up to the equivalent of 1344 telephone conversations simultaneously per radio channel. There are 11 operating radio channels in the frequency band.

# One dynamic reason to buy Mostek's 4K static.

Delivery.

Delivery's fast and that's good news, but there are more dynamic reasons to buy the Mostek 4104 4K X 1 static RAM. For one, it offers the industry's best speed/power product. Using our own widelycopied Edge-Activated™ design concept, Mostek engineers developed the 4104 offering the best features of static and

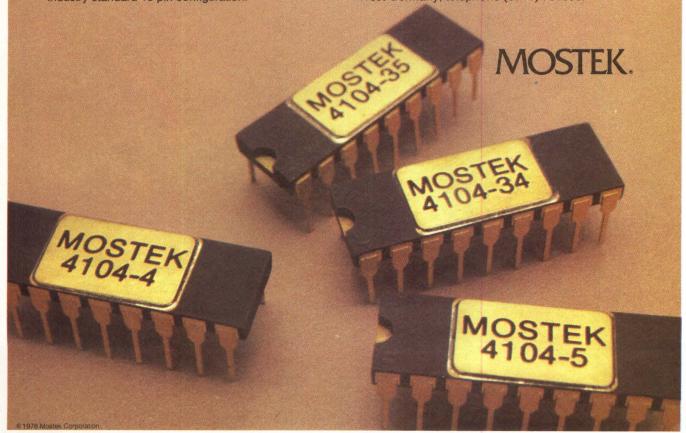
dynamic RAMs. Power is extremely low—just 150mW active and 28mW standby. It's directly compatible with TTL. It operates on a single  $\pm$  5 Volt power supply with a tolerance of  $\pm$  10%. And you can get it in the industry-standard 18-pin configuration.

	ACCESS TIME	CYCLE TIME	ACTIVE POWER (MAX)	STANDBY POWER [MAX]	BATTERY BACKUP POWER (-3X Series)
MK4104-4/-34	250ns	385ns			
MK4104-5/-35	300ns	460ns	150mW	28mW	10mW
MK4104-6	350ns	535ns			

The new 4104-3X series offers the capability of retaining data in a reduced power mode. When Vcc is lowered to 3V, maximum power dissipation is only 10mW. This allows complete data retention during battery operation.

There's a lot of dynamic reasons for Mostek's 4104 static RAM. To get the

complete story, call a Mostek distributor or sales representative now. Or contact Mostek at 1215 W. Crosby Road, Carrollton, Texas 75006; telephone (214) 242-0444. In Europe, contact Mostek GmbH, West Germany; telephone (0711) 701096.



TEKTRONIX
thinks your logic analyzer
should be as versatile
as you are



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The logic analyzer . . . it's become the essential measurement tool for digital designers like you. But just a logic analyzer isn't enough. Because your logic analyzer should be as versatile as you are. Our dictionary calls versatile "capable of turning with ease from one to another of various tasks." And versatile is exactly what you have to be in your day to day digital design work. Versatile in the tasks you perform, and versatile in your role as part of the design team.

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rk right Data it for you. /hile Look at logic in your language: choose binary, hex, octal, mapping, timing, GPIB, or ASCII



The faster your measurements, the better the resolution. Sample up to 100 MHz at 15 ns resolution



See all the Information you need to see with our large 4K formattable memory



Get the whole picture: verify logic on the bus synchronously; verify timing sequences asynchronously



Concentrate on other work while Automatic Data Comparison verifies operation — or identifies faults



For technical data, circle 22 on inquiry Card. For a demonstration, circle 23 on inquiry Card.

# **DIGITAL TECHNOLOGY REVIEW**

# **Low Cost Impact Printer Constructs Characters On An Infinite Matrix**

A low cost wire-matrix impact printer with the quality and automated features of ink jet and laser printing techniques, the Media 12/7 can perform utility printing at up to 216 char/s and produce executive quality type at up to 50 char/s on plain paper. Developed by R. C. Sanders Technology Systems, Inc, 5 Tinkham Ave, PO Box 324, Derry, NH 03038, the printer uses "Infinite Matrix Principle" technology to precisely construct character and graphic images by making up to four passes with a 7-pin printhead. Characters can range in size from 7 to 72 points. The smaller size will be useful in printing two pages of computer output on an 8.5 x 11" (21.6- x 27.9-cm)

Several proprietary processes are used to accomplish printing. Ink dot placement is positioned horizontally to a resolution of 0.001" (0.025 mm) and vertically to 0.0035" (0.0889 mm). Character or graphic images are constructed with a series of multiple horizontal passes by the 7-pin impact printhead. The head traverses each line at a constant speed and impacts the paper through a standard carbon ribbon.

Print quality and speed are determined by the number of passes per print line. In 1-pass operation the printer can produce up to 216 characters/s; on a 2-pass printing function, the head impacts each character on the line going left to right then right to left. This enhances the quality of the character while maintaining a speed of approximately 116 char/s. On a 4-pass operation with speeds in the 35 and 50 char/s range, quality



Four principal electronic boards in the MEDIA 12/7 typographic printer are Z80 processor card, parallel/serial I/O ROM storage card for internal storage of typefaces or signatures, motor/ printer driver board, and motor/print head logic board. Switched power supply in rear allows cool operation and provides high reliability

of characters is well suited for reproduction or for executive business applications.

Combination of a totally integrated design which embodies a minimum of moving parts and an advanced microprocessor controller provide a maximum of system flexibility, operating reliability, and serviceability. The printing mechanism is a 7-pin impact dot matrix head which is driven by a microprocessor based control system that regulates dot placement and paper movement. Horizontal movements of the printhead are interlaced with vertical paper motion to position dots as required.

Characters are constructed with a large number of 0.010" (0.254-mm) ink dots; therefore there is no limit on the shape or size of the image produced. Possibilities include Chinese, cursive handwriting, signatures, and graphic images in the form of line drawings or solid area designs. From 12 to 20 type faces can be stored internally in ROM. Graphic images such as signatures, logos, letterheads, and sketches may be digitized, and

then electronically stored.

Up to 56k bytes of storage are available for typefaces, graphic images, or forms storage. An average high quality 4-pass type face uses less than 4k, while a high speed 1-pass font will use less than 2k bytes, and a signature or logo may require 2k bytes. This provides the average user with storage capacity for three to six high quality faces, three or four draft faces, and six or more signatures. Optional cards provide additional internal storage or supply

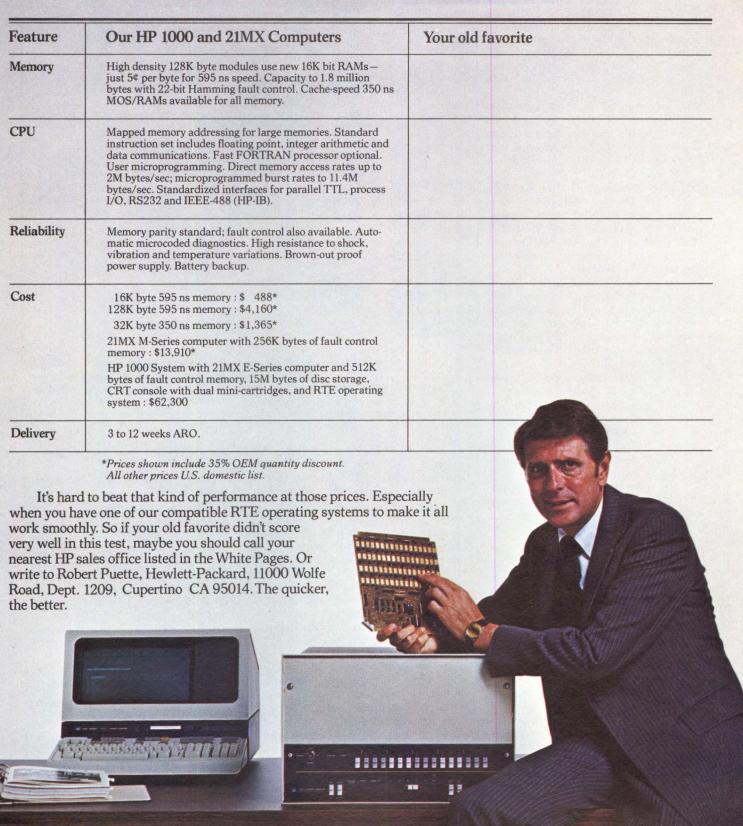
This is a high quality correspondence type face called Messenger-12, which was printed at 36 characters per sec ond. Messenger-12 is a 12 pitch mono spaced typeface requiring 4 passes of the print head for each line of type.

High quality text output can be produced with this 8 point Helevasan typeface which prints at 50 characters per second. Helevasan is a proportionally spaced, san serif typeface that is produced with 4 passes of the print head. This typeface is recommended for high quality printing of business documents, such as reports and proposals.

Daniel Hall 2/0/ Hana Dr. Pahala, Ha. 20/12

Designed to provide both high quality and utility grade printing, Sanders Technology's printer generates characters from footnote to headline size in any language set including Japanese or Chinese

# Aquick memory test.





a floppy disc interface for virtually unlimited storage.

Users have the option of varying print quality and specifying type-face, type size, line length, leading value, margins, and justification without making mechanical adjustments or interrupting printing operation. Different type faces and sizes can be intermixed on the same print line.

Electronics are contained on four boards: processor board holding the Z80 microprocessor and DMA chip; parallel/serial I/O ROM storage card for internal storage of type-faces, motor/printer driver board, and motor/printhead logic board. Standard TTL compatible parallel and RS-232-C compatible serial in-

terfaces are provided.

Functional features include a replaceable printhead, internal selftest program, and dual-line input buffers. Manual operator functions have been minimized by providing pushbutton operation. The operator simply places a sheet of paper in the slot provided and pushes "start print." The printer automatically locates the edge of the paper and feeds the sheet to the first print line. Lighted message indicators on the control panel show printer status and alert the operator to conditions requiring attention.

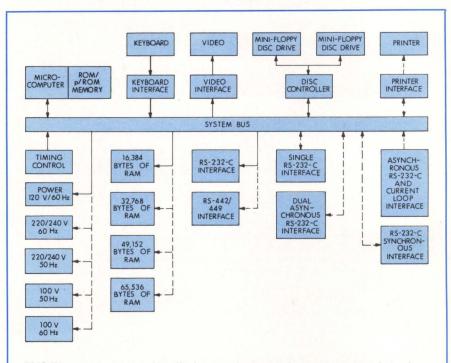
The basic unit is priced at approximately \$4000 in single quantity; OEM prices are as low as \$1350.

Circle 360 on Inquiry Card

# User-Programmable Display Terminals Adapt to Special Needs

ZMS-50, -70, and -90 user-programmable terminals are intended to fill customer's needs for intelligent, software-oriented, and expandable systems at low cost. All three share 8080 microprocessor bus architecture that offers powerful, flexible use of firmware, software programming, and peripheral interfaces. In the units, Zentec Corp, 2400 Walsh Ave, Santa Clara, CA 95051 has concentrated intelligence and video display in a compact package capable of filling various requirements.

A useful feature, built into firmware, is a list-driven structure that provides video flexibility by allowing data that are distributed throughout memory to be displayed contiguously



ZMS-70 user-programmable display terminal contains an Intel 8080A-1 microprocessor with up to 64k bytes of memory along with a 15" video display, keyboard, telecommunications interface, and 143k bytes of online disc storage

on the screen. This is accomplished by using a 16-bit pointer to the control list that contains the address of the beginning of each line or segment, and information about it. Hardware displays the line on the screen from anywhere in memory with any length, fills out any remainder with blanks, then picks up the next entry in the list to display the next line. This provides for compacted memory, because blanks are not stored, and requires less complicated programming, simplifying adaptation to individual system designs.

For communications flexibility, the units provide programmable synchronous or asynchronous communications interfacing without hardware changes. A programmed chip controls the output port under program control. By sending one byte of information through the port as the system powers up, output is specified as being asynchronous or not, internal clock rate is determined, and odd, even, or no parity is defined.

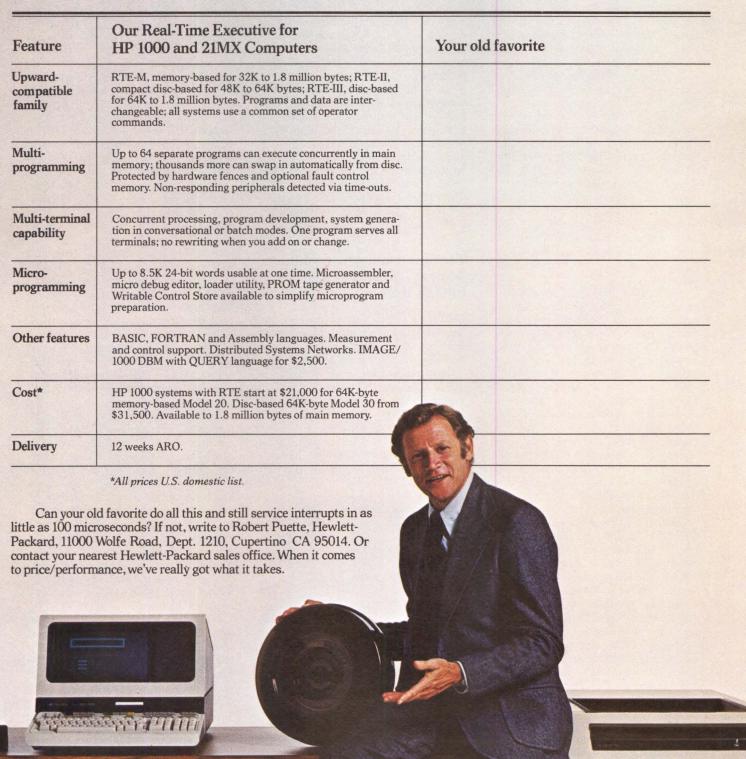
Another system design feature is the screen's "25th line" which provides operator messages and system status information. With this feature the terminal can bypass the display screen, and communicate directly with the host computer or display messages from the host to the terminal operator.

Aimed at applications that require a substantial amount of intelligence but no peripheral capability beyond a printer, the ZMS-50 comes with up to 8k bytes of Rom and/or p/Rom capacity and 4k bytes of RAM; a 16k-byte version is available. The basic 4k bytes of RAM are used as refresh memory for up to two pages of video displays; where two pages are not necessary, the second page of RAM can be used for storage and execution



A self-contained microcomputer featuring dual mini-floppy diskettes and a powerful operating system, Zentec's ZMS-70 uses a list-driven architecture which allows data to be spread throughout memory, yet displayed contiguously

# Performance: has your operating system got what it takes?





of user-supplied programs that can be downloaded from the host. The 16k version significantly extends this capability.

An asynchronous RS-232-C interface and a firmware package enable the terminal to communicate data to/ from a remote system. A comprehensive text editor performs a number of editing functions and a form generator mode allows generation and display of any kind of programmed form.

A totally software-oriented system, the ZMS-70's operating system takes full advantage of the list-driven structure to provide the video flexibility needed for heavy text editing and data base manipulation applications. This unit houses a microcomputer system in the desktop enclosure along with 65k bytes of memory, 15" (38cm) diagonal video screen, extensive keyboard, telecommunications interface, and a pair of built-in minidiskettes.

The system uses 2k of ROM and/or p/ROM for a disc bootstrap routine and some basic self-test diagnostics; this is expandable to 12k bytes maximum. On power-up the bootstrap automatically loads operating programs into RAM from the disc, putting the system under software control. The basic system contains 16k bytes of RAM, which is expandable to 60k bytes. RAM provides storage for programs and data, including that to be displayed on the video display screen.

Internally housed, the online disc system consists of two mini flexible disc drives interfaced with a built-in DMA controller such that the microprocessor may operate concurrently with disc operations. Each diskette holds 71.5k bytes of formatted data, allowing 143k bytes of online storage.

Supplementing this system, an extensive set of software routines for application program development and system operation includes a generalpurpose disc-based executive file manager, and complete assembly language development package.

A programmable RS-232-C serial interface can operate in asynchronous, synchronous, or isochronous modes. In synchronous or isochronous modes, speeds of up to 19.2k bits/s are determined by an external clock. In asynchronous mode, speed can be set at 110, 300, 1200, 2400, 4800, or 9600 bits/s. As an option the unit may be equipped for hardcopy printing using a second asynchronous interface. Alternatively, a complete printer subsystem that includes a parallel interface and corresponding printer is available.

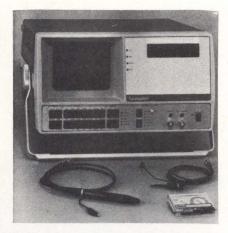
The most flexible of the family, the ZMS-90 can be, within reasonable parameters, any kind of terminal the customer wants. Offering all video display handling, keyboard, and function capability of the -70, the -90 can be configured as a software-oriented machine through connection to external floppy disc drives, or as a hardware-oriented terminal with RAM/ ROM/p/ROM expansion capability to 65k bytes. It is outfitted with additional card slots for custom boards and interfaces and can support a larger number of peripherals than other members of the family.

Circle 361 on Inquiry Card

### **Test Instrument Combines** Analog/Digital Functions In One Unit

DTO-1, a digital testing oscilloscope, handles digital circuitry like a logic analyzer and analog circuitry like an oscilloscope, and automates go/no-go testing procedures with comparison tester functions. The combination of functions in one instrument allows production testing to be performed at the completed unit level.

Developed by Biomation Corp, a div of Gould Inc, 4600 Old Ironside Dr, Santa Clara, CA 95050, the unit



Designed for production test and troubleshooting of any digital system or product, Biomation's DTO-1 digital testing oscilloscope is shown with standard equipment that includes a single-point test probe with built-in LED go/no-go indicator and advance button, single-point trigger probe, and one mini-data cartridge

incorporates a single signal input probe, trigger probe, CRT display, and oscilloscope-type controls, with microprocessor intelligence. It is ideal for solving digital problems as well as associated analog circuit design problems, and its performance is high enough to handle all but the fastest digital circuits. Digital signals are sampled at rates including 100 MHz and its analog scope capability has usable bandwidth to 25 MHz. The instrument can reduce the time required to test a product for proper operation, and allows faults to be traced to the component level.

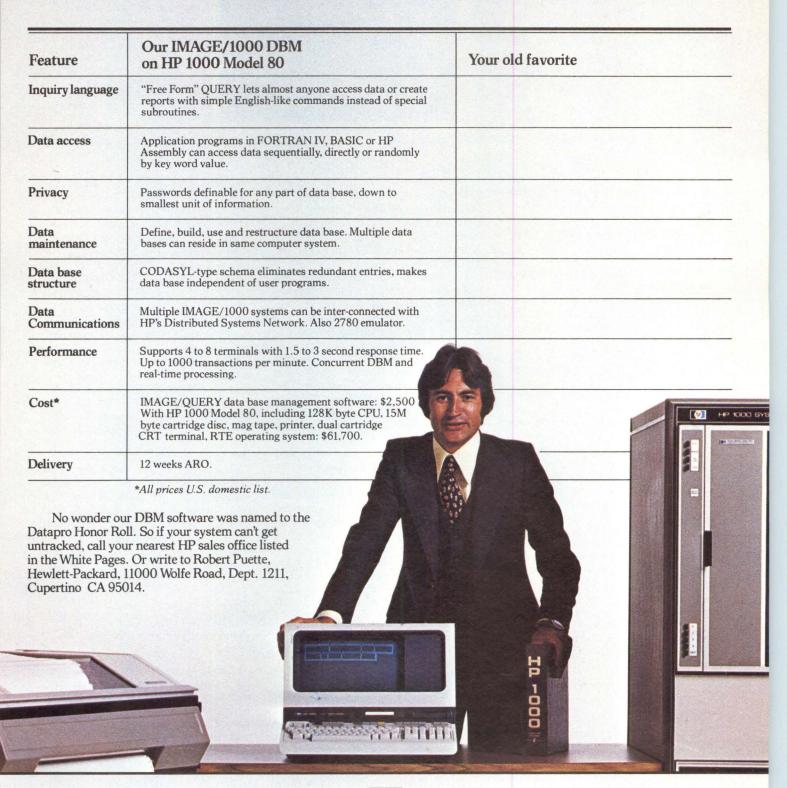
Basically a single-channel logic recorder that can compare digital signals with previously recorded good signals, the microprocessor-based instrument stores operating software as firmware within 14k bytes of ROM. Although 4k bytes of RAM are standard, the unit expands to 16k bytes to handle high volume tape duplication requirements. RAM is used to record digital signals and transcribe test records and sequences. The device reads and writes to standard 3M mini-cartridges. No special software syntax is required for programming because the unit stores reference logic signals in the integral magnetic tape unit the same way as an oscilloscope is normally used.

Essentially, the instrument's input circuit is a variable speed A-D converter. Input signals are converted to a digital data stream that is stored in memory. Instrument settings are also stored in RAM. CRT display information, obtained via a direct memory access (DMA) channel from RAM, generates trace lines, analog waveform display data, and alphanumeric characters. Permanent test programs can be established by transferring the logic trace data and associated control setting data from RAM to tape storage. When test records are read from tape back into RAM, the microprocessor uses the control settings to set up the instrument; displayed information is again obtained through the DMA channel.

Operational features of the instrument have been kept as close as possible to oscilloscope nomenclatureanalyzer sampling rates are automatically derived from a second/division setting and pretriggering is expressed in CRT divisions. Pushbuttons are used for selection of ranges and other variables, with button increment or decrement value displayed on the CRT screen. Panel controls are divided into four groups: sweep, data, trigger, and mode.

Trigger sources may be internal, automatic, or external. Internal triggers are generated from the input

# Data Base Management: is your small computer on the right track?





signal. External triggers are acquired with a trigger probe or combinational trigger accessory. Automatic trigger refers to pseudotrigger events generated by the instrument. Both data and trigger probes have an impedance of  $10~M\Omega$ , 15~pF, and 10:1 attenuation. The data probe carries controls needed for automatic testing.

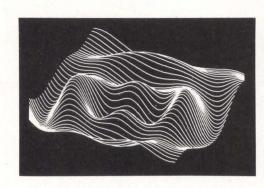
Operation in all six modes is supervised by the microprocessor. Four modes are for actual test use and two are for programming. In trim mode the probe acquires a calibration waveform from a test point on the instrument's front panel. Autoscope is the automated comparison testing mode. The CRT display shows as many as eight logic traces, including the known good system and system under test traces being compared and up to six previous system under test traces.

In either mixed or scope mode, up to eight logic traces or up to three traces plus analog waveforms can be displayed on the CRT. In mixed mode, the two bottom traces may be hold-overs from a previous mode. In most cases, they will be a known good/system under test trace pair with system under test disagreements underlined.

In program mode, up to 100 new traces can be stored, displayed, and recorded onto a single magnetic tape cartridge. Before a trace is recorded on tape, it can be seen on the display; and then transferred from RAM to magnetic tape. Up to eight newly acquired logic traces or traces recalled from magnetic tape can be displayed in this mode. In transcribe mode, the microprocessor transfers test records between RAM and the tape cartridge unit. Records can be written back onto the same tape or onto different tapes. Newly recorded and previously recorded test records can be mixed for assembly on tapes for specific applications. Tapes may also be duplicated in this manner. Circle 362 on Inquiry Card

### Software/Firmware Package Overcomes 3-D Plotting Constraints

3-D PLOT is a software/firmware package that supplies 3-dimensional plotting and editing capabilities to users of the Tektronix 4051 graphics computing system. Available from Second



Containing 4000 vectors, plot represents an array of 8000 elements, which require only 16k bytes of storage when compacted using Second Source's 3-D PLOT software/firmware package. Supplying enhancements to the Tektronix 4051 that overcome speed and space constraints, package allows this plot to be drawn in less than 1 minute

Source Industries, a div of I Corp, 735 Addison St, Berkeley, CA 94710, the package contains a 2902 graphics ROM and 2901 conics ROM which overcome speed and space contraints when dealing with 3-D plots on the 4051 system.

Problems encountered in using 3-D plots include difficulties in constructing and storing the plots, eliminating the hidden lines, and repeating the plots in different scales and with different viewpoints to achieve the most meaningful perspective. The software/ firmware enhancements enable the 4051 to overcome the problem. Although the ROM packs have different graphics orientations, either may be used to simplify 3-D plotting. The conics pack is primarily a function and image generator but will speed plotting; the graphics pack is an image manipulator that both packs data into less memory space and plots faster. It is more effective when the primary application is 3-D plotting.

Firmware in both ROMS uses a dark vector approach to solve the problem of drawing speed. This approach allows moves and draws in one matrix. Moves are distinguished from draws by making the sign of the X-

coordinate negative. To solve the problem of workspace memory size, the graphics ROM pack provides the ability to compact graphics data by a factor of four. Compacted data are then treated as named images that can be selectively edited, printed, negated, deleted, concatenated, sorted, or moved with the commands provided.

The surface plot illustrated, which is fairly typical in density and size, will not fit in the 4051's memory without use of the graphics pack, but requires only 16k bytes when compacted. Drawing this plot with the pack, using compacted data, takes less than 1 min. With uncompacted data and the conics pack, it takes less than 2.5 min. View point generation (hidden line selection) took 45 min. Since, frequently, the data base for plots will already exist, this time frame makes it practical to do several trial plots with varying viewpoints and scales. Overall, the dark vector approach can reduce time required for 3-D plots by an order of magnitude or more.

Circle 363 on Inquiry Card

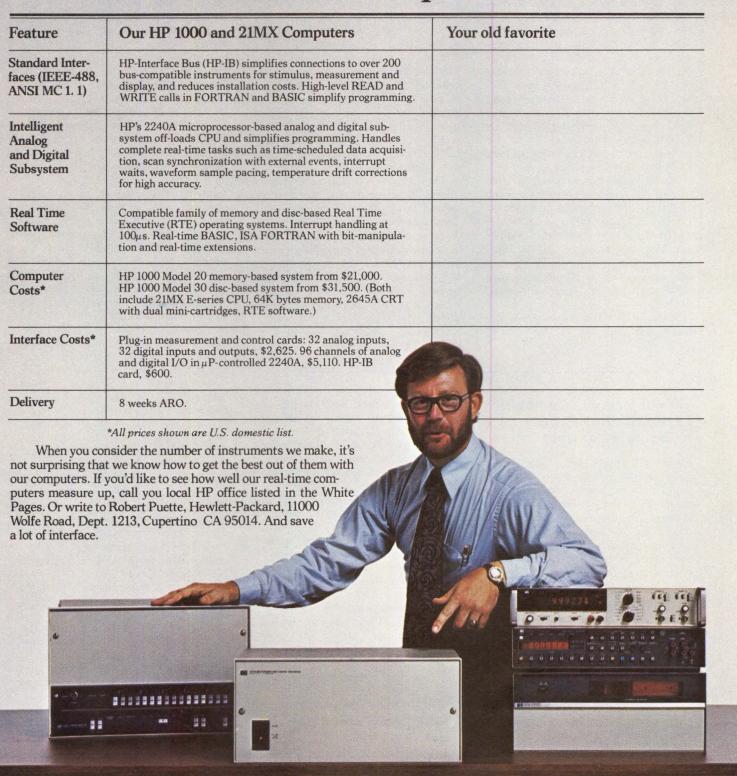
### Single Medium-Scale Computer System Replaces Five Separate Models

A single system Level 64 replaces five Level 64 models now offered by Honeywell Information Systems, 200 Smith St, Waltham, MA 02154. Users may enter at any point and expand their configurations in four dimensions—CPU performance, memory capacity, peripheral mix, and com-

munications processing. The concept claims to offer large system benefits, including distributed processing, at medium system prices, while on-site growth minimizes disruption of service caused by hardware swapouts.

Level 64 includes five levels of instruction execution speed, 64k to 768k bytes of 4k-bit mos memory, and a broad selection of peripherals for configuring a system to multiprogram up to 10 batch and/or communications jobs using either con-

# Instrumentation Interfacing: how does your real-time computer measure up?





ventional or data base file organizations. Supporting the system are various peripheral devices, systems and applications software, and a remote maintenance system.

Central processor supports 64k to 768k bytes of mos main storage capacity with a read time of 1  $\mu$ s to 740 ns and a write time of 1  $\mu$ s to 940 ns. Control memory has 175-to 145-ns access time. The processor provides from two to 10 independent 1/0 channels, with capability for 1250M-byte/s transfer on each. Aggregate 1/0 transfer rate is from 4.0M to 4.25M bytes/s.

Mass storage is provided on from two to 24 disc drives with capacity of 29M, 70M, or 100M bytes/drive. Printers include 600- or 800-line/min drum printers, 600- or 800-line/min belt printers, and 1200- or 1600-line/min belt printers. The system also supports up to 16 magnetic tape units and up to eight unit-record devices.

As many as three data communication controllers support up to 14 lines each. Connections may be synchronous, asynchronous, or binary synchronous. Rates range from 100 to 19,200 baud/line.

The Level 64 ccos operating system gives users the ability to process up to 10 jobs concurrently while utilizing the system input reader. These jobs may be any combination of batch, communications, or transactional, including up to four output writers. An enter active text editing and operations facility allows terminal users to create, update, and maintain files containing source programs, JCL, user data, and job results.

The remote maintenance system allows field engineers to monitor, control, and diagnose system installations and to take corrective action from a remote support center. Built-in security features provide for supervision and control of the process by the user, by allowing the diagnostic process to occur only after the customer manually activates a maintenance interface.

Circle 364 on Inquiry Card

# a price previously reserved for minicomputers." Priced starting at \$150,000, the system consumes only 1400 W (CPU memory and all controllers) of power, can run on ordinary 110-V power, and can operate in normal office environments. Mainframe competitors include Honeywell Level 62, Univac 90/30, and IBM System/3, 370/115, and 370/125.

Extending the top end of the family, the DECsystem 2060 provides essentially the same performance as the 2050, but because of doubled memory capacity—4M bytes—can handle up to 80 concurrent jobs. It uses an advanced version of the KL central processor used in other family members and enhances growth within the family through increases in memory capacity, online disc storage, and asynchronous communications capacity.

With its 36-bit word length, the general-purpose computer offers concurrent interactive timesharing, multistream batch, and transaction-oriented processing, yet houses processor, memory, console control, and integral peripheral device controllers in a single 5-ft (1.5-m) high cabinet. The system consists of four major subsystems: KS10 central processor with 512-word virtual address cache memory, console unit, Unibus™ adapters, and peripheral controllers and devices. Built using lower power Schottky TTL, the microprogrammed KS10 processor features eight blocks of 16 fast general-purpose registers, (96-bits/word) writable 2k-word RAM microstore, and basic microinstruction cycle time of 300 ns. Parity checking occurs in microstore, on the data paths, and on the backplane bus.

Memory system consists of a single extended hex control module that connects to the backplane bus and controls up to eight storage modules, each containing 64k words of Mos memory. With capacity for up to 512k 36-bit words, the memory has 1.050-µs cycle time and provides single-bit error correction and double-bit error detection.

All console and diagnostic functions are performed by the console unit. Housed on a single extended hex module, it contains a microprocessor, and provides two asynchronous interfaces—one for console operation and one for remote diagnostics. The diagnostic link and the microprocessor allow diagnosis of the system via a remote link.

### Virtual Memory Computer System Shares Access to 2M-Bytes of Data

Prime 350 gives users high speed, large system capabilities normally found only on larger systems. Introduced by Prime Computer, Inc, 40 Walnut St, Wellesley Hills, MA 02181, the system runs programs as large as 768k bytes, and takes advantage of features in the PRIMOS IV operating system to give all users simultaneous shared access to 2M bytes of virtual memory. These characteristics adapt the system to use in medium-scale applications in computational timesharing and interactive data processing.

Based on proven architecture of its medium- and large-scale predecessors, the 350, combined with the company's virtual memory BASIC/VM compiler, offers performance features and program capacities unavailable on most comparable systems in computational applications. For interactive data processing it uses COBOL and MIDAS data management software. It also supports RPG II and 2780, HASP, UT200, and ICL 7020 emulators.

The 350 offers a 50% performance improvement over the model 300

running fortran applications, by using 2k bytes of high speed cache memory and standard floating-point instructions. These features, along with business instructions that it emulates, give it a 200% performance increase in COBOL programs.

Compatible with PRIMOS IV, the system also runs shared, reentrant procedures that execute in a virtual memory that is segmented, paged, and protected by multiple rings. It is compatible with the company's full line of systems, and can be field upgraded to model 400 or 500 simply by exchanging central processor circuit boards. User software requires no modification.

Circle 365 on Inquiry Card

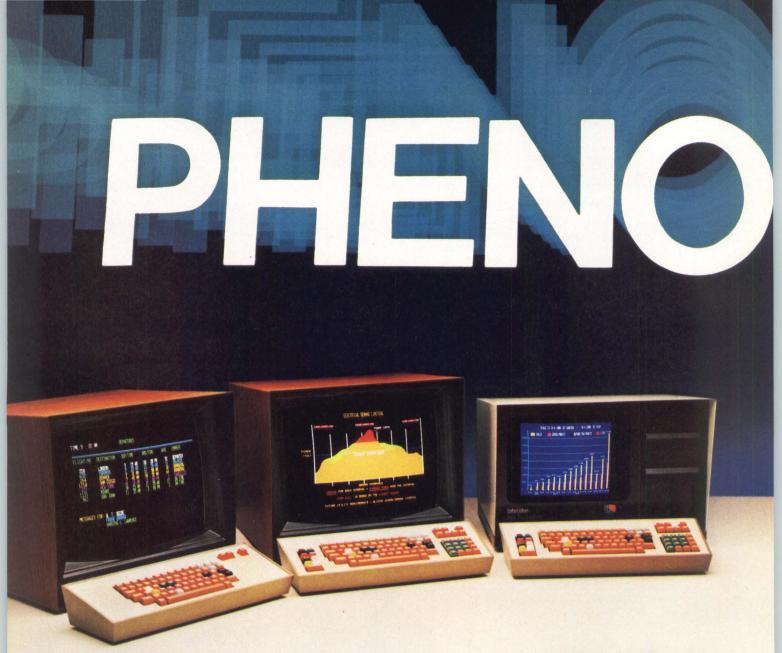
### Mainframe Computers Claim Power, Size, and Price Records

Claiming to establish several records in mainframe computer systems, the DECsystem 2020, according to John Leng, vice-president of the Large Computer Group, Digital Equipment Corp, Marlborough, MA 01752, "provides full mainframe functionality at

## Processor growth: can your small computer make the upgrade?







Intecolor 8001 Color Data Terminal - \$995\*

Color Graphics 8001G - \$1,925\*

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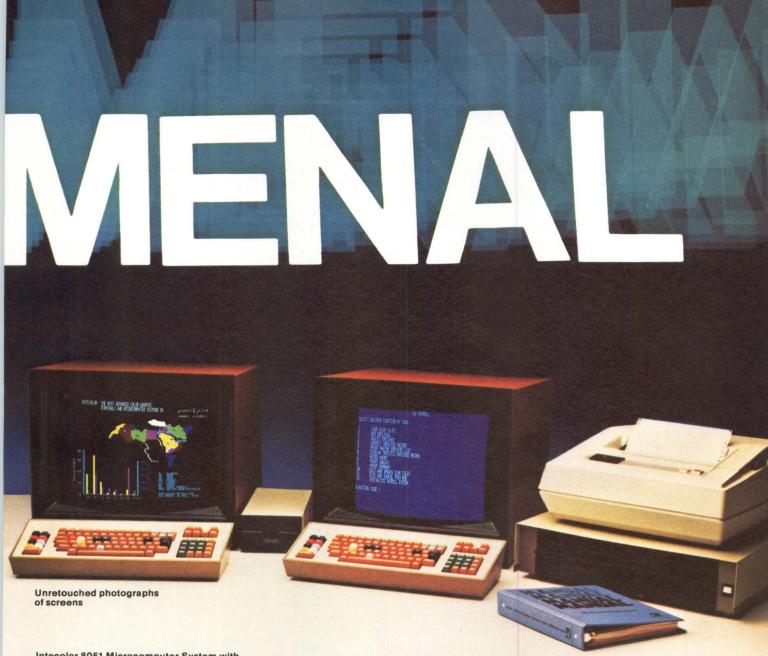
shortly after development of the microprocessor opened up the industry to a whole new range of possibilities. One of those possibilities, low-cost color data terminals, was the main thrust of our endeavor. With a combination of sound research and development and aggressive marketing, we were able to introduce an intelligent data terminal with the extra advantages of color at a price any company could afford.

And because of even more advanced technology, coupled with growing sales, we've also been able to bring sophisticated color graphics down to the price levels of black and white.

Having pioneered the development of low-cost color graphics for the process control industry, new emphasis is being placed on the use of color graphics for business applications. Instead of drab black and white alpha-numerics,

\*Prices for the 8001 and 8001G are based on orders of one evaluation unit, cash-with-order, guaranteed 30-day delivery or your money back. Prices for the 8032, 8051 and 8070 are 100 unit prices, net 20 days.

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Intecolor 8051 Microcomputer System with mini-disk drive — \$3,150\* (Shown with special ARABIC/FARSI configuration. Optionally available at extra cost.)

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Appropriate manuals are provided with all equipment. Others are optionally available.

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Today, ISC is the world's largest supplier of color terminals and not only markets 8-color data entry terminals, but also compact desk top computers with a color graphic display and a wide range of lowpriced peripherals for full-fledged small business systems. We also have a variety of options available

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Peripheral devices interface to the system through two Unibus adapters (UBAS): one is for discs only, the second is used for tape, printer, and communication lines. Provision is made for eight asynchronous communication lines, expandable to 32 provisions for two synchronous communication lines. Also available are two high performance disc systems to provide virtual memory file storage, a reliable magnetic tape system, interactive CRT terminal, and hardcopy equipment.

Key to the system's easy operation, the TOPS-20 operating system supports FORTRAN IV, CODASYL-standard DBMS, COBOL, APL, ALGOL, IQL, CPL, and BASIC-PLUS-2 languages. The virtual memory operating system offers a multiuser, multifunction environment to support concurrent interactive online and multistream batch

computing capabilities. In addition to providing 1M bytes of user virtual address space, the software provides communications capability for both asynchronous and synchronous lines.

In a minimum configuration, a 2020 consists of KS10 central processor, 0.5M-byte mos memory, RM03 disc system with 67M-byte capacity, TM03/TU45 tape subsystem with data transfer rate of 120k bytes/s, eight asynchronous communications lines, and a DECwriter II console teleprinter. Price is \$150,000. A fully expanded system may contain 512k words of main memory, eight 176Mor 67M-byte disc systems, four tape subsystems, 32 asynchronous communication lines and two synchronous lines, and one line printer and one card reader.

Circle 366 on Inquiry Card

## Signal Processing System Uses Oscilloscope For Real-Time Analysis

Sequential real-time analysis of vibration, seismic, sonar, communications, speech, and other data can now be performed without the need for expensive graphics consoles. Using conventional oscilloscopes, the low-cost turnkey SPS-21 FORTRAN signal processing system provides what appears to the eyes as "time-lapse" or slow motion photography when analyzing data in a wide range of applications, instead of the long lists of numerical data which must be interpreted or reprocessed to provide usable results.

Developed by Signal Processing Systems, Inc, 223 Crescent St, Waltham, MA 02154, the system features direct I/O capability with self-contained high speed A-D and D-A converters as components of the signal processor. This permits real-time processing and analysis of signals independent of the host computer. The D-A output allows real-time observation and verification via a conventional oscilloscope. The approach produces flicker-free displays of high quality, eliminating the need for expensive graphics consoles.

Components of the processor include an input/output processor (IOP), an arithmetic processor (AP), a 16-bit wide data bus operating at 5-MHz, an interface for the PDP-11 host computer, a 16k x 16-bit bulk memory, a 12-bit high speed A-D converter, and a 10-bit high speed D-A converter. Expansion of memory to 32k x 16 bits, additional I/O channels, and a rack mountable oscilloscope are available as options.

The instrument comes complete with a comprehensive subroutine library for executing signal processing, arithmetic, data manipulation, display, and 1/0 operations. Price is \$29,500.

Circle 367 on Inquiry Card

### Vector Memory Display Offers Dynamic Functions For CAD Systems

Vector memory display, an erasable video display, features a 21" (53-cm) video monitor refreshed from solid-state memory. Offered as an option for all computer-based design, drafting, and mapping systems from Cal-

ma, 527 Lakeside Dr, Sunnyvale, CA 94086, the vmp provides 10 times the brightness of typical storage tubes, and offers dynamic features that include selective erase, continuous pan and zoom, and instantaneous context switching.

Because the monitor, in effect, has its own built-in memory, the work-load on the graphics systems' CPU is reduced, and greater image detail is possible. VMD incorporates up to four 64-word, 16-bit memory boards, developed jointly by engineers at Calma and Intel. Vector memory is capable of holding enough vectors to represent an entire schematic, PC board layout, or mask for an IC.

The option allows users of minicomputer-based interactive graphics systems to engage in dynamic activities. Selective erase permits screen graphics to be deleted or modified and the result instantaneously reflected on the screen. Continuous pan and zoom cause the image to move smoothly across the screen or to zoom in on (or out from) an image, allowing the designer to inspect the fine structure. They can occur continuously and independently as data are input; a feature which enables errorfree routing of long metal runs through intricate geometries. Instantaneous context switching allows layers to be added or deleted in the view. It also means that "menus" can be added and deleted instantly, under control of the designer.

The user loads vectors into memory and, whenever he wants to change the picture, rewrites raster memory in real-time from this data. Data in the raster memory are refreshed in 25 ms and then continually refreshed onto the monitor. The image is continually refreshing itself at a 40 frames/s rate. System memory is associative, which means all vectors and polygons in effect carry "tags" for easy identification. The display also offers multiple viewport capability. Users can work in any single view-including pan, zoom, and erase capabilities-without affecting other views. Six different views can be displayed concurrently. There is no demand on the CPU during these activities.

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# DX00 SERIES SMART TERMINALS



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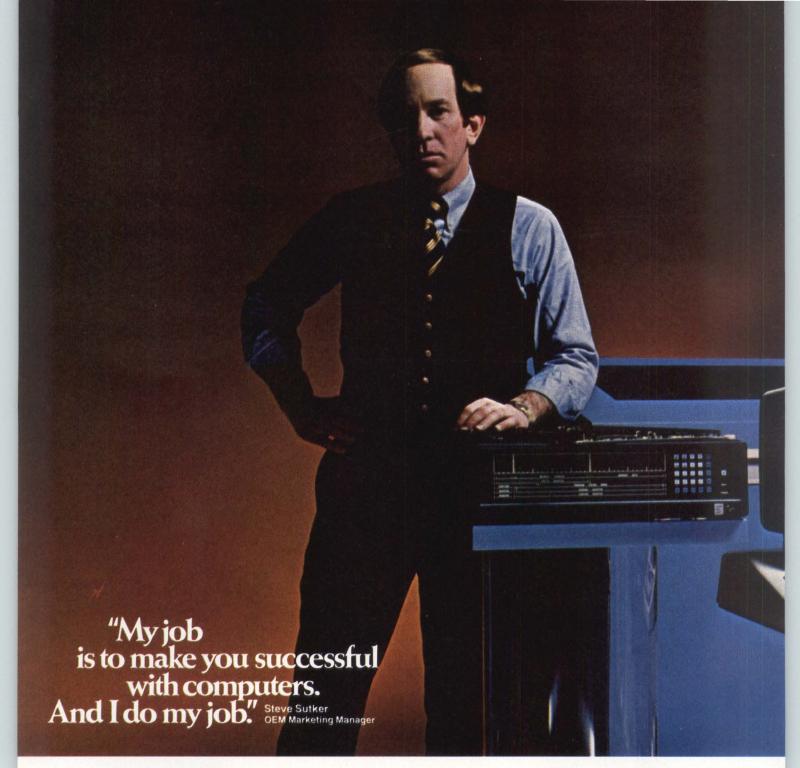
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CIRCLE 198 ON INQUIRY CARD



I'll make you successful with computers. Not because I like you. Not because I'm such a great guy. But, because I know that the more successful you are, the more computers you'll buy. And the more successful I'll be

Sure it's selfish. But, when my own career is at stake, you can be certain I'll give you better products, better delivery, better prices, and better terms and conditions.

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Interdata 16-bit computers are built better for one very good reason. Our people have been on your side of the desk. They know the kind of quality it takes to make an OEM successful.

So we build more carefully and test more thoroughly than our competition. And you get computers that run as soon as they're installed and keep on running.

Choose the Interdata 5/16 with microbus architecture to communicate with terminals and peripherals via low-cost interface chips. The 6/16, king of the box computers. Or the 8/16E system, with up to 256KB memory and peripherals. And for even more power, take a look at our 32-bit line.

### Better delivery. 60 days ARO.

To be successful in this business, first you have to have a computer to

be successful with. We deliver 16-bit Interdata computers in 60 days or less. Guaranteed.

Ask our competition if they can guarantee 60-day delivery.

#### Better terms and conditions.

We also write terms and conditions to make you successful. Like a 38% discount on orders of 100 or more units. Mix and match quantity discounts. Standard multi-year agreements. Spare parts discounts that save you money after the sale. And multiple ordering locations with no penalty for using them.

Ask your sales representative for a copy of our new super OEM agreement.



### A special OEM hotline.

Agreements are fine. But the true test of a computer manufacturer is service. And that's where we really shine. We back up our local support people with a 24-hour OEM hotline. If you have a problem, one call gets us. Days. Nights. Weekends. Holidays. We're there whenever you need us.

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**Data Systems** 

CIRCLE 30 ON INQUIRY CARD

## DIGITAL CONTROL AND AUTOMATION SYSTEMS

## Multiple-Microcomputer Building Control System Reduces Both Electrical and Employee Costs

A building management system installed in the Denton, Tex Federal Center originally was planned to reduce building security costs and monitor pumping and ventilation equipment. Then the concept was altered to include energy management and smoke/fire detection. Now, the system—based on five distributed microcomputers—controls equipment, provides smoke and fire detection, and prevents intrusion by unauthorized personnel—while reducing electrical demand by 38% and electrical consumption by 49%.

Electrical power charges are based on demand—the maximum level of service provided—and consumption—the power actually used. By monitoring and controlling both functions, the system reduced demand costs by an average of \$240/mo and consumption costs by \$1230/mo. In addition, maintenance and security personnel costs in the 55,000-ft² building were reduced \$2000/mo. The total annual savings in a 12-mo period was \$41,640—about twice the cost of system, materials, and federal personnel time for installation.

The control system was developed by Radix II Inc of Oxon Hills, Md using five SC/MP-based microcomputer cards and 10 memory cards from the Microcomputer Systems Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Each of five ISP-8C/100 microcomputer boards contains an 8-bit SC/MP microprocessor with its onchip functions such as oscillator, serial input/output circuits, and address and data bus buffers. These 4.5" (11.4-cm) square boards also contain control buffers, 256 words of random-access memory, and 512 words of programmable read-only memory. On-board memory is augmented by 4k-word by 8-bit ISP-8C/002 RAM cards and p/ROM cards of varied capacities. 1/0 interface cards sense up to 64 digital and 32 analog inputs and up to 128 digital outputs.

One battery backed-up microcomputer performs all supervisory functions for the system; two others monitor both electrical demand and electrical consumption, sense building temperatures, operate heating, ventilation and air conditioning (HVAC) equipment, detect smoke and fire, and provide security; a fourth controls a local status printer; and the fifth serves as a telephone line communications controller to link the system with a central facility in Dallas.

Since electrical equipment draws more current when starting than it does during operation, a high level demand function must be maintained in the event that several pieces of equipment start simultaneously. This demand factor typically constitutes from 20 to 30% of the total electric bill.

Time of day (including day and year) as well as day/night, weekend, and holiday schedules are maintained by the supervisory microcomputer. On a normal day the system starts activating equipment about two hours before employees arrive. To reduce demand level, a microcomputer monitors the rotating wheel on each watt/hour meter to detect the demand on that circuit. If the demand peak approaches the next rate level, the microcomputer inhibits the start of other equipment until the load reaches a steady-state condition. Because steady-state is attained in a few seconds, the delay is virtually unnoticed. The system recognizes weekends and federal holidays and suspends equipment start-up on those days.

During a normal working day, the system implements an energy conservation program based on operating within predetermined maximum levels of power consumption for optimum equipment use. Some equipment is shut down during the time intervals when operation is unnecessary. Other equipment, such as an air conditioner, is slowly cycled while the heat content of the area is calculated.

Instead of merely controlling room temperature, the microcomputers measure increases in area heat content and predict the optimum time to start air conditioners. Conversely, when the heat content drops below acceptable levels the system turns on heaters. This contributes to energy savings because it takes less power to maintain a room within certain temperature limits than it does to cool a hot room or heat a cold one. Although other unnecessary equipment is shut down through the periods when the building is unoccupied, the cooling and heating system continues to operate. As an example of resultant energy savings, during a 3-mo period on which a comparison could be made, the average electrical demand was down from 281 kW/mo to 137 kW/mo and the average electrical consumption was reduced from 165,440 kWh/mo to 83,360 kWh/mo.

System microcomputers monitor 37 alarm conditions ranging from sump water level to smoke and fire detectors and control 24 pieces of equipment ranging from chillers and exhaust fans to area lighting. Because frequent intense thunderstorm activity makes power failure fairly commonplace, the system senses power

Intel's new in-7000 static memory system with Word/Byte Control delivers speed, convenience and design flexibility. It's the easiest way to get our high-density 2114 4K static RAMs into your system.

The in-7000 is a complete static memory with interface and control logic contained on a single 10.8" x 8.175" printed circuit card. The system requires only a +5V power supply, is TTL compatible, and needs no refresh. You can choose from two versions, differing only in speed: the 7000, with a

read and write cycle time of 250 ns; and the 7001 (350 ns).

The basic in-7000 card is available in four 16K configurations: 16K x 12, 16, 20 or 24 bits. Two chassis models are also available. The in-Minichassis can house six in-7000 circuit

cards, and the in-Unichassis has a 32-card capacity.

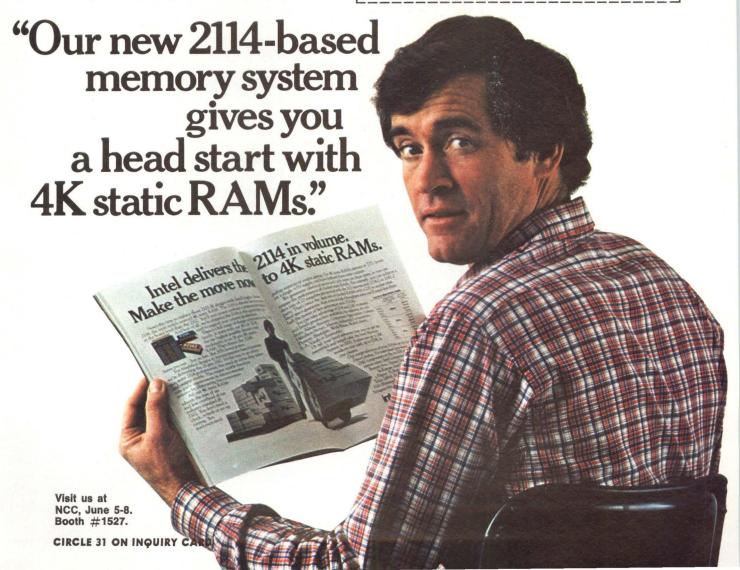
A unique feature called Word/Byte Control gives you the design flexibility to standardize on the in-7000 for all your systems applications. Word/Byte Control allows the Byte Control inputs to be used either

for reconfiguration or byte data control. In the Word mode, the Byte Control inputs select either or both halves of a word, effectively reconfiguring a 16K x 24 card to 32K x 12; a 16K x 16 card to 32K x 8; and so on. In the Byte mode, any combination of three bytes in a 24-bit word may be selected by the Byte Control inputs.

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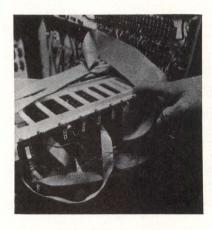


Fig 1 Five SC/MP-based microcomputer cards in Denton, Tex Federal Center control HVAC equipment, monitor building security, and detect smoke and fire. System has reduced electrical consumption by 49%

loss and activates a standby generator. The microcomputers initiate special power-loss control routines and reestablish proper equipment operation when utility power is restored and stable.

Monitoring of equipment is maintained constantly to assure proper operation. Control memory contains 128 error correction codes. If a piece of equipment does not function correctly after 10 signals from the computer, a malfunction message is transmitted.

Detection of smoke or fire activates warning and safety procedures in the building. In addition, fire alarm messages are transmitted to a Dallas central location.

Building security control is a major function of this system. Personnel authorized to enter the building are assigned unique identification numbers which they type into the keyboard at each controlled-access door when they want to pass through. Microcomputer memory contains the personnel identification numbers, correlated with preprogrammed data on the specific hours each person is authorized to enter an area either during or after normal working hours.

The system verifies that the individual is authorized to enter, automatically unlocks the door, and prints a hardcopy record of the person entering or leaving the area. To prevent intrusion or tampering, the system sounds an alarm if three consecutive errors in the ID number are entered.



Fig 2 Building personnel must enter unique identification numbers into keyboard before entering. Microcomputer checks memory to determine if person is authorized to enter building at that time of day (or day of week) and unlocks door if person is entitled to enter

One microcomputer acts as telephone line communications controller and accepts status reports from all of the other microcomputers. This microcomputer also detects message transmission errors and retransmits the corrected messages. To test the communication link integrity, both Dallas and Denton systems call one another every 30 min.

All incoming and outgoing messages, including equipment malfunctions, are routinely printed and recorded by the printers. Time of day is added to each message for chronological record. Printers have double-font capability. For routine messages, such as equipment status, a standard size type is used. Letters four times larger signify warning messages such as fire or intrusion.

### Microcomputer Kits Featured In Amusement Park Control Systems

An in-house engineering staff has used computer kits to build computerized control systems for the "nation's oldest and third-largest theme amusement park." Engineers of the Construction and Maintenance Div at Knott's Berry Farm in Buena Park, Calif purchased three MITS/Altair<sup>TM</sup> 8800 microcomputer kits from an Altair computer center as the basis of the systems which they designed to help control park operations.

Each of the three computers, manufactured by Pertec Computer Corp's Microsystems Div, 20630 Nordhoff St, Chatsworth, CA 91311, is dedicated to a specific application: work order scheduling, lighting, and air conditioning. System hardware consists of an Ann Arbor CRT terminal, 100-char/s Okidata line printer, and 300k-byte floppy disc drive for each system. The work order scheduling system includes 40k bytes of memory while the lighting system has 16k and the air conditioning system has 20k. Any CRT terminal or printer can be switched to either of the other applications if necessary.

The work order expediting system schedules the division's workload based on due dates and priorities that have been assigned to the various jobs. If more than one shop is involved in a particular job, the computer coordinates the different shops. A printed listing, showing all jobs in priority order, is furnished periodically to various managers.

In the lighting control system, the computer provides centralized control to turn various groups of lights on and off at prespecified times. Except a few parking lots and other peripheral areas, all of the Farm's lighting is controlled. Currently lighting is divided into 11 control sections but the system can control up to 100 separate lighting areas. Therefore, at a future date the 11 sections will be divided into smaller groupings.

A fairly constant lighting schedule is maintained normally, but different on/off times can be set up for special events that require lighting at unscheduled

# Now available: ruggedized terminals that cost less and do more.





Immediately available. The Interstate Electronics Alpha/Graphic Model PD 3000 plasma display computer terminal. It's qualified for reliable operation in the military environmental spectrum: mobile or fixed ground, shipboard, and airborne. And the price won't strain the most rigid budget.

Costing thousands of dollars less than competitive units, the PD 3000 provides more capabilities, such as alphanumeric and graphics display—standard. Or both 5 x 7 and 7 x 9 dot matrices for character font.

Among many functions, it generates and displays all standard alphanumeric characters and complete graphics, and decodes and implements the complete ASCII character and control set. It also has a full ASCII-compatible solid-state keyboard.

This small (13" x 14" x 12", 53 lb.) unit features a flicker-free,

distortion-free flat display.
The -RFI-EMI enclosure to meet
MIL-E-5400R, MIL-STD-901C, and
MIL-STD-461 is standard.

PD 3000 offers high-altitude capability (20,000 ft. operating; 70,000 ft. nonoperating), high-resolution graphics, with more than 4000 characters displayed, and an operating temperature range of -32°C to 55°C.

Proven software includes a



real-time/high-level macroinstruction set that provides subroutines for display control, alphanumeric display, incremental and vector graphics. Custom software and engineering are also available.

Some 200 field personnel, located worldwide, provide a major support effort.

We're delivering.

Write for the complete PD 3000 data package to Interstate Electronics Corporation, Don Poulos, Computer Products, 1001 E. Ball Rd., P.O. Box 3117, Anaheim, CA 92803.

INTERSTATE ELECTRONICS CORPORATION

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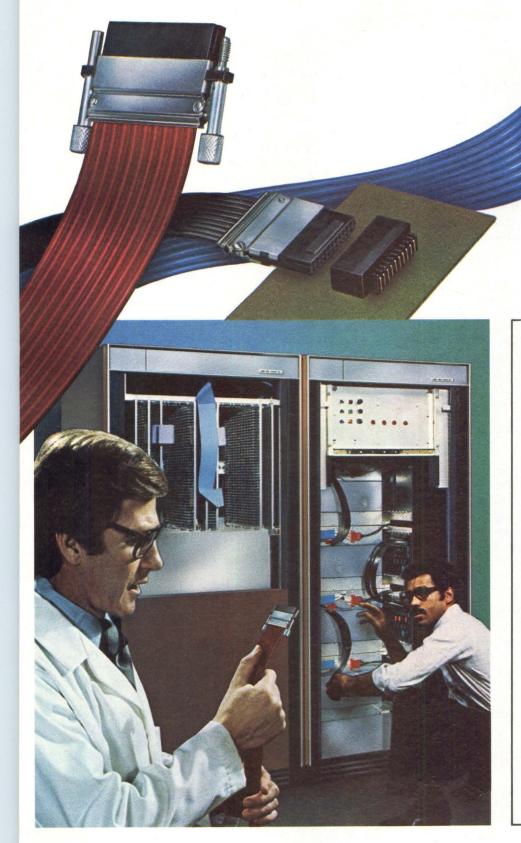


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times. After the special event is over, the "non-constant" plan is purged from the memory and the system reverts to its normal schedule.

The third computerized system is designed to conserve energy and minimize the Farm's electric utility bills through control of about 50 air conditioning units. It compares actual kilowatts being used by the entire Farm at any given moment with an amount that has been designated as a standard for that particular time of day. Whenever the actual kilowatt use exceeds the standard, various air conditioning units are ordered to cycle off and on at short intervals—usually every 10 minutes.

All air conditioners are grouped into three different priorities. The control system automatically searches its memory, finds the air conditioners in the lowest priority group which are running at the time the signal to begin cycling is received, and selectively cycles those units. If cycling a major portion of the lowest priority units does not return power to standard, the system cycles the next priority group, and continues this procedure until actual kilowatts return to the standard amount.

An additional system feature guards against excessive peak power usage which could adversely affect the Farm's utility rate structure. If power usage reaches a maximum kilowatt figure, the system continues to cycle as before, but increases off times by 20%.

Design and implementation of the lighting and air conditioning control systems required installation of about \$75,000 worth of acoustically-coupled transmission and receiving equipment. Total cost of computer hardware was \$21,800 and custom programming performed by a software contractor cost \$10,500.

As many as 100 individually controlled air conditioners can be handled, allowing expansion beyond the 50 in the original installation. In addition, inventory management will be added in the near future to keep track of parts required in the various shops.

Circle 280 on Inquiry Card

### Hierarchical CNC System Features Real-Time Monitoring of Machine Tools

Computer numerical control being implemented by Rohr Industries in Chula Vista, Calif is based on a 3-tier hierarchy of minicomputers. Real-time function monitoring—an innovation for the machine tool industry—is a major portion of this system despite a 1977 Delphi-type survey conducted by the Society of Manufacturing Engineers and the Univ of Michigan which projects implementation of this type CNC system for 1985.

All three present tiers of the hierarchy feature minicomputers made by Computer Automation, Inc, 18651 Von Karman, Irvine, CA 92664. The first level consists of an LSI 3/05 Naked Milli™ that continuously monitors 80 machine functions; second level is an LSI 2/20 that serves as a machine control unit (MCU), and the third is another LSI 2/20 that acts as supervisory computer. At a future date a fourth hierarchical level will be handled by IBM 360 and 370 computers. At present, however, these mainframes store a library of thousands of parts programs and are used in program development.

Parts programs are transferred as needed from mainframe mass memory to the supervisory computer via paper tape. An automatic switching network being implemented will permit the supervisory computer to call for and receive programs over a data line.

The CNC supervisor, located on the factory floor, is configured with 32k words of core memory, a 10M-byte disc storage device for active parts programs, a floppy disc for offline program storage, a line printer for hard-

copy output, a teleprinter as backup for the printer, and a video display terminal. In operation, the floppy disc controls the sequence of programs to the MCU.

Each supervisory minicomputer has eight ports. Of these, six will be used for MCU interface, one for test purposes, and one for backup. Thus one CNC supervisor configuration will be required for every six machine tools.

The MCU, which is housed physically within the machine tool, contains 8k words of core memory. Input from the CNC supervisor is via a data line interface.

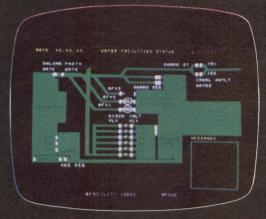
Real-time monitoring of machine functions is maintained by the dedicated "millicomputer," which is also housed inside the tool. Operation of electronic and mechanical components monitored by this computer is displayed on a CRT terminal.

Rohr Industries personnel design, engineer, build, and maintain their machine tools, which might cost as much as \$900,000 if purchased. Mechanical and electronic features enable titanium and aluminum to be machined to tolerances as close as 0.001" (0.0254 mm).

The first two of a proposed 16 new bridge-type milling machines were placed in operation last summer. Others will be phased in over a period of time. In addition, 36 older machines will be upgraded with the control system. The program, which has immediate application to aircraft projects such as the Air Force F-14, Navy P-3, and Boeing 747, is claimed to offer at least 25% improvement in productivity. Circle 281 on Inquiry Card

# What You Need Is What You Get.

Ramtek's RM9000 modular graphics and imagery system gives you expandability, economy and flexibility.



Process Control: Water facilities plant.



Imaging: Viking I Orbiter.

#### Select The Performance You Need.

The RM9000's total modularity lets you select the exact performance you need to fill your particular application. You pay only for the performance you need. Nothing more. And that's like money in the bank.

### Add On As You Have To.

As your needs change and grow, the RM9000's capability will grow right along with them. A comprehensive list of options such as expansion from black and white to grey scale or color—even a complete range of interactive peripherals and additional independent channels.

#### Microprocessor-Controlled Raster Scan.

The RM9000 is the first raster scan graphics and imagery system to be totally microprocessor

controlled. That means you can implement a higher-order user language to minimize programming costs without a sacrifice in system throughput.

### Functional. Reliable. Maintainable.

High reliability is the direct result of intensive testing of components and systems prior to shipment. Solid state components and printed circuit construction are used exclusively. Result? No special preventive maintenance measures are required. In fact, the RM9000 can be preprogrammed with self-diagnostic capability.

#### You Need To Know More.

To fully appreciate the RM9000's capability, you need more details. Call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale, CA 94086. (408) 735-8400.



### To a PDP-11, our EMU™ is the World's Fastest Disk.

### Seeing is believing.

When you connect our EMU (Extended Memory Unit) to your PDP-11/04 through 70 don't be surprised to see a look of astonishment from your CPU.

To a PDP-11 the EMU looks just like a DEC fixed head disk. However, instead of waiting 8.5 to 17 milliseconds average access time for a disk, the EMU requires only 2.1 microseconds to set up control registers. That's anywhere from 4,000 to 8,000 times faster than fixed head disks.

More throughput. The EMU transfers information at a 1 microsecond selectable data transfer rate. That's 16 times faster than the RF/RS-11 and 4 times faster than the RJS-04 disk.

**EMU adds life.** An EMU can add years of productive life to an overloaded PDP-11 system. Budgetwise it makes sense.

Environmentally safe. Because the EMU is unaffected by shock, vibration, temperature or high particulate atmospheres it is particularly suited to shipboard installation and other "disk hazardous" environments.

Big, bigger, biggest. You can start with 512 KB and build to 2.8 MB in a 10½" x 19" rackmount chassis. With an additional 5¼" chassis you can have 4.0 MB.

Advantageous applications. Here are some of the many advantages to replacing your PDP-11 disk with an EMU.

Time sharing:
Decreased wait states,
faster response times.

Program development: Faster assembly, linking and compilation.

Data communications: More communications lines per processor.

Data Base
Management: Faster information access.

Data Acquisition: Higher sampling frequencies.

Process Control: Higher control loop bandwidths. Data Analysis: Ability to handle 1024 by 1024 floating point word data arrays at near processor speeds with BASIC, FORTRAN, and other

high-level languages.

Relax. The EMU is totally hardware and software compatible with every PDP-11/04 through 70. Battery backup provides nonvolatility and a one year warranty reflects our confidence in our extensive component burn in and system testing procedures.

Now showing. We are holding a series of free EMU seminars throughout the U.S. to explain specific applications in detail.

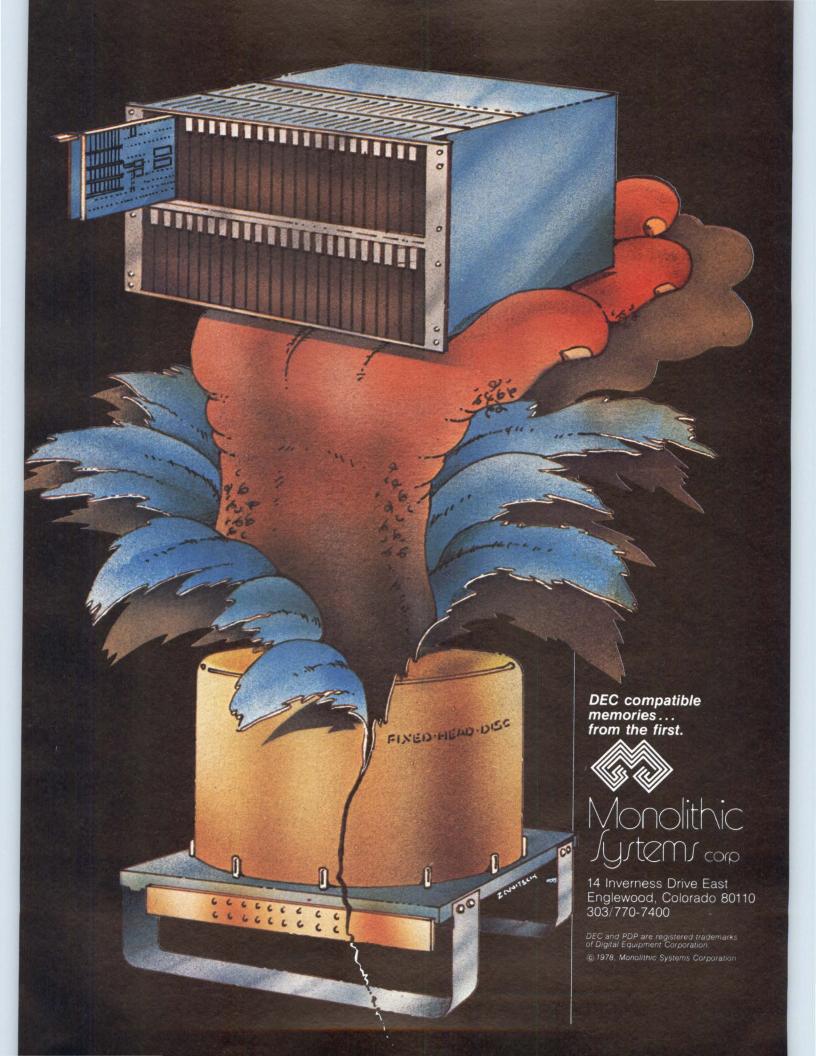
If you would like to attend, circle the appropriate reader service number on "the coupon you can't fill out."

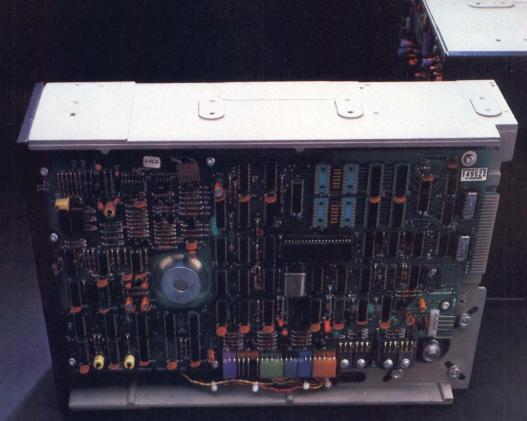
Invite me to see the World's Fastest Disk! CIRCLE 19

Send me your new brochure.
CIRCLE 35

The EMU can be seen at:

Mini/Micro '78 Booth 719-723 Philadelphia April 18-19 and NCC Show Booth 1803-1809 Anaheim June 5-8





# Disk drives or subsystems? Remex announces two low-cost controller/formatter/drives.

The RFS 1100 and micro-based 1200 are part of the Remex family of disk drive subsystems, complete with built-in controller/formatters.

Now time and money you might otherwise spend developing your own controller/formatter can be concentrated on application software and total systems — where you can make the greatest contribution.

The savings are sizable, even if the subsystems are not—many man-months of development time and dollars. And that's not considering getting your system to market months sooner.

Whether your system is based on a popular minicomputer or microprocessor, we've got the application notes and assistance capability to help make interfacing a breeze.

Both units are media compatible with the IBM 3740, 3540 and System 32. In fact, they'll read sectors of any length, provided standard IBM header information is used.

And both feature the Remex high quality disk drive hardware, with head geometry identical to IBM, assuring precise media interchangeability now and later on.

The RFS 1100 is available in 3 models, including 2 with buffers that permit greater CPU efficiency in your system.

The RFS 1200 has its own integral microprocessor for maximizing system speed and minimizing software overhead. It's available in a master/slave configuration for reducing costs in multiple drive applications.

Only Remex offers so much for so little in such neat, integrated packages — with nearly 20 years of electro-mechanical experience and nationwide field service to back it up.

Call or write today for complete information on complete subsystems. Ex-Cell-O Corporation, Remex Division, 1733 East Alton St., P.O. Box C19533, Irvine, CA 92713.

Phone: (714) 557-6860. TWX: (910) 595-1715.

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REMEX DIVISION

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CIRCLE 201 ON INQUIRY CARD

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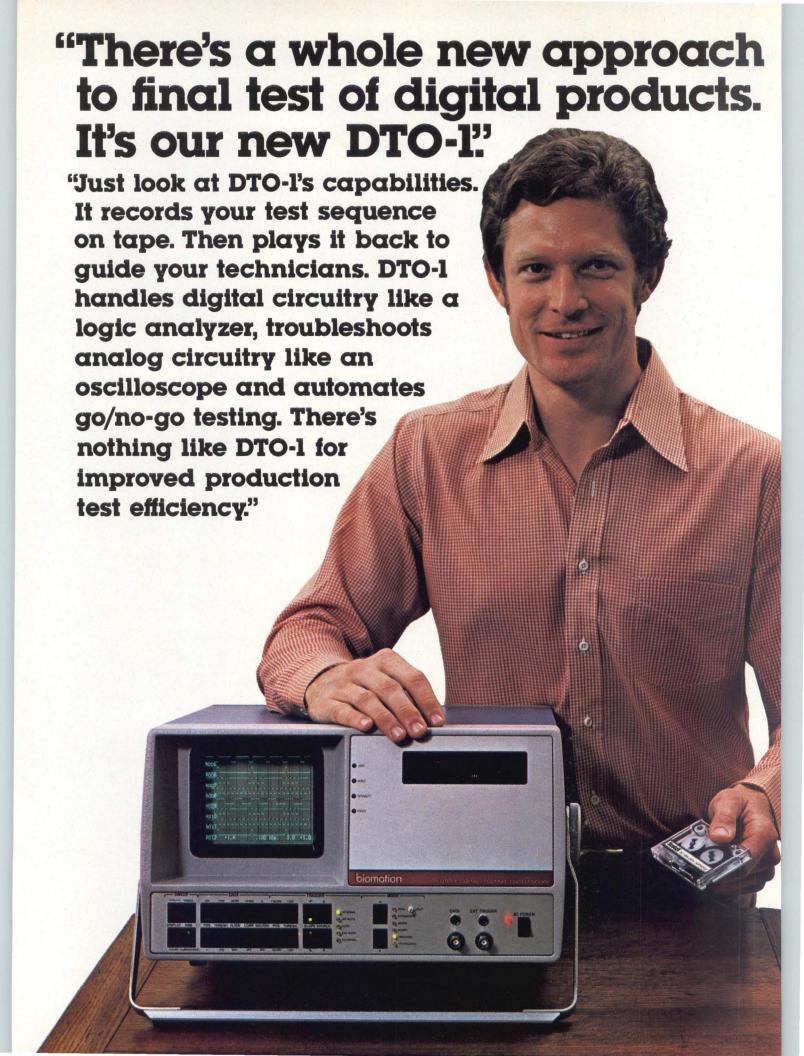
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CIRCLE 36 ON INQUIRY CARD



## "Here are five ways Biomation can cut your test costs."

**Like having a design engineer test every product.** DTO-1 is the fast, easy way

for engineering to develop thorough test procedures



for new digital products. Step through your test sequence once and DTO-1 records reference logic traces for the entire program on a tape cartridge. So you can quickly produce test programs for each design change and every

new product. And DTO-1 is virtually selfprogramming, with no software development needed.

### Finally, automated comparison testing.

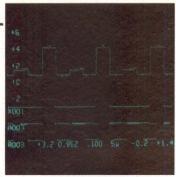
The time-consuming, error-prone monotony of total product checkout is ended by DTO-1. Technicians just follow the established test sequence and DTO-1's powerful microprocessor auto-



matically compares logic traces with the recorded reference traces. Pass-Fail lights on DTO-1's probe guide technicians through complete testing of product functions. You get improved quality control. It's quick and it's foolproof.

# Speeds and simplifies trouble-shooting, too.

When a fault is detected, the probe's red light alerts the technician to check DTO-1's builtin scope. There he has the diagnostic capability to pinpoint both digital and analog



faults. Like a logic analyzer, DTO-1 displays time domain logic traces, comparing the test trace with the reference trace and highlighting any disagreement. Analog waveforms can be simultaneously displayed with logic traces, on the same time base.

That makes it easy for the troubleshooter to determine if the malfunction is digital or analog. Result: Quick, positive fault isolation.



### Technicians love DTO-1.

Finding, training and keeping test technicians is a growing, costly problem. DTO-1 is the answer. It practically trains technicians for you, using your recorded test programs to control the test

sequence. It automatically aligns itself to the frequency of the system under test, is self-calibrating and includes built-in diagnostics. DTO-1 frees your technicians from the repetitious routine of product test, and lets them concentrate on finding and fixing malfunctions.

### DTO-1: A cost effective solution.

At \$8950\* you can build your entire test and service capability around DTO-1. It's a cost effective instrument at the end of your assembly line. And you can afford to put one in the development lab



for before and after testing of design changes. Supply your repair depots and field service force with DTO-ls. Then by sending the latest tape you can provide them with test routines for new products and design changes.

The coupon below will get you a demonstration, or a reprint of an eight-page article on the DTO. See why we say that there's nothing like DTO-1 for improving production test efficiency.

\*U.S. price only.

Gould Inc., Biomation Division 4600 Old Ironsides Dr., Santa Clara, CA 95050 (408) 988-6800							
I'm in a hu	arry. Call me at/						
extto arrange a demonstration.							
Send me	the reprint and complete product data.						
Name	Title						
Company							
	Mail Stop						
City	State Zip						



NOTE: See DTO-1 in action at booths 2318-22 at Electro '78.



### DIGITAL CONTROL AND AUTOMATION SYSTEMS

DC&AS BRIEFS

### Programmable Industrial Control Unit Serves as Learning Aid

A 2-board industrial control system that combines a highly functional, prewired programmable logic controller with an ancillary input/output simulator that serves as a system development tool and demonstration unit is now available from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. It is based on the company's MC14500B industrial control unit, a single-bit microprocessor, and can serve first as a learning tool to acquaint designers with the power and potential of a 1-bit microprocessor and, thereafter, as a dedicated functional control system. As a functional system, the I/O simulator is replaced by the actual I/O devices associated with the working system.

The system has 15 inputs and 16 outputs and incorporates a RAM capable of holding 128 program instructions. Users can examine or change the contents of any memory location and can single-step or run programs. Alternatively, a programmed p/ROM may be installed in an available socket to run the program. Built-in LEDs display the state of the program within the system for monitoring or troubleshooting. Circle 286 on Inquiry Card

### Machine Tool CNC Provided in Cost-Effective, Dedicated Packages

Machine manufacturers now are able to implement computerized numerical control to fit exact requirements at about half the usual cost of adapting general-purpose control systems according to Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 and Omnicron, Inc, 1111 E Ten Mile Rd, Madison Heights, MI 48071. Those two companies have signed an agreement to provide a microcomputer-based CNC package that uses parametric programming based on interactive machine/programmer communication in plain English.

Parameters of interest are displayed on a CRT. The operator responds by entering required dimensional data through a keyboard. When all the questions are answered, the system is programmed and ready to start production.

Other typical systems provide additional capabilities such as standard editing that permits changing and improving programs right at the machine, and manual entry of multiblock programs at the control panel. Circle 287 on Inquiry Card

# READ THESE TEN CHAPTERS. AVOID CHAPTER 11.

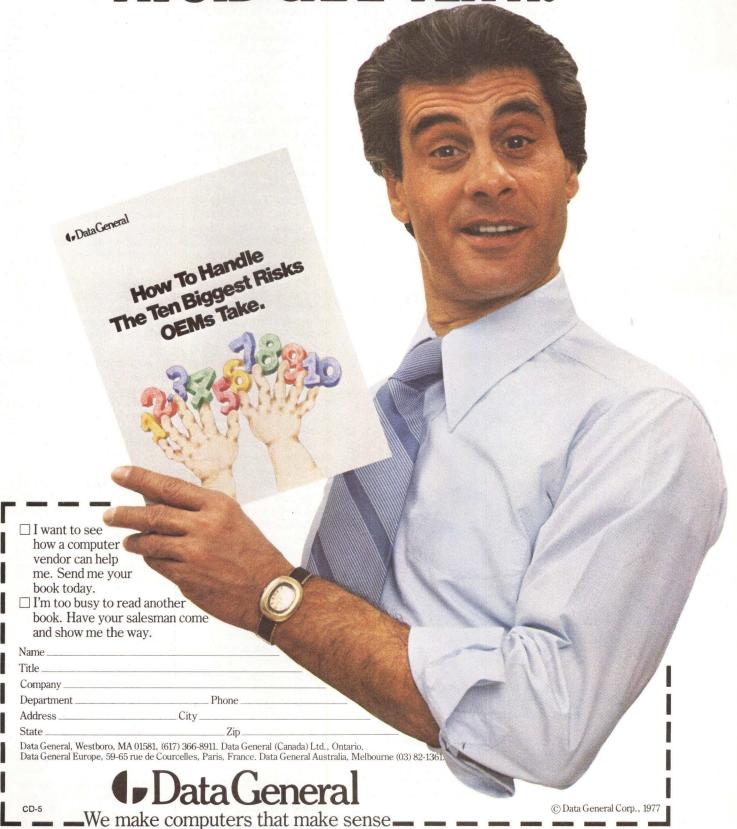




Photo Courtesy of Anaheim Visitor & Convention Bureau

Anaheim Convention Center, Anaheim, California, June 5-8

# 1978 National Computer Conference



Stephen W. Miller Conference Chairman



Dr Sakti P. Ghosh Program Co-Chairman



Dr Leonard Y. Liu Program Co-Chairman

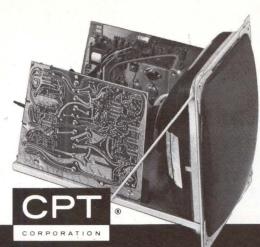
Claiming to be the biggest computer show on earth, the 1978 National Computer Conference will explore frontiers in information processing and examine the impact of current technology and methodology on the industrial, business, and public sectors. Conference chairman Stephen W. Miller, SRI International, Menlo Park, Calif sees this year's conference as encompassing the complete spectrum of information processing technology and applications. Trends receiving special attention will include software engineering and small systems.

Program committee co-chairmen Dr Leonard Y. Liu, director of systems architecture and standards, IBM, Poughkeepsie, NY, and Dr Sakti P. Ghosh, IBM Research Laboratory, San Jose, Calif have defined a program consisting of 25 technical and professional areas. An average of four sessions are planned within each area, for a total of approximately 100 sessions, all designed to expand on new knowledge in information processing by computer specialists as well as users, managers, educators, hobbyists, and government officials. Areas slated for special attention include electronic funds transfer systems, office automation, microcomputer applications, simulation, information processing management, software techniques, database management, regulatory policies, and computer-related legislation. Sessions will be user-oriented and will present recent developments having practical applications rather than theoretical concepts. Increased attention will be given this year to computer developments in Japan. NCC '78 is sponsored by the American Federation of Information Processing Societies, Inc (AFIPS) together with four of its participating organizations—the Association for Computing Machinery, the Data Processing Management Association, the IEEE Computer Society, and the Society for Computer Simulation.

The technical program, emphasizing practical applications and effective solutions to data processing problems, will include four major areas covering computer Applications, Methodology, Systems, and the impact of computers on People and Society. The Applications area ranges from special-purpose terminals, design automation and computer graphics, and artificial intelligence to electronic fund transfer systems, simulation, and home and hobby computing. Emphasis will be placed on applications of computers to solve world energy and resource problems, plus analyses of efforts in office automation. Methodology will include coverage of performance measurement and evaluation, programming methodology, automatic programming, and analyses of software techniques and tools. Systems will cover data networks, distributed systems, programming, and operating systems, with emphasis on computer architecture, the impact of recent developments on hardware technology, and database management systems. Lastly, the area of People and Society will explore communications regulatory policy, legislation and its impact, and computer careers and education.

### **Special Activities**

The trend towards small computing systems will be given special attention at the NCC '78 Personal Computing Festival to be held apart from the main conference, in the Disneyland Hotel Complex. The Festival will include a separate program covering personal computer graphics, music systems, speech synthesis, amateur radio, computer games, small business computers, and floppy disc systems. An exhibit area will show commercial displays of personal computing products and services. A Personal Computing Contest will consist of demonstrations and exhibits of a wide range of systems, devices, and applications. Separate one- and three-day registrations are available for this Festival, as is a booklet, Festival Digest '78, offering the papers presented during these sessions.



# Only from CPT Unique clarity and high density in a new black-on-white display module

This is an un-retouched photo of the new CPT HRD-15 Model S, black-on-white high resolution, high density raster display. As a result of faster scanning speeds and faster rise/fall rates, it gives you this unique clarity and high density. The "smear" at the edge of the dot is eliminated. The dot has more edge contrast, better definition. Developed to look as much as possible like the typewritten page, the CPT HRD-15 is human engineered for daily use without eyestrain.

For this photo, the <u>non-interlaced</u> system scans at 50,000 scan lines per second, refreshing the entire image at 60 times per second. Dot resolution is rated at .01 inch with clear definition, since rise/fall time is less than 3 nanoseconds. The phosphor is P-4, with others available on request.

Designed for text processing, the HRD-15 uses a 15" CRT to display up to 64 lines of text, 96 characters to the line and at a lower cost per character than ordinary display tubes. Other applications include graphics, typesetting, and data terminal users.

This monitor component is offered with an attractive OEM schedule, and is available within 30 days of receipt of order. Choose from two models:

Model S Model H

With more than 12,000 word processing systems in use, CPT has proved itself an established and reliable leader in the field. CPT products are sold and serviced in over 100 U.S. cities and 30 countries around the world.

For more information or a demonstration on the new HRD-15, write: CPT Corporation, 1001 Second Street South, Hopkins, MN 55343. Or phone: (612)935-0381

Under the direction of Gopal Kapur, a consultant from Danville, Calif, the Professional Development Series of 12 seminars will cover areas critical to system development, structured methodology, software engineering, database management, and cost-effective computer usage. Held at The Inn at the Park Hotel, each seminar will consist of a one-day minicourse designed to increase professional skills and aid in career development. The separate fee for each seminar is \$45 and includes complete course material plus access to the four-day exhibit program and Personal Computing Festival.

### **Exhibits**

With the addition of West Hall at the Anaheim Convention Center, over 4000 industry representatives from more than 330 organizations will demonstrate products and services, provide technical and commercial data, and help attendees find solutions to their information processing needs. Exhibit hours will be from 11 am-7 pm on Monday, 10 am-6 pm on Tuesday and Wednesday, and 9 am-4 pm on Thursday. The exhibits will cover areas such as components, data communications equipment, education and training materials, minicomputers, memory systems, and test equipment.

### Registration

Conference attendees who have not preregistered (May 19 deadline) may register at The Convention Center, Fees are:

Full Conference (4-day program, exhibits, Conference Proceedings, 3-day Personal Computing Festival program, exhibits) \$75 Full Week Exhibits Only (including Personal Computing) \$25

1-Day Program and Exhibits (including Personal Computing) \$25 Students (Full week of exhibits

and programs) \$10 Personal Computing Festival (3-day program

and exhibits) \$9 1-Day Personal Computing (program and

Additional copies of the Conference Proceedings may be purchased at the Conference for \$30, or after the Conference for \$60. The Personal Computing Digest price is \$9.

The NCC Travel Service will feature low cost air transportation, special attention upon arrival at Los Angeles International Airport, courtesy desk at the Anaheim Convention Center to handle flight reservation changes, and assistance in coordinating air and ground travel arrangements. Travel information is available from the NCC '78 travel service by calling 800-556-6882. For details on where to go and what to see in Southern California, contact the Southern California Visitors Council, 705 West Seventh St, Los Angeles, CA 90017. Additional information on the National Computer Conference may be obtained by writing AFIPS, 210 Summit Ave, Montvale, NJ 07645 or by calling

Excerpts from the Technical Program contain sessions of particular interest to readers of Computer Design. Information is limited to that available at press time.

### **CONFERENCE AT A GLANCE**

### MONDAY A M

**OPENING PLENARY SESSION** 

9:30 a m, Monday, June 5 Leading members of the Administration will assess Computers and Energy

2:00-3:40 3:50-5:30

COMPUTER MODELS IN SOLVING WORLD'S ENERGY PROBLEM

**Energy Decision** Analysis Robert Korsan

Computer Modeling in Energy Technology Julius Chang

### DATA PROCESSING MANAGEMENT & ADMINISTRATION

Time Management for the DP Professional James F. Towsen

Motivation of the DP Professional J. Daniel Couger

### DATABASE MANAGEMENT SYSTEMS

Distributed Database Technology Robert W. Taylor

Database Design Methodology Vincent Y. Lum

### DATA NETWORKS

International Data Networks **Barry Wessler** 

Nationwide Packet Switching Networks Lawrence G. Roberts

### OFFICE ' **AUTOMATION**

Word Processing: A Revolution or an Evolution? Evelyn Berezin

COMPUTER ARCHITECTURE

User Impact on Architecture Stephen S. Yau

#### HOME & HOBBYING COMPUTING

The Current Situation & the Forseeable Future Jim C. Warren, Jr.

Personal Hardware, Software and Applications Carl T. Helmers, Jr.

### **DESIGN AUTOMATION &** COMPUTER GRAPHICS

Computer Aid for Automatic Layout of Integrated Circuit Masks Charles W. Gwyn

Automated Design of Digital Systems William M. vanCleemput

### PERFORMANCE MEASUREMENT & EVALUATION

Mathematical Analysis of Computer Performance Computer Performance Hisashi Kobayashi

Management Philip J. Kiviat

### CONFERENCE RECEPTION

6:30 pm Disneyland Hotel

TUESDAY A M 8:15-9:55 10:05-11:45			TUESDAY PM 2:00-3:40 3:50-5:30		
Protection in Operating Systems R. Stockton Gaines	PROGRAMMING & History of Programming Languages Jean E. Sammet	C	PERATING SYSTEMS  COBOL—A Status Report Paul Oliver	Data Encryption Peter Denning	
COMPUTER MO WORLD'S ENE Computers in Oil Exploration Pierre L. Goupillaud	DELS IN SOLVING RGY PROBLEM Energy Modeling Panei William F. Rousseau				
	SIMULATION SIMULATION SIMULATION SIMULATION SIMULATION Walter J. Karplus	1C	Large Scale Simulation: Can Large Scale Models Alleviate World Resource Problems? John McLeod	Microprogramming & Simulation Gary J. Nutt	
DATABASE MANA Data & Program Conversion Allen Merten	GEMENT SYSTEMS Programming Language Interfaces to DBMS Sham Navathe				
DATA NE International Computer Communications Regu- lations George J. Lissandrello	TWORKS Satellite Data Communications for Public Service Sector John Witherspoon		PERFORMANCE & EVAL Computer Performance Technologies Stephen R. Kimbleton	MEASUREMENT LUATION Computer Performance Modeling Jeffrey P. Buzen	
	COMPUTER A Impact of Semiconductor Technology on Computer Architecture Gordon Moore	AR	Architecture Evolution I Samuel H. Fuller Daniel E. Siewiorek C. Gordon Bell	Architecture Evolution II Samuel H. Fuller Daniel E. Siewiorek C. Gordon Bell	
HOME & HOBBY Computers for the Mass Consumer Market	ING COMPUTING		OFFICE AU Hardware Architecture for Office Automation	TOMATION  Organizational Software for the Automated Office	

Computers for the Mass Consumer Market David A. Lien

DESIGN"

**AUTOMATION** 

Mature Design Automation Systems

Computers & Their Applications Nobukozu Inada RECENT PROGRESS IN JAPAN
Overview of Recent Progress in Japan I Toru Mikami

Larry J. Little

Overview of Recent Progress in Japan II Toru Mikami

Thomas M. Lodahl

### Waldo Magnuson, Jr. LEGISLATION & ITS IMPACT

Computer Crime Donn B. Parker Legal Aspects of Software Protection Michael S. Keplinger

Privacy Oliver. R. Smoot

### INDUSTRY LUNCHEON

12:00 noon, Tuesday, June 6
Featured Speaker: Harold J. Haynes, Chairman of the
Board and Chief Executive Officer, Standard Oil
Company of California

### ENERGY SYMPOSIUM

6:30 p m , Tuesday, June 6
Developing Energy and Computing Technology,
Chairman: Dr Cuthbert C. Hurd, President, Solar Energy
Research Associates

### PROFESSIONAL DEVELOPMENT SERIES

An Overview of Word Processing Amy D. Wohl, Datapro Research Corporation

Women and Management Update — Skills for Winning With

Dr Dru Scott, Dru Scott Associates, Inc

How to Get Started With Microcomputers Eric R. Garen, Integrated Computer Systems, Inc

Developing Managerial Skills

Donn L. O'Neil, Ph.D., National Learning Institute, Inc

Information Systems Architecture — A Management Perspective Cory K. Foster and Ocie M. Gamble, Cincom Systems, Inc

### WEDNESDAY A M

8:15-9:55 10:05-11:4

### WEDNESDAY PM

0-3:40 3:50-5:30

Introduction & Leading Applications Donald T. Lauer

Techniques & Programming Considerations John J. Quann Image Processing System Design George McMurtry Panel on Satellite & Other Data Characteristics Fred C. Billingsley

**LEGISLATION & ITS IMPACT** 

Personnel James P. Chandler Communications Philip S. Nyborg DISTRIBUTED SYSTEMS

Panel Discussion David J. Farber

**IMAGE PROCESSING & REMOTE SENSING** 

Design Methodology for Distributed Processing E. Douglas Jensen

OFFICE AUTOMATION

The Future of Office Automation David L. Holzman Computer-Based Document Distribution
Gwen C. Edwards

DATA PROCESSING MANAGEMENT & ADMINISTRATION

Organizational Repsonse & Information Technology Sichard L. Nolan

Why is DP Management So Difficult? Frederick Finch

DATABASE MANAGEMENT SYSTEMS

Making the Decision to
Go Database
James McKinney

Training Company & EDP
Personnel for Database
John Lyon
William Wilson

End User Facilities Henry C. Lefkovits Installation & Use of Database Systems George G. Dodd

PERFORMANCE MEASUREMENT & EVALUATION

End User Performance Considerations Shirley W. Watkins PIONEER DAY

SWAC Harry D. Huskey

COMPUTER ARCHITECTURE

Impact of Standardization on Architecture Tse-yun Feng Large Scale Computer Architecture Charles R. Vick

Special Purpose Machines I K.S. Fu Special Purpose Machines II K.S. Fu

SOFTWARE

METHODOLOGY Software Design & Analysis Donna Dunaway Advanced Specification Techniques Cordell Green

AUTOMATIC PROGRAMMING

Advanced Implementation Techniques
Thomas Standish

Advanced Implementation Techniques
Rot

Whither Automatic Programming
Robert Balzer

**EVOLUTION OF NEW HARDWARE TECHNOLOGY** 

VLSI: The New Semiconductor Revolution Frederico Faggin What's Ahead in Computer Memory & Storage Technology Lewis M. Terman The Future of Peripheral Devices Gil Gates Opportunity for New Technology Companies Vir A. Dhaka

**COMPUTER CAREERS & EDUCATION** 

CC&E: Requirements & Alternatives I **Michael Mulder**  CC&E: Requirements & Alternatives II Richard H. Austing How Does the Computing Professional Keep Up? Terry J. Frederick

What is Professionalism?
Donald B. Medley

**CONFERENCE LUNCHEON** 

12:00 noon, Wednesday, June 7
Featured Speaker: Dr. Theodore J. Williams, President,
The American Federation of Information Processing
Societies, Inc.

DINNER/THEATRE PARTY

6:00 p.m., Grand Hotel Cocktails, Dinner, Theatre Sebastian Playhouse Production Fiddler on the Roof

PROFESSIONAL DEVELOPMENT SERIES

Requirements Analysis and Definition Peter Freeman, SofTech, Inc

Computer Systems Capacity Planning and Performance Evaluation Dr Jeffrey P. Buzen, BGS Systems, Inc.

An Overview of Distributed Processing

Marshall D. Abrams, Ph D., Integrated Computer Systems, Inc.

Managing and Motivating the DP Professionals D. Grote, Performance Systems Corporation

Hows and Whys of Effective Computer Negotiations Kenneth G. Brindle, International Computer Negotiations, Inc

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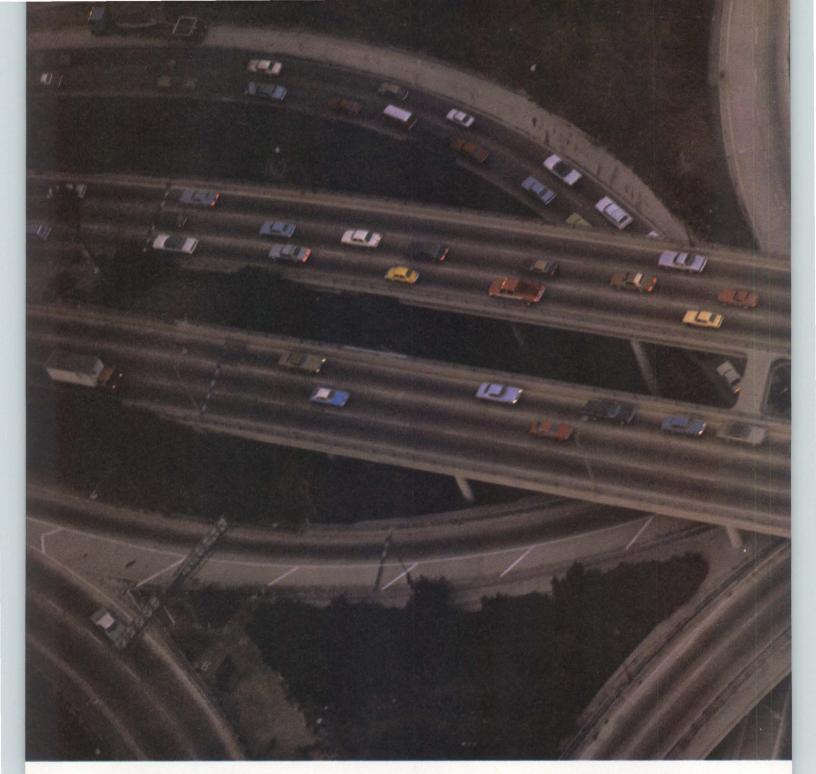
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CIRCLE 41 ON INQUIRY CARD





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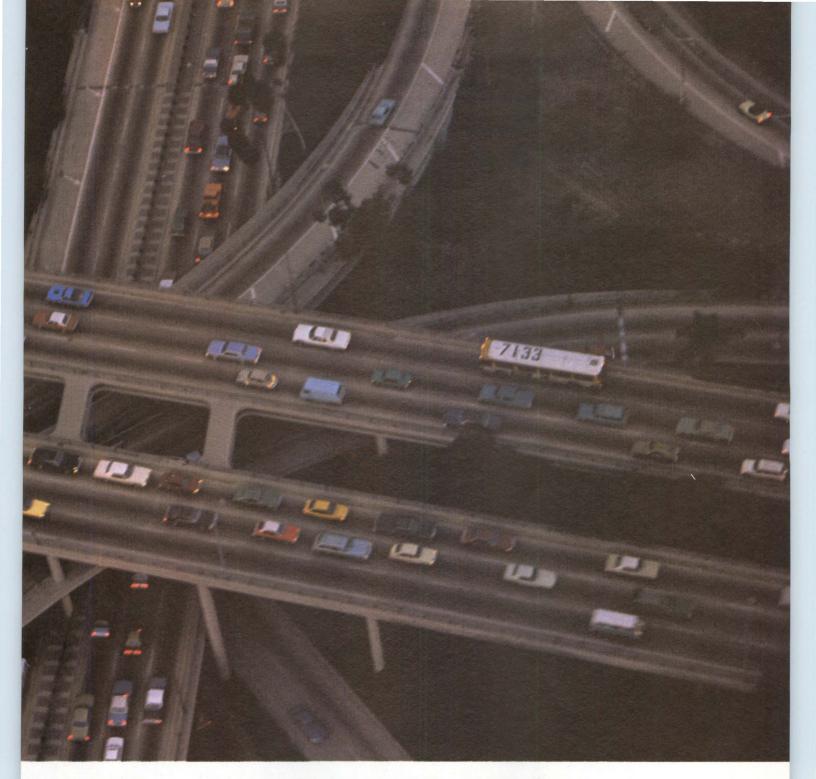
Such as the aggravating throughput problems you get from inadequate network design, limited CPU performance, and insufficient data base management capabilities.

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CIRCLE 42 ON INQUIRY CARD

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07608. Or call (201) 288-2000, extension 1789.



CIRCLE 43 ON INQUIRY CARD



### THURSDAY A M

10:05-11:45

### THURSDAY PM

	CDECIAL DUDE	0	OF TEDA AINIALO		
			SE TERMINALS	15.4.5.4.4	
Voice Interface to Computer Systems I George Glaser	Voice Interface to Computer Systems II George Glaser		Special Purpose vs. General Purpose Terminals Donald J. Birmingham	Future Developments of Special Purpose Terminals Rein Turn	
	DISTRIBUTE	D	SYSTEMS		
Local Data Networks Ira W. Cotton  Software/Applications/Pro- gramming Languages for Distributed Environment Eric Manning			Installing Distributed Systems George M. Crandell, Jr.		
DATA	PROCESSING MANA	G	FMFNT & ADMINISTRA	ATION	
Security Assessment Techniques James Cash  Contribution of Planning to Information Systems Productivity Charles Tucker			EDP Auditing-Member of the DP Community Joe Antal	Organizational Factors in the Allocation of Com- puting Resources Rob Kling	
	SOFTWARE DEVELOP	M	ENT METHODOLOGY		
Programming Method- ology Susan Gerhart  Software Verification, Vali- dation, & Testing Edward F. Miller			User Experience with New Software Methods Vic Basili	Software Maintenance Edward Yourdon	
	ARTIFICIAL I	N	TELLIGENCE		
Artificial Intelligence as a Scientific Field Raj Reddy	Question the Experts Peter Hart		Artificial Intelligence in Science & Medicine I Saul Amarel	Artificial Intelligence in Science & Medicine II Saul Amarel	
	EFTS ELECTRONIC FUI	VIL	TRANSFER SYSTEMS		
Current Developments in EFTS Stephen J. Kohn	Technical & Social Issues Russell H. Dewey		Legal Issues in EFTS Developments Robert Zimmer		
FORMAL N	METHODS IN PROGRAI	11/	MING & MICPOPPOG	PAMMING -	
Microprogramming Tools George Leeman	Micro-Code Correctness, Optimization & Speci- fication	V II	When Will Formal Methods be Practical? Karl N. Levitt		
	Bruce Shriver				
			NEW APP	LICATIONS	
				Application of Minicom- puters to Library Systems & Services Laura J. Rainey	
	COMPUTER CAREE				
Designing & Debugging Careers for Women in the Computer Industry Thelma Estrin	Computers in Early Education Orlando S. Madrigal		Accreditation Gerald E. Wagner		
	PERSONAL COM	PL	JTING LUNCHEON		
		R. F	Poppa, Chairman of the Officer, Pertec Computer		

### PROFESSIONAL DEVELOPMENT SERIES

Business Protection from Computer Crime and Accidental Loss Donn B. Parker, SRI International

Cryptographic Protection in Computer Systems

Principal Instructor: Richard E. Lennon, Systems Communications Division, IBM

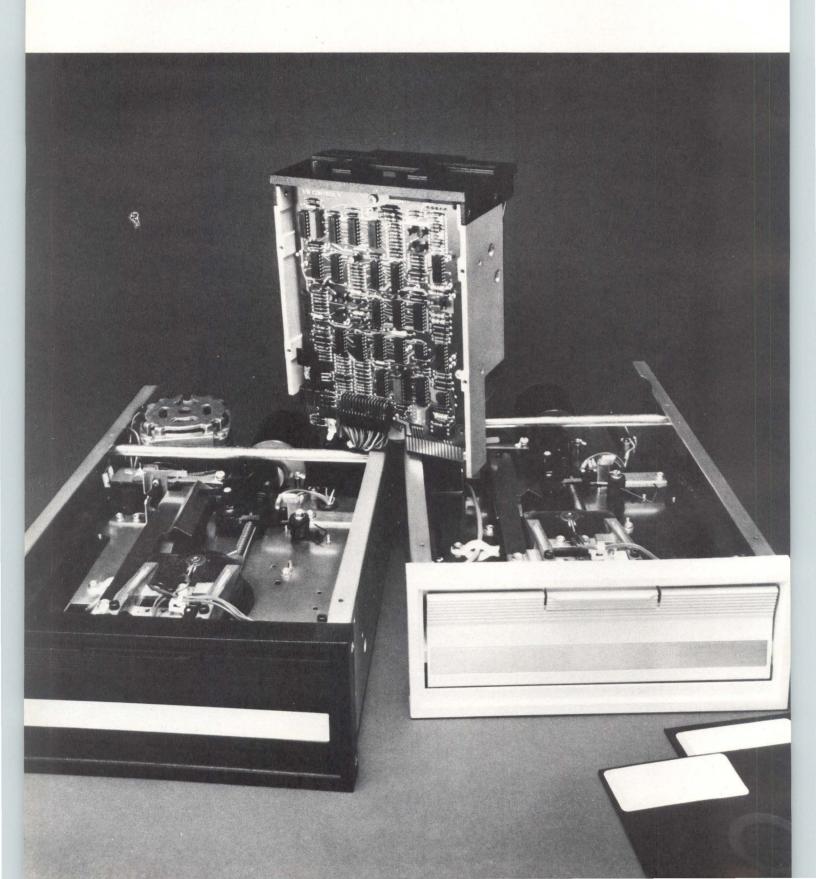
Designing the Database System Project

Leo J. Cohen, Performance Development Corporation

Hands-On Microcomputer Software/Hardware Workshop Eric R. Garen, Integrated Computer Systems, Inc.

Software Design Techniques: Structured Methodology — Truths and Fallacies Gopal K. Kapur, Kapur & Associates, Inc

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FD200	125K bytes/side (250K bytes/side, double density)	40	
FD400 (DC)	400K bytes (800K bytes, double density)	77	
FD500 (AC)	400K bytes (800K bytes, double density)	77	
FD250	218,250 bytes (437,500 bytes, double density)	70	
Name			
Title	Phone	Ext	



### **Technical Program Excerpts**

### **Monday Afternoon**

Session I

2-3:40 pm

California I-II

### Home and Hobbying Computing: The Current Situation and The Forseeable Future

Chairman: Jim C. Warren, Jr, Peoples Computer Co, Menlo Park, Calif

Since 1975 a multitude of companies have been created to address the marketplace of personal computing, resulting in 50,000 to 90,000 general-purpose digital computers in homes today. The chairman will briefly survey the history of this movement, detail the present situation, and hypothesize concerning the forseeable future. Panelists Ted Nelson, Swarthmore College; Portia Isaacson, The Micro Store; and Dan Ingalls, Xerox Palo Alto Research Center will address aspects of alternative forseeable futures.

Session 5

2-3:40 pm

Santa Ana I

#### International Data Networks

Chairman: Barry Wessler, Telenet Corp, Washington, DC

Public data networks are developing in several countries to provide domestic service to local subscribers. A requirement exists for international data services, but due to the structure of the international telecommunications industry, international service requires multiple organizations interconnecting dissimilar equipment rather than a single, coordinated, homogenous network. This creates special problems and requirements in order to result in a viable service. Panelists Mansanori Amano, KDD, Tokyo, Japan; John Goodman and George Orchard, British Post Office, London, England; and Tony Rybczynski, Bell Canada, Ottawa, Canada will describe aspects of the interconnection problem, potential solutions, and internetworking field trials underway.

Session 6

2-3:40 pm

Santa Ana II

### Computer Aid for Automatic Layout of Integrated Circuit Masks

Chairman: Charles W. Gwyn, Sandia Laboratories, Albuquerque, NM

Design of IC masks using manual techniques is tedious, time consuming, and often subject to errors because of precise design rules which must be followed during mask layout. In recent years, a number of computer aids have been developed to automatically generate custom design philosophies. These aids support the automatic layout of custom ICs by using the master slice approach with fixed cell locations, standard cells, various sized rectangular cells, and the connection of arbitrarily shaped components described via a shorthand manual layout description. This session will describe computer aids for each IC mask layout technique and example circuit layouts.

"The Automatic Wiring of LSI Chips," Ning Nan and Michael Feuer, IBM Corp

"A Speed Oriented Fully Automatic Layout Program for vLsi Devices," Al Feller, RCA Advanced Technology Laboratories "IC Design—Misery or Magic," Ken Loosemore, Compeda Ltd, Herfordshire, England

"STICKS: A Graphical Compiler for High Level LSI Design," John Williams, Hewlett-Packard Co

### Session 7 2-3:40 pm Garden Grove III Mathematical Analysis of Computer Performance

Chairman: Hisashi Kobayashi, T. J. Watson Research Center, Yorktown Heights, NY

This session describes recent results in the interdisciplinary area of computer systems modeling. Such models are important because they constitute a key source of design insight. New techniques for evaluating the performance of queueing systems, including an entropy-based approach to obtaining the time dependent behavior of certain queues and an efficient means for obtaining the cycle time of a closed queueing network, will be presented. In addition, recent results in evaluating the performance of processor scheduling algorithms will be described.

"Performance Evaluation of Nonpreemptive Response-Ratio Schedulers," Manfred Ruschitzka, Rutgers University

"Derivation of Equilibrium and Time-Dependent Solutions to  $M/M/\infty/N$  and  $M/M\infty$  Queueing Systems Using Entropy Maximization," John E. Shore, Naval Research Laboratory

"The Cycle Time of a Class of Closed Queueing Network Models," We-Min Show, T. J. Watson Research Center

Session 8

2-3:40 pm

Anaheim

### Word Processing: A Revolution or an Evolution?

Chairman: Evelyn Berezin, Redactron Corp, Hauppauge, NY

After reviewing the history and current state of office automation through considering evolutionary changes of the field from technical and marketing points of view, the economic history and current projection of the industry will be developed and compared to the data processing industry. Finally, panelists Jerry Tellefsen, Booz-Allan and Hamilton; and Amy Wohl, Datapro Research Corp will outline the surprising diversity of the office automation industry with a review of range, applications, and present areas of concentration.

Session 9

3:50-5:30 pm

California I-II

#### Personal Hardware, Software, and Applications

Chairman: Carl T. Helmers, Jr, Byte, Peterborough, NH

A variety of usual and unusual hardware, software, and applications are appearing as computers become personal devices. These facilities provide a wide range of problems and promise. The chairman will provide an overview of positive and negative aspects of personal computing equipment, programs, and uses. Panelists Louis E. Frenzel, Heath Co; Jeff Raskin, Apple Computer, Inc; Gary Kildall, Digital Research; and Adam Osborne, Osborne & Associates will present views regarding hard and soft facilities unique to consumer computing.

### Session 12 3:50-5:30 pm Orange County 18 Database Design Methodology

Chairman: Vincent Y. Lum, IBM Corp, San Jose, Calif

An important element for a successful database application is the presence of a good database design. While much work has been done and experience gained in the use of database systems, a solution to database design remains elusive. One important area is physical design. Because of the large number of parameters to be dealt with, it has been difficult to obtain a broadly applicable and reasonably accurate solution. The papers in this session will address this problem by proposing a method for the selection of appropriate access paths from numerous possibilities and by discussing a software implementation of a model for evaluating network database storage structures.

"Selection Efficiency Combination of Data Files for a Multiuser Database," Dennis G. Seyerance and Richardo A. Duhne, University of Minnesota

"Network Database Evaluation Using Analytical Modeling," Toby J. Teorey and Lewis B. Oberlander, University of Michigan

Speakers: M. Schkolnick, IBM Corp; and R. R. Brown, Hughes Aircraft Co

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Systems per year

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#### Session 13

the architectural design.

3:50-5:30 pm

Santa Ana I

#### **Nationwide Packet Switching Networks**

Chairman: Lawrence G. Roberts, Telenet Corp, Washington, DC Following the development of the research-oriented ARPANET, the first large-scale packet switching network, several other packet-type networks for a variety of applications have become operational or are under development. This session focuses upon the architectural similarities and differences of several packet-type networks, and how the application of the network influences

"Packet Switching Services for the Autodin Community," Donald O'Rourke, Civil Service Commission

"Implications of a National Computer Network for Higher Education and Science Research," SRI International; and Ron Segal, EDUCOM, Interuniversity Communications Council, Inc

"The Architecture of Telenet's Public Packet Network," Holger Opderbeck, Christopher B. Newport, Jay Hoffmeier, and Roy Spitzer, Telenet Corp

"A Comparison of Network Architectures: The ARPANET and SNA," Gilbert Falk, Bolt, Beranek and Newman Inc

### Session 14 3:50-5:30 pm Santa Ana II Automated Design Methodology of Digital Systems

Chairman: William M. vanCleemput, Stanford University, Stanford, Calif

Discussing computer-aided methods for design and analysis of hardware or software systems, this session will include papers describing an interactive programming system, SARA, which supports creative multilevel design of concurrent hardware or software systems. A panel will discuss various machine description languages and experiences with their use in analysis and design. This session's two parts are strongly interrelated since verification of real systems requires effective machine processable models of those systems; and design of real concurrent systems depends upon the validity of models of the systems out of which they are composed.

"A Methodology for the Design of Digital Systems Supported by SARA," Gerald Estrin, University of California

"SARA-Aided Design of Software for Concurrent Systems," I. Campos and Gerald Estrin, University of California

Speakers: M. Barbacci, Digital Equipment Corp and Carnegie-Mellon University; Daniel E. Siewiorek, Carnegie-Mellon University; and S. Crocker, USC Information Sciences Institute

### Session 16 3:50-5:30 pm Anaheim User Impact on Architecture

Chairman: Stephen S. Yau, Northwestern University, Evanston, Ill

This session's three papers will concern user's impact on computer architecture. Topics will include a computer with a multi-processor, a design methodology for a user-oriented computer system, and virtual addressing mechanism on the DEC PDP-11 family.

"Reflections in a Pool of Processors," William A. Wulf and Samuel P. Harbison, Carnegie-Mellon University

"A Design Methodology for A User-Oriented Computer System," C. V. Ramamoorthy and G. S. Ho, University of California at Berkeley

"VAX-11/780, A Virtual Address Extension to the DEC PDP-11 Family," W. D. Strecker, Digital Equipment Corp

Speakers: Samuel H. Fuller, Carnegie-Mellon University, and R. L. Ashenhurst, University of Chicago

#### **Tuesday Morning**

Session 17 8:1

8:15-9:55 am California | & ||

### Impact of Semiconductor Technology on Computer Architecture

Chairman: Gordon Moore, Intel Corp, Santa Clara, Calif

LSI technology advances have revolutionized computer architecture. As this technology progresses, achievements will be limited by the designer's ingenuity rather than by the semiconductor processing technology. In this session the chairman will review the history of semiconductor technology in relation to computer architecture, and the problems that are still existing. Future trends, opportunities, and impact of LSI technology on computer architecture will be discussed by panelists Lester Hogan, Fairchild Camera & Instrument Corp; and Robert Heikes, Motorola Inc.

### Session 18 8:15-9:55 am California III Mature Design Automation Systems

Chairman: Waldo Magnuson, Jr, Lawrence Livermore Laboratory, Livermore, Calif

Design automation using computers has been with us for over 20 years. This session will look at several aspects of using computers in design, documentation, and fabrication. In particular, this session will describe several mature design automation systems, all of which cover a wide spectrum of applications and have been in use for several years. Through the diversity of the systems described the impact of design automation systems will be apparent. In addition to pointing out where mature systems are contributing, future directions for design automation will be related.

"Interactive Graphics in Design Automation," Carl Machover, Machover Associates Corp

"The GM Network Station: A Low Cost Graphics System for Body Tooling," Thomas J. Reno, General Motors Corp

"Cost-Effectiveness of Computer-Aided Design," Vernon Pearl, USAARRDCOM

"Electronic can System Description," Bruce Inman, Boeing Aerospace Co

### Session 19 8:15-9:55 am California IV Protection in Operating Systems

Chairman: R. Stockton Gaines, The Rand Corp, Santa Monica, Calif

Over the last several years, the nature and dimensions of the security problem have become clearer, making it evident that it is a very difficult matter to design systems which can be relied on because of the correctness of the system design. The papers and panel speakers will address some of the issues that are involved and provide an assessment of the state-of-the-art today, and what can be expected in the future.

"Issues in Kernel Design," Gerald J. Popek and Charles S. Kline, University of California at Los Angeles

"Computer System Integrity," Peter G. Neumann, SRI International

Speakers: Anita Jones, Carnegie-Mellon University; and Michael Schroeder, Xerox Corp

### Session 21 8:15-9:55 am Santa Ana I International Computer

**Communications Regulations** 

Chairman: George J. Lissandrello, IBM Corp, North Tarrytown, NY

This session will match future international regulations against the continued growth of computer communications systems and technology utilizing international transmission media. Concerns will include the nonhomogeneous nature of national regulations as they apply to international computer communications systems, transborder data flow, and the need for new regulatory considerations for international satellite-oriented computer communications networks. These concerns and recommended solutions will be addressed from the point-of-view of a national satellite common carrier, a gateway state common carrier, and a data processing manufacturer and international service bureau company.

"Challenges in the Planning of International Communications," David J. Horton, Hawaiian Telephone Co

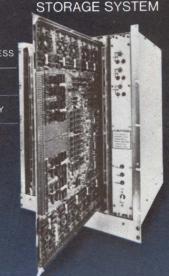
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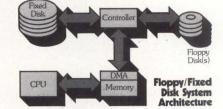
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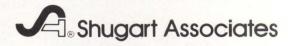


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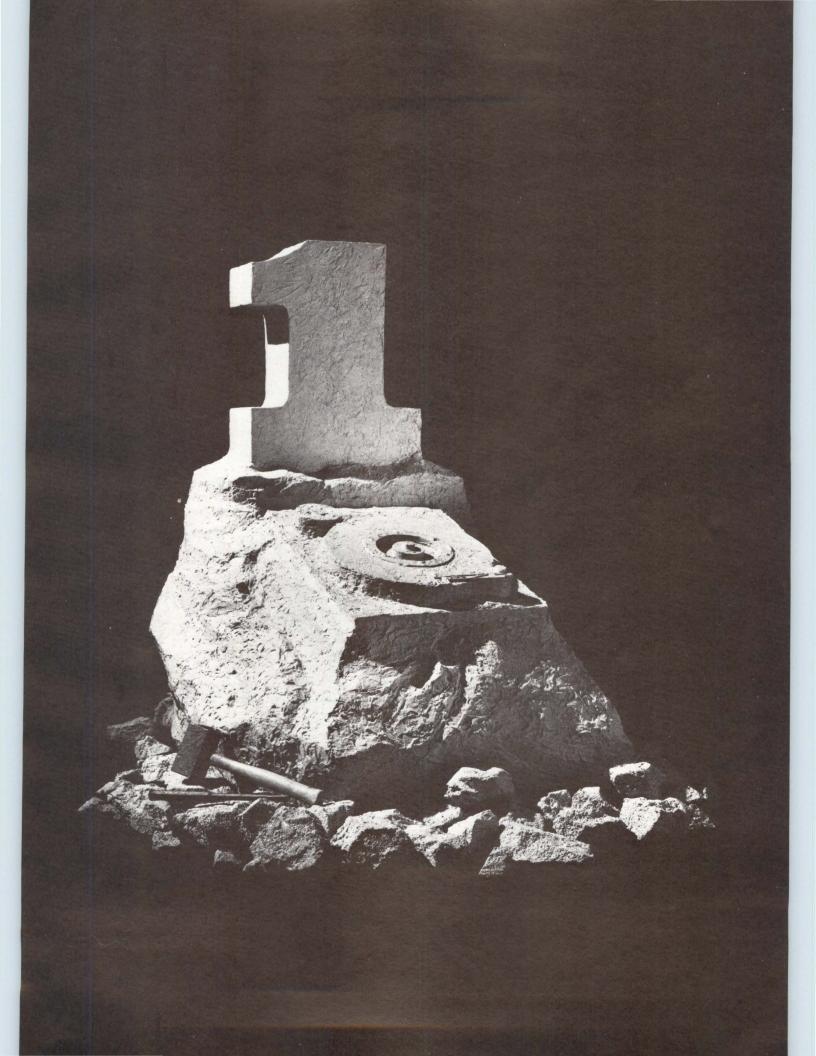
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"The Need for Continuation of Full-Period Transparent Private-Line Service," Philip C. Onstad, Control Data Corp

"Satellite Business Systems Innovative Services for Business Communications," Ronald W. McCabe, Satellite Business Systems

### Session 23 8:15-9:55 am Garden Grove III Computers for the Mass Consumer Market

Chairman: David A. Lien, Grossmont College, El Cajon, Calif

The microcomputer has progressed from a laboratory curiosity to a hobbyist toy, to a usable business and industrial tool. What of its potential as a mass-merchandised electronics device which can be used by persons technically disinterested and incompetent? Panelists Carroll D. Ray, Jr, Radio Shack; Stephen Jobs, Apple Computer Inc; Don Thompson, Atari, Inc; and C. Peddle, Commodore Business Machines will present their views and insights.

### Session 25 10:05-11:45 am California III Peripheral and Multiprocessors in Simulation

Chairman: Walter J. Karplus, University of California, Los Angeles, Calif

Hardware can be inexpensively produced in configurations suited to simulation applications. Most simulation problems involve a large number of parallel elements and concurrent activities. Hardware elements can be connected in parallel to handle such problems through several different approaches; the parallel system may be an add-on to a general-purpose computer; a general parallel multiprocessor may be built; or a parallel system may be specifically configured for a particular class of problems. This session will contain papers describing a system that can be used with many large computers, and the use of multiple processors working in parallel.

"A Multiprocessor Digital Computer for Dynamic Systems Simulation," R. M. Howe, University of Michigan; and E. Gilbert, Applied Dynamics International

"Plasma Simulation on the UCLA CHI Computer System," R. W. Huff, C. C. Wu, and John M. Dawson, University of California, Los Angeles

"A Multiple Microcomputer Approach to Fluid Flow Problems," J. Steinhoff, Grumman Aerospace Corp

### Session 30 10:05-11:45 am Garden Grove III Computers and Their Applications

Chairman: Nobukozu Inada, Nippon Telegraph and Telephone Public Corp, Kanagawa, Japan

Presentation topics will include the development of a high performance n-Mos/sos microprocessor with flexible architecture, which speaks well of the level of semiconductor and computer technologies in Japan. Two computer applications will be presented: a comprehensive automobile control system designed for optimally navigating drivers to their destinations, and an advanced process control system using a distributed processor systems concept. The advantages and possibilities of the latter in both hardware and software developments will be discussed.

"Development of a High Performance Universal Computing Element—PULSE," Hajime Iizuka and Yutaka Hayashi, Electrotechnical Laboratory, Japan; and Keikichi Tamaru and Hisashi Hara, Tokyo Shibaura Electric Co, Japan

"CACS-Urban Traffic Control System Featuring Computer Control," Toru Mikami, Nippon Electric Co, Ltd, Japan

"A Distributed Processing System and Its Application to Industrial Control," Y. Matsumoto, O. Sasaki, and T. Sumi, Toshiba Electric Co, Japan

### **Tuesday Afternoon**

### Session 31 2-3:40 pm California I & II Architecture Evolution—I

Chairmen: Samuel H. Fuller and C. Gordon Bell, Digital Equipment Corp, Maynard, Mass; and Daniel E. Siewiorek, Carnegie-Mellon University, Pittsburgh, Pa

Double session will feature presentations based on the January 1978 Computer Architecture issue of the Communications of the ACM. Two presentations will deal with machines designed and built at Manchester University, Manchester, England, which have had a strong influence on the English computer industry. The remaining presentations will focus on three successful compercial computers, including an examination of how and why these computer architectures evolved over the last 15 years. The final paper will concern the Cray-1 computer, a very high speed, vector-oriented processor.

"Manchester Mark I & Atlas—A Historical Perspective," S. H. Lavington, University of Manchester, England

"The Development of MU-5 Computer Systems," R. N. Ibbett and P. C. Capon, University of Manchester, England

"Evolution of Sperry Univac 1100 Series—A History, Analysis, and Projection," Barry R. Borgerson, M. L. Hanson, and P. A. Hartley, Sperry Univac

"Evolution of DECsystem 10," C. Gordon Bell, Alan Kotok, Thomas N. Hastings, and R. Hill, Digital Equipment Corp

"Architecture of IBM System/370," R. P. Case and Andris Padegs, IBM Corp

"Cray-1 Computer System," Richard Russell, Cray Research, Inc

### Session 33 2-3:40 pm California IV COBOL—A Status Report

Chairman: Paul Oliver, Federal COBOL Compiling Testing Service, Dept of the Navy, Washington, DC

COBOL is the most widely used programming language in the U.S. It was first standardized in 1968 and updated six years later. By mid-1977 about one dozen COBOL 74 compilers had been made available to the public, with its impact just now becoming apparent to most users. The COBOL standard will most likely be revised again in 1980. This session will provide a COBOL status update. Papers will suggest what the 1980 COBOL might look like, and will include a discussion of the database interface capability being considered for inclusion in the next COBOL standard.

"COBOL—The 1980 Standard—A Preview," George N. Baird, Margaret M. Cook, and Roger J. Gorg, Federal COBOL Compiler Testing Service, Dept of the Navy

"Database Facility for COBOL 80," Margaret M. Cook, Federal COBOL Compiler Testing Service, Dept of the Navy

"COBOL, Its Relationship with Other American National Standards," L. Arnold Johnson, Patrick M. Hoyt, and George N. Baird, Federal COBOL Compiler Testing Service, Dept of the Navy Speakers: Grace M. Hopper, U.S. Navy; and Jitze Couperus, Control Data Corp

### Session 35 2-3:40 pm Santa Ana I Hardware Architecture for Office Automation

Chairman: Larry J. Little, University of California, Livermore, Calif

The architecture of systems for office automation is diverse and rapidly changing. This session will present three views on these changes: firmware to software, standalone to distributed, and maxi to micro. Panelists Paul A. Mangione, Lexitron Corp; Harold S. Koplow, Wang Laboratories; and Jack T. Gilmore, Digital Equipment Corp will focus on the long range user effects.

### Session 36 2-3:40 pm Santa Ana II Computer Performance Technologies

Chairman: Stephen R. Kimbleton, National Bureau of Standards, Washington, DC

Unacceptable system performance requires changing either the system or its workload. Provided that both can be appropriately characterized, performance prediction techniques can be used to evaluate the results of specific user-oriented changes. New techniques will be described for classifying the workload of a computer system into clusters, for characterizing individual jobs, and for predicting system performance measures using a model based on a fast queueing network-based analysis technique.



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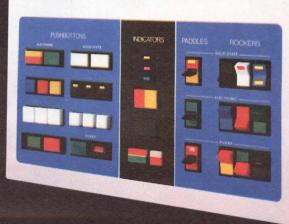
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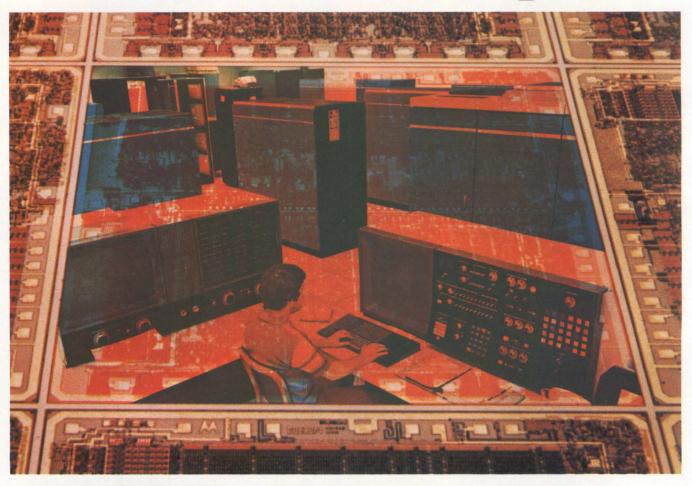
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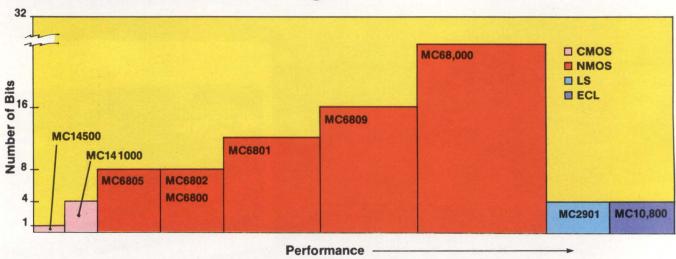
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A new brochure covering Motorola's total systems-onsilicon capability is just out. For a copy, and for copies of the MC6802 and MC6846 data sheets plus a product preview of the MC6801, circle the reader service number or write to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036.

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With 1.0, 1.5 and 2.0 MHz speed options of the MC6800 microprocessor at the center of the multi-chip approach, all necessary I/O, memory, and peripheral family functions complete the system. Later this year, introduction of the MC6809 advances multi-chip systems to a new performance dimension, and provides the bridge from 8-bit to 16-bit applications.

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of the multi-chip system to two, with little or no sacrifice in processing power or design flexibility, is the mission of our MC6802-6846 combination. It's the low-cost way to get more of the system on less of the silicon.

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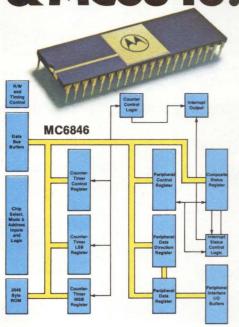
for low-end, low-cost applications.

Every one of Motorola's microprocessor-microcomputer products uses the EXORciser\* and/or its compatible system development tools for system development. All M6800 software, including FORTRAN, COBOL, BASIC, and MPL high-level languages, is fully compatible.

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Ten parallel I/O lines for controlling

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Together, these two chips supply

Output Butters

MC6802

ALU

Output Butters

Output Butters

Control

Control

Decode
Pointer
Program
Counter

Stack
Pointer
Planta
Control

Index
Register

Accumulator

Code
Register

Outs
Guiter

Accumulator

Ac

M6800 Family functions like the Asynchronous Communications Interface Adapter, MODEMs, Peripheral Controllers, and General Purpose Interface Adapter work with the '6802 just like it was a '6800. Indeed, they can't tell that it isn't a '6800. External multiplexed interfacing or buffering is never required between the MC6802 and any peripherals or memory.

In addition to the standard MC6800 features of the MC6802, it has a couple of unique advantages. The first 32 bytes of RAM can be held in a low-power mode during power down situations, permitting retention of critical data when power is lost.



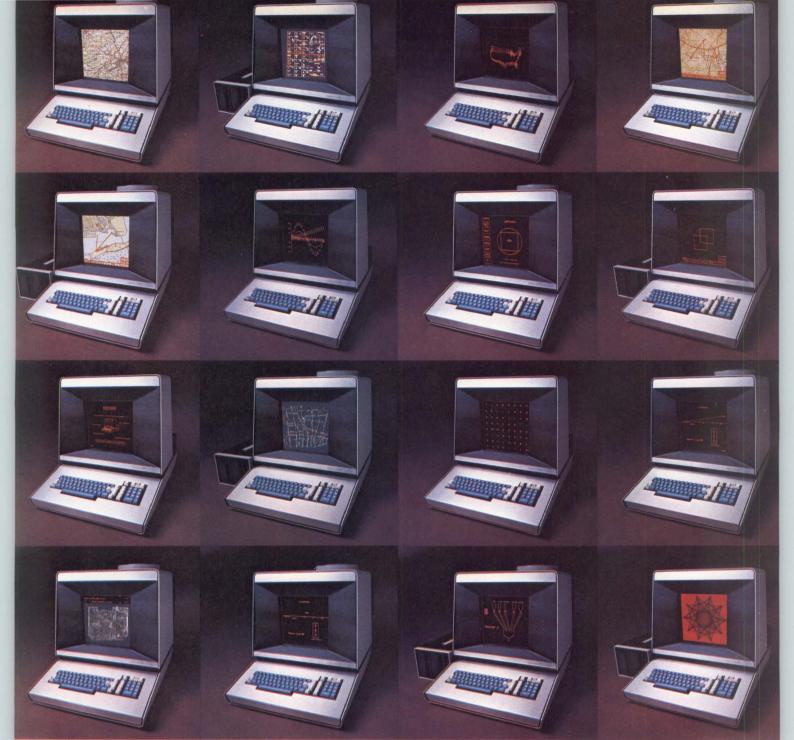
For enhancement of MC6802 system cost-effectiveness, you can replace the normal 1-MHz crystal with a 4-MHz crystal.

This low-cost, two-chip system is a winner. So you can familiarize yourself with it, Motorola authorized distributors are offering, for a limited time, a special information package with the MC6802 and MC6846, all for the price of the units, themselves.



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with three control lines for synchronous control of external circuits also are provided.



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DISPLAY SYSTEMS

CIRCLE 51 ON INQUIRY CARD

"BEST/1: Design of a Tool for Computer System Capacity Planning," J. P. Buzen, R. P. Goldberg, and A. M. Langer, BGS Systems, Inc; R. Lentz, H. S. Schwenk, and K. A. Sheetz, Booz-Allan Hamilton, Inc; and A. Shum, IBM Corp

"Job Scripts: A Workload Description Based on System Event Data," R. L. Mead and H. D. Schwetman, Purdue University "Predicting the Workload of a Computer System," A. K. Agrawala and J. M. Mohr, University of Maryland

Session 37 2-3:40 pm Garden Grove III

### Overview of Recent Progress in Japan—I Chairman: Toru Mikami, Nippon Electric Co, Kawasaki, Japan

This session will give an overview of the present status of semiconductor technology in Japan including lithographic methods and direct electron beam pattern generation schemes. These are considered to be the most important technologies for developing advanced VLSI ICS for next-generation computers. Presentations on research and development of new semiconductor devices with high speed switching capability and low power dissipation will also be included.

"Electron Beam Lithography for Advanced LSI Fabrication," Elichi Goto, University of Tokyo, Japan; and Takashi Soma, Masanori Idesawa, and Tateaki Sasaki, Institute of Physical and Chemical Research, Japan

"Semiconductor Technology in Japan," Takuo Sugano, University of Tokyo, Japan

Session 38 3:50-5:30 pm California | & ||
Architecture Evolution—||

This session is a continuation of Architecture Evolution—I, covered in Session 31.

Session 39 3:50-5:30 pm California III

Microprogramming and Simulation

Chairman: Gary J. Nutt, University of Colorado, Boulder, Colo

Technical developments have extended the range and power of simulation. One long-standing problem has been the development of software and systems for computers which are unavailable for use, unsuited for development, or not even built yet. Simulation has long been used to solve this problem and the experiment with new architectures and recent hardware developments have made it possible to create special computer facilities for these purposes. Such facilities can serve as universal hosts, capable of simulating a variety of computers. This session will present an overview of uses and advantages of emulation, and will describe an emulation facility and example application.

"Emulation: Tool for Software Development," N. F. Schneidewind, Naval Postgraduate School

"PRIM System: A Framework for Emulation-Based Debugging Tools," J. Goldberg, A. Cooperband, and L. Gallenson, University of Southern California

"A Microprogrammed AN/UYK-20 (V) Emulation," D. A. Deel and Walter A. Burkhard, University of California at La Jolla

Session 40 3:50-5:30 pm California IV

Data Encryption

Chairman: Peter Denning, Purdue University, West Lafayette, Ind

Cryptography fascinates because it appeals to instincts for exploring worlds of enigmas and puzzles. Its technology will secure data communications before leakage changes from a threat to a problem. In this session a computer terminal suitable for data retrieval will be discussed. Also reviewed will be NBS' encryption standard and cryptographic systems for data networks. The themes of this session may provide discussion on whether unbreakable ciphers based on short keys really exist; on the practical problems likely to be solved by this technology; and on whether this technology ultimately bolsters or threatens privacy.

"Data Dependent Keys for a Selective Encryption Terminal," Robert J. Flynn, Polytechnic Institute of New York

"Ciphertext/Plaintext and Ciphertext/Key Dependence Vs Number of Rounds for the Data Encryption Standard," Carl Meyer, IBM Corp.

"Security in Communication Networks," Martin E. Hellman, Stanford University

Session 43 3:50-5:30 pm Santa Ana II

### Computer Performance Modeling Chairman: Jeffrey P. Buzen, BGS Systems Inc. Lincoln, Mass

Models are tools for answering "what if" questions that arise during the evaluation of computer system performance. Typical questions concern the impact of growth in user workloads, upgrades to existing configurations, and adjustments to operating system parameters. Models can serve the needs of capacity planners, configuration managers, and system programmers, as well as mainframe vendors and peripheral manufacturers. This session will deal with the development and application of models for a variety

"A Hybrid Hierarchical Model of a Multiple Virtual Storage Operating System," W. W. Chiu and We-Min Chow, T. J. Watson Research Center

of performance evaluation problems.

"Effects of Peripheral Processor Wait List Positioning on System Performance," Ronnie G. Ward, B. B. Turner, and G. J. Hubbard, University of Texas

Speakers: T. P. Giammo, Social Security Administration; and A. W. C. Shum, IBM Corp

Session 44 3:50-5:30 pm Garden Grove III

Overview of Recent Progress in Japan—II

Chairman: Toru Mikami, Nippon Electric Co, Kawasaki, Japan

Recent advances in Japanese computer technology will be discussed from viewpoints of research and development in the field of computers. The characteristics of a newly developed computer series will be presented with a short historical background. The research and development projects of both VLSI and PIPS (pattern information processing systems) will be briefly described. Technological trends in applications of large computers will also be presented.

"The Development of Computers in Japan," Osamu Ishii, Electrotechnical Laboratory, Japan

"Remote Data Processing in Japan," Kanjiro Koshi and Kimio Ibuki, Nippon Telegraph and Telephone Public Corp, Japan "Train Operation Control Systems for High Speed Railway," Yoshiro Hayashi and Shigeo Yokota, Japanese National Railways, Japan; and Taizo Nauchi, Hitachi, Ltd, Japan

### **Wednesday Morning**

Session 47 8:15-9:55 am California III
Impact of Standardization on Architecture

Chairman: Tse-Yun Feng, Wayne State University, Detroit, Mich

A large degree of incompatability between subsystems of various manufacturers currently exists in spite of advances in computer technology. In this session, experts from various organizations will discuss the problems and possible solutions to intracomputer standards. The speakers will concentrate on different areas such as microprocessors, memory, and software, and where establishing the standards is of utmost importance.

"Intra-Computer Standards," Tse-yun Feng, Wayne State University

"Software Standards—With Hints of Their Relation to Computer Architecture," H. Hecht, La Jolla, Calif

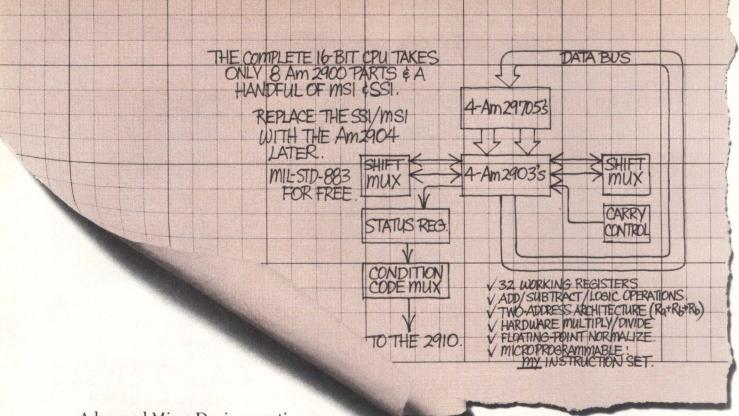
"Standards for Semiconductor Memory," J. Reese Brown, Jr, Burroughs Corp

"Microprocessor Standards," Robert G. Stewart, Stewart Research Enterprises

Session 48 8:15-9:55 am California IV

**VLSI: The New Semiconductor Revolution** 

Chairman: Frederico Faggin, Zilog Corp, Cupertino, Calif



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### CHAPTER THREE: THE CPU, PART ONE.

The Central Processing Unit is where all arithmetic functions take place.

The CPU consists of an Arithmetic Logic Unit, working registers, circuits to control the

# BUILDING A MICROCOMPUTER, CONTINUED.

shifting of registers and storage for the results.

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"Impact of vlsi on Future Microcomputers," Frederico Faggin, Zilog Corp

"Impact of vlsi on Computer Memories," Ron Whittier, Intel Corp

Session 52 8:15-9:55 am Garden Grove III

#### CC & E: Requirements and Alternatives—I

Chairman: Michael Mulder, U.S. Dept of the Interior, Portland, Ore

Panelists George Roe, Vashon, Wa; Harley Perkins, Tektronix Inc; Seymour Jeffrey, National Bureau of Standards; Charles Tonies, Hughes Aircraft Co; Robert Valek, Motorola; and Jack Shemer, Xerox Corp will present a variety of viewpoints on what skills and background graduates should have to enter computing careers. In addition, viewpoints will be given on what constitutes proper training after graduation. Weaknesses in the education of recent graduates will also be identified with panelists assessing the current structure of known curricula, and offering suggestions for improvement.

Session 53

8:15-9:55 am

Anaheim

#### Software Design and Analysis

Chairman: Donna Dunaway, Texas Instruments, Inc, Dallas, Tex

This session will emphasize software design, the activity that occurs between specification of a problem and the programming of its solution. One author will present a modeling scheme to aid in the design of the collection of concurrent processes. Also proposed will be a methodology for the construction of interactive systems. Techniques used to maintain reliability by placing the major responsibility for recovery from failures on software, and a tool for displaying system structure will be described.

"A Description Scheme to Aid the Design of Collections of Concurrent Processes," W. E. Riddle, University of Colorado; J. H. Sayler, University of Michigan; A. M. Stavely, New Mexico Institute of Mining and Technology; and J. C. Wileden, University of Massachusetts

"On the Construction of Interpretive Systems," Martin Freeman, Stanford University

"Software Fault-Tolerance in the Pluribus," John G. Robinson and Eric S. Roberts, Bolt, Beranek and Newman Inc

"MTR: A Tool for Displaying the Global Structure of Software Systems," Guy de Balbine, Caine, Farber and Gordon, Inc

Speaker: Ken Schoman, Jr. SofTech, Inc.

Session 56

10:05-11:45 am

California III

#### Large-Scale Computer Architecture

Chairman: Charles R. Vick, Ballistic Missile Defense Advanced Technology Center, Huntsville, Ala

To achieve solutions to real-time application problems, several millions of dollars were spent in generations of advanced computers resulting in supercomputers. However, the scope of solutions attained are far from those desired and new directions for future large-scale systems need to be defined. In order to do this it is essential to look back and assess the effectiveness of existing large-scale systems in satisfying user requirements. In this session, a perspective of large-scale systems will be given with an evaluation of their effectiveness.

"PEPE Architecture-Present and Future," Charles R. Vick, Ballis-

### BERGERLONG

### 2-Phase PM Stepping Motors & Drives

Step angles - 3.6°, 7.5°, 9°, 11.25°, 15°, 18° Steps per revolution - 20 to 100 Start/stop speed - up to 750 steps/sec Slew speed - up to 3,500 steps/sec









**Features** — Exclusive dual self-aligning sleeve or ball bearings. Unequaled reliability. Largest selection of angles per model. Wide choice of winding resistances. Performance unaffected by extremes in duty cycle and temperature (-20 to +80°C). Exceptionally high shock immunity.

3.6° step angle

Model RDM253/25 features the only 3.6° step angle in the industry. Highest efficiency — rare earth magnet design results in optimum torque/inertia/power/size ratios.

2-Phase drives

Inexpensive unipolar single chip translator driver (.35 A/phase) with optional output drive chip (1.5 A/phase). Bipolar constant current driver 90 V dc (12.5 A/phase).

Model No.	Step angle, degrees	Running torque, oz in.	Holding torque, oz in.	Phase cur- rent, amps	Phase resist- ance, ohms	Wgt,	Motor OD, in. (mm)	Shaft dia, in. (mm)
RDM 36/8 RDM 36/10	11.25 9	0.7 0.6	1.0 0.9	0.26 0.26	11.0 10.8	0.09	1.417 (36) 1.417 (36)	.078 (2) .078 (2)
RDM 50/5 RDM 50/6 RDM 50/8 RDM 50/10 RDM 50/12	18 15 11.25 9 7.5	4.1 4.9 5.1 5.4 6.4	5.7 6.9 7.1 7.1 9.2	0.67 0.67 0.67 0.67 0.67	4.4 4.4 4.4 4.4 4.4	0.25 0.25 0.25 0.25 0.25 0.25	1.968 (50) 1.968 (50) 1.968 (50) 1.968 (50) 1.968 (50)	.118 (3) .118 (3) .118 (3) .118 (3) .118 (3)
RDM 63/8 RDM 63/10 RDM 63/12	11.25 9 7.5	15.6 17.0 21.2	21.2 24.1 28.3	1.10 1.10 1.10	3.2 3.3 3.3	0.50 0.50 0.50	2.519 (64) 2.519 (64) 2.519 (64)	.157 (4) .157 (4) .157 (4)
RDM 253/25	3.6	8.9	10.0	0.15	75.0	0.21	1.653 (42)	.196 (5)

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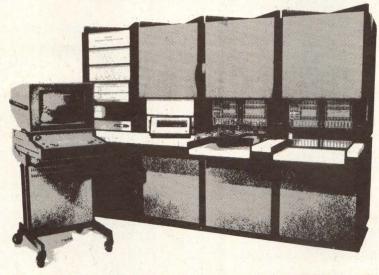
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The power of 5-MHz test rates to run fast LSI boards at their normal operating speeds.

The power of 444 channels to handle the most complex circuits without compromise.

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The power of automatic probing, to maximize throughput in high-volume applications.

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tic Missile Defense Advanced Technology Center; and Jack Cornell, System Development Corp

"PEPE—A User's Viewpoint: A Powerful Real-Time Adjunct," M. P. Mariani, TRW Inc

"Safari Through the Star 100 Architecture with Gun and a Camera," Neil Lincoln, Control Data Corp

"The Star 100-A User's Viewpoint," Frank McMohan, Lawrence Livermore Laboratory

### Session 57 10:05-11:45 am California IV What's Ahead in Computer Storage Technology

Chairman: Lewis M. Terman, T. J. Watson Research Center, Yorktown Heights, NY

Technical innovations and developments in computer memories and storage technologies have been remarkable. Magnetic core memories have been completely replaced by semiconductor RAMS, which reach a complexity of 64k bits on a chip. Magnetic bubbles and CCD memories have reached a stage where a prospect of solid-state mass storage is at hand. The fixed and moving disc memory technology continues to improve with significant reduction in cost/byte. In this session, the current status of computer memory and storage technologies will be described and an attempt will be made to project future progress.

"Semiconductor RAMS of the Future," Andy Varadi, National Semiconductor Corp

"Bubbles and CCD Memories: Solid-State Mass Storage," J. Egil Juliussen, Texas Instruments Inc

"Dynamic Evolution of Large Storage Magnetic Technologies," Steven Puthuff, Memorex Corp

Session 60 10:05-11:45 am Santa Ana II
Communications

Chairman: Philip S. Nyborg, Computer and Communications Industry Assoc, Arlington, Va

Communications policy has long been a matter of direct federal concern, based on the government's responsibility to regulate the communications industry. Panelists Donald A. Dunn, Stanford University; John M. Eger, Lamb, Halleck & Keats; and Philip M. Walker, Telenet Communications Corp will address the present status of federal policy, regulation, and legislation impinging on computer communications, as well as relevant anticipated developments and their impact on the data processing field. Specifically, the panel will discuss communications-related policy organizations in the Executive Branch, the ongoing FCC's "Computer Inquiry," and relevant legislation under consideration by the U.S. Congress.

Session 61 10:05-11:45 am Garden Grove III
CC & E: Requirements and Alternatives—II

Chairman: Richard H. Austing, University of Maryland, College Park, Md

Panelists will review alternative educational opportunities which are available for preparing for careers in computing. In particular, existing curricula at community colleges, four-year undergraduate degree programs, graduate programs, and professional development programs will be identified. The panel will summarize their papers and react to the comments on the educational requirements offered by the panelists in Part I.

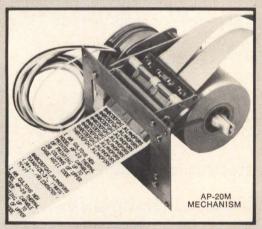
"Computer Education in Higher Education: Status, Alternatives, and Needs," John W. Hamblen, University of Missouri

"Computer Science and Computer Engineering: A Review and Overview of Curriculum," Gerald L. Engel, Old Dominion University; and Oscar N. Garcia, National Science Foundation

"The Status of Computer Education in the Community and Junior Colleges: Needs and Alternatives," Joyce Currie Little, Community College of Baltimore

"Business/Computer Science Curricula—A Survey," Kathryn L. Schenk and James R. Pinkert, California State University at Chico

### New Fixed Head Digital Thermal Printer Mechanisms



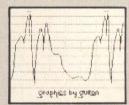
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AP-20M PRINTOUT

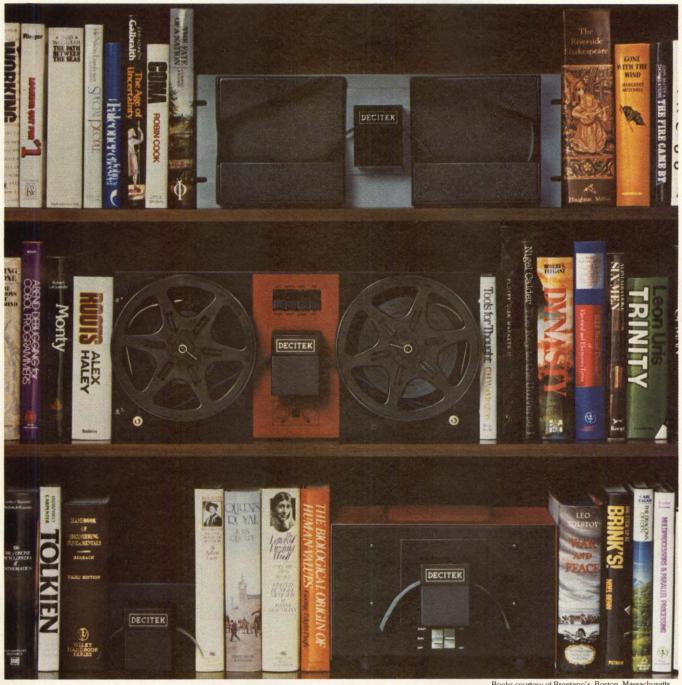
36--93.74 35+835.3 34--70.54 33--57.04 32+421.3

NP-7M PRINTOUT

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ANP-9M PRINTOUT

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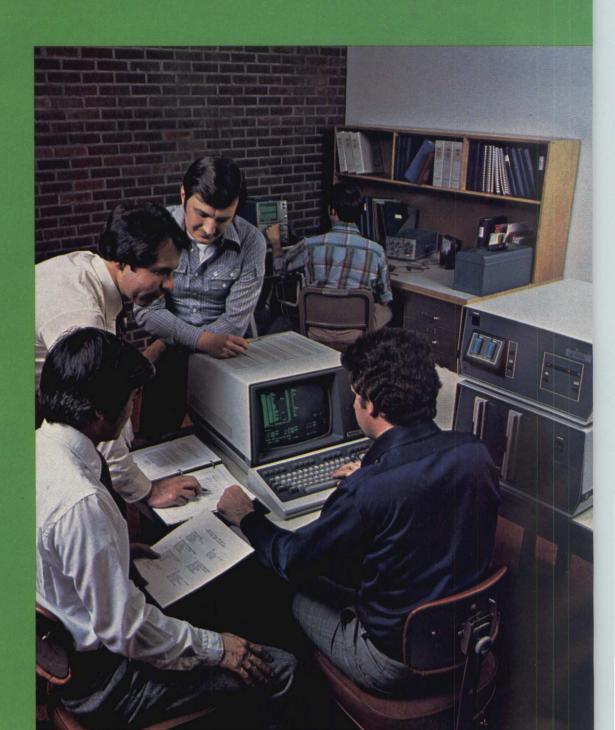
include tape readers for every OEM requirement plus a new desk top model with plug-it-in simplicity and flexibility.

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### WE'LL GET YOU GOING RIGHT.

Any new tool deserves a proper introduction. With Tektronix, that means installation and simplified training direct from the manufacturer.

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and your design team thoroughly at ease with the system—in short order. Tektronix quick service, exceptional documentation and quality assurance are all part of the package.

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Software can be tested, traced and debugged on a microprocessor identical to the one in your product design. Then software and hardware can be integrated and debugged stepwise, from partial to full in-prototype emulation.



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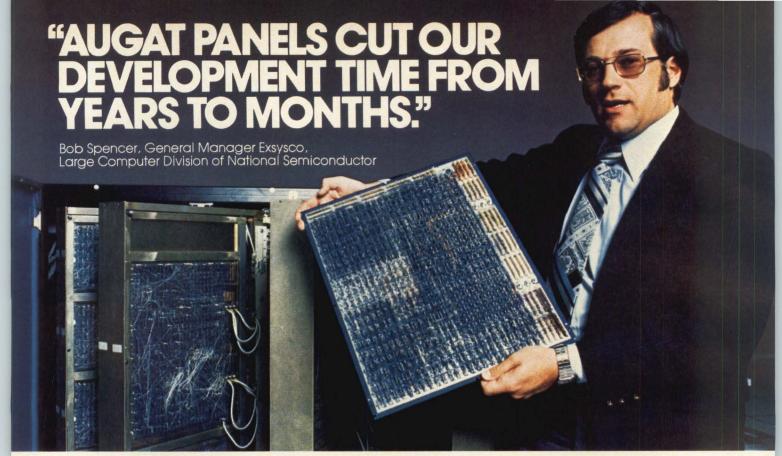
Tektronix has been building great instrumentation with full service back-up for 30 years. That's why 95% of all Tektronix customers come back for more. Ask your local Tektronix Sales Engineer for the full story, or write Tektronix, Inc., P.O. box 500, Beaverton, Oregon 97077. (503) 644-0161. In Europe, Tektronix, Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.



CIRCLE 56 ON INQUIRY CARD

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The dynamics of the computer industry demands that manufacturers capitalize on opportunities during the limited lifespan of the "current" technology. That's why initial development time is crucial. One sure way to cut that time is with Augat Wire-Wrap\* panels. Bob Spencer explains: "Multi-layer boards meant a lead time of

thousands of dollars, not to mention staffing and equipment. The Augat approach drastically reduced these costs allowing us to concentrate our resources on other critical design elements."

Packaging density is also vital in evaluating interconnection alternatives. "The multi-layer approach, with boards of typically 475 IC's,

would have required 15 layers to achieve the same density that Augat gave us."

National builds the Advanced



a year or more to design and prototype with another six months to get into production. With Augat boards, we reduced this cycle to a few months and started production the day we approved the prototype. Augat also gave us a flexibility to make circuit changes during the development cycle without causing delays."

Time isn't the only consideration—cost is also critical. "The expense to design and develop dozens of different, large multi-layer boards can easily run into the hundreds of

Systems<sup>™</sup> 4 and 5 computers for ITEL. These systems must offer high reliability. "As the temperature inside a computer goes up, the reliability goes down. Augat boards reduce the temperature problem because Wire-Wrap pins are excellent radiators."

The benefits also carry into the field. "Thanks to Augat boards, service engineers can make any required changes using simple tools. And because the boards are designed with sockets, we make repairs or upgrade systems quickly

by pulling the old chips and plugging in new ones. We also eliminated the cost and logistics of stocking hundreds of different, completed PC boards. Now we simply stock IC's."



How would Bob Spencer rate the performance of Augat Wire-Wrap panels? "Excellent! Our system uses high speed ECL throughout. Augat's patented logic panel, combined with unique automatic wiring from Augat's Datatex subsidiary, performs with no noise or transmission problems."

Throughout the computer industry, you'll find Augat boards at work in all kinds of logic applications delivering high speed performance and system flexibility at dramatic cost and time savings.

For further information, call Len Doucet at 617-222-2202. Or write Augat, Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703.

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Augat interconnection products, Isotronics microcircuit packaging, and Alco subminiature switches.

"A Brief Survey of Computer Science and Engineering Education," C. V. Ramamoorthy, University of California at Berkeley Speaker: Rahul Chattergy, Texas A&M

### **Wednesday Afternoon**

California I Session 62 2-3:40 pm

Image Processing System Design

Chairman: George McMurtry, Pennsylvania State University, University Park, Pa

The required image analysis cannot exist in a vacuum. This session will involve three types of efficient systems including large pipeline systems for handling large quantities of data routinely and quickly; flexible, modular systems for research and/or interactive analysis; and geographically-oriented systems for use with geocoded databases. These all have features in common: need for efficiency, need to retrieve and handle large multiple data sets, and possible need for interactive analysis and refreshed image displays.

"Applications of Interactive Digital Image Processing to Problems of Data Registration and Correlation," William B. Green, Jet Propulsion Laboratory

"Design of Pipelined Systems for Landsat Image Processing," Don Brabston and John E. Taber, TRW, Inc

"AOIPS-An Interactive Image Processing System," Peter A. Bracken, J. T. Dalton, J. J. Quann, and J. B. Billingsley, Goddard Space Flight Center

Session 64 2-3:40 pm Special-Purpose Machines—I

Chairman: K. S. Fu, Purdue University, West Lafayette, Ind

In most applications of pattern recognition and image processing, because of the large volumes of data involved, specialized pro-

cessors, designed to speed up processing with a high degree of sophistication, are replacing general-purpose computers. Thus, it is of the utmost importance to discuss the interface problems between computer architectures, and pattern recognition and image processing. This session will deal with possible forms of computer architecture suitable for pattern recognition and image processing applications.

"Special Computer Architecture for Pattern Recognition and Image Processing: An Overview," K. S. Fu, Purdue University "Experience with a Picture Processor in Pattern Recognition

Processing," B. Kruse, Kinkoping University, Sweden

"Design of Local Parallel Pattern Processor for Image Processing," Ken-ichi Mori, Masatsugu Kidode, Hidenori Shinoda, and Haruo Asada, Toshiba Research and Development Center, Japan "A Multi-Microprocessor ARES with Associative Processing Capability on Semantic Data Bases," Tadao Ichikawa, Kokusai Denshin Denwa Co, Ltd, Japan

"The STARAN Architecture and Its Application to Image Processing and Pattern Recognition Algorithms," J. Potter, Goodyear Aerospace

"The Criterion COBOL System," Michael D. Shapiro, NRC Corp "Reviews of the CLIP Image Processing System," M. J. B. Duff, University College of London, England

2-3:40 pm California IV

The Future of Peripheral Devices

Chairman: Gil Gates, Control Data Corp, Minneapolis, Minn

Printers and disc media constitute major computer peripheral devices. Significant development in these two areas including the future of printers with respect to both impact and nonimpact printing technologies compatible with plain paper will be discussed. The status of electrophotographic and ink jet nonimpact printer technology will also be described. Product performance capabilities and features will be analyzed. The evolution of disc technology will be covered.

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California III





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or 300 baud to 600 or 1200 baud transmission easily. Just flip the convenient switch and the terminal easily adapts to your communication speeds.

Front panel accessibility — All the normally used operator controls are organized into functional groups and logically arranged for maximum operator convenience.

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It's called the Sprint 5. And it's from Qume.

That's right. Qume.

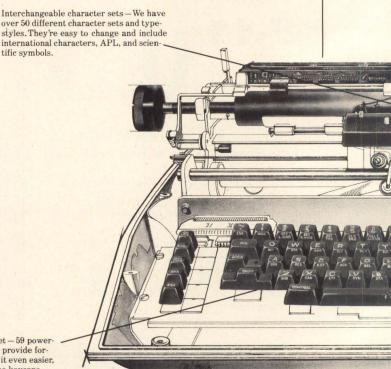
We've established quite a reputation in the word processing business. A reputation for letter quality print. And because of that, we didn't want to simply attach a keyboard to a printer and present it to the computer industry as a full blown terminal.

So we designed our Sprint 5 daisywheel terminal from the ground up to meet the needs of the computer industry. Complete with our famous print quality. And 55 cps speed.

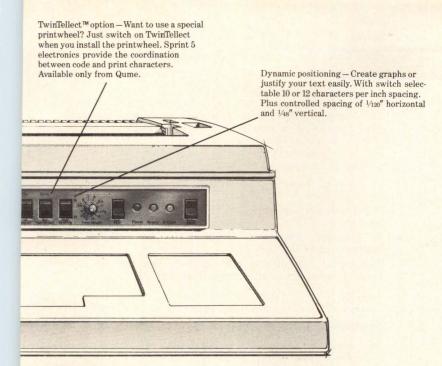
Qume's smart microprocessor gives the Sprint 5 many capabilities not found in conventional terminals. Such as a powerful command set, self-diagnostics, memory storage of tab settings, and forms control programs.

Smart microprocessor logic —You get flexible character spacing, precise plotting resolution, and smart multi-direction carriage slewing. Not to mention high quality printing. Fast.

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Comprehensive command set — 59 powerful user oriented commands provide format flexibility. And to make it even easier, commands are printed on the keycaps.



wheel terminal designed computer industry.

Multicolor ribbons - over 15 different

ribbons (10 color choices) to color your

Serial or parallel interface — Sprint 5's can provide a standard serial RS232C interface to your system. In addition, the keyboard version is available with DC current loop interface, and the printer version is available with DC current loop or parallel interface.

messages. Easy to handle cartridges with carbon or fabric multicolor ribbons.

Surprisingly enough, however, the Sprint 5 costs no more than competitive terminals.

Obviously, a product that does much more but costs no more is a better buy.

And when all is said and done, that may be Sprint 5's most outstanding advantage.

For further information on how the Sprint 5 can give your computer letter quality output, contact: Qume Corporation, 2323 Industrial Parkway West, Hayward, CA 94545 or phone Lee Cannon, (415) 783-6100, Extension 338.



Self test — Internal self-diagnostic routines can be initiated from the keyboard or from remote sites.

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"Trends in Printer Technology," Donald S. Swatik, Computer Peripherals, Inc

"Future of Disc Technology," David L. Conway and Thomas L. Muran, Magnetic Peripherals, Inc

Orange County 18 2-3:40 pm Session 66 **Advanced Implementation Techniques** 

Chairman: Thomas Standish, University of California, Irvine,

Once a formal specification has been created an implementation of it must be provided. Because so much effort is currently devoted to determining whether an implementation is a valid instantiation of its specification, it is important to recognize that the difficulty arises in the step from specification to implementation. Since implementation was conceptually achieved as a stepwise development process, validity is easier to prove by ensuring it at each step by the development of implementation. This approach is taken by the systems presented in the session.

"DEDALUS: The DEDuctive Algorithm Ur-Synthesizer," Zohar Manna, Stanford University; and Richard Waldinger, SRI International

"Automatic Representation Selection for Associative Data Structures," Paul Rovner, University of Rochester

"Efficiency Estimation: Controlling Search in Program Synthesis," Elaine Kant, Stanford University

"Transformational Implementation," David Wile and Robert Balzer, USC Information Sciences Institute

Session 67 2-3:40 pm Santa Ana I

**Panel Discussion** 

Chairman: David J. Farber, The Rand Corp, Santa Monica, Calif Panelists E. Douglas Jensen, Honeywell Systems & Research Center; Dick Eckhouse, Digital Equipment Corp; and Eric Manning, University of Waterloo, Canada will focus on some of the problems and solutions associated with distributed systems.

2-3:40 pm Garden Grove III How Does the Computing Professional Keep Up?

Chairman: Terry J. Frederick, Florida Technological University, Orlando, Fla

Many people now believe that the half-life of computing knowledge is only five to ten years. This consideration, plus the rapid growth of computing knowledge, make it impossible for anyone to know the entire field. This session will cover three aspects of how the computing professional keeps up: the nature of the problem, self-assessment, and professional development.

"A Problem: Knowledge Obsolescence of the Computing Professional," Paul Armer, On-Line Business Systems, Inc

"Self-Diagnosis: How ACM Uses Self-Assessment," Eric A. Weiss,

"A Treatment: Professional Development," Fred A. Gluckson, National Bank of Detroit

"Educational Considerations in Corporate Computer Careers," Roger Sullivan, Commercial Union Assurance Co

3:50-5:30 pm California III Session 72 Special-Purpose Machines—II

This session is a continuation of Special-Purpose Machines-I, covered in Session 64.

3:50-5:30 pm Session 73 California IV

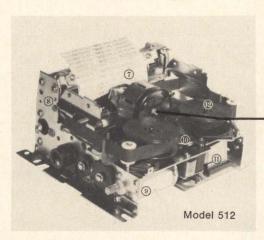
**Opportunity for New Technology Companies** 

Chairman: Vir A. Dhaka, Xerox Corp, El Segundo, Calif The last twenty years have been characterized by rapid tech-

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- · Samples \$245 each. Deliveries begin second quarter '78.
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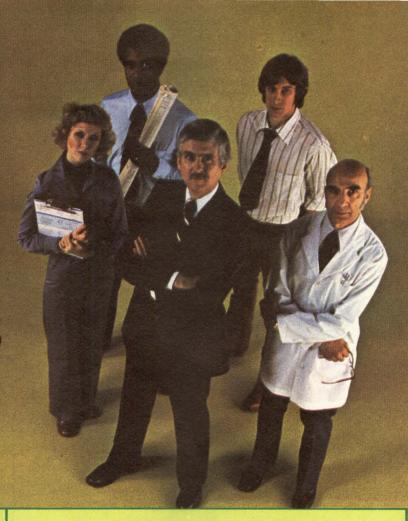
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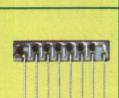
#### SQUELCH CIRCUIT

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Why have so many designers and buyers switched to Centralab thick film networks? The reasons are many. Compared to chip and wire hybrids, Centralab discrete hybrids are the most economical to buy...with lower start up costs. Compared to discrete components, our networks require less board space...help to minimize noise...and can reduce overall costs for equivalent circuitry. But some other reasons include...faster delivery...reduced assembly costs...higher yield...computer-aided design...automated production...five separate worldwide facilities...and over 30 years of Centralab experience in customized circuitry.

Why should you investigate Centralab thick film networks? Well, until you do, you won't know how our computer-aided design service optimizes layout, minimizes human error and, incidentally, speeds service. Or how our design engineering services — including worst-case analysis, component selection, thick film processing and 100% functional testing — produce reliable circuits. Until you investigate, you won't know how much you can gain using Centralab's cost-effective CERBON™ and Cermet thick film technology. To find out the ways that Centralab service can help your product, send for our new Thick Film brochure. Use the reader service card or call us at 414/228-2874.

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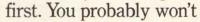


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nological innovations and developments in all areas related to computer technology such as processors, memories, magnetic disc and tape media, printers, and semiconductor technology. Technological innovations create unique opportunities for developing new markets. New enterprises which are not encumbered with an inventory of equipment representing the older technology often become the vehicle to bring the new technology to the marketplace. This panel discussion will focus on aspects of bringing new technologies successfully to the marketplace. All members of the panel including Robert H. F. Lloyd, Conver Corp; Richard Petritz, New Business Resources; Jessie Aweida, Storage Technology Corp; and Renn Zaphiropoulos, Versatec have achieved such a distinction. A brief statement from each panelist will be followed by audience questions and answers.

Session 75

3:50-5:30 pm

Santa Ana I

#### **Design Methodology for Distributed Processing**

Chairman: E. Douglas Jensen, Honeywell Systems and Research Center, Minneapolis, Minn

This session will include a paper dealing with message processing in a multilevel secure environment, and discussion of an implementation approach to network operating systems and a distributed processing system for a Naval Data Communication Network.

"Design of a Message Processing System for a Multilevel Secure Environment," Stanley R. Ames, Jr, The MITRE Corp; and Donald R. Oestreicher, USC Information Sciences Institute

"Network Operating Systems: An Implementation Approach," Stephen R. Kimbleton, National Bureau of Standards

"A Distributed Processing Systems for A Naval Data Communication Network," Wesley W. Chu, University of California at Los Angeles

Session 78

3:50-5:30 pm

Anaheim

#### **Technical Seminar—SWAC**

Chairman: Harry D. Huskey, University of California, Santa Cruz, Calif

Honoring the project team that created the NBS Western Automated Computer, known as swac, the first computer to use standard CRTs as memory devices and the first parallel stored program computer to become operational, seminar affords attendees the opportunity to gain an appreciation of the efforts involved when pioneering an industry.

#### **Thursday Morning**

Session 80

8:15-9:55 am

California II

#### Voice Interface to Computer Systems—I

Chairman: George Glaser, Centigram Corp, Sunnyvale, Calif

Bringing together leading experts to report on the state-of-the-art of voice input to computer systems, double session will consider the underlying technology and will review current applications. There will be a survey of current and pioneering efforts at several universities and equipment vendors, and a look at applications in government and industry, including speaker identification and verification. Panelists Wayne A. Lea, Speech Research Communication Laboratory; Frederick Jelinek, IBM Corp; Raj Reddy, Carnegie-Mellon University; Michael Curran, U.S. Naval Air Development Center; George R. Doddington, Texas Instruments, Inc; and Thomas B. Martin, Threshold Technology will conduct a question and answer period to conclude the session.

Session 81

8:15-9:55 am

California III

#### **Current Developments in EFTS**

Chairman: Stephen J. Kohn, Cleveland, Ohio

Panelists Les Plumly, Dept of the Treasury; Del Olson, Dayton-Hudson Corp; and Jerry Svigals, IBM Corp will bring together experts in EFTS, representing a variety of viewpoints. They will discuss where EFTS has been, what was promised, what was delivered, where we are now, and what trends are likely to emerge in the future. Viewpoints of the government, retail merchants,

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banks, and hardware/software vendors will be represented. Included in the discussion will be considerations of planning and integration into existing systems, marketing to consumers, retailers, and corporations; security; and cost impact and financial feasibility of alternate system approaches.

Session 83 8:15-9:55 am Orange County 18
Artificial Intelligence as a Scientific Field

Chairman: Raj Reddy, Carnegie-Mellon University, Pittsburgh, Pa

Through two invited papers, this session focuses on the incorporation and effective utilization of special-purpose expert-level knowledge appropriate for specific tasks. The first chronicals this development through the activities of the Stanford Heuristic programs. The second, which is the 1977 Computers and Thought Lecture, describes a system for discovering new mathematical concepts and conjectures involving those concepts.

"The Art of Artificial Intelligence: Themes and Case Studies of Knowledge Engineering," Ed Feigenbaum, Stanford University "The Ubiquity of Discovery," Doug Lenat, Carnegie-Mellon University

Session 85 8:15-9:55 am Santa Ana II

Microprogramming Tools

Chairman: George Leeman, T. J. Watson Research Center, Yorktown Heights, NY

Three issues confronting the microprogrammer are producing microcode, assuring that it is efficient, and guaranteeing that the code meets its specifications. This session will deal with three problems of emulation, optimization, and validation, describing techniques and tools that have been applied to existing production machines. A system for producing microcode by using both a high-level microprogramming language and techniques from structured programming and microprogram verification, and an approach for the formal validation of microprograms, will be considered.

"Code Optimization Techniques for Microcode Compilers," C. J. Tan, T. J. Watson Research Center

"An Approach to Firmware Engineering," David A. Patterson, University of California at Berkeley

"Microprogram Verification Considered Necessary," W. C. Carter, W. H. Joyner, Jr, and D. Brand, T. J. Watson Research Center

Session 86 8:15-9:55 am Garden Grove III

Designing and Debugging Careers for Women in the Computer Industry

Chairman: Thelma Estrin, UCLA-Brain Research Institute, Los Angeles, Calif

Career planning, useful to all computer professionals, is especially valuable to women in overcoming barriers to upward mobility. Panelists Marlys C. Hanson, Lawrence Livermore Laboratory; R. Naomi Guillen-Williams, Control Data Corp; Anita Cochran, Bell Laboratories; Carolyn J. Morris, Hewlett-Packard Co; and Donnamarie E. White, Advanced Micro Devices, Inc will discuss various approaches to career development, and the "bugs" women encounter as they advance up career ladders in hardware, software, and technical marketing areas. Both men and women can benefit from increased awareness of those societal and professional attitudes which hinder women from achieving positions of technical management leadership.

Session 88 10:05-11:45 am California II
Voice Interface to Computer Systems—II

This session is a continuation of Voice Interface to Computer Systems—I, covered in Session 80.

Session 89 10:05-11:45 am California III

**Technical and Social Issues** 

Chairman: Russel H. Dewey, SRI International, Menlo Park, Calif Panel will focus on issues that developers of EFTS systems will face in the areas of standards, auditability, control, and social



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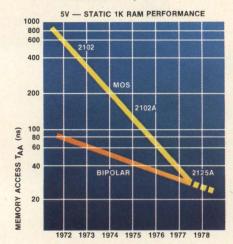
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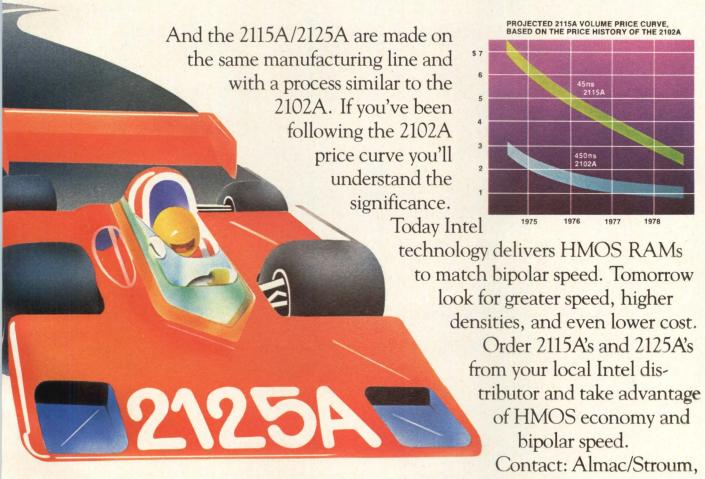
The 2115A and 2125A silicon gate static RAMs are pin-for-pin plug-in replacements for the popular 93415 and 93425 bipolar RAMs. They offer the same advantages. No need for external clocks or refresh circuits, fully TTL compatible, 16mA output sink current and operation from a single +5V supply. Worst case access time on our fastest version is 45nsec.

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2125AL 50% less power than the 93415/93425. This saves power supply and cooling costs which all adds up to additional savings in the cost of your system. And there's more. Unlike bipolar RAMs, the 2115A/2125A use only a single layer of metalization which means lower manufacturing cost and a more reliable process. So you can look for continued improvement in cost/performance. To put the cost potential in proper perspective, consider this: The 2115A/2125A chip is 35% smaller than Intel's industry standard 2102A.

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impacts. Specific issues to be discussed deal with standards for the plastic card, message interchange, encryption, and personal identification; EDP controls in the areas of transaction origination, terminal data entry, data communications, database update, and output processing; and audit tools and techniques for the EFTS environment. Finally, to present a balanced perspective, the impacts of different EFTS arrangements on the quality of life in American society will be explored from a theoretical position.

"Systems Auditability and Control in an EFTS Environment," Russell H. Dewey, SRI International

"Electronic Fund Transfer Systems and Quality of Life," Robert King, University of California at Irvine

Speaker: Irwin H. Derman, VISA U.S.A., Inc

#### Session 90 10:05-11:45 am California IV Software Verification, Validation, and Testing

Chairman: Edward F. Miller, Software Research Associates, San Francisco, Calif

The verification, validation, and testing area of software engineering represents a viable method for assuring necessary software quality levels regardless of the complexity and application of the software system. This method now involves the full spectrum of theoretical, application, and experimental sub-technologies. Three areas will be selected for in-depth investigation. Also presented will be a modern technological plan that can be applied to a wide variety of software quality assurance situations.

"A Language for Specifying Software Tests," David J. Panzl, General Electric Co

"A Software Quality Plan for Higher Education," Barry L. Bateman and Chadwick H. Nestman, Southern Illinois University

"The Design of a Prototype Mutation System," Timothy A. Budd and Richard J. Lipton, Yale University; and Richard DeMillo, Georgia Institute of Technology

Speaker: William E. Howden, University of California at San Diego

Session 91 10:05-11:45 am Orange County 18

#### **Question the Experts**

Chairman: Peter Hart, SRI International, Menlo Park, Calif

Devoted to answering questions posed by the audience, this session, immediately following the invited papers given during "AI as a Scientific Field," is expected to answer the many questions that arise from those papers. The experts include Saul Amarel, Rutgers University; Doug Lenat, Carnegie-Mellon University; Ed Feigenbaum, Stanford University; and Raj Reddy, Carnegie-Mellon University.

Session 93 10:05-11:45 am Santa Ana II

#### Microcode Correctness, Optimization and Specification

Chairman: Bruce Shriver, University of Southwestern Louisiana, Lafayette, La

There are several outstanding problems in the area of generating correct, highly efficient microcode, which runs according to its specifications. Panelists Barry Press, TRW Defense Space Systems Group; Steve Crocker, USC Information Sciences Institute; and George Leeman, T. J. Watson Research Center will contrast their views of these problems and examine solutions to them. Tools required to formally specify a machine with the intent of proving the correctness of its microcode will be discussed. A comprehensive test plan to determine the utility of several proposed algorithms for generating highly improved horizontal microcode will be presented. Finally, the general problem of microprogram specification will be reviewed.

#### **Thursday Afternoon**

Session 96 2-3:40 pm California II

#### Special-Purpose Vs General-Purpose Terminals

Chairman: Donald J. Birmingham, Data Pathing, Inc, Sunnyvale, Calif



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The EXORciser II\* Development System improves on the original EXORciser\* without making it obsolete. MACE 29/800\* extends the EXORciser's capability to systems using bit-slice architecture. The 3870 Emulator and 141000 Simulator are EXORciser-based development tools for single-chip microcomputers.



#### **EXORciser II develops high-speed systems.**

EXORciser II does everything the EXORciser does, adds a couple of neat new wrinkles, and operates at twice the speed. The key to the high speed is the new MPU II module, which includes both the system clock and the 2.0 MHz MC68B00 MPU. The clock circuit generates your choice of 1.0, 1.5, or 2.0 MHz signals, so the EXORciser II supports the full range of M6800 Family microprocessors.

DEbug II provides EXORciser II with a dual memory map. This capability dedicates a full 64K memory

map to EXORciser II, and creates a second 64K map in which you may implement your system. EXORciser II I/O can be accessed from either memory map.

The EXORciser II includes 32K of RAM, power supply, RS-232 port, selectable Baud rates from 110 to 9600, and a Macro Assembler/Editor. Optional modules also are available.

As for software, EXORciser II operates with all Motorola standard resident software packages; FORTRAN, COBOL, MPL, BASIC and Macro Assembler/Linking Loader.

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#### MC14 1000 Development System provides microcomputer simulation.

The 141000/1200 Simulator is an EXOP ciser-based system development tool for debugging designs using the new MC141000 series CMOS single-chip microcomputers. Complete software requirements are met, including cross assembler, loader, and debug package.

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For additional information on any of Motorola's EXORciser or EXORciser-based system development tools, complete the coupon or write your request for specific information to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

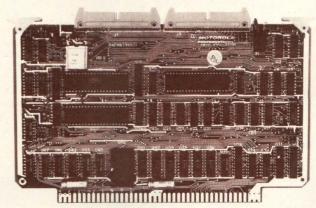


#### MACE develops ultra-high-speed systems.

MACE 29/800 minimizes the time and trouble of producing microprograms for systems based on bit-slice families like Motorola's high-speed M2900 and ultra high-speed M10800. The MACE 29/800 includes an EXORciser bus-compatible interface module and an EXORciser-resident software package that translate all microprogramming tasks into M6800-oriented operations.

The Write Control Store (WCS) in which your microprogram will reside is expandable in both depth and width. Ratios range between 8K words by 16 bits and 2K words by 112 bits, with intermediate configurations selectable in increments of 2K words or 16 bits. A maximum of seven WCS modules can be used.

MACE 29/800 is available as a separate unit for those who already have an EXORciser, terminal, and printer, or as a complete development station.



#### MC 3870 Development System provides real-time emulation.

The 3870 Emulator is another plug-in extension of the EXORciser. It provides real-time emulation of the MC3870 single-chip microcomputer.

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Special-purpose terminals are making a larger based market than ever before against traditional general-purpose terminals. An exploration of the terminal manufacturer's decision process to produce special-purpose data collection terminals and market them against established terminals will be presented. Also, the process of making special-purpose factory-oriented terminals work in a general-purpose computing systems environment of a large industrial manufacturer will be detailed. Highlighted in this session will be the directions of the specialized terminal industry and its impact on producers and potential users of general-purpose terminals.

"Decision Criteria in Terminal Product Planning," Eric C. Westerfield, Data Pathing, Inc

"Making a Special-Purpose Terminal Work in a General-Purpose Systems Environment," Donald J. Birmingham, Data Pathing, Inc

Session 99 2-3:40 pm Orange County 18
Artificial Intelligence in Science and Medicine—I

Chairman: Saul Ameral, Rutgers University, New Brunswick, NJ

The first four presentations in this double session will focus on the development of artificial intelligence (AI) systems in medicine. Aspects of research to be discussed include diagnostic problem-solving in internal medicine, treatment planning in glaucoma, experience with the evolution of designs of knowledge-based consultation systems, and applications of AI to the diagnosis and management of pulmonary diseases. Remaining presentations will concentrate on problems in AI systems designed to support scientific inquiry, in design of experiments, and in theory formation. Related work in the context of a mineral exploration task will be presented.

"A Dependency-Based Modeling Mechanism for Problem Solving," Philip London, University of Maryland

"Error Recovery in Robots Through Failure Analysis," S. Srinivas, Bell Telephone Laboratories

Speakers: Peter Szolovits, Massachusetts Institute of Technology; Casimir Kulikowski, Rutgers University; Harry Pople, University of Pittsburgh; Lawrence Fagan, Stanford University; John Kunz, Institute for Medical Science; Mark Stefik, Stanford University; Natesa S. Sridharan, Rutgers University; and Peter Hart, SRI International

Session 104 3:50-5:30 pm California II

#### Future Developments of Special-Purpose Terminals

Chairman: Rein Turn, TRW Systems, Inc, Redondo Beach, Calif

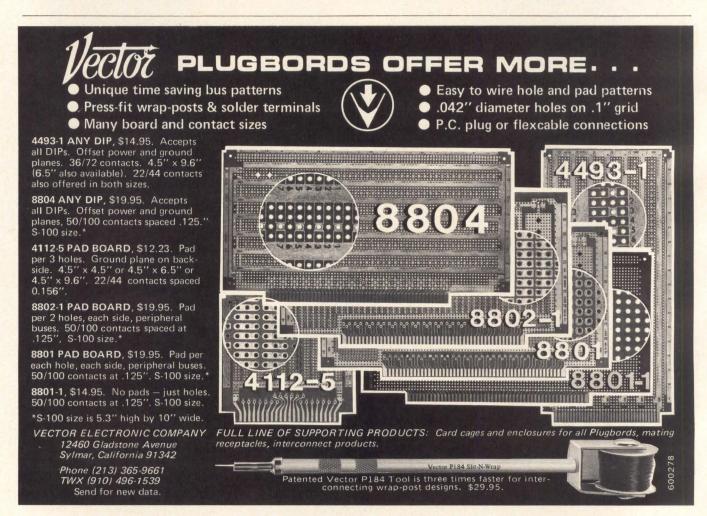
Many types of special-purpose terminals are being developed to increase the performance and cost-effectiveness of man-computer interfaces in various applications. As discussed by the chairman and panel speakers in this session, future advances in computer technology will provide new design options, such as providing built-in intelligence through the use of microprocessors and memory chips. Thus, in future terminals, more processing and storing information, and effective security features will be possible.

"The Future of Special-Purpose Terminals," D. G. Kovar, TRW Communications Systems and Services

Speakers: Robert Anderson, The Rand Corp; Carolyn Dunning, PCC Business Systems; and Marvin B. Herscher, Threshold Technology, Inc

Session 107 3:50-5:30 pm Orange County 18
Artificial Intelligence in Science and Medicine—II

This session is a continuation of Artificial Intelligence in Science and Medicine—I, covered in Session 99.



A new land speed record? A candidate for Guinness' Book of Records?

Perhaps so.

At any rate, Telefile Computer Products, Inc., of Irvine, California, decided to see if Telex' new highperformance tape drive really was as flexible as we've touted (and have a little fun along the way).

The results in Telefile's own words:

"We were impressed by Telex' engineering achievements and interfacing ease. To be able to offer such a variety of speeds and densities in a single basic unit seemed almost too good to be true.

"But Telex passed the test with flying colors. "It means that our customers can upgrade and increase system performance simply by changing circuit modules and heads on site. This flexibility will help keep our spares, training and logistics costs down, too."

Telefile has since increased their tape order to 200

units including formatters.

Now they can offer users of various minicomputers

and major mainframes the full range of storage capability in their Matchmaker systems—high- and low-density disk drives with tape to match.

Look into Telex' new dual-density tape drives and triple-density formatters. You'll have full IBM compatibility, break speed records (forward and reverse) and be able to handle lower-density PE and NRZI data formats ... and GCR as well.

Telex has the only tape drive and formatter in its class that writes 0.3-inch interrecord gaps—without

program restriction.

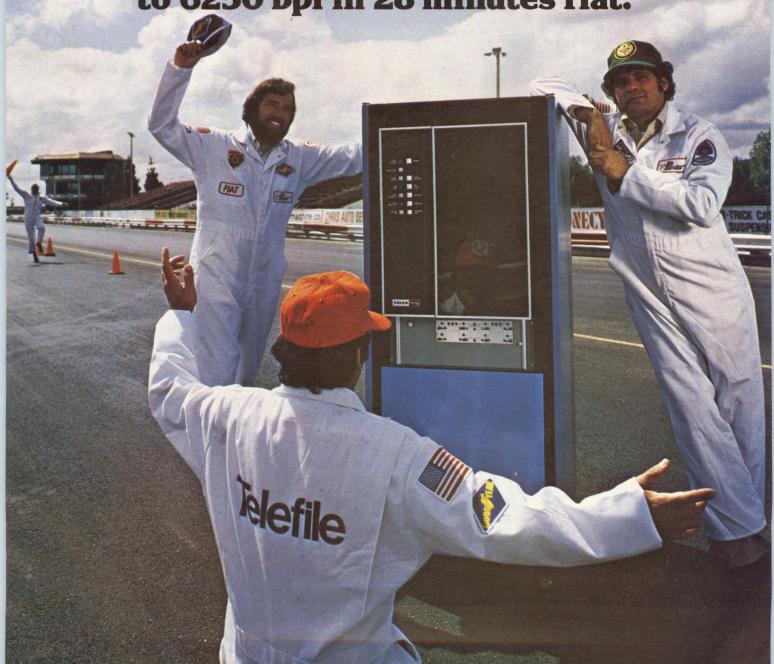
Get on the right track, contact: Dan O'Neill, Telex Computer Products, Inc., 6422 E. 41st St., Tulsa, OK 74135. Telephone: (918) 627-1111.

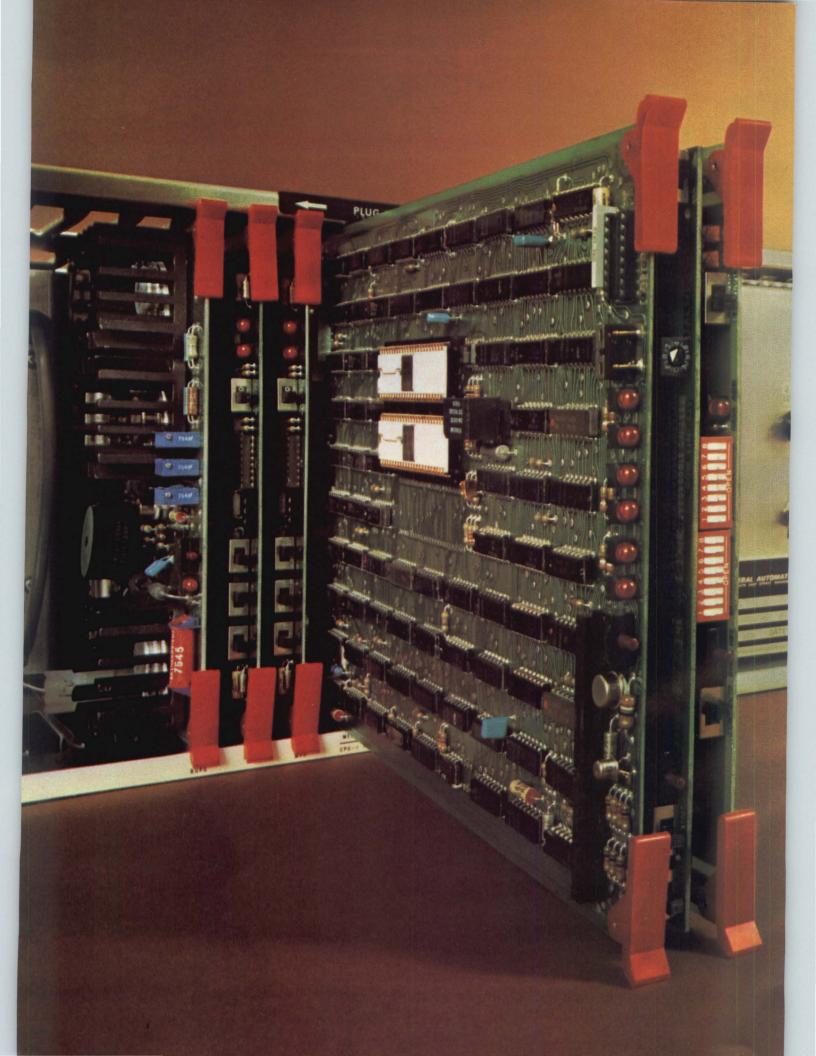


Tape drive miniaturization . . . in a big way.

CIRCLE 74 ON INQUIRY CARD

It went from 45 to 125 ips and 800 to 6250 bpi in 28 minutes flat.





## GA counts in microcomputing.

There's not a machine that can touch GA's 220. Not from DEC, Data General, or anywhere else.

- 1. The only  $\mu$ C with COBOL, FORTRAN and in-depth software support.
- 2. The only  $\mu$ C with a full file management system.
- 3. The only μC to offer OEMs a wide choice of operating systems: like FSOS, DBOS, RTX, RTOS.
- 4. The broadest  $\mu$ C instruction repertoire: speeds program development, conserves memory, accelerates execution.
- 5. The only  $\mu$ C that can handle big disks: I/O rate is 2.0 mB/second.

- **6. The fastest**  $\mu$ **C:** LDR/STR (indexed) 2.6  $\mu$ s.
- 7. The only μC with parity built-in: hardware test, verification, fault isolation, plus write protect.
- 8. The only  $\mu$ C with a back-up power supply built-in: protects semiconductor memory from power failures.
- 9. The only  $\mu$ C with boardlevel operator controls, switches and displays: in a microconsole.
- 10. The only  $\mu$ C with over 100 field-proven I/O controllers.

### **GENERAL AUTOMATION**

A big break for OEMs: family compatibility, throughout General Automation's extensive micro/mini line, gives GA-16/220 instant access to multiple batch and real-time operating systems, and to software off-the-shelf.

☐ Rush me full details on GA-capabilities.	-16/220 μC
☐ Contact me for immediate re	equirements.
Name	
Title	
Phone	Ext
Clip coupon to company letterl send to General Automation, 1 East Street, Anaheim, CA 928 (714) 778-4800.	.055 South

See us at NCC, Booth #2426.

## Datum the Intelligent Alternative for PDP-11 Disk Users

#### Price

- · Significant cost savings for OEMS and End users.
- Dollar for dollar Datum offers you the lowest possible cost per byte without sacrificing performance or dependability.

#### Dependability

- More than 9 years of designing and selling peripheral systems. Over 10,000 peripheral products installed, has made Datum the leading independent supplier of peripheral systems.
- With major service centers in the United States and Europe, Datum is prepared to service its products worldwide with direct factory trained personnel.
- Utilizes the same microprocessor technology used in our larger capacity disk systems.

#### Performance

- Complete Software & Media transparency to the DEC RK11
- Mix or Match Drive capacities at speeds of 1500 or 2400 RPM
- Single board design, occupying 1 SPC slot of a DD11-A (or equivalent) System Unit
- 34 byte data buffer
- Controls up to four 2.5, 5 or 10 megabyte disk drives
- Interfaces to drives manufactured by Diablo, Pertec, Western Dynex, Wangco, Caelus & DRI
- 11 reasons we want you to look at our disk products for your PDP11 computer.



SEE DATUM AT THE NATIONAL COMPUTER CONFERENCE—BOOTH #1647

Peripheral Products Division, 1363 South State College Boulevard, Anaheim, California 92806, Telephone: 714/533-6333, TWX: 910/592-1289, Telex: 68-5579
Mid West Sales, Des Plaines, II., (312) 296-1064 • East Coast Sales, Mountainside, N.J., (201) 654-5590 • District Sales, San Jose, Ca., (408) 249-5370
EUROPEAN HEADQUARTERS, DATUM ELECTRONICS, LTD., DATUM House, Cranford Lane, Harlington, Middlesex, England, Tel: 01-897-0456, TELEX: 935-398
CIRCLE 76 ON INQUIRY CARD

#### NCC PRODUCT REVIEW

Computer Design polled NCC '78 exhibitors of record to obtain advance information on products being exhibited for the first time at NCC '78 or which have only recently been announced. To the best of our knowledge, the following 46 products meet one or both of those requisites. However, because the copy deadline for this issue was so early in respect to the dates of NCC '78, many companies will display products on which they could not supply advance information.

#### MINIATURE DIGITAL CASSETTE RECORDER

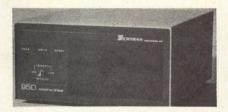


Complete bidirectional capability allowing backspace and bidirectional block search has been incorporated in the model 6409-21, an improved version of the company's 6409-11. An additional option, dual channel read/write, provides direct access to the entire storage media without physical handling of the mini data cassette. Data can be recorded in endless loop fashion by recording on 1 track in 1 direction to the

end of tape, then reversing tape direction and recording on the second track. Data transfer rate can be doubled by utilizing both data channels simultaneously. Models are compatible with proposed ANSI stds for mini data cassettes. Raymond Engineering, Inc, Raycorder Products Div, 217 Smith St, Middletown, CT 06457.

See at Booth 1101 Circle 410 on Inquiry Card

#### INTELLIGENT MINIDISKETTE SYSTEM



Over 200k char of storage are available with the 950 micro-disc, which incorporates a Shugart drive. RS-232 or 20-mA plug compatibility permits connection to timesharing and mini or microcomputer-based systems. Data can be recorded in either file or batch modes, with the system automatically entering file names into the directory and updating it for total random access. Single commands retrieve a specific file or all collected data. Microproces-

sor software is stored in resident memory; recording format is M<sup>2</sup>FM, soft-sectored, and self-initialized. Switch selectable data rates to 9600 baud supply fast online or offline operations. Binary mode provides for code transparent applications. **Techtran Industries**, **Inc**, 200 Commerce Dr, Rochester, NY 14623.

#### See at Booth 2751

Circle 411 on Inquiry Card

#### HARDWARE/SOFTWARE CRT TERMINAL SYSTEM



Previously unavailable in a self-contained desktop microprocessor-based workstation, hardware/software provided by the Microterm II terminal includes multitasking and ISAM. Running in a high performance hardware package, multitasking permits concurrent execution of communications functions, key entry operations, processing, and I/O jobs. A sort package reduces local batch functions to routine operations. ISAM allows fast access to diskette

data bases. Communications packages are available for emulated operation in either IBM 2780 batch or teleprinter interactive mode. Assembly and Extended Business BASIC languages are provided for interactive user programming from the keyboard. Digi-Log Systems, Inc, Babylon Rd, Horsham, PA 19044.

#### See at Booth 1465

Circle 412 on Inquiry Card

#### UNIVERSAL BASIC COMPILER

A high level language that can be compiled to run on 8080, 8085, 6800, and Z80 microprocessors, compiler package includes a high level debugger that allows program debugging without dealing directly with assembly language. Programs written in BASIC can be compiled for any of the processors, eliminating the need to rewrite programs when switching from one to another.

All std BASIC statements are included. Assembly language instructions can be intermixed in the BASIC program. Debugger allows users to set and clear breakpoints with statement numbers and display variables in memory using the variable name. Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045.

#### See at Booth 1235

Circle 413 on Inquiry Card

#### NOTE

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## Everything you need to

NORTH AMERICAN SALES OFFICES: Phoenix, AZ (602) 265-5261/Irvine, CA (714) 540-9945/Los Angeles, CA (213) 473-4581/Mountain View, CA (415) 968-3681/Orlando, FL (305) 859-7500/Schiller Park, IL (312) 671-4554/Indianapolis, IN (317) 842-3130/Wheaton, MD (301) 949-1664/Waltham, MA (617) 890-2654/Southfield, MI (313) 644-4944/Minneapolis, MN (612) 881-0190/South Plainfield, NJ (201) 757-2211/Albuquerque, NM (505) 294-5790/Dallas, TX (214) 387-0229/Olympia, WA (206) 866-2001/Toronto, Canada (416) 661-3711



## know about DEC peripherals:

Plessey offers a complete line of DEC compatible products. Reliability, quick delivery and substantial cost savings are some of the reasons to make Plessey your supplier. For complete price and delivery information, please contact the nearest listed sales office.

Plessey
Peripheral Systems

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#### NCC PRODUCT REVIEW

#### 600-LINE/MIN BAND PRINTER



Model B-600 uses a steel band font carrier, patented Mark V hammer system, custom IC hammer drivers, and microprogrammed control to produce 600-line/min throughput. Hammer is a single-mass, flex-pivot, voice-coil-actuated system which results from advances in magnet technology and hammer construction processes, and enables the use of reliable low power ICs as hammer drivers. A microprogrammed controller using bit-slice architecture simplifies control electronics

while providing spares commonality and increasing reliability. The printer uses a stepper motor paper feed system, and will handle industry std forms up to 6 parts, from 3 to 15" (7.6 to 38 cm) wide and up to 14" (35.6 cm) long. It prints at 6 or 8 lines/in (2.3 or 3.1/cm) and prints automatically to the bottom of the last form. **Dataproducts Corp**, 6219 De Soto Ave, Woodland Hills, CA 91364.

See at Booth 1562 Circle 414 on Inquiry Card

#### MULTIFUNCTION REMOTE INFORMATION SYSTEMS



Based on a multitasking model 85 attached applications processor (AAP) that performs high level language processing using interactive RPG II and COBOL, in conjunction with model 76, 78, 82, or Keybatch terminals systems, remote information systems enable users to perform batch communication, data entry, IBM 3270-compatible online file inquiry, standalone processing, and file management activities at sites remote from the host computer. Model 85

consists of control unit with 96k to 128k of main memory, 10M to 100M char of fixed and/or removable cartridge disc storage, and up to 15 CRT display stations located up to 2000 ft (610 m) from the processor. Peripherals can include up to 5 printers ranging from 62 to 1250 lines/min and magnetic tape drives. **Data 100 Corp**, 6110 Blue Circle Dr, Minneapolis, MN 55435.

See at Booth 2337 Circle 415 on Inquiry Card

#### DOUBLE-HEAD/DENSITY SMALL FLOPPY DISC DRIVE



The FD250 Microfloppy,  $^{TM}$  a double-head version of the 200, stores up to 437.5k bytes without operator intervention. Double-density, hard or soft sectoring, and write protect are std. The unit can write and read data on both sides of a diskette. Measuring 8 x 5.75 x 3.25" (20 x 14.6 x 8.3 cm), the drive weighs 3.2 lb (1.5 kg). Seek time is 25 ms track-to-track, with head settling time of 10 ms (last track addressed) and head loading time of 35

ms (max). Recommended recording mode is FM on single density and MFM on double density. Recording density (inside track) is 2768/5536 bits/in (1090/2180 bits/cm) with 1.75M (single density) and 3.5M bits/disc (double density), both unformatted. Pertec Computer Corp, Pertec Div, 9600 Irondale Ave, Chatsworth, CA 91311.

See at Booth 2103

Circle 416 on Inquiry Card

#### SERIAL INTERFACE MINI-FLOPPY DATA TERMINAL

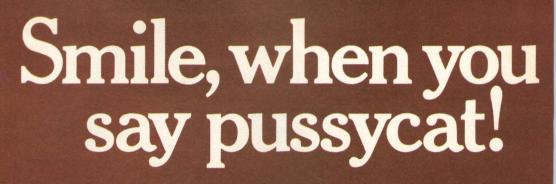


A fast access intelligent buffered data terminal, model 3901 uses a std 5.25" (13.34-cm) diskette drive and is RS-232-C compatible. Avg access time is 0.6 s. It has a fully editable data buffer holding up to 128 char, and block rewrite capability; blocks or entire paragraphs can be inserted into previously written text. Automatic high speed block search and verify capability can be controlled either by commands previously inserted in the data or initiated by the operator.

There are 30 simple ASCII commands; output consists of 13 plain English messages. Other features include storage of 143k bytes/diskette (formatted), switch-selectable asynchronous baud rates from 110 to 19,200, ASCII text as well as transparent binary modes, and auto-error check and retry. **Interdyne Co**, 14761 Califa St, Van Nuys, CA 91411.

See at Booth 2561

Circle 417 on Inquiry Card



Pussycat. Perkin-Elmer's \$795, 100 cps CRT Page Printer.

Pussycat. That's what we call our new 100 cps thermal printer, The Model 650 CRT Page Printer.

Pussycat. People who make 30 cps printers will think it's an incredibly funny name. Until they realize our meek little Model 650 is half the price of their machines, three times faster, and a whole lot quieter and easier to maintain.

In quantity 75, the Model 650 is only \$795 each. Which means you can buy a CRT and a Pussycat printer for what you're now paying for a printing terminal alone.

The Model 650 is fast. It prints an entire screen full of characters in 20 seconds. And, because it's the only printer in its class with a full-screen buffer, the Model 650 can free the CRT in 2 seconds or less. So the operator can go back to work while the printer is printing.

The Model 650 connects to any CRT terminal with an RS232 port-a Perkin-Elmer terminal or, perish the thought, someone

else's. No need to replace existing hardware or software.

And no need to worry about noise or maintenance. The Model 650 has only one moving part—the platen.

Check out The Pussycat from Perkin-

Elmer. It's a great little printer at a very reasonable price.

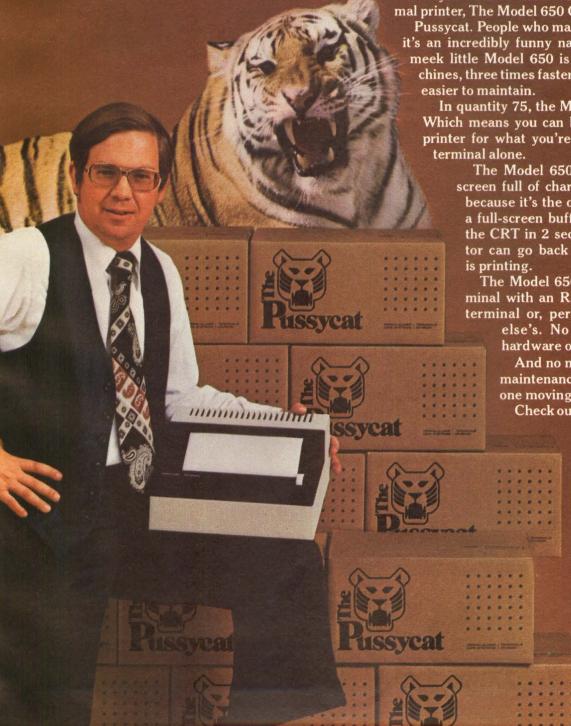
And, if you're one of our competitors...Smile, when you say pussycat!

For more information, write Perkin-Elmer Data Systems Sales and Service Division, 106 Apple Street, Tinton Falls, New Jersey 07724 or telephone toll-free 1-800-631-2154.

\*Quantity 75.

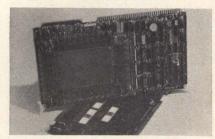
PERKIN-ELMER

CIRCLE 78 ON INQUIRY CARD



#### NCC PRODUCT REVIEW

#### MICROCOMPUTER 16k-BYTE CORE MEMORY



Fully compatible with SBC 80 single-board computers, MCM-8080 provides nonvolatile storage for 16,384 bytes and data access within 325 ns. Read and write cycle times are 780 and 1240 ns, respectively. Each board includes data save circuitry which detects input dc power conditions and inhibits operation when out of tolerance. A pin-compatible alternative to SBC 016, SBC 046, SBC 416, and MDS 016 boards used with Intel SBC 80/05, 80/10, and 80/20 or equivalent computers, memory

can be used to provide up to 64k addressable locations for either 8- or 16-bit applications. Board contains switches to select 16k contiguous addresses, eliminating the need to install or relocate jumpers. Measuring 12 x 6.75 x 0.50" (30.48 x 17.14 x 1.27 cm), board occupies 1 card slot in Intel or equivalent card rack. Ampex Corp, 200 N Nash St, El Segundo, CA 90245.

See at Booth 4113

Circle 418 on Inquiry Card

#### ALTERNATE TIME BASE DISPLAY OSCILLOSCOPE



A 100-MHz, 5-mV (2 mV at 35 MHz) dual trace, general-purpose oscilloscope weighing 9.6 kg is suited to field use, handling most measurement problems, including those in advanced electronics environments. PM3262 features an alternate time base display facility of the complete signal and magnified detail over the full screen width. A third channel provides simultaneous viewing of trigger impulses. Operation is simplified with composite triggering;

due to 50-mV to 24-V dynamic range, the unit accepts most trigger inputs. CRT has a brighter display and high writing speeds. Double-insulated power supply eliminates ground loop problems and measurement inaccuracies caused by hum or other spurious signals. Unit also has a high tolerance to line noise. Philips Test & Measuring Instruments, Inc, 85 McKee Dr, Mahwah, NJ 07430. See at Booth 2163

Circle 419 on Inquiry Card

#### VECTOR PROCESSOR TO PLOTTER INTERFACE

A multiple microprocessor-based intelligent interface, vector processor performs functions formerly assigned to host computer or dedicated minicomputer. It converts vectors describing a plot into raster data acceptable by electrostatic plotter, significantly reducing host computer resource requirements. One microprocessor con-

trols input of data to the device; the second performs vector to raster conversion at speeds approximating those of large mainframes. A third microprocessor reads data from the other raster buffer and outputs it to the plotter. The output microprocessor also performs plotter control and status functions. **Gould Inc, Instruments Div,** 3631 Perkins Ave, Cleveland, OH 44114.

See at Booth 1107

Circle 420 on Inquiry Card

#### NOTE

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#### MINICOMPUTER-BASED HARD DISC BUSINESS SYSTEMS



Two Link 200 family models use a disc with 60% faster throughput, accomplished by design of a drive which rotates at 2400 r/min. Hardware and software compatible with the rest of the company's Link computers, a std model 240 has 32k bytes of storage, 1 CRT terminal, and a 110-char/s printer. Up to 5 users can be handled simultaneously. Link 250 uses the company's RTOS II partitioned operating system offering up to 10 users exclusive ac-

cess to their data. Internal storage capacity is from 64k to 128k bytes. Battery backup, 3 CRT terminals, and a 110-char/s printer are std. Also offered are the Link 540 and 550 systems, with 110-char/s printers. The 540 has a 50M-char drive, 1 CRT terminal, and RTOS I; the 550 has 3 terminals and RTOS II. Randal Data Systems, Inc, 365 Maple Ave, Torrance, CA 90503.

See at Booth 2464

Circle 421 on Inquiry Card

## Rare bird.

#### An editing CRT that's ideal for transaction processing.

Lower software costs. Easier programming.

System builders say our Model 1200 Editing Terminal is ideal for transaction processing. We agree.

The Model 1200 makes programming easier because it tells the programmer (and the host computer) the status at the terminal. Communications strap setting, printer errors, operator mode key setting, and more.

The Model 1200 also cuts down on host computer loading by automatically setting modified data "tags," whenever a field is updated, so the host computer can request only modified fields, and skip thousands of needless compare operations.

> To further lighten the load on the host computer, the Model 1200 has programmable send keys that let the program regulate the amount of data returned to the computer as terminal loading varies.

More productive operators.

Thanks to a 9 x 12 character matrix, the Model 1200 has crisp, clear, strikingly sharp characters. So operators see their work better and make fewer mistakes. Data entry is incredibly accurate due to field attributes like low intensity, numeric only, blink, and inverse video.

Editing is fast and easy, too. Single keystrokes insert and delete characters

All our standard goodies. Only \$1383.\*

A big, 12-inch screen, 128-character ASCII set, upper and lower case, 15 cps Typamatic repeat on all keys, and a 24-line display are standard. So is our exclusive No Hassle toll-free 800 number for service. One call gets you service. Where you need it. When you need it. World-wide.

So go ahead. Get a CRT terminal that's specifically designed for transaction processing. Perkin-Elmer's Model 1200 Editing Terminal.

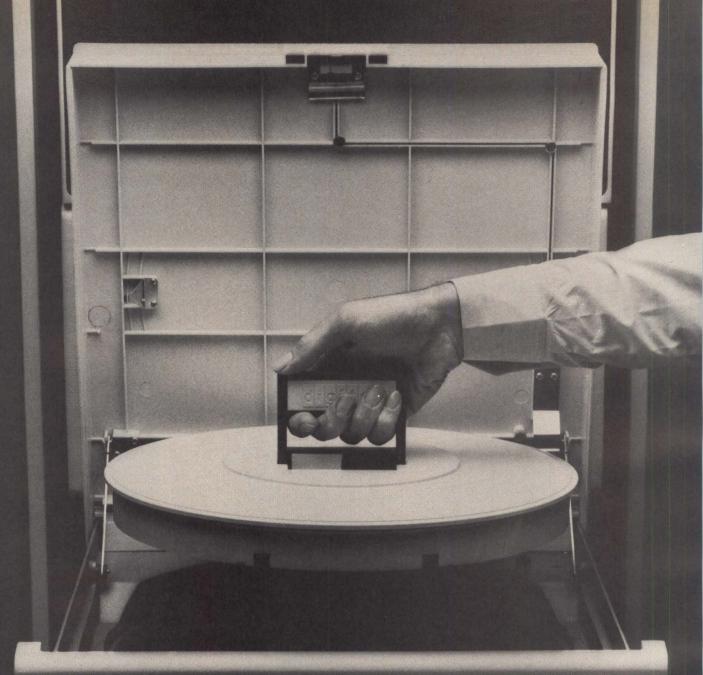
For more information, write Perkin-Elmer Data Systems Sales and Service Division, 106 Apple Street, Tinton Falls, New Jersey 07724 or telephone toll-free 1-800-631-2154.

CIRCLE 79 ON INQUIRY CARD

PERKIN-ELMER

**Data Systems** 





INTRODUCING EVERYTHING OEMs WANT IN A 5Mb DISK.

### PLUS EVERYTHING THEY WANT IT IN.

#### The new RL01 5Mb disk.

Introducing a top-load, rack mountable, low priced 5.2Mb disk with state-of-the-art performance and solid OEM reliability.

The RL01 features 512Kb per second transfer rate.

Plus an incredibly simple design. There's no back plane. And just 5 elec-

tronic modules. So it's super reliable and easy to spare.

The RL01 is simple to service, too. All maintenance is done from the top of the unit. The heads can be changed in minutes, not hours. There's even a universal power supply with a frequency range of 47.5-63 Hz that can be quickly (but not accidentally) switched between 100-127V and 200-254V. And it can be replaced with just four screws without disturbing heads or logic.

The RL01 is also easy to configure. Our one board controller can power

four drives for up to 20.8Mb.

Our RL01 is so good, you probably won't want a system without one. So we're offering those, too.

Incredibly priced new packaged systems, starting at just \$18,000.

Here's what you get: a PDP-11 CPU with 64 Kb of main memory, clock, serial line interface, cabinet, 10Mb of RL01 capacity with controller, an LA-36 terminal, and our RT-11 operating system.

You can get a PDP-11/03 based system for just \$18,000, PDP-11/04 based for just \$21,000, and the PDP-11/34 based one in the picture for just \$25,500. And prices go even lower with our OEM discounts.

The new RL01 disk and new PDP-11/RL01 packaged systems.

They're the systems you've always wanted.

Which is just what you'd expect from the OEM Group at Digital.

Call or write: Digital Equipment Corporation, PK3/M-86, Maynard, MA 01754. (617) 493-4237. In Europe: 12 av. des Morgines, 1213 Petit-Lancy/Geneva. Tel. 93 33 11. In Canada: Digital Equipment of Canada, Ltd.





#### NCC PRODUCT REVIEW

#### CONTROLLER/TAPE SYSTEMS FOR IBM SERIES/1



Consisting of a controller, universal users adapter, and as many as 4 tape transports, the 5191 is a complete online operational tape subsystem that conforms to requirements of IBM Series/1 computer. Controller can accommodate as many as 4 transports with speeds of 12.5 to 125 in/s (31.75 to 317.5 cm/s). It will handle 7- or 9-track tape formats in densities of 200, 556, 800, and 1600 bytes/in (78, 218, 314, and 629/cm). Controller reads or writes to one transport at a time, inter-

facing with the computer through the users adapter. A 64-byte read/write buffer eliminates a variety of timing restrictions on the CPU I/O bus, and quartz-crystal-generated timing eliminates adjustments. A 64-bit skew buffer/channel allows PE tapes to be read. Datum Inc, Peripheral Products Div, 1363 S State College Blvd, Anaheim, CA 92806.

#### See at Booth 1647

Circle 422 on Inquiry Card

#### IN-CIRCUIT AUTOMATED TEST SYSTEMS

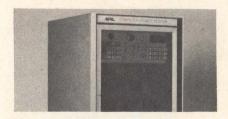


MICA 5000 provides a componentoriented language for automated test program generation, along with simple operator command structure, clear concise rework information, and an extensive library of component descriptions for testing digital circuits. The unit performs truth table testing as much as 10 times faster than competitive products as the result of its ability to simultaneously scan output from multiple pins. It incorporates a 16-bit Naked Mini processor, 32k words of memory, integrated alphanumeric CRT display, programming keyboard, operator's console, repair message printer, 256k-byte floppy disc, and full system software. A fully-enclosed vacuum system for bed of nails fixturing is std. Unit is prewired for 640 pins; expansion to 1024 and 1408 pins are options. Computer Automation, Inc, 18651 Von Karman, Irvine, CA 92713.

#### See at Booth 2436

Circle 423 on Inquiry Card

#### COMPUTER SYSTEM CENTRAL POWER SUPPLY



Computer Power Center provides a central node for power distribution to computer system and establishes a single-point ground. Programmed to provide proper voltages and currents, it isolates all computer equipment from spurious signals in building wiring, and turns off equipment in case of safety hazard. When changes are necessary, it can be reprogrammed or moved. Std models range from 15 to 200 kVA, and can

accept input voltages of from 208 to 600 Vac. Power is fed to an electrostatically-shielded, computer-grade isolation transformer to adjust for voltage variation. Output voltages can be specified from 120 to 240 Vac. Up to 126 1- $\phi$  or 42 3- $\phi$  lines can be run from the center. **Emergency Power Engineering**, 2919 S Halladay, Santa Ana, CA 92705. **See at Booth 4021** 

Circle 424 on Inquiry Card

#### COMPUTER TERMINAL WITH AUDIO INPUT/OUTPUT

A microprocessor-based, isolated-word voice recognition/response system, MIKE<sup>TM</sup> can be trained to recognize 16 commands, repeat the command or respond to it orally for confirmation, and to react to commands by generating signals that can be used to enter data or control equipment. Unit can operate as a remote computer terminal via RS-232-C serial interface, or can be connected directly to a computer

for voice data entry, file inquiry, or control applications. Voice recognition circuits are contained on 4 PC cards, an additional card houses the interface. With audio response feature, sound segments are recorded as the system is trained. 16 such segments, each representing 0.5-s of speech and corresponding to 1 of the 16 commands, can be recorded. Centigram Corp, 1294 Hammerwood Ave, Sunnyvale, CA 94086.

See at Booth 1566 Circle 425 on Inquiry Card

#### 90-DEG PRINTER TRACTOR

For low profile printers, model 1040-90 feeds forms along a right angle path, overcoming the problem of misregistration of multipart forms encountered with sprocket-fed pin wheel systems. An optional guide bar provides continuous guiding of cardstock [at slew speeds up to 30 in (76 cm)/s], without interfering with horizontal tractor adjustment. Precision Handling Devices, Inc, 63 S Main St, Assonet, MA 02702. See at Booth 4016

Circle 426 on Inquiry Card



## The soft terminal. Designed to be redesigned.

Chances are, the intelligent terminal you really need doesn't exist yet.

That's why we build the Conrac 480, The Soft

Terminal. It's designed to be redesigned by your software to fit your system like a glove.

#### Flexible hardware to start you off.

Most CRT terminals are built around one large circuit board, which doesn't leave you much flexibility.

The Conrac 480, on the other hand, offers you the benefits of a clean bus architecture. Plug in four cards, and get a basic working terminal. Plug in up to twelve additional cards, and get some real power. Cards like RAM up to

48K bytes, PROM up to 16K bytes, and interfaces to floppy disk drives, printers and other peripherals.

#### Software to make it happen.

Do you need a special keyboard, character set, or set of terminal attributes? No problem. Just plug in a special PROM.

With the proper MPU software, the Conrac 480 can be configured as a polling terminal or as a powerful microcomputer. Or as anything in between. This software can reside in

PROM, or can be downloaded into RAM from a host computer or from disk.

Many software modules are available off-the-shelf,

like a basic editing package, and protocol handlers for IBM, Burroughs, and

Univac. More are on the way.
To make microprogramming
easy, you can use the AMI 6800
Microcomputer Development
Center software, which runs
perfectly on our terminal.
That's power!

#### Attractive outside as well as inside.

Any way you look at it, the Conrac 480 is attractive. The basic version is only 20" deep and fits where space is limited. Its understated

modern styling blends into virtually any decor. And you can have your own color and texture.

Operators love the feel of our long-life capacitive keyboard with sculptured keys. And our sharp and stable CRT display. As a matter of fact, we're known worldwide as the manufacturer of professional video monitors.

Write to us or give us a call for more facts.

We'll send you a comprehensive 12-page brochure on The Soft Terminal. And we promise not to use "hard sell."



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Telephone (213) 966-3511; Telex 670437

**EUROPEAN SALES** 

Conrac GmbH, Industriestrasse 18, D-6992 Weikersheim, W. Germany Telephone (07934) 675, Telex 74250

#### NCC PRODUCT REVIEW

#### INTELLIGENT DISKETTE CONTROLLER



Compatible with IBM diskette 2D and 3740 formats and the S-100 bus, standalone model 1170 is a Z80-based double-density controller that can manage single- (FM) or double-density (MFM) recording on as many as 32 diskette sides for a total capacity of 16M bytes. Basically a 1-board computer for diskette subsystem management and microcomputer uses, the unit has a microprocessor that communicates by file name and assumes house-keeping functions usually performed by

the CPU, minimizing its software burden. File management functions are resident in firmware. The controller supports up to 8 model 299 4-headed drives at once, and can handle 2 model 277 dual diskette drives or combinations of models 299 and 277. An RS-232 interface is optional. **PerSci, Inc,** 12210 Nebraska Ave, West Los Angeles, CA 90025.

See at Booth 1239

Circle 427 on Inquiry Card

#### RESOURCE SHARING FOR DISTRIBUTED NETWORKS

Sycorlink provides for linking of multiple processors and for sharing of all disc files and peripherals in a network, allowing model 405 distributed processing systems to be combined to create individual processing centers of exact capacity. Networks can communicate in either asynchronous, binary synchronous, or SDLC mode. Link consists of a microprocessor-based hardware con-

troller, which handles network protocol and insures data integrity by providing automatic error checking and recovery, and a configurable system software module, which provides automatic services necessary to connect dataset access methods of home node to those of other nodes in the network. **Sycor Inc**, 100 Phoenix Dr, Ann Arbor, MI 48104.

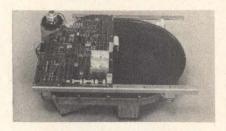
#### See at Booth 2420

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#### NOTE

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#### SINGLE-PLATTER RIGID DISC DRIVE



Marksman is a 17M-byte, single-platter Winchester technology disc drive that uses floppy disc techniques for low cost. No preventive maintenance is required and the drive is designed to exceed 8000-h MTBF. A stepper motor driven band positioner is used to achieve low cost. An integral microprocessor allows the motor to slew at high speed with controlled acceleration, providing a significant increase in performance. Data transfer rate is 12 times that of a double density floppy

disc; 10 times the data can be accessed in one-half the time. Avg access time is 80 ms, track to track is 3 ms, and avg latency is 12.5 ms. Unit is power supply compatible with floppy disc systems and has provision for mounting by customer designed formatters and controllers. California Computer Products, Inc, 2411 W LaPalma Ave, Anaheim, CA 92801.

#### See at Booth 2408

Circle 429 on Inquiry Card

#### SINGLE- AND TRIPLE-OUTPUT SWITCHING POWER SUPPLIES



High performance switching-regulated supplies designed for minicomputers, microcomputer systems, and peripherals, Sub-Modular Switchers are based on use of LSI control circuits mounted on PC boards to form std modular sub-assemblies. Each subassembly performs separate, distinct functions within the supply itself. Subassemblies are interconnected by means of a backplane strip similar to those used to link memory, CPU, and interface boards within a

minicomputer chassis. Units have min holdover storage specified at 40 ms; holdover times of >60 ms are typical. Ripple is held to 5 mV rms max through use of low ESR capacitors with pk-pk high frequency noise typically <30 mV. Transient response is <500  $\mu s$  for a 50% load step; regulation is 0.1%. ACDC Electronics, 401 Jones Rd, Oceanside, CA 92054.

#### See at Booth 2660

Circle 430 on Inquiry Card

### FOR RENT...NOW...

Beehive's versatile and easy-to-use BlOO and Mini Bee 2 terminals, both available for immediate short-term, low cost rentals today.

If you need a self-contained, feature-filled video display terminal fast, the B100 will fill the bill . . . and it's available today. Beehive International's B100 features both RS232C or current loop interface, has switch selectable transmission rates from 75 to 19,200 bps, and includes cursor control. You'll also like the addressable cursor. The terminal has an easy-to-read 12-inch non-glare screen which is formatted to display 24 lines with 80 characters per line. You can choose upper and lower case characters, too. The B100 has a total page memory of 1920 characters, and the 82-key, ANSI compatible keyboard features auto repeat, 2-key rollover and alpha lock. The addressable cursor lets you directly position by line and column, and an erase mode allows you to erase from cursor to end of line, from cursor to end of memory, and clear. You'll also find operation more efficient because of B100's 11-key numeric pad with decimal and additional function keys. Communications mode is Full Duplex (Echoplex), Half Duplex, and Block (asynchronous 10 or 11-bit word). It's ready for you now.

The low-rental rates on Mini Bee 2 will make you happy if you need a TTY-compatible terminal with cursor control and a detachable keyboard. Beehive's Mini Bee 2 is a stand-alone, operator/computer accessible remote display terminal with a detachable keyboard. You use Mini Bee 2 to transmit and receive data serially through an RS232C interface at any of several preselected transmission rates to a maximum of 9600 baud. Mini Bee 2 has a 12" rectangular monitor which displays 25 lines with 80 characters per line. It has a total page memory of 2000 characters, and each character is generated from a 5x7 dot matrix with two dot spacing between adjoining characters. Communications mode can be full duplex, half duplex, 10 or 11-bit asynchronous word. Mini Bee 2 also features character-by-character transmission, an escape sequence mode for unique CRT functions, and an erase mode. It's also available off-the-shelf from REI immediately.

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Tell me more about B100 and Mini B2 now! Call me at. Send me a copy of your free illustrated Rental Catalog. ☐ I might be interested in buying—on a money-back guarantee basis - some of your late-model, well-maintained "previously owned" equipment. Please send me your Equipment Sales Catalog. ☐ I have a pressing need right now for the following: Please phone me immediately at\_ NAME. COMPANY\_ ADDRESS\_ PHONE NUMBER\_ Complete this coupon and return it today to REI, 19347 Londelius St., Northridge, CA 91324. GSA #GS-04S-21963 Neg © 1978 Rental Electronics, Inc.

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#### NCC PRODUCT REVIEW

#### 75-IN/s MAGNETIC TAPE TRANSPORT

Using tension arm buffering for compactness, transport mounts 10.5" (26.6-cm) reels in a std 19 x 24" (48- x 61-cm) rack space and extends only 10.8" (27.6 cm) behind the front panel. It weighs only 90 lb (40.5 kg) and uses a max of 400 W, compared with up to 1000 W for vacuum drives. Absence of vacuum motors or drive belts results in long MTBF while freedom from vacuum

restrictions widens the environmental envelope to 20,000 ft (6080 m) and 2 to 50 °C. Capable of controlling up to 4 tape drives in any combination of 2 speeds, 9- or 7-track recording, 1600- or 800-bit/in density, an imbedded dual formatter provides microprocessor direction of write, read, and control functions. **Digi-Data Corp**, 8580 Dorsey Run Rd, Jessup, MD 20794.

#### See at Booth 4323

Circle 431 on Inquiry Card

#### NOTE

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#### 6300-CHAR RASTER SCAN CRT DISPLAY MODULE



High char density/graphics display is supplied by the M4408 15" (38-cm) module for word and data processing systems. Capable of displaying over 6300 u/lc char, green on black background, the unit can be mounted vertically to display 96 char x 66 rows, or horizontally for 132 char x 48 rows. Horizontal scanning frequencies are 28.5 to 32.5 kHz, 50 or 60 Hz vertical. TTL level separate sync input signals are accepted. Power required is 55 Vdc at

1.2 A. Dual 50-MHz video amps and a 10-mil spot size provide required bandwidth and resolution; 2-axis dynamic focus maintains optimal corner focus. Complete reverse video capability and 4 levels of video output for variable intensity highlights are also included. **Motorola, Inc, Data Products,** 455 E North Ave, Carol Stream, IL 60187.

#### See at Booth 1818

Circle 432 on Inquiry Card

#### 500k-BYTE/SIDE DUAL FLOPPY DISC DRIVE



A dual-drive floppy disc that incorporates an intelligent controller to facilitate interface to any 8- or 16-bit host computer, the 1055 uses GCR technique to record 500k bytes (formatted) on one surface of a 5.25" (13.34-cm) diskette. Dual drive configuration provides nearly 1M bytes of usable file space. A microprocessor-based controller performs data formatting, encoding and decoding, sector buffering, error detection and recovery, and gen-

eral housekeeping duties. Select capability permits 4 drives to be connected to a common host interface. In buffered mode with automatic error recovery, transfer rate is 32k bytes/s; direct mode has a throughput of 38k bytes/s. Micropolis Corp, 7959 Deering Ave, Canoga Park, CA 91304.

#### See at Booth 4443

Circle 433 on Inquiry Card

#### PERSONAL COMPUTING SYSTEM

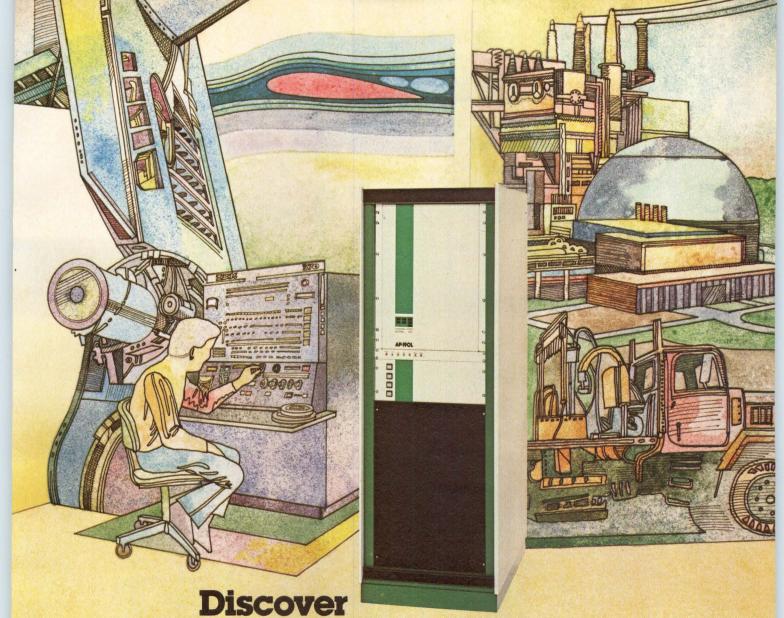


Compucolor II has 8-color, 13" (33-cm) diag display, typewriter-like keyboard with extra function keys, 24k memory, 8080A CPU, and built-in mini-floppy drive mass storage device. It uses BASIC 8001, a conversational programming language with English-type statements and familiar mathematical notations. Internal EPROM/ROM provides up to 16k bytes of nondestructive storage. Memory sockets are provided for 16k bytes of additional EPROM/ROM, which includes Disc BASIC 8001,

file control system, and terminal software. 4k bytes of RAM are incorporated for screen refresh and scratchpad; 4k bytes of user workspace are expandable with up to 12k additional RAM. System is designed for 512 ports; 25 ports are implemented in std unit. RS-232-C serial asynchronous channel for printer or modem is optional. Compucolor Corp, PO Box 569, Nor-Cross, GA 30091.

#### See at Booth 79

Circle 434 on Inquiry Card



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The key to unequalled systems solutions for scientific processing is available from FPS for users of large computers such as IBM 360/370 and Univac 1100 Series.

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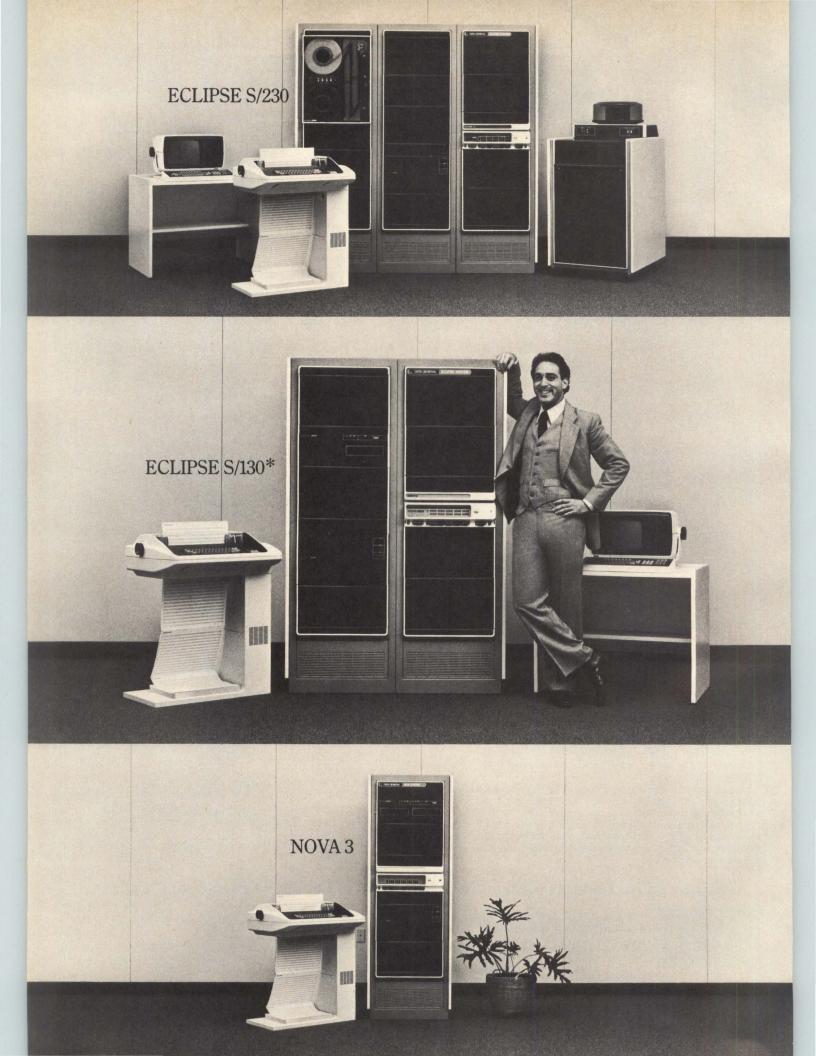
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The ECLIPSE S/130 computer system proves it is still possible to make ends meet. Its performance, on the one hand, approaches that of our super high-speed ECLIPSE S/230. While its price is much closer to the

level of our best-selling NOVA 3.

The ECLIPSE S/130 is built around the same powerful architecture as the ECLIPSE S/230. But it has its own unique character. Like our fast micro-coded floating point, efficient character string instruction set, our second-generation WCS microprogramming ability, as well as AOS, our heuristic multiprogramming advanced operating system.

All of which means that even though the ECLIPSE S/130 is in the middle of our family, it's in a class by itself when it comes to performance, features, and power for the money. And if you still think that value is a virtue, the ECLIPSE S/130 system won't let you down. Call (617) 366-8911, Ext. 4735 or write.

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\*The ECLIPSE S/130 System shown includes 128K bytes of memory, floating point instruction set, clock, Dasher\* terminal printer and display, 10 megabyte fixed/removable cartridge disc, 315K byte diskette, and all applicable controls, cabinetry, and cabling. Licensed software available on this configuration are RDOS, FORTRAN IV, optimizing FORTRAN V, and BASIC. Domestic U.S. list price \$42,040, including licensed software. OEM and volume discounts available.

Data General Corporation, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario. Data General Europe, 61 rue de Courcelles, Paris, France, 766.51.78. Data General Australia, (03) 82-1361. Data General Ltda., Sao Paulo, Brazil, 543-0138 © Data General Corporation, 1978. ECLIPSE is a registered trademark of the Data General Corporation.

# NCC PRODUCT REVIEW

## 16k x 18 ADD-IN CORE MEMORY FOR LSI-11



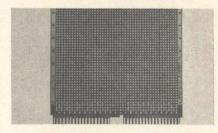
DR-115, for use with DEC's LSI-11, LSI-11/2, and PDP-11/03, is packaged on one std DEC quad board. Organization is 8k x 18 or 16k x 18. The 18-bit word length allows either parity or nonparity operation. Access and cycle times are 425 ns and 1.15  $\mu$ s, respectively. The memory operates on 5 and 12 V. A DIP switch is provided for address strapping. Operating modes are read/restore, clear/write, read/modify/write, and byte. The 8k or 16k stack used is

mounted via pluggable pins on the solder side of the system's electronics board. Because of the stack positioning, the memory occupies two card slots in the LSI-11, even though only one row of connectors is used for interfacing to the computer. **Dataram Corp**, Princeton-Hightstown Rd, Cranbury, NJ 08512.

## See at Booth 2543

Circle 435 on Inquiry Card

# PROTOTYPING BOARD FOR DEC AND HEATH COMPUTERS



A general-purpose board permitting construction of custom interface circuits for Heath H-11 microcomputers and DEC LSI-11, PDP-8, and PDP-11 series minicomputers, the 4607 Plugbord measures 8.430 x 5.187 x 0.062" (21.4 x 13.17 x 0.16 cm). It is form, size, and connector compatible with the DEC "double-height, extended-length" module. Etched contacts are spaced to fit the 2 18/36 pin connectors used in the computers. Board has an array of 0.042" (0.106-cm) dia holes on 0.1"

(0.254-cm) centers; DIP sockets of any size or discrete components may be placed anywhere on the board. Boards are blue, epoxy-glass composite material with 2-oz (57-g) copper cladding; pin terminations and edge strips are hot-solder plated; and card edge contacts are gold-flashed nickel plate. Vector Electronic Co Inc, 12460 Gladstone Ave, Sylmar, CA 91342.

## See at Booth 84

Circle 436 on Inquiry Card

## MICROPROCESSOR-BASED MULTIPORT MODEMS



A series of modems operating at 9600, 7200, and 4800 bits/s reduce equalization time to 30 ms, permitting operation in 9600-bit/s multidrop data communications networks. Models are available with automatic port allocation to maximize data channel usage. A 9600-bit/s modem can transmit data between up to 4 terminals simultaneously over the same data channel at 2400 bits/s. If a terminal goes offline, the modem continues to use the full 9600-bit/s

transmission capacity by automatically reassigning the unused channel capacity to the primary port. Units can be equipped with built-in modem sharing devices to allow multiple terminals to share a single modem or modem port. Status and test indicators and test features are built-in. Remote test is optional. Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166.

## See at Booth 1611

Circle 437 on Inquiry Card

## QUAD-DENSITY DATA CARTRIDGE

Providing 4 times the data storage capacity of a std 0.25" (0.63-cm) data cartridge in the same package, the TC 4000 stores approximately 10M bytes of data (formatted) or 11.5M bytes (unformatted), making it suitable as back-up storage for post-Winchester generation fixed-disc drives. Tape has a special oxide formulation which allows reliable operation at 6400-bit/in (2520/cm) density. Cartridges are compatible

with std ANSI, ECMA 0.25" (0.635-cm) cartridge drives. The D<sup>a</sup> Minidisk, a 5.25" (13.34-cm) dia double-sided, double-density diskette has capacity for 0.6M to 1.0M bytes, depending on formatting. It is compatible with Shugart and other dual-head drives, and is available in soft, 10-, or 16-sector versions. Information Terminals Corp, 323 Soquel Way, Sunnyvale, CA 94086.

## See at Booth 1364

Circle 438 on Inquiry Card

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RELIABLE. The Megabyte Memory contains one megabyte of reliable, non-volatile core memory on each pluggable pc module. Two versions are available, 1024K x 8 & 1088K x 8. COST EFFECTIVE. The Megabyte Memory is priced at less than 0.1¢ per bit in OEM quantities. LOW POWER. While operating at a 2 microsecond cycle time the Megabyte Memory consumes only 12.00 microwatts per bit; standby power is 3.4 microwatts per bit. The system

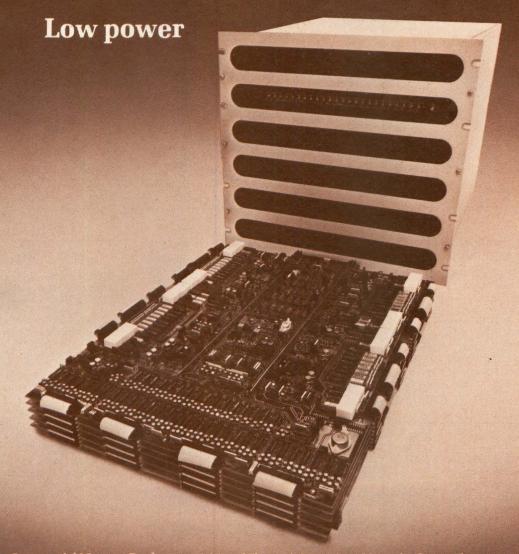
chassis can accommodate up to four Megabyte modules, two logic cards and a power supply. General purpose I/O cards or custom interfaces are available to meet most OEM applications. Call or write us today for complete technical information.

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145

# NCC PRODUCT REVIEW

## 300-BIT/s FULL-DUPLEX MODEMS



VA355 series of low profile standalone modems are designed for remote terminal uses requiring 300-bit/s full-duplex operation over switched networks or 2-wire leased lines. Registered for direct connect under FCC Rules, Part 68, the series includes VA355 P for direct connect to voice or data jack, S for direct connect to data jack only, and G for 2-wire leased line (point-to-point or multipoint). The crystal-controlled units use CMOS circuits for min power consumption. Com-

pact power supply is located at the ac plug to reduce heat within the modem itself. Compatible with major timesharing services, the devices are direct replacements for Bell 103/113. Originate/answer, diagnostic interface display, and local analog and digital loopbacks are also featured. **The Vadic Corp**, 222 Caspian Dr, Sunnyvale, CA 94086.

## See at Booth 2141

Circle 439 on Inquiry Card

## MAGNETIC CARD READER/ENCODER



Series LC-31 Gameloader<sup>TM</sup> conveniently loads programs for home/hobby computers. Programming/data storage media holding 1k 8-bit bytes is the company's 4-stripe Kilobyte Card.<sup>TM</sup> An enclosed strobe controlled PC/LED/shaft encoder provides data accuracy independent of head speed. A 2-channel R/W type head provides recording densities of 420 bits/in (165/cm) on the card, with typ ISO/ANSI-std 2.81" (7.14-cm) track length. Char load time is 5k bytes/min. Read speed is 3.1"

(7.9 cm)/s, with R/W cycle time of 5 s/stripe. Power required is 12 Vdc, at 350 mA max. Design includes 1 full track of I/O buffering, F8 microprocessor control with ROM and RAM, plus magnetically shielded and electrically suppressed drive motor. Interface configurations are RS-232, EIA; TTY; and byte parallel. **Vertel, Inc,** 125 Ellsworth St, Clifton, NJ 07012.

## See at Booth 1856

Circle 440 on Inquiry Card

# REMOTE BATCH SYSTEM FOR ELECTROSTATIC PRINTING

Emulating IBM 2780/3780 data communications terminals, RSVP™ (remote spooling vector processor) for the IBM 360/370 uses IBM bisync protocol and EBCDIC code. It carries its own self-test, line trace, and dump capabilities. The system converts vectors to rasters, and routes jobs to multiple electrostatic printer/plotters and/or mag tape. Dial-up or leased

line communications occur at 2400 to 9600 baud. Local operation supports tape to printer/plotter, card to tape, and card to printer. System components include a vector processor with operator panel and display, mag tape deck, card reader, and up to 4 combinations of printers and plotters. Versatec, a Xerox Co, 2805 Bowers Ave, Santa Clara, CA 95051.

## See at Booth 1463

Circle 441 on Inquiry Card

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## MICROPROCESSOR KEYBOARD WITH REED SWITCHES

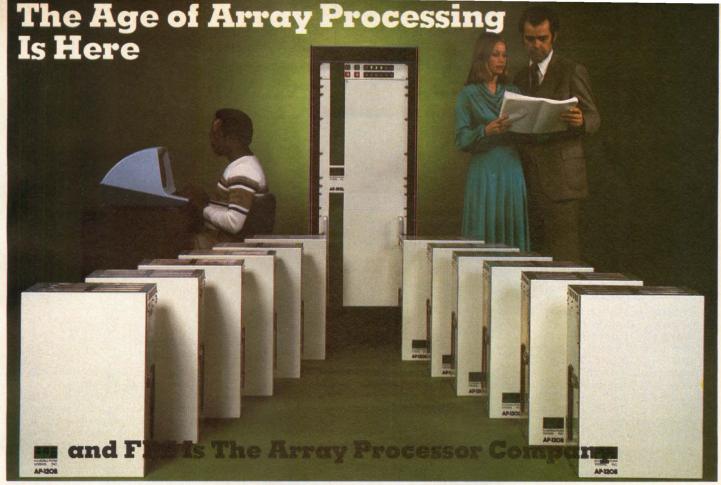


Full function programmable keyboard uses a single-chip 8-bit microprocessor that incorporates ROM and RAM, as well as an erasable p/ROM, which enables complete software control of all key functions. Microprocessor also permits automatic repeats, multiple programming of a single board, program changes in the field, serial and/or parallel I/O, and n-key rollover (3-key rollover is std). Reed keyswitches are low profile, measuring 1.03125" (0.793

cm) from base to key top, and are sealed against dust, humidity, and hostile environments. They require low operating power and have 0 power drain. Life expectancy is 100M operations. Keytops are nonglare, double-shot molded, and color controlled. Legends are sharp and clear. C. P. Clare & Co, 3101 W Pratt Ave, Chicago, IL 60645.

## See at Booth 125

Circle 442 on Inquiry Card



The AP-120B
ARRAY PROCESSOR COMPUTER
Interfaces to all popular minicomputers . . . a typical AP-120B complete is less than \$50K.

The AP-190L
ARRAY PROCESSOR COMPUTER
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1100, Sigma 5-9, and DEC System 10
. . . a typical AP-190L System is less
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More than 500 FPS Array Processor computers are in use worldwide, providing their users with the computational power of large, mega-dollar scientific computers at greater reliability, greater applicability, easier programmability, and at a small fraction of the cost.

A typical minicomputer/FPS Array Processor system (such as a PDP 11/34 and AP-120B) provides a computational throughput

for scientific and signal processing algorithms that is on the order of **two hundred times greater** than the throughput of the mini alone.

A large computer/FPS Array Processor system allows heavy data processing, which would severely load the host CPU, to be off-loaded to the AP-190L for efficient processing while the host CPU is utilized for tasks more appropriate to its architecture and operating system.

The unique, efficient instruction set and complementary architecture of FPS Array Processor computers are specifically designed to accommodate the vector and matrix algorithms for scientific data processing. High processing speeds result from the seven independent data paths that move operands synchronously to and from the 38-bit floating-point arithmetic units, accumulators, and multiple memories. This inherent simplicity allows FPS Array Processors to be readily simulated on the host or frontend computers for program development. It allows FPS to provide you with a large volume Scientific Math Library (more than 200 functions) and additional volumes for Signal Processing and other special operations. And it allows you to program FPS Array Processors so you can create your own special, unique, or proprietary functions.

FPS Array Processor computers offer high reliability (much more than your present computer) and compactness (only slightly larger than minicomputers). They are found in research, shipboard, airborne, and mobile installations, as well as computer rooms throughout the world.

### FAST

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The following algorithms are memory to memory
2.7ms 1024 pt real FFT
26.1ms 8192 pt real FFT
1.55s 512 x 512 real 2D FFT
10.2ms 20 x 20 matrix inverse

## EASY PROGRAMMING

The power of FPS Array Processors is easily called through FORTRAN subroutines resident in the host or front-end minicomputer. A Vector Function Chainer permits routines to be chained together for a single call, reducing host overhead. Extensive documentation and a simulator/debugger help you create new routines.

### HIGH CAPACITY

Data memory to 512K words (2-million bytes)

# PRECISION

38-bit floating point arithmetic

FPS can bring new power to your computer system. Find out how FPS Array Processor technology can benefit your application. For more information and an FPS Array Processor brochure, use the reader response number or coupon below. For immediate consultation, contact Floating Point Systems directly.

See FPS Array Processors at NCC June 5-8, Booth 1615



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# NCC PRODUCT REVIEW

# PLOTTER FOR PERSONAL COMPUTING SYSTEMS



Designed to serve the needs of system builders, as well as microcomputer and personal computer users, Microplotter  $2^{\text{TM}}$  is a ready-to-use unit, complete with RS-232-C interface. This digital plotter features an  $8.5 \times 11^{\prime\prime}$  (21.6-  $\times$  27.9-cm) page size. Resolution is either 0.005 or 0.01" (0.013 or 0.025 cm). Houston ląstrument, One Houston Sq, Austin, TX 78753.

See at Booth 1631 Circle 443 on Inquiry Card

## **SWITCHING POWER SUPPLIES**

Operating at the 25-W level, the OL25 series provides 4 outputs-5 V at 3.5 A, 12 V at 0.5 A, -12 V at 0.5 A, and -5 V at 0.5 A-on a barrier strip. Measuring 2.5 x 4 x 6" (6.4 x 10 x 15 cm), the switcher serves MPU-based systems, CRT terminals, and plasma gas displays. Input line regulation is ±0.2% max, input voltage is 95 to 130 Vac, input frequency range is 47 to 440 Hz, and typ efficiency is 65%. Min holdup time is 16 ms. Load regulation at 5 V is ±1% (±4% for all other voltages). Protection is offered against short circuits, overvoltages (5-V output), input surge currents, and inherent reverse voltages. Boschert Associates, Inc, 384 Santa Trinita Ave, Sunnyvale, CA 94086.

See at Booth 1728 Circle 444 on Inquiry Card

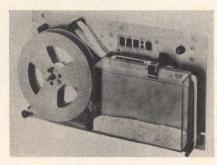
## MULTIPURPOSE INTELLIGENT TERMINAL SYSTEM

VDP-1000 is a programmable system designed to perform data cleanup or tabulation or full scale processing of system or application programs. It offers a 16-bit computer, 5M-byte disc, up to 128k bytes of high speed memory, and a virtual memory operating system to manage main memory and disc exchange as required without special instructions from the application program.

Intelligence is software dependent and under user control. Application software can be written in BASIC, COBOL, or ASGOL. In addition, the equipment interacts with the screen to prompt, edit, and display full forms from memory. Lear Siegler, Inc, Electronic Instrumentation Div, 714 N Brookhurst St, Anaheim, CA 92803.

See at Booth 1519 Circle 445 on Inquiry Card

# RACK-PANEL-MOUNTED PUNCH SYSTEM



Concentric spooling, serial or parallel interface, high capacity chad container, Moduperf punch mechanism guaranteed for 1M ft (305 km) min of paper tape, and a tape sensor package are featured in the RP-75. The system receives data at speeds up to 75 char/s asynchronously, or at 300, 600, or 750 baud in serial configuration. Mylar, Mylar laminates, oiled, and unoiled tape may be punched interchangeably without readjustment. Data Specialties, Inc, 3455 Commercial, Northbrook, IL 60062.

See at Booth 1663 Circle 446 on Inquiry Card

# INTERACTIVE COMPUTER GRAPHIC TERMINAL

The 8500M is an intelligent, self-contained ASCII and APL keyboard/CRT terminal based on the Motorola 6800 microprocessor. It can be directly wired or connected via telephone lines to large-scale or minicomputers. Vectors, alphanumeric text, and live TV or stills may be intermixed. Features are 32-level gray scale, 256 text sizes, 360-deg rotation, scaling, and windowing. The flicker-free, high resolution, self-refreshing display has a 4096 viewable matrix and 8129 addressable matrix. Also included are stroke table char

generation, selective erase by computer, video frame store, CCTV compatibility, and zoom capability. Character and vector hardware generators are built-in. **Princeton Electronic Products, Inc,** PO Box 101, North Brunswick, NJ 08902.

See at Booth 4439 Circle 447 on Inquiry Card

## ALPHANUMERIC DISPLAY TERMINAL

High quality char generation and 132-col x 30-line format are offered in the model 132B terminal, containing dual microprocessors for separate control of terminal and communication functions. Memory is 8k bytes, expandable to 16k. Features include line and page editing, tabbing, full cursor control, 10-key numeric pad, 12 function keys, and optional polling and printer interfaces. Communication is asynchronous ASCII at selectable rates of 110 to 9600 baud. **DatagraphiX**, **Inc**, PO Box 82449, San Diego, CA 92138.



See at Booth 2452 Circle 448 on Inquiry Card

# NOTE

1000 series booths are located in North Hall, 2000 series are in South Hall, 3000 series are in the Arena, and 4000 series are in West Hall—all at the Anaheim Convention Center; however, booths numbered 1 through 999 are located at the Disneyland Hotel Exhibition Hall in the Personal Computing Festival area.

# From a single CPU board



# to a half million word super computer

That's the selection you get from ROLM's AN/UYK-19 family. It's the most complete line of Mil-Spec computers in the industry. And every piece is backed by extensive, updated, upward compatible software.

Delivery? 30 days or less because they're all standard products in continuous production. Plus they follow a modular concept for interchangeability, compatibility and upgrading.

Rolm completes the package with full nomenclature and an integrated line of both military and commercial peripherals.

In just seven years we've been able to put together a family plan that lowers your programing costs, reduces hardware costs, cuts out your risk and gives you quicker reaction time.

# That's Why We're #1 in Mil-Spec Computer Systems



MIL-SPEC Computers

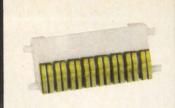
4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

Visit our booths at AFCEA Show, Washington, D.C.-June 20-22 & International Naval Technology Expo, Rotterdam-June 6-8.

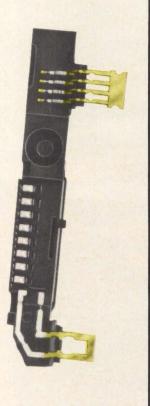
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# SPRING ASSEMBLIES

# Instrument Specialties assumes all the headaches and guarantees quality!

Until recently, Instrument Specialties was known only for the superb quality and performance of our beryllium copper springs and spring contacts. Customers bought the springs, and frequently assembled them into molded blocks in their own plants—with varying degrees of success.

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We'll be happy to discuss your specific needs—just phone. Or, for a free catalog, write today to Dept. CD-84.

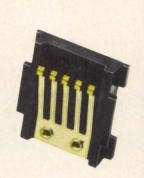


Little Falls, New Jersey 07424

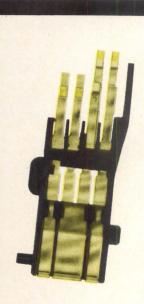
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# NCC PRODUCT REVIEW

# SBC-COMPATIBLE MEMORY BOARDS

Line of Intel<sup>TM</sup> Multibus<sup>TM</sup> compatible memories includes 4k, 8k, 12k, 16k (2 versions), 32k, 48k, and 64k byte boards; 4k, 8k, 12k, and 16k boards use 4k dynamic RAMs, 16k and larger boards use 16k RAMs. All are available in 3 configurations, without error detection, with single bit parity, or with single-bit error correction and double-bit error detection. Error correcting configurations are equipped with diagnostic indicators to pinpoint precisely the chip in which error occurred. Each board has onboard refresh of RAM, as well as external refresh synchronization. Mupro, Computer Products Div, 424 Oakmead Pkwy, Sunnyvale, CA 94086.

See at Booth 4038 Circle 449 on Inquiry Card

### CARD/BADGE READERS

CB3 series readers for use by OEM manufacturers are designed to be mounted in a data collection terminal or used as standalone units. They accept both std or mark sense tab cards, and type 3 plastic badges all intermixed. Reciprocating mechanism allows data to be read during insertion and/or on the return, thus verifying data. An optional straight through feed feature may be used for capturing the source document or for performing special requirements. A stacking option for captured cards is available. Operating life is 15,000 h or 20M read cycles. MTBF is 3000 h. Various mechanical configurations permit direct replacement of most current card/badge readers. Peripheral Dynamics, Inc, 1850 Gravers Rd, Norristown, PA 19401.

See at Booth 4149 Circle 450 on Inquiry Card

## LOW PROFILE RACK-MOUNTED 8-BIT MICROCOMPUTER

Based on the BLC80/10 central processor board using the INS8080A microprocessor, the model RMC 80/10 microcomputer incorporates programmable serial and parallel I/O, complete busing, power supply, fans, and 3 expansion-board slots. It features 6 general-purpose 8-bit registers, used singly or in pairs for double precision operations; an accumulator; a 16-bit program counter for direct addressing of 64k bytes of memory; a 16-bit stack pointer; and 6 interrupts. CPU has 1k bytes of

RAM and 4 sockets for up to 4k bytes of p/ROM using MM2708 devices; 2 ROM sockets support an optional system monitor for loading, debugging, and executing programs. Programmable communications interface provides synchronous or asynchronous serial I/O with jumper-selectable baud rates from 110 to 19.2k, either as 20-mA currentloop or RS-232-C signals. 48 lines may be software or firmware programmed to any uni- or bidirectional I/O configuration. I/O can be increased with the company's combination boards. National Semiconductor Corp, Computer Products Group, 2900 Semiconductor Dr, Santa Clara, CA 95051.

See at Booth 4135

# LSI-11 BASED TABLETOP MICROCOMPUTER



MTV/X3 desktop microsystem contains a PDP-11 compatible microprocessor, 62k bytes of RAM, extended instruction set, floating point arithmetic, and 8-quad slot backplane. Also included are a 12-line x 40-col plasma display, keyboard with numeric pad, triple minifloppy disc with >1M bytes of storage, and 132-col, 60-char/s impact printer. The system is housed in a 41- x 53- x 61-cm enclosure and weighs 35 kg. DEC RT-11 operating system license and 15 minidiskettes are std. **General Robotics Corp**, 57 N Main St, Hartford, WI 53027.

See at Booth 2602 Circle 451 on Inquiry Card

# UNIVERSAL LIGHTED PUSHBUTTON SWITCH

Series 05-6 are offered in momentary and maintained action in lighted, nonlighted, and indicator-only versions. Maintained action provides dual indication, light and lens position. Logic level switching versions have bifurcated contacts which offer self-cleaning wiping action. Mounting in a 0.750" (19-mm) sq panel cutout, switches accept the T-1¾ flange base lamp. Lamps are easily replaceable from front of panel. All units are provided with wide terminal clearance, 0.180" (4.5 mm) min, to facilitate handwiring and to offer ample clearance for most international requirements. Ratings are 1 or 3 A, 125 Vac max. Licon, a div of Illinois Tool Works, Inc, 6615 W Irving Park Rd, Chicago, IL 60634.

See at Booth 2509 Circle 452 on Inquiry Card

## STEPPER MOTOR OPTIONS FOR PRINTERS

Stepper option for DMTP-6 series printers allows vertical spacing of either 6 lines/in (2.4/cm) for normal text or 9 lines/in (3.5/cm) for high density applications such as graphics, plotting, or forms. With the latter, a continuous vertical line can be printed anywhere on the page. Alternation between modes can occur dynamically line by line, Additional control input allows forward or reverse operation. Paper slewing without duty cycle limitations, quiet operation, and "paper in motion" output are included; 2 logic level inputs provide motor control. Practical Automation, Inc, Trap Falls Rd, Shelton, CT 06484.

See at Booth 1345 Circle 453 on Inquiry Card

## HIGH PERFORMANCE 16-BIT MICROPROCESSOR

Implemented in n-channel, depletion load, silicon-gate technology, and packaged in a 40-pin cerDIP, the 8086 addresses up to 1M bytes of memory logically as a linear sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. Internal pipelining and overlapped instruction fetch and execution further improve performance, providing throughput 10 times that of the 8080A. A strap pin defines the system configuration; definition of a subset of the pins changes dependent on the condition of the strap pin. Bus structure allows use of existing 8080A peripherals. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.

See at Booth 1527 Circle 454 on Inquiry Card Some companies exhibiting at NCC '78 are showing products that could not be disclosed by Computer Design's printing deadline; some are exhibiting only standard, off-the-shelf products; still others supplied information that was too late or too little for processing as "first time shown" products. The following short summaries point out a sampling of the products that NCC '78 attendees can expect to be exhibited by these categories of companies. Information is based on that received by press time.

# Now you can do Zilog Z80 development on your MDS-800

If you are a MDS-800 or Series II user, and you need high performance Zilog Z80 hardware and software development capability at a low price, read on. Only RELMS offers you the powerful In-circuit Emulator (ICE) and the Systems Adaptor Module (SAM) for hardware and software development.

Here's real price/performance value. The complete Z80 package is priced at \$3,890 (thousands of dollars under comparable systems). ICE and SAM are also totally transparent and compatible with your MDS-800 or Series II. The Z80 board replaces your Intel CPU board in the MDS. SAM supports all the Z80 features with a relocatable disk macro-assembler and monitor for extensive software debugging. ICE features full speed emulation of the Z80A with 256 x 40 TRACE, memory mapping, hardware BREAKREGION,™ selectable clock speed and RAM based control program. All come with complete documentation.

Learn more about ICE and SAM. The affordable Z80 development tools for your MDS. They are available separately or together for immediate delivery. Call or write today for full details.



BREAKREGION™ is a trademark of RELMS

# relms

Relational Memory Systems, Inc. P.O. Box 6719, San Jose, CA 95150, (408) 248-6356 Amcomp (Booth 3206): 8500 series 2.5M- to 40.2M-bit hard disc memories; model 2730 12.5- to 45-in/s (31.8-to 114-cm/s) tension arm and model 2790 75- to 125-in/s (190- to 317-cm/s) vacuum column magnetic tape units.

Axiom Corp (Booth 52): Electrosensitive, 8048-based EX-801 MicroPrinter; plus EX-820 MicroGraphics printer for graphics and alphanumerics.

Byte Industries Inc (Booth 113):
Junior™ 8080-based microcomputer system; also smaller, slower, lower cost version of business computer.

Centronics Data Computer Corp (Booth 1442): Serial (S1) and parallel (P1) interface electrosensitive printers for microprocessor systems; 300 series 100/165-char/s impact printers; 700 series 60/165-char/s serial, dot matrix printers; 6000 series 50/750-line/min printers.

Cherry Electrical Products Corp (Booth 2750): Low profile, solid-state capacitive keyboard rated at over 300 x 10° operations; also flexible keyboard for personal computer and OEM markets.

Chromatics, Inc (Booth 1726): CG line, high resolution color graphics computers featuring Z80 CPU with full memory and I/O structure, and RS-232-C interface.

Computalker Consultants (Booth 39): Model CT-1 voice synthesizer designed for standard S-100 I/O bus configuration is controlled by nine acoustic-phonetic parameters for perceptual and physiological fundamental aspects of speech.

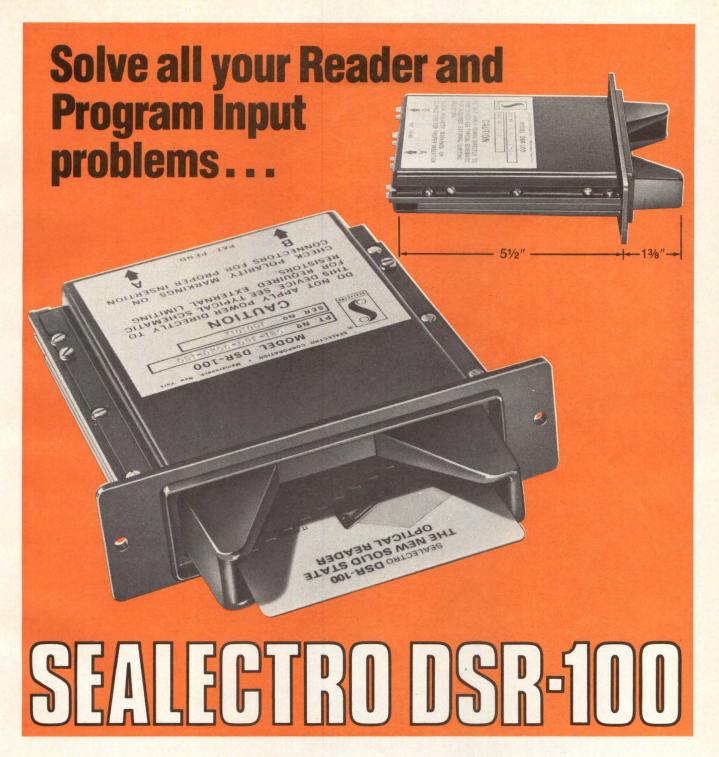
Data Electronics, Inc (Booth 4415): High density 17.28M-byte, 450-ft (76.2-m) cartridge tape drive with data transfer rate of 192k bits/s.

Data Printer Corp (Booth 1360): Model 1260 microprocessor-controlled, 600-line/min chain printer with motorized upper and lower tractor positioning.

Dataware, Inc (Booth 2749): Updated version of RPG/RPG II to COBOL translator for most major mainframes; other packages convert to ANS COBOL and PL/1 (DOS or OS).

**Deltec Corp (Booth 4333):** 22.5- to 90-kVA,  $3\phi$  computer room power conditioning systems providing 120 dB of common and normal mode rejection.

Digital Associates (Booth 1732): Plug-compatible printers for IBM Series/1, DEC PDP-11, Data General,



- Models for all standard punched hole badges styles...up to 22 columns.
- Reads complete Alpha-Numeric Hollerith code.
- Complete validity check...no false data readouts.

Sealectro's DSR-100 solid-state badge reader solves all your reader and program input problems. Extra compact...fits anywhere in your system. Maximum capability at lowest dollar costs. Ultra-reliable for time-

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PROGRAMMING DEVICES DIVISION

# SEALECTRO

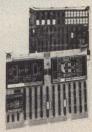
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1901 Old Middlefield Way, Suite 19, Mountain View, Ca. 94043 (415) 965-1212
Sealectro Ltd., Portsmouth, Hants, England
Sealectro S.A., Zone Industrielle Toulon Est, 83087 Toulon Cedex, France

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CIRCUIT COMPONENTS R.F. COMPONENTS PROGRAMMING DEVICES



Microcomputer Analog I/O Systems





For:

INTEL SBC-80 Series (8080A) ZILOG MCB Series (Z-80) DEC LSI-11 & LSI-11/2

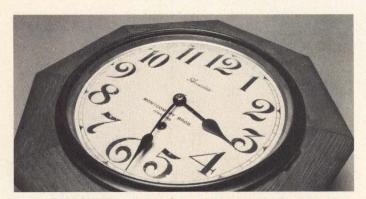
Computer Automation LSI 2,3 & 4 Series National Semi IMP/PACE & BLC-80 Series

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almost anyone gives you. 56 standard models, 375 or 750 watts output over –10° C to +60° C without derating. Fast delivery too. Call us.



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## NCC PRODUCT REVIEW

Hewlett-Packard, Interdata, General Automation, and other computer systems.

The Digital Group (Booth 2854):
Completely integrated computer
package with 18k or 32k of memory
and ability to support up to 64k, with
CRT data display, Z80 CPU, and
mini-floppy or digital cassette
interface.

Diva, Inc (Booth 1161): PDP-11/70 compatible disc system communicates directly with computer's cache bus controller, transfers full 32-bit words directly into memory without Unibus intervention.

**Documation, Inc (Booth 2363):** Impact 3000, 3000-line/min printer; also 50-char/s serial printer.

Elgar Corp (Booth 1209): 15-kVA uninterruptible power system with either 1- or  $3\phi$  input to  $1\phi$  output for minicomputer applications; and  $3\phi$  high isolation transformers with ratings from 3 to 60 kVA.

Epicom Inc (Booth 2654): Line monitor for data communications networks permits viewing and analysis of half- or full-duplex traffic up to 100k bit/s; also portable standalone system which records digital communications data and status signals regardless of line discipline.

Florida Data Corp (Booth 4028):
Model PB-600 bidirectional,
microprocessor-controlled 600-char/s
serial printer has speed of 240 to
1200 lines/min, uses standard 7 x 7
dot matrix or 8 x 7 for lower case
characters with descenders.

General DataComm Industries Inc (Booth 3015): Netcon-5 network diagnostic and control system, 300- to 19,200-bit/s modems; microprocessorbased high speed modems; data line concentrators; plus time and frequency division multiplexers.

General Electric Co, Data
Communication Products Dept (Booth
4309): Termi-Net<sup>TM</sup> 1232, 132-col,
1200-baud teleprinter includes 1k
buffer, has replaceable print fingers,
and uses rotating print belt with
510-char/s hammerbank mechanism.

Harris Corp (Booth 2639): Series 300 computer system; remote batch terminals; intelligent, interactive terminals; and distributed processing systems.

# GE puts it on the line with a full family of TermiNet line printers

Four value-packed <u>true</u> line printers with <u>real</u> 90-340 lines per minute throughput at practical, low prices

Small size. Compact design. Modern styling. Quiet operation. Low prices.

At the same time this new space-saving family of GE TermiNet line printers is big on throughput. Gives you a range of speeds from 90 lpm to 340 lpm, depending on the number of printable characters per line and the size (64 or 96) of the ASCII subset. And that's *real* throughput.

They're big on reliability backed by years of proven electronics and rotating belt technology. (Over 75,000 GE belt printers installed worldwide.)

Big on quietness. They're a welcomed addition to any office or computer room. Big on value-packed features. 132 columns. Original and 5 copies. A unique ribbon cartridge. With a life span of 50 million print characters.

The only thing you'll find small about this family of true line printers is their size and price. In these days of spiraling costs, GE is putting it on the line with practical, low prices. From \$4300 for the TermiNet 310 printer to \$5130 for the TermiNet 340 printer (user quantity 1).

Let us prove it. Write General Electric Company, TermiNet 794-17A, Waynesboro, VA 22980.

For your special kind of needsa special kind of printer

GENERAL & ELECTRIC

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Inforex, Inc (Booth 1121): System 7000 standalone and master control terminals with IBM 2780 and 3780 batch communications capabilities; 5000 file access system; 1330 remote data entry system; and 3300 key-to-disc system.

Informer Inc (Booth 1315): Lightweight model D303/9655 intelligent terminal reads ABA stripe 2 on common credit cards in either interactive or polled block mode, standard character CRT display is 40 x 12, interfacing is RS-232:

Integrated Software Systems Corp (Booth 1338): Tell-A-Graf computer graphics system uses sophisticated language processor to produce high quality chart or graph with just a few words of simple English.

Intelligent Systems Corp (Booth 4407): Standalone model 8051 desktop microcomputer system includes 8080A CPU, 19" (48-cm) CRT, complete graphics package, 21k-bytes ROM, single mini-floppy drive; model 8001G 48-line x 80-char/line graphic CRT display system has 19" (48-cm) screen with 8 colors foreground and background.

International Power Machines Corp (Booth 2501): 415-Hz uninterruptible power systems for IBM 3032, 3033, and 370/168; also 60-Hz UPS.

Lynwood Scientific Developments Ltd (Booth 1244): User-programmable, microprocessor-based model GD-1 visual display unit with programs stored in UV light erasable p/ROMs.

Management Systems and Programming Ltd (Booth 1133): "Datamanager" data dictionary system for data resource management with automatic error recovery and status facility; and "Testmanager" structural programming testing system.

MDB Systems (Booth 2106): Interface products for IBM Series/1 including line printer controller, TTY/RS-232 serial adapter, and wirewrap board configurations; peripheral device controllers; general-purpose logic modules; and communications modules.

Megatek Corp (Booth 1715): Megagraphic 7000 intelligent refresh vector display system has 32-bit graphic word length.

Memorex Corp (Booth 2327): Disc drives and controllers; add-on memories; and data communications controllers.

Midwest Scientific Instruments, Inc (Booth 109): MSI 6800 computer system contains up to 56k RAM and 8k EPROM, 8 I/O ports, 16-position motherboard, and heavy duty power supply; also FD-8 Quad, double-density, double-sided floppy disc used with microcomputer systems.

Modular Technology (Booth 1133): Modem or terminal diagnostic and patching equipment; self-contained baseband modem.

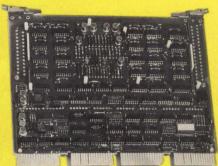
Mostek Corp (Booth 3415): MK 8000 general-purpose, 5M-byte mainframe add-on memory system or disc replacement features from 16k x 18 to 128k x 24 words of storage.

# MICROPROCESSOR CORE MEMORIES

FOR THE LSI-11, 8080, 6800, IMP-16P, S100

THE MM-1103 OFFERS 2 OR 4 TIMES THE MEMORY CAPACITY! FOR THE SAME SIZE AND POWER AS THE DEC MMV-11A!

MM-1103 8K X 16



MM-1103/16 16K X 16

PLUGS DIRECTLY TO DEC LSI-11 AND PDP 11-03 COMPUTER



# MM-6800 8K X 8

USED ON MOTOROLA'S EXORCISER
AND MICRO MODULES



MM-S100 8K X 8

USED ON IMSAI 8080, ALTAIR, AND SOL MICROCOMPUTER



# **FEATURES:**

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- PIN-TO-PIN COMPATIBILITY.
- POWER MONITORING FOR DATA PROTECTION.
- DELIVERY FROM STOCK.
- ONE YEAR WARRANTY ON PARTS AND LABOR.
- ALL UNITS TEMPERATURE CYCLED AND BURNED IN.



# MM-8080AL 8K X 8

USED ON INTEL'S MDS 800 AND SBC 80/10 MICROCOMPUTER

9438 Irondale Ave. Chatsworth, California 91311 Telephone: (213) 998-0070 4 MHz Z80 + 4 MHz AMD9511 On One Board =

# COMPUTER POWER

# PCS plans ahead.

PCS saw the need in the industry for a Z80 based module, but didn't start there. PCS designed for the 4 MHz version AND the latest and fastest (4 MHz) single chip floating point processor, put them on the same board, the PCS 1880, and made it work.

# The PCS 1880 module,

the first designed to interface the AMD9511 LSI math chip directly to the Z80 microprocessor, means speed (fewer T cycles/instruction, fewer instructions necessary to obtain the same results), and

# What everyone should know

is that the PCS 1880 means real capability. Its enhanced instruction set, crystal controlled Real Time Clock, RAM/ROM/EPROM memory, optically isolated tri-function serial port (RS232-20mA current loop or party line), baud rates switch-selectable from 110-9600 baud, and interrupts, COMBINED with the 4 MHz math chip capable of add, subtract, multiply, divide,



# DAS

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Please send me more information about:

The PCS 1880 SuperPac Industrial

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floating point, square root, logarithms, exponentiation, trig and inverse trig functions, means computer power. And the module is compatible with all Super-Pac Series hardware and software.

# PCS microcomputers perform,

and the 1880 microcomputer can outperform many existing minicomputers, particularly when trig functions are required.

# Cost-effective

design, manufacturing, and implementation makes the PCS 1880 and other PCS products possible.

# PCS microcomputers make sense.

PCS created the popular SuperPac (4- and 8-slot versions), the stand-alone ready-to-plug-in industrial microcomputer with TTY format keyboard and CRT, backed with a complete line of standard industrial hardware and software, memory, I/O, and peripheral interfacing. PCS created the 1880.

Prince to the Princes

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# LOCAL STOCK



# **Open Frame Power Supplies**

ARIZONA: Scottsdale, PLS Associates (602) 994-5461

CALIFORNIA: Pasadena, A-F Sales Engineering Inc. (213) 681-5631

San Jose, Richards Associates (408) 246-5860

COLORADO:

Denver, PLS Associates (303) 773-1218 CONNECTICUT:

Litchfield, Digital Sales Assoc. (203) 567-9776

FLORIDA:

Orlando, Gra-Mar, Inc. (305) 894-3351

ILLINOIS:

Chicago, Coombs Assoc. (312) 298-4830

INDIANA:

Indianapolis, Coombs Assoc. (317) 897-5424

MARYLAND:

Lanham, Brimberg Sales Assoc., Inc. (301) 946-2670 Baltimore, Brimberg Sales Assoc., Inc.

(301) 792-8661

MASSACHUSETTS:

Waltham, Digital Sales Assoc. (617) 899-4300

MINNESOTA:

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Syracuse, C.W. Beach Company (315) 446-9587

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# NCC PRODUCT REVIEW

Newbury Laboratories Ltd (Booth 1244): Model 7000, 7001, and 7002 visual display terminals with 24 lines of 80 characters and selectable speeds from 50 to 19,200 baud; models 7008 and 7009 have cursor controls and other features.

North Atlantic Industries, Inc, Qantex Div (Booth 1213): Model 200 Minidrive<sup>™</sup> tape transport for 3M model DC100A miniature data cartridge; model 3400 militarized data cartridge storage system; plus model 650 low cost drive.

North Star Computers, Inc (Booth 60): Horizon-1 microcomputer system with Z80A CPU, 16k RAM, mini-floppy, and 12-slot S-100 motherboard; -2 has second floppy drive.

Oliver Advanced Engineering Div (Booth 116): Series of piggyback p/ROM programmers; paper tape reader; standalone computer controller.

Perkin-Elmer Data Systems (Booth 2430): Interdata 800 business system; model 1100, 1200, and 600 terminals; and Wangco mini-floppies.

Rair Microcomputers (Booth 1133): Fully integrated microcomputer systems featuring 8085 microprocessor, floppy disc operating system, advanced BASIC interpreter, and FORTRAN and COBOL compilers.

RDA, Inc (Booth 45): RD-11C microcomputer system based on DEC LSI-11 CPU includes dual mini-floppy drive with 205k bytes of storage and 64k-bytes RAM.

Sheldon-Sodeco Printer Corp (Booth 2661): Series PR2100 alphanumeric impact multicopy ticket printers operate at speeds up to 3 lines/s numeric and 1.5 lines/s full alphanumeric, feature dual independent paper feed.

Shugart Associates (Booth 2445): Winchester technology rigid disc drive, more compact and less expensive than comparable units available to OEMs, yet IBM Systems/32 and /34 and Series/1 compatible.

Silonics (Booth 3122): Ink-jet printer (see Product Feature, pp 256-257 this issue).

Sintrom Electronics Inc (Booth 1244): Microprocessor-based model 6051

continuous data logger; model 6041 cartridge storage system for communications environments: 300 series cartridge drive; and 3041 plotter controller.

The Space Byte Corp (Booth 7): Modular computers with business application software, designed for first time users, based on 8085 CPU and 16k memory, includes iCOM FDOS III operating system.

Systems Furniture Co (Booth 4100): Data Desk II computer furniture system featuring modular building block approach with optional desk sizes, shelves, enclosures, pedestals, and partitions.

Tally Corp (Booth 1115): 1200-baud model T-1612 bidirectional, 160-char/s printer terminal; 1000 series 120-char/s, undirectional serial printer; 2000 series 125-line/min printer with serial or buffered serial RS-232 interface; and 500-line/min model T-5000 dot matrix impact printer.

Technical Design Labs (Booth 103): Computer systems based on Z80 CPU with software supplied on cassette.

Tektronix, Inc (Booth 2309): 4025/24 alphanumeric display terminals allow scrolling of both alphanumerics and graphics, can copy up to 53 lines with 4631 copier; also Option 40 programmable keyboard capability for high resolution 19" (48-cm) 4014-1 and 4015-1 display terminals.

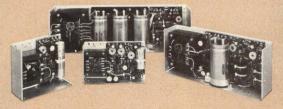
Texas Instruments, Inc (Booth 1339): Model 774/1 intelligent terminal system; 765 portable memory terminal; and 990 computer family.

Vu-Data Corp (Booth 2557): 50-MHz, small, lightweight oscilloscope with DMM and counter; and 20-MHz, battery-operated versions.

Wang Laboratories (Booth 2764): Dual diskette, CRT, WP10A standalone word processing system; WCS-80 multi-user/multi-job computer with COBOL, RPG II, and BASIC; plus 2200VS user-oriented business processor.

Western Union Information Systems (Booth 1310): System 4100/2 statistical multiplexer accommodates synchronous and asynchronous data terminal equipment at speeds up to 9600 bits/s. 

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		ilana e e e e	and the same			±.02%	REGULATION	• REMOTE S	SENSING						
VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9
5	3.0 6.0 12.0 18.0	B5-3 C5-6 D5-12 E5-18	\$24.95 44.95 74.95 104.95	12	1.7 3.4 6.8 10.2	B15-1.5 C15-3 D15-6 E15-9	\$24.95 44.95 74.95 104.95	18	1.3 2.6 5.2 7.8	B24-1.2 C24-2.4 D24-4.8 E24-7.2	\$24.95 44.95 74.95 104.95	24	1.2 2.4 4.8 7.2	B24-1.2 C24-2.4 D24-4.8 E24-7.2	\$24.95 44.95 74.95 104.95
6	3.0 6.0 12.0 18.0	B5-3 C5-6 D5-12 E5-18	\$24.95 44.95 74.95 104.95	15	1.5 3.0 6.0 9.0	B15-1.5 C15-3 D15-6 E15-9	\$24.95 44.95 74.95 104.95	20	1.3 2.6 5.2 7.8	B24-1.2 C24-2.4 D24-4.8 E24-7.2	\$24.95 44.95 74.95 104.95	-	-	-	-

# SINGLE OUTPUT — HI-VOL

VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9	VOLTS	AMPS	MODEL	PRICE 1-9
2	3.0 6.0 12.0 18.0	HB2-3 HC2-6 HD2-12 HE2-18	\$29.95 49.95 79.95 109.95	12	0.5 1.7 3.4 5.1	HA15-0.5 HB12-1.7 HC12-3.4 HN12-5.1	\$22.95 24.95 44.95 64.95	24	1.2 2.4 3.6 4.8	HB24-1.2 HC24-2.4 HN24-3.6 HD24-4.8	\$24.95 44.95 64.95 74.95	48	0.5 1.0 3.0 4.0	HB48-0.5 HC48-1 HD48-3 HE48-4	\$29.95 49.95 79.95 109.95
5	1.2 3.0	HA5-1.2/OVP* HB5-3/OVP*	24.95		6.8 10.2	HD12-6.8 HE12-10.2	74.95 104.95	- L	7.2	HE24-7.2	104.95				
	6.0 9.0 12.0	HC5-6/OVP* HN5-9/OVP* HD5-12/OVP*	49.95 69.95 79.95	15	0.5 1.5 3.0	HA15-0.5 HB15-1.5 HC15-3	\$22.95 24.95 44.95	28	1.0 2.0 3.0	HB24-1.2 HC28-2 HN28-3.0	\$24.95 44.95 64.95	180, 200	0.12	HB200-0.12	\$34.95
	18.0	HE5-18/OVP*	114.95		4.5 6.0 9.0	HN15-4.5 HD15-6 HE15-9	64.95 74.95 104.95		4.0 6.0	HD28-4 HE28-6	74.95 104.95	250	0.1	HB250-0.1	\$34.95

# SINGLE OUTPUT — HIGH POWER

VOLTS	AMPS	MODEL	PRICE 1-9
5	25.0 35.0	F5-25/OVP* G5-35/OVP*	\$149.00 185.00
12	16.0	F15-15	\$149.00
15	15.0	F15-15	\$149.00
24	12.0	F24-12	\$149.00
28	10.0	F24-12	\$149.00

# SINGLE OUTPUT - HIGH EFFICIENCY

VOLTS	AMPS	EFFICIENCY @ NOMINAL LINE	MODEL	PRICE 1-9
5	9	66 %	RD5-15/OVP*	\$ 99.95
	12	63 %		
	15	60%		
5	14	63%	RE5-23/OVP*	\$130.00
	18	60%		
	23	57 %	The section of the section of	
5	25	63 %	RG5-40/OVP*	\$220.00
	32	60 %	TANGENTS I TEM ELVIN	D4.10.11.11.11.11
	40	57 %		

# **DUAL OUTPUT — STANDARD**

MODEL	OUTPUT #1	OUTPUT #2	PRICE 1-9
AA15-0.8	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A	\$42.95
BB15-1.5	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A	\$53.95
CC15-3.0	12V @ 3.4A or 15V @ 3.0A	-12V @ 3.4A or -15V @ 3.0A	\$84.95

# **DUAL OUTPUT — HI-VOL**

MODEL	OUTPUT #1	OUTPUT #2	PRICE 1-9
±12 to 15V HAA15-0.8 HBB15-1.5 HCC15-3.0	12V @ 1.0A or 15V @ 0.8A 12V @ 1.7A or 15V @ 1.5A 12V @ 3.4A or 15V @ 3.0A	-12V @ 1.0A or -15V @ 0.8A or -5V @ 0.4A -12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A -12V @ 3.4A or -15V @ 3.0A	\$39.95 49.95 79.95
±18 to 24V HAA24-0.6	18-20V @ 0.4A or 24V @ 0.6A	(-)18-20V @ 0.4A or -24V @ 0.6A	\$39.95
±5V HBB5-3/OVP HCC5-6/OVP	5V @ 3.0A* 5V @ 6.0A*	−5V @ 3.0A* −5V @ 6.0A*	\$61.95 92.95
5V and 9-15V (Isolated Outputs) HAA512 HBB512 HCC512	5V @ 2.0A * 5V @ 3.0A * 5V @ 6.0A *	9-15V @ 0.5A 9-15V @ 1.25A 9-15V @ 2.5A	\$44.95 54.95 86.95

# TRIPLE OUTPUT — STANDARD

		ACKING REGULATORS . I.	02% REGULATION	
MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
BAA-40W	5V @ 3.0A	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A	\$ 69.95
CBB-75W	5V @ 6.0A	12V @ 1.7A or 15V @ 1.5A	-12V @1.7A or -15V @ 1.5A	\$ 91.95
DBB-105W	5V @ 12.0A	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A	\$126.95

# TRIPLE OUTPUT - HI-VOL

MODEL	OUTPUT #1	OUTPUT #2	OUTPUT #3	PRICE 1-9
HTAA-16W	5V @ 2.0A*	9-15V @ 0.4A	(-)9-15V @ 0.4A or -5V @ 0.2A	\$ 49.95
HBAA-40W	5V @ 3.0A*	12V @ 1.0A or 15V @ 0.8A	-12V @ 1.0A or -15V @ 0.8A or -5V @ 0.4A	\$ 69.95
HCBB-75W	5V @ 6.0A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$ 91.95
CP-131	5V @ 8.0A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$110.00
HDBB-105W	5V @ 12A*	12V @ 1.7A or 15V @ 1.5A	-12V @ 1.7A or -15V @ 1.5A or -5V @ 0.7A	\$126.95
HDCC-150W	5V @ 12A*	12V @ 3.4A or 15V @ 3.0A	-12V @ 3.4A or -15V @ 3.0A	\$149.00

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+24V and ±5V CP-205 CP-206 CP-162	1A 2.5A 3A	0.5A 0.5A 0.6A		1.5A/1.7A 3.0A/3.4A 5A/6A	\$ 69.95 \$ 91.95 \$120.00

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# DATA REDUCTION AND DISPLAY IN AUTOMATED TEST SYSTEMS

An automated test system with a versatile data reduction software package can present the masses of accumulated test data in a comprehensible visual format, thereby easing the job of characterizing devices

**Trent Cave and Douglas Smith** 

Tektronix, Incorporated, Beaverton, Oregon

A versatile automated test system solves a wide range of circuit design test and measurement problems by indepth examination, evaluation, and characterization of complex semiconductor devices. Of vital interest to designers, processed test data not only provide guidelines on which to compare devices from various vendors, but also serve as the basis on which to design a circuit or to choose a device for a given circuit. Effective characterization furnishes valuable device information, such as definitive boundaries, worst-case operating conditions, functional shortcomings, and limitation sources, allowing parameters and limits to be readily classified as solid or marginal. However, the sample of characterized devices must be large enough to produce a high level of confidence in the distribution of parameters and to verify that the device meets circuit specifications.

For fast and complete device analysis, the designer needs a combination integrated circuit (IC) test and data processing system under computer control. This automated test system must integrate hardware flexibility to simulate various combinations of circuit conditions, software control to implement testing, and graphics display capability to present test results visually for easy understanding and interpretation. For example, a memory chip is exercised rapidly by the test system to ensure that each memory cell functions independently of all other cells; then, test data are plotted almost instantly on a cathode-ray tube (CRT) terminal as a map to show which cells are not independent. Since large amounts of test data must be collected and reduced for rapid analysis on a large variety of devices, the software package must allow versatile data acquisition and reporting.

# **Data Reduction**

Automated testers are used by IC vendors during design cycles to characterize new devices. Reduced data supplied by the tester may indicate that redesigning is necessary if the device does not perform as desired. Characterizing a device also allows the vendor to define all operational specifications.

As IC users, equipment designers employ automated testers for device characterization and to qualify and select vendors. Circuits are designed based on available device data. Although different vendor's devices may have the same published specifications, parametric, and sometimes even functional, differences often exist between devices with the same part number. For example, when testing a microprocessor with a fixed test pattern, one vendor's parts may pass while another's fail. If a design is based on a single vendor's device, and production tries to incorporate another vendor's device due to cost or availability, the circuit may not be acceptable. If part differences are determined early, the circuit may be designed to accommodate all vendors' devices.

Test and design engineers check device margins and upper and lower operating limits for critical parameters. To determine typical values of device parameters and what variances are likely to exist, extensive data are collected, reduced, and analyzed on a statistically valid sample of devices. If there are n device parameters, 2<sup>n</sup> tests are needed, since a parameter cannot be regarded as being independent of any other parameter until sufficient data have been collected and evaluated to verify independence. Evaluating memory arrays, for example,

## **Typical Data Plotting Techniques**

Data Category	Data Types	Suggested Plotting Technique
Individual device data	Time vs voltage (or current) Frequency vs gain	y = f(x) curve plots
	Pass/fail data for two independent variables (eg, V <sub>cc</sub> vs V <sub>DD</sub> )	Shmoo plots
	Three parameter variations (eg, V <sub>cc</sub> vs V <sub>DD</sub> vs propagation delay)	3-Dimensional and contour plots
	Pass/fail data for each memory location	Memory maps
Device population data	Burn-in variations Individual lot parameter variations	Histograms
	Lot-to-lot variations  Vendor-to-vendor variations	Cumulative histograms
	Yield analysis studies	Composite shmoo plots
	Failure analysis studies	Scatter plots

often requires test pattern sequences that are millions of steps long. Virtually overwhelming to comprehend, much less use, this flood of device information must be reduced to a manageable number of distinct items.

# **Data Reduction Methods**

Data reduction methods aid designers in interpreting and analyzing device characteristics and circuit requirements. Using these methods, designers can base their decisions on device-sensitive and solid parameters. By evaluating parameter definitions, the designer determines the particular device that will satisfy circuit requirements, resulting in significant design time and cost savings.

In a sophisticated automated tester, floating-point hardware, rather than a software routine, permits fast and accurate calculations to be performed while test programs are being run. Then, the tester controller stores test data in various media, such as a disc file (for moderate amounts of data) or a magnetic tape (for large amounts of rapidly gathered data. In addition, general program parameters may be included in the files of logged data. Since the storage technique can be specified in the test program, data can be formatted to suit the application. The designer may use either standardized or sophisticated analysis routines, developed to evaluate specific data. A line printer or a graphics display terminal plus an associated hardcopy unit provides permanent records of test results.

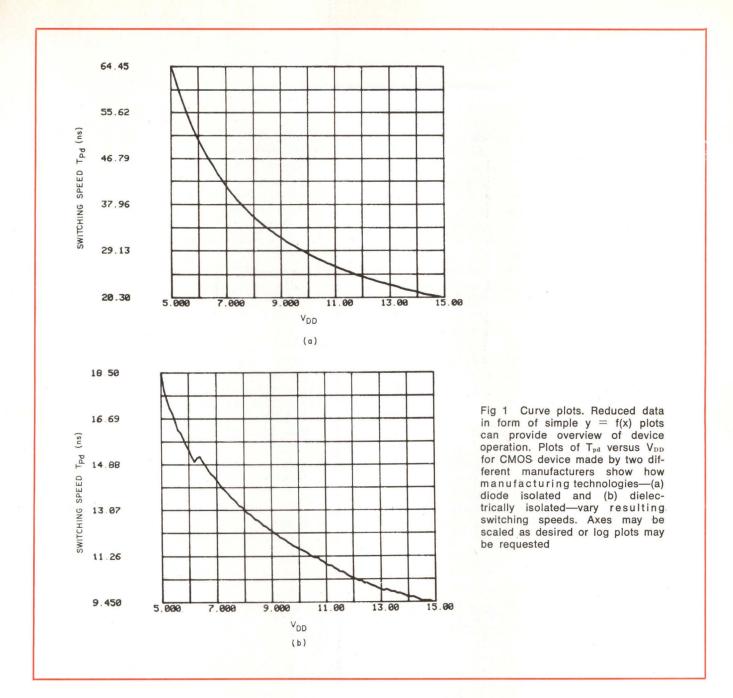
In its simplest form, raw output of an automated tester is 1s and 0s, that is, pass/fail or logic state information. The forced data and the resultant data are logged for

each test pattern word. In a functional test of a microprocessor, raw data consisting of 1s and 0s patterns millions of words long results. To interpret these data, the designer has to determine the memory address accessed, either by the pattern step number or by decoding which address pins are being forced, and then decide whether the resultant pattern is correct. From this example it is evident that such data cannot be realistically examined, digested, and evaluated.

Consequently, suitable methods are needed to reduce large amounts of raw data to a useful, comprehensible form, such as that provided by graphic displays and statistical analyses. Since a sophisticated, computer-controlled test system can store vast amounts of data for each device tested, detailed data on individual devices can not only be processed, but an overview of data on a quantity of devices is available. Statistically valid samples of devices can be tested, and the resultant data can be processed and visually displayed. Typical plotting techniques that can be used for two data categories-individual device data and device population data—are listed in the "Typical Data Plotting Techniques." Examples of these plots are subsequently defined, discussed, and illustrated. Each display is designed to maximize insight into the parameter of interest.

# **Curve Plots**

Simple y = f(x) curve plots provide overviews of device operation. For example, the IC designer may need to know which of two manufacturing techniques provides better device performance. By comparing curve plots of how a critical parameter varies with a second param-



eter, the designer can determine the effects of different techniques and, possibly, which technology is better for the application. Fig 1 shows two plots of switching speeds (Tpd) versus supply voltage (VDD) for a complementary metal-oxide semiconductor (CMOS) device made by two different manufacturers—one using diode isolated technology [Fig 1(a)] and the other using dielectrically isolated technology [Fig 1(b)]. These plots illustrate how curve plots allow comparison of two manufacturing techniques. It can be seen that the dielectrically isolated device at its slowest switching speed is faster than the diode isolated device at its fastest switching speed. Second, variability in Tpd of the diode isolated device is about 3 to 1, whereas that of the dielectrically isolated device is only 2 to 1. Using curve plots, two (or a few) devices are compared with ease; however, to compare whole lots of devices, another form of data reduction, such as histograms, should be employed.

# Shmoo Plots

Shmoo plots display actual limits of device performance (safe operating region) and, therefore, are useful in determining whether a device will function in the desired circuit. The advantage of a shmoo plot is that it shows a great deal of data in a single small display. To get an overview of device limits and to increase level of confidence in a device, several shmoo plots are compared. In the sample shmoo plot (Fig 2), a plus sign (+) indicates where the device—a 4k random-access memory (RAM)—failed within the limits of two voltage parameters (V<sub>CC</sub> and V<sub>GG</sub>); a dot (•) indicates correct operation. Knowing the limits of device performance, the designer either chooses a device that will function correctly in the circuit or redesigns the circuit. A shmoo plot does not indicate specifically why the device failed; that is, for a certain combination of two parameters, a

critical third parameter may be adversely affected. A 3-dimensional plot helps to determine why a device failed.

# 3-Dimensional and Contour Plots

Three-dimensional (3-D) plots assist in device characterization by allowing interaction among three different parameters to be observed. Height elevation of the z-axis indicates the quantitative value of the parameter of interest. Unlike the shmoo plot, a 3-D plot will indicate that a device failed for given values of two parameters because a third critical parameter was forced too high or too low. These 3-D plots are often used by IC vendors for wafer studies, with the x-y grid defining device position on the wafer and the z-axis being value of the parameter under study to determine whether it is affecting yield or probability of a good die. By studying 3-D plots generated by testing several wafers (each fabricated under different conditions), the designer can evaluate effects of various diffusions, ion implementations, or other process variables.

Fig 3(a) is a 3-dimensional plot showing the probability of a good die for each location on a wafer. At the base of the x-y grid, each square represents a die location on the wafer. The z-axis defines the probability of a good die. The designer may also use 3-D plots to see if the parameter of interest is consistent across the wafer.

A contour plot [Fig 3(b)] shows overall variance of a given parameter with respect to two other parameters. Since it is difficult to measure z-axis value in the usual isometric-view 3-dimensional plot, designers use contour plots to study precise parameter values, such as gain.

However, by using a contour plot rather than a 3-dimensional plot, the designer loses the visualization of high and low parameter values.

# Memory Maps

Memory maps indicate all locations at which data read from memory differ from expected data. Since circuit components other than memory arrays often determine memory device performance, memory maps are useful for displaying pass/fail information, thereby showing which memory cells failed under parameter conditions set in the test program. Varying a device parameter and rerunning the functional pattern to create another memory map gives a visual picture of sensitive parameters of memory layout. However, no relationship between parameters is displayed. The sample memory map (Fig 4) shows the complete memory grid; highlighted locations (solid white) indicate cell failures. By evaluating highlighted locations on the memory map, the designer can easily and rapidly see how the failure patterns of the two halves of the memory array differ.

The memory map (Fig 4) indicates that one-half of the memory has a defect that causes rows of cells to fail, while the other half has a defect that causes rows and columns of cells to fail. However, even though a memory map might help a designer to diagnose a defect, it does not indicate what caused the failure. A sophisticated memory map program allows the designer to display pass/fail information for an area of the memory grid; this is an important capability as memory size increases, since the designer wants to see which locations failed while still having a large quantity of data presented in a small picture.

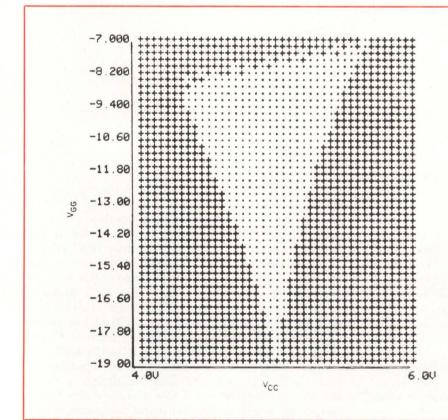


Fig 2 Shmoo plot. Reduced data in form of shmoo plot. On this particular plot, dots show safe operating region of device within limits of two parameters— $V_{\rm GG}$  and  $V_{\rm CC}$ 

# Interval Testing

Interval testing involves initially testing a device, next exposing it to an extreme stimulus, such as a high temperature, and then testing it. This process is repeated several times to establish parameter drifting from initial values. When devices are being interval tested, it is important to collect data for each device in the batch on several occasions. This type of data handling is enhanced with an automated test system. For example, data can be logged so that long-term drift can be monitored. Fig 5(a) tabulates initial values of  $V_{\rm GST}$  (voltage from gate to substrate) for a metal-oxide semiconductor (Mos) field-effect transistor, succeeding values over device life, and percent of value changes for 10 devices. These values

allow defective devices to be flagged and weeded out, but value trends are hard to visualize. Fig 5(b) shows curve plots of the percent of drift with respect to time so that value trends can be visualized.

# Statistical Data Analysis

Manual test methods take weeks or months to qualify a vendor source as to acceptable parts. An automated tester with proper data reduction and display capabilities reduces vendor qualification time to days. By using identical test program and data reduction routines, different vendors' devices can be characterized and compared. Fig. 6(a) presents a partial list of propagation delay values for a group of devices from one vendor. With





(a)

## PROBABILITY OF GOOD DIE ON WAFER

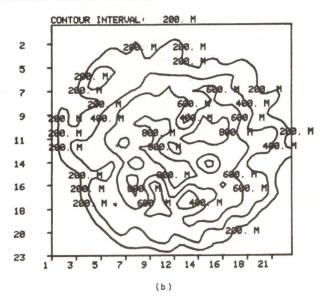


Fig 3 3-dimensional and contour plots. In 3-dimensional plot used in wafer study (a), x-y grid base defines die locations and z-axis represents probability of good die. If, on all wafers tested, location always contained good die, its z-axis dimension would be 1000. Note that maximum probability for good die for the best location in this example is 96.8%. Plot can be rotated for viewing from any angle, Contour plot of same data (b) is also based on value of 1000 for location that always yields good die. From plot it can be seen that locations in center of wafer have higher yield. Versatile contour plotting routine allows designer to blow up section of map for more detail

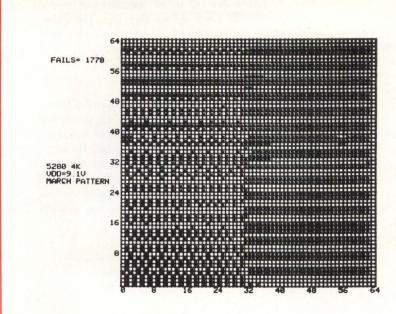
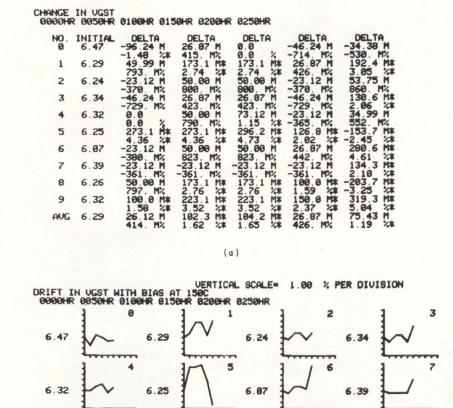


Fig 4 Memory map. Map indicates, by highlighting, which cells failed during functional test pattern



(b)

Fig 5 Tabulated and graphical life test data. Example (a) tabulates parameter variation with device life. For 10 devices,  $V_{\rm GST}$  parameter values of MOS device are tabulated along with percent of value change for five time intervals. Times within device life at which testing was performed are specified along top of display. Data can also be dis-played graphically (b). Vertical axis is in units of percent of value change; horizontal axis is in time units. Separate graphs are plotted for each of 10 devices

6.26

14.550000 14.550000 14.550000 14.550000 14.550000 14.5500000 14.66500000 14.75000000 14.95000000 14.95000000 15.15000000 15.15000000 15.22000000 15.55000000 15.55000000 15.55000000 15.566500000 15.566500000 15.566500000 15.566500000 15.566500000 15.5665000000	15.80000N 16.15000N 16.150000N 16.250000N 16.350000N 16.350000N 16.40000N 16.550000N 16.550000N 16.555000N 16.555000N 16.655000N 16.655000N 16.655000N 16.655000N 16.655000N 16.655000N 16.850000N 16.850000N 16.850000N	17.10000N 17.20000N 17.20000N 17.300000N 17.350000N 17.350000N 17.450000N 17.450000N 17.550000N 17.750000N 17.750000N 17.750000N 17.750000N 17.750000N 17.750000N 17.750000N 17.80000N 17.9950000N 17.9950000N 18.050000N 188.050000N	18.25000N 18.30000N 18.30000N 18.450000N 18.50000N 18.7550000N 18.850000N 18.850000N 18.950000N 18.950000N 19.100000N 19.10000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N 19.120000N	19.55500000X 19.5550000X 19.55500000X 19.555000000X 19.555000000X 19.5665000000X 19.5665000000X 19.56650000000X 19.56650000000X 19.56650000000X 19.56650000000X 19.56650000000X 19.56650000000X 19.5660000000X 19.56600000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.5660000000X 19.56600000000X 19.5660000000X 19.56600000000X 19.5660000000X 19.56600000000X 19.56600000000X 19.56600000000X 19.56600000000000X 19.5660000000000X 19.56600000000000X 19.5660000000000000X 19.56600000000000000000X 19.56600000000000000000000000000000000000	Fig 6 Tabulated statistical data and distribution of analyzed data. Partial list of propagation delay values (a) for a lot of devices in raw form is difficult to digest. Detailed analysis on tabulated propagation delay values shows visually (b) how devices are distributed	
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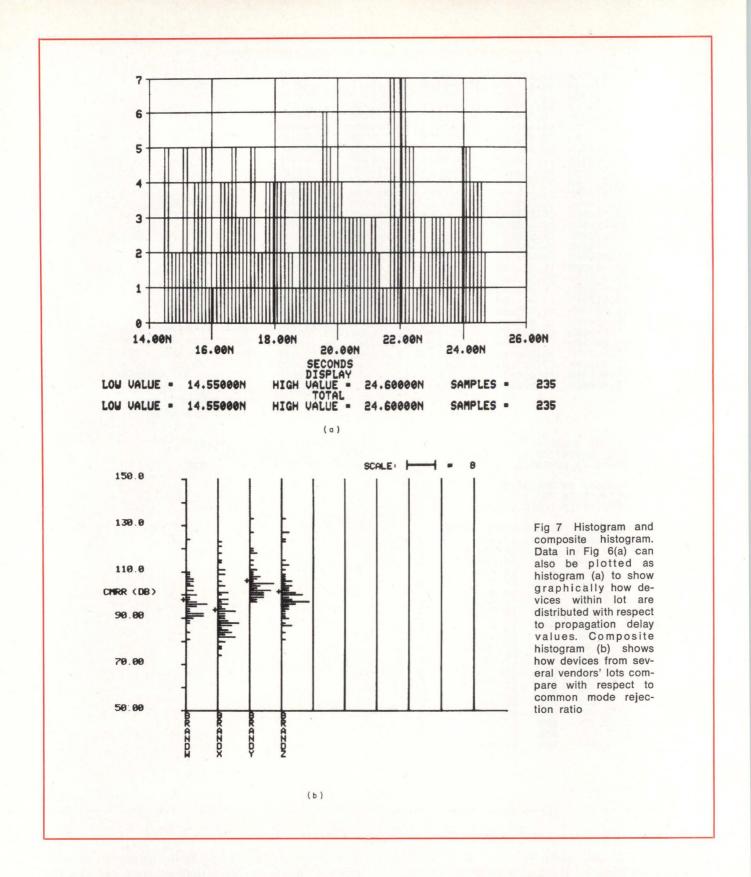
(b)

data presented in this undigested state, it is hard to evaluate distribution and to compare vendors adequately. By performing statistical analysis on these data, the distribution is easier to detect [Fig 6(b)]; however, two or more vendors' devices would still be difficult to compare.

# Histograms

Data in Fig 6(a) can also be configured as a histogram [Fig 7(a)]. A histogram displays the distribution with-

in a device lot of a single device parameter; it scales values of the parameter of interest along one axis and the number of devices falling into each measured parameter category along the other axis. Histograms show where devices cluster (for some parameters, defective devices tend to cluster in areas separate from good devices), thereby making them easier to sort out from the lot. A histogram of each lot of devices also allows comparison of vendor parameter distributions. Availability of statistical distribution data of device parameters al-



lows the designer to decide whether the device fits the specifications and to predict vendor yield. A composite histogram [Fig 7(b)] shows individual histograms of each lot of devices side-by-side so that lots can be compared simultaneously. In a similar manner, the life test results of Fig 5 can be plotted as composite histograms to show how a device parameter varies over the life of the test.

# Composite Shmoo Plots

For device populations, composite shmoo plots can be used to determine the yield expected from a lot of devices when certain minimum and maximum values are used as the specified parameters. Composite shmoo plots—generated by combining data from several shmoo plots—are surface maps of 3-dimensional information. The de-

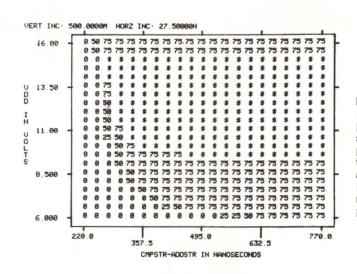


Fig 8 Composite shmoo plot. Safe operating region of lot of devices within limits of two parameters— $V_{\rm DD}$  and address access time—are shown with dollar sign (\$) indicating where all passed the testing. Other parameter pair locations are defined with percentiles. In this example, designer chose to round percentiles to multiples of 25; however, he could have selected more tightly defined regions, such as rounding percentiles to multiples of 10 or 5

fined operating region indicates where all the tested devices passed; in Fig 8, dollar signs establish this region. Other parameter pair locations have the percent of devices passing indicated as a percentile number (eg, 75, 50, 25). After the areas (\$\mathscr{\phi}\$) where all devices have not passed are known, further study, and use of other forms of data reduction, should uncover the design problem.

# Scatter Plots

A scatter plot reveals the general relationship between two parameters. It traces the value of one parameter as a function of a second parameter for several devices, and it helps the designer determine where acceptable devices cluster for establishing a good device region. A leastsquares-linear fit is performed on the data set, and the

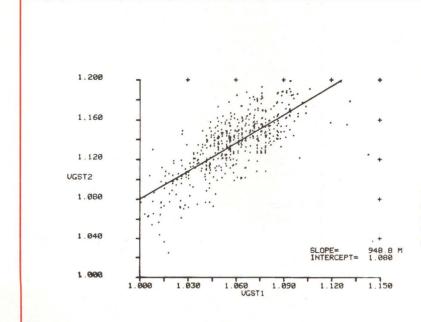


Fig 9 Scatter plot. Dot on this particular scatter plot indicates individual device values for  $V_{\rm GST1}$  versus  $V_{\rm GST2}$ . Least-squares-fit curve summarizes how devices tend to operate

best fitting line is drawn. This is the only attempt that this type of data reduction makes at determining a specific relationship from the data presented. However, scatter plots help the designer to visualize correlations between two parameters considered independent; in many cases, they are not, but a change in one causes a change in the other.

Designers can use scatter plots to measure and compare different vendors' devices, to test unknown devices, and to screen out bad devices. Fig 9 is a scatter plot of threshold voltage readings. Note that defective devices can be screened out by testing the device and comparing parameter values to determine whether they fall in the established good device region.

# **Data Analysis**

The described data reduction and display methods help the designer to decide which tests are essential and which are not. Then, actual limits of device performance can be compared with expected worst-case conditions that the device is likely to encounter. Through a parameter-by-parameter comparison of device performance limits versus worst-case performance demands, the designer can determine which parameters are critical to safe device operation. Time and cost can then be saved by testing for only those parameters that ensure that the device embodies the desired requirements.

## **Data Reduction Software**

A high level language, similar in format to FORTRAN or BASIC, used in preparing test and data analysis programs should minimize the time required for program development and, therefore, should provide more efficiency than an assembler code or macroinstructions. With a high level language, the program designer writes fewer statements than with assembler code; the higher the level of the statement, the greater the portion of the complete test the statement implements. An English-like programming language with familiar words, such as LOOP, IF, CONNECT, and WAIT, projects the intent of each command on a first encounter; provides familiar formats, such as loop counters, conditional branching, subroutines, simple variables and arrays, and equations written in mathematical forms; and offers program self-documentation. With the same language directed toward both device testing and data reduction problems, designers can write test program and data processing routines to meet particular application requirements. A flexible data reduction package presents data in a format the designer understands, and makes specialized displays easy to produce. Basic routines already exist, and the high level language provides quick program preparation.

Versatile test system software provides efficient procedures for entering and then modifying test programs, data analysis procedures, and test patterns. Program lines may be deleted, inserted, moved, and copied with simple commands; in addition, files can be merged. Test pattern editing capabilities range from modification of a single data bit to entire data rows and columns.

A data reduction software package should permit versatile acquisition and reporting of test data, as well as easy creation and execution of test programs, by providing standard routines for the types of data reduction discussed in this article, such as statistical analyses, histograms, and curve, 3-dimensional, and shmoo plots. With sophisticated automated testers, these standard routines should not require further system programming; it should only be necessary to give the test system the correct command and to indicate which data file to analyze. Logged data are then rapidly converted to easy to read graphics, allowing analyses of large amounts of data through visual scanning. After a one-time collection, data can be presented in several different visual and hardcopy formats, for permanent records of device characteristics.

Handling data processing with the same computer that controls test system hardware avoids delays and associated costs of using offline equipment. Using a second computer may involve a second language, and analyzed data may not be immediately available. Operators have to transfer gathered data to the second computer, process them and return them to the designer. Test systems that use the same computer allow data files to be kept in the same format and automated data input/output operations to be set up. In addition to lower cost, automation means that less time is consumed since data is manipulated without operator intervention.

Offline data reduction also entails the cost of writing and maintaining specialized software. For example, most computers do not have routines to make specialized shmoo plots. However, automated test systems exist that include this type of software, keep it updated and compatible with previously created data files, and provide diagnostic assistance, which are significant cost-saving factors.

With built-in data reduction capability, test system results may be depicted immediately on a graphics display terminal or reported on a line printer during execution of device test programs. Since format can be determined under test program control, presented data can be custom-tailored for the application. For extensive data analysis, information contained in the data files should be available immediately upon completion of testing.

An automated test system with multi-user foreground/background architecture should provide data reduction while not adversely affecting system throughput. This architecture should permit test programs to run in what is called the foreground, while operations such as data reduction and program development occur in the background, during the time the test system controller is idling and test program instructions are being executed (Fig 10). The controller routinely encounters natural pauses and time gaps that exist in the execution of the real-time foreground test program. These pauses occur frequently during hardware operations, such as reed

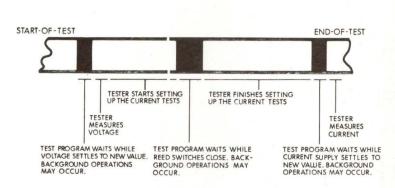


Fig 10 Foreground/background processing. With foreground/background architecture, central processor takes advantage of idle time during test program execution to perform background tasks, such as data reduction on previously created data files. Test program operating in foreground has priority. Shaded areas illustrate controller time slots available for background operations

switch settling and power supply slewing and settling. With true foreground/background operation, these time gaps are not wasted; rather, they are available for performing background tasks. Since data can be processed while testing continues, device testing and data analyzing are efficiently implemented.

# **Automated Test System**

A versatile, computer-controlled automated test system (Fig 11) can perform parametric, functional, and dynamic tests on complex devices such as Mos and bipolar shift registers, central processing units, RAMs, read-only memories (ROMs), calculator chips, microprocessors, and complex logic arrays. For these tests, the test system forces required voltage or current, and measures resultant current or voltage. Accuracy is obtained by differential measurement techniques to enhance resolution and minimize ground loop interference, by Kelvin sensing to minimize the effects of lead and contact resistances, and by a driver guard to minimize the effects of lead capacitance.

To exercise a functional test, the test system forces or compares data on the device bus pins during every clock cycle. Many devices have outputs with either a high impedance state or a don't-care state. To accommodate these states, the test system inhibits the drive function or masks the compare function. A complex device may have several data buses, each of which may require different timing; therefore, the automated test system needs multiple programmable clock phases.

In addition, the test system must be able to generate lengthy test patterns either during the test or prior to testing. Some test patterns can be described by simple algorithms while others are nearly random in nature. A sophisticated test system must provide effective methods of pattern generation to free the designer from this timeconsuming task.

To operate this test system, the operator selects the appropriate test program for the device under test (DUT) on a test station control unit. Then, after device insertion, the operator presses the start button to run the test. Upon completion of the test, the appropriate pass, fail, and sort indicators tell the operator what action to take. The test station can also be equipped with automatic handlers for device insertion and sorting. Addition of an environmental handler allows testing the device in simulated, final-product operating conditions.

A test system with multiple graphics terminals allows several users to analyze data and develop test programs simultaneously. A variety of peripheral devices provide flexible data input/output operations and allow test programs to be recorded on several media.

# Summary

An automated test system with both device characterization and data reduction capabilities produces a volume of device data in a short time that is not available from manual methods; in addition, data are supplied in easy to comprehend formats. In manually manipulated data, mistakes inevitably arise and results come slow. An automated test system speeds device evaluation; test results are obtained, processed, and analyzed quickly. Increased numbers of devices for each device type can be evaluated with significant time and cost savings. While data are being reduced for effective presentation, true foreground/background system architecture permits device testing to proceed without interruption.

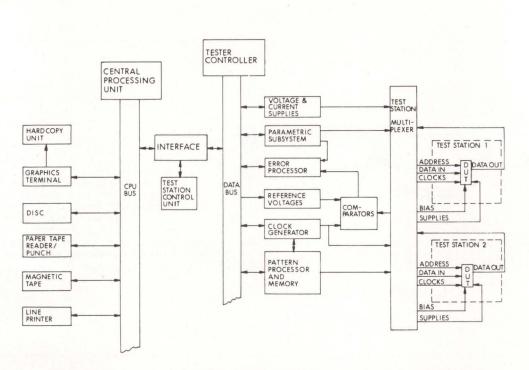


Fig 11 Automated tester. Versatile, computer-based automated test system includes several test stations (point at which device under test is actually probed). Under program control, specific bias, clock, and signal input stimuli are applied to device, and parameters of resulting outputs (time, amplitude, logic operation) are measured. Tester controller data bus communicates with CPU bus, which, in turn, is used for overall system control, program input, and background data reduction. Virtually any standard computer I/O device can be interfaced

Certain techniques for data reduction, such as curve, shmoo, 3-dimensional, and contour plots, and memory maps, are best suited for individual device data. Other techniques, including histograms, composite plots, and scatter plots, are suited for the reduction of device population data. Each of these techniques has its advantages, emphasizing the device relationship that the designer wants to investigate.

By using an automated test system with a versatile data reduction software package, a designer can have test data presented in a visual format that is readily understood and is best suited for the application. The designer can then design rapidly, easily, and accurately with the acquired data.

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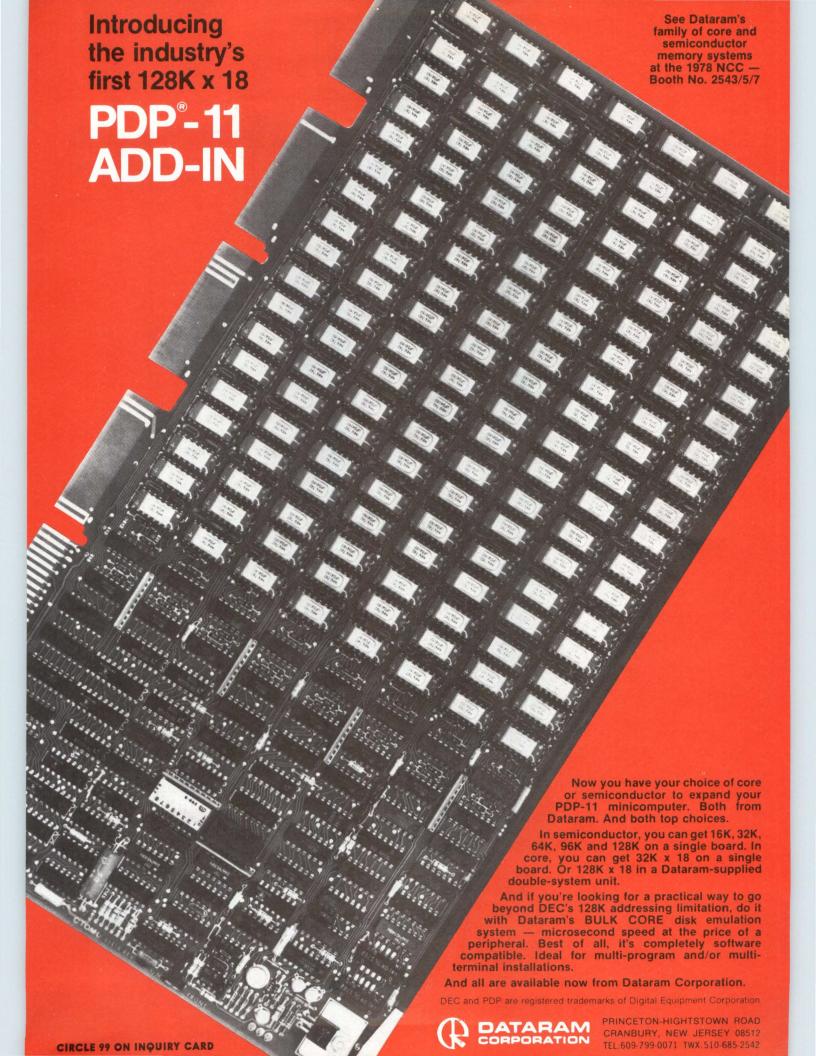
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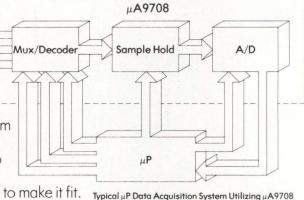
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# SINGLE ERROR CORRECTING CODE MAXIMIZES MEMORY SYSTEM **EFFICIENCY**

When applied to memory systems, derived algorithm generates a single error correcting code with a maximum partial double error detection capability for increased protective redundancy. Additional double error information is obtained without the need for an extra check bit and at minimal hardware cost.

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Reliable memory systems can be designed either by using highly reliable but expensive components or by employing inexpensive protective redundancy in terms of a single error correcting code that uses redundant check bits. The degree of reliability can be increased if this protective redundancy matches the failure mode of the memory system. Presently, use of semiconductor memory is increasing because of lower cost, higher speed, higher density, and better long-term reliability compared with core memories. Semiconductor readwrite memory chips are available in n-word x 1-bit configurations (where n = 256 through 16,384 words). For memory systems built with these chips, a single-bit failure in a word is more probable than a multiple-bit failure. Therefore, a single error correcting code is quite effective in increasing system reliability.1,2,3

For memory systems in need of increased reliability, a single error correcting and double error detecting (SEC-DED) code can be incorporated. This code needs an additional check bit to indicate overall parity.3 Double error information, when detected, can be designed to interrupt the computer which, in turn, can display the failure mode.

Inherently, a single error correcting code has the potential of partial double error detection. Without using an extra check bit, as necessary in a SEC-DED code, a modified SEC code is capable of detecting an appreciable percentage of total double error possibilities. Since variation exists in the amount of double error detection, to maximize memory system efficiency, an algorithmcalled a single error correcting and partial double error detecting (SEC-PDED) code—has been evolved that generates a code for correcting all single errors and detecting a maximum number out of the total possible double errors.

This SEC-PDED code requires only as many check bits as are needed in the SEC code, while approaching the reliability of the SEC-DED code. Moreover, extra hardware for the implementation of the SEC-PDED code is minimal.

# Background

To correct a single-bit error, information in the form of check bits is required to address the bit in error. As check bits are equally prone to failure, they are required to address themselves also, in case of error. Absence of error should indicate a null selection. For a computer memory system with a specified word length, the number of check bits needed for an SEC code can be determined by the Hamming relationship.3 For example, for

a 16-bit computer, five check bits are needed. Thus, 16 + 5 or 21 bits are required for addressing and for indicating a no-error condition. This is commonly referred to as a 21, 16 code. A SEC-DED code for a 16-bit computer needs one more check bit to indicate overall parity, thus increasing the total bit length to 22.

With five check bits in a SEC code, 2<sup>5</sup> or 32 different bit patterns (called syndrome patterns or SPS) can be formed. Again, the all-0 bit pattern normally represents the no-error condition. Of the remaining 31 SPS, 21 are associated with the required 21 address bits (data plus check bits), leaving 10 unused patterns. The possible utilization of these unused SPS in the SEC code initiated an investigation from which the SEC-PDED code evolved.

In a 21-bit memory, if 2-bit failures are considered, there will be 210 distinct double error possibilities, calculated as follows. The first bit can form 20 different pairs with the remaining 20 bits, the second bit can form 19 different pairs, and so on. By adding the pairs  $(20+19+18+\ldots+1)$ , a sum of 210 is obtained. Therefore, whenever a double error occurs, such that the modulo-2 addition of the two vector patterns corresponding to the two bits in error results in one of the 10 unused SPs, that double error can be detected.

This derived algorithm generates a class of SEC-PDED codes with maximum PDED capability. Given the number of data and check bits, this algorithm directly constructs the associated SPS (called parity check matrices or PCMS). Since it is possible to have a class of PCMS with the same maximum PDED capability, the algorithm is also capable of generating all the PCMS.

The probability of errors remaining undetected can be reduced greatly by combining the single error correction process with the detection of a large percentage of double errors. Extra hardware needed to achieve this capability is minimal when compared with that needed for a SEC-Hamming code. For example, for a 21, 16 SEC-PDED code, only one extra 10-input NAND gate is needed. The 10 unused outputs (active low) of the SP decoder, in this case, are fed to the extra NAND gate, which is activated in the presence of any detectable double error.

As the cost per bit of memory is steadily decreasing, the trend of employing a SEC or a SEC-DED code in memory systems is gradually increasing to provide better system reliability. The PDED capability of a SEC-PDED code with a long word length is very high, eg, 72.96% for a 71, 64 code. Thus, a memory system using a 71-bit word length employing SEC-PDED code can benefit from the advantage of having more than 72% of possible double errors detected without the requirement of an extra memory bit.

# Single Error Correcting Code

A SEC code is generated by appending certain parity check bits to the data bits. These check bits are generated with the help of the parity check matrix of the SEC code. Whenever there is a single error, the check bits will indicate the position of the bit in error; moreover, they will indicate a no-error condition by an all-0 pattern.

Assume that d is the number of data bits and m is number of check bits; then the check bits must describe d + m + 1 different bit patterns. Thus

$$2^{m} \ge d + m + 1 \tag{1}$$

Eq (1) is the well-known Hamming relationship.<sup>3</sup> For 16 data bits (d), the number of check bits (m) is 5 from the equation.

# **Mathematical Representation**

Assume that vector v is a coded message of order n (ie, d + m) and H is a parity check matrix of order  $m \times n$ ; then

$$vH^{T} = 0 (2)$$

where H<sup>T</sup> is the transpose of the H-matrix.<sup>4</sup> If the H-matrix is represented as

then HT is

$$\begin{array}{cccc} h_{11} & h_{21} & h_{31} \\ h_{12} & h_{22} & h_{32} \\ h_{13} & h_{23} & h_{33} \end{array}$$

More clearly, if v is equal to  $a_1, a_2, \ldots, a_i, \ldots a_n$ , where  $a_1, a_2, \ldots, a_i, \ldots, a_n$  correspond to each bit position value of the coded message, and the element in row i and column j of H is denoted by  $h_{ij}$ , Eq (2) implies:

$$\sum a_i h_{ij} = 0$$
 for all i values (3)

This equation generates the generalized parity check bits. For each row of H, the number of 1s in v corresponding to the number of 1s in that row (the "dot product" of v and each row of H) will be an even value. For example, assume that u = code vector of order n,

Fig 1 Parity check matrix for single error correcting code with 16 data (D) bits and five check (C) bits. Each column ( $S_1$  to  $S_5$ ) represents the syndrome pattern (SP) associated with corresponding data and check bits

and e = error vector of order n. If an error occurs, then the resulting code is u + e (modulo-2 addition). Therefore, the syndrome pattern for u + e is

$$SP = (u + e) H^{T} = uH^{T} + eH^{T}$$
 (4)

From Eq (2),  $uH^T = 0$ ; therefore, the resulting syndrome pattern for Eq (4) is

$$SP = eH^{T}$$
 (5)

If e corresponds to an error (eg, in bit k),  $SP = eH^T = h_k$ , ie, the corresponding pattern in parity check matrix-H.

Fig 1 shows the PCM for a 21, 16 SEC code. Note from this PCM that one portion corresponds to data bit positions  $D_1$  through  $D_{16}$ , and the other to check bit positions  $C_1$  through  $C_5$ . Syndrome patterns ( $S_1$  through  $S_5$ ) for this code correspond to the data plus check bit positions. Distinct 5-bit columns exist in the PCM, corresponding to each data bit position in the code word (eg,  $D_1 = 00011$ ). The check bit portions of the SPs contain a single 1 bit, located in different check bit positions. Therefore, check bits can be individually generated.

# **Encoding and Decoding with PCMs**

Two PCM stages of operation occur from the implementation point of view. First the data word is encoded using the data portion of the PCM; second the encoded data is stored in memory. When reading from memory, the stored data (information plus check bits) are used to generate all possible SPS for the entire PCM.

From Fig 1 and Eq (3), if  $C_1$  through  $C_5$  are check bits and  $D_1$  through  $D_{16}$  are data bits to be written into memory,

 $C_1\,=\,D_{12}\oplus\,D_{13}\oplus\,D_{14}\oplus\,D_{15}\oplus\,D_{16}$ 

 $C_2 = D_5 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{11}$ 

 $C_3 \, = \, D_2 \oplus D_3 \oplus D_4 \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{15} \oplus D_{16}$ 

 $C_4\,=\,D_1\oplus D_3\oplus D_4\oplus D_6\oplus D_7\oplus D_{10}\oplus D_{11}\oplus D_{13}\oplus D_{14}$ 

 $C_5 = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus D_{12} \oplus D_{14} \oplus D_{16}$  (6)

Fig 2 Parity check matrix for single error correcting and double error detecting code for 16 data (D) bits and six check (C) bits. Check bit  $C_{\rm 0}$  represents overall parity bit, useful for double error detection. Each column ( $S_{\rm 1}$  to  $S_{\rm 0}$ ) represents SP associated with corresponding data and check bits

where  $\oplus$  represents the logical operation exclusive-or. Generation of Eq (6) can be explained as follows. If check bits are generated using the data portion of the PCM, each check bit will indicate the parity of data bits for which the PCM has a 1 in the corresponding column in the pertinent row. After check bit generation, the encoded word will follow Eq (3) by definition.

When reading from memory, if  $C_1$ ' through  $C_5$ ' are check bits,  $D_1$ ' through  $D_{16}$ ' are data bits, and  $S_1$  through  $S_5$  are the SP bits generated,

 $S_1 = D_{12}' \oplus D_{13}' \oplus D_{14}' \oplus D_{15}' \oplus D_{16}' \oplus C_{1}'$ 

 $S_2 = D_{5'} \oplus D_{6'} \oplus D_{7'} \oplus D_{8'} \oplus D_{9'} \oplus D_{10'} \oplus D_{11'} \oplus C_{2'}$ 

 $\begin{array}{l} S_3 \,=\, D_2{'} \oplus D_3{'} \oplus D_4{'} \oplus D_8{'} \oplus D_9{'} \oplus D_{10}{'} \oplus D_{11}{'} \oplus D_{15}{'} \oplus D_{16}{'} \\ \oplus \, C_3{'} \end{array}$ 

 $S_4 \,=\, D_{1}{'} \oplus D_{3}{'} \oplus D_{4}{'} \oplus D_{6}{'} \oplus D_{7}{'} \oplus D_{10}{'} \oplus D_{11}{'} \oplus D_{13}{'} \oplus D_{14}{'} \oplus C_{4}{'}$ 

 $\begin{array}{l} S_5 \,=\, D_1' \oplus D_2' \oplus D_4' \oplus D_5' \oplus D_7' \oplus D_{\theta'} \oplus D_{11}' \oplus D_{12}' \oplus D_{14}' \\ \oplus D_{16}' \oplus C_5' \end{array} \eqno(7)$ 

In the generation of Eq (7), the SP bits indicate the parity of encoded data bits (data plus check bits) for which the entire PCM (data plus check portion) has a 1 in the corresponding position in the pertinent row. A distinct SP (each column of the PCM) is associated with each data and check bit. In case of no error,  $S_1$  through  $S_5$  will be all 0s; otherwise a specific syndrome pattern will be generated corresponding to the bit in error.

# SEC Code Example

Assume that a 16-bit data word is being used with the PCM of Fig 1. The data word to be written into memory is 1111 1111 1111 1111. From Eq (6),  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$ , and  $C_5 = 11110$ . Therefore, the encoded data word is 1111 1111 1111 11110.

Assume that the fourth most significant bit (MSB) position  $(D_4)$  of the data word is in error. Hence, the data word read from memory is: 1110 1111 1111 1111 11110. From Eq (7),  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $S_5 = 00111$ . In Fig 1, this generated SP corresponds to the column at the fourth MSB position  $(D_4)$ . Note that the bit position in error is easily identified using this approach. In practice, the erroneous bit is usually reversed immediately after detection. In binary logic, a bit is either 0 or 1; consequently, if a bit is known to be erroneous, ie, it is detected to have changed state, bit reversal will correct the error.

# Single Error Correcting and Double Error Detecting Code

To construct a single error correcting and double error detecting (SEC-DED) code for increased reliability, one check bit is added to the number of check bits needed for a SEC code. Continuing the SEC example, a sixth bit is added to the five check bits. This additional check bit checks all the previous positions (data bits plus SEC check bits) using an even parity check.<sup>3</sup>

In Eq (5), if e corresponds to a double error, the SP equals  $eH^T = h_k + h_1$  (modulo-2 addition), where bit k and bit 1 are in error. Fig 2 represents the PCM for a 22, 16 SEC-DED code. By utilizing this PCM, the check and SP bits can be generated directly without writing the associated equations. Accordingly,  $C_1$  through

 $C_5$  and  $S_1$  through  $S_5$  will follow Eq (6) and (7) because the Fig 1 PCM is a subset of the Fig 2 PCM. Extra bits  $C_6$  and  $S_6$  are generated as follows.

$$\begin{array}{lll} C_6 = D_1 \oplus D_2 \oplus \ldots \oplus D_{16} \oplus C_1 \oplus C_2 \oplus \ldots \oplus C_5 & (6a) \\ S_6 = D_{1'} \oplus D_{2'} \oplus \ldots \oplus D_{16'} \oplus C_{1'} \oplus C_{2'} \oplus \ldots \oplus C_{5'} \oplus C_{6'} & (7a) \\ \text{where } D_1, \ D_2, \ldots, \ C_1, \ C_2, \ldots, \ D_{1'}, \ D_{2'}, \ldots, \ \text{and} \ C_{1,'} \\ C_{2,'} \ldots, \ C_{6'} \ \text{are as defined in Eq (6) and (7).} \end{array}$$

# SEC-DED Example

Assume that a 16-bit data word is used with the PCM of Fig 2. The data word to be written into memory is 1111 1111 1111. From Eq (6) and (6a),  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$ ,  $C_5$ , and  $C_6 = 111100$ . Therefore, the encoded data word is 1111 1111 1111 1111 111100. Assume that when the data word is read, the two MSBs ( $D_1$  and  $D_2$ ) are in error. Hence, the encoded data read is 0011 1111 1111 1111 1111 1111 111100.

From Eq (7) and (7a),  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ ,  $S_5$ , and  $S_6 = 110000$ . Because  $S_6 = 0$  and  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $S_5$  are not equal to 0, a double error is indicated. This observation can be generalized to cover all three possible error cases as follows:

(1	) No	error	S.	through	Se	= 0
( I	1 110	CIIUI	N1	unougn	26	- 0

(2) Single error 
$$S_6 = 1$$
;  $S_1$  through  $S_6$  indicate the corresponding SP

(3) Double error 
$$S_6 = 0$$
;  $S_1$  through  $S_5 \neq 0$ 

In practice, the double error indication in computer memory may be used to interrupt the main computer and to indicate failure information.

# Single Error Correcting and Partial Double Error Detecting Code

If e corresponds to a double error, ie, in bit k and bit 1, from Eq (5), the resulting

$$SP = eH^{T} = h_{k} + h_{1} \text{ (modulo-2 addition)}$$
 (8)

Detection of this double error is possible only if

$$h_k + h_1 = h_1 \pmod{\text{modulo-2 addition}}$$
 for no  $h_1$  in  $H(PCM)$  (9)

In a SEC code, double errors for which Eq (9) is valid will be detectable. For some double errors, modulo-2 addition of associated SPS may yield one of the SPS used in the PCM. In these cases, the double errors will exercise a false single error correction.

The SEC-PDED code maximizes the probability of detection of double errors (explained in the algorithm section). Hence, although it uses the same number of memory bits as a SEC code, it is more powerful. The SEC-PDED code will have a minimum possible number of double errors that violate Eq (9). Thus, it will have a minimal chance of false single error correction (in case of undetectable double errors) when compared with SEC code. In addition, in case of detectable double errors, the SEC code will fail, whereas the SEC-PDED code will behave as a SEC-DED code. Moreover, PDED capability becomes higher with an increase in unused syndrome patterns; for a 65, 58 SEC-PDED code generated by the algorithm, PDED capability turns out to be more than 95%. This high reliability is achieved without the need for an eighth check bit, as would have been necessary

for a SEC-DED code. For a very large memory system, saving one memory bit while still almost equaling the power of double error detection are highly attractive system characteristics.

# SEC-PDED Example

Assume that a 16-bit data word is used with the PCM of Fig 1. The data word to be written into memory is 1111 1111 1111 1111. The SEC encoded data word is 1111 1111 1111 1111 11110, as defined previously.

Case I —Assume that a double error has occurred in the  $D_{11}$  and  $C_1$  positions. Thus, data read from memory are 1111 1111 1101 1111 01110. From Eq (7),  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $S_5 = 11111$ . This SP is not used in any column of the PCM of Fig 1; hence, it satisfies Eq (9). Thus, this double error will be detected.

Case 2—Assume that a double error has occurred in the  $D_1$  and  $D_6$  positions; therefore, data read from memory is <u>0</u>111 1<u>0</u>11 1111 1111 1111 11110. From Eq (7),  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $S_5 = 01001$ . Since this SP corresponds to the column associated with  $D_5$  in the PCM of Fig 1, this double error will not be detected.

From Eq (9), it is clear that to maximize the PDED capability of a SEC code, the H-matrix PCM should be chosen so that the number of double errors for which the SP equals one of the columns of the H-matrix is minimized. In the 21, 16 SEC code [refer to the PCM in Fig 1], out of the total of 25 or 32 sps, 21 distinct sps are associated with the 16 data bits plus five check bits. The 5-check-bit sps (C1 through C5) should have column patterns containing a single 1 bit to avoid interdependence of check bit generation.3 The all-0 pattern is reserved for the no-error condition. For the 16 data bit positions, any 16 distinct SPs will produce a 21, 16 SEC code. There are 32 - 5 - 1 or 26 sps from which the required 16 sps can be chosen. Using a combination formula, the choice of 16 out of 26 terms generates an astronomical figure. The term MCN symbolically indicates selection of N elements out of M possible elements at a time when all such distinct combinations are possible. M is called factorial M and indicates the product term of M x (M-1) x (M-2) ... x 3 x 2 x 1. Therefore  $^{\mathrm{M}}\mathrm{C}_{\mathrm{N}} = \frac{\mathrm{M!}}{(\mathrm{M} - \mathrm{N})! \; \mathrm{N!}}$ 

 $=\frac{\mathbb{I}M\,(M-1)\,(M-2)\,\ldots\,(M-N+1)\,(M-N)\,(M-N-1)\,\ldots\,(3)\,(2)\,(1)\,\mathbb{I}}{\mathbb{I}\,(M-N)\,(M-N-1)\,\ldots\,(3)\,(2)\,(1)\,\mathbb{I}\,[\,N(N-1)\,(N-2)\,\ldots\,(3)\,(2)\,(1)\,\mathbb{I}}\,\,(10)$ 

Fig 3 Complement matrix of parity check matrix in Fig 1. For five check bits, out of possible 32 different SPs, all-0s pattern is reserved for no-error indication, 21 are used in Fig 1 PCM, and remaining 10 are presented here. They are obtained by simply eliminating 22 SPs that are used from 32 total possible patterns

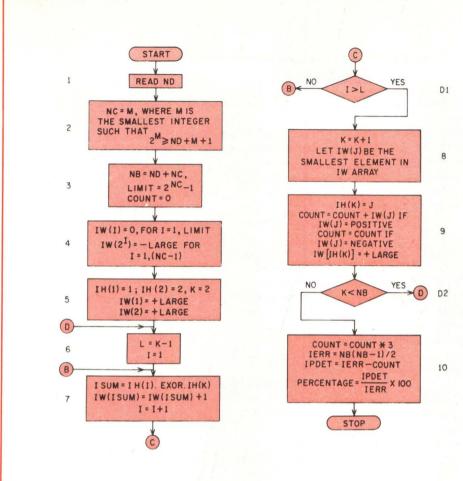


Fig 4 SEC-PDED algorithm. By computer simulation, algorithm generates the parity check matrix for single error correcting and partial double error detecting code with maximum partial double error detection capability for memory word of arbitrary length. It also calculates percentage of double error detection

Out of the  $^{26}C_{16}$  possible PCMs for an SEC code, a subclass of PCMs should be selected so that out of the  $^{21}C_2$  (or 210) possible double errors, the maximum number of errors should utilize the 10 unused SPS [Fig 3].

In hardware, the resultant 5-bit column or SP is used to address the bit in error. In case of no error, the five bits will be all Os. For a single error, the resultant sp will be the same as the SP associated (by the PCM) with the bit in error. The need for state reversal of the bit in error (for correction purposes) necessitates decoding the 5-bit SP into 32-bit information. In the case of a single error, the associated decoder output will be active (low). A set of 21 exclusive-NOR gates (two input gates) will have one input from the memory output and the other input from the decoder output. Active (low) output of the decoder will invert the bit in error. In case of no error, the memory output will ripple through without inversion. The remaining 10 outputs of the decoder indicate the presence of detectable double errors. These 10 outputs are fed to a 10-input NAND gate to generate a double error (high) signal, which can be used to interrupt the computer.

#### Algorithm

An algorithm is presented in the form of a flowchart (Fig 4) that allows selection of a PCM (or a class of PCMs) for a SEC-PDED code with maximum PDED capability. This general algorithm is also applicable for a

code of any length. It generates the PCM and calculates the percentage of PDED capability for a particular code.

Basic requirement for a particular code is that it should generate a PCM in which the maximum number of column-pair modulo-2 additions yield column vectors that are outside the PCM. A convention for representing column vectors by decimal numbers is introduced for convenience. For example, the column vector

is considered as the binary number 10100 and is represented as 20<sub>10</sub>, its decimal equivalent. Modulo-2 addition of two column vectors, 20<sub>10</sub> and 5<sub>10</sub>, for example, yields \*\* and is represented by 17<sub>10</sub>, following this convention.

#### Flowchart

The first step in the algorithm (Fig 4) reads the number of data bits (ND); the second step generates the number of check bits (NC) as determined by Eq (1).

Term NB, defined in the third step as the sum of ND and NC, indicates the number of columns in the PCM for a particular code. Decimal value of any column vector in the PCM can range from 1 to LIMIT, where LIMIT =  $2^{NC} - 1$ . The all-0 column vector is eliminated from the total number of possibilities, 2NC, because it is used for the no-error condition. The term COUNT indicates the number of double errors that cannot be detected; it is initialized in Step 3. Step 4 introduces a weight matrix IW, where IW(I) gives the weight of the ith element. For example, initially, all possible (LIMIT) column vectors are considered as suitable candidates for the PCM to be generated. This is represented by generating a weight matrix IW that corresponds to all the columns possible (from 1 to LIMIT); initially they are all set to 0.

An implementation consideration stipulates that all check bit positions should contain a single 1 bit. Thus, in Step 4, all corresponding IW(2<sup>I</sup>) elements in the weight matrix IW are set to the —LARGE quantity. Later, the selection criterion of an element from the IW-matrix for transfer to the IH-matrix, the actual PCM, is made on a least count basis. Therefore, these single-1-bit columns are purposely selected.

In Step 5, actual selection of column vectors starts. Initially, the first two elements, 1 and 2, are selected. Immediately after selection, corresponding weights in IW for these two elements are changed to +LARGE so that they are not reselected. The number of column vectors currently selected (K) is initialized to 2 in the first iteration.

Step 6 puts L equal to K-1; in the first iteration, L=1, and I is initialized to 1. Step 7 generates the modulo-2 sum of IH(K) with all IH(I) values for I=1 to K-1, and in each case, increments the weight of the corresponding sum in the IW matrix by 1. Term K is incremented in Step 8. Then, the selection criterion is applied. It is assumed that the element of the IW matrix with the least count is the best choice at this step. Thus, the element IW(J) is determined. If more than one element with the same least count exists, selection of any one of them will yield a PCM with the same PDED capability. Hence, the choice is versatile.

In Step 9, the selected IW(J) is accepted as the next column vector IH(K) of IH. After selection, IW(IH(K)) is changed to +LARGE to avoid any further selection of this column. In the IW-matrix, the count corresponding to all elements is initialized to 0. Then, in the process of selecting elements for the IH-matrix (the PCM), the corresponding counts undergo three types of change. First, when an element is selected in IH, the corresponding count in IW is made very large, thereby eliminating the possibility of its reselection. Second, the single-1 elements are initialized to -LARGE, so that they are immediately selected. Third, some elements of IW, at any phase, will indicate a particular count of 1, 2, etc. At any stage of selection, the selected columns, when added (modulo-2 addition) pairwise, will yield some other columns. Elements of the IW-matrix corresponding to the resulting columns are incremented by 1 at every stage.

It can be argued that when two vector elements (columns of the PCM) are added (modulo-2 addition), they result in a third vector. In the course of generating the PCM, assume that three elements—t<sub>1</sub>, t<sub>2</sub>, and t<sub>3</sub>—have

been selected so far, and that  $t_1 + t_2 = t_4$ ,  $t_2 + t_3 = t_5$ , and  $t_1 + t_3 = t_6$  (modulo-2 addition). Now, if the counts corresponding to t4, t5, and t6 are considered according to present terminology, each value of t1, t2, and t3 will have a +LARGE count, and the values of t4, t5, and te a count of 1 each. In terms of selecting the next probable element out of t4, t5, and t6, all of them have the same count of 1. This indicates that if any one of them is chosen, its selection will lead to the failure of three double error detections. Assume that t4 is selected. Then, out of t1, t2, t3, and t4, if t1 and t2 are both in error, the modulo-2 sum will yield t4. Hence, according to Eq (9), this double error will not be detectable. In case the t1, t4 or t2, t4 pair is in error, again, these two double errors will not be detectable because they yield t<sub>2</sub> and t<sub>1</sub>, respectively [refer to Eq (9)].

For any three elements, only three distinct pairs exist. Consider that  $t_1$ ,  $t_2$ , and  $t_4$  are three distinct elements; then  $t_2$  and  $t_4$  can be added to  $t_1$ , thus yielding two distinct pairs. Pairing  $t_2$  and  $t_4$  yields the third and last possible pair. From the combination formula, Eq (10),  ${}^3C_2$  yields

$$\frac{3!}{(3-2)!2!} = \frac{3!}{1!2!} = \frac{3 \times 2 \times 1}{1 \times 2 \times 1} = 3$$

By generalizing this argument, it can be stated that for every selected element of the IH-matrix, its COUNT (from IW matrix) indicates COUNT\*3 undetectable double errors. Any time an element is selected, its count is added to the present total count and, finally, it is multiplied by three to indicate the total number of undetectable double errors.

Step 9 generates the total incremental count at any stage. When the compulsory single-1 elements are selected for the PCM, according to the criterion described in Step 4, its corresponding —LARGE count is effectively considered as a 0 count because the —LARGE count only mechanizes the automatic selection of these single-1 elements; it does not contribute to the actual count of undetectable double errors.

Decision box (D2) checks whether all the NB elements of the PCM are selected. If so, Step 10 computes COUNT = COUNT\*3, which gives the total number of undetectable double errors. In a memory containing NB bits, the number of possible double errors can be calculated using Eq 10.

$$^{NB}C_2 = \frac{NB!}{(NB-2)! \ 2!} = \frac{NB \ x \ (NB-1)}{2}$$

Hence, the number of detectable double errors equals the number of possible double errors minus the number of undetectable double errors. From this computation, the percentage of partial double error detection can also be calculated.

#### Algorithm Example

A practical example (Fig 5) is presented to clarify the algorithm. In this example, decimal representations of the column vectors are used. The selection of each column vector and the corresponding incremental change in the count matrix are shown at each step of the algorithm.

Initially, the counts corresponding to the single-1 columns, ie, 1, 2, 4, 8, and 16 are made equal to -LARGE

Selected Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Total Count
	- 00	- 00	0	- 00	0	0	0	-00	0	0	0	0	0	0	0	-00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	O
1	+00																															0
2		+00	+1																			100			u la							0
4				+00	+1	+1			99																							0
8			33					+00	+1	+1		+1						A														0
16									-				15.19			+00	+1	+1		+1				+1	52.							0
7			+1		+1	+1	+00								+1						-79		+1									0
11		N. S.	+1	2019	N.				+1	+1	+00	+1			+1											2.0	+1		200			0
13					+1	+1			+1	+1		+1	+00		+1														+1			0
14			+1		+1	+1			+1	+1		+1		+00	+1												+1			+1		0
19			+1										個				+1	+1	+00	+1			+1	+1			+1		+1	+1		0
21			ug.		+1	+1											+1	+1		+1	+00		+1	+1			+1		+1	+1		0
22			+1		+1	+1											+1	+1	538	+1		+00	+1	+1			+1		+1	+1	76	0
25									+1	+1		+1			+1		+1	+1	A	+1			+1	+1	+00		+1		+1	+1		0
26			+1	11					+1	+1		+1		15.1	+1		+1	+1		+1			+1	+1		+00	+1		+1	+1		0
28					+1	+1			+1	+1		+1		2	+1		+1	+1		+1			+1	+1			+1	+00	+1	+1		0
31		6	+1		+1	+1			+1	+1		+1			+1		+1	+1	1	+1			+1	+1			+1		+1	+1	+00	0
3	(·)	<b>(1)</b>	+00	<b>(1)</b>			(F)	(1)			( <del>+</del> 1)		(+1)	.(+1)		<b>(1)</b>			( <del>1</del> )		(+1)	( <del>1</del> )			(+1)	(+1)		( <del>+</del> 1)			<b>(1)</b>	8
5	1	•		(1)	+00	+1	1	0			<u>+</u>		<u>•</u>	•		•			<b>(1)</b>		(+1)	<b>(+)</b>			0	•1)		(a)			0	16
10	(f)	<u>•</u>		0			1	•	+1	+00	•		•	<b>(1)</b>	+1	<u>•</u>			<u>•</u>		<u>(1)</u>	•			<b>(1)</b>	(+1)		<u>(1)</u>			<b>①</b>	24
20	0	•	197	0		J. J.	1	1			<u>+</u>		<u>+1</u>	<u>•</u>		<b>(1)</b>	+1		<u>+</u>	+00	( <del>1</del> )	0	+1		( <del>1</del> )	<u>(1)</u>		<u>+1</u>		+1	(A)	32
24	(I)	•		(1)			(P)	0			(+1)	+1	<u>(+)</u>	(+1)		(I)		+1	<u>+</u>		(+)	(P)		+00	( <del>1</del> )	(+1)		( <del>1</del> )			0	40

Fig 5 Selecting elements for PCM. For 21, 16 single error correcting and maximum partial double error detecting code, listed data give details for selecting elements for parity check matrix, illustrating count increase of each element at each phase of selection, and indicating total count

 $(-\infty)$  for the forced selection of these columns; the remainder of the columns are assigned a 0 count, as shown in the first row of Fig 5. In each phase of selection, the counts corresponding to the resultant columns (modulo-2 addition of the selected column with all previously selected columns generate the resultant columns) are incremented by 1 to reduce the probability of selection of those elements on a least count basis.

The iterative process of column selection, when applied to the elements of the IW-matrix (1 to 31), select columns 1, 2, 4, 8, 16, 7, 11, 13, 14, 19, 21, 22, 25, 26, 28, 31, 3, 5, 10, 20, and 24. When at first, columns 1 and 2 are selected, the count corresponding to column 3 (modulo-2 addition of column 1 and column 2 yields column 3) is incremented by +1, and individual counts corresponding to column 1 and column 2 are made equal to  $+LARGE (+\infty)$  to avoid their reselection in further iterations. In the next phase, column 4 is selected, and counts of resultant columns 5 and 6 are incremented by +1. Continuing in this mode, selection of up to column element 31 is done. Since all selected column elements have a count of 0, the total count column remains 0 after selected column 31. In the next iteration, note that selected columns 3, 5, 10, 20, and 24 each have a count of 8. For example, the count corresponding to selected column element 3 (still nonselected)

can be determined by adding the corresponding column of +1 incremental counts (Fig 5).

Any one of the remaining selected column elements (3, 5, 10, 20, or 24) could have been chosen because of their identical count. In this example, selected column 3 is chosen, and the counts of all resultant columns are incremented by 1. At this stage, it can be seen that all resultant columns (result of modulo-2 addition of column 3 with all previously selected columns) are already selected and, hence, the count of each resultant element has already been changed to  $+\text{LARGE}(+\infty)$ . Thus, the effective incremental count of resultant column elements is a "don't care" condition, and it is represented by a circled +1 in Fig 3.

Final total count is 40. Therefore, COUNT = COUNT\*3 = 40 x 3 or 120 is the number of undetectable double errors. Thus, from Step 10:

IERR (number of possible double errors) = 
$$\frac{\text{NB x (NB - 1)}}{2}$$
  
=  $\frac{21 \times 20}{2}$  = 210

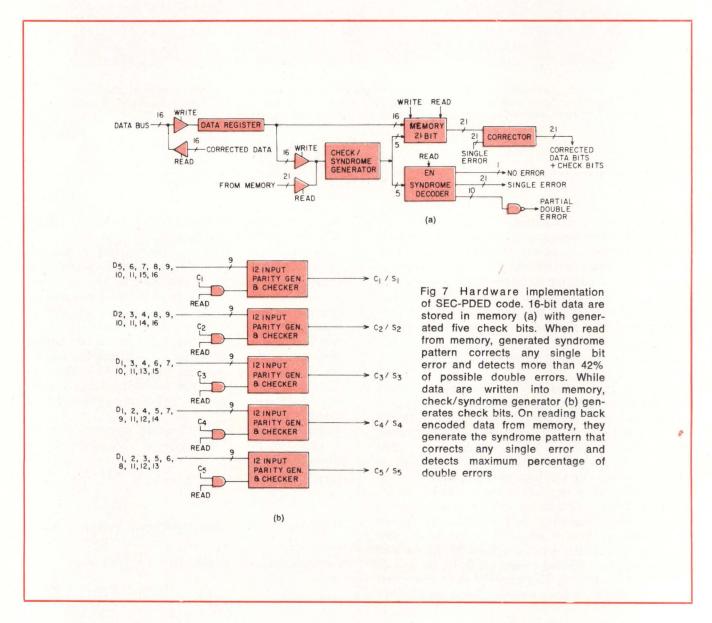
IPDET (number of detectable double errors) =  $\stackrel{2}{\text{IERR}}$  - COUNT = 210 - 120 = 90

Percentage of double error detection = 
$$\frac{\text{IPDET}}{\text{IERR}} \times 100$$
  
=  $\frac{90}{210} \times 100\% = 42.86\%$ 

Fig 6 PCM for 21, 16 single error correcting and maximum partial double error detecting code. This matrix also yields minimum achievable delay for check bit generation

#### Implementation

Considering the PCM (data portion) represented by Eq (6), it can be seen that each check bit is generated by generating the parity of those data bits for which the corresponding column in the PCM has Is in the relevant row. Depending on the number of Is in each row, that many exclusive-OR gates will be necessary for each check bit generation. According to Eq (6), C<sub>1</sub> generation needs five gates, whereas C<sub>5</sub> needs 10 gates. Therefore, C<sub>1</sub> introduces a 5-gate level delay and C<sub>5</sub> introduces a 10-gate level delay. Because encoded data (data plus check bits) cannot be written into memory until all check bits are generated, the maximum delay will be governed by the check bit having the maximum number of gates, a 10-gate level delay in this example. Hence, a PCM that has a minimum delay in check bit



generation will be most suitable. After generating a class of PCMs with SEC-maximum PDED capability, a computerized search can be conducted to obtain a matrix that satisfies the above criterion.

The PCM for a 21, 16 SEC-PDED code with maximum PDED capability and minimum gate delay for check bit generation is presented in Fig 6. Steps for generating this PCM are presented in the data of Fig 5 and follow the algorithm of Fig 4. It can be seen from the PCM of Fig 6, that each check bit generates a 9-gate level delay; ie, nine 1s are present in each row of  $D_1$  through  $D_{16}$ . In addition, this will yield a maximum PDED capability of 42.86%. Hardware diagrams [Figs 7(a) and 7(b)] illustrate the implementation of the 21, 16 SEC-PDED code, as represented by the PCM in Fig 6.

While writing into memory, the write signal is delayed [not shown in Fig 7(a)] to accommodate the delay in check bit generation. Input to the check/syndrome (C/s) generator is obtained from the data bus during write mode. The write signal enables the write 3-state buffer and inputs the 16 data bits into the C/s generator. In write mode, the C/s generator acts as the check bit generator. Also, signals C<sub>1</sub>, C<sub>2</sub>, C<sub>3</sub>, C<sub>4</sub>, and C<sub>5</sub> are disabled (made low) by the read control signal in Fig 7(b), which is low during write mode. Hence, the C/s generator generates the check bits, and encoded data are written into memory by the delayed write signal.

During reading of encoded data, input to the c/s generator is from the 21-bit memory. Signals C1 through C5 are enabled by the read control signal during read mode. The c/s generator acts as an SP generator during this mode. The syndrome decoder (SD), which is also enabled in this mode, is a 5-to-32 decoder, which can be implemented by using 3-to-8 fast decoders with active low outputs. An all-0 output indicates no error. A single error, if present, will be indicated by the corresponding SP; ie, the relevant output of the decoder will be active (low). This single-bit error indication is used in the corrector to obtain correct data immediately. A bank of 21 exclusive-NOR gates is used to implement the corrector function. One input of each gate is from memory and the other input is from the SD. In case a single error is present, the corresponding decoder output will be low, and will invert the erroneous memory data bit, thus correcting it. Normally, the data bits from memory will ripple through the corrector. Any one of the remaining 10 outputs of the SD, if active, will indicate one of the detectable double errors. These 10 outputs are fed to a 10-input NAND gate, which will indicate the partial double error automatically.

In Fig 8, maximum PDED capabilities (in percentage) versus code length (in number of bits) are presented in graphical form for five, six, and seven check bits. For five check bits [Fig 8(a)], the maximum PDED capability of the SEC-PDED code for 12 data plus five check bits is more than 80%. For six and seven check bits (ie, 27 data plus six check bits and 58 data plus seven check bits) [Figs 8(b) and 8(c)], maximum PDED capabilities are more than 90% and 95%, respectively.

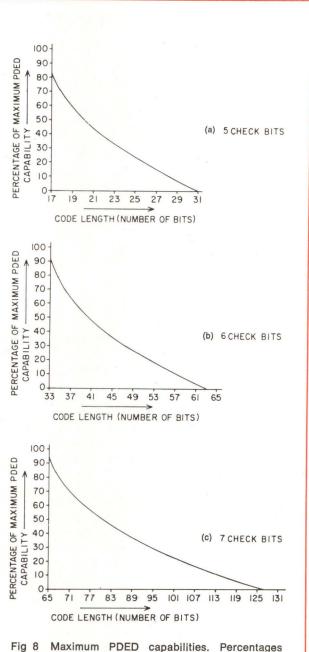


Fig 8 Maximum PDED capabilities. Percentages of maximum partial double error detection capability of single error correcting and maximum partial double error detecting codes with different code lengths are shown for five, six, and seven check bits

PCMs with SEC-maximum PDED capability are presented in Fig 9. These PCMs have been generated by computer simulation of the algorithm of Fig 4. Presented using a decimal representation (explained earlier), each PCM is a general type, representative of the PCM for the corre-

1	2	4	8	16	7	11	13	14	19	21	22	25	26	28	31	3	5	9	15
17	23	27	29	6	10	18	30	12	20	24									
											(a)	5 C	HEC	K BI	rs				
1	2	4	8	16	32	7	11	13	14	19	21	22	25	26	28	31	35	37	38
41	42	44	47	49	50	52	55	56	59	61	62	3	5	9	15	17	23	27	29
33	39	43	45	51	53	57	63	6	10	18	30	34	46	54	58	12	20	36	60
24	40	48																	
											(b)	6 C	HEC	K BIT	rs				
1	2	4	8	16	32	64	7	11	13	14	19	21	22	25	26	28	31	35	37
38	41	42	44	47	49	50	52	55	56	59	61	62	67	69	70	73	74	76	79
81	82	84	87	88	91	93	94	97	98	100	103	104	107	109	110	112	115	117	118
121	122	124	127	3	5	9	15	17	23	27	29	33	39	43	45	51	53	63	65
71	75	77	83	85	89	95	99	101	105	111	113	119	123	125	6	10	18	30	34
46	54	58	66	78	86	90	102	106	114	126	12	20	36	60	68	92	108	116	24
40	72	120	48	80	96														
											(c	7 0	HEC	K RI	TS				

Fig 9 General parity check matrices. Corresponding to five, six, and seven check bits, PCMs are shown in distinct formats with each decimal number representing column vector. Each PCM is generated by following algorithm; number of elements in each matrix is equal to  $2^{\rm NC}-1=$  LIMIT. To get particular PCM of length NB (NB = ND + NC), general PCM for corresponding NC is chosen, and first NB columns (ie, first NB decimal numbers) will give PCM yielding single error correction with maximum partial double error detection capability

sponding check bit. Each is generated by the described algorithm, and the number of elements in each is equal to  $2^{\rm NB}-1={\rm LIMIT}.$  To get a particular PCM of fixed NB (NB = ND + NC), the general PCM for that NC is chosen, and the first NB columns (ie, first NB decimal numbers) give the PCM yielding the SEC code with maximum PDED capability.

For example, consider a computer with a memory of 12-bit words. From Eq (1), it is known that five check bits are necessary for SEC capability. The associated SEC-maximum PDED PCM is obtained by considering the first 12 plus five of 17 columns of Fig 9(a), which gives a PCM of 1, 2, 4, 8, 16, 7, 11, 13, 14, 19, 21, 22, 25, 26, 28, 31, and 3 (represented in decimal form). From Fig 8(a), the corresponding maximum PDED capability for a code length of 17 bits is found to be 82%. For a computer memory requiring six or seven check bits, the corresponding PCM can be found from Fig 9(b) or Fig 9(c) in a similar way. Fig 8(b) or Fig 8(c) will yield maximum PDED capability for the particular PCM.

Conclusions

A single error correcting code is capable of partial double error detection for increased reliability with minimal extra hardware expense. The partial double error detection capability of a SEC code also can be maximized by suitable choice of PCM. The given algorithm can generate a class of PCMs with SEC and maximum PDED capability. This algorithm has been thoroughly computer simulated and successfully tested.

A computer memory with single error correction and maximum partial double error detection (employing a 21, 16 sec-maximum pded code) for a minicomputer system has been successfully implemented in the laboratory. Computer memory systems, instead of using sec code, can use sec-maximum pded code. This code will detect a sizeable percentage of total possible double errors, which the sec code will not be able to detect.

In addition, SEC-PDED code minimizes the number of undetectable double errors with the least chance of false single error correction (in case of undetectable double errors). Hence, for practical memory systems, employing protective redundancy, this code is quite attractive.

The algorithm, although very general in nature, does not consider the criterion of minimal delay in check bit generation. Hence, generalizing the algorithm even further is possible.

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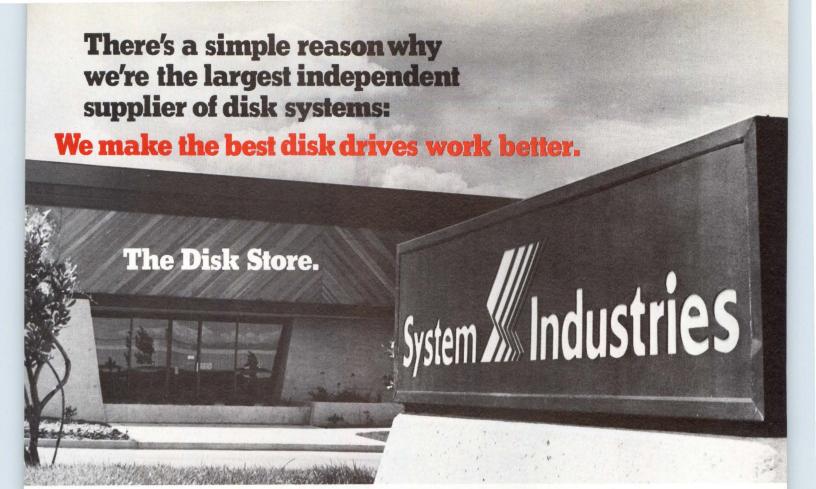
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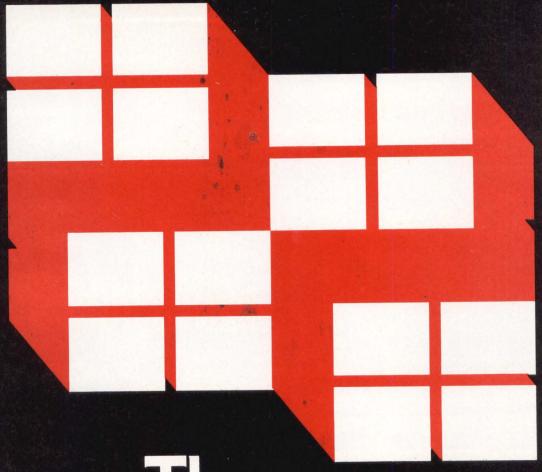
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# INTERFACING CALCULATOR CHIPS AS MICROCOMPUTER PREPROCESSORS

Adapting a calculator chip to a microcomputer system to execute intricate mathematical computations with reduced software costs involves interface design considerations of logic levels and impedances, supply voltages, and data command circuitry, and produces slightly slower arithmetic operations

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M icrocomputer systems that are effectively utilized for data processing and control applications require prohibitive programming to carry out complex numerical, scientific, or engineering calculations. For computations of this type, a commercially available calculator chip can be interfaced with the microcomputer system, if a relatively slow calculation speed is acceptable. The interface circuitry is not extensive, but it is dependent upon the characteristics of the particular calculator chip chosen. However, the design approach can be adapted to most chip types. When properly designed, the calculator chip and its support circuits serve as a peripheral module or subsystem to be attached to the microcomputer system. The microcomputer routes operands in binary-coded decimal form to the calculator subsystem, dictates the sequence of calculations to be executed, and controls the result readout, display, or entry into memory. The calculator subsystem's capabilities obviate the need for the programmer to construct machine language algorithms for each of the mathematical operations required in the application.

Since the extent of the required interface circuitry is not strongly dependent upon the chip type, the

designer should choose a calculator chip with powerful computational capabilities. Chips in this category include the MOS Technology MPS 7529-010 and 7529-103 and the National Semiconductor MM 57103 units. For flexibility, a multikey scientific calculator chip is used. This class of chip provides complex engineering functions as well as more basic arithmetic operations. Scientific notation on the readout provides a wide range of valid calculation results.

#### Calculator Subsystem Principles

Conventional structure of a handheld calculator unit is illustrated in Fig 1. A 12-digit display is assumed to be employed for result readouts, while the keyboard provides for operand entry and manual selection of operations in a calculation sequence. Viewed from left to right, the display consists of a mantissa sign (digit position 1), eight mantissa magnitude digits (positions 2 through 9), an exponent sign (position 10), and two exponent magnitude digits (positions 11 and 12). Digit 1 may also be used to indicate an overrange condition. In most applications, each display

digit is made up of seven segments and a decimal point. Segment-select signals appear on calculator chip outputs SG1 through SG8. These signals appear in sequence for display positions 1 through 12. When a valid digit or character is present on the segment-select lines, a pulse appearing on one of the digit-select outputs (DS1 through DS12) designates the display digit being read out of calculator chip memory and activates the digit driver for that display position. Outputs normally connected to the display are cyclical, and are maintained unless the calculator chip is performing an operation or lapses into a power-save mode.

Pulses on the digit-select outputs also are used to interrogate the keyboard for selected functions or operand digits. When a key is depressed, a keyboard switch is closed and one of the 12 digit-select pulses is returned on one of the four data and command entry lines (EN1 through EN4). This line and the time of occurrence of the returned pulse within the display cycle are decoded in the calculator chip to direct the initiation of the selected calculation operation or entry of the selected digit.

#### Interfacing the Calculator Chip

A primary design consideration in the adaptation of any calculator chip is the establishing of interface communications between the calculator subsystem and the microcomputer system. Since most calculator chips are metal-oxide semiconductor (MOS) devices and most microcomputers, such as those built around the Intel 8080 and Motorola M6800 microprocessors, produce and accept transistor-transistor logic (TTL) signals, voltage levels appearing on the calculator chip inputs and outputs must be adjusted. This task is made easier when the calculator chip source supply voltage, V<sub>SS</sub>, level is set to 5 V, which is the normal TTL supply level, and the drain supply voltage, VDD, is adjusted to provide the required supply voltage differential on the chip, typically 15 V. Mos transistor outputs designed into many calculator chips can be connected directly to one or more TTL inputs if a resistor is connected between the output itself and one of the supply voltages. The resistor value depends upon the supply voltage and the "on" impedance of the Mos transistor.

Two common types of Mos outputs are shown connected to a standard TTL input stage in Fig 2. In the upper output configuration, the Mos transistor can be considered as either an open circuit or a relatively low impedance to  $V_{\rm SS}$ . The external resistor  $(R_1)$  is connected to  $V_{\rm DD}$  and its value is chosen so that the TTL input is held near ground when the Mos transistor is off (essentially an open circuit). This resistor value can be made lower than required since the clamping diode protects the TTL input.

In the lower output configuration, a second Mos device is used as a load resistor on the active output transistor. The output appears as a relatively low impedance to  $V_{\rm SS}$  or a relatively high impedance to  $V_{\rm DD}$ . The added resistor  $(R_2)$  is connected to  $V_{\rm DD}$  to assist the load resistor in pulling the TTL input near ground when the output transistor is off. Obviously, other output configurations are possible; the designer must determine the circuit needed to achieve com-

patibility in each application, based upon the output provided by the calculator chip and the characteristics of the applied load.

In some applications, the calculator chip with  $V_{\rm SS}$  and  $V_{\rm DD}$  supply levels as described can accept TTL levels directly on the entry inputs. If direct connection is impossible and a simple resistor addition cannot effect compatibility, the designer should consider using an Mos-to-TTL level shifter integrated circuit (IC). Since only the four entry lines must be level shifted, a single IC package should suffice.

#### Calculator Subsystem Ready Signal

If the calculator subsystem is to act as a peripheral device attached to a microcomputer, the subsystem must respond to write and read commands issued by the microcomputer. Within the calculator subsystem, a write operation can be defined as the successful entry of a single digit, sign, or decimal point, or the successful initiation of a single functional step in a calculation. A read operation can be defined as the latching of a single selected digit (of the 12-digit display cycle) into the output register of the calculator subsystem. Since the microcomputer should not direct the calculator to initiate any activity until the previously commanded action is completed, the subsystem must produce a ready signal indicating its availability for another read or write operation.

A subsystem ready indication can be derived from calculator chip outputs normally connected to the display. As described under Calculator Subsystem Principles, these outputs are cyclical for a given displayed result, and control each digit position of the display in sequence. Most calculator chips will blank the display while a calculation is in progress. Blanking is accomplished by holding all segment-select outputs off while the digit-select outputs function normally. Therefore, the subsystem ready signal can be produced by circuitry monitoring each display cycle for the presence of a valid output. Once this is detected, the calculator subsystem is ready to accept the next command in the operational sequence.

The circuit shown in Fig 3 can be used to develop the calculator subsystem READY signal. The digit- and segment-select signals shown are assumed to have been converted to TTL levels and are active high. Flip-flop 1 (FF 1) is set on the leading edge of the DS 2 pulse and is reset when SG 8, the decimal-point segment-select line, goes high. The status of FF 1 sets the condition of FF 2 during display of the tenth digit (DS 10). If no decimal-point selection (SG 8) appears after FF 1 is set, FF 2 is set on the rise of the DS 10 pulse; otherwise FF 2 is reset by DS 10. The READY signal is obtained from the  $\overline{Q}$  output of FF 2, and is updated near the end of each display cycle.

Some calculator chips lapse into a low power mode when no operation has been requested or no data entry made for a prescribed length of time, typically 40 to 75 s. Power saving is accomplished by blanking the normal display. Operation of the chip in this mode is usually indicated by display of an abnormal character in one display position. One possible low power mode indication would be a decimal point displayed

in position 12. Since the calculator chip is ready to respond to a microcomputer request in the low power mode, the READY indication must accommodate this condition. The circuit producing the indication must be expanded to detect the presence of the display output peculiar to the low power mode, and to activate the READY line whenever that output is detected.

Incorporation of a time delay that prevents the READY signal from rising to the high state immediately when valid display outputs return can improve the circuitry in Fig 3. A delay of one or more display cycles would assure that the calculator subsystem has returned to a stable condition before another data entry or operational command is accepted.

#### **Write Operation**

To interface the calculator chip with the microcomputer, entry steering can be accomplished by a multiplexer-demultiplexer tandem circuit under microcomputer control. One arrangement is represented by the calculator subsystem block diagram of Fig 4. A 6-bit entry control word (EC 1 through EC 6) is supplied by the microcomputer. Bits EC 1 through EC 4 choose one of the 12 digit-select signals for passage through the multiplexer. Bits EC 5 and EC 6 control the particular entry line on which the selected digit pulse is passed into the calculator chip. The demultiplexer is enabled only when a WRITE pulse is issued by the microcomputer. Therefore, an entry control word can be latched into one or more of the microcomputer output ports before the WRITE command is given.

Many calculator chips are designed to guard against key contact bounce by requiring that any entry request must persist unchanged for two or more keyboard interrogation cycles. The duration of the WRITE pulse should exceed the keybounce persistance requirement of the selected chip. No WRITE pulse should be initiated unless the READY signal from the calculator subsystem is present.

Although entry of a data digit or operational command is accomplished by a single microcomputer control word, the exact nature of that word depends upon the connection between a digit-select output and an entry input. One possibly inconvenient aspect is that the control word required to enter a particular digit will probably bear no resemblance to that digit. For example, entry of a numerical 8 into the calculator chip might be effected by connecting the DS 9 output to input EN 1. In the configuration of Fig 4, this entry is made when bits EC 1, EC 4, and EC 5 of the control word are 1s and all other bits are 0s. Therefore, the control word required for entry of an eight is octal 31 or hexadecimal 19, neither of which resembles the entered digit.

The problem is one of format conversion and can be solved either by inclusion of a table lookup operation in each programmed issuance of a control word or by a hardware addition to the calculator subsystem. The latter approach improves the subsystem's flexibility as a peripheral and reduces programming demands. A user-loaded programmable read-only memory (p/ROM) can be placed between the microcomputer and calculator chip to convert from the command format utilized

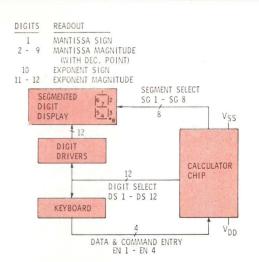


Fig 1 Conventional handheld calculator configuration. Calculator chip produces signals to interrogate keyboard periodically and to display calculation results. Same signals are utilized when chip is interfaced as microcomputer peripheral device

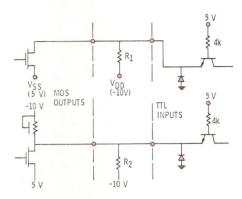


Fig 2 Interfacing MOS to TTL. Compatibility can be achieved in many applications by selective addition of resistor from each MOS output to one supply voltage

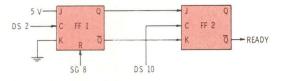


Fig 3 Development of calculator subsystem READY signal. First flip-flop detects occurrence of decimal point during readout (display) cycle, indicating that valid readout occurred and that calculator is available. Second flip-flop is reset to produce READY output if readout is valid

in the microcomputer to that necessitated by the peculiarities of the selected calculator chip.

The foregoing discussion assumed the use of a calculator chip designed for connection to a keyboard made up of single-function keys. The 12 digit-select lines and four entry lines permit the use of 48 different valid control words, not all of which may effect an entry. Some chips allow the individual keys to be used for two different functions. On the Hewlett-Packard HP-45 calculator, for example, the same key is used for squaring and requesting the square root of the operand. The select key (prefix key) must be depressed before a square root operation can be activated. A chip designed for multifunction keys can serve in the calculator subsystem; however, command of an operation corresponding to the upper case function requires two successive write operations. The first operation indicates that the succeeding entry corresponds to the upper case.

#### **Read Operation**

Readout of a single digit from the calculator subsystem is controlled by the contents of bits EC 1 through EC 4 of the control word and by a READ command. One method of implementing the readout is illustrated in Fig 4. The eight segment-select outputs, first converted to TTL levels, serve as address inputs to a continuously-enabled inexpensive p/ROM, such as a 1702A, which converts the unwieldy 7-segment code to the designer's format. In Fig 4, four bits of the output word (8-4-2-1) provide binary-coded decimal representation of result digits, one bit (DP) indicates the presence of a decimal point, one bit (NEG) indicates the occurrence of a negative sign output, and one bit (OOR) flags the presence of an overflow indication caused by a calculation result falling outside the allowable range. Other assignments can readily be made, depending upon the capabilities of the calculator chip chosen and the format most compatible with the microcomputer.

The multiplexer-selected digit-select pulse and the microcomputer-generated READ command are combined (ANDed) to produce a LOAD pulse that latches the desired digit, in the converted format, in the sub-

system output register. Outputs from this register can be connected to a microcomputer input port and may be sampled as soon as loading has been completed. Readout of the calculator output to one display position requires, at most, one display cycle. The read operation should not be initiated when the subsystem READY signal is deactivated. An invalid and meaningless readout will be made whenever the calculator chip is in low power mode.

#### **Speed and Accuracy**

The calculator subsystem represented in Fig 4 is flexible and provides a wide range of mathematical capabilities, but the chip is not designed for speed. Rate of calculation and length of a display cycle are controlled by the clock, which is usually built into the chip and is not available to the designer. Many of the single-operand algorithms used by the chip consist of calculations of truncated power series sums. Each successive term in a power series involves raising the operand to a higher power. For example, the function sin x, with x in radians, can be expressed as

$$\sin x = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \dots$$

A particular angle's sine is determined in the chip through the calculation of each term in the series, in turn, and the addition of the term value to the accumulated sum. The magnitude of each term is tested and the calculation is terminated (series sum is truncated) when the magnitude of a term falls below a predetermined allowable error value. This type of calculation, in general, requires a long calculation time (up to several seconds), which may depend upon the magnitude of the operand.

Entry and readout of data from the subsystem also are relatively slow since both must be done serially by the individual digit. A write operation also is required for entry of a decimal point. The readout process may be shortened when the designer has ad-

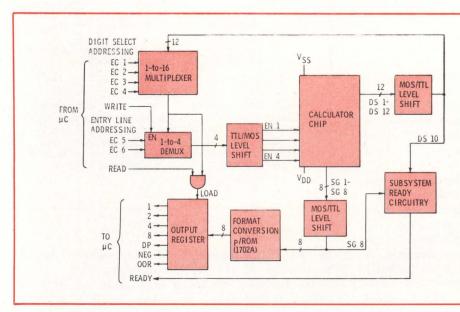
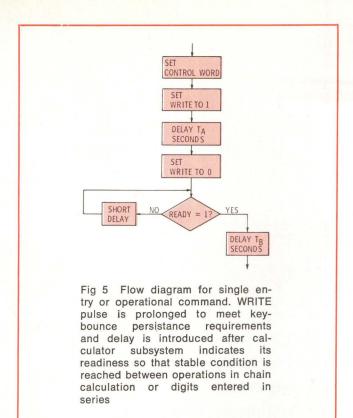


Fig 4 Calculation subsystem interfaced to microcomputer. 8-bit commands are accepted to initiate calculations and control readout of results. Selected calculations are carried out within calculator chip. Output format can be customized to meet requirements of any application



vance knowledge of the range of possible results from a series of calculations. The microcomputer program is written to read out only the necessary digits. If a calculator chip providing one or more memory locations is chosen, advance entry of frequently used constants can eliminate repetitive entries. Storage locations can be useful for holding intermediate calculation results that might otherwise, of necessity, be read out and loaded into microcomputer memory, then reentered into the calculator subsystem when needed.

Overall calculation error of a chip is a function of roundoff error and algorithmic accuracy. Calculation results generally are accurate to within several counts in the last digit of the mantissa (the eighth digit in the assumed configuration). This accuracy is more than adequate for use with most microcomputer systems.

#### Chain Calculations

The calculator subsystem is most useful as a microcomputer peripheral when it is employed in a series of calculations involving two or more numerical operands, especially those including some trigonometric and scientific functions available in scientific calculator chips. In this case, the microcomputer has to produce only a single control word and write command for each operation performed in the sequence.

Calculator chip characteristics can place some restrictions on the sequence of commands issued by the microcomputer to effect a chain calculation. In addition to the keybounce persistance requirement on the entry command, a minimum "dead" time between successive WRITE commands is imposed by some chips. A timed

sequence (Fig 5) can be used to enter each of a number of digits in an operand, or to command each of a succession of operations, if the chip has limits on both persistance and dead time. In Fig 5, TA is an interval in excess of the chip persistance requirement, and T<sub>B</sub> is a reliable downtime between WRITE pulses. Each WRITE pulse exists for TA seconds. When one WRITE pulse is completed, the following one cannot be begun within T<sub>B</sub> seconds after the calculator subsystem indicates its readiness. With the exception of the first step, which is dependent upon the entry to be made, the process represented in Fig 5 can be implemented as a subroutine stored in the memory of the microcomputer. Addition of a delay by the calculator subsystem in the generation of its READY indication was mentioned previously. If such a delay is incorporated, and if it exceeds TB seconds in length, the last step of the process represented in Fig 5 may be deleted.

#### Conclusions

Hardware design of a calculator subsystem requires a thorough investigation of the characteristics of the selected calculator chip; its implementation, however, requires minimal circuitry and is inexpensive. Power consumption of the chip is low, and since the circuitry used in its adaptation need not be of the high speed variety, overall subsystem power consumption is reasonable. A calculator subsystem added to a microcomputer system can greatly enhance computational capabilities and increase the numerical range of permitted operands. Although the system programmer must be aware of the interface requirements, the task of developing algorithms for the possibly complex calculations required is eliminated. If a microcomputer system must execute the type of calculations normally encountered in engineering and scientific activities, development of a calculator subsystem as a microcomputer system peripheral can readily be justified.

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#### **APPLICATION NOTE**

## Floppy Disc-Based Emulator Replaces Paper Tape Reader

Because of high repair rates and diminishing spare parts inventory, obsolete paper tape readers in test sets have been replaced by pin-compatible microcomputer-based disc-storage emulators, thereby preserving test console hardware, saving the existing large test data base, and simplifying operator involvement

Kenneth W. Fisher

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actory testing of electromechanical telephone switching frames and units (subframes) requires storage of large data blocks to provide the test sequence. This factory testing was previously controlled with 28-channel punched paper tape readers, originally designed for use in automatic message accounting by telephone companies, but adapted to testing applications because of availability and large storage capacity. The outdated readers are currently being replaced with more modern and efficient equipment, leaving factory test sets as the only remaining application. Therefore, tapes and spare reader parts have become more difficult and expensive to obtain.

To replace and update the automatic message accounting (AMA) readers used in factory testing, a

tape reader emulator module (TREM) has been designed. The module consists of an SBC 80/10-based microcomputer, appropriate input/output (I/O) ports, floppy-disc drive and controller, and sufficient interface circuitry to provide pin-for-pin compatibility with existing paper tape readers.

#### Background

Of the factory test sets being controlled, several similar types utilize the AMA reader, the most common being a Western Electric SID-9170. This test set contains telephone-type wire-spring relay command decoding and switching circuitry with from 200 to 800 test point access capability along with detection circuits that permit testing for ground, open, and continuity, in addition to certain transmission measurements.

The AMA reader cycle time of 62.5 ms per character is used for making timing measurements on the unit under test (UUT) with multiple dummy test lines, which provide no information to the test set, to establish the proper time interval. Failure of any test causes the reader clutch to disengage, which, in turn, halts the paper tape and stops the test. Test set lamps indicate the type of failure to the operator.

The failure must be cleared before testing can proceed; therefore, a unit or frame under test can only be considered acceptable by passing all required tests. For failure analysis, the operator must rely both on the associated test procedure documentation and the unit or frame schematic diagram in order to troubleshoot the defect. The test sequence is divided into independent



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blocks with a release-all command between blocks to clear all previous tape entries. When a failure has been cleared, the tape must be returned to the previous release-all position and the test sequence is repeated from that point.

The tape reader provides 28 punched channels (Fig 1) which are subdivided into six coded characters (A through F) decoded by the test set. Character A (three bits) determines the type of test being performed; B, C, and D (five bits) describe the terminal being selected or the type of test; and E and F (five bits) indicate the sequence number.

#### **Basic Design Considerations**

To minimize investment and preserve cost reduction, TREM modules are pin-for-pin compatible with existing tape readers and require no test-set modifications. While this precludes speed improvement through decreased cycle time, it, however, makes all test sequences previously written with dummy timing lines directly applicable to the TREM modules, saving considerable engineering redesign time. With more than 2000 codes of existing tests on file, this is an important cost saving.

A master file containing the test data base is stored on magnetic tape and processed through an offline PDP-11/45 computer system when a punched tape is required for shop use. This tape storage system lends itself equally well to a floppy discoriented system where the floppy disc replaces the paper tape. Data are stored in ASCII code on the master magnetic tape and include comments along with the AMA test code. When test control data are processed in either punched tape or floppy disc form, a printout is also generated to assist in shop troubleshooting. Although ASCII storage might be considered wasteful in terms of computer capacity, it is beneficial in floppy-disc storage in order to provide a data base that will minimize the required microcomputer processing for future diagnostics.

#### Computer and Peripheral Hardware Design

Hardware for the TREM module (Fig 2) centers around an SBC 80/10 single-board microcomputer, which

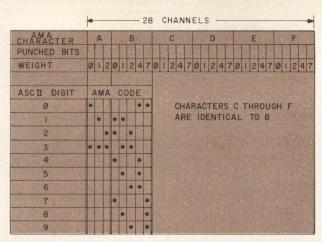


Fig 1 ASCII-to-28 channel AMA code conversion scheme. AMA code columns represent holes punched in 28-channel paper tape. Character A has unique pattern, while characters B through F are 2-of-5 code

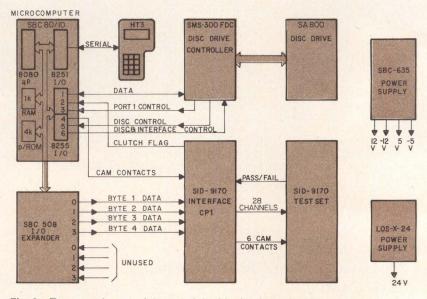


Fig 2 Tape reader emulator module block diagram. Microcomputer block consists of one circuit board which acts as system controller. Dialogue with disc is handled through disc drive controller. Expander extends interface to drive test set

contains one serial I/O port, six parallel I/O ports, and all clock and control hardware. A disc drive is used as the bulk storage device with a floppy disc replacing the paper tape as the shop-selected test sequence. The disc drive controller, by means of its microprocessor, provides all disc handshaking and requires macrolevel commands from the microcomputer to initiate each action. This technique ties up three I/O ports on the microcomputer, making additional I/O capability necessary. An I/O expander is added to provide an additional four input

and four output ports to drive the SID-9170 interface. An interconnecting point where flat cable is terminated from each peripheral device is furnished by a pluggable wirewrap board.

An HT3 handheld terminal supplies the operator interface for the microcomputer system. This terminal has an alphanumeric display with 12 output characters and a multifunction keyboard, where each key has four functions through three shift keys. At present, to allow for one-hand operation, only nonshifted characters are used.

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The TREM module is housed in a standard 19" (48 cm) wide, 10.5" (26.7 cm) high, by 21" (53 cm) deep cabinet, which is dimensionally interchangeable with the AMA tape reader. The cabinet contains a pluggable circuit pack housing for the microcomputer, 1/0 expander, and cable terminator, along with dc power supplies for ±12, ±5, and 24 V. Fan cooling is provided to dissipate peak power of approximately 250 W. Weighing approximately 75 pounds (34 kg), the cabinet has handles on both sides for transportability. Pluggable flat cable used for interwiring permits easy removal of components for maintenance.

#### Interface

The computer interface design posed interesting and challenging problems. The SID 9170 test-set command-translation circuit contains 90-Ω, 48-V relays that draw approximately 0.5 A/channel. Circuit voltage and current requirements are incompatible with the TTL provided by the I/O ports. Several interface designs were evaluated, including both electromechanical and totally solid state. A combination electromechanical/solid-state circuit offered the most economy with fewer parts and was therefore chosen. Mercurywetted relays with solid-state drivers provide complete isolation between I/O ports and test set wirespring relays. A specially designed double-sided printed wiring board mounts the interface across the rear of the TREM module cabinet. This board contains 28 channels of test data along with six channels of control contacts that are cam-operated in the AMA reader. An opto-isolator circuit on the interface board translates the reader-clutch signal from the test set into a stop/run flag for the microcomputer to monitor. This circuit allows the operator to control the test set as done previously with the paper tape reader, thereby minimizing the amount of operator retraining required.

#### Software

System-control software resides on 4k of programmable read-only memory (p/ROM) within the microcomputer board; also 1k of randomaccess memory (RAM) provides scratchpad and disc-buffer storage

for the system. Software can be divided into several discrete program modules. An ASCII-to-AMA converter program takes six ASCII characters (channels A to F) and generates four bytes to be fed to the test set, simulating 28-channel AMA code. Except for channel A, this is a two-of-five code (Fig 1), where the bits are weighted 0, 1, 2, 4, and 7. Error-checking circuitry within the test set verifies that not more than two of five bits are active in channels B, C, and D. Failure to meet this test will stop the test set and energize the check failure alarm lamp.

Since timing test accuracy must be maintained, a computer interrupt structure is used. The microcomputer clock is divided down to provide a pulse that interrupts the computer program every 0.44 ms. By counting these pulses each time an interrupt occurs, a timing sequence is set up in software that supplies test commands to the test set at the same rate as a tape reader. This maintains the integrity of any timing tests designed into the test sequence.

Disc control is accomplished with dialogue between the microcomputer and the disc drive controller; both are compatible such that a command library can be defined for use with the microcomputer. Handshaking signals are provided using the bit set/reset capability of the parallel I/o chip located on the microcomputer board. In other words, the microcomputer monitors the flags detected on one port and sends appropriate control signals through another port.

Test data are read from the disc drive a sector at a time into the microcomputer RAM. A program analyzes the ASCII code contained in the RAM buffer to extract test lines, page number of the test document, last release-all point, and certain timing information. These data are then passed to the ASCII-to-AMA converter for output to the test set.

A software module to display messages and accept keyboard information allows the handheld terminal to interface with the operator. By keying in certain codes, the operator can request diagnostic assistance from the data base stored on the disc for the particular unit being tested, or can alter the test progress as desired.

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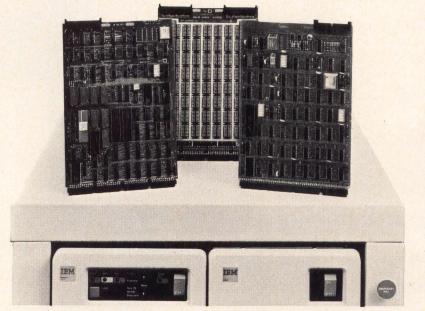
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Circle 57 for IBM: 107 for PDP-11; 108 for LSI-11; 109 for Data General; 110 for Interdata.

To aid in understanding the design of the TREM module, a typical startup and test sequence is presented. First, the unit or frame to be tested is connected to the test set with appropriate cords. The proper test sequence is then selected by inserting the associated floppy disc into the TREM module. Next the operator pushes the interrupt button on the test console to begin the test sequence. The disc head loads on track 00, sector 01 and reads the UUT number. The operator pushes any numbered key on the handheld terminal, and the system responds with the tape and issue number to verify that the proper disc has been inserted. A software routine to recognize any numbered key rather than a specific key is used to distribute key wear. The operator pushes any numbered key again, and the current page appears to the operator on the terminal showing that the test sequence has begun. If a failure is encountered, the test set will stop, displaying the test code and current page on the terminal. The defect must be cleared before the test set will accept additional test data. Using the display information on both terminal and test console, the operator can quickly locate the test sequence in the printed documentation so that troubleshooting can begin. Pushing a minus key on the terminal will direct the test sequence to return to the last release-all and to start again from that point. Pushing an asterisk key on the terminal directs the test sequence to restart from the beginning.

In the event of a failure, pushing the period key on the terminal causes the program to enter the single-step mode. Pushing any number key in this mode allows the test to be stepped one test command at a time. This capability is especially useful to an operator when troubleshooting electromechanical units where relay operation can be observed. Pushing the period key again restores the program to the automatic mode.

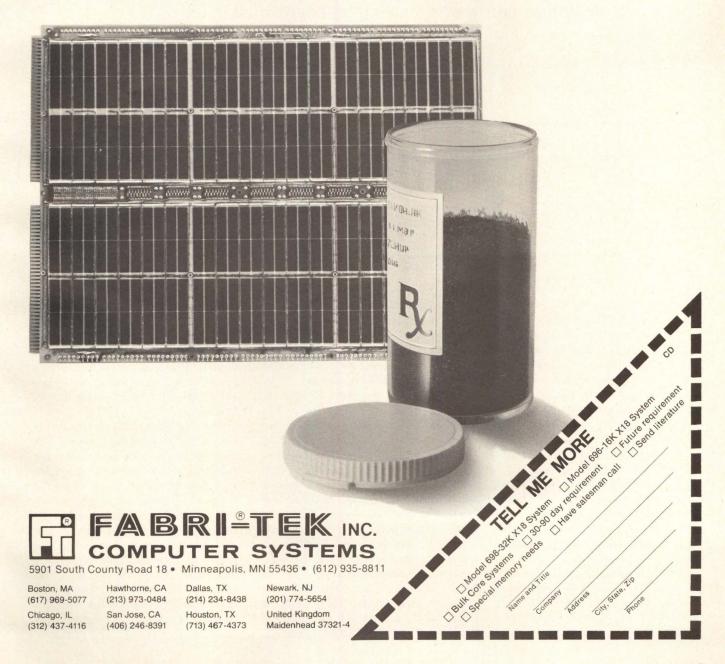
With the versatility of software control coupled with a handheld, portable terminal, the TREM module enables the operator to perform all test control functions in close proximity to the UUT without the need to move to the test console.

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#### **DESIGN NOTE**

# Low Cost Data Acquisition System Using Standard DIPs

A complete 12-bit, 16-channel data acquisition system that saves space and mounting hardware by using standard dual-in-line packages offers excellent characteristics for real-time microprocessor-based applications, at much less cost than modular approaches

John F. Munn Micro Networks Corporation, Worcester, Massachusetts

igh performance data acquisition systems can be installed on the same circuit board as a microprocessor using standard dual-in-line packaged components. In addition to saving space and eliminating the need for special mounting hardware, this approach costs 25 to 75% less than available data acquisition modules.

Data acquisition systems are multichannel, digitally addressable, analog-to-digital converters (ADCs) widely used in microprocessor-based control and monitoring systems to digitize the analog outputs of strain gauges, thermocouples, tachometers, and other transducers for input to the microprocessor. Until recently, 12-bit, 16-channel data acquisition systems have been available only in modular or printed circuit (PC) card form. This form factor is physically incompatible with other microprocessor components and often difficult to use. Special mounting hardware is usually required, as are expensive connectors and extra "offboard height" clearances.

Reducing a complete 12-bit, 16channel system (Fig 1) to a few dual-in-line packages (DIPs) is accomplished with two thin-film hybrid DIPS. The MN7130 multiplexed sample/hold (s/H) amplifier contains all the data acquisition system front-end components. Included are two 8-channel analog multiplexers. an instrumentation amplifier, and an s/H amplifier. The digitally addressable multiplexers can be connected for either 16 single-ended or eight differential input channels. The instrumentation amplifier, with a gain of 1, buffers the multiplexers and provides differential input capability, while the S/H amplifier acquires and holds the analog input signal for conversion by an ADC. Packaged in a hermetically sealed, double wide, 32-pin DIP, the S/H amplifier has all internal subsections available at the pins for application flexibility.

The ADC80 is a 32-pin, triple-wide, hermetically sealed 12-bit ADC. This converter provides excellent performance at low cost, and is complete with internal clock. The only other components required to configure a complete data acquisition system are two 10-turn trimpots, power supply bypass capacitors, and a few logic packages to interface to the particular microprocessor used. Despite its simplicity, the data acquisition system has excellent specifications: throughput is over 30,000 channels/s, aperture time is typical-

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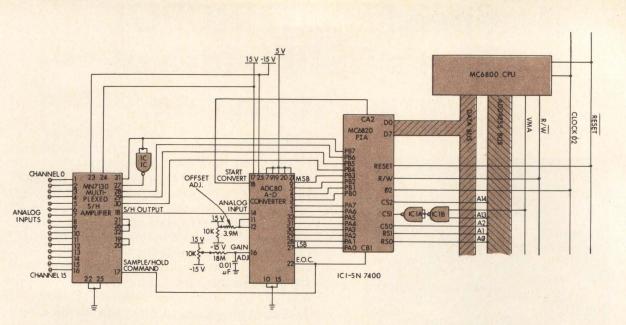


Fig 1 16-channel data acquisition system. Complex hybrids and LSI ICs reduce fabrication of high performance system to four DIPs. System provides 12-bit resolution and 30k-channel/s throughput. Design approach is less expensive than A-D modular and discrete systems

ly 60 ns, and power consumption is under 2 W.

The entire data acquisition system fabrication with interfacing requires less than a 5 by 5" (12.7 by 12.7-cm) area on a PC card. Care should be taken during layout to avoid digital runs close to the analog inputs and analog connections between the s/H amplifier and converter. Also, both units should be bypassed with  $1-\mu F$  tantalum capacitors at the power supply leads.

#### **System Application**

In a typical application (Fig 1), the data acquisition system is shown interfaced to the MC6800 microprocessor via an MC6820 peripheral interface adapter (PIA). Use of the PIA results in a simple interface requiring minimal hardware. Interfacing to other microprocessors would be similar, with specific details depending on the particular central processing unit (CPU) and input/output integrated circuits (I/O ICs) chosen. Only four IC packages are needed for the complete data acquisition system, including all interfacing logic.

The PIA (Fig 2) interfaces to the CPU with an 8-bit bidirectional data

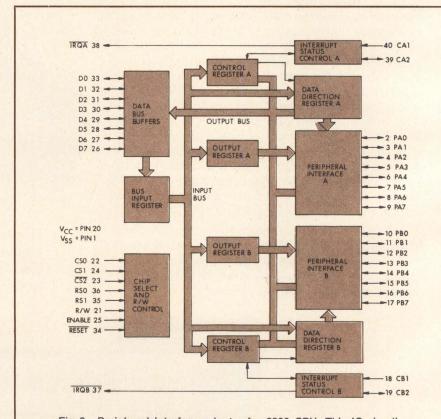


Fig 2 Peripheral interface adapter for 6800 CPU. This IC simplifies both hardware and software requirements when interfacing data acquisition systems to microprocessors. Control lines and two 8-bit bidirectional data ports are incorporated into a single package



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TABLE 1
Peripheral Interface Adapter Register Addressing

Hexadecimal		Port A Control Register Bit 2	Port B Control Register Bit 2	Addressed Register
8004	1000 0000 0000 0100	0	X	Port A data direction register
8004	1000 0000 0000 0100	1	X	Port A data buffer register
8005	1000 0000 0000 0101	X	X	Port A control register
8006	1000 0000 0000 0110	X	0	Port B data direction register
8006	1000 0000 0000 0110	X	1	Port B data buffer register
8007	1000 0000 0000 0111	X	X	Port B control register

bus, three chip select lines, two register select lines, a read/write line, and two interrupt request lines. Two additional pins are used for system reset and clock ( $\phi$ 2). Connections from the adapter to the controlled peripheral are made via two 8-bit bidirectional I/O ports and four interrupt/control lines. Any combination of bits within a port can be designated as read or write bits, and two of the four interrupt/control lines can be used to read as well as write.

Associated with each of the two I/O ports of the PIA are three registers, which provide latching and 3-state buffering. Two of these, the control and data direction registers, are loaded during program initialization and determine the mode of operation and which specific bits are designated to read or write. The third register, the data buffer register, is used for data transfer between the CPU and the peripheral being controlled.

CPU control, instead of handshaking or interrupt modes of operation, is used for this application. The relatively fast acquisition and conversion times of the data acquisition system do not allow time for enough instructions to make interrupt operation worthwhile. For the same reasons, the acquisition delay of  $10~\mu s$  and the start convert command are generated in software rather than hardware.

In all communications between the CPU and PIA, the latter is treated

as one of four memory locations (8004, 8005, 8006, and 8007).\* Status of the internal control registers is used to further differentiate whether the data direction or the data buffer register is addressed. This allows all six of the PIA internal registers to be addressed (Table 1) even though only four apparent memory locations are used. In addition, the valid memory address (VMA) output of the CPU is ANDEd with one of the chip select inputs to prevent spurious data, which may appear on the address bus during nonmemory transfer operations, from accessing the PIA. Addresses other than 8004 through 8007 could be used to address the PIA by different address bus connections to the chip select and register select lines, or with further address decoding.

Once the PIA addressing is defined, the port bit and control line assignments to the data acquisition system must be made. The four most significant bits (MSBs) of port B are assigned in the write mode and are used to address the 16 possible analog input channels for conversion. The remaining four bits of port B are used to read the four MSBs of converted data. All of port A is used to read the remaining eight least significant bits (LSBs) of converted data. Assignment of the individual bits to the read or write mode is made by loading the port's data direction register during program initialization. Logic 0 in a specific bit sets the corresponding bit of the data buffer for the read mode, and logic 1 for the write mode.

In addition, two of the four interrupt/control lines are used. Signal CA2 is used in the write mode to provide the start convert command pulse to the data acquisition system. Signal CB1 is used in the read mode to detect the falling edge of the system's end-of-conversion (EOC) output, which indicates that the conversion is completed and data are valid and ready to be read. Assignment of the interrupt/control lines is also determined by the information in the two PIA control registers (Fig 3).

#### System Software

Software instructions (Table 2) show both the subroutine needed to initialize the PIA and the subroutine needed to convert a given analog channel. Instructions listed for addresses 0010 through 002A are used to load the 6820 PIA control and data direction registers. These registers define the adapter's mode of operation and the read/write assignment of the individual port bits. This subroutine requires execution only once, on power-up or at the beginning of the application program.

Instructions shown for addresses 0030 through 0050 are used to ad-

<sup>\*</sup>All memory locations listed in this note are in hexadecimal notation.

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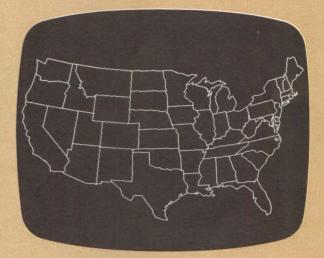
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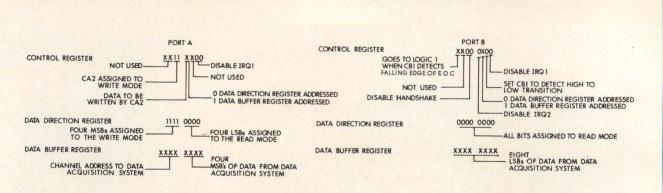


Fig 3 PIA register bit functions. Individual bits in the control registers of ports A and B determine their 1/O and control line functions. Thus, read or write data mode, as well as two interrupt lines to data acquisition system, are easily programmed

TABLE 2
Subroutines for Servicing Data Acquisition System

Address	Contents	Instruction	Address	Contents	Instruction	Comments
0010	86	LDA A #\$30	0030	( B7	STA A \$8006	
0011	30		0031	80		
0012	B7	STA A \$8005	0032	06		
0013	80		0033	01	NOP	Delay while analog sections of data
0014	05		0034	01	NOP	acquisition system settle
0015	B7	STA A \$8007	0035	01	NOP	
0016	80		0036	01	NOP	
0017	07		0037	86	LDA A #\$3C	Generate Start Convert pulse
0018	7F	CLR \$8004	0038	3C		
0019	80		0039	B7	STA A \$8005	
001A	04		003A	80		
001B	86	LDA A #\$FO	003B	05		
001C	F0		003C	86	LDA A #\$34	
001D	B7	STA A \$8006	003D	34		
001E	80		003E	B7	STA A \$8005	
001F	06		003F	80		
0020	86	LDA A #\$34	0040	05		
0021	34		0041	OC	CLC	Loop until PIA detects falling edge of
0022	B7	STA A \$8005	0042	B6	LDA A \$8007	data acquisition system EOC output
0023	80		0043	80		
0024	05		0044	07		
0025	86	LDA A #\$04	0045	49	ROLA	
0026	04		0046	24	BCC \$0042	
0027	B7	STA A \$8007	0047	FA		
0028	80		0048	B6	LDA A \$8006	Load four MSBs from PIA
0029	07		0049	80		
002A	39	RTS	004A	06		
			004B	84	AND A #\$OF	
			004C	OF		
			004D	F6	LDA B \$8004	Load eight LSBs from PIA
			004E	80		
			004F	04		
			0050	39	RTS	

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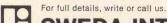
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dress, command conversion of, and retrieve the data from a given analog input channel. The sequence of operations is as follows: the subroutine is entered from the main program at address 0030 with the desired analog channel address, in binary, stored in the four MSBs of accumulator A. Instruction 0030 loads the address into the four MSBs of PIA port B to address the desired data acquisition system channel. The next four instructions generate 8 µs of the required 10-µs acquisition delay. The LDA instruction at address 0037 generates the remaining 2 µs of acquisition delay, needed to allow the analog portions of the data acquisition system to acquire the input signal. In addition, the instructions at addresses 0037 through 0040 are used to generate the 2-μs wide convert command pulse from the adapter's CA2 control line to the data acquisition system. Instructions in addresses 0041 through 0047 are used to test bit 7 of PIA control register B. This bit will be set to logic 1 when the adapter's CB1 control line detects the falling edge of the data acquisition system's EOC output. The remaining instructions are used to load the digital answer from the data acquisition system into CPU accumulators A and B. The subroutine is exited with the four MSBs of the answer stored in the four LSBs of accumulator A, and the remaining eight bits

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stored in accumulator B.

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"MC6800 Microcomputer System Design Data," RCA Corp, Somerville, NJ

"MC6800 Microprocessor Programming Manual," RCA Corp, Somerville, NJ

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#### **MICROCOMPUTER INTERFACING:** INTEGER MULTIPLICATION AND DIVISION

Peter R. Rony and David G. Larsen

Virginia Polytechnic Institute and State University

Jonathan A. Titus and Christopher Titus Tychon, Inc

Since microprocessors like the 8080 and 6800 do not have multiplication and division instructions, subroutines that contain addition and subtraction instructions (discussed in last month's column, pp 168-169) must be written to perform these operations. Typical paper-andpencil decimal and binary multiplications of two different sets of numbers are shown in Fig 1. The "mechanics" of multiplication are similar in these two examples. As the multiplicand is multiplied by larger and larger powers of ten or powers of two, the result of the multiplication has to be shifted to the left by one, to increase the significance of the result.

00100110 × 596 × 00011011 00100110 6144 9216 00100110 00000000 + 5120 610304 00100110 00100110 00000000 00000000 00000000 000010000000010

Fig 1 Decimal and binary multiplication

00001110 10011011 1011 10000 - 1011 1011 Fig 2 Binary division 1011 00001

To multiply two binary numbers, the 8080 must examine the multiplier, one bit at a time. If the bit is a logic 1, the multiplicand is added to the partial sum (initially 0). If the bit examined is a logic 0, then the multiplicand is not added to the partial sum. Regardless of whether or not that addition takes place, the partial sum must be shifted one bit position after each bit in the

multiplier is examined.

To keep the 8080 multiplication software (Example 1) as simple as possible, a subroutine has been written that multiplies two 8-bit numbers. These two numbers must be stored in the 8080 D and E registers, and the 16-bit result will be stored in registers B and C (register pair B). When the MP88 subroutine is called, register pair B is cleared, because it will be used to store the partial sum and final result of the multiplication. The L register is loaded with the number of bits in the multiplier: octal 010, hexadecimal 08, or decimal 8. At NXTBIT, the multiplier contained in register D is moved to register A, shifted once to the right, and saved back in register D. These instructions shift a single bit of the multiplier into the carry so that the state of the bit (logic 1 or 0) can be tested with software instructions.

If the state of the carry after the shift is a logic 0, the multiplicand is not added to the partial sum; JMP to NOADD (no addition) is executed. If the carry is a logic 1, the IMP to NOADD is not executed. Instead, the multiplicand contained in register E is added to the partial sum

in register pair B.

At NOADD, the 16-bit number contained in register pair B is shifted to the right by one bit position. The multiplier's bit count contained in register L is then decremented by one. When this bit count is decremented to zero, the 8080 will return from the MP88 subroutine, with the 16-bit result of the multiplication in register pair B. If the bit count is nonzero, the JMP to NXTBIT is executed so that another bit in the multiplier can be tested and any additions performed.

Multiplication of two 8-bit binary numbers was performed by an add and shift algorithm. Binary division, which is more complex than multiplication, can be performed by a subtract and shift algorithm; the division is

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# EXAMPLE 1

### 8-Bit x 8-Bit Multiplication Subroutine

MP88,	LXIB 000 000 MVIL 010	/Set the register pair that will hold the /result of the multiplication to /000 000 (hexadecimal 0000) /Load L with 8 (decimal), the bit count /or the number of shifts to take place
NXTBIT,	MOVAD RAR MOVDA	/Move the multiplier into A /Shift it one bit to the right /The carry is either 1 or 0, save the /multiplier
	NOADD 0 MOVAB ADDE MOVBA	/If the carry is 0, just shift the /result. If the carry is a 1, add the /multiplicand to the result, then shift it /Get the MSBY of the result /Add the multiplicand /and save the MSBY of the result
NOADD,	MOVAB RAR MOVBA MOVAC RAR MOVCA	/Now shift the 16-bit result one /place to the right. /Save the new MSBY /Now shift the LSBY to the right.
	DCRL JNZ NXTBIT 0	/Have all eight bits of the multiplier /been tested yet? No, test another bit
	RET	/Yes, the answer is in register pair B

### **EXAMPLE 2**

### 8-Bit Division Subroutine

DIV88,	LXIH	/Load the L register with 010 (decimal 8)
	010	/or hexadecimal 08 and load the H
	000	/register with 000 (the result will be in H)
	MVIC	/Load the C register with 000
	000	/This register will be used for storage
NXTBIT,	MOVAE	/Move the dividend to A
	RAL	/Shift the MSB of A into the carry
	MOVEA	/Save the shifted dividend back in E
	MOVAC	/Get the partial dividend stored in C
	RAL	/Shift the carry into the LSB of A.
	SUBD	/Subtract the divisor from this number
	JNC	/If the carry = 0, the subtraction did not
	NOADD	
	0	/quotient. Otherwise add the divisor
		/back to A
	ADDD	/Add the divisor back to the content of A.
NOADD,	MOVCA	
NOADD,	CMC	/Complement the carry,
	MOVAH	/and shift the carry into the LSB
	RAL	/of the H register. If a borrow, C = 0
	MOVHA	/If not, $C = 1$
	DCRL	/Have all eight bits been shifted yet?
	JNZ	/No, shift another bit of the
	NXTBIT	/dividend and try another subtraction
	0	
	RET	/The answer is in H when the 8080
		/returns

illustrated in Fig 2. To divide two binary numbers, the divisor is subtracted from a larger and larger portion of the dividend, that has less and less significance. If the divisor is larger than the part of the dividend that it is being subtracted from, a borrow occurs. In this case, the divisor is added to the result of the subtraction to regenerate the original part of the dividend that was being tested. A 0 is then entered in the quotient for the bit position being tested. If no borrow occurs when the subtraction is performed, the result of the subtraction is used as the new partial dividend and a 1 is entered into the quotient since the divisor was successfully subtracted from the dividend. The subroutine listed in Example 2 divides the content of register E (the dividend) by the 8-bit content of register D (the divisor), with the 8-bit result (the quotient) saved in register H and the remainder saved in

The LXIH instruction in the DIV88 subroutine (Example 2) loads the number of bits in the divisor (octal 010, decimal 8) into the L register. The H register is loaded with 0, because it will be used to store the quotient. The MVIC instruction loads the C register with 0, as it will be used to store the partial dividend. At NXTBIT, the dividend is shifted one bit to the right. The most significant bit (MSB) is shifted into the carry and the remaining bits of the dividend are saved back in the E register. The partial dividend in register C is then moved to register A, and the bit from the dividend is shifted from the carry into the least significant bit (LSB) of register A. The SUBD instruction subtracts the divisor from the partial dividend, which was in the A register. If the divisor is subtracted

from a larger or equal number, the JMP to NOADD is executed. If the divisor is greater than the partial dividend, a borrow occurs, so the divisor is added to the result of the subtraction by the ADDB instruction. Register A now contains the original partial dividend.

When the 8080 executes the instructions at NOADD, it must enter a logic 0 or 1 into the quotient. Therefore, the state of the carry is complemented by the CMC instruction and then saved in register H. If the subtraction did not generate a borrow, then the carry is a logic 0, but a logic 1 must be entered in the quotient. If a borrow was generated, the carry is a logic 1, meaning that a logic 0 must be entered into the quotient. The CMC instruction simply complements the state of the carry to the state needed in the program. Finally, the content of register L is decremented by the DCRL instruction. If more bits within the dividend must be tested, the 8080 jumps back to NXTBIT; otherwise it returns from the subroutine with the quotient in the H register and the remainder in the C register.

There are a number of software tricks that can be used to simplify these two mathematical subroutines. However, unless the microcomputer can execute multiply and divide instructions or has special multiply/divide hardware, multiplication and division operations will have to be performed using these or similar algorithms.

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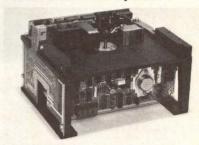
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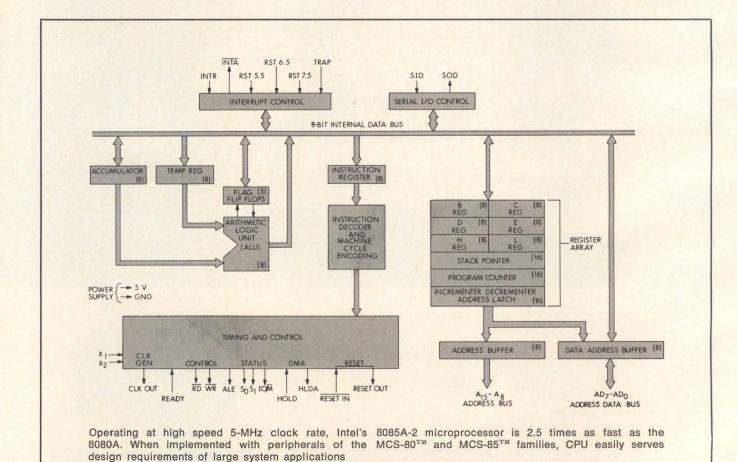
The development of 8085A-2 systems as an extension of the 8085 system has been accomplished by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 as a means of solving the problem of supplying a new system with proven support. Completely compatible with other MCS-85 family members, the 5-MHz CPU is an upgraded version of the 3-MHz 8085A; it runs 8080A programs without modification and is bus compatible with 8080A components. The system's larger application range covers industrial process control and instrumentation systems, diagnostic subsystems, general-purpose 8-bit minicomputers, high speed printers, diskette memories, intelligent CRT terminals, and other computer peripherals.

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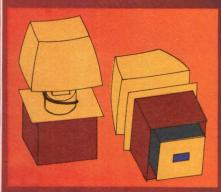
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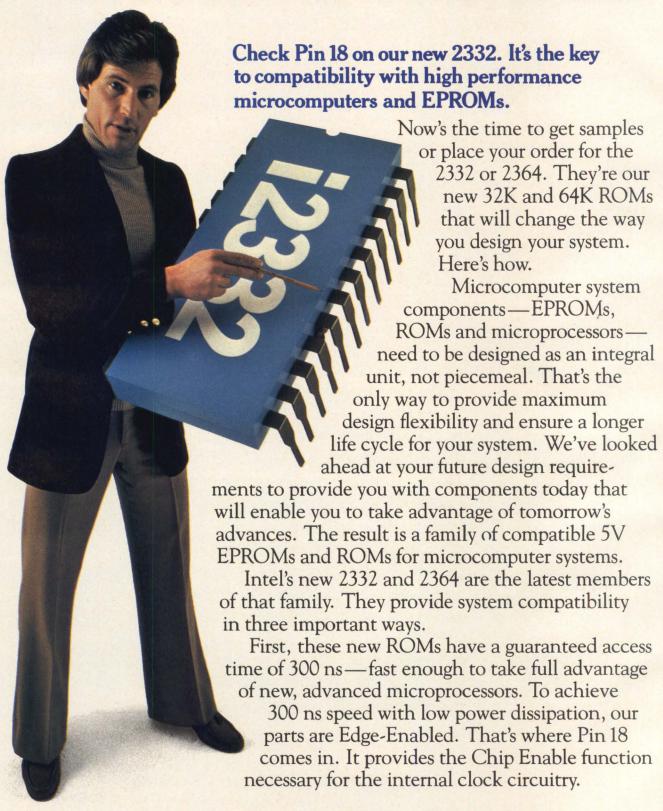
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Organization	2Kx8	4Kx8	8Kx8
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Standby Icc (max)	25 mA	15 mA	15 mA
Access Time (max)	350-450 ns	300 ns	300 ns

Engineering the 2332 and 2364 for microcomputer system compatibility led us to the third important advance—the end of bus contention problems. In new multiplexed microprocessor systems, such as the MCS-85 and MCS-86, the Output Enable (Pin 20) needs to be independent of the Chip Enable (Pin 18) which is the power control and selection function. So the 2332 and 2364 have an Output Enable (OE) for independent control of the data bus, with no possibility of multiple device selection. And input latches on all Edge-Enabled devices allow direct interface with new multiplexed microprocessors.

Low power is essential to meet today's design requirements. We've achieved low power in our 32K and 64K ROMs that can't be matched by fully static parts. Active current of the 2332 and 2364 is 40 mA (maximum). And Intel's Edge-Enabled devices have the added benefit of using Pin 18 for the power control function. So standby current is automatically reduced to 15 mA (maximum).

To get complete details on this important and complex subject, send for our 2332/2364 applications note AP-30, "Applications of Intel's 5V EPROM and

ROM family for microcomputer systems." It provides board layout recommendations, system design applications, timing diagrams, function explanations and discusses PL/M modular software compatibility. Write: Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051. Or for samples of these new parts, contact your local Intel representative.

intal delivers.

Europe: Intel International Corporation S.A., Rue du Moulin a Papier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814.

Japan: Intel Japan Corporation K.K., Flower Hill-Shinmachi East Building 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.

tem controller, multilevel maskable vectored interrupt control, and a programmable interval timer and event counter.

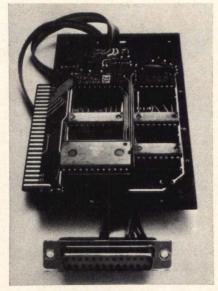
Programmable peripheral devices directly interface with either the MCS-80 or -85 system bus and are made with the same 5-V MOS/LSI technology. Configured and controlled with system software to perform specialized interface requirements, options include the 8251A programmable USART communications interface, the 8253-three interval timers with 16-bit binary/BCD counters, the 8255 containing three fully programmable 8-bit 1/0 ports, the 8259 programmable 8-level interrupt controller (expandable to 64 levels), and the 8279 programmable keyboard/display unit.

System development is supported by low cost enhancements of the Intellec<sup>R</sup> Microcomputer Development System. A PL/M compiler, which produces linkable and relocatable object code, and ISIS-II system implementation supervisor have been updated to support 8080A, 8085A, and 8085A-2 modular programming. Other available packages are a system monitor, macro assembler, text editor, ROM simulator, p/ROM mapper, diagnostic programs, ICE-85 in-circuit emulation module, and an intelligent universal p/ROM programmer. Circle 380 on Inquiry Card

# Personal Computer System Adds Communications, Printer Interfaces

Recently introduced by Apple Computer, Inc, 10260 Bandley Drive, Cupertino, CA 95014, model A2B0003X intelligent communications interface (ICI) card can be connected to any devices which will accept the EIA standard RS-232-C interface including 103A-type modems. Operation is at 110 or 330 baud.

The ICI interface has integral intelligence, eliminating the need for extensive software, and making the peripherals accessible by using simple commands built into Apple II's BASIC language. Operation is achieved by plugging the ICI into one of Apple's eight peripheral slots, and connecting the output cable to the desired device, such as the 103A-type modem. The unit is supplied com-



Intelligent communications interface provides Apple II users with capability for such applications as high speed message transfer, telephone transmission for the deaf, contests between remotely located computers, remote system failure diagnosis, and access to data banks and program libraries

plete with cable and operation manual.

Another peripheral is the model A2B0002X intelligent printer interface (IPI). This parallel printer card provides the Apple II owner with hard copy, using such printers as Axiom, Centronics, Okidata, Printronix, Qume, SWTP, and others.

Among the features: widths up to 255 char/line can be handled; 5000-char/s print speed; automatic powerdown of card components when no printing occurs; no external power requirement; and general-purpose 8-bit parallel output port. The IPI comes with firmware on ROM, printer configuration block, ribbon cable, and complete instruction manual. Circle 381 on Inquiry Card

# 16k Bank-Switchable ROM System for LSI-11/ PDP-11/03 Microcomputers

The concept of bank switching in memories is particularly useful in time-shared systems. Switching from one user to another does not require the use of a disc overlay with its associated loss of time. It needs only the execution of several simple instructions which disable one memory bank and enable another.

A versatile bank-switchable ROM system, ROM-016, has been developed by Digital Pathways, Inc, 4151 Middlefield Rd, Palo Alto, CA 94306. The system will function within DEC LSI-11 based computers, and is constructed on a single quad-board. It will accommodate up to 16k 16-bit words which have been programmed into Intel 2716 EPROMS or 2316E ROMs. The system can be expanded beyond the normal address limitations of the LSI-11 without running out of "memory space" because of the powerful addressing structure incorporated into each board. This results, according to the supplier, in a virtually limitless number of programs or routines which can be stored in instantly accessible form within this system.

"Bank switching" concept is the key to the versatility of the system. The memory is physically divided into four independent 4k-word blocks. Using either a set of manual switches or a device register, each of these blocks can be enabled and assigned a portion of the available address space. When enabled and assigned manually, the memory responds similarly to all other ROM systems. However, when the device register performs the block assignment, the blocks can be switched in and out within microseconds. Thus, a computer with limited address space can use extensive libraries of routines for beyond normal capacity by selectively enabling one, or more blocks, while disabling those remaining unused.

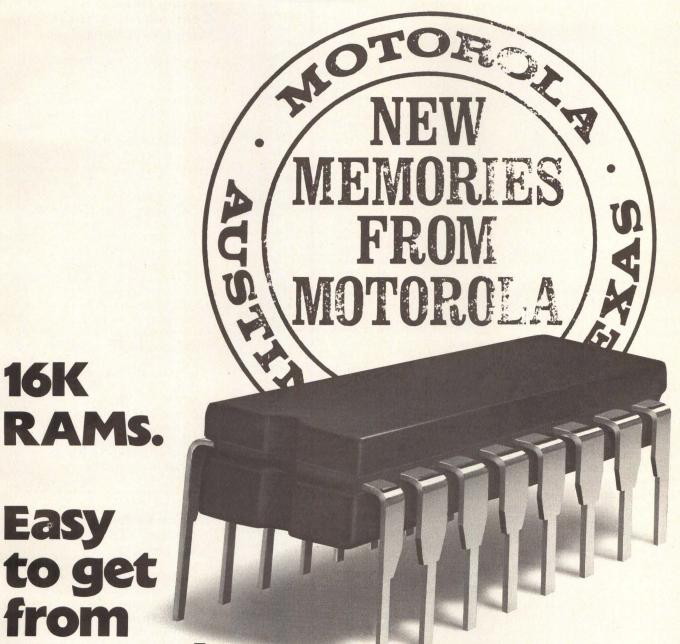
In the event that absolutely no address space is available within a given LSI-11 system, the ROM system can still be accessed in its indirect mode. All words on the board are individually or sequentially accessible at any time through a common port having a single peripheral address.

A companion product, RMP-004, a 4k version of the ROM-016, having full programming capability for Intel 2716 EPROMS on the board, is also available.

Circle 382 on Inquiry Card

# uComputer Teaches Computer Concepts

KX-33B microcomputer is designed to teach the basic concepts of computer technology, including the execution of functions by combining instructions with input signals. It is available from



from Motorola.

16K

Easy

The 16K RAM shortage is over. Motorola has the industry standard 16K in volume production, now. Our MC4116 is available in quantity, easy to get, and priced the way a volume memory should be

# And 4Ks, too.

priced.

The 4K RAMs are still in great P.O. Box 20912, Phoenix, demand. We've got them in

volume quantities and off-theshelf . . . the MCM4096, 4027, and 6604A, all priced the way you want them.

Our authorized Motorola distributors and Motorola sales offices can handle your order. For a data sheet, call one of them, or write to Motorola Semiconductor Products Inc., Arizona 85036.



OTOROLA

Semiconductor Group



Music, games, simulated sounds, and basic concepts of computer technology are provided by KX-33B microcomputer from Energy Electronics Products

Energy Electronics Products Corp, 6060 Manchester Ave, Los Angeles, CA 90045, and is intended to provide some idea of microcomputer operations as well as to introduce the world of the CPU, registers, and memory.

Basically a controller, the microcomputer is built around the Panasonic MN1400 microprocessor. In addition to the arithmetic/logic unit, the chip includes 1k words by 8 bits of ROM for the system program and 64 words by 8 bits of RAM for storage of keyboard data. There are also two static RAM chips, each with 256 words of 4 bits, which store tunes keyed in by the user. An 8-bit latch, audio amplifier and multivibrator ICS, and a loudspeaker are also included, as well as a 4-digit LED display.

The microcomputer can store any song that does not exceed its 3-octave range, and can perform control tasks over a 24-h period. It can also produce a 1-min buzzer tone. Both music and tone outputs may be triggered at a preset time by keyboard actuation, or by an input signal. Input signals are provided by three transducers: a cadmium sulfide photocell, a transducer that responds to moisture, and a reed switch that is actuated by the proximity of a magnet. An integral external speaker/earphone jack is also provided. Circle 383 on Inquiry Card

# General-Purpose Assembler Microprograms Bit Slice µProcessors

Eliminating microprogramming through the binary coding process of assembly languages, the Micro Assem-

bler software package can be used for complete microprogramming of most bipolar (bit slice) microprocessors. In addition, it allows editing to speed debugging and program alterations through iterated loops, updates, and replacements, and has a built-in test program to check system accuracy.

Signetics Corp, PO Box 9052, 811 E Arques Ave, Sunnyvale, CA 94086 has written the assembler in ANSI FORTRAN IV, to run on any 16- or 32-bit computer with FORTRAN capability. It may also be accessed through Tymeshare, GE, or NCSS timesharing services.

The language presently provides direct support for the 3002 and 2901-1 bipolar microprocessors and the 8X02 control store sequencer. Support of the 3001 microprogram control unit, as well as other elements and sequences, is obtained through the inclusion of explicit definitions.

Two programs are contained in the assembly language. The first reads the microprogram and the appropriate configuration and format descriptions written in the assembly language. A listing is produced containing source input, resulting binary form of the microinstructions, diagnostic errors, and symbol cross-reference. The second program punches paper tapes that can be used to program micro control-store p/Roms. The microprogram object form of the first program is read and partitioned into p/Rom modules, and a separate output is produced for each p/Rom.

Assembly language input to the assembler has two sections. The first defines the microinstruction formats and device configurations of the user system, specifying codes and name and length of each field. The second is the microprogram which is the sequence of symbolic microinstructions. User-defined opcodes allow mnemonic specification of field values. Standard assembler directives are supported.

Values may be decimal, hexadecimal, octal, or binary constants, ascu character constants, or symbolic values. These may be combined into expressions using arithmetic, binary shift, and logical operators.

The 2650 absolute object code, SMS format, and various BNPF formats are supported for programming p/ROMS. The \$775 assembler is available in source form on 9-track tape.

Circle 384 on Inquiry Card

# Moving Head Disc Controller Interfaces With LSI-11 Backplanes

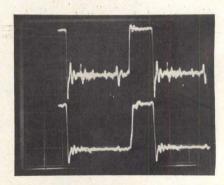
Model DI-C03, a compact single-quad size moving head disc controller module, interfaces directly with LSI-11 backplanes. Its bipolar microprocessor and circuit design achieves 1-board size for complete emulation of a DEC RK-11<sup>R</sup> disc system (transparent to RT-11<sup>R</sup> and RSX-11S<sup>R</sup> systems). It is available from Dynus, Inc, 3198 G Airport Loop Dr, Costa Mesa, CA 92626, to provide software and diagnostic compatibility with new or existing LSI-11<sup>R</sup> systems.

The disc controller uses DEC-approved circuit drivers and receivers; 8-word fifo buffer for DMA latency, and overlap seek capability plus automatic retry on seek error capability. It also includes two additional address bits for up to 128k words of direct addressing capability, allowing upward compatibility to future LSI-11s.

DMA transfer rate of 6.4 µs/word, cartridge capacity of 2.5M to 5M bytes, and double-frequency recording technique for storage on 2315- or 5540-type disc cartridges are provided. Power requirement for the module is 5 Vdc at 3.5 A. Circle 385 on Inquiry Card

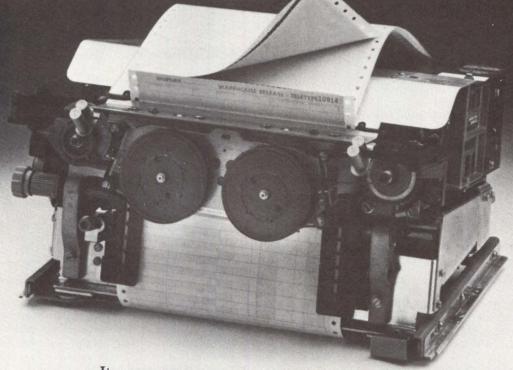
# Device Reduces Noise, Glitches, and Jitter on S-100 Bus

The "Glitch Grabber," a device that reduces noise, glitches and jitter on the S-100 microcomputer bus, has been announced by Extensys Corp, 380 Bernardo Ave, Mountain View, CA 94040. The edge-connective print-



Oscilloscope traces show "before" (top) and "after" noise reduction provided by Extensys "Glitch Grabber"

# OUR NEW 300 LPM FORMS ACCESS PRINTER DOES SOMETHING OTHER PRINTERS DON'T.



It saves paper.

That's because this new Teletype\* model 40 printer is designed with a unique tractor feed mechanism. One that's located below the print line. This provides your customers with immediate access to tickets, receipts, policies or reservation forms printed on a demand basis.

As soon as the printing operation is completed, the form can be torn off quickly. Without tearing or destroying the next form in the printer.

With the new Forms Access model 40 printer, your customers can print anything from a single label to a multi-part invoice, at 300 LPM, on forms ranging from  $4\frac{1}{4}$ " to  $8\frac{1}{2}$ " wide, and from  $2\frac{1}{2}$ " to 22" long.

That's what's different about the newest model 40 printer. What we didn't change is the model 40's outstanding reliability, simple OEM interface, interchangeable character sets, switch-selectable options, and the nationwide service and engineering support.

The OEM cost? \$1550 for a completely operational unit that includes everything you need to go on-line. All the OEM supplies is 115 VAC power and the serial signal source. Period.

No wonder we're getting a reputation as the OEM printer people.



\*Teletype is a trademark and service mark of the Teletype Corporation.

ed circuit maintains clean signals on the notoriously noisy S-100 bus, and safeguards the low tolerance voltage differential of bus signals that are asserted "high." It provides glitch-free signals, with no spikes, interference, or crosstalk, by applying well-documented analog techniques, used in transmission line analysis, to the digital environment of S-100 computers.

The device plugs into any open slot on the bus, and features a proprietary self-regulating transistor network that controls voltages and modifies circuitry to handle less or more voltage. Circuitry is only activated, however, in the event of a glitch, so that there is no loading of S-100 bus signals. The device is said to be also effective in business applications where reliability of operation is a prime concern.

Circle 386 on Inquiry Card

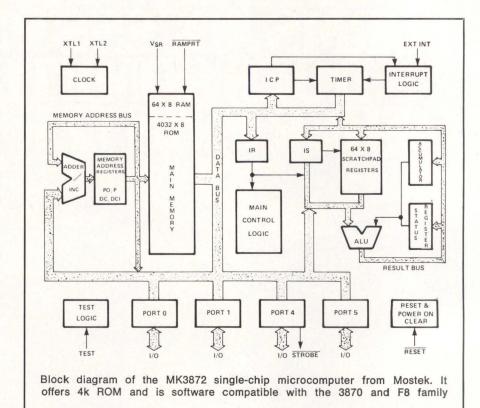
# Conditional Branching Function Is Added to Sequence Controller

Capabilities of sequential addressing and conditional branching of up to 4096 words of microprogram-stored microinstructions are contained in the 12-bit controller from Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086. An on-chip loop counter counts and controls repetition of a single or loop of microinstructions. The slice is a 40pin ceramic DIP, or 42-pin flat package for use over military and commercial operating temperature ranges. It operates with high speed, pipelined microprogrammed systems, particularly those with the company's Am 2901A or 2903 bipolar microprocessors.

Circle 387 on Inquiry Card

# Single-Chip uComputer Offers 4k ROM

Increased ROM allows the MK3872 to solve more difficult problems than any previous such device, according to Mostek Corp, PO Box 169, 1215 West Crosby Rd, Carrollton, TX 75006. Alternatively, the increased memory can be used to hold the programs for several products or prod-



uct versions, resulting in reduced manufacturing costs. The MK3872 is the first of a series of single-chip microcomputers based on the company's MK3870. While retaining a commonality with the 3870, the 3872 offers 4032 x 8 bytes of mask-programmable ROM, 64 bytes of scratch-pad RAM, and an additional 64 bytes of executable RAM. The latter is sup-

ported by an optional standby power mode for easy battery backup.

Other features include 32 bits (four ports) of bidirectional 1/0 (30 bits with standby power mode), programmable binary timer, external interrupt, low power—typically 285 mW, and a single 5 V ±10% power supply.

Circle 388 on Inquiry Card

# Printer Line Complements uComputer Development Systems

Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036 has announced a line of four models of dot-matrix printers to complement its microcomputer development systems. The line of printers features high reliability, 80- and 132-column formats; 60, 120, and 180 char/s; and bidirectional and logic-seeking printheads.

All four models are equipped with an interface 1/0 module plus an interconnection cable assembly that specifically adapt them to the various systems, including the EXORciser and the EXORterm 100 and 200.

These accessories also permit the printers to be used with the company's line of Micromodules (microcomputer board systems and subsystems) to provide more complete single-source availability of system components.

Modules in the printer line are: 779—capable of printing from 80 to 132 columns of 5 x 7 dot matrix



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shipped over 10,000 small digital tape drives last year. To more than 100 customers!

We manufacture:

# Model 6406 Raycorder

for Philips cassettes — the industry standard for more than 6 years.



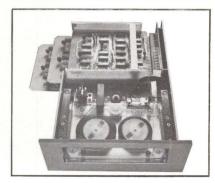
# Model 6409 Mini-Raycorder

for ANSI X3B5/77-22 Mini-Data cassettes — the first in the industry. Now added features make it even better — the runaway leader in its class.



# Model 6413 Cartridge Raycorder

for  $\frac{1}{4}$ -inch data cartridges. A new offering this year from Raymond — a new package with a proven track record.



Shouldn't you be buying the best? From the small tape drive experts —

Raycorder Products Division

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See us at the NCC, Booths 1101 and 1200. at a rate of 21 to 90 lines/min at 60 char/s. 781—an 80-column character unit featuring bidirectional, logic-seeking printhead movement, with throughput of up to 120 lines/min. 702—also with the bidirectional, logic-seeking printhead with a head speed of 120 char/s; it has 132-character columns, and throughput is from 45 to 185 lines/min. 703—the top of the line, ideally suited to business systems; head speed is 180 char/s, and throughput rates are from 70 to 280 lines/min.

All models except 779 have tractor feed, with a "paper-out" sensor, and use 1- to 6-part standard computer paper. Model 779 has pinch roll feed and uses standard Teletype roll

paper.

These printers are mechanically identical to equivalent model numbers available from Centronics Data Computer Corp, but are styled to match the Motorola line of microcomputer development products and micromodules.

Circle 389 on Inquiry Card

# Disc System Extends Storage Capacity of Microcomputers

Owners of small business or engineering computers with insufficient storage capacity are prospective users of the SIA-2000, a complete standalone disc subsystem. It was designed by System Integration Associates, Little Conestoga Rd and Adams Dr, Glenmoore, PA 19343, to provide database functions to support a wide range of small systems. The subsystem will interface with most microcomputer systems with little or no modification. Storage capacity ranges from 12M to 48M bytes; a variety of disc drives may be connected.

There are two standard interfaces. An S-100 interface treats the disc database RAM as an extension of the S-100 RAM space, and allows a simple handshaking convention between the systems. For systems without the S-100 bus, connection is via a custom interface which can be designed by the supplier at nominal cost.

The SIA-2000 contains 16k bytes RAM with DMA interface, an 8080A microprocessor, and disc interface logic which includes real-time keysearch hardware. Firmware is contained in 15k bytes of p/ROM.

All tasks associated with storage management, record blocking, directory maintenance, sorting, searching, and indexing of files are performed. Commands to the database system are in symbolic English and in the form of symbolic strings. All references to data are made using symbolic names assigned by the user.

Extensive error diagnostic capabilities, including automatic retries on disc errors, are included. At power-on time the SIA-2000 performs a self-test of the subsystem before becoming ready. A card cage, power supply, and cabinet are available. Delivery is 30 days ARO.

Circle 390 on Inquiry Card

# SBC Prototype Board Offers Standard Packaging Scheme

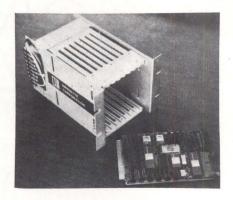
A prototyping PC board, compatible with Intel's SBC-80/10, 80/20, and Intellec series, provides breadboard adaptation to basic SBC microcomputer systems and expansion of system bus configurations. Card edge output connectors are located across the top of the board, with holes directly below them to mount an additional wirewrap connector. Holes are provided for potentiometer and 14- and 16-pin IC package mounting for output control.

SenDEC Corp, 54 West Ave, Fairport, NY 14450 has included two buses on each side of the expandable board, with ±5 V on one side and ±12 V on the other. Buses are staggered and set up to accept bypass capacitors. Bottom edge connections are designated by the system bus to which they connect.

Circle 391 on Inquiry Card

# Standalone µComputer Includes Serial Communications Interface

Model 0B8001, a single-board computer having processor, memory, and 1/0 on a 4.5 x 6.5" (11.4 x 16.5-cm) card, also includes serial communications interface meeting both the 20 mA and RS-232-C standards. The supplier, Omnibyte Corp, 2711B Curtiss St, Downers Grove, IL 60515, anticipates applications in machine and process control, and in the scien-



tific instrument, military, aerospace, energy management, commercial, and hobby markets.

Included on the board are the MC6800 processor, 1-MHz crystal-controlled clock, 1k bytes RAM, sockets for 2k/4k p/ROM, and serial interface with selectable baud rate. An MC6821 peripheral interface adapter provides two bytes of programmable binary I/O along with four programmable control bits. There are fully buffered address, data, and control lines for offboard expansion; full decoding for eight pages of off-board I/O addressing, and a separate 128-byte RAM for scratchpad memory.

This card is fully compatible with the company's family of memory and I/o cards, and, using a card cage, can be expanded to larger microcomputer systems; for example, an 0B8001 and an 8k RAM card can implement a mini-floppy disc based software development system. Power requirement for the card is ±5 and ±12 V.

Circle 392 on Inquiry Card

# 8080 In-Circuit Emulator Expands Utilization Into Factory and Field

The model 80FS portable real-time in-circuit emulator for the 8080 microprocessor accommodates a full 64k bytes of online memory that can be allocated between the user's system and the emulator. User generated diagnostics stored in RAM, ROM, or p/ROM in the unit from MuPro Systems Div, 424 Oakmead Pkwy, Sunnyvale, CA 94086 can run in real time in conjunction with the user's product. This capability combined with crossloading of programs from a user system's ROM into the emulator's RAM provides powerful

# THE MAXI VALUE FOR YOUR MINI-COMPUTER GRAPHICS.

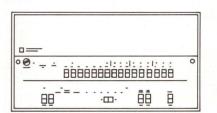


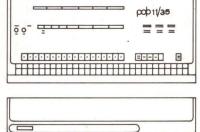
Gould offers the most cost effective and reliable electrostatic printer/plotters to use with PDP-11, Nova/ Eclipse and HP 2100/21 MX mini-computers.

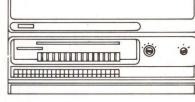
That's because they offer outstanding features that add up to value. High speed. High resolution. Outstanding contrast. Patented closed loop toner system. Timed-phase imaging system. And high density staggered imaging head, to name a few.

All hardware interfaces utilize direct memory access to reduce CPU overhead and are connected directly to a standard I/O bus or Unibus. A multiplexing capability allows you to share one Gould printer/plotter with two CPU's, or one CPU and a Tektronix 4010 Series graphic terminal hardcopy interface, supporting up to four terminals.

Gould's in-house software engineering staff developed device drivers and plot packages which









operate with the popular operating systems. In addition, Gould maintains a full technical support staff for assistance in the users system integration.

Plot packages offer plotting routines and calling sequences that are upward compatible with the basic Calcomp Pen plotter graphics package. The addition of an optional hardware character generator allows the plotter to be used as a high speed non-impact line printer (up to 1625 lpm).

Regardless of your application, the printer/plotter's ability to function as a high-speed graphic plotter, line printer or Tektronix CRT hardcopy unit makes Gould your maxi value. Contact us today for more information. Gould, Instruments Division, 3631 Perkins Ave., Cleveland, OH 44114. Phone (216) 361-3315.

For brochure call toll free (800) 325-6400, ext. 77. In Missouri: (800) 342-6600.







capability for testing, upgrading, and maintaining 8080-based products.

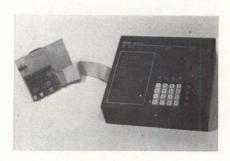
Other functions allow the user to monitor and modify registers and memory, set breakpoint conditions, and trace computer operations. Also included are general-purpose parallel and serial 1/o.

The device is equipped with 8k bytes of static RAM, a rugged carrying case, and card ejector. The 22 x 7.5 x 10" (56 x 19 x 25-cm) case provides space for the emulator/ computer, memory and 1/o cards, spare 40-pin headers, and power card, as well as the optional 2708 p/ROM programmer.

# **Fully Functional** In-Circuit Emulator for 6800-Based Systems

Circle 393 on Inquiry Card

The 68/01E provides an efficient and economical means for testing and debugging hardware and software on 6800-based microcomputer circuits. All of the 6800 MPU signals are terminated in a 40-pin DIP plug, which is inserted into the 6800 socket of the microcomputer circuit under test. This places the microcomputer under the emulator's diagnostic control, and enables the user to examine MPU registers, read/alter memory locations, enter and execute programs, set/remove breakpoints, and move through programs one step at a time.



Rank Peripherals of Canada Ltd. 4998 Blvd de Maisonneuve West, Suite 1020, Montreal, Quebec H3Z 1N2, Canada supplies the emulator. It comes fully assembled in a compact metal cabinet, with 6-character hexadecimal display and keyboard, 256 bytes of user RAM, Motorola's IBUG monitor in ROM, cassette interface, and user manuals.

Circle 394 on Inquiry Card

# Software Products Aid **uProcessor** Application **Program Development**

A family of computer programs, Microbench™ software operates in 16k words of memory with PDP-11 and LSI-11 computers under the RT-11 operating system to provide economical microprocessor program development capability. Featured are relocating assemblers and linking loaders coded in Macro-11 for the 8080/8085, Zilog Intel Motorola 6800, and equivalent microprocessors. Assemblers are source language compatible with manufacturers' assemblers.

Virtual Systems, Inc. 1500 Newell Ave, #406, Walnut Creek, CA 94596 has included such features as a system macro library, optional cross reference listings, object file library maintenance, and ROM/RAM alignment at load time. Binary output formats are available for many p/ROM programmers.

Circle 395 on Inquiry Card

# **DMA Interface Board** for LSI-11 and LSI-11/2 Features Dual-Height Card

Among the features of the DMA-L11 direct memory access board are a dual-height 8.5 x 5" (21.6- x 12.7cm) card, onboard bootstrap facility for the user's p/ROM, and a buffered bidirectional data bus for ease of interfacing to the user's device. Computer Technology, 6043 Lawton Ave, Oakland, CA 94618 says that it is the only available general-purpose DMA interface that will work with DEC's LSI-11/2 product line. Word or byte transfers are handled at rates up to 400k transfers/s.

Programmed 1/0 is allowed between the CPU and five 16-bit registers in the external device for control of complex devices. Three 16-bit registers on the DMA board include command/status, memory address, and byte count. Extended memory is supported, and up to 32k words or 65k bytes may be transferred in a single operation.

A 16-bit bidirectional data bus between the DMA and the user's external device is used for both programmed and DMA I/o. Control lines to the device include write, read, three address lines, high/low byte indicator, DMA grant, and initialize. Signal lines from the device to the DMA interface include DMA request, interrupt request, and power OK. Sockets for two 32 x 8 p/ROMs are included, allowing implementation of a 32-word program for automatic boot-strapping from the external de-

The interface takes up one-half slot in the LSI-11 backplane. Typical power requirement is 5 V at 1.0 A. A 40-conductor flat ribbon cable is required for connection to the external device.

Circle 396 on Inquiry Card

# Timesharing 16-Bit Microprocessor Board Has I/O Support Facilities

AM-100,™ an S-100 bus compatible microprocessor board set, offers multitasking, multiuser timesharing in a disc operating system environment. Utilizing Western Digital's WD-16 microprocessor, the 16-bit board has 11-digit floating point arithmetic and onboard real-time clock. Utilities include a multipass macro assembler, Alphabasic $^{\text{\tiny TM}}$  compiler, Alphalisp, $^{\text{\tiny TM}}$ SORT, and ISAM; licensed software includes AMOS<sup>TM</sup> operating system.

Alpha Microsystems, 17875 Sky Park N, Suite N, Irvine, CA 92714 has enabled many S-100 bus peripherals such as static memory, memory paging, and 1/0 facilities to be supported. AM-300<sup>™</sup> is an S-100 bus compatible, 6-port serial 1/0 board containing six Western Digital ASTRO chips. Compatible with 8080-based microprocessors, it provides six programmable RS-232 ports with 16 baud rates up to 19.2k. Each multilevel, interrupt driven port accepts data in either asynchronous or synchronous mode.

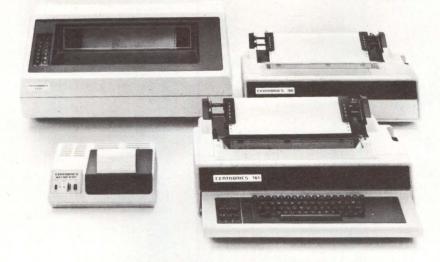
Circle 397 on Inquiry Card

# Does single source make Centronics better than other printer Companies? No. Although our 9 model companies? No. Although our 9 model printers, 4 model 6000 series of band printers, 760 series tele-

printers and new non-impact electrostatic printer give us the most complete line in the industry, it still takes more than breadth of line to be the leader.

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# MICRO PROCESSOR DATA STACK

# **Motherboard Eliminates Bus Noise and Ringing** in S-100 Systems

A shielded motherboard eliminates all noise and ringing in buses according to the supplier, Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070. The board is compatible with S-100 computer systems, and is made of 0.125" (3.2-mm) FR4 glass epoxy. By placing substantial ground traces between adjacent bus lines, line-to-line coupling, responsible for most of the bus noise in S-100 systems, has been eliminated.

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The shielded motherboard comes in a 16-slot configuration, and will be available later in a 10-slot version. It fits any standard chassis and requires no soldering. Circle 398 on Inquiry Card

33061. The system has two 40-key keyboards, an 8-digit LED display, and other control switches. Clocking speed is 4 MHz with a 12-bit word size. The language is PDP-8 compatible, and most instructions are single-cycle execute.

Applications are expected in vehicular systems, in areas where power sources are unreliable, remote area data collection, on-site data reduction, and remote instrumentation. The unit will deliver full operation for eight hours using an integral battery with charger, and data can be stored for up to one year in the standby mode. Circle 399 on Inquiry Card

# **Personal Computer** and Calculator Use Minidisc for Storage

An innovative minidisc for program and file storage, and a Mini-BASIC language are features of the P6040, a 17-lb (8-kg) programmable computer and calculator from Olivetti Corp of America, 500 Park Ave, New York, NY 10022. The integral, paper-thin, 2.5" (6.4-cm) dia minidisc has a 3k byte capacity; typical

# **uComputer** in a Briefcase **Operates Off Battery** for Portable Applications



A portable microcomputer contained within a small briefcase has been developed by Adaptive Systems, Inc. PO Box 1481, Pompano Beach, FL



program can reside on one disc. Mini-BASIC is a subset of BASIC, and is based on seven keyboard-located programming verbs.

P6040's base unit includes a 16-col alphanumeric printer, keyboard, minidisc unit, 16-char LED display, hardwired Mini-BASIC interpreter, and 3k user memory. A wide variety of peripherals can be supported via optional parallel and RS-232-C interfaces. The standard P6040 operating system handles the logic for these connections.

Circle 400 on Inquiry Card

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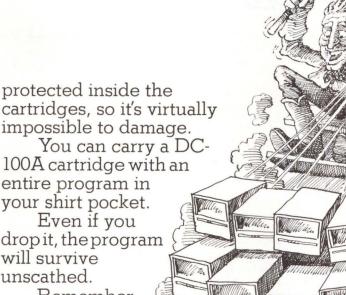
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Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



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One formatter can control eight drives at once.

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your shirt pocket.

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# AROUND THE IC LOOP

# MONOLITHIC DATA CONVERSION DEVICES PART 3: AUXILIARY INTEGRATED CIRCUITS

Eric R. Garen
Integrated Computer Systems, Santa Monica, California

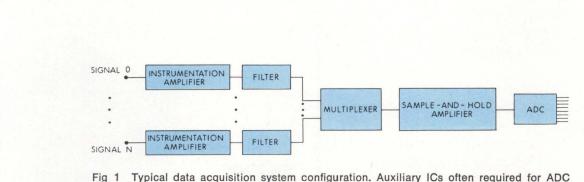
The first two columns in this series covered the status of monolithic digital-to-analog and analog-to-digital converters (Mar 1978, pp 152-158; Apr 1978, pp 188-196). This month's column completes the series by describing the status and application of auxiliary integrated circuits which often are as necessary in data conversion systems as the converters themselves. The most important of these circuits are instrumentation amplifiers, filters, multiplexers, and sample-and-hold amplifiers (Fig 1).

### Instrumentation Amplifiers

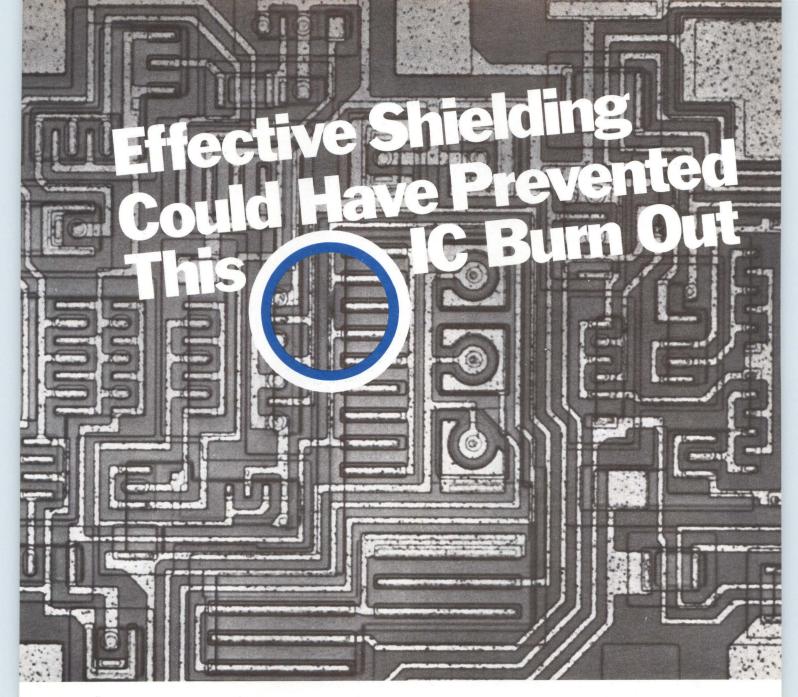
Data acquisition systems often require a differential input amplifier to retrieve millivolts of analog data from volts of common-mode interference. In some cases, it is necessary also to isolate the amplifier's input galvanically from its output and the power source to protect the amplifier from high voltage, to protect the device being measured (eg, a hospital patient) from stray leakage current, or simply to obtain better common-mode rejection. Instrumentation amplifiers are used for this purpose.

Although instrumentation amplifiers often contain operational amplifiers, they are distinguished from op amps in being committed devices with a definite set of input-output relationships and an essentially fixed configuration. They are designed to meet the specific objectives of high common-mode rejection ratio, low noise and drift, moderate bandwidth, and a limited range of gains (usually 1 to 1000, programmable by a single resistor).

The instrumentation amplifier is a committed-gain amplifier with internal high precision feedback networks. Excellent drift, linearity, and noise-rejection capability make it a natural choice for extracting and amplifying



or DAC circuits are instrumentation amplifiers, filters, multiplexers, and sample-and-hold ampliers



Micro-min electronics in low power, complex digital circuitry is increasing rapidly in EDP mainframes and peripherals.

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CIRCLE 131 ON INQUIRY CARD

low level signals in the presence of high common-modenoise voltages.

These devices are commonly used as transducer amplifiers for thermocouples, strain-gauge bridges, current shunts, and biological probes. As preamplifiers, they are capable of extracting small differential signals superimposed on large common-mode voltages. Wideband designs are also available for data acquisition systems.<sup>1</sup>

Many monolithic IC instrumentation amplifiers are now available (see Table). Most allow the user to set the gain with an external, low temperature dependent resistor. A now common circuit configuration is the differential current feedback circuit, of which Analog Devices' AD520 was the first (Fig 2).

This circuit utilizes high impedance FETs to buffer the inputs,  $E_1$  and  $E_2$ . The difference between these buffered inputs is then amplified to provide  $E_0$ , the output. Thus, small differential signals can be extracted from commonmode noise (appearing identically on both  $E_1$  and  $E_2$ ).

Sense and Reference feedback inputs are used to alleviate any distortion due to circuits which follow the amplifier. In normal applications, Sense and Reference terminals are connected to achieve feedback from the specific points at which the output is to be accurately maintained; the circuit can then compensate for voltage drops in the output signal or ground lines.

The Sense terminal is especially useful in circuits employing current-booster followers, since the booster may then be included within the feedback loop and its offsets, drifts, and gain errors nullified. Sense and Reference terminals, if high enough in impedance to avoid significant loading, are also useful for driving current to either floating or grounded loads.

# **Filters**

Further signal conditioning may be necessary following the instrumentation amplifier to improve the signal-to-noise ratio by filtering out noise and/or to restrict the bandwidth of the input signal to less than one-half the sampling rate. Most typically, active filters are custom-designed with op amps for each application. Alternatively, "universal" active filters are available from Burr-Brown (the UAF series) and other manufacturers. Many of these hybrid DIPs include the basic building blocks necessary to construct Bessel, Butterworth, or Chebyschev low pass, high pass, band pass, and band reject filters.

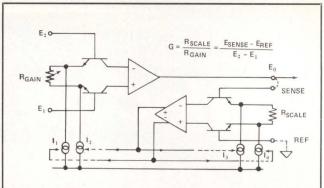


Fig 2 Differential current-feedback monolithic instrumentation amplifier, the AD520 (Courtesy Analog Devices, Inc)

As shown in Fig 1, these filters are often implemented on a per channel basis immediately following each amplifier. If the signals on all channels are identical in nature, however, a common filter which follows the multiplexer is an obvious cost-saving approach. Similarly, a single-programmable-gain amplifier which follows the multiplexer, rather than multiple amplifiers preceding, would appear desirable. However, this approach assumes that unamplified signals will pass undistorted through the multiplexer itself.

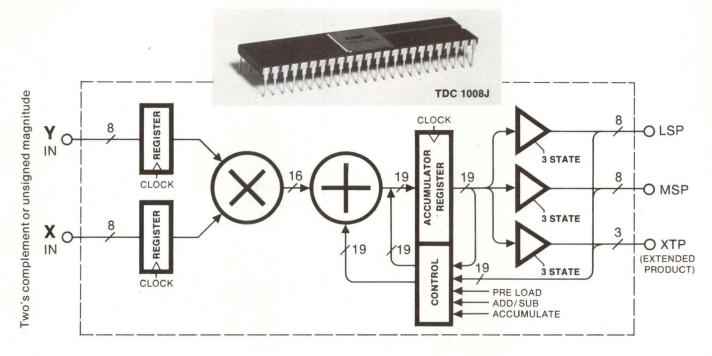
# Multiplexers

Multiplexers used in data acquisition systems are most typically either constructed with reed relays of IC JFET of CMOS analog switches. Reed relays, because of their minute impedance, are used to switch low level unamplified (millivolt) analog signals such as those produced by thermocouples. When all inputs to the multiplexer are of this nature, a relay multiplexer is often the most cost-effective approach because it permits a single amplifier to be used after the multiplexer instead of one amplifier per channel. Chief disadvantages of this approach are the slow speed of reed relays by comparison with solid-state switches, limited life (109 operations typ), and PC board space requirements.

### Partial Listing of Typical Monolithic Auxiliary Circuits for Data Conversion

Manufacturer	Instrumentation Amplifiers	Multiplexers	Sample-and-Hold Amplifiers
Analog Devices	AD520 series	AD7501 series	AD582 series
Burr-Brown Research	3627, 3660	MPC 4D/8D/8S/16S	SHC 80
Datel Systems	AM435	MXD series MVD series	SHM-IC SHM-LM
Harris Semiconductor Products		HI-506/507/508/509 HI-1818/1828 HI-1840	HA-2420/25
National Semiconductor	LF 152/252/352 LH 0036	AH5009, AM2009, AM3705 CD 4051/2/3	LF 198/298/398 LH 0023/43/53
Precision Monolithics	<del></del>	MUX-88	

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- Controllable addition or subtraction in accumulator
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- Bipolar TTL monolithic technology
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More and more, solid-state multiplexers are being used, and this will certainly be true in the future given the rapidly declining cost of high quality  $10^{\circ}$  amplifiers. The primary problems in utilizing  $10^{\circ}$  multiplexers are finite on-resistance, typically 50 to 1500  $10^{\circ}$ ; crosstalk caused primarily by stray capacitance; switching transients. A major limitation is that the input signal range is typically only  $10^{\circ}$  and larger signals may destroy the switch.

The most important single requirement for a multiplexer is that it operate without introducing unacceptable error at a speed consistent with the sample rate requirements. Because of their non-ideal transmission and opencircuit characteristics, analog multiplexers introduce static and dynamic errors into the selected signal path. These include leakage through switches, coupling of control signals into the analog path, and interaction with both source and following amplifiers. Poor circuit layout and cabling can compound these effects and further degrade performance.

For dc or low frequency conditions the capacitive components can be neglected and signal attenuation is due to the resistance,  $R_{\rm DS(on)}$ . Hence multiplexer insertion loss at low frequencies may be given by

$$\frac{V_{\rm IN}-V_{\rm L}}{V_{\rm IN}}~=~\frac{R_{\rm DS(on)}}{R_{\rm L}+R_{\rm DS(on)}}$$

where R<sub>DS</sub> is the switch resistance.

For example, if  $R_L=10~k\Omega$  and  $R_{DS(on)}=100~\Omega$  at dc, the insertion loss is about 1% error, which is an acceptable level for many dc multiplexing applications.

For JFET switches  $R_{DS\,(on)}$  max may be lower than  $10~\Omega$  at  $25~^\circ F~(-4~^\circ C)$  as is the case for the Siliconix DG180 2-channel switch with typical values of around  $8~\Omega$ . cmos devices exhibit higher values of  $R_{DS\,(on)}$ ; eg, the Siliconix DG200 2-channel switch exhibits typically  $50~\Omega$  with analog signals up to  $\pm 10~V$ , and the DG506 16-channel cmos multiplexer exhibits  $250~\Omega$  typically. Other cmos multiplexers have up to 1500- $\Omega$  resistance. Furthermore, for most cmos devices, the channel resistance is typically subject to 20% overall variation throughout the entire analog signal range.

At high frequencies, the contributions of capacitance become significant. Such considerations become important for applications involving the switching of rf, video, or pulsed signals.

Channel isolation at low frequencies is limited by leakage components such as  $I_{D(off)}$  and  $I_{S(off)}$ , while at higher frequencies it is principally dependent on capacitive coupling. At higher frequencies, care must be taken with circuit layout to minimize capacitive strays between input and output terminals of the off channels. These strays

may be combined to give a component  $C_{\rm stray}$  appearing in parallel with  $C_{\rm DS}$ , for the off switch. Inter-lead capacitances due to pin spacing on the package can be an additional contribution to this stray capacitance.<sup>2</sup>

Some typical monolithic multiplexers are listed in the Table. These devices accept TTL level address signals which are binary coded to select the desired channel.

Most of these devices have designed out certain fatal flaws that plagued early semiconductor analog switches. These protections include: latch-up protection (formerly an on-channel might not turn off until it crossed 0 V), power failure protect (formerly input devices might be shorted together when power was removed), and breakbefore-make (formerly, input channels might be shorted together for a short time during switching). With these flaws corrected, applying monolithic multiplexers is a question of selecting the proper switching speeds, crosstalk, and channel-on impedance at the frequencies to be sampled.

# Sample-and-Hold Amplifiers

Many data acquisition systems require a sample-and-hold (s/H) amplifier between the multiplexer and the A-D converter. The s/H is needed to very quickly sample the input signal and hold that sampled voltage constant while the A-D conversion is in progress. Otherwise, considerable error may result. For example, consider the case where a sinusoidal signal is to be sampled. The maximum change in signal voltage during the conversion (or aperture) time occurs when the sinusoid crosses zero. In this case  $\Delta V/V = 2_\pi f t_a$ , where f is the sinusoidal frequency, and  $t_a$  is the aperture time. To achieve 10-bit resolution requires an error of less than one part per thousand. Even for a comparatively slow signal of 1 kHz, this requires an aperture time of

$$t_a = \frac{\Delta V}{V} \ x \ \frac{1}{2\pi f} \ = \ \frac{0.001}{6.28 \ x \ 10^3} = 160 \ x \ 10^{-\theta}$$

The result is a required aperture time of only 160 ns to remain within 1 bit (0.1%) of resolution due to the rate of change of the signal. It can be seen from this result that to convert even a slowly varying signal to moderate resolution levels requires an extremely fast and, therefore, expensive A-D converter. As discussed in last month's column, most counter-type monolithic ADCs have conversion times of several hundred microseconds, and even sar-type adds may take 20 to 80  $\mu$ s. Fortunately a simple and inexpensive way around this problem is the use of the s/H circuit, which can reduce the aperture time considerably by taking a rapid sample of the signal and then holding its value for the required conversion time.

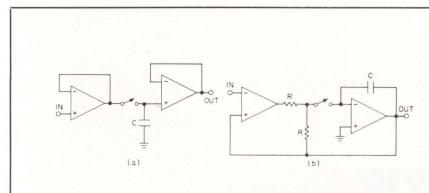


Fig 3 Sample-and-hold circuit configurations (Courtesy Datel Systems, Inc)

# SZK K()

It's fully-static NMOS. It's fast (300 ns max. cycle time). It's available in volume now.

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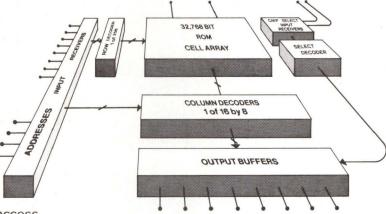
The R2332 is universally compatible with N-Channel microprocessors, and supports Rockwell's growing R6500 microprocessor family.

The fast R2332-3 features maximum access and cycle time of 300 ns. Both the R2332-3 and the standard 450 ns R2332 use 400 mW power

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R2332 and R2332-3 inputs are TTL compatible with a 400 mV minimum noise immunity on both the HIGH and LOW inputs. All eight outputs are tri-state drivers capable of driving 100 pf and a TTL gate.

The R2332 from Rockwell operates totally asynchronously and requires no clock input, so it's compatible with both static and clocked-static versions. Two mask-programmable chip select



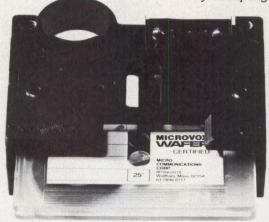
inputs allow four 32K ROMS to be OR-tied without external decoding. Programming allows selection when the input is HIGH or LOW or in a don't care mode. Both chip select and chip deselect delays are 100 ns.

Get started today by getting more information on R2332 and the R6500 family. Contact a local Hamilton/Avnet distributor or write: D-727-A, Microelectronic Devices, Rockwell International; P.O. Box 3669, Anaheim, CA. 92803 or phone (714) 632-3729. Telex (via TWX) 910-591-1698.



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# MICRO COMMUNICATIONS CORPORATION

80 BACON STREET WALTHAM, MASS. 02154 617/899-8111 A s/H in its basic form consists of a switch and a capacitor. When the switch is closed the unit is in the sampling or tracking mode and will follow a changing input signal. When the switch is open the unit is in the hold mode and retains a voltage on the capacitor for some period of time depending on capacitor and switch leakage.

Practical s/H circuits also use input and output buffer amplifiers and sophisticated switching techniques. The output buffer amplifier must be a low input current fet amplifier in order to have as small an effect as possible on the leakage of the capacitor. Similarly, the electronic switch must be a low leakage type such as an fet switch. Fig 3 illustrates two s/H circuit configurations which are commonly used. Circuit (a) is used for fast s/Hs and is an open loop configuration using fast voltage-follower amplifiers. Circuit (b) is a closed loop configuration with an operational integrator in the feedback path of the input buffer amplifier. This circuit results in extremely good accuracy and linearity.<sup>3</sup>

Note that performance of these monolithic s/Hs is greatly affected by the storage capacitor. Smaller capacitors offer fast acquisition times but rapid droop (drift rate). A larger capacitor will decrease the drift rate at the expense of slower acquisition times. In order to minimize drift error, care in selection of the storage capacitor and layout of the PC board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. A guard conductor connected to the output surrounding the storage node will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the PC board.

Size of the capacitor is dictated by required drift rate and acquisition time. Drift is determined by leakage current at the capacitor pin and may be calculated by

$$\frac{\mathrm{d}V}{\mathrm{d}t}\,=\,\frac{I_{\scriptscriptstyle 1}}{C_{\scriptscriptstyle 8}}$$

where  $I_1$  is the total leakage current of the device at the capacitor pin, and  $C_{\rm S}$  is the value of the storage capacitor. Many manufacturers offer a variety of monolithic s/H amplifiers; several of these are listed in the Table.

### Summary

Proper selection and use of these auxiliary devices will often be the difference between success and failure in data conversion. The engineer must take a true systems approach to the design, and match performance of all components in the system to avoid any "weak links." Fortunately, the availability of inexpensive, high quality, reliable components—including instrumentation amplifiers, filters, multiplexers, sample-and-holds, and D-A and A-D converters—makes the design far easier and less expensive than it was even a few short years ago.

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- "Datel Engineering Product Handbook," Datel Systems, Inc, Canton, Mass, 1977/78
- "Linear Data Book," National Semiconductor Corp, Santa Clara, Calif, 1976

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# **Charge-Transfer Devices Perform Sophisticated Signal Processing Functions**

As discussed in a 3-part series in Computer Design (Nov 1977, pp 146-152; Dec 1977, pp 130-140; Jan 1978, pp 154-157), many potential applications for charge-transfer devices (CTDS) relate to digital circuits. Two CTD transversal filters for such applications have been announced as inventory items by Reticon Corp, 910 Benicia Ave, Sunnyvale, CA 94086. One product, a charge-coupled device (CCD) quad filter, calculates the discrete Fourier transform using the chirp Z algorithm. The second announcement covers a family of bucket-brigade devices (BBDs) that serve as standard and programmable filters: two low pass and two high pass, each in narrow and broad band versions.

# Spectrum Analyzer

The R5601 consists of two separate 512-stage ccps that implement four transversal filters using the split-electrode weighting technique. Filter weighting coefficients and internal

circuit connections are configured such that the device, with additional off-chip components, can implement the chirp Z transform algorithm to calculate a 512-point discrete Fourier transform. (See Figs 1 and 2.)

Two versions of the quad chirped transversal filter are available, differing in the type of window applied to the data to be transformed. The -1 uses a rectangular window for maximum resolution in the transform (or frequency) domain but has relatively high side lobe response (frequency leaks). The -2 uses a Hanning window to decrease the side lobes; however, this window also decreases the frequency resolution of the resulting discrete Fourier transform by about a factor of two. In general, the -2 is intended for use in spectral analysis applications and -1 for direct calculation of the complex Fourier coefficients.

To perform the Fourier transform it is necessary to multiply the input signal by a complex chirp waveform, convolve the real and imaginary parts with a second complex chirp waveform, and then post-multiply the output by the same chirp waveform used in the premultiplication. The R5601 performs the convolution of the real and imaginary input signals with a complex chirp [e (i $\pi$ n²)/N,  $1 \le n \le 512$  for the R5601-1]. If only the magnitude of the spectrum is required, the filter outputs are squared and summed.

A complete circuit module is also available. The RC5601 operates at sample rates from 1 to 100 kHz and contains all the pre- and postprocessing required to compute power spectral density. It requires only the addition of dc power supplies and an oscilloscope for an output display.

Both device and module perform a sliding transform using 512 time samples of the input signal to obtain a spectrum which has a frequency resolution 1/512 of the sample rate. Although the present evaluation module operates only to 100 kHz, the device itself is capable of sampling rates up to 2 MHz. Dynamic range is 70 dB; 2-tone range is 45 dB. Transform accuracy is equal to that obtained with a 13-bit, 512-point fft. Circle 345 on Inquiry Card

# Tunable Filters

Sixty-four-stage split electrode BBD architecture is used in the R5602 family of transversal filters. Also called finite impulse response (FIR) filters, the family currently consists of two low pass and two band pass devices. Usable sampling frequency range is 250 Hz to 1 MHz. Filters are electronically tunable by varying input clock frequency.

These sampling filters are linear in phase; they have transition rates exceeding 150 dB/octave and more than 45-dB stop-band rejection. Each device also contains on-chip timing and output control circuits. Weighting function is determined by the relative sizes of the electrodes associated with each stage. The filter tap weights are determined to an accuracy of ±0.5% by programmed control of the size of capacitive sensing electrodes. Only one mask layer is involved in the programming of the impulse response. Tap weights to give a desired spectral response are determined by an optimum FIR filter design program.

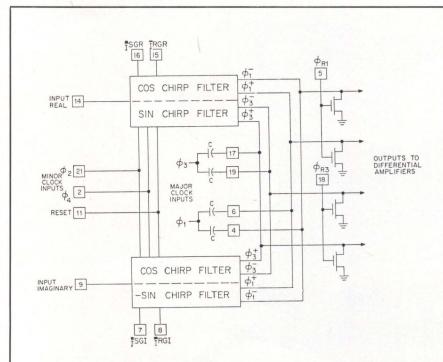


Fig 1 Simplified block diagram of Reticon CCD quad transversal filter. Four 512-point transversal filters are implemented using split electrode structure and made using  $4\phi$  surface channel CCD process. R5601-1 contains regular chirp waveforms, while -2 contains chirp waveform multiplied by Hanning window function which reduces frequency leakages into adjacent spectral lines

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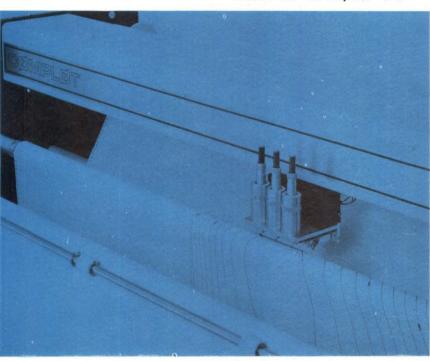
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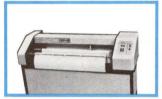




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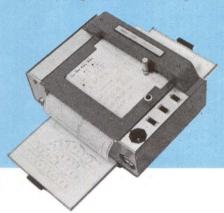
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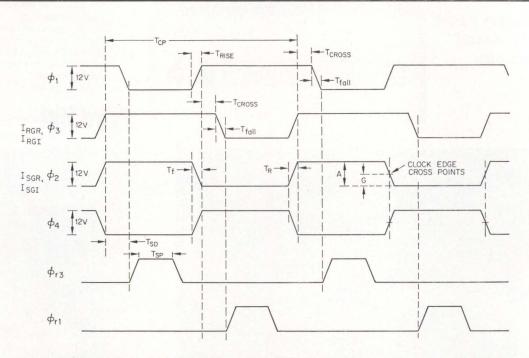


Fig 2 Clock waveforms and timing diagram of CCD "spectrum analyzer on a chip." Input signal gates  $I_{\text{SGR}}$  and  $I_{\text{SGI}}$ , for real and imaginary channels, respectively, are clocked with same phase as  $\phi_2$ ; therefore, signal is sampled into both channels when  $\phi_2$  goes low.  $I_{\text{RGR}}$  and  $I_{\text{RGI}}$  are receiving gates for real and imaginary channels, respectively

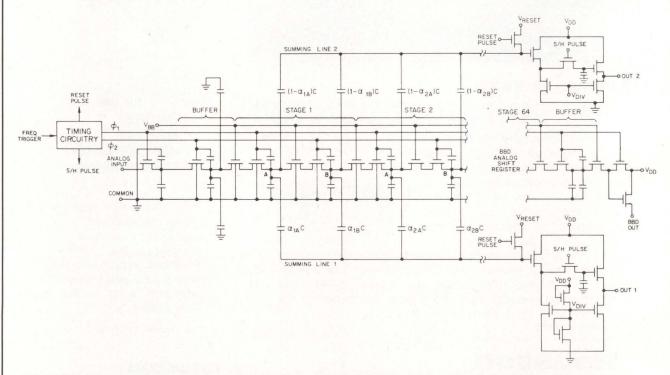


Fig 3 Equivalent circuit for Reticon BBD programmable transversal filters. Each has linear phase with no added device complexity and is electronically tunable by varying input clock frequency. Roll-off from pass band to stop band is typically >200 dB/octave, corresponding to a 33-pole filter

246

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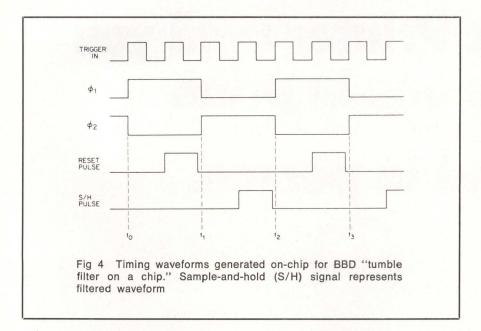
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Sampling rate is controlled by  $\phi_1$  (Figs 3 and 4) at one-fourth the frequency of the input trigger clock. At the negative transition of  $\phi_1$ , new samples of the input waveform are entered (locked) into the CTD. At the positive transitions of  $\phi_1$ , zeros (ie, a fixed threshold level) enter.

At every  $\phi_1$  clock transition the alternate pattern of signal samples and reference levels are shifted forward along the tapped structure. Each sample and reference pair is

multiplied by the weighting factors in differential manner, and all weighed pairs combine at the output.

These filters are discrete-time processors. Time is quantized, but signal amplitudes retain the analog values associated with the discrete-time values corresponding to the falling edges of  $\phi_1$  (the sample times). Behavior is that of a discrete-time or sampled-data system.

Circle 346 on Inquiry Card

# 4k HMOS Static RAMs Operate at Speeds As Low As 120 ns

Only a fraction of the power required by conventional Mos static RAMs is reportedly needed for the 7-device 2141 family of HMos 4k x 1-bit fully static random-access memories. Maximum access times (and minimum cycle times) range from 120 to 250 ns for various devices. All use a single 5-V  $\pm 10\%$  power supply and are directly TTL compatible on all inputs and outputs.

Very low power requirements are combined with fully static operation. Maximum operating currents range from 40 to 70 mA and respective maximum standby currents range from 5 to 20 mA. Power reduction is achieved automatically without the need for a clock, address setup and hold times, or edge activated operation.

Announced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, the 2141 family is directly interchangeable with that company's 2147 static RAMS, which operate at maximum access times as low as 55 ns. Both families are fabricated with HMOS (high-performance n-channel silicon-gate MOS) technology.

Prices range from \$18.75 to \$26.80 for 18-pin plastic DIPS in quantities of 100 to 999. Cerdip devices in the same quantities range from \$21.45 to \$29.50.

Circle 347 on Inquiry Card

# 70-ns Multiplexer/ Accumulator Can Be Communications Filter

A monolithic, multifunction arithmetic device that can perform 8 x 8-

bit multiplication/accumulation in only 70-ns has been introduced by TRW's LSI Products Div, 3435 Wilshire Blvd, Los Angeles, CA 90010. The TDC1008J can be used as either a multiplier or a multiplier-accumulator. It also features controllable addition or subtraction in a 19-bit accumulator-subtractor.

Designed as a central arithmetic block for both recursive and non-recursive digital filters, and particularly fffts, the device is said to provide much faster operating time than MSI equivalent multipliers and is suited for telecommunications filtering applications.

In addition to the accumulation registers on the output, input registers are included on-chip. A round control also is provided in the 2's complement or unsigned magnitude multiplier. Inputs and outputs are TTL compatible. Three-state outputs are standard.

Circle 348 on Inquiry Card

# 64k-Bit ROM Doubles Storage in µP Systems

A 64-bit read-only memory, organized in an 8k-word by 8-bit configuration and requiring 200-mW power typically, is being produced by Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803. The A88XX can be interchanged with A66-, A52-, and A05-ROMS in the company's existing PPS-4 and -8 microprocessor systems by inserting the device directly into the socket. Because bus interface electronics are included on the chip, there is no need to change boards when substituting these ROMS.

Functionally, the A88XX ROM is similar to the A66XX ROM except that the A88XX ROM provides twice as much storage capacity. Pinouts and external circuitry are similar except pin 5 is an additional chip select input (AS7) that can be used for bank switching in new system applications (diagram). AS5, AS6, and AS7 have the strap option of "don't care" (always selected).

This 42-pin package has been designed with dynamic address decoded logic for interface compatibility with the PPS CPU. It is programmed with a custom mask and is primarily used to store 8-bit instructions for control and sequencing of data within a PPS set. The ROM's 13 address and

# Eclipse and Nova Users, Take Note.

# The MSC-1300 single board, CPU resident, disk controller is here.

And it's big news for a number of reasons. One, because the MSC-1300 can accommodate up to four disk drives with industry-standard interfaces, allowing the host Eclipse or Nova to access up to 1200 megabytes of on-line storage. Two, because the MSC-1300 is microprocessor-based, delivering reliability and performance features now so critical—and, before now, unattainable. And three, because the MSC-1300 is microprogrammable, thus achieving the flexibility and efficiency to support all popular drives, even the Winchester fixed media type.

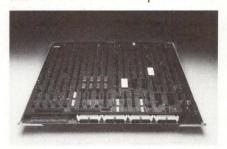
# You can't buy more. You probably shouldn't buy less.

The MSC-1300 has it all. Error correction, a data integrity "must" these days. Sophisticated I/O channel techniques that dramatically increase overall system throughput. Sector chaining. Extended diagnostics. Overlap and implied seek. Automatic alternate track.

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Programmable sector interleaving and extra data buffering that together accommodate variable system data rates without memory hogging or data misses. And any number of CPU resource-wasting tasks — command chaining, data chaining and key word processing.

Side by side, more important fea-tures wind up on the MSC-1300 side than on that of our competitors. And



The noteworthy MSC-1300 CPU resident disk controller.

not necessarily at the expense of expense. Discounting the occasional controller that offers little but price, the best controller, ours, comes in for about the same money as the good ones. And often, even less money.

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Of course, there is more to minicomputers than Data General's. Which is why there is more to Microcomputer Systems than the 1300. Our 1000 Series, for instance, is considered by many as the "consummate controller" for a wide range of minicomputer operating systems. Like the 1300, it reflects a dedication to "conception through product" development of microprogrammed controllers a year or two ahead of the pack.

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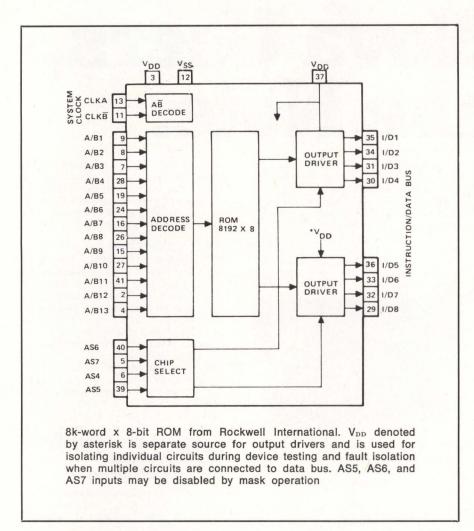


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CIRCLE 139 ON INQUIRY CARD

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four chip select inputs provide for direct selection of up to 16 ROM chips (131k words of instruction).

Operating characteristics include  $V_{\rm DD}$  of  $-17~V~\pm5\%,~V_{\rm SS}$  of 0 V (ground), system operating frequency of 199 kHz, device power consumption of 410 mW max, input capaci-

tance of <5 pF, and input leakage of  $<10~\mu\text{A}$ . Operating temperature range is 0 to 70 °C.

Prototypes are available four weeks after ROM code approval. Prices are \$37.65 in lots of 100, \$12 in large volume.

Circle 349 on Inquiry Card

# CCD Serves as Driver For MOS RAM Inputs

A CCD memory driver IC, the SN7536NE, introduced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 is offered in a 2-W 14-pin plastic DIP (NE suffix) with six internally connected heat sink pins for improved heat dissipation. Package leads fit standard 14-pin sockets.

The device is an interface circuit for use between TTL and high current, high voltage systems and drives high capacitive loads at frequencies ranging from 1 to 5 MHz. It also may be used to drive the chip-enable clock input of the TMS3040 MOS RAM as well as address, control, and timing inputs for other MOS RAMS.

Operation is from standard bipolar and mos supply voltages. The device has been optimized for operation with  $V_{\rm CC2}$  supply voltage from 11 to 15 V and with nominal  $V_{\rm CC3}$  supply voltage from 0 to 4 V higher than  $V_{\rm CC2}$ . In most CCD applications, the  $V_{\rm CC3}$  power supply can be eliminated by jumpering  $V_{\rm CC3}$  and  $V_{\rm CC2}$  pins.

Circle 350 on Inquiry Card

# p/ROMs and SPROMS Offer 70% Power Reductions

Four 4k devices announced by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040 consist of two standard programmable read-only memories (the 29620 for the opencollector version, and 29621 for the 3-state version) and two p/ROMS with built-in power switching (sproms) (the 29622 for the open collector version, and the 29623 for the 3-state version). The standard p/ROMs have a 65-ns access time over the commercial temperature range with an 80-ns access time for the military temperature range. The sproms have an access time of 70 ns for the commercial range and 85 ns for the military.

The sprom devices offer a power savings of up to 70% when used in place of conventional p/Roms. Overall system power can be reduced by onchip power switches which turn off most of the internal circuitry for unselected devices.

Maximum power dissipation for both groups of p/ROMS, when selected, is 850 mW. When not selected, the 3-state version of the sprom dissipates 250 mW.

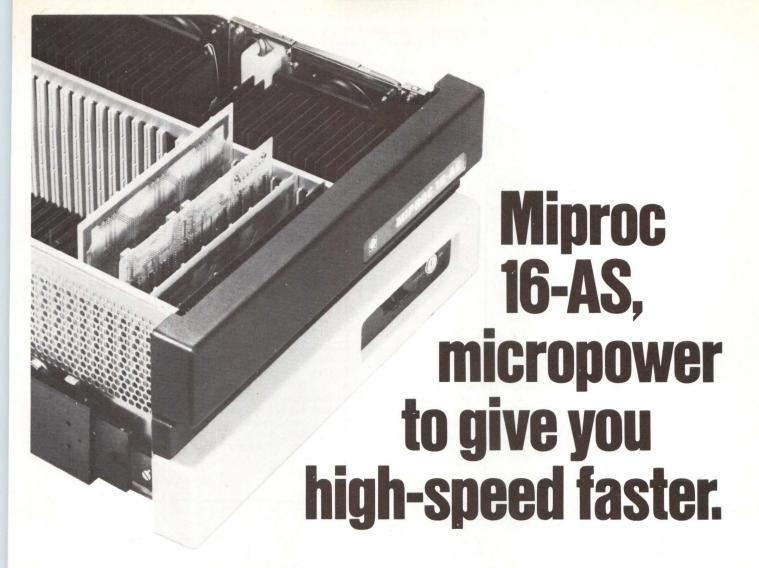
Circle 351 on Inquiry Card

# Single CMOS Chip Is Complete Data Acquisition System

Chopper stabilized comparator, 16-channel multiplexer, 8-bit analog-to-digital converter, Tri-State® latched output buffer, and all control logic are housed in a single low power CMOS device. The 40-pin DIP, essentially a complete data acquisition system on a monolithic chip, requires only a single 5-V supply and consumes 15 mW, worst case.

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has introduced the INS8292 as one of its line of INS8080A microprocessor products that interface with the universal Microbus™ system and data, address, and control bus functions

The 16-channel multiplexer accepts single-ended analog signals from ratiometric sensors or transducers where the change in value is measured instead of absolute value. Channels are selected by an internal 4-bit address decoder. Address setup and hold times are typically 25 ns each. Typical capacitance at the multiplexer input is 5 pF, typical off-



Internationally acclaimed Miproc-16 with a compute-rate of up to 4 million instructions per second is the fastest 16-bit microcomputer card family available.

Now supplied with an OEM chassis package, Miproc-16 is even more quickly brought into action. This cost-effective application system, named Miproc-16 AS, has room for one, two or even three Miproc-16 CPU's. Smartly styled and equipped with add-in 13-slot card bay modules, fans and power supply, this new OEM chassis package eases the way into high speed microcomputing.

#### **Instruction Power**

Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

#### 16-bit Power

16-bit program words make programming easy. 16-bit data words maintain high precision in arithmetic operations.

#### Addressing Power

16-bit dual memory architecture gives 65k words of directly addressable program memory *and* 65k words of data memory with 8 powerful address modes.

#### **Interrupt Power**

Multilevel, priority vectored interrupt system handles context changes in less than 2 microseconds.

#### I/O Power

256 directly addressable I/O channels with data I/O rates of up to 1.7 megabytes/sec. under program control, and up to 20 megabytes/sec. for DMA.

#### High Speed Processing Power

The unique dual memory architecture combines with high speed Schottky TTL technology to execute most instructions in a single machine cycle.

#### **Software Power**

Easy to use cross-assemblers for mainframe or minicomputer make programming faster, *and* PL-MIPROC, a super-efficient high level assembly language.

#### **Hardware Power**

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#### **Ruggedized Power**

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#### AROUND THE IC LOOP

channel leakage current is 10 nA, and typical on-resistance is 1.5 k $\Omega$ .

Multiplexer output and comparator input are separately pinned out, which permits channel expansion using other multiplexers into the INS8292 ADC. It also accommodates signal conditioning such as prescaling, sample and hold, signal preamplification, and standard-signal insertion for absolute measurements.

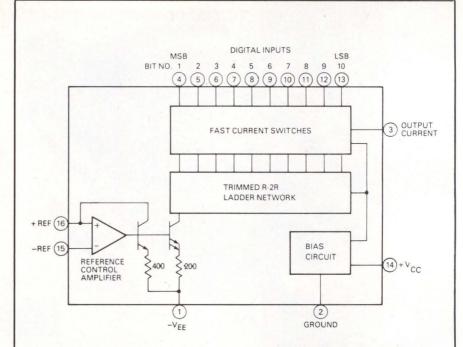
A chopper-stabilizer comparator minimizes the effects of temperature, long term drift, and input offset errors, increasing accuracy of the entire 8-bit conversion process. Chopper frequency typically is 640 kHz. It may also function at any clock frequency from 10 kHz to 1.2 MHz.

The ADC uses successive approximation techniques through a 256-step (256R) register-ladder network rather than the conventional 2-value network (R-2R). This procedure provides consistent reference-voltage loading, eliminates missing conversion codes, and provides guaranteed monotonicity important in closed loop systems.

Maximum linearity error, zero error, and full-scale error are not more than ±½ LSB each; a total unadjusted error, the sum of all three, does not exceed ±½ LSB. Absolute accuracy—the difference between actual input voltage and the equivalent binary output, including quantization errors and all other errors-is specified as ±1 LSB. Conversion time, using a 640-kHz clock, is typically 100 us. Multiplexer delay time is less than 2.5 µs. Converter output is through on-chip Tri-State latched buffers. Output capacitance is 5 pF/buffer. Operating temperature range is -40 to 85 °C; storage temperature range is -65 to 150 °C.

#### 10-Bit DAC Offers 250-ns Settling Time

DAC-1C10BC, a monolithic D-A converter with 10-bit resolution, achieves a 250-ns settling time for a full scale output change. It requires only an external reference and operational amplifier for voltage output operation. With a fast 1C op amp, a 10-V output change can settle within 1  $\mu$ s. Digital inputs accept positive true logic; and input coding is straight binary for unipolar operation, offset



Block diagram of Datel Systems 10-bit monolithic bipolar DAC. Device incorporates 10 fast switching current sources which drive diffused resistor R-2R network, and contains both reference control amplifier and bias circuit. External 2-mA reference current is required at +Ref input terminal (accomplished by external voltage reference and metal film resistor)

binary for bipolar. Logic inputs are compatible with TTL and CMOS.

Linearity is  $\pm \frac{1}{2}$  LSB typical and  $\pm 1$  LSB maximum. Gain tempco is -20 ppm/°C. An external reference current programs the scale factor and may be varied over a 4 to 1 range. Output current is 0 to 4 mA with an output voltage compliance of -2.5 to 0.2 V, permitting direct drive of a 625- $\Omega$  resistor for a voltage output.

Other characteristics include ±1bit linearity with monotonicity guaranteed at room temperature (25 °C). Reference input current can be varied from 0.5 to 2 mA to give monotonic operation as a 1- or 2-quadrant multiplier. Power supply requirement is 5 and -15 Vdc. Typical power dissipation is 220 mW. Operating temperature range is 0 to 70 °C.

The 16-pin ceramic DIPs are available from Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021. Pricing is \$10.95 in 1 to 24 quantity. Circle 352 on Inquiry Card

#### 12-Bit CMOS DAC Features 4-Quadrant Multiplier

A true 12-bit monolithic CMOS D-A converter, the AD7541 introduced by Analog Devices Semiconductor, 829 Woburn St, Wilmington, MA 01887 is available in both 0.01% and 0.02% accuracy versions. However it is pincompatible with the company's earlier AD7521 which has 0.05% accuracy.

The device features full 4-quadrant multiplication. No circuit changes are necessary to function with both positive and negative references, either ac or dc. It can provide 0.01%

linearity for digitally-controlled gain or attenuator circuits, synchro/digital converters, digitally-controlled power supplies, ratiometric low power converters, and other such applications.

Since only 15-V power is required, the DAC can be used for battery and other low power instrument requirements. Inputs are scaled to interface to either TTL or CMOS levels.

Maximum settling time is 1 µs. Feedthrough error is <½ LSB at 10 kHz and maximum supply current is 2 mA. Six versions are available for operation over the 0 to 70, -25 to 85 °C, or extended -55 to 125 °C temperature ranges.

Circle 353 on Inquiry Card

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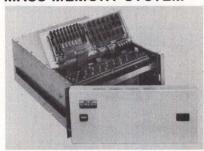
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The MODEL EIGHTY features totally new head/disc magnetics, highly efficient data coding, modern electronic read-back signal equalization, balanced line/driver receivers in the external signal interface for maximum noise immunity, and advanced packaging concepts to minimize equipment size while maximizing ease of access to all replaceable parts.

The MODEL EIGHTY is compatible with ALPHA DATA's computer controllers for Data General and DEC computers. A simple change of one interface card permits emulation of other manufacturers' products.

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#### AROUND THE IC LOOP

#### Hi-Rel ADC Converts In 2.8 µs

ADC541-8 series 8-bit A-D converters are now offered by Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730 with conversion time of 2.8 μs. This 350% speed improvement over the earlier version will expand application opportunities where MIL-STD-883A, Class B processing is required. The device includes precision DAC, clock, comparator, reference, and successive approximation register.

Units are also available processed for commercial/industrial microprocessor applications. All models in the series are hermetically sealed in 24-pin metal DIPs.

Simple pin-jumpering allows the user to select from three unipolar and three bipolar input ranges. Output coding in the bipolar mode is user-selectable as either offset binary or 2's complement codes. The overall temperature coefficient is ±45 ppm/°C and long term stability is 0.1%/yr.

Operating temperature range for the MIL-STD-883A, Class B version is specified at -55 to 125 °C. The range for the commercial/industrial version is -25 to 85 °C.

Circle 354 on Inquiry Card

#### Programmable Counters Feature 3-State Outputs

Am25LS2568 and Am25LS2569, 3-state counters fabricated with low power Schottky technology, are respectively programmable up/down BCD and binary counters. They feature maximum clock-to-output delay of 27 ns. A ripple carry output allows cascaded operation by connecting to the succeeding device. Clock carry output provides a glitch-free pulse for clock driving.

These devices from Advanced Micro Devices Inc, 901 Thompson Place, Sunnyvale, CA 94086, replace up to five ssi and Msi packages previously required to implement the equivalent function. They are available in the space-saving 20-pin molded and ceramic dual-inline and flat package for use over commercial and military operating temperature ranges.

Circle 355 on Inquiry Card

#### BiSync/SDLC Chip Operates in Fullor Half-Duplex Modes

An n-channel Mos synchronous receiver/transmitter chip that can handle either binary-synchronous (BiSync) or synchronous data link control (SDLC) protocols in microcomputer systems has been announced by NEC Microcomputers, Inc, 5 Militia Dr, Lexington, MA 02173. The uPD379 can operate in full- or half-duplex mode; is directly TTL compatible; has 3-state data outputs; has a programmable synchronous word (character); contains detection/rejection of flag, abort, and idle patterns; has

zero insertion and rejection; and has an indication of overrun and underrun errors. Operation of the 42-pin ceramic DIP is at 800k bits/s.

Operating mode, baud rate, and synchronous character can be changed through external control for modems, CRTS, and other terminals. Devices using this chip can be updated to handle the more advanced SDLC communications protocol through software commands rather than by redesign of the equipment.

#### Bipolar LSI Circuits Involved In Alternate Source Agreement

Monolithic Memories, Inc, Sunnyvale, Calif and Raytheon Semiconductor, Mountain View, Calif have agreed to alternate-source certain of each other's proprietary bipolar LSI IC products. The second-source pact calls for mutual exchanges of logic drawings, circuit diagrams, design tapes, certain process information, assembly and packaging procedures, and other technical and test data necessary for complete device characterization. In addition, there will be a 2-way transfer of related product and application services.

The companies have also agreed to conduct joint discussions on "customer programmable logic components" which could lead to future product exchanges. First devices to be exchanged under the agreement are Monolithic Memories' FIFO and 8 x 8 multiplier, and Raytheon Semiconductor's power-switched p/ROMS (SPROMS) and programmable multiplexer (PMUX).

# Meet a couple of low cost Slowpokes in our high speed 1200 Series family: ChainTrain® Models 1260/1290.

Data Printer Corp's 1200 Series of ChainTrain high speed Line Printers includes a pair of low cost, lower speed printers that offer the advanced features of our 1200 LPM Models—motorized upper and lower tractor positioning; complete microprocessor control; heavy duty reliability—plus plug-to-plug compatability and 95%

parts commonality. Just about the only two important things you don't get are the high speed and the high price tag!

Our ChainTrain 1260 trots along at 600 LPM's, but costs no more than our conventional 600 LPM Printers. The Model 1290 jogs along somewhat faster at 900 LPM's and is also competitively priced with conventional 1000 LPM counterparts.

If you've always admired the ChainTrain 1200's features, but didn't need 1200 LPM speed, check out this pair of Slowpokes. There are already thousands in the field—all being utilized to maximum advantage. We'll give you a free 30 day comparison trial and/or all the specs you need. Give us a call.

#### **Data Printer Corp**

99 Middlesex Avenue, Malden, MA 02148, Tel: (617) 321-2400, TWX: 710-348-0794 Sales Offices: Costa Mesa, CA, Clifton, NJ, San Jose, CA

CIRCLE 143 ON INQUIRY CARD



Visit Data Printer Corp. at the National Computer Conterence, Anaheim, California, June 5-8, Booth 1261.

#### PRODUCT FEATURE



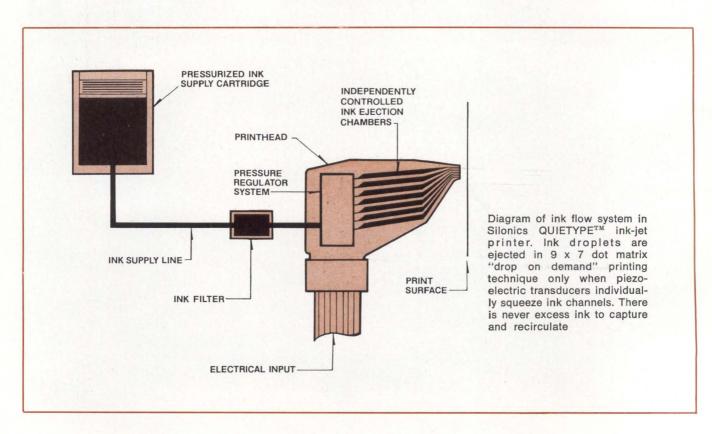
See at NCC Booth 3122



Ink-jet printing—the imprinting of characters on untreated paper by controlling a jet of ink drops—has passed through several research and development stages over the past decade and a half in several countries. Most resulting printers offered to the market have been relatively expensive and, in some cases, unreliable.

A major problem area has consistently been the ink-jet phase itself. Now, however, a U.S. company, Silonics, has announced a low cost ink-jet printer that promises high reliability through use of a simple but effective ink delivery system. Called QUIETYPE<sup>TM</sup>, this 180-char/s OEM printer is aimed at mini- and microcomputer based systems where dependability and low price are critical considerations.

#### **High Reliability to Small System Manufacturers**



#### **Functional Description**

Much of the QUIETYPE printer's hardware simplicity and reliability results from printhead design. Printing occurs when ink droplets are selectively ejected from a 7-nozzle printhead (diagram) as it traverses the page. Patterned combinations of ink droplets are ejected in a manner somewhat analogous to the action of a wire matrix printer; however, this ink-jet printing technique is based upon flexing a plastic part rather than accelerating and impacting mechanical parts.

Piezoelectric transducers individually squeeze ink channels to dispense ink, a technique known as "drop on demand" printing. A pressurized disposable ink cartridge supplies ink to the printhead through a flexible tube. The head, which weighs 50 grams, incorporates a pressure regulator system that continually replenishes ink that has been ejected. Each of seven nozzles is fed by its own channel and related piezoelectric transducer. Upon receiving an electrical pulse, the transducer flexes and deforms one wall of the ink channel. This abrupt reduction of channel volume causes an ink droplet to be expelled from the nozzle and propelled toward the paper.

Ink drops are expelled only when needed to form part of a 9 x 7 dot matrix. Since no surplus drops are produced there is no need for capture and recirculation of excess ink. Ink is never exposed to air until the instant the droplets are ejected toward the paper. There are no impacting parts or pumps involved in the ejection process.

#### **Operating Specifications**

The basic asynchronous printer operates unidirectionally at 180 char/s, 80 char/line, 65 lines/min; or optionally compressed at 210 char/s, 132 char/line, 46 lines/min. As an option, it can print bidirectionally using a motion-miniaturization algorithm to maximize throughput. Bi-

directional speeds are 180 char/s, 80 char/line, 123 lines/min; or optionally compressed at 210 char/s, 132 char/line, 90 lines/min. Line spacing is switch selectable at 6 or 8 lines/in (2.4 or 3/cm).

A 64-char ASCII set is printed at 0.10" (2.54 mm) character spacing, or optionally at 0.06" (1.5-mm) in compressed form. Line advance time is 40 ms. Electronic interface is 8-bit parallel standard; RS-232 is optional.

Normally, printing is on a self-contained 300- to 450-ft (91- to 137-m) long, 8.5" (21.6-cm) wide roll of standard class II teleprinter paper. However, even better quality print can be obtained by using a slightly more expensive fine white paper. Ink cartridge capacity is 50 cm<sup>3</sup>, or 6 x 10<sup>6</sup> characters (about 3000 pages).

Power requirements are 1.25 A, 115 V  $\pm 10\%$  or 0.63 A at 230 V  $\pm 10\%$ , 47 to 66 Hz. Operating environment is stated as 40 to 104 °F (10 to 40 °C), 20 to 80% humidity,  $\pm 15$ -deg attitude from horizontal. Non-operating environment is 15 to 131 °F (-6 to 55 °C), 10 to 90% humidity, with no attitude restrictions. The unit meets UL, IEC, and CSA safety standards.

Physical size is 7.0" high, 18.1" wide, 18.5" deep (17.8 x 46.0 x 47.0 cm). Weight, excluding paper, is 25 lb (11.3 kg).

#### **Price and Delivery**

Single-unit price for a fully-featured bidirectional QUIETYPE printer with an RS-232 interface is \$2495.00. An ink cartridge is priced at \$17.50. OEM-quantity discounts are offered on printers, ink cartridges, and mechanisms. Delivery of production quantities will begin in the third quarter of this year. Silonics, subsidiary of System Industries, Inc, 525 Oakmead Parkway, Sunnyvale, CA 94086. Tel: 408/732-1650.

For additional information circle 209 on inquiry card.

#### Intel compatible data acquisition system for only \$495\*

The low-cost ADAC Model 735 series of data acquisition systems is mounted on a single PC board that plugs into the same card cage as the Intel SBC-80/10, and SBC-80/20 single board computers and also the Intel MDS-800 microcomputer development system. The Model 735 bus interface includes a software choice of program control or program interrupt and a jumper choice of moment, managed L/O crisical ded L/O.

memory mapped I/O or isolated I/O. The basic 735 OEM system which is contained on a single PC board (12" x 6.72" x 0.4") consists of 16 single-ended or 8 differential analog input channels, either voltage or current inputs (4-20 mA or 5-50 mA), 12 bit high speed A/D converter, sample and hold and bus interface. The throughput rate of the Model 735 is 35 KHz. Optionally available is the capability of expanding on the same card to a total of 64 single ended or 32 differential voltage/current inputs. up to two 12 bit D/A converters, software programmable gain amplifier with auto zero circuit, scope control and third wire sensing.
ADAC Corporation, 15 Cummings

ADAC Corporation, 15 Cummings Park, Woburn, MA 01801. (617) 935-6668

\*Price in quantities of 1 to 4.



#### System Tests PC Boards Containing Microprocessors and Associated LSI Devices

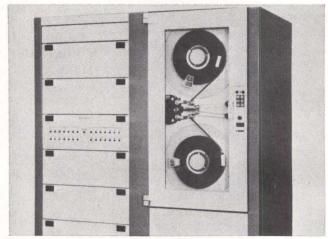
The L135 test system provides the capability of emulating the system environment of most LSI boards. With a high degree of controllability, the system permits detection of design- and device-related failures as well as manufacturing faults. Basic configuration offers economical testing of relatively simple SSI/MSI digital boards; hardware and software modules are available for extending integrated testing and diagnosing capability to handle increasingly complex boards containing analog circuitry as well as microprocessors and LSI devices. Major features include the Electronic Knife which is a diagnosing tool for pinpointing faults on bus lines down to the device level, and expanded pin and memory capacity for handling boards with up to 444 pins. In addition to clock rate testing up to 5 MHz, the system tests at static rates. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.



Circle 210 on Inquiry Card

#### High Density Digital Storage and Retrieval System Has Error Detection and Correction Capability

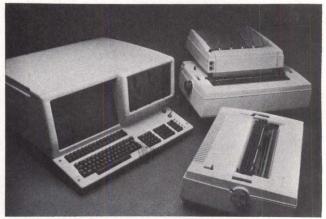
Achieving error-free recording at high data rates, System 100 operates at up to 100M bits/s on 28 tracks with packing density of 33k bits/in (1299/mm) on 1 transport. Multiple transports may be synchronized and run in parallel to increase I/O data rates to 300M bits/s. EDAC<sup>TM</sup> error detection and correction capability produces error-free data on std, noncertified, instrumentation recording tape, achieving bit error rates of 1 x 10<sup>-10</sup> to 1 x 10<sup>-12</sup>. EDAC longitudinally and laterally scans recorded tracks for variations of odd and even parities, word lengths, and word cycles; this is done in several loop operators to assure data bit correction. The system operates at tape speeds of 1 to 135 in (2.5 to 343 cm)/s, and includes bidirectional data address search and built-in test equipment. **Bell & Howell, Datatape Div,** 300 Sierra Madre Villa, Pasadena, CA 91109.



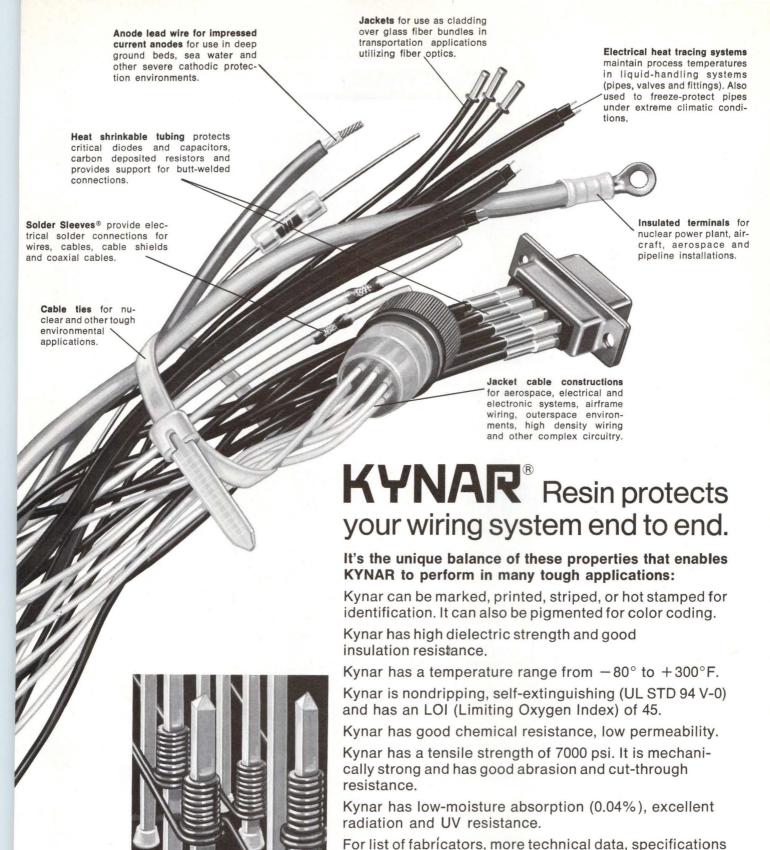
Circle 211 on Inquiry Card

#### Desktop Computer Adapts to Applications, Operating As a Standalone System or in a Network Environment

System 85 is a self-contained computer with programmable keyboard, built-in 1920-char display, Shugart dual floppy disc drives, and up to 64k of RAM enabling it to be tailored to handle both word and data processing applications. CPU architecture has an Intel compatible Multibus structure and 8085 microprocessor. Either minidiskettes having 80k char of storage capacity or std diskettes having 200k char may be specified. The system also accommodates from 2 to 4 single- or dual-headed drives. Communications can be asynchronous, bisynchronous, or synchronous at programmable baud rates from 50 to 19.2k in polled, interrupt, dial-up, or online environment. Various protocols can be emulated. The system is Intel PL/M compatible; multiple languages and specialized software packages are available. Odell Industries Corp, 2351 Charleston Rd, Mountain View, CA 94043.



Circle 212 on Inquiry Card



Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels. (UL and military), write or call Joe Michaud. Plastics Department, Pennwalt Corporation, Three Parkway,

Philadelphia, PA 19102. (215) 587-7520.

\*KYNAR is Pennwalt's registered trademark for its polyvinylidene fluoride resin.

Solder Sleeves is a registered trademark of Raychem Corporation.



#### DATA COMMUNICATION INTERFACE FOR PERIPHERALS

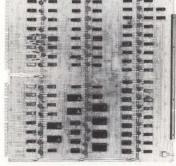


Peripherals such as typesetters, paper tape punches, editing terminals, minicomputers, and printers are adapted to BSC protocol by this microprocessorbased interface. BSC protocol provides error checking and retransmission of data blocks containing errors. Interface allows compatibility with IBM 360/370, Univac 9000 series, and other computers that communicate using BSC. It may be used with modems over the dial-up network at 1200 baud, or up to 9600 baud over leased lines. Epic Technology, Inc, 807 SE 10th Terr, Deerfield Beach, FL 33441.

Circle 213 on Inquiry Card

# High-Speed Multiply-Divide-Shift plugs into NOVA 2 NOVA 1200 and 800 series





SINGLE UNIT PRICES NOVA 2 — \$1,400 NOVA 1200 — \$2,000 NOVA 800 — \$2,400 DISCOUNTS IN OEM QUANTITIES.

Speed up program execution with this "15 x 15" arithmetic unit. It's fully compatible with Data General software.

UNITECH & DATA GENERAL HARDWARE COMPARISONS, EXECUTION TIME IN **MICROSECONDS** 

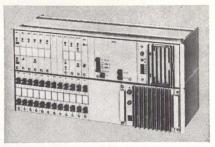
Operation	NOVA 1200		NOVA 800		NOVA 2	
	UNITECH	DGC*	UNITECH	DGC*	UNITECH	DGC*
MUL	3.75	3.75max.	3.6	8.8	3.6	5.5
DIV	4.35**	4.05max	3.6	8.8	3.6	5.8
SHIFT	3.75	Feature	3.6	Feature	3.6	Feature
		not available	)	not availab	le	not available

<sup>\*</sup>Published execution time for an UNSIGNED operation.

Two options available at \$100 each: "signed multiply" for performing two's complement multiplication (thereby eliminating software sign correction); and a "high-speed" option that cuts execution time for signed and unsigned multiplication and division, and for shifts.



#### uprocessor-controlled TDM **FOR DATA NETWORKS**

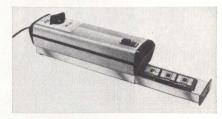


Speed range of the ZD-1000-Cl is from 50 through 300 baud, with code framed from 7.5 to 11 unit length elements. It can be used in standalone mode or linked to a parent TDM system for a total 64k-bit/s bit stream, and transmits according to either CCITT A or B standards. On the MUX side, total bit stream is 2400 or 4800 bits/s; at 2400 bits/s, max system capacity is 46 channels at 50 baud. The unit can transmit switching and signaling criteria, and can be incorporated into existing dial-up or dedicated circuits. Data Communications Div, Siemens Corp, 186 Wood Ave S, Iselin, NJ 08830. Circle 214 on Inquiry Card

#### **ADJUSTMENT-FREE 8-BIT DAC**

Four times the accuracy normally associated with 8-bit DACs is claimed for the DAC336-8, factory pretrimmed to ±0.05%. Pin jumpers allow choice of 0 to -10, 0 to 10,  $\pm 5$ , and  $\pm 10$  V outputs. Power required is 200 mW. Unit accepts TTL, DTL, and 5-V CMOS logic levels and delivers 5 mA min at ±10 V. Hybrid IC design includes 4-μs (LSB) settling time, ±1/2-LSB max linearity, and accuracy tempco of ±50 ppm/°C (max) over operating range of -55 to 125 °C. Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730. Circle 215 on Inquiry Card

#### **EPROM ERASING LAMPS**



Two compact UV lamps, PE-14, designed especially for small systems users and hobbyists, and PE-14T, with a 60-min timer for automatic shut-off, can erase up to 6 EPROM chips in 14 min. Units feature a high intensity UV lamp, specular reflector, and V-shaped holding tray to hold up to 6 chips at a constant exposure distance. Safety interlock prevents operation unless tray is fully inserted. Spectronics Corp, 956 Brush Hollow Rd, PO Box 483, Westbury, NY 11590.

Circle 216 on Inquiry Card

<sup>\*\*</sup>For Unsuccessful Division (overflow) = 3.15 microseconds.



# Alumax Mic-6 cast aluminum plate. All it needs are your finishing touches.

By the time our Mic-6 cast plate reaches you, the tough work has already been done. It's been stress-relieved, precision-machined and cut to size. All you do is finish it.

What can you do with it? Almost anything. Mic-6 can be sawed, drilled, tapped or milled. And it can be welded or anodized. All at speeds compatible with today's processing equipment.

Mic-6 is held to exceedingly close tolerances. Plate thickness is  $\pm .005$ ". And its fine, precision-machined surface finish (typically 25 micro-inch) eliminates the high costs of in-plant surface machining.

All in all, it's the "answer material" for computers, printing systems, instrumentation, electronics and other high-spec OEM industries. It saves you the costs of permanent mold castings. And frees you from the eccentricities of wrought plate.

See your nearby Alumax distributor. Or write for the Mic-6 brochure that gives you complete information and specs.

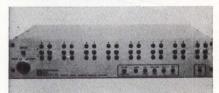
Mic-6 cast aluminum plate from Alumax. We started it, you finish it.



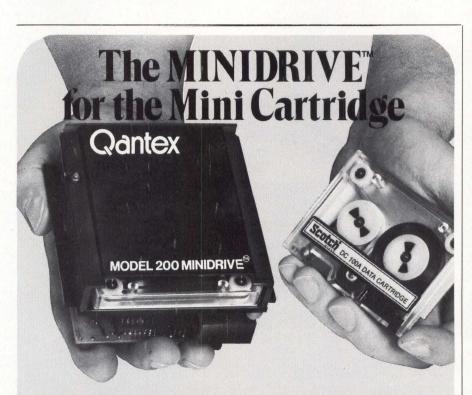
A subsidiary of Alumax Inc. 5555 E. Highway 6, Morris, Ill. 60450 West Coast office: 1495 Columbia Avenue, Riverside, California 92507

CIRCLE 147 ON INQUIRY CARD

#### MASTER PANEL FOR REMOTE CONTROL SYSTEM



Individual remote control and status display, for up to 16 channels of A,B switching from a central site via an asynchronous dial-up link, are provided by model 8933. Microprocessor-controlled unit can switch up to 256 remotely-located cages. In operation mode, front-panel LEDs indicate the status of the remote 16-channel system in an FDX mode. In status mode, the position of each remote switch is periodically interrogated to update LED display. International Data Sciences, Inc, 100 Nashua St, Providence, RI 02904. Circle 217 on Inquiry Card



#### 4"x 3"x 4"/Hi Performance/Lo Power One Moving Part/Hard Mounted Motor

	DENSITY		
No.	800 bpi	1600 bpi	
Tracks	1 or 2	1 or 2	
Capacity (bytes) 1 Track	160,000	320,000	
2 Tracks	320,000	640,000	
Transfer Rate (bits/sec)	24,000	48,000	
Speed Read/Write Rewind/Search	30 ips 90 ips		

#### AVAILABLE WITH:

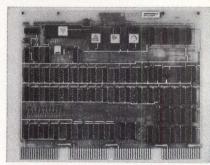
- READ-AFTER-WRITE HEAD
- PIA INTERFACE
- READ/WRITE ELECTRONICS
- MOTION ELECTRONICS
- MOUNTING FRAME



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See us at NCC, Booth 1213-1215.

#### DATA SECURITY BOARD FOR MINICOMPUTERS



A complete encryption system on one board, the DES1100DSM is compatible with the DEC PDP-11, relieves the computer from time-consuming tasks, and minimizes software impact. Module enciphers data using the cipher feedback (CFB) or cipher block chaining (CBC) encryption mode. A custom single-chip n-MOS LSI device implements the NBS data encryption standard algorithm. An M6800 microprocessor is the heart of the system, and handles the tasks of DMA transfer and encryption. Motorola, Government Electronics Div, 8201 E McDowell Rd, Scottsdale, AZ 85252. Circle 218 on Inquiry Card

#### FIBER-OPTIC LINK KIT



Housed in an executive style brief case, the Fibre Link 3100 series engineers' kit contains everything needed to assemble working fiber-optic data links. Kit includes a selection of transmitters, receivers, connectors, ferrules, and an automatic terminator tool, together with 30-m of sheathed polymer optical fiber and various accessories, and a set of application notes. **Intrade, Inc,** Box 608, Litchfield, CT 06759.

Circle 219 on Inquiry Card

#### **SWITCHING POWER SUPPLIES**

Six models ranging from 5 Vdc at 20 A to 28 Vdc at 3.6 A make up the S series. Max power is 100 W. Line and load regulation is 0.1% and ripple and noise ratings are 50 mV pk-pk or 0.5%, whichever is greater. All units include integral overvoltage protection, 20 ms min hold-up for loss of line, and 92 to 130/184 to 260-Vac, 47 to 450-Hz input ratings. All units meet UL 478. Max dimensions 9.5 x 4 x 2.5" (24 x 10 x 6-cm); approx weight 3 lb (1.35 kg). Deltron, Inc, Wissahickon Ave, North Wales, PA 19454.

Thanks to the N123's interactive programming, non-technical people can do what programmers do. And non-technical people are a lot easier to find these days.

The fact is, the N123 programs itself automatically from any verified backplane. Your "programmer" merely sets up the pin-naming scheme, enabling the system to print error messages in your own language.

And all this involves is using a keyboard to answer a series of questions asked by the system through its CRT display.

#### SMALL SYSTEM, BIG ADVANTAGE.

Although designed for smaller backplanes (8000 points or less), the N123 has many advantages in common with our larger, computer-controlled N151.

Easily understood error messages are one advantage. Daisy-chained fixture cards are a second. A ten-year warranty is a third.

Best of all, users of the N123 report exceptionally fast payback.

For an information package that includes both details of the system and a payback analysis, write Teradyne, 183 Essex Street, Boston, Massachusetts 02111.

# SO SIMPLE TO PROGRAM YOU DON'T NEED PROGRAMMERS.



The N123 backplane test system.



CIRCLE 149 ON INQUIRY CARD

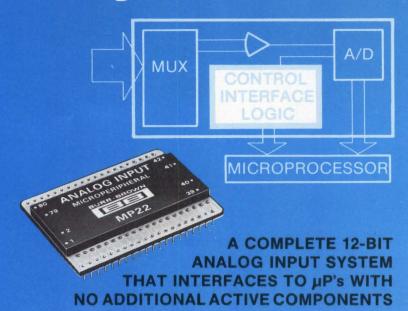
#### RECEIVE-ONLY CRT TERMINAL



An RO version of the 400E smart terminal features 24 x 80 display on a 15" (38-cm) glareless screen; upward scroll; blink, dim, and reverse video char accents; RS-232-C data; and RS-170 video interfaces. Baud rates from 110 to 9600 may be specified, and can be field-changed. Unit responds to 14 different commands. Options include 19" (48-cm) rack mounting, u/lc char display, 40-char line, double-high chars, export power, current-loop cable, bell, and CR/LF options. Dimensions are 15 x 14 x 13.6" (38 x 36 x 35 cm). Ann Arbor Terminals, Inc, 6107 Jackson Rd, Ann Arbor, MI 48103.

Circle 221 on Inquiry Card

### No One Else Does This In Hybrid Form



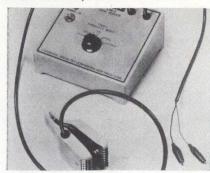
MP22 is a memory-mapped hybrid data acquisition system. Address it directly as though it were memory: one instruction acquires data and internal logic provides a choice of halt, interrupt or DMA operating modes.

MP22 contains address decoder, timing and control logic, 16 channel multiplexer, instrumentation amp and CMOS A/D converter! It's a stand-alone 12-bit device that accepts high or low level inputs and channel expansion is unlimited. Even with all these features, MP22 is contained in an 80-pin quad-inline package that measures only 2-1/8" x 1-11/16" x 3/16" high. Price \$245.00. BURR-BROWN, Box 11400, International Airport Industrial Park, Tucson, AZ 85734. Phone (602) 746-1111.



AMSTERDAM, BOSTON, CHICAGO, LONDON, LOS ANGELES, NEW YORK, PARIS, SAN FRANCISCO, STUTTGART, TOKYO, TUCSON, ZURICH

#### LOGIC STATE TESTER FOR HIGH SPEED, LOW POWER ICS



A fully isolated power supply eliminates test circuit loading in the LM-Z logic monitor. In testing, selector switch chooses between RTL/DTL, TTL/HTL, and CMOS logic families. With a black clip lead attached to ground reference on the board under test, a second red clip establishes proper threshold level for CMOS circuits. Monitor clip then clips over the IC and shows the logic state at each pin on an LED display. Max useful input frequency is 30 kHz at 50% duty cycle. Continental Specialties Corp, 70 Fulton Terr, New Haven, CT 06509.

Circle 222 on Inquiry Card

#### 100-W SWITCHING POWER SUPPLIES

D series units come in a package 5 x 9.05 x 2.25" (13 x 23 x 6 cm), with power densities from 1.02 W/in³ for the 5-V at 20-A model, to 1.48 W/in³ for the 48-V at 3-A unit. Electrical specs: line range, 95-135 V rms; ripple and noise, 100 mV pk-pk max; line regulation, ±0.2%, load, 0.2%. Min efficiencies range from 74% for the 5-V, 20-A model (D5S20), to 82% for the 48-V, 3-A model (D48S3). Etatech, Inc, 187-M W Orangethorpe Ave, Placentia, CA 92670. Circle 223 on Inquiry Card

#### HARDCOPY FOR MOBILE SYSTEMS



Hardcopy messages are available in vehicles with the 2002 digital mobile communications system. Microprocessor-controlled base terminal permits recall, editing, and selective calling. Messages up to 45 words can be stored and displayed; 180-word/min transmission rate saves air time. Receiver digital printer has DIP switch-programmable selective call decoding, and will operate unattended. RF Applications, 83 East Ave, Norwalk, CT 06851.

Circle 224 on Inquiry Card

### in RS-232 digital recorders

# Techtran does it best!





# New Datacassette Series

\$950. and up

... singles & duals available

- Now ANSI/ECMA compatible and TI 733, NCR...
- New character string search
- New powerful text editor
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- Microprocessor controlled

#### New Mini disc Series

only \$1395.

... much lower in OEM quantities

- Over 200K capacity per disc
- · Hi speed random file access
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Send for details today
CIRCLE 151 ON INQUIRY CARD

See us at NCC, Booth 2751

#### LARGE DIGIT LED DISPLAY ASSEMBLIES



Digit heights of more than 1" (2.54 cm) are provided in the 1000 series multidigit numeric display assemblies. Bright red display requires 5- to 10-mA forward drive current per segment in directdrive configuration. Presently available in 2- and 6-digit common anode directdrive arrangement, assemblies can be had in any number of digits with optional decimal point, colons, and ± sign. Typ specs include luminous intensity of 350 mcd at 10 mA, peak emission wavelength, 690 nm; 4.4-V forward voltage at 10 mA; and reverse current of 50 µA at 9.0 V. Opcoa, Div IDS, Inc, 330 Talmadge Rd, Edison, NJ 08817.

Circle 225 on Inquiry Card

#### HIGH POWERED ARRAY SIGNAL PROCESSORS

Application of the DEC PDP-11 to communications and medical functions is enhanced by the MSP-32, MSP-33, and MSP-34 high-powered array signal processors. MSP-32 has 3 hex-size boards. (1 control and 2 arithmetic), plug-compatible with the PDP-11 UNIBUS; it provides full 24-bit block floating point arithmetic, 8k 24-bit scratch memory, and an average 1024 complex FFT speed of under 7 ms. MSP-33 has 3 arithmetic boards, 12k scratch memory, and average 1024 complex FFT time of 4.3 ms. MSP-34, with 4 arithmetic boards, has 16k scratch memory and FFT speed of 3.3 ms. Computer Design and Applications, 377 Elliot St, Newton,

Circle 226 on Inquiry Card

#### INDUSTRIAL DATA MODEM FOR COAXIAL NETWORKS

Typical bit error rates of 1 x 10-8 are achieved at an S/N ratio of 25 dB by model 741, a high performance, low cost, broadband data modem for 0 to 9600-bit/s operation. It is designed for asynchronous FDX or HDX transmission over 2-way coaxial cable networks, in point-to-point or multipoint operation. A loopback feature permits the 741 to retransmit received data, thus testing the modem and the network from one site. The unit is supplied with an RS-232-C interface; others are available as options. American Modem Corp. 160 Wilbur Place, Bohemia, NY 11716. Circle 227 on Inquiry Card

#### MOVING HEAD DISC CONTROLLER

Up to 40M bytes storage can be added to PDP-11/03, VO3 systems using the PX-C45L. It is Q-BUS compatible and he a 5M-or 10M-byte disc drive. RT-11, FORTRAN, BASIC, and other LSI-11 software compatibility is inherent. The controller is supplied complete with bootstrap loader, 5-V 25-A power supply, slides, cardcage assembly, fans, and disc drives. An 8-ft (2.4-m) cable connects to the PDP-11/03 Q-BUS. Three prewired slots are available for peripherals. **Xylogics OEM Components Group, Inc,** 42 Third Ave, Burlington, MA 01803.



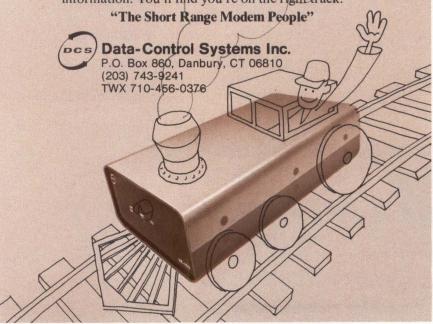
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# "Loca-Modems" Slash Local Data Commutation Costs

PRICES START AT \$240. THE ONLY WAY TO GO FOR LOW COST, SHORT RANGE DATA COMMUNICATIONS!

Data-Control Systems "Loca-Modems" are rugged, reliable data sets specifically designed to access terminals at distances up to 10 miles. At a fraction of the cost of standard modems. Available synchronous at 2.4, 4.8, 9.6 and 19.2 kbps (others optional). Or asynchronous up to 1 megabit. Equipped with remote testing switch and transmit, receive and clear-to-send LED's. Full duplex, half duplex, simplex, point-to-point and multipoint operation. Solid, twisted-pair cabling.

Call or write Data-Control Systems for further information. You'll find you're on the right track.



# Every 8080 and 6800 user needs at least one.



## AUL

# The only microsystem analyzer for both 8080 and 6800 based systems.

#### MILLENNIUM DOES IT ALL.

Other manufacturers make part of the  $\mu$ SA Microsystem Analyzer. Some make in-circuit emulators. Some make logic analyzers. And some make signature analyzers. Only Millennium combines in-circuit emulation, signature analysis and time domain analysis in a single inexpensive instrument.

UNIVERSAL.  $\mu$ SA avoids equipment obsolescence and extends your engineering capability.  $\mu$ SA supports 8080 and 6800 now. Other CPUs coming soon.

COMPLETE CAPABILITY. The  $\mu$ SA

performs functional Go/No-Go testing and isolates faults to the component level in your 8080 or 6800 based systems. It also provides pulse, frequency and transition measurements.

#### LEADING EDGE TECHNOLOGY.

Our state-of-the-art is your peace of mind. We got to the leading edge by designing test and development systems for some of the biggest names in the business. That put us so far down the learning curve that we're able to offer the only complete microsystem analyzer on the market today. µSA Microsystem Analyzer from Millennium Systems.

#### APPLICATIONS

#### LABORATORY DEVELOPMENT.

In conjunction with your software development system,  $\mu SA$  Microsystem Analyzer greatly simplifies hardware checkout and hardware/software integration. It also increases engineering productivity and enables greater design flexibility with many  $\mu Ps$ .

**PRODUCTION TESTING.** Use the  $\mu SA$  for rapid testing and quality assurance. Complete diagnostic and test programs can be easily executed for fault isolation by non-technical personnel. It reduces test set-up time, labor costs relating to operator training time and equipment requirements. And  $\mu SA$  reduces operator input error.

FIELD SERVICE. Board float inventory is increasing at an alarming rate. Turn around time and transit costs are also rising. It's estimated that 40% of board floats are good boards.  $\mu$ SA enables your serviceman to check and verify boards. Exchange and repair bad boards only. Direct reading display eliminates assumptions or interpretations by nontechnical personnel.

DEPOT/REPAIR. Rapid fault isolation makes it economical to repair or replace components at the depot level. Results: Faster turnaround. Reduced board inventory. Lowered costs.

sound interesting? Call us at (408) 996-9109 or return the coupon below. We'll send you complete information on the µSA Microsystem Analyzer.



#### MILLENNIUM

#### MILLENNIUM SYSTEMS, INC.

19020 Pruneridge Ave., Cupertino, CA 95014 Immediate information: (408) 996-9109

Gentlemen:  $\mu$ SA sounds like a breakthrough.  $\square$  Call me to set-up a demonstration.  $\square$  I would like to see a sales representative.  $\square$  Send me everything I need to know on your Microsystem Analyzer.

Name	
Commonu	

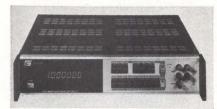
Company\_\_\_\_

Address\_\_\_\_\_

State\_\_\_\_Zip\_\_\_\_ CDO 578

CIRCLE 153 ON INQUIRY CARD

#### SMART DIGITAL **VOLTMETERS**

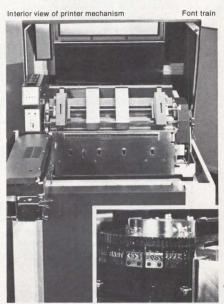


Two "Intelligent" DVMs, models 9575 (51/2 digit) and 9576 (61/2 digit), are microprocessor controlled and provide dc and ac voltage, resistance measurements, plus a choice of processing programs and interface options. Using measurements as base data, the DVMs can compute 16 various results via eight separate programs. A ninth program, using an internal clock reference, provides time control over sequence of measurements: start, stop, and interval between operations can be set on 96-h timebase. Four available interface options are BCD, binary, RS-232-C, and IEEE-488. Guildline Instruments, Inc, 2 Westchester Plaza, Elmsford, NY 10523. Circle 229 on Inquiry Card

#### CITIZEN SERIES8000 PRINTERS

heavy-duty 132 Columns 250-720 LPM **Chain Printer** Excellent Quality and Price

Manufactured by CITIZEN WATCH CO. Tokyo, Japan





If you are an OEM in the computer industry, you know the crucial importance of gaining a competitive edge. We know it, too.

CITIZEN is the largest independent line printer manufacturer in Japan. We are new in the U.S. market. A very tough market. And we are growing fast because we offer our clients a very advantageous price/performance mix. The competitive edge.

The Citizen Series 8000 Line Printers are available in two basic models, with the following minimum speeds:

Model 8201

Model 8601

298 LPM — 48 characters — 720 LPM 250 LPM — 64 characters — 600 LPM 188 LPM - 96 characters - 444 LPM

Full details on the competitive edge offered by the Citizen Series 8000 printers are yours for the asking. Call or write to:

> Mike M. Fujiwara Marketing Manager, Line Printers C. ITOH ELECTRONICS, INC. 5301 Beethoven Street Los Angeles, California 90066 Telephone: 213/390-7778

Distributed by:

C. ITOH ELECTRONICS, INC.

#### MODULAR IC PACKAGING



One rack assembly can handle variety of panel sizes, IC densities, and userselectable voltages using the "Mixer." This system will accommodate panels ranging in size from 4.5 x 6" to 8 x 14.9" (11 x 15 to 20 x 38 cm), with 32 to 192 ICs. Panels, having from 108 to 540 I/O pins, are available in all sizes, each with one, two, or three voltage planes. System design allows logic to be subdivided into multiple sized functions, permits high frequency applications, and provides optimum noise immunity. Mupac Corp, 64 Summer St, Brockton, MA 02402. Circle 230 on Inquiry Card

#### SOURCE AND MEASUREMENT **TEST MODULES**

This line of modules, suitable for testing ICs and logic assemblies, provides std testing functions to simplify design and building of fixtures for automatic test equipment. First 11 modules offered provide high speed and high power drivers, current-to-voltage converters, comparators, and I/O switches. 2 modules have 600-ps risetimes for driving high speed ECL circuits. The small, encapsulated units are 0.375" (1 cm) high, and 0.8 to 1.7" (2 to 4 cm) on a side. EH International, Inc, 515 Eleventh St, PO Box 1289, Oakland, CA 94604. Circle 231 on Inquiry Card

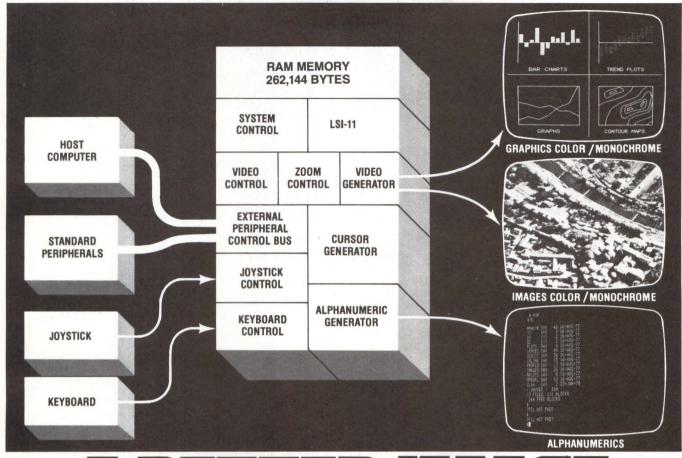
#### **ROTARY PORT SELECTOR**



Four separate data terminals can communicate through a single modem on a shared basis using the 7251 rotary port selector. The unit sequentially monitors the request-to-send lines from the four terminals. When such a signal is received from any terminal, the device automatically selects the appropriate port to connect that terminal to the modem. Panel lamps indicate the terminal in control; other lamps indicate modem carrier detect and clear-to-send. Tele-Dynamics/Ambac, 525 Virginia Dr. Fort Washington, PA 19034.

Circle 232 on Inquiry Card

## GIVE YOURSELF



A BETTER MAAGE

The VISACOM Visual Image and Computer System is a totally integrated Microcomputer and Display System... another in a series of innovative products from De Anza Systems, designed to enhance your image.

#### **FEATURES**

**Microcomputer** Digital Equipment Corporation LSI-11 microcomputer provides high speed capability and has an instruction set compatible with the PDP-11 series. The system provides a powerful stand-alone computer capability. **System Control** Provides the LSI-11 with virtual addressing capability. The entire 256K byte memory can be addressed. **RAM Memory** 256 K bytes of RAM memory are

**RAM Memory** 256 K bytes of RAM memory are organized to provide processing and image refresh. This organization greatly reduces

transfer times and increases interaction between the CPU and display image.

**Zoom** Allows a 64x64x16,

128x128x16 or 256x256x16 bit portion of the memory to fill the entire image window under hardware control.

**Video Generator** Provides four or eight bit digital to analog conversion and intensity transformation tables.

**Dual Cursor** Provides two individual cursors controlled by an external Joystick with multifunctions. **Alphanumeric Generator** Provides up to four separate 80 character by 25 line overlays.

**Software** An operating system is provided to handle memory management, and also provides facilities to interface I/O and user subroutines. Subroutines for high speed generation of vectors, conics and rectangles are also available.

#### **De Anza Systems Incorporated**

3444 De La Cruz Blvd. Santa Clara, CA 95050 (408) 988-2656

#### HYBRID CRYSTAL CLOCK **OSCILLATOR MODULE**

Series XO-33 uses precision crystals and hybrid techniques to provide frequency stability of ±0.005% for XO-33A; ±0.01% for XO-33B; ±0.05% for XO-33C; and  $\pm 0.1\%$  for XO-33D. Std op temp range is 0 to 70 °C, and storage temp range from -55 to 125 °C. Max seated height of the hermeticallysealed, low-profile ceramic package is 0.2" (0.5 cm). It is compatible with TTL loading and drives up to 10 TTL gates. Input power requirement: 5 Vdc at 30 mA typ (4 to 15.9 MHz) and 50 mA typ (16 to 25 MHz). Dale Electronics, Inc, Frequency Control Group, 930 W 23rd St, Tempe, AZ 85282. Circle 233 on Inquiry Card

#### MICROCOMPUTER-BASED PLOTTER CONTROLLER

Model 6300 may be combined with any of the company's plotters to configure a plotting workstation. Four integral microcomputers relieve the host CPU of much of the plotting-associated computation, and provide such features as operator preprogramming, communications option, and error correction. Distributed computing is enabled by the controller for arc and circle generation, any radius, any direction; dot/dash mode for lines and curves in user-defined patterns; built-in character-generator produces 214 different characters. Zeta Research, div of Nicolet Instrument Corp, 2300 Stanwell Dr, Concord, CA 94520. Circle 234 on Inquiry Card

#### COMPUTER POWER **DISTRIBUTION SYSTEM**



PowerMite MKII, designed specifically for smaller computer installations, ranges from 15- to 45-kVA capacity. Power distribution is either by plugging devices into receptacles at the rear of the system or via output circuit cable to remote system devices. Input voltages are 440/460/480 V, 3φ; 230/240 V, single or  $3\phi$ ; and 120/208 V, single or  $3\phi$ . Outputs are 120/208 V single or  $3\phi$  and 230 V  $3\phi$ . Unit is 35 x 22 x 33" (89 x 56 x 84 cm); approx weight is 375 lb (169 kg) for the 15-kVA, and 650 lb (293 kg) for the 45-kVA units. Computer Power Systems Corp, 3398 E 70th St, Long Beach, CA 90805. Circle 235 on Inquiry Card

#### SYNCHRO-TO-DC CONVERTER

Zero tracking error up to 1440 deg/s is provided by model 426 tracking s/dc converter, which has an accuracy of ±6 arc-min. There is a choice of 4 outputs: 0 to 5, 0 to 10, ±5, and ±10 Vdc. Unipolar outputs are for 0 to 360 deg rotation, bipolar for ±180 deg. Unit size is 2.6 x 3.1 x 0.82" (7 x 8 x 2.1 cm). Input impedance for low level inputs is >200 k $\Omega$ ; for high level inputs >1 M $\Omega$ . Power requirements are  $\pm 15$ Vdc at 100 mA max. Natel Engineering Co, Inc, 8954 Mason Ave, Canoga Park, CA 91306. Circle 236 on Inquiry Card

#### MEMORY RELAY FOR **CONTROL SYSTEMS**

Output of the MR series relay is an optically-isolated triac which turns an alternating current of 5 A max on or off to control an external load. The compact, octal-base, plug-in unit is fully protected against transients. An LED indicator shows when the relay is in a reset condition. Memory feature is maintained by an internal battery, activated only in event of power failure. The series is available with input voltages of 24, 48, 120, and 240 Vac at 1.2 VA. Master Electronic Controls, Box 25662, Los Angeles, CA 90025. Circle 237 on Inquiry Card

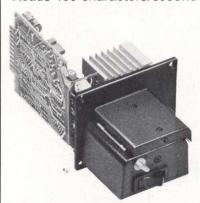
#### HANDHELD OCR READER



Series 600 OCR system features model 610 OCReader™, which can accurately read up to 130 char/s. Automatic line tracking (ALTTM) works with the reader's "eye" to minimize wobble, tilt, and skew errors. System operates over a wide range of voltages and frequencies; power requirement is under 25 W. A 10ft (3-m) retractable cable attached to the 3-oz (84-g) wand allows freedom of movement and system positioning. Series 600 works within the NRMA voluntary retail identification standard spec A. Caere Corp, 345 E Middlefield Rd, Mountain View, CA 94043. Circle 238 on Inquiry Card

#### 601 Reader

Stops on character Stepper motor Reads 150 characters/second





#### 612 Stand Alone Reader

Same features as 601 . . . plus . . . Parallel TTL Level or RS-232C or TTY configurations

#### 640 Data Loader

Low cost Reads 350 characters/second





416 Junipero Serra Drive San Gabriel, California 91776







Save engineering time and expense. Take advantage of Intermec's years of expertise. The Intermec Model 9200 is a completely designed bar code reader that's ready to integrate into your system. All the programming needed is on the card. Read the code of your choice; Code 39, Codabar, UPC or another popular bar code. The reliable RUBY WAND® Light Pen is included in the low, low price of under \$400 in OEM quantities.

Features you'll get include bidirectional scanning, ASCII code transmission, and RS-232-C interface with dual connectors for operation with other devices. Parallel data interface boards and custom communications protocol are available or can be developed to meet your exact requirements.

For more information, write or call: Interface Mechanisms, Inc. P.O. Box N Lynnwood, WA 98036 Phone (206) 743-7036

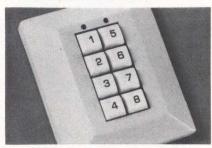
"See us at NCC, Booth 4413"

#### PRODUCTS

#### **DIGITAL ANGLE TO** SIN/COS CONVERTER

14-bit resolution, ±2 arc-min accuracy, continuous simultaneous sine and cosine outputs, and conversion time of 2 μs are offered by the model 1500 converter. Input is a digital natural, binarycoded angle representing 0 to 360 deg with 14-bit resolution. Digital outputs are 12-bit sine and 12-bit cosine coded angles; logic level "1" for minus and "0" for plus are the signs for each output. Size is 3 x 4 x 4" (7.6 x 10.2 x 10.2 cm). 0 to 70 °C, -55 to 85 °C, and MIL-883 modules are available. Transmagnetics, Inc, 210 Adams Blvd, Farmingdale, NY 11735. Circle 239 on Inquiry Card

#### **ELECTRONIC SECURITY DEVICE**



Keys and code cards are not needed with electronic keyboard that operates by a 4-digit code, with a 2-digit reset code. An incorrect code, or tampering, automatically locks up the device. Units can accept up to 10 different codes on the same keyboard. An LED indicator verifies code; another is provided for such functions as test or violation. Interchanging code blocks will change the code. The device operates on 6-24 V ac or dc, of any polarity and has dual-isolated 1-A contacts. SenDEC Corp, 54 West Ave, Fairport, NY 14450. Circle 240 on Inquiry Card

#### 2 and 3" HIGH LIQUID CRYSTAL DISPLAYS

Three models of a 2'' (5.1-cm) high char, and of a 3'' (7.6-cm) high char, are available in 7- or 16-segment or 5 x 7 dot matrix alphanumeric configurations. Displays available in reflective, transmissive, or transflective mode can be stacked or placed end-to-end for distance viewing. For night viewing, backlighting is possible. Colors available are black, white, yellow, blue, and red. One flashlight battery will power 1500 displays. Extended op temp range is -20 to 60 °C; an 80 °C model is available for special applications. Crystaloid Electronics Co, Box 628, Hudson, OH 44236.

Circle 241 on Inquiry Card

#### Canon

## Motor Tachs

for OFMs

#### ac or dc Outputs

Rated Voltages, 4.5 to 24 Vdc Starting Torque, 0.7 to 35 oz.-in. No Load Speed to 9400 rpm



#### Output

(Standard Models)

V/1000 rpm 1.2,2.4 or 7 Linearity 0.15%

ac

12 Hz per revolution 1.2, 2.0, 2.2 or 2.47 V, p-p

Canon Camera Quality in Electronic Components



Send for brochure containing installation and performance data

#### Canon U.S.A., Inc.

**Electronics Components Division** 10 Nevada Drive Lake Success, L.I., N.Y. 11040 516/488-6700/Telex No. 96-1333 Cable - Canon USA LAKS

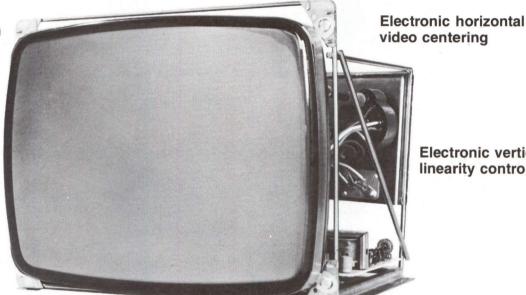
# The new features in this Ball high performance monitor will save you money tomorrow.

20 MHz bandwidth

100% silicon circuitry

Modular sync stripper board

converts to EIA composite input



Electronic vertical linearity control

Optional dynamic focus and skip-scan

#### The new low price will save you money today.

Ball's 2nd generation TTL-series monitors cost less to operate because of the way we build them - built for reliable service with long life and low maintenance requirements.

For example, we've added more electronic controls for faster set-up and service. Widened the bandwidth to 20 MHz for better performance. Expanded our simple subassembly interconnection idea for greater versatility. We've even reduced the size of our 12" model so it fits where no competitor can.

For video quality, our specially selected CRT gun and deflection assembly delivers the kind of bright, well detailed characters you demand in a high performance

#### Compare life cycle costs. You'll have a Ball.

If you've been waiting to upgrade to Ball quality, now's your chance. Not only are our new TTL-120 and 150 monitors fully interchangeable with our present TTL-12 and TTL-15 units, but drop-in models for other makes are available as well.

Give us a call and find out how Ball can lower your costs at a new low price.

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273

# Flicker-free and ultrahigh resolution color TV displays...

You can have your choice with the Model 374.

1024 x 512 pixel graphics displayed at a non-flicker, 60-Hz refresh rate. Ideal for the display of computer graphics.

#### or

1024 x 1024 ultrahigh resolution pixel graphics displayed at a 30-Hz rate using 2:1 interlace. Video bandwidth in excess of 30 MHz assures that resolution is not electronically limited.

Write or call Dick Holmes for a Model 374 descriptive brochure.





#### **Electronic Image Systems**Division of Systems Research Laboratories, Inc.

Division of Systems Research Laboratories, Inc. 2800 Indian Ripple Road ● Dayton, Ohio 45440 Phone 513/426-6000 ● TWX 810/450-8621

CIRCLE 161 ON INQUIRY CARD

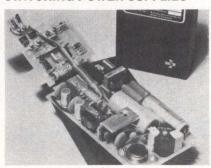
#### PRODUCTS

#### FIELD-PROGRAMMABLE MODEM

Field-programmable protocol, in the form of DIP switches, allows the 9113B 300-baud modem compatibility with Bell 103A to F, 113, 212A, and Vadic VA3467 and VA3437. Design also provides RS-232-C or 20-mA current loop interface. FCC-registered DAAs are built in. Among other DIP switch selectable options: transmit power level; space disconnect, call abort, and long space transmit durations; FDX or HDX operation; and loss of carrier disconnect. Omnitec Data, 2405 So 20th St, Phoenix, AZ 95034.

Circle 242 on Inquiry Card

#### LINE OF MINIATURE SWITCHING POWER SUPPLIES



Three 12-, 15-, and 24-V units are additions to the company's line of 5-V, 25-W MMG supplies. Efficiencies are from 75 to 85%. Units operate from 110/120 or 220/240 V ±10%, 50/60 Hz, 1.4 to 2.5 A. 4-kV rms insulation between input and output is provided by optical coupling. Operation is series or parallel without special interconnections. Switching output voltages are ±10% adjustable. Ripple is <10 mV rms or 50 mV pk-pk over a 30-MHz bandwidth. Overcurrent and overvoltage protection are std. Gould Inc, Electronic Components Div, 4601 N Arden Dr, El Monte, CA 91731.

Circle 243 on Inquiry Card

#### 90-DEG MONOCHROME CRT

Completing the company's line of 15" (38-cm) industrial and monitor display tubes, this 90-deg deflection alphanumeric CRT provides improved performance over the 110-deg version, and reduced weight and length advantages over the 70-deg tube. Overall length is 14.94" (38 cm). Tubes are available with integral mounting, implosion protection, and choice of phosphors. Screen sizes range from 5 to 22" (13 to 56 cm) measured diagonally. **GTE Sylvania**, 700 N Pratt St, Ottawa, OH 45875.

#### **FULL FUNCTION DATA LOGGER**



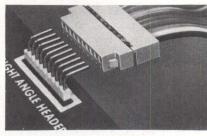
Datalogger 2000 measures up to four mixed parameters selected from the temperature, dc voltage, dc autoranging, ac voltage, true rms, and transmitter outputs. It offers skip-channel capability and provides up to 1200 individually assignable alarms, displays and records accurate time, Julian date, channel number, measured data, and parameter symbol. Data outputs include isolated BCD, isolated RS-232-C, or TTY compatible with selectable baud rates from 110 to 9600. United Systems Corp, 918 Woodley Rd, Dayton, OH 45403.

Circle 245 on Inquiry Card

#### IMAGE AND GRAPHICS DISPLAY SYSTEM

ID 1000 series image display system can store and display a 256- x 256-bit image array with 6, 8, or 12 bits/pixel in gray shades or color. Graphic modes and alphanumeric generator are included. System includes the interface to PDP-11 UNIBUS or LSI-11 Q-bus; other popular minicomputer interfaces are available. Options include intensity transformation units for monochrome and color applications, cursors, and joystick control. **DeAnza Systems**, 3444 De La Cruz, Santa Clara, CA 95050. Circle 246 on Inquiry Card

#### MASS TERMINATION RIBBON CABLE CONNECTOR



Cable-to-board ribbon cable may be mass terminated on 0.100" (0.25-cm) centers with insulation piercing Term-Apierce connectors. Available in straight-on or right angle version, they have double the current rating of available 0.050" (0.13-cm) products. They will pierce ribbon cable or discrete wires 10- through 28-contact positions, 22 through 26 AWG, and have as standard tin-plated brass contacts. Gold contacts are available. **Methode Electronics, Inc,** 1700 Hicks Rd, Rolling Meadows, IL 60008.

Circle 247 on Inquiry Card

Sure, I'd like to get five VERBATIM™ TC-1200 data cartridges and only pay for four!

Name:	Or Call Toll Free:
Title:	
Company:	(In Missouri call: 800-892-7655, ext. 515
Address:	
Phone: ()	160
City:State:Zip	Verbatim
Type of equipment we use:	500
Offer void where prohibited, expires June 15, 197 Mail to Information Terminals Corp., 323 Soquel Sunnyvale, CA 94086. 86-5-78	Way,

# IBM 5100 and Tektronix 4051 users: Let's talk!

At ITC we're working on some interesting ideas for your removable magnetic storage media. We know you'll want to keep informed. To make it easier for you to let us know where you are, we're giving you a first-ever (and limited time) 20% discount on a box of five quality VERBATIM TC-1200 data cartridges.

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TWX: (510) 697-0784

Central Region: Overland Park, KS (913) 642-2185, TWX: (910) 749-4045

Western Region: Sunnyvale, CA (408) 245-4400,

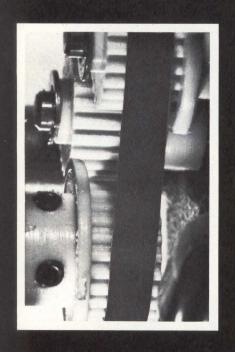
TWX: (910) 339-9381

Just let us know where you are!

Thanks.

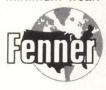
InformationTerminals Corp.

#### It's What's Inside **That** Counts



# "40 DP" TIMING BELTS

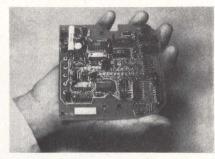
Recommended for light duty fractional horsepower applications Fenner "40 DP" timing belts offer the ultimate in synchronized engagement and precision performance. These belts have excellent flex as well as resistance to abrasion, ozone and oil. The slip-proof feature provides continuous accuracy and reduces strain on bearings as compared to flat belts or V-belts. Constant pulley gear contact insures smooth drive and



**FENNER AMERICA** 400 East Main St. Middletown, Conn. 06457 Tel: 203-346-7721

#### PRODUCTS

#### **COMPUTER TERMINAL DIALER**



Auto-Call single-number dialer provides dedicated services via a standard telephone set without the need of a leased line. Unit meets telco specs and does not affect data or voice transmission. PBX compatible, it has a 16-digit programmable memory for storing numbers and allows user to program extra digits. Unit automatically dials the computer center when handset is lifted, or, in manual mode, by pushing a button. Touch-Tone<sup>R</sup> or rotary models are available. Dialer draws its power directly from the telephone line. Alsyc Telecommunication Systems, 1140-F N Kraemer Blvd, Anaheim, CA 92806. Circle 248 on Inquiry Card

#### **OPEN FRAME POWER SUPPLIES**

56 models in 6 package sizes, with single, dual, and triple outputs up to 28 Vdc and currents up to 25 A, comprise the LO series. Features include foldback current limiting and no overshoot on turn-on, turn-off, or power failure. Tempco is 0.03%; all models are convection cooled. Amb op temp range is 0 to 60 °C; storage temp is -20 to 85 °C. Tracking accuracy on dual- and triple-output models is 2% abs voltage difference, with an 0.2% change for all conditions of line, load, and temp. Lambda Electronics, 515 Broad Hollow Rd, Melville, NY 11746. Circle 249 on Inquiry Card

#### **SERIES-COMPATIBLE DOT-MATRIX PRINTER**

Three printing modes, quickly-replaceable cartridge ribbon, auto underlining, and bidirectional printing are among the features of HP2631, first in a family of 180-char/s dot-matrix serial printers. It is fully compatible with HP 9825, 9830, 9831, and 9800 system 45 desktop computers. The unit also includes silicon-on-sapphire microprocessor. With the appropriate interface the printer may be used with installed HP desktop computers. Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. Circle 250 on Inquiry Card

#### SUBMINIATURE **TOGGLE SWITCHES**

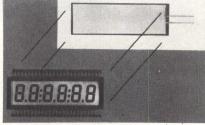
Three contact rating options are offered in this addition to the 753 series switches: low level, 0.4 VA at 20 V, ac or dc; standard, 5 A at 120 Vac or 28 Vdc, or 2 A at 250 Vac; and low level/standard combination. Switches have terminals bent 90 deg, so that the mounted toggle is actuated in a plane perpendicular to the board. Series includes spdt and dpdt units, and 9 combinations of momentary or alternate "on" or "off" functions. Dialight, 203 Harrison Pl, Brooklyn, NY 11237. Circle 251 on Inquiry Card

#### FIBER-OPTIC VIDEO LINKS



Fibercom<sup>TM</sup> wide band analog links use single-fiber guided lightwave for 10to 20-MHz operation at distances from several meters to >1 km. Min S/N ratio is 50 dB at 1-V pk-pk input; flatness, ±1 dB; linearity >1%, pulse overshoot <5%; temp stability, ±0.5%/°C; 50- or 75-Ω impedance; and single supply operation. RFI-tight aluminum enclosures, 15.9 x 5.1 x 10.1 cm in size, house transmitters and receivers. 115-Vac, 40to 400-Hz operated models are std. Radiation Devices Co, Inc, 10026 York Rd, Cockeysville, MD 21030. Circle 252 on Inquiry Card

#### LIQUID CRYSTAL DISPLAY **BACKLIGHT PANEL**



Filaments, sockets, and fragile subassemblies are eliminated in Capsul LCD lamps by providing an integrated, thin, sealed-profile electroluminescent panel, sized to fit directly behind the LCD. Low ac power is converted to a uniform glow over the entire phosphorcoated lamp surface. Varying either frequency or voltage regulates the brightness. Pretinned IC-type leads and pressure-sensitive adhesive on the front surface facilitate assembly. A choice of highly visible colors is available. Atkins & Merrill, Inc, Electro-Products Div, Etna Rd, Lebanon, NH 03766.

Circle 253 on Inquiry Card

#### LOADED WITH EXTRAS AT NO EXTRA COST

- Microprocessor controller
- Serial RS232C interface
- Parallel TTL level interface
- Full upper and lower case ASCII character set (96 characters)
- Full 81/2 inch wide paper
- Line length of 80 columns at 10 characters per inch
- Impact printing
- 7x7dot matrix
- Ordinary paper roll, fanfold, or sheet
- Serial baud rate to 1200 bits per second
- Multiple line buffer of 256 characters
- · Built-in self test mode
- Instantaneous print rate to 100 characters per second
- Sustained throughput to 50 characters per second
- Multiple copies without adjustment
- Reinking ribbon mechanism
- Expected ribbon life of 10 million characters
- Front panel operator controls
- Attractive table top console

# Check the impressive features on Integral's new IP-125 Impact Printer only \$799

Complete, ready-to-operate...
the first impact printer to offer
big printer performance at a
mini-printer cost.

Write for complete information or call (617) 926-1011



## Integral Data Systems

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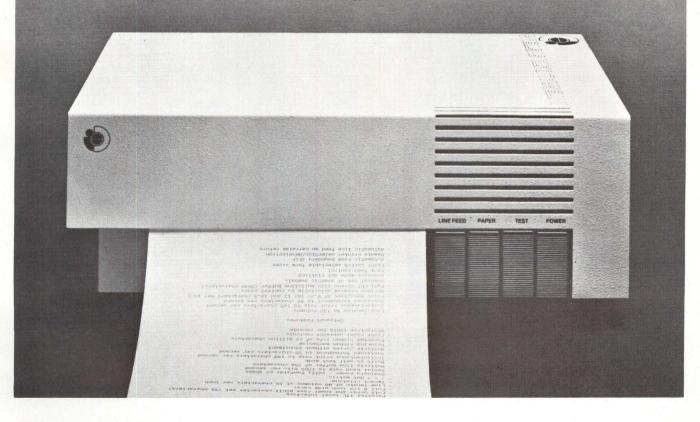
#### ... AND FOR VERY LITTLE MORE

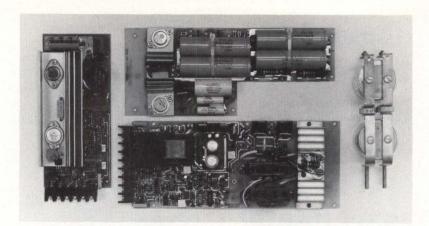
- · Line lengths to 132 columns
- Instantaneous print rate to 165 characters per second
- Sustained throughput to 80 characters per second
- Print densities of 8.3, 10, 12 and 16.5 characters per inch
- Options program selectable by control codes
- Full CRT screen size multiline buffer (2048 characters)
- Special set of graphic symbols
- · Graphics mode dot plotting
- Form feed control
- Eight switch selectable form sizes
- Automatic page boundary skip
- Remote printer selection/ deselection
- Automatic line feed on carriage return

IP-225

#### "The Tractor Impact"

the pin feed version of the IP-125 with tractor drive forms control plus all the standard features of the IP-125.





#### **SWITCH OUR SWITCHERS TO** SUIT YOURSEL

Maybe one of our 56 standard products won't fit your application. No problem. Because our modular design means you can switch components to suit your requirements. 375 to 750 watts.

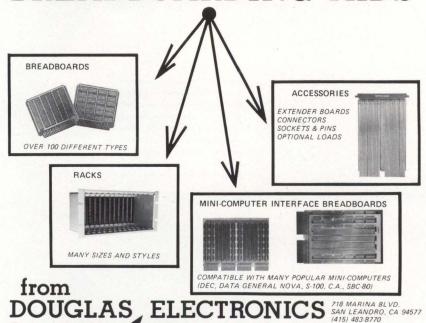
Single, dual, triple or quad output. 5, 12, 15, 18, 24 and 28 Vdc currents from 2 to 150 amperes. Put our ruggedized construction to the test. Call us.

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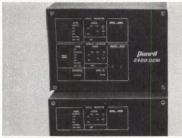


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#### PRODUCTS

#### **MODEM WITH NETWORK** DIAGNOSTICS



Features of the 2400 DCM diagnostic controlled, 2400-bit/s synchronous modem allow it to function as a controller for the entire data network. Diagnostics, integral with master and remote modems, provide test and control of the remote units over a secondary channel without interfering with mainstream transmission. LSI logic, built-in test pattern generator and detector, RS-232-C interface, and compatibility with Bell 201B and 201C data sets are included. Penril Corp, 5520 Randolph Rd, Rockville, MD 20852.

Circle 254 on Inquiry Card

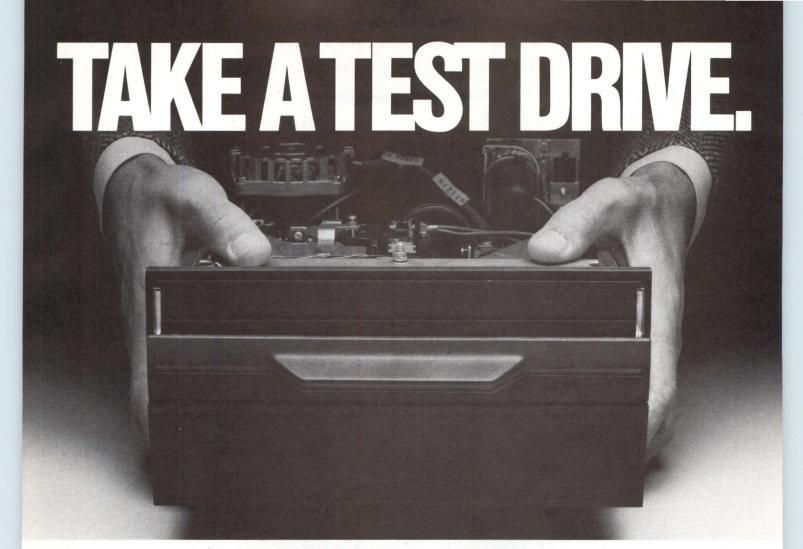
#### OSCILLOSCOPE ADAPTER

Single-trace scopes can be converted into 4-trace units by the Four Tracer. Front panel binding posts provide 4 inputs, each equivalent to a single TTL load in parallel with a 6.8-kΩ pull-up resistor. Gain and positioning are internally fixed. Unit's output feeds composite waveform of the 4 input signals to the scope's vertical input; 100-ns pulses are easily viewed on a scope of sufficient bandwidth. Display is in either chopped or alternate mode. Weight is 1 lb 9 oz (0.7 kg); dimensions, 2.625 x 4 x 7.25" (6.7 x 10.2 x 18.4 cm). Nittany Digital Devices, Box 56(N), Pennsylvania Furnace, PA 16865. Circle 255 on Inquiry Card

#### SINGLE-SIDED **WIREWRAP BOARDS**

A family of single-sided, IC-pluggable wirewrap boards is now available in metric dimensions. Single sizes (series SMP64) and double sizes (DMP64) are included in the line. Design has wirewrapping terminals on the component side; boards can be spaced interchangeably with standard PCB rack assemblies. SMP64 accommodates 20 16position ICs, while the DMP64 will accept 55. Boards are supplied with either discrete 16-position molded sockets, or 16-position patterns of individual socket/terminals. Garry Manufacturing Co, 1010 Jersey Ave, New Brunswick, NJ 08902.

Circle 256 on Inquiry Card



Introducing the Memorex 552 Dual-Head Flexible Disc Drive—and a great way to find out just how great it is:

Just give us a call and we'll loan you one of our new 552's. So you can test it in your systems, under the conditions important to you. So you can confirm for yourself the 552's 1600 kilobyte capacity, 3 msec access time, and high reliability. So you can see for yourself the benefits of all the features Memorex builds in for better performance, greater versatility, operating ease, and reduced cost of lifetime ownership.

If a dual-head drive is more than you need; our 550 single-head, double density drive may be just the one you need. All the features you've come to expect as industry standard, plus some others that are setting new standards. Like the fastest access time of any single-head drive. And fast conversion of our 550 to dual-head, because of the near total parts commonality with our 552. Unique features that make the 550 a uniquely-effective performer. Take one of our test units and you'll see just how well the 550 performs.

To get your evaluation unit, just call the Memorex office nearest you, or write us at General Systems Group (OEM Division), San Tomas at Central Expressway, Santa Clara, CA 95052.

We'd be pleased to have you test our drives, because we're confident you'll be pleased with the results.

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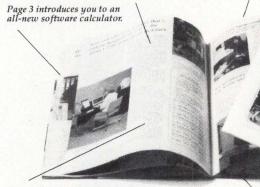
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#### PRODUCTS

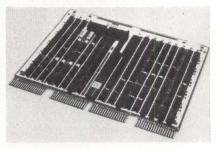
#### **PROGRAMMABLE ROTARY ENCODED LOGIC SWITCH**

Subminiature P/Rel switch is fully programmable up to 40 detent positions with 6 lines of information. A miniature PC disc on a silver plate copper laminate PCB provides full programming to the truth table and uses any code. A single disc can directly drive LED displays. The switch is 1.25" W x 1.125" H (3.2 x 2.9 cm). Design of the unit resists contact contamination and provides positive indexing and longer life. Contact life is 50k cycles of 720 deg min or 100k cycles of 360 deg min. Standard Grigsby, 920 Rathbone Ave, Aurora, IL 60507. Circle 257 on Inquiry Card

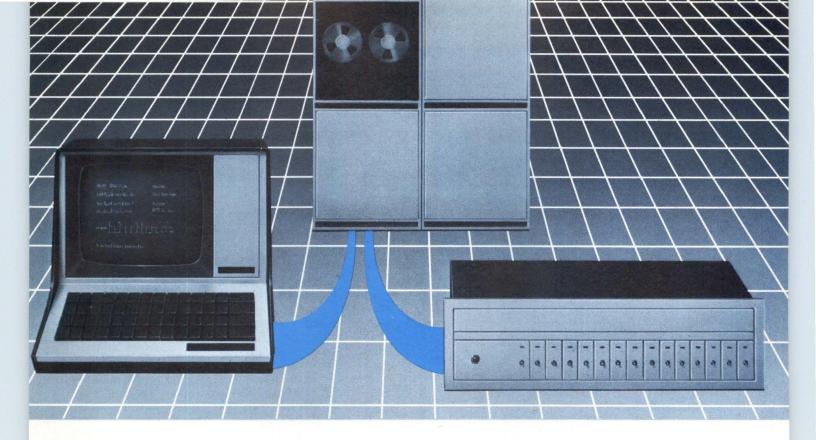
#### **OPEN FRAME** SWITCHING POWER SUPPLIES

Ratings of 5 V at 20 A (5C5), 5 V at 35 A (5E5), and 5 V at 65 A (5G5) for this line of switching OEM units are claimed to provide more output current than any other such available supply. A substantial 0.125 x 0.187" (0.3 x 0.5cm) frame is suitable for mounting on 4 sides. Features include input LC filtering, integral OVP, logic inhibit, reduced component count, single PCB construction, 100% 24-h burn-in, and std 2-yr warranty. Alpha Power, Inc, 20536 Plummer St, Chatsworth, CA 91311. Circle 258 on Inquiry Card

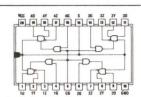
#### CARTRIDGE DISC CONTROLLER BOARD



Users of the PDP-11/03/11V03 and other LSI-11 based systems can couple from 2.4M to 80M bytes storage with the Dilog-1 single-board controller. Software transparent with DEC RK11 disc systems, the controller operates under RT-11 and RSX-11 OS. Design incorporates microprocessor which enables automatic self-test. Controllers are supplied either singly or as complete disc subsystems, and come with diagnostic software and instruction manual. Distributed Logic Corp, 12800 G Garden Grove Blvd, Garden Grove, CA 92643. Circle 259 on Inquiry Card

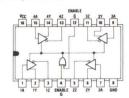


#### Four more new line circuits. Meet EIA Standard RS-422. From the leader. Texas Instruments.



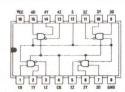
#### SN75151 Quad differential line driver with 3-state outputs.

- 40mA sink and source capability.
- · Common strobe and enable.
- Individual enable control for each driver.
- · Very low power dissipation in disabled state.
- Low output skew



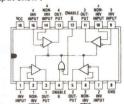
#### AM26LS31 Quad differential line driver with 3-state outputs.

- High output impedance in power-off conditions.
- · Complementary enable inputs.
- TTL/DTL compatible.
- · Low output skew.



#### SN75153 Quad differential line driver with 3-state outputs.

- 40mA sink and source capability.
- Common strobe and enable.
- Very low power dissipation in disabled state.
- · Low input current to minimize loading.
- Low output skew



#### AM26LS32 Quad differential line receiver with 3-state outputs.

- · Complementary enable inputs.
- Built-in input threshold hysteresis.
- Meets EIA Std. 422 and 423, Fed. Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

Two innovative quad differential line drivers. Two second source circuits, one quad differential line driver and one quad line receiver.

All are designed to meet EIA and federal interface standards to ensure balanced voltage for the interchange of serial binary signals between data terminal and data communications equipment. Or any interface of binary signals between voice and data equipment.

Each offers 3-state outputs and low power Schottky circuitry to reduce power consumption without sacrificing speed. They all operate from a 5 V power supply.

In addition to these new line circuits, TI offers the SN55/75158 and SN75159 dual differential line drivers that meet EIA RS-422.

For more information on your most complete source of linear and interface circuits, write Texas Instruments, P.O. Box 5012, M/S 308, Dallas, Tx. 75222.

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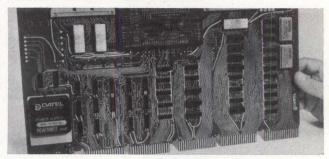


**CIRCLE 170 ON INQUIRY CARD** 



#### PRODUCTS

#### 64-CHANNEL, A-D/D-A INTERFACE/PERIPHERAL BOARD



SineTrac ST-PDP is a complete data acquisition peripheral built on a single DEC BB-11 connector block which loads directly inside PDP-11 minicomputers. It uses 5-V power from the computer backplane and generates its own  $\pm 15$  V for analog circuits using an onboard dc-dc converter. 64 single-ended or 32 differential input channels are accepted and digitized to 12-bit binary data words. The unit is expandable to 256 channels. Data samples are then placed on the UNIBUS by assembly language program instructions on diagnostic tape. Input voltages of -10 to 10 V and other high level ranges may be accepted. A-D conversion speed is 20  $\mu s$ . Effective channel throughput rates of 45k samples/s are possible using optional DMA logic. Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021.

#### **AUTOMATED SEMICONDUCTOR TEST SYSTEM**

The S-3280 provides fully automated testing of ECL LSI devices (up to 64 pins) and other current mode logic devices. Pulse risetime for pin drivers is  $\leq 1$  ns for a 2-V swing and a 50- $\Omega$  load. Positions of drive pulse leading and trailing edges can be set under program control in 100-ps increments; timing skew can be adjusted to <100 ps between any 2 pins on the DUT. Sampling head and programmable circuitry capable of controlling drive pulse amplitude, width, and delay are provided for each pin. Single-shot or sampling test modes can be employed for outputs. A 50- $\Omega$  impedance is established at all I/O pins; the 50- $\Omega$  interface extends up to the fingers of a wafer probe. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 261 on Inquiry Card

#### HIGH PERFORMANCE SIGNAL CONDITIONER

Line-powered, single-channel SigCon 701D translates 2-terminal variable resistance signals of a Metritape level, or combined Level/Temp, sensor into a stable analog level or temp signal. Sensor input resistance range may be 0 to 100 up to 3500  $\Omega$ , which accommodates tanks from 3 to 115 ft (0.9 to 35 m) high containing liquids, slurries, or dry granular solids. Packaged in an oil-tight 6 x 6 x 4" (15- x 15- x 10-cm) NEMA-12 box, the device generates such std process outputs as 1 to 5, 4 to 20, and 10 to 50 mA, and voltages of 1 to 5, 0 to 4, and 0 to 10 Vdc for a computer or data logger. Auxiliary zero-based current output, 0 to 1 mA or 0 to 100  $\mu$ A, drives a remotely located analog or digital meter, recorder, or computer. **Metritape, Inc,** 33 Bradford St, Concord, MA 01742.

Circle 262 on Inquiry Card

You tell us what your data collection requirements are. We've added more data collection building blocks to satisfy them.

RS232 1/0





EPIC DATA's Model 1647 data collection terminals and Model 1648 system control units (SCUs), let you configure exactly the data collection system you need. These "building blocks," based on microprocessor architecture and modularity, provide you with simple, practical and flexible terminals or systems for virtually any combination of requirements you may have.

Simple. Building blocks can be combined to enable collection of information from a wide variety of pre-prepared and variable data with resulting improved efficiency and reduced errors. No computer knowledge is required for operation. Terminals can be programmed to: provide customized input, output and processing of data; prompt the user through entry steps and validating of data; and enable off-line or on-line operation.

EPIC DATA terminals are rugged, compact and lightweight. They can be wall-mounted or placed on a desk and are easily exchanged during maintenance.

**Practical.** Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in an impressive MTBF.

**flexible.** EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Terminals can be configured to scan bar codes and magnetic stripes or accommodate other peripherals through RS232 ports. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. Serial asynchronous or synchronous communications ports with either RS232 or line driver I/O and a low speed modem may be added. Parallel communications ports are also available. Both PROM and RAM memories are expandable.

Newest Building Block: More to Come in Next Few Months

A self-contained cassette tape recorder providing up to 2.88 megabits of storage for transaction logging or store-and-forward applications is now available. The modular reel-drive tape recorder, like the rest of the building blocks, features high reliability and ease of maintenance. There is no pinch-roller or capstan to wear tape; only the head touches the tape.



SCUs. Model 1648 SCUs can be configured to poll up to 100 terminals, assemble transactions, format data, append time and date, and store or forward collected data to the host.

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The Datec 30 Originate Only and the Datec 32 Originate/Answer acoustic couplers provide reliable Bell System 103/113 compatible Duplex or Half-Duplex, 300 bps data communication over conventional telephones.

Datec acoustic couplers are the only couplers on the market with CRYSTAL CONTROL for both the receiver and the transmitter.

The Datec 30 and Datec 32 acoustic couplers connect, time and time again.



P. O. Box 839 Chapel Hill, North Carolina 27514 phone: (919) 967-5605

#### **CIRCLE 173 ON INQUIRY CARD**



#### PRODUCTS

#### 300-LINE/MIN FORMS ACCESS PRINTER

Anything from a single label to a multipart invoice, on forms ranging from 4.25 to 8.5" (10.8 to 21.6 cm) wide, and 2.5 to 22" (6.4 to 56 cm) long, can be printed by the model 40 at 300 line/min. A specially-designed tractor-feed mechanism



provides instant access to tickets, receipts, or reservation forms printed on a demand basis. There are three available interfaces: the company's std serial interface for communication between controllers and devices of the model 40 product line; a

parallel interface, which requires a conversion kit; and simplified EIA, for printer control and synchronous data input, with a provision for RNC (Request Next Character). It provides char at a time data transfer, uses available EIA hardware, and provides internal clocking for 150, 300, 600, 1200, 2400, 4800, and 9600 bits/s. **Teletype Corp**, 5555 Touhy Ave, Skokie, IL 60076.

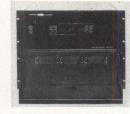
Circle 263 on Inquiry Card

#### **8-CHANNEL ANALOG OUTPUT SYSTEM BOARD**

Plugging directly into the backplane of Computer Automation's LSI 2, 3, and 4 minicomputers, the DT1735 fits one std half slot of the card cage, requiring no additional components or interfacing to form a complete 8-channel analog output system for computerized control and readout applications. The board has 8 completely independent D-A converter channels. Each converter is fully buffered to avoid intermediate outputs. All channels are powered directly from the minicomputer 5-V power through a highly regulated low noise dc-dc converter. 4- to 20-ms current loop outputs are optional for all channels. Resolution is 12-bit and accuracy is  $\pm 0.012\%$  FSR. Differential linearity is  $\pm 1/2$  LSB; gain and offset are adjustable to 0 for each channel; and settling time is 3  $\mu s$  to 0.01% FSR. Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760.

Circle 264 on Inquiry Card

#### MATRIX SWITCHING SYSTEM FOR ATE



Microprocessor-based model 3570 offers a convenient means of controlling signals and power to a unit under test (UUT) in an IEEE-488 configured automatic test equipment (ATE) system. It comprises 2 units—3571A control, and 3573A matrix switching. Control unit contains system control functions and

power: microprocessor, memory, IEEE bus, and RS-232-C bus interfaces, and matrix switch power. Modularly-designed switching unit comes std with 1 16 x 64 switching matrix module, and is expandable. Switching of signals up to 10 MHz is provided. Signal transmission quality similar to coax switching networks is achieved by 5-wire transmission line design. Std software includes assigning labels to control relay closure paths, and error messages. System measures 35.6 cm high x 48.3 cm wide. Systron-Donner Corp, Data Products Div, 935 Detroit Ave, Concord, CA 94518.

Circle 265 on Inquiry Card



If you feel like your fixed head disk is taking you for a ride when it comes to reliability, throughput and maintenance costs... it's time to get off the merry-go-round.

The BUSCOMM® DS-11 Disk Emulator is the new diskreplacement core memory that can eliminate all the ups and downs of your DEC Fixed Head Disk. With no moving parts, this economical system gives you rapid access and greater reliability with no fear of data loss if the power fails.

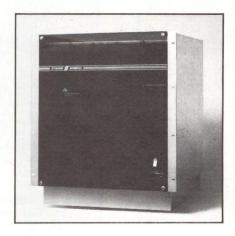
The chassis can hold eight memory modules providing a maximum storage capacity of 1 million words (2 Mega-

Bytes). The memory unit interfaces to the processor system with the DEC UNIBUS interface, and is completely software transparent to all DEC operating systems and diagnostics which support RF-11/RS-11 disk systems.

Other features include on-line/off-line switch, built-in self-test, selectable transfer rates to 1 million words per second, selectable block transfer mode, and complete user assignable configuration controls to minimize downtime.

So, give us a ring...and we'll give you the full technical details. (714) 540-3605.

# Replace Your DEC Fixed Head Disk With The DS-11 Disk Emulator



#### Standard Memories

has grown into a new name



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The Memory Man toll free: (800) 854-3792, (in California) (800)

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VT55 DECscope	2,695	260	135	
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ADDS Regent 100	1,325	126	67	
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#### **CIRCLE 176 ON INQUIRY CARD**

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Explore the possibility of joining our team of skilled professionals in the expanding Computer Aided Manufacturing area developing advanced systems and technology by sending your resume to:

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#### PRODUCTS

#### **DATA ENCRYPTION CIRCUIT CARD**

Second in a series of products implementing the Federal Data Encryption Standard (DES) Algorithm chip, the CR-300 circuit card can be incorporated in data terminals to prevent theft or misuse of computer data by providing a high level of communications security. Card connects to an 8-bit data bus, typically an 8080, 6800, or 6500, for data I/O and cryptovariable loading. DIP switch on the card selects control lines; data are loaded and unloaded in 8-bit bytes to and from card-mounted buffers. Operation is in 2 modes: block, which processes 64 bits at a time and is self-synchronizing; and cipher feedback, which processes 8 bits at a time and requires an initial vector for synchronization. Up to 32 cryptovariables may be stored and addressed in either encrypted or clear form in the in-card RAM. Rockwell International, Collins Telecommunications Products Div, Cedar Rapids, IA 52406.

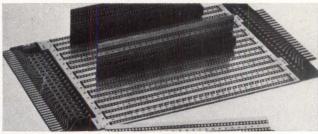
Circle 266 on Inquiry Card

#### SERIAL DATA TRANSLATOR

This device, model ST-1, allows the user to change peripherals without the need to modify software written for peripherals using different codes. It communicates via 2 RS-232-C serial ports at rates up to 19.2k baud, and is compatible with any host computer. Std translations include ASCII/EBCDIC/Baudot, and translation of terminal control codes has been implemented, with other translations either available, or user-programmable in Intel MCS-48 compatible machine language. Specs include: 8035 microprocessor; 512byte EPROM; 64-bytes RAM integral to processor; parallel to serial conversion via 2 COM-2502 UARTs; and clock, selectable between external or internal crystal-controlled oscillator. Integral power supply provides 5 V at 300 mA max and -12 V at 100 mA max. Input power is 110 to 130 Vac, 60 Hz, 10 W max. Sigma Data Systems, 715 Torreya Ct, Palo Alto, CA 94303.

Circle 267 on Inquiry Card

#### MODULAR HIGH DENSITY INTERCONNECT SYSTEM

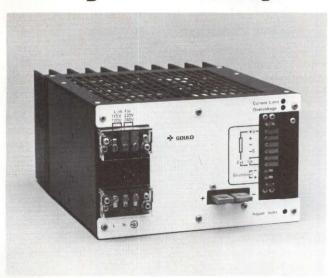


Modcon series is designed for board-to-board interconnect applications. It uses box-form contacts that mate with conventional 0.025 x 0.025" (0.06- x 0.06-cm) wiring posts on 0.100" (0.25-cm) center-to-center spacing. Contacts are spring-tempered phosphor bronze, featuring dual cantilever beams, and housed in high-temp glass-filled insulator. First of the line being produced is the 2505 series, available in double-row pin configurations of 10, 20, 40, 60, 80, and 100. Next to be available is the 2506 series, with single rows of 5, 10, 20, 30, 40, and 50. Other pin configurations are available on special order. Op temp range is -55 to  $150\ ^{\circ}\text{C}.$  Operating voltage, 800 Vdc at sea level; insulation resistance, 5000 M $\Omega$  min, at 500 Vdc; max current rating, 3 A; and contact resistance 10 m $\Omega$  at 3 A. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.

Circle 268 on Inquiry Card

# The big switch

# ...is to full cycle holdup.



The 500 watt MG5-100: 28 millisecond holdup.

Switching power supplies offer substantial holdup. Linears don't.

A Gould switcher will give you full regulated output at -20% line. Or during complete loss of power you'll get full output power for more than a missing line cycle.

Switchers offer other benefits too. They're 1/3 the size and 1/4 the weight of linears.

And they save energy with efficiencies of up to 85%.

Gould offers single and multiple output switchers with power levels from 8 to 2,250 watts. Custom designs can be provided to meet your exact specifications. You'll be backed by a high volume production capability and worldwide service network that only a \$1.6 billion company like Gould could offer.

For more information or to arrange for an evaluation unit, contact Gould Inc., Electronic Components Division, 4601 N. Arden Drive, El Monte, CA 91731. Phone (213) 442-7755.

#### Gould.

The power in switching power supplies.





CIRCLE 179 ON INQUIRY CARD



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### ... THE BEST FOR MODERN DATA PROCESSING EQUIPMENT

PAPER TAPE — 7 Colors plus Black Opaque; Printed Top/Arrow; Oiled and Unoiled Rolls: FOLD-ED TAPES — For specialized applications.

THERMAL PAPER — Rolls and Folded. Marginally punched and cross perforated for all types of printers and calculators.

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**FOLDED LISTER PAPERS** — For Digital Print-out Units.

**TELETYPE ROLLS:** Single copy; Multi-copy Carbon inter-leaved and Carbonless Friction Feed Sprocket feed.

CONTINUOUS TELETYPE FORMS:  $8\frac{1}{2}$ " x 11" Carbon inter-leaved 1 through 6 part; Carbonless 1 through 6 part (NCR).

EASTERN SPECIALTIES COMPANY, INC.

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P. O. Box 350, Holyoke, Ma. 01040, Tel: 413 533-7103

#### PRODUCTS

#### HDX/FDX MODEM WITH ALL-CMOS CIRCUITRY



Interface with both data communications terminals and multiplexers, and asynchronous data transmission over leased lines are permitted by AM-202, a Bell-compatible half/full duplex modem with all-CMOS circuitry and integral diagnostics. Data rates are 0-1200 baud over unconditioned lines and to 1800 baud on C-2 conditioned lines. Unit's diagnostics include LED status indicators and digital and analog loopback switches. Remote digital loopback feature allows complete end-to-end network evaluation. RTS/CTS delay is 8  $\pm$ 0.3 ms; Carrier Detect On, 6.19  $\pm$ 0.4 ms; and Carrier Detect Off, 5 ±0.5 ms. Other specs include FSK modulation with mark-space frequencies of 1300 and 2100 Hz, respectively; weight, 0.45 kg; dimensions, 5.1 x 10.2 x 19.1 cm. A card version of the modem is also available. Prentice Corp. 795 San Antonio Rd. Palo Alto, CA 94303. Circle 269 on Inquiry Card

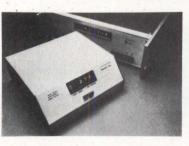
#### IMBEDDED DISC DRIVE CONTROLLER FOR PDP-11

Modular storage from 2.5M to 20M bytes/drive is provided by the DFC-803 controller for DEC PDP-11 UNIBUS™ computers. It is compatible with DEC operating systems, media, and RK11/RK05F diagnostics. Comprised of 2 hex boards, the unit operates with such disc drives as Diablo's model 31 and 44, Pertec's 3000 family, and CDC's Hawk and Falcon. It is compatible with either front or top loading models. Other features are 16-word data buffer allowing max DMA latency, transfer of up to 65k words in a single operation, and switch selectable platter zero. Fast positioning disc drives and 2400 r/min increase system throughput. Complete system consisting of controller, drive, and cables also is available. **Aviv Corp**, 300 Sweetwater Ave, Bedford, MA 01730.

Circle 270 on Inquiry Card

#### **AUTOMATIC CABLE/CIRCUIT TESTERS**

Wires or circuits can be sequentially identified during cable/ circuit assembly fabrication by series 3000 all-solid-state high speed, 118-circuit (236-point) capacity tester. Capacity is expandable in 118-circuit increments. Sensitivity ranges



from 2 to 100  $\Omega$ . Readout rates are up to 2000 circuits/s. For production, there is a wire finder and wire number mode, and for test inspection, shorts, opens, and miswires. LED display shows test results, identifier, and type of fault. Foot switch pro-

vides hands-off operation. Power input is 115 Vac, 60 Hz, 50 W; 220/230 Vac, 50 Hz optional. Series 4000 is for high production flat cable and similar cable/connector assemblies. Fully automatic, it has 60 to 102 circuit capacity, and computes type of fault or test complete at a rate of 500 circuit tests/s. **Glenair, Inc,** 1211 Air Way, Glendale, CA 91201. Circle 271 on Inquiry Card

N.C.C. Convention in Anaheim



## Twenty minicomputer makers are testing the 6250 bpi capability of the STC 1900...

What about the high-performance capability of your minis?

Can you offer your customers the high performance read-write capability of the GCR format?

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Can you remain competitive without a 6250 bpi tape subsystem for your minicomputer?

You can, with the STC 1900 high density magnetic tape subsystem. It includes 1600 and 6250 bpi as a standard feature, so you have library interchangeability with other systems operating at these densities.



and they're buying it.

You can offer the storage capability formerly available only with big mainframes.

Computer output microfilm (COM), and seismic exploration equipment makers have tested and approved the 1900. Minicomputer manufacturers have tested the 1900 and found it fits their needs for a rack mountable high density tape subsystem.

You can afford this high density subsystem because it's designed specifically for the OEM market by the world leader in high density tape subsystems.

To arrange for an evaluation, call Ron Brown direct, toll free. 800-525-2940.



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**CIRCLE 182 ON INQUIRY CARD** 



#### PRODUCTS

#### HIGH SPEED MODEM FOR DIGITAL **SWITCHING SYSTEM**

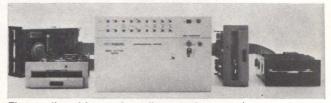
Integrated self-test diagnostic functions, speed, and modularity are among the features of the M437-2 modem, designed to be an integral component of the company's M3200 Pacuit<sup>®</sup> network switching and management system. It comes in 2 configurations: rack-mounted, and as the M681, a standalone add-on for currently operating M3200s. Operation is at 9600 bits/s, synchronous, on unconditioned voicegrade 3002 lines, an economic benefit by eliminating tariffs on conditioned lines. Diagnostic function enables performance of fault isolation procedures via operator-initiated computer commands to activate local and remote loopbacks. Modular design allows up to five modems to be installed in M3200 series cabinets. M681 standalone unit comes with one M437-2 as std equipment. Modem will operate at 9600 or 4800 bits/s, selectable, with FDX synchronous binary serial data transmission. Computer Transmission Corp, 2352 Utah Ave, El Segundo, CA 90245. Circle 272 on Inquiry Card

#### MULTIPORT LARGE SEMICONDUCTOR MEMORY

18M words x 16 bits RAM, and interfaces with 4 independent external CPUs are features of the SEMS-17 memory system. It contains 56 memory cards, each with 32k- x 16-bit storage capability; 6 interface cards; 4 control cards; and 4 error detection/correction cards. Control card monitors system performance and relays fault information to the primary computer. With an error detection/correction card, it also handles single bit error correction and multiple error detection. Use of the company's low power 4k static, full temp range memory chips results in 700-W max dissipation while maintaining 1 ms/word data rate. Organization is in a 4 x 13 array of 32k x 18 memories in front access rack 72 x 15.5 x 19.5" (183 x 39 x 50 cm). System is shockmounted to ensure compliance with MIL-S-901. Electronic Memories and Magnetics, Severe Environment Products Div, 20630 Plummer St, Chatsworth, CA 91311.

Circle 273 on Inquiry Card

#### **MULTIPLE FORMAT TESTER FOR FLOPPY DISC SYSTEMS**



Floppy disc drive and media manufacturers, system houses, and large end-users can use the programmable 70T-300 test system in engineering evaluation, production testing, and incoming inspection. It operates with either singleor double-density floppies, and with either single- or doublesided units. Being programmable, the format can be IBMcompatible, or any other industry-std or non-std format can be used. Complete test program includes routines for read/ write maintenance, error testing, variable step rate, and window margining for bit shift. Diagnostics are presented in ready-to-use sequence. Test program is prerecorded on ready-to-load floppy disc. Two models, 70T-300-2 for testing up to 2 drives, and 70T-300-4 for up to 4, are available. Applied Data Communications, Inc, 1509 E McFadden Ave, Santa Ana, CA 92705.

Circle 274 on Inquiry Card

# A new breed of printer/plotters...

So uniquely different in concept and design that no other medium speed printer can compare on a cost/performance basis.

ABCDEFGHIJKLMNOPGRSTUVWXYZI BCDEFGHIJKLMNOPGRSTUVWXYZI CDEFGHIJKLMNOPGRSTUVWXYZ[\ DEFGHIJKLMNOP@RSTUVWXYZ[\] EFGHIJKLMNOPGRSTUVWXYZ[\]^ FGHIJKLMNOPQRSTUVWXYZ[\]^\_ GHIJKLMNOPGRSTUVWXYZ[\]^\_ GHIJKLMNOPGRSTUVWXYZ[\]^\_!" IJKLMNDPQRSTUVWXYZ[\]^\_ !"#: JKLMNOPQRSTUVWXYZ[\]^\_!"#: KLMNOPQRSTUVWXYZ[\]^\_!"#\$;

Unequalled print quality.

Printronix printer/plotters are the only matrix line printers that form characters one dot row at a time, overlapping them vertically and horizontally with uniform hammer energy to produce solid appearing characters of unequalled print quality on the first to last copy of 6-part forms. They're even suitable for OCR equipment.

Unlimited font versatility.

Unlike drum/chain/belt printers with fixed, engraved fonts, Printronix characters are formed electronically, via plug-in PROM's, permitting unlimited versatility in font styles. Printer capacity is 160 characters. For example, a 96 ASCII set plus a 64 set such as OCR or a foreign language set.



Full plotting capability.

Its unique design enables the Printronix Printer to plot anything: drawings, graphs, bar codes, large characters, labels.

This significant capability is provided at no extra cost!



Incomparable reliability.

The key to Printronix superb print quality and demonstrated high reliability is an elegantly simple printing mechanism unlike any other. It is comprised of flat, spring steel hammers, each controlled electronically by its own simple coil. That's all. Periodic adjust-ments for character alignment are never required as with drum/chain/belt printers. With up to 50% fewer

parts than mechanical font

printers, a Printronix should

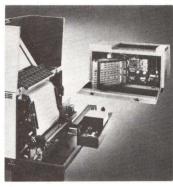
have proportionately higher

Minimum downtime.

Modular construction provides easy access to all function modules to hold maintenance and repair time to a minimum.

This new breed has set the pace for performance, versatility, reliability, and cost of ownership for 150 and 300 line-minute printers. Try one. Write or call for complete information.

Printronix, Inc., 17421 Derian, Irvine, CA 92714. (714) 549-8272





#### LITERATURE

#### µComputer Analog I/O System

Data sheets give description, theory of operation, specs, block diagrams, and operating instructions for 64-channel analog input/2-channel analog output systems. Burr-Brown, Tucson, Ariz.

Circle 300 on Inquiry Card

#### **OEM Impact Printers**

Data sheet depicts line of model 40, fully operational, 300-line/min OEM printers by pointing out std features and technical information. **Teletype Corp**, Skokie, Ill. Circle 301 on Inquiry Card

#### **Power Supplies**

Typ applications, selection guide, electrical and mechanical spec listings, and outline drawings appear in 52-pg catalog on single, dual, and triple output models. **Acopian Corp**, Easton, Pa.

Circle 302 on Inquiry Card

#### **Miniature Motors**

Catalog condenses specs and performance data for precision miniature ac and dc motors, gearmotors, fans, and blowers, which deliver up to 500 ft³/min of air. TRW Inc, TRW Globe Motor Div, Dayton, Ohio.

Circle 303 on Inquiry Card

#### **Fiber-Optic Connectors**

Color data sheets point out features of gold-plated fiber-optic connectors, designed for precision alignment and compatibility with conventional single fiber cables. Hughes Aircraft Co, Connecting Devices Div, Irvine, Calif.

Circle 304 on Inquiry Card

#### **Microcomputer System**

Catalog details Horizon computer and S-100 bus peripherals, including floppy disc systems, monitors, boards, and CRT terminals. North Star Computers, Inc, Berkeley, Calif.

Circle 305 on Inquiry Card

#### **uProcessor Power Supplies**

Including features, voltage and current ratings, and physical data, booklet depicts MPU-1 and -2 dual and triple output power supplies. Lambda Electronics, div of Vecco Instruments Inc, Melville, NY. Circle 306 on Inquiry Card

#### **Electronic Test Accessories**

Covering molded patch cords and test leads, cable assemblies, test socket adaptors, connecting leads, and banana and phone plugs, 86-pg catalog also contains cable and wire description and metric conversion charts. ITT Pomona Electronics, a div of ITT, Pomona, Calif.

Circle 307 on Inquiry Card

#### Digital Switches/Keyboards

Characteristics of nine digital switches, plus low profile keyboards and general-purpose thumbwheel and lever switches, are given in product guide which provides photos and feature/option chart. The Digitran Co, a div of Becton, Dickinson, and Co, Pasadena, Calif. Circle 308 on Inquiry Card

#### **Data Communications**

Catalog describes Range Rider® test sets, Hawk® 4000 datatraps, automatic data error correctors, frontend processor switches, and EIA data cables, in addition to other data communications products. International Data Sciences, Inc, Providence, RI.

Circle 309 on Inquiry Card

#### **Disc Controllers**

Literature discusses Phoenix 311 mass storage disc controller for Data General computers, which provides up to 1.2G bytes of online storage, and can be connected to up to four storage modules or disc drives offered by various manufacturers. **Xylogics**, **Inc**, Burlington, Mass. Circle 310 on Inquiry Card

#### **Wire Line Modems**

Applications and features of 263A wire line modem, which transmits and receives digital data up to 24 mi (39 km), are detailed in 28-pg booklet including its operation, engineering, installation, and maintenance. GTE Lenkurt Inc, San Carlos, Calif.

Circle 311 on Inquiry Card

#### **Hyperbolic Function Generator**

Application notes present theories of operation, design considerations, schematic diagrams, and waveform displays focusing on generation of hyperbolic functions by Bifet op amps and DACS. Precision Monolithics Inc, Santa Clara, Calif.

Circle 312 on Inquiry Card

#### RAM and p/ROM Boards

Specs and features of SBC 80/10 compatible memories are discussed in data sheet with photos of RAM-8 and p/ROM-8 boards. Electronic Solutions, Inc, San Diego, Calif.

Circle 313 on Inquiry Card

#### Microprocessors

Booklet exhibits basic functions, pin numbers, signal names, and interfacing of the 8080A family components to the company's Microbus<sup>TM</sup>. National Semiconductor Corp, Santa Clara, Calif.

Circle 314 on Inquiry Card

#### **Instrumentation Amps**

Four models of DX series high performance amps are cited in brochure which supplies specs, outline dimensional diagrams, and photo of front panel controls. **Preston Scientific, Inc,** Anaheim, Calif. Circle 315 on Inquiry Card

#### **Computer Systems**

Brochure details hardware and software features of Eclipse M/600 systems including topics on computation abilities, operating systems, programming aids, and peripherals. **Data General Corp**, Westboro, Mass.

Circle 316 on Inquiry Card

#### **Text Editors and Printers**

Leaflet provides features of advanced Redactor I Series Q printer editing typewriter, together with Q-Pak printer that upgrades existing equipment. Redactron Corp, Hauppauge, NY.

Circle 317 on Inquiry Card

#### **Coaxial Cables**

Guide provides concise information on terminology and formulas necessary to understand design and function of PTFE and FEP coaxial cables. Haveg Industries, Inc, Winooski, Vt. Circle 318 on Inquiry Card

#### Mobile Power Supply System

Bulletin covers PEP system, a self-contained, regulated, uninterruptible electric power source designed to provide ac power to electronic equipment. Marine Electric RPD Inc, Edison, NJ.

Circle 319 on Inquiry Card



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#### LITERATURE

#### **Light Emitting Diodes**

By presenting dimensional diagrams, electrical and mechanical data, and operating characteristics, catalog highlights line of LED panel lights, packaged LEDS, and accessories. Data Display Products, Inglewood, Calif.

Circle 320 on Inquiry Card

#### **Gate Arrays**

Data sheet on ECL 10k gate array presents electrical and mechanical characteristics, logic and circuit diagrams, logic level and swings, package outline, dimensional drawings, and pin assignments. NEC America, Inc., Santa Clara, Calif.
Circle 321 on Inquiry Card

#### Programmed Access/ Security System

Components, backup equipment, and processor options of PASS<sup>TM</sup> system, which visually displays location of emergency condition when it occurs, appear in 2-pg data sheet. Cardkey Systems, a div of Greer Hydraulies, Inc, Chatsworth, Calif. Circle 322 on Inquiry Card

#### **Line Printers**

Brochure including specs and photos describes chaintrain, drum, dot matrix, and thermal line printers which feature builtin, offline test capability and minicomputer compatibility. **Digital Associates Corp**, Stamford, Conn.

Circle 323 on Inquiry Card

#### **Thumbwheel Switches**

Diagrams, truth tables, and module specs are offered in bulletin on series of littel. Thumbwheel<sup>R</sup> miniature sealed and unsealed switches, which feature rear panel mounting and variety of output codes. Switcheraft, Inc, Chicago, Ill. Circle 324 on Inquiry Card

#### **Switchers**

Input and output characteristics, general specs, construction and circuit details, stabilization tables, and photos are given in 8-pg booklet on variety of single and triple output switching power supplies. **Kepco, Inc,** Flushing, NY.

Circle 325 on Inquiry Card

#### **Open Frame Power Supplies**

Catalog presents specs, photos, and mechanical drawings of 83 models of dc power supplies including single, dual, and triple

outputs, as well as models for floppy disc/microprocessor applications. Power One Inc, Camarillo, Calif.
Circle 326 on Inquiry Card

#### **Computer Interconnections**

Sample programs and flowcharts depicting techniques for program to program communication between HP 1000 systems and HP 9825 desktop computers are shown in application note. Hewlett-Packard Co, Palo Alto, Calif.

Circle 327 on Inquiry Card

#### uComputers/Digital Logic Modules

Encompassing a line of microcomputers, digital logic modules, and software, brochure includes photos and facts on parallel and serial digital 1/0, analog 1/0, and communications modules. Wyle Laboratories/Computer Products, Hampton, Va. Circle 328 on Inquiry Card

#### **Bell Compatible Modem**

Pointing out troubleshooting features, illustrated bulletin discusses advantages of the 7208, a 4800-bit/s modem that transmits over unconditioned voice-grade lines. Tele-Dynamics Div of Ambac Industries, Inc, Fort Washington, Pa. Circle 329 on Inquiry Card





#### **GUIDE TO PRODUCT INFORMATION**

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Monochrome CRT

#### THE DEDICATED CONSUMER MICROCOMPUTER MARKET

Frost & Sullivan has completed a 174-page report analyzing and forecasting the market through 1984, in numbers of units and sales value, for both the dedicated consumer microcomputers and the end-use market they used in: home video games, microwave ovens, other appliances, automobiles, calculators and other markets.

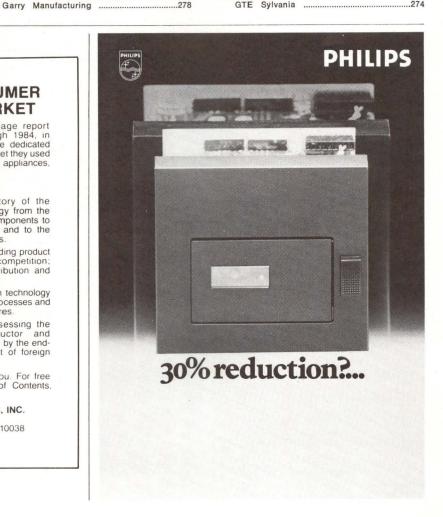
The study:

- Reviews the background and history of the microprocessor/microcomputer technology from the early four-function personal calculator components to the general purpose multi-chip systems and to the single-chip systems for consumer products.
- Probes expected industry trends, including product obsolescence; domestic and foreign competition; problems associated with pricing, distribution and availability; and vertical integration.
- Investigates the latest developments in technology including an analysis of semiconductor processes and a discussion of microcomputer architectures.
- Reviews the industry suppliers, assessing the strategies of the U.S. semiconductor and microcomputer suppliers, possible moves by the endproduct producers and also the impact of foreign suppliers.

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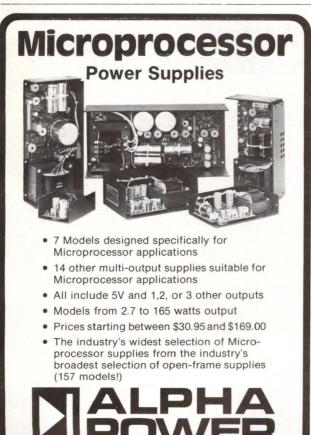
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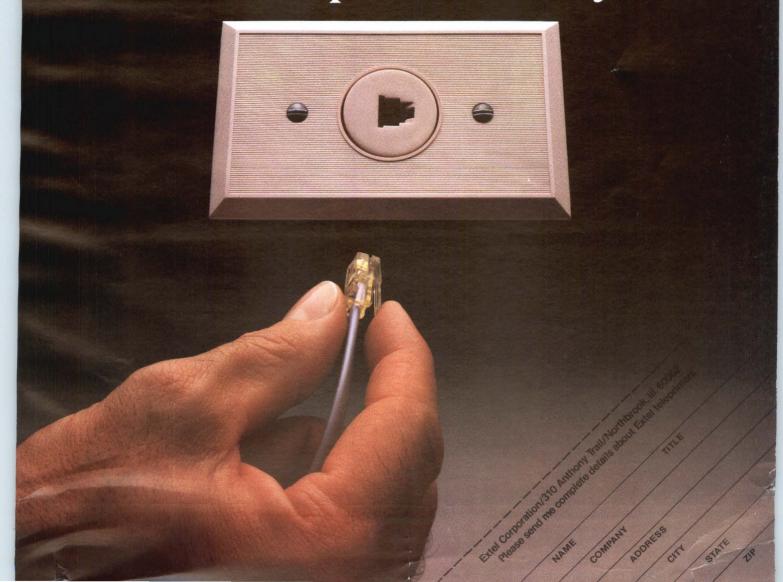
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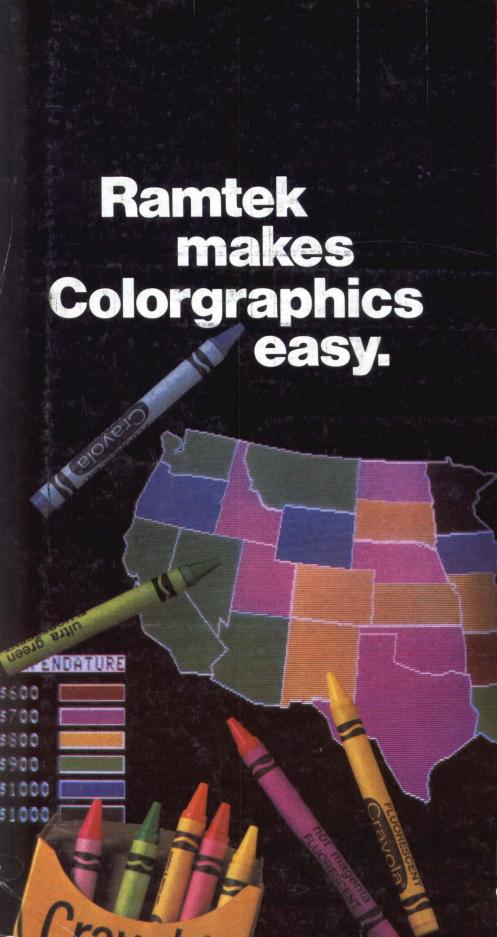
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