COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JUNE 1979

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BUBBLE MEMORY RECORDERS FOR SPACE APPLICATIONS

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* Trade name of Digital Equipment Corp.

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There's more. Designed to wage war on the lost time of downtime, the Tally T-3000 is modularly constructed for quick service access. And the diagnostic display pinpoints any fault condition. And even tells if it's operator correctable.

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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DEPARTMENTS

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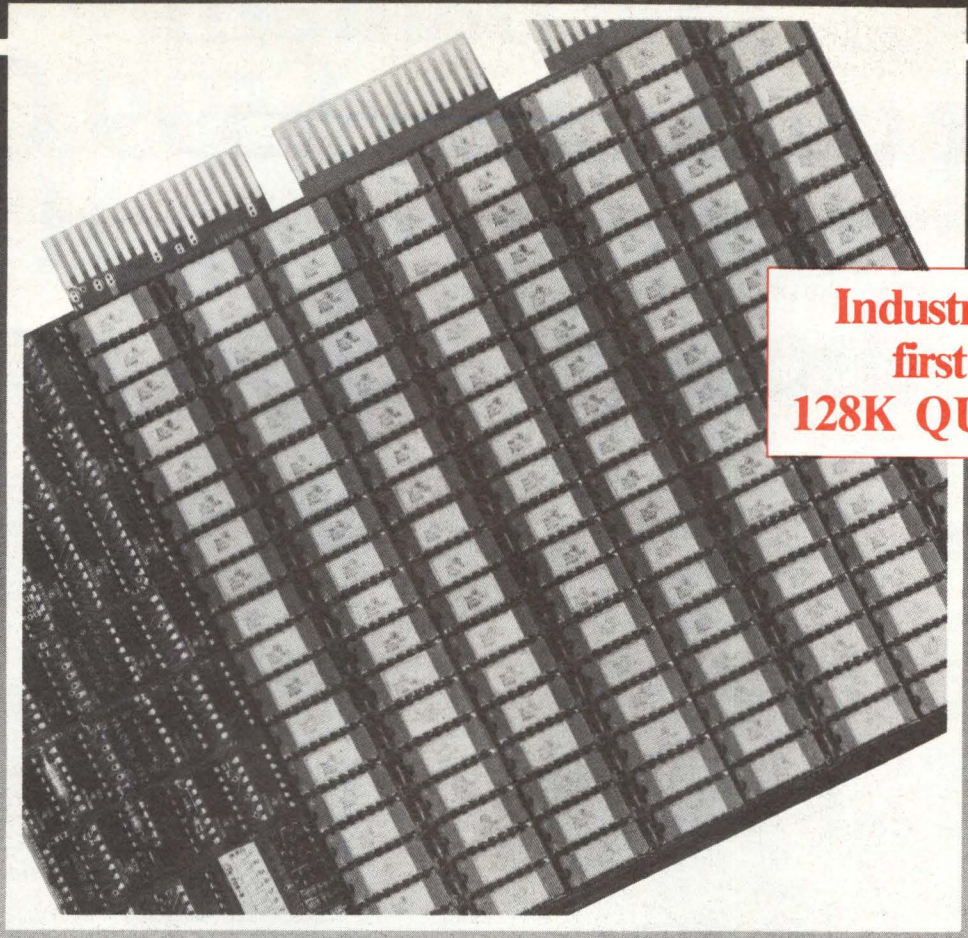

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128K x 18 FOR LSI-11/23®

Dataram Corporation, first to offer a 128K x 18 single-board PDP®-11 ADD-IN, has done it again.

This time with an incredible 128K x 18 semiconductor ADD-IN for DEC®'s LSI-11/23!

This industry first, the DR-113S, is packaged on a standard DEC 8½" x 10" quad board. But more than just being a "first," the DR-113S is also a "best," saving you not only space and money, but also greatly reducing overhead circuitry, optimizing MTBF, and minimizing power consumption. And the DR-113S is also available in 64K and 96K configurations.

From Dataram Corporation, the people who provide everything you need to make a big thing out of the LSI-11 —
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CIRCLE 5 ON INQUIRY CARD

The Bantam. The cocky new $599* CRT that just changed the pecking order.

User Need	Feature	P-E BANTAM	LSI ADM-3A	Hazeltine 1400	Hazeltine 1500	Adds Regent 100
Easy to read display	7 x 10 matrix for highly legible characters	Yes	No	No	Yes	No
	Black on white or white on black display	Yes	No	No	Yes	Yes
	Display set deep in hood to reduce glare	Yes	No	No	No	No
	Full 24 x 80 display	Yes	Yes	Yes	Yes	Yes
	Full upper and lower case	Yes	Option	No	Yes	Yes
	Non-glare screen	Option	Yes	No	Yes	Yes
High operator throughput, low operator fatigue	Tab stops/tab key	Yes	No	No	Yes	Yes
	Backspace key	Yes	No	No	Yes	Yes
	Repeat key	Yes	Yes	No	No	Yes
	Shiftlock key	Yes	No	No	No	No
	Separate print key	Yes	No	No	No	Yes
Convenient switching Local/on-line	Local—remote key	Yes	No	Option	Option	Yes
International Character sets	French/German/ Swedish/Danish/ British/Spanish	Option	Option	No	Option	Option
High speed numeric	Integrated numeric pad	Yes	Option	No	Yes	Yes
Convenient system interfacing	RS-232/CCITT-V24	Yes	Yes	Yes	Yes	Yes
	Current loop	Option	Yes	No	Yes	Yes
Simplified program debugging	Transparent mode and displayable control characters	Yes	No	No	No	No
Faster maintenance	Self-test	Yes	No	Yes	No	Yes
Minimum desk space	Small size	15Wx 19Dx 14H	15.5Wx 20.2Dx 13.5H	15.5Wx 20.5Dx 13.5H	15.5Wx 20.5Dx 13.5H	21Wx 23Dx 14.5H
Printer port	Printer port	Option	Yes	No	Yes	Option
Cost effectiveness	Qty. 100 OEM price	$599†	$740	Less than $550 in quantity 1000	$860	$895

*In quantities of 100.
†Qty. 1, End User Price $966.

Nobody ever offered you a tough, high quality, compact CRT like the BANTAM before. At $599 or any price. Designed for hectic office environments. And, human engineered to make an operator's life easier.

You get everything you need for cleaner input and faster throughput. An upper and lower case character set displayed on a sharp 7 x 10 dot matrix. A full 24-line by 80-character screen. A complete, sure-touch keyboard with shadow numeric pad.

You get complete tabbing. Full cursor addressing. Repeat, backspace and shiftlock keys. A transparent mode with displayable control characters to simplify host program debugging. And, a self-test mode for easy maintainability.

And, you get everything your operators need to make their jobs a joy. A hooded display that cuts glare. A wide bandwidth monitor for sharp images everywhere on the screen. Below-the-line character descenders to make reading easier.

A switchable white-on-black or black-on-white display, whichever your operator prefers. An easy-to-find cursor that frames the entire character position in a transparent, inverted video block.

Plus plenty of options you can't get with CRTs costing much more. Like our low-cost Pussycat page printer. A full range of foreign language character sets. We even have a model you can switch from ASCII to full overstrike APL.

But that's not all. The BANTAM's compact good looks fit any decor. It's handsome enough for executive row and rugged enough for the stockroom. Silent? The BANTAM's fan-free design makes it quieter than an electric typewriter. And, the BANTAM only weighs 28 pounds.

Only an industry leader like Perkin-Elmer could do it. We designed a powerful, custom LSI controller chip that makes the BANTAM the one and only high quality CRT in its class.

But see for yourself. Use the comparison chart. Learn why we're so proud to add this $599 CRT to the 250,000 peripherals that bear our good name.

And, remember our terminals come equipped with a No Hassle, 800 toll-free service phone number.

One call does it all. We give you service *where* you need it, when you need it. We're there. Not just "worldwide," but wherever you are.

For more information call or write Perkin-Elmer Terminals Division, Randolph Park West, Route 10 & Emery Avenue, Randolph, N.J. 07801 (201) 366-5550. Or contact any of our sales offices. Then watch the feathers fly.

The Bantam's available at all these places

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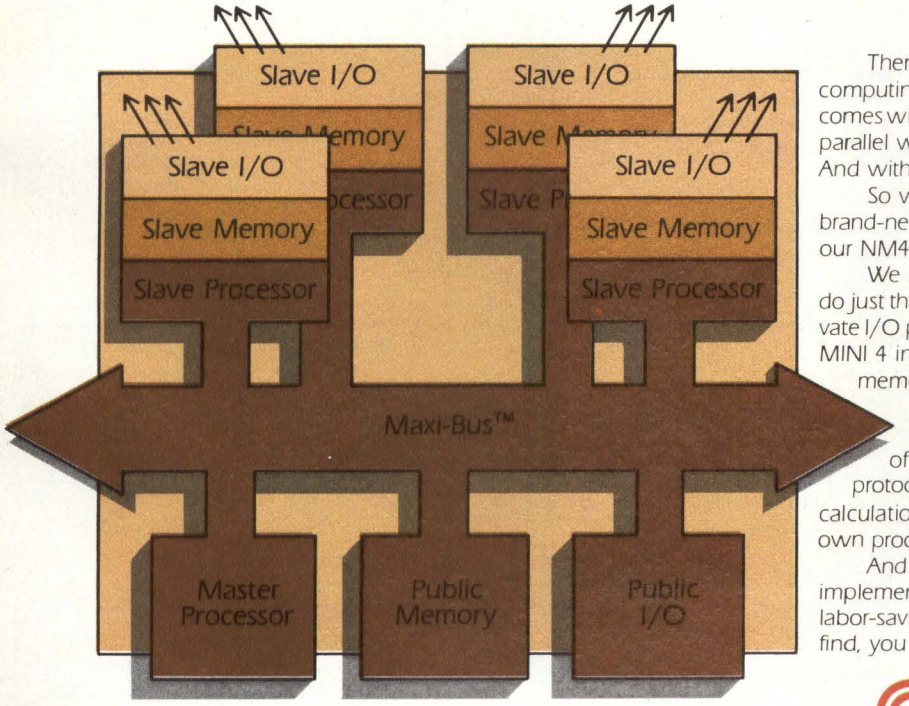
PERKIN-ELMER

CIRCLE 6 ON INQUIRY CARD

INTRODUCING "SLAVE COMPUTING."

Finally. An innovative alternative to multi-processing.



There is a powerful difference between slave computing and multi-processing. A slave computer comes with its own memory and I/O. And it operates in parallel with the host processor. On the same bus. And with minimal software headaches.

So we've implemented this concept with our brand-new 4/10S (the "S" stands for slave) to work with our NM4 and LSI-2 as masters.

We made sure the 4/10S is well-equipped to do just that. A private, 32K byte RAM memory. Four private I/O ports. A real-time clock. An extended NAKED MINI 4 instruction set. Plus, full access to its master's memory and peripherals.

Working in parallel with a master, up to four 4/10S computers can process all kinds of off-loaded tasks. Like communications protocol jobs. Process control work. Even complex calculations. All without slowing down the hosts' own processing chores.

And our system's software makes it easy to implement. Contact Computer Automation for the labor-saving details. With good help getting harder to find, you can't beat it. Not even with a whip.

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CIRCLE 7 ON INQUIRY CARD

CALENDAR

CONFERENCES

JULY 16-18—Summer Computer Simulation Conf, Toronto, Canada. INFORMATION: Dr A. J. Schiewe, Chm 79 SCSC, c/o The Aerospace Corp, PO Box 92957, Los Angeles, CA 90009

JULY 17-20—Joint Intermag/Magnetism and Magnetic Materials Conf, Statler Hilton, New York, NY. INFORMATION: Dr E. F. Luborsky, Conf Chm, General Electric R&D Ctr, PO Box 8, Schenectady, NY 12301

AUG 6-8—Pattern Recognition and Image Processing, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: PRIP 79, PO Box 639, Silver Spring, MD 20901

AUG 13-15—Conf on Simulation, Measurement, and Modeling of Computer Systems, Boulder, Colo. INFORMATION: Paul F. Roth, National Bureau of Standards, Technology Bldg, Rm B-250, Washington, DC 20234

AUG 21-24—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: 1979 Internat'l Conf on Parallel Processing, Dept of Electrical and Computer Engineering, Wayne State U, Detroit, MI 48202

SEPT 4-7—COMPCON, Washington, DC. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEPT 5-7—Internat'l Fiber Optics and Communications Exposition, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Michael A. O'Bryant, Director, Expositions and Publications, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

SEPT 5-8—INFO/ASIA, Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017

SEPT 7-9—Internat'l Microcomputer Exposition, Dallas, Tex. INFORMATION: IME, 413 Carillon Tower, 13601 Preston Rd, Dallas, TX 75240

SEPT 17-19—Fourth Internat'l Conf on Software Engineering, Munich, Germany. INFORMATION: Prof Fritz Bauer, Institut fur Informatik der Technischen Universitat, D-8, Munchen 2 Arcisstrasse 21, Postfach 90 94 90, Germany

SEPT 17-19—Optical Communication Conf, RAI Conf Buildings, Amsterdam, The Netherlands. INFORMATION: J. H. C. Van Heuven, Philips Research Labs, Eindhoven, The Netherlands

SEPT 18-20—5th European Solid State Circuits Conf, U of Southhampton, England. INFORMATION: IEE Conf Dept, Savoy Place, London WC2R OBL, England

SEPT 18-21—WESCON, Brooks Hall and St Francis Hotel, San Francisco, Calif. INFORMATION: William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/722-2965

SEPT 19-21—Internat'l Automatic Testing Conf, Radisson Hotel, Minneapolis, Minn. INFORMATION: A. O. Thornsjo, Honeywell Inc, 1625 Zarthan Ave S, St Louis Park, MN 55416. Tel: 612/542-4811

SEPT 20-26—TELCOM '79, Geneva, Switzerland. INFORMATION: John Sodolski, 2001 Eye St NW, Washington, DC 20006. Tel: 202/457-4934

SEPT 25-27—Mini/Micro Computer Conf and Expo, Anaheim, Calif. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807

SEPT 25-29—Relcomex '79—Reliability and Exploitation of Computer Systems, Ksiaz Castle, Wroclaw, Poland. INFORMATION: I. Jozwiak, Institute of Engineering Cybernetics of Wroclaw Technical U, Janiszewskiego St 11/17, 50-372 Wroclaw, Poland

SEPT 26-29—Mini and Microcomputers Internat'l Sym and Exhibition, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: The Secretary, MIMI '79, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

SEPT 28-30—Northeast Personal and Business Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: Northeast Expositions, PO Box 678, Brookline Village, MA 02147. Tel: 617/522-4467

OCT 2-4—Internat'l Electrical, Electronics Conf and Exposition, Exhibition Place, Toronto, Canada. INFORMATION: Internat'l Electrical, Electronics Conf and Exposition, 1450 Don Mills Rd, Don Mills, Ontario M3B 2X7, Canada

OCT 3-5—Internat'l Conf on Very Large Data Bases, National Hotel, Rio de Janeiro, Brazil. INFORMATION: Prof Stanley Y. W. Su, 500 A Weil Hall, U of Florida, Gainesville, FL 32611. Tel: 904/392-2371

OCT 9-11—Compusign, Anaheim, Calif. INFORMATION: Golden Gate Enterprises, Inc, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94087. Tel: 408/735-1122

OCT 22-24—Computers in Aerospace Conf, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Richard Erkeneff, McDonnell Douglas Astronautics Co, Dept 236, Bldg 13-3, 5301 Bolsa Ave, Huntington Beach, CA 92644. Tel: 714/896-4975

OCT 23-25—European Sym on Realtime Data Handling and Process Control, West Berlin, Germany. INFORMATION: Real-Time Data 79, Congress Organization Co, Kongress Zentrale, John Foster Dulles Allee 10, D-1000 Berlin 21, Germany

OCT 23-25—Test Conf on Semiconductors, Hyatt House, Cherry Hill, NJ. INFORMATION: Raymon Oberly, Program Chm, IBM Corp, PO Box 100-53X 057, Kingston, NY 12401

OCT 29-31—Foundations of Computer Science, San Juan, Puerto Rico. INFORMATION: Prof Ronald V. Book, Dept of Math & Computer Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778

NOV 6-8—COMPEC Peripherals, Systems, and Mini and Microcomputer Specialized Exhibition, Olympia Grand Hall, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

SEMINARS

JULY 9-11, 18-20, and 23-25—Data Communications—An Introduction to Concepts and Systems; and JULY 9-11 and 16-18—Distributed Systems—Are They Right for You? San Francisco, Calif, Washington, DC, and Detroit, Mich; and Washington, DC and Los Angeles, Calif. INFORMATION: Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100

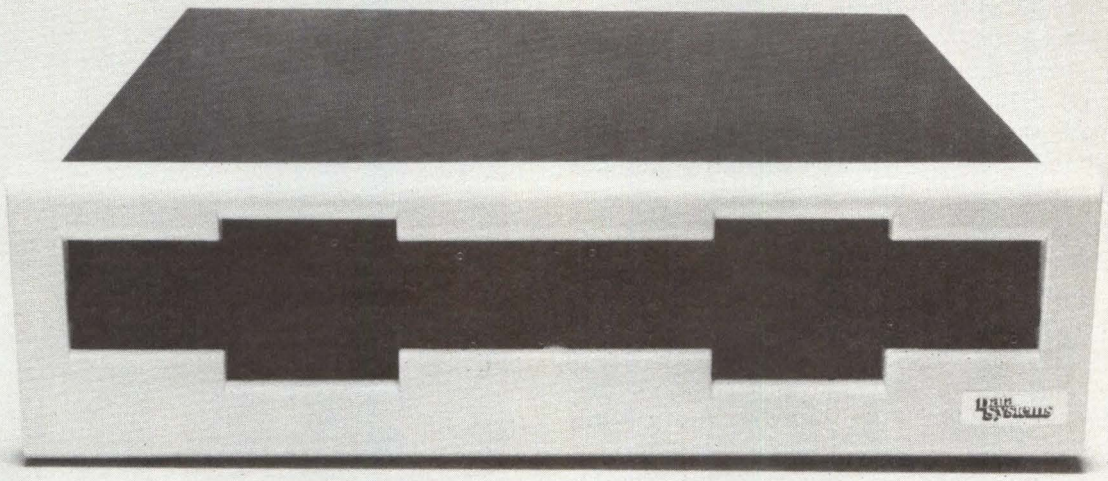
JULY 23-25 and AUG 15-17—Minicomputers and Distributed Processing, Toronto, Canada and Atlanta, Ga. INFORMATION: Heidi E. Kaplan, Dept 20 NR, U of Chicago Continuing Education Programs, 360 Lexington Ave, New York, NY 10017. Tel: 800/223-7450

SHORT COURSES

JULY 9-13—Microprogramming Workshop, and JULY 16-27—Designing Microprocessor Based Systems, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Director of the Summer Session, Rm E19-356, MIT, Cambridge, MA 02139. Tel: 617/253-2101

Announcements intended for publication in this department of *Computer Design* must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,



AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

FOR LESS

The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery... at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

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CIRCLE 8 ON INQUIRY CARD

The intelligent memory for PDP®-11/70's.

More than bits in a box. The MSC 3602 PDP-11/70 add-on memory has its own microcomputer that keeps it, your 11/70 and you out of trouble.

Up to 4 megabytes with single bit error correction and double bit error detection that won't hassle your CPU.

Intelligence speaks for itself. The self-diagnostic microcomputer has RS-232 I/O. No need to interrupt your system. Connect your terminal and the MSC 3602 will speak for itself. You'll know the specific memory addresses which have experienced self corrected one bit errors.

Even without a terminal you can easily view error indications on the front LED display.

Knowing better. The MSC 3602 knows better than to cause a system crash. The microcomputer scans one bit errors from its storage register and decodes them into a usable format. No more need for look-up charts. And error dumps to the terminal can be programmed at any timed interval.

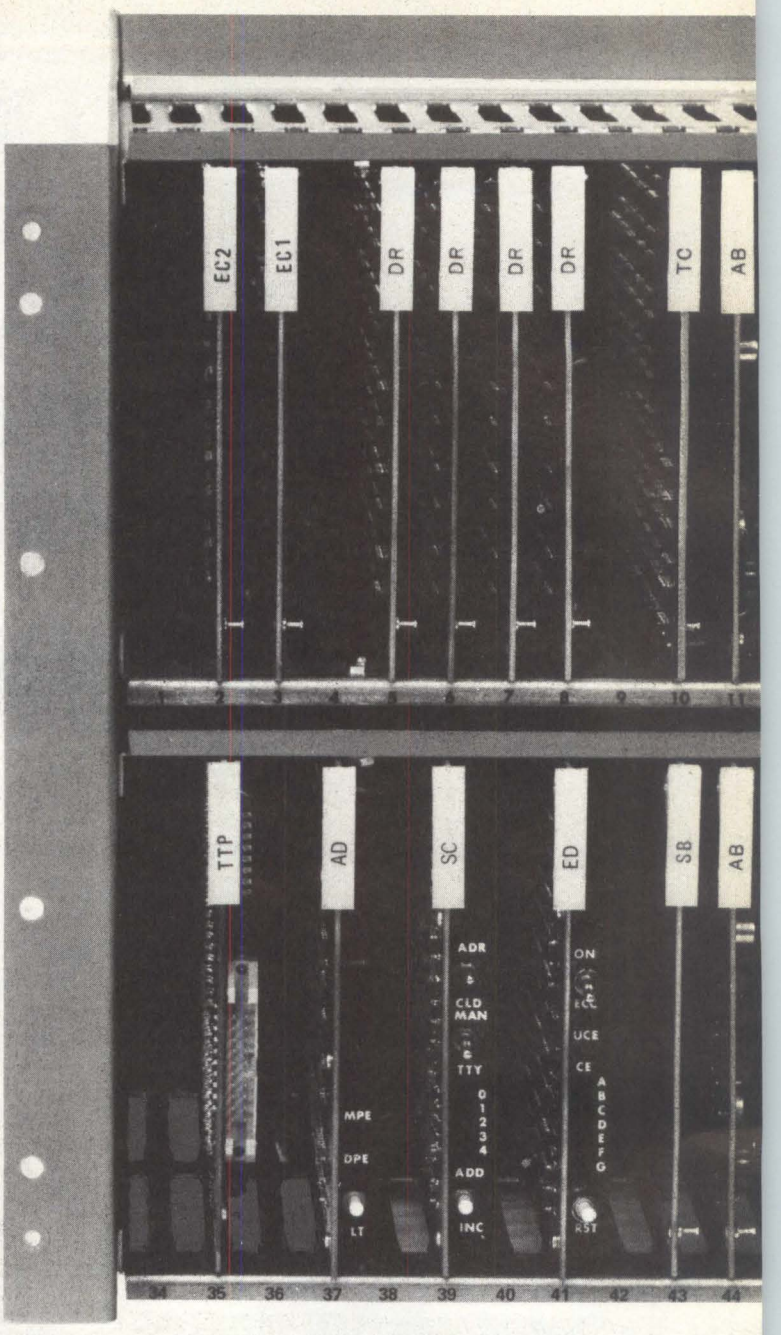
A double bit error causes a parity error message to be sent directly to the CPU.

Turn off the ECC and you can run full diagnostics.

Leaving interleaving. Our intelligent add-on performs at maximum bus speed without using complex interleaving addressing techniques. So, the MSC 3602 is easier to maintain and simpler to manage for you and your 11/70.

Memorizing more? The MSC 3602 will grow with you. It's expandable in 64K byte increments, with 2 megabytes in a single 10½" high free-standing or rackmount chassis including power supply and forced air cooling. An additional 10½" chassis will give you the total 4 megabyte PDP-11/70 maximum memory.

And MOS memory offers you low power requirements. Nonvolatility is available with battery backup.



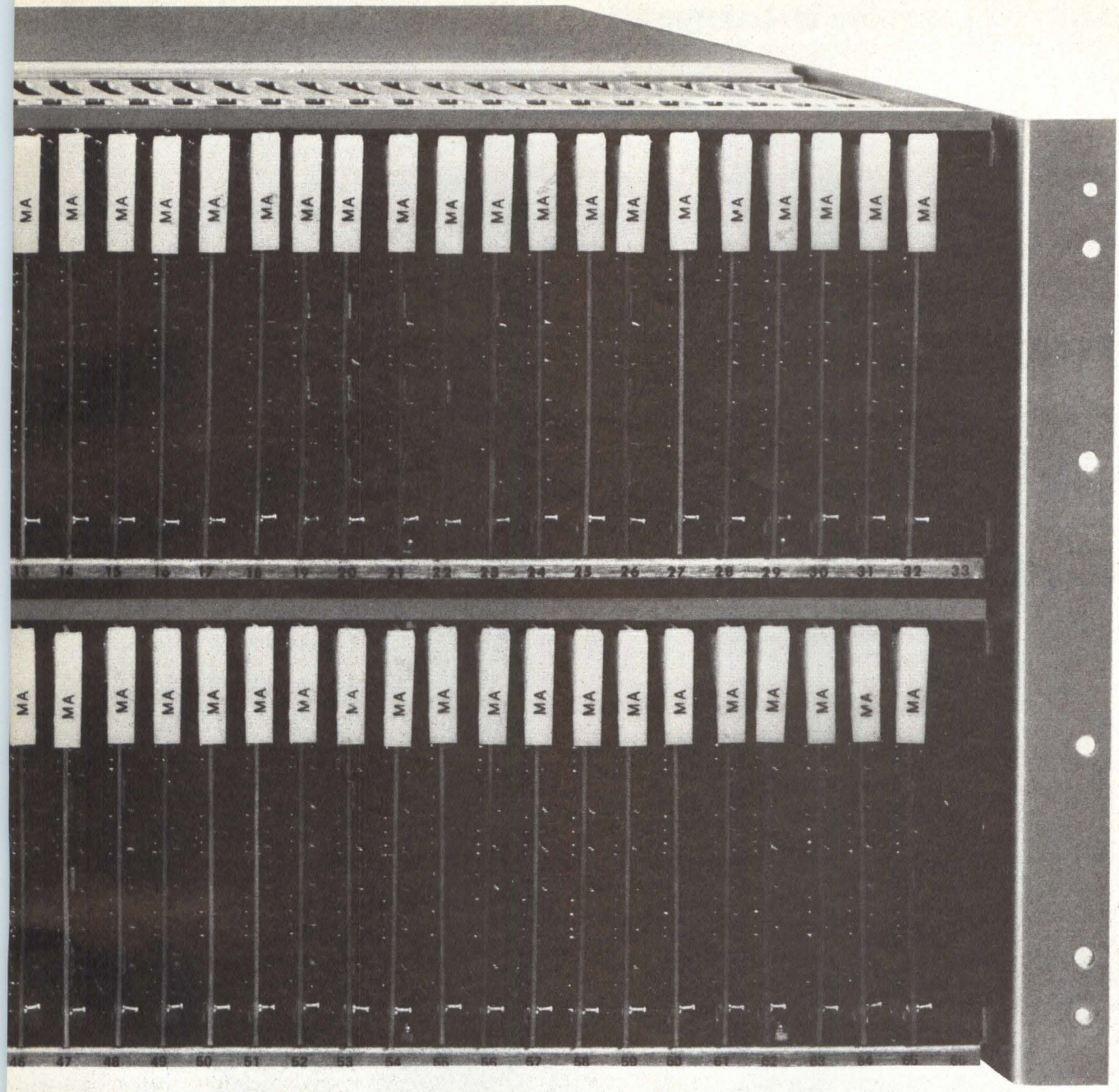
Intelligent design. The MSC 3602's small size allows close placement to the CPU. Shorter bus lengths allow higher speed and reduce noise problems.

Socketed elements offer easy maintenance.

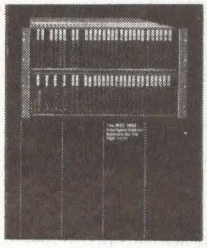
All cards are removable from the front.

Taking care of you. The MSC 3602 will help your system and your budget. It is competitively priced with unintelligent core and semiconductor add-ons.

PDP is a registered trademark of Digital Equipment Corp.



Send away.



Our new brochure fully describes the MSC 3602's features. Call or send for it today.

Intelligent memory... from the first.

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CIRCLE 9 ON INQUIRY CARD

EMERGENCE OF THE INTEGRATED SERVICES DIGITAL NETWORK

Russell G. DeWitt

Western Union Telegraph Company
Upper Saddle River, New Jersey

In the United States, Canada, the United Kingdom, France, Switzerland, Italy, and elsewhere in the world, telecommunication networks are gradually going digital, and this trend will continue. That this should happen should surprise no one. Digital computers replaced analog machines many years ago because they were more cost effective, accurate, powerful, and flexible. The slide rule gave way to the digital calculator, and digital wrist watches have all but replaced their analog counterparts because of improved accuracy and the ability to provide more information than the time of day. Clearly, solid state technology has fueled this digital evolution for both telecommunication networks and for the simpler examples cited. The steady decrease in the cost of a pair of logic gates or a memory bit over the past 15 years (Fig 1) has also been an important factor in the trend toward the implementation of digital techniques.

Digital vs Analog Overview

"What's past is prologue." Digital transmission appeared much earlier in the history of communications than did analog methods. Smoke signals, drumbeats, signal flags, windmill arms, and lanterns were used to send discrete messages. A famed example is the "one if by land and two if by sea" message to Paul Revere from lanterns in the tower of the Old North Church. Also, at the end of the 18th century, towers using semaphore arms, situated at line of sight distances, relayed messages across Europe at a speed of one signal per minute for many hundreds of miles.[1] With the invention of the electric telegraph in 1835 the Morse code, another form of digital transmission, took over as a signaling medium.

The coming of the telephone in 1876 marked the beginning of analog transmission, which quickly became the dominant method because voice traffic grew more rapidly than did telegraph.[2] With the invention of pulse code modulation (PCM) by A. H. Reeves in 1938, and of the transistor by Shockley, Bardeen, and Brattain in 1948, there was a resurgence of the digital mode. The first PCM carrier system, called T1 carrier, was put into production by Western Electric in 1962, and digital transmission technology has been accelerating ever since.

Implementation of PCM

The fact that it took 24 years after the invention of PCM techniques to apply them to live telecommunication service is not surprising. Other important ideas were conceived well before the practical means of implementing them were available; many of Charles Babbage's ideas (1792-1871) which formed the basis of the modern computer could not be put to practical use during his lifetime due to the lack of adequate materials and components.

PCM and computers have much in common. They both manipulate digital information. Therefore they both made early use of discrete, high speed switching transistors as soon as they became available. These devices were replaced by integrated circuits with the accompanying savings in cost and space. Medium scale integration (MSI)

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IDC-

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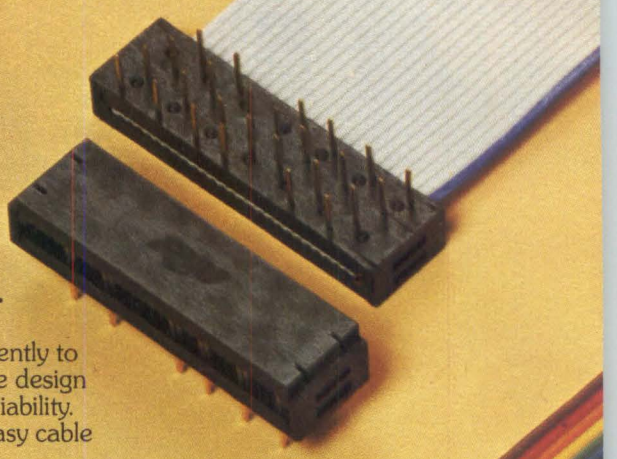
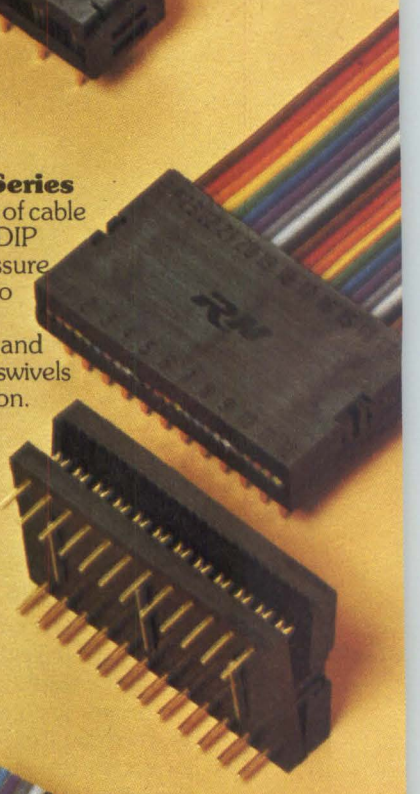


Transition Connectors—IDT Series
Used to attach cable permanently to PCB, Has rugged single piece design for fast assembly and high reliability. Cover latch swivels for easy cable insertion.

Cable Plugs—IDP Series
Offer fast, easy plugging of cable to PCB directly or into DIP sockets. Tapered pins assure quick, easy insertion into DIP sockets. One unit design speeds handling and assembly. Cover latch swivels for easy cable insertion.



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Mounts permanently to PCB and accepts socket connectors. In straight or right angle mounting—for solder or wrap/pin termination. Handy ejector/latch available—when closed it locks socket into place and serves as ejector when open.

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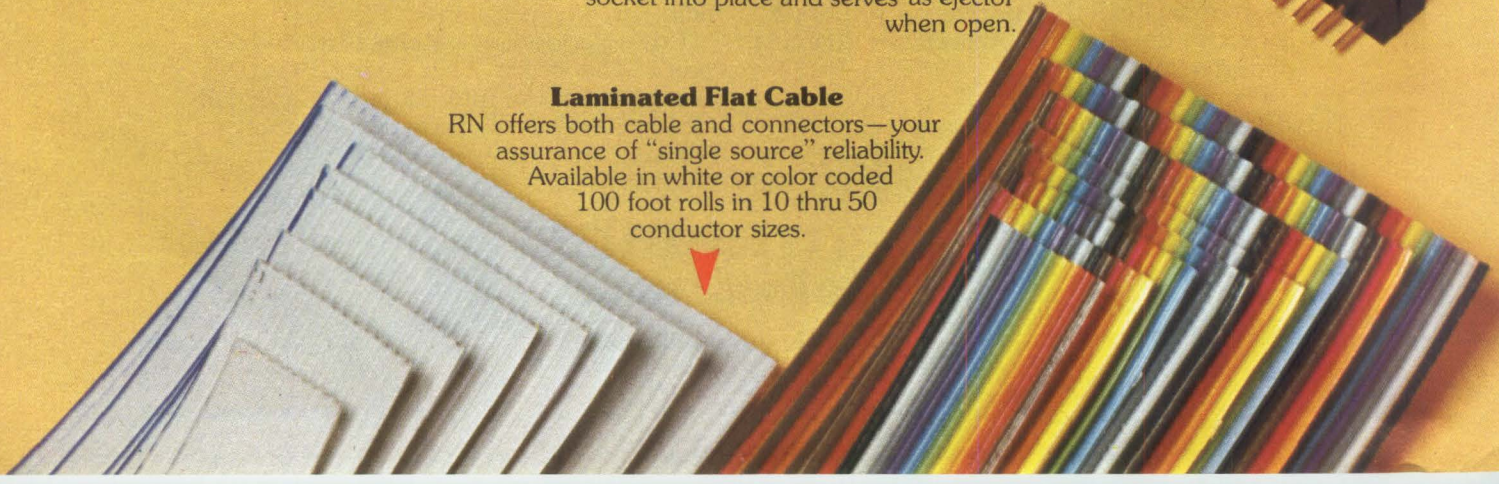

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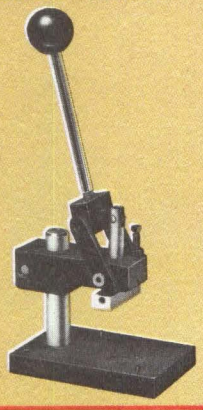

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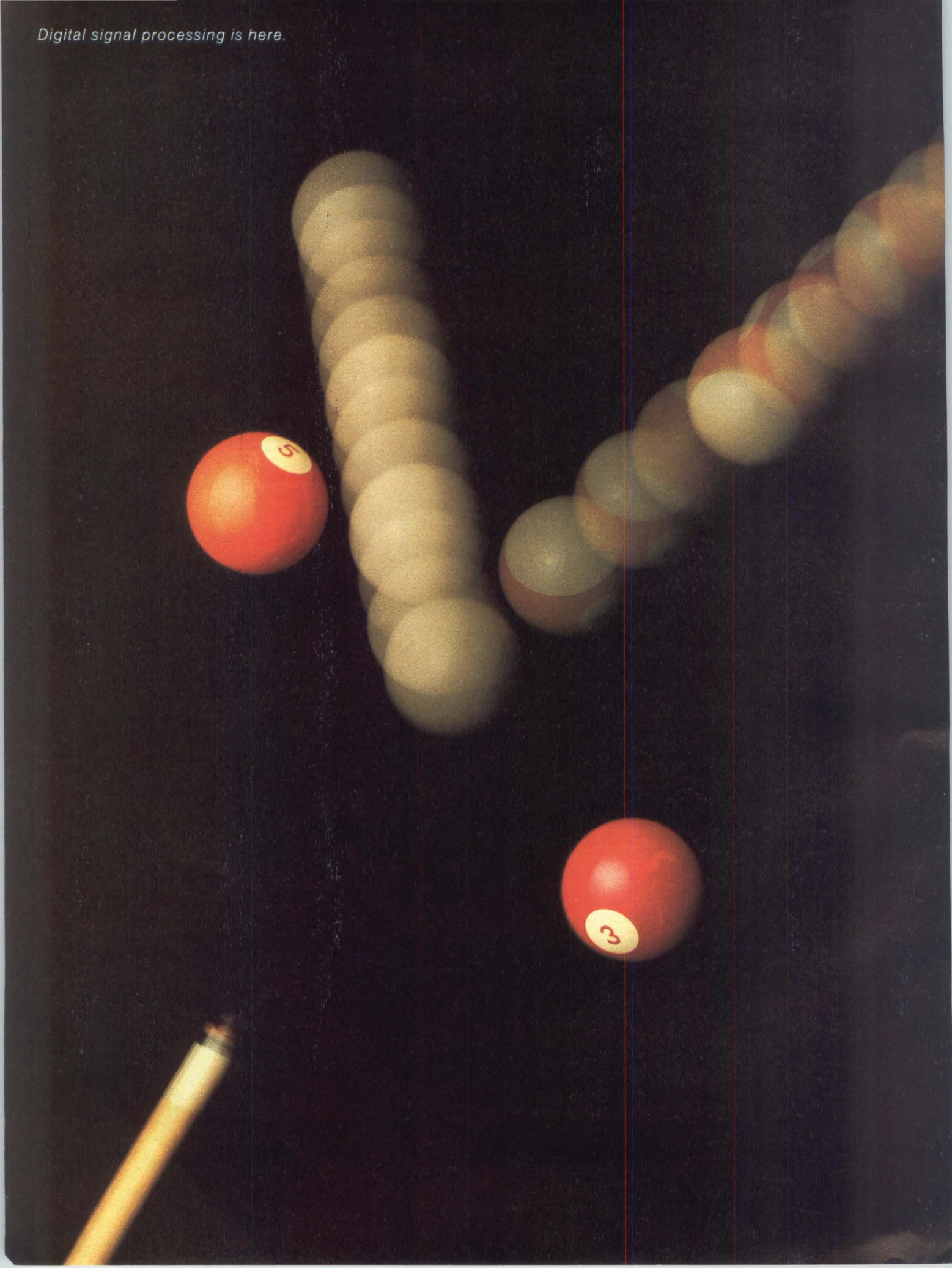
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We've developed a family of single chip, 30MHz A/D converters with VLSI technology. They're TTL devices that bring all the advantages of digital signal processing to high-speed, wide-bandwidth signals like those used in radar, broadcast video and closed-circuit TV systems. We've designated the 8-bit converter TDC-1007J and the 6-bit device, TDC-1014J.

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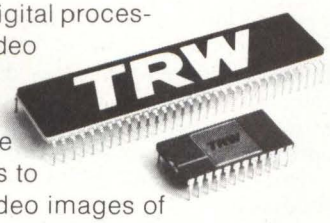

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Our TDC-1007J features full eight-bit resolution. It is a single chip with 255 comparators and a resistive voltage divider. Activating a single device pin strobes the comparators, encodes all their binary outputs into an eight-bit word, and stores the word in an output latch. All this can happen 30 million times a second—now *that's* video-speed data conversion!

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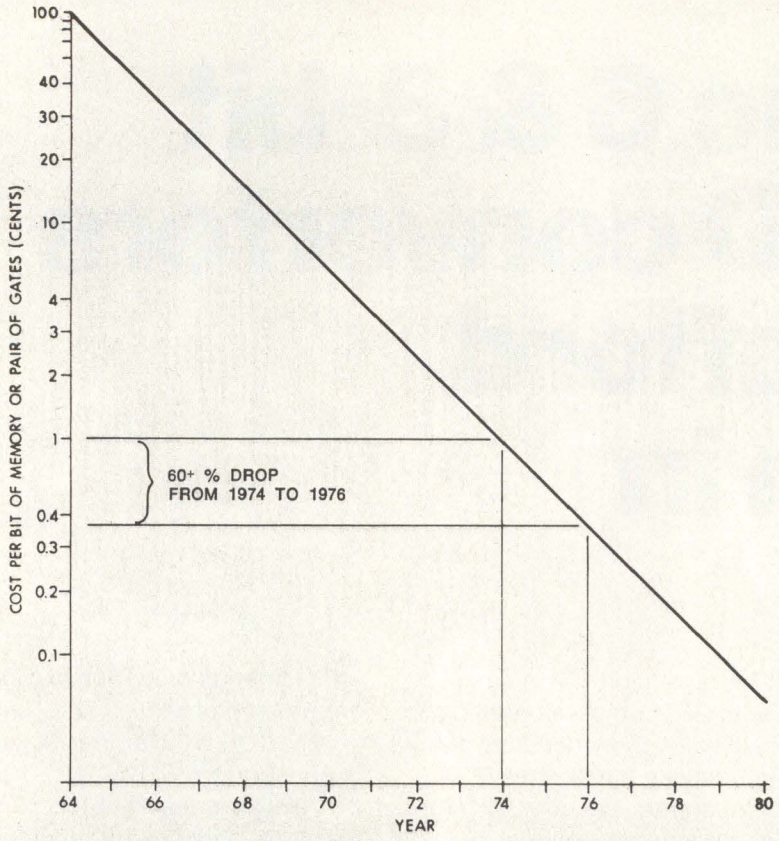

Fig 1 Cost trends per memory bit or pair of gates

and large scale integration (LSI) have brought further reductions in cost and size, and work has begun on very large scale integration (VLSI).

A classic paper by Oliver, Pierce, and Shannon in 1948, "The Philosophy of PCM," acted as a catalyst in spurring development work on PCM.[3] The authors pointed out that in PCM the principle of regeneration, only possible with digital transmission, is the payoff. The pulse train is regenerated at regular intervals before noise, distortion, and other forms of interference are sufficient to cause excessive error rates.

Fig 2 shows regeneration distances for five different digital transmission systems. In Fig 2(a), which is only of historical interest, the early telegraph circuit used heavy wire of sufficiently low resistance to maximize the repeater distance. The limit was reached when the dc arriving at the repeater point was just strong enough to activate a sounder so that a man located at that point could act as the regenerative repeater. Repeater spacing was between 250 and 300 mi (400 and 480 km), and voltages in the order of ±300 Vdc were used. The large amount of redundancy in the English language revealed by C. E. Shannon in his concept of information theory[4] allowed human regenerators to do both forward error correction (FEC) and repeat request (RQ) to correct errors caused by the sending operator, or by interference on the line. Later, man was replaced by the telegraph relay which reacted to the small current arriving at the end of one repeater link and applied voltage to the next.

In Fig 2(b) the regenerator distance is slightly greater than 1 mi (1.6 km) for the T1 carrier PCM system. This carries 24 high quality voice channels or digital data on a 1.544M-bit/s bipolar pulse train. Fig 2(c) shows the typical present day regeneration distance of about 4 mi (6.4 km) for an optical fiber transmission system at the DS-3 level of the digital hierarchy, which is 44.736M bits/s. (The North American digital hierarchy is shown in the Table.)

As shown in Fig 2(d), regeneration distance for digital transmission via satellite is about 45,000 mi (72,000 km.)

North American Digital Hierarchy

Level	Bit/s Rate	No Time Slots
DS-0	64K	1
DS-1	1.544M	24
DS-1C	3.152M	48
DS-2	6.312M	96
DS-3	44.736M	672
DS-4	274.176M	4032

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He'd go right to that 35-pound catalog under the philodendron.

A CRT stand?
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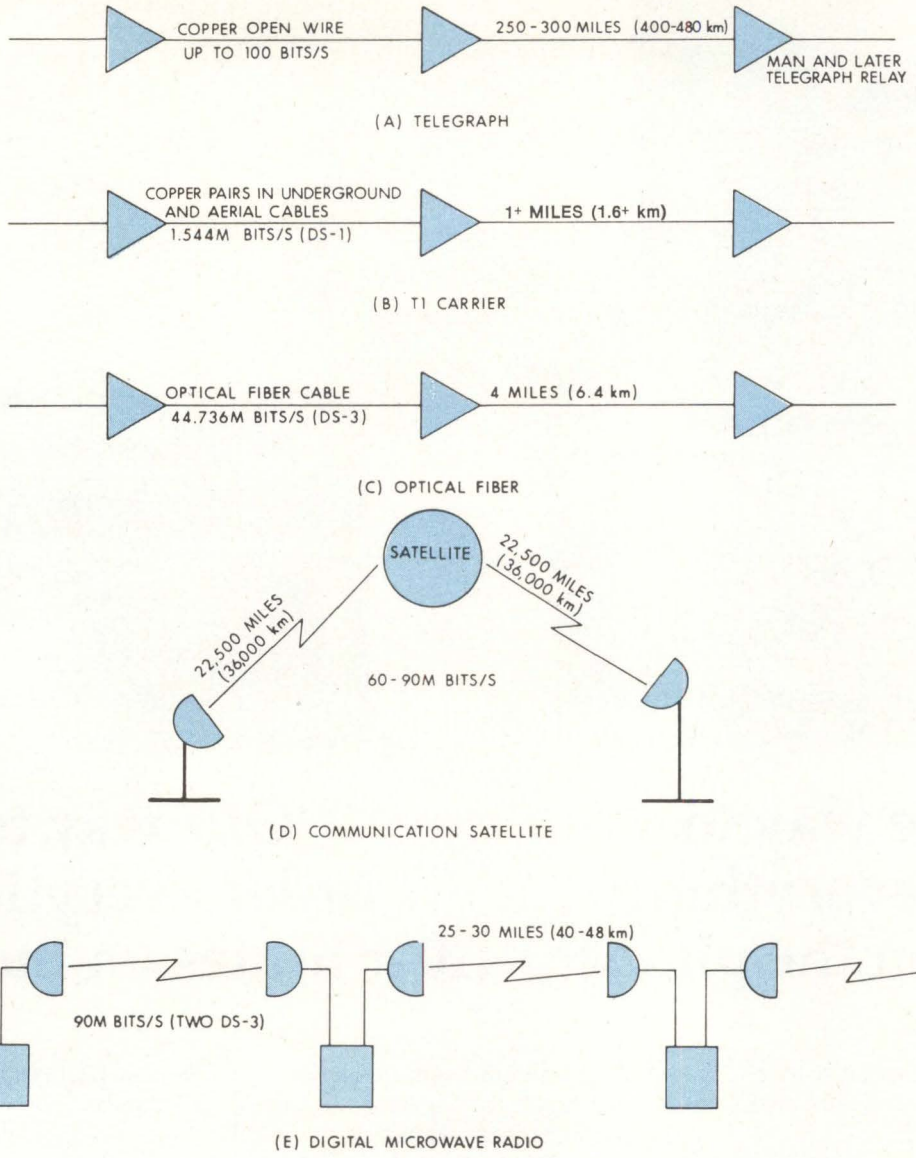

Fig 2 Repeater distances for various digital transmission systems

It might be possible some day to regenerate in the satellite itself and thus cut this distance in half. Recent technical articles have indicated that such a step would provide an advantage of somewhere between 3 and 5 dB. Fig 2(e) shows the regeneration distance for a typical digital microwave radio, such as the 6-GHz, 90M-bit/s system recently installed in the Washington, DC area.

All the digital systems shown in Fig 2 are fundamentally the same. Discrete messages are transmitted as far as the medium will permit, and regenerated before noise and distortion produce errors at an unacceptable rate. Another important advantage of digital transmission is that it can be made truly secure, whether the security involved is military or commercial. Likewise, designers of computers, terminal equipment, and voiceband modems are familiar with various types of degradation that occur on an analog network, such as dropouts, phase and amplitude hits, intermodulation, crosstalk, fading, and impulse noise. On a digital network these are replaced by a few less troublesome degradations such as bit errors, jitter, quantization noise, and short breaks due to temporary lack of synchronization, which are very rare.

Short haul PCM on cable is growing rapidly in North America, Europe, and Japan. In many places, it has captured anywhere from 30 to 80% of the market. This has occurred because it was more cost effective than the competing FDM analog system which in North America was N carrier. As production quantities grew and as the cost of digital logic and memory fell, it was able to penetrate the market more and more. To illustrate the point, if all the T1 line currently installed in the U.S. alone were put end to end it would reach to the moon and back four times, ie, 2 million mi (3.2 million km). Today a PCM terminal VF channel end costs about one-half to one-third of the cost of an FDM VF channel end. There will be about 300,000 PCM channel banks installed in the U.S. by the end of 1979.

The development of PCM digital switching was started

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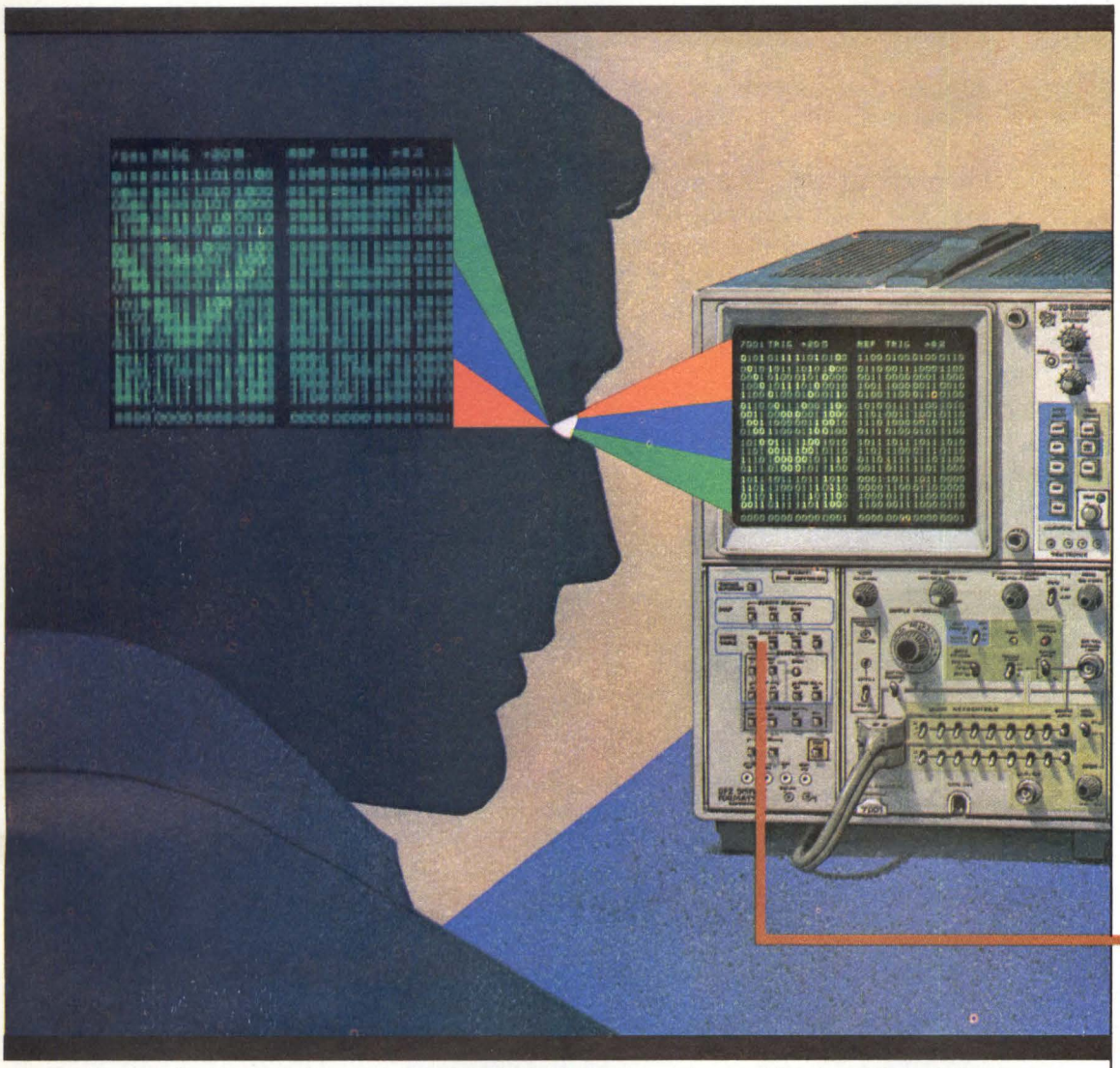

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The outcome was actually two models. The HP 2621A, which sells for $1450. And the HP 2621P, which has a built-in printer, costs $2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

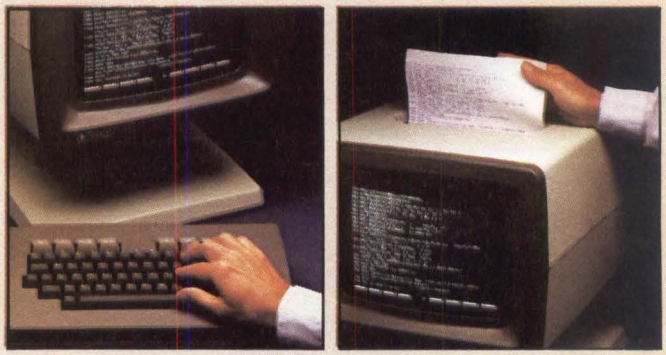
We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.



Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

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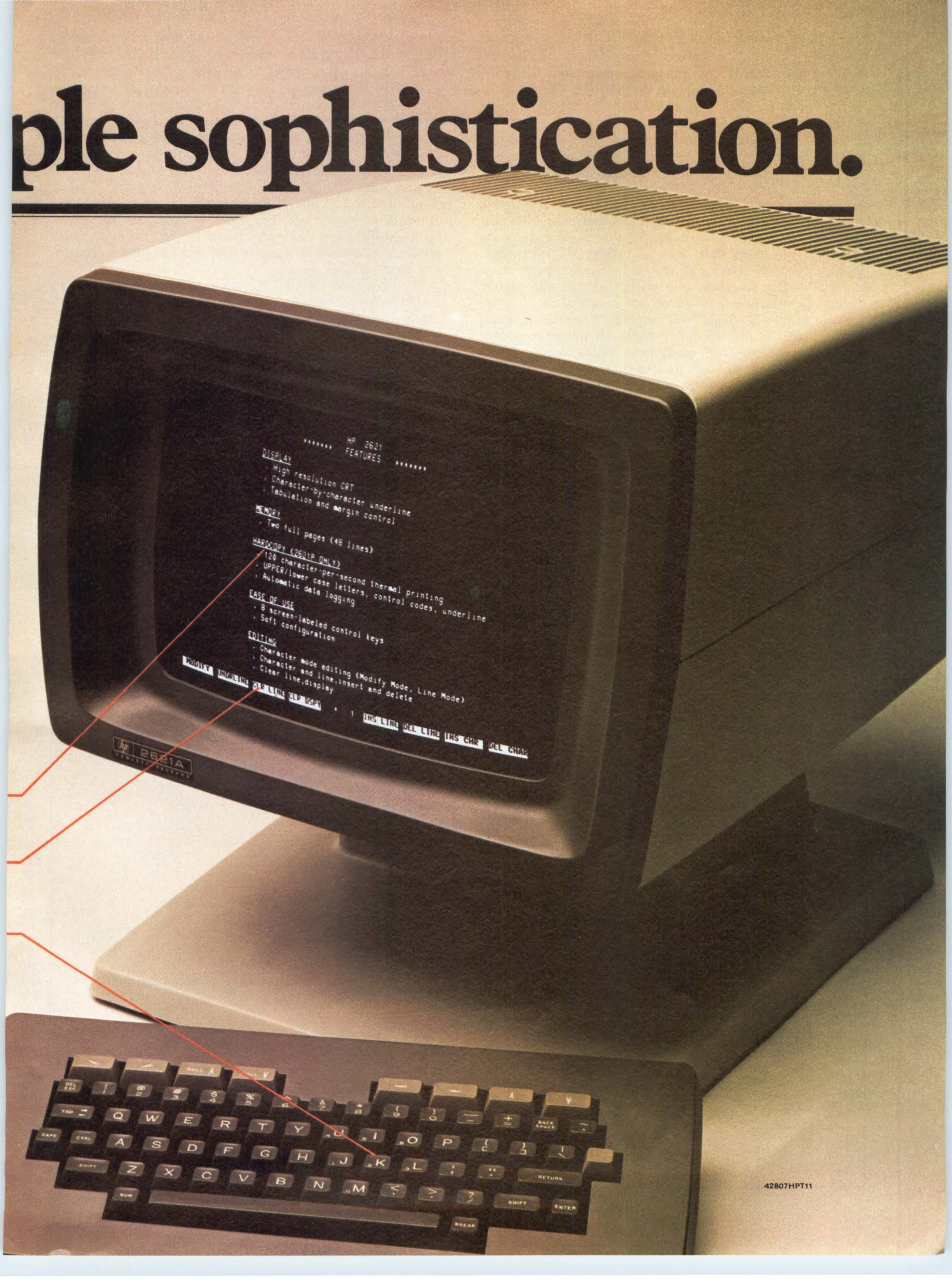

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in France in the mid-1960s. Their first installation occurred in Lannion, Brittany in 1970, and since then the number of switches in service in France has continued to grow. In 1976, PCM digital switching appeared on the scene in the U.S. when the Bell System installed its first No. 4 ESS machine in Chicago. By the end of 1979, Bell will have 34 such machines in service. The No 4 ESS, called a super switcher because it is the biggest switch ever developed, has 107,000 terminations. Key ingredient in a PCM digital switch is the time slot interchange of 8-bit bytes which can be PCM samples of voice or digital data or digital facsimile, etc. Thus, bytes from incoming PCM lines are transferred to time slots on outgoing PCM lines under control of a processor that, in the newest digital switch designs, normally consists of one or more microprocessors. In most digital switches, two paths through the matrix are set up to handle both directions of a call.

No new central office (CO) analog switches are being designed at the present time, while all major manufacturers of CO switching equipment either have digital switches (Class 4, Class 5, and Class 4/5) in production or in development. This is an example of a remarkably rapid acceptance of a new concept. However, it happened because PCM digital transmission had become ubiquitous and because a PCM digital switch uses the same digital logic and memory components as do computers.

The combination of digital transmission and digital switching is an ideal marriage and is called an integrated digital network (IDN). Channel banks are eliminated when two digital switches are directly connected to each other via digital transmission with cost savings that prove-in more digital transmission. The process feeds on itself, producing increasing savings until the network is totally digital. The IDN requires two other ingredients that are network synchronization and common channel signaling. Of the several approaches to achieve network synchronization master-slave is the most commonly used technique. A very precise master clock, usually an atomic standard located near the geographic center of the network, is distributed to the rest of the network by an overlaid tree network. At each node, this clock is used as a reference for a local clock which can survive for several days without drifting enough to cause a slip, if it loses the reference due to a network outage.

With common channel signaling, the signaling information is removed from its present association with the voice channel to which it pertains. Instead, it is carried over a separate signaling data link network which may or may not be routed differently from the information channels themselves. This leads to many additional network advantages including cost savings and additional flexibility for providing new services. One example is the ability to display the calling party number to the called party; another is the ability to insure that voice or data calls do not traverse more than one satellite hop.

The trend to digital is impacting each type of transmission medium and each type of switch in the network. Cable pairs used for local distribution and medium

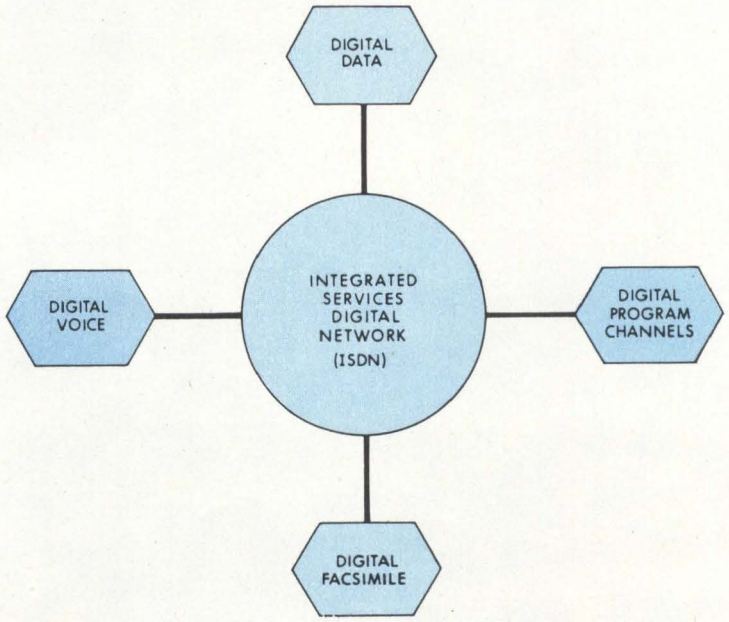

Fig 3 Model of the integrated services digital network

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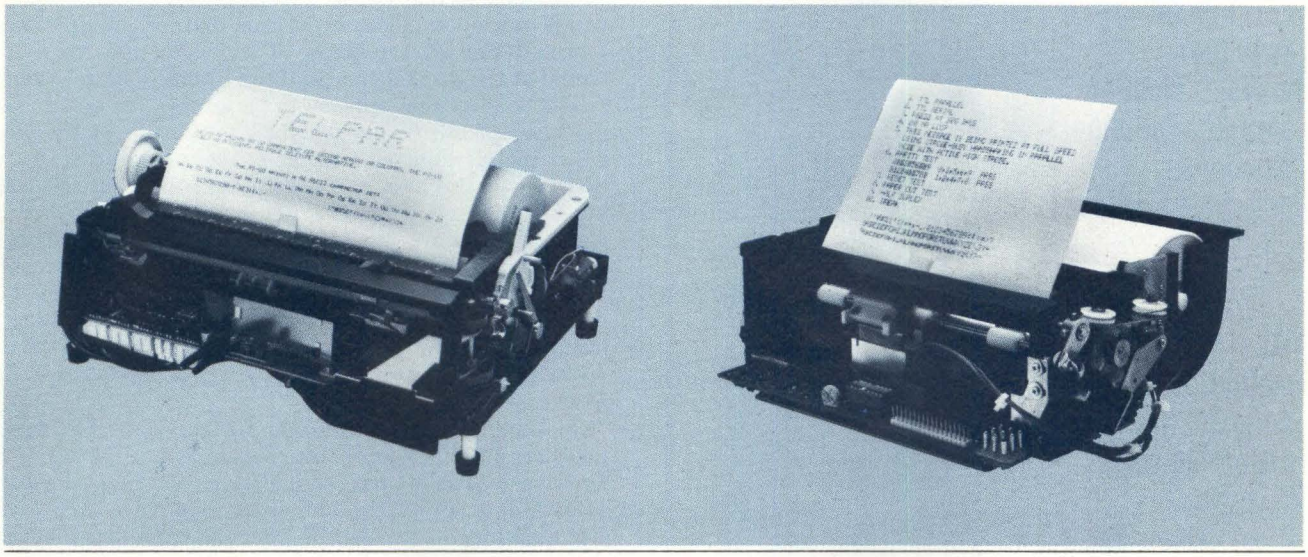

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CIRCLE 15 ON INQUIRY CARD

distances up to 500 mi (800 km) are already heavily digital and will be totally so in the future. Coaxial cables are already being replaced by optical fiber cables because they have the required bandwidth and are more cost effective. Optical fiber cables are here now and are getting more cost effective by the month. They are inherently more attractive for digital transmission because lasers are nonlinear and analog signals can only be carried for short distances. For long haul heavy route transmission, all signs point to digital transmission becoming dominant on satellites in the near future because of the higher bandwidth utilization efficiency of time division multiple access (TDMA). For all categories of switching the trend is to digital at the present time and the future is entirely digital.

The country that appears to be leading the race to have the first nationwide IDN for voice is Canada. It has recognized the advantages and, in effect, made an IDN a national goal. Business profits can result because the building blocks needed for the IDN can be sold all over the world if they are already being built and tested in an actual network. In Canada, the last remaining obstacle to an IDN, which are cost effective long-haul digital facilities, has been recently surmounted. To this end they are installing 90M-bit/s digital radio from coast to coast and are also planning for 90M-bit/s transponders on their new Anik C satellites.

In the future, there is one further step that can be taken and it will probably occur first, once again, in Canada. It is called the integrated services digital network (ISDN). It is an IDN which carries more than one service. For example, an IDN can be built for voice and then have data, facsimile, program channels, etc, added later, as shown in Fig 3. When the second service is added it becomes an ISDN because the same integrated switching and transmission facilities are being used to provide both services. The basic element of the ISDN is a time slot which contains an 8-bit byte occurring 8000 times/s. Therefore, a time slot has an equivalent capacity of 64k bits/s. Some services can use a single time slot such as voice, data at rates up to 56k bits/s, and facsimile at rates up to 56k bits/s. Other services will require multiple time slots such as 5-, 8-, 10-, and 15-kHz program channels, data at rates above 56k bits/s, and facsimile at rates above 56k bits/s such as would be needed for the high resolution transmission of newspaper pages.

In summary, the earliest long distance communications used the digital mode starting with non-electrical means followed by telegraph. Even wireless communications in the early 1900s used the digital mode; ie, a carrier was turned on and off to send Morse code. When the telephone network grew, the analog mode was preferred, until recently. Now the pendulum has swung back toward the digital mode and the full cycle will soon be completed with the appearance around the world of integrated services digital networks in the decade of the 80s. Voice, data, and facsimile services and features which have not been possible heretofore will be available. Switched data services at a variety of bit rates will be made available with fast connect time, high performance, high availability, and low cost. The digital world will indeed be filled with attractive, cost effective, and innovative services and features.

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4. C. E. Shannon, "A Mathematical Theory of Communication," *Bell System Technical Journal*, Oct 1948, pp 623-656

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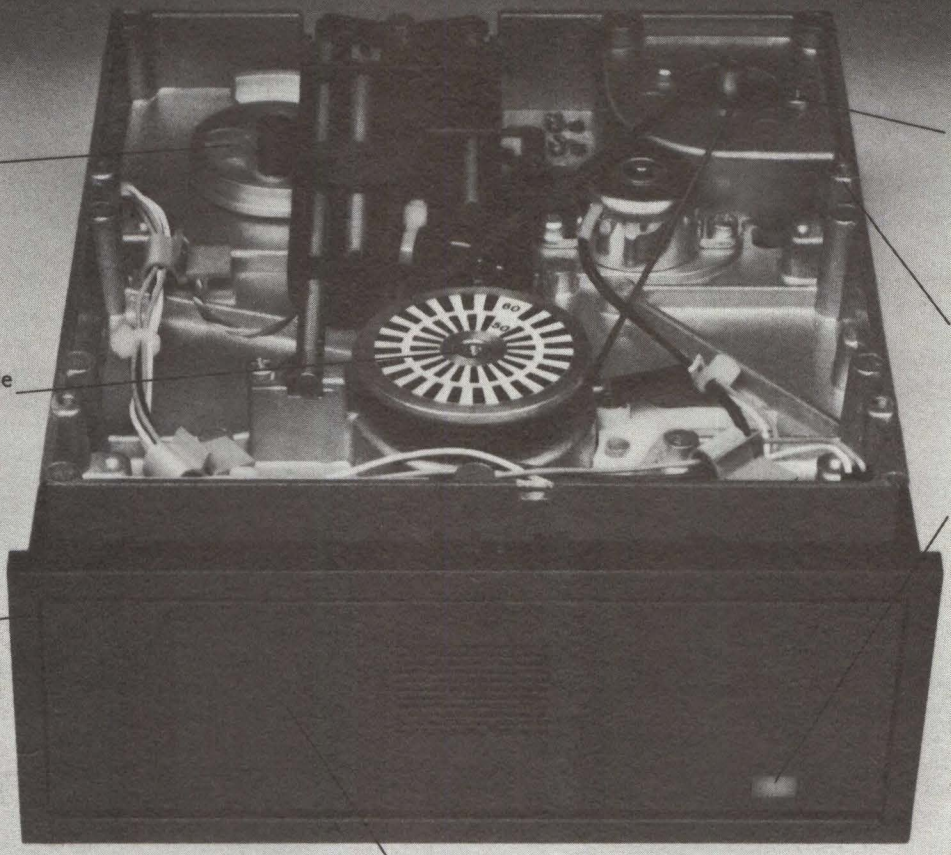

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Intelligence and Sophistication Mark Product Displays at Interface '79

Data communications products shown during Interface '79, McCormick Place, Chicago, April 9-12, 1979, were notable for increasingly sophisticated technology, and for the application of intelligence via the ubiquitous microprocessor to a growing number of systems and equipments. In the space available here we can but skim the surface of the total exhibition. In fact, many of the products shown have already been treated in recent issues of *Computer Design*, the May NCC issue in particular. So we are presenting below nutshell descriptions of some items we feel might be of particular interest.

Readers who wish detailed information on any of the products described may write to the companies directly, or circle the associated reader service number(s).

The NCS-100 network control system by Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22314 (Circle No 400), is actually a family of central site tech control facilities using modules for patching, switching, and testing. Modular design allows future expansion as well as the ability to assemble modules to meet the exact needs of differing applications. Designed for the computer center environment, the system identifies and corrects data transmission malfunctions and enables fingertip control of virtually any size network. Trend and alarm information is also provided for preventive maintenance before actual failure.

Elements of this tech control system include: Datapatch series of modules for facilitating access to data lines; modules for fallback switching ranging from manual A/B devices to computer or touch tone controlled RS-232/V.24 circuit or group switching; a line of digital and analog monitors and interactive testers; and associated cables and components.

A pair of fiberoptic digital transmitter and receiver modules, CTM-100 and CRM-100 respectively, were shown by Canoga Data Systems, 6740 Eton Ave, Canoga Park, CA 91303 (Circle No 401). They feature data speeds of 0 to 2M bits/s NRZ over a single fiberoptic channel, integral optical port connectors, and external clock input/output for synchronous transmission. Both units are in low profile PCB mountable packages to fit 0.5" (1.27-cm) card rack spacing.

Transmitter uses an IR LED emitter for typical output power to connector of 70 μW (−11.5 dBm). Output wavelength is 900 ±25 nm, with typical numerical aperture of 48. Supply voltage is 5 V at 170 mA max.

Receiver module uses a PIN diode detector with a min sensitivity of −30 dBm for 10^{-9} BER. Supply requirements are −6 V at 30 mA, 5 V at 80 mA, and 12 V at 10 mA.

Integral optical port connectors on both units alleviate problem of light source to fiber alignment. Together the modules offer 500-m data link capabilities and functional link monitor and test when used with appropriate cable/connector assemblies.

Among the products shown by Codex Corp, 20 Cabot Blvd, Mansfield, MA 02048 (Circle No 402), was the distributed network control system (DNCS) which provides constant monitoring of network performance, indication of device malfunction, and the means to restore network operation from a central site. The system combines a multi microprocessor based distributed network processor (DNP) that supports simultaneous and continuous network monitoring with distributed network terminal (DNT). DNT comprises an intelligent CRT terminal, printer, and floppy disc, and acts as the operator interface. All executed programs, network configuration, and parameter data are stored on a dual floppy disc. Network management is done via the independent secondary channel of master and remote modems. This channel is frequency division multiplexed with the main channel using a standard protocol.

Terminal port cards in the network controller allow for line expansion. One to four port nest configurations support up to 124 central site lines and 64 drops/line. A simple English command set eases entry of line and device related data. Desired threshold parameters to be monitored can be entered and modified as network conditions require. Threshold exceed conditions are immediately reported and logged by the printer. A complete advanced repertoire of modem and line testing to isolate problems as well as to provide restoration capability is available. Modems that operate with DNCS with optional control card include the MX 2400 series and the LSI "fast poll" series for multipoint and point to point operation at 4800, 7200, and 9600 bits/s.

Distributed network control system. DNP with four series LSI48FPX modems and DNT operator workstation with CRT, printer, and floppy disc package

---

Model Ei 310, called Epibert, is a rack mountable bit error rate tester that will exercise, test, and evaluate modems, total data systems, digital microwave links, and digital data networks. Available from Epicom, Inc, 592 N Douglas Ave, Altamonte Springs, FL 32701 (Circle No 403), it operates with both synchronous and asynchronous systems in simplex, half, or full-duplex at rates to 100k bits/s. The unit can simultaneously display bit and block errors, block count, RTS/CTS delay, loop delay,

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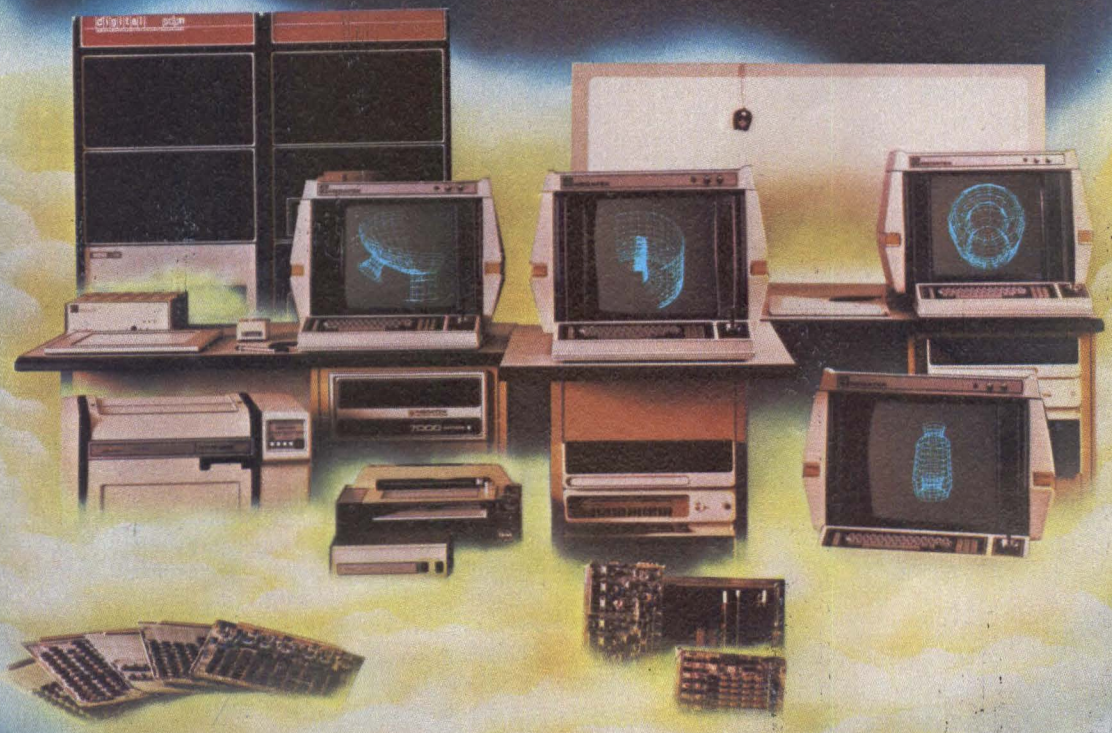

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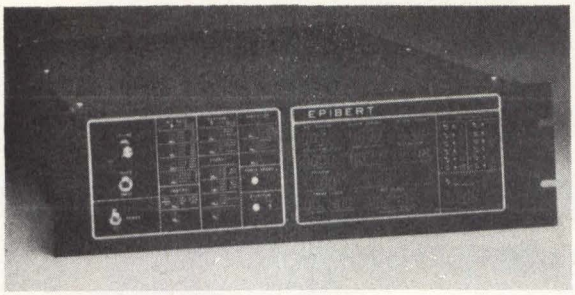
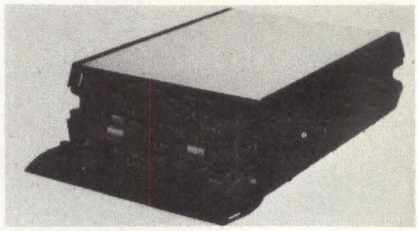


Epibert bit error rate tester. Claimed to have largest display capability of any currently available test set, it can simultaneously display ten line measurements and test parameters

percent distortion, telco dB, transmit and receive clock rate, and dc voltage. Choice of pattern setup includes continuous mark, continuous space, mark/space alternating, incrementing binary, and pseudorandom sequences.

An attention-getting device was the SM 9600 full-duplex synchronous intelligent modem. Called superModem by the manufacturer, Gandalf Data, Inc, 1019 S. Noel, Wheeling, IL 60090 (Circle No 404), it handles 9600-bit/s data over 3002 unconditioned voiceband data channels; no equalization is required. Performance includes BER, 10^{-6} at S/N of 26 dB in the presence of 5 Hz frequency translation; impulse noise tolerance of 4 dB below rms signal; and ±7 Hz frequency translation. Performance of the SM 9600 is achieved by the transmitter simultaneously generating a large number of discrete carriers, and modulating each to represent only a portion of the total data stream. The composite signal has the desired low baud rate for good noise immunity, and allows time for envelope delay effects to pass. At the receiver, each carrier is independently demodulated and its data are combined with data from the others to reconstruct the original data stream.



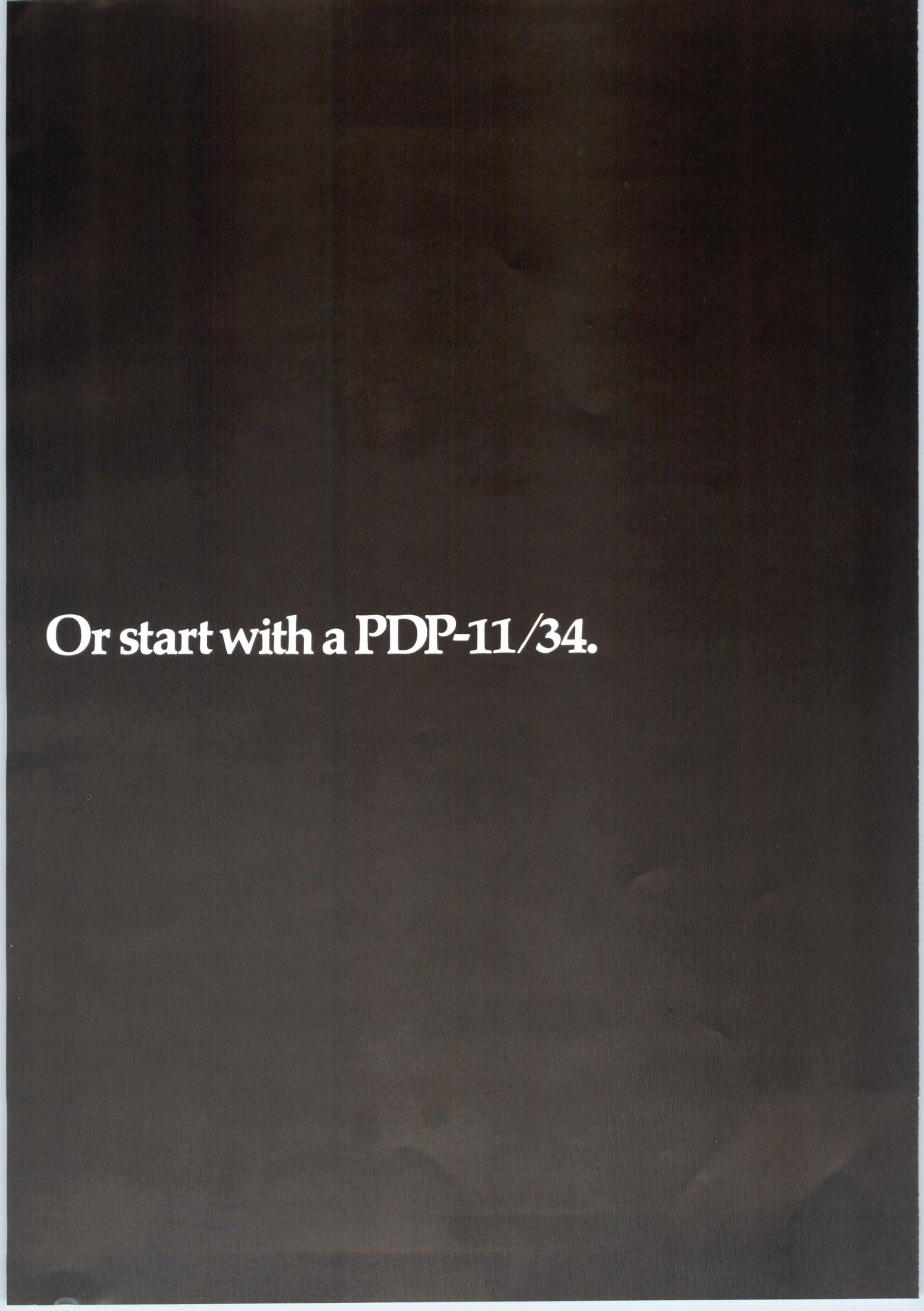
SM-9600 modem, front panel open. From bottom to top: program ROM, 24-bit processor, and I/O modules for data and voice frequency interface

Heart of the unit is a proprietary 24-bit digital processor whose pipeline architecture enables an operating speed of 10M instructions/s. It digitally generates the transmit signal, filters and extracts the data from the receive signal, and controls all the I/O functions. The processor is also used to analyze circuit parameters while online, and perform routine diagnostics.

Operating instructions for the processor are resident in ROM. The program is built around algorithms which perform realtime analysis of the receive signal using discrete

There are only two ways for an OEM to design a mid-range computer system that precisely fits each application.


digital
pdp11/34
ADDRS
DATA
RUN
DIS AD
EXAM
DEP
H.LT/SS
DC ON
BATT
SR DISP
LAD
CONT
DC OFF
DC ON
STD BY
BUS ERR
LSR
BOOT
MAINT
CLR
INIT
CNTRL
START


Or start with a PDP-11/34.

If you don't need all the capability of RSX-11M, the beauty of the 11/34 is you don't have to get it. You can get RSX-11S instead. It offers you the same multi-task, event-driven real-time capability without the overhead of interactive program development.

And if your application calls for real-time, but doesn't call for multi-programming, you can call on RT-11. It's a single user foreground-background system that's designed for both program development and dedicated, on-line applications.

For timesharing applications, Digital offers RSTS/E—a powerful, flexible system that can handle up to 16 different users on an 11/34 at one time.

Then there are all the languages. Depending on your application and operating system, you can choose BASIC, Multi-User BASIC, MACRO-11, COBOL, DIBOL-11 (Digital's business/commercial language), FORTRAN, APL, RPG and FOCAL, with still more languages in development.

And finally, you have available an extensive library of applications software. You can pick and choose the exact OEM software tools that make the most of your hardware. And your application.

Then do what you want with your system.

With the PDP-11/34, you can vary your system according to the requirements of your customers. You can offer a wide range of terminals, peripherals and communications packages. You can make fine adjustments in design and manufacture.

In short, you can turn more good prospects into good customers simply by adapting to their individual needs. And you can do it without incurring the major losses in time and money that are involved when you design the complete system yourself.

The PDP-11/34 opens up a new world of flexibility in manufacturing and marketing your products.

It also opens up a new world of applications flexibility. With all its options, the 11/34 is ideally suited for applications involving instrument interfacing. And with all its programming tools, it's ideally suited for applications involving program development. The PDP-11/34 even gives you the flexibility to link your system with any other Digital system anywhere in the world through DECnet networking software. And that means you can offer your customers the benefits of distributed data processing using the broadest range of upwardly compatible systems anywhere.

The PDP-11/34. If you designed your computer from scratch, you wouldn't come up with a more precise mid-range system for your application.

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digital

Digital's PDP-11/34 gives you more design flexibility than any other mid-range in the world.

If that sounds like a bold claim, consider this. There are more than a million ways to configure a PDP-11/34 computer system.

That figure is not based on frivolous options, but on significant choices like CPU capabilities, memory options, peripherals, operating systems, languages, communications packages and network systems.

All of these options are in addition to a basic PDP-11/34 that is extremely flexible to begin with. Here are some of its standard features: a 16-bit microprogrammed processor, parity memory, direct memory access, vectored interrupts with four priority levels, hardware stacking, operator's console, multi-function ROM with virtual console capability, diagnostics and bootstraps, memory management, hardware multiply and divide, power fail/auto restart, and prewired slots for expansion options.

With the basic computer so flexible, and the system options so numerous, you can virtually design your own mid-range system with the PDP-11/34. Without having to start from scratch.

Choose the hardware you need.

Take the PDP-11/34 CPU, for example. You can pick and choose among 21 CPU options for the precise combination you want. The 11/34 offers a new superfast cache that makes a powerful system even more powerful. It can increase your program execution speeds by as much as 60%. Other options include a fast floating point processor, serial communications line interface, and real-time clock, to name just a few.

You can also choose from twelve memory options, including MOS, core or any combination. Digital's MOS memory uses industry-standard 16K RAM chips with a 500ns cycle time. And it's available on 128Kb or 256Kb boards.

Of course, there's more to a system than a CPU. And the 11/34 offers more.

You can choose from 6 disks, 4 tapes, 10 terminals, 8 printers, 6 card readers, and 9 kinds of I/O. Plus 10 different kinds of communications options that cover the broadest range of devices in the industry.

You can even pick your packaging, because the PDP-11/34 comes in eight models with two battery back-up choices and five different backplanes.

Given all these options, you can configure the perfect combination of hardware for your application. Without paying for more power than you need, or settling for less.

Choose from four operating systems and ten languages.

Even with the precise hardware in place, you're still only halfway to the precise system for your application. The software options of the PDP-11/34 will take you the rest of the way.

For real-time applications, there's RSX-11M. It's specifically designed for multi-programming and concurrent program development. And it offers you the power of an event-driven software system with dynamic memory management, multiple programming languages and a complete list of utilities.

The PDP-11/34.
Just look at the freedom it gives you.

Packaged systems*

11/34A CPU with 64Kb MOS memory, 1Mb disk storage, video or hardcopy terminal, RT-11 operating system.

11/34A CPU with 128Kb MOS memory, 10Mb disk storage, video or hardcopy terminal, RSX-11M operating system.

11/34A CPU with 128Kb MOS memory, 56Mb disk storage, video or hardcopy terminal, RSX-11M operating system.

11/34A CPU with 256Kb MOS memory, 67Mb disk storage, 9 track/45ips tape, video or hardcopy terminal, RSX-11M operating system.

*In some cases, available with other operating systems, less memory, and with core instead of MOS.

CPU configurations

MOS memory of 256Kb, 128Kb, 64Kb and 32Kb.

Core memory of 128Kb, 64Kb and 32Kb.

Optional cache memory.

Optional programmer's panel and serial line interface.

Optional floating point processor.

Optional MOS battery back-up.

Software

RSX-11M multi-user, multi-tasking operating system featuring program checkpointing, dynamic partitioning, and memory management.

RSX-11S execute-only operating system for monitoring and controlling multiple real-time processors.

RT-11 real-time, foreground/background operating system.

RSTS/E timesharing operating system.

DECNET II distributed data processing networking package.

FMS-11 forms generation software.

DATATRIEVE-11 data inquiry and report writing system.

DBMS data base management system.

RMS-11 record management system supporting ISAM, sequential, and random access file structures.

SORT-11 for re-ordering data based on key fields in the data record.

Languages

FORTRAN IV	BASIC PLUS	APL
FORTRAN IV+	BASIC+2	MACRO 11
BASIC	COBOL	CORAL 66
	DIBOL	

Memory

MOS memory modules of 256Kb, 128Kb, 64Kb, 32Kb and 16Kb.

Core memory modules of 64Kb, 32Kb and 16Kb.

Disks

RX02 1.0Mb, dual drive (diskette).

RL01 5.2Mb, removable.

RK07 28Mb, removable.

RM02 67Mb, removable.

RP05 88Mb, removable.

RP06 176Mb, removable.

Special I/O

IEEE interface with software.

Industrial control remote sub-system.

Industrial control master sub-system.

D/A control.

12 bit A/D converter, 16 channels.

48 channel multiplexer.

10 bit A/D converter, 16 channels.

Parallel I/O with direct memory access.

16-bit parallel I/O, program controlled.

Communications options

Full/half duplex synchronous interface for both byte and bit oriented protocols.

Full/half duplex synchronous interface for byte oriented protocols.

Full/half duplex NPR synchronous interface.

Network link, local or remote, DDCMP up to 1Mb.

Asynchronous 8 and 16 line multiplexer.

Programmable 16 line asynchronous multiplexer.

Synchronous/asynchronous 16 line multiplexer.

16 line modem control multiplexer.

360/370 channel interface.

Asynchronous serial line unit, with or without modem controls.

Tapes

TE16 800/1600bpi, 45ips, ½" magtape.

TU45 800/1600bpi, 75ips, ½" magtape.

TU77 800/1600bpi, 125ips, ½" magtape.

TU58 800bpi, ¼" cassette.

Video terminals

VT-100 video terminal, 80 or 132 columns, with extensive video attributes and detachable keyboard.

VT-52 video terminal.

VT-55 graphics terminal.

VT-62 block mode terminal.

VT-61 editing terminal.

Hardcopy terminals

LA-120 "smart," 120cps hardcopy terminal.

LA-38 hardcopy terminal, 30cps, with tractor feed, with or without stand.

LA-34 hardcopy terminal, 30cps, with roll paper feed, with or without stand.

LA-36 hardcopy terminal, 30cps, on stand.

LA-37 APL, hardcopy terminal, 30cps, on stand.

Optional cabinetry

10½" expander box.

5¼" expander box.

Cabinet with power control.

Short cabinet with power control.

digital

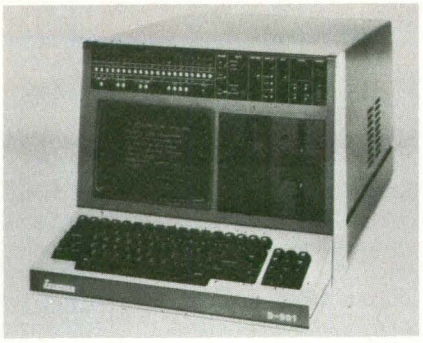
Fourier transforms to accomplish filtering and data demodulation.

An I/O control module controls the VF and data interfaces under processor direction. Standard data interface operates at 9600 bits/s and all signals meet RS-232-C and CCITT V.24 requirements. An optional 4-channel multiplexer may be configured from the front panel for all normal channel speed combinations.

Another intelligent unit, the 610 port selector, was unveiled by Micom Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311 (Circle No 405). Designed primarily for users with multiple minicomputers, the selector allows automatic contention for the computer port attached to it by users connected either directly or via dial-up or dedicated modems. Port class may be selected: either all the ports on a particular computer, or those supporting a particular application or type of terminal. If a selected port is not available, the 610 will advise the reason, set up a queue, advise how many terminals are ahead, and send a "go" message when the connection is available. Any asynchronous terminal may be connected. An Autobaud feature provides automatic terminal speed detection to 4800 bits/s. Unit is available in table top configuration for single minicomputer installations, and in a floor standing model for installations supporting several hundred port and terminal connections.

Newest member of the Datascope family of monitors and data analyzers, the D-901 was introduced by Spectron Corp, 344 New Albany Rd, Moorestown, NJ 08057 (Circle No 406). The unit can monitor and analyze incoming data at speeds up to 1.6M bits/s and can store data along with selected control signals at speeds to 72k bits/s under manual or program control. Data stream can be displayed and frozen on the 9" (22.8-cm) CRT. Prompting messages simplify program entry.

A communications oriented compiler-level language enables programming of a wide variety of diagnostic tests and emulation routines. All instructions are entered from the keyboard. Of two integral floppy drives, the data diskette records data and status of up to eight control signals, and system diskette stores user programs, system configuration parameters, and operating system. A 4k-char log buffer and separate 4k-char output buffer are standard. The D-901 can be used with the company's remote access switching and patching (RASP) system also introduced at the show, for remote control of multiple sites from a central location.



D-901 Datascope. Unit combines programmable interactive data analyzer with two large capacity data storage and retrieval devices for handling complex network problems

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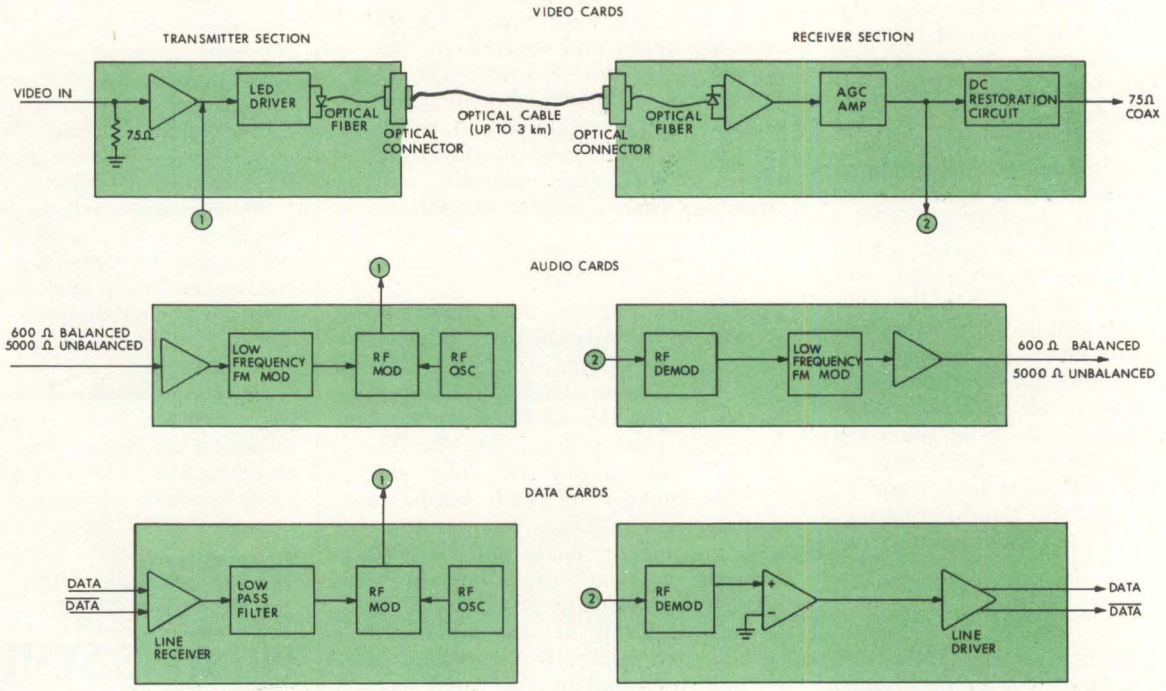
First major product in a new line of proprietary instruments to be manufactured by T-Bar, Inc, 141 Danbury Rd, Wilton, CT 06897 (Circle No 407), the TD-12 microprocessor based data link tester called the Explorer™ was introduced. The unit enables isolation of both hardware and software problems in front ends, modems, and terminals, and can also separate communication line problems from hardware problems. Data circuits operating at any one of 16 speeds from 50 to 19,200 bits/s can be monitored and tested. Tester configurations, options, and commands are keyboard selected; no selector switches are used.

Prompting displays on the integral 5" (12.7-cm) diagonal CRT guide the operator through available options and operating modes. A selective trap and storage capability allows storage and display of only that portion of the data stream suspected of containing a problem. 4k-byte internal memory is standard, with an 8k-byte memory unit available. Adaptable to most data communications environments, the TD-12 allows monitoring, and terminal or computer emulation in networks using any one of a number of different protocols and also provides for bit error rate testing, time and clock measurement, and network efficiency measurement.

A multimedia fiberoptic link, vs-100, that can multiplex voice, data, and baseband video into a single optical signal was announced by Valtec Corp, 99 Hartwell St, W Boylston, MA 01583 (Circle No 408). The link can deliver better than 50 dB S/N video over nearly 3 km of fiber cable without repeaters, and has provisions for adding audio and/or data channels to provide an effective bandwidth up to 250k bits/s. The transmitter converts the multiplexed electrical input into a modulated optical output signal by directly varying the LED light source current. The receiver includes a PIN photodetector, amplifier and demodulation circuits, as well as AGC and dc restoration.

All video link connections are preengineered and EIA RS-170 compatible. Integrated power supply, test points, and fault light indicators are standard.



Simplified block diagram VS-100 link circuitry. Both transmitter and receiver contain power supply, as well as individual video, voice, and data cards, which may be mixed or matched in any combination

MiniMate is an RS232 compatible minifloppy disc storage and edit terminal from Western Telematic, Inc, 2435 S Anne St, Santa Ana, CA 92704 (Circle No 409). It is designed as an attachment to intelligent CRT or printer terminals to replace paper tape, cassette, or mag card units in store and forward applications. The unit includes character edit capability, and can address up to 560 records of 128 chars each, for a working storage of more than 71k chars. Each record is automatically numbered.

The unit can communicate with a host computer in either batch or interactive mode at 8 switch-selectable speeds from 110 to 9600 baud. Access time is 1 s max. Character edit features include backspace/erase, delete, modify, link, and stop. A "go to" command allows jumping to random file locations for repeat and linking applications. Two RS-232 ports allow series connection between any ASCII coded asynchronous printer/display terminal and the modem. □

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Best μP.
Here's why. Its second-generation microprocessor has EPROM capability — real smarts. It gets us from your keyboard concept to a prototype design in record time. It enables completely customized software control of all key functions. You can program in automatic repeats, multiple program a single keyboard, program changes in the field. You can have 8-bit serial and/or parallel I/O. Three-key rollover is built in with N-key rollover possible. There are no compromises and the options are unlimited.

Best of both worlds.
Couple this μP with the unique low-profile reed switches we manufacture and you've got the best of two technologies — an unbeatable keyboard system. You know reed contacts are sealed against hostile environments. You know reeds are extremely dependable and stable. They'll switch faultlessly over 10^8 times. They are low in power consumption. And zero in power drain. Another key point: they've got the feel operators like, so speed and accuracy increase.

Best keytops.
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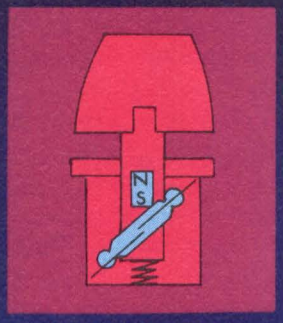


Height with keytop: $1\frac{5}{16}$"

C. P. CLARE & COMPANY
GENERAL INSTRUMENT CORPORATION

CIRCLE 22 ON INQUIRY CARD

Technological leadership.

Most functions on the in systems. The MC6801

Power, speed and the unique design flexibility of multimode operation put Motorola's MC6801 single-chip microcomputer in a class by itself. It's general purpose in application, high in performance and packs more function on the chip. All 'round, it's unequalled.

An unprecedented combination of on-chip functions with the CPU includes 2K bytes of ROM, 128 bytes of RAM, 31 parallel I/O lines, a serial communications I/O port, a clock and a 16-bit programmable timer.

User-selectable operating modes.

Each of the operating and self-test modes is built-in and user-selectable, for either testing or shipping.

In the single-chip mode, all ports are configured for I/O, with a total of 29 I/O and two control lines.

In the expanded non-multiplexed mode, no external logic is required to directly address 256 external locations including any and all M6800 family peripherals. Thirteen to 20 I/O lines are still available.

The expanded multiplexed mode enables an impressive 64K-byte addressing capability.

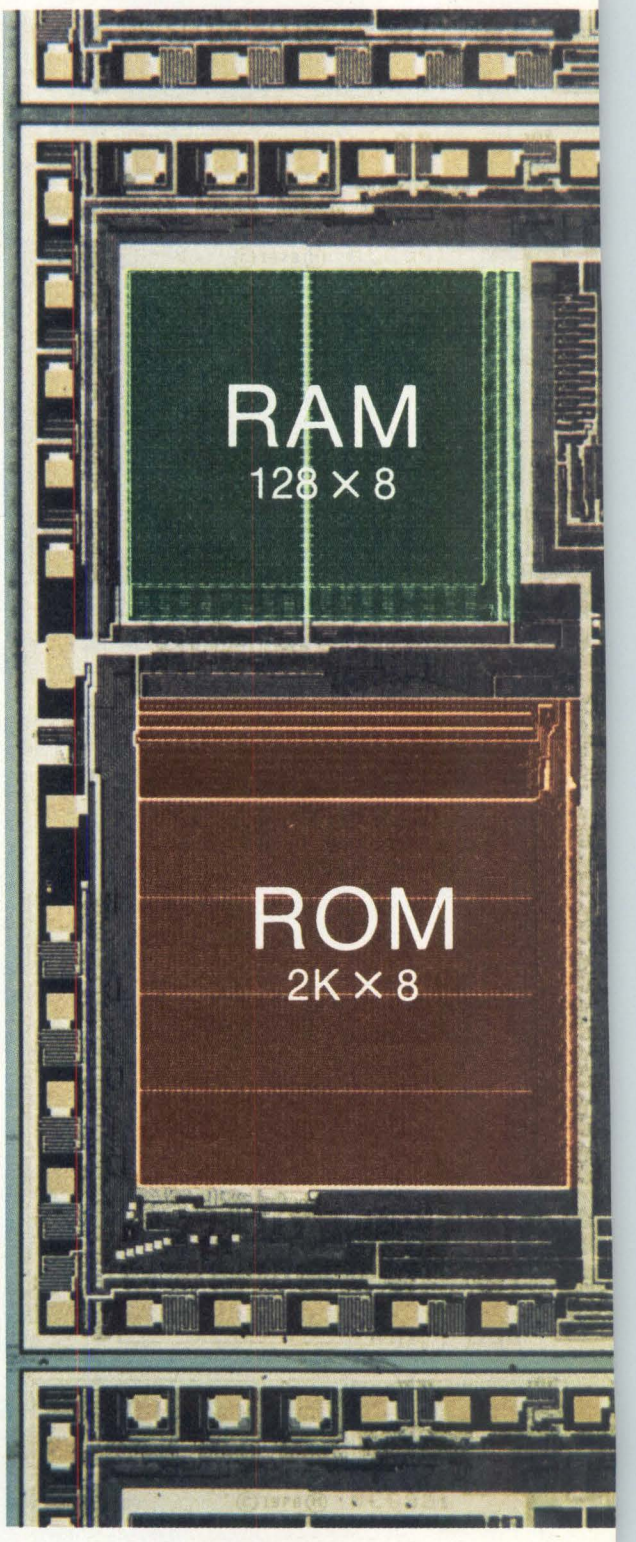
Other modes facilitate testing and other special operations. It's an unparalleled state-of-the-art advance in design convenience. In all of these modes, the on-chip 16-bit timer can count or time events and generate or measure pulses.

The on-chip fully-buffered serial communications interface offers operation at four baud rates—full duplex asynchronous formats. The SCI operates at over 75K baud, and other special features—such as wake-up, NRZ and biphase—promote efficient multi-processor system configuration.

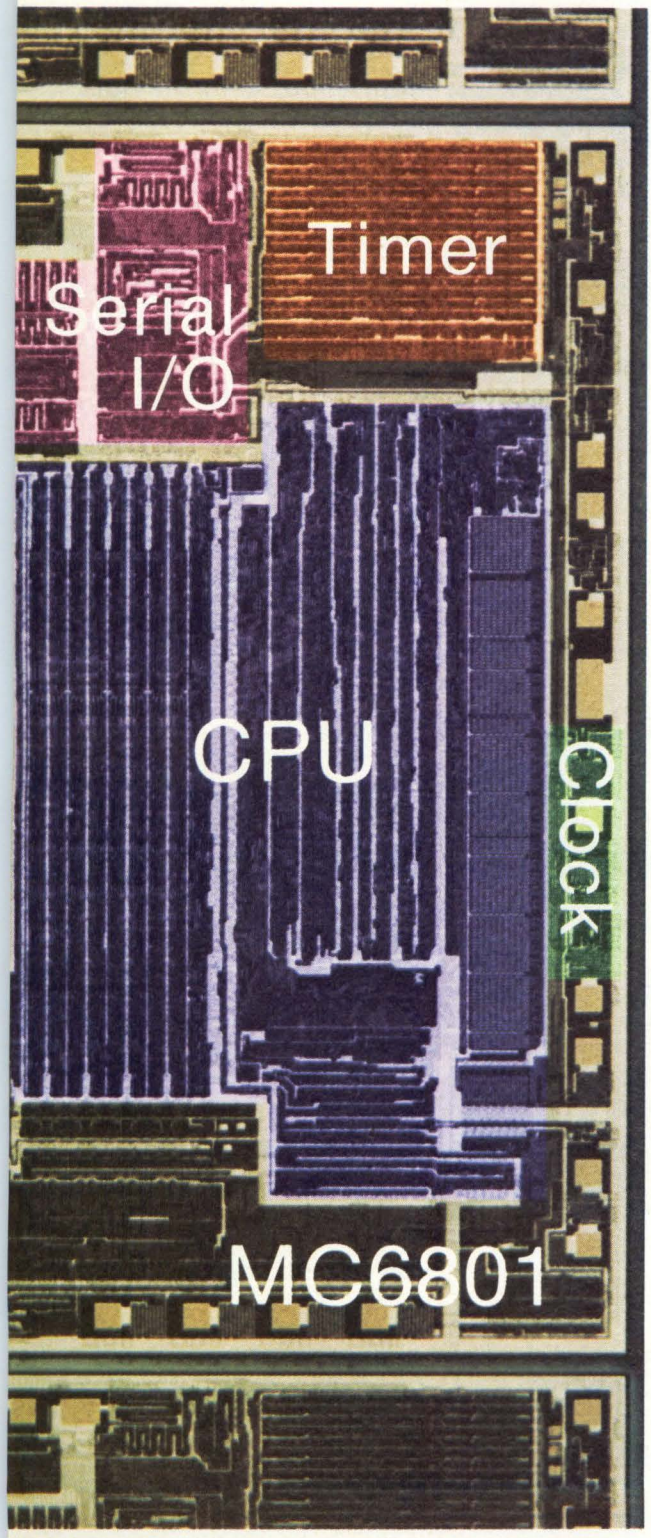
The CPU of the MC6801 is an enhancement of the highly-capable MC6800, which puts seven addressing modes at the designer's disposal. An MC6800 machine code-compatible instruction set is expanded by new 16-bit instructions, including a 10 μs hard-ware multiply. Execution time of most instructions has been reduced to increase throughput.

Gets you to market faster

Compare the MC6801 with any other general-purpose single-chip microcomputer available today for on-board hardware capability, programming ease and system performance. Do whatever benchmarks are appropriate for your application or just take our word for it: the MC6801 can get you to market faster with more aggressive designs.



chip, most performance one-chip microcomputer.



Watch for user-programmable version.

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The world's first high-performance single-chipper with EPROM on board, the MC68701, is an MC6801 with 2K bytes of MCM2716-equivalent EPROM instead of mask-programmable ROM. The MC68701 is ideal for low-volume systems, initial production field test units of a user system, or those which may require reprogramming in the field. It especially aids prototyping because the control program is easily evaluated and changed during development.

Watch for the availability announcement soon.

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Total MC6801 support.

Motorola supports the MC6801 in every way. The entire, fully-compatible M6800 family provides a broad range of microcomponents and memories for system expandability. EXORciser™ development systems and Motorola development software support all M6800 family units, including the MC6801, with real-time emulation capability.

For additional information, contact your Motorola sales office or authorized distributor, write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number.

Motorola's MC6801 is the world's most versatile single-chip microcomputer. It is representative of Motorola's dedication to product excellence in all phases of its discrete and integrated circuit operations supporting the designers and manufacturers of

Innovative systems through silicon.

MOTOROLA INC.

CIRCLE 23 ON INQUIRY CARD

TECHNOLOGY AND ECONOMICS: RELATIONSHIP BETWEEN DIAGNOSTIC PROGRAMS AND MTTR

Montgomery Phister, Jr
Systems Consulting
Santa Monica, California

Diagnostic programs, in software or firmware, serve to detect failures and to identify subassemblies likely to be at fault. A model describes the diagnostic process, relating the customer engineer's mean time to repair to the important characteristics of a diagnostic program. The model identifies design and operating factors that are important in determining equipment mean time to repair and measures the relative importance of each.

Mean time to repair (MTTR) is measured from the time the customer engineer (CE) takes charge at a customer site until the fault is resolved and the equipment is returned to the customer. It includes time required to review symptoms with the customer, run diagnostic programs, locate and repair the fault, wait (if necessary) while parts are delivered from another location, and review the problem solution with the customer. This article considers only diagnostic, location, and repair aspects of this process.

Diagnostic Procedure

The diagnostic process described by Gay* is illustrated in Fig 1. Assume that the diagnostic program has a probability D that it will not detect the fault. This case requires time t_a to effect a cure. If it detects a fault (probability 1 − D), the program generates a list of parts to be replaced in most-likely-first order. When these parts have been replaced and the problem remains (probability $1 - A_m$) a backup procedure is used to locate and repair the fault. Given this model, MTTR can be written as

$$\text{MTTR} = D\,t_a + (1 - D)\,R_m\,t_r + (1 - D)(1 - A_m)\,(M\,t_r + t_b)$$

where R_m is the average number of parts replaced when the fault is cured in the diagnostic cycle, and other terms are as defined in Fig 1. Alternatively

$$\frac{\text{MTTR}}{t_r} = D\,\frac{t_a}{t_r} + (1 - D) \times (\text{Equivalent Diagnostic Cycles}) \qquad (1)$$

where

$$\text{Equivalent Diagnostic Cycles} = \text{EDC} = R_m + (1 - A_m)\left(M + \frac{t_b}{t_r}\right) \qquad (2)$$

To achieve a given MTTR, design procedures to make t_r, t_a, and t_b as small as possible; develop a diagnostic having characteristics D, A_m, and R_m; choose a

*F. A. Gay, "Evaluation of Maintenance Software in Realtime Systems," *IEEE Transactions on Computers,* June 1978, pp 576-582

The NEC Thumbwheel.

Its helpful features make our printers work better for you.

Most printers have a rotary switch that's used to select one of 12 fixed forms lengths. The NEC Spinwriter™ and Trimliner™ printers use two thumbwheel switches.

The thumbwheels do the important extras that make printing easier, faster and more productive. You can dial in 100 forms lengths – from a fraction of an inch to up to 14 inches. Our printers adapt to your forms, rather than your forms adapting to our printers.

The wheels are interactive with the lines-per-inch operator switch or under program control. You can mix six- or eight-LPI spacing with fine-quality plotting (in $^{1}/_{48}$-inch increments) in a single print run, and always return automatically to the right top-of-form. Neat.

NEC's thumbwheels also run diagnostic print sequences on paper of any width. Just dial the desired line length before pressing the test print mode button and full testing is run within the line length selected. Saves wear on platens and print elements, and speeds up your get-ready and job-changing tasks.

A thumbwheel may not be the most exciting part of a printer. But it's important enough that NEC gave it three capabilities no other printer offers.

The 55 CPS Spinwriter and 300-600 LPM Trimliner printers are loaded with features and extras not built into other printers.

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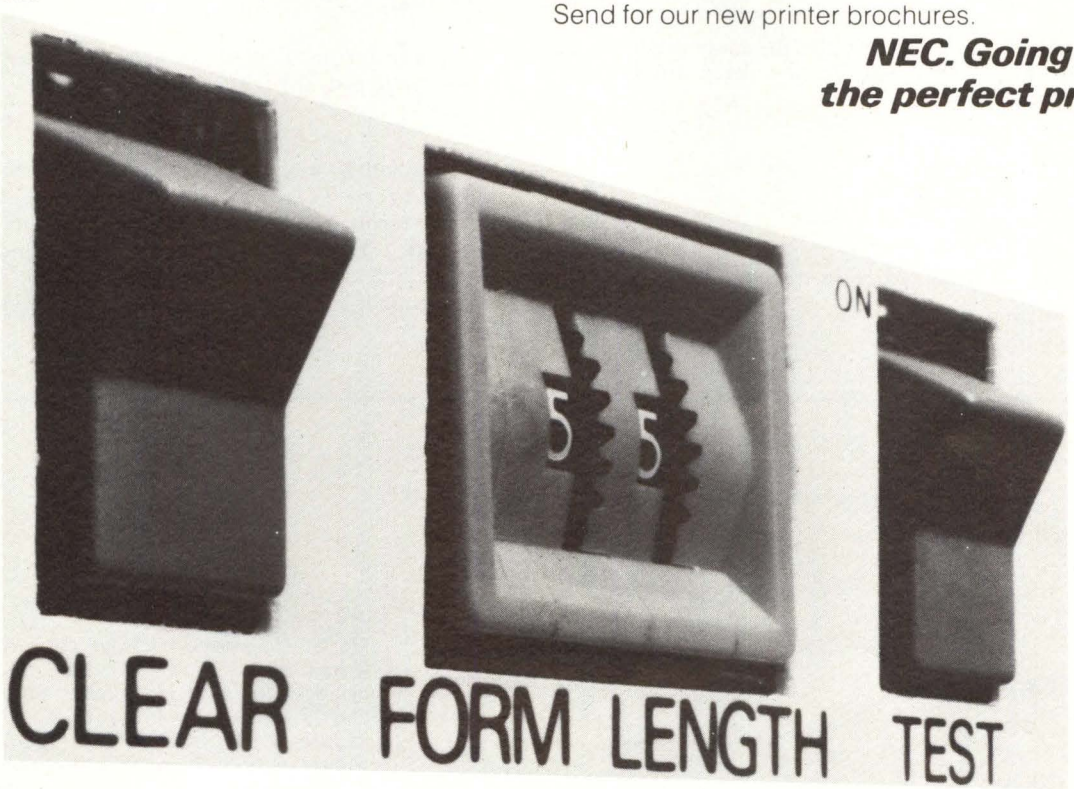

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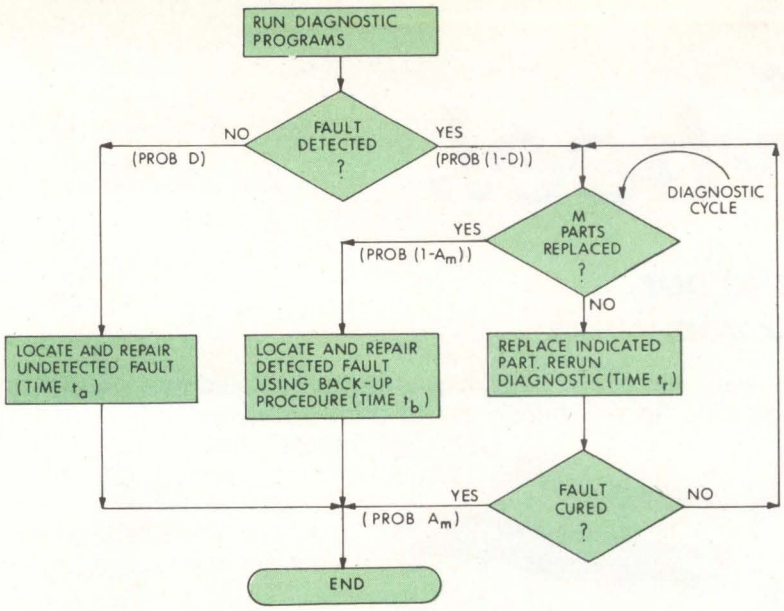

Fig 1 Repair procedure. If diagnostic program detects fault, it lists parts to be replaced in most-likely-first sequence. Maintenance strategy consists of replacing parts in sequence and rerunning diagnostic until fault is cured or some specified number of parts (M) have been replaced without solving problem. In latter case, fault is located and repaired using backup procedure which requires time t_b, where $t_a > t_b > t_r$

value of M; and then (if necessary) revise procedures and diagnostic until the desired MTTR is attained.

For a given system and diagnostic, compute D, A_m, and R_m from results obtained by running experiments or, alternatively, compute A_m and R_m from the following model of the diagnostic. Assume that

T = Total number of replaceable parts in the system

n_j = Fraction of the time that the diagnostic calls out the failed part as the jth part on its ordered list of parts to be replaced.

Then

$$\sum_{j=1}^{T} n_j = 1$$

and, assuming that all parts in the system are equally likely to fail,

$$A_m = \sum_{j=1}^{M} n_j$$

and

$$R_m = \sum_{j=1}^{M} j \times n_j$$

Suppose further that n_j are members of a geometric series with ratio $x < 1$. In other words

$$n_{j+1} = x n_j$$

For example, a system with three parts and $x = 0.8$ will have $n_1 = 0.41$, $n_2 = 0.33$, and $n_3 = 0.26$. (Each of these terms is 0.8 times the previous one, and their sum is 1.00.) That is, when a failure occurs and the diagnostic detects it and lists the three parts in the sequence it has determined is appropriate to the observed symptoms, re-

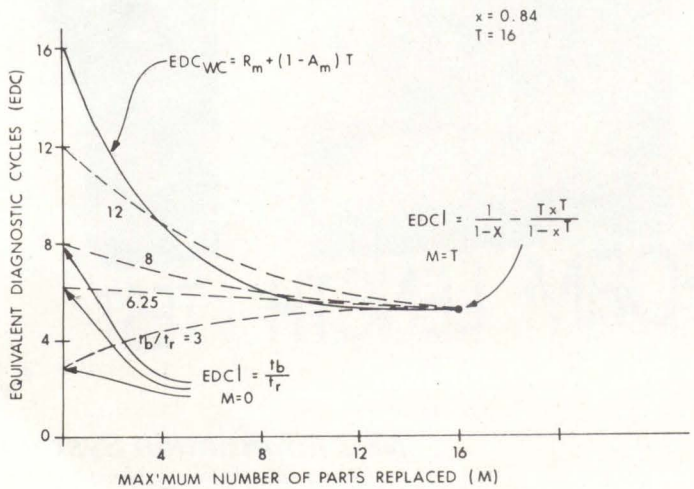

Fig 2 Diagnostic cycle vs parts replaced. Graph shows how equivalent diagnostic cycle varies with M, number of parts replaced before reverting to backup procedure. If $t_b/t_r = 3$, minimum EDC occurs with M = 0 (ie, diagnostic program should be used only for fault detection). For $t_b/t_r > 6$, minimum value of EDC occurs when M = T (ie, backup procedure is never used)

The Power Paradox:

The AC power your computer needs in order to operate is also a major cause of computer error, malfunction and damage.

The computers that control your operations (and therefore your profits) are designed to operate from a clean, steady supply of ac power.

This ac power *must* be kept within manufacturer-specified tolerances in order for the computers to operate properly and safely.

In fact, the U.S. Department of Commerce states that "if a computer's voltage exceeds 120% [of the rated voltage] for a duration as short as 1 to 10 milliseconds, the computer will make errors."[1] Unfortunately, interruptions and disturbances of this nature are commonplace occurrences within most computer facilities.

A comprehensive study of power line disturbances which affect sensitive computerized equipment was conducted by two IBM researchers. They concluded that such disturbances occur on an average of 128 times each month.[2] For users of computer-based equipment, power disturbances can and do create a variety of costly problems.

Effects upon data processing computers.

When these power disturbances occur in your data processing center they can cause entry errors, program changes or loss, head crash, data loss, the generation of false or garbled data, the need to rerun programs, and computer downtime.

Effects upon computerized process control equipment.

Process control equipment is also vulnerable to power disturbances. Common problems created by these disturbances include improper batch termination and even program changes. The program changes can result in the repetition of process errors and in downtime while equipment is being reprogrammed.

Effects upon energy management systems.

Most energy management systems use small computers to make energy-saving decisions, but their effectiveness can be offset by these same disturbances. Program changes and errors may prevent useful operation of these systems as energy savers.

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Topaz power peripherals can protect all of your computers.

Topaz can provide the power peripherals specifically designed to keep your company's data processing, process control and energy management computers from making costly power-related errors.

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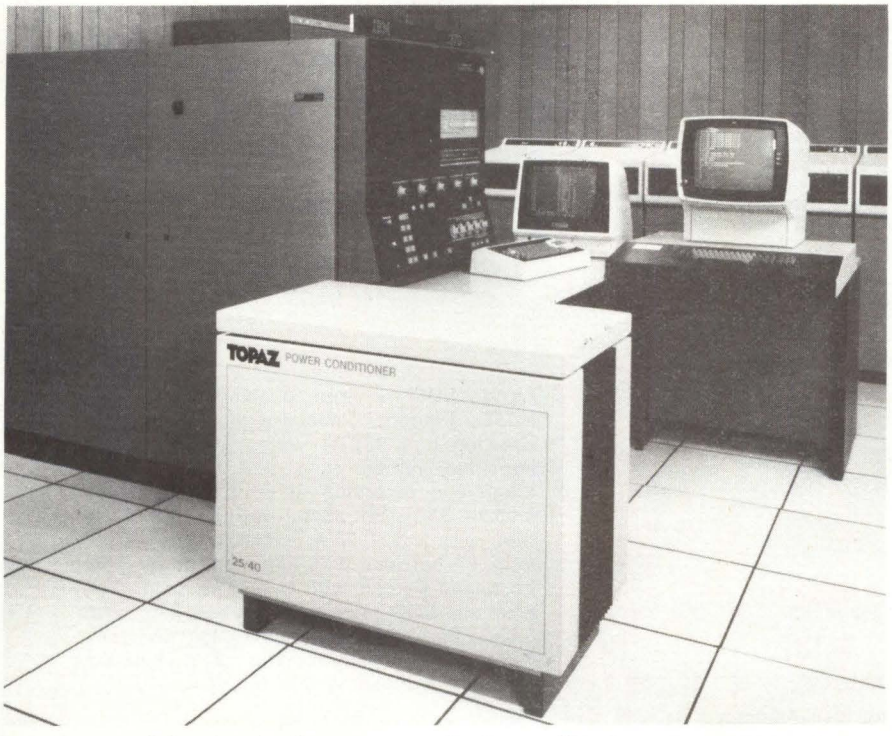
References:

1. *U.S. Department of Commerce, "The Effects of Electrical Power Variation Upon Computers: an Overview."*
2. *George W. Allen and Donald Segall, IBM Systems Development Div., "Monitoring of Computer Installations for Power Line Disturbances," presented to the IEEE Power Engineering Society.*



Topaz peripherals solve the power paradox by conditioning normal ac power for your computer and computer-based equipment.

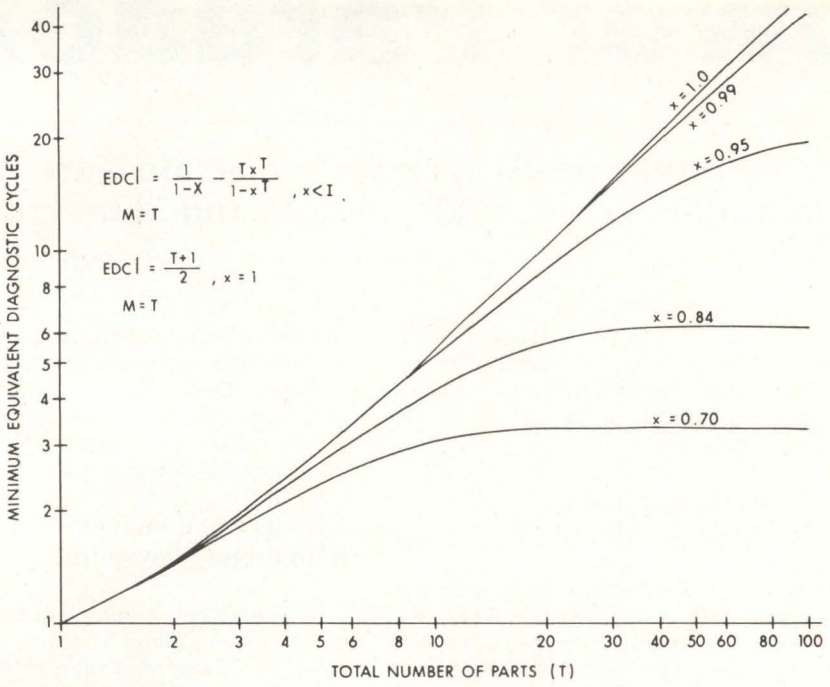


Fig 3 Minimum EDC vs T and x. For given diagnostic discrimination x, minimum equivalent diagnostic cycle increases with number of parts T in system, reaching maximum value of 1/(1 − x) for large values of T. EDC for x = 1 corresponds to useless diagnostic resulting in random sequence of parts replacement

placement of the first part on the list cures the problem 41% of the time, the second part 33% of the time, and the last listed part the remaining 26% of the time. With this assumption

$$n_j = \frac{x^{j-1}(1-x)}{(1-x^T)} \qquad A_m = \frac{(1-x^M)}{(1-x^T)} \tag{3}$$

and

$$R_m = \frac{1}{(1-x^T)}\left[\frac{(1-x^M)}{(1-x)} - M\,x^M\right] \tag{4}$$

Substituting Eqs (3) and (4) into Eq (2) results in EDC expressed as a function of the "diagnostic discriminator" x.

Fig 2 shows the EDC for a system having 16 parts, assuming a diagnostic with x = 0.84. Three points must be made in connection with this illustration.

(1) If the backup repair time t_b is too large, there may be a value of M for which it will be better to replace all remaining parts (going around the diagnostic cycle of Fig 1) than to use the backup procedure. Referring to Eq (2), the smaller of $(M + t_b/t_r)$ and T should be used. In other words, the worst case value of EDC is

$$EDC_{wc} = R_m + (1 - A_m)\,T$$

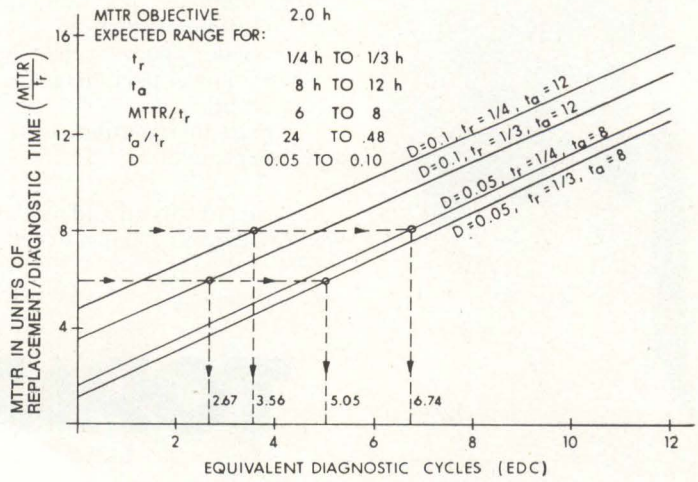


Fig 4 EDC required to achieve specified MTTR. Diagonal lines are plots of Eq (1) showing how MTTR varies with EDC for specified values of t_r and t_a, and with diagnostic detection at 90 to 95% (D = 0.05 to 0.10). Horizontal dotted lines show that, with t_r = 0.25 h (MTTR/t_r = 8), EDC must lie between 3.56 and 6.74, depending on t_a and D; and with t_r = 0.33 h (MTTR/t_r = 6), EDC must lie between 2.67 and 5.05. Fig 3 then determines for given T, what value of discrimination x is required to achieve these values for EDC

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The Maxi-Mini.™

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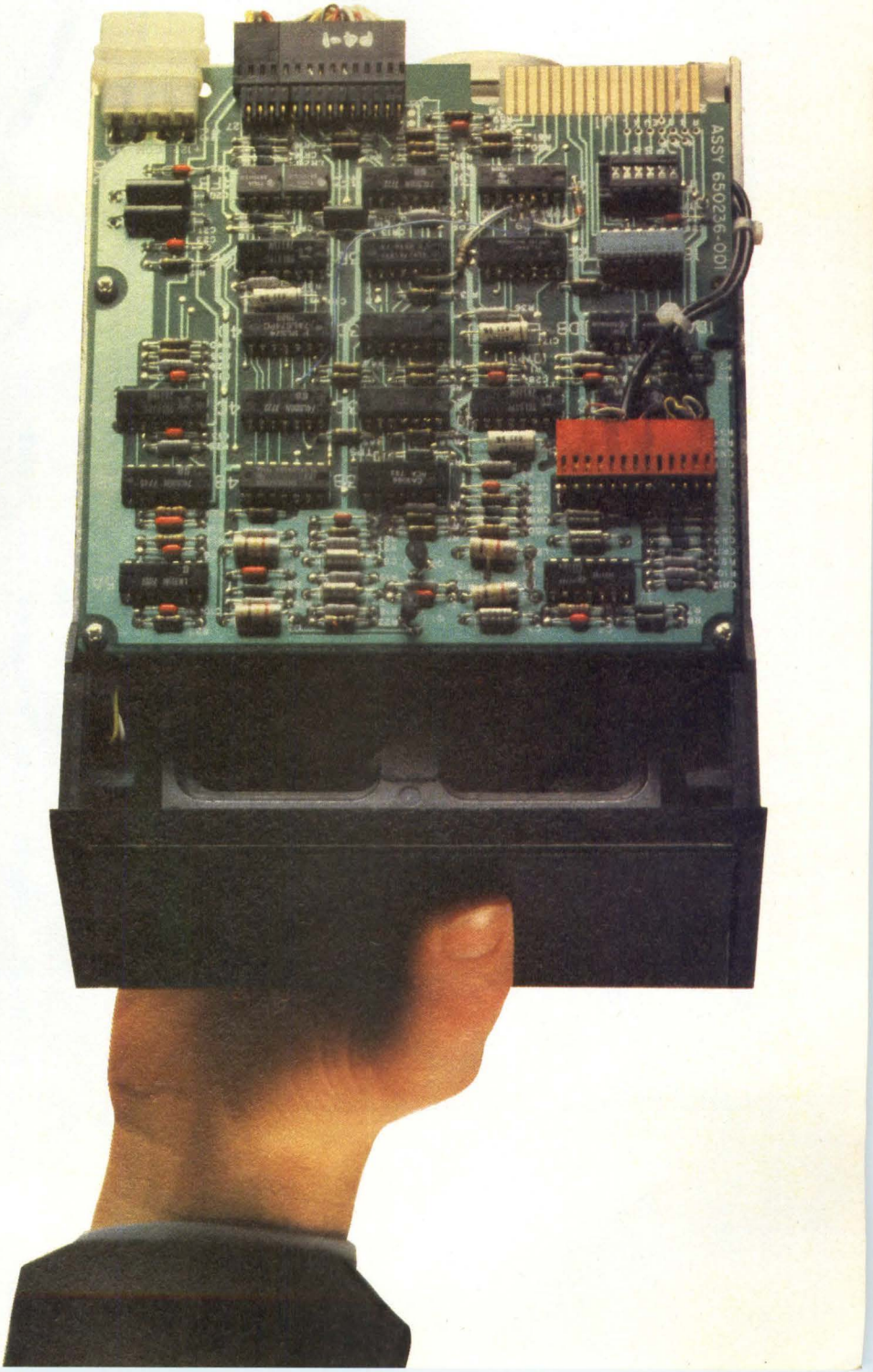

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CIRCLE 26 ON INQUIRY CARD

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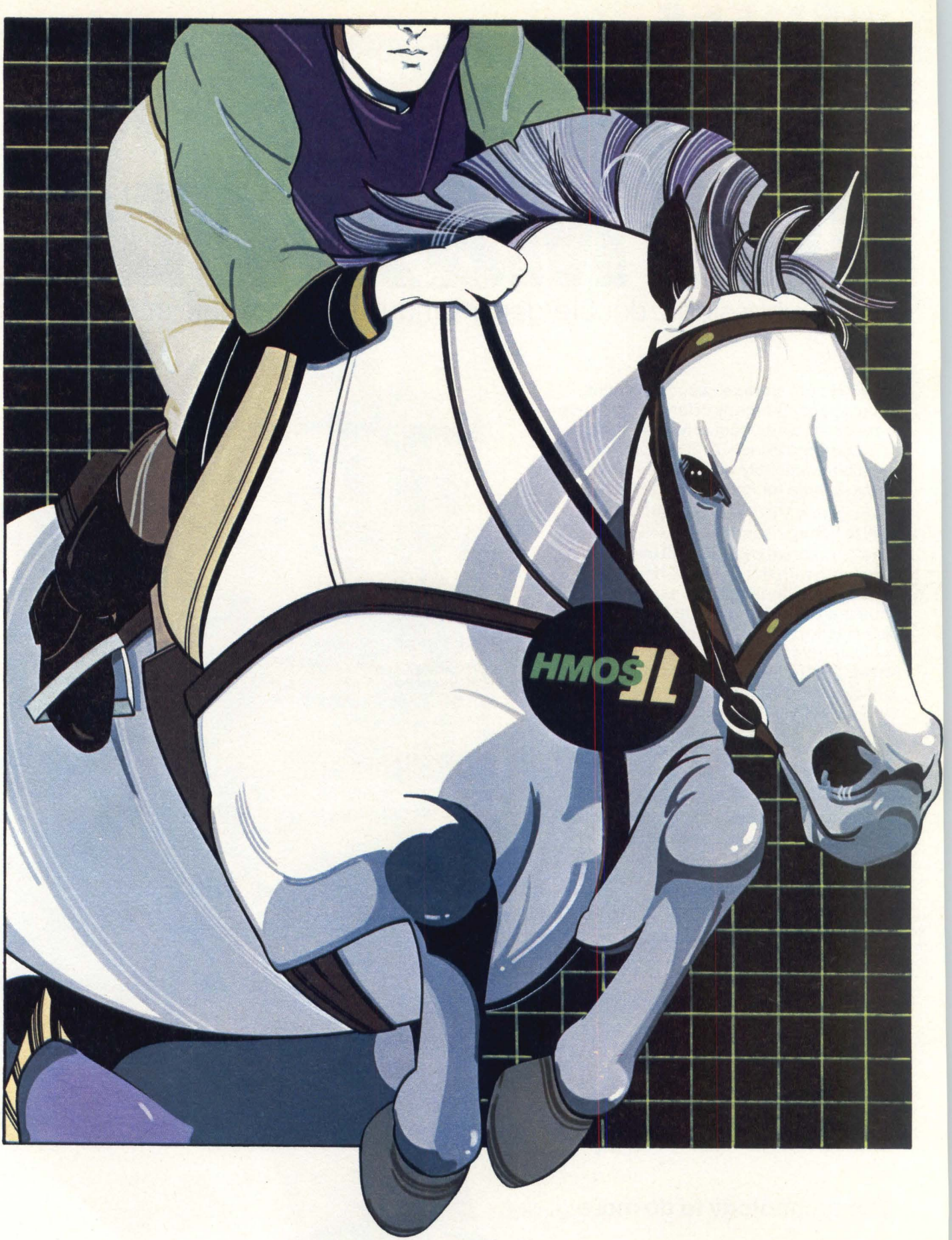

HMOS 3L

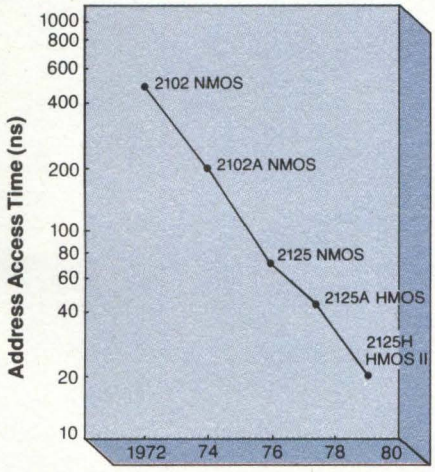
New Breed of MOS.

Intel introduces HMOS II*–and a new family of static RAMs that cross the finish line in 20 ns.

Intel just set a new pace for high performance memory with HMOS II. It's our patented next generation MOS technology so advanced it delivers speeds faster than bipolar and even our own first generation HMOS process. HMOS II gives designers the fastest, lowest power static RAMs ever—plus traditional MOS economy and reliability. Our new 2115H/2125H 1K RAMs ideal. For new designs, two versions deliver record access speeds of 20 ns and 25 ns, with a speed/power product twice as good as slower bipolar RAMs.

Our 35 ns and low power 30 ns models can be used as direct plug-in replacements for 93415A and 93425A bipolar RAMs. They'll cut power dissipation up to 36%. And, best of all, they're available now.

History of MOS speed



Intel's continued process and scaling improvements have doubled MOS speeds every two years. The above graph demonstrates this trend with Intel's 1K x 1 static RAMs.

1K and 4K RAMs are fully compatible, higher speed upgrades of Intel's time-tested 2115A/2125A and 2147 devices.

1K fast statics that leave bipolars behind

Designers building cache, writeable control store or buffer memories will find our 16-pin

New, faster 4K with no power increase

Intel's new 2147H gives you all the advantages of our 18-pin 4K x 1 industry standard 2147, with twice the speed and no increase in power. With access times as fast as most 1K RAMs, it's important news for anyone designing buffer, cache, control store and main memory systems. If you're presently working with 1K RAMs, you can increase density or reduce board space by a factor of four. In a 4K format, the 2147H makes possible a new dimension of higher performance systems.

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HMOS II fast static RAMs

Part No.	Maximum Access Time (ns)*	Power Consumption (mA)* Active	Standby
4096x1			
2147H-1	35	180	30
2147H-2	45	180	30
1024x1**			
2125H-1	20	125	
2115H-2 2125H-2	25	125	
2115H-3 2125H-3	30	100	
2115H-4 2125H-4	35	125	

*Over full 0° to 75°C operating temperature range.
**All 2115H versions have open-collector outputs, all 2125H versions have tri-state outputs.

All HMOS II components are fully static and can be used in clocked and unclocked systems. They are directly TTL compatible in all respects: inputs, outputs and operation from a single +5V supply.

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*HMOS II is a patented process of Intel Corporation.

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North Star has quadrupled the disk capacity of the Horizon computer but prices have increased a modest 15 percent. On a dollar per byte basis, that's a bargain that is hard to beat!

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Horizon 1-32K-Q	$1510
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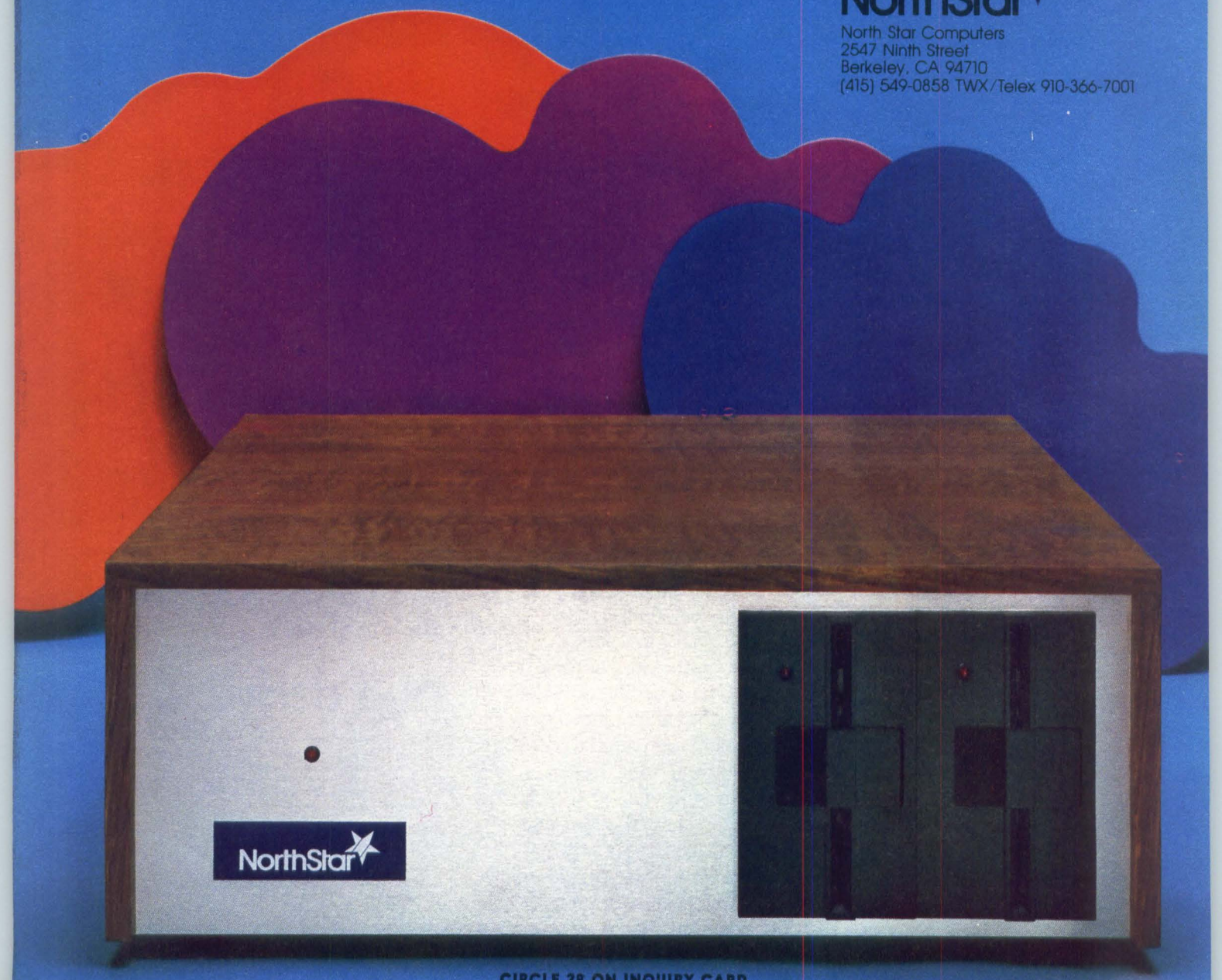


CIRCLE 28 ON INQUIRY CARD

(2) For reasonably large values of t_b the minimum EDC (and thus the minimum MTTR) occurs for M = T, and has the value

$$EDC_{min} = \frac{1}{1-x} - \frac{T\,x^T}{1-x^T} \qquad (5)$$

(3) If $t_b/t_r < EDC_{min}$, the backup repair procedure is so effective that the diagnostic should not be used except as a fault detector.

Fig 3 illustrates how the minimum EDC varies with T and x. This curve, along with Eq (1) for MTTR, can be used in maintenance planning. For example, suppose that an electronic system has 64 modules and an MTTR of 2.0 h is desired. Assume that t_r is expected to be between 15 and 20 min, and that t_a is to be between 8 and 12 h. Then, if the diagnostic programmers expect that their detection probability will be 90 to 95% (D = 0.05 to 0.10), what value of discrimination x must be achieved? Fig 4 shows that an EDC of 2.67 to 6.74 is required, depending on the values of D, t_r, and t_a. Fig 3 indicates that for T = 64, x must lie between 0.63 and 0.85 to achieve those EDCs. If the diagnostic programmers commit to D = 0.07 and x = 0.8, then from Eq (5) EDC ≅ 5, and from Eq (1)

$$t_a \leqq 28.6 - 66.4\,t_r$$

From this it becomes obvious that maintenance procedures which result in a repair/diagnostic time t_r of 15 min will permit a t_a of 12 h, but that an increase in t_r to 20 min will require t_a to be 6.5 h.

Conclusions

The most important characteristics of diagnostic programs are the ability to detect failures (measured by D) and to pinpoint faulty parts (measured by x). Most important aspects of a maintenance procedure, once a diagnostic has been designed, are the average time required to locate and repair a fault which the diagnostic does not detect (measured by t_a) and the average time required to replace a part and rerun the diagnostic (measured by t_r).

If the diagnostic program's discriminatory powers can not be approximated by a geometric series with ratio x, its properties can still be measured in terms of the parameters n_j, and A_m and R_m can be computed, and thus EDC and MTTR as a function of M. Gay's data for the telephone company's ESS diagnostics suggest that a diagnostic as originally written may have discriminatory characteristics with geometric series properties, but that such a diagnostic can be improved by focusing attention on the items at the top of the ordered list. If diagnostic analysis can be refined so that the probability of choosing the proper part in, say, one of the first three tries is increased (ie, n_1, n_2, and n_3 each increased at the expense of later values of n), then R_m, EDC, and MTTR will all decrease.

It has been shown that, in theory, the backup procedure should never be used. It is always better to continue replacing parts until the faulty part is found. In practice, however, the backup procedure is necessary to handle the awkward problem not covered by the "pretty" model—the situation where no part replacement will cure the fault, or where two or more parts must be replaced.

The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—**Ed.**

Minicomputers Reduce Form Factor and Add Slave and Component Capabilities

A compact slave minicomputer aimed at communications and process control applications and a series of board level minicomputer products directed at integrated component and multiple computer environments, the LSI 4/10S and the Scout Naked Mini model 4/04 extend the existing Naked Mini 4 line from Computer Automation, Inc, Naked Mini Div, 18651 Von Karman, Irvine, CA 92713. Both units incorporate the LSI 4/10 instruction set and use the same processor, but reduce the form factor through the use of higher density memory and logic circuitry, and the use of programmable logic devices that afford space savings at a ratio of 4:1.

Processor board of Computer Automation's Scout 4/04 (left foreground) is about half the size of LSI 4/10's CPU board. Overall size reduction is dramatic when power supply, chassis, and memory and logic boards are included in comparison

Slave Computer

The 4/10S is a slave minicomputer with 32k bytes of dynamic RAM and four I/O ports, packaged onboard with a 2-chip custom MOS processor and associated logic. Up to four slaves operate under control of a single host. Attaching to the same bus as the system processor, the slave operates as a peripheral DMA device for offloading CPU functions that run concurrent with and independently of the host processor. Software is provided for using the slave with either the Naked Mini 4 or LSI 2 series computers.

The company's concept of slave computing, as distinct from multiprocessing, is the technique for improving performance by adding parallel, autonomous computers with their own memory and I/O ports to a host computer system. Since the slaves operate under their own program control software, impact on the host system is minimal. The slave is similar to the existing LSI 4/10 in terms of physical size, bus architecture, CPU, and software compatibility; it differs in memory design and interface logic.

The slave is distinguished from multiprocessing devices by its private memory, and distributed I/O ports that accept all intelligent cables. I/O transfer rates can reach more than 38k bytes/s with private memory. Major benefits are increased overall system throughput, more efficient memory utilization, and ability to modularize applications programs. A slave computer is not limited by bus speed, software overhead, or memory contention problems when operating autonomously.

More efficient memory utilization results from the processor's direct addressing of its own onboard RAM and half of the host processor's 64k bytes of public memory. Instructions execute out of either memory, and data or instructions can be block moved from public to private memory.

Another important aspect is the software compatibility between master and slave. The slave's instruction set is a superset of the master's standard set with additional instructions for addressing, communications, and master-slave control services. The slave may be reset, interrupted, and have slave control service functions performed from the host machine through I/O instructions.

Standard on the half-card processor are realtime clock that is independent of the host's realtime clock. A buffered Maxi-Bus DMA interface provides for internal memory operations without Maxi-Bus interference. The slave can be used in any chassis position that a standard DMA controller can occupy. Multiple slave processors can operate in a single chassis, provided power, slot, and DMA priority chain requirements are met. Circle 175 on Inquiry Card

Component Computer

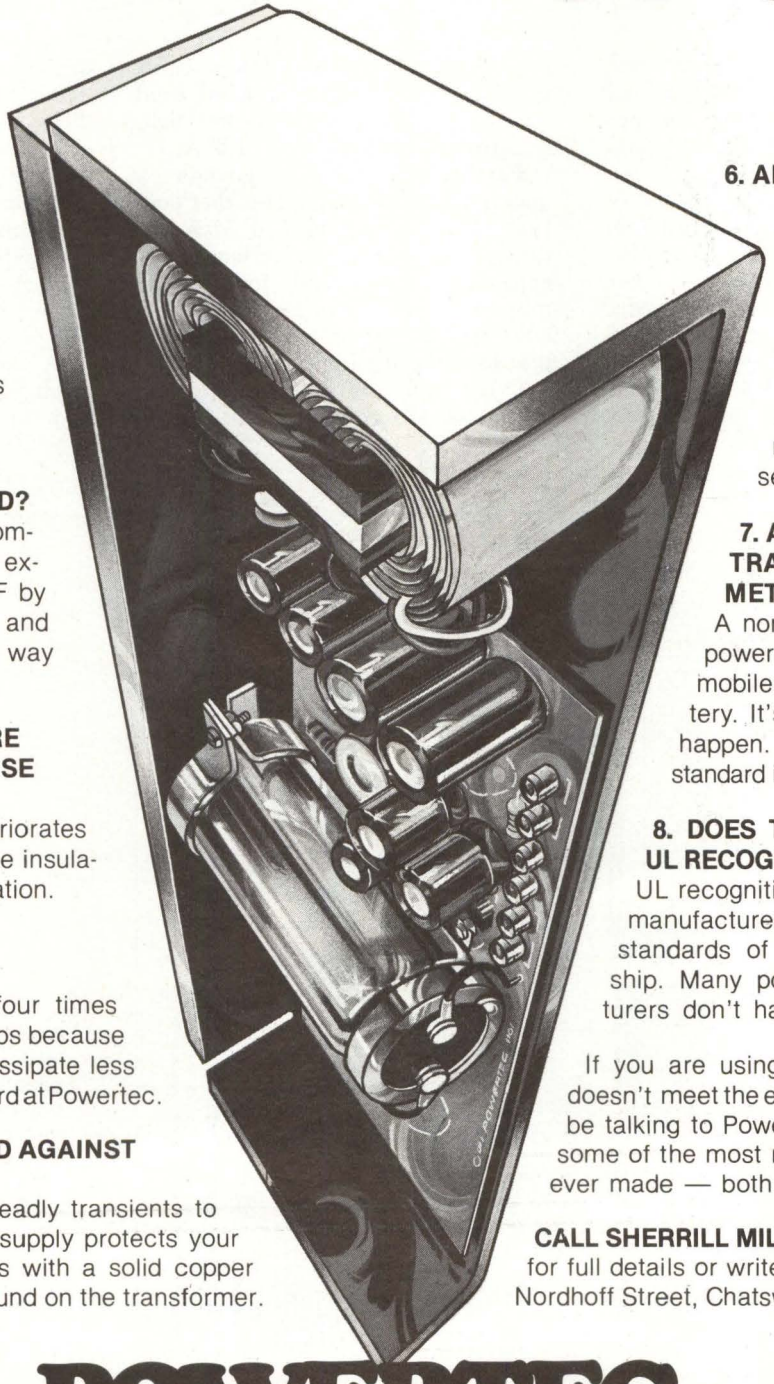
Board level products in the Scout Naked Mini 4/04 series extend the line downward in size and price but deliver approximately the same performance as an LSI 4/10. A Scout configured with four modular circuit boards and power supply occupies less than one-half the space of a 4/10 package, but sells for approximately 20% less. Both size and price adapt the unit to use as a component within a larger system and in multicomputer environments where several units perform under control of a supervisory computer. Other criteria influencing its development relate to reliability, software compatibility, modularity, and repairability.

The computer system consists of a CPU, 10 supporting system and functional boards, card cages, and a 5-V power supply. Some circuit boards, measuring 6.25 x 8.3" (15.8 x 21.1 cm) are priced low enough to make the throw-away versus repair decision an issue. A minimum useful configuration consists of three cards. Either 4- or 9-card cages are provided.

Central processor board provides architecture compatible with other family members in terms of data types processed, addressing modes, I/O modes, register file, status register contents, interrupt and trap handling, optional realtime clock, and autoload/autostart capabilities. The processor is word or byte addressable, with direct addressing to 128k bytes. Multiple DMA and interrupt devices are supported. The instruction set is common to the LSI 4/10.

A dynamic RAM board with 32k bytes is standard with ability to ex-

Eight Ways to Rate a Power Supply



1. DOES THE PC BOARD USE 2-MIL COPPER?
Many power supply companies use cheap 1-mil copper — even 0.5 mil copper. Powertec uses expensive 2-mil copper in all high-current circuits to keep temperatures low and the MTBF high.

2. ARE HOT COMPONENTS RAISED OFF THE PC BOARD?
Mounting heat-dissipating components off the board is more expensive, but raises the MTBF by keeping them in the open — and therefore cooler. That's the way we mount them at Powertec.

3. DOES THE TEMPERATURE OF THE TRANSFORMER RISE LESS THAN 45°C?
If it doesn't, insulation deteriorates fast. At Powertec, we keep the insulation cool by vacuum impregnation.

4. ARE THE CAPACITORS COMPUTER GRADE?
Computer grade caps last four times longer than ordinary grade caps because they use a better seal and dissipate less heat. That's why they're standard at Powertec.

5. IS THE LOAD PROTECTED AGAINST LINE TRANSIENTS?
Many power supplies pass deadly transients to the load. A Powertec power supply protects your device against line transients with a solid copper electrostatic safety shield wound on the transformer.

6. ARE THE IC'S PRE-TESTED?
If not, watch out! Marginal IC's are a prime cause of power supply failure. That's why Powertec tests all significant semi-conductor parameters — *before* assembly!

7. ARE THE POWER TRANSISTORS HERMETICALLY SEALED?
A non-hermetic device in a power supply is like an automobile with an uncapped battery. It's a disaster waiting to happen. Hermetic devices are standard in all Powertec products.

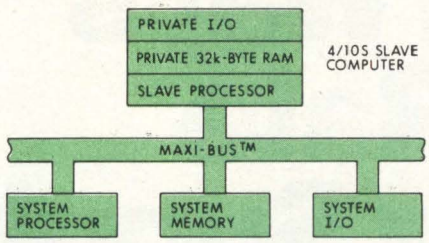
8. DOES THE PRODUCT HAVE UL RECOGNITION?
UL recognition means a product is manufactured to consistently high standards of safety and workmanship. Many power supply manufacturers don't have it. Powertec does.

If you are using a power supply that doesn't meet the eight criteria, you should be talking to Powertec. We manufacture some of the most reliable power supplies ever made — both switchers and linears.

CALL SHERRILL MILNER at (213) 882-0004 for full details or write Powertec Inc., 20550 Nordhoff Street, Chatsworth, California 91311.

POWERTEC

CIRCLE 30 ON INQUIRY CARD



LSI 4/10S attaches to same bus and operates as slave under control of host system, but uses its own program control software to minimize impact on host computer's throughput and prevent memory contention problems

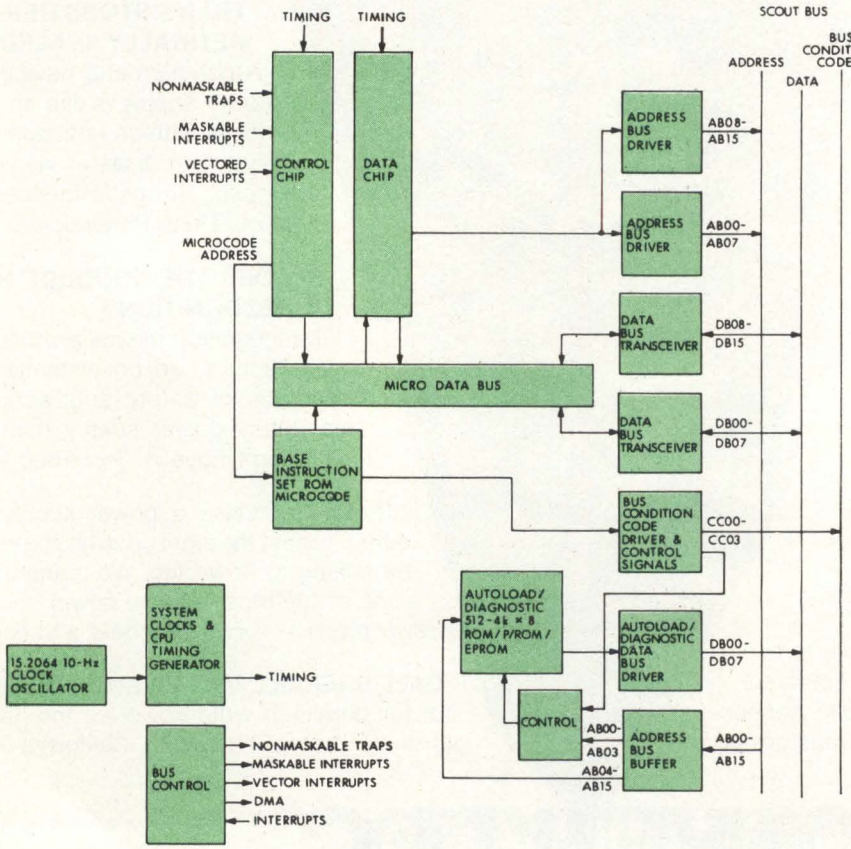
pand to 64k or 128k on the same board. Cycle time is 550 ns, and automatic address allocation is provided. A combination RAM/EPROM board allows static RAM to be selected in increments of 0, 4k, or 8k bytes. Chip sockets permit addition in 4k-byte increments of user programmable EPROM up to 32k bytes.

Although a console is not needed in most applications, a remote console interface board interfaces the processor bus to an LSI 4 remote console for system development, test, or debug operations. Relay cards provide eight optically isolated solid state relays each, with control voltage from 5 to 120 V at 1.5 A.

Parallel I/O boards contain a microprogrammed computer that controls data transfer to and from I/O devices. Boards for paper tape reader/punch control and for general purpose 16-bit interface are available. Similar serial I/O boards support RS-232 compatible devices.

Other boards in the support group consist of A-D converter with 12-bit resolution, 16 single-ended or 8 differential input channels, and 20-kHz throughput rate; an extender card that provides access to signals on the processor board for test and development as well as an optional interconnection between Scout motherboards to extend bus signals; and a blank prototype board that allows users to develop interfaces to the processor bus.

A self-diagnostic capability on each board signals go/no go via an LED to allow users to conduct their



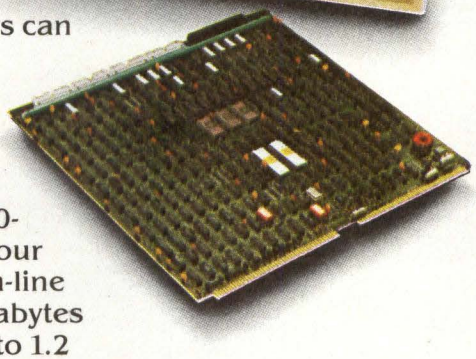
Processor board in Scout Naked Mini 4/04 packs family compatible architecture, interrupt and trap handling capability, and direct addressing of 128k bytes of memory, along with diagnostic capabilities into a 6.25 x 8.3″ (15.8 x 21.1-cm) area

Nova, Eclipse and PDP-11 Users:

TAKE YOUR COMPUTER, ADD ONE BALL DISK CONTROLLER, AND MIX OR MATCH FOUR DISK DRIVES.

At last. Intelligent disk controllers for your Nova/Eclipse or PDP-11. They plug right into the host computer. They accommodate both removable and Winchester fixed media drives. And best of all, they allow intermixing of any four SMD interface-compatible disk drives. That's right, four drives in any mix of standard capacities, transfer rates or organizations.

The new 3255 Disk Controller for Nova and Eclipse
Now, Nova and Eclipse users can meet their particular mass storage needs with a wider choice of drives. The 3255 controller allows intermixing of any four Storage Module, Winchester or 3330-type disk drives (including our own Ball drives) for total on-line storage of up to 1200 megabytes and data transfer rates up to 1.2 megabytes/second. All this from a single board, host-resident controller with the latest operational features.



Standard features: **Automatic 11-bit ECC. Self-diagnostics. A 2K FIFO data buffer. Support of multiple record length formats, overlapped multiple seeks, strobe/track offset error recovery, and much more.**

The new 3211 Host-Resident Disk Controller for PDP-11
All the same features of the 3255, including drive intermix capability, are available with the 3211 controller for the PDP-11 series. The 3211 emulates the DEC RM02 controller without software modification.

Ball is more than a controller supplier—Add our BD Series 50 or 80 megabyte drives and you have a fully integrated, ready-to-run data storage subsystem. You get a smooth running package with single source responsibility.

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Ball Computer Products Division

CIRCLE 31 ON INQUIRY CARD

Mostek quality. Commit it to memory.

At Mostek, we build only the highest quality memory systems.

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That's why we can put a one-year warranty on every memory board we sell.

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Our broad line of memory systems gives you a wide choice of density options, including some of industry's largest and fastest configurations.

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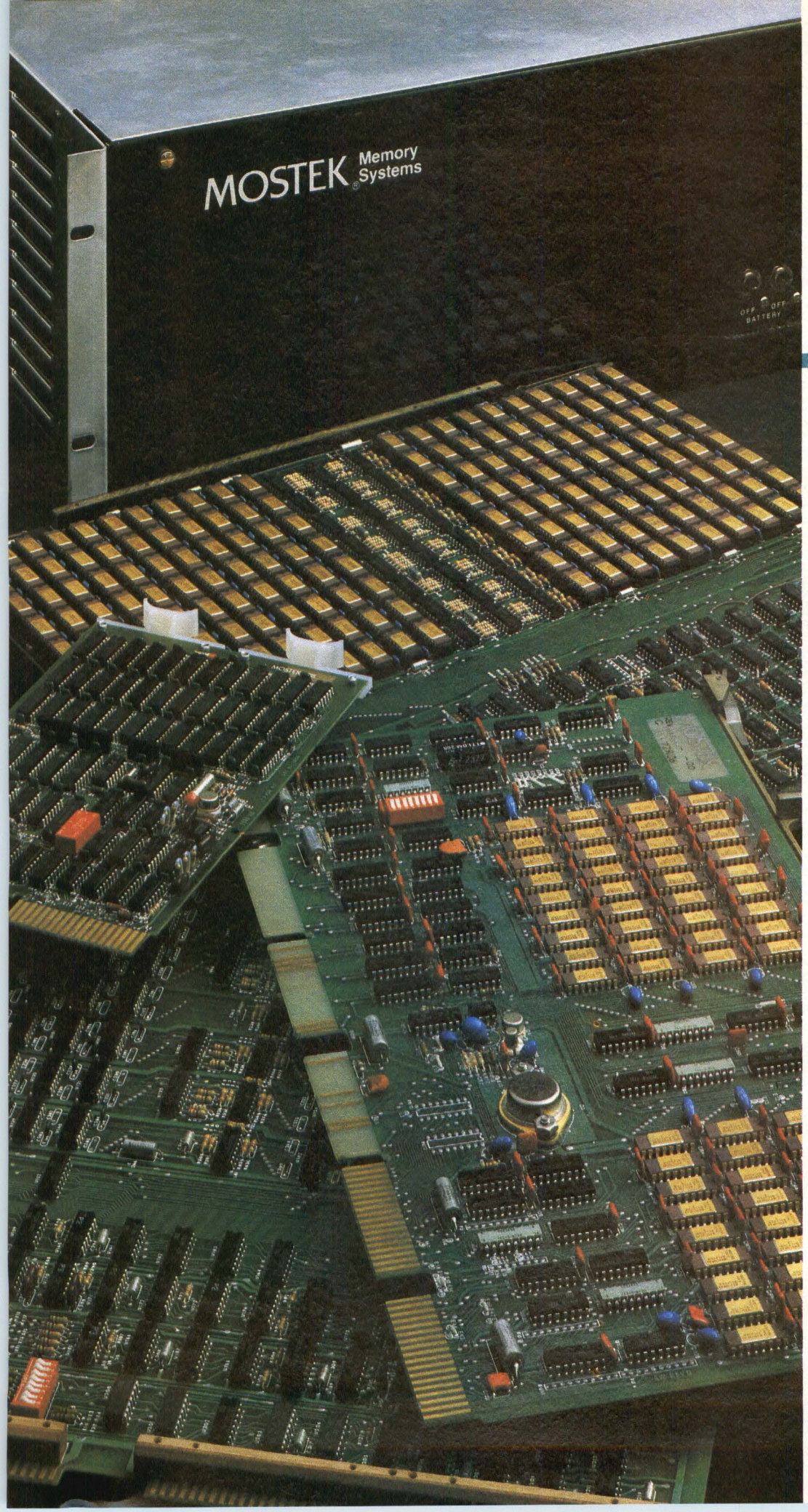
Our competitive pricing, OEM discounts, and fast delivery. Call one of our offices: Eastern, (201) 842-5100; Central, (214) 386-9141; Western, (408) 287-5081; Southern California, (714) 549-0397; Memory Systems Marketing, (214) 242-0444, ext. 3552. Or write us at 1215 West Crosby Road, Carrollton, Texas 75006.

MOSTEK Memory Systems

Mostek System Number	Minicomputer	Density Options	Special Features
MK 8001	PDP-11*	16K, 32K, or 64K words X 18 bits	Voltage options available
MK 8011†	PDP-11*	16K, 32K, or 64K words X 18 bits	Optional on-board parity generation and check.
MK 8005	LSI-11/2*	16K, or 32K words X 18 bits	Optional on-board parity generation and check.
MK 8009	PDP-8*	Coming Soon!	
MK 8601	PDP-11/70*	Up to two megabytes in a seven inch chassis.	Can operate in the interleave and serial modes simultaneously.
MK 8003	Nova 3**	16K, 32K, 64K or 128K words X 17 bits	Industry's highest density Nova 3 Add-in
MK 8004	Eclipse**	16K, 32K, 64K, or 128K words X 16/21 bits	Optional ERCC
MK 8000	General Purpose	Up to 128K words X 24 bits	Configure one megabyte with three cards.
MK 8600	General Purpose	Up to 5 megabytes in a 12 inch chassis.	Industry's largest Add-on system.

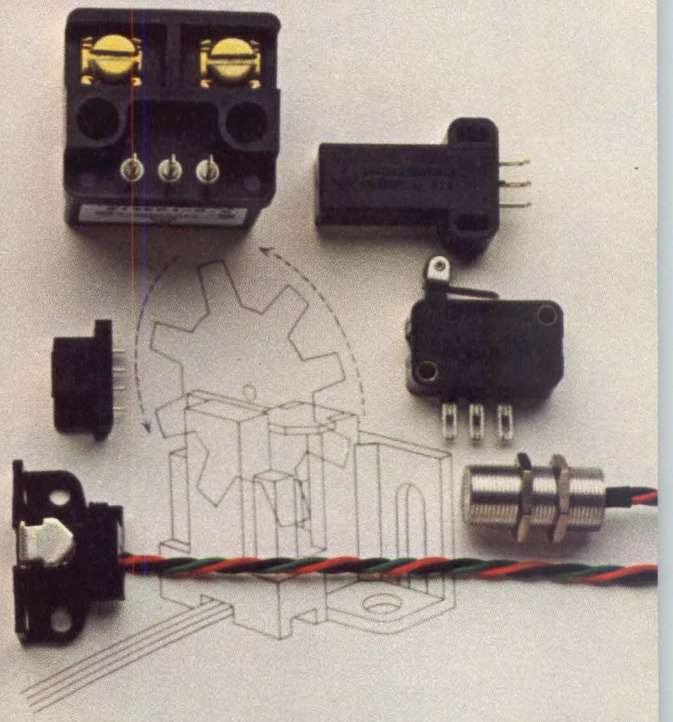
* A trademark of Digital Equipment Corp.
** A trademark of Data General Corp.
† Available 3rd Q.

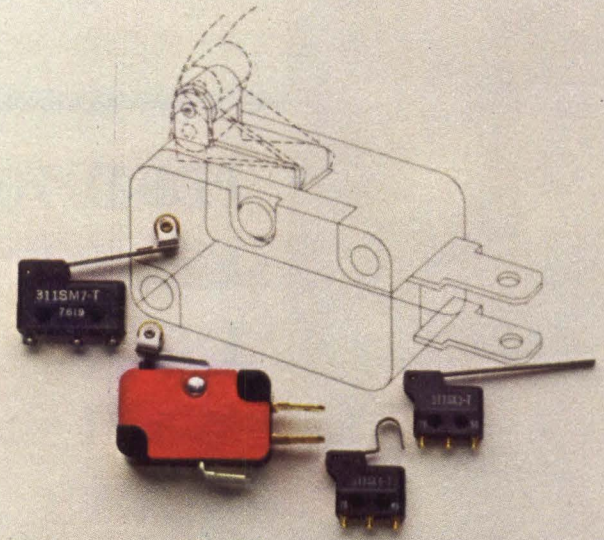


PDP-11/70
ECLIPSE
LSI-11/2
PDP-11
NOVA 3

Some of these components will probably never. The others will just come close.

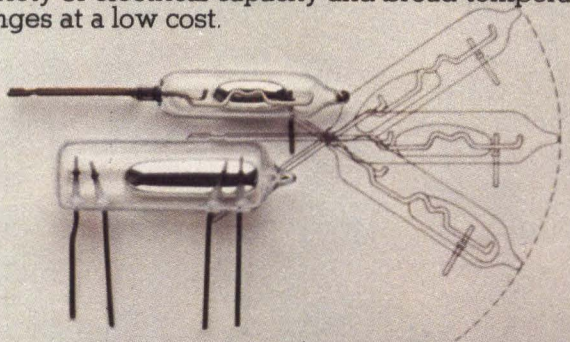
The SR, XL, XK and AV are solid state position sensors featuring almost infinite life. All offer zero speed operation with some up to 100 Khz. ES current sensor utilizes Hall-effect IC and protects against damage from short circuits or overcurrent conditions.

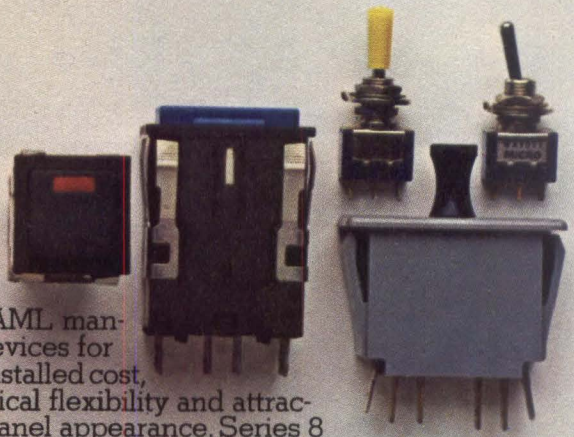




Snap-action V3, SM and SX switches offer wide variety of actuators, electrical capacity and termination.

Mercury switches offer hermetic sealing, a variety of electrical capacity and broad temperature ranges at a low cost.





AML manual devices for low installed cost, electrical flexibility and attractive panel appearance. Series 8 miniature manual switches provide small size and wide variety of operators. DM offers inexpensive snap-in panel mount design.

Solid state keyboards provide high reliability no mechanical keyboard can offer. Panel sealed versions also available.

own test of board level components. Users can allow the diagnostic routine to execute automatically at startup or can invoke the program via software command.

The diagnostic on each board is implemented in a 4k-byte ROM and may include an autoload capability. Optionally the user may program the ROM to his own specifications. Firmware provides for chained diagnostics so that each board in the configuration can be tested sequentially.

Software consists of OMEGA 4, a general purpose memory based software development system that includes assembler, editor, object loader, and debug utility; realtime executive, a small fast version of RTX4 which can be made ROM-resident, that includes interrupt, clock and task control services, I/O, file management, and communication services; and INTERCOMM, a communications subsystem that supports asynchronous devices using the DDCMP protocol and enables downline loading of application programs.

Circle 176 on Inquiry Card

Medium to Large Scale Computer Systems Offer Distributed Processing

Series 60 computer systems, addressing the distributed processing area, bracket IBM 4341 and 4331 systems and are price/performance competitive with them. Level 66/Distributed Processing System models DPS-440 and -520 and Level 64 models DPS-320 and -350 extend the existing 66 and 64 lines downward and upward, respectively, and support the distributed systems environment implemented by Honeywell Inc, United States Information Systems Group, 200 Smith St, Waltham, MA 02154.

Level 66 DPS-440 and -520 models extend the large scale family downward, fit within DSE as hosts or cohosts, and offer software compatibility with Level 6 minicomputers. DPS-440 offers twice the performance of the previous entry level system, while the -520 offers performance about 1.5 times that of a -440. Both use integrated system modules and 16k MOS circuitry to provide floor space, power, and cooling savings over previous Level 66/DPS systems.

The DPS-440 consists of a central system that includes CPU, system control unit, and one I/O multiplexer with 18 channel function slots. 1M- or 2M-byte memory made from 16k MOS RAMs is available. The DPS-520 central system is configured similarly but provides 1M-, 2M-, and 4M-byte memory versions.

For use on these two machines only, the Datanet 6641 frontend network processor provides network communication power. Using minicomputer technology, the 6641 processor operates asynchronously under firmware control. A basic unit includes 64k bytes of memory, with capacity for an additional 64k, and is compatible with system software and user generated programs of the Datanet 6600 family.

The multipurpose CSU 6601 system console combines technology and design conveniences to improve operator interface with the system. The freestanding console provides 12" (30.5-cm) CRT, 120-char/s printer, and interactive message transfer capability.

Extending the medium scale Level 64 family, DPS-320 and -350 central processors are claimed to improve hardware price and performance, and software functionality. The DPS-320 is estimated to equal the IBM 4331 in price and performance, while the -350 increases performance significantly at a small increase in price.

A basic -320 has 50% greater internal performance and five times the memory capacity of the family's previous basic processor, and the -350 has 2.6 times greater performance and five times the memory capacity. Basic memory in both units is 512k bytes, expandable in 256k increments to 1M bytes in the -320 and 2M in the -350.

An integrated communications controller supports up to 14 communications lines. Each line handles 16 display or printer terminals. The controller enables the units to communicate with other Series 60 computers and to be configured as part of the distributed systems environment. In this configuration it is supported by a network of Level 6 minicomputers in remote batch processing, remote job entry, and interactive data entry from a single terminal or a cluster of terminals.

Other standard features include an integrated mass storage processor capable of attaching eight 100M- or 200M-byte discs, an integrated unit record processor for attaching printers and card equipment, a console

and 30-char/s console printer, and RMS-64 to provide remote maintenance capability.

Among the software packages available for use on the systems, the GCOS 64 operating system communicates with Level 6 satellites, the query driven system provides a command and inquiry capability for file inquiry and report building using English language commands, and a terminal oriented facility operates in interactive mode for terminal based file browsing and updating. BASIC programming language offers a complete program development system as a tool in scientific and business applications.

Purchase price for the 512k-byte DPS-320 is $81,360; a 512k-byte DPS-350 sells for $155,232. Deliveries will begin in the second and third quarter of the year, respectively. With deliveries planned to begin first quarter 1980, prices of 1M-byte DPS-440 and -520 are $198,338 and $371,316 respectively.

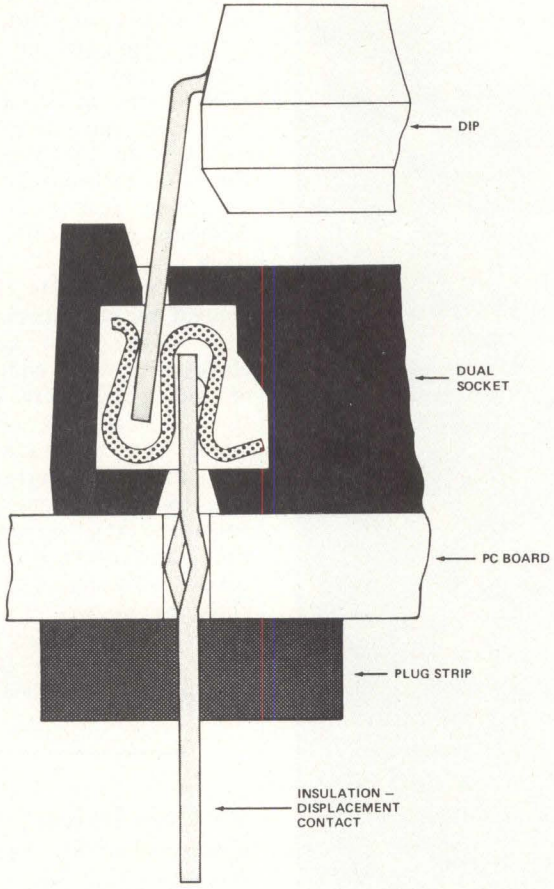
Circle 177 on Inquiry Card

Breadboard System Increases Accuracy And Aids Direct Conversion

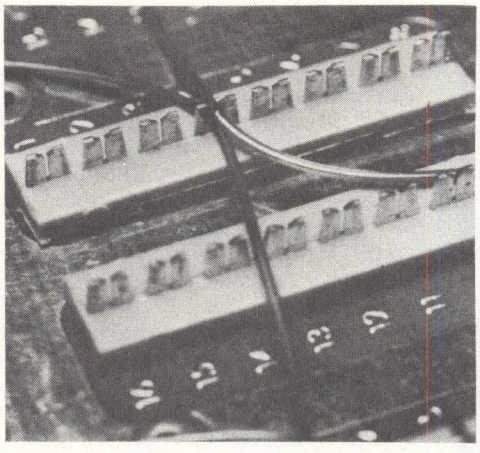
Insulation displacing contacts are combined with a solderless connection system to provide fast reliable prototyping of printed circuit boards. 3M Co's Electronics Products Div, PO Box 33600, St Paul, MN 55133, claims several advantages for the breadboard system over wrap post systems. Cited are labor and time savings, accuracy, and direct conversion from prototype to production boards.

The system combines the insulation displacing capabilities of Scotchflex "U"-contacts with a connecting system that permits solderless connection to boards with plated-through holes. Connectors include solder strips, plug strips, and 16-position dual sockets.

A connection is made with continuous 30 AWG solid insulated wire which is inserted into the U-contact using an inexpensive hand tool. Labor and time savings of more than 50% result from the elimination of the stripping, soldering, and crimping operations in interconnection of contacts. Time savings and accuracy are particularly evident where multiple busing is necessary. Each contact



Breadboarding system from 3M's Electronic Products Div uses solderless connections. "S" shaped interior connector holds dual socket and plug strip together and makes firm contact with DIP lead. Split tail maintains consistent electrical connection without soldering in plated-through hole



Insulation displacement contact used in breadboard system accommodates two wires making 4-connection busing possible and eliminating four separate stripping and wirewrapping operations

"Golly, I found a pain in my parity."

The only GCR tape sub-system for minis that troubleshoots itself 3 ways.

This GCR tape transport subsystem gives you three self-diagnosing systems, each in a different mode.

First, there's the only continuous self-circuit-checking system on the market. Then, in the off-line mode, via a built-in key-board, there's full fault isolation right down to the chip level. And finally, in the on-line mode, there's PCC's superior total check-out diagnostic system which also has fault isolation to the chip level.

Besides this unique 3-level diagnostic capability you get GCR recording density of 6250 bpi and a transport speed of 125 ips all in a 19"x24" package.

You also get the simplest interface in the business. By far. Direct parallel transfer 16-bit words, all in only 29 lines.

The PCC GCR–the tape transport system with three built-in doctors. So there's no waiting.

PCC PERIPHERALS
PERTEC COMPUTER CORPORATION

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(In Oklahoma, call collect 918-664-8300.)

CIRCLE 33 ON INQUIRY CARD

accepts two wires, providing four connections or the equivalent of four separate stripping and wirewrapping operations.

Because contacts are approximately one-third the height of wrap posts, prototype boards can mount in the same space as production boards. This not only improves prototype packaging density, but contributes to more noise free operation, especially in high speed circuits. Furthermore, it enables the designer to move directly from prototype to production board without redesign or fine tuning.

In addition, the system simplifies reuse of the board and components. Wires can be removed without unwrapping or cutting, and dual sockets and plug strips can be removed using a hand tool.

Breadboard components are compatible with all boards with or without plated-through holes. Other system components include a G-10 quality board measuring 4.5 x 5.5" (11.4 x 13.9 cm) and wiring tool with self-contained wire feeder and cutting tip. Components are available separately for those working with their own PC boards; a kit that includes a board and quantities of individual components is available for those needing a PC board.

Single kits are priced at $97.50; discounts on quantities of 25 or more reduce the cost to $81.25. 8-contact solder strips and plug strips are $0.29 each, and dual sockets are $1.22 each in quantities of 1000 or more.

Circle 178 on Inquiry Card

Dot Matrix Printer Combines Speed/Quality For Word Processing

Printer model 753 combines high density dot matrix print quality with 130- to 150-char/s throughput, proportional spacing, and right justification to meet the need for high print quality without sacrificing speed. Offered by Centronics Data Computer Corp, Hudson, NH 03051, the printer gains speed through use of a high speed paper motion system capable of 15-in (38-cm)/s slew.

A 9-pin free flight printhead controlled by the unit's microprocessor places dots in up to 18 horizontal and 9 vertical positions per character, creating characters with twice the density of those formed using a traditional matrix. The free flight printhead operates by propelling solenoid-actuated wires against the paper in a near straight line. This enables different forms thicknesses to be used without adjusting the printhead gap.

The N x 9 high density dot matrix feature allows large letters, such as capital M and W, to have a near letter quality appearance since more dots are used in their creation and these dots are so close that they appear to overlap. The printer's proportional spacing feature automatically compensates for character size differences by adjusting the horizontal width of letters, further improving the overall appearance. The combination of proportional spacing and high dot density generates high quality characters that are easy to read.

Standard features of the unit include 132-char wide columns, bidirectional logic seeking operations, downstream loading of vertical format commands, tractor paper feed, paper out indicator, auto motor control, tear bar, and single line feed switch. Options include audio alarm, 2-channel electronic VFU, operator selectable 6- or 8-line/in (2 or 3/cm) paper spacing, interface connector, and quietized cabinet. Each of four models has a self-contained test print capability that permits the printer to be operated offline for forms setup or operation tests.

Circle 179 on Inquiry Card

Computer Series Enhances Performance, Retains Family Compatibility

Four Series 700 machines—models 720, 730, 750, and 760—in the CYBER 170 family improve performance as much as 60% while reducing costs by 3 to 15%. The series, introduced by Control Data Corp, PO Box O, Minneapolis, MN 55440, replaces five existing family members and retains compatibility with existing software and peripheral products.

Incorporated in the machines are improvements in design and configuration that enhance interactive, remote batch, and transaction data processing as well as database management for commercial and scientific applications. Of primary concern in the design was improvement of operating economy in areas such as space and power, and provision for incremental growth.

Two central processor types are used in the series: unified and functional. These processors use emitter coupled logic to effect high reliability and reduce power requirements.

Model 720 and 730 feature a unified arithmetic central processor; instructions and operands use common system components that permit optimum use of system circuits. The CPU's instruction control section directs arithmetic operation, manages character manipulative functions of compare/move unit, and provides an interface between the arithmetic section and central memory control.

Central memory control provides service to all memory access paths on a priority basis, queues access requests as necessary, and resolves access conflicts. It controls read/write operations, increments addresses, and processes parity generation and checking for addresses and data.

Built from 4k static MOS RAMS, central memory is available with capacities from 0.98M to 2.62M characters. It is organized in eight logically independent phased banks of 60-bit words and permits 10 6-bit characters to be stored in each word. Complete cycle time is 400 ns (major cycle) and banks are phased so that successive addresses are in different banks, permitting operation at higher than basic rates. Maximum data transfer rate is 10 char/50 ns (minor cycle).

Central processor for models 750 and 760 features nine phased arithmetic units that operate independently, permitting concurrent execution of specific functions. Phased functional units perform Boolean, shift, normalize, integer add, floating add, multiply, divide, population count, and increment functions. This phasing increases data flow without comparative increase in required computer resources. Data move in and out of functional units through internal operating registers.

Central memory control circuits direct arithmetic operation and provide interface between functional units and central memory. These circuits also perform instruction retrieval, address preparation, memory protection, and data retrieval and storage.

Access to the central processor is provided via central memory and optional groups of peripheral pro-

Advanced Microcomputer Development System

μP μP and away

Futuredata introduces the development system that sets you free.

This newest development in development systems sets you free to cope with the expanding world of μP-based product design. Free to design with the 8086, 8085, 8080, 6800, 6802 or Z-80 and free to add many other processors soon. This system puts universal hardware and software development capabilities at your fingertips: real-time in-circuit emulation to 5 MHz, real-time 48-channel logic analyzer, up to 2 megabytes of disk memory, and every software aid, including high level language compilers, relocating macro-assemblers and disassembling symbolic debuggers. CPU, CRT and keyboard are all neatly integrated in one compact, mobile station to liberate more of your bench space. It's the universal, compact, state-of-the-art AMDS — Advanced Microcomputer Development System. Futuredata, 11205 S. La Cienega Blvd., Los Angeles, CA 90045. (213) 641-7700 TWX: 910-328-7202.

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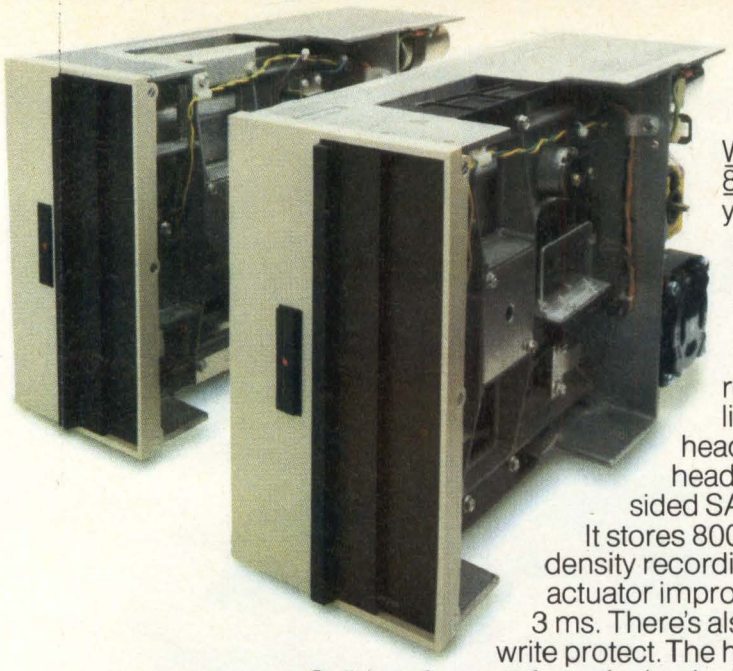
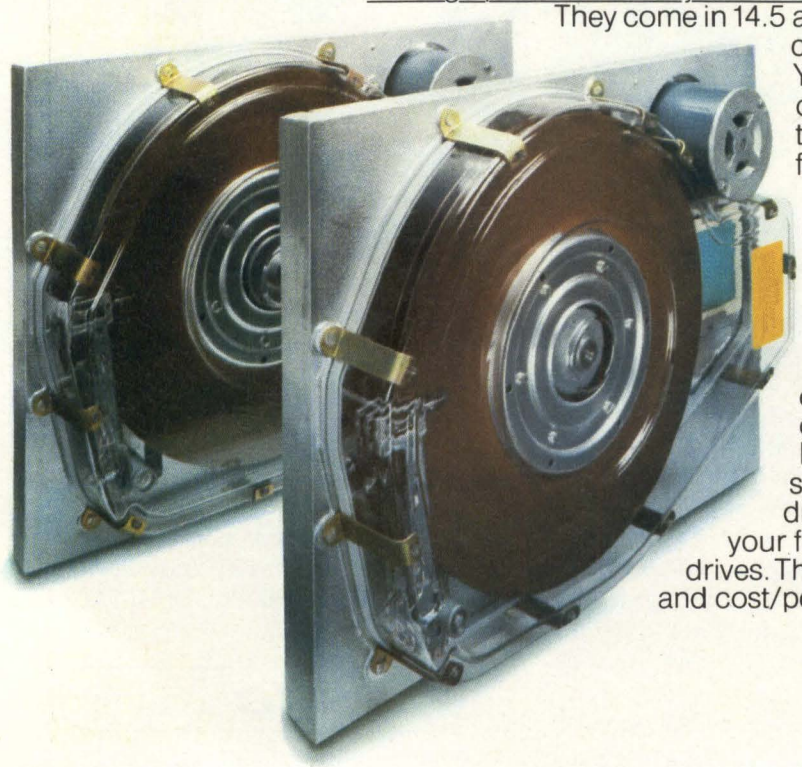
CIRCLE 20 ON INQUIRY CARD

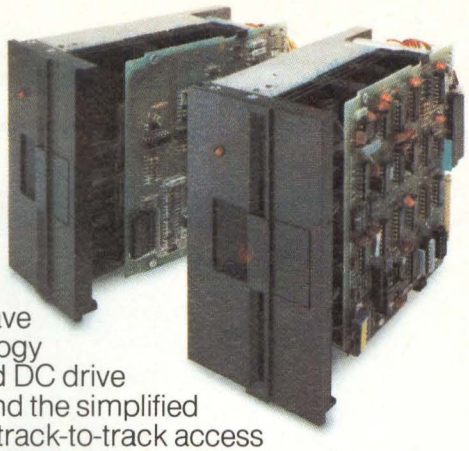


Want 400-1600 Kbytes? Choose our SA801/851 series. With the SA801 8-inch floppy, you have a choice of 400 or 800 Kbytes in single or double density, on the same drive for the same price. More than 400,000 of these standard-setting drives have been specified by OEM's around the world. They know that they can count on Shugart's proprietary read/write head technology to deliver media life of over 3.5 million passes per track, and head life of more than 15,000 hours. That's headstrong performance. And the double-sided SA851 drive gives you even more capacity. It stores 800 to 1600 Kbytes using single or double density recording. The 851's proprietary Fasflex™ band actuator improves track-to-track access time to a fast 3 ms. There's also a programmable door lock and write protect. The headstrong SA801/851. Solid performers from the leader in floppy technology.

The head
Choose your

Moving up to 14.5-29 Mbytes? Check the SA4000 fixed disk drives. They come in 14.5 and 29 Mbyte versions with the lowest cost per Mbyte in their capacity range. You can get an optional 144 Kbytes of head-per-track storage, too. And these newest members of the Shugart family of high performance, low cost disk drives use proven Winchester head and media technology to ensure better data integrity and longer trouble-free life. The Fasflex™ II band actuator reduces heat dissipation to 200 watts (typical) and requires no field adjustments. The drives weigh only 35 pounds, use only 5.25-inches of panel space, and mount easily in a RETMA rack. You can lower your systems costs too, because SA4000 drives can share a power supply with your floppy drives. The SA4000 fixed disk drives. The head of the family in capacity and cost/performance.

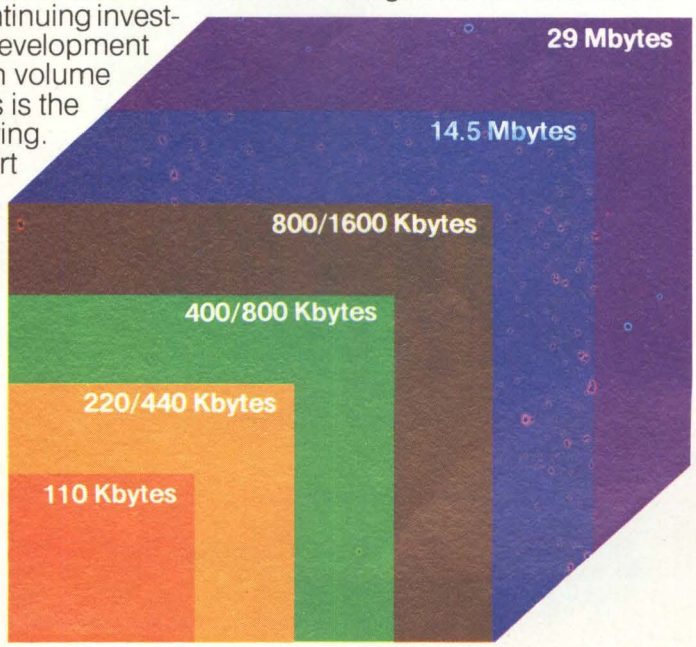




Need 110-440 Kbytes? The famous Minifloppy™ is the right choice. The Minifloppy stores from 110 to 440 Kbytes in a package about half the size of a standard floppy. We invented the Minifloppy family just two years ago and there are already well over 150,000 installed world wide. Compact size, reliability, and lowest cost per function are the reasons. Minifloppy drives have the same headstrong read/write head technology as their big brothers. The servo-controlled DC drive motor eliminates AC power requirements and the simplified actuator with direct drive spiral cam gives you track-to-track access as fast as 25 ms. The little drives offer the lowest heat dissipation of any floppy drive and feature positive media insertion, write protect, and activity light. Minifloppy. The original, and still the most popular 5¼-inch floppy drive in the world.

strong family. capacity.

The Shugart Family. Headstrong and proud of it. We're headstrong about our commitment to our customers. This means supplying you with a family of highly reliable, low cost disk drives in the quantities you need. And it means providing you with the best technical support and documentation in the industry. But it goes deeper. Like maintaining in-house control over the design and manufacture of 100% of our floppy read/write heads. And the continuing investment of financial and human resources in the development of new products and the most modern high volume manufacturing facilities in the business. This is the commitment that keeps our family growing. Headstrong? You bet. And proud of it. Shugart Associates Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 737-9241; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 176006; Shugart products are also available off the shelf from local Hamilton Avnet outlets.

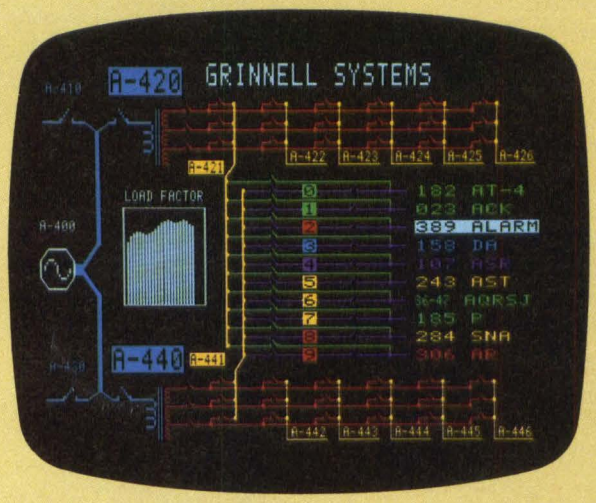


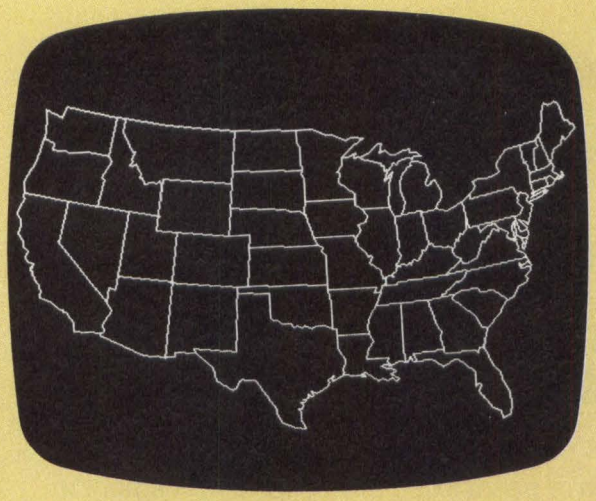
Shugart®

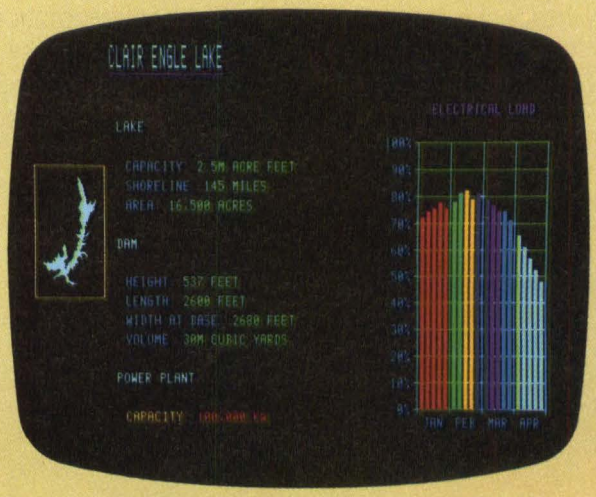
The Headstrong Company

CIRCLE 35 ON INQUIRY CARD

Vector graphics. OEM prices.







Now, with Grinnell's GMR-37 graphic display systems, you can have the resolution and input advantages of dot matrix television for about the same price as more limited character-based systems.

And, every GMR-37 display is a complete operating system: display generator, MOS refresh memory, vector and rectilinear graphics, alphanumerics in 4 sizes, bi-directional RS-232 computer interface and RS-170 video interface. Systems, including power supplies, are housed in a 7″, rack-mountable chassis and drive standard closed circuit monitors.

Four basic GMR-37 models can be tailored to fit into almost any computer-based system. Here are just a few examples. (Prices are F.O.B. San Jose, and quantity discounts are available. TV monitors are extra.):

GMR 37-10: $3300
256 x 256 resolution, one channel RGB color plus blink. (Two channels: $3700)

GMR 37-20: $3700
256 x 512 resolution, one channel RGB color plus blink. (Two channels: $4500)

GMR 37-30: $4500
512 x 512 resolution, one channel RGB color plus blink.

GMR 37-60: $4700
1024 x 1024 resolution, one channel B/W.

In addition, you can also have several economical options: independent cursors, joysticks, keyboards, special character sets and 16 bit, plug-compatible parallel minicomputer interfaces.

Further, if you ever want to move up, Grinnell has a complete line of larger systems—all software compatible with the GMR-37—to do things like animation, image processing and real-time frame grabbing.

So, if quality graphic displays are important to your product, look at the GMR-37 line. For a quotation on the system that meets your specific requirements, call or write.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

CIRCLE 36 ON INQUIRY CARD

cessors. Isolated memory facilities in each peripheral processor enable programs to be executed independently within each. Basic PPS consists of 10 peripheral processors and 12 data channels. A second optional PPS can be used to expand to 14, 17, or 20 peripheral processors overall, and includes an additional 12 data channels.

Each peripheral processor is a functionally independent computer comprising 8k 6-bit characters of MOS memory and arithmetic section that supports a full repertoire of arithmetic and I/O instructions. Depending on options, 12 or 24 data channels are serviced and each bidirectional data channel has a maximum data rate of 4M char/s.

Circle 180 on Inquiry Card

Dielectric Paper Overcomes Environmental Recording Restrictions

A dielectric recording paper that is functional within a relative humidity range from 0 to 100% enables terminal output systems to provide high quality graphic results under the most extreme climatic conditions. Introduced by Matsushita Electric Corp of America, One Panasonic Way, Secaucus, NJ 07094, the paper employs new materials and production technology to overcome the limitations of standard papers that perform effectively only in the 40 to 70% relative humidity range.

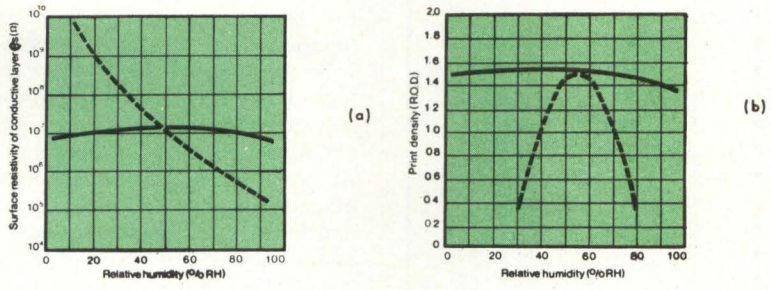
The problem of humidity extremes is solved by incorporating electroconductive materials in the conductive layer. These are principally tin, zinc, and indium oxides. Other additives adjust the conductivity of the electroconductive materials, so that the paper maintains a stabilized surface resistivity of 10^7 Ω, regardless of humidity.

In dry or humid air, standard papers undergo distortions in shape and size which affect the quality of graphic material and cause a failure to reproduce the image. For example, under desert conditions any part of a standard paper that is exposed to dry air will not reproduce the desired information or pattern. Extremely humid air has the same effect.

To overcome this, the dielectric paper uses a base paper, a conductive layer 6- to 7-μm thick, and a dielectric layer 4- to 5-μm thick. The dielectric layer is essentially a thin film of resins that are charged when placed in contact with electrodes in the printing mechanism. The conductive layer acts as the opposite electrode, depositing a pattern of electrostatically charged areas on the dielectric layer.

To form the images deposited by the electrodes, the sheet is passed through an electrostatically charged toner. Images are fixed to the paper either by heat or pressure.

Circle 181 on Inquiry Card



Graphs illustrate how relative humidity affects quality of print achieved using standard recording paper that incorporates ionic conductive material in its conductive layer (dotted lines) and Matsushita's extreme environment paper (solid line). Variation in surface resistivity with change in relative humidity (a) affects density of print achieved (b) and can cause failure to print in extreme environments

Small Business Computers Derive Power from Use of Technology

Astra series small business computers accommodate from 1 to 32 operator stations, each operating at peak efficiency in transaction processing mode. To provide high performance capabilities, NEC Information Systems Inc, 5 Militia Dr, Lexington, MA 02173, built into the systems technical advances, and supported the hardware with an integrated structure of programming languages, operating systems, and applications packages.

Key to the power of the systems is the extensive use of advanced semiconductor technology. Operator interaction with the processor occurs on a microprocessor based DMA bus at data rates of 1M bits/s. This allows a single 2000-char screen to be transferred from main memory in less than 0.1 s. Speed of the DMA controller is a major factor in the concurrent multitasking capability of the series.

CPU in the models 210, 230, and 250 is the UCOM 1600 microprocessor with a 16-bit word, 800-ns cycle time, and 114 business oriented instructions. The model 270 uses a high speed bipolar processor that is

hardware and software compatible with the UCOM 1600.

A single CRT station system, the 210 has main memory capacity of 128k bytes and supports from one to four diskette storage subsystems. The 230 supports up to four operator stations and provides main memory up to 256k bytes. Either diskette or Winchester type fixed disc drives with capacity for 20M, 40M, or 80M bytes/drive can be used.

Up to 16 operator stations are supported on the 250, which supplies up to 256k bytes of main memory. Multiple disc drives on this system can provide up to 160M-byte capacity for large database applications. Largest of the systems, the 270 can support up to 32 operator stations working concurrently. Maximum main memory on this system is 512k bytes and up to four 80M-byte disc drives may be attached.

Operator stations are intelligent devices that perform many functions on a self-supporting basis. Each has its own microprocessor, 32k memory, 2000-char CRT screen, and typewriter keypad. Separate refresh memory, attribute storage, and operator generated horizontal and vertical lines for format definition free the station for screen prompting and editing functions with host CPU support.

Supporting the hardware is an integrated structure of programming languages, operating systems, and applications packages. BASIC and ANSI 74 COBOL compilers are incorporated in each model. Also provided are a multiuser, multitasking executive, and an advanced data management system that supports formatted data entry and update, file management, report generation, and English language query functions. An integrated applications software system simplifies startup operations by providing order processing, sales analysis, inventory control, accounts receivable/payable, and general ledger and payroll packages.

Data communications facilities allow the systems to fit into distributed processing network environments. Remote workstation and remote printing protocols, IBM 2780 and 3780 batch, HASP remote job entry, and IBM 3270 bisynchronous emulators are available. Data rates up to 9600 bits/s are supported on all models.

Circle 182 on Inquiry Card

The Paper Tiger™ is here.

The Paper Tiger sets a new standard for low-cost impact printers. More capability. More versatility. For just $995.

You get a full upper and lower case 96-character set. Eight software-selectable character sizes. Plain paper, multiple copies. Forms length control. Parallel and serial interfaces. Multiple line buffer. Tractor feed. Automatic re-inking. 80 and 132 columns.

It's all standard with the Paper Tiger.

Unbeatable capability.

The Paper Tiger prints just about any paper form you need. From address labels to multicopy invoices and legal-size reports.

Adjust the tractor width from 1-3/4 to 9-1/2 inches. Choose from 8 switch-selectable forms lengths. Print 6 or 8 lines per inch.

Unmatched versatility.

Want graphics? Add the Paper Tiger's software-selectable full dot plotting graphics. Print illustrations, block letters, charts, graphs, and more.

Need a bigger buffer? The Paper Tiger features an optional 2K-byte memory that holds a full 24-by-80 CRT screen.

Feature \ Printer	Integral Data 440	Tally 1200	Lear-Seigler 300	Texas Instruments 810	Centronics 779-2
96-character ASCII set, upper and lower case	YES	OPTION	YES	OPTION	NO
Software-selectable character sizes	YES	NO	NO	OPTION	NO
Throughput, lines per minute @ 10 char./line @ 132 char./line	 275 42	 100 40	 Data not available	 440 64	 130 21
Parallel and RS-232 serial interfaces standard	YES	NO	NO	NO	NO
CRT screen buffer	OPTION	NO	OPTION	NO	NO
Footprint (W x D = sq. ft.)	1.37	3.45	3.18	3.58	2.44
Weight (lbs.)	20	64	50	55	45
Forms length control	YES	OPTION	YES	OPTION	NO
Full dot plotting graphics	OPTION	NO	NO	NO	NO
Unit Price	$995	$2500	$1995	$1895	$1350

Comparison data from manufacturers' current literature.

And there's more.

The Paper Tiger is small, lightweight, and compact. That's because it's designed especially to work in small computer systems.

And it's built rugged and simple. For high reliability and easy maintenance. Just like the thousands of IDS printers already in the field.

See for yourself.

Check the comparison chart.

Find out why this Paper Tiger just set a new standard for low-cost impact printers.

For more information, write or call. We'll send you our free brochure. Integral Data Systems, 14 Tech Circle, Natick, MA 01760. (617) 237-7610.

CIRCLE 38 ON INQUIRY CARD

Integral Data Systems, Inc.

Pack 10 to 120 megabytes in a unit one-third the size of conventional disk drives.

For OEMs and system builders, the D100 family of compact disk drives offers a surprising list of advantages. Two new models, D140 and D160 add capacity and flexibility to the proven performance of the D120. The D140 includes a 10MB fixed platter in addition to the 10MB removable cartridge as used with the D120. The D160 uses a sealed (non-removable) module which includes low pressure heads and carriage.

Small Size: Occupying approximately one-third the volume of conventional drives, models D120 and D160 measure 5.6″ × 12.2″ × 21.8″. Model D140 is slightly taller at 6.7″.

Innovative Cartridge: Both D120 and D140 models use a flat, thin (11″ square by .9″) self-ventilated cartridge weighing only 2.8 pounds.

Common Interface: The same controller handles D120, D140, D160, or any combination of the three models. One or more D160's in conjunction with a D120 provide a fixed data base with a high-throughput-10MB load-dump yielding twice the operating flexibility at half the size of conventional single-spindle drives.

High Density/Speed: Up to 7300 BPI, 600 TPI; 920 kilobytes/sec transfer rate.

Accuracy: Data-imbedded servo-tracking techniques assure accurate head positioning and full cartridge interchangeability.

Low Power Consumption: From 100 to 130 watts depending on model.

Reliability: Simplified mechanisms rule out any need for preventive maintenance. The spindle-mounted dc motor is brushless. There are no belts or pulleys, no blower, no transducer, no thermal compensation device. And no head alignment is required. MTBF is 5000 hours for models D120 and D140, 8000 hours for the D160.

Cii Honeywell Bull

For more information, send coupon to:
Jean-Paul Garodel, Bull Corporation of America, 200 Smith Street (MS 430), Waltham, Massachusetts 02154. Or call, (617) 890-8400, extension 2019.
[In Europe, write Alain Kiffer, Cii Honeywell Bull, 6 Avenue des Usines, 90001 Belfort, France. Or call, (84) 228200.]

Name

Company

Address

City State Zip

CD

CIRCLE 39 ON INQUIRY CARD

Concurrency Software Extends Distributed Data Systems

Added capabilities of the Series 21 line of distributed data processing systems include an increase in memory, price reductions for add-on memory, and concurrency software for low end systems. The additions are intended to make the systems cost-effective in applications that require more than a single terminal, but are not large enough for a second processor.

Included in the announcement, made by Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054, are increases in basic memory sizes to 48k, expandable to 96k on the 21/20 and 21/40, and 96k expandable to 256k on the 21/50. Prices of both 16k and 32k memory modules for all systems were reduced 50%.

Concurrency software for 21/20 and /40 permits simultaneous execution of programs in foreground and background modes. Single-operator station systems will be able to execute source data entry in the foreground while communications, printing, or media conversion occurs in the background. Larger configurations can execute two different foreground programs on two stations or execute the same foreground program on two stations while performing a background task.

Background programs requiring little operator intervention will run on a virtual operator station under control of an actual station, while the actual station remains free for interactive applications. When operator intervention is necessary, the operator can swap the foreground task with the background job, perform necessary functions, and return to the foreground operations.

A single station 21/20 with extended memory, concurrency software, two diskettes, and communications will sell for $11,499. A 2-station 21/40 with extended memory, concurrency, one diskette, 10M-byte internal disc, and communications is priced at $21,578. Initial shipments of concurrency software are planned for third quarter this year.

Circle 183 on Inquiry Card

Memory/Operating System Improvements Made to Desktop Computer System

Revisions to the System 45 desktop computer increase main memory capacity, speed and simplify use, and accommodate added printer and disc options. In announcing the enhanced System 45B, Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, also revealed details of 28 additional software packs that operate on the system, providing extended capabilities in structural engineering, business management, and electrical engineering.

Expansion of memory to 449k bytes, all user accessible and integrated within the desktop unit, is coupled with a 50% reduction in the cost of additional memory. Operating ease results from changes in the operating system. Among these functions are automatic transfer of tape cartridge directories into main memory and expansion of line numbers to a maximum of 32,766, which together result in an improvement in the speed with which the machine responds to user demands, and relieve some limitations on operating flexibility.

Potential for expansion has been significantly increased. Space for adding ROM options has increased from 8 to 16 slots. An Advanced Programming ROM with BASIC statements improves data handling capabilities; also added are matrix SORT and REORDER, and upper and lower case character transformations that expand programming versatility. Retained from the System 45A (see *Computer Design*, Oct 1977, p 30) are graphics, mass storage, and I/O ROMs. The I/O ROM contains additional commands to provide asynchronous data communications.

Additional options include both character sets and keyboards for French, German, Spanish, Katakana, and Swedish/Finnish languages. Peripheral accommodations provide for the HP 2631G graphics printer, a 450-char/s dot matrix impact printer that can reproduce a full CRT screen of graphic material, and the 120M-byte HP 7925 disc storage system.

Circle 184 on Inquiry Card

Configuration Management System Controls Central Switching Functions

Centralized computer control and management for large multiple processor IBM or IBM compatible complexes are provided by the 1100 computer configuration management system (CCMS) by Data/Switch Corp, Landmark Sq, Norwalk, CT 06851. The system controls all switching functions within the central computer complex.

Up to 16 individual switch matrices of different configuration sizes and types may be controlled. All connections are made via an interface control unit. Typical systems will incorporate the CPS-1000 peripheral switch matrices, DCS-2000 communications switches, and CTS-3000 coaxial terminal switches; DACS-4000 direct access control systems for control of magnetic storage devices may also be included.

The system uses an LSI-11 microprocessor with 64k 16-bit words of main memory. Online storage is provided by two floppy discs with one serving as a redundant backup for the other. A 30-char/s printer with keyboard and a CRT display with keyboard provide redundant input and output.

Operating system and applications programs operate in quiescent, configuration, and operating modes. Security codes are built into the system. Operator controllable functions include make and break single crosspoints, revertive crosspoint check, execute preprogrammed multiswitch configuration, execute systems exchange switch, status retrieval, time of day record and print, switch configuration display, and system configuration map.

Among the functional advantages of the CCMS are the FORTRAN programming language, modular software architecture, and upward growth potential. The preprogrammed multiswitch configuration provides 100 different configurations or a total of 25,600 crosspoints available to the system. Since every element of the system is solid state, a total reconfiguration change has a nominal elapsed time of 25 μs. This could mean reconfiguration of as many as 16 switch matrices. □

Circle 185 on Inquiry Card

DIGITAL CONTROL AND AUTOMATION SYSTEMS

4-Bit Single-Chip Microcomputers Serve in Automotive Applications

A number of dedicated control applications for members of a family of single-chip microcomputers were demonstrated at the Society of Automotive Engineers Congress and Exposition this year. Called microcontrollers by the manufacturer, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, each of the 4-bit COP400 series is said to contain all system timing, internal logic, ROM, RAM, and I/O necessary to implement control functions in a wide variety of applications. Onchip ROM sizes range from 512 x 8 to 2k x 8 bits, RAM from 32 x 4 to 128 x 4 bits, instruction sets from 43 to 57 commands, I/O lines from 16 to 36, and instruction cycle execution times from 4 to 16 μs.

Pushbutton Adjustable Seat

Recaro, a division of the Keiper Co Group, used a low power COP410L microcontroller chip in the design of an experimental computerized pushbutton controlled seat adjustment system. The seat can be adapted to the particular physique of each driver, adding or reducing fractions of an inch, and adjusted up and down as well as forward or backward. In addition, the back can be tilted forward and backward. Each position is programmed by four switches on a keyboard. Additional memory keys allow sets of positions to be stored in RAM for two different drivers.

The automobile's battery provides a minimal standby current to maintain the memory. Once the set of eight different positions is set, the memory retains the information even when the automobile ignition switch is turned off. When re-entering the car, the driver pushes a memory key and the seat automatically adjusts to the proper position.

In this application, the controller chip contains 4k bits of ROM for program storage, 128 bits of RAM for user programmable data storage, and 19 I/O lines. Digitized information from sensors in the seat is input directly to the chip. If the electronic system fails, the seat can be adjusted manually.

AM/FM Radio Tuning

A COP420L microcontroller, DS8907 phase lock loop (PLL) synthesizer, MM5450 serial data LED driver, and LM130 3-terminal positive voltage regulator are used in the digital tuning system for an am/fm automobile radio. Features include precise station tuning, display of exact receive frequency, keyboard entry of station frequency, storage of multiple stations in memory, pushbutton up/down scan through the band, pushbutton search (stop on next station), power-on to last station tuned, provision for time-of-day clock, static drive of LED display for noise free operation, and ability to address CB synthesizer.

The controller contains 8k bits of ROM, 256 bits of programmable RAM, and 23 I/O lines. It has a single 4.5- to 9.5-V supply voltage range, a variety of output configurations, 8-mA max current drain, and internal time base counter for realtime processing.

Emitter coupled logic (ECL) and integrated injection logic (IIL) bipolar technology are combined on the PLL synthesizer which contains 13-bit dual modulus IIL divider, ECL phase comparator, ECL prescaler, and high speed charge pump, plus 18-bit shift register/latch for serial data entry. It operates from two supply voltages (10 V for the charge pump and reference divider and 5 V for the high speed programmable divider). The IIL divider is clocked by the am input via an ECL $\div 7/8$ prescaler or through a $\div 63/64$ prescaler from the fm input.

The serial data LED display driver can drive up to four digits and was designed to specifically overcome the interference problems caused by previous LED drivers that used multiplexing techniques. Serial data entry reduces interconnections to the controller. Once loaded, the drive to the LED is static. An onchip 36-bit shift register receives the incoming data; and when the last data bit is received, the first bit loads the 34 display bits into latches. On the next half clock cycle, the shift register is cleared and ready to receive new data. An enable pin prevents data from entering the circuit from the common data bus when the IC is not selected.

Onboard Computers

Two companies have based onboard computers on COP400 microcontrollers. Both computers are applicable for use on automobiles, trucks, vans, and recreational vehicles.

One, built by Prince Corp, to aid human control by providing the driver with otherwise not readily available information, contains 36 single-function keys and switches; there are no double-use keys to confuse the driver. A calibrate mode allows the computer to be adjusted to operate with most vehicles.

Data input to the microcomputer are obtained from two transducers installed under the hood: one on the speedometer drive cable and one on the fuel line. The speed transducer converts cable revolutions per second into electronic pulses, sending them to the computer

ANNOUNCING–THE POWERFUL, NEW FPS-100 ARITHMETIC PROCESSOR–FOR THE OEM.

EIGHT MILLION FLOATING-POINT OPERATIONS PER SECOND... PRICE: $16,728*

A NEW LEVEL OF COST/PERFORMANCE FOR THE OEM is now available from the leader in array processing — FLOATING POINT SYSTEMS. If your application demands maximum floating point compute power — but at minimal system cost — the FPS-100 Arithmetic Processor can satisfy your need.

EIGHT MILLION FLOATING POINT OPERATIONS PER SECOND is achieved through a unique pipelined parallel synchronous architecture. In each 250nsec cycle the FPS-100 can produce one multiply result and one add result. And with 38 bits of precision — over eight decimal digits of accuracy!

A FULL COMPLEMENT OF PROVEN SOFTWARE is available including FORTRAN Compiler, Assembler, Simulator, Debugger, Math Library — with more than 250 routines, Signal Processing Library, a Vector Function Chainer, and the APEX host executive.

SUPER-100, A NEW RESIDENT REAL-TIME OPERATING SYSTEM introduces a new dimension to array processing. Prioritized multi-tasking and extensive services permit maximum utilization of the FPS-100. The FPS-100 with the optional Super-100 and priority interrupt structure can easily accommodate demanding real-time applications.

COMPACT and completely self-contained, the FPS-100 is only 10.5" high for quick integration into your system cabinet.

ECONOMICAL HIGH PERFORMANCE COMPUTING is now within your reach — the FPS-100 can be attached easily to a small host mini to create a Super Computer System for mathematically intensive calculations.

Contact your nearest FPS representative for more details or call Jim Strelchun, (503) 641-3151.

*OEM Quantity 100 (minimum 20 units).

FLOATING POINT SYSTEMS, INC.

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CIRCLE 41 FOR CONTACT BY FPS

"Only one DIP socket gives you all the best features. And more.

New DIPLOMATE— from AMP."

The new low profile Diplomate combines the best engineering features with AMP's own exclusive contact design innovations. Here are some of its outstanding advantages:

1. Metal-to-metal-to-metal contacts with dual side-wiping action ensure low contact resistance and excellent electrical reliability.
2. Unique closed bottom design prevents solder wicking and flux contamination for complete contact protection.
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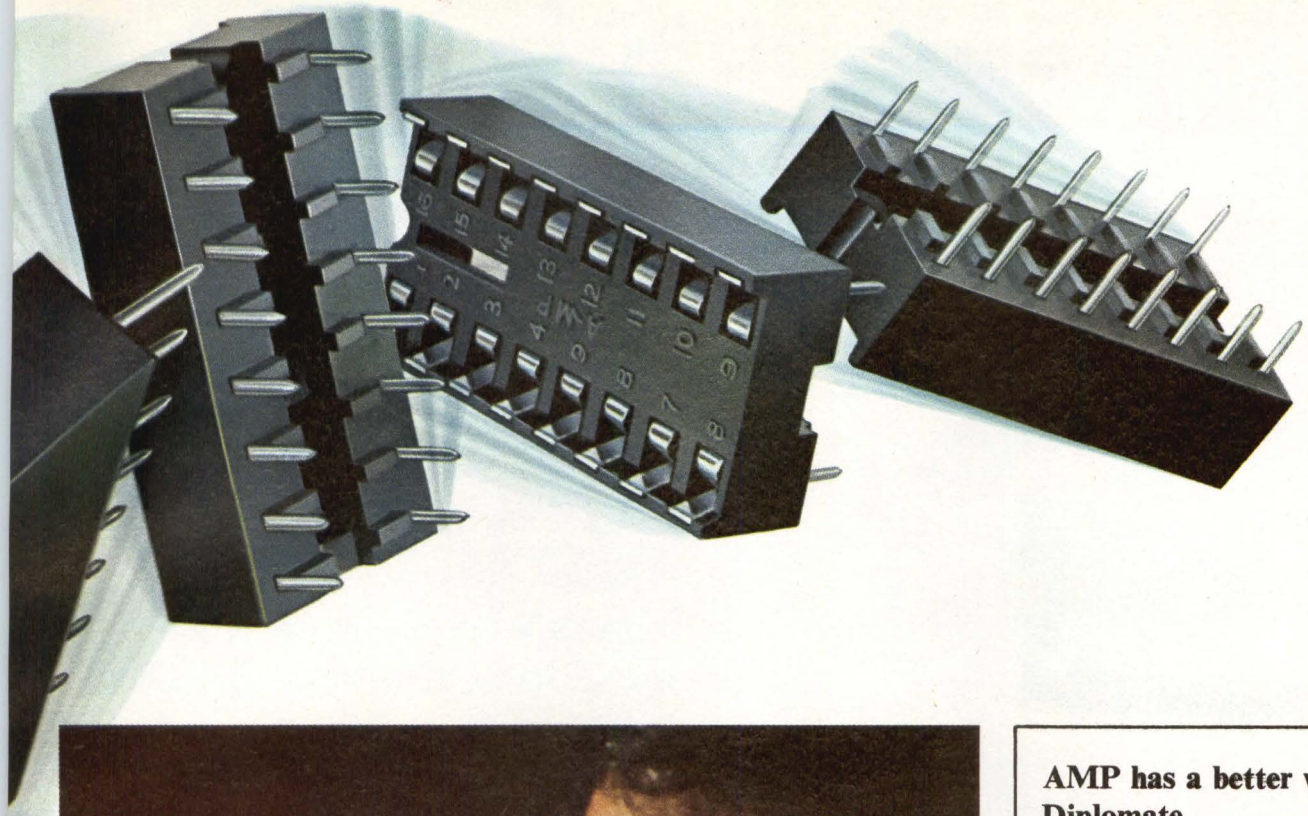

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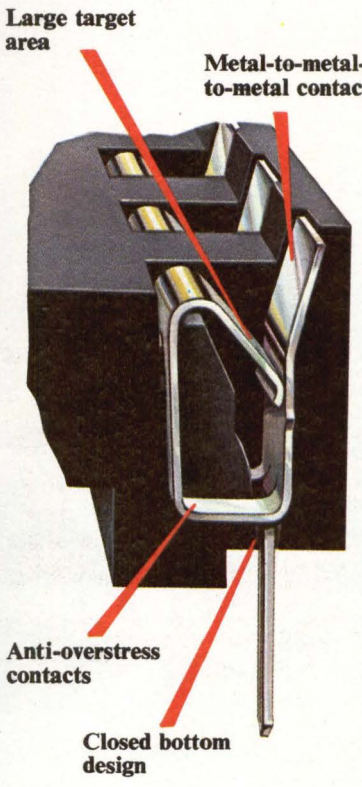

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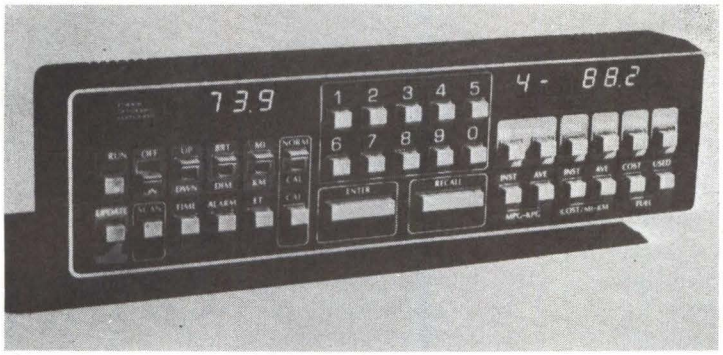
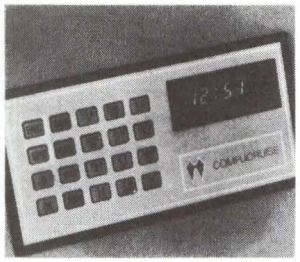




Two onboard computers based on National Semiconductor COP400 series 4-bit microcontrollers. Each supplies data on time (elapsed time, trip driving time, time of arrival, time to empty fuel tank); distance (on trip, to destination, to empty fuel tank); fuel (used since fillup, used on trip, to destination, to empty, current consumption, average consumption, efficiency); temperature; and speed, in choice of English or metric units

for calibration; the fuel transducer measures fuel flow between the fuel pump and the carburetor and converts it into digital information.

Two high intensity digital displays allow reading, day or night, in selectable English or metric units. Trip information is available (in miles or kilometers) as distance to go, distance traveled, distance on a tank or tanks of fuel, vehicle location, vehicle speed, and instant update to correct for slippery roads. The driver can preprogram trip stops and turnoffs and have an audio visual warning on the computer 1 mi (1.6 km) before they occur. Time is available as time of day, elapsed time, time alarm, estimated time of arrival constantly updated with speed, or as a stop watch function. Fuel functions are displayed as instant or average distance per unit of volume, instant or average cost per unit of distance, and fuel used to date and cost paid per unit of volume.

The other 4-bit onboard computer, Compucruise, is manufactured by Zemco, Inc. A 20-position keyboard enables the operator to specify any of 44 functions, including choices of English or metric readouts and most of those found in the Prince unit.

Among the capabilities are efficient fuel management. The computer displays the most fuel efficient driving speed; which brand and grade of fuel is most economical; effects of tire brands, types, and pressures; when tune-up and repair is needed; whether tuneups have been properly performed; and other fuel saving data. In addition, by entering expected trip distance, the controller can continually display time, distance, or fuel to arrival, all updated once a second and based on current vehicle speed and fuel consumption.

A third onboard computer, this one made by General Motors for the 1979 Cadillac Seville, includes National Semiconductor's 16-channel, 8-bit ADC0816 single-chip data acquisition system. That chip provides analog to digital interface for keyboard entry, fuel level monitor, battery voltage, engine temperature, and other analog signal data which are converted to 8-bit microprocessor data bus compatible binary words.

A preprogrammed system in the computer computes and displays operational information in three separate instrument panel areas. A digital speedometer above the steering wheel constantly indicates current operating speed and the fuel gauge reads the amount of gasoline in the tank. Other driving information is available on command to the driver or front seat passenger by depressing one of the console buttons on the computer. Included are actual instantaneous fuel economy, average fuel economy for the trip, average car speed, total elapsed trip time, driving range on remaining fuel, distance to go to a predetermined destination, as well as estimated arrival time at that destination based on current driving conditions, time of day, engine r/min, engine temperature, and system voltage.

Microcontroller Description

Various members of the COP400 family allow the user to specify an optimum microcontroller for a particular

application. RAM, ROM, I/O, speed values, and electrical characteristics can be chosen to fit specific tasks. Each device contains a number of clock, I/O, and other options mask programmed into the chip at the same time the ROM is coded with the user's dedicated program.

COP420/420L/420C devices are central configurations of the family. Each of the 28-pin DIPs has 1k x 8 ROM, 64 x 4 RAM, true vectored interrupt plus restart, 3-level subroutine stack, 23 I/O lines, 57-command instruction set, internal time base counter for realtime processing, internal binary counter register with serial I/O capability, general purpose and Tri-State® outputs, LED direct drive, and software/hardware compatibility with the rest of the family.

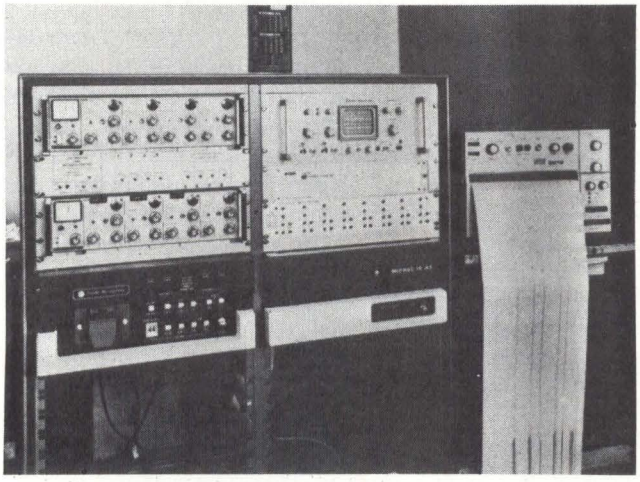
The NMOS 420 operates over a 4.5- to 6.3-V single supply range and has a 4-μs instruction cycle execution time. Operating supply current is 20 mA at 5 V. 420L uses only 40-mW max power and has a 4.5- to 9.5-V supply range, a 16-μs instruction cycle execution time, a divide-by-32 crystal clock option, and direct LED digit drive capability. 420C is a CMOS version with a 2.4- to 6.3-V operating supply range and a dual-clock mode option for operation at low speed (244 μs) with low power consumption, or high speed (16 μs) when necessary to perform internal data computations at a faster rate.

421/421L are identical to the 420/420L versions except that they are 24-pin devices having 19 I/O lines instead of 23 and no interrupt capability. 410L/411L have the same electrical specifications as the 420L/421L but only 512 x 8 ROM, 32 x 4 RAM, and 43 instructions, plus two instead of three stack levels, no interrupt capability, and 19 and 16 I/O lines, respectively. They are in 24- and 20-pin packages, respectively.

440/444L are expanded versions of the 420/420L devices, with the same instruction set but double the memory (2k x 8 ROM and 128 x 4 RAM). The 28-pin 444L has 24 I/O lines and the 40-pin 440 has 36. The 40-pin 402 and 404L are ROM-less versions of the 420 and 440L, respectively, available for prototyping a 400 system. They are also used for small volume applications requiring up to 1k x 8 and 2k x 8 bits of external ROM.

Microcomputers Replace Mainframe For Test System Signal Processing

Realtime processing of data from the wheels of a high speed railway vehicle is accomplished in a system commissioned by the British Rail Research and Development Division at Derby, England. British Rail retained responsibility for all basic research and definition of signal processing algorithms; however, system implementation and detailed software development was accomplished by Plessey Microsystems, Water Lane, Towcester, Northamptonshire NN12 7JN, England.



Part of instrumentation for realtime signal processing in railway vehicle wheel monitoring system. Similar configuration, containing Miproc 16-AS microcomputer, is dedicated to each of two wheels in test vehicle. Realtime microcomputer system replaces offline system that required mainframe computer

The British Rail sig al processing system provides information used to design vehicle suspensions that optimize the interaction between railway wheels and the track but still ensure adequate stability at top speed. In the previous system only indirect measurements of suspension forces and vehicle ride accelerations were available, and recorded raw data were processed offline.

In addition, that method required signal processing by a mainframe computer, while the realtime system uses only two microcomputers. Data acquired from the wheels, which serve as transducers for measurement of wheel/rail forces, are processed by the pair of microcomputers and then output to a chart recorder or other analog recording device. Continuous scaling corrections are performed to compensate for complex calibration characteristics of the rotating transducers (wheels).

System hardware consists of two standard Miproc 16-AS microcomputer modules, one dedicated to each of a pair of axially opposed wheels on the test vehicle, plus special hardware developed for this application. Separate analog signals proportional to vertical, longitudinal, and lateral wheel/rail forces, obtained from an array of strain gauges mounted on the wheels, are

New high resolution graphics from the leader in low-cost color.

With our 8001G graphics terminal, ISC pioneered low resolution color graphics at black and white prices. Now we're able to offer the world's most cost effective high resolution capabilities – at prices that are true-to-ISC tradition.

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The high resolution graphic hardware consists of 512 software programmable characters, each comprised of a 6 x 8 dot matrix with all 48 dots addressable by software. This translates into a 480 x 384 resolution for random vectors and symbols, resulting in a 6x improvement from the standard 8001G.

Three main modes of operation are available, including a special character mode, ISC standard plot mode, and the high resolution plot mode for drawing bar graphs, vectors and point plots. Eight brilliant communicative colors are at your disposal, to convey information quickly and accurately, with critical control over detail.

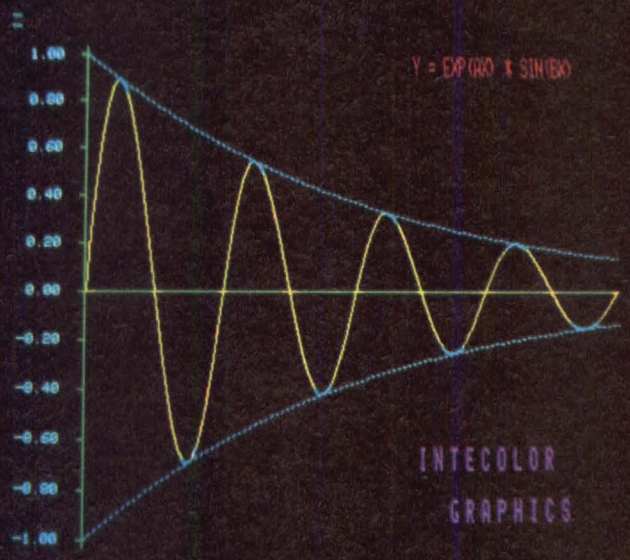
The 8001H has an 8080A microprocessor capable of handling data on a two megahertz processing cycle. It provides 2K of ROM, RS-232C interfacing capabilities, and flexible editing made still easier by a keyboard with color and numeric key clusters.

And its cost is nothing short of phenomenal. $3650 is all you pay for a single unit; $2500 each for 100 or more.

If you'd like to upgrade your present 8001G units to high resolution, hardware and software options are available for as little as $1500 per single unit; $1000 for 100 or more. All Intecolor terminals are covered by a six month warranty, and cash with order guarantees delivery of a single evaluation unit at the 100-unit price within 30 days, or your money back.

If you need high resolution color, but have found the cost prohibitive, here's your opportunity. Now that Intecolor is perfectly capable of high resolution color, you can be, too. Call your ISC rep today.

Color Communicates Better



Unretouched photo of screen

*U.S. domestic prices

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No matter what major microprocessor you are using in product development or in production test, the MicroSystem Analyzer is the one universal and portable instrument for you.

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sampled at a 4-kHz rate and the samples are digitized to 12-bit precision for subsequent digital processing.

The system logs, processes, and displays or records the three forces in realtime for vehicle speeds up to 120 mi (209 km)/h. Because the transducer configuration for vertical force measurement, chosen for stability and sensitivity, generates an output signal which for constant force input varies substantially as a function of wheel rotation, a set of previously measured calibration coefficients is applied as compensation. Interpolation between calibration points provides the necessary degree of accuracy.

Although lateral and longitudinal force signals are quite pure, the vertical force signal contains considerable cross-modulation components of the other force signals. These unwanted components are removed by the signal processing algorithm to yield a true reconstructed vertical force signal.

Circle 160 on Inquiry Card

Integrated Control System Expected to Ease Mexico City Traffic Congestion

A record size computerized traffic control system has been ordered for the Mexico City (Mexico) Traffic Authority from Philips Telecommunications Industrie BV, Hilversum, The Netherlands. Valued initially at 29 million Dutch Guilders (14 million U.S. dollars), the contract is said to be the largest so far awarded in the traffic control field. In its first phase the integrated system involves 1000 intersections.

The system will be configured around the Philips P857 computer, which will control, monitor, and supervise overall traffic movement at all intersections. Dynamic operating intelligence will be decentralized in 25 secondary processors allocated to subareas, each of which will coordinate and supervise groups of intersection controllers. Several thousand detectors will be deployed at strategic points to collect the traffic data necessary for efficient regulation and flow continuity.

Because of the hierarchical system configuration, which includes local site microprocessors, the project will benefit from computer control even in its early stages. If a fault develops in the central computer, continued 2-way transfer of traffic and control data will remain assured between the lower levels of the system, thus minimizing the risk of disruption in traffic control.

The initial phase of the traffic system project, which will be extended in steps to include an additional 600 intersections plus the necessary cable network, is scheduled for completion in 1980 with the first subareas operational in mid-1979. This traffic control project is part of an overall plan instigated by the Mexican authorities to solve the problems of traffic congestion, air pollution, and waste of energy.

Circle 161 on Inquiry Card

DC&AS BRIEFS

Modules Increase Capabilities of Microcomputer Family for Industrial Application

A group of memory and I/O expansion modules announced by Texas Instruments Inc, PO Box 1443, Houston, TX 77001, for use with TM990/9900 family microcomputers is intended for industrial applications. Included are boards with up to 64k bytes of dynamic RAM, I/O boards for up to 64 channels, combination memory and I/O boards, and I/O units that enable the microcomputers to interface directly with ac or dc signals or loads.

TM990/203 is available in three models: -21 provides 16k bytes using 4k x 1 TMS4027 dynamic RAMs; -22 provides 32k to 64k bytes with 16k x 1 TMS4116 RAMs, and -23 provides 64k bytes with the 16k x 1 RAMs. All models have a parity option with parity indicator light and interrupt signal, as well as jumper selectable access times and cycle steal or transparent refresh modes.

Data and address bus interfaces are 3-state TTL compatible; control bus interface is TTL compatible. Memory device access time is 250 ns and cycle time at 3 MHz is 0.667 μs. Operating temperature range is 0 to 70 °C.

Analog I/O expansion modules include four input only, two output only, and three combination I/O. TM990/1001 provides 16 single-ended or differential input channels expandable to 64 single-ended and 32 differential input channels. It features switch programmable input configuration, has an onboard dc-dc converter, provides for eight 0- to 50-mA current inputs, has 15 interrupts, and offers ±25% full-scale accuracy at full throughput rate of 30 kHz with 12-bit resolution.

The /1002 is a low level input module with 16-bit ADC. Features include excellent accuracy, linearity, and stability; thermocouple cold junction compensation and linearization; and environmental immunity. One version is offered for J type thermocouples, another for K type. A similar module, /1240, provides 16 single-ended or eight differential input channels, expandable to 32 and 16, respectively.

A /1243 high level analog output module provides eight channels of analog output and eight high current logic driver outputs, eight 12-bit DACs with input codes and output ranges independently selectable, and onboard 10-V precision reference. The /2001, another output module, has four output channels.

The /1241 combination analog I/O interface module has up to 32 single-ended or 16 differential input channels and two channels of 12-bit analog output, and onboard 10-V precision reference. Version S has 1, 2, 4, and 8 programmable gain while the version R has 1 to 1000. In addition, the /3001 features 32 single-ended or 16 differential input channels and two output channels.

Output codes for all nine I/O modules are binary, offset binary, and 2's complement. Each features 15 interrupts. Throughput rates are 30k channels/s for the /1001 and /3001, 10 samples/s for the /1002, and 40 channels/s for the /1240, /1241S and /1241R.

A combination memory and I/O expansion module, the /305 provides memory capacity up to 32k bytes. Eight 24-pin memory sockets can accommodate TMS2516 2k x 8 EPROMs, TMS2532 4k x 8 EPROMs, or 24-pin 2k x 8 static RAMs. The board has 32 optically isolated I/O lines, 16 dedicated parallel input lines, and 16 user configurable parallel I/O lines. Memory map configuration is jumper selectable. Input to output isolation is 500 V.

Series /5MT ac and dc I/O modules are available in four types: ac input, dc input, ac output, and dc output. An ac or dc input module converts ac or dc signals from pushbuttons, limit switches, and other pilot devices into low logic levels that are compatible with levels required by the microcomputer modules; an ac or dc output module converts microcomputer logic levels into high ac or dc output signals to drive loads such as motor starters, contactors, positioning valves, and pilot lights.

Circle 162 on Inquiry Card

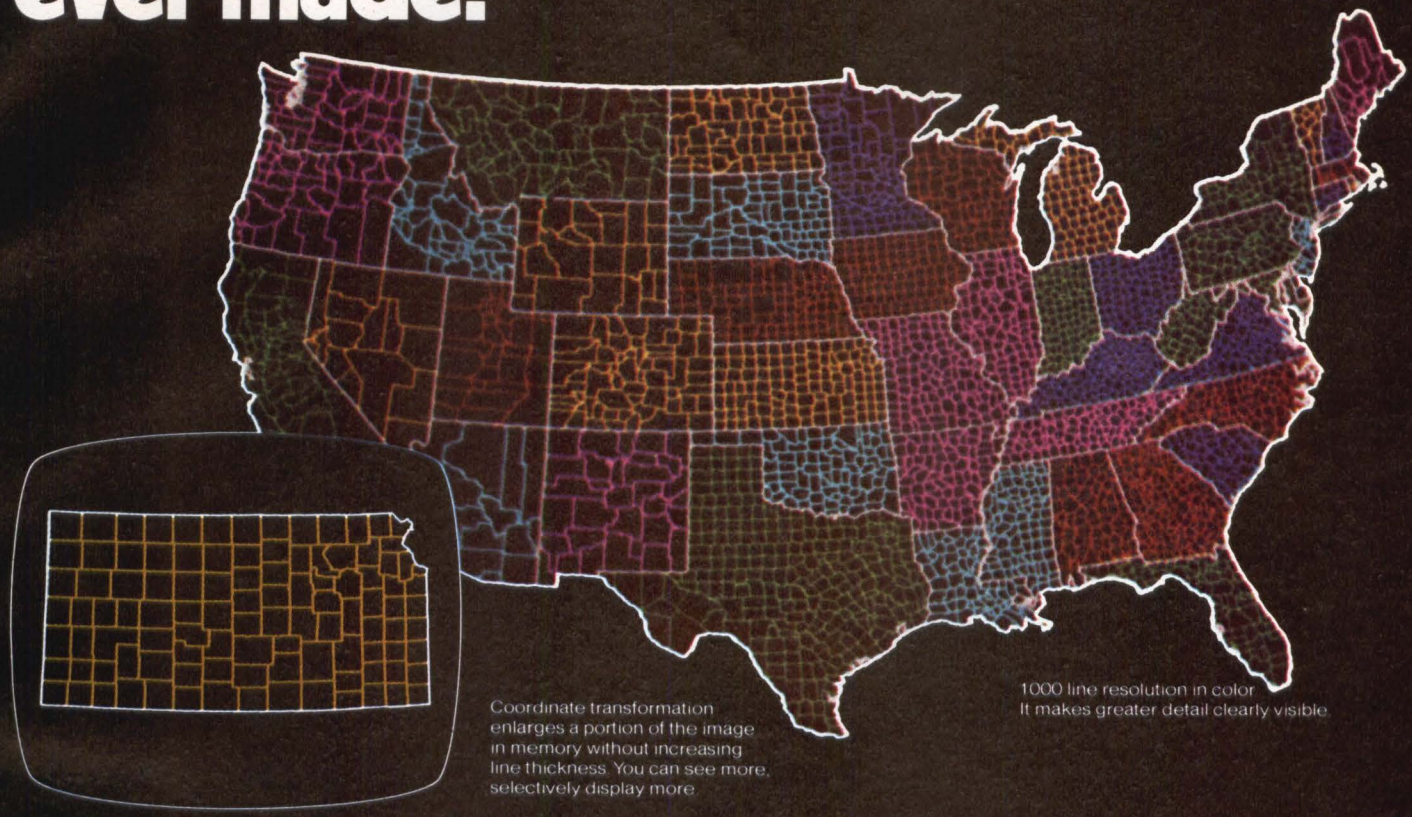
Energy Demand Control Systems Reduce Electrical Costs

Two electrical demand control systems have been developed by Avco Electronics Div, 4807 Bradford Dr, Huntsville, AL 35804. The 7700 EDACS (energy demand and control system) monitors and controls electrical usage under computer control in buildings to minimize energy costs. PEDALS (power electrical demand and load shedding), in contrast, was developed for industries that use large amounts of electric power and typically contract for supplemental power on a demand limit pricing schedule.

Based on a system concept, EDACS includes sensors and actuators for remote measurement and control, distributed computer intelligence via localized field panels, communications from each building to a centralized location, a central computer system with building management operation and control interface, and all software necessary to optimize start/stop of equipment, chiller control, electrical demand peak load shedding, and enthalpy control for maximum energy cost savings.

Each remote field panel and remote unit processor has complete microprocessor intelligence and can perform all local control at maximum system efficiency as well as take over in case of power failure. Each remote processor can accept any combination of digital or analog input for sensing applications and provide any combination of digital and analog outputs for system control applications. The processors also can be software downloaded, via the communication lines

Ramtek introduces the most powerful raster graphics and imaging display system ever made.



Coordinate transformation enlarges a portion of the image in memory without increasing line thickness. You can see more, selectively display more

1000 line resolution in color
It makes greater detail clearly visible

Here's the Ramtek 9400. Finally, a display that combines raster color, 1000 line resolution, coordinate transformation, high-speed graphics and more—all in one package.

It's colorful. More than 16 million color possibilities thanks to raster scan technology. Or, choose black and white or gray scale.

It's fast. Vector writing speeds are greater than 16,000 vectors a second with 50 pixel average vector lengths.

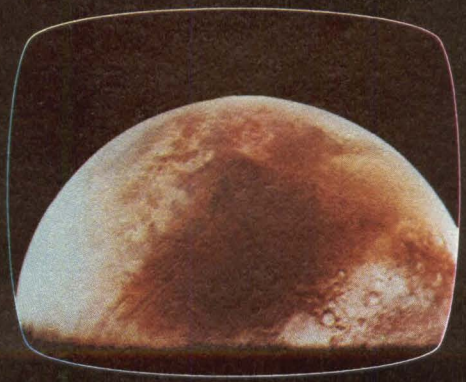
It's sharp. At the top of the line you can display—in color—1024 scan lines of 1280 elements.

It's powerful. Local spatial transformations include translate, rotate, scale, pan and zoom. You can store and deal with pictures that are much larger or more detailed than can be displayed at one time. De-cluttering allows greater detail to be displayed as the picture is enlarged or less as it's reduced.

It's convenient. Subpictures and special symbols may be down loaded and stored in user memory. Pictures from display lists can be clipped to arbitrary viewports on the display surface.

It's interactive. Subpictures can be called by keyboard function keys. The entity detection feature identifies graphic procedures and instructions that draw objects pointed out by the operator. Interactive controls include a general purpose keyboard, trackball, joystick, light pen and tablet.

It's more than one. The 9400 system is seven different models offering resolution from 256 x 640 to 1024 x 1280. All with the same powerful range of capabilities for command and control, process control, mapping, computer aided design, remote sensing—or any application requiring the ultimate in graphics and imaging potential.



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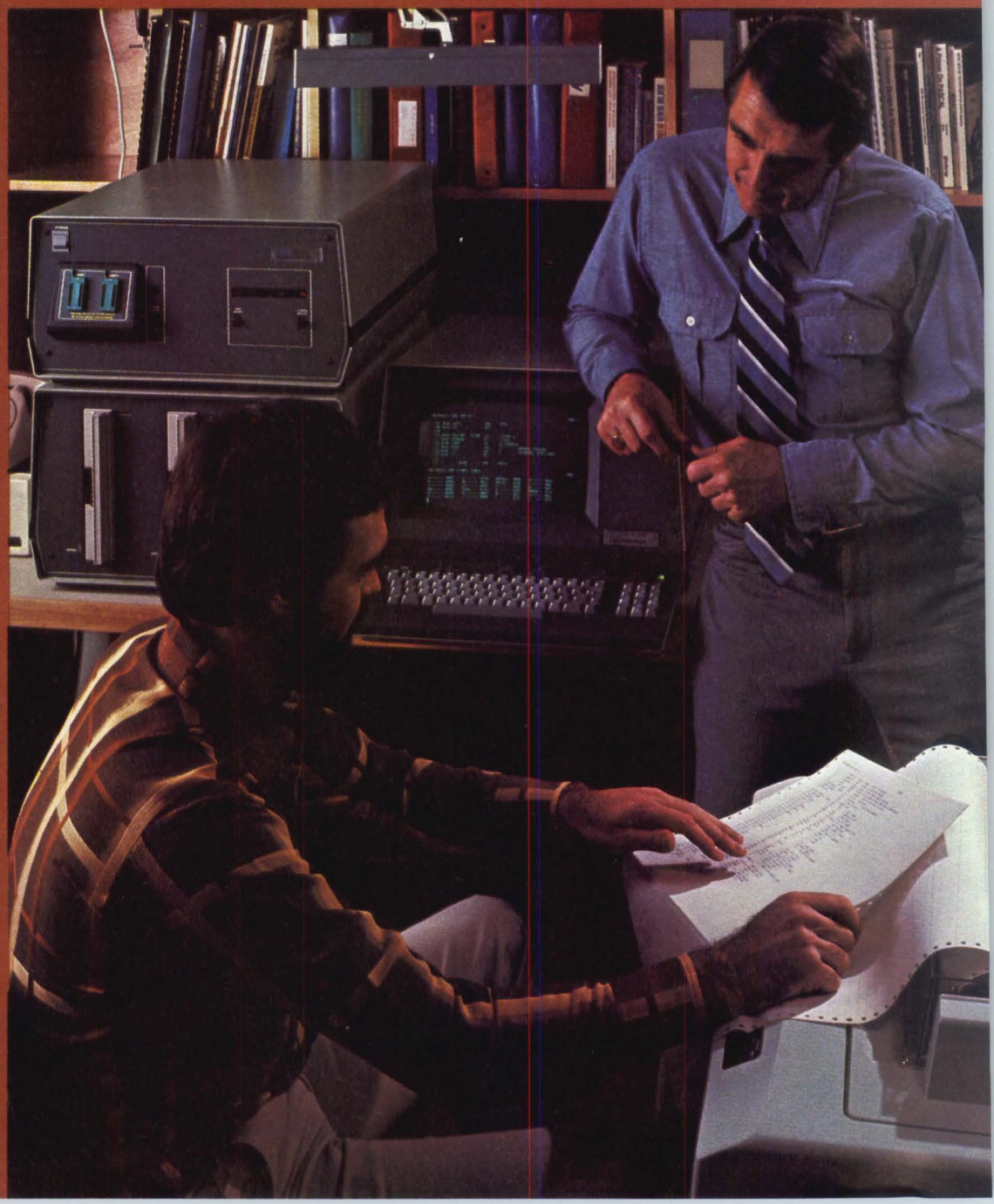

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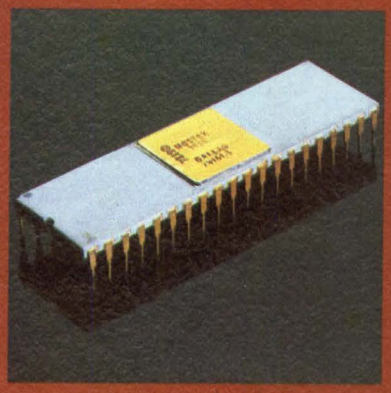

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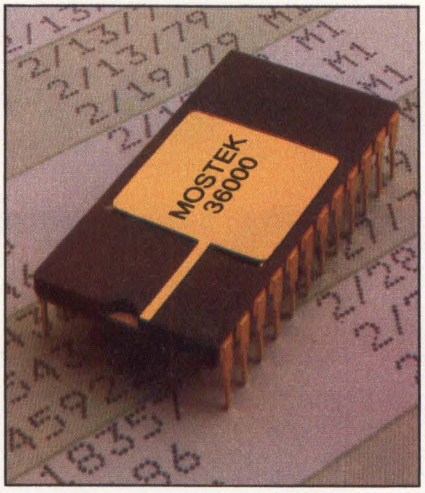

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from the central facility, to perform any of the host computer application programs for the local equipment.

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Some power loads must run continuously while others are required only intermittently to sustain plant operation. Intermittent loads can be dropped or "shed" without seriously impairing plant operation. PEDALS controls a set of priorities to automatically shed loads as the end of a power demand period approaches so that the demand limit will not be exceeded.

At the beginning of each demand period and every following 3 s the computer checks the tieline current direction and magnitude, enabling the system to automatically limit the tieline current to a value set by the operators. If the tieline current goes above this limit in the "in" direction, the generators are stepped down. This controller overrides all other control of the generators.

When there is no tieline limit, the generators are manipulated to make the purchased power follow the "generator line." If purchased power is above this line, the generators are stepped up; if purchased power is below, the generators are stepped down.

At the beginning of each demand period, all loads are put online. Every 6 s the computer checks the purchased power and takes appropriate action on the loads. Loads are manipulated to make the purchased power follow the "load line." If the purchased power is above this line (positive) and headed away by more than a threshold, loads are dropped; if the purchased power is below (negative) and headed away from the line, loads are added.

Circle 163 on Inquiry Card

Video PLL Module Meets Control Environment Requirements

A phase lock loop module, claimed to be the first device in the industry that allows a user to synchronize a video display board to a TV camera, master sync generator, or other external sync source, has been introduced by Matrox Electronic Systems Ltd, 2795 Bates Rd, Montreal, Quebec H3S 1B5, Canada. The PLL-01 module is intended for use with video display and interface boards in industrial control environments where alphanumeric and/or graphic data must be overlaid on a TV camera picture.

Only a single 5-V power supply, such as obtained from a video RAM to which the module interfaces, is required. The 3 x 3.5" (7.6 x 8.9-cm) unit consists of two main parts—horizontal phase lock loop and vertical reset delay—that control horizontal and vertical timing. Onboard timing permits the user to adjust the position of the video display output relative to the reference sync. Either composite or separate syncs will be accepted. The unit will lock to a single TTL level composite sync signal.

Circle 164 on Inquiry Card

ADC Module Increases Capabilities of Programmable Controller

An ADC module is now available for the MaxiMiser programmable controller made by Cincinnati Milacron, Mason Rd & Rte 48, Lebanon, OH 45036. The plug-in board fits any slot in the controller's card cage and converts graduated analog input signals into digital inputs that can be processed by the data arithmetic module. Each input channel in the ADC module has its own independent instrumentation amplifier which can be resistor programmed for gains from 0.1 to 1000 and for either voltage or current input.

Circle 165 on Inquiry Card

Data Acquisition System Handles Multiple Inputs

System 3500, a multiple input data acquisition and control system from LeCroy Research Systems Corp, 700 S Main St, Spring Valley, NY 10977, is directly CAMAC compatible, including all necessary hardware and software for interfacing with any CAMAC module. An 8-slot CAMAC minicrate is integral and up to 11 external CAMAC crates can be supported by the system.

Setup parameters are graphically displayed on an integral display, and parameter selections are implemented by an interactive lightpen that prompts the user to enter appropriate numerical entries on the ASCII keyboard. Routine and frequently used display operations are implemented by an understandable direct reading 22-function keypad. Built-in processing capabilities include add, subtract, smooth, differentiate, and normalize, all of which are predefined and implemented by a lightpen command.

Adding a model 3921 dual floppy disc provides a fully programmable system with extensive programming and processing capability. Either FORTRAN or BASIC programming languages are available for writing CAMAC control programs as well as user defined data analysis routines. Analysis of previously acquired data or writing new programs can be performed concurrently with high speed acquisition.

A standard system contains 64k of computational memory; 8k of DMA data memory expandable to 64k; a 9" (22.9-cm) CRT for display of data, graphics, and listings; ASCII keyboard; 22-function keypad; lightpen; 8-module CAMAC minicrate; and RS-232 I/O port. Accessories include dual floppy disc, the GPIB I/O port, and software packages.

Circle 166 on Inquiry Card

Machinery Function Controller Operates Online

Simultaneous online monitoring, timing, control, and coordination of machine systems and functions, without the need for encoders or resolvers, are said to be capabilities of the angle resolving controller. Introduced by Kadoc Registration and Control Corp, 1350 Main St, Lynnfield, MA 01940, the microprocessor based unit provides multichannel control of continuous or single-cycle timing and phasing of rotary cyclical motions in machinery. Its basic program provides advance/retard/rate change plus up to eight optional channels with open/closed loop electronic cams or servos. The standard 11 x 9.5 x 12″ (28 x 24 x 30.5-cm) unit can handle as many as eight sensors.

Circle 167 on Inquiry Card

Distributed Process Control Systems Permit Expansion of Control Levels

Among the presentations at Petro Expo '79 were two distributed process control systems. Both are microprocessor based and can handle multiple I/Os. In addition, the users of either system can start with a basic entry level configuration expandable later to a more sophisticated system that can handle additional process units.

Multivariable Format

Beckman Instruments, Inc, 2500 Harbor Blvd, Fullerton, CA 92634, introduced the MV 8000 system featuring an architecture that combines single-loop and shared digital processing with redundant CRT displays. Included are multivariable control units (MVCUs), multivariable I/O units (MVIOs), an interactive noncomputer supported plant graphics library, an alarm priority structure, and historic trend capability.

Up to 40 algorithmic functions can be processed on the MVCU. Internal components are redundant; if a malfunction or failure condition occurs, duplicate circuits assume control until the problem is corrected. The MVCU alerts the system operator via the CRT that this condition exists, diagnoses the trouble, and specifies the location. Throughout this phase the process loops continue to operate.

For multiplexing functions, the MVIO offers the same analog and digital I/O structure as the MVCU. However, it has no algorithmic function capability. All communications within the system between remote controllers and the central control room take place over 16 redundant data highways using ASCII RS-232-C interface ports. Controllers can be located at distances of up to 5000 ft (1500 m) from the central CRT displays.

For small, simple processes, the control system offers single-loop hybrid analog/digital control with existing series 8800 controllers, and multiloop digital processing with multivariable controllers, or a combination of both. For more complex multiloop digital processing needs where dedicated control is preferred, the system can be configured with the MVCU for continuous or batch processes. The MVCU offers up to 32 analog inputs, 16 analog outputs, 32 digital inputs, and 32 digital outputs.

Up to 99 selectable 8-color representations of a plant's loops, viewed on 19″ (48-cm) CRT screens, enable the operator to physically manipulate process control loops. To review immediate or past process performance, historic trending times of 10 min, 100 min, 8 h, and 24 h are standard. The operator can routinely select a process loop and change specific process rates at remote locations by using a lightpen or keying the required command into the keyboard without leaving the central station.

Circle 168 on Inquiry Card

Hierarchical Family

Fischer & Porter Co, 312 Jacksonville Rd, Warminster, PA 18974, showed the DCI-4000, in essence a hierarchical family of products that can be assembled to provide the precise degree of needed control for continuous or batch processes of any size. A functional entry into distributed control can be made for a process unit as small as eight loops, at less cost than for a conventional panelboard of comparable capacity, and without disrupting conventional control of other process units in the same plant. Later, this system can be expanded to take over control of additional process units, including implementation of high level control strategies.

The system uses a hierarchy of microcomputers and a central minicomputer to apportion control functions at every level of the process. At the basic level, a local operator's panel (LOP) combines with one to four distributed control units (DCU) to form a complete control system for 8 to 64 loops in continuous and batch processes. In addition to performing all the functions of a conventional panelboard, including up to 128 analog and digital displays, this level also provides the capability for high speed communications with higher level devices through a data highway.

At the operations level, a central operator's panel (COP) displays as many as 512 variables and provides access to as many as 256 control loops, from as many as 16 DCUs located on one or two data highways, each of which can be 1.2 mi (2 km) long. The COP performs all the functions of the LOP and can generate special graphic displays for up to 128 process variables.

At the supervisory level, a central computer can be used in addition to or instead of one or more COPs, depending on the size of the distributed control system. The computer implements high level control strategies by passing instructions to all system DCUs and collects information for data processing. □

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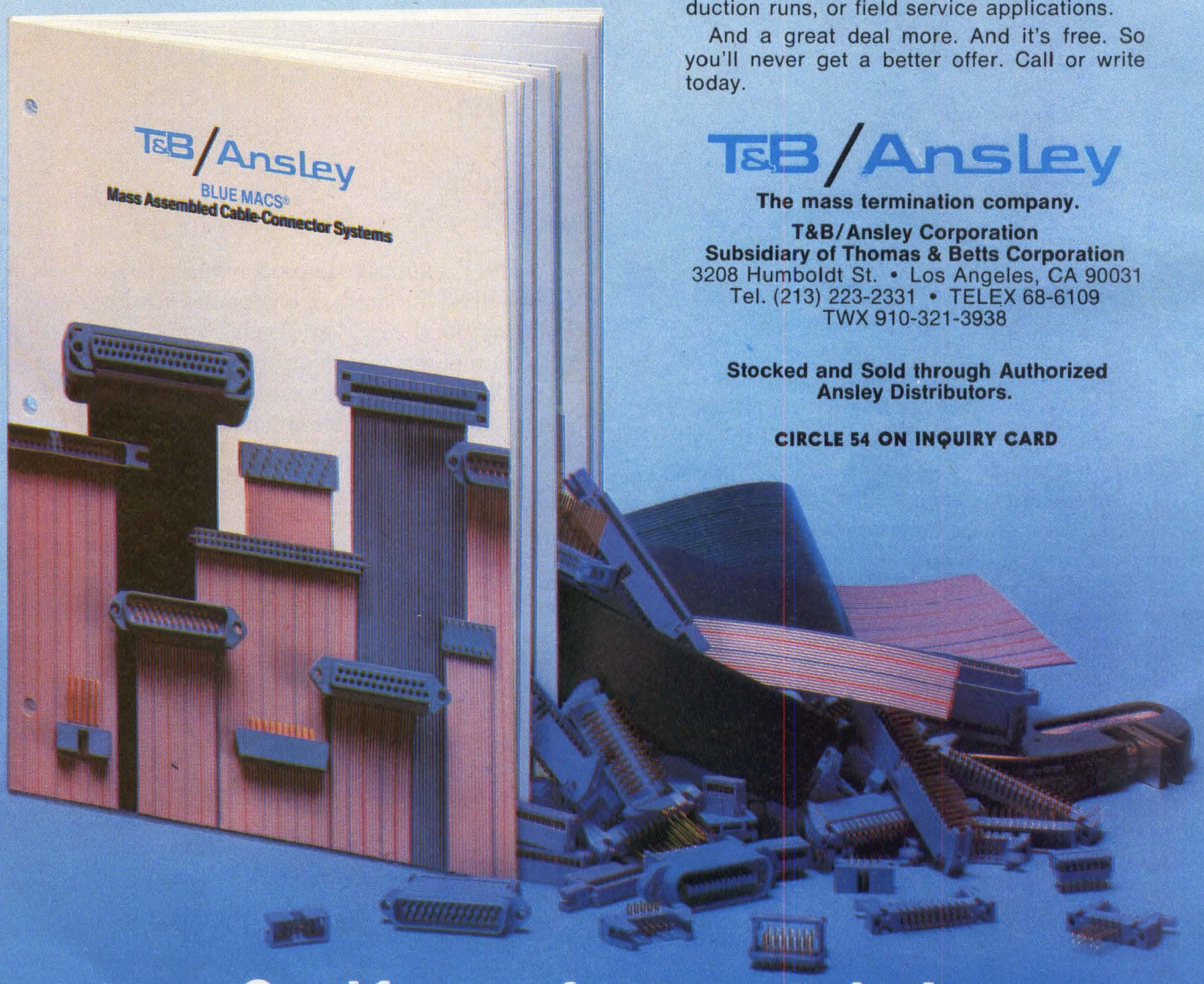

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SPEECH RECOGNITION TECHNOLOGY

Overview of current automatic speech recognition technology examines primary characteristics of installed systems and evaluates benefits and short comings

E. Joseph Simmons, Jr Threshold Technology, Incorporated, Delran, New Jersey

Ever since the computer became an integral processing element, scientists and engineers have been seeking a method of feeding verbal data directly into its memory for storage, computation, and output. Automatic speech recognition technology has achieved this goal in offices, warehouses, and factories, and has proved its merit in a variety of applications. In one such system, microprocessor based voice terminals, capable of replacing intelligent video display/keyboard stations, are linked with central processors to provide complete voice data entry systems suitable for cost-competitive source data entry applications.

Historically, operational requirements of the machine dictated communication with computers. To control machines or computers, designers and users learned the programming language of the machine or the manipulation of panel switches or keys in proper sequence and format. Any deviation from this unnatural machine input produced errors, which were not always easily detectable because of the complexities of the input/output (I/O) rules for man/machine communication.

Development of voice recognition systems permits humans to talk information directly into a computer, with no intermediate keying or handwritten steps involved, and to control mechanical systems with voice commands. Voice input to machines is simple since the operator provides instructions in a natural language—the spoken word. The automatic speech recognition (ASR) system translates these words to computer compatible data or machine commands.

Speech Response

A brief review of speech response technology serves as a frame of reference for comparison with speech recognition technology. Speech processing distinguishes between automatic speech recognition (ASR) or voice data entry (VDE) systems and speech (audio or voice) response systems. Speech response, a comparatively old technology, is encountered in several daily activities. For example, a recorded message results when a telephone number is dialed incorrectly, or responds to a telephone inquiry for a time or weather check.

Speech response can be accomplished by either of two basic methods: speech synthesis or stored speech. Both can be either analog or digital. Speech synthesis typically formulates computerized speech from fundamental descriptive phonetic units. This technology is normally used in large vocabulary systems that change frequently. Stored speech uses human voice recordings, and is usually found in small, stable, vocabulary systems. Speech is stored using a data compression technique; this technology is available on chip sets.

In speech response, research and development activities comprise technological refinements directed at low cost and application proliferation, and contextual and situation analysis refinements of input text in terms of syntax, semantics, and environmental situations.

Human Speech Factors

The problems and challenges encountered with ASR differ greatly from those of speech response. Consider normal conversation. A speaker rarely repeats words in exactly the same manner, and words are not always heard by the listener in the same way. Pronunciation, pauses, background noise, speed, amplitude, and environmental and personal stress levels vary considerably in their individual contribution to both speaker and listener. To further simplify the understanding processes—

the objective of human speech—the listener provides subtle but definite, on-going feedback mechanisms. A facial expression, a head tilt, eye contact, and hand or body motions are some indications of verbal comprehension and acceptance. A more direct mechanism occurs when the listener requests that the speaker repeat or clarify. Then again, there is contextual association, as when a speaker mistakenly says, "I need tree circuit boards." Although the listener hears "tree," the correct word is immediately substituted. A high level mental function enables the listener to "know" what the speaker meant. Similarly, the listener weighs the words, appreciates the concept, or provides understanding for what the speaker is trying to convey by responding positively to the projected emotion. Empathy aids both speaker and listener. Perception of environmental, stress, emotional, and psychological pressures clearly increases understanding.

In examining ASR, using the human as a model, what can be duplicated and what must be compensated? More specifically, what physiological understandings are required, and which can not be duplicated? In humans, the processes of hearing are understood with two important exceptions: the process that codifies sound information for transmission to the brain, and the decodification process whereby the brain correlates transmitted information and makes a "recognition decision."

The high level mental processes associated with total contextual determination, or understanding, are beyond the ability of any machine to duplicate, artificial intelligence notwithstanding. To what extent context influences a given "word-recognition" decision is still uncertain. Everyday experience demonstrates that spoken words can be phonetically ambiguous even when clearly separated and articulated in a low background noise situation. In "normal" or conversational speech, where inflections and word boundaries change, recognition is even more difficult because it is unrealistic to require that everyone pronounce words in the same way. Individual difference will always exist; it is incumbent upon technology to adjust to human differences.

Speech Recognition Technology

Approximately 90% of today's installed ASR base combines these speech technology characteristics:

Isolated word—recognizes words, letters, numbers, and short phrases that are separated by 100-ms pauses

Speaker adaptive—recognizes any speaker using any language, provided voice patterns for all words in the transaction dictionary are stored for comparison

Limited vocabulary—accommodates a relatively small set of utterances for a given transaction, the size of which is a function of present microprocessor speeds and memory sizes

Terminal interface—voice data entry to computers and voice keyboard to displays or printers.

Alternatives—continuous vs isolated word, universal vs speaker adaptive, and large unstructured vs limited vocabulary technologies—are available, but exhibit operational limitations.

Universal, Isolated, Limited Vocabulary Systems

A universal type system recognizes words spoken in a specific language by any speaker. Individual voice patterns are not stored for comparison processing to make a recognition decision. A speaker's words are compared against averaged or merged patterns, whereas in speaker-adaptive systems a speaker's words are compared against his own specific reference patterns. For this reason, universal systems presently do not provide the same high degree of recognition accuracy as speaker-adaptive systems. Universal systems are isolated; the speaker must pause briefly between utterances.

Another factor is that in a universal type system, vocabularies must be predefined and stable; presently they are limited to fewer than 100 utterances. If the system dictionary contains English words, everyone talking to the system must speak English, and usually in a general dialect. By contrast, in isolated, speaker-adaptive systems, vocabularies and pronounciation are flexible, so that any language can be used. Multiple languages can be used on the same terminal, and persons having speech impediments can utter sounds that, although meaningless to the human ear, carry specific associations in a voice terminal. This is all possible with no special modifications to the speaker-adaptive system.

For most event or transaction oriented applications, speaker-adaptive systems offer the best alternative. They yield the highest proven accuracy, provide the most individual flexibility, operate adequately in high background noise and hostile environments (up to 90 dB), and cost the least.

An identified application for universal, isolated, limited vocabulary systems is banking by telephone, where spoken input is primarily numeric. In this case, voice input is combined with an associated technology, voice response. Although some systems of this type are installed, several parameters prevent greater proliferation. These include inconsistent quality of telephone lines, diverse regional accents that must be accommodated, presently achievable recognition accuracy, and high cost of voice entry when compared with one existing alternative, the Touch-Tone pad.

Cost reduction, wider implementation of fiber optic technology, greater predictability of telephone line performance and quality, improved techniques for telephone line signal normalization, adaptations of feature extraction, and refinements in reference sets—digital patterns against which spoken utterances are matched to achieve a recognition decision—all are required to achieve sufficient performance for the systems to be widely acceptable. All these improvements are expected within a 2-year time frame.

Connected, Speaker-Adaptive, Limited Vocabulary Systems

Connected speech represents the transition step between isolated word technology and continuous speech technology. In continuous speech, words are spoken in a contiguous string, and the speaker may optionally pause between any words in the string. Recognition begins coincident with the speaker's words or at any system-perceptible break in the word stream. This

technology is not currently available in a cost-effective system. Cost-effectiveness is emphasized because expected future availability of low cost microprocessors with improved speed, memory, and addressing capabilities will permit the eventual introduction of a viable price/performance continuous system. The expertise exists to produce a continuous speech system. However, the technology's limited combination possibilities with other technological building blocks, and high cost make such a system a solution in search of a problem.

A recent interim design that permits a predefined number of connected words to be spoken in a given time frame—normally four or five words—has a vocabulary of 120 utterances and is approximately seven times the cost of an isolated word (utterance) terminal. If an application involves rapid, sustained entry (without pauses) of numeric digits only (ie, onetwothreefour), connected speech is clearly faster by 2 to 1, and is more natural than pausing approximately one-tenth of a second between words or numbers, as is required by an isolated (paused) word system (ie, one-two-three-four). Applications that require input of connected digits by voice presently cost over $65,000 for a terminal. This high price necessarily limits cost-justifiable applications.

When phrases or word combinations are involved, the input speed advantage of connected over isolated speech can be questioned. Since an isolated word (utterance) system works on the principle of sound recognition, several words can be grouped and spoken as a single utterance in an isolated system. In this limited case, an isolated system performs as fast as a connected system. If the application is event or transaction oriented and common phrases, short sentences, or other word groupings are used, the isolated system is faster because groupings are set by dynamically adjustable time frames, not by number of words spoken (as in a connected system). The "pause" occurs at the end of the isolated phrase, not after each word. However, performance is clearly application dependent.

Other advantages of available isolated (utterance) systems over connected systems are vocabulary size—state of the art isolated systems have a 6:1 advantage; costs—isolated systems cost less than one-sixth as much as connected systems; and environmental stability—isolated systems have resolved the problems of stability of speaker reference data and accurate operation in high background noise situations.

Basic System Principles

An isolated word recognition system (Fig 1) identifies a spoken word by measuring acoustic characteristics of the word and comparing these characteristics with those of reference words stored in computer memory. The reference word characteristics are input beforehand by the same speaker who is to use the system. Features are extracted from incoming words that are characteristic of the basic sounds that comprise the words. Spectrum analysis is performed and a variety of spectral measurements are made. Combinations and sequences of these functions are processed to produce a set of significant acoustic features, including end of word indication.

The acoustic features of each word are then processed in real time. When the end of an utterance is detected by the feature extractor logic, the time normalizer processes the data so that dependence on word duration is minimized. Pattern matching classifier logic then compares the time-normalized feature set for the spoken word with stored reference patterns for each word in the vocabulary. The "best fit" is classified as a word in the vocabulary, provided that the comparison process exceeds a threshold level of similarity. If the incoming word does not match any word in the vocabulary, a reject decision is made. All recognition and reject decisions are displayed back to the operator for visual verification.

An ASR system is "trained" to recognize voice characteristics of any user by having the user speak each desired word several times (5 to 10) to provide a reference set of features for each word in the system. During this training process, the system automatically extracts a time-normalized feature matrix for each repetition of a given word. Fig 2(a) illustrates the reference matrix for the word "seven." A total of 512 bits of information (16 time segments, each containing 32 features) are required to store a feature map or reference matrix for each utterance or reference pattern. A consistent matrix resulting from successive

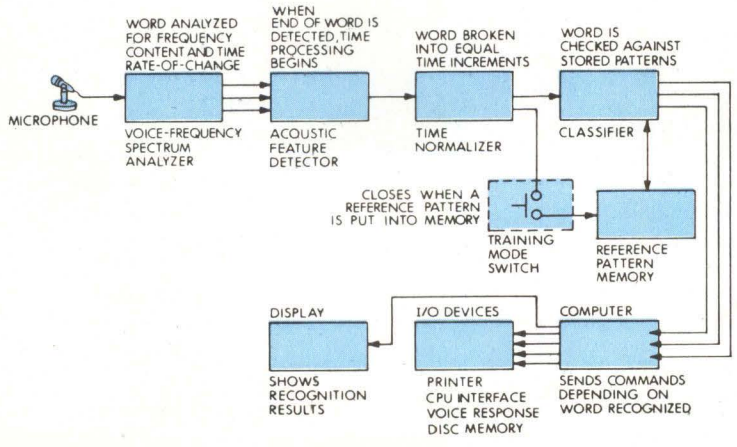


Fig 1 Basic speech recognition system. Spoken words are identified by measuring their acoustic characteristics and comparing them with reference patterns previously stored in memory. Pertinent word features are extracted, digitized, and time normalized. All word and realtime functions are performed in hardware; classification function is performed by software and recognition microprocessor. Each output decision is visually displayed or printed for instant verification

repetitions is required before features are stored in reference pattern memory. Feature occurrence is considered valid only when it occurs a minimum number of times relative to the number of training samples. This relationship is influenced by the choice of the template threshold factor, which is usually set to be 30 to 50% of a feature's occurrences.

The matrix in Fig 2(b) is derived from the same word as spoken during actual operation. This matrix also results from examination of 32 speech features normalized in 16 time segments, processed in a manner analogous to training mode procedure; ie, features are extracted, digitized, time normalized, and stored.

During the actual recognition process, the matrix in Fig 2(b) is compared against the matrix of Fig 2(a), as well as against every other matrix in the system vocabulary. With each comparison, a correlation product is calculated [Fig 2(c)]. The highest correlation product results in a recognition decision, provided that the product falls within the established recognition threshold. If the respective correlation falls outside the established recognition threshold, the system rejects the word with appropriate audio and/or visible indication to the speaker.

To be recognized, then, a spoken word must not only find a potential match among the matrices in the system dictionary, but must also match closely enough to assure the highest probability of an accurate recognition. These two measures assure optimal rejection of out-of-vocabulary words and extraneous background noises.

System Components

An ASR system (Fig 3) combines three integrated functional subsystems.

Preprocessor

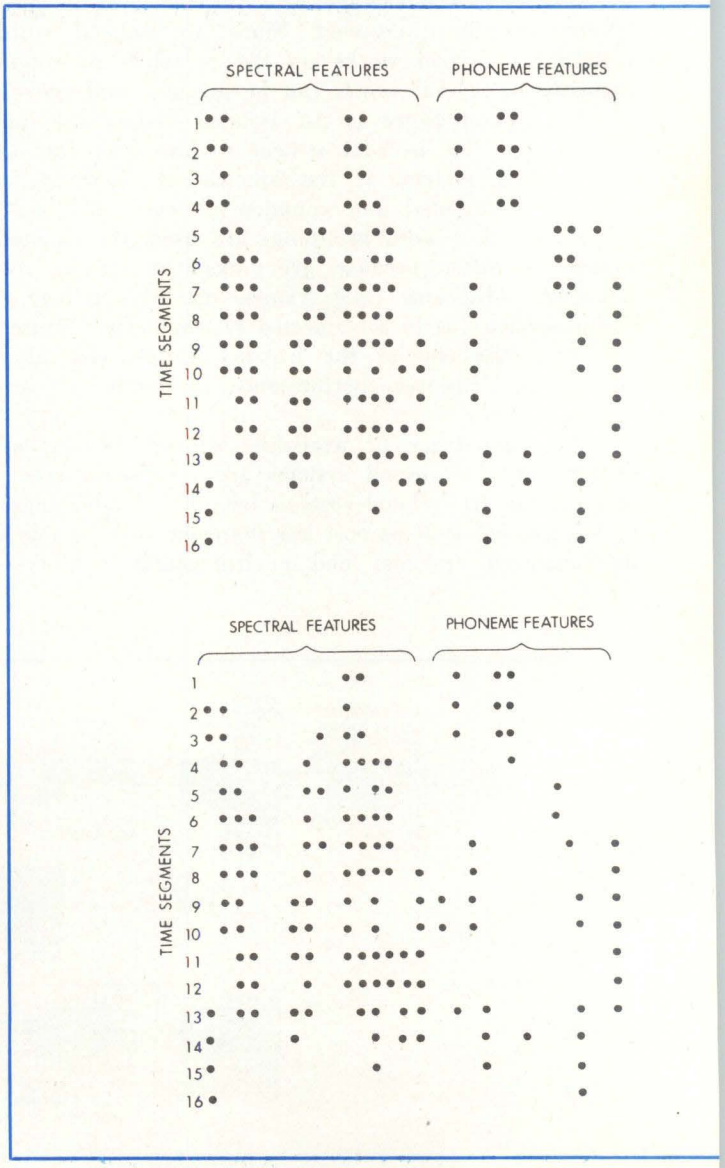
Microphones of different types—and sometimes of the same type—possess differing characteristics, causing varying output amplitude signals vs frequency. To achieve optimal feature extraction, the next function in the speech recognition process, microphone output, is standardized in the preprocessor using a spectrum shaper and a spectral analyzer.

The spectrum shaper compensates output energy from the noise canceling microphone to remove irregularities (amplitude vs frequency) and to produce a normalized speech spectrum. The spectrum analyzer breaks down the energy (E) vs frequency (f) content of the speech signals and normalizes this information for the subsequent feature extraction function. Normalized signals are passed through 16 contiguous bandpass filters, ranging in frequency from 250 to 4484 Hz. Output signals are full-wave rectified and logarithmically compressed to minimize amplitude dependence.

Feature Extractor

The spectral shape detector develops spectral derivative (dE/df) features and local maxima, indicating the overall spectrum shape. Spectral shape and its changes with time are measured continuously over the 250- to 4484-Hz frequency range of interest. Combinations and sequences of these measurements are processed in hardware to produce a set of 32 significant acoustic features, one of which is the initial estimate of word boundary.

Each feature is extracted by a combination of analog operations and binary logic. The output of the feature extractor consists of 32 binary signals. Features fall into two groups: 16 broad class or spectral features and 16 phonetic event features. Broad class features include such categories as vowel/vowel-like, formant characteristics, short pauses (less than 100 ms), and unvoiced noise-like consonants. Spectral features measure such regions as: energy maximums vs frequency (maxima), energy increases vs frequency (positive slopes), and energy decreases vs frequency (negative slopes). The 16 phonetic event features represent measurements corresponding to phoneme-like occurrences. Phonemes are the basic sounds in human speech. For example, the English language has approximately 40 phonemes. In normal conversation, about 10 phonemes/s are uttered. Changes in both spectral and phonetic features are also measured.



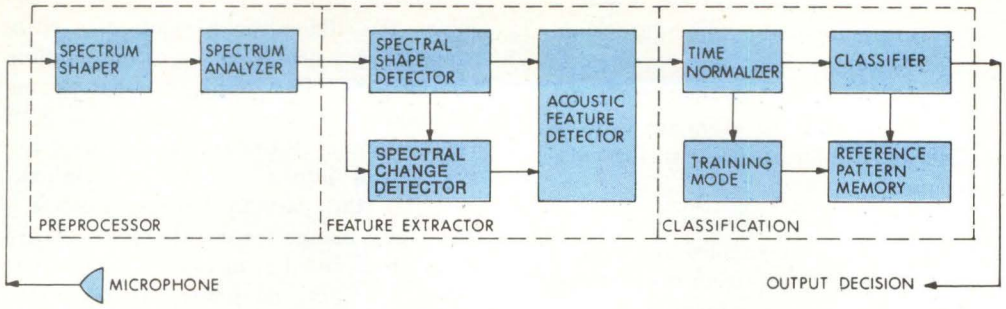


Fig 3 Isolated word recognition system. Three major functions—preprocessor, feature extractor, and classification—comprise system. First two functions derive acoustic parameters that are inherent to basic sound composition of each word. Combinations and sequences of spectrum and spectral measurements produce individualized set of significant acoustic features. Pattern matching logic compares time-normalized feature set with reference word patterns. Best correlation fit yields positive recognition output decision; otherwise reject decision results

WORD	CORRELATION PRODUCT
0	-168
1	-368
2	-261
3	-235
4	-214
5	-247
6	-161
7	+133
8	-230
9	-454
10	-261
11	-305
12	-120
13	-348
14	- 44
15	-371
16	-313
17	-272
18	-354
19	-281
20	-192
21	-149

Fig 2 Reference/spoken word matrices and resulting correlation products. Reference matrix for word "seven" (a) requires a consistent matrix of feature occurrences (between repetitions in training mode) before features are stored in reference pattern memory. In operational mode, spoken word matrix (b) is compared digitally with each stored reference matrix. Similarities and dissimilarities in each compared matrix are weighted, and net result provides weighted correlation products. Correlation products in 22-word vocabulary (c) are compared; stored reference word producing highest overall correlation product (+133) is selected as being correct if it exceeds minimum threshold correlation value

Classifier

This portion of the recognition system includes a time normalizer, training mode, reference pattern memory, and decision algorithm. A microprocessor accomplishes these functions.

The 32 encoded features, resulting from feature extraction, and their times of occurrence are stored in a short term memory. When the end of a word (utterance) is detected, the length of that word is computed and divided into 16 equal time segments, and the features are reconstructed into a normalized time base. An utterance—defined as a spoken sound with minimum length of 150 ms, maximum length of 2 s, and pause of 100 ms before the subsequent sound—is a letter, number, word, short phrase, or string of words that can be defined, flexibly, according to the application. Pattern matching logic next compares these feature occurrence patterns to the stored reference patterns for the various pre-established vocabulary words, determines a best fit, and makes a subsequent recognition decision.

This voice recognition system is speaker adaptive and, therefore, requires tuning to individual voice characteristics of any single user. This training mode is accomplished by repeating each word in the desired vocabulary several times to provide a reference set of features. The system stores in memory an individual reference set of word features for each word in the vocabulary and for each speaker in the application. A consistent matrix of feature occurrences (between repetitions) is required before the features are stored in the reference pattern memory.

In operational mode, spoken words are compared against an individual speaker's reference sets. The closest fit is selected as the recognized word. A "no decision" or a reject occurs when characteristics of the words in reference memory (data obtained from the training process) are not close enough to the word or words spoken in normal transaction use.

System Applications

Automatic speech recognition terminals are installed in numerous and diverse applications, which are characterized by one or more of the following parameters:

Hands-busy task is combined with the need to enter data at the source of a transaction or event, in contrast to entry of information at an intermediate data preparation step, such as keypunching.

Mobility is required during the data entry step. A VHF-FM or UHF-FM radio input link enables an operator to move freely up to 1000 ft (305 m) from the terminal in any direction, while talking input information.

Voice data entry is coincident with the immediacy of the event being recorded. As such, it convincingly addresses the problem of information perishability.

Voice data entry is widely used in general factory applications, such as quality control, incoming inspection, reviewing, traceability, warehousing, and sortation. In computer-aided design and manufacturing (CAD/CAM) applications, voice data entry is being used in such processes as printed circuit board component layout for text annotations, generation of wire lists, data retrieval/paging, selection of function modes, preparation of program tapes for numerical control (NC) equipment, civil engineering drawings, structural drawings, and bill of materials generation. Selective office, command and control, and word processing applications have also been voice adapted.

Voice data entry systems are usually implemented on the basis of strong cost justifications with early paybacks. Four primary reasons for these requirements are:

Acceptance of the technology has been hampered by the lack of announced products from a large corporation to sanction or precondition attitudes.

Existing off-the-shelf products and systems are not directed primarily at intermediate data preparation tasks (competing with a key entry clerk).

Voice is not selected in many source data entry applications because its economics are marginal. The technology is still not positioned optimally on the price/time curve.

Improvements and recombinations of the building blocks of ASR technology that address broader applications are just beginning to emerge.

Voice Programming

Preparation of program tapes for numerically controlled (NC) machine tools is a voice data entry application that clearly overcomes the man-machine obstacle of computerized parts programming. A computer programmer with a working knowledge of COBOL, FORTRAN, BASIC, or other software languages possesses the necessary skills to program a computer for a particular data processing application. However, programming an NC machine requires a separate set of skills, including an ability to read blueprints, understanding of specific machine tools, and knowledge of machine shop operations and procedures (Fig 4).

An alternative to developing a hybrid computer programmer is to train shop-experienced personnel in the programming and operation of digital computers. The latter alternative presents different but equally formidable problems. However, voice programming resolves the difficulty. Instead of writing instructions, performing calculations, and undergoing error prone, intermediate, data preparation steps necessary to get information into the computer, a shop-trained operator (not computer trained) merely talks information from a blueprint into a data entry terminal. This operator describes the part to be machined in everyday shop language, using words that are easily and flexibly established in the memory of the terminal or host computer. Using an interactive program, the words are converted to a series of programmed instruction steps that the computer understands, and from which the computer produces a paper tape to run the machine tool. Not only is the man-machine dilemma solved with "voice" as part of the input equation, but fast, accurate computerized parts programming output results.

Voice programming of paper tapes for NC machines offers the following advantages over traditional methods: reduced programming time and increased NC machine utilization, use of personnel with no computer programming training, increased program accuracy because of instant visual verification, and elimination of typing (input) errors.

A simplified example of how a typical NC task is verbally programmed is given below. The task is stated as: Provide a sequence of commands for producing "h" holes, equally spaced along an arc having a radius "r." The first hole is θ_1 degrees from the X axis and the last hole is θ_2 degrees from the X axis.

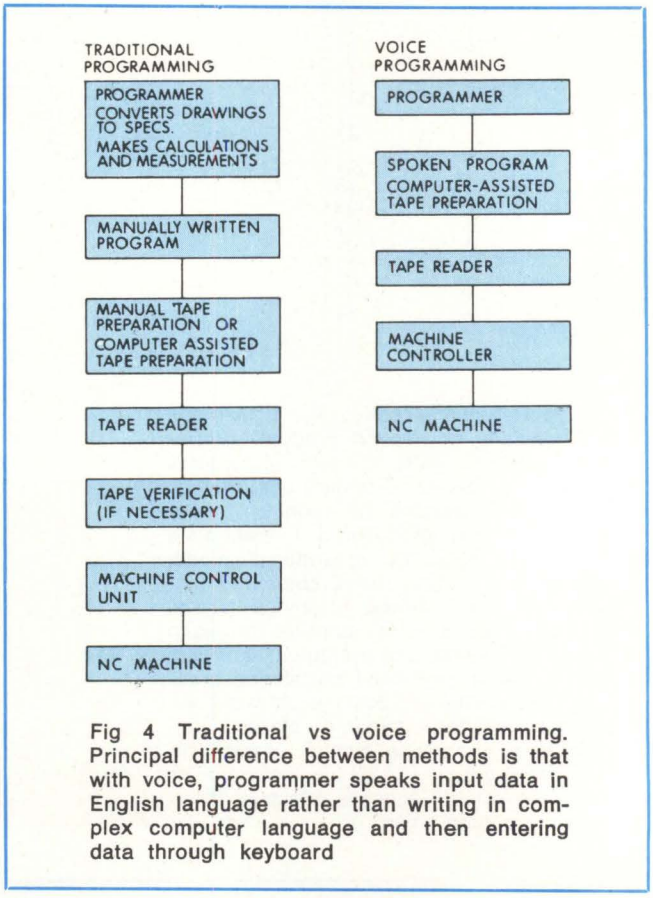


Fig 4 Traditional vs voice programming. Principal difference between methods is that with voice, programmer speaks input data in English language rather than writing in complex computer language and then entering data through keyboard

Format: ARC, θ_1, θ_2, h, and r
Data: $\theta_1 = 60°$, $\theta_2 = 135°$, r = 3.25", and h = 4

Task Sequence	Voice Commands	Display Readout
1	ARC	ARC angle 1 =
2	Six, Zero	ARC angle 1 = 60
3	OK	ARC angle 2 =
4	One, Three, Five	ARC angle 2 = 135
5	OK	ARC radius =
6	Three, Point, Two, Five	ARC radius = 3.25
7	OK	No. of holes =
8	Four	No. of holes = 4
9	OK	ARC 60 135 3.25 4*

Voice Identification

Voice grams or voice prints (used for speaker identification) have achieved high accuracy in laboratories. However, there is no consistent predictability regarding the degree of accuracy that can be achieved under nonlaboratory conditions, and the National Academy of Sciences recently discouraged the use of voice grams in forensic situations. Many factors about the science of voice recognition (as it relates to speaker identification) remain unknown, including the basic characteristics that distinguish one voice from another, the distribution of these characteristics within large populations, and the susceptibility of voices to voluntary control, as in mimicry.

Speaker verification (as distinct from speech recognition and speaker identification) is a logical outgrowth of speech recognition technology. Differences in the building blocks of speaker verification systems exist, just as in speech recognition. Current costs are prohibitive for many applications, and the techniques used are situation or application dependent.

In speech recognition, a feature extraction process identifies speech invariants (stable, repeatable characteristics) and measures them. Typically, these measurements are consistent and relatively speaker-independent over a wide speaker population. A resulting set of essential features, and their interrelationship over time, describe the elements needed for identification of a word.

However, speaker verification makes use of measurements which are highly speaker dependent. The speaker is identified by comparing these measurements against a prestored reference set of measurements for that respective speaker.

Currently, speaker verification can be used, reliably, as an integral part of a total security system. It would work in concert with other checks and balances in an overall security system to achieve optimal results. Used by itself, accuracy in excess of 95% can be achieved. Two types of possible occurring errors are defined as Type I, false rejections, and Type II, false acceptances; improvements can be made in either type, but to the detriment of the other.

Moral and ethical issues, as well as potential for abuse, are topics for serious consideration and discussion. Although the optimal speech verification system is not imminent, the potential of this technology, when combined with advanced artificial intelligence technology, represents a definite future reality.

*Teleprinter prints out: ARC 60 135 3.25 4

Summary

Available for widespread use today in voice data entry is a technique that is characterized as a limited vocabulary, speaker adaptive, isolated utterance automatic speech recognition system. It fits into source data entry and selected word processing systems as a terminal or as an intelligent keyboard. It is most advantageous if one or more of three parameters characterize an application: a hands/eyes busy task is combined with a data entry function, an operator requires freedom to move about in the process of a data entry transaction, and the necessity to record is coincident with the immediacy of the event being transacted. As such, ASR addresses the problem of information perishability more convincingly than any other method of data entry, and with emphasis on timeliness and accuracy.

With voice input, there are no preparatory or subsidiary requirements in the traditional sense: no hand recording, keying, dependence on media input, or introduction of intermediate steps. Accuracy is assured by recognition techniques which are integral to voice data entry, while the more cumbersome interlocks or comparison techniques of previous systems of entry are eliminated. Voice data entry combines in a single step, the basic elements of all data gathering systems: generation—it starts immediately and locally, verification—it agrees to predetermined concepts, and correction—accuracy is guaranteed before it proceeds to an accumulator as an element of useful information.

From a human perspective, ASR places the power of the computer at the disposal of a transaction-originator in a manner that does not require the personal restriction or alterations in behavioral patterns that are characteristic of traditional source data entry devices.

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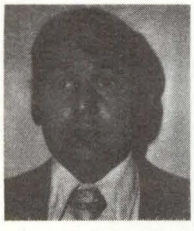
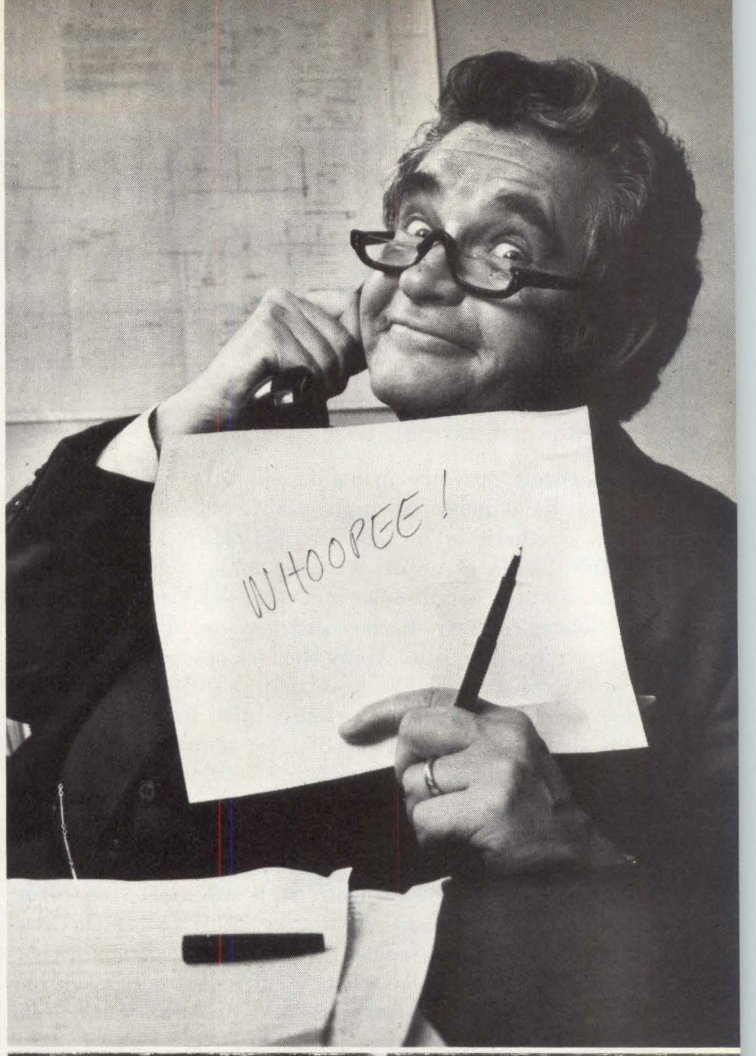


Prior to becoming marketing vice president for Threshold Technology, Mr Simmons served as a manufacturing systems analyst, and held various marketing management positions throughout the industry. He holds a BA degree from Providence College.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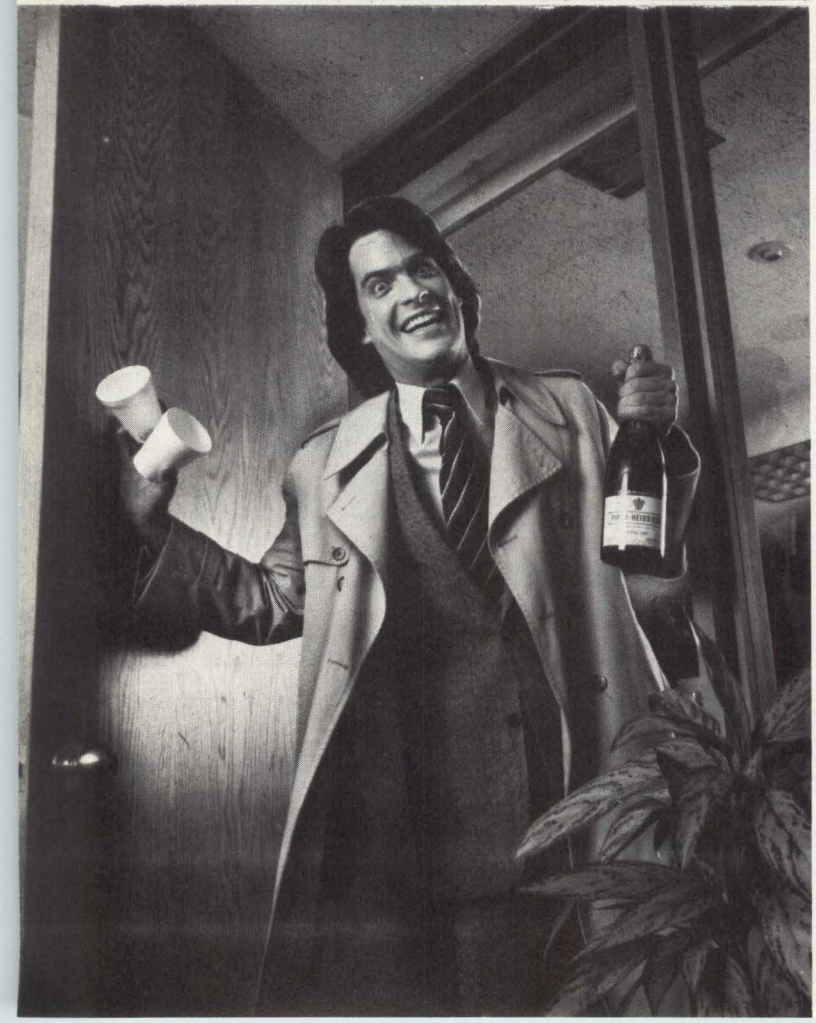

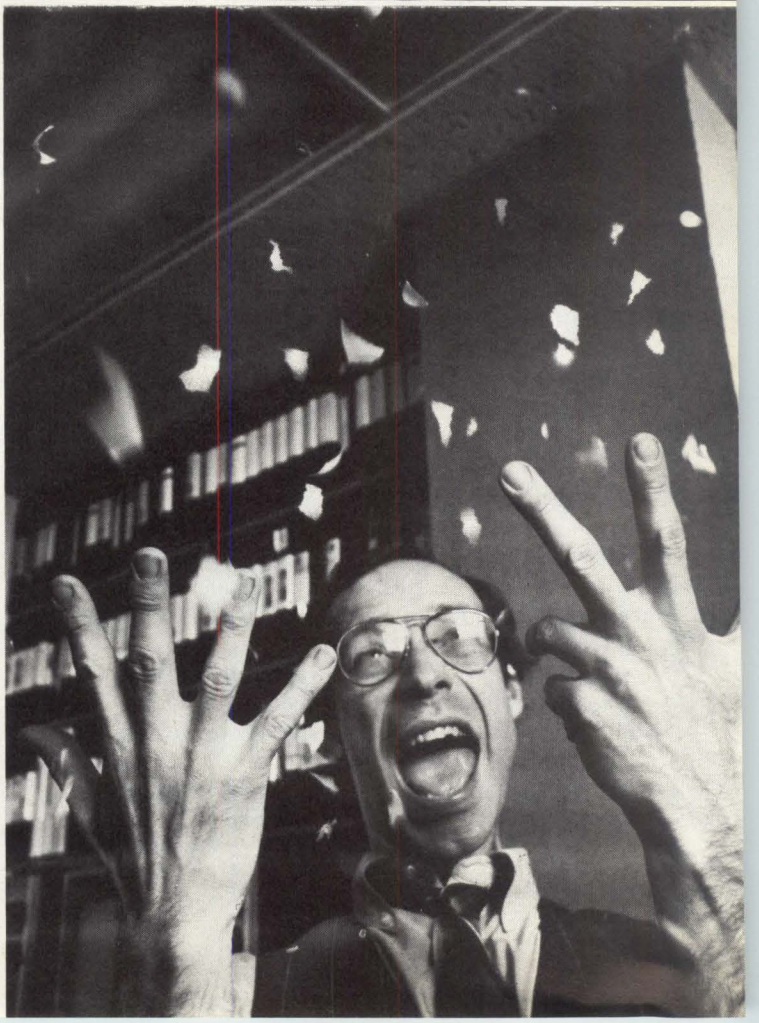

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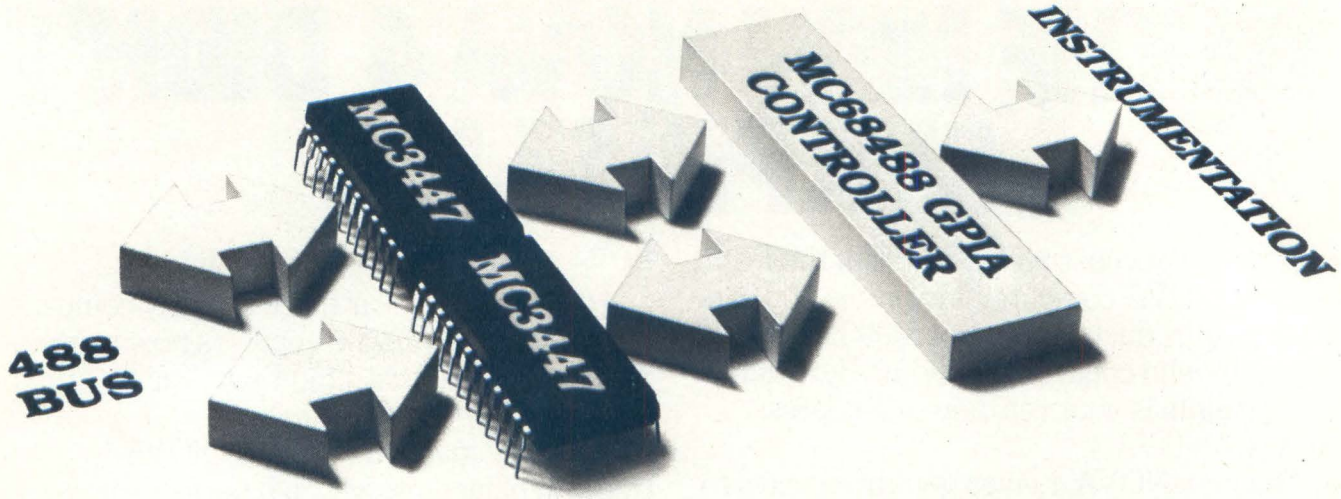

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MULTIPLIER/DIVIDER HARDWARE DESIGN ACCELERATES MICROPROCESSOR THROUGHPUT

Multiply and divide software routines usually curtail microprocessor based system throughput. For increased processing, added hardware logic performs very fast multiplication and division with minimal time and programming

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Microprocessors are increasingly being designed into data acquisition systems as controllers in process control instrumentation because they accurately govern changing input conditions, record data, and perform limited calculations. Large scale data acquisition applications require that microprocessors handle extensive, high speed data reductions. Although some currently available microprocessors perform high speed arithmetic operations, many are limited in this capacity because their instruction sets do not include multiply or divide operations.* In applications where these operations are required, multiplications and divisions can be performed by software routines or by additional hardware. However, software routines may be time consuming. For example, a 1-MHz MC6800 microprocessor from Motorola requires about 200 μs to complete a multiplication and about 300 μs to complete a division. Hardware that performs the same operations is about two orders of magnitude faster. Although this hardware represents added cost, its speed is essential for online applications that require recurrent multiplications or divisions.

The introduction of monolithic, parallel multipliers has prompted recent articles showing the ease of interfacing them to a microprocessor bus.[3,4] The speed of these multipliers (about 100 ns) cannot, however, be fully realized since the result is ready long before the microprocessor can possibly access it. A commercial divide device is not currently available.

An add-on hardware unit designed to perform 8-bit multiplications and 16-bit divisions presumes unsigned binary operands and returns unsigned results. This hardware multiply and divide unit comprises three sections—bus interface, control logic, and arithmetic. Bus interface provides the communications link between the system bus and the latter two sections. Control logic in conjunction with arithmetic sections performs multiplication and division operations by serial algo-

*Motorola has introduced the MC6801 and has announced the availability of the MC6809.[1] Instruction sets of both microprocessors are to include an 8-bit multiplication operation. Zilog's Z8000 is to be capable of performing 16-bit multiplication or division operations.[2]

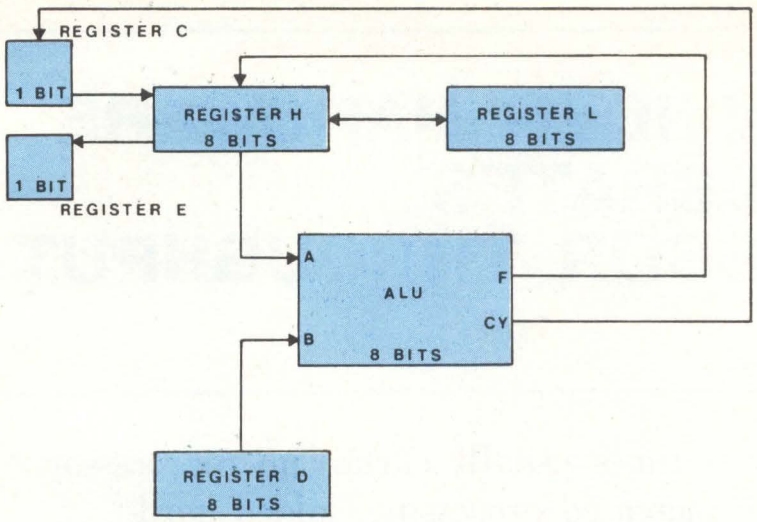


Fig 1 Block diagram of arithmetic section. This section consists of ALU and five registers that contain operands. It can perform n-bit by n-bit multiplications and 2n-bit by n-bit divisions. For hardware multiply and divide unit design, n is equal to eight

rithms. Although the interface has been designed to be compatible with a transistor-transistor logic (TTL) buffered MC6800 microprocessor based system, similar interfaces can be easily designed for other microprocessor systems using the same principles. The interface scheme for this multiplier/divider takes a somewhat different approach from those referenced previously; that is, only one microprocessor store instruction is required to initiate a hardware multiply and divide operation. The hardware design suggests a powerful addressing scheme that has numerous data acquisition system applications. Its operation is designed for simplicity, consistent with instruction set capabilities.

Design Considerations

Primary factors considered were the ability to perform an 8-bit by 8-bit multiplication to yield a 16-bit product, and a 16-bit by 8-bit division to yield an 8-bit quotient with an 8-bit remainder. Also, the unit had to provide an error indication whenever an invalid division was attempted.

Since this design began as a project in electronic instrumentation, the monolithic multipliers and the parallel algorithm were discarded in favor of common TTL circuitry and a serial algorithm, largely for educational reasons. The choice of a slower serial algorithm does not degrade the overall performance of the microprocessor based system because the former methods are much faster than necessary. Most microprocessors are unable to request a result fast enough to exploit the speed of the parallel, monolithic multipliers.

Multiplication and Division Algorithms

The arithmetic section of the hardware unit (Fig 1) performs an 8-bit by 8-bit multiplication or a 16-bit by 8-bit division according to the serial algorithms. Registers H, L, and D must each contain eight bits, whereas registers E and C need only contain one bit each. For a multiplication, the arithmetic logic unit (ALU) must be able to perform an 8-bit addition; its output must be the sum of registers H and D. Likewise, for a division, the ALU must be able to perform an 8-bit subtraction. Its output must be the value of register H minus register D. The serial algorithm also requires that registers C-H-L and E-H-L be able to perform a synchronous right shift (C-H-L) or a synchronous left shift (E-H-L).

Booth's Algorithm[5] is used to perform 8-bit by 8-bit binary multiplications. This algorithm consists of eight sequences of add and shift cycles and is equivalent to a longhand binary multiplication. Add and shift cycles and longhand multiplication for the simpler case of a 4-bit multiplication are shown in Fig 2. Initially, registers D and L are loaded with the multiplicand and the multiplier, respectively, and register H is cleared. The least significant bit (LSB) of register L(L_0) is tested to determine whether an addition of register D to register H is to be performed. If the value of L_0 is 1, addition is performed by replacing the contents of registers C and H with the CARRY OUT and FUNCTION outputs of the ALU, respectively. This operation is equivalent to adding the multiplicand that is stored in register D to the accumulating product. If the value of L_0 is 0, replacement is inhibited. After each add sequence is completed, the 17-bit register C-H-L is shifted right one position. The next LSB of the multiplier is then in position L_0 and is ready to be tested on the next cycle. A right shift of register C-H-L is performed every cycle regardless of the value of the test bit, L_0. When eight add and shift cycles have been executed, the multiplication is finished. The eight most significant bits (MSBs) and eight LSBs of the 16-bit product reside in registers H and L, respectively.

The serial algorithm for division is equivalent to a longhand binary division—the inverse of serial multi-

LONGHAND BINARY MULTIPLICATION

```
1111 = 15
0011 =  3
------
1111
1111
0000
0000
-------
0101101 = 45
```

ADD AND SHIFT ALGORITHM FOR A MULTIPLICATION

	REGISTER C	REGISTER H	REGISTER L	REGISTER D
INITIAL	0	0000	MULTIPLIER→0011 = 3	1111 = 15
TEST, ADD H + D → (C-H)	0	1111	0011	↑
SHIFT C-H-L ONE BIT RIGHT	0	0111	1001	MULTIPLICAND
TEST, ADD H + D → (C-H)	1	0110	1001	
SHIFT C-H-L ONE BIT RIGHT	0	1011	0100	
TEST, SHIFT C-H-L ONE BIT RIGHT	0	0101	1010	
TEST, SHIFT C-H-L ONE BIT RIGHT	0	PRODUCT→ 0010	1101 = 45	

Fig 2 Binary multiplication—longhand and add/shift methods. Add and shift cycles of Booth's Algorithm are similar to steps of longhand binary multiplication; 8-bit product from 4-bit by 4-bit multiplication is contained in registers H and L (Fig 1)

plication; the division sequence is subtract and shift left. A longhand binary division and the serial algorithm sequences for the simple case of an 8-bit by 4-bit division appear in Fig 3. The divide operation is initialized after loading the most significant byte and the least significant byte of the 2-byte dividend into registers H and L, respectively. The divisor is placed into register D, and register E is cleared. The decision of whether to subtract register D from register H is determined by the CARRY OUT value of the ALU and the value of register E. For the ALU (74181) used in this design, CARRY OUT is 1 if a borrow is necessary to perform the subtraction, and CARRY OUT is 0 if a borrow is not necessary. When the value of E + $\overline{\text{CARRY OUT}}$ is 1, the result of the subtraction of register D from register H is loaded into register H; however,

LONGHAND BINARY DIVISION

```
                00011 =  3
15 = 1111 ) 00101111 = 47
            0000
            ----
             0101
             0000
             ----
              1011
              0000
              ----
               10111
               1111
               ----
                10001
                 1111
                 ----
                 0010 =  2
```

SUBTRACT AND SHIFT ALGORITHM FOR A DIVISION

	REGISTER E	REGISTER H	REGISTER L	REGISTER D
INITIAL	0	DIVIDEND→ 0010	1111 = 47	1111 = 15
TEST, SHIFT E-H-L ONE BIT LEFT	0	0101	1110	↑
TEST, SHIFT E-H-L ONE BIT LEFT	0	1011	1100	DIVISOR
TEST, SHIFT E-H-L ONE BIT LEFT	1	0111	1000	
TEST, SUBTRACT (E-H) — D → H	1	1000	1000	
SHIFT E-H-L ONE BIT LEFT	1	0001	0001	
TEST, SUBTRACT (E-H) — D → H	1	0010	0001	
SHIFT L ONE BIT LEFT	0	0010 = 2	0011 = 3	
		↑	↑	
		REMAINDER	QUOTIENT	

Fig 3 Binary division—longhand and subtract/shift methods. Subtract and shift cycles of serial algorithm are similar to steps of longhand division. Remainder and quotient of 8-bit by 4-bit division are contained in registers H and L (Fig 1)

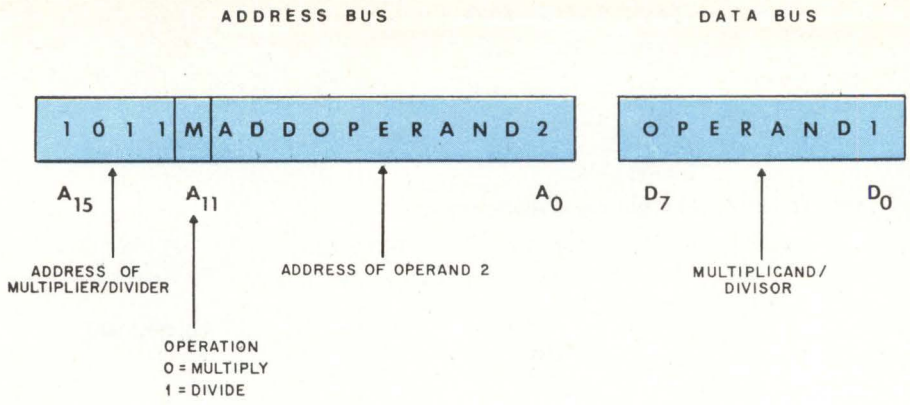
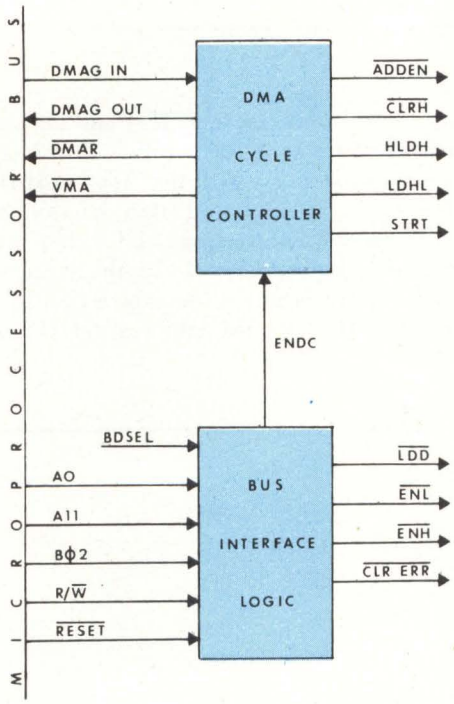


Fig 4 System address and data buses. "Snapshot" of system address and data buses during store (write) into hardware multiply/divide unit shows that information is transferred via both buses. Unit is enabled by four MSBs of address bus, which also contains address of second operand. One operand is transferred via data bus



SIGNALS

ADDEN—ADDRESS ENABLE
BDSEL—BOARD SELECT ADDRESS SPECIFIED
BΦ2—MC6800 PHASE 2 CLOCK SIGNAL
CLRH—CLEAR H
DMAG IN—DMA GRANT
DMAG OUT—DMA GRANT
DMAR—DMA REQUEST
ENDC—ENABLE DMA CYCLE CONTROLLER
ENH, ENL—ENABLE H, L
HLDH—HOLD H
LDHL—LOAD H, L
LDD—LOAD D

Fig 5 DMA schemes. Bus interface logic enables DMA cycle controller after microprocessor executes a store (write) into hardware unit. One DMA cycle is required to fetch multiplier; two DMA cycles are required to fetch dividend. Microprocessor reads result of arithmetic operation from two consecutive locations in multiply/divide device

if the value of E + CARRY OUT is 0, the load is inhibited. The 17-bit register E-H-L is shifted left on each cycle with the value of E + CARRY OUT entering at L_0. After the division is completed, the 8-bit quotient is contained in register L, while the 8-bit remainder is contained in register H. Division requires one cycle more than multiplication (nine total), because the first subtraction must lead to a negative result (E + CARRY OUT = 0) if the quotient is to be expressed in eight bits. If the first subtraction yields a positive result (E + CARRY OUT = 1), either an overflow division (quotient is larger than $2^8 - 1 = 255$) or a division by zero is being attempted. This error condition is indicated by filling registers H and L with 1s (register H = register L = 255). The result is impossible because a valid division may never have a remainder with a value larger than or equal to the divisor. This overflow condition may be used to "trap" program execution via one of the processor interrupt lines. During the last cycle of the division, only register L is shifted left in order to enter the value of E + CARRY OUT into the LSB of the quotient.

Interface Scheme

The number of bytes of information required by the hardware unit is dependent on the operation that is to be performed. A multiplication requires only a 1-byte multiplicand and a 1-byte multiplier, whereas a division requires a 2-byte dividend and a 1-byte divisor. Two and three stores by the microprocessor would, therefore, be required to initiate a multiplication and a division, respectively. The suggested procedure to transfer data to the multiplier/divider is to execute the necessary number of store instructions under program control.[3,4] Although this method is satisfactory, it does require a significant amount of microprocessor intervention. The addressing scheme described is unique in that only one store execution by the microprocessor is necessary to initiate the hardware multiply/divide operation. Also, this scheme is unusual in that both data and address buses are used to transfer information to the unit. The latter technique has been used in the design of a video display.[6]

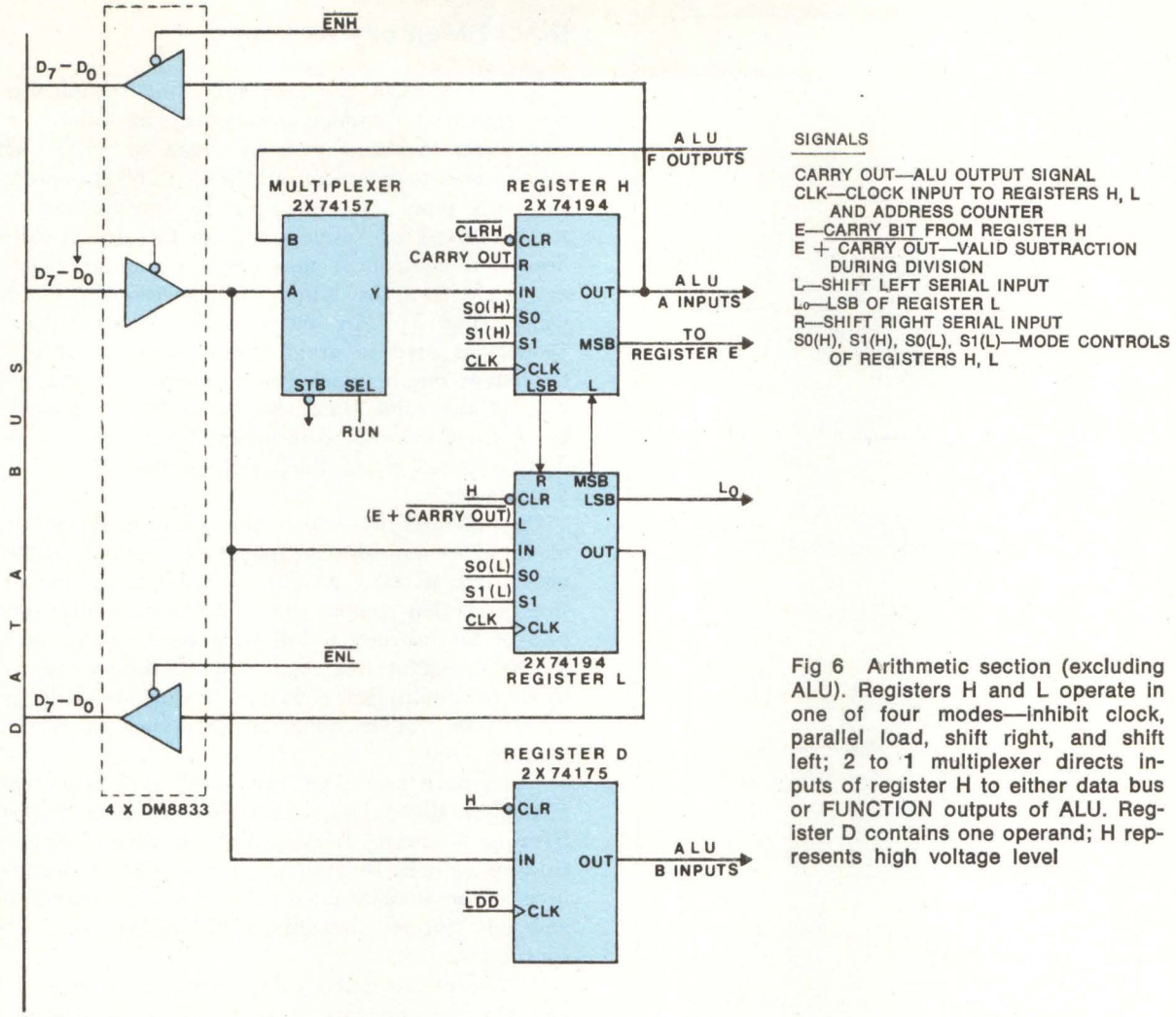
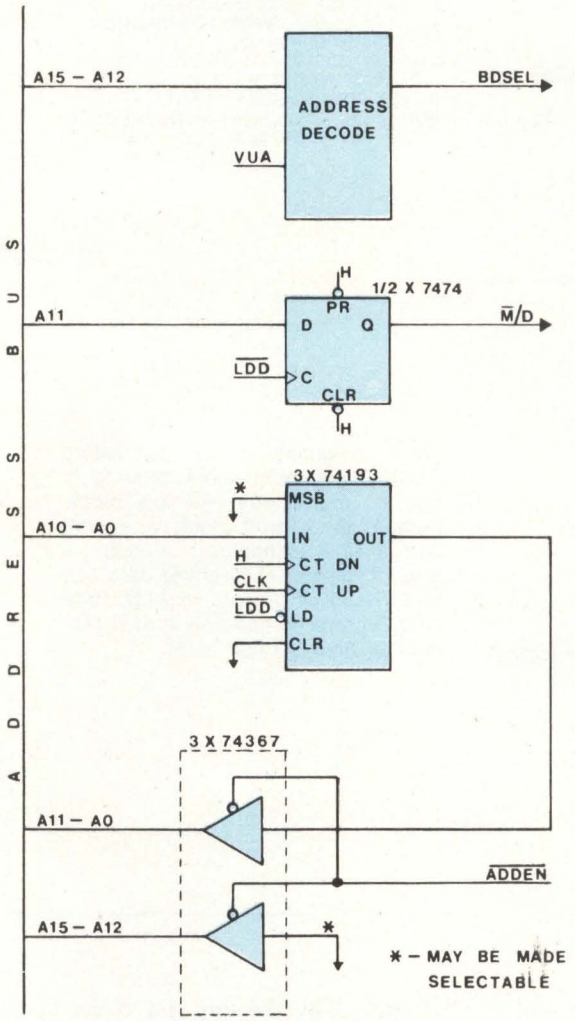


Fig 6 Arithmetic section (excluding ALU). Registers H and L operate in one of four modes—inhibit clock, parallel load, shift right, and shift left; 2 to 1 multiplexer directs inputs of register H to either data bus or FUNCTION outputs of ALU. Register D contains one operand; H represents high voltage level

The 16-bit address that appears on the address bus during the microprocessor store cycle initiates the multiplier/divider and contains several action items (Fig 4). During this cycle the data bus contains the first operand, which is either the multiplicand or the divisor. The four MSBs (A_{15} to A_{12}) of the 16-bit address are decoded to enable the hardware unit, while address bit A_{11} functions as the multiply/divide operation code. The least significant 11 address bits determine the address of the second operand, which is a 1-byte multiplier or a 2-byte dividend. Because only the four MSBs of the 16-bit address are used to enable the multiplier/divider, it appears to occupy a 4k-byte address block. This addressing scheme does, of course, restrict the location of the second operand to a 2k block of memory.

At the end of the write cycle, the hardware unit latches the first operand from the data bus. Operation code (A_{11}) and address of the second operand (A_{10} to A_0) are also latched from the address bus. The second operand is then fetched by the unit via direct memory access (DMA). When a DMA cycle is granted, the multiplier/divider places the address of the second operand on the address bus. The five MSBs of the 16-bit address are set equal to 0, although they can be made designer selectable by additional circuitry. Only one DMA cycle is necessary to fetch the second operand before a multiplication may begin. For a division, however, two DMA cycles are required to fetch the 2-byte dividend, which must be stored in two consecutive locations in memory (high order byte, low order byte).

The microprocessor may fetch the result, which is a 2-byte product or a 1-byte quotient with a 1-byte remainder, by reading from two consecutive addresses in the multiplier/divider. It returns either the high order byte of the product (multiplication) or the remainder (division), and either the low order byte of the product (multiplication) or the quotient (division) during a read from addresses $\$B000_{16}$ and $\$B001_{16}$, respectively.



SIGNAL

M/D—MULTIPLY/DIVIDE

Fig 7 Interface section. This section determines when hardware unit is being selected (BDSEL) and latches low order 12 bits from address bus during a store (write) into multiplier/divider. Address of second operand, A_{10} to A_0, is placed into 12-bit counter, which is incremented before second DMA cycle. Address bit A_{11} indicates whether operation is to be multiplication ($A_{11} = 0$) or division ($A_{11} = 1$); H represents high voltage level

Direct Memory Access

DMA occurs when the microprocessor relinquishes system control to another component in order for that component to access memory (read or write) without microprocessor intervention. On an MC6800 microprocessor, two types of DMA may be implemented—either HALT (HOLD) or "cycle-steal." In this bus architecture design, a component may request one or more DMA cycles via an active low, open collector, TTL bus line—$\overline{\text{DMAR}}$ (Fig 5). An active high, daisy chained line (DMAG) is used to grant (acknowledge) a DMA cycle. Of course, one or more system components may request DMA at the same time; however, the component with the highest priority, determined by its position in the daisy chained grant line, will be the first to receive a DMA cycle.

One method by which the microprocessor can be made to relinquish control of the system bus is to put it into a HALT condition. The microprocessor will stop execution (enter the HALT state) after completion of an instruction following the one during which the DMA request was made (microprocessor store into hardware multiplier/divider). It may be held in the HALT state for as long as necessary to service all DMA requests.

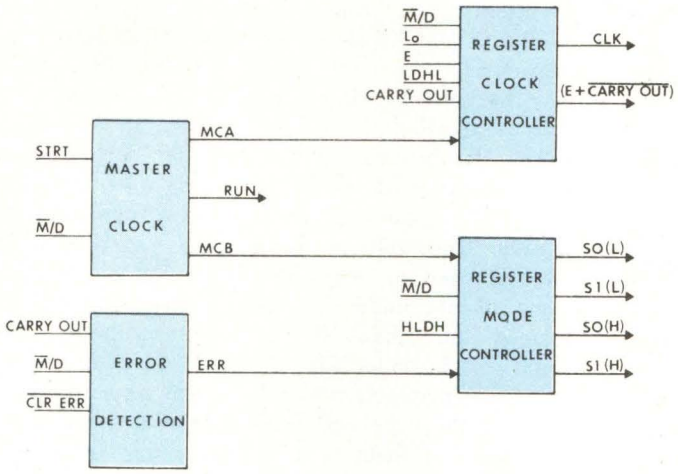
The second DMA type, cycle-steal, is a more dynamic method in that microprocessor execution is stopped by freezing its master clocks. Only a limited number of DMA cycles may be granted sequentially by this method because the MC6800 microprocessor is a dynamic device and will "forget" its status if the clocks remain frozen for too long.[7]

The hardware unit operates with either type of DMA; however, in one case a slight software change must be made. Because the microprocessor does not halt until the completion of the instruction following the DMA request, the read instruction to fetch the result from the device may not immediately follow the store instruction when HALT type DMA is being used.

Hardware

Registers H and L (Fig 6) each contain eight bits and are formed by two 4-bit bidirectional shift registers (74194). Register D also contains eight bits and is made of two quadruple D type flipflops (74175). The ALU, which is capable of adding or subtracting two 8-bit operands, is made of two 4-bit ALUs (74181). Because register H has to be loaded from both the system data bus and the FUNCTION outputs of the ALU, the input to register H is controlled by a 2 to 1 multiplexer (74157). While a multiplication or a division is being performed, the input of register H is connected to the FUNCTION outputs of the ALU. At all other times, the input of register H is connected to the data bus.

The interface (Fig 7) decodes the four MSBs of the 16-bit address (A_{15} to A_{12}) and the valid user address (VUA) control bus line to determine if the multiplier/



SIGNALS

ERR—INDICATES INVALID DIVISION
MCA, MCB—MASTER CLOCK A, B

Fig 8 Control logic section. This section generates clock pulses (CLK) and mode control waveforms [S0(L), S1(L), S0(H), S1(H)] for registers H and L, and makes decisions whether or not to inhibit addition (multiplication) or subtraction (division) during each cycle. Division by zero or overflow division is signaled by ERR

divider is being specified (BDSEL). VUA is an open collector line equivalent to the MC6800 microprocessor valid memory address (VMA) control line.[8] The address (A_{10} to A_0) of the second operand and the multiply/divide operation code (A_{11}) are latched into a 12-bit counter (3 x 74193) and a D type flipflop (½ x 7474), respectively.

The remainder of the interface is shown in Fig 5. Bus interface logic synchronizes the multiplier/divider to the microprocessor bus; $\overline{\text{LDD}}$ causes information to be latched into the unit during the microprocessor store (write) cycle. Results of arithmetic operations are placed onto the data bus by activating $\overline{\text{ENH}}$ and $\overline{\text{ENL}}$, which enable bus drivers (Fig 6) attached to registers H and L. $\overline{\text{CLR ERR}}$ will clear an error condition caused by a previous overflow division or a division by zero. The DMA cycle controller directs the DMA cycles and initiates the operation of the control logic (STRT). Registers H and L are controlled by $\overline{\text{CLRH}}$, HLDH, and LDHL during DMA cycles.

Control logic (Fig 8) produces clock pulses (CLK) and waveforms that determine the modes of operation of registers H and L: S0(H), S1(H), S0(L), and S1(L). The harmony of these signals generates the add/subtract and shift sequences of the serial algorithms.

Software

The access scheme developed for the hardware multiply/divide design simplifies programming because only one store instruction is required to initiate the unit's operation. A sample multiplication program for the MC6800 microprocessor is

Operation Code (hex)			Mnemonic		Remarks
•			•		
•			•		
•			•		
86	08		LDAA	= 8	Load multiplicand
B7	BX	LL	STAA	$BXLL	Store multiplicand (initiate multiplication)
FE	B0	00	LDX	$B000	Load result
•			•		
•			•		
•			•		

A similar division program is

Operation Code (hex)			Mnemonic		Remarks
•			•		
•			•		
•			•		
86	07		LDAA	= 7	Load divisor
B7	BY	LL	STAA	$BYLL	Store divisor (initiate division)
FE	B0	00	LDX	$B000	Load result
•			•		
•			•		
•			•		

The multiplier or the first byte of the 2-byte dividend must be located in memory at an address $0XLL, which may have any value between and including $0000 and $07FF. The multiplicand or the divisor is loaded into either accumulator A or B, and that accumulator is stored into the multiplier/divider at address $BXLL or $BYLL for multiplication or division, respectively. The value of Y is equal to the value of X + 8. If halt type DMA is being used, at least one instruction must be placed between the store instruction (STAA or STAB) and the fetch instruction

because the microprocessor will not halt until completion of the instruction following the store. This precaution is not necessary when cycle-steal DMA is used.

Software control of the multiplier/divider is consistent with the instruction set of the MC6800 microprocessor. A store instruction into the device at location \$BXLL (XLL = 000 → 7FF) is equivalent to a multiply instruction (MPYA or MPYB) that would multiply the contents of either accumulator A (STAA) or accumulator B (STAB) with the contents of memory location \$0XLL. The divide instruction is analogous to the multiply instruction. Thus, a store instruction into the device at location \$BYLL (Y = X + 8) is equivalent to a divide instruction (DVDA or DVDB) that would divide the 2-byte word in memory locations XLL and XLM (LM = LL + 1) by either the contents of accumulator A or B. These multiply and divide instructions resemble other instructions of the MC6800 microprocessor. An ADD instruction, for example, adds the contents of a memory location to the contents of either accumulator A or B and places the result into the same accumulator. The multiply and divide instructions, therefore, parallel the ADD instruction except that the former instructions do not return the result of the operation to the internal registers of the microprocessor. Instead, the result of a multiplication or division resides in a memory location external to the microprocessor (\$B000, \$B001).

The scheme previously described to transfer necessary information separately stores the multiplicand and the multiplier into the hardware unit's registers. Two STA instructions are, of course, required to initiate operation of the hardware multiplier. In contrast, the scheme used to operate the hardware design is similar to the extended arithmetic hardware option of the LSI-11™ microprocessor. In the latter case, a multiplication (MUL) or a division (DIV) is performed by one software instruction.

The time required for an MC6800 microprocessor and the multiplier/divider to perform an unsigned 8-bit by 8-bit multiplication and to fetch the result is 11 μs.† This time compares favorably with that of the LSI-11 microprocessor, which requires at least 24 μs and up to 37 μs to perform the same operation (MUL), except that it is a signed multiply.[9] The MC6800 microprocessor and multiplier/divider require only 12 μs (two DMA cycles) to perform a 16-bit by 8-bit division; the LSI-11 microprocessor, on the other hand, requires 78 μs to perform the same operation (DIV) except that it is a signed division.

Summary

Maximum operating speeds of the multiplier/divider by itself, which contains mostly 7400 series devices, are 1.6 μs and 1.8 μs for a multiplication and a division, respectively. Other series devices (74H, 74L, 74S, 74LS) may be used to either reduce power consumption or increase speed.

The hardware's multiply/divide performance had been tested with a program that sequentially generates every possible multiplication and division operation. The unit performed all operations correctly, and returned an error condition for all invalid divisions. While under continuous testing, the unit performed more than 10^{10} operations without a mistake. Total cost is under fifty dollars.†† In comparison, commercially available multipliers are approximately 100 dollars; they do not perform the division operation, and many of them do not include the cost of interfacing hardware.

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™LSI-11 is a registered trademark of Digital Equipment Corp, Maynard, Mass.

†This includes an STAA instruction (extended, 5 μs); an LDX instruction (extended, 5 μs); one DMA cycle via cycle-steal DMA (1 μs); and a 1-MHz microprocessor clock.

††For information about the hardware multiply/divide unit's schematics and PC boards, please communicate with Dr Robert S. Rodgers, Dept of Chemistry, Seeley G. Mudd Bldg 6, Lehigh University, Bethlehem, PA 18015.

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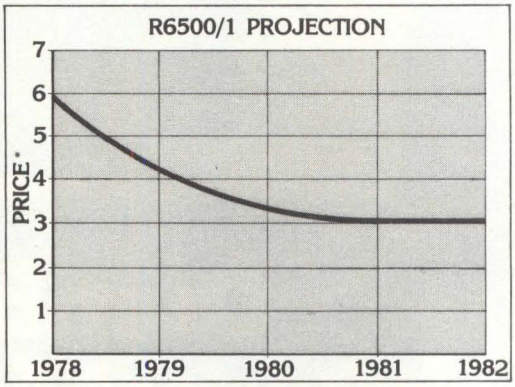

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BUBBLE MEMORY RECORDERS FOR SPACE APPLICATIONS

Solid state bubble domain recorder design and development aim toward improved reliability, chip capacity, and application versatility

Oliver D. Bohning Rockwell International Corp, Electronic Systems Group, Anaheim, California

In current satellite and deep space systems, magnetic tape recorders play an important role in information collection, storage, and transmission. While they offer a wide range of storage capacities and operating frequencies for fulfilling different mission requirements, tape recorders have the prime disadvantage of low reliability. Because of the high percentage of failures associated with mechanical tape handlers, in the early 1970s NASA decided to develop a totally solid state bubble domain recorder that would have the desirable attributes of magnetic tape units but without the moving parts, inherent mechanical inertia, or limited lifetime.*

Bubble Recorder Advantages

Bubble recorders differ from other storage media in that they are modularized naturally in data blocks of several kilobits to a megabit or more. Unlike moving media recorders, the bubble devices have data blocks that are electronically addressable without consideration for interblock spaces or for block headers. Among the many bubble organization possibilities, three offer advantages in current bubble recorder technology (Fig 1).

The serially organized design exemplifies current recorder hardware development. In this design, data flow serially through a serpentine path enclosed on itself so that once written, data continue to cycle until purposely erased. Sensing is done on an auxiliary replicated data path, and erasing by transferring data off the main track. Simplicity and low power dissipation are primary advantages of serial organization, especially for incremental power interruptible first in first out (FIFO) stack operation such as in data logging applications.

In conventional major/minor design, data flow from the generator into the major loop, and when synchronized with the minor loops, data are transferred as a block into all active loops. One advantage of this design is that only one transfer conductor is required, and another feature is that bad loops can be excluded by data organization. For economic reasons, this approach is beneficial since it increases yield and decreases cost. It is a disadvantage in many recorder applications that this design requires more ancillary hardware and more power than does the serial design.

In the block oriented design data blocks fill specific minor loops. Primary advantage of this approach is its fast data block access, but at the disadvantage of requiring a conductor per minor loop.

Bubble photolithographic simplicity, device design

*For additional background information on bubble recorders, refer to: "Designing a Magnetic Bubble Data Recorder; Part 1—Component Level, and Part 2—System Level," E. J. Hoffman, *et al*, *Computer Design*, Mar and Apr 1976

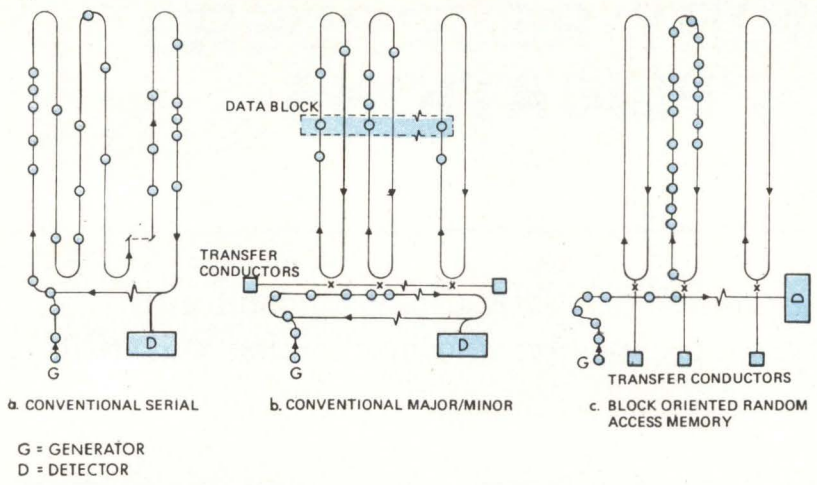

Fig 1 Three storage organizations for bubble recorders. Serial organizations are lower in system power dissipation and are easier to implement. Major/minor designs permit faster block access. Nonconventional designs offer advantages in special aerospace applications

innovations, and lowering costs of mask manufacture enable development of custom bubble storage devices for special recorders. Bubble recorder design for spacecraft applications will benefit from the growing technological base being established around garnet materials.

Nonvolatile and naturally incremental, a bubble recorder can be turned on from a powered-off condition in about 10 μs to retrieve or store a single byte of data. This can be done because the permalloy pattern on the garnet (Fig 2) is a discrete rather than continuous storage medium. When the clockwise rotating field (Hxy) is off, the bubble rests on strong permalloy poles, such as "A", which are enhanced by an inplane static holding field. When Hxy is rotated, the bubble responds by moving and undulating around the permalloy element so that it moves a discrete step during every field rotation. In this manner, it is possible to always know electronically where a data record is located in storage. Bubble storage, with its zero standby power and fast turn on, seems a natural choice whenever an incremental or a transient record must be made, such as for seismic events, radiation bursts, or cataclysmic occurrences.

Bubble recorders can be designed to be intolerant to failure. Modularity of bubble storage is exploited in highly reliable systems by providing multiple paths from system interface to storage modules so that a single failure slightly degrades system capacity rather than causing failure of the whole system. An important aspect of reliability is the error rate of bubble storage. For hard errors, defined as a spurious or a missing bubble, error rate depends on how close the operating field is to bubble collapse or to bubble strip-out. Strip-out is a condition where a bubble domain stretches between permalloy elements. A guard band of approximately 3 oersteds (Oe) of bias margin guarantees a hard error rate below 10^{-14} errors per field rotation. Soft error rate, the number of bits misread for every one read, is currently better than 10^{-8} for individual chip operation.

Bubble Recorder Development

The first demonstrated feasibility of a bubble spacecraft recorder is a 60k-bit engineering model recorder (Fig 3) delivered in 1975 to NASA's Langley Research Center. A magnetic module contains bias magnets, shield plates, and field adjusting screws for four separate cavities. Two chip ceramic packages are installed in three of the cavities. With amplifiers placed in the

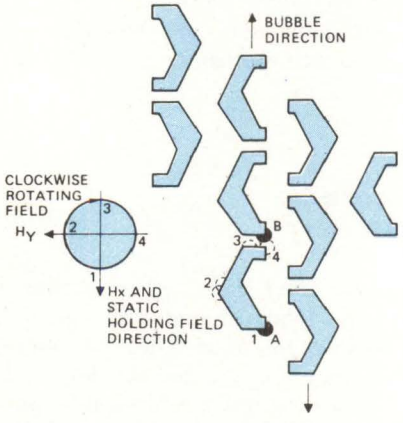

Fig 2 Propagation pattern. As magnetic field is rotated clockwise one full revolution, bubble at "A" will move one discrete step to location "B"

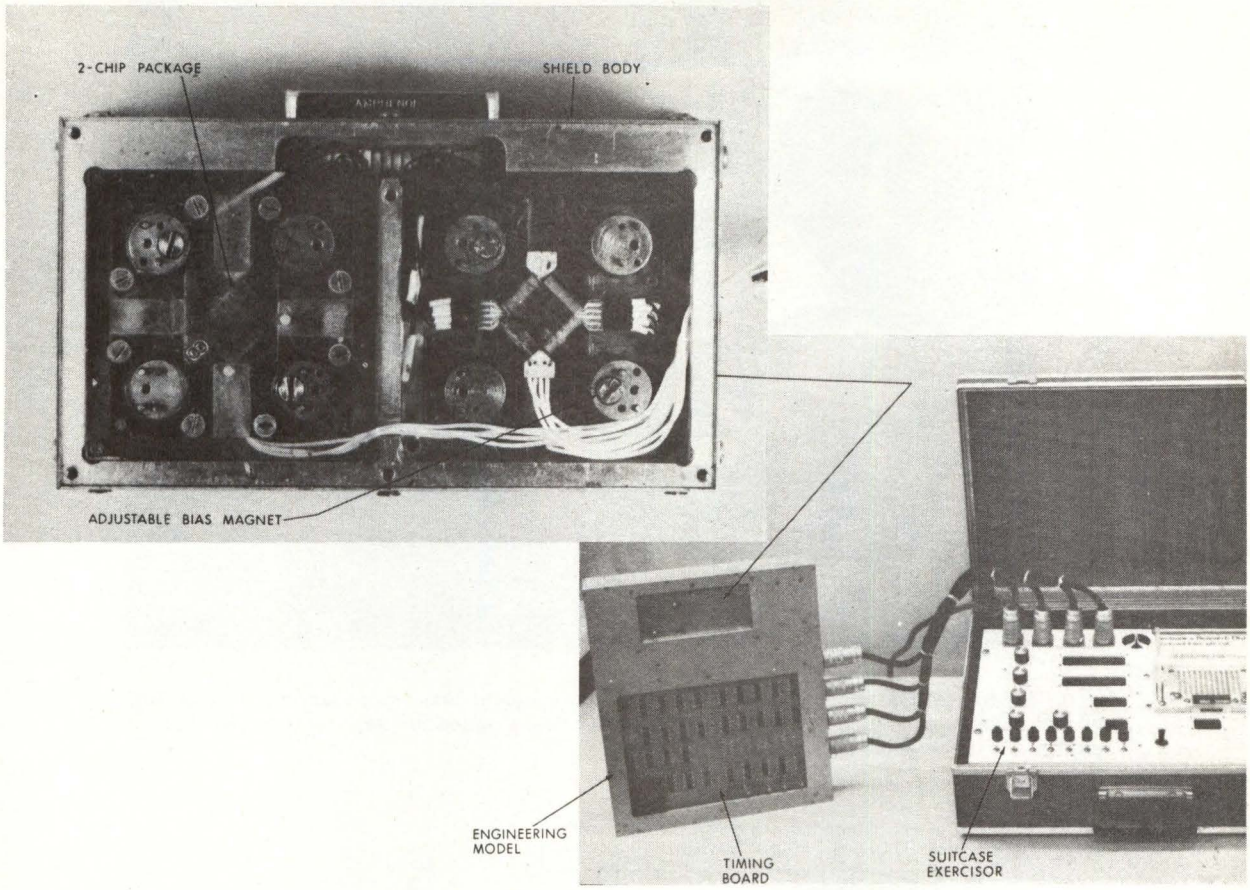

Fig 3 Engineering model of bubble recorder. Developed for NASA in 1974, capacity is 60k bits on three separate tracks. When operated at 150-kHz max data rate, power dissipation is 5 W/track. Magnetic bias assembly contains three ceramic packages. Sequential exerciser tests read, write, erase, and synchronous operation of recorder

packages, output signals are approximately 50 mV. A multiplexed sensing design is used where the sense amplifiers are bus-connected to minimize the number of components and power associated with bubble detection. Power dissipation in the coils and drivers is minimized by tuning the drive coils with capacitors at 150 kHz. Tank circuits are driven in parallel resonance with a periodic digital refresh switch circuit.

A prototype of a 10^8 solid state data recorder (SSDR) for space applications was delivered to NASA in 1978. Design requirements involved space environments, including launch vibration, near earth radiation, low power availability, and potentially long missions. Basic storage for this recorder is a 102.4k-bit serial register chip with provision for bubble generation, annihilation, and sensing. Active storage of the chip is in an epitaxially grown, doped garnet film on a non-magnetic garnet substrate. Permalloy and aluminum depositions on the surface control bubble generation, detection, and propagation. Sixteen chips are mounted on two substrates per cell, as shown in Fig 4, providing a total cell capacity of 1.64M bits and a total recorder capacity of 168M bits divided in two storage modules of 32 cells each.

Cell design reflects several tradeoffs. Sixteen single-chip cells are easily driven because the coil volt-ampere (VA) product is low; therefore, components are inexpensive and readily implemented. A single 16-chip cell, however, has lower total power per word and better volumetric efficiency. Any number of realistic estimates would probably show an optimum 8- to 16-chip cell capacity on the basis of a 150-kHz rotating field rate, available drive transistors, and thermal considerations. The cell design adopted for the SSDR as a result of tradeoffs has a volume of 2.2 in^3 (35.2 cm^3) and a weight of 0.25 lb (0.11 kg), and dissipates 11.4 W when operated continuously at 150 kHz.

Control of all recorder functions is accomplished by a master control unit (MCU) (Fig 5). Central to unit operation are four 8-bit PPS8 microprocessors. In addition, the MCU contains command interface, timing, and sequencing logic for the data storage. By changing the

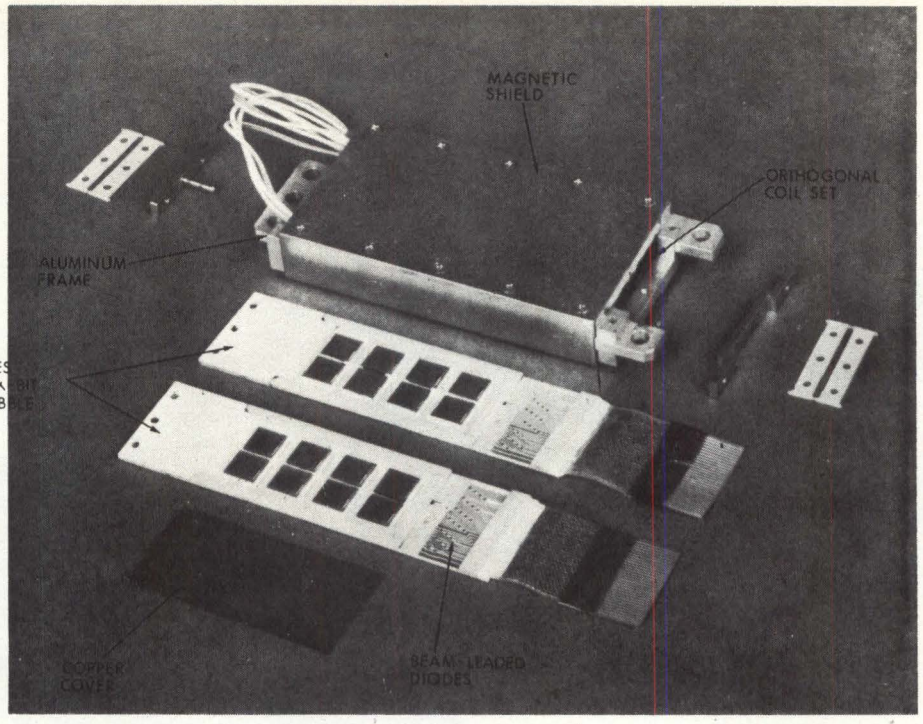

Fig 4 16-chip bubble memory cell. It consists of magnetic assembly, orthogonal coil set, and two substrates with eight bubble chips each. Beam-leaded diodes are for selection in sensing and generation and annihilation matrices

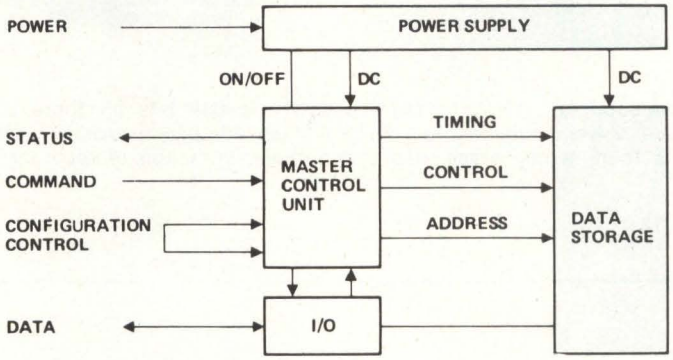

Fig 5 SSDR block diagram. Microprocessor control of modular bubble storage offers capabilities not possible with conventional tape recorders. Data rate can vary from dc to 2 MHz over one to four channels with mixture of write and read operations. Commands at MCU control power, I/O, and bubble storage

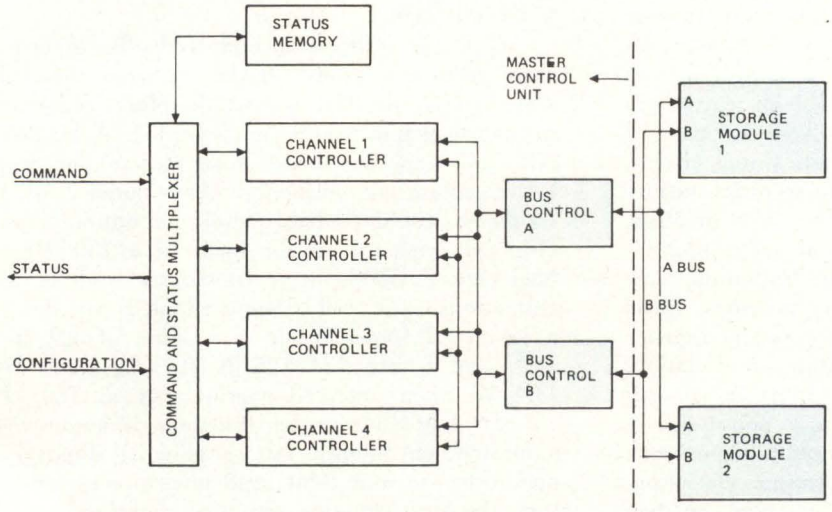

Fig 6 SSDR organization. Configuration can be changed from 1- to 4-channel recorder. Single points of failure have been eliminated by dual bus structure

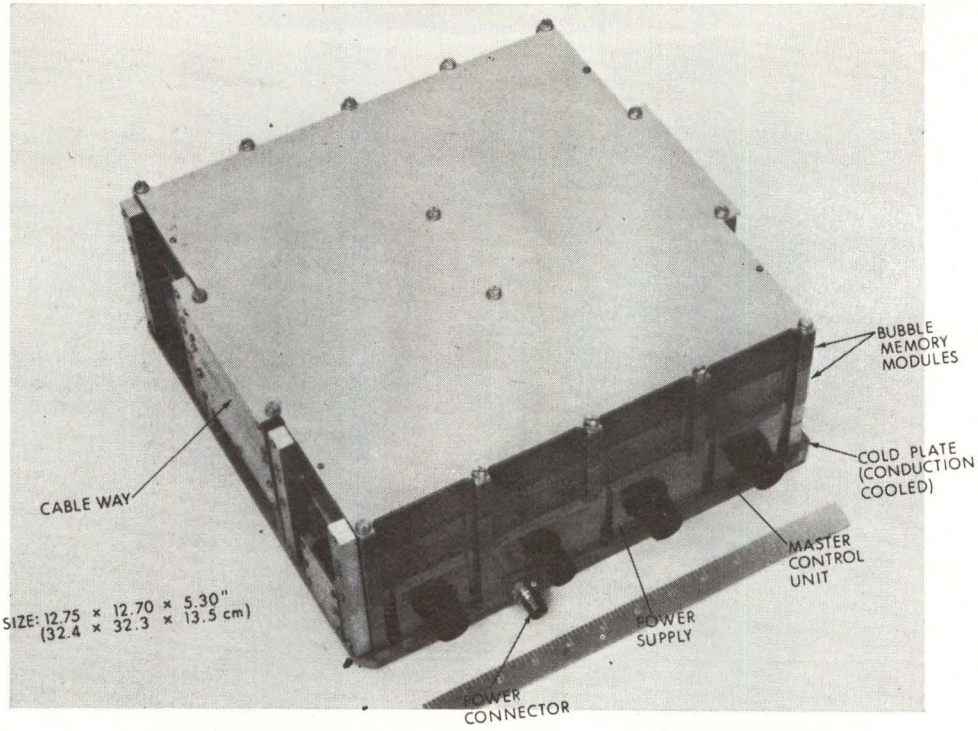

Fig 7 Spacecraft data recorder. 10^8-bit unit weighs approximately 47 lb (21.2 kg), occupies 860 in^3 (13,760 cm^3), and is conduction cooled through cold plate. Structural design is based on environmental and thermal considerations, while materials have been selected to meet thermal vacuum and heat sterilization requirements

configuration control either by hardware or software, the recorder can be changed from a single-channel recorder of 10^8-bit capacity and 1.2-MHz max data rate, to a four 2.5 x 10^7 bits/channel recorder operable asynchronously to 2.4 MHz. Each channel has its own microprocessor based controller (Fig 6) for independent control of data rate, monitoring of system status, and bubble storage allocation. Storage modules are accessible through either the A or B bus so that failures occurring in either of the bus controls, or any of the controllers, can be bypassed.

To be reliable, small in size, and low in power, mass storage must be carefully organized to minimize overhead electronics. Storage module electronics (Fig 6) are divided into a sensing matrix, an operator (generation and annihilation) matrix, and a coil drive matrix, each of which conserves volume and power by sharing overhead electronics between cells. Beam leaded diodes are used for selection in the sensing and operator matrices. The SSDR design (Fig 7) is partially populated to a capacity of 13.1M bits in two storage modules, the top two slices, or frames. Next lower slice with the four connectors is the MCU. Two of the connectors are for command, one for status, and one for configuration control. The bottom slice with the small connector is the power supply, which converts 28 Vdc to the secondary voltages required by the recorder.

Critical design areas identified during the program require further development before environmental goals are satisfied. Extensive testing of the 100k-bit devices in the modules shows operation of the recorder is limited to a range of 0 to 40 °C because of chip propagation track limitations and because of noisy sense channels. A revised module design, currently in development, will remove the identified deficiencies. Modified chip design incorporates high temperature material, gap-tolerant permalloy elements, and improved detectors. A hermetically sealed cell design reduces noise coupling and coil power dissipation.

Major Design Considerations

Design of a memory using bubble storage devices differs from that of a memory with semiconductor devices, because bubble devices require magnetic fields for operation. A static field of about 150 Oe perpendicular to the chip surface is required to create stable bubble domains. Thus, a magnetic structure is needed that is small and lightweight; matches the chip temperature coefficient; provides a stable, uniform field;

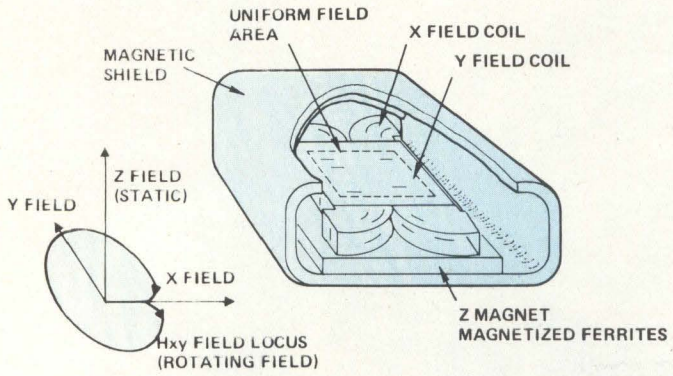

Fig 8 Magnetic field structure. Magnets inside shield produce vertical field normal to chips while x coil and y coil produce rotating field vector in chip plane. Coil envelope holds two carriers

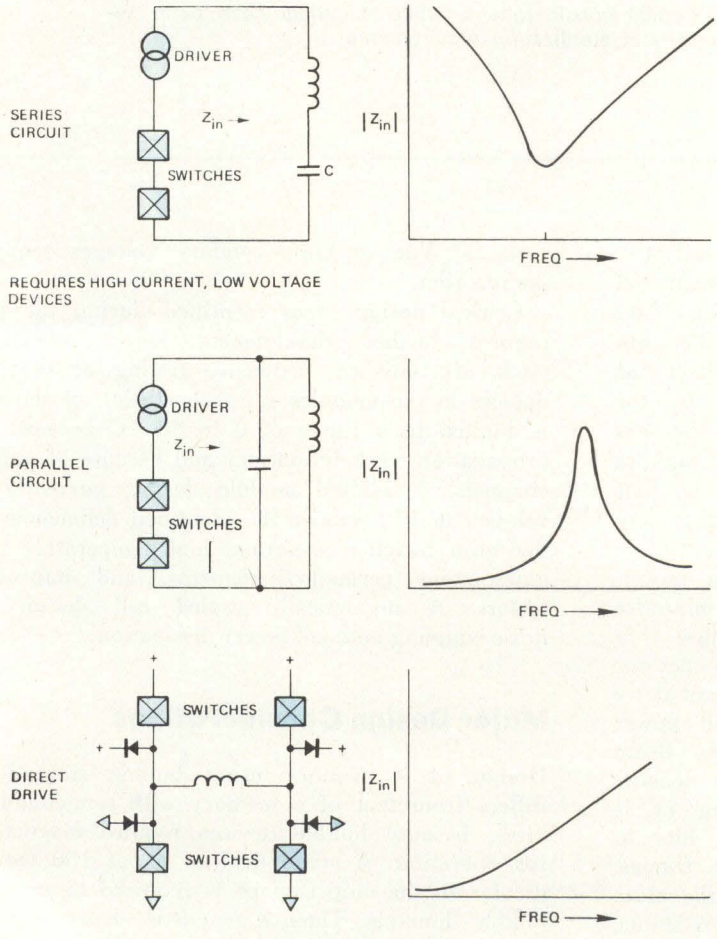

Fig 9 Three methods for driving coils. Series tuned circuits require high current low voltage drivers, while parallel tuned circuits require low current high voltage devices. Direct drive circuits are advantageous where many cells are matrixed, as in mass memory

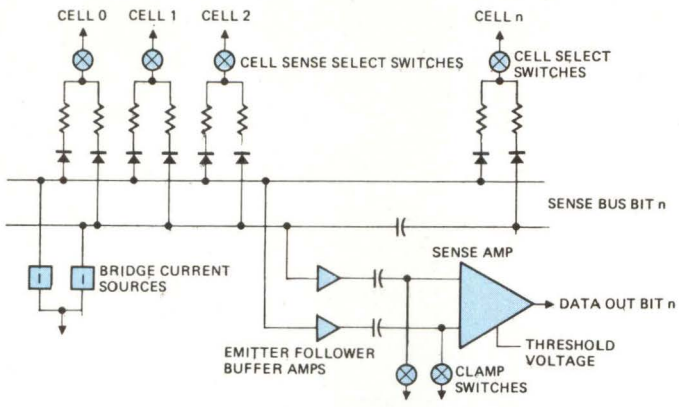

Fig 10 Matrixed circuit for sensing multiple chips. Matrixing is important in mass memory and recorder designs to reduce overhead electronics

and is not affected by external magnetic fields. In the most commonly used design, a magnetic shield surrounds the chips (Fig 8) and has a magnet attached to its upper and lower inside surfaces. Chips are located in the gap between the two magnets where the field is uniform. The magnetic shield design is adequate, but in space applications, shield weight is a considerable burden. Therefore, the tendency is to enclose as many chips in one structure as is practicable based on a statistical selection of chips with overlapping field requirements and common temperature coefficients.

To move bubble domains around the register permalloy pattern requires two inplane fields of about 50 Oe each, provided by a pair of orthogonal coils. These rotating field coils can contain only a limited number of chips governed by drive voltage and drive current capabilities of available semiconductors. Essentially, the coil VA product, which is proportional to frequency, volume, and magnetic field squared, expresses the available tradeoffs. The relationship suggests that the coil field has the most effect on the VA product, but volume probably has the largest potential for optimization. In the SSDR coil, actual chip volume is 0.016 in^3 (0.26 cm^3), whereas field volume is 0.22 in^3 (3.52 cm^3), an order of magnitude potential for improvement. Of course, other factors such as mechanical requirements, power losses, and heat removal affect the tradeoffs.

Fig 9 shows three common methods for driving coils. At the top is a series circuit which predominated in the early development phase. In series circuits, all pass elements, including leads, must be able to carry maximum coil current. The resistor voltage drop, plus semiconductor junction drops (0.6 V $\times$ number of junctions) times the current is the power loss. Because of semiconductor junction characteristics, power dissipation does not decrease as a function of increasing coil Q. On the other hand, a parallel circuit of high Q requires very low current from the driver making possible lower dissipation in the pass elements as Q is increased. For low power applications, where a high Q coil is used, the parallel tank circuit appears to be the most satisfactory.

Both methods, however, suffer from inherent timing and amplitude instability due to component and temperature variations for high Q. At the bottom of Fig 9 is a direct drive circuit, the design chosen for the SSDR. It has the advantage of being stable and, most important to recorder design, can be easily matrixed, but at the price of higher power dissipation.

Another major consideration is detection of the magnetic field from a tiny 4-μm bubble in the presence of a coil field and system noise. The bubble is first stretched into a strip about 1 mm in length along a permalloy magnetoresistance detector. This strip field changes the resistance of the detector about 0.3% compared to an adjacent identical detector without a bubble. The difference signal is amplified and discriminated to provide a TTL level signal.

Functionally, most sense channel designs contain a current source or resistor pair to supply bridge current, emitter followers to lower impedance, coupling capacitors, a clamp, and a latching sense amplifier. In addition, mass memory or recorder designs, such as the SSDR, are configured to share costly or bulky components (Fig 10). An ac coupled sense channel seems a logical choice when signal level is about the same magnitude as amplifier offsets and much smaller than system transients. In operation, the amplifier input is clamped to ground during system transients

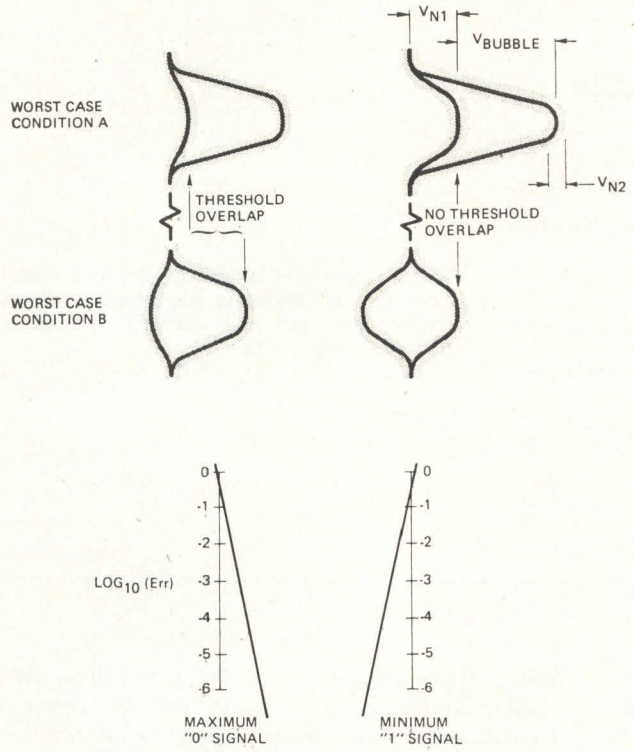

Fig 11 General aspects of sensing many bubble detectors on common differential bus. Total systematic noise (V_{N1}) is bipolar, while bubble signal (V_{BUBBLE}) is unipolar. Random noise (V_{N2}) is primarily detector switching noise. Adequate control of total noise is necessary to ensure reliable detection. System error rate (lower curves) depends on composite signal overlap and random noise

and released just before signal time. To minimize detector loading, high impedance current sources are used to provide the current for the detector and dummy, and emitter followers are used to buffer detectors from restore and amplifier circuits.

Two general aspects of the sense channel design are most critical (Fig 11). First is variation in parameters of detector sensitivity, detector dummy balance, and common mode conversion. Second are the various noise sources: random detector, coil field ($d\phi/dt$), coupling, and system noise. Parameter variations and systematic noise determine the total minimum composite signal overlap when several chips are connected on a common differential sense bus. Random noise determines how closely the threshold can approach the minimum "1" or the maximum "0" and still guarantee the desired error rate. Magnetic domain switching variations cause most of the random noise, with thermal noise as a minor contributor.

Summary

Because of the high failure rate of mechanical tape recorders in a space environment, NASA determined to implement an investigation of the totally solid state bubble domain data recorder. Such a recorder has been developed which offers a flexible, low power alternative to conventional magnetic tape recorders. Steps in the evolution of the bubble device design are traced through storage configuration, magnetic circuit design, control elements, and packaging organization.

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Oliver D. Bohning is a memory development engineer in Rockwell's Autonetics Strategic Systems Division. Primarily involved in working on high density bubble memory development activities, he is presently working on the development of standard memory modules for NASA applications. He holds a BEEE degree from the University of Minnesota.

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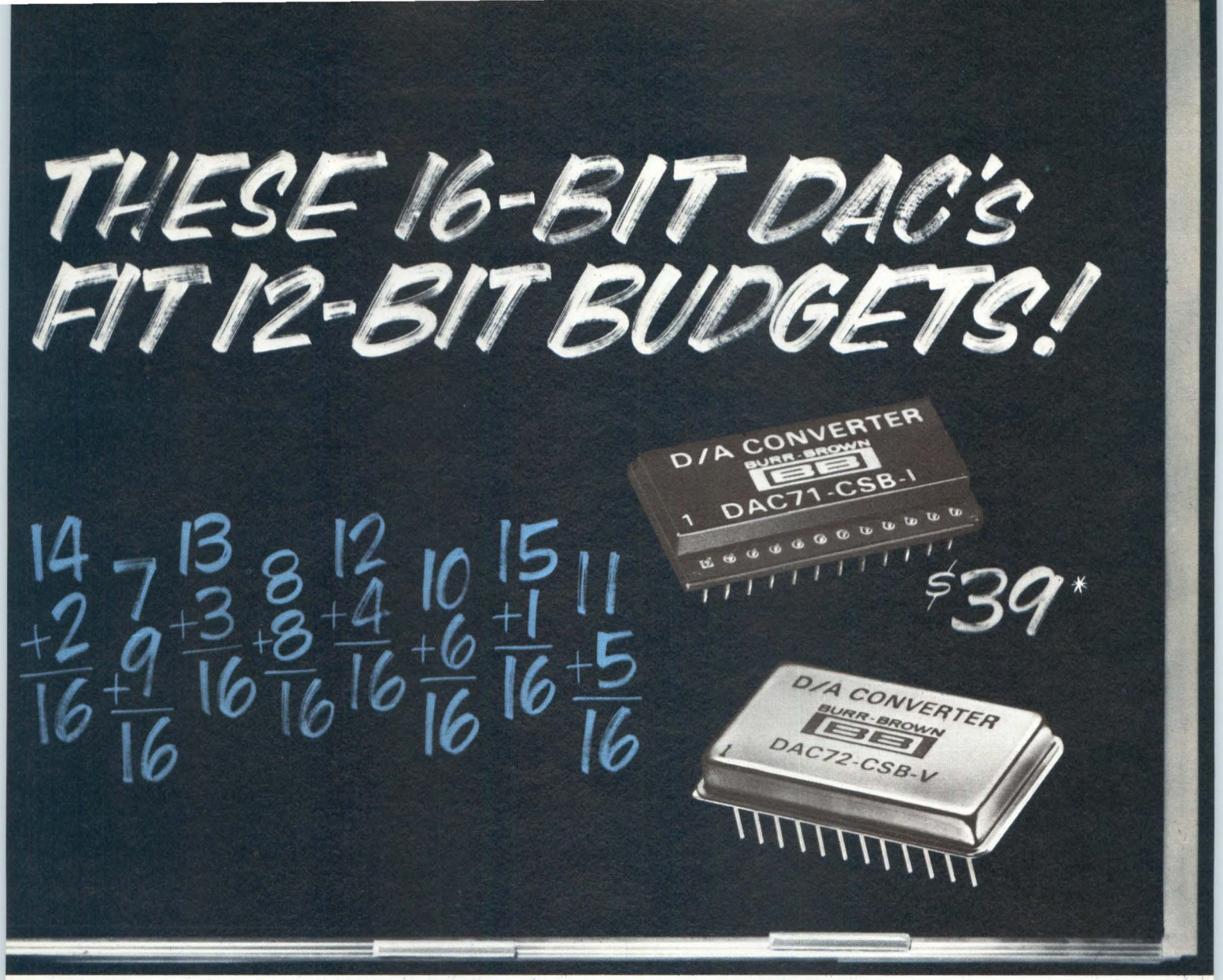

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DESIGN NOTE

RAM Tester Adapts to Memory Interface Requirements

Clock and counter hardware compose static RAM chip tester that writes, reads, and validates test data patterns for different memory organizations by modifying counter bit lengths and clock phases

Alan W. Bentley Cubic Corporation, Defense Systems Division, San Diego, California

The need for a static random access memory chip tester to support a microprocessor based system development led to a flexible memory testing approach that can be generalized to fulfill most memory testing requirements. By using multiphase clock and counter logic, with minimum additional hardware, control and test commands are generated to write, read, and validate test data patterns for each memory address location. Test parameters, such as various data patterns or the number of times each address location is tested, are chosen by adjusting the bit length of the counter logic output. Memory control line activation through the test patterns is repetitive and is derived from logical combinations of the counter contents and the clock phases, while meeting memory timing requirements.

Memory Interface Requirements

Memory to be exercised is a 1024-bit static silicon gate complementary metal oxide semiconductor random access memory (CMOS RAM), MM74C921, organized as 256 address locations of 4 bits each. Access is through a noninverting bidirectional data port (D1 to D4) with 3-state output control, thereby permitting bus organization (Fig 1). All four RAM control lines—strobe ($\overline{ST}$), chip select stored ($\overline{CES}$), chip select level ($\overline{CEL}$), and write enable ($\overline{WE}$), are active low (digital 0).

The falling edge of $\overline{ST}$ stores the eight address bits (A0 to A7) and $\overline{CES}$ in an internal memory input storage register. The rising edge of $\overline{ST}$ loads the 4-bit data output into an internal data storage register that drives 3-state buffers. These buffers are switched to the active state by ANDing $\overline{CES}$ and $\overline{CEL}$, both active low with $\overline{WE}$ high or inactive; therefore, data can be read from RAM only when both chip selects are in the active state and a write cycle is not in progress (Fig 2).

Control line sequencing is as follows for either a read or a write cycle. The 8-bit RAM address (A0 to A7) is placed on the address bus, the $\overline{CES}$ input line is driven to active low, and then $\overline{ST}$ is driven to active low, storing the address and $\overline{CES}$ internally. For a read cycle, addressed data are stored in the data output register on the rising edge of $\overline{ST}$, and then placed on the output data

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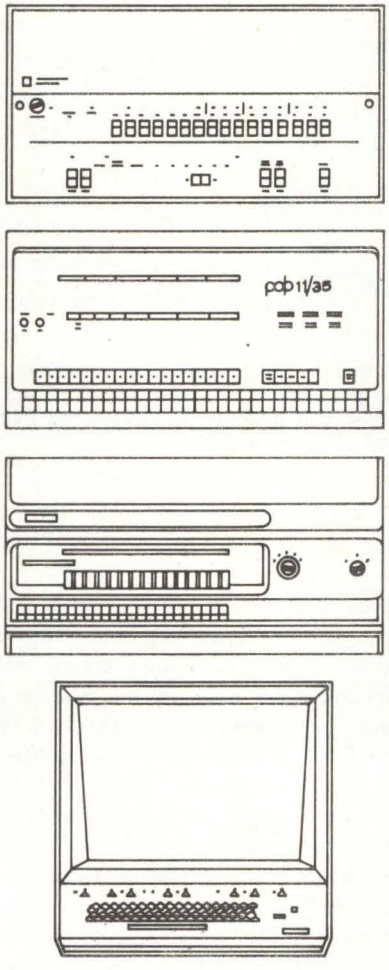

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RAM ADDRESS	REPETITIVE TESTS EACH ADDRESS	NUMBER OF RAM ADDRESS SEQUENCES
2^3-2^{10}	1	16
2^4-2^{11}	2	8
2^5-2^{12}	4	4
2^6-2^{13}	8	2
2^7-2^{14}	16	1

TEST SEQUENCING POSSIBILITIES WHEN USING 16-BIT COUNTER (2^0-2^{15}). RAM ADDRESS COMBINATIONS RANGE FROM 2^3 THROUGH 2^{10} to 2^{N-9} THROUGH 2^{N-2}.

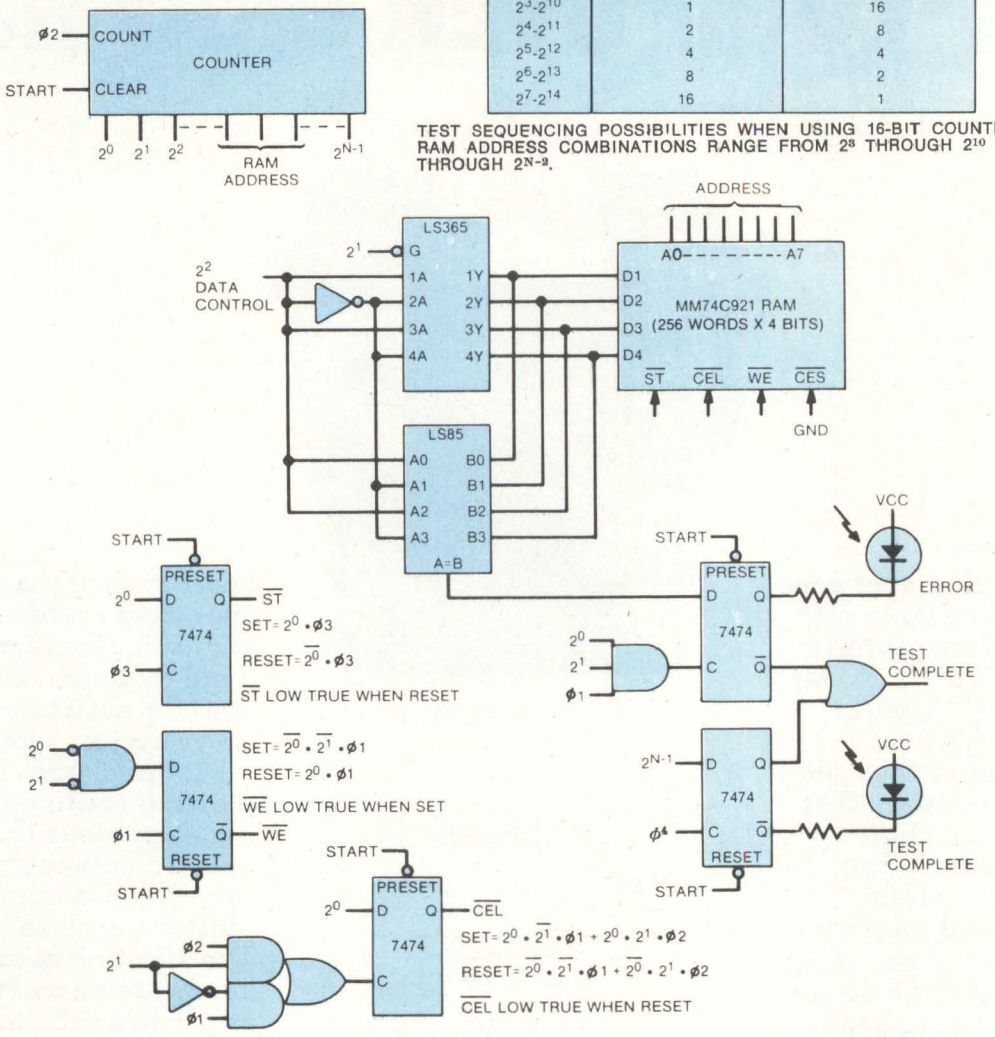

Fig 1 Logic circuits of RAM tester. Table illustrates variations in test sequence by RAM address selection. Counter bit length determines test duration and number of tests at each address. Initial condition of counter and flipflops is established by START command. Flipflop input gating establishes control signals shown in Fig 2

bus by switching on the 3-state buffers with $\overline{CEL}$ active low, $\overline{WE}$ inactive high, and $\overline{CES}$ active low, which had been stored on the $\overline{ST}$ leading edge. If a write cycle is desired while $\overline{ST}$ is active low, the data to be written into the stored address must be placed on the data input lines with $\overline{CEL}$ and $\overline{WE}$ both active low. With all control lines active low, an internal write control command is enabled. When any one of the control lines is driven to inactive high, the rising edge from the internal write control command stores the input data in the addressed location. Since the bidirectional data bus is active during the memory write cycle, the memory output buffers must be held in the 3-state or standby condition. As either $\overline{WE}$ low or $\overline{CEL}$ high selects this condition, standby is maintained by simultaneously driving both signals from the active to inactive state.

Memory access timing restrictions generally fall into two categories. First are the setup and hold times for input stability requirements preceding and following a control signal activation. Second is sequencing time, the minimum time that a control line must be active, or the minimum time between sequential control commands. Setup and hold times for both the address and $\overline{CES}$ inputs measured from the falling of $\overline{ST}$ are 25 ns each. When writing, data setup and hold times are 90 and 60 ns, respectively, measured from the rise of the internally generated write control command. This command must be active low at least 130 ns prior to rising.

When either reading or writing, the minimum $\overline{ST}$ width is 130 ns, and the minimum time between successive memory cycles is 255 ns.

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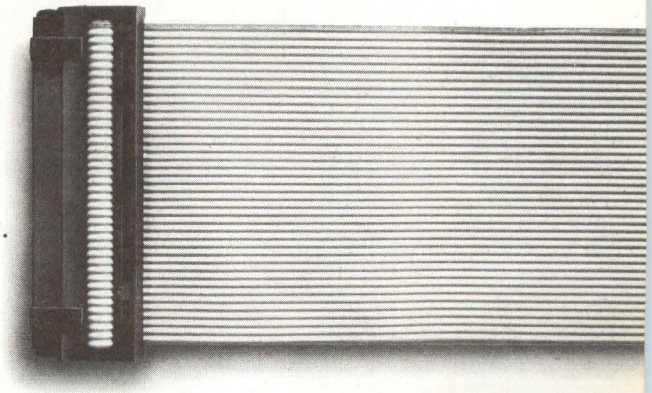

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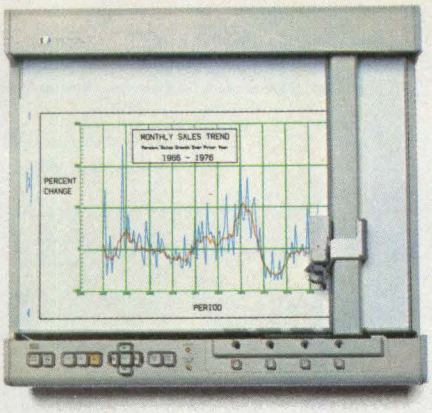

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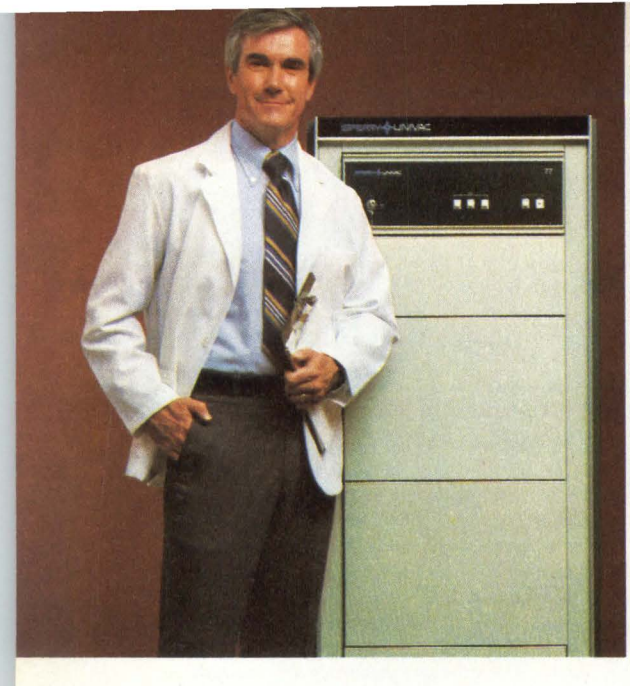

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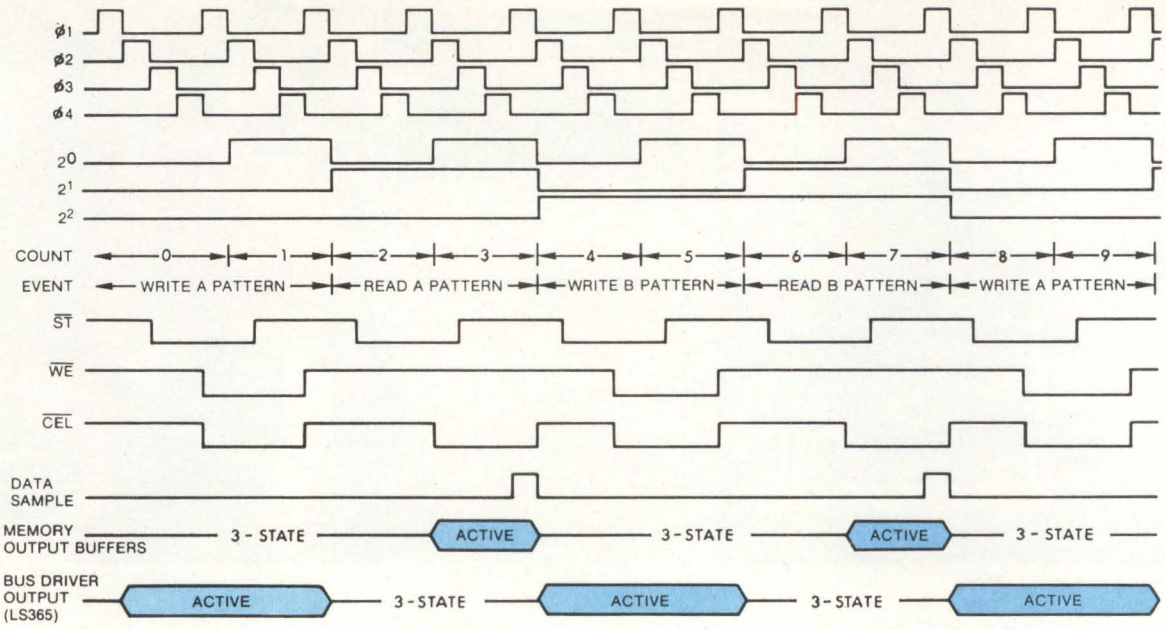

Fig 2 Test timing diagram. Relationships are shown between four clock phases, three counter outputs, control and test signals, and data sample. Also shown are active states of bus driver and memory 3-state output buffers

When reading data, the time from the rising of $\overline{ST}$ to the completion of data storage in the output registers and the time to enable the 3-state buffers by $\overline{CEL}$ are 90 and 130 ns, respectively.

RAM Test Principles

The static RAMs under test are used in a TMS 9900 based microprocessor system that utilizes a 4-phase, 3-MHz clock generated by a 74LS362 clock chip. This microprocessor requires two clock cycles, 8 phases or 667 ns, to complete one memory access cycle. To perform memory testing, a read or write cycle must be completed within eight clock phases. To relate memory timing requirements to the system clock, the address and $\overline{CES}$ setup and hold times are less than one clock phase, and the data set up and hold times are less than two and one clock phases, respectively. The $\overline{ST}$ and $\overline{WE}$ commands must each be valid for a minimum of two clock phases and, when reading, output data will be valid two clock phases after the rising edge of the $\overline{ST}$ command and activation of the 3-state buffers.

System development proceeds through two stages: first, establishment of the hardware logic relationships and the sequence of test events and, second, specific selection of counter outputs and clock phases to fulfill memory timing criteria. To meet the test relationship of completing one memory cycle, each containing two clock cycles, and to institute the test sequence of initially writing and then reading one data pattern, and next writing and reading the complementary or inverse data pattern, the assignment of events for an accumulated count can be established. The test sequence requires eight counts (0 to 7) and is repetitive; therefore, control and test commands can be derived from logical combinations of the three least significant counter outputs (2^0, 2^1, and 2^2) and four clock phases ($\phi 1$ to $\phi 4$).

In Fig 1, an N-bit counter, 2^0 through 2^{N-1}, is cleared upon start and is then incremented by one after each clock cycle. Four inputs (1A to 4A) to 3-state buffers (74LS365) and to one word (A0 to A3) of a data comparator (74LS85) are connected with alternate bits inverted so that complementary data patterns, either 1010 or 0101, can be generated by switching the 2^2 data control line from the counter. The RAM 4-bit bidirectional data port (D1 to D4 is connected to the output of the 3-state buffer (1Y to 4Y) and to the other input word of the data comparator (B0 to B3). The test sequence requires selection of one test data pattern and enabling of the bus 3-state buffer to pass this pattern to the RAM data port while executing a memory write cycle. Then, while maintaining the same address and test data pattern, and with the LS365 buffers switched to the 3-state mode, a memory read cycle is executed to validate the data. Memory data are valid when both data words are identical and the A = B output of the LS85 comparator is a logic 1. In Fig 2, the read and write patterns are directly related to the counter 2^1 bit; therefore this bit can be used to switch the control input (G) of the LS365 buffer. The data pattern must remain valid for an entire write and read sequence, then complemented for the following write/read sequence; this is accomplished by driv-

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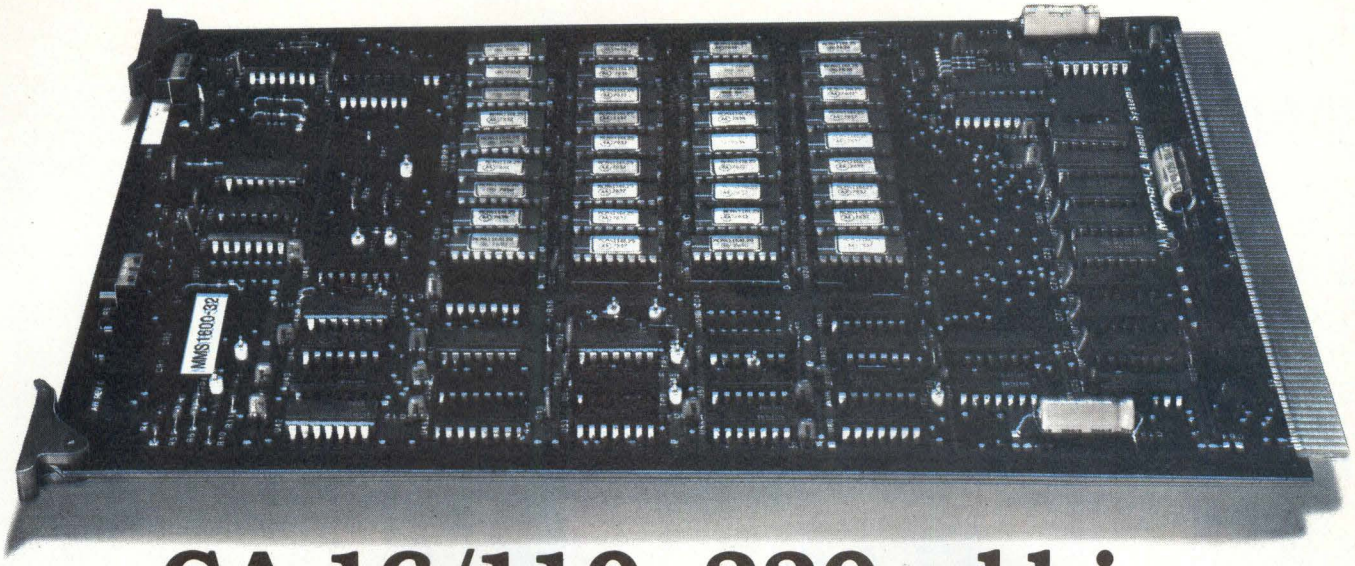

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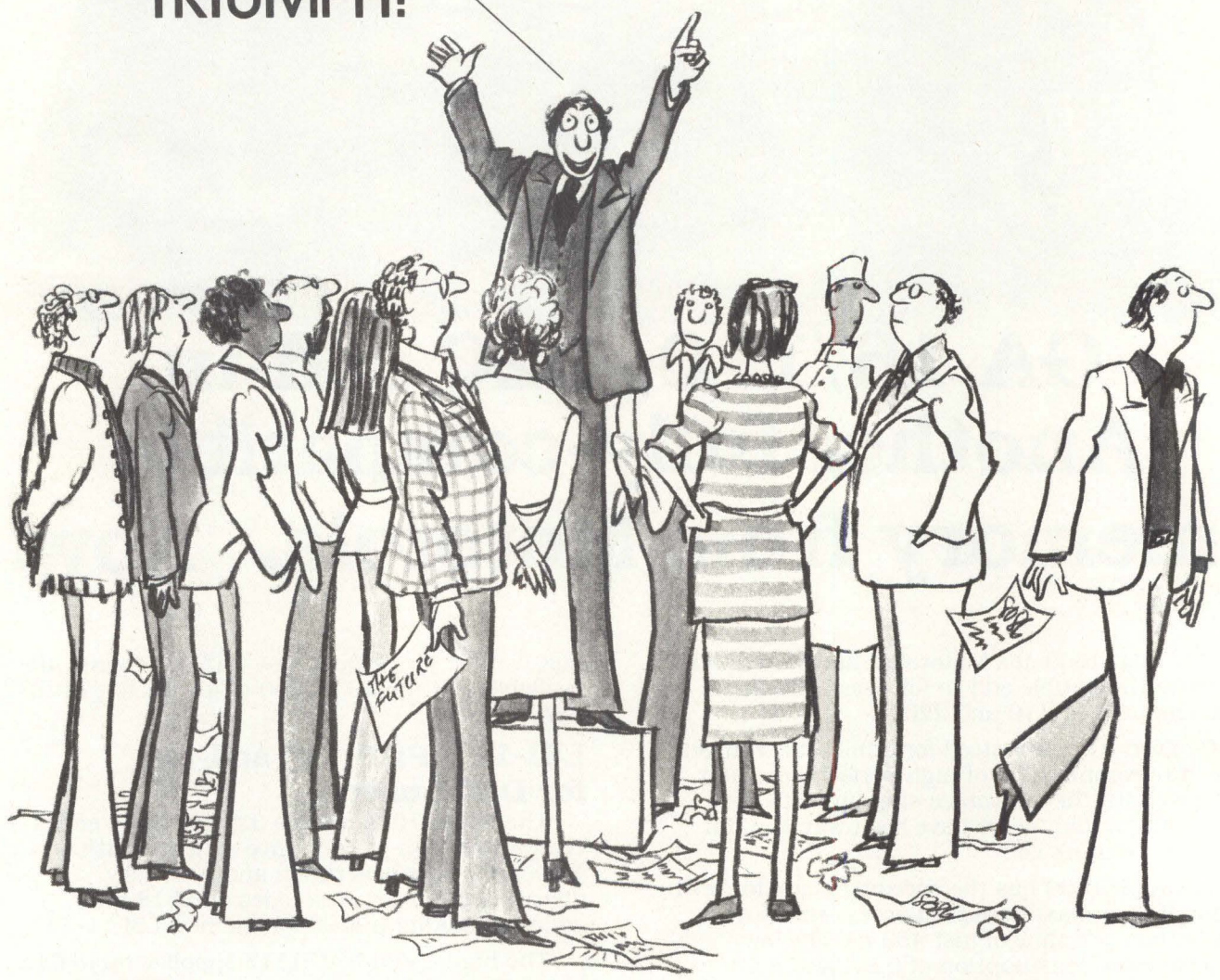

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ing the data control line with the counter 2^2 bit.

Control Signals

The strobe command ($\overline{ST}$) is required for every memory cycle; therefore, it must be initiated at each even count, ie, 0, 2, 4, etc (Fig 2). To meet timing requirements with minimum hardware, $\overline{ST}$ command is generated one clock phase after data are established and maintained for one clock cycle. Write enable ($\overline{WE}$) is required on alternate memory cycles, ie, 0, 4, 8, etc. Timing restrictions are satisfied by generating a $\overline{WE}$ command of one clock cycle duration, two clock phases after $\overline{ST}$. This event occurs only when the counter 2^0 and 2^1 outputs are false.

For write cycles, $\overline{CEL}$ active low is an element of the RAM chip internal write control; however, $\overline{CEL}$ must be equal to or encompassed by $\overline{WE}$ to prevent the memory output buffers from becoming active. When reading, data are stored in the memory output register on the rising edge of $\overline{ST}$, and two clock phases are required both from this data storage and from the activation of the output buffers by $\overline{CEL}$ until output data testing. Since memory output data storage occurs on the leading edge of clock phase 3, data cannot be sampled until the following clock phase 1; therefore, $\overline{CEL}$ must stay active low through clock phase 1 of the read cycle. For write cycles (counts of 0, 4, 8, etc) when the counter 2^1 bit is false, $\overline{CEL}$ is switched by clock phase 1 to align with $\overline{WE}$, ensuring that the output buffers will remain in the 3-state mode. During read cycles (counts 2, 6, etc) when the 2^1 bit is true, $\overline{CEL}$ is switched by clock phase 2, thus holding the output buffers active during the data sample time.

Fig 2 shows when the memory output buffers are active, and the data sample timing that complies with memory interface restrictions. The data control line is the counter 2^2 bit, and it is not changed between the memory write cycle and the data sample time. Therefore, the test patterns created by the data control line and read from the memory location should be identical. Both patterns are applied to the inputs of the LS85 comparator, and for a valid write and read cycle, the comparator A = B output will be true at data sample time. As shown in Fig 2, this data sample time occurs at clock phase 1 of counts 3, 7, etc, when the 2^0 and 2^1 outputs are both true. A clocking pulse (2^0, 2^1, and $\phi 1$) is generated at data sample time and is applied to the clock (C) input of the error flipflop (7474). The comparator A = B output is applied to the D input of the same error flipflop; this output is false if the comparator inputs are different, causing the clocking pulse to reset the error flipflop, to light the error light emitting diode (LED), and to generate a test complete signal to stop the counter. If sampled data are always correct, the error flipflop remains set. Testing continues until the counter 2^{N-1} line becomes true; then, the test complete flipflop is set, which illuminates the test complete LED and generates the test complete signal.

The RAM address is supplied by the counter bits between 2^2 and 2^{N-1}. The counter bit length determines the number of test patterns completed in a test cycle (Fig 1). In this application, the RAM requires 8 address bits (256 address locations); thus, the minimum counter length is 12 bits with 2^3 through 2^{10} used for address and 2^{11} for the test complete bit, 2^{N-1}. This configuration tests each address location with one write and read cycle. Note that expansion of the counter bit length results in multiple tests of each address location. For example, by using a 16-bit counter, counter bits 2^3 through 2^{14} are available for RAM addressing. Four of these counter lines are not needed to create 256 RAM addresses and when the change in the counter output is confined to these lines, the RAM address remains unchanged, thereby causing repetitive testing. In this instance, there will be 2^4 or 16 tests at each address location. When excess counter outputs are available, the sequence of address testing can be varied by selection of the addressing lines. Upon initiating a test, timing is synchronized, all flipflops and the counter are reset, and test sequencing continues until either the error flipflop or the test complete flipflop is set, either of which lights the appropriate LED and issues the test complete signal to interrupt the sequence. The test is run at a go/no go level. If further investigation is desired, the counter reading, upon sequence interruption, provides the memory address and the data pattern of the failure.

Summary

This RAM tester design concept is flexible and, through modification of the control and addressing schemes, can be adapted to fulfill different memory testing requirements. For example, the write and read cycles do not have to be performed consecutively; instead, data can be written into blocks of addresses. Then, the block can be read and verified. This approach can be accomplished by selecting different counter outputs when forming the address and control functions. Reordering the test sequence permits testing memories with inherent latency, such as magnetic bubble, charge-coupled devices, or conventional shift register. Similarly, dynamic RAM testing can be organized to insert one or several refresh cycles between the write and the read and verify cycle.

This direct test method meets memory control and timing requirements with a minimum amount of hardware. The procedure can be generalized to test different memory organizations by initially selecting a clock frequency consistent with memory timing requirements and then by establishing appropriate control signal and addressing sequences.

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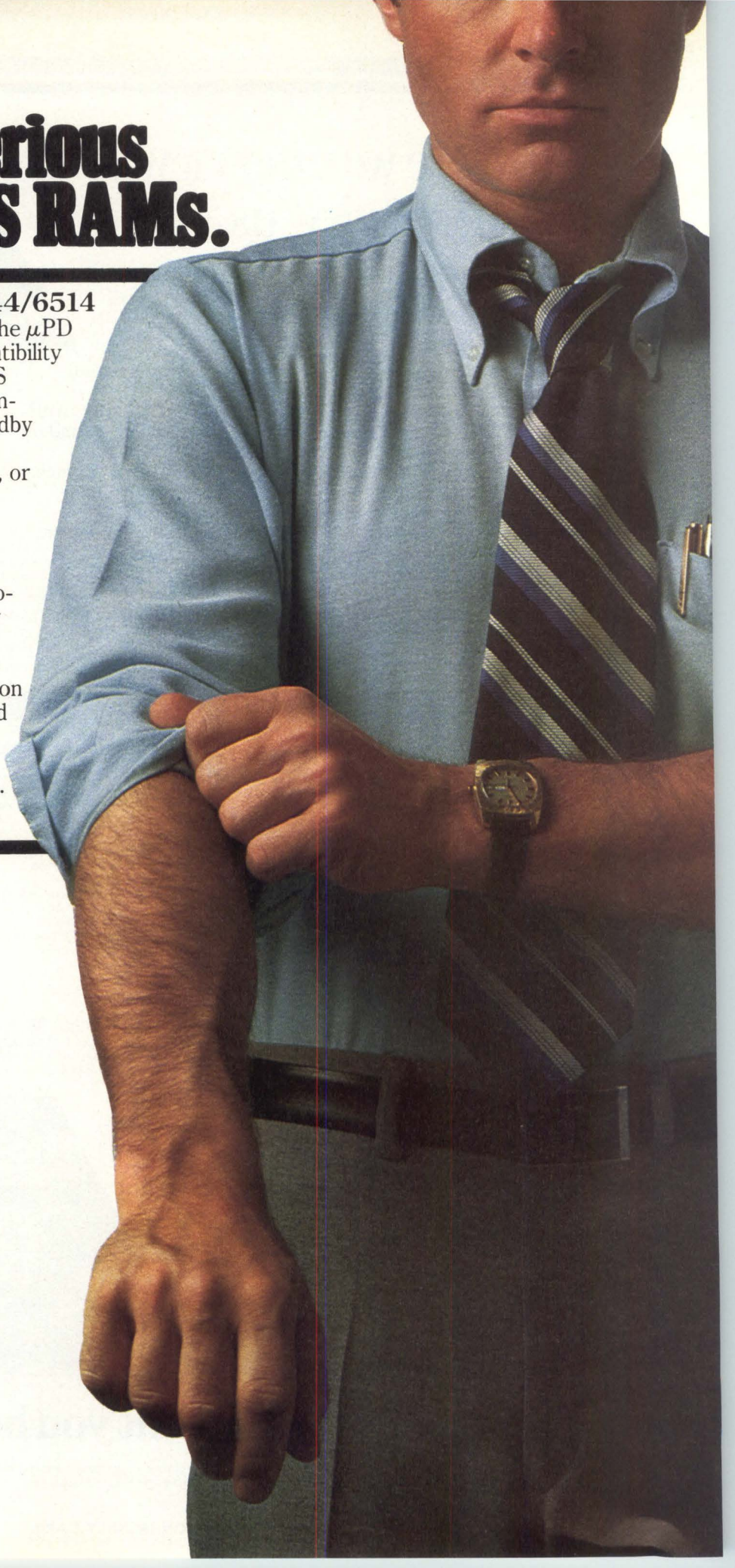

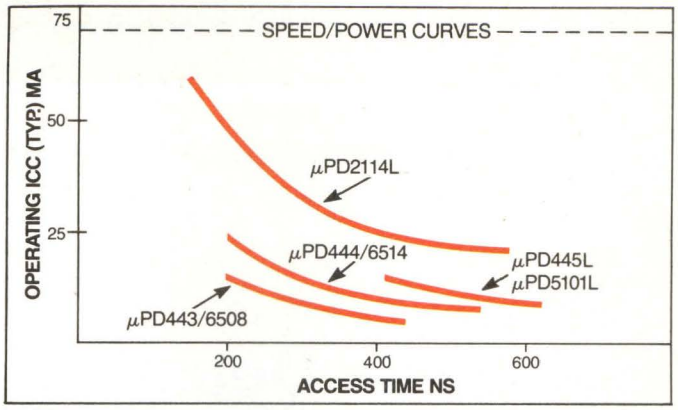

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μPD444/6514C-1	300 ns	60 mW	18	.065 μW	.022 μW
μPD444/6514C-2	250 ns	75 mW	18	.065 μW	.022 μW
μPD444/6514C-3	200 ns	95 mW	18	.065 μW	.022 μW
μPD445LC	650 ns	45 mW	20	100 μW	1 μW
μPD445LC-1	450 ns	75 mW	20	100 μW	1 μW
μPD5101LC	650 ns	45 mW	22	1 μW	.016 μW
μPD5101LC-1	450 ns	75 mW	22	1 μW	.016 μW
μPD443/6508C/D	450 ns	25 mW	16	5 μW	.3 μW
μPD443/6508C/D-1	300 ns	45 mW	16	5 μW	.3 μW

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APPLICATION NOTE

High Level Design Language Develops Low Level Microprocessor-Independent Software

Proposed software development approach frees the programmer from constraints of specific microprocessors by implementing software on any available high level language computer system

D. B. Wecker, R. L. Krutz, and D. T. Tuma Carnegie-Mellon University, Pittsburgh, Pennsylvania

The development cycle from code writing to assembling, debugging, and rewriting is difficult and time consuming when developing software for new microprocessors. A programmer creating a software system on the object machine usually has few tools, if any, to work with, and must, therefore, hand-assemble various versions of the code. If a development system or a downloading large computer is used, debugging tools are available, but the cost of such systems, with the amount of memory required, is relatively high compared to the microcomputer system itself. Using these methods, the programmer normally writes the code in assembly language—a lengthy process. Use of a higher level language for code generation circumvents this difficulty, but languages applicable to a variety of microprocessors are either nonexistant or have not yet reached maturity.

A simple technique can solve these problems. It requires no specialized hardware, is easy to learn, and rapidly creates an end result—a high level language that can be altered and debugged with minimum effort. The high level implementation can be translated almost line for line into assembly code, thus speeding code generation. In addition, reasonably accurate estimates of memory space needs and execution times can be obtained prior to implementation on the microprocessor system. The methodology can be used with several high level languages. To illustrate this generality, examples in FORTRAN, PASCAL, and SAIL (an ALGOL-like language) are presented.

Program Generation

After selecting a suitable (and available) high level language, the programmer must place restrictions on the software, since the end product will be implemented on a microcomputer. Variables must be integers, integers must be eight bits, arrays must be 1-dimensional, loops must have simple loop counters (usually ending or starting at zero), arithmetic operations must be those

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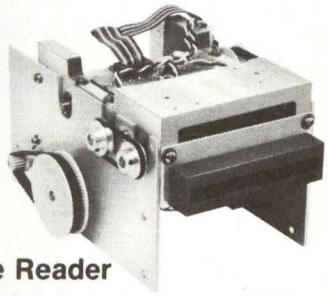

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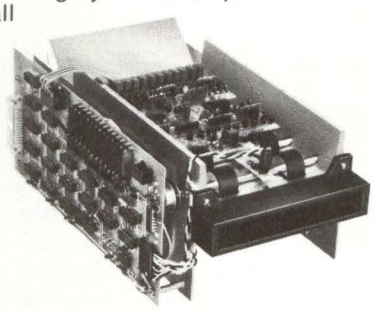

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performable by the object processor or those for which subroutines are available, and subroutines must be used wherever possible to keep from repeating the same code. Global variables must be allocated to two memory spaces—fixed or static and alterable or dynamic—for read only memory and random access memory, respectively; temporary variables must be used for computed values and addresses that are referenced frequently; and input/output (I/O) must be handled through subroutine calls, allowing for easy insertion into an actual object system when completed. All code must be written with the size and power of the object machine in mind; and since that is assumed to be an 8-bit microprocessor, the examples specifically apply to an 8080 central processing unit.[1]

The list of restrictions is not exhaustive, and may be altered to suit the programmer, based on familiarity with the technique. The programmer can develop an entire software system, and run and debug it, without ever using microprocessor hardware. Thus, generality of application is maintained while system algorithms are developed and tested.

Sample Programs

FORTRAN and PASCAL implementations of an averaging routine demonstrate the high level language technique.

NAME: AVE

USE: Find average of group of numbers

PARAMETERS: N—number of entries in array
X[ ]—array of numbers to average

Table 1 presents software for two implementations of the above routine and shows a typical hand translation of the FORTRAN routine. A second routine demonstrates the technique in SAIL (Stanford Artificial Intelligence Language).

NAME: SETBIT

USE: Sets and clears bits in an array of bytes

PARAMETERS: BYTPIN — top 5 bits: address of byte in array; bottom 3 bits: address of bit in byte
STATE — 1 to set bit: 0 to clear
BYTE[ ]—1-dimensional array of bytes

This implementation in Table 2 is also followed by a hand translation into assembly code.

TABLE 1

Averaging Routine

FORTRAN Implementation

```
C       Denotes program comment
C  THIS PROGRAM COMPUTES AN AVERAGE VALUE FROM A GIVEN
   VECTOR
      FUNCTION AVE(N,X)
C  EXPLICITLY DEFINE ALL VARIABLES, TO AID IN TRANSLATION
      INTEGER N,SUM
C  MAKE SURE THAT ARRAYS ARE NO MORE THAN 1 DIMENSION
      DIMENSION X(100)
C  THE ALGORITHM USED WILL BE
C    AVE = SUM(X(J),J=0,N-1) / N
C  >>>>>>> NOTE: SUM WILL HAVE TO BE DOUBLE PRECISION
C                WHEN TRANSLATED, OR THERE MAY BE
C                OVERFLOW PROBLEMS
C  INITIALIZE SUM
      SUM = 0
C  ADD UP ALL THE ELEMENTS
      DO 100 J=0,N-1
100      SUM = SUM + X(J)
C  CREATE AVERAGE AND RETURN
      AVE = SUM / N
      RETURN
      END
```

PASCAL Implementation

```
Procedure AVE(var AVEVAL,N: integer; x: array(0 . . 100) of integer0;
              var SUM,J: integer;
              begin
(*            The algorithm to be used will be:
                AVE = SUM(X(J),J=+O,N-1) / N
NOTE>>>>  sum will have to be double precision to avoid overflow
          when translated        *)
SUM   := 0;       (* initialize sum   *)
for J := 0 to N-1 do SUM := SUM + X[J];  (* add up elements   *)
AVEVAL := SUM div N   (* return value      *)
end { AVE } ;
```

Assembly Translation of FORTRAN Implementation

```
;  **** FUNCTION AVE(N,X) ****
ave:            push    b           ; save registers
                push    d
                push    h
; passed parameters:       a = N,    hl = X [ ]
; variables:               b = LOOP, c = copy of N, de = SUM
;   **** INTEGER N,SUM ****
;   **** DIMENSION X(100) ***
                mov     c,a         ; set up N
                mov     b,a         ; set up LOOP counter
;   **** SUM = 0 ****
                xra     a           ; clear accumulator
                mov     d,a         ; clear high part of SUM
                mov     e,a         ; clear low part of SUM
;   **** DO 100 J=0,N-1 ****
;   ****    SUM = SUM + X(J)  ****
ave1:           mov     a,m         ; get X(J)
                add     e           ; accum. = SUM(low) + X(J)
                mov     e,a         ; SUM(low) = accum.
                jnc     ave2        ; check for carry out
                inr     d           ; if there was a carry: SUM(high)+1
ave2:           inx     h           ; set up for next entry
                dcr     b           ; see if loop finished
                jnz     ave1        ; go to ave1 if not done
;   **** AVE = SUM / N ****
                mov     a,c         ; get divisor
                xchg    d           ; hl exchanged with de
                call    divide      ; subroutine to give: hl / accum.
;   **** RETURN ****
                pop     h           ; restore registers
                pop     d
                pop     b
                ret
:  **** END ****
```

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TABLE 2

Bit Changing Routine

SAIL Implementation

```
procedure SETBIT(integer BYTPIN,STATE);
begin
integer BYTNUM,PINDAT;
BYTNUM ← (BYTPIN lsh -3) IAND '037;
PINDAT ← 1 ISH (BYTPIN IAND 7);
if STATE then
      BYTE[BYTNUM] ← BYTE[BYTNUM] IOR PINDAT
else  BYTE[BYTNUM] ← BYTE[BYTNUM] IAND INOT PINDAT;
end;
```

Assembly Translation of Sail Implementation

```
; **** PROCEDURE SETBIT (INTEGER BYTPIN,STATE) ****
setbit:         push    b           ; save registers
                push    d
                push    h
;
; Passed parameters:      b = BYTPIN,   c = STATE
; Variables:              e = BYTNUM, hl = BYTE[ ]
;                                 d = PINDAT
; **** BYTNUM ← (BYTPIN ISH -3) IAND '037 ****
                mov     a,b         ; get input command
                rrc                 ; transform command
                rrc                 ; into address in array
                rrc                 ;
                ani     37          ; finish transformation
                mov     e,a         ; save result in e
                mvi     d,0         ; de = offset into BYTE [ ]
                lxi     h,BYTE      ; form actual address of desired byte
                dad     d           ; hl = BYTE[BYTNUM]
; **** PINDAT ← 1 ISH (BYTPIN IAND 7) ****
                mov     a,b         ; obtain bit number
                ani     7
                mov     b,a         ; save in b
                mvi     a,1         ; place bit to be set in a
setbi1: dcr     b
                jm      setbi2      ; move bit to correct position
                rlc
                jmp     setbi1
setbi2:         mov     d,a         ;save bit to be set in d
; **** if STATE then ****
                mov     a,c         ; get state from c
                cpi     1           ; is it equal to one?
                jnz     setbi3      ; if not, turn bit off
; **** BYTE[BYTNUM] ← BYTE[BYTNUM] IOR PINDAT ****
                mov     a,m         ; get current byte
                ora     d           ; set desired bit
                jmp     setbi4      ; write result to memory
; **** BYTE[BYTNUM] ← BYTE[BYTNUM] IAND INOT PINDAT ****
setbi3:         mov     a,d         ; set up byte
                cma
                ana     m           ; turn off bit
setbi4:         mov     m,a         ; write result to memory
                pop     h           ; restore registers
                pop     d
                pop     b
                ret                 ; return to main program
```

Memory Space and Time Estimates

Writing in a high level language before creating machine code allows the programmer to estimate the amount of memory space needed for the end product. Previously, hardware estimation consisted of taking into account the average number of machine code bytes needed by arithmetic, logical, conditional, and other high level instructions. This approach is accurate, but time consuming, for categorizing each instruction in the code. The following methodology lists parameters to estimate needed memory space.

(1) Choose a small subroutine (under a page in size) that is representative of the overall code. Ensure that it contains arithmetic operations, loops, conditionals, and any other forms that appear in the large system.

(2) Hand translate this routine, and tally the number of bytes obtained. (Do not count global variables.)

(3) Count the number of active lines of high level code. An active line is one that generates codes. In PASCAL, "begin" and "end" on lines by themselves are not active. Multiple or separated statements on the same line are considered as multiple active lines. (Active lines are boldfaced in the Implementations in Tables 1 and 2.)

(4) Divide the number of bytes by the number of lines to obtain the average number of bytes/line.

(5) Count the number of active lines in the entire source code to get an estimate of the total number of program bytes by multiplying the number of active lines by the average number of bytes/line.

For systems of 4k bytes or larger, the entire method of memory space estimation has proven to be more than 90% accurate. The average number of generated lines will vary from programmer to programmer; thus, the small sample subroutine is translated by hand to provide a reasonable estimate. For the previous examples, PASCAL and SAIL programs translate into 8080 assembly code on an expansion ratio of about 7 (1 line in SAIL to 7 in 8080 assembly code); FORTRAN translates on an expansion ratio of about 4 (see Table 3).

Execution time estimates can also be made by implementing, in code, software counters into routines that are being timed (along with software counters in all subloops). A reasonably accurate time estimate results from multiplying each count by its estimated number of bytes, and then multiplying the total number of run bytes by the average amount of time to execute one byte

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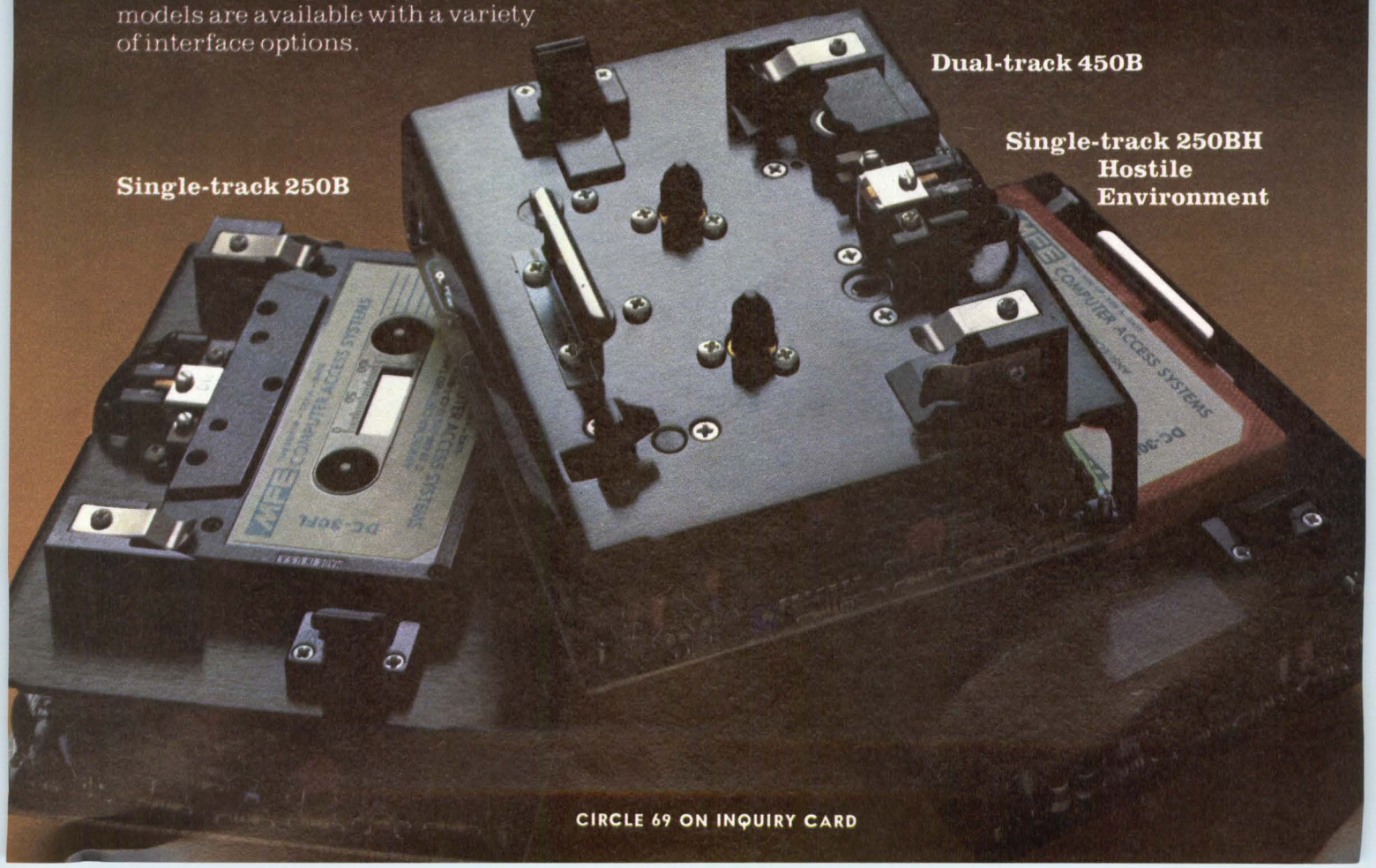

CIRCLE 69 ON INQUIRY CARD

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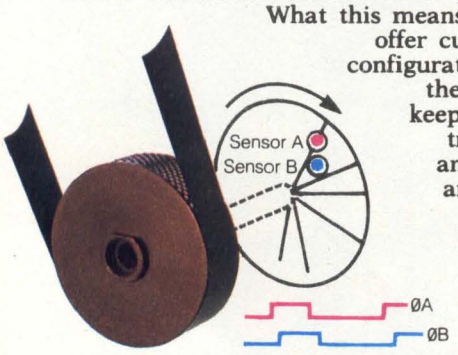

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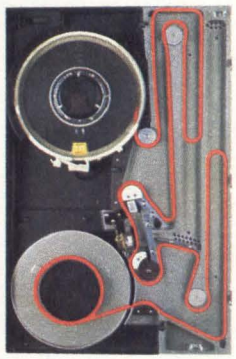

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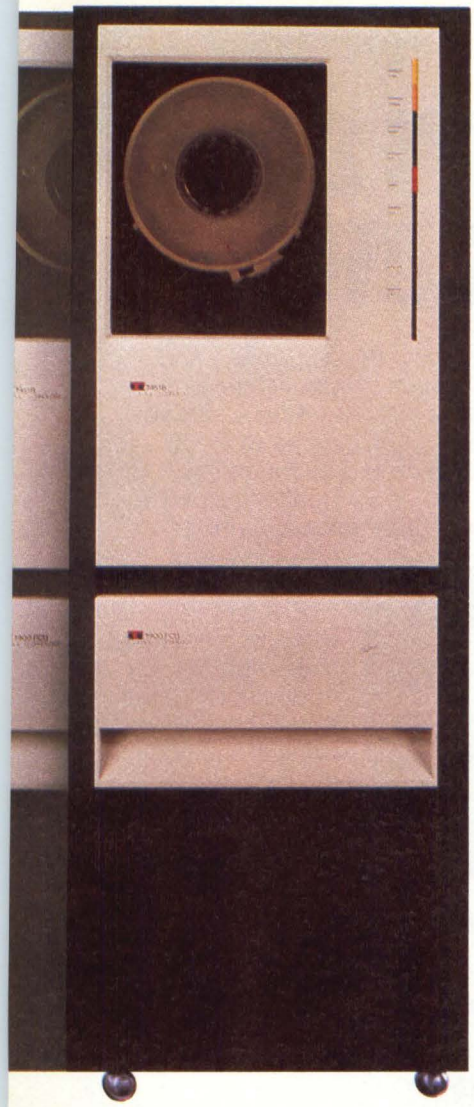

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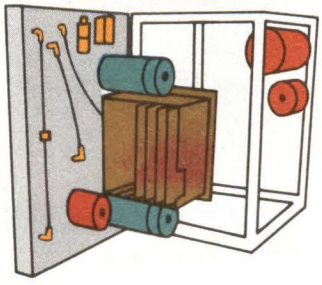

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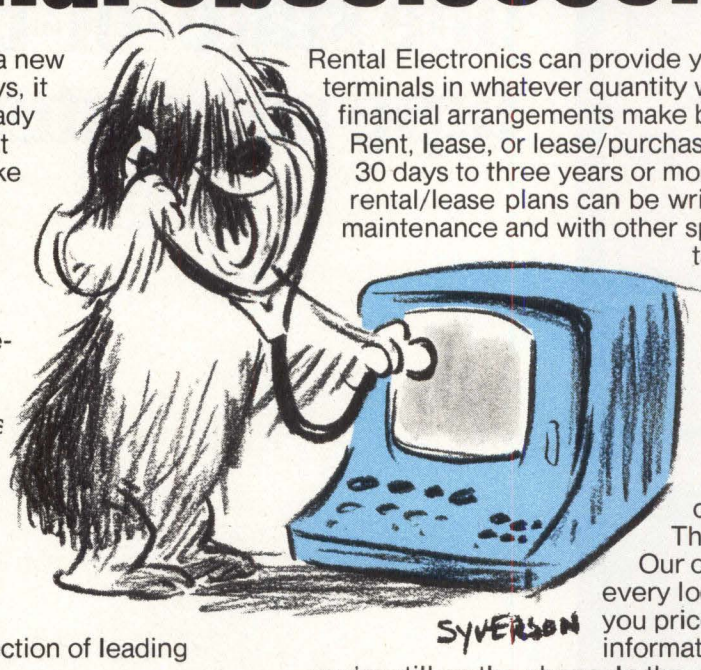

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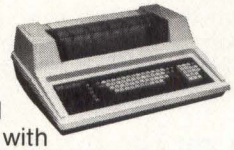

TI Model 820 Keyboard Send-Receive Data Terminal/Printer Printer operates at 150 cps on 9 x 7 wire matrix assembly printhead. Full ASCII Keyboard (ANSI-compatible) with N-key roll over. Operates in Asynchronous, USASCII, RS232C interfaces and is compatible with Bell 103, 113, 202 and 212 units. Selectable baud rates of 110 to 9600.

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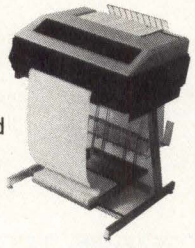

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TABLE 3

Space Estimates

	FORTRAN	PASCAL	SAIL
Active Lines	8	5	7
Space Estimates	(8 x 4) = 32 bytes	(5 x 7) = 35 bytes	(7 x 7) = 49 bytes
Actual Size	29 bytes	29 bytes	49 bytes

on the object machine. This technique allows for relatively easy estimation of memory requirements; it can also be used in selecting the proper microprocessor for a specific application by comparing memory requirements and execution speeds for different microprocessors executing the same algorithm.

Large System Application

Developed at Carnegie-Mellon University, MIDAS serves as an example of a large system implemented with an 8080 microprocessor.[2] This system was written as a generalized instructional tool to allow low cost interactive computer aided instruction. The first version of MIDAS was a digital systems simulator that allowed the student to define logical functions (gates, flipflops, monostables, I/O streams), connect them, and simulate an entire logic circuit interactively.

Since this was an instructional tool, the system had to be self-contained and self-explanatory, and perform error detection, error correction, and prompting. The entire software system for MIDAS was written in SAIL on a Digital Equipment Corp PDP-10 using the methods described. Within a week, a debugged and verified program was running. An estimate of the final size of the program was 559 lines of active code times 7 bytes/line, yielding 3913 bytes of program space. The actual code when finally written was 3596 bytes. The estimate was only 8% high and had allowed for the development of the microprocessor hardware long before the software was written in machine code.

Hand-translated into 8080 assembler, the software was then simulated on the PDP-10 with little subsequent debugging. At this point, the program was first burned into erasable programmable read only memory, and it executed the first time on the 8080 without error. As added capabilities and modifications evolved, they were implemented initially with the high level version, and then were added to the assembly language implementation.

Conclusions

This simple approach of using existing languages and debugging tools for the development of new and unique systems has aided greatly in the writing of several large software systems for microprocessors. It has reduced the turnaround time from inception to actual running code by freeing the programmer from the drudgery of the actual object machine until the last stages of development, while at the same time simplifying that last transition. In addition, reasonable hardware estimates along with memory and speed requirements can be obtained long before final software is completed.

References

1. Intel Corp, *8080 User Manual*, Intel Corp, Santa Clara, Calif, 1976
2. R. Krutz, D. Tuma, and D. Wecker, "A Microprocessor-Based Interactive Learning System," *86th Annual Conference of ASEE*, of British Columbia, Vancouver, British Columbia, Canada, June 19-22, 1978

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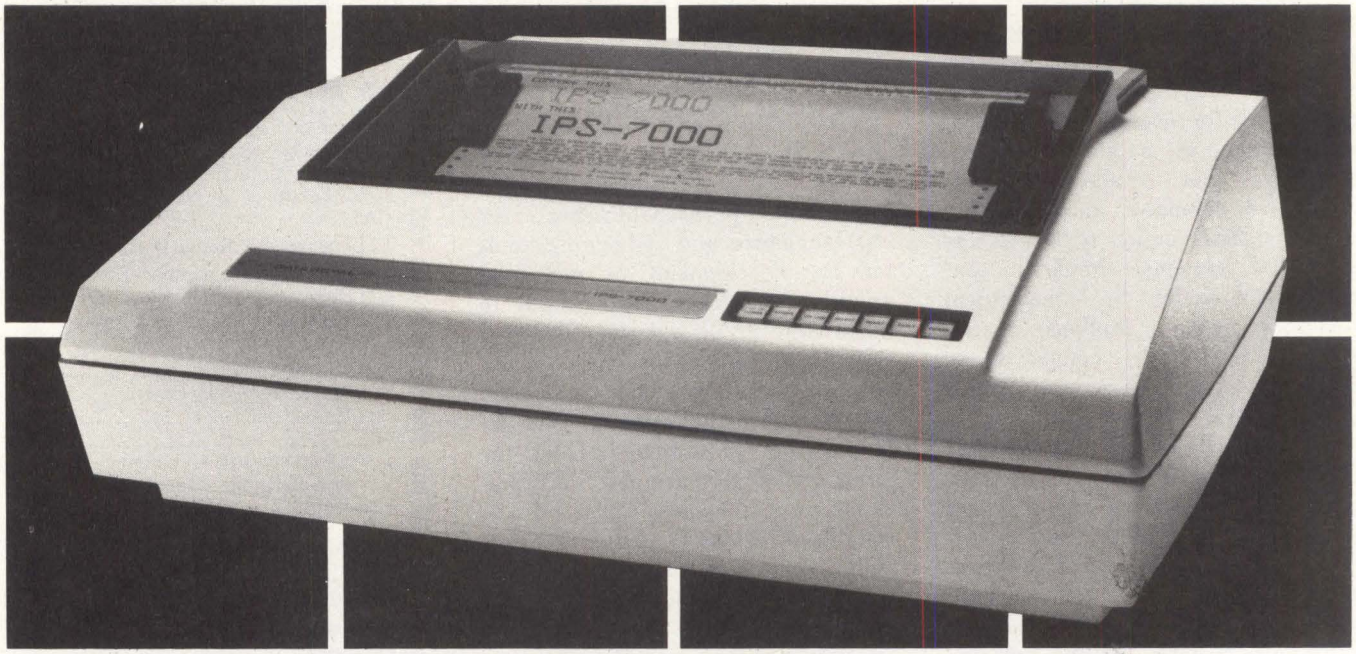

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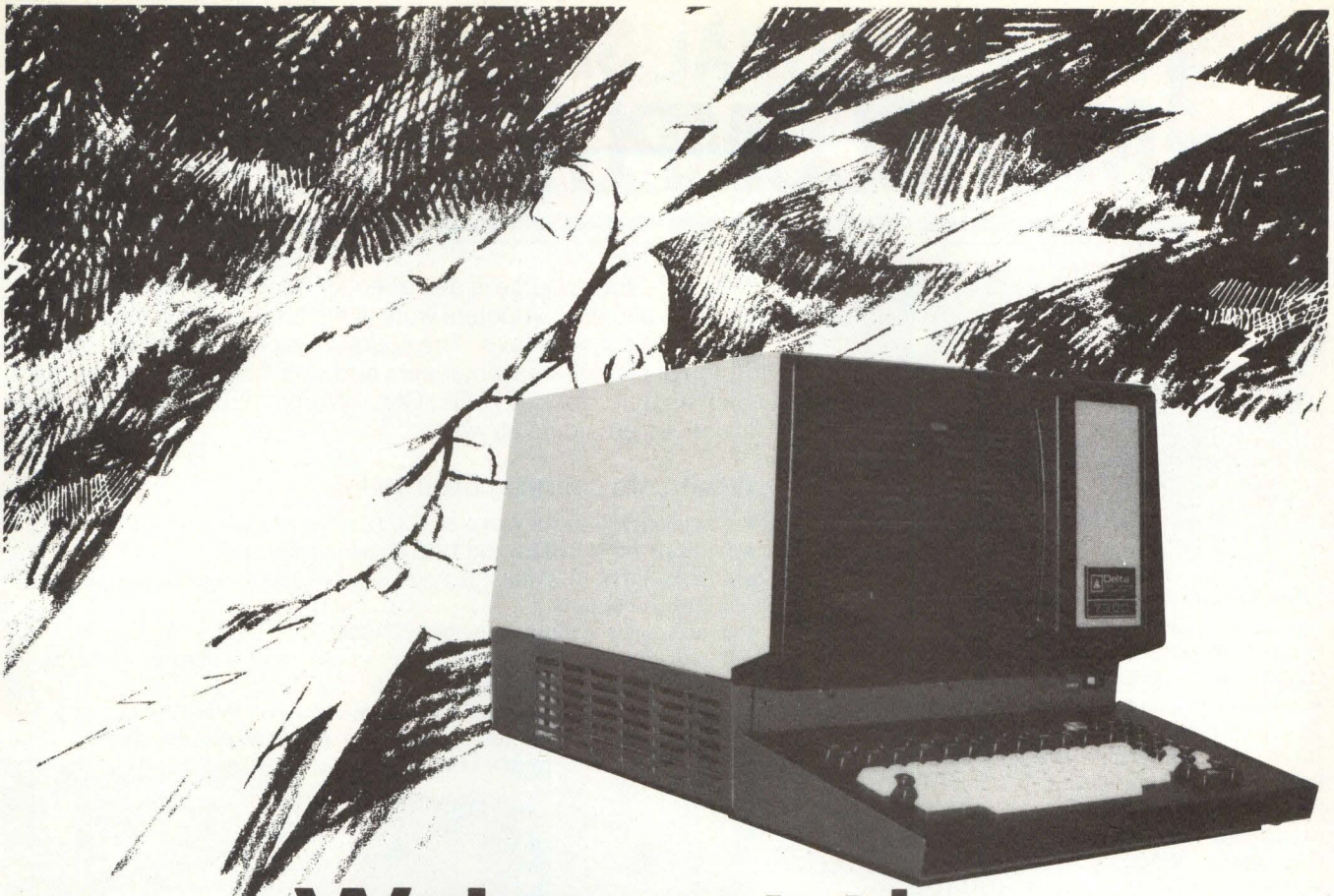

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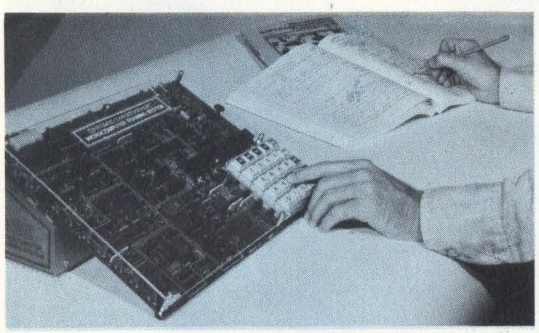

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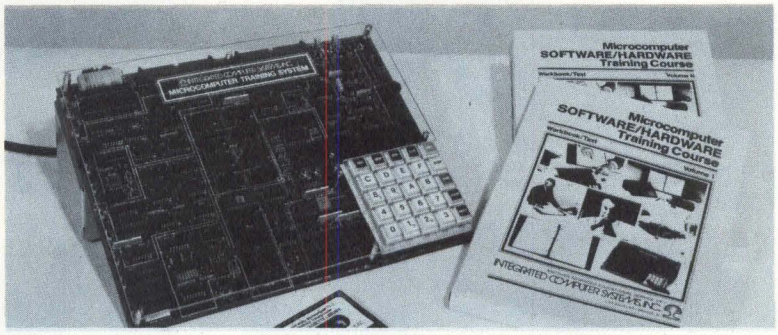

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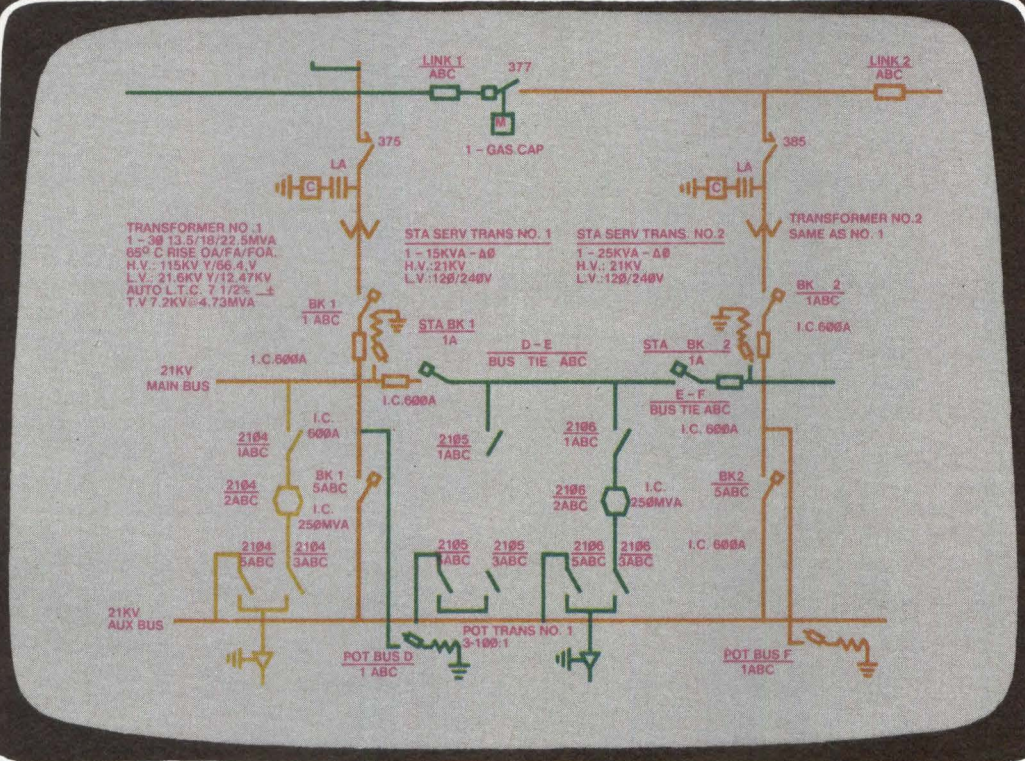

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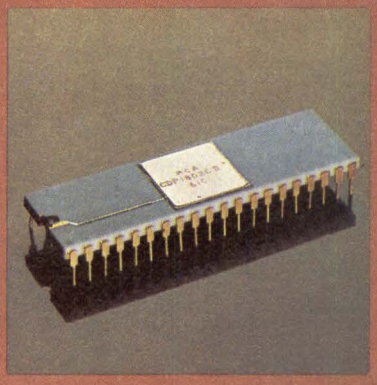

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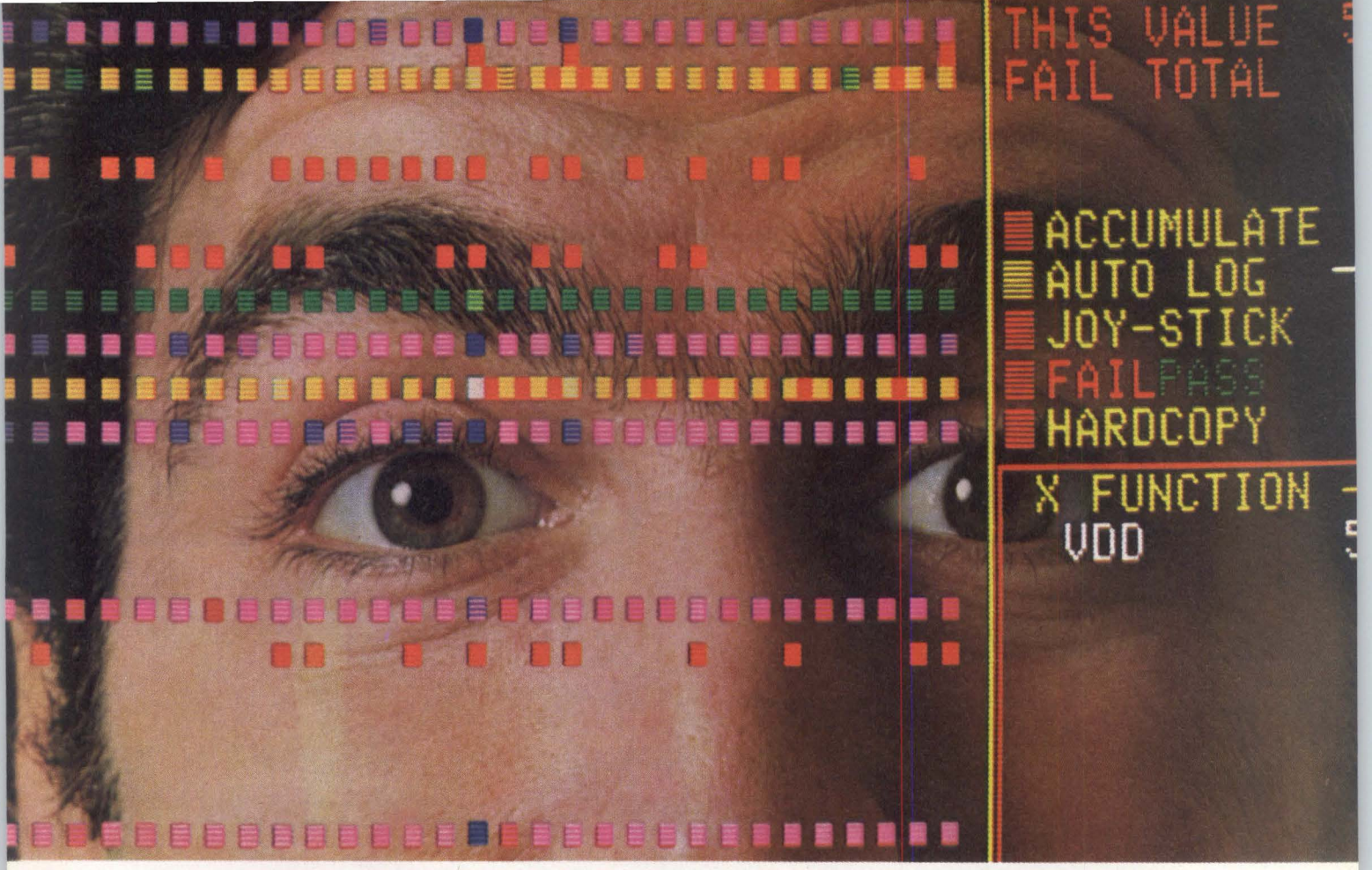

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CIRCLE 142 ON INQUIRY CARD

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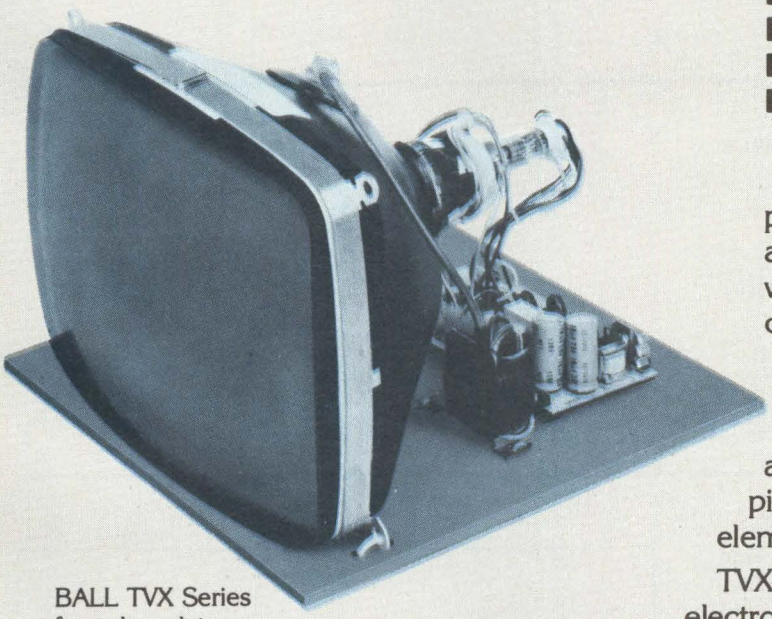

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CIRCLE 77 ON INQUIRY CARD

INTERFACING FUNDAMENTALS: HARDWARE ENCODED AND SCANNED KEYBOARDS

Jonathan A. Titus and Christopher A. Titus
Tychon, Inc

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute and State University

General purpose devices for entering information into a microcomputer include keyboards, thumbwheel switches, analog to digital converters, thermostatic switches, and pressure switches. Of all the input devices, keyboards are probably the most widely used, simply because they are the most general purpose.

Two basic types of keyboards used with microcomputers are hardware encoded and scanned. A hardware encoded keyboard, regardless of the type of keys (metallic contact, Hall effect, capacitive), produces a unique code—ASCII, EBCDIC, binary, or BCD—for each key. The encoder section of the keyboard also produces some sort of strobe pulse, or logic level change, to indicate that a key is pressed.

Owing to recent advances in IC technology, the encoding logic may not only produce a unique key code, but also transmit the code as an asynchronous serial character. Some ICs that are used to encode individual key closures include the AY-5-3600 (General Instrument Corp), the MM74C922 and MM74C923 (National Semiconductor Corp), and the 8279 (Intel Corp). A typical hardware encoded keyboard interface is shown in Fig 1. Because the hardware in the keyboard already encodes the key closures, the software required to sense a key closure and input a key code is very simple (Subroutine 1).

The first instruction in Subroutine 1 inputs the strobe line, or flag, of the keyboard into the 8080 micropro-

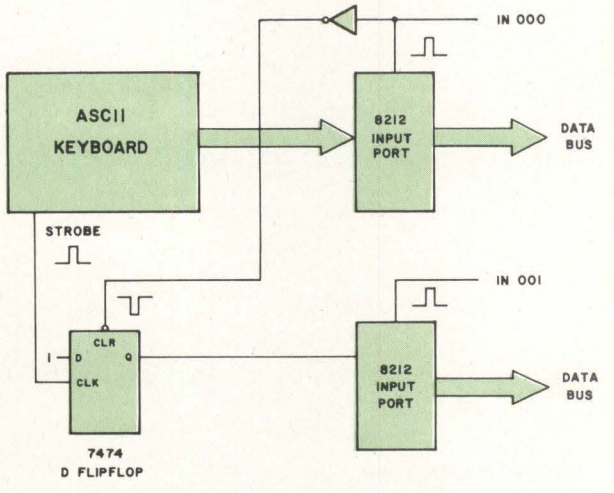

Fig 1 Hardware encoded keyboard. Simple interface uses keyboard that produces ASCII code for each key when it is pressed

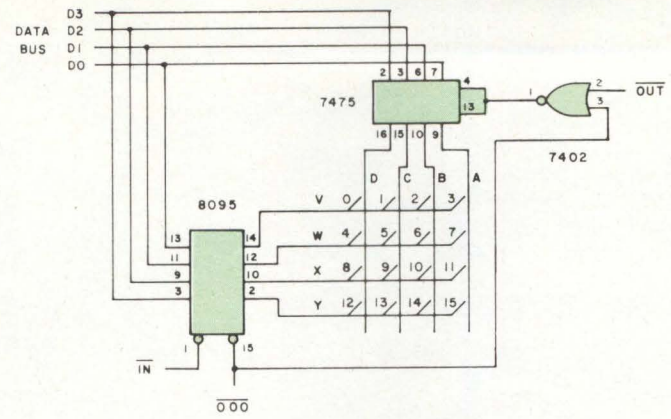

Fig 2 Scanned keyboard interface. Using software, microcomputer scans 4 x 4 matrix keyboard and generates code for each key

cessor's A register. If the flag is a logic 0, no key in the keyboard is pressed. If the flag is a logic 1, a key is pressed. The ANI instruction sets all bits in register A to a logic 0 with the exception of bit D0, which represents the state of the keyboard's flag. If the flag is a logic 0 (no key is pressed), register A will contain zero as a result of the ANI instruction and the JZ (jump on zero) instruction to KEYIN will be executed. When a key is pressed, bit D0 of register A will be a logic 1 after the first IN instruction is executed. As a result of the ANI instruction, the JZ to KEYIN will no longer be executed. Instead, the second IN instruction will be executed, causing the code for the key that is pressed to be read into register A. This instruction also causes the keyboard's flag to be cleared. The keyboard flag must be cleared before the 8080 calls the KEYIN subroutine again, so that the microprocessor does not sense that the same key is pressed. Remember, the key has been pressed only once. After the key code is input, the second ANI instruction sets the parity bit (D7) of the code to a logic 0. This means that programs which call KEYIN can be used with keyboards that generate odd parity, even parity, or no parity.

Scanned keyboards, typically used in calculators, microwave ovens, single-board microcomputers, and low cost microcomputer based games, require very little interface hardware but a large amount of software. The interface for a 16-key keyboard, arranged as four columns of four keys, is shown in Fig 2. The software that causes the microprocessor to scan the keyboard and generate a unique code for each key is listed in Subroutine 2. This software has to perform many of the functions previously handled by the hardware encoding logic. For instance, the software must sense a key closure, debounce the key closure, determine which key is pressed, generate a unique key code for that key, wait for the key to be released, and debounce the key opening.

SUBROUTINE 1

ASCII Keyboard Input

```
/THIS SUBROUTINE SENSES A KEY CLOSURE ON AN
/ASCII KEYBOARD AND THEN INPUTS 8-BIT
/PARALLEL ASCII KEY CODE.

KEYIN, IN     /INPUT DATA WORD THAT CONTAINS
       001    /STATUS BIT FOR ASCII KEYBOARD
       ANI    /SAVE ONLY STATUS BIT FOR
       001    /KEYBOARD
       JZ     /JUMP BACK TO KEYIN IF STATUS BIT
       KEYIN  /IS ZERO, BECAUSE NO KEY IS PRESSED
       0
       IN     /KEY IS PRESSED, SO INPUT
       000    /ASCII CODE INTO A
       ANI    /SET PARITY BIT TO
       177    /LOGIC 0
       RET    /AND THEN RETURN TO CALLING PROGRAM
```

SUBROUTINE 2

Scan of 16-Key Keyboard

```
/THIS SUBROUTINE SCANS A MATRIX KEYBOARD
/THAT IS ARRANGED AS FOUR ROWS OF FOUR KEYS—
/A 4 X 4 KEY MATRIX. IN ADDITION, INSTRUCTIONS
/HAVE BEEN ADDED TO THE SUBROUTINE TO DEBOUNCE
/THE KEYS.
KEYSCN,  MVID    /LOAD D WITH CODE FOR
         003     /FIRST KEY THAT CAN BE SENSED
         MVIB    /LOAD B WITH WORD THAT IS USED TO
         376     /ACTIVATE ONE ROW OF KEYS AT A TIME
NXTGRP,  MOVAB   /GET TEST WORD
         OUT     /AND OUTPUT IT TO KEYBOARD
         003
         RLC     /ROTATE TEST WORD LEFT ONE BIT
         MOVBA   /AND THEN SAVE IT IN B
         IN      /INPUT DATA FROM FOUR
         000     /ROWS OF KEYS
         ANI     /SAVE ONLY FOUR LSBS, WHICH
         017     /CONTAIN ROW DATA
         CPI     /SEE IF ANY KEYS ARE PRESSED BY
         017     /COMPARING 017 (0F) TO INPUT WORD
         JNZ     /KEY IS PRESSED IN THIS ROW, SO
         NXTKEY  /DETERMINE WHICH KEY IT IS
         0
         DCRD    /NO KEYS ARE PRESSED IN TESTED ROW
         MOVAD   /SO DECREMENT KEY CODE BY ONE AND
         CPI     /SEE IF ALL FOUR ROWS HAVE BEEN TESTED
         377     /377—HEX FF
         JNZ     /NOT ALL FOUR ROWS HAVE BEEN TESTED,
         NXTGRP  /SO TEST ANOTHER ROW
         0
         JMP     /ALL ROWS HAVE BEEN TESTED AND
         KEYSCN  /NO KEYS ARE PRESSED, SO KEEP LOOKING
         0
NXTKEY,  CALL    /KEY IS PRESSED, SO EXECUTE
         DELAY   /DELAY SUBROUTINE FOR 10 ms
         0
AGAIN,   RRC     /ROTATE ROW DATA INTO CARRY
         JNC     /FOUND KEY, SO WAIT FOR IT TO
         RELESE  /BE RELEASED BEFORE RETURNING FROM
         0       /SUBROUTINE
         PUSHPSW /OTHERWISE, SAVE PSW ON STACK
         MOVAD   /AND INCREASE KEY CODE IN D BY 4
         ADI
         004
         MOVDA   /SAVE NEW KEY CODE IN D
         POPPSW  /POP PSW OFF OF STACK
         JMP     /AND THEN TRY FOR ZERO CARRY
         AGAIN   /AGAIN
         0
RELESE,  IN      /INPUT DATA WORD AGAIN
         000
         ANI     /SAVE ONLY FOUR DATA BITS THAT
         017     /REPRESENT ROWS OF KEYS
         CPI     /COMPARE THIS VALUE TO VALUE OBTAINED
         017     /WHEN NO KEYS ARE PRESSED (017, HEX 0F)
         JNZ     /JUMP IF KEY IS STILL PRESSED
         RELESE  /AND WAIT FOR IT TO BE RELEASED
         0
DELAY,   PUSHPSW /SAVE PSW ON STACK
         PUSHD   /THEN SAVE REGISTER PAIR D ON STACK
         LXID    /LOAD REGISTER PAIR D WITH COUNT
         101     /OF 003 101 (HEX 0341)
         003
WAIT,    DCXD    /DECREMENT COUNT
         MOVAD   /MOVE MSBY TO A
         ORAE    /OR IT WITH LSBY
         JNZ     /IF RESULT IS NONZERO, JUMP
         WAIT    /TO DCXD INSTRUCTION
         0
         POPD    /WHEN IT IS ZERO, POP D AND E OFF OF STACK
         POPPSW  /AND THEN POP PSW OFF OF STACK
         RET     /AND RETURN WITH KEY CODE IN D
```

To detect if a key is pressed, the microprocessor outputs a logic 0 to one column of keys and a logic 1 to the remaining columns. If one of the keys in the column that is being "driven" by logic 0 is pressed, the microprocessor will input a logic 0 and three logic 1s into register A. If no keys in the column being driven by logic 0 are pressed, the microprocessor will input four logic 1s. If this occurs, the microprocessor tests another column of keys with a logic 0.

At the beginning of KEYSCN in Subroutine 2, register D is loaded with 003 (octal), the code for the first key closure that can be detected. The B register is loaded with 11111110 (octal 376, hexadecimal FE), the first test pattern that will be output to the scanned keyboard. The test pattern is then moved to register A, where it is output to the keyboard. The same test pattern is then rotated once to the left, and the result 11111101, is saved in register B. The microprocessor then inputs the row data of the keyboard and sets bits D7 to D4 of register A to zero (ANI 017). If no key in column A is pressed (keys 3, 7, 11, or 15), register A will contain 017. If one of the keys in column A is pressed, the A register will not contain 017. Therefore, JNZ to NXTKEY will be executed if one of the keys in column A is pressed. If no key in this column is pressed, the microprocessor executes the DCRD instruction, causing the content of register D to be decremented from three to two. Since this value is not equal to 377, the microprocessor jumps back to NXTGRP, so that column B of the keyboard can be tested. Register B already contains the test pattern required to test this column of keys.

If a key in column A is pressed, the microprocessor calls the DELAY subroutine at NXTKEY. The microprocessor returns from DELAY in 10 ms—a sufficient period of time to debounce the switch closure. The microprocessor now has to determine which key in column A is pressed. It does this by rotating the previously input word to the right into the carry. If a logic 1 is rotated into the carry, JNC to RELESE is not executed. Instead, the content of register D is increased by four. By jumping back to AGAIN, the microprocessor can rotate another bit of register A into the carry. When a logic 0 is rotated into the carry, the unique code for the pressed key is in the D register, so the microprocessor executes the jump to RELESE. The microprocessor now waits for the key to be released, at which time the DELAY subroutine is called again. This causes the key opening to be debounced. The RET instruction at the end of DELAY causes the microprocessor to return to the program that called KEYSCN. When it does, the key code is in register D.

As an example, when the 9 key is pressed, the microprocessor loads the D register with 003 (octal) and the B register with 11111110. The content of register B is output to the keyboard and then rotated to 11111101. The row data from the keyboard are input, but since no key in column A is pressed, the A register contains 017 after the ANI instruction is executed. Therefore, the content of register D is decremented from three to two, and the microprocessor jumps back to NXTGRP so that column B can be tested. When the microprocessor executes the instruction at NXTGRP this time, a 11111101 is output to the keyboard, but since no keys in the B column are pressed, the microprocessor inputs a 017. Because of this, the content of register D is decremented from two to one, and since this value is not equal to 377, the microprocessor jumps back to NXTGRP.

The microprocessor now tests column C by latching out a 11111011 to the keyboard interface. Since a key in column C is pressed (the 9 key), register A will contain 11111011 when the IN 000 instruction is executed. The ANI 017 instruction sets bits D7 through D4 to zero, so register A contains 00001011. Since this value is not equal to 017, the microprocessor executes the jump to NXTKEY. The DELAY subroutine is then called, so that the key closure is debounced. Register A still contains 00001011, so a logic 1 is rotated into the carry when the RRC instruction is executed the first time. This means that the JNC to RELESE is not executed. Instead, four is added to the content of the D register (one), and the result (five) is saved in that register. By jumping back to AGAIN, the microprocessor rotates the 00000101 once to the right, and a logic 1 is again rotated into the carry. As before, the JNC to RELESE is not executed, so four is added to the content of the D register (five) and the result (octal 011, decimal 9) is saved in the D register. When the microprocessor jumps to AGAIN this time, the 00000010 in register A is rotated to 00000001, and a logic 0 is rotated into the carry. This means that the JNC to RELESE is executed. Once the 9 key is released, the DELAY instructions are executed, and the microprocessor returns from the subroutine with the code for the 9 key (octal 011, decimal 9) in the D register.

Surprisingly enough, no additional software instructions have to be added to Subroutine 2 in order for the microprocessor to scan and encode a 64-key keyboard. In fact, only four immediate data bytes have to be changed. However, the interface would have to consist of an 8-bit output port to output a test pattern for eight columns of keys) and an 8-bit input port (because each column has eight keys). This means that the keyboard consists of eight columns, each containing eight keys. Note that the software in Subroutine 2 does not produce ASCII values for the key closures. However, this could be done simply by using a lookup table that contains 64 entries.

Key closures can be encoded by either hardware or software methods. A number of IC manufacturers have keyboard encoder ICs available for easy use with a minimum of software. However, they may be too expensive or not flexible enough for a specific need. By using a scanned keyboard, the interface electronics are kept to a minimum; however, a long and complex subroutine must be used to debounce and encode the key closures. This subroutine consists of 38 instructions and requires 67 memory locations for storage. If a lookup table is used to convert the key codes to ASCII values, an additional 72 memory locations will be required to store the lookup table and some additional assembly language instructions.

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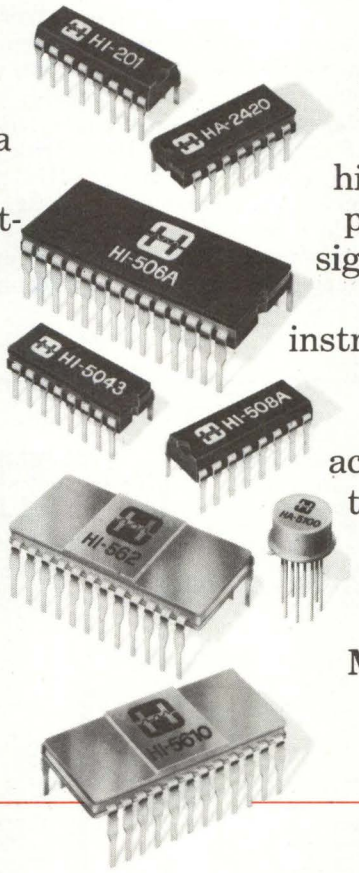

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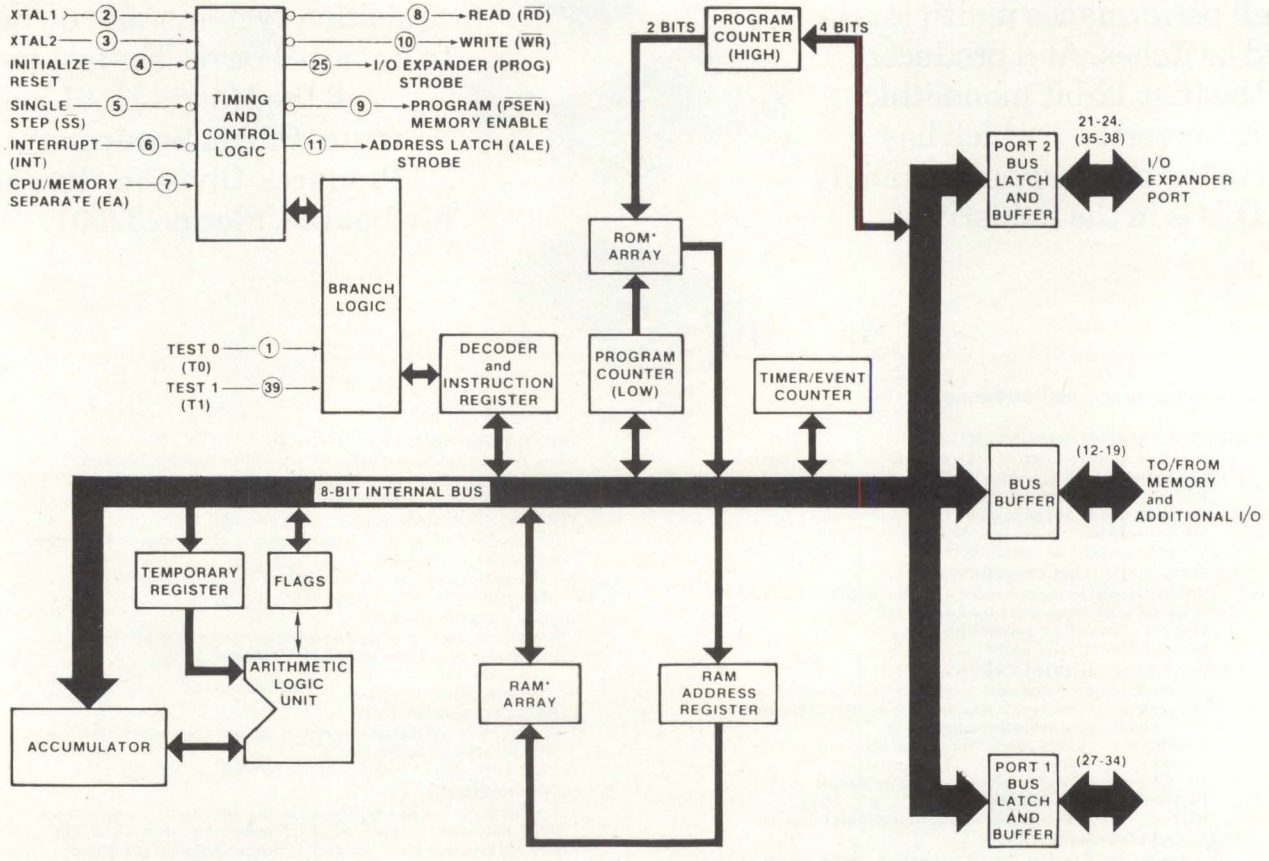
CIRCLE 78 ON INQUIRY CARD

Advanced Process Used For High Density Single-Chip 8-Bit Microcomputers Reduces Size and Lowers Power

Advanced XMOS processing, used to develop an enhanced version of the industry standard INS8048 family of single-chip 8-bit microcomputers results in devices which are 15 to 20% smaller in chip size, consume 20 to 25% less power in full operation, and 12 to 35 times less power in standby mode. Standby voltage is only 2.2 V, less than half that required for present NMOS 8048 devices.

The family initially will include six single-chip microcomputers, all fully programmable systems that perform I/O control and processing tasks at rates up to 400k operations/s. Common features of the systems in pin compatible 40-pin packages are an 8-bit general purpose CPU with internally expandable register and stack array, 96 instructions, and a 2.5-μs cycle time for the 6-MHz part and 1.36 μs for the 11-MHz part, three programmable I/O ports and eight other control and timing lines, programmable interval/timer/event counter, priority interrupt controls, system clock generator, and full set of generally required systems control and utilities. The CPU can operate as a byte processor (8-bit parallel binary), 4-bit binary, or BCD arithmetic processor. Program and data memories are independently addressable and expandable.

INS8048 operates as a standalone single-chip system with programs stored in 1k bytes (8k bits) of masked ROM on the chip and 64 bytes of data RAM, while INS8049 has 2k bytes of masked ROM and 128 bytes

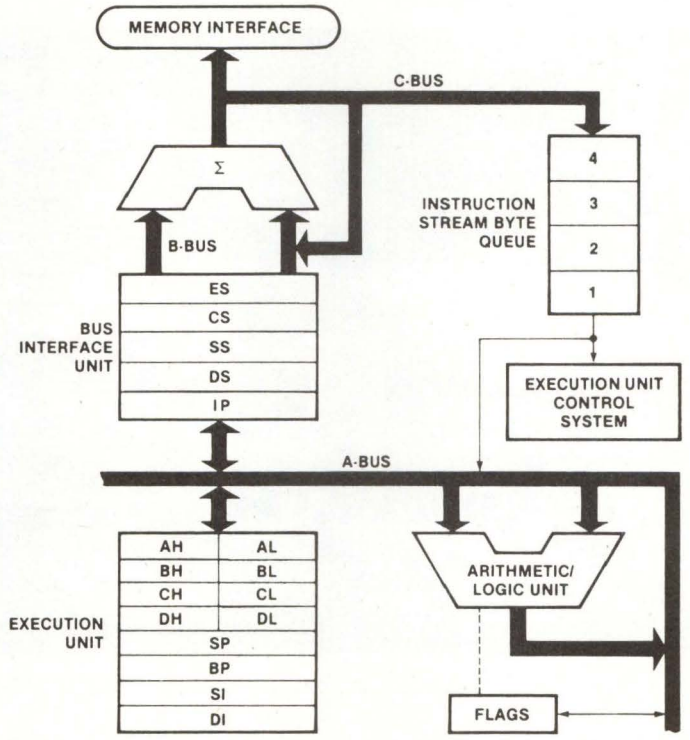


Higher density and smaller chip size of National Semiconductor's 40-pin INS8048 family is achieved with XMOS processing. Standby voltage is lowered to 2.2 V; ROM and RAM capacities vary for individual microcomputers. Increased capacities of 8-bit single-chip devices allow designers to upgrade system features with addition of more memory as well as processing and control functions

of RAM onchip. Centerpiece of the family is the proprietary high density INS8050 with 4k bytes of masked ROM and 256 bytes of RAM on the same chip with the CPU—twice the capacity of any similar single-chip microcomputer, according to National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. With this device, designers can upgrade system features without making artwork changes to the system or relocating software presently generated for the 8048/49 design. INS8038, 8039, and 8040 are ROMless versions of the three previously mentioned devices.

The family is designed as direct pin-for-pin and function-for-function replacements of similar devices in Intel's MCS-48 family. User transparent improvements have been incorporated onchip. Standby current for the INS8049's RAM is programmable, depending on the amount of data memory required: 3, 5, 7, or 9 mA for 32, 64, 96, or 128 words, respectively; three mask programmable options of the chip are transistor drive of 1.5 mA at 1.5 V, TTL drive of 125 μA at 2.4 V, and open collector of 10 μA max. Other onchip features are a battery charging circuit, crystal oscillator capacitors, and Schmitt trigger with hysteresis.

The microcomputers are expandable with the company's family of peripherals and standard memory components via MICROBUS. System support includes the Starplex development system and In-System Emulator (ISE). Organized as four 4-bit programmable ports, the INS8243 I/O expander is a 24-pin device with 16 I/O lines; it attaches to one of the I/O ports of the INS8048/49/50 for expansion of I/O alone. Port 2 serves as the 8243 bus for attachment of the expander. One unit expands four lines of port 2 to four 4-bit programmable ports; additional expanders are added by using an I/O line to select each unit.



Internal functions of Intel's 8088 microprocessor are divided into execution/control unit (EU) and bus interface unit (BIU); they interact directly, but for the most part perform their separate functions independently of each other. Containing data registers and ALU, EU performs basic processing functions. BIU maximizes bus bandwidth utilization, as this is major factor limiting processor speed

Power of 16-Bit Structure Allows 8-Bit µProcessor to Outperform Other CPUs

The 16-bit internal architecture of the 8086 together with the 8-bit bus interface of the 8085A are key design features of the 8088 microprocessor which brings minicomputer levels of CPU performance to 8-bit systems. A major reason that Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, has retained an 8-bit bus structure is to maintain compatibility with existing hardware when designing a new microprocessor system. Another consideration for using an 8-bit wide bus is the savings obtained in drivers, transceivers, and board space.

The 8088 is 100% software compatible with the 8086; upgrading an 8088 system to an 8086 system simply requires hardware conversion. The 8088 features advanced arithmetic and alphanumeric (ASCII) data capabilities so that the programs require fewer instructions and run faster than with other 8-bit machines. The instruction set structure for efficient high level and assembly language programming shortens development times.

The internal structure enables the CPU to process 8- or 16-bit data in single, string, or block form. The CPU automatically fetches and writes 16-bit quantities a byte at a time. Special control lines facilitate operation with multiple processors and shared resources, and interfacing with the company's MASSBUS™ architecture.

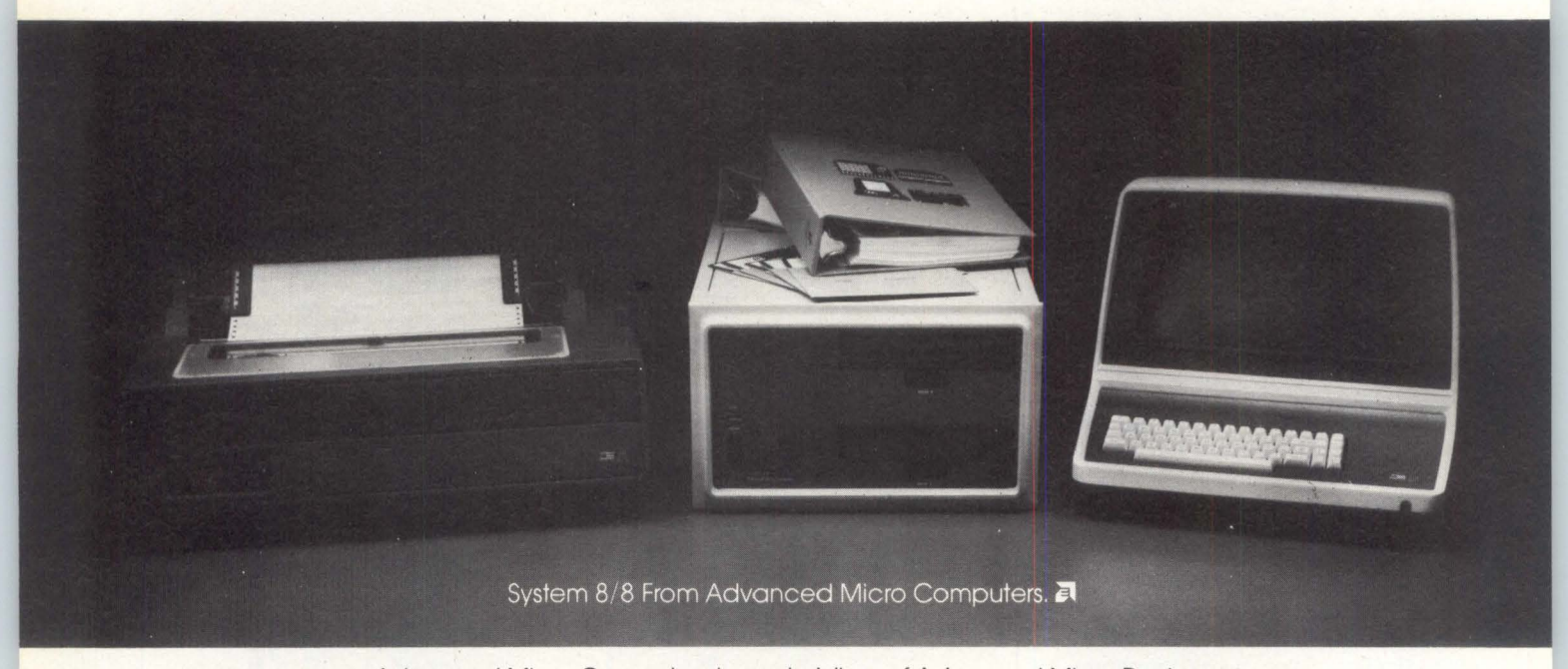
Addressing of 1M bytes of memory is facilitated by the 20-bit addressing feature. Memory is addressed in 64k-byte segments. There are 24 addressing modes; three levels of indexing—base register value, index register value, and displacement—are possible in a single operation. Segmentation allows program code

You've compared the AmZ8000 with the 8086. Now you know what we know. The AmZ8000 is the best 16-bit CPU.

But if you're still a little worried about support. Don't be.

Advanced Micro Devices Announces System 8/8.

System 8/8 was designed especially to support the AmZ8000 in both hardware



System 8/8 From Advanced Micro Computers.

Advanced Micro Computers is a subsidiary of Advanced Micro Devices.

"OK, the AmZ8000 is better. But what about support?"

and software development. But thanks to its multiple-master bus structure, System 8/8 also supports the 8080, 8085 and Z80. It's the only upgradeable, expandable development system you can buy.

The basic machine comes with 32K bytes of RAM, two floppy disk drives, an RS232 serial port, six 8-bit parallel ports and an Am9080A main CPU.

And along with all that powerful hardware, you get an equally powerful set of software.

There's an AmZ8000 translator and macroassembler, a terrific text editor, 8080 macroassemblers, a linking loader and a dynamite debugger. Plus a very sophisticated disk operating system that provides rapid access to programs through a comprehensive file management structure. Its friends call it AMDOS 8/8.

Those are the standard features. Hang on for the options.

System 8/8 speaks four languages fluently: BASIC, FORTRAN, COBOL AND PASCAL. Take your pick. (PASCAL is a new systems implementation language that lets you write more reliable software, lower your development costs and decrease software maintenance.)

We've also got in-circuit emulation, cartridge disks, 8085 and Z80 macroassemblers, CPU boards and a variety of data storage options.

If you want the best 16-bit CPU and the best development system in the business, call or write Advanced Micro Devices.

We've got what you want. No question about it.

Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086 Telephone: (408) 732-2400

Make reservations now for our 4-day seminar on the AmZ8000. Call (408) 732-2400, ext. 2325.

CIRCLE 79 ON INQUIRY CARD

and data to be dynamically relocated by moving the code or data and changing the value of the segment register. Program branches are made relative to the current program counter to provide position independent and relocatable code.

The CPU contains hardware 8- and 16-bit, signed and unsigned, multiply and divide instructions, which use binary, ASCII, or packed decimal numbers. String operations for handling alphanumeric data perform manipulations such as block moves, string comparisons, data scans, and data translations.

The CPU is divided into two processors: a bus interface unit (BIU) that handles I/O data transfers and interfaces with memory, and an execution unit (EU) that includes the ALU, executes the instruction stream from the queue, and manipulates the internal registers. This concurrent operation improves bus efficiency by eliminating much of the bus dead time. At the same time, it permits a memory access time of 460 ns.

Operating at 5 MHz, the microprocessor uses a 4-clock (800-ns) bus cycle. The 8-bit multiplies take 15 μs, and 16-bit multiplies require 26 μs with full 32-bit results.

Comprehensive software runs on the Intellec™ Microcomputer Development System. It includes ASM-86 assembler, PL/M-86 structured high level programming language compiler, and CONV-86 converter program to translate 8080A/8085A assembly code to 8086/8088 assembly code. Other compatible support products include latches, transceivers, memories, and peripherals.

Circle 420 on Inquiry Card

Memory Board Packs 512k Bytes, As Well As Parity And Error Correction

Board level computer memory system provides MOS dynamic RAM storage for 8- or 16-bit CPU systems compatible with iSBC Multibus®, Extended Multibus®, Multiprocessor Operation, and Series II Development Systems. The various memory configurations (memory only, memory with parity, and memory with error correction) and 10 memory sizes from 16k to 512k bytes are implemented with industry standard 16-pin 16k, 32k, or 64k RAMs.

Models with error detection capability employ single-bit parity circuitry; those with error correction capability employ error correction Hamming code circuitry. The latter provides for detection and correction of all single-bit errors and detection of all double-bit errors. This is claimed to provide 85 times better reliability during the first 10k hours of operation.

Two error detection options are available from Mupro, Inc, 424 Oakmead Pkwy, Sunnyvale, CA 94086. The first detects odd numbers of bit errors through the use of an additional parity bit/8-bit memory byte. The second, as part of the single-bit ECC option, also detects, visually indicates with latching error indicator LEDs, and signals the user of all single- and double-bit errors. A fully readable error status register provides row, syndrome, and single/double-bit error status to the host processor.

Five additional ECC bits are employed in the byte oriented boards, and six additional ECC bits are employed in the combinational byte/word oriented boards. ECC bits are transparent to the Multibus.

The board has 330-ns access and 450-ns cycle times. Power-fail recovery capability has protection and control lines to ensure memory integrity. A special backup power bus gives minimum standby power drain. Also included is oncard transparent refresh or external refresh synchronization.

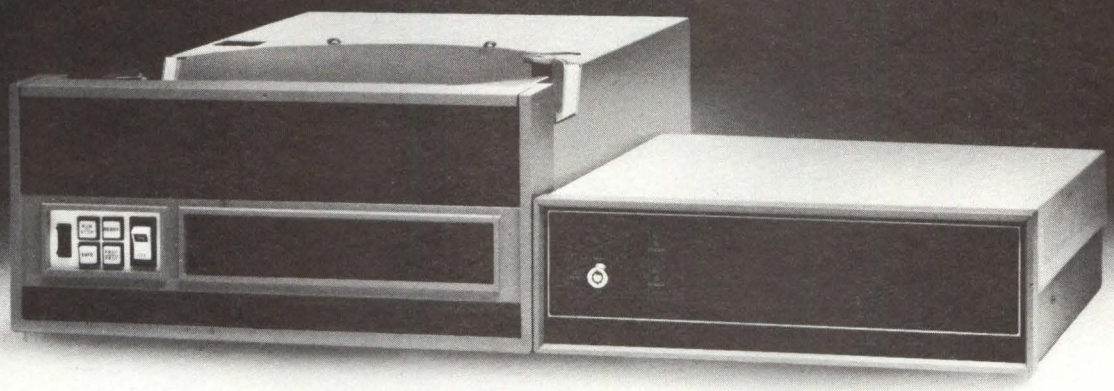
Circle 421 on Inquiry Card

Powerful Low End Single-Chip µComputer Augments Program Storage Capacity

The S2150 single-chip member of the S2000 family of low end microcomputers for high volume appliances, automotive, industrial, and other control applications is in full production by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051. This device improves upon the S2000 (see *Computer Design*, Jan 1978, pp 138, 140), while providing upward software and hardware compatibility.

The microcomputer has 50% more ROM than the previous device (1536 bytes versus 1024 bytes) and 25%

Now, a 10 megabyte hard disk subsystem designed for micros.



And iCOM® has it.

It's here. The iCOM 4511R.

Slide these S-100 components into a standard 19-inch rack and you've got big computer storage capacity for your microsystem: 10 megabytes of useable storage.

The 4511R disk drive incorporates two 5 MB platters. The bottom one's fixed. The top one is removable, for efficient data backup and operating flexibility.

You can change cartridges easily, so the effective storage capacity of the system is limited only by the space on your shelf.

It can handle three more drives, too...boosting total, on-line, random-access memory to 40 megabytes.

And the 4511R is fast. Disks spin at 2400 rpm, and the average access time is only 40 milliseconds.

The bipolar disk controller provides integral power supply and key lock security.

But hardware is only part of the story. The 4511R is available with CP/M,™ a sophisticated operating system which supports Microsoft's FORTRAN, BASIC, and COBOL.

PCC's iCOM Family.

The 4511R hard disk subsystem rounds out PCC's iCOM family. From our compact little 2411 Microfloppy™ to our dual-density, dual flexible disk drive 3812 system, iCOM is the first name to look for in Microperipherals.®

PCC SYSTEMS
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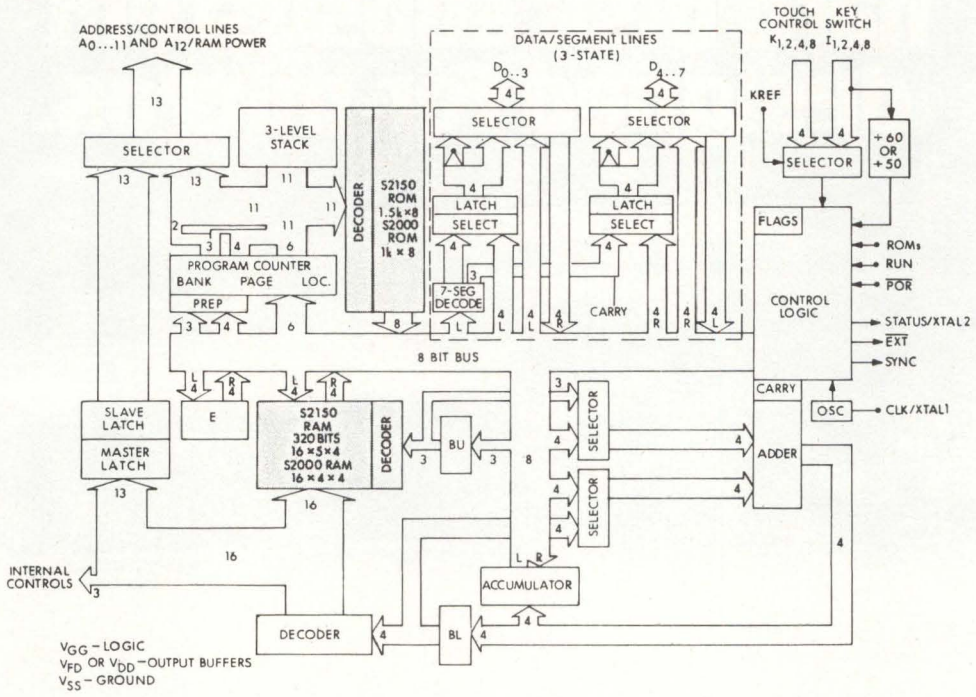
For further information, call this toll-free number: 800-331-1000. (In Oklahoma, call 918-664-8300 collect.)



Produced by American Microsystems, S2150 single-chip microcomputer handles greater program storage of 1536 bytes of ROM and 320 bits of RAM. Shaded and outlined areas in detailed block diagram indicate sections of microcomputer that differ from S2000. Both are software and hardware compatible

more RAM (320 bits compared to 256 bits). Thus, the S2150 can upgrade an existing S2000 application to a more powerful version, while allowing new users to replace electromechanical systems with a microcomputer.

Onchip capabilities are a timer (50- or 60-Hz line compatibility), touch panel keyboard inputs, zero level voltage crossing detection, three subroutine levels, two flags, and direct drivers for an LED display. A crystal controlled clock is optional. The 40-pin plastic DIP is priced under $3 in 50,000 quantities.

System development support includes the company's floppy disc based Microcomputer Development Center, MDC-140 logic analyzer with P/ROM burner on the console, and the SES-2150 emulator, a pin-for-pin substitute for the microcomputer that allows use of EPROMS to debug a system. Software consists of a text editor, macro assembler, loader, and simulator. **Circle 422 on Inquiry Card**

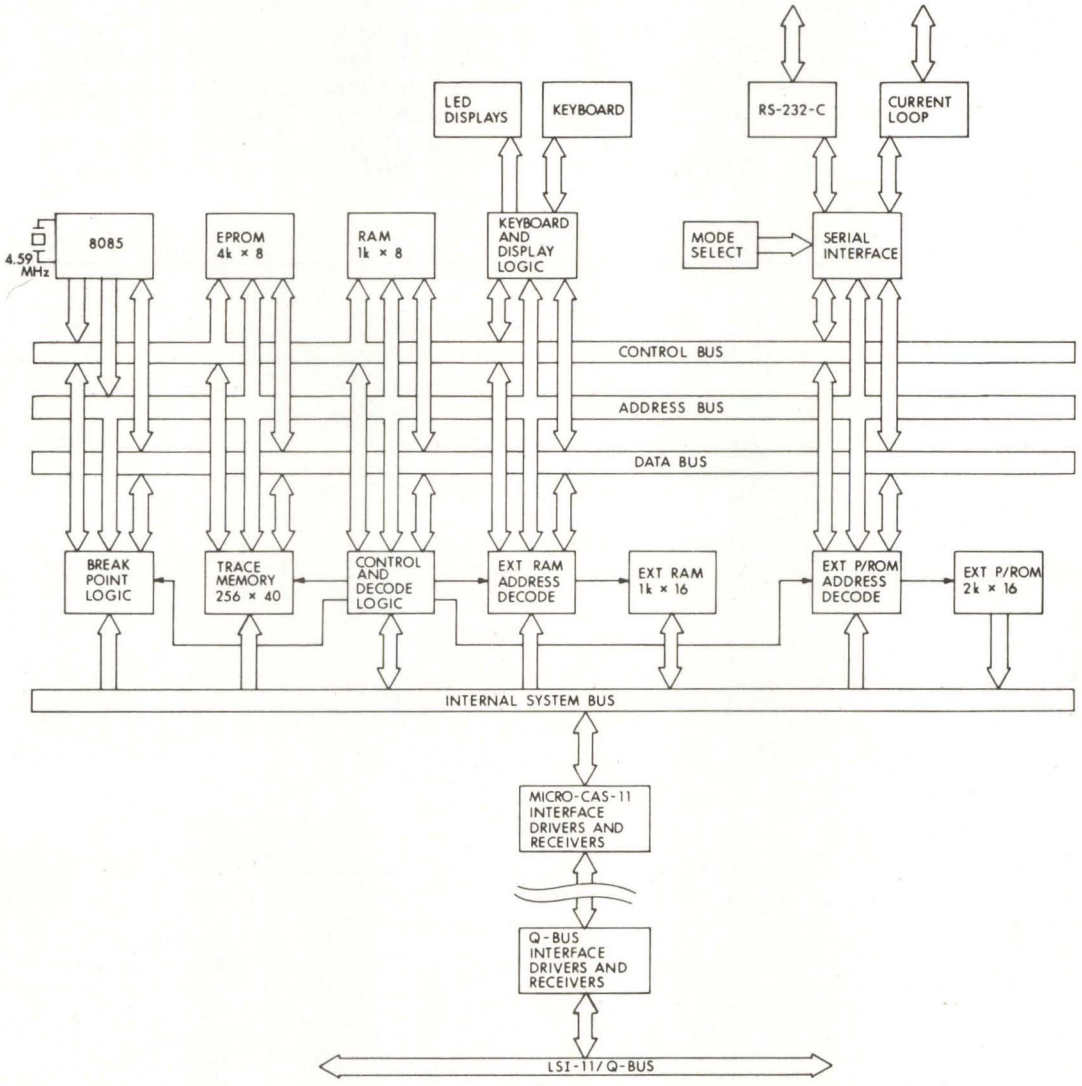
System Console Debugs And Analyzes LSI-11 Software and Hardware

Economical maintenance and troubleshooting of Digital Equipment Corp's LSI-11 and LSI-11/2 computers is possible with microCAS-11. Provided are breakpoint, program trace, examine/alter memory and registers, and single-step program execution for both inhouse development and field diagnostics/debugging.

The microprocessor based unit with memory, keyboard, and LED display replaces a standard DLV-11 serial interface and console device. Self-contained power supply and components represent one device load to the corresponding bus. An integral cable interfaces to the processor under test via the bus connection.

Used in executable program memory, or nonexecutable data or scratchpad areas, the single breakpoint has several actions—program halt, call to extended memory, no action, or display breakpoint word—that the user may designate. Realtime program trace is disabled or enabled by the user. A buffer stores the most recent (256) address, data, and control signal states that occurred during program execution.

The user can examine and modify contents of memory or processor registers while the program is executing (dynamically) or once a program breakpoint occurs. Single in-



Software/hardware analyzer. Packaged in rugged briefcase, Microcomputer Analyzer System-11 from Eldyne replaces standard DLV-11 serial interface and console device. Unit functions as front panel control and display for LSI-11, computer analyzer and debugging tool, and substitute or extended program memory

struction stepping can be done once normal program execution is halted.

Sockets for 2708 or 2716 P/ROMs store up to 2k bytes for diagnostic programs. An internal 1k of RAM handles scratchpad and short programs. An RS-232-C serial interface permits control and display with a terminal.

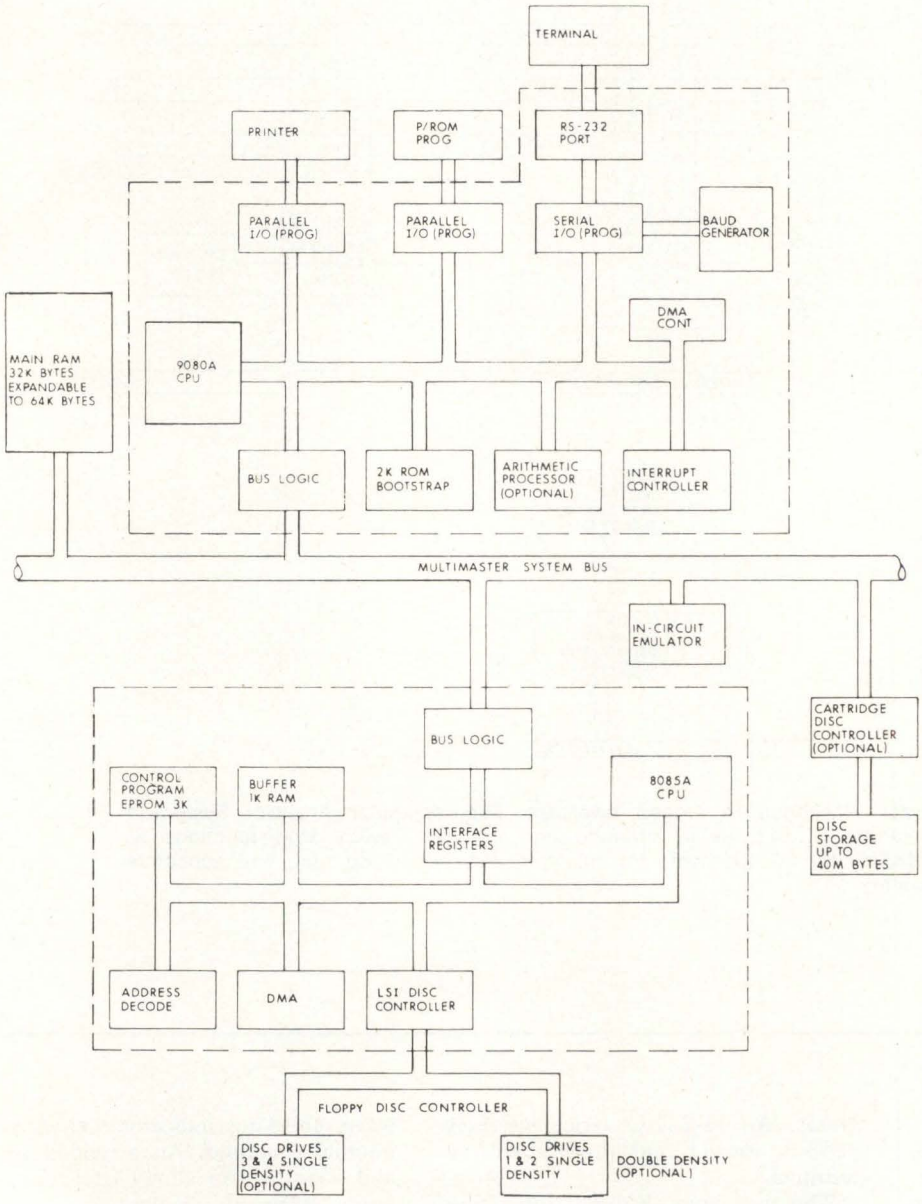
The unit from Eldyne, Inc, 7364 Convoy Ct, San Diego, CA 92111, tests its internal hardware and software, checking indicators, RAM, and internal functions. An extended ROM and RAM feature allows execution of preprogrammed maintenance and troubleshooting programs from the instrument's front panel.

Circle 423 on Inquiry Card

µProcessor Development System Produces 8- and 16-Bit Programs

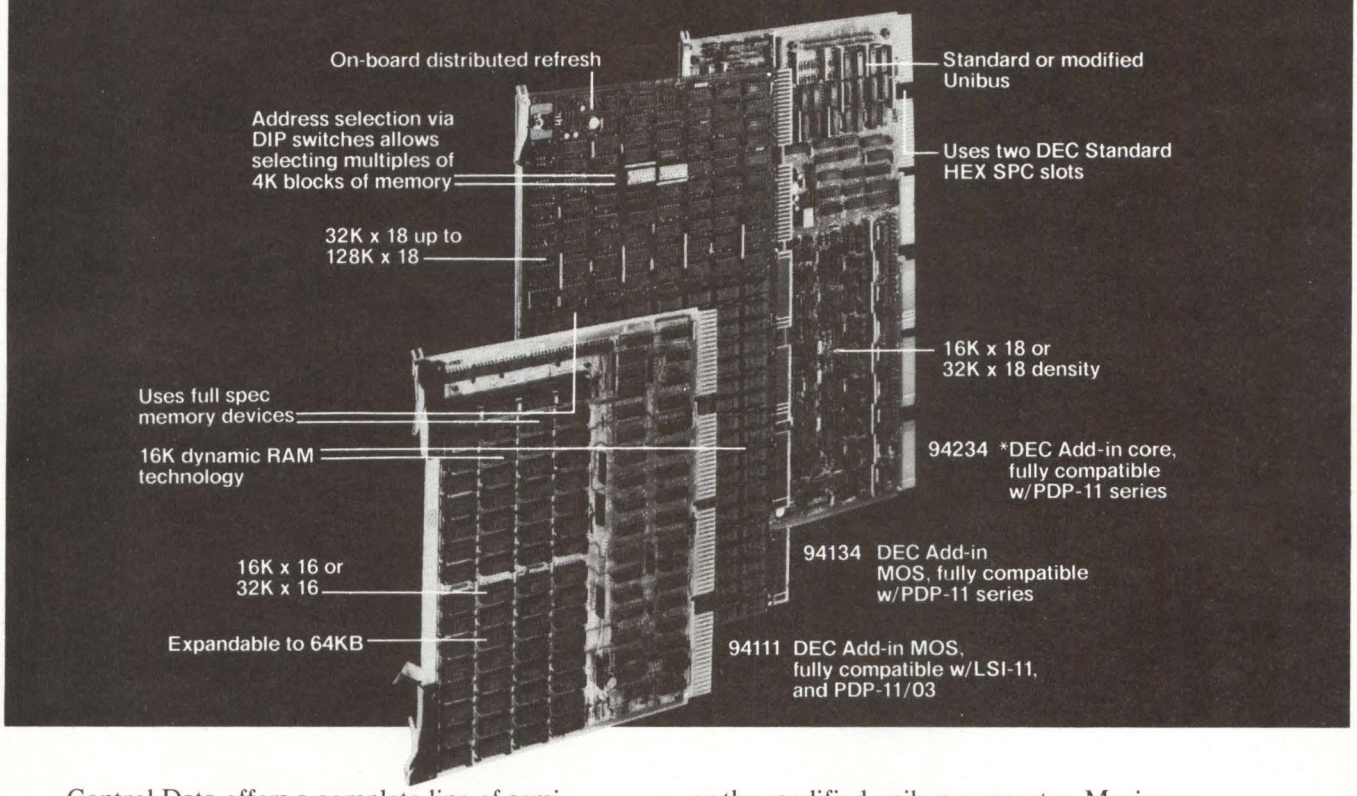
Amsys 8/8 Microcomputer Development System, designed for hardware and software support of the AmZ8000 16-bit microprocessor from Advanced Micro Devices, also provides software support for the 8080, 8085, and Z80 8-bit microprocessors. Contained in a single desktop chassis, the standard system consists of an Am9080A CPU, 32k bytes of RAM, 512k bytes of single-sided floppy disc storage (with controller), one RS-232-C serial port, and six 8-bit parallel ports. All power supplies and cooling are internal to the chassis. Although the CPU is an 8-bit device, the Multimaster system bus design is compatible with the AmZ8000, allowing development of both 8- and 16-bit software programs. The CPU module has DMA capability and can operate in a master/slave environment.

Advanced Micro Computers, 3340 Scott Blvd, Santa Clara, CA 95051, has designed the system for expansion and upgrade capability. The 96/4116 16-bit CPU board, 95/1000 RAM board, and disc drives are some of the boards which can be added. The ports permit communication with optional CRT terminals, 60- to 300-line/min printers, and other peripherals. External I/O boards plug into



Multimaster bus of Advanced Micro Computers' AmSYS8 series of development systems allows upgrading with minimum of change. Addition of 96/4116 Z8000 board upgrades it to AmSYS 8/16 Z8000 system. Basic system features main CPU module with Am9080A microprocessor, 32k-byte RAM module, and floppy disc module

Add-on quality, Add-in quality with OEM memory from Control Data.

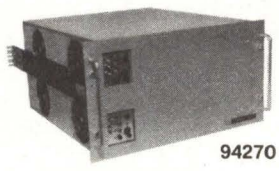


Control Data offers a complete line of semiconductor and core memory that's fully compatible with today's processors. Enclosures, too. And all are built with the same concern for quality that goes into every product we manufacture.

You see, Control Data believes in improving upon basic design when we make memory for mini-computer processors. All chips in our semiconductor memory are "full-goods." So you get all the quality and density you pay for. We use IC sockets instead of hardwiring our chips, so servicing is easier.

When your *PDP-11 needs more memory...

Add-in our 94234 Core Memory Module. It's fully compatible, of course, but you also get the inherent reliability and non-volatility of core memory technology.


94270

Our *Add-on* core is fully compatible too, and fits into your PDP-11/70 rack. It gives you up to 512 Kbytes in a 10½ inch enclosure housing two power supplies, one back plane, one controller circuit board, two to eight memory modules (in pairs), four interconnect cables and four terminator circuit boards.

And when you need better semiconductor memory...

Our 94134 MOS RAM module is fully compatible with your PDP-11/34 and uses either the standard or the modified unibus connector. Maximum configuration is 128K x 18, but smaller densities are also available. Refresh is automatic.

Our 94111 MOS RAM has block address selection via switches for the standard configuration of 16K or 32K x 16. It is pin-to-pin, voltage, signal, hardware and software compatible with *LSI-11 and PDP-11/03 systems.

Put quality behind your nameplate. Call us at 612/830-6018 or send us the coupon below.

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Please tell me more about memory for my _____ processor.

Name _____ Phone _____

Company _____ Title _____

Address _____

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CONTROL DATA CORPORATION

More than a computer company

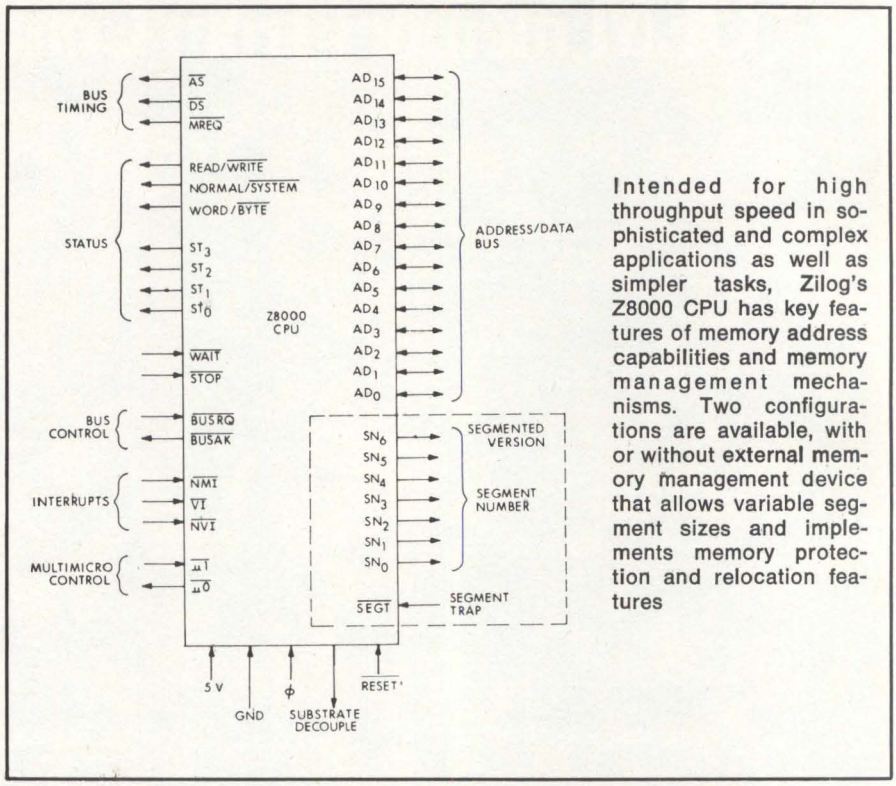
the system's four extra card slots to provide added ports.

Extensive modular software complements the hardware; it may be added as needed. The disc operating system, AMDOS 8/8 accesses programs through a file management structure. It supports a named file structure with dynamic space allocation as well as sequential and random file access.

Several macro assemblers are necessary to handle the various microprocessors. Macro 8/8 assembles relocatable 8080 programs (8085 and Z80 macro assemblers are optional); it also provides CREF 8/8, a cross reference facility, and LIBR 8/8, an object file library manager. Macro 8/8000 supports the full AmZ8000 mnemonic instruction set and permits unlimited macro nesting. The TRANS 8000 program accepts standard 8080/8085/Z80 source code and translates it into standard AmZ8000 source code.

Other system software is EDIT 8/8 line oriented context editor, LINK 8/8 relocatable linkage editor, and DEBUG 8/8 interactive tester and debugger. COBOL, FORTRAN, BASIC, and PASCAL are optional languages to speed 8-bit microprocessor program development. The languages will be announced for the AmZ8000 at a later date.

Circle 424 on Inquiry Card



Intended for high throughput speed in sophisticated and complex applications as well as simpler tasks, Zilog's Z8000 CPU has key features of memory address capabilities and memory management mechanisms. Two configurations are available, with or without external memory management device that allows variable segment sizes and implements memory protection and relocation features

CPU Compresses Mini and Mainframe Capabilities Into Single-Chip Circuit

Two versions of the general purpose Z8000 are designed for both minicomputer and microcomputer applications. Produced by Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, using a scaled NMOS depletion-load silicon-gate technology, the CPU features 24 onchip 16-bit registers that reduce the number of memory references needed in programming. Sixteen of these registers are general purpose. The problem solving instruction set supports 7 data types from single bits to 32-bit words; it has 8 addressing modes and 418 usable opcode combinations.

Other characteristics are resource sharing capabilities for multiprocessor systems, 8M bytes of directly addressable memory, sophisticated interrupt structure, and double-precision signed multiply and divide instructions in hardware for both 16- and 32-bit integers. Claimed to have throughputs that are five to ten times faster than 8-bit microprocessors and two to five times faster than other 16-bit microcomputers and many minicomputers, the CPU uses a moderate 4-MHz clock rate that allows the use of slower memories.

Compilers are supported by multiple stacks, a large address space, and consistent instruction set, as well as by a set of compiler oriented instructions. Operating systems are supported by specific privileged instructions, a sophisticated interrupt and trap structure, system and normal modes, and separate system and normal stack spaces. Translators for PLZ, BASIC, COBOL, and FORTRAN create Z8000 code; an automatic translator performs Z80 code translation.

Z8001 in a 48-pin ceramic DIP allows the user to address up to 8M bytes of memory. Compatible with this version is the 40-pin Z8002, designed for smaller, less memory intensive applications; this CPU's addressing is limited to 64k bytes in each of its six address spaces. Pricing for 1 to 9 pieces is $195 and $150, respectively.

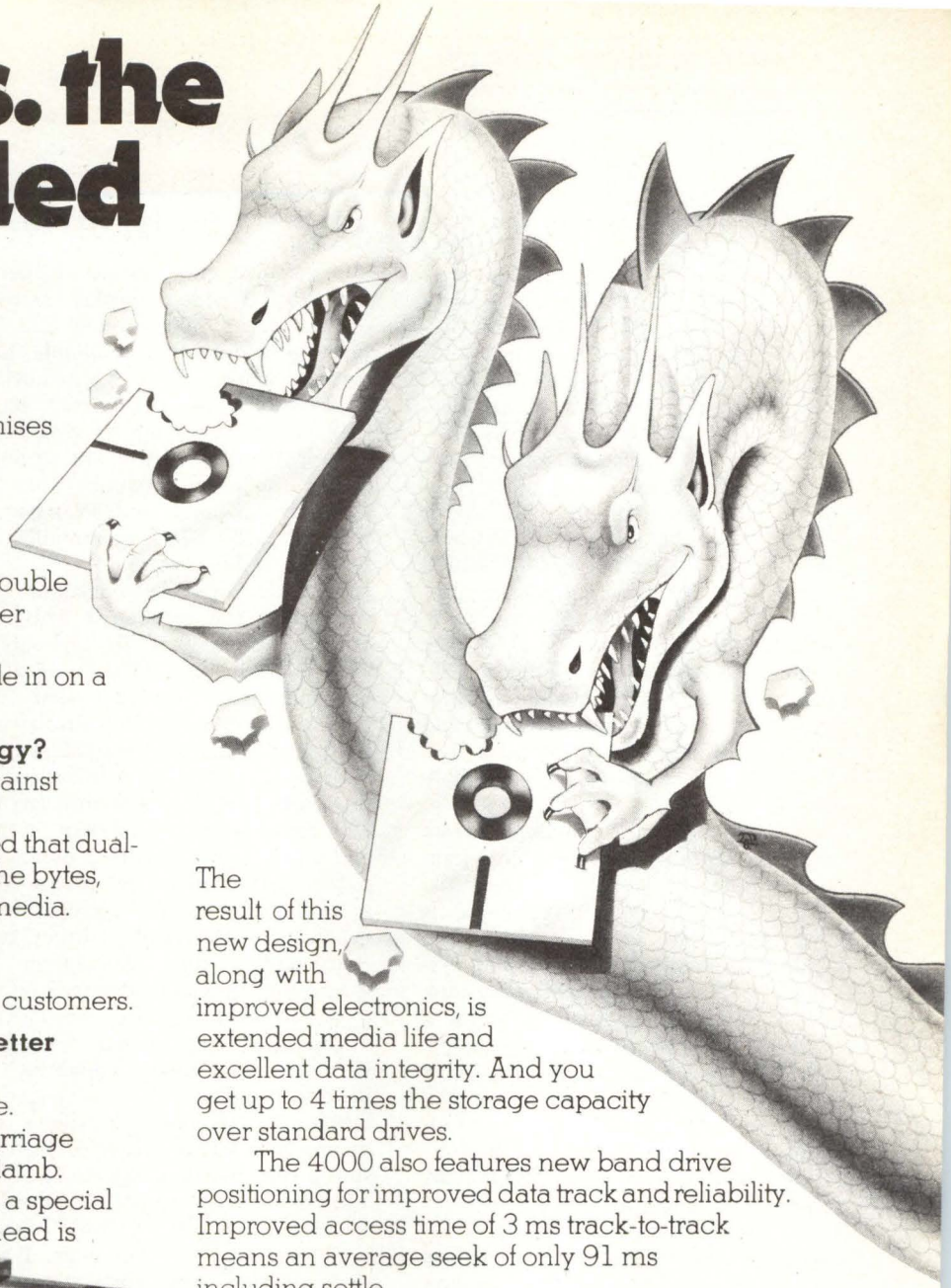
Companion peripheral and memory circuits to be announced to complete the family are the Z-MMU memory management unit, Z-SIO serial I/O circuit, Z-UPC universal peripheral controller, Z-CIO counter and parallel I/O, Z-FIFO first in, first out buffer memory, and self-refreshing 4096 x 8-bit pseudostatic RAM for local storage. All these circuits will be compatible with the CPU's Z-BUS architecture. Advanced Micro Devices, Sunnyvale, Calif, is supporting the entire family (see *Computer Design*, Nov 1978, p 164).

Circle 425 on Inquiry Card

Disc Systems, Computer, and Software Add to Low and Mid-Range Line

Two models of double-sided, double-density flexible disc storage, software for mid-range systems, and a single-board microcomputer extend the DS990 commercial computer family from Texas Instruments, Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001. The family's systems are upward software compatible and,

Remex vs. the two-headed monster.



Were all those dual-head promises just fairy tales?

A lot of people are starting to think so.

They waited. And they waited. And what they finally got for their trouble was trouble — a two-headed monster that ate diskettes.

Until the Remex RFD 4000 rode in on a white horse, that is.

Is it taps for dual-head technology?

Tap, tap, tap went the heads against the diskettes.

In no time at all tap tests showed that dual-head drives not only offered twice the bytes, they took twice the bites out of the media.

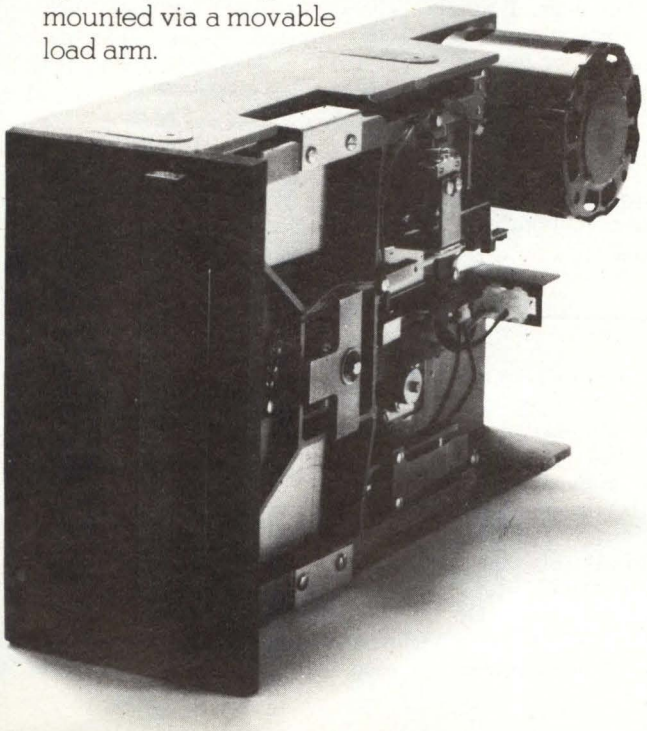
Diskettes just wore out too fast, causing errors.

"Off with their heads," shouted customers.

Rejoice. Two heads really are better than one.

Remex RFD 4000 to the rescue.

Its improved dual head and carriage assembly treat diskettes gentle as a lamb. The ceramic bottom head is fixed in a special lightweight carriage while the top head is mounted via a movable load arm.



The result of this new design, along with improved electronics, is extended media life and excellent data integrity. And you get up to 4 times the storage capacity over standard drives.

The 4000 also features new band drive positioning for improved data track and reliability. Improved access time of 3 ms track-to-track means an average seek of only 91 ms including settle.

Shugart/IBM-compatible

What's more, it's physically and electrically compatible with systems designed to use other popular dual-head drives. And it's backed by one of the strongest companies in the realm.

Ex-Cell-O Corporation, Remex Division, 1733 E. Alton St., P.O. Box C19533, Irvine, CA 92713. Phone: 714/957-0039. TWX: 910/595-1715.

Call us if you're in distress.

Ex-Cell-O Corporation

REMEX DIVISION

Paper isn't the only thing we look good on.

DATA WAREHOUSE T.M.

CIRCLE 83 ON INQUIRY CARD

for the most part, hardware compatible.

DS990 model 1 is a single-user desktop system for low cost data entry and standalone business applications. The main housing holds the TMS9900 16-bit microprocessor, 64k bytes of RAM, two communications ports, a 1920-char video display, and keyboard with cursor control pad, numeric pad, eight programmable keys, and terminal status lights. Two to four 1.15M-byte double-sided, double-density diskette drives in tabletop enclosures provide data storage. Options are a 30-char/s Silent 700™ thermal printer option, display screen graphics, 150-char/s OMNI 800™ model 810 receive-only printer, and modems and auto-call units for synchronous and asynchronous communications to 4800 baud.

System software includes TX BASIC and the Terminal Programming Language (TPL). Running under the TX5 Operating System, TX BASIC is file compatible with the DX10 Operating System on larger DS990 systems. The TX5 Operating System, when purchased separately, includes 990 assembly language support. TPL, which includes a data entry forms generator and a data processing language, runs under the TPL Operating System. Communications software includes IBM 2780/3780, TTY, and TI 742 emulators.

The multi-user system model 2 for small business applications comes in either a desktop or 30″ (76-cm) cabinet. It is based on the newly announced 990/5 microcomputer, a single circuit board containing CPU, memory, and I/O; the computer shares packaging, peripherals, and software with the model 990/4 microcomputer and model 990/10 minicomputer. The disc system features 64k bytes of RAM, two EIA asynchronous ports, and two to four double-sided, double-density diskette drives. Either a model 911 video display terminal or an OMNI 800 model 820 KSR printing terminal is available as a system workstation. An additional workstation, the OMNI 800 model 810 printer, and up to two 9.4M-byte DS10 disc drives are optional. System software includes the 990 assembly language and TX BASIC, as well as 2780/3780 communications software and hardware.

Several software packages that run under the company's DX10 Operating System were also announced. The 3270 Interactive Communications Software (ICS) emulates IBM 3271 control units, IBM 3277 display stations/keyboards, and IBM 3284 printers for remote communications to IBM host computer systems. TIFORM-990 operates with FORTRAN, COBOL, and PASCAL programs to provide simplified man-machine interfaces. Both a prompting display screen forms generator with simple editing functions and a form description language that provides advanced editing of screen input comprise the package.

Query-990 inquiry/report language with a guided-query capability enhances the Data Base Management System (DBMS-990). It allows customers interactive access to the data stored in the data base. The final addition is DX10 BASIC, an advanced ANSI standard (X3.6-1978) business oriented interactive language. Extensions provide conditional statements, subprograms, advanced data file I/O, upper and lower case letters, multiline functions, and assembly subroutines, among others. It also interfaces to optional 2780/3780 communication and supports multi-user program development execution.

Circle 426 on Inquiry Card

Control Computer Focuses On Overall Application, Rather Than Design Details

With the CPU-1, based on a 3-MHz 8085 microprocessor, manufacturers and users are able to concentrate on their overall application, rather than on detailed microcomputer design. The basic system contains 256 bytes of RAM, 22 I/O lines, one serial I/O port, one programmable counter/timer, and an RC clock. An optional crystal handles applications requiring precise timing. The system has power on reset and a manual reset button, and supports the microprocessor's vectored interrupt structure. Sockets hold up to 4k of EPROM (2708, 2758, 2716, or TMS2716).

Manufactured by Pragmatic Designs, Inc, 711 Stierlin Rd, Mountain View, CA 94043, the single-card computer expands to 512 bytes of RAM, 44 I/O lines, and 2 programmable counter/timers to serve larger applications. It can be customized using a PC board area laid out for wire-wrapping or soldering special functions; system I/O and control traces are bused to pads adjoining this area. An onboard power supply with ±5- and 12-V outputs can be accommodated.

Applications programs can be developed using any 8080/8085 development system. A connector and logic are provided with the computer so that it can also utilize the company's DMM-1 debug memory card's hardware trap facility; a trap LED shows the trap latch state during debugging. This feature allows users to develop programs quickly using a larger S-100 computer. Once development is complete, EPROMS can be programmed and installed in the computer for normal system operation.

Circle 427 on Inquiry Card

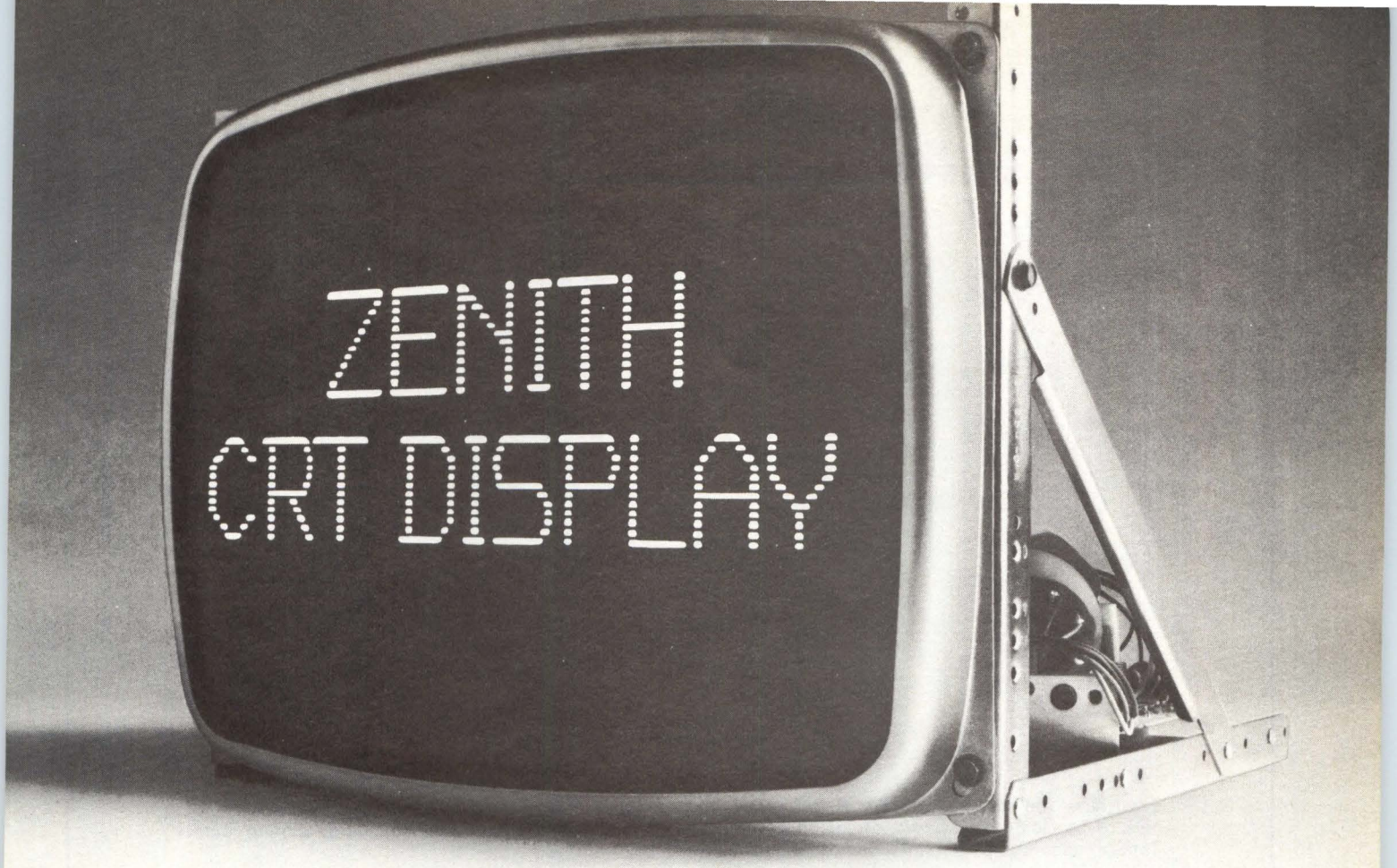
Four Triple-Output Power Supplies Handle Microprocessor Needs

Expanding the RS/RT series of switchers, ACDC Electronics, a div of Emerson Electric Co, 401 Jones Rd, Oceanside, CA 92054, has added models RT153, 154, 303, and 304 that offer isolated auxiliary outputs of 5 and 12 V or 5 and 15 V, in addition to the main 5-V output. RT153 and 154, packaged in 5 x 5.5 x 9.5″ (13 x 13.9 x 24.1-cm) T15 cases, both feature 5 V at 30 A and 5 V at 2 A; the 153 has 12 V at 5 A and the 154 has 15 V at 4 A. Models RT303 and 304 in the standard 5 x 8 x 10″ (13 x 20 x 25-cm) T30 case size both have 5 V at 60 A and 5 V at 5 A; the 303 has 12 V at 5 A while the 304 has 15 V at 4 A.

Circle 428 on Inquiry Card

Terminal's Keyboard Improvements Permit Use of CRT Editor

As a terminal and console to be used with the EXORciser™ I or II,



The read-out is quality.

Quality is what has made Zenith famous for over sixty years and number one in the television industry. It's that quality, that commitment to excellence – that insures the reliability of every product we make.

Our manufacturing facilities, laboratories, equipment, procedures, experience and know-how give you the quality and reliability that you look for in a CRT Display. A CRT Display that will hold up under really tough operating conditions.

And to all this, our people add the personal service and special attention you want from your CRT Display source.

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Our testing insures that every component operates to exacting Zenith standards. Exhaustive computer analysis, electron microscope and thermograph scan tests are only a sample of what we do.

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Every CRT Display we design has our customers in mind. Before our engineers even begin new circuit layouts, we'll meet with you and find out what your exact needs and specifications are.

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Components in the CRT Display are designed with reserve capacity for low maintenance and continued reliability.

The Zenith CRT Display is equipped with a Zenith designed and built deflection transformer. It not only gives a consistent scan, but it is also embedded in epoxy for long-term reliability and the elimination of high frequency squeal.

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The Zenith CRT Display is precision engineered. No linearity controls are required and the CRT Display's vertical and horizontal synchronization is automatic.

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For further information and specifications, write CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call 312-773-0074.

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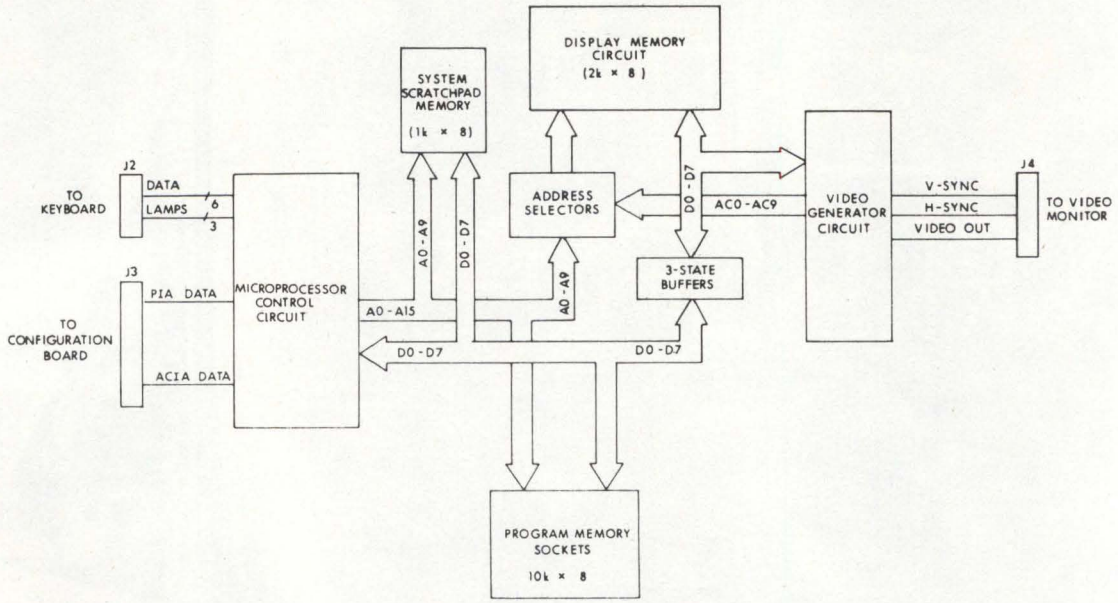
CIRCLE 84 ON INQUIRY CARD



EXORterm 150 for use with EXORciser I and II upgrades Motorola Microsystems' line of display terminals to provide total system. Major improvement over previous model is to keyboard, adding cursor control, tabbing, page, line, and character control keys

EXORterm™ 150 serves primarily as a total system that allows use of the company's CRT editor. The EXORciser display console facilitates data exchange between the user and system via a video interface, keyboard entry, and serial communications link using speeds up to 9600 bits/s.

Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036, has combined an M3000 video monitor, CRT controller board, CRT configuration board for manual selection of basic criteria, chassis/housing with power supply, data entry keyboard, and resident executive firmware to control the display and communications interface. Upgraded from the EXORterm 100, the M6800 based terminal has an improved keyboard with added cursor control, tabbing, page, line, and character control keys.

The system controls display attributes, communication facility, terminal switch/indicator, and keyboard inputs. Microexecutive firmware, together with control and application task firmware, coordinates the system functions in EXORciser oriented activity.

The basic console's unit price (1 to 5 quantities) is $2490. EXORterm 100 users may purchase the improved keyboard assembly and extended display ROM separately for $340 and $200, respectively. The CRT editor is priced at $300 per unit.

Circle 429 on Inquiry Card

Floppy Disc Controller Combines With I/O To Serve As System CPU

Floppy Disk Controller-I combines the controller with the I/O required in a microcomputer system, allowing its configuration as the central processor in an S-100 system or as a smart floppy disc controller. The 5 x 10″ (13 x 25-cm) microprocessor board features a cassette port; parallel port; two serial ports; floppy disc controller; 8k-byte capacity in any combination of EPROM, ROM, or RAM; onboard Intel type 2716 programmer; and Z80A CPU.

CP/M, FAMOS, and OASIS comprise the disc operating systems. Connecting up to three mini (5″, 13-cm) drives or four full-size (8″, 20-cm) floppy drives, the controller reads and writes single- or dual-density diskettes in IBM 3740 or System/34 format. Software that Teletek, 9767F Business Park Dr, Sacramento, CA 95827, has included onboard allows flexibility in developing applications. Among other capabilities, the onboard monitor in EPROM reduces the complexity of disc interfacing to a few user callable routines; patching to other programs is accomplished by a call to the appropriate I/O routine, and a well-defined interrupt structure efficiently uses the onboard I/O in multitasking operations.

Circle 430 on Inquiry Card

Almost perfect.

Our new ADM-42 doesn't have quite everything. But it comes so close, you might never notice.

Because it's a complete, semi-intelligent terminal for just about any application you can name. And it does just what you want it to do, just when you want it done.

The ADM-42 is completely self-contained, and provides you with flexibility of format, security, editing, interface, and transmission. It also features a full two-page display as standard equipment. Not as an option. And it comes with a truly staggering array of options.

THE MORE YOU USE IT, THE SMARTER IT SEEMS.

We gave the ADM-42 a bright, easy-to-read 2000 character display. A full 128 ASCII character set. 16 function keys for 32 separate commands. And five separate cursor control keys.

The 42's behavior modification gives you a factory installed personality for an alternative ESC sequence lead-in—in addition to the standard ESC. And End Block character. A New Line character sequence. A field separator. And even a function sequence preamble.

Its status displays on the screen give you a conveniently wide range of information at a glance. While its special symbols indicate the entry of control characters in memory. Also, all control characters can be stored using the escape sequence or program mode. And the Field Protect Mode allows rapid data entry into forms or instruction pages.

THE ADM-42 WILL HAND YOU ANOTHER LINE.

The terminal's displayed data is formatted in 24 lines per page, 80 characters per line. And, to top it off, it comes with a 25th line established and reserved exclusively for status indicators and messages of up to 79 characters.

As if all this weren't enough, the ADM-42 has an impressive list of options. Like synchronous transmission with various line protocols. An extended memory capable of adding data space up to a maximum of 8 pages. And programmable function keys, to name but a few.

THE ADM-42 IS ONE TOUGH ACT TO FOLLOW.

The ADM-42 has just about everything. Including a microprocessor that increases reliability and ease of operation. Any way you look at it, in fact, it's one pretty smart buy.

So if you're thinking of upgrading to a more intelligent terminal, at a more than reasonable price, call us today. Or better yet, contact your local distributor.

We'll show you how easy it is to move up to the ADM-42.

The terminal that's so smart, you'll swear it's got a mind of its own.

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CIRCLE 145 ON INQUIRY CARD

SOFTWARE

Operating System Uses Existing Software Application Packages

A timesharing operation system for Digital Equipment Corp's PDP- or LSI-11 based systems protects a user's investment in DIBOL (Digital Business Oriented Language) software while providing new users with access to the large base of existing application packages. The Plug Compatible Operating Software (PCOS) is an extension of the DIBEX runtime system. Depending on program mix, up to 20 terminals run on the system without interfacing to several different operating systems.

Initially both DIBOL and DIBEX language processors are offered with other languages scheduled for future release. Extensions to DIBEX are copy/include, if/else, and while statements; also featured are binary field manipulation, virtual memory and optimization techniques, and support of group levels. Information Access Systems, Inc, 1140 Bloomfield Ave, West Caldwell, NJ 07006, also plans to offer the system on other 16-bit computers.

The multiterminal program development feature performs program development while concurrently executing applications from any available terminal. The system supports remote program development (requiring a terminal with hardcopy output and a single-line communication connection to a single-board computer), monitor commands, multiterminal utilities, ISAM utility, and sequential, random, and index sequential file structures. Using a source compare utility, a developer can examine two source files with an option to list the differences. A DIBEX debugging technique steps through a program to locate software problems.

The base system required is 56k bytes of memory, realtime clock, serial line interface, terminal I/O device, and a disc. Prices of the operating system are $2995 for microcomputers and $3745 for minis. A runtime only version is available.

Circle 431 on Inquiry Card

Program Quickly Copies Diskette to Itself With Formatting

Running under Intel's ISIS-II™ operating system, a disc copy program for the Intel MDS™ family of development systems duplicates a single- or double-density diskette in less than 1 min. Optionally, the user may specify formatting or verification of the object disc. The binary copy from Xener Corp, Suite 211, 6641 Backlick Rd, Springfield, VA 22150, is not limited to copying ISIS-II diskettes; it copies any standard format single- or double-density diskette.

The program's major feature is that it allows a diskette to be copied to itself with formatting. This is useful when all data on a diskette have been lost because of a bad CRC on one sector. By copying a diskette to itself, all soft errors are corrected, allowing access to the data again; destroyed data are not replaced, but in the case of soft errors, the diskette is made readable.

Circle 432 on Inquiry Card

Software Automates Creation of Calculator Keystroke Programs

Users familiar with BASIC can create a complex calculator program using the BASIC to TI 58/59 cross compiler (translator) written in BASIC. The user develops, refines, and tests the programs in BASIC. The compiler accepts the resulting BASIC programs as input and automatically translates them to keystroke programs for Texas Instruments' TI 58 and 59 calculators.

The software, priced at $65, runs on a BASIC machine with 16k of RAM. Extended features incorporated by Singular Systems, 810 Stratford, Sidney, OH 45365, are keystroke optimization, complete keystroke program listing geared to printers or video monitors, listing of BASIC variables used and corresponding calculator memory registers, listing of calculator labels used, and recognition of both standard and nonstandard BASIC commands and functions.

Circle 433 on Inquiry Card

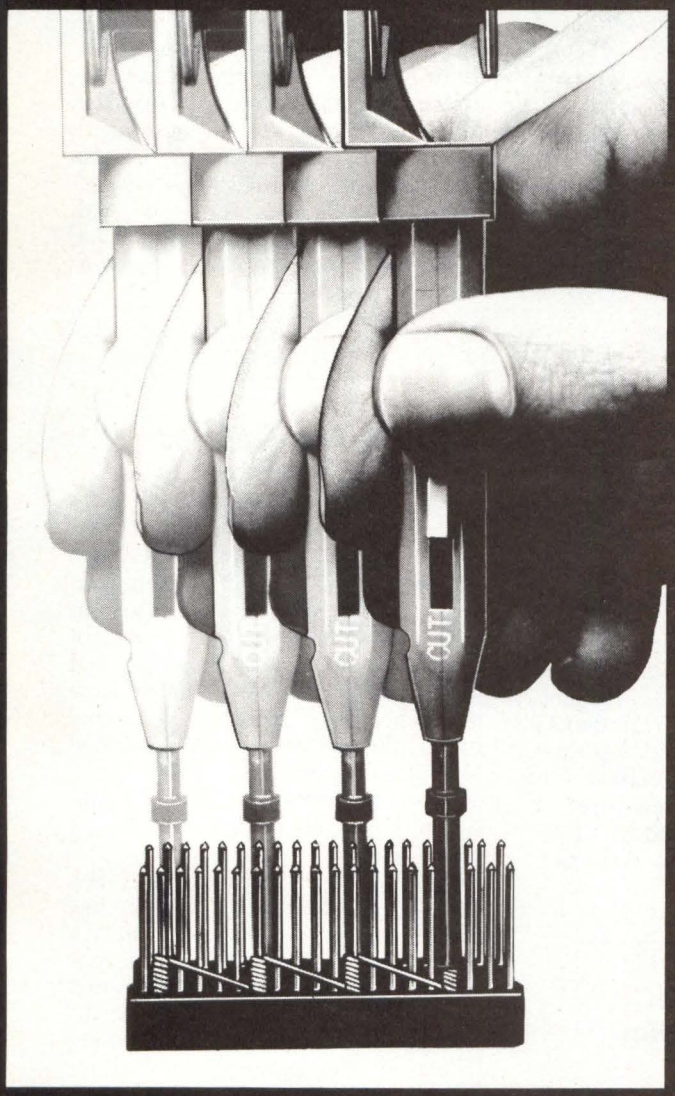
Software Package Cuts Development Time For Mini And µComputers

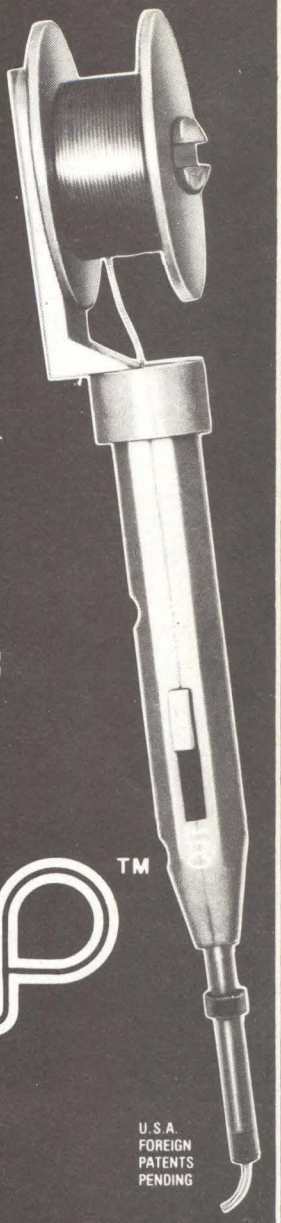
A fully interactive operating system and multilevel programming language for the TI9900 and 8080, polyFORTH™ can cut software development time for mini and microcomputers by 50 to 90% while reducing memory requirements by 30 to 80%. It will be available for the 8086, LSI-11, PDP-11, Series/1, and Honeywell Level 6 later this year. Features include faster dictionary search algorithm, all 16-bit arithmetic, more secure multiprogrammer, simplified vocabulary handling, simpler target compiler, and improved text editor. With the target compiler, code can be executed directly for testing or can be immediately output.

Developed by Forth, Inc, 815 Manhattan Ave, Manhattan Beach, CA 90266, the standard package requires only 4k bytes of memory with an added 2k bytes for the assembler and text editor. The structure is made up of a nucleus of essential operators surrounded by outer levels of the compiler and terminal handler, and a buffer handler that supports RAM as mass storage. Options include database management and applications software, and delivery of the basic 6k system in P/ROM.

Circle 434 on Inquiry Card

NEW!





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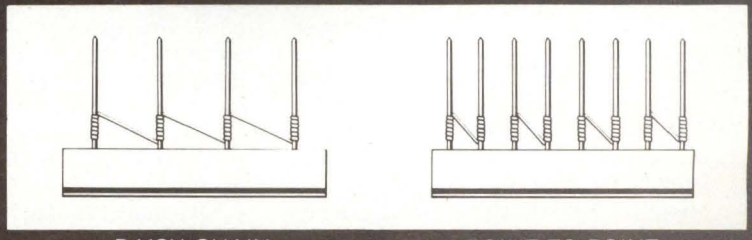

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SOFTWARE

Language Operates Faster, Covering Standard and Extended Functions

The floating point BASIC interpreter for the 6800, residing in 9.5k bytes of memory (16k are recommended), is claimed by Technical Systems Consultants, Inc, Box 2574, West Lafayette, IN 47906, to have typical speed increases of 2 to 10 times over other BASICS. All standard statements and functions, as well as many extended capabilities are supported.

Both floating point and string variables are provided with strings being fully dynamic and unrestricted in size. Variable names are either standard types or double letter combinations allowing limited variable name mnemonics. Floating point arithmetic is performed to 7-digit accuracy internally, with answers printed to six. Dynamic range of numbers is from 10^{-37} to 10^{37}.

Other features are single- and double-dimensioned arrays, an "if . . . then . . . else" construct, input line buffer increased to 127 characters, complex statement structures, and hexadecimal number representation. Array size, loop nesting, subroutine nesting, and string length are limited only by the amount of available user memory.

The language is offered on Kansas City Standard cassette with manual for $39.95; no source listing is available. A full disc file version to run under the FLEX™ disc operating system will be available shortly.
Circle 435 on Inquiry Card

FORTRAN Compiler Provides Efficient Code Sequences

A high level language facility for the Intel 8086 microprocessor includes a cross compiler operating on PDP-11 and LSI-11 computers and a runtime support library for the 8086. The compiler's FORTRAN-77 language conforms to ANSI standard X3.9-1978 at the subset level. Extensions facilitate usage in a ROM/RAM environment.

The compiler translates FORTRAN programs into assembly language statements that are assembled, linked with subprograms and runtime support routines, and downloaded to the microprocessor for execution. An application program may occupy up to 1M bytes of storage and any one program or subprogram unit may consist of up to 65k of code and 65k of local data. Arrays may be any size, up to 1M bytes.

For dedicated applications, programs may be burned into P/ROM, with RAM used for variable data storage. Assembly, linkage, and downloading facilities are provided by the Microbench™ 8086 cross assembly system also available from Virtual Systems, Inc, 1500 Newell Ave, #406, Walnut Creek, CA 94596.

Other features include 32-bit arithmetic, ROM/RAM allocation control, local code optimization, inline assembly language, user operating system interface, and Boolean functions. The package is coded in MACRO-11 for high throughput, and operates under all current DEC operating systems. Perpetual license fees start at $3750 for FORTRAN-77 and at $1695 for the Microbench cross assembler.
Circle 436 on Inquiry Card

Disc Extended BASIC Integrates Sequential Search Technique

KBASIC is Microsoft's disc extended BASIC with all the facilities of Tascon Corp's keyed indexed sequential search (KISS) file control technique integrated by EIDOS Systems Corp, 315 Wilhagan Rd, Nashville, TN 37217, into a homogeneous database management system. Several commands and a function such as initialize, open, close, insert, remove, and update files add to the repertoire of BASIC commands to produce a high level language with file control sophistication.

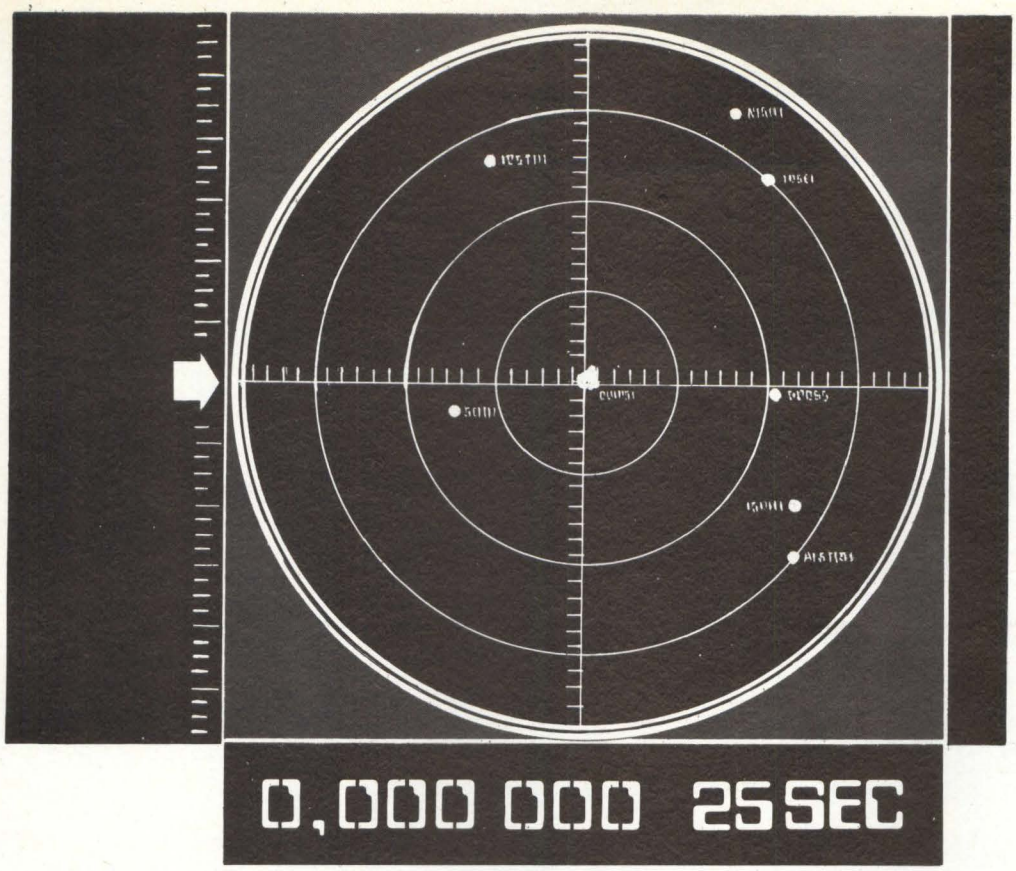
Depending on key and data length, the file control produces record search and file retrieval operations on microcomputers, under Intel's ISIS II™ and Digital Research's CP/M™, at a rate faster than that of currently available file methods. Absolute number of disc accesses to retrieve any record is three. The file system is modularly organized to provide a distinct logic file manager for both the multikeyed indexed sequential and direct access systems, controlling logical random records in sizes from 64 to 512 bytes in 64-byte increments. The file technique is also available as a relocatable object module configured for use with FORTRAN and assembler under CP/M, as well as PL/M, FORTRAN, and assembler under ISIS II.
Circle 437 on Inquiry Card

Memory-Resident and Transient Commands Power Operating System

A floppy disc based operating system for the 6800 family of microprocessors, CP/68™ furnishes a combination of memory resident and transient commands to achieve flexibility and power. The peripheral interchange program (PIP) transfers data between physical devices. Manipulation of classes of files allows either ambiguous or unambiguous file specification. User commands can be added to the system.

Hemenway Associates, Inc, 101 Tremont St, Suite 208, Boston, MA 02108, has included complete device independent I/O, sequential and random file access methods, command files, dynamic allocation and expansion of files, and chaining and overlaying of user programs. Fitting in less than 8k of memory, the system can be relocated anywhere. DOS services are available through a single supervisor call. The instruction set has been extended to include 19 6809 type instructions.

Running on Percom, ICOM, MSI, Smoke Signal, Micropolis, and SWTPC systems, the software interfaces easily with devices and peripherals, such as line printers, CRT consoles, paper tape readers and punches, and auxiliary consoles. Other software that runs more efficiently on the operating system includes EDIT 68 text editor, ASMD68 macro-relocating assembler, STRUBAL+ compiler, LNKEDT linkage editor, and XREF cross reference generator, all of which reside as transient commands. □
Circle 438 on Inquiry Card



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654 2 097

IMPLEMENTING A DIGITAL FILTER IN CUSTOM LSI—CHIP AREA CONSIDERATIONS

Lynn Schmidt

Hewlett-Packard Company
Loveland, Colorado

Once the exclusive province of analog systems, many signal processing functions are now achieved with digital integrated circuits, because of significant cost reductions accomplished within recent years. A most exciting aspect of this trend is the ability to integrate entire digital signal processors on one chip through the use of custom integrated circuits.

Having an integrated circuit process available gives the digital filter circuit designer an added dimension in flexibility, since virtually any type of memory or arithmetic device can be specified. However, along with this freedom comes an added constraint relating to total chip area. Together, these factors require the filter designer to make tradeoff decisions and seek innovative solutions that differ from those used in building digital filters using TTL.

The digital filter IC used in the Hewlett-Packard 3582A spectrum analyzer exemplifies such a design.[1] Based entirely on digital signal processing techniques, the analyzer derives much of its signal processing capability from four single-chip custom LSI digital filters. These filters in the analyzer band-select that portion of the spectrum to be analyzed and reduce the sample rate accordingly. This process of simultaneous digital low pass filtering and sample rate reduction is called "decimation filtering."

Interest in integrating these digital filters was motivated by the promise of hardware savings of more than 80%, with lower cost, lower power, and higher reliability, when compared to the discrete TTL alternatives (see Table). The requirement for performing 3M to 6M multiplications/s virtually eliminated any possibility of using available microprocessors to perform the filtering.

Cascaded Filters

In designing the filters for the analyzer, it was recognized that certain advantages could be obtained by implementing each filter as a cascade of several smaller filters with interstage decimation of the sample rate. Each filter stage then needs to accomplish only a modest sample rate reduction with a consequent reduction in the complexity of the filter stage. In addition, downstream filters in the cascade compute at reduced sample rates, further simplifying computational requirements.

As shown in Fig 1, a cascade of eight filters in series is used with the output selected from any of the eight. Each filter stage is allowed to compute either a decimation by 2 or a decimation by 5, giving overall decimation ratios of $2^m \times 5^n$ where $m + n \leqq 8$. This easily satisfies the requirements for the 14 frequency spans with decimation ratios ranging from 1 to 25,000 in a 1, 2.5, 5, 10, . . . , 25,000 sequence.

An interesting aspect of this filter structure surfaces when the total computational requirements are examined. Consider the case where each of the eight filters is performing a decimation by 2. The first filter computes at the input sample rate, while the second filter needs to compute at only one-half that rate because of the sample rate reduction. In like manner, the third filter computes at one-fourth the rate, the fourth at one-eighth the rate, and so on, forming a geometric series, $1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots$ that converges to 2. This means that the total computational requirement of all eight filter stages can be satisfied by a single processor operating at twice the rate required by the first filter stage. Actually, hardware is

Discrete Versus Custom LSI

IC Process	Number of PC Boards	ICs	Power	Relative Failure Rate	Relative Production Cost
Discrete	2 to 3	160	60 W	R	C
Custom LSI	1	29	12 W	$\frac{3R}{8}$	$\frac{C}{2}$

needed for only one filter stage. The processor has eight channels of memory to store intermediate states of the filters, but uses only one set of arithmetic hardware. Fig 1(c) illustrates how the processing steps are scheduled so that the eight filter stages can timeshare the hardware.

Chip Area Considerations

Implementing this digital filter structure in LSI involves some special consideration of the elements requiring area on a chip. Fig 2 provides a miniature catalog of all basic digital elements required for construction of a digital filter. The 5- x 5-mm die size shown represents the approximate practical upper limit in the size of the total chip, based on cost and power.*

Multipliers consume the largest proportion of chip area. The analyzer's digital filter requires 12 multipliers, similar to the one shown in Fig 2, and the high speed multiply rates demanded exclude the possibility of timesharing a lesser number of multipliers.

A second area consumer is memory. The design requires approximately 1600 bits of memory. Dynamic memory takes less space than static, and serial shift registers require much less than random access memory.

The third large consumer of chip area is interconnect. About 40% of the area of most LSI chips is devoted to interconnecting the various active devices. Serial arithmetic structures offer an advantage here since only a single interconnect is needed to transfer a 24-bit word. This, however, is at the expense of the total transfer time.

Even when dynamic shift register memory and serial arithmetic are used, the total area required appears to be much greater that that available onchip. The most difficult requirement involves the arithmetic parts, with the 12 multipliers alone consuming a total area greater than that available on an entire chip.

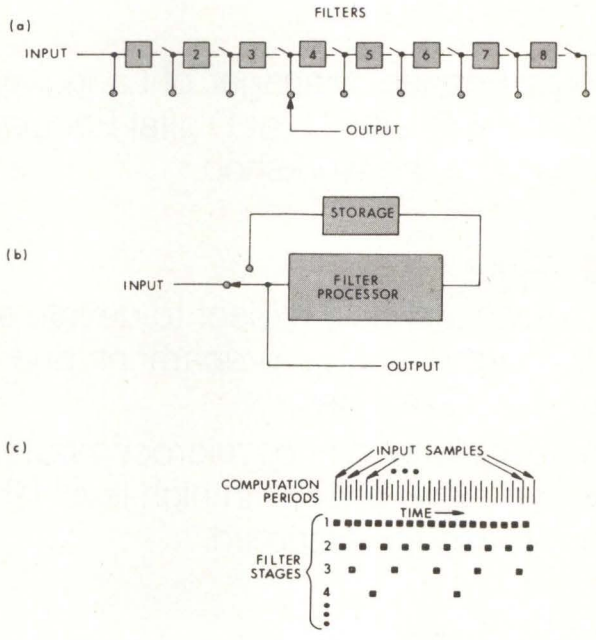

Fig 1 Cascade of eight digital filters (a) with interstage sample rate reduction used to implement filtering. Required arithmetic processing can be performed by single filter with multiple memory (b) operating at 2X speed. Interleaved processing scheme (c) for digital filter indicates that two complete filter computations are performed during each input sample period: one for first filter stage, and one for one of downstream filters

* Examples given use Hewlett-Packard's NMOS II process.[2] Recent advances in VLSI result in smaller device sizes, with relative proportions remaining the same.

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George Poonen, Manager of Languages and Data Base Research at Digital Equipment Corp. will conduct the workshop.

WARNING:

Participants should expect to devote some evening hours to course preparation and group programming exercises.

Familiarity with mini or microcomputer architecture and experience with high-level language programming is assumed.

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— overview of course

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a. Mastery of the language, and

b. Developing good programming style

A) PASCAL-I

— general form of PASCAL programs

— assignment statement

— basic I/O

— reading programs, syntax charts

— exercise 1

B) PASCAL-II

— constants, variables

— primitive data types

— precedence of operators

— lab (supervised sessions during which you will complete the given exercises)

C) PASCAL-III

— conditions

— loop structures

— selection

— exercise 2

D) PASCAL-IV

— introduction to procedures

— passing parameters by value and by reference

— functions

— nested procedures/functions and scope of names

— lab

PROGRAMMING MICROCOMPUTERS / Aug. 13-17, 1979

E) PASCAL-V
- general concepts of data types
- user-defined data types
- scalar data types
- arrays
- exercise 3

F) PASCAL-VI
- records
- sets
- pointers
- dynamic storage
- lab

G) PASCAL-VII
- sequential files
- text files
- formatting
- exercise 4
- list processing
- recursion
- advanced features—extensions
- survey of PASCAL implementation
- lab

3. High-level languages

Having learned one language, you will now be presented with a generic approach to programming languages. This approach will enable you to grasp the essential features of new languages in a matter of days.
- general approach to learning languages including PL/M and PL/Z
- introduction to ADA
- exercise 5 — ADA

4. Compilers and optimization

A brief introduction to compiler design and organization to illustrate trade-offs in language design and use. This session's objective is to enable you to utilize high-level languages in the most effective way.
- design and organization of compilers
- what good compilers will do for you
- programming techniques to improve performance
- space/time trade-offs
- examples from LSI-11, INTEL 8080, P-Code Machine

5. Evaluation of languages
- checklist for languages
- when and when not to use high-level languages

6. Summary
- review
- new developments in languages and their use in small computers

Course materials:

Specially prepared course notes, programming aids, and the following text are provided for class use and future reference:

Programming In PASCAL by P. Grogono.

Tuition, schedule and continuing education credits

Tuition is $600. This includes course notes and text, as well as Tuesday evening reception. The seminar is scheduled for 8:30 a.m. Monday, August 13, 1979, through 4:30 p.m. Friday, August 17, 1979.

3 continuing education units will be offered by Polytechnic Institute of New York to participants completing the course.

Further information

For additional information on course content, objectives, and intended audience, you can call the course coordinator, Mr. Poonen, at 617/897-5111, ext. 3537. For administrative information, call the Institute for Advanced Professional Studies at 617/964-1412. Participants are urged to register early as enrollment is limited.

In-house programs:

This workshop plus a variety of other customized technical and management courses are available for on-site presentation. Contact Donald French at (617) 964-1412 for details.

Course Registration Form

☐ Please register me for the five-day course, PASCAL PROGRAMMING FOR MINI AND MICROCOMPUTERS co-sponsored by Polytechnic Institute of New York and Institute for Advanced Professional Studies to be held August 13-17 at the Ramada Inn, Woburn, Massachusetts 01801.

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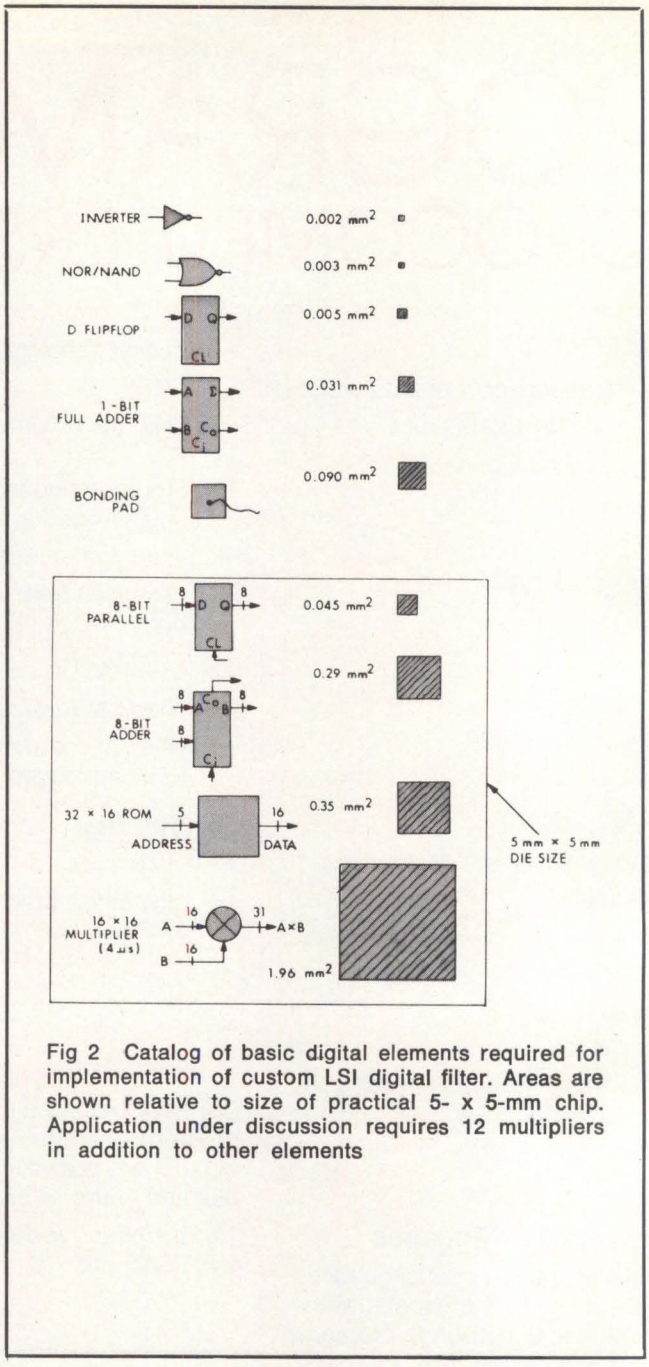

Fig 2 Catalog of basic digital elements required for implementation of custom LSI digital filter. Areas are shown relative to size of practical 5- x 5-mm chip. Application under discussion requires 12 multipliers in addition to other elements

Summary

A digital filter structure, implemented as a cascade of eight filters, is to be integrated on one chip. However, some parts occupy considerably more space than others, with arithmetic portions of the structure posing the major problem. As a result the multipliers and associated coefficients become the key elements in design strategy, requiring special arithmetic techniques to allow a reduction in chip area required by the multipliers. These techniques will be discussed in the July column.

References

1. N. A. Pendergrass and J. S. Farbach, "A High-Resolution, Low-Frequency Spectrum Analyzer", *Hewlett-Packard Journal*, Sept 1978, pp 2-14
2. J. E. Deweese and T. R. Ligon, "An NMOS Process for High-Performance LSI Circuits", *Hewlett-Packard Journal*, Nov 1977, pp 26-32

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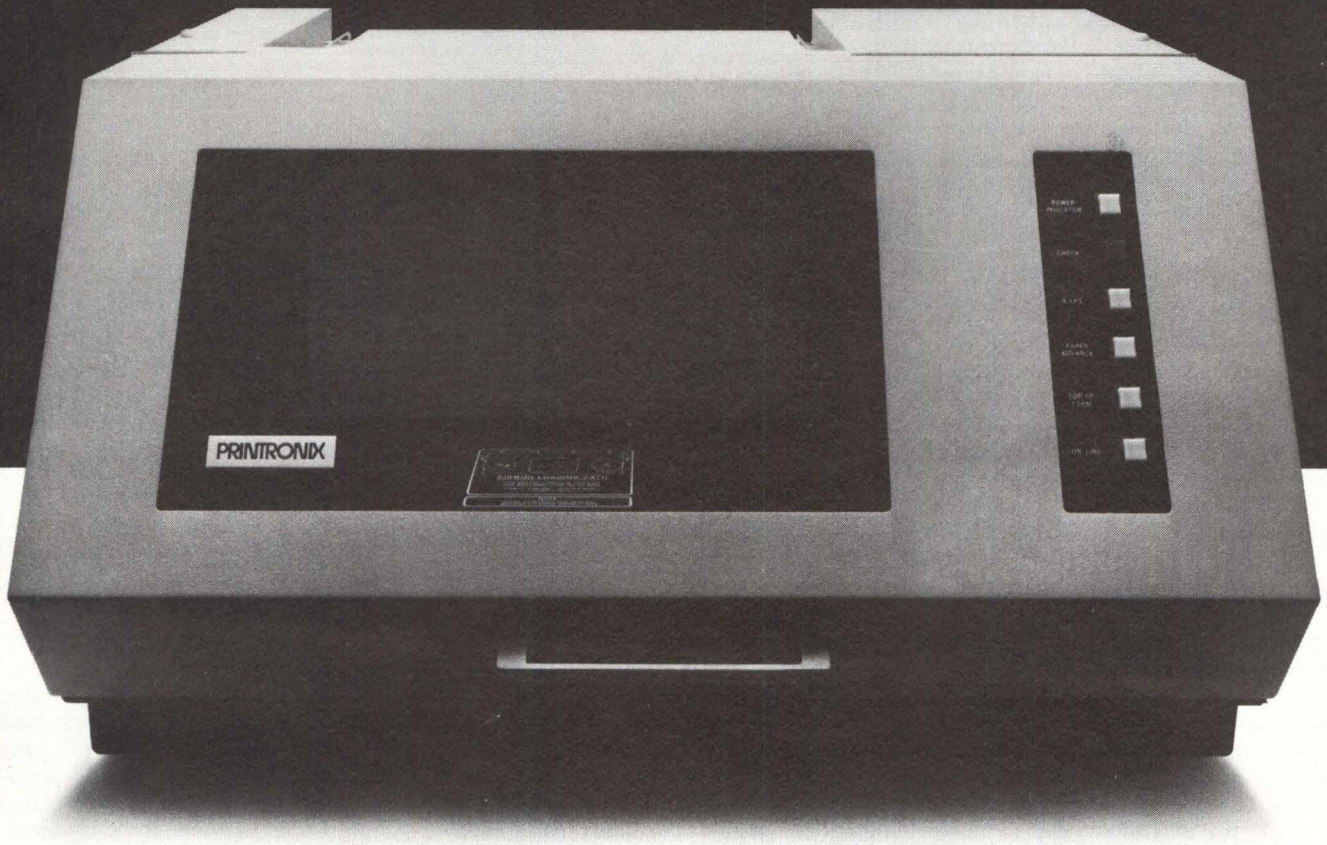

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CCD Image Sensors Offer Improved Sensitivity Over Visible and IR Spectrum

Charge-coupled devices functioning as linear image sensors are more sensitive than previous devices by a factor ranging from 2 to 4 over a broad band of visible and infrared wavelengths, with the relative blue response at 450 nm increased approximately fivefold (Fig 1). Applications for the sensors are in facsimile systems as well as other line scan systems.

These buried channel isoplanar sensors are the CCD122 in a 24-pin package with 1728 elements/line and the CCD142 in a 28-pin package with 2048 elements/line. As a second generation of line imaging devices, the family is designated LID-II. Produced by Fairchild Camera and Instrument Corp, Semiconductor Products, 464 Ellis St, Mountain View, CA 94042, the devices provide resolution of 200 elements/in (79/cm) for two common paper formats. The major areas of sensor improvement are in the electro-optical characteristics, the simplicity of external drive functions, and the quality and versatility of the output signals.

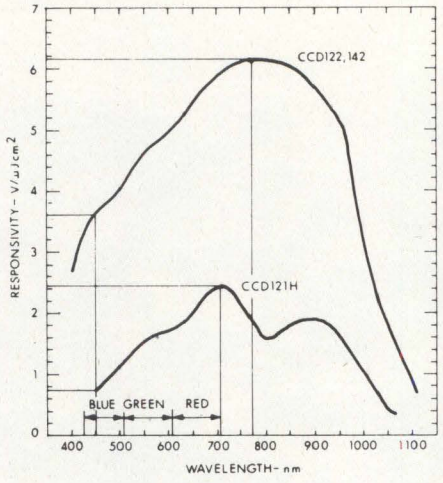

Fig 1 CCD line-imaging devices, Fairchild's CCD122/142, have greater responsivity than old version, from blue part of spectrum through IR. Improvement is particularly evident in blue region, as demonstrated by factor of approximately 4.8 at 450 nm

Responsivity of an image sensing device significantly affects the design of document and scanning systems because it determines the required light source intensity. Need for high intensity light sources increases the structural, ventilating and power requirements of the equipment, thus impacting size, weight, and cost. In the LID-II sensor design, the photosensing area does not require an overlaying polysilicon gate as did the first generation sensor. Removal of the gate structure eliminates light absorption, particularly in the blue region of the spectrum. The improved response is obtained from square photoelements 13-μm on a side, instead of the 13- x 17-μm elements in the first generation design, thereby increasing the resolution in the mechanical scanning direction to equal that of the electrically scanned direction.

Photosites are spaced 13 μm center to center along the long axis of the sensor die. The photosensitive area is 13 μm x 2.246 cm for the 1728-element device and 13 μm x 2.662 cm for the 2048-element device. A 70-μm separation between the transfer region and the photosites reduces optical crosstalk from the photosites to the transport registers (Fig 2), effectively increasing sensor resolution. Without the long separation, carriers generated in the neutral bulk can diffuse laterally and collect in the transport register, where they combine with any charge packet in transit.

Both sensors include onchip driver circuits, which permit operation to be controlled with only three external clock signal inputs instead of the five clocks needed with earlier devices. A square wave transport clock controls the readout rate of video data from the sensor, a transfer clock pulse controls exposure time of the sensor, and a reset clock signal controls the integrated output signal amplifier.

An integrated sample-and-hold charge sensing circuit provides a continuous low source-impedance analog video waveform at the chip output, with a typical amplitude at saturation of more than 1 V pk-pk. The video waveform includes dark and white reference levels to permit easy dc restoration or the use of automatic gain control circuitry. Second output ports provide an end-of-scan output pulse indicating that readout of a line of information has been completed.

In operation, photoelectrons are collected in the individual photosites under control of a photogate. At the end of an integration interval of selected duration, a transfer gate is pulsed high to transfer the packets of accumulated electrons into the two neighboring CCD shift registers. The charge packets are then transported serially down the analog shift registers under control of the transport clock and are sequentially detected by the first stage of the output amplifier. A MOS sampling switch couples the sensed charge levels to the output stage of the video sense amplifier.

A 4.5 x 5" (11.4 x 13-cm) demonstration board is available for familiarization with CCD linear imaging devices or for construction of

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CIRCLE 90 ON INQUIRY CARD

experimental systems using these sensors. The preassembled board provides all bias voltages and clock waveforms required for operation of the sensors, as well as an elementary processing circuit providing a low output impedance video output signal. A CCD sensor can be placed in a socket on the back of the demonstration board, and the user can easily mount a lens in front of the sensor to complete a fully functional linear image sensing system.

Typical performance characteristics of the sensors include a data rate of 500 kHz and a 10-ms integration time at a 25 °C operating temperature. The two devices are pin compatible, the 24-pin device being usable in the socket of the 28-pin device whose four corner pins are either grounded or not connected. Both sensors utilize a ceramic DIP with a plastic-sealed optical glass window.

Circle 350 on Inquiry Card

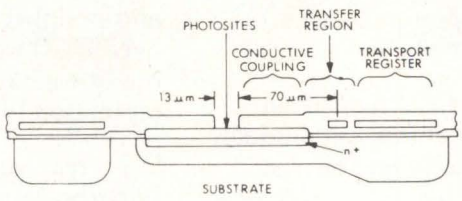

Fig 2 Cross-section of line-imaging device. Electron packets generated by photon absorption and collection in photosites are conductively coupled to transfer region over 70 μm distance. Conductive coupling is applied to avoid slow, inefficient transfer that would normally result from CCD transfer over this distance

Back Panels Constructed And Wirewrapped To Custom Specs

Both standard and custom-built backplane assemblies, wirewrapped and constructed to customer specifications, are available as a complete design service from Garry Manufacturing Co, 1010 Jersey Ave, New Brunswick, NJ 08902. These assemblies include a low impedance voltage/ground distribution system with connector terminals connected directly to the V_{CC} and ground bus.

The manufacturer also provides standard catalog backplanes, which fit the industry standard EIA 19″ (48-cm) card racks. These accommodate 13 single- or double-height wirewrap cards or 25 single- or double-height PC boards. Custom wirewrapped backplanes include Multibus, Omnibus, CAMAC, LSI-11, and S-100 bus interconnections.

On all of the backplanes, the motherboard is 0.125″ (3.175-mm) thick glass epoxy 94V2 material, with 2-oz (56-g) copper voltage and ground planes, both sides solder coated. Board-mounted connectors are either card edge type or socket receptacles with wirewrap terminals protruding through the rear of the motherboard.

Circle 351 on Inquiry Card

Diffused Resistors Are Utilized in Trimless 12-Bit DACs

A digital to analog converter having a guaranteed maximum nonlinearity to ±0.012% (13 bits) over its full operating range is claimed to be the first 12-bit DAC to use standard bipolar processing without any requirement for thin film resistors or active trimming of individual devices. The converter departs from traditional R-2R ladder designs to utilize a proprietary diffused resistor approach, providing monotonicity and speed.

Based on this design approach, the Am6012 from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, furnishes, in addition to its guaranteed linearity, a guaranteed full 12-bit monotonicity for all grades over the −55 to 125 °C operating range. This performance is independent of power supply voltage and temperature variations.

Other characteristics include a 250-ns (typ) settling time to ±0.01%, high impedance outputs with a voltage compliance of −5 to 10 V, and ±5-ppm/°C full-scale drift. High speed multiplying inputs allow the use of a dc, ac, or pulsed reference signal. Power dissipation typically ranges from 230 to 290 mW depending on supply levels.

In operation the DAC requires 4.5 to 18 V and −10.8- to −18-V supplies and drives a full-scale output current of 4 mA. Its dual complementary outputs permit differential operation and can present a constant load current to significantly reduce switching transients and increase throughput. These outputs can usually connect directly to the analog portion of the system without op amps.

The proprietary segmented design of the device furnishes a more uniform step size than is possible with standard binary weighted DACs. This allows for finer resolution of levels and is important where local linearity is critical. In many applications, uniform step size is more desirable than conformance to an ideal straight line from zero to full scale. Additional features include a reduction in resistor matching and tolerance requirements by a factor of eight, and reduction of component count from 37 resistors (for an R-2R ladder implementation) to 24 resistors in this segmented design.

Circle 352 on Inquiry Card

64k Dynamic RAM Includes 3k Spare Elements to Replace Faulty Cells

Spare elements on a 65,536-bit random access memory chip are used to replace elements in faulty bit locations on the same chip. Along with this built-in error correction capability, the RAM has an access time of less than 170 ns and requires refresh only 128 times every 4 ms. NMOS technology is utilized in the fabrication of this dynamic memory, developed by Bell Telephone Laboratories, Mountain Ave, Murray Hill, NJ 07974, and designed to be compatible with Western Electric's 16k memory. Adaptation for that purpose requires lowering the V_{DD} power sup-

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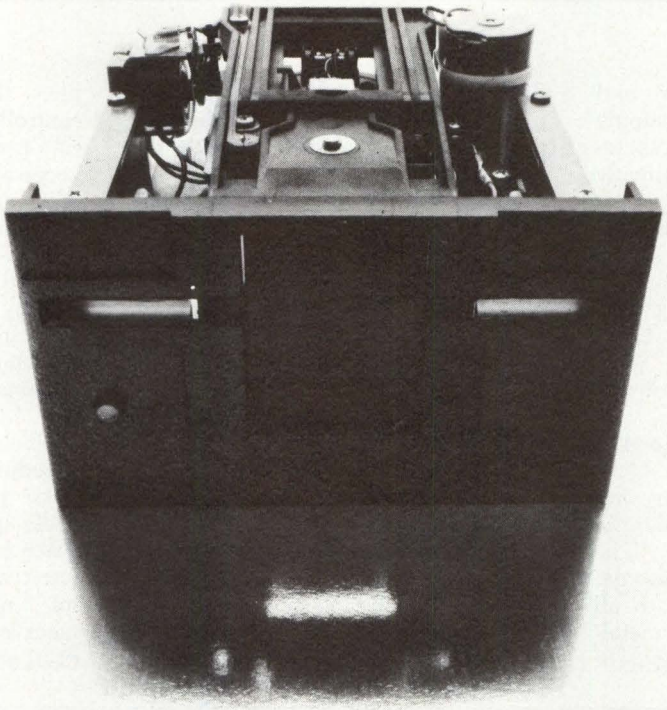

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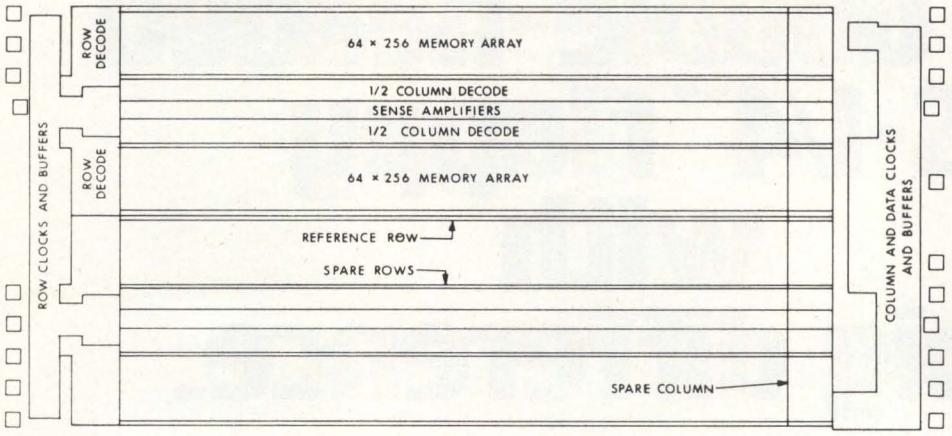

64k dynamic RAM from Bell Telephone Laboratories includes redundant elements to replace faulty memory locations. Chip contains 5% more elements than needed. Substitution of spares is accomplished in less than 10 s (typ)

ply voltage from 12 to 8 V and replacing the 5-V V_{CC} power supply lead with a multiplexed address input. A −5-V V_{BB} supply is already available at the socket.

The memory cell, a 1-transistor, 1-capacitor structure, uses polysilicon bit lines for signal enhancement. Dual 32k-bit architecture, along with partial selection and stepped recovery, holds active power and peak current to values below that of the 16k memory. Worst case row- and column-enable access times are 170 and 100 ns, respectively.

Selecting and incorporating redundant elements involves only the opening of appropriate links. The 3-μm wide polysilicon links are deposited and patterned along with all active transistor gates. Prior to metallization, the links and the balance of the chip are covered with phosphorous glass. There are no separate processing steps associated with the links.

Laser opening of the links is done on a commercially available laser trimming machine modified to provide automatic wafer handling as well as the necessary positioning accuracy. Testing and replacement of elements in the memory chips are fully automatic and require no additional wafer handling or manual intervention.

At the probe station, the wafer is functionally tested and the location of elements to be replaced is mapped out in the computer memory. Since there are many ways to put in the redundant elements, the computer program uses an algorithm to determine the optimum way to exploit the redundancy. A computer controlled laser beam is directed to the precise locations on each chip necessary to delete elements and program in selected redundant elements.

To remove a row, the polysilicon link in series with the metal line is opened with the laser beam. In removing a column, the links in the path from the sense amplifier to the data bus are opened. The column line remains connected to the sense amplifier, but the output from it never reaches the data bus. To substitute a redundant row or column, several links within the row or column decoder are opened by laser energy. After laser programming, the chip is retested. The substitution of spares for marginal elements typically takes less than 10 s/chip.

Circle 353 on Inquiry Card

Nonmultiplexed CMOS Driver/Decoders Drive LCD, LED Displays

Capable of driving 4-digit, 7-segment displays, two nonmultiplexed CMOS devices are available from Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014. They are a BCD to LCD display driver for use in low power applications and a driver/decoder for LED displays. CMOS construction requires only minimal power, typically 10 μA at 5 Vdc.

The ICM7211 is configured to drive conventional LCD displays, and includes a complete (no external components necessary) RC oscillator, divider chain, backplane driver devices, and 28 segment outputs. These outputs provide the zero dc component signals necessary for long display life.

Configured to drive common anode LED displays, the ICM7212 provides 28 current controlled low leakage open-drain n-channel outputs. It furnishes a brightness input which may be used at normal logic levels as a display enable or (with a potentiometer) as a continuous display brightness control.

Both the LCD and LED drivers are available with two input configurations. The basic models provide four data bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226, and ICL7103. The microprocessor interface (suffix M) versions provide data input latches and digit select code latches under control of high speed chip select inputs. They simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

Two different decoder configurations are available. The basic device will decode the 4-bit binary input into a 7-segment alphanumeric hexadecimal output. Versions with suffix A will provide the same output code as the ICM7218 Code B, ie, 0 through

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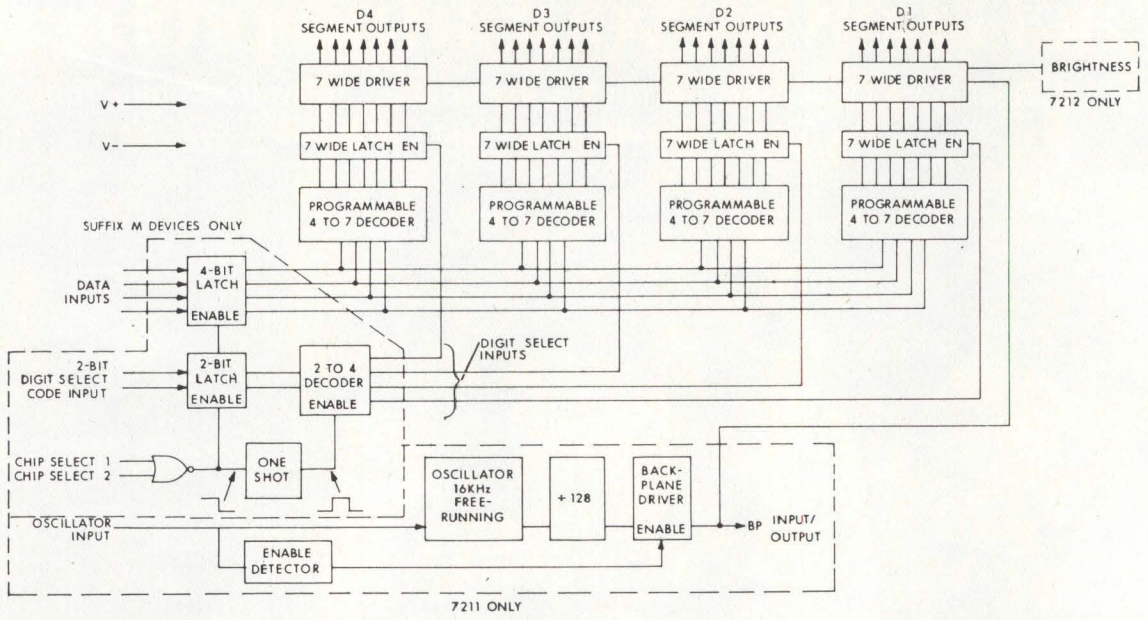

Intersil's 4-digit LED/LCD decoder/drivers are available in two basic models, ICM7211 (LCD driver) and ICM7212 (LED driver). Suffix M versions of these are suitable for microprocessor interface

9, E, H, L, P, dash, and blank. Either version will correctly decode true BCD to 7-segment decimal outputs.

The chips may be ganged or cascaded to allow for 8-, 12- or 16-digit displays. Applications include: low cost direct interface between digital systems and microprocessors to the LCD or LED display; 3½-digit BCD readouts for A-D converters; instrumentation displays such as capacitance meters, counters, DVMs, and DPMs; and battery powered digital systems.

Absolute maximum ratings for all the driver/decoders set 0.5 W as the upper limit on power dissipation (at 70 °C). Supply voltage ($V^+ - V^-$) must be 6.5 V or less, and input voltage on any terminal must lie between V^+ 0.3 V and V^- −0.3 V. The allowable temperature range is −20 to 70 °C for operation and −55 to 125 °C for storage. All devices in the family are provided in standard 40-pin plastic dual-inline packages.

Circle 354 on Inquiry Card

Temperature Range Extended for CMOS MUXs

Operation is guaranteed over a −55 to 125 °C temperature range for a family of CMOS multiplexers. The 4551-01 is a differential 8-channel device, with a 3-bit digital word plus enable selecting the channel, while the 4552-01 has 16 single-ended channels selected by a 4-bit word plus enable. Produced by Teledyne Philbrick, Allied Dr at Route 128, Dedham, MA 02026, these are wide temperature versions of the 4551 and 4552, existing multiplexer products by the same manufacturer.

Other recent additions to this line include the 4553 (differential 4-channel) and 4554 (8-channel single-ended), with the -01 suffix wide temperature versions (−55 to 125 °C) announced concurrently. For these devices, channel selection is controlled by enable plus 2- and 3-bit words respectively.

All of these devices feature overvoltage protection on both analog and digital inputs and are also protected against damage when inputs are present with power removed. Switching action provides break-before-make operation, thereby preventing the connection of one input to another when a new channel is selected. In data acquisition systems, channels may be selected in sequence by driving the digital inputs directly from a counter, or may be controlled randomly from a central processor. These multiplexers are particularly useful in portable applications due to their low power consumption, and their ease of compatibility with CMOS, DTL, and TTL families. Other characteristics include input voltage range of ±15 V, input leakage current of ±50 nA, power dissipation of 7.5 mW, and access time of 1 μs.

Circle 355 on Inquiry Card

Two Phase Comparators Are Combined In MiniDIP

A pair of independent output phase comparator circuits make up the MM74C932, a CMOS device produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara,

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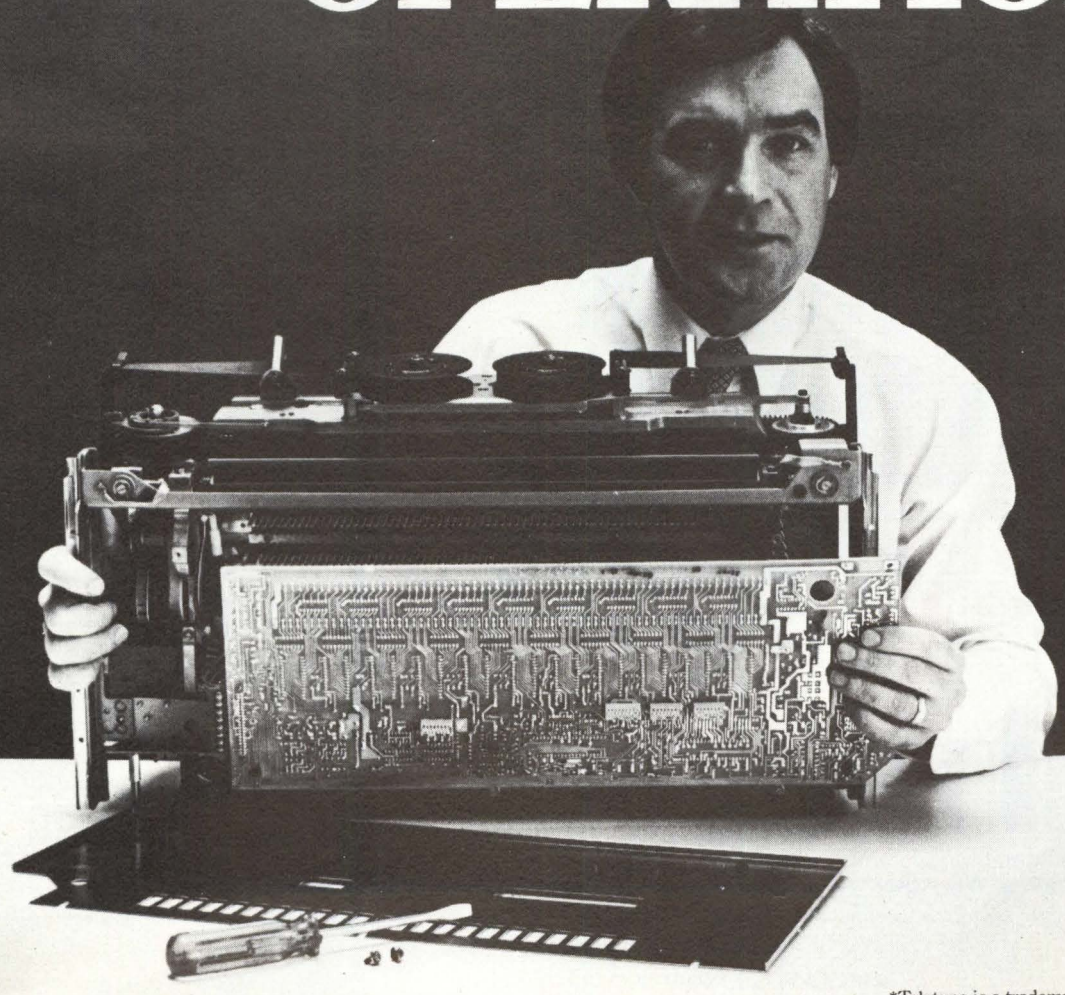

CIRCLE 93 ON INQUIRY CARD

*Teletype is a trademark and service mark of the Teletype Corporation.

CA 95051. It features a wide supply voltage range and an input voltage sensitivity of 200 mV (typ).

The first phase comparator is an exclusive-OR gate circuit that provides a digital error signal output, while maintaining 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle) it may lock onto the signal input frequencies that are close to the harmonics of the VCO center frequency. The second phase comparator is an edge controlled digital memory network that provides a digital error signal and lock-in signal (phase pulses) to indicate a locked condition, and maintains a 0° phase shift between signal input and comparator input.

Both comparators have the same signal input and comparator input, enabling the user to couple the signal input directly for a large voltage signal or to couple it capacitively to the self-biasing amplifier at the signal input for a smaller voltage signal. The combined device is housed in an 8-pin MINIDIP and is priced at $0.65 in thousands.

Fast Gate Arrays Implemented With ECL Circuits

A 0.5-ns gate delay and the capability of replacing 15 to 20 standard ECL 100k circuits characterizes a family of gate arrays offered by Siemens Corp, 186 Wood Ave S, Iselin, NJ 08830. The arrays feature 64 pins and typically accommodate 500 gates at 2-W dissipation. These devices are part of the SH ECL family, by the same manufacturer, a family that also includes LSI and MSI circuits.

Designed for use in very fast computing applications, the arrays provide a high packing density, with a maximum of up to 700 gates per chip. Power dissipation is 2 mW per internal gate (typ). Other general features include simple design access, short turnaround time, and I/O levels fully compatible with the SH 100 circuits.

Customized circuits are based on three gate array types. The LSI 24 contains 24 logic cells, 300 gates (typ), and dissipates 1.7 W (typ). A total of 36 logic cells, 550 gates (typ), and a 2.4-W (typ) power dissipation are characteristic of the LSI 36. Finally, the LSI 24 RAM contains 24 logic cells, 4 RAM cells of 32 bits each, and a 2.5-W typical power dissipation. Each of the three array types includes 58 I/O cells.

A logic cell contains a pattern of 54 components (38 transistors, 16 resistors). Through use of individual metallization patterns stored in a library, 32 different MSI functions can be realized by a logic cell. These functions are comparable in complexity to those in existing ECL 10k families, and include such examples as: two 3-input NOR gates and two 1-input expandable OR/NOR gates; three 2-bit multiplexers with common inhibit; and a 4-bit flipflop arrangement for a counter (quad cell).

Circle 356 on Inquiry Card

C. Itoh's Model 8300 printer looks superb.

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CIRCLE 95 ON INQUIRY CARD

Octal Bidirectional Transceivers Meet IEEE 488 GPIB

Octal bidirectional transceivers conforming to the IEEE 488 Instrumentation Bus Standard are now independently available, in differing designs, from two different sources. Replacing previously existing quad transceivers, these devices interface between instrumentation systems and the 16 lines of the General Purpose Interface Bus.

Specialized Data and Protocol Transceivers

Two 8-line bidirectional bus transceivers, the SN75160 data bus transceiver and the SN75161 management bus transceiver (Fig 1), introduced by Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, meet IEEE Standard 488-1978. Both devices feature built-in bus-terminating resistors on driver outputs, no loading of the bus when the device is powered down, high impedance PNP inputs, high speed low power Schottky circuitry, 95-mW (max) power dissipation per channel, and a receiver hysteresis of 500 mV (typ).

The data bus transceiver has an open collector, driver output option, which is selectable through applying a pullup enable (PE) signal to the device. When PE is low, the bus outputs of the transceiver act as open collector outputs. The outputs act as 3-state ports when PE is high.

All the internal logic required for proper direction control on the management bus is contained in the management bus transceiver. This transceiver also has properly assigned output structures, totem-pole or open collector, in compliance with the IEEE standard.

Each of these complementary devices is manufactured in a copper-clad KOVAR lead frame that extends the maximum allowable power dissipation to 1675 mW at 25 °C. They are offered in 20-pin, 300-mil wide plastic dual-inline packages, and are specified for operation over the commercial temperature range of 0 to 70 °C.

Propagation delay times from terminal to bus for each of the transceivers (at V_{CC} = 5 V, T_A = 25 °C, and C_L = 15 pF) are 14 ns with low to high level output and 17 ns with high to low level output. For the bus to terminal condition, these values become, respectively, 30 and 35 ns. A single 5-V supply provides the power, with an absolute maximum rating of 7 V for V_{CC}. Supply current with receivers low and enabled is 80 mA (typ), 105 mA (max). With drivers low and enabled, the corresponding values are 100 mA (typ), 145 mA (max).

Circle 357 on Inquiry Card

Single Design for Data or Protocol

The MC3447, from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, meets IEEE Standard 488-1975. An identical pair of octal GPIB transceivers permits the implementation of the 16-line standard (Fig 2). By choosing an appropriate organization of data and protocol lines through the transceiver, and by choosing an appropriate organization of the enable combinations and polarities within the transceiver, this single device can be made to serve in either a data or protocol function.

Either the driver or the receiver of each channel is enabled by a send/receive input, with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis (600 mV typ) to improve noise margin, and their input loading follows the bus standard specifications.

Low power consumption (95 mA max supply current, with all drivers on) has been achieved by trading speed for low current drain on noncritical channels; that is, seven of

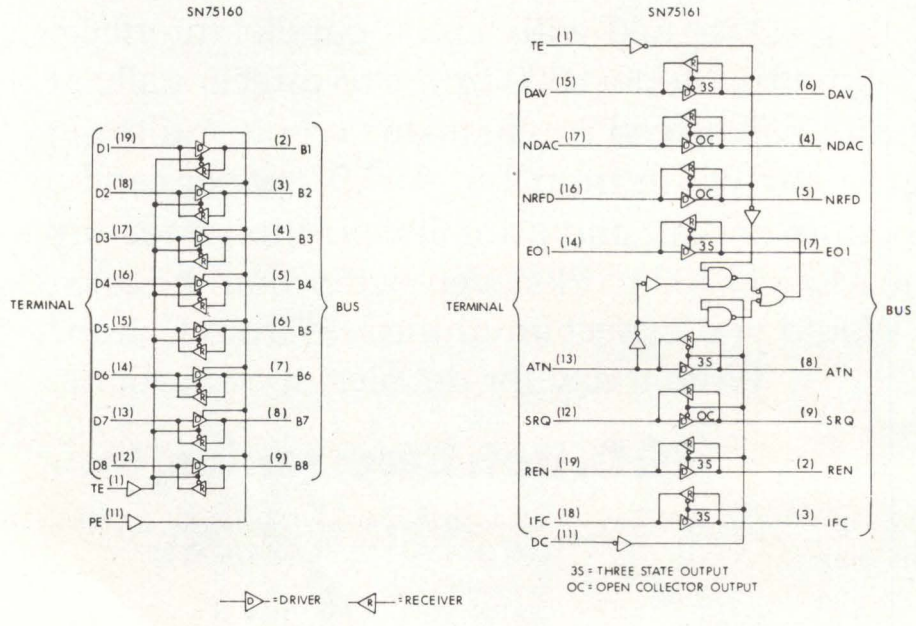
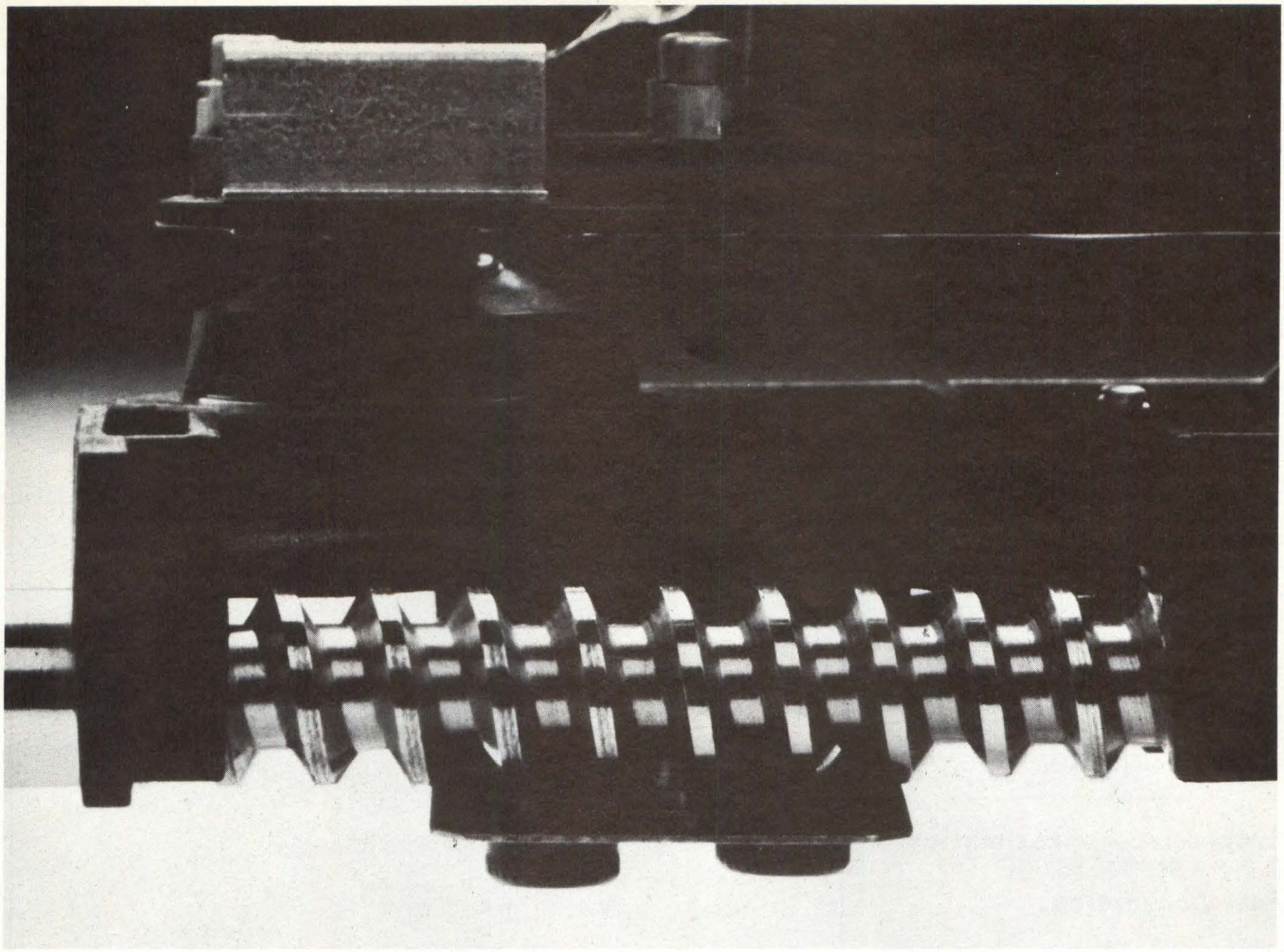


Fig 1 GPIB transceivers from Texas Instruments are designed to IEEE 488-1978 standard. Data bus lines are handled by SN75160 transceiver. Protocol lines are interfaced via SN75161



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We do it by increasing the track density of our MegaFloppy drives to 100 tracks per inch. That lets us record 77 tracks – as many as on 8-inch 48 TPI drives. This configuration gives us a capacity of up to 946K bytes per drive.

Here's how our double track density works.

While most floppy drives use a cheap, less accurate plastic cam or cam follower to position the read/write head, we use a stainless steel, precision-ground lead screw. Because it helps us achieve high-track storage capacity with lower cost per thousand bytes. And significantly increases reliability.

The lead screw is coupled to the head carriage using a zero backlash, leaf-spring loaded ball. Whose diameter is large enough to contact both lead screw side walls. So ball and screw wear don't lead to loss of positioning accuracy.

A 7.5° 4 phase permanent magnet stepper motor activates the lead screw so that each step command causes the motor to increment 4 "mini steps" equal to one track movement. This reduces stepper motor inaccuracies and friction effects by the ratio 4:1.

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Maybe all this is why people are beginning to realize just how good our drives really are. Because they've made us Number 2 in the marketplace, with over 20,000 units shipped.

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For a descriptive brochure, in the U.S. call or write Micropolis Corporation, 7959 Deering Avenue, Canoga Park, California 91304. Phone (213) 703-1121. Or, better yet, see your local representative.

CIRCLE 96 ON INQUIRY CARD

the eight channels have a worst case propagation delay of 50 ns, which is adequate for a wide variety of applications. The eighth is a fast channel that provides for critical ATN (attention line) and EOI (end or identify) paths, with worst case propagation delays of 30 ns low to high and 22 ns high to low. This meets the turnaround delay requirements of the transceiver/bus controller combination on the ATN and EOI protocol lines as required by the 488-1975 standard. Typical propagation times range from 15 to 20 ns.

The transceiver has TTL compatible receiver outputs and operates from a single 5-V supply. It provides power up/power down protection against transmission of invalid information and does not load the bus when power is removed from the devices. The 24-pin package is available in both plastic and ceramic versions.

Circle 358 on Inquiry Card

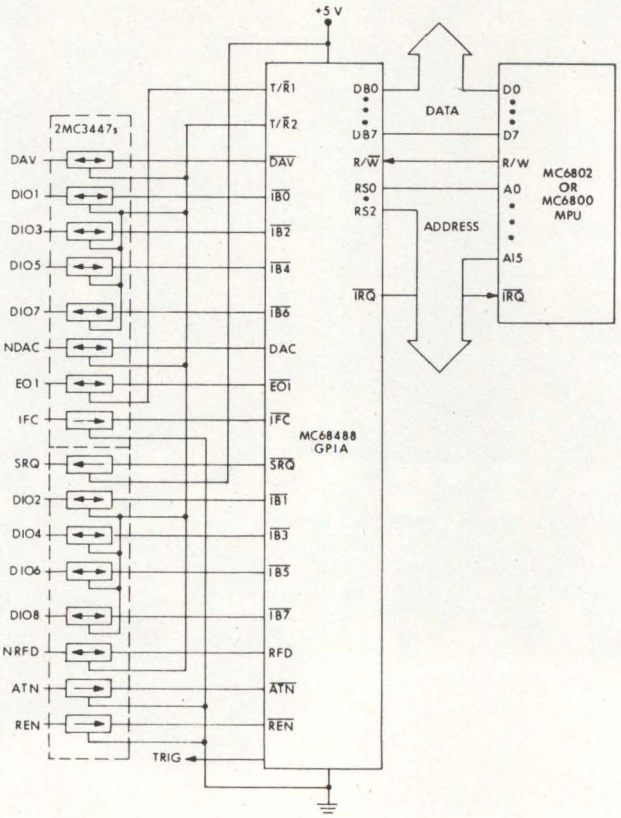


Fig 2 Single design is employed by Motorola to meet IEEE 1975 standard. Pair of MC3447 transceivers handle data and protocol lines from GPIB

Successive Approximation 8-Bit ADC Performs Fast Conversion

Offering a 25-μs conversion time (typ) to $\pm\frac{1}{2}$ LSB accuracy, an integrated circuit chip is said to be the lowest cost complete 8-bit successive approximation analog to digital converter in the industry. The monolithic microprocessor compatible device contains a clock, comparator, successive approximation register, buried zener reference, DAC, and 3-state output buffers, and requires no external components to perform a full accuracy conversion. Pricing for the converter is from $14.95 in hundreds.

Features of the AD570 from Analog Devices, Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062, include guaranteed 8-bit accuracy and no missing codes over the operating temperature range. Utilizing power supplies of 5 and −15 V, the ADC will accept externally selectable inputs of 0 to 10 V unipolar or ±5 V bipolar. Power dissipation for the IIL laser trimmed device is 145 mW (typ).

Two grades are available: the J suffix version is specified over the 0 to 70 °C temperature range, while the S suffix is specified over the −55 to 125 °C range and is available fully processed to MIL-STD-883B, class B. Both grades are packaged in hermetic sealed, ceramic side-brazed DIPs. All devices are given long term stabilization bakes, burned in under power at 125 °C, temperature cycled ten times from −65 to 150 °C prior to final test, and are tested 100% over their respective temperature ranges. Circle 359 on Inquiry Card

1k High Density CMOS Static RAMs Operate at Low Power

A single 5-V power supply and a maximum supply current of 10 μA, dropping to 1 μA (typ) while on standby, are characteristics of a line of high density CMOS (HD/CMOS) 1024-bit static random access memories. The MP6508 (16-pin DIP) and MP6518 (18-pin DIP) retain data when power drops to as low as 2 V. These devices are recommended by the manufacturer, Micro Power Systems, Inc, 3100 Alfred St, Santa Clara, CA 95050, for "nonvolatile storage" through the use of battery backup.

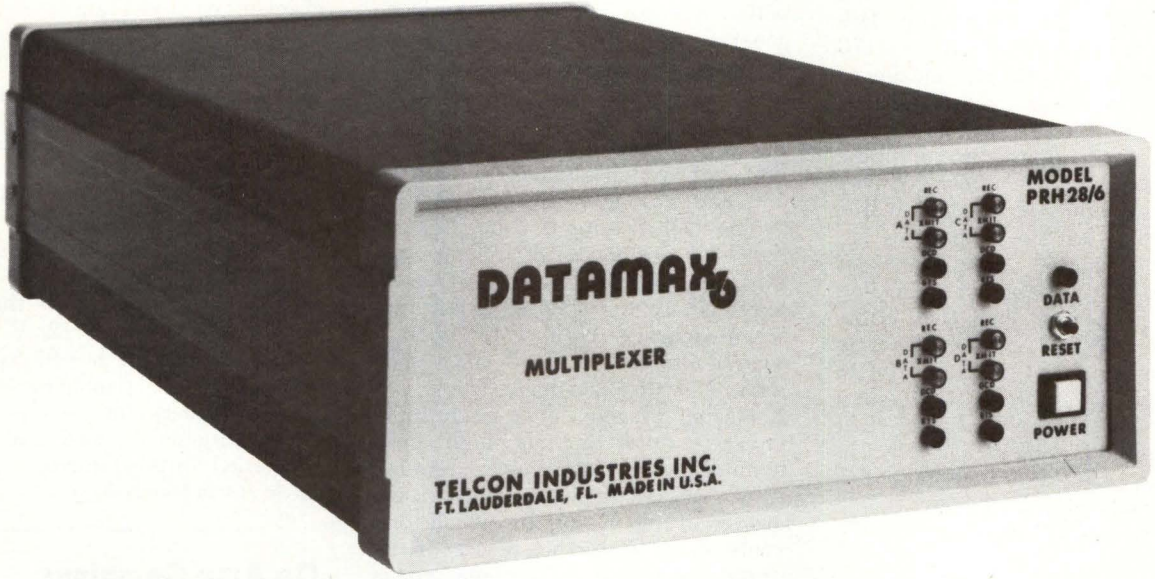
Inputs and output are fully TTL compatible. A 3-state output and on-chip address registers allow easy interfacing with microprocessor based designs. Two chip select inputs simplify system expansion. Other features include a 300-ns access time, high noise immunity, and 1024 x 1 organization.

The proprietary HD/CMOS process used in the design of the two RAMs includes 2-layer metal interconnects and silicon-nitride passivation. Packaged in plastic, CERDIP, and ceramic for commercial, industrial, and military environments, the memories are pin compatible with Intersil's IM6508 and IM6518. They are designed for applications requiring low power operations, high speed, and maximum reliability. The only functional difference between the two models is that the $\overline{CE}$, $\overline{CS}_1$, and $\overline{CS}_2$ inputs are internally connected in the 16-pin version, but not in the 18-pin DIP.

Circle 360 on Inquiry Card

The Squeezable One

DATAMAX PRH-28/6



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CIRCLE 97 ON INQUIRY CARD

14-Lead DIP Houses Bipolar Dc Motor Speed Control

Intended primarily for use with ac tachometer signals, a monolithic bipolar dc motor speed control is provided in a 14-lead plastic dual-inline package. Produced by Cherry Semiconductor Corp, 99 Bald Hill Rd, Cranston, RI 02920, the cs-175 is designed to provide maximum flexibility at lowest possible cost. Requirements for adjustment and external components in multiple speed applications have been reduced by giving accurate, pin programmable speed ratios for slow, medium, or fast motor velocities.

The unit is capable of providing a level of stability such that errors are dominated by terms created by the finite loop bandwidth needed to ensure stability with the dynamics of the specific motor and load. List price is $1.68 with a net cost in 1000-piece quantities of $0.79 and in 10,000 quantities of $0.65.

Circle 361 on Inquiry Card

12-Bit Storage Register D-A Converter Features Low Power Consumption

A complete 12-bit storage register DAC that combines low power consumption with 8- and 12-bit bus compatibility contains a precision ladder network, reference, switches, an output amplifier, and an input register. The DAC336B-12, fully processed to MIL-STD-883, Class B screening, and DAC336C-12, the standard commercial version, are produced by Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730, and are particularly recommended by the manufacturer for microprocessor applications.

Independent strobe inputs permit 4-, 8-, and 12-bit data input with full input storage or continuous conversion from digital codes to analog output. Proprietary laser trimmed, low drift, thin film nichrome resistor networks provide long-term stability.

Other features include a power disipation of 300 mW (typ), TTL and CMOS compatibility, and output capability of 0 to 10 V and ±10 V. Both models are specified from −55 to 125 °C. The devices are hermetically sealed in 24-pin DIPs.

Circle 362 on Inquiry Card

CMOS Divider Circuits Are Housed in 8-Pin DIPs

The RED series devices from LSI Computer Systems, Inc, 1235 Walt Whitman Rd, Melville, NY 11747, claimed to be the only divider circuits available in 8-pin dual-inline packages, directly accept slow edge or sine waves as well as square waves, to generate pulses from either 50- or 60-Hz input signals. Two members of the series are the RED 100/120, which divides by 100 or 120 and produces 1 pulse/2 s, and the RED 300/360, which divides by 300 or 360 and produces 1 pulse/0.1 min.

The versatile input capabilities of the CMOS devices result from a clock input shaping network. An enable input allows the counter to advance when signal is high, hold when it switches to low, and advance again when it switches to high. The device is cleared to zero by a reset input. Other features include high noise immunity and low power requirements, a square wave output, and an arrangement of pins which prevents damage if the device is inserted backwards. A single power supply is required for each of the dividers, with V_{DD} ranging between 5 and 15 Vdc. Circle 363 on Inquiry Card

Family of Programmable Bipolar Array Circuits Provide Logic Options

The first 9 of 15 arrays in a bipolar LSI programmable array logic (PAL) family, announced last year while undergoing sampling (see *Computer Design*, June 1978, p 180), are now available from Monolithic Memories, Inc, 1165 E Arques Ave, Sunnyvale, CA 94086. Each of the devices is to contain a programming network to interconnect gate arrays made up of AND/OR and AND/NOR gates, exclusive-OR gates, registers, programmable 3-state outputs, and feedback connections. They are designed to replace up to 90% of standard SSI/MSI (54/74 series) TTL and to reduce random logic chip count by a 4 to 1 factor.

The nine versions currently available consist of four AND/OR arrays (PAL10H8, 12H6, 14H4, and 16H2), four AND/NOR arrays (PAL10L8, 12L6, 14L4, and 16L2), and one AND/OR/NOR array, the PAL16C1. By blowing fusible links to configure AND and OR gates to perform a desired logic function, an engineer can govern the design of the chip. Complex interconnections, which previously required time consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype checkout or production.

Additional characteristics common to all of the devices include 25-ns propagation delay (typ), programming on standard P/ROM programmers, and packaging in 20-pin ceramic DIPs. Absolute maximum ratings require that, during operation, supply voltage (V_{CC}) not exceed 7 V, while input voltage and off-state output voltage must not exceed 5.5 V. During programming, all of these voltages are limited to 12 V. Storage temperature range is −65 to 150 °C.

Four of the remaining six chips are scheduled for second quarter 1979 introduction. The final two are scheduled for third quarter.

Circle 364 on Inquiry Card

Op Amp Combines High Slew Rate, Fast Settling Times

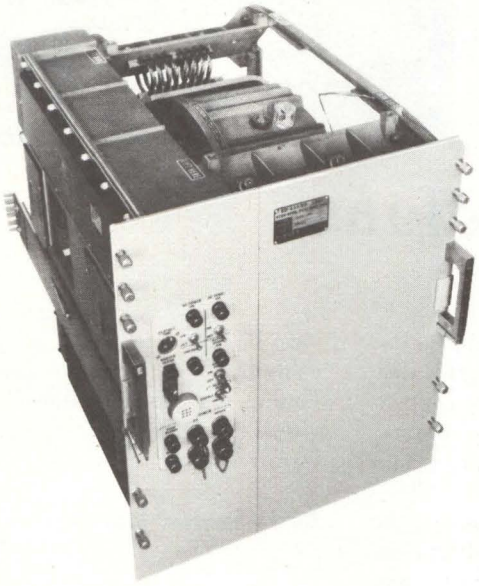
An operational amplifier, available in three models, provides a 200-V/μs slew rate and a settling time of 70 ns (0.1%, 5-V output step). This op amp family is designed to operate at gains ≥5, without requiring external compensation.

These differential amplifiers employ monolithic bipolar construction coupled with dielectric isolation. Parameters include a 150-MHz gain-bandwidth product and a 6.5-MHz full power bandwidth. Input characteristics include a 5-mV offset voltage and 15-nV/$\sqrt{\text{Hz}}$ input voltage noise.

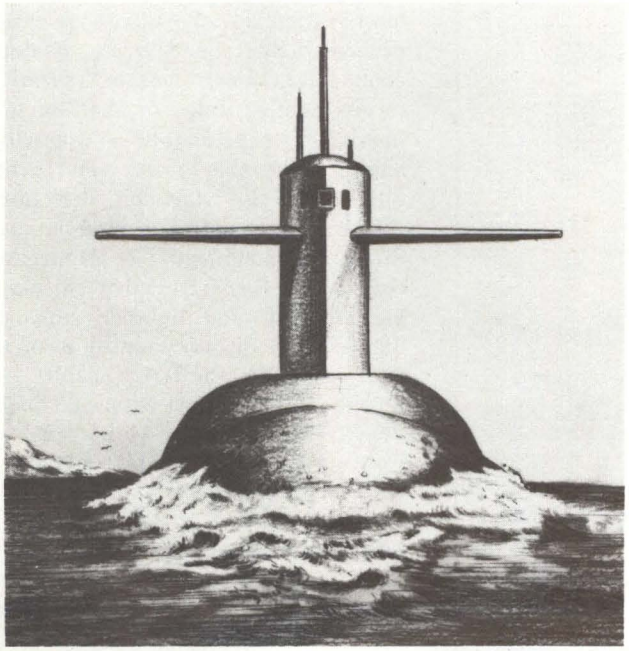
Produced by Harris Semiconductor Products, Div, PO Box 883, Melbourne, FL 32901, the high speed op amps are suited for use as output amplifiers for fast, precise DACs or as the amplifier components in high speed sample-and-hold circuits, as required in high performance data acquisition systems. Their wide bandwidth is appropriate to a variety of pulse and wideband video amplifier applications, including avionic and military equipment, oscilloscopes, and other types of graphic displays.

Circle 365 on Inquiry Card □

Librascope's RD-433 Militarized Mass Memory Goes Anywhere The U.S. Navy Goes.



THE dependable Mass Memory subsystem the ultimate in data reliability for shipboard and submarine installations to interface the Navy's standard computers. This specially configured model for the Shipboard Tactical Intelligence (TACINTEL) program is listed in the Navy's inventory under the military designation RD-433 (XG-1)/SSH. TACINTEL is one of the latest operational systems in the Fleet Satellite Communications (FLTSATCOM).



Installed in any compartment on board a ship, the RD-433 fits in an open standard 19″ Retma rack, meets MIL-E-16400, Class 4, operational requirements in free air ambient 0°C to 50°C, and withstands MIL-S-901C drop hammer shock. The system is also humidity and drip proof, and EMI/RFI secure without additional enclosure just as shown in the photograph.

Modularly designed for easy on-call maintenance, no preventative maintenance is required. The controller is made up of low-cost SEMS (the Standard Electronic Modules developed by NAFI), with low power Schotky integrated circuits.

Other production Mass Memories such as the Model CL107MA, are used in the Integrated Radio Room (IR^2) of TRIDENT submarines and in a new torpedo fire control system for the Royal Australian Navy. Librascope's mass memories are on board in many other U.S. Navy programs such as, for example, the prominently successful BQR-24 program.

Call or write today for additional information on these rugged, reliable Militarized Mass Memory Systems.

The Singer Company, Librascope Division, Department N, 833 Sonora Avenue, Glendale, California 91201. Telephone (213) 244-6541, extension 1891.

SINGER
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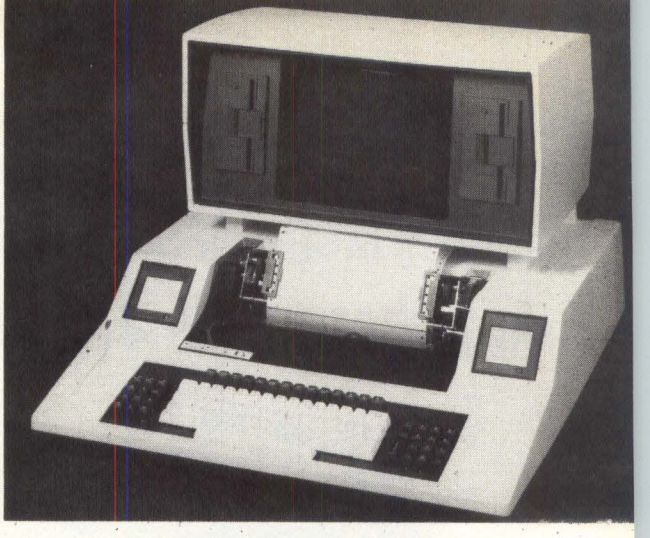
CIRCLE 98 ON INQUIRY CARD

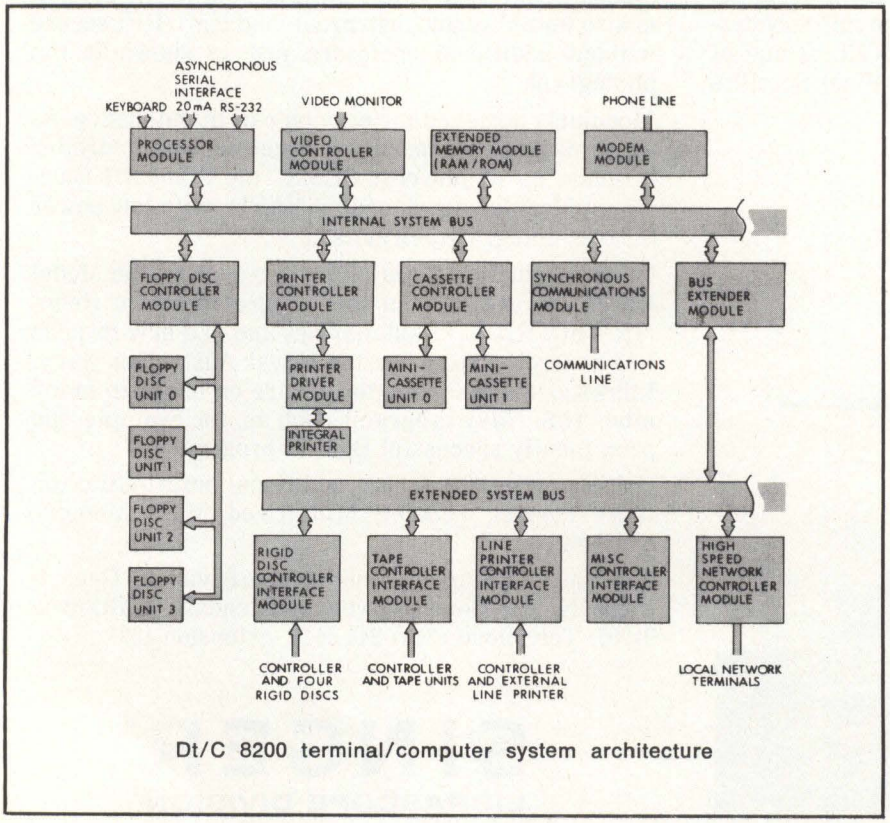
PRODUCT FEATURE



Desktop Computers Fit Broad Range of Applications

Whether configured as remote stations in a distributed processing network or as standalone systems, Solid State Technology's desktop Dt/C 8200 series terminal/computers provide large scale data processing capabilities. A basic system consists of processor, video controller, CRT display, keyboard, motherboard, and power supply modules. Optional modules include extended memory; line printer, one or two minicassette transports, up to four floppy disc drives, and up to four rigid disc drives, all with dedicated controllers; synchronous communications; high speed network controller; and modem.

Standard system software is the AMOS™ multitasking operating system with buffer pool device, and file managers. An Auto-SYSGEN™ program customizes the operating system by calling up separate device handlers for each of the self-contained optional peripherals. Faults are isolated down to individual modules by internal firmware/software diagnostics.



Dt/C 8200 terminal/computer system architecture

Basic System Hardware

Controlling device in the processor module is an 8085A microprocessor (3 MHz standard, 5 MHz optional). This module, in addition, contains 2k RAM, 12k ROM, CMOS RAM with battery backup (256 x 4, but software configured to appear as 128 x 8), 12 levels of vectored interrupts that are transparent to the user, keyboard interface, system bus interface, and audible alarm. An asynchronous communications interface offers RS-232-C and 20-mA current loop interfaces, keyboard selected programmable baud rate, modem control functions, separate transmit/receive rates, full- or half-duplex operation, selectable character length, selectable parity and stop bits, and false start bit detection.

The video controller module features an intelligent CRT controller chip with programmable display, custom font, and lightpen support. 4k x 16 of display/control RAM in two separate buffers enables a 2-page buffer space, with one page displayed while the other is in waiting. A total of 160 characters can be presented as full/half intensity, underline, inverse, blink, or transparent on the CRT display: 96 ASCII in a 7 x 7 format with lower case descenders, 32 control, and 32 graphic symbols.

Keys on the keyboard module are grouped in 4 clusters: full ASCII typewriter format board, 15-key numeric pad, 12-key editing pad, and 14 special function keys of which 8 are programmable. Integral LED displays indicate status of all mode select keys. N-key rollover ensures registration of each keystroke.

A motherboard module contains nine nondedicated logic module slots with 36-position dual-sided PC board edge connectors. Signal traces are routed above the groundplane. An optional expansion module provides additional module slots.

Power, supplied as 5, 12, and −12 V, is short circuit, thermal, and overvoltage protected. Full ac line filtering absorbs source voltage transient spikes.

Optional System Hardware

Dynamic RAM and ROM or EPROM are combined on a single module to allow extended buffering and use of high level languages such as BASIC, COBOL, FORTRAN, PASCAL, APL, and macroassembler. A total of 512k bytes of extended memory are available with an initial increment of 48k bytes of RAM and 2k or 4k bytes of ROM.

Printer module operations as well as diagnostics of both the 150-char/s printer and its controller are handled by a microprocessor and ROM firmware. Data are in parallel format.

Each minicassette controller, with its microprocessor and ROM firmware, handles either one or two transports. 128k bytes of data can be recorded on each minicassette at 800 bits/in (315/cm).

Up to four 5 or 8″ (13- or 20-cm), single- or double-sided floppy disc drives can be supported by a single controller. Recording is double-density IBM 3740 soft sector format. In addition, as many as four rigid disc drives and a dedicated controller can be added to the system. Fixed, removable, or a combination of media can be used for a possible maximum of 1.2G bytes.

Optional synchronous communications modules support SDLC, HDLC, ADCCP, DDCMP, and BISYNC protocols in addition to 2780/3780 emulation. A high speed network controller module can link a host terminal/computer to as many as 128 other terminal/computers at 300k baud.

As an option, a voice grade, low speed (up to 2400 baud) modem interfaces directly to the system bus. Full software control is provided of all modem functions. The phone line connects directly to the rear of the terminal/computer, without need for an acoustic coupler.

Standard System Software

The AMOS operating system requires only 12k of ROM, yet allows single files as large as 8M bytes and data bases as large as 1.2G bytes to be addressed. Existing utilities include multitask executive and executive support; memory, device, and file managers; file utilities; mode handler; command interpreter; and real-time clock.

Firmware/software diagnostics isolate faults down to individual modules. Under initiation of the processor module, tests are performed locally by intelligent controllers for all modules which have such controllers; for those modules which do not have dedicated controllers, the processor module carries out the diagnostics. Basic diagnostics are initiated automatically when power is turned on but more extensive diagnostics are user selected.

Tasks can be debugged while the remainder of the system is operational. The user can set multiple breakpoints anywhere within an object file and can single step, display or change registers, and look up any program location.

Specifications

Unit size is 20.25″ (51.4 cm) high, 27.4″ (69.5 cm) wide, and 27″ (68.6 cm) deep and it weighs 85 lb (38.6 kg). Electrical requirements are 117 Vac, 50/60 Hz, 5 A in domestic versions and 220 V, 3 A on export units. Operating temperature range is 40 to 90 °F (4 to 32 °C) at 90% humidity, noncondensing.

Price and Delivery

OEM unit price for a basic Dt/C 8200 terminal/computer in 100 quantities is $2475. First product units will be available in August. Solid State Technology, Inc, 17 Wheeling Ave, Woburn, MA 01801. Tel: 617/935-3910.

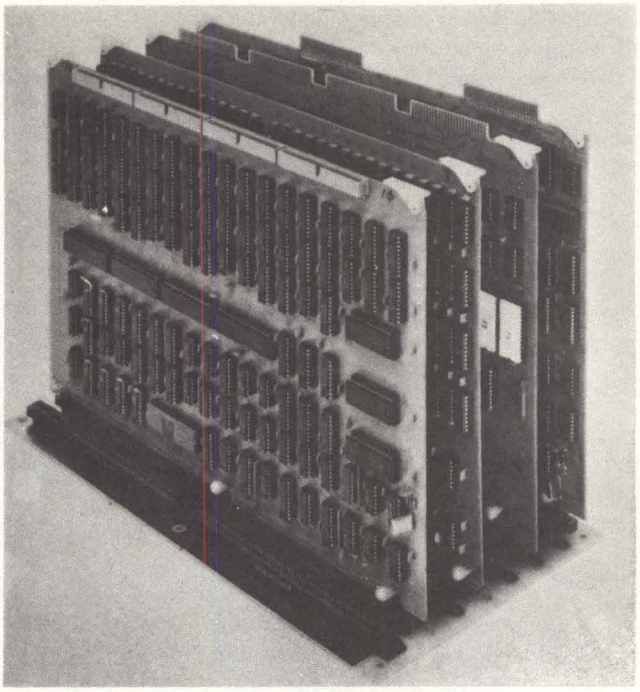
For additional information circle 199 on inquiry card.

PRODUCTS

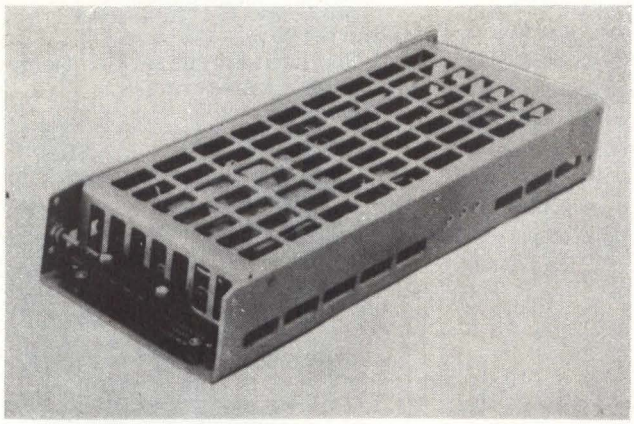
16-Bit Microprogrammable Minicomputer Accommodates 32 Timesharing Users

A multitasking computer capable of supporting up to 32 users, HEX-29 is based on a bipolar bit-slice processor that includes 16- or 32-bit integer and 64-bit floating point operations, multibyte/char string processing, and transition table instructions. It will accommodate bit, byte, word, double-word, quad-word, and variable field operations. High level instruction set offers optimum control of system power and speed. Basic machine cycle time is 160 ns, with many instructions operating in 2 machine cycles. Std system incorporates CPU card, EXEC card (operating system support with 8 RS-232 asynchronous ports), 94k bytes of memory, 0.5M bytes of floppy disc storage, high speed 64-bit floating point and 32-bit integer math, and compact cabinet with switching power supply, fan, and 8-slot motherboard. All systems include HOST operating system and BASIC+ language. System expands to include 1M bytes of CPU memory, 32 terminal ports, 4.8G char of disc storage, and any number of printers and terminals. **Digital Microsystems,** 4448 Piedmont Ave, Oakland, CA 94611.

Circle 200 on Inquiry Card



200-W Switching Power Supply Uses Direct Drive Circuitry

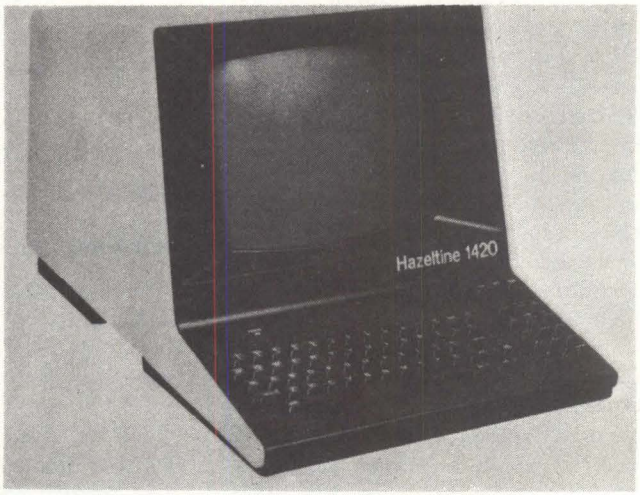


SK5-40/OVP, with dc output of 5 V at 40 A with 200-W max continuous output power, fits into a 5″ (12.7-cm) rack, measures 4.88 x 13 x 2″ (12.4 x 33.0 x 5.1 cm), and weighs 3 lb, 14 oz (1.74 kg). Direct drive circuitry eliminates starting bias, drive, and current sensing transformers, providing reduction in weight and cost, and more precise control, as well as a reduction in input to output noise coupling. Digital control feedback system uses pulse transformer to isolate the feedback loop, yielding exceptional loop stability and consistent performance to specs. Volt-second regulation maintains a constant volt-second product applied to power transformer under all ac conditions. Unit operates at 28 kHz. An antisaturation circuit continuously returns magnetizing current to zero, protecting the power transformer from accumulated residual magnetism, and eliminating the chance of burning out the switching transistors. **Power-One, Inc,** Power-One Dr, Camarillo, CA 93010.

Circle 201 on Inquiry Card

Computer Terminal Supports Data and Word Processing Software

Video terminal model 1420 features a typewriter style keyboard arrangement with both upper and lower case, making it suitable for fast, accurate entry with minimal operator training. It fills the need for a high quality, economy terminal that is compatible with data processing systems, including word processing applications, and is designed with user oriented features such as high intensity, blink, or nondisplay (zero intensity) modes. A program function key mode, as well as column and field tabs, are provided. An enhanced separate numeric key pad makes numeric entry faster. Cursor control keys, typamatic, and optional remotely controlled auxiliary EIA output are supplied. The unit operates with a std EIA RS-232 interface with 8 switch selectable transmission rates up to 9600 baud and accommodates all 128 ASCII codes. Characters are formed on the 12″ (30-cm) diag CRT screen using a TV raster scan technique with a 5 x 8 dot matrix char window. **Hazeltine Corp, Computer Terminal Equipment,** Greenlawn, NY 11740.



Circle 202 on Inquiry Card

Genisco High Resolution Displays.

Let us make your computer graphics 'crystal-clear'- fast!

Your future in graphics and image processing can't help being bright with all the Genisco Raster Display "good-omen" benefits going for you. Like ultra-high resolution, nanosecond processing, reliable performance, synergistic software, and modular architecture — that lets you quickly go "on-line" at minimal cost and expand as your needs dictate. Yet, with all this sophistication they're thin-pocket-book priced.

16K MOS/RAM Refresh Memories that go up to 1280 pixels/line X 1024 lines, in 16 gray scales, and 1024^2 full color versions. And, they're all directly addressable.

16-Bit User Programmable Graphics Processor lets you realize optimum operation with 150 ns cycle time manipulation, a set of 55 mnemonic instructions, automatic DMA access, selective erase, user selection from 4096 colors or 256 gray shades, and over 32 refresh memory planes control — using a unique "group select" method. We even offer a scroll and zoom, and a character/vector generator.

Versatile Output. Up to 12 monitors can be operated from a single system. TV/video mixing. Remote monitoring. RS232 ports. Automatic "Circumfill". These are but a smattering of the many advanced monitor control benefits offered by Genisco.

Full Complement of Interfaces for most popular minicomputers are available as standards, and we can economically fabricate a specific configuration where a stock unit won't do.

Flexible FORTRAN Software puts you "on-line" quickly, economically. Present offerings include a comprehensive set of Basic Graphics instructions, an efficient Cross Assembler, and our special GRAFPAC II package of FORTRAN callable subroutines — to simplify programming of your particular display configurations. With all this to back your display developments, a bright and 'crystal-clear' future is assured.

Contact Genisco, a name that has been synonymous with technology advances for more than 30 years, for all the particulars— and get a fast start on the path to good fortune.

GENISCO COMPUTERS

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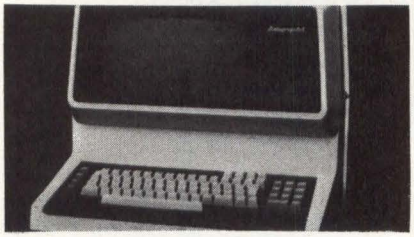
CIRCLE 100 FOR SALES CALL
CIRCLE 101 FOR LITERATURE ONLY

PRODUCTS

132-COL INTERACTIVE DISPLAY TERMINALS



The Charactron® CRT of the model 132-1 terminal handles 3168 char with a bright, high resolution, flicker free display of 24 lines plus a status line. An 11-key pad for numeric input, cursor controls with host sensing and addressing, 132 tabbing positions, dual intensity, and ASCII 96 displayable u/lc char set are also included. Unit eliminates the reprogramming and reformatting of 80-col terminals, as well as the generation of paper printouts. **DatagraphiX, Inc,** PO Box 82449, San Diego, CA 92138.
Circle 203 on Inquiry Card

MESSAGE SWITCHING MODULE AND TERMINAL CONTROLLER

Microprocessor controlled MSM provides multiplexing systems to handle remote data traffic. -L version, for low speed/volume traffic operates up to 8 lines at 75 to 9600 bits/s. Designed to handle large volumes of traffic between a limited number of stations, model -H processes up to 19.2k bits/s with EIA RS-232-C interface. Both models operate asynchronously or synchronously in full duplex. **DP Group,** 132 W 31st St, New York, NY 10001.
Circle 204 on Inquiry Card

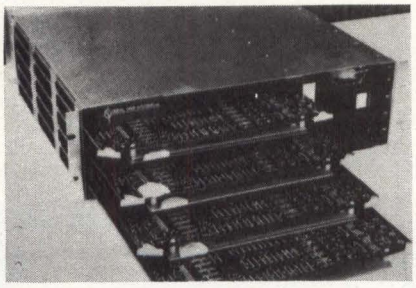
ALPHANUMERIC GAS DISCHARGE DISPLAY SYSTEM

SA-252 displays 16 char in a single line. Mounted on a 12 x 2 x 1″ (30 x 5 x 2.5-cm) circuit board, the assembly interfaces with TTL/MOS logic, and operates from a single 5-Vdc supply that draws 1.5 A (max). Input signals range from 0.8 V for logic 0 to 2.0 V for logic 1. The 14-segment format provides 63 char. Each is 0.55″ (14-mm) high and is displayed in a bright neon orange color, viewable from 40 ft (12 m) under normal conditions. **Beckman Instruments, Inc, Display Systems Div,** 350 N Hayden Rd, Scottsdale, AZ 85257.
Circle 205 on Inquiry Card

6500 BASED P/ROM PROGRAMMER

CSB 10 programmer card for Intel 2758, 2716, and 2732 UV EPROMs and compatible devices features gold-plated edge connector which adheres to the Rockwell System 65 bus std. Required voltages are derived from the 5 V supplied on the card edge connector. Programmer includes a zero insertion force socket for ease of EPROM insertion and removal. Model 10 may be used with other CSB modules, the Rockwell System 65 or AIM 65. **Compas Microsystems,** 224 SE 16th St, Ames, IA 50010.
Circle 206 on Inquiry Card

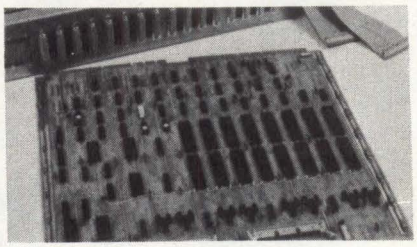
MEMORY EXPANSION SYSTEM



Self-contained memory expansion system houses up to 512k words x 20 bits of core or semiconductor memory. System, in rackmountable 5.25 x 10.5″ (13.34 x 26.7-cm) chassis, includes power supply and blowers. Memory unit features complete burn-in with optional interleave and word parity or error correction. Expansion chassis also houses necessary interface module. **Digital Data Systems Inc,** 1396 NW 65th Terrace, Plantation, FL 33313.
Circle 207 on Inquiry Card

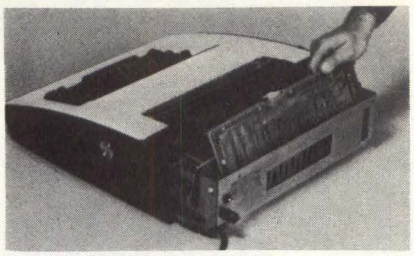
16-CHANNEL MULTIPLEXER

SMUX-16 controls full-duplex asynchronous communication on independent lines and is Data General 4060 software compatible. It requires no special chassis. Four boards may be used simultaneously for a max of 64 full-duplex lines; a secondary device code can be used for 64 more lines. Baud rates range from 75 to 19.2k. All 16 lines may use the same rate, or any combination may be selected. The board comes with 4, 8, 12, or 16 channels. **SOS Computer Systems,** 1900 N Canyon Rd, Provo, UT 84601.



Circle 208 on Inquiry Card

BUFFERED INTERFACE FOR DESKTOP TERMINAL

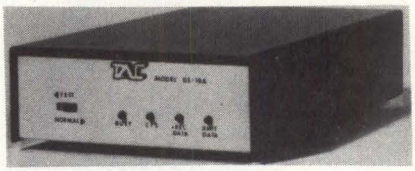


Tinybuffer 43, a smaller version of the 8k to 16k Telebuffer 43, supports offline entry and preparation of data for more efficient line and system utilization. Its RS-232-C interface connector makes it plug compatible with the Teletype 43. The board is also sensitive to std paper tape control codes received from downline for automatic send/receive operations. Both the 1k and 4k versions offer switchable speeds of 110 and 300 bits/s (strappable up to 9600 bits/s). **Edge Technology Inc,** PO Box 1387, Portland, OR 97207.
Circle 209 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEM FOR MICROCOMPUTERS

The MICRO/POWER™ series provides up to 250 W of regulated ac power to computers, and also filters incoming utility power. For uninterrupted power during power failures or brownouts, a 20-Ah, 12-V battery provides necessary power to maintain a computer for 15 min. Batteries may be connected in parallel for extended operation. Typ specs are 80% efficiency, ±10% line or load regulation, and ±0.5% line or load frequency regulation. **Nova Electric Manufacturing Co,** 263 Hillside Ave, Nutley, NJ 07110.
Circle 210 on Inquiry Card

SYNCHRONOUS DATA SET FOR LOCAL COMMUNICATION



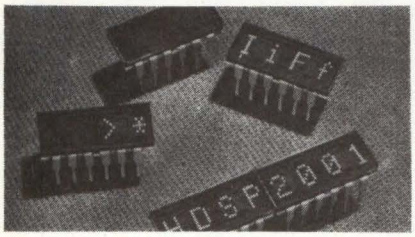
One model DS-10A data set with SYNC-1 plug-in synchronizer module, operating at data rates of 2.4k, 4.8k, 9.6k, and 19.2k bits/s, satisfies all local synchronous serial data communications needs. Switch selectable contention feature, Multishare, allows several terminals to share the same computer or multiplexer port without the use of a multipoint protocol. Operation is full- or half-duplex over twisted pair cables for up to 20 mi (32 km). **Telecomm-Automation Corp,** Box 283, Newtown, CT 06470.
Circle 211 on Inquiry Card

COLOR GRAPHICS MANAGEMENT SYSTEM

Using an active pen and digitizer tablet, system reduces time required to draw original artwork or to trace drawings. Corrections and changes can be made through software editing routines. A drawing in process is displayed on a 512 x 512 resolution 13" (33-cm) color CRT screen. Completed images can be stored on the integral dual floppy disc, or reproduced on paper or transparencies with Xerox 6500 color graphics printer. Supplied Microsoft BASIC eases chart and graph programming. **Chromatics Inc,** 3923 Oakcliff Industrial Ct, Atlanta, GA 30340.

Circle 212 on Inquiry Card

YELLOW ALPHANUMERIC LED DISPLAY

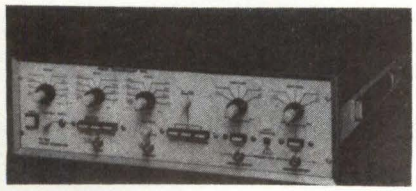


Applications requiring small size and prohibiting the use of red displays will profit from the HDSP-2001. It may be used in bright ambient light with appropriate filtering. Each char is formed with a 5 x 7 dot matrix, capable of displaying the full ASCII code, u/lc letters, punctuation marks, math and other symbols, and numerals. Each TTL compatible, 4-char package measures 17.7 mm long x 7.25 mm high. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 213 on Inquiry Card

INTERMEDIATE POWER PULSE GENERATOR

Solid state model PG-75A provides dual 1.5- to 50-V outputs and wide control ranges together with 100% duty cycle capability and 10-ns rise/fall times. Frequency ranges from 0.1 Hz to 10 MHz; std pulse widths at full output power vary from a min of 30 ns to 2 s. Double pulse mode of operation allows the operator to attain an effective pulse repetition rate of 20 MHz, without restriction of pulse amplitude. **Pulse Technology, Inc,** 15823 S San Pedro St, Gardena, CA 90248.



Circle 214 on Inquiry Card

PRODUCTS

FULL CHARACTER LINE PRINTER

The QUIET 300 uses a Teletype® model 40 print mechanism, which is a heavy duty, line at a time, hard-copy impact printer. It prints on up to 6-part forms. The 80-col unit offers either friction or tractor feed, while the 132-col unit offers tractor feed. It can print 300 lines/min with the ASCII 63-char set and 500-lines/min with the 48-char set. The parallel interface is Centronics or Dataproducts compatible. **Local Data Co,** 2741 Toledo St, Suite 214, Torrance, CA 90503.
Circle 215 on Inquiry Card

PASCAL FOR PROCESS CONTROL COMPUTERS

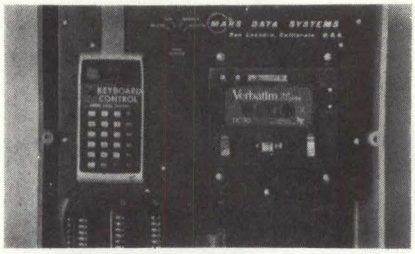
PascalPac operating system supports a Z80 macroassembler, PASCAL compiler, BASIC compiler, and a Link Editor with extensive library capabilities. Interactive text editor is provided for preparing programs and documentation, and a Filer allows creation of named files of multiple data image types plus directory creation and maintenance. **Process Computer Systems, Inc,** 750 N Maple Rd, Saline, MI 48176.
Circle 216 on Inquiry Card

300-LINE/MIN PRINTER FOR 3270 SYSTEMS

Using Printronix 300 printer with a built-in interface, model PR-300 is plug compatible with IBM 3271, 3273, and 3274 (Type B) control units. In addition to high speed conventional character output, it offers optional large character printing, bar codes, and scannable character print (OCR). A companion model, PR-150, offers the same capabilities and options, but operates at 150 lines/min. **Interface Systems, Inc,** 462 Jackson Plaza, Ann Arbor, MI 48103.
Circle 217 on Inquiry Card

REMOTE SITE DATA ACQUISITION TERMINALS

Integral microprocessor and realtime clock control DAT-2/3 reading and recording of up to 64 analog and 8 digital event-type inputs. Data are stored in memory until unit is instructed to process or transmit data to central site via phone, radio, or dedicated wire link. Philips type cassette provides mass storage. Weather proof enclosure affords −25 to 70 °C, 100% humidity operating conditions. CMOS logic permits battery operation for primary or backup power. **MARS Data Systems,** 5191 N Douglas Fir Rd, Calabasas, CA 91302.



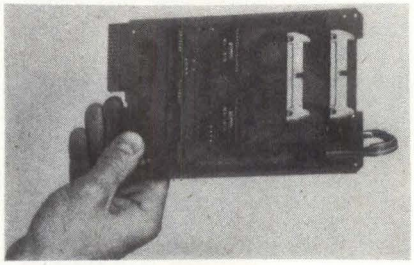
Circle 218 on Inquiry Card

4-CHANNEL LOCAL COMMUNICATIONS INTERFACE

QALTA, a quad asynchronous local terminal adapter, replaces Interdata single-channel adapters. Four full- or half-duplex channels operate from 50 to 19.2k baud. Fully compatible with PASLA, PALMS, and other adapter channels, the half-board adapter requires only 2.5 V for all 4 channels. Two control lines plus transmit and receive lines are provided for each channel interface. **Macrolink,** 1740-E S Anaheim Blvd, Anaheim, CA 92805.
Circle 219 on Inquiry Card

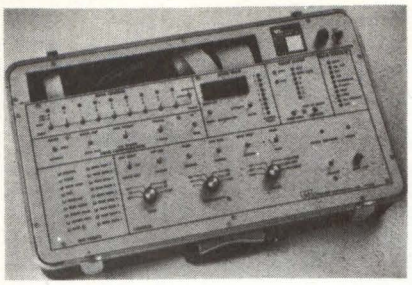
PERIPHERAL A-D EXPANDER BOARDS FOR LSI-11

ST-LSI-ADX allows system expansion up to 32 differential or 64 single-ended channels, when used with ST-LSI A-D/D-A master control oards. Slave cards slide into and interface directly with LSI-11 bus. Master-slave card pairs may be linked together for indefinite channel expansion as long as sufficient additional card slots and power are available from bus. Each board features multiplexer crosstalk from off channels of 0.01%, ranging from dc to 1 kHz. **Datel Systems, Inc,** 11 Cabot Blvd, Mansfield, MA 02048.



Circle 220 on Inquiry Card

MAGNETIC TAPE DRIVE EXERCISER



Digital readout of speed in inches/second and digital skew in microinches for forward/reverse tracking alignment plus tests for intermittent errors or permanent malfunctions are capabilities of TX-1200 exerciser for 6.25- to 125-in/s (15.88- to 318-cm/s) mag tape drives. Attache-case mounted exerciser weighing less than 20 lb (9 kg) performs both programmed exercise testing and specific function troubleshooting of all drive functions. **Wilson Laboratories, Inc,** 2237 N Batavia St, Orange, CA 92665.

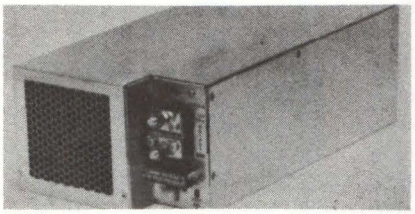
Circle 221 on Inquiry Card

MULTISPEED BAUD RATE CONVERTER

For use primarily with Bell (WECO) 212A (or compatible) dual speed modems that operate at speeds up to 300 or 1200 baud, the rackmounted BRC system allows computer dial-up ports to be configured for any 2 std baud rates rather than the typ single baud rate. No hardware or software changes to the computer system are required; speed recognition is automatic. All ports operate at both selected rates. **Link Communications,** Suite 1040, 36 S State St, Salt Lake City, UT 84111.

Circle 222 on Inquiry Card

COMPACT 1-kW SWITCHING POWER SUPPLIES

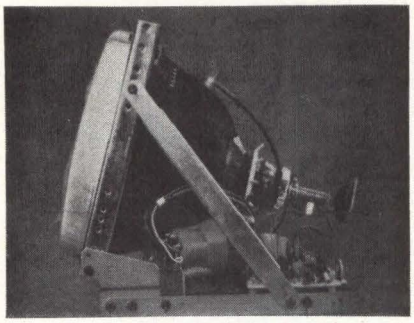


Providing wide range brownout capability with ac inputs of 184 to 250 Vrms, single-output model PM2499 supplies regulate through line dips to 140 V and offer extended holdup of up to 60 ms at low line. Standard dc outputs range from 2 to 48 V, with 5 V at 200 A typ. MTBF exceeds 100k hours. Std features include overload, short circuit, and reverse voltage protection on the output; and automatic overtemperature shutdown and overvoltage protection. **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.

Circle 223 on Inquiry Card

PRODUCTS

VIDEO DISPLAYS



CRTs incorporated in displays measure 12″ (30-cm) diag and feature 90° deflection and 12.5-kV nom high voltage at 50-μA beam current. P4 phosphor is std; other EIA phosphors and bonded antireflective face plate are optional. D12 series have 900 lines min resolution at center of display with less than 25-ns pulse rise time for 30-V rise at CRT. Other features include TTL level inputs, and interconnection via 10-pin edge connector. **Zenith Radio Corp,** 1000 N Milwaukee Ave, Glenview, IL 60025.
Circle 224 on Inquiry Card

SYNCHRONOUS/ASYNCHRONOUS CONVERSION INTERFACE

Synchronous/asynchronous AS1 allows a full-duplex terminal high speed access to a computer via 2-wire dial-up telephone lines. The device performs the sync/async conversion and interfaces to synchronous modems (Bell 201 or 208). Data rates of 1200, 2000, 2400, 4800, and 9600 baud are supported. Indicator lights are provided for input data, output data, and power. XON/XOFF protocol and transmission error detection and retransmission are available. **Communications Interface, Inc,** Box 2320 Loop Sta, Minneapolis, MN 55402.
Circle 225 on Inquiry Card

RS-232 MOLDED CABLE ASSEMBLIES

Available in std 10, 15, 25, 50, and 70′ (3, 7.6, 15, and 21-m) lengths, series uses UL listed 25-conductor cable that passes the FR-1 vertical flame test. Cable construction employs 22-gauge stranded tinned copper conductors, color coded PVC insulation, and overall 0.370″ (9.398-mm) dia chrome PVC jacket. Cable specs include a nom capacitance of 35 pF/ft (10.6/m) and a suggested max working voltage of 200 Vdc. **Belden Corp, Electronic Div,** PO Box 1327, Richmond, IN 47374.
Circle 226 on Inquiry Card

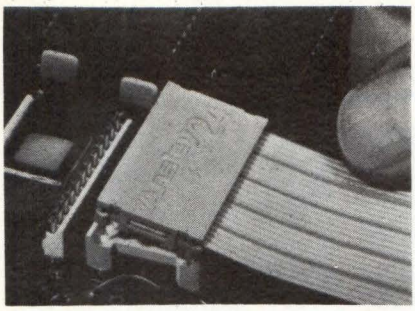
COMPACT PANEL INDICATOR LIGHTS

Recommended panel cutouts for lights are 1.08 x 0.48″ (2.74 x 1.22 cm). Snap-in panel mounting allows for ease of installation. 0.25″ (0.64-cm) slip-on type terminals also allow soldering. Lenses are available in white, red, clear, amber, green, and blue. Lamps are neon or incandescent. Custom lamps, hot stamping, and metal bezels are available. Series matches 16X and 171 series rocker and paddle switches. **Chicago Switch, Inc,** 1714 N Damen Ave, Chicago, IL 60647.
Circle 227 on Inquiry Card

SOFTWARE UTILITY FOR MASS STORAGE SYSTEM

Designed to manage data sets automatically in a hierarchical information storage environment, Storage Management System software provides automatic migration and backup of disc data sets to 38500 Mass Storage System, and from mass storage to 0.5″ (1.3-cm) magnetic tape under predefined, user specified criteria. Instead of copying an entire disc pack to tape to record the changed data, the system provides for automatic backup of only those data sets in which recorded information has changed. **Control Data Corp,** Box O, Minneapolis, MN 55440.
Circle 228 on Inquiry Card

LOW PROFILE 40-POSITION DIP PLUG CONNECTOR



Specifically for microprocessor board applications utilizing DIP sockets on 2.54 x 15.24-mm grids, the BLUE MACS® 40-pin connector employs heavy duty pins for extra strength, especially in situations where constant insertion and extraction are required. Primary use is as a disconnectable interface with DIP sockets. The line includes 24- and 40-position plugs in heavy duty versions only, and 14- and 16-pin versions with both std and heavy duty contacts. **T&B/Ansley Corp,** 3208 Humboldt St, Los Angeles, CA 90031.

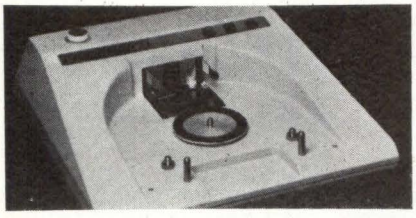
Circle 229 on Inquiry Card

BRIGHT RED AND YELLOW T-¾ LED LAMPS

Added to LLL Mini-LED series, lamps have a fully illuminated lens dia of 0.090" (2.3 mm), overall lens height of 0.150" (3.8 mm), and base flange dia of 0.120" (3.1 mm). LLL-39-1 yellow and 49-1 red illuminators with transparent tinted lenses provide an intense light source, ideal for back lighting. LLL-37 yellow and 47 red indicators are supplied with diffused tinted lenses for contrast and off axis visibility in high amb lighting situations. Luminous intensity ranges from 4 to 12 mcd at a forward current of 25 mA. **OPCOA, Div of IDS Inc,** 330 Talmadge Rd, Edison, NJ 08817.

Circle 230 on Inquiry Card

DISC CARTRIDGE CLEANERS



Model 9100 for front loading cartridges and 9200 for top loading cartridges remove dirt, dust, cigarette smoke particles, paper bits, and oxide redeposits, leaving no residue, in less than 3 min. The cartridge to be cleaned is inserted into the 24 x 24 x 9" (61 x 61 x 23-cm), 23-lb (10-kg) cleaner and the operator pushes the process button. The unit shuts off automatically when cleaning is completed. **3M Co, Data Recording Products Div,** PO Box 33600, 3M Center, St Paul, MN 55133.

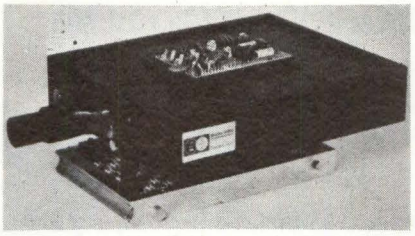
Circle 231 on Inquiry Card

DATA COMMUNICATIONS LINE MONITOR

When placed in series with a std data cable, model 20 provides 25 test points, clearly marked and numbered, in the form of 0.025" (0.064-cm) sq pins. All pins and data connectors are mounted in a small rugged aluminum housing. Two jumpers allow the loopback function to be implemented anywhere on a std EIA RS-232-C data path, and also provide a single means of connecting an LED probe or oscilloscope to the test points for diagnosing data communications problems. **Remark International,** 4 Sycamore Dr, Woodbury, NY 11797.

Circle 232 on Inquiry Card

PCB TEST FIXTURE

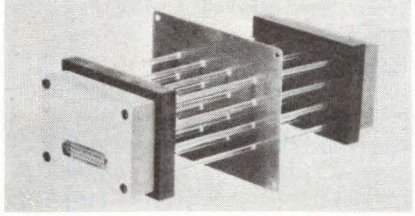


Featuring a solid pin and predrilling for easy pin addition, CheckMate is adaptable to all tester interface methods. The 1-piece solid test pin has very low contact resistance; 2-point pin guiding leaves only a small part of the pin exposed. Pilot holes are predrilled for every component pad location. Extruded aluminum frame and swing away feature allow pin and wiring additions to be done with the fixture still in place on the test system. **Qual-Pro Corp,** 22541 S Normandie Ave, Torrance, CA 90501.

Circle 233 on Inquiry Card

LOW COST OPTICAL COUPLING MODULES

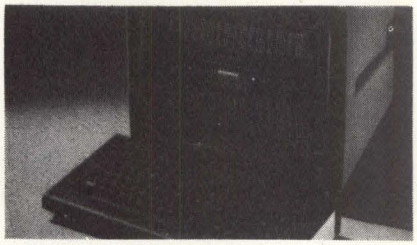
Modules increase transient noise suppression by 103 dB for single-channel, 87 dB for 8-channel, and 75 dB for 16-channel versions when compared to commercially available single-chip isolators. Units feature TTL, CMOS, and switch sensing input signals; TTL, CMOS, and relay driver output signals. Coupling capacities are 4 x 10^{-6} pF for single-channel, 2.5 x 10^{-5} pF for 8-channel, and 1 x 10^{-4} pF for 16-channel modules. Voltage isolation is 30 kV in 6" (15-cm) module. **Precision Instruments,** 9920 Trumbull, SE, Albuquerque, NM 87123.



Circle 234 on Inquiry Card

PRODUCTS

Z80 BASED 3200-CHAR DISPLAY TERMINAL



Displaying 40 lines of 80 char on a 15" (38-cm) nonglare screen, model 4080-COMPAT is software compatible with the TTL based K4080D terminal. Std features are 7 x 7 dot matrix u/lc char formed in a 10 x 10 dot field; blink, dim, and reverse-video accent char; and blinking field cursor. Detachable keyboard with 72 keys, separate numeric pad, and separate cursor control keys generates full 128-char ASCII set. **Ann Arbor Terminals,** 6107 Jackson Rd, Ann Arbor, MI 48103.

Circle 235 on Inquiry Card

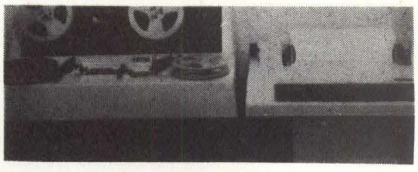
DISTRIBUTED DATABASE SOFTWARE FOR SERIES/1

Machine-independent modular CDPS software is an adjunct to the Series/1 minicomputer. Package incorporates a database manager, menu system, program language, screen handler, procedure control, communications, bisynchronous communications control, and utilities, all running under an operating system. Programs written using the system can run on 360, 370, DOS/VS, OS/VS, or Series/1 without modification. **Tominy Inc,** 4152 Crossgate Dr, Cincinnati, OH 45236.

Circle 236 on Inquiry Card

TAPE PREPARATION SYSTEM MULTITASKING CAPABILITY

A flexible diskette option to the existing MPS-2000 tape system adds multitasking capability. The operator can go directly from keyboard to diskette to communications with a central site computer, back to diskette, and then to punch, generating a near-perfect tape on the first pass. The diskette allows simultaneous operations, correction of errors, and a solution to tape storage problems. All commands are from the keyboard. **Radian Corp, Unitech Products,** 1005 E St Elmo Rd, Austin, TX 78745.



Circle 237 on Inquiry Card

ULTRA HIGH DENSITY GCR MAGNETIC TAPE SYSTEM

Model 6250 improves system performance by providing 6250 bits/in (2461/cm); enhanced tape capacity of IBM/ANSI compatible GCR provides 3:1 file compaction. The system consists of 1 to 4 tape transports, an expandable formatter/controller to control up to 4 tape transports simultaneously, and a half-board host adapter that plugs into selector channels of a Perkin-Elmer/Interdata computer. Auto thread/load and self-contained takeup reel are std. **California Minicomputer Systems,** 605 N Nash St, El Segundo, CA 90245.

Circle 238 on Inquiry Card

DATA TRANSACTION TERMINAL

Vutran, designed for short inquiry/response data applications, uses microprocessor technology in a housing not much larger than a telephone set to provide 300-baud ASCII data transmission. Prompting indicators on the 16-char LED display, 10 numeric and 10 function key keypad, and ABA Track II magnetic stripe reader are provided. Up to 452-char RAM are partitioned into max of 254 char for transaction data, 89 char for protected data, and 109 char for telephone number storage. **The Computer Communications Group,** 12th Floor, 160 Elgin St, Ottawa, Ontario K1G 3J4, Canada.

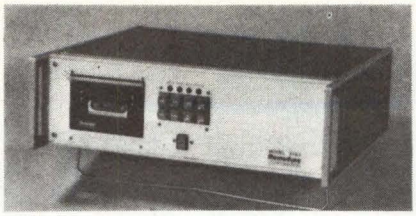
Circle 239 on Inquiry Card

SYNCHRONOUS SHORT HAUL MODEM

Model LDS 329 operates at 2400, 4800, or 9600 bits/s over dedicated 4-wire unloaded lines up to 8 mi (13 km) and requires no dc continuity. Unit meets Bell Spec 43401 and is functionally and line compatible with the company's RM 3309 rackmounted digital data set. Features include front panel indicators for power, test, marginal channel, receive carrier, receive data, and transmit data. Enclosed, self-powered unit is fully protected against line transients and conforms to EIA RS-232-C and CCITT V.24. **Gandalf Data, Inc,** 1019 S Noel, Wheeling, IL 60090.

Circle 240 on Inquiry Card

VERY HIGH SPEED CASSETTE RECORDING SYSTEM



Model 3783HV, oriented toward frequent program loading, has a cassette loading rate of 9600 baud with min tape wear. Compatibility between recorders allows tapes recorded on one system to be read by any other with equal reliability. Resistance to tape imperfections and environmental emi is assured. Specs include RS-232-C serial input format with ±5 V, RS-232-C serial output format with ±12 V, and capacity of >150k bytes. **Memodyne Corp,** 220 Reservoir St, Needham Heights, MA 02194.

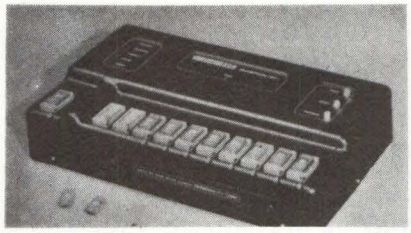
Circle 241 on Inquiry Card

FAST LINEAR TAIL PULSE GENERATOR

A 3-ns risetime, min pulse duration of 5 ns, and 1% linearity and stability are features of the calibration pulser. Variable output pulse risetime, falltime, amplitude, and duration allow the model BL-2 to simulate outputs and to check linearity, pulse pair resolution, and effects of risetime, count rate, and overloads. Pulse shape can be either a tail pulse or a flat top pulse, with repetition rates as high as 50 MHz (100 MHz in the double-pulse mode). **Berkeley Nucleonics Corp,** 1198 Tenth St, Berkeley, CA 94710.

Circle 242 on Inquiry Card

10-COPY EPROM PROGRAMMER



Benchtop PEP 1 fully programs from 1 to 10 EPROMs in ≤4 min, with 3 personality cards handling commercially available NMOS EPROMs. The programmer conducts an automatic system and device check, programs the devices, and then verifies; throughout these sequences it buffers the master EPROM against damage. An LED and audible tone indicate pass/fail. The unit programs from master EPROM, the company's Pseudo P/ROM module, or external reader using hexadecimal paper tape. **ITT Components Group,** 1551 Osgood St, North Andover, MA 01845.

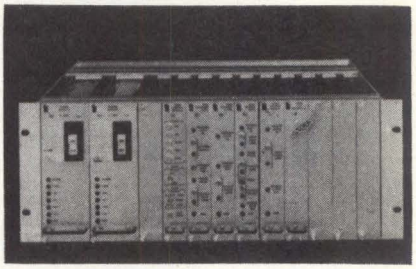
Circle 243 on Inquiry Card

PRODUCTS

PLOT COMPRESSION FOR REMOTE VECTOR PROCESSOR

Remote spooling vector processor (RSVP™), an electrostatic plotting system with remote entry capabilities emulating IBM 2780/3780 terminals, supports an algorithm that compresses data in both X and Y directions. The raster compression algorithm reduces data transmission time by as much as 4:1 for dense drawings [20k or more vectors/ft² (222k/m²)]. Transmission time for plots in the 3k to 10k vectors/ft² (33k to 111k/m²) range show a 2:1 improvement. **Versatec, a Xerox Corp,** 2805 Bowers Ave, Santa Clara, CA 95051.
Circle 244 on Inquiry Card

T1 DATA SET

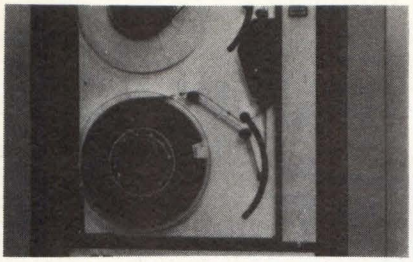


High speed data are accepted from a business machine and output at 1.544M bits/s for transmission over T-carrier facilities using the 306 data set. As a full-duplex device, it also accepts a T-carrier signal and delivers data and clock to the business machine. To match IBM 2701 type interface, clock and data interfaces are CCITT V.35, and control interfaces are RS-232-C. The set operates with either internal or external clock and features built-in loopback. **Telecommunications Techniques Corp,** 112 Frederick Ave, Rockville, MD 20850.
Circle 245 on Inquiry Card

PREPROCESSOR FOR FORTRAN IV

Program development can be pursued at 2 levels using the structured language preprocessor that is available on disc for the company's disc system with 2 drives and 48k of memory. It receives, as input, a program written in RATFOR and outputs a program written in the company's FORTRAN IV, which can be compiled with their FORTRAN compiler. The FORTRAN output features comments that are indented according to the RATFOR structure in which they are included. **Cromemco, Inc,** 280 Bernardo Ave, Mountain View, CA 94043.
Circle 246 on Inquiry Card

0.5" MAG TAPE SYSTEMS FOR HP DESKTOP COMPUTERS



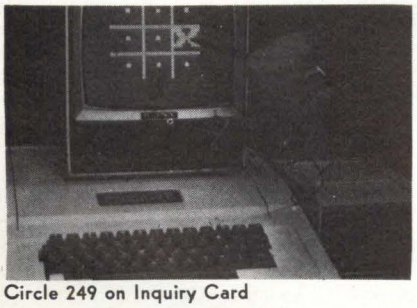
Electrical, physical, and logical plug compatibility is achieved between the series 2000/9000 tape systems and HP 9800 series, HP 250, and HP 300 computers. A microprocessor permits the IBM/ANSI compatible system to be added through the HP-IB I/O. Controlling up to 4 tape drives, the intelligent controller performs all programming, free formatting, and error detection with automatic correction. Included are dual 2048-byte buffers and 7- or 9-track R/W. **Dylon Corp,** 3670 Ruffin Rd, San Diego, CA 92123.
Circle 247 on Inquiry Card

HALF-BOARD UNIVERSAL LOGIC MODULE

Interfacing Interdata computer with a peripheral device, module features switch selectable 10-bit device address, 16-bit input register, 16-bit output register, and 42 12-, 16-, and 18- to 40-pin IC positions for user designed logic. The bus side provides device addressing, handshake, and status and interrupt control to multiplexer or selector channel bus, plus the 16-bit I/O registers. User side contains the IC positions for user designed logic. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.
Circle 248 on Inquiry Card

LOW COST LIGHTPEN FOR APPLE II COMPUTER SYSTEM

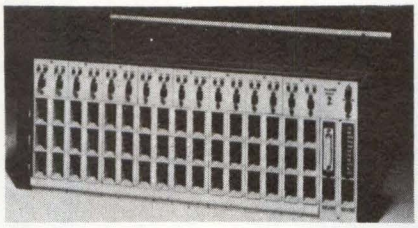
For applications such as bar graphs, charts, and games, the Apple II lightpen is supplied with 3 cassette demonstration programs that aid in developing BASIC programs to drive the pen. The Pointer software driver performs 7 functions which include selection of graphics mode and page 2 display, search for X and Y ordinates, a test for odd/even Y ordinate, set page 1 display, and return to calling program. **Programma International, Inc,** 3400 Wilshire Blvd, Los Angeles, CA 90010.



Circle 249 on Inquiry Card

PATCHING, MONITORING, AND FALLBACK SWITCHING UNIT

Unit manages EIA RS-232/CCITT V.24 digital data channels between modems and terminals or computer ports. Patch cords breaking the normal-through connections crosspatch terminals and modems to different channels. Push-button single-channel or group fallback switching instantly changes over between online and standby equipment. Noninterrupting monitoring permits patching of signals to a 25-pin test equipment connector or to an LED status indicator panel. **Dynatech Data Systems,** 7644 Dynatech Ct, Springfield, VA 22153.

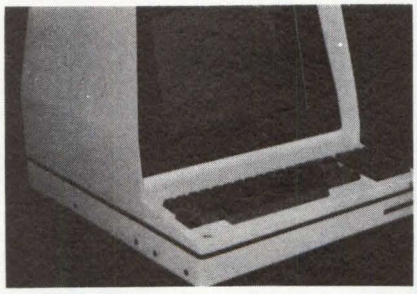


Circle 250 on Inquiry Card

DISC BASED REMOTE BATCH TERMINAL

Extended capabilities of expanded memory, local batch processing, COBOL, and sort-merge characterize the 1630 system that can be configured with the company's 1600-02 model II processor, and their IBM 3741 or 5230 emulators. Support of up to 128k of high speed MOS memory permits max concurrent processing. Extended Communications Operating System (ECOS) control provides the terminal's multiprogramming functions. **Harris Corp, Data Communications Div,** 16001 Dallas Pkwy, Dallas, TX 75240.
Circle 251 on Inquiry Card

CRT TERMINAL REPLACEMENT FOR VT52

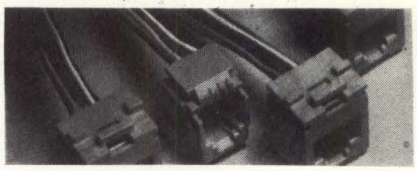


Monarch-52 replaces the DEC VT52 CRT terminal with no software changes. 1920 5 x 7 dot matrix char are displayed in 24 lines of 80 char on the 12" (31-cm) diag screen. Features include direct cursor addressing, selectable baud rates from 75 to 9600, extended ASCII code, and EIA interface. Audible signals are bell and selectable key-click. Terminal requires 115 V, 60 Hz at 100 W or optional 230 V, 50 Hz. **Dataview, Inc,** 23A Dana St, Malden, MA 02148.
Circle 252 on Inquiry Card

PRODUCTS

FCC-STANDARD JACKS FOR INTERCONNECT DEVICES

The 285 series jacks that conform to FCC Docket #19528 are available in 8-position keyed, nonkeyed, and series models, plus a 6-position model. Jacks are furnished with color-coded, PVC-insulated, 26 AWG solid wire leads in 4 termination styles: stripped ends only, spade lugs, ring lugs, and taper pins. Std wire length is 6" (15 cm), std body material is Cycolac ABS. Contacts are 50-μin (1270-μm) gold-plated on a phosphor-bronze base. **Amphenol North America Div, Bunker Ramo Corp,** 2122 York Rd, Oak Brook, IL 60521.



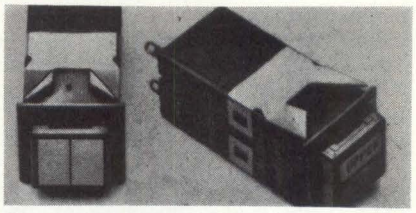
Circle 253 on Inquiry Card

DISC SUBSYSTEM FOR NOVA MINICOMPUTERS

IBM Winchester technology disc subsystem, the Cruise 1, features 62M-bytes online storage, less than 50-ms full stroke positioner time, and less than 7-ms single-track positioning. Designed to operate on Data General Novas, the subsystem's controller requires only 1 slot in computer chassis, and can be cabled to up to 4 disc drives. System is fully software compatible with Data General RDOS. **Computer Business Systems, Inc,** 167 Moore Rd, East Weymouth, MA 02189.

Circle 254 on Inquiry Card

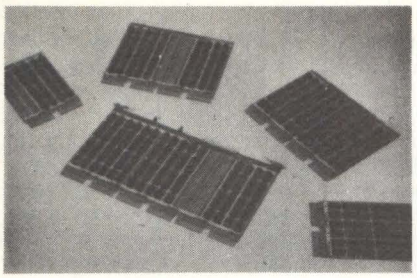
SPLIT SCREEN PUSHBUTTON SWITCHES



Horizontally (330 series) or vertically (331 series) split display dual-lamp pushbuttons use two 5- to 28-V T-1¾ lamps that can be energized together or separately. Caps are available with engraved legends on black or white fill, or on film legends readable when lamp is on, or when it is on or off. Lens options are colorless, or transparent or translucent in 1 of 7 colors. Filters can be provided for either or both lamps. **Dialight, A North American Philips Co,** 203 Harrison Pl, Brookline, NY 11237.

Circle 255 on Inquiry Card

UNIVERSAL WIREWRAP MODULES



Universal rows of the series 2040 high density wirewrap module accept any size IC. Quad modules accommodate up to 72 16-pin or 84 14-pin ICs. Dual and hex heights are also available. Low profile sockets and wirewrap pins permit board-to-board insertion on standard 0.5" (1.3-cm) slot spacing. Wirewrap pins are inserted in all IC positions and I/O locations; 0.100" (0.254-cm) pin geometry permits use of automatic wirewrapping techniques and 0.300" (0.762-cm) pin height allows for 2 levels of #30 AWG wraps. **Gen/Comp Inc,** 6 Algonquin Rd, Canton, MA 02021.

Circle 256 on Inquiry Card

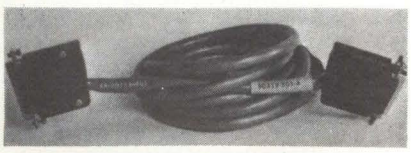
IMPACT DOT MATRIX PRINTER/PLOTTER

T-100 utilizes raster matrix technology to plot at 15 in(38 cm)/min with a dot density of 100 dots/in (39/cm) on std fanfold paper. Forms are accommodated from 4 to 16" (10 to 41 cm) wide and up to 6 parts. Printing speed is 250 lines/min with a std 96-char set. The plotter interfaces with Printronix plot software and has plug compatibility with Printronix, Centronics, and Data Products printers. Other features are underlining and double high char. **Trilog, Inc,** 16705 Hale Ave, Irvine, CA 92714.

Circle 257 on Inquiry Card

COMPUTER INTERFACE AND EIA CABLES

With guaranteed zero defects, cables having 25 and 37 conductors are available in lengths up to 300 ft (91 m). Every circuit is hi-potted and checked for continuity. Cable ends are permanently identified with hot stamped markers of heat shrinkable tubing and terminated with connectors having gold plated contacts in accordance with RS-232-C specs. Custom configurations are also produced in the guaranteed zero defects mode. **VIP Industries, Inc,** 246 Knickerbocker Ave, Paterson, NJ 07503.



Circle 258 on Inquiry Card

PCB MOUNTED DC TO DC CONVERTERS

The 2303 through 2317 series of 15 converters service isolated power requirements, providing input voltages that range from 5 to 28 V with complementary output voltages ranging from 5 V at 1000 mA to ±15 V at ±412 mA. Current limiting is provided, with the max current output limited to 150% of rated load current. Units have thermal shutdown circuits, and can survive for 8 h with all outputs shorted while at an amb temp of 71 °C. **Teledyne Philbrick,** Allied Dr at Rte 128, Dedham, MA 02026.

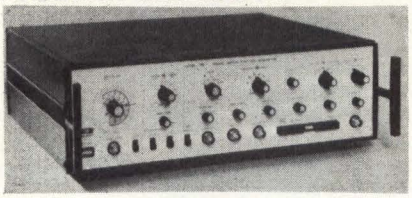
Circle 259 on Inquiry Card

HIGH VOLTAGE, LOW CURRENT DC CONNECTOR

Connectors offer high voltage, low amperage couplings without current leakage or unwanted corona effects. Mated connector fittings pass a 20-kV hipot test; losses at 16-kV operating potential are lower than 10 nA/pair. Assembled connectors operate from −54 to 65 °C and withstand 24" (61-cm) deep water immersion at operating voltage. Applications include use in commercial high voltage power supplies, and military and commercial CRTs. **Barclay Electronics, Inc,** 927 Madison, Birmingham, MI 48008.

Circle 260 on Inquiry Card

30-MHz AM/FM FUNCTION GENERATOR

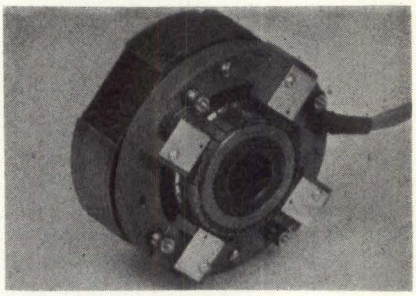


Two separate generators in 1 package generate sine, square, and triangle waveforms. Main generator frequency range is 0.0001 Hz to 30 MHz; the AUX generator has a range of 0.01 Hz to 1 MHz. The latter can frequency modulate (over a 3-decade frequency band), sweep (over a 1000:1 ratio), gate, trigger, or amplitude modulate the MAIN generator. For each generator of model 739, the symmetry of the selected waveform can be varied from 19:1 to 1:19. **Exact Electronics, Inc,** PO Box 347, Tillamook, OR 97141.

Circle 261 on Inquiry Card

DC TACHOMETER-GENERATOR WITH PM FIELD

Air stabilized tachometer-generator requires no keeper. Designed for integral attachment to the drive machine, model NCS is 3.062" in dia x 1.75" long (7.777 x 4.45-cm) and weighs 27 oz (756 g). Outputs available are 3, 7, 9, 19, 31.5, and 38 Vdc/1000 r/min with speed range of 4 to 4000 r/min. Housed or unhoused units feature replaceable cartridge brushes, and an average-to-peak ripple of less than 2%. **Powertron Corp,** 3821 Barringer Dr, Charlotte, NC 28224.



Circle 262 on Inquiry Card

16-BIT S-D CONVERTER

Accurate to 1.3 arc min with 16-bits resolution, the SD436 is packaged in a 3.12 x 2.62 x 0.82" (7.92 x 6.65 x 2.08-cm) module. Input/reference voltages are 11.8/26 Vrms ± 10%. Input frequency is 400 Hz ±10%. 16-bit binary output is DTL/TTL compatible. Tracking rate is 360°/s max. Military range is −55 to 105 °C; commercial range is 0 to 70 °C. Power requirements are ±15 Vdc at 100 mA and 5 Vdc at 400 mA. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

Circle 263 on Inquiry Card

NCR COMPATIBLE CASSETTE TERMINAL

The 5450VRL 8080 based memory storage system features an optional variable record length read capability for compatibility with NCR's variable block length systems. The std unit is compatible with Sweda, TI, and all other RS-232 compatible systems. Accommodating ANSI/ECMA compatible cassettes, the terminals automatically perform read after write, CRC, and parity error checks. For the 5450, capacity is 442k formatted char; for the 5000, 221k char; and for the 2500, 350k char. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.

Circle 264 on Inquiry Card

MINI-CASSETTE TRANSPORT WITH READ AFTER WRITE

Read after write capability added to CM-600 miniature cassette transport allows verification of data during recording. The 3.5 x 3.5 x 2.5" (8.9 x 8.9 x 6.3-cm) device contains all motor control and read/write electronics. The drive uses 50 and 80' (15.2- and 24.4-m) certified digital minicassettes with a capacity of more than 1M bits at a density of 800 bits/in (315/cm). Data transfer rate is 2400 baud. Power requirement is 5 Vdc at less than 1 W. **Braemar Computer Devices, Inc,** 11950 12th Ave S, Burnsville, MN 55337.
Circle 265 on Inquiry Card

CARTRIDGE DISC CONTROLLER FOR PDP-11 UNIBUS

Controlling 2.5M-, 5M-, 10M-, and 20M-byte cartridge disc drives, model 610 provides complete emulation of the RK11 in a single 2-sided quad-board package. It is hardware, software, and media compatible with the RK11/RK05 when used with 100-track/in (39/cm) drives. Its Micro-Module concept, developed using bit slice technology, supports Winchester drives. Added features are 100% position verification, sector write protect, and self-test. **Xylogics Inc,** 42 Third Ave, Burlington, MA 01803.
Circle 266 on Inquiry Card

INTERFACE CONTROLLER AND POWER MODULE

Model 8960-A can simultaneously switch up to 160 channels to A or B by the master A,B switch, computer command, or model 8930 remote control panel. Module controls and monitors DCD status on up to 8 8906 or 8909 2-channel EIA A,B switch, patch, and monitor modules (16 channels of switching). Master control switches all 16 channels to A or B. Individual A,B switching is provided on each switching module or at remote control panel. LEDs display status of 12 key EIA signals present at monitor in front panel connector. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.
Circle 267 on Inquiry Card

BRIGHT WIDE VIEWING ANGLE LED

Super bright version of LED has >180° viewing through the use of a flat topped, cylindrical lexan fresnel lens. Mounting on top of or below panel is via panel mounting clips, mounting bushings, or mounting sockets; the LEDs can be soldered directly to PC boards. Measuring 0.280" (7.112 mm) long and 0.203" (5.156 mm) in dia, LEDy Bugs are available in red, amber, and green versions with a brightness of 8, 8, and 5 mcd, respectively. **Data Display Products,** 303 N Oak St, Inglewood, CA 90302.
Circle 268 on Inquiry Card

SERIAL PERIPHERAL CONVERTER BOARDS

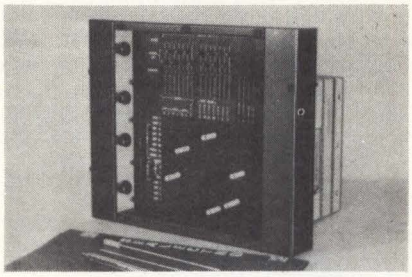
Mounted inside the host peripheral and powered from it, SIO V.24 series devices enable the peripheral to be connected to either a CCITT V.24/RS-232 serial interface or a current loop serial interface. The boards have programming switches to select baud rate, char format, and error codes. Models are available for the Trend UDR 700 paper tape reader, Facit 4070 paper tape punch, and Data Products B300 line printer. **Warren Logic Ltd,** Hockley Rd, Broseley, Salop TF12 5HT, England.
Circle 269 on Inquiry Card

VOLTAGE REGULATORS WITH TRIPLED VOLTAGE LIMITS

Linear IC voltage regulators can handle input levels of between 200 and 250 Vdc and output 180 Vdc with ±5% regulation. 1-package 3-terminal plug-in circuits output 20 mA or less (900 model) or 50 mA or less (905 model). Current surges or spikes above either level will fold the current back to a safe point, holding at that point until the malfunction is corrected. In addition to 25-dB at 120-Hz ripple rejection, regulators also have built-in thermal shutdown. **Dionics, Inc,** 65 Rushmore St, Westbury, NY 11590.
Circle 270 on Inquiry Card

PRODUCTS

10-DECK CUSTOM MATRIX ASSEMBLY



Multideck matrix program board embodies waterproof momentary pushbutton switches for circuit test, LED status display indicators, safety illumination for nighttime operation, and removable name tags. Pin lockout permits insertion of only 1 pin/column to prevent mixing of circuits. Shielded construction minimizes crosstalk. Front plate has tapped holes for each program point; dummy pins can be inserted to prevent accidental programming of unauthorized channels. **Sealectro Corp, Programming Devices Div,** Mamaroneck, NY 10543.
Circle 271 on Inquiry Card

EVENT TRAPPING FOR APL SYSTEMS

Allowing the programmer to specify an action to be performed when an error interrupt or other event occurs, Event Trapping enhancement improves user interface, reliability, efficiency, and security of APL application systems. The event contingent action usually consists of a line of APL which is to be executed when the event occurs and an action code describing how the line is to be put into execution. **I. P. Sharp Associates Ltd,** 145 King St W, Toronto, Ontario M5H 1J8, Canada.
Circle 272 on Inquiry Card

COMPACT DISCRETE AUTOMATIC TEST SYSTEM

Test hardware, power supplies, control processor, and dual-cassette drive comprise DATASPEC, which tests bipolars, darlingtons, FETs, switching diodes, rectifiers, zeners, SCRs, and triacs. Choice of 1 or 2 test stations and control terminal complete the system. The tester programs up to 125 tests and 99 sorts, and allows simultaneous use of 2 different test programs. It performs 1-kHz ac measurements. Power to 2 kV and 100 A is available. Datalogging capability is also included. **Lorlin Industries, Inc,** Precision Rd, Danbury, CT 06810.
Circle 273 on Inquiry Card

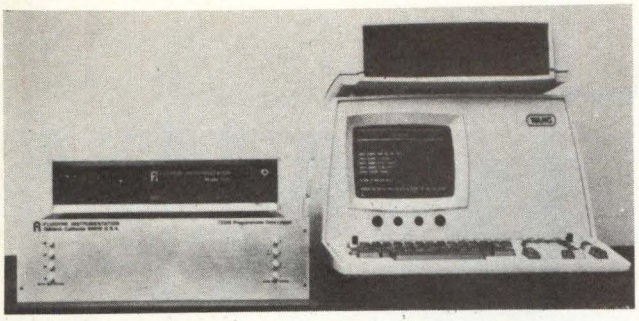
HIGH SPEED 14- AND 16-BIT ADCs

Mechanically interchangeable with Analogic MP2714 series, ADCs meet analytical instrumentation requirements. Model 2816 converts 16 bits in 100 μs; model 2814 requires only 50 μs to convert 14 bits. Max linearity error is $\pm$0.0015% and $\pm$0.003% of full scale, respectively, for the two versions. Max linearity tempco is $\pm$0.5 ppm/°C, and max power consumption is only 1.5 W for both converters. Four full-scale standard signal range selections are provided. **Dynamic Measurements Corp,** 6 Lowell Ave, Winchester, MA 01890.
Circle 274 on Inquiry Card

HIGH LINEARITY ISOLATION AMPLIFIER

Featuring 0.005% linearity for compatibility with 12-bit data acquisition systems, model IA175 operates at common-mode input voltages up to 5000 Vdc for use with signal sources in high voltage systems and other hazardous locations. Common-mode rejection is at least 120 dB with source imbalance of up to 5000 Ω. Input voltage noise is 1 μV, 10 Hz to 1 kHz, and current noise is 10 pA for the same range. **Intronics,** 57 Chapel St, Newton, MA 02158.
Circle 275 on Inquiry Card

PROGRAMMABLE DATA LOGGER WITH MINICOMPUTER



Combining a minicomputer that operates in BASIC with precision measuring capabilities, the 7251B contains a 4½-digit integrating autoranging digital voltmeter with a sample rate of 2.5 readings/s. Scanner mainframe can accommodate either 140 low level 3-wire reed relay multiplexer channels or 224 high level channels, or any combination between the two. Output or feedback control from the computer and up to 112 Form C (spdt) output relay contacts can be provided. The internal computer contains a CRT with 16 lines and 64 char/line, a read/write minidiskette with storage for programs or data (89k bytes), 42.5-byte ROM extended basic interpreter, and 8k bytes of RAM expandable to 32k. An 80-col 300-char/s dot matrix printer is included with the system. **F. I. Electronics,** 968 Piner Rd, Santa Rosa, CA 95401.

Circle 276 on Inquiry Card

FIBER OPTIC COMMUNICATION SYSTEM

Practical detachable connection with a 10-min field termination time includes optical emitter and optical detector. Emitter transforms electrical input into modulated light output using a LED and optical lens held in the unit's housing. The RCA C30123 IR LED is a high speed edge emitter with 8-ns rise time, 50-MHz frequency response, and 830-nm typ wavelength. Power output is 1 mW. Detector uses a photodiode and optical lens to transform optical input into an electrical output. The planar diffused silicon pin photodiode has a response time of 15 ns and dark current of 0.1 μA; it is typically operated in the photoconductive mode. Detector/connector assembly can operate from −55 to 90 °C. Both intermate with std MIL-C-81511 electrical receptacles for input and outputs. **The Deutsch Co,** Municipal Airport, Banning, CA 92220.

Circle 277 on Inquiry Card

0- to 1200-BAUD ACOUSTIC COUPLER/MODEM

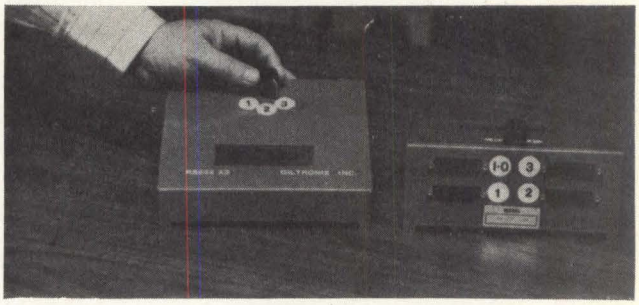
Model TC3003 Hotline™, an acoustic coupler for voice grade telephone lines and long distance direct dial systems, offers a full set of test functions and system troubleshooting. Design and operational features include 0- to 1200-baud, asynchronous, full-duplex operation or 0- to 300-baud operation with Bell 113B; compatibility with all computer systems and data terminals using Bell 103 handshakes; and lack of restrictions (not character oriented like other acoustic couplers). The unit meets EIA RS-232-C and 20-mA current loop standards, and provides accuracy and stability over wide variations in temperature, data rate, line voltage, and received signal amplitudes. Sensitivity is −42 dBm. **Tek-Com Inc,** 1147 Sonora St, Sunnyvale, CA 94086.

Circle 278 on Inquiry Card

CIRCLE 124 ON INQUIRY CARD

PRODUCTS

MINIATURE RS-232 SWITCHING UNITS



RS232-X3 allows connection of an RS-232 peripheral (line printer, CRT, or modem) to 3 driving sources. By turning the 3-position switch, mounted on the switching unit, the user can select which driving device will drive the peripheral unit. Two or more switches may be cascaded to expand selection from 3 devices to 5 or more. RS232-XF is similar to the -X3 but switches additional signals. Both -X3 and -XF come with 25-pin female connectors. -X8K, -X16K, -X8, and -X16 are similar to the other units but have different switching configurations, allowing a wide selection to users. In addition, -X16K and -X16 switch 16 EIA pins, which are 3 more than the previous maximum of 13. Units are available fully assembled or in kit form. **Giltronix Inc,** 3156 Avalon St, Palo Alto, CA 94306.
Circle 279 on Inquiry Card

HIGH RESOLUTION GRAPHICS PROCESSOR FOR PDP-11

Contained on 2 hex boards that are plug compatible with DEC's PDP-11, MDP-3 has a refresh memory of 65,536 words by 18 bits. Of the 18 bits, 16 contain the images to be displayed; the remainder are for graphic overlays that highlight particular data. The unit will simultaneously drive both black/white and color monitors, and is equipped with a zoom capability. The processor board is a general purpose 16-bit computer microprogrammed with an instruction set similar to that of a minicomputer. The graphics processor is a 16-bit general purpose computer built with the bipolar 2903 bit slice. Displays are possible in formats of 512 x 512 interlaced picture elements by 4 bits or 256 x 256 noninterlaced elements by 16 bits. **Computer Design & Applications, Inc,** 377 Elliot St, Newton, MA 02164.
Circle 280 on Inquiry Card

MODULAR 2400-BIT/s SYNCHRONOUS DATA MODEM

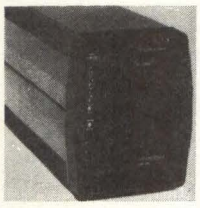
Based on MOS LSI devices, the R24 consists of 3 modules which can be assembled on 1 or more of the system boards of terminals and other data equipment. Each module is encased in a plastic package with vertical pins on 100-mil centers, permitting them to be plugged into std connectors or wavesoldered on PC boards. One module implements the transmitter, while 2 modules implement the receiver function. Each is 0.5" (1.27 cm) deep and about 3" (7.62 cm) on a side. Transmitter and R1 and R2 receiver modules are compatible with Bell 201B/C and CCITT V.26 A/B stds. High performance is attained with a transmitter design based on differential phase modulation and receiver using coherent phase detection techniques. Device has signaling rate of 1200 ±0.1% baud and carrier frequency of 1800 ±1 Hz. **Rockwell International, Electronic Devices Div,** 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803.
Circle 281 on Inquiry Card

INFORMATION MANAGEMENT SYSTEM

Factmatcher combines an information storage and retrieval system capable of extracting information from a structured or unstructured data base of 10,000 documents in less than 1 s, an easy to learn query language that enables target facts to be matched with all documents containing them, a word processing system, and a communications capability that permits text to be transferred, displayed, or printed at any local or remote station of the system. Memory sizes range from 64k to 256k bytes. The system can communicate with other vendor's equipment via a bisynchronous interface at rates varying from 2400 to 9600 baud; with a typical 4800-baud line, some 1000 pages of text can be transmitted in 1 h. **Mini-Computer Systems, Inc,** 399 Fairview Park Dr, Elmsford, NY 10523.

Circle 282 on Inquiry Card

BELL COMPATIBLE 2400-BIT/s SYNCHRONOUS MODEM

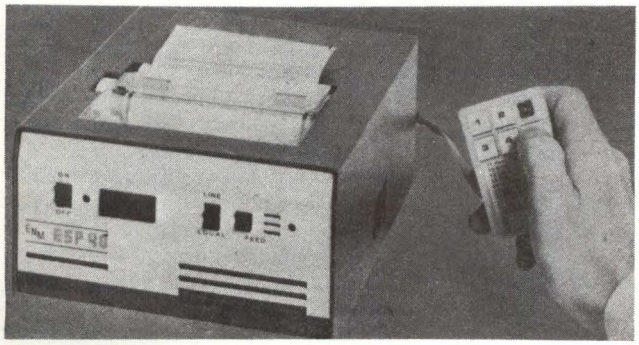


Two LSI chips perform all transmitter and receiver digital signal functions associated with 2400-bit/s Bell 201C operation or the standards of CCITT V.26. Chips are mounted on a single PC module, accessible through the front panel for easy replacement. Reduction in component count extends reliability, with MTBF for the unit exceeding 40k hours. LSI 2400 supports full-duplex operation on conditioned or unconditioned 4-wire telephone lines at 2400 bits/s with fallback to 1200 bits/s under adverse line conditions. Initialization or train times of 7 ms or less, low error rates, and high immunity to communications line impairments, especially noise and phase jitter, are features. LED indicators provide operators with information on current operating status. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.

Circle 283 on Inquiry Card

MINIATURE PRINTER FOR MOBILE APPLICATIONS

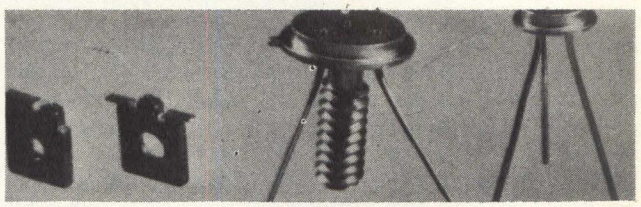
ESP-40 operates in any plane, printing images transmitted by digital facsimile equipment or from a keyboard. Using a nonimpact matrix printing process, the unit outputs on electrosensitive paper 114-mm wide at rates up to 280 char/s. A built-in microprocessor with a 320-char buffer store enables the unit to print u/lc char (7 or 9 dots high). Between 2 and 8 char/cm can be printed and chars of different widths can be mixed on the same line. For plotting diagrams, the buffer output is applied directly to the printhead, enabling up to 8 vertical dots to be printed at 240 printhead positions across the width of the paper. Unit measures 205 x 210 x 105 mm without cooling fan and weighs 3.6 kg. It operates from a 12-Vdc supply and consumes 24 W when printing and <11 W in standby. **English Numbering Machines Ltd, Printer Div,** Queensway, Enfield EN3 4SB, Middlesex, England.



Circle 284 on Inquiry Card

PRODUCTS

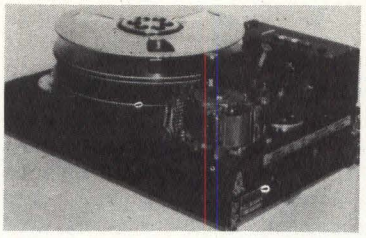
INFRARED EMITTING DIODES



HLP20 to 60 series are made of GaAlAs and feature a hemispherical emitting surface. Available in 4 types of packages in wavelengths from 715 to 950 nm, diodes are characterized by their high power output, and offer an 18% power efficiency with rise and fall times of less than 12 ns, 3 dB down at 40 mHz. The IRED chip is formed by a p-n junction grown by liquid phase epitaxy, and is isolated by an etched groove around the n-region. When the p-n junction is forward biased, photons are generated through recombination; this photon energy varies according to the energy gap of the p-region. Thus, varying the mole fraction of Al in the GaAlAs of the p-region can change the peak wavelength of the emission from 715 to 905 while maintaining high external efficiency. **Hitachi America, Ltd,** 707 W Algonquin Rd, Arlington Heights, IL 60005.
Circle 285 on Inquiry Card

COMPACT MIL-SPEC AIRBORNE RECORDER

Designed for data acquisition during flight tests, the Sabre XII has full 8-speed capability (0.9 through 120 in/s, or 2.4 to 304.8 cm/s). Interchangeable IRIG formats are available in 7, 14, or 28 channels. Compact separate mainframe and record electronics modules can be installed up to 45 ft (13.7 m) apart in the aircraft. Control from the cockpit is possible with 2 types of miniature remote units, each with single button pretest, all-channel automatic calibration, and multifunction alarm. Unit is fully operational under extreme conditions of temperature, vibration, and shock. Unit withstands vibration per MIL-E-5400 and shock on all axes per MIL-STD-810. **Sangamo Data Recorders,** PO Box 3041, Sarasota, FL 33578.



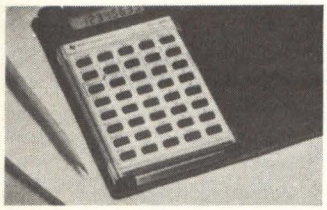
Circle 286 on Inquiry Card

SOFTWARE PACKAGE FOR HASP EMULATION

HASP/16 Workstation Emulator software enables 16-bit minicomputers to emulate the industry standard IBM HASP workstation while satisfying local processing requirements. It turns the processor into a remote job entry station where users submit batch jobs to a host IBM processor using binary synchronous communications protocol. Batch jobs can be processed by host systems with results returned to processor for local storage or output. Both host and alternate remote mode of operation are supported to permit communication between 16-bit systems. Executing as a user task under OS/16MT2, the package supports up to 7 card readers and 8 printing devices, control console, and dial-up or leased communications line operating at speeds up to 19.2k baud. **The Perkin-Elmer Corp, Computer Systems Div,** 2 Crescent Pl, Oceanport, NJ 07757.
Circle 287 on Inquiry Card

ECONOMICAL HANDHELD SCIENTIFIC CALCULATOR

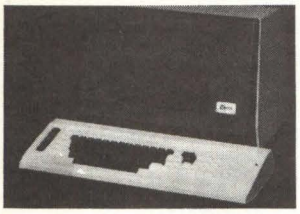
Slimline Ti-35™ calculator includes a 4-key Constant Memory™ which can store, recall, sum to memory, and exchange memory with the display, while retaining data when turned off. The 54-function slide rule calculator has roots, powers, reciprocals, common and natural logarithms, and trigonometric functions in degrees, radians, or grads. Special functions include pi, factorial, and constant. Scientific notation extends the useful range of calculations. Built-in statistical capabilities include mean and standard deviation for both sample and population data. AOS™ algebraic operating system allows entry of problems from left to right. The unit automatically retains up to 4 pending operations and up to 15 levels of parentheses. **Texas Instruments Inc,** PO Box 53, Lubbock, TX 79408.



Circle 288 on Inquiry Card

VT52 COMPATIBLE AND APL TERMINALS

Microprocessor based asynchronous data terminal for use in small business systems, computer timesharing, and with mini/microcomputers, the model VC4152 is compatible with DEC's VT52 display terminal and features a detachable u/lc typewriter keyboard, 1920-char display, and data rates to 9600 baud. Features include a 25th status line, character highlighting, and 10 special function keys. Hold screen mode and dual mode keypad are selectable from the keyboard and a transparent/tape mode switch is std to allow the operator to display all 128 ASCII characters. Model VC415APL offers both ASCII compatibility and full APL overstrike capability switch selectable. The terminal features a buffered line edit mode for preparation of data, and selectable independent window for host responses so existing screen data are not erased during programming operations. **Volker-Craig Ltd,** 266 Marsland Dr, Waterloo, Ontario N2J 3Z1, Canada.



Circle 289 on Inquiry Card

DOUBLE-DENSITY FLOPPY SYSTEM WITH INTEGRAL MICROPROCESSOR

Functionally identical to DEC's 11V03L, the MF-211 includes double-density controller with dual Shugart floppy discs that operate in both single- and double-density mode and provide complete RX02 instruction set compatibility. Also included is the DEC H9270 4-quad-slot backplane with LSI-11/2, power supply, and front panel console, all within a 10.5" (26.7-cm) rack-mountable enclosure. Front panel console offers switches for line time clock, enable/halt, and bootstrap loader, with indicators for Run and DC OK. DMA data transfer by sector, bootstrap loader (eliminating need for DEC's REV-11 or BDV-11), IBM 3740 formatter, self-diagnostic, and interface electronics are all contained on a single dual-height card which plugs directly into the H9270 backplane. **Charles River Data Systems, Inc,** 4 Tech Circle, Natick, MA 01760.

Circle 290 on Inquiry Card

LITERATURE

Logic Test Equipment

Flowcharts, sample monitor displays, and selection flow diagram, along with text, describe selection and application of logic analyzers; second guide lists logic measurement products according to application. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 300 on Inquiry Card

Data Converters

Catalog features A-D and D-A converters, S/H and T-H amplifiers, and related products, and provides product parameter comparison tables. **ILC Data Device Corp,** Bohemia, NY.
Circle 301 on Inquiry Card

Components

Featuring specs, engineering drawings, and application information, catalog assists in selection of solder and insulated terminals, variable and fixed coils, connectors, and panel and chassis hardware. **Cambridge Thermionic Corp,** Cambridge, Mass.
Circle 302 on Inquiry Card

PCB Edge Card Connectors

Photos, specs, and dimensional drawings in 96-p catalog specify 2- to 200-contact gold, silver, or tin plated, eyelet or wrap post terminated connectors. **ITT Cannon Electric Div,** Santa Ana, Calif.
Circle 303 on Inquiry Card

Power Sources and Converters

General specs, dimensional drawings, circuit diagrams, and mechanical information are provided in 42-p catalog. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 304 on Inquiry Card

Severe Environment Hardware

Catalog provides information on ruggedized single-board microcomputer and support modules, 16-bit minicomputer emulator, digital data recorder, and digital data acquisition package. **EMM/Sesco,** Chatsworth, Calif.
Circle 305 on Inquiry Card

Intelligent CRT Terminals

Brochure profiles three models, including system architectures, block diagrams, memory maps, and spec and comparison sheets. **Zentec Corp,** Santa Clara, Calif.
Circle 306 on Inquiry Card

Programmable Controllers

Brochure provides a succinct look at programmable controllers with sections covering what they are, how they work, what they do, and why they are better than other control systems. **Gould Inc, Modicon Div,** Troy, Mich.
Circle 307 on Inquiry Card

Delta Modulation for Voice Transmission

Application note describes continuously variable slope delta modulator, all-digital CMOS IC modulator/demodulator, and applications for each. **Harris Semiconductor Products Div,** Melbourne, Fla.
Circle 308 on Inquiry Card

Gearmotors

Cutaway photographs, dimensional drawings, charts of output torque in lb-in, and a speed-torque horsepower chart for FHP induction or universal/dc powered motors are supplied in catalog. **Howard Industries,** Milford, Ill.
Circle 309 on Inquiry Card

Uninterruptible Power Systems

Guide describes units used to create uninterruptible power systems, and how they are linked to furnish required power. **CML Macarr Div of Marine Electric RPD,** Edison, NJ.
Circle 310 on Inquiry Card

Punched Tape Readers

Suitability of punched paper tape for machine control, applications, and product definitions for line of punched paper tape readers are described in brochure. **EECO,** Santa Ana, Calif.
Circle 311 on Inquiry Card

Trackballs

A blend of technical and application data with specs for standard units comprise 12-p catalog on trackballs. **Measurement Systems, Inc,** Norwalk, Conn.
Circle 312 on Inquiry Card

Miniature LEDs

Catalog details line of LEDs with electrical, optical, and electro-optical characteristics; max ratings; schematics; and dimensional drawings. **Chicago Miniature Lamp Works, General Instrument Corp,** Chicago, Ill.
Circle 313 on Inquiry Card

Process Control Wire and Cable

With emphasis on flame retardant and nuclear grade constructions, catalog uses descriptions, spec charts, and stripped-cable photographs to compare constructions and insulation systems. **Brand-Rex Co, Electronic and Industrial Cable Div,** Williamantic, Conn.
Circle 314 on Inquiry Card

Color Graphics Display Generator

Brochure describes features and capabilities of model 5217, a standalone fully buffered 8-color generator packaged within its own keyboard, that interfaces with any monochrome or color monitor. **Aydin Controls,** Fort Washington, Pa.
Circle 315 on Inquiry Card

Flat Ribbon Cable Mass Termination Connectors

Catalog contains a technical documents list of Latch product applications and performance, typical connector and header configurations, and specs, and covers PCB mounting, and application tooling. **AMP Inc,** Harrisburg, Pa.
Circle 316 on Inquiry Card

In-Circuit Test Fixture

Advantages of Mark II's vacuum actuated fixed pin design, reliability of replaceable probe pins, easy access hinged assembly, and broad range of board size compatibility are discussed in brochure. **Plantronics Zehntel,** Walnut Creek, Calif.
Circle 317 on Inquiry Card

Laboratory Minicomputers

Family of minicomputer systems configured for research laboratories are presented in pamphlet that discusses central processor and options, I/O interfaces, mass storage devices, and terminals. **Digital Equipment Corp,** Maynard, Mass.
Circle 318 on Inquiry Card

P/ROM Selection Guide

Guide presents basic information, commercial and military part numbers, configurations, and pinouts for P/ROMs, EPROMs, diode arrays, FPLAS, FPGAS, and PALS; second section discusses P/ROM programming. Send letterhead requests to **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 94301.

25-MHz Memory Test System

Brochure discusses major system modules, software, reliability and maintainability, typical configurations, and options for memory tester. **Macrodata Corp,** Woodland Hills, Calif.
Circle 319 on Inquiry Card

Synchros, Resolvers, and Pick-Offs

Data sheet lists specs for control and torque systems designed to MIL-S-20708C and to NEPR No 22, and features 2- and 3-speed slab synchros and resolvers. **Muirhead-Vactric Div, Muirhead, Inc,** Mountainside, NJ.
Circle 320 on Inquiry Card

Reed Keyboard Switches

General technical information, and mechanical and electrical specs are supplied for snap and screw mounting and plunger style glass enclosed reeds. **Standard Grigsby, Inc,** Aurora, Ill.
Circle 321 on Inquiry Card

Statistical Network Processor

Brochure supplies specs, operating parameters, and typical application diagrams for processor that combines functions of intelligent concentrator and statistical time division multiplexer. **Prentice Corp,** Palo Alto, Calif.
Circle 322 on Inquiry Card

Printer and Display Terminals

30/15/10, 60/30, and bidirectional 180-char/s, keyboard send/receive and receive-only printer terminals plus swivel-tilt display terminal with detachable keyboard are featured in brochure. **Data General Corp,** Westboro, Mass.
Circle 323 on Inquiry Card

Miniature Alphanumeric Printer

Simplified block diagrams, I/O line listing, and specs describe 1.5-line/s thermal printer that forms 20 5 x 7 dot matrix characters across a 2.25" (57.2-mm) wide, 150' (45-m) roll of thermal paper. **Datel Systems, Inc,** Mansfield, Mass.
Circle 324 on Inquiry Card

Heat Sinks

"Thermal System Approach to Heat Sink Selection," a 24-p application handbook includes theorems, graphs, applications, how to solve problem areas, and cost saving methods. Send requests on company letterhead to **AHAM Tor,** 27901 Front St, Rancho California, CA 92390.

Standard and Custom Keypads

Photos, specs, and dimensional drawings are supplied in catalog for 3 x 4 and 4 x 4 keypads as well as for array stackable 1-, 2-, 3-, and 6-button switch modules. **Grayhill, Inc,** La Grange, Ill.
Circle 325 on Inquiry Card

Supervisory Control Systems

Stressing man/machine interface, supervisory control functions, and calculation capability, brochure presents TDC 2000 systems. **Honeywell Inc, Process Management Systems Div,** Phoenix, Ariz.
Circle 326 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

COMPUTERS AND COMPUTER SYSTEMS

ADVERTISERS' INDEX

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For complete information on the new CPS Digital Plotting Systems, call or write Houston Instrument, One Houston Square, Austin, Texas 78753. (512) 837-2820. For rush literature requests or sales office information, persons outside Texas call toll free 1-800-531-5205. In Europe contact Houston Instrument, Rochesterlaan 6 8240 Gistel Belgium, phone (059) 27 74 45.

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