A PennWell Publication

NOVEMBER 1982

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT: DESIGNING FOR AUTOMATION AND CONTROL

MULTIPROCESSING IMPROVES ROBOTIC ACCURACY AND CONTROL

UNDERSTANDING THE HIGH SPEED DIGITAL LOGIC SIGNAL

UP FRONT

Manufacturers recommend recording format for streaming drives

Representatives of 15 companies from 3 continents are attempting to define an Interchange Identification Capability (I^2C) that will identify the format, including track layout, of data recorded on quarter-inch tape cartridges by streaming drives. Completion of the I^2C is expected this month at a meeting in San Diego. Committee participants include Archive, BNR, Cipher Data Products, Computer Storage Technology, Data Electronics, Data Packaging, Kennedy, Nippon Electric, the Qantex Div of North Atlantic Industries, Rosscomp, Sankyo Seiki Mfg, Tandberg Data, TEAC, 3M, and Western Digital. I^2C will permit a drive to determine what acceptable recording format was used to generate a cartridge and enable the drive to read and write data in the same format.

Joint technology agreements

Motorola Semiconductor Products and Advanced Micro Devices (AMD) have agreed to jointly develop and supply three dynamic memory support ICs: a dynamic memory controller and two memory timing controllers. Memory support functions will be partitioned among the chips to allow more flexibility and higher performance than would be possible with all functions on a single chip. The circuits will be fabricated using oxide-isolated bipolar technologies with TTL I/Os. Sample quantities of these ICs are expected in Q4 1983. Samples of a version containing error detection and correction circuits will be available from Motorola in Q1 1983 with production starting in Q2. The AMD version is available now.

AEG-Telefunken AG and United Technologies Corp (UTC) have signed a final agreement to create an electronic components joint venture company, Telefunken Elektronische Bauelemente GmbH (TBG), which will start operating this month. After a capital increase to approximately $40 million by the end of 1982, each partner will hold 49%; Sueddeutsche Industriebeteiligungs GmbH, a subsidiary of Dresdner Bank AG, will hold the remaining 2%. TBG will continue the activity of AEG's Elektronische Bauelemente Div and will take over its assets, as well as the manufacturing of discrete semiconductors, opto-electronic components, ICs, solar cells, and thick film circuits. The joint venture agreement calls for TBG and UTC to form a new company, Telemos Electronic GmbH, which will concentrate on the development and production of custom semiconductor devices using NMOS, CMOS, and gate array technology. Under the agreement, the UTC Microelectronics Center and UTC's Mostek subsidiary will cooperate in introducing advanced VLSI technology to Telemos.

ZyMOS Corp and Standard Microsystems Corp have an agreement-in-principle to act as second-source suppliers for each other's custom IC devices. The agreement covers silicon gate NMOS and CMOS custom devices and will be finalized when qualification testing is complete.

AT&T International and NV Philips' Gloeilampenfabrieken have begun formal discussion of a possible joint effort in the field of telecommunications in countries outside the United States, with initial emphasis on digital switching for public networks. No final agreements on the type or scope of cooperation, if any, have been made.

The Technical Products Div of Data General Corp and CSP, Inc have signed an agreement "to address the marketing of related product offerings for computationally demanding applications." DG's 32-bit Eclipse MV/8000 and MV/6000 computers and CSPI's MAP array processors are now used together in scientific and industrial markets requiring realtime processing and high throughput.

UP FRONT

Pretriggers

Single-chip Ethernet controllers dramatically reduce the cost of connecting to related local area networks. Comparable versions from Intel and Seeq Technology replace previous controllers that were implemented on one or two PC boards.

A nonimpact printer system based on ion deposition imaging that operates at 60 pages/min is a lower cost alternative for laser xerographic systems. Mercurion I from Southern Systems costs 50% less than the laser versions and is predicted to provide letter quality copy at about 50% less per page.

VME based 16-bit computer systems support different processors and a variety of mass storage devices. Victory Computer Systems' Spirit and Mentor, for EDP and robotics/control applications, respectively, differ in their microprocessor and system software.

A high performance scientific and engineering minicomputer, the MassComp MC-500 exceeds the system performance of general purpose minicomputer systems in realtime data acquisition and control, high speed analysis, and graphical presentation and data manipulation. The 32-bit UNIX based computer has a 16M-byte virtual memory.

Expense and complexity of logic analyzer use is reduced by Dolch Logic Instruments' adaptive test and logic analysis system. ATLAS incorporates a general purpose computer for display and control and accepts plug-in frontend instrumentation modules for specific tasks.

Up to 100 times the data handling and arithmetic throughput of superminicomputers that cost 10 times as much is promised for Analogic's array processor. The AP500 performs a 100 x 100 matrix inversion in 649 ms and a 1024-point complex FFT in 4.7 ms.

X.25 networking at up to 1.544M bps is predicted for a flexible communications network processor that interfaces virtual operating system superminicomputers to several communications protocols. The 8470 from Harris Corp's Computer Systems Div also supports direct X.25 lines for local CPU to CPU communications.

A fiber optic Ethernet compatible local area network communications system, Fiber Optic Net/One, is the result of a 3-company joint technology development effort. The LAN uses Ungermann-Bass network interface units, Codenoll Technology optical transceivers, and Siecor/FiberLAN optical cables and connectors.

Execution of 1.25 MIPS and a bus rate of 20M bytes/s plus a price under $10,000 are key features of the Universe 68/05 computer. Charles River Data Systems claims it to be the cheapest 32-bit system on the market.

Ada compiler increases portability, decreases software development effort for DOD applications. Intel and Western Digital have released separate compiler versions for operation on different computers.

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BPA ABP

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Dataram goes to extremes to satisfy LSI-11 users.

	DATARAM B23 PLUS	PDP-11/23 PLUS	DATARAM M23	PDP-11/24	DATARAM W23
CHASSIS	5¼″ Front loading	5¼″ Front loading	5¼″ Rear loading	5¼″ Side loading or 10½″ Top loading	10½″ Top loading with 80 MB Winchester
BACKPLANE	8 x 4	9 x 4	9 x 6	9 x 6	9 x 6
I/O MAPPING	None	None	Q-MAP	KT24	Q-MAP
BUS	22-bit Q-BUS	22-bit Q-BUS	22-bit Q-BUS and 18-bit Q-BUS	22-bit extended UNIBUS (EUB) & 18-bit UNIBUS	22-bit Q-BUS and 18-bit Q-BUS
MEMORY & PERIPHERAL SUPPORT	Up to 4.0MB, but limited to 256KB when using peripherals other than RL01/RL02 or RX01		Up to 4.0MB. No basic limitation on peripherals.		
PRICING	B23, M23, and W23 are approximately 35% less than comparable DEC systems in 1.0MB configurations. Additional 1.0MB memory modules from Dataram are about 40% less than DEC's equivalent 1.0MB memory. Contact us for actual price comparisons.				

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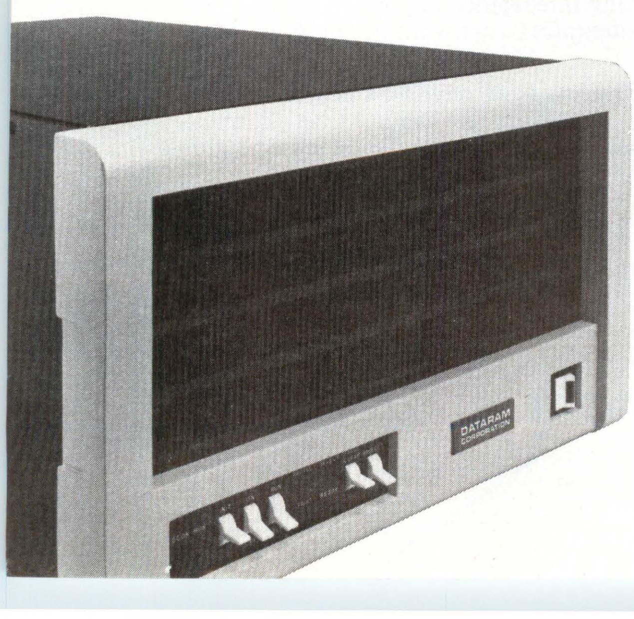
From Q-BUS Pricing to UNIBUS Performance



From top to bottom, chart the range of LSI-11 system performance you get from Dataram...and only Dataram.

It starts with our low-end B23 PLUS Q-BUS system at lower (much lower!) than DEC prices. And continues with high-end M23 and W23 Q-BUS systems that use Dataram's innovative Q-MAP™ I/O mapping module to generate a separate 18-bit bus from the LSI-11/23's 22-bit bus. Allowing you to put 4.0MB of memory on the 22-bit bus while interfacing your high-performance peripherals (RM02, TM11, RX02 and more) to the 18-bit bus. Giving you much more performance than provided by the PDP-11/23 PLUS, which supports only the RL01/RL02 and RX01 on its 22-bit bus.

It's possible, because Dataram's Q-MAP duplicates the functions of DEC's KT24 — which exists only in UNIBUS minicomputers from DEC — enabling Dataram's 4.0MB M23 and W23 minicomputers to be completely compatible with RSX11-M, RSX11-M PLUS, RSTS, UNIX and any other operating system which supports KT24 memory management.

Our W23 system goes a step further, integrating an 80MB Winchester drive and associated controller to provide even greater performance.

Q-BUS pricing...UNIBUS performance...in an LSI-11 megabyte system. Plus a wide range of disk and tape controllers, and related LSI-11 accessories. Only from Dataram. **Call us at (609) 799-0071. We'd like to tell you more about our family of LSI-11/23 based systems.**

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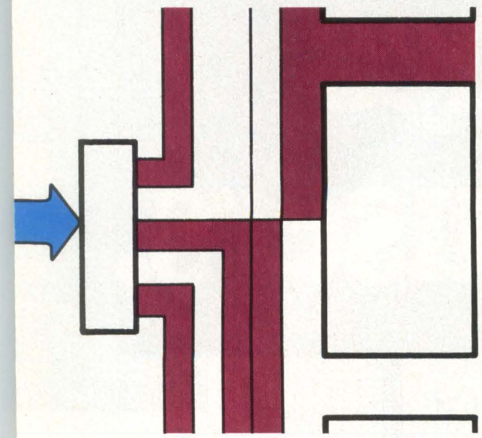
CIRCLE 4

COMPUTER DESIGN®

System technology



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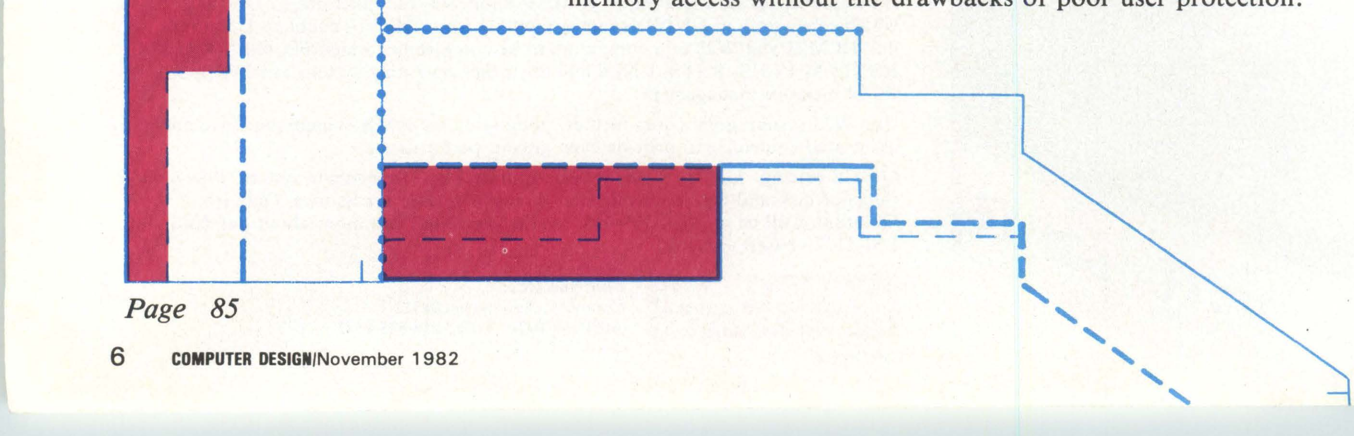
System design



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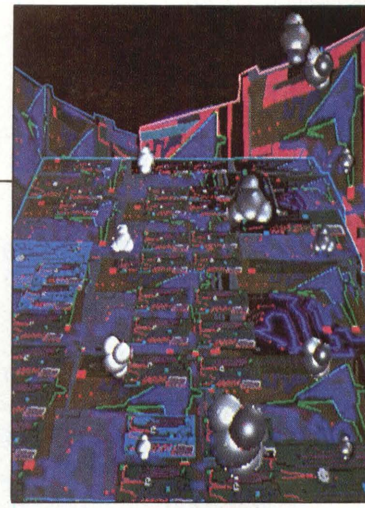
Nov 1982



This month's cover, entitled "Robotics," was created by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

Special report on designing for automation and control

System components

Departments

Designers' preference survey*

Editorial reviewers for parts of this issue:

James Crafts
David Dicklich

*Appearing in Domestic issues only

Gould Biomation

Sophisticated μPs require sophisticated debug tools.

You've got a problem. A big one. Or maybe just an annoying-as-hell little one that's hiding out somewhere in the system.

And, with so many signals flying around today's complex microprocessor architecture, just separating out the relevant information is a complex job.

You need an analyzing tool that can look at many simultaneous signals. In every practical combination. From every relevant perspective. At the push of a button.

You need internal clocking for timing analysis, external clocking to follow program execution, and a mixture of both to resolve system integration problems.

You need an instrument that can look at program execution in multiphased, multiplexed and multiprocessor systems.

And it's got to be fast, to look at TTL, ECL and bit-slice devices. At least 100 MHz internal clocking.

As well as being able to cope with a 68000 as readily as a Z80 or an 8088. Without making you build some complicated clocking arrangement of your own.

Twelve external clocks. Unlimited combinations.

With the K101-D's 12 external clocks—6 edge-sensitive "sample" and 6 level-sensitive "latch enable" clocks—you can create virtually any conceivable clocking scheme. In AND or OR combinations. For any microprocessor. Right from the keyboard.

You can synchronize the analyzer to the target system at rates to 50 MHz. Or perform high-speed timing analysis to 10 ns resolution. On as many as 48 sample inputs at once.

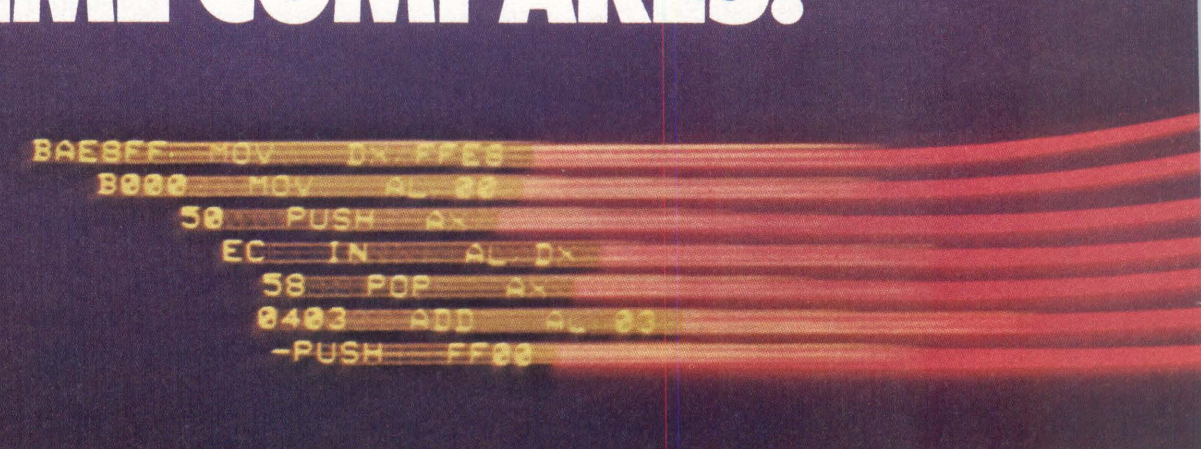
Comprehensive, intelligent sampling.

Comprehensive sampling allows all the system activity in one machine cycle—address, data, status and control lines—to be evaluated simultaneously. Even if it didn't occur that way. The K101-D collects, realigns and reduces the data you want into a meaningful sample that doesn't waste memory space. You simply set up the conditions; the analyzer makes the decisions about what to save.

Uncover the cause with trace control.

Once the clocking and input modes have untangled and realigned the data you want—generally reducing out 99% of the irrelevant data—you can pinpoint the exact cause of failure with the K101-D's 16 levels of trace control.

FOR DECIPHERING EACH MACHINE CYCLE, NO OTHER CLOCKING SCHEME COMPARES.



Clearly the best.

More sophisticated than any classical triggering system, trace control allows you to isolate and capture widely-separated slices of program flow for review and comparison. And determine exactly what caused the failure, not just where the failure occurred.

High-speed timing.

The K101-D provides full-length, full-width, full-speed analysis of all inputs. On all 512 samples. To 10 ns resolution. Across 48 channels.

You can check pulse widths, glitches, and complex skews. Any sort of timing problem. Plus timing relationships of address, data, status and control lines.

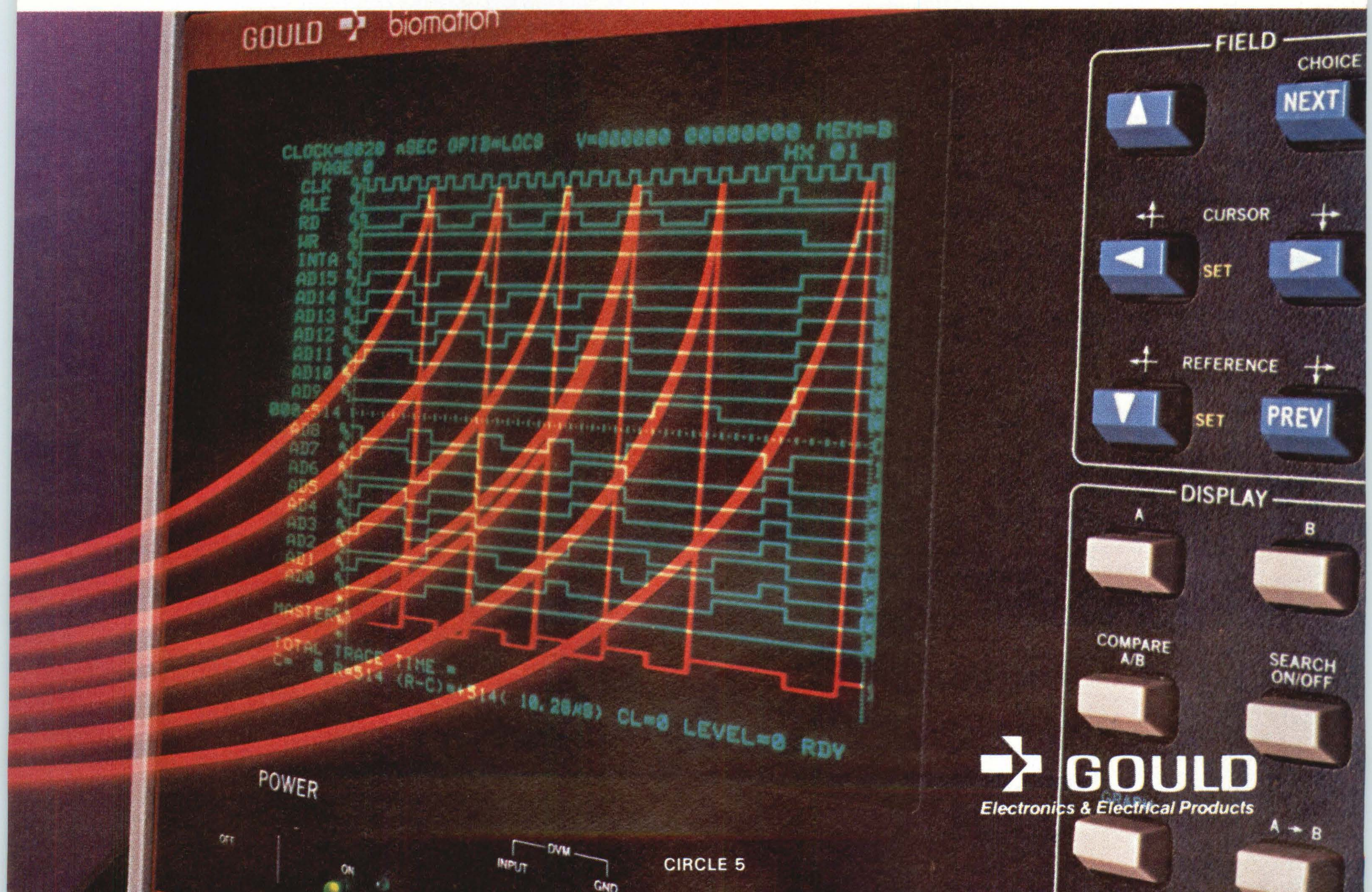
Uncompromising dedication to high performance.

The Gould Biomation philosophy dictates that every instrument we make be the best for the job it's designed to do. The K101-D and the K102-D are designed as the ultimate tools for logic analysis. The K102-D has the same powerful feature set with 32 channels and 8 clock inputs—6 edge-sensitive "sample" and 2 level-sensitive "latch enable" clocks. The K101-D and K102-D allow you to solve many system problems in a fraction of the time required by less sophisticated instruments. When you encounter the problem you couldn't solve any other way, rest assured there is no other logic analyzer that can outperform them.

For a demonstration or detailed application notes, write Gould Inc., Instruments Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279, Gould Biomation and Gould Millennium Products.

For fastest response, call toll-free: Nationwide (800) 538-9320; in California (800) 662-9231 or (408) 988-6800.

Below is an actual recording made on the K101-D, portrayed in the time domain to illustrate input clock relationships and also the resultant 8086 mnemonics display. Address, data, control and status signals are labelled as you would see them on your schematics. The simulated master clock diagram in red shows the relationship between sample points and information at those points, as shown in mnemonics. The red vertical lines indicate where each comprehensive sample is taken, for evaluation by trace control.



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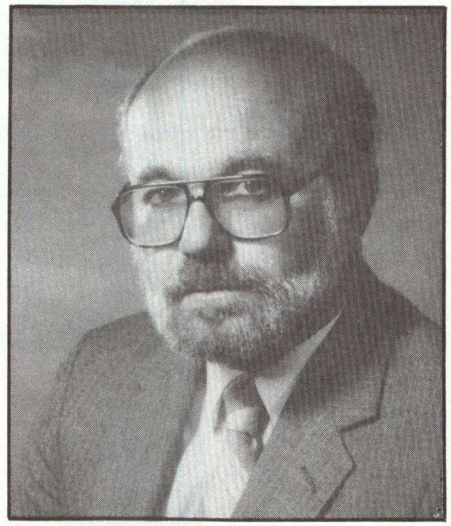
Electronics & Electrical Products

CIRCLE 5

TECHNICAL CREATIVITY AND THE EDIFICE COMPLEX



As we interviewed Hall of Fame nominees and leading industry technologists for our special 20th Anniversary December issue, I was struck by the contrast between the typical mind-set of American Big Business and the attitude that seems to have developed in American high tech Big Business.

There is no question that customs and mores are changing as younger men, and women of all ages, take their turns at the helm of corporate America, but those changes are occurring even faster in the high tech industry. Whether called relaxed, laid back, or informal, these attitudes are apparent in today's high tech corporate headquarters. The days of the three-piece, button-down-suited businessman in his deep-pile carpeted, mahogany paneled, Victorian furnished boardroom are moving into antiquity along with the prop-driven airplane and the carbon copy. Yesterday's jean-clad, slide-rule slinging engineers are now heading today's high tech companies and, spurred on by the relaxed attitudes of their younger charges, have carried leisure America right into the boardroom and the CEO's office.

Informally but tastefully dressed, one of the major pioneers of IC technology, Robert Noyce of Intel, sits in a sea of simple cubicles made from movable partitions. Says Noyce, "It makes you feel as if you're in touch with what's going on." Jack Kilby of Texas Instruments, credited as the father of the integrated circuit, stated in his interview that "environmental details such as interior decor have never affected my output." A photo of him casually attired amidst the Spartan surroundings that house his current project confirms his viewpoint.

In observing some of the recent company startups that have been kicked off in a blaze of marble halls and walnut paneled fanfare, I begin to think that maybe Jack Kilby does have the right outlook on fostering technical creativity after all.

Saul B. Dinman
Editor in Chief

Best Technical Article of the Month—March
"Eliminating Crosstalk over Long Distance Busing"
R. V. Balakrishnan, National Semiconductor

Best Technical Article of the Month—April
"A Smart Operating System for 8-bit Micros"
Roy Soltoff, Logical Systems, Inc

These articles will now compete with other monthly winning articles for the 1982 editorial excellence award.


7704A OSCILLOSCOPE SYSTEM
CH 1
POSITION
VOLTS/DIV
MEMORY DISPLAY
CURSOR WFM
TRIGGERING
CH 2
CURSORS
HOLD
TIME/DIV
EXT CLOCK
EXT TRIG
PROGRAMMABLE DIGITIZER
7D20
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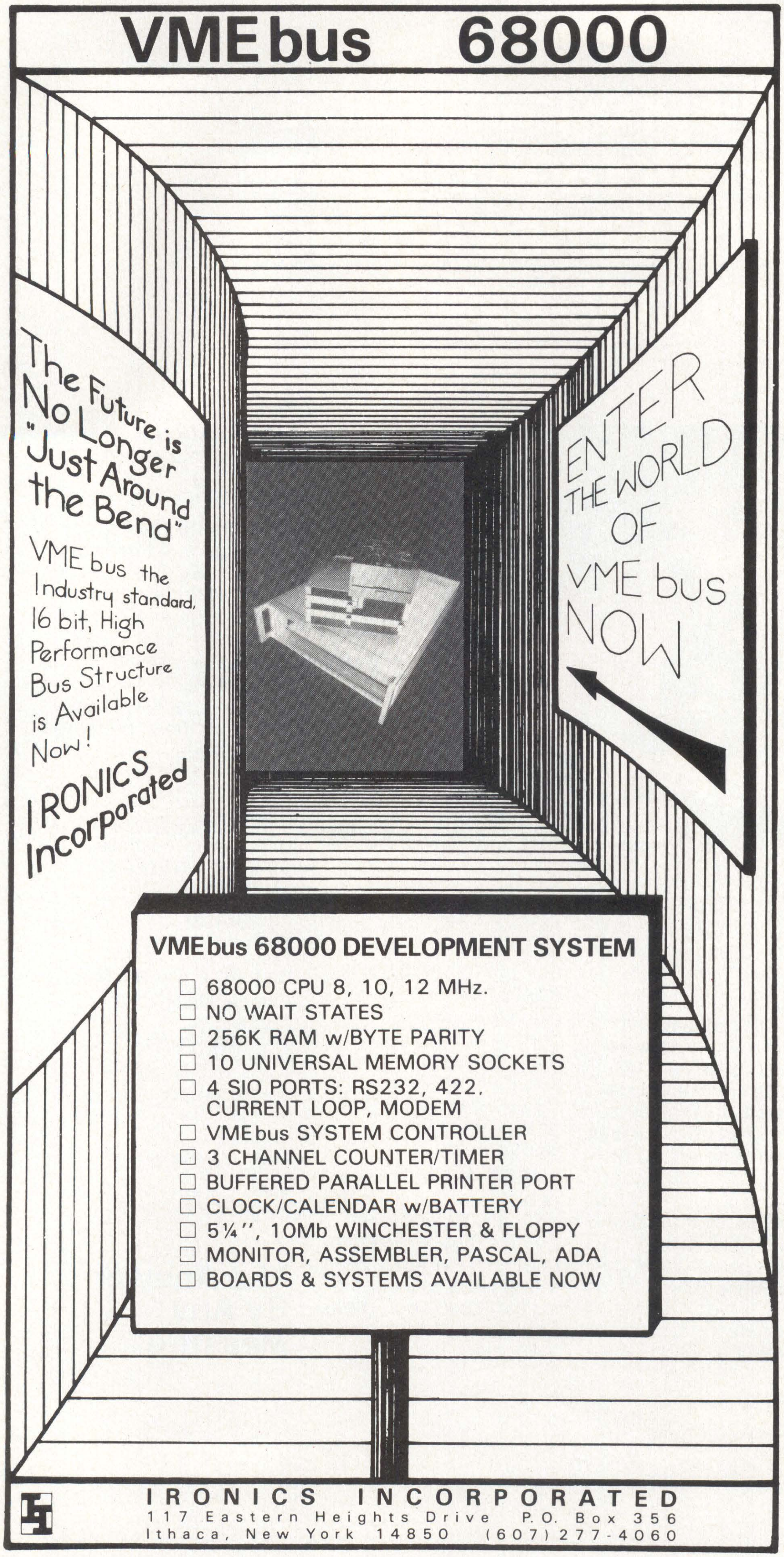

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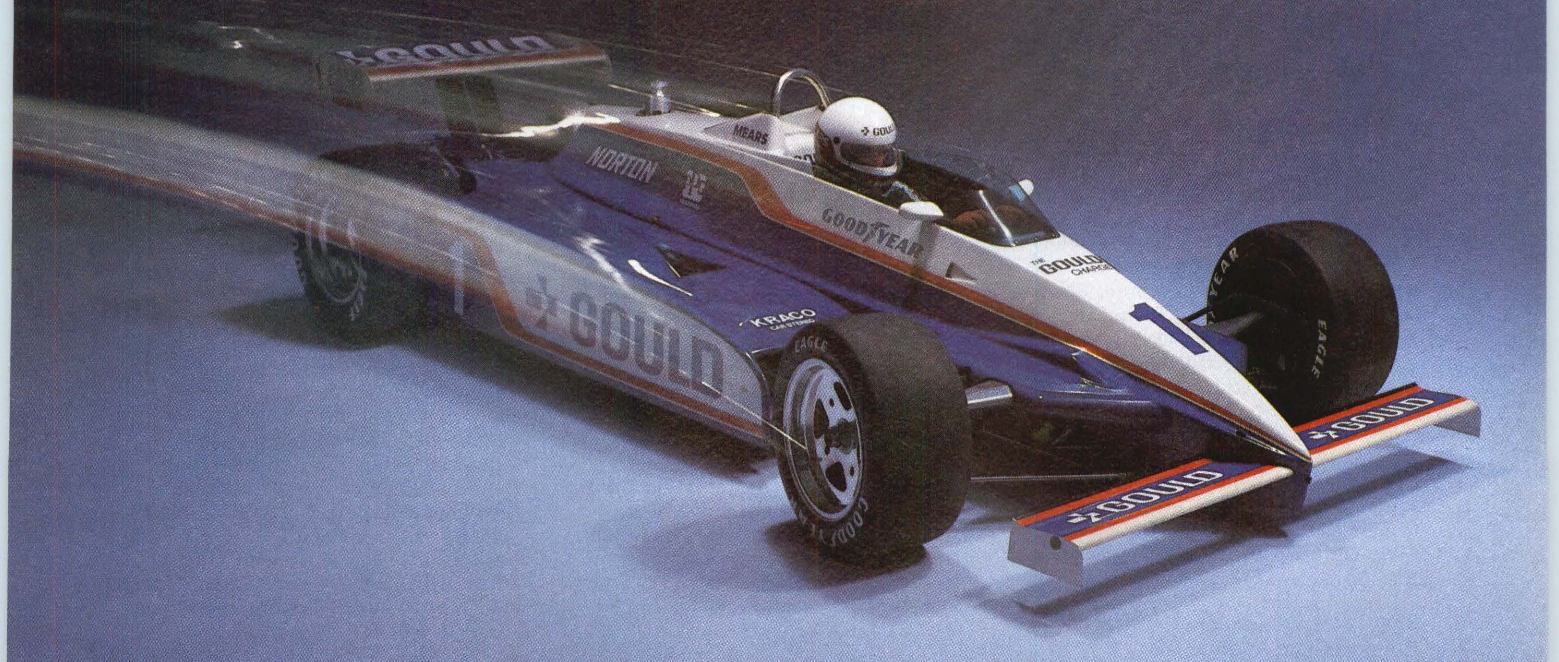
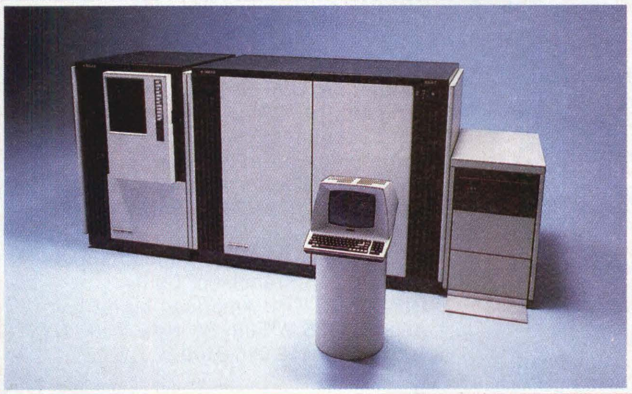
Setting the performance pace... CONCEPT 32/8780.



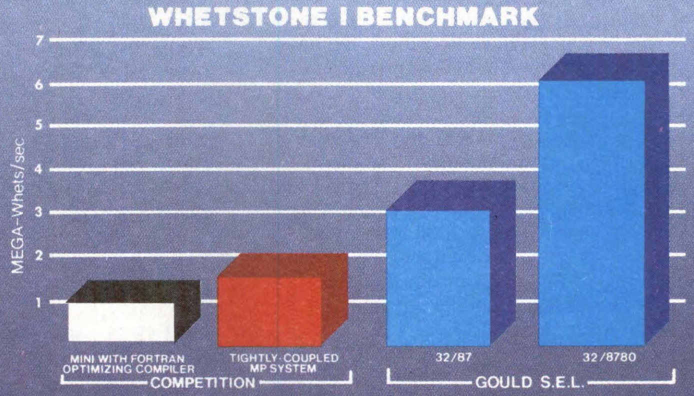
Gould is accustomed to being in first place. In auto racing and in technology. This year, we're doing even better.

Introducing the Gould CONCEPT 32/8780. A true performance champion. A 32-bit superminicomputer so powerful, it not only out-performs the competition, it passed the industry leader—our own 32/87.



Just check out the chart to see how significant the lead really is.

You'll also notice that the traditional K-Whet scale just wasn't adequate for displaying the operation of the 32/8780. Our strength needed measurement in millions, not just thousands.



Results were achieved using system configurations equivalent to those described in published benchmark data and the software tools methodology available as standard Gould S.E.L. products.

At Gould S.E.L., we're not merely keeping pace. We're setting the pace. We know that once we've reached the limits, it's time to set new ones. Challenge us to meet or beat your limits. We'll benchmark Gould CONCEPT 32/8780 performance against any 32-bit minicomputer. And win.

To learn more about our winning attitude, call or write:

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6901 West Sunrise Boulevard, Fort Lauderdale, Florida 33310. 1-800-327-9716.

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Electronics & Electrical Products

CIRCLE 11

CONFERENCES

DEC 7-9—Computers in Science, Conrad Hilton, Chicago, Ill. INFORMATION: Scherago Assocs, Inc, 1515 Broadway, New York, NY 10036

DEC 7-9—DEXPO/West (DEC-Compatible Industry Expo), Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: Lawrence Hollander, Expoconsul Internat'l, Inc, 19 Yeger Rd, Cranbury, NJ 08512. Tel: 609/799-1661

DEC 9-12—Southeast Computer Show & Office Equipment Expo, Civic Ctr, Atlanta, Ga. INFORMATION: Computer Expos, Inc, PO Box 3315, Annapolis, MD 21403. Tel: 301/263-8044; 800/368-2066 (outside Md)

JAN 17-19—CADCON (Computer Aided Design Conf), Disneyland Conv Ctr, Anaheim, Calif. INFORMATION: Robert A. Poggi, Morgan-Grampian Expo Group, 2 Park Ave, New York, NY 10016. Tel: 212/340-9700

JAN 18-20—Southcon, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Eileen Algaze, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

JAN 21-23—CP/M Internat'l Expo and Conf, Moscone Ctr, San Francisco, Calif. INFORMATION: Northeast Expos, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

JAN 31-FEB 2—Communication Networks Conf and Expo, The Rivergate, New Orleans, La. INFORMATION: Louise Myerow, CW Conf Mgmt Group, PO Box 880, 375 Cochituate Rd, Framingham, MA 01701. Tel: 617/879-0700; 800/225-4698 (outside Mass)

FEB 21-23—Office Automation Conf, Civic Ctr, Philadelphia, Pa. INFORMATION: AFIPS, 1815 N Lynn St, Arlington, VA 22209. Tel: 703/558-3614

FEB 23-25—ISSCC (Internat'l Solid State Circuits Conf), Sheraton Center Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 28-MAR 4—Compcon Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 8-10—Localnet, London, England. INFORMATION: Online Confs Ltd, Argyle House, Northwood Hills, HA6 1TS, Middx, U.K. Tel: Northwood 09274/28211; 44/9274 28211 (internat'l)

MAR 10-12—Internat'l Computer Color Graphics Conf, Tallahassee-Leon County Civic Ctr, Tallahassee, Fla. INFORMATION: Ron Spencer, 555 W Pensacola St, PO Box 10604, Tallahassee, FL 32302. Tel: 904/487-1691

MAR 14-16—Phoenix Conf on Computers and Communications, Phoenix, Ariz. INFORMATION: Gerald Fetterer, GTE Automatic Electric Lab, 2500 W Utopia, Phoenix, AZ 85027

MAR 21-24—Interface, Miami Beach Conv Ctr, Miami Beach, Fla. INFORMATION: The Interface Group, 160 Speen St, PO Box 927, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

MAR 22-23—Office Automation Conf and Expo, Holiday Inn Mövenpick Hotel, Zurich-Regensdorf, Switzerland. INFORMATION: Foreign Commercial Service, American Embassy, PO Box 1065, CH-3001, Bern, Switzerland. Tel: 031/437011

APR 5-8—Communications Tokyo, Tokyo Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak Internat'l, PO Box 70007, Washington, DC 20088. Tel: 301/657-3090

APR 19-21—Electro, New York Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Eileen Algaze, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 19-21—Mini/Micro-Northeast, New York Conv Ctr, New York, NY. INFORMATION: Eileen Algaze, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965; 800/421-6816 (outside Calif)

APR 27-29—Satellite and Computer Communications Internat'l Sym, Versailles, France. INFORMATION: T. Bricheteau, Secrĕtariat du Symposium, Domaine de Voluceau, Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France. Tel: 3/954.9020; Poste 600

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

SEMINARS

DEC 15-17—Introduction to Network Architectures, Miyako Hotel, San Francisco, Calif. INFORMATION: Systems Technology Forum, Inc, 9000 Fern Park Dr, Burke, VA 22015. Tel: 703/425-9441; 800/336-7409 (outside Va)

JAN 10-12—Error Correcting and Detecting Codes with Applications to Computer Systems Design, Palo Alto, Calif. INFORMATION: Hellman Assocs, Inc, Dept R, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

MAR 7-11—Computer Aided Engineering and Manufacturing Seminars and Exhibition, North Carolina State Univ, Raleigh, NC. INFORMATION: R. L. Edwards, Industrial Extension Service, North Carolina State Univ, PO Box 5506, Raleigh, NC 27650. Tel: 919/737-3470

MAR 21-23—Digital Control, Boston, Mass. INFORMATION: Hellman Assocs, Inc, Dept R, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

SHORT COURSES

DEC 6-10—Design and Measurement for Control of emi, San Francisco, Calif. INFORMATION: Don White Consultants, Inc, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030

DEC 13-17—Digital Continuous-System Simulation, Univ of Maryland, College Park, Md. INFORMATION: Marc Rosenberg, UCLA Extension Continuing Ed in Engineering and Math, 6266 Boelter Hall, Los Angeles, CA 90024. Tel: 213/825-1047

FEB 14-18—Database Concepts and Design, San Francisco, Calif. INFORMATION: American Mgmt Assocs, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

FEB 15-18—Peripheral Array Processors for Signal Processing and Simulation, Univ of California, Los Angeles. INFORMATION: Marc Rosenberg, UCLA Extension, Continuing Ed in Engineering and Math, 6266 Boelter Hall, Los Angeles, CA 90024. Tel: 213/825-1047

MAR 30-31—IEEE VLSI Test Workshop, Bally's Park Place Casino Hotel, Atlantic City, NJ. INFORMATION: Jerry Kunert, Naval Air Engineering Ctr, Code 92A32, Lakehurst, NJ 08733. Tel: 201/323-2663

METHEUS OEM GRAPHICS

392 FEWER THINGS TO GO WRONG

The Metheus Ω400 Display Controller gives you 1024 × 768 pixel resolution, one million pixels/second vector drawing speed, choice of 4 or 8 bit planes, plus a full complement of graphics features.

In a compact OEM package. At a compact OEM price. Quantity 100 pricing as low as $8,385 makes the Ω400 cost effective for a wide range of applications from CAD/CAM to computer animation.

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Exceptional reliability was a primary Ω400 design goal. We've used 64K RAMs and other advanced VLSI components to produce a design so efficient it (conservatively) uses nearly 400 fewer chips than the nearest performance competitor.

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Compare these specs.

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METHEUS

Dependable by Design

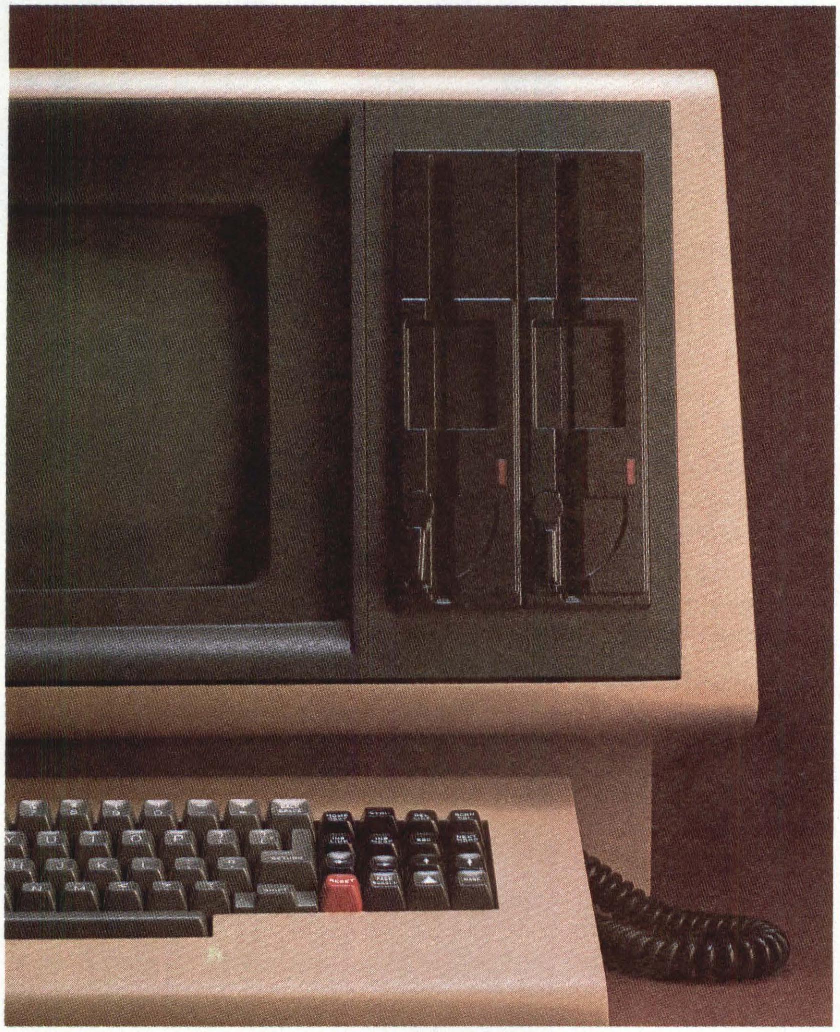
CIRCLE 12

OUR NEW 8" DRIVES PUT US IN A TIGHT SPOT.

They're half the height of a conventional 8-inch floppy.

The exact depth of a standard 12-inch CRT terminal.

And actually capable of squeezing 8-inch drive performance into desktop systems that haven't room for full size 8-inch drives.



What's more, they're Shugart's newest family members—our SA810 single-sided and SA860 double-sided floppy disk drives.

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They also offer a bundle of features not found in conventional 8-inch drives.

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THE iAPX86 FAMILY HAS IT ALL TOGETHER. NOW.

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CIRCLE 14

Crossed Signals

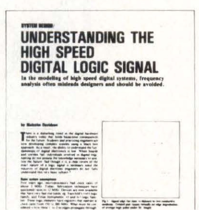
In the May edition of your magazine you published an article entitled "Borrowing rf Techniques for Digital Design." Having spent many years studying the electromagnetic field aspects of digital systems, I cannot agree with the author.

I have found rf network analyzers to be of little use and, in fact, they often confuse the issue for the unwary engineer. There is also the philosophical point of whether Fourier analysis can be used on a realtime digital signal.

For example, is it useful or even realistic to consider a 0, for a long time prior to an event, to be represented by an infinite series of sine waves? It seems logical that if our system can be characterized by two cases, a positive and a negative going step, then all types of digital signals, regardless of a particular repetition rate, have been covered. This precludes the concept of frequency, which infers a certain speed or rate.

Malcolm F. Davidson
Heaviside Industries, Ltd
56B Wedgewood Rd
Stratford, CT 06497


BORROWING RF TECHNIQUES FOR DIGITAL DESIGN


UNDERSTANDING THE HIGH SPEED DIGITAL LOGIC SIGNAL

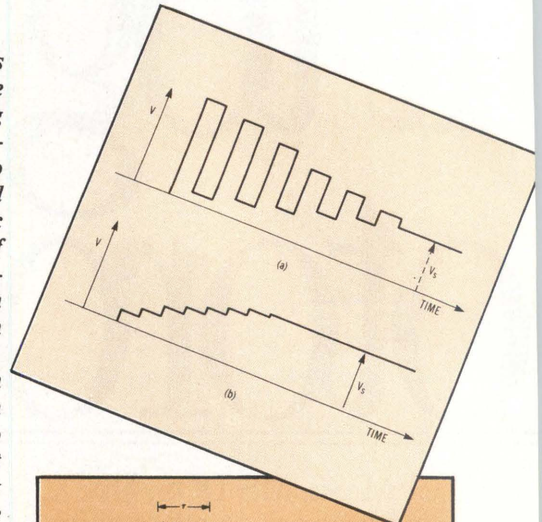
Deciphering digital signals

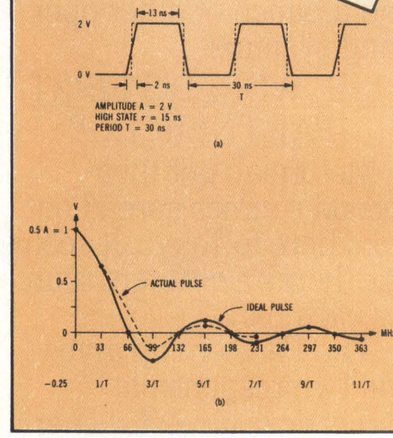
In response to Malcolm Davidson's letter, Fourier analysis is an appropriate and straightforward way of analyzing digital signals. Virtually all digital components and pathways are designed to handle an alternating stream of 1s and 0s, ie, a square wave. Since any periodic wave can be represented by a number of harmonically related sine waves, frequency domain or Fourier analysis can give the designer valuable information about a circuit's performance.

Mr Davidson rejects frequency domain analysis because it "infers a certain speed or rate." I beg Mr Davidson to find me a circuit within a computer that does not operate at a specified clock rate! Analyzing a positive or negative going voltage step as if it were isolated in time may be an interesting theoretical exercise, but it is not representative of an operating circuit.

Thank you for allowing me to reply to Mr Davidson's letter. I look forward to reading his article in the November issue.

David S. Montgomery
Hewlett-Packard Co
1400 Fountain Grove Pkwy
Santa Rosa, CA 95404





Readers intrigued by this philosophic debate on the nature and essence of digital logic signals should read the article beginning on p 79 of this issue.

More on the Tower of Babel

I read with interest your editorial entitled "The Tower of Babel Revisited," (Aug 1982, p 11). In reference to it, I would like to make the following comments: I agree that applications software must be improved to take advantage of all "the hardware being churned out." I do not agree, however, that "nonworking hardware is a lot easier to detect than nonworking software." Unless, of course, you are in the hardware business. For me, the opposite is true.

To serve as large a market base as possible, applications software must be designed to be general purpose: it must be easy to customize, to meet the varied needs of all those first-time, nontechnical users; to make it cost-effective for the manufacturer, it had better be inexpensive to maintain. I also agree that the kinds of customers purchasing inexpensive systems have no choice but to demand software that caters to their specific needs (real or imagined). In all fairness, it must be said that control hungry programmers are very often merely responding to "feature" hungry customers. They are just a little misguided in how they go about it, that's all.

"Most terminal manuals do not explain, in plain language, just what control codes make the terminal do its wonderful things." Hear! Hear! "Plain language and friendliness" are in the eye of the beholder. CTRL-U is very plain to me, not because I am a demented office efficiency expert, but because I use these tools everyday. Typing ESC-UP a few hundred times per day is not fun. Furthermore, I challenge you to find two people that can agree on which is the better way. We have been marketing a full-screen editor for over a year, and have found no agreement among our customers on that matter. On the other hand, I would also say that the novice or casual user should have the option to use the verbose version if he/she so wishes.

Finally, we have found that coming up with the software is the easy task in successfully marketing a package, while making people aware of these packages is the really hard part. I suspect what is lacking is the widespread motivation for this type of software. The prevailing attitude from software developers is first, "What are you talking about?" and then, "Who needs that when my special purpose front end can do it faster and in less memory?" End users do show a bit more enthusiasm, but only a little more. The response that has most stuck in my mind came from a potential distributor who asked, "How do you sell that?" I am keeping my fingers crossed that yours is just the first of many demands for effectiveness over efficiency, and flexible and friendly interfaces instead of clever (?) ones.

Matt M. Perez
Information Nexus, Ltd
6272 W North Ave
Chicago, IL 60639

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Better reliability. Closed-loop servo with imbedded digital servo (**DigiLok**™) ensures cartridge interchangeability while allowing variable sectoring. **Chromaflux**™ graphite coated thin film metallic alloy discs protect against contamination. No long purge cycle required.

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It Fits.

CIRCLE 15

LETTERS TO THE EDITOR

An accusation

An article by Mr Henry Davis (Aug 1982, p 103) has been called to my attention. I do not read this magazine, hence, I did not see the article when it was published.

I wish to point out to you that Mr Davis plagiarized my work, almost word for word. Oblique reference was given in Table 2 and the bibliography; however, my name was misspelled. A drafting error in my paper was even copied directly into Fig 4 of Mr Davis' article.

Based on this introduction to your publication, I now know why I do not read it.

Harvey Cragon
Texas Instruments
13500 N Central Expressway
Dallas, TX 75266

A rebuttal

The analysis of the different pure computer architectures contained in my article is based on theoretical work done in 1978 by myself for "Comparing Architectures of Three 16-bit Microprocessors" published in Computer Design *(July 1979, p 91). Since Mr Cragon's paper contained several simplifying assumptions that would enhance reader understanding and had little impact on the validity of my own analysis, I elected to use it as a reference for this article. Since I did follow Mr Cragon's derivation in my manuscript, full, explicit credit was given to him. I also elected to use Mr Cragon's figure with credit since it showed very similar results to my own.*

Unfortunately, during editing, credits to Mr Cragon and Harold Stone as originators of several figures and general approaches were removed by the staff of Computer Design.

Finally, it is my responsibility that Fig 4 was reproduced with the errors and Mr Cragon's name was misspelled. I apologize for these errors.

Henry A. Davis
SOLOSystems, Inc
482 Oakmead Pkwy
Sunnyvale, CA 94086

An explanation

Computer Design's *editors did delete the specific credits to Mr Stone for Figs 6 and 7, although his article was listed in the bibliography. However, credits to Mr Cragon for Table 2 and Fig 4 were published exactly as in the manuscript received from Mr Davis. The editors of* Computer Design *sincerely apologize to both Mr Cragon and Mr Stone for the unfortunate action.*

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Intelligent, high performance Ethernet controllers make the critical difference in how well your computer performs on the network. We can prove it.

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It stands to reason that in an Ethernet installation, the burden on your host CPU will be increased. Because large amounts of information must be moved quickly and shared among the network's users. That's when high performance, intelligent controllers make complete sense.

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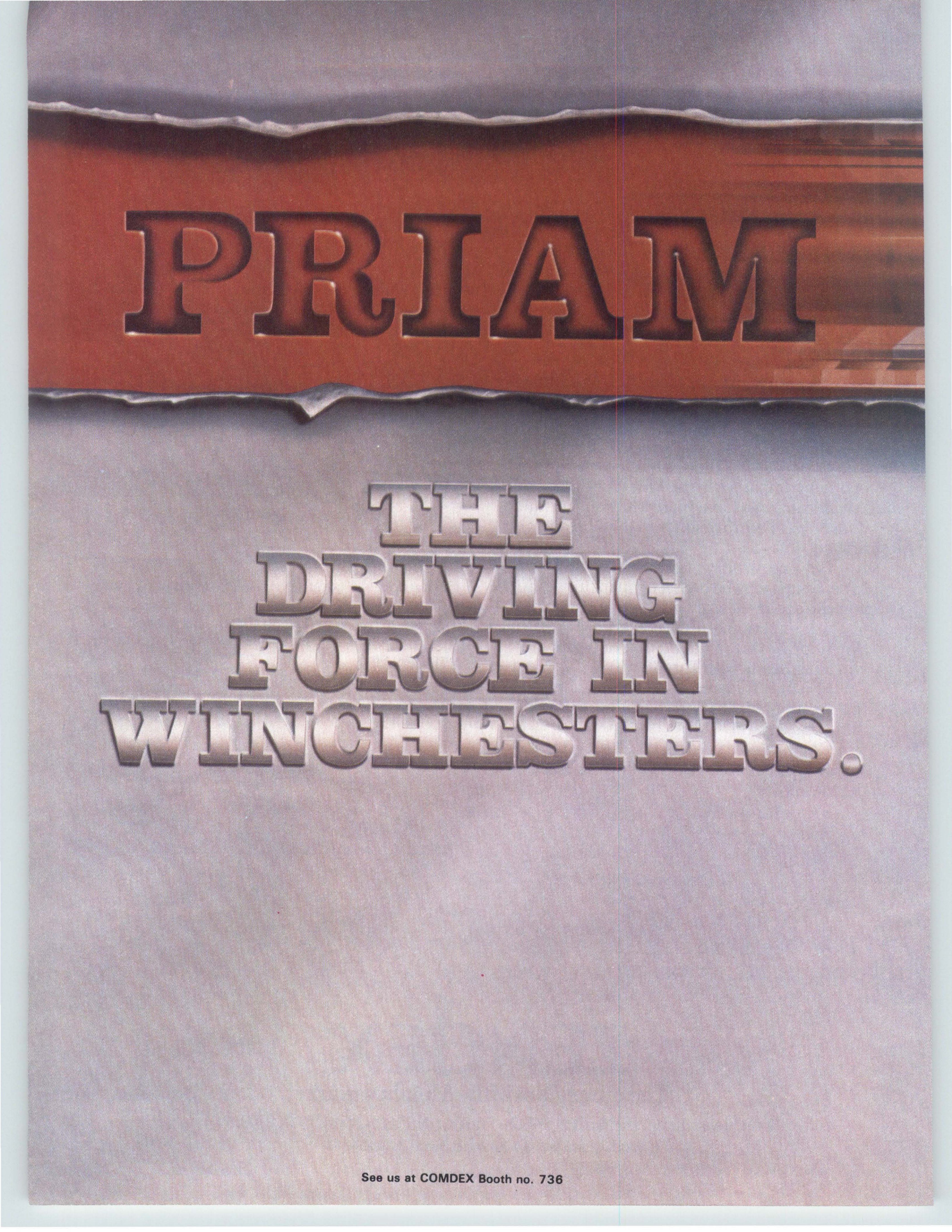
CIRCLE 17

Who is winning the battle of the Multibus Giants?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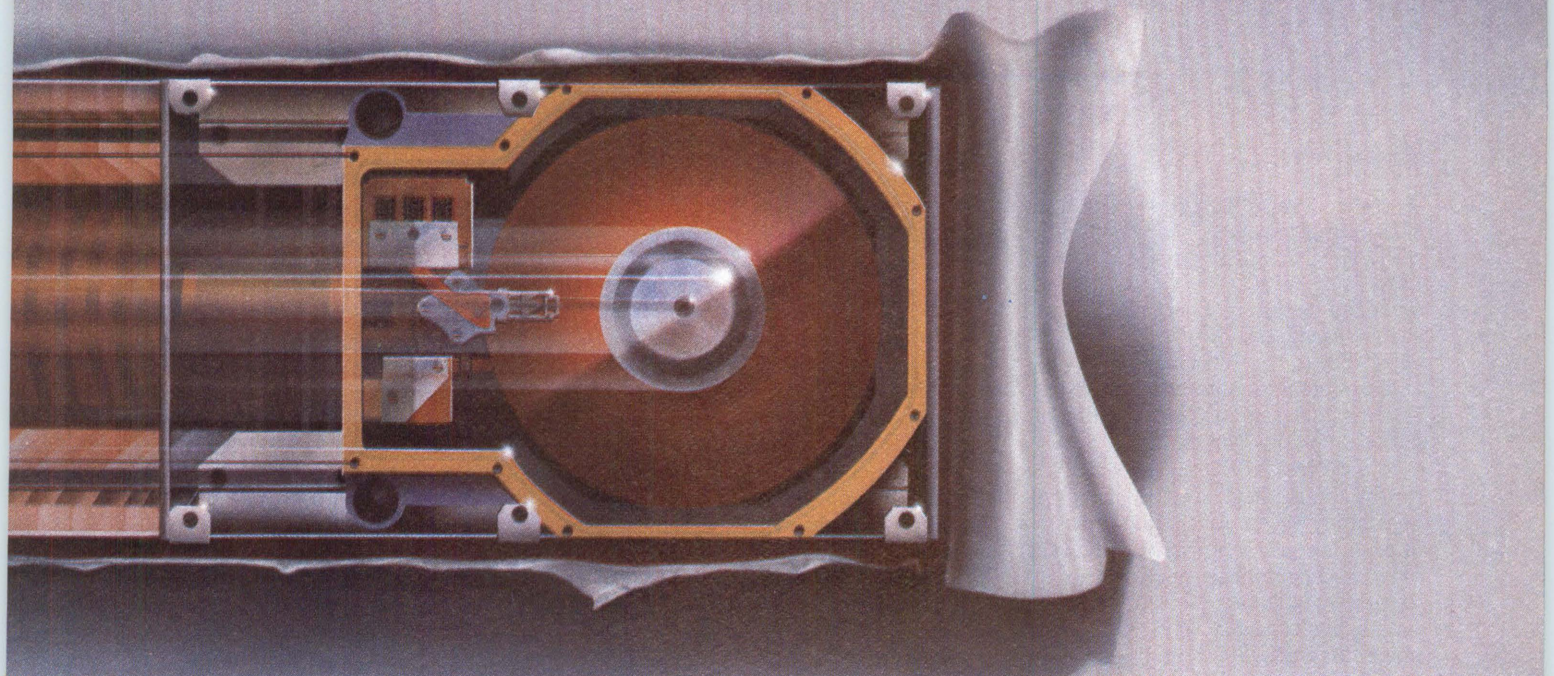

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A growing family of winners. From the beginning in 1978, PRIAM has been the driving force in high-end Winchester technology. We've proven our technology in the 14-inch Winchester market with our 34, 68 and 158 Mbyte units. Our 8-inch drives have capacities of 35, 70 and 105 Mbytes in a floppy-sized package. And, we're adding a 50 Mbyte 5¼-inch drive to our growing family.

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Size	Model	Capacity (MB)	Access Time
14″	3350	34	45 ms
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	15450	158	45 ms
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	7050	70	42 ms
	804	105	42 ms
5¼″	502	50	35 ms

SMART Interfaces. PRIAM gives you the finest in interfacing flexibility. Our intelligent interfaces can control up to four drives in any mix, plus tape or floppy backup. They're your fastest and easiest route to putting a Winchester database in your system. Or, if you have an SMD or ANSI controller, our drives can be supplied with a matching interface.

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CIRCLE 19

Single-chip VLSI processor promotes realtime control

A higher level of integration than ever before achieved in a single-chip controller is claimed by Intel Corp for its iACX-96 family. The 16-bit microcontrollers contain over 120,000 transistors each, and Intel says that they offer better performance than most 16-bit multichip, microprocessor based systems. CPU and I/O are tightly integrated functionally onchip.

The devices are designed specifically for the control field, whether in a printer or plotter, automotive braking system, or data acquisition system. However, inherent capabilities probably offer most to applications where the controllers can interface with any of a broad range of transducers and sensors for precision data acquisition and process control. The 16-bit performance particularly favors robotics or other realtime applications where extra accuracy is needed.

Rated 10 times faster than its 8048 predecessor, the iACX-96 microcontrollers have 8 times more program memory, 3 times the data memory, higher speed I/O ports, serial channels, onchip counter timers, A-D converters, and high math capability. They have a 12-MHz input frequency and can perform a 16-bit addition to 1.0 μs, and a 16- x 16-bit multiply or 32/16-bit divide in 6.5 μs. In typical applications, instruction execution times are expected to average 1 to 2 μs.

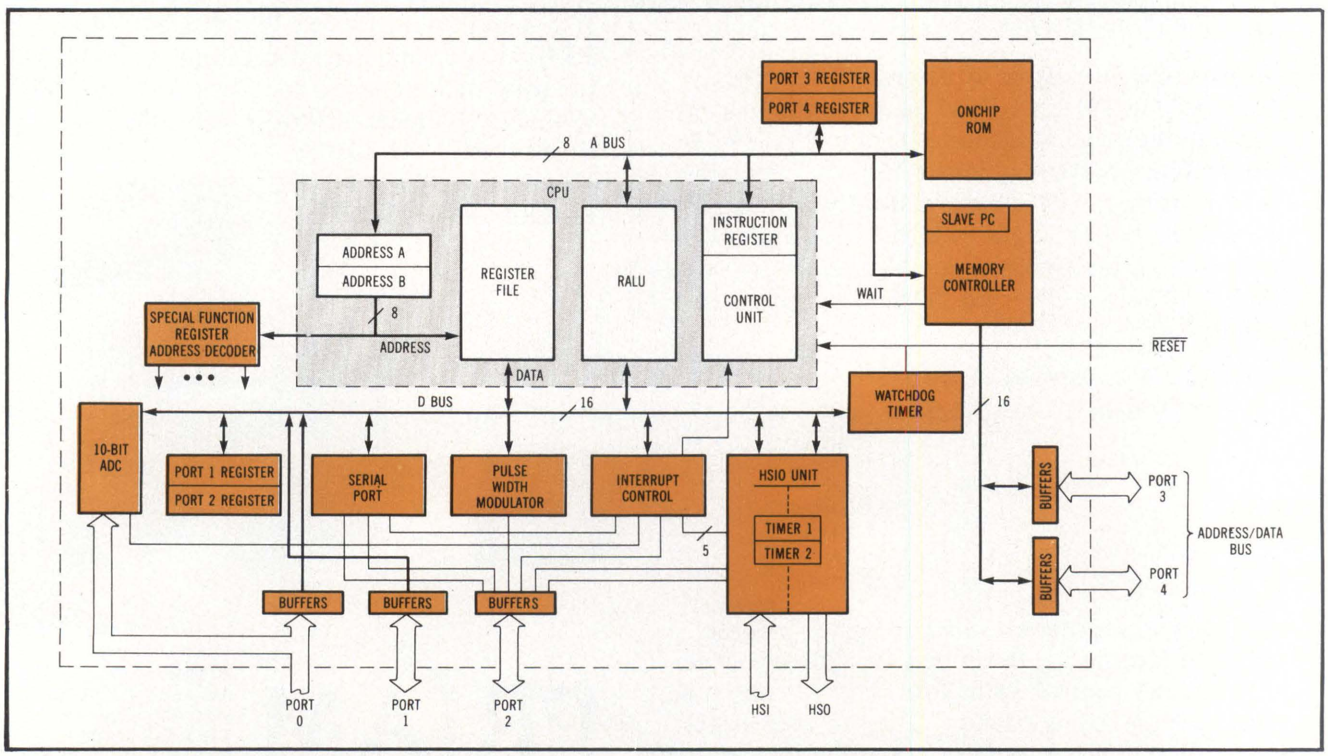
Two devices—the 8096 and the 8396, which is an 8096 with 8k bytes of ROM onchip—will be available initially. Both will be offered in 48- and 68-pin versions. A 10-bit, successive approximation A-D converter with eight multiplexed channels will be optional on 68-pin devices. An 8796 EPROM version will be available in the future.

Four high speed trigger inputs record the times that external events occur, and six high speed pulse generator outputs trigger external events at preset times. The high speed output unit can simultaneously perform timer functions. Up to four such 16-bit software timers can operate simultaneously.

Internal data transfers are handled in a 16-bit data bus (D bus) and an 8-bit address bus (A bus) dual-bus structure, as shown on the simplified block diagram. Internal registers occupy lower addresses; communication with higher memory locations is through the A bus and the memory controller. Instruction and data bytes are also carried by the A bus. Identical address space is used for program and data memory. Instructions can be executed from any memory address except internal RAM.

The memory controller maintains a 3-byte instruction queue for the instruction register. Addresses for instruction fetches are maintained in a slave program counter (PC) residing in the memory controller. After each instruction fetch, the slave PC is incremented and updated by the CPU when program jumps are executed. Data access addresses are assembled from the 8-bit bus into a 16-bit data address register within the memory controller. Accesses to offchip memory are through the multiplexed address/data bus.

CPU and I/O are functionally integrated. The CPU includes a register file, a register arithmetic logic unit (RALU), and a control unit. The register file contains 232 bytes of RAM as bytes, words, or double words. Users can keep the most commonly used variables in fast access, onchip RAM. The RALU consists of a 17-bit ALU, the program status word, the program counter, multiply and divide hardware, and temporary registers. Main control section components are the *(continued on page 32)*



Simplified block diagram of 8396 16-bit microcontroller. Memory to memory architecture is organized around dual buses. Five 8-bit I/O ports include input only (port 0), quasi-bidirectional I/O (port 1), multifunction (port 2), and two bidirectional (3 and 4).

Single-chip VLSI processor
(continued from page 30)
instruction register and the programmable logic array.

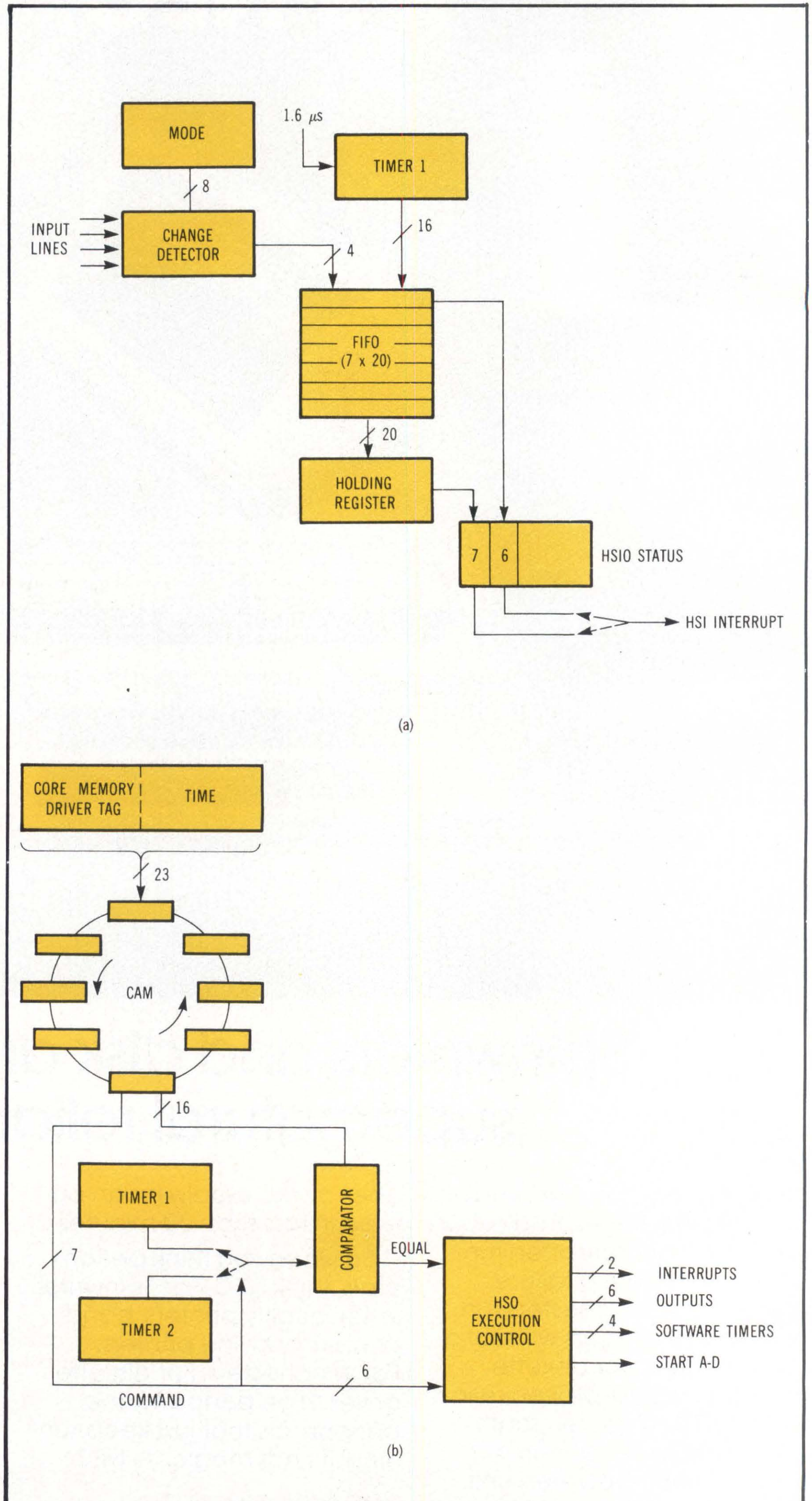
All I/O processing is via a high speed I/O unit (HSIO) containing two timers. (See functional diagrams.) Within this master unit, a high speed input (HSI) unit looks for transitions in input lines and records the time and line making the transition. This information is stored in an 8-deep FIFO. The unit can be programmed to look for either positive or negative transitions, and to activate the HSI data available interrupt when the first or seventh entry to the FIFO is made. The HSI unit has four input lines, two of which are shared with the high speed output (HSO) unit. Each input line can be software enabled or disabled. The HSO unit can be programmed to cause transitions on any output line at specified times, or to set or clear any output line, reset a timer, or trigger an A-D conversion at a preset time.

HSO commands are stored in an 8-deep content addressable memory (CAM) file. Each CAM register is 23 bits wide; 16 bits specify the time an action is to occur and 7 specify the nature of the action and which of the two timers is referenced. The CAM file rotates one register position per state time. Time resolution of the HSO unit is eight state times (2 μs if the oscillator frequency is 12 MHz). It takes eight state times for a holding register to access all eight CAM registers; similarly, it takes eight state times for the comparator to obtain access to all eight CAM registers.

A full-duplex serial I/O channel enables several microcontrollers to be daisy chained. The full-duplex port is compatible with the MCS-51 serial port. Receive buffered, it can receive a byte before a previously received byte has been read from the receive register. High level languages that support the 8096/8396 microcontrollers are of particular value for industrial control applications. FORTH and C will be available first and PL/M will follow.

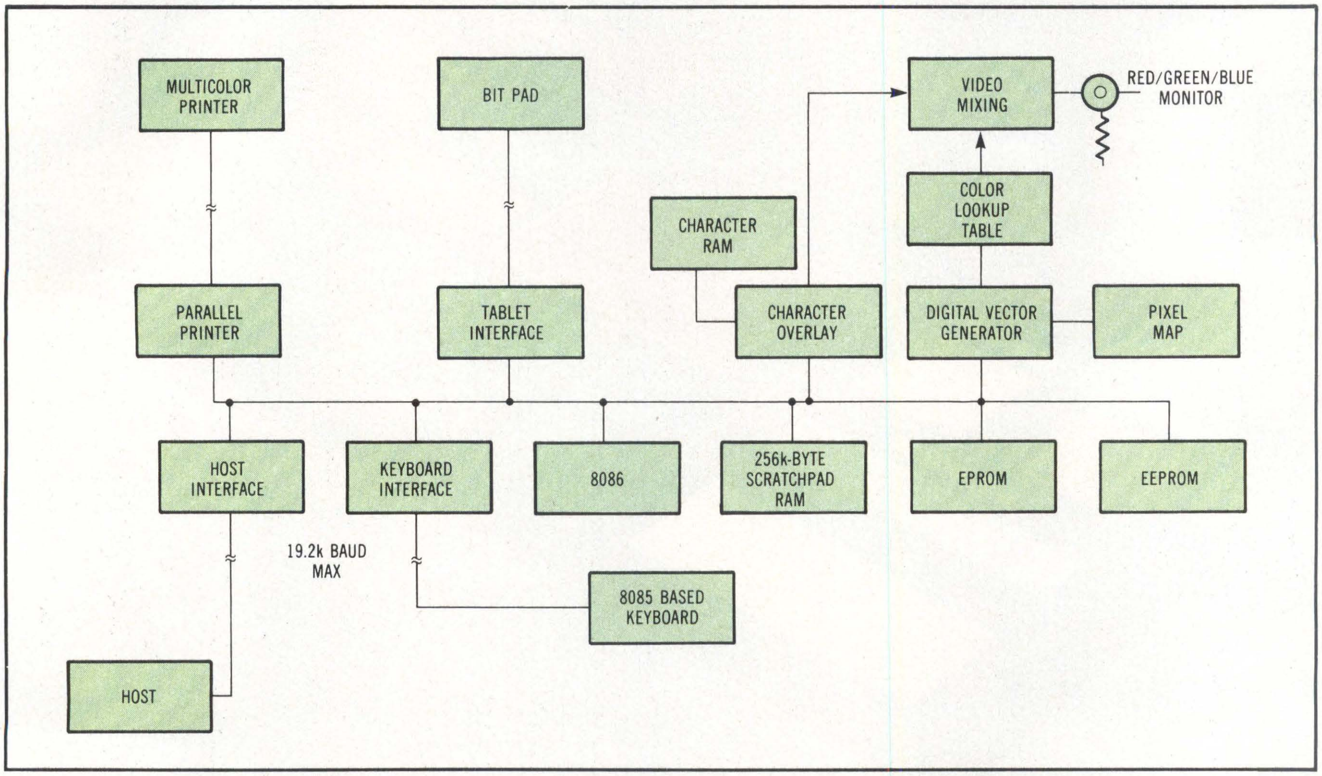
Evaluation units of the microcontrollers are now in use. Production quantities are planned for the first quarter of 1983. Probable prices for up to 24 units will be $58 for 68-pin devices and $50 for 48-pin versions. In 10,000-unit quantity, the basic 8096 will have a U.S. price of $15 each. (By 1985, the large quantity price is predicted to be under $10 and $6 each for the 68- and 48-pin versions, respectively.) **Intel Corp,** 5000 W Williams Field Rd, Chandler, AZ 85224.

—Syd Shapiro, Managing Editor, and Douglas Eidsmore, Senior Editor
Circle 240



Functional diagrams of 8096/8396 HSI and HSO units. HSI unit (a) sees input line transitions and stores input line number and transition time in 8-deep FIFO. Unit can be programmed to activate HSI data available interrupt. HSO unit (b) can be programmed to cause output line transitions.

Workstation compresses graphics functions onto single board



Processing for Whizzard 1650 raster graphics terminal is distributed and shared by various dedicated chips. While 8086 forms main processor, other circuits handle such functions as vector generation and graphics transformation. A single board contains all circuitry.

Designed for use in engineering workstation applications, the Whizzard 1650 raster graphics terminal by Megatek connects single-board electronics with software compatibility to other members of the Whizzard family. The 1650 is software compatible on the 2-D level with the $50,000 7600 and contains many of that product's options as standard features. In the alphanumeric mode, the 1650 emulates standard VT100 terminal operation. The user can define an alphanumeric window to communicate with the host while using the rest of the screen for graphics work.

Electronics of the Whizzard 1650 are contained on a single circuit board that distributes the processing load among several processors. In addition, the keyboard has its own 8085 processor to handle the interface with joystick and valuator dials. The main processor is a 16-bit 8086. There is a separate digital vector generator that can run at an average speed of 200 ns/pixel. The display is 640 x 480 pixels with 4 bit planes, and a 4096 x 4096 virtual display space; up to 256k bytes of display list memory are also provided. The 1650 can simultaneously display 16 out of 4096 possible palette colors. A 32-row by 80-char overlay is used to overlay graphics information or is confined to a window as a separate editing terminal area.

The combination of microprocessors and firmware allows such operations as 2-D graphics transformations (including rotate, continuous scale and translate, and clip). Firmware supports direct pixel addressing, hardware line texture, blinks, dash, pick, and fill.

EEPROM stores setup parameters for the type printer being used, background color, and diagnostics. A menu of diagnostic routines provides a check of all 1650 functions. There is also a routine that monitors both alpha and graphic communications to and from the host. The user can set up a breakpoint to look for some character of interest and halt when it appears in the data stream.

Whizzard 1650 interfaces with a digital tablet as well as a parallel printer interface. Firmware routines are provided for use with several popular multicolor printers including those made by ACT, Printacolor, and IDS.

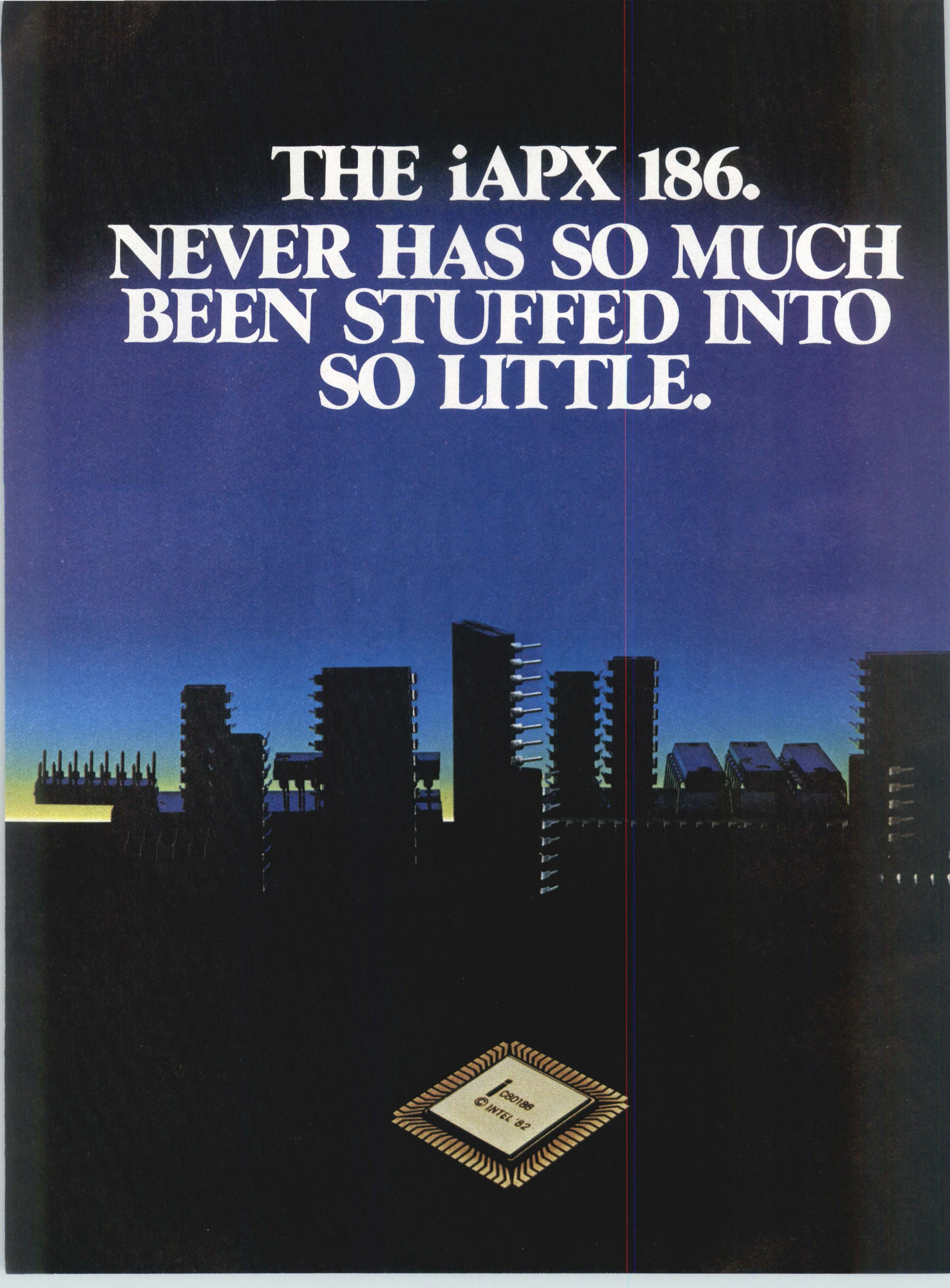
The Whizzard 1650 price starts at $15,900. **Megatek Corp**, 3985 Sorrento Valley Blvd, San Diego, CA 92121. **Circle 241**

Minicomputer users gain access to CP/M software with coprocessor boards

Expanding the repertoire of minicomputers to include programs running under CP/M, Virtual Microsystems Inc has announced a Z80 based coprocessor for Digital Equipment Corp's VAX-11, PDP-11, and LSI-11 systems. Computer Automation has a similar Z80 coprocessor for its OMNIX network workstations. Users will benefit from the vast library of CP/M applications software without being limited by resources like line printers, disk drives, and main memory. With either configuration, the coprocessor appears as an I/O peripheral to the operating system and CP/M as an application program.

Actual implementation of the Z80 coprocessor differs: Computer Automation (CA) set aside 64k bytes of the total 128k bytes in main memory for CP/M and application programs, with the board performing as a DMA device. Virtual Microsystems Inc (VMI), on the other hand, provides 64k bytes of onboard memory for each Z80. UNIBUS *(continued on page 40)*

ANNOUNCING THE BIGGEST LITTLE BREAKTHROUGHS IN 16-BIT TECHNOLOGY.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Introducing the biggest, little thing in 16-bit technology today.

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Perfected through HMOS III technology, the 186 is a remarkable microprocessor that handily integrates 15-20 LSI chips.

More remarkably, the 186 is available now. At a price that's a small wonder in itself.

There isn't another processor around with as high a level of integration. The 186 brings together almost all the functions of a CPU board.

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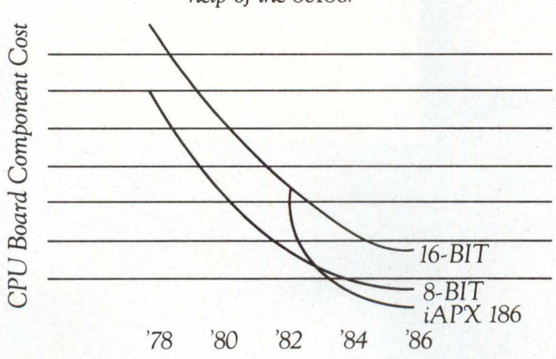
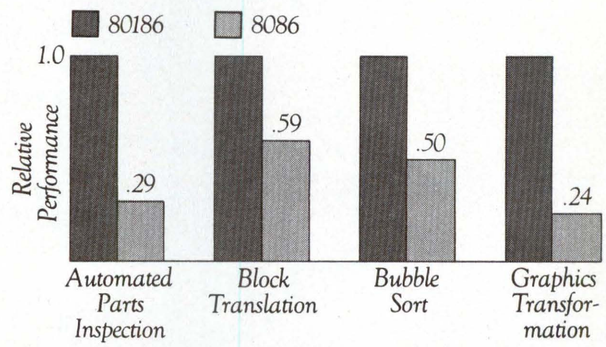
Incredibly, the 186 does all this in production volume for just $30. Or in hundred unit quantities for $50. That's less than half the cost of the chips it replaces.

Which means if you've been settling for less performance to save money, now you can't afford not to step up to 16-bits.

A comparison of CPU board component costs shows that 16-bit performance can be purchased at 8-bit prices with the help of the 80186.



Benchmark results measuring the standard (5 MHz) 8086 vs. the standard (8 MHz) 80186 show an overall performance increase of approximately 2.0.



Worried about software? Don't be. Because its software is totally compatible with Intel's iAPX 86, 88 family, the 186 is immediately supported by the largest base of 16-bit software in the industry.

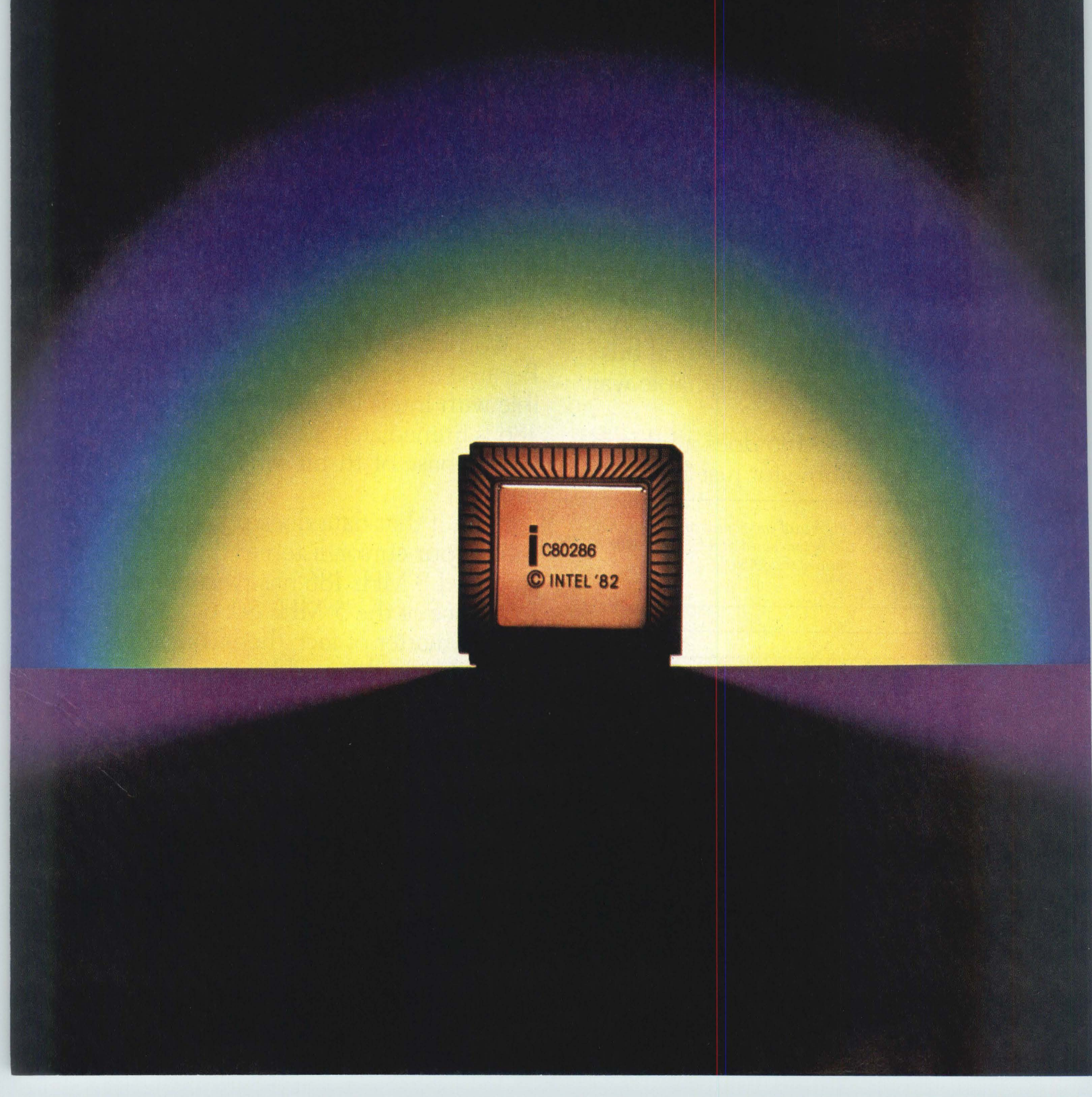
Now, if that data doesn't make you move your cursor, listen to this. The standard 8 MHz 186 has twice the performance of the 5 MHz 8086.

As a matter of fact, there's only one other chip in the world faster than the 186.

You'll read about it on the next two pages.

The Intel iAPX 186. It's no big thing. Just a minor miracle.

AND OUR iAPX 286. ITS PERFORMANCE IS OVERPOWERING.



Introducing the processor that can outperform, outclass any microprocessor.

Anywhere.

The Intel iAPX 286.

It gives you three times the performance of what you thought was the fastest chip in the market.

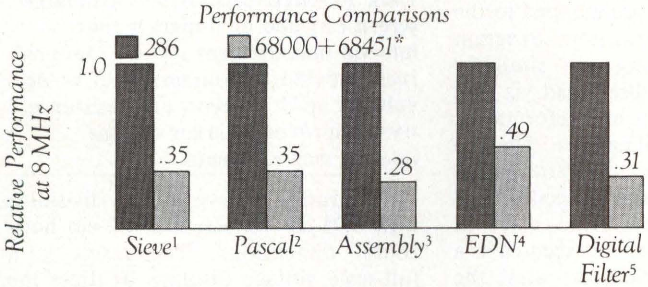
To add more power to the punch, this one has been designed from the beginning to include memory management and protection on chip.

Which means you can design these sophisticated capabilities into your system without the cost, complexity or performance degradation of external hardware.

If 16 Megabytes of physical memory isn't enough, there's a virtual memory capacity of 1 gigabyte per user.

The 286 has been optimized to handle advanced operating systems such as the UNIX* and iRMX™ OS. It also provides new instructions for languages such as Pascal, BASIC, FORTRAN, C and ADA.

Performance Comparisons



*Performance adjusted to reflect indicated system configuration. Details available from Intel. [1] "A High Level Language Benchmark." Byte. Sept., 1981. [2] "A Performance Evaluation of the Intel iAPX 432," Computer Architecture News. June 1982. [3] "16 Bit Microprocessor Benchmark Report," Intel Corporation, 1981. [4] "16 Bit Microprocessor Benchmarks," EDN, Sept., 1981. [5] "Digital Filter Implementation on 16 Bit Microprocessors," IEEE MICRO, Feb., 1981.

And to simplify sophisticated system development even further, there's an integration of performance-critical functions. Such as task switching, interrupt handling and O.S. call, among other things.

A couple more hard facts about software. The 286 is compatible with the iAPX 86, 88. So not only will you have the hottest CPU on the market, but also immediate access to a huge software base.

System Comparisons

	iAPX 286 System	68000 + 68451* System	Advantages of Integrated Memory Management & Protection
Typical System (16 Users)	1 CPU	1 CPU 1-4 MMU's 2 Transceivers 1 MMU Selector	Less Board Space
Wait States Required 8 MHz	0. W.S.	2. W.S.	Higher Performance
Task Switch Overhead	22 μS	>120 μS	Faster Response
Max. BUS Bandwidth at 8 MHz	8 MB/Sec	2.67 MB/Sec	Higher Throughput

*Based on published data sheets.

On the hardware side, the iAPX 286 is a well integrated 16-bit family. It delivers full performance at the systems level, through support circuits like the 8207 DRAM controller and the 80287 floating point numerics processor.

All this allows the Intel 286 to give the ultimate in command performance.

But now, it's your turn to act. Call us toll-free at **(800) 538-1876.** In California, call **(800) 672-1833.** Within 24 hours, we'll send you complete information on the 186 and the 286. Including wall size posters of each part.

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Z80 based coprocessor
(continued from page 34)
versions of the coprocessor board contain four Z80s with 256k bytes of RAM. Q-bus versions can be populated with one to four Z80 processors with associated memory.

The z-Board for DEC computers is a hardware accelerator for VMI's Bridge virtual microcomputer system. Running as a task under the VMS, RSX, RSTS, RT-11, or UNIX operating systems, the Bridge contains a modified version of CP/M. Necessary drivers are provided to handle all I/O, disk storage, printing, and communications functions. This software interrogates the bus for available z-Boards, which are identified with DIP switches as multiple boards that can be supported without changes to the Bridge or resident operating system. Individual Z80 processors are allocated to users on a first come first served basis by the Bridge, with the 64k-byte RAM used as a dedicated workspace for application programs. If a Z80 processor is unavailable, the user is switched to an 8080 virtual machine that simulates the 8080 instruction set in software with performance similar to communicating to the processor over a 1200-bps line. Multiple users running the software simultaneously can create multiple virtual microcomputers to run CP/M if physical processors are already allocated. Free Z80 processors replace the 8080 simulator so that a user's terminal appears as a 4-MHz microcomputer with a Winchester disk drive.

Programs and data are stored on virtual floppies that reside on the system's disk pack and have the structure of a CP/M floppy disk. Each virtual floppy contains up to 64 CP/M files (2M bytes maximum). The host operating system sees each virtual floppy as a single entry in its directory, with the internal organization formatted according to its own format (eg, VMS, RSX). Utility programs read standard single-density 8″ diskettes into the virtual floppies via RX01 or RX02 floppy disk drives and move CP/M files to the host operating system from virtual floppies as well. As such, the Bridge traps disk access and I/O requests from each Z80 and initiates the necessary actions by interrupting the host operating system. For example, requests for printer output automatically create temporary files to store the microprocessor output. Output is either sent to the host spooler or stored in the host directory space for action after leaving the CP/M environment.

The z-Board uses a bit-slice state machine to coordinate activities of the multiple Z80s (each running at 4 MHz) with the system bus. An internal multiplexer handles bus functions like timing control and data transfer between the bit-slice processor and the Z80 processors. The bit slice handles system bus interrupts. Each 64k-byte memory has dual ports for Z80 or bit-slice access.

Memory allocation and access for CA's OMNIX system coprocessor is handled by the OPUS I operating system. The 64k bytes are allocated between the 12k bytes used by the operating systems and I/O buffers located at the upper range of the 128k-byte main memory. According to the company, system main memory is used to simplify coprocessor implementation, as well as reduce board size (the coprocessor fits on a card roughly one-third the size of the DEC quad board used by VMI). Addresses generated by the Z80 are mapped to actual memory locations with offset values so that the Z80 addresses begin at any one of sixteen 8k-boundaries. Data transfers are handled as DMA calls. Interrupts are generated by both the host processor and coprocessor. Wait states are used to synchronize the 4-MHz Z80 with the system clock.

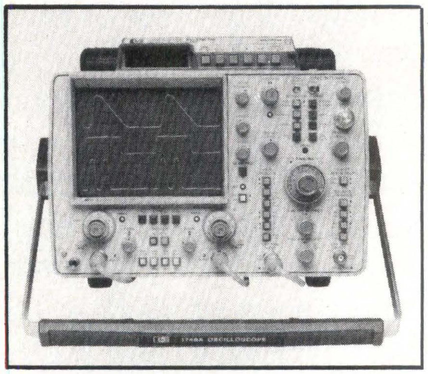
Like the VMI implementation, a modified version of CP/M is used to run application programs as tasks under the host operating system. Disk access and I/O processing routines are written in both Z80 assembly code and native object code so that such requests are mapped to the appropriate OPUS I function. Program loading and handling are similarly treated, with floppy disks read via CDC compatible disk drives and reformatted to meet OPUS I specifications. The file handler also translates the reformatted files into CP/M structures as needed. The CA coprocessor differs from VMI's in that CP/M programs can be executed as a single task by a single user, while the z-Board allows simultaneous execution of multiple tasks by multiple users.

The z-Board is available for $4000 for UNIBUS versions and $1250 to $3500 for Q-bus versions (depending on the number of installed processors). Bridge is priced between $1000 and $3500, depending on the minicomputer used. Price for the Z80 coprocessor and CP/M license is available upon request from Computer Automation. **Computer Automation, Inc, NAKED MINI® Div**, 18651 Von Karman, Irvine, CA 92713. **Virtual Microsystems Inc**, 2150 Shattuck Ave, Suite 720, Berkeley, CA 94704.
Computer Automation—**Circle 242**
Virtual Microsystems—**Circle 243**

TEST & MEASUREMENT

Oscilloscopes have 43% larger displays for higher resolution and accuracy

Designed with substantial measurement features to meet the requirements of laboratory, production, and field environments, Hewlett-Packard's (HP) 1745A and 1746A 100-MHz oscilloscopes feature display areas 43% larger than standard. The display measures 9.5 x 12 cm as opposed to the conventional 8- x 10-cm size. This improves visual resolution and measurement accuracy, particularly in 3-channel displays that use trigger view. The 1746A incorporates a proprietary dual-marker system to increase speed and accuracy of time interval measurements.



1746A 100-MHz oscilloscope with large screen CRT and dual-marker time interval measurement system. Optional DMM provides measurements of ac/dc voltage, ac/dc current, and resistance. DMM improves accuracy of time interval measurements.

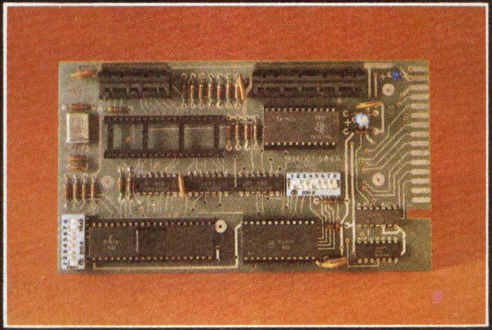
CRT graticules have 10 x 10 divisions, with 0.95-cm vertical and 1.2-cm horizontal dimensions. The result is a full-scale voltage display, 10 times the deflection factor, which can be as low as 1 mV/division. The company claims that this reduces the required calculations, operator errors, and measurement time. The gray contrast display screen is heat treated with a coating that eliminates light reflections. This process increases contrast between trace and background and improves trace definition and brightness.

One measurement capability of the oscilloscopes is third-channel trigger view that permits simultaneous viewing and timing of the external trigger signal with both vertical channels. A x10 horizontal magnifier produces main and
(continued on page 42)

Oak puts E³ up against the world's fastest typists.

In a keyboard market clogged with claims and confusion about "N-key-rollover," look to Oak's FTM® keyboard for the practical answer. It provides E³-Entry Error Elimination. And that means precisely what it says. We challenge the fastest typists in the world to make it error. They can't.

Yet E³ makes its real contribution to Oak's Full Travel Membrane (FTM) keyboard—and to you—in the cost column. You get the Entry Error Elimination and 100-million-cycle-plus performance you've got to have in a keyboard at prices far below those of keyboards with comparable performance. That's practical. Entry Error Elimination is a remarkably sensible microprocessor based N-key-rollover and phantom key lockout system developed by Oak engineers. Without the cost and complexity of Hall Effect and capacitive technologies.



And that's not all. Beneath the FTM keyboard is Oak's proven, industry-leading membrane switch technology. So you get all the good things of membrane switching—reliability, durability, RFI and EMI resistance, design flexibility, and—of course—low cost. All without sacrificing the qualities you demand in a keyboard, right down to human engineered industry standard feel and touch.

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Circle 24 for further information

Circle 25 for salesman to call.

Oscilloscopes
(continued from page 40)
delayed sweep speeds to 5 ns/division. Selectable input terminations are 1 MΩ or 50 Ω.

The 1746A uses HP's dual-marker, delta-time method to speed time interval measurements and improve their accuracy. When this technique is combined with the optional digital multimeter (DMM), time interval measurements can be read out directly on the DMM's LED display with an accuracy nearing ±5%.

Several options increase the scopes' performance level. A 3.5-digit autoranging DMM can be added to either model for increased measurement convenience. Auto-ranging produces measurements that always have the same multiplier: voltage in volts, current in amperes, and resistance in kilohms. The DMM's auto-zero feature eliminates the need to zero the instrument before a test, and auto-polarity allows measurement of either positive or negative values without reversing the test leads. Adding an HP temperature probe to the DMM allows direct temperature reading in degrees Celsius by touching the probe to the surface being measured, and pressing a button.

A TV/video sync option has a TV sync separator circuit that triggers the main sweep on the vertical interval of a composite video waveform, and triggers the delayed sweep on individual horizontal lines. This allows analysis of fields, test signals, timing relationships, lines, or line segments.

Optional HP miniature probe accessories allow easy access to test points in dense circuitry environments. An IC clip added to the probe enables access to DIP pins with high pulse fidelity, without the worry of shorting adjacent pins.

Prices for the 1745A and 1746A are $2840 and $3140, respectively; delivery time is four weeks. Contact local **Hewlett-Packard** sales offices.
Circle 244

Portable maintenance processor uses ATE techniques for field troubleshooting applications

Field maintenance processor (FMP) 2620, first in a series of compatible testers designed by GenRad's Service Products Div, provides an integrated systems test approach to servicing microprocessor based products. It combines in-circuit emulation, logic analysis, communication testing, and program preparation with interactive software.

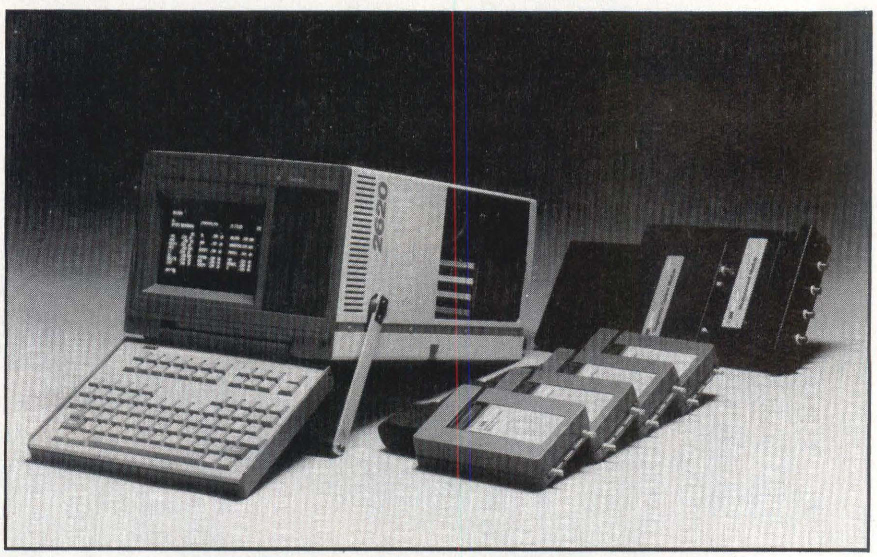
Control interface testing, the name applied to the 2600-series testing approach, allows interface to the unit under test (UUT) through a system bus backplane, microprocessor socket, I/O port, or custom system test connector. This breaks from the traditional method of connecting to the UUT through a PCB's edge connector. With the control interface testing approach, the FMP can test the product at several levels. A system test can be performed using a system test bus interface adapter to run diagnostic routines that isolate failing lower level assemblies. When the faulty module is identified, the interface adapter is changed for different levels of fault isolation until the desired level is reached.

Hardware is Z80A microprocessor based and consists of 256k bytes of memory; 5¼" disk drive; software controlled 7" (18-cm) CRT display; and 85-key keyboard that includes 20 special function keys, 20-column thermal printer, and an integral acoustic coupler with modem.

Diagnostic control module (DCM) and an array of control interface modules are two major subsystems of the 2620 emulation control system. The DCM performs most emulation control functions and provides synchronization to support test routine memory mapping, bus emulation control, and microprocessor control signal multiplexing for fault isolation. There are three types of interface modules: microprocessor, bus, and user designed product modules. Each module conditions and adapts interface bus signals to the DCM, which provides emulation for a variety of microprocessor bus architectures. Users may also devise custom interface modules to accommodate nonstandard system buses and microprocessors. Adapters for the 8085, Z80, 6502, and 6802 microprocessors are currently offered. Additional interface modules for communication testing and system buses will be available the first quarter of 1983.

A plug-in measurement module is closely coupled with the FMP's in-circuit emulation hardware. This module is a versatile data acquisition subsystem that provides realtime sampling and recording of digital and analog information to support both testing operations and program preparation.

Three software levels tailor the tester to specific applications: automated test environment provides a step by step
(continued on page 44)



Field maintenance processor 2620. Plug-in architecture features patented device specific adapter bus and four adapter slots to provide capability for universal product interface. Special function keys allow single keystroke initiation of lengthy test sequences or test mode specification.

"Everybody talks about microprocessor support; here's what we're doing to deliver."

Al Carlson,
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8085	x		Now
Z80	x		Now
6502	x		Now
6800	x		Now
6802 (6802NS/6808)	x		Now
9900		x	Now
8048 (8035/8039 8040/8041/8041A 8042/8049/8050/8741 8741A/8742/8748/8749)	x		Now
8086		x	Now
8088		x	Now
1802 (1804/1805/ 1806)	x		Now
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For technical data circle no. 26

Maintenance processor

(continued from page 42)

product testing sequence; interactive test environment gives a selection of automatic test utilities; and a comprehensive automated programming system prepares a product test program. The tester uses programmer's high level application language GR-PAL™, designed especially for emulation testing.

The broad spectrum of automatic test utilities that the tester offers suits it to a wide range of applications. Among these are system level testing, board level fault isolation, remote diagnostic control and execution, microprocessor control and emulation, peripheral exercising, software analysis and verification, and engineering and production tests. The unit weighs 34 lb (15 kg); prices start at under $10,000. Deliveries are scheduled for Dec 1982. **GenRad, Inc,** 170 Tracer Ln, Waltham, MA 02254.

Circle 245

MICROPROCESSORS/MICROCOMPUTERS

Four board modules utilize VME bus capabilities

Beginning a line of products for the VME bus, Signetics announced four board level modules and a VME bus card cage. The boards provide a "computing nucleus" to take advantage of the VME bus ability to support 16- and 32-bit multiple processor systems. Moreover, the boards allow upgrades to equipment already in the system. Included in the boards are a 68000 CPU with optional memory management unit (MMU), a 256k-byte memory board, a disk controller that can support a mixture of hard disk and floppy drives, and a system controller board. All four are implemented on the double-size VME card form factor.

The system controller has its circuitry on half of the card, leaving room for future options. It is designed to consolidate all the bus arbitration, system utilities, and system monitors that would be needlessly duplicated in multiprocessor systems if they were contained on the CPU board. In the event of ac power failure, the controller provides for orderly shutdown and coordinates it with system reset.

Users can select the most advantageous bus arbitration protocol. Priority protocol is best suited to systems where some tasks need more access to system resources than others. Under priority protocol, preference is granted to four levels of bus masters; bus masters can be daisy chained at each priority level. In systems where all tasks have relatively equal need for access to system resources, the round-robin protocol can be selected. Thus, usage is uniformly distributed among bus masters.

Two clock functions are provided by the system controller. Other boards on the bus can use the 16-MHz system clock for general clocking functions. For systems using the VME bus interprocessor serial communications link and for intermodule information exchange, a serial bus clock is provided. The user can set the controller's watchdog timer from 4 μs to 8192 μs to alert the bus master of error conditions. Similarly, an address verification function can be used to notify the master of an illegal address combination.

In dedicated applications, the CPU board can be used as a standalone single-board computer. In addition to the 8-MHz 68000, it can contain up to 48k

(continued on page 48)

In 5 1/4" and 8" Winchesters. Disctron has the brightest ideas.

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To 40 megabytes.
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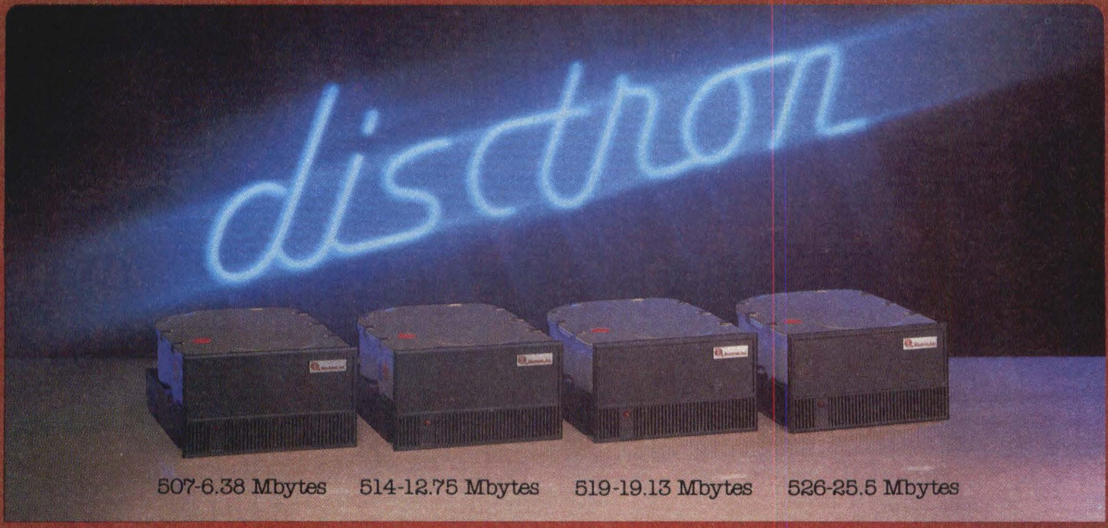

Disctron offers you more capacity, higher performance, and easier integration in 5¼-inch Winchester. With capacities to 40 megabytes. With average access times as low as 35 ms. And with special features—electronically dampened actuator, buffered step mode, electrical spindle brake, integral microprocessor control and built-in AGC.

Easy integration. Slip these 5¼-inch drives into an existing minifloppy cavity. Use standard minifloppy voltages. Use standard ST506/ST412 interfacing. These drives are ready to go.

Plug in the Disctron difference in 5¼-inch Winchester.

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CIRCLE 29

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Board level modules

(continued from page 44)

words of ROM, PROM, or EPROM, or up to 24k words of RAM. Three pairs of JEDEC standard sockets are provided for onboard memory; each pair has address and data lines for 16k words maximum. Two serial RS-232 I/O ports are provided, along with one parallel port that is programmable but defaults to support a Centronics compatible printer.

When the CPU board is used in larger multi-user, multitasking systems, it can be supplied with an optional SC68451 memory management chip. The MMU provides address translation and protection over the 68000's entire 16M-byte address range. It can partition the address range into 32 segments ranging in size from 256 bytes to the full 16M bytes. In addition to the 68000's ability to respond to 1537 interrupting devices, the CPU module can respond to any of the 7 priority interrupt levels from the VME bus.

Designed to negate the need to replace memory boards for system upgrades, the 256k-byte memory module automatically responds to data demands for 8-, 16-, or 32-bit transfers. Memory uses byte parity and is divided into four arrays of 64k bytes each. During byte transfer, the appropriate array undergoes a parity check; on 16-bit transfers, the array pair accessed is checked. For 32-bit transfers, the entire memory is checked.

To decrease effective memory cycle time, users can select either 16- or 32-bit mode 2-way interleaving. This 2-way interleaving requires that memory modules exist in the system in pairs and allows the master CPU or DMA device to direct sequential memory accesses to alternate memory boards. Consequently, one member of the pair can be accessed while the other is completing a read or write cycle.

The disk controller module uses an 8X305 bipolar microcontroller running at 5 MHz, along with various onboard support chips to do all data handling, DMA, error handling, and other control operations. The board supports up to 4 drives, two of which can be 5¼" or 8" Winchesters with ST506 or SA1000 interfaces. Hard drives can be mixed, but they must have the same data transfer rate. Data rates up to 8M bps can be used. Any combination of floppy drives can be supported.

To ease operating system integration, the disk controller module uses device control block and DMA protocols. It performs automatic track and cylinder crossing. In addition to the ability to select data buffers anywhere in main memory, the controller has a 1024-byte onboard buffer and can utilize either 256- or 512-byte sector sizes.

To tie together the various modules, Signetics plans to license Motorola's RMS68K operating system. There will be future system level software offerings as the product line grows. **Signetics Corp**, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 246

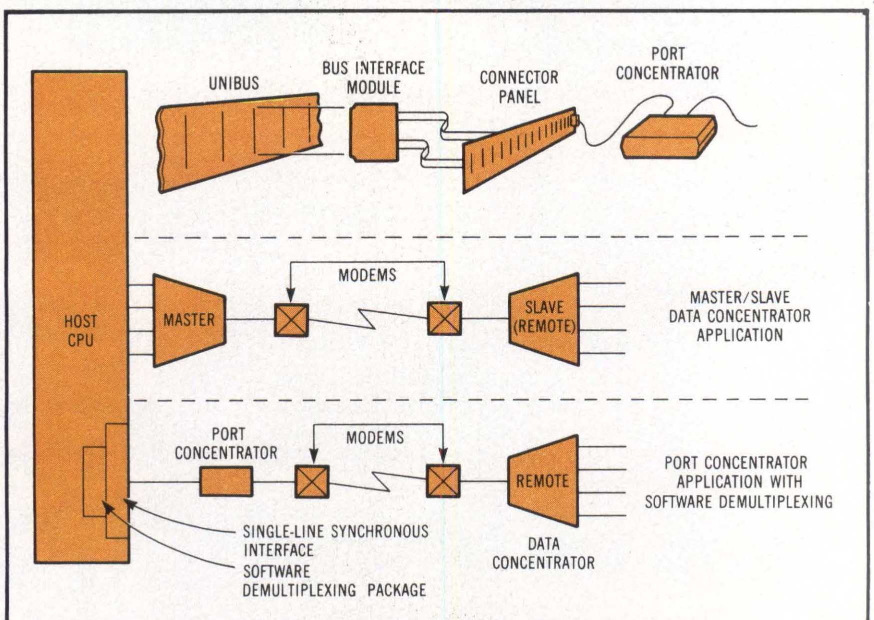
DATA COMMUNICATIONS

Single terminal interface provides local and remote communications for PDP-11/VAX-11 systems

Combining host computer multiplexing and port concentration in a fully integrated interface, the jointly developed Emulex STATCON Series 21 and Micom Series 11 bus driver support asynchronous communications for up to 32 local and remote terminals, with a single UNIBUS slot of any PDP-11 or VAX-11 systems. Each of the 16 RS-232 interfaces can link a single local terminal or a remote cluster of up to 16 terminals, with either DZ11 or DH11 emulations provided for compatibility with Digital Equipment Corp's operating systems.

Terminal interfaces consist of three units: a statistical port concentrator without modem, a bus interface module, and a 16-port distribution panel. The port concentrator supports statistically multiplexed remote communications by handling retransmission of data received in error, data buffering requirements, initialization and synchronization of the communication link, and configuration of the remote terminal concentrator to establish data rates and code levels for each channel. However, instead of fanning out the multiplexed data it receives to multiple RS-232 connectors, it adds channel identifier information to the incoming data stream and routes it through its link to the interface module. Built around a bit-slice microprocessor, the interface module handles the multiplexed data streams from one or more port concentrators simultaneously with traffic from local terminals. Each channel can control data flow with the XON/XOFF function. During extremely busy CPU cycles, the interface module can also control the incoming data flow from the module to the host.

Intended to blend traditional methods of statistical multiplexing with software multiplexing/port concentration, the *(continued on page 54)*



STATCON Series 21/11 bus driver remote configuration (top) is compared with traditional approaches. Neither traditional approach can simultaneously support both local and remote terminals.

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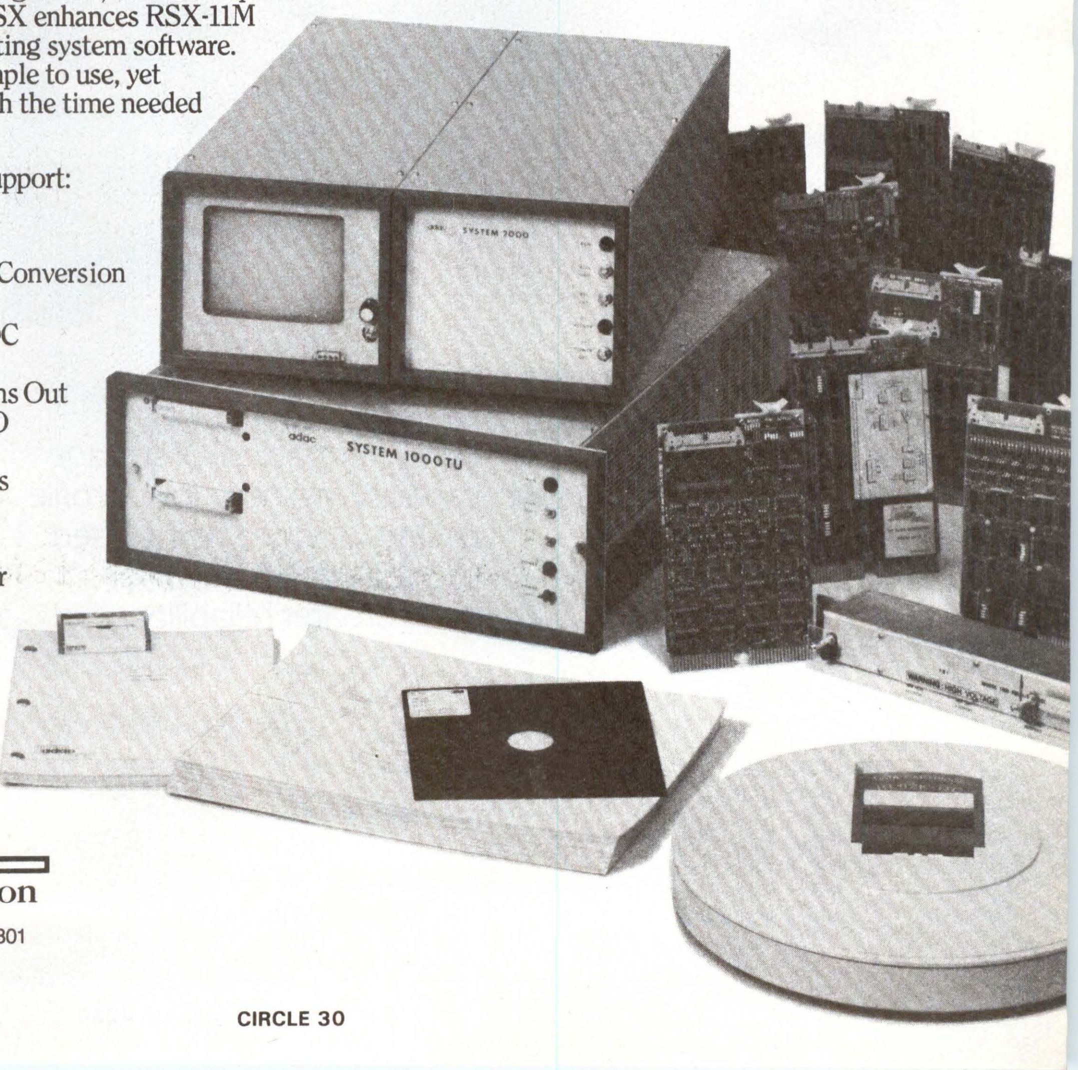

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CIRCLE 30

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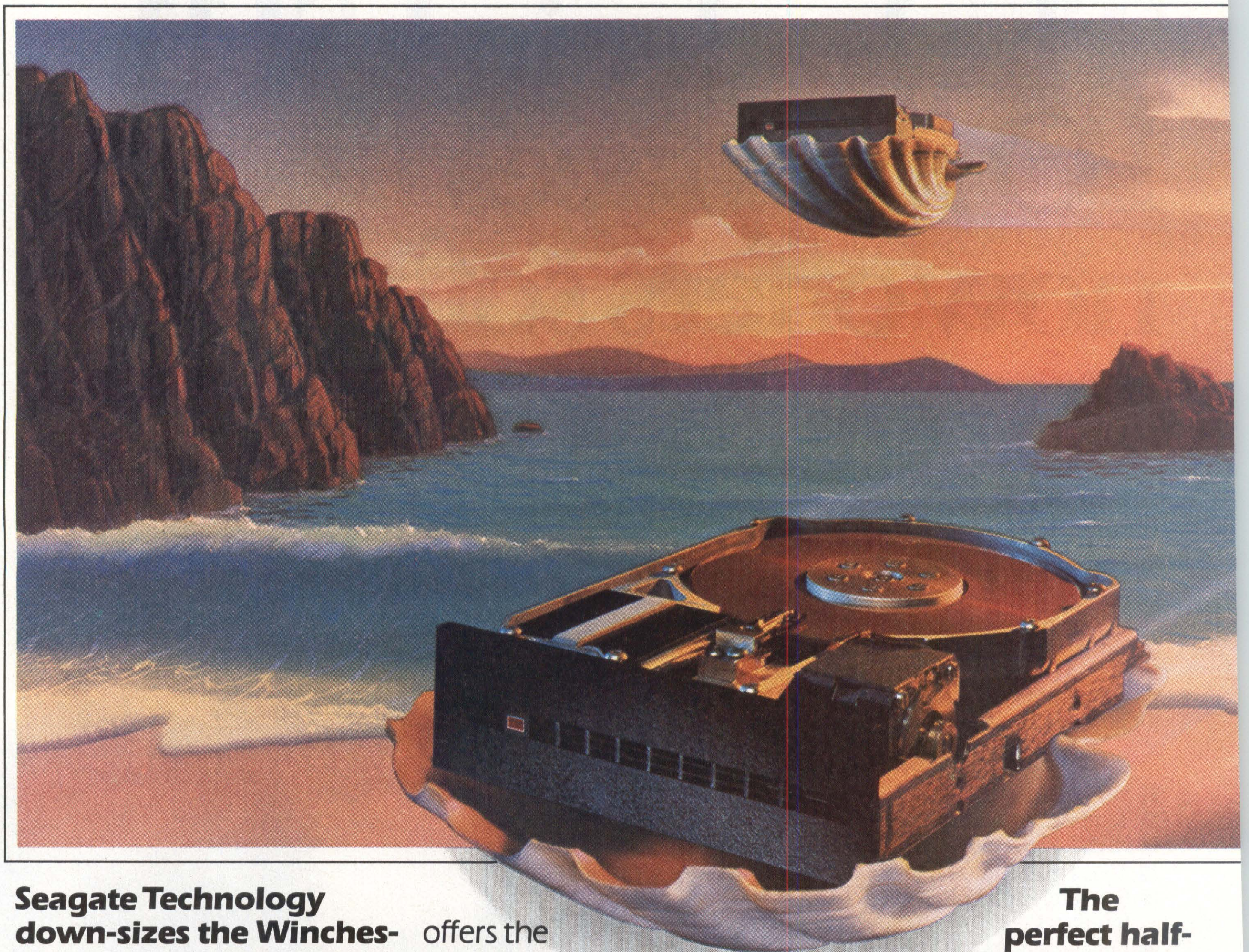

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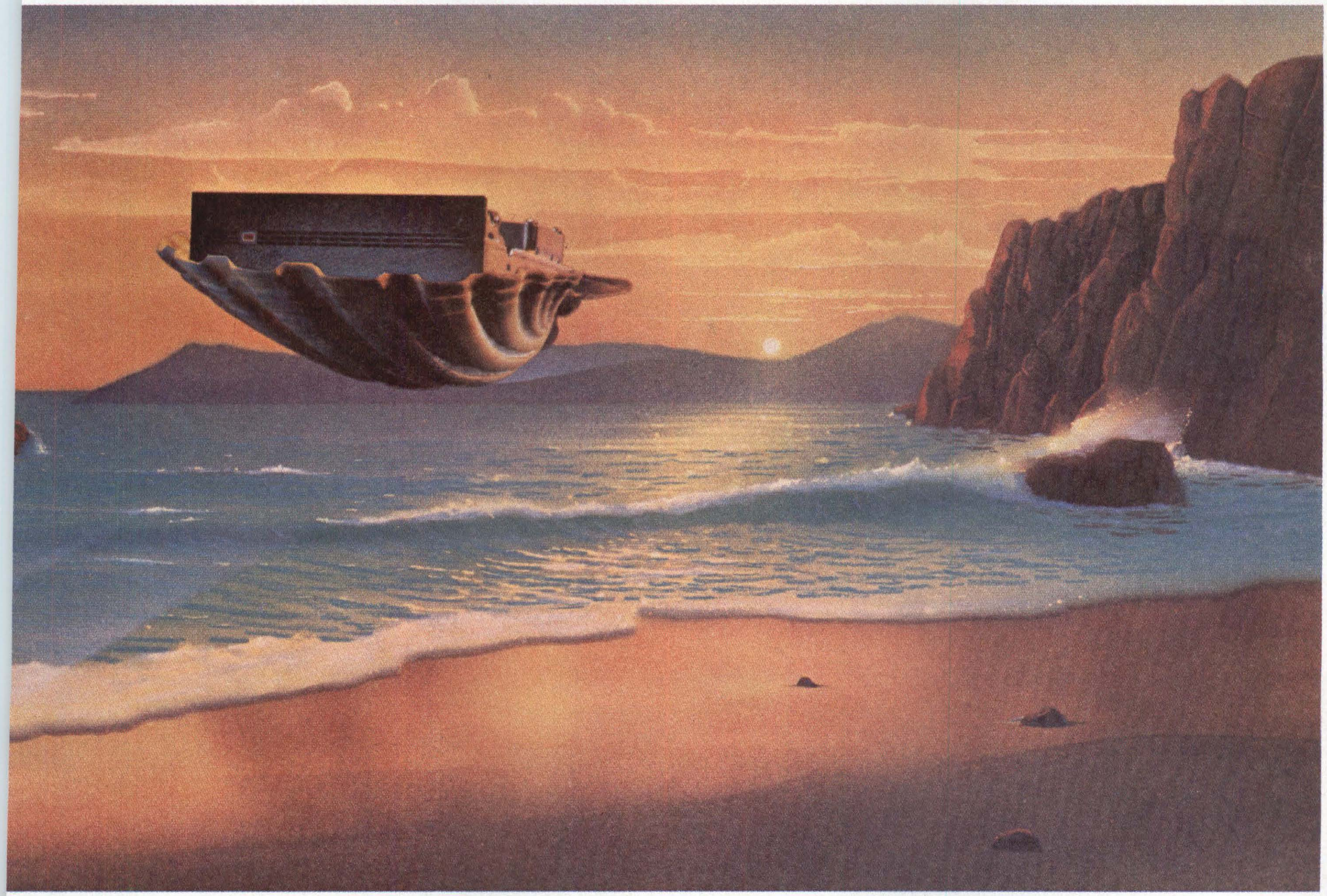

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CIRCLE 31

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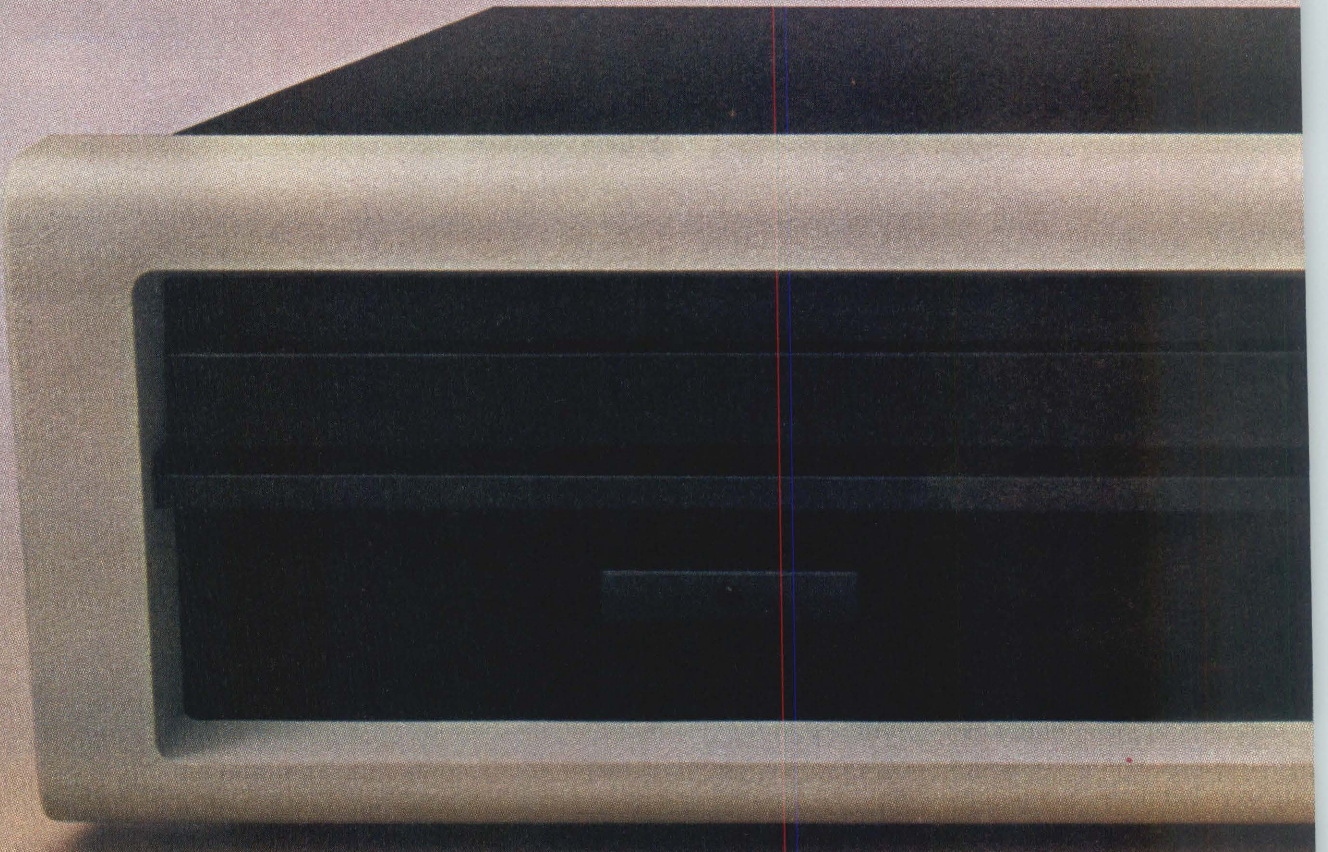

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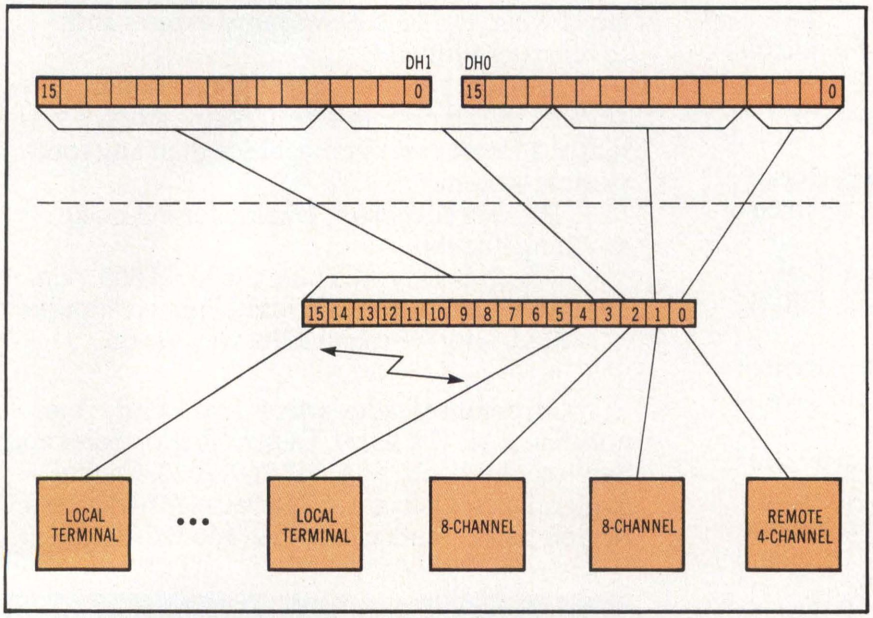
CIRCLE 32

Single terminal interface
(continued from page 48)



Remote terminal clusters can be allocated channels from separate DH11 interfaces. This is also true of 8-channel DZ11 interfaces. Note that port 3 remains unused after local and remote terminals are allocated all 32 channels.

products take advantage of the strengths of both approaches, without suffering from their weaknesses. Statistical multiplexers have long been used to efficiently share telephone lines and dedicated data links among remote terminals with the benefit of fully automatic retransmission of data when errors occur, as well as data compression. However, this means that there are as many local ports and cables between the CPU and the local concentrator as there are remote terminals, in addition to the need for twin statistical multiplexers at either end. Integrating statistical multiplexers and host interfaces in products such as the ComDesign TC-3 and Digital Communication Assocs Series 205 reduces implementation cost by eliminating a conventional statistical multiplexer and associated cables at the host computer, and by offering from 8 to 128 channels (Series 205) with DZ11 host interfaces. However, these products share the same weakness of conventional multiplexers—duplicate host interfaces and distribution panels are needed to support local terminals.

To conserve computer ports, software multiplexing with port concentration directly links the composite communication line into the host CPU through a single high speed data channel using only one port with a port concentrator (eg, the Micom Micro200). Custom software packages handle multiplexing and demultiplexing of data, monitoring link error status, providing local/remote diagnostic loopback, modem control, data rates, and data flow. Since software multiplexing is not a trivial task (especially error control protocol), it is only justified when multiple remote statistical multiplexers are used and the application is oriented to a specific task. Using port concentrators, however, reduces the programming task with its link integrity and analog loopback facilities. By integrating the software multiplexing tasks with the emulation of 2 DH11 or 4 DZ11 line multiplexers, integrated terminal interfaces can allocate unused ports to local asynchronous lines, provided the total number of remote and local lines does not exceed 32.

The allocation scheme is unique in that either terminal interface can allocate DZ11 or DH11 and 16 lines/DH11 if the required number of channels for a given remote cluster exceeds the number of lines available in any one DH11 or DZ11 board. For example, if 1 remote cluster needed 4 DH11 channels and 2 others required 8 channels each, the interface module would allocate 4 of 16 DH11 lines to the first cluster, 8 lines to the second cluster, and the remaining 4 lines to the third. The interface module would then allocate 4 lines from the other DH11 to complete the third cluster's needs. Local terminals are serviced from the highest order port (port 15) downward to other ports not used by remote clusters. Any physical RS-232 connections not dedicated to either local or remote terminals remain unused.

Both terminal interfaces are compatible with standard Micom Micro800/2 and Micro8000/2 remote data concentrators with the composite data link operating synchronously at either 9600 or 19,200 bps. A special algorithm within the port concentrator provides fast echoplex to improve response time for remote terminal users when supported in DEC software. Also provided with the remote data concentrators are remote dial-up capability, automatic terminal speed recognition, command port for error logging, and statistics collection.

A minimum Emulex STATCON Series 21 or Series 11 bus driver configuration consists of a single bus interface module, port concentrator, and distribution panel, and is priced at $6300 in single-unit quantities. Emulex quotes additional port concentrators at $2200 each (without modem). Both Emulex and Micom provide 4 to 16 channel remote data concentrators, with or without integral modems, at standard prices. Deliveries are scheduled 60 days ARO. **Emulex Corp**, 2001 E Deere Ave, Santa Ana, CA 92705. **Micom Systems, Inc**, 20151 Nordhoff St, Chatsworth, CA 91311. **ComDesign**, 751 S Kellogg Ave, Goleta, CA 93117. **Digital Communications Assocs, Inc**, 303 Technology Pk, Norcross, GA 30092.

—*Joseph Aseo, Field Editor*

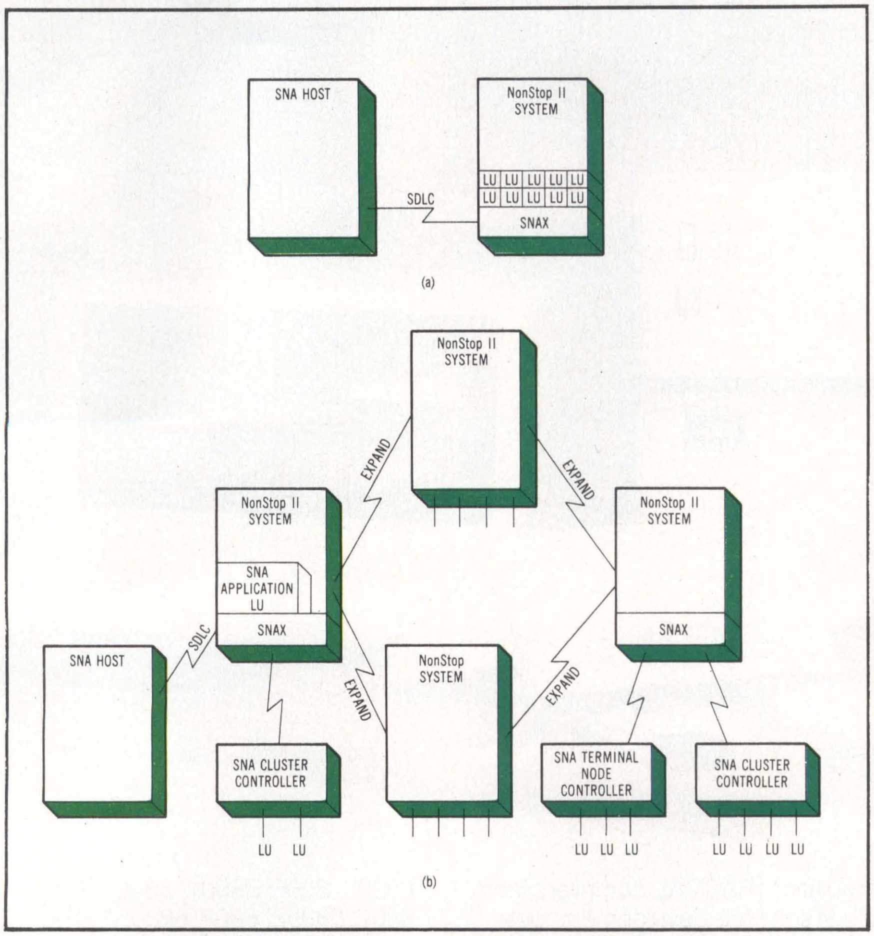
Emulex—**Circle 247**
Micom Systems—**Circle 248**
ComDesign—**Circle 249**
Digital Communications—**Circle 250**

Software interface links SNA devices to fault tolerant systems

Intended to connect IBM System Network Architecture (SNA) network with its own EXPAND™ data communications network, Tandem's SNAX communications services software allows its fault tolerant computer systems to control most SNA devices, as well as to communicate directly with the SNA network as a fully functional SNA node. Not only can application programs on the EXPAND network access existing SNA applications, but SNA devices can also communicate with SNA hosts through the EXPAND network's passthrough mode. Thus, devices such as automated teller machines, point-of-sale terminals, and manufacturing floor terminals are easily integrated into the EXPAND network with little or no code modification.

The communications package makes the NonStop II™ system behave as an
(continued on page 56)

Software interface
(continued from page 54)



Viewed by host as cluster controller (a), several Tandem systems can support several SNA devices to reduce network management chores for host (b).

SNA cluster controller, handling several application tasks as well as communicating with many applications in other SNA hosts simultaneously. Several such systems can be linked to the host on a single line. Therefore, the host's network management workload is reduced from managing multiple physical units on many lines, to managing a single physical unit with multiple logic units on a single line. Downloading operational microcode or other files from the SNA host to devices with the passthrough mode allows the Tandem system to freely pass data without modification.

A communications manager handles configuration, network operation, network monitoring, and problem definition functions needed to integrate SNA devices and applications. First, the manager defines all physical units and logical units with their attributes. System generation procedures are then used to define communications lines, controllers, and SNAX input/output processes, with dynamically alterable parameters.

Network initialization involves activating SDLC lines that link SNA devices with the Tandem subhost, and initiating system services control point to physical unit and logical unit sessions. Users can then monitor passthrough sessions, line quality, and physical unit failures, as well as check status of unit sessions and de-activation of SDLC lines. Additional monitoring in EXPAND networks checks traffic thresholds between nodes and between processors. Without host involvement, SNA devices have access to distributed data bases, automatic routing, and online reconfiguration.

Various sessions for SNA devices are established and controlled through the SNAX Application Logical Unit (SNALU) interface. Application processes can either provide primary logical unit (PLU) services (the application controls the session by defining rules and communication formats) or secondary logical unit (SLU) services (any LU-LU session formats allowed for SNA cluster controllers). An application running on a Nonstop II system can act as a PLU to SNA devices, but must behave like an SLU to an SNA host application.

Designers unfamiliar with SNA structures and protocols can use a high level interface to link 3270 family devices to the EXPAND network. Supported protocols include the 3270 data stream interface (CRT), 3270 line printer interface (PTR), and 3270 interactive terminal interface (ITI). CRT protocol supplies information that the 3270 screen format orders. It also supplies text to both terminals and printers when data are buffered and transmitted as a group rather than one line at a time. PTR protocol handles output one line at a time to 3270 style printers from spoolers or from applications written to employ conventional printers. Only the basic 3270 data stream character set is supported (the SNA character set is not). ITI protocol provides a similar line-at-a-time format for the 3270 terminal. Each write to the terminal by an application is presented as a single line of output on the display. A minimum level of screen support is provided so that programs like command interpreters can run on 3270 devices. When an SNA 3270-type device is connected to a Tandem system, access to distributed database software and online transaction processing is also provided. Little, if any, modification is needed.

SNAX supports all SNA devices connected to SNA terminal node controllers (physical unit type 1) and cluster controllers (physical unit type 2) through the SNALU interface. Contact the company for information on specific 3270-type devices supported by the high level interface, as well as information on other SNA devices. A license fee for the SNAX software is $2750/processor, with general availability scheduled for April 1983. **Tandem Computers Inc**, 19333 Vallco Pkwy, Cupertino, CA 95014.
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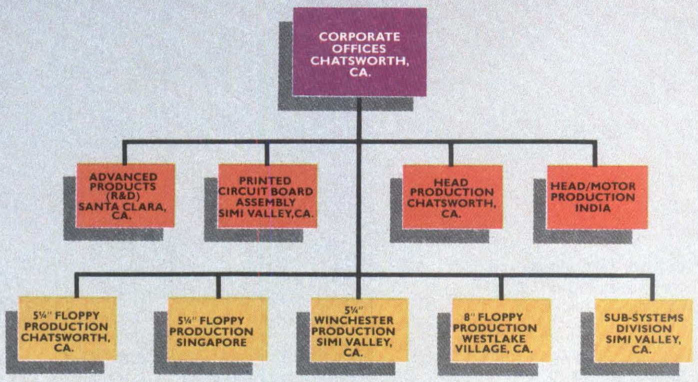

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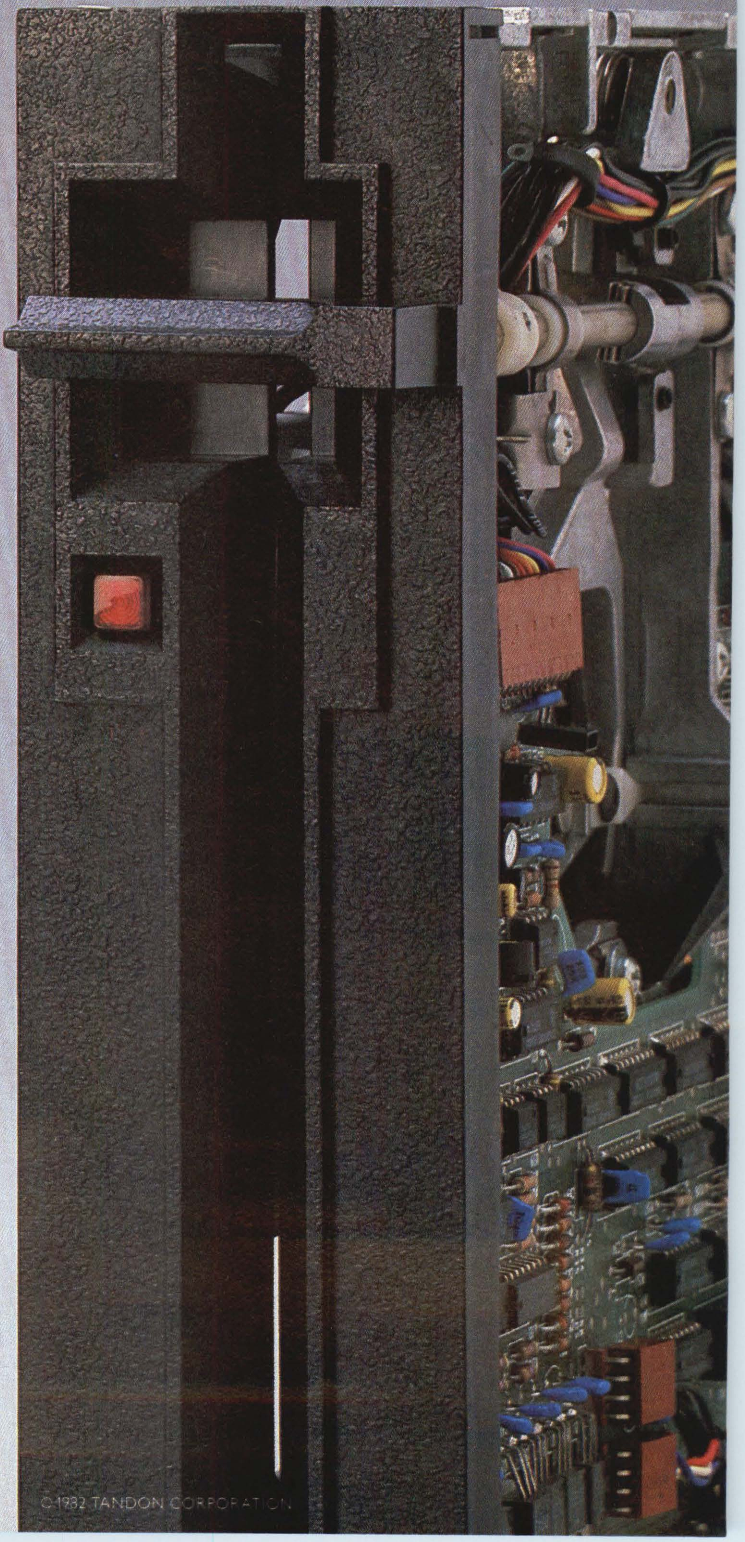

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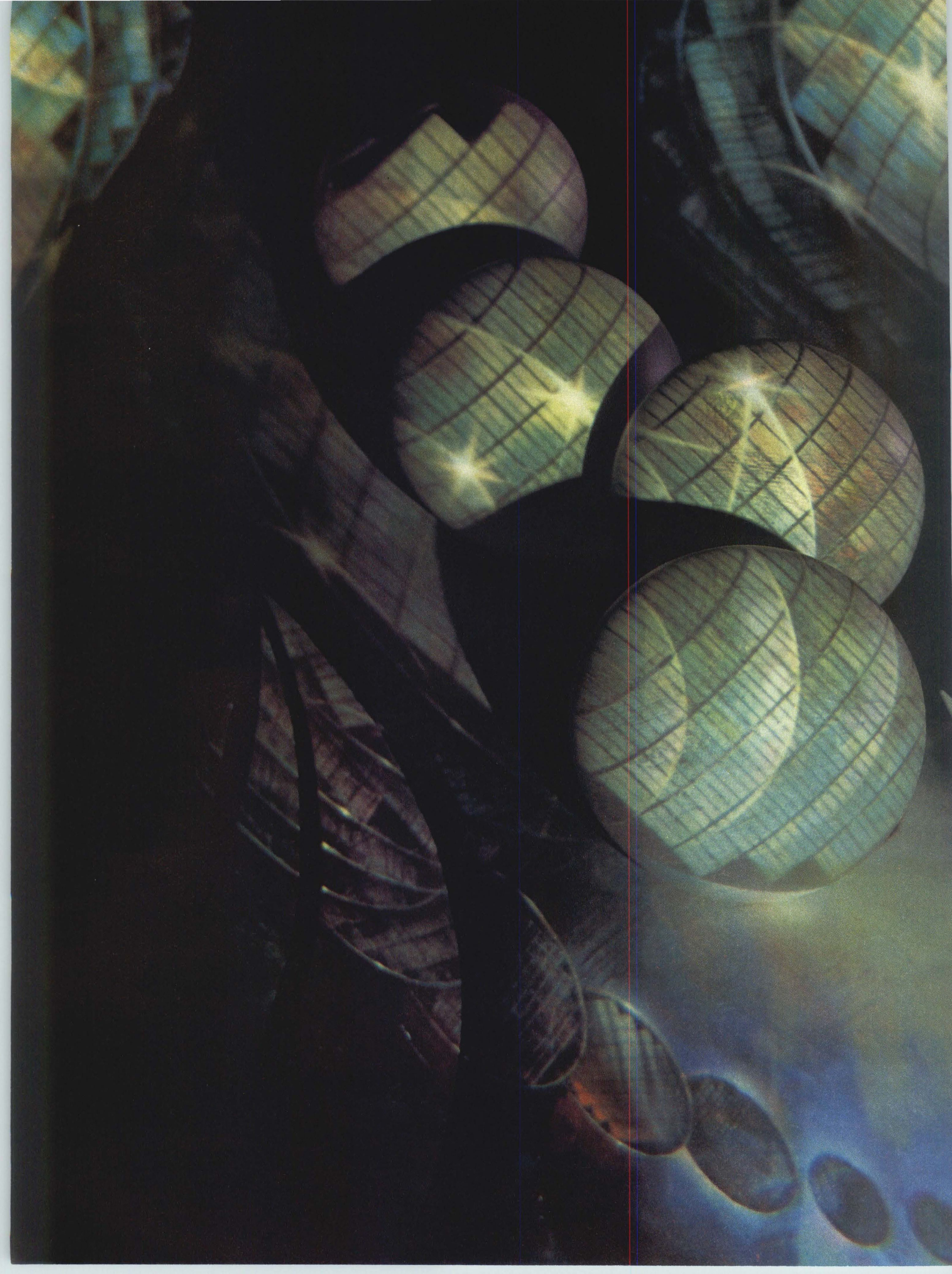
CIRCLE 36



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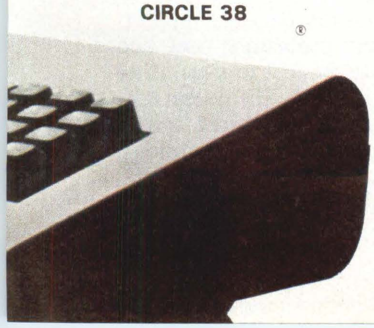


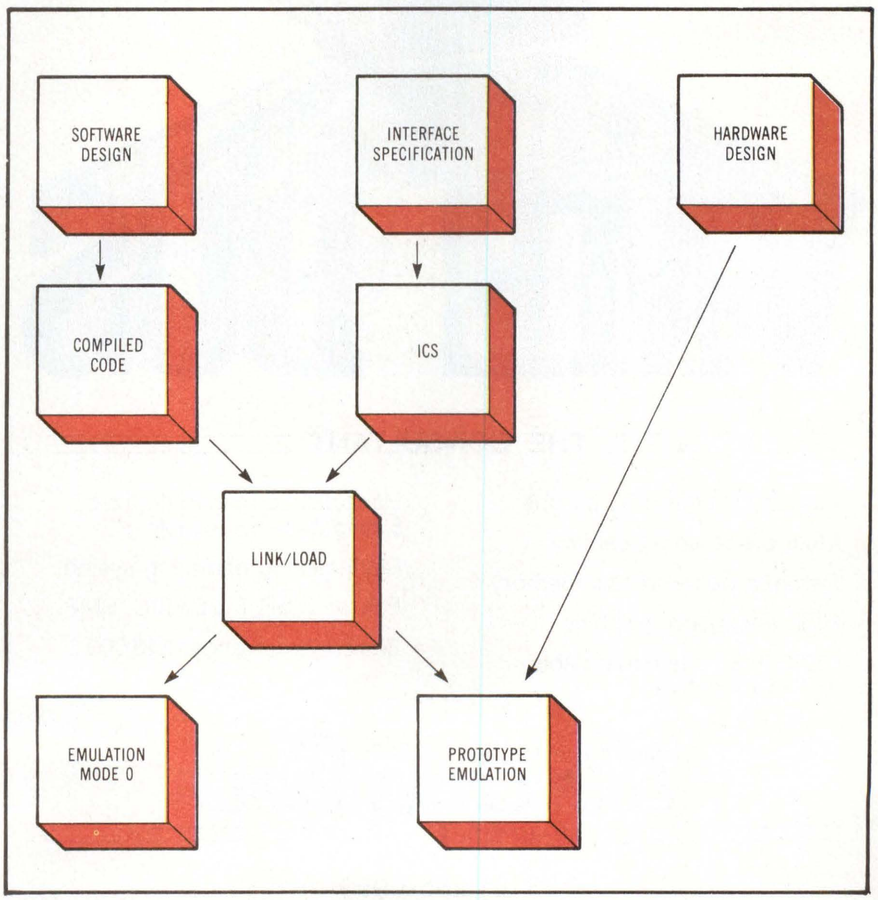
Pascal language package automates microcomputer software development process

Estimated to be eating up 50% of computer manufacturers' research and development dollars, software development costs for microcomputer based products continue to grow as designers switch to advanced 16- and 32-bit processors. One estimate is that, by 1985, a typical microcomputer application will cost $3 million using conventional development techniques. One step toward controlling these escalating costs is automation.

A Pascal language development system called LANDS responds to this need by allowing programmers to work in high level language from source code entry through debugging in the prototype environment. Introduced by Tektronix's Design Automation Div, the package implements automated development concepts proven at the mainframe level to double programmer productivity at the microcomputer level. Jack Liskear, Tektronix marketing manager for microcomputer development products, states that the product moves the software development process from an "art" to an engineering discipline that combines structured programming with specialized design tools.

The package runs on the 8560 Multiuser Software Development Unit (introduced last November) under the TNIX™ operating system. It is divided into four parts: the language directed editor (LDE), Pascal compiler, integration control system (ICS), and Pascal debug segments; each automates a particular design phase.

The LDE operates at the source code level, offering full Pascal syntax checking and an advanced user interface. Incorporating the compiler's parse phase into the editor allows users to run a syntax check at the line, procedure/
(continued on page 64)



ICS within LANDS automatically reconciles hardware/software interface problems by generating all interrupt initialization and vector routines, linker commands, and library selections. It also performs consistency checks on requested setup and hardware configurations.

Pascal language development system
(continued from page 63)

function, or program level. At any level, the LDE flags all syntax errors before they reach the compiler, reducing source code modification and recompilation by eliminating compiler errors.

The screen oriented editor automatically indents all Pascal syntactical units to their proper form; they can be moved, deleted, or copied to any program text location. All Pascal keywords, as well as commonly used text, can be abbreviated to reduce keyboard errors. Supporting machine level manipulation and debugging through realtime emulation, the Pascal compiler handles the software design environment. It supplies direct dialogue with I/O ports, absolute location of variables, and manipulation of bit level data. Interrupt procedures can be defined and called as needed.

The compiler's Pascal operating system interface allows I/O simulation to be conducted through development system resources, but keeps simulation modules independent of the main program. This permits temporary I/O modules, linked to the program during initial emulation, to be replaced later with prototype I/O modules that supply the final I/O code. The compiler performs single-pass switchable optimization, with each optimization typically tested as performed. Pascal code remains the same; only the object code changes. Optimization produces a 37% code reduction that results in a 20% to 50% speed increase.

Configuring software to prototype hardware requires minimal user input because of the package's ICS. This package, patent pending, provides memory configuration to place individual code segments in RAM or ROM address spaces, low level interrupt handling and connection to Pascal generated service routines, and automatic assembly code generation to accomplish hardware initialization and reset.

A user menu lists all parameters necessary for hardware/software integration. From the user's input, the control system generates a linker control file and calls those object modules necessary for machine level operations. At link time, the system automatically configures Pascal modules, library modules, and low level object code to conform to prototype hardware requirements.

By raising all debug commands to the Pascal level, the Pascal debug system eliminates the need to translate assembly level data into source code for analysis or modification. Breakpoints can be controlled by compiler assigned statement numbers, user assigned labels, or module names. Variables can be accessed and modified using original Pascal data types, and arithmetic variables can be automatically evaluated. Where assembly modules have been linked to the main Pascal program, the debug system permits transparent access to assembly language debug.

The Pascal LANDS package supports all major 16-bit processors; 8086 and Z8000 versions are the first releases. Price of the package is $8000. The system runs on the 8560, an LSI-11/23 based system that supports up to eight workstations. **Tektronix, Inc, Design Automation Div,** PO Box 1700, Beaverton, OR 97075.
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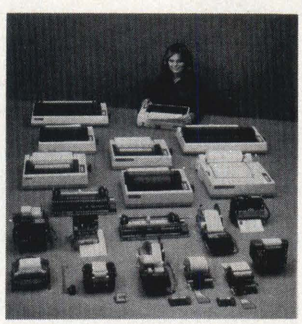

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CIRCLE 41

Universal Medium aids distribution of programs in p-System object code

Developments in 5¼" floppy disk drive and controller design have made it possible to greatly simplify distribution of applications programs written under the UCSD p-System. What has emerged is the soft sectored 5¼" diskette as the dominant mass storage medium for software distribution for small computers, as well as the use of programmable controller chips in small disk controllers. Together with p-System object code, portable to any computer running the p-System, these developments make it possible for software suppliers to distribute programs on a single medium and format. Adaptation to various target machines is then possible.

Distributed on a standard disk and format, p-System object code can be read and rewritten in the target machine's format by SofTech Microsystems' Universal Medium Adaptor. The Universal Medium Adaptor is a routine tailored for the target machine that can supply parameters to the disk drive's programmable controller. These parameters allow it to read the data in the standard format of the distribution diskette. Then the computer copies data it has read back onto a disk in its native format. Since p-System object code constitutes all data, it runs without further modification.

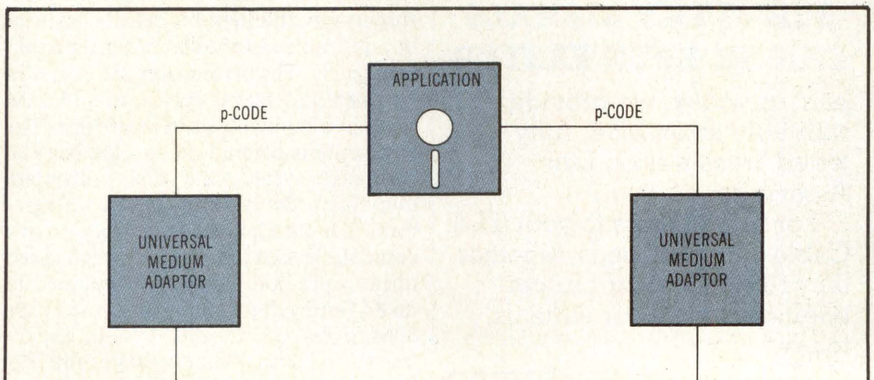
For computers without programmable controllers, a special version of the Adaptor can be written. The known format parameters are embedded in this version, which can also read the distribution media and write it back in the machine's native format. SofTech Microsystems will supply the Adaptor with Version IV of the UCSD p-System.

This Adaptor concept allows other options to be built into a distribution copy of software. Using the p-System's native code generation capability, the software developer can trade off between the compactness inherent in p-code and speed advantages by having some sections of the program in the target machine's native code. The distribution copy has markers for native code generation done during the same copy operation in which the user adapts the program to his machine. This capability can be used to incorporate different peripheral-specific routines. These can be selected at adaptation time and copied with the p-System runtime OS to run immediately.

The Universal Medium format will be recorded on the label side of the diskette in MFM format with 35 tracks numbered 0 to 35. There will be eight 512-byte sectors/track with no interleaving or track to track skew of sectors. In addition to other pertinent information like bootstraps, the last byte of the first sector will contain a version number. Allowances will be made for future versions such as a 40-track option or the use of double-density (96-tpi) drives. The flip side of the disk will contain Universal Medium Adaptor formats for one specific machine whose controller is not programmable. This side will be in 16-sector, 256-byte format; capacity for both sides is 140k bytes. **SofTech Microsystems**, 9494 Black Mountain Rd, San Diego, CA 92126.

—Tom Williams
West Coast Managing Editor

Circle 253



Compiled p-code Version IV UCSD p-System application is portable to any computer supporting p-System (including most 8- and 16-bit machines). When p-code is recorded on Universal Medium diskette, it becomes accessible to a wide range of computers by using adapter routines tailored to their disk formats.

Software library aids waveform analysis

A waveform measurement software library developed by Hewlett-Packard defines time domain measurement programs using the company's 1980A/B oscilloscope in conjunction with HP 9826 and 9836 computer systems. This combination allows time domain waveforms to be characterized, automatically eliminating many sources of error such as improper oscilloscope setup. Waveforms and parameters can be written onto the screen and stored on disk for future reference, eliminating the traditional "grease pencil" method of characterizing waveforms directly on the CRT. Since the 1980A/B oscilloscope is itself programmable, its use with a computer adds capabilities for data storage and retrieval, as well as for the generation of ideal waveforms by means of proper algorithms in the computer. These can then be compared with waveforms from the circuits under test.

The HP 19800A waveform measurement library consists of measurement program, library subprograms, and programming aids. One measurement program makes complete time domain characterization and comparison measurements, providing results on the first day of use without requiring the user to write additional software.

A total of 36 subprograms form the key to the 19800A system. Subprograms fall into five functional groups: waveform setup, waveform data management, waveform characterization, waveform comparison, and general utilities. In waveform setup, for example, the user can define a waveform window in terms of maximum and minimum voltage, and a time window in terms of start time and duration. Since a computer is *(continued on page 68)*

Software library
(continued from page 67)
involved, waveform data management routines handle waveform data records on disk and can even be used to create and manage a waveform data base.

Waveform characterization routines provide a set of parametric, time domain measurements. Specific routines are included to measure the voltage at a given point, the voltage difference between two points, and the average or rms voltage of a waveform. Timing routines measure a waveform's rise time, fall time, pulse width, and pulse period. Delta time measurements can be made between two waveforms or two points on the same waveform. In order to make these measurements, two routines define transition levels of a waveform and locate all of the complete transitions. Transition levels are defined using a histogram that ignores ringing or overshoot on the top and base of the pulse. Only transitions that pass sequentially through all three defined transition levels are recorded as transitions. Finally, three routines are included that use the 1980A/B's trigger flag to make voltage and timing measurements.

Several programming aids develop the main measurement programs that call the subprograms. These include documentation, step by step instructions, an auto-loader that links subprograms together and to the main program, and a program file to contain variable declarations. Contact local **Hewlett-Packard** sales offices.
Circle 254

MEMORY SYSTEMS

Fixed/removable 8″ disk drive incorporates Whitney suspension and read/write technology

State of the art IBM 3370/3380 disk drives, code-named Whitney, feature an advanced performance head suspension, a new encoding method for high bit density, and thin film heads. This Whitney level suspension and read/write technology is the model for Amcodyne's Arapahoe™ 7110 8″ fixed/removable disk drive. The 7110, described by the manufacturer as the first Whitney removable disk drive, incorporates head suspension and high bit density features but uses mini-composite rather than thin film heads. The drive stores 25M bytes in its fixed and sealed enclosure and 25M bytes in a removable ANSI cartridge. The Arapahoe is offered on an OEM basis to computer system and disk subsystem manufacturers and to system integrators. It has a Control Data Corp's Lark compatible SMD interface and high speed linear voice coil actuator. Contained in an 8″ floppy disk drive's form factor are 50M bytes of storage, system input/output, backup, data exchange, and off-line storage.

Whitney suspension is characterized by lightness, stiffness, and a stable ride. Coupling mini-composite heads with Whitney suspension results in a low mass inertia and high aerodynamic stability. For example, a Winchester suspension has 30 vibration modes below 10 kHz, and a Whitney has 8 vibration modes. Improved head/disk compliance is obtained with a higher signal/noise
(continued on page 72)

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- Full editing
- Programmable non-volatile columnar tabbing, or field tabbing, forward and backward

The U.L. listed VISUAL 330 exceeds FCC Class A requirements and U.S. Government standards for X-ray emissions.

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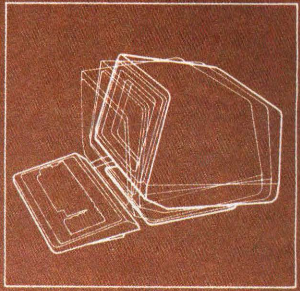
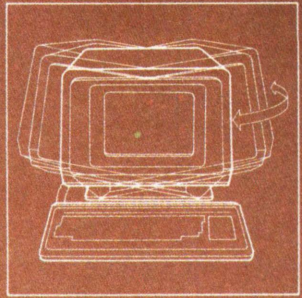
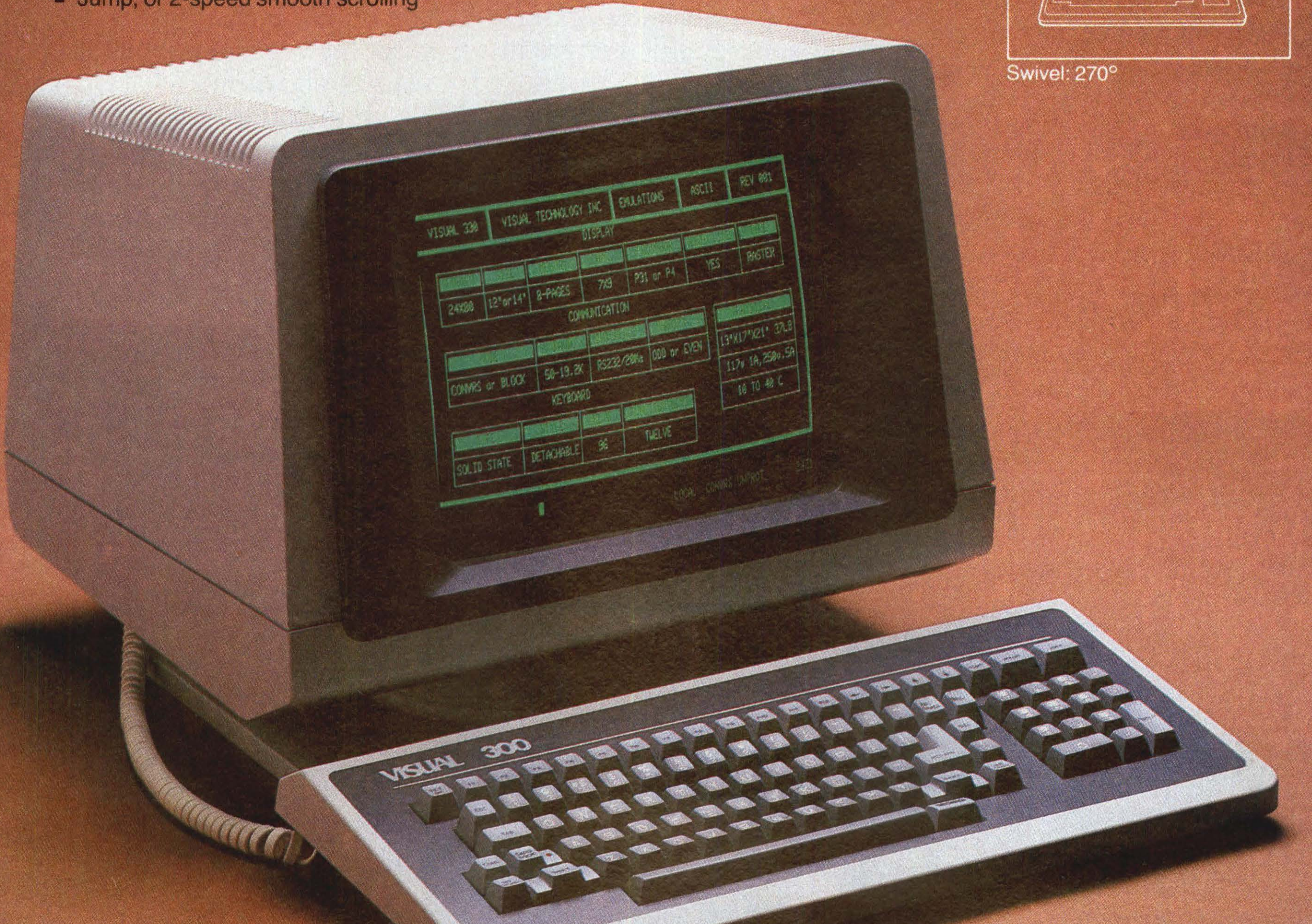


Tilt: 10° forward, 15° backward



Swivel: 270°



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CIRCLE 43

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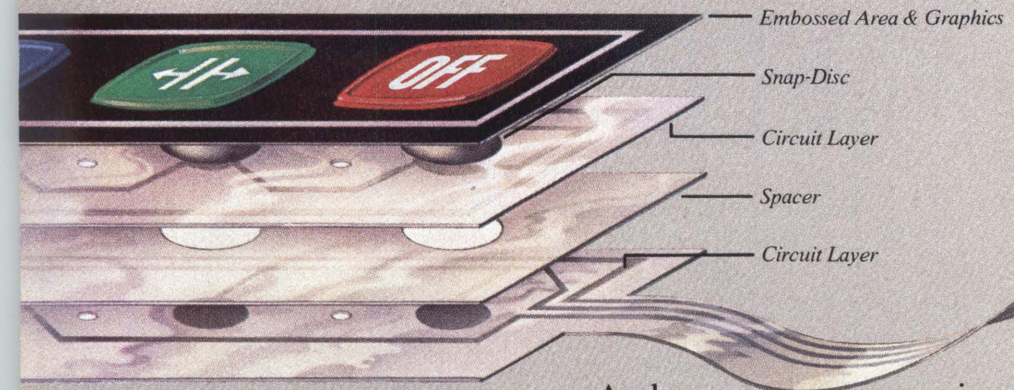

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It can bring you a touch panel with more human engineering in front of it.

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As a result, we can help you design a touch panel to meet the ergonomic needs of your application.

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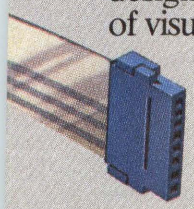
Gasoline pump monitor, manufactured by Southwest Pump, features MICRO SWITCH custom touch panel.

years of innovation bring only a few years old?



a positive feel of the switching action. The touch surface can also be embossed to enable finger positioning on the switch stations.

Your touch panel can be designed to include a variety of visual feedback options including LCD, LED, or electroluminescent displays. Audible feedback is also available.

The touch panel is a critical interface between your product and its user. We put more human engineering in front of it, so you'll get better communications through it.

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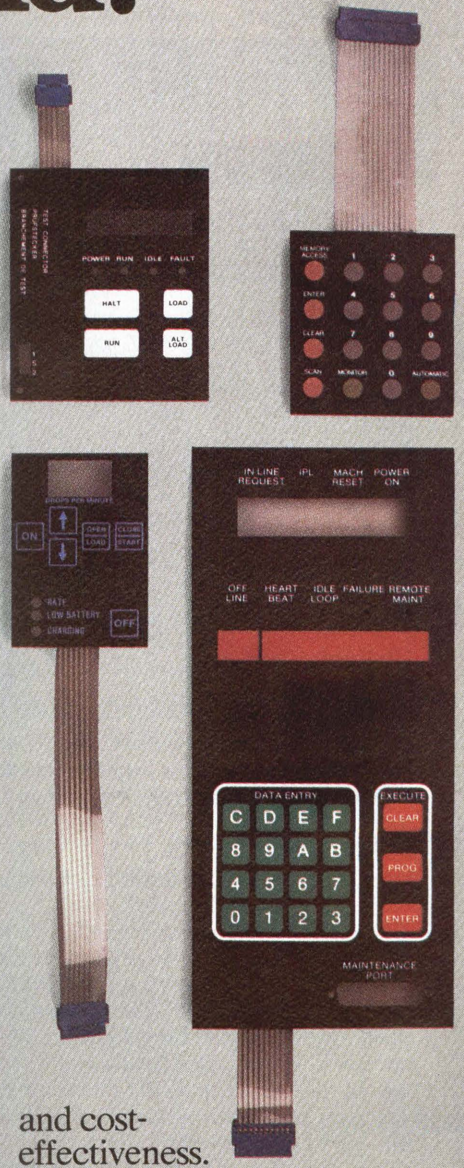

and cost-effectiveness.

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For more information about our touch panel capabilities, and for the locations of our sales offices around the world, call 815-235-6600. Or write MICRO SWITCH, Freeport, IL 61032.

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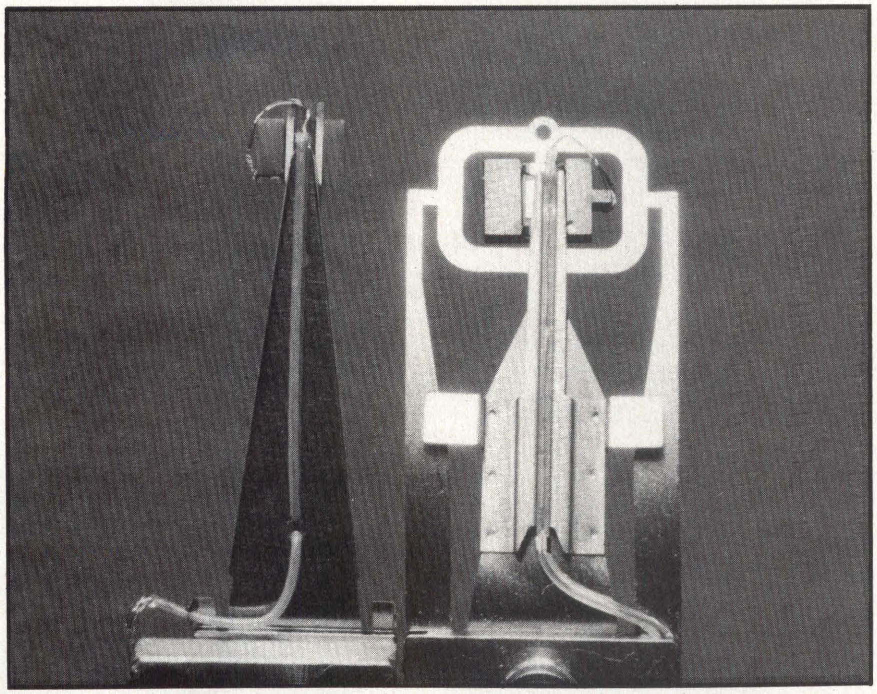
CIRCLE 44

Whitney disk drives
(continued from page 68)



Comparison of Whitney (left) and Winchester (right) suspensions. Load beams are similar, but Whitney suspension has lighter, stiffer side rails. Result is more stable read/write platform with much lower flying height modulation in readback signal.

ratio. Also, there is no instability when a Whitney head is launched.

A ramp-loading system is used in both the fixed and removable drives. Heads are held off the disk until a proprietary clean air system scrubs the plenum to clean room levels and the spindle reaches operating speed. The heads are then loaded on an established air bearing. The start time with purging is 50 s and the stop time is 10 s. Dragging is eliminated. The company claims that 50,000 head launches and landings result in less disk burnishing than 10,000 traditional Winchester starts and stops. This system was developed to meet the rugged requirements of the removable cartridge. It also saves the heads and the fixed disk surface during shipping.

Read/write electronic innovations result in a recording density of 10,000 bpi. "Two-of-seven," a specific type of run-length limited code (RLLC), is used on the 3370/3380. IBM writes 15,000 bpi, although the maximum flux changes are only 10,000/in. By using two-of-seven RLLC, IBM attained a 50% reduction in the flux changes/in to bits per inch. A certain number of flux changes on a disk, apparent to humans, will be interpreted by the controller as more bits per inch. For example, the 3350-type machine had one flux reversal/in for every bit. The 3370/3380 has one flux change/in for every 1.5 bpi. The RLLC significantly improves linear density.

Amcodyne uses the same encoding and decoding as IBM, but changed the preamble and synchronization. Without losing any reliability, they simplified the electronics required to recognize the beginning of data. Added detection features enhance read reliability by improving off-track performance and reducing susceptibility to high frequency noise. Gate array technology reduces the number of integrated circuits required for encoding/decoding from 16 to 1.

An embedded servo system provides position and velocity data from the recorded servo sectors in each data track to an onboard microprocessor. This processor controls actuator mechanical functions and eliminates head/disk alignment problems. An average access time of 35 ms is obtained with high tracking accuracy.

Evaluation units are available now. Quantity shipping is expected to start in January 1983. Pricing is available from the company. **Amcodyne Inc,** 805 S Lincoln St, Longmont, CO 80501.

—Douglas Eidsmore, Senior Editor
Circle 255

5¼" disk cartridge nears physical standard; format agreement still distant

In the quest for data interchangeability on 5¼" hard disks, the first goal is within reach—acceptance as a mechanical standard by the American National Standards Institute (ANSI) committee. While the committee has not approved the 1981 proposal, it has voted it into the working standard proposal category. This means that the proposal is the only one under consideration because no competing proposals for the 5¼" cartridge have been submitted to the committee. Therefore, it is likely that it will be accepted in close to its present form. The draft proposal has been submitted to the International Standards Organization (ISO) as well.

Seagate Technology, DMA Systems, and Dysan Corp—the three original members of the "cartridge club"—are working on the present mechanical standard. In addition to environmental and dimensional requirements, the proposal covers physical characteristics of the rotating media like moment of inertia, maximum speed, and shock and vibration. The disk substrate itself is not specifically covered in the proposal.

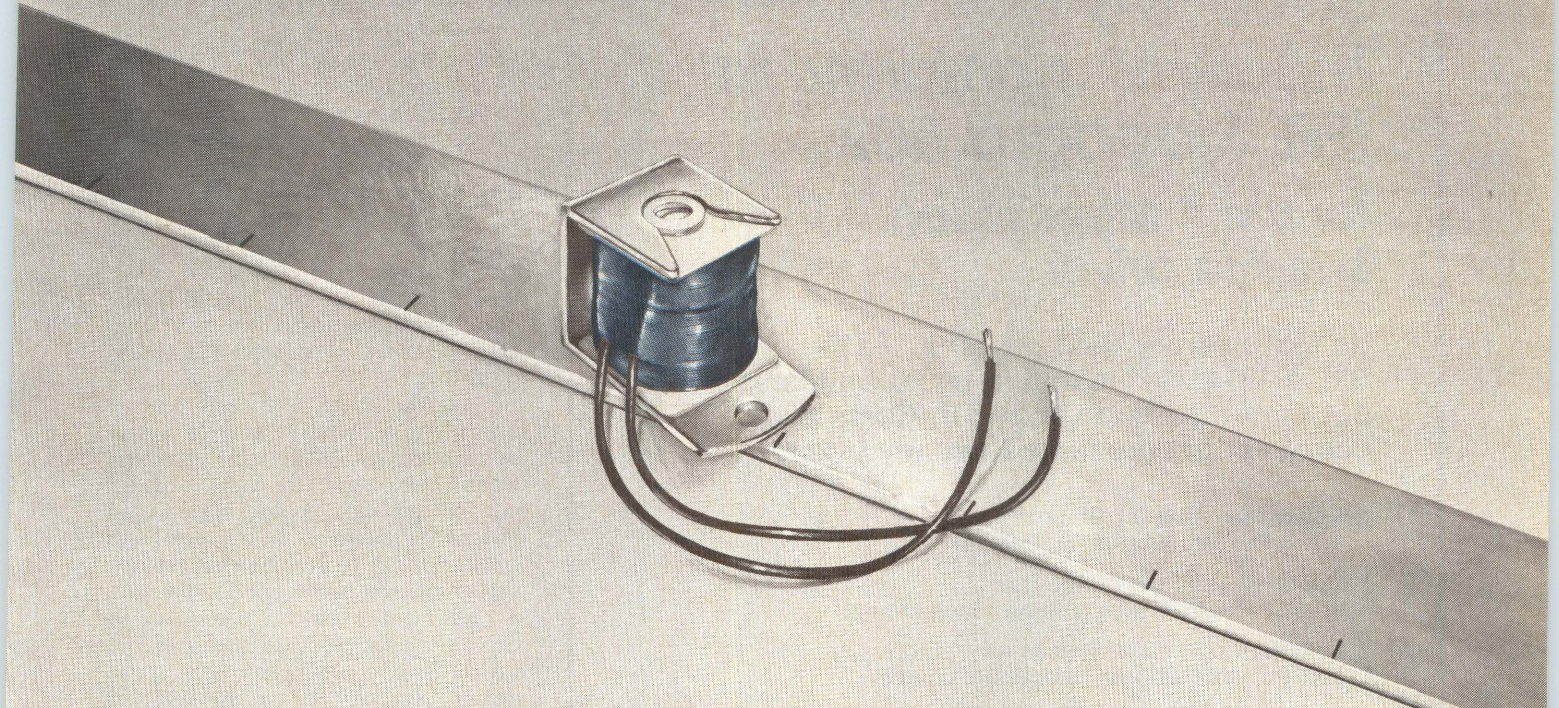
The recording disk is expected to meet all requirements of the latest proposed ANSI standard for contact start/stop storage disks with 130 mm outside and 40 mm inside diameters. This presumably leaves room for improvements in bit and/or track density like those provided by plated media, in addition to preserving a physical standard.

Dave Sutton, vice president of engineering at DMA Systems, remarked that this stage of progress in standards is unprecedented since it took place without influence from IBM, the traditional industry standard fountainhead.

While the three club members seem to agree on the mechanical aspects of removable 5¼" cartridges, questions surrounding data and servo format and error correction techniques are a different matter. Although DMA Systems submitted a draft proposal for an embedded servo format, there has been no agreement with any other manufacturer, notably Seagate, and none appears forthcoming.

Questions of agreement on format cannot be restricted to agreement among the few companies actively working in the removable cartridge area, but must
(continued on page 74)

Sound Advice
on a
Sound Device



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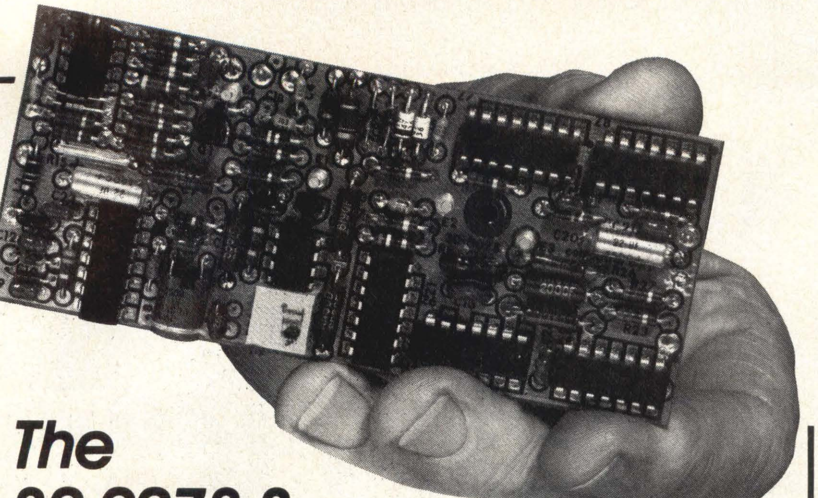

Mechanical standard close

(continued from page 72)

extend to controller design and operating systems. According to Sutton, "We are really talking about more than just a format on a disk media. We're [talking about] drive design and controller design, too."

Servo information, which lets the heads find the track, is the first level of difficulty. Then the controller must be able to read the headers. That information must be uniform as well.

However, areas where agreement is necessary go beyond this. To economically manufacture hard disks, there has to be a mechanism by which spare tracks can be substituted for one or two tracks that may have a small physical defect. This is a function normally handled by controller intelligence, as well as a function for which every manufacturer has his own approach. In some cases, though, defect mapping is done by the operating system, and there is still no agreement on a way to make all methods transparent.

Moreover, there is a great deal of diversity in approaches to error correction technology. While some controller manufacturers use Fire codes to detect and correct data errors, there is an increasing tendency to use computer generated code to avoid the pattern sensitivity inherent in Fire codes. Typically, a manufacturer pays a consultant to develop a computer generated code and adopts it as a proprietary part of his design. Obviously, no two are alike.

"All the hardware and control standardization in the world won't do you any good if you're using two different software interfaces," Sutton added. "Our level of contribution will break down at that level."

While not very optimistic about the chances for format standardization, Seagate Technology's Alan Shugart points to the value of the effort in the mechanical area: "You won't have interchangeability between one guy's cartridge and the other guy's cartridge...but at least we've provided a standard so that the cost of the cartridge can be brought down to something reasonable."

—Tom Williams
West Coast Managing Editor

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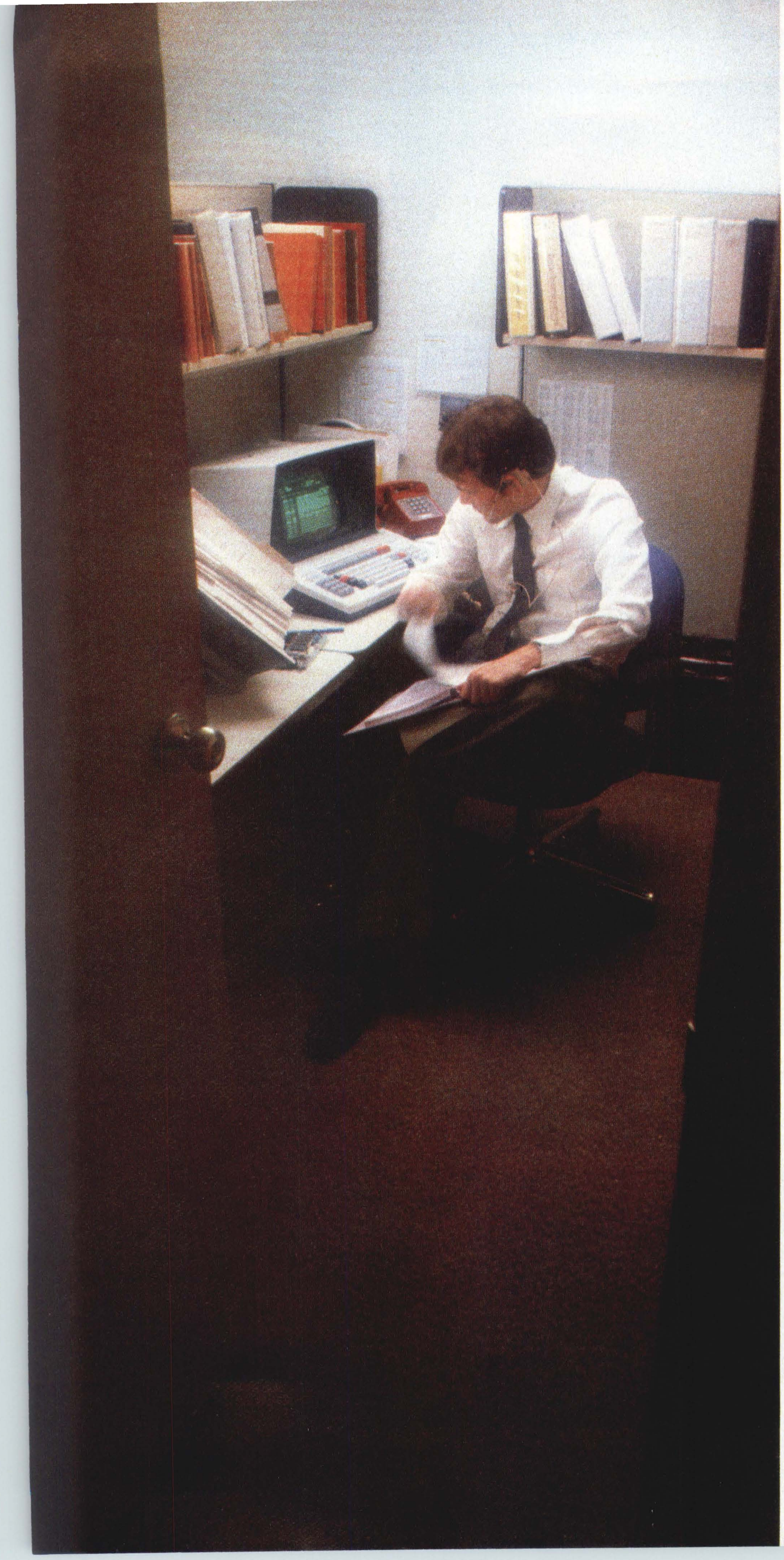

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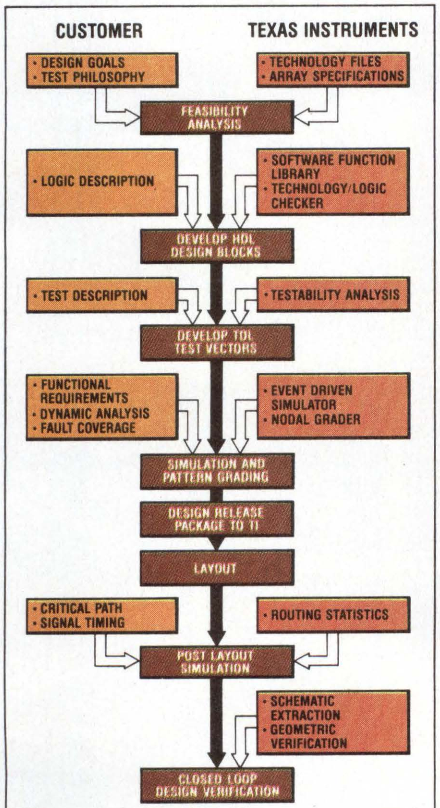

Teamwork is essential to successful logic array design. As shown, the TI design process divides responsibilities for maximum contribution by both parties and eliminates many manual, error-prone tasks.

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TAT004	400	STL	2.5 ns	600 μW	76	C/M
TAT008	800	STL	2.5 ns	600 μW	104	C/M
TAT010	1000	ASTL	1.0 ns	300 μW	88	C
TAT020	2000	ASTL	1.0 ns	300 μW	120	C/M
STL700	560	STL	3.0 ns	300 μW	61	M
SBP96700	1120	I^2L	11/15 ns	100 μW	96	M
SBP96600	2120	I^2L	11/15 ns	100 μW	140	M

*TAL Series Arrays are manually routed by you and schematically verified by TI with your software HDL model prior to prototyping.

**Usable gates

†LPS — Low-power Schottky

†STL — Schottky Transistor Logic

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†I^2L — Integrated Injection Logic

When circumstances warrant, we'll conduct the seminar at your plant.

If you want to study on your own, appropriate documentation may be obtained from TI. This consists of a detailed Logic Array Designers Manual, data sheets of logic array characteristics, information packets on library-accessible, predesigned software functions, and related technology application notes.

Where can I get actual design assistance?

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TEXAS INSTRUMENTS

27-5030

CIRCLE 49

UNDERSTANDING THE HIGH SPEED DIGITAL LOGIC SIGNAL

In the modeling of high speed digital systems, frequency analysis often misleads designers and should be avoided.

by Malcolm Davidson

There is a disturbing trend in the digital hardware industry today that holds hazardous consequences for the future. Students and practicing engineers are now developing complex systems using a black box approach. As a result, the ability to understand the fundamentals of digital electronics is lost. When boards and systems fail, individuals involved in digital engineering do not possess the knowledge necessary to analyze the failure. Sad though it is, a clear review of the exact nature of a logic signal is necessary since the majority of digital electronic engineers do not fully understand this very basic subject.*

Basic system assumptions

Five years ago, microprocessors had clock rates of about 2 MHz. Today, fabrication techniques have quickened rates to 12 MHz. Devices are now available that have very fast rise times; eg, Fairchild's FAST logic family, and Texas Instruments' AS and ALS logic families. These logic elements have registers that operate at clock rates from 150 to 200 MHz. What must be considered is how these 1- to 2-ns edges propagate throughout the hardware.

Consider the graph shown in Fig 1. This was produced by sending a fast edge down different lengths of cable and measuring the rise time of the received signal. It is clear that a 2-ns step will propagate up to about 24′ (7 m) along a twisted pair, without degradation.

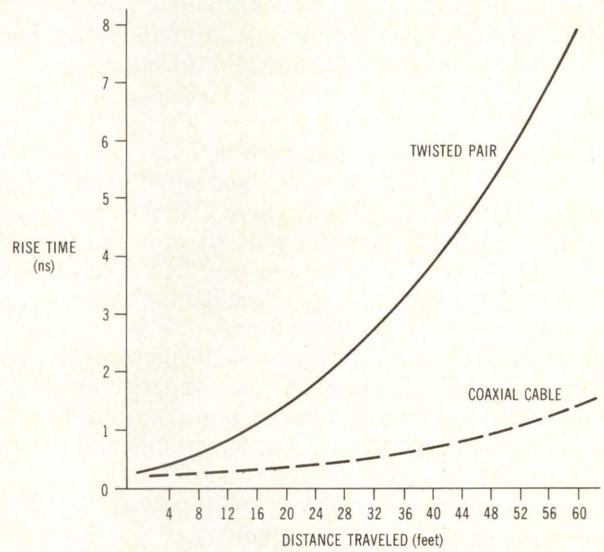

Fig 1 Signal edge rise time vs distance in two conductive mediums. Twisted pair causes virtually no edge degradation of average logic pulse under 24′ length.

Up to this length, it can be assumed that the twisted pair transmission line is a perfect medium for distribution of 2-ns edges. In other words, what comes out is exactly what went in. Therefore, the ideal, lossless

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*For a different view of digital logic signals, see the article by David Montgomery, "Borrowing rf Techniques for Digital Design," (*Computer Design,* May 1982, pp 207-217).

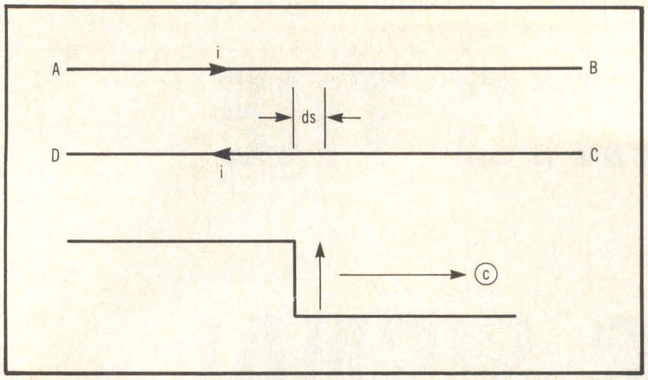


Fig 2 Transmission line equivalent circuit for digital logic signal analysis. Signal can be viewed as step propagating down each side of line.

transmission line is a good approximation to use for propagating high speed digital data in a localized system with signal paths shorter than 24′.

Transmission line properties

Consider the signal path in Fig 2, a step function (assuming zero rise time) that propagates along a 2-wire line. Using Faraday's Law, $(V - d\phi/dt)$ around the loop ABCD, and defining L as the inductance per unit length of the wire pair, $L = \phi/i$. In time t, the step advances a distance such that $\delta s/\delta t =$ ⓒ. Where ⓒ is the speed of light for that medium, the change of flux is $\delta\phi = L\delta s i$. Substitutions into Faraday's Law find the voltage applied to the line to overcome the back electromotive force (emf) and yield the equation

$$V_{ad} = L\, ds/dt\, i = Li ⓒ$$

From the definition of a capacitor, $q = VC$, and $i = dq/dt$. As before, $\delta q/\delta s = VC$, and $\delta q = VC\delta s$. Therefore, $i = VC\, ds/dt = VC$ ⓒ where C is the capacitance per unit length of the wire pair. It now follows that $c = \pm\sqrt{1/LC}$ and $V/i = Z_o = \sqrt{L/C}\,\Omega$. It can be seen that Z_o is purely resistive and is called the characteristic impedance of the transmission line.

L and C are merely functions of the permeability and permitivity of the medium, and the copper acts only as a guide for the energy propagating along the line. There is no frequency dependent component inherent in the ideal, lossless transmission line.

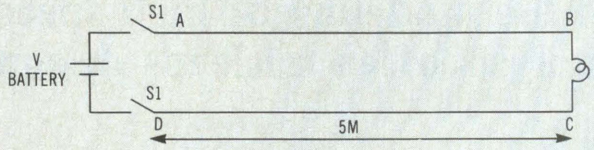
Further, Vⓒ is merely a function of μ and ϵ, and Z_o is a function of μ, ϵ, and the geometry of the line. Note that, to define these constants, a signal line and return line are needed. The Table, "Characteristic Impedances of Various Lines," lists some useful values of differing Z_o.

Characteristic Impedances of Various Lines

Line	Valve
Coaxial cable	$Z_o \simeq$ 50 to 75 Ω
Twisted pair	$Z_o \simeq$ 100 to 120 Ω
Two lines, 1″ apart (backplane)	$Z_o \simeq$ 200 to 300 Ω
Circuit board tracks	$Z_o \simeq$ 50 to 150 Ω
Free space	$Z_o \simeq$ 376 Ω

When the switch is closed

An increasing amount of information is required for today's engineering graduate to assimilate. In the quest for knowledge of "new" theories and technologies, the electronic engineering student tends only to understand on a superficial level. Because he cannot comprehend or appreciate fundamentals, he cannot develop and build reliable, complex digital systems. Below is a very basic question that should be posed to all electronic and computer engineers. The answer lies at the heart of digital electronic theory.

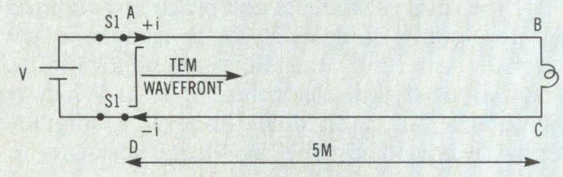


(A)

In Fig A, S1 is a switch that can connect a battery of voltage (V) to 2 wires, each 5 m long, with a light bulb at the end. For the purposes of this question, assume the copper wires to be perfect conductors (ie, zero resistance). Also, switch S1 is perfect—that is, it can close in zero time.

What happens when the switch is closed?

Because of the perfect switch S1, a zero rise time step is developed across lines A and D.



(B)

In Fig B, $V_{step} = V_{battery}$ because of the proximity of the switch to the battery. $I_{step} = V_{step}/Z_o$, where Z_o is the characteristic impedance of the 5-m interconnect, and equals $\sqrt{\mu/\epsilon}$. Thus a rise time step, or a transverse electromagnetic (TEM) wavefront, travels down the 5-m transmission line with a velocity equal to $1/\mu\epsilon$. (This would be the speed of light in air.) A + i and − i flow in the wire at the same time. When this energy (Poynting Vector) reaches the end of the interconnection BC, it sees a discontinuity. Some of the energy travels through the resistive material of the light bulb, illuminating it. The remainder is reflected back toward the battery. Eventually, all reflections cease.

Signal propagation on a board

On a typical logic board, a fast step will travel 1′ (30 cm) in 1 ns. Using the ideal line as a model, characteristic impedance and the time delay ($t_D = \sqrt{\epsilon\mu}$) must be considered. Assume T1 and T2 are perfect switches as shown in the circuit of Fig 3(a). T2 has been on for a long time; ie, 0 is present, T2 goes off, and T1 goes on.

$$V_{PROP} = V_s \cdot Z_o/R + Z_o$$

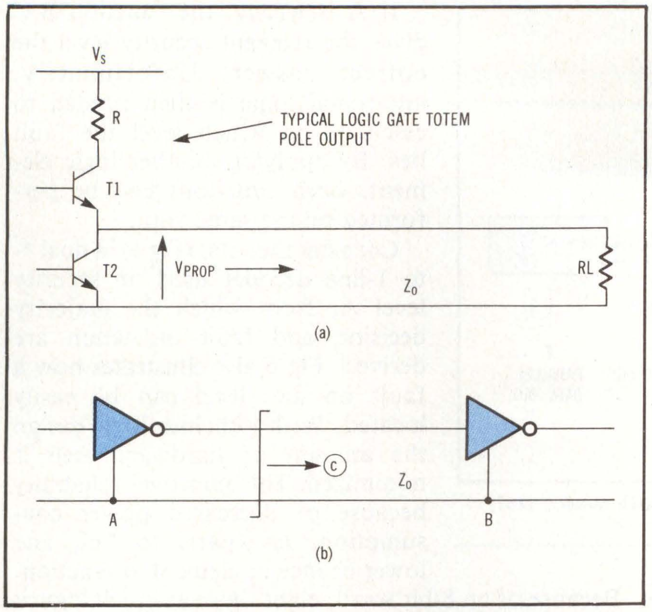


Fig 3 Logic gate action in typical digital application. Circuit of (a) shows that as signal edge travels from gate to gate (b) its amplitude is dependent on R and Z_O only.

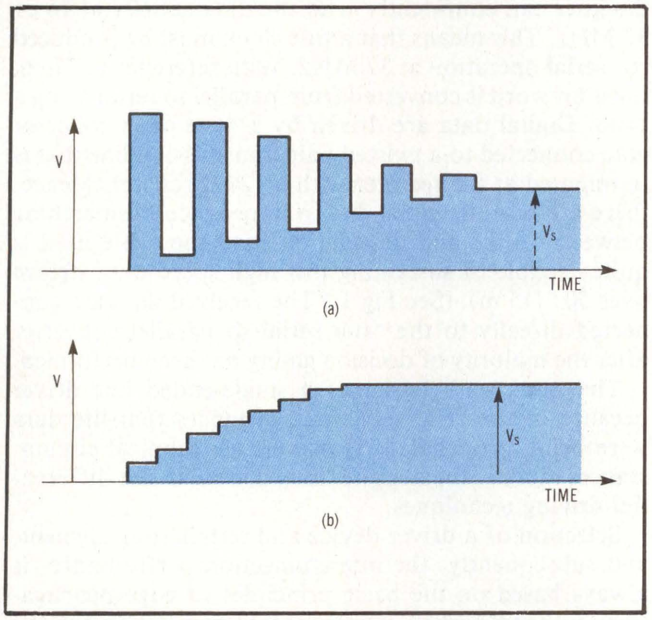


Fig 4 Digital pulse decay waveforms caused by impedance mismatch on signal lines. Vastly different waveforms associated with inductive ringing (a) and capacitive charging (b) result from differing amounts of signal reflection.

This initial voltage travels from A to B [in Fig 3(b)] at a constant speed. Its amplitude is a function of R and Z_O and has nothing to do with either the length of the line or the load (number of gates). When it reaches B unchanged, it sees a change of characteristic impedance because $R\ell$ does not typically equal Z_O. The step is reflected and the amplitude of the reflected voltage is defined by

$$\alpha = R\ell - Z_O/R\ell + Z_O$$

If $R\ell$ is ∞ (open circuit): $\alpha = 1$, the entire step is reflected giving voltage doubling, and total currents equal zero. The reflected wave travels back to A where it again reflects if $R \neq Z_O$. This process continues until all the energy initially launched from the logic gate is absorbed. If R is small compared with Z_O, and R is large, the familiar signal seen in Fig 4(a) is present. However, making R large compared with Z_O produces a totally different waveform [Fig 4(b)]. Fig 4(a) is often referred to as inductive ringing and Fig 4(b) as capacitive charging. The interconnection does not change at all in creating these different waveforms; only the value of the reflection coefficient changes.

When it is necessary to define logic signal edges in fast systems using the transmission line model, α source, t_D, Z_O, and α load are calculated. Frequency does not enter into the analysis at all.

By characterizing connections for a leading edge and a trailing edge, the design engineer can confidently produce systems that work over any data rate, be it 1 MHz or 100 MHz. Regardless of frequency, nothing at the component level has changed except there are more edges on the line at higher data rates.

Viewing logic signals in a frequency domain is ill-advised, since the initial voltage on the line between the two logic gates, V_{PROP}, can only be a function of Z_O and R because it cannot "see" ahead of itself. The signal travels at the speed of light, so it will only encounter the load and any discontinuity on the line when it is reached. Thus, companies that issue switching specifications using lumped components (15-pF capacitors) are of no help to the logic designer, who always works in a distributed world with time delays and various load conditions. If a signal return line is not used, Z_O cannot easily be defined and also changes along the transmission line. The prudent designer must assess whether his logic signals can have 5 to 10 ns worth of reflections on each rising and falling edge.

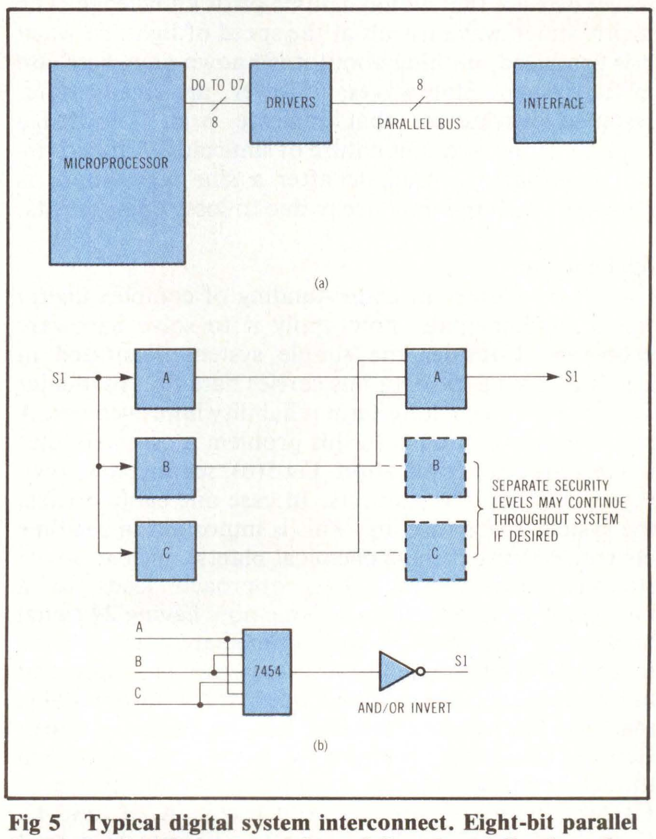


Fig 5 Typical digital system interconnect. Eight-bit parallel data bus of (a) is protected from failure by triplication of signal paths (b). Inevitable increases in wire reduce reliability and foster noise and crosstalk problems.

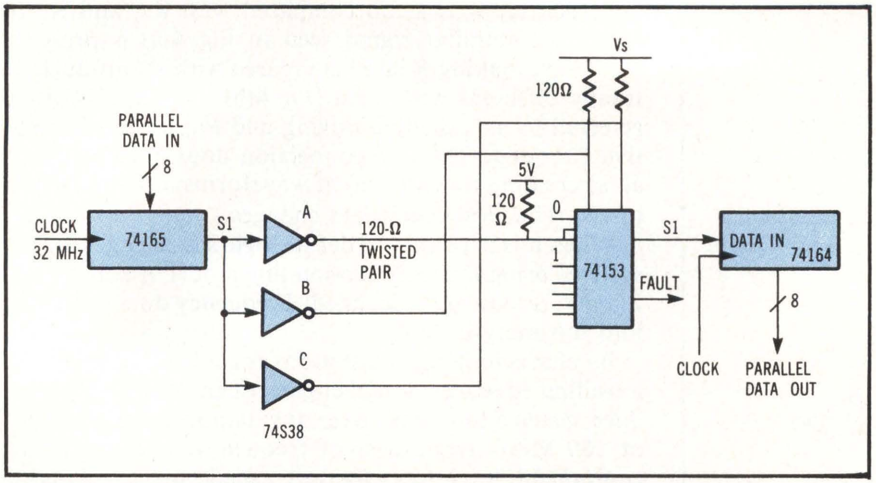


Fig 6 Triplicated serial data system using three twisted pairs. Both source and return lines must be connected close to integrated circuits.

Realtime logic signals

If it is understood how any particular connection responds to either a positive edge or a negative edge, then all signal possibilities have been covered. Therefore, a logic gate will react in exactly the same way to all edges, be they part of a square wave, or part of a random (realtime) digital sequence. Additionally, a logic element does not "know" a square wave from any other type of signal. It only reacts to edges as they reach the gate.

As a result, a digital designer should never use the concept of frequency in logic systems; neither should he consider using Fourier analysis on these logic signals. A gate can never predict the arrival of a logic signal (shock wave) because that would assume prior knowledge. The digital shock wave travels at the speed of light, so when it is produced, nothing about it is known anywhere else in the system. Sine waves, however, are steady state, resonant waveforms that indicate prior knowledge because of the resonant nature of sinusoids. A tuned circuit continues to oscillate after a sine wave input is removed, with the only decay due to lossy components.

Applications

Having developed an understanding of complex digital signal fundamentals, now apply it to solve hardware problems. Consider the simple system illustrated in Fig 5(a). This 8-bit data bus carries data to a particular interface requiring long-term reliability improvement. A conventional approach to this problem most likely uses the technique of triplication, Fig 5(b), sending data over three identical interconnects. In case one cable breaks, the system keeps running. This is important in realtime control systems such as chemical plants, nuclear power stations, and aircraft. This approach leads to a backplane or interconnect scheme now having 24 signal lines. The increase in wire immediately lowers the inherent system reliability and increases crosstalk and noise problems. Thus, in the quest for a more reliable machine, the unwary designer has the opposite effect. Before retreating completely from this approach though, consider how it is applied. As illustrated in Fig 5(b) there are three security levels: A, B, and C. Considering one signal line only (two wires), the output signal can be defined as S1. Therefore, S1 = A.B + B.C + C.A. This can be implemented using a 7454 gate.

If A is wrong, the function B.C gives the relevant security level the correct answer. Unfortunately, additional logic is then needed to calculate on which level the fault lies. By applying another logic element, both functions can be performed on the same chip.

Consider the 74153 (Fig 6), a dual 4- to 1-line decoder used on security level A, from which the majority decision and fault indication are derived. Fig 6 also illustrates how a fault on any level can be easily located. With judicious logic design the amount of hardware used is minimized. This improves reliability because of decreased power consumption, less parts to fail, and lower chance of element interaction.

Because of an 8-bit word, eight times as much logic is needed. If the transmission line model for interconnection is applied, then instead of having a 2- to 4-MHz clock and data rate with parallel distribution, the designer can confidently send the data serially at 16 or 32 MHz. This means that a fast clock must be produced for serial operation at 32 MHz. With reference to Fig 6, the 8-bit word is converted from parallel to serial using a 74165. Digital data are driven by a 74S38 open collector gate connected to a twisted pair transmission line that is terminated at the receiver with a 120-Ω resistor. Hence, there are no reflections due to impedance mismatching between source and destination, and the cable used is quite capable of sustaining this high speed data stream over 50′ (15 m). (See Fig 1.) The received data are connected directly to the 74164 serial to parallel converter after the majority of decision gating has been performed.

The 74S38 was chosen as a single-ended line driver because of the relatively short distances that the data were being propagated. However, as technical circumstances dictate, the designer may choose to use differential driving techniques.

Selection of a driver device and terminating element, and subsequently, the interconnection performance, is always based on the basic principles of edge propagation outlined earlier. The concepts mentioned are the first steps in designing and building more reliable digital systems.

Digital systems differ greatly from analog systems and demand radically different design techniques. Though there is an immense gulf between the two, designers constantly attempt to bridge this gap and use quite inappropriate techniques to solve problems they do not fully understand. Hopefully, this article has shed some light on what exactly a logic signal is and how it can be conceptualized on a fundamental level.

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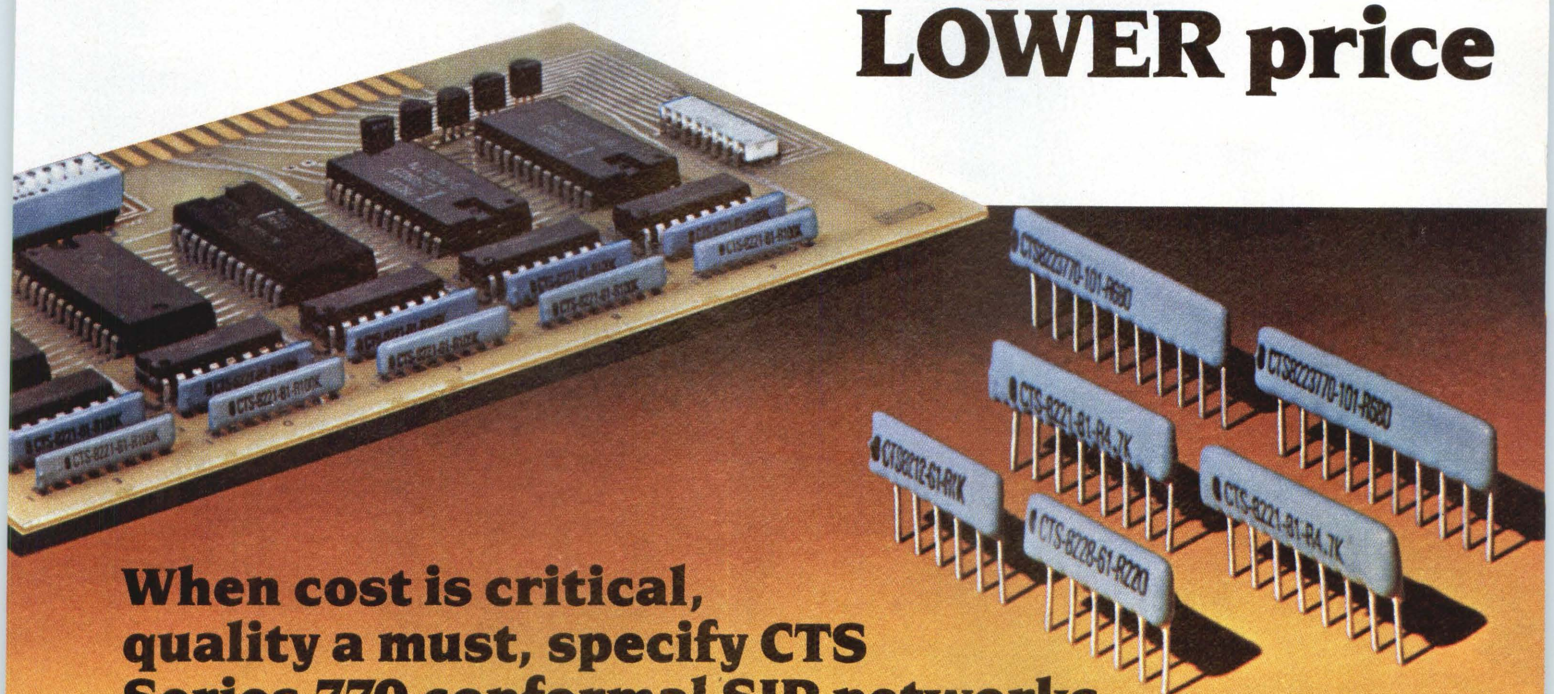

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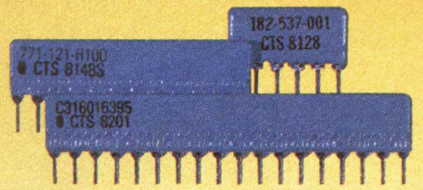

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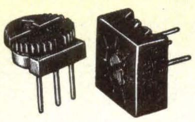

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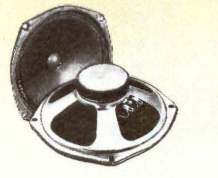

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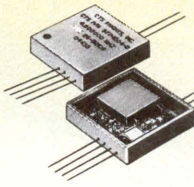

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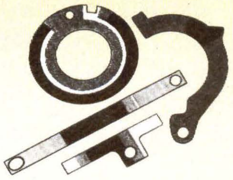

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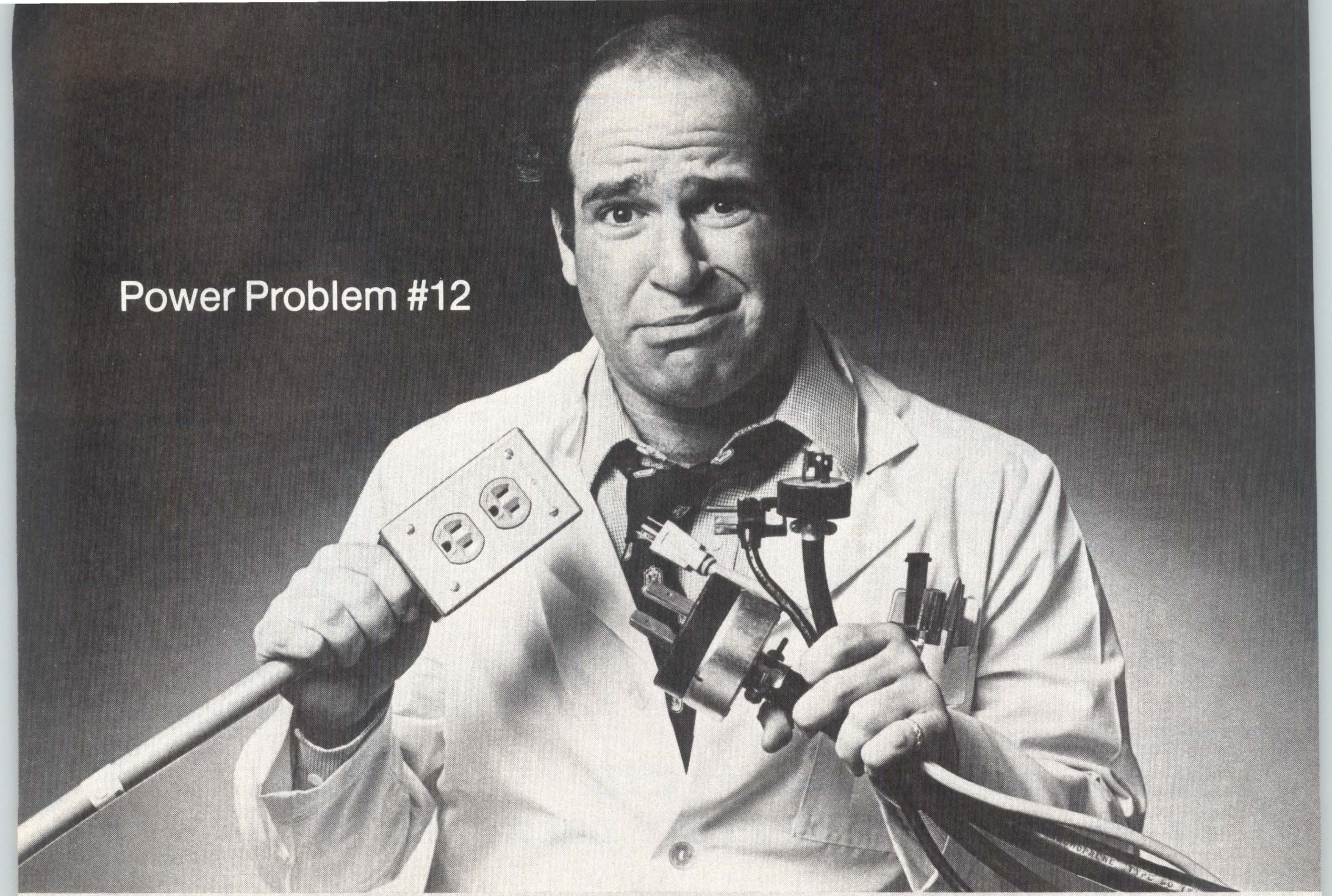

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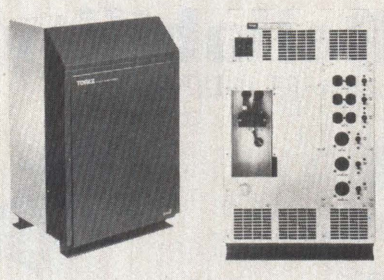

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TOUGHER RULES BEING SET TO GOVERN SYSTEM NOISE

European regulatory agencies are taking an aggressive stance on acoustic and rf emissions of computer systems. Here is a guide to the coming rule changes and the agencies behind them.

by Gary W. Collins

American computer equipment manufacturers who want to broaden their customer base to European markets face a confounding situation. At first glance, there appears to be a melange of regulatory bodies in the European theater that rivals the gaggle of American industry overseers. Faced with cryptic acronyms like DIN, VDE, and IEC, most American manufacturers marketing products in Europe choose the path of least resistance to deal with these organizations—they simply ignore them.

Unfortunately, this head in the sand approach will not work much longer. Increasing workplace awareness of both blue- and white-collar European workers, in union with renewed social activism, is bringing many European regulatory agencies to the fore. While West German acoustical regulations covering computer equipment are being tightened, several other European countries are drafting similar legislation. All computer manufacturers, especially those in the United States, will soon be affected.

For American manufacturers selling abroad, the consequence will be greater product scrutiny by the organizations concerned. In fact, the limits of that scrutiny are expanding to include acoustical as well as radio frequency (rf) emissions, in both large and small data processing (DP) settings.

Confusion in the DP equipment manufacturing industry has existed for some time as to the extent, and impact, of German acoustical requirements. These are presumably the toughest requirements in the world, but what exactly *do* they require? What does it mean for U.S. built machines? Moreover, since U.S. manufacturers export to Germany, why have they not been hit harder by these restrictions? The answers are emerging from foreign customers, domestic computer manufacturers who are faced with these restrictions, and standards committee members involved in interpreting them.

In the German market, computer manufacturers will be required to take the following steps: acoustical labels will have to be put on most, if not all, machines; most present tape products will have to be quieted 4 to 5 dB; and most present disk products will have to be quieted 4 to 9 dB.

Players in the game

To unscramble the European regulatory maze, as well as examine the acoustic, electromagnetic interference (emi) and labeling requirements that must be met by American computer hardware operating in European installations, the players in the regulatory game must be identified. It is difficult, however, if not a bit inaccurate, to compare German or European standards organizations with what appear to be their U.S. counterparts. According to one source, Verband Deutscher Elektrotechniker (VDE) writes standards similar to the Institute of Electrical and Electronics Engineers (IEEE) and has the certification power of the Underwriters Laboratories (UL); the West German

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OSHA noise limits

OSHA identifies permitted exposure for three noise types. A hearing test is also part of the OSHA noise regulation. Although most computer rooms do not reach these levels, this information is provided for reference. The average U.S. computer room is 75- to 80-dB(A) sound pressure level.

Steady level noise

Sound level dB(A)	Time permitted (hours-minutes)	Sound level dB(A)	Time permitted (hours-minutes)
85	16-0	101	1-44
86	13-56	102	1-31
87	12-8	103	1-19
88	10-34	104	1-9
89	9-11	105	1-0
90	8-0	106	0-52
91	6-56	107	0-46
92	6-4	108	0-40
93	5-17	109	0-34
94	4-36	110	0-30
95	4-0	111	0-26
96	3-29	112	0-23
97	3-2	113	0-20
98	2-50	114	0-17
99	2-15	115	0-15
100	2-0		

Varying level noise

Exposures to continuous noise at two or more levels may not exceed a daily noise dose (D) of unity

$$D = \frac{C_1}{T_1} + \frac{C_2}{T_2} + \ldots + \frac{C_n}{T_n}$$

where

C_n = actual duration of exposure (hours)

T_n = noise exposure limit (hours) from the preceding table

Impact noise

Peak sound pressure level (SPL) determines maximum number of impacts/day

dB SPL	Impacts/day
140	100
130	1,000
120	10,000
110	100,000

Exposure to impact noise must not exceed 140-dB peak SPL as measured with a peak-hold responding sound meter.

Hearing conservation

A hearing conservation program includes at least an annual audiometric test for employees exposed to noise levels greater than 85 dB(A) for 8 hours.

Deutsche Institut fur Normung (DIN) is similar to the American National Standards Institute (ANSI).

In Europe, standards writing bodies cooperate closely with government offices and are often quasi-government agencies. Thus, their standards have a more mandatory flavor. Laws, standards and measurements, and enforcement matters tend to be coordinated in an ongoing fashion. In Germany, for example, the Work Place Law establishes the regulations, the Bundespost enforces the regulations, and VDE provides the standards and instructions to measure compliance or noncompliance with the standards. Compliance with an established standard is much more voluntary in Europe, and there may or may not be a specific law or regulation to give it "teeth."

In Germany, VDE is older than DIN and dominates the electrical and electronics areas. VDE is roughly 60% electronics (chips, semiconductors, radio frequency interference, and emi) and 40% electrical (fuses, transformers, and component parts). DIN, on the other hand, is 10% electronics and 90% electrical, plus acoustics. VDE and DIN overlap at times, and there is increasing coordination and joint numbering of the standards. VDE's rf standards are not tougher on the whole than the Federal Communication Commission's (FCC). Work is under way to harmonize UL standards with International Electrotechnical Commission (IEC) guidelines.

In America, the Occupational Safety and Health Administration (OSHA) is the regulatory agency that covers acoustics (see the Panel, "OSHA noise limits"). Other organizations in the United States are not involved with acoustic limit setting. OSHA regulations ensure workplace safety and compliance with appropriate existing regulations. While OSHA has groups studying rf and emi effects (rfi nonionizing body effects, microwave emissions in wafer fabrication, video display terminal, and x-ray radiation), they are reluctant to commit to any rf guidelines not covered in ANSI's 1971 works or guidelines that differ from those of the FCC.

Acoustical laws and regulations that concern American manufacturers are the 1975 German Work Place Law; German DIN Standard 45635, Teil 19, "Measurement of Airborne Noise Emitted by Office Machines"; and a drafted regulation scheduled to become law that requires sound labeling on all machines.

Work Place Law

The heart of the matter is the 1975 German Work Place Law, similar to the OSHA law, which makes the country's concern for a safe worker's environment official. England, Norway, and Sweden are working on adopting similar laws.

The Work Place Law does not specify machine noise levels. Rather, it is a noise immission law concerned with the noise a worker encounters during a day, measured at his desk or terminal. It states that environments such as operations centers must be below 70 dB(A), adjusted for impulsive noise; offices where mental concentration is required must be 55 dB(A) or below. This dB(A) measurement is an A-weighted scale where the mid-tones are emphasized to approximate the human auditory range.

The Work Place Law spawned other requirements, including regulations about how to measure noise, and a labeling law. From the equipment manufacturer's standpoint, things are no clearer now than before. What it means to the United States remains the question. A scramble within the German government and the international DP industry to interpret the law was, and still is, underway. The full implications of the law have not been felt because, apparently, the storm is still gathering. All the regulations and techniques to drive the law are not firmly in place. It is important to understand this, lest U.S. manufacturers think they can continue to get by as they have for the seven years since the law went into effect.

Measuring requirement

The second requirement, partially prompted by the first, is the German standard DIN 45635, Teil 19, "Measurement of Airborne Noise Emitted by Machines," which tells how to measure the machine-emitted noise. The specification says that four quantities need to be measured:

- dB(A) sound pressure level at certain spots over a measuring surface, specified by International Standards Organization (ISO) 3745, using the slow time constant
- dB(A) sound pressure level at the operator's position, using the impulse time constant (this may be the same placements as above, if no defined operator's position exists)
- dB(A) sound power level, according to ISO 3745
- octave band pressure levels, flat weighted, in 125-Hz to 8-kHz octave bands

The DIN specification is not concerned with how loud the noise is or what portion falls on the listener's ears, but it can be used to predict a listener's dose. It also does not specify how information shall be presented or labeled, but only that it should be presented. What it does is state what sound to measure and how to make the measurement. These qualities are necessary because they are used in the third law to state the machine sound level.

Labeling requirement

The third regulation requires all machines sold in Germany to display a label that states the sound power emission level if that level exceeds 65 dB(A) (6.5 bels). This level was chosen because the German Ministry of Labor correlates it with the Work Place Law 55-dB(A) emission level. This does not mean that a machine will necessarily be rejected if it exceeds 65-dB(A) sound power, but that anything over this level must be labeled.

Acceptance or rejection is the customer's prerogative. Because this information must be used to determine if he meets the Work Place Law requirement, the customer will no doubt add noise to the machine's performance equation—a variable that could be significant. Machines that are otherwise competitive will be rejected for noise because the customer does not want government or union interference with his operation.

Furthermore, the value on the label must be the maximum guaranteed noise value that can be measured on any sample of the machine that a manufacturer produces. For statistical reasons, the maximum guaranteed noise volume is judged to be 5 dB greater than the measured average value. Thus, even if a machine produces 60-dB(A) sound power—approximately 50-dB(A) sound pressure—it must be labeled. This assures that virtually all data and office products will have to be labeled. For example, even an average overhead projector is about 52-dB(A) sound pressure.

Implications

To meet the Work Place Law requirements, the noise level that machines have to meet is still unclear. The interpretation effort focuses on converting the *immission* requirements for workers to *emission* requirements for typical machines. To find an answer, one must work backward, from the requirement that a worker would receive no more than 70-dB(A) impulsive for an 8-hour period, toward the individual machine's emission level.

The interpretation effort focuses on converting the immission *requirements for workers to* emission *requirements for typical machines.*

First, many assumptions must be made, among them room size, room sound absorbing capacity, number of machines present, arrangement and spacing of the machines, machine operating duty cycles, relative noise levels at these duty cycles, and where the operators are. Because of the variables that influence a calculation, the best course is to take typical, "model" representative rooms. However, that will still only provide a close estimate. But, with careful attention to detail, the calculations should be within 2 dB of actual situations—close enough to let manufacturers know if they are in real trouble or not. Moreover, acoustical prediction formulas vary, but the chosen formulas are sufficiently accurate and have been checked in a DP center.

The mathematical model was programmed and used to predict new situations. Three cases were taken to see at what sound level manufacturers' machines must operate to meet German requirements. In Case I, the following assumptions were made about a medium to large DP center: 80′ x 70′ (24 x 21 m) room size; hard removable tile floor, α = 0.03, noise absorption coefficient; hard walls, α = 0.03; acoustical tile ceiling, α = 0.70 at 500 Hz; layout and machines as shown in a DP room; machine surfaces = floor, α = 0.03, are essentially reflective baffles; and machine duty cycle, 30% in read/write mode, 20% in column loaded mode, and 50% in standby mode over eight hours. (See Fig 1.)

Considering only the tape drive area, where the operator is near the machines, the noise contribution

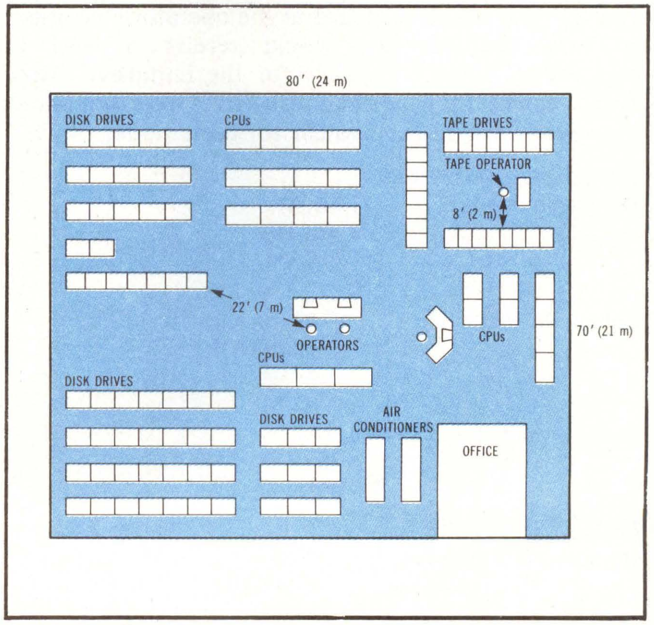

Fig 1 Physical layout that serves as basis of mathematical model of medium to large DP center used to determine acoustic measurements

from each machine is as follows: direct sound is the contribution coming directly from the machine

$L_{ID} = L_{PAI} + 10 \log k - 20 \log R_2/R_1$

where

L_{ID} = impulsive sound pressure level due to direct sound, in dB

L_{PAI} = a weighted impulsive sound pressure level measured 1 m away from the machine at bystander's distance (per ANSI S1.29, 1979)

k = 1 if machine is well away from wall
= 2 if machine is near one wall
= 4 if machine is near two walls (a corner)

R_2 = distance from operator to machine in feet

R_1 = 1 m (3.28 '), ANSI measuring position

Reflected sound is the contribution independent of location in the room

$L_R = L_{WA} - 10 \log a + 16.4$ dB, classical reverberant field equation

where

L_R = reflected sound pressure level, dB
= a weighted, nonimpulsive sound pressure level due to reflected sound

L_{WA} = a weighted sound power level of machine

a = room absorption, sabins = $\Sigma\, \alpha_i S_i$

where

α = absorption coefficient as above

S = wall surface area, feet

The total noise contribution from reflected and direct sources for each machine, adding decibels as powers, is

L_{PAI} total $= 10 \log (10^{0.1 L_{ID}} + 10^{0.1 L_R})$

Using this formula, and adding at the tape operator's position—the critical position in this case—the contribution of each individual machine below will meet the 70-dB(A)I German standard at the operator's position. In fact, the operator would receive a level of 68.5 dB(A)I, where I stands for the impulsive dB(A) measurement if the tape and disk drives were the following values, roughly equivalent for each mode:

Tape drive levels must be

Running mode	L_{WA}	71 dB(A)
	or L_{PAI}	63 dB(A)I
	or L_{PA}	61 dB(A)
	or NC	56
Column loaded mode	L_{WA}	69 dB(A)
	or L_{PAI}	60 dB(A)I
	or L_{PA}	59 dB(A)
	or NC	54
Standby mode	L_{WA}	66 dB(A)
	or L_{PAI}	57 dB(A)I
	or L_{PA}	56 dB(A)

Disk drives must meet

Running (all modes)	L_{WA}	73 dB(A)
	or L_{PAI}	64 dB(A)I
	or L_{PA}	63 dB(A)
	or NC	61

In Case II, the following assumptions were made for a small DP center: 24 ' x 20 ' (7 x 6 m) room size, with acoustical coefficients as before; and six tapes and three large disks. (See Fig 2.) In this case, the machines must be quieter than in Case I. With the machines operating as quietly as is economically practical, the operator is still subjected to a noise level of 69.5 dB(A)I. Thus, the machines barely meet the 70-dB(A)I requirement.

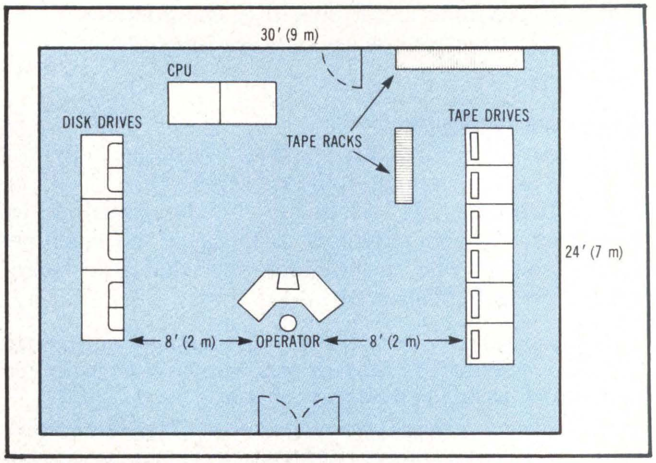

Fig 2 Physical layout of small DP center used in acoustic calculations and measurements

Tapes must be

Running mode	L_{WA}	70 dB(A)
	or L_{PAI}	62 dB(A)I
	or L_{PA}	60 dB(A)
	or NC	55
Column loaded mode	L_{WA}	69 dB(A)
	or L_{PAI}	60 dB(A)I
	or L_{PA}	59 dB(A)
	or NC	54
Standby mode	L_{WA}	66 dB(A)
	or L_{PAI}	57 dB(A)I
	or L_{PA}	56 dB(A)

Disk must be

Running (all modes)	L_{WA}	69 dB(A)
	or L_{PAI}	60 dB(A)I
	or L_{PA}	59 dB(A)
	or NC	57

In Case III, the following assumptions were made for an office or design area: one small tape drive and one small rackmounted or tabletop disk; good sound treatment of walls, $\alpha = 0.70$; fiberglass cloth covered partition dividers; and carpet, $\alpha = 0.20$. (See Fig 3.)

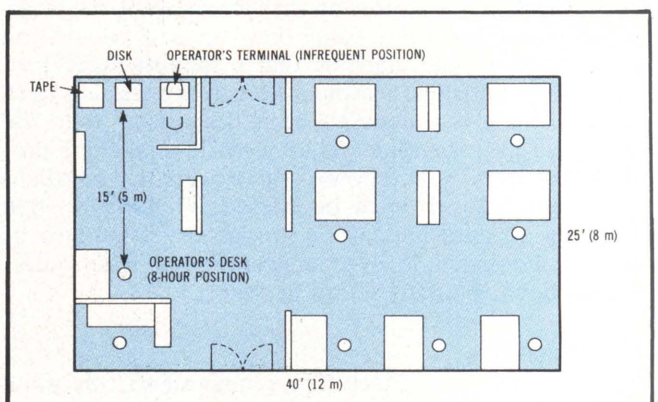

Fig 3 Physical layout of office/design space used in calculations and measurements of acoustic levels

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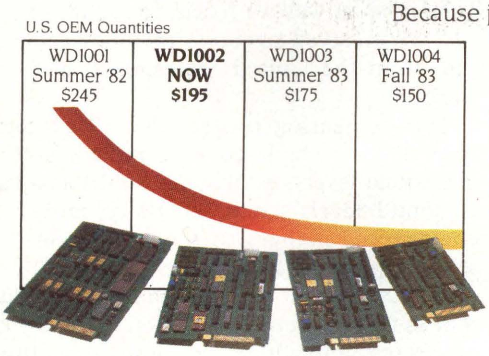

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For the design area, 55 dB(A)I is the standard to achieve. The tape drive must be lower than what normally can be achieved with a high performance vacuum column machine, and the disk must be a quiet 56 dB(A). Even at this, the operator's desk would receive 55.1 dB(A)I, slightly over the German requirement of 55.0 dB(A)I.

Tape must be

Running mode	L_{WA}	69 dB(A)
	or L_{PAI}	61 dB(A)I
	or L_{PA}	59 dB(A)
	or NA	54
Column loaded mode	L_{WA}	68 dB(A)
	or L_{PAI}	59 dB(A)I
	or L_{PA}	58 dB(A)
Standby mode	L_{WA}	64 dB(A)
	or L_{PAI}	55 dB(A)I
	or L_{PA}	54 dB(A)

Disk must be

Running (all modes)	L_{WA}	66 dB(A)
	or L_{PAI}	57 dB(A)I
	or L_{PA}	56 dB(A)
	or NC	54

Of the three cases, the small design office is the limiting case. The office requirement can almost be met with quieted DP center machines, but, since it is not practical to tailor the acoustics or performance of present high performance machines for the small office, manufacturers in the high end of the DP industry may choose not to be bound by the low noise levels required for offices. Office/word processor manufacturers must make special efforts to conform to the small-office proposed standards. Even the required noise levels of 70 dB(A)I for DP centers, which are modest, will keep manufacturers busy.

Meeting requirements

To meet the emerging German DP center requirements, it is estimated that manufacturers' machines must meet the following levels: *tape drives*—70-dB(A) sound power, roughly NC55 or 60-dB(A) sound pressure; and *disk drives and other steady sources*—69-dB(A) sound power, roughly NC57 or 59-dB(A) sound pressure. To meet the German office environment requirements, where mental concentration is required, it is estimated that manufacturers' machines must meet the following levels: *tape drives*—69-dB(A) sound power, roughly NC54 or 59-dB(A) sound pressure; and *disk drives and other steady sources*—66-dB(A) sound power, roughly NC54 or 56-dB(A) sound pressure.

Sound power emission labels must be prepared for all products. Although the exact format has not been finalized, the labels will have the following general appearance:

Larm
Bruit $\quad L_{WA} = \dfrac{\text{dB}}{\text{Re } 10^{-12}\text{ W}}$
Noise
Rumore $\quad$ per ISO...ECMA*...

Many tape products marketed in Europe need to have their noise levels reduced by an average of 4 to 5 dB. Manufacturers should consult their acoustical department or a consultant to precisely establish the size of this job. Manufacturers should also obtain a qualified legal opinion as to the ultimate interpretation and impact of the German law and accompanying regulations. These will not be fully known until the German government implements and enforces the law.

A number of large disk products must be reduced by 5 to 9 dB—a very tall order. Small disks are much quieter but may still need attention to meet the office requirement. Again, acoustical engineers need to be consulted, and each company will have to make a cost/benefits decision based on what it will cost to reduce the machine's noise level; what the interest is in the European market; and finally, what the impact will be of European manufactured quiet machines on the American market. If American manufacturers decide to continue competing in the European market, they must also know the range of rf standards and regulations.

An example of an American company meeting the challenge of the coming German acoustical standards and laws, as well as increased domestic customer awareness of them, is Storage Technology Corp. The company doubled its full-time acoustical personnel, dedicated to silencing all models of high performance tape and disk drives, high speed printers, and telecommunications equipment. Also, the company added over 1300 square feet of acoustical engineering laboratories to increase product handling ability. A semi-anechoic room was built for sound pressure measurements and for diagnostic work in locating discrete acoustical problems. A complete reverberation room was built for easy and rapid sound-power measurements. While sound power can be measured in either room, according to the German standard and the ISO 3741 and 3745 standards, it is more easily and directly done in the reverberation room.

The latest in acoustical analyzing equipment, including realtime, one-third, and single-octave measuring devices, and separate narrow band analyzers with acoustical and vibratory pickups, is used in measurements. As a result, increased acoustical control and efforts to contain unwanted noise throughout the computer industry will positively affect domestic customers.

Additional domestic and international standards

Electronic DP equipment manufacturers not only must meet acoustical standards in the United States and Europe, but they must also conform to rigorous domestic and international rf radiation specifications that limit emissions as well as to electrical safety standards. The cast of involved agencies includes OSHA, the FCC, and the UL in the United States; DIN, IEC, and the VDE in Europe.

OSHA's hearing protection and conservation regulation 1910.95, which governs industrial U.S. workplace acoustical levels, establishes 80 dB as a safe noise level. If sound levels reach 90 dB or more, OSHA requires engineering changes to the equipment. OSHA does not set rf requirements, however, and the OSHA regulation is more lax than the 1975 German Work Place Law. OSHA makes no distinctions between different kinds of workplaces (eg, a machine shop must meet the same requirements as a data processing office, and vice versa). Although there is no plan to match the Work Place Law standards, according to an OSHA spokesperson, OSHA is

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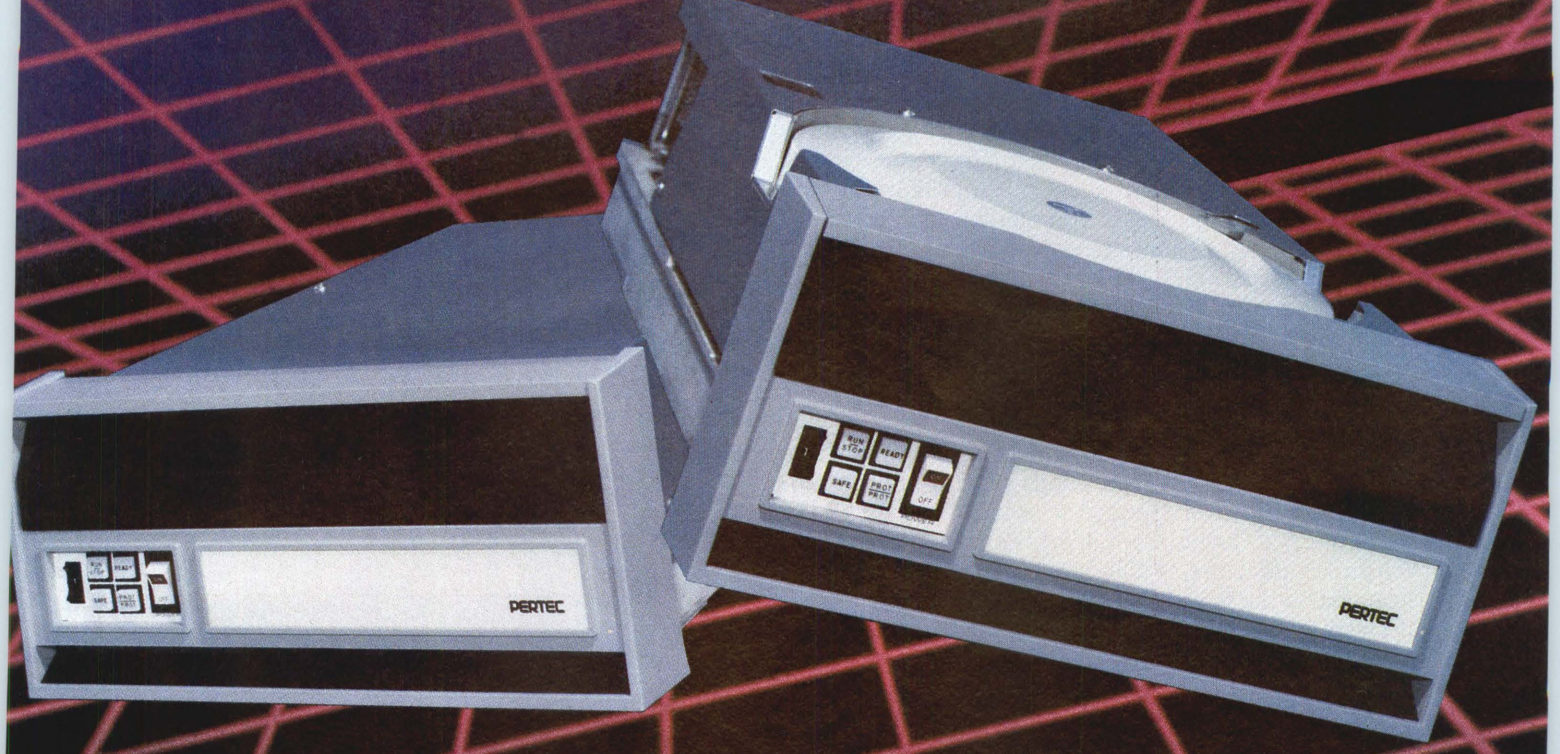

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watching the German machine engineering and design technology that reduces noise levels in industrial work areas.

Other U.S. organizations are not involved with acoustical or rfi standards. UL is primarily concerned with a system's electrical safety performance, such as safe spacing distances for power line filters, grounding, and fire hazards. Compliance with UL standards is voluntary. The U.S. Department of Health and Human Services is not involved in either monitoring or enforcing acoustical noise or rfi radiation standards.

FCC sets U.S. standards

The FCC regulates devices sold in the United States that emit rf energy. The commission uses the 1971 ANSI specifications for electrical equipment as a guideline. Restrictions of rf radiation produced by digital equipment that functionally use indirect rf energy for purposes other than communications are included in the FCC Rules and Regulations, Part 15.818.

FCC regulations for radiation and conduction limits, and performance verification and labeling requirements, address two categories of devices or systems that use digital techniques and generate timing pulses beyond 10,000 cycles/s. The first category, of primary interest here, is Class A industrial or commercial equipment; the second is Class B consumer products, such as self-contained electronic games that use digital logic generating a clock frequency below 495 kHz, personal computers and peripheral equipment exclusive of hand-held and desktop calculators or digital watches, and devices designed to interface with a television for use in residential areas.

VDE specifications for industrial equipment match, or are stricter than, FCC regulations (Figs 4 and 5). VDE measurements cover frequency ranges from 150 kHz, while the FCC ranges from 450 kHz to 30 MHz. In the consumer area, the FCC imposes tighter controls than VDE, above the 0.5-MHz ranges.

Overall, the IEC in Geneva acts as a standards and measurement coordinating organization, keeping members aware of new developments and making recommendations to member country standards bodies on an international level. U.S., Canadian, and European standards writing bodies are making a more active effort to bring their specifications into line with one another through the IEC. Eventually, this growing international trend toward standardization will help manufacturers marketing products abroad.

However, when the target is the European theater, design engineers must be mindful of Germany's VDE regarding rf radiation. A recent cooperative program in Germany calls for VDE's new standards to be adopted by DIN and vice versa, and assigned a dual reference number. Previously, such joint standards only appeared in the limited areas where DIN and VDE overlapped.

VDE specification 0871 (DIN 57 871/VDE 0871) sets rf performance standards for electrical equipment, including digital devices, that generates or utilizes either discrete or repetition frequencies above 10 kHz and are not used for telecommunications functions. (See the Table, "VDE Specifications.") To meet VDE specifications, the influence of the measurement area must be considered when field strengths are measured at other than the specified distances.

The specification does not apply to electrical equipment generating frequencies up to 10 kHz. DIN 57 875/VDE 0875 covers those devices. Both the DIN/VDE 0871 and 0875 standards are applicable as defined in the scope of each specification where equipment produces frequencies above and below 10 kHz.

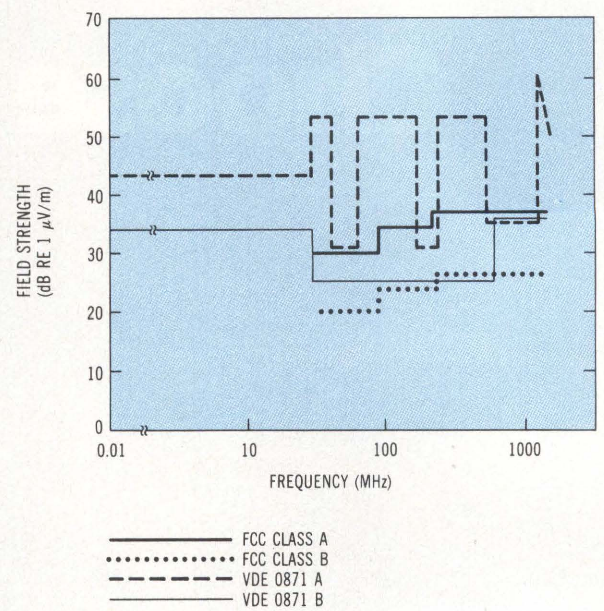


Fig 4 Comparison of FCC and VDE radiation emission limits for Class A (commercial) computer equipment. FCC is stricter in the 30-MHz to 1000-MHz region.

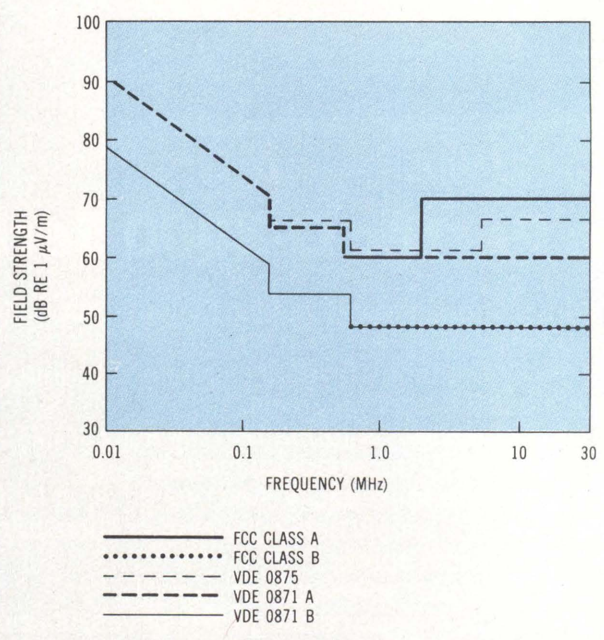
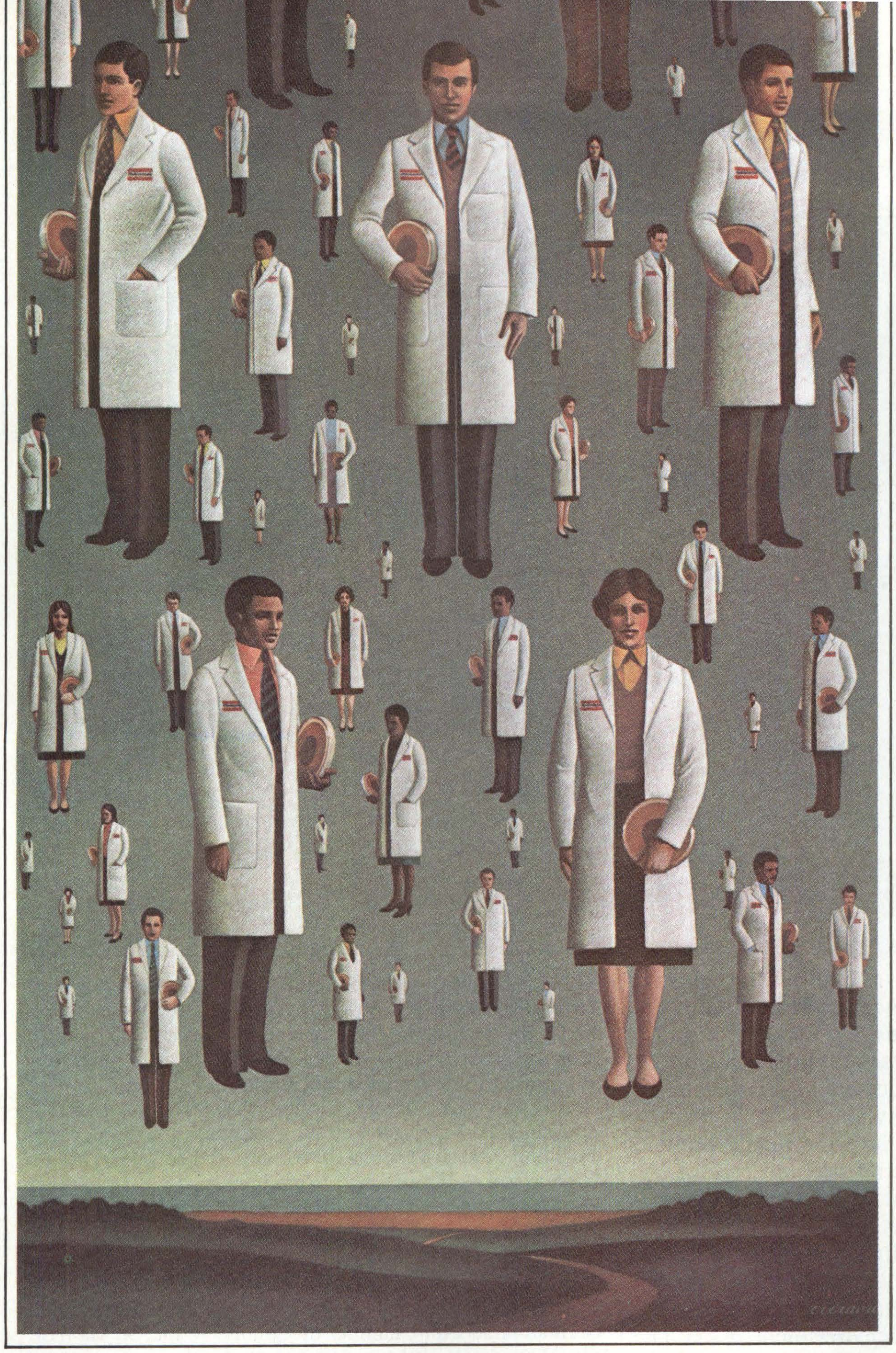


Fig 5 Comparison of FCC and VDE conducted emission limits for Class A (commercial) hardware. VDE 0871A and B curves, from 150 kHz to 10 kHz, represent proposed limits. Note that some requirement levels overlap.



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VDE Specifications

Frequency range (in MHz)			RFI field strength measured at measurement site and distance of: Limit Class A 30 m μV/m	Limit Class A 100 m μV/m	Limit Class B 10 m μV/m	Limit Class B 30 m μV/m	RFI field strength measured at operational site and distance of: Limit Class C 30 m[5] μV/m	Limit Class C 100 m[5] μV/m	300 m[6] μV/m
0.01	to	0.15[2]	—	50	—	50	—	250	200
>0.15	to	0.285	—	50	—	50	—	50	200
>0.285	to	0.49	—	50	—	50	—	250	200
>0.49	to	1.605	—	50	—	50	—	50	200
>1.605	to	3.95	—	50	—	50	—	250	200
>3.95	to	30.0	—	50	—	50	—	50	200
>30.0	to	41.0	500	—	50	—	500	—	200
>41.0	to	68.0	30	—	50	—	30	—	200
>68.0	to	87.0	500	—	50	—	500	—	200
>87.0	to	107.828	500	—	50	—	30[1]	—	200
>107.828	to	174.0	500	—	50	—	500	—	200
>174.0	to	230.0	30	—	50	—	30	—	200
>230.0	to	470.0	500	—	50	—	500	—	200
>470.0	to	760.0	180[3]	—	200	—	100	—	200
>760.0	to	790.0	—[3,4]	—	200	—	100	—	200
>790.0	to	1000.0	—[3,4]	—	200	—	500	—	200

1. Recommended value is limit = 500 μV/m.
2. Values in 0.10 to 0.15 frequency range are only recommended at present.
3. RFI field strengths are measured at a distance of 10 m at a measurement site.
4. RFI field strength is 900 μV/m at 760 MHz and decreases linearly to 700 μV/m at 1000 MHz.
5. Distances of 30 m and 100 m are measured from boundary of contiguous work areas or from industrially zoned area.
6. Distance of 300 m is measured from operating location of equipment.

DIN 57 876 Part 1/VDE 0876 Part 1 references the equipment used to measure rf interference and rf interference measurement equipment with quasi-peak indicator and accessories. VDE 0877 Part 1 and Part 2 stipulate requirements for measuring rf interference voltages and interference field strengths, respectively.

VDE qualified products falling into the higher limits are generally restricted to industrial use and receive a general purpose permit from the West German post office. Electronic devices that meet the stricter rf performance criteria require an individual permit for operation in general public, consumer locations.

In Germany, the Work Place Law obligates employers to provide a safe work environment. As consumers of regulated equipment, whether made in Europe or the United States, they protect themselves by purchasing and installing devices specified to VDE standards. VDE does not test regulated equipment unless it first receives a complaint from a user against a machine as not meeting VDE standards, and then receives a protest of that complaint from the manufacturer.

If VDE tests the equipment and it fails, the customer-employer must bring the machine up to standards to protect the employees. Although not required to do so, the manufacturer should modify the equipment designs to meet VDE requirements if future sales are planned in the German marketplace.

Further information

International Trade Administration, U.S. Department of Commerce, German Desk, Washington, DC 20230, 202/377-2841—for West German regulations and which standards apply to various areas of concern.

National Technical Information Service (NTIS), 5285 Port Royal Rd, Springfield, VA 22161, 703/487-4650—for orders of specific reports on domestic and international standards. It offers no personal guidance regarding what reports may be required for specified applications.

ANSI, 1430 Broadway, New York, NY 10018, 212/354-3300—for DIN and VDE standards in hard copy, including English versions of VDE 0871 and 0875.

Information Handling Services, 15 Inverness Way E, Englewood, CO 80112, 303/779-0600—for cross-indexed and cross-referenced data to government and military specifications, as well as catalogs from major vendors, in a 16-mm microfilm cassette system.

Techniker Uberwachung Vereine (TUV), TUV Rheinland, German American Chamber of Commerce Inc, 50 Main St, Mt Kisco, NY 10549, 914/241-2400—the only official organization in the United States licensed to test equipment for compliance with VDE specifications at either their site or at the manufacturer's facility. TUV is authorized to issue certificates of compliance recognized by both VDE and the West German Labor Department.

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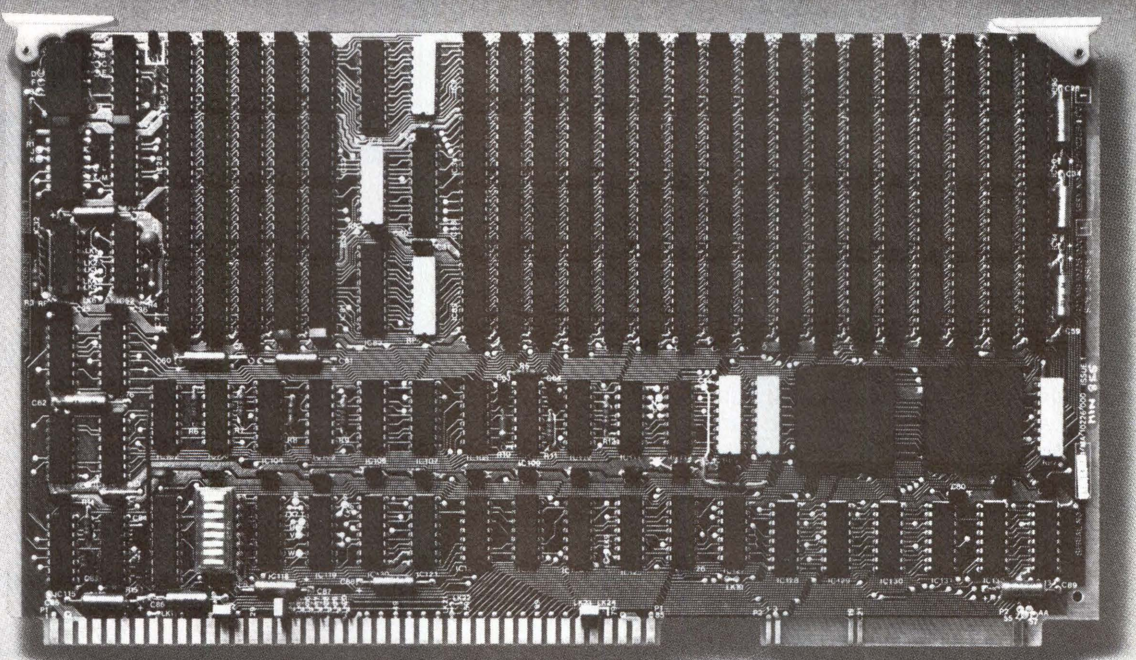

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Three EPROM MCUs.

And even with so many options among the eight HMOS types, selection of the right M6805 Family MCU is simple. The family has five basic variations and three of these are complemented by EPROM versions.

All M6805 Family MCUs are based on the same powerful, MC6800 computer-type architecture optimized for control. They use true bit-manipulation instructions and ten addressing modes, with byte-efficient, enhanced indexed addressing.

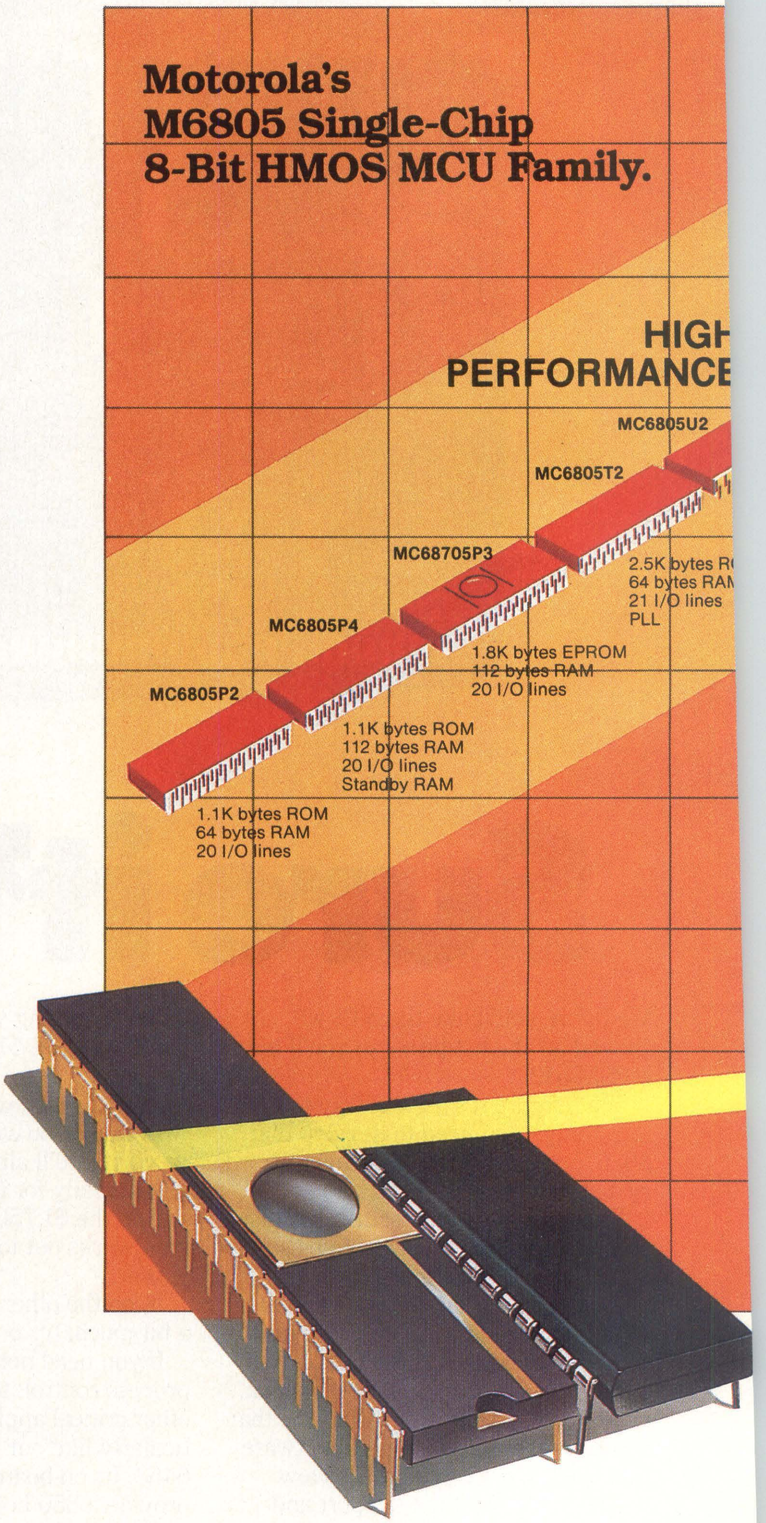
Two general purpose and three special registers are uniform for M6805 MCUs, and all eight HMOS types utilize the same basic 59-instruction set. ROM, RAM and I/O vary, and many of the M6805 Family MCUs have differing special features.

The table suggests how easy the family is to understand and demonstrates how easy it is to select the MCU that's practically tailored to your needs.

M6805 FAMILY SINGLE-CHIP, 8-BIT HMOS MCUs

	MC6805P2	MC6805P4	MC68705P3	MC6805T2	MC6805U2	MC68705U3	MC6805R2	MC68705R3
ROM (bytes)	1K	1K		2.5K	2K		2K	
EPROM (bytes)			1.8K			3.8K		3.8K
RAM (bytes)	64	112	112	64	64	112	64	112
I/O Pins Input					8	8	2-5	2-5
Program Bidirectional	20	20	20	19	24	24	24	24
Special				2			1-4 Anal.	1-4 Anal.
8-bit A/D							yes	yes
Frequency Synth.				yes				
I/O Drive Capability	12 TTL/CMOS 8 LED	12 TTL/CMOS 8 LED	11 TTL/CMOS 8 LED	11 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED
Timer Interrupts	1	1	1	1	2	2	2	2
Self Check	yes	yes		yes	yes		yes	
Bootstrap			yes			yes		yes
PLL				yes				

Powerful instructions and a large complement of addressing modes are a programmer's delight. The similarity and compatibility between M6800 and M6805 make transition from one to the other a simple matter. Simplicity, compatibility and the economy of programming ease movement among Motorola MCUs and reduce system design costs.



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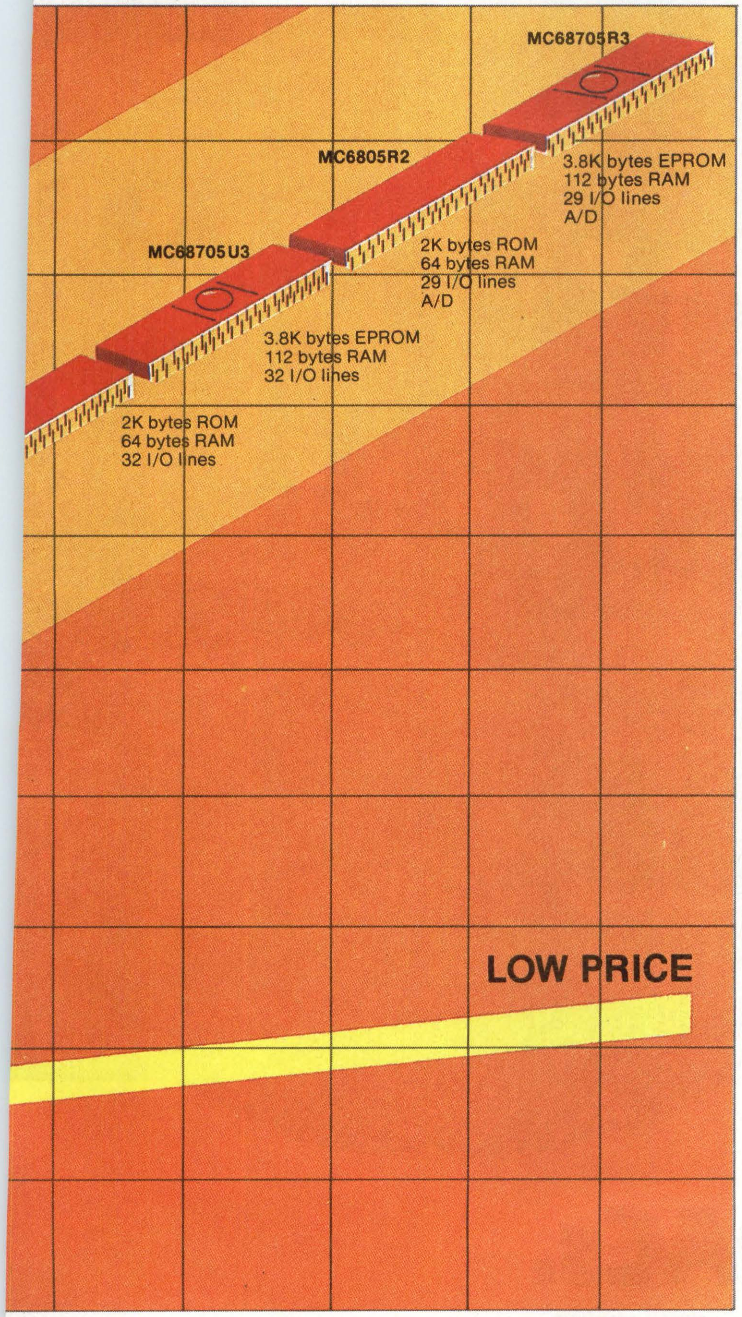

Software and hardware development for all M6805 MCU-based systems is efficiently handled by simple variations of the MEX6805 system. Each is fully compatible with both the MC6800- and MC6809-based EXORciser® and EXORterm™ development systems.

The MEX6805 provides real-time emulation capability and a complete memory map. Debugging features include trace, display of registers and memory, single-step capability, plus halt-on-address and break points. Software support is also provided on the low-cost EXORset™ development system. An inexpensive PROM Programmer supports the MC68705 MCUs.

M6805 Family MCUs also available in CMOS.

For designers of portable, battery, battery back-up and other low-power systems, the broad M6805 Family also includes three fully-static CMOS single-chip MCUs. Actually, the MC146805E2 is a ROMless unit, and the MC146805F2 and MC146805G2 have 1K and 2K bytes of mask ROM respectively. Motorola also supplies the MC146818 real-time clock for use with most multiplexed-bus processors.

For the latest information on the various MCUs, both HMOS and CMOS, write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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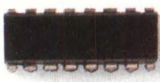
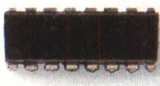


AD558 The state-of-the-art 8-bit "DACPORT." Includes reference, output amplifier and 8-bit I^2L latch. No trims required, operates on single +5V supply. $4.95 in 1,000's.



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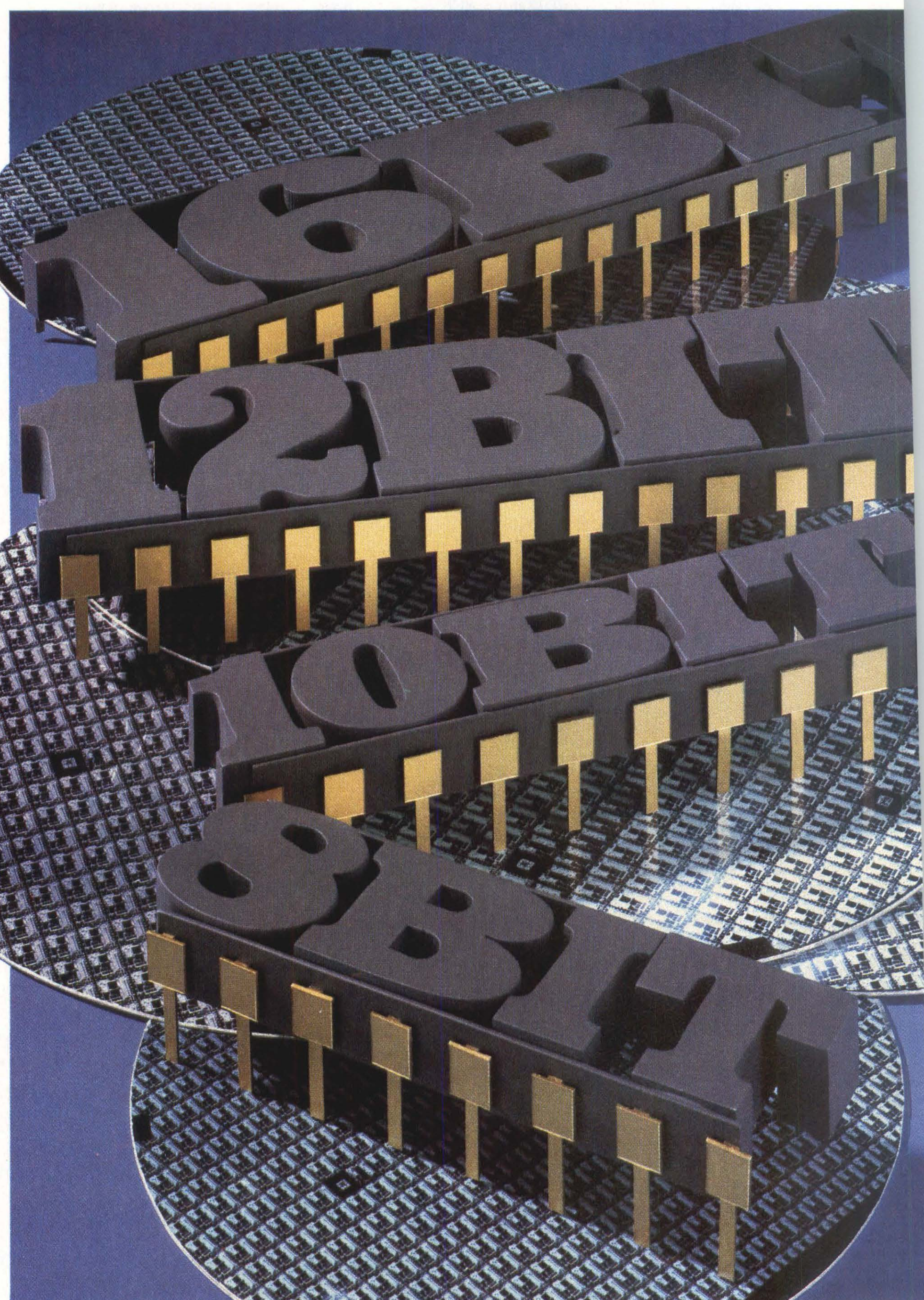

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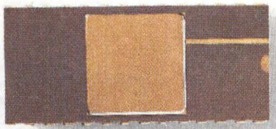

AD7527 10-bit "smart" CMOS MDAC. On-chip logic includes data readback, up-down counter, preset calibration points, 8-bit bus interface. Ideal for closed-loop control applications and smart instruments.
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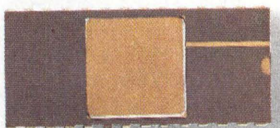

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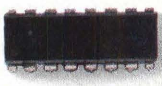

AD7542 12-bit low power CMOS MDAC in space-saving 16-pin DIP. Accepts data in three 4-bit words.
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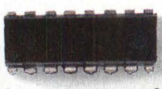

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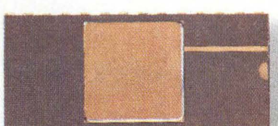

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CIRCLE 61

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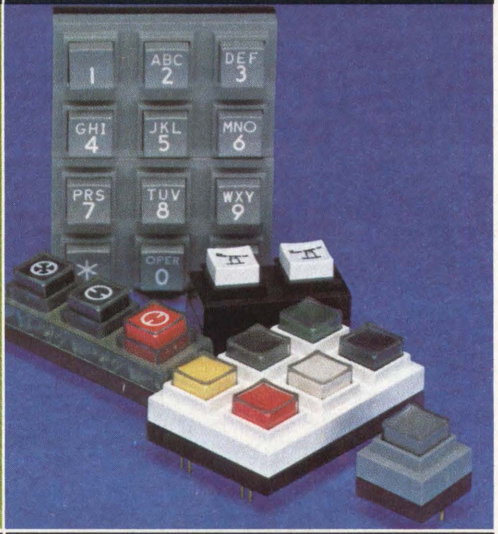
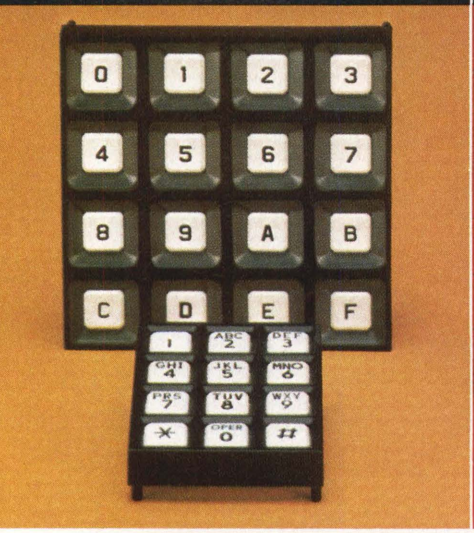


SERIES 83-84-86 Short stroke standard 3x4 and 4x4 keyboard configurations. Choice of ½ inch or ¾ inch button centers and post or flange mounting. Standard coded outputs—easily interfaces with logic circuitry. Excellent audible and tactile feedback.



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CIRCLE 62

PAIRED PROCESSORS BOOST MICRO'S PERFORMANCE

A dual-processing micro achieves a true division of labor by allocating tasks to each CPU according to its means.

by Barry James Folsom, Robert S. McNamara, and Mark Sheffield

Personal computers and application software packages introduced in recent years have offered progressively greater power and more functions. At the same time, business users have come to expect more capability, performance, and variety in their application programs. They also expect their machines to keep up with future needs and not become obsolete as new hardware and software products are developed.

Currently, the personal computer industry is in a state of transition from 8- to 16-bit word length. Software packages written for 16-bit computers offer more functions and faster response than equivalent applications on 8-bit machines at essentially no additional cost. Both 8- and 16-bit computers are being marketed by a number of manufacturers. Because 8-bit personal computers have been applied in the office since the mid-1970s, there are many 8-bit application packages available to the user—including a choice of at least several packages for the more popular applications. Presently, few 16-bit packages are commercially available, but it is safe to say that they will overtake the current 8-bit offerings in only a few years.

Clearly, for the best possible utilization of their computing resources now and in the future, users will benefit by having both 8- and 16-bit capabilities. They will then be able to keep their 8-bit programs, replace some with 16-bit counterparts, and invest in new 16-bit applications.

Digital Equipment Corp's RAINBOW 100 runs both 8- and 16-bit industry-available application software. Because most of the intended users are not computer oriented, they should not have to know whether programs are written for 8- or 16-bit processors, but only that they are useful in their jobs. This computer recognizes either 8- or 16-bit software automatically.

System software

The largest library of 8-bit application programs is written for the CP/M™ – 80 operating system developed by Digital Research, Inc and runs on the Zilog Z80 microprocessor. Similarly, most 16-bit software being developed for personal computers is based on the CP/M-86 operating system running on the Intel 8086/8088 microprocessors. The 8088 combines the 16-bit instruction set of the 8086 with an 8-bit bus interface. The personal computer runs both 8- and 16-bit CP/M programs by including both the Z80 and 8088 microprocessors and, functionally at least, both the CP/M-80 and CP/M-86 operating systems.

CP/M-86/80, the RAINBOW 100 dual operating system, is a hybrid version of the CP/M-80 and CP/M-86 operating systems. When an application is specified by the user, the computer first determines whether it is an 8- or a 16-bit program and then links the appropriate CP/M-86/80 system software modules. This entire process is fast and entirely transparent; users need not mount a particular system diskette or enter special instructions at the keyboard. Other operating systems are available as well.

Hardware

A basic RAINBOW 100 consists of three components: a 12″ (30-cm) diagonal monochrome cathode ray tube (CRT) monitor, a keyboard, and a system box enclosing

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Robert S. McNamara is senior engineer at Digital Equipment Corp, responsible for RAINBOW 100 hardware design. Mr McNamara has a BSEE from the Univ of Michigan.

Mark Sheffield is senior engineering project leader for the RAINBOW 100 at Digital Equipment Corp. Mr Sheffield has a BSEE from Clarkson College and an MSEE from Northeastern University.

all system hardware, including random access memory (RAM), and mass storage and interface electronics for various options.

The CRT monitor has a standard display format of either 80 x 24 or 132 x 24, weighs only 15 lbs (6 kg) (with antiglare filter), and is 13.75″ (34.92 cm) wide x 11.5″ (29.2 cm) high x 12.25″ (31.11 cm) deep. It can be tilted to any viewing angle in a 30° range and includes a built-in handle to facilitate carrying. The microprocessor driven keyboard, which is 21″ (53 cm) wide x 6.75″ (15.87 cm) deep, has 103 keys in separate sections for a standard typewriter character array, numerical keypad, and cursor controls. The system box weighs just under 28 lb (12 kg) and is 19.25″ wide x 14.62″ deep x 6.5″ high (48.89 x 37.13 x 16.5 cm).

As might be expected in a product directed at the highly active personal computer market, the design constraints were severe. Production costs had to be low and printed circuit board space for integrated circuits limited. A single 10.4″ x 14″ (26.4- x 35-cm) system board had to contain central processing unit (CPU) hardware, basic RAM chips, read only memory (ROM) chips, video subsystem, and standard peripheral interfaces. The floppy disk controller module and three option modules were to be daughterboards mounted directly on the system board. Both cost and real estate constraints influenced the architecture, and resulted in departures from conventional computer design practice.

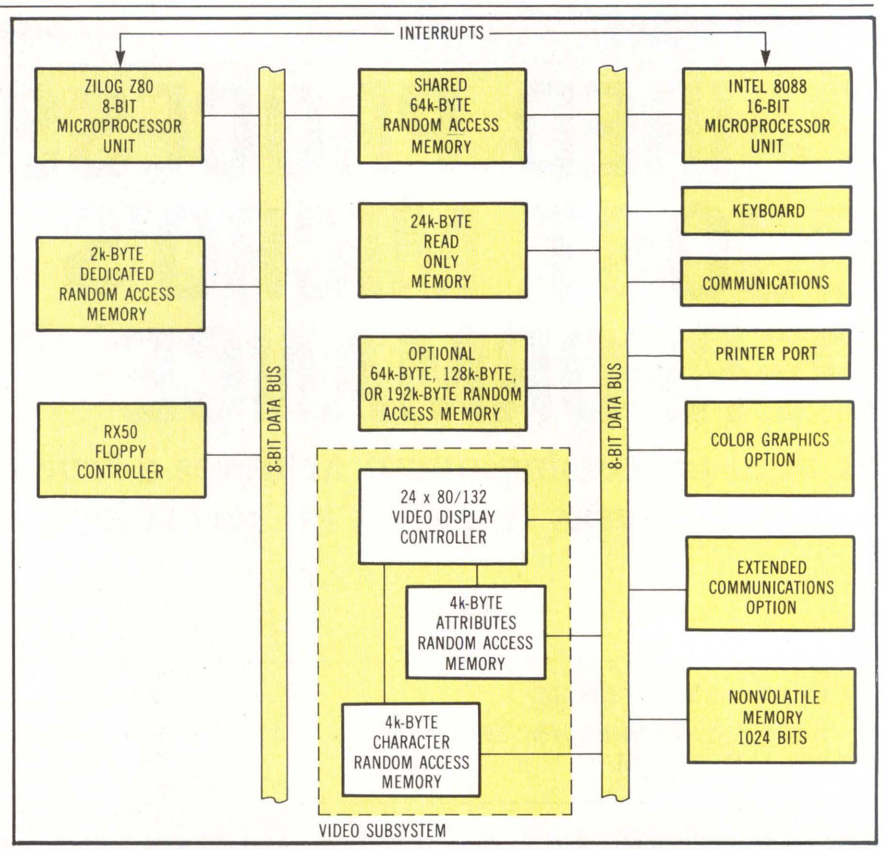


Fig 1 Dual-processor architecture. Each microprocessor unit employs dedicated and shared resources for more efficient use of hardware while maintaining software compatibility.

Dual-computer architecture

The dual-computer architecture shown in Fig 1 is, in concept, very simple. Each of the two CPUs has its own 8-bit bus, shares 62k bytes of RAM, and communicates with the other through an interrupt scheme. When either CPU is running an application program, it exchanges data directly with devices on its own 8-bit bus and indirectly with devices on the other 8-bit bus via a buffer "mailbox" in shared memory. Each CPU also functions as an intelligent controller for the devices on its own 8-bit bus. In doing so, it offloads input/output (I/O) tasks from the other CPU and hastens program execution time and system response.

Shared RAM provides a fast method of transferring data from CPU to CPU. Not only is the time for memory to memory transfers eliminated, but shared RAM saves the cost and board space of a second set of eight 64k-bit RAM packages.

The traffic cop for shared memory accesses is a state controller in the RAM arbitration logic. This controller is notified that either a CPU or direct memory access (DMA) device (via the extended communications option) wishes to read data out of or write data into shared memory. The controller either permits memory addressing and establishes the proper timing, or locks out the requested data transfer until ongoing activity in memory has been completed. Design of the state controller was more difficult in implementation than in concept because of the different clocks and execution times of the Z80 and 8088 CPUs.

On the Z80 side

Basic and optional peripheral devices are assigned to the two CPUs so as to optimize overall performance. Floppy storage, which consists of either one or two 800k-byte dual diskette units, is located on the Z80 bus. Therefore, the Z80 CPU alone has access to the floppy disk controller and is responsible for controlling floppy data transfers. This is done through programmed I/O to avoid the cost and board space of a DMA controller.

The Z80 CPU's floppy access service must be optimized by cutting out any unnecessary transfer time. For this reason, the Z80 is assigned 2k bytes of dedicated RAM (inaccessible to the 8088) for storing its interrupt vectors and any other software that affects floppy access timing. The time-critical floppy read/write routines are always executed from the Z80's dedicated RAM, eliminating the possibility of data overrun or lost data due to contention for the shared RAM. It is therefore extremely unlikely that a floppy disk data transfer will be interrupted. If the 8088 is currently processing an application, it has made the data transfer request itself and handles the peripheral devices on its bus. There are no peripherals other than the floppy controller on the Z80 bus to originate an interrupt.

Since the Z80 can only address a total of 64k bytes of memory, it can access only 62k bytes of shared RAM in addition to its 2k bytes of dedicated RAM. The remaining

2k bytes of shared RAM are therefore used for dedicated location of the 8088's interrupt vectors. In this way, the possibility of a conflict between Z80 and 8088 interrupt vectors is eliminated.

Data transfer time on the 8088 is minimized to provide high speed execution of 16-bit CP/M programs. Initial benchmark tests indicate that the 8088 CPU is capable of executing 16-bit programs at least as fast as equivalent 8088-only personal computers.

On the 8088 side

The 8088 processor makes use of several different types of memory:

- It includes 64k bytes of dynamic RAM (62k bytes shared with the Z80 CPU).
- 24k bytes of ROM contains bootstrap, diagnostics, and VT102 emulation firmware code for both the 8088 and Z80 CPUs. Digital Equipment Corp's full-function VT102 video display terminal is emulated in two modes: console and terminal. In console mode, RAINBOW emulates a VT102 in running programs locally as a standalone machine. In terminal mode, RAINBOW 100 appears as a VT102 terminal to a host computer connected to the communications port.
- Optional unshared dynamic memory includes additional 8088 RAM of 64k bytes or 192k bytes on an option module (daughterboard).
- Video Control RAM has separate 4k-byte RAM for character and attribute codes to be used by the 8088 CPU to control characters on the video display.
- 1024 bits of nonvolatile memory stores setup parameters that establish characteristics of keyboard, video display, and communication interfaces. System setup parameters are stored as part of hardware rather than relying on loading them in from floppy disks.

In addition to 24-line x 80- or 132-column displays, the video subsystem provides such VT102 features as full- and split-screen smooth scrolling; double-height and double-width lines; and reverse video, bold, blinking, and underlined characters. The video display processor accesses the 4k-byte blocks of character and attribute RAM a small portion of the time, in order to index the American National Standard Code for Information Interchange character codes into a character generator and apply attribute information to modify the video data. The memory mapped video screen RAM allows high speed data transfers to the user; this is especially important when editing or paging through a file.

Serial line interfaces are provided to the keyboard, communications port, and printer. The keyboard interface is an RS423 full-duplex connection running asynchronously at 4800 bits per second. Communications with other computers are through an RS423 asynchronous/byte synchronous interface. The general purpose printer port provides an RS423 interface to a variety of Digital Equipment Corp's printers.

The color graphics option provides the required bit-map memory array and additional video controller logic for use with the monochrome CRT monitor or optional color monitor. A high level command language is used to draw figures ranging from simple vectors to complex open and closed curves. There are two resolution modes for graphics: 800 x 240 picture elements with two planes and 320 x 240 picture elements with four planes. Four colors out of a 16-color palette are available in the high resolution mode, and up to 16 colors in the low resolution mode.

The extended communications option provides a high speed DMA serial line for a Winchester drive and a second (RS-232-C) communications port with asynchronous, and bit and byte synchronous capability. An RD50 Winchester disk drive unit provides an additional 5M bytes of mass storage.

Dual CP/M operating system

After power-up, diagnostics, and bootstrap, code in the 8088's ROM prepares the personal computer for processing an application. As shown in the memory map in Fig 2, the CP/M-86/80 operating system is loaded into its proper location in the 64k-byte RAM. Software modules in CP/M-86/80 fall into two groups: the CP/M-86/80 kernel and the CP/M-80 interface layer. The CP/M-86/80 kernel has essentially the same characteristics and functions as the CP/M-86 16-bit operating system for the 8088 CPU. The CP/M-80 interface layer appears to an 8-bit CP/M-80 application program to be a basic disk operating system (BDOS) and basic input/output system (BIOS) as defined by Digital Research for the CP/M-80 operating system.

When the user keys in the 8-character name for the selected application program, CP/M-86/80 searches for its file name on the floppy disks. The operating system is able to soft sense whether the file is a Z80 or an 8088 program because all the application programs are identified by either of two file extensions. They exist on disk as either filename .COM files for CP/M-80 programs or filename .CMD files for CP/M-86 programs (file extensions are customarily used for file organization purposes).

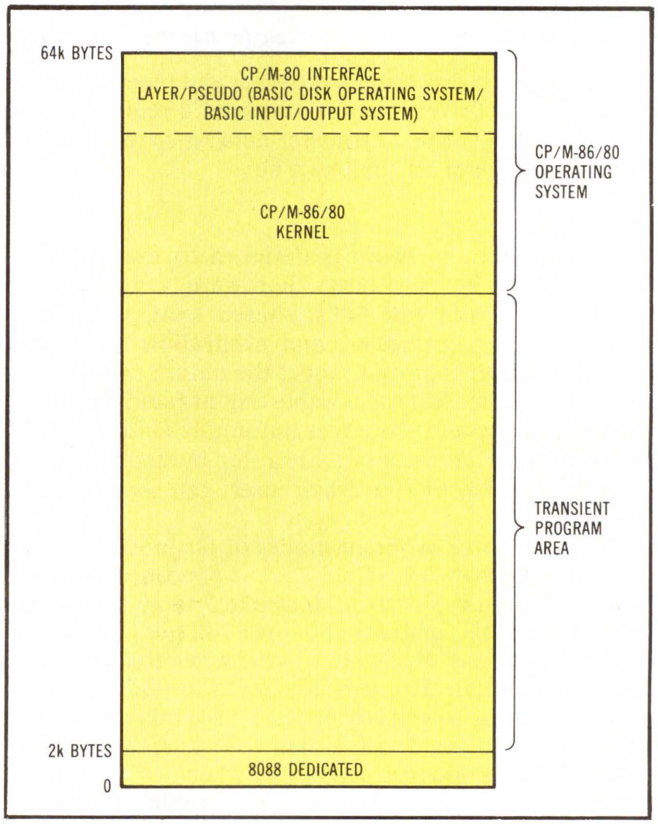


Fig 2 Shared RAM memory map. 62k-byte shared area provides space for the CP/M operating system as well as applications programs.

The selected application program is loaded into transient program area space in shared memory. If it is an 8088 program, it communicates with the CP/M-86/80 kernel in the usual way (as defined in Digital Research's CP/M-86 system guide). If it is a Z80 program, it makes operating system calls to the CP/M-80 interface layer (or pseudoBDOS/BIOS).

The Z80 executes CP/M-80 programs and the 8088 executes CP/M-86 programs, but the two processors do not have equal responsibility or authority. CP/M-86/80 actually runs on the 8088, so that the 8088 performs all operating system functions. Even when the Z80 is executing a program, the 8088 is handling such tasks as keyboard code, servicing communications, and video screen refresh.

The 8088 is always the master and Z80 the slave, even when the Z80 is logically the master in executing a CP/M-80 program. If a CP/M-80 program is to be run, the 8088 must set up the Z80 to begin execution at the right location. If the Z80 wants to communicate with a peripheral device or requires a service from CP/M-86/80, it makes a system call to the 8088. When an 8088 program is running, the Z80 is idle but ready (looping) as it waits for an 8088 request for floppy disk data transfer.

When the 8088 wishes to transfer a block of data to a floppy disk, for example, the following sequence occurs:

- 8088 transfers data to a buffer in shared RAM.
- 8088 interrupts Z80 and passes parameters (via shared RAM) that describe what is to be done and where the data is located in shared RAM.
- Z80 accesses data in shared RAM and transfers it to the indicated disk location.
- Z80 reports to the 8088 that the transfer has been completed.

When the Z80 is executing a program and requires access to the floppy drives, it must still send a request to the 8088, just as if it had to transfer data to or receive data from a peripheral on the 8088's bus.

Diagnostics

The diagnostics software is designed to test all functional units in the basic hardware configuration including Z80 and 8088 CPUs, shared RAM, video subsystem, floppy controller, and arbitration logic. The tests must determine and report the nature of the error and identify the field replaceable unit at fault. The diagnostics process must be either automatic (and transparent to the user) or must provide a step by step process in plain text that the average user can comfortably manage.

There are three different modes of diagnostics operation in RAINBOW 100. Cold-start diagnostics perform automatically on power-up and take 7 to 10 s. Though noticeable, this amount of time is not disturbing to the user. Reset diagnostics occur when the computer has been booted. The user initiates the reset function and thus begins reset diagnostics. These take about 2 s. This process is less detailed than cold-start diagnostics. Self-test diagnostics are performed when "S" is selected from the main system menu and take 1 min 15 s to execute. Tests of the basic system hardware, as well as optional RAM, are performed. Floppy drive related tests also occur. This test requires a formatted diskette in drive A. If a disk is also detected in drive B, tests will be run on drive B as well.

A diagnostic disk is also available that provides several types of tests via diagnostics menus. Typically, the user has tried reset diagnostics several times without success and now wants to determine whether the malfunction is in the application program or hardware. The diagnostic disk checks basic system elements, such as floppy disks and serial lines, more thoroughly and adds tests on optional RAM and graphics video controllers.

When the user boots the diagnostic diskette, the main diagnostics menu appears on the monitor screen. The user may decide to run a separate floppy test, which takes from 3 to 5 mins, for drives A and B. Or as the first step in the extended test sequence, which takes from 30 to 45 mins altogether. The floppy test checks a number of aspects of the drive: internal registers in floppy controller, timing of head stepping motor, track 0 switch, rotational speed of disk, operation of data separator in floppy controller, disk read and write, and capability for detecting header and cyclic redundancy check data errors.

The extended test sequence [second screen in extended test menu in Fig 3(a)] checks the floppies, shared RAM, and communications interfaces automatically. As each test segment is completed, acceptable operation is indicated by displaying "OK" on the screen at the end of the test line. Error messages, such as for the floppy data loopback failure in Fig 3(a), are displayed at the bottom of the screen. (Typing "L" requests repetitive internal

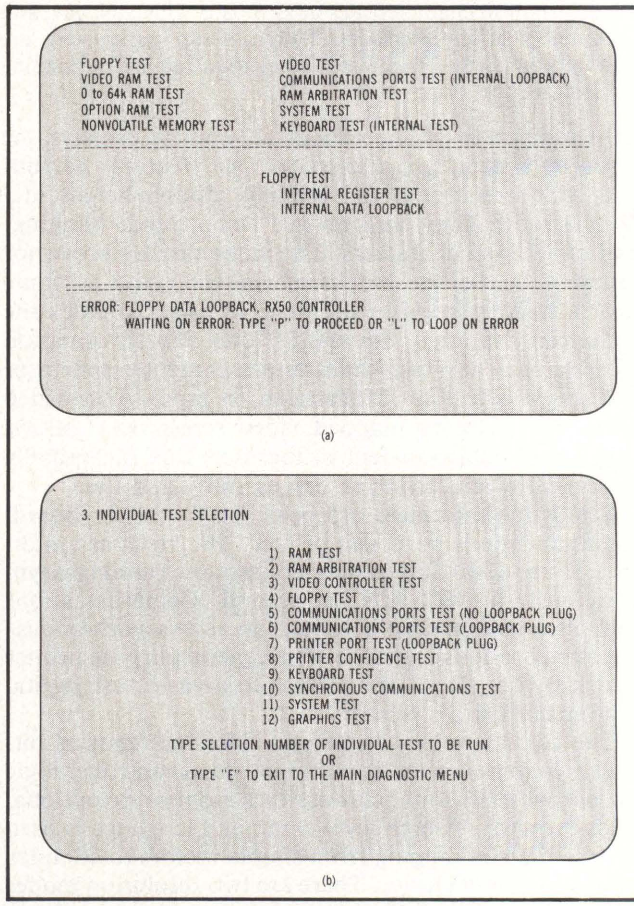
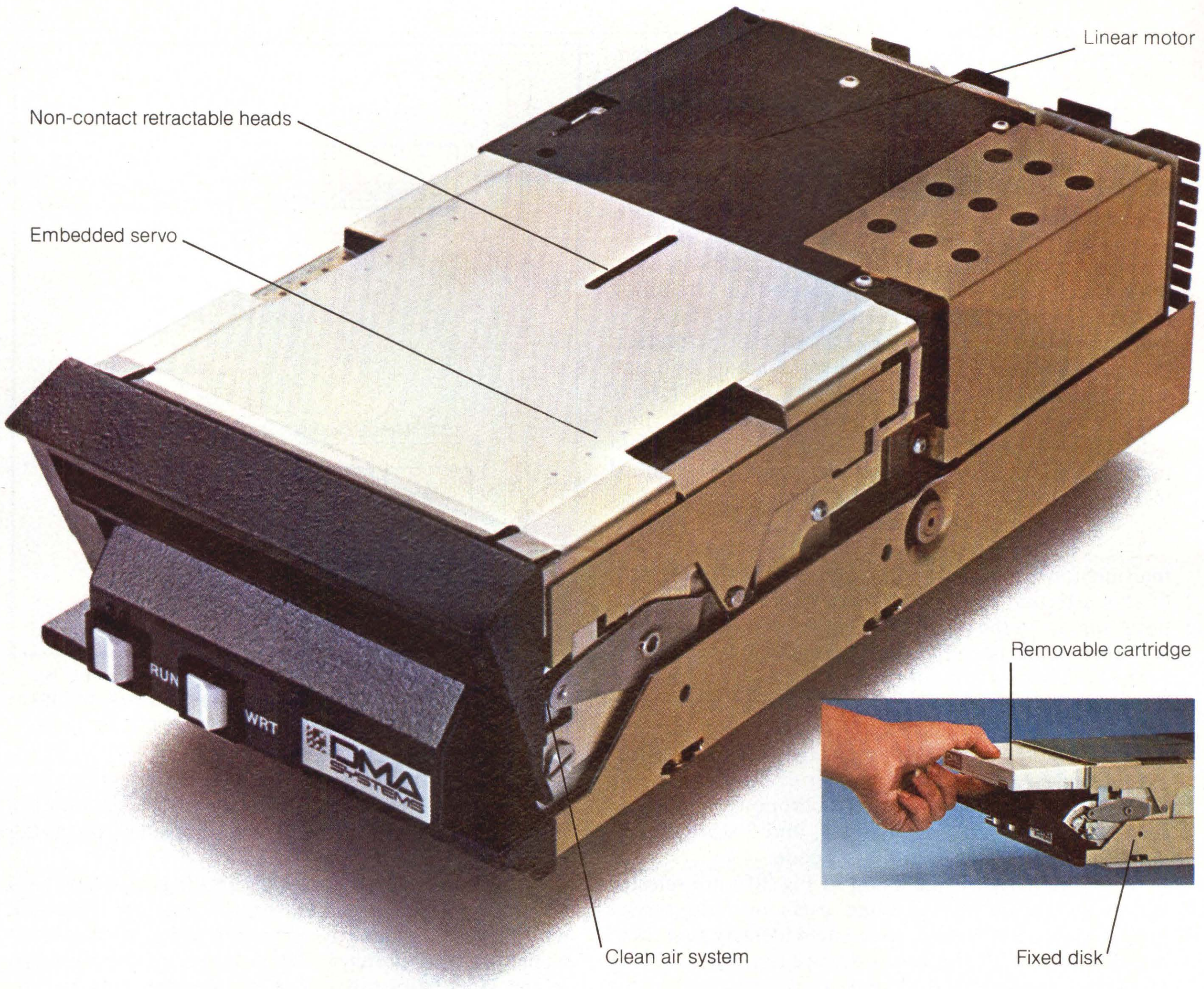


Fig 3 Extended diagnostics (a) are available on a diagnostic disk. If necessary, individual tests can be run separately from menu driven display (b).



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looping, which is followed by a display of the percentage of loops that failed. This test function, which is designed mainly for field service people, may indicate the need to replace a system component.)

RAM tests provided in the RAINBOW 100 diagnostic package include addressing to determine that the select logic for RAM chips is working properly, a gallop test that validates data timing by alternate reads of complementary data in quick succession; code execution that checks capability of processor in handling instructions and data transfers in tight loops by switching data rapidly between adjacent addresses; refresh that checks refresh logic by loading data and determining if still present after 3 s (refresh rate is once every 2 ms); and alpha contamination that determines whether alpha particles are destroying data in RAM storage. "Time to complete" on the extended test screen displays how much time remains for each test segment that lasts for over 1.5 mins.

The communications port tests determine if there is a malfunction and whether it is in the onboard interface or it is external, such as in a modem, in a communications line, or in the printer itself. Communications tests are much more thorough on the diagnostic diskette than in the cold-start procedure. In cold start, for example, the serial lines are tested only under the most common conditions: a data stream with 1 stop bit, no parity, and 7-bit code at 9600 bps. With the diagnostic diskette, the serial lines are checked at a number of baud rates from 50 to 9600 and in several synchronous and asynchronous message formats: 1, 1.5, and 2 stop bits; no parity and parity bit; 7- and 8-bit code.

Individual tests on the menu in Fig 3(b) are selected mainly by technically oriented users or field service people for loopback tests, which help identify sources of malfunctions. The printer confidence test prints a block of characters specified by the user.

If all individual tests have been run and a malfunction still exists, the user may select a system test. In this procedure, the computer is subjected to worst-case conditions—all possible devices on the two buses request access to the two CPUs at the same time—and tested as a system. If individual tests have already found all units acceptable, the malfunction is likely to be in the interaction between two units and the solution may be to replace the system board.

Loopback testing

Conventional computer diagnostic routines identify a malfunction as originating somewhere in a peripheral subsystem but cannot go further to identify the specific source. For example, a floppy disk subsystem would be pinpointed but would not indicate whether the problem is in the disk drive, floppy controller, or floppy data separator. Such a distinction is important so that the user can remove and replace the particular faulty unit.

An internal loopback arrangement, shown schematically for a floppy disk subsystem in Fig 4, provides a fast, convenient method of testing for malfunctions. By inserting a loopback multiplexer at the system connection to the floppy disk drive, a data stream is transmitted from the 8088 CPU to the floppy data separator as if it were coming right off the diskette drive itself. Any failure in this transmission may eliminate the floppy disk drive as the source of the problem. An error message

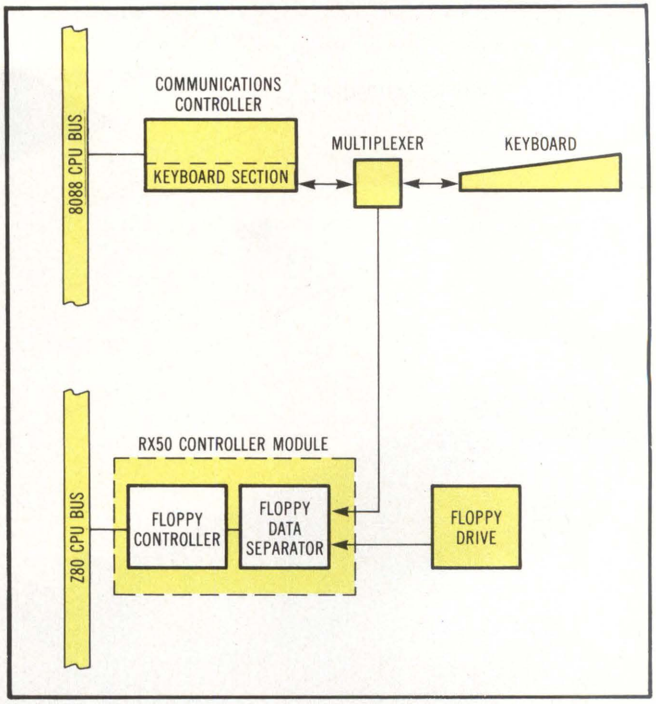

Fig 4 Internal loopback testing of system components is possible. Failures may be pinpointed beyond peripheral level to system components. Here floppy controller, data separator, and system board are checked.

on the CRT monitor indicates whether the malfunction is on the floppy daughterboard, which contains the floppy data separator and floppy controller, or on the system board.

The loopback procedure for checking RAINBOW 100's video subsystem is similar except that the loopback multiplexer is placed between the video display controller and CRT monitor. The 8088 sets up a test pattern in the video subsystem. The serial video data is then looped back into the printer universal synchronous/asynchronous receiver/transmitter converted to parallel form, and transferred to RAM by the 8088. Finally, a checksum is calculated to verify the data.

The loopback arrangement supports testing in cold start, reset, and self-test diagnostics. The user can then handle a significantly greater proportion of malfunctions by replacing units, rather than by calling on Digital Equipment Corp's field service staff.

The design approach taken in the RAINBOW 100 personal computer integrates hardware and system software closely and allows the Z80 and 8088 CPUs to run side by side. Hardware integration, which helps reduce cost and board space, is achieved by avoiding duplicate functions and designing the system architecture so that the two processors complement each other. In addition to executing its own programs, each processor performs system tasks that contribute to optimum program execution by the other processor.

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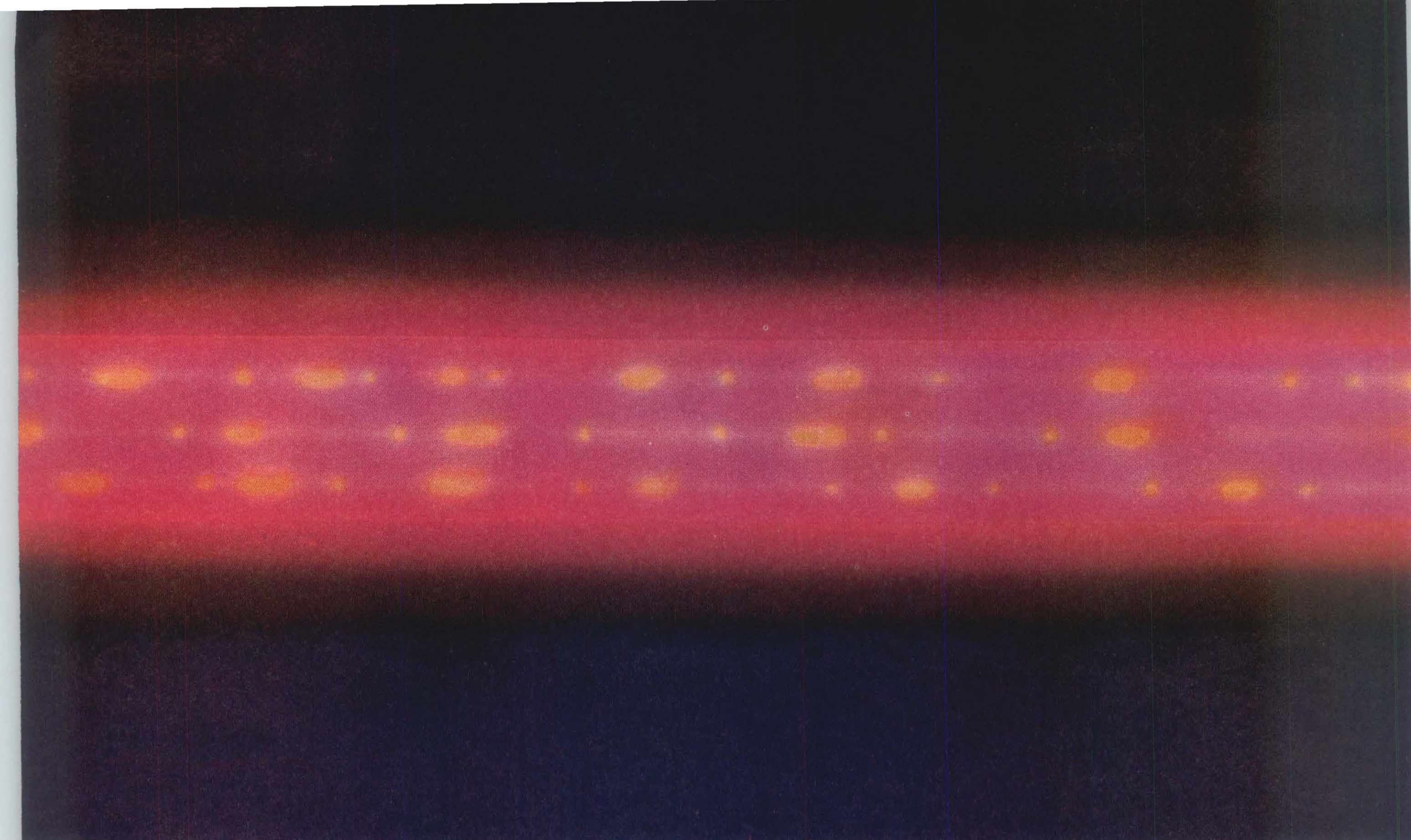

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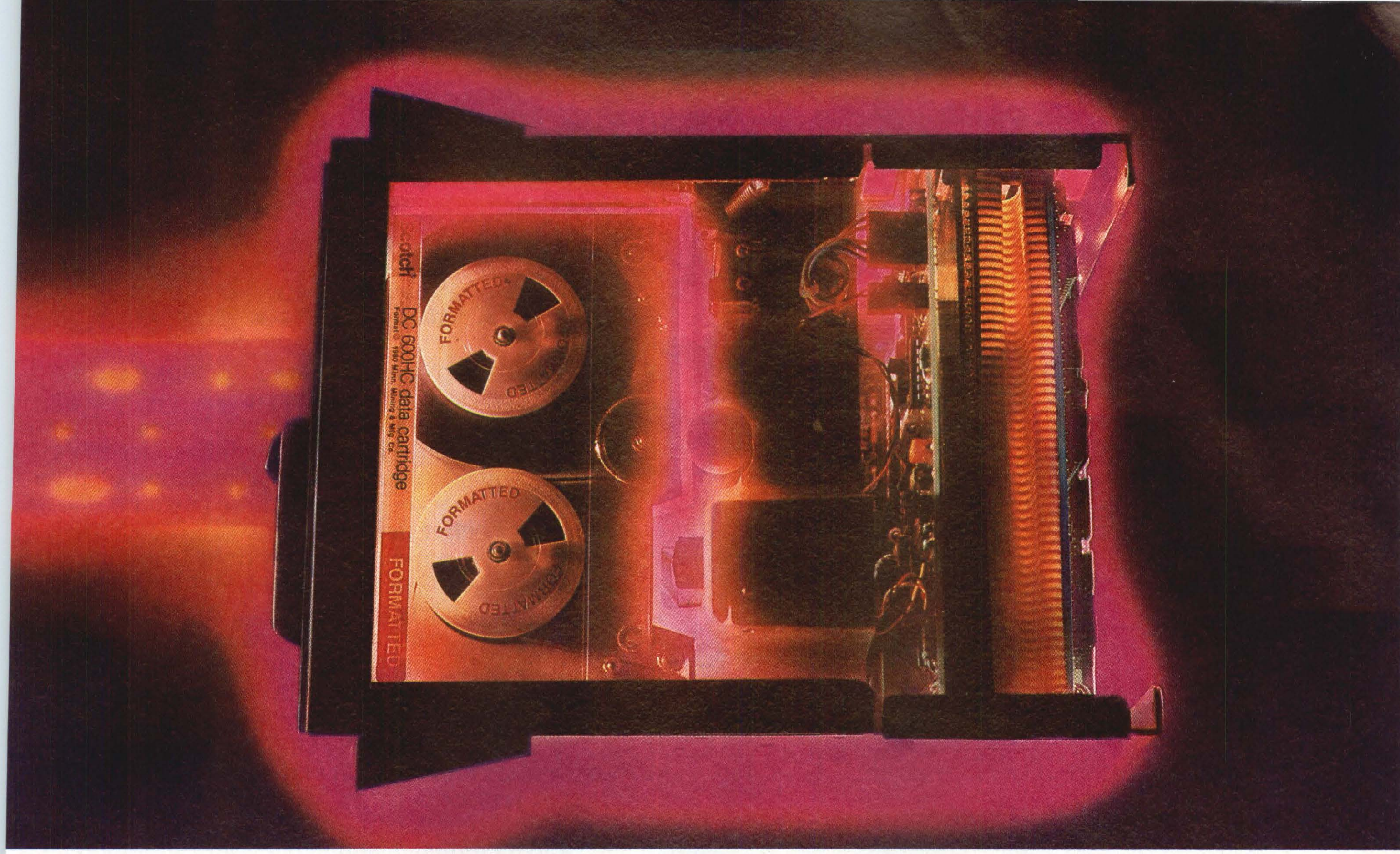
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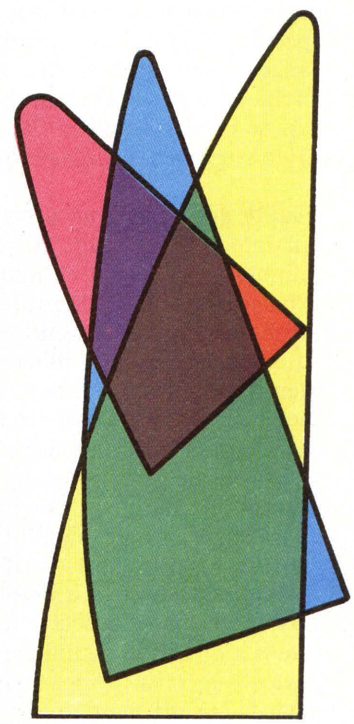

by Ross E. Roberts and Dick Gossen

In this very large scale integration era, parts destined to become major components of complex systems must be made as reliable as possible. From the time a new-generation memory chip is first cast in silicon until it becomes an established component of a computer manufacturer's equipment, the device is analyzed, probed, baked, shaken, immersed, and stressed in order to identify which manufacturers' parts are best qualified for use. From both the manufacturer's and the buyer's standpoints, online testing is invaluable in helping chip producers increase both *in situ* performance and production yields, leading to even more dependable devices at lower cost.

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Dynamic random access memory (DRAM) chips constitute the most commonly used group of components in today's minicomputers. As a result, to successfully vend such a part requires the chip maker to produce devices that are consistent with the customer's specification. On the other hand, the computer original equipment manufacturer (OEM) must select vendors by carefully evaluating the semiconductor manufacturer's assets, including advanced fabrication technology and the ability to deliver large quantities of quality parts on schedule. In addition to considering vendor selection, memory system designers must accommodate their architectures, timing, circuitry, and layouts to the probable distributions of production parts from a principal vendor and anticipated alternate sources. For example, system adjustments can result in loosened timing specifications on the DRAM chip. Faster operating parts are usually more expensive and less common than those that offer basic performance.

At the outset, when a company attempts to find a potential memory device vendor, its attitude is necessarily very critical. Its initial task is to uncover intrinsic flaws in the chip producer's design, processing method, or testing program. However, once a vendor is selected, a symbiotic relationship develops between the parties:

because both vendor and customer can now benefit from the end product's success, establishing mutual confidence becomes critical.

Any test program, no matter how comprehensive, is only as reliable as the data it generates.

Since it requires extensive and time-consuming engineering to integrate 64k-DRAM chips into minicomputer systems, a user is wise to enter the design/decision loop as early as possible. Chip manufacturers such as Texas Instruments (TI) often welcome users' early inputs, since they can help direct the designers toward design and processing solutions. For example, potential problems with power supply bumping and input undershoots were among the considerations that led TI to select the highly successful, epitaxial processing technology for 64k devices.

Customers can enter the evaluation programs as soon as the earliest prototypes are available. Although these early prototypes need not meet all the OEM's target specifications such as temperature, voltage, and humidity ranges, they must be operational and suited for basic engineering tests. During this trial phase, when changes can be implemented easily and inexpensively, users can often suggest desirable modifications to the chip maker.

Quality and performance testing

All integrated circuits (ICs) earmarked for the highly reliable performance computer systems demand must be extensively tested. Manufacturers perform electrical, mechanical, and hermetic seal tests, as well as reliability studies to verify the failure rate, and screening tests to identify potential failures. Users' incoming inspections include both visual and electrical checks. In many cases, users first subject a sample of devices to the identical test program performed by manufacturers; then, comparing their data with the manufacturers', verify device characteristics and reliability.

Since it is difficult to verify device failure rates, quality assurance testing of a highly reliable memory device is now a primary aspect of IC procurement. A failure rate is a quantitative indication of the probability of the device's survival; exact failure rates for highly reliable devices are difficult to verify because many test hours must be logged before the number of failures becomes statistically significant. Hence, failure rates for highly reliable devices are largely unavailable.

Users and manufacturers that require highly reliable devices generally turn to intensive quality assurance testing. Typically, this involves a combination of screening procedures; 100% testing; and acceptance (sampling) tests, including visual inspection and physical, environmental, electrical, and life tests. In addition, a 64k DRAM requires a wide variety of "pattern tests" to determine if an individual memory cell retains correct data while the data in surrounding cells are changing.

A computer manufacturer ideally wants the semiconductor manufacturer to perform most of the quality tests. Computer houses are more concerned with a random access memory's (RAM) system performance—ie, how many of the devices work together while executing the computer system operations. The chip manufacturer, on the other hand, is more concerned with individual performance and single device specifications.

TI's test program begins at a level called Multiprobe (Fig 1), the first stage at which silicon slices are tested for functionality. Multiprobe is a 3-stage procedure consisting of three sequential tests. The first eliminates nonfunctional chips which, if assembled, would not meet the requirements of the final test. The second test provides process engineering with the actual metal oxide semiconductor (MOS) parameters, which are a fabrication process function. Onchip test sites are provided only when they are relevant to the devices used in the memory periphery and array. These test sites include transistors, capacitors, continuity, and leakage structures. The final test provides minimum and maximum

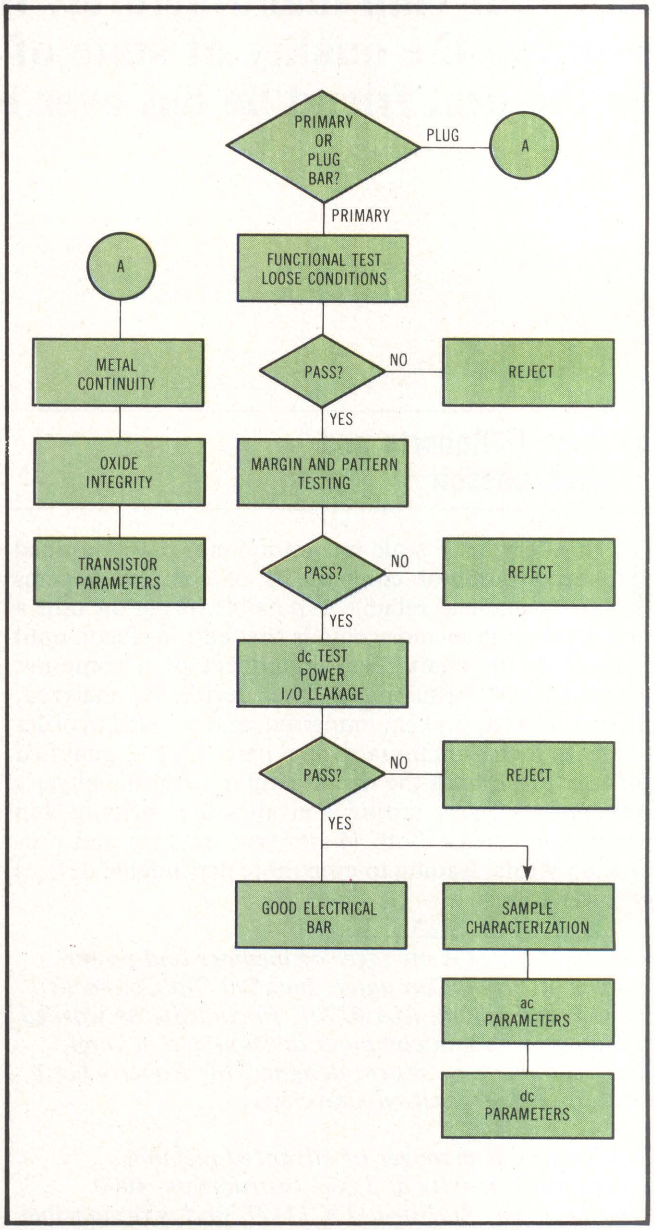
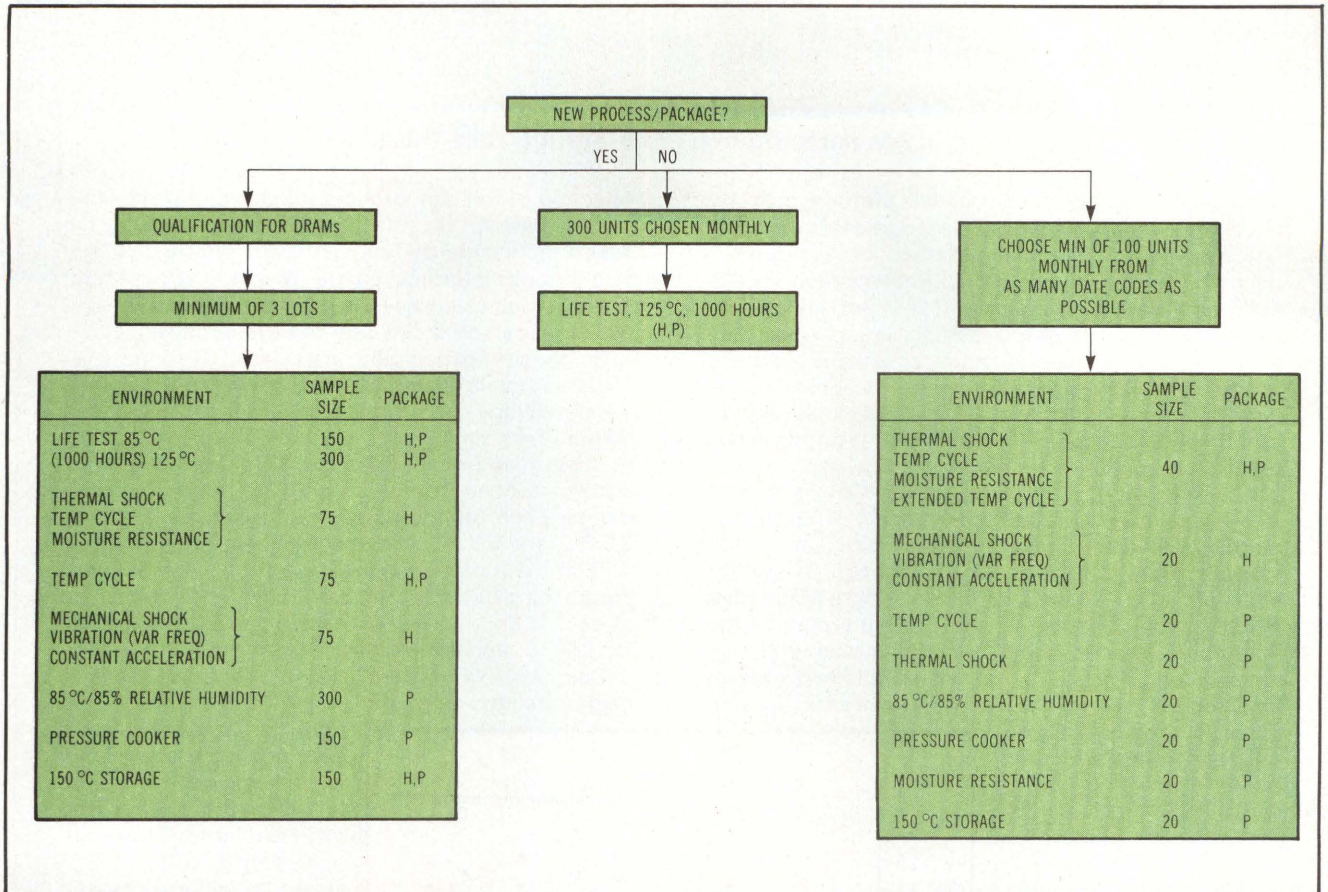


Fig 1 Block diagram of Multiprobe test program. Multiprobe begins testing chips before assembled for functionality, MOS parameters, and minimum and maximum dc parameters. "Primary" indicates 64k circuits, "plug" indicates test structures, and "bar" indicates a die.



ENVIRONMENT	SAMPLE SIZE	PACKAGE
LIFE TEST 85 °C (1000 HOURS)	150	H,P
LIFE TEST 125 °C (1000 HOURS)	300	H,P
THERMAL SHOCK / TEMP CYCLE / MOISTURE RESISTANCE	75	H
TEMP CYCLE	75	H,P
MECHANICAL SHOCK / VIBRATION (VAR FREQ) / CONSTANT ACCELERATION	75	H
85 °C/85% RELATIVE HUMIDITY	300	P
PRESSURE COOKER	150	P
150 °C STORAGE	150	H,P

ENVIRONMENT	SAMPLE SIZE	PACKAGE
THERMAL SHOCK / TEMP CYCLE / MOISTURE RESISTANCE / EXTENDED TEMP CYCLE	40	H,P
MECHANICAL SHOCK / VIBRATION (VAR FREQ) / CONSTANT ACCELERATION	20	H
TEMP CYCLE	20	P
THERMAL SHOCK	20	P
85 °C/85% RELATIVE HUMIDITY	20	P
PRESSURE COOKER	20	P
MOISTURE RESISTANCE	20	P
150 °C STORAGE	20	P

Fig 2 TI's qualification program for 64k DRAMs. Devices are chosen at random. Numbers represent sample size per lot. "H" indicates hermetic package, "P" indicates plastic package.

operating parameters of the memory device. Typically, these characterizations are performed on a sample basis so that process and product engineering departments receive immediate feedback.

If a DRAM successfully passes the three levels of Multiprobe, it is packaged and run through a series of assembly tests that consists of checks for solderability, 100% gross/fine leak, and a visual/mechanical inspection. Only devices that complete this test sequence proceed to the final phase, where pre-burn-in, post-burn-in, and quality assurance lot acceptance procedures are performed.

Currently, TI performs 85 °C dynamic testing on DRAMs; in order to learn more about device failure mechanisms, the company is considering a program based on dynamic testing at 125 °C. This program would burn in devices up to 160 hours, then dynamically test all critical timing parameters. A dynamic test program to be run at 150 °C is being planned.

Fig 2 illustrates the tests and numbers of devices used in the qualification program. All sample population units are randomly selected and electrically tested at the conclusion of the 1000-hour life test. Currently, 40 devices are checked in the thermal shock, temperature cycle, and mechanical shock test sequences; when plastic packaged DRAMs come on line, the sample population will increase to 200 devices. Similarly, the pressure cooker tests, now run with 20 chips, will increase to lot sizes of 200 for qualification. Monthly monitoring tests on 1000-hour life test devices have recently been increased from 200 to 300 devices.

All DRAMs in the qualification program are tested for continuity; input/output (I/O) leakage current; and operating, refresh, and standby current levels. Moreover, each device must be tested for functionality with rigorous pattern programs that test the memory array at the worst-case occurrences of data storage. Examples of this type of testing include the checkerboard pattern; walking one and zero; sliding diagonal, horizontal, and vertical stripes; and gray code. All patterns are applied to 100% of the memory array under various voltage and timing conditions.

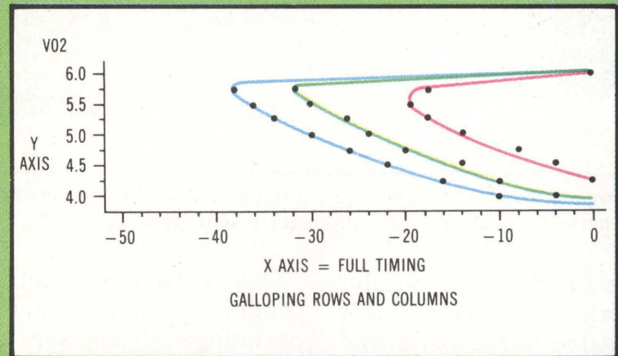
One of the best ways to combine test patterns with voltage and temperature variations is the so-called "Shmoo plot" method. (See the Panel.) This technique allows engineers to apply any type of test pattern to a memory device, while changing both supply voltage and temperature. This establishes a region of operation in which the chip not only handles data correctly, but does so under varying voltage and temperature conditions.

Any test program, no matter how comprehensive, is only as reliable as the data it generates. To assure that data are accurate, TI has established an auxiliary quality control procedure for the TMS4164 program test equipment. This test consists of a set of diagnostic routines, in addition to the normal maintenance of the test equipment, unique to the 4164 program. To prevent address skew and to enhance compare-strobe integrity, the diagnostic routines include a test for maximum edge accuracy on all timing signals. In addition, driver voltages are checked for precise V_{IH} and V_{IL} levels, power supply levels are checked for accuracy, temperature

DRAM performance—the Shmoo tells the tale*

To assure that a 64k DRAM will perform properly under the variety of possible conditions in system operation is the primary objective of a computer manufacturer such as Prime. Recent advances in automated test equipment and test software allow the OEMs to test an entire memory board while they vary critical parameters such as supply voltage, timing, temperature, and test patterns applied to the RAMs. The test results, called "Shmoo plots," establish the operating region in which device performance meets computer system requirements.

Although DRAM manufacturers such as TI emphasize specifications and performance of individual memory devices, Prime's testing aims at understanding how groups of DRAMs function as system elements in specific applications. Using a Macrodata MD207/11 memory board tester, Prime programs the instrument to generate the voltage vs timing Shmoo plots. Each plot represents a different test pattern imposed on the RAMs. A family of plots can be produced from tests performed on a simple memory array board containing 78 of TI's 64k x 1 DRAM chips, operating in parallel but with neither internal timing generation nor error detection and correction logic.



To determine the operating region of individual DRAMs, relative to the operating region of the entire memory board, requires defining two sets of timing parameters: the absolute minimum timing of the DRAM chips specified by the semiconductor manufacturer, and the minimum memory board timing specified by the system designer.

The Macrodata board tester's compatible Shmoo program gives designers the ability to select the axis size, the minimum and incremental variable values, and the desired test pattern, and allows them to define timing parameter values. Minimum timing of the DRAM chips is defined as the 0% point, while the minimum memory board timing is defined as the 100% point. Between these extremes, a designer can expand or compress the board timing relative to the points from −99% to 99% by the proper selection of the plot size and the minimum and incremental values. On the plot illustrated below, the Y-axis represents the voltage to the DRAMs only, not to the logic interface on the memory array board. Y-axis range, as well as the minimum and incremental voltages, can be defined by the system designer.

Composite Shmoo plots are created using TI's 4164 chips and have 9 vertical and 26 horizontal points. Y-axis voltage runs from 4 to 6 V in 0.25-V increments. Two timing sets are defined for the X-axis: the first goes from −50% to 0% in 2% increments, and the second from −25% to 100% in 5% increments. Each Shmoo runs at temperatures of 0 °C, 25 °C, and 60 °C, and each temperature run uses 6 different test patterns, yielding a total of 36 different plots. The plot curves indicate the pass/fail threshold at each different temperature: blue for 0 °C, green for 25 °C, and red for 60 °C.

One possible pattern, called the Scan pattern, begins its test by complementing the current contents of the data register and writing resulting data into all memory locations between the lowest and highest addresses in ascending order. The entire test is repeated under extreme timing variations.

Another test, the March pattern, is performed twice, and the pass execution time is 232 ms at 0% timing and 285 ms at 100% timing. Floating ones and Floating zeros are two separate tests that are complements of one another. For both tests, pass execution time is 878 ms at 0% timing and 1061 ms at 100% timing.

Prime also uses the Galloping Rows and Columns shown in the Figure, and the Gallop test patterns. These patterns also begin with background data written into the memory and a test bit circulated through memory.

*The test patterns described here are provided by Macrodata's test patterns library. The parameters described are characteristic of Prime's test sequence and do not necessarily apply to other applications.

levels of IC handlers are checked, and a test is performed to assure test handler continuity (ie, low contact resistance and low leakage). These diagnostic routines are performed before each quality assurance lot acceptance procedure and each production shift.

Raw diagnostic data from all chip production line test sites are transmitted to a central computer system for analysis. A minicomputer links the test system central computer to online I/O devices so that input data and test results can be accessed quickly. Software, called test data management (TDM), manipulates and extracts test results via its statistical analysis processes and its editing capabilities. The TDM package creates a data base of processing history and displays data graphically, simplifying their interpretation as well as the day to day monitoring of chips, slices, and test lots.

TI has begun coordinating its 64k-DRAM test effort on a worldwide basis. Ultimately, the system will receive, process, and transmit test data and their results to and from the company's manufacturing facilities throughout the world. The coordinated universal test system will provide continuous process control information. It will also provide the customer's design engineers with crucial test results.

Before Prime Computer can qualify any manufacturer's 64k DRAM for possible inclusion in its computer systems, engineers from the memory department must ascertain that chip's most sensitive characteristics. Chip operation parameters affected by variations in such system level values as power supply and signal voltage levels, ambient temperature, and data patterns are determined. These engineers, aided by memory system designers, attempt to induce failures and/or errors by operating the devices to their limits as defined by the manufacturers' specifications (specs). In addition, devices are typically tested well beyond the specified limit in order to determine the degree of safety margin built into the device.

Initial tests are performed on single devices in a test socket. However, single-device test socket procedures produce a level of performance not often achieved in system operation. Thus, it is wise to test memory devices in more realistic, harsher environments, in order to practically assess their in-system capabilities.

After test socket evaluation, DRAMs are placed in an appropriate system environment that subjects them to a battery of internally designed tests. The test program is unique and, in most cases, does not duplicate the chip maker's tests. At the same time, the proposed DRAM should be placed into the manufacturing flow to obtain feedback on potential production problems. At this point in the evaluation phase, Prime, and usually the chip manufacturer, have not yet defined the chip's final specs.

One of the principal objectives is to evaluate memory devices from as many different vendors as possible. By relaxing initial engineering specs, memory system designers can accept devices from any manufacturer willing to submit rough cut devices for testing. Further, the actual receipt of chips—albeit preliminary versions—provides a good indication of both the companies actively seeking to participate in the market and their development programs' status. When the time comes to purchase chips in volume, the company can use this information to gauge the progress of the primary producers of the device in question.

Chip makers can cause great problems for computer manufacturers when they fail to deliver ICs in sufficient quantities. To prevent production shutdowns, Prime has a fallback position for such emergencies. For example, current memory boards using 16k DRAMs were designed to be upgradable when 64k devices became available. With a few cuts and jumpers, the board can accommodate the 64k chip. In fact, this board can run with one of several DRAM chip types: a 3-supply 16k; a single-supply 16k; or a 64k device. Unless all three DRAM types suddenly become unavailable, memory board production will continue.

Besides production continuity insurance, the fallback position precludes parallel engineering efforts. That is, Prime ensures that equipment production based on standardized devices overlaps with production based on the next generation of chips. This allows the company to supply a range of memory devices. Moreover, if engineering is dissatisfied with a new piece of memory hardware, industry standard alternative hardware can still be delivered to customers on schedule, while the technical bugs are worked out of the new generation of equipment.

The complete qualification process for a 64k DRAM takes time and effort and requires close customer/vendor cooperation. The qualification program begins in the memory engineering group.

Charting the qualification program's flow

As the Fig 3 flow chart shows, the procedure to qualify the 64k DRAM begins when the engineering group's need for a new memory component can be met by proposed semiconductor industry developments. Potential vendors are surveyed and inquiries sent out for preliminary specs in order to obtain a rough target spec from the manufacturer that includes supply voltages, package size and type, and special features.

After consulting with the internal engineering groups to determine their desired specs, sample chips are procured as soon as possible. Receipt of samples initiates parallel efforts in the engineering groups—one team begins testing the DRAM as a component, while a second establishes a product environment for the device. The inproduct testing effort reflects the emphasis on evaluating the device in a system application. If there is no appropriate product environment, a suitable real-world application is emulated.

If problems develop in either device or product testing, engineers inform the manufacturer and provide the information and assistance necessary to duplicate the problem. This is a critical point in the program, since the chip manufacturer must either resolve the problem or risk rejection until satisfactory devices can be produced. If events progress smoothly, a composite spec is generated for the DRAM against which more samples are repeatedly tested. These tests are not as extensive as those in the earlier program, since the chip's basic performance has already been established. The goal at this point is to verify the composite spec. At this time, the DRAM is not yet an approved part, but the composite spec allows purchasing to begin its preproduction procurement.

The second phase of qualification testing begins at receipt of the preproduction DRAM samples (Fig 4). Whether to test inhouse or at an outside test facility should be decided. Although the decision depends on the available test capability, the tests are usually performed inhouse for closer control and more comprehensive procedures.

DRAM samples are again tested, first as individual chips, then in product environments. Manufacturing engineers perform the tests that are, in many cases, more rigorous than those performed in design engineering. At the device level, testing is fairly routine and intended to uncover major inconsistencies in operation. At the product testing level, however, procedures uncover subtle problems associated with total system operation. When the manufacturing engineers are satisfied with the testing, all test procedures are reviewed and modified, if necessary. If any unusual problems are uncovered, the device is returned to engineering and goes through its test program again. (See shaded area of Fig 3.) Once manufacturing is certain the chip operates correctly in the system environment, the device is added to the company's approved product list. Production procurement teams can now open negotiations to purchase the device in production quantities.

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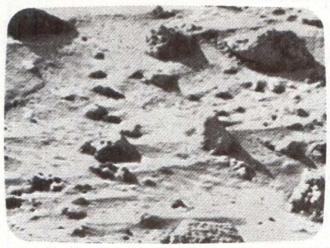

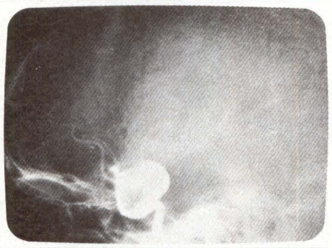

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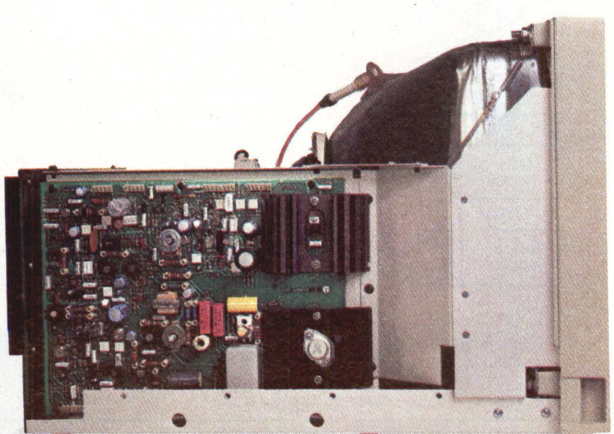

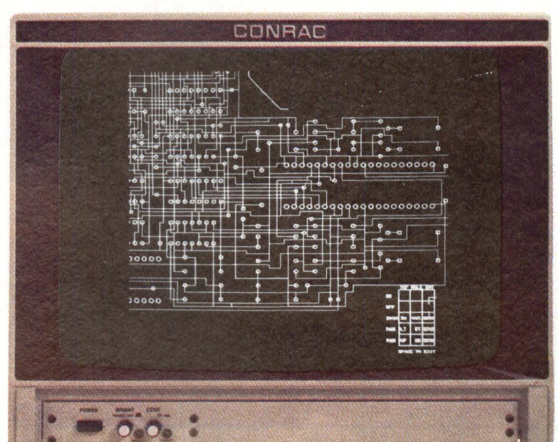

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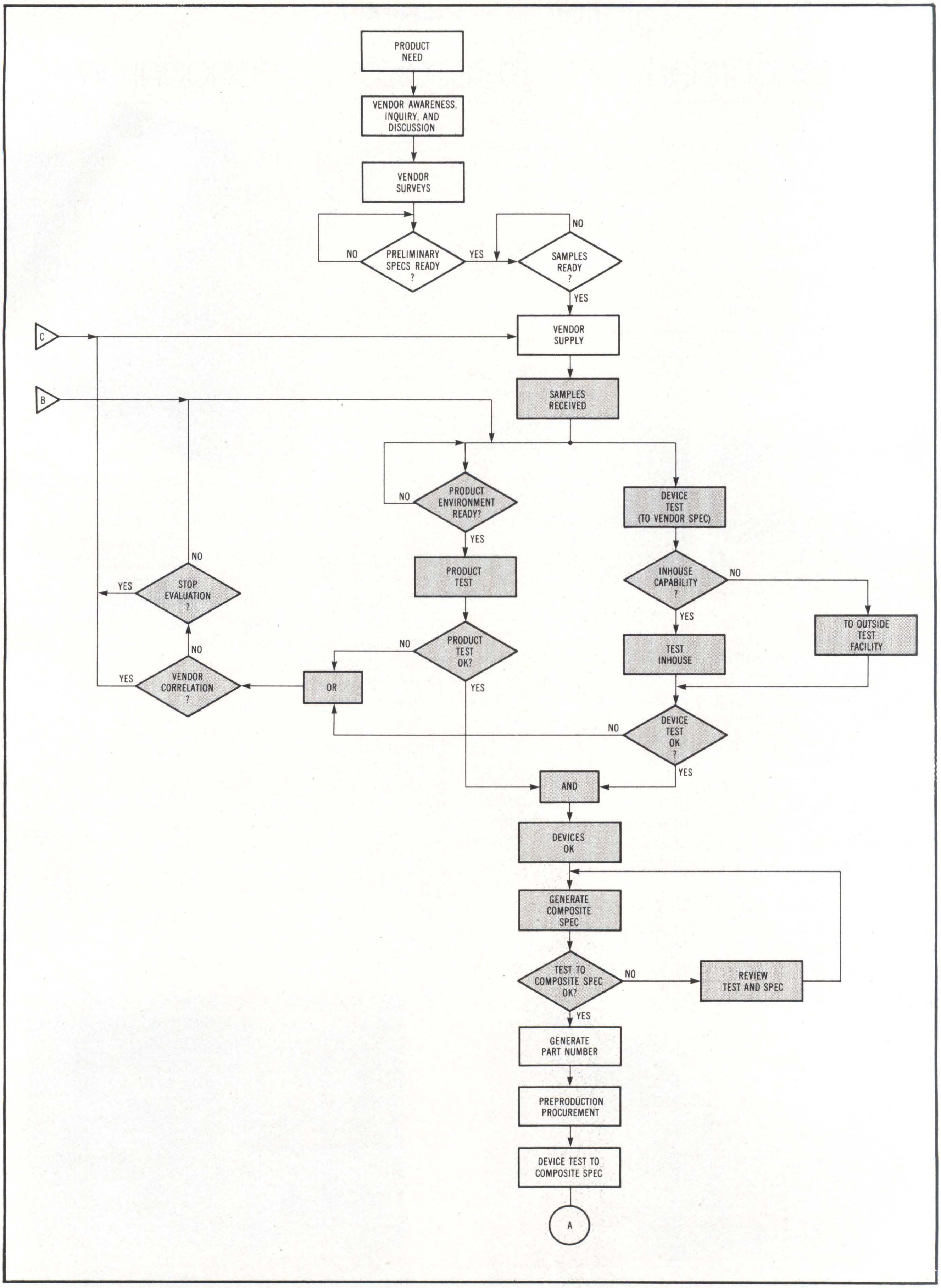

Fig 3 Prime's engineering qualification of 64k DRAMs. Program runs parallel tests on chips, both as individual devices and in product environment.

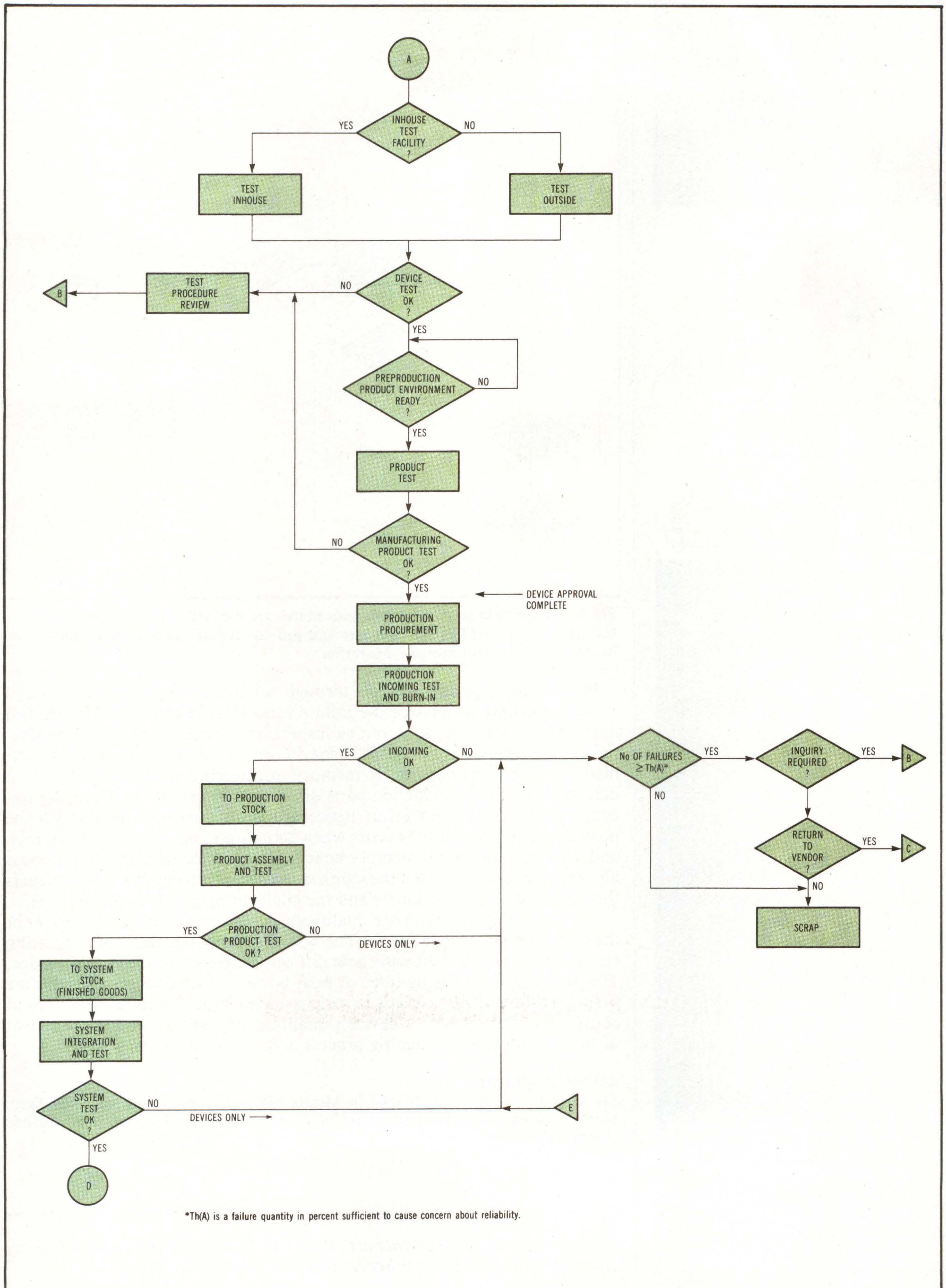

Fig 4 Prime's manufacturing qualification of 64k DRAMs. Here, more rigorous tests are run on the same devices, both individually and in product environment, before production procurement is approved.

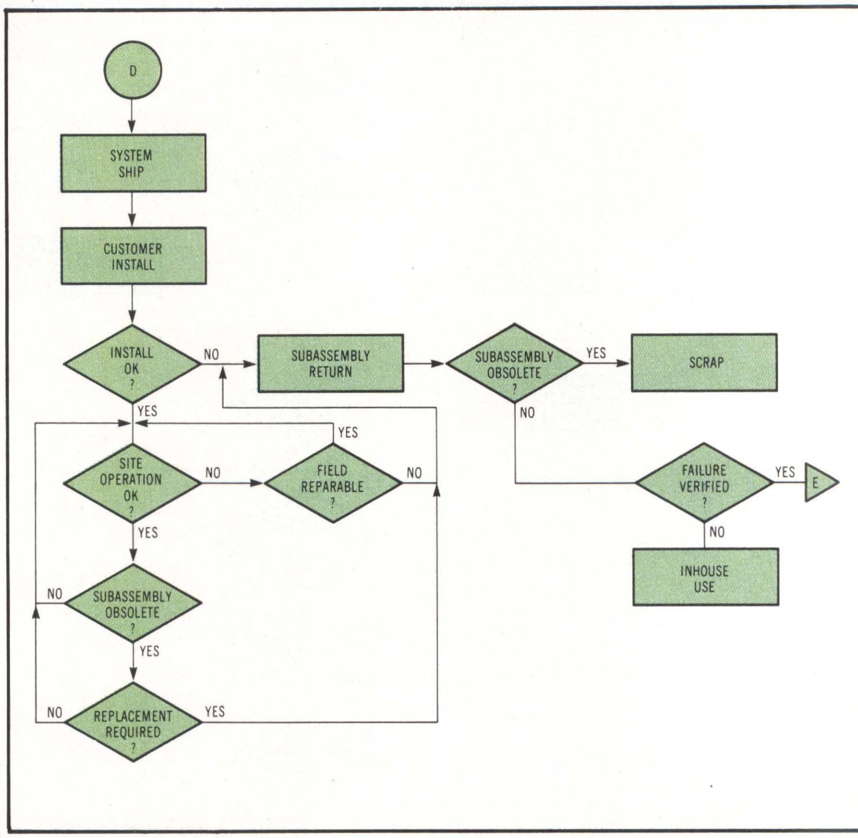

Fig 5 Prime field service systems procedures are a continuation of manufacturing qualification program and provide further data on new chips based on actual customer site operation.

Production versions are run through an incoming test program, and statistical programs analyze the failure rate. If more than a predetermined number of devices fail at incoming inspection, Prime informs the manufacturer. In some cases, the DRAM may need to be returned to either the manufacturing engineering or memory engineering groups for testing to determine whether production parts differ from those run in the earlier test programs. Often a joint effort between manufacturer and user solves the problem. The "acid test" occurs when DRAMs are sent to production stock and inserted into system memory boards intended for sale. If the chips pass all system integration tests, they are assumed to be acceptable. The system is then shipped to the customer, and the engineering group's role declines.

A critical phase of ultimate qualification starts when a system arrives at the customer's site. (See Fig 5.) The system is now in its ultimate operating environment; failures here can cause difficult problems for the system vendor. The key statistic is the number of boards/devices that fail in a given time period. If the number exceeds a predetermined limit, it may be necessary to consult the chip vendor. A device's qualification does not end at the arrival of the system; it is an ongoing process even at the customer's site.

Acknowledgments

Mr Roberts expresses his thanks to Messrs Michael Coomey, Ronald Remillard, Stephen Albino, and Richard Stone of Prime Computer, Inc, for their aid and critical comments.

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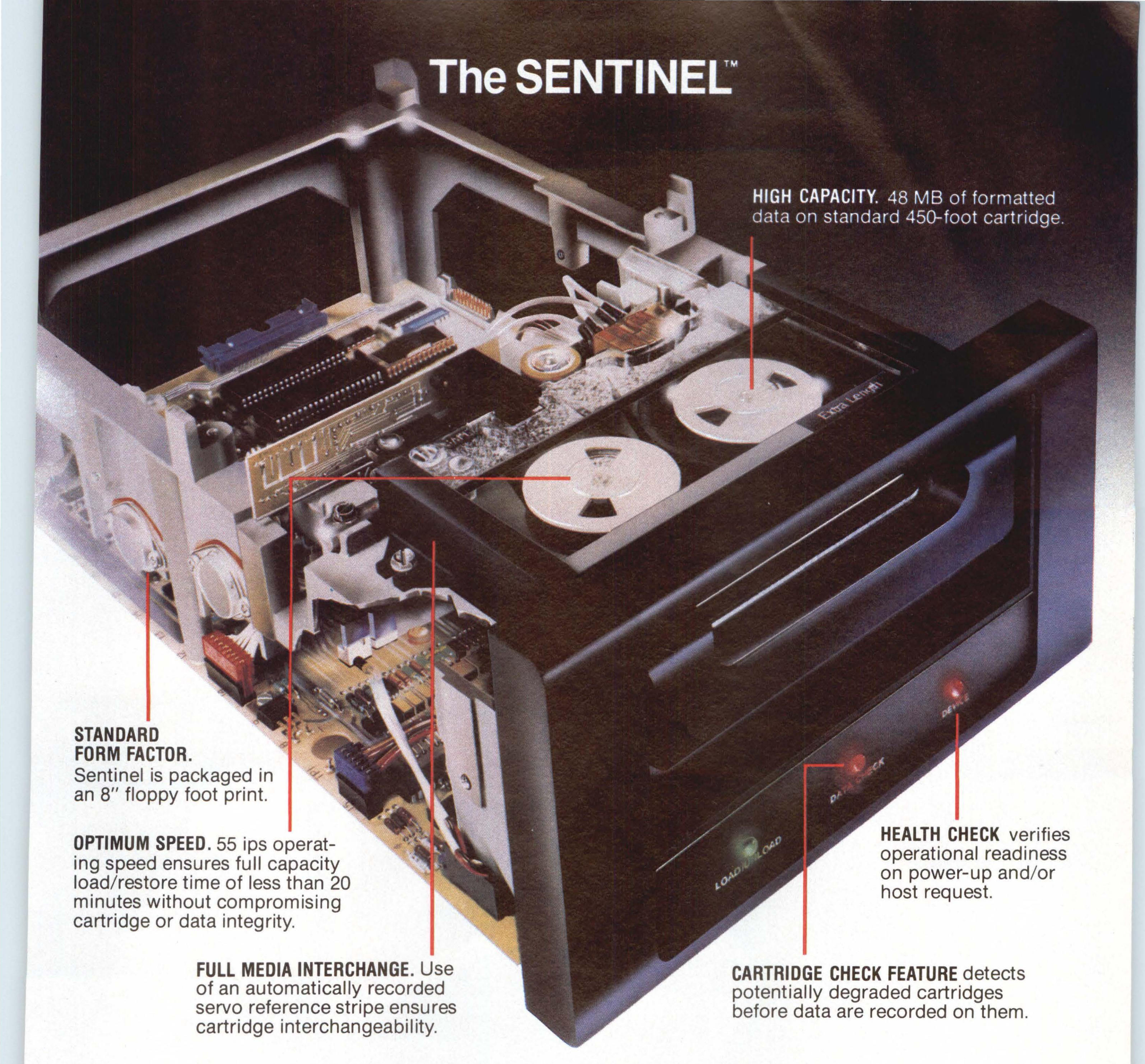

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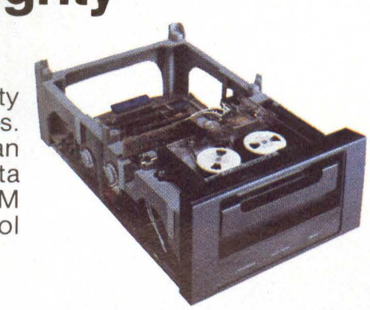

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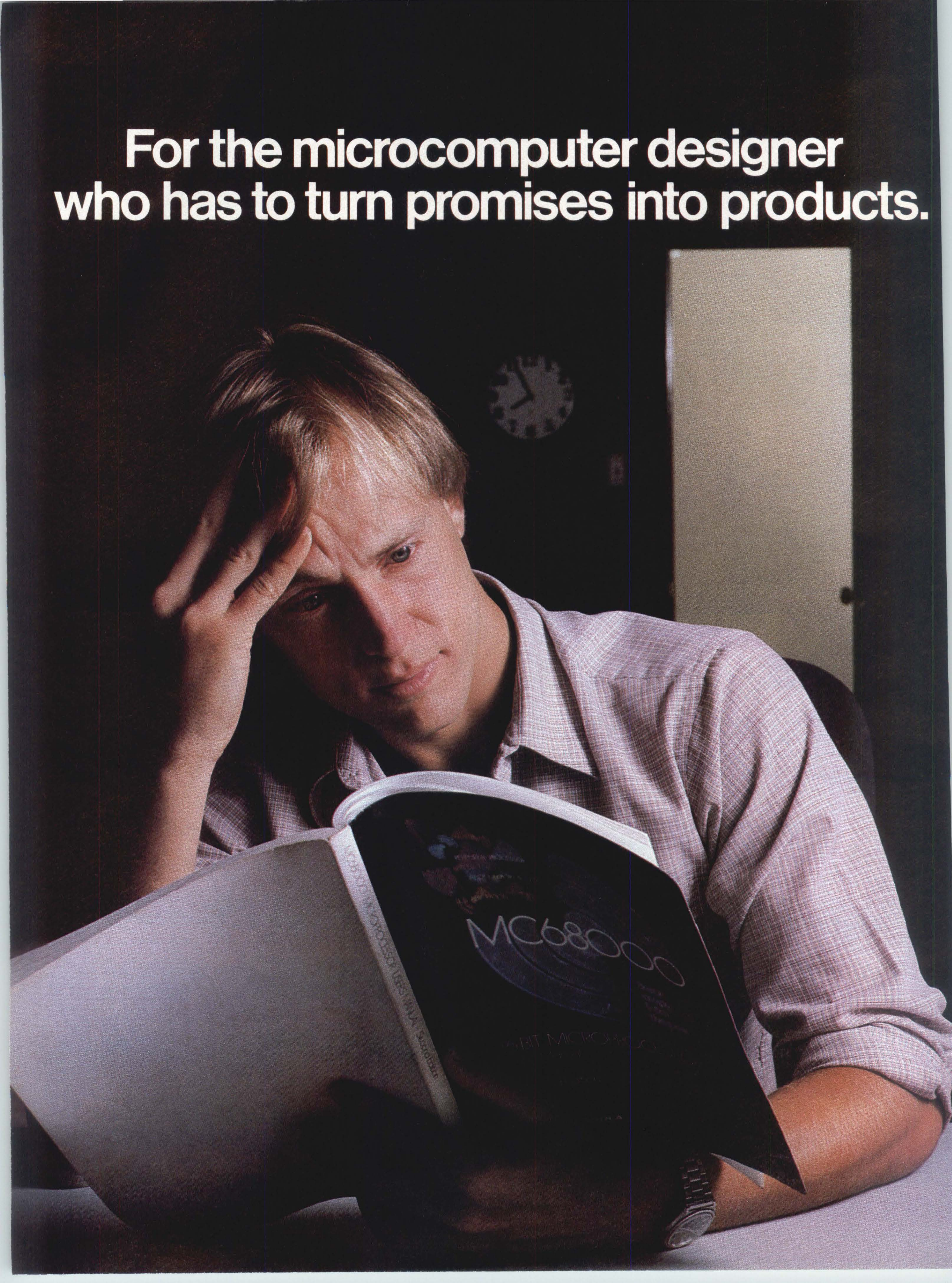
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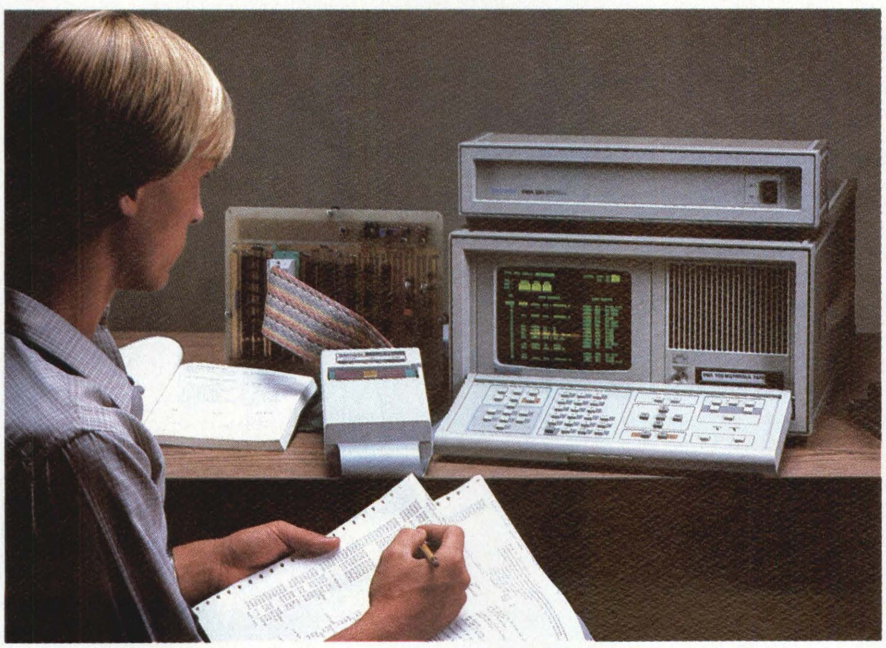

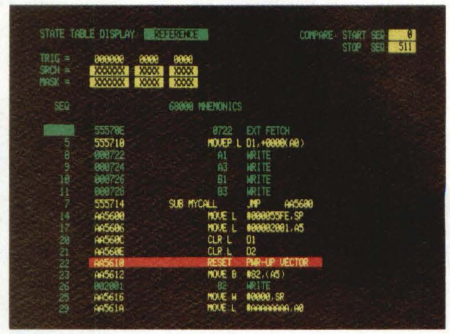

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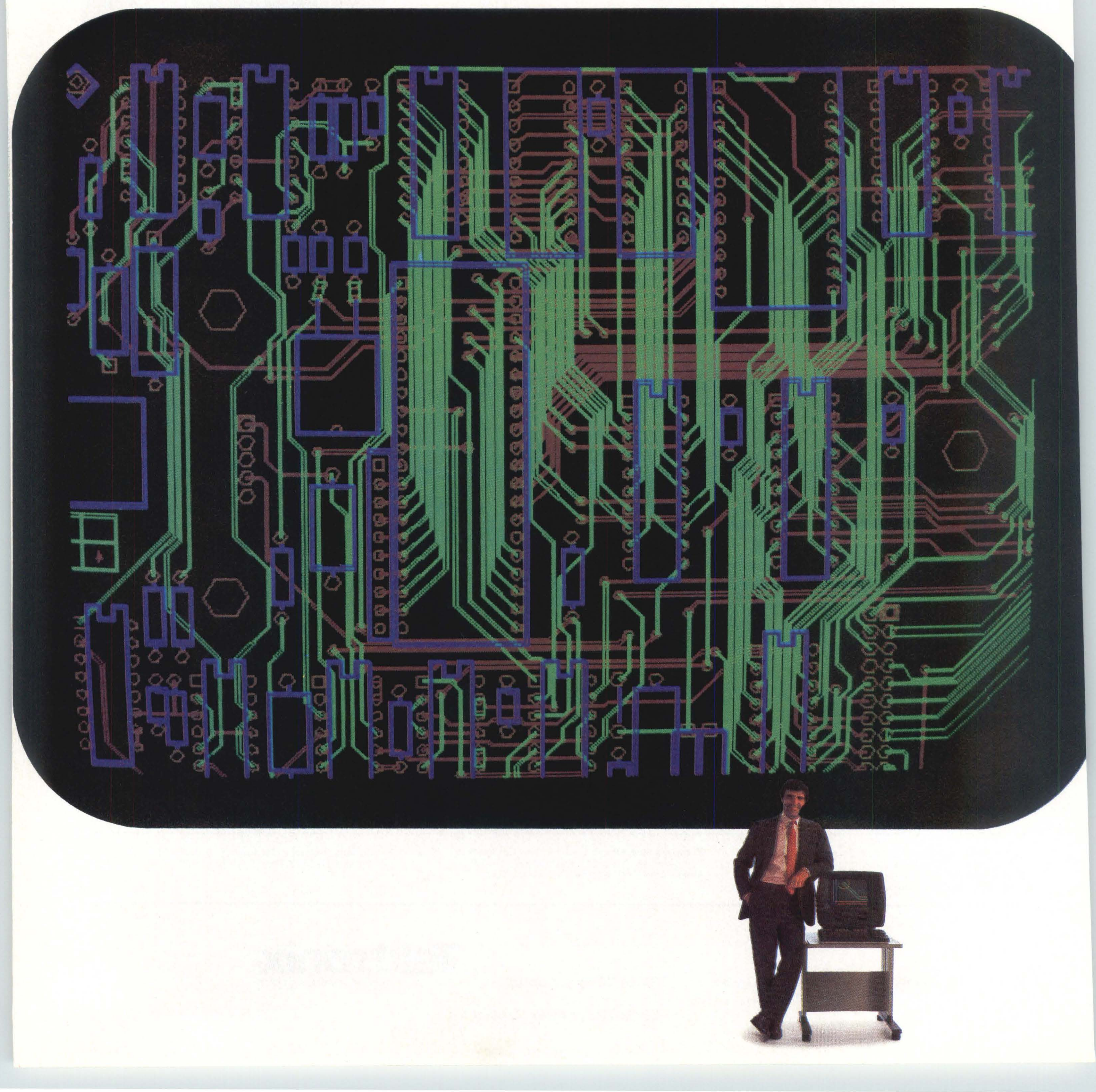

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CIRCLE 74

EXCEPTION HANDLING IMPROVES REALTIME SYSTEM PERFORMANCE

Operating systems hold the key to spontaneity for realtime exception handling in control and other time-critical applications.

by Michael D. Broido

Error handling is one of the most important aspects of a realtime computer system. It is vital that the system be able to detect, isolate, identify, and correct abnormal conditions that occur during the execution of any task. This is especially true in systems with time-critical requirements or other aspects that make it imperative to maintain control.

In computer systems employing some kind of memory map, application programs are often isolated from critical system tables that would be otherwise vulnerable to errant or even hostile user code. However, this same protective mechanism can make it difficult for an application program to determine precisely what has gone wrong, and quickly and appropriately respond to exceptional conditions.

The most common solutions to this complex situation create problems of their own. How can users construct complex, realtime applications that respond correctly to a wide variety of situations, yet keep development time to a minimum? The Computer Automation Realtime Operating System (CARTOS*) is designed to address these difficulties in a fashion that meets response time requirements without compromising system integrity.

Michael D. Broido was manager of software development and software quality assurance at Computer Automation, Inc when this article was prepared. He is currently manager of software at Data Card Corp, Troy Div, 2331 S Pullman St, Santa Ana, CA 92705. Mr Broido holds a BS in math and information science from the California Institute of Technology and an MSCS from the University of Southern California.

Traditional operating systems

Historically, effectiveness in the development and execution of realtime applications was impeded by the management of exceptional situations. A process that must make use of operating system services explicitly (by subprogram invocation) or implicitly (eg, arithmetic exceptions) usually takes one of two paths.

In many systems, the process committing the offense is simply terminated unconditionally. Loss of control over a program's destiny makes this method inappropriate for process control or other realtime applications. In other systems, all system service calls return a status value in some predefined location, which is typically a register. This usually requires the expenditure of additional code and execution time to examine the return status on each call, even though a normal status is most often returned. Such an all or nothing approach promotes the creation of large amounts of "throwaway" code. As successively larger subsystems are integrated, previously written stubs are discarded. This increases application development time.

In addition, of all the possible error conditions that can occur in a system call, only a few are of special interest such as "resource not available" and device errors. The applications programmer addresses and corrects these "locally." Other kinds of errors typically not handled locally include uninstalled memory, arithmetic exceptions, and unimplemented instructions. For these conditions, corrective action is likely to be centralized or ignored.

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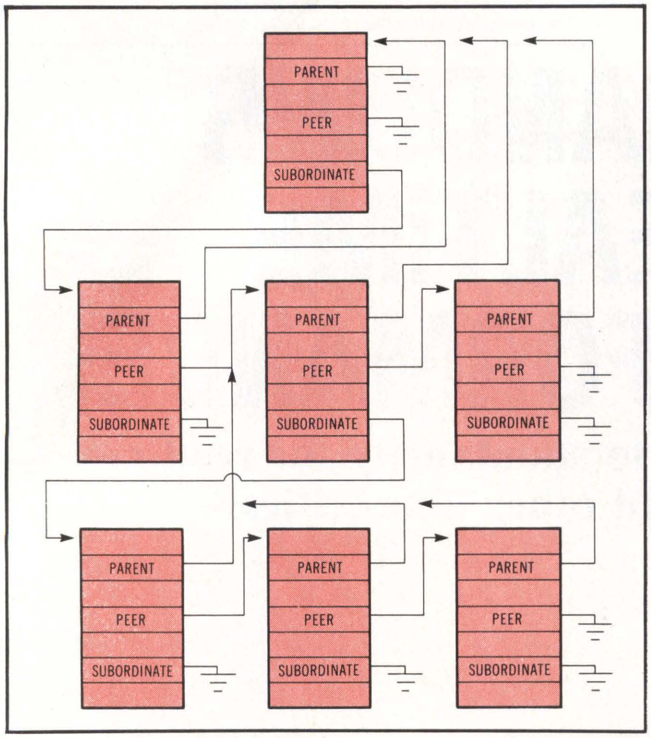

Fig 1 Relationship of typical system environment structures to each other. Each environment can point to three others via an internal table.

How this system differs

CARTOS runs on the Computer Automation NAKED MINI** 4/Series 5 systems. The 4/Series 5 systems contain a memory map that supports up to 16 simultaneous logical address spaces and a total physical memory of up to 8M bytes. These systems also contain extensions to the instruction repertoire of earlier NAKED MINI 4 systems, including single instructions that save and restore context, manipulate semaphores, and provide stack-relative addressing. They also have a user protected mode, in which certain privileged instructions, such as initiating input/output (I/O) and inhibiting interrupts, are not allowed. Because it is independent of operation in the system map or in a user map, this mode allows the software to selectively determine which programs may execute the privileged instructions. Since I/O drivers and managers need not be in the system map, bottlenecks common in other extended minicomputer operating systems are greatly alleviated.

The hardware memory map allows the software to assign almost any combination of logical to physical memory mapping. While each logical address space typically has up to 64 of its own 2k-byte pages, the physical pages can be shared among several of the logical address spaces. If several logical spaces share the same page, they are not restricted to assigning that page to the same locations in each logical map.

Designers were faced with the problems extending from earlier systems of incorporating a realtime executive with supporting I/O and file management subsystems into the 4/Series 5 processors. Here, the system and user memory were isolated from one another by the memory map. System services had to be added to facilitate communication between the user application and the system. In addition, the designers wanted to increase the system's flexibility. Now, system blocks, such as semaphores, mailboxes, and logical units, are dynamic instead of static. In addition, a mechanism for transmitting relatively large blocks of data among the maps is used. Most importantly, a mechanism for communicating error conditions has been devised to meet designers' speed and flexibility goals, while protecting the system from errant or hostile user programs.

In order to meet speed and memory size goals, all possible conditions are assigned a 16-bit (1-word) value. This value is passed from whatever software detects the condition to all other parts of the system (including user applications) that need it. User oriented programs, such as the master control environment of the application development system, can readily translate these into meaningful text. The possible responses, or condition values, are divided into three classes. Normal ("good") returns are always assigned the value zero. Other responses are divided into two sets: abnormal conditions and exceptions. Abnormal conditions, such as end of file, are assigned positive values. More serious problems, such as trying to access a resource that does not exist, are termed exceptions and are assigned negative values. This facilitates rapid classification of the possible results from system service requests.

To further speed disposition of error results, all nonzero conditions are divided into 16 classes, including realtime errors, I/O errors, internal traps (eg, arithmetic exceptions), and so on. One of the 16 classes is permanently reserved for definition by application designers. Within each class, up to 256 distinct error conditions can be defined. In addition, a special system service permits an application, user written system service, or user written device driver to generate an exception, invoking all the mechanisms described below.

When running, the system consists of a hierarchy of environments. Each environment is separately linked and corresponds to a program. Typically, each environment has its own logical address space, although multiple cooperating environments can share a single space. Each environment can point to three others in a binary tree: its first subordinate, a peer, and its parent (Fig 1). The system environment is at the root. Environments are used for privilege and resource allocation. This is accomplished through an internal table, called an environment control block (ECB), associated with each active environment. The ECBs are kept in the system space, where users cannot tamper with them.

Another important data structure associated with each environment is the exception vector table (XVT). The XVT is optional, but must be present if the environments' activities (exception instances) are to handle their own exceptions. If present, the XVT is in the user's logical address space. Consequently, it may be modified dynamically as activities pass through different phases in order to accomplish their objectives.

The ECB has a pointer to the corresponding XVT, so that the operating system can determine the appropriate actions to take if an exception occurs. The XVT consists of two parts, as shown in Fig 2. The first part contains fixed information, including a checkword. The checkword is used to determine that the programmer has not reused the memory occupied by the XVT for some other

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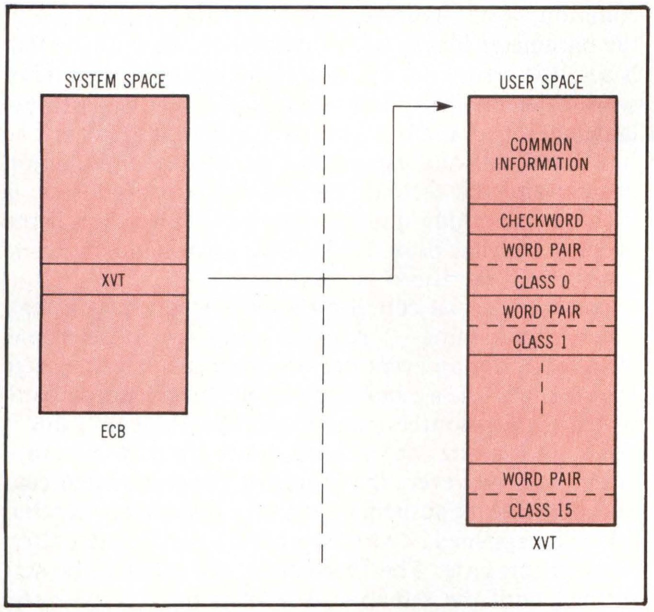

Fig 2 Constituents of exception vector table (XVT). Vector table determines when, where, and what exception action is appropriate.

purpose by the time an exception is encountered. The second part of the XVT consists of 16 word pairs, one for each exception class. Each pair consists of a mode word, which selects the specific actions to be taken for that class of exception, and an address.

Programmers can select any combination of the following modes for each class: ignore the error, cause a dump (to disk), pass the exception to the parent environment, or transfer to the address associated with this class. The address generally points to a generalized debugger, such as one supplied with the system, or to the address of specific application-dependent code that handles exceptions of the given class. Several classes may vector to the same location. This structure permits a program to handle certain classes of exceptions itself, and to hand off other classes to its parent environment. Such a design supports the phased evolution of the program, allowing it to gradually take on more responsibility for handling its own errors.

This data flow works in the following way (Fig 3). The system first determines that an exception should be generated. This can occur because the application has gotten some internal trap, such as divide by zero, or attempted execution of an unimplemented instruction. It can also occur because the program has deliberately generated an exception, using a special system service. Most commonly, however, the exceptional condition is detected at the conclusion of a system service call, just prior to returning to the application code. At that time, the status value used internally by the operating system is examined. If negative, the requested service could not be completed normally.

The operating system then determines if the environment on whose behalf it is running contains a valid XVT. If not, each environment, starting with the parent environment, is examined until one is found that can handle the exception. The system environment, at the root of the environment tree, always handles exceptions internal to itself or passed to it by its direct subordinates. Each exception code contains a class field; the word pair of the corresponding class is selected from the chosen environment's XVT. If the error class is to be ignored, control is immediately returned to the application program, which proceeds as if no exception occurred.

Otherwise, the system generates an exception information block (XIB) on the stack in use by the activity. Any errors encountered in building the XIB, such as insufficient stack space or uninstalled memory, cause the exception to be passed to the next eligible ancestral environment. In addition, the word pair selected from the XVT may indicate that any exceptions of the given class should be passed up. The activity is also marked, so that if it should generate any new exceptions prior to the resolution of the first, the later exceptions will also be passed up. The XIB contains the complete context of the error, including all register settings, a description of the activity and environment in which the exception was generated, the instruction last executed and its effective address, a checkword, and the error code itself.

If the activity is to handle its own exceptions, the system uses the second half of the word pair as a transfer address. This can point at code designed to specifically handle that class of error, or it can point to a general purpose debugging tool. One of the registers is set up to point at the XIB just generated. The original register values can still be found in the XIB itself.

At this point, the activity can rapidly process the exception, especially since the first level of error decoding has already been done. The activity can correct the condition that caused the fault and retry. It can invoke some extraordinary recovery code. This activity can also examine all the conditions surrounding the exception, including detailed decoding of the error, and then decide not to handle the error itself. That is, it can

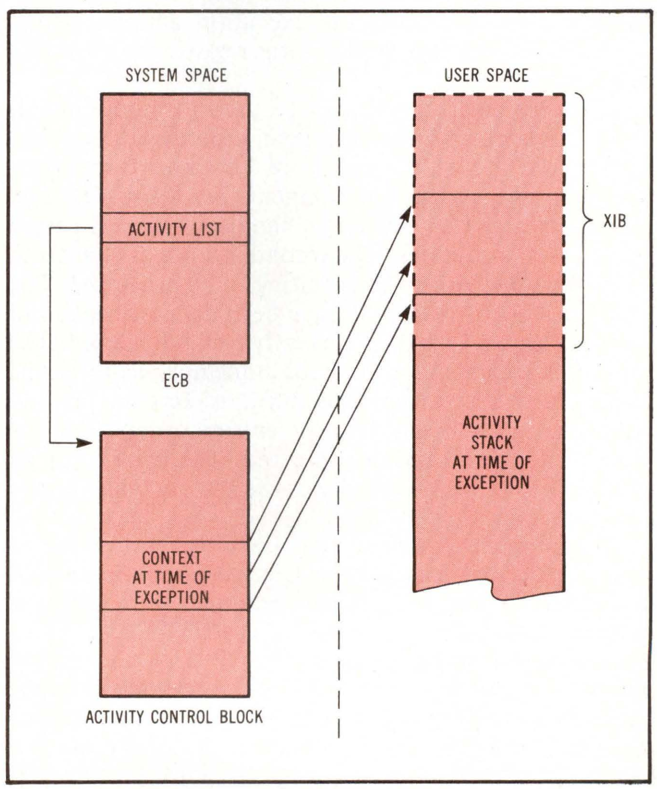

Fig 3 Exception data flow sequence. Once system determines that exception action is necessary and valid XVT is available, activity is initiated.

further sieve out the errors it will correct and later decide to pass the hard ones to its parent environment anyway.

An activity may not handle its own exceptions for several reasons. Either its environment has no XVT, or the XVT directs that they be passed up to the parent for a particular class. Further, the activity may selectively pass up a specific error. In any of these cases, the activity causing the exception is suspended. The XIB is given to an activity in the parent environment, which has executed a "wait for exception" system service. The activity in the parent environment may take whatever corrective action is necessary and then release the XIB. This allows the suspended activity to resume. The master development environment has several interactive commands that allow a human operator to perform these corrections. One of these, the reenter command, allows the suspended activity to resume execution at the point of failure. If the failure is detected on exit from a system service call, the call is reexecuted, unless the instruction register of the context has been modified.

This system...provides greater flexibility, since programs can evolve into increasingly more complex and detailed error recovery schemes.

The exception is cleared when one of three actions takes place: when the exception is passed to an ancestral environment, when the activity ends, or when the activity executes a special "return from exception" system service. The third action may follow context modification, including the execution address. However, the privilege bits in the status register are protected from modification.

A parent environment can be used to monitor multiple cooperating or independent subordinate environments. To do this, each ECB contains three lists, although only parent environments use them. The first is a list of activities waiting to handle exceptions passed up from subordinates. The second is a list of XIBs from subordinate environments waiting to be processed. The third is a list of XIBs that have been acknowledged but not yet cleared—the ones currently being processed. The first and second list cannot be nonempty at the same time. Each list, except the third, is kept in priority sequence, with equal priority entries ordered by the times that the exceptions occurred. The priority of an XIB is taken to be the priority of the activity that received the exception.

A parent environment can use a system service to copy a block of memory to or from any of its direct subordinates. In this way it can examine or modify the address space (but not sensitive system blocks) of its subordinates, using data in the XIB. If the parent chooses, it can also interface with a cathode ray tube (CRT) to assist programmers in debugging applications.

There are a few special circumstances under which a slightly modified scheme is applied. One such case is when input or output operations are either directly or indirectly involved, as when a program or an overlay is being loaded. Under these conditions, errors are at least common, if not expected. A special flag is provided in the parameter blocks used for these services. If the flag is set, I/O errors do not cause an exception, but other types of errors do. These services provide the assembly language programmer with two return addresses. The first is used if any exceptional or abnormal condition occurs, and the second, the normal return address, is used when nothing unusual happens. Thus, even if the programmer has provided his own error handling, code speed is not sacrificed in most cases.

Another special condition applies frequently in realtime programming. It is often necessary to determine whether or not an event has occurred such as a message inserted in a list, a clock expired, an I/O operation completed, or a resource made available. Typically, this is done by waiting on a semaphore. In realtime programming, however, the inquiring program often cannot afford to be suspended if the anticipated action has not yet happened. CARTOS provides two kinds of services in this case. The first causes the caller to be suspended until the semaphore reaches the desired state; the second uses two return addresses, analogous to the treatment of the I/O services. The first is used, without generating any exception, if the event has not taken place. The second is used if the event has occurred. Any messages are then transferred to the appropriate places.

Another troublesome area in realtime systems programming deals with asynchronous exceptions. These are generally events that occur outside the scope and control of the current environment, such as CRT "break" interrupts, power failure, and system shutdown requests. It is highly desirable to avoid polling a flag, while not consuming resources for an activity that explicitly waits for such events.

Under CARTOS, an activity can "sign up" its environment to receive each specific error, such as break exceptions from a particular CRT. The environment is put on a list to receive such warnings, but the sytem is otherwise passive. It is the environment that is inserted in the list, rather than the activity, since environments own resources (ie, the right to be notified of the event).

When an appropriate event occurs, the environment is marked. The next time any activity of that environment is dispatched (ie, gains control of the central processing unit) with no other exception pending, a special exception is generated. The XIB fully describes the condition. Using this mechanism, the environment gets the earliest notification that is consistent with the strict priority ordering needed for a realtime system.

Advantages for developer and user

This structure, although more complex than that employed in other systems, provides several advantages to applications developers and users. First, programs are smaller, because it is no longer necessary to explicitly check the results of each system service call. If control returns after the call, the application may "assume" that everything proceeded normally. Second, programs are faster, since status checking is not done by the application program after each call. Thus, no delay is experienced in most cases. In addition, for programs running on the 4/95 model, the smaller programs lead to increased "locality" of code executed in loops. This yields a higher probability of getting a cache hit in the memory unit, reducing effective memory reference time.

This system also provides greater flexibility, since programs can evolve into increasingly more complex and detailed error recovery schemes. The dynamic nature of the XVT permits the use of different error recovery techniques at various times during program execution. In addition, diverse application programs can be created under a development host, which can cope with any error conditions not handled by the applications themselves.

Reliability of the system as a whole is increased by limiting the scope of a program gone wild.

Reliability increases because the design facilitates the separation of mainline flow from error handling. The programmer can concentrate on normal flow conditions without being distracted by possible exceptions. Similarly, centralized abnormal condition handling encourages a uniform approach to managing errors. Moreover, development takes place on the same system used for execution, avoiding problems with cross compilers, media interchange, and downline loading to a different target system.

In addition, system reliability as a whole is increased by limiting the scope of a program gone wild. A program can only run rampant in its own logical address space. Other maps (environments), including the system code itself, are protected. Also, any exception that requires operator intervention need only hold up the environment handling it; the rest of the system can proceed independently.

Development time is reduced because programs do not need extensive stubs for handling errors as design and implementation proceed. The hierarchical error recovery scheme allows developers to use a parent environment to trap all errors not handled by the program under development. Thus, if the program does not deal with any errors, its parent can trap them and notify the tester. CARTOS includes one such parent, the master development environment; users may also write their own. The message, queue, and shared memory capabilities can also be used to communicate more information about the circumstances, or for the test case being attempted. This system also allows the parent and subordinate environments to share the same logical address space. This gives each environment access to all user code and data in the other.

The hierarchical environment structure and memory map allow a parent environment to monitor one or more subordinates, safe from exceptions occurring in immature applications. Developers can gradually increase the robustness of new programs, adding exception handling at their convenience.

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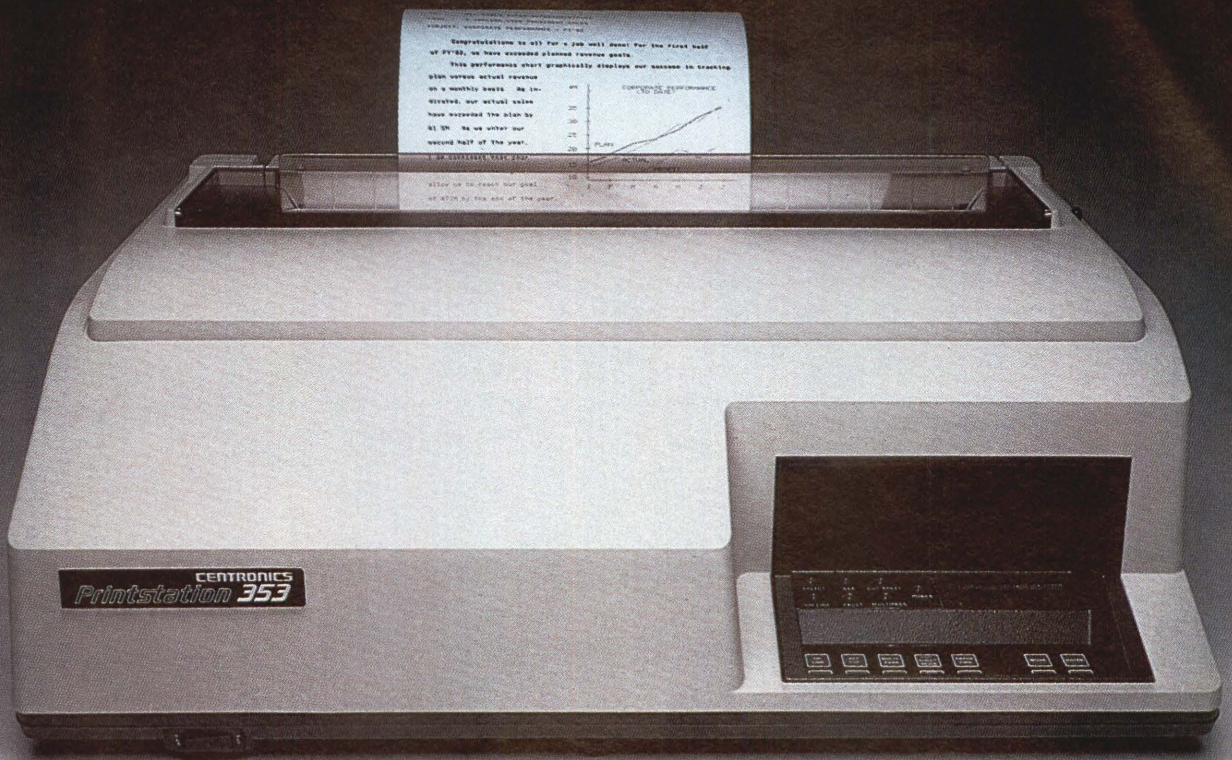

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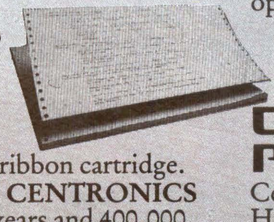

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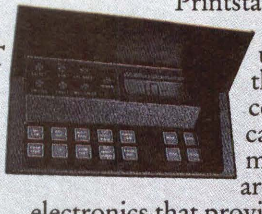

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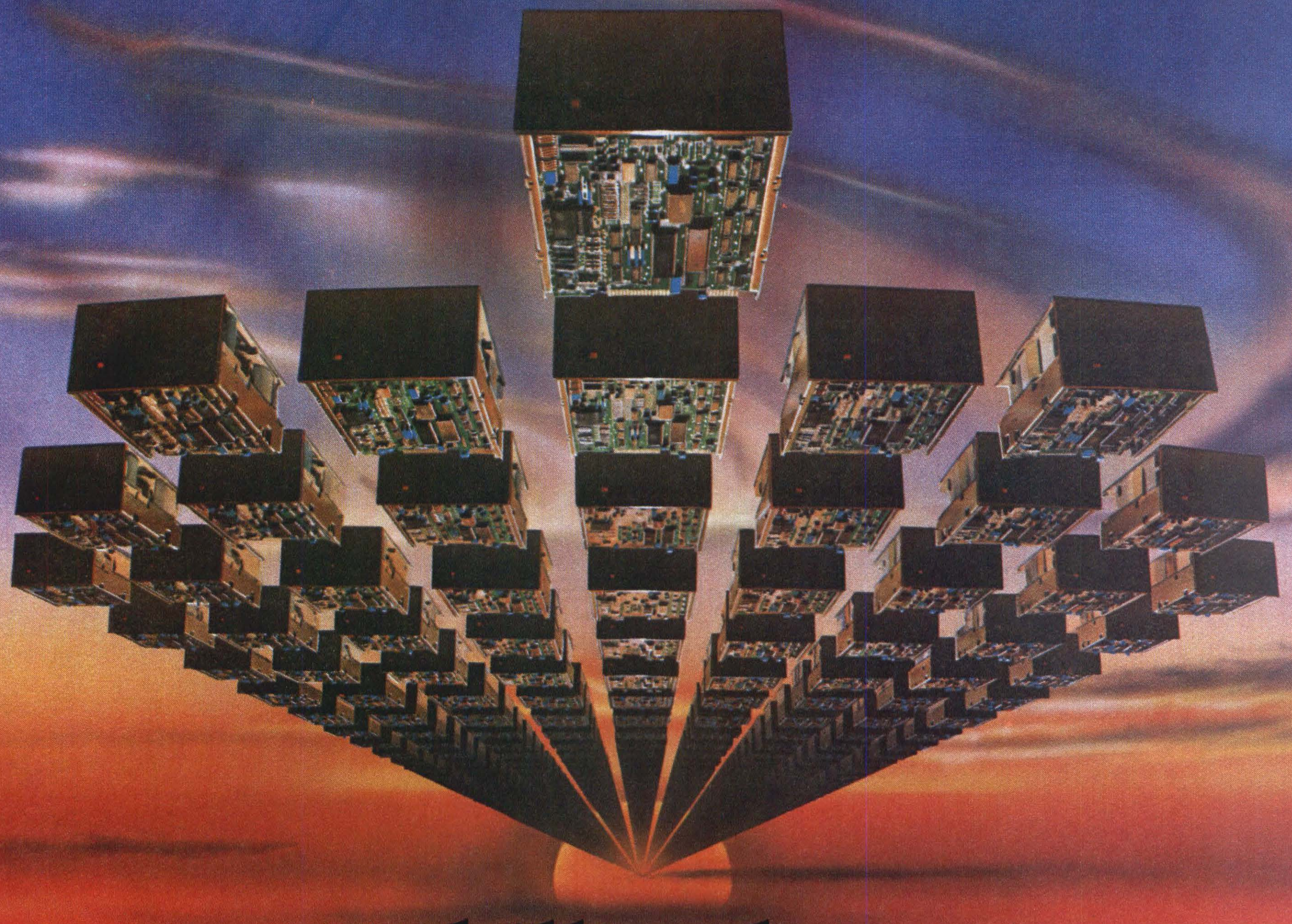

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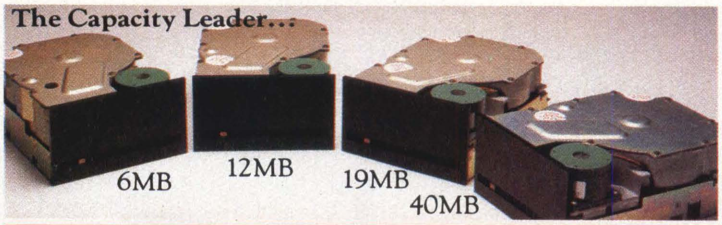

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SMART APPROACHES TO MAGNETIC PERIPHERAL INTEGRATION

Exploiting intelligence of today's smart controllers is one way system integrators cope with the problem of peripheral interfacing.

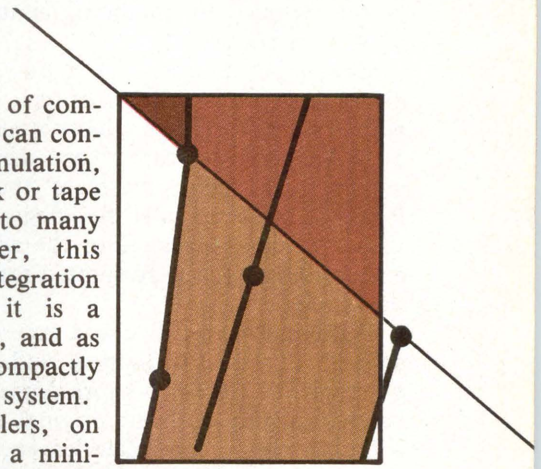
by Chappell Cory, III

As computer system prices drop and performance increases, mass storage becomes a bigger part of the ticket price. Confronted with a plethora of memory products to choose from, system integrators must interface a particular device with a particular processor. This task increases in difficulty as technology advances in memory peripheral design, leaving computer development, especially software, woefully lagging.

Building a magnetic peripheral into a system creates many problems for the integrator. Disk and tape technologies have advanced at different rates and many standardization levels exist. Moreover, a wide array of interfaces and buses compound system development problems. Packaging and protecting cumbersome and temperamental drives often adds to the integrator's headaches as well. Over the past several years, the manufacturer specializing in peripheral controller technology filled this void. As memory technology advances over the next decade, his role will continue to evolve.

Current technology

The disk and tape control world is divided into two parts, represented by formatted and embedded controllers. The formatted approach supplies an integrator with a general purpose box using various adapter cards suitable for a variety of computers. The box itself can contain intelligence for emulation, allowing a single disk or tape drive to be coupled to many processors. However, this approach presents integration difficulties because it is a standalone controller, and as such, cannot be compactly packaged into a total system.



Embedded controllers, on the other hand, use a minimum of printed circuit cards that meet the form factor of specific processors. This allows cards to be embedded directly in the input/output (I/O) slots of the computer. Cables run directly from such cards to the memory drives and provide the integrator with a more compact, more reliable (ie, with fewer parts), and specifically dedicated controller. Because the controller is designed with a single disk and a single computer in mind, software can be optimized with special features and different emulations supplied through microprogramming. Not only are upgrades accomplished more easily, but, as is done with the formatted approach and its coupler cards, newer system components can be accommodated through software rather than hardware adaptations.

Disk drive controllers are evenly divided between formatted and embedded approaches. As new disk drive technologies debut, integrators tend to favor the formatted approach for evaluations. A single formatted controller, with many customized boards for various drives and a full stock of coupler cards for the processors, allows the integrator full flexibility to look at all disk drive models. Once an integrator has chosen a drive, an embedded controller provides the reliability of a lowered component count, as well as increased performance of microprogrammed special features and

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TABLE 1

Popular Bus Structures

Name	Manufacturer	Width (Bit)	Card Size
S100	Many	16	5.25 x 8
MULTIBUS	Intel	16	6.75 x 12
Q-bus	DEC	16	5.25 x 8.5
UNIBUS	DEC	16	8 x 15
I/O	DG	16	15 x 15
STD	Zilog	16	15 x 15
IEEE 488	HP	8	Various
VMEBUS	Motorola	16/32	9.2 x 6.3
VERSABUS	Motorola	16/32	9.25 x 14.5
CMI	DEC	32	8 x 15
SBI	DEC	32	15 x 15

emulations. This is possible at about the same cost as a formatted drive, plus custom coupler card.

Formatted controllers are favored by OEM users because of the inherent flexibility and greater power of the controller. Features of the disk drive, which have to be downgraded by emulating controllers, can be fully utilized by the OEM.

Many tape manufacturers supply their own formatted drives with coupler cards. In fact, Pertec's 9-track formatted interface is an industry standard for most. A lot of the half-inch streamer tape drives coming into the market also have interfaces that closely resemble Pertec's. Once again, if the integrator is not concerned with a compact package or the advantages of a dedicated controller, the formatted tape drive approach is the answer.

Combinations of disk and tape drive controllers are offered in both formatted and embedded models, although the former is more popular by far. Unfortunately, hanging both the original drive and its backup off of a single controller leaves the integrator, who determines data integrity, particularly vulnerable to a single point of failure.

Changing parameters of integration

Integrating disk and tape drives into a total system becomes increasingly difficult as those drives take on more of their own monitoring via self-contained intelligence. The transfer of intelligence from the main processor out to the controllers is rapidly progressing. In some instances, the integrator is faced with a drive loaded with unnecessary options. Without a massive outlay in software development costs, such drives leave little room for flexible interfacing with the many central processing units (CPUs) being stocked.

Some disk drives incorporate features like error correction coding, sector flagging, and buffering. Manufacturers of these intelligent drives have defined their own internal bus to help monitor all functions, creating additional interfacing nightmares for integrators. Flexibility restrictions inhibit the number of CPUs a systems integrator works with because all software development for intelligent disk drives must be done from the ground level up.

Physically integrating disk drives into systems is no longer an easy chore. Floppy disk drives and small systems are made for each other, and with some engineering, work together easily. However, 8" Winchester disk drives are a different matter. They do not come with built-in power supplies, nor are they rackmountable. And, they cannot just be put on a desk next to a small business system. In this area, systems integrators have help from controller houses. Whether the disk drive is embedded or formatted, the controller house can solve some of the packaging problems.

Embedded disk drive controller cards fit snugly into the main chassis of the CPU, and the drives are built into cabinets. Although not completely incorporated in the CPU housing, formatted disk drive controllers can be packaged as standalone units. The coupler cards act as connectors to the main processor. In either case, it is the controller that now provides the needed power supplies, antistatic guards, and durable housing for sensitive drives.

Bus structures represent half of the interfacing problem that all integrators face. (See Table 1, "Popular Bus Structures.") Each manufacturer has its own bus peculiar to a computer family. Thus, every bus is incompatible with buses from different manufacturers. Much of a systems integrator's time and effort is spent trying to maintain compatibility, with respect to bus architectures, among different computers and disk drives. Controller houses are trying to help solve the problems inherent in this lack of bus standardization. Through a combination of hardware and microcode, the controller house can surmount this difficulty by making minimal changes to the bus interface architecture.

Bus structures represent half of the interfacing problem...integrators face.

The other half of the interfacing problem is that there is no single I/O standard, with respect to both tape and disk drives, that is truly accepted in the industry. For high performance, large Winchester disk drives, Control Data Corp has supplied the SMD as a *de facto* standard. Pertec has standards for tape drives that are applicable to both unformatted and formatted units. This is also true of the half-inch streamer tape that uses a Pertec standard. Moreover, 8" Winchesters may very well use the XT3.9 American National Standards Institute as standard, although this is yet to be established. The 5¼" Winchesters have the *de facto* Seagate standard to operate under. Suppliers of tomorrow's high performance hard disks have no standard as yet. And manufacturers of the quarter-inch streamer tapes are still looking for a standard. (See Table 2, "Interface Standards," for a breakdown of some of the more common disk interface uses.)

Where there are no standards, growth in the number of available controllers and drivers is slowed dramatically. Even if an integrator develops a special I/O interface for a particular drive, he runs the risk that the drive will not find acceptance. And yet, if the drive is not consistent with an available standard, evaluation is difficult, if not impossible.

Software technology drag is the single most inhibiting factor in the integration of state of the art magnetic peripherals into present-day computer systems. Operating systems that computer manufacturers

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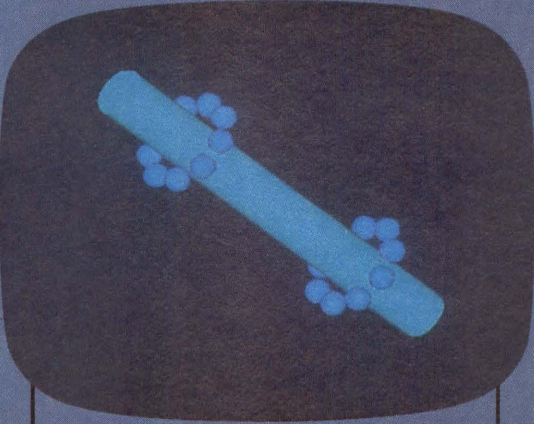

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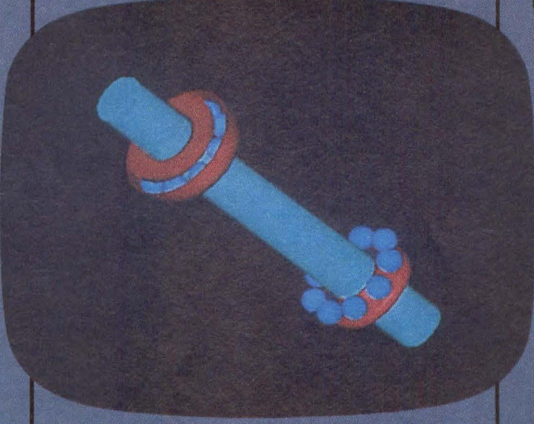

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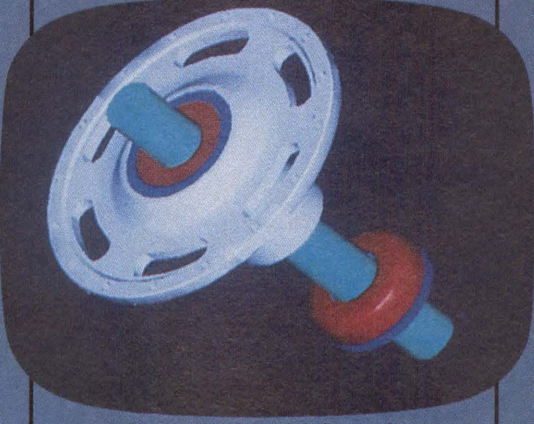

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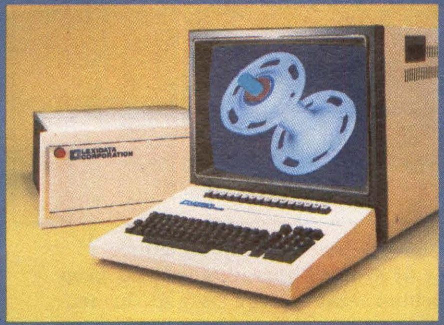

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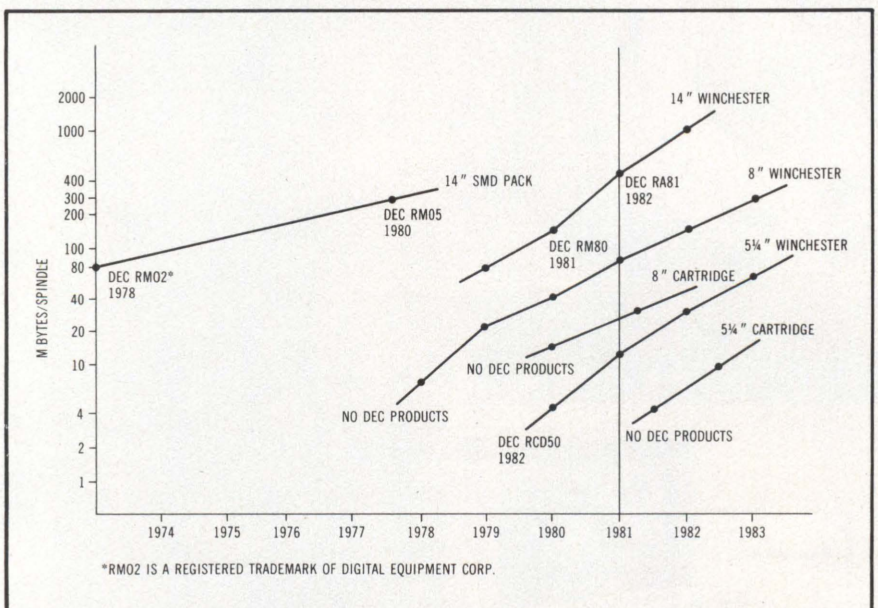
TABLE 2

Interface Standards

Interface	Manufacturer	Drive type	Data rate (M bytes/s)	Capacity	Performance
D44B	Diablo	5440	0.312	5M to 20M bytes	Medium
T50	Calcomp	Pack	0.806	50M to 300M bytes	High
SMD	CDC	14" pack	1.2	40M to 300M bytes	High
		8" removable Winchester	1.2	8M to 80M bytes	High
ANSI	Many	Various	Up to 1.2	8M to 80M bytes	Medium-high
ST506	Seagate	5¼"	0.625	6M to 14M bytes	Low
SA1000	Shugart	8" Winchester	0.650	10M to 40M bytes	Low
Disk bus	Kennedy	8" Winchester	0.800	8M to 40M bytes	High
Disc bus	IMI	5¼", 8" Winchester	0.648	5M to 40M bytes	High
Priam bus	Priam	8" Winchester	1.0	10M to 70M bytes	High
		14" Winchester	1.0	33M to 154M bytes	High
Micropolis	Micropolis	8" Winchester	0.929		
Unknown	1983-5	8", 14"	1.8 to 3.0		

implemented in earlier development cycles have locked these manufacturers into outmoded, underpowered peripherals for their systems. Most mainframe vendors lag several years behind in state of the art peripheral technology. Thus, their operating systems cannot keep pace with faster, more complex housekeeping chores associated with the up to date peripheral technology.

At most minicomputer companies (except IBM), the evaluation and integration design cycle is long for purchased equipment like disk and tape peripherals. This extended integration cycle adds to the technology drag. For example, Digital Equipment Corp (DEC) had not announced a disk drive family with state of the art timing for the last few years until recently (see the Figure). Trend lines show capacities for five state of the art drive technologies increasing over a 10-year period. During this time, DEC announcements have run from one to four years behind for larger drives; DEC's newest announcement for small 5¼" disks is a purchased product. The DEC RL01/02, not shown on the chart, was announced in 1979 and is based on embedded servo technology introduced by Diablo in 1973.



Mass storage capacity advances for typical large mainframe manufacturer. Extended integration cycles and inadequacy of evolved operating systems keep large computer makers one to four years behind mass storage state of the art.

Enhancing the present

Current systems cannot, for the most part, use intelligent emulators to their maximum. Rather, the intelligence in these more powerful processors is used to make the disk drives look more like the ones used 10 to 15 years ago. This is for compatibility with operating systems developed at that time. The only manufacturers who can use all of the power associated with the newer magnetic peripherals are those who have recently developed totally new operating systems, such as Apollo or Stratus.

An operating system typically takes four to five years to develop, at a cost of up to $5 million. Vendors often decide to live with outmoded magnetic peripheral technology rather than attempt to update an operating system for newer technology. However, in an attempt to bridge the software technology gap, controller houses are building more into disk drive controllers. Added features often include self-diagnostics, error correction coding, flaw mapping, buffering, and intelligent direct memory access (DMA). This saves valuable processing time, as well as increases compatibility between older software products and new magnetic peripherals.

Self-diagnostics. Improved self-checking functionality is possible because most magnetic peripheral controllers contain microprocessors. On power-up or initialization, a controller can run special microcode that confirms the health of major portions of the controller itself. Also, special commands or switch

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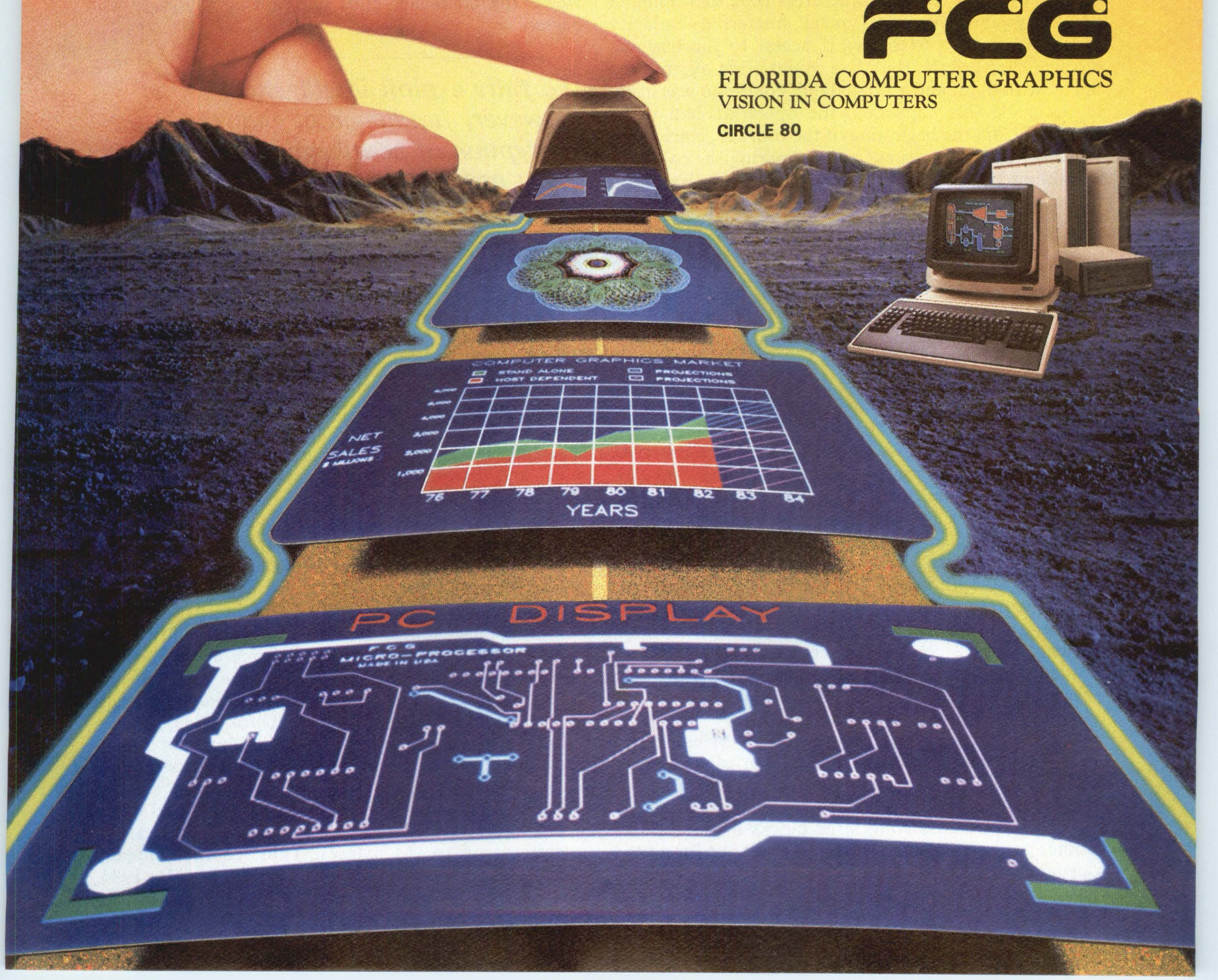

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functions can perform even more thorough diagnostic checking, formatting, and calibration procedures on both the controller and the disk or tape. The customer field service engineer or the manufacturer's test department can use these features to rapidly isolate faults as well as install and totally integrate the system.

Error correction and flaw mapping. Available high density disk drives, especially Winchesters, have a higher media defect count and soft error rate than drives using older technology. Most operating systems are not well equipped to deal with these conditions. However, many disk controllers on today's market can take corrective action without interfering with the operating system. Using the controller's internal microprocessor, error correction can be accomplished by applying Fire codes or other error correction codes to the data before transfer to the main CPU. Sector slip and alternate track techniques can be used by the controller to map out media defects during formatting. With these approaches, average transfer rates improve. In addition, with its innately higher performance, the high technology disk can be made to look like a lower performance, older disk drive to less efficient operating systems.

Buffering. Most disk and tape controller buffers offered by computer manufacturers have had minimal buffering capabilities. Typical buffering capacity ranged from 2 to 64 bytes. If access to the bus was blocked even briefly, the drive would often overrun the buffer with data, and a "data late" condition was likely to occur. If this happened, the operation had to be restarted from the beginning of the transfer, consuming valuable processor time and requiring a complete revolution of the disk drive. Although this condition was considered a soft error and was automatically corrected by the operating system without the user being aware that it had ever occurred, overall system performance was degraded.

By increasing buffer size to at least one sector—the physical record size on the disk, typically 256 or 512 bytes—a large percentage of all data lates are eliminated. No data lates occur if a 2-sector buffer scheme is used, although slowdowns are possible during long data transfers. Most emulating disk controllers have two or more sector buffers.

Intelligent DMA. Most CPU manufacturers use DMA for their peripheral controllers. DMA is a fast and efficient way to transfer data between disk or tape peripherals and main memory. In its simplest form (exemplified by devices supplied by CPU vendors) DMA has several drawbacks. Normally, a DMA transfer consists of only a few words at a time and is most desirable to prevent data lates from occurring on other DMA devices using the same bus. However, transferring only a small number of words consumes latency time—time used in requesting access, and then getting on and off the bus. Therefore, large block transfers are more desirable to lessen latency losses.

A method called adaptive DMA is used by emulating controllers to decrease such losses. In an adaptive DMA mode, the controller requests access to the bus. Once in control and transferring, the controller stays on the bus and continues transferring large blocks of data unless another peripheral controller requests the bus for a DMA transfer. By monitoring bus request lines, the controller can sense when another device needs the bus to get off quickly. This adaptive DMA technique allows high average transfer rates without "bus hog" or data late problems. No changes have to be made in software to take full advantage of this technique.

Future challenges

Intelligence in many disk drive controllers now equals the power of the computers to which they are connected. Integrators use some of that intelligence to improve overall system performance. To fully exploit intelligence, however, fundamental changes in the perception of peripherals and controllers must occur.

As system architecture grows more sophisticated, the controller will be able to perform functions like remote diagnostics, creating high speed data paths, command queuing, optimized command sorts, command chaining, key word searches, caching, file management, multiple-processor access, offline backup, database management, and network servicing. These functions will be implemented in peripheral controllers over the next five to eight years. Some capabilities, such as database management system and network servers, will take the controller into the arena of a fully developed computer. Eventually, users will find it difficult to determine where the controller ends and the computer system begins.

To fully exploit intelligence, however, fundamental changes in the perception of peripherals and controllers must occur.

Because technology is rapidly changing the scope of peripherals, selecting a competitive, optimum technology and form factoı with a minimum risk of obsolescence is the greatest difficulty facing an integrator. Major areas of concern include *technology*—Winchester, removable Winchester, group code recording tape, and streamer tape; *form factor*—5¼", 8", or 14" drives; *media size*—5", 8", or 14" in hard disk and quarter-inch and half-inch in (streamer) tape; *media compatibility*—IBM, DEC, Data General, etc; *buses*—8-, 16-, or 32-bits wide; and *drive interfaces*—currently SMD and others, with more to come in the future.

To give the systems integrator the maximum number of technological options in form factor, media size, and media compatibility, the controller house has the difficult task of providing connections for the buses and the drive interfaces. This difficulty is threefold. First, new computer buses appear on the market continually, while certain older bus architectures become more popular. Second, new peripherals appear with new interfaces at a very rapid rate, and more are on the drawing board with as yet undetermined interfaces. Third, data transfer rates increase on some peripherals and buses at a more rapid rate than on others, creating major speed inequities. (See Table 2.)

Disk transfer rates vary between 0.3M and 1.8M bytes/s. However, many 16-bit computer buses can operate at up to 2M bytes/s. Thus, conflicts already exist because of multiple devices on one bus. By 1984, disk drives with transfer rates of 3M bytes/s will be

available to the integrator. These drives are already available with some IBM systems.

Continuing role of the controller house

There is no defined interface at the drive level that can handle these rates. Most of what is available in controller technology will have to be revised to support these data rates. At that time, all 16-bit processor buses on the market will be inadequate to support the data rates. The push for high speed backup for faster Winchesters will also require faster controllers. The trend seems to be controllers moving to 32-bit buses with access to dual-ported memories using high speed data paths. Higher performance disk and tape interfaces will be integrated as soon as they are defined.

The push for high speed backup for faster Winchesters will also require faster controllers.

Soon, dual-purpose controllers will be capable of running both disk and tape peripherals simultaneously, as well as providing much needed, readily accessed, intelligent, offline backup. Overall controller intelligence is also increasing, with 16- and 32-bit metal oxide semiconductor microprocessors joining bit-slice processors directly within the controller to perform management functions associated with remote diagnostics, file management, backup, and transfer optimization. System modularity will become more prevalent, making quick adaptation of new computer, disk, and tape interfaces of prime importance to provide maximum flexibility for the integrator. The controller house will also serve as a packaging consultant, providing integrated subsystems of newer technologies.

Key to magnetic peripheral integration in the 1980s will be the continued cooperation of all parts of the industry—peripheral manufacturers developing interface standards and the controller houses working with the integrators and peripheral manufacturers to provide the necessary link between technologies.

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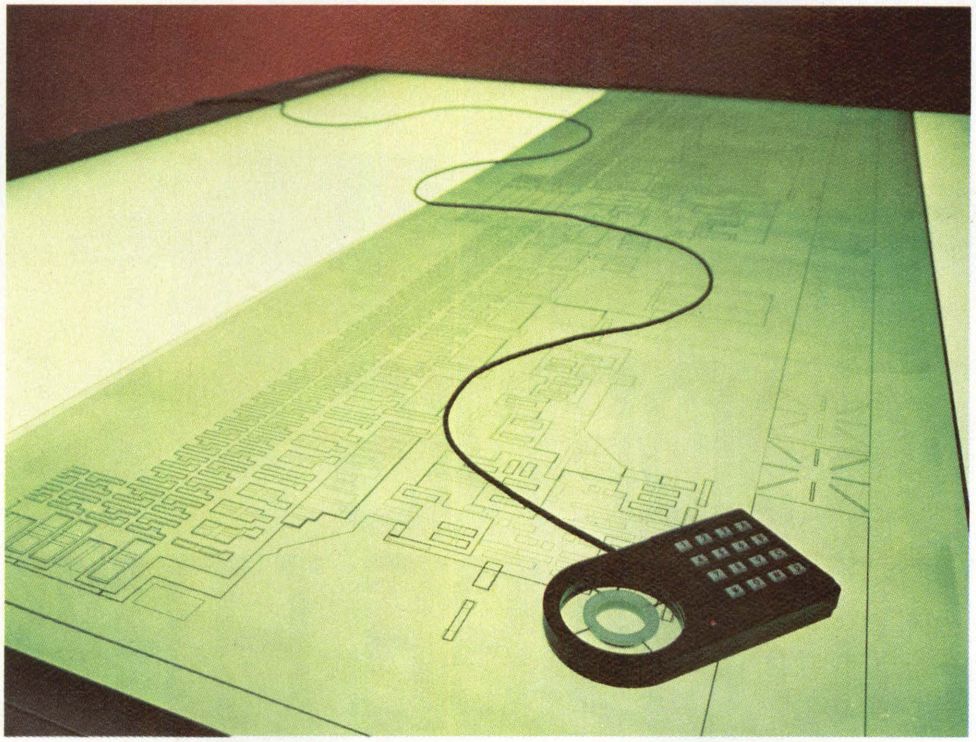

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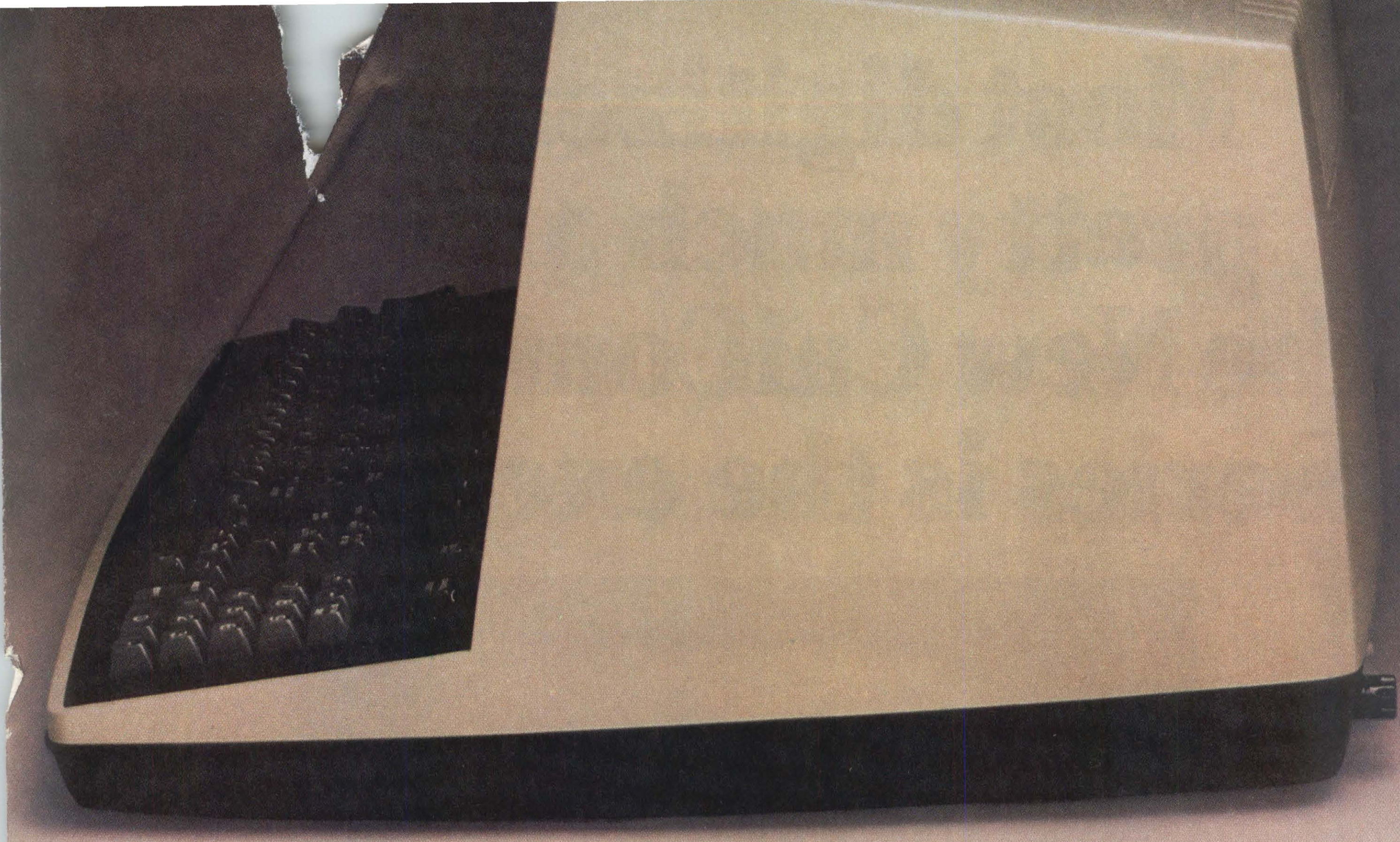


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MULTI-USER SYSTEMS FROM ADVANCED PROCESSOR CHIPS

Modern processors like the iAPX 286 allow designers to build multi-user systems that provide the benefits of global memory access without the drawbacks of poor user protection.

by Richard M. Schell

Today's very large scale integration and peripheral technologies enable marketing of small but powerful multi-user computers for less than $50,000. No multi-user system comes close to this cost. Based on microprocessor central processing units, often coupled to Winchester disks and thermal printer/copiers, they can support 5 to 15 users. Although primarily aimed at the small and medium business markets, these systems also find widespread use in engineering and scientific applications, computer aided design, computer aided manufacturing, and software development.

In the past, computers were shared for economic reasons. Today, with system hardware costs dropping, the major issue is database sharing. Data intensive applications involving groups of users or tasks are abundant and include very large scale integration design, office automation, medical diagnosis systems, public automatic branch exchange, and telecommunications. Multiple users must be connected to a single data base. Two basic configurations support sharing: distributed computing, which uses networks; and centralized computing, which uses workstations attached to a central computer.

Richard M. Schell is strategic planner at Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, where he is responsible for development systems planning. Previously, he worked for Intel as a microprocessor and 286 software architect. Mr Schell holds a BA, an MS, and a PhD from the University of Illinois.

Although networking is rapidly increasing in importance, in many applications it is still necessary to connect a data base to a single computer. Bandwidth requirements and file integrity make centralized data important; in addition, current operating systems are better suited to the shared computer model than to distributed computing. As a result, a combination of these concepts is being used to provide networked multi-user systems where the individual nodes help maintain a localized data base while providing sufficient processing power to accommodate the attached users' needs.

System requirements

Most contemporary multi-user minicomputer systems provide sophisticated computing environments and support large virtual and physical memories. Performance guarantees apparently instantaneous response on a moderately loaded system, and many systems operate extremely reliably. Multi-user systems software is abundant and encompasses large sets of useful tools and operating systems that provide primitive operations for putting the tools together. File systems are sophisticated and are often coupled to database management systems. Small multi-user systems will follow the current large systems in most of these respects, providing the sophisticated capabilities users have come to expect with significantly more cost-effective computing.

Any multi-user system must incorporate a large virtual memory. Current personal computer applications have 256k to 512k bytes of physical memory available. Users expect virtual memory of at least this size on a multi-user computer system. Minimum virtual memory for many next generation microprocessor based systems will be 4M to 8M bytes/user. In multi-user systems, the total virtual memory will easily exceed the system's physical memory. To prevent thrashing (ie, excessive swaps between main memory and peripheral storage) from creating a performance bottleneck, and to allow large resident portions of the operating system, more than 1M byte of physical memory will also be required. The operating system must efficiently implement swapping.

Users must be prevented from destroying the operating system or from interfering with one another, but the protection system must not be so rigid that users cannot interact with one another. Such a prohibition prevents the use of services such as computer mail and terminal intercom.

In a multi-user system, each user expects to have a large virtual address space, much of which is devoted to private code and data.

Obviously, to support multiple users requires multitasking. In addition to providing multiprogramming, many successful systems provide general multitasking, which allows users to execute parallel tasks. This facility often permits a more natural program structure, simplifying software development. A general multitasking facility can be used to compose standard software tools for specialized applications.

The principal factor in determining user productivity in an interactive multi-user system is response time.[1] To guarantee acceptable response time, the central processing unit (CPU) must sustain high bandwidth execution rates. It must process data quickly, including decimal and floating point data. It must also support efficient interaction between users and the operating system for input/output (I/O). Further, to minimize the effects of switching between users, the processor must be able to perform rapid context switches.

All of these requirements place a heavy demand on CPU architecture. Luckily, microprocessor architectures have met these demands. Eight-bit and early 16-bit microprocessors had severe limitations that hindered their use in multi-user systems. Performance was inadequate, physical memory was small (less than 65k bytes), instruction sets were limited, and protection and virtual memory were not provided at all. Recent advances in microprocessor technology allow current microprocessor based systems to have virtual memory, multitasking, and sophisticated protection, while nearly matching the performance of high end minicomputers.

A microprocessor solution

One leader among these microprocessors is the iAPX 286. The 286 is implemented as a high performance metal oxide semiconductor component containing about 130,000 active devices in a 68-pin Joint Electron Device Engineering Council (JEDEC) package. The processor architecture provides a protected, virtual address extension to the 8086 instruction set family. This chip is compatible with the 8086 and executes nearly all 8086 application software without modification.

Like the 8086, the 286 address space is byte addressable and segmented. The 286 provides 1G byte of virtual address space that contains as many as 16,383 segments of up to 64k bytes each. This virtual address space maps to a physical address space of 16M bytes. Address translation is based on descriptors, and its scheme is similar in some respects to the methods used in the multiplexed information and computing service (MULTICS) and on the Digital Equipment Corp PDP-11/45.[2,3] These similarities include the use of segment descriptors and privilege levels for memory management and protection.

The processor provides protection for each process as well as address translation. Protection is based on descriptor access control and visibility control, through the use of local and global descriptor tables and separate privilege levels. Using separate descriptor tables for each task gives each a private interval address space and intertask isolation. Four privilege levels provide additional access control within a task. Protection and address translation hardware are also provided on the CPU for maximum performance.

The 286 instruction set extends 8086 instructions, yet shares many features with the 8086. The 286 uses all the 8086 instructions and addressing modes and even includes the 8086 register set. The full instruction set contains over 300 separate instructions. The base set includes operations for general data manipulation, string processing, binary coded decimal arithmetic, and floating point numerics. Instructions added to the 8086 base set support protection, multitasking, operating system calls, and common high level language functions.

Operating on its demultiplexed bus at 8 MHz, the 286 executes at approximately 1.2 MIPS. (A 10-MHz version is also available, with proportionally higher performance.) User calls to the operating system can be performed in less than 12.6 μs, and tasks can be switched in less than 23 μs. Overall system performance exceeds that of a typical high end minicomputer.

Virtual addressing

In a multi-user system, each user expects to have a large virtual address space, much of which is devoted to private code and data. The part of the address space that contains the operating system must be common to all users; yet another part of the address space can be shared among multiple users. For practical reasons, the virtual address space occupied by all the users is too large to fit into physical memory, so swapping must be employed.

The 286 provides direct onchip support for virtual addressing through its descriptor based addressing. Typed descriptors are used to translate virtual addresses to physical addresses, to control address space access, and to assist in implementing virtual memory. The usual descriptor type references a segment; other descriptor types reference special data types used by the operating system.

All active descriptors are stored in either a local descriptor table (LDT) or a global descriptor table (GDT). Each table can contain up to 8192 eight-byte descriptors. Local descriptor tables are allocated on a per-task basis. There can be as many LDTs in a system as there are tasks, which allows each user to have a private virtual address space of 0.5G byte. The GDT is system wide and contains descriptors for segments and other data structures that the operating system needs, as well as for

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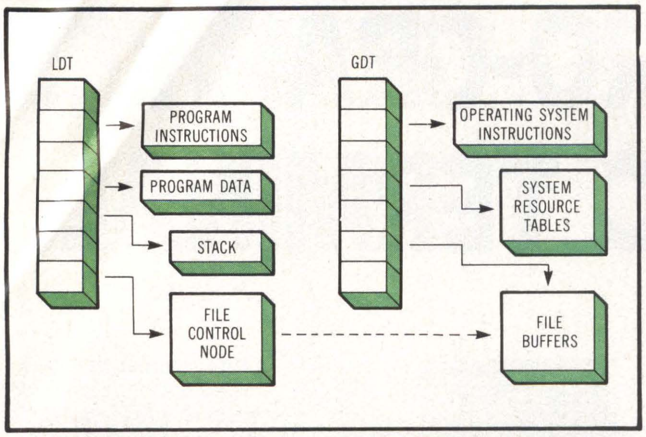

Fig 1 Descriptor based virtual addressing scheme uses descriptor tables for local and global segment access. Task specific and system-wide data structures can be referenced.

all the LDTs. Because all tasks access the same GDT, users can share a common operating system.

Fig 1 illustrates the use of descriptor tables to reference local and global structures. Descriptors that reside in the LDT or GDT are provided for instructions and data that the program accesses directly, and for special segments used by the operating system. These special segments can include auxiliary tables, file control nodes, buffers, tasks, and other system data structures.

The 32-bit virtual address consists of a 16-bit selector and a 16-bit offset. As shown in Fig 2, 14 bits of the 16-bit selector are used to select 1 of 15,384 descriptors (2 bits are used for access control); 1 of the 14 bits is used to pick from one of the two tables. When the descriptor is a segment descriptor, the 16-bit segment offset is added to a 24-bit physical address base contained in the descriptor. The processor performs a limit check and access checks based on other bits in the descriptor. Sixteen descriptor bits are reserved for a segment limit; additional bits indicate access restrictions, including execute only, read only, and no access. Out-of-range memory accesses and incorrect access types are trapped in the operating system.

Virtual memory

Other descriptor bits support virtual memory. The 286 assists segment swapping by including 2 bits in each segment descriptor specifically for use in a swapping system—the present and accessed bits. The present bit is set to 1 when a segment is resident and cleared when a segment is not present (usually indicating that it is in backing storage). Accessing a segment through a descriptor with

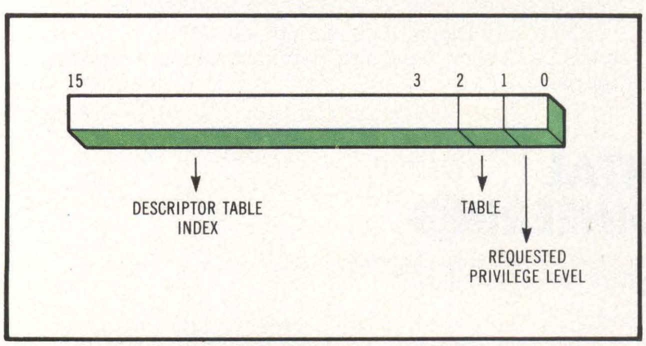

Fig 2 Selector part of virtual address. Selector specifies which table (and descriptor within table) will generate physical address. Privilege level is also indicated.

present indicator 0 results in a segment fault, which causes an interrupt to the operating system. When a segment fault occurs, the operating system restores the segment from backing storage. Only a small number of restartable instructions can cause this fault to occur. To the task referencing it, the segment appears to be in memory.

The accessed bit is set to 1 whenever a segment is read, written, or executed from. It is initialized to 0 by the operating system when the segment is initially loaded and when it is restored by the swapping system. A swapping system can also use the accessed bit to age segments, which is done to determine which segment to remove when the swapping system needs memory. Usually, one of the oldest segments is removed from residency. Other factors are taken into account such as whether a copy of the segment needs to be written out. To age a segment, a user can periodically check the accessed bit of each descriptor in the system. If the accessed bit is a set, the descriptor is marked with a time stamp and the accessed bit is cleared. Periodic aging can be performed by a separate operating system task or each nth time a swap occurs.

Once the swapping system determines which segment to remove, it then determines whether to copy the segment to backing storage. If the segment has not been accessed since last copied back, or if it is a read only or executable segment for which a copy already exists in secondary storage, the segment can be removed from residency without making a copy. When a segment is finally removed, the accessed and present bits in its descriptor are zeroed. Its location on secondary storage is then recorded in an auxiliary table.

Enforcing protection

The processor enforces protection through a combination of descriptor access control and the use of four privilege states. Interuser (intertask) isolation is achieved by giving each user a separate LDT; the processor forces local accesses through descriptors in the user's LDT. The operating system controls what goes into the LDT, which prevents a user from creating a descriptor for something in another user's address space (ie, the user cannot access his LDT as data and change a segment's base address). To access new segments, files, and tasks, a user program must call the operating system. Security software in the operating system verifies ownership before it gives or updates a descriptor.

Since each task and the operating system share a common virtual address space, privilege levels are employed to isolate user applications or tasks from the operating system. A task executes at one of four privilege levels. Each descriptor contains a descriptor privilege level (DPL) that the processor compares with a task's privilege level to determine access validity. For data segment accesses, the DPL must be numerically as large or larger than the task privilege level, or a protection fault is raised. For ordinary instruction segments, the two levels must match. These restrictions allow more access rights to the operating system than are directly available to user programs.

A task can switch privilege levels by calling a procedure in a segment with a lower DPL, and can then execute in a more privileged state. These interlevel calls must be made indirectly through a special descriptor,

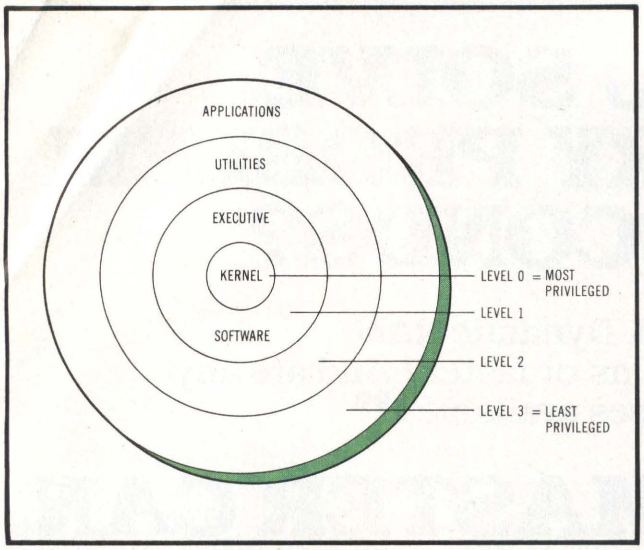

Fig 3 Privilege levels available in iAPX 286 protection model. Note use of small kernel to eliminate excessive operating system access of data base.

named a call gate, and can only be made to a lower or equal level. Calls through these gates allow user programs to communicate with the operating system. At the instruction level, an interlevel call is indistinguishable from an ordinary call. To guarantee system integrity, each of the four privilege levels has its own stack, which prevents a user program from causing stack overflow in the operating system. Also, if a user program accidentally overwrites its stack pointer with an invalid value, there is no harm done to the operating system, which has its own stack pointer(s).

The privilege level facility allows the operating system to decentralize data structures that belong to specific user programs. If a user's LDT contains a descriptor for a file control node, it can be made invisible to user software, yet visible to the operating system, by marking the descriptor with a low numbered DPL. User software normally runs a privilege level 3, the highest numbered level, stopping access to the file node. This prevents the user from overwriting information in the node that results in a fatal file error. The I/O system, executing at a lower privilege level, is able to read and write information from the file node.

Operating system structure

Using four privilege levels, rather than the conventional two (user/supervisor), allows a more structured operating system. This approach has been successful in operating systems for the Digital Equipment Corp VAX, which uses a similar structure.[4] As illustrated in Fig 3, system software can be allocated to levels 0 through 2, with user software in level 3. Level 0 is used for the operating system kernel; level 1 for executive services, including I/O and memory management; and level 2 for applications services, including high level language runtime support, utilities, and command processors. Separating applications services from the user level allows these services to call system routines unavailable to the user. For example, a runtime system can invoke asynchronous I/O operations inaccessible to the application program, accommodating different privileges.

Separating the kernel from the rest of the executive allows isolation of protection and security enforcement in a small part of the operating system. A common problem in large multi-user systems is that too many operating system modules can reference the protection data base. This leads to protection holes in the system.[5] Secure, modern systems use a small kernel with very primitive operations.[6] This kernel executes in a more privileged state than the rest of the operating system, eliminating these compromises.

Multitasking

Modern systems use multitasking for more than just multijobbing; most allow each user to execute multiple tasks in parallel. Users can create foreground and background partitions for interactive and batch tasks. In addition, users can combine cooperating tasks to perform a single service. This facility, as exemplified in UNIX, allows the combination of simple standard tools to produce a customized service.[7] Multitasking is often used in the operating system itself. Device servers, files, loaders, swappers, garbage collectors, and others conveniently execute as tasks.

For this degree of multitasking, task hierarchies are required and are achieved through some form of task forking.[8] Task destruction, to eliminate completed tasks, is also required. To support task cooperation, tasks in a hierarchy must be able to communicate with each other. Using files, tasks need to share special data structures such as mailboxes and events, or ordinary data segments. To software, a task is an image of the processor executing a sequence of instructions on a set of data. The task's execution context includes the processor state such as registers, condition codes, other state flags, data, and instructions. The 286 recognizes a special segment, called a task state segment, that contains this execution context (Fig 4). The task state segment contains a copy of the processor registers, four task stacks, a selector that links the task to an invoking task or to an interrupted task, and a selector for an LDT.

Processor hardware uses the task state segment when it performs task switches. The task state segment has a special descriptor that prevents the segment from being used in ordinary operations. To access or manipulate the contents of a task state segment, the operating system must alias the segment with another descriptor that references the memory locations containing the segment.

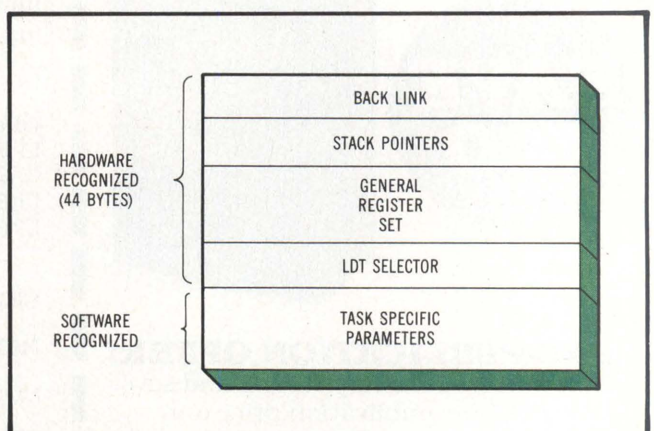

Fig 4 Task state segment used to support multitasking. Hardware and software specifics of each task are kept together, facilitating task operation.

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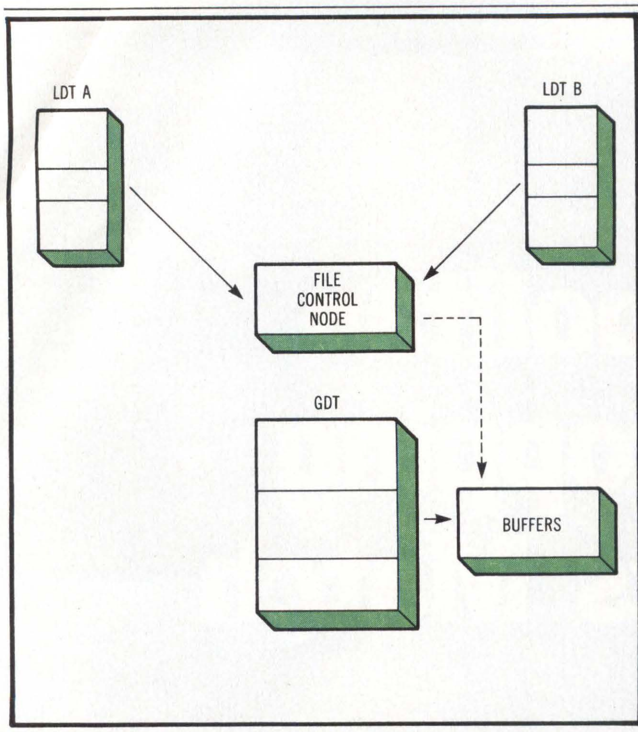

Fig 5 Task sharing of data structures. File control node allows tasks to access common file control blocks.

Software can extend the task state to contain additional data. Task specific parameters can be stored in the remainder of the segment beyond the 44 bytes used by the processor hardware. This area can contain task priority, time slice, elapsed execution time, and memory limits, among other things. Both the hardware and software task representations can be kept together to facilitate task creation and destruction.

Task segments, like other segments, can be created and destroyed, which requires other actions as well. To create a task, the operating system must create a valid initial state. To do this, it must provide the task with valid stacks for each privilege level used in the system. The task's LDT must be created and initialized, and several registers must be allocated. The software part of the task segment must also be initialized. Additional software actions, such as linking the task to its parent and placing the task on a scheduling queue, are also required. Destroying a task requires freeing the LDT and destroying the task segment. Software actions are required to destroy offspring tasks, to free segments allocated to the task, and to remove the task from scheduling queues. In all these operations, software uses the task state segment.

To fork a new task, an existing task creates a new task, links between itself and the new task, then places the new task on a scheduling queue where it will be dispatched in turn. Task dispatching is easier with instructions that cause a new task to start execution. Extended to allow their targets to be task segments, the 8086 "call" and "jump" instructions cause the target task to start or resume execution. In addition to these synchronous task innovations, interrupts can also cause task dispatching, allowing device servers to be structured as tasks.

Tasks can interact through files. This interaction allows two users to communicate and supports an inter-terminal intercom. It also provides a facility for a parallel user task to pass information and to synchronize. In a 286 system, files can be shared via a file control block. Each task's LDT contains an identical descriptor for the single control block, as shown in Fig 5. The operating system makes copies of the descriptor when the common file is created.

Performance

The 286 architecture contains a number of features designed to meet the performance requirements of multi-user systems. Overhead in supporting virtual memory, operating system calls, and task switching have been minimized. Since these are major components of operating system overhead in a multi-user system, the net effect is higher performance.

Processors normally incur a major penalty when they translate virtual addresses to physical addresses. Usually, memory reference time is extended 25% or longer if address translation buffers do not contain the necessary translation information. Additional overhead is incurred when users are switched so that translation maps can be switched. One solution is to maintain multiple translation maps, but this often restricts the number of tasks a user can create.

By keeping an active set of four segment descriptors in onchip registers, the 286 overcomes this problem. These registers contain descriptors for the current instruction, data, and stack segment, plus an extra descriptor for general use. To maintain protection, the programmer-visible part of the register contains only the descriptor's selector. With all the descriptor information onchip, base address translation can be performed parallel to other processor activities. In addition, bus bandwidth is not used to perform translation. When a task switch is performed, only these four registers need to be switched, which lowers the overhead for task switches. Overall, less than 5% overhead is associated with the processor's virtual addressing mechanism.

Microprocessors must support large virtual memories and multimegabyte applications for each user.

Operating system calls are another potential source of overhead. By making operating system calls a special case of ordinary procedure calls, the 286 reduces this overhead. Because system calls must be made through call gates that point to specific procedures, hardware performs the necessary bounds checks and address translation required to ensure that the call is directed to the correct routine. Hardware also performs the stack switching and parameter copying that is often left to software in conventional systems. As a result, a user program can call an operating system routine, passing it two parameters in fewer than 100 clocks, or 12.5 μs at 8 MHz.

In a multi-user, multitasking system, task switching must be very efficient. The 286 processor requires little assistance from software to switch tasks. Control transfers referencing the task state segment cause processor microcode to save and restore the processor execution context in a single operation. A task switch can be performed in about 180 processor clocks (22.5 μs at

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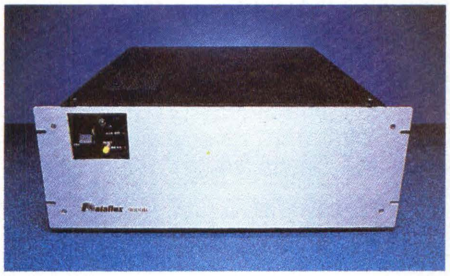

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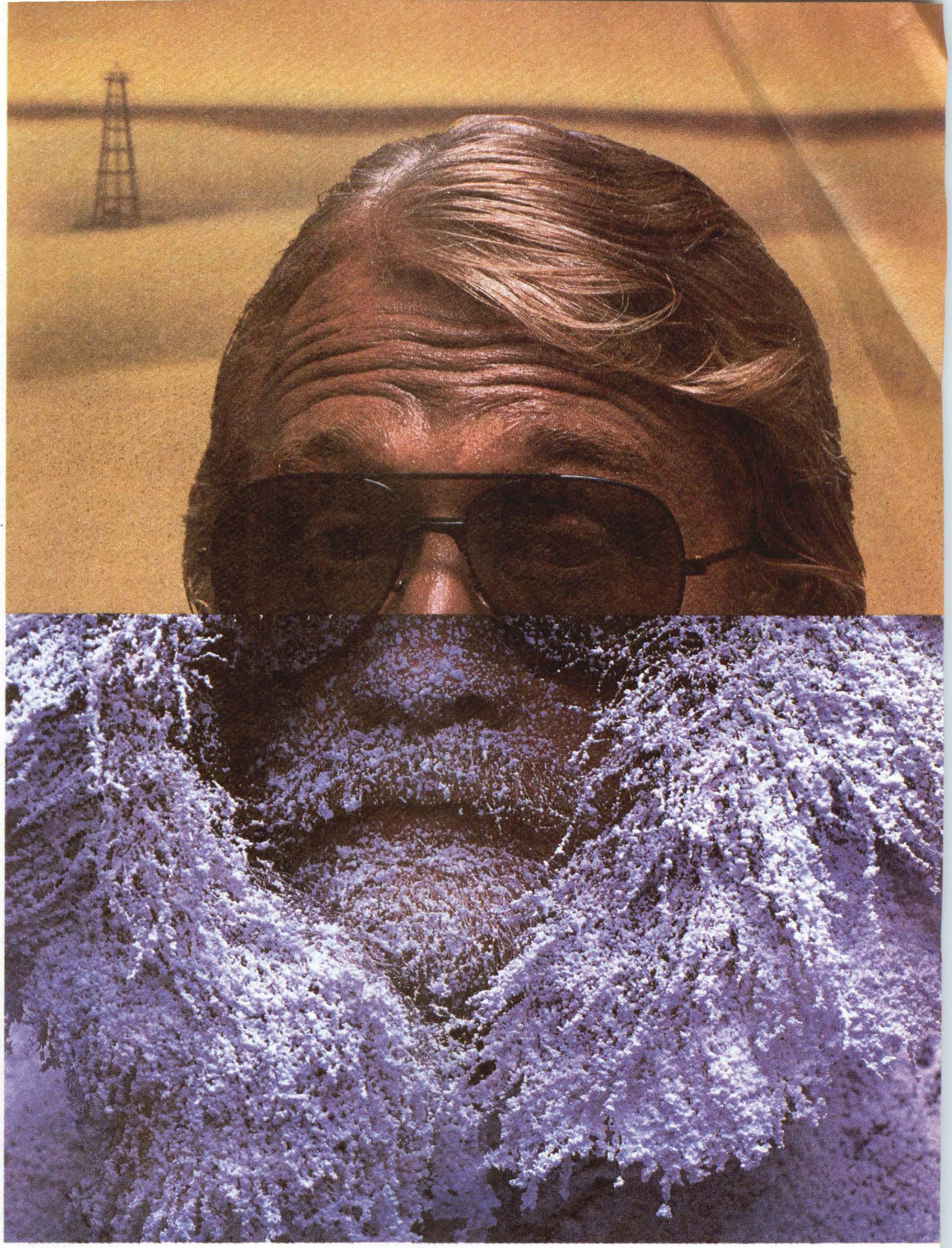

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8 MHz). This attention to system performance in the 286 architecture allows it to execute applications six times faster than the standard 8086 in multi-user systems. In addition to general performance improvements gained through microarchitecture sophistication, the 286 executes single instructions that replace long operating system software instruction sequences.

As technology drives down the cost of multi-user computers, microprocessor architecture advances to support the sophisticated operating systems that run on them. New processors, like the iAPX 286, provide architectural support for these systems. Future microprocessors must support large virtual memories and multimegabyte applications for each user. Protection strategies for such systems demand reliable and secure operating systems. Multitasking primitives, integrated into the instruction sets, will sustain efficient implementation of operating systems such as UNIX. Much of this support can be included in a single processor component. Computer systems based on these processors will compete with minicomputers many times their cost.

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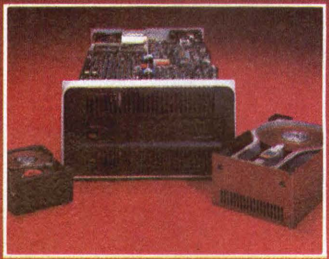

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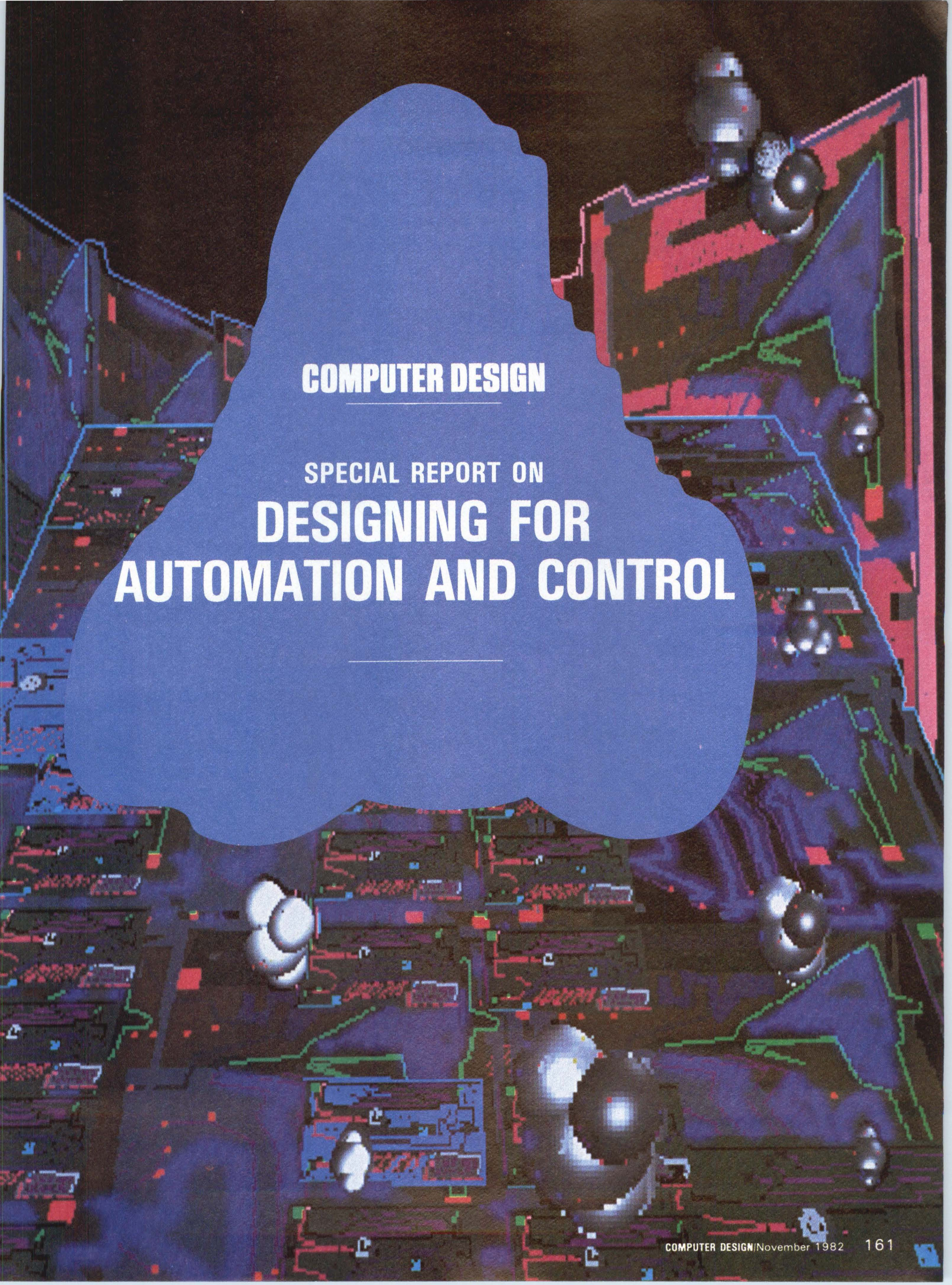

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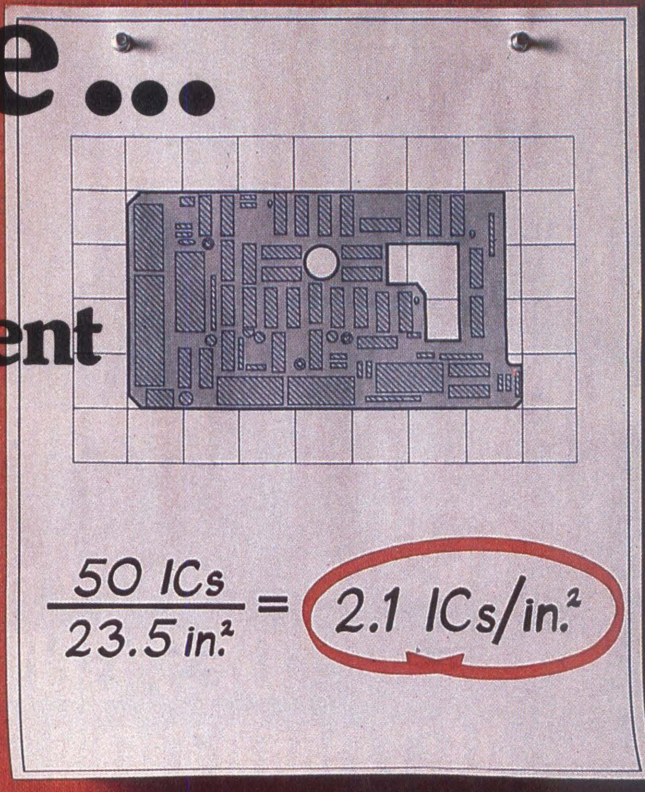

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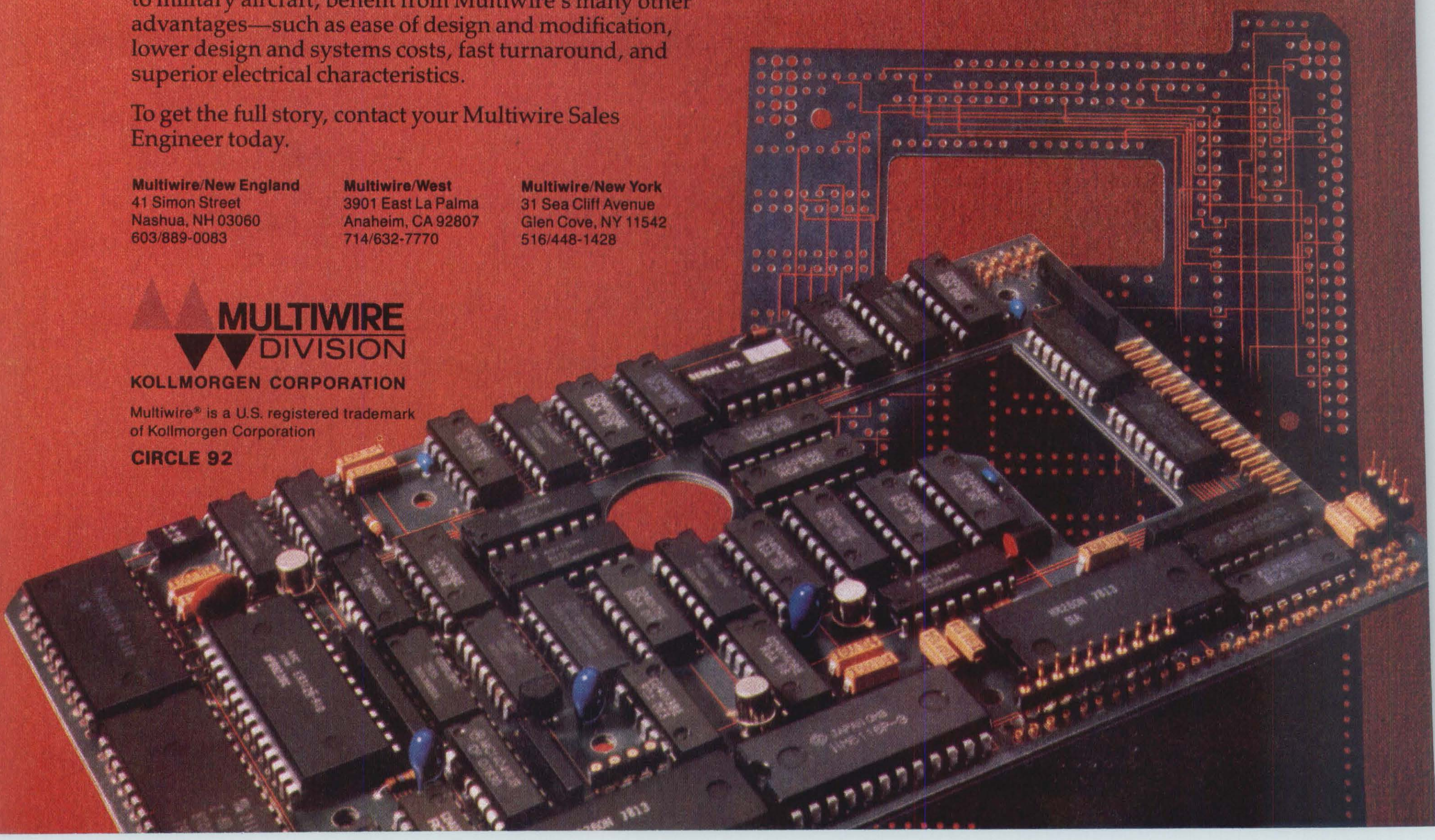
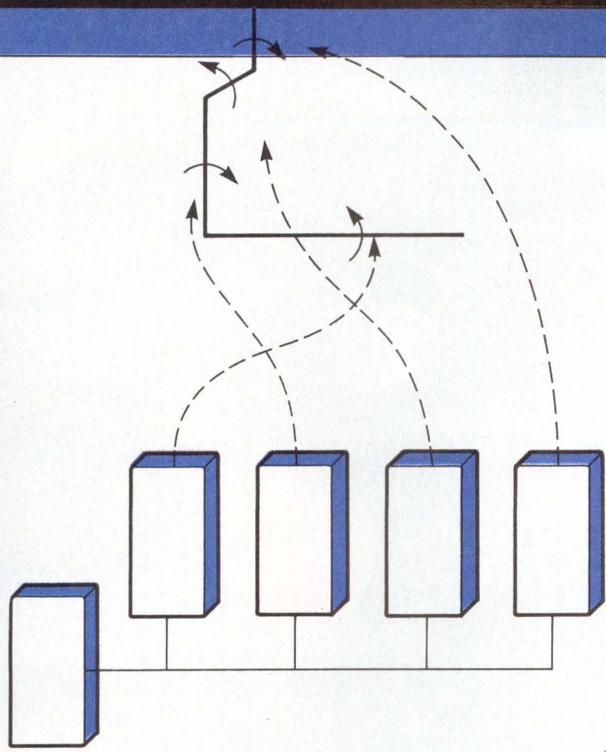
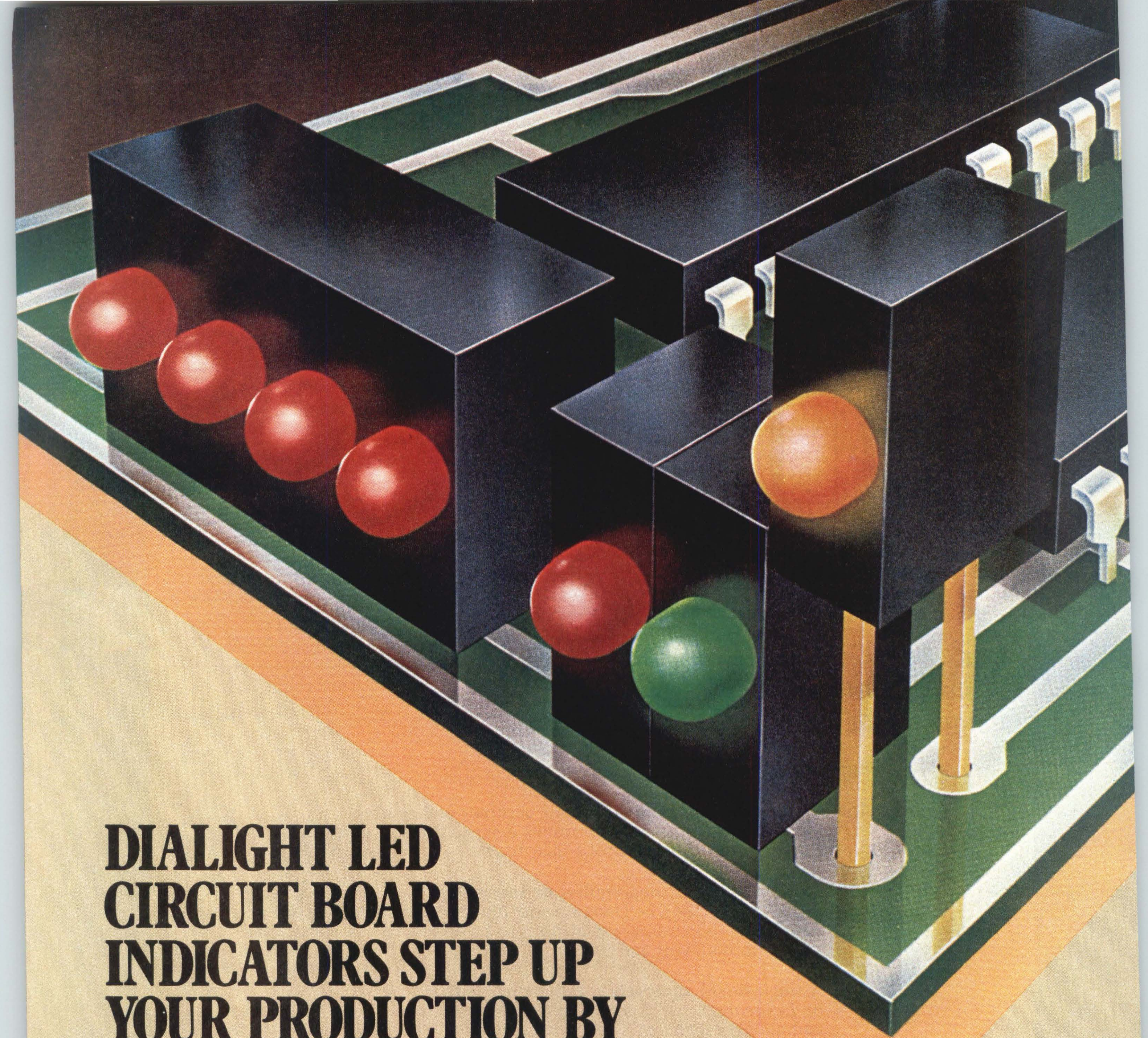
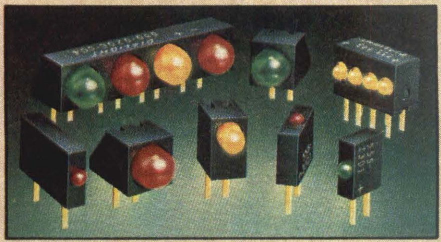




169 *A master processor supplies angle, loading, and stress data to individual axis processors in a multi-axis robotic system. Both master and axis processors are powerful single-chip microcomputers with large amounts of onchip I/O.*

Special report on designing for automation and control





INTRODUCTION

Automation, from its beginning, has included three basic elements: sensors that permit measurement, actuators that provide control, and a decision maker that directs the control action. In very early systems, those elements were a person's eyes, hands, and brain.

Analog controllers were limited in that only individual loops could be controlled. Though there was reasonably consistent control action within loops, the interaction among loops had to be provided by an operator. Starting in the sixties, with the growth of digital computer control, it became possible to control many loops simultaneously and interactively. The control process could be maintained in its entirety rather than as a set of independent parts.

Despite these developments, digital automation and control is just beginning to strongly influence industry. The reasons are not simply stated. Though certainly not the sole component, one major factor that delayed acceptance of automation and its growth as a major industry is the human element—the failure to maintain feasible man/machine interface. This reluctance to accept automation is based on both a fear of the unknown and a fear that jobs would be eliminated.

An even greater concern of decision makers, however, has been a seeming lack of justification for financing automation. Because of their inherent depreciation complex concerning capital equipment, those decision makers could not recognize the financial advantages of replacing existing pneumatic or hydraulic systems (the ubiquitous ROI syndrome). Fostered by the U.S. Government, the depreciation allowance, as it applies to some older capital equipment intensive industries, has encouraged many to maintain a status quo—to hold the line with old, low efficiency equipment while foreign competitors automated and practically put them out of business. Witness the automobile industry and many of the public utilities.

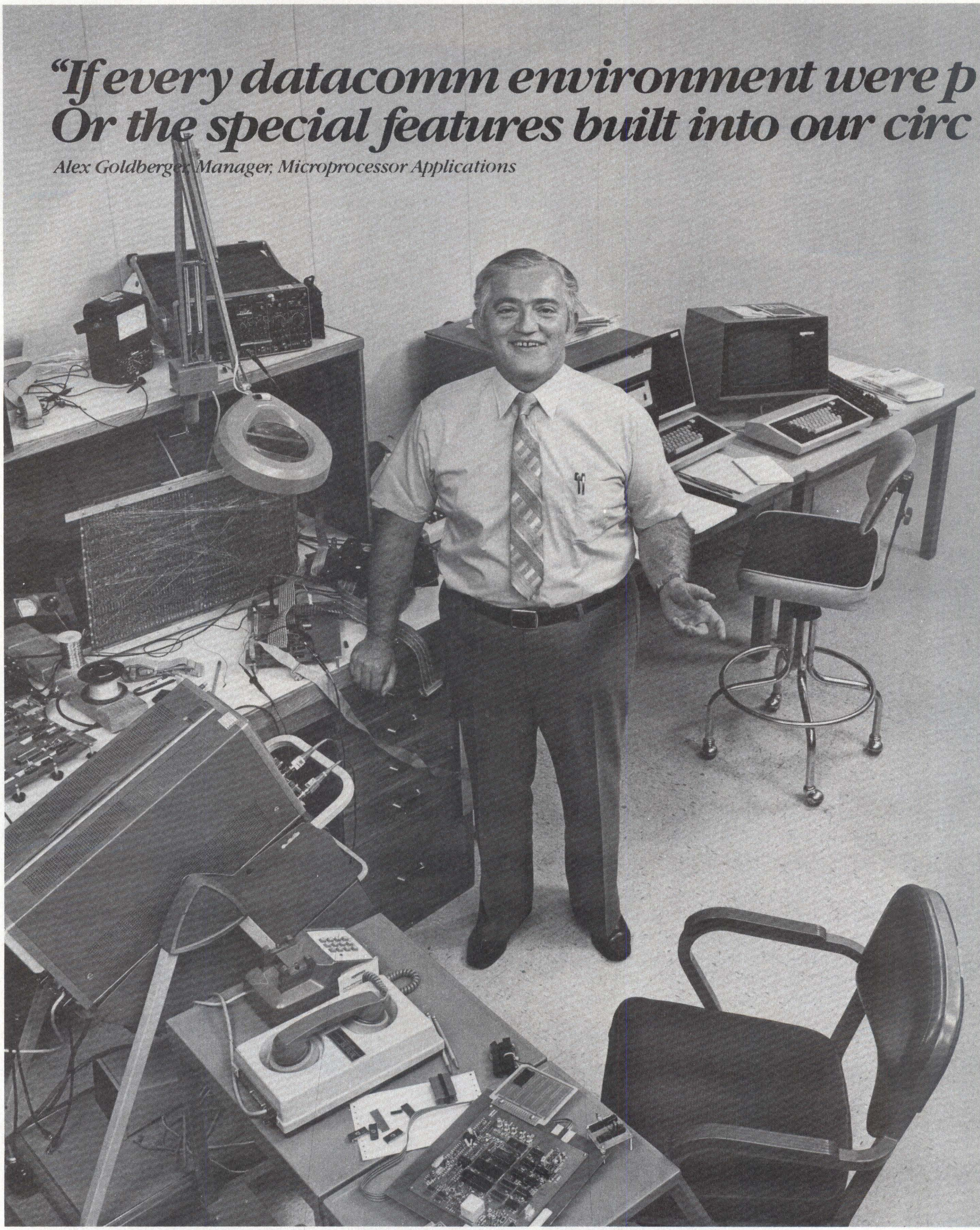
Ramifications of recent growth and its purpose involve the human element more than ever. At a time when unemployment is so high, what will be the effect of greater automation? Certainly, automation reduces the number of persons needed to carry out a manufacturing process. But it also improves productivity and quality—and does not necessarily increase unemployment. Experts predict that in the long run, automation will reduce unemployment as new jobs develop and improve the working environment. For example, robots have now been accepted, whether or not reluctantly, for use as welders or in dangerous or unpleasant situations.

Currently, automation and control is one of the fastest growing domains of the computer industry. This includes more than robots—although they are certainly today's glamour element. Both artificial vision and artificial intelligence, probably best known for their association with robotics, meet the needs for applications far beyond that relatively small area.

Although removed from many production steps, the human is still present and in strength. A control engineer must design and install the control system, a programmer must write application programs, and management must agree to automate. The three basic elements—sensors, actuators, and decision—are still there. And the fourth element—the human—is more important than ever. Without intending to be Pollyannaish, my feeling is that those experts who predict long term benefits of automation are correct.

Syd Shapiro

Syd Shapiro
Managing Editor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Cyclic Redundancy Check. This is a more sophisticated system of block checking. CRC divides the data stream with a complex polynomial to obtain the Block Check Character. As with LRC, this character is compared to the BCC generated by the receiver.

In addition to checking for data errors, protocols have other techniques for detecting sequence errors. These include alternating acknowledgements and block sequencing. You'll find them—along with VRC, LRC and CRC—discussed in depth in Signetics' Datacomm Information Kit #4.

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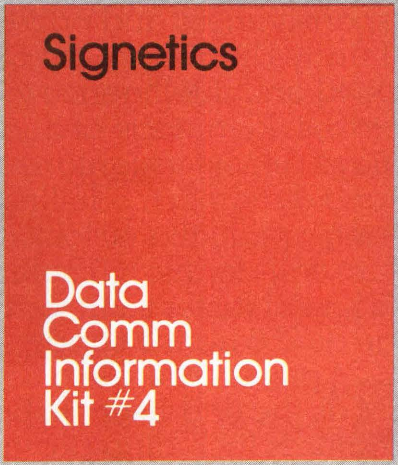

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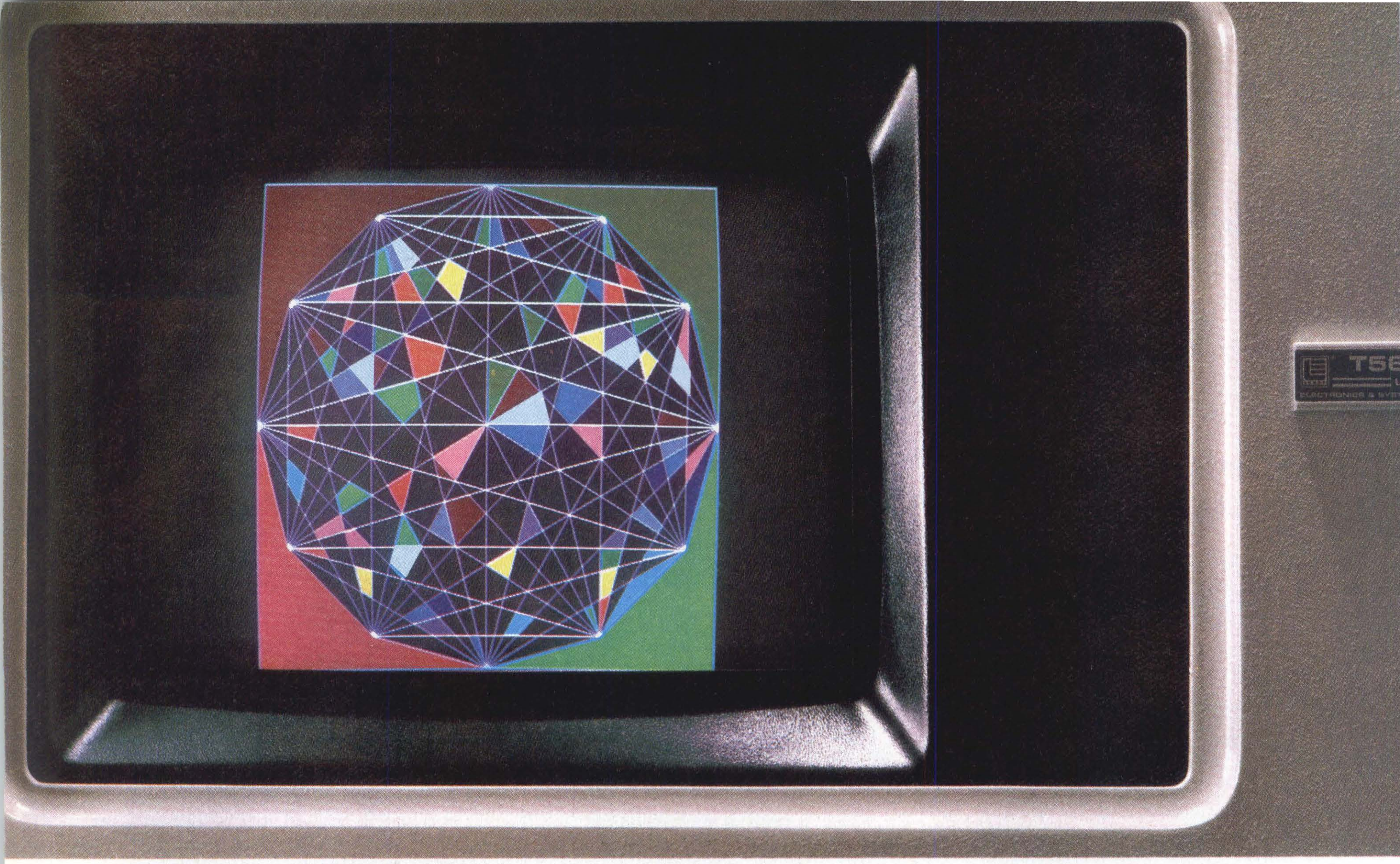

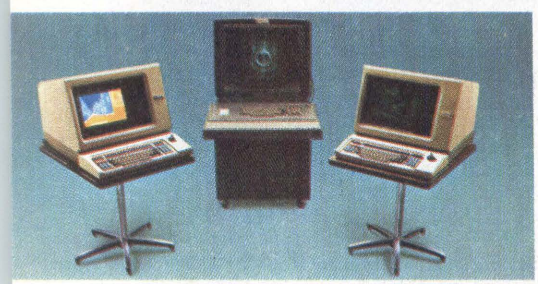

MULTIPROCESSING IMPROVES ROBOTIC ACCURACY AND CONTROL

Modern robots demand a microcontroller per axis for the brains to fully exploit their brawn.

by Parveen Gupta

In the last few years, both the complexity and use of industrial robots have greatly increased. Robots are now used in many manufacturing industries including automotive, castings/foundry, heavy and light manufacturing, electronics/electrical machinery, and aerospace. Though robotics applications vary, their technical characteristics and problems are similar. The next robotic generation will meet these challenges by distributing the robot's processing functions using multiple processors.

A typical robot provides several axes of movement. Current control loop technology per axis is analog with digital set point input from the microprocessor [Fig 1(a)]. For the next generation of robots, positional accuracy must be improved. This goal can be accomplished by making the digital control computer an integral part of the control loop, as shown in Fig 1(b). When this is done, the computer algorithm can compensate for load variation, robot member warping under load, mechanical tolerance, and stress.

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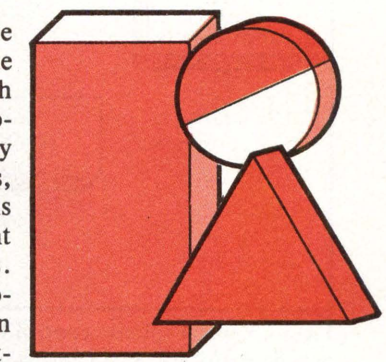
Master control processor



Many robots require multiprocessors with one processor per axis, each controlled by a master processor (Fig 2). Since they serve different purposes, the master control and axis processors require different architectural attributes. Many master control processor problems exist in robot development. Software is probably the toughest and most expensive of these problems and can entail up to one-half the robot's cost. Processing for some of the more advanced features requested by robot users will increase this software burden. Hardware design is not as great a problem because most manufacturers simply assemble their boards and card cages in the robot's control cabinet.

Another problem with robots is the large memory their master processors require. (Memory requirements in excess of 64k bytes will be very common in the future.) In addition, the master control processor must have built-in features for multiprocessor support—both tightly coupled parallel multiprocessing and loosely coupled serial configurations. Noise is also a major problem with industrial robots. Microprocessors that can survive the industrial environment with security and reliability will be most successful. Another drawback is the significant microprocessor computing ability required. For robots, multiply and divide are probably the most important of these instructions. All robotic

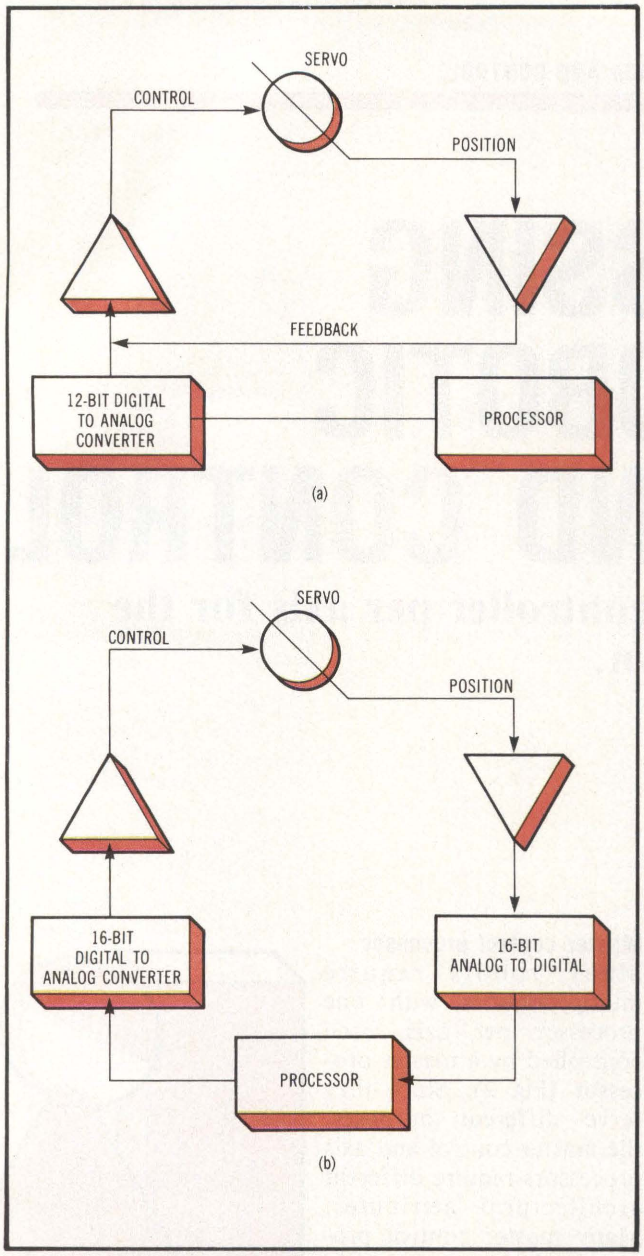


Fig 1 Typical robotic control loop yields positional accuracy of 0.05″ (0.13 cm) (a). Digital control loop improves accuracy to 0.02″ (0.05 cm) or better (b).

problems identified here are addressed by the MK68000, a 16/32-bit state of the art very large scale integration microprocessor.

Software solutions

Debugging and maintenance are major software costs. For robotics applications, software problems are even greater due to low volumes with high software content. High level language implementation using structured programming techniques can help solve these problems. The 68000 microprocessor has several architectural features that efficiently implement high level languages. Pascal constructs and 68000 features and instructions are compared in Table 1.

The LINK and UNLK instructions automatically allocate and de-allocate space on the stack for local variables. A move multiple (MOVEM) instruction facilitates saving or restoring of the registers during procedure

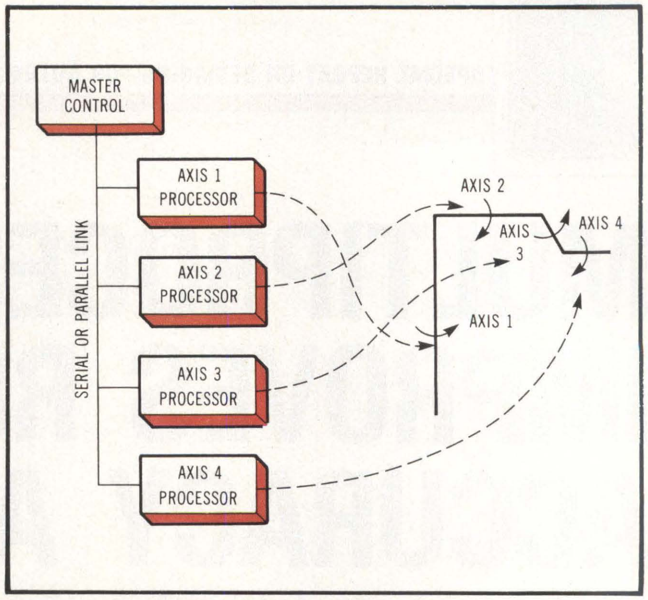


Fig 2 Multiprocessor robotic system with processor for each axis. Master processor supplies angular position and time frame, as well as loading and stress factor information to adjust algorithm for maximum accuracy.

calls. Only the registers that must be saved are put on the stack. MOVEM also guarantees that data pushed from a register will be pulled back into the same register. Few addressing mode restrictions mean that the compiler writer has the freedom necessary to generate an efficient code with minimal overhead. Memory to memory operations, coupled with the test condition, decrement, and branch instructions, and postincrement and predecrement addressing modes, extend the basic set of five data types—bits, binary coded decimal (BCD) digits, bytes, words, and long words—to include larger precision numbers, vectors, arrays, and complex data structures. The load effective address (LEA) instruction helps reduce execution time when repeated access to an individual element is required. By doing the address calculation once and saving the result in an address register, LEA allows the faster address register indirect to be used repeatedly. LEA and push effective address (PEA) also implement parameter passing. The 68000's multiple bit-shift capability, from 1 to 31 bits at a time, makes it easier to find data field areas.

TABLE 1

High Level Language Implementation

Pascal construct	68000
Procedure calls	Use stacks pointed to by address registers
Push parameters, address	MOVE, PEA
Call procedure	JUMP to subroutine
Establish local environment	LINK
Save and restore registers	MOVEM
Reestablish environment	UNLK
Return from procedure	RETURN
Restore stack	Add immediate instruction to stack pointer

For most processors, floating point software implementation suffers from either loss of precision in keeping a floating point number within a single register or from loss of execution speed in manipulating multiple registers for a single floating point number. The 32-bit 68000 registers alleviate this problem.

Regular instruction sets ease compiler implementation. The 68000's addressing modes allow any address registers to be used with a given addressing mode so that all registers are available to a compiler. The orthogonality of using data registers with respect to instructions reduces data register restrictions. Thus, the high level language implementer has a greater degree of flexibility in using data and address registers and selecting addressing modes.

These features help minimize software development costs. Also, almost all of the instructions operate on bytes, words, and double words; most instructions can use any addressing mode.

This microprocessor's uniform and regular structure simplifies writing in either assembly code or in a high level language. Special instructions to operate on byte, word, and double-word integers are not needed; a programmer needs to remember only one mnemonic for each instruction type. As a result, the 68000 has only 61 instruction mnemonics.

Debugging and maintenance

It usually takes longer to debug a program than to write it. The 68000 offers several hardware traps to indicate abnormal internal conditions that help to minimize debugging time. These are word access with odd address, unimplemented instruction, illegal instruction, illegal addressing mode, illegal memory access (bus error), overflow on divide (divide by zero), and overflow condition code (a separate instruction, TRAPV).

A CHK instruction is used for array-bound checking by verifying that

$$0 \leq \text{(register)} < \text{limit}$$

A trap occurs if the register contents are negative or greater than the limit. A trace mode allows the program to be tracked instruction by instruction during program debugging. After each instruction is executed, a trap is made to a tracing routine. This trace mode is available to the programmer when the processor is in either the supervisor or user modes. With an external memory manager such as the 68451, both user and supervisory states can guard against error by protecting selected memory areas.

Additional features

A 24-bit address bus on the 68000 allows direct addressing of 16M bytes of memory without segmentation. Function code lines extend this direct addressing capability to 64M bytes. Each 68000 family bus master, including the processor, provides a function code during each bus cycle to indicate which address space to use. The address bus then specifies a location within this address space for the current bus cycle operation.

Master or control processors in high end robots require large programs, many in excess of 64k bytes. The large addressing capability of the 68000, together with the memory management system, lead to efficient and secure robot central processors.

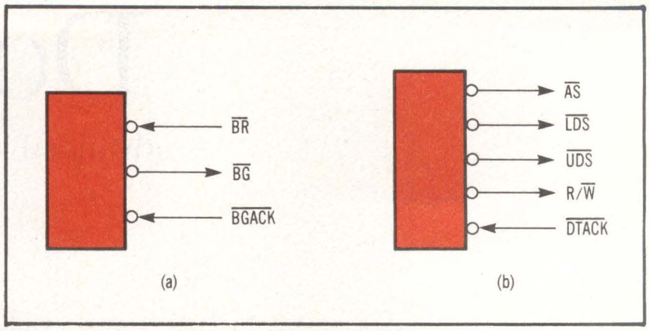


Fig 3 68000 bus arbitration lines. Only one device controls bus at one time (a). Asynchronous bus control lines require proper handshake (DTACK) from external devices (b).

Another key feature of future robots is multiprocessing, which the 68000 is equipped to support. An arbitration control bus allows hardware interlock [Fig 3(a)]. When more than one device needs the bus, only one device is allowed to control it, and all others are locked out. Locking out other resources via software can also be accomplished with the test and set (TAS) instruction, which allows the user to define a semaphore bit in memory. A memory byte is then read or tested. Condition codes are set appropriately, and the high order bit of the tested byte is set. Since the memory location is tested, then written to, a read-modify-write instruction is needed. To protect data transfers from occurring in the middle of it, the instruction is indivisible. Address strobe asserted throughout the cycle provides this indivisibility. The TAS instruction promotes processor communication in a multiprocessor system. An area of memory can be associated with a resource. If one of the processors needs to access that resource, it will test and set the memory byte first. It should be determined whether the memory location associated with that resource has been previously tested and set to find out if that resource is available. In this way, multiple processors can be synchronized in their access to shared resources.

An asynchronous bus provided by the 68000 also enhances multiprocessor system designs. [See Fig 3(b).] The data transfer acknowledge (DTACK) signal is an input indicating that the data transfer is complete. In a multiple processor system, the processors do not have to be contained in a small area; in a loosely coupled system, different processors can be separated. This is a valuable arrangement in a robotics environment. In a synchronous system, errors may occur as data are delayed traveling down long lines. In the asynchronous system, data transmission delays do not cause problems because synchronization is not required.

Supervisor and user operating modes enhance multiprocessor system capability. All exception processing is done in the supervisor mode, where the processor can perform special operations prohibited in the user mode. User software can operate on a specific task of a particular processor; supervisor software can contain system software to operate on system abnormalities. This supervisor software can reside in a shared memory area (reentrant code), or it can have duplicate software for the supervisor routines.

Most robots operate in noisy industrial environments, which can easily cause halts and errors in digital systems. The 68000 can work in such an environment, and

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TABLE 2

Instruction Execution Times

Instruction type	Clock periods	Execution time*
Move register to register	3	0.5
Add register to register (binary or BCD)	3	0.5
Move memory to register	6	1.0
Add register to memory	9	1.5
Multiply (16 x 16)	21	3.5
Divide (32/16)	24	4.0
Move multiple (save or restore all registers)	55	9.2

*with 6-MHz clock (μs)

its features provide system security and reliability. These are achieved by automatic detection of exceptions in the system that can be generated internally or externally.

Axis processor in robotic applications

Each axis processor in a robot takes commands from the host processor and performs control and command functions on an axis. To be effective in a robot system, the axis processor should be a powerful single-chip microcomputer with as much onchip input/output (I/O) as possible. It should also have a powerful instruction set including fast 16-bit multiply and divide. The axis processor should provide excellent multiprocessing and distributed processing support and should easily interface to the master control processor. A single-chip microcomputer, the MK68200, works well as an axis processor for modern robot systems. The 68200's 16-bit central processing unit includes three system registers, eight data registers, and six address registers in an arrangement modeled after the 68000 register set. It directly addresses a 64k-byte memory space. Memory is byte addressable, but most transfers occur 16 bits at a time for increased performance over 8-bit microcomputers. This processor supports nine addressing modes, including four register indirect modes and a special I/O port mode that allows most instructions to access the most often referenced I/O data with one word.

The 68200 instruction set is designed for regularity and ease of programming. In addition, instructions are encoded to minimize code space. Most instructions execute in either three or six clock periods (a clock period is equal to 167 ns with a 6-MHz clock). Table 2 lists the instruction execution times for various instruction types. The 68200 has rapid bit manipulation instructions that operate on both registers and memory. Available bit operations include bit set, clear, test, change, and exchange; all bit operations perform a bit test as well. Since each instruction is indivisible, the necessary test and set function is provided for semaphore implementation.

I/O architecture. To minimize the chip count in an axis processor, the 68200 has an extensive repertoire of I/O functions including timers, a serial channel, parallel I/O, an interrupt controller, automatic bus arbitration, and an onchip direct memory access (DMA) controller. A total of 40 of the 48 pins are used for I/O, and most pins can perform multiple programmable functions. The 68200 also contains 4k bytes of onchip read only memory (ROM) and 256 bytes of onchip random access memory (RAM).

Timers. Three full 16-bit timers are onchip. Timer A provides interval, event, pulse width, and period measurement modes. Timer B provides interval, retriggerable 1-shot, and nonretriggerable 1-shot modes. Timer C is a simple interval timer that can also be used as a baud rate generator for the serial channel. Timers A and B also have associated input and output pins.

Serial channel. A full-duplex universal synchronous/asynchronous receiver/transmitter (USART) included on the 68200 has double buffering on both transmit and receive. The asynchronous mode supports bit rates up to 250k bps, and the byte synchronous mode operates up to 1M bps. Internal or external clocks can be used. In addition to the typical USART functions, the serial channel can transmit and receive in several wake-up modes by appending a wake-up bit to each data word. This wake-up bit differentiates normal data words and special address modes. The receiver can be programmed to receive only address words, or address words with a specific data value. Hence, the processor can be interrupted only when it receives its particular address and can then change mode to receive the following data words. Wake-up capability is especially useful when several 68200s are interconnected on one serial link.

Interrupt controller. The interrupt controller on the 68200 provides rapid service of up to 16 interrupt sources, each with a unique internal vector. A nonmaskable interrupt is also provided. All other sources share an interrupt enable bit in the processor status register. Also, there is a separate interrupt enable bit for each source. This feature allows selective enabling of particular interrupts, including the ability to choose any desired priority scheme with minimal software overhead. In fact, 15 levels of nested priority can be programmed.

Parallel I/O. Two 16-bit ports, port 0 and port 1, can be used for parallel I/O. If individual bits are desired, each of the 32 bits can be separately defined as input or output. Bits can be grouped to provide exact data widths. Port 0 can operate under the control of external handshaking signals. Eight- or 16-bit sections of port 0 can be individually controlled as input, output, or bidirectional I/O with two pairs of ready and strobe signals.

External bus. When it is necessary to expand the onchip complement of RAM, ROM, or I/O, or when DMA access to external memory space is desired, the 68200 can be put in an external bus mode. Single-chip I/O or external bus selection is done with the mode pin at reset time. Port 0 and a portion of port 1 are reconfigured to provide the necessary bus functions. Fig 4 illustrates the external bus logical pinout. When the 68200 makes an offchip reference, the bus request and bus grant signal operation is automatic and invisible to the programmer. Any offchip reference causes the processor's control section to issue a bus request and to enter the idle state until the bus is granted. This process occurs for each offchip reference, and the bus is relinquished whenever the processor does not immediately need to go offchip. Successive offchip references occur without relinquishing the bus. In situations where the processor needs to retain constant bus ownership, the bus lock bit of port 15 can be used. Setting this bit enables the processor to maintain bus ownership until the bit is cleared. The bus lock bit can be used when it is desirable to keep

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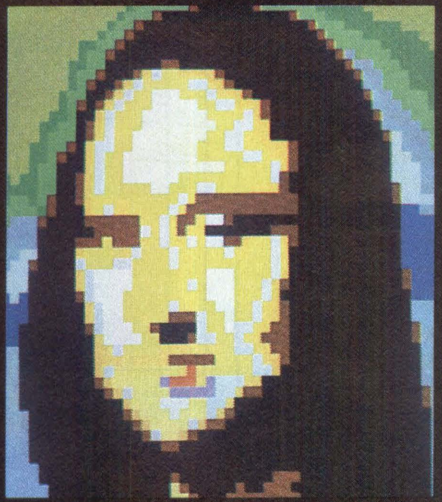

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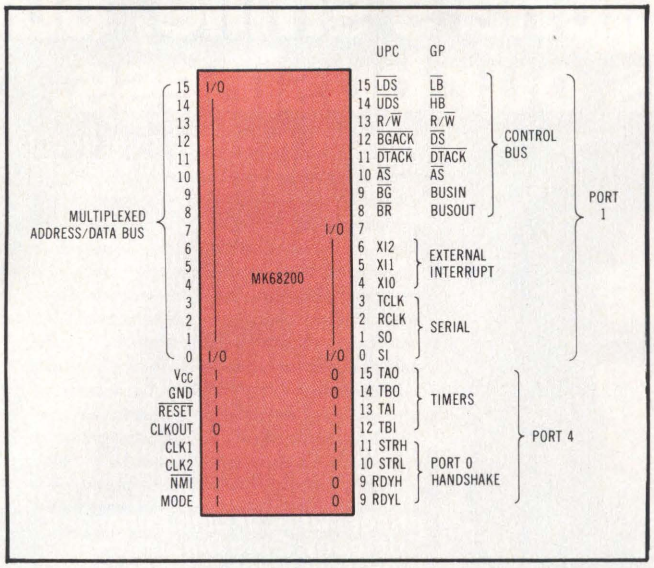

Fig 4 **68200 external bus logical pinout. 68200 has extensive repertoire of I/O functions.**

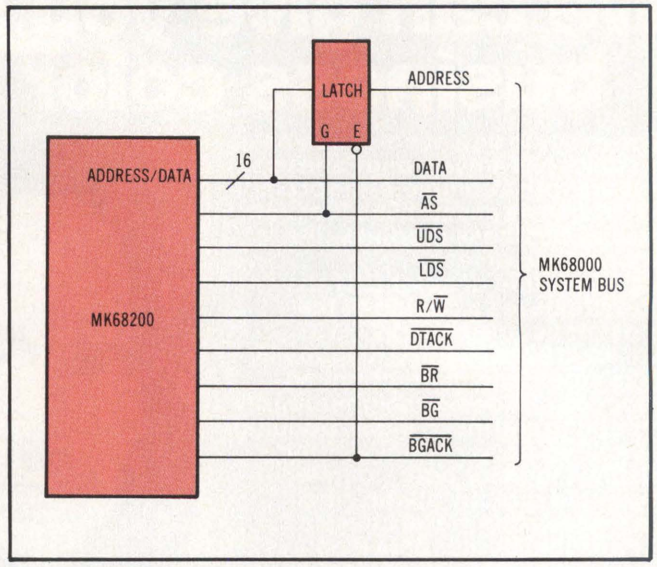

Fig 5 **68200 connects to 68000 system bus via external address latch. All control signals can be connected directly.**

the bus for the duration of the block transfer. MOVEM instructions can hold the bus continuously for the data transfer portion of their execution.

There are at least three ways to make DMA block transfers onto the external bus with the 68200. If a traditional MOVE instruction is used in a loop, each single word or transferred byte will make a bus acquisition. This operation, often referred to as cycle stealing, places a minimal load on the external bus. The use of MOVEM instructions allows continuous transfer of up to 13 words or 16 bytes to or from the onchip registers in sequential memory cycles. This method is usually the fastest since it requires fewer fetches and memory cycles. A final approach is to transfer an entire block of data with a single bus acquisition using the bus lock feature just described. This option is useful if the other system processors do not need the bus during the DMA transfers.

Interface. The 68200 easily connects to a 68000 system bus with the addition of an external address latch shown in Fig 5. The 68000 can transfer the initial command information to the 68200 in several ways. One way is when a specific command area in common memory is predetermined. The 68000 interrupts the 68200 when the command information is available. In another instance, the 68200 powers-up in the nonexpanded mode. The 68000 supplies the pointer for the command information via port 0. The 68200 then reads the command pointer, switches to expanded mode, and reads the command information from common memory in DMA fashion. Another method is when the 68200 powers-up in the nonexpanded mode and transfers the entire command block via port 0, one word at a time. It then switches to expanded mode for DMA data transfers.

When using an external bus, the 68200 can be configured several different ways. Designers can select whether or not to retain the onchip ROM and whether the chip should be a bus slave or a master. In all cases, the onchip RAM and I/O ports are retained. The 68200 mode pin chooses the desired expansion capability on power-up and reset and is usually strapped to a fixed value in a system. The pin has three states that signify either full, partial, or no expansion. With partial expansion, onchip ROM, RAM, and ports are retained, and a portion of the memory space is allocated to the external bus. Although the mode pin selects the configuration on reset, the chip may be dynamically reconfigured with software.

Next-generation robots will demand higher performance from very large scale integration microprocessors. The 68000 is a well-suited master control processor for robotics applications because of its clean architecture, powerful instruction set for high level language implementation, generous exception handling for security and reliability, large memory addressing range, and multiprocessing features.

As an axis processor, the 68200 is well suited for robotics because of its 16-bit CPU, powerful instruction set, 4k bytes of ROM, 256 bytes of RAM, three multifunction 16-bit timers, serial port with full-function wake-up feature, automatic bus arbitration, onchip DMA controller, and onchip interrupt control. It also interfaces easily to the 68000 either serially or tightly coupled through the parallel system bus. In addition, the 68200 does not tie up the 68000 system bus during data transfers with the I/O device, or during internal processing. These two processors provide effective multiprocessor solutions to the challenge of robotics.

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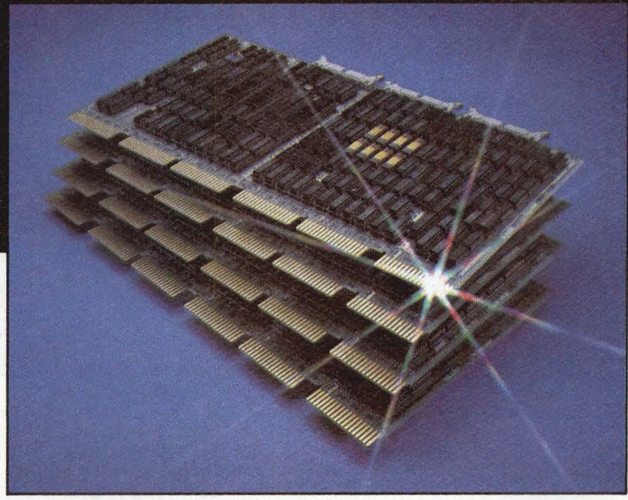

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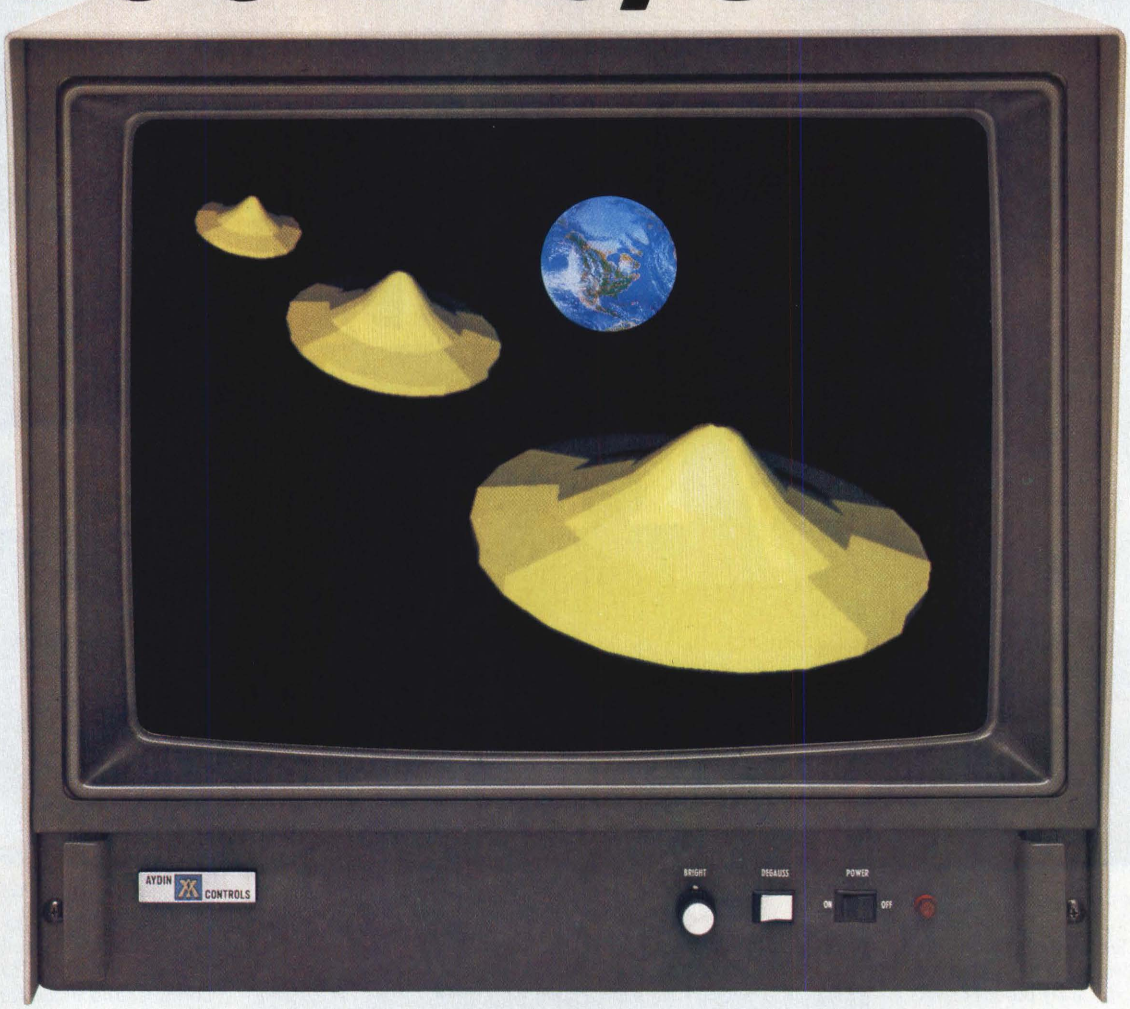

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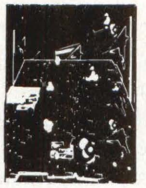

SCULPT CUSTOM MICROCONTROLLERS ON SINGLE CHIPS

Designs using the alterable microcomputer as a basis allow full custom applications to be developed at a substantial savings in both cost and time.

by Naveen J. Tangri

Microcomputers are replacing small and medium scale integration logic in specific applications, just as integrated circuits replaced discrete transistors more than a decade ago. Complete microcomputer systems can give primitive application systems impressive intelligence inexpensively. In particular, microcomputers have greatly affected control and automation. Since most control and automation systems deal with physical (mechanical) processes, the relatively slow processing speeds of microcomputers usually suffice. Moreover, control and automation applications are diverse enough to require microcomputer systems that incorporate functions unavailable on a single chip.

Of greater significance, though, are the performance benefits, low power consumption, reliability, repeatability, and versatility that microcomputers provide. While a wider variety of standard microcomputers and peripherals is available, it is unlikely that a standard microcomputer system will meet specific application needs. This is also true of standard single-chip microcomputers and microcontrollers. Until recently, it has not been economically feasible to incorporate custom microcomputers into high performance, medium volume control systems for automation, instrumentation, and telecommunications.

Incorporating semicustom or full-custom products into designs gives system designers the exact required functions for specific applications. By definition, the custom alternative eliminates compromises inherent in standard products. Custom designs also give customers a wide variety of fabrication processes to choose from. Thus, custom products lower unit costs and improve system performance.

High frontend design costs and long development times have limited the growth of the custom marketplace. Development costs and times are directly related to product complexity; a fully custom designed, low end microcomputer can cost several million dollars over several years. As a result, these microcomputers are only cost effective in large volumes. Fig 1 shows typical cost/volume curves for custom large scale integration (LSI).

The need for an innovative design philosophy that offers low cost, quick turnaround, high performance custom microcomputers, resulted in the concept of an alterable microcomputer unit (AMU). An alterable microcomputer is designed for easy customization. This concept treats every architectural element of a custom microcomputer as a modular cell, each with a few versatile and well-defined interface signals. Thus, an AMU has a modular central processing unit (CPU) and functional cells for input/output (I/O), peripherals, and memory—all topologically designed for easy integration

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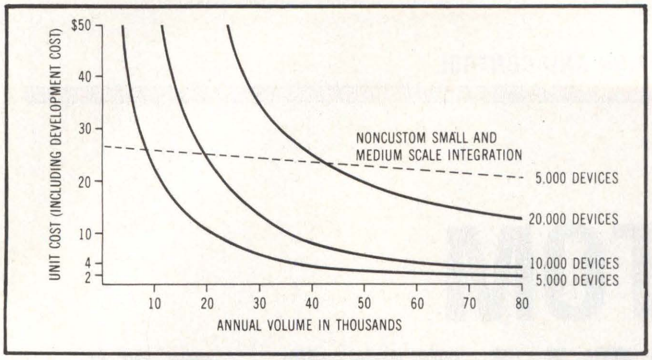

Fig 1 Cost/volume relationships for custom LSI of varying complexity. Software development costs are not included.

on a single silicon chip. The strength of the AMU concept is the substantial savings in design cost and time it offers. This results from integrating predesigned and tested modules, including the CPU, into a custom microcomputer.

The AMU is not a standard product, but the building block of an easily customized high performance microcomputer. A high performance CPU, with instruction set and architecture that cannot be customized, is the core of an AMU. This core processor is linked to the target system through highly functional peripheral and I/O modules. The entire AMU is fabricated in dual-polysilicon complementary metal oxide semiconductor (CMOS) technology. The core processor selected has a control oriented 16-bit architecture. Predesigned modules, including the core processor, are available separately. American Microsystems Inc's (AMI) alterable microcomputer family of standard products offers the S99C91, a CMOS 16-bit microprocessor, which is the core processor of an AMU; the S99C923, a CMOS device containing 16 general purpose I/O ports (GPIO); and the S99C922, which contains the GPIO together with a versatile counter/timer subsystem. The prototyping device for an AMU design-in is the AMU/PR, which contains the core processor integrated with 2k bytes of read only memory (ROM) and 128 bytes of random access memory (RAM). A special feature of this device is that it contains pinout functions useful in prototyping application systems.

Application system requirements

It is instructive to examine the considerations involved in designing application systems that require a high performance microcomputer and peripherals. In many applications, microcomputers with a 4-bit word length lack precision and speed. Double-precision operation also entails a speed penalty. Though 8-bit microcomputers provide a much higher performance/price ratio than 4-bit machines, applications requiring significant computational ability, including multiply and divide, demand a 16-bit microcomputer to overcome the disadvantages of performing double-precision operations with an 8-bit word length.

Though power consumption and space requirements may not be critical in industrial control and automation systems, they are of prime importance for portable applications. In any application, power consumption and physical size affect overall cost. High power dissipation ratings inflate system costs by requiring cooling systems and higher capacity power supplies. Higher power dissipation also increases chip temperatures, and adversely affects reliability.

Combining more functions onto fewer chips results in savings in logic, packaging, and board area. Secondary savings result from reduced power consumption due to the elimination of interchip interface logic, such as bus drivers and receivers. Therefore, there is a growing trend toward implementations involving a minimal chip count.

Popular microprocessors introduced over the past few years have evolved into families. Vendors have attempted to maintain upward compatible software within these families. At the same time, there is a trend toward introducing microcomputer family components suitable for specific applications. For example, several single-chip microcomputers are available with the same CPU, but with varying amounts of RAM and ROM. Similar variations are available with regard to I/O ports and counter/timer subsystems.

The custom solution

Using a custom chip for the application prevents most of the inefficiencies inherent in application systems designed using standard components. Custom microcomputers offer a much higher performance/price ratio than equivalent noncustom solutions. Moreover, it is feasible to place entire board level systems on a single chip, thus opening new target markets for the application system. For example, a handheld computer (HHC) requires the integration of an entire microcomputer system, complete with CPU, RAM, ROM, keyboard interface, and display drivers, within tight physical and electrical constraints. The HHC would have been impossible without a custom microcomputer. Other examples include handheld intelligent games, fully electronic cameras, and portable video equipment. In the automobile, custom microcomputers have replaced board level control and automation systems.

The possibility of incorporating major modifications and improvements that are impossible at the board level is another advantage of the custom solution. The incorporation of additional functions in a board level system entails the costs of silicon, assembly, printed circuit board area, connectors and sockets—estimated at more than $3/component.[1] In a custom chip, the only significant costs of incorporating additional functions result from increased silicon area and, possibly, increased pinouts. Thus, additional functions and enhancements can be incorporated into custom microcomputers at more than an order of magnitude less cost than if they are made at the board level.

Custom microcomputers have yet another advantage over standard microcomputer systems. As with most custom products, custom microcomputers can be manufactured in any fabrication process that suits the customer's needs for reduced cost or high performance. A wide variety of fabrication processes is available to the custom microcomputer designer, although bipolar, N-channel MOS, and CMOS are the dominant process technologies. The process technology for a custom microcomputer is determined by three major criteria: cost, performance, and operating environment.

A custom microcomputer's cost is determined by its design and fabrication. Since custom microcomputers have a long production lifetime and large production

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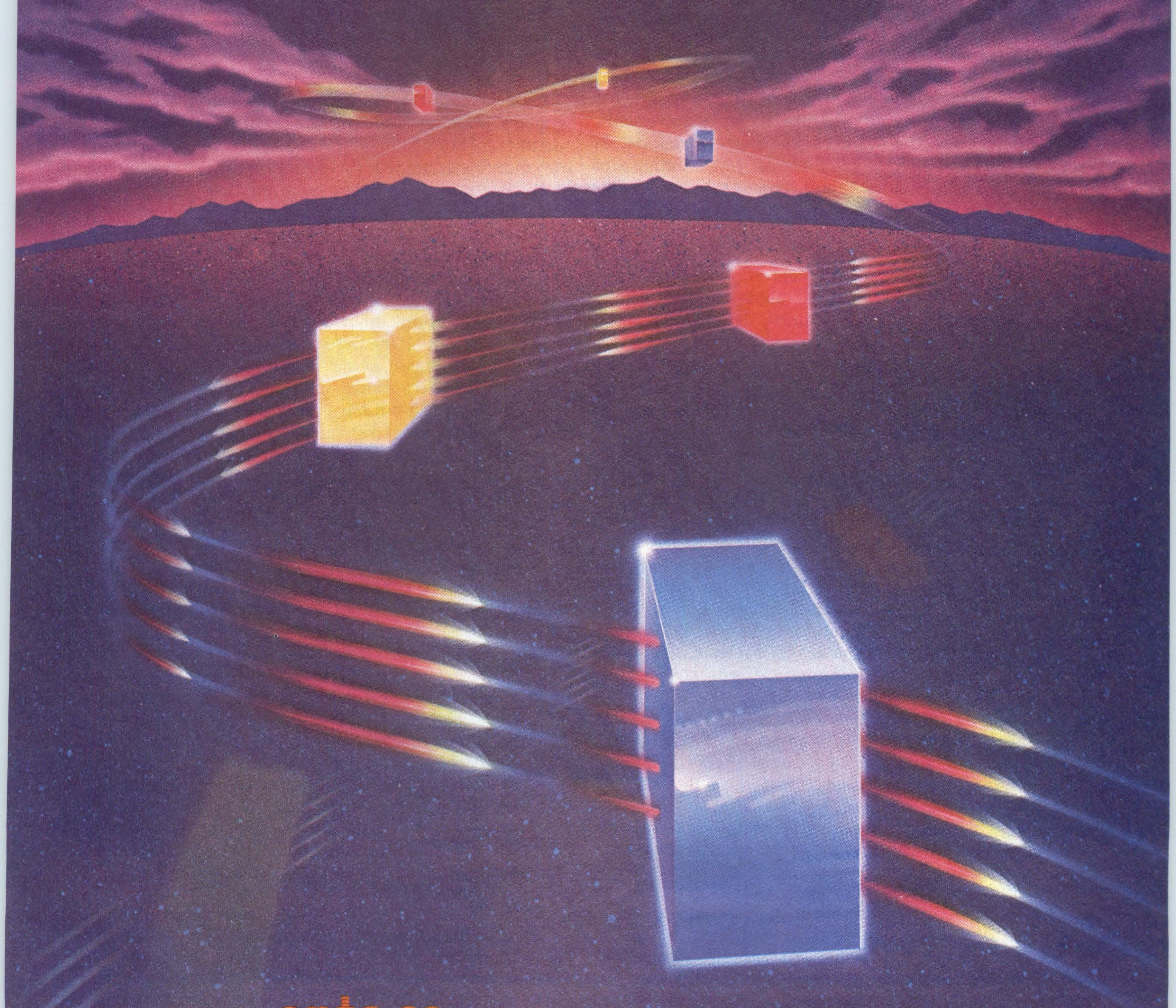

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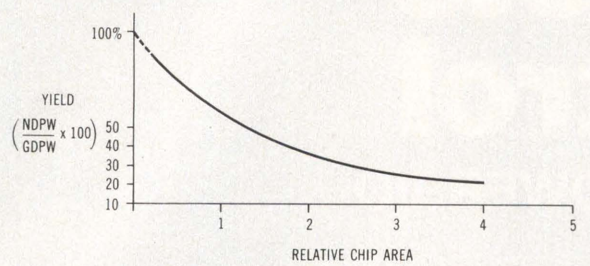

Fig 2 Net die per wafer (NDPW) is divided by gross die per wafer (GDPW), then multiplied by 100 to determine relationship between net die yield and die size.

volumes, fabrication costs are the major cost of a unit. Design costs are virtually recovered for a product that has matured. Fabrication costs largely depend on the net die per wafer (NDPW) product yield. Although the NDPW figure is inversely proportional to the silicon area of the device (Fig 2), it is affected by several secondary factors as well. NDPW yield is susceptible to design and fabrication complexity and packaging requirements. Chip defect density, which is the average number of defects/chip, is directly proportional to the active area of the chip occupied by circuit elements, as well as the area defect density. The last quantity is a function of the process technology and depends on minimum tolerances.[2] Using process technologies that reduce active chip area can improve yield and lower cost. For example, the CMOS process used for fabricating alterable microcomputer family devices uses two polysilicon layers to boost gate density.

At least two major performance factors affect fabrication process choice—speed and power consumption. The highest typical operating speed of the custom microcomputer determines the maximum allowable propagation delay/gate. Depending on the intended application, power dissipation/gate can also be a limiting factor. One important effect is the correlation between device operating speed and power consumption. Switching circuits in general, including microprocessors, tend to consume greater power at higher switching frequencies.

System designers have the freedom to specify different analog functional modules on a single-chip custom microcomputer. Therefore, the selected fabrication process must be capable of implementing those analog functions with a minimum of process step overheads. The dual-polysilicon CMOS process used for AMUs allows analog functional modules, including switched-capacitor filters, to be fabricated on an AMU chip.

Control and automation systems often function in extreme environments. In aerospace and military applications, including satellites, electronic systems are subject to high temperatures as well as alpha particle and ionizing radiation. Industrial automation systems also must withstand considerable electrical noise. Thus, suitability of different process technologies to the intended operating environment must be considered in process selection. For example, although integrated injection logic (I^2L) and CMOS processes are comparable in device density and speed power product, I^2L is preferred in high temperature and high radiation environments.

Custom microcomputer architectural elements

Most custom microcomputers are designed with fairly standard von Neuman architectures. A custom microcomputer has a CPU, memory, interface, and I/O peripherals as architectural elements. One major difference in design philosophy between standard and custom microcomputers is that, while the former serves a broader application spectrum with its wider range of features, a custom microcomputer must be an optimal design that satisfies all requirements for the specific application. Three major factors must be considered in the design of a custom CPU: word length of the CPU, its instruction set, and the bus structure for memory and I/O.

Address and data word lengths. Address word length of the CPU is determined by the maximum amount of memory it is required to directly address. Most 8-bit standard microcomputers have an address word length of 16 bits and thus can directly address 64k words (bytes). This is not necessarily the case for a custom microcomputer, however.

Typical control, automation, and data acquisition systems require sampling rates of a few hundred samples/s. For a standalone dedicated controller that is not multiprogrammed, the execution time of the longest path of control algorithm program flow must be less than or equal to the sampling period. Assuming a typical average instruction execution cycle time of 4 μs, with a sampling rate of 200 Hz, the maximum length of one path of the control algorithm is $(1/200) \times [1/(4 \times 10^{-6})] = 1250$ instructions. At an average of 2 bytes/instruction, this translates to a memory access space of about 2500 bytes for the longest program flowpath. Of course, some memory is also required for storing vectors, constants, and tables. Since typical control algorithms do not have more than a few full-length program flowpaths, the memory space required for dedicated microcontrollers is often less than 64k bytes.

This example shows that the maximum address space required by a microcontroller is a function of the sampling rate required by the application, its instruction execution time, its object code density, memory requirements for data table storage, and the number of distinct execution paths contained in the control algorithm. Address word length depends on the maximum required addressable memory space.

A CPU's data word length is primarily determined by the type of data it must process with precision. An 8-bit data word is suitable for handling alphanumeric characters, as well as for representing analog quantities without loss of precision. A 4-bit data word reduces the silicon area required for the CPU, but also reduces processing speed in applications requiring considerable 8-bit (double-precision) computation. Although double-precision operation of silicon-efficient 4-bit microcomputers does have advantages under certain conditions, several subtle disadvantages are apparent.

An obvious disadvantage of double-precision data processing is loss of speed. A 4-bit microcomputer crunching data in double precision can be slower than an 8-bit microcomputer by more than a factor of two. This is true because the 4-bit machine takes twice the time required by an 8-bit CPU to move and process data, plus it expends considerable time in fetching the large

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number of instructions required for double-precision operations. Therefore, the conservative approach is to derate processing speed by a factor greater than two, depending on the architecture and instruction set, whenever a 4-bit microcomputer is required to perform double-precision operations.

Another disadvantage of double-precision computation is that it requires memory to store such software routines. Although some custom microcomputers may not have any memory onchip, this requirement is critical in single-chip microcomputers, where memory is at a premium. A more subtle disadvantage of double-precision operations is a higher energy consumption/executed function. One aspect often overlooked in standalone microcomputer system design is its energy efficiency, or the number of operations executed by the system per millijoule of consumed energy. It is difficult and perhaps unnecessary to compute the numerical energy efficiency figure for a given microcomputer system application, because it is a complex function of factors such as the microcomputer's architecture and instruction set, word length, process technology, clock frequency,[3] and the amount of system RAM and ROM. However, the most useful feature of the energy efficiency concept is that it allows system designers to compare various designs with regard to their effect on the overall energy efficiency of the system. Such evaluations can prove valuable in designing efficient microcomputer based systems for avionics, satellites, and portable applications where power is at a premium.

A case in point is the foregoing comparison of double-precision operations in a 4-bit microcomputer versus equivalent single-precision operations in an 8-bit CPU. Double-precision operations greatly reduce the energy efficiency of microcomputer systems because the microcomputer consumes additional power for the greater amount of time required to execute double-precision routines. Moreover, the additional amount of program memory required to store those routines constantly consumes power.

Addressing schemes and compact object code are more efficiently implemented when the address word length is an integral multiple of the data word length, because an instruction word can than contain source and/or destination address information with no wasted bits. That is why most 8-bit microprocessors have 16-bit address words. However, some standard 8-bit microcomputers have address word lengths that are less than 16 bits wide, perhaps due to pinout limitations and because a 64k-word address space is rarely required for dedicated controller applications.

Instruction set. Standard microcomputer instruction sets contain instructions for performing data transfer operations, arithmetic and logical operations, and control functions. Improvements in execution speed and memory efficiency for a custom microcomputer are possible if its instruction set is optimized for the specific application. Typical microcontroller applications require powerful bit-manipulation capabilities, whereas realtime process control microcomputer systems require number crunching ability. In the latter case, the microcomputer must have multiply and divide instructions for adequate performance. Customized AMUs are well suited to realtime control applications because the AMU

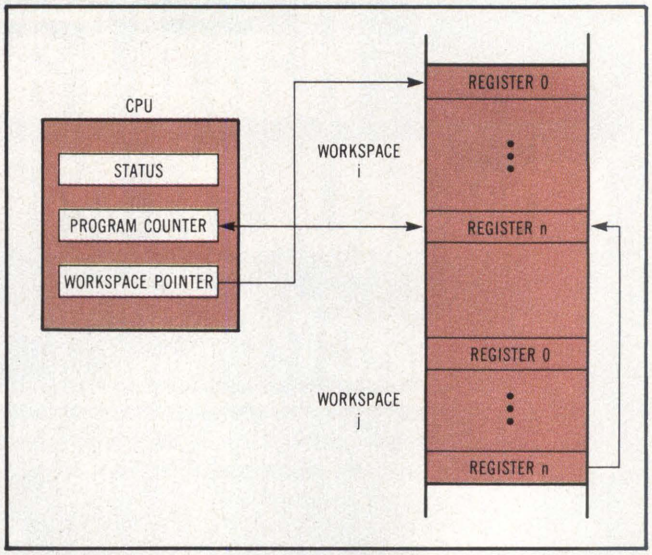

Fig 3 Memory to memory architecture employs multiple memory blocks as working register banks. Link vectors are stored in select workspace registers, eliminating need for stack.

contains hardware multiply and divide features, in addition to a flexible I/O interface.

Factors such as overall chip size, average instruction cycle time, and object code density determine the number of working registers in a custom microcomputer. Onchip working registers require expensive silicon real estate and also increase the complexity of CPU control logic. However, onchip registers have fast access times and greatly simplify the available addressing modes. Placing registers onchip improves object code density because source and destination addresses can be specified in far fewer bits than in an extended address for accessing an offchip register.

In a workspace register scheme, blocks of read/write memory are designated as workspaces and contain as many words each as there are working registers. An onchip register, the workspace pointer, holds the base address of a workspace. Fig 3 illustrates the workspace concept. The workspace register bank concept represents the best compromise between onchip and offchip registers. Placing all working registers offchip conserves onchip silicon. Object code density and addressing efficiency are maintained by using the workspace pointer, eliminating the need for extended addressing of source or destination registers in an instruction. Another advantage of such a memory to memory architecture is that a context switch requires saving and restoring a few onchip registers—the program counter, the workspace pointer, and the status register. Linking between context switches is done by saving link vectors in predesignated workspace registers (Fig 3). Another important advantage in the use of a memory to memory architecture is the flexibility with which the number of workspace registers can be adapted to a specific application. A change in workspace size requires only the addition or deletion of RAM.

Bus structure. A CPU's bus structure is reflected in the organization of its address and data buses, along with the physical and logical mapping of its I/O space. For microcomputers required to access offchip memory, a multiplexed address and data bus structure makes

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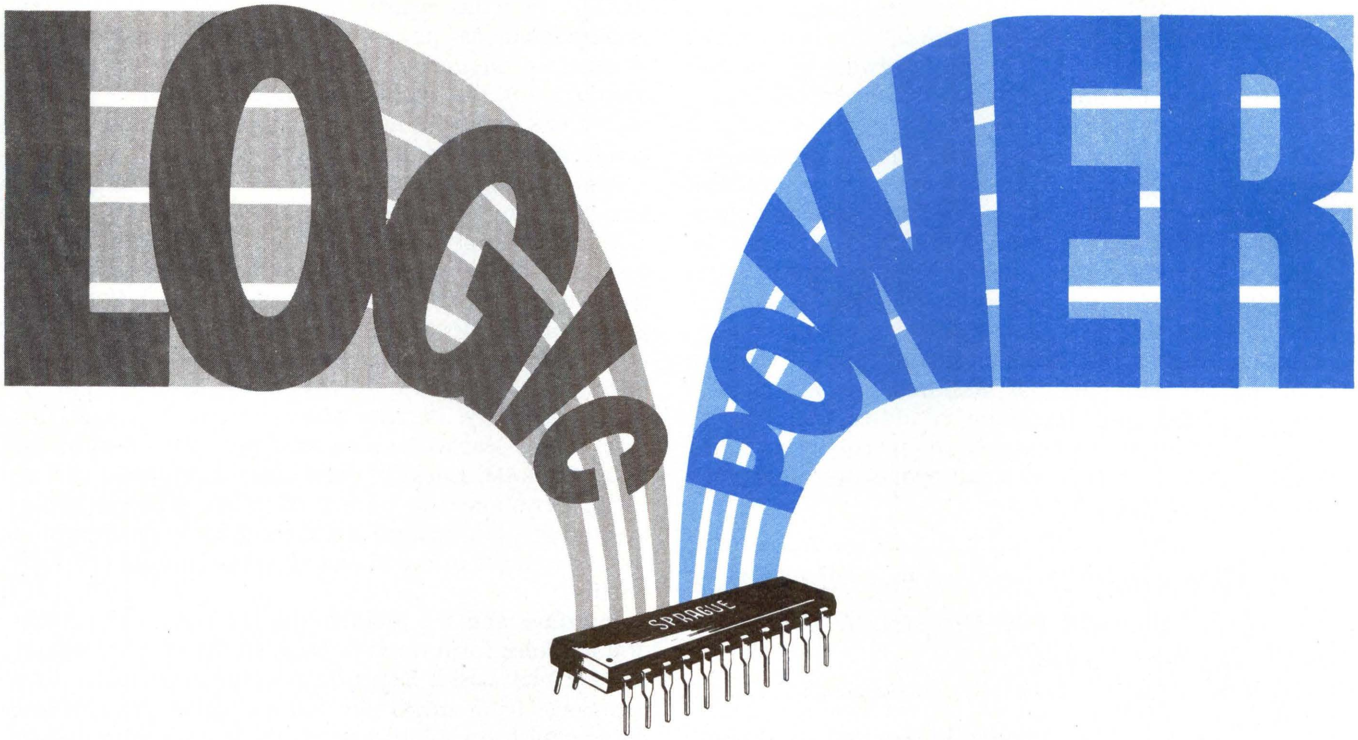

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efficient use of available pinouts. Several factors must be considered in deciding whether the I/O of a custom microcomputer should be memory mapped or have an independent address space.

In theory, there are several advantages to a single unified memory mapped I/O address space. Such a scheme eliminates the need for special I/O instructions and simplifies onchip addressing hardware by treating all I/O ports as memory locations. However, one major disadvantage of memory mapped I/O is that additional hardware is required for complete address decoding of each offchip I/O port. This becomes more acute when applications require a microcomputer system with a minimum chip count. Moreover, I/O ports must be grouped together in either low or high memory to avoid segmentation of memory used for programs or data. If only a few I/O ports are required, a custom microcomputer can carry them onchip and support memory mapped I/O with minimal additional onchip address decoding hardware. Reduction in addressable memory space due to memory mapped I/O is usually insignificant, due to the relatively small proportion of address space typically used for I/O.

Interface and peripheral modules form the link between the microcomputer and the real world.

If a custom microcomputer is required to support many more I/O ports than can be implemented onchip, it is advantageous to create a separate I/O space just large enough to map the required number of ports. If the majority of I/O ports are offchip and thus require some address decoding hardware, it is more economical to create a small I/O address space distinct from the memory space to minimize such decoding hardware (although a few I/O instructions will have to be added to the instruction set).

A custom microcomputer's bus structure is based on the number of available pinouts and the number of required I/O ports. When the custom microcomputer must be a single-chip microcontroller, the pinout crunch becomes acute. In such cases, all memory may be contained onchip, with all pinouts dedicated exclusively to I/O functions. It is difficult to test such microcomputers after packaging because there is no means of externally supplying the CPU with test vectors. The testability problem can be solved at the expense of onchip space by storing test vectors in ROM.

Memory. Control and automation oriented microcomputers execute control algorithms in response to either a periodic sampling clock or to asynchronous external events. Programs are stored in ROM, except in applications where a substantial amount of RAM is required for data buffering or overlaying of a long control program. A small amount of RAM is usually required for storing variables and working registers during context switches. Control programs for custom microcomputers are often designed to require so few data variables that read/write storage in the form of onchip registers, data latches, and I/O port latches are fully exploited for variable storage, reducing the need for RAM.

Schemes to minimize onchip RAM requirements are silicon efficient even where some additional ROM may be required for a complicated control algorithm, since ROM is typically 16 times as dense as RAM. Even so, RAM cells are the most silicon-efficient form of read/write storage. For this reason, working registers are often implemented as portions of onchip RAM, thereby eliminating the need for a separate set of address decoders for the register bank. Since typical control algorithms require a high ROM/RAM ratio, and ROM is much denser than RAM, a one-chip microcomputer system solution is often appropriate for a given application problem.

Where memory requirements for a custom microcomputer are so large that they are not economically feasible onchip, offchip standard RAM and ROM integrated circuits (ICs) are the most efficient solution. This point is reached when the incremental cost of onchip memory exceeds the total cost of the same amount of offchip memory. Because ROM is denser than RAM, this threshold is reached at a significantly lower number of bytes for RAM. Luckily, most control programs can be entirely contained in onchip ROM. An efficient implementation of a custom microcomputer system would thus have most of the ROM and a small amount of RAM onchip.

Interface and I/O peripherals. Interface and peripheral modules form the link between the microcomputer and the real world. Depending on the application, they can range from simple buffers and drivers to complex data acquisition subsystems. If the specific interface or I/O peripheral is available as a standard device, it may be economical to place it offchip or, if a single-chip microcomputer is required, to work from available tooling. Often, custom design houses maintain a library of standard cell designs that provide a variety of interface and I/O configurations for the design of a specific custom microcomputer. This functional cell approach to peripheral modules saves repetitive design cost and time.

Peripherals and I/O modules in a custom microcomputer compete with memory for available silicon area. There is a tradeoff between the relatively large pinout required when memory is offchip, and the low cost of offchip standard memory ICs. However, if custom designed peripherals and I/O modules are placed offchip, extra silicon and design efforts are required for pad drivers and input protection circuits. Therefore, in most custom microcomputers where single-chip implementations are infeasible, peripheral and I/O modules are integrated with the CPU while external RAM and ROM are used.

Alterable microcomputer methodology

Cost analyses of custom microcomputers reveal that 60% to 80% of the overall design cost and time is expended in the design and debugging of the CPU logic—the single most complex architectural element of a microcomputer. However, since peripheral and I/O modules are more directly coupled to the application system, they have a greater impact on overall system performance. Therefore, conventional approaches to custom microcomputers waste design resources.

AMI's alterable microcomputer shifts the focus of custom microcomputer design from CPU to peripheral

and I/O module design and integration. A customized AMU contains a predesigned 16-bit CMOS CPU. This core processor is integrated with memory and peripheral modules that are either available in AMI's functional cell library or are fully custom designed. Fig 4 shows the topological layout of a typical customized AMU.

Core processor selection

Peripheral modules for an AMU are highly functional and application specific. The core processor has the processing ability and word length to interface such peripherals efficiently, both in hardware and software. High end analog to digital (A-D) and digital to analog (D-A) converters offer resolutions greater than 12 bits, and many signal processing applications require that such data be processed in single precision, due to speed constraints. On the other hand, while a 16-bit core processor may not be required for a low end AMU, it offers a low cost upward migration path. For these reasons, a 16-bit core processor was selected for the AMU.

Once a 16-bit CPU was chosen, several other architectural factors were considered. In microcomputer systems for high end control and automation applications, several processes are simultaneously active. For example, the CPU can be multiprogrammed for multiplexing a display, handling A-D or D-A conversions, performing I/O with a console, and handling data communications with a modem. In such situations, event driven CPU operation is almost always more efficient than polled processing. Most AMU applications are interrupt driven to some degree. An AMU's performance would be greatly enhanced in an interrupt-intensive environment if its core processor were capable of fast context switching.

A memory to memory architecture is highly efficient in terms of context switching time. Since the processor's working registers are contained in memory and accessed through an onchip workspace pointer, a save or restore of processor state involves only this pointer, the program counter, and the status register. Since a processor with memory to memory architecture is also highly silicon efficient, it is ideal for a single-chip AMU. Therefore, the AMU's core processor has a memory to memory architecture.

The instruction set for the core processors must be optimized for memory to memory architecture and must feature advanced capabilities, including multiply and divide. The instruction set must also be compatible with an existing software base, due to increasing outlays on application system software. Since the 9900 family instruction set has these features, the AMU core processor's instruction set was designed as an enhancement of the 9900 instruction set.

The core processor has separate memory, I/O, and interrupt bus structures. Its 16-bit address and data word length is supported by an 8-bit memory data bus. It has a separate 32k-bit I/O space, bit-mapped through the use of a communications register unit (CRU) structure. The core processor's I/O instructions can directly address and perform I/O operations on fields, from 1 to 16 bits at a time. While this feature is ideal for many applications, it has special significance in the AMU core processor, which interfaces with custom designed peripherals that typically have nonstandard word lengths. For example, if the core processor had a byte-mapped I/O structure instead of its bit-mapped CRU structure, a 13-bit A-D converter would require two I/O instructions for a 2-byte conversion fetch. However, the AMU's core processor can fetch such a value in a single I/O instruction.

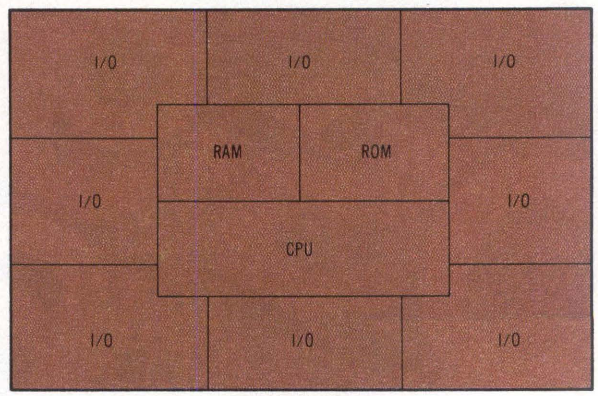

Fig 4 Alterable microcomputer functional block diagram. Core processor is integrated with required amounts of RAM and ROM, together with library cell or fully customized I/O and peripheral functional modules.

Silicon efficiency of the core processor's memory to memory architecture can be gauged by a comparison with other microprocessors fabricated in the same process technology. The S99C91 16-bit CMOS microprocessor, the AMU's core processor, has a die size of only 175 mils^2. This is about 30% to 40% smaller than existing 8-bit machines.

The core processor has a software initiated power-down state, which further minimizes average power consumption in low power applications. Its four prioritized interrupt levels allow it to function efficiently in an interrupt-intensive environment.

AMU economics

A customized alterable microcomputer offers several advantages and opens up new applications for low cost customized CMOS 16-bit microcomputers. Design effort required for a customized AMU is primarily due to integrating various functional cells, including the CPU, as well as designing and integrating any fully custom designed peripheral modules. By shifting the focus of the design effort from the CPU to peripherals and I/O modules, the AMU concept will spawn more specialized, but less expensive custom microcomputers. Cost reductions result because adding standard peripheral modules to an AMU design requires a minimal integration effort for a large increase in functionality. However, design costs of fully custom designed peripheral modules will reduce overall savings to some extent. In any case, a customized AMU will always offer savings from integrating predesigned modules, especially since each customized AMU design will not need a new core processor design.

There are several more advantages to the functional cell approach to custom microcomputer design. First, benefits result from spreading one-time module design costs over several customized products. Second, functional cell libraries are inherently self-propagating. If

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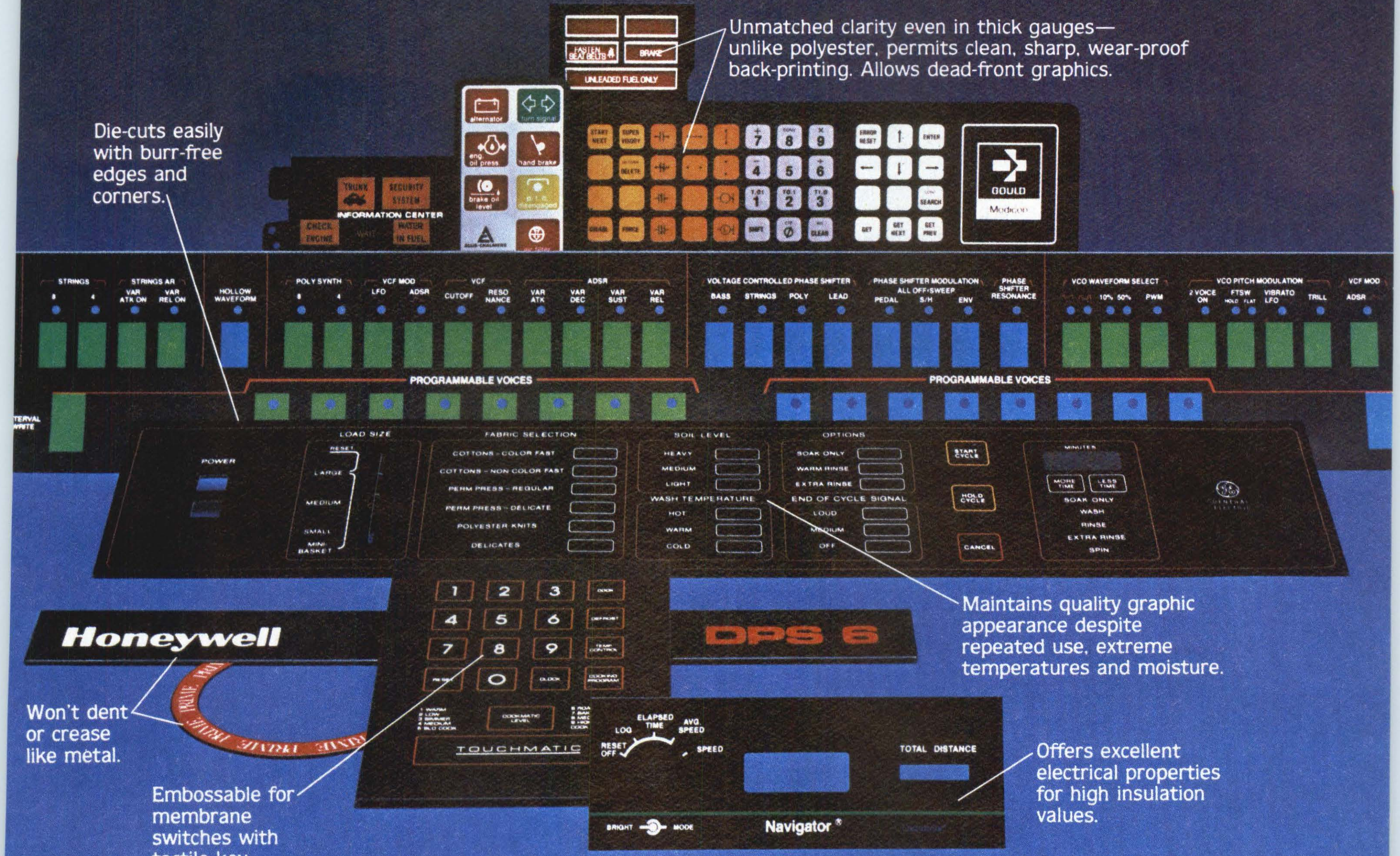

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proprietary considerations are not involved, a customer has the option of contributing any fully custom designed modules from his customized AMU to the functional cell library and selling standard product rights to AMI. Besides reducing the proportion of original design costs reflected in the first-time use of newly custom designed modules, this mechanism guarantees continued growth of AMI's functional cell library.

Architectural and technological considerations involved in custom microcomputer design closely parallel those involved in standard microcomputer design. However, the specific application dictates functional requirements and directly affects the design of peripheral and I/O modules.

Ironically, for a conventional custom microcomputer, a large proportion of design effort is expended in CPU design, even though peripheral and I/O modules have a more direct bearing on overall system performance.

With the AMU, the focus of design effort for a custom microcomputer shifts from the CPU to the peripheral modules. A custom 16-bit CMOS AMU can be produced less expensively and in less time than a fully custom designed microcomputer, since it is integrated from predesigned functional cells that include the CPU and peripheral modules. These functional cells can also be obtained separately as alterable microcomputer family standard products, including a 16-bit CMOS microprocessor, and I/O and counter/timer devices.

The functional cell library for AMU peripheral modules is expected to continue growing. As CMOS process technology progresses, the silicon area occupied by the core processor is likely to shrink, allowing more room on an AMU chip for integrating further functional peripheral modules and additional memory.

One possibility for the next generation is a microprogrammed AMU, capable of emulating different existing microprocessor architectures and instruction sets by a mere change in mask programmed microcode. Such a microcomputer would result in great savings in high volume microprocessor applications, including personal and business computers, where compatibility with a large existing software base is the primary requirement for CPU hardware.

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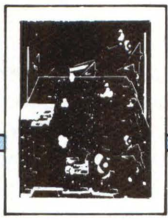

A SINGLE-BOARD APPROACH TO ROBOTIC INTELLIGENCE

The challenge: keep costs low, intelligence and mobility high.

by Lawrence A. Goshorn

Most industrial robots use numerical control technology developed in the 1970s. As a result, these robots and their internal hardware rely on a host computer to interpret control signals. Typically, the host computer is packaged in a cabinet and situated in a remote location. Data interpretation, transfer, and communication is via cables that connect computer and robot. Robots like this usually cost between $50,000 and $70,000, which puts them out of reach for many small manufacturers.

Providing the industrial community with an affordable robot for less than $10,000 that works for under $1.00/hour, operates in real time, and has minimum installation expense requires creative design. A thorough understanding of process control and microprocessor technology is also essential. Similarly, an understanding of typical industrial work is vital if the robot is to perform functions on the factory floor that cost justify its existence.

Developing a standalone robot with onboard computer power was the goal. This robot must easily fit into a wide range of factory environments without extensive programming. Also, the ideal machine must be reliable, easy to repair, and capable of interlinking into a totally automated factory system. Finally, the computing system must be less than one-fourth of the overall robot cost.

Lawrence A. Goshorn is president and founder of International Robomation/Intelligence, Palomar Airport Rd, Carlsbad, CA 92008. Mr Goshorn holds eight patents in industrial computer design. He received a BSEE in computer engineering and an MSEE in control systems from Arizona State University, where he also worked as an engineering instructor.

Single-board approach

Using onboard computing on the robots eliminates the need for cabling and connectors. It also saves factory floor space that can be occupied by robots rather than computers. At $200/square foot of factory floor space, a 3′ x 3′ (0.9- x 0.9-m) computer takes up $1800 worth of space. The onboard computer must control up to six robot axis motors in real time (ie, torso, shoulder, elbow, wrist pitch and roll, and optional hand and gripper). Accurately controlling these motions in a rugged industrial environment demands a dependable computing system.

In the preliminary breadboarding of International Robomation/Intelligence's multiple microcomputer processing robot controller, the computing power needed to control a 6-axis machine in real time required four printed circuit boards (PCBs). These boards were horizontally mounted in a card cage within the robot's trunk section. However, there are disadvantages to this approach.

Cost alone makes the 4-board approach unrealistic. Extra components, like the motherboard, connectors, card cage, and an interconnect bus are expensive to manufacture and lower reliability in factory environments. In addition, horizontal mounting causes excessive vibration and unavoidable heat spots, so a fan is required for cooling. Finally, a multiple-card approach costs substantially more to manufacture, spare, and repair.

On the other hand, single-board design (Fig 1) reduces the robot's overall cost, but requires a much greater design and development investment at the beginning of the product development cycle. A single vertically mounted PCB eliminates the need for a fan, card cage housing, connectors, backplane bus, and

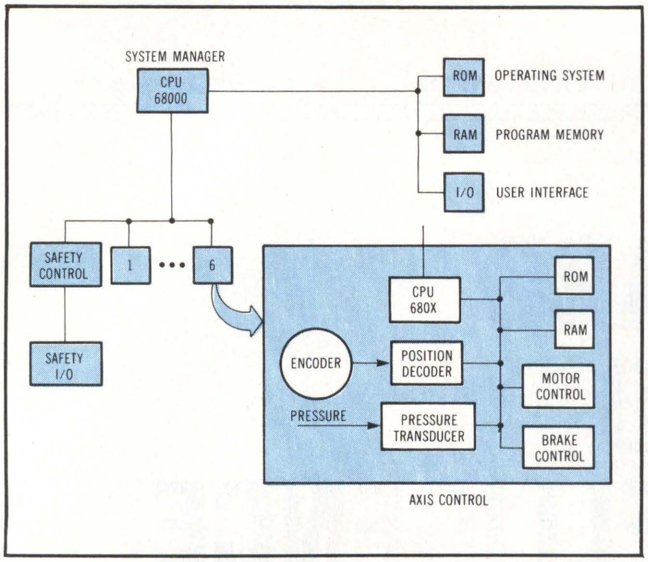

Fig 1 Single-board robot control unit. Six-layer PCB performs 10 MIPS and features six 6800-type axis processors running under control of one 68000 processor.

other expensive constraints encountered with a multiple-card approach. In addition, the mean time to repair a unit is reduced to minutes. A user can replace an entire control board with a spare and send the defective board to a repair depot.

Packaging enough horsepower on the PCB

To keep costs low, pneumatic motors are used to drive the gears and chains that move the robot's various axes. Air motors reduce the cost of powering the robot to a tenth of what direct current servomotors and hardware cost. Air motors, however, require tremendous computing power to control because of the extreme variations in motor parameters between zero and full revolutions per minute (rpm) at varying loads. Controlling speeds at rates lower than 50 rpm requires extensive mathematical calculations. With six such motors on one robot, even the most advanced central processing unit (CPU) runs out of power. A computing capacity of 2 MHz/axis is required. A minimum of 12-MHz computing power is required just to control each axis and its motor.

PCBs designed to provide this control can generate from 35- to 40-MHz computing horsepower. That clock rate translates to a realtime processing capability of from 8 to 10M instructions/s (MIPS). In Fig 2, the system block diagram illustrates the board architecture necessary to provide this computing power.

The board contains eight microprocessors. Six are Motorola 6800 family 8-bit chips, all with associated memory—2k bytes of random access memory (RAM) and 8k bytes of erasable programmable read only memory (EPROM)—analog to digital converters, pressure transducers, digital timers, relay drivers, and digital feedback circuitry. Each 8-bit microprocessor operates as an independent process control computer in charge of a certain axis on the robot. Each microprocessor can operate at a 2-MHz clock speed and power range. The computers for axis control do not communicate with each other. Rather, they take commands from and are monitored by another very powerful microprocessor on the PCB. A 16-bit Motorola 68000 controls realtime foreground activity, as well as programming, reporting, and background activity. It has its own onboard RAM up to 265k bytes, 64k bytes of EPROM, and all the associated hardware, input/output (I/O), and firmware necessary to oversee total robot operations. Designed to perform between 4 and 16 MHz, the 68000 acts as the master computer coordinating all activity of the six axis computers in real time.

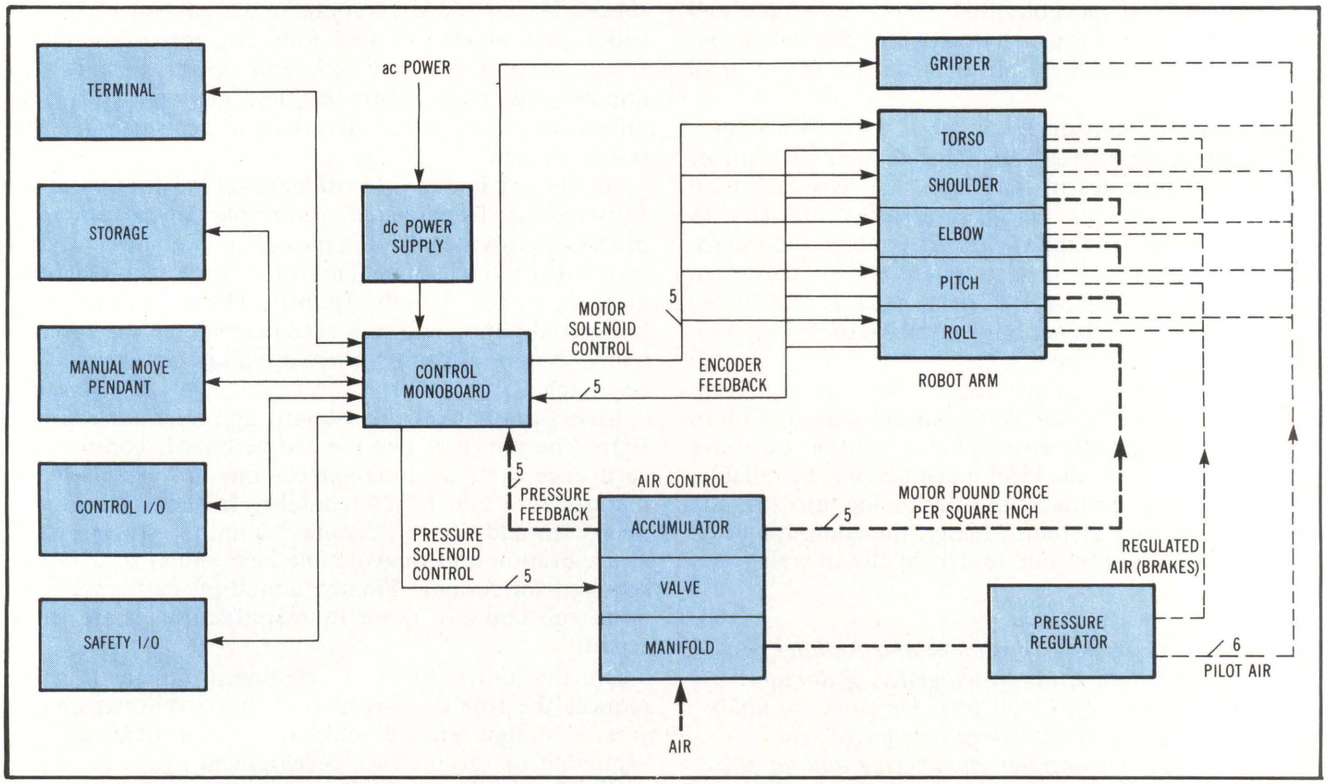

Fig 2 Robot system component block diagram. Monoboard oversees all facets of robot operation as well as provides means for I/O and system programming.

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Another 8-bit microprocessor serves as the safety computer. It monitors the 16-bit master computer's operations and can also be equipped with external sensor lines to monitor the robot's workspace for safety conditions. Thus, each of the eight microprocessors on the PCB performs a dedicated task and operates within an architectural hierarchy, termed "micro-array computing."

A data acquisition cycle of 2 ms or less is maintained at all times. Interrupts are held to less than 100 μs, and control algorithms are computed at varying intervals. Axis motor control processors constantly receive signals from sensors monitoring each axis motor's activity. Signals consist of computing and controlling torque, acceleration, rpm, location, air pressure, and braking. The 16-bit 68000 microprocessor coordinates the axis control processors, sends each calculated load factors, and synchronizes the robot movements at precisely the right location in precisely the right time.

Innovative circuit design is necessary to incorporate all these microcomputer systems onto a single card. Six layers of circuits contain more than 11 interconnected system buses. These buses include two serial communications buses, pendant direct control bus, power supply bus, transducer monitor (diagnostic and analog) bus, computer expansion bus, memory expansion bus, position feedback bus, industrial I/O bus, and maintenance monitor bus. In addition, the board contains large scale integration circuitry, analog circuits, fluid pressure transducers, and other complex components. There are many legs to interconnect and not enough room on a 2-sided board—hence, six layers. Two layers are for power and ground, four are for signal interconnects. Computer aided design/computer aided manufacturing was used to develop the circuit layout, since it is beyond human capability to accurately lay out six layers within the given time constraints.

Packaging the PCB for optimum performance

Laying out a single PCB with eight computers, each dedicated to performing specific robotic functions, is difficult. Form-factoring the PCB to fit onto a shock-isolated, swing-out chassis is yet another task. Industrial environments add problems of electrical noise, contamination, vibration, and heat. To overcome vibrations, a rigid mount supports the PCB in a shock-isolated housing. Stiffeners assure that the board remains stable during all kinds of robot operations. The housing swings out, allowing each side of the board to be easily accessed without board disconnect.

Single-plane mounting is housed vertically to provide natural convection cooling and rapid heat dissipation. Possibility of contamination from liquid or solid debris is minimized with the vertical mount. Vertical mounting effectively provides more room for mechanical maintenance and separates the PCB from the heat of the power supply, which is mounted well away from the PCB. Filters and battery backup are included with the power supply module. A standard off-the-shelf high performance radio frequency interference/electromagnetic interference filter isolates line transients and spikes from the logic supply. All short transients are filtered so the board receives smooth, continuous power despite surges. The filter controls power glitches from 0 to 10 ms. An onboard battery handles long transients of 10 ms to 10 hours in duration.

Functional partitioning for minimum communications

State of the art PCB design enables placing a tremendous amount of processing power on a single board. For true array processing to occur, however, each microprocessor's activity must be partitioned. A form of communication between the master Motorola 68000 and the dedicated 8-bit axis control computers is needed.

Because all six axis processors require a continuous exchange of information with the 68000, a shared communication scheme that optimizes throughput and minimizes contention is necessary. This scheme must be reliable and easy to troubleshoot. The communication scheme uses a mailbox (register) pair per axis and associated semaphores or flags, along with prioritized vectored interrupts. Interrupt vectors are used for attention getting in both transfer directions to minimize latency for any one axis service. In other words, any axis processor knows (within its interrupt service time) when a message from the 68000 is placed in its mailbox. The 68000 on the other hand, knows (by unique vector) exactly which axis processor places a message in its outbound mailbox. Furthermore, since the axes run asynchronously, it is highly likely that no other axis needs attention at that time. In the worst case, all six axes would request service simultaneously. If that were to happen, the 68000 would see the highest priority axis interrupt first. Taking the data from that mailbox would cause the next lower priority axis interrupt to be presented. The vectoring scheme allows automatic, random interrupt servicing to occur without software intervention for axis identification.

Both the 68000 and the axis processors can see the flags they raise when they send a message and thereby avoid overwriting their previous transfer. The 68000 reads each axis mailbox at a unique memory mapped address. Writing, however, can be done to any axis, any combination of axes, or all six at once based on a bit setting in a subaddress field. This "broadcast write" mode permits

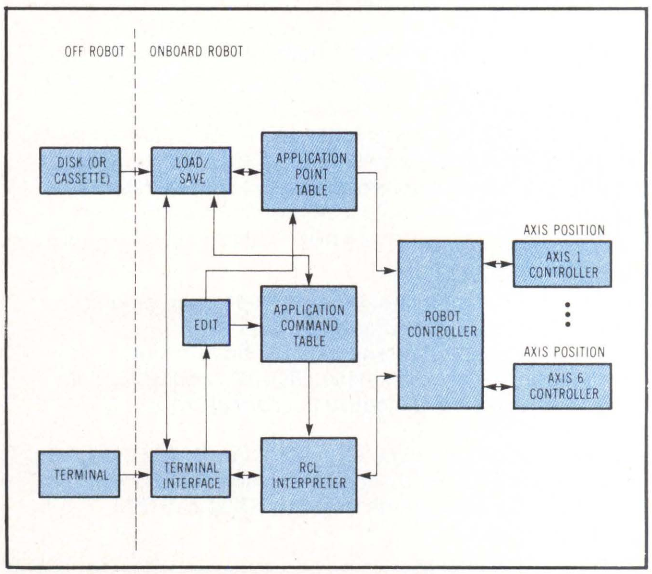

Fig 3 Software architecture overview. Segmented software supports six axis controllers in real time and supplies system and housekeeping instructions.

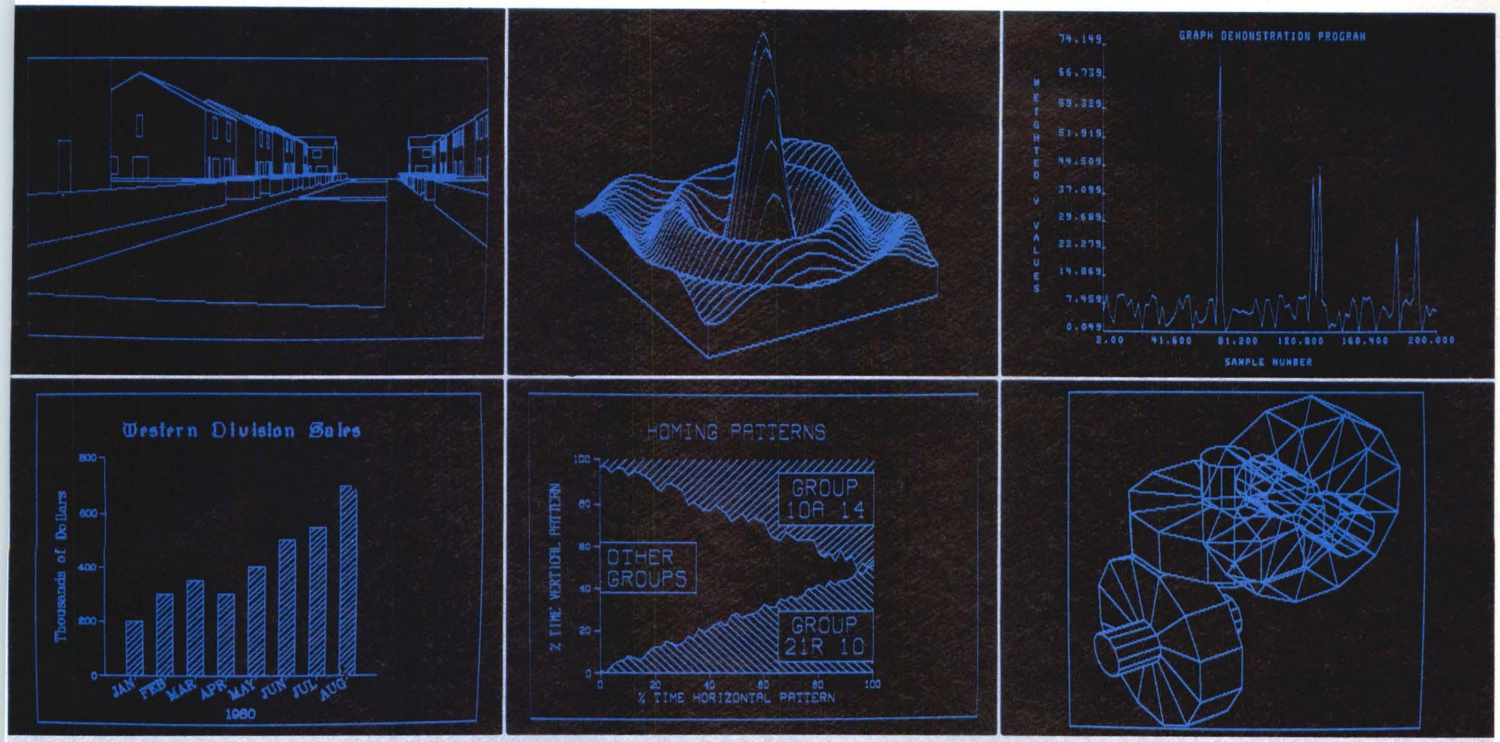

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TABLE 1

Robot Commands

Mnemonic	Parameter field	Description
HOMER (HR)		Move all axes to home position
HOMEA (HA)	axis number	Move specified axis to home position
INIT (IN)	point number	Clear each axis controller and set robot position to specified point number
MOVER (MR)	point number	Move robot to specified point
MOVEA (MA)	axis number, delta theta, speed	Move specified axis through angle of delta theta at specified speed
JOGR (JR)	point number	JOG robot to specified point
JOGA (JA)	axis number, delta theta, speed	JOG specified axis through angle of delta theta at specified speed
OPEN (OP)		Turn on gripper, open output line, and wait for gripper open input line to go high
CLOSE (CL)		Turn off gripper, open output line, and wait for gripper closed input line to go high
TOL (TL)	tolerance factor	Specified tolerance factor is multiple of 0.04" and is transmitted to each axis. Zero means no tolerance specified for fastest possible move
ATOL (AT)	tf1, tf2, tf3, tf4, tf5	Each of five specified tolerance factors are multiples of 0.04" and are transmitted to specified axis
SPEED (SP)	speed factor	Speed factor is a percentage of maximum speed and is transmitted to axis with largest distance to move. Speed factor transmitted to other axes is ratio of their distance to move, divided by largest distance to move, times specified speed factor
ASPEED (AS)	sf1, sf2, sf3, sf4, sf5	Speed factor is specified for each axis and transmitted to corresponding axis
SMOD (SM)	speed modifier	Speed modifier is percentage (0 to 200%) that modifies all speed factors in application program. This allows user to modify speed of application without changing all individual speed factors in program
COMPP (CP)		This command instructs robot controller to compute pressure reference for each axis as function of load factor and speed
PRES (PR)	p1, p2, p3, p4, p5	Transmit specified pressure reference, pound force per square inch (psi), to each of corresponding axes
APRES (AP)	axis number, pressure	Transmit specified pressure reference (psi) to specified axis
LOAD (LD)	load	Specifies payload in pounds, which is being carried by robot
DEBUGON (ON)		Prints starting, target, and actual thetas for each axis after each move or jog command is executed
DEBUGOFF (OFF)		Stops DEBUGON feature (default = DEBUGOFF)
AXIS (AX)	a1, a2, a3, a4, a5	Enables/disables specified axis from communication: 0 = disabled, 1 = enabled
SNAP (SN)	a1, a2, a3, a4, a5, b, d, t1, t2, t3, t4	Enables and disables snapshot requests. a1 to a5 specifies axis to be snapped where 0 = axis snapshot disabled and 1 = axis snapshot enabled. b = buffer type: 1 = fixed, 2 = recirculating. d = data type: 1 = 2 ms theta, 2 = dither interval snap data. t1 to t4 enables and disables snapshot during various modes of control: t1 = acceleration. t2 = velocity, t3 = deceleration, t4 = jog, 1 = on, and 0 = off for each

perfect axis synchronization to occur when needed, or allows fast emergency codes to be sent in safety situations.

Control computer command language

To support minimum communications, a special language provides compact forms for commands. These commands require a minimum amount of communication between processors. When the 68000 tells a processor to begin execution, no further communication with the master computer is needed. The language provides a series of commands based on a number of different control states within the 6800. These include acceleration, velocity, deceleration, stopping distance, slow approach, jog, hold, brake, and motor pressure control. Control states, written as subroutines, are called depending on the category of the work statement issued by the 68000. Each subroutine allows a maximum amount of work to be performed with a minimum amount of communications. Rather than defining motions, each task of the axis is defined (ie, move slow, move little, move big, accelerate, slow down, and stop). These different kinds of work are grouped in the subroutine library. What ensues is task oriented macros that carry each axis through a work cycle. Included in the subroutines are error condition checks that are sent to the master computer.

All axes have specific tasks to perform in any given robot motion. Perhaps three must move at rapid acceleration and velocity to reach a certain location, while two may have to move slightly, and a third may be required to perform a very slow and accurate task. Thus, there are a number of commands that the master processor (68000) must deliver to each computer. It may also let each know how long they have to do the task so that all computers complete their jobs simultaneously.

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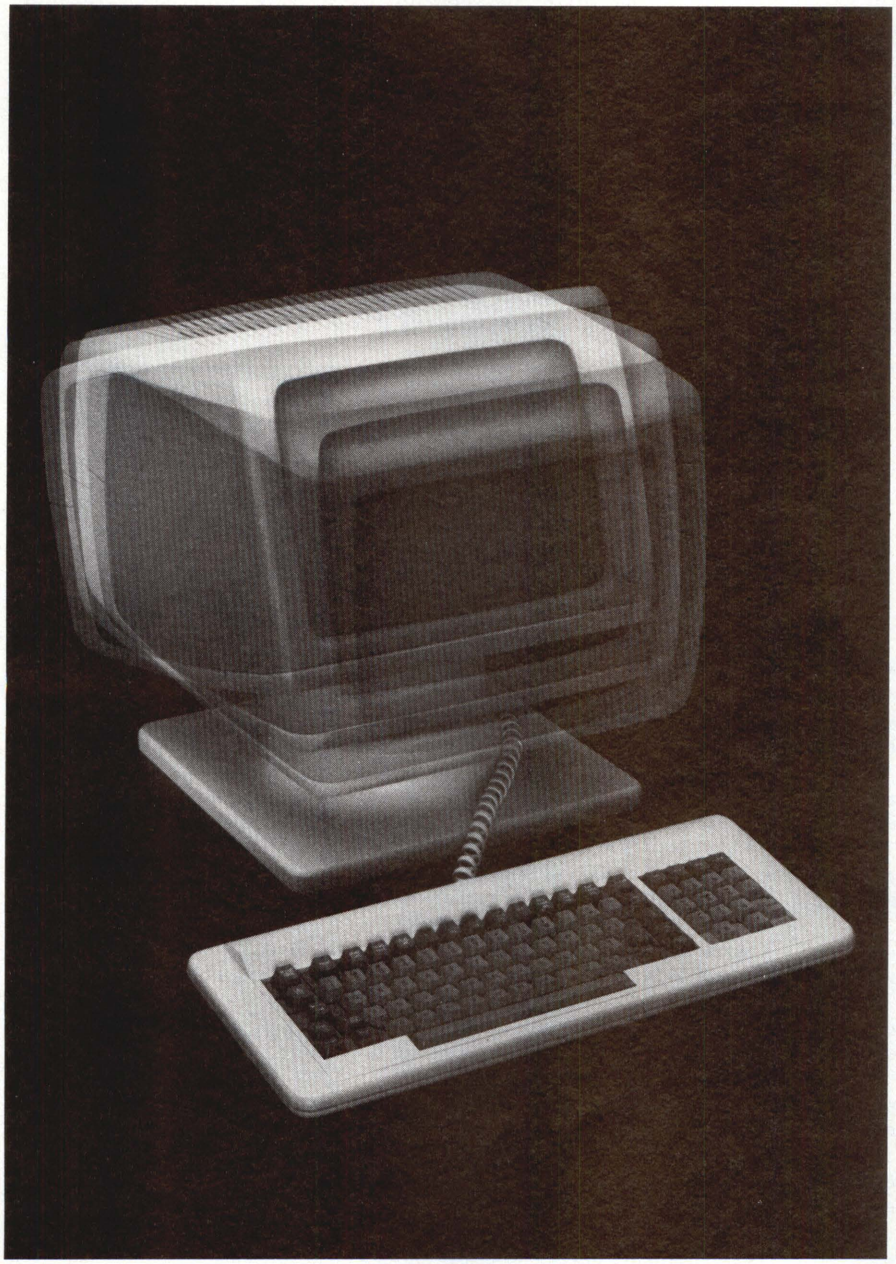

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TABLE 2

Range of Parameter Field

Parameter	Range
Pressure	40 to 120
Load	0 to 50
Delta theta	8,388,608 to 8,388,607 (23 bits)
Speed modifier	0 to 200
Speed factor	0 to 100
Tolerance factor	0 to 127

The master computer also tells the safety computer that everyone on the board is going into a task mode. Therefore, the 68000 computer issues the commands and monitors individual processors. At the same time, the 68000 performs background data manipulation, such as adaptive load calculations, for each axis and coordinate transformation. It also prepares to issue the next sequence of commands in the robot's work cycle.

Foreground activity is performed in real time. The entire process is like a football game. The 68000 is both the coach and the quarterback—responsible for the entire game plan and for executing that plan. Six axis control computers are the players, performing the required moves. The safety computer is like the referee, monitoring the execution of each play by the quarterback.

Segmented programming facilitates implementation

At first glance, programming requirements to make the eight computers work together seem enormous, especially the mathematics involved. Software is broken into nine different sections to simplify the programming task: one section for each axis control computer, one section for the 68000's foreground operations, one section for the 68000's background operations, and another section for the safety computer. It is much easier to organize programming efforts by assigning programming teams to each aspect.

While all 6800 axis control computers have identical software, each computer has its own set of parameter tables of approximately 140 task oriented parameters unique to that axis. Within the 6800s, there are various subroutines or control states, which were divided to be

TABLE 3

Logic Commands

Mnemonic	Parameter field	Description
SET (ST)	bit number	Set flag or digital output specified by bit number to a one
RESET (RS)	bit number	Reset flag or digital output specified by bit number to a zero
INCR (IR)	register number	Increment register specified by register number by one
DECR (DR)	register number	Decrement register specified by register number by one
NOT	register number	Perform 1's compliment on register or I/O port specified by register number
XFER (XF)	register 1 number, register 2 number	Transfer contents of register or I/O port specified by register 1 to register or I/O port specified by register 2
ADD	register 1 number, register 2 number	Add contents of register or I/O port specified by register 1 to contents of register or I/O port specified by register 2 and put results in register 2
SUB	register 1 number, register 2 number	Subtract contents of register or I/O port specified by register 1 from contents of register or I/O port specified by register 2 and put results in register 2
OR	register 1 number, register 2 number	Logical OR contents of register or I/O port specified by register 1 with contents of register or I/O port specified by register 2 and put results in register 2
AND	register 1 number, register 2 number	Logical AND contents of register or I/O port specified by register 1 with contents of register or I/O port specified by register 2 and put results in register 2
XOR	register 1 number, register 2 number	Logical exclusive OR contents of register or I/O port specified by register 1 with contents of register or I/O port specified by register 2 and put results in register 2
TSTL (TL)	register 1 number, register 2 number	Test if contents of register or I/O port specified by register 1 are less than contents of register or I/O port specified by register 2
TSTE (TE)	register 1 number, register 2 number	Test if contents of register or I/O port specified by register 1 are equal to contents of register or I/O port specified by register 2
TSTG (TG)	register 1 number, register 2 number	Test if contents of register or I/O port specified by register 1 are greater than register or I/O port specified by register 2
TSTB (TB)	bit number	Test if flag or digital input specified by bit number is set
BTRUE (BT)	label	Branch to specified label if preceeding command is true
BFALSE (BF)	label	Branch to specified label if preceeding command is false
GOTO (GT)	label	Branch always to specified label
LOADI (LI)	register number, constant	Load immediate specified constant to register or I/O port specified by register number
WAIT (WT)	milliseconds	Wait specified milliseconds before going to next command
LCALL (LC)	label	Call library subroutine specified by label
UCALL (UC)	label	Call user-created subroutine specified by label
NOP		No operation

worked on separately for efficient programming. In addition, an automatic calibration program that generates more than 700 unique control parameters for the robot's axes is addressed as an individual programming task.

Due to hardware design and hierarchical architecture, neither a multiprogramming operating system nor memory mapping was necessary. Communications take place in parallel transfers, via structured commands. The goal, again, is a low overhead operating system for the 6800 axis control processors. Within each 6800 CPU, the entire realtime operating system takes up 600 bytes of instruction.

In the 68000 master computer process controller, commands are burned into the 64k bytes of EPROM. However, all 64k bytes are not used, leaving approximately 32k bytes for the 68000 RMS operating system and future enhancements. On the 68000 CPU, 256k bytes of RAM contain all the robot applications programs, feedback, and point tables.

Robot software is segmented to tackle each task (see Fig 3). In addition to the six axis controllers, the software systems include a robot controller, a robot control language (RCL) interpreter, a load/save interface, an RCL command table editor, an application point table creator, editor, and a programming terminal interface. The RCL is further segmented into three subsections. A straightforward group of robot and logic commands contains approximately 100 commands that move the axes to home positions or specific points, provide tolerance specifications, speed requirements, speed factors, speed modifiers, and load factors that specify payload carried by the robot. These commands are required to set parameters needed during robot motion. (See Table 1, "Robot Commands.")

Logic and arithmetic commands allow the advanced user to perform more intelligent robot activities. These include basic logic, testing, branching, and arithmetic operations. Logic commands include a command mnemonic that immediately establishes the parameter field (See Table 2 for a range of values for each of the tested parameters.) They also describe the task to be performed. (See Table 3, "Logic Commands.")

User programming

To implement a robot program using the RCL, a system terminal with standard RS-232-C interface and editing, as well as communications capabilities, is required. Actual commands are entered through the terminal. For loading and saving application programs and point tables, one of three methods is available—a floppy disk drive, a cassette recorder, or a remote computer.

User application point tables for the robot are entered via the "teach pendant" (ie, a portable handheld programmer). (See Fig 4.) The teach pendant enables the user to input a data point relative to an application. The robot's coordinate system is based on axis angles and, in the near future, users may work in standard Cartesian coordinates X, Y, and Z. The X, Y, Z points in space take the user to the end of the wrist plate. While the wrist provides pitch and roll, a robot hand or other tool attached to the end of the wrist plate can provide yaw. By stepping the robot to the next application point in space and pressing the pendant's enter button, the robot can be programmed manually in axis formats.

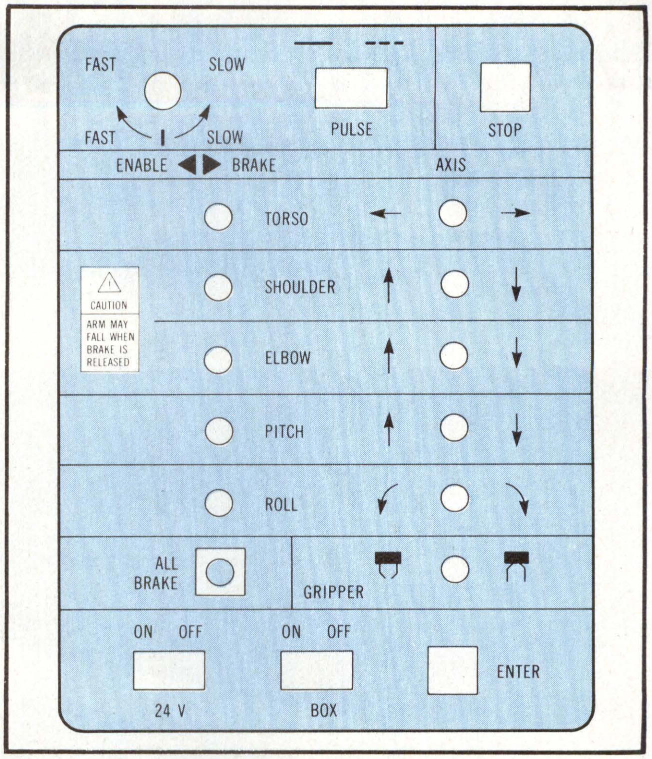

Fig 4 Handheld teach pendant programming aid. By manually controlling robot's motion with teach pendant, users can quickly and easily program robot for most pick and place tasks.

It is possible for an entire factory floor to be occupied by a few hundred robots, each performing a specific part of the manufacturing cycle. Robots are engineered to take up the same floor space as their human counterparts. However, these robots work at about $0.60/hour (2 shifts usage plus required power), compared with an average of more than $10/hour (burdened) per employee.

RS-232-C or RS-422 communications capability provides a link between the robot and a remote control processing system if a truly automated factory environment is to be created. Robots can easily be programmed to keep track of inventory and work in progress if required.

Processing hardware and architecture, developed to operate this industrial robot, represent a major step toward affordable methods of artificial intelligence. Segmenting computer activity, along with the rapid communications possible with parallel transfer of data through onboard circuitry, marks the beginning of an era in computer architecture technology. Micro-array computing lends itself to the tremendous amount of data processing required for computers to maintain control and make viable judgments. While the board designed to operate the industrial robot operates at speeds from 8 to 10 MIPS (more computing horsepower on a single card than available from most superminis or mainframes), the possibilities are far greater.

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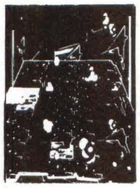

SILICON OPERATING SYSTEM MODULES AID REALTIME CONTROL

A system designer's toolbox should include standard silicon software components that can be quickly assembled to create a responsive custom operating system.

by Phil Bunce

The latest generation of industrial automation and control systems uses embedded 16-bit microprocessors. To fully exploit the power of these microprocessors and to provide a programming methodology for structuring realtime control applications, a multitasking realtime operating system is critical.

An embedded microprocessor is buried inside some larger system—inside intelligent terminals, a communications system, analytical instruments, industrial robots, or peripheral controllers. Embedded microprocessors are distinguished from standalone microcomputers, such as business computer systems, personal computers, and word processors, by the uniqueness of their applications.

Software running on embedded computers must meet a different set of requirements than standalone system software. Perhaps the most important one is realtime responsiveness. Dedicated control systems must be able to respond to unexpected events in the outside world rapidly enough to control some ongoing process. Their software must also be able to handle many tasks concurrently, since real world events generally overlap each other, rather than occur serially.

Programmers find that a common set of mechanisms is necessary to support such realtime applications. Moreover, realtime system designers generally spend more of their time on these basic software blocks than on the application program itself. These software mechanisms are usually contained in the operating system which, in these embedded applications, is often called a realtime operating system or realtime executive. The realtime executive serves as the foundation upon which the rest of the application software is built. These executives greatly differ in design from operating systems for standalone applications such as UNIX. Three characteristics of realtime executives are support for multitasking (ie, the ability to support several subprograms that all compete for system resources); quick response to external events, usually through sophisticated interrupt handling mechanisms; and the ability to be easily extended to support new input/output (I/O) devices, interrupts, and system calls.

For microprocessor applications, however, widespread use of realtime operating systems has been severely hindered by board level dependencies of typical software packages. Minicomputers and mainframes are delivered as complete computers, whereas microprocessors contain only the central processing unit (CPU) of a board level computer. Several additional chips—timers, interrupt controllers, I/O controllers,

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etc—must be added to the CPU to create a fully functional computer. Consequently, minicomputer and mainframe vendors are able to supply software that works on all their products, whereas microprocessor vendors can only supply software that works on a fraction of their product line.

Implementors of systems that do not conform exactly to an existing board level product are forced to design, build, debug, and maintain their own realtime system, or they must buy and extensively modify source code to run on their own hardware. Both alternatives are risky, time-consuming, and expensive. This software problem can be solved by using techniques that have worked well in reducing hardware costs. The basic cause of lower hardware costs is the use of standard large scale integrated (LSI) circuits, which board designers can easily connect without detailed knowledge of the components' inner workings. Similarly, designers of microprocessor based systems need standard software components, analogous to standard LSI circuits, to drive down the high cost of software.

A software design methodology known as silicon software offers a potential solution to the software cost problem. One of the first products to use this methodology is the versatile realtime executive (VRTX), a silicon software component for embedded microprocessors. VRTX (pronounced "vertex") can be used in any computer hardware environment without being modified. In fact, it is used more like a hardware component than as a traditional piece of software. The VRTX family currently includes versions for use with three of the most popular 16-bit microprocessors: Motorola's 68000, Intel's 8086, 8088, and 186, and Zilog's Z8002. Although these versions differ internally—each is written in assembly language—they function identically. Applications written in the same high level language (eg, C) make calls to VRTX resources and, when compiled in a given microprocessor's native code, are portable among the three processors now supported by VRTX.

Overview

A system based on VRTX is designed like a stack of bricks (Fig 1) with each level making use of the functions provided by the level below. The system's hardware occupies the bottom level, above which reside the simplest, most hardware-dependent operating system software functions. User defined application programs are on top. Thus, each level defines a virtual machine for the level above.

Functions provided by high levels of software are indistinguishable from functions provided by the hardware. Each software level adds several instructions to the system's instruction set. In application programs, VRTX adds 22 high level instructions (system calls) to the microprocessor architecture.

In Fig 1, the cross-hatched area indicates the operating system primitives contained within the VRTX read only memory (ROM). Interrupt service routines reside in the space left between the system and the hardware. These routines are small, hardware-dependent code segments that provide interrupt-handling capabilities for particular peripheral chips, such as widely used timers and serial I/O chips. These routines reside outside the VRTX ROM and are either written by the designer or are selected from a peripheral chip support library.

Other operating system devices not provided within the system are shown to the right of the system nucleus in Fig 1. These include user defined system call handlers and mechanisms for initializing and saving the state of special user devices (eg, a Fourier transform chip in a signal processing application).

Task management

A task is the basic unit controlled by VRTX. Each task is a logically complete execution path through user code that demands the use of system resources. In VRTX, as many as 256 separate tasks can compete for system resources, with each task assigned a level of priority. The system allocates control of the CPU to the task with the highest priority.

Tasks can create other tasks. They can also delete, suspend, resume, and alter their own priority or that of others. The system employs an event driven, priority based scheduling algorithm that ensures the highest priority task available for execution is running on the processor. If a clock is present, VRTX also permits task delays and round-robin scheduling. All of these task management functions, as well as other functions, are implemented by system calls. (See the Table, "VRTX System Calls.")

Tasks can also send messages to one another. Two calls, SC_POST and SC_PEND, provide a complete mechanism for communication and synchronization. Tasks can send and receive 2- or 4-byte values, depending on the processor's address length, to any location in memory. These values may, of course, be pointers to large data structures. If a location is empty (holds no message), a task attempting to receive data from it suspends execution (pends) until a message arrives.

This approach obviates the need for complex, predefined entities such as semaphores, message headers, and exchanges. Resource locking and mutual exclusion are as easy as message sending. Resource locking occurs when all the tasks attempting to use the resource pend at the same location. As each task finishes with the resource, it sends a message to that location, enabling the next task.

The VRTX memory allocation mechanism represents a compromise between static and dynamic memory

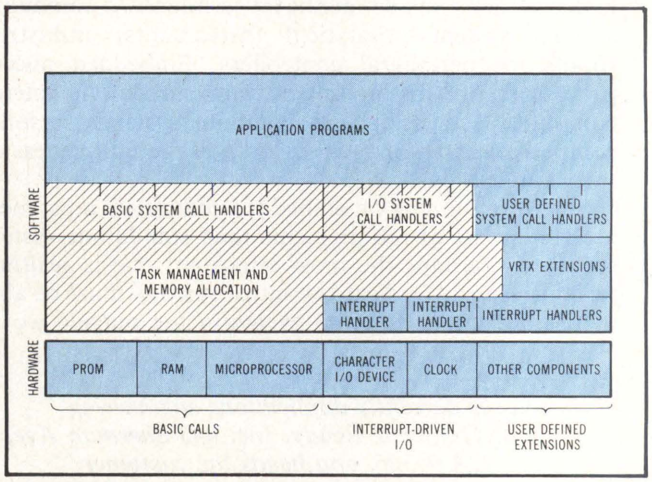

Fig 1 Typical component operating system structure. Dashed areas indicate functions provided by system nucleus. Only hardware assumptions made are specific microprocessor being used, and existence of 1k of RAM.

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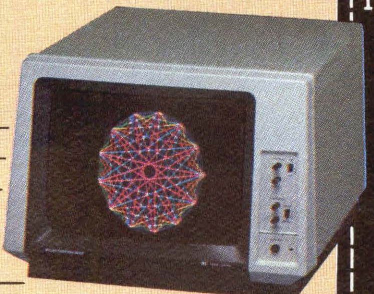

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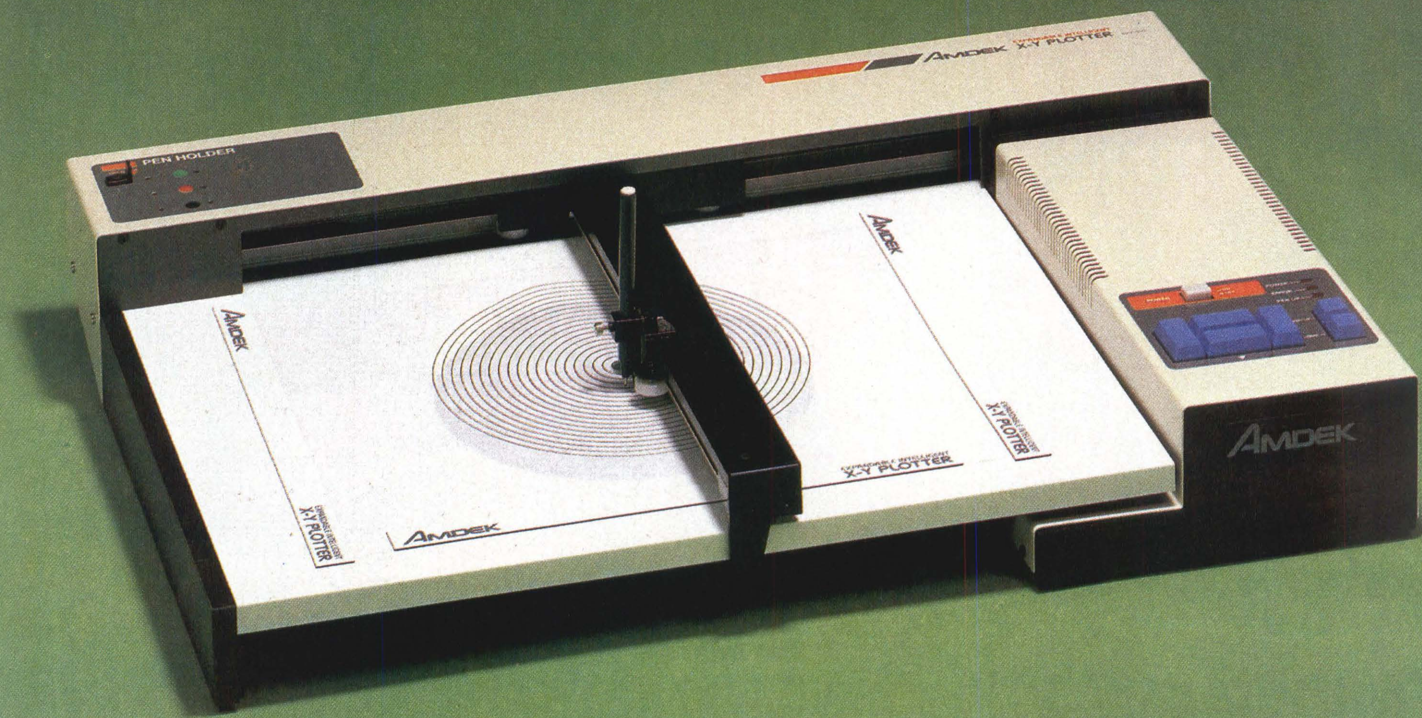

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VRTX Systems Calls

Call	Function
	Task management
SC TCREATE	Task create
SC TDELETE	Task delete
SC TSUSPEND	Task suspend
SC TRESUME	Task resume
SC TPRIORITY	Task priority change
SC TINQUIRY	Task inquiry
	Intertask communication and synchronization
SC POST	Post message
SC PEND	Pend for message
	Interrupt servicing
UI POST	Post from interrupt handler
UI EXIT	Exit from interrupt handler
UI TIMER	Timer interrupt
UI RXCHR	Received-character interrupt
UI TXRDY	Transmitter-ready interrupt
	Realtime clock
SC GTIME	Get time
SC STIME	Set time
SC TDELAY	Task delay
SC TSLICE	Enable round-robin scheduling
	Character I/O
SC GETC	Get character
SC PUTC	Put character
SC WAITC	Wait for special character
	Memory allocation
SC GBLOCK	Get memory block
SC RBLOCK	Release memory block

allocation schemes with memory compaction (garbage collection). The tradeoff is between static allocation, which is too restrictive, and a dynamically allocated memory with compaction, which imposes too high a system overhead. To circumvent these shortcomings, a VRTX task is allocated a fixed-size stack. Each task can also dynamically acquire memory in fixed-size blocks. Dynamic allocation is provided by the system calls SC_GBLOCK and SC_RBLOCK, with which user tasks get and release blocks of memory. The user sets the block size and the stack size via parameters specified at runtime.

Interrupts, I/O, and initialization

For quick response in a system using VRTX, user supplied interrupt handlers issue system calls to alter the scheduling of critical tasks. When a significant event occurs, the interrupt handler posts a message to a waiting task using the UI_POST command. The UI_EXIT command forces immediate rescheduling after the interrupt handler finishes servicing the interrupt. These two commands provide a general interface between VRTX functions and device-dependent service routines.

Many applications require a realtime clock and at least one character oriented I/O device. The user need only supply a small hardware-dependent interrupt service routine for each. Using seven clock and character system calls (see Table, "VRTX System Calls"), VRTX manages all the logical operations needed to provide user application tasks with a full repertoire of associated clock management and character I/O commands.

System initialization comprises those preliminary activities—such as setting the initial values of registers, memory locations, and VRTX variables—that must be performed before the main application program is executed. As with I/O devices, system initialization depends upon the overall board environment. Because VRTX is designed to make few assumptions about its environment, it performs only those initialization activities that depend on the existence of the CPU and memory. The rest of initialization is left up to the user. Hooks within VRTX allow the user to initialize special user supplied devices upon system reset.

Configuration

Any dependencies on board particulars (eg, specific clock and interrupt chips or I/O structure) have been removed from VRTX. This chip level support is provided by object code, which means that users with custom boards do not have to acquire and modify source code. A user supplied configuration table, along with device-specific interrupt handlers, provides the interface between VRTX and its environment. Like the exception vector table (EVT) for the 68000 processor, the interrupt vector table (IVT) for the 8086, and the new program status area (NPSA) for the Z8000, the configuration table is a window to the board environment. With this table, the user can specify all the parameters needed by VRTX for a particular configuration.

A location in the system points to the base of the configuration table, and one vector in the EVT (or IVT or NPSA) points to the system's entry point. These two pointers are the only links between VRTX and the board. Values in the configuration table specify the beginnings of system random access memory (RAM) and user RAM; the length of user memory; the maximum number of active tasks; and the location of any special routines to be invoked upon task switch, task create and delete, or system initialization. Fig 2 shows these relationships. Since VRTX is supplied in ROM, it does not require any particular development system for its configuration or its linkage to user programs. ROM can be located anywhere in the user's address space, since it is written entirely in position-independent code. The system acts

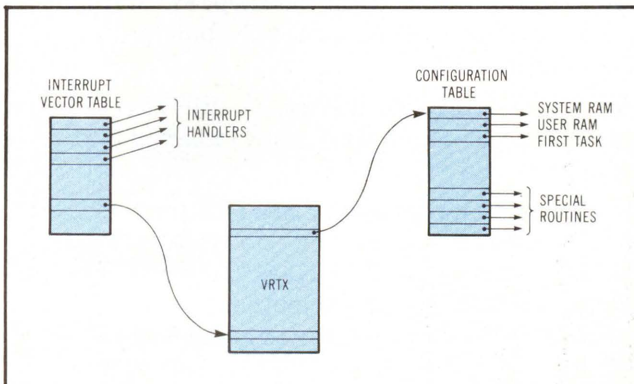

Fig 2 System configuration requires programmer to supply only one address that connects operating system to application. User supplies configuration table.

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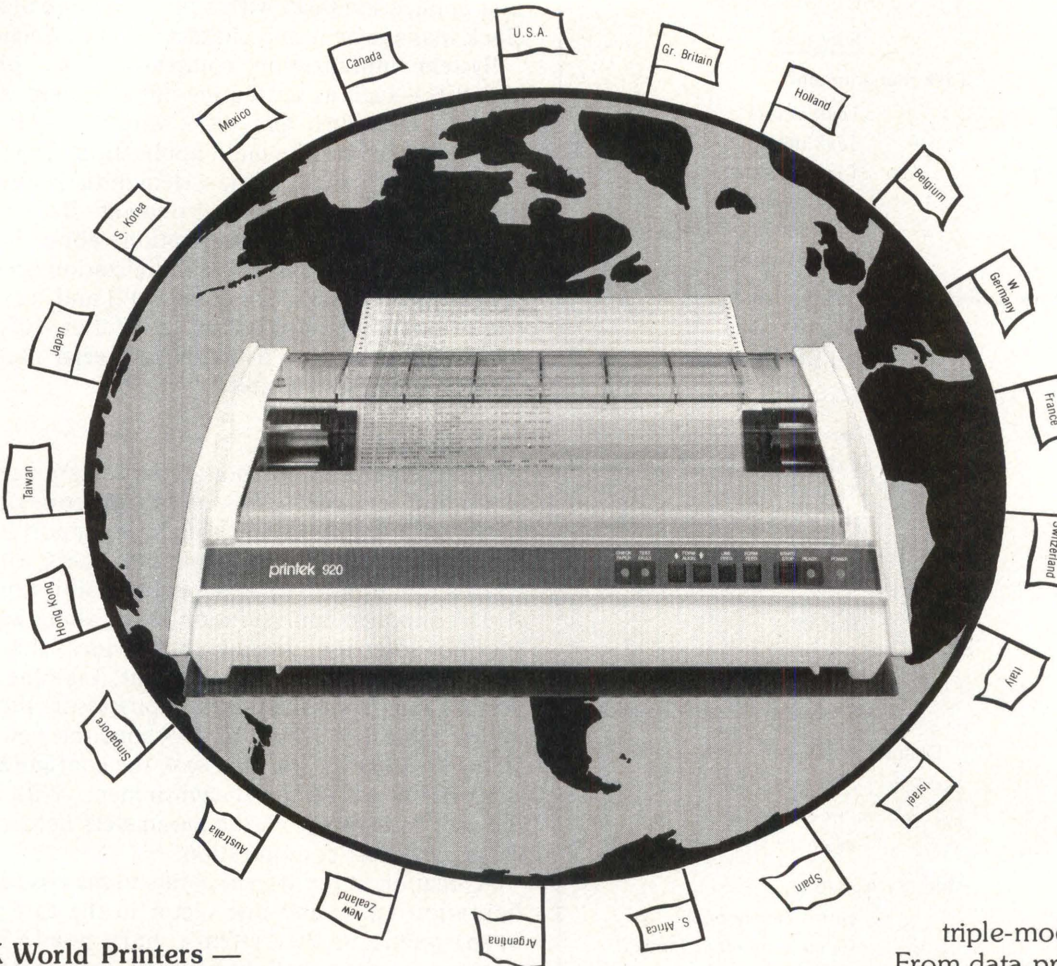

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A software component

Although the operating system supplies much of the system software requirements for most embedded microprocessor applications, it does not contain all the code that might be found in an operating system tailored to a specific microcomputer board. Users with special I/O devices may want to add special system calls to support their devices. For example, if the system includes a local area network (eg, Ethernet), certain communications primitives (eg, send and receive) can be implemented with user defined system calls, which can be added without any modifications to the ROM nucleus. Adding a system call handler is simply a matter of adding a 1-word pointer to the IVT or EVT (or the configuration table on VRTX/8002). It is unnecessary to obtain VRTX source code, even when extending the system.

The system is easily extended by adding values to the configuration table to specify user routines for initializing special devices at system startup, or for saving the states of custom devices on task switches. For example, if a floating point processor exists in the system, it will be necessary to save floating point registers when executing a context switch. Other operating systems do not offer a simple method of adding user save routines and initialization routines to the system scheduler. Most systems cannot be extended without modifying the source code—an expensive and risky operation.

Other extended state devices that could be added to a VRTX system include a memory management unit and a fast Fourier transform for signal processing applications. In each case, the extended state can be saved in a task control block extension and manipulated by user code that is activated during task create, delete, or swap processing.

Another example of a user defined VRTX extension is special code that is run when tasks are created to set up the runtime environment of a high level language (eg, to allocate stack frames of a particular size). Tracing and debugging can also be implemented with VRTX extensions. For example, user supplied code can be activated upon each task swap to record the identification of each task run, thus generating a usage profile.

Increasing the responsiveness and flexibility of realtime control systems is no easy task. The secret lies in the software, however, and designers, endeavoring to customize control systems, can simplify the software side of their lives. By viewing their operating systems as a collection of standardized software primitives, designers are able to pick and place operating system components as they would hardware. Gaining independence from the restrictions of specific hardware configurations will allow designers to place emphasis on perfection rather than patching.

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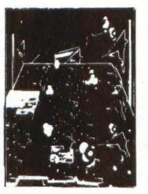


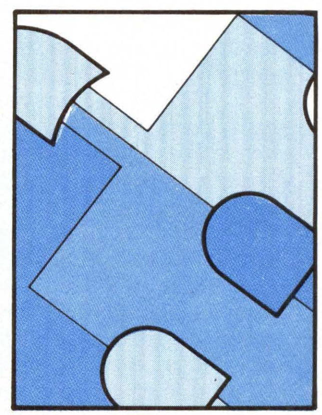
FAULT TOLERANT SYSTEMS CAN PREVENT TIMING PROBLEMS

Reliable control systems that incorporate hardware redundancy create special problems for the designer. System voting must be synchronized so that data rendezvous are on schedule.

by John H. Wensley

Computers are used increasingly in control, monitoring, and safety applications in large industrial plants. It is therefore imperative that they survive faults in their individual components. The system must carry out control applications correctly even when individual components fail. Design of such a fault tolerant system can, in theory, allow for many internal faults without external malfunction. Economic considerations, however, usually necessitate that the system be designed to withstand one or two faults. In most fault tolerant systems, the objective is to guarantee survival after a single fault. Such a system will usually tolerate many combinations of a larger number of faults but with more limited guarantees.

A major reason for using computers in control and monitoring is flexibility of operations. For example, a computer enables one to change the conditions of the plant during operation. This action may be in response to some external stimulus, such as a change in composition of raw material. Another factor favoring computerization is the improved man/machine interfaces made possible by sophisticated and highly flexible graphics terminals. Such terminals allow the operator to examine the state of a process and modify it if necessary. Another factor related to computer control is the rapid cost reduction in computerized control systems. Advances in semiconductor technology allow greater capability while decreasing overall control cost.



Large industrial plants are placing increased emphasis on productivity. Production per man-hour is the classic measure of productivity. Other measures are also becoming highly important, such as production per unit of raw material, or production per invested dollar. These factors require sophisticated control algorithms that, in turn, demand the computing power of a modern, digital computer to carry out control.

John H. Wensley is founder and chairman of August Systems, Inc, 18277 SW Boones Ferry Rd, Tigard, OR 97223. Prior to this, he directed a project at Stanford Research Institute to develop software implemented fault tolerance. Mr Wensley is a published expert in software and fault tolerant technologies, and holds a BA and an MA in mathematics from Cambridge University, England.

Modern industrial plants also require complex control procedures. These are evidenced by the need for certain control actions to be executed at specific times. In other cases, this complexity is due to interaction between what were once individual elements of the control system. Another factor contributing to system complexity is the increased use of sophisticated algorithms in control loops. When the computer system is also used for alarms and safety shutdown, the critical nature of industrial processes becomes evident. Such contingencies frequently require interaction between process variables such as pressure, temperature, and flow rate of a raw material. These interactions are yet another factor in sophisticated computerized control systems.

The effects of failure in a control system vary immensely in each industrial plant. Potential failed control in nuclear power plants threatens lives, and downtime in an industrial plant poses severe economic penalties on corporations whose cost margins may be narrow. In the field of food and drug preparation, the risks of improper control are obvious: they may produce undesirable effects and health hazards. Another area requiring correct operation is in computerized security systems. Finally, the need for correct control also affects the convenience and comfort of everyday life. The most obvious example, electric power generation and distribution, requires reliable operation to prevent discomfort and disruption to a large number of people.

The malicious fault

Many everyday systems, such as multiple elevator cables and dual braking systems in automobiles, are designed to tolerate faults. In both instances, the fault being tolerated can be predicted; in the case of the elevator, it is the breaking of one of the cables; in the automobile braking system, the fault is a leak in one of the hydraulic systems. Modern digital electronics are so complex that the behavior of components cannot be predicted when a fault develops. This complicates both the design of the system and the analysis of its behavior.

It is theoretically possible to observe fault modes of components that have been used in large quantities or for a long period of time, and to design the system to protect against these occurrences. Such a view, however, presents very practical difficulties. First, there is the operational complication of recording all the faults that occur. Second, there is great economic pressure on a digital system designer to utilize new circuitry. This is primarily due to the increased rate of progress and also the continued reduction in cost of large scale integration circuits.

Therefore, the system must be designed to tolerate faults that are of an unknown type. If fault tolerance of the system is to be guaranteed, it is impossible to make any assumptions concerning the faulty behavior of the components. Further, the system must be designed to tolerate malicious behavior such as a faulty component that attempts to corrupt the correct behavior of the remaining good circuitry. Any system designed only to tolerate certain assumed failure modes may indeed be reliable, if the designer is very clever or very lucky, but that reliability cannot be guaranteed.

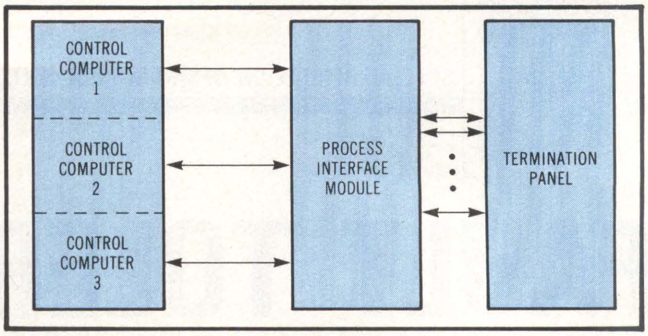


Fig 1 Fault tolerant computer architecture of August 300 system. Three computers analyze each other's results via read only data link.

Fault tolerance

All fault tolerant schemes rely on certain fundamental principles. The first such principle is to incorporate redundant equipment into the system, ie, equipment that would not be used if components could be guaranteed fault-free. Fault tolerant schemes vary in the way they incorporate and manage redundancy.

Perhaps the most important factor in incorporating fault tolerance is the ability to guarantee fault isolation—the ability to prevent any effects of a fault in one unit from propagating to another. If isolation cannot be guaranteed, redundancy has limited value, because redundant equipment can be corrupted.

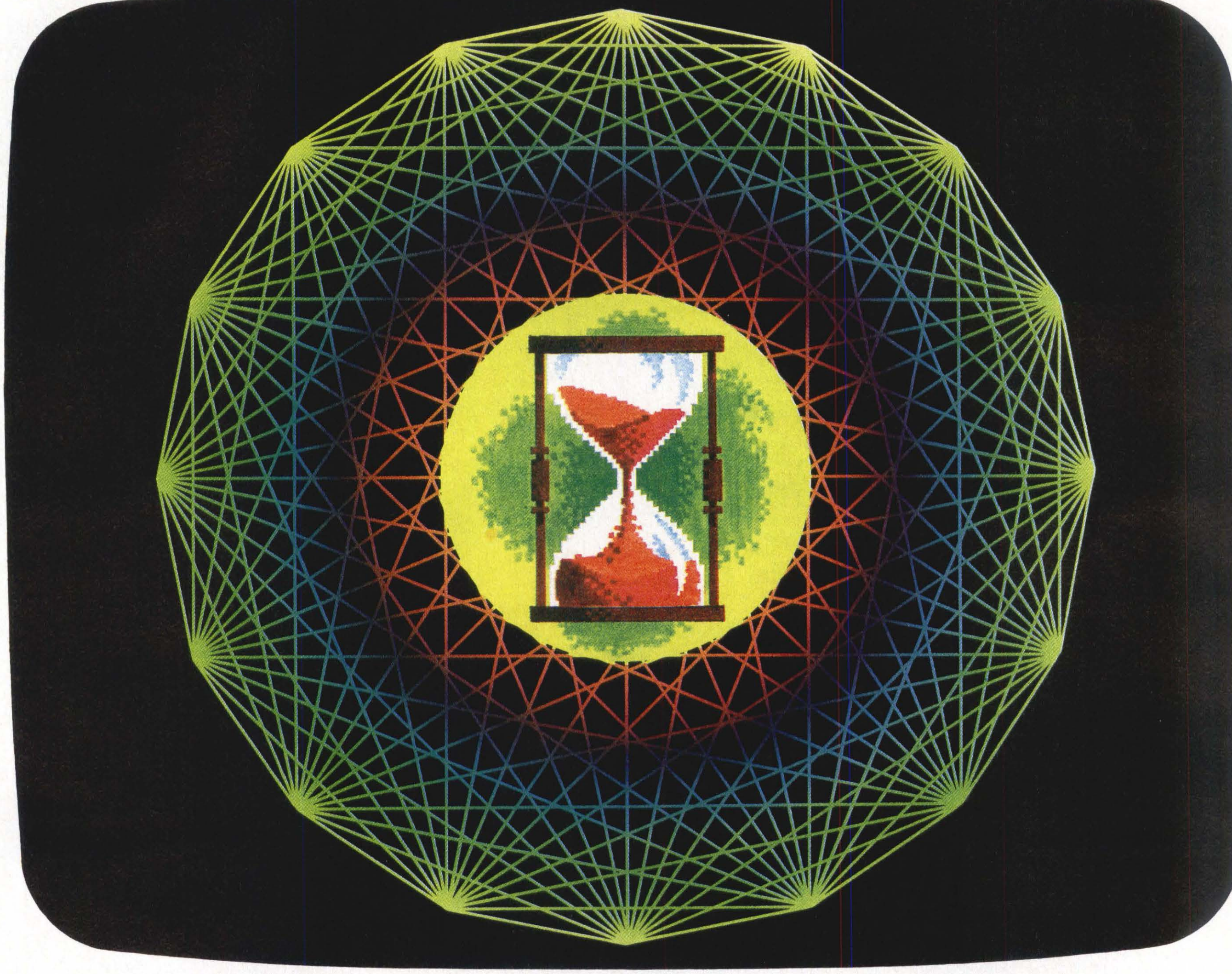
Fault tolerant computer systems employ varying hardware and software techniques to manage redundancy. The immediate and obvious advantage of using hardware schemes is that, in general, redundancy management is quicker. An example of such techniques is the use of error correcting codes in computer memories. Such codes provide limited fault tolerance by correcting a small number of errors in the memory, without any degradation in system speed. The advantage of software schemes in managing fault tolerance is their extreme flexibility. This flexibility results in a better match between a fault tolerant control system and a particular application.

Fault tolerant control computer

August Systems' series 300 fault tolerant control computer is illustrated in Fig 1. At the heart of the system are three independent computers, each capable of providing all the control required for the process. The principle of operation is that all three computers independently carry out the control algorithm calculation. If a fault occurs in one of the units, then the other two dominate the faulty unit and prevent it from having any erroneous system effect.

For internal computational actions, each computer can independently read results of the other computers' calculations and compare all three values. Thus, if one is in error, it becomes immediately apparent and can be corrected. This reading of data from the other computers is carried out through a read only communication link between them. Read only communication ensures that a faulty computer cannot damage valid data in the other computers. Thus, the principle of fault isolation can be preserved.

When data have been obtained from the other computers, each computer carries out a comparison and, if necessary, makes a correction. This comparison and



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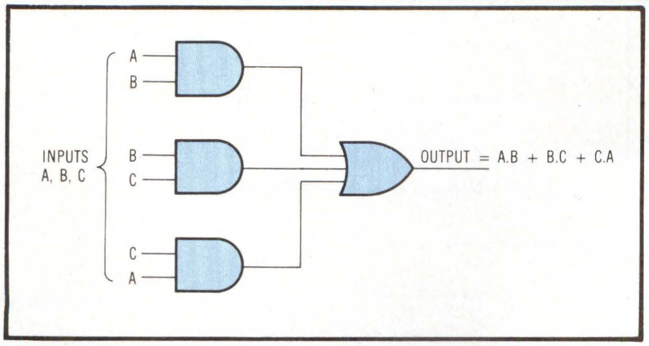

Fig 2 Simplified hardware voting scheme to achieve fault tolerant data. Such a scheme does not prevent faults internal to voting circuit from producing errors.

correction is implemented in software. As noted, the advantage of this software technique is its flexibility. For example, if the data being compared are derived from analog sensors, it would not make sense to expect identical values from correctly functioning computers. By using software to carry out this comparison, it is possible to determine if two values are acceptably close to each other, even though the data representing those inputs may, on a bit by bit basis, be different. Such flexible comparison or voting techniques are difficult to provide using hardware comparison techniques.

In addition to the three central control computers, means must be provided to interface the computers to the plant being controlled. This interfacing is carried out in one or more process interface modules (PIMs). The essential provision of fault tolerance in the PIMs is by two basic techniques: one for input of data from the plant, the other for output of data to the plant.

Data input from the plant to the computers are made fault tolerant by providing three independent interfaces, one to each control computer. The control input is fed to each of the three interfaces. Thus, each of the three control computers can independently read data from sensors through independent interfacing electronics. Provisions are made for such data to be in digital, analog, or other commonly used forms, such as pulse count or pulse width.

Computer output is a more complex operation. It is indeed simple to take data from three control computers and to vote that data via hardware voters. One such scheme is illustrated in Fig 2. Such a simplistic voter designed for discrete data does not, however, survive possible internal faults within itself. Thus, it is necessary that the voter within the PIM be designed in accordance with two principles: it should be able to derive an output, which is the same as the two correct outputs, from two good control computers and ignore data from the third, faulty computer; and it should not corrupt the output in the event that it experiences an internal fault.

Management of these fault tolerant features is carried out by the same operating system that provides conventional operating system features, such as scheduling, dispatching, and handling interrupts. The operating system design is also based on two principles. First, the operating system should make fault tolerance management transparent to the user. That is, the control engineer who uses the computer need not be concerned with aspects such as voting, communication, comparison, and correction of data. These tasks should be an automatic function of the operating system. Flexibility

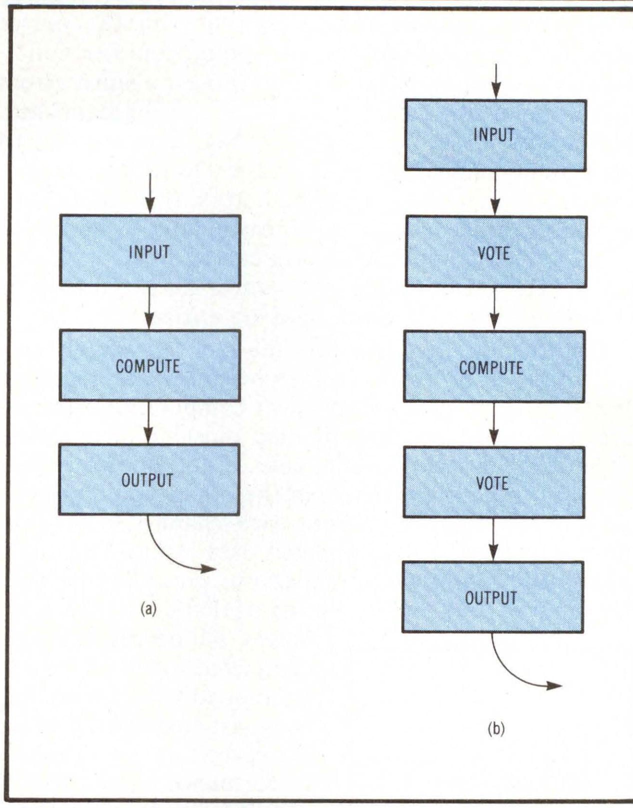

Fig 3 Typical control program sample loop in (a) can be modified to perform voting operation associated with fault tolerance (b).

is the second principle upon which the operating system is based. The system can be used in many different application environments. As mentioned, this can include different aspects of the control system—control, monitoring, safety shutdown, and alarm. Flexibility should also be possible over a wide range of applications such as chemical reactors, steel mills, oil refineries, and power stations.

Rendezvous and synchronization

In many fault tolerant computer systems, the application program or task designer must be aware of the fault tolerance techniques. In some cases the designer must consider the details of procedures employed for error detection, error correction, fault diagnosis, voting, reconfiguration, etc. A firm design requirement specified for the series 300 was that the application programmer need not be concerned with the details of these procedures. This requirement implies that the application program be incorporated into the operating system so that it can run from start to finish without any interaction with the fault tolerance procedures.

Note that programs for control tasks are repetitive and designed according to the scheme shown in Fig 3(a). During the first phase, all data from sensors are read. During the second phase, the necessary control algorithms are executed, followed by the third phase of output to actuators. Typically, for each task, this scheme must be accomplished in a fraction of a second. When voting is required, it takes place after the input of data. Voting is intended to remove any errors that occur due to faults in the sensors, or in the computer interface to the sensors. At the end of this first voting procedure, all good processors (ie, those that are not faulty) have the same view of input data. They then carry out the control algorithm computation. At this point, another voting takes place, which is intended to protect against errors that occur in the calculation of the control algorithm. Following this second level of voting, data are sent to the actuators. Because it is necessary to protect against faults in the interface to the actuators, this output process incorporates voting that is carried out by hardware [Fig 3(b)]. The application task can be written without any concern for voting procedures except that it is necessary to specify which data are critical.

Fig 3(b) does not illustrate the fact that certain synchronization or rendezvous procedures are required. When three or more independent computation channels are employed, the input of data must be separated in time from the voting of that data. If not, one processing channel operating faster than the others could attempt to vote the input data from each channel, before the slowest channel had completed data input. Thus, it is necessary to interpose a rendezvous procedure between the input of data and the voting of that data. This guarantees all processors have completed input before any attempt to vote. Of course, no guarantee can be made about the faulty processor's performance, but that is handled by the voting process itself.

Following computation, it is again necessary to vote on all critical data. Computation of results must also be isolated from the voting of those results, so that voting is not attempted by the fastest channel before the slowest one has computed its results. Thus, there are several places in the computation scheme where each processor must be brought to the same state as other processors, ie, a rendezvous must be accomplished. This rendezvous is frequently referred to as synchronization. In the series 300, no distinction is made between rendezvous of processors carrying out a computation and synchronization, which is achieved against an external standard, such as a realtime clock.

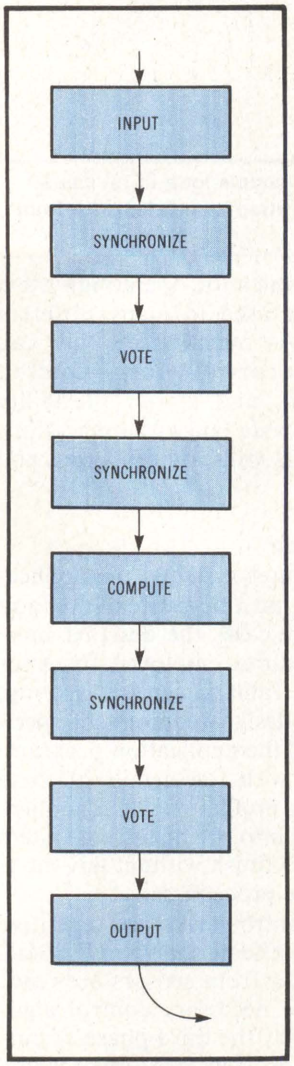

Fig 4 Control program flow incorporating processor synchronization. Periodic rendezvous of redundant elements eliminates errors due to timing or sampling discrepancies.

Fig 4 illustrates the complete computation scheme with the appropriate rendezvous, or synchronizations, incorporated. The goal in designing such systems is to achieve synchronization between good processors even if one is faulty. Further, modern digital computers are so complex that it is impossible to predict a faulty processor's behavior. The only meaningful guarantee is one that assures system behavior in the presence of the most malicious fault in a processing channel. Such a malicious fault is deemed to be one that produces results that could force good processors to produce incorrect results.

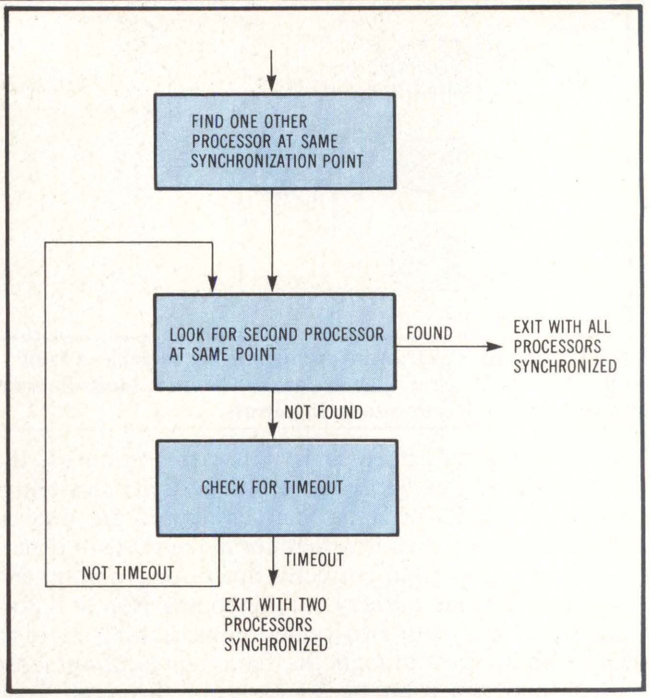

Fig 5 Basic synchronization scheme used to keep processors functioning concurrently. Timeout allows each processor a finite wait period if catch-up is needed.

A basic scheme used for synchronization is illustrated in Fig 5. Each processor reaches a particular synchronization point in its program, at which time it determines if the other processors have arrived at the same place. If it has succeeded in doing so with one other processor, then it attempts to find the third processor at the same point, but only carries out this attempt for a limited time. The third processor may be faulty and not arrive at the same synchronization point. Such a circumstance should not prevent the other processors from correctly continuing the computation.

The problem of bringing two or more independently operating computers to the same point in program execution simultaneously has been studied by many researchers. Much of the computational context of this work has been one in which several computers may be executing different sets of programs and may, from time to time, have to come to a commonly agreed point in the programs before some cooperative action is carried out. Many schemes for achieving this rendezvous are expressed in programming language constructs. The earliest proposal, by Conway, used the constructs fork and join. A programmer used the fork construct to indicate that two or more processors could commence independent operations. Join was intended to express that two or more processors should all reach the same point before continuing. Any processor that reached this point before the others should be forced to wait.

This concept of controlling a rendezvous between processors was intended to express the programmer's

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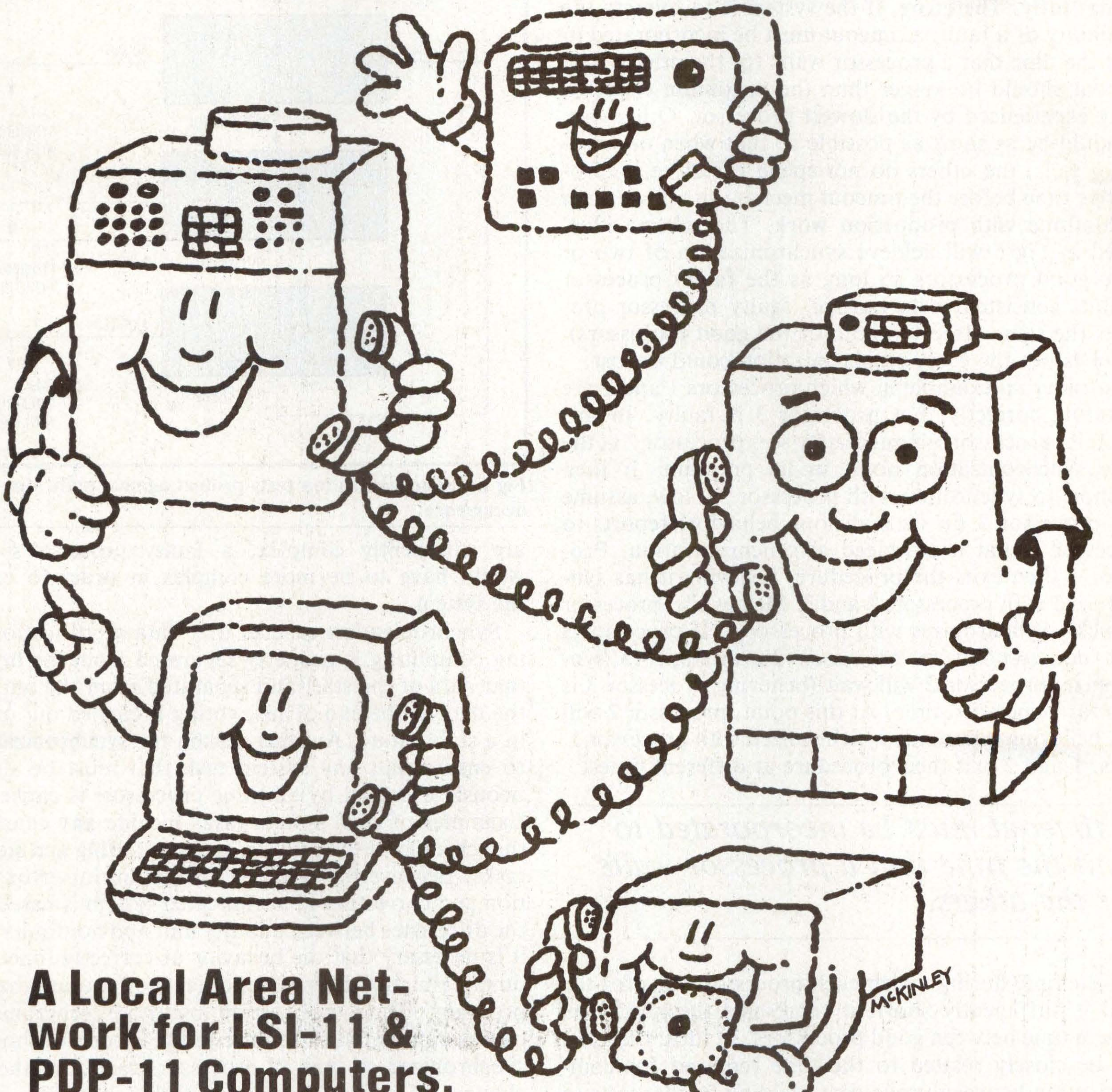

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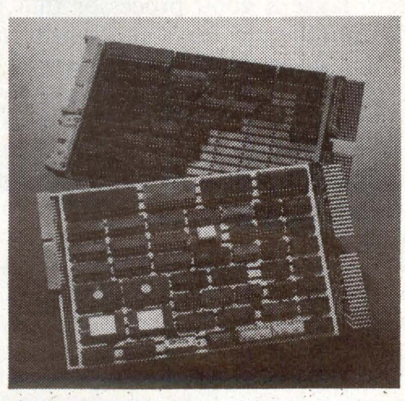

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CIRCLE 121

intent. A fault tolerant system must implement these constructs even if one of the processors is at fault. For example, in a conventional join, an early processor would wait until all others had reached the same point, but in a system where a processor may be at fault and never arrive at its join instruction in the program, this would cause all others that are waiting for it to hang up permanently. Therefore, if the system is to tolerate the possibility of a fault, a timeout must be incorporated to limit the time that a processor waits for the others. The timeout should be longer than the maximum expected delay experienced by the slowest processor. Otherwise, it should be as short as possible so that when one processor fails, the others do not spend excessive, unproductive time before the timeout mechanism allows them to continue with production work. The scheme illustrated in Fig 5 will achieve synchronization of two or three good processors so long as the faulty processor exhibits consistent behavior (ie, faulty processor produces the same effect on both of the good processors). If this is not the case, synchronization could be lost.

Consider an example in which processors 1 and 2 are operating correctly, but processor 3 is faulty. In this example, processor 1 immediately sees processor 2 at the same synchronization point in its program. It then attempts to synchronize with processor 3. Now, assume that processor 3 (in its malicious behavior) reports to processor 1 that it is indeed at synchronization. Processor 1 then exits the procedure, believing it has synchronized with processors 2 and 3. Meanwhile, processor 2 quickly synchronizes with processor 1. If processor 3 does not respond to processor 2's attempt to synchronize, processor 2 will wait (believing processor 3 is late) for a specified time. At this point, processor 2 will exit, believing it has only synchronized with processor 1. Thus, 1 and 2 exit their procedure at different times.

A timeout must be incorporated to limit the time that a processor waits for the others.

If the time during which each processor waits for the third is sufficiently short, it represents the maximum skew in time between good processors. In turn, the skew will be closely related to the time required for communication between processors. Adding further tests to the synchronization procedure resolves this problem. These tests cause a good processor that has synchronized with another to leave the synchronization procedure if that other processor also leaves. Thus, if the maliciously faulty processor attempts to confuse the good processors, it will fail to do so, because they will both exit the procedure at close to the same time (Fig 6).

An extremely malicious processor can possibly confuse such a scheme. The behavior pattern of such a processor would, however, have to be very complex. That processor would first appear to synchronize with one other and then to leave its synchronization early so that the other processor does also. Meanwhile, to the third processor, the faulty one must appear to not synchronize so that the third processor is delayed waiting for synchronization. Such a behavior pattern of a faulty processor is highly unlikely. If the tests for synchronization

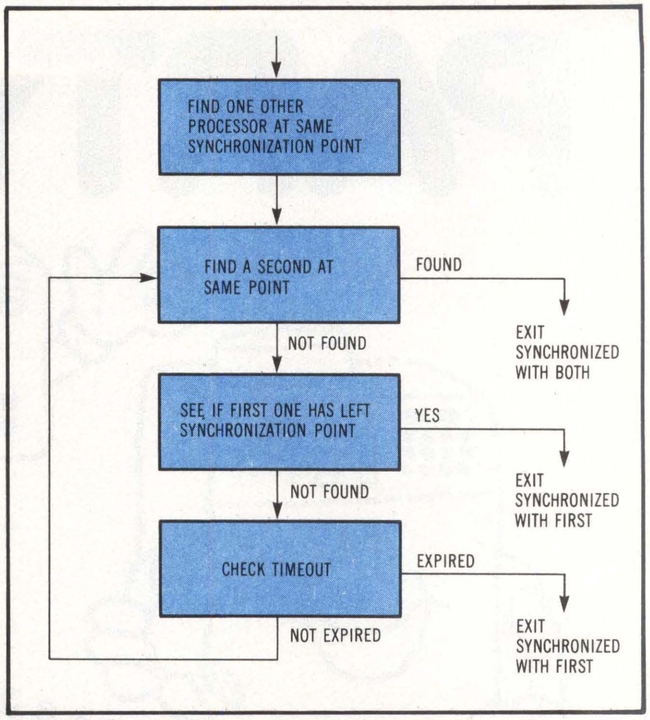

Fig 6 Synchronization tests protect against malicious fault occurrence.

are sufficiently complex, a faulty processor's errors would have to be more complex in order to confuse the system.

Synchronization ensures that data modification during computing is properly separated from the input of that data at the start and separated from the output of the data at the end. Thus, voting is carried out on data in a stable state. Another reason for synchronization is to ensure that any system task that must be simultaneously executed by all three processors is carried out. Examples of such system tasks include any changes to the scheduler or dispatcher, such as starting and stopping tasks. Because the principal technique for error detection and correction in a triplicated system is based upon the difference between a faulty unit and nonfaulty units, it is necessary that the behavior of correctly functioning units be highly deterministic, ie, they execute the same program. Thus, any action by those programs that causes a potential difference in the execution should be synchronized so that all processors carry out the same changes. Clearly, changes in task scheduling or dispatching represent places where there are potential changes in execution. Therefore, synchronization must be incorporated.

Some operating systems allow direct interaction between different tasks. For example, one task may initiate another while causing itself to be terminated. Such direct interaction requires that all processors be synchronized. A preferable solution is to base such system actions on message exchange so that the processors have independent control over their own execution stream. If one task must interact with another, message exchange between the tasks can make any required changes. This message exchange enables the mechanism that passes messages to be used for all possible changes. Therefore, synchronization is only required when messages are passed. This greatly simplifies the overall operating system design.

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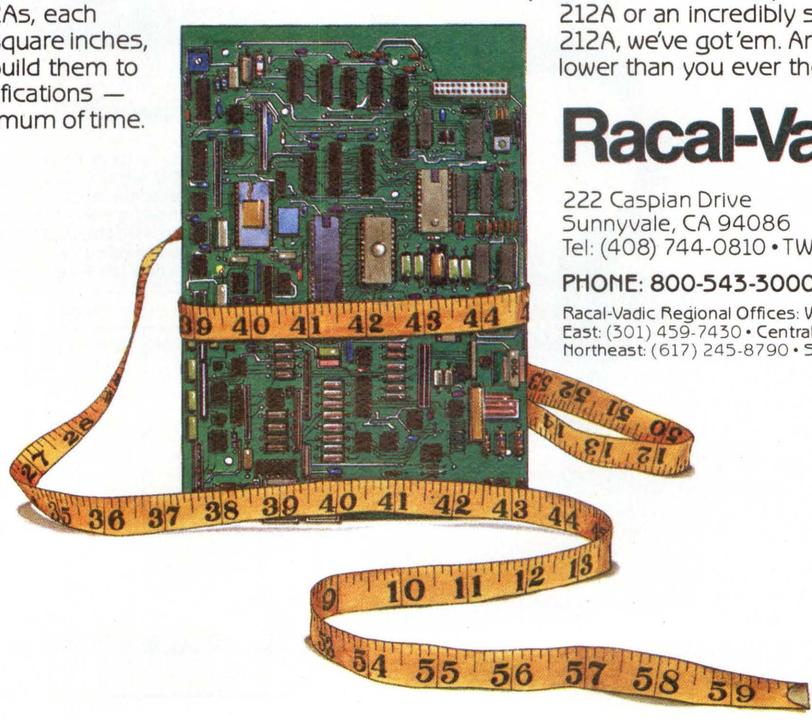

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CIRCLE 122

Synchronization is also required in interrupt handling. In most realtime computer systems, interrupts are allowed. An external device can signal the computer system that an event has occurred and that new tasks should be initiated or old tasks terminated or interrupted for a short period. It is necessary that such execution stream changes be synchronized over the three processors. The technique used is to attempt synchronization immediately following an interrupt. All good processors will be at approximately the same point in their program, and each will have received the same set of interrupts.

It is possible to devise schemes whereby all good processors respond to the same set of interrupts.

It is possible that two processors may differ slightly, in that one has received more interrupts than another because of the slight timing differences of the interrupt circuits. If a delay is introduced, the slowest processor has a chance to field an interrupt to which the fastest processor has already responded. Of course, the fastest processor may receive yet another interrupt, so that the execution of this delay needs to be carried out repeatedly until all processors have received the same set of interrupts. This sampling must be carried out at close to the same time in each processor. This is achieved by using the synchronization procedure. In this way it is possible to devise schemes whereby all good processors respond to the same set of interrupts.

An extreme case of responding to an interrupt is evidenced by a realtime clock system that causes such an interrupt. Using the techniques described, it is possible for all nonfaulty processors to respond in an identical fashion, thereby assuring that each one has the same view concerning real time.

Synchronization is an important element in a fault tolerant control system. Simplistic schemes have the potential for incorrect operation unless they are designed to protect against the most malicious faults.

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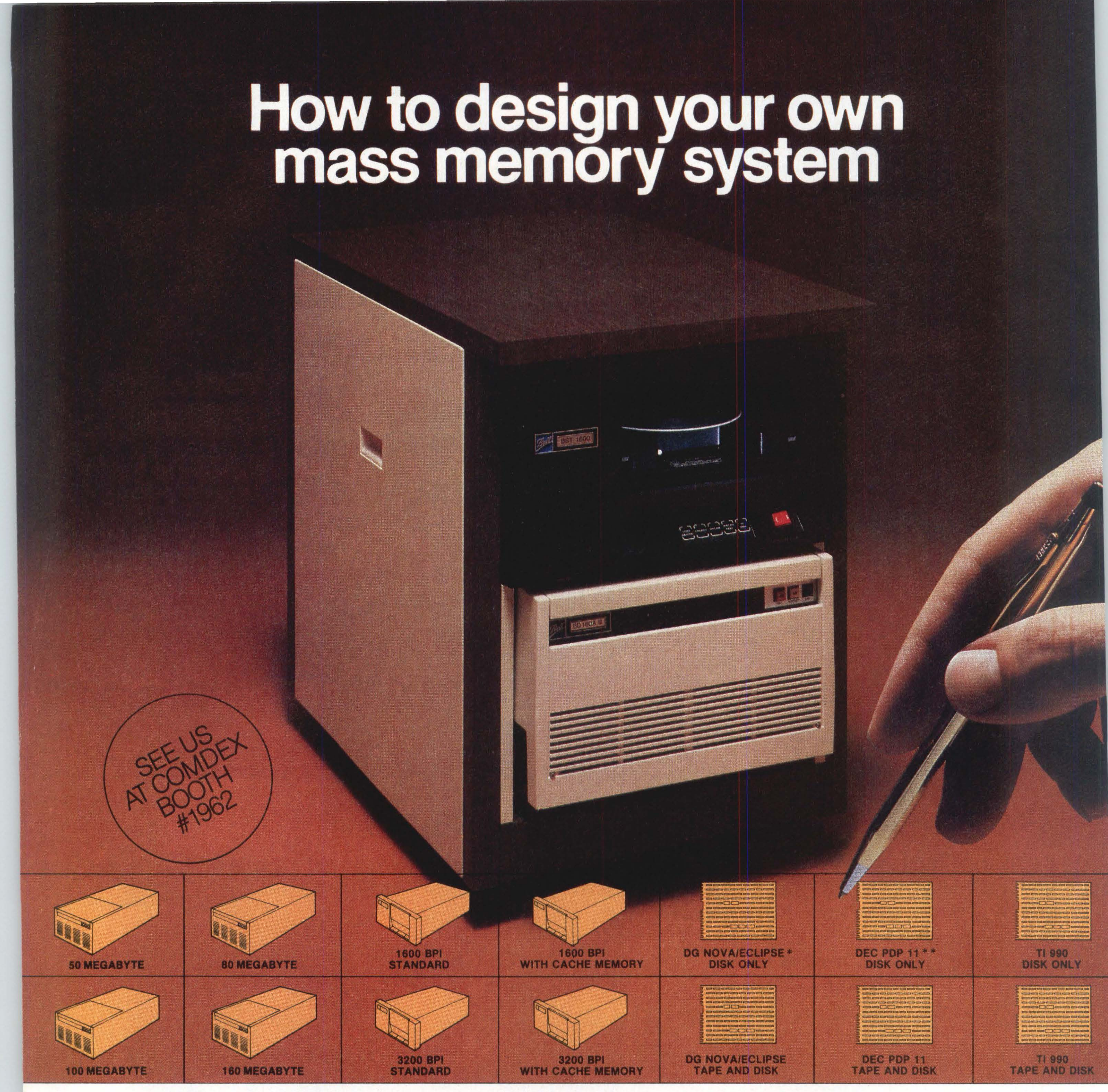

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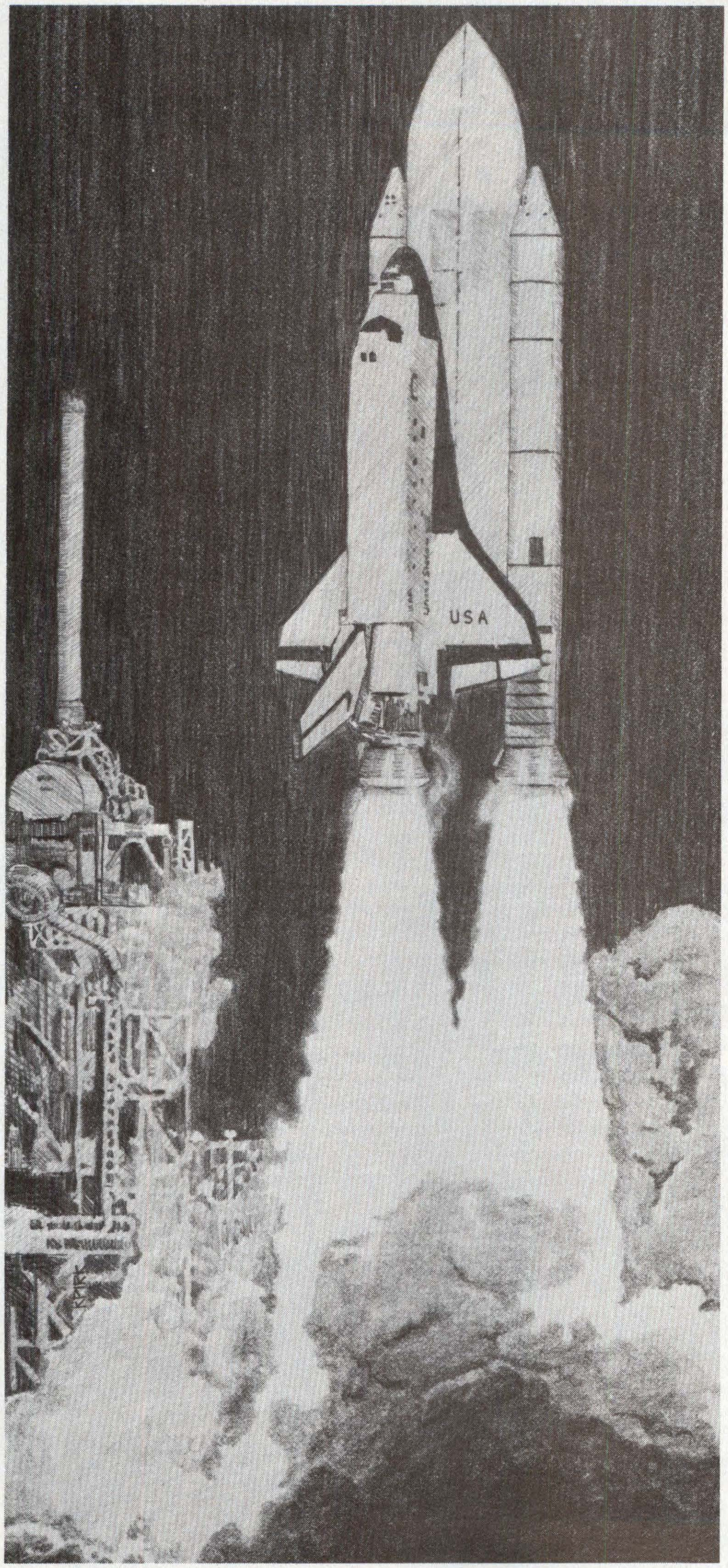
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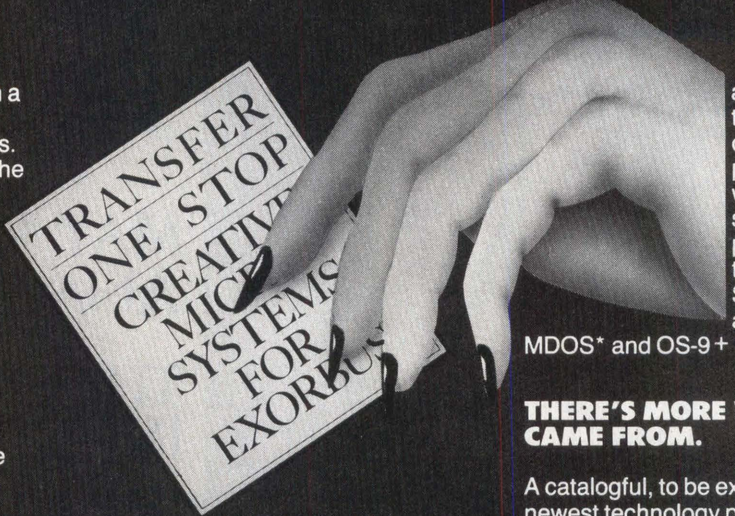

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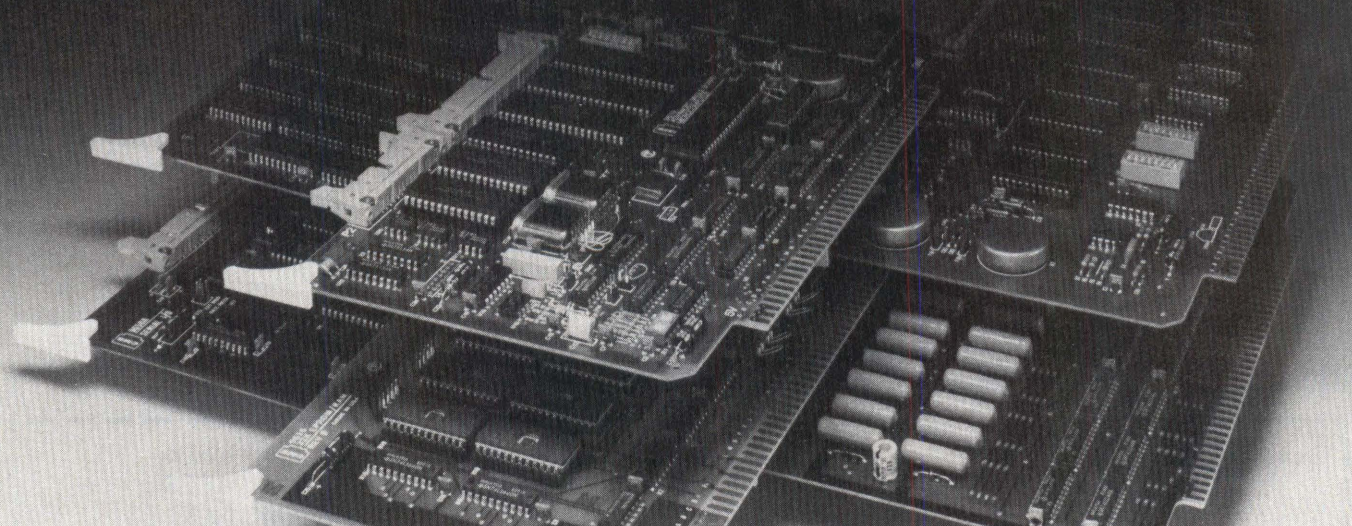

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CIRCLE 130

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Software is MP/M-86, a multitasking superset of CP/M-86. All software used on earlier Macsym units will function on the latest version, but Macsym 350 software will not function on earlier systems. This compatibility also provides access to a large library of third-party software, including FORTRAN and Pascal. Process parameters can be changed in real time from the keyboard without interrupting program execution. A software based password system prevents unauthorized access to keyboards.

Macsym 350 consists of two subsystems as illustrated in the photo and in the block diagram: a system console and an intelligent measurement front end. The two subsystems function with as much as 1000′ (305 m) separation. Usually the system console will be located in an office or other relatively clean environment, while the front end might be on the factory floor. Because temperatures in the factory or shop may vary widely within short time periods, the front end calibrates itself every 5 min to adjust to any temperature changes. The self-calibration is fully transparent to the user since all readings are corrected before being sent to the system console. Calibration can also be user initiated by a software command.

The system console includes CRT, Intel 8086 16-bit CPU, 5-MHz processor clock, 8087 math coprocessor, 128k bytes of RAM, intelligent graphics controller, floppy disk, keyboard, and communications controller. Six I/O slots allow for addition of communication and memory options (up to 1M byte of RAM). Hamming code error correction circuitry is one of the options, particularly useful in a noisy factory environment. A single, 1-sided, 5¼″ floppy disk drive with 320k bytes unformatted is standard; a dual-drive is optional.

Although the standard CRT is a 12″ (30.5-cm) unit with green phosphor, an RGB color monitor is available as an option. In text mode, the CRT displays 24 x 80 characters in a full ASCII set. Blinking, underline, and reverse video are standard. There is also a graphic character set. Graphics capabilities are 640 x 240 pixels on both standard and 8-color units. Communications are via RS-232/422 and 20 mA, IEEE 488.

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(continued on page 229)

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ZU-1601	IS01 (IATA)
ZU-1602	IS02 (ABA)
Magnetic Encoders	
ZU-2401	IS01 (IATA)
ZU-2402	IS02 (ABA)
Automatic Magnetic	
ZU-1507	IS02 (ABA)
ZU-1521	IS01 (IATA)
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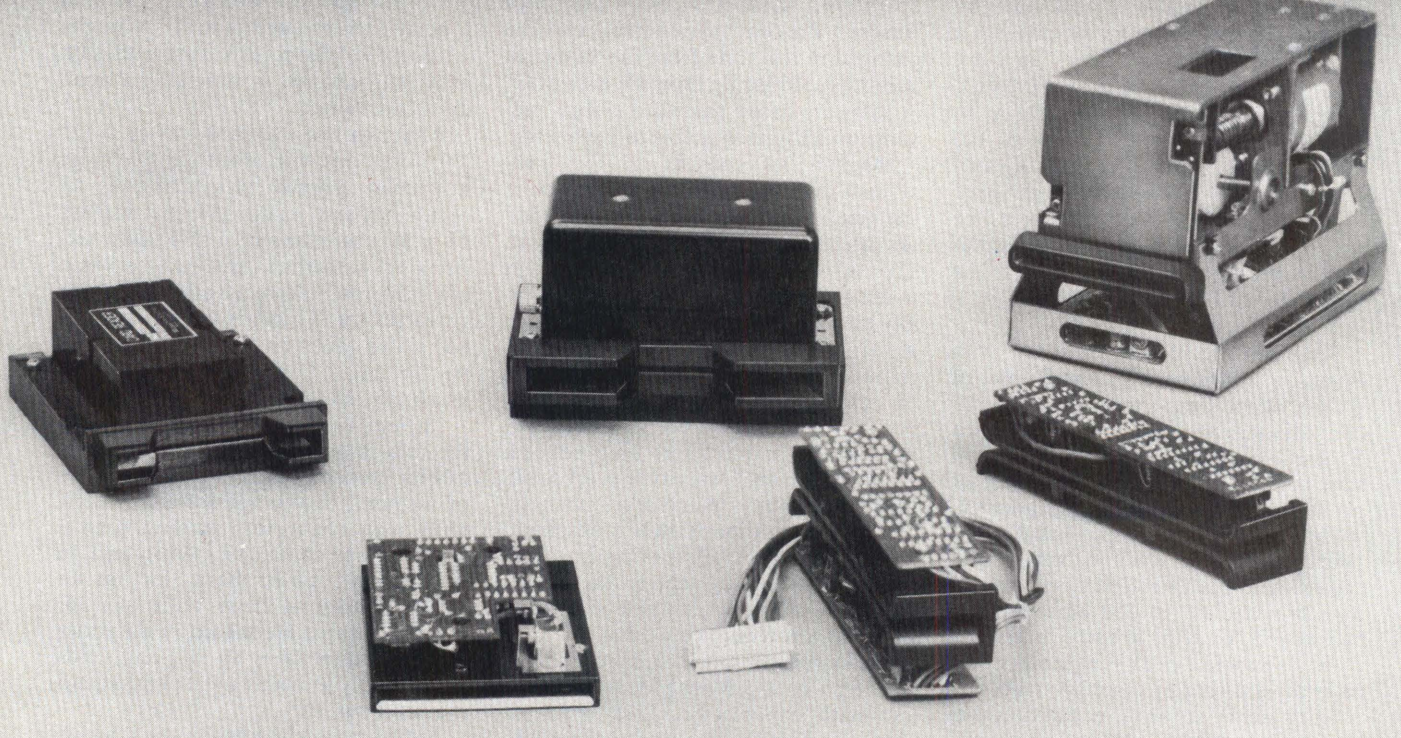

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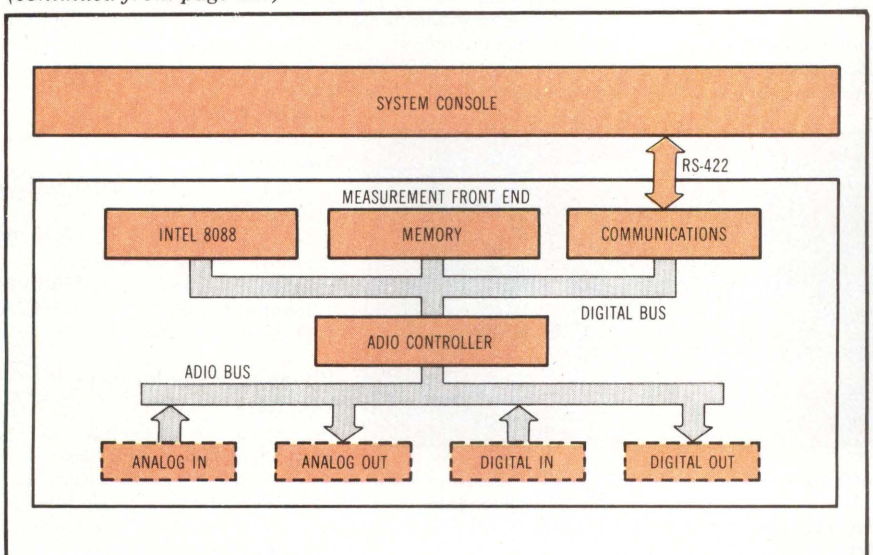
SYSTEM COMPONENTS

Factory automation control system
(continued from page 227)



Block diagram of Macsym 350 measurement and control system. Library of 32 different I/O cards is available for attachment to ADIO bus.

noise off the low speed bus. A-D converter modes are integrating, for 16-bit resolution and improved noise rejection, and successive approximation, for high speed acquisition with 12-bit accuracy. Overall converter accuracy is 12 bits with 0.012% nonlinearity. Conversion speeds are 1 line cycle period integrating (16.6 ms for 60-Hz, 20 ms for 50-Hz line frequency), 25 μs for successive approximation. Sampling rate in successive approximation, burst mode is 33 kHz.

I/O cards include isolated and non-isolated analog and digital inputs and outputs, IEEE 488 controller, RS-232/422 and 20-mA current loop communications, speech synthesis, interrupt, setpoint alarm, strain gage, thermocouple, RTD, mA, mV, V, and other I/O designed for direct connection to process control equipment, product test instrumentation, signal sources, and actuators. A system will accommodate up to 512 channels.

Environmental range for the system console is 0 to 35 °C, 0 to 90% relative humidity (RH) noncondensing. For the front end, the range is 0 to 50 °C, 0 to 95% RH.

The basic Macsym 350 system, without optional extensions, is priced at less than $10,000. Demonstration units are available immediately (several evaluation units are already in the field). Customer shipments will begin in February 1983, with delivery 90 days ARO thereafter. **Analog Devices, Inc**, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

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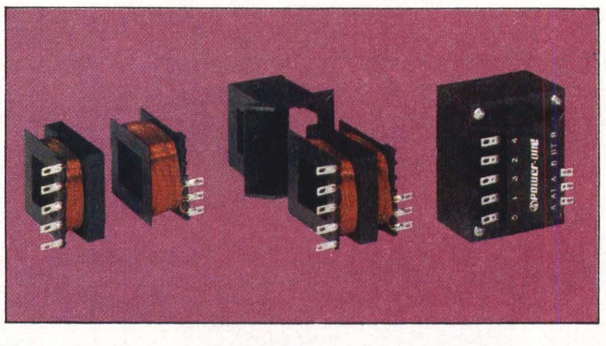
More and more countries are adopting tougher safety standards, but the International Series can be used anywhere, for almost any application. It meets the most important requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.



Power-One's patented International Series transformers feature separate, fully enclosed, primary and secondary coils. Meets safety requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.

How did we achieve this technological breakthrough? Take a close look at our power transformers. Our new patented winding process features separate, fully enclosed primary and secondary windings. This unique construction complies with the most respected safety standards, worldwide. These include:

Leakage Current,	
Line to Ground:	5.0 μa
Spacings,	
Live Parts to Dead Metal:	9.0 mm
Other Than Field Terminals:	5.25 mm
Dielectric Withstand Voltage,	
Input to Ground:	3750 VAC
Input to Outputs:	3750 VAC
Outputs to Ground:	500 VAC

Phone or Write for New Brochure

No way can we tell the full International Series story here, so we've prepared a new brochure for you with all the details. Send for it today, and see what it takes to set a new standard for the world!

"Innovators in Power Supply Technology"

POWER-ONE D.C. POWER SUPPLIES

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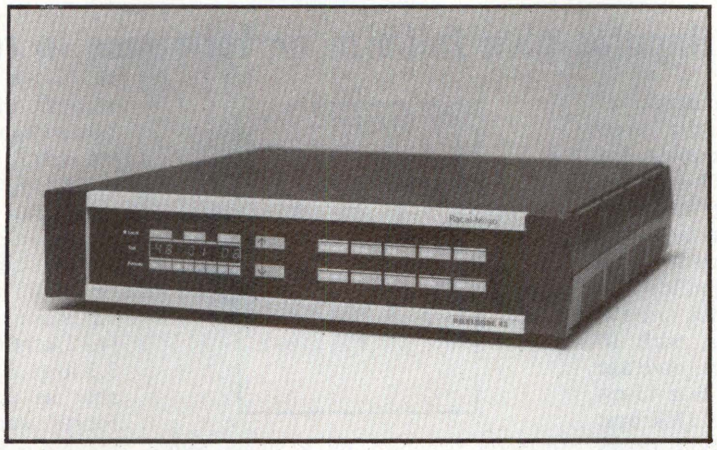
CIRCLE 133

4800-bps modem monitors and controls communications network



Omnimode 48, the first in a series of high performance modems, melds computer and communications technologies for significant advances in modem capabilities. The 4800-bps modem provides a wide selection of diagnostic and control features for improved network management, including a front panel control and information center that displays realtime modem and system performance data, and line and interface status.

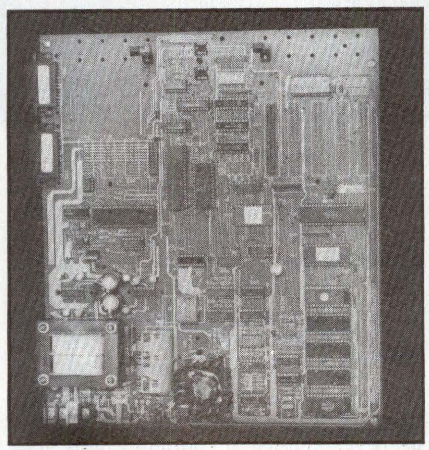
The front panel also controls selection and change of modem speed, port configuration, transmit level, strapping, modulation, and training method. The panel locks against unauthorized use or data interruption and allows authorized use via password entry. Firmware based for flexibility, the modem can operate in domestic data networks when software strapped as an MPS 48 or as an MPS 4827 for international CCITT V.27 compatible applications. Internal hardware straps are eliminated.

Extending these capabilities to remote Omnimode sites is the remote modem control (RMC) option. Modems on multidrop or point to point lines can have access to information and control center functions from the central site front panel without need for remote site operators. In addition to monitoring each remote modem from the central site front panel, alarms can be sent by the remote modems as critical network failure indications and displayed on the front panel. The RMC option also provides a "call" feature for message exchanges between remote and central site operators as an alternative to long distance calls. Built-in CCITT V.54 loop can test both the local and remote modems.

Available in 2- or 4-port versions that are backward compatible with the MPS 48 and MPS 4827, the multiport option allows port assignments of combined 1200-, 2400-, 3600-, or 4800-bps data rates up to an aggregate 4800 bps. Individual port interface monitor and digital loop can be performed locally without interrupting data on remaining ports. Each port can be individually monitored for status and looped for fault isolation from the front panel. Each port can also operate in switched carrier or dial-up mode via control signal simulation. When the multiport option is combined with the RMC option, active ports and their rates can be dynamically allocated by the Omnimode 48 for max bandwidth utilization.

Omnimode 48 operates on 4-wire point to point or multipoint unconditioned lines and is available for immediate delivery. Without options, it is priced at $3600. **Racal-Milgo**, 8600 NW 41st St, PO Box 520399, Miami, FL 33152. **Circle 267**

Single-board controller adapts to STD BUS data acquisition systems



A custom configurable, single-board data acquisition and control system, the IR-800 Leverage series can be used in applications ranging from a node in distributed processing networks to being embedded in small OEM equipment. The modularly designed measurement and control system is smaller than its functionally equivalent STD BUS system, and can be used as an STD BUS replacement.

Sixty percent of the 11" x 13" (28- x 33-cm) IR-801 board is permanently dedicated to application independent computer functions, including onboard power supply; Z80A CPU; 8 universal RAM/ROM sockets (64k max); 4 counter/timer channels; 2 configurable serial I/O channels (RS-232, RS-422, or current loop); and a debug monitor. A high speed arithmetic processing unit, power fail management system, realtime clock/calendar, and battery backup are options.

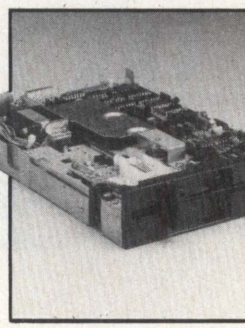
The remaining 40% of the board is dedicated to application dependent modules for analog signal conditioning, A-D conversion, and digital I/O. An onboard STD BUS connector allows use of previously designed and custom STD BUS functions. In small volumes and during application development, the modules are in plug-in card format and use Eurocard connectors. In production quantity, the modular circuitry can be etched directly onto the computer board to further reduce system size and cost.

Since target and development system environments are the same, the computer board also acts as its own CP/M development system. Typical development system problems, such as incompatible timing and I/O mapping constraints, are eliminated. A realtime, multitasking, BASIC type language in either ROM or disk based versions is provided. IMON debug monitor chains commands, delays, and repeats, and sets up I/O status routines. It can be used both as a comprehensive test system and debug tool, and as a simple application programming language.

Available for immediate delivery, typical prices for the series range from $600 to $1700, depending on configuration and quantity. **Ironics Inc**, 117 Eastern Heights Dr, PO Box 356, Ithaca, NY 14850. **Circle 268**

Half-height 5¼″ floppies give full-size performance in reduced space

Exactly half the height of standard 5¼″ Minifloppy™ disk drives, the SA455 48-tpi and SA465 96-tpi double-sided drives provide up to 500k-byte or 1M-byte unformatted storage capacity. The drives are media and interface compatible with industry standard SA400/450 and SA410/460 full-height Minifloppies. Track to track access time for SA455 is 6 ms, while SA465 is 3 ms, with 10 sectors/track for both drives. Average access time is 94 ms, including 15-ms settling time. Transfer rate is 250k bps; average latency is 100 ms. Both drives feature positive media insertion and direct drive dc motors that eliminate belts and pulleys.



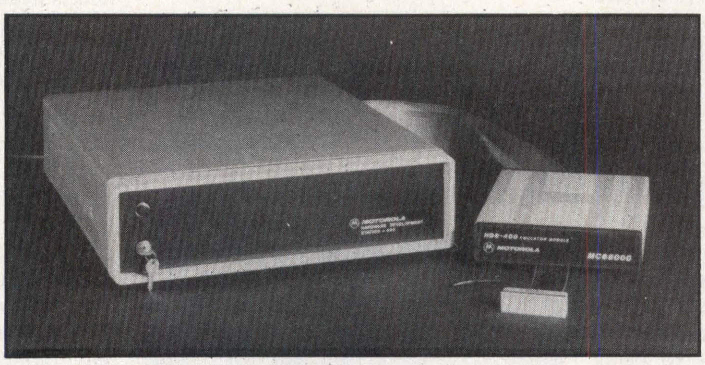
As alternatives to standard-height drives, existing storage capacity can be doubled by fitting 2 drives in the space formerly occupied by a single Minifloppy. LSI electronics help to achieve the 10k MTBF POH and 30-min MTTR. Rotational speed is 300 rpm, with max inside track recording density of 5876 bpi for SA455 and 5922 bpi for SA465. Ambient temp range is 10 to 46.1 °C, within 20% to 80% humidity. Power requirements are 12 Vdc ±5% at 0.6 A typ, 1 A max; and 5 Vdc ±5% at 0.7 A typ, 0.9 A max.

Typical applications include word processors, personal and portable computers, small business computers, and as terminal add-ons. With mechanical dimensions of 1.62″ x 5.75″ x 8.46″ (4.12 x 14.61 x 21.5 cm) and weight of 3.3 lb (1.5 kg), the drives will be available as evaluation units during the fourth quarter of 1982. Production volume is planned for the first half of 1983. In 5k quantity, domestic price will be approximately $165 each for SA455 and $195 each for SA465. **Shugart Assocs**, 475 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 269

Development station balances simplicity and reduced design time

Simplicity for the user—a chief design criteria for the HDS-400 hardware development station—also brings as a major benefit reduced product development time. The HDS-400 provides real-time 10-MHz no wait state emulation of the MC68000 16-bit microprocessor, and communicates with the host EXORmacs™ development system. Up to 8 development stations can simultaneously communicate with EXORmacs. Users edit, assemble, or compile programs with software development capabilities available on the EXORmacs system. Resultant object files can be downloaded into the HDS-400 and/or target system RAM and integrated into both hardware and software.



All components for processor based system designs are in the HDS-400 package, including a 4-slot chassis with 30-A power supply, a workstation control module, and an MC68000 emulator with M68000 family module, symbolic debugging software, and a link to the host EXORmacs system. Two slots are free to use with a bus state analyzer or other optional modules.

The user symbol table, which provides names for actual physical addresses for memory, variables, and data, along with assembled object code, is available from the EXORmacs system. Other symbols defined during the debug process can be added to the table. Once the symbolic table is complete, with references to data, program, and subprogram labels and variables, conversion between symbols and hex code addresses is no longer required. When tracing or displaying MC68000 program code, it is displayed using assembler mnemonics and user symbols for both operands and labels, instead of hex code. Up to 4 breakpoints can be entered for control of program flow. Symbolic assembly allows entry of MC68000 assembler mnemonics, while the symbolic debugger provides automatic conversion to MC68000 machine code.

The 32k-byte 100-ns access time emulation RAM can be mapped in 4k-byte blocks to replace or expand target system RAM. Emulation RAM can be substituted for target system ROM, and can be write protected so that code can be modified and tested in lieu of reprogramming ROMs. User has exclusive use of the full 16M-byte MC68000 address space, including all vectors and interrupts.

Easy to use keyboard, single-stroke selection prompting menus, and macro commands provide total system control. A power-up self-test is included as part of the system's comprehensive diagnostics. Available 60 days ARO, the HDS-400 in 1 through 5 quantities is priced at $6000. MC68000 emulator and family modules and cables are $4000. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.

Circle 270

Judge Hi-G by the company it keeps.

The verdict is in: Our 132 Column Durawriter™ Printer wins hands down, compared to the competiton.

It's super quiet at < 60dbA. And it's fully featured, with an extra-rugged design for longer life and optimum performance.

Accessible, single motherboard design plus our exclusive pre-calibrated printhead makes the Durawriter easiest to service.

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Manufacturers Model No.	List Price	Print Speed CPS	Matrix Character	Size of Buffer	Noise	Dot Graphic D.P.I.
Hi-G 9/132PS Durawriter	$1395.00	150	9 x 9	3,422	58dbA	72 x 72
		75	18 x 9			
Texas Instruments 810	$1895.00	150	9 x 7	256 to 2,048*	72dbA	72 x 60 Optional $600.00
DataSouth DS-180	$1595.00	180	9 x 7	2,000	68dbA	75 x 72
DataRoyal 5000C	$1695.00	165	9 x 9	512 to 2,048*	68dbA	72 x 72 Optional $100.00
Okidata ML-84	$1495.00	200	9 x 9	2,048	72dbA	72 x 72
		50	13 x 17			144 x 144

NOTE: Chart based on manufacturer's information available as of October 1, 1982
*Optional @ extra cost

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CIRCLE 134

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Pascal compiler develops 8086/8088/6800 applications on VAX

Directly addressing accuracy and speed of program development, the BSO/Pascal compiler for Intel's 8086 and 8088 and Motorola's 6800 microprocessors operating on DEC's VAX computers is flexible enough to interface to any operating system and provides manual optimization through its assembly language output. General features include a runtime math function library, recursive and reentrant code programming capability, ROM/RAM segmentation, and ISO standard Pascal accepted as a subset.

Interrupt handling instructions, I/O statements, and file variables for writing I/O routines provide special I/O handling functions for realtime programming. I/O commands can be directed to specific I/O ports on the microprocessor that support I/O instructions. Memory mapped I/O instructions can also be used for microprocessors whose memory can be accessed directly by peripheral interface circuitry. Interrupt procedures can define actions of the user's program when a software or hardware interrupt occurs, with concurrent programs made to communicate via these interrupts.

Large programs can be broken into manageable modules for separate compilation, with support given to modules written in either BSO/Pascal or assembly language. Each module can be individually checked and debugged. Subroutines can also be saved in libraries for later use.

Two stages of automatic compiler optimization during the initial pass of the compiler and one stage of optional manual optimizations include branching for more compact code (when both long and short branches are available), addressing mode simplification for code size reduction, and storing register contents. The compiler eases mapping between the Pascal source and the assembly language output during debug or manual optimization. Pascal source program labels can be passed by the compiler to appear as labels in the assembly language output. The compiler also allows Pascal source symbols to be automatically entered as comments into the compiler's assembly language output.

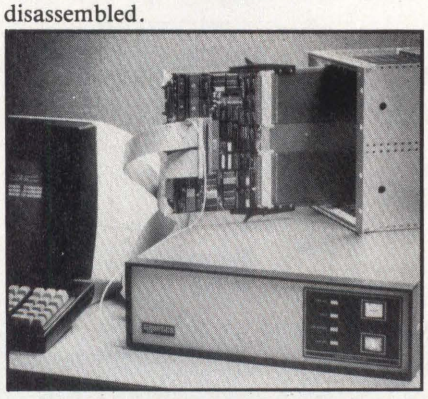
As an alternative to a p-code interpreter, the compiler provides programs that are compiled faster, smaller, and lower in overhead at runtime. No added interpretation steps during execution are required. BSO/Pascal is available immediately for $5000 in the U.S. when bought with its corresponding assembler and debugger. **Boston Systems Office**, 469 Moody St, Waltham, MA 02154.
Circle 271

Microprocessor development tool executes and debugs S68000 software

A low cost but powerful tool for language translators in cross-development environments, the User Work Station (UWS) provides software execution and debug for the S68000 16-bit microprocessor family. Software development can occur on mainframes or minicomputers already existing in the workplace, with cross-development software linking to the existing computing resources. Hardware emulation, software debug and execution, data communications with peripherals, command entry, and memory programming are performed in the single station.

Software is first entered via the host computer text editor, then assembled or compiled. Generated object code is downloaded to the UWS through a serial communications link. A UWS ROM resident debugger provides further tests to set up to 10 concurrent execution breakpoints, examine and modify registers, and make software changes using the resident line oriented assembler/disassembler.

Existing machine code hex values can be translated into readable mnemonics, or new S68000 instructions can be created and inserted into the routine being tested. After keyboard entry, each instruction is verified as it is stored in memory. A user supplied CRT displays both the relative and absolute addresses of the generated code, along with resultant machine code, instruction mnemonic, and instruction operands within the specified range. The disassemble command allows the UWS to accept a range of addresses where code is to be disassembled.



Debugging can be completed entirely within the UWS, or 64k bytes of the total RAM complement can be mapped into the system under development. An emulation cable and Footprint™ probe make all S68000 pins available for connection of oscilloscope and logic analyzer probes, and provide full 8-MHz S68000 hardware emulation.

Required peripheral hardware includes one asynchronous RS-232 CRT terminal with 110- to 19.2k-bps data transmission rates, and one standard RS-232 modem or short distance line drivers for asynchronous communications with the host computer. Also supported are a serial printer interface and a Centronics parallel printer interface. A serial port connection and firmware drivers for the Data I/O Model 19 and Kontron PROM programmers are provided, along with commands for reading, writing, and verifying PROMs.

UWS firmware supports transparent terminal to host operation, downloading of object code from the host to the UWS, and uploading of debugged or partially debugged object code from the UWS to the host. Debugging results can thereby be stored and retrieved later. Either an internal or external clock can be used to increase timing flexibility and to allow debugging to occur with or without a target system. Since concurrent users and multimicroprocessor systems are served, an external clock allows debug of multiprocessor software.

Cross-development software to be introduced will include a macro assembler and a Pascal cross compiler. Approximately the size of a small desktop computer, the User Work Station is priced at $5500 for single units, with quantity discounts available. **Signetics Corp**, 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086.
Circle 272

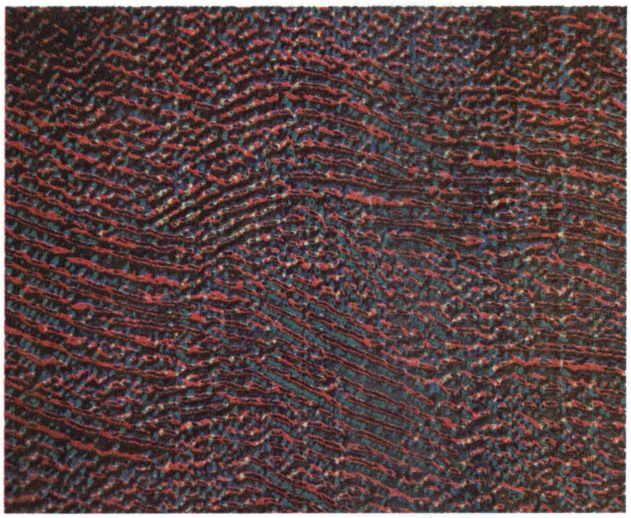
IMAGE PROCESSING: THE FASTEST, LEAST EXPENSIVE WAY TO FIND OIL.

Where to drill? Traditionally, exploring a 25,000 square mile frontier for an answer to that question could take months. And cost over a million dollars for consultant fees and aerial photography.

Today, a DeAnza Image Processing System can narrow the same frontier to a few miles using roughly $100.00 worth of satellite data. *And* help project the final drill site in less than thirty days. Remarkably, the system itself is paid for several times over, exploring just a single frontier.

Get The Complete Picture

Image processing is the *only* way all geological data can be considered *simultaneously:* LANDSAT, SEASAT, radar, magnetic, gravity, topographical, etc. Step-by-step, a DeAnza Image Processing System graphically displays faults, folds and stratigraphic units to pinpoint areas small enough for seismic exploration. Finally, the system enhances seismic data gathered in the field to project final drill sites. And these projections stay completely confidential, because they're done in-house.


Enhanced seismic data of an oil find.

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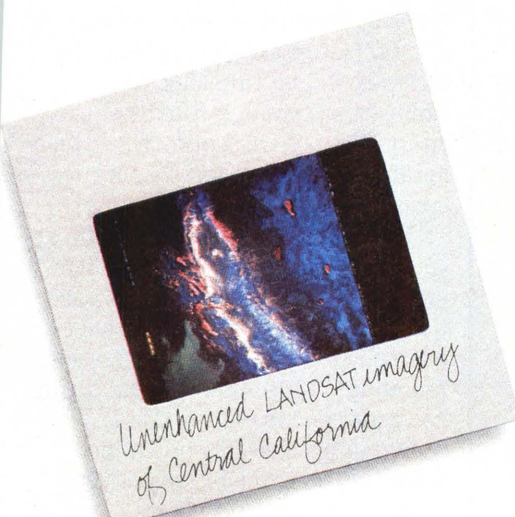
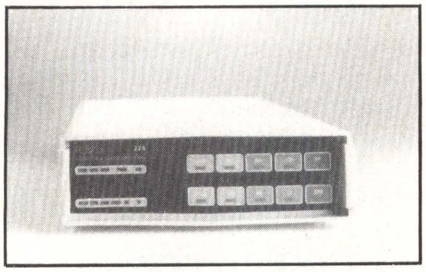


2400-bps full-duplex dial modem



CDS 224 operates at 2400 bps full-duplex in synchronous and asynchronous modes. Automatic 1200-bps, 212-compatible fallback mode enables a centrally located unit to accept data from modems transmitting at 1200 or 2400 bps by adjusting itself to the speed and modulation of the incoming call. Other features are automatic adaptive equalization and local/remote diagnostics. The modem supports half- and full-duplex protocols, including HDLC, SDLC, X.25, and teletex. In tabletop or 7-unit rackmount configuration, quantity-1 price is $1695. **Concord Data Systems,** 303 Bear Hill Rd, Waltham, MA 02154.
Circle 273

Stat mux with programmable options

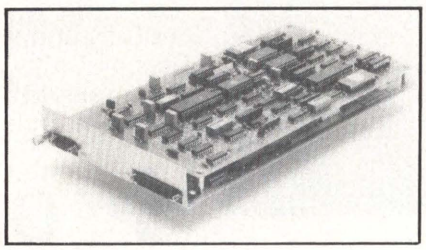
TC-500 concentrates synchronous and asynchronous terminals at 50 to 9600 bps, plus auto-baud. Multiprocessor architecture provides fast throughput and echo response. Automatic channel priority processes full-duplex, character-mode CRT entries before full-stream data output. Std and user programmable flow control conventions are selectable at each end of each channel. Front panel displays selected channel's status in simple English. TC-500 configures with 4 to 32 channels, starting at $1700. Options include split speeds of 1200/75 and 1200/150 bps and Wang flow control. **ComDesign, Inc,** 751 S Kellogg Ave, Goleta, CA 93117.
Circle 274

High speed, fiber optic T1 modem

CSY-306T1 modem directly replaces conventional wire cable in T1 data link applications. It is plug compatible with 1.5440M-bps T1-type data devices, providing an interference-free data channel up to 2 km. Bit error rate is 10^{-9} or better. Fiber optic cable used between full-duplex links is completely immune to emi/rfi and unauthorized data tapping or monitoring. Cable can be buried or routed adjacent to power lines or conduits. Single-unit price for stand-alone or rackmount version is $1800. **Canoga Data Systems,** 21218 Vanowen St, Canoga Park, CA 91303.
Circle 275

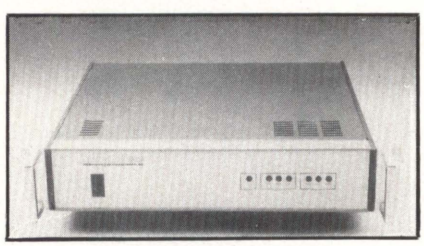
Reduced size 4800-bps modem

VA4840 operates without conditioning level requirements over 2-wire switched networks or 2/4-wire leased lines. It is completely compatible with Bell 208A/B. Up to 8 units fit in the company's 7" (18-cm) rackmount chassis; a single-channel desktop cabinet is available for remote terminal use. VA4840 operates in point to point or multipoint configuration, and features automatic adaptive equalization. A built-in general purpose 8-bit microprocessor controls a 16-bit multiplier and memory to perform all signal processing functions. Unit price is $1600. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.



Circle 276

Data compressor for 100% network capacity



DCU-192 communications data compression/expansion unit extends existing leased line capacity up to 100%. Compatible with most synchronous/asynchronous protocols, the unit connects between the modem and data terminal RS-232-C ports to provide bit stream compression of 2:1 for operation at speeds exceeding the existing communications bit rate. Unit employs 3 high speed 16-bit microprocessors that encode/decode algorithms for performance at rates to 19.2k bps, full duplex. Single-unit is $4950. **Widergren Communications, Inc (WIDCOM),** 1190 S Bascom Ave, San Jose, CA 95128.
Circle 277

The Alps Advantage in keyboards:

Keyboards for modern product design. When you bring your keyboard requirement to Alps, you'll find yourself in good company, alongside many of the most prestigious OEM industry names in the world. From single key switches to complete keyboard units including matrix and encoder circuits, you'll discover the quality, reliability and customer service that have become such important parts of The Alps Advantage, together with everything you need to sharpen the competitive edge of your products:

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CIRCLE 136

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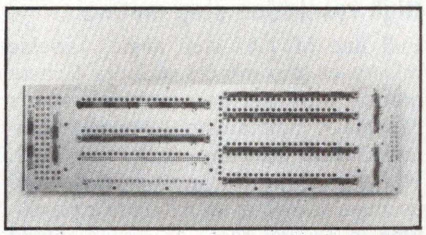
CIRCLE 137

Rugged microcomputer housing

Industrial enclosure for prototype microcomputer development is targeted for control applications. It has power supplies, 12-slot card cage, and capacity to cool 3 CPUs with supporting hardware. Front and rear panels accept industrial or mil grade connectors for communication with controlled equipment or process, and other computers and peripherals via RS-232-C or IEEE 488 interface. Bench- or rackmount unit measures 10.5" x 19" x 24" (26.7 x 48 x 61 cm). **Automotive Environmental Systems, Inc**, 7300 Bolsa Ave, Westminster, CA 92683.

Circle 278

High performance industrial backplane system



ISM series tuning fork aluminum backplanes for severe operating conditions utilize tuning fork contacts, insulators, ground bushings, ground posts, and polarizing keys that conform to MIL-C-28754. Series provides interconnection in 0.1" (0.3-cm) grid configurations with 2- and 3-row connector patterns of virtually any length. Tuning fork contact provides optimal performance when used with rectangular cross-section male blade header connector. Aluminum panel serves as a ground plane and reduces emi and crosstalk. **Stanford Applied Engineering, Inc**, 3520 De La Cruz Blvd, Santa Clara, CA 95050.

Circle 279

Multilayered PCB connectors with reduced gold content

Copper alloy based PAGOS contacts incorporate multiple layers of nickel, palladium, and gold in corrosion resistant PCB connectors. Thinner gold plating makes possible a cost-effective alternative to more heavily plated models. Connectors accommodate Fujitsu flat cables, constructed with 0.100" (0.254-cm) grid terminals and 0.025-in^2 (0.161-cm^2) posts. They come as DIP, card edge, PCB transition, and header assemblies in std pin configurations. **Team Electronics, Inc**, 7 Strathmore Rd, Natick, MA 01760.

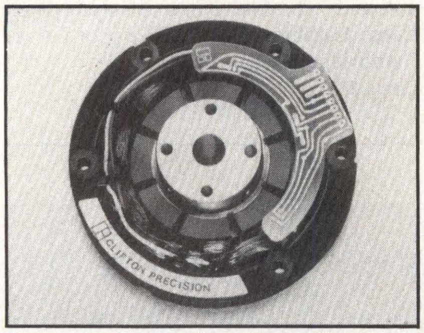
Circle 280

Prototyping/production IC sockets

Series 1100 wire wrappable sockets come in 6-, 8-, 14-, 16-, 18-, 20-, 22-, 24-, 28-, and 40-pin dual-leaf side wipe configurations. Socket body detaches from pins for easy removal or replacement. With 2- and 3-wrap 0.025 in^2 wrapost lengths, units have above-board profile of 0.250". Body is glass reinforced polyester, with CA510 phosphor bronze spring temper contacts. Finish is 10-μin gold over 200-μin nickel, or 200-μin electrotin over 100-μin copper. Contact rating is 1 A, with resistance of 6.1 mΩ at 100 mA and 7.2 mΩ at 1 mA. **Midland-Ross Corp, Cambion Div**, 445 Concord Ave, Cambridge, MA 02138.

Circle 281

Brushless dc motor with commutation logic



DB-3500-HD rotor/stator motor is set with 3 Hall-effect devices for commutation logic. It is compatible with DTL, RTL, TTL, or MOS circuits. Motor direct drives a disk load from standstill to 3600 rpm in 25 ms, and can develop 30 oz-in reserve torque for synchronism. No-load speed is 6300 rpm, with 54-oz-in stall torque. Rated voltage is 24 V. DB-3500-HD is 1.035" (2.629-cm) wide and weighs 14 oz (397 g). **Clifton Precision, Litton Systems, Inc**, Marple at Broadway, Clifton Heights, PA 19018.
Circle 282

Thermocouple/RTD temp sensor input modules

Smart I/O™ thermocouple and RTD temperature sensor input modules are plug compatible with MODICON 584[R] and 184/384 programmable controllers by Gould. Model B251 multiplexes 10 thermocouple or other mV signals into 1 Modicon PC input register. Each solid state differential circuit is fully isolated and filtered. Model B253 multiplexes eight 2- or 3-wire RTD signals into 1 Modicon PC input register. Each solid state input circuit provides excitation power for its variable resistance device. **Lion Precision Corp**, 60 Bridge St, Newton, MA 02195.
Circle 283

Illuminated switch barriers

Snap-in end and center barriers for Series 554 electromechanical and solid state pushbutton switches fit 0.63" and 0.75" (1.6- and 1.9-cm) form factors. End and center types can be mixed when 2 or more switches mount in one hole. From stock, barriers cost $0.16 in quantity-10. **Dialight**, 203 Harrison Pl, Brooklyn, NY 11237.
Circle 284

High slew, wide bandwidth, low noise op amps

OP-27 series operational amplifiers features input offset voltage of 10 μV, low input offset tempco, and input bias current of 10 nA. Noise is between 0.1 and 10 Hz of 0.08 μV pk-pk. Stable input offset voltages as low as 25 μV are guaranteed. Undistorted output up to its 34-kHz power bandwidth and an undistorted output of 8 V pk-pk at 100 kHz are featured. Power supply rejection and common mode rejection in excess of 120 dB are provided. Versions in cerDIP ($3.90) or metal can be processed to MIL-STD-883 level B. **Raytheon Semiconductor**, 350 Ellis St, Mountain View, CA 94040.
Circle 285

Speech synthesis expansion module

GDX-SPEECH TI addition to the GDX™ line of speech synthesizer expansion modules is compatible with Intel's SBC and National Semiconductor's BLC board expansion sockets. Device uses the TI-5220 chip and employs LPC 10 techniques. Module allows speech generation from onboard ROM vocabulary or unlimited vocabulary via CPU provided data. Onboard LPF, 2-W audio amplifier, and volume control are provided. Quantity-1 price is $285. **General Digital Corp**, 700 Burnside Ave, East Hartford, CT 06108.
Circle 286

Low cost infrared emitter/detector

Infrared emitting diode MLED71 manufactured with gallium arsenide and 30-V phototransistor MRD701 are contained in a miniature TO-92 clear plastic package. Devices can operate together as optical slotted coupler/interrupters, light modulators, and shaft position encoders. Diode provides continuous power output of 2.5 mW at a forward current of 50 mA. Devices provide transistor output of approx 10 mA for diode current of 50 mA, with separation of 4 mm. MLED71 is $0.41 to $0.51; MRD701 is $0.34 to $0.42. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.
Circle 287

Re-inking for Printronix printers

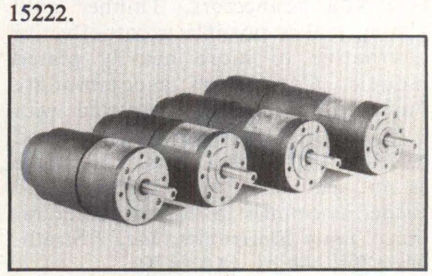
A retrofit system to extend ribbon life on Printronix P series printers features a barrel shaped ink roll that keeps ribbon moist with a constant supply of fresh ink. Roller's barrel shape improves the migration of ink from top and bottom of ribbon and ensures proper contact with the printer's ribbon. Company tests on printers running at top line speed show 100% to 300% increases in ribbon life. Modification system includes 2 rolls ($60/doz) and set of 2 mounting brackets ($23/set). **Porelon Inc**, 1480 Gould Dr, Cookeville, TN 38501.
Circle 288

High resolution step motors

Full line of 1.8° step angle, variable reluctance step motors includes 4-phase models with soft iron multipole rotors capable of maintaining ±5% noncumulative step accuracy under no load. Holding torques range from 20 oz-in to as much as 150 oz-in. All units are available in flange, face, or servomounted configurations. Computerized selection program aids determination of motor characteristics for system designs. **Warner Electric Brake & Clutch Co**, 449 Gardner St, S Beloit, IL 61080.
Circle 289

Permanent-magnet servomotors

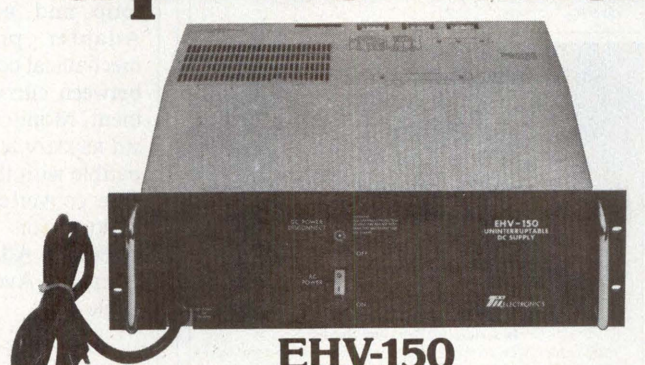
Nonventilated series C400 (Photo) and F560 are completely sealed against oil and dust. Continuous-torque ratings for the C400 are 15 to 60 lb-in, 75 to 300 lb-in for the F560. With optional blower ventilation, F560 units will deliver continuous torque of 500 lb-in. Operating speeds of the two series match 4000 and 3000 rpm, respectively. C400 motors have integral tachometer with externally accessible brushes. F560 options include integral brake and precision geared resolver and encoder feedback assemblies. **Contraves Goerz Corp, Motion Control Div**, 632 Fort Duquesne Blvd, Pittsburgh, PA 15222.



Circle 290

Design in: Uninterruptible DC Disk Drive Power

so your computer won't lose its place in a power failure.



EHV-150 Uninterruptible DC Power System

Loss of stored computer data and damage due to power disturbances are now *avoidable* hazards for Winchester Disk based computers, when our Model EHV-150, 400 W Uninterruptible DC Power System is designed in. By engineering this value added feature into your computer system, you provide automatic shutdown control in the event of AC line loss.

While some power systems merely hold up the memory on batteries for a period of time, the EHV-150 does a lot more. It supports the CPU, memory and Winchester disk on internal batteries during momentary power dips and fluctuations. In the event of extended power outages, the EHV-150 provides your computer with information that allows it to save its memory and system status on disk and initiate an orderly shutdown.

Once power is restored, the EHV-150 tells your system it has come out of power failure so memory and system status can be restored from disk **and your system resumes from where it left off.**

Only 5¼" high the EHV-150 fits into a standard 19" rack. At a time when the market is virtually flooded with competitive computer systems, the EHV-150 should fit into your future designs and create sales appeal to the buyers of your system. To get complete information on this compact uninterruptible DC power system, call 516-789-5020 or write to TII Electronics.

TII® ELECTRONICS, INC.

Sales Office: 1375 Akron Street, Copiague, NY 11726 516-789-5020
Engineering: 226 Terminal Road, East Setauket, NY 11733 516-751-6066

Every computer needs an EHV-150.

To Have a Salesman Call Circle 139 **For Reference Only Circle 140**

TII is a registered trademark.

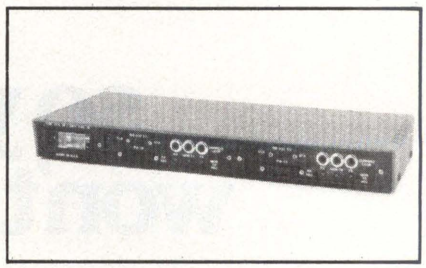
32-user S-100 I/O board

Interfacer 4, serial/parallel interface board, allows 32 max contiguous users at the same 8-port locations. Conforming to S-100/IEEE 696 timing specs, board incorporates an asynchronous serial interface, 2 synchronous/asynchronous high speed channels, Centronics style parallel interface, and a universal parallel port. Proprietary user selection port allows cascading of up to 8 boards at the same port address. System operation at more than 10 MHz and switch-selectable port addressing to any 8-port block are provided. Price is $350. **CompuPro Systems**, Oakland Airport, CA 94614.
Circle 291

Analog and digital I/O for LSI-11s

Measurement and control LSI-11 interface system provides full analog and digital I/O capability, while occupying 1 or 2 slots in the computer backplane. The plug-in DMS511 and DMS512 dual-height cards allow a single card to accept any module to create a common I/O software structure. DMS511 has sockets for 2 I/O modules and provides up to 16 analog inputs, 8 analog outputs, or 32 digital I/Os in various combinations. DMS512 is used as a slave with the DMS511 for system expansion. **DI-AN Micro Systems Ltd**, Mersey House, Battersea Rd, Heaton Mersey, Stockport, Cheshire, England SK4 3EA.
Circle 292

Current loop adapter

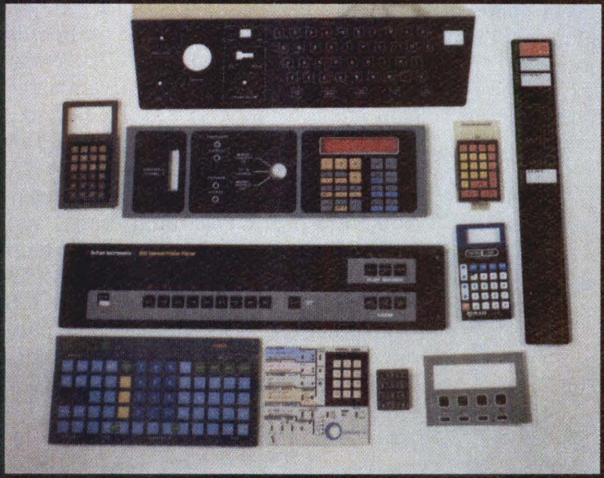


IFA-18 current loop adapter furnishes conversion between 20/60-mA current loop and RS-232/V.24 environments. Adapter provides electrical and mechanical compatibility for differences between current loop and RS-232 equipment. Monitor channel can be used with std RS-232/V.24 data monitors and is compatible with the company's line of interface converters. Unit can be mounted desktop or in a 19" (48-cm) rack assembly. **Atlantic Research Corp**, 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 293

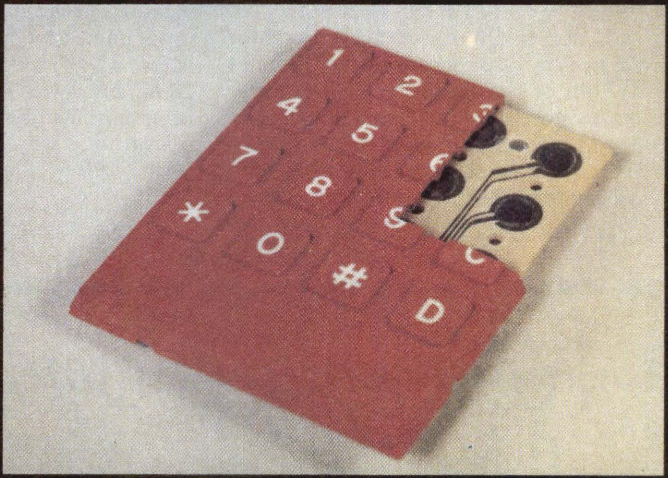
IEEE/488 STD BUS interface boards

TL-488 GPIB talker/listener lets a STD BUS microcomputer system communicate with peripheral GPIB equipment. Talk only or listen only configuration is available for dedicated communication links. TLC-488 GPIB talker/listener/controller handles 14 GPIB devices and can help implement a microprocessor controlled ATE system. Boards operate using interrupts or DMA, and transfer data at 200k bytes/s. Each board uses 1 A of 5-Vdc power. Price of TL-488 is $275; TLC-488, $350. **Quasitronics, Inc**, 211 Vandale Dr, Houston, PA 15342.
Circle 294

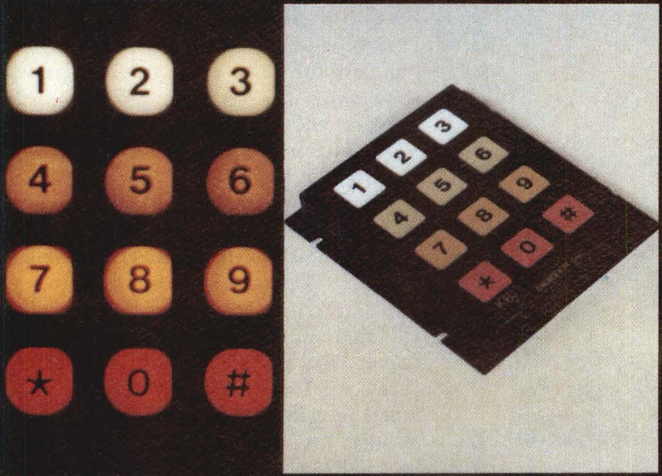
OH! IT'S HARD TO BE HUMBLE
ALL WITH TACTILE FEEDBACK TECHNOLOGY



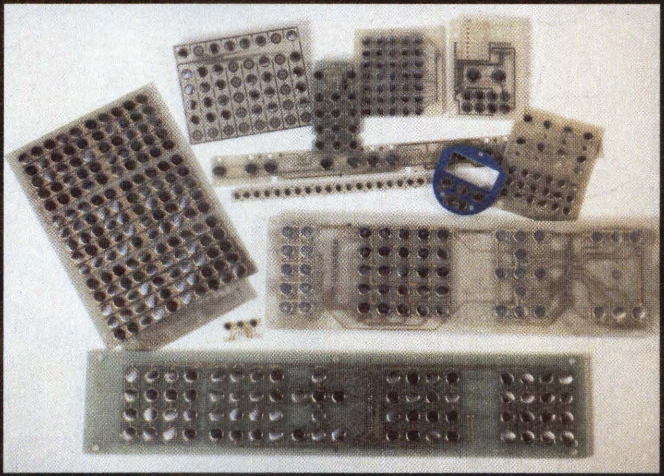
CUSTOM SWITCH PANELS
(Unlimited colors and graphics)



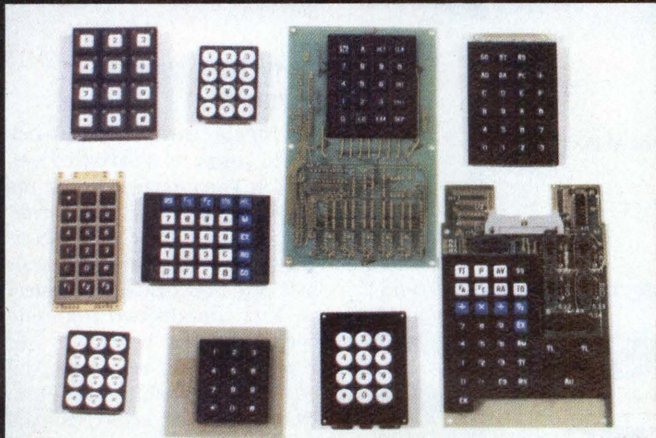
MOD-44 RUBBER BOOT KEYBOARD
(For extreme environmental applications)



MODEL 600 ILLUMINATED KEYBOARD
(Backlit at each key station)



CUSTOM PRINTED CIRCUIT CARD ASSEMBLIES
(You provide your own keycaps or overlays)



CUSTOM KEYBOARDS WITH TWO SHOT MOLDED KEYCAPS

KB DENVER Inc.
A Colorado Corporation

DENVER: (303) 659-0814
TWX: 910 320 2820

P.O. Box 119
451 Oak Street
Frederick, Colorado 80530
Phone: (303) 833-3500

SNAP DOME SWITCHES
(The Heart of all our Products)

CIRCLE 142

Microprocessor interface with nonvolatile program memory

M206 PLL interface for microprocessor controlled TV applications incorporates 512 bits of nonvolatile read/write memory to store tuning information. Device contains a PLL frequency synthesizer, 6 DACs, 4-bit parallel output buffer, clock oscillator, and infrared remote control signal preprocessor. Device interfaces via 3-wire bidirectional serial bus and is programmed by loading 13 internal registers, 12 of which are readable. The 28-pin DIP device requires 25-V supply to program memory and features standby operation. SGS-ATES **Semiconductor Corp**, 7070 E Third Ave, Scottsdale, AZ 85251.
Circle 295

MULTIBUS compatible, battery-operated analog I/O

CBC 8730 series of CMOS analog I/O boards features 32 single-ended/16 differential A-D and 2 D-A channels, programmable gain amplifier with 11 binary selectable gains of 1 to 1024, programmable offset option using 1 of the 12-bit DACs, software selectable true rms to dc conversion, user selectable addressing, and provisions for 4- to 20-mA current loop I/Os. Power dissipation is under 2.5 W max, allowing for battery operation. Op temp range is 0 to 70 °C. Single-quantity price is $1570. **Diversified Technology, Inc**, PO Box 748, Ridgeland, MS 39157.
Circle 296

Video interface, firmware handlers for color graphics copier

Direct video interface and firmware handlers for ACT-I color graphics copier (*Computer Design*, Dec 1981, p 222) operate via existing parallel interface. Video interface comes either installed or as upgrade, without added software, firmware, or special cables. "Remote copy" feature allows host control of the copier. Third-party firmware handlers provide 125-shade onboard lookup table, text/graphics merge from different sources, and daisy chaining. ACT-I copier with parallel (line printer) interface costs $9000, quantity-1; $9975 with video interface. **Advanced Color Technology, Inc**, 21 Alpha Rd, Chelmsford, MA 01824.
Circle 297

Network interface board for S-100 systems

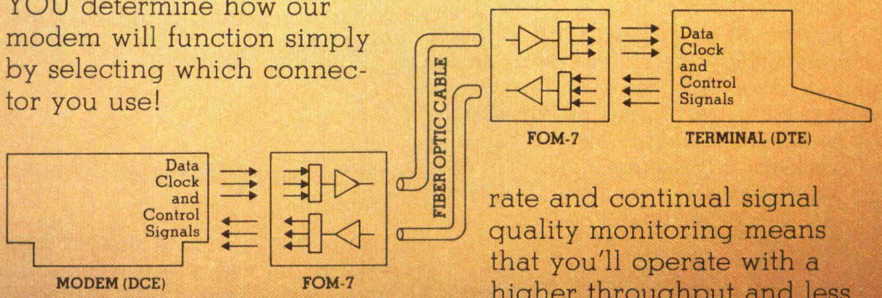
A starter kit for the DESNET™ network interface board connects S-100 based systems into a LAN. The interface board fits in the S-100 backplane, multi-user terminals, or microcomputers. The LAN is independent of processors/protocols and supports std network interconnect cable types. Kits contain two NIB-100/01 S-100 network interface boards in std configuration; two NIT-100/01 coaxial taps; two 10′ (3-m) tap cable assemblies; one 20′ (6-m) length of RG-59U coaxial cable; and one 8″ single-density CP/M diskette. Kit costs $1295. **The Destek Group**, 2111 Landings Dr, Mountain View, CA 94043.
Circle 298

This New Fiber Optic Modem will Extend a DCE Interface to Any Point in Your Local Area Network.

Plus a whole lot more.

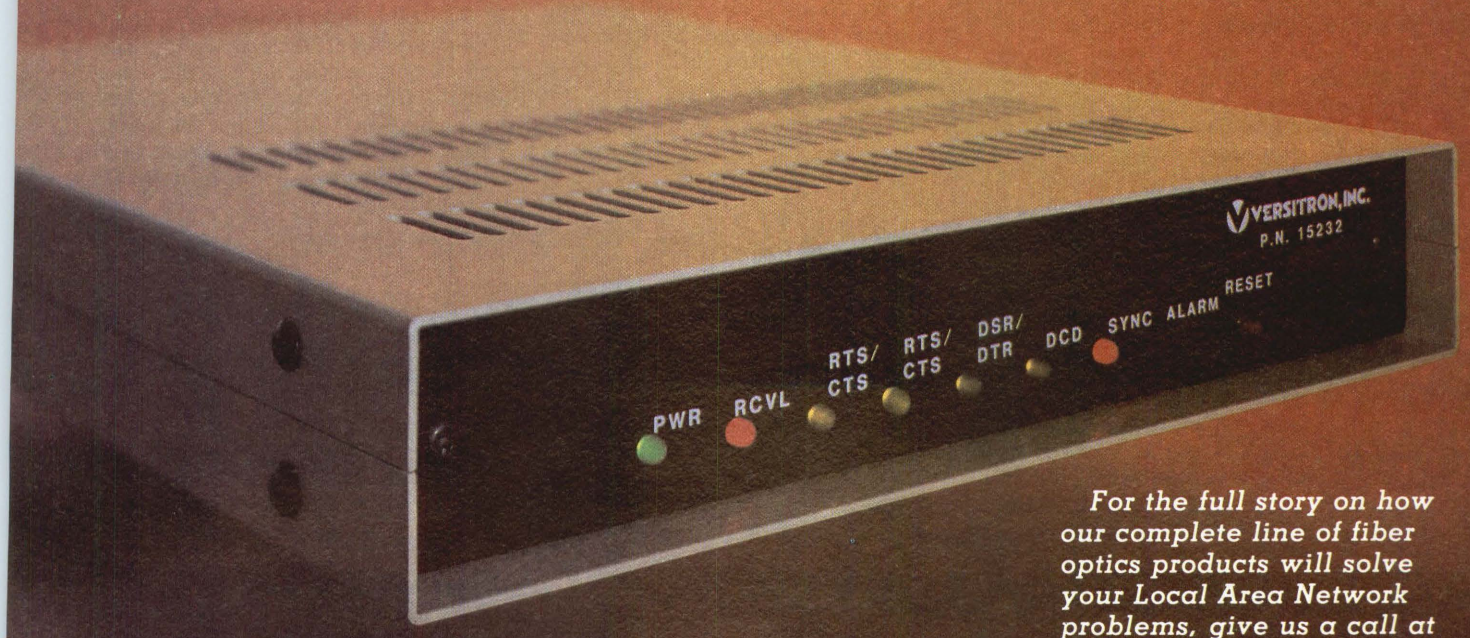
- **Can also be used for standard modem applications**
- **Automatically accepts or supplies DCE/DTE clocks**
- **Fully supports all EIA handshaking signals**
- **Provides secondary data channel**

In short, you can use our new fiber optic modem between *any* two plug compatible units in your local area network. And it won't require any jury-rigging or looping clock and interface signals. That's because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you're going from a long-haul modem to a remote terminal or from a CPU port to a printer. And it's just about as easy to install as a cable — we even provide two separate connectors (DTE and DCE) on each modem. YOU determine how our modem will function simply by selecting which connector you use!



Once our fiber optic modem is installed and operating it'll really begin to shine. You'll benefit not only from the advantages inherent with fiber optics (traffic security plus noise immunity) but also from the exceptional operating performance. Our very low error rate and continual signal quality monitoring means that you'll operate with a higher throughput and less downtime than ever before.

Versitron manufactures a complete line of fiber optic products for Local Area Networks. Our 20 years' experience in fiber optic is reflected in the performance capabilities of our products.



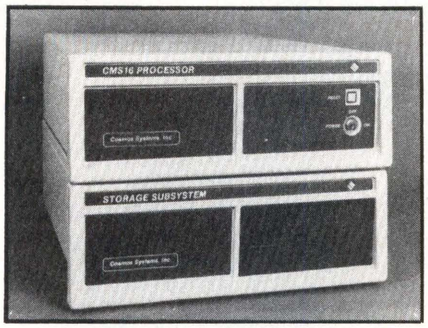
For the full story on how our complete line of fiber optics products will solve your Local Area Network problems, give us a call at (202) 882-8464. Or write:

VERSITRON, INC.

6310 Chillum Place, N.W., Washington, D.C. 20011, TWX: 710-822-1179

CIRCLE 144

Single-packaged 68000, MULTIBUS, and UNIX



CMS16/UNX system combines the 68000 processor, MULTIBUS compatibility, and UNIX Version 7 OS in a single package. System uses a variety of software including C, Pascal, FORTRAN, BASIC, and COBOL. IEEE 796 system features the CMT-CPU 68000 16-bit microprocessor board based on the MC68000. Unit is available in OEM quantities, 30 days ARO. **Cosmos Systems, Inc**, 525 University Ave, Palo Alto, CA 94301.
Circle 299

EXORbus microcomputer with 6801 MCU

MBK6801 single-board microcomputer uses the single-chip 6801 microcomputer unit (MCU) for expanded 6800 instruction set with object code compatibility and improved throughput. Dual serial I/O ports, 8-bit parallel I/O, and onboard memory capacity are provided. Onchip triple-function 16-bit timer schedules events, keeps real time, measures waveform periods, and generates output waveforms. With 2k-byte monitor, 128 bytes of onchip RAM, and sockets for 11k-byte EPROM/ROM/RAM, price is $545. **MRC Systems**, S-302, 7320 Ashcroft, Houston, TX 77081.
Circle 300

Second source for 8086

An off-the-shelf double for Intel's 8086, SAB 8086 comes in 40-pin ceramic package and has operating frequencies to 10 MHz. It is supported by microcomputer system peripherals including SAB 8256A MUART, SAB 8259A interrupt controller, SAB 8282/83 octal latch, SAB 8284A clock generator, SAB 8286/87 octal bus transceiver, SAB 8288 bus controller, and SAB 8289 bus arbiter. Quantity-100 unit prices for the second source in 5-, 8-, and 10-MHz versions are $29.75, $36.75, and $59, respectively. **Siemens Corp, Components Group**, 186 Wood Ave S, Iselin, NJ 08830.
Circle 301

Dedicated CPU adds users without degrading system

With its own 2k-byte EPROM, 64k-byte bank switched RAM, Z80A, and 4 serial/2 parallel I/O ports, SUPER-SLAVE shares data with its host only when accessing common peripherals. Each dedicated processor fits any S-100 motherboard. In system configuration, boards form a master-slave network protected by the advanced failure detection and recovery of Turbo-Dos operating system. Modular operating system architecture allows individual users to perform on single-task, multitask, or network level without affecting other users. Unit price is $650. **Advanced Micro Digital Corp**, 12700 B Knott Ave, Garden Grove, CA 92641.
Circle 302

Z80 based expandable single-board computer

SD/E COMBO, a double-Eurocard format, 4-MHz Z80 based single-board computer, can be expanded with added SD/E bus compatible boards. Featured are 64k dynamic RAM and two 28-pin Bytewyde™ sockets for either 2k x 8 or 8k x 8 ROMS or EPROMS. Memory map PROM provides 8 memory configurations for combined RAM and ROM/EPROM. Two RS-232-C serial I/Os with programmable rates from 50 to 19.2k baud and four 8-bit parallel I/O ports are included. DMA and floppy disk controllers are provided. Board is $1995. **Mostek Corp, Subsidiary of United Technologies Corp**, 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 303

Microcomputer with onboard solid state mass storage

BBC-128 single-board MULTIBUS microcomputer is Z80A based and includes a 1M-bit magnetic bubble device with 128k-byte onboard mass storage. Need for floppy disks or magnetic tape is eliminated. CP/M mass storage OS can be loaded into the bubble device and operated with added terminal and power supply. Using no part of the 64k user memory space, onboard shadow ROM contains power-up bootstrap, error detection/correction algorithms, and self-test routines. The microcomputer is $1443. **Bubbl-Tec**, 6800 Sierra Ct, Dublin, CA 94568.
Circle 304

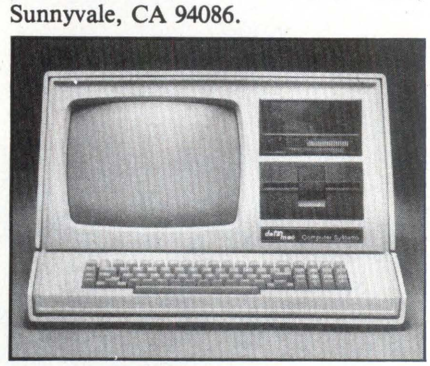
COMPUTERS

MULTIBUS compatible control system

DCS/86L 9-slot MULTIBUS compatible development control system in an all-metal rackmountable enclosure utilizes CDC Lark cartridge disk to eliminate need for Winchester backup via streaming tape. A 1M-byte floppy disk and 5 slots for further MULTIBUS modules are included. DCS/8616 single-board computer has 5-MHz 8086 16-bit processor with full multimaster capability. CPU includes 24-bit parallel I/O and 3 serial ports. An 8088 based intelligent disk controller provides full multiprocessor operation, has multisector buffering, and implements a disk cache strategy. OS includes CP/M-86, MS-DOS, MPM-86, and Concurrent CP/M-86. **Distributed Computer Systems**, 223 Crescent St, Waltham, MA 02154.
Circle 305

8-bit enhanced desktop computer with optional 5¼" Winchester

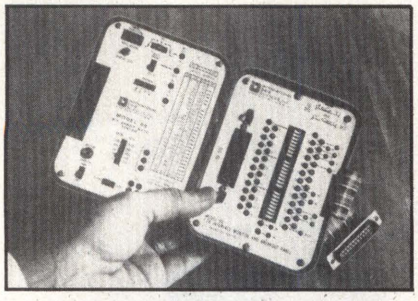
Series 800 enhanced version of the series 1255 8-bit desktop computer system features streamlined chassis, detachable keyboard, and optional 5¼" Winchester disk. The CP/M based system includes Z80 processor, 64k-byte RAM, two RS-232 I/O ports, and 1 parallel port. Drives are configured as 5¼" or 8" floppies of single or double density, single or double sided, 48 or 96 tpi; and 5¼" Winchesters of 6M, 12M, and 18M bytes. Corvus networking, multi-user capability, IBM 3270 terminal emulation, and multidisk formats are featured. **Datamac Computer Systems**, 680 Almanor Ave, Sunnyvale, CA 94086.



Circle 306

Talk to the editors
Have you written to us lately? We're waiting to hear from you.

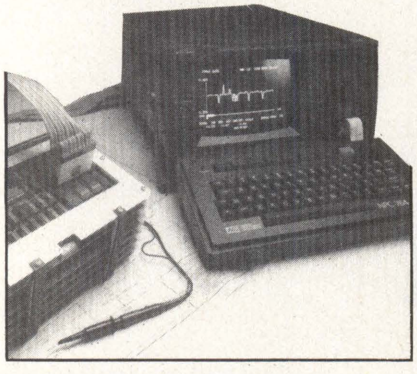
Modem tester



Model 65/60 "Red Box" tests asynchronous modems at 1800 bps. The battery operated tester has separate transmitter and receiver sections to perform full-duplex tests in end to end or loopback configuration. The transmitter continuously generates 1 of 4 switch-selectable data patterns, including 63-, 511-, and 2047-bit repeating pseudorandom sequences and an alternating mark-space pattern. The receiver compares an error-free replica of a transmitted data pattern with the received data pattern. Price is $195. **International Data Sciences, Inc**, 7 Wellington Rd, Lincoln, RI 02865.
Circle 307

Firmware enhanced logic analysis system

Enhancements for NPC-764 logic analysis system include expanded I/O firmware for unified I/O command set that gives user complete control of both GPIB and RS-232 interfaces. All features are accessed through self-contained menus and soft keys. Firmware allows master/slave operation among multiple analyzers, using the same control menus. Instructions can be transmitted directly from keyboard to remote CRT. System combines 48-channel state and 16-channel timing analyzers. Optional plug-ins include waveform recorder and 5-function counter/timer. **Nicolet Paratronics Corp**, 201 Fourier Ave, Fremont, CA 94539.

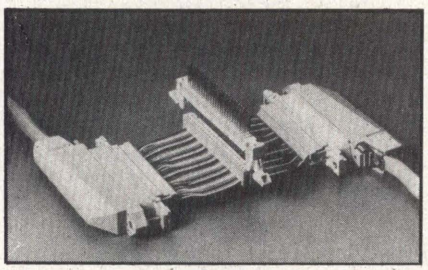


Circle 308

VLSI test system

S-3295 VLSI automated tester of pin capacity up to 256 channels handles ECL, TTL, and MOS logic families, as well as mixed hybrids. Pin electronics are 1 V/ns, have submillivolt level control, subnanosecond timing control, and programmable driver slew rate and dynamic load circuitry. The 128k, pin resident, 20-MHz pattern memory minimizes pattern overlays and provides for realtime error storage. Median price is $975,000; device will be available during the second quarter of 1983. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077.
Circle 309

Assembly circuit tester

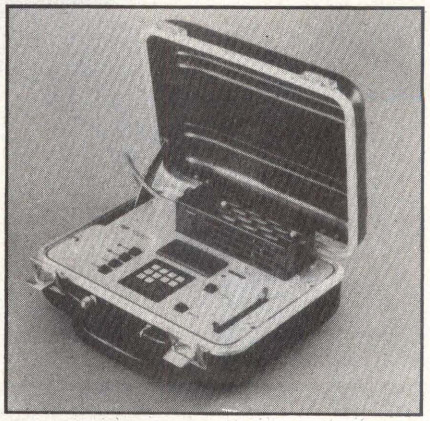


SuperEx™ cable extender provides test access points for 50-position miniature ribbon connectors (RJ21X) with no need to disconnect the entire 25-pair connected cable to test a specific pair. Cable extender is point to point wired; terminated midway between the ribbon connectors and socket is an IDC flat cable socket connector that can be fitted with a wirewrap header utilizing 0.025" (0.064-cm) square pins for test points or for attaching temporary/permanent external signaling devices. **TRW Electronic Components Group**, 1501 Morse Ave, Elk Grove Village, IL 60007.
Circle 310

Rugged data line analyzer

Model K 1190's generator and receiver come in one casing with microcomputer, keyboard, and VDU. Interactive screen dialogue prompts operators, and long-term program storage recalls individual settings and test results. Built-in interface handles remote control master/slave operation. Telephone hookup connects the analyzer and voice communications over the line under test. Optional IEEE 488 bus connects analyzer for speaker/listener control in an automatic system. With recorder and video outputs, analyzer costs about $14,500. **Siemens Corp, Transmission Equipment Div**, 186 Wood Ave S, Iselin, NJ 08830.
Circle 311

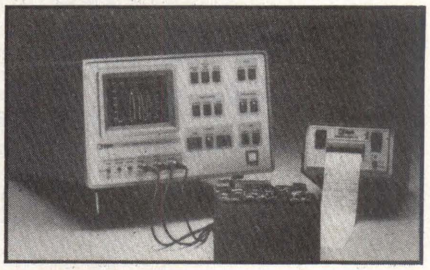
Automatic tester for fixed drives



A portable test system automatically exercises 8" Winchester ANSI fixed disk drives. Test/evaluation functions prompt DX8000 operators through up to 16 programs. The microprocessor interacts with the operator during test programs and controls disk drive exercising functions. It also remembers parameters and setup conditions so later tests can run without reentry of values. Priced at $2025 quantity-1, the DX8000 measures 10" x 12" x 5" (25 x 30 x 13 cm) and weighs 6 lb (3 kg). **Applied Memory Technology**, 2822 Walnut Ave, Tustin, CA 92680.
Circle 312

TIA for tape/disk drive testing

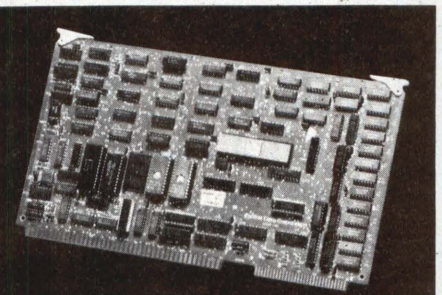
Time interval analyzer (TIA) 100A provides bit shift data and isolates problems to media, heads, or defects in read electronics. It can be remotely controlled via the integral IEEE 488/GPIB bus. Tool accepts encoded logic level reproduced data and uses pulse interval measurement technique and CRT display format for near realtime evaluation of jitter, bit shift, margin, asymmetry, estimated error rate, and other parameters. The statistical time interval counter diagnostic tool has printer option for dedicated hardcopy documentation. **Kode Inc**, 2752 Walnut Ave, Tustin, CA 92680.



Circle 313

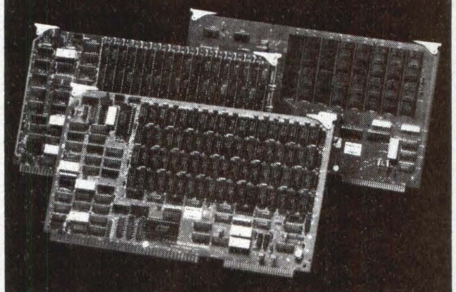
Look to Central Data

for a complete line of Multibus* boards and accessories



CPU BOARDS

The **Z8000* Processor Board** features a unique memory management circuit that maps physical memory into 2K pages for a total system-wide memory of 16 megabytes. Completely Multibus compatible, the Z8000 also has full multimaster capabilities to allow the use of several processor boards and DMA devices on the bus at one time. Two automatically-selected 2716 EPROMs are optionally available. $710.

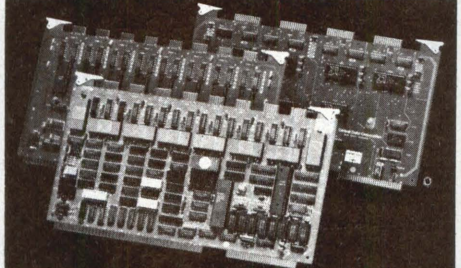


Memory Boards

A **Dynamic Memory Board** allows the user to add from 32K to 128K of dynamic RAM to a system. Automatic refresh and parity checking are standard. 32K - $640, 64K - $705, 96K - $775, 128K - $845.

A **Static Memory Board** adds either 16K or 32K of static memory to any Multibus system. The board has an access of 250 ns and parity checking is a standard feature. 16K - $715, 32K - $1,060.

A **PROM Board** works with all standard EPROMs, both those currently available and those in development. $225.



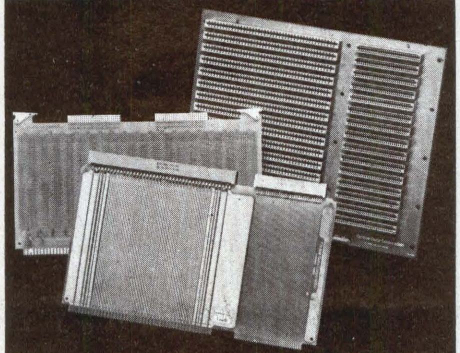
I/O Boards

I/O Boards are available in three models to meet any user's needs. All have standard RS-232 connections.

An **Intelligent Octal Serial Interface** provides 8 ports and 16K of dual-port RAM for data transfers with no bus overhead. $650.

A **Quad Serial Interface** hooks up to four EIA Interfaces to a system. $280.

An **Octal Serial Interface** allows up to eight interfaces, each controlled by a USART with an on-chip baud rate generator. $375.

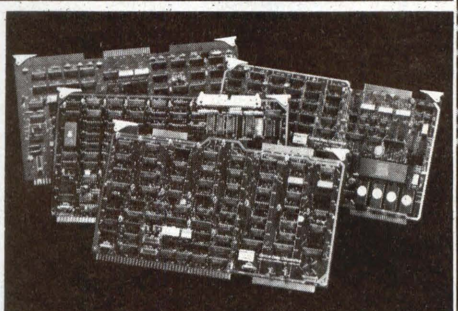


Specialized Boards

An **Extender Board** is available to raise a board up to a height of 6.9 inches for easy testing of Multibus cards. $95.

A **Prototyping Board** will accommodate up to 95 16-pin sockets, allowing the user to wire wrap a prototype circuit. $95.

A **Multibus Mother Board** can hold up to 15 cards with both P1 and P2 provided for each card position. $670.



Disk Controllers

New this year is a **Winchester Controller** that works with an **IMI intelligent disk drive** and an **Archive streaming tape unit**, both controlled by the same board. $310.

A **Winchester Disk Controller** fully conforms to ANSI standards and can control up to eight drives. $530.

A **Cartridge Disk Controller** provides DMA transfers to or from cartridge disk drives with capacities of 10 or 20 megabytes. $750.

A **Double-Density Floppy Disk Controller** adds from one to four double density standard floppy disk drives, either single or double-sided. $375.

All quoted prices are single unit, effective November 1, 1982 and are subject to change. Quantity prices are available upon request.

For more details on Central Data's full line of boards, subsystems and systems, call or write:

Central Data Corporation

1602 Newton Drive
Champaign, IL 61820
(217) 359-8010 TWX 910-245-0787

Your complete multibus* source

*Multibus is a trademark of Intel Corporation
*Z8000 is a trademark of Zilog Corporation

CIRCLE 149

PROM development system

Simulating PROM from RAM, YES-5 allows code test before burn-in. The board-level microcomputer helps developers build, troubleshoot, and evaluate the Z80. It also simulates and programs 2758, 2516, 2716, 2532, and 2732 EPROMs. System monitor accommodates direct code loading in Intel's hex or CP/M dump format through RS-232 port to onboard 8k-byte RAM. Including board, chassis, power supply, software, and jumper, tested unit costs $495. Interconnecting cable plugs into 24-pin DIP socket. **Yang Electronic Systems, Inc**, 307 Compton Ave, Laurel, MD 20707. **Circle 314**

STD BUS control/development

SYS-10 is a single-board system that develops, tests, stores, and exercises program control of peripherals on the STD BUS. It can replace the present controller in an existing system, or be used as a smart peripheral. Features include a complete operating system in firmware; CAMBASIC language with interpreter/debugger/editor; direct connection to CRT and serial printer; and EPROM programmer that converts RAM based programs to EPROM copies for control application. Price is $485. **Octagon Systems Corp**, 5150 W 80th Ave, Westminster, CO 80030.
Circle 315

Single-channel second source for TI voice synthesizer

TIM™ (Texas Instruments Module) connects to any MULTIBUS based SBC that supports an iSBX bus. VoiceWare™ development system drives TI's VSP 5220 voice synthesis chip. Vocabulary stored either in EPROMs on the SBC or on disk will drive the unit; vocabulary size is limited only by available storage. Module has full range of audio response applications and direct audio output for amp interface with phone lines. Crystal controlled sample rate maintains voice quality. TIM costs $350; VoiceWare/TIM system is $29,500. **Centigram Corp**, 155A Moffett Pk Dr, Sunnyvale, CA 94086.
Circle 316

More features for 64000 logic development system

Software driven emulation capabilities have been added to 16-bit emulators for 8086, 8088, Z8001, Z8002, and 68000 microprocessors. Accessed through directed-syntax soft keys, features include 16 breakpoints to set a trace on, or break on, an instruction's execution; display or modification of I/O ports and floating point memory; simulated I/O; initiation of command files from the emulation environment; wait command; run-until syntax; and measurement system compatibility for interactive operation of 16-bit emulators within an HP 64000 station. Contact local **Hewlett-Packard** sales offices.
Circle 317

 CIRCLE 146

Positive protection for personal computers.

Airpax magnetic circuit breakers.

Whether the surroundings are hot or cold, Airpax magnetic circuit breakers' minimum trip current is not affected by temperature extremes, as is the case with fuses and thermal devices. These "trip-free" breakers won't stay closed on an overload even if the handle is held in the "on" position. Their built-in inertia delay avoids nuisance trip-outs due to transient surges.

Designed to conform with VDE and IEC standards 380 and 435, Airpax SNAPAK® breakers make your product ready for export markets. A wide choice of handle actuations, colors, illumination, terminals and hardware gives you the styling and selection you want. They are tested, listed and qualified under various military, UL, CSA and SEV specifications. Proven performance has made them the choice of leading manufacturers of computers, peripherals, broadcast equipment and machine controllers.

Because they combine the functions of power switching and overload protection and have zero replacement requirements, Airpax breakers are an affordable option to fuse-switch combinations.

For complete specifications, write or call Airpax Corporation, a North American Philips Company, Cambridge Division, Woods Road, P.O. Box 520, Cambridge, MD 21613. (301) 228-4600.

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CAMBRIDGE DIVISION

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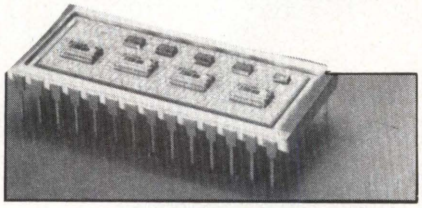
CIRCLE 147

Quad-DAC in single 28-pin DIP



AD390 28-pin DIP contains 4 pretrimmed 12-bit DACs and provides buffered voltage outputs, guaranteed monotonic performance over temp, precision internal reference, and double-buffered data latches. Processing to MIL-STD-883B is available on S/T grades. Control architecture eases microprocessor interfacing and provides independent DAC addressability. Exercising 4 chip selects and 2 address lines activates the double-buffered data latches and loads specified DACs through common input port. Operating with ±15-V supplies, DAC draws max quiescent current of 20 and −90 mA for total max power dissipation of 1.65 W. Prices in 100-lots are $115/$136 for J/K grades and $296/$347 for S/T grades. **Analog Devices, Inc,** 804 Woburn St, Wilmington, MA 01887. **Circle 318**

Simultaneous sample/hold data acquisition module

DT5704 12-bit data acquisition module features simultaneous sample and hold functions for up to 12 single-ended 0- to 10-V or ±10-V analog input channels. Module includes an analog input multiplexer, 100-kHz ADC, and internal timing/control logic. With capacity for up to 4 input channels, DT04EX expander module ($495) provides 12 sample/hold channels. Digital data outputs are 3-state buffered. In 1 to 9 quantity, module is $795. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752.

Circle 319

2-wire remote I/O and communications system

Metra 500 microprocessor based distributed processing system has preprogrammed remote stations placed close to signal sources and/or control points. Each remote station can accept up to 3 I/O boards. I/O board can handle 16 analog input, 32 digital input channels, or 32 TTL output channels. Analog inputs include mV, V, mA, T/C, RTD, and strain gauges; digital inputs include contact closure, TTL, optically isolated high level Vac or Vdc, pulse rate, and event counters. Up to 255 slave stations can be daisy chained by a single twisted pair cable that can send control signals to any remote station. **Metra Instruments, Inc,** 2056 Bering Dr, San Jose, CA 95131.

Circle 320

Rugged 12-bit ADCs

ADC87/MIL series high performance ADCs feature ±0.5 LSB linearity, ±0.1% FS accuracy, ±15-ppm drift, 8-μs conversion, and optional MIL-STD-883 screening. Converters have internal reference, input buffer amplifiers, and internal clock. Five analog input ranges, as well as parallel and serial digital output formats, are available. All digital I/O is TTL compatible. Premium grade units function from −55 to 125 °C; U grade op temp is −25 to 85 °C and −55 to 125 °C. All models are hermetically sealed in 32-pin DIPs. Unit prices range from $230 to $415. **Burr-Brown,** PO Box 11400, Tucson, AZ 85734.

Circle 321

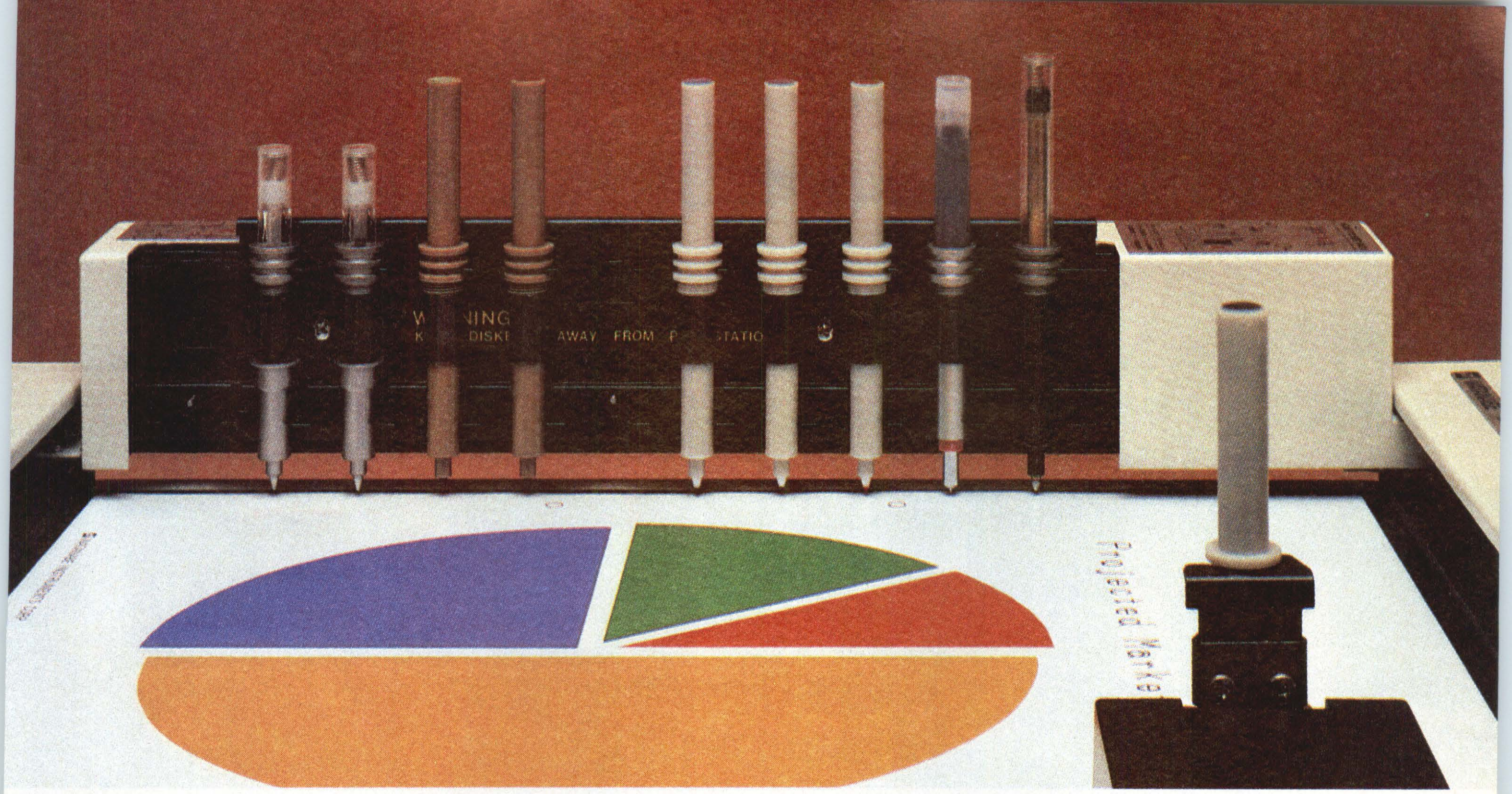
Alternative to potentiometric ADCs

SOFTPOT optical incremental encoder converts shaft rotation directly to digital output. Torque is loaded to feel like a potentiometer, but with no stops. Full use of software driven systems, including software presetable parameters, definable limits, and programmable interaction is possible. Noise-free 2-channel output provides both direction and rate of rotation. There are no wiping contacts to wear out or debounce. Units require 22 mA from a single 5-V supply, and couple directly to std TTL devices. **U.S. Digital,** 5405 Garden Grove Blvd, Westminster, CA 92683.

Circle 322

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? Turn to the Editorial Score Box on the Reader Inquiry Card.



Watanabe plots color. Fast, accurate and easy as pie.

Watanabe brings you a multi-pen digital plotter you can even use at your desk. Its low cost makes it affordable. And its sophistication makes it the answer to your need for economical high-speed, hard-copy graphics. Whether for engineering drawings, scientific plotting, architectural design, or business graphics.

Easy to program and use. You don't have to be an engineer to use a Watanabe plotter. Yet it can produce complex engineering drawings. Intelligence is built into the plotter through our unique microprocessor controllers.

So it can perform complex tasks using the single-letter commands you give it. Programs are also simple to write, making the plotter very convenient to use. Or you can use one of the many software packages available for Watanabe plotters.

Choose the model that's right for you. Why pay for features you don't need? Watanabe plotters are available in a variety of models. One will be best for your budget and graphics needs. Choose from our low cost, single-pen plotter, through a range of multi-pen configurations, to our high-speed, intelligent plotters. Or select a machine that blends analog and digital technology.

Use water or oil-based pens, or ink pens. Choose from sheet-feed or roll-feed models, or produce drawings on acetate for overhead projection. In addition to programmable graphics and function commands, the complete ASCII character set is standard. Each plotter can interface to any computer with an RS-232-C serial interface, IEEE-488 interface, or parallel port.

Designed for long use. Just one example of Watanabe's built-in reliability is the ingeniously simple, automatic mechanical pen pickup used on the multi-pen models.

When your plotter does need maintenance or repair, one of our many locations worldwide will provide prompt service. We design, manufacture, and service our plotters ourselves. So we know we can stand behind them with confidence.

Let us put a plotter at your fingertips. Call Don Pierson toll-free at (800) 854-8385 to arrange a demonstration. In California call (714) 546-5344. Or write: Watanabe Instruments Corporation, 3186 Airway Avenue, Costa Mesa, California 92626.

W WATANABE

CIRCLE 148

Communications terminal

Standalone model 4015 communications terminal operates under Bell 8A1 communications protocol and features a common mode that allows the host CPU/master terminal to downline load date and time of day, and to change supervisory passwords. Six function keys allow immediate call-up of std formats stored in memory. Model 4220/UTS-20 communications system is functionally compatible with Univac's U100, U200, and UTS-20 terminal systems, and has no limit to the number of field control chars that can be used in a single line. Model 4015 is $4155; model 4220 is $3370. **Racal-Milgo**, 6250 NW 27th Way, Fort Lauderdale, FL 33309.
Circle 323

Bar code industrial terminal

RT137 addition to the RT100 family of industrial terminals can read code 39, 2 of 5, interleaved 2 of 5, and code 11 bar code types using a handheld visible light scanning wand. Designed for harsh environments, terminal has protective exterior hardware and flat membrane keyboards. Terminal is priced from $4500; deliveries are 30 to 60 days ARO. **Digital Equipment Corp**, Maynard, MA 01754.
Circle 324

Low cost 16-col printer

SP-150 16-col dot matrix impact printer has 4.7" x 2.7" x 4.8" (11.9- x 6.9- x 12.2-cm) housing and accepts either parallel BCD or 7-bit parallel ASCII inputs. It is available for either ac or dc applications. Alphanumeric char set is PROM configured. Standard paper tape and dot matrix chars are accommodated. Price is $450. **Kessler-Ellis Products Co**, 120 First Ave, Atlantic Heights, NJ 07716.
Circle 325

Intelligent programmable terminal

Intended to replace the GT-110 and GT-101, AVANT 250 and 251 combine ergonomic features like tilt-swivel monitor mount and detachable keyboard with versatile programmability. Data storage of 10k bytes of RAM can be downline loaded from host. Initialization EPROM will automatically load RAM and function keys on power-up. User/host programmable function keys and video attributes, as well as a range of peripheral interfaces and baud rates, are included. Green or white phosphor screen displays twenty-four 80-char lines, with a 25th status line. Unit price of either model is $1095. **General Terminal Corp**, 14831 Franklin Ave, Tustin, CA 92680.
Circle 326

Plotter interfaces to any computer

Model 3200 D-size flatbed pen plotter has a plotting area of 25" x 37" (64 x 94 cm) and built-in plot subroutines as part of the controller. The plotters are compatible with any programming language and any OS at any revision level. Units automatically generate second-degree curves without calculating each increment for circles or ellipses. Also featured are 2496 bytes of user programmable RAM and downloaded repetitive graphics symbols. RS-232-C asynchronous serial ASCII interface and optional GPIB interface are furnished. Price is $11,500; OEM discounts are available. **Data Design Logic Systems, Inc**, 4800 Patrick Henry Dr, Santa Clara, CA 95054.
Circle 327

Raster scan display with 35% price cut

RM-9460 display system provides all features of the RM-9400 family but is priced starting at 35% less. The 16-bit system uses the MC68000 CPU and 64k RAM. Multiple memory processors provide independent graphics operations on multiple workstations. Resolution is 1280 x 1024 pixels and up to 32 refresh memory planes. Writing speeds exceed 16k vectors/s, based on average vector length of 50 pixels. System displays up to 1.3M colors simultaneously from a palette of 16M. An MC68000 CPU upgrade card for the RM-9400 is $7250. RM-9460 is priced in the mid $20,000 range with OEM discounts available. **Ramtek Corp**, 2211 Lawson Ln, Santa Clara, CA 95050.
Circle 328

Letter quality printer for IBM Series/1

Certainty 410 letter quality daisy wheel printer for IBM Series/1 minicomputers prints at 55 cps, and provides selectable compressed formats, changeable print wheels, and snap-on ribbon cartridge. Unit operates with single sheets or continuous form feed, and can use 6-part forms up to 15" (38 cm) wide. Options include bidirectional forms tractor feed and paper handling basket. Printer is $2775 for 5 to 9 units; volume discounts are available. **Control Data Corp**, PO Box O, Minneapolis, MN 55440.
Circle 329

1k x 1k raster display system

GMR 27-64 provides a 1024 x 1024 display with 30-Hz interlaced refresh, generating RS-170 compatible video signals that drive standard color or black and white monitors. Up to 16 colors can be displayed. Display generator and power supply, 4-bit refresh memory, 200-ns/pixel vector generator, full alphanumerics, and rectangle/image generators compose the system. Pan, zoom, and combined 10 x 12 lookup table/video card are standard. A range of software and hardware options is available. Quantity-1 price is $15,750. **Grinnell Systems Corp**, 2159 Bering Dr, San Jose, CA 95131.
Circle 330

4-D digitizer

Graphics digitizer produces X, Y, and Z digitized data, and also 4-D stylus tilt. Direct controlled rotation of 2- or 3-D images or pan while zoomed is possible by using stylus tilt information transmitted concurrently with the X, Y, and Z data. Electronic sensing of magnitude and direction of stylus tilt with respect to the tablet's surface transforms the stylus into an unrestricted joystick/digitizer. Nonmechanical tilt sensing is independent of acceleration, vibration, gravity, or wear. The 4-D option is $200 on any size Digi Pad. **GTCO Corp**, 1055 First St, Rockville, MD 20850.
Circle 331

Experts needed
How about reviewing technical articles for Computer Design? Circle **501** *on the Reader Inquiry Card.*

Low cost, 16 x 16 NMOS parallel array multipliers

With a 200-ns typ multiply time, WTL2516/2517 are pin for pin functional equivalents to bipolar multipliers like the TRW MPY16HJ and AMD 29516/17, which have multiply times of 60 to 100 ns. The multipliers use a modified Booth's algorithm and advanced NMOS VLSI design. I/O latches operate in clocked or transparent mode. Input data are accepted in 16-bit 2's complement, unsigned magnitude, or mixed format. Devices require 5-V supply and have TTL compatible I/O levels. Both come in 64-pin plastic DIPs and cost $65 in quantity-100. **Weitek Corp**, 3255 Scott Blvd, Santa Clara, CA 95050. **Circle 332**

Microprocessor compatible DACs with double-buffered inputs

DAC-608, DAC-610, and DAC-612 interface directly with the standard control bus of 8080 derivatives via double-buffered inputs. The 8-, 10-, and 12-bit DACs do not need interfacing logic because they look like a memory location or I/O port to the microprocessor. Models operate as normal DACs for non-microprocessor based applications. Cased in 20-pin plastic DIPs, DAC-608 and DAC-610 operate at 0 to 70 °C and cost $4 and $14, respectively. Priced at $30, DAC-612 comes in 24-pin cerDIP with op temp of −25 to 85 °C. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.
Circle 333

Universal DAC for 8-bit MPUs

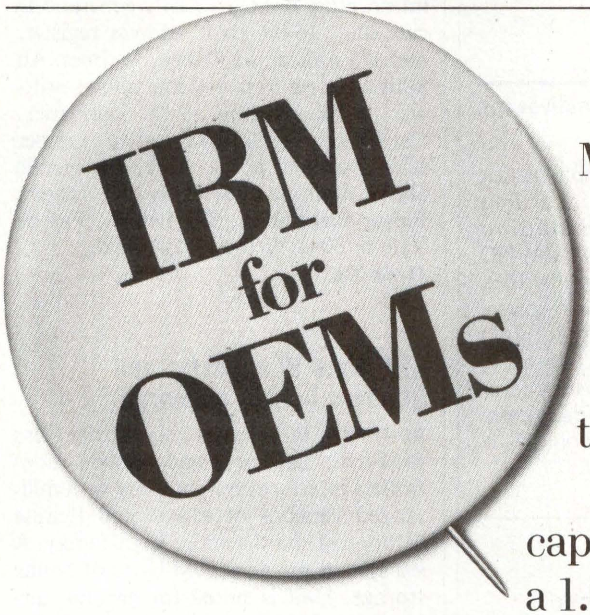
MC6890 DAC uses monolithic bipolar technology, thin film resistors, double-buffered input latches, control logic, precision 2.5-V band gap reference, and span/bipolar offset resistors. The 8-bit bus compatible DAC guarantees full-scale accuracy without external trim potentiometers. Linearity is 8-bit accurate over temp with settling time no greater than 300 ns to 1/2 LSB. With 1 external op amp, the precision span and bipolar offset resistors provide calibrated unipolar/bipolar full-scale outputs of ±2.5, 5, ±5, 10, ±10, or 20 V. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.
Circle 334

10-bit DAC with improved accuracy/wider compliance voltage

NE/SE5410 10-bit multiplying DAC is a pin and function compatible upgrade of the MC3410. The 16-pin analog IC guarantees relative accuracy of ±1/2 LSB over both 0 to 70 °C and −55 to 125 °C ranges. Differential nonlinearity is within 1/2 LSB; output compliance range is −2.5 to 2.5 V. Typ 2 mA is consumed from the positive supply rail and 12 mA from the negative rail. Built-in reference amplifier slews at 20 mA/μs typ; settling time is 250 ns. Output current for a full-scale step is typ within 0.5% of 3.996 mA with a 2-V reference and a 1k-Ω reference input resistor. **Signetics Corp**, 811 E Arques Ave, Sunnyvale, CA 94086.
Circle 335

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Now OEMs can buy IBM 8-inch Winchester disk assemblies. They're backed by IBM quality and a commitment to OEMs.



IBM's first products for OEMs are the Models 680 and 676 Disk Storage Assemblies.

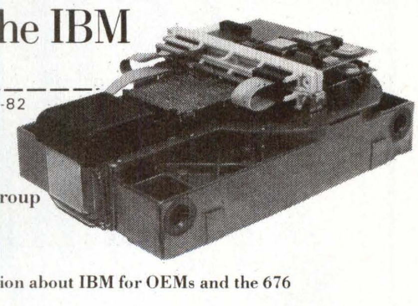
These reliable disk assemblies are backed by an OEM product support team you can call on for free consultation on interface design and software.

The IBM 680 has 64.5 MB formatted capacity and 27 ms average access time with a 1.03 MB/sec data rate. The new IBM 676 has a formatted capacity of 30.8 MB, average access time of 40 ms and a 1.25 MB/sec data rate. And it comes with a 30-month Head Disk Assembly replacement guarantee. These high-performance characteristics, combined with outstanding reliability, a wide range of environmental tolerances and worldwide parts availability make the 680 and 676 excellent choices for OEMs.

IBM wants to discuss and understand your OEM requirements. We'd like to relate your needs to our technology and experience in making quality products. To learn more about the IBM program for OEMs, as well as the Models 680 and 676 Disk Assemblies, return the coupon. Or call Bruce Prestwich, collect, at (408) 224-4622.

IBM

Come see the IBM exhibit (Booth 1320) at COMDEX in Las Vegas, November 29 to December 2.



CD-11-82

Bruce W. Prestwich
IBM
OEM Product Marketing Group
44 West Brokaw Road
San Jose, CA 95110

Please send me more information about IBM for OEMs and the 676 and 680 Disk Assemblies.

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SYSTEM COMPONENTS/
MEMORY SYSTEMS

256k-byte RAM card with parity

6000 series 256k-byte RAM card for STD BUS/Z80 processor systems features interrupting onboard parity generation/checking, 16-bit error address register, and 175-ns access 300-ns cycle times. An 8-bit base address register allows software bank selection at 1k boundaries. Card occupies 2 consecutive jumper selectable I/O ports. Software enable allows multiple RAM cards in 1 system. **Pulsar Electronics**, 323 Bell St, Pascoe Vale S, 3044 Victoria, Australia.
Circle 336

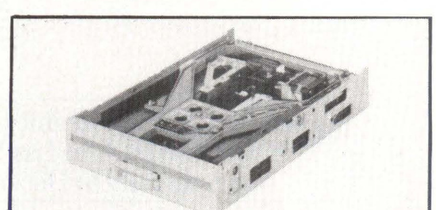
45M-byte Winchester and 8M-byte bubble memory

RD-45 8" Winchester disk drive has 45M-byte capacity and system controllers interface compatibility with militarized versions of PDP-11 and Eclipse computers and the entire NTDS family. A std system provides 90M bytes of online storage. Unit is suited for ground, airborne, and shipboard applications.

BMS1000 bubble memory system is provided as fixed and removable media, or combination thereof. A std cartridge emulates a floppy disk drive and is completely software transparent to the host computer. Capacities are up to 8M bytes. **Miltope Corp**, 1770 Walt Whitman Rd, Melville, NY 11747.
Circle 337

1.6M-byte, 8" half-height drive

Model M2896 flexible disk drive measures 2.25" x 8.55" x 12.4" (5.72 x 21.72 x 31.5 cm) and features dual Gimbal head assembly for improved performance and media wear. Drive requires half the space of std double-sided, double-density 8" drives and delivers 1.6M-byte storage capacity. It is fully compatible with SA850R and IBM media. Two ferrite manganese zinc heads enable soft, stable contact with media regardless of disk surface fluctuations. Power requirements are 5 and 24 Vdc. **Mitsubishi Electronics America, Inc**, 2200 W Artesia Blvd, Compton, CA 99220.



Circle 338

Digi-Data Value Means:

FASTER DISK BACK-UP AT LOWER COST

Digi-Data's new Series 2000 Streamer will back-up your disk at up to 9.3M bytes per minute. It can record 1600 bpi densities at 125 ips, or 3200 bpi density at 62.5 ips. That means you can back-up 92M bytes on a single tape reel in under 10 minutes . . . including rewind. And the Series 2000 is ANSI/IBM compatible with start/stop speeds of 25 or 12.5 ips available.

We designed the Series 2000 for 3200 bpi from the start. Step-write . . . microprocessor controlled read electronics . . . and extended de-skew buffer are some of the unique Digi-Data features that make 3200 bpi operation more reliable. Check other streamers for comparable features.

The Series 2000 benefits from our 20 years experience in tape drive design. Microprocessor controlled calibration and power-up diagnostics are standard. Sensors are solid state and I/O lines are properly terminated. There are no loud vacuum blowers. And the number of moving parts has been minimized.

At 50 lbs and less than 19″ depth, you won't find a smaller 1/2″ streamer. Best of all, prices start at $1850. in large OEM quantities.

The Series 2000 is complemented by a full line of 1/2″ and 1/4″ tape drives for conventional start/stop operation.

DIGI-DATA CORPORATION
8580 Dorsey Run Road
Jessup, MD 20794
(301) 498-0200 TWX 710-867-9254
®. . . **First In Value**

In Europe contact:
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Kings House, 18 King Street
Maidenhead, Berkshire
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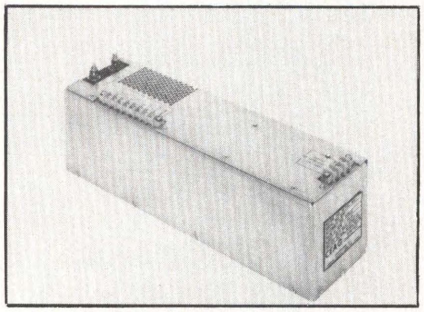
Tel. No. 0628 29555-6
Telex: 847720

CIRCLE 153

Dealer Inquiries Welcomed

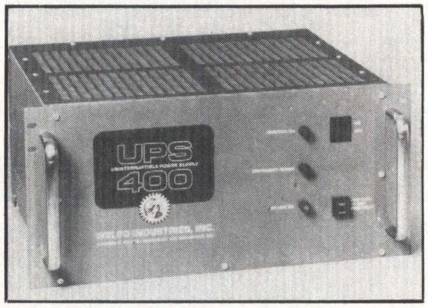
Switcher for harsh environment microprocessor applications

Model 7917 conforms with MIL-E-4158, MIL-STD-810, and MIL-STD-461, withstanding a shock of 20 G. The 180-W switcher operates from 108 to 132 V, single-phase, with 47- to 63-Hz input power. Supply operates full load with 65% min efficiency at 0 to 52 °C. MTBF is over 50k hours. In std configuration, supply delivers a 5-V, 30-A main output, with secondary outputs of 5 V at 2 A and 12 V at 1 A. Unit measures 4" x 4" x 14" (10 x 10 x 36 cm) and weighs 12 lb (5 kg). **CEAG Electric Corp, Power Supply Div**, 1324 Motor Pkwy, Hauppauge, NY 11788.



Circle 339

UPS with 400-VA output



UPS 400 provides clean transient-free sine wave with up to 400-VA continuous output maintained within ±3%. Output frequency varies less than 1%. Output waveform distortion is less than 5%. No single harmonic exceeds 3% of fundamental. Enclosure fits std 19" (48-cm) rack. Battery capacity is sized for each application. Separate 2.5-Ah 72-V battery pack is available. Internal battery charger is current limited constant voltage type. Output inverter withstands 150% overload and is protected against overload, short circuit, and overtemp. **Welco Industries, Inc**, 9027 Shell Rd, Cincinnati, OH 45236.

Circle 340

3-terminal switching regulators with wide input range

Models 3T12AP-6130 and 3T20AP-6115 3-terminal switching regulators have input voltage range of 10 to 60 Vdc. The -6130 has a 4.5- to 30-Vdc user adjustable output rated at 15 A; the 6115 is rated at 20 A and is user adjustable from 4.5 to 15 Vdc. Both provide overload and short circuit protection, and contain remote sensing and inhibit as well as soft start. Models measure 5.25" x 5" x 1.55" (13.34 x 13 x 3.94 cm). Customized hybrid power supplies can be used. In 100 pieces 3T12AP-6130 is $61 and 3T20AP-6115 is $80. **Boschert Inc**, 384 Santa Trinita Ave, Sunnyvale, CA 94086.

Circle 341

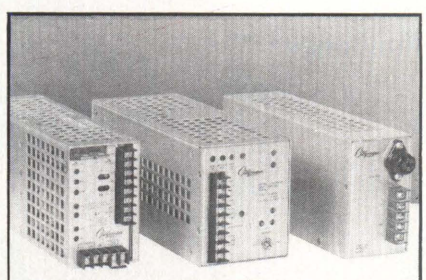
Surge protectors with rf noise filters

"Noise Filtering Surge Protectors" protect computers against voltage spikes and also filter out rf line noise. Surge protector 6676 is a 120-V 60-Hz device with 2 power outlets. Measuring 4" x 3" x 1.5" (10 x 8 x 3.8 cm), device maintains a max continuous load of 15 A and can absorb transient pulses up to 4000 A. Surge protector 6677 has max continuous load of 10 A. Providing 8 power outlets, unit measures 6.5" x 5" x 2.25" (16.5 x 13 x 5.72 cm). **INMAC**, 2465 Augustine Dr, Santa Clara, CA 95051.

Circle 342

Combined power supply, UPS

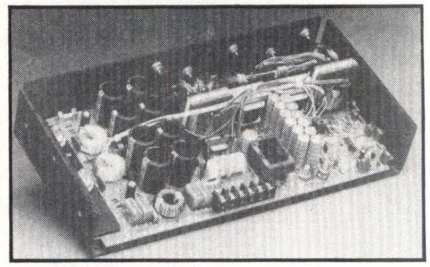
Companion™ switching regulated power supplies, associated UPS, and battery modules provide built-in protection from ac line interruptions for up to 15 min. Power supplies in 150- and 300-W output capacities are provided. UPS and battery modules provide a dc bus voltage to support power supply outputs during power line failure. Available with single- or multi-outputs, the power modules meet FCC conducted and emitted radiation specs, are UL listed, with CSA certification pending. **Lorain Products**, 1122 F St, Lorain, OH 44052.



Circle 343

SYSTEM COMPONENTS/ POWER SOURCES & PROTECTION

International 500-W switchers



5k series low profile, open frame switchers meet VDE 0806 and 0871/A safety requirements and FCC 20780/A conducted emi regulations. Four convection cooled, single-output models provide 500-W output at 40 °C. Power operates over dual-range, 90 to 130 and 180 to 264 Vac input, at full rated load. Half-bridge switching regulator design shows 80% efficiency, line and load regulation of 0.15%, and 50-mV pk-pk typ ripple and noise. Holdup time is 32 ms from nom line at full load; transient response is 400 μs max with 4% deviation. Unit price is $285. **Sierracin/Power Systems**, 20500 Plummer St, Chatsworth, CA 91311.
Circle 344

Line monitor power conditioners

Dataguard™ ac line power conditioners include model 115 plug-in, and multi-outlet strip models that absorb typ surges and spikes to 6000 V max with max energy of 50 J. Units clamp overvoltage surges at 155 V over the nominal voltage as it appears on the sine wave. Model 315 provides voltage surge suppression at 55 V clamping, 7000 V max, and includes electronic noise filtering in both hot to neutral and hot to ground modes. All are 3-wire, grounded units with 15-A max capacity. List prices range from $49.95 to $193.95. **SGL Waber Electric**, 300 Harvard Ave, Westville, NJ 08093.
Circle 345

Primary cells with lithium anode

High energy density (1-Wh/cm^3) primary cells with lithium as anode material allow a high current drain rate at −40 to 150 °C. Average open circuit voltage is 3.9 V. Contained in corrosion resistant 304L stainless steel, each nonpressurized hermetic cell is individually fused for long life. Test data are available on safety and performance of the cells in environmental extremes. **Electrochem Industries/Wilson Greatbatch Ltd**, 9990 Wehrle Dr, Clarence, NY 14031.
Circle 346

New LM-4. The 40-Channel Logic Monitor you hold in your hand.

Now, there's a unique new way to speed and simplify your work with complex digital circuits. By simultaneously monitoring up to 40 points in a logic system with a compact, easy-to-use instrument that's faster than a scope and safer than a voltmeter. Our new multi-family LM-4. At $199.00,*it's one of the best buys in logic today!

Simply slip its 40-pin IC test clip over your CMOS or TTL ROM, RAM, microprocessor or MSI/LSI chip and instantly see the logic state of each pin on a big, easy-to-read liquid crystal display.

But that's only the beginning. You can wire the LM-4 into a computer bus; fit it with two 16-pin test clips or sockets for comparing known good and questionable ICs; use it as a clip-on display for micros, minis and other computers during design, setup, testing, troubleshooting ...there's no limit to the ways LM-4 can save you time and money!

Measuring just 5.9 × 3.2 × 1.2," the pocket-sized LM-4 comes with a 24" 40-conductor ribbon cable terminated in a 40-pin IC test clip, plus instructions/applications manual and high-impact carrying case. (An optional Universal Cable Kit is also available for special interfacing requirements, priced at $75.00.*)

So whatever the job–in design, production or service–simplify your testing with the power of 40-channel monitoring: Order your LM-4 today.

Call toll-free for details
1-800-243-6077
During business hours

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Canada: Len Finkler Ltd., Downsview, Ontario.

* U.S. Resale only; price, specifications subject to change without notice.

SEE US AT MIDCON BOOTH #s 615, 617

CIRCLE 158

Expanded BASIC

Enhanced version of BASIC provides full compatibility under the company's DX10 Micro, DX10, and DNOS operating systems. The software includes interactive development/debugging capabilities and program security features. The enhanced BASIC is a superset of ANSI std BASIC. Operating modes include development mode with breakpoints and fast mode that eliminates debug support. Prices range from approx $700 to $3250. **Texas Instruments Inc**, PO Box 202146, H-630, Dallas, TX 75220. **Circle 347**

Interactive graphics language

Peachtree Graphics Language (PGL) is an interactive graphics software package for CP/M based computers. At the heart of the language is a device independent programming system for both input and output. Two- and 3-D graphics transformations, zoom, pan, strip chart scrolling, multi-independent graphics, and rotation are supported. CP/M 86 and IBM Personal Computer versions of PGL will be available this fall. **Peachtree Software Inc**, 3445 Peachtree Rd NE, Atlanta, GA 30326. **Circle 348**

Pascal modules for robot programming language

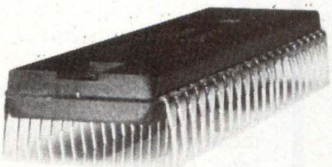
Completely embedded in Pascal, PASRO can be used to program any microcomputer controlled robot with an ISO std compiler. PASRO modules form part of a Pascal system library and link to the running Pascal program routines. The language offers elements to control the robot and claw, elements to address process peripherals and sensors, predefined data types for robot control programming, and arithmetic operators for flexible manipulation of new data types. Available the first quarter of 1983, PASRO will cost about $750. **Biomatik GmbH**, Carl-Mez-Str 81-83, D-7800 Freiburg i Br, West Germany. **Circle 349**

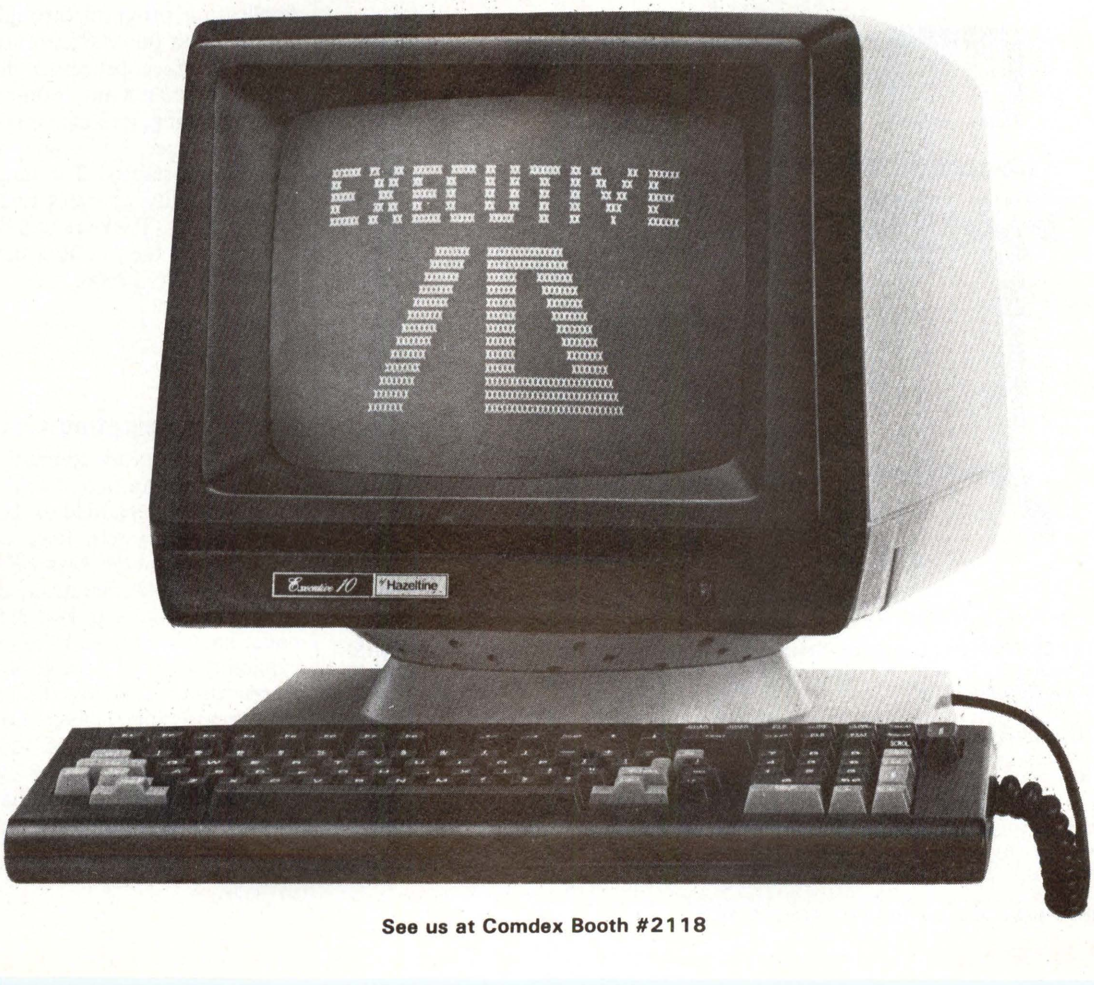
Pascal cross compiler in source/object code versions

A Pascal cross compiler for the Intel 8080/8085, Pascal-85 portable program is available in source code version for installation on a variety of host computers. Object code only version can be initially licensed for DEC computers. Compiler translates nearly all ISO std Pascal to native 8080 assembly language. Pascal extensions include separate compilation, bit manipulation, interrupt procedures, and direct memory accessing. Package includes enhanced 8080/8085 cross assembler and linking loader programs. License fees range from $4900 to $10,000. **Microtec**, PO Box 60337, Sunnyvale, CA 94088. **Circle 350**

Enhanced Forth compiler for Tektronix development systems

A Forth compiler for Tektronix 8550 and 8002 microprocessor development labs, proForth™ is Forth-79 compatible and separates target code from system software during its 1-pass compilation process. Procedure names are stored in a system/dictionary memory and are linked to the runtime code in target ROM for interactive symbolic testing during in-circuit emulation. Smooth interface and intermix of assembly code with high level code is provided. Runtime nucleus occupies 1300 bytes. System's editor, assembler, and compiler are normally resident for development/debug. **Microsystems, Inc**, 2500 E Foothill Blvd, Pasadena, CA 91107. **Circle 351**




EXECUTIVE
10
Executive 10
Hazeltine

SYSTEM COMPONENTS/ SOFTWARE

High level language compatible with PL/M compilers

To support software development on MCS-51 microcontrollers, the PL/M 51 package iMDX 352 is an alternative to ASM 51 assembly language. The modular software package supports Boolean processing and can link its modules to ASM modules. A linking and relocating utility and library manager are included. Object modules are compatible with in-circuit emulators and emulation vehicles for MCS processors. Provided on diskettes, the software runs under ISIS-II on the Intellec 64k microcomputer development system. Domestic price is $2950. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 352

Modular program with screen displays stored as disk files

MCDISPLAY packages for CP/M systems include display utility DISPLAYDEF for user defined screen displays on cursor addressable terminals/CRTs. Displays are saved as disk files and used by the application program through directives contained in the DISPLAYASM user interface. Interface processes data entries, handles messages and prompts, provides error checking, and converts entries into string, integer, or single- or double-precision variables. The language independent utility operates under BASIC-80 and BASCOM. Package is $175. **Master-Computing, Inc**, 11 Regency Hills Dr, Greenville, SC 29606.

Circle 353

EXORmacs operating systems

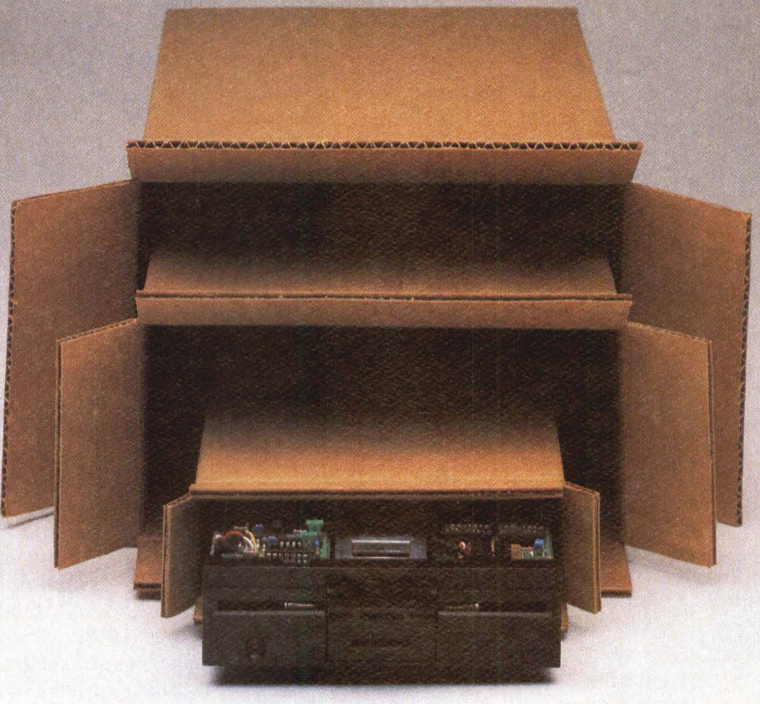
UNIDOS, a UNIX V7 compatible OS, and CP/M-68K, an MC68000 based version of CP/M, have been added to the EXORmacs development system line. UNIDOS features an assembler, text editor, linkage editor, symbolic debugger, and C compiler. CP/M-68K, with two mag disk formats, has monitor and file management capabilities. CP/M format will be on 8″ floppy disk, including the CP/M-68K OS, MC68000 assembler, linker, librarian, and file management utilities. VERSAdos format will be available on 8″ floppy, 16″ SMD, and 8″ Lark disk media. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.

Circle 354

ADVANCED AND EVER ADVANCING **MITSUBISHI ELECTRONICS**

INTRODUCING 1.6 Mb REPACKAGED

See us at COMDEX '82 Booth #242



More Storage. Less Space.

It's new and it's from Mitsubishi: the M4854 half-height 5¼" flexible drive. The M4854 delivers up to 1.6 Mb of storage–the same as most 8" drives–yet it takes up only half as much space as a conventional 5¼" drive. Not bad, considering the M4854 is about the same price as most conventional 5¼" disk drives. And just in case you prefer a half-height unit with 1.0 Mb of storage, Mitsubishi also makes the M4853.

More Features. Less Money.

As with all other Mitsubishi flexible disk drives, the M4854, 1.6 Mb, 5¼" half-height offers more than a lot of memory. It gives you many features:

Like a head load mechanism with all ferrite heads. A patented circular Gimbal support that ensures stable read/write operation and long media life. An advanced Direct Drive brushless DC Motor that eliminates all concern for changing drive belts. It also provides the torque necessary to reduce the disk rotation starting time to only 250 milliseconds. And for speed, the M4854 has a steel band head positioning mechanism which results in a track-to-track time of only three milliseconds and average access time of 91 milliseconds.

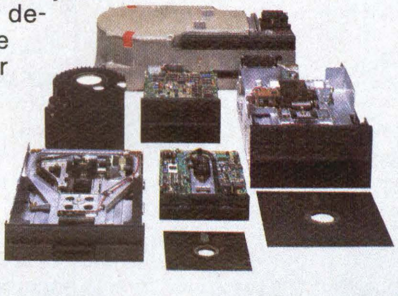
You'll also find Mitsubishi OEM prices are extremely competitive.

More Products. Less Hassle.

Of course, features like these aren't just limited to Mitsubishi 5¼" half-height drives. You'll find them throughout the entire Mitsubishi line, which includes standard-height 5¼" fixed and flexible drives, 8" fixed drives and 8" full and half-height flexible drives.

More Reliability. Less Maintenance.

Now that you know what goes into our drives, you'll know why they have a MTBF rate of 10,000 POH or more. Unit life is even more impressive–5 years or 20,000 power-on hours, whichever occurs first. No matter which type of drive you need, Mitsubishi has a package that's just right for you. For details on the entire line, contact your Mitsubishi representative today.



MITSUBISHI ELECTRONICS

MITSUBISHI ELECTRONICS AMERICA, INC.
COMPUTER PERIPHERALS DIVISION
2200 W. Artesia Blvd., Compton, CA 90220 (213) 979-6055
Boston (617) 938-1220 · Dallas (214) 258-1266

CIRCLE 163

Programmable automation controller handles 8 axes

ICC 3000 simultaneously controls up to 8 axes of closed loop, coordinated motion. Proprietary technology eliminates tachometers and optical encoders. Hierarchical computer architecture incorporates 9 microprocessors with high speed bidirectional communication and interface. A high level automation programming language, CYBER-BASIC™, provides for realtime control programs; English-like commands interface process elements while providing full arithmetic functions, data acquisition, and productivity reporting. System prices start at $6500. **International Cybernetics Corp**, 263 Kappa Dr, Pittsburgh, PA 15238.

Circle 355

Preprogrammed single-board multiloop PID controllers

Preprogrammed microprocessor based controllers for up to 8 cascadable PID loops, the CINCH PAC™ models 30 and 31 have adaptive gain on error/squared error, bumpless transfer, warning alarm testing on process variables, and controller output. Also included are anti-reset windup, forward/reverse gain, ramp and soak, auto-output limiting, and auto-fallback conditions. Control functions contained in each controller allow central host to monitor only. Both models are compatible with CINCHNET™ control network. Model 30 supports 16 analog inputs, 6 analog outputs, and 16 alarm closures; model 31 supports 16 analog inputs and 8 analog outputs. **Inconix Corp**, 10 Tech Circle, Natick, MA 01760.

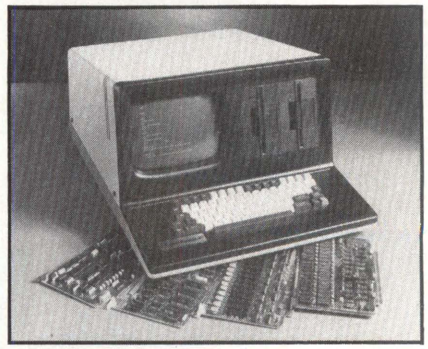
Circle 356

Tough industrial control chassis

ICP-100 chassis is suitable for industrial control and data acquisition applications. Configuration includes an 8-slot MULTIBUS card cage and motherboard with 6- or 12-slot option. Chassis comes with ±5-, ±12-, and ±24-V power supply. Power line filter protects interior boards from surges. Battery backup source and power fail detection on logic save user programming and dynamic memory during power outages. Rear panel cutouts are arranged for flexible system I/O configuration. **Sibthorp Systems, Inc**, 800 Cox Ave, Erlanger, KY 41018.

Circle 357

High performance desktop controller



EXORset 35 easily configures for industrial and lab automation, data acquisition, and analysis applications. Based on the 8/16-bit MC6809 microprocessor, the controller is suitable for high level language program development. Complete packaged system includes ASCII keyboard with 16 user definable function keys, 9" (23-cm) 320- x 256-dot CRT, and up to 328k bytes of optional mass storage on floppy disks. Onboard I/O includes asynchronous serial communications port, 16-bit parallel port, and triple 16-bit programmable counter/timer. Prices range from $3305 to $4675. **Motorola Semiconductor Products Inc**, PO Box 20912, Phoenix, AZ 85036.

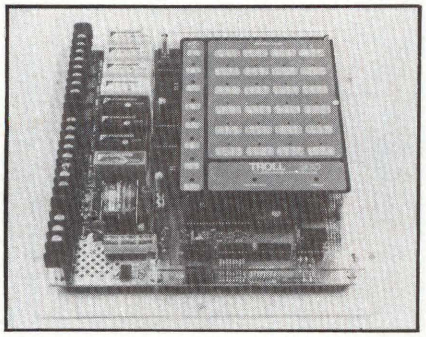
Circle 358

Programmable alarm controller

Microprocessor based programmable alarm controller monitors 16 digital and 4 analog signals, and provides lighted alarm indicators, control outputs, critical value response, and a hardcopy record. The controller reacts automatically to alarm input via 16 control relay outputs that can trigger system shutdown, speed reduction, or opening/closing of valves. Time switch program allows each control relay output to be multiplexed over 14 digital/analog events, for a total of 224 events that can be responded to automatically. **Selco Products Co**, 7580 Stage Rd, Buena Park, CA 90621.

Circle 359

Segmented controller and 4-function timer/counter



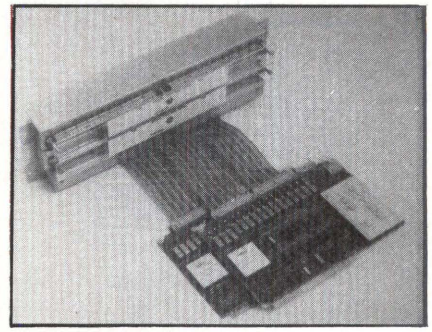
Troll-200 programmable controller uses segmented plastic blocks with connector pins representing 256 combinations/ block. Controller has a 6-rung x 4-element switch matrix memory, uses ladder logic, and provides 8 channels. Troll-100, with up to 4 timer/counter functions, has memory in a 4-row x 6-element switch matrix and 10 channels, and a ladder programming language. Both units provide 3 status indicators per function, power/run indicators, error diagnostics, and time scan of less than 10 ms. Units have a modified RS-422 format and provide analog capability. Base price for either unit is $300. **Conrac Corp, Cramer Div**, Old Saybrook, CT 06475. **Circle 360**

Rugged portable computer simulates peripherals

Husky is a portable computer with 144k-byte data memory and a 4-line, 128-char display. The CP/M compatible computer has RS-232/V.24 port backed with software selected protocols, data rates, and parameters. Husky will simulate a peripheral to DEC, IBM, and Honeywell computers. In "clone" mode, one Husky will reproduce its contents in another. Sealed aluminum case with membrane protected keyboard measures 9.5" x 8" x 1.75" (24.1 x 20 x 4.45 cm). The battery powered unit operates in 15' (5 m) of water. **Redland Automation, Inc, Sarasota Div**, 1500 N Washington Blvd, Sarasota, FL 33577.

Circle 361

Low level input system for TM-990 bus



410 series input modules fit directly into the TM-990 bus to simultaneously handle thermocouples, RTD, strain gauge, and mV signals. Model 410-RL provides direct flying capacitor multiplexing for 8 or 16 channels of differential input. It accommodates up to 7 410-RX expander cards, each with 8 or 16 channels, for 128 channels max of 250-V common mode protected differential input. Programmable sequential or random channel access, selection of triggering modes, and 8 strappable multipriority interrupt levels are provided. Prices for 410-RL/RX start under $900. **ADAC Corp**, 70 Tower Office Pk, Woburn, MA 01801.
Circle 362

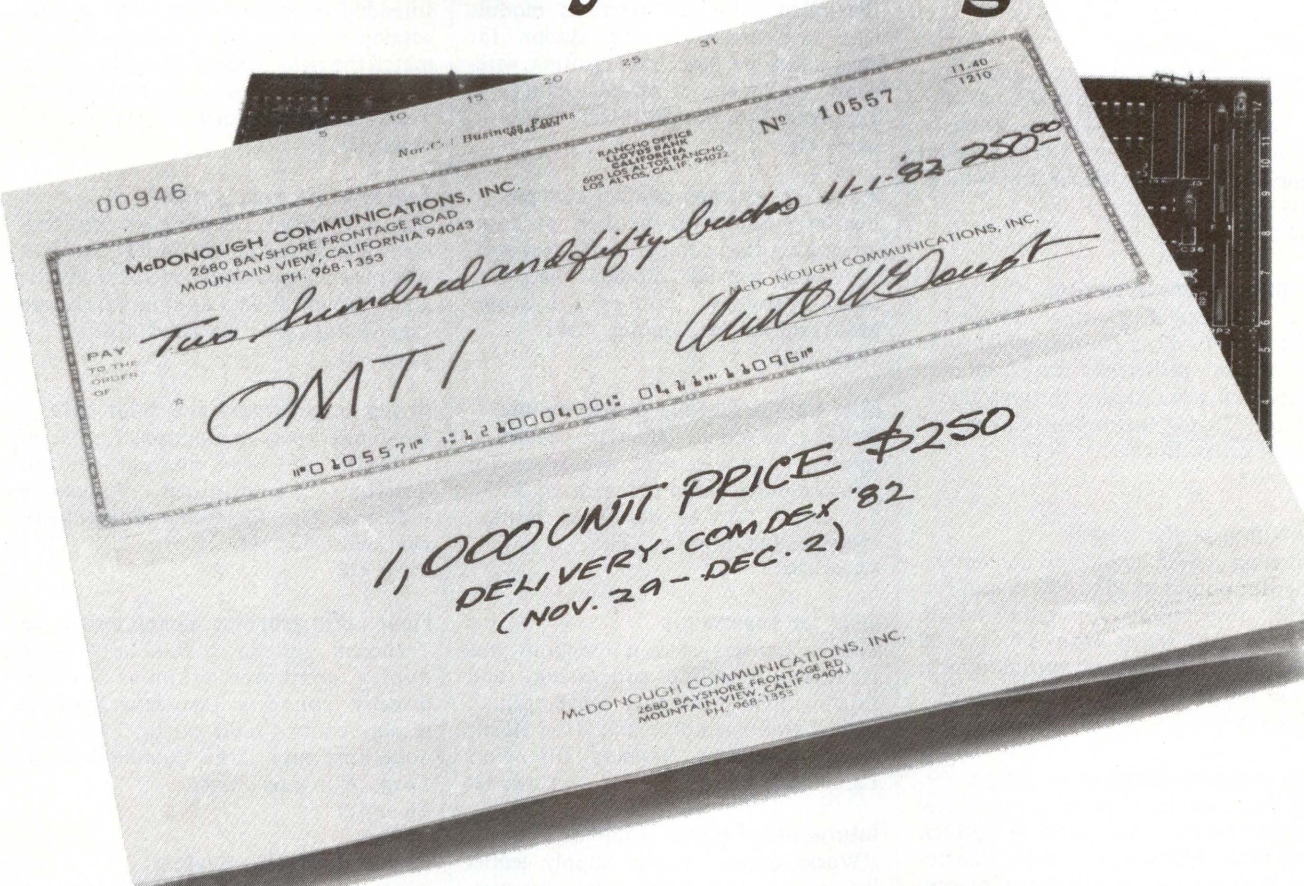
Programmable control for AIM-65, SYM-1

UC/L System One hardware/software package converts the AIM-65 or SYM-1 microcomputer into a programmable controller. Interface module and cable connect the microcomputer directly to any std I/O module mounting board to provide optically isolated inputs and outputs, along with ac and dc power handling. The 36 instructions in UC/L high level programming language include input sensing, output switching, delay, and step motor control. Linkage to external code is provided for operations unavailable in the UC/L instruction set or requiring higher speed execution. Package quantity-1 cost is $175. **Polyarts Assocs, Inc**, PO Box 21169, Seattle, WA 98111.
Circle 363

Experts needed
How about reviewing technical articles for Computer Design? Circle **501** *on the Reader Inquiry Card.*

OMTI introduces a brand new 5¼" intelligent Disk Controller specifically designed to blow your mind...

but not your budget.



Keep this price in mind when you're adding up these standard 20L features:

- 5¾ x 8″ form factor
- Formatted capacity increased by 20%
- Full track buffer
- SASI BUS simplifies host attachments

And, of course, all of the standard features such as: ECC, on-board data separator, 1.0 megabyte data transfer rate, etc., etc., etc., etc., and so forth.

A simple request will get you all the details. If you're on the verge of buying, call our marketing department for instant information and outstanding prices.

Also, if you're looking for cartridge or floppy support for your fixed disk... talk to us about our new OMTI Models 510A and 520A.

By the way, a good place to look would be our *OMTI Suite in the Desert Inn during the Las Vegas COMDEX gathering.*

First come... first save!

WHAT'S AN OMTI ?

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CIRCLE 168

Choosing applications software
A Guide to Successful Software Selection explains how to identify internal needs, compare features and capabilities, and evaluate vendor demonstrations. **Software International Corp, subsidiary of General Electric Information Services Co,** Andover, Mass.
Circle 410

Multiloop controller
Diagrams, specs, and installation information for MLC 100™ digital controller for continuous processes are given in product folder. **INCONIX Corp, Control Logic Industrial Systems Group,** Natick, Mass.
Circle 411

Designing process control
Your Successful Control Project... Requires More Than Hardware highlights MOD system's project services, from project planning and design through maintenance. **Taylor Instrument Co, div of Sybron Corp,** Rochester, NY.
Circle 412

Switching power supply
Switching power and dc-dc converters, with max output of 25 to 100 W and 1 to 50 W, respectively, are tabulated on separate data sheets with dimensional drawings and socket configurations. **Power General,** Canton, Mass.
Circle 413

High capacity Winchester drives
Brochure examines 82M-byte model 5380 and 165M-byte model 53160 14" drives, both with 1000k-byte/s data transfer rate. **Kennedy Co, an Allegheny International Co,** Monrovia, Calif.
Circle 414

Modular power supplies
Models 926, 927, 928, 972, 974, and 976 high efficiency ac-dc power supplies and 12 low profile dc-dc converters, in PC or chassis mount versions, are introduced in catalog. **Analog Devices,** Norwood, Mass.
Circle 415

1-A rfi noise filters
Pamphlet describes F1100, F1200, and F1300 power line filters, with circuit schematics, dimensional drawings, and technical specs. **Curtis Industries, Inc,** Milwaukee, Wis.
Circle 416

20M- to 116M-byte Winchesters
Three spec sheets detail low to high capacity 8" Winchester disk drives with SA1000/ST512 and SMD/ANSI interfaces. **MegaVault, an SLI company,** Woodland Hills, Calif.
Circle 417

Automatic backplane testing
Illustrated brochure describes module N221 interconnection test system for backplanes or bare boards using wire-wrap, PC panels, or mixed technology. **Teradyne, Inc,** Boston, Mass.
Circle 418

Industrial process control system
Leaflet outlines off-the-shelf package, integrating DEC compatible CyNet software and RDS-1600 modular hardware into process control system. **MultiTronics, Inc,** Dublin, Calif.
Circle 419

Mini uninterruptible power system
Bulletin describes standard features, options, and electrical site specs for minicomputer based UPS with 1-, 2-, 3-, 5-, and 7.5-kVA, 50/60-Hz ratings. **CYBEREX Inc,** Mentor, Ohio.
Circle 420

CPUs for superminis
Brochure covers CPUs in 3 sections: bus structure, pipeline processing, and floating point processors; cache, virtual, and shared memory; and I/O. **Harris Corp, Computer Systems Div,** Fort Lauderdale, Fla. **Circle 421**

International power supplies
"World Series" power supply leaflet lists single- and multi-output supplies, along with safety requirements, for international markets. **Deltron Inc,** North Wales, Pa.
Circle 422

Analog I/O for micros
Over 25 hardware and software items are introduced in 336-p catalog, which gives full technical specs and prices. **Data Translation,** Marlboro, Mass.
Circle 423

Data communications networks
Altos-Net software for networking the company's 16-bit micros, along with Ethernet networking and mainframe communications protocol software, is covered in pamphlet. **Altos Computer Systems,** San Jose, Calif. **Circle 424**

Thermistors
Short-form catalog provides tables for resistance deviation beta tolerance, tempco, and resistance temperature conversion. **Fenwal Electronics, div of Kidde, Inc,** Framingham, Mass.
Circle 425

Plug-in probes
Intended as an add-in to 1982 general catalog, selection guide explains how to match the right scope to the right plug-in and probe for 7000 series mainframes. **Tektronix, Inc,** Lexington, Mass.
Circle 426

Temperature measurement
The 500-p 1983 *Temperature Measurement Handbook* covers 14,000 temperature measurement and control products, giving technical data and prices. **Omega Engineering, Inc,** Stamford, Conn.
Circle 427

Hi res monochrome and color CRTs
Functional specs and options for line of 7" to 19" (18- to 48-cm) high contrast terminals are outlined. **Panasonic Industrial Co, Electronic Components Div,** Secaucus, NJ.
Circle 428

Fiber optic graphics communications
Technical bulletin covers how LS-100 duplex computer graphics modem directly connects IBM 3250 graphics display control units up to 5 km with noise immunity. **Artel Communications Corp,** Worcester, Mass.
Circle 429

Packet switching system
SL-10 packet switching technique and data communications network management are discussed in brochure. **Northern Telecom Inc,** Richardson, Tex.
Circle 430

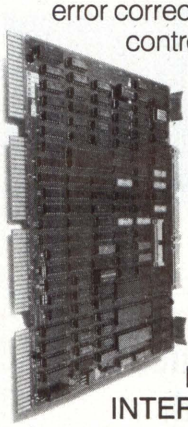
Test and measurement equipment
Stock catalog features half-rack waveform monitor and companion vectorscope for audio/video testing. **Leader Instruments Corp,** Hauppauge, NY.
Circle 431

High performance disk subsystem
Data sheet for STC 8675, designed for 4341 CPU users, gives operating and electromechanical specs; system has 2 storage directors and 4 disk drives. **Storage Technology Corp,** Louisville, Colo.
Circle 432

DILOG INTERFACES WINCHESTER/BACK-UP PDP-11*

You can't find a better, high-performance line of low-cost, single board, disc and tape controllers for your PDP-11 data storage system. All Winchester disc and ½″ tape controllers are based on uP architecture and automated design common to the thousands of DILOG controllers in use. So they consistently offer you best price/performance.

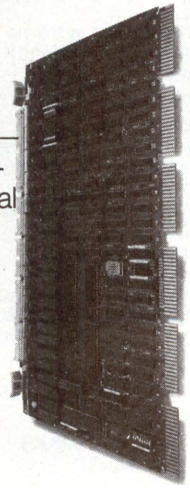
The vital time-saving and data base protecting features you want, including diagnostic test/self-test/error correction/etc., are all built into each intelligent controller. You'll also find RT-11, RSX-11, RSTS, IAS, MUMPS, DSM or VMS software compatibility, plus I/O compatibility with all popular drives.



WINCHESTER/SMD/CMD CONTROLLERS

These controllers mate with larger capacity hard disc drives employing RK, RM and RP emulations. The following is a partial listing of models:

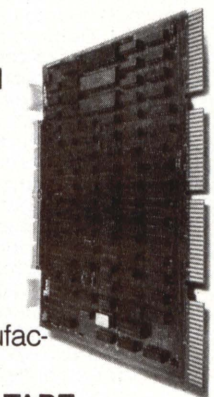
NEW—UNIVERSAL SMD INTERFACE COMPATIBLE—Model DU215—Interfaces UNIBUS to SMD I/O drives—switch selectable RK06/RK07—two 8″ or 14″ Winchester SMD/CMD drives to 300 MB capacity (mix or match without any component change)—56-bit ECC—88% utilization of unformatted storage capacity—exclusive universal formatting.



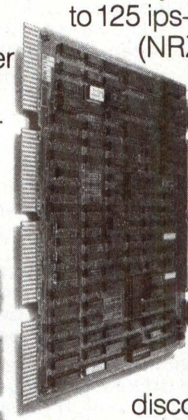
NEW—SMD INTERFACE COMPATIBLE—Model DU218—Full RM02/RM05/RP06 media compatibility—interfaces PDP-11/04 through 11/60 computers with up to four Winchester, or CDC9762/9766 equivalent disc drives employing industry standard SMD interface, as well as Memorex 677/RP06 type drives—includes three sector buffering, 32-bit ECC and dual port capability.

MAGNETIC TAPE CONTROLLERS

These ½″ mag tape controllers/couplers handle standard start-stop and streaming drives with TM-11 or TS-11 emulations.



½″ STREAMING/START-STOP COMPATIBLE—Model DU130—Handles up to eight 9-track, 800/1600 BPI industry standard drives at 12.5 ips to 125 ips—interfaces dual density (NRZI/PE) drives from all manufacturers. TM-11 emulation.



NEW—½″ MAGNETIC TAPE COMPATIBLE—Model DU132—Emulates TS-11—interfaces up to four start-stop or streamer drives, including "Cache Streamer"—**12.5 ips to 125 ips speeds—exclusive 800/1600 BPI dual density—also interfaces GCR transports.

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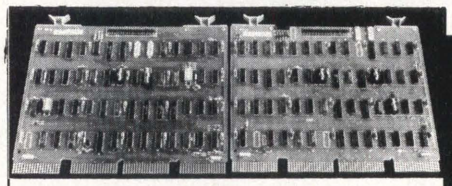
The new CmC Model LA-12, a self-contained and sophisticated unit used by digital designers, is now available for nearly 50% less than any other on the market. Features include 12-channel width, 16-word storage, data capture rate in excess of 10 MHz, clock qualifier, trigger input, 3 trigger qualifiers, selectable polarities of clock, trigger and qualifier and built-in display (no oscilloscope needed). **CONNECTICUT MICROCOMPUTER, INC**, 36 Del Mar Drive, Brookfield, CT 06804. Tel: (203)775-4595, TWX (710) 456-0052. **CIRCLE 476**



New DEC-compatible shared memory link obsoletes traditional CPU links.

The PPL-1 Peripheral Processor Link is a unique shared memory interface between any two Q-bus (LSI-11) and/or Unibus (PDP-11)-based DEC CPU's. Two quad boards and a connecting cable link the peripheral unit with the host. Up to 32KB of memory can be accessed by the peripheral processor in 4KB boundaries anywhere in the address space of the host. Address spaces are 18 bits for Unibus and 22 bits for the Q-bus. This memory sharing does not require software to support the link. 16 vectored interrupts (8 from each direction) provide necessary hardware for protocol implementation.

DEC, LSI-11, PDP-11 Q-bus and Unibus are registered trademarks of Digital Equipment Corp.

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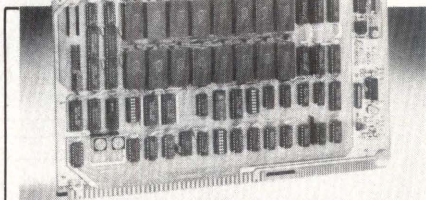
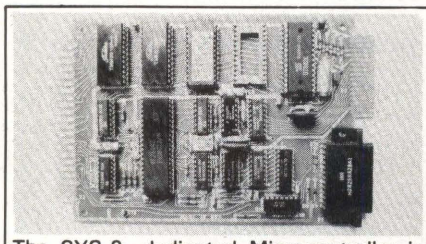
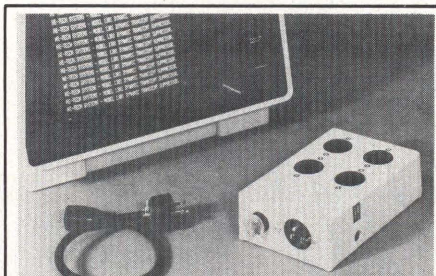


NEW – MULTIBUS READ/WRITE PROM BOARD

The EEPROM-32 is a Multibus compatible EEPROM/EPROM board that utilizes the latest in program-store technology. With E2PROMs, reprogramming now takes only milliseconds instead of hours of expensive manpower. The EEPROM-32 accepts 2815, 2816 type E2PROMS or 2716 UV-erasable EPROMS, with an 8 or 16 bit data path and a 20 bit address space. Delivery from stock...Price: $695 unpopulated. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake Ct, San Diego, CA 92123. Tel: (714)292-0242, outside CA (800) 854-7086, TLX (910)335-1167. **CIRCLE 478**



The SYS-2, dedicated Microcontroller is ready-to-run requiring only a terminal and 5V supply. The Control Basic language guarantees hassle-free program development and opens computer control to those of nearly every level of expertise. Standard features are: EPROM programmer, multichannel A/D conversion, eight 50V-1/2A outputs, 8 switch closure inputs, directly addresses more than 2000 peripheral devices, auto-run, moniter and debug firmware, and more. Support products and other microcontrollers available. **OCTAGON SYSTEMS CORPORATION**, 5150 W 80th Ave, Westminster, CO 80030.
Tel: (303)426-8540. **CIRCLE 479**



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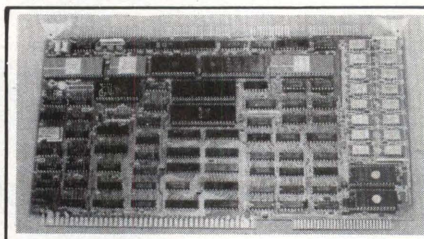
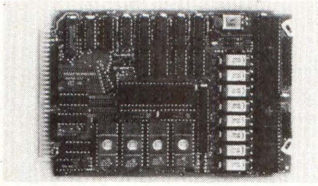
Features Auto Ranging Lo Level clamping & transient indicator at 20% above line voltage waveform peak. 5 nanosecond response time suited for MOS or TTL circuitry, Op Amps & comparators, computers, microprocessor controlled devices. Stock priced $350. **HI-TECH SYSTEMS, INC**, 3985 N State Rd 39, Lebanon, IN 46052. Tel: TOLL FREE (800)428-4403, Indiana (317)482-5878. **CIRCLE 480**



THE SBC80A designed for multiprocessor/slave or I/O processor, has on card Z80A-CPU; DMA; 128K dual ported RAM, no wait state, byte/word accessible; Eprom sockets up to 32K; 2 RS232; 2 parallel ports; memory map Prom; 3 counter/timer; floppy controller; hard disk interface; math chip AM9511; 20 bit Intel multibus 21 vectored interrupts; auxiliary power input for stand alone. From $895 (qty 1). **INNOVATIVE RESEARCH INC**, 17071 Kampen Lanen, Huntington Beach, CA 92647. Tel: (714)842-0492. Multibus trade mark of Intel.

SBC80A Microcomputer

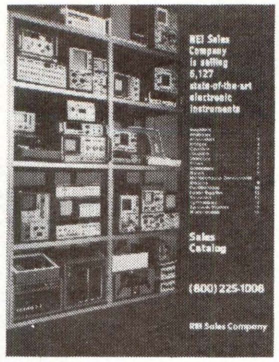
CIRCLE 481



STD BUS SINGLE BOARD MICROCOMPUTER

The MCPU-800 features a 4 MHZ Z80A, 64K RAM, 32K ROM, 32 I/O bits and a programmable serial port on a single STD size card. Memory mapping and I/O space expansion are under software control. Optional software includes a versatile Monitor, a 2K BASIC interpreter, and a full function 8K BASIC. Many applications may be served by this card alone, although full STD bus compatibility is maintained. 16K RAM MCPU-800 from $560, full 64K system for $695. **MILLER TECHNOLOGY**, 647 N Santa Cruz Ave, Los Gatos, CA 95030. Tel: (408)395-2032.

CIRCLE 482



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The ES-500 Line Conditioner protects computers from AC power line brownouts, voltage surges and spikes. The ES-500 ferroresonant 500VA unit provides isolation, regulation and noise suppression in a compact, attractive package. Meters optional. Available from stock—Part #ES-500-$385, Part #ES-500M-$440. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake CT, San Diego, CA 92123. Tel: (714)292-0242, TOLL FREE (800) 854-7086, TLX (910)335-1167.

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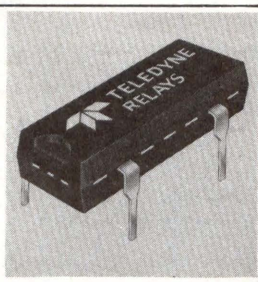
SOLID STATE HYBRID AC/DC RELAY



Teledyne's 641 AC relay provides a triac output rated at ½ amp up to 50°C ambient without a heat sink. Transformer isolation is 2500VRMS, turn-on time is 20μsec. Other features include TTL compatible input, 10 amp surge capability, low minimum output current (5mA), UL recognized, CSA certified. Hybrid microcircuit assembly is molded in a TO-116 plastic DIP. Model 643 is the DC version. Priced in quantity from $5.80 to $6.20 ea. **TELEDYNE RELAYS**, 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213) 777-0077.

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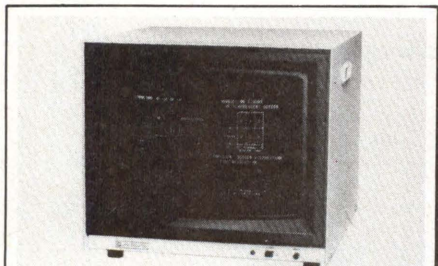

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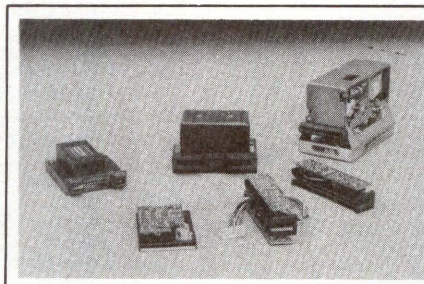

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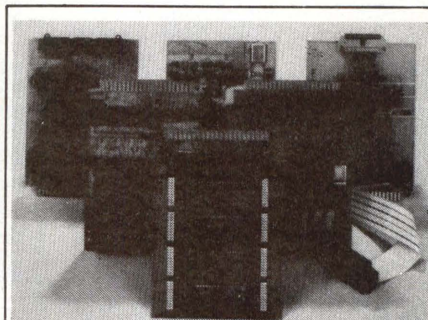

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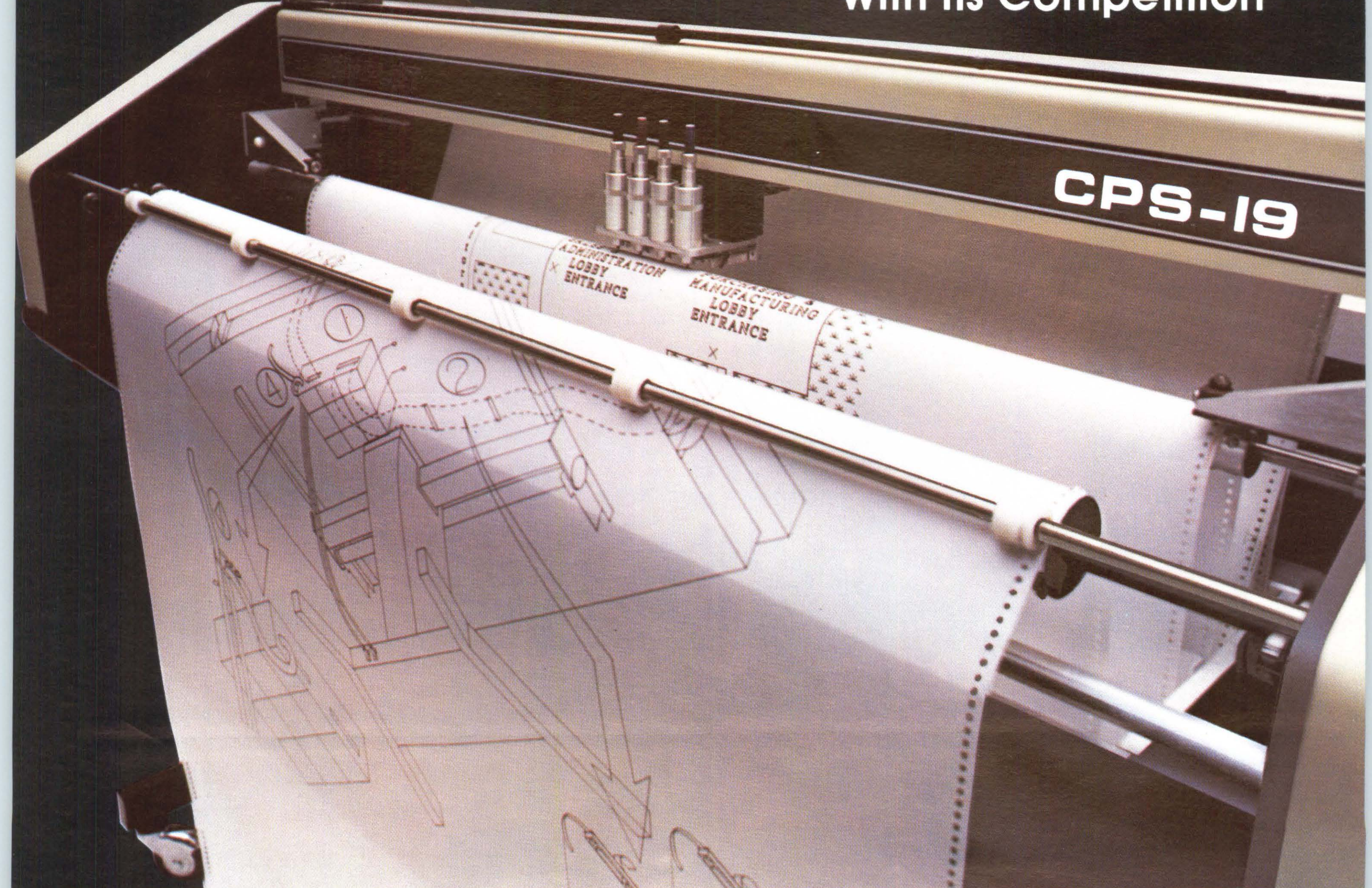

We invite comparison on the basis of quality, reliability and performance... even though the comparison may seem unfair since the Houston Instrument CØMPLØT® costs much less than the competition. The competitive edge of the CPS-19 is based on solid design and meaningful capabilities. The end result is a highly cost effective 34.5" four-pen plotter that performs tirelessly and flawlessly on its owner's behalf. At a bottom line price of only $14,950*, the Houston Instrument CPS-19 full-size plotter is thousands of dollars more affordable than others of comparable performance.

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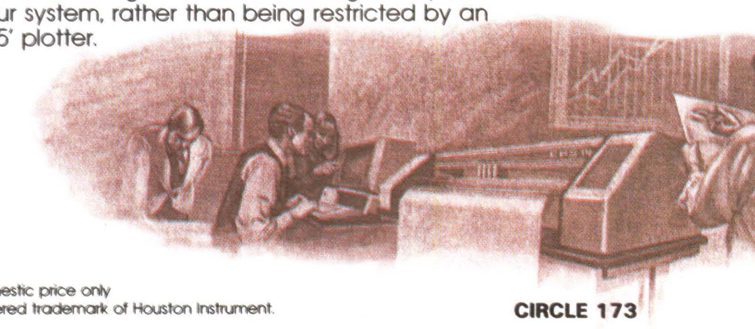

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