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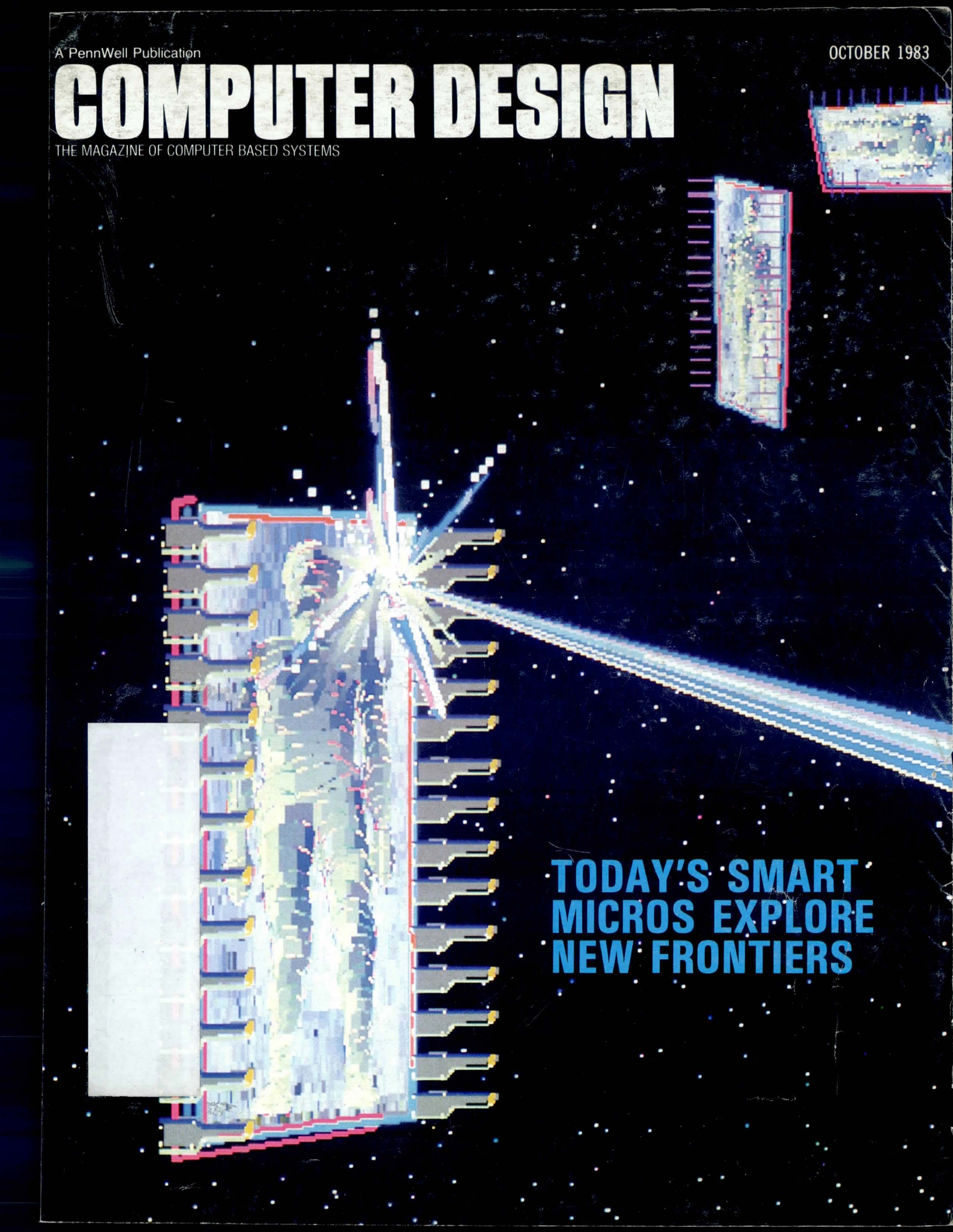
OCTOBER 1983

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS



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CIRCLE 1

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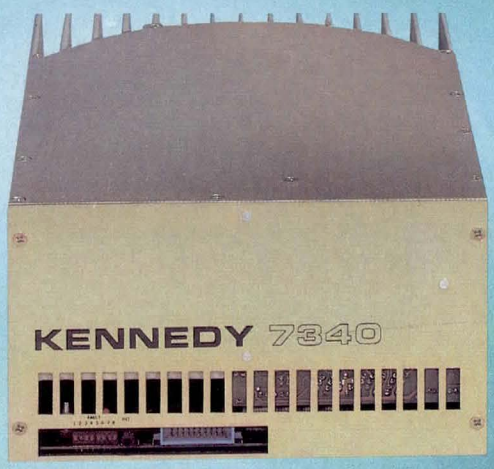

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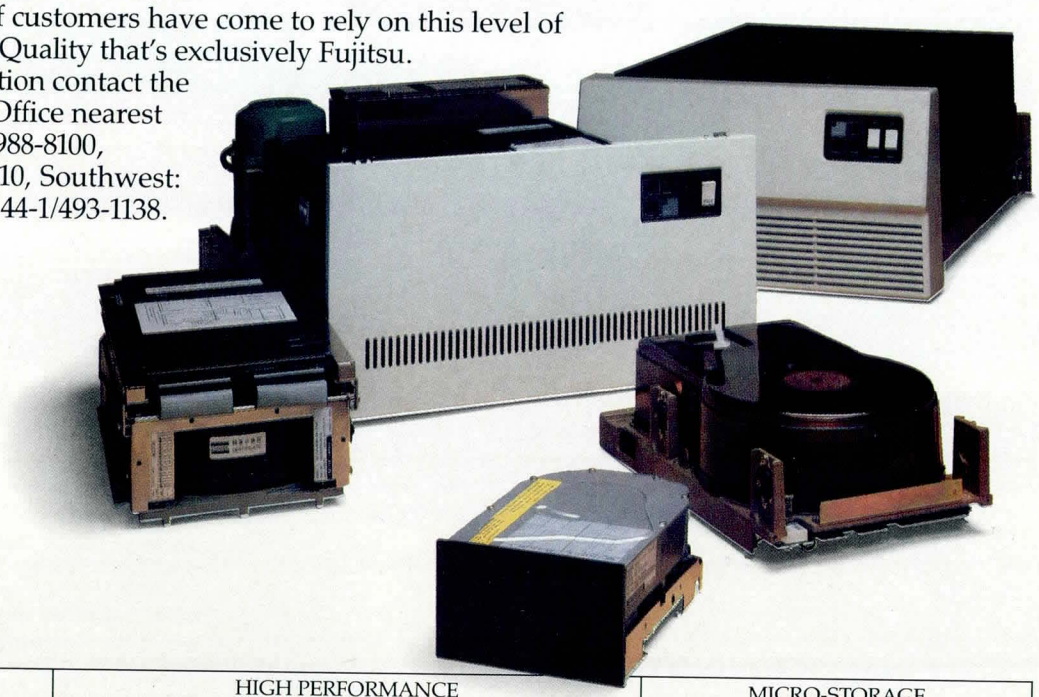

	HIGH PERFORMANCE			MICRO-STORAGE	
	A 14-INCH	B 10½-INCH	C 8-INCH	D 8-INCH	E 5¼-INCH
CAPACITY (M Bytes)	84 / 168 / 336	474	48 / 84 / 168	24 / 48	7 / 13 / 20 / 27
AVG. POSITIONING TIME (ms)	27	18	20	70	83
TRANSFER RATE (K Bytes/s)	1,012	1,859	1,229	593 / 1,200*	625
INTERFACE	SMD	Modified SMD	SMD	SA4000	ST506/SA4000
POSITIONING METHOD	Rotary Voice-Coil	Rotary Voice-Coil	Rotary Voice-Coil	Buffered Stepper	Buffered Stepper

*48 M Bytes Configuration available only in 1200 K Bytes/s

FUJITSU

CIRCLE 3

UP FRONT

Signal processing ICs soon to be available

Gallium arsenide digital ICs will be released as commercial products by Harris Microwave Semiconductor in six to nine months. The first products will include a 4-bit universal shift register, a divide by 2/4/8 divider, and various SSI logic chips. Clock rates will be in the range from 1.5 to 4 GHz. Harris is initially targeting the parts for signal processing applications.

Appeals court rules in favor of Apple for software protection

The Third Circuit U.S. Court of Appeals in Philadelphia has reversed a lower court decision made last year that denied a motion for a preliminary injunction brought by Apple Computer against Franklin Computer. Apple's programs for the Apple II personal computer—particularly those stored in the computer's ROM components and operating systems—are now ruled to be subject to copyright protection. This reverses an Aug 2, 1982 lower court ruling that the copyright law was unclear as to its application toward the code used for the computer's operating system. The case is now remanded to the district court for further proceedings.

Franklin Computer, however, claims that it anticipates only a "negligible" effect on its business as a result of the ruling. The company's chairman said that "the only immediate effect of the decision is to require the district judge to hold further hearings on the issue [and that] we think we have an ample basis to prevent issuance of an injunction, even under the appellate court's view of the scope of copyright protection afforded to computer operating systems, which we consider to be both novel and expansive."

Sub-4″ Winchester disk dimension defined

Ten disk drive and media manufacturers have agreed that rigid disks to be used in sub-4″ Winchester disk drives will have an outside diameter of 95 mm (3.74″) and an inside diameter of 25 mm (0.98″). The disks will be 1.27 mm (0.050″) thick. Specifications on magnetic characteristics or areal densities of these disks have not been prepared. Drive manufacturers Seagate and MiniScribe, and media vendors Charlton Associates, Dysan, KSI Disk Products, Nashua Corp, and Poly Disc Systems supported the standards, as did Applied Information Memories, which supplies both drives and media.

Joint ventures, mergers, and second-source agreements

Texas Instruments has acquired a 25% equity position in Lisp Machine, a manufacturer of computers for use in artificial intelligence applications, including expert systems. Lisp Machine will support TI in the development of advanced hardware and software for Lisp-based systems.

The Shen Zhen provincial government of the People's Republic of China has approved a joint venture agreement between Bishop Graphics and three other firms to manufacture and distribute a wide range of proprietary printed circuit design products. The agreement, scheduled to run 10 years, involves the Shen Zhen Electric Appliances Manufacturing Co of China, the Shen Zhen branch of The Bank of China, and Thai-An Trading Corp of Hong Kong. The operation will be located in a special economic zone established by the People's Republic of China in its Shen Zhen province.

Three major European computer companies—Compagnie Machines Bull (formerly Cii Honeywell Bull), ICL, and Siemens—have signed a memorandum of understanding to form a research institute that will undertake precompetitive research into selected areas of information processing in the common interest of the three companies. All research will belong to the three companies and will be freely available to them. Research areas will be centered on knowledge processing.

UP FRONT

Pretriggers

A tool for analyzing and simulating traffic on LANs is reportedly on its way from Excelan. The standalone Multibus-based workstation will ease the job of network developers by letting them locate bugs and characterize the system at heavy traffic loads.

Pitting a batch of Q-bus products head on against competition, Digital Equipment Corp has produced a board-level microcomputer with PDP-11/70 performance and has upgraded the single-board Falcon to a Falcon-Plus.

A plug-in color graphics board set for the Symbolics 3600 Lisp-based processor puts image memory into the CPU's physical address space. This eliminates bottlenecks to provide faster access time and supplies realtime image update capability.

By taking disk caching techniques developed for mainframes down to the minicomputer level, Gould/SEL has reduced access time of a moving head disk to 1 ms.

Direct sensor connection capability and a measurement and control oriented, extended Basic language enable Analog Devices' μMAC-5000 to meet distributed intelligence or local frontend applications. The standalone, single-board system can be used with user-defined keywords for custom applications to protect proprietary software.

A 256K DRAM with 32K x 8 architecture, said to be a "first" on the market, has been announced by Mostek. The chip is specifically designed for small microprocessor-based systems that do not require large amounts of solid state memory.

A 32-bit virtual memory workstation with integrated floating point processor and array processor, also said to be a market "first," Masscomp's 500 supports two 19″ raster displays. It executes a multi-user/multitasking Unix operating system featuring the company's RTU software enhancements.

An engineering workstation that speeds up design, development, and integration of software for 8- and 16-bit microcomputer systems will be introduced by Gould Design and Test Systems Div at Wescon in November. Both Motorola's 68000 and Intel's 8086 can be used in design systems.

A 64-bit multiple processor computer system by Elxsi allows up to ten 4-MIPS CPUs to be placed on a high speed bus at one time. Intelligent I/O and memory modules permit a system configuration with up to 192M bytes of physical memory and 4G-byte virtual memory for each user process. A message-based operating system balances throughput load and allows up to 40-MIPS operation.

The highest performance from a single processor is claimed by Harris Computer Systems Div for its model 1000, an ECL-based superminicomputer with 4-MIPS Whetstone performance.

Claimed to be the first rigid disk controller for the IBM PC and look-alikes that can support the SMD interface, the Maverick SMD PC-80 has been developed by Interphase. It can accommodate 8″ or larger disks with fixed and/or removable cartridges without software or hardware modifications.

COMPUTER DESIGN (ISSN-0010-4566) is published monthly, with a thirteenth and fourteenth issue respectively in April and October by PennWell Publishing Company, Advanced Technology Group, 119 Russell Street, Littleton, MA 01460. Second-class postage paid at Littleton, MA 01460 and additional mailing offices. COMPUTER DESIGN is distributed without charge to U.S. and W. Europe-based engineers and engineering managers responsible for computer-based equipment and systems design. Subscription rate for others is $50 in U.S.A. and $75 elsewhere. Single copy price is $5.00 in U.S.A. and $7.50 elsewhere. Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Road, Ann Arbor, Michigan 48106. POSTMASTER: CHANGE OF ADDRESS-FORM 3579 to be sent to COMPUTER DESIGN, Circulation Department, P.O. Box 593, Littleton, MA 01460 (USPS 127-340).

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CIRCLE 4

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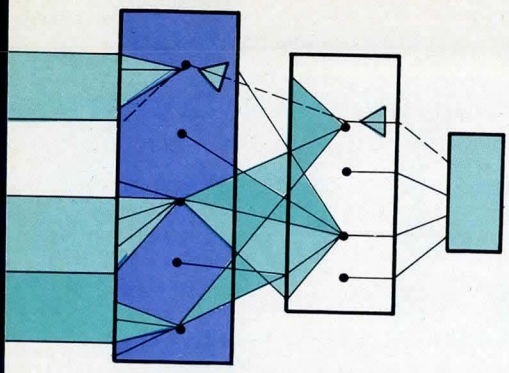
System technology



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36 **Development systems:** Software tools automate circuit designs

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53 **Computers:** Computer control store swapped for speed

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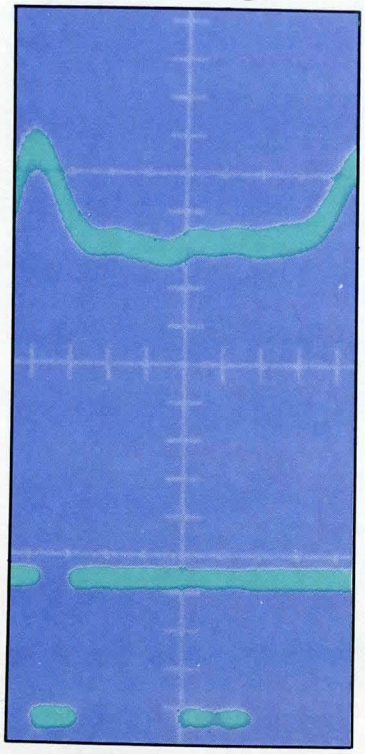
60 **Data communications:** Networking hardware and software connect unlike systems

66 **Software:** Piggybacked operating systems add flexibility

System design



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107 Peripherals: **Improving mass storage data integrity**
by Max Roth—Designers can do a lot to improve the reliability of the data being read from Winchester disks and other mass storage media. In fact, they should be doing more.

117 Interface: **Getting the best of both buses**
by Roger R. Russ—Building an interface that links the potent VERSAbus to the popular Unibus forces designers to consider trade-offs carefully.

125 Computers: **Designing a parallel Simula machine**
by Mike P. Papazoglou, Panayiotis I. Georgiadis, and Dimitris G. Maritsas—Modeling hardware architecture along the lines of the Simula software language allows designers to exploit the advantages of parallel instruction execution.

141 Software: **Single-chip micro speaks Forth**
by Gerald E. Bernier—An extended Forth interpreter embedded in read only memory brings high level language efficiency to microcomputer application programming.

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by Po Chen—The numerous trade-offs between various switching approaches point to a hybrid solution as optimum.

161 Software: **Constructing benchmarks that measure up**
by Jeffrey Pulcini—There is more to gauging hardware performance than tallying the number of instructions executed in a second. Instruction mixes, formats, and compilation methods all skew performance.

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74 **Wescon and Mini/Micro West**

93 **IECON '83**

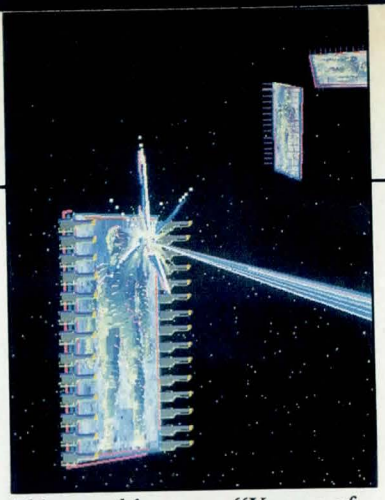
99 **AUTOFACT 5**

Four separate conferences in two cities will make for a jam-packed second week of November. Teaming up in San Francisco next month, Wescon, Mini/Micro West, and IECON participants will investigate a diverse range of interests spanning from electronic components and packaging to architecture and industrial application of small computers. At the same time, computer integrated manufacturing will be examined at AUTOFACT 5 in Detroit.

Vol 22, No 11
Oct 1983

Special report on microprocessors/microcomputers

173 In the past year, several trends have appeared in the microprocessor world. Greater speed, lower prices, and CMOS have dominated among manufacturers. The use of VLSI design has put more functions onchip and opened the door to 32-bit devices. Coprocessors have been developed to offload numerical and memory management tasks. Advanced microcontrollers based on 16-bit architectures have been introduced. In addition, microprogramming is becoming a tool for design engineers, not just for microprocessor architects.



This month's cover, "Voyage of the Super Micro," was created by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

System components

249 Workstation connects 16/32-bit micro power to Unix and graphics
250 System plays dual role in control and development
251 Plotter draws up graphics for small-computer workstations
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257 Op amps display increased performance

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*Appearing in Domestic issues only

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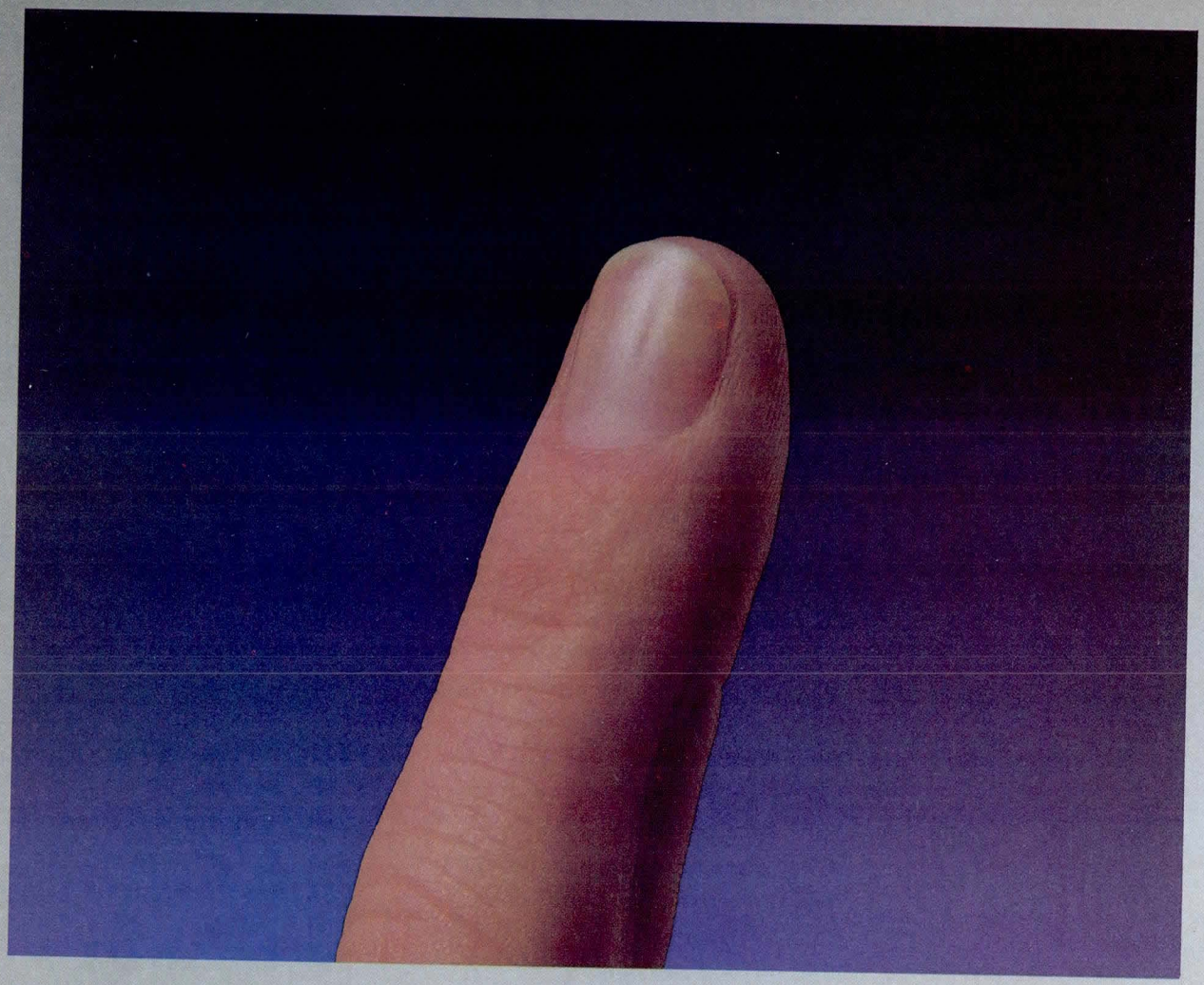

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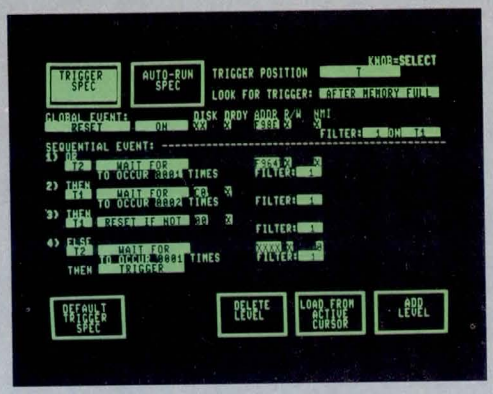

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CIRCLE 8

WA VERSUS THE GUNSLINGERS

Many American companies have examined Japanese management techniques in the hope of finding some magic formula that could help them compete more effectively in world markets. But, though some companies have successfully adopted the most superficial Japanese strategies such as the use of quality circles, the essence of Japanese management has proved elusive for Americans. Deep-rooted cultural differences make it difficult, and perhaps unwise, for American companies to run themselves the Japanese way.

Basically, there is a conflict between the Japanese goal of *wa* (usually translated as group harmony) and the Western ideal of rugged individual leadership. Somehow, it is difficult to imagine the gunslinging entrepreneurs of Silicon Valley functioning as cogs in a smoothly running Japanese management machine. And judging from the growth of the Silicon Valley startups, the macho style of many Western managers looks just as effective as the more nurturing and supportive Japanese style.

Perhaps there is room in the computer industry for both management styles, or for a new philosophy that draws on the strengths of each culture. The Japanese approach has already proved its worth in manufacturing and quality control—notably in the automotive industry. On the other hand, the Western approach seems quite effective in research and development—especially in the sort of rapid product development required for competitive high technology markets.

When creativity needs to be maximized and accelerated, peer recognition seems to be a powerful motivator. A dramatic example of how the need for individual recognition can be a driving force occurred when several video game designers left Atari to start Activision because they had not received credit for their "authorship" at Atari. Now those game designers enjoy the same sort of celebrity status as rock musicians and movie actors. Also, several studies have shown that the creativity of a group is rarely greater than that of the most creative individual in the group.

Of course, many successful American companies—like Japanese companies—emphasize group achievement rather than individual achievement. But they tend to be large companies such as IBM, Hewlett-Packard, and Digital Equipment. So perhaps the Japanese approach works best for large organizations, whereas the Western approach fosters entrepreneurship.

In any event, the coming struggle for economic and technical supremacy between Japan and the United States is shaping up as a shootout between the competing management styles of *wa* and the gunslingers. But just as the two countries have continually borrowed technical ideas from each other, they may also be smart enough to adopt those management ideas that work best within their changing cultures. (For those engineers who would like to learn more about this subject, we recommend *The Art of Japanese Management* by Richard Tanner Pascale and Anthony G. Athos, published by Warner Books.)

Michael Elphick

Michael Elphick
Editor in Chief

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Check the chart.

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	IMS2620-12	120ns	190ns
	IMS2620-15	150ns	240ns
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	IMS2600-12	120ns	190ns
	IMS2600-15	150ns	230ns

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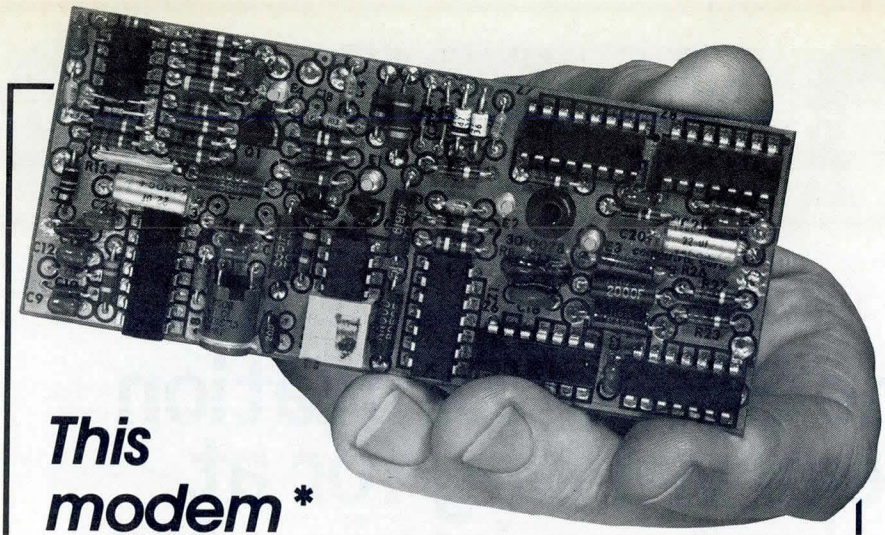

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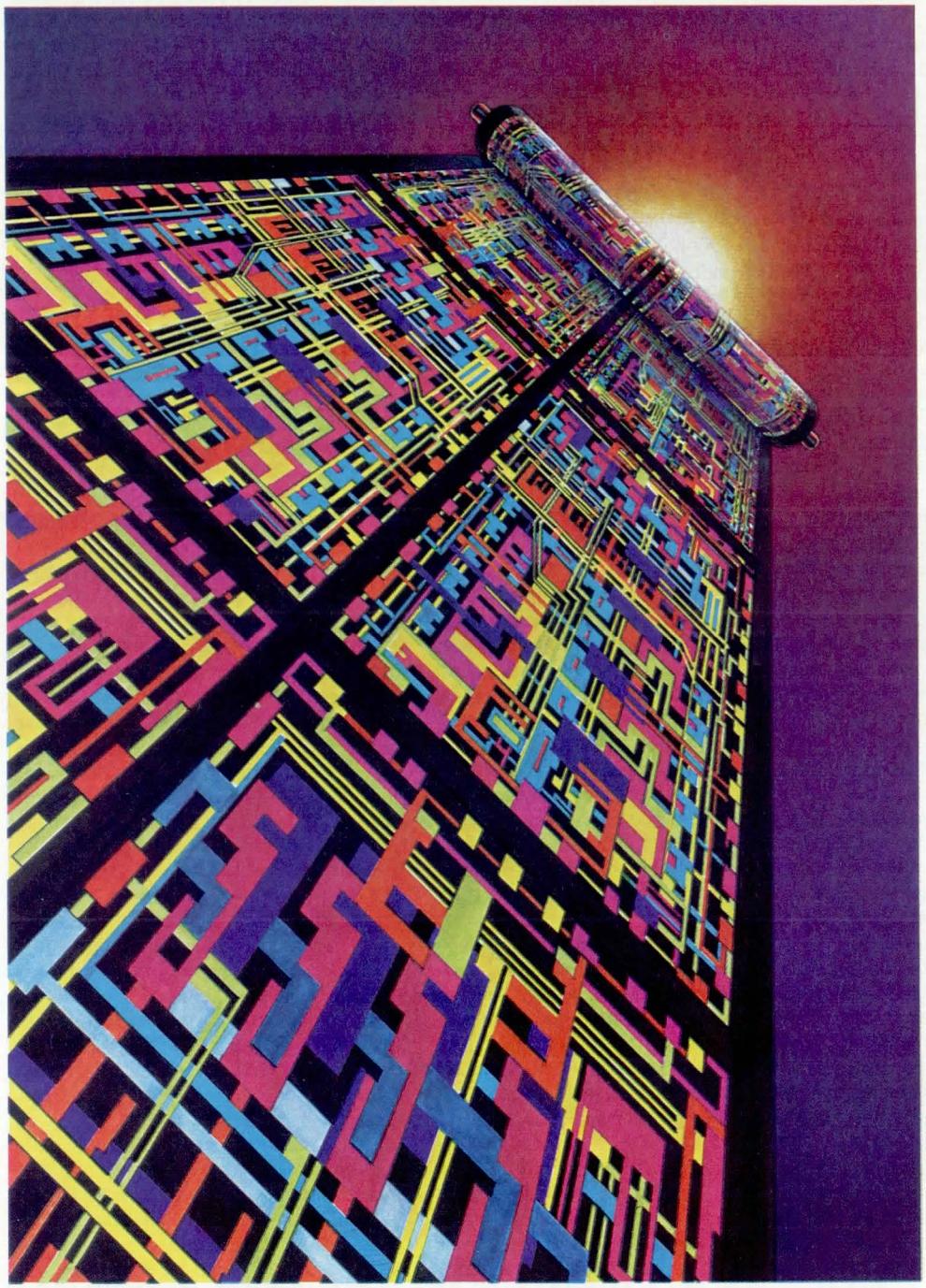

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Fortunately, there is a way to get a chip that's perfectly suited to your needs without paying for a full custom effort. The Ferranti ULA*.

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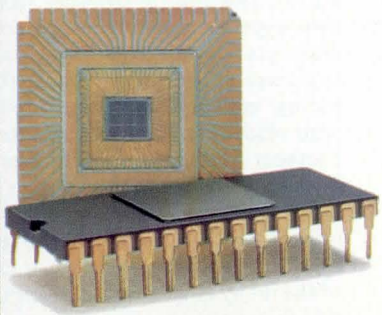
Ferranti Semiconductors.



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*ULA is the Ferranti brand name for uncommitted logic arrays and is a trademark of Ferranti plc.

CIRCLE 12

CAE should focus on user needs

The May 1983 editorial solicited input from readers on the qualities they would like to see in a workstation, so as to enhance their abilities as creative engineers.

At Exxon Research and Engineering, we have been anticipating vendor-provided engineering workstations for the past three years, and have done some prototype development to better understand the potential and limitations of this new approach to computer-aided engineering and research. Management is strongly committed to a program that would provide our engineers, scientists, administrators, and support personnel with powerful workstations through an implementation program spanning 1985 to 1990. Individual workstations will be purchased when the productivity and effectiveness justify their cost. Communication among workstations and to central computers is an essential part of the concept.

The editorial illustrates some of the pitfalls we have seen in the evolution of the area. One is the tendency for manufacturers to focus first on hardware, then on applications, and only then on determining what users need. This may be due to the fact that the engineers involved in developing the product can draw upon their own experience to hypothesize needs.

But not all engineers and scientists are computer engineers and scientists, and not all research and engineering organizations carry out their activities the way computer companies do. Hence, there is a great risk that in drawing from their own experience about needs, computer designers will fail to satisfy the needs of engineers and scientists outside the computing industry. Soliciting input from your readership is not much better, since I suspect your readership consists largely of people involved in the design aspects of computer engineering and science, rather than users and those who represent users. There is a real danger that the needs of the many engineers and scientists outside the computing field will not be well served by the readers who, in their computer design activities, are guided by published responses to your solicitation.

This is of particular concern with respect to applications software and ease of use. The best application software stems from an understanding of the application domain as much as it does from ability in software development. Tools must be made available for engineers and scientists with limited computer experience to develop applications that make effective use of the new equipment without requiring inordinate development time or the mastering of arcane new skills.

After all, these engineers and scientists should be concentrating on their specialties, and the computing aspects should be an aid and not an impediment to doing so. As for ease of use, it would be a mistake to assume that people with technical backgrounds need any less friendly and integrated systems than people in finance or management.

In short, the engineering and scientific workstation should provide both technical and general tools. It should be as easy to use as possible, its capabilities should reflect engineering and scientific needs beyond those of the computing field, and it should permit easy application development by technical specialists.

Mark J. Eisner
Exxon Research and Engineering Co
PO Box 101
Florham Park, NJ 07932

Need for custom CAE software

In response to the editorial request in May 1983, I submit the following comments, based on experience as a computer systems engineer involved in creation and evaluation of CAD and CAE programs.

The engineers I worked with were interested in 3-dimensional views of objects, mass properties of the objects, and ability to define the objects for finite element analysis for thermal and stress analysis. They wanted the ability to combine objects into assemblies that could also be analyzed. Some wished to simulate operation of mechanisms.

Not all engineers want the same things. There was general agreement that programs or software should be user oriented (ie, should guide the user through the program's operation. Quick response was also important. Many engineers refused to use timesharing computers when waiting time became excessive.

These needs or desires require programs to be rather "wordy" to guide the user. Also, most people underestimate memory and disk storage needed for these program types.

Computers with very large memories have become available in the past few years that can do the job for CAE if suitable software is available. Much research has been done in the software area and many good programs are available. Some of the results are spectacular. Engineers will find that no programs are available for many activities, and many programs will handle only problems of a very limited scope. Software development can be accelerated if engineers will define activities that need computer assistance.

To a degree, I agree with your comments on word processing and spreadsheets. However, professional engineers generally must document their work. A convenient word processing program can be a valuable aid in the documentation process. Many such programs are very difficult to use when use is intermittent.

Lee Toliver
206 Howell
Belen, NM 87008

CAE is nothing new

In response to your editorial (May 1983) soliciting comments on CAE, I've been doing CAE work for 27 years and I've never had a computer terminal. I don't need one except for a hand-held programmable calculator that has replaced my slide rule and handbook tables.

Putting a computer terminal on my desk does not make me more creative. I'm already creative, but modern calculators and computers have made me significantly more productive. I frequently solve problems today which were not feasible to calculate a few years ago. As a creative engineer, I do not necessarily want to be programming a computer. What is more useful to me is an assistant who programs engineering problems under my direction. This leaves me free to do creative engineering and interpretation.

Too often computer programmers who are not cognizant of engineering principles are being employed as engineers. For this reason, they incorrectly formulate problems and produce incorrect results.

Much of what is put into computers today is inept and unnecessary, making what comes out incorrect and subject to misinterpretation. Furthermore, it appears the present faddishness and clamor for computers is going to perpetuate these inanities.

I wish to point out, then, that CAE is not some new invention. It is an ongoing process and has been since the invention of counting machines. All that is happening is that the computers have become more complex, do faster and more advanced calculations, and thereby allow the engineer to better design and analyze more complicated technical problems.

Dale L. Jensen
PO Box 1183
Downey, CA 90240

LETTERS TO THE EDITOR

(continued on page 22)

The World's Most Elegant Microprocessor Family

is Banishing Current Benchmarks to Computer History.

Be advised: the NS16000 family is establishing all new benchmarks for 8-, 16-, and 32-bit microprocessors.

Here is proof beyond doubt that any NS16000-based product will outperform any other microprocessor-based product.

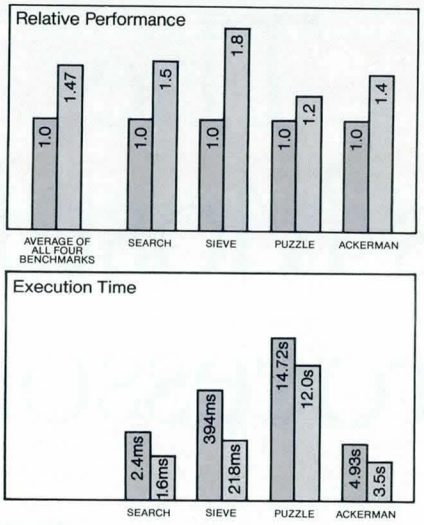
Of course, comparing the NS16000 family and the microprocessors your competition is banking on is difficult—perhaps even irrelevant—because the NS16000 family is, fundamentally, much more advanced.

No other commercial processor (micro, mini *or* mainframe) is designed to fully support the use of high-level languages. All members of the NS16000 family of CPUs,[1] however, feature not only 32-bit internal architecture, but also a high degree of regularity in the arrangement and use of their 32-bit registers. Data can be read or written 1, 8, 16, or 32 bits at a time, as sophisticated programs require, and transfers from one register to another are not restricted.

Moreover, the symmetrical instruction set of the NS16000 CPUs includes over 100 genuine two-operand instruction types, but avoids special-case instructions that compilers cannot use. All instructions can be used with the addressing modes common to most microprocessors (register, immediate, absolute, and register relative), as well as with powerful HLL-oriented modes that only the NS16000 offers: top-of-stack, scaled indexing, memory relative, and external. And any operand length and any general-purpose register may be used with any mode.

The combination of these virtues makes it possible to write especially lean high-level language programs on NS16000-based systems. The simplicity with which a programmer can implement a compiler, for instance, is matched only by the compiler's increased speed of execution. In effect, the dream of being able to pack the enviable working environment and performance of a large computer into a microprocessor has become reality.

HIGH-LEVEL LANGUAGE COMPARISONS[2]



Putting large-computer performance into a microprocessor is further advanced through the implementation of the NS16000's Demand Paged Virtual Memory—a strategy equivalent to that used in such systems as the VAX-11 series and all present IBM mainframes.

With an architecture that supports uniform addressing, the NS16000 is the first commercial microprocessor able to feature Demand Paged Virtual Memory as a means of solving large-memory-management problems. As a result, an NS16000-based system, blessed with this completely flexible memory configuration, can maximize the use of its physical and virtual memory resources and achieve a level of performance heretofore unrealized.

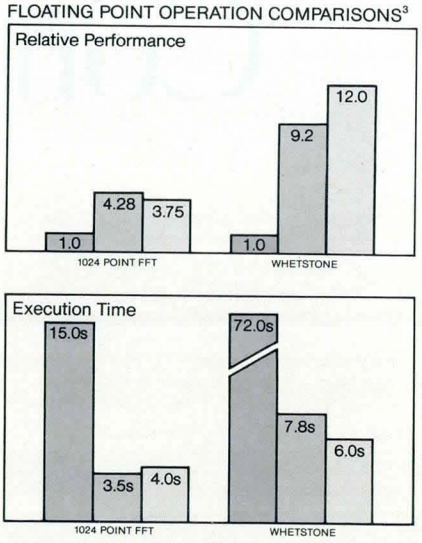
With the NS16082 Memory Management Unit (MMU), only the information most recently used is kept in RAM: other information is swapped in and out from mass storage, as needed. Consequently, each programmer, each program, each task has access to a uniform addressing space of 16 Mbytes simultaneously and independently, without reservation or special exception. (And more efficiently than on any other commercial processor—micro, mini, or mainframe.)

Among the reasons for the MMU's prowess is its support of a *two-level* page-table translation, whose process is speeded up by an associative on-chip cache. Utilizing a very fast Least-Recently-Used (LRU) algorithm and a powerful "referenced bit," the NS16082 MMU achieves a translation cache hit rate of over 98 percent.

The NS16081 Floating Point Unit (FPU) extends the NS16000 instruction set with very high-speed floating-point operations for both single- and double-precision IEEE operands.

Designing the FPU into a system allows programmers to treat floating-point numbers as they would any other data types, and to use any of the addressing modes to reference them. For example, the scaled index mode permits an array of floating-point data elements to be addressed by its logical index, rather than its physical address. The power this can add to a system makes it especially applicable for graphics and engineering work-stations.

FLOATING POINT OPERATION COMPARISONS[3]

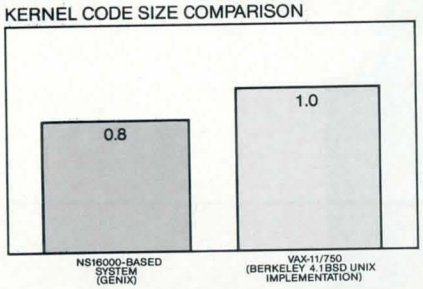


With the introduction of National's proprietary GENIX™ operating system, even the advantages of using UNIX® on a large computer have been ported to the NS16000 microprocessor family.

GENIX is an elegant implementation of the proven Berkeley 4.1 bsd version of UNIX. Created in-house, to facilitate the development of software for NS16000-based applications, it is the first UNIX operating system to support Demand Paged Virtual Memory in a microprocessor.

Here, then, is a demonstration not only of the pure functionality of the NS16000 family architecture, but of the large-computer-like results now possible on a microprocessor-based system using GENIX.

KERNEL CODE SIZE COMPARISON



When you consider applications for the NS16000 microprocessor family—from elegant personal and business computers, to graphics work-stations, to industrial control systems—keep in mind that:

1. The NS16032 CPU and the NS16201 TCU are in production now.
2. The NS16082 MMU, the NS16081 FPU, and the NS16202 ICU are being sampled now.
3. Evaluation tools are available now.
4. Development tools are available now.
5. Training classes are in progress now.
6. Third-party software for the family is available now and increasing daily.
7. The software you write now will work *without modification* if you move your product line from one NS16000 CPU to another in the future.

   Similarly, the optional use of the NS16000's MMU and FPU slave processors—integral parts of the NS16000 architecture—will allow you to determine price/performance trade-offs while preserving your initial software investment.
8. Only the NS16000 family can make it possible for you to put a large-computer-like product on the market today—at microprocessor prices.

Footnotes:

1. The NS16032 CPU, the first of the NS16000 CPUs, has a 16-bit-wide data path to memory and 32-bit internal architecture. Before the end of this year, CPUs implementing the same 32-bit internal architecture, but with 8- and 32-bit-wide data paths to memory will also be available, to allow maximum price/performance flexibility within your product line.

2. Results for the 68000 were taken from *Computer Architecture News*, Vol. 10, No. 4, June 1982, pp. 17-28. The 68000 was run at 10MHz, with no Wait States. Source programs in Pascal.

   Results for the NS16032 were obtained on a DB16000 at 10MHz, with no Wait States. Source programs in Pascal. All variable sizes are 32-bit.

3. Results for the 68000 were obtained on a SUN System at 10MHz, with no Wait States, using Motorola's ROM-based floating point subroutine package.

   Results for the NS16032, utilizing the NS16081 FPU, were obtained on a DB16000 at 10MHz, with no Wait States. IEEE floating point, variable sizes.

   Results for the VAX-11/750 were obtained without using floating point accelerator.

NS16000

Elegance is everything.

See it.

The NS16000 microprocessor family will be on exhibition at WESCON.

Talk with us.

Please call the National Sales Representative nearest you for more information, and the answers to your questions. Ask to meet with one of our Field Applications Engineers, too. Or, circle the number below.

Read about it.

You haven't heard the last word on the NS16000 microprocessor family yet. In the meantime, you may want to further your understanding of what we've accomplished by requesting copies of *NS16000: Demand Paged Virtual Memory* and *NS16000: Benchmarks*.

NS16000: Demand Paged Virtual Memory

NS16000: Benchmarks

VAX is a trademark of Digital Equipment Corporation.
UNIX is a registered trademark of Bell Laboratories.
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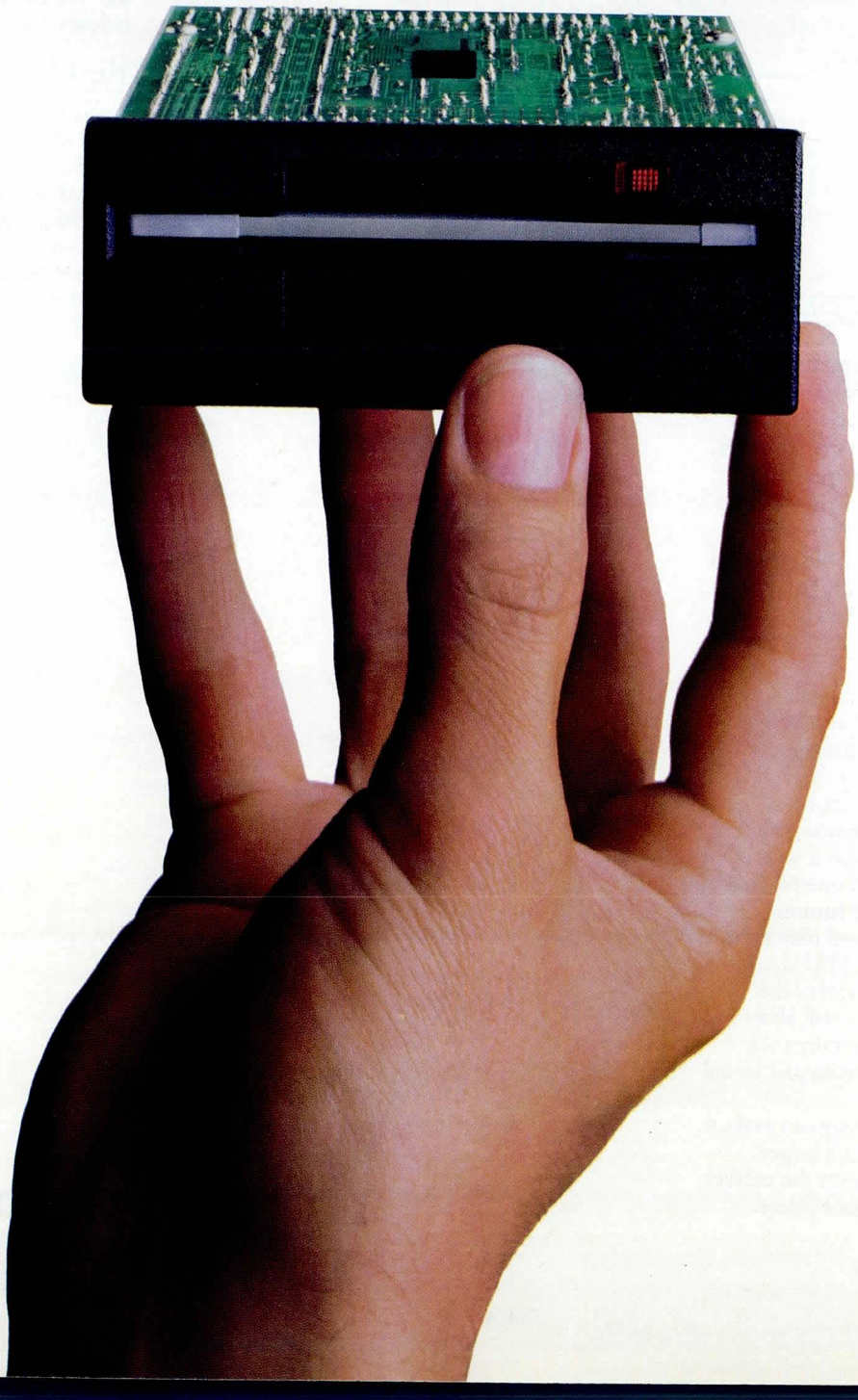
National Semiconductor

MICROCOMPUTER SYSTEMS DIVISION

CIRCLE 13

DO YOU HAVE THE DRIVE TO SUCCEED?



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It's also quite an achievement. One that allows you to engineer a wealth of advantages into smaller, more competitive systems.

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Size. With the SA300 you can make your personal and home systems less imposing, more, well, personal. Our microfloppy takes up 75% less room than a standard sized Minifloppy.™

The 3.5" Micro-Cartridge provides maximum media protection.

And it weighs just a tad over a pound. So your portable system can be more, you guessed it, portable, even with two drives in it.

Yet the SA300 still delivers 500 Kbytes in the single-sided version (1 Mbyte in the double-sided version) and uses less power, worst case, than an 8-watt night-light.

It's also so quiet, you can't hear it running unless you put your ear right down on top of it.

And with an MTBF of over 10,000 power-on hours, it should run for quite some time.

Then, of course, there's the not-so-small matter of the industry standard 3.5" microfloppy diskette.

Which offers a few important advantages of its own.

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CIRCLE 14

(continued from page 16)

CAD and the user

In the May 1983 editorial, I noted your request for comments on computer workstations. I regularly use three pieces of computer-aided design equipment: a desktop computer running packaged design analysis software and my own programs, a printed circuit board design computer, and a microprocessor software and hardware development station.

In all cases, my work involves entering a fair amount of data in a text format. These units are shared with five or six colleagues. As work must be saved for later use, each unit has a tape unit for this. The microprocessor development station (MDS) also has disk-based storage.

The tapes for each are identical, but tapes can only be read on the unit that wrote them. The formats are all different. While this is acceptable for program files, it is sad that text files cannot be transferred. Often one terminal is free and I could at least get my data in. The three units are an HP 85 desktop, an HP 64000 MDS and a Racal Cadet PC board designer. The latter uses an HP 1000 series terminal! If Hewlett-Packard cannot make three products that use identical tape transports with the same format, what hope is there for the rest of industry?

This leads me to another point that I think is very important. It is unlikely that a universal workstation will be produced that is cheap enough for most companies to give one to each of their designers. Terminals on a central system may be one answer, but here again, the initial cost is high.

I feel that there is a strong case for a modular approach; a set of units that stands alone or that can be integrated to provide an adaptable workstation. It is important that the module cost and the initial entry fee, in terms of hardware and software, be low enough for even the smaller firms to buy. It is in this area where improvements in productivity can have the greatest impact in terms of company performance. This in turn leads to increased employment. In larger firms, the converse tends to be true. The machines are seen as a means to reduce expensive labor.

Gordon M. Message
92 Harrow Rd
Leighton Buzzard
Bedfordshire
LU7 8UQ
England

Pirates ahoy

This is in reference to Chris Brown's article, "Setting Sail against the Software Pirates" (June 1983, p 30). Here at LJM, we are both end users and software manufacturers in the microcomputing industry who vigorously uphold the rights of software authors, and abhor software piracy.

We contend, however, that software manufacturers (especially in the microcomputing industry) encourage software piracy with artificially high software prices. Of course, the author is entitled to make a living, but by selling a product for more than the consumer thinks it is worth, manufacturers help justify the act of software piracy.

In our efforts to produce quality software, we maintain a pricing policy that enables us to survive comfortably, while discouraging piracy. After all, a pirate cannot obtain service from a manufacturer or manufacturer's representative when a problem occurs. It is the manufacturer's responsibility and duty to put the pirates out of business, not by legal remedies, but in the marketplace through intelligent pricing policies.

Lewis J. Metzger
LJM Computer Consulting
96 Orchard St
Garfield, NJ 07026

Economic reality

With floppy disks selling for $1 each, how low are you willing to go?

Chris Brown
Technical Editor

A bit of an error

This is just a note to call attention to a typo in Gary Martin's article, "Virtual Memory Management Expands Microprocessors" (June 1983, p 169), that was generated by this office for National Semiconductor. No doubt, others have commented on it already. As editor and writer for *IEEE Spectrum* for many years, I know the feeling and the futility it sometimes brings.

The error appeared on the second line of the subtitle. It should have read "24-bit" rather than "124-bit" virtual address space. A startled reader should have recovered by the time the last paragraph on the page (where it is referenced correctly) was reached, anyway.

Thank you for the coverage of this vital development in the microprocessor art.

Marce Eleccion
Paul Purdom & Co
1845 Magnolia Ave
Burlingame, CA 94010

Right model, wrong function

Many thanks for the mention of Metheus Corp products on p 156 of the July 1983 article, "Workstations That Take Chip Design from End to End." I must point out, however, that the Omega 400 is not a workstation "intelligent enough to handle an entire design problem from back to front."

The Omega 400 display controller is a complete graphics processor. It interfaces with a host computer and color video monitor, and provides a 1024- x 1024-pixel display, as well as the drawing speed and other features the article mentions.

The system that does "handle an entire design problem from back to front" is the Lambda 750 engineering workstation, which was described quite well in the following paragraph on p 156.

Bob Behrens
Metheus Corp
PO Box 1049
Hillsboro, OR 97123

Search for interfaces

I am looking for some companies that manufacture communication interfaces capable of emulating IBM controllers, the purpose being to hook non-IBM peripherals onto IBM mainframes at a competitive price. If you know of any reliable firms producing such items, would you please be so kind as to let me have their addresses, or pass my request on to them?

Renato Covi
Via Padova, 95
Milano
20127
Italy

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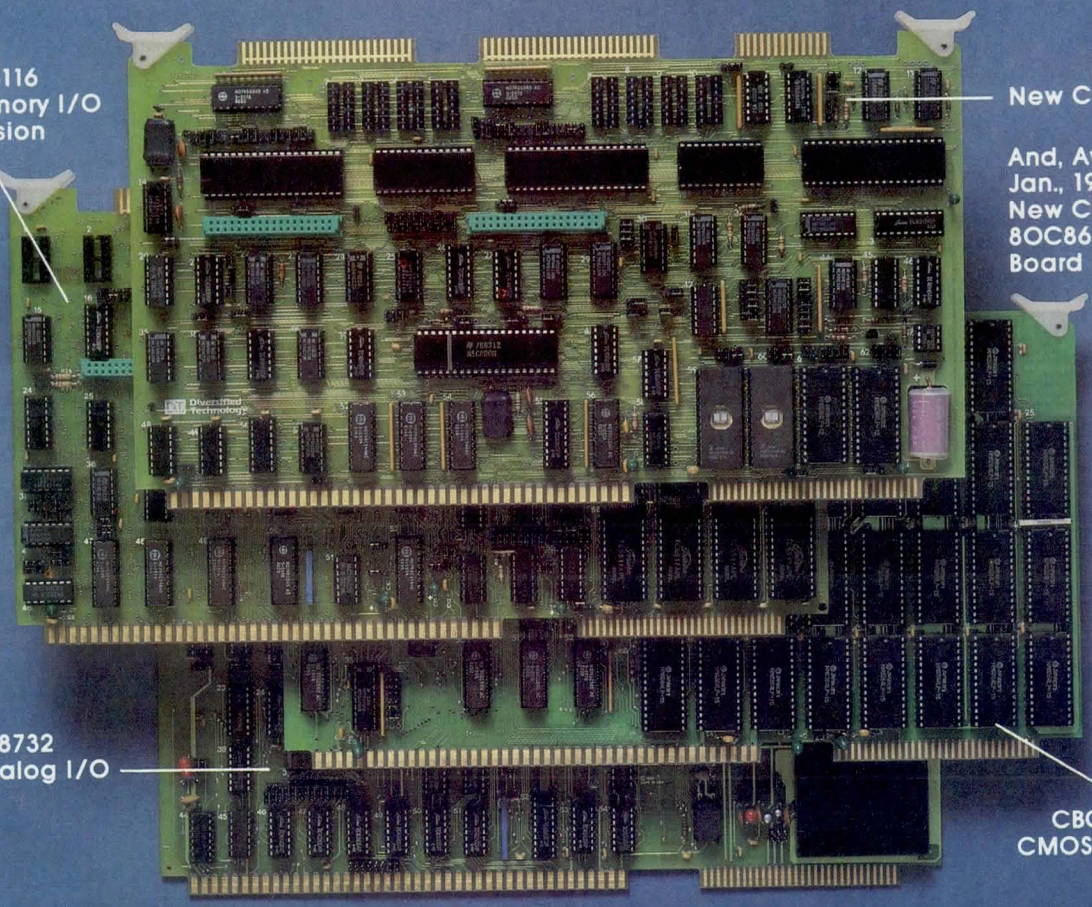

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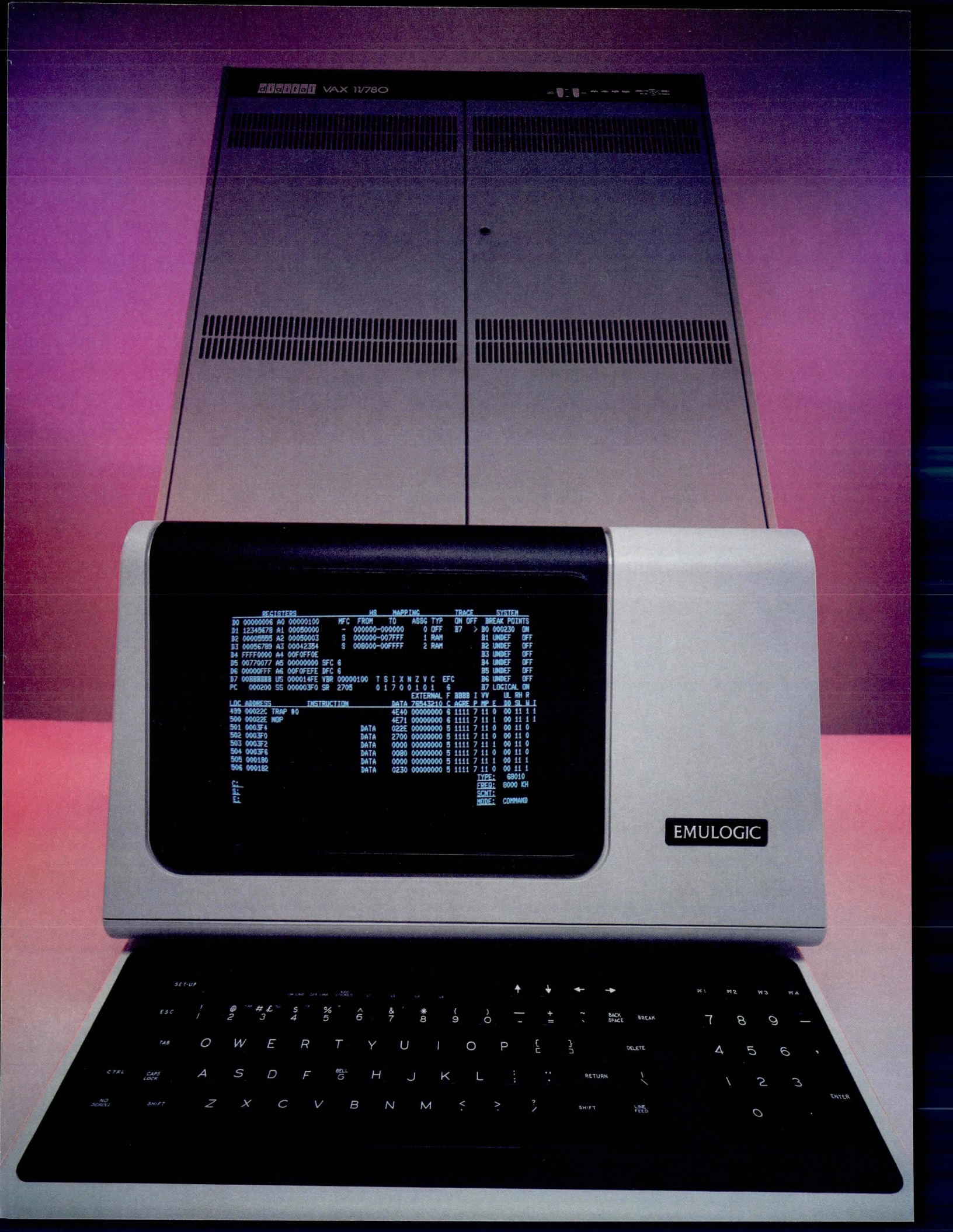
CIRCLE 15


VAX 11/780
REGISTERS
D0 00000006 A0 00000100
D1 12345678 A1 00050000
D2 00005555 A2 00050003
D3 00056789 A3 00042354
D4 FFFF0000 A4 00F0FF0E
D5 00770077 A5 00000000
D6 00000FFF A6 00F0FEFE
D7 00BBBBBB A7 000014FE
PC 000200 SS 000003F0
MAPPING
MFC FROM TO ASSG TYP
0 000000-000000 0 OFF
S 000000-007FFF 1 RAM
S 008000-00FFFF 2 RAM
TRACE
ON OFF
B7 >
SYSTEM
BREAK POINTS
B0 000230 ON
B1 UNDEF OFF
B2 UNDEF OFF
B3 UNDEF OFF
B4 UNDEF OFF
B5 UNDEF OFF
B6 UNDEF OFF
B7 LOGICAL ON
TYPE: 68010
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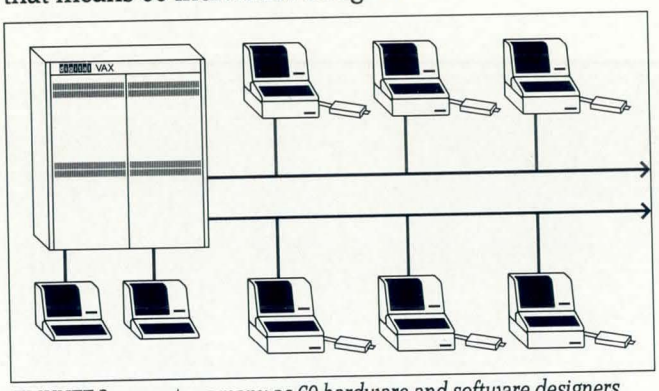

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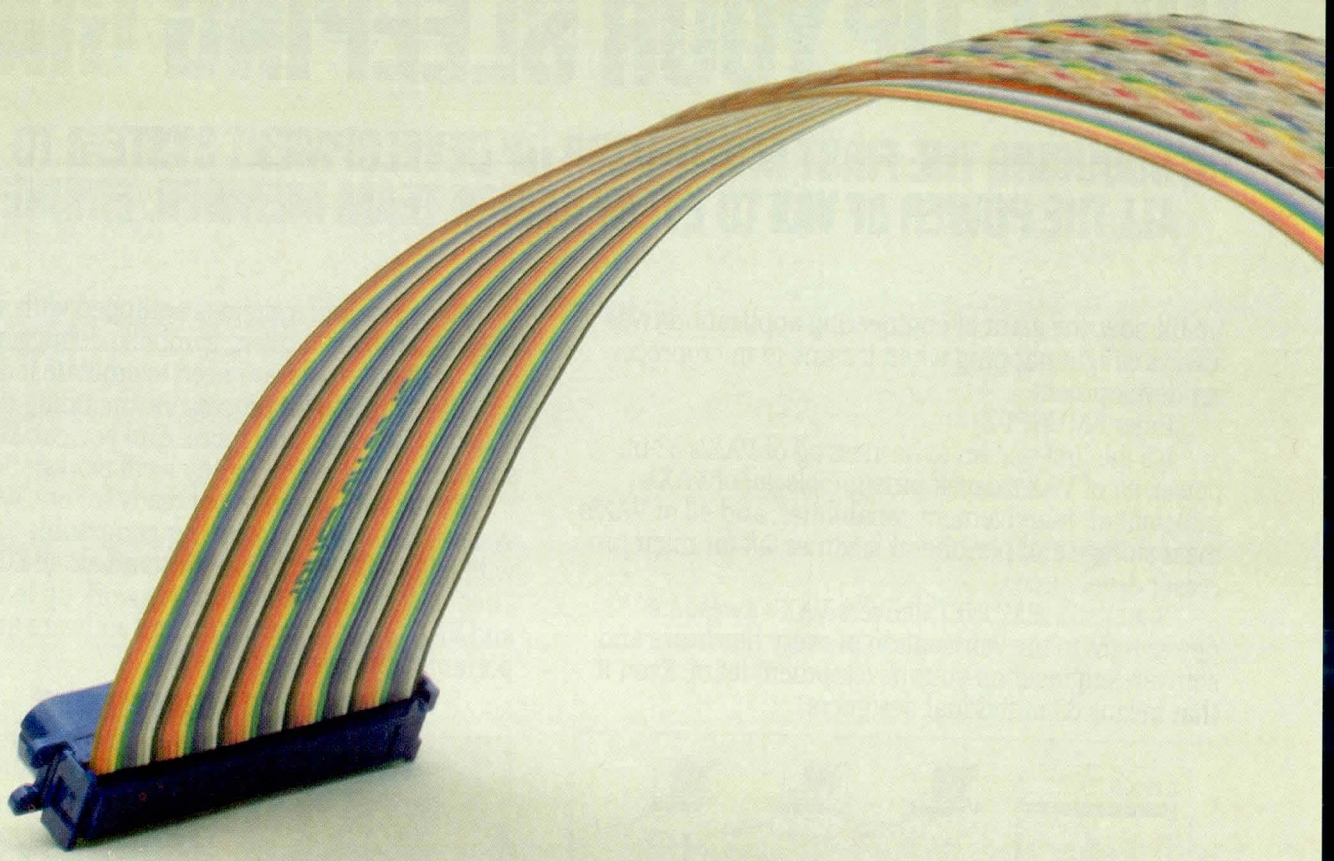
CIRCLE 16



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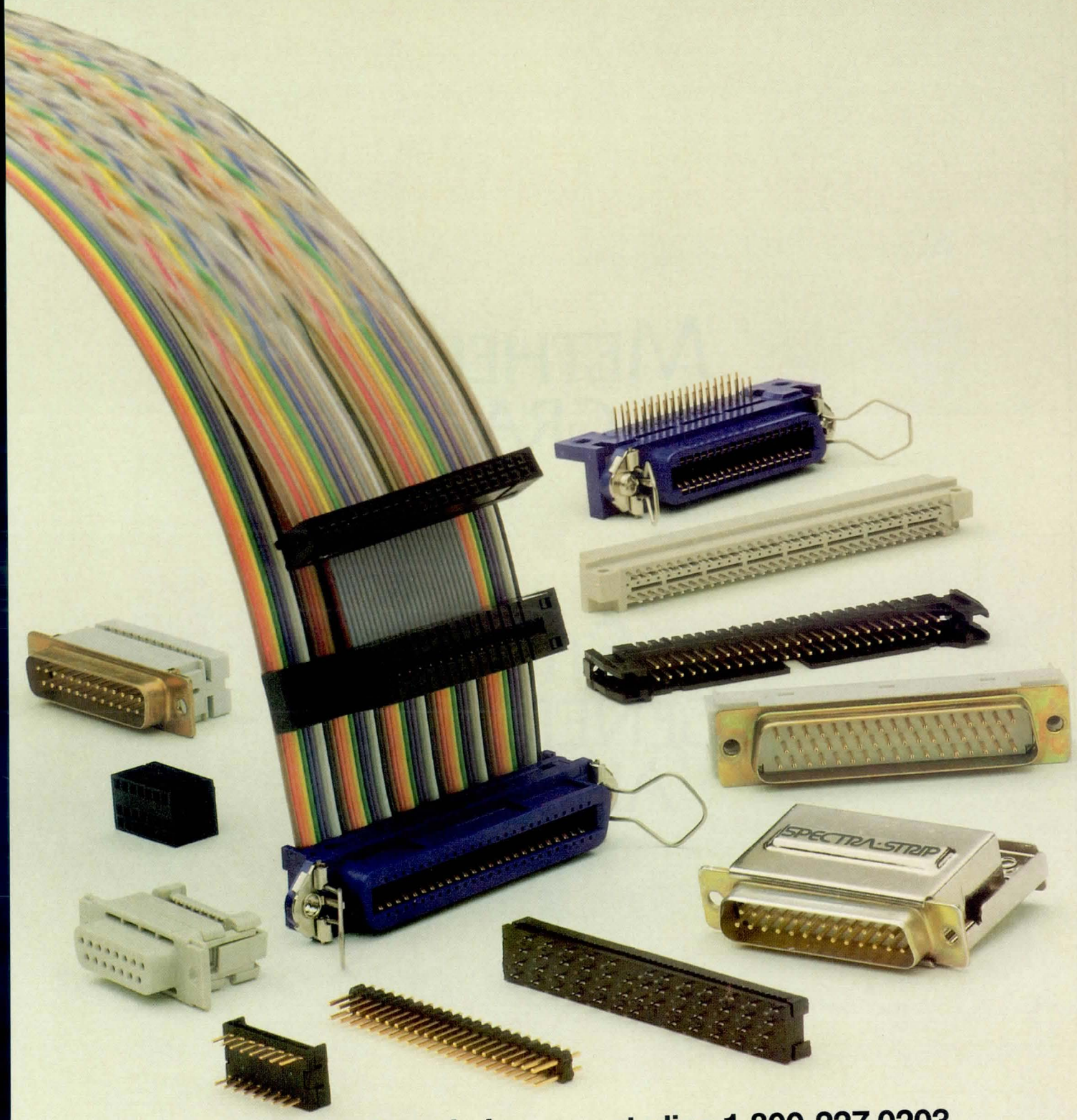

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CIRCLE 17

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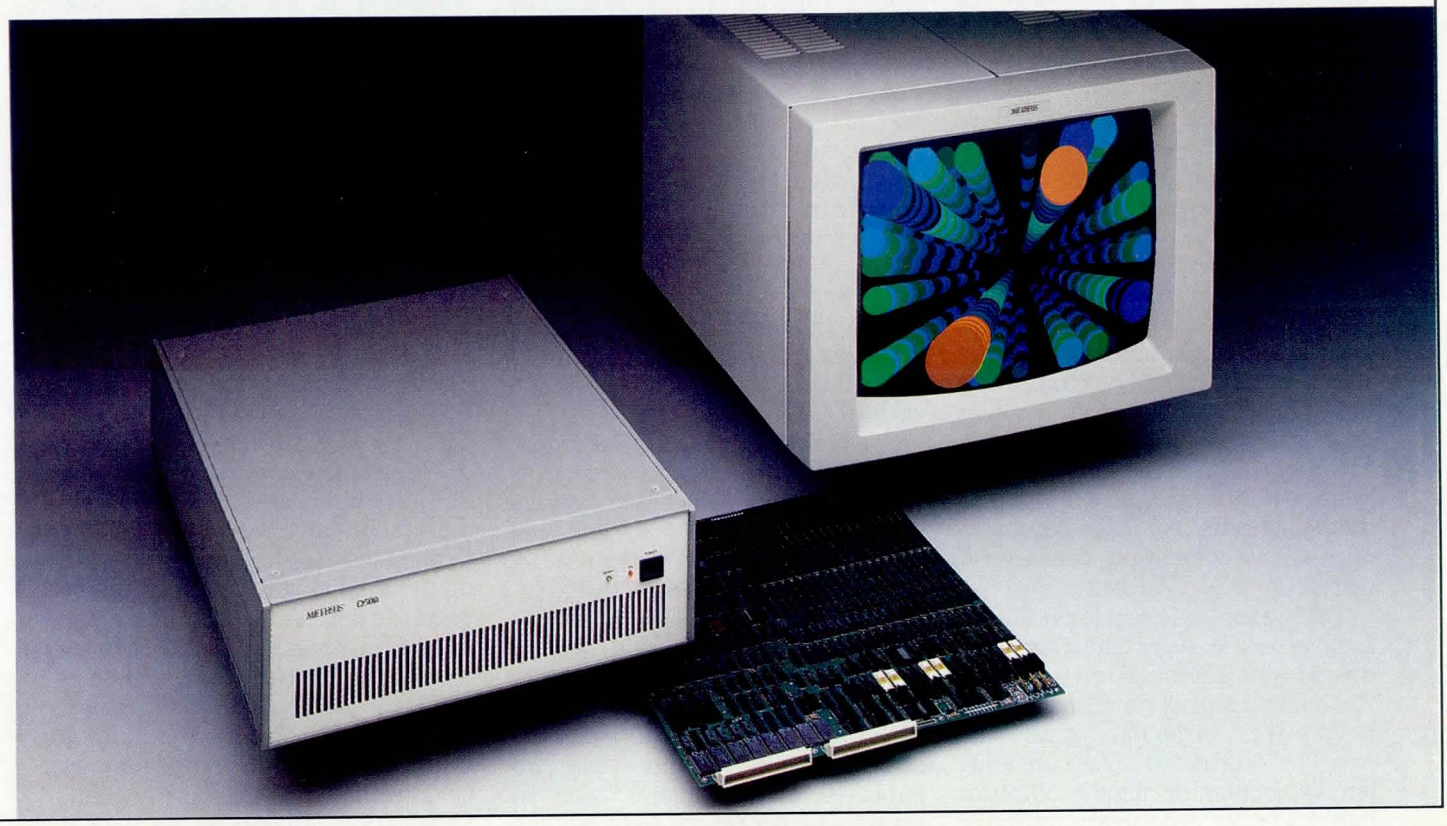
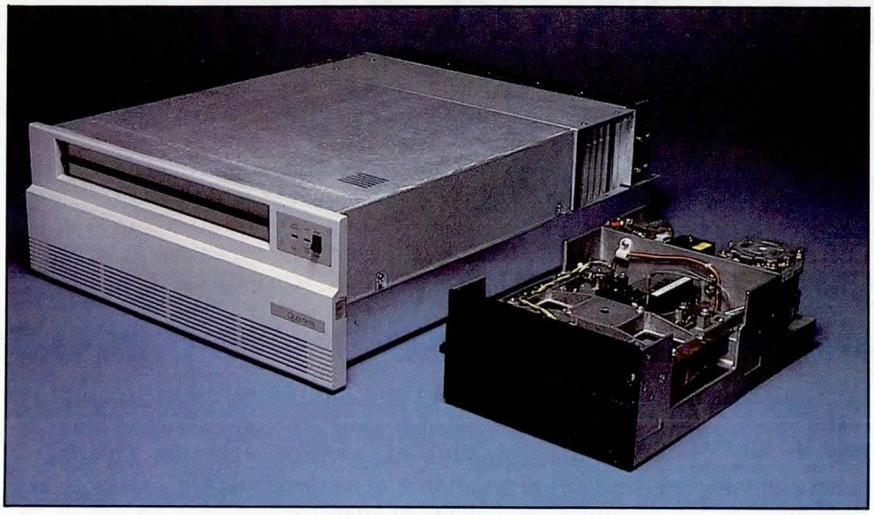


CIRCLE 18

High capacity optical disk system appears at last



Shugart Corp's Optimem 1000 laser-based optical disk drive is shown with an SA801 8″ floppy for size comparison.

Until recently, optical memory aimed at computer systems has been basically a laboratory project. But the Optimem 1000, a 1G-byte optical disk from the Optimem Division of Shugart Corp (formerly Shugart Associates), is about to appear for 1984 systems.

The Optimem 1000 produces a "write-once, read-often" disk—it cannot be erased and rewritten, since the laser permanently deforms the reflective material in the process of writing. This was viewed as a disadvantage when the technology was first investigated, but it is now seen as a way of creating archival computer records.

Magnetic records decay over time, and valuable data and imagery can be lost. However, the optical medium used in this system has a very long lifetime. Although no body of experience with the medium exists as yet, testing indicates that it should survive in readable condition for several decades.

The system uses a gallium aluminum arsenide semiconductor laser operating at a nominal wavelength of 830 nm and a peak power level of 15 to 20 mW, to write data on one side of a 12″ optical disk. Data are written as circular or slightly elliptical bubbles in the proprietary reflective disk surface developed by Thompson-CSF (Paris, France). Since the track width is, in effect, the width of a data bit, the bpi and tpi are equal at 14.5k. Reading is done with the same laser, but at much lower power (1 to 2 mW). Laser light is reflected from the data surface and detected by a photodetector. Lack of a signal, due to a dark area produced by a bubble in the surface, is interpreted as 1 bit.

Optical disks for the system are pregrooved and preformatted in a manner similar to that used for Laservision optical video disks and digital audio disks. Precision mastering allows Thompson-CSF to produce large quantities of disks with an areal density of 2×10^8 bpi^2, and to price them at approximately $100 each in OEM quantities.

A voice coil actuator similar to that used for magnetic disk drives controls the optical read/write head. Average access time is 150 ms, and the maximum data rate is 5M bps. A hardware board developed by Cyclotomics (Berkeley, Calif) handles error correction. As data are written to the disk, an additional 80 bytes of redundant data are added to each record. When each record is read back, the error-correcting circuitry uses an improved Reed-Solomon code to ensure an error rate of less than one error in 10^{12} bits read. The error-correcting circuit imposes a delay of two record times, which is approximately 217 μs at a nominal 5M-bps data rate.

Areas such as medical imaging (ie, X-rays, and CAT-scanning data), archival storage of accounting or security data, and distribution of large data bases are all likely system applications. In addition, "date stamping" individual records would enable the system to serve as a pseudoread/write disk—only the most recent copy of a file would be returned in response to a request for a given file name.

Similar systems to be announced

Several other companies are preparing to introduce similar optical disk systems in the near future, according to informed industry sources. For instance, Storage Technology Corp (Louisville, Colo) has announced that it will be shipping evaluation units this fall, with volume shipments in the spring of 1984. RCA's Government Systems Division (Moorestown, NJ) is also working on an optical memory unit, although when it will be introduced is not yet clear.

More directly competitive, Optical Peripherals Laboratory (Colorado Springs, Colo), a joint venture of Control Data Corp (Minneapolis, Minn) and Philips (Eindhoven, the Netherlands), is expected to introduce a 1G- to 5G-byte unit soon. NEC Electronics U.S.A., Inc (Santa Clara, Calif) showed a demonstration unit privately at NCC this year. Several other Japanese companies including Sony, Hitachi, and Matsushita will reportedly introduce units at the Osaka Business Show this month. All of these units will be aimed at the domestic market for graphic storage of Kanji (ideographic) text.

Another possible entrant is Thompson-CSF, the optical disk manufacturer that is expected to show a rotating optical memory unit at Comdex in Las Vegas next month. Shugart and Thompson do have a

(continued on page 32)

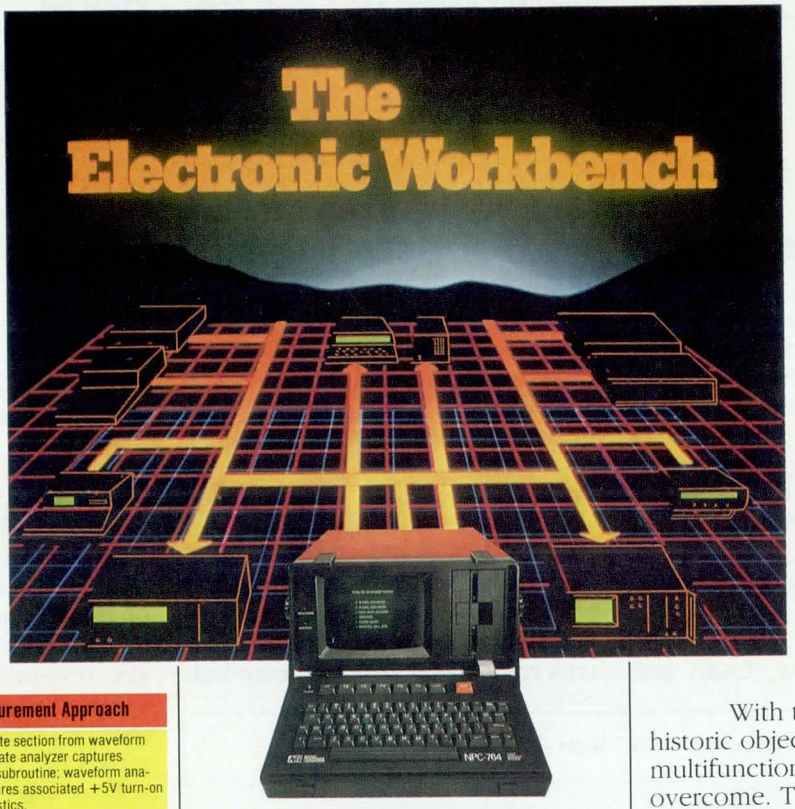
Designer Note #4

Focus on Cross-Domain Analysis: The Electronic Workbench!

Cross-domain analysis is a new test methodology that requires the combination of two or more distinct measurement functions to trace or quantify hardware and software interactions.

The table below describes some of the many analysis tasks that fall into the cross-domain category.

The need for cross-domain analysis has grown out of the increasing complexity of hardware and software functions. Although cross-domain analysis can be achieved by interconnecting individual instruments from different manufacturers—interfacing problems and operational complexities has made this approach impractical.



Analysis Task	Measurement Approach
1. Verify your system's power-up subroutine when +5V power is first applied.	Trigger state section from waveform section. State analyzer captures power-up subroutine; waveform analyzer captures associated +5V turn-on characteristics.
2. Monitor I/O hardware subsystem operation when I/O subroutine is executed.	Trigger timing section from state section. Timing analyzer captures I/O hand-shaking signals and data; state analyzer captures associated I/O subroutine.
3. Examine interrupt subsystem software execution.	Trigger state section from timing section. State analyzer captures interrupt subroutine; timing analyzer captures hardware interrupts.
4. Trace overall hardware/software interactions in a process controller product.	Trigger state section from timing section which in turn is triggered from waveform front-end. State analyzer captures process controller software; timing analyzer captures digitized transducer output when triggering by the analog input crossing a pre-set threshold.
5. Measure subroutine execution time.	Start counter-timer with subroutine entry address and stop it with exit address. Counter-timer's interval mode then reads execution time.

Because of this fact, a trend is developing towards the *Electronic Workbench*. An Electronic Workbench is defined as a multifunctional instrument system where all measurements are controlled through a single ASCII keyboard and all results are displayed on a single CRT. In its basic form, such an instrument system is typified by the NPC-748.

For more advanced tests and test automation, a floppy disk and an operating system are added as typified by the NPC-764.

The Electronic Workbench is not a new concept. Prior to the incorporation of the microprocessor into test equipment, the only advantage that early multifunctional instruments offered was compact packaging. For each test function, dedicated switches still had to be set, knobs still had to be rotated and readouts interpreted. There was no unified test methodology.

With the NPC-700 series, the historic objections that users had to multifunctional instruments were overcome. This was accomplished by using a single ASCII keyboard and CRT interface and a "start simple and build" test methodology that allows routine, independent measurements to be performed with little or no set-up. As increasingly complex measurements are needed, more powerful functions are accessed on an "as required" basis. For cross-domain analysis simple keystroke commands are used to link various internal analysis resources.

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CIRCLE 19

High capacity

(continued from page 30)

technology transfer agreement, but no agreements on joint marketing.

Prior to these announcements, Shugart was predicting the introduction of an optical disk unit in early 1984. The reason for the early introduction, and showing of sample drives at Comdex, may be the imminent appearance of the other manufacturers' units.

The Optimem 1000's dimensions are 7″ x 17.6″ x 24″ (18 x 44.7 x 61 cm), and it weighs approximately 50 lbs (23 kg). Price for the system is approximately $10,000 in unit quantities, and $6000 in quantities of 500, with appropriate OEM discounts. A Small Computer System Interface (SCSI) bus controller is in development, but pricing has not yet been determined. Evaluation units are scheduled for shipment in the first or second quarter of 1984, with volume shipments expected in the third or fourth quarter. **Shugart Corp, Optimem Div,** 475 Oakmead Pkwy, Sunnyvale, CA 94087.

—Sam Bassett, Field Editor

Circle 240

Vendors hedge on rigid disk interface specs

Fence-sitting remains a popular occupation for many vendors of 5¼″ Winchester disk drives and controllers as two announced interface proposals jockey for position to replace the ST506 interface in high capacity drives. The Enhanced Small Disk Interface (ESDI) and the American National Standards Institute (ANSI) BSR X3.101 are both being proposed as standards. ESDI supporters include Maxtor Corp (Santa Clara, Calif) and OMTI (Campbell, Calif), while Priam Corp (San Jose, Calif) and Xebec Corp (Sunnyvale, Calif) just as vehemently advocate the BSR X3.101 specification.

As yet, however, most drive and controller manufacturers remain uncommitted to either interface proposal. High volume manufacturers including Seagate Corp (Scotts Valley, Calif), Shugart Associates (Sunnyvale, Calif), and Tandon Corp (Chatsworth, Calif) have not participated in the debates concerning either interface. As a result of inertia contained within each proposal, it may be six months to a year before one interface emerges as an industry standard.

High Performance 5¼″ Rigid Disk Interfaces

Parameters	ANSI BSR X3.101	Enhanced Small Disk Interface	Modified ST506
Data transfer rate	10M bps	10M bps	8.2M bps
Cables	Single 50-pin	34 and 20 pins (ST506 compatible)	34 and 20 pins (ST506 compatible)
Data separator on drive	Yes	Yes	No
ST506-type protocol	No	Possible in step mode	Yes
Compatible with ST506 controllers and drives	No	No	No
Drive vendors	Priam	Disctron Memorex Maxtor MPI/CDC	Evotek Vertex
Controller vendors	Xebec DTC Interphase	OMTI DTC Emulex	OMTI DTC

Interface comparisons

Although the debates typically characterize distinctions, the ESDI and BSR X3.101 specifications have many similarities when implemented. Perhaps the most important common attribute is the data separator's placement on the drive rather than on the controller. Both interfaces also transmit data in a serial mode where the drive is told to go to a specified track and sector and begin read/write operations.

Cost was a major factor in the way that the older ST506 and its 8″ SA1100 predecessor were implemented. To keep the price of the initial ST506 drives down, the drive interface was kept as simple as possible, with the disk controller containing most of the intelligence.

Therefore, the controller must not only separate the clock and data signal from a multiplexed line, but generate step pulses as a means to step across individual tracks before read/write operations can occur. Although several vendors buffer step pulses to reduce seek times, the significant overhead involved in the stepper mode limits the ST506 interface's ability to handle higher disk capacities with fast access times.

In contrast, removing the clock signal from the data at the drive itself (as in the more expensive ESDI and BSR X3.101 interfaces) allows

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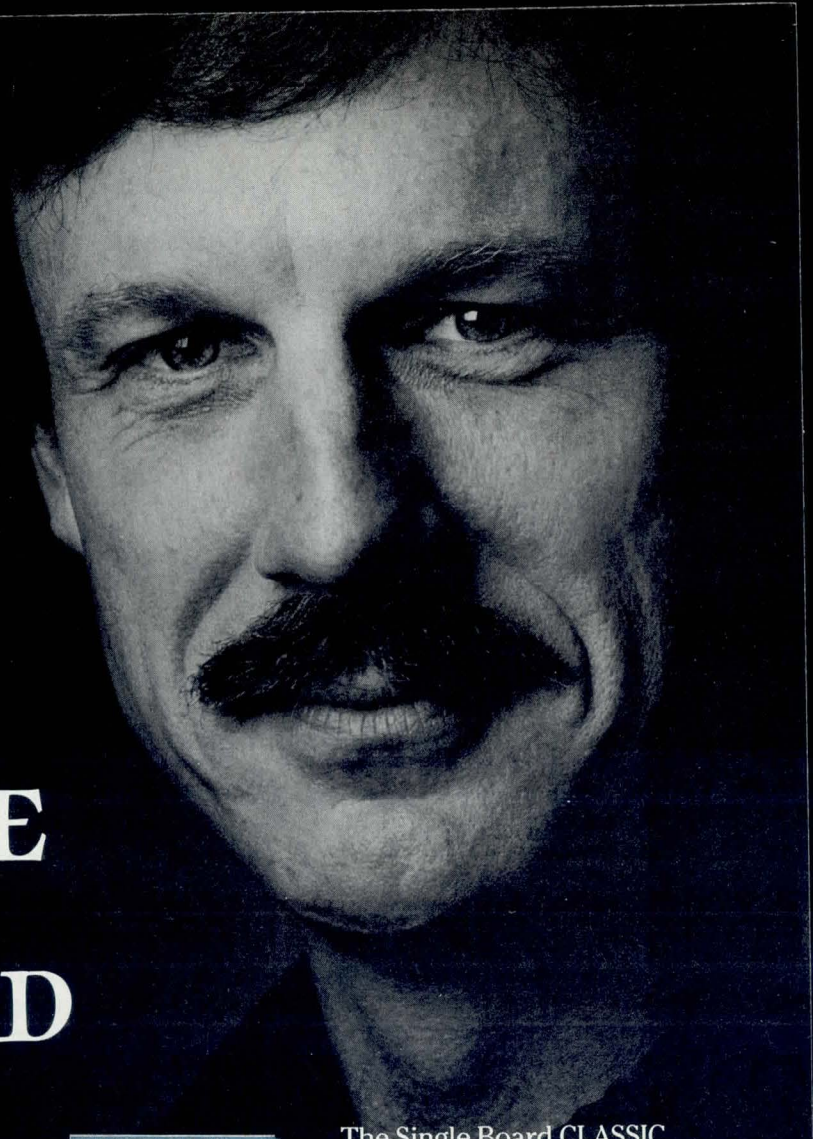

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CIRCLE 20

Vendors hedge

(continued from page 32)

individual clock and data lines to be used. Data rates are extended to 10M bps through the use of non-return to zero, change on 1 (NRZI) data encoding techniques, rather than holding to the slower rates via modified frequency modulation (MFM). Disk drives can readily support capacities exceeding 100M bytes with the higher data rate. In addition, the serial transmission mode called for in either proposed interface can keep average access times down to 35 ms.

Compatibility questions

With much in common, the BSR X3.101 and ESDI specifications seem to differ only in the physical cable used and ambiguities within the command set. Yet, such minor differences raise compatibility questions significant enough to delay the manufacturers' commitment to either interface. Only four of the 15 drive vendors endorsing the ESDI proposal are actively designing products—Disctron, Inc (Milpitas, Calif), Magnetic Peripherals, Inc/ Control Data Corp (Oklahoma City, Okla), Maxtor, and Memorex Corp (Santa Clara, Calif).

Likewise, Priam Corp has failed to win over other principal vendors of 8″ BSR X3.101 drives, such as International Memories, Inc (Cupertino, Calif) and Micropolis, (Chatsworth, Calif) which are most likely to implement that interface on their 5¼″ products. Most controller manufacturers show no preference for either interface. Perhaps as a compromise, Data Technology Corp (Santa Clara, Calif) hedges its bets by having controllers available for either interface.

Cost and technical superiority play little part in the deliberations. According to Priam Corp's calculations, the cost of implementing either interface on a computer system differs by less than $2. Both factions agree that neither interface is technically superior to the other. The major delay seems to stem from the extensive redesign involved in moving the data separator to the disk drive. This in turn causes each vendor to carefully scrutinize each interface for any other required modifications.

The BSR X3.101 specification changes the 2-cable connection (34 and 20 pins) used in the ST506 interface to a single 50-pin ribbon cable. The ESDI proposal retains the same cable setup used in ST506, but redefines many of the signals for serial operation. A stepper mode is also specified in the ESDI that retains most of the ST506 signal definitions and commands, while still transmitting NRZI-encoded data. BSR X3.101 also specifies an 8-bit wide bidirectional bus for the command protocol, while ESDI uses a 16-bit serial line—another difference noted among the specifications.

Perhaps more troublesome than physical differences is whether either interface can be thought of as a standard, whether *de facto*, as was the ST506, or blessed by a sanctioning body such as ANSI, IEEE, or ISO. Compatibility of different vendors' disk drives built to a published specification with different controllers built to that same specification has become of extreme importance.

Both interface proposals contain enough ambiguities in their published specifications to hinder compatibility among different drive and controller implementations. Even sanctioned standards cannot determine who is responsible if drives and controllers do not work with each other. There are incipient, problematic concerns surfacing from each interface proposal.

The ESDI still contains unresolved questions regarding maximum data rate (20M or 24M bps), as well as specific soft-sectored formats and run-length limited codes. The BSR X3.101 specification is so broad in implementing optional command sets that several vendors, including International Memories, Kennedy Co (Monrovia, Calif), Micropolis, and Priam have discussed what should be considered a "standard" implementation of the interface for 8″ disk drives. Several vendors agree

(continued on page 36)

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CIRCLE 21

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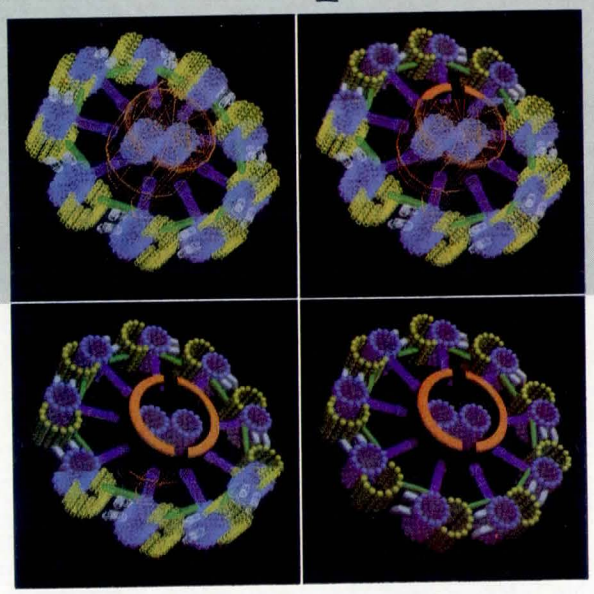

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CIRCLE 22

Vendors hedge

(continued from page 34)

that a similar effort is needed to bring the BSR X3.101 proposal into the 5¼" realm. Questions pertaining to soft-sectored formats and run-length limited codes are also not fully addressed in the BSR, although general provisions are made for both.

Pushed to the limits

Because of these unanswered questions, some vendors are choosing a third path to higher disk capacities. That is, to push the proven ST506 interface past its present 5M-bps data rate. Both Evotek Corp (Fremont, Calif) and Vertex Peripherals (San Jose, Calif) plan to increase the data rate to around 8M bps, while retaining ST506 signal definitions and commands.

However, compatibility with other ST506 disk drives is lost since modifications are needed to the data separator (primarily changing component values for resistors, capacitors, and crystals) and to some firmware portions of the controller. Other vendors are investigating this modified ST506 interface as an interim solution until either BSR X3.101 or ESDI emerges as the industry leader.

—Joseph Aseo, Field Editor

DEVELOPMENT SYSTEMS

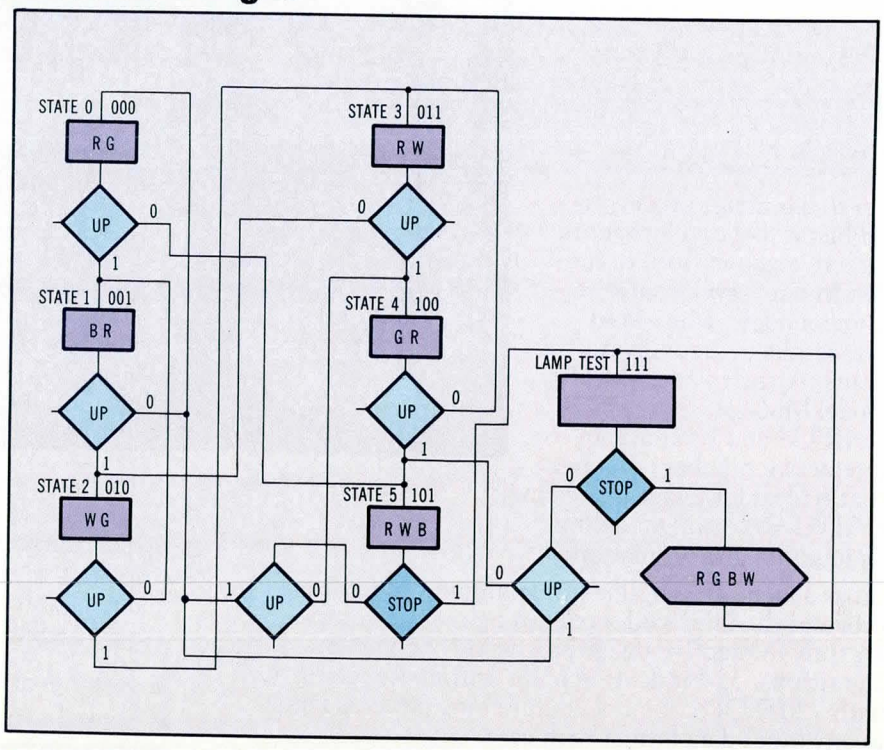
Software tools automate circuit designs

Design automation systems grow by adding software tools to a hardware base. Both hardware design and verification become relatively automatic using circuit design software running on Daisy Systems Corp's Logician and Gatemaster design systems. One package lets users design and realize finite state machines; the other two use the data base created for the company's logic simulator to help build testability into ICs and systems, and to verify the testability.

A finite state machine (FSM) is a common way to describe what a circuit is intended to do, and in what order. Every possible action is described, as well as every possible reaction to inputs. However, building an FSM manually, even with PLAs, is a time-consuming and error-prone process.

Daisy Systems' hardware compiler includes a graphic language, which uses three symbols, for building state machines. A state box describes the outputs of the system between clock pulses, a decision box shows the possible results of inputs to the system, and a conditional output box depicts which outputs occur as the system changes from one state to another. An underlying assumption is that the system changes state every time a clock pulse is received.

In addition, the hardware compiler can translate the graphic representation to a linguistic one, which



As part of Daisy Systems' hardware compiler, a simple finite state machine controls a set of four lights, noted as red (R), green (G), blue (B), and white (W). There are six distinct states, and two input signals (UP and STOP). The flow of control passes from a given state (boxes) through a decision point (diamonds) on every clock pulse. When STOP is true, the FSM cycles forever through a lamp test (state 111).

can be compiled into a procedure for programming a logic array. The two major constructs of this language are the familiar IF (variable) THEN...ELSE...and NEXTSTATE. The user can also enter a description of the state machine directly in the PLA compiling language.

At this point, the compiled PLA specification can be run through a minimizer to find the minimum

(continued on page 38)

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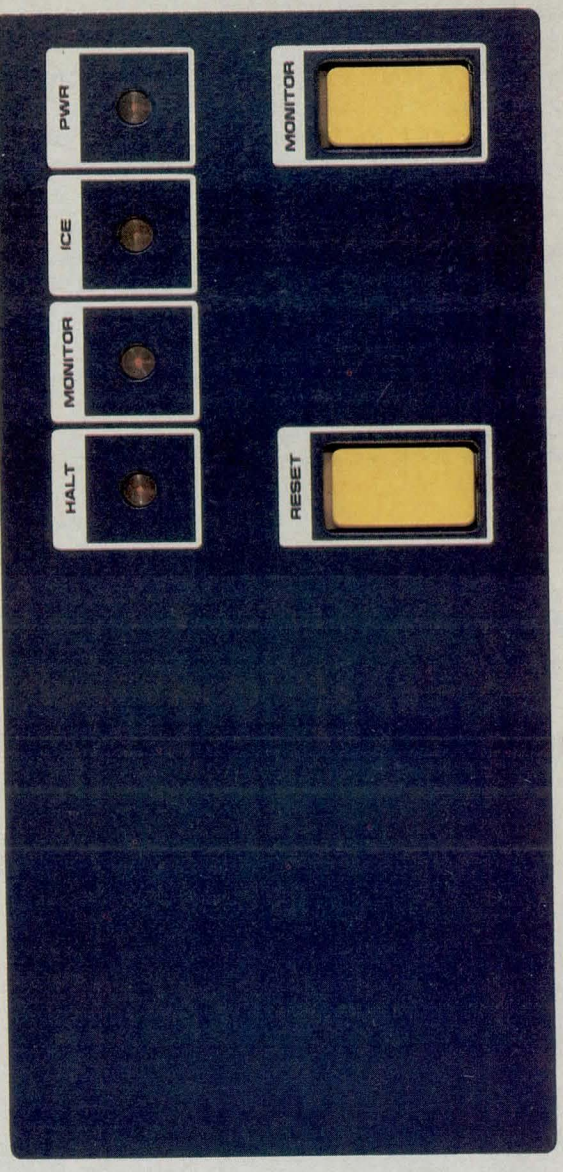

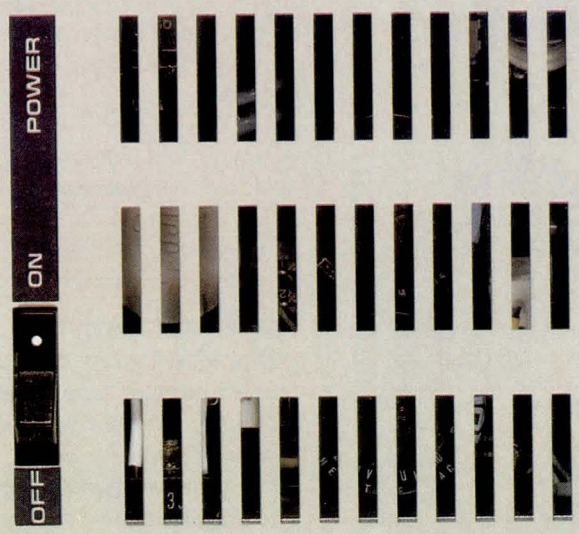

8088

FOR 9808 8808

IN-CIRCUIT DEBUGGER 178

i86·i87/i88·i87 USE BY INTERNAL CHANGE

Software tools

(*continued from page 36*)

number of inputs and choices needed to make the state machine run properly and to increase its speed. Once the data required to build an FSM are available, FPLAs, PLAs, PROMs, or EPROMs can be programmed via an RS-232 connection to a device programmer.

The compiler runs entirely within the Daisy engineering environment and lets the designer specify circuit behavior without worrying about physical implementation. Since the computer system maintains the design file, necessary changes can be made easily, and the state machine is verified as correct in the initial stages of the design process.

Building in testability

Testing complex VLSI devices also typically eats up time and resources. Quality control, on the other hand, is an absolute necessity.

The Daisy testability analyzer runs on the company's Logician and Gatemaster workstations and uses the same data base as the logic simulator. Both the IC and system-level designs can be tested interactively or automatically with the analyzer. Used in conjunction with the logic simulator early in the design cycle, it can indicate how testable a digital circuit is and suggest possible improvements.

After a few iterations with the testability analyzer, a test program can be generated for the proposed circuit. This test program is then passed on to the fault simulator for verification. The fault simulator completes a statistical simulation, selecting nodes to be tested either at random, or as specified by the user. Both visible faults that cause a measurable change in the circuit under test and invisible faults can be simulated. The program generates comprehensive fault reports, a fault dictionary, and histograms, as well as supports incremental test vectors.

All three programs are supplied as part of the standard set of software tools for new machines, and as no-charge upgrades to existing systems. **Daisy Systems Corp,** 139 Kifer Ct, Sunnyvale, CA 94086.

Circle 241

SYSTEM TECHNOLOGY

(*continued on page 44*)

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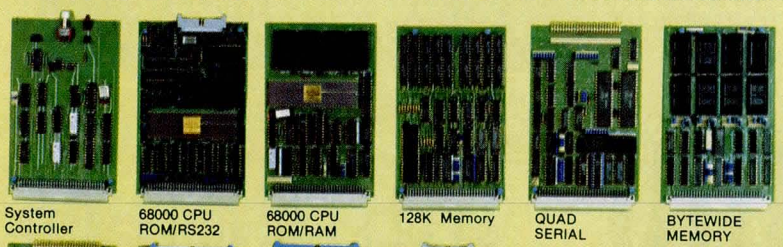
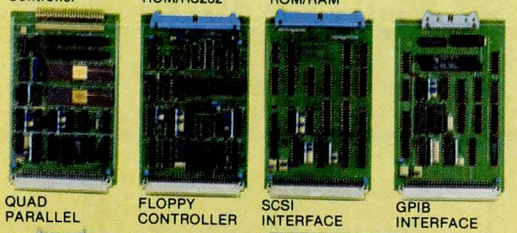
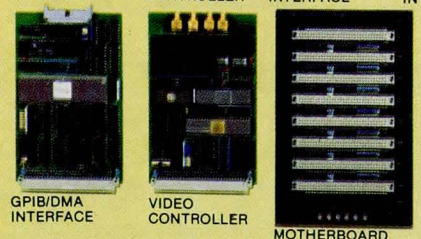


System Controller | 68000 CPU ROM/RS232 | 68000 CPU ROM/RAM | 128K Memory | QUAD SERIAL | BYTEWIDE MEMORY



QUAD PARALLEL | FLOPPY CONTROLLER | SCSI INTERFACE | GPIB INTERFACE



GPIB/DMA INTERFACE | VIDEO CONTROLLER | MOTHERBOARD

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CIRCLE 24

Get your own

If you're reading someone else's copy of Computer Design, why not get your own? To receive a subscription-application form, circle **504** *on the Reader Inquiry Card.*

This Lundy has an all-pervasive breath-takingly beautiful 4097th color. It's called high resolution.

Lundy's T5484 Color Raster Graphics Terminals have the highest color resolution available. Think of that resolution as a Super Hue—a 4097th color—that mixes with all other 4096 colors to make each as sharp as you've ever seen.

Our 5480 Series of color raster terminals and workstations aren't the only ones with 4096 colors. But the colors have never looked so good. Because resolution has never been higher.

New standards.

The 1536 × 1024 pixels set a new standard for displayable resolution. Raster staircasing is significantly reduced without the complexity of anti-aliasing.

But new standards don't stop with highest resolution. Areas are filled virtually instantaneously so the 5480 Series also sets a new standard for polygon fill.

Vector generation sets a new standard, too. The time lapse between the moment you draw until the picture is generated is as much as 50 percent faster than many others.

Enemy of obsolescence.

You shouldn't be forced to ditch programs in place when you buy a new terminal. For that reason, standard with all 5000 Series models is a Tektronix 4010 or 4014 Emulator with mixed-mode software switch for enhancing existing programs with color-native protocol.

Lundy's 5484 color raster design workstation.

Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software development program to provide the most comprehensive application packages.

Lundy will help you see more in graphics.

When you look at our 5480 Series, take a close look at Lundy, too. We're a company that's as good as its products.

A company that balances high tech with solid business sense.

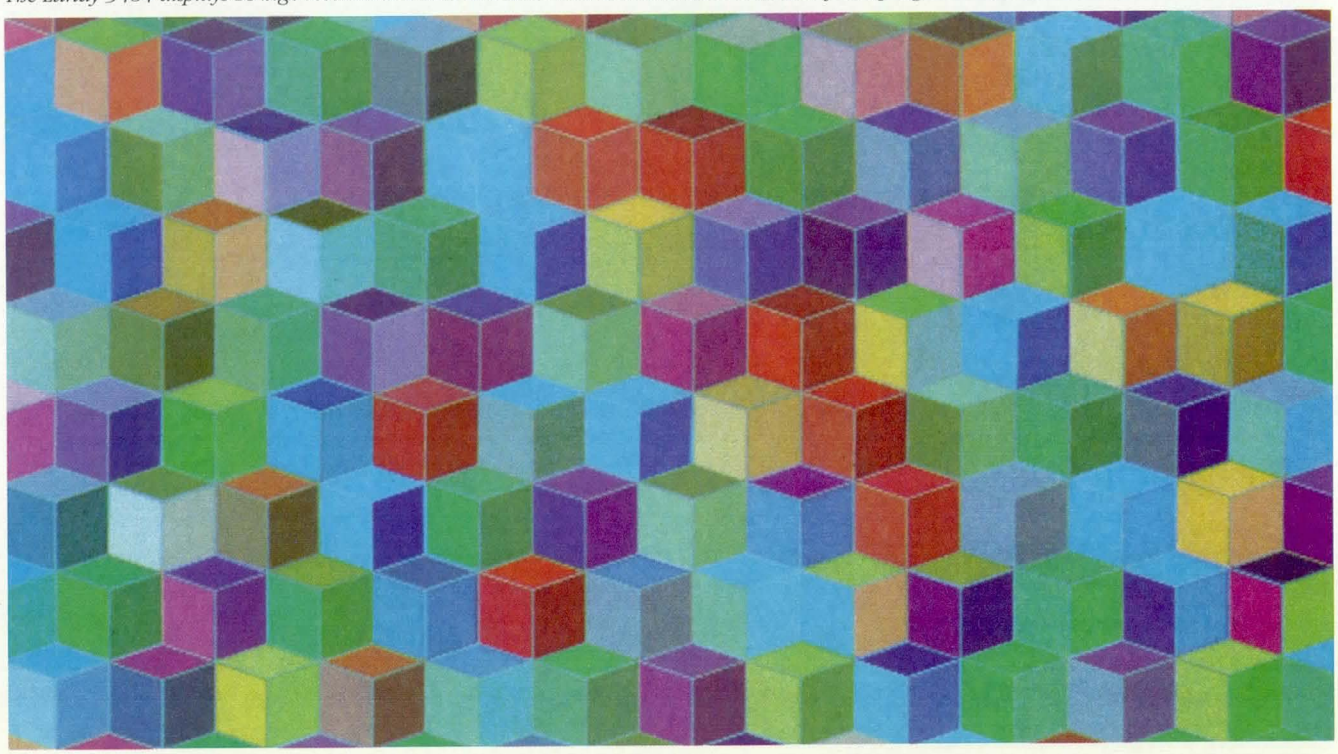
A company as proud of its service (one of the largest service organizations in the industry—39 locations nationwide) as its engineering expertise.

A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

For more information, write Lundy, Glen Head, New York 11545, or call: (516) 671-9000.

LUNDY®

The Lundy 5484 displays 16 high resolution colors at a time. User downloadable character fonts; programmable character sizes.



CIRCLE 25

Share is the reward for quality.

We've been rewarded.

Computer Memories is the leader in large-capacity 5¼" Winchester disk drives. That didn't happen by accident. We simply delivered the high quality that the market demands.

We did it with optimum design and strict quality control. By using proven concepts and only quality materials, and then completely testing for all possible defects.

For instance, every Computer Memories drive is placed in a dedicated burn-in room at 120°F and then operated constantly for three full days. If there is even a slight out of spec condition, it isn't shipped.

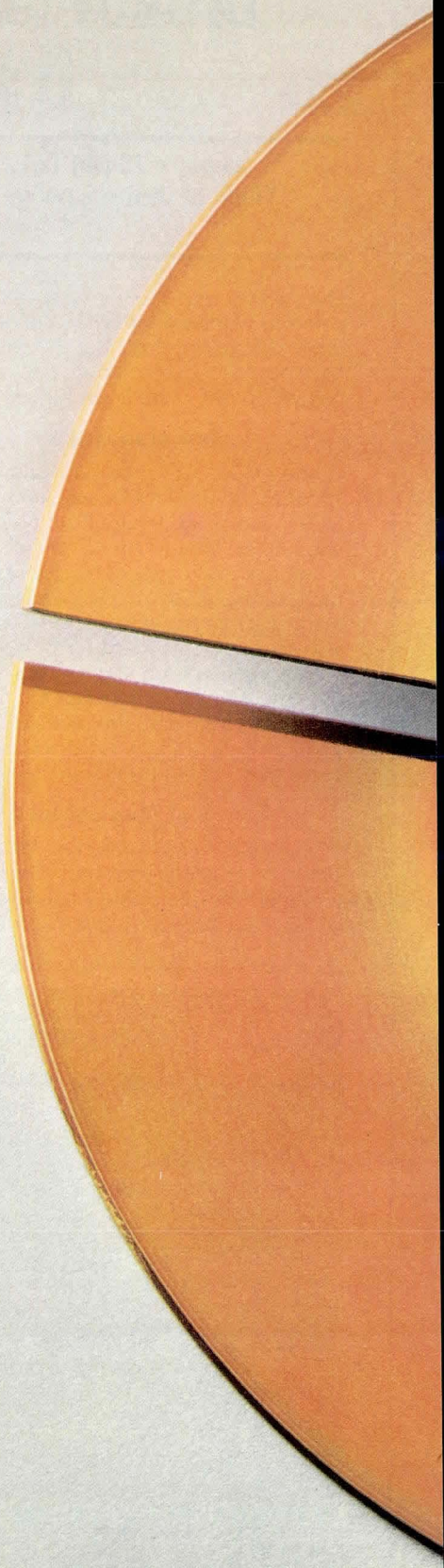
We also make random selections of drives and submit them to life tests, in which they are operated day after day, month after month. The eighth unit we ever produced is still being life-tested, and is still running strong.

The result of all this testing is a remarkable plug-and-play reliability record for our complete line of 12, 19, 26 and 40-megabyte drives. It's a reliability record that nobody else within the industry can match. That's why we have a position in the market nobody can touch.

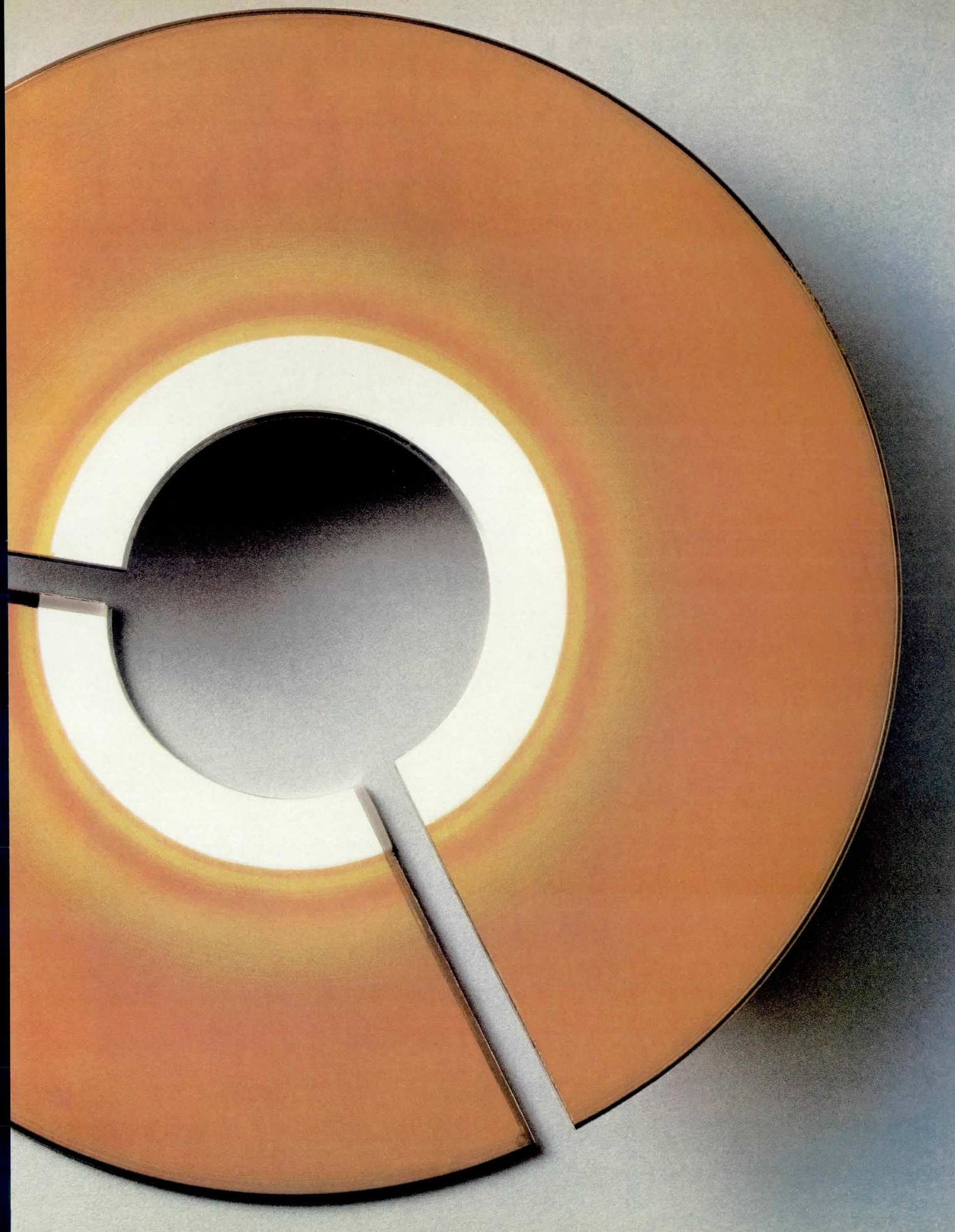
The capacity leader.

Computer Memories Incorporated

9216 Eton Avenue, Chatsworth, CA 91311 (213) 709-6445/ Ft. Worth, TX, (817) 332-7859/Costa Mesa, CA, (714) 241-9260/Springfield, MA, (413) 783-2386/In Europe: Bray-on-Thames, Berks, UK, 06283-4281 Telex 847591. For small quantities, call Schweber Electronics, (800) 645-3040.



CIRCLE 26



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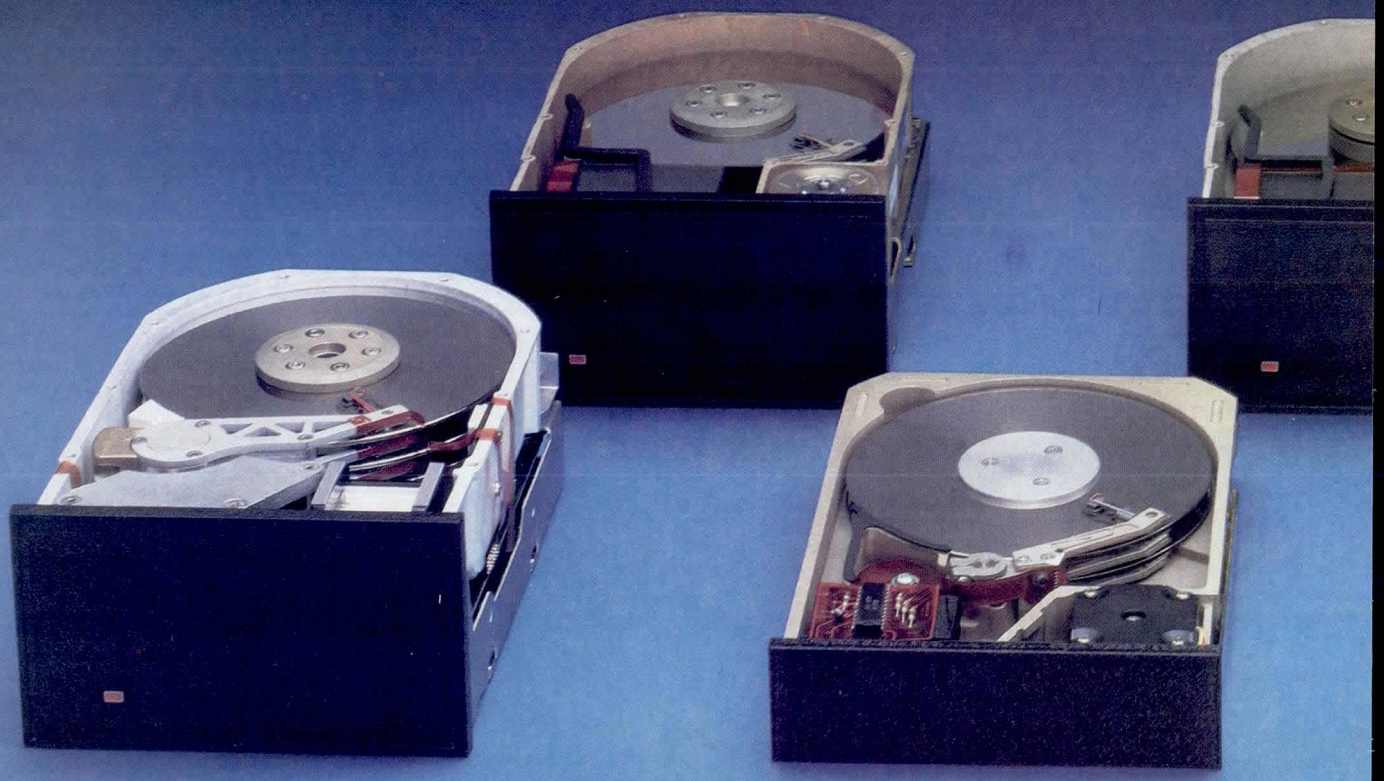

Since we first entered the Winchester market two years ago, we've accomplished many things our competition claimed were impossible.

It was impossible, they said, for a floppy disk company to make a significant dent in the highly competitive Winchester market.

We've not only made a dent, we're the second-largest company in the business, and we have the capacity in place to be first.

It was impossible to expand our production capacity from 0 to 60,000 drives a month practically overnight. But we did it.

It was impossible to sell Winchesters at such a low cost. But last year our 500 series drives were introduced at under $500, 30% under then-standard industry costs. And since then, we've led the industry to ever-lower costs on full and half-height drives.

It was impossible to produce and ship high-performance plated media drives in high volume at prices lower than most vendors are charging for oxide media drives. One of our competitors backed away from plated media because they couldn't buy enough of it to build drives in efficient quantities.

We solved that problem by building our

Tandon Corporation. 20320 Prairie, Chatsworth, CA 91311, (213) 993-6644, TWX: 910-494-1721, Telex: 194794. Regional Sales Offices:
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UR COMPETITION, POSSIBLE.

own plated media factory dedicated to plated media production in high volume. Because we make our own, our costs are low and we are independent of outside vendors for supply.

It was impossible for a start-up company to produce and ship a broad line of products: full and half-height drives, open and closed-loop, from 6.4 to 50 MB. But we've done it. With the help of one of the industry's best-funded R&D programs. And with our steady supply of plated media, we will soon be offering 5¼" drives that push Winchester technology to the limits of its capacity. In high volume. At prices that are pure Tandon.

Impossible?

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But not for the Tandon Winchester Company.

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CIRCLE 27

Symbolic debug, code analyzer ease microprogramming

Microprocessor and bit-slice designers benefit from symbolic debug and performance analysis features added to Step Engineering's Step-7 firmware integration and test station (FITS). The microcode development system now displays source code so that users no longer need refer to an assembler listing to interpret the address sequence in the trace buffer. By applying labels that remain the same from one assembly to the next, users can also specify addresses. In addition, performance optimization allows offline analysis of the trace buffer contents to show address, event, and time-interval distributions.

Symbolic debug capability consists of two elements: user source (USOURCE) and user symbol (USYMBOL). USOURCE allows users to read instruction mnemonics and labels directly rather than having to painstakingly correlate them with the numeric display or printout of the microcode. By interleaving lines of source code with the display of the writable control store's contents USOURCE permits easy comparison with the original assembly listing. By allowing users to reference memory locations with source code symbols, USYMBOL provides a bridge between microde and program source code.

When the trace buffer contents are displayed, they very often contain realtime address sequences that jump around a great deal. The interleaved source listing allows users not only to see the instruction source listing in the order of execution, but to check the current machine state also stored in the trace buffer.

In addition to defining and using symbolic names to specify addresses, designers can use them to specify breakpoints. Thus, after one or more reassemblies, which can alter the position of addresses, the functional breakpoints defined as symbols will remain in the desired program flow locations.

This proves quite convenient when used with the Step-7 GO command, a "jump and execute" command for the target processor. Instead of specifying an absolute address, users name the starting point and desired breakpoints, using their labels in much the same manner as with a microprocessor development system.

The performance optimization and analysis tools operate with the logic (LSA-1), which is part of the Step-7 development system. They deal with the fact that microcode, even after it is debugged and running correctly, may not be running efficiently.

Event occurrence allows both 16-bit addresses, and 16- or 32-bit data that are entered in the trace buffer, to make up an event. Since not every event bit is pertinent to the analysis, it is possible to use a "don't-care" mask to disable selected bits. Thus, an event can be address, data, or some user-defined combination of address and data. Up to eight events can specify any given analysis.

Time interval measurement depicts a histogram of the time spent in a given memory range. The address histogram displays the percentage of time spent in specific addresses as defined by their symbolic label.

Analysis results are used to detect problem areas and to determine minimum, maximum, and average times for "wait" or "status check" routines. Step-7 typically sells for $20,000 with 30-day ARO availability. **Step Engineering,** 757 Pastoria Ave, Sunnyvale, CA 94088.
Circle 242

SYSTEM TECHNOLOGY
(continued on page 46)

Premier Edition Preview—
Portable computers—in late October.

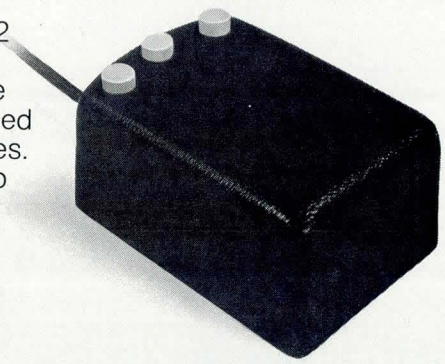
Mouse Controls
Cursor Control The Easy Way

They operate on any surface. They're easy to use. And they're durable.

They're the new Series 122 mouse for cursor control. From Measurement Systems, of course.

The key feature of these versatile user friendly position entry devices is the long-life x and y optical encoders. They're independently driven, with very low friction and torque requirements. That makes the controls exceptionally easy to use. And it reduces to a bare minimum the chance that dirt or loose materials will interfere with normal operation.

You can get any of the Series 122 mouse controls with quadrature square wave output, scaled pulse output, variable pulse rate or coded digital, in up to 3 function switches. Standard counts range from 20 to 300 per inch of mouse motion.



Once you've seen these controls in action, you'll be a confirmed mouseketeer, too. Contact us for more information.

MS Measurement Systems, Inc.
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THE WY-50.
PRETTY SMALL
A NEW GENERATION OF LOW-COST TERMINALS FROM WYSE.

Never before has anyone put so much into something so small. The WY-50 gives you big terminal features without occupying your entire work-space. This took revolutionary design. Design a lot of people couldn't accomplish for the price. But we did.

In fact, the WY-50 introduces a new standard for low-cost terminals. You get a compact, full-featured design that meets the most advanced European ergonomic standards. 30% more viewing area than standard screens. And a price tag as small as they come.

The WY-50 sells for only $695.00.

FEATURES:

- **14″ screen.**
- **80/132 column format.**
- **Soft-set up mode.**
- **High resolution characters.**
- **Low-profile keyboard.**
- **Industry compatible.**
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For more information on the revolutionary design, outstanding features and unique good looks of the new WY-50, contact WYSE and we'll send you a brochure filled with everything you need to know. The WY-50. The full-featured terminal with the small price.

WYSE *Make the Wyse Decision.*

WYSE TECHNOLOGY, *3040 N. First St., San Jose, CA 95134, 408/946-3075, TLX 910-338-2251, in the east, call 516/293-5563, call toll-free, 800/538-8157, ext. 932, in CA 800/672-3470, ext. 932, in the midwest, 313/227-5011, in So. CA, 213/340-2013.*

CIRCLE 29

Image recorders copy display photographically

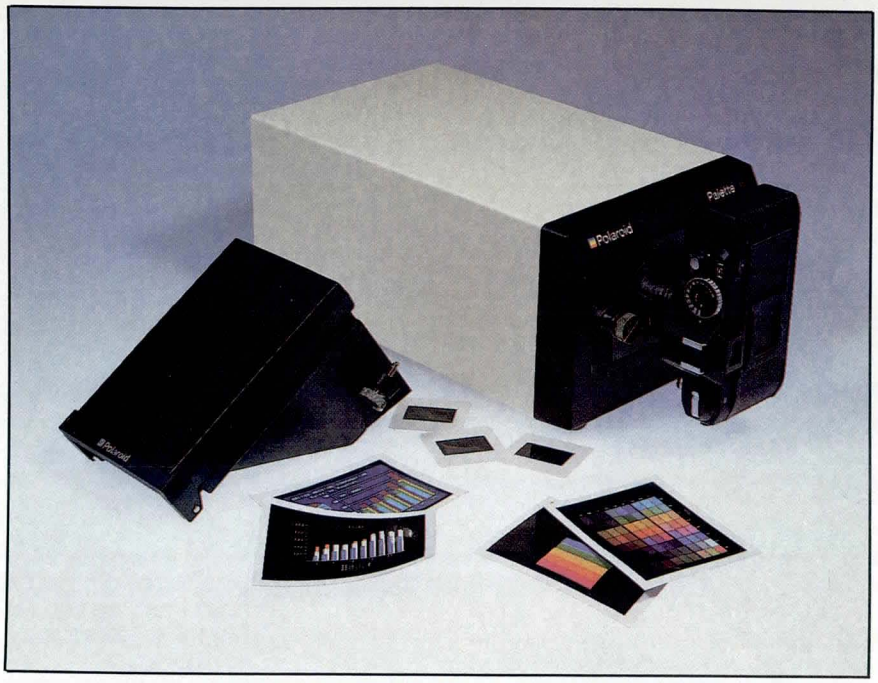


Fig 1 Palette computer image recorder produces photographic-quality hard copy from small computer terminals. Polaroid's system forms 35-mm color slides from color or black-and-white computer graphics displays on personal and small business computers. An optional camera back produces 3¼ ″ x 4¼ ″ prints.

Cameras could displace the printer and the plotter as hardcopy output devices. Some astute people have brought the camera into the I/O picture where it serves to transfer the CRT display directly to its hardcopy image. A simple connection between the camera and the display's video output lets users expose the image on the spot, producing instant prints, or with slide-making apparatus, instant slides.

As one might expect, the two giant camera manufacturers—Kodak (Rochester, NY) and Polaroid (Cambridge, Mass)—lead the field in instant imaging. Other electronic companies, however, have also developed systems that are either based on devices from Polaroid or Kodak, or are of a unique design. The companies include Celtic Technology (Woodland Hills, Calif) and Lang Systems, Inc (Menlo Park, Calif).

Whereas high-resolution systems like Dicomed's Dicomedia and General Electric's Genigraphics sport price tags between $60,000 and $400,000, these low-end devices feature good resolution at prices under $7000. Polaroid's Palette computer image recorder, for instance, costs around $1500. It was designed specifically for personal and business computers to make presentation-quality color and black-and-white graphics hard copy on Polaroid's 35-mm Autoprocess transparency films and on Polacolor instant print film type 669.

Palette connects to the computer via an RS-170 video line and RS-232-C communication line. The compact unit measures 16 ″ x 8 ″ x 6 ″ (40.6 cm x 20.3 cm x 15.2 cm) and weighs only 12 lb (5.4 k) (Fig 1). It can be used with IBM Personal Computers, and with Apple II Plus and Apple IIe computers. Polaroid is also determining Palette's compatibility with other computers.

The unit comprises a flat-faced, 920- x 700-line resolution monochrome video screen with a tri-color filter wheel. The wheel lets even monochrome-display computers with graphics capability produce a color hardcopy output. An internal computer matches exposure parameters to the film being used, while allowing users to control color selection and location.

Palette maintains low cost by putting its image manipulation features in software supplied in diskette form. Included with the system, these features allow users to select any of 72 colors for changing or adding colors on the film. Users can manipulate the system to create a virtually unlimited number of color sets to match or modify a given computer's color display. Other features include transfering pre-existing images from disk to film without modification, eliminating raster lines using a fill technique, and exposing a batch of images through automatic sequencing.

Driver development

Independent publishers of graphics software packages are currently developing drivers to provide Palette users with additional options for hardcopy imaging. These include hidden surface removal for 3-dimensional graphs, and interlacing to enhance color saturation and improve image resolution.

Other systems also use Polaroid equipment. Lang Systems, Inc (Menlo Park, Calif), for example, uses its VideoSlide 35 (Fig 2). This computer graphics camera system is a 24-kHz line rate version for compatibility with high-end workstations. These include the Apple Lisa, the NEC Advanced Personal Computer, the Vectrix 128 and 384 display systems, and graphics terminals such as the Advanced Electric Design 767, the Jupiter 7, the HMW C3419, and the Hewlett-Packard 2627A. The 24-kHz version is also adaptable to the Intelligent Systems Executive Presentation business graphics system.

The original VideoSlide 35 is compatible with systems that operate with line rates between 15 and 19 kHz. These systems include the Apple II, IBM's Personal Computer, Texas Instruments' Professional Computer and a wide variety of graphics terminals such as the IBM 3279, the Tektronix 4027 and 4113, and the Ramtek 6211 and 6214. Lang claims

(continued on page 48)

BENCHMARKS.

4SS-3106

STANDARDS FOR INTERFACE POWER ICs.

Sprague Series ULN-2000 Darlington Arrays still set the industry standard for power-interface ICs with improved ratings, hermetic packaging (cer-DIP or side-brazed), and processing to MIL-STD-883. Series ULN/ULQ/ULS-2000 (and ULN/ULQ/ULS-2800) high-voltage, high-current arrays have been driving relays, solenoids, stepper motors, LED and incandescent displays since Sprague introduced the ICs a decade ago. For Engineering Bulletin group 29304, write to Technical Literature Service, Sprague Electric Co., 555 Marshall St., North Adams, Mass. 01247. For application engineering assistance, call Mark Heisig at 617/853-5000.

SPRAGUE
THE MARK OF RELIABILITY

a Penn Central unit

CIRCLE 30

Image recorders

(continued from page 46)

that both versions allow users to generate 35-mm slides, at a cost of less than $0.50 per slide, in as little as half an hour, from images off these types of terminals. In a comparison, the conventional method of generating slides can take as long as three weeks from an outside studio and can cost up to $30 a slide.

To operate VideoSlide 35, users need only load standard 35-mm film into the camera and press a button. No additional software is required for system operation. The 24-kHz version costs $3049, including the camera unit and a TTL RGB video interface. The 15-kHz model is priced from $2799 and uses the same interface.

Celtic Technology's VFR 2000 uses a principle similar to Lang's and costs $2495. All of the above prices can be misleading, however; depending upon the final computer and camera system configuration, a system could end up costing nearly $5500.

The VFR 2000 interfaces with most computers that operate with the Lang system. It also can be used with DEC's Rainbow and Professional 350 as well as with Sony's personal computer. An example of the slide quality achieved from the VFR 2000 operating with a Ramtek 6000 graphics terminal is shown in Fig 3.

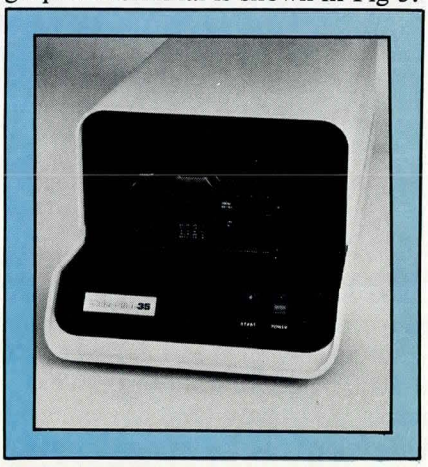


Fig 2 VideoSlide 35 interfaces with most graphics workstations, personal computers, and graphics terminals. In as little as half an hour, 35-mm color slides can be generated in-house at a cost of less than $0.50 per slide.

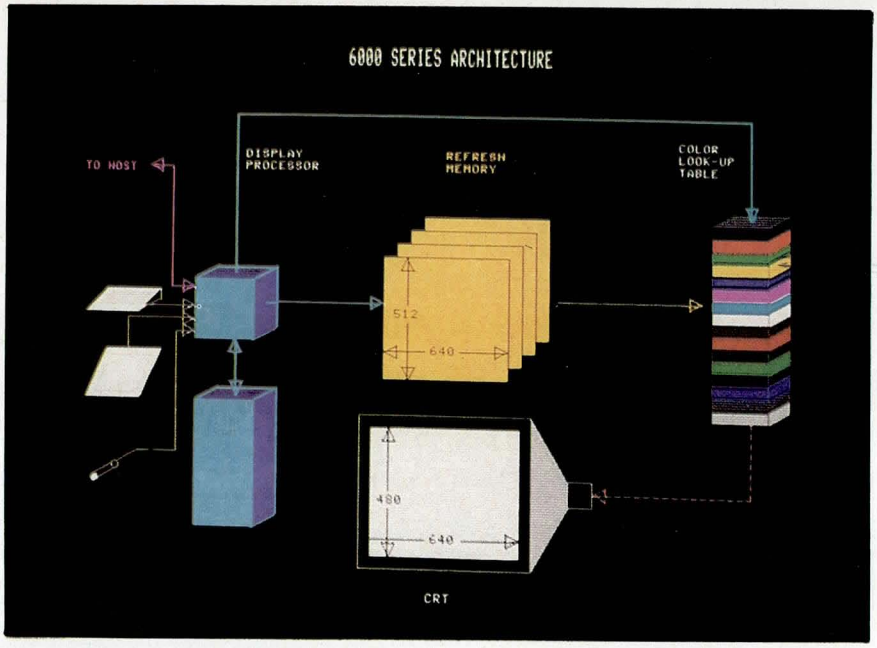


Fig 3 This slide produced using Celtic Technology's VFR 2000 with Ramtek's 6000 terminal shows the internal configuration of the 6000 terminal. The ability to generate slides quickly right off the screen is essential for audiovisual presentations in today's corporate environment.

The slide depicts the internal configuration of the 6000 terminal. While Polaroid, Land, and Celtic Technology use Polaroid's equipment exclusively for generating both slides and prints, Kodak's Instagraphic imaging system can be outfitted for any 12″ or 13″ screen. The $195 unit mounts right on the screen to product thin prints; if outfitted with a 35-mm camera, it can also generate slides. The imaging outfit includes the camera with a close-up lens, two packages of Kodak's Instagraphic color print film, a filter, and brackets for adapting a 35-mm camera to the cone.

To operate, the user must initially orient the unit. When proper cone alignment specific for each individual display terminal has been achieved, the outfit is ready for use. The cone with the attached camera is placed over the screen while holding the lens at the correct distance from the screen. This eliminates any problems with ambient light and parallax effect. The close-up lens is used to obtain a sharp focus and, if necessary, a filter can be used to balance the color for the screen phosphor in a particular terminal.

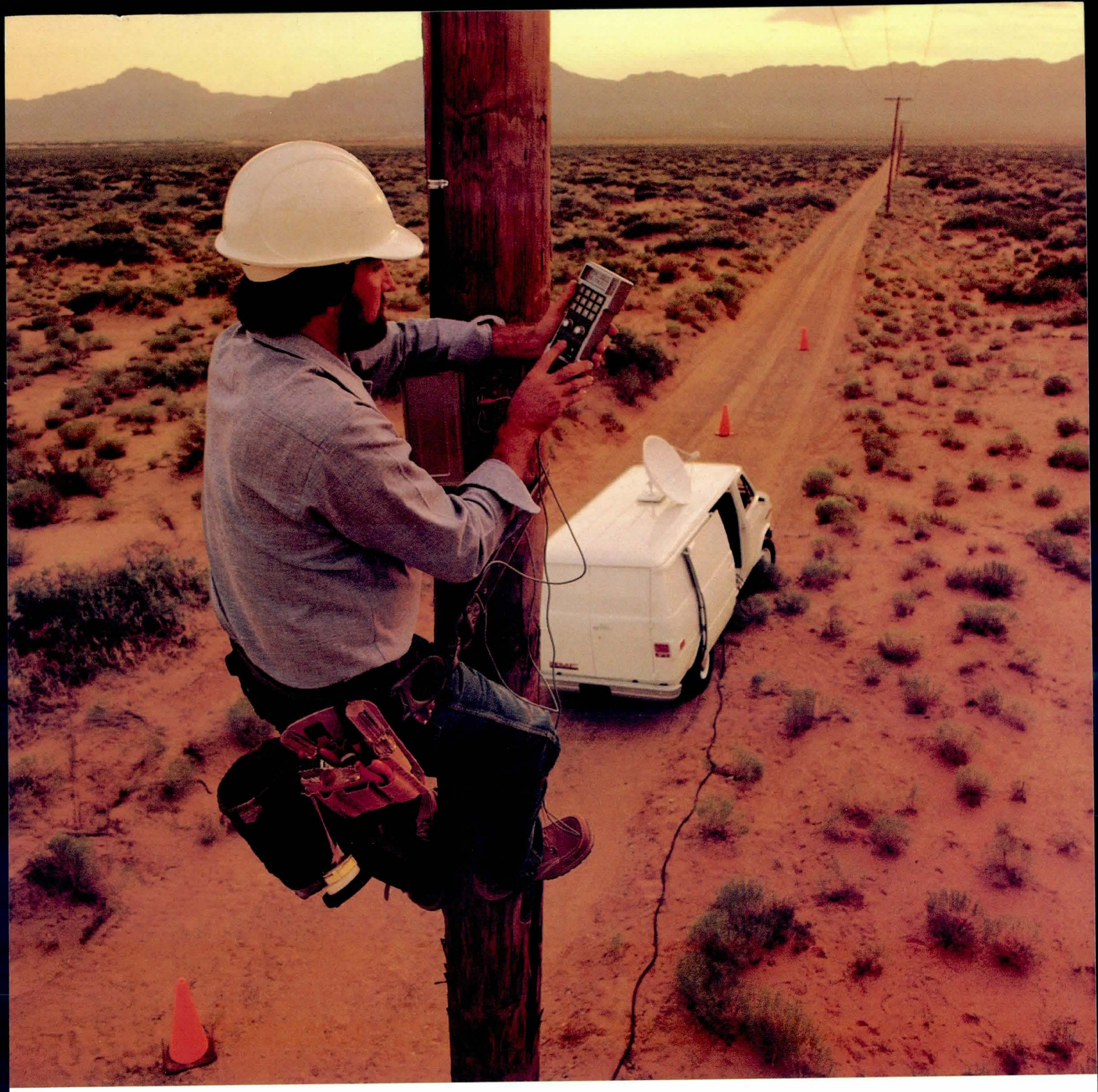
The camera uses Kodak's new instant film that is manufactured to industrial tolerances. The Instagraphic camera does not require focusing or exposure adjustment. When the shutter is released, the instant color print pops out of the camera. The picture area part of the print can either be left on its backing or removed after waiting for an hour.

Without the backing, the color print is as thick as a conventional 35-mm print, and as easy to trim and mount. The company has capitalized on its best asset and developed the Instagraphic film to be of equal reproduction quality to a 35-mm print, and just as thin and light. Consequently, a stack of fifty 3½″ x 4″ prints without backing occupies 25% of the space required as compared to the space needed when backing is left intact.

—Nicolas Mokhoff, Senior Editor

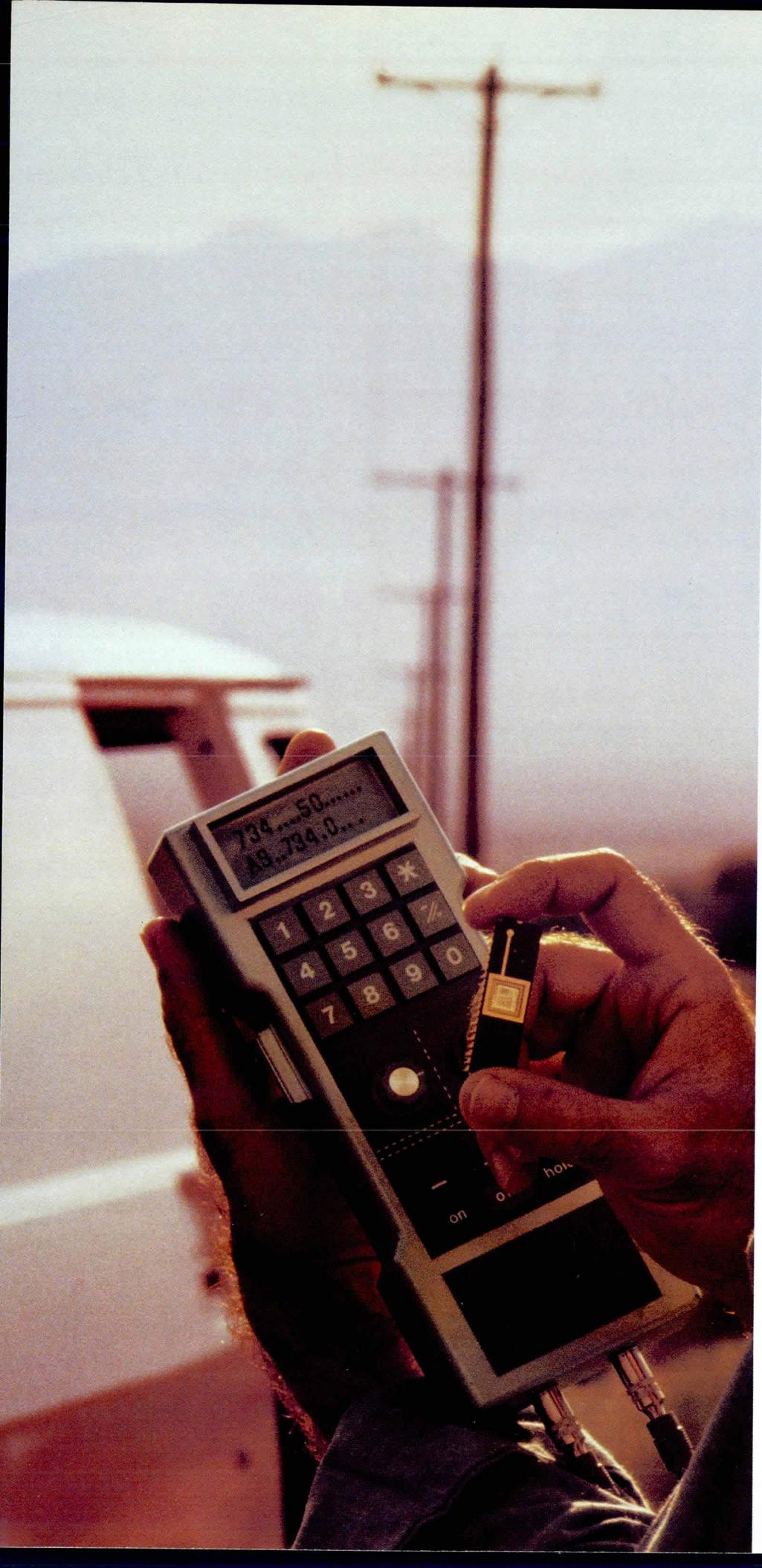
SYSTEM TECHNOLOGY

(continued on page 53)



Digital Signal Processing: Texas Instruments brings it down to earth by getting it off the ground.

- **Ultrahigh speed, precision, economy** of TI's new TMS320 Processor will spur widespread use of digital signal processing *(Page 2)*.
- **Easy implementation** of high-throughput, realtime applications, such as speech processing, is achieved with TMS320 *(Page 3)*.
- **Application design help** from TI includes a series of intensive seminars on digital signal processing *(Page 4)*. ▶



One-chip 16/32-bit

The processing speed of a bit-slice-based computer. In a single, 40-pin package. That's the new TMS320 Processor from Texas Instruments. Making digital signal processing (DSP) feasible anywhere, anytime.

For example, the lineman's advanced testing unit shown here. Only a concept now, it could be a reality tomorrow. The new TMS320 would enable the unit to process a staggering amount of data. Permit portability. Assure reliability. And allow quick programming changes for performing a wide variety of analyses to diagnose trouble, even up the pole.

5,000,000 instructions per second

This incredible performance is achieved through TI's modified Harvard architecture. It allows the TMS320 to fetch one instruction while executing another. In a typical application, more than 90% of all instructions are executed in a 200-ns cycle by the TMS32010 version.

32-bit precision

While the TMS32010 accepts 16-bit inputs and has a 16-bit output, its 32-bit arithmetic logic unit (ALU) and accumulator carries all of the arithmetic functions to 32 places. The ALU also features a 16-bit × 16-bit parallel multiplier that can form a 32-bit product in 200 ns.

Large on-chip memory

Data memory is supplied by 288 bytes of random-access memory. Enough to hold the data needed to perform a 64-point complex fast Fourier transform (FFT) while maintaining system-linkage variables and constants for other functions.

◀ **Low-cost digital signal processor,** TI's TMS320 is the inexpensive, single-chip alternative to multichip bit-slice systems and custom VLSI devices now used to process signals digitally. TMS320 speed and economy will open unlimited design opportunities for DSP such as the portable telecommunications circuit tester shown here conceptually.

economy. 200-ns cycle. TI's new processor makes DSP practical.

Digital Signal Processing: Coming of Age

Highlights from a discussion with Thomas W. Parks and G. Sidney Burris, Professors, Department of Electrical Engineering, Rice University.

Q. In your opinion, why has digital signal processing rather suddenly become practical and economical?

A. Well, digital signal processing has been possible for some years. We've had computers and bit-slice approaches that could do the job, but these were cumbersome, expensive, and consumed lots of power. One major factor accelerating the implementation of digital signal processing is the onward thrust of the electronic components industry.

The continued development of VLSI devices, by packing more and more circuitry on chip, has shrunk processor size dramatically. Throughput rates and architectures have also been improved enormously so that complex algorithms can be computed with incredible speed and reduced power consumption.

Of course, the development of these extremely efficient algorithms has contributed greatly to wider use.

Q. What do you consider the most outstanding advantages of DSP?

A. Digital signal processing provides the flexibility, precision, and speed required to execute increasingly sophisticated signal processing.

For example, spectrum analysis is frequently integral to signal processing, but for years there were no efficient, high-resolution methods to implement it. Now that VLSI digital signal processors can speed through the fast Fourier transform algorithm, such analyses are greatly simplified at a feasible cost.

Digital processing eliminates most voltage, temperature, drift, and noise problems associated with analog techniques. Digital filters can reliably meet tough specifications on magnitude and phase that would be difficult, or impossible, for analog filters to meet.

Q. What new applications do you see for DSP in the near future?

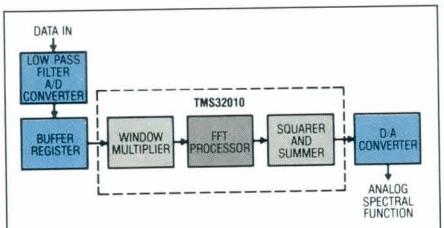
A. We are seeing digital technology applied to signal processing in image, seismic, and speech processing as well as in telecommunications, instrumentation, and high-speed control. In the near term—say, five to ten years—it is probable that we'll see digital signal processors becoming ubiquitous in the home, office, and factory. ■

TMS320 processors excel at realtime applications.

Because of their high-speed numeric capability, the new TMS320 processors can be used for realtime computations in many applications: Telecommunications. Instrumentation. Voice recognition and synthesis. Image processing. High-speed process control.

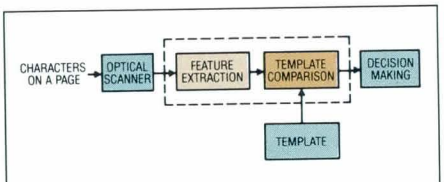
The TMS320 family can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, and FFT—performing a 64-complex point FFT in only 580 μs!

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features, then perform a template comparison to achieve optical character recognition.



New TMS32010 simplifies spectrum analysis

The efficient TMS320 devices can also be used to build high-speed modems having rates up to 9600 baud.



New TMS32010 enhances image processing

With full-speed memory expansion capability, the TMS320 DSP family can be used in many other applications. ■

See back page for more information.

Full development support

In-depth support for the TMS320 consists of a host-independent development system, as well as software that can be run on a variety of host computers. An evaluation module, macro assembler/linker, simulator, and full in-circuit emulation are now available.

Choice of three

The TMS320M10 microcomputer is designed for applications where up to 3K bytes of program memory are mask-programmed into the read-only memory (ROM), expandable with up to eight kilobytes of total program memory (5K bytes off chip at full speed).

The TMS32010, a microprocessor without on-chip ROM, addresses up to 8K bytes of off-chip program memory at full speed.

A military version, SMJ32010JDL, is available processed to the requirements of MIL-STD-883B.

There's much more to learn about the TMS320 family. For our brochure, return the coupon on the following page. ■

Learn how to design with DSP. At a nearby, two-day TI seminar.

You can become thoroughly familiar with the ground rules of digital signal processing. And learn when and how to apply TI's remarkable new TMS320 processors. Conveniently and economically.

Two-day DSP/TMS320 seminars are being held by TI at selected locations around the country (see schedule at right). Developed in conjunction with recognized DSP authorities, the seminars will present the basics of DSP theory and cover in detail the flexible modified Harvard architecture of the TMS320. A full morning will be spent studying practical applications of DSP—an intensive review reinforced by in-depth demonstrations.

In order to gain the most from the seminar, you need to have knowledge of, or experience with, microprocessors and/or programming.

Included in the $395.00 cost of the two-day seminar are all study materials—user's guide, manuals, notebook—lunch each day, and a reception. A special package including a TMS320 Evaluation Module is also available for $995.00.

Call (713) 879-2001 to enroll in the seminar most convenient for you, or for more information.

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TEXAS INSTRUMENTS

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Computer control store swapped for speed

Faster application program execution results from swapping speed-critical portions directly into the control store of the Lambda computer from Lisp Machine, Inc. A microcompiler converts already assembled Lisp object code into microcoded equivalents, thus simplifying microprogramming tasks.

The computer's flexibility also extends to its hardware design. A high speed bus primarily handles processors and memory devices, while slower peripherals such as disk drives and printers reside on a separate Multibus backplane. A system diagnostic unit (SDU) supervises interbus communications and automatically monitors the status of installed devices.

In addition to microcoding high speed application program sections, the microcompiler can be used for application-specific instruction sets and to secure proprietary software. Users can directly address 52K words of the 64K-word virtual control store memory without regard to the control store's actual size (a limitation in previous machines). Because 12K words are reserved for system programs that remain at all times, paging techniques load only 16 word segments at a time from disk into the 16K-word physical memory.

Such microcompilation techniques more than double performance speeds as compared to conventionally compiled Lisp programs, according to the company. However, users must first complete program flow analysis to determine which low level functions are performance bottlenecks. These bottlenecks usually occur because of the extensive overhead needed to keep object programs at the symbolic assembly language level, rather than at the more compact machine language level. The microcompiler strips off this overhead as setup routines from the assembled object code and optimizes the remaining microprogram.

Memory addressing scheme

Virtual control store memory complements the memory addressing capability of the Nubus system backplane, where the 4-board Lisp processor resides. Nubus architecture treats the system backplane as a 4.3G-byte wide memory pool, rather than implementing conventional Multibus or S100/IEEE 696 bus arbitration logic. Each device on the backplane has a 32-bit address that not only identifies the slot location (4 bits) but also selects an address within the slot (24 bits). The remaining 4 bits allow up to 16 Nubus machines to be connected into a local area network.

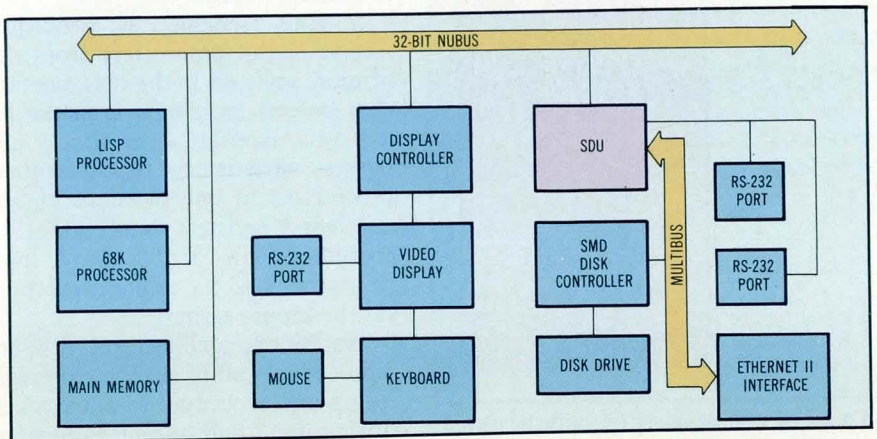
This memory addressing scheme eliminates the significant overhead associated with bus arbitration. In conventional systems, one device initiates data transfers, asserts control of the bus, and sends a message to the intended receiver. The bus is then used to initiate the actual data transfer, and to have the receiver acknowledge the transfer.

However, the Nubus transfer scheme does closely resemble memory transfers within a monolithic processor, even though many processors may reside on the bus. A processor merely specifies the 2-address memory location of the desired data in a packaged request, asserts ownership of that memory location (even if it is another processor's register) and relinquishes control when finished. Bus overhead is minimized since data need not be copied from one location to another, although transfers can occur at a rate of 37.5M bytes/s. Transfers are further optimized with the Lisp processor's 4K-word cache memory.

Such an addressing scheme also eases integration of a Unix coprocessor for use as a multi-user front end that packages and sends requests to the Lisp processor. Running concurrently with Lisp, the Unix front end communicates on a process-to-process basis through a defined streams/pipes interfacd. Streams and pipes are generalized I/O interfaces providing virtual circuit capabilities.

Independently of the Lisp processor, the Unix processor can run as a backend processor if users maintain existing Pascal, Fortran,

(continued on page 54)



The SDU receives peripheral service requests from processors residing on Nubus. The unit schedules the necessary actions on Multibus peripherals, and returns the necessary acknowledgments upon completion.

Computer control store

(continued from page 53)

or C programs while using Lisp for the user interface. Lisp software features the Flavors object-oriented programming system (see *Computer Design*, June 1983, p 28) that supports full windowing. Unix runs on a 10-MHz MC68010 with a 4K word cache. The Berkeley Unix enhancements support demand-paged virtual memory with 24-bit addressing.

System diagnostics

The SDU automatically handles configuration and maintenance. Rather than configure the Lambda computer with DIP switches or jumpers, the SDU dynamically senses the devices installed on the 21-slot backplane (13 for Nubus, five for Multibus, and three for either). To take advantage of hardware capabilities, it also simultaneously adjusts system operations. Diagnostics are run concurrently with regular program execution by the 8088 processor. Moreover, faulty peripherals are taken out of service without adversely affecting the rest of the system.

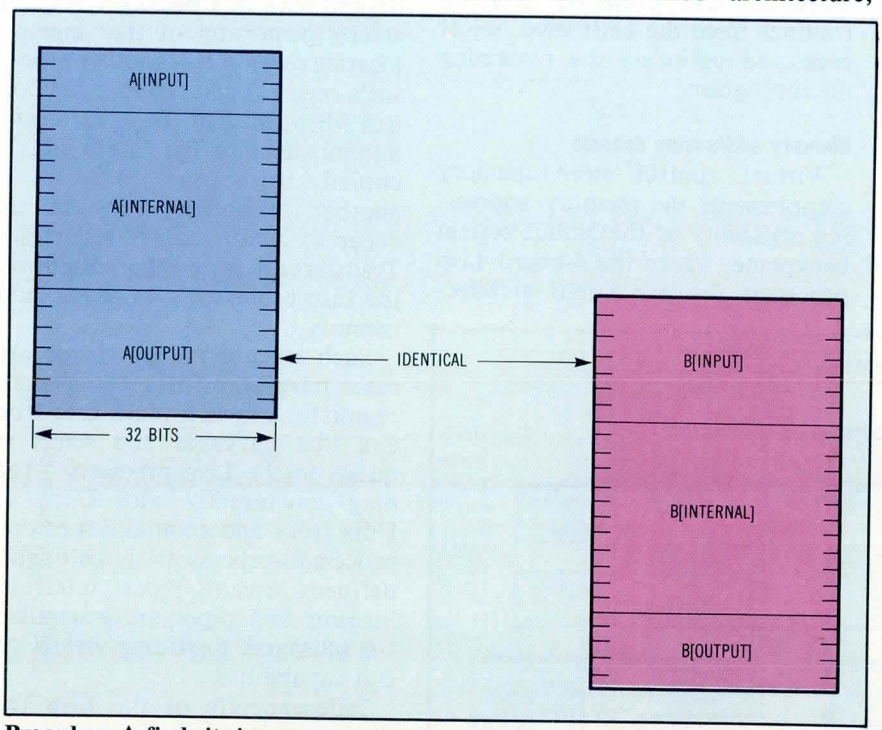
The SDU links the 32-bit Nubus and Multibus peripherals, including disk drives and printers. All requests from Nubus processors for peripheral services are routed through the SDU. This scheme allows the Lambda to benefit from the range of Multibus peripherals available without being limited to the Multibus's slower speed. In addition to the 8088-based supervisory processor, the SDU contains two RS-232 serial I/O ports and a quarter-inch streaming tape drive controller.

A $72,500 single-unit Lambda computer includes a 256K x 32-bit main memory with error correction, one 470M-byte storage module drive (SMD) type disk drive (the SMD disk controller can handle four drives), a 16 x 16 matrix multiplier, and an 800- x 1024-pixel black and white display with mouse. Delivery is quoted at 8 to 12 weeks. A 40-bit version with 32-bit floating point arithmetic and 21.5G-byte virtual address space is expected early next year. **Lisp Machine, Inc,** 3916 S Sepulveda Blvd, Culver City, CA 90230.

Circle 243

Cutting instruction set builds CPU speed

Reduced instruction set computer (RISC) architectures developed at the University of California, Berkeley promise more speed and better function than the traditional, more complicated system architectures. A commercially available machine based on the RISC architecture, Pyramid 90x from Pyramid Technology is a 32-bit superminicomputer whose proprietary CPU includes a register-intensive instruction set with provisions for passing parameters. The 125-ns CPU is implemented in TTL on three PC boards and includes 528 registers, in contrast to the 8 to 32 registers included in other minicomputer architectures. These registers are used to pass parameters from one procedure to another, instead of going through memory, storing, and reloading values.



Procedure A finds its input parameters in a set of CPU registers (A[Input]), uses a block of registers for its internal operations (A[Internal]), and passes parameters to procedure B via another set of registers (A[Output]). When Procedure B begins execution, its input parameter registers (B[Input]) are identical to A[Output].

In this scheme, a procedure receives input parameters from one or more registers in the CPU, uses the next several sequential registers for its own internal operations, and passes parameters to subsequent procedures in one or more higher-numbered registers (see Figure). A procedure can, if necessary, pass values back to its calling procedure via the input registers.

Traditional architectures produce a procedure call (a change from executing one procedure to another) by storing input and output parameters in memory or on a hardware stack. While this mechanism does work

(continued on page 56)

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Cutting instruction

(continued from page 54)

satisfactorily for simple computers with low clock speeds, it presents a problem for high performance, multi-user systems.

At clock speeds of 8 MHz or more, the system bus acts like a transmission line. Line capacitance however, can delay signals by a small, but significant amount, over and above the time needed for the signal to travel the length of the line (approx 1 ns/foot). Even fast (100-ns) memories take a finite time to return data when addressed. All of these times must be summed to find the effective memory speed and can total an appreciable fraction of a microsecond.

The RISC register windowing scheme avoids these delays, since the parameters are not stored in memory, and signals travel only a few tens of microns onchip. A procedure call, which is the most common operation in programs written in high level languages, thus becomes extremely fast.

In addition to register windowing, the Pyramid 90x has virtual memory, and thereby simulates more memory than is physically present. With its fast instruction cache and intelligent I/O processors, the CPU handles only computational tasks, not I/O. The system bus is synchronous and has a bandwidth of 32M bytes/s. It can accept the CPU, one to four memory modules (2M bytes max), the 68000-based system support processor (handling system control and diagnostics), multiple I/O processors, and a Multibus adapter.

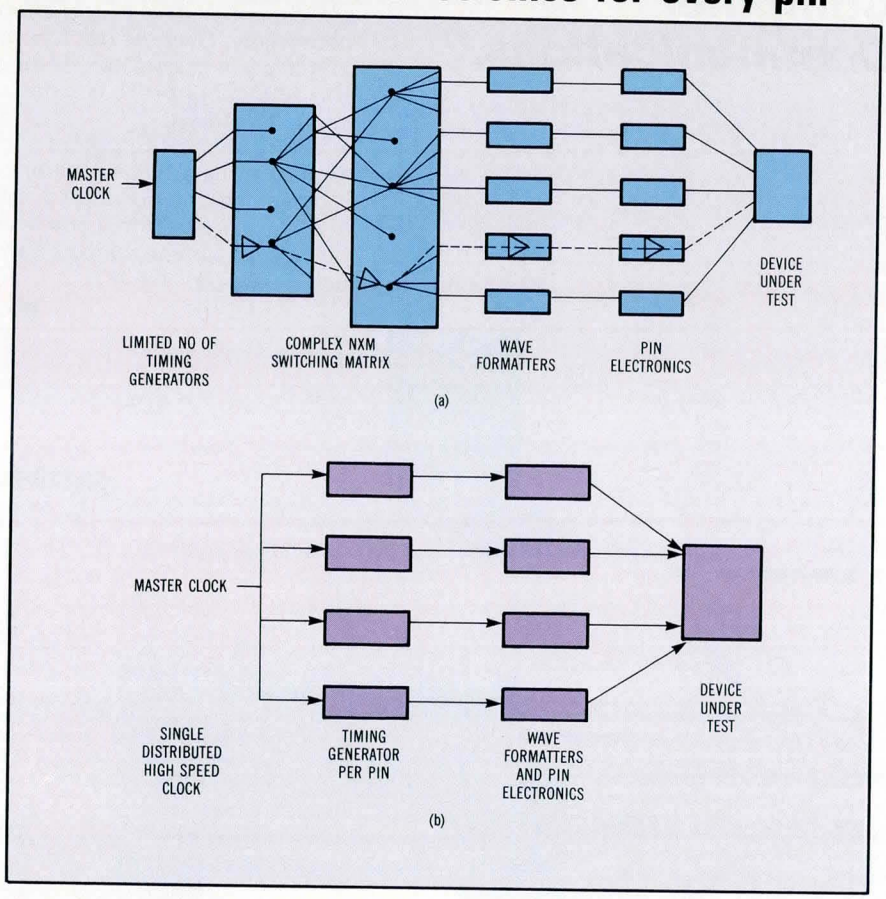
Unix System V, with Berkeley enhancements as well as proprietary features, is used as the supermini's operating system. Each Unix process can address a 4G-byte address space and is supported by demand paging in 2K-byte increments. Supported languages are C, Pascal, and Fortran 77; Cobol is scheduled for availability in 1984.

Pyramid 90x system prices range from under $100,000 to over $300,000, depending on configuration. **Pyramid Technology Corp,** 1295 Charleston Rd, Mountain View, CA 94043.

Circle 244

TEST & MEASUREMENT

VLSI tester has test electronics for every pin



The cumbersome switching matrix of shared resource testers (a) introduces timing errors and requires programming at a low hardware level. The tester-part-pin architecture (b) allows precise calibration of all timing and can be programmed at a high level with user-defined variables and labels.

Tester-per-pin architecture attacks the increasingly complex task of testing VLSI device functions. Megatest Corp's MegaOne VLSI test system dedicates a complete set of testing electronics to every pin of the device under test. An integral 32-bit computer controls all this and allows tests to be developed offline using high level languages.

The complexity and speed of VLSI circuitry has made the testing of VLSI devices primarily a software problem. This has come about because of the time and effort needed to develop comprehensive test programs for the wide range of functions now being used in VLSI.

Using the "throwing hardware at the software problem" approach has resulted in a tester-per-pin architecture that alleviates many of the problems inherent in shared-resource tester architectures. Fundamental to the MegaOne scheme is a complete set of dedicated test electronics for every pin on the device under test (DUT). This includes an independent timing generator, wave formatter, and vector memory. It allows independent setting of high and low drive levels, high and low comparator levels, direct current (dc) parametrics, and current loads for each pin.

Simpler test methods for VLSI functions

The tester-per-pin approach brings with it many ramifications affecting software development. For one thing, test engineers no longer need

(continued on page 59)

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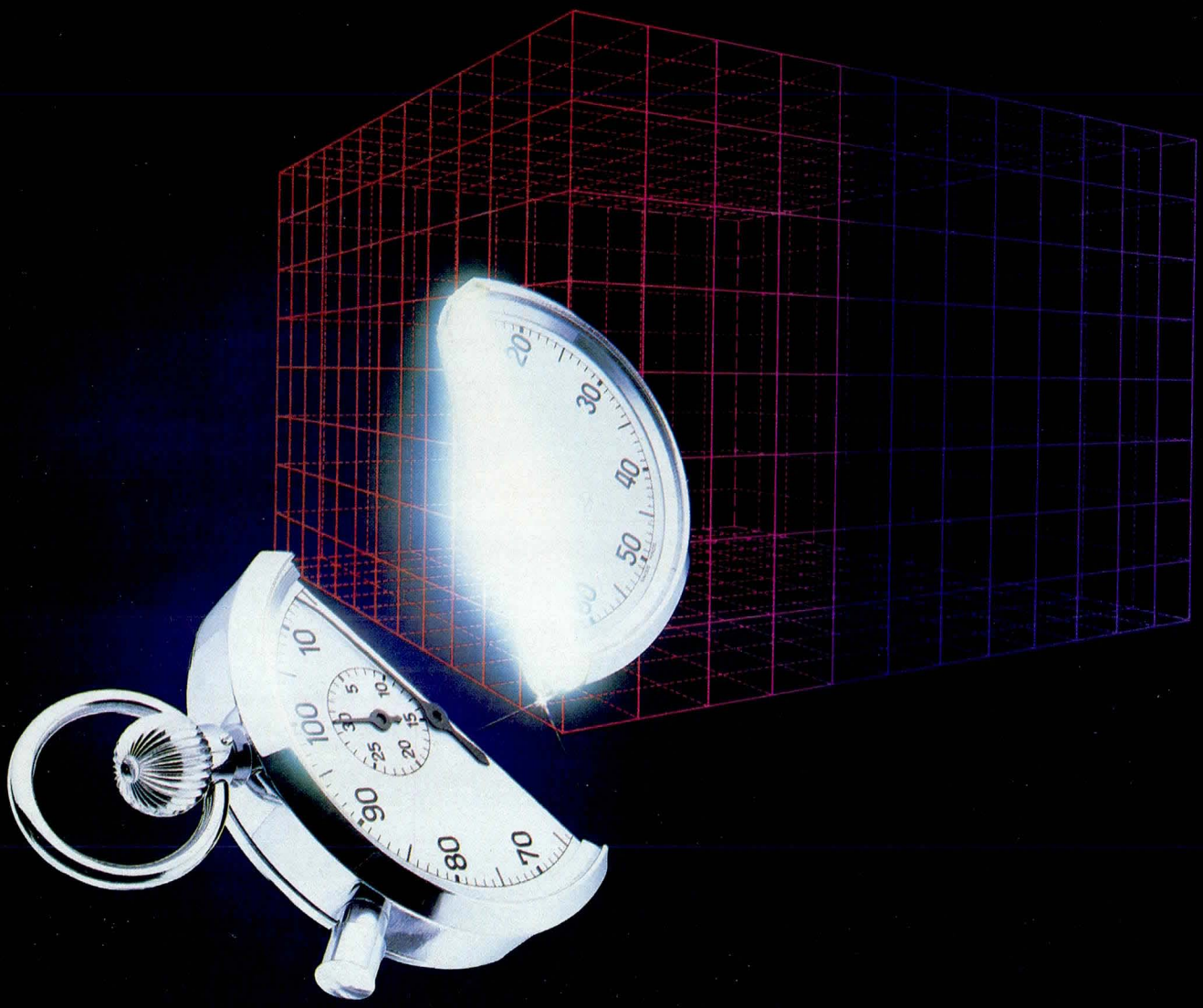

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VLSI tester

(continued from page 56)

think of their task in terms of low level tester terms (registers, etc), but in relation to test functions—ie, waveforms and parameters. The abundance of test resources means engineers no longer have to manage limited tester resources and make compromises between test completeness and test length.

This architecture also does away with the internal switching matrix used in multiplexing a limited number of shared resources. It eliminates timing errors that occur in the complex matrix as the pin count goes up. As a result, the test engineer/programmer no longer need be concerned with deskewing the timing to compensate for the different lengths of signal paths caused by the switching matrix.

In fact, the master clock is the only high speed signal that need to be distributed throughout the system. It is bussed in parallel and used as the reference by the dedicated timing generators. Each pin has a timing generator that produces three edges per vector. Positioning resolution per pin is 100 ps while overall system resolution is 700 ps.

The high speed controller produces a 40-MHz master clock signal. By pairing waveform generators on a pin-by-pin basis, however, the controller can achieve an 80-MHz operation when needed. The controller is transparent to users but has a 3M-byte onboard control store to take care of parallel parametric tests, timing and level searches, and routine autocalibration.

An autocalibration circuit standardizes all timings at all possible edge positions. The "autocal" uses time domain reflectometry to null fixturing delays. Routine autocalibration of a DUT interface board change takes 30 s to perform; full system calibration from a cold start requires 5 min.

Other advantages gained by tester-per-pin architecture are higher bandwidth and accuracy. Since signal paths are dedicated instead of switched, the system can precalibrate every possible timing per pin rather than relying on deskewing only the average error for a given signal path. Systems are also easier to repair and upgrade; pin count can be increased modularly, thereby making conceivable systems exceeding 512 pins.

Besides the high speed controller shared by the system as a whole, certain other resources are available for each test head. One of these is the Parametric Measurement Unit (PMU). The PMU provides accurate monitoring of force voltages, and current and temperature. It also supplies information for autocalibration and the DUT power supplies.

Since the overall design philosophy of the MegaOne is to provide a sufficiently rich hardware environment for solving testing problems with high level software, a 32-bit 68010-based computer has been integrated into the system. The computer not only controls the per-pin testers for up to three DUTs at once, it also provides program development environments via the Unix operating system. This results in a great deal of test program development that takes place offline. Up to 16 terminals can be used without degrading system throughput while at the same time running up to three test heads in production testing. For final device characterization and debug, the programmer would use one of the three test heads; up until that time, however, all three could be used for production work.

Hardware and software combined

Megatest provides a standard Pascal compiler (Berkeley Pascal 2.0) and a Vector Programming Language (VPL) for writing the test patterns. VPL is a block-structured language with all instructions expressed in device data sheet nomenclature. For debugging, the system provides multiple window screens to simultaneously examine program values, timing, and source code, etc. Changes can be made interactively in a program using the system that mixes compiled and interpretive code. Thus, there is no need to recompile the program to

(continued on page 60)

VLSI tester

(continued from page 59)

test small changes. All such interactions take place at the Pascal source code level using the programmer's own variable names and labels. No reference to actual tester hardware is necessary.

Usually, the greater part of a test program can be written using the computer-aided program generation tools by answering a series of questions about the DUT. This process outputs a standard Pascal test program. VPL can translate almost any arbitrary test pattern into the system format. In addition, the system provides on line documentation to check command syntax and definitions. The documentation can be called up in screen windows and consulted next to the program code or other information in question. MegaOne is initially priced at $1 million. **Megatest Corp,** 3940 Freedom Circle, Santa Clara, CA 95050.

—Tom Williams
West Coast Managing Editor

Circle 245

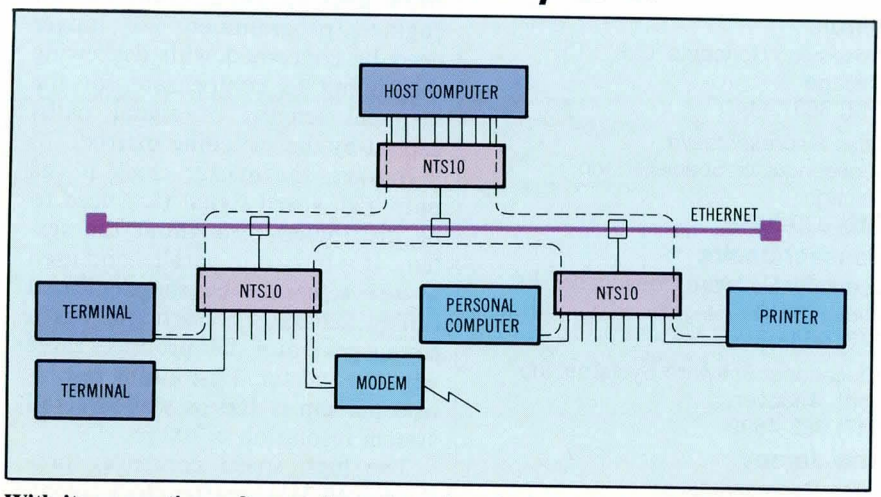
DATA COMMUNICATIONS

Networking hardware and software connect unlike systems

Terminals, mini and mainframe computer ports, personal computers, printers, and modems connect to Ethernet through the NTS10 terminal server. With additional software packages, personal computer users can access a wide variety of data processing resources available on the network. This not only allows information sharing among personal computers and the mainframe data base, but also resolves long-standing distributed environment problems.

The NTS10 interfaces any asynchronous EIA RS-232-C serial I/O device to the Ethernet/IEEE 802.3 local area network. Interlan's unit provides a virtual circuit communication service that interconnects equipment. Although the virtual circuits appear as direct physical connections between devices, protocol procedures in the NTS10 electronically create and terminate them.

In addition, the protocols resolve device incompatibilities (eg, a 1200-baud terminal can be connected to a 9600-baud computer port). The NTS10 contains either four or eight ports. Large clusters of devices can be attached to the network by daisy chaining up to four units (32 ports) to share a common transceiver connection to the Ethernet. The Ethernet terminal server offers several advantages including port switching, port contention resolution, resource sharing, personal computer networking, and simplified wiring for dispersed terminals and printers.



With its supporting software, the NTS10 solves the information sharing problem between personal computers and the corporate data base. It also eliminates the distributed environment problem of terminal access to several host computers and a variety of peripherals.

By issuing a CALL command, any computer on the network can be accessed. If computer ports are busy, the NTS10 searches for an open port or waits for the first available port. In addition, because the virtual circuits overcome device incompatibilities, users can share resources such as modems, printers, plotters, and statistical multiplexers.

For installations with personal computers, the NTS10 interconnects personal computers from different vendors, or connects them to the host computer or other devices. The associated networking software permits easy file transfer and RS-232 device access.

Networking software for 12 different personal computers is available in two separate functional packages: poly-TRM for terminal emulation, and poly-XFR for file transfer. Poly-TRM effectively converts a personal computer into a terminal. Once a connection is made from the personal computer to the target device through the NTS10, the personal computer appears to the user as a terminal directly connected to the device.

Moreover, the software package can transmit and receive ASCII text files without any special software running at the other end of the virtual connection. Poly-XFR provides transfer of binary and ASCII files over Ethernet. With this package, user commands establish an NTS10 virtual circuit to the host, perform log on, invoke execution of the host

(continued on page 62)

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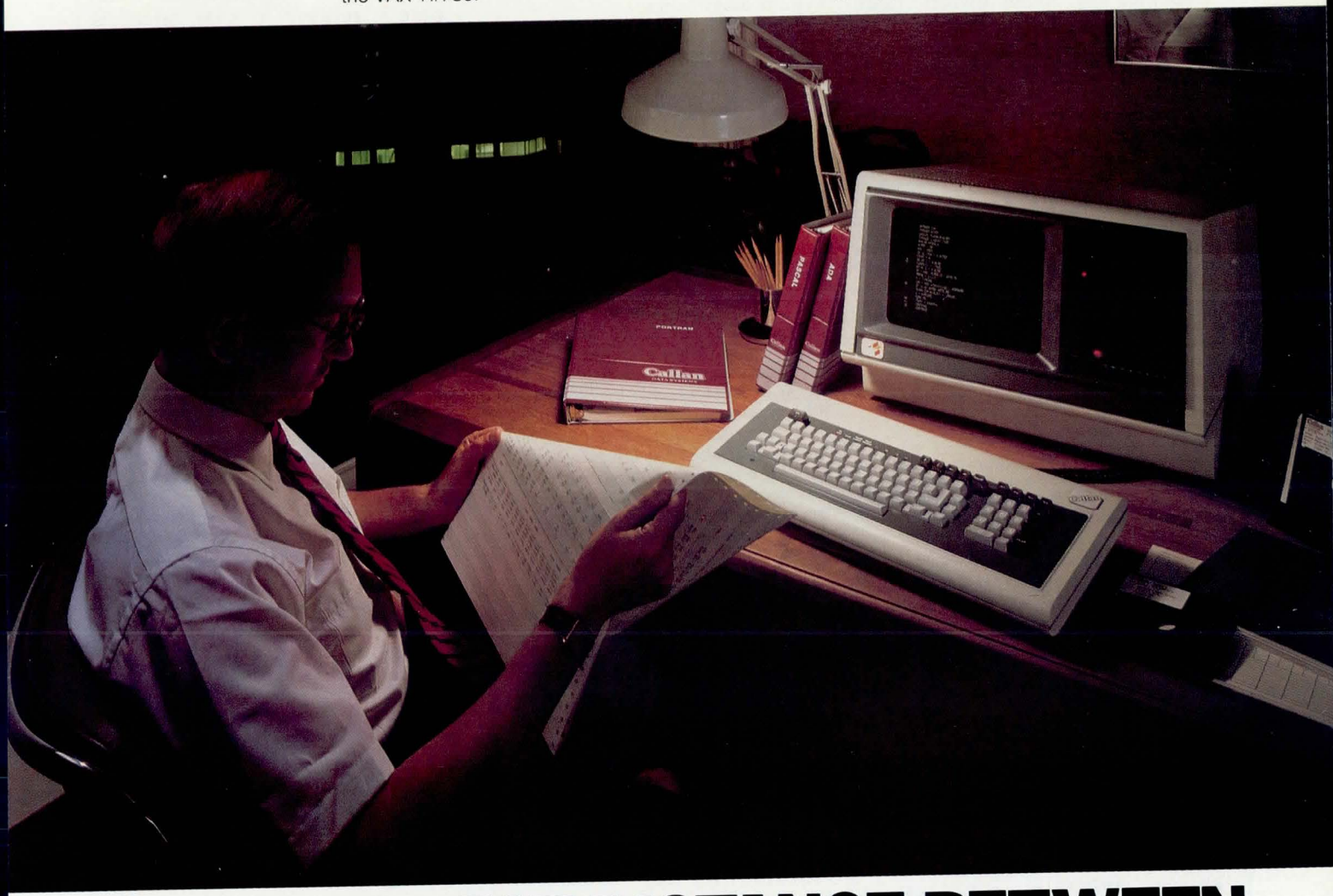

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CIRCLE 35

Networking hardware/software

(continued from page 60)

computer's poly-XFR software, and initiate the file transfer program.

The terminal server and software provide network management, which establishes the control necessary for network integrity. For example, the NTS10 divides users into two classes: ordinary users, and network managers who are responsible for configuring the network and limiting connection access. Network managers can also designate permanent virtual circuits and run system diagnostics.

Each device can be assigned two different logical names, and multiple devices can have the same logical name. Programmable passwords protect against unauthorized connections or reconfigurations. Software is resident in RAM, which is downline loaded from another device. However, each NTS10 stores its own configuration parameters in electrically alterable ROM. This eliminates the need for a central file system. **Interlan, Inc**, 3 Lyberty Way, Westford, MA 01886.

—John Bond, Senior Editor

Circle 246

Controller plugs into different networks

Plug-in communication adapters on the Easyway network controller from Able Computer simplify the task of supporting different networking schemes on a DEC PDP-11 or VAX computer. While the host interface remains constant, the electrical interface needed to support Ethernet can be easily changed to that required for token passing, X.25 packet switching, or IBM SNA type communications.

This approach isolates the host computer from dependencies imposed at the physical and link layers of the International Standards Organization/Open Systems Interconnect (ISO/OSI) network model (layers 1 and 2). Software intensive functions, such as message routing and data checking, are also offloaded from the host to the controller, since Easyway handles the network and transport layers (layers 3 and 4).

As a result, the host computer does not see the significant data arbitration involved in transferring information across networks. Users need only provide source and destination addresses. All that is visible to VAX/VMS or RSX-11M/S operating systems are a series of DMA transfers across Unibus, between the host and the network controller via dual

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CIRCLE 36

ported memory (64K words x 22 bits with error correction). A common software driver, Connect, coordinates communications for different applications and passes data formats transparently to the Easyway controller. The combined controller and software driver provides protocol independence.

On the network controller, protocol independence is achieved using the standard IEEE 802 handshaking scheme between host and communication adapters. Regardless of the electrical interface used to communicate with other networks, data are passed between the host and communication adapter in the same manner. Users supply connection to the external world through a transceiver that connects to Ethernet or other networks.

Both the communication and host adapters occupy a single hex-width board on any DD11 Unibus backplane configured for DMA operation. A transceiver interface cable is also supplied with the Ethernet version to connect the user-supplied transceiver.

Initial Easyway controllers are priced at $5000 with delivery 30 days ARO. The Connect software driver is available 60 days ARO for $1000. **Able Computer**, 1732 Reynolds Ave, Irvine, CA 92714.
Circle 247

SYSTEM TECHNOLOGY
(continued on page 66)

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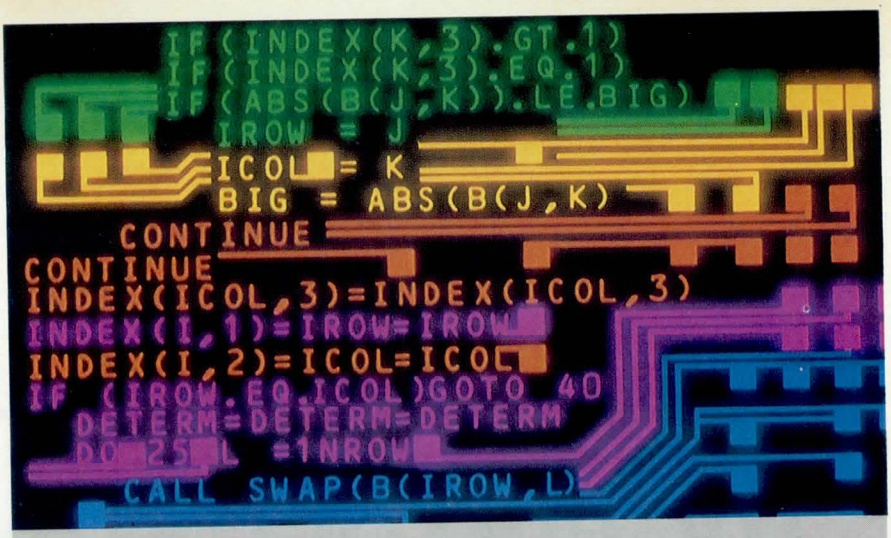

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CIRCLE 37

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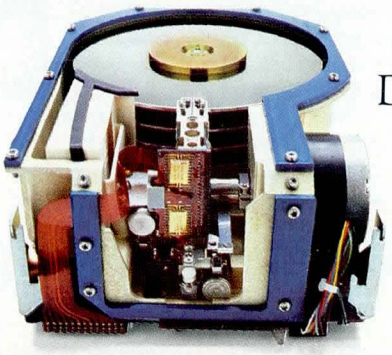

But thin-film media isn't the only reason to buy Evotek drives. With capacities up to 51.68 MB, they have such advanced features as high-torque precision motors. Superior brake force. Six-bearing linear actuator with a 49 ms average access time. Even an on-board microprocessor.

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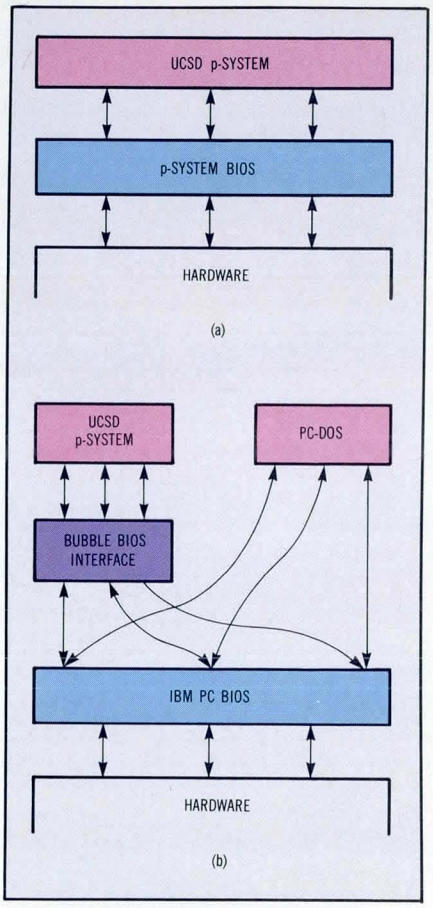
Piggybacked operating systems add flexibility



Standard microcomputer operating systems interface with computer hardware directly through an assembly language BIOS (a). Datalex has substituted a special routine in the PC-DOS bubble to interface the p-System to the normal PC-DOS (b), thereby providing both the p-System and PC-DOS the same functions.

System programming, at least on microcomputers, is no longer a mysterious art. Running one operating system from within another (piggybacking) offers the freedom to manipulate files of either. Datalex's PC-DOS Bubble software operates the UCSD p-System from within an IBM PC-DOS environment to make languages running under both systems available. Under the Bubble, both p-System and PC-DOS files and disks can be read or written, PC-DOS primitives can be invoked from the p-System, and/or a mix of programs can be run without rebooting or leaving PC-DOS.

Operating systems usually have exclusive control of the machines that they run on and manage the available physical resources. The application programmer can then concentrate on program logic and functions, without having to delineate control of I/O ports or placement of drive heads to find a file.

Providing a link

Traditionally, operating systems are written in assembly language for a particular hardware configuration, then tediously recoded for transportation to other machines when necessary. In the absence of common standards for disk formats, directories, or function calls, developers have produced wildly incompatible ways of doing essentially the same thing. A common thread among microcomputer operating systems, in contrast to those for mainframes and minicomputers, exists in the creation of a Basic I/O System (BIOS). This set of machine-specific assembly language routines is called from the main body of the operating system to handle I/O details [Figure (a)].

Splitting machine-dependent parts of the operating system from the more general parts allows both CP/M and the UCSD p-System to be transported to machines made by different manufacturers. With p-System, the use of assembly language interpreters to execute the pseudocode (p-code) produced by the systems' Pascal, Fortran, and Basic compilers allows it to be transported to a range of architectures, from MOS Technology's 6502 to DEC's PDP-11. Neither BIOS routines nor interpreters, however, address file system or disk format incompatibilities.

If all operating systems were equal, providing the same functions and programs, file transfer utilities would be the answer. Different operating systems, however, and the different languages they offer, attract very different type of users. Programs for PC-DOS tend to be

(continued on page 68)

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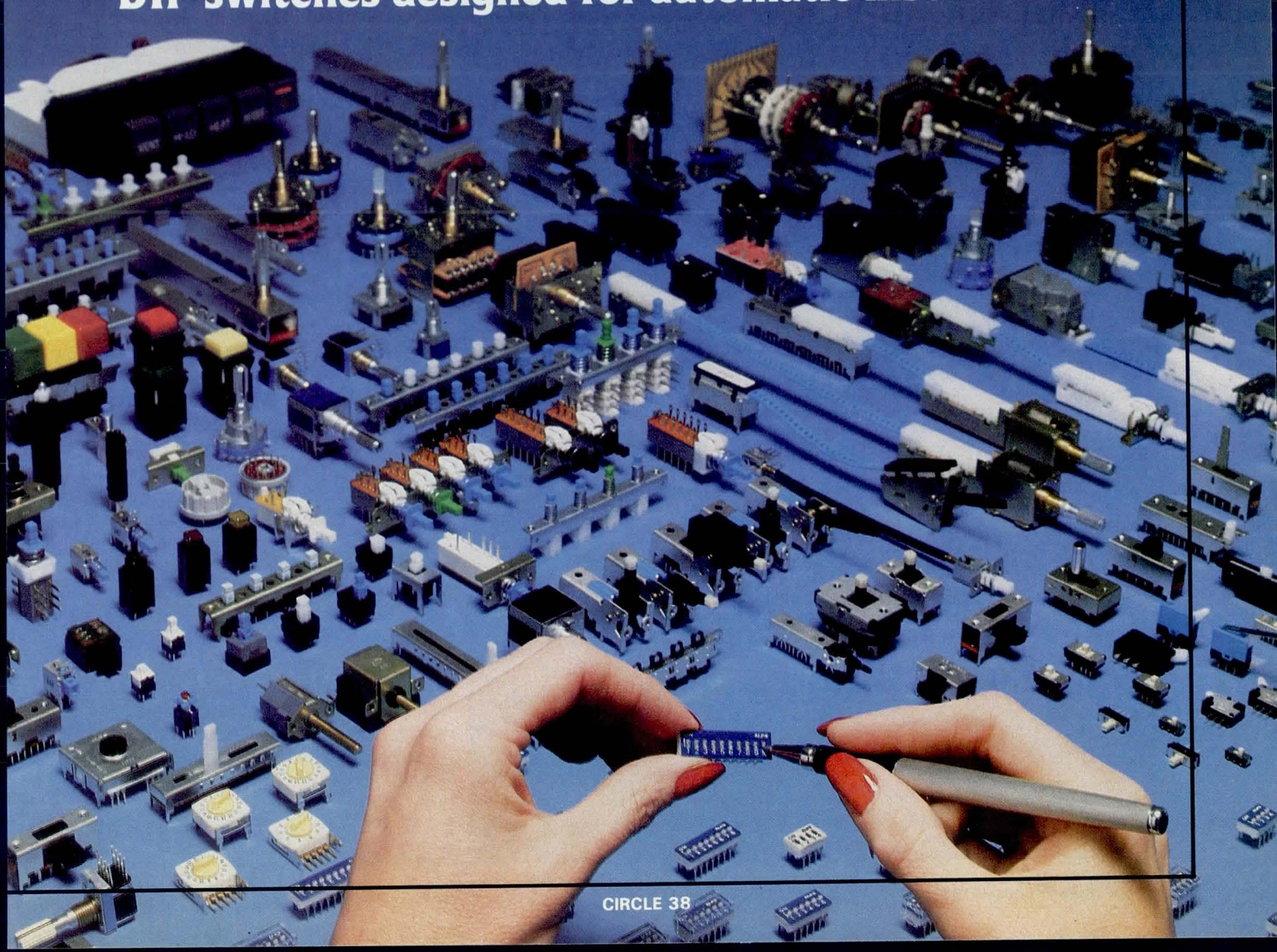
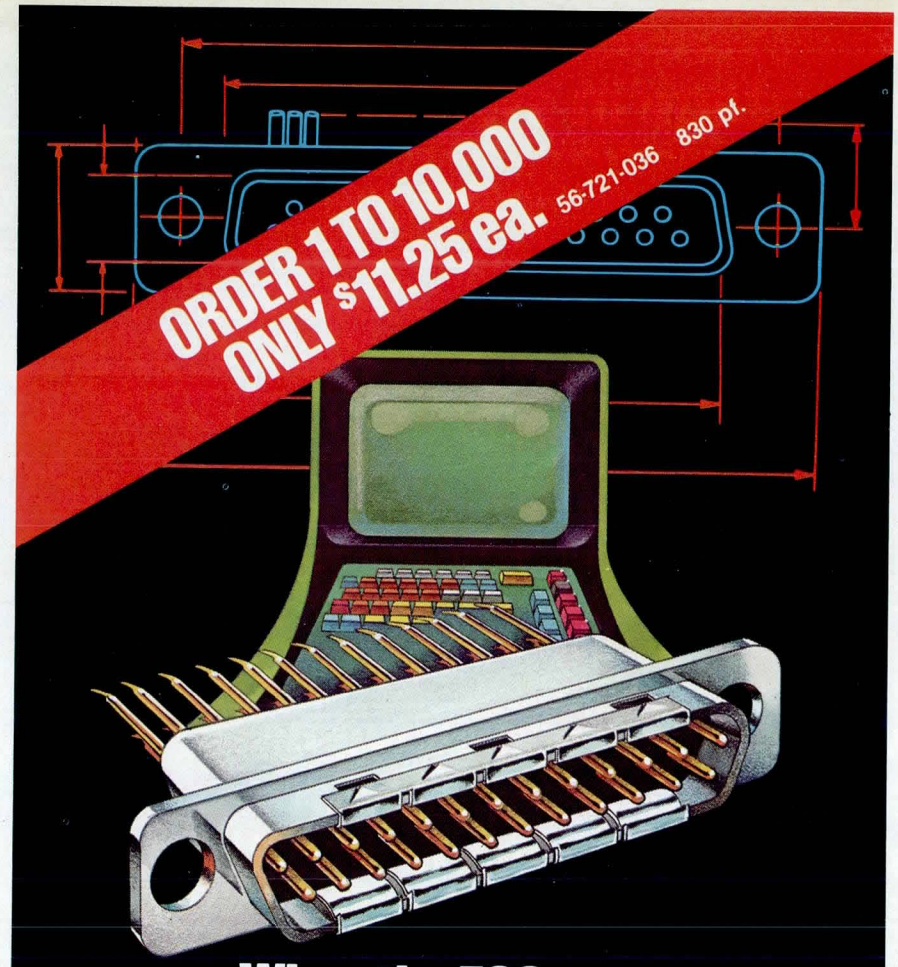


CIRCLE 38



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SYSTEM TECHNOLOGY/ SOFTWARE

Piggybacked operating systems

(continued from page 66)

written in Basic or assembly language, while p-System programs are almost exclusively in the more structured Pascal.

Tying it together

The combined p-System/PC-DOS Bubble conveniently and directly ties the power and portability of the p-System to the extensive PC-DOS software packages and to industry common devices such as hard disks and communication cards. The Bubble is started by selecting an executable file named PSYSTEM from the PC-DOS command prompt. The p-System interpreter is then loaded into memory, files and values are configured, and the normal p-System prompt line is displayed. The Bubble can be terminated from the p-System command level with the HALT command, or a PC-DOS function call can be generated via an included utility.

A set of assembly language routines that access the PC-DOS BIOS replace the normal p-System BIOS (Figure (b)). In addition to remapping the BIOS, changes have also been made in the p-System file manipulation utility to display both the PC-DOS files and a RAMDISK utility. This utility allows unused memory in the IBM PC to mimic a very fast (but volatile) disk drive.

Datalex distributes the Bubble directly through OEMs and provides it to software distributors so that their p-System software can run transparently on the IBM PC. Development is also in progress on a version of the Bubble for CP/M-86 and MS-DOS.

When included with a complete p-System, the Bubble is available for $850 from PCD Systems, 163 Main St, PO Box 143, Penn Yan, NY 14527. As a separate product (without the p-System) it is $200. The OEM price for inclusion in single-user systems ranges downward from $24. **The Datalex Company,** 650 Fifth St, San Francisco, CA 94107.

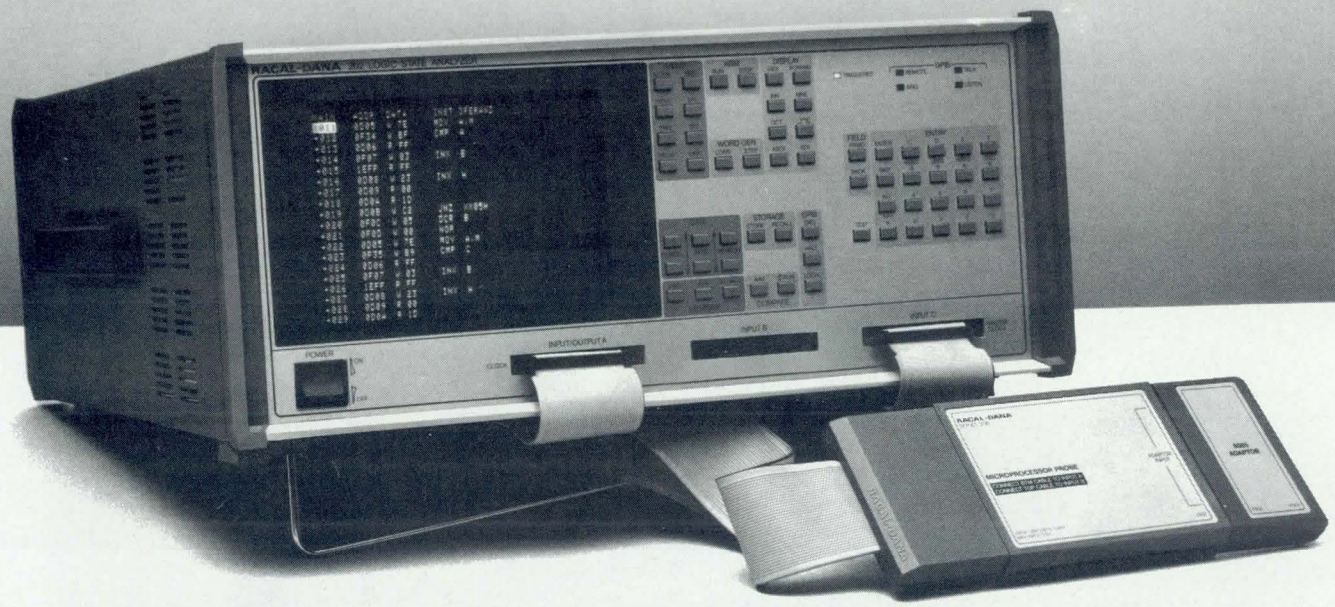
—Sam Bassett, Field Editor

Circle 248

CIRCLE 39

RACAL-DANA SERIES 200 μP ANALYZERS

μP SOFTWARE DEBUGGING?



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CIRCLE 40

Motorola's virtual memory 16-
mainframe capabilities for

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The MC68010 fully supports virtual memory/virtual machine/virtual I/O techniques in microprocessor based systems. This allows a system to operate as if it has many times the amount of physical memory it actually has, and makes it tolerant of faults.

Faults on any bus cycle can suspend any instruction and begin a controlled correction. The MC68010 doesn't try to predict faults; it responds to them intelligently. No segmented architecture offers these features.

The MC68010 tolerates failures of memory cards to make proper transfers, cleanly, regardless of cause.

It handles faults caused by hardware failure and the software protection faults that a memory manager finds.

MC68010 systems don't care whether faults are due to protection violation, non-existent memory, circuit failure, bad RAM or a watchdog timer. Even memory errors during important operating system procedures are tolerated routinely.

The MC68010 provides capabilities that once were confined to mainframe and minicomputer systems, and extends the leadership characteristics which have made the MC68000 so popular in new designs.

Applications programmers should love the MC68010.

Applications programmers don't have to code around, or even know about memory management. That's handled by the operating system. Many memory management techniques can be implemented, including demand paging, to make the bank-switching schemes of segmented architectures obsolete.

And, don't forget the MC68010 gives you the same 16 megabyte linear memory space as the MC68000.

For systems designed with error detection and correction (EDAC), the MC68010 helps you improve the design of systems with slower memories.

Enhanced instruction timing results in execution of MC68000 instructions up to 50% faster by the MC68010, at the same clock speed. The MC68010 runs all MC68000 user code identically, so your existing system is upgraded simply by placing the MC68010 in the MC68000 socket.

M68000 Family: 32-bit architecture makes it the only 8/16/32-bit migration path.

From the time the MC68000 was introduced it claimed the leader's mantle. One of the most significant reasons is its 32-bit architecture. It's not an 8-bit architecture stretched to 16, but 32 bits confined to a 16-bit bus. It's now also available in 8-bit form as the MC68008. That's a 32-bit architecture on an 8-bit bus. Full 32-bit power will soon be unleashed in the MC68020. From the MC68000 and MC68010, in both directions to the MC68008 and the MC68020, the M68000 family becomes the very definition of code compatibility . . . the only migration path along the 8/16/32-bit route.

Advanced tools assist fast, accurate system development.

Advanced MC68010 support is provided by the EXORmacs™ system, the first 8-/16-/32-bit multiuser development system, and by the new

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When you need a variety of logic analysis and system performance histogram features, the Bus State Analyzer adapts to the MC68010 through a unique personality module.

Basic and C will soon be offered with existing Pascal and Fortran compliers, and symbolic debug is available. A broad and rapidly expanding base of development and applications software also is available from independent, third-party vendors.

M68000 family peripherals, memories, discretes, linear and logic meet your broad system needs.

M68000 MPUs are supported by a growing family of Motorola-developed peripherals. Contributions from our worldwide major second sources are adding even greater breadth and depth to the family.

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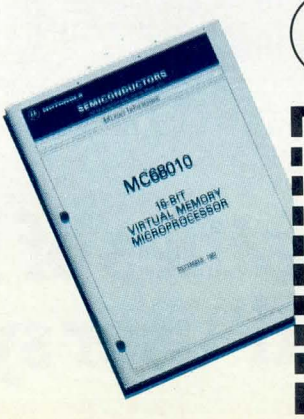
For direct M68000 Family assistance, call your local Motorola office or distributor. For information on the MC68010, send to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix AZ 85036.



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And wins the battles of ISIS-II, CP/M-86, and multi-user systems, too!

The battle of the Multibus Giants goes on!
And Zendex (you may call us "The Little Giant") continues to win. For you.

A complete RMX-86 Development Environment.

There are three ways to develop RMX-86 application software for MULTIBUS target systems.

Two of them have problems. The third is Zendex.

Zendex makes it easy to develop software for RMX-86 board level applications.

And just as easy to get this software into firmware for the target system.

In today's technology, the two best-known RMX development systems make very little sense.

You can go on using the Intel Microcomputer Development System Approach, with MDX, Series II, III or IV.

Or the Intel SYS 86/380 and SYS 86/330 OEM Microcomputer System Approach.

You may *enjoy* buying extra equipment, developing additional software, spending up to four times the money (especially for single-user systems when your project has several engineers).

You may not mind debugging problems, PROM programming limitations.

Or maybe you just like doing things the same old way.

Much better, buy an RMX-86 system and complete software development environment from Zendex.

Here's how you'll benefit:

1. More Hardware Features at Lower Cost:

	Zendex 95/86A	Zendex 95/86W	Intel 86/330	Intel 86/380
Open card slots	5	6	2	11
Open drive slots	1	1	0	1
RAM	512KB	512KB	384KB	384KB
Floppy	1MB	500KB	1MB	1MB
Winchester	42MB	10MB	35MB	35MB
Clock/calendar	Yes	No	No	No
Prices	$18,045	$14,245	$23,500	$30,500

2. Soft-Scope, a high level source debugger for RMX-86 compatible PL/M-86, PASCAL-86, FORTRAN-86 and Mark Williams 'C.' It's the best debugger we've seen for any operating system. Featuring:

1) High-level breakpoints;
2) High-level single step;
3) Remote debugging with second terminal;
4) High level trace;
5) Machine disassembly and 8087 floating point support.**

3. PROM Programming Utilities. Let you program inexpensively with Zendex single-board PROM programmers.**

How Zendex Beats "The Giant" in ISIS-II.

If you use ISIS-II, you'll want our Model 835. Fully ISIS and ICE compatible, and only $8,545. ("The Giant's" MDX-225AFD costs $17,500.)

And Zendex offers:

More expansion slots.

A choice of chassis, modular or integrated, rack-mount or tabletop.

Removable cartridge disk drives fully ISIS-compatible, for thousands less than an MDX-750 subsystem.

And it works with your choice of terminals.

How Zendex Beats "The Giant" in CP/M-86.

When you don't need the real-time power of RMX-86, we offer a CP/M-86/*MULTIBUS SYSTEM*. "The Giant" doesn't have it.

ZENDEX CP/M-86 SAVES YOU MONEY. With 128K RAM and 2MB floppy as a minimum configuration, it is ready to go. Less than half the price of "The Giant's" 16-bit MULTIBUS systems.

ZENDEX CP/M-86 IS HIGHLY CONFIGURABLE. Available as integrated system chassis or modular chassis. Rack-mount or tabletop. 128KB, 256KB or 512KB RAM. Parity or ECC. 10MB, 20MB, or 40MB Winchester options.

Compatible with Zendex PROM Programmers, *MULTIBUS* display and *MULTIBUS* tracer.

Zendex even beats "The Giant" in the Series-III.

To expand your Series-III development capability, use the Zendex Universal Development Interface System utility. With 8-inch floppies, compatible with the MDX-286 in single density, it lets you add a new development workstation for under $10,000.

ZENDEX Multi-User Systems:

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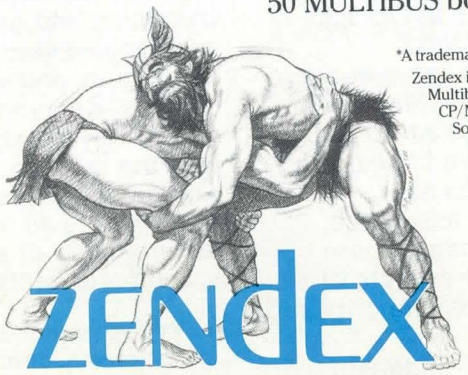
Send for our free catalog featuring more than 50 MULTIBUS boards and systems.



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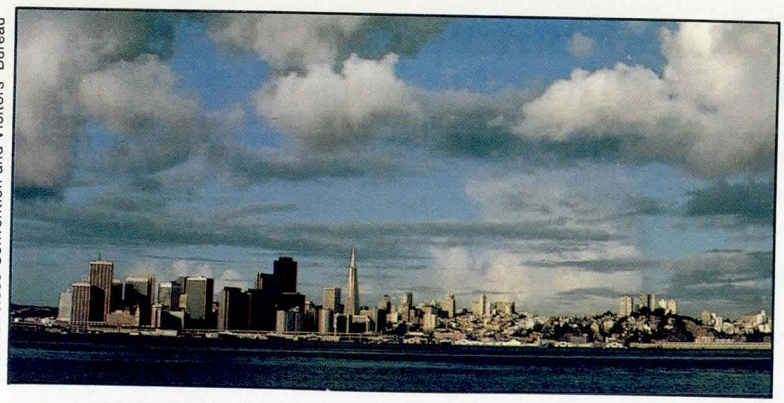


Photo courtesy of San Francisco Convention and Visitors' Bureau

Wescon/83

Mini/Micro West

Moscone Convention Center
Brooks Hall and Civic Auditorium
San Francisco, California
November 8 to 11, 1983

Electronics Show and Computer Conference

Reflecting the rapid growth and expansion within the electronics industry, Wescon/83 will present the largest, most comprehensive show in its 32-year history. More than 900 electronics firms are scheduled as exhibitors, and over 75,000 professionals are expected to fill the convention halls.

Wescon is listed as the nation's largest high tech electronics show, and adding to its attraction this fall will be the concurrent Mini/Micro West-83 convention. As the West Coast's only major computer conference and technical symposium geared directly to OEMs, Mini/Micro West is expected to filter out at least 30,000 attendees from the Wescon show.

Wescon has 35 Professional Program sessions (see p 75) along with four short courses. The tutorial, "Robotics—Research in Business Opportunities" (Nov 8, 9 am to 3:30 pm) will cover current and future robot applications, and how companies can prepare to implement industrial robotics. "The Manager's Perception of Reliability" (Nov 8, 9 am to 3:30 pm) will review reliability through a breakdown of its functional components, such as contractual requirements, quality assurance, design review, and parts control/degradation. The course will stress managerial aspects of understanding and controlling these functions to maximize cost effectiveness.

Communication techniques will be taught during "Strategies for Technical Report Writing" (Nov 11, 9 am to 4 pm). Initiating writing as a planned endeavor for clearer and more quickly completed reports will be discussed through audience analysis, modular format, inductive outline, the communication triad, and executive summary. Finally, "Technical Entrepreneurship: Starting a High Tech Company" (Nov 11, 9 am to 5 pm) will be of interest to both individuals and companies looking to diversify. The course will assess the personal characteristics of successful entrepreneurs, the balance between product/service and the marketplace, cash flow management, and the critical first two years of a business.

Mini/Micro's Professional Program (see p 80) likewise addresses the need of OEMs to keep abreast of the latest innovations in their fields. Pertinent discourses will encompass new micro architectures and solid state software, number crunching and graphics, 16/32-bit microprocessors, high level language, personal computers, and videotex and workstation designs. Keeping OEMs up to date will be the goal set by nearly 100 top clinicians who will lead the sessions of Mini/Micro West-83. Topics will include areas such as local area networks and upper level ISO protocols, peripheral requirements of advanced microprocessors, system architectures, and software.

For registration information, contact Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965; 800/421-6816 (outside Calif)

Photo courtesy of San Francisco Convention and Visitors' Bureau

Wescon/83

Professional Program Excerpts*

Session 1: Integrating CAE Workstations into the Total Design Environment

Tues 9 to 11 am

Chair: G. H. Langeler, Mentor Graphics Corp

1/1 "Tying CAE Workstations into Existing In-house Design Tools—The Tradeoffs"

1/2 "The Impact of CAE Workstations on the Next Generation CAD/CAM Systems"

1/3 "The Value and the Limits of CAE"

1/4 "It's Time for Computer Integrated Engineering"

1/5 "Engineering Workstation for VLSI Design"

Session 2: Developments In VLSI Disk Controllers

Tues 9 to 11 am

Chair: A. Goldberger, Excel Microelectronics

2/1 "ACS 5000 SCSI (SASI) Disk Controller Chip Set"

2/2 "Building a SASA Disk Controller with the NCR VLSI Chip Set"

2/3 "An Intelligent Hard and Floppy Disk Controller for the M68000 Family"

2/4 "LSI Controller for 5¼" Winchester Disk Drives"

Session 4: Can Systems, PC Board, and IC Design Engineers All Use Engineering Workstations?

Tues 12:30 to 2:30 pm

Chair: D. Laughlin, CAE Systems, Inc

4/1 "Defining the Problem and the Solution"

4/2 "Integrating IC Design into a Systems Environment"

4/3 "PC Board CAD Requirements"

4/4 "Designing ICs with an EWS"

4/5 "Logic Simulation on an EWS"

Session 5: New VLSI Solutions for Winchester Disk Control

Tues 12:30 to 2:30 pm

Chair: M. Herman, Standard Microsystems Corp

5/1 "A new VLSI Hard/Floppy Disk Controller"

5/2 "An LSI Solution to the Hard Disk Controller: UPD7261"

5/3 "LSI Control for SMD Drives"

5/4 "A High Performance Disk Data Controller"

Session 8: Low Cost Networks and Their Impact on System Architecture

Tues 3:30 to 5:30 pm

Chair: R. Dahlberg, Intel Corp

8/1 "Realizing Serial Backplanes: Tradeoffs between Centralized and Distributed Network Control"

8/2 "A Low Cost Peripheral Interface for the Workstation Environment"

8/3 "Low Cost Multiple Access Networks Realized by a High Performance Microcontroller"

8/4 "High Performance Microcontroller Provides Local Intelligence and Manages Interface to a Fast Serial Network"

Session 9: Electromagnetic Interference and Government Regulations—How to Cope

Tues 3:30 to 5:30 pm

Chair: J. J. Reilly, Electro-Kinetic Systems, Inc

9/1 "FCC Regulation Update"

9/2 "Designing Business Machines for Optimal emc Capability"

9/3 "EMI Shielding Techniques for Plastic Packages"

9/4 "The ABCs of Good Design for rfi Shielding"

Session 11: Recent Applications in Voice Technology

Wed 9 to 11 am

Chair: J. Johnson, Votan

11/1 "Human Engineered Robot for the Home"

11/2 "Interactive Application Programming without a Keyboard"

11/3 "Integrating a Voice System with Your Phone and LAN"

11/4 "Incorporating Voice in the Microcomputer Environment"

(continued on page 76)

*Professional Program sessions are subject to last-minute changes.

(continued from page 75)

Session 12: LSI Modem Integration

Wed 9 to 11 am

Chair: S. J. Durham, Cermetek Microelectronics, Inc

12/1 "Get Top Performance with Single-Chip P^2CMOS Modems"

12/2 "Intelligent 212A-Type Modem Integration"

12/3 "CMOS LSI Modem Technology Enhances the Role of the Digital PBX"

12/4 "1200-bps Modem Application"

12/5 "High Speed Short Haul Single-Chip Modems"

Session 13: New CAD Tools for Programmable Logic

Wed 12:30 to 2:30 pm

Chair: V. J. Coli, Monolithic Memories, Inc

13/1 "A CAD Environment for Logic Design"

13/2 "Testing Algorithms for LSI PALS"

13/3 "A Programmable Logic CAD Station"

13/4 "Second-Generation PAL Programmers"

13/5 "A Universal Approach to Programming and Functional Testing of Programmable Logic Devices"

Session 14: Applications of Machine Vision in Electronics

Wed 12:30 to 2:30 pm

Chair: J. E. Trombly, Octek, Inc

14/1 "Machine Vision Technology Primer"

14/2 "Automated Visual Inspection of Keyboards"

14/3 "A Pattern Recognition System for Automated Wafer Alignment"

14/4 "Managing Complexity in Vision Based Systems"

Session 15: VLSI Simplifies Customer Access to the ISDN

Wed 12:30 to 2:30 pm

Chair: C. Stevens, Intel Corp

15/1 "Advanced Generation Integrated SLIC"

15/2 "Partitioning Digital Telecommunications Systems for Implementation in Silicon"

15/3 "The Impact of CMOS LSI on Voice and Data Networks"

15/4 "Advanced Telecom Products Support"

Session 16: New Tools for Designing with Programmable Logic

Wed 3:30 to 5:30 pm

Chair: S. Walters, Valley Data Sciences

16/1 "Computer Based Functional Test Grading of Programmable Logic"

16/2 "A Universal Approach to the Programmable Logic Revolution"

16/3 "Programmable Logic Workstation for Programmable Logic Devices"

16/4 "Test Vector Generation for Programmable Logic Devices"

16/5 "System Advantages of Programmable Logic"

Session 17: Controlling Static Electricity Damage to Microprocessors

Wed 3:30 to 5:30 pm

Chair: G. A. Mellevold, Eldon Industries, Inc

17/1 "Preventing Static Electricity Damage in Assembly and Repair"

17/2 "Preventing Static Electricity Damage in Handling, Shipping, and Storage"

17/3 "Military Requirements for Controlling Static Electricity Damage to Microprocessors"

17/4 "An Overview of the Static Electricity Problems and Solutions"

Session 18: Alternative Approaches to Digital Signal Processing

Wed 3:30 to 5:30 pm

Chair: T. Dintersmith, Analog Devices, Inc

18/1 "DSP Building Blocks Allow Resource Optimization"

18/2 "Building a Digital Signal Processing System around CMOS Parts"

18/3 "A Single-Chip Approach to Digital Signal Processing"

18/4 "Floating Point—The Second Generation for Digital Signal Processing"

Session 19: User Oriented Tools for Custom VLSI/LSI Design

Thurs 9 to 11 am

Chair: D. E. Farina, Dumont Alphatron, Inc

19/1 "How to VLSI for Systems Designers"

19/2 "Gate Array Design Approach—A Variety of Logical Structures"

19/3 "The Evolution of Cell Libraries as User Tools"

19/4 "Integrated CAD System for Custom IC Design"

19/5 "Standard Cells and a Successful Design Strategy—Cause and Effect"

Session 20: LAN Silicon and Systems

Thurs 9 to 11 am

Chair: V. Coleman, Advanced Micro Devices, Inc

20/1 "Complete Implementation of Ethernet/IEEE 802-3 in VLSI"

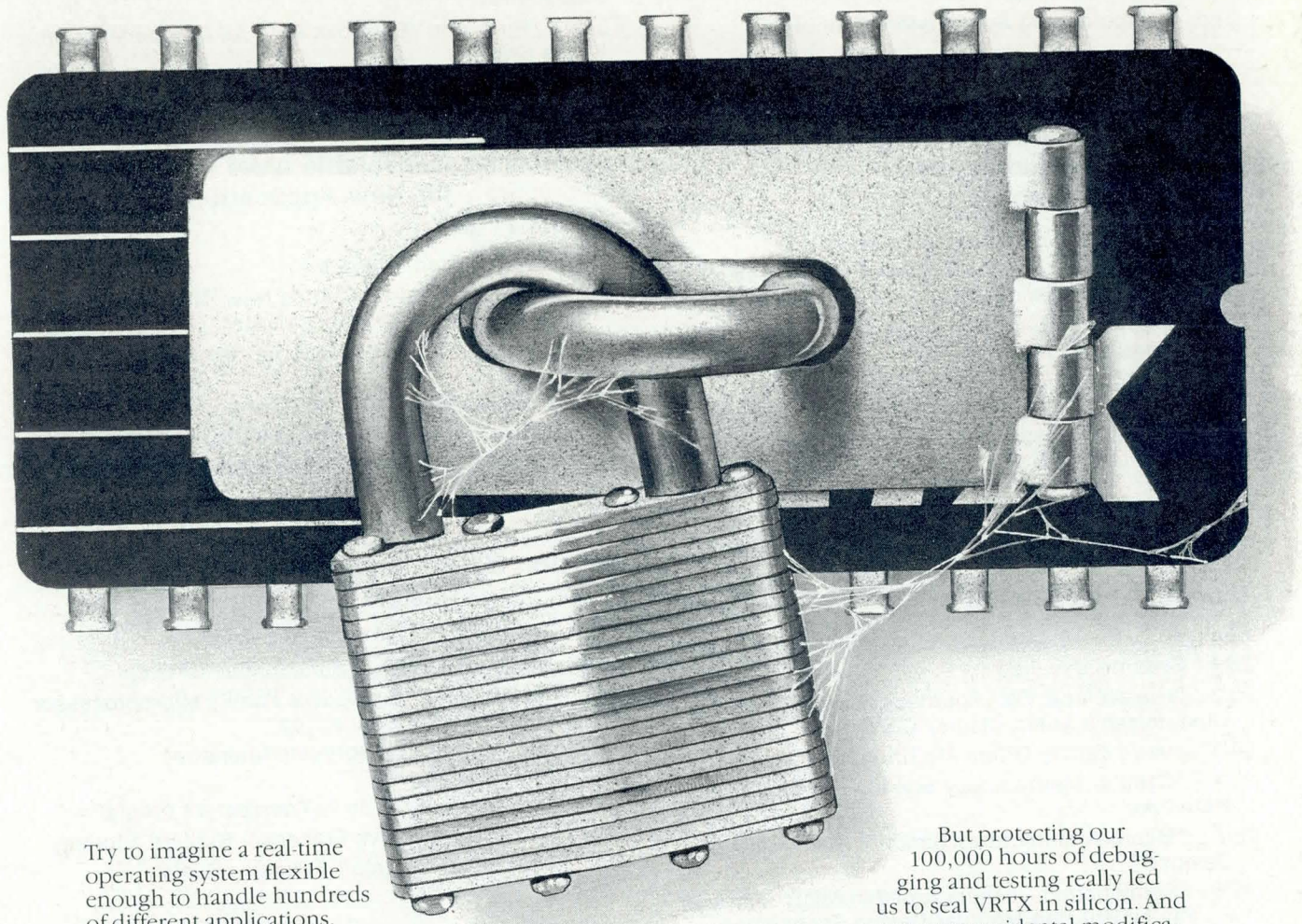
20/2 "State Machine Implementation of Ethernet for the S-100 Bus"

20/3 "Node Processor Architecture for Ethernet"

20/4 "Efficient Token Passing through Silicon"

(continued on page 78)

All this success and we haven't changed a bit.



Try to imagine a real-time operating system flexible enough to handle hundreds of different applications.

Without any modification.

Our VRTX® microprocessor operating system can do just that. Over 200 diverse applications, from navigating aircraft to controlling disks, to playing video games, have been successfully implemented around VRTX. All without tweaking a single bit of VRTX code.

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Because our VRTX operating system is delivered in 4K bytes of ROM. Which naturally makes tweaking a little impractical.

But it does make VRTX the most bug-free operating system you'll ever use. And the easiest one you'll ever install.

In fact, we wouldn't be surprised if you saved six to 12 months of development time using VRTX.

But protecting our 100,000 hours of debugging and testing really led us to seal VRTX in silicon. And prevent even accidental modifications from introducing new bugs. So now we know, no matter how successful we get, we'll never get spoiled.

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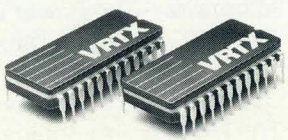

Operating systems in silicon.

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CIRCLE 43

(continued from page 76)

Session 22: The Emerging Role of Semicustom LSI: A Long Term Perspective

Thurs 12:30 to 2:30 pm

Chair: A. Rappaport, *EDN* magazine

22/1 "Determining Semicustom IC User's Needs"

22/2 "Customer/Vendor Roles in the Custom Circuit World: Benefits and Pitfalls"

22/3 "Trends in CMOS Gate Arrays"

22/4 "Semicustom Alternatives for System Design and Manufacturing"

22/5 "Directions in Semicustom Evolution"

Session 23: VLSI Logic to Support High Speed Bit Streams in LANs and Winchesters

Thurs 12:30 to 2:30 pm

Chair: S. Rajpal, Monolithic Memories, Inc

23/1 "Serializing FIFOs and Burst Error Processor Team up to Enhance Serial Data Reliability"

23/2 "Ethernet Type Systems"

23/3 "Impact of Protocols on VLSI Implementation for Disks and LANs"

23/4 "CMOS Manchester Code Converter for Ethernet"

23/5 "LSI/VLSI Encapsulation Considerations of Token Passing LANs"

Session 25: Functional Cells Define New "Standard" Products

Thurs 3:30 to 5:30 pm

Chair: H. L. Supp, American Microsystems Inc

25/1 Session Overview

25/2 "Hierarchical Cell Approach Speeds Design of Customizable Video Display Controller"

25/3 "M6805 Family Offers Multifunction Capabilities"

25/4 "Cellular Methodology Speeds LAN Chip Design Networks"

25/5 "Macro Architectures Simplify Standard Product Designs"

25/6 "Semicustom Designs Broaden Microcomputer Family by Utilizing Modular Design Techniques"

Session 26: Serial Bus Structures for Microcomputers—Small Area Networks

Thurs 3:30 to 5:30 pm

Chair: C. Kaplinsky, Signetics Corp

26/1 "An Introduction to Small Area Networks"

26/2 "Microwire—The Power of Simplicity"

26/3 "The D^2B—A Digital Data Bus for Small Area Networks"

26/4 "Using the 8051's 9-bit Serial Mode"

26/5 "The I^2C Bus—An Interconnect Structure for Integrated Circuits"

Session 27: Advances in Precision Converters

Fri 9 to 11 am

Chair: J. M. Bryant, Analog Devices, Inc

27/1 "The Evolution of Converter Characteristics, Applications, and Testing"

27/2 "New Designs and Processes for High Resolution DACs"

27/3 "Very High Speed Precision Converters"

27/4 "The Design of 12-bit Data Conversion Systems"

27/5 "Precision 16-Bit DAC Puts All Components on One Chip"

27/6 "A Monolithic 4½-Digit Integrating ADC"

Session 28: Nonvolatile RAMs and EEPROMs for New Applications

Fri 9 to 11 am

Chair: W. E. Tchon, Xicor, Inc

28/1 "Intelligent EEPROM Adds New Dimensions to Nonvolatile Memory Applications"

28/2 "Design Considerations for Nonvolatile Memories"

28/3 "Applications Using E^2 Technology"

28/4 "User Features in New EEPROM Designs"

28/5 "NOVRAMs and EEPROMs with User Oriented Features"

Session 29: Advanced In-Circuit Emulator Design

Fri 9 to 11 am

Chair: C. Ching, National Semiconductor Corp

29/1 "Solutions to the NS16000 Family Microprocessor Emulation Design Challenges"

29/2 "Debugging in a Software Intensive Environment"

29/3 "Approaches for Truly Transparent Emulation"

29/4 "A Comprehensive Processor Support Strategy"

29/5 "Advanced In-Circuit Emulator Design"

Session 31: Design Considerations for '80s Instrumentation

Fri 12:30 to 2:30 pm

Chair: J. Taggart, Tektronix, Inc

31/1 "Field Measurements ... Past, Present, and Future"

31/2 "Integrating Intelligence into Instrumentation to Enhance Capability"

31/3 "Instrumentation Networks with Distributed Control"

31/4 "Components for Instruments That Employ Digital Signal Processing Technologies"

31/5 "Applying New Technologies to Meet Instrument Users' Needs"

(continued on page 80)

We've just expanded our pin and socket system three ways. Worldwide.

The AMP Metrimate interconnection system has three new members. The Power Distribution Module. The Drawer Connector. The Data Bus Connector.

Like all Metrimate products they meet UL, CSA and VDE standards. They're available around the world. And they come with the service and support you want wherever you are.

These special styles complement an extensive line that costs less to apply, too, because of housings with molded-in mounting and latching hardware. Also includes coax, electro optics, signal, and power snap-in contacts.

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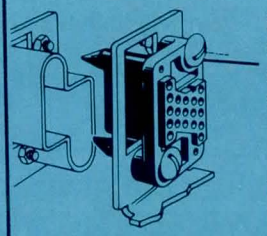
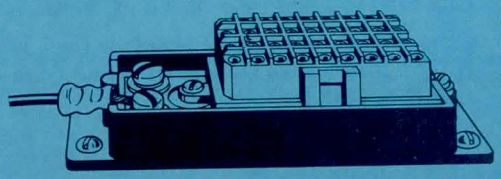


Drawer connector has .090" radial float and integral alignment for blind mating applications.

Power Distribution module eliminates tedious point-to-point wiring.



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CIRCLE NUMBER 10

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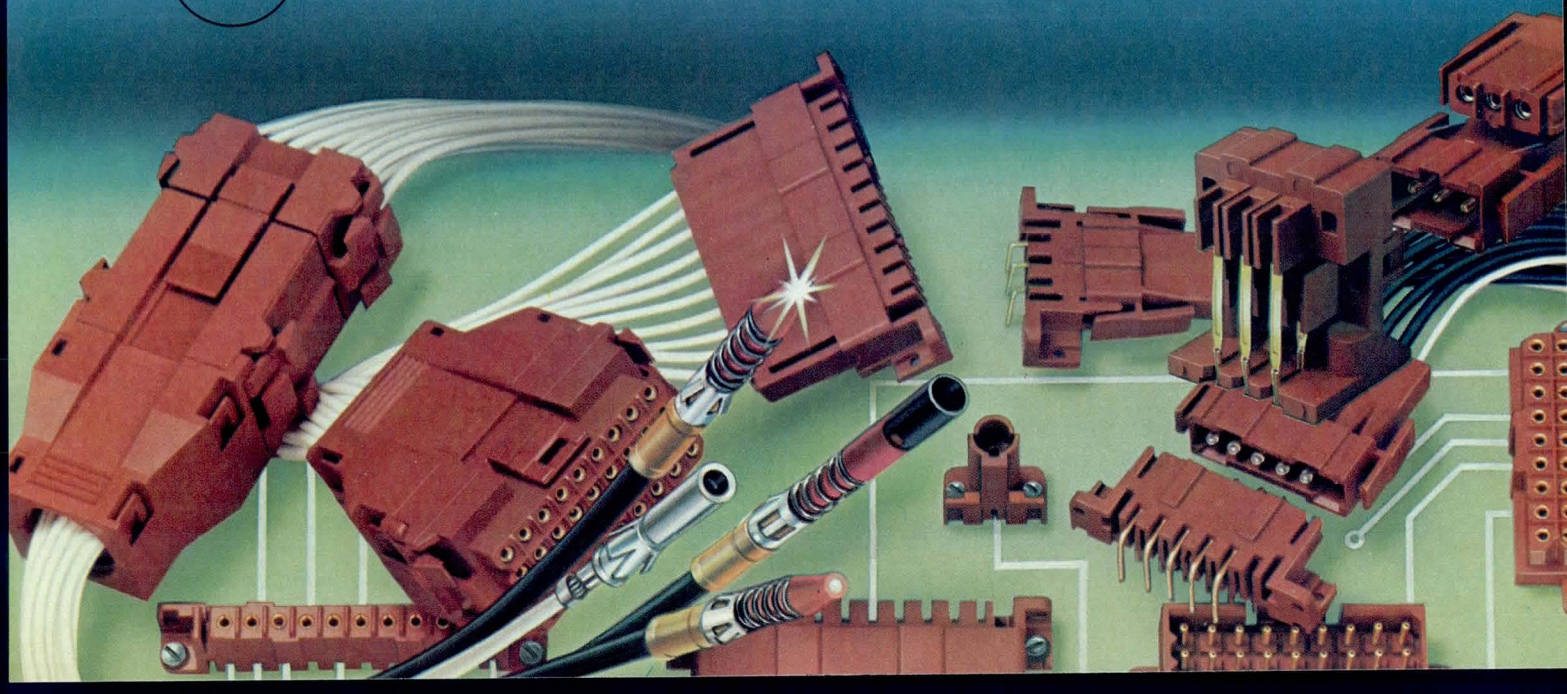

(continued from page 78)

Session 32: Tools for 16-Bit Software Development

Fri 12:30 to 2:30 pm

Chair: R. E. Hoffman, First Systems Corp

32/1 "Software Tools to Match Growing Microprocessor Sophistication"

32/2 "High Level Language Productivity Using the LANDS Tool Box"

32/3 "Advanced System/Software Development Tools Using Unix Systems V"

32/4 "Cross-Compiling, Cross-Assembling, and Now Cross-Debugging"

Session 33: Small Digital Gate Arrays

Fri 3:30 to 5:30 pm

Chair: S. R. Allen, Master Logic Corp

33/1 "Mini-Arrays for CMOS Standard Products"

33/2 "Interactive Design of Small Gate Arrays—A Progress Report"

33/3 "A CMOS Gate Array Family: A Perspective on Some Real Applications"

33/4 "Silicon Breadboards—A Stepping Stone to Custom LSI"

33/5 "Semiautomatic and Automatic Layout Tools for User Defined ICs"

33/6 "Future Directions in User Defined ICs"

Session 34: Alterable Microcomputers Usher in a Dynamic New Era

Fri 3:30 to 5:30 pm

Chair: B. Huston, Motorola, Inc

34/1 "Single-Chip Microcomputer with EEPROM Allows Flexible System Design"

34/2 "Innovative Microcomputers with a High Level of Integration Allow a Wide Range of Applications in Functional Space"

34/3 "A New Single-Chip Microcomputer Offers Design Flexibility for High End Applications"

34/4 "Will There Be ROM Based Microcontrollers in 1985?"

34/5 "EPROM Based Microcomputers Open Up New Applications"

Session 35: Changes in Tools for the Microprocessor Software Engineer

Fri 3:30 to 5:30 pm

Chair: R. Drohan, Gould Design & Test Systems

35/1 "High Level Language Product Design for Microprocessors"

35/2 "Evaluating Software Performance in Microprocessor Design"

35/3 "Software Tools for Embedded Systems"

35/4 "Hardware Based Tools for High Level Language Debug" □

Mini/Micro West

Professional Program*

Session 1: LAN Silicon and Systems

Tues 9 to 11 am

Chair: V. Coleman, Advanced Micro Devices, Inc

1/1 "Complete Implementation of Ethernet/IEEE 802-3 in VLSI"

1/2 "State Machine Implementation of Ethernet for the S-100 Bus"

1/3 "Node Processor Architecture for Ethernet"

1/4 "Efficient Token Passing through Silicon"

*Professional Program sessions are subject to last-minute changes.

Session 2: 16/32-Bit Microprocessor Architectures

Tues 9 to 11 am

Chair: M. A. Davidson, Motorola, Inc

2/1 "The 16000 Microprocessor Family"

2/2 "The iAPX 286 Architecture"

Session 3: Upper Level Protocols for Local Area Networks

Tues 12:30 to 2:30 pm

Chair: M. Hall, Sytek, Inc

3/1 "Real World Implementation of Upper Level Protocols"

(continued on page 82)

"No pictures. No promises. No joke."

When other keyboard companies are running around asking their people to show pictures and make promises about their Low Profile Programs, remember that one company is prototyping, building, and shipping, custom low profile keyboards and enclosures, faster than any other. Guess who?

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Computer Products Division
Keyboard Business Section
General Instrument Corporation
P.O. Box 758
Post Falls, ID 83854
208/773-4541
Telex: 32-6448

CIRCLE 44

(continued from page 80)

3/2 "Experiences Providing Support for XNS Protocols"
3/3 "ISO's Open System Integration Upper Level Protocols on a Broadband Local Area Network"

Session 4: Advanced Peripherals for 16/32-Bit Microprocessors

Tues 12:30 to 2:30 pm

Chair: J. Browne, Motorola, Inc
4/1 "High Performance Peripherals for the M68000 Family"
4/2 "The 16000 Peripheral Family"
4/3 "Intelligent Controllers for the 68000 Family"
4/4 "High Performance Intelligent Disk Controllers"
4/5 "Advanced Systems Elements in the Am9516 Universal DMA Controller"

Session 5: Protecting Codes in Private/Security-Sensitive Applications

Tues 3:30 to 5:30 pm

Chair: A. Toth, Intel Corp
5/1 "Need for Software Security from a User's Point of View"
5/2 "Keeping Software from Being Copied—A New Silicon Method"
5/3 "Secure EPROMS—A Micro Controller Offering of Proprietary Software Protection"
5/4 "EEROM Adaptive Security for Single-Chip Microcomputers"

Session 6: Contrasting Memory Management Philosophies in 16/32-Bit Microprocessors

Tues 3:30 to 5:30 pm

Chair: R. Mateosian, National Semiconductor Corp
6/1 "The Virtual 68010"
6/2 "Demand Paged Virtual Memory with the Z8003"
6/3 "Memory Management Implementation on the iAPX 286"
6/4 "Elegant Memory Management: NS16000"

Session 7: Flexible Terminals Used As Packaged Control Panels for Service, Setup, and Control

Wed 9 to 11 am

Chair: W. E. Fletcher, Termiflex Corp
7/1 "Service of Rotating Memories Using a Handheld Terminal"
7/2 "New York Stock Exchange Experiences with Online Interactive Floor Control"
7/3 "Survey of Commercially Available Packaged Control Panel Equipment"
7/4 "Handheld Set Communicator for the Engine Test Set on the M1-Tank"

Session 8: System Implementation Languages—Present and Future Directions

Wed 9 to 11 am

Chair: L. R. Carter, Motorola, Inc
8/1 "Pascal Enhancements: Past and Future"
8/2 "A Pragmatic Approach to Compiler Construction"
8/3 "Trends in Test Programming"
8/4 "Augmentation Language: An Extension to Other Languages"
8/5 "S/SL: A User's Experience"

Session 9: Chip/System Implementation Considerations for Videotex/Teletext Terminals

Wed 12:30 to 2:30 pm

Chair: O. P. Agrawal, Synertek, Inc
9/1 "NAPLPS Videotex Terminals"
9/2 "Implementation Considerations for NAPLPS Videotex"
9/3 "NABTS Teletext for the Consumer Market"
9/4 "LSI/VLSI Encapsulation Considerations for Videotex/Teletext"

Session 10: Microcomputer and the C Language, Development Path of the Future

Wed 12:30 to 2:30 pm

Chair: J. Handy, Intel Corp
10/1 "Source Level Debugging Technology for the C Language"
10/2 "A User Friendly C Compiler Designed for Programmers"
10/3 "A User's Perspective of the C Programming Language"
10/4 "A C Compiler for the iAPX-86 Family Architectures"
10/5 "C Programming on a Workstation"

Session 11: Architectural Requirements for an Engineering Workstation

Wed 3:30 to 5:30 pm

Chair: D. Laughlin, CAE Systems, Inc
11/1 "Hardware and Software Requirements for an EEWS"

(continued on page 84)

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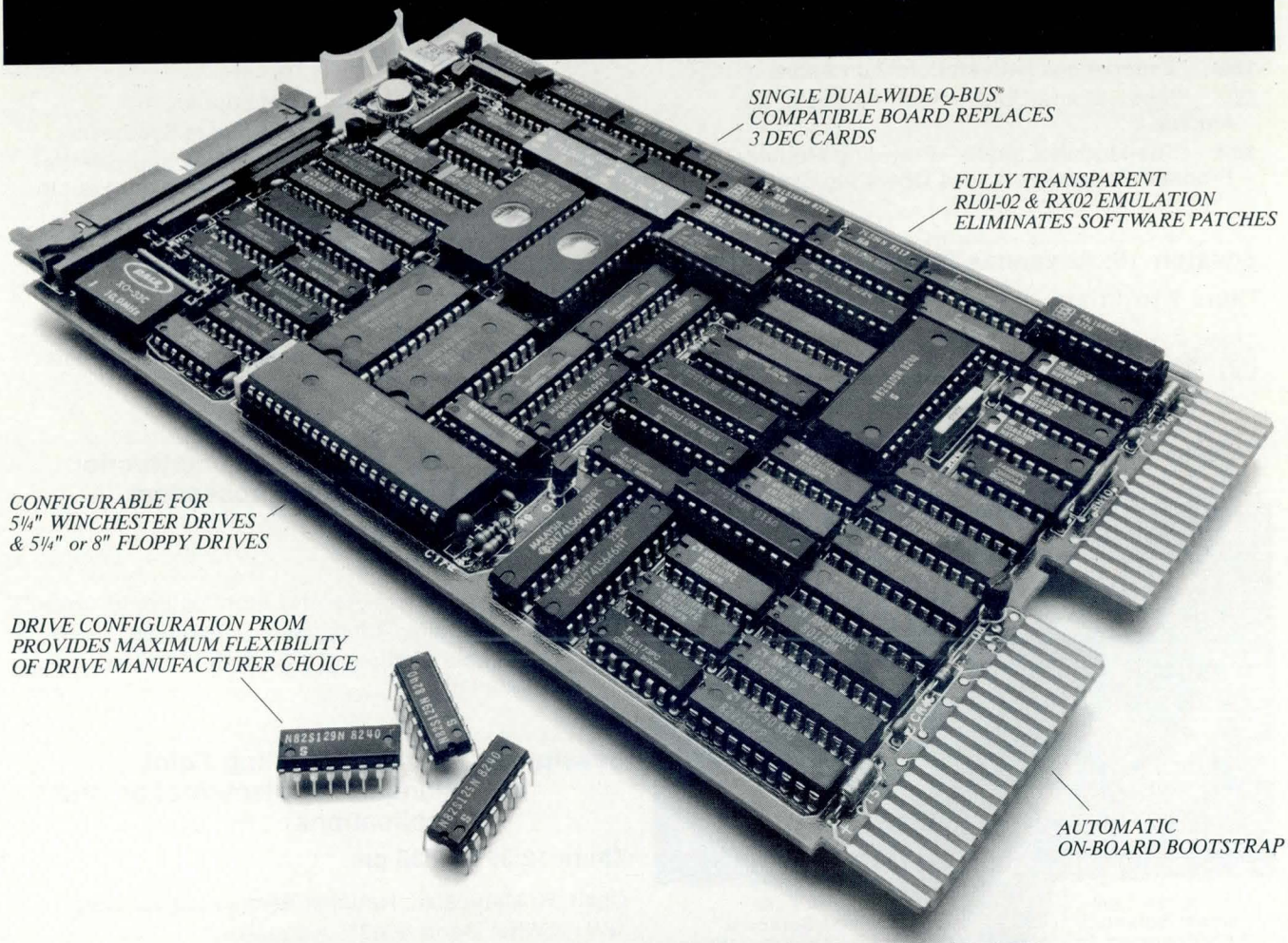

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CIRCLE 45

(continued from page 82)

11/2 "Professional Workstations"
11/3 "Workstations for OEMS"
11/4 "A Workstation for VLSI"

Session 12: Experience with Modula-2

Wed 3:30 to 5:30 pm

Chair: A. W. Brown, Volition Systems
12/1 "A Novice Programmer's View of Modula-2"
12/2 "Experiences with Modula-2 on Apple III"
12/3 "Modular and Object Oriented Design in Modula-2"
12/4 "The Module Library—Providing Modula-2 Program Portability across Operating Systems"

Session 13: Advances in Microprocessors

Thurs 9 to 11 am

Chair: F. Krupecki, Signetics Corp
13/1 "The 8X305 Microcontroller: A Special Processor of Intelligent Control Systems"
13/2 "High Performance Microprogrammed Controller Architecture"
13/3 "Using the Alterable Microcomputer Ultra High Performance Low Cost Graphics Terminal"
13/4 "A New High Performance Microprocessor with Z80 Software Compatibility"
13/5 "The 32032: An Ultra High Performance Microprocessor"

Session 14: Real World Number Crunching

Thurs 9 to 11 am

Chair: C. Hastings, Monolithic Memories, Inc
14/1 "High Performance Digital Music Synthesis"
14/2 "16 x 16 Flow through Multipliers Improve the Performance and Economics of Long Word Length Multiplication"
14/3 "A Practical Architecture for Feeding Number Crunchers"
14/4 "Cycle vs Access Time: Optimizing Semiconductor Parts for Number Crunching"
14/5 "Lucasfilm Audio Signal Processor and Music Instrument"

Session 15: Independent Data/Instruction Stream Microprocessors

Thurs 12:30 to 2:30 pm

Chair: T. Miller, NCR Corp
15/1 "Performance of Harvard Architecture in TMS320"
15/2 "Architecture Comparison of Two MIPS"
15/3 "A Simple Multiple ALU Computer for Low Level Parallelism"

Session 16: The New Floating Point Standard: Implementation and Applications

Thurs 12:30 to 2:30 pm

Chair: R. Mateosian, National Semiconductor Corp
16/1 "What Good Is It?"
16/2 "High Performance Floating Point Coprocessor for Protected Multi-User Systems"
16/3 "Floating Point Support for the NS16000 Family"
16/4 "Elementary Functions Based upon IEEE Arithmetic"
16/5 "Floating Point Power for the M68000 Family"
16/6 "ELXSI's 6400 Arithmetic Processor"

Session 17: System Software in Silicon

Thurs 3:30 to 5:30 pm

Chair: S. Ohr, *Electronic Design* magazine
17/1 "Software Logic Replacement"
17/2 "Software and Hardware Integration Leads to Compact Systems: CP/M-86 and iRMX-86 on Silicon"

(continued on page 86)

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Circle 46 for Literature

Circle 177 for Demonstration

(continued from page 84)

17/3 "A p-Code Interpreter for the 1804"
17/4 "The R65F11 Forth Microcomputer"
17/5 "Silicon Software Supports Many Users"

Session 18: Graphics Display Memory

Thurs 3:30 to 5:30 pm

Chair: S. Gupta, IBM Corp
18/1 "CMOS DRAMS Improve Graphics Bandwidth"
18/2 "Memories in Graphics—Present and Future"
18/3 "Memory Architecture Comparisons"
18/4 "Dual-Port Memory with High Speed Serial Access"
18/5 "High Resolution Graphic System"

Session 19: System Design with 16/32-Bit Microprocessors

Fri 9 to 11 am

Chair: R. Mateosian, National Semiconductor Corp
19/1 "A Simple Z8000 System"
19/2 "M68000 Educational Computer Board Design"
19/3 "A 16/32-Bit Architecture for Signal Processing"
19/4 "System Design with the NS16000 Family"
19/5 "Designing a High Performance 286 System"
19/6 "Multiprocessor Systems Using the Transputer"

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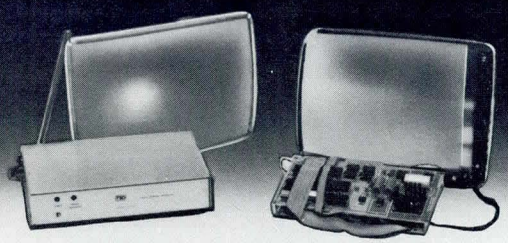

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Session 20: Desktop and Personal Computers

Fri 9 to 11 am

Chair: R. Melen, Cromemco, Inc
20/1 "Riding the IBM Wave"
20/2 "The Executive I: An Advanced Portable Desktop Computer"
20/3 "An IEEE 696 Bus Xenix Based Virtual Memory Desktop Computer"

Session 21: Realtime Fail-Safe and Fault Tolerant Mini/Microcomputer

Fri 12:30 to 2:30 pm

Chair: G. A. Kravetz, Fail-Safe Technology Corp
21/1 "Design Considerations for Achieving a Fault Tolerant System"
21/2 "New Architecture for Fault Tolerant Systems"
21/3 "Applications of Fault Tolerance in Industrial Control"
21/4 "Micro Based Fault Tolerant Architecture"

Session 22: Advanced Personal Computers and Their Processors

Fri 12:30 to 2:30 pm

Chair: J. J. Farrell, Motorola, Inc
22/1 "Microprocessors for a Broad Family of Personal Computers"
22/2 "Cost-Effective 16/32-Bit Solution"
22/3 "The Future of Personal Computers"
22/4 "High Level Computation for Personal Computers"

Session 23: The MPU Product Path: 8 Bit, 16 Bit, 32 Bit

Fri 3:30 to 5:30 pm

Chair: J. Nutt, Motorola, Inc
23/1 "Compatible Microprocessor Systems: 16 Bits to 32 Bits"
23/2 "8/16/32-Bit Compatible MPUs Offer Product Breadth"
23/3 "Software Compatibility Is a Must"
23/4 "8/16/32-Bit MPU Requirements for Managing Energy and Facilities"

Session 24: Distributed Networking with Personal Computers and Terminals

Fri 3:30 to 5:30 pm

Chair: W. Ferris, Advanced Systems Concepts, Inc
24/1 "Peripheral Networks for the Small Business Office"
24/2 "Making the Link with Micros and Distributed Networks"
24/3 "Electronic Mail"
24/4 "Networked PCs; Ether Series Case Studies" □

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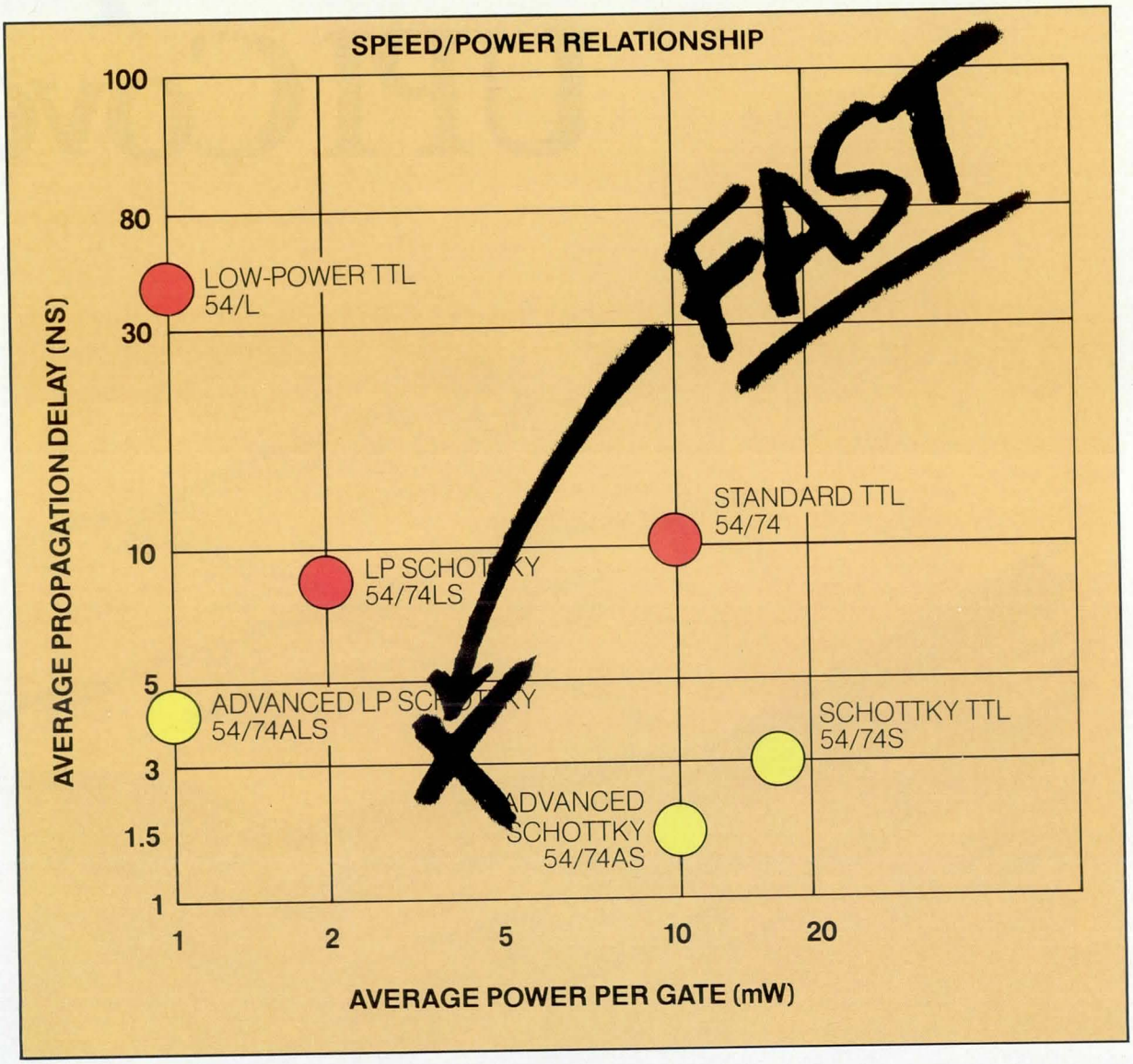

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CIRCLE 47

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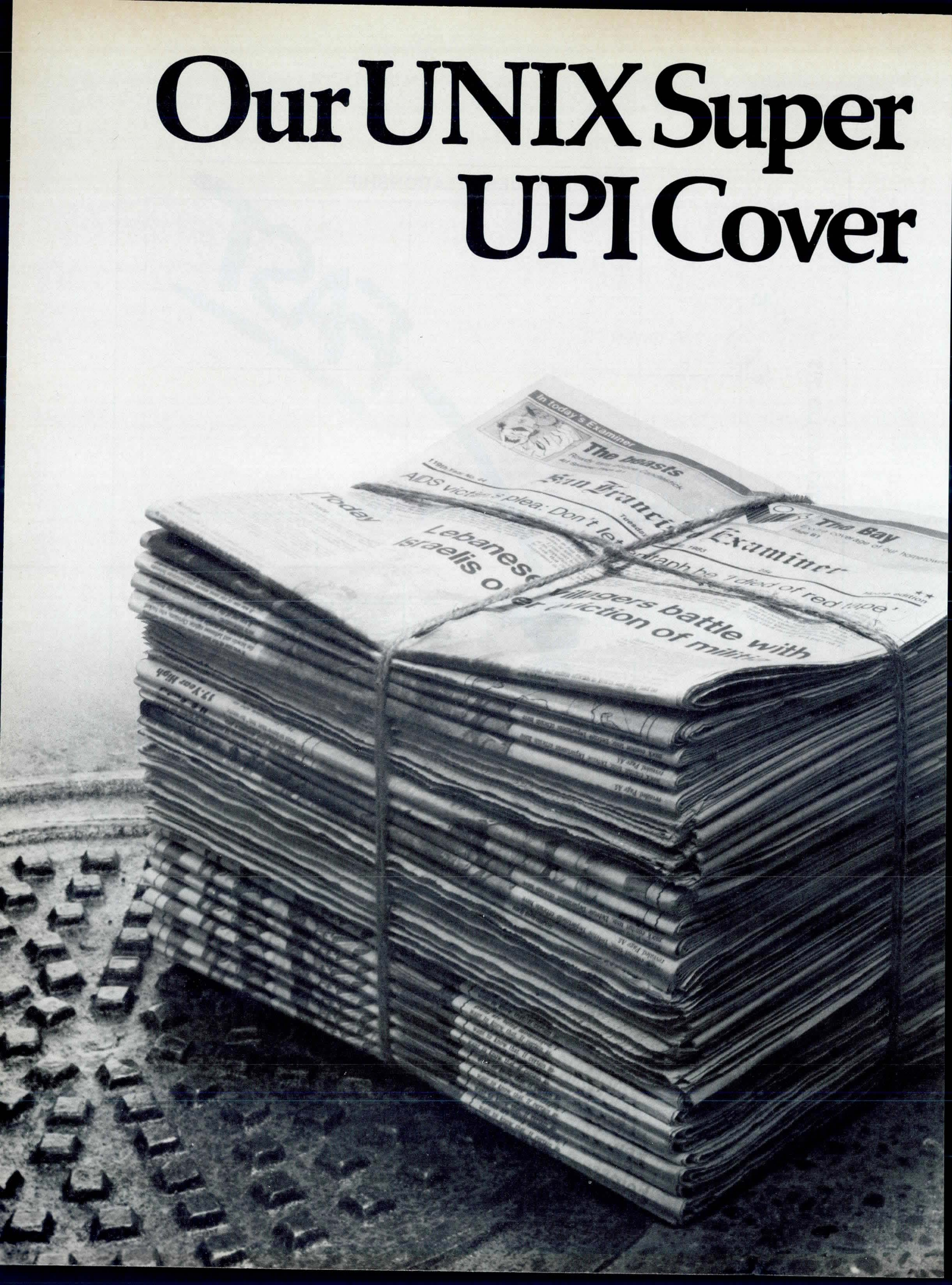

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CIRCLE 48

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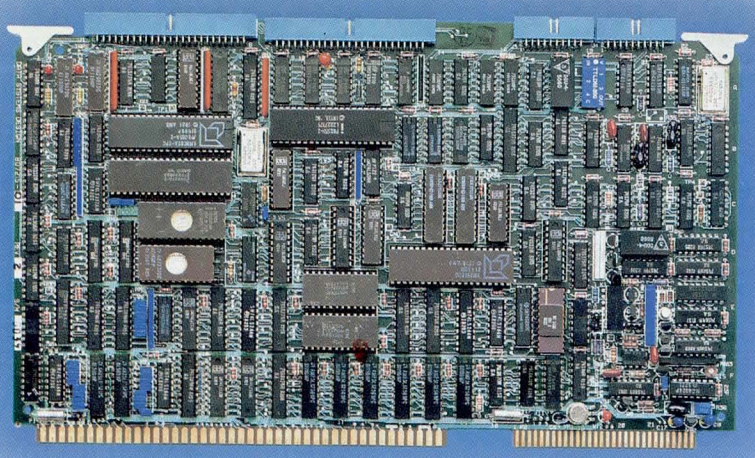

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CIRCLE 50

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Annual Conference on Industrial Electronics

Hyatt Regency Hotel
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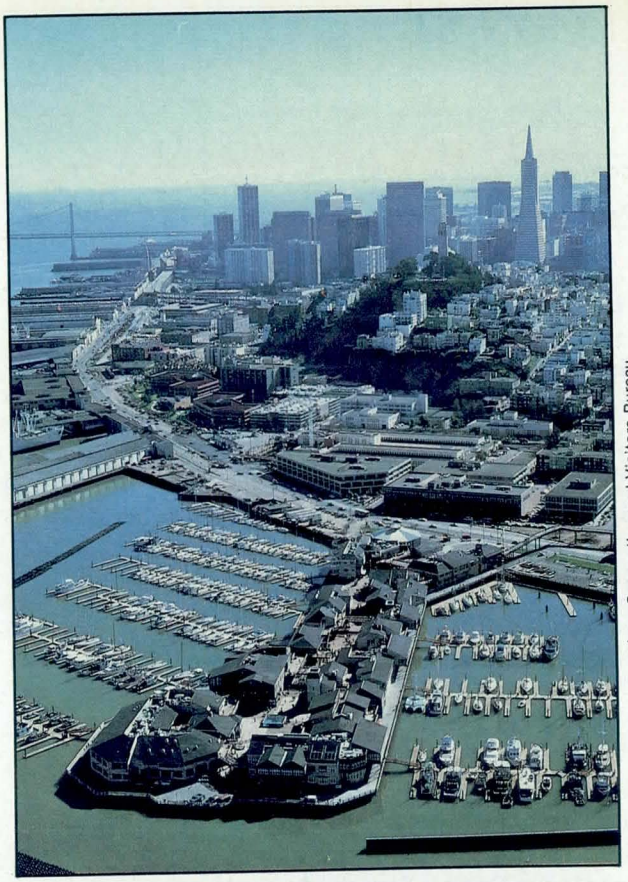

Photo courtesy of San Francisco Convention and Visitors Bureau.

The impact of small computers on control and automation, which has increased exponentially in the past few years, will be the prime focus of information disseminated at IECON '83. IEEE Industrial Electronics Society's ninth annual conference on industrial applications of mini and microcomputers is international in scope. Speakers from leading companies around the world will discuss the increasing number of applications for mini and micro systems in industrial electronics.

Contributing authors will present papers on designing, implementing, and testing hardware and software systems for manufacturing process control, energy systems, data acquisition, and signal processing. Even those papers that describe new product releases will provide high quality technical information, not marketing or sales hype. The conference keynote speaker, Ted Jenkins, (general manager, peripheral components, Intel Corp) will address "VLSI Technology: Past, Present, and Future." Special sessions preceding and following the address will amplify this topic, along with five tutorials that promise in-depth coverage of specific areas of mini/micro industrial applications.

Tutorial I will establish the fundamental design criteria enabling microprocessors to be built into realtime process control. This is in response to a request that technical data cover a recent trend: process control and programmable controller systems using vendor-supplied hardware have become the most frequently used distributed computer control systems today. Dr M. Andrews, professor of computer science at Colorado State University, will lead the discussion on programmable addressing modes and instruction sets, real world interfaces, data acquisition, process control digital algorithms, and a method of converting Laplace into digital code.

Each of the remaining four tutorials will be similarly presented by respected engineering scientists. Speakers will provide answers to such questions as "How is fault tolerance achieved and why is it important in digital design?" (Dr J. A. Humphrey, president, Del Rey Systems). Also "What are the latest digital IC design techniques?" and "How are combination networks, PAL- and PLA-based designs, modern sequential networks, and LSI/MSI used as system building blocks?" (Dr J. R. Story, chair, Electrical Engineering and Technology Dept, Florida International University).

Personnel aspects of software development and high level software design quality assurance will be presented by Dr A. B. Delfino, consultant, Software Engineering & Instruction, Inc, and adjunct professor of computer science, Santa Clara University. To round out the conference, Dr A. Weaver, associate professor, University of Virginia, will discuss the topology of local area networks in terms of virtual circuits, queuing theory, ISO layered architectures, contention, token-passing and hybrid protocols, and data encryption and security.

IECON '83 will run concurrently with this year's Wescon conference and exposition (see p 74). Registration for IECON includes free admission to Wescon; shuttle buses between the two conventions will be available.

(continued on page 94)

For registration information, contact Frank A. Jur, Bechtel Corp, 45 Fremont St, MS45/17A26, San Francisco, CA 94109. Tel: 415/768-3023

IECON'83

(continued from page 93)

Professional Program Excerpts*

Tutorial I: Microprocessors in Control and Instrumentation

Mon 9 am to 5 pm

M. Andrews, Colorado State Univ

Tutorial II: Software Engineering Management

Mon 9 am to 5 pm

A. B. Delfino, Software Engineering & Instruction, Inc

Session 1: Automated Manufacturing

Tues 9 to 11:30 am

Chair: P. Gold, Adolph Coors Co

1/1 "The Use of Touch-sensitive Video Displays in Online Control Systems"

1/2 "A Locally Intelligent, Programmable, Flat-panel Display for Industrial Control Applications"

1/3 "The Synor 9900: A New Continuity Tester for Bare PC Boards"

1/4 "A Minicomputer-based Continuous Annealing System for Mechanical Filter Long Elinvar Wire"

1/5 "Identification Camera Control"

1/6 "Design of an Automated Labeling System"

Session 2: Data Acquisition

Tues 9 to 11:30 am

Chair: C. W. Einolf, Jr, Westinghouse Electric Corp

2/1 "A Data Acquisition System with Wide Dynamic Range and Weak Signal Enhancement Properties"

2/2 "Marrying a Remote Data Acquisition and Control System to a Medium Resolution Graphic Computer"

2/3 "Microprocessor Application in Data Acquisition Systems"

2/4 "A Microcomputer-based Distributed Event Monitoring System"

2/5 "Personal Computers Monitor Industrial Waste"

Session 4: Machine Vision

Tues 9 to 11:30 am

Chair: J. E. Trombly, Octek Inc

4/1 "Managing Complexity in Vision-based Systems"

4/2 "Applying Machine Vision: A New Approach"

4/3 "The CAV-1000—A High Performance, Cost-effective Vision System"

4/4 "Online Shape Recognition System for Hot-Strips of Steel Using High Speed Image Processing Techniques"

4/5 "Programmable High Speed Image Processor PPI-II"

Session 5: Automated Testing

Tues 2 to 4:30 pm

Chair: T. Goldstein, Bell Labs

5/1 "Computer Switch Tester"

5/2 "Test Set Hardware Performance Evaluation"

5/3 "A Data Acquisition and Control System for Automated Testing of Motor Drives"

5/4 "Personal Computer-based Directional Tool Test Stand"

5/5 "Universal Microcomputer Electrical Testing System"

Workshop I: Software Reliability

Tues 2 to 4:30 pm

Organizer: A. Abramovich, Control Automation

Special Session I: Local Area Networks and Factory Communication

Wed 8:30 to 9:45 am

Chair: L. Hsieh, General Electric Co

Special Session II: VLSI Impact on Industrial Electronics

Wed 10 to 11:15 am

Chair: R. Bruns, Intel Corp

Keynote Address: VLSI Technology: Past, Present, and Future

Wed 11:30 am to 1:30 pm

Speaker: T. Jenkins, Intel Corp

Special Session III: Robotics—Today and Tomorrow

Wed 2 to 3:15 pm

Chair: J. Cassidy, General Electric Co

(continued on page 96)

*Professional Program sessions are subject to last-minute changes.

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The Peripheral Processor Link from Ranyan. It lets PDP-11, LSI-11 and VAX computers share memory. Without making you invest in a whole new system.

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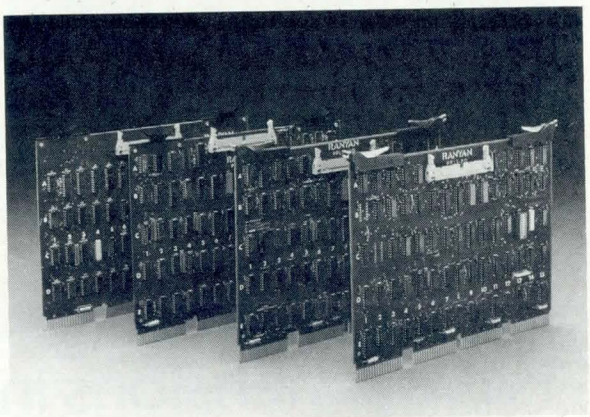

Unforgettable performance. By allowing Unibus or Q-Bus computers to share memory, the Peripheral Processor Link not only dramatically adds computing power, but also provides for parallel processing. Or redundancy computing with one system backing up another so there's never any lost data. Plus data communications and data acquisition system front-ending to keep a host from wasting valuable overhead on menial protocol chores. And unlike other "so-called" means of memory sharing, no special software is required with the Peripheral Processor Link.

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Memorable users. When we introduced the Peripheral Processor Link series nearly two years ago, some very big names took notice. And action. Industry giants like Teledyne, General Electric, Raytheon, and Western Electric; plus scientific labs at Cal Tech and the University of Wisconsin are all using it in their systems. But you don't have to be a big name to take advantage of its big benefits. Especially with its very small price.

For more about the Peripheral Processor Link or any of our DEC system enhancements, call or write Ranyan today. And start sharing the wealth. Ranyan Corporation, 15239 Springdale Street, Huntington Beach, CA 92649. 714-895-5504.

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CIRCLE 51

IECON'83

(continued from page 94)

Special Session IV: Quality in Industrial Electronics: Is It Really Free?

Wed 3:30 to 4:45 pm

Chair: R. Goodman, General Electric Co

Special Session V: Trends in Motion Control

Wed 3:30 to 4:45 pm

Chair: K. Phillips, Eaton Corp, Cutler Hammer Products

Session 8: Programmable Control

Thurs 9 to 11:30 am

Chair: H. Haneda, Kobe Univ

8/1 "A Programmable Logic Controller Based on a High Level Specification Tool"

8/2 "Programmable Controller with a Multiprocessor-based High Speed Interactive Language System"

8/3 "Microcomputer-based Programmable Controller Systems for Industrial Applications"

8/4 "A Novel Sequential Control Function for Analog and Discrete Environments"

8/5 "Ensuring Fail-Soft Process Control: A Distributed Valve Controller Network"

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Session 9: Power Systems

Thurs 9 to 11:30 am

Chair: T. Hasegawa, Toshiba Corp

9/1 "Programmable Controller Standardized Application Programs and Documentation for Nuclear Power Plants"

9/2 "Programmable Front End for Power Network Parameter Monitoring"

9/3 "An Equivalent Circuit Model Identification for Secondary Storage Battery in Power System Load Leveling"

9/4 "Application of Microprocessor to Automatic Reclosing of Electric Power Systems"

9/5 "Application of Microprocessors to Computer-based SCADA System for Electric Power Systems"

Session 10: Software Techniques

Thurs 9 to 11:30 am

Chair: J. F. Ready, Hunter & Ready Inc

10/1 "Specification and Evaluation of Requirements for Embedded Systems"

10/2 "A New Synchronization Scheme for Microprocessor-based Realtime Control Systems"

10/3 "Relational Database Model in the Control of Dynamic Systems"

10/4 "When the Cost of Going Down Goes Up . . ."

Session 11: Robotics

Thurs 9 to 11:30 am

Chair: J. C. Harshaw, Bell Labs

11/1 "Dynamic Computer Control of a Robot Leg"

11/2 "A Software Package for Micro-Robot and Coordination between Robots with Voice Command"

11/3 "Analog vs Digital Nonlinear Control of Master-Slave Manipulators"

11/4 "A Simulation and Operation Software for Manipulator with Pantographic Mechanism"

Session 12: Numerical Control

Thurs 2 to 4:30 pm

Chair: M. A. Catalano, Canberra Industries

12/1 "Modular, High Throughput Computer Numerical Control for Flexible Manufacturing Systems"

12/2 "DNC/CNC—A Way to Improve Quality and Reliability in NC Machining"

12/3 "Microprocessor-based Automatic Programming CNC for Machining Center"

12/4 "Mark Century 200 Computer Numerical Controls: Hardware Architecture and Development Strategy"

12/5 "Mark Century 2000 Computer Numerical Controls: Software Development and Strategy"

 CIRCLE 56

12/6 "Mark Century 2000 Computer Numerical Controls: A System Design for Self Test"

Session 13: Computer Control

Thurs 2 to 4:30 pm

Chair: Y. K. Wo, Bell Labs

13/1 "Microprocessor Controller for a Solar Heating System"

13/2 "Microprocessor-controlled MOSFET Inverter for Solar Energy System"

13/3 "Microprocessor-based Gate Pulse Generator for a Phase-controlled Rectifier"

13/4 "Microcomputer Digital Control of an SCR Type Arc Welding Power Source"

13/5 "Suboptimal Control of the Roof Crane by Using the Microcomputer"

Session 14: Local Area Networks

Thurs 2 to 4:30 pm

Chair: A. Sauer, Siemens AG

14/1 "Design Philosophy of a Portable and Extensible Network Message Processor Software for Microcomputer Network"

14/2 "Onboard Optical Data Communication Network for Train Control"

14/3 "A High Speed Optical Data Highway for Industrial Control Systems"

Workshop II: Manufacturing Work Cell Architecture

Thurs 2 to 4:30 pm

Organizer: A. Abramovich, Control Automation

Tutorial III: Fault Tolerant Computers in Industrial Applications

Fri 9 am to 5 pm

J. A. Humphrey, Del Rey Systems

Tutorial IV: Modern Digital Systems Design

Fri 9 am to 5 pm

J. R. Story, Florida International Univ

Tutorial V: Local Area Networks

Fri 9 am to 5 pm

A. Weaver, Univ of Virginia □

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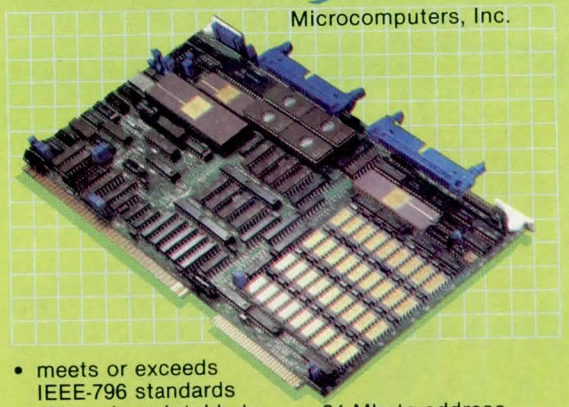

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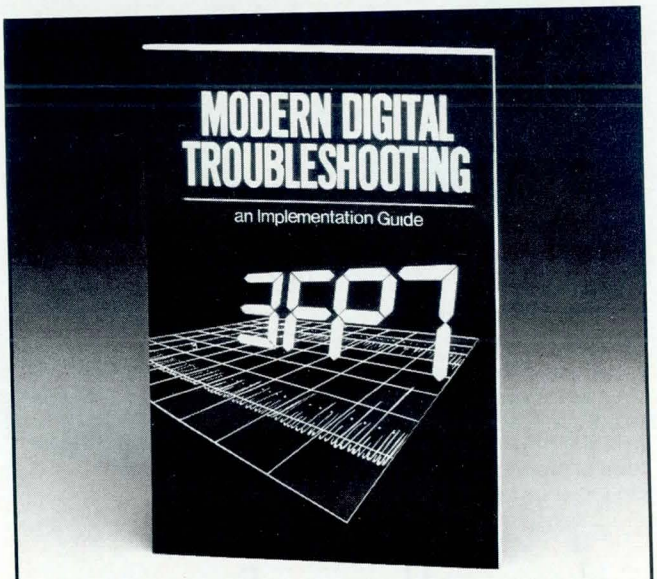
CIRCLE 57



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CIRCLE 53

AUTOFACT 5

AUTOMATED INTEGRATED FACTORY OF TOMORROW

Photo courtesy of Metropolitan Detroit Convention and Visitors' Bureau.

CONFERENCE AND EXPOSITION

Cobo Hall
Detroit, Michigan
Conference: November 14 to 17, 1983 **Exposition: November 15 to 17, 1983**

The best way to automate, computerize, and integrate manufacturing operations—from start to finish—is an ongoing concern of manufacturing engineers at the forefront of production technology. Such know-how is the focal point of the AUTOFACT 5 convention, to be held at Detroit's Cobo Hall November 14 through 17. Complementing the show's technical program sessions is the exposition, which will run three days. It will feature over 100 companies offering hands-on demonstrations of systems equipment and proven methods of computer automation.

A bonus at this year's AUTOFACT will be the PCI/MOTORCON exhibition. This adjoining event will feature power electronics, sensor and motion control equipment, and components useful in developing shop floor automation systems and facilities.

Computer integrated manufacturing (CIM), as AUTOFACT 5's theme, is the backbone of each program session and of over nine hours of tutorials. Computer-aided design and manufacturing (CAD/CAM) will be demonstrated as a means of breaking out from under a closed loop manufacturing operation into a unified, efficient, computer-based network of design, engineering, and production tasks. More than 100 experts chosen for their experience in the field will address other CIM techniques such as analysis and simulation, process facilities, industrial robotics, materials handling systems, integrated graphics, computerized storage and retrieval, group technology, automated assembly, quality assurance and control, and CAD/CAM software.

During the first three days of AUTOFACT 5, tutorials that explain the fundamentals of automated manufacturing will be offered in evening sessions. Several of the tutorials will be repeated for the convenience of the attendees. Both theory and practice will be taught to give insights into CAD/CAM's present capabilities and its prospects for future development.

Basics and applications of 3-D solids modeling will be reviewed. These discussions will cover not only hardware requirements, but also who sells the machines and for what price. The tutorial sessions dealing with CIM will cover the parametric design process, the graphics automated template system (GATS), the tubend process, finite element analysis, and automated diagram systems. Requirements for communications, control networks, and database management to implement a CAD/CAM manufacturing process will also be examined.

The Computer and Automated Systems Association of the Society of Manufacturing Engineers (CASA/SME), in cooperation with SME and Robotics International (SME/RI), is sponsoring AUTOFACT 5.

(continued on page 100)

For registration information, contact SME Public Relations Dept, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

(continued from page 99)

Professional Program Excerpts*

Session 1: Integration
Tues 8:30 to 10:30 am

Chair: W. D. Beeby, William Beeby & Assoc, Inc

1/1 "Integrating CAD and CAM"

1/2 "New Hardware and Software Trends in CAD/CAM"

1/3 "Productivity in the High Technology Industry"

Session 2: Design
Tues 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: A. Bernat, General Motors Corp

2/1 "Solid Geometric Modeling—A Design and Manufacturing Strategy"

2/2 "An Approach to Computer-integrated Manufacturing at Brigham Young University"

2/3 "Computer-aided Design for Complex Geometry Molds"

2/4 "Integration Considerations for CAD/CAM Systems"

2/5 "A CAD/CAM System for Sculptured Surfaces"

2/6 "Recent Progress of a Spline-based Solid Modeler"

2/7 "The Role of Facility Design in Achieving CAD/CAM Productivity"

Session 3: Documentation
Tues 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: J. Thompson, Macomb Community College

3/1 "Information Transfer between Computer-aided Design Systems: An Assessment of IGES"

3/2 "CAD to CAM—Using a Shared Data Base"

3/3 "Production Systems Management"

3/4 "The Problems of Using CAD-generated Data for CAM"

3/5 "Clfile Interpreter/Editor"

3/6 "Computerized Electrical Harness Documentation"

3/7 "The Role of Database Management and Simulation in Engineering Projects"

Session 4: Analysis and Simulation
Tues 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: R. Kohl, *Machine Design* magazine

4/1 "FMS Design Using Microcomputer Graphics"

4/2 "Computerized Methods for Predicting Robot Performance"

4/3 "Comparison of Modeling Languages for Simulation of Automated Manufacturing Systems"

4/4 "Finite Element Method—A Design Engineer's Tool"

4/5 "The Reality of Cost-Effective Nonlinear Analysis"

4/6 "Prediction of Binder Wrap in Sheet Metal Stampings Using Finite Element Method"

4/7 "Cost Savings through Material Nesting"

Session 5: CAD/CAM Unification
Tues 10:45 am to 12:30 pm

Chair: C. Michael, Ramtek Corp

5/1 "Taking the 'Slash' Out of CAD/CAM True Design-Manufacturing Integration"

5/2 "Database Management and Distributed Processing"

5/3 "Environment Theory: The Effects of CIM Elements on System Relationship and Performance"

Session 6: Integration
Wed 8:30 to 10:30 am

Chair: C. Skinner, Allen & Hamilton, Inc

6/1 "To be announced

6/2 "Computer-integrated Manufacturing—How To Get Started"

6/3 "Factory Automation—Economics or Survival"

Session 7: Scheduling and Materials
Wed 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: F. M. Zenobia, Jr, Dresser Industries, Inc

7/1 "Technology Integration . . . The Time Has Come"

7/2 "Improving Management Performance—Management's Vital Challenge"

7/3 "Shop Floor Control Sequencing"

7/4 "The Role of Buffer Storage on the Productivity of a Production Line with Robots"

7/5 "Shop Floor Control"

7/6 "The Paperless Factory"

(continued on page 102)

*Professional Program sessions are subject to last-minute changes.

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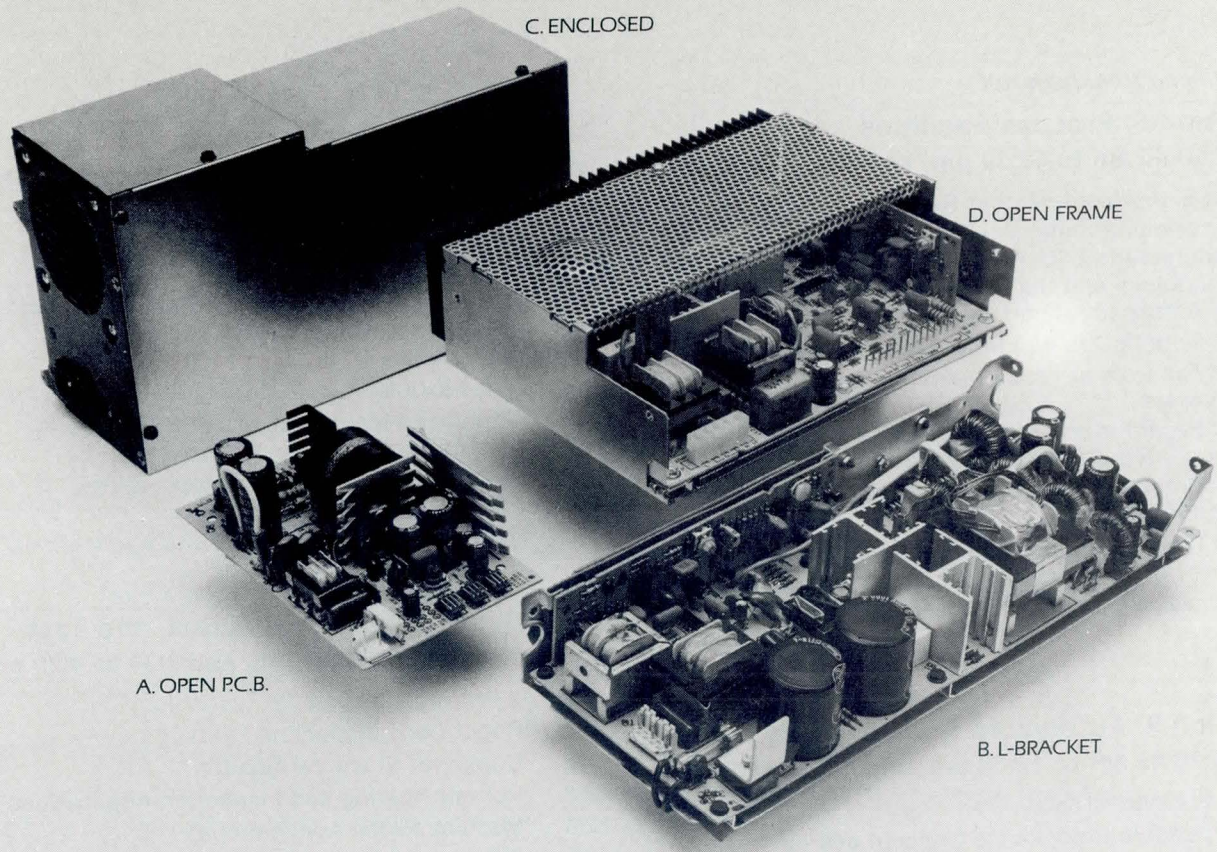

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Z-42-DF	42	.5/2.5	—	.3/2	.04/.5	—	—	Convection	A	6.3 x 3.9 x 1.8
Z-42-EB	42	1/5	—	.7/1.3	.02/.1	—	—	Convection	B	7.3 x 3.9 x 2.0
Z-43-J	43	1.4/4	0/.1	—	—	—	+15 V @ .7/1.5	Convection	A	8.3 x 5.5 x 2.5
Z-64-C	64	2.5/7	0/.3	.5/2	0/.2	—	—	Forced Air	A	9.5 x 5.5 x 4.8
Z-65-DG	65	1/5	—	.3/2	0/.2	0/1.5	—	Convection	B	8.3 x 4.3 x 2.3
Z-73-BA	73	.5/5	—	0/2	0/2	—	—	Convection	C	12.2 x 5.8 x 2.0
Z-74-CA	74	3/6	—	.3/2	0/.2	0/1.5	—	Convection	A	8.5 x 5.0 x 2.0
Z-128-CH	128	1/15	0/.2	.15/1	—	—	+32 V @ .1/1.25	Convection	D	7.5 x 9.4 x 4.0
Z-218-BC	218	10/28	—	.6/4	0/1	0/1.5	—	Forced Air	B	11.8 x 4.8 x 2.5
Z-240-BD	240	2/12	—	.4/5.2	—	.5/1.5	+8 V @ .15/8 +16 V @ 0/1 −16 V @ 0/1	Forced Air*	C	11.3 x 5.7 x 6.5
Z-240-CB										11.4 x 4.2 x 6.6
Z-352-BG	352	1.6/8	—	.4/2	—	—	+27.5 V @ .25/4.8 −27.5 V @ .25/3.5 +170 V @ 0/.5	Convection	A	11.5 x 11.5 x 4
Z-9-ED	9	—	—	—	—	—	+18 kV @ 20/500μA	Convection	C	5.5 x 4.4 x 2.5

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CIRCLE 54

(continued from page 100)

Session 8: Process Facilities

Wed 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: E. J. Adlard, Metcut Research Assocs, Inc

8/1 "Computer-integrated Composites Manufacturing: Its Role in the Transfer of Technology and the Perpetuation of Composites in the Aerospace Community"

8/2 "Robotic Arc Welding—HSLA Galvanized Steel"

8/3 "The Role of PCS in Industrial Data Highways"

8/4 "Facilities and Manufacturing Planning Using Integrated Computerized Technologies"

8/5 "Group Technology: A Pragmatic Approach for that First Step"

8/6 "The Road from Variant to Generative Process Planning"

8/7 "CAM-I's Experimental Planning System, XPS-1"

Session 9: Automated Assembly

Thurs 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: J. Dohner, CALMA Co

9/1 "Variable Compliance Concept and Its Application for Automatic Assembly"

9/2 "Computer Simulation and Control of Automatic Assembly Systems"

9/3 "Automation Systems in the Lighting Industry"

9/4 "Computer Technology—The Backbone of Electronic Assembly"

9/5 "Assembly Robot Language and Control Software"

9/6 "Robotic Application Development Using Interactive Tools and Fixtures"

Session 10: Managing the Introduction of New Manufacturing Technology

Wed 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: J. De Kriek, SofTech, Inc

10/1 "Technology—Can U.S. Management Meet the Challenge"

10/2 "Factory Integration: Lessons from Experience"

10/3 "Advanced Manufacturing Research—Foundation of the Future"

10/4 "Automation on the Manufacturing Floor—Who's Holding It Back?"

10/5 "Cost Benefit Analysis and Cost Benefit Tracking"

10/6 "An Insider's View of the Acquisition of CAD/CAM Equipment"

10/7 "The Automatic Factory: One Example and How It Grew"

Session 11: Material Handling

Wed 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: R. L. Dratch, Allen & Hamilton, Inc

11/1 "Handling Work-in-Process in Integrated Manufacturing Systems"

11/2 "Rapid Retrieval System for Robotic Kitting"

11/3 "The Application of Vision Systems in Materials Handling"

11/4 "FMS-Flexible Manufacturing Systems"

11/5 "Automatic Identification in the Factory of Today—and Tomorrow"

11/6 "Voice Data Entry System Applications: Three Case Histories"

11/7 "The Use of Sensors in Robotic Applications"

Session 12: Quality, Inspection, and Test

Thurs 10:45 am to 12:30 pm, and 1:30 to 4:30 pm

Chair: R. Paolino, Mechanical Technology, Inc

12/1 "Robot Body Inspection System"

12/2 "Computer Stock Verification"

12/3 "Robotic Testing and Inspection Applications"

12/4 "Machine Probe Applications"

12/5 "Primer for Computer-aided Quality Information Systems"

12/6 "Quality Assurance in the Integrated Computer-aided Manufacturing Environment"

Tutorials

Mon 6:30 to 9:30 pm

1. "Introduction to Robotics"
   W. J. Higgins, Prab Robots, Inc
2. "CIM—Integrating CAD and CAM"
   W. D. Beeby, William Beeby & Assoc, Inc
3. "Solids Modeling—Concepts, Requirements, Advantages, and Capabilities"
   R. E. Crowley, Consultant

Tues 6:30 to 9:30 pm

1. "Material Handling in the Automated Factory"
   Speaker to be announced
2. "CAD/CAM Implementation and Integration"
   K. C. Bonine, General Dynamics
3. "Applied Machine Vision"
   P. West, Automated Vision Systems
4. "Database Management"
   D. S. Appleton, D. Appleton Co, Inc

Wed 6:30 to 9:30 pm

1. "Automated Database Capture for CAD/CAM"
   Speaker to be announced □

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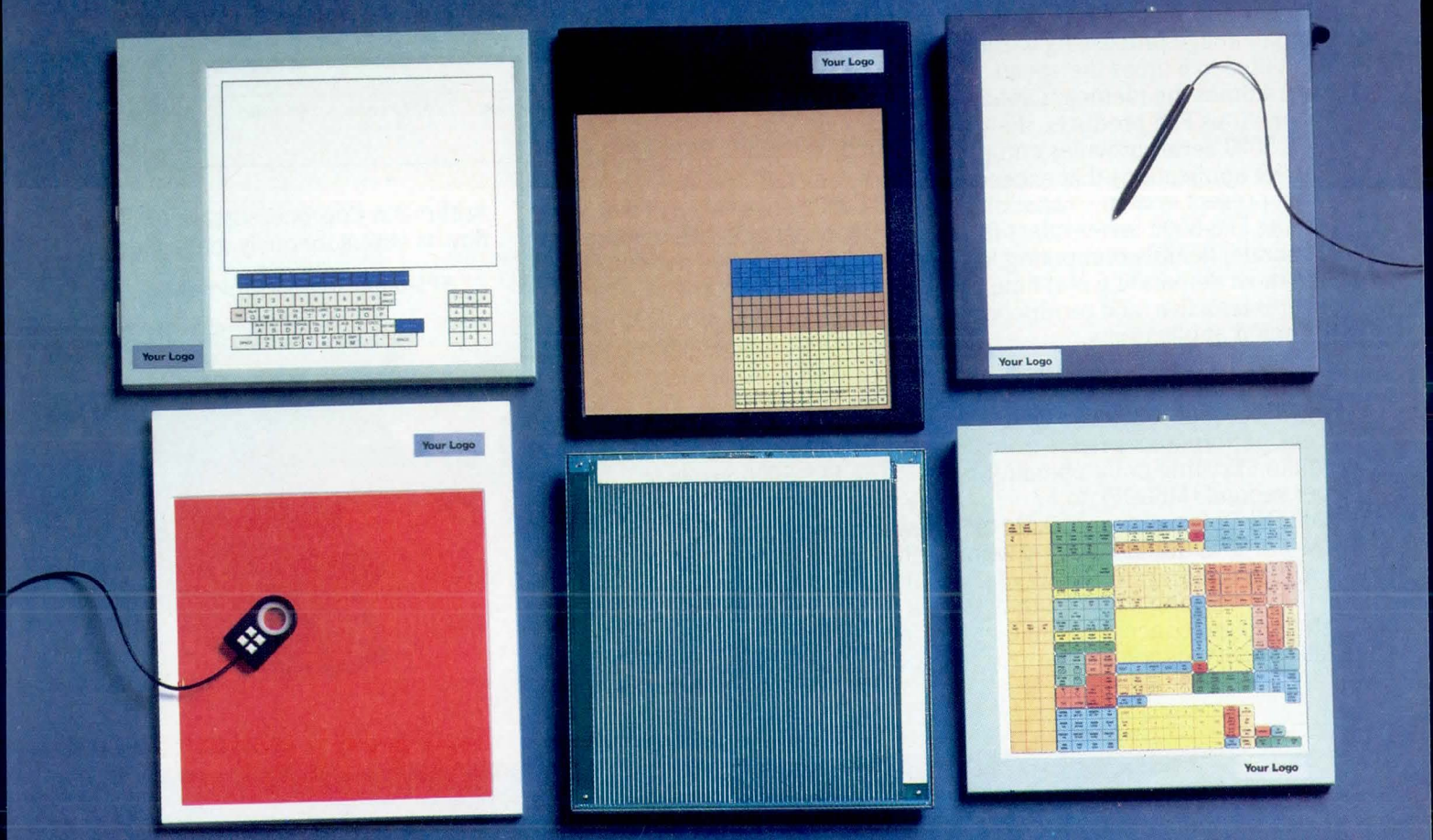

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CIRCLE 59

Floating Point Systems array processor to break

The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Typical performance examples of geophysical, medical imaging and signal/image processing applications.

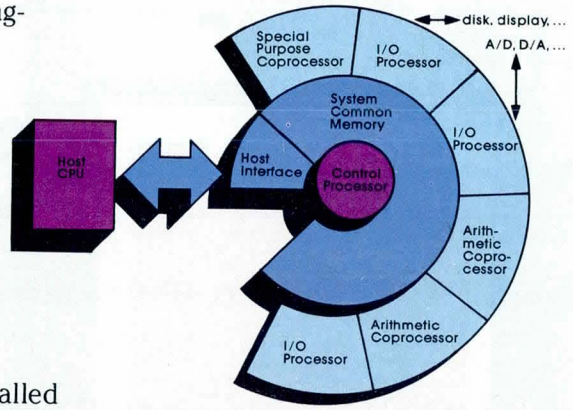
Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

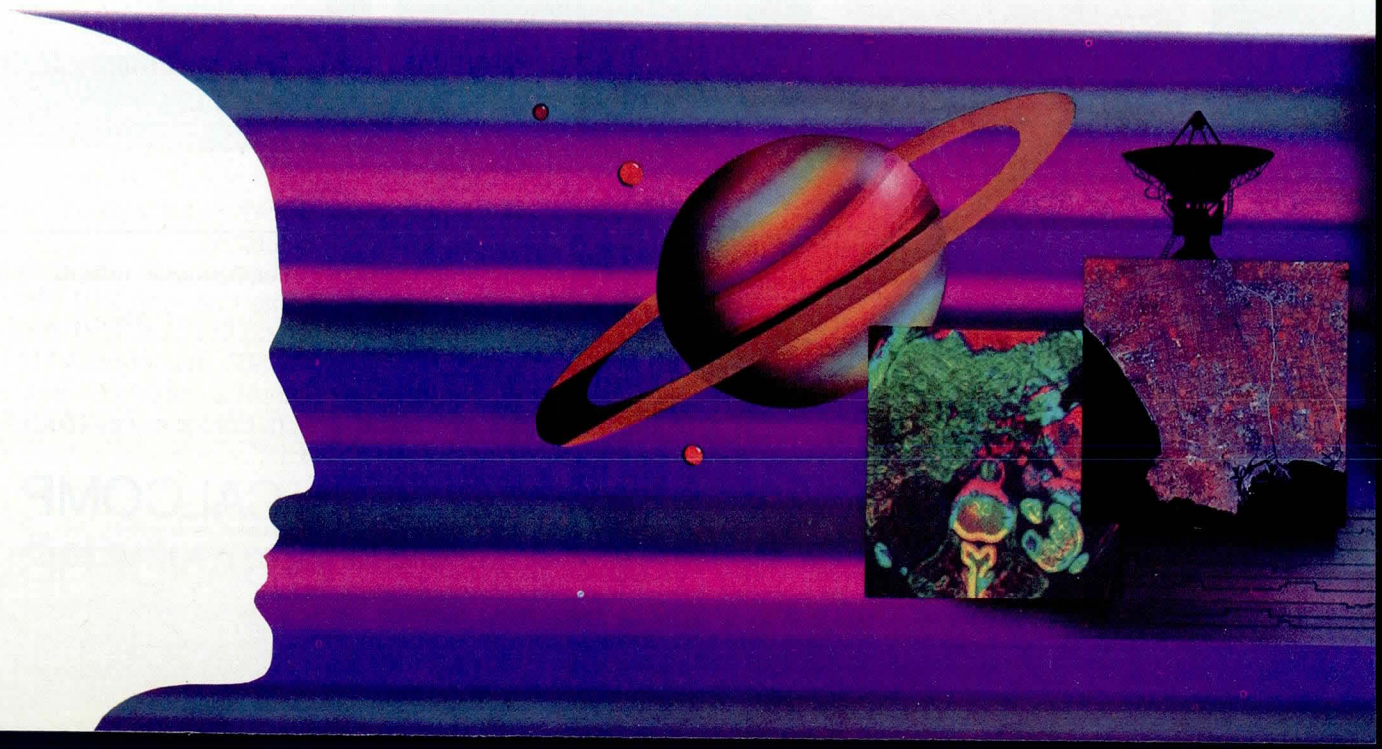
Based upon specifications subject to change.

Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed

FPS-5000 Series Architecture





introduces the first the $2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.

Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

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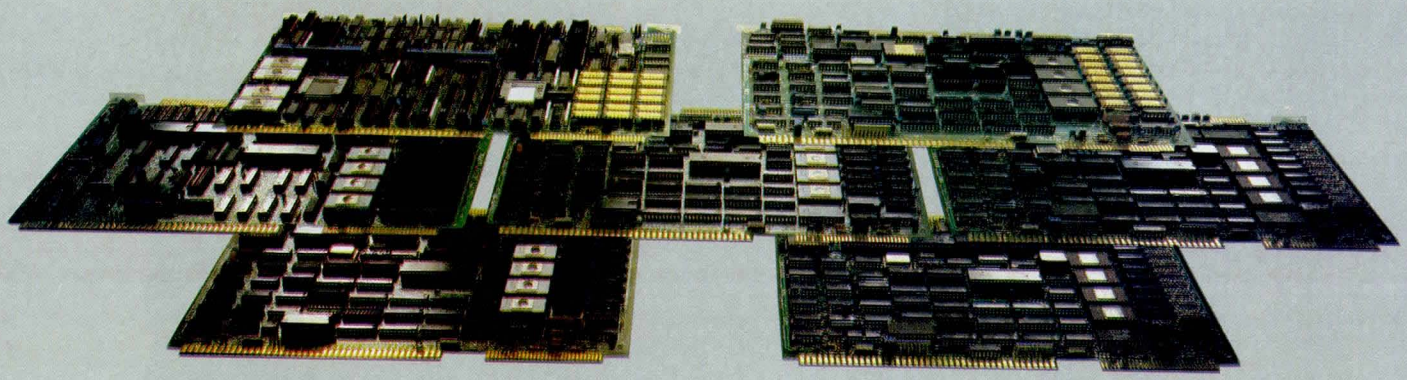

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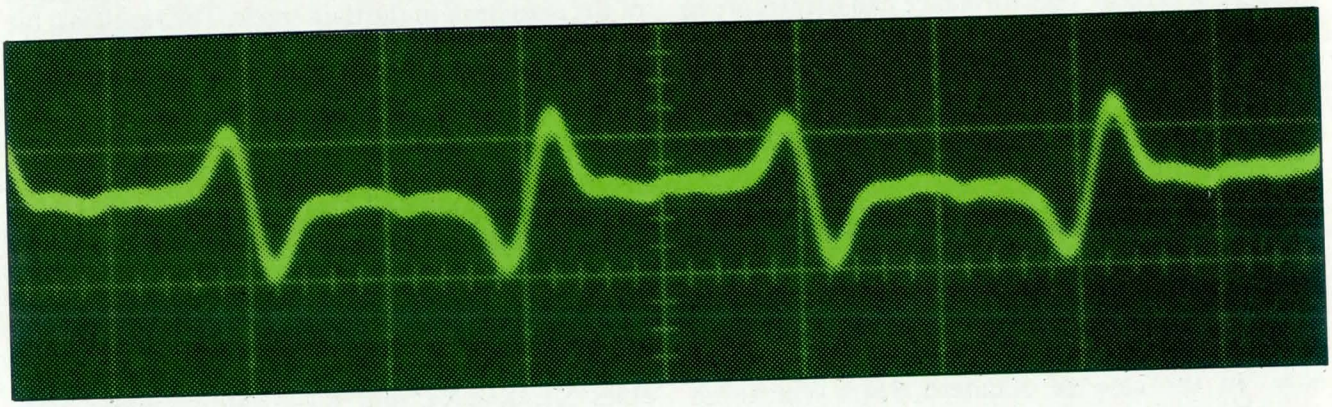
IMPROVING MASS STORAGE DATA INTEGRITY

Designers can do a lot to improve the reliability of the data being read from Winchester disks and other mass storage media. In fact, they should be doing more.



by Max Roth

Mass storage performance and reliability are tied to data integrity. However, even with error correction schemes, many recoverable errors impede throughput. Lost data affect performance even more dramatically. As 5¼" Winchester drive capacities and bit and track density increase, the read channel must be enhanced to maintain acceptable disk drive error rates.

Primarily, acceptable disk drive error rates are determined (somewhat arbitrarily) by disk technology rather than by predefined system requirements. Most 5¼" Winchester products support error rates of 1 in 10^{10} bits for recoverable (soft) errors. For nonrecoverable (hard) errors, 1 in 10^{12} bits is the norm. By definition, soft errors are recoverable by multiple read retries and therefore do not necessarily affect data reliability. Excessive soft errors, however, may degrade throughput because of multiple read retries. Nonrecoverable hard errors occur primarily as a result of defects in a disk's recording surface.

Data integrity can be maintained two ways. First, the system designer can maintain low error rates by using error correction code (ECC). ECC solutions vary dramatically in terms of redundancy required, correction capability, and miscorrection errors. Both hard and soft errors are correctable with ECC. However, it should not be used to correct soft errors where a particular code's miscorrection is greater than the probability of recovery from multiple read retries. On the other hand, ECC does offer significant data reliability improvement for detecting and correcting hard errors. Historically, though, few system designers have accepted the responsibility of maintaining data integrity.

Relying on disk drive manufacturers to assure low error rates is the second and traditional way to maintain data integrity. But many in the computer industry believe that disk drive manufacturers are unnecessarily carrying the primary burden for maintaining disk system data reliability. By providing nearly perfect disk media and sophisticated read/write (R/W) channels, disk manufacturers have maintained very low disk drive error rates.

Max Roth is a member of the technical staff at Vertex Peripherals Corp, 2150 Bering Dr, San Jose, CA 95131, where he is responsible for read/write channel and spindle motor control. Mr Roth holds a BS from the Technion Institute of Technology, Haifa, Israel.

System reliability could easily be maintained if the controller manufacturers/designers improve their own error correction schemes by using greater redundancy. They could also improve reliability by selecting ECC codes that increase correction capability while minimizing miscorrection. This would even be true with a significant increase in raw disk drive error rates. In any case, system manufacturers should implement ECC to guard against error rate variations among disk drives.

While system designers continue to rely on disk drive manufacturers to provide low error rates, the manufacturers must maintain these low error rates by using nearly perfect recording surfaces and a capable read channel. It is worth noting that data separation is an important read channel function. This feature is implemented in the disk controller for present 5¼" Winchester disk drives. Because the data separator's performance can contribute to data errors, future interface standards are incorporating data separation in the disk drive electronics rather than in the controller. This places full responsibility for data integrity on the disk drive manufacturer.

Causes of data errors

A data bit from the disk drive must be detected within a fixed length of time, known as the decision window. The data transfer rate and the encoding scheme determine the duration of the decision window. In the case of standard 5¼" Winchester drives, using a 5M-bps data transfer rate and modified frequency modulation (MFM) encoding, the decision window is 100 ns wide. Any bit undetected within this time period is considered an error.

In the ideal world where there is no interference and no noise, all data bits are centered within the decision window and no data errors occur. If intersymbol interference (pulse interaction) is considered, a bit shift or jitter occurs (no pulses are exactly centered but all are within the decision window). The amount of bit shift can be determined by superimposing adjacent bits. This amount is primarily a function of the encoding scheme used.

Noise and jitter intrinsic to the data separator also induce bit shift. Noise includes media head and electronic noise, overwrite modulation, and adjacent track interference caused by misposition of the read head in the data track. The result is a bit distribution superimposed on the bit shift due to pulse interaction. Mathematically, the bit shift (J = bit shift jitter) can be expressed as

$$J = X_1 + X_2 + X_3 + X_4$$

where

X_1 = zero-crossing jitter caused by noise
X_2 = intersymbol interference
X_3 = data separator window jitter
X_4 = mispositioning jitter

The nominal value of J is zero, as in the ideal case. Deviation from nominal is due to the variables X_1, X_2, X_3, and X_4. These variables have

Just what is ECC?

by Neal Glover
Data Systems Technology

Error correction code (ECC) allows data to be accurately reconstructed from encoded data that contain errors. These codes are used in computer and communication systems to increase data storage and transmission integrity.

An encoded data record typically contains a data segment that is identical to the raw data, and a redundant segment that is generated from the raw data by a generator polynomial. Dividing the encoded data by the generator polynomial is the first step in decoding. Data are assumed to be error free only if the remainder is zero. Usually, a nonzero remainder has enough information to allow the accurate reconstruction of the original data, provided that errors within the encoded record do not exceed the capability of the code being used.

ECC has guaranteed correction and detection abilities. Errors that exceed a code's guaranteed correction and detection capacities are subject to miscorrection. Miscorrection probability is a function of record length, correction ability, and redundancy. If some error types are more probable than others, polynomial selection can influence miscorrection probability.

Historically, most magnetic disk controllers have used single-burst correcting codes. Most of these controllers use reread to recover from temporary errors, and error correction to recover from hard errors. This technique maintains data accuracy with codes that use only a modest amount of redundancy.

Some new controller designs use more redundancy to implement more powerful codes, including multiple-burst correcting codes. In addition, error-tolerant techniques are being used for address marks, sync marks, and header information. Multiple-burst correcting codes and other error-tolerant techniques will likely be widely used in future disk controllers due to new pushes in disk technology, new defect philosophies, and the lower cost of large scale integration.

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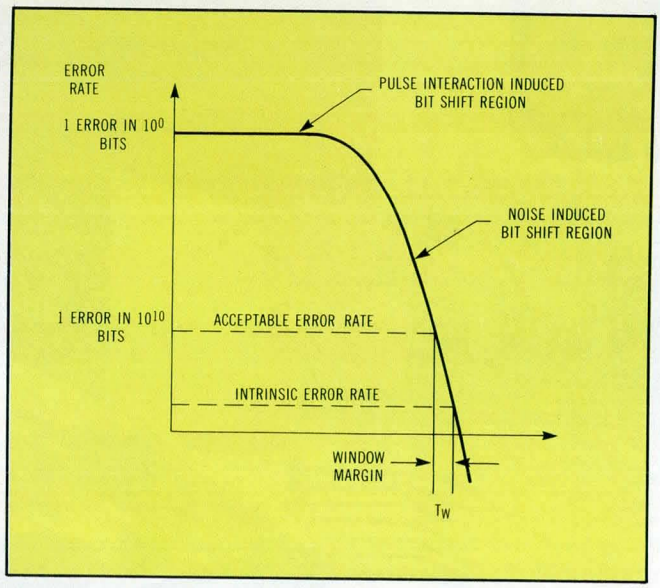

Fig 1 A marginal variable frequency oscillator (MVFO) plot is useful in determining error rate and margin information. The bit shift's relation to error rates and time is plotted with the goal of optimizing window margin (T_w) times.

mean value n (equal zero) and a symmetrical (with respect to n) probability density function (PDF). In most cases, the PDF can be approximated by a Gaussian distribution.

If the total bit shift jitter, J, is to satisfy a stringent requirement, the same holds for variables X_1, X_2, etc. A practical measure for the total jitter would be the variance of this function as derived from the variance of the variables.

Assuming that the input variables are not correlated and are normally distributed, the PDF for J will be a normal distribution. Since a read error occurs any time the zero-crossing or bit detection is outside the decision window, the probability of making an error is the area from a time (T_w) to infinity if the PDF of the zero-crossing jitter is Gaussian. (See the Bibliography for publications that support this assumption.)

If the decision window is varied, the number of errors will also vary. Errors can easily be plotted against variable decision window time. If the log of errors is plotted against a variable decision window, however, the resultant curve is referred to as a marginal variable frequency oscillator (MVFO) plot (Fig 1).

MVFO gets its name from the technique of varying the data separator window or decision window by marginal control of the data separator's clock frequency. Test equipment can plot MVFO curves for disk drives. The MVFO plot in Fig 1 shows the relative bit shift induced by both pulse interaction and noise.

Error rates are essentially 100% when the decision window is reduced to less than the bit shift time induced by pulse interaction. The intrinsic error rate is the best error rate achieved when using the maximum available decision window. By reducing the decision window until the acceptable error rate is measured, a window margin factor can be obtained. Note that any chosen acceptable error rate must be higher than the read channel's intrinsic error rate. An MVFO plot can be generated for any disk drive. It is also a useful tool in characterizing error-rate performance.

If data rates are fixed, as in present 5¼" Winchesters, then higher track density achieves increased capacity. Thermal expansion between servo surface and data surfaces, bearing noise (referred to as "nonservoable" mechanical errors), and servo tracking errors limit track density. The density of recently introduced 5¼" Winchesters is approximately 1000 tpi, as opposed to 300 to 400 tpi in low capacity drives.

Ontrack and offtrack adjacent interference are primary contributors to the bit shift noise component. Fig 2 illustrates the ontrack and offtrack interference mechanism. Offtrack interference [Fig 2(a)] is due to signal noise picked up by the R/W head from the adjacent track as a result of head-to-track misposition. Ontrack interference [Fig 2(b)]

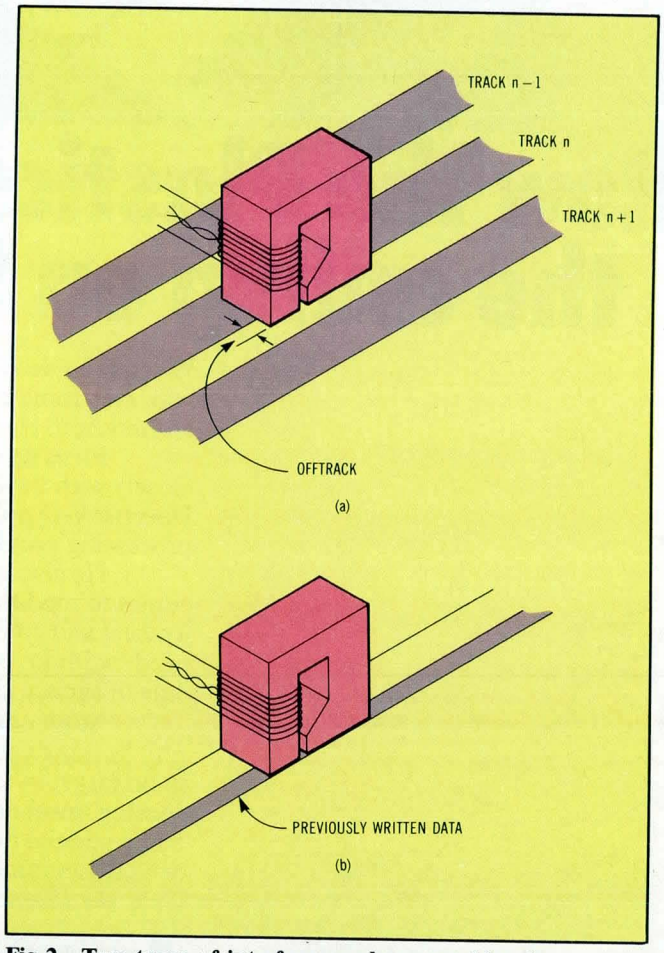

Fig 2 Two types of interference plague read heads. Offtrack interference (a) is caused by the pickup of adjacent track data. Ontrack interference (b) is caused by previously recorded information that was not precisely centered on track.

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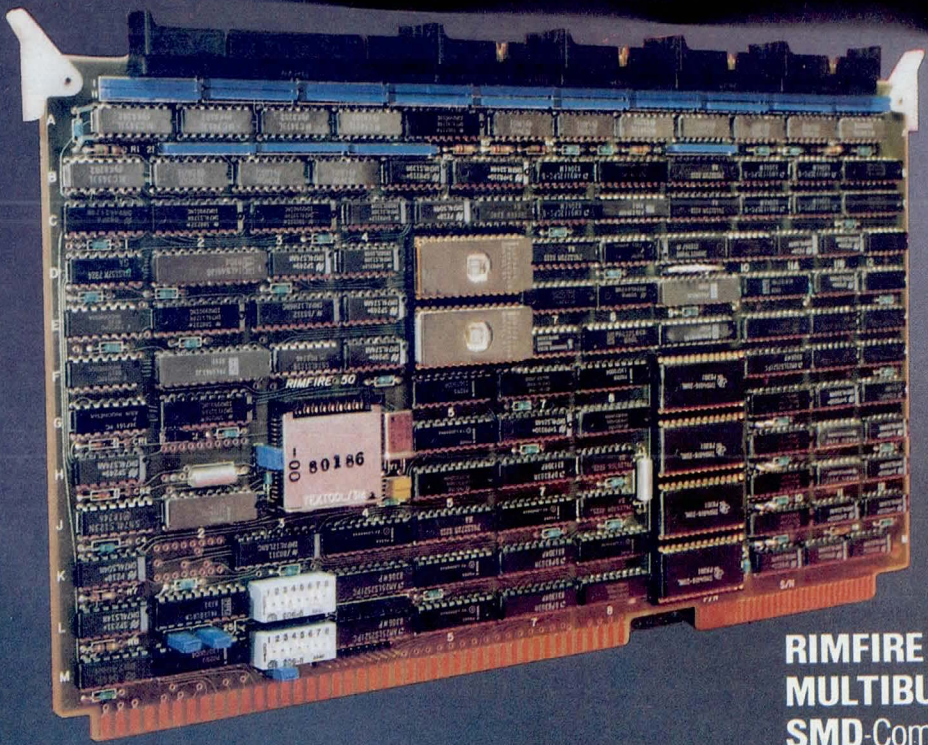

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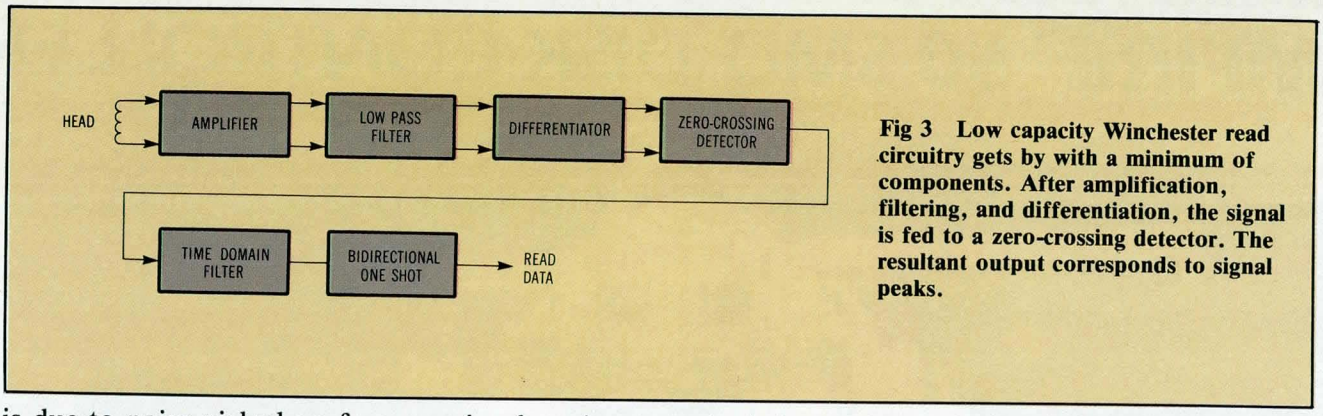

Fig 3 Low capacity Winchester read circuitry gets by with a minimum of components. After amplification, filtering, and differentiation, the signal is fed to a zero-crossing detector. The resultant output corresponds to signal peaks.

is due to noise picked up from previously written data on the same track, where the overwrite was not precisely centered. The read channel must accommodate approximately 12% misposition of head to track to maintain an acceptable error rate. It is up to the disk drive mechanical and servo systems to ensure that head to track misposition is maintained at less than 12% of track pitch.

A read channel rationale

In simple form, a drive's read channel amplifies the signal emanating from the magnetic read heads. However, read channels are becoming increasingly complex and vital to data reliability as 5¼ ″ Winchesters grow in capacity and performance. Today's high capacity drives operate at up to 960 tpi. They use much less signal energy and have higher noise interference susceptibility. For example, the Vertex V100 series generates a signal of 0.4 to 0.8 mV peak to peak, versus 2 to 5 mV for a typical low capacity drive.

Obviously, read channel design becomes mor[9] critical in the higher capacity unit. In addition, many high capacity drives operate with varied encoding schemes, such as run length limited (RLL). These schemes are more efficient, but they also require greater bandwidth than MFM encoding. Unfortunately, greater bandwidth channels are more susceptible to noise.

Fig 3 illustrates a typical low capacity 5¼ ″ Winchester read channel control circuit. The readback signal picked up by the head is amplified and then differentiated after it is filtered by the low pass filter. The zero-crossing detector output corresponds to the readback signal peaks. In the high resolution case, false detection can occur due to a droop in the differentiated signal. A time domain filter solves the problem by ignoring those pulses. However, this solution is sensitive to the encoding scheme used.

To achieve low error rates and allow flexible selection of recording codes, several circuit elements can be incorporated into modern Winchester hardware. Signal preamplifiers located on the actuator arm, near the R/W heads, improve the signal-to-noise ratio by amplifying the signal before additive noise is introduced. Automatic gain control (AGC) compensates for variations in head signal amplitude. These variations are caused by normal variations in head flying height and differences in the efficiency of media and heads. Signal qualifier circuits ensure accurate data detection.

The signal qualifier circuit couples a peak detector with a zero-crossing detector. The peak detector accurately determines the position of the peaks in the time domain. By correlating those peaks with the zero-crossing detector output, the pulses that are caused by noise can be rejected. As the frequency span of the recording code is enlarged, the probability of false zero-crossing detection becomes higher.

While the MFM frequency ratio is 1:2, it can be as high as 1:4 in some RLL codes. Therefore, a peak detector scheme is less code dependent than a time domain filter. Fig 4 illustrates the qualifier circuit's effectiveness and shows an actual signal from the R/W head after preamplification. The differentiated signal shows significant deflections near the zero crossing.

If a zero-crossing detector circuit is used without signal qualification, the resultant data out are not usable. With signal qualification, nondata induced zero-crossing pulses are eliminated, leaving usable data out. Although these circuit elements are not generally found in low capacity 5¼ ″ Winchesters,

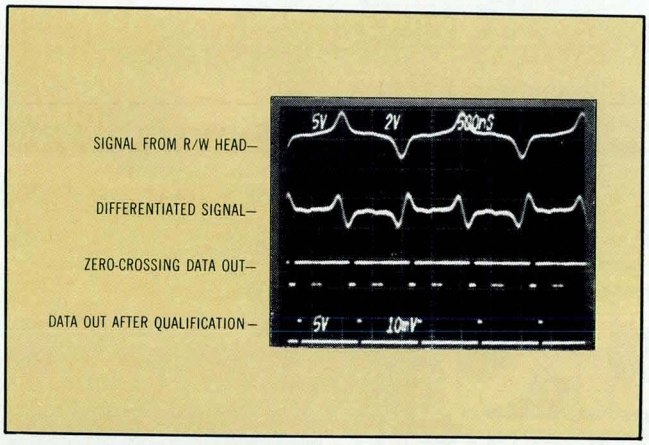

Fig 4 By eliminating false zero-crossing frequency components, reliable data are ensured.

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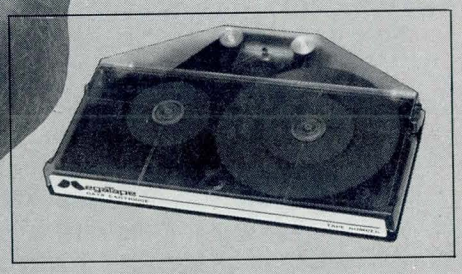

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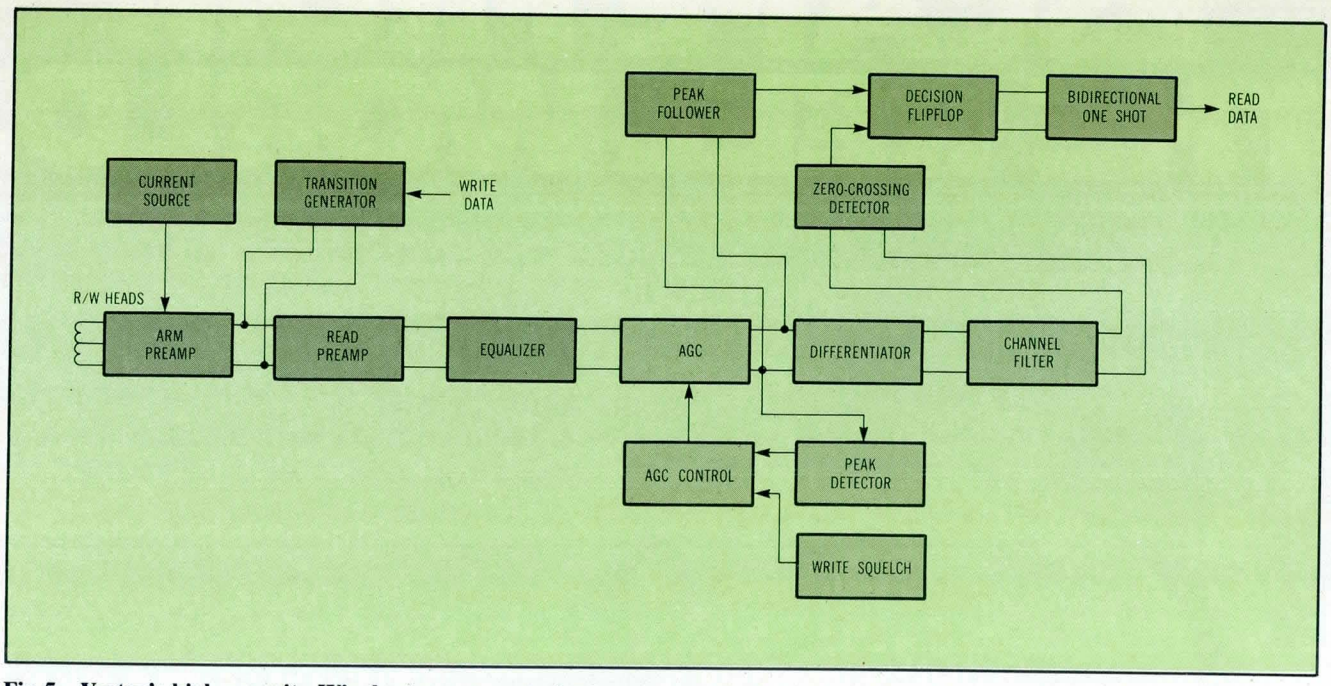

Fig 5 Vertex's high capacity Winchester R/W control takes an equalized signal output of the AGC amplifier and differentiates, filters, and digitizes it. A peak follower circuit processes this signal and, in conjunction with a zero-crossing detector, generates read data.

they are common in high capacity, high performance disk drives such as the IBM 3380.

The control block diagram of the V100 series read channel incorporates the elements described (Fig 5). In the V100 read channel, a preamp located close to the head itself amplifies the head signal. The amplified signal is applied to the read preamp via a balanced transmission line. After amplification, an equalizer modifies the signal spectrum. An AGC amplifier holds the signal at a constant amplitude to allow for head output variation and amplifier tolerances. AGC amp output is differentiated, filtered, and digitized by the zero-crossing detector. Then, after qualification by the peak follower, these data are available for reading.

Sophisticated read channel implementations will become increasingly important as 5¼" Winchester drive capacity and performance increase. Track and bit densities will continue to rise with improvements in magnetic head and media technologies. New encoding schemes and higher transfer rates will further enhance 5¼" drive performance. However, read channel implementation will make or break small drive data reliability in the near term, by amplifying and accurately differentiating the signal from the drive's R/W heads. The exceptions will occur when controller manufacturers take on an enlarged responsibility for implementing ECC.

In the foreseeable future, 5¼" drives will use enhanced equalization along with the ability to modify particular frequencies of the readback signal spectrum. This capability is essential to vertical recording schemes. Adaptive filtering will also be implemented using a microprocessor to change the bandwidth of a channel as a function of the head's position on the disk. Finally, enhanced signal processing, using correlation techniques adapted from radar technology, will allow accurate processing of signals in even worst-case signal-to-noise conditions.

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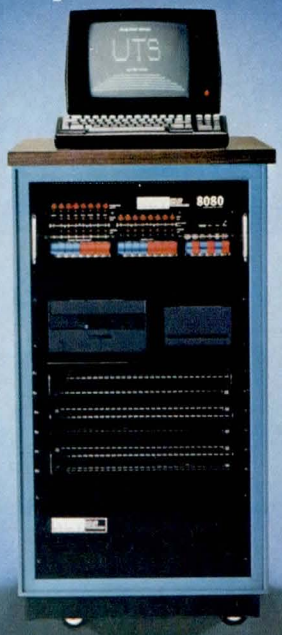

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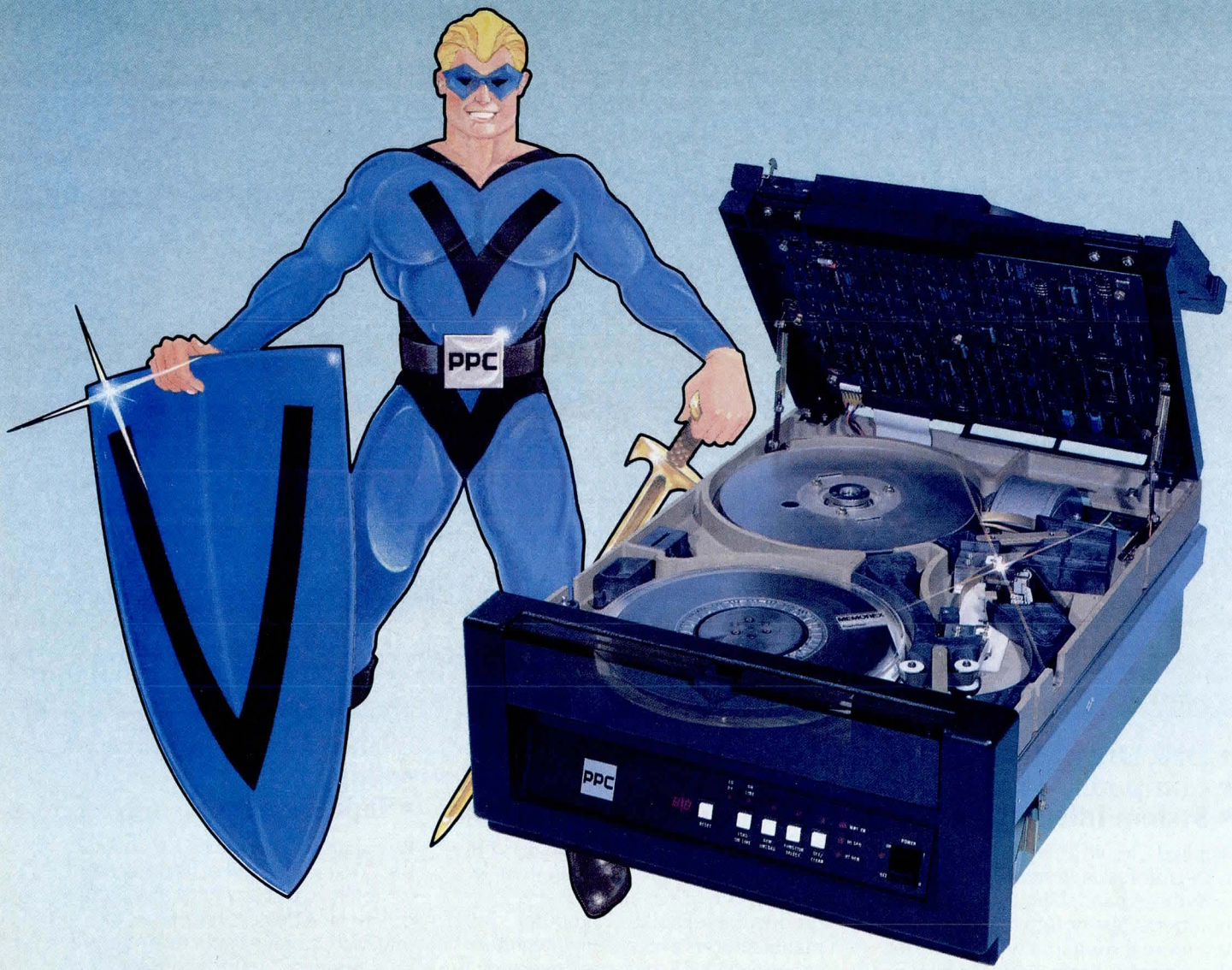

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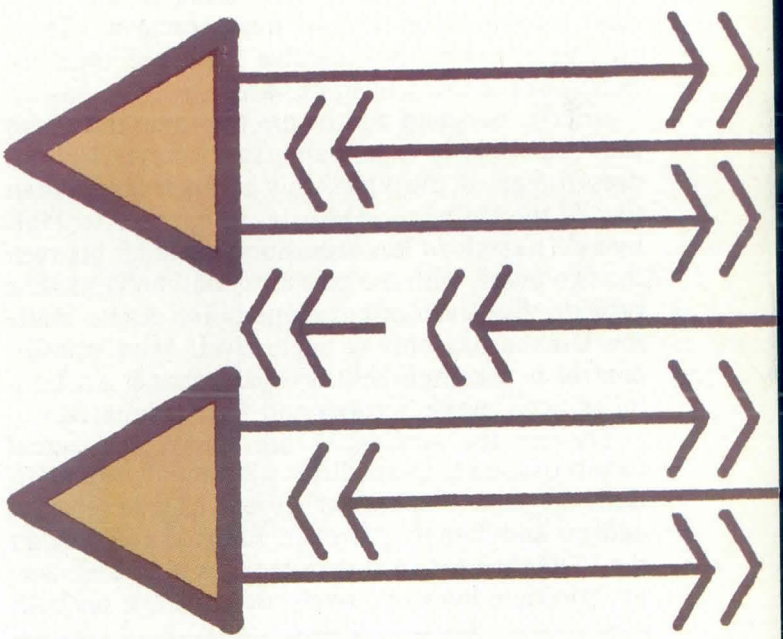

by Roger R. Russ

One of the most salient characteristics of the computer industry is the relentless advance of its technology. Hardware size shrinks, cost per bit plummets, computing power explodes, and overall performance soars. This rapid evolution presents the industry with unique problems, and designers with difficult choices. Often a choice must be made between a product exhibiting high performance but little support and another boasting excellent support but less than state-of-the-art technology.

A central architectural feature of most advanced computers is some kind of data transfer bus. And, each type of bus has a specified number of data bits, an address range, and control signals defining its acquisition and use of protocols. Each system element—the central processing unit (CPU), memory, and input/output (I/O) devices—must interface with the data transfer bus. Hypothetically, an interface between two different data transfer buses could link a high performance bus to a widely supported product, giving designers the best of both worlds.

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In such a scheme, a lower performance host can offload time-consuming tasks to a high performance microprocessor. This can free host CPU resources and increase overall performance. In addition, this approach allows dedicated microprocessors to perform mundane data processing, networking, or other computational chores. A system integrator working with a developed product can also take advantage of such a bus interface for development purposes by allowing new technology to be incorporated in an existing system. Development efforts using entirely new technology also have uses for such a hybrid interface. In this case, the designers latest brainchild can be structured with an interface to another bus to take advantage of a wider range of I/O devices, software, or product support.

A system configuration encompassing two different levels of performance is depicted in Fig 1. Here, each bus has its own CPU, memory, and I/O devices. Each bus also has its own rules for arbitration, use, data path width, and address range. The problems involved in the design of an interface for such a system revolve around the differences in these parameters. Differences in data path width or address bits point to relatively straightforward design solutions. However, the differences in control structures pose more difficult problems.

The UNI/VERS concept is an example of an interface linking two dissimilar buses. This interface provides a link between the Digital Equipment Corp Unibus and the more recent Motorola VERSAbus. The Unibus and VERSAbus share a common philosophy. Both are asynchronous, and both follow similar rules for direct memory access (DMA) and interrupt cycles. Despite this similarity, there are considerable differences in implementation and performance. The Table, "Bus Comparison," presents a comparison of chief bus parameters. These parameters exert considerable influence over the design of the UNI/VERS interface.

Briefly, the data widths are the same (although the VERSAbus is expandable to 32 bits). The address range of the VERSAbus is much larger than that of the Unibus—16M bytes as opposed to 256K bytes. The style of bus acquisition is similar between the two buses, with the exception that the VERSAbus provides five levels of bus requests and grants, while the Unibus has only a single level. Data transfer control is accomplished in a like manner on both buses, with master strobes and slave responses.

Though the similarities are many, the actual details of data transfer differ substantially. In addition, the VERSAbus master strobes include separate address and data byte strobes. Parity is available on the VERSAbus for each data byte, as is address parity. Multiple interrupt levels are available on both buses, with seven levels on the VERSAbus and four on the Unibus. Finally, deskewing time is typically 150 ns on the Unibus and 20 ns on the VERSAbus.[1,2]

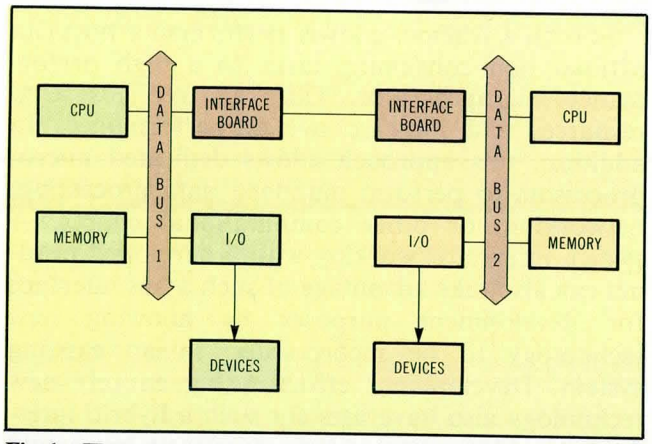

Fig 1 The generic bus interface strategy involves providing common, as well as specific, hardware resources to each bus. Control problems pose the greatest threat to such a system, especially when bus performance differs markedly.

Bus Comparison

Parameter	Unibus	VERSAbus
Address	A(00-17)	A(01-24)
Data	D(00-15)	D(00-15)
Bus acquisition control		
Requests	NPR	BR(0-4)
Grants	NPG	BG(0-4) IN/OUT
	SACK	
	BBSY	BBSY
		BCLR, BREL
Bus transfer control		
Master strobes	MSYN	AS, DS(0-1)
Slave strobes	SSYN	DTACK, BERR
Parity	PA, PB	DPARITY(0-1), DPVAL APARITY(0-1), APVAL
Control bits	C(0-1)	LWORD, WRITE
Interrupts	BR(0-4)	IRQ(1-7)
	BG(0-4)	
	ACKIN/OUT	ACKIN/OUT, A(01-03)
Utilities		
Reset	INIT	SYSRESET
Power monitor	ACLO, DCLO	ACFAIL
Other utilities		ACCLK, SYSCLK
		SYSFAIL, TEST(0-1)
Deskewing time	150 ns	20 ns

Making design choices

These bus characteristics dictated several design criteria and strategies. The first was the memory mapping of the Unibus's entire address range onto the VERSAbus. The reason for this is the VERSAbus's much larger address range. This decision has several operational consequences. Primarily, it makes any Unibus cell appear to be a normal memory location from the point of view of any VERSAbus master. Since both buses are asynchronous, transfers merely take longer.

The UNI/VERS may be thought of primarily as a DMA device that does memory to memory block moves on the VERSAbus. In DMA mode, the UNI/VERS is master on each bus in succession. Since the Unibus is memory mapped, VERSAbus to Unibus moves are merely moves to specific addresses. From the point of view of a VERSAbus program, there is nothing unique about Unibus accesses.

DMA transfers are not the only mode that the interface can assume. The UNI/VERS can also assume the transparent mode, allowing any VERSAbus master direct access the Unibus. In this mode, the UNI/VERS acts as a slave on the VERSAbus and a master on the Unibus. Transparent mode has no

restrictions. It can even occur during a DMA block move. In addition, the transparent mode cycle can be interleaved with DMA cycles.

Memory mapping the Unibus places most of the control information on the VERSAbus side of the interface. Individual cycles are always generated from the UNI/VERS VERSAbus board (V-board). Thus, the relationship between the two boards in the interface can be thought of as a master/slave relationship. The UNI/VERS Unibus board (U-board) is always the slave within the interface, even though it is a Unibus master in DMA and transparent modes.

The interface is neither symmetrical in design or operation, nor is there a method for a Unibus master to directly access a VERSAbus cell. This situation led to another design choice that facilitates initiation of DMA moves by the Unibus CPU. A set of 16 dual-ported I/O registers reside in the interface for process to process communication. There are 15 user definable, soft registers, and 1 predefined register. These communication registers occupy user selectable I/O addresses on each bus and can support a variety of user defined protocols.

Hence, from the Unibus software's standpoint, the UNI/VERS system can appear to be a normal DMA device. The Unibus process can load address, block length, and status information into the communication registers. Then, by setting a bit in the first register, the Unibus process can interrupt the VERSAbus process. The interrupt handler on the VERSAbus can then read the communication registers, set up the DMA controller on the V-board, and initiate the transfer.

The protocol employed causes the UNI/VERS to appear to be a multiple asynchronous DMA device on the Unibus. The Unibus CPU places parameters into the communication registers and interrupts the VERSAbus processor. The VERSAbus processor will send status signals indicating the information has been accepted. Later, it will interrupt the Unibus again with completion status signals. However, between these two interrupts, the Unibus may send new DMA parameters, and multiple DMA moves may be pending at the same time.

Other protocols can be supported as well, including synchronous protocols or simulations of standard Unibus DMA devices. Note that, although the hardware implies a master/slave relationship between the VERSAbus and the Unibus, the UNI/VERS system appears to be a standard DMA device on the Unibus from the software's point of view.

Interrupts and controller implementation

Another design decision follows from the use of the communication registers. This is the ability of either CPU to interrupt the other. The first communication register contains bits that, when set, cause an interrupt. There are 2 bits available for each processor, and each bit has a unique user selectable vector. These interrupts define two logical channels. They can be used to simulate a DMA channel in each direction, or a parameter acceptance and DMA completion interrupt. They can also provide dual DMA channels for multiple processors on the VERSAbus, or support for a variety of protocols. In this respect, the interrupts are completely flexible.

The next design choice involved DMA controller implementation. While a 68000-based DMA controller is currently available (in sample quantities), when UNI/VERS was designed no DMA controller was available. As a result, the UNI/VERS DMA controller was implemented with transistor-transistor logic (TTL) registers and counters. The main reason for this approach is high throughput. Transfer rates on the VERSAbus are much faster than those on the Unibus, and TTL offered the best chance of achieving these high rates. Consequently, the style of the V-board is asynchronous logic composed of registers, counters, and gates. The disadvantage of this approach is that many TTL packages are used in place of what might have been a single 64-pin package.

Since space is at a premium on any board, the style of the DMA controller is simple. The DMA controller is composed of five registers and has a limited set of operating modes. It is also easy to program and use. The implementation does achieve high transfer rates on the VERSAbus. This has led to some interesting applications not originally envisioned for the interface. For instance, because it does VERSAbus to VERSAbus moves so quickly, it has been used as a DMA device for block moves on the VERSAbus only.

It is anticipated that the U-board will be used in a variety of applications.

A design consequence of the high speed on the VERSAbus is the manner in which cycles on both buses are used. Since Unibus memory cycles take longer than VERSAbus cycles, each cycle occurs in succession. During VERSAbus to Unibus transfers, the VERSAbus does not wait for the Unibus cycle to complete. Instead, VERSAbus data are read into the DMA controller's data register. At this time, the VERSAbus is released if there are any requests pending for bus use. Then, a Unibus cycle is requested, and the transfer takes place after the Unibus request is granted. This allows the controller to provide bus cycles at the rate of each bus, rather than to force a busy-wait state on each bus for both cycles. This makes the UNI/VERS a fast VERSAbus DMA controller. The UNI/VERS is a release-on-request bus master on the VERSAbus and a cycle-at-a-time bus master on the Unibus.

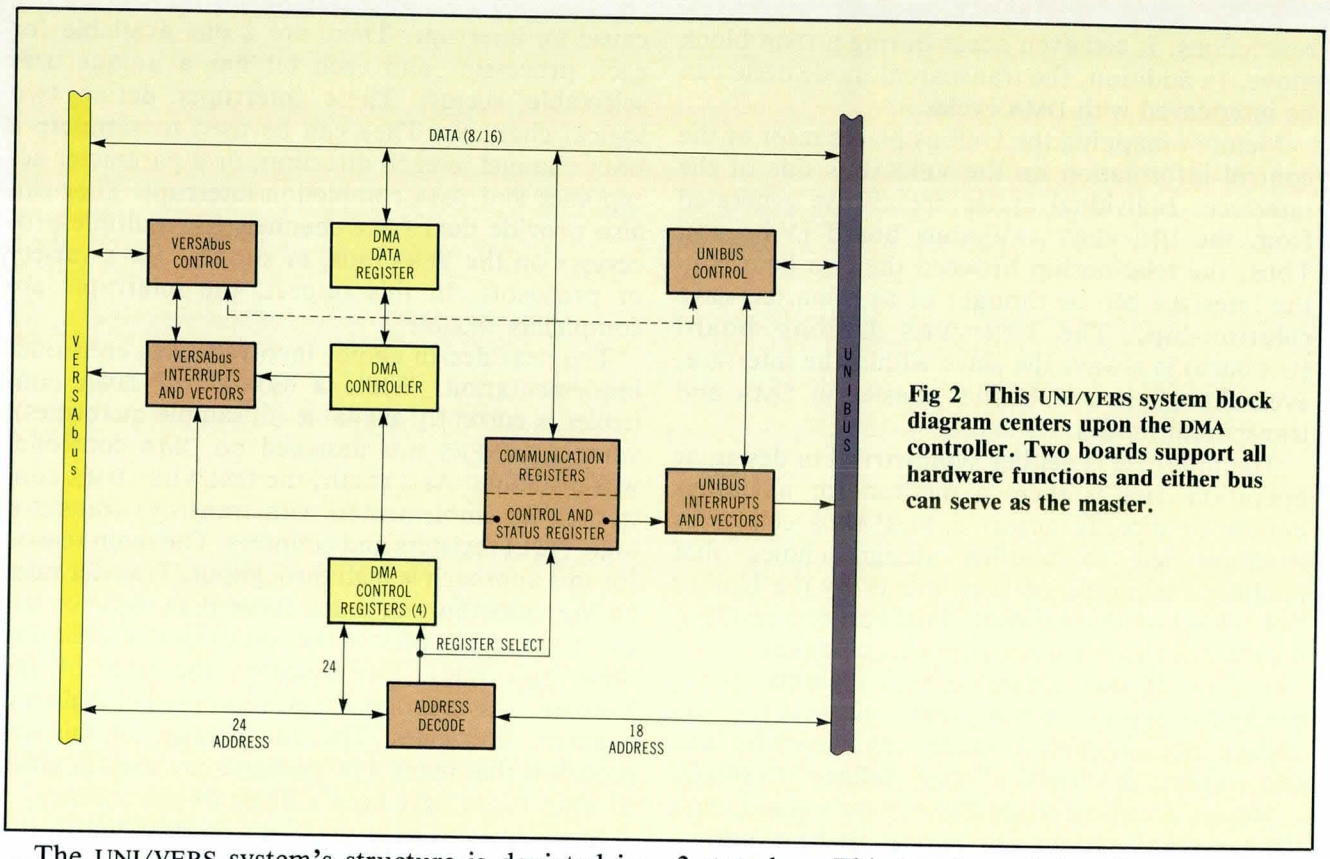

Fig 2 This UNI/VERS system block diagram centers upon the DMA controller. Two boards support all hardware functions and either bus can serve as the master.

The UNI/VERS system's structure is depicted in Fig 2. This diagram represents the elements of the UNI/VERS from a software perspective; the main functional element is the DMA controller. The initiation of action occurs by command of a CPU on the VERSAbus. This CPU initializes address counters, the transfer counter, and the control register. Then the "Go" bit is set in the control register, enabling the DMA controller. If the transfers are from the VERSAbus to the Unibus, the controller reads VERSAbus locations and deposits the data into its DMA data register. A Unibus cycle is then requested, and the cycle takes place under the auspices of Unibus control. Transfers continue in this manner until the last data element is written to the Unibus, causing a completion interrupt to be posted on the VERSAbus. The communication registers can be reached from either bus via the data path depicted in the diagram. The last important element from the perspective of Unibus software is the ability to post interrupts on the Unibus.

Building the boards

The V-board contains a rich VERSAbus interface, with logic supplied to support VERSAbus slave, master, bus requester, and interrupter modules (Fig 3). After initialization of the DMA registers, the block labeled "master cycle control" is enabled. The DMA registers include the DMA control register, source address register, destination address register, transfer count register, and data register. Each register is attached to an internal 3-state bus. This bus is used for all slave transactions with the DMA register, all VERSAbus master cycles by the DMA controller, and all transparent mode cycles.

Since this is a multipurpose bus, provisions are made for separate control of internal cycle arbitration. During DMA cycles, one of the two address registers is always the source of the current address. The current cycle is internally recognized to be either a source or destination cycle, so the proper choice is made in the block labeled "address selection." The address is either driven onto the VERSAbus or onto the U-board where it will be used on the Unibus.

Connection between the boards is accomplished through a set of differential drivers and receivers, in an effort to obtain good noise immunity. The particular drivers and receivers chosen have TTL 3-state outputs. Hence, the differential data inputs and outputs are actually a differential 3-state bus. This reduces the total number of wires needed for the interface cable.

Further, the choice of differential drivers and receivers allows considerable flexibility in cable length. The interface is manufactured with a 12′ (4-m) cable. This length should be adequate to establish a connection between a host computer cabinet and an adjacent cabinet or a tabletop. Theoretically, it is possible to drive a 4000′ (1392-m) cable; however, this has not been tested. Cable lengths up to 300′ (91 m) should not greatly affect throughput, and 500′ (152-m) cables have

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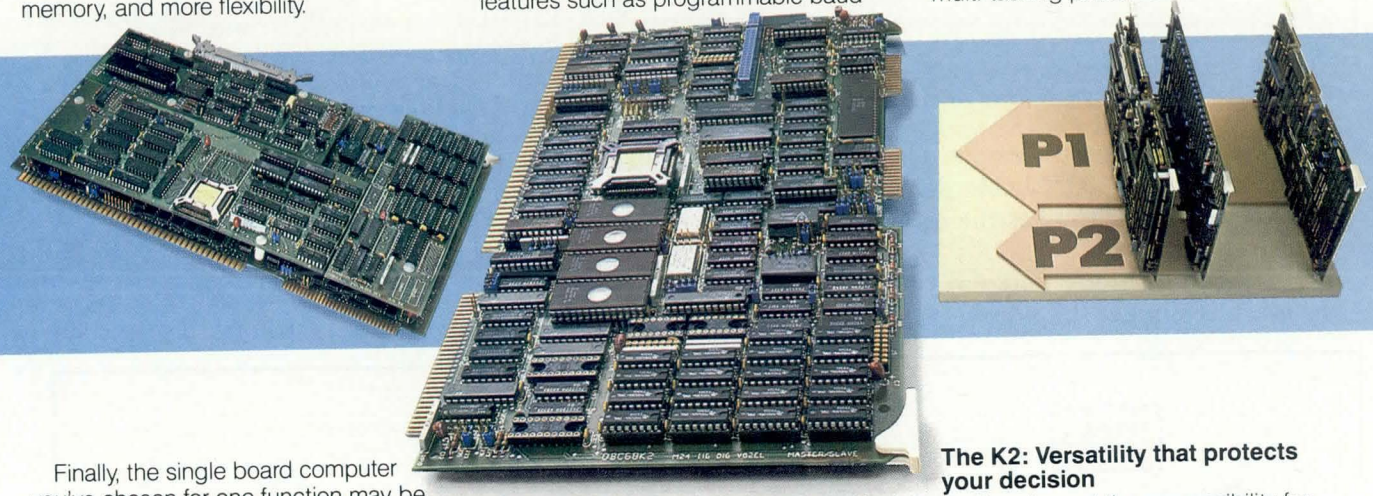

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CIRCLE 66

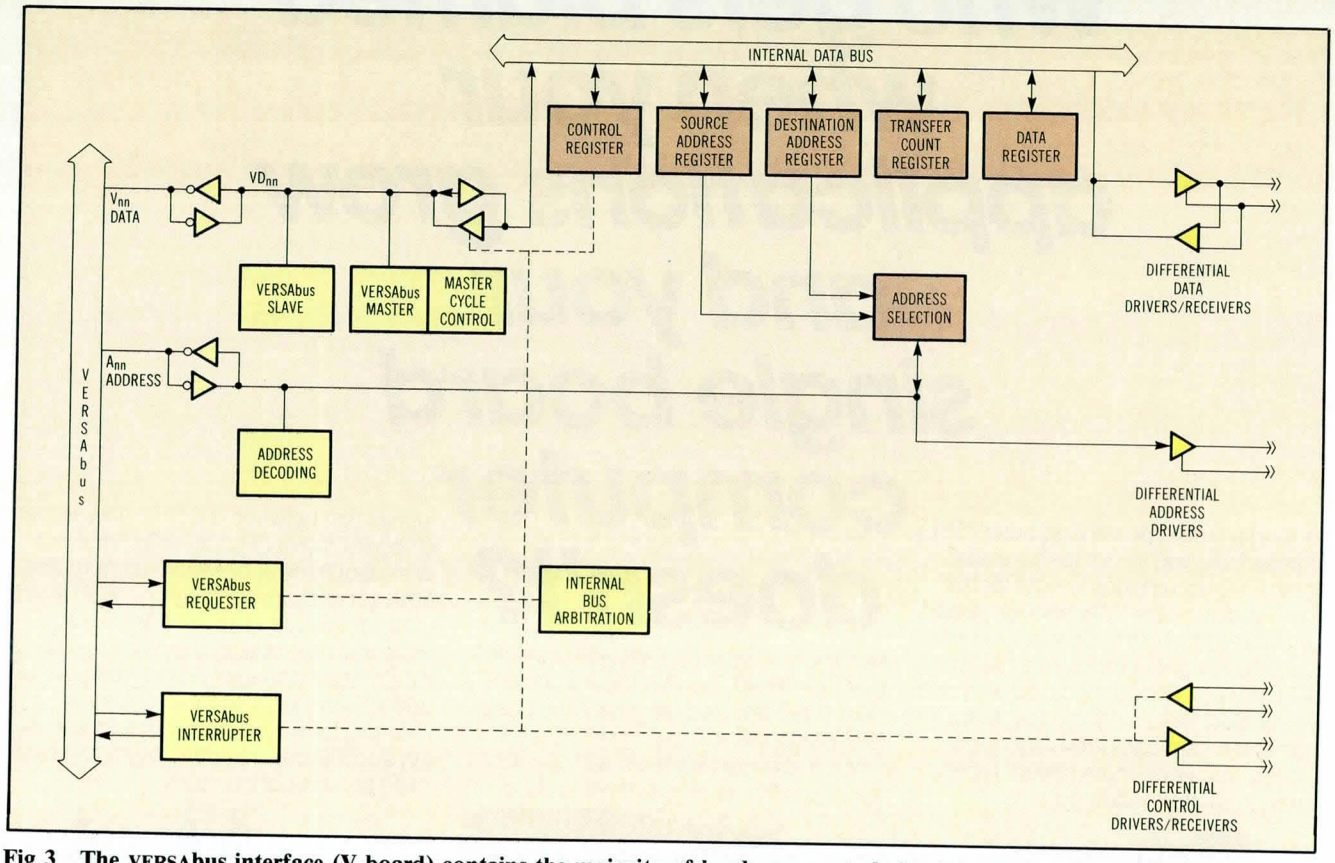

Fig 3 The VERSAbus interface (V-board) contains the majority of hardware control circuitry. It features an internal 3-state bus for communications, and solid-state drivers (TTL) that provide plenty of punch for longer cable runs.

been tested without data errors occurring. However, in runs over 300′, cable delays are on the same order of magnitude as the delay through the interface itself.

Fig 4 shows a block diagram of the U-board. This board is simpler than the V-board and is controlled by a finite state machine. A state machine is used in order to reduce the package count on the board, and the 75-ns state machine clock facilitates the deskewing time on the Unibus. While this approach is not as time efficient as discrete logic, 500k-byte/s throughput can be achieved on the

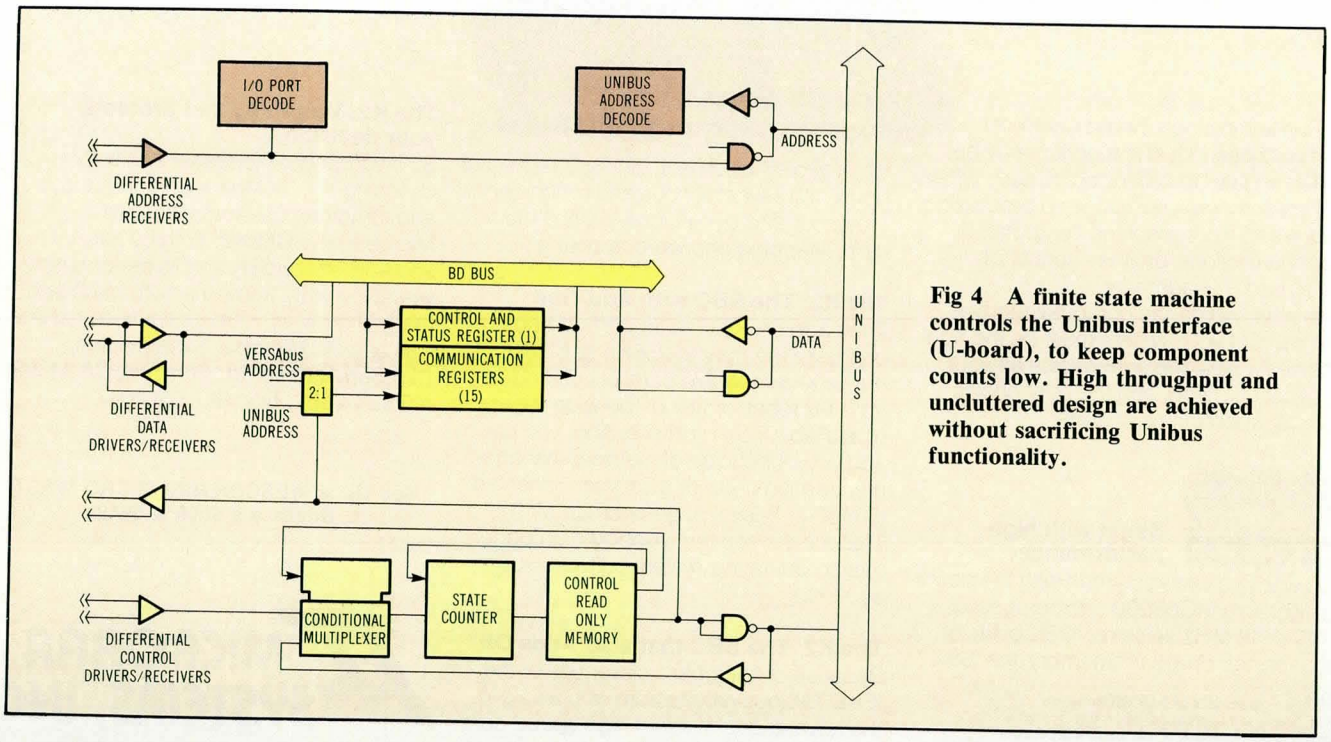

Fig 4 A finite state machine controls the Unibus interface (U-board), to keep component counts low. High throughput and uncluttered design are achieved without sacrificing Unibus functionality.

Unibus with this structure. This rate is a practical limit on the Unibus for any specific DMA device if Unibus saturation is to be avoided.

Other elements in Fig 4 include the differential drivers and receivers for the V-board, the communication registers, and the actual Unibus interface circuits. Some decoding must be done on this board for communication register accesses from the Unibus. This board also contains an internally buffered 3-state bus, the BD bus.

It is anticipated that this interface will be used in a variety of applications. Any VERSAbus-based system can be easily linked to a host PDP-11, or VAX, via the UNI/VERS. Originally, the reason for UNI/VERS development was to link a VERSAbus-based IBM channel control unit to the Unibus. With the existing VERSAbus hardware, this link was easy to establish using the UNI/VERS. The entire VERSAbus-based system consisted of the IBM interface, a VERSAbus microprocessor, and 256K bytes of random access memory on the VERSAbus. This is an intelligent interface meant to establish a vehicle for process to process communication on the IBM computer. With the addition of the UNI/VERS, the IBM interface increased its functionality. The process to process communication now includes processes residing on the Unibus. In the case of a PDP-11/34 serving as a network front end for the IBM 370, a powerful interface was created by adding the UNI/VERS.

The company is also developing various network and local area network interfaces that are VERSAbus boards. Since all these boards have the VERSAbus in common, a variety of system configurations and attachments can be made. For groups doing microprocessor development, this is an important feature. With board level products designed for VERSAbus attachment proliferating, the development of new interfaces and new systems changes the very nature of the VERSAbus. Further, the development process is not necessarily one of concurrent hardware and software progress. Instead, the effort is one of software integration with existing hardware. As more VERSAbus products are introduced, only the software effort needed to achieve integration will limit the types of systems possible.

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2. *VERSAbus Specification Manual,* Motorola Inc, 1981.

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CIRCLE 67

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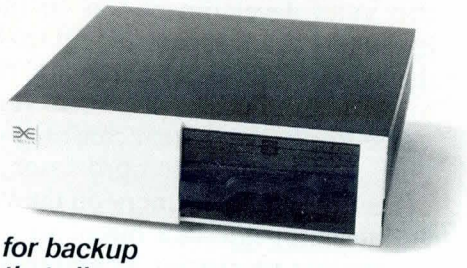

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CIRCLE 68

DESIGNING A PARALLEL SIMULA MACHINE

Modeling hardware architecture along the lines of the Simula software language allows designers to exploit the advantages of parallel instruction execution.

by Mike P. Papazoglou,
Panayiotis I. Georgiadis, and
Dimitris G. Maritsas

Simula-67 is a process oriented, general purpose language. It is intended to be a programming tool that is particularly suited to complex large scale software simulation projects. Such projects are usually characterized by inherent parallelism reflecting corresponding activities of the simulated model. This parallelism, up to now impossible to exploit in the single-processor machine environment, points toward multiprocessor architectures. By nature, the Simula-67 language's process structure allows the definition of concurrent activities within programs. Those activities can be efficiently executed in parallel if appropriate hardware is available.

The parallel Simula machine (PSM) architecture is based upon a master/slave topology, incorporating a master microprocessor. (The analysis and basic software support mechanisms for the PSM have already been covered.[1,2]) Interconnection circuitry between the master and slave processor modules uses a timesharing system bus and various programmable interrupt control units (PICUs). Common and private memory modules reside in the PSM, and direct memory access (DMA) transfers ease the master processor's workload.

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Simula's shape

The parts of any Simula program modeling a discrete event are introduced as classes at the program definition level. At the execution level, these classes constitute processes. Any attempt to achieve parallelism must focus on successfully coordinating control among the various processes within the Simula program. Process interaction occurs in one of two ways: by interrupting processes in the midst of their execution with communication commands (ACTIVATE, REACTIVATE, PASSIVATE, CANCEL, WAIT, HOLD); or by sharing common variables. These variables, which can read or modify more than one process, are called system variables. At the program definition level, this type of process interaction can be identified by a preprocessor software module. This module accepts source programs written in Simula as input and generates tables containing all static level information. These tables include the system variable table (SV-table) and the class template (CT).

The SV-table shows the classes (and, therefore, the potential processes) that refer to a specific system variable (SV_1). The CTs provide the action record of a particular class, tabulating all communication commands issued on behalf of this class. They also show the chains of classes related on a producer/consumer basis. A class is defined as producer (P-class) if it alters the environment of other classes. All classes affected by at least one P-class are called consumer classes (C-classes). Processes originating from corresponding classes are qualified accordingly.

Precedence relations among the various processes, as well as the finite number of processors in a multiprocessor system, establish requirements evoking

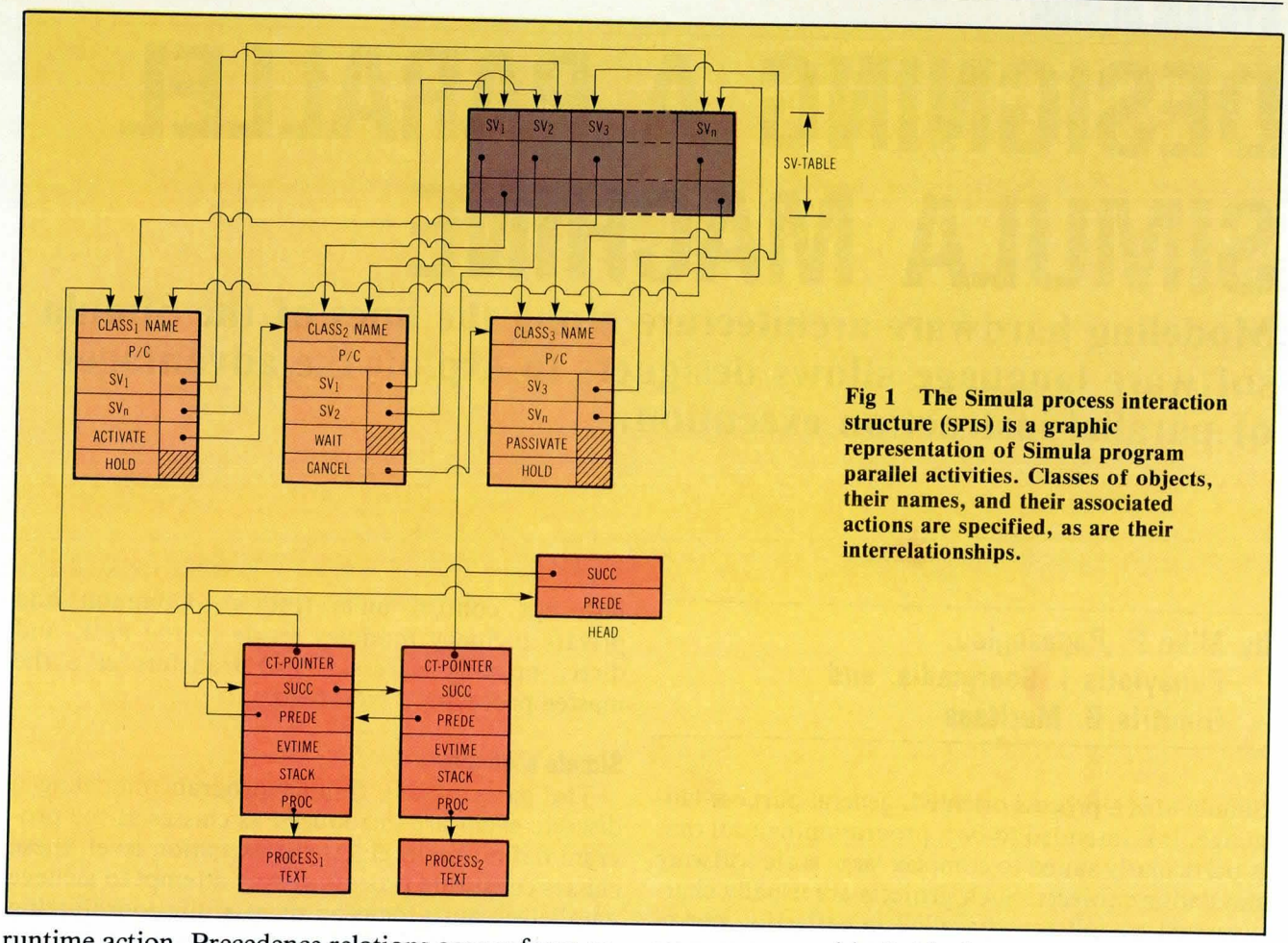

Fig 1 The Simula process interaction structure (SPIS) is a graphic representation of Simula program parallel activities. Classes of objects, their names, and their associated actions are specified, as are their interrelationships.

runtime action. Precedence relations accrue from an event-time attribute inherent in each Simula process.

To accommodate runtime information, the 2-way circular list, or sequencing set (SQS), of a single-processor Simula system is extended. This extended SQS structure (ESQS) incorporates pointers to the various CTs and to a stack area associated with the process being executed. The preprocessor output tables and the ESQS compose the Simula process interaction structure (SPIS), shown in Fig 1. The SPIS also shows how the SV-table and the CTs are associated with each other during the execution phase of a Simula program.

An executive algorithm constituting the kernel of the PSM operating system is a necessity. This executive algorithm uses information contained within the SPIS structure to direct the deterministic parallel evolution of the Simula processes. In designing the executive algorithm, the methodology followed is to decompose a Simula program into groups of simultaneous processes. This decomposition is done with information obtained both at compile time and runtime.

Such a development procedure results in a hierarchy of process groups eligible for parallel execution. The safe and successful sharing of information determines the basis for process group formulation and assignment to hierarchical structures. In addition, the correct transfer of control between the process groups and individual processors plays a part in program decomposition.

To ensure that program determinacy is not violated, the executive algorithm controls the evolution of hardware processors and also processes collaboration. This algorithm also incorporates dispatcher and synchronizer procedures to overcome contortion issues that arise during parallel operation. In the Simula machine, the dispatcher allocates the process to a specific processor at program execution. In doing so, the dispatcher applies certain rules that take into account the number of processors within the machine and the population of the P-processes inside the ESQS.

After initially dispatching processes among the various system processors, the simulated system's behavior becomes dynamic. This is due to frequent activation, removal, and suspension of processes. As a result, a continuous rearrangement of processor/controller (P/C) processes occurs inside the ESQS according to program needs. In general, applying dispatching rules has two main objectives: first, to maximize the number of processors used at any given time; and second, to minimize system reconfiguration overhead.

The synchronizer establishes proper sharing relationships between system variables to preserve their integrity. To design the synchronizer mechanism efficiently, the time-dependent interaction points among

parallel processes must be determined from the SPIS. In particular, the synchronizer is designed around two fundamental synchronization modes. These modes represent either critical regions within processes, or communication commands within these regions.

Hardware design issues

System architecture takes into account the object code produced by the Simula compiler, and the information structure (SPIS) of the Simula program. The parallel machine consists of a number of processors communicating asynchronously with a master processor. These processors share common memory while executing in parallel. In addition, each processor has its own private memory as well as an interconnection path for efficient communication between itself and the master processor.

Simula hardware exhibits four levels of architectural hierarchy. Level 1 assumes that the machine is an integral part of a major mainframe system and accepts the executable code as produced in the host computer. Along with the Simula executable code, the host computer loads the PSM with the appropriate information structure (SPIS). The communication facility that interfaces the host machine and the PSM is a universal synchronous/asynchronous receiver/transmitter (USART).

Level 1 also includes facilities supporting its devices, such as an American Standard Code for Information Interchange (ASCII) keyboard input interface, a cathode ray tube controller, and a floppy disk controller. Information transfer between the host machine and the PSM is accomplished by a timeshared bus. The system bus is initially loaded with the Simula object program and with the SPIS, which are produced in the host computer.

Level 2 consists of the master central processing unit (CPU) and the system shared memory (Fig 2). The shared memory contains the object code and the executive algorithm along with the SPIS. Note that the shared memory consists of random access memory (RAM) and erasable programmable read only memory (EPROM). Executable code, program data, and the SPIS program supporting facilities reside with RAM. The EPROM contains the executive algorithm.

After consulting the executive algorithm, the master processor directs the satellite processors by issuing status signals. It is important that the master CPU alleviate problems, such as multiple resource requests and multiple interrupts, as well as synchronize the satellite CPUs.

Level 3 provides intercommunication. Since the system contains a number of identical processors, it must provide efficient communication between the various system devices. The intercommunication system comprises the various peripheral interface adapters (PIAs) attached to the master CPU and satellite processors. These are called master PIA and private (slave) PIA, respectively (Fig 3). It also comprises the system interrupt controllers and the DMA devices. In order to achieve high data transfer rates, the DMA devices bypass the processor operations. The PIAs appropriately interface their associated CPUs with the system bus and the various system devices. In essence, each individual PIA provides all necessary bus communication and handshaking.

The rise of Simula-67

Early developments in general purpose languages promised the possibility of formally describing computing processes. However, this possibility rapidly diminished as the number of processes making up a system became more complex and interactive. In addition, conventional languages were heavily oriented toward solving numerical problems. When handling very large or highly interactive problems, a novel approach is required. Moreover, a general purpose programming language must decompose complex problems into logical processes. Such languages must also provide flexible control switching between the various program processes so that the interaction pattern between these processes can be faithfully expressed.

At the beginning of the 1960s, Simula's designers analyzed the commonly used languages in efforts to determine whether any were equal to the demands of parallel operation. A very strong candidate surfaced with the appearance of Algo-60. The block concept of Algol-60 lends itself to the formulation of the elegant Simula class concept. Simula is itself the projection of a block, but has instances of staying power (co-routine facility). A class modularizes programs and facilitates their structural decomposition.

A Simula co-routine is equivalent to a procedure, but each time it is executed by a processor, control is directed to the point of last abandonment. Furthermore, co-routines can suspend their own execution for specified or unspecified duration.

Simula-67 incorporates Algol-60 features and extends this language's block concept to allow the generation and naming of blocks that can coexist as co-routines. Such blocks, known as objects, are generated from templates, known as class declarations. Thus, the concept of class and object in Simula can be traced back to similar notions in Algol-60.

A Simula-67 [3,4] definition also includes the Simset package for list processing and the Simulation package for discrete event simulation. These two standard packages can handle quasiparallel execution in generated class objects.

Simset provides for the creation of a doubly linked circular list, the sequencing set (SQS). It also permits the placement of class objects with the circular list. The Simulation facility associates a simulation time with each class object included in the SQS. This simulation time is called event-time. It denotes the activation instance at which a specific object is found to be executed. Each class participating in the SQS is called a Simula process.

Consequently, Simula provides advanced features as a general purpose programming language, while also serving as a powerful simulation tool. It offers conceptual clarity, consistency, security, and efficient implementation mechanisms.

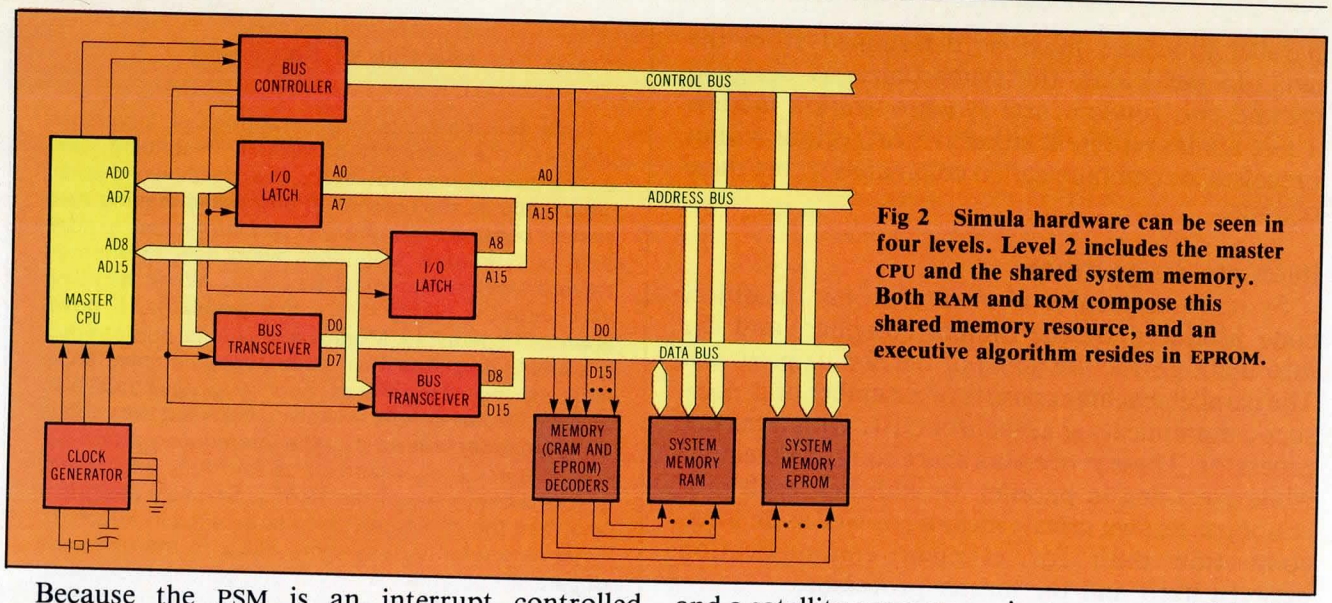

Fig 2 Simula hardware can be seen in four levels. Level 2 includes the master CPU and the shared system memory. Both RAM and ROM compose this shared memory resource, and an executive algorithm resides in EPROM.

Because the PSM is an interrupt controlled machine, multiple interrupt resolution is necessary. The PSM's interrupt circuitry has a single PICU designated as the master. This master controls up to eight additional PICUs (in the case of Intel 8259A), designated as slaves. This allows a maximum of 64 interrupt priority levels. Priority arbitration schemes in such a configuration can be set independently for the master PICU and for each slave PICU. This can result in a bewildering profusion of arbitration possibilities.

Obviously, the master CPU and the satellite CPUs are connected to the appropriate slave PICUs. The DMA controller accepts and resolves DMA requests as they originate from the various system devices. After software initialization, the DMA controller can transfer a data block (up to 16K bytes in the case of Intel 8257) between the shared system memory and a satellite processor private memory. This data transfer takes place directly without master CPU intervention. In essence, the DMA controller treats the satellite circuitries as a set of input/output (I/O) devices.

Level 4 consists of the satellite processors and their private memory modules. As directed by the master CPU, the satellite CPUs operate asynchronously. They execute the Simula object code that has been loaded in their private memories in parallel fasion. The private memories are dual-port devices and communicate with their associated satellite processor via their private bus. They may use the system bus as well, when necessary.

Timeshared bus configurations are notorious for throughput limitations imposed by the system bus. Similarly, a configuration in which all memory is held in common will suffer the effects of congestion.

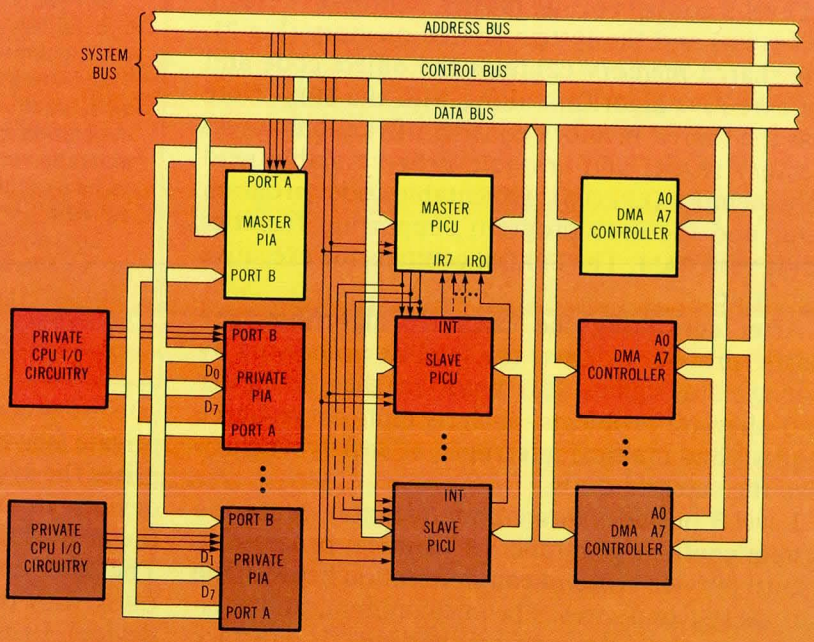

Fig 3 Intercommunication between the system elements is the function of hardware level 3. Here, programmable I/O chips provide their associated CPUs, master peripheral interface adapter (PIA), and master programmable interrupt control unit (PICU) with avenues to system and data buses. Interrupt priority is possible at 64 levels, and the principles of DMA are operant in all satellite/master exchanges.

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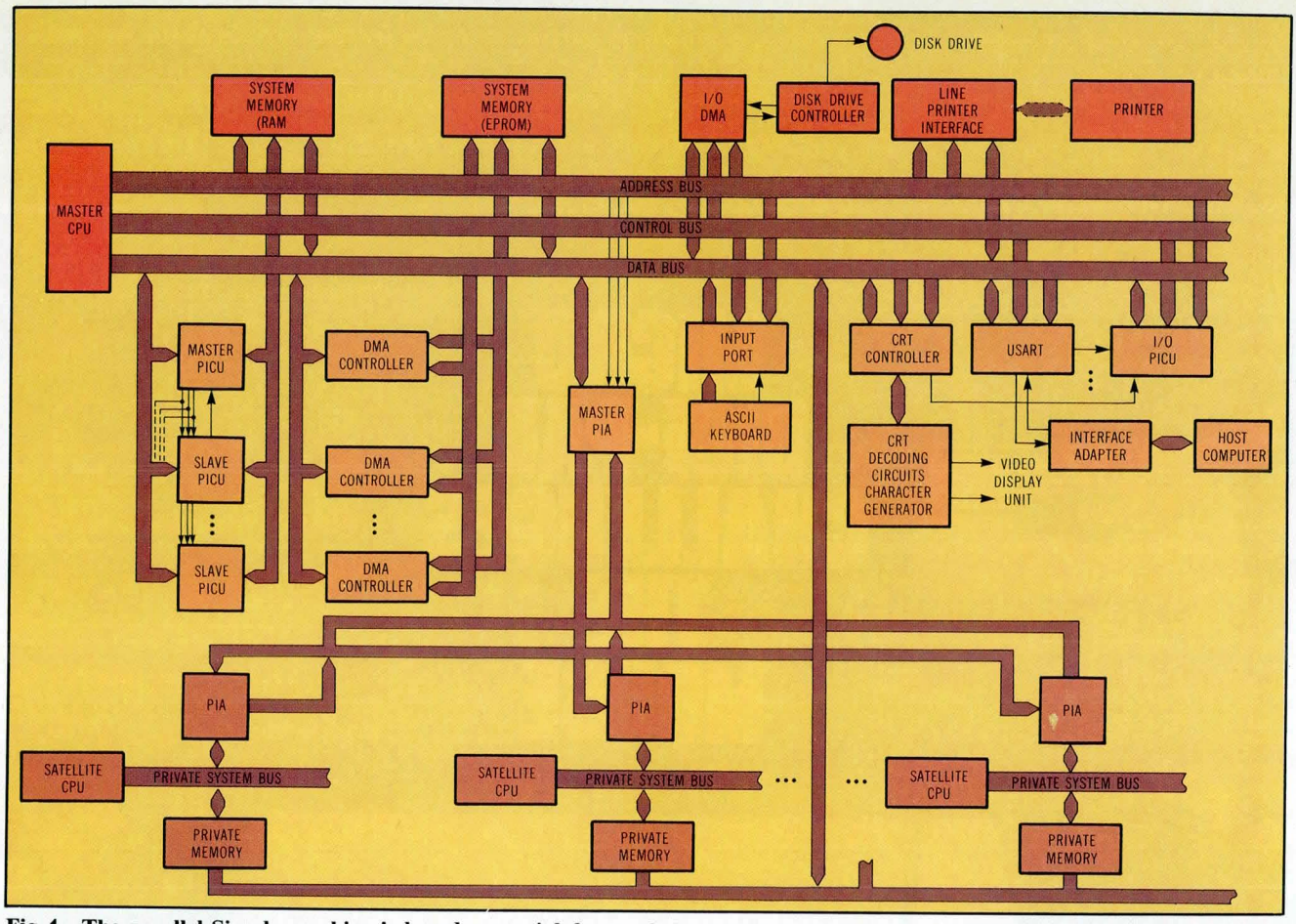

Fig 4 The parallel Simula machine is based upon tightly coupled processors operating in master/slave topology. This interrupt-driven architecture tends to improve performance by actually reducing software overhead through asynchronous service schedules.

As a result, an important design objective is to partition the hardware in a way that diminishes potential bottleneck effects.

System topology concepts

System configuration is based on the notion of tightly coupling microprocessor devices[5]. Tight coupling implies high bandwidth interconnections and thus, physical proximity. In such settings, shared memory is used for data transfers and program storage. Fig 4 shows the overall PSM structure. The system can be classified as a master/slave multiprocessor machine with the control centralized at the master processor. The master processor allocates tasks to the satellite processors and resolves any possible conflicts arising during the execution of a Simula program.

The PSM functions as an interrupt-driven environment. Whenever a satellite CPU wishes to communicate with the master CPU, it issues an interrupt command. Upon inspection by the master processor, the interrupt circuitry resolves the various interrupt requests according to the executed process priorities. To resolve simultaneous interrupts, a specific interrupt algorithm is used. This algorithm systematically examines each alternative and solves every operational issue.

Because interrupts handle all interprocessor communications, there is an actual diminution of bottlenecks. This is due to the fact that only one satellite CPU can communicate with the master CPU at any one time. Therefore, the interrupt concept provides an enhanced asynchronous interface with the service requests. A further benefit is that little software overhead is required until an event captures the master processor's attention.

Private memory consists of dual-port memory modules that allow all private memory to be accessed from the system bus. Such an approach is necessary only in large systems where throughput is limited by bus capacity and data transfer requests are high. All data transfers occur between system memory and the satellite processors' private memories, and there is no means of intercommunication among the private memories.

System implementation

Initialization of the master processor begins by executing the executive algorithm, which resides in EPROM. Meanwhile, the satellite processors await appropriate initialization instructions from the master CPU. The runtime actions of the executive algorithm achieve several ends. First is the establishment of ESQS. This includes instances of certain

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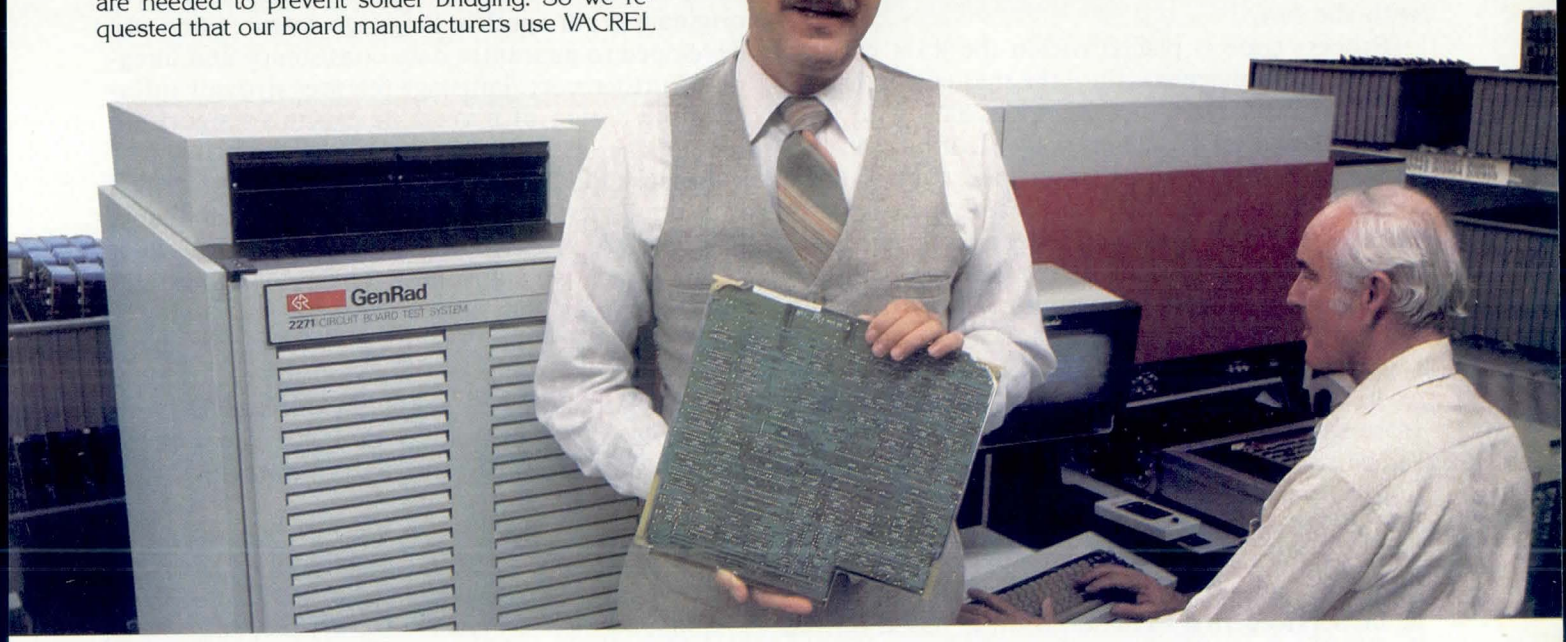

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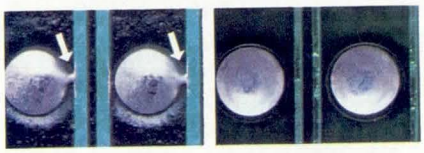

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Simula processes. Second is the recognition at every instance of all the Simula processes that can run in parallel. Dispatching rules are also imposed at this point. Finally, a copy of the process about to be executed is sent to each processor.

During the recognition instances, the PIA quickly realizes that it is about to receive a process object and generates an interrupt signal. The interrupt circuitry directs the interrupt toward the master CPU. An EPROM routine is initiated upon master processor recognition of the interrupt. Then, the information is extracted from the system memory by placing the PIA's address on the system address bus. The process code (now on the data bus) is made available to all system sections. At this stage, the DMA circuitry intervenes and starts dumping the process code directly to the private RAM associated with the PIA.

Process code is placed within the RAM with no processor involvement, since the master CPU is electrically isolated from the system bus during the DMA cycles. Isolation is achieved by floating the processor's tri-state address, data, and control lines. During this time, the PSM can execute specified processes in parallel. However, since Simula processes are highly interactive, an appropriate mechanism is required for process cooperation.

Execution of Simula communication commands results in ESQS rearrangements. Consequently, there exists the possibility of de-allocation of processes from their corresponding processors. Whenever a satellite processor attempts to execute a communication command, it issues an interrupt signal. The master PICU processes this interrupt and halts the whole system. If several interrupts occur concurrently, the master PICU determines which request is to be serviced first. This decision is based on the event-time of each executed process.

Even when a particular Simula process gains priority over another, due to a communication command, it cannot immediately seize the system bus. It must wait until the present bus occupant completes its transfer cycle. This ensures transfer integrity. Upon completion of its transfer cycle, the bus occupant immediately releases the bus.

When a process stays with its satellite processor, the content is maintained within private memory. After interrupts, the process resumes execution from the point where it left off. In the case of process de-allocation, the new process resuming execution overwrites the content of the old process. No harm is done since the system has already saved this process's volatile environment in the common memory. On the other hand, a copy of this de-allocated process always exists within the common memory. In addition, all alterations affected by running processes are eventually recorded in the system common memory. In the case of process cooperation, the frequency of interrupts is proportional to the frequency of communication command appearances within the running process text.

During their evolution, processes establish sharing relationships. This implies that their results must rely on certain consistency constraints. These constraints are implemented by the executive synchronizer procedure. When the synchronizer wishes to enforce a particular order on actions within parallel Simula processes, it must issue a synchronization message to the Simula processes. Interrupts at the hardware level implement this message. Whenever the synchronizer intervenes, interrupts occur and are resolved in a manner analogous to the one previously analyzed.

The parallel Simula machine requires the establishment of several information structures, both at precompile and at runtime levels. These structures originate from specific language features and are developed to guarantee data consistency and integrity. Furthermore, language features strongly influence the design of a versatile executive algorithm serving the operating system kernel.

Because the PSM structure is an interrupt-driven environment, the concept of processor interrupts implies close interaction with the operating system kernel (executive algorithm). This strong interrelationship suggest that device interrupts and the internal operations of the executive algorithm procedures must be handled according to an integral philosophy. This design guarantees simplicity and ease of construction, while exploiting most of the natural parallelism inherent to Simula programs.

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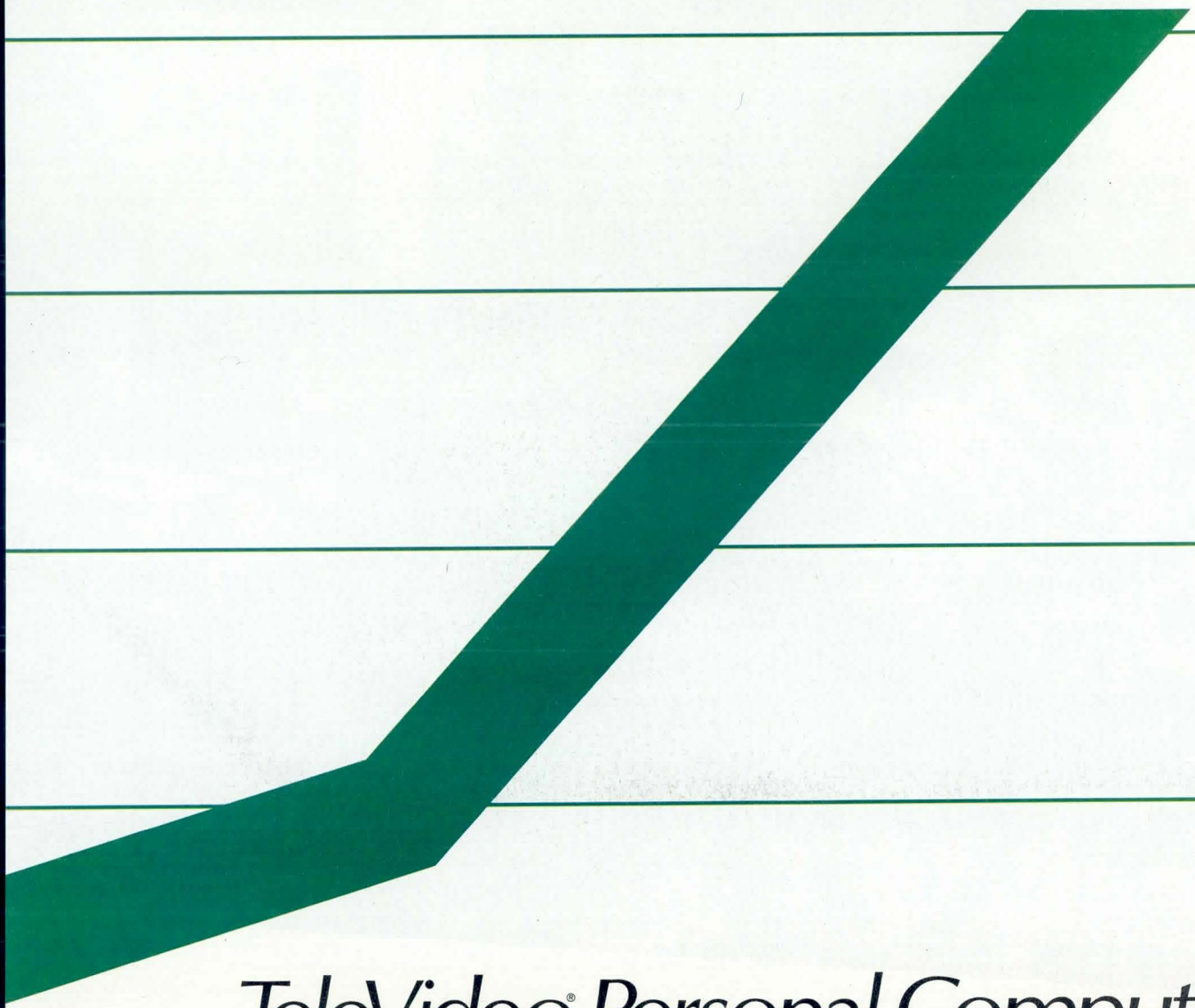

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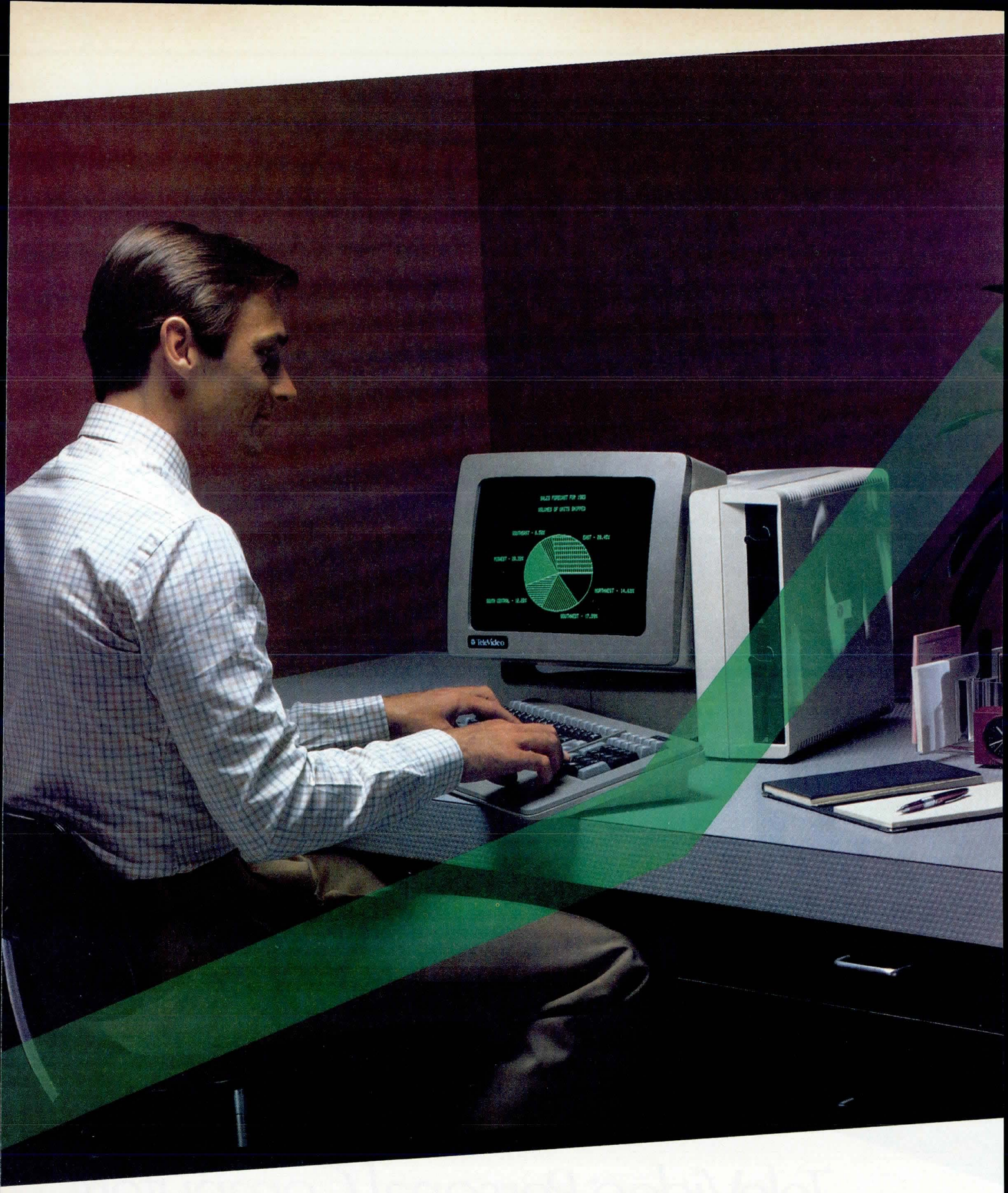
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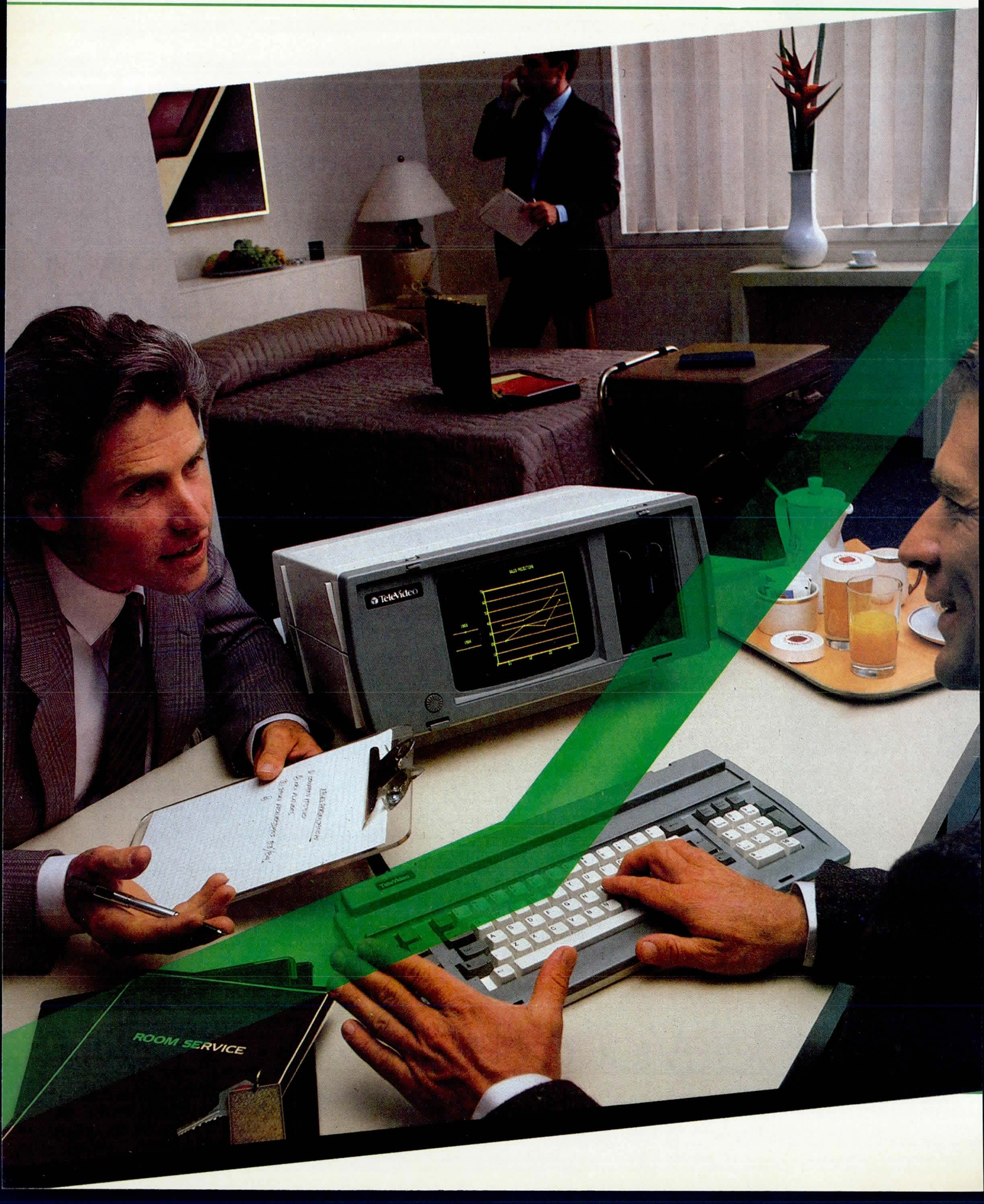
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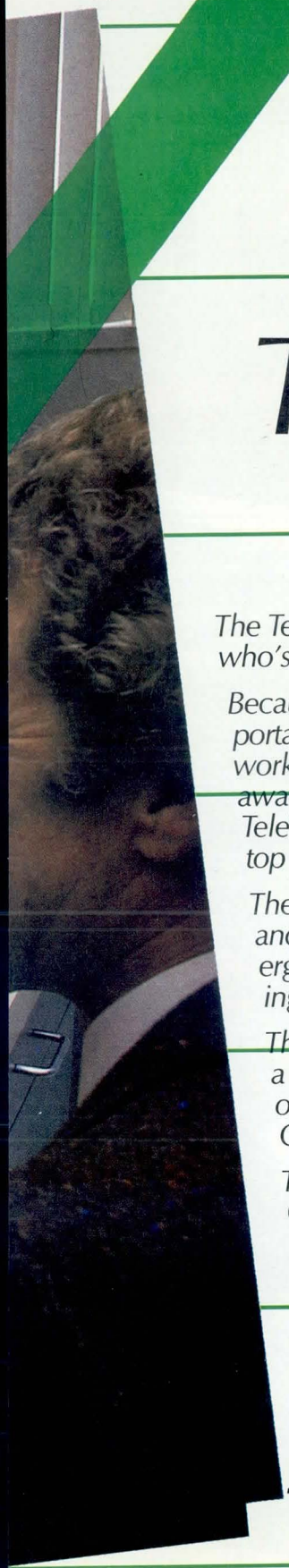

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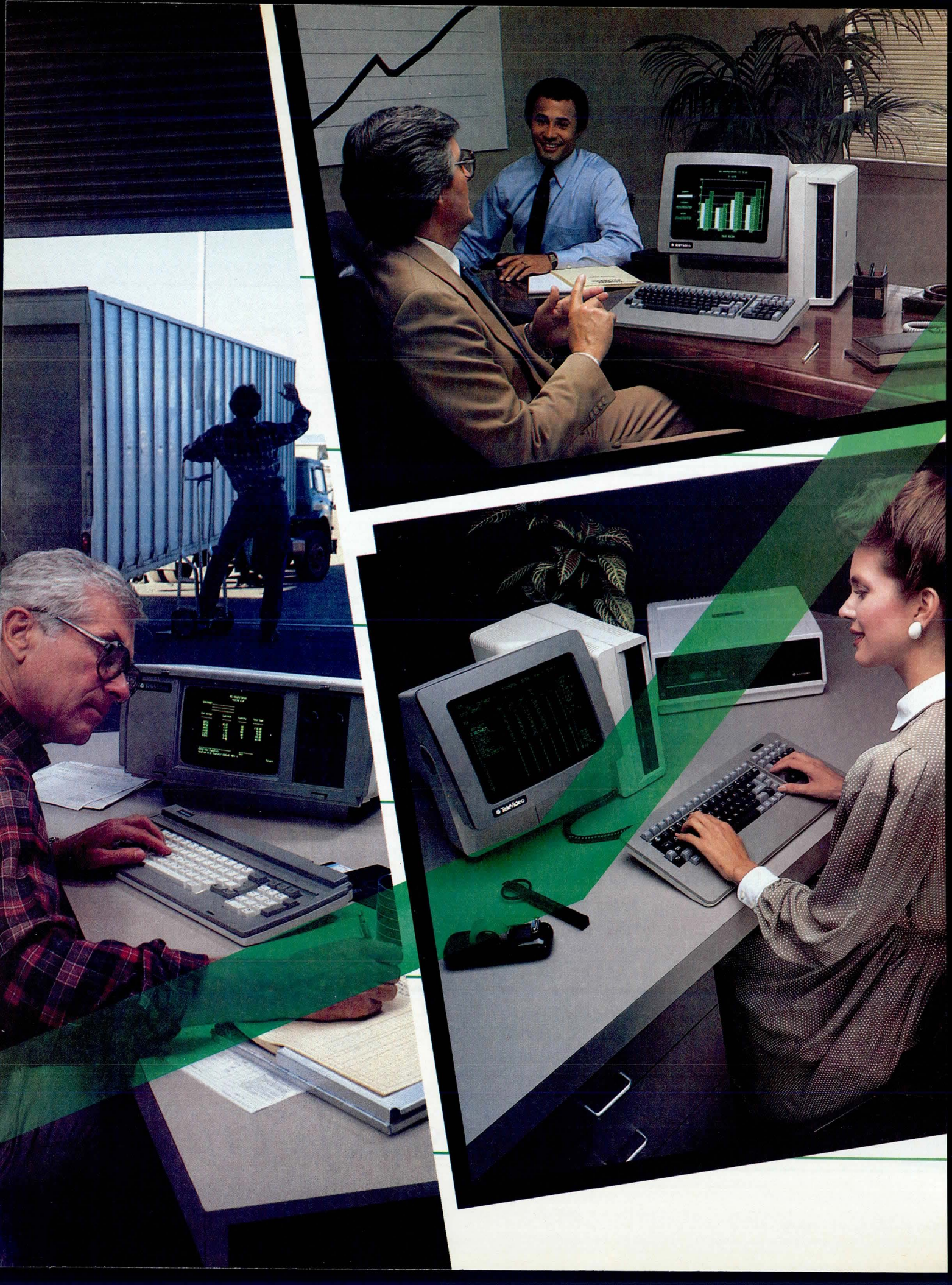

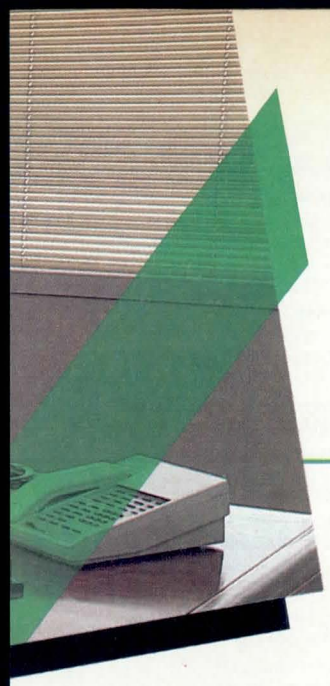

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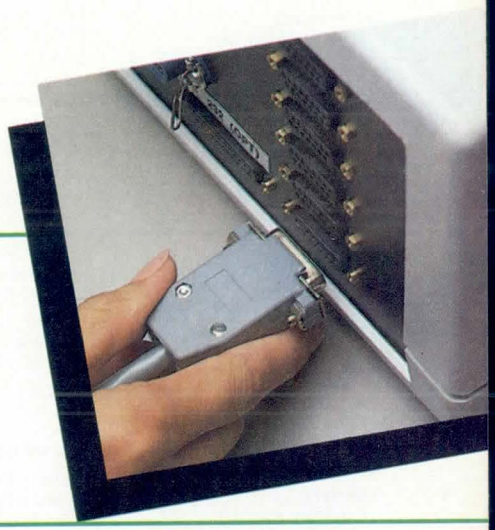

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CIRCLE 72

SINGLE-CHIP MICRO SPEAKS FORTH

An extended Forth interpreter embedded in read only memory brings high level language efficiency to microcomputer application programming.

by Gerald E. Bernier

Programming takes an increasing percentage of system design time. This is particularly true for single-chip, microcomputer-based systems where the hardware design may be quick and easy but software takes as long as it ever has. Any reduction in programming time will directly affect the development cost of micro-based systems.

Consequently, development costs can be substantially reduced by writing the application programs in a high level language rather than in the microprocessor's assembly or machine language. Software costs decrease because powerful commands are available, programs are shorter, and details such as housekeeping are handled by the language developer instead of the programmer. Programs can be written and debugged more quickly, and modifications incorporated more easily. Moreover, documentation is better because the programs are more readable.

High level languages are either interpreted or compiled. An interpreter performs each instruction at runtime, while a compiler translates programs into machine code prior to runtime. Program development is significantly enhanced when working in the user friendly environment of an interactive development system, and this requires an interpreted language. But the interactive environment is useful only during program development, not at runtime.

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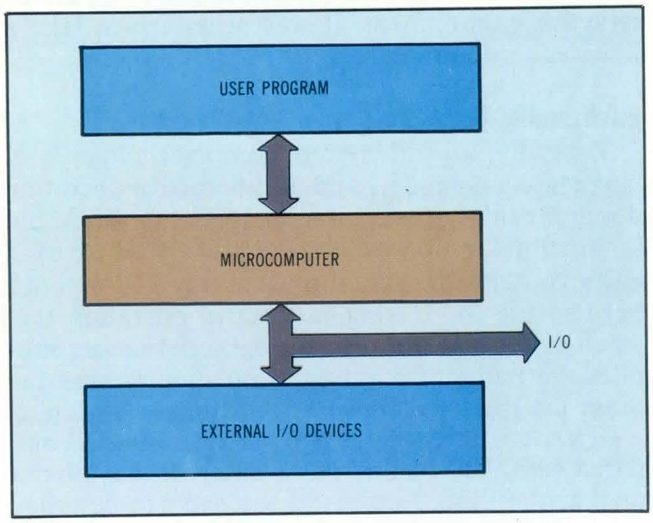

Fig 1 A minimum chip count system consists of the microcomputer chip and a ROM/PROM containing the compiled user program written in the high level language. The external I/O devices are optional.

Putting an interpreter in the onboard read only memory (ROM) of a single-chip microcomputer allows it to be programmed directly in the high level language provided. Not only can the microprocessor's instruction set be extended to give it the power of the high level language, but the interpreter can be tuned to the characteristics of the underlying microprocessor and optimized for runtime applications. These features permit the design of minimum chip count systems (Fig 1) while using a high level language to cut programming costs.

An interpreter based on the Forth language has been developed for RCA's CDP1804 microcomputer (Fig 2). It has 200 instructions including all of the standard Forth instructions applicable to runtime applications, input/output (I/O) instructions, byte operations, efficient memory access instructions, and interrupt-handling instructions. Forth was chosen because, unlike many interpretive languages, it executes instructions fairly fast. Also,

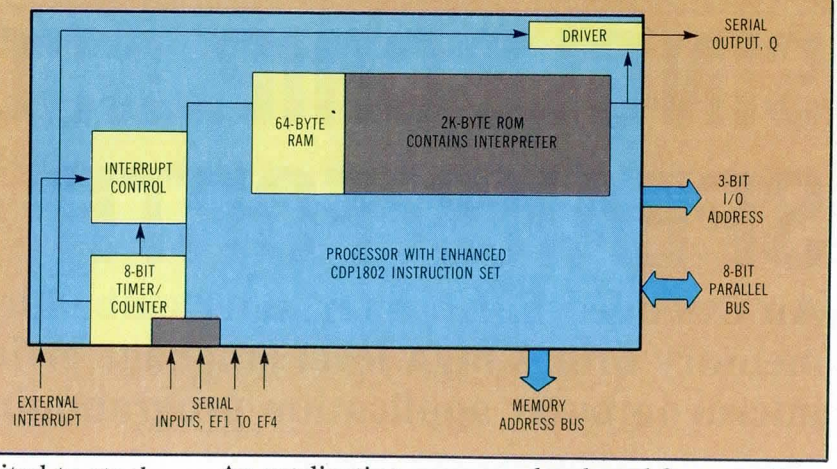

Fig 2 The CDP1804 single-chip microcomputer is an enhanced CDP1802 microprocessor with an 8-bit timer/counter, ROM and RAM added.

family of microprocessors is ideally suited to stack the architecture and instruction set of the 1800 oriented, threaded-code interpreters such as Forth. But, because Forth has been designed for an interactive environment, it was necessary to take a nonstandard approach.

Partitioning Forth

Typically, a Forth system combines a high level language, a compiler, and an interactive operating development system. In such a system, all of the instructions compose a large dictionary where each entry contains the actual routine (the body) plus a header (Fig 3). During interactive operation (eg, when developing a runtime program), the user supplies the name of a routine (mnemonic), and the outer interpreter searches the dictionary beginning with a specified entry. The given mnemonic is compared with the "name" in the entry. If they do not match, the "link" points to the entry to be tested next. This process is repeated for each successive entry until a matching name is found or until the end of the dictionary is reached. If a match is found, either the instruction (body) is executed or its address is compiled into a program. Once a program is compiled, it can be run by sequentially executing the routines found at its addresses.

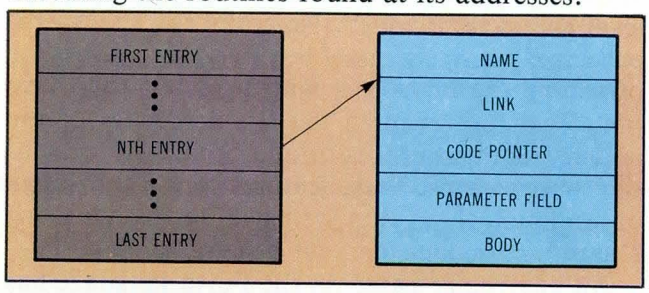

Fig 3 In a typical Forth system, the dictionary contains all of the available instructions in a linked list format. Each entry contains the elements shown. The name is the string of ASCII codes for the instruction name or mnemonic. The link is a pointer to another entry in the dictionary. The code pointer is a pointer to the body (the executable routine). The parameter field, which is often empty, contains specific parameters to be used by the body. A set of entries may share the same body.

An application program developed for a runtime environment must be ROMable. But Forth programs, as previously described, are not ROMable because the routines called by each program are scattered throughout the dictionary, which is much too large to be placed in ROM. The usual approach to obtaining a ROMable runtime program is to use a target compiler to collect the bodies of the routines, actually called by the runtime program, together with that program. While that is a workable approach to the development of ROMable runtime programs, it is incompatible with the fixed, limited memory of a single-chip microcomputer. But, there is an equivalent, alternate approach (Fig 4).

The complete Forth system is divided, conceptually, into two parts: the first part consists of the bodies of the instructions useful in application programs (called f-code); the second part is a dictionary containing the headers for the f-code instructions plus all other system instructions. Thus, of all the instructions in a complete Forth dictionary (eg, compiler instructions, editor instructions, assembler instructions, arithmetic instructions), only those that are useful in runtime applications are utilized in the f-code kernel. The microcomputer with the f-code kernel in its ROM functions as a microprocessor with Forth and Forth-like instructions. An application program calls those onboard routines, thus driving the single-chip microcomputer. This approach provides the benefits of a high level language for application programs without the overhead of a typical Forth system.

Partitioning of the Forth vocabulary has further advantages. Omitting the headers from the space-limited interpreter ROM allows the number of instructions to be doubled because the average header is as long as the body. The additional space can be used to enhance the instruction set by adding many new instructions.

Proper use of the resulting rich instruction set allows a program to be written with fewer instructions. This reduces both program development time and execution time. Also, the development

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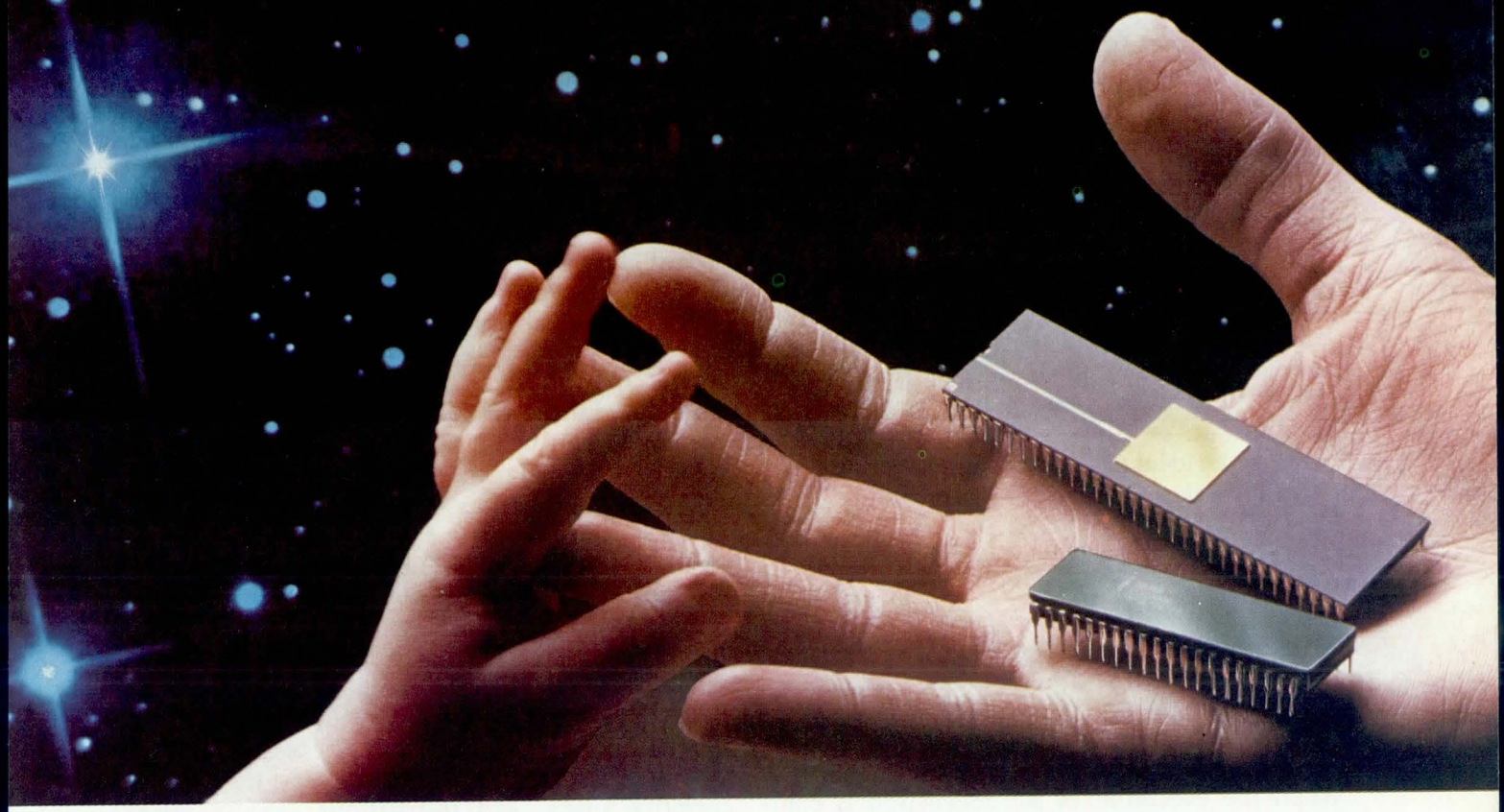

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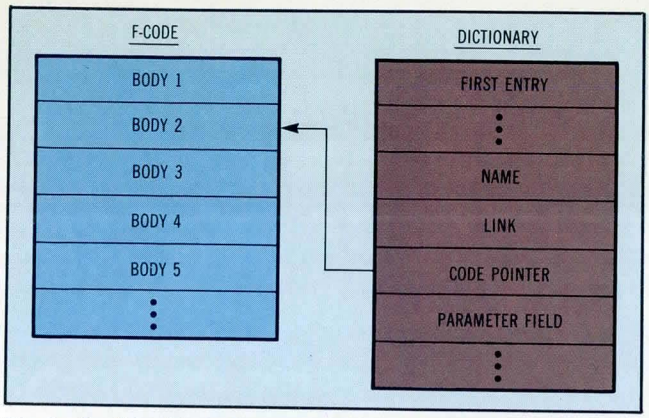

Fig 4 In this alternate approach to the organization of the Forth dictionary, the bodies of entries are removed to a separate location. This subset of the executable routines is called f-code.

system contains, as its nucleus, the f-code kernel. Therefore, as a program is developed, it can be tested with the actual interpreter to be used in the application, rather than with a simulation. Not only is this the ideal means of program verification, but it also makes accurate program timing information available.

The interpreter

The Forth-based f-code interpreter is a threaded-code interpreter with a data stack. It has a separate return address stack and uses reverse Polish notation. This is a direct threaded-code interpreter, which means the user program is a sequential list of addresses of the instructions to be executed.

When the execution of an instruction is completed, the interpreter NEXT routine fetches the next address from the user's program, loads it into the program counter, and initiates its execution. Many Forth systems use indirect threaded-code interpreters because of the increased flexibility. But, increased flexibility is not a factor in the runtime environment, so the direct threaded-code approach was selected because it is faster and saves space.

With its array of 16 general purpose 16-bit registers, the CDP1804 processor is well suited to the implementation of an interpreter. Assigning some registers as pointers, instead of storing pointers in general memory, makes possible fast and efficient access to various elements of the interpreter. Three registers are assigned to the threaded-code interpreter mechanism. The first one, the pseudo-program counter, points at the user program's next instruction. The second register, the program counter, executes the machine language code. The third register executes the NEXT routine.

Three more registers are used to achieve fast access to the data and return address stacks. Two of these are pointers to the respective stacks, and the third contains the top 2 bytes of the data stack. Storing the top of the data stack in a register increases the overall speed of operation. This speed increase occurs primarily in the instructions that access the second word on the stack (eg, arithmetic operations), and those that treat the top of the stack as an address, such as the fetch and store instructions (@ and !). Simple stack manipulations (eg, DROP) are slightly slower. Registers are also assigned as the current DO loop counter, a memory pointer, and a table pointer. Of course, all of these registers are invisible to the high level language programmer.

The memory pointer permits fast, efficient access to memory. The table pointer can be used for relative addressing of memory. An interrupt structure services interrupts between Forth instructions, allowing the interrupt program to be written in the high level language. There are many Forth-like extension instructions, including I/O instructions and byte operations. Fast multiply and divide instructions utilize CDP1855 multiply and divide units in addition to the normal software routines. Additional instructions support the writing of reentrant routines and make accessible all of the resources of the 1804 host processor. This includes the timer/counter, the standard interrupt structure, direct memory access, and the full instruction set.

Many Forth-like extensions to the instruction set are byte manipulations and operations that resemble the standard Forth word manipulations and operations, although the standard Forth word is 2 bytes. Byte instructions are included because byte data are natural for the host processor, an 8-bit machine. Byte data work well because they use less memory space, and instructions execute faster. Therefore, byte data are practical for representing physical data in many applications. To maximize the benefits of using byte-sized data, bytes are placed on the stack as 8-bit quantities. This is contrary to the normal Forth approach of putting a byte on the stack as part of a 16-bit field, with the upper 8 bits being zeros.

The interpreter supports both hardware and software interrupts. Hardware interrupts use the host processor's normal interrupt structure. This

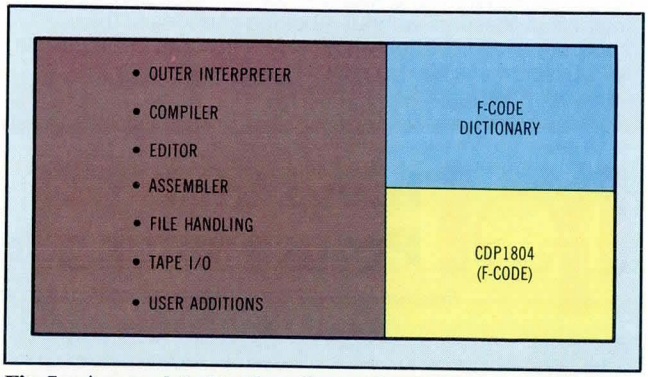

Fig 5 A complete Forth software development system can be constructed using the f-code kernel. It includes all of the Forth routines that are not included in the f-code, plus the headers for the f-code routines.

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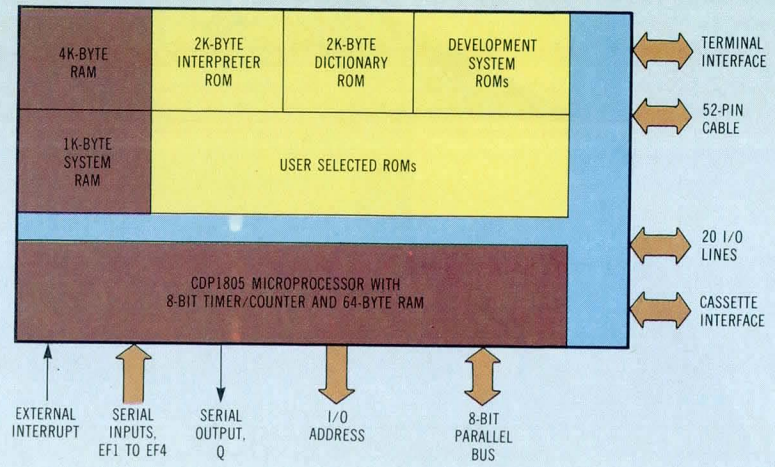

Fig 6 A complete development system using the Microboard Computer Development System has a CDP1805 microprocessor, a separate 2K-byte interpreter ROM, and dictionary and development system ROMs totaling 8K bytes. The user selected ROM area has sufficient sockets for 20K bytes of memory, and the 4K-byte user RAM is expandable to 32K bytes.

permits fast response, because the interrupt routine is executed following the machine language instruction during which the interrupt appears. However, since the interpreter could be in the middle of an instruction, its state is unknown. Consequently, the interrupt routine must be written in machine language. This approach would be used where fast response to an interrupt is needed.

Software interrupts also use the host processor's interrupt structure. However, the interrupt routine is executed following the Forth instruction during which the interrupt appears (at a time when the interpreter state is known). This allows the user to write the interrupt routine in the high level language, making software interrupts a clear choice whenever the slower interrupt response can be tolerated.

There are program control instructions, such as DO, BEGIN, and ELSE, which are used at runtime. The Forth compiler contains instructions with the same names that are included in the development system, because they are used only in the interactive mode. There are several enhancements, including FOR END loops (faster than DO loops), several jump instructions, and two instructions that support recursive subroutine calls.

The data pointer, which points at memory for fast, easy memory access, is useful for string handling and for algorithmic computations. It is also useful whenever it is convenient to store data on the stack. Both the data pointer and the table pointer can be used for relative addressing. The I/O instructions include input and output between the data stack memory and the 8-bit data bus. There are instructions to manipulate the output line, Q, and to read the four input lines, EF1 to EF4 (Fig 2).

The interpreter supports the onboard timer/counter, the CDP1855 multiply/divide unit (MDU), and the CDP1854 universal asynchronous receiver/transmitter (UART). Other instructions provide straightforward use of the timer/counter and the CDP1854 UART. In addition, the interrupt control instructions include use of the timer interrupts. Various Forth routines use multiply and divide operations. Most such instructions appear in two forms—one using the software multiply and divide routines contained in the interpreter, and one using hardware routines. While the software version is resident in the interpreter, the hardware version requires that a pair of MDU chips be added to the system. The software version takes four to five times longer than the hardware version for each such instruction. Thus, the system designer can weigh cost versus performance for each application.

Program development

As with any standard microprocessor, efficient program development requires a software development system. In the case of the Forth language microprocessor, a full Forth system is the obvious choice. And, just as the f-code kernel was extracted from the complete Forth dictionary (Fig 4), that dictionary can be rebuilt around the f-code kernel as shown in Fig 5.

Such a software system has been developed. It is designed to be compatible with RCA's Microboard Computer Development System (MCDS). (The complete system is shown schematically in Fig 6.) The CDP1805 microprocessor used in the development system is the ROMless version of the CDP1804. Thus, a CDP1805 plus an external 2K ROM is equivalent to a CDP1804 for program verification purposes.

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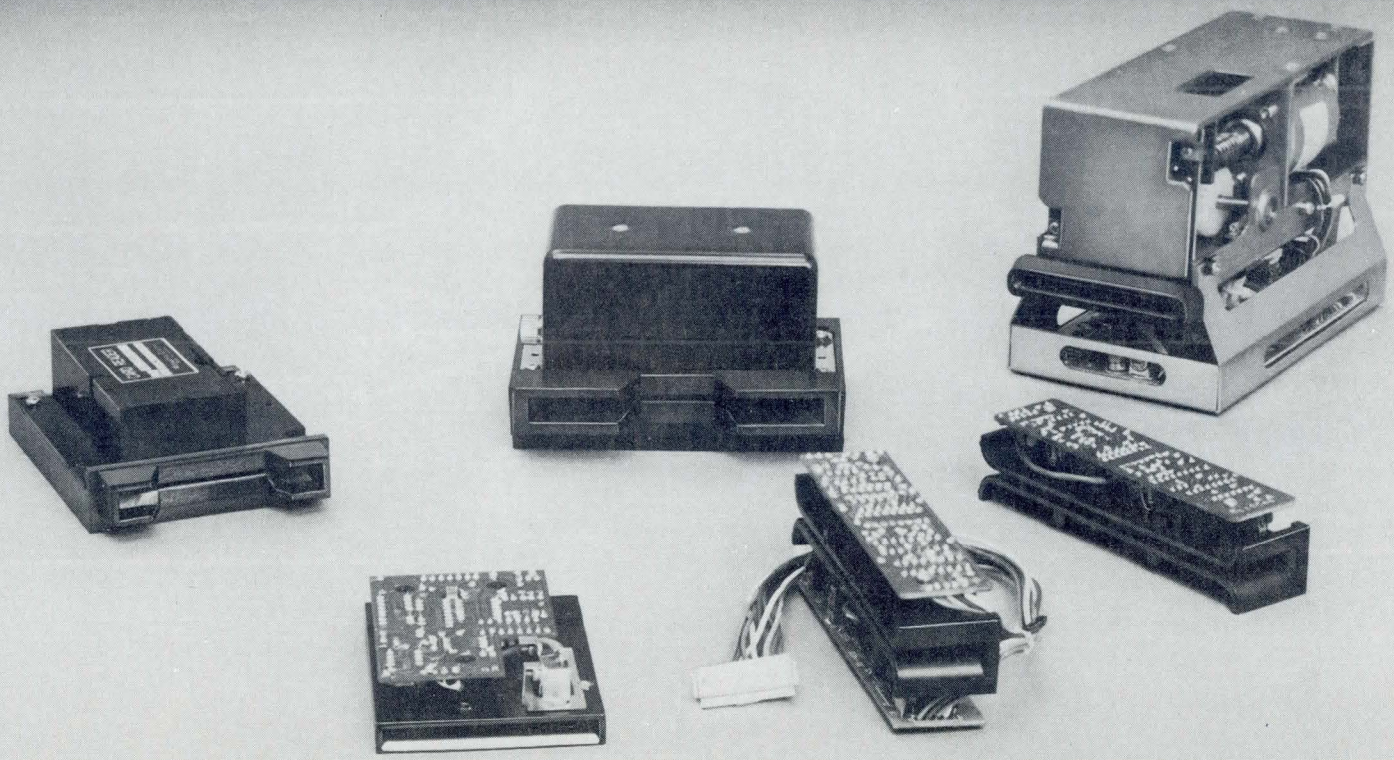

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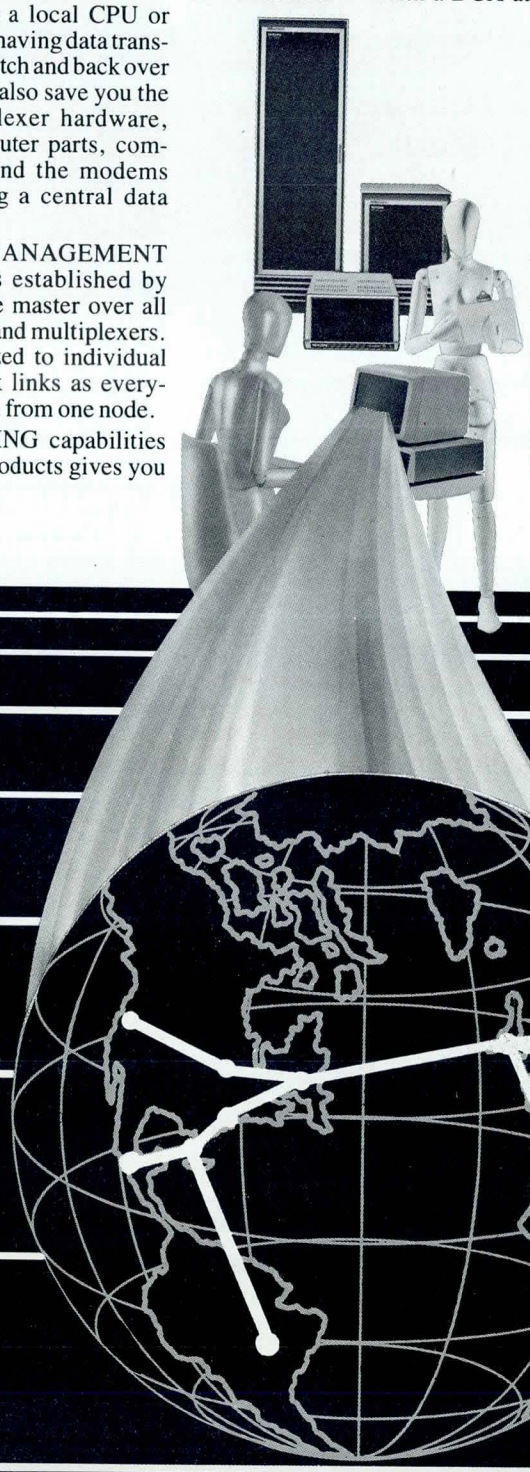

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CIRCLE 75

USE HYBRID SWITCHES FOR VOICE AND DATA

The numerous trade-offs between various switching approaches point to a hybrid solution as optimum.

by Po Chen

Until recently, most switched telecommunication networks provided direct voice communications via an end-to-end connection. Today, however, an increasing variety of data terminals provide both man/machine and machine/machine communications in addition to the traditional voice connections. To complicate the picture even more, network designers have to take into account the wide disparities in traffic rates, transaction sizes, and delivery times.

The disparities are embodied in such items as low speed terminals and wideband graphic devices, which may have variable transaction sizes ranging from interactive messages to bulk data transfers. These devices also require varying delivery times from that of realtime voice and video signals to that of intermittent interactive and bulk data. Finding a solution that encompasses all possibilities requires revamping available switching technologies.

Currently, two switching techniques predominate: circuit switching and packet switching. In a circuit-switching network, whether digital or analog, the end-to-end physical circuit is held for the duration of the call [Fig 1(a)]. Because this circuit is dedicated to individual users, it is not shared with other traffic. Thus, channel utilization efficiency is low. In such a network, a voice channel in normal conversation is idle about 50% of the time, while pauses and words between phrases add to the idle time. As a result, useful energy is transmitted on the average only 37% of the time.

A packet-switching network has digitized speech or data information packed into small segments, or packets, that are routed through dynamic or fixed paths [Fig 1(b)]. For packetized voice, a speech detector can be used to filter out the idle signal, and thereby improve the channel utilization efficiency. Total throughput can be increased by having routing paths share other packets during idle periods. Packet-switching networks such as ARPANET and GTE-Telenet primarily serve the data communication community, however, and packet voice communication networks are still largely experimental.

Both circuit and packet switching offer clear advantages that could be maximized in a hybrid configuration. Variations of both circuit and packet switching have been proposed in recent years. These include fast circuit switching, enhanced circuit switching, and hybrid packet circuit switching.

Switching options

In fast circuit switching, signaling messages set up and tear down a connection before and after each transmission. The signaling speed is so fast that it becomes practical to establish a circuit for

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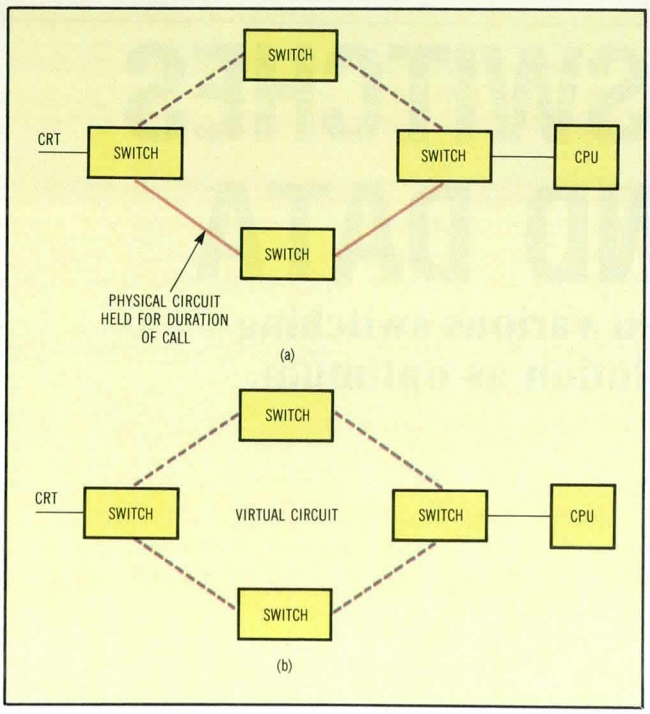

Fig 1 In a traditional circuit-switching network (a), a physical circuit makes connections between two switches during a call. This provides for an inefficient use of channels with only about 37% used at any one time. A similar packet-switching network (b) increases channel efficiency but inserts an unacceptable delay for voice transmission at high usage.

every message to be sent, and then disconnect it after transmission is completed. Thus, some channel capacity is saved by not dedicating the circuit during idle time. The setup or disconnection of a circuit can be done in 140 ms or less. This would satisfy the strict end-to-end delay requirements of 200 to 250 ms for interactive data users and realtime voice conversations.

As the idle time between interactive messages decreases, the efficiency of dedicated circuits to individuals increases. The crossover point is reached when the idle time is 1 to 2 s, or less. Traditional circuit switching then becomes more effective than fast circuit switching. However, such fast switches or networks are not yet available.

Enhanced circuit switching attempts to improve the channel efficiency associated with the traditional circuit switching of voice and interactive data. Techniques such as time assignment speech interpolation (TASI) for voice, and adaptive data multiplexing (ADM) for interactive data propose to enhance circuit switching. These techniques take advantage of gaps between messages by multiplexing message streams on already setup circuits. However, they are expensive to implement, and neither has been sufficiently developed to be considered viable in the short term.

On the other hand, packet-switched networks have been designed for low-to-medium-volume data users. The carrier's network resources usages are optimized, and higher resource use is achieved by sharing network paths among multiple interactive users.

In currently implemented packet networks, maximum packet sizes at the user interface range from 16 to 1024 octets. Each packet is made up of a network-defined header that controls the packet throughout the network and the user data/voice. When the arrival rate of packets at a network node momentarily exceeds the transmission capability of a node, packets are typically queued in buffers and forwarded when a transmission time period is available.

Because packet switches and networks are store and forward, they can have functions such as code, speed and protocol conversion, and error control, which traditional circuit-switching networks cannot provide. Speech and data require different packet sizes and transport protocols. This complicates combining both on the same network switches. Within a packetized voice/data network, voice transmission would need to have a high priority, which requires that the packet switch would have to readily distinguish between the two.

Taking a hybrid approach

A viable alternative for transmitting both voice and data is to use circuit switching for voice and bulk data, and packet switching for other data. A communication channel linking two nodes in a hybrid switching system could use a time-division multiplexed master frame format. The frame would then be defined as a constant time interval throughout the entire backbone network.

In such an approach, voice traffic and bulk data traffic would use the circuit-switching subchannel, while signaling message traffic and other data communication applications would use the packet-switched subchannel. Each slot in a frame could be of a different size, depending on the bandwidth requirement in the circuit-switching mode, and the packet size and signaling message size in the packet-switched mode. However, the duration of each frame should be very short.

The transmission capacity can be shared in two ways. Using a fixed boundary technique, the partition of link capacity between the circuit-switched and packet-switched traffic is fixed. With a movable boundary, the packet-switched traffic can dynamically use idle channel capacity assigned to the circuit-switched mode. The interaction between the packet and circuit-routing algorithms still needs to be addressed, however. The movable boundary arrangement seems to be more efficient than the fixed boundary arrangement.

Current voice/data networks require two separate switching arrangements to handle voice and data traffic. Each is designed to handle a specific type of traffic. However, since each switch

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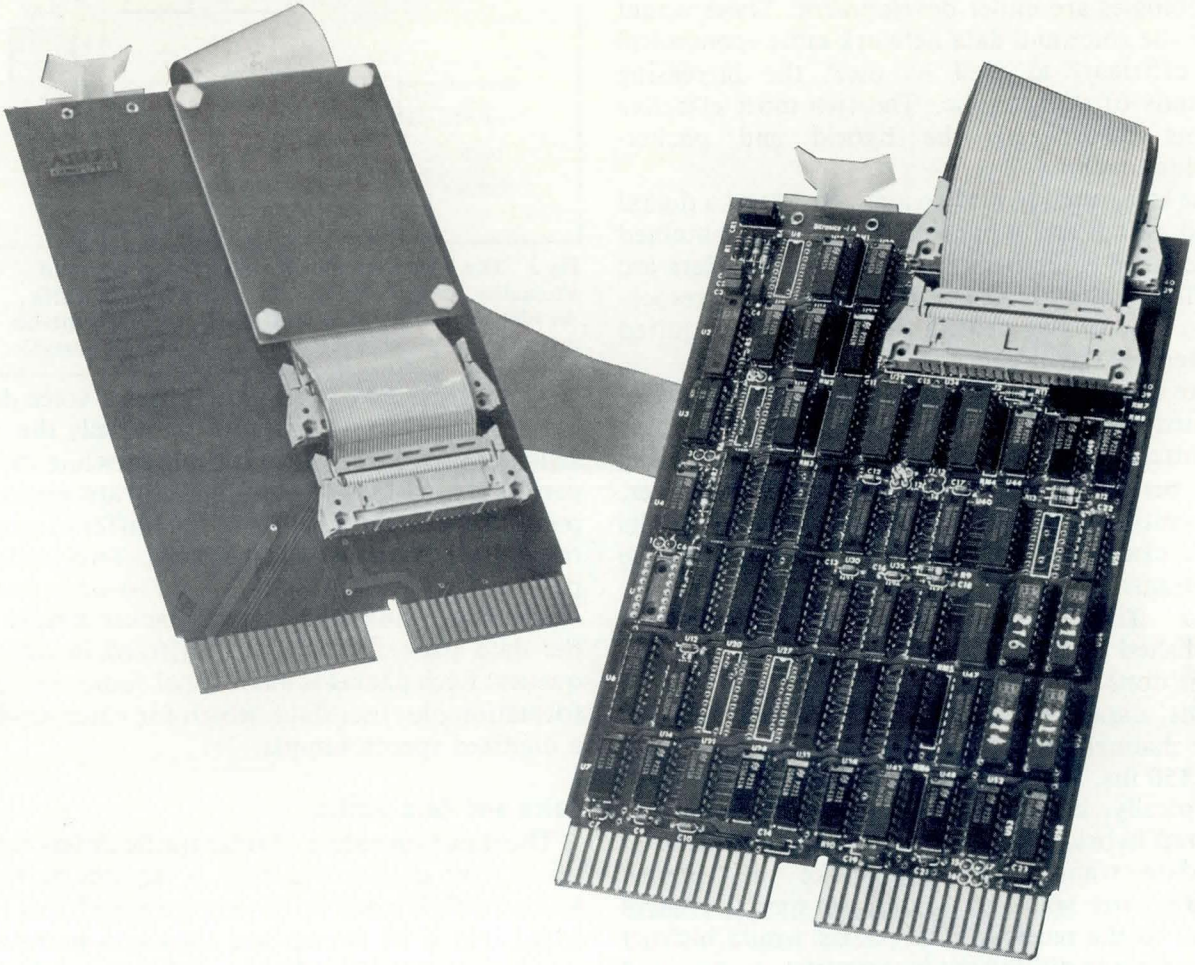

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needs separate transmission facilities, the cost of operating two separate switching arrangements is invariably high.

Integrated networks combining certain switching technologies are under development. These would make the voice and data network more economical and efficient, as well as meet the increasing demands of data traffic. The two most effective designs incorporate the hybrid and packet-switching technologies.

The integrated hybrid switch consists of a digital circuit switch and a packet switch, both contained in the same equipment (Fig 2). voice and data are handled by the circuit and packet switches, respectively. One or two central processors are required to interface the circuit and the packet switch.

One way to improve the efficiency of such an integrated switch is to implement a voice detector and insert the data into the voice channels during silent periods in the voice conversation. However, transmitting data on a silent voice channel results in the next voice segment being "clipped" if the data transmission on the voice channel is not completed. Therefore, a threshold needs to be established to determine when the data insertion can be done. For example, if the threshold is set at 150 ms, data packets can be transmitted over this voice channel only when the silent period is longer than 150 ms.

Typically, a network control center in the integrated hybrid switch would be able to interrupt the data transmission and make the channel available for voice by sending a special control packet to the receiver. The packet would instruct the receiver to discard the incompletely transmitted data packet. The data transmission and retransmission would resume at the next available time slot.

Certainly, these controls would further complicate the function of an integrated switch, which in turn would increase the cost. Also, the effect of clipping on voice signals needs to be studied more before voice detectors can be implemented in integrated hybrid switches.

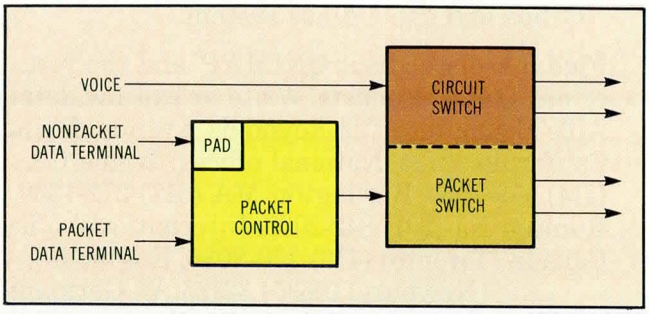

Fig 2 One proposed integrated network for efficiently handling the growing voice and data traffic is the integrated hybrid switch. This switch offers the least disruption during transition from today's circuit switch to an integrated switch.

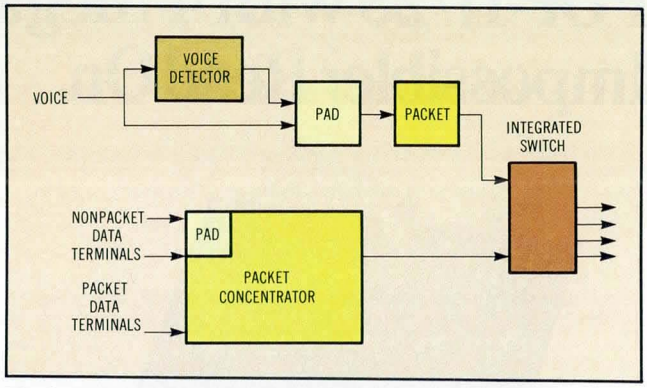

Fig 3 The integrated packet switch offers a second alternative for contending with voice and data traffic. As with the integrated hybrid switch, the unacceptable delay for the voice channels poses the biggest obstable.

The integrated packet switch uses a voice detector to sense the talk spurts (Fig 3). Only the voice signal is packetized and transmitted while the idle period is used for the data-packet transmission. A packet concentrator serves as the buffer to concentrate and distribute the packets. Two different packet streams are multiplexed over a set of transmission links. The voice packet stream and the data packet stream are buffered in different queues. Each packet is made up of some control information plus user data, which for voice would be a digitized speech sample.

Voice and data traffic

The statistical nature of voice traffic differs considerably from data traffic; thus, it requires buffering. Voice traffic is made up of sampled speech that is encoded into a bit stream and then into packets for subsequent switching. Voice packets must be buffered and the appropriate buffers emptied before the next voice packet arrives. A fixed delay is inserted in the voice-packet transmission path that is equal to the time required to load and unload the buffer. In this way, the switch continues to transmit voice packets as long as the input buffer is full. The input buffer for voice has to be at least two packets wide to guarantee switching within a fixed time interval for each voice conversation.

Data traffic is much less predictable than voice traffic. In fact, line use per data terminal could even be less than that for a line with an active voice conversation. Keeping the criterion of assigning voice packets a higher priority than data packets, the integrated packet switch controller must first assign any voice packet to an available time slot, and then, if there are no more voice packets, multiplex data packets into the remaining time slots. Within each priority class, packets need to be transmitted in the order of their arrival.

An integrated voice/data packet switch appears to offer many advantages but is difficult to implement. It could improve the efficiency of channel

utilization and could suitably handle interactive data communication. However, the delay for voice packets increases as the traffic increases even though the voice packets have a higher priority than data packets.

This long delay can be dealt with in the packet voice network. For packets that are lost in routing or have a long delay, several reassembly techniques could be used. They include repeating the last received error-free packet or interpolating those packets that are immediately before and after a lost packet. Another inherent problem is voice clipping. Its effect, as perceived by the subscribers, still needs to be studied.

Integrated hybrid switching—a practical alternative

On the other hand, the integrated hybrid switch is a practical technical solution to concurrent voice and packet traffic. The efficiency of channel utilization with a hybrid system is not as good as with the packet switch, but it is better than with the circuit switch. Therefore, hybrid switching would seem to be the best choice for future voice/data communication networks.

Hybrid switching offers several advantages. For instance, bulk data, facsimile, and video signals can be transmitted with greater transmission efficiency and less delay in the circuit-switching portion of a hybrid switch than in a packet switch. Moreover, after call setup is completed, voice communication suffers less end-to-end delay in a hybrid switch than in a packet switch. This delay could be significant if added to the delay caused by a satellite link. In addition, the ease of transition from today's circuit switch to the hybrid switch makes the hybrid-switching technique more attractive than others.

Although transmission efficiency and channel utilization for voice transmission in the circuit-switching portion of a hybrid switch is not as great as that of a packet switch, the circuit-switching portion can transmit continuous realtime data. Thus, if a practical packet-switched voice system can be realized, the hybrid system can be easily reconfigured to handle voice and interactive data via a packet-switching portion, while transmitting bulk data, video, and facsimile through the circuit-switched portion of the hybrid switch.

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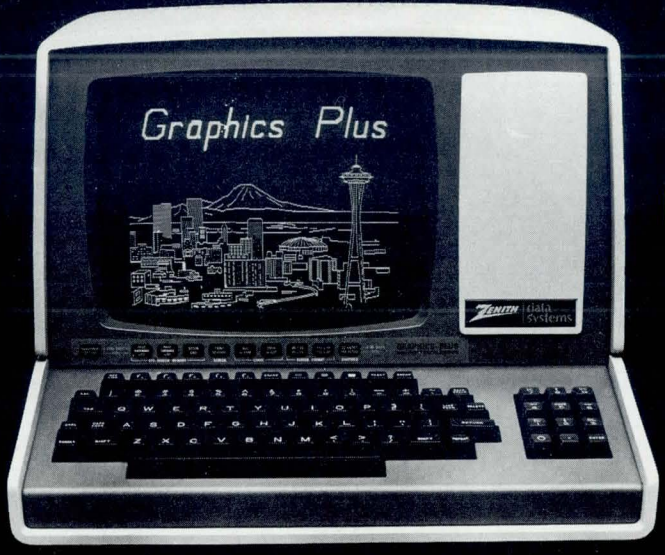

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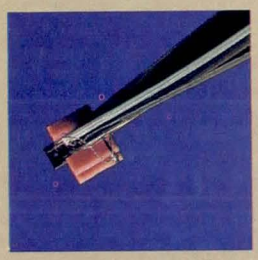

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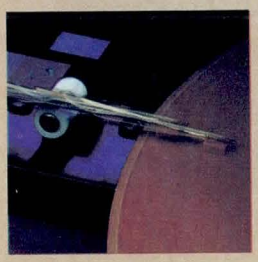

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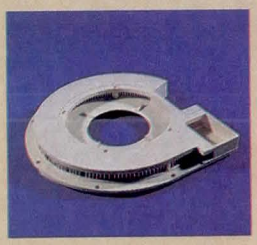

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Inset photos depict the Whitney Suspension (at left, top), retracted head launch (at left, bottom), active hub seal (at right, top), and the recirculating air filter (at right, bottom).

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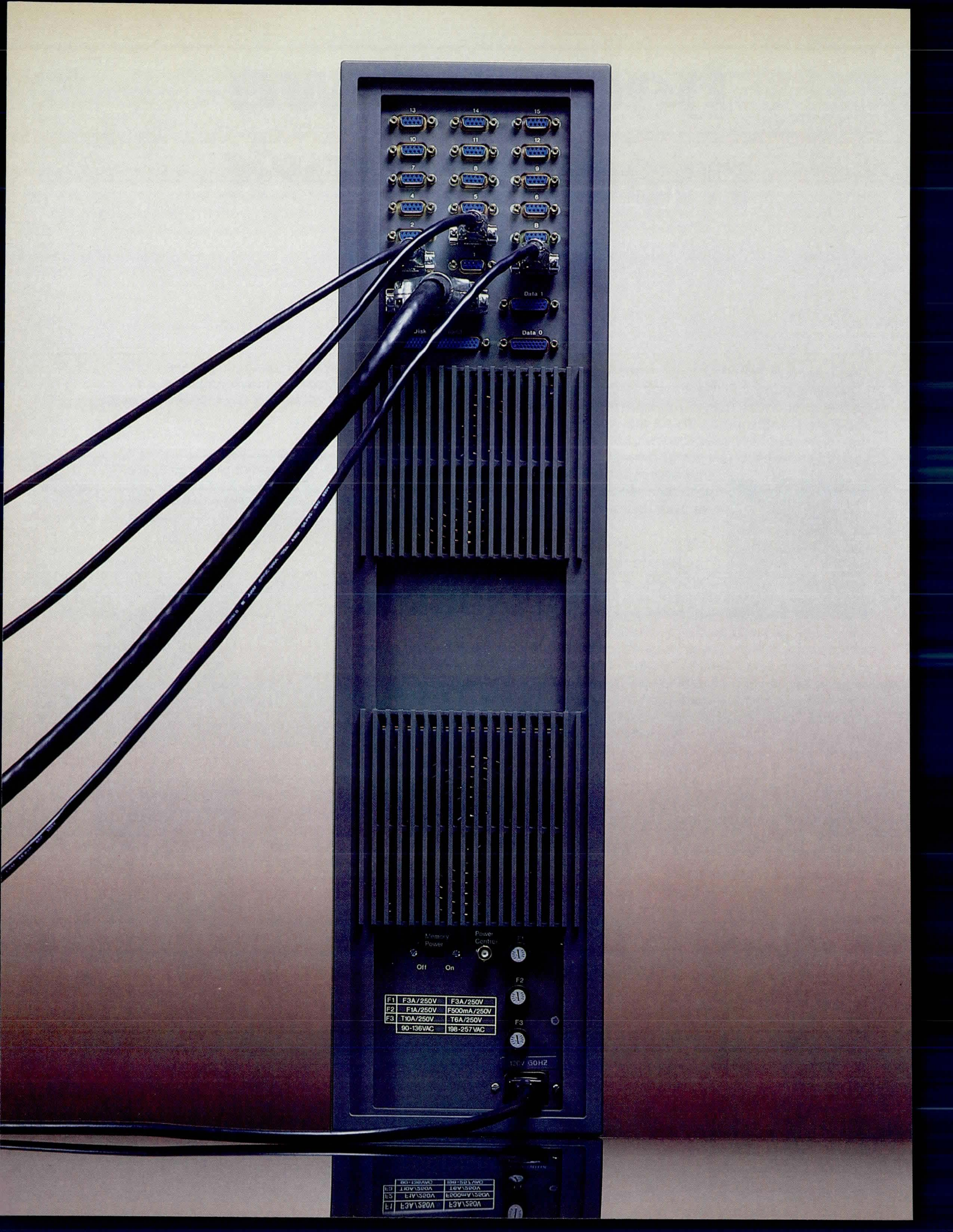
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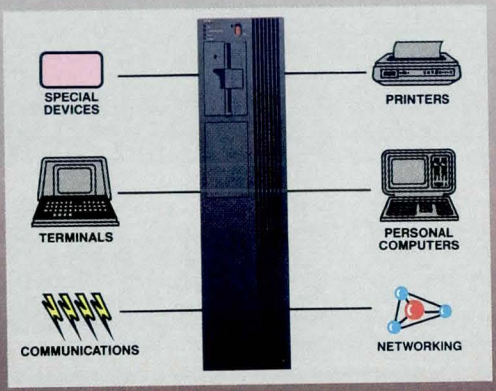

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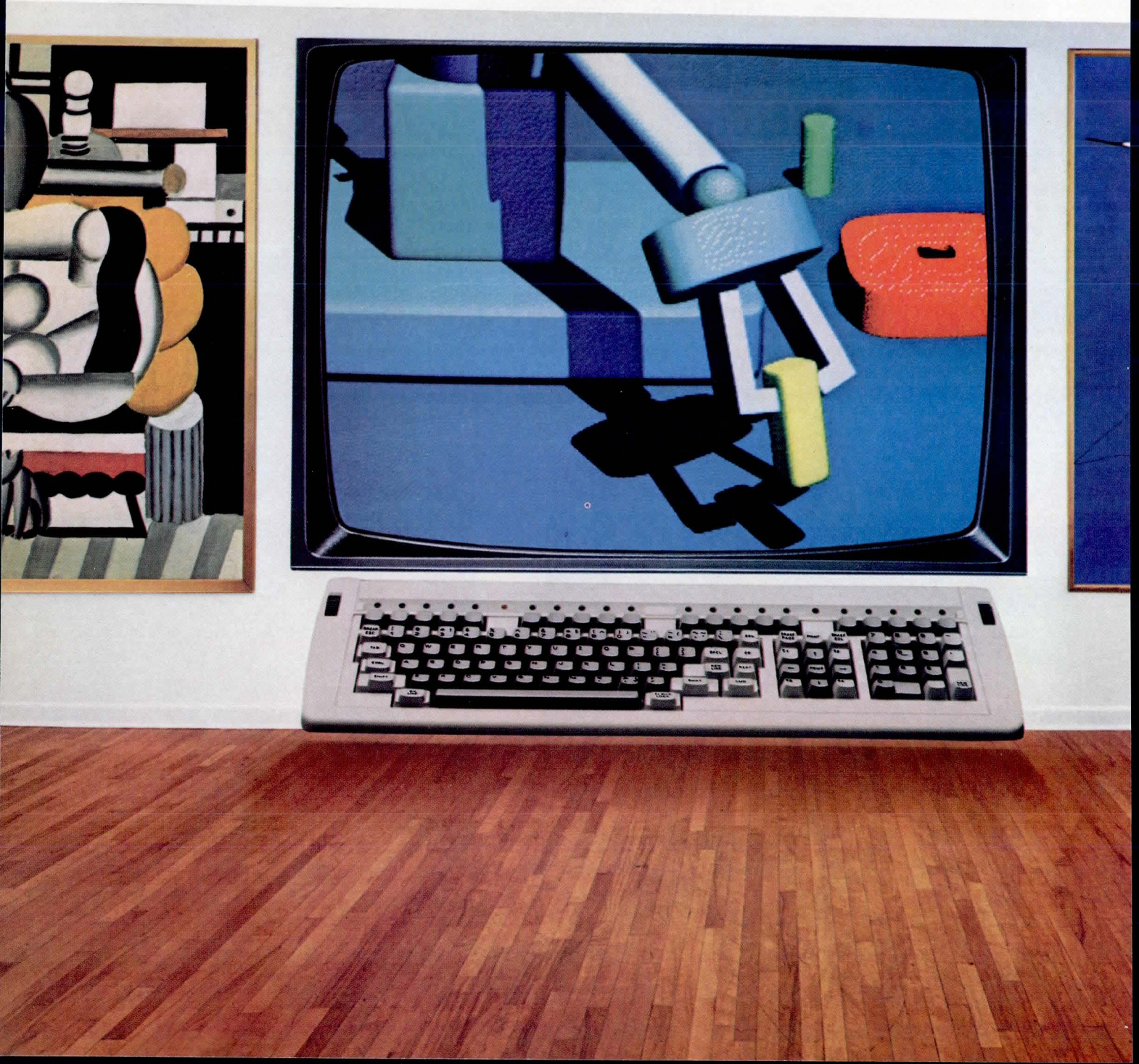

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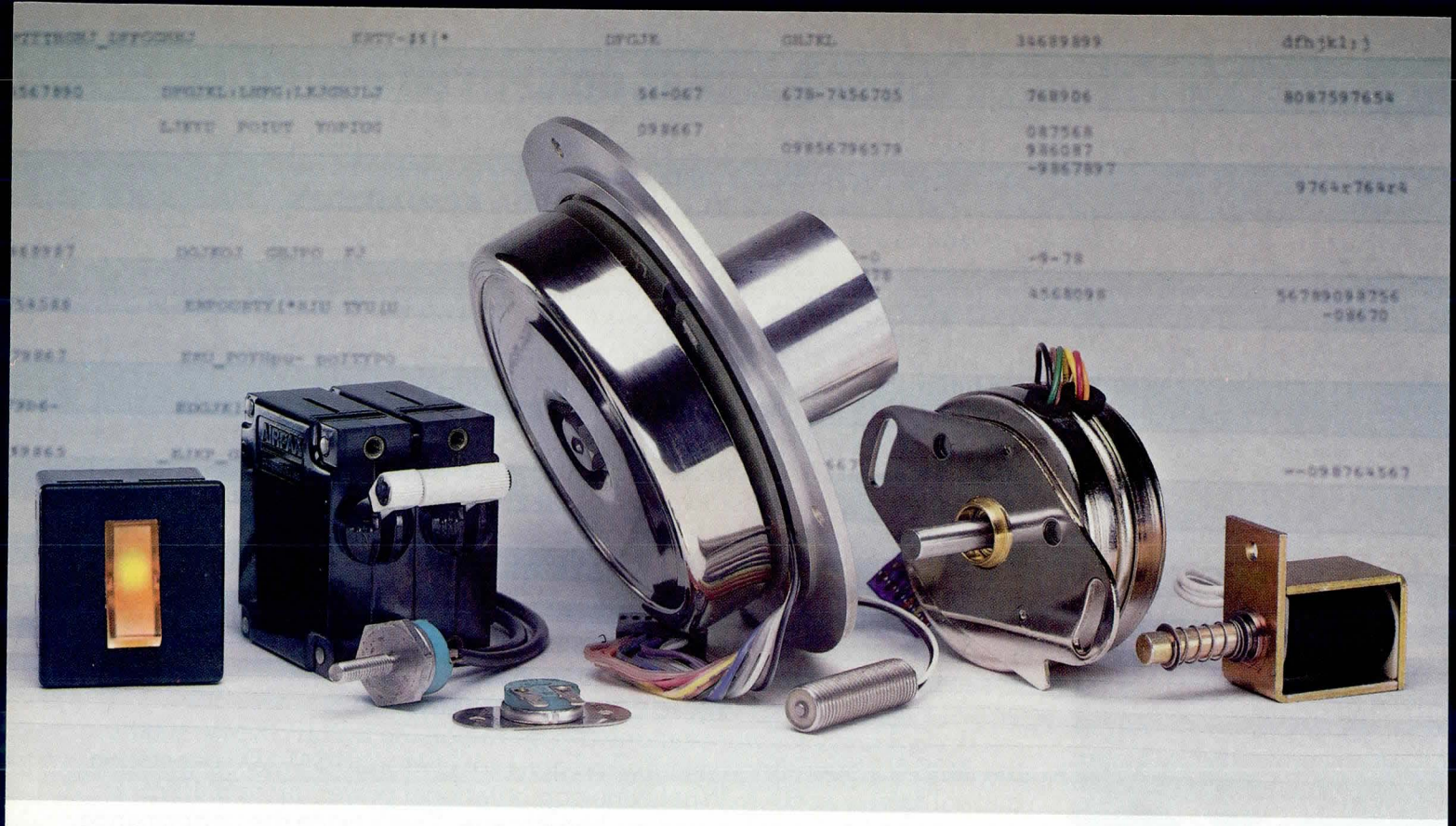

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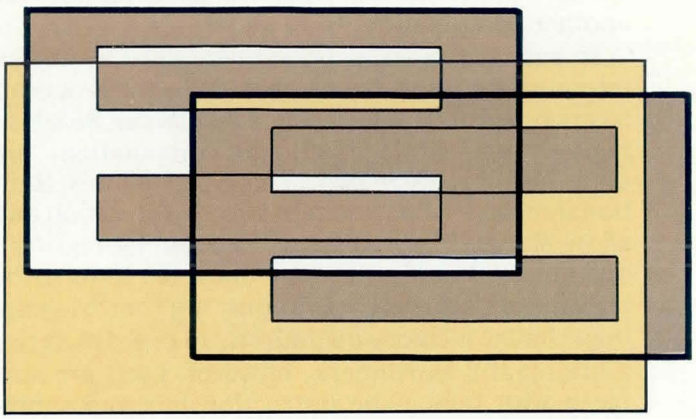
CONSTRUCTING BENCHMARKS THAT MEASURE UP

There is more to gauging hardware performance than tallying the number of instructions executed in a second. Instruction mixes, formats, and compilation methods all skew performance.



by Jeffrey Pulcini

Objectively rating a computer's performance is, at best, problematical. Vendors, in attempting to portray their product in the best possible light, often yield to competitive pressure and concentrate on one aspect of performance. To further complicate matters, they often invoke esoteric standards of measurement. Consequently, the burden of accurate performance measurement is placed on users.

The user community, however, is faced with problems of its own. First, users must create benchmarks that represent their environment. This is more difficult than it may seem, and demands a global understanding of the problem that is not always possible. Second, truly valid benchmarks must be capable of outsmarting a diverse selection of hardware. For example, unless a benchmark program's flow paths and size are representative of the user environment, a small benchmark may fit totally within cache memory. This results in artificially high performance figures. Finally, users must recognize the strengths and weaknesses of benchmarks. Unfortunately, many benchmarks are hastily prepared, by people with little experience, and then as a secondary task.

Traditionally, rating a computer's performance has always been difficult. One approach has focused upon instruction execution speed. Simply, a machine capable of addition in 1 μs is faster than another that performs the same addition in 2 μs. Stated differently, machine number one is capable of executing 1M (1-μs) instructions per second (1 MIPS). Machine number two executes 0.5M (2-μs) instructions per second (0.5 MIPS).

This deceptively simple way of measuring performance has been complicated by hardware designers who have included other instructions such as subtract, multiply, divide, shift, load, store, and branch. This has resulted in different execution times for each kind of instruction. To deal with this disparity, the concept of an instruction mix is necessary.

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An instruction mix is the average percentage of adds, subtracts, etc, that a program requires to perform its function. Instruction mixes are not easily determined by analysis, since this involves writing analysis tasks and then tallying the types of operations involved. Ultimately, numerical values representing instruction mixes are obtained.

This concept has several problems, however. First, the tasks performed can change. For instance, an instruction mix using a particular job structure may change radically simply by adding a graphics function to a program. In this case, the percentage of load store instructions, as well as computational instructions, are altered. In fact, as applications are developed, changes in features, functions, and capabilities all work to modify the established instruction mix.

Registers and instruction format

Hardware designers, in efforts to increase the speed of the processor, add many features. Prominent among these are additional registers. The earliest computers had only one register or accumulator. Programmers loaded the accumulator, added the contents of a memory location, and then stored the result to free the accumulator for another computation.

In such a system, programmers must return an intermediate result to memory. When a processor has two registers, intermediate results can be left in register one, while additional computations are done, using register two. The effect of this additional register is to eliminate a store instruction and allow the multiply to be a "register by register" operation. Because memory does not have to be referenced, register operations are much faster than similar memory operations. In order to derive a meaningful benchmark, however, users are now faced with taking the instruction mix and subdividing instruction types by format. Instruction capability or efficiency, the ability to do more operations with fewer instructions, is also a factor.

The following example illustrates efficiency and the problems it entails for benchmarking. A simulator manufacturer may require 1 MIPS to solve a problem. The instruction mix can be represented by a) % LOADS/STORES, b) % ADD/SUBTRACT, c) % MULT/DRIVE, d) % OTHER. By examining a computer's instructions and execution times, designers find that Brand X computer executes this mix at a rate of 0.5 MIPS. Thus, two Brand X machines are required. Suppose, however, that Brand Y computer company has just introduced a new computer with an instruction set that does twice the work in each instruction that Brand X does. Each instruction, however, requires twice as long to execute. Because of this, the rating for Brand Y is 0.25 MIPS. Although users' jobs could be done with fewer instructions due to higher instruction efficiency, designers looking only at MIPS rating might believe they will need four Brand Y machines to solve their "1-MIPS" problem.

Cache—a further complication

As if instructions and register differences were not enough, another system element that can muddy the waters for software designers is cache. This high speed intermediate buffer between main memory and the processor stores instructions and data requested once by a program. Future requests for the same section of program and/or data are then quickly retrieved from this high speed buffer. Data or instructions retrieved from cache arrive at the processor two to five times faster than the same information retrieved from main memory. Fetching information from cache rather than memory is termed a cache "hit." If the needed program piece is not in cache, it becomes necessary to go to main memory. This is termed a cache "miss." As the information is retrieved from main memory, it is delivered to the cache to be stored in case it is needed again.

The Figure (a) illustrates the placement of the cache in the system. Program steps Y_1 through Y_N [Figure (b)] are used repetitively. The first time through the program, cache misses occur as the cache is filled. The next time through, instructions are retrieved from the cache (hits), and the processor appears to be executing faster. Actually, the processor is not waiting as long for its next instruction. The key is repetition. Only if the program steps are repeated is a cache of value. Program segment X_1 through X_N will not benefit from a cache since this section of code is never repeated.

Notice that the cache in the Figure (a) contains four locations while main memory contains many more. There is good reason for this. Cache is expensive. Designers must balance the benefit against the cost and the benefit is gained in only one way—by using information contained in cache.

Certain types of processing, such as simulation, do very little looping within a single program. In a properly designed system, even simulation benefits from a cache. If the memory system responds to a cache miss by sending the requested word, plus three additional words, the next request for an instruction will find that instruction in the cache. In fact, after the first miss, the next three instructions will be found in cache, resulting in a 75% hit rate. Although this example is simplistic, it shows that a properly designed memory cache system will help the simulation user.

Where hardware is concerned, certain points should be kept in mind when evaluating benchmarks. First, instruction mixes vary. Second, matching architecture causes instruction mix variation. Third, instruction speed depends on

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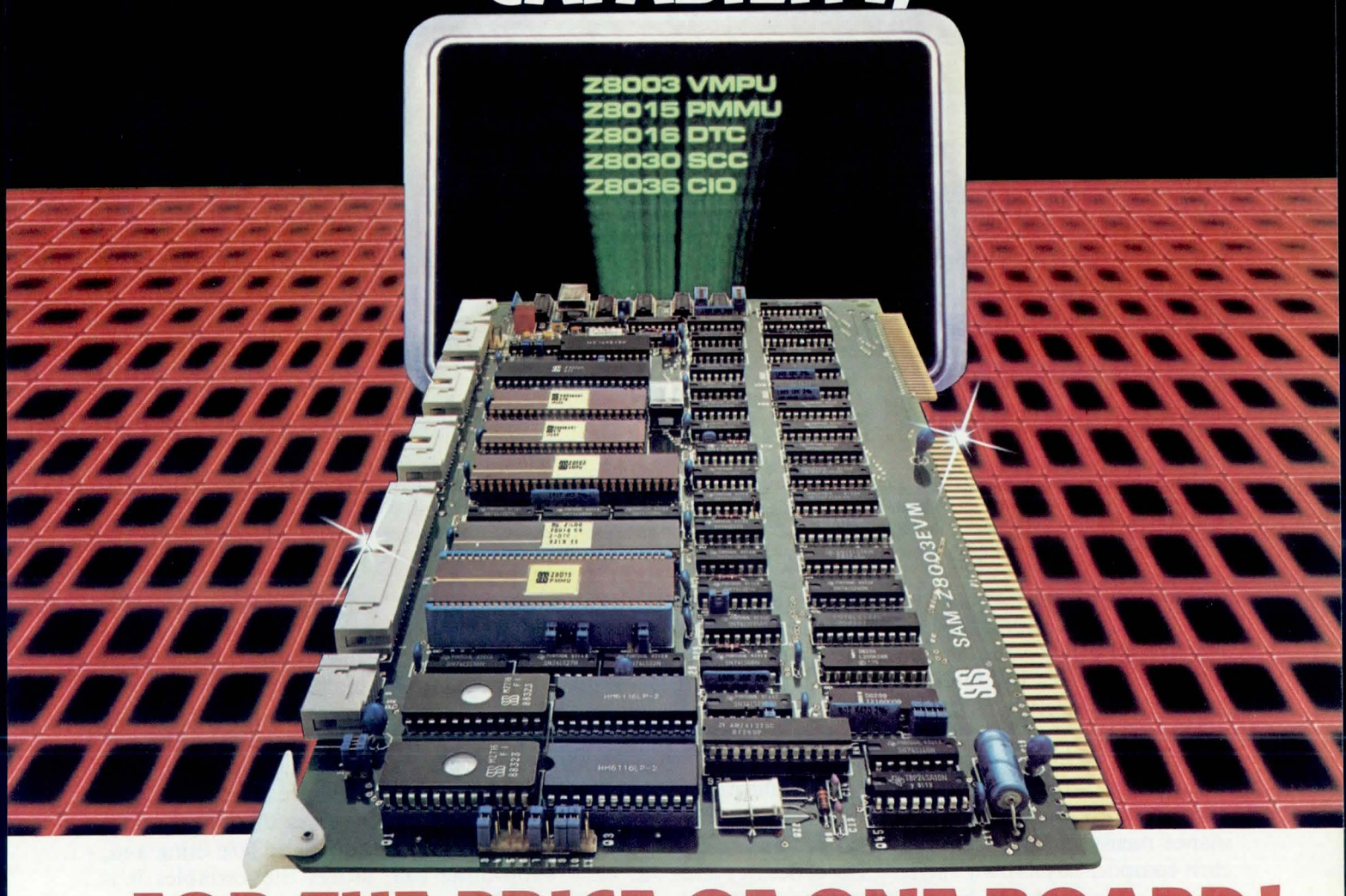

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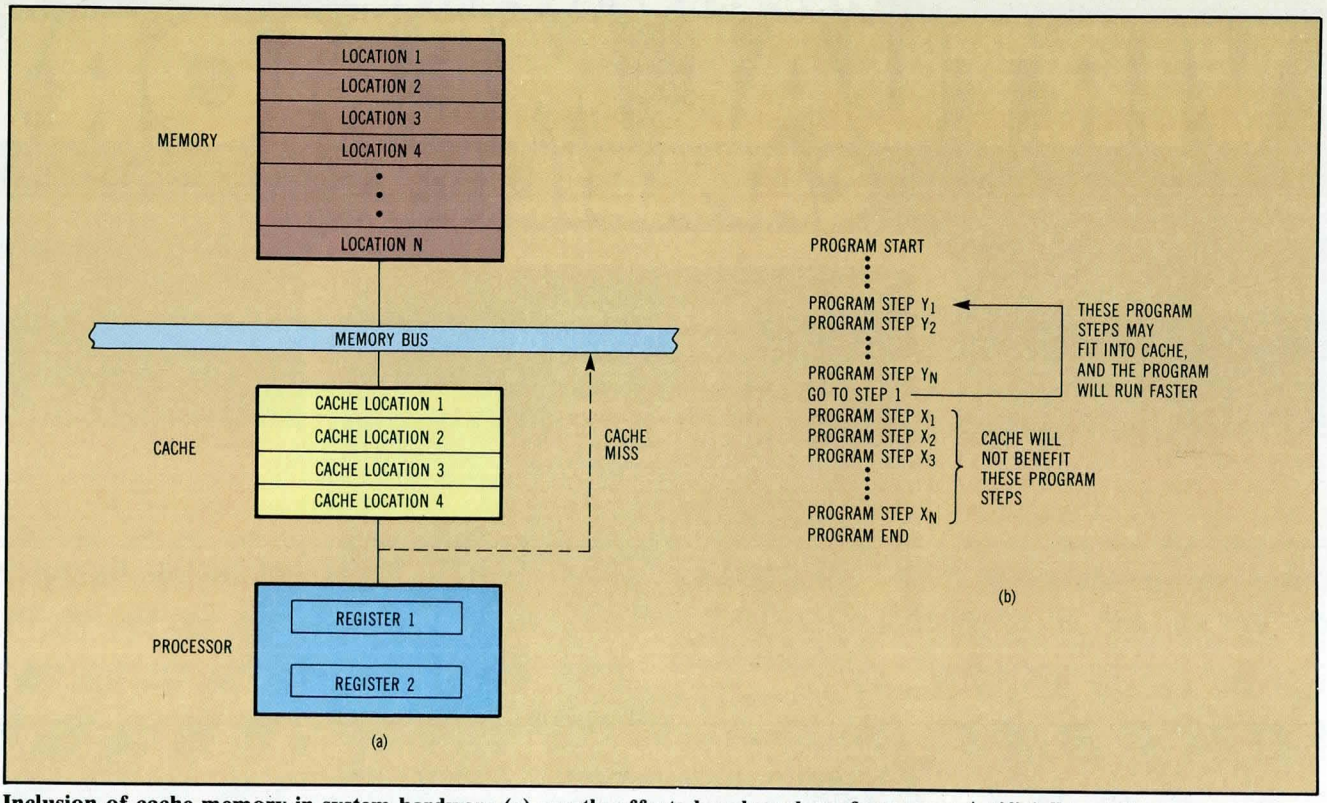

Inclusion of cache memory in system hardware (a) greatly affects benchmark performance. Artificially small benchmarks may reside totally in cache and give false indications of performance. Code segment in (b) between Y_1 and Y_N should not fit entirely in cache. Segment X_1 to X_N will not affect cache since it is not repeated.

instruction format. Fourth, cache will change the instruction execution speed of any instruction, but the overall effect will vary depending upon cache hit rate. Finally, hit rates depend on cache and memory architecture as well as program flow.

The effects of high level languages

Imposing a high level language on applications adds an additional level of complexity to performance measurement. Like individual programmers, each compiler has its own "style." The efficiency and type of code produced has a direct bearing on the amount of hardware required to do the job. To illustrate the effects of compiler technology, two benchmark programs were compiled using three different compiler technologies: block optimization, global optimization, and universal optimization.

The block optimizer breaks a program into small segments and then tries to make intelligent decisions as to how to program the hardware. This is representative of the technology employed by the majority of minicomputer manufacturers. The obvious disadvantage of block optimization is the compiler's limited ability to see the whole program. Since the compiler starts from scratch on each code block or segment, variables used in the first block are returned to memory at the completion of that block. If any or all of these variables are used in the second block, they must be loaded again. The net result is that a large percentage of time is spent repetitively loading and storing to memory.

Global optimization, on the other hand, is a technique that allows the entire program to be seen by the compiler. Because the complete program is considered, the compiler makes smarter decisions about the type of code it generates. As a result, the amount of code is drastically reduced. The globally optimizing compiler has one limitation though—subroutine calls. Subroutines are compiled separately, thereby breaking the flow of the program. Thus, the global optimizer does the safe thing and, at each subroutine call, stores the variables it is using. This is done to ensure that the subroutine has the latest values. So, while code produced in this way is much better than that produced by block optimization, there is still some inefficiency.

An alternative to a globally optimizing compiler is a universally optimizing one. At the user's direction, this compiler allows the automatic inline expansion of subprograms. This feature results in sizable benefits. Not only are needless loads and stores eliminated, but the compiler produces better code because more of the program is seen. This technique fosters structured programming too, since program segments can be tested individually and then compiled automatically. Thus, runtime inefficiencies are eliminated.

To measure the benefits of universal compilation, Perkin-Elmer designers built a performance monitoring unit. This unit, when attached to a Perkin-Elmer processor, counts and times each instruction. It then tallies the results by operation

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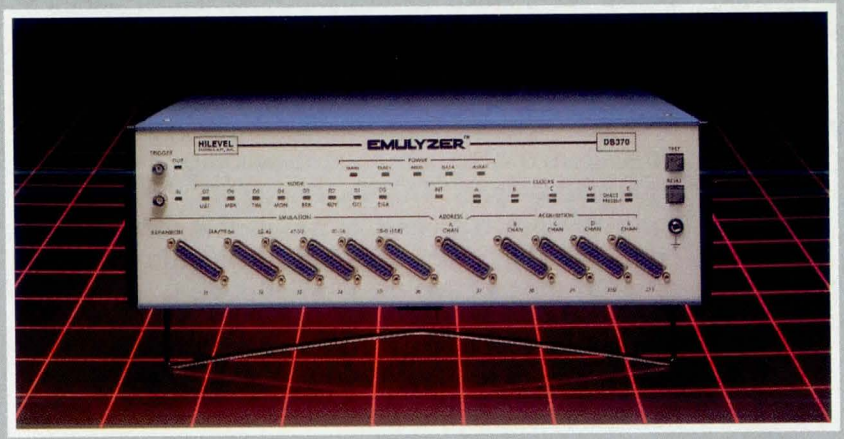

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TABLE 1

Average Execution Times in Microseconds

Benchmark tasks	Operations	Block optimization FORTRAN VI	Global optimization FORTRAN VII O	Universal optimization FORTRAN VII Z
Matrix inversion	Integer/logical	1.512	0.743	–
	Branches	1.134	1.112	–
	Floating point	3.072	2.906	–
Simulation	Integer/logical	1.638	1.775	1.078
	Branches	1.343	1.348	1.325
	Floating point	2.727	2.616	2.506

code and format. Each instruction execution is precisely timed by counting 50-ns clock ticks between instruction fetch pulses. To simplify timing, measurements are taken without cache. The two programs used are a matrix inversion program and a simulation program. The matrix inversion program merely inverts a matrix and then checks the result. This program requires no subroutine calls.

The simulation program, however, calls five major subroutines. Of the five major subroutines called, three request further subroutine calls. Subroutine one calls two secondary subroutines a total of three times. Subroutine two calls three secondary subroutines 11 times, while subroutine three, the most complex, calls eight secondary routines a total of 19 times. The secondary subroutines are passed between 9 and 12 arguments. These subroutines perform variable search and interpolation between two or more points.

Both types of programs were compiled using a block optimizing compiler, as well as global and universal optimizing compilers. Because the matrix inversion program did not call subroutines, it did not benefit from the universal optimizer. Each program was then run on the processor equipped with the program analyzer. The results are summarized in Table 1.

Table 2 shows the instruction format variance when different compilers are used. In terms of execution time, short format (SF) and register to register (RR) are the least costly to execute while memory reference (RX) is the most costly. Obviously, the trend is toward selection of the least costly instructions to do the job. In each case, the number of RX instructions decreases while SF and RR instructions increase as a percentage of the total. The less one has to reference memory, the faster a program will execute. The summary data show that instruction mixes change dramatically, thus proving the point that basing performance evaluation on instruction mix is very misleading.

While all this is interesting, the real benefit of the compiler technology is shown in Table 3. Without changing the hardware in the simulation program, the universally optimizing compiler reduces the job to 15.2M instructions and 26.8 s. This is 61% fewer instruction executions and 64% less time than required for a block optimizer. By means of simple arithmetic, users can determine instruction execution and show how hardware performance, while generally increasing due to faster instruction execution, does not increase 64%. The hardware MIPS rating varies from 0.49 to 0.79 MIPS, depending on the program and compiler. This decrease in MIPS rating also occurred when FORTRAN VII was used in the simulation task. The decrease in hardware performance is offset by the fact that the job was done 41% faster. The MIPS rating, then, does not really measure the true system performance.

Hardware considerations

Not only must the processor MIPS rating be considered, but the entire system's performance must be measured as well. An important reason for doing

TABLE 2

Instruction Mix Expressed as Percentage of Total

Benchmark tasks	Instruction types	Block optimization FORTRAN VI	Global optimization FORTRAN VII O	Universal optimization FORTRAN VII Z
Matrix inversion	SF	16.96	7.33	–
	RR	1.68	65.56	–
	RI	0.04	0.09	–
	RX	81.32	27.01	–
Simulation	SF	22.14	6.24	12.46
	RR	13.51	45.38	45.97
	RI	3.44	5.19	4.61
	RX	60.91	43.19	36.96

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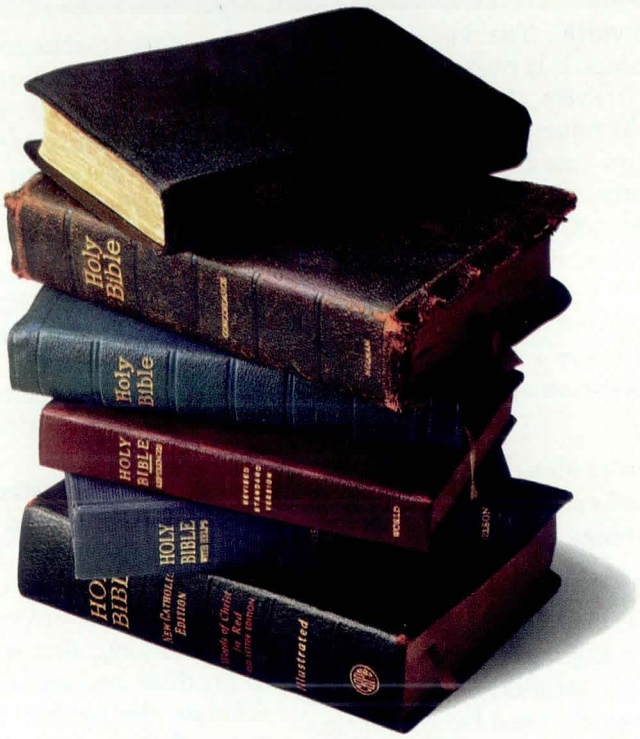

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TABLE 3

System Performance vs Processor Performance

Benchmark tasks	Block optimization FORTRAN VI	Global optimization	Universal optimization
Matrix inversion	10.7M instructions	6.8M instructions	—
	17.9 s	8.6 s	—
	0.6 MIPS	0.8 MIPS	—
Simulation	39.6M instructions	21.3M instructions	15.2M instructions
	74.1 s	43.6 s	26.8 s
	0.5 MIPS	0.5 MIPS	0.6 MIPS

so is system bus bandwidth. The key ingredient here is the system bus, since it is over this path that all traffic to memory travels. Several computer manufacturers have built buses at different widths and speeds. Rating buses has been as esoteric as processor rating systems. Common ratings are 13M, 26M, and 64M bytes/s. The speed of the bus depends on several factors. First and foremost is processor speed.

A good rule of thumb for required bus bandwidth is 8M bytes/s for every 1 MIPS of hardware processor instruction execution speed. This is shown as follows:

1 million 32-bit (4 byte) instructions = 4M bytes/s
If half the instructions need data, then
0.5 million references to memory for data = 2M bytes/s
Total instruction requirement is thus 6M bytes/s

In some cases, this rule of thumb is high and in others, low. It is generally high when using a global or universally optimizing compiler. The extra 2M bytes/s are a slop factor used to resolve contention problems on the system bus, as input/output (I/O) devices also communicate to memory across this bus. Since I/O devices are mechanical, when they are transferring data they require immediate access to the bus. To achieve the needed access, I/O devices are given highest priority on the bus. The processor is the lowest priority device in the system. Since the processor is electronic, it can wait until the bus is free. Of course, the longer the processor waits, the fewer instructions it executes every second. This is called processor throttling. To keep the processor running, in other words, to minimize bus contention, additional bandwidth is required.

So, how fast should the system bus be? That depends on the speed of the processor attached to the bus and the amount of I/O. If the bus is a 13M-byte bus, and the processor is rated at 1.5 MIPS, the rule of thumb dictates

1.5 x 8M bytes/s = 12M bytes/s bus bandwidth

That leaves 1M byte/s left over for I/O. If users exceed the 1M-byte/s I/O rate, then the processor will throttle or slow down to compensate.

In this discussion of benchmarks, physical counts of instructions are accurate and available. In other situations, these data are usually unavailable. Thus, users are forced to evaluate other processors in relation to a known quantity. This clearly points to the need to standardize the terminology.

Actually, the most descriptive concept may be effective system performance. This concept should divorce one from the hardware/software controversy and allow a work-related evaluation measure. High level language benchmarks, can and do, indicate relative effective system performance. However, they may not provide an accurate indication of brute speed.

Conventional methods of rating processor performance only do not give a true picture of the overall system performance. The system, consisting of hardware, software and I/O, must be tested by simulating the production environment. This process, called benchmarking, demands two essential criteria if it is to produce accurate results. First, benchmarks must simulate the production environment. This implies size and flow paths that can negate effects of very large caches. Second, benchmarks must place the proper I/O load on the system. In a system where a processor's required bandwidth approximates the system bus bandwidth, I/O operations will significantly degrade CPU performance. Benchmarks are artificial tests designed to simulate a real world environment. They are not, and never will be, absolute. A good benchmark should, however, place the processor performance within 10% of the customer's application.

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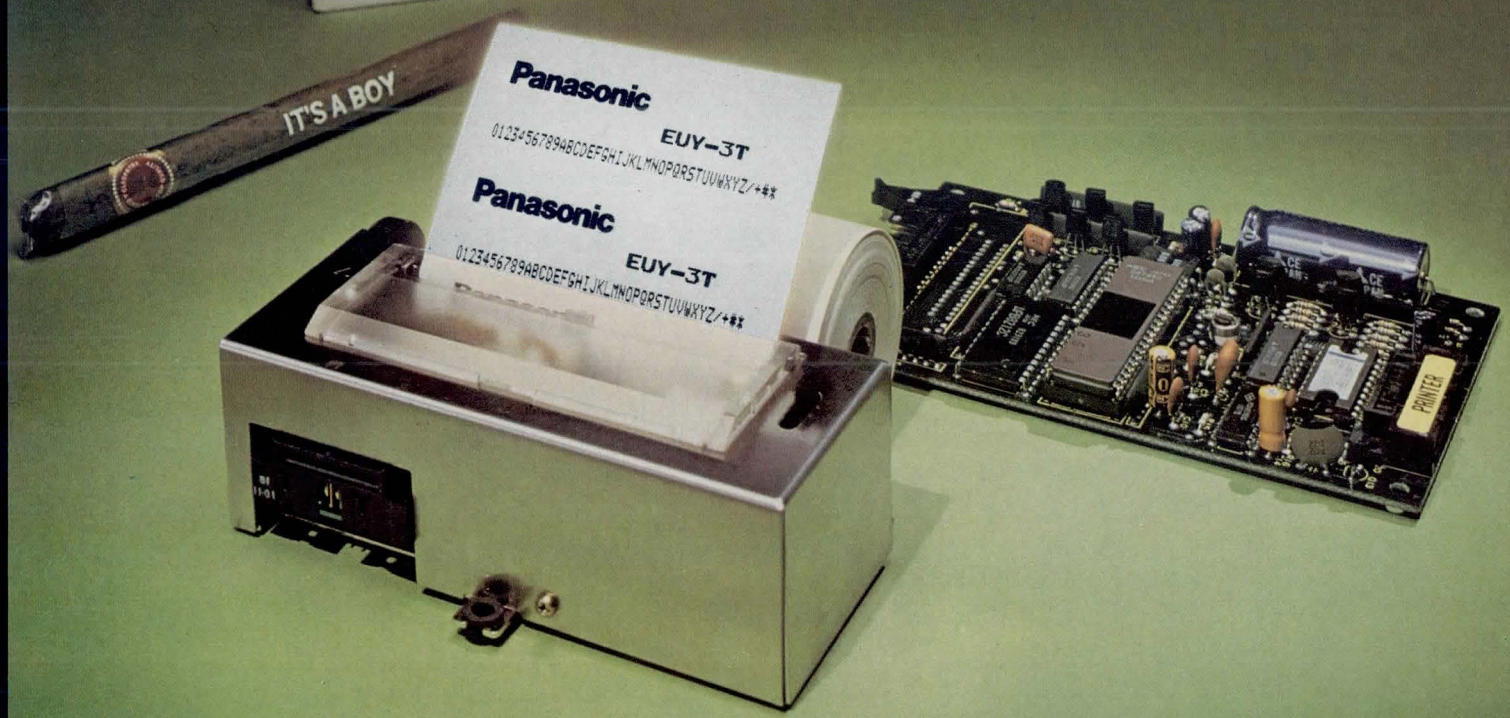

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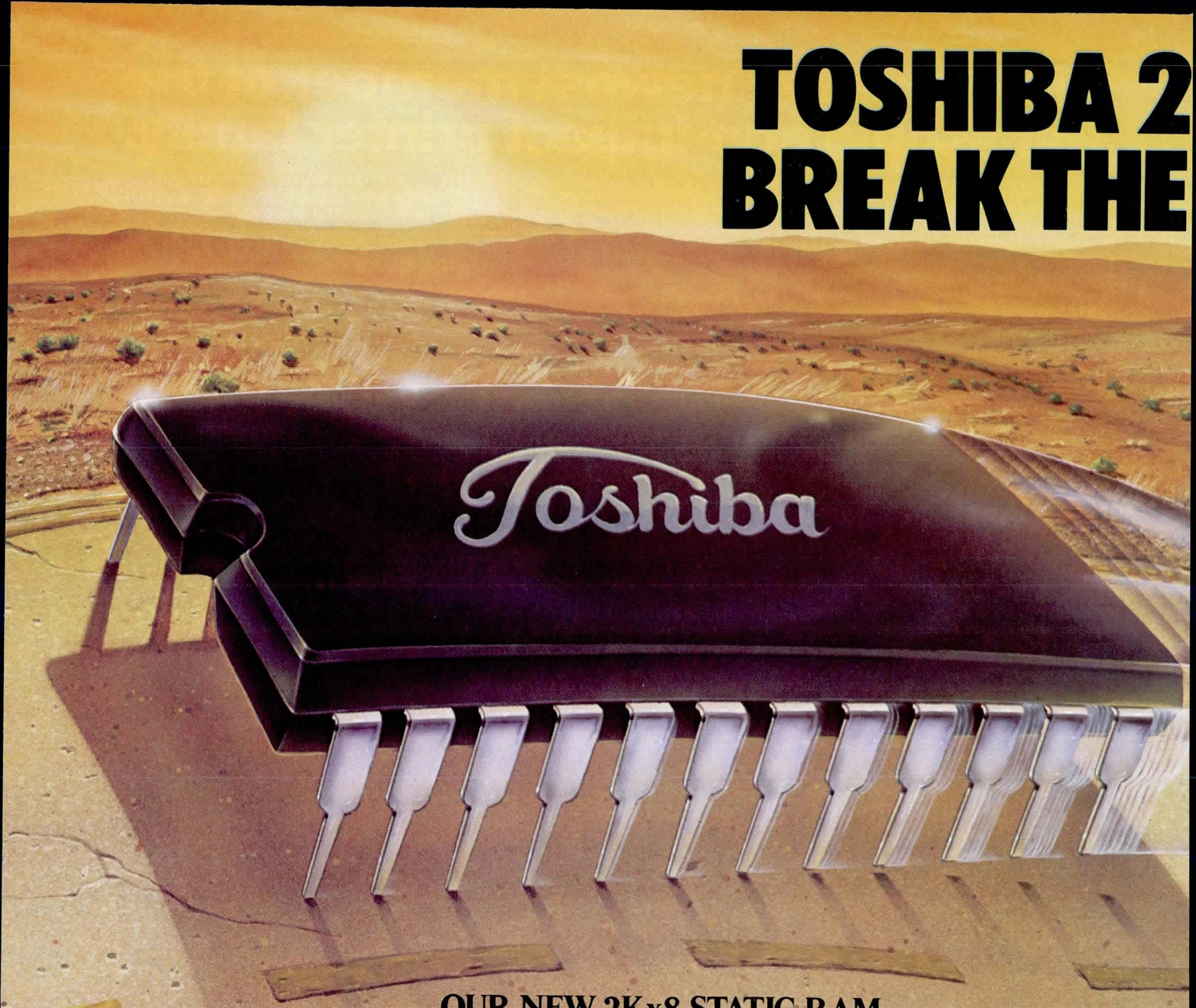

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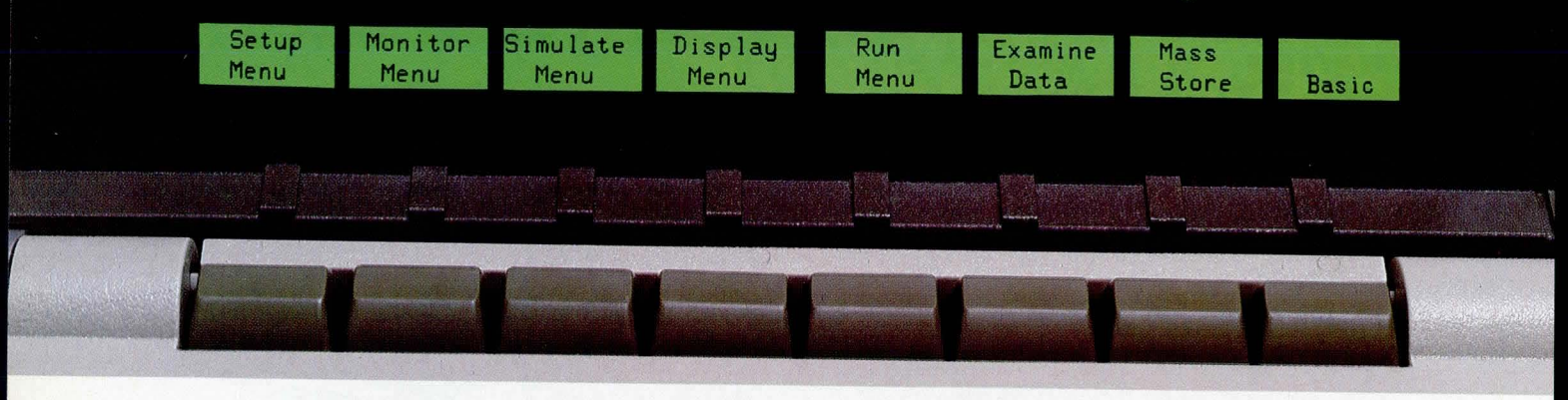

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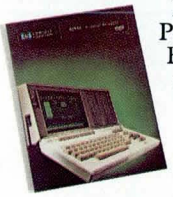

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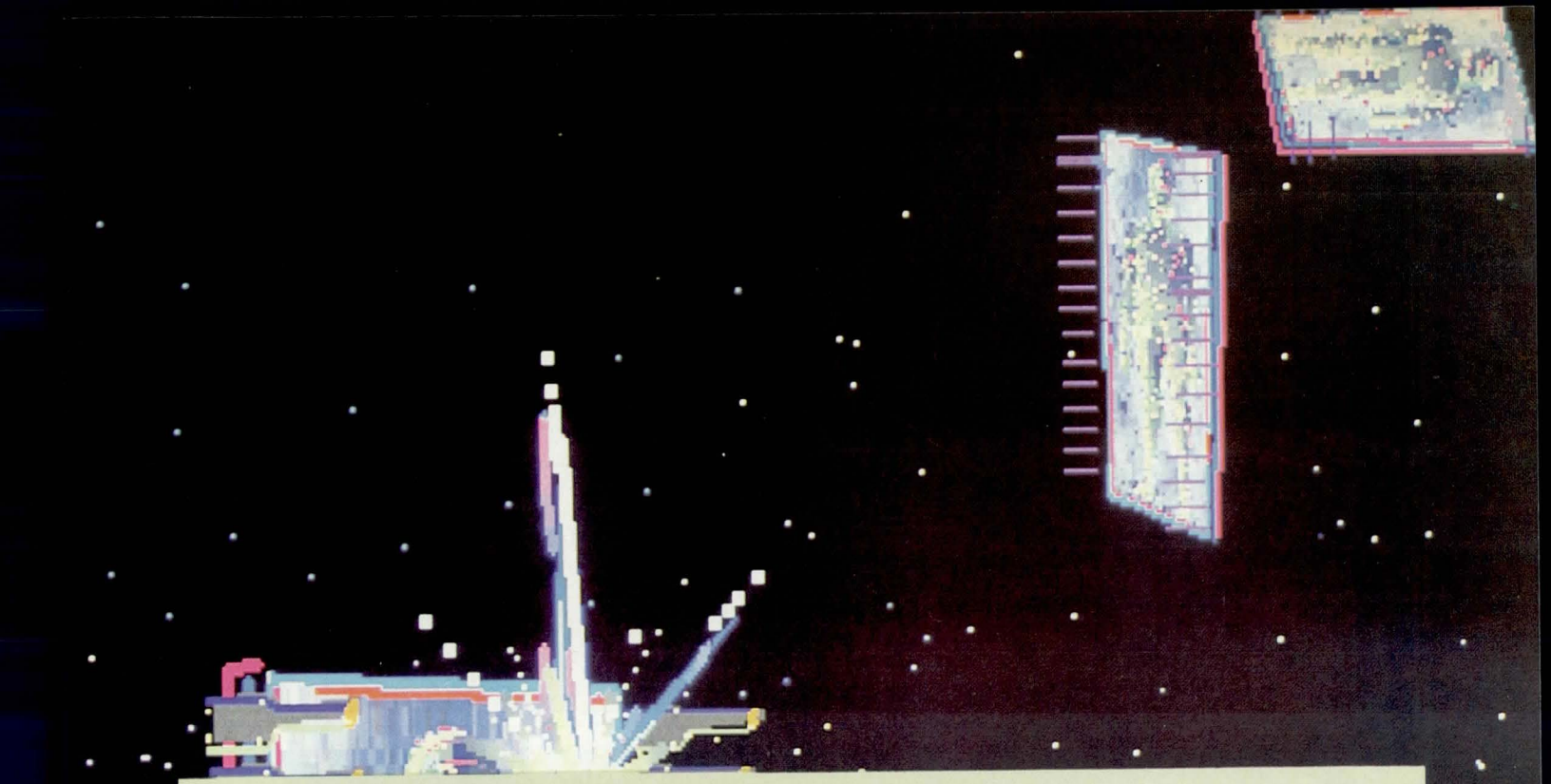


SPECIAL REPORT ON

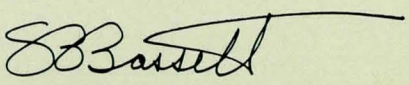
MICROPROCESSORS/ MICROCOMPUTERS

Microprocessor technology never stands still—there are too many bright, creative minds in Silicon Valley and other design enclaves scattered throughout the world. On the horizon is a wave of new developments including 32-bit and ultrafast devices. Thus far, however, these devices have not arrived in significant numbers.

The trend among manufacturers has been to shrink geometries and tweak the fabrication process in order to increase existing chip speeds; increase yields and therefore drop unit prices; and develop CMOS versions to decrease the power required to operate a chip and thus the heat it generates. As VLSI design, manufacturing, and testing have matured, more functions have been brought onchip, freeing board space and easing the system integrator's job. Memory management, instruction pipelining, additional registers, and 32-bit capabilities have all been implemented in this way.

Most microprocessors have been used in dedicated control applications, and the number of different varieties keeps growing at an exponential rate. By and large, 8-bit devices are replacing 4-bit ones, and dedicated 16-bit controllers have recently appeared on the market.

All of these trends have developed relatively slowly and steadily—advances in fabrication and process control develop over time with experience. The 32-bit chips and architectures still in the experimental stage should begin to become important late next year, with strong growth in 1985 and beyond. Comprehensive tools for end to end automated chip design, user-microprogrammable chips, and innovative architectures using reduced instruction sets and high speed emitter-coupled logic are on the way. Indeed, the next three years should prove very interesting.



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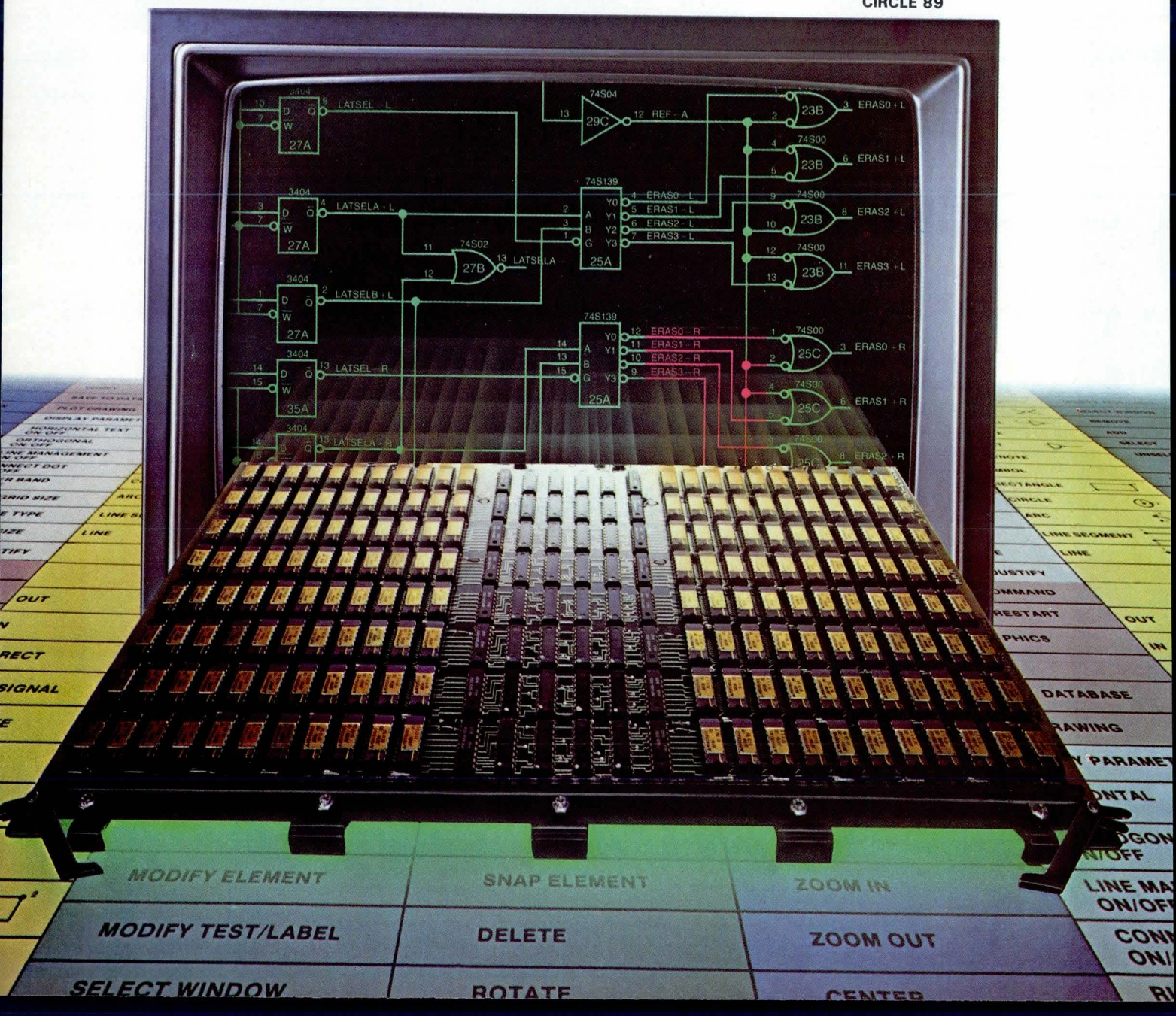

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21 MIPS–Move over VAX and MV/10000, the fast lane belongs to Perkin-Elmer.

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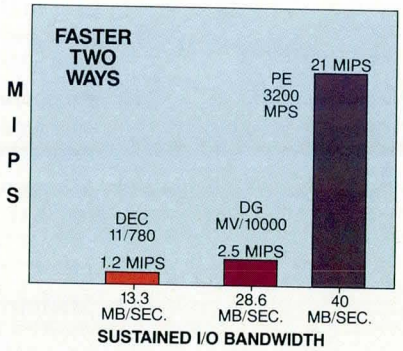

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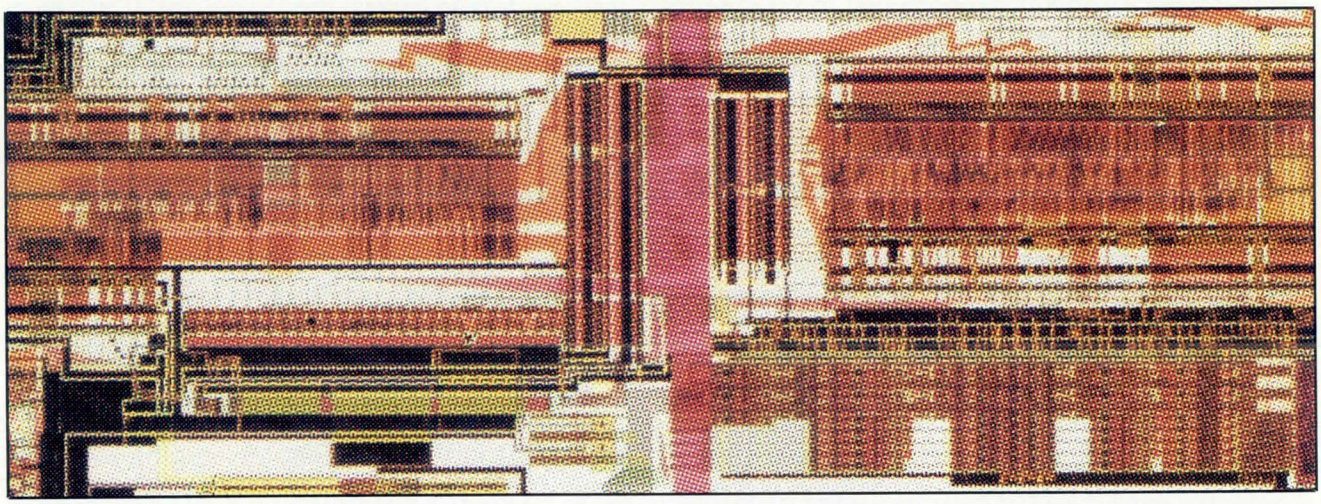
MICROPROCESSORS: SPEED UP, PRICE DOWN, AND CMOS EVERYWHERE

Shrinking geometries increase speed, improved yields drop prices, and CMOS technology decreases heat and power.



by Sam Bassett,
Field Editor

This is a year of evolution and development—not revolution. Although there have been (or soon will be) announcements of several 32-bit microprocessors, the real progress has been in increased yields and reduced prices of 16-bit parts. Eight-bit chips (mainly the Z80 and 6502 variants) still dominate in terms of sales and are expected to do so for the next several years. This is especially true since they are beginning to replace 4-bit parts in control applications.

Four-bit microprocessors are not dead, however—as a sales rep from Texas Instruments (Dallas, Tex) says, "We can't kill off the business!" But little design effort is being made to put them into new products. Given the wealth of software and hardware tools available for 8-bit machines, it is easier (and generally as inexpensive) to use the 8-bit units as it is to use a 4-bit controller. In addition, companies like Rockwell International, of Newport Beach, Calif, (the R6500 series), TI (the TMS1000 series), and Motorola, of Austin, Tex, (the 6800 series parts) have put significant effort into bringing functions onchip, and building parts optimized for controller applications.

Examining the main trends

Manufacturers continue to work toward optimizing design and fabrication to increase working chip yields. This lets them sell more parts at a lower price, or increase the profit/part. Besides price, experience with controlling fabrication, along with shrinking geometries, has enabled an increase in processing speed. From 1 to 2 MHz three years ago, Z80s have accelerated to 6 to 8 MHz, with 10-MHz parts available on a limited basis.

Complementary metal oxide semiconductor (CMOS) processes, while still fractionally slower and more expensive than the alternatives, have also been the focus of much development effort. This is because they require less power and tolerate more heat. As circuits become denser, especially in very large scale integration (VLSI) devices, the amount of heat generated by the power needed to run the chip becomes a problem. Power supplies also generate heat and are expensive. CMOS alleviates both heat and power problems, since it consumes much less power than competing high performance MOS (HMOS) or N-channel MOS (NMOS) processes.

Depending on the circuit being built, and the designer's experience with CMOS design and fabrication, it is possible to achieve power ratios (HMOS:CMOS) from 3:1 to 10:1. A fairly typical example is the 16032 from National Semiconductor (Santa Clara, Calif), which draws approximately 180 mA of current in the HMOS version, in contrast to 50 mA in CMOS for a 3.6:1 ratio. Since junction temperature is roughly proportional to power consumption, CMOS devices run much cooler than their HMOS equivalents. CMOS is also well suited for military applications because it operates reliably at 125 °C. Other device types reach the outer limits of their performance at that temperature.

Silicon is cheap, while software is expensive. The factor that will sell a given microprocessor in the years ahead is support (see Panel, "The designer's perspective"). Designers will increasingly opt for devices with extensive hardware and software support. No matter how good and inventive a microprocessor's architecture may be (see Panel, "Taking a RISC on new architectures"), few managers will pay for reinventing the wheel. The availability of assemblers, compilers, and hardware development systems, as well as instruction-set compatibility, indicates that the 86 family from Intel (Santa Clara, Calif) will have a long and fruitful life (see Panel, "Steady evolution at Intel").

The workhorse—the 8-bit microprocessor

Estimates indicate that more than 75% of all microprocessors are used for embedded control applications, with the remainder found in Apples, IBM PCs, and other microcomputer systems. Price competition and second sources—the *IC Master* lists 32 chip makers, of whom five, besides Zilog (Cupertino, Calif), produce Z80s or Z80-compatible microprocessors—give manufacturers a compelling reason to improve their manufacturing processes.

The work done to improve yields also creates increases in speed. As the fabrication process matures and becomes better controlled, the understanding gained lets the process engineer tweak the chip's parameters for better performance. A well-characterized device also makes scaling down the geometry much easier. As the point-to-point distances onchip and the capacitance of metal interconnect lines shrink, chip speed increases. In addition, as more consumer products (ie, automobiles, ovens, and toasters) become more intelligent, the microprocessors built into them must handle more tasks, and faster.

Consumer applications also impose power and heat-dissipation constraints on embedded microprocessors. This is where CMOS proves highly advantageous. All major chip houses have active CMOS development projects, and most are already shipping some CMOS parts. At National Semiconductor, designers reportedly have to show good reason for developing in anything but CMOS. Intel has also made a major commitment to CMOS.

Given the price/performance/power constraints, and since the majority of the parts go into controllers, most of the recent development work in 8-bit microprocessors has gone into single-chip microcomputers and microcontrollers, and not into unadorned central processing unit (CPU) chips. The sheer number of variations on the basic theme is overwhelming. A buyer can get single-chip microcomputers with read only memory (ROM), programmable ROM (PROM), erasable programmable ROM (EPROM), or electrically erasable programmable ROM (EEPROM). Also available are analog to digital or digital to analog converters; 256 to 1K bytes of random access memory (RAM); onboard universal synchronous/asynchronous receiver transmitters (USARTs); and much more.

Some typical controllers

Motorola's venerable 6800 family continues to grow, with no end in sight. According to a company spokesperson, many of the variants came about due to the specific requirements of large-volume customers. The company's policy is to encourage standard part use rather than putting design effort into new ones. While this is true, an order for several 100,000 parts/year, over two or more years, is a good justification for developing a new standard part.

One of the most interesting controllers is the 6804 serial device. Unlike most other processors, it operates internally at several times the external clock rate. All input data are handled over one line, and a latch is used to talk to 8-bit devices (eg, RAM) over the system bus.

The most intriguing 8-bit device introduced in the last year, and the most significant in its future implications, is TI's TMS7020. Seeq Technology (San Jose, Calif) offers the identical device, but calls it the 72720. The device (from both companies) has onchip EEPROM, which allows data or program instructions to be changed at will, yet remain when the power is off. Applications in robotics and

The designer's perspective

Chuck Peddle, 6502 designer and president of Victor Technologies (Scotts Valley, Calif), and his chief designer, Bobby Taylor, provide an informative look at the impact of microprocessor architectures on system design, and the decisions that need to be made when choosing a particular processor. In their analysis, the two issues in processors—putting more functions on silicon, and Reduced Instruction Set Computer (RISC) architectures—provide a starting point.

Both Peddle and Taylor believe that RISC devices are a long way from being commercially important products. Although microprocessors started out with very small instruction sets, designs have evolved, adding more and more functions to either the microcode expansions, or to actual hardwired logic. This expansion has come more or less at the expense of speed. The other approach—a very simple but very fast instruction set—is a matter of choosing the right subset, according to Peddle and Taylor.

To Peddle, basic speed is not of paramount importance. In the 6502, for example, separating the data and address lines allows the machine to run twice as fast as an equivalent Z80, given the same clock rate. The Z80 must multiplex address and data information over the same set of lines.

The basic argument for RISC architectures assumes that most programmers code in high level languages. Given this, the current state of compiler writing makes it possible to generate code that will run faster on a less sophisticated (but inherently faster) instruction set machine. This is significantly better than having this code run on a machine with a complicated but powerful instruction set.

Both Peddle and Taylor see a tendency toward integrating more functions onchip in the next few years. They foresee many special purpose controllers, like the 8048, with additional functions. The technique is fairly easy, since the architecture is well known. The question is mostly one of finding useful functions, packaging them, and taking advantage of existing technology. According to Taylor, the reduced instruction set has a good chance of becoming important, but is more applicable to the higher performance end of the spectrum. "It's going to take a fairly long time to become practical, though," he says.

Support is sometimes lacking

As system designers, Peddle and Taylor feel that vendors often build the wrong set of peripheral chips. The peripheral chips needed to support a given family tend to lag behind processor and support software development. Because the peripheral chips available are not that well thought out from a system standpoint, designers must then create special purpose subsystems.

When Peddle and Taylor decided to put Intel's 8088 into the Victor 9000, they evaluated three main candidates—the Motorola 68000, the 8088, and the 6502 "plus." The 6502 "plus" comes in three configurations: a 6502 plus a second 6502, a 6502 plus a Z80, or a 6502 plus a 6809. All three 6502 "plus" configurations were viable candidates featuring a shared processor scheme. The 6809 had an interesting instruction set and 16-bit internal operations, but

Chuck Peddle (left) and Bobby Taylor (right)

suffered from a lack of software support. This left the Z80—in fact a 6502/Z80—which remained a viable contender for a long time.

Comments Peddle, "We finally concluded that the 8088 was going to be a cheaper solution in the long term. It may not have been the right decision—we might have done better to use a 6502 plus an 8088." What helped convince them, however, was the fact that Intel was shipping the 8088, second sources had become available for it, support-oriented companies were also shipping the product, and it looked like good compilers would be available soon thereafter. What finally sold them was that Bill Gates of Microsoft (Bellevue, Wash) could provide a lot of the software.

The 8088 also solved the biggest drawbacks of 8-bit processors—addressability and the 64K limit. Getting around the 64K limit would have entailed using bank-switching schemes and creating unique, nonportable software. Says Peddle, "It looked like there was a reasonable migration path from the 8080/Z80 family to the 8088. Yet, because it was software compatible with the 8086, the 8088 had some of the cost benefits of the 8-bit processors, but the power and software availability of the 86 family." At the time design began on the Victor 9000, Peddle and Taylor did not know about the IBM PC, but had confidence in Gates, and that the programs and tools he had available for any given 16-bit processor would also be available for the 8086.

Another consideration was that the 8086 was used in the IBM Displaywriter. According to Peddle, this provided Victor Technologies with a good clue as to which way IBM was leaning. To Peddle, the choice of the 86 for the Displaywriter was a good sign that IBM would also use the 8088. In the end, the final consideration in choosing the microprocessor for the Victor 9000 was software support.

"I'm not convinced that the market will ever respond as positively as you would intellectually to great microprocessors," comments Peddle, "I think it does respond to the vendor that looks like a viable supplier." Summing up the biggest factor in choosing a microprocessor, Peddle adds, "The bigger the processor, the more you need other people's software to support it."

dynamic process control are obvious, but the implications are even greater.

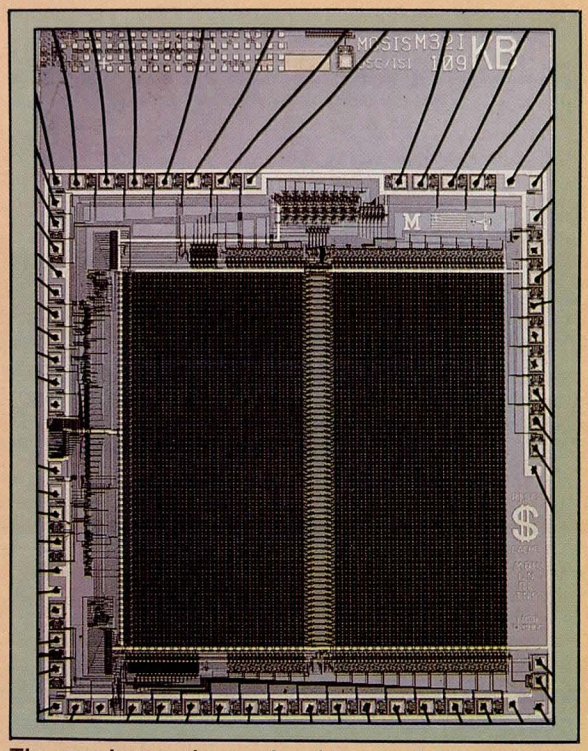
The microcode that defines a CPU architecture is currently stored in ROM. Implementing microcode in EEPROM will allow the chip's instruction set to be tailored to a specific application. The problem of object-code compatibility would thus greatly diminish. Given two reasonably similar architectures (ie, if the processor is executing a program in 6809 code, and the next program in the queue is written for the 6800), a simple direct memory access (DMA) request could download the new architecture into the processor.

Zilog's Z800 is the exception to the stampede toward microcontrollers in the 8-bit world. The chip combines a CPU that runs all documented Z80 instructions with a memory management unit (MMU) that can address up to 16M bytes of memory. However, onchip RAM, clocks, universal asynchronous receiver/transmitter (UART), counter/timers, and DMA controllers parallel the developments in other new 8-bit devices. The device is positioned between the Z80 and the Z8000, and designed to provide a graceful upward transition. It is described as compatible with the company's recently announced Z80,000 32-bit device.

Taking a RISC on new architectures

For quite some time, RISC has been the focus of extensive research at the University of California, Berkeley. At the forefront of this work has been Dr David A. Patterson, an associate professor in the electrical engineering and computer science department there, and his students. Now, according to Dr Patterson, the RISC project is wrapping up, and the design group is going into the final stages of publishing the research.

One of the most important results of the research is RISC II, a microprocessor with a 32-bit multiplexed address data bus. Its large register set has an instruction set that is hardwired (implemented in logic circuitry) rather than microcoded. RISC II was designed by students in approximately a year and a half, and fabricated by a commercial chip maker.



The RISC instruction cache chip was fabricated in NMOS. It has a 250-ns access time, with a 480-ns cycle time. Thus, it is compatible with the 500-ns RISC II CPU.

Dr Patterson claims that RISC II is a better silicon implementation of RISC than RISC I and works quite well at the speed for which it was designed. On its design, he comments, "Our original architectural evaluations were that we could build a device which would execute an instruction every 400 ns. RISC II was designed to run at one instruction every 480 ns, and it actually executes one every 500 ns."

In a separate project, Dr Patterson's group also completed the design of an instruction cache. The group was shooting for something compatible with RISC, which runs at 500 ns. The instruction cache also ran on first silicon at 500 ns.

Another project was undertaken to answer the question of whether the RISC architecture only makes sense in silicon, or whether different technologies and more transistors/chip would render RISC impractical. To answer this question, Dr Patterson had a student do a master's thesis and design which included the use of the schematic capture and logic design (SCALD) system by Valid Logic (Sunnyvale, Calif). The purpose of this project was to do logic simulation and timing analysis on the design of a 100k emitter-coupled logic RISC implementation.

The SCALD system was used to predict the performance of the Big RISC (B-RISC) machine on three different benchmark programs. This performance was compared with that on a number of different existing machines, such as the Amdahl V70, IBM 3081, and VAX-780. Even given the most pessimistic estimates, the simulation indicated that the machine would run almost 1.5 times as fast as the nearest competitor, the Amdahl V70.

RISC machines produced at the university are designed to run high level language programs, and to handle only integer arithmetic directly—not floating point calculations. The philosophy behind this choice is that several companies are developing specialized processors that could interface with the RISC CPU. Also, including various functions onchip would significantly slow it down, as well as lengthen the time needed to design the chip. Dr Patterson is a firm believer in replacing software by silicon, thus offloading as many functions as possible from the CPU.

Register windowing

TI's 9900, and some of the bigger machines, have separate register sets for interrupt switching, but the RISC architecture includes them for every procedure.

Since 1980, 16-bit devices have been the center of attention. MS-DOS and CP/M-86 on the Intel 8088, and Unix on the Motorola 68000 are the hot items in the microcomputer world. Since the technology is newer, there are fewer players and fewer second sources, and not all of the announced parts are equally real or available. There is a significant difference between delivering engineering evaluation samples of a part, and shipping commercial quantities. Throughout the electronics industry, announcements depend on marketing realities, while shipment depends on the much tougher fabrication and testing realities.

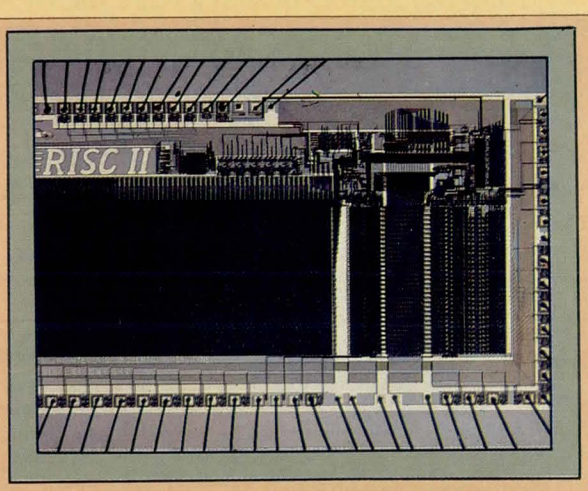
While in many cases announced products never materialize, there can be no question about the reality of the 9900 and 99000 series from TI, or the Z8000 from Zilog. The 9900 series, patterned on TI's minicomputer architecture, has been in production since the late 70s. It is described as being optimized for program context switching, since all registers and stacks are kept in RAM. The Z8000, introduced in 1980, is also register oriented and addresses memory via segment registers. Designers have widely accepted both companies' products, although the Z8000's similarity to the Z80 has led to greater use.

According to Dr Patterson, this is because measurements show that procedure calls happen 100 times more frequently than context switches. Overlapping the registers this way brings the cost of a processor call or return down very low—an order of magnitude faster than other machines. Pyramid Computer (Mountain View, Calif) has picked up on this idea and integrated it into the otherwise traditional 90x microprogrammed computer, which the company has just introduced (see article this issue, p 54). There are various rumors that other companies are doing comparable work in research projects and product development.

The professor believes that there is an important segment of the computer industry that does not care about assembly language programming. In the future, he hopes that people will design systems where the users write in high level languages and use operating systems that can move from one machine to another. When that happens, says Patterson, there will be tremendous opportunities. It will be possible to change architectures as the technology moves, without losing the software investment. "That's really what the RISC argument boils down to," notes Dr Patterson, "coming up with a chip that doesn't take forever to design, and being able to track the technology."

Design tools, like SCALD, CAESAR, and John Ousterhout's Crystal, help substantially and work best with simple architectures. As design tools improve, simple architectural designs can be completed faster. According to Dr Patterson, in a technology that gets twice as good every year or two, being able to design a system to hit the market in two years becomes not only desirable, but a necessity. He comments, "I'd rather put the work into being able to do that, than try to figure out what will make sense in 1988—you have to be real smart, or lucky, to do that."

Right now, Dr Patterson and his group are trying to design "tomorrow's microprocessor with yesterday's technology." As the professor points out, they can use "pretty old" technology, and still come up with a microprocessor that runs C programs very fast—faster than the 12-MHz 68000, the 16032, the HP 9000 CPU, and the 286. According to Dr Patterson, "It seems strange that universities, in a year or so of a student's part-time work, can come up with a microprocessor competitive with, or better than, what the established manufacturers have done."



RISC II, a 32-bit NMOS microprocessor designed at the University of California, Berkeley, is 25% smaller than RISC I, even though it has 75% more registers. Using an 8-MHz clock, it executes instructions in 500 ns and consumes 1.25 W.

In considering whether this university advantage might be due to the design tools available, and if the average designer in industry has such tools, Dr Patterson states that the Berkeley design tools set had been distributed to more than 100 locations, including several manufacturers. Another factor, according to Dr Patterson, is the cultural difference between industry and the university. On the basis of past experience, manufacturers expect that a new chip design will take three to five years and cost $30 million. Thus, they make their corporate plans accordingly.

Universities, on the other hand, do not have the time or resources to devote to that extensive a project. Instead, there is a premium on quick results. The professor also expects that as the marketplace becomes more competitive, companies will be pushed more into using design tools with better yields and more capability to produce parts more quickly.

Dr Patterson puts the situation into perspective when he says, "It will be easy to continue taking a long time to build microprocessors as long as everyone plays the game the same way, but the question is, what happens when other people start playing the game differently?"

Similarly, Intel's iAPX 86 family of parts is in widespread use, with the 8088 in the lead. Since it allows designers to configure systems around well-known and reasonably inexpensive 8-bit bus and peripheral technology, the part is well on its way to becoming the successor to the 6502 as the workhorse of the microcomputer industry.

The full 16-bit bus members of the family are following along, but without the shipment volume associated with the 8088. The 8086 has found a steady market in technical systems, and the June announcement that Harris Semiconductor's CMOS Division (Melbourne, Fla) has introduced a CMOS version—the 80C86—will ensure its future, especially if the projected fall '83 shipping schedule is met.

In addition, the enhanced members of the family (iAPX 186 and 286) seem to be doing well. The 186 is available in quantity. It provides direct addressing of up to 1M byte of memory, a 4M-byte/s (1M-bps x 16-bit) bus transfer rate, a 6-byte prefetch queue, and 16-bit registers for memory segmentation, via its onchip bus interface unit (BIU). The device also has an onchip clock generator, programmable interface controller, timers and control registers, a local bus controller, and a DMA unit. Intel also provides development software consisting of an assembler; PL/M, Pascal, and Fortran compilers; a set of system utilities; and an in-circuit emulator to interface with its microcomputer development systems.

The 286 integrates even more functions onchip, thus reducing the chip count, and reducing signaling and propagation delays (see Jim Slager's article, "Advanced Features Squeeze onto Processor Chip," p 189). For the most part, the sample quantities released thus far have lived up to the specifications Intel has published. But true production quantities and prices are just not available yet.

Sixteen-bit controller architectures, analogous to the 8-bit ones, are in the cards as well. Intel is using a "96" in the part number to designate microcontrollers. The company has announced and is shipping 8096 controllers, and is talking about a 196. A continuation of the general policy will probably bring a 296 to market in a couple of years, as well as a 396, and so on through the product line.

Coprocessors add functions

In 16-bit chips, coprocessors are the interesting technical innovation. These chips share the bus with the main CPU and intercept certain commands in the code stream to perform specialized tasks that

Steady evolution at Intel

Giving a clear indication about the future of Intel's microprocessor line, senior vice president Les Vadasz comments, "We are committed to two main paths: first, to take existing microprocessors and reduce the cost of solutions by integrating as much onto the silicon as technology allows; second, to extend the architecture in a compatible manner using advanced silicon technology to produce more powerful CPUs."

According to Vadasz, the 8086, 186, and 286 all illustrate the direction the company is taking, and future parts will, of course, reflect this philosophy. Meanwhile, maintaining architectural compatibility is paramount to ensure easy and direct integration. Although the company maintains a strong R&D effort, there are currently no plans to change architecture, or to produce microprocessors that do not reflect the 8086 family philosophy.

The general thrust of 86 family development has been to provide both more power and functionality with new parts. This is evident with memory management in the 286, and the same functionality in a smaller and less expensive package (ie, the 186 as compared with the 8086).

Semiconductor fabrication techniques are advancing rapidly, and, according to Vadasz, million-transistor circuits are well within reach. While the company currently uses 2-μm technology (the smallest features onchip), 1.5- to 1-μm chip technologies are being developed. They are, as Vadasz claims, "coming soon," but he declines to say when.

In discussing the 432, Vadasz maintains that the unit does, indeed, fit into the overall company strategy for microprocessor development. He does admit, however, that the 432 is mainly being used in fault-tolerant applications. He also notes that continuous improvements are being made on the unit, although the same amount of effort (smaller geometries and more speed) is not being devoted to it.

Despite the fact that "4-bit parts are dead at Intel," as Vadasz points out, the 8-bit microcontroller and microcomputer are very much alive. The 803X, 804X, and 805X parts are being manufactured in large volume. In controller applications, 16-bit processors are being used, and Intel is producing the 8096, a dedicated controller that shares the 86 family architecture. Theoretically, there is no reason why there could not be a 196 or 296, but neither is being discussed at present.

Intel is currently working on CMOS applications (mainly because of power considerations), even though CMOS is more complex and expensive than NMOS, and its processes permit fewer gates per given area. Comments Vadasz, "It doesn't make much sense to have a low cost 10-W chip." Since both power and heat become serious problems as the number of onchip functions increases, the heavy investment required to scale down CMOS is seen as being cost effective in the long run.

Future technologies, such as gallium arsenide, Josephson junctions, and 3-dimensional architectures (multiply layers of active and passive devices) are also being monitored at Intel. At present, these technologies are seen as too expensive and too little understood. They will have to wait for commercial development and until a real need arises.

For now, the company's attitude is basically cautious—to move ahead carefully and provide products and services for which there is an established engineering demand. Yet, the company also keeps abreast, or slightly ahead of, current technology.

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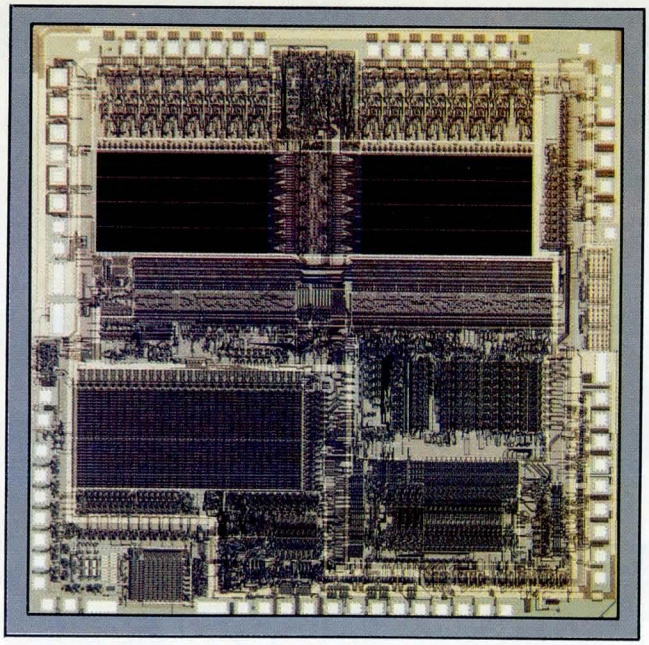


Intel's 8096 is a dedicated 16-bit microcontroller. Like the 8048 and 8051, it is an architectural implementation of the current microprocessor generation, with added functions and RAM onchip.

would seriously slow down the main CPU. Intel's first floating point unit (FPU) coprocessor, the 8087, is now being delivered, and significant numbers are going into sockets provided for them on microcomputer motherboards. The 187 is being sampled, and seems to be doing well, but the announced 8089 MMU seems not to have taken off at all. It is unclear whether this is due to technical difficulties in making the part work, or the fact that this function is being brought onchip in the advanced parts (186 and 286).

Motorola is shipping 16-bit parts, and the 68000 has taken the Unix and technical worlds by storm. Its orthogonal (very regular) instruction set, ability to address up to 16M bytes of memory without segmentation, as well as separate address and data buses, have given it a reduced overall part count and a conceptual advantage over devices that multiplex data and address information over the same lines.

In addition to the 50 or so smaller computer system manufacturers who offer the UniSoft (Berkeley, Calif) Unix port, both IBM (Armonk, NY) and Hewlett-Packard (Palo Alto, Calif) are shipping advanced laboratory systems based on the 68000.

The basic CPU is available in five clock speeds, from 4 to 12 MHz. Given the general push for higher speeds and functionality, the higher speed versions will probably be more widely used than the 4-MHz parts, especially as fast RAM becomes less expensive.

Just as Intel has produced the 8088, Motorola offers the 68008, an 8-bit bus variety. The technical system niche that the 68000 seems to have staked out as its own is less concerned with price and more willing to put in the extra design work necessary to produce a full-function 16-bit system. Therefore, the 68008 is not expected to be as popular as the 8088.

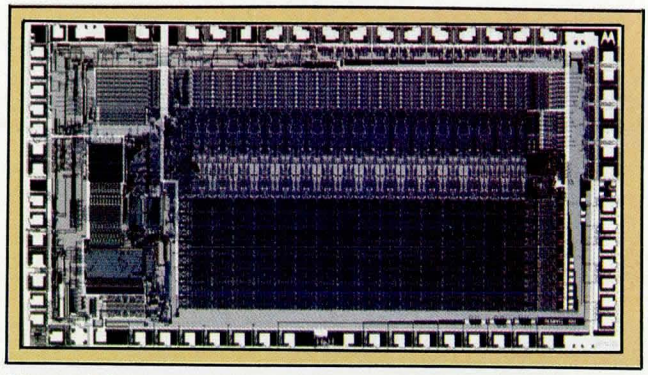
Motorola has announced its intention to put out floating point (68881) and memory management (68451) coprocessors for the 68000, as well as a complete line of peripheral controllers. The 68451 MMU is likely to suffer the same fate as Intel's 8089, however, since the 68010 CPU with onboard memory management will be in production before designers learn how to use it. While Motorola has not yet announced plans to produce dedicated controller chips for the 68000 family, the company is not likely to ignore demands for these functions when they develop. Meanwhile, United Technologies Mostek (Carrollton, Tex) has announced the 68200, which should spark that demand (see "Microcontroller Addresses Control and Instrumentation," by Don Folkes and John Bates, p 229).

Another orthogonal architecture

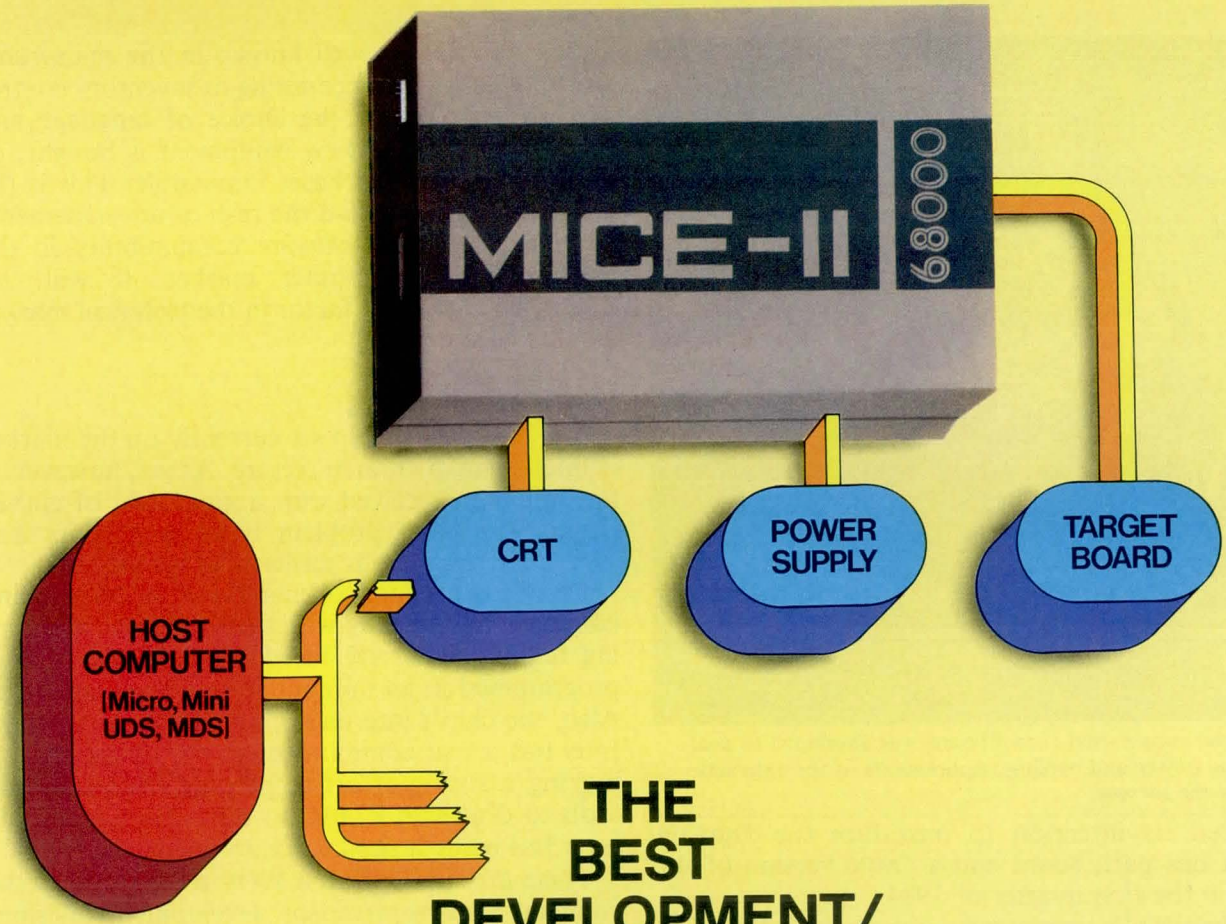
National Semiconductor was actually the first to produce a 16-bit microprocessor, the PACE, in the mid to late 70s, but it is just now coming back into the market with a second product, the 16000 family. The basic outline of the family more closely resembles Motorola's scheme than Intel's. This scheme includes a basic 16-bit bus part, which has a 32-bit internal architecture. It also includes variants with larger (32-bit) and smaller (8-bit) buses.

Because of its extremely orthogonal instruction set, the 16000 architecture has been the focus of a lot of interest and excitement in the theoretical and academic communities. It remains to be seen, however, whether or not the superior performance claimed for the family can overcome the product's late start.

Significant quantities of the 16032 basic CPU and its support chips are only now beginning to appear, but high volume production has not yet started. The 8-bit bus variant (16008) has been introduced in sample quantities, and as of midyear, National had



Motorola's 68451 MMU provides memory management services to 68000 bus-master devices. It supports paging, segmentation, write protection, and the separation of data and program spaces in memory.



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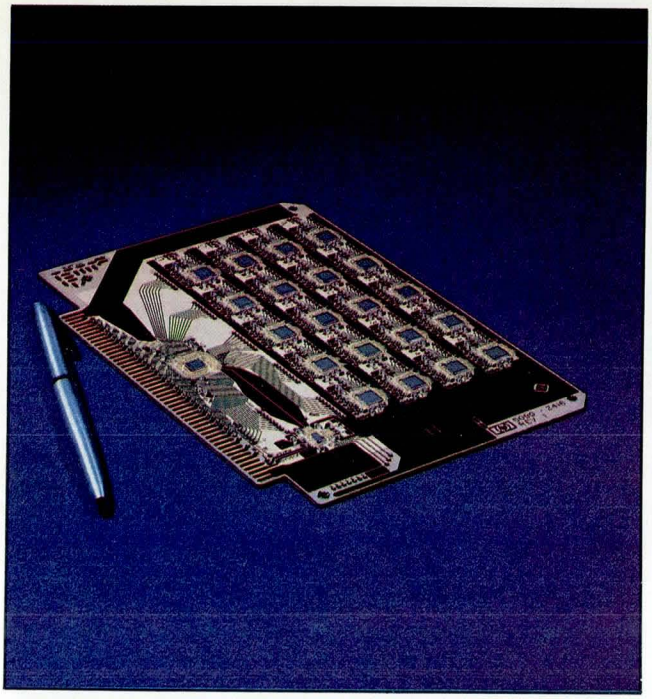


A special copper-clad circuit board was developed to deal with the power and cooling requirements of the chip sets used in the HP 9000.

revealed its intention to introduce the 32032, a 32-bit bus part, soon, and a CMOS version of the 16032 in the first quarter of 1984.

In National's terminology, coprocessors are called slave processors. Two are currently defined—the FPU (16081) and the MMU (16082). Custom slaves are mentioned in the company's promotional literature, but it remains to be seen whether any designer or manager will find it profitable to develop such parts.

Zilog is also producing coprocessors, called Extended Processor Architecture products, for the Z8000. These devices are designed to work with the company's Z-Bus. They include three types of MMUs, a DMA, serial and asynchronous controllers, various timers and buffer units, a burst error processor, and a data ciphering processor that uses the data encryption standard algorithm to encrypt data. An IEEE standard FPU is also in the works, but is currently being emulated by a software package.

One of the encouraging trends in the 16-bit world, which seems to be carrying through to most 32-bit devices, is upward compatibility. This enables object code written for a less capable chip to run on one with advanced functions. As both standalone and embedded microcomputer systems become more complex, thus adding more functions and peripherals, the price of the software written to drive these systems will become the major cost factor. To upgrade the system (provide increased speed or functions), one of the chief criteria in choosing the hardware will be whether this software needs to be rewritten for a new CPU.

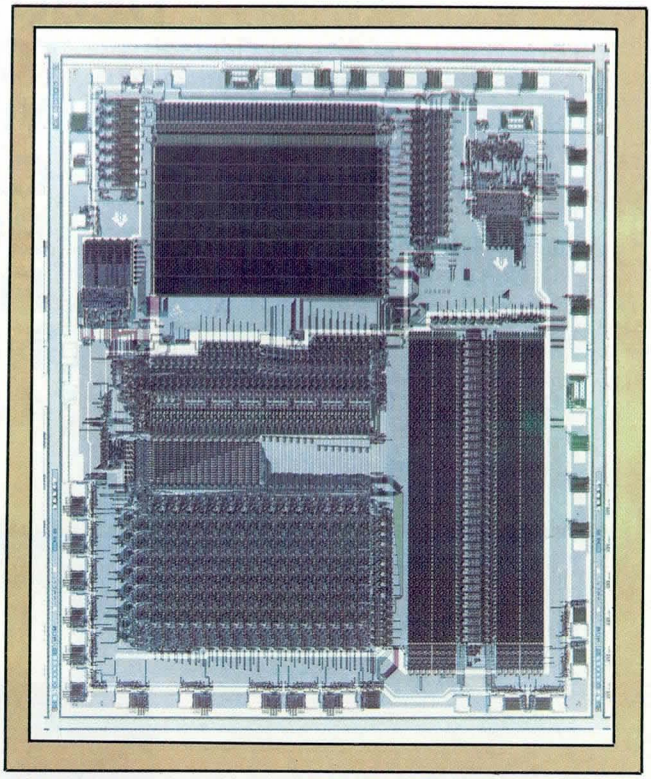
This problem is well known in the mainframe world, where large accounting or inventory control systems may dictate the choice of language and manufacturer when new equipment is bought, or even make such purchases impossible. This is the technical reason behind the rash of advertisements for hardware and software compatibility in the consumer microcomputer market. It will, no doubt, be a growing factor in the technical market as time goes on.

On the horizon

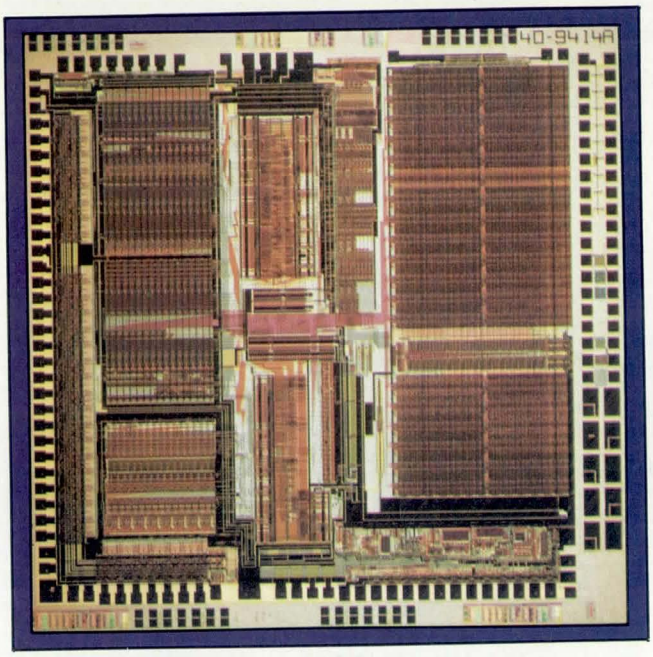
The only 32-bit chip set currently on the market is Intel's 3-chip 432 architecture. As yet, however, it has not been received with a great deal of enthusiasm. The chief problem is its complexity and sheer difference from earlier microprocessors.

Designers used to working in 8080 or Z80 machine language, and dealing with their interface and timing requirements, are faced with a device that is programmed in an unfamiliar high level language. Also, the chip's internals are difficult to visualize. Intel has a real commitment to the device, and is making a strong effort to provide education and tools to deal with it, but no other large manufacturer has made a similar commitment.

There are rumors that a 386 is in the works in the company's microprocessor development division. This would be an encouraging sign—an extension



TI's 32-bit TMS320 is optimized as a signal processor and implements a Harvard architecture with separate data and program memory. It is not clear if it is intended as a competitor in the general purpose CPU race.



Hewlett-Packard's 32-bit CPU chip for the HP 9000 is fabricated using the company's proprietary NMOS-III process. It has a minimum feature size of 1.5 μm, and a spacing of 1 μm. Other chips in the set handle memory management, timing, and instruction cache functions.

of familiar architecture to include new capabilities. Such a nonthreatening approach is exactly the direction that the other manufacturers have taken with their future products. Motorola's 68020, Zilog's Z80,000, and National's 32032 and 32132 (on-chip memory management) are billed as being object-code compatible with the earlier 16-bit parts. The concept of "graceful upgrading" is working with the 8088—it provides a natural upward path from the 8080 and 8085 without too many startling changes.

TI's TMS320 is also a 32-bit device that is being sampled, but it is unclear whether the device is aimed at the microcomputer or signal-processing markets. Like many of TI's products, it is fast and ingenious. However, average designers may find this product difficult to work with due to its Harvard architecture (featuring separate data and program address spaces). It will likely find steady use (like the company's 9900 series) in embedded instrumentation and military applications.

Hewlett-Packard and Bell Labs (Murray Hill, NJ) offer working 32-bit parts. However, they are not currently offering their parts to the general public. In the latter case, this may change in January with AT&T's (New York, NY) divestiture of the Bell operating companies.

Hewlett-Packard's 5-chip set, integrated into its HP 9000 computer systems, consists of a CPU, an input/output (I/O) processor, 128K of RAM, a memory controller, and a clock generator. It has a 32-bit address bus, with pipelined data transfers at 36M bytes/s, a 55-ns cycle time, and a reported performance of 1 million instructions per second (MIPS). With 230 instructions, including floating point, multiprocessing and master/slave, it is definitely one of the more complicated and sophisticated devices. Hewlett-Packard is reluctant to discuss the architecture any further, pointing out that it is only being used in the company's products. At present, the company has no plans to offer it as a commercial product.

Future speculation

Western Electric (New York, NY) is the biggest unknown in the microprocessor industry. When it emerges as a subsidiary of an unregulated AT&T in January of 1984, it will certainly have the potential to become a major competitor. Bell is known to have a suite of excellent devices (the Bellmac series), and an R&D arm (Bell Labs) that the Japanese refer to as the premier American "national treasure."

There has been a good deal of speculation, however, about whether the company will be able to make an effective transition from a captive subsidiary of an enormous and highly structured utility to an aggressive competitor in a cutthroat commercial market. The consensus is that there will be a transition period lasting two or more years, while it adjusts to the sales, service, and support levels necessary for success in the noncaptive market.

Judging by the technical presentations at professional seminars like the International Solid State Circuits Conference (ISSCC), IBM could also become a major microprocessor supplier. To date, however, there are only rumors that such parts may be under development at their East Fishkill, NY facility. The company's microprocessor-based products have already employed chips from outside suppliers. This reflects sound engineering judgment about cost effectiveness in the absence of in-house parts.

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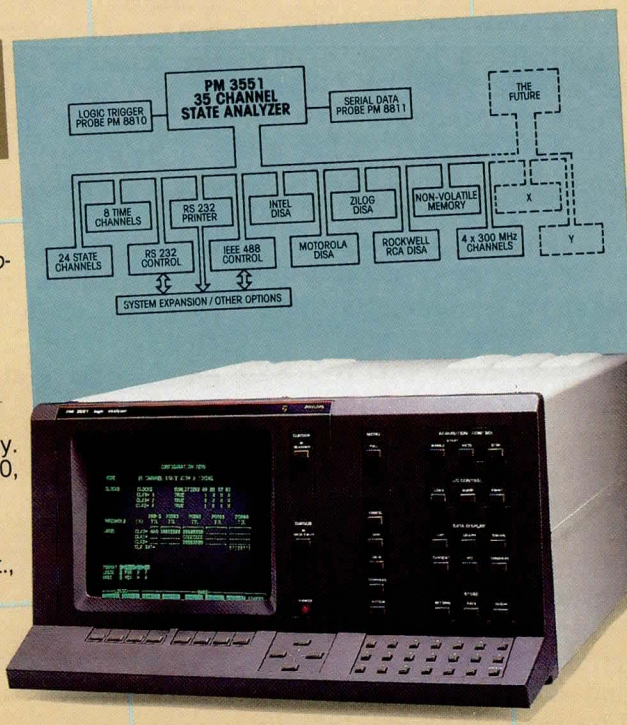

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ADVANCED FEATURES SQUEEZE ONTO PROCESSOR CHIP

VLSI brings minicomputer performance and memory management to 16-bit microprocessors.

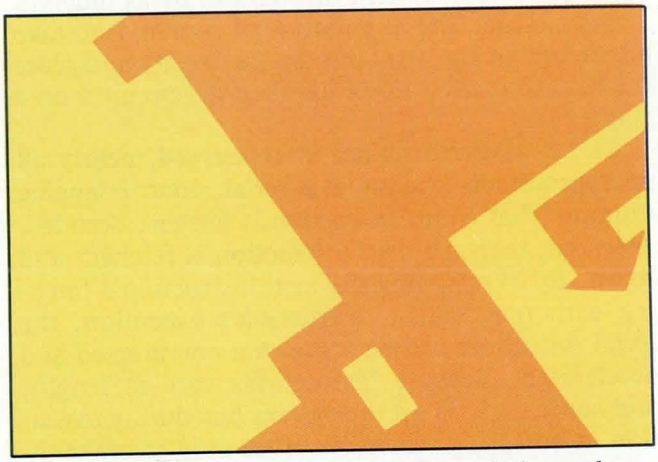
by Jim Slager

Systems are often designed for multitasking and multi-user applications. As such, they require a means to protect software files from inadvertent access by other users. In addition, these systems must accommodate larger programs and provide comparable performance to 16-bit single-user systems.

The iAPX 286 microprocessor responds to the needs of designers working on such systems. Its fundamental design objectives are to preserve software compatibility with the iAPX 86 (8086 and 8088); provide both a large, directly addressable memory capacity, and an even larger virtual memory management capability; and offer a built-in facility for protecting system and user memory. Another major design goal of the 286 is to supply performance (in either a protected or unprotected mode) higher than any other existing 16-bit microprocessor.

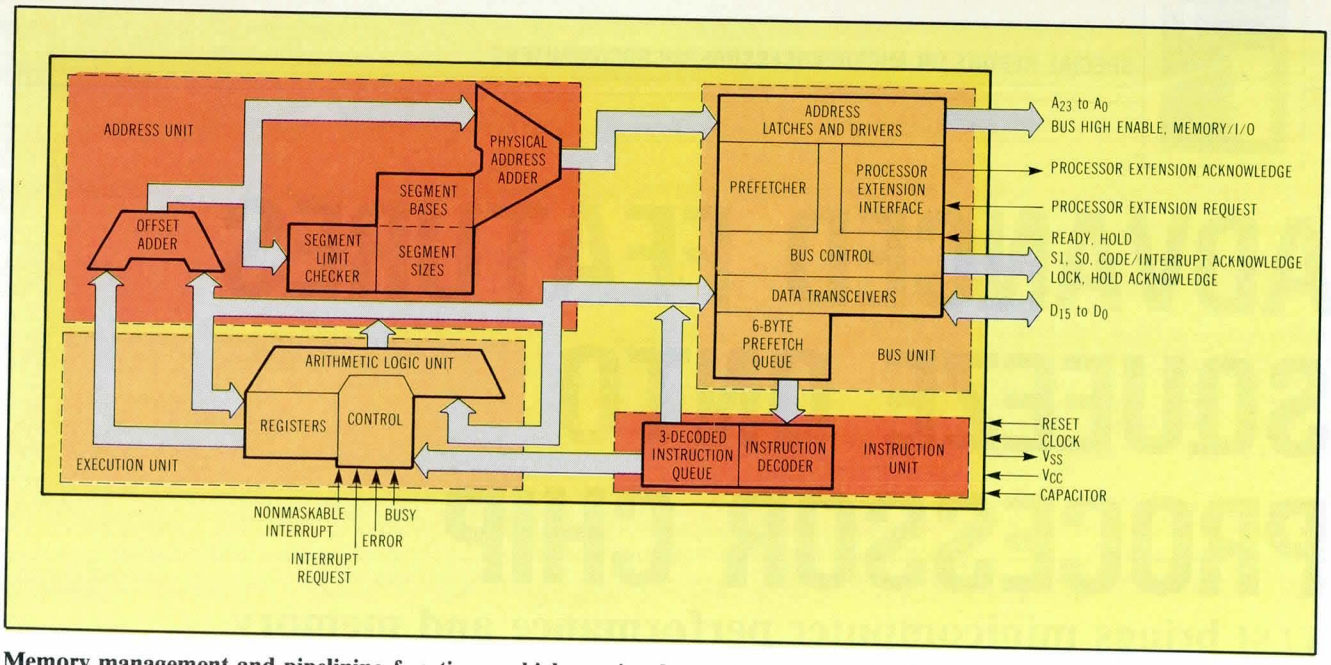
Design considerations

The most immediate way to achieve higher performance is to increase the microprocessor's clock frequency. All else being equal, a 20% increase in clock rate would increase chip performance 20%. It is not that simple, however. By increasing the frequency, execution times are scaled, and to achieve the increase in performance, memory access times must shrink. Either the designer must select higher speed (and more costly) memory devices, or the increased performance must be degraded by adding wait states to the bus cycle. This allows the slower memory to complete its cycle.



With regard to memory management and protection, the designer can implement these functions on a separate chip that works in conjunction with the microprocessor. This would, of course, simplify the central processing unit (CPU) chip designer's task. However, a serious trade-off results from adopting this approach. By placing the memory management and protection functions on a different chip, the time required for data and signals to travel from the CPU to the memory management unit (MMU), and then flow through the MMU, must be subtracted from the already tight memory

Jim Slager is a principal engineer at Intel Corp, 2625 Walsh Ave, Santa Clara, CA 95051. He is responsible for logic design of microprocessor chips. Mr Slager holds a BS in electrical engineering from the University of Illinois.



Memory management and pipelining functions, which previously separated chips or whole circuit boards, are brought onchip in the 286. Thus, multi-user and multiprocessing applications are possible, while maintaining code compatibility with the 8088 and 8086 processors.

system time. Thus, dividing the design tasks in two degrades overall system throughput by as much as 30% or more. The alternative, of course, is to take advantage of the available device density and place the MMU circuitry alongside the CPU circuitry on a single die.

As far as performance is concerned, nearly all microprocessors operate in a serial, nonoverlapping fashion. That is, an instruction is fetched, decoded, executed, then the next instruction is fetched, and so on. By overlapping the next instruction's fetching with the current instruction's execution, the serial procedure can be somewhat compressed and accelerated. Because instructions vary in length, and some may tie up the system bus during execution, a buffering scheme is often used to make instruction prefetch statistically more effective. It is often possible to hide nearly 100% of the instruction prefetch activity by performing it when the CPU is busy with internal operations and does not require the bus.

Overlapping instruction decode with instruction execution achieves an even higher throughput. This is an especially useful technique for instruction sets designed for high code density. Normally, such instruction sets vary greatly in instruction formats and lengths. Additional problems for the microprocessor designer offset code-compaction benefits for the user. Longer instruction decode times usually accompany these benefits as well.

Decoding prefetched instructions also hides instruction decode time. In effect, instead of passing raw code from the prefetch queue to the processor's execution unit, a pre-decode takes place in the instruction preparation pipeline. Very fast execution is possible since the designer can tailor the predecode format, which is internal to the CPU.

An extensive instruction frequency analysis performed on 14 different programs written in assembly language, PL/M, and Pascal (for a combined total of nearly 31M instructions) showed that over 60% of instructions require memory access. High performance computers often use complex addressing modes as one way to obtain high throughput, while memory management and protection further complicate the address generation process. However, large numbers of onchip transistors can prove useful in implementing fast address generation.

If instruction fetch and decode are overlapped with instruction execution, and the latter has been accelerated with very fast address generation, the processor can outstrip the system bus's ability to deliver code and data. In this case, bus saturation occurs, acting like a bottleneck and preventing the processor from attaining its potential throughput.

Partitioning for throughput

With these considerations in mind, the 286 is partitioned into four separately operating units (see the Figure). These units process instructions in a pipelined manner to achieve very high throughput.

The bus unit is capable of performing bus cycles autonomously. It contains a prefetcher and a 6-byte code queue that enable it to fetch and buffer (store) code until needed. The prefetcher contains a limit checker that prevents this prefetcher from accessing code in protected memory locations.

Because the bus cycle is pipelined, a new address is sent out on the address pins, while data from the previous address are taken in on the data pins. In

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CIRCLE 94

TABLE 1

Execution Time Comparison

Instruction	286 Cycles	8086 Cycles	Factor
MOV CX, CONSTANT	2	4	2
MOV AR RAY [DI], CONSTANT	3	19	6.3
ADD [BX] [DI], AX	7	24	3.4
JC CARRY_SET	9	16	1.8
REP MOVS SCREEN, BUFFER	4/word	17/word	4.3
MUL CX	21	125	6

this way, high throughput can be supported without requiring excessively fast memory access times. This bus can provide an 8M-byte/s transfer rate while allowing 242.5 ns of address-to-data delay at the chip pins for each bus cycle. Thus, the microprocessor can access the bus at a rate of one bus cycle for every two clock cycles, and each bus cycle has three clock cycles for completion.

In addition, the bus unit contains a processor extension data channel that can perform operand transfers between a coprocessor extension and memory in accordance with the processor's memory protection rules. This data channel supports the iAPX 287 numeric coprocessor, which performs high speed, floating point math processing.

The instruction unit prepares and buffers instructions before they are executed. It accesses code bytes from the bus unit's code queue and interprets them. Fully decoded instructions are buffered in a 3-word instruction queue. Each entry in this queue consists of 69 bits and includes all the information the processor needs to execute the instruction, except for memory-resident operands.

In essence, the execution unit carries out the instructions. It receives fully decoded instructions from the instruction queue (located in the instruction unit) and executes them very quickly. It also contains a 1536-word x 35-bit control read only memory (ROM) and a 22-word x 16-bit register file. Fast hardware allows arithmetic or logical operations to be performed on two register operands, with the result returned to the register file in 250 ns.

Fast address calculations are the address unit's domain. This unit can add two 16-bit numbers to form an effective address in one 62.5-ns clock phase, and simultaneously perform a limit check and a segment base translation in a second clock phase of the same duration. This fast address calculation is handled by a 16-bit effective address adder, a 16-bit limit checker/subtractor, a 24-bit physical address adder, and an 8-word x 48-bit segment descriptor cache.

Because these four units can operate independently, up to four different instructions can be in various processing stages at the same time. For example, the bus unit can be prefetching instruction A, the instruction unit decoding instruction B, the execution unit executing instruction C, while the address unit is calculating an address for instruction D. Buffering between the units ensures efficient operation and lets the units work in concert despite different throughput rates. This reflects the design objective to keep the execution unit constantly busy executing instructions.

Improving bus bandwidth

The design goal for the 286 is an execution rate of 1.5 million instructions per second (MIPS). Based on the aforementioned instruction frequency analysis, the average instruction is 2.39 bytes long and performs 0.63 data reads and writes. Therefore, (2.39/2) + 0.63 = 1.83 bus cycles required/average instruction. Bus cycles (with zero wait states) take two clock cycles. An 8-MHz 286, therefore, has sufficient bus bandwidth to support up to 2.2 MIPS [8 MHz/(1.83 x 2) = 2.2].

With a maximum bus bandwidth capacity of 2.2 MIPS, the instruction unit must be able to prepare instructions at least that quickly, in order to take full advantage of the bus's speed. Operating at 1 byte/clock cycle, the instruction can prepare average (2.39-byte) instructions at a maximum rate of 3.35 MIPS, giving a comfortable margin.

For the execution unit to work constantly, it must not be forced to wait because of read-cycle bus collisions with the prefetcher. Therefore, a special provision allows the execution unit to give the bus unit an early warning that a data cycle will be required on the next clock cycle. In that event, the bus unit will not permit a prefetch to begin, thus eliminating the possibility that the execution unit will have to wait on the prefetcher.

In a highly pipelined machine, the possibility exists that frequent control transfers, coupled with the time needed to fill the pipeline after such a transfer, will statistically defeat any throughput advantage that pipelining achieves. This would be the case if control transfers took place very frequently.

The 286 protects users from one another, and also protects the system software from its users.

However, analysis of 8086 code indicates that instructions perform a control transfer only about one out of seven times, or about 15% of the time. Thus, pipelining does provide a performance benefit if the fill delay on control transfers is kept short. Consequently, the 286 is designed with particular attention to keeping the fill delay short. When the bus unit code queue is empty, as it would be after each control transfer, new code bytes pass

right through the bus unit without suffering clock phase delay. Similarly, instructions the instruction unit prepares pass right through an empty instruction queue to the execution unit.

The entire pipeline is designed so that only two clock cycles are required in the minimum case. These begin when the first code byte signals are valid at the chip's input pins and continue until the entry point address for that instruction is taken into the execution unit's control ROM. Any computer architecture that executes an instruction set with a variable format, such as the 286, would probably require one clock cycle just to receive an instruction and generate a control ROM address. In the case of the 286, the fill penalty following a control transfer is one clock cycle, and it occurs an average of once every seven instructions. This creates a 2.5% fill penalty for which the pipelined architecture's added performance more than compensates.

Comparing the 286 with the 8086 shows a performance improvement of 1.8 to 6.3 times (Table 1). When weighting instruction execution times by their dynamic frequencies, the 286's performance is 1.88 MIPS. Though the 286 is designed to provide high throughput without dependence on high cost and high speed memory, there may still be situations in which wait states are required. The effect of these wait states (Table 2) is such that even when three are required, the 286's throughput will still exceed 1 MIPS.

TABLE 2

Effect of Wait States on iAPX 286 Performance

Number of wait states	Address to data delay (ns)	Normalized execution time	Throughput (MIPS)
0	242.5	1.0	1.88
1	367.5	1.24	1.52
2	492.5	1.51	1.25
3	617.5	1.83	1.03

Functional requirements

Whereas the 286 meets and exceeds its performance expectations, it is fair to ask whether it also provides the functional support intended by its designers. Does it protect system and user software and provide onchip memory management?

In fact, the 286 does protect users from one another, and also protects the system software from its users. Each user has up to 1G byte of virtual address space, which can be split between shared and private use. In shared space, common data, files, and library routines might all be stored. Private space, on the other hand, is accessible only to its user. Therefore, files kept in private space are protected from access by other users.

The 286 hardware supports a 4-level protection hierarchy. Should a task attempt to access an address without having access rights, the CPU will prevent it from doing so and issue a signal that a fault has taken place. Compared with 2-level protection systems used in some minicomputers and microprocessors, this architecture offers broader and more efficient protection.

Levels are arranged from highest to lowest priority. For example, a kernel level would be reserved for the most important and vulnerable system software routines. Following that, a supervisor or system service level might have next priority, then application service, and finally, applications.

The kernel might be software that governs memory space management, task scheduling, and intertask communications. A supervisor might handle input/output (I/O) resource management, memory policies, and overall job scheduling. Application services could include file control, job control, language processing, and application support utilities, such as a cathode ray tube editor. The lowest privilege level would be the application level. Confined to this level, software with erroneous routines can be prevented from crashing the system.

With regard to software compatibility, the 286 is designed to operate in two modes—real and protected. In the real mode, machine code written for the 8088 or 8086 can run without modification on a 286. The advantage is an immediate improvement in performance without the expanded memory management and protection functions.

In the protected mode, the values used in segment registers differ from those used in real mode. Thus, to move 8086 code into the protected mode, the code must be reassembled or recompiled. Ultimately, however, still higher performance, coupled with the hardware-based memory management and protection features, more than compensates for the time spent in making the conversion.

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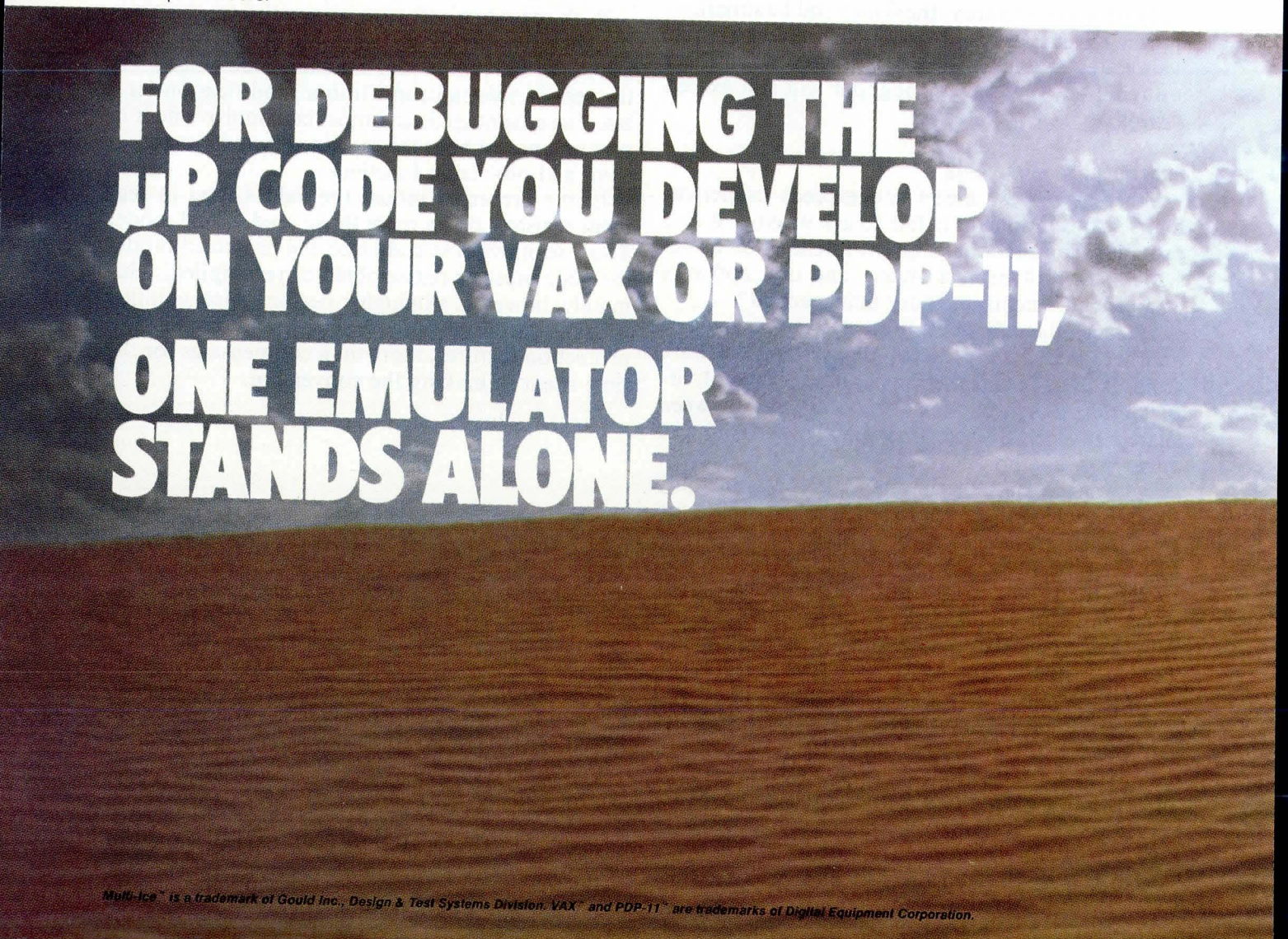

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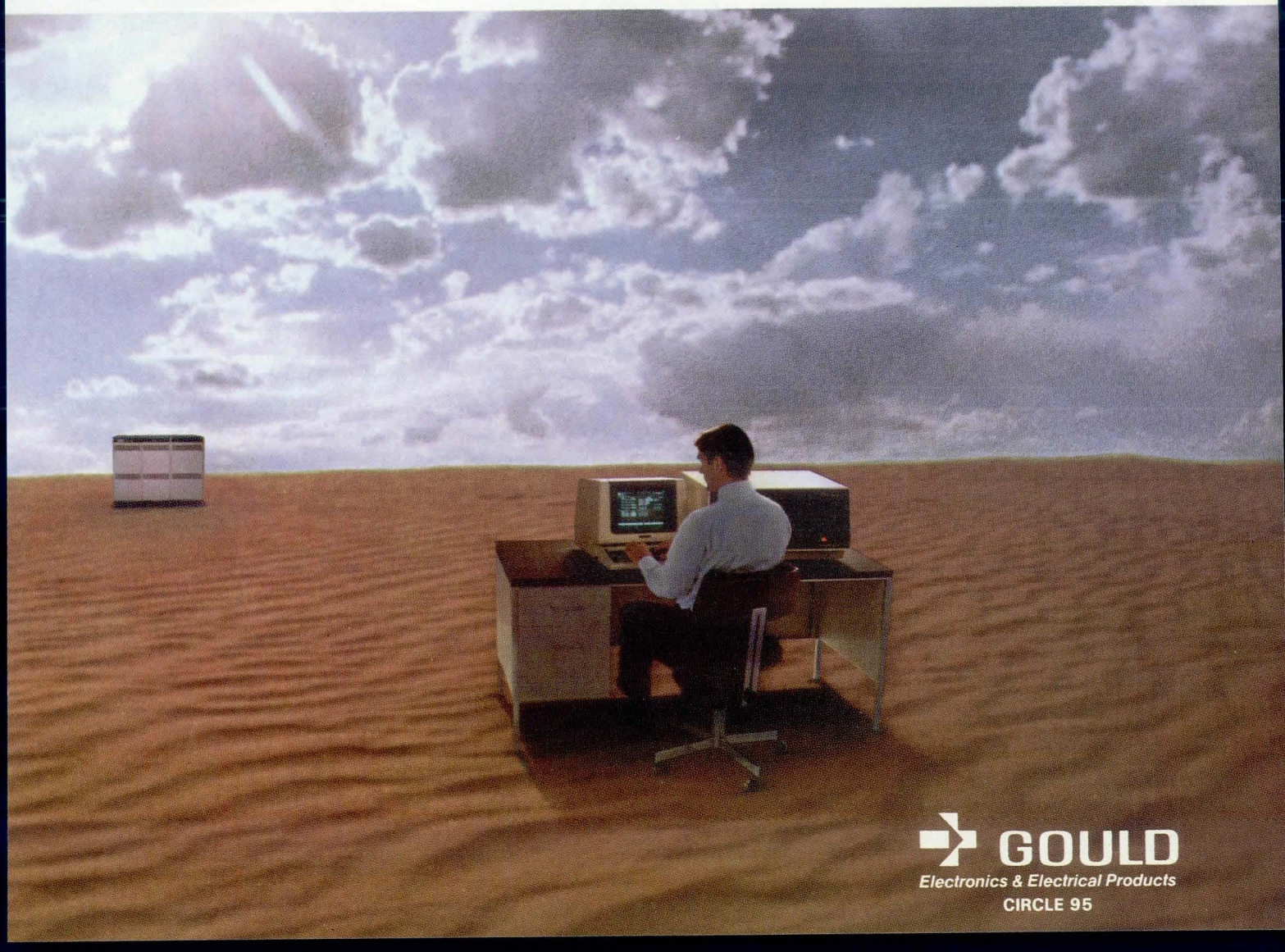

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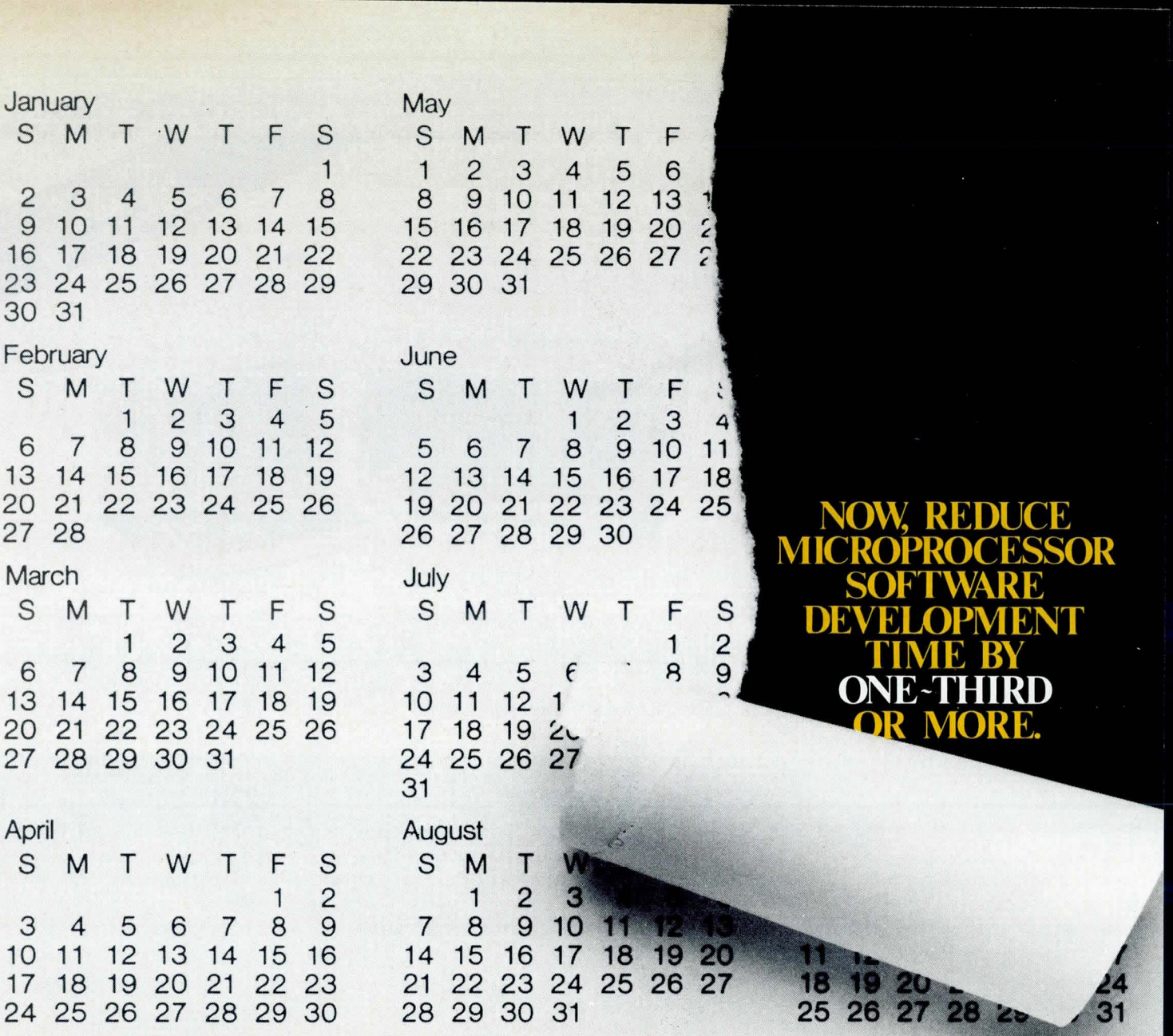

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CIRCLE 106

COPROCESSORS SPEED FLOATING POINT CALCULATIONS

Operating in a master/slave relationship with an NS16032 processor, this dedicated floating point chip executes high speed numeric computations as ordered.

by Moshe Gavrielov,
Asher Kaminker, and
Yom-Tov Sidi

Attempting to pack greater functions onto single-chip microprocessors, manufacturers eventually run out of silicon real estate. One way to enhance a microprocessor's computational power without enlarging the basic chip is through the concept of coprocessing—building a dedicated slave chip that takes orders directly from the processor's central processing unit.

This is the principle behind National Semiconductor's NS16081 Floating Point Unit (FPU), a dedicated arithmetic processor that performs floating point computations for the NS16032 high performance 32-bit microprocessor.

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Asher Kaminker is an engineering manager at National Semiconductor. He holds a BSEE and an MSEE from the Technion Institute of Technology.

Yom-Tov Sidi is a microprocessor design engineer at National Semiconductor. He holds a BSEE from the Negev University, Beer Sheva, Israel.

Slave processing—master commands, slave obeys

The master/slave relationship between the NS16032 central processing unit (CPU) and the NS16081 FPU is one technological solution to the problem of conserving silicon area while upgrading microprocessor capabilities. As semiconductor technology improves, processor support chips, such as floating point and memory management units, will be incorporated onto the same chip with the CPU. For now, however, the next best approach is the hardware extension chip as exemplified by the master/slave technique.

With this approach, the CPU and FPU operate together in a manner transparent to the user's software. Responsibility for executing all nonslave instructions resides in the 16032's CPU. When it detects a slave instruction, such as for the FPU, the CPU invokes a special protocol to inform the slave of its selection. Instruction opcodes and operands are then transferred to the slave. In the case of the FPU, it performs the required computations and informs the CPU upon completion. The CPU proceeds to strobe the slave to obtain its status and arithmetic results. The status word updates the CPU's

TABLE 1

NS16032 Floating Point Instructions

Instruction	Description
MOVf	Move a floating point value
MOVDF	Move and convert from double precision to single precision
MOVFL	Move and convert from single precision to double precision
MOVif	Convert integer to floating point
ROUNDfi	Convert floating to integer. Round to nearest, if rounding is necessary
TRUNCfi	Convert floating to integer. Round to zero, if rounding is necessary
FLOORfi	Convert floating to integer. Round to minus infinity, if rounding is necessary
ADDf	Add
SUBf	Subtract
MULf	Multiply
DIVf	Divide
CMPf	Compare
NEGf	Negate
ABSf	Take absolute value
LFSR	Load FSR
SFSR	Store FSR

i is integer length suffix— B = Byte, W = Word, D = Double word

f is floating point length suffix— F = Single precision, L = Double precision

status register and can invoke a trap-handling routine if an abnormal situation such as an overflow occurs.

All data and instruction transfers flow across a 16-bit bus connecting the two devices. The FPU uses CPU status bits ST0 and ST1 to differentiate between various types of 200-ns transfers. The CPU's $\overline{\text{SPC}}$ line serves as the data-strobe output for slave processor transfers, and a slave uses it to acknowledge completion of an instruction.

Partitioning capabilities between the two chips allows the slave instructions to enjoy all CPU addressing modes without an investment in slave chip area. Just a very small portion of the slave's silicon is required to maintain the protocol with the CPU. The CPU contains a special configuration register that records the presence or absence of slave processors in the system.

When the CPU encounters a slave instruction for which there is no slave processor, it executes an undefined trap. This permits software emulation of the slave in applications where time is not critical. It also allows upgrading of emulated slave systems without changing the user's software. In addition to the FPU, the NS16032 can operate in a master/slave relationship with the NS16082 memory management unit and with custom (user definable) slave processors.

TABLE 2

Floating Point Operation Execution Time Comparisons

With FPU	Add/Subtract		Multiply		Divide	
Register to register	7.4	7.4	4.8	6.2	8.9	11.9
Memory to register	8.5	9.6	5.9	8.4	10.0	14.1
Register to memory	9.6	11.8	7.0	10.6	11.1	16.3
Memory to memory	11.1	14.4	8.5	13.2	12.6	18.9
With FPP	1330	1500	1300	1700	1300	1950

Floating point improves performance

An integral part of the NS16032's command set are the floating point instructions. The NS16081 is designed to support these instructions by providing high speed arithmetic execution, fast communication with the CPU, and conforming with the IEEE's Floating Point Standard.

In a typical operation, the CPU decodes the floating point opcode and proceeds with the initial execution steps. Table 1 lists the CPU's floating point repertoire. A typical floating point instruction has two operands that are accessible by all of the CPU's operating modes. This provides architectural symmetry, but requires the CPU to perform effective-address calculations.

If there is an FPU in the system, the CPU's configuration register should be set appropriately (CFG F bit = 1). If the system has no FPU, a trap is generated that invokes a software-emulated floating point routine. The CPU fetches floating point operands and opcodes, and tranfers them to the FPU via a slave communication protocol. The FPU executes the instructions and returns the status of the computation and the results to the CPU, where they are stored in memory.

As shown in Table 2, there is a significant execution-time difference between floating point instructions performed by an FPU hardware processor and through software emulation. In most cases, FPU execution time is about 100 times faster than the software routine. Execution times provided in Table 2 are maximum times for three of the most common routines. Times listed are in microseconds for 10-MHz clock rates. In the FPU columns, the first value is for single precision, the second for double precision. All times are for an entire instruction cycle, including CPU operand addressing, and CPU/FPU communications via the slave protocol.

The FPU supports both single (32-bit) and double (64-bit) precision operands. This conforms with draft 10.0 of the IEEE Standard for Binary Floating Point Arithmetic. Conversion instructions can

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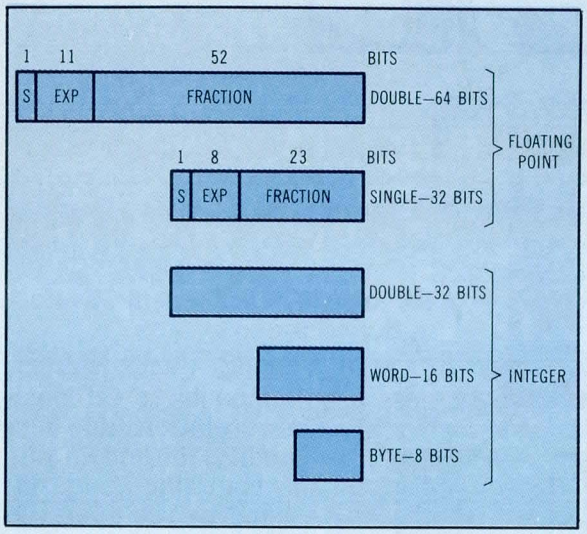
CIRCLE 97

The IEEE Floating Point Standard

IEEE Task P754 defines methods to perform floating point arithmetic by specifying number formats, operations, rounding modes, and exception handling. Floating point and integer formats handled by the NS16081 FPU are shown in the Figure. A floating point number in these formats is defined as

$(-1)^S \times 2^{E-B} \times 1.F$

where S is the sign, E is the exponent, F is the fraction, and B is the bias—127 for single precision and 1023 for double precision. Positive and negative zero are represented by an all zero exponent, and a fraction having a 0 or 1 sign bit, respectively.



According to the standard, floating point numbers must be available in at least the single-precision format. Additional formats defined but not obligatory include double, single extended, and double extended. The FPU supports the single and double formats. A software floating point package adds the double extended format. Additional numbers represent reserved operands such as infinities (plus and minus), zero (plus and minus), Not a Number (NaN), and denormalized numbers. The denormalized numbers are used to implement gradual underflow.

The standard defines the following operations: addition, subtraction, multiplication, division, comparison, square root, remainder, conversion between floating point formats, and conversion to and from decimal and integer formats. The result of each operation is required to be infinitely precise, and only then rounded according to the appropriate rounding mode.

Four rounding modes are defined: round to the nearest even, to zero, to plus infinity, and to minus infinity. These modes affect all arithmetic operations, and a user must be able to choose among them.

There are five exceptions that must be flagged when they occur: division by zero, overflow, underflow, invalid operation, and inexact result. If an exception occurs and its enable flag is activated, a trap must occur. If the flag is not activated, the standard defines the default result.

convert 8-, 16-, or 32-bit integers into any of the floating point formats and vice versa. Further details on the standard can be found in the Panel, "The IEEE Floating Point Standard."

A 3-block architecture

As shown in Fig 1, the FPU consists essentially of three major architectural blocks: the control unit is responsible for controlling the arithmetic execution flow; an execution unit uses parallel dedicated hardware to achieve fast execution of arithmetic operations; and an interface and storage unit is responsible for managing the fast master (CPU) to slave (FPU) protocol.

The control unit is responsible for internal data transfers between the execution and interface units and for the activation of all the execution unit's subblocks. Parallel activation of all the subblocks was the major design goal. This was implemented by using horizontal microcode with a separate field for each unit.

Opcode decoder controls the first block of the control unit, the entry point generator, which defines the beginning of the microcode sequence. This block feeds into a micro read only memory (ROM) store, which contains 450 (20-bit) control words, including 70 words dedicated to test routines. Each word is composed of four fields, three for control of the execution unit's major blocks and one for sequencing to the next operation. This horizontal approach is partially responsible for the FPU's extremely fast throughput.

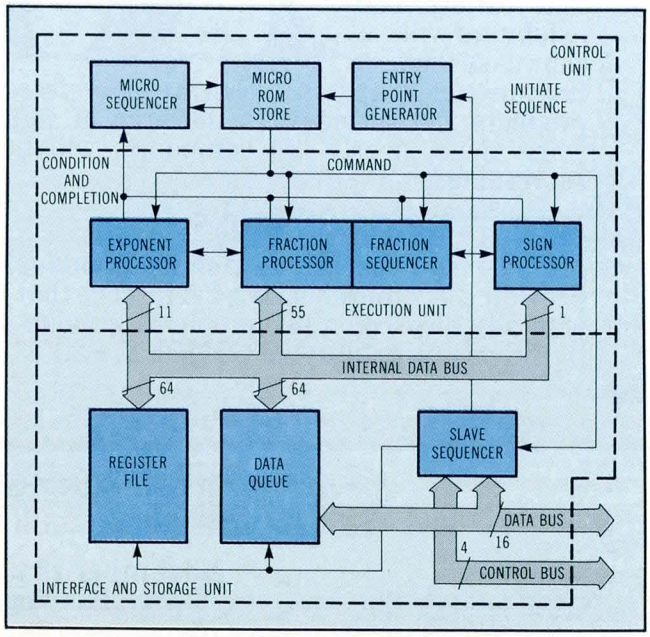


Fig 1 Control, execution, and input/output handling are the major functional breakdowns in the NS16081 FPU. Parallel execution of arithmetic computations and special hardware-implemented algorithms are key elements in the chip's high speed capabilities.

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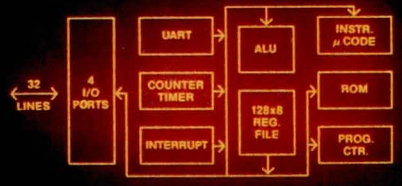

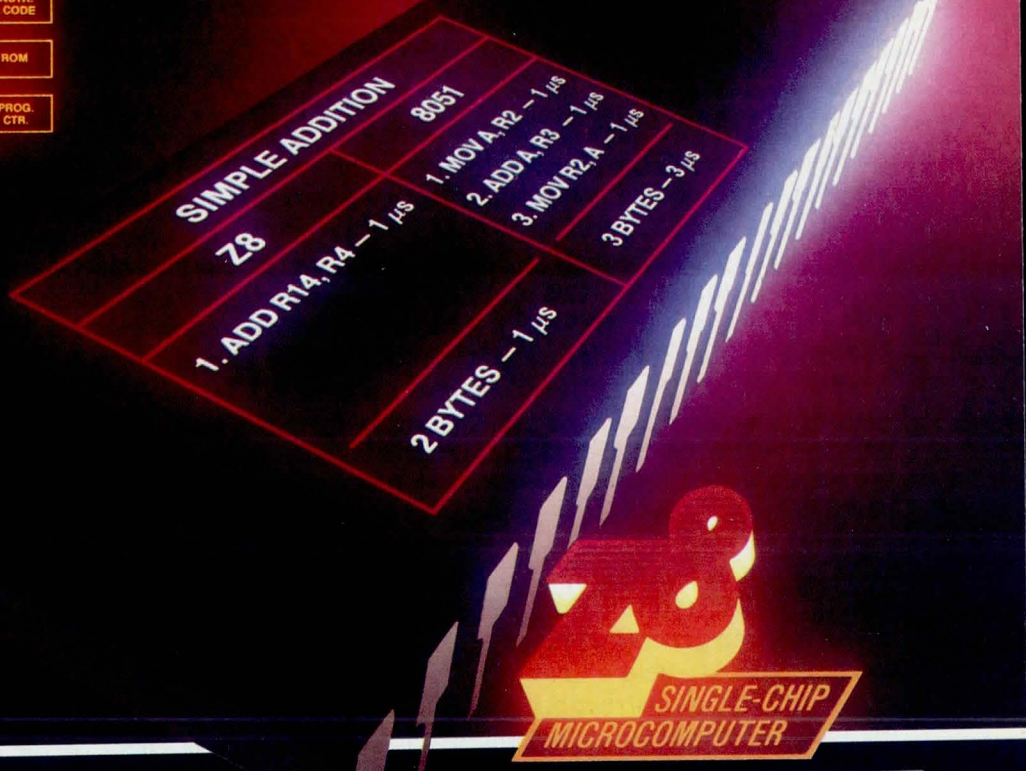

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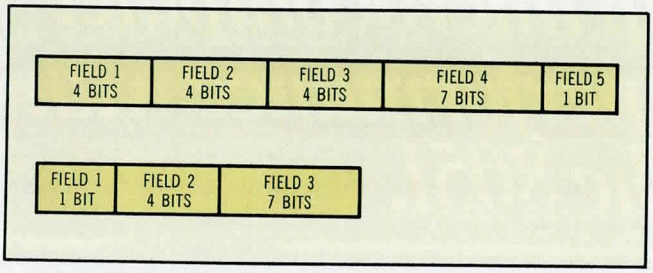

Fig 2 The arithmetic execution unit runs under the command of a dedicated microcontroller whose instruction and address fields are shown here. Each microinstruction contains a part of the address of the following microinstruction, making high speed operation possible.

The proliferation of special cases in the IEEE standard and the intricacy of implementing floating point arithmetic both profoundly affect the FPU's internal architecture. For example, in order to avoid long, time-consuming "check and branch" sequences in the microcode, a nonprogram-counter method of sequencing is used. Each microinstruction includes part of the next microinstruction's address. It also includes a condition code that, together with the status of the execution unit, defines the full address. The micro sequencer defines the next address. Fig 2 illustrates the microinstruction structure, which is divided into two parts: a micro ROM instruction and a micro ROM address.

As shown in the figure, the 20-bit microinstruction is divided into five fields. Field 1 is dedicated to the fraction processor; fields 2 and 3 are used by all other blocks; field 4 determines address field 3 of the next microinstruction; and field 5 is a wait bit used to synchronize the microcontroller with the asynchronous blocks.

Further, the 12-bit micro ROM address is partitioned into three fields. Field 1 is a prefix assigned by the slave sequencer; field 2 contains data resulting from the condition code and serving to implement conditional branching; and field 3 is determined by the instruction field of the previous microinstruction. Table 3 shows a typical line of microcode for a multiplication.

Computing arithmetic values

All numerical computations of the FPU are performed in the execution unit. It consists of three computation units—the sign, exponent, and fraction processors—and a control unit, the fraction sequencer; all four units operate in parallel.

Arithmetic operations are always initiated by the microcontroller. Fields 2, 3, and 4 control the sign and exponent processors and the fraction sequencer. On the other hand, the fraction processor is under the control of both the microcontroller and the fraction sequencer.

As the smallest part of the execution unit, the sign processor is responsible for computing the sign of the result. Aside from handling the operand signs, the exponent and fraction processors may provide additional information. For example, an addition sign depends upon the magnitudes of the addends when they have different signs. Typical sign processor operations include load operand sign, store result sign, and complement sign bit. The exponent processor's three internal registers and fast 13-bit arithmetic logic unit (ALU) compute the exponent of an arithmetic result. The ALU adds and subtracts exponents.

Data often flow between the exponent processor and fraction sequencer. For example, the exponent processor informs the fraction sequencer of any difference between the exponents of the operands during addition and subtraction. This permits alignment of the operand's fractions before addition or subtraction is performed. Similarly, the fraction sequencer notifies the exponent processor of the number of shifts performed during normalization of a result, allowing a correct exponent to be generated for the result. In addition to exponent computations, the exponent processor detects

TABLE 3

Typical Line of Microcode

MUL 12: STOR MUL ADDEX MUL 15/OPEQ0, MUL 16/NOPEQ0 WAIT

Mnemonic	Definition
MUL 12	Address of the current microinstruction
STOR	Move data from the fraction processor shifter to the fraction processor recoder
MUL	Commence multiplication
ADDEX	Add the exponents
MUL 15	Next address field if the operands equal 0
OPEQ0	Condition code detects 0 operands
MUL 16	Next address field if the operands do not equal 0
WAIT	Perform the current microinstruction only when the execution of the previous microinstruction has been terminated

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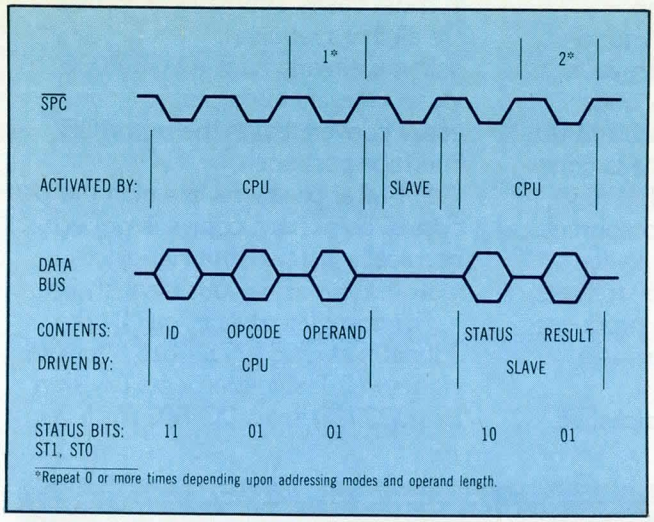

Fig 3 A slave sequencer controls transactions between the FPU and its master, the CPU. All transactions depend upon the $\overline{SPC}$ pulse, which controls information flow from the CPU to the FPU and vice versa.

prohibited operands such as zero divisors and illegal operands. It also looks for anomalous results such as under and overflows.

Fraction calculations are handled by the fraction processor and sequencer. In contrast to the sign and exponent processors, which are sequenced entirely by the microcontroller, the fraction sequencer is only initiated by the microcontroller. It proceeds to sequence through a series of transitions while the microcontroller remains idle. A finite state machine and a counter in the fraction sequencer govern transitions. At the conclusion of the transition sequence, the state machine returns to its starting state and informs the microcontroller to continue. This type of control is necessary to implement the fast algorithms used for fraction computations.

Both the microcontroller and fraction sequencer control the fraction processor. During most computations, it is necessary for both units to send simultaneous control signals to obtain correct results. The fraction processor consists of seven special purpose registers that communicate over an internal data bus. The bus transfers data between registers, and the registers shift the operands and partial results during normalization, alignment, multiplication, and division. Some of the registers input to special arithmetic units such as the recoder and carry-save adder. The recoder recodes operands, while the carry-save adder accelerates multiple additions. This concept of parallelism is vital in the execution unit. Together with the unique hardware implemented algorithms, the FPU offers high speed and exceptional arithmetic capabilities.

Besides handling communication with the CPU, the interface and storage unit buffers operands and results between the CPU and FPU, and contains all user accessible registers.

CPU/FPU transactions are under the control of a finite state machine, the slave sequencer. Sequencing between states is controlled by the $\overline{SPC}$ pulses according to the stage of the protocol (Fig 3). The first stage is to recognize the FPU slave identification. The slave sequencer then latches the FPU instruction into its instruction register. Following this, the sequencer loads operands sent one word at a time from the CPU into a 16-word x 8-bit register file, called the queue.

The queue buffers operands and results passed between the CPU and FPU, aligning them with the 64-bit internal data bus. This is not necessary in all addressing modes, since operands in some cases are in the FPU. Next, the slave sequencer informs the microcode sequencer that it can start a computation. When the computation is complete, the slave sequencer informs the CPU using the bidirectional $\overline{SPC}$ line, and strobes the result and status from the queue to the CPU.

In addition to the slave sequencer and queue, the interface and storage unit contains a register file and a 32-bit floating status register. Within the register file are eight 32-bit user accessible floating data registers that can be paired to form 64-bit double-precision registers.

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In applications where time is not critical, the FPP executes an emulation mode for the FPU. Through the slave processing concept, this allows the development of software for arithmetic purposes without the FPU. But if faster execution is required, the FPU can be integrated into the system without making any changes to the original software.

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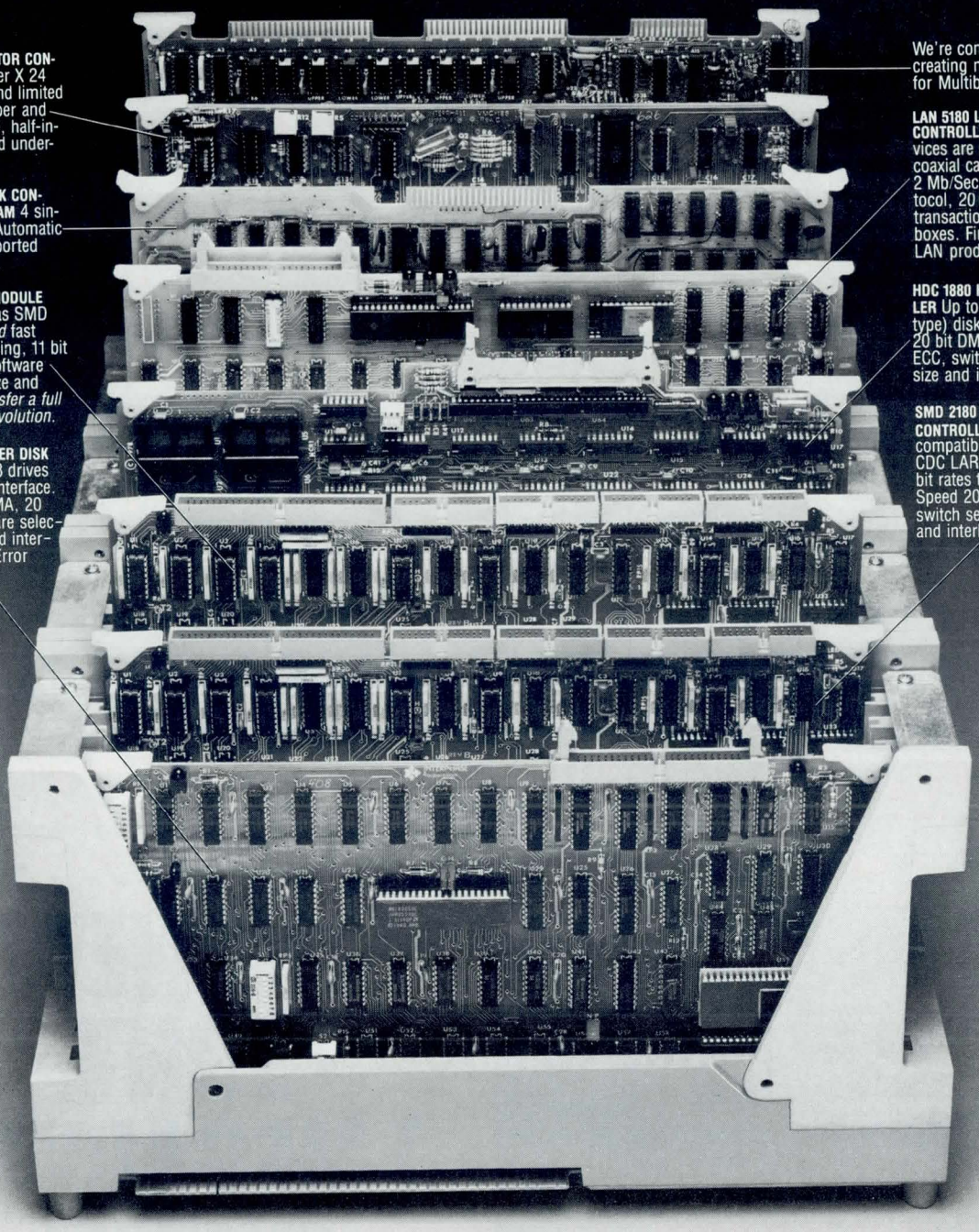

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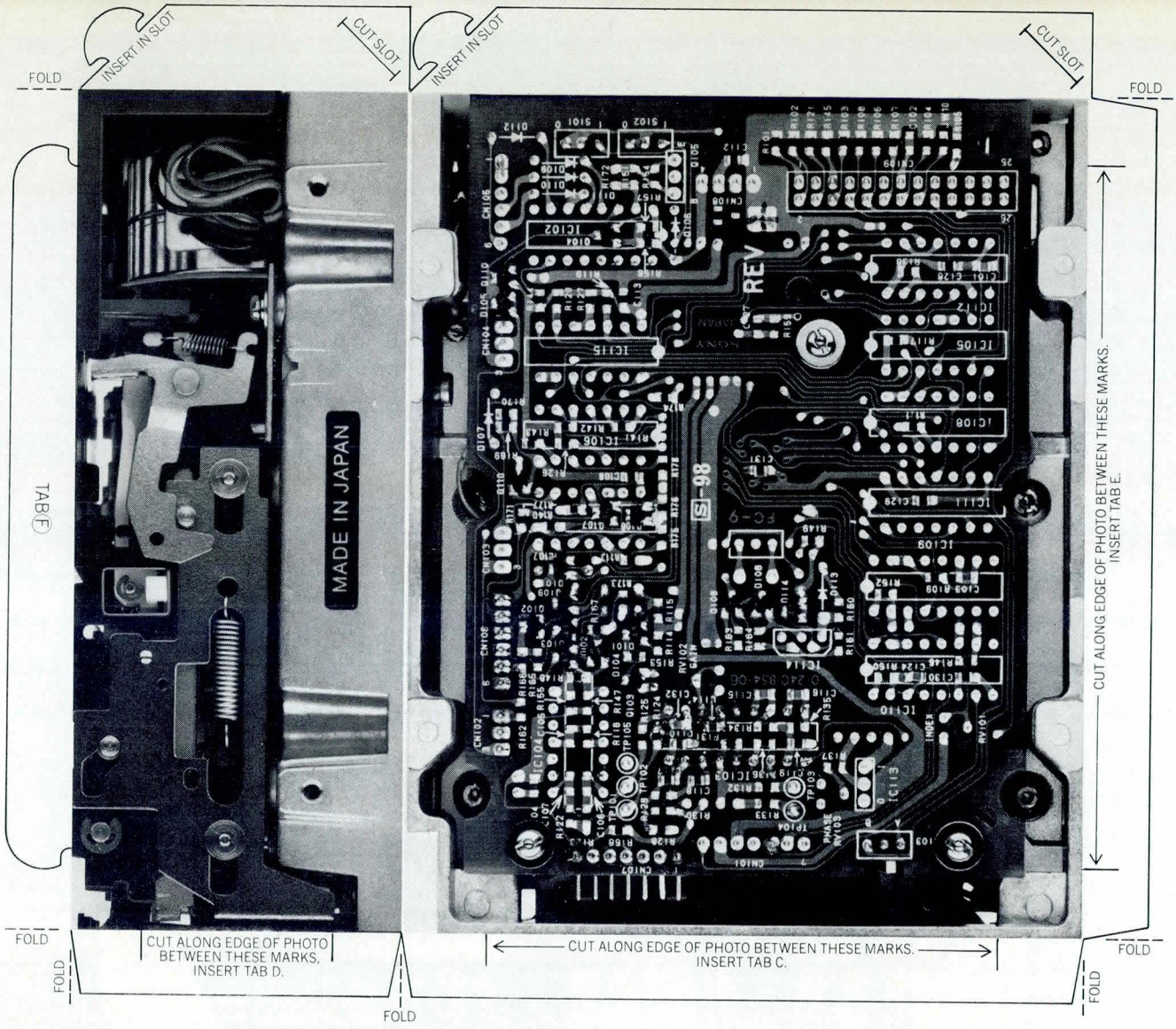

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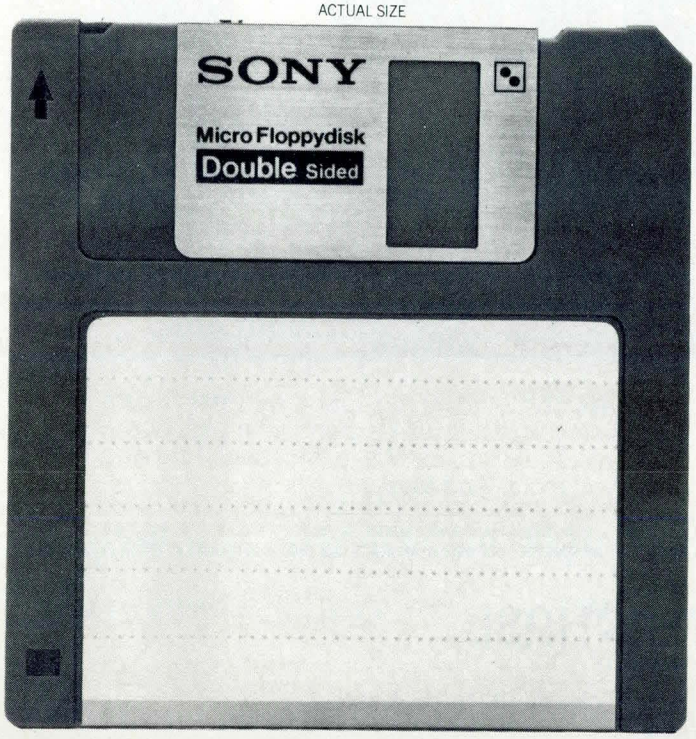

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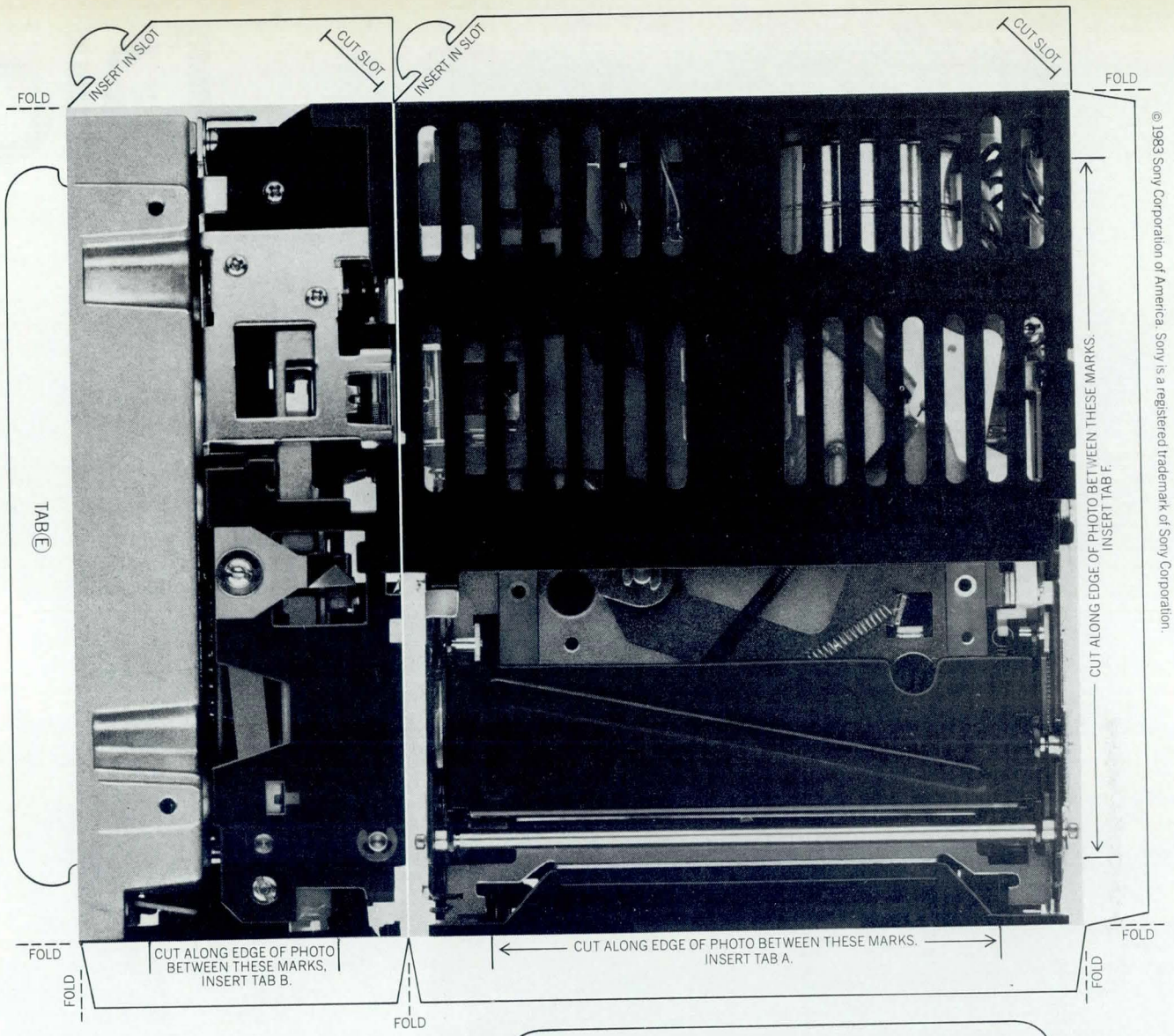

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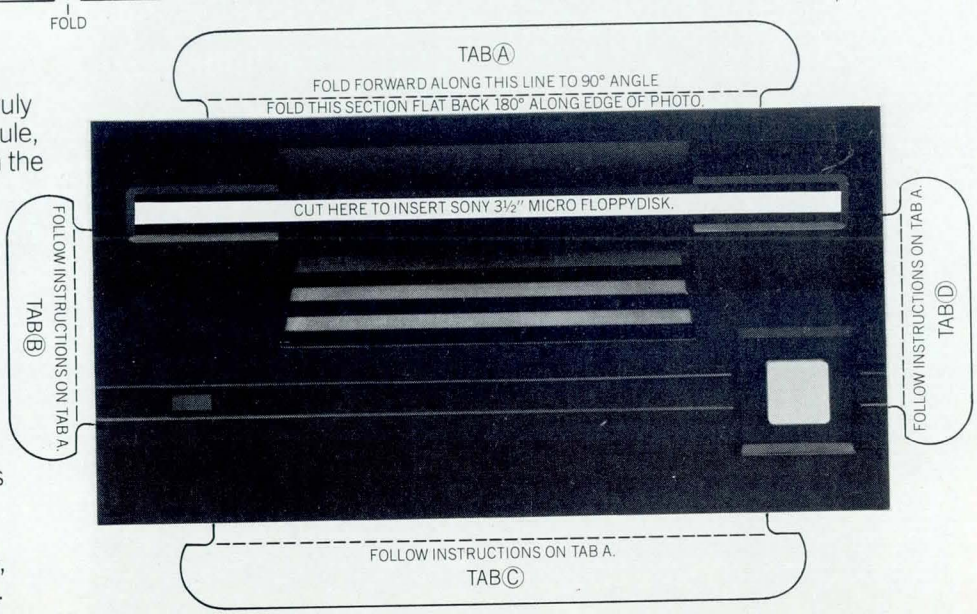

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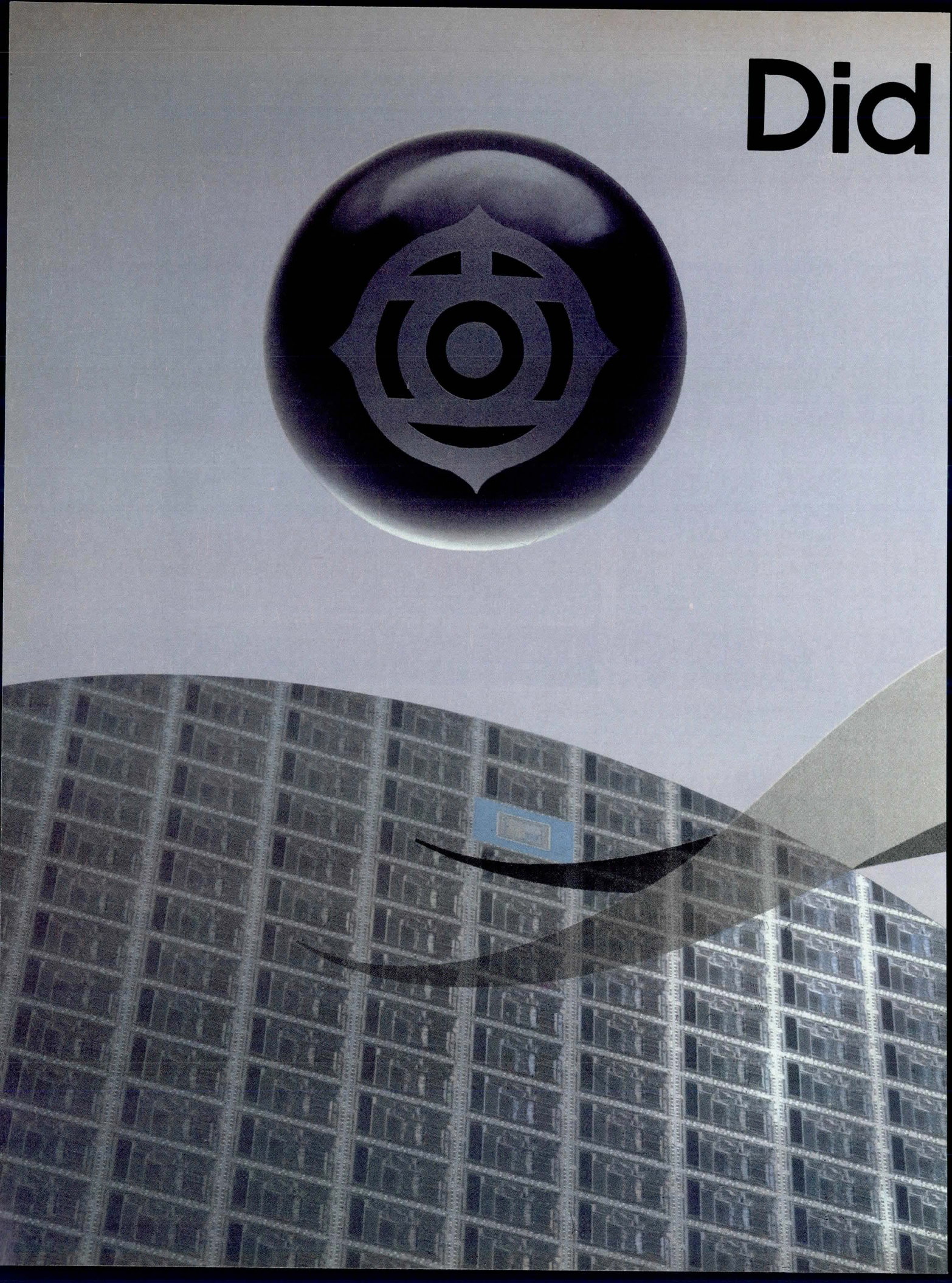
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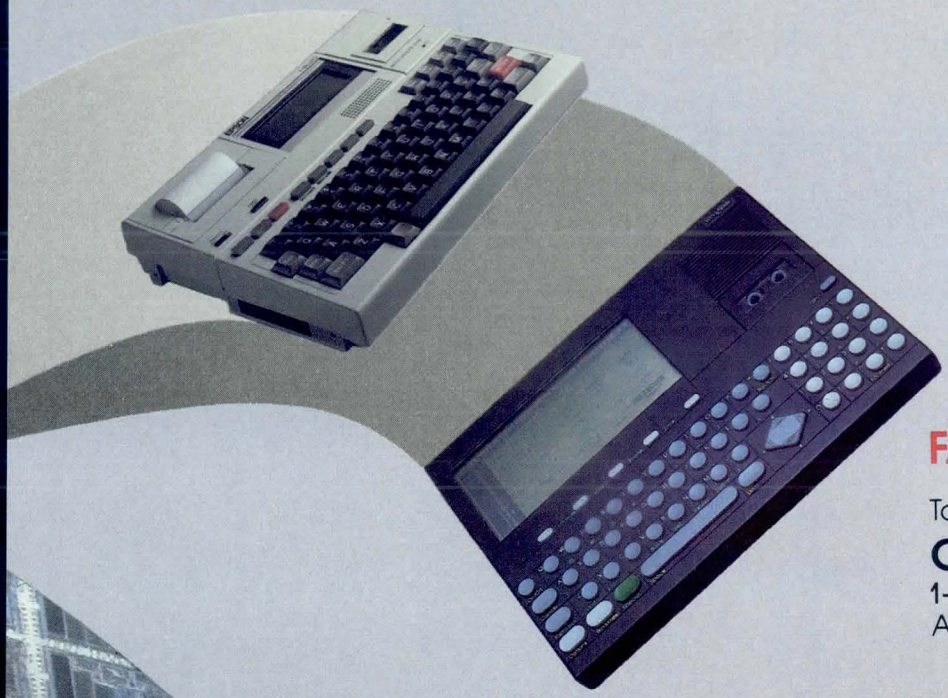

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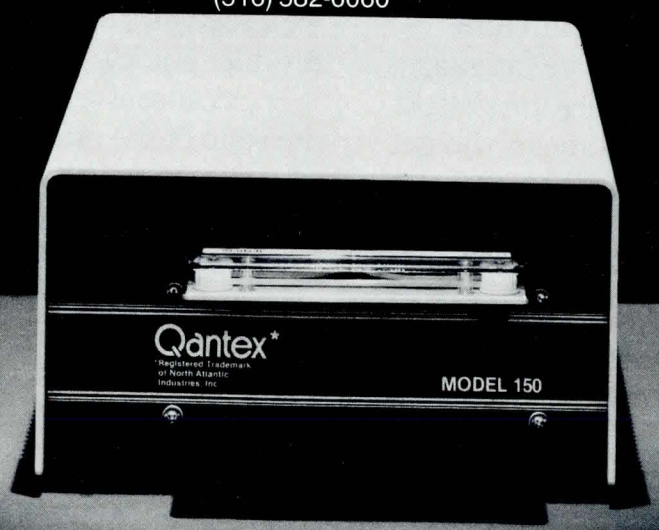


CIRCLE 104

POWERFUL 32-BIT MICRO INCLUDES MEMORY MANAGEMENT

Managing a 4G-byte address space, this 32-bit microprocessor does address translation and access protection.

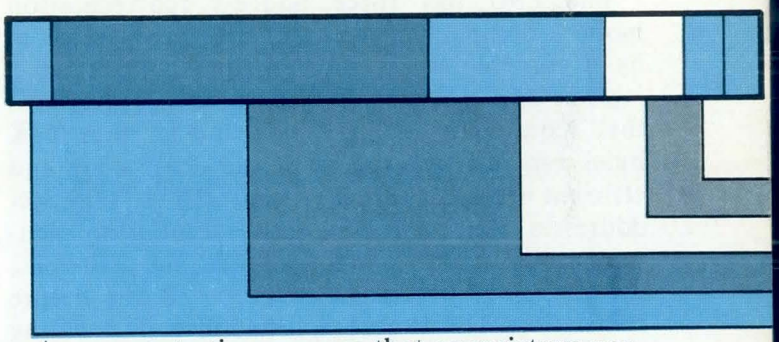
by Donald Alpert

Memory management is becoming an indispensable tool for microprocessor-based system designers. Thus far, because of semiconductor technology limitations, 16-bit microprocessor families have been unable to offer both memory management and central processing unit in the same integrated circuit. Soon, however, Zilog's Z80,000 32-bit microprocessor will do just that.

This compatible extension of the Z8000 architecture will be available in the spring of 1984. Until then, a combined Z8003 virtual memory processing unit and Z8015 paged memory management unit system can implement a subset of the Z80,000 memory management feature. This opens the path for migration from 16- to 32-bit microprocessor systems.

There are two primary advantages of having memory management and central processing unit (CPU) on one chip: a parts-count reduction, and a memory access time improvement. Memory management itself provides access protection and address translation—two valuable attributes.

Donald Alpert is a component architect at Zilog, Inc, 1315 Dell Ave, Campbell, CA 95008. He is responsible for the Z80,000 microprocessor architecture. Mr Alpert holds an MSEE from Stanford University.



Access protection ensures that proprietary portions of memory, or those portions concerned with crucial operating system functions, are protected from tampering. Address translation, the process of mapping logical to physical memory addresses, streamlines system performance. It allows programs to be relocated in memory, thus freeing the operating system from rigid allocation constraints.

Another memory management attribute, virtual memory, allows programs to execute even when only part of the required memory is available in the form of random access memory (RAM). The rest of the program can be stored on disk. Thus, virtual memory improves a system's cost/performance by permitting programs to execute on systems with varying amounts of memory.

System architecture

Compatible with Z8000 family application software, operating systems, and peripheral components, the Z80,000 CPU enhances addressing, register files, instruction sets, and external interfaces.

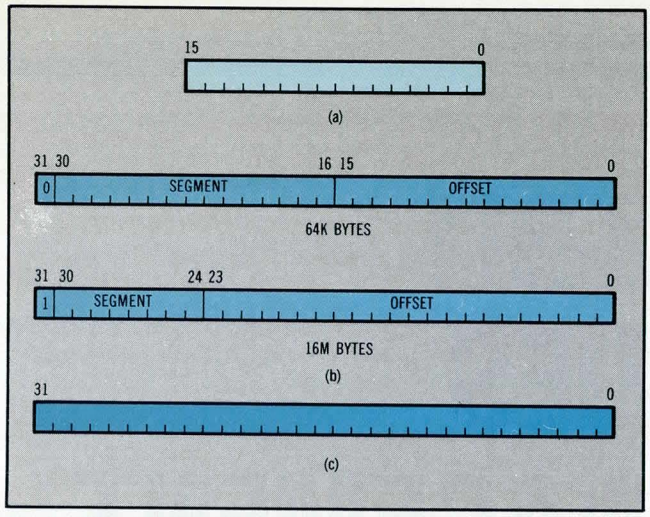


Fig 1 The Z80,000 CPU supports three address representation modes—compact address (a), segmented address (b), and linear address (c). The 16-bit, compact addresses are preferred when less than 64K bytes are addressed. Segmented mode offers two segment sizes (64K and 16M bytes). Linear mode provides uniform access to 4G bytes.

Logical 32-bit addresses offer direct access to 4G bytes of memory in each of four address spaces: system instruction, system data, normal instruction, and normal data.

The CPU has three address representation modes—compact, segmented, and linear—selected by 2 control bits in the flag and control word register (Fig 1). Using compact mode, applications that require an address space smaller than 64K bytes can take advantage of the dense code and efficient use of base registers with 16-bit, compact addresses. Although programs executing in compact mode can only manipulate 16-bit addresses, the logical address is extended to 32 bits before translation. This is accomplished by concatenating the program counter register's 16 most significant bits (MSBs).

Segmented mode supports two segment sizes—64K and 16M bytes. The MSB of the 32-bit address is used to select a 15-bit segment number with 16-bit offset, or a 7-bit segment number with 24-bit offset. Thus, up to 32,768 of the smaller segments and 128 of the larger segments are available to the programmer. In segmented mode, address calculations involve only the segment offset; the segment number is unaffected. Allocating individual objects such as a program module, stack, or large data structure to separate segments, lets many applications benefit from segmentation's logical structure.

The 32-bit addresses in linear mode provide uniform and unstructured access to the 4G bytes of memory. Some applications benefit from linear addressing's flexibility by allocating objects to arbitrary locations in the address space.

The Z80,000 CPU's register file includes sixteen 32-bit general purpose registers that can be used as data accumulators, index values, or memory addresses. The instruction set is oriented toward compilation of high level language programs. Nine addressing modes can combine with operations on many data types including 8-, 16-, and 32-bit integer and logical values; bits; bit fields; packed binary coded decimal bytes; and dynamic length strings. Call, enter, exit, and return instructions perform procedure linkage. The Z8070 arithmetic processing unit, a coprocessor, implements floating point arithmetic.

While the CPU also provides separate operating modes and corresponding address spaces for system and application software, only programs in the system mode are allowed to execute sensitive instructions controlling interrupts and memory management. The memory management mechanism grants the system mode programs access to memory areas inaccessible to programs operating in the less privileged, normal mode. Furthermore, the two operating modes use separate stacks. Sensitive operating system parts usually execute in system mode, where they are protected from potential errors and mischief. Normal mode programs use both the system call instruction and trap to request operating system services.

An onchip cache for instructions and data is also included in the CPU. This highly pipelined design can execute 1.0 to 1.5 million instructions per second (MIPS) at a 10-MHz clock frequency, and up to 3.5 MIPS at the 25-MHz clock rate. A system designer can fine tune performance by selecting not only the clock rate, but also the access time and data width for the memory. For two memory regions, the CPU can be programmed to control both the number of wait states automatically inserted, and whether the data path is 16 or 32 bits. Given these options, a system can easily accommodate a slow, 16-bit wide bootstrap read only memory in one memory region, and a fast, 32-bit wide RAM in another region. In addition, the CPU supports an optional burst transfer of several memory words from consecutive addresses. This makes it easy to use with "nibble mode" RAMs.

Organizing memory management

The CPU and operating system cooperate to translate a program's logical addresses into physical addresses that are used to access memory. The CPU's paging scheme is similar to that in most mainframes and superminicomputers. First, the operating system creates translation tables in memory, then initializes pointers to the tables in control registers. The CPU automatically references the tables to perform address translation and access protection for each memory reference.

To manage the 4G-byte logical address space, the translation scheme divides it into fixed-size, 1K-byte pages. The logical address's 22 high order bits select a page in the address space, while the 10

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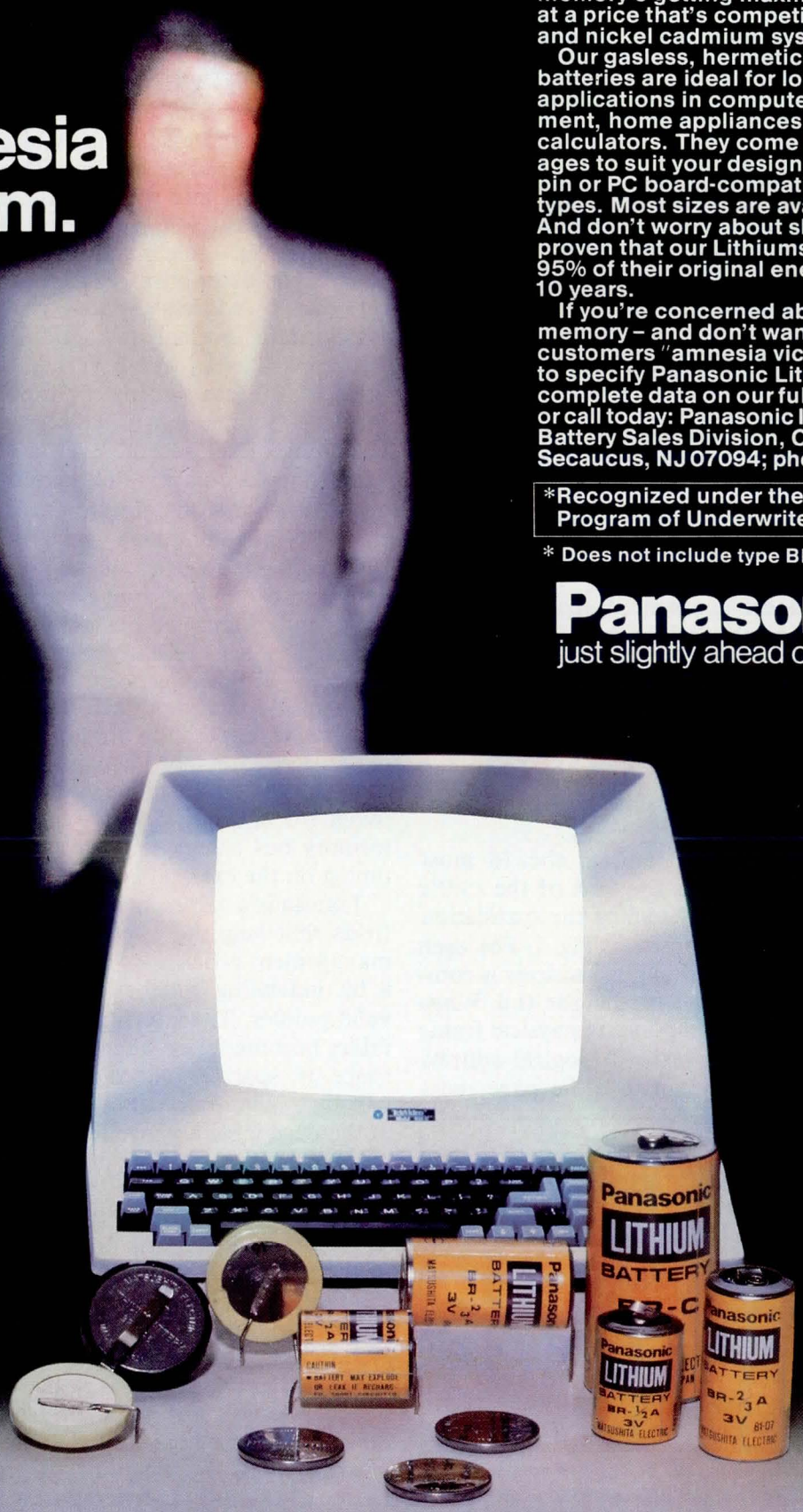

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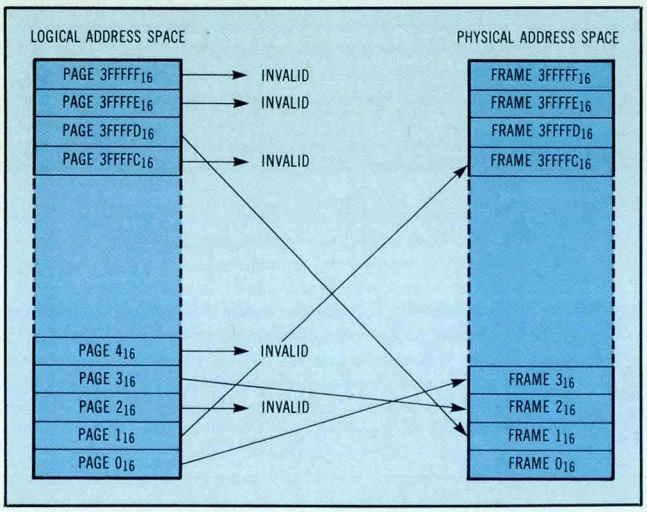

Fig 2 Paged address translation maps a logical page to any physical frame. For the CPU to perform the mapping, the operating system creates tables to tell the CPU which frame corresponds to each page. Some pages can be stored on disk instead of memory and are marked invalid. Pages and frames contain 1K byte each.

low order bits select a byte within the page. Similarly, the physical address space is divided into equal-sized 1K-byte units, called frames. The memory management mechanism maps a logical page to an arbitrary physical frame (Fig 2). Having both the pages and frames of fixed and equal size greatly simplifies the operating system's memory allocation problem. For example, when more memory is needed because a stack has grown, or a program must be brought in from the disk, any frame from a list of free frames can be selected for use.

Storing information to translate the 16 most recently referenced pages is the task of the CPU's onchip associative memory, called the translation lookaside buffer (TLB), shown in Fig 3. For each memory reference, the logical page address is compared with the address tags stored in the TLB. When a match is found, the corresponding physical frame address is read. The low order 10 logical address bits, which select the byte within the page, pass

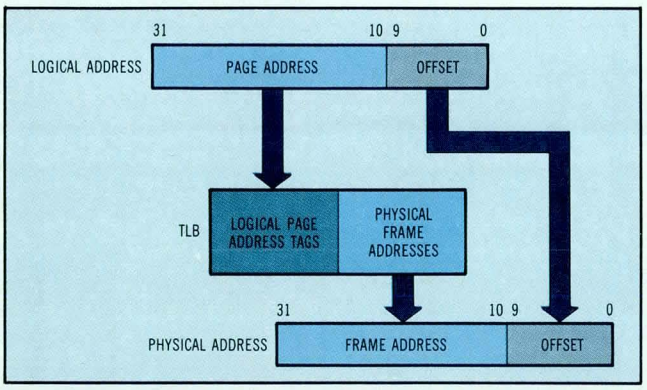

Fig 3 For address translation, the onchip TLB translates logical to physical addresses. The fully associative memory buffers translation information for the 16 most recently referenced pages.

through untranslated. Sometimes (2% or fewer memory references), the information needed to translate a logical address is missing from the TLB. When this occurs, the CPU references translation tables in memory to automatically load the TLB. The missing information replaces the least recently referenced page's TLB entry.

To load a missing TLB entry, the CPU translates the logical address using tables the operating system has placed in memory. The logical page address is divided into three fields that correspond to different translation table levels (Fig 4). The CPU finds the first table's address by selecting one of four table descriptor registers according to the reference's address space—system instruction, system data, normal instruction, or normal data. The L1-NO (level 1 number) field of the logical address is an index into the first level table to select the level 1 table entry. This entry points to the beginning of the second level table. Similarly, the L2-NO (level 2 number) field selects the level 2 table entry, which in turn points to the page table. Finally, the P-NO (page number) field acts as an index into the page table to select the page table entry, which contains the physical frame address. The CPU loads page and frame addresses into the TLB entry holding the least recently referenced page.

System designers can use the address translation mechanism for memory mapped input/output (I/O). In this way, application programs are permitted protected access to individual peripheral devices. The CPU uses the frame address's MSB to distinguish between I/O and memory references because I/O and memory bus transactions have different status and timing on the external interfaces.

Translation table entries (Fig 5) include several fields that help the operating system use memory management efficiently. First, each table entry has a bit indicating whether the contents make up a valid pointer. The advantage of such multiple-level tables becomes clear when the large logical address space is sparsely allocated. For example, if a 64K-byte memory block is not in use, all 64 entries in the page table are invalid. Rather than waste 256 bytes of memory to store a page table filled with invalid entries, the pointer to the page table can simply be marked "invalid." Also, when only part of the table entry is valid, it is unnecessary to fill the rest of the table with invalid entries. A field indicating the table size in 256-byte increments accompanies pointers to the first two table levels. Moreover, the growth direction bit indicates whether the upper or lower entries in a partial table are valid. This is particularly useful for managing stacks that grow downward from high to low addresses.

Since many applications do not require the Z80,000 CPU's full 4G-byte address space, the table descriptor register's field indicates that the CPU should skip either or both of the first two table

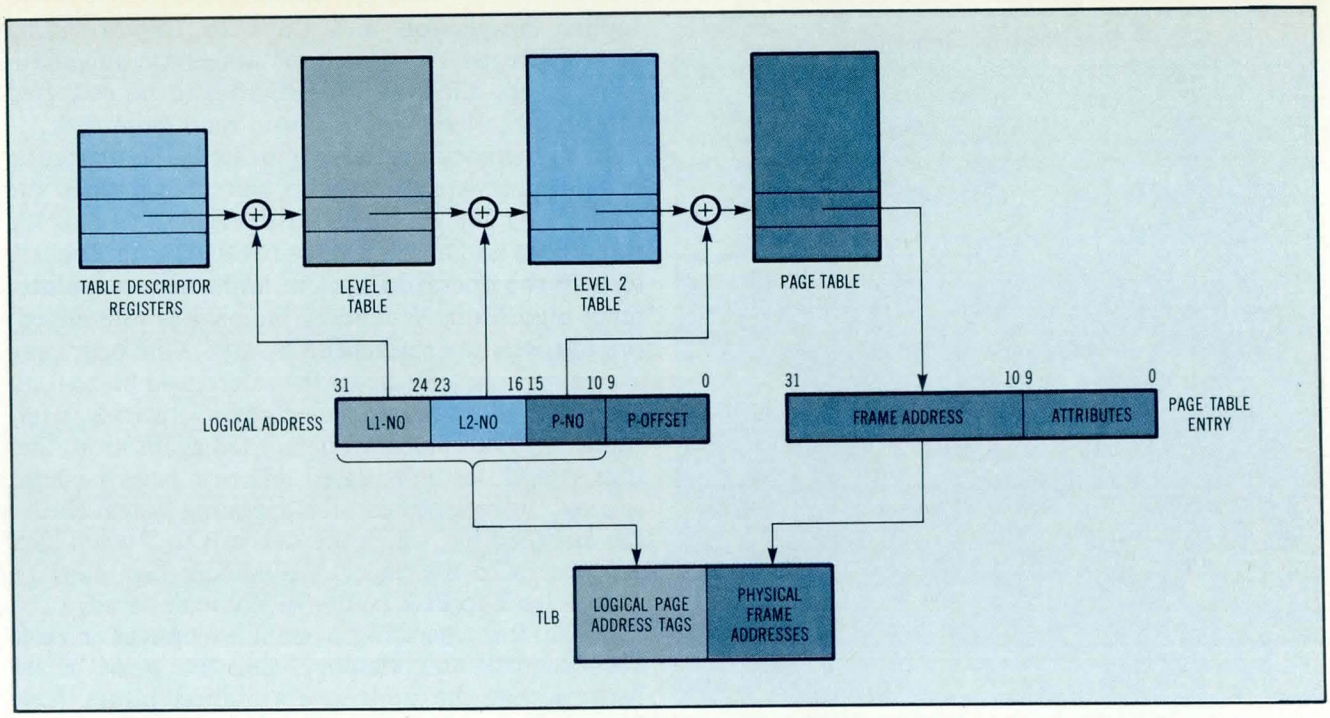

Fig 4 Using tables in memory, the CPU automatically loads the TLB. Three table levels are used to accommodate address spaces from 64K bytes to 4G bytes. System designers can eliminate either or both of the first levels to make tables smaller and to speed translation.

levels. For example, a 16M-byte address space using 24-bit addresses can be translated by skipping level 1 tables. Compact 16-bit addresses can skip both levels. The level 2 tables can be skipped for compatibility with the segmented Z8000 address scheme. By eliminating superfluous translation tables, system designers can save memory space and shorten the TLB loading time.

On each memory reference, the CPU uses information stored in the TLB for access protection and for translation. Read, write, and execute access rights are checked in both system and normal

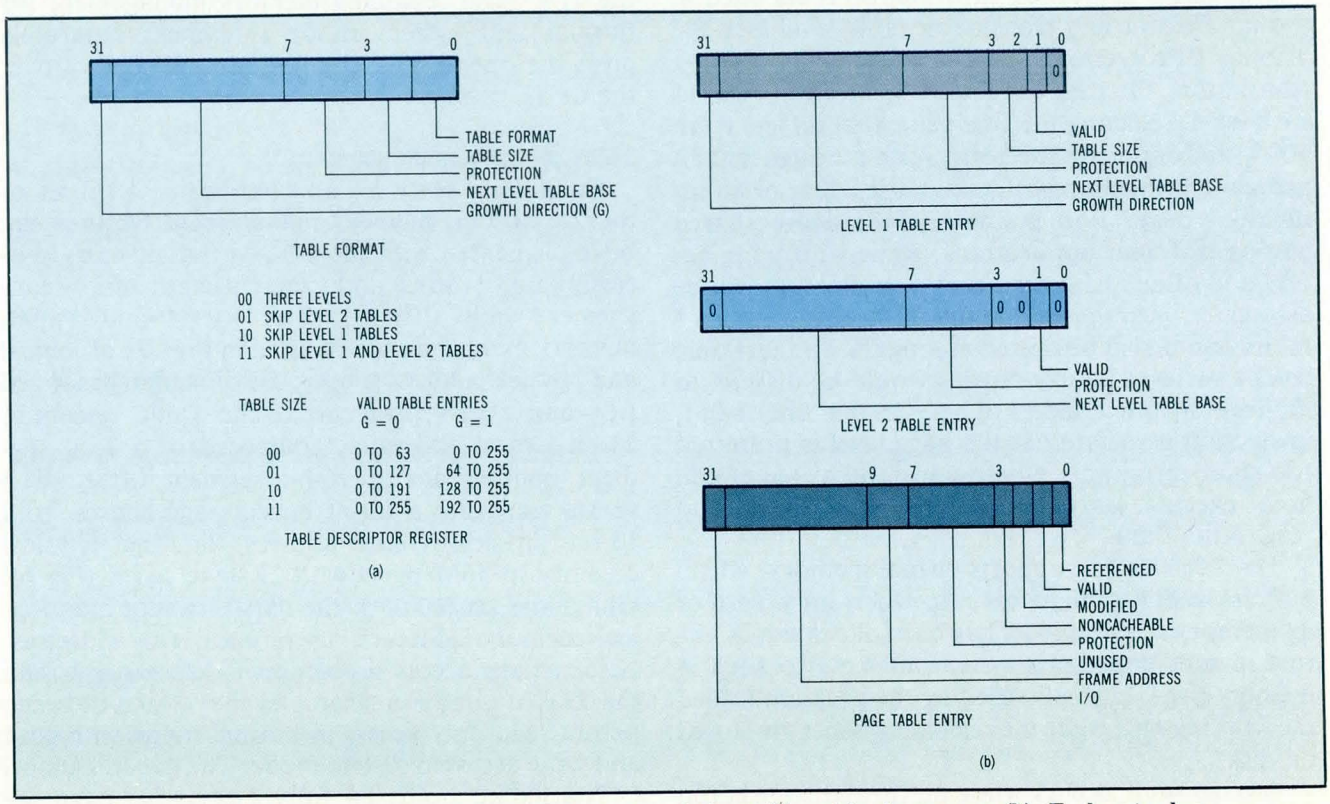

Fig 5 The CPU's table descriptor register (a) points to the translation table entries in memory (b). Each entry has several fields, allowing the operating system efficient control over memory management.

Protection Field Encoding

Encoding	System	Normal
0000	NA	NA
0001	RE	NA
0010	RE	E
0011	RE	RE
0100	E	NA
0101	E	E
0110	R	NA
0111	R	R
1000	Note	Note
1001	RW	NA
1010	RW	R
1011	RW	RW
1100	RWE	NA
1101	RWE	E
1110	RWE	RE
1111	RWE	RWE

NA – no access permitted
R – read access permitted
W – write access permitted
E – execute access permitted
Note – use the protection field of the next level translation table or NA (for page tables).

operating modes. Data can thus be protected from being overwritten or mistaken as executable code. The CPU protects proprietary programs from duplication by permitting execute access but not read access. System mode has all normal mode access rights, but can optionally have more. Thus, regions of system memory can be kept totally inaccessible to applications, or restricted access can be granted to applications.

The access protection information is encoded in a 4-bit field at any translation table level (see the Table, "Protection Field Encoding"). During translation, the CPU checks the protection field at each level, selecting the first value that differs from 1000, and ignoring the rest. System designers can associate protection with either a segment or an individual page. For example, if data are shared among different applications, some with write access and others with read access, protection will be associated with the data segment. In this way, page tables could also be shared among the applications; level 1 or level 2 table entries would be distinct to indicate different access rights. On the other hand, protection associated at the page level is preferred for small programs where consecutive pages can hold execute only code, read only data, and read/write data.

The Z80,000 CPU supports virtual memory, which permits a program to execute when only part of its memory requirements has been allocated. A virtual memory operating system attempts to keep in memory pages currently used by the program (called the working set), while the remaining pages are stored on disk.

A page fault occurs when an invalid translation table entry indicates that a referenced page is not in memory. The CPU then suspends execution of the faulted instruction and traps to the operating system. Register and memory states are automatically saved, allowing the program to be restarted after the faulted page has been read from disk.

If all memory has been allocated, the operating system must select a page to be replaced when the memory is loaded from disk. The CPU sets the referenced and modified bits in the page table entry to help the operating system implement a replacement algorithm. Whenever the page is referenced, the CPU sets the referenced bit to 1. The operating system periodically clears the referenced bit to 0, to determine recently referenced pages. Recently referenced pages are likely to be needed again soon, and thus should not be replaced. When a page has been selected for replacement, the operating system checks the modified bit, which the CPU sets to 1 when data are written to the page. A modified page must be written back to disk before it can be replaced.

When the operating system exchanges a page between disk and memory, the CPU must be informed that the address translation tables have been changed. This allows stale information to be removed from the TLB. There are three Purge TLB instructions. Purge TLB entry is used when the information mapping a single page has been changed. Purge TLB normal is used to remove the normal mode TLB entries. When a process switch occurs, the entire normal mode memory map changes but the system mode map does not. The third instruction, Purge TLB, is used to remove all entries from the TLB. Also, enabling memory management for normal and system mode references separately gives the operating system additional control over the CPU.

Z8003 memory management

Combining software and hardware, a subset of the Z80,000 CPU memory management features can be implemented with the Z8003 virtual memory processing unit (VMPU) and Z8015 paged memory management unit (PMMU). The VMPU and PMMU memory management is limited in the size of logical and physical address spaces, use of memory mapped I/O, and access protection. The VMPU generates 23-bit logical addresses, composed of a 7-bit segment number and a 16-bit segment offset. The PMMU translates a 12-bit logical page address to a 13-bit physical frame address, limiting physical memory to 16M bytes with 2K-byte pages (Fig 6). Unlike the Z80,000 CPU, the PMMU cannot map logical memory addresses to physical I/O addresses. Also, PMMU access protection is less general than the Z80,000 CPU. For example, the Z80,000 CPU can permit read only access in normal mode with read and write access in system mode. The PMMU cannot.

The PMMU holds 64 fully associative page descriptor registers. Like the Z80,000 TLB entries, each of the PMMU registers contains a logical page

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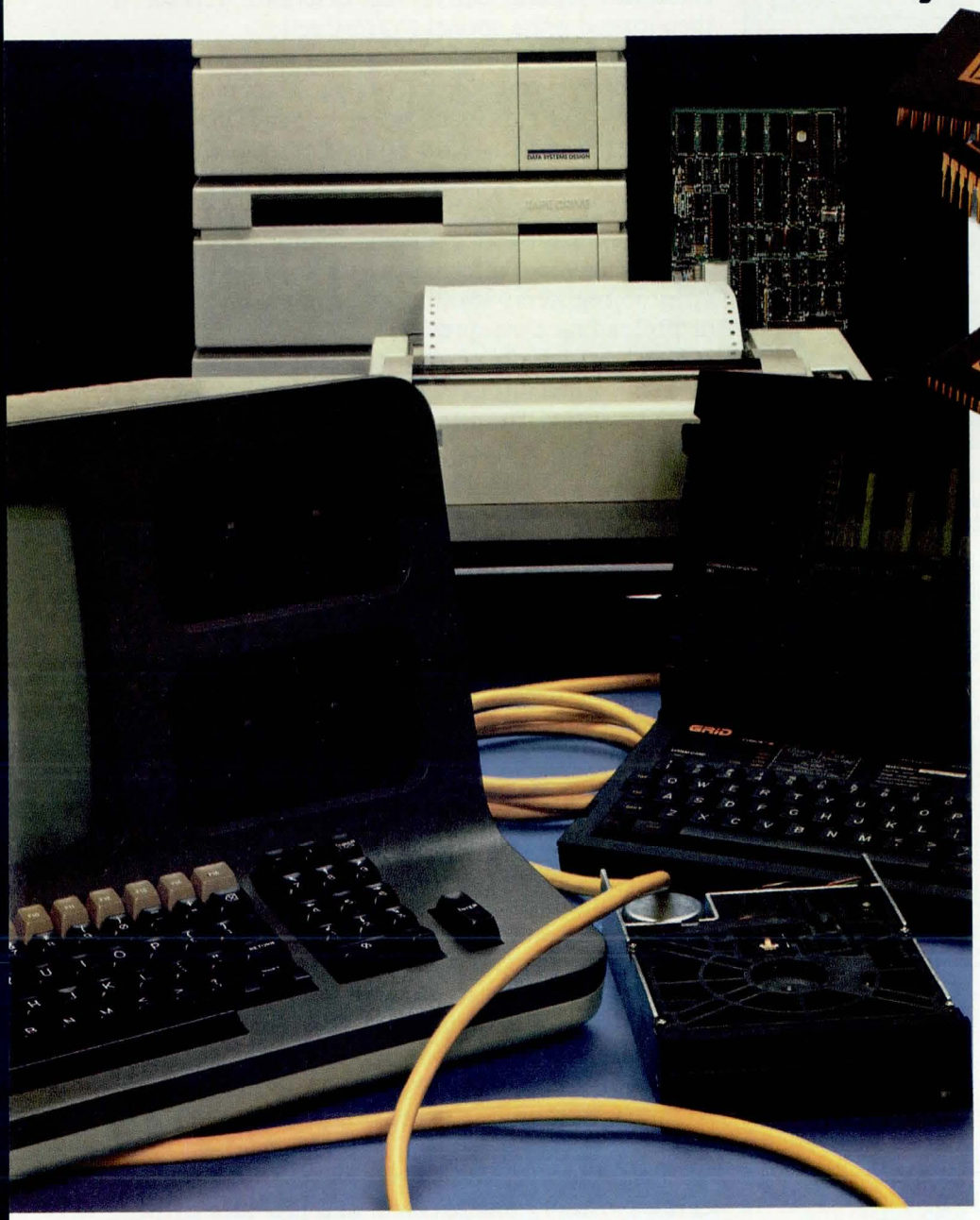

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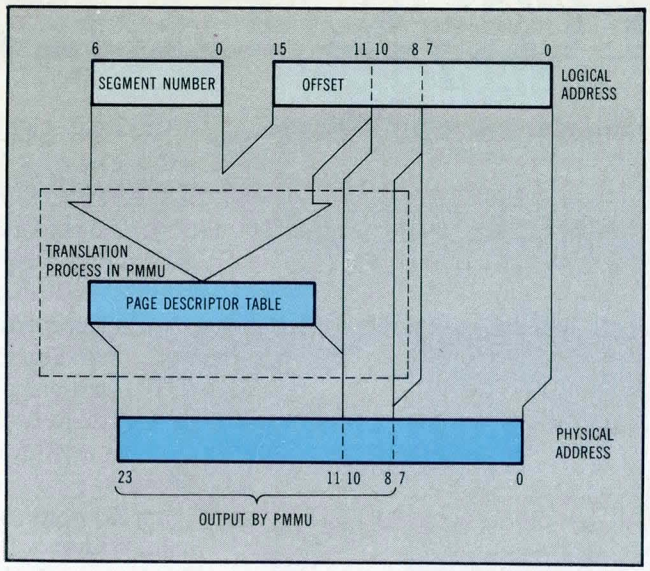

Fig 6 In logical to physical address translation, the PMMU translates a 12-bit logical page address to a 13-bit physical frame address. Like the Z80,000 CPU, the PMMU translation buffer is fully associative.

address, a corresponding physical frame address, and an attribute field. This field includes protection information, and referenced, modified, and valid bits. However, unlike the Z80,000 CPU, which automatically loads missing information into the TLB, software must load the PMMU registers.

On every memory reference the VMPU makes, the PMMU performs an associative search of the page descriptor registers to locate a valid matching page address. If it finds a match, it reads the corresponding frame address and attributes. If the attributes permit memory reference, the PMMU outputs the physical frame address to memory. If no match is found or a protection violation occurs, the PMMU requests the processor to abort the instruction and generate a trap.

In a hardware configuration, one VMPU and two PMMUs can be used to support the 1K-byte pages used in the Z80,000 CPU. One PMMU is used to translate even page addresses (address bit 10 is 0); the other PMMU translates odd page addresses (address bit 10 is 1). The CPU references the contents of the PMMUs with the special I/O instructions, which transfer data on the upper byte of the data bus. If separation of system/normal or instruction/data address spaces is desired, additional PMMUs are used.

The VMPU's operating system constructs translation tables in memory using the Z80,000 CPU's skip level 2 format. The operating system must also implement two functions that the Z80,000 automatically performs—loading translation table entries from memory to the PMMU, and recovering from address translation traps.

To load the translation entry for a logical page, software executes the algorithm described for the Z80,000 CPU. The physical frame address, protection field, referenced bit, and modified bit are fetched from tables in memory and used to construct a PMMU descriptor register entry. The descriptor register is then loaded using special I/O instructions.

If the memory contains less than 128K bytes, two PMMU circuits can map every page in memory. The operating system loads a new page descriptor whenever a page is read from disk, replacing the descriptor that previously pointed to the frame. More often, however, the memory is too large to be fully mapped by two PMMUs. Thus, the system designer has two alternatives for loading page descriptor registers: loading descriptors on demand or preloading descriptors.

Loading descriptors on demand, as the Z80,000 CPU does when information to translate a referenced page is missing from the TLB, incurs a small delay to move a single descriptor whenever a new page is referenced. Preloading descriptors when a new program is selected to run on the VMPU incurs a large, onetime delay. If the user's programs run for a short time and reference few pages, preloading is better than demand loading. System designers must consider memory size, amount of multiprocessing, and other performance requirements of a system to make the correct choice. With either choice, a descriptor register must be selected for replacement when a new entry is loaded. For this, a first in, first out algorithm is adequate. Upon replacing a PMMU descriptor, the referenced and modified bits must be copied back to the page table entry in memory.

When an address translation trap occurs, some software intervention is necessary before the program can be restarted. Generally, this just involves replacing the program counter value, saved by the VMPU on the system stack, with the correct address of the trapped instruction. This instruction is found in a PMMU control register. For some instructions, such as push and pop, it may also be necessary to modify the general purpose registers' contents.

Thus, the Z80,000 32-bit microprocessor integrates memory management and provides significant performance improvements over current 16-bit microprocessors. A compatible migration path to high performance, 32-bit microprocessor systems is available with the Z8003 VMPU and Z8015 PMMU 16-bit microprocessor components.

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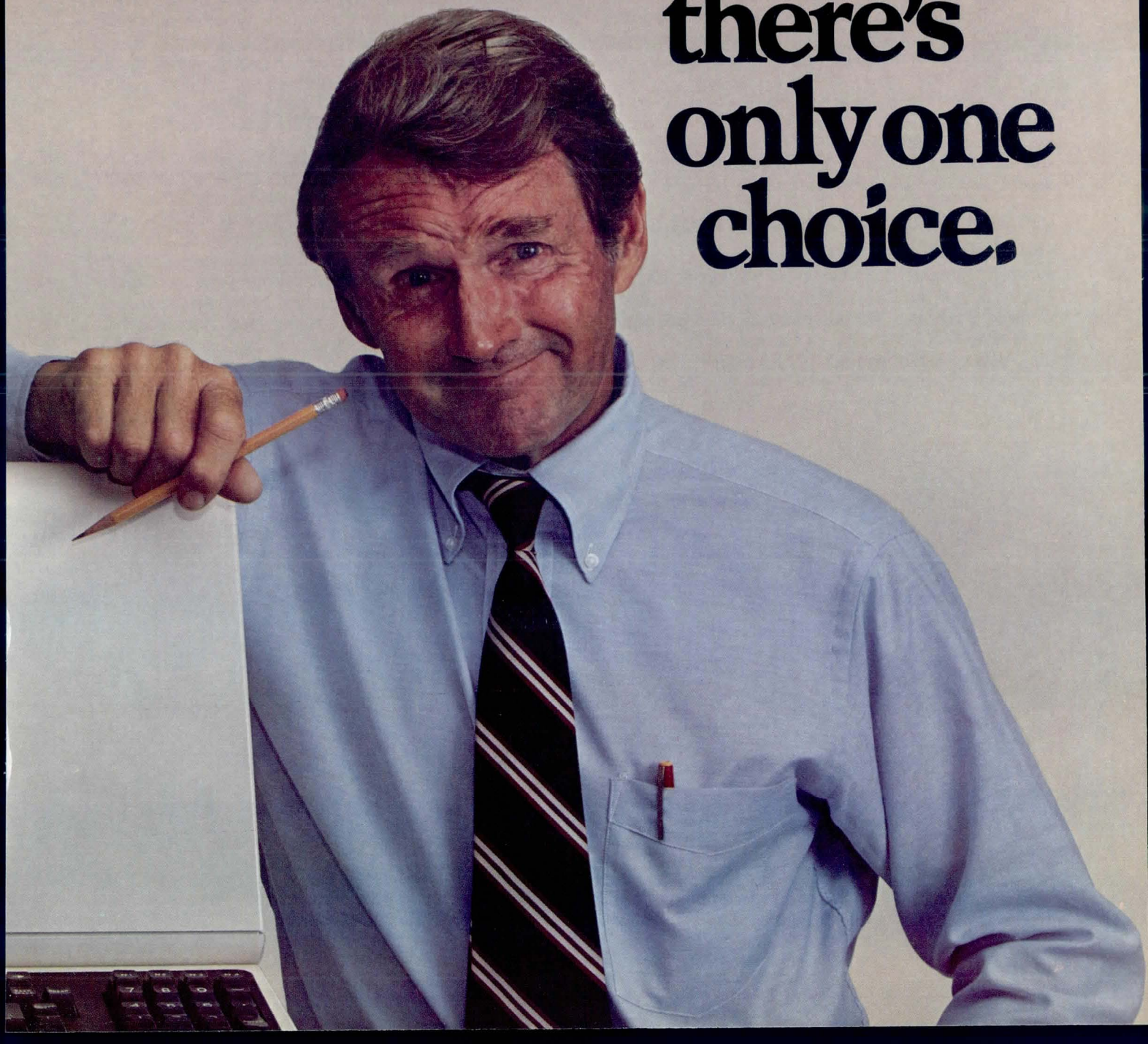

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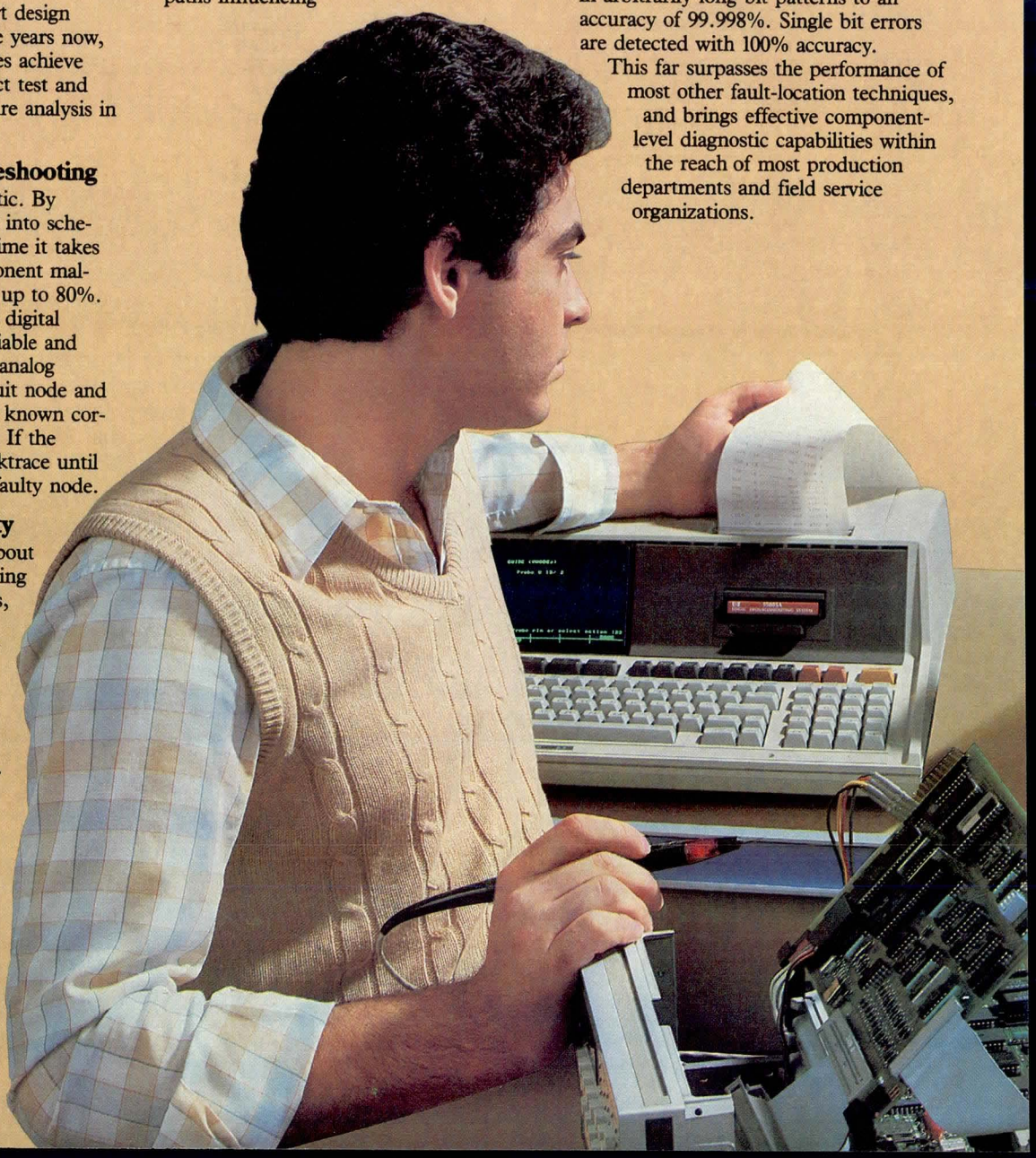

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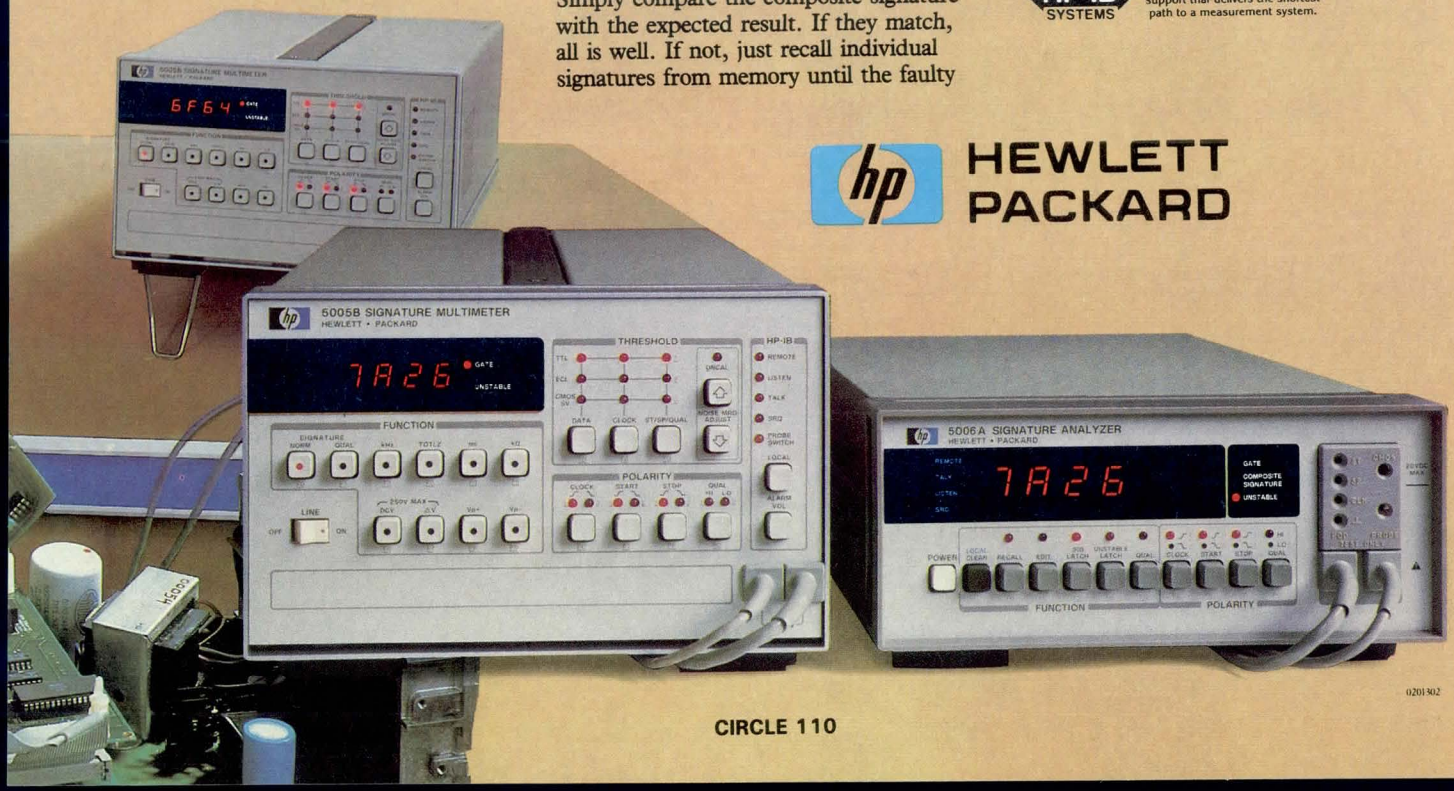

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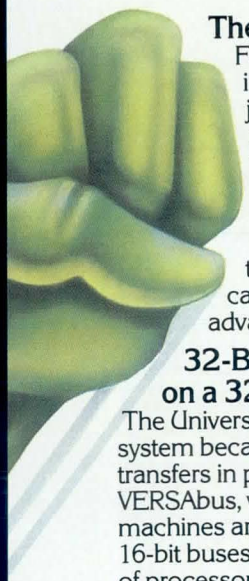

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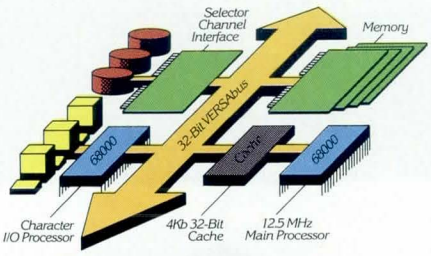

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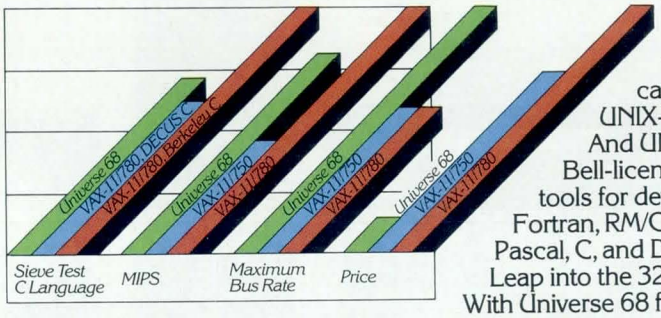

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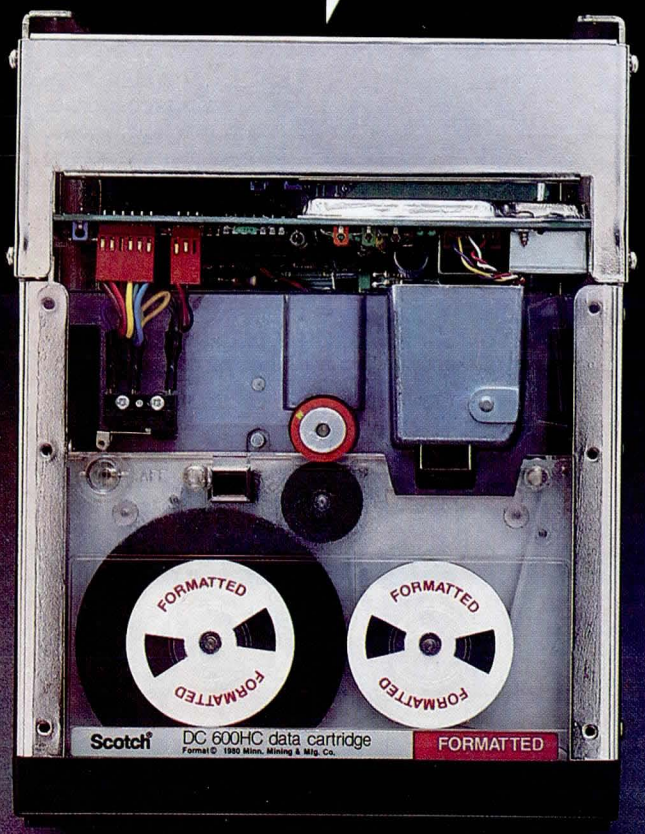

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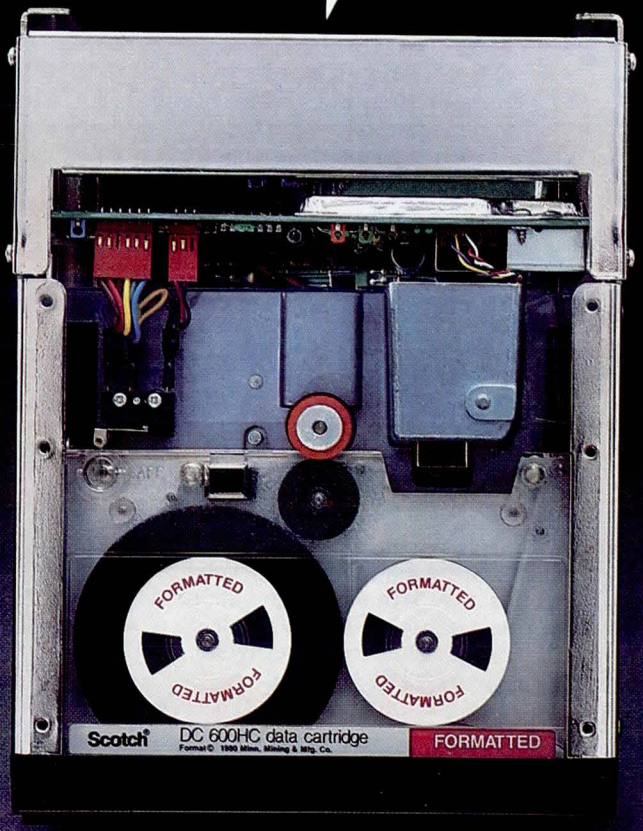

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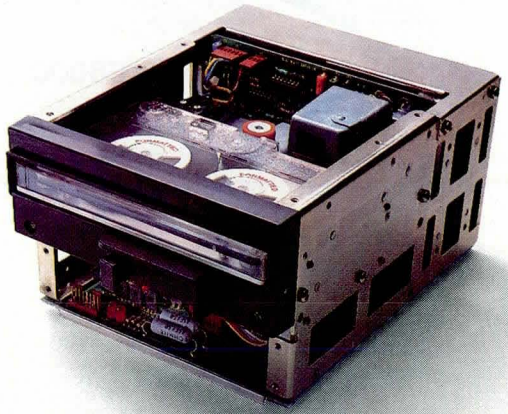

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MICROCONTROLLER ADDRESSES CONTROL AND INSTRUMENTATION

A 16-bit single-chip microcontroller, with a 68000-like architecture, handles I/O tasks in standalone or multiple CPU systems.

by Don Folkes and John Bates

Control and instrumentation applications, such as robotics and engine controls, require high throughput and extensive math capability from their processors. Similarly, intelligent peripheral subsystems can be considered control systems, since they must handle the interface to such input/output devices as terminal concentrators, floppy disks, and magnetic tape drives.

Since these subsystems must operate in parallel with a data processing central processing unit (CPU), they should have an interface that allows a high speed parallel data transfer to and from system memory using direct memory access (DMA). Although these systems can be built with multichip microprocessor components, a high performance single-chip microcontroller with extensive onchip input/output (I/O) resources can effectively reduce the part count.

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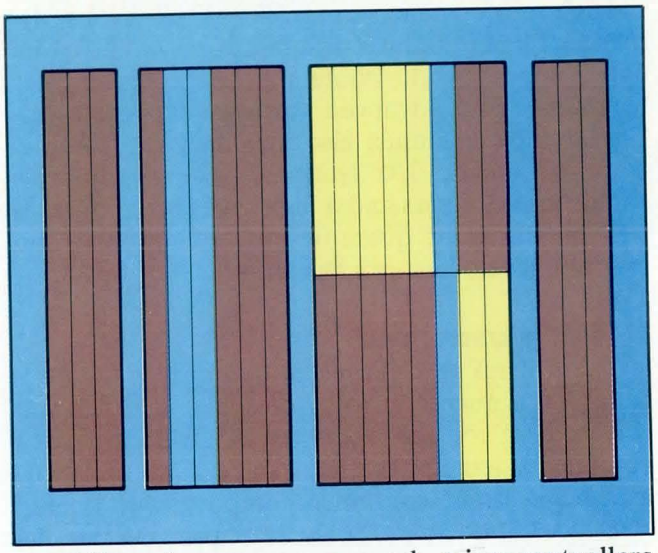
John Bates is a senior software engineer at Mostek. He holds a BS in engineering science from Florida State University and an MS in systems engineering from Southern Methodist University.



While microprocessors and microcontrollers have architectural similarities, there are major differences. For I/O-intensive applications, a microcontroller must provide extensive bit-manipulation capability as well as fast accessing of I/O ports. The instruction set must be powerful, but must also be optimized in order to save code space and meet the constraints of onchip read only memory (ROM). Instruction execution time must be kept to a minimum so that high speed control loops can be coded and still have time available for numerical calculations.

Rapid interrupt response and provisions for multiple interrupt sources are necessary for efficient processing of external stimuli. However, special

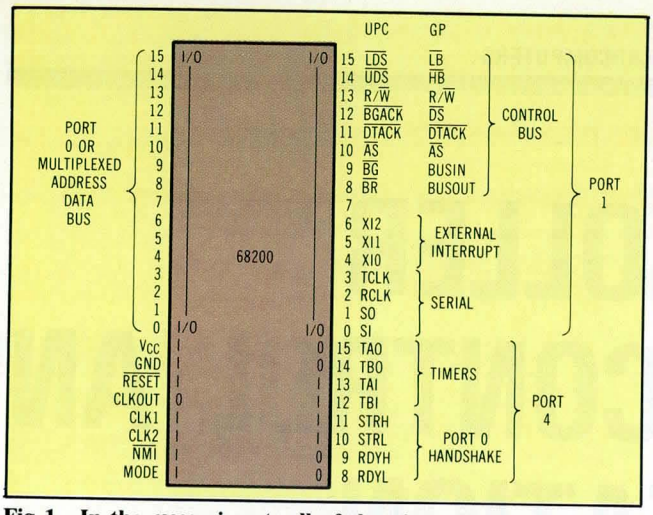


Fig 1 In the 68200 pinout, all of the pins shown on ports 0 and 1 can function as general purpose parallel I/Os. The I/O pins with special functions can be programmed to serve those functions or be used as simple inputs or outputs. Strapping the mode pin selects one of the expanded bus modes, where port 0 becomes a 16-bit multiplexed address data bus and eight pins of port 1 function as associated control signals.

instructions that support multi-user or multitasking environments are unnecessary because microcontrollers rarely communicate directly with a user in a data processing application.

High performance controller applications demand a regular architecture that is easy to program and support with contemporary programming techniques and advanced software support tools. The architecture must also include a full complement of onchip I/O features, such as multiple sophisticated timers and a high speed serial port, as well as sufficient quantities of onchip ROM and random access memory (RAM).

A 16-bit microcontroller

The Mostek 68200, a recent addition to the 68000 family, is a microcontroller device designed to suit the needs of control processing in a wide variety of complex system applications. In addition to its role as a 16-bit single-chip microcomputer with onchip CPU, ROM, RAM, and I/O, the 68200 provides parallel expanded bus modes that operate with a full complement of multiprocessing features. It thus breaks the tradition set by previous generation single-chip microcomputers. The user-selectable I/O architecture allows the device to operate as a high performance single-chip microcomputer, a fully expandable CPU that can address external memory and I/O, or as a dedicated I/O controller that can share a 16-bit system bus with a 68000 or some other 16-bit microprocessor. In addition, the 68200 provides an onchip serial I/O port that operates efficiently in a multidrop network.

This device has a CPU architecture and instruction set modeled after the 68000, but optimized for microcontroller applications. Not only does the instruction set offer full 16-bit computational capability with multiply and divide, but it also emphasizes 8-bit handling, I/O port handling, and bit manipulation. These are crucial features in high performance control applications.

The architectural similarities make it easy for a designer familiar with the 68000 to develop systems incorporating the 68200. In hardware, the expanded bus is available with a version of the chip that provides 68000 control signals. In this way, the 68200 can connect directly to the 68000 system bus as a universal peripheral controller (UPC). In software, the assembly language mnemonics and syntax are very similar for both processors, making it easy for a programmer familiar with the 68000 to write code for a 68200.

Pinout configuration

Forty of the 48 available pins on the package can be used for I/O, and their functions are programmable. I/O capabilities include parallel I/O, three timers, a serial channel, and an interrupt controller. In the single-chip configuration, all 16 bits of port 0 and 9 bits of port 1 are used for general purpose I/Os (Fig 1). In addition, either half or the entire 16 bits in port 0 can be selected as bidirectional I/O pins, using the handshake option on port 4. The remaining 7 bits in port 1 can also be programmed as I/Os, or used to serve the designated special function shown in the diagram. Up to three of these pins on port 1 can be programmed as external interrupt sources, and up to four pins can be programmed as I/Os for the onchip serial channel.

The 68200's data-register organization allows more efficient register use for byte-oriented operations.

Similarly, all 8 bits in port 4 can be used as simple inputs or outputs or can serve the alternate function designated in the diagram. For example, TAI can be used as an input for timer A, an interrupt source, or a general purpose input pin. If it is used as an interrupt source, it can be selected simultaneously with either of the other two functions. These flexible I/O features make the 68200 a good choice for standalone applications that also require 16-bit computational capability, such as engine control.

Strapping the mode pin places the 68200 in its expanded bus mode. Port 0 and port 1 are then reconfigured to provide the necessary functions. Port 0 becomes the 16-bit multiplexed address/data bus, and 8 bits from port 1 become control signals that handle data transfer and bus arbitration. As shown in Fig 1, two different control buses are available as a mask option: a UPC bus that generates 68000-compatible signals, and a general

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purpose (GP) bus that can be used to interface to a wide variety of existing microprocessor buses. When the expanded bus mode is selected, the 68200 can either act as a GP bus grant or host CPU chip, or as a peripheral I/O controller to a host CPU. These two system configurations are illustrated in Fig 2.

The GP bus version can be used in implementing the host CPU configuration shown in Fig 2(a). In this configuration, the 68200 can be used to interface to external memory and I/O devices in a manner analogous to a general purpose microprocessor. But the 68200 retains its onchip RAM and I/O resources, with onchip ROM as an option. Sixteen lines on the device are still available for I/O functions, including eight lines from port 1 and all eight lines of port 4. The GP control signals include two bus arbitration handshake signals, BUSIN and BUSOUT, which respectively provide the functions of a bus request input and a bus grant output. This feature allows other potential bus masters in the system, such as DMA devices or peripheral I/O control processors, to gain control of the system bus.

As a peripheral I/O controller, the 68200 operates as a bus requester that gains control of the system bus from the bus grant CPU [Fig 2(b)]. In this configuration, the UPC bus version provides a direct interface to a 68000 bus grant CPU. Once the UPC gains control of the system bus via the 68000 bus arbitration handshake lines ($\overline{BR}$, $\overline{BG}$, and $\overline{BGACK}$), it can perform DMA transfers and communicate with system memory or other I/O devices in the system.

Alternatively, the GP bus version can be selected to implement this system configuration in cases where a different host CPU, such as another 68200, is desired. In this case, the BUSIN and BUSOUT lines also perform the bus arbitration handshake function, where BUSOUT now acts as bus request output and BUSIN acts as a bus grant input. Here, the 68200 can conceivably act as a complete peripheral I/O control subsystem on a single chip, with 16 lines of I/O and its onchip ROM, RAM, timers, and serial I/O performing the necessary interface to the I/O device.

If the onchip resources are not sufficient to perform the control task, external devices can be added on an optional local bus, which is physically the same as the system bus, but separated logically by bus buffers. This serves to isolate the I/O subsystem, and the 68200 can relieve the host CPU of I/O-related processing overhead. In other words, the 68200 I/O controller and the host CPU can execute programs concurrently.

Programming architecture

The 68200 register file includes eight data registers, six address registers, and three system registers, all of which are 16 bits wide [Fig 3(a)]. This diagram can be compared with the register set for the

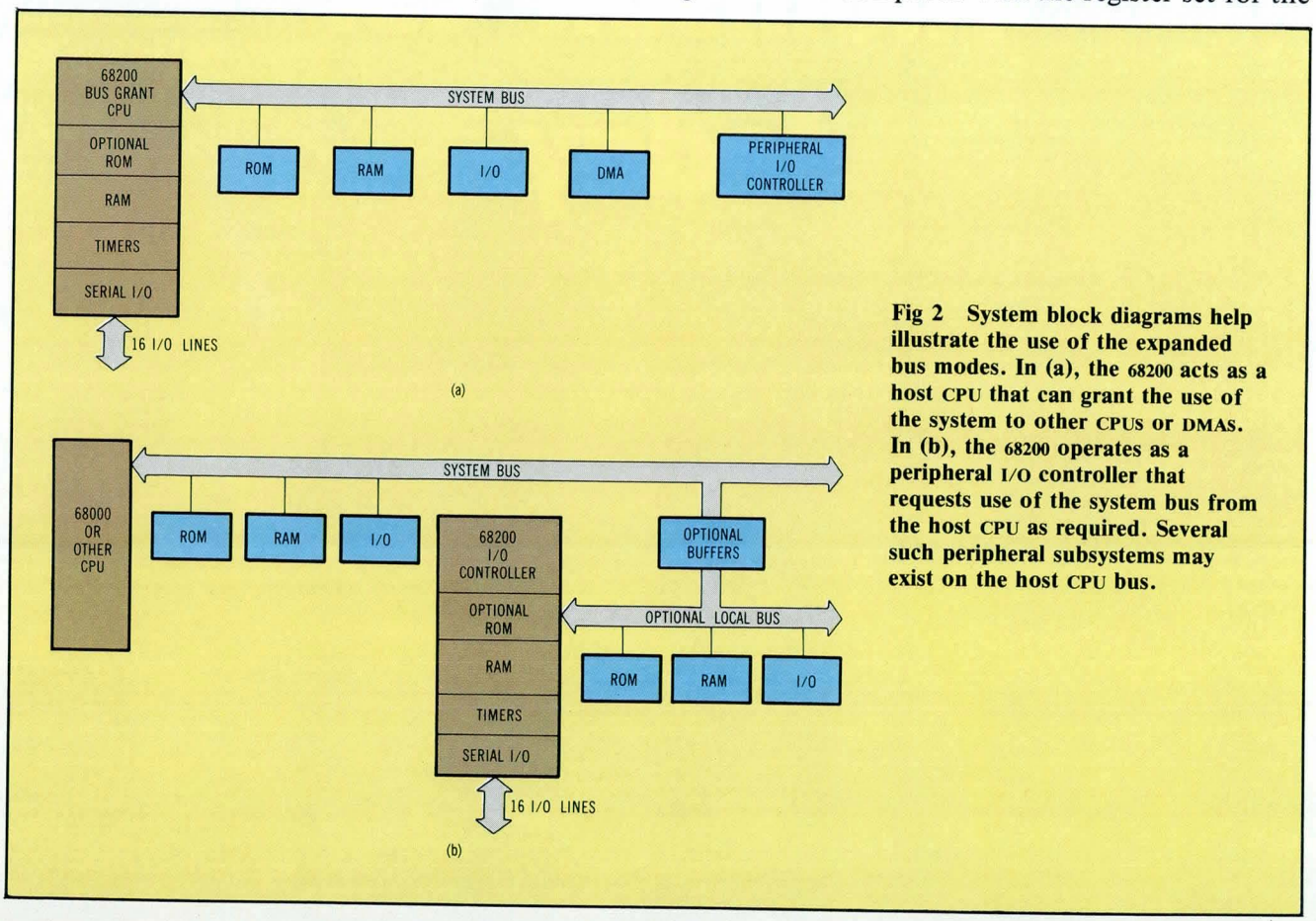

Fig 2 System block diagrams help illustrate the use of the expanded bus modes. In (a), the 68200 acts as a host CPU that can grant the use of the system to other CPUs or DMAs. In (b), the 68200 operates as a peripheral I/O controller that requests use of the system bus from the host CPU as required. Several such peripheral subsystems may exist on the host CPU bus.

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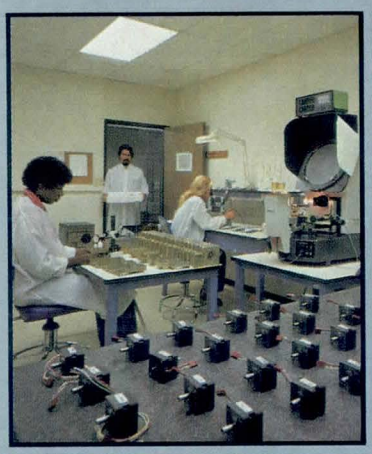

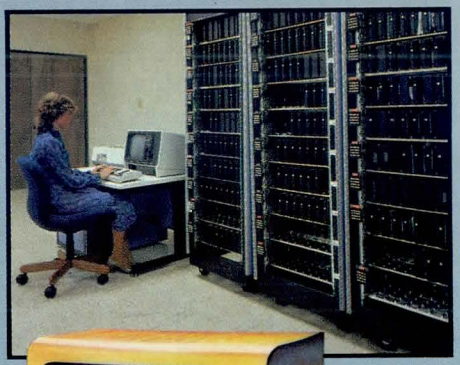

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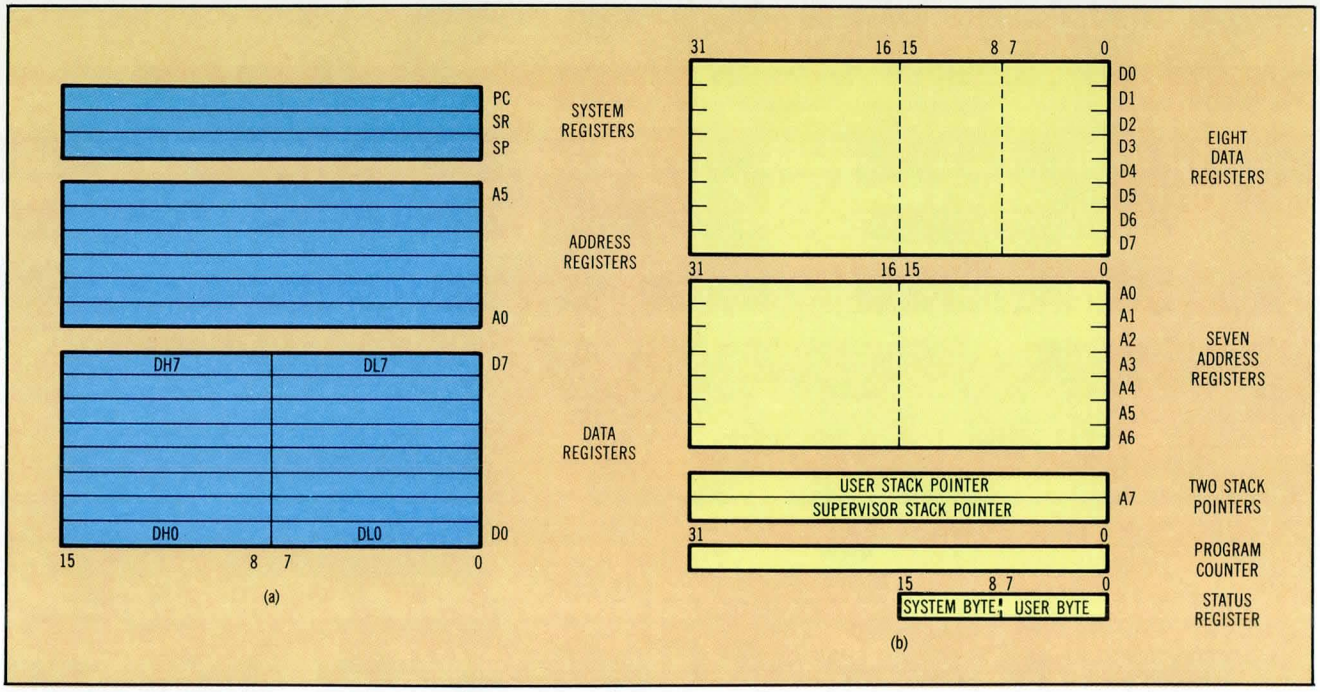

Fig 3 Both the 68200 and 68000 exhibit a regular register architecture with several general purpose data registers and address registers. The 68200 has 16-bit registers that can handle 8-bit data more efficiently (a). The 68000 has 32-bit registers to support a full 32-bit internal processor architecture (b).

68000 [Fig 3(b)]. The general structure of the two register files are very similar. Both machines have several general purpose data and address registers. The basic difference is that the 68200 registers are all 16-bit registers, and the 68000 registers, with the exception of the status register, are all 32 bits wide.

There are other important differences between the register sets of the two machines. The 68200 has eight 16-bit or sixteen 8-bit data-only registers. Each of the 68000's eight data-only registers must be assigned as either an 8-, 16-, or 32-bit register. The 68200 has six 16-bit address registers that can also be used for data. Seven address registers exist in the 68000. They are assigned as either 16 or 32 bits, and can only be used for addressing. The 68200 has one 16-bit stack pointer, while the 68000 incorporates two such registers to support user and supervisory modes in multi-user systems. Similarly, the status register is divided into two parts to support a multi-user environment.

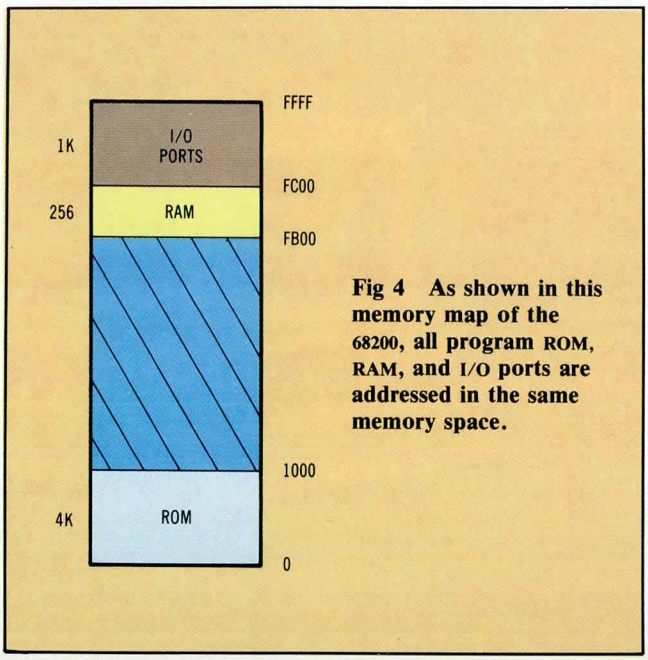

Fig 4 As shown in this memory map of the 68200, all program ROM, RAM, and I/O ports are addressed in the same memory space.

The 68200's data-register organization allows more efficient register utilization for byte-oriented operations. Future high performance control applications will require an increasing number of 16-bit calculations, so the data registers in the 68200 can be used to hold these data. However, it is still necessary to handle 8-bit numbers efficiently. For example, many I/O operations require the handling of ASCII data. Loop counters are also typically implemented in the course of programming control routines, and most of the time these counters are 8 bits or less. Since it is not very efficient to tie up a 16-bit register with an 8-bit counter value, the data registers in the 68200 have the option of using either the entire register for 16 bits, or either half as an independent 8-bit register.

As reflected in the register map, all of the data paths within the 68200 are 16 bits wide, including those to the program memory, RAM, arithmetic logic unit (ALU), and register file. Therefore, the unit can directly address a 64K-byte addressing space that is organized as 32K, 16-bit words. Normally, data are addressed on word boundaries, but the memory is also byte addressable so that data transfers can occur 8 bits at a time.

Since the addressing range matches the size of the internal data path, a full 16-bit address field can be passed in a single memory cycle. This speeds up the instruction execution time. It also allows the ALU to be shared for performing both operand data and address calculations, thereby minimizing the die size.

Fig 4 illustrates the 68200's memory map. The initial ROM version incorporates 4K bytes of ROM and 256 bytes of RAM. As illustrated, all of the 68200's internal RAM and I/O is addressed in the same space as program memory. This allows all of the instructions and addressing modes that can be used to manipulate program variables in RAM to also operate on data contained in lookup tables in ROM, or on data contained in I/O ports.

Similar sets

As the instruction set summary in Table 1 shows, the 68200's instruction set closely resembles the 68000. Because of the architectural differences, the 68200 cannot be opcode compatible with the 68000. However, many of the 68200 instructions bear the same mnemonic to aid the programmer familiar with the 68000 instruction set. In fact, in most cases, the 68000 assembler syntax has been duplicated in ASM-68200, the structured macro cross-assembler available for the 68200.

TABLE 1

68200 Instruction Set

Instruction	Description
ADD	Add
ADD.B	Add Byte
ADDC	Add with Carry
ADDC.B	Add with Carry Byte
AND	Logical And
AND.B	Logical And Byte
ASL	Arithmetic Shift Left
ASL.B	Arithmetic Shift Left Byte
ASR	Arithmetic Shift Right
ASR.B	Arithmetic Shift Right Byte
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BEXG	Bit Test and Exchange
BSET	Bit Test and Set
BTST	Bit Test
CALLA	Call Absolute
CALLR	Call Relative
CLR	Clear
CLR.B	Clear Byte
CMP	Compare
CMP.B	Compare Byte
DADD	Decimal Add
DADD.B	Decimal Add Byte
DADDC	Decimal Add with Carry
DADDC.B	Decimal Add with Carry Byte
DI	Disable Interrupts
DIVU	Divide Unsigned
DJNZ	Decrement Count and Jump if Non-zero
DJNZ.B	Decrement Count Byte and Jump if Non-zero
DNEG	Decimal Negate
DNEG.B	Decimal Negate Byte
DNEGC	Decimal Negate with Carry
DNEGC.B	Decimal Negate with Carry Byte
DSUB	Decimal Subtract
DSUB.B	Decimal Subtract Byte
DSUBC	Decimal Subtract with Carry
DSUBC.B	Decimal Subtract with Carry Byte
EI	Enable Interrupts
EOR	Exclusive Or
EOR.B	Exclusive Or Byte
EXG	Exchange
EXG.B	Exchange Byte
EXT	Extend Sign
HALT	Halt
JMPA	Jump Absolute
JMPR	Jump Relative
LIBA	Load Indexed Byte Address
LIWA	Load Indexed Word Address
LSR	Logical Shift Right
LSR.B	Logical Shift Right Byte
MOVE	Move
MOVE.B	Move Byte
MOVEM	Move Multiple Registers
MOVEM.B	Move Multiple Registers Byte
MULS	Multiply Signed
MULU	Multiply Unsigned
NEG	Negate
NEG.B	Negate Byte
NEGC	Negate with Carry
NEGC.B	Negate with Carry Byte
NOP	No Operation
NOT	One's Complement
NOT.B	One's Complement Byte
OR	Logical Or
OR.B	Logical Or Byte
POP	Pop
POPM	Pop Multiple Registers
PUSH	Push
PUSHM	Push Multiple Registers
RET	Return from Subroutine
RETI	Return from Interrupt
ROL	Rotate Left
ROL.B	Rotate Left Byte
ROLC	Rotate Left through Carry
ROLC.B	Rotate Left through Carry Byte
ROR	Rotate Right
ROR.B	Rotate Right Byte
RORC	Rotate Right through Carry
RORC.B	Rotate Right through Carry Byte
SUB	Subtract
SUB.B	Subtract Byte
SUBC	Subtract with Carry
SUBC.B	Subtract with Carry Byte
TEST	Test
TEST.B	Test Byte
TESTN	Test Not
TESTN.B	Test Not Byte

TABLE 2

68200 Typical Instruction Execution Times

Instruction type	Clock periods	Execution time with 6-MHz clock (microseconds)
Move register to register	3	0.5
Add register to register (binary or BCD)	3	0.5
Move memory to register	6	1.0
Add register to memory	9	1.5
Multiply (16 x 16)	21	3.5
Divide (32/16)	23	3.84
Move multiple (save or restore all registers)	55	9.2

The 68200's nine addressing modes are similar to the 68000's, and the 68200 provides all but one of the address register indirect modes available on the 68000. The register indirect modes can be used with all of the address registers as well as with the stack pointer. These addressing modes support many common data structures, including arrays, stacks, queues, and linked lists. Two addressing modes, an index register indirect with displacement mode and a relative displacement with index mode, are present on the 68000 but are not implemented on the 68200.

However, the 68200's special I/O port addressing mode allows a fast, single-instruction word access to internal I/O ports. The 68200's relative displacement mode can accommodate an 8- or 12-bit field for efficient encoding of relative jump instructions. Similarly, its immediate mode can accommodate 4-, 8-, or 16-bit operands, which also provide efficient program memory utilization.

Many 68200 instructions bear the same mnemonic to aid the programmer familiar with the 68000 instruction set.

The 68200's instruction set incorporates a set of operations optimized for single-chip microcomputer applications. In addition, instructions are encoded to minimize code space, a feature that is especially important in single-chip microcomputers. Small code space is related to execution speed, and most instructions execute in either three or six clock periods. (A clock period is equal to 167 ns with a 6-MHz clock.) Table 2 shows instruction execution times for a number of typical instruction classes.

In addition to operations on bytes and words, the 68200 includes bit-manipulation instructions that can operate on both registers and memory. Bit manipulation is emphasized in the 68200 architecture to support I/O-intensive applications. The bit affected may be expressed as an immediate operand of the instruction, or may be dynamically specified in an address or data register. Operations available include bit set, clear, test, change, and exchange. Bit operations always perform a bit test as well.

The 68200 incorporates a bit exchange instruction (BEXG) that does not exist in the 68000. A bit operation instruction in the 68200 tests the destination bit and places it in the carry flag (C-bit) in the status register. The sign of the destination word is placed in the N-bit and the Z-bit is set if the destination word is zero. In the 68000, the destination bit is tested and the result's inverse is placed in the Z-bit, while all other bits in the status register remain unaffected.

To demonstrate the performance capabilities of the 68200, an example code segment is shown in Fig 5. This example is designed to illustrate the 68200 implementation of a linear scaling operation ($y = mx + b$) of a binary value with conversion of the scaled result to binary coded decimal (BCD). The binary value is a 12-bit number that is initially read from one of the 68200's parallel ports. This number could possibly originate from an external high resolution analog to digital converter that is interfaced to the 68200 port. The scaling that is performed uses a value of $m = 0.8$ and $b = -1784$. This 12-bit scaled result is converted into a 4-digit BCD number with sign.

In the programming example, the high speed multiply and divide instructions are used to perform the calculation of m times x. The 68000 supports multiply and divide instructions using several different addressing modes, while the 68200 only supports register direct addressing for these instructions. However, the 68200 executes these instructions very quickly: 21 clock periods for a 16 x 16 multiply and 23 clock periods for a 32/16 divide. The 68000 takes 70 to 86 clock cycles for a multiply, and 140 to 156 for a divide. Even though the 68000 is available in versions that operate at a much higher clock rate than the 68200, the 68200 can outperform it for these operations.

Another significant feature of the 68200, as brought out in the programming example, is the advanced BCD handling capabilities. The 68200 has a total of six instructions to handle BCD arithmetic. These allow either an 8- or 16-bit calculation using the carry bit as an option. The 68200 instruction Decimal Add (DADD) is used in the example to perform a 16-bit BCD addition. In comparison, the 68000 has only three instructions to handle BCD numbers. All of these instructions only operate on two 8-bit BCD values with the extend flag always used in the calculation. In order to implement a

```
Line S Loc  Value           Source

   1 0                      ; BENCHMARK:  SCALING AND BCD CONVERSION
   2 0                      ;
   3 0                      ; MACHINE:    MK68200
   4 0                      ; CLOCK RATE: 4 MHz
   5 0
   6 0                      ; REGISTERS:
   7 0                      ;  D0  BINARY VALUE       D2  BCDBIT_WEIGHT
   8 0                      ;  DL1 COUNTER            D3  BCD ACCUMULATOR
   9 0                      ;  DH1 SIGN NIBBLE
  10 0
  11 0                      ;
  12 0                      ;        SCALING OF 12 BIT VALUE: Y = M * X - B;  M = 0.8;  B = 1784
  13 0                      ;
  14 1      0001                    SECTION  1
  15 1                      SCAL62:
  16 1 0000 00B1                    MOVE     P1,D0              ; T=  6: INPUT 12 BIT BINARY VALUE
  17 1 0002 02970008                MOVE     #8,D2              ; T=  6
  18 1 0006 5290                    MULU     D2,D0              ; T= 21: MULTIPLY BY 8 AND THEN
  19 1 0008 EA0A                    MOVE.B   #10,DL2            ; T=  3: DIVIDE THE RESULT BY 10
  20 1 000A 52D0                    DIVU     D2,D0              ; T= 23: TO MULTIPLY BY M = 0.8.
  21 1 000C 20F706F8                SUB      #1784,D0           ; T=  6: SUBTRACT B = -1784
  22 1                      ;
  23 1 0010 E12B                    MOVE.B   #'+',DH1           ; T=  3: SET SIGN NIBBLE POSITIVE
  24 1 0012 8401                    JMPR     GE,L1              ; T=4/7: BRANCH IF >
  25 1 0014 37E0                    NEG      D0                 ; T=  3:
  26 1 0016 E12D                    MOVE.B   #'-',DH1           ; T=  3: SET SIGN NIBBLE NEGATIVE
  27 1                      ;
  28 1                      ;        CONVERSION OF BINARY VALUE TO BCD (4 DIGITS PLUS SIGN)
  29 1                      ;
  30 1 0018 E90C            L1:     MOVE.B   #12,DL1            ; T=  3: INIT COUNTER
  31 1 001A EA01                    MOVE.B   #1,DL2             ; T=  3: INIT BCDBIT_WEIGHT
  32 1 001C 13B7                    CLR      D3                 ; T=  3: INIT BCDACC
  33 1                      ;
  34 1 001E B0A1            L2:     ASR      D0                 ; T=  3: START BCD CONVERSION
  35 1 0020 8A00                    JMPR     CC,L3              ; T=4/7: TEST BIT
  36 1 0022 A3C2                    DADD     D2,D3              ; T=  3: BCDACC:=BCDADD+BCDBIT_WEIGHT
  37 1
  38 1 0024 A2C2            L3:     DADD     D2,D2              ; T=  3: BCDBIT_WEIGHT=2*BCDBIT_WEIGHT
  39 1 0026 9106                    DJNZ.B   DH1,L2             ; T=6/9: REPEAT LOOP UNTIL DONE
  40 1                      ;
  41 1 0028 1F83FB00                MOVE     D3,RESULT          ; T=  9: STORE RESULT IN MEMORY
  42 1 002C 1F02FB02                MOVE.B   DH2,SIGN           ; T=  9: STORE SIGN IN MEMORY
  43 1
  44        FB00                    ORG      $FB00
  45   FB00 0002            RESULT: DS       1                  ; START OF 68200 INTERNAL RAM
  46   FB02 0001            SIGN:   DS.B     1
  47                        ;
  48                        ;  SUMMARY:
  49                        ;          INSTRUCTIONS:          20
  50                        ;          BYTES                  47
  51                        ;          EXECUTION TIME (uS)    92.25 uS (WORST CASE)
  52        0000                    END
 no errors detected.
```

Fig 5 As coded for the 68200, this linear scaling programming example utilizes the high speed multiply and divide instructions, as well as the powerful BCD handling instructions. These operations are often required in high performance control applications.

68000 routine, which performs the BCD conversion shown in the programming example, the extend flag must first be initialized and two Add BCD (ABCD) instructions must be used to perform a single 16-bit BCD calculation.

The 68200 has an advanced architecture that supports features such as enhanced BCD and bit-manipulation instructions, fast multiply and divide instructions, compact instruction encoding, and fast access to I/O ports. Because of these features, the 68200 can significantly outperform other state-of-the-art microprocessors, including the 68000, in controller applications.

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CIRCLE 114

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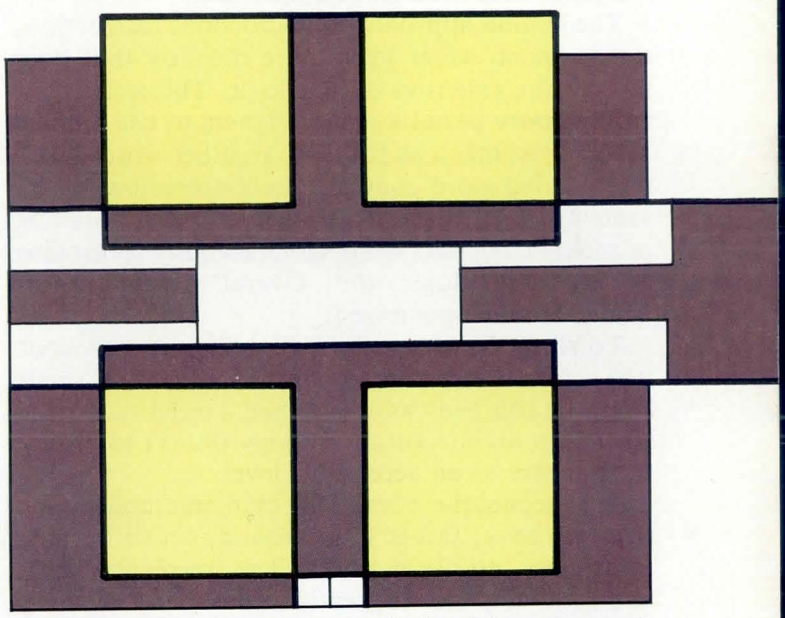
CIRCLE 115

MICROPROGRAMMING FOR THE MASSES

Microprogrammable, single-chip processors and their associated software tool kits are falling into the hands of designers. The result may be a revolution in instruction coding.

by Roy M. Matney, Andre Orban, and Tom M. Albers



For years, microcoding of custom instructions has been common in large computers incorporating writable control stores—and for good reason. Custom microcoded instructions execute at far greater speeds than assembly language sequences, thereby optimizing the processor for specific applications. Microcoding, however, is tedious and can be likened to brain surgery: the slightest error renders the entire organism incapable of executing any instructions at all. For this reason, among others, the science of microcoding has been limited to exotic hardware tended to by a select few.

Texas Instruments is changing this picture with its family of single-chip processors that are user microprogrammable. This feature is achieved by a package of support software and hardware that enables design engineers working on a microprocessor-based system to take advantage of custom instructions. It also eases system design by allowing programming, rather than costly hardware, to meet execution speed-related goals. The microprogramming of a custom TMS7000 chip accrues a 1-time cost while providing an elegant as well as economical solution to the performance price problem.

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Microcode defines an instruction set

The instruction set of a central processing unit (CPU) can be defined in one of two ways: by hardwired logic or by microcode. In the hardwired case, random logic gates are connected in a manner that determines actions required to execute an instruction. When using microcode, a set of microinstructions defines instruction sequences. These microinstructions are held in the control store memory which, on current microprocessors, is read only. Thus, if it were possible to program a different set of microinstructions into the control store, the processor's instruction set could be altered.

Traditionally, microprocessor control has been implemented in random logic instead of microcode. The microcode approach, however, is easier and faster and, since most of the logic is in read only memory (ROM), requires less silicon. The real advantage of microcoding is its flexibility and the inherent ease with which functionality can be increased. Indeed, the increasing complexity of very large scale integration chips has necessitated the move to microcoded architectures.

Two approaches to microcoded processors are available. In one case, designers can select a narrow width microstore memory and implement the opcodes in a lengthy sequential manner. This approach requires each data transfer to have its own microcode step. Thus, the microcode memory needs to be longer and the execution of each opcode becomes slower. Another penalty of narrow microcoded devices is the need for extensive decode logic to interface the output of this control memory to the gates that need to be controlled.

The second approach to microcoded instructions uses a much wider microstore memory that does not require extensive decode logic. This wider control memory permits chip designers to use parallel activities as much as possible. In other words, each microcoded word controls many operations at the same time. A typical example might be the loading of multiple registers while simultaneously controlling an arithmetic logic unit. Overall device performance is thus maximized.

To allow the integration of horizontal microcode (the wider micromemory approach) into a single chip, the company has developed a technique called strip chip architectural topology (SCAT) to reduce the bar size to an acceptable level.

This technique routes all chip interconnection circuitry over, rather than around, active devices. In this way, no silicon is wasted on interconnections, and total chip size is greatly reduced. All memory elements, such as chip registers, are aligned vertically so that a single set of straight data lines can be run over them, while all control lines are aligned horizontally alongside the control read only memory (ROM) that activates them. This technique makes maximum use of available silicon.

Moreover, the SCAT structure of the chip allows parallel operations to be performed simultaneously. To maximize parallel operations and increase speed, horizontal control stores have also been implemented.

There is one bit in the control ROM word for each function to be controlled in the horizontal architecture of this family of chips. For example, a single bit controls the loading of the instruction register or the gating of a specified register onto a designated internal bus. Obviously, the horizontal store consumes more silicon; however, any of the internal source registers can be strobed simultaneously—

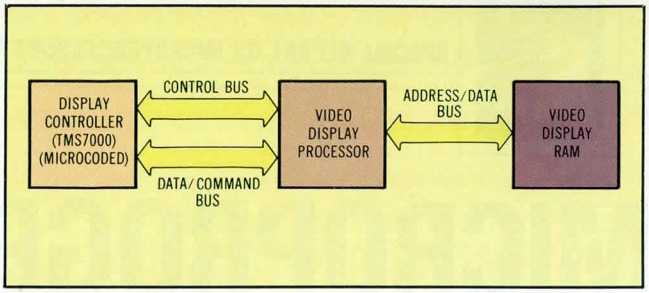

Fig 1 The display controller/video display processor interface illustrates how user written microcode helps simplify the problem of display control. Streamlined code capable of simultaneously controlling several functions optimizes the control process.

something that is impossible with the vertically encoded control store. For instance, if three registers are to receive the same value, it would take three operations with the vertically encoded store, but only one with the horizontal store. Also, the vertical store requires decoders near the registers to interpret their encoded fields. These decoders slow down the execution speed of vertically encoded machines even further. In the TMS7000, a 45-bit wide horizontal control ROM is required to control every device function.

Adding special instructions

User microcoded machines allow new instructions to be added to the standard set. Almost every system has some high speed aspect that the microprocessor cannot serve without external latches and other logic. With a microprogrammable part, however, a special instruction can be added to the basic repertoire to satisfy that need without external hardware.

A user defined microinstruction can execute up to 10 times faster than an equivalent assembly language sequence, since users specify the exact sequence of operations to perform a certain function. In this way, users can take advantage of all the parallel operations that can be performed to execute a function quickly. For instance, each internal bus can be used to carry out many parallel data transfers simultaneously.

One advantage of the inherent speed of a horizontally encoded control store is in the interface protocols among the system elements. Controllers for printers, tape drives, and video displays all require intricate bit patterns. The speed at which these control words can be sent often determines the speed of the system. Sometimes it takes several assembly language instructions to perform the mask operations required to compose these intricate control codes. On the other hand, just one user defined microcoded instruction can perform the same job.

Typically, system designers determine the operations that are most often used, yet difficult to perform, for a particular application. New designers

can add custom microinstructions to perform them. Custom instructions can also reduce costs for applications requiring very fast response to external signals. Rather than add special purpose hardware to service an external input, a special instruction can be added to service the external input in microcode rather than assembly language. This situation is analogous to dropping into assembly language from Basic to perform some time-critical task like sorting.

Microprocessing system designers now have another level to drop to when even greater speed is required. This solution involves a 1-time tooling cost to implement the custom instructions, rather than the cumulative cost of special purpose hardware. It further improves on existing approaches since microcode cannot be easily read or copied.

Microcoded solutions

An operation that produces a 100-bit pulse train illustrates the speed that can be gained by using microcode. In assembly language, this requires sending an output to a port, waiting, sending the inverted bit to the port, and then looping 100 times. Such an operation requires at least three instructions and all the associated overhead incurred fetching them from memory. In microcode, a single instruction can be custom tailored to perform the same task. That is all it will do, but it will do it about 15 times faster.

On the system level, a similar example is the optimization of the interface between a TMS7000 computer, functioning as a display controller (DC), and a video display processor (VDP). In this example, the display controller is used to control the display operation of the VDP through a 3-line control bus and an 8-line data command bus (Fig 1). The VDP, in turn, uses an 8-bit address data bus to communicate with its video display random access memory (VD-RAM). The latter bus interface is optimized and operates in a speed-efficient manner.

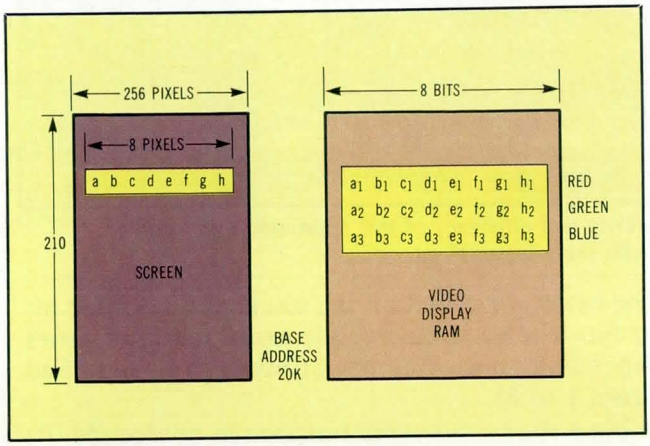

Fig 2 Video display RAM to screen mapping uses 3 bytes to represent 8 pixels. The RMOD instruction allows 1 bit in each byte to be modified for a color change. The R,G,B bits define colors in VD-RAM.

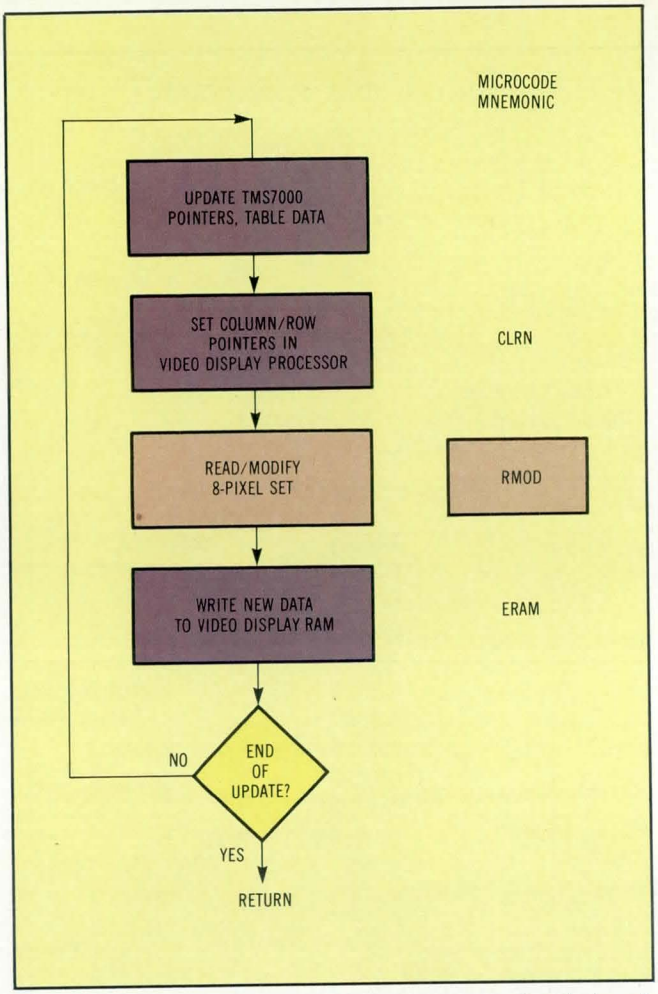

Fig 3 Software flow during a typical screen update is based upon three instructions: CLRN, RMOD, and ERAM. The objective is to vertically map 3 color bits into pixel definition bytes.

However, the DC/VDP interface is complicated by the control bus structure that the VDP requires. Obviously, this is a case for microcoding.

As stated, the display controller must communicate to the VD-RAM through the VDP. Hence, reads and writes of these data (and screen updates) are very speed dependent. The visual effect of slow throughput can be devastating. As shown in Fig 2, 3 bytes of VD-RAM are used to define each set of 8 pixels. The display controller can only access these through the VDP. Hence, to change a particular pixel without altering the surrounding pixels, 3 bytes must be read and 1 bit in each of the 3 bytes modified. For example, if users wish to change pixel "f," bits f_1, f_2, and f_3 must be modified to the new color "code." This is the read/modify portion (RMOD) of a screen update. Before this action, the display controller must "point to" the 3 bytes. This is done by the column/row microinstruction (CLRN). After the RMOD execution, the 3 altered bytes must be written back to the VD-RAM through the VDP, executed by write to RAM (ERAM). This flow is illustrated in Fig 3, which also describes the overall flow for a screen update.

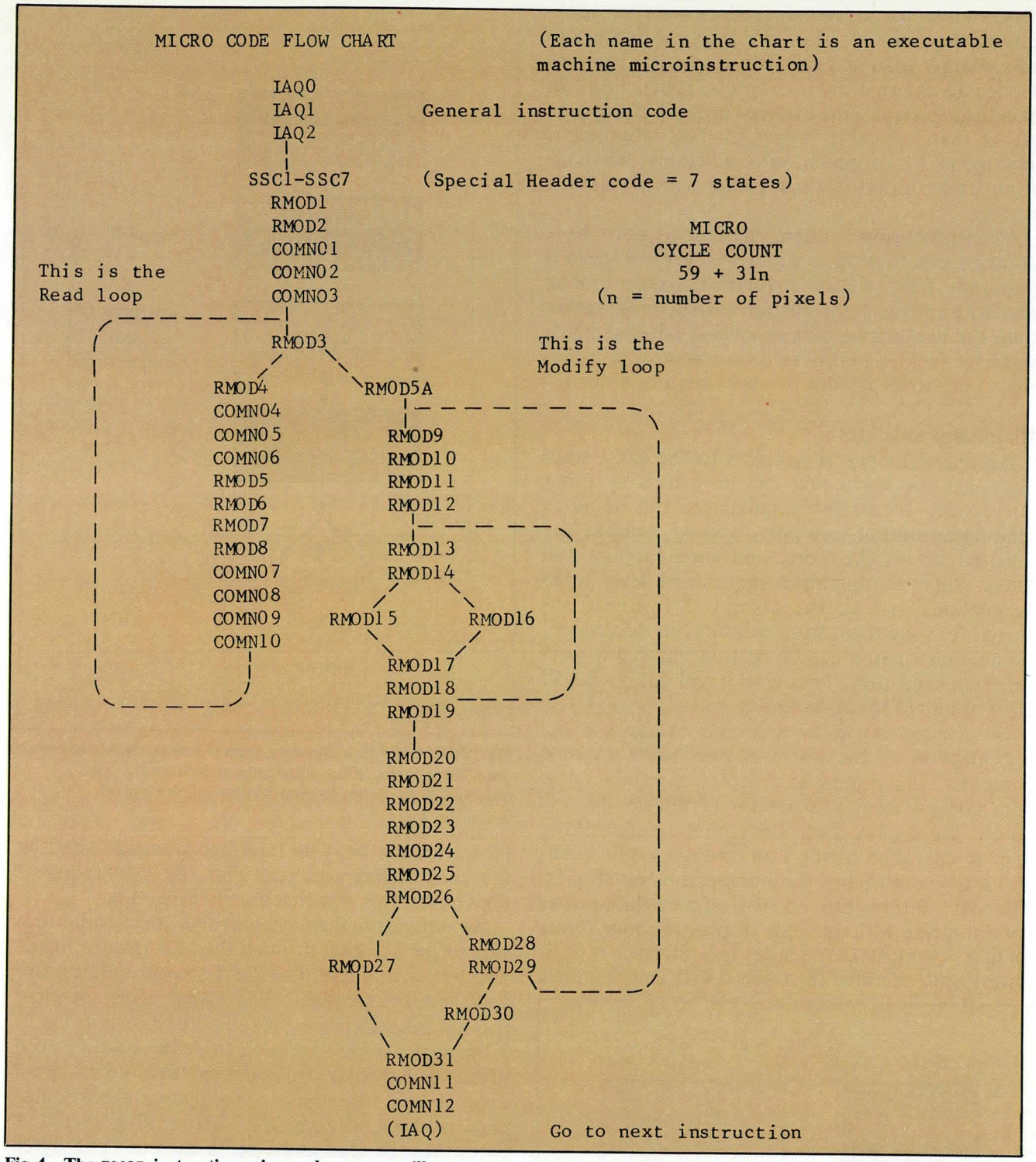

Fig 4 The RMOD instruction microcode sequence illustrates the brevity and efficiency of this approach. This code consumes only 50 control ROM locations, 19 of which are shared with other instructions.

Of the three routines (RMOD, CLRN, and ERAM), RMOD provides the greatest speed increase. The assembly language code necessary to read 3 bytes of the VD-RAM, and then modify them according to control information, would require about 40 lines of code. Basically, a 3-bit color value must be mapped vertically into the 3 bytes that together define the pixel. A mask points to each bit while two other masks set and reset bits in the 3 bytes. The bytes are stored on the stack and modified bit by bit. The total macrocode execution time varies depending on the number of pixels to be modified (from 1 to 8).

Fig 4 shows this same function in microcode. Its functional execution basically corresponds to the assembly language source, but is executed much more efficiently. Further, it optimizes the power of the CPU, something general assembly language

statements cannot do. The common code statements (COMN01-COMN12) are shaped with the other microcoded routines (such as CLRN and ERAM), exhibiting the versatility of microcode. This routine executes up to eight times faster than assembly language, and uses less ROM space.

The Table "Macro Micro Comparison," compares the ROM usage, the total machine cycles, and the resultant execution speed of the microcode and macrocode routines. For this routine, the improvement is overwhelming. The ROM usage is superior by 59 to 1, a critical measure for tightly packed code. Execution speed, based on machine cycles executed, ranges from five to almost eight times better for the microcoded sequence. This is because a complex routine, requring extensive CPU usage, can optimize the display controller's microcoded architecture effectively. The microcode also optimizes the peripheral point's usage input/output to satisfy the VDP's complex interfacing protocol.

Macro Micro Comparison

	Code level: Macro	Micro	Relative performance
ROM bytes used	60	1	60
Machine cycles required	183 x 281n	59 x 31n	See below
Time required at 5MHz	73.2 + 112.4n	23.6 + 12.4n	See below

(a)

Value of n, number of pixels modified					
Cycle count	1	2	4	6	8
Macro	464	745	1307	1869	2431
Micro	90	121	183	245	307
Execution speed (microseconds)					
Macro	185.6	298.0	522.8	747.6	972.4
Micro	36.0	48.4	73.2	98.0	122.8
Relative performance					
Ratio	5.2	6.2	7.1	7.6	7.9

(b)

Development tools simplify microcoding

There are special problems associated with designing microcode software development tools, especially for horizontally encoded machines like the TMS7000. With wide control stores, such as 45 bits, conditions arise that have no equivalents in standard assembly level situations. Parallel operations that produce conflicts must be avoided while maximizing legal parallel operations. For instance, no two line drivers for the same data path can be simultaneously active. However, as many input registers as desired, which require data from that path, can be strobed simultaneously.

In vertical machines, the encoded microcode fields and their associated decoders and multiplexers prevent bus contention. Thus, vertically encoded machines present fewer bus contention problems and allow users merely to specify source and destination registers for an operation, as in a normal assembly process.

For the TMS7000, however, anything can happen in parallel, and all 45 bits of each microcode word must be carefully checked for contention problems. Normal software development tools do not handle the problem presented by bus contentions due to concurrent activities occurring at the microcode level.

For these reasons, the company has developed an integrated hardware/software microcode development package (Fig 5) that works in conjunction with its development systems. The hardware consists of a special emulator that can reconfigure itself to execute the new user defined micro opcodes. The output of the micro assembler is downloaded into the emulator where new instructions can then be tested in the target system hardware. This special emulator holds the new instructions in a fast RAM control store that functionally duplicates the control ROM in a production device.

The micro assembler (MICASM) augments the standard tools normally available for microprocessor software development. MICASM is written in Pascal and is designed to run on any hard disk TI minicomputer. It divides the micro assembly task into three phases: definition, assembly, and formatting.

In phase 1, users employ the standard definition file that consists of a mnemonic definition, conflict, and inclusion statements. The definitions file also includes a control-signal description that gives an overview of the relationship between particular mnemonics and the bits that they affect. This information is used for references as well as for decoding MICASM-generated control ROM words. The mnemonic definition part of the file is fixed for the type of processor being used (in this case, the TMS7000), since those mnemonics refer to the particular architectural features of the processor.

Similarly, conflict statements are specific to the architectural features of the processor. They specify the mnemonics that cannot be coded

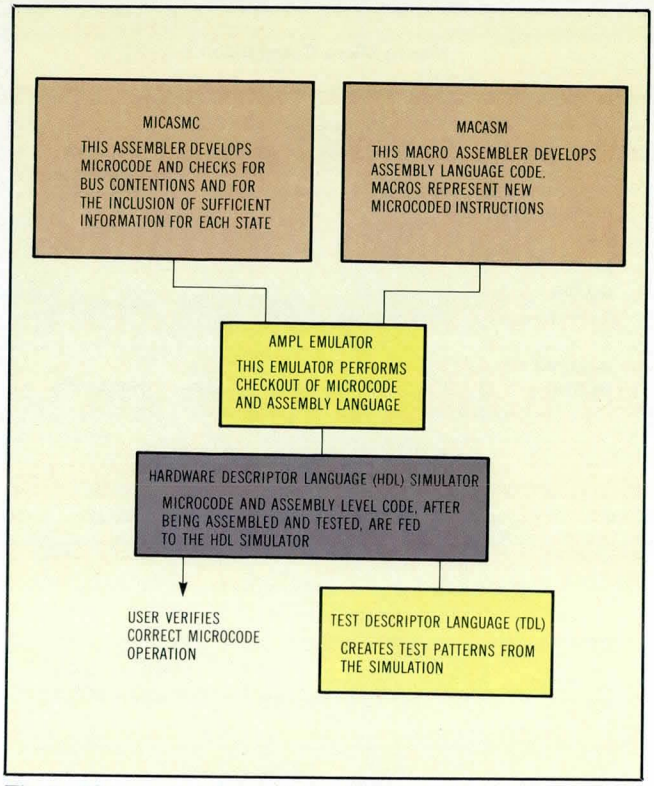

Fig 5 The user's microcode tool kit includes a microcode assembler, a macro assembly language assembler, an emulator, a simulator, and a test pattern generation utility.

together in a single microinstruction. In addition, they prevent the micro assembler from creating contention on buses due to multiple sources for a single destination, and multiple destinations from a single source (when the latter is architecturally impossible).

Conflict statements are used together with inclusion statements that define specific strings of mnemonics, one of which must be included in each microinstruction. The inclusion statement guarantees that each state is completely defined—ie, a source, destination, and function are specified for each machine state. Together, they ensure that an optimal solution to the microcoding problem will be found.

After microcode mnemonics have been fully defined, the assembly phase consists of using those definitions to convert a user's source file into a microcode object file. The formatting phase then converts the object file into a modular form useful for reference by designers. It also appends the file to a full micro assembly listing. Here, address data word pairs are given in a tabular form in the same order in which they were defined in the source code.

Adding to the standard set

The standard instruction set on a display controller uses the entire 160-word control ROM. About 25% of control ROM can be redefined by users to create new instructions. To assist users further, the standard microinstructions are documented so that their mechanisms can be used to minimize the amount of control ROM required. For instance, determining the addresses of operands and fetching them can all be done by existing microcode subroutines. Users simply add the special arithmetic/logic operations required for a specific application. In this way, a typical user can add up to 20 new instructions to the core set of 160 instructions. In applications requiring a large number of custom instructions, it is possible to identify more unneeded instructions. It is even possible for users to define a completely unique instruction set. Most users, however, choose merely to modify the standard set.

The future promises an expansion of programmable control store ROMs as well as software tool choices. Simulators and automatic test pattern generators are two additions that can be expected very soon.

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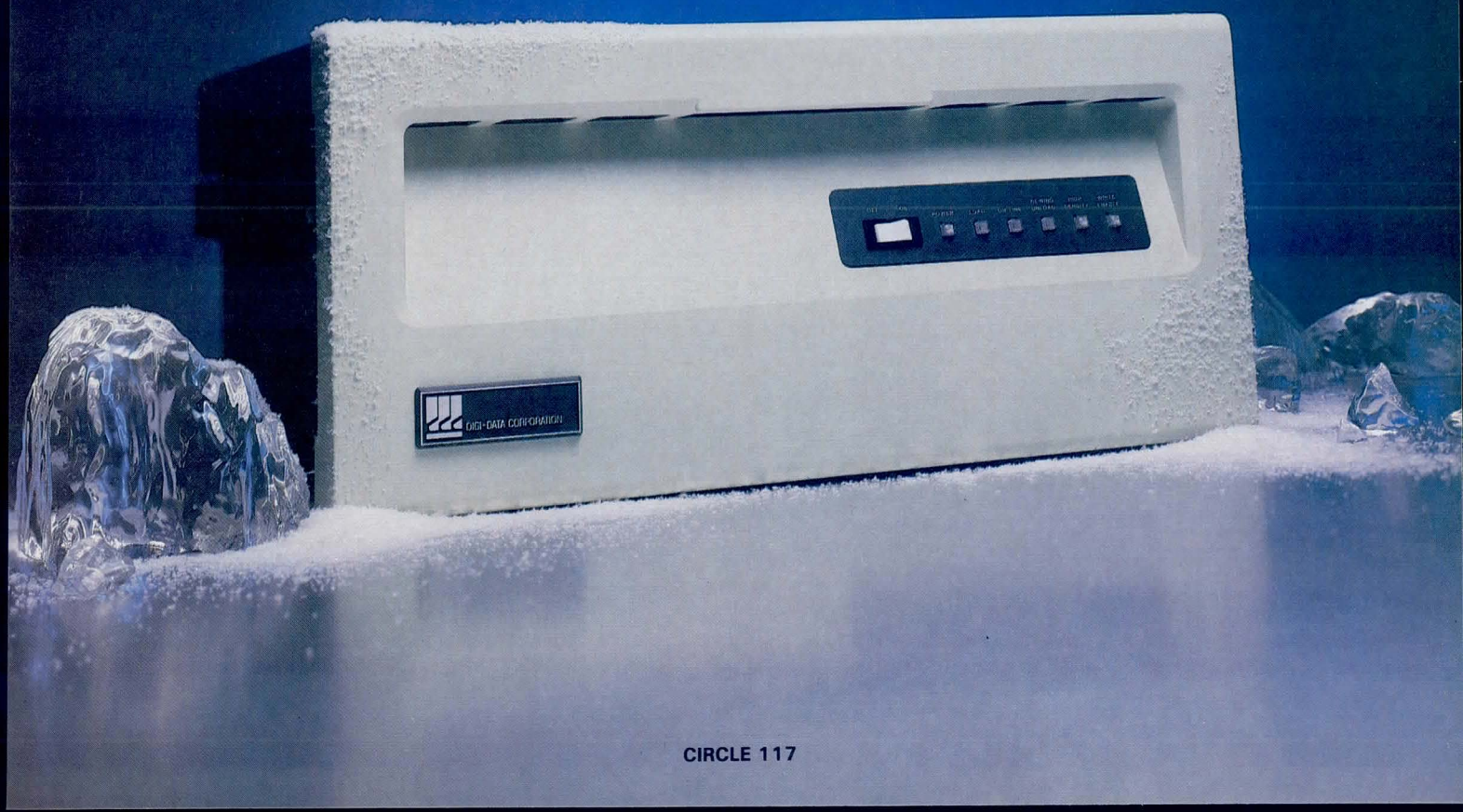

CIRCLE 117

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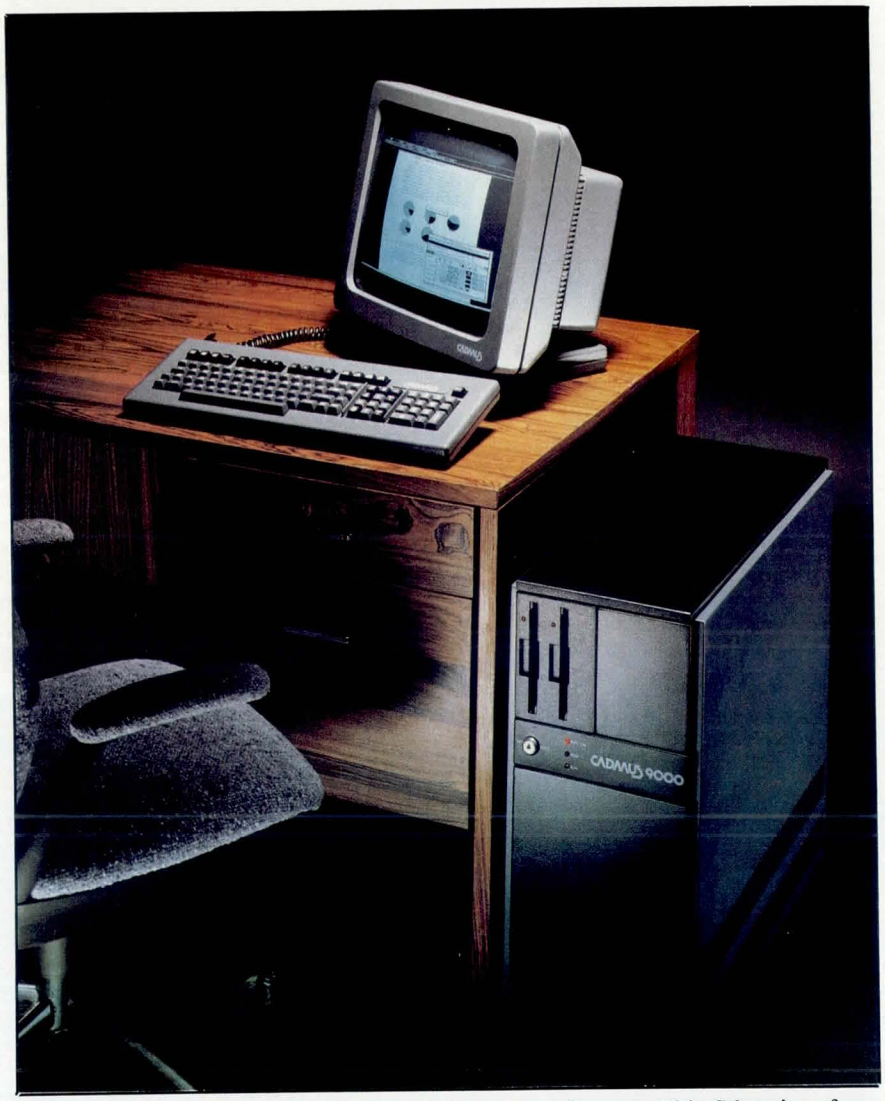
CIRCLE 118

Workstation connects 16/32-bit micro power to Unix and graphics



Cadmus 9790 ties microprocessor capability, the Unix operating system, and high resolution graphics together in an advanced function workstation. Based on the 16/32-bit MC68000 (68010), the central processor is supported by a discrete memory management unit (MMU) using a 2-step implementation. The MMU performs address translation, enforces access protection, and provides support for demand-paged virtual memory. A 10-MHz clock speed allows the processor to run computation-intensive applications. Processor onboard memory consists of 8K bytes of ROM with standalone boot, monitor/debugger, and 4K bytes of scratchpad RAM.

The system bus structure encompasses a Q-bus compatible backplane bus, and an S-bus that acts as a proprietary memory channel. This S-bus interfaces with dual-port memory cards via two 40-connector ribbon cables and allows main memory access to take place at full processor speed without Q-bus intervention. Through Q-bus flexibility, the workstation system has expansion room in the card cage and free positions for 5¼" peripherals. The arrangement of signals on the Q-bus permits full-width and half-width modules to be intermixed for a more compact, economical system.

The workstation's graphics terminal features a 1024 x 1024 addressable resolution and a 1024 x 800 displayed resolution. Graphic processing is supported by a hardware raster mechanism that allows construction, modification, and duplication of graphic primitives and complex symbols. This display method transfers bit blocks in which pixel rectangles are moved to and from any position in the video, program, or disk memories.

During the transfer, all binary combinations of source and destination pixels are performed. A word-addressing scheme permits transfers from the frame buffer or other memory. The display itself is a 17" monochrome device with a tilt and swivel base and a mouse interface. Cursor controls and function keys are the main features of the display's detachable keyboard.

Main memory specifications are based on the dual-ported architecture with Q-bus and S-bus contentions handled onboard. Memory capacity per board is 512K bytes of dynamic RAM with parity protection. Maximum memory per system is 4M bytes.

Additional memory is available in the Winchester disk subsystem. The 5¼" fixed drive has a 62.04M-byte formatted capacity and a 30-ms average access time. The recording medium is metallic film plated on a 130-mm diameter aluminum substrate, while recording heads are Whitney-type minicomposite ferrite read/write heads. The subsystem features a dedicated head landing/shipping zone at power off, a rotary voice coil actuator, and a closed-loop track-following servo system. An ST-560/412 type interface provides a 5M-bps transfer rate.

Using the Unix Version 7/System III operating system, the workstation contributes additional utilities with the Berkeley and Cadmus enhancements. Unix supplies a hierarchical file structure, a consistent method of device access, and a customizable user interface. Available third-party software packages include database, spreadsheet, word processing, and CAE capabilities, as well as development tools such as language compilers and an application generator.

Expansion options include a Multibus adapter and card cage, floating point processor, and an array processor. Also available are an Ethernet (for resource sharing), high performance (50M bps) fiber optic LAN, and a 20M-byte streaming cartridge tape and controller.

The system typically requires 600 W of power. Line voltage is 115 Vac (±10%) or 230 Vac (±10%) with a line frequency of 48 to 62 Hz. The 9790 system is priced at $17,900. **Cadmus Computer Systems,** 600 Suffolk St, Lowell, MA 01854.

Circle 260

System plays dual role in control and development

EXORset 110 provides users with dual capacity. First, the desktop system can be used as a controller in a variety of automation and data acquisition applications. Second, it allows major microprocessor developments to take place efficiently.

The controller uses an MC6809 16/8-bit microprocessor. This micro has an extended instruction set and addressing modes and an architecture that allows efficient software execution. In addition, structured programming, position-independent code, reentrant routines, and realtime operations make the processor suitable for high level language program development.

Three versions of mass storage are offered: no floppy disk drives, one double-sided minifloppy disk drive for 160K bytes, and two disk drives for 320K bytes. All three versions include 2K bytes of dynamic RAM for CRT character refresh, 56K bytes of dynamic RAM, and three strappable sockets. The sockets are set for 1K, 2K, 4K, or 8K ROMs or EPROMs. A fourth socket can be set up for a user-defined monitor routine.

EXORset provides three inboard I/O ports. An asynchronous serial communication port has a strap-selectable interface option (RS-232-C, RS-422, or RS-423) and can be configured as a terminal or a modem. The software programmable baud rate is

110 to 19.2k baud. The parallel I/O consists of a 16-bit data control line plus four handshake control lines. It has a buffered PIA device with a Centronics printer-compatible interface.

The system serves as an integration center for hardware/software development. A communication link with the HDS-200 allows emulation for the M6805 and M146805 families. In this mode, the device acts as a host and terminal. Programs are downloaded into the development station so that the EXORset is free for other software development tasks.

Moreover, the EXORbug monitor can be located anywhere in the memory map. Its debugging capabilities include memory read and change, memory block move, search for 8- or 16-bit patterns, and traces. In addition, hardware breakpoints can be set (up to 4096 within a 4K-byte address range) with realtime execution between breakpoints. The monitor also performs screen, terminal, and printer functions.

A 4-slot cage with bus connectors allows the system to expand through the use of EXORbus-compatible modules. The EXORset 110 pricing in quantities of one to five is $5900. This includes the X-DOS operating system, CRT editor, 6809 macro assembler, and a complete set of user guides. **Motorola Semiconductor Products, Inc,** PO Box 20912, Phoenix, AZ 85036. **Circle 261**

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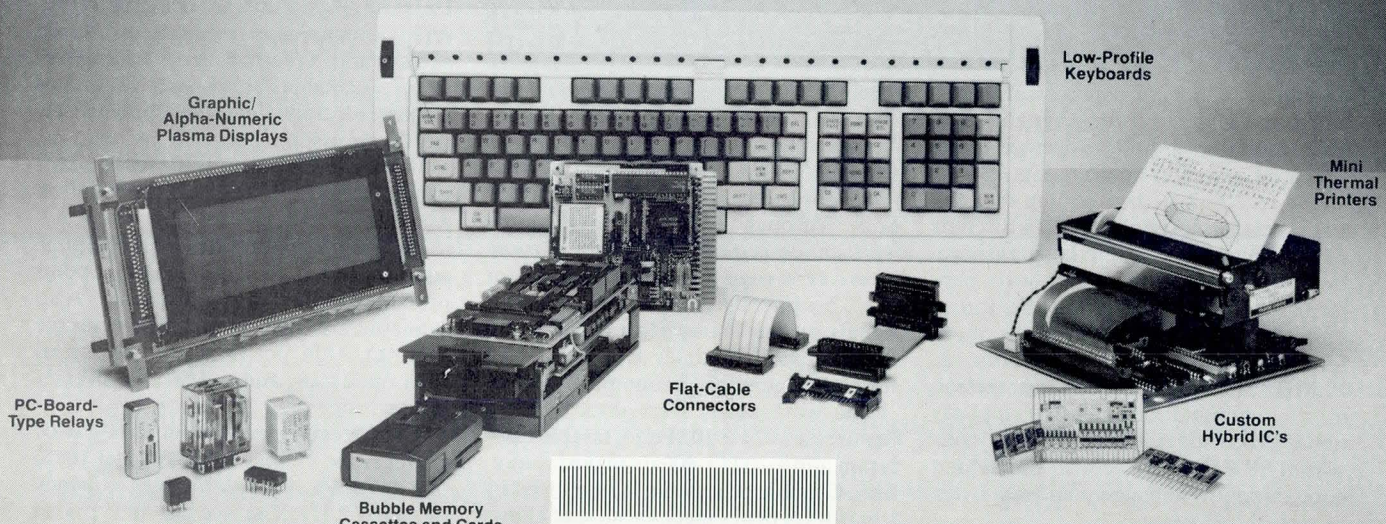

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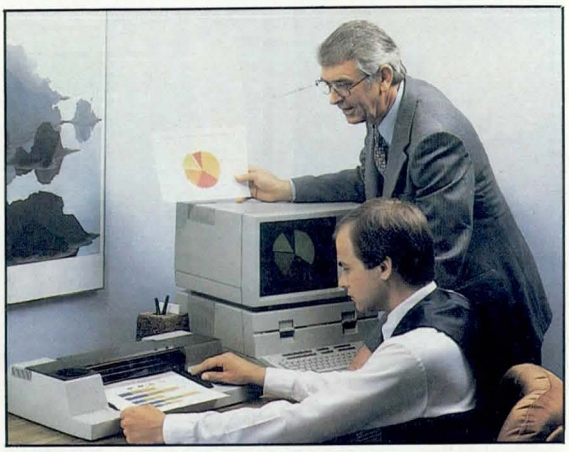
Plotter draws up graphics for small-computer workstations

Because of their usefulness in analyzing and presenting information, plotters have become essential peripherals for small-computer workstations. The HP 7475A plotter was specifically designed to meet the needs of low cost graphics in small-computer systems.

Interface flexibility is provided. Two interfaces can be specified: HP-IB, which is an enhanced version of the IEEE 488 bus; or RS-232-C, which provides plotter compatibility with small computers from Hewlett-Packard, IBM, Apple, DEC, Commodore, Compaq, and others. As an option (when using the RS-232-C interface), an eavesdrop cable allows the plotter to operate in series with a terminal, thereby using only one serial port.

Pens are selected by front-panel controls or program commands. A pen-velocity command is available for special drawing conditions; a "view" mode stops operation for review of the plot; and a rotating feature allows horizontal charts to be formatted vertically. When the pens are returned to the 6-pen carousel, they are automatically capped to prevent them from drying out. A variety of pen widths and colors is available.



Several software houses supply plotter software for users who do not want to do their own programming. However, the plotter contains more than 50 Hewlett-Packard graphics language commands. These commands cover pen movement, character selection, area fill, and scrolling. There are 19 character sets including ISO European standards and Katakana.

Acceptable media sizes include two ANSI sizes, A (8½" x 11") and B (11" x 17"); and two ISO sizes, A4 (210 x 297 mm) and A3 (297 x 420 mm). The plotter accepts overhead transparency film.

Multicolor pie, bar, line, and text charts are produced with high line quality. This line quality results from a 0.001" (0.025-mm) resolution. The plotter draws at speeds of 15 ips (38.1 cm/s) with a 2-g pen acceleration. Each velocity axis is programmable from 1 to 38 cm/s in 1-cm/s increments.

The plotter requires minimal space. Its dimensions are 22.4" x 14.5" x 5" (568 x 367 x 127 mm). The HP 7475A is priced at $1895 and delivery is estimated at stock to two weeks ARO. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 262**

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CIRCLE 119

Graphics processor contributes roam, zoom, and high resolution

Using three microprocessors and a dual-ported architecture, Telesis Systems Corp's graphics processor produces picture resolutions up to 2000 x 1000 pixels. Several processor functions allow high performance processing in CAD/CAM systems.

Advanced processor functions are controlled through a proprietary "function screen." The function screen replaces the conventional array of I/O devices, computer languages, and menu codes with a single user friendly device. English commands step the operator through design steps with an interactive approach.

The "roam" function allows the user to scan through a stored picture. This function is accessible in two modes. The first is the "joystick" mode where the function screen takes on the characteristics of a velocity joystick. By using a lightpen, the user can roam the picture with a speed related to the displacement from the initial point on the screen. Therefore, the farther away one moves the lightpen from its starting point, the faster the picture will move.

Second, the "natural" roam mode allows the designer to work normally on the portion of a picture that is currently displayed. When the cursor is moved to the outer edges of the screen, the system automatically detects the limit and moves the picture in the appropriate direction.

Zoom control enables the designer to magnify picture size in increments of one, two, or four times. The designer can then focus on a particular section of the design for detailed editing. All functions and features are reentrant so that changes made in the zoom mode are automatically updated.

World window allows the designer to switch from a view of an entire schematic or board design to a portion stored in the picture space. The switch occurs in less than 0.5 s, and synchronization is maintained between both representations. Window area can be increased or decreased at will, and the window portion is highlighted for visual verification.

There are two forms of cursor control. The system uses a full-screen vertical and horizontal crosshair to pinpoint the present cursor position. In addition, a dynamic cursor allows a symbol, a string of text, or a portion of a drawing to become the cursor. Once the cursor is chosen, it can be moved, in real time, to any desired location on the screen. No restrictions are placed on the dynamic cursor's size.

Implemented with a pipeline architecture, the system uses an 8-MHz 68000 (the 8085) and the NEC 7220 graphics processor. Dual-ported memory and an optimizing cross compiler allow graphics software from the first-generation system to be downloaded to the 68000 for faster execution times. The 68000 also accesses data stored in pages on a Winchester disk, processes the data, then passes the data to the 7220 processor. The graphics processor is priced at $7500. **Telesis Systems Corp,** 21 Alpha Rd, Chelmsford, MA 01824.
Circle 263

Microprocessor development system puts the VAX into service

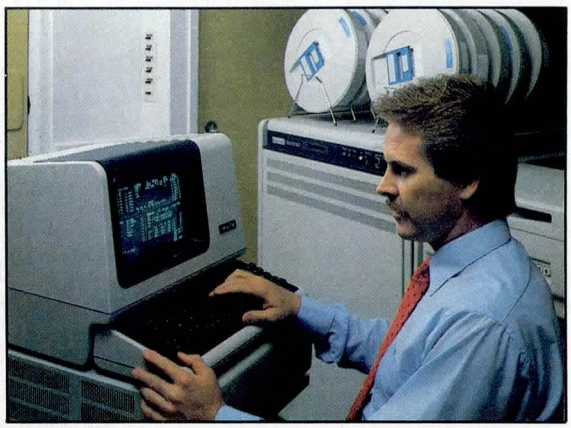
EMUNET-2 is based on DEC's VAX, a 32-bit minicomputer that uses the VMS operating system. This microprocessor development system is host independent, enabling it to work with any VAX—either the 11/730, the 11/750, or the 11/780—with easy migration from one model to the next.

The system supports up to 60 hardware/software workstations at distances of up to 5000 ' from the host. The modified ECL-3211 standalone systems are linked to the VAX via coaxial cable data links. All software-only stations are connected to the VAX via RS-232 lines. Each ECL-3211 workstation has its own DEC LSI-11 CPU. As a result, no individual workstation places a significant load on the host during emulation or "local" operation. The workstation arrangement can easily change as each multidrop data link accommodates up to 15 hardware/software workstations. In addition, four links of this kind can be used in one system. Data transfers between the host and the workstations occur at rates of 1M baud.

A virtual disk architecture gives each workstation transparent access to the mass storage available on the VAX. Using the virtual disk process allows increased product coordination and software version control with no loss of realtime response.

EMUNET-2 is both hardware and software compatible with the standalone ECL-3211 and the previously announced EMUNET-1. Because the hardware and software are directly transportable from the low end to the high end, users can start with a small system and easily expand to a larger one without losing their initial investment.

A typical EMUNET-2 system consisting of six satellite hardware/software workstations in addition to six software-only stations is priced from $110,000 to



$160,000. However, this price does not include a customer-supplied VAX. Additional hardware/software stations are priced between $18,000 and $25,000. Delivery is 30 to 60 days ARO with complete specifications. **Emulogic Inc,** 3 Technology Way, Norwood, MA 02062.
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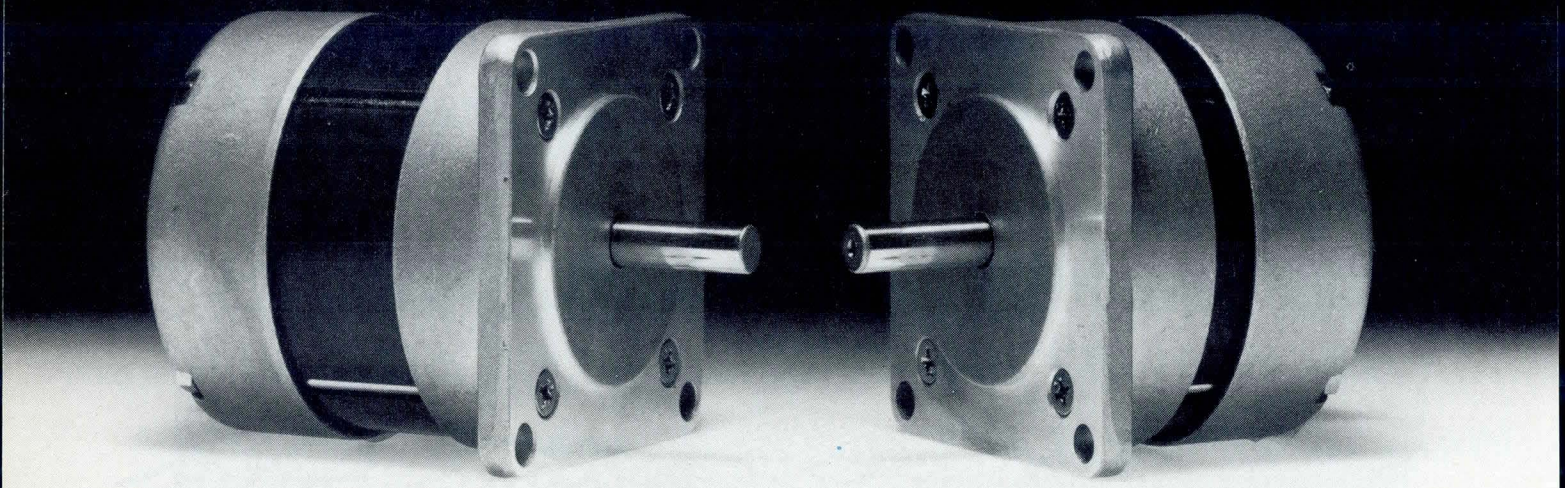

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CIRCLE 121

Color display oscilloscope incorporates liquid crystal shutter

The 5116 introduces color to the 5000 series oscilloscope line. Coupled with the 5D10 waveform digitizer, which contains necessary source signals to operate the color shutter, the scope becomes a liquid crystal color shutter display with digital storage.

A proprietary liquid crystal color shutter technology uses a single frequency material in an optical switch called a π cell. This cell offers millisecond switching rates and eliminates the higher power, complex drive circuitry, undesirable temperature effects, and poor viewing angle of the 2-frequency switches.

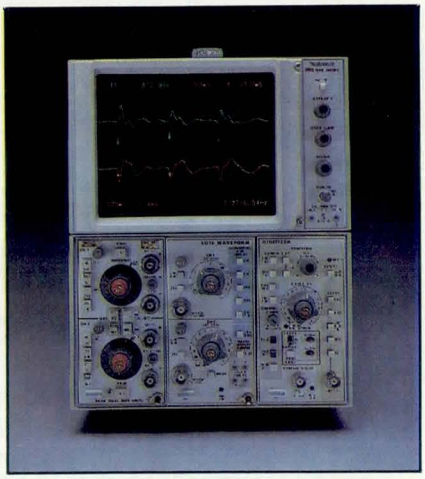
In the π cell, the fast switching time is achieved by the liquid crystal molecular arrangement. When an electric field is turned off, the necessary liquid aligns with the elastically induced rotation of the liquid crystal molecules. This alignment (plus thin cell spacing) results in fast cell switching.

The shutter-CRT system is created by mounting a fast liquid crystal color shutter in front of a monochrome CRT. The color shutter contains the π cell sandwiched between two orthogonal color polarizers and a neutral polarizer. Switch polarization determines which phosphor peak will be transmitted. Two sequential fields feed the transmitted information to the CRT, all synchronized with the shutter. The two primary colors are combined and appear this way to the eye.

Color images (consisting of two primary fields) must be presented at a 60-Hz rate to prevent flicker. As a result, the field rate must be 120 Hz for the entire image display. In the 5116, the color shutter must switch in less than 3 ms for adequate active display time for each color.

The 5D10 waveform digitizer plugs into all 5000 series scopes, transforming 5000 series mainframes into digital storage scopes. The digitizer stores transient events with frequency components up to 100 kHz (single-channel acquisition) and 50 kHz (dual-channel acquisition). Vertical resolution is 8 bits with 1024 data points. Accompanying digital readouts provide 1% accuracy both vertically and horizontally.

Color traces act as coding devices to separate or emphasize information, enhance pattern recognition, and improve



the user interface. Alphanumeric readouts are color coded by channel, while X-Y and time measurements appear in neutral. Channel 1 data are blue-green and channel 2 data are orange; voltage measurements are color coded by channel.

The 5116 mainframe is priced at $2335 and the 5D10 digitizer is priced at $2850. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077. **Circle 265**

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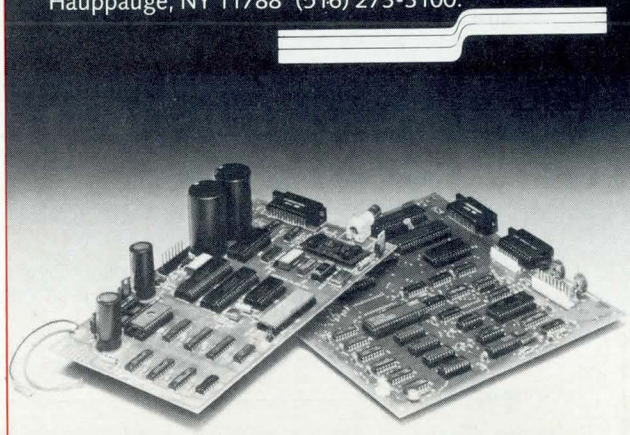

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CIRCLE 165

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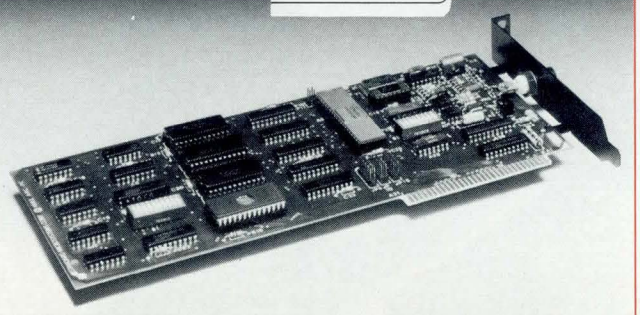

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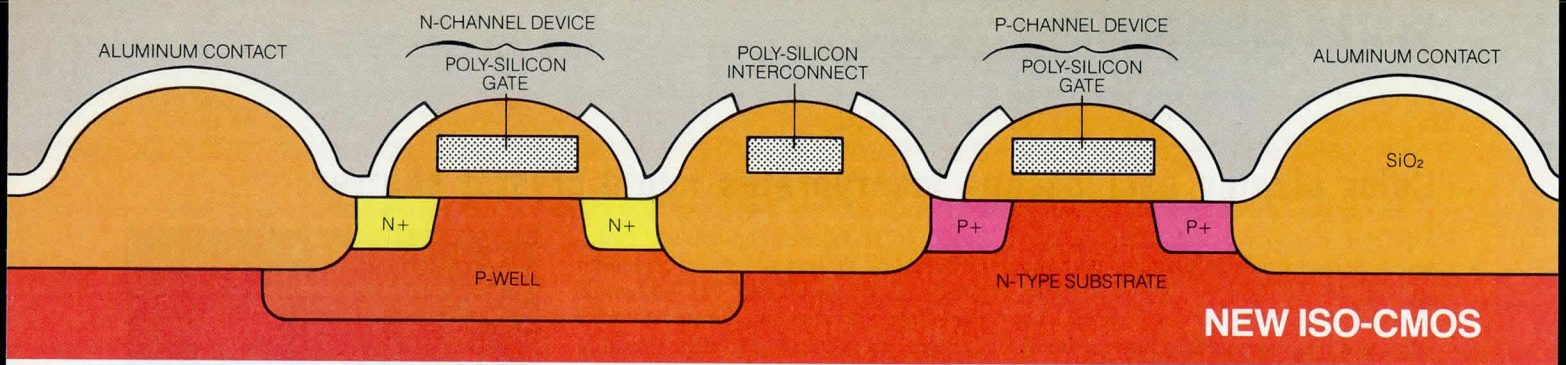

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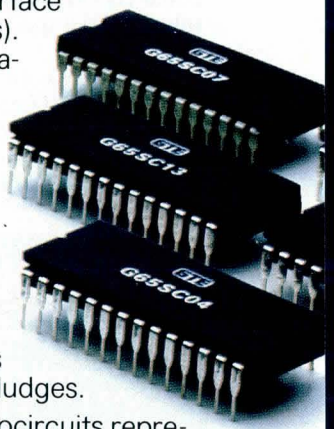

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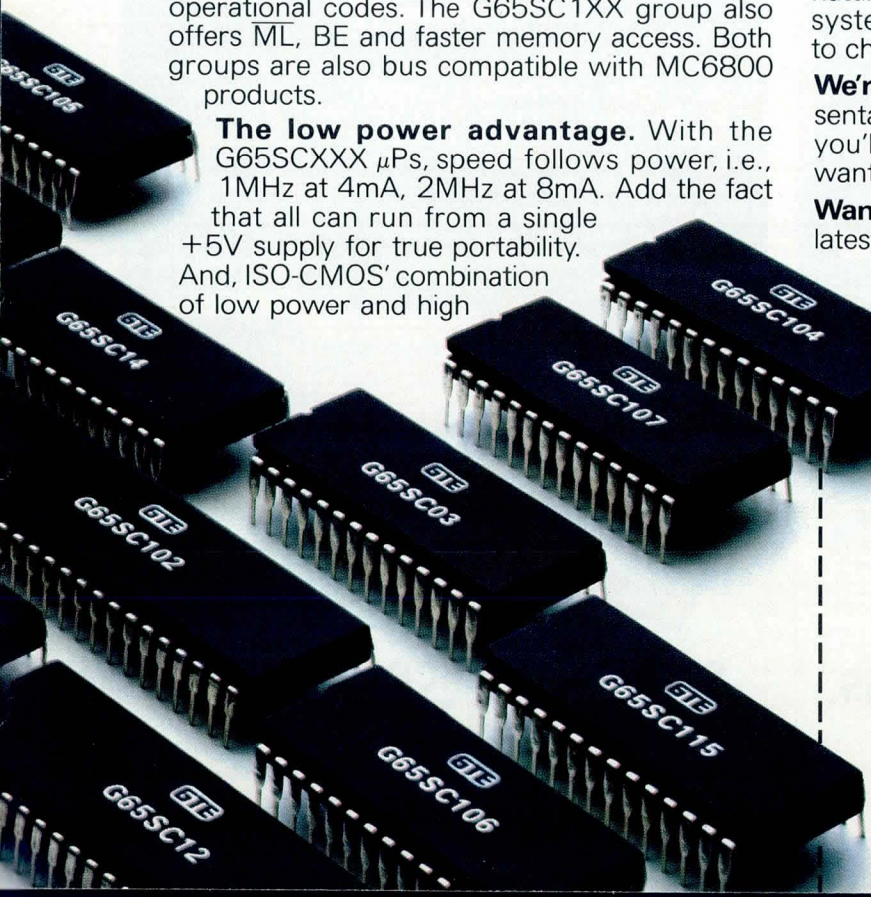

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CIRCLE 123

Op amps display increased performance

The 200 series of operational amplifiers are versatile devices with a multitude of applications. The three amplifiers in the series (CLC200, CLC210, and CLC220) have application areas that include digital and wideband analog communications, data conversion and acquisition, fiber optics, radar, and navigation.

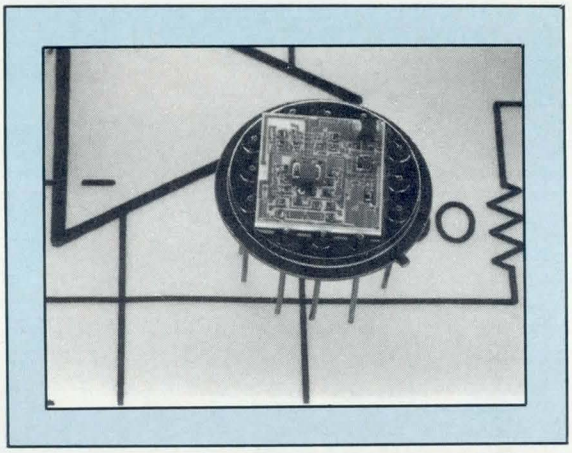
Various specifications of the CLC200 allow a diversity of applications. The amp's dc-100-MHz, −3-dB bandwidth provides oscillation-free operation over the full range of gain settings. This bandwidth, together with a 25-ns (to 0.03%) settling time and a ±12-V, ±100-mA drive capability, allows the amp to drive "flash" analog to digital converters.

Offering a 3.5-ns rise time and overshoot of <5%, the amp can be used in high speed pulsed information applications. A 1° deviation from linear phase spec and low distortion are ideal characteristics for communication systems and instrumentation applications. Users add a single gain-setting resistor and power supplies to the amp. The resistor allows the user to change the feedback to match an application. Such applications include using the CLC200 as a video log amp or as an integrator.

Not only does the CLC210 display the same high performance as the CLC200, but it has a 10-MHz full power bandwidth that produces signals up to 60 V peak to peak as well. This spec is necessary for high resolution displays. These features are also used in driving varactors in voltage-controlled oscillator loops and phase correction loops. In addition, the CLC210 offers ±32-V, ±50-mA drive capability, dc-65 MHz with −3-dB bandwidth, and 4.5 V/ns slew rate.

CLC220 provides dc-200 MHz with −3-dB bandwidth over gain settings of 1 to 50, inverting or noninverting. This amp's settling time is 15 ns to 0.03%, its rise and fall time is 1.8 ns, and it has an 800-V/μs slew rate. These features make it suitable as a general purpose op amp.

The CLC200, CLC210, CLC220 are packaged in 12-pin TO-8 cans. The CLC200 and CLC210 cost $85 in 100-piece quantities. The CLC220 is $96 in 100-piece quantities. **Comlinear Corp,** 2468 E 9th St, Loveland, CO 80537. **Circle 266**



S100 CONTROLLER BOARDS BUILD MORE VERSATILE SYSTEMS.

SMC's S100 controller boards present new opportunities in system design. Our **QSI0S100** board provides 4 independent serial I/O channels for simultaneous use of a variety of peripherals. The **FDCS100** board controls up to 4 floppy disk drives for removable mass storage capability. The **VRAMS100** board adds advanced video display capabilities, including smooth scrolling and double-height, double-width data rows. Our **ARCNET®-S100** board links up and controls a network of up to 255 computers. For complete details, contact Standard Microsystems Corporation, 35 Marcus Boulevard, Hauppauge, NY 11788 (516) 273-3100.

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CIRCLE 178

CUSTOM CONTROLLER BOARDS MEET UNIQUE STANDARDS.

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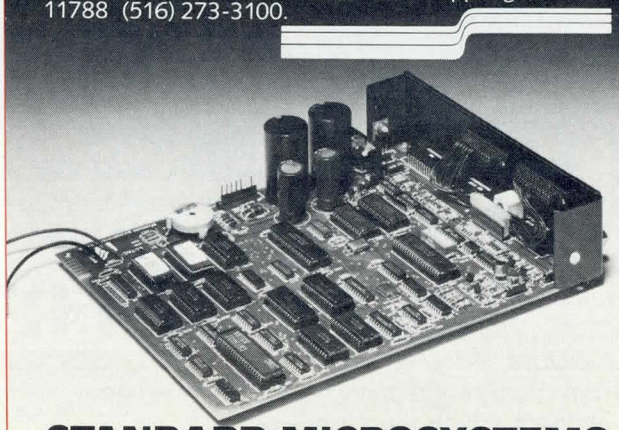
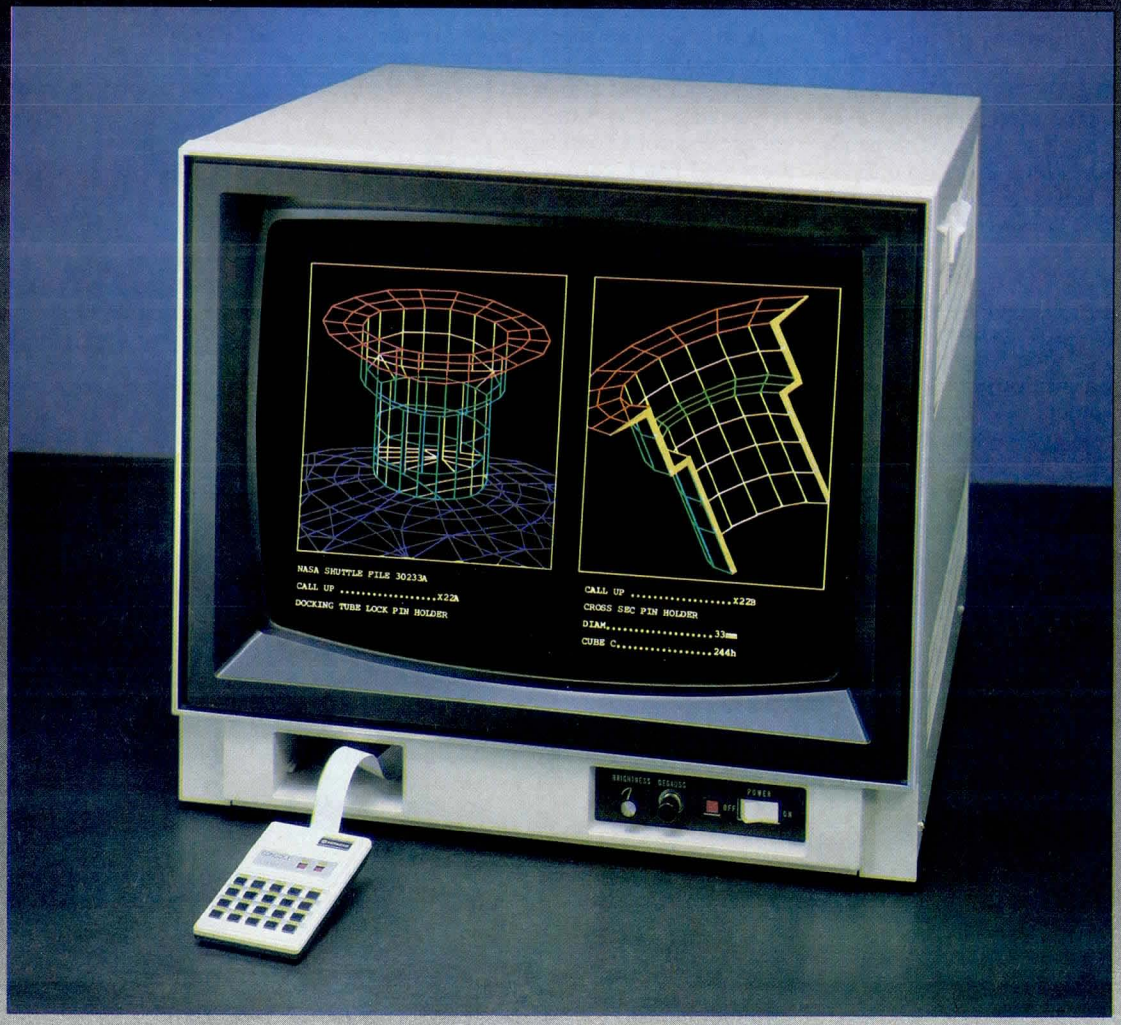


STANDARD MICROSYSTEMS. THE ONE TO WATCH.

CIRCLE 179

the genius is in the design the proof is in the image



Conventional monitor pixel

Hitachi DDC monitor pixel

THE DIFFERENCE between a conventional RGB monitor and Hitachi's monitors with Digital Dynamic Convergence™ (DDC) is the difference between a snap-shot and a professional photograph.

Take a look at the image you get from Hitachi. What you see is a beautiful picture. Why? In order to achieve maximum image clarity each picture element (pixel) must be as sharp; as clear as possible. Hitachi's DDC system offers an amazing 0.1/0.3 convergence. That's sharp.

Proven Dependability

Most importantly, the Hitachi DDC system has proven to be a success in the field. Hitachi quality keeps them working; Hitachi innovation keeps them in demand.

CONVERGENCE CHART

	Hitachi Monitor with DDC	Conventional Monitor
Quality Circle	0.1mm	0.5mm
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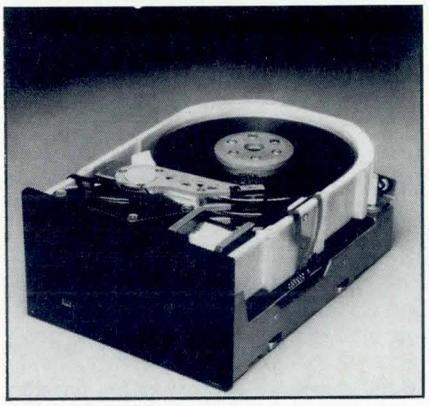
CIRCLE 124

Servo Winchester

Model TM705 is a closed loop 5¼" Winchester disk drive with 50M bytes of fast-access storage capacity. High density recording is performed on five data surfaces, with the sixth dedicated to servo control. The drive has a 1000-tpi density and a 10,416-byte/track lineal density. It is configured into 962 recording cylinders with a 5-ms track-to-track access time; avg access time is 39 ms with a max of 85 ms, and a 2-ms head settling time. The drive is priced at less than $1000 in OEM quantities. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311.



Circle 267

Compatible HP Winchesters

Series 3000, a line of Winchester disk subsystems for HP computers, offers 12 models. Winchester capacity is 5M, 10M, or 15M bytes and the optional built-in floppy drives are available in 3½", 5¼", or 8". The series is completely hardware, software, and media compatible with all HP technical and personal computers. Transfer rate is 174k bytes/s. A built-in error-correction code circuit provides added data integrity. Storage can be partitioned into formatted blocks of 1.2M, 4.8M, or 9.7M bytes. Prices start at $2860. **Bering Industries, Inc,** 747 E Brokaw Rd, San Jose, CA 95112. **Circle 268**

Internal hard disk

A hard disk system for DEC's Rainbow computer features 11M bytes of formatted capacity. The internal disk system is housed within the computer in the second floppy disk drive space. Host bus adapter plugs into the memory option slot and comes std with an additional 64K bytes of RAM. A special connector allows an additional 256K bytes of RAM for a total of 384K bytes. System supports both CP/M-80/86 and MS-DOS operating systems, and users can partition their system into a number of logical drives to allocate disk space. Software is included for virtual disk operation. **Univation Inc,** 1037 N Fairoaks Ave, Sunnyvale, CA 94089.

Circle 269

Enhanced solid state storage

Larger storage capacities and improved performance are available in the 4305 optimizer storage subsystems. Features can be installed on existing 4305 devices at customer sites, including IBM 3380 disk drive emulation. The enhanced 4305 model 3 doubles its current capacity and data rate, providing 48M bytes of semiconductor storage with a single controller. It transfers data at 3M bytes/s; data access is 0.6 ms using a 16K-bit MOS RAM. Prices range from $76,730 to $229,620. **Storage Technology Corp,** 2270 S 88th St, Louisville, CO 80028.

Circle 270

Multibus board with 1M memory

Each MM-9000D Multibus memory board, when filled with 64K-byte DRAMs, provides a 1M-byte max memory capacity. If 256K-byte DRAMs are used, the capacity is increased to 4M bytes. Six memory capacity versions are available: 512K, 768K, 1M, 2M, 3M, and 4M bytes. The board is compatible with the 68000, 8086, and Z8000 Multibus system versions. Cycle and access times are 325 ns and 220 ns, respectively. Odd parity generation and checking is included with the status of output stored in an error status register. The 1M-byte version is priced at $1695. **Micro Memory, Inc,** 9436 Irondale Ave, Chatsworth, CA 91311.

Circle 271

VAX-11/780 memory modules

The PINCOMM 780SX memory modules provide 1M byte of storage on a single card. They use 64K-bit RAMs and are hardware and software compatible with VAX-11/780s using MS780E memory systems. Each data word stored by a board is 39 bits wide, consisting of 32 data bits and 7 error correction check bits. Check bits allow single error correction and double or multiple bit error detection. A switch permits the memory to be switched offline for troubleshooting. A memory diagnostic is available as an option. The modules are priced at $2800 in a single lot. **Trendata Corp,** 3400 W Segerstrom Ave, Santa Ana, CA 92704. **Circle 272**

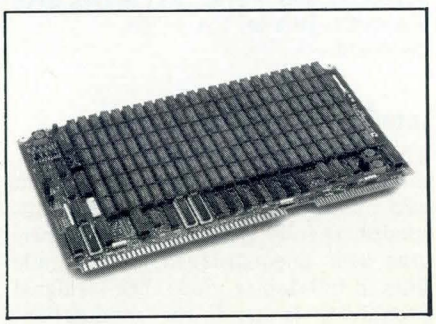
Data logging system

The Data Library is a large capacity ¼" cartridge tape data logging system. It is available with std interfaces such as RS-232-C, IEEE 488, and Multibus, and operating software for the Apple II/IIE, and IBM PC and XT. The transportable cartridge has 16 tracks recorded on 600' of tape. Each track has 4096 blocks with 1024 bytes/block. System features include a 10k-hr MTBF, a 1-bit in 10M bits error rate, and preformatting to allow block addressable data rates. Data are recorded at 10k bpi and the system operates at 60 ips with a 90-ips search speed. **Advanced Digital Information Co,** 723 9th Ave, Kirkland, WA 98033.

Circle 273

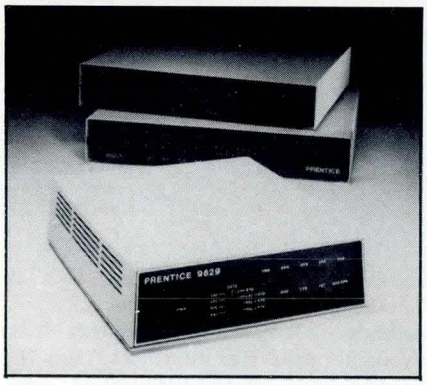
Multibus-compatible RAM board

The Am97/0000B family of RAM boards feature 1M byte of memory using 64K-byte dynamic RAMs. The board consumes 12.5 W max and has a 200-ns max access time and a 300-ns max cycle time. It supports 24-bit addressing for a max address range of 16M bytes. Board memory can start on any 64K-byte boundary and cross any megabyte boundary. Rotary switches easily set the starting address. Family also features 8- or 16-bit word size with byte-swapping capability, parity with latching error register, and interrupt generation. In quantities of one to nine, the boards range in price from $1950 to $2995. **Advanced Micro Devices Inc,** 901 Thompson P1, Sunnyvale, CA 94086.



Circle 274

High speed modem



The 9629 sync standalone modem operates over 4-wire, 3002 unconditioned or equivalent leased lines in point to point applications. Peak operating data rate is 9.6k bps with fallback rates of 7.2k and 4.8k bps. Modem features auto-adaptive equalization, which eliminates the effects of large variations in delay and amplitude distortion. Diagnostics are provided via front panel monitoring and operation and test control. Remote and local analog and digital loopback tests can be done without external equipment. Single-unit price is $2750. **Prentice Corp,** 266 Caspian Dr, PO Box 3544, Sunnyvale, CA 94088.
Circle 275

Multibus comm controller

Communications controller 8140 can operate in a multiboard system or as a standalone controller. The Multibus-compatible board contains two RS-232-C ports, two Bell 202/103 modems (CCITT V.21, V.23), an onboard 8085A micro, dual-port RAM, and two firmware levels. Resident interrupt-driven communication firmware supports packet-switching protocols. In conjunction with the 8183 direct access arrangement, the controller provides pulsed auto-dial and auto-answer. Communication between the 8140 and the bus master occurs through the dual-ported RAM. The 8140 price is $1240; the 8183 is $190. **ETI Micro,** 6918 Sierra Ct, Dublin, CA 94568.
Circle 276

Intelligent 9.6k-bps modem

The 7165 SNA-compatible diagnostic modem is available in both point to point and multipoint versions. The 9.6k-bps modem is fully synchronous and operates over unconditioned, voice grade lines in full-duplex mode. Digital signal processing is used for modulation, demodulation, and dynamic equalization. Device features built-in diagnostics and is compatible with IBM mainstream diagnostics. The host operator can automatically initiate diagnostics. Prices start at $5800 for quantity one. **NCR Comten, Inc,** 2700 Snelling Ave N, St. Paul, MN 55113.
Circle 277

Protocol converter

The PCI 3780/SNA protocol converter allows bisync 3780 terminals and emulators to communicate with an SNA/SDLC host. Conversion support is included for printers, card readers, and card punch devices. Converters can be multidropped with SDLC terminals, and multiple hosts can benefit from the SNA's enhanced network job entry capabilities. When communicating through the converter, the 3780 terminal becomes SNA/SDLC- compatible, thereby appearing to the host as an IBM 3776-2 single logical unit RJE workstation. Pricing begins at $3100. **Protocol Computers, Inc,** 6150 Canoga Ave, Woodland Hills, CA 91367.
Circle 278

Mini modem

A pocket-sized auto equalized modem, the mLDS 122 is designed for use on dedicated 4-wire unloaded metallic circuits and local area data service circuits. The async modem plugs directly into data terminal equipment and operates point to point from 50 to 9.6k bps. It is transformer coupled for isolation between terminal and phone line. Compatible with LDS 120/121 and RM 3120, the modem is powered from the EIA RS-232-C interface via data and control signals. The mLDS 122 is priced at $95 for quantity one. **Gandalf Data Inc,** 1019 S Noel, Wheeling, IL 60090.
Circle 279

Single-card modem

The VA212PAR is a Bell 212A/103-compatible modem. Printed on a single-circuit card, the direct-connect, originate/answer, full-duplex modem is capable of 0- to 300-bps async and 1.2k-bps async or sync operation. Additional features include manual and auto-call and auto-answer. Telephone numbers can be entered from the computer while the dialer's memory stores the last number dialed (up to 32 digits). Single-char command auto-redials (up to nine times) the last number. Unit price of the self-diagnostic modem is $695. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.
Circle 280

Modem/UART

The SE/SBX1 communication controller, designed for use with the iSBX, Multibus, and STD bus interfaces, incorporates UART, modem, and FCC certified line interface functions into one module. Controller thereby provides for increased system packaging density. Digital signal processing uses communications at 300 baud (full duplex) to 1.2k baud (half duplex) and follows Bell 103/202 and CCITT V.21/V.23 stds. Modem reliability is increased with MOS/LSI technology and self-test capability. **SEI,** PO Box 920522, Norcross, GA 30092.
Circle 281

DATA CONVERSION

Low power A-D converter

The ADC1143 is a 16-bit ADC that guarantees 150-mW power consumption when operated at ±12 V and 175 mW when operated ±15 V. It has an internal converter, a 10-V precision reference, and a 16-bit successive approximation register and clock. Accuracy specs include max integral and differential nonlinearity of ±0.006% (full scale range) or ±0.003% (full scale range), depending on model. Max conversions vary from 70 to 100 μs, making the converter suitable for multiple channel conversions where systems scan and convert input channels. The ADC1143J and the ADC1143K are priced at $149 and $172, respectively, in 100s. **Analog Devices, Inc,** PO Box 280, 2 Technology Way, Norwood, MA 02062.
Circle 282

Hybrid video DAC

Model AH8308T is a single-chip, fully TTL-compatible, 8-bit hybrid video DAC. The device features 1.15-W (max) power dissipation and a 65-MHz update rate. The DAC accepts 8-bits of digital data plus sync and blanking commands directly from a 5-V TTL source to support up to 1K x 1K display resolution. It generates analog composite video signals internally, has a 75-Ω source impedance, and enough analog output power to drive a 75-Ω coaxial cable and monitor with a 1-V pk to pk signal. The hybrid is housed in a 24-pin steel foil shielded double DIP. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 283

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Low cost 16-bit DAC

The DAC701 and DAC703 are complete 16-bit DACs. Included in the package are a current-to-voltage output op amp, low drift voltage reference, and fast settling switches. Linearity error is ±0.003%, settling time is 4 μs to ±0.003% full scale range (0.5 bit in 14 bits), and gain drift is limited to ±15 PPM/°C max over the temp range. The DACs operate over the −55 to 125 °C temp range and pass all criteria for MIL-STD-883, method 1014, conditions A and C under 100% test. In 100s, prices start at $25 for voltage output models. **Burr-Brown, Data Products Div,** Box 11400, Tucson, AZ 85734.
Circle 284

Adding communications to the STD BUS? Micro/sys makes it...

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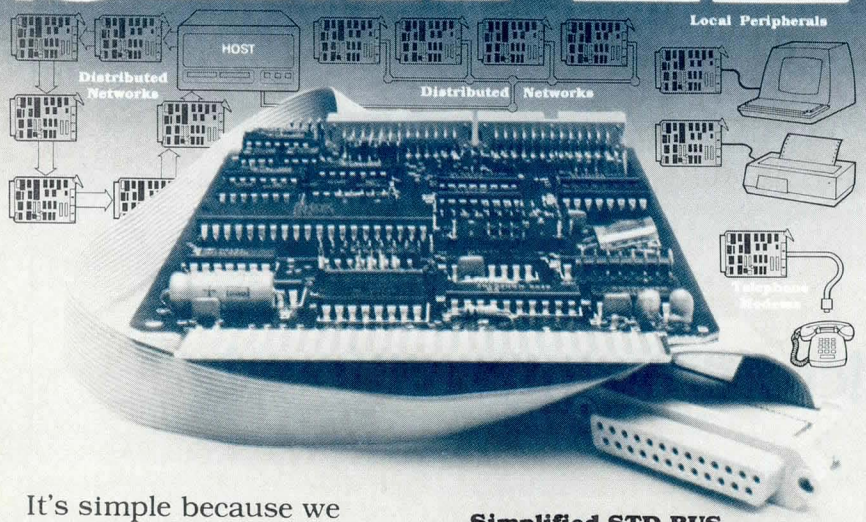

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CIRCLE 126

Micro-compatible ADC

ADC0844 is an 8-bit successive approximation ADC with a ±½ LSB or ±1 LSB total unadjusted error. The CMOS device contains an internal clock with a 40-μs max conversion time. Total unadjusted error includes nonlinearity, and full / zero-scale errors. The ADC contains a 4-channel MUX that has differential, single-ended, or pseudo-differential operating modes. Differential mode gives low frequency input, common mode rejection, and offsets the analog range. Single-ended mode assigns each of the four channels as positive; in pseudo mode, three channels act as positive inputs. Prices range from $3.85 to $8.95, depending on quantity and version. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 285

Low cost resolver/converter

A 16-bit resolver, synchro or inductosyn to digital converter, the SDC-19160 series features 16-bit/65,536-count resolution and accuracy up to ±1.3 min. The small-sized device offers a 3-state output, tracking up to 360 rpm, ±0.65-min repeatability, direction/count outputs, and velocity output. The converters are available in ±1.3- and ±2.6-min accuracies; the 14-, 12-, and 10-bit units have accuracies of ±5.3, ±8.5, and ±21 min, respectively. In 100-piece quantities, the device is $195. **ILC Data Device Corp,** 105 Wilbur P1, Bohemia, NY 11716.
Circle 286

Wideband A-D conversion system

The model GMAD2A A-D conversion system is designed to meet requirements for high accuracy conversion of wideband analog signals in data acquisition systems. It uses a sample and hold (S/H) amp that provides a 1-ns aperture time and can be ordered with 8 simultaneous S/H channels in a dual chassis, or up to 256 in a multiple chassis system. Max full-scale input voltage level is 10.24 V; dc crosstalk between channels is held to less than ±0.005% of full scale. Common mode voltage is ±11 V and common mode rejection is 70 dB. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.
Circle 287

Special Edition Preview—
Portable computers—in late October.

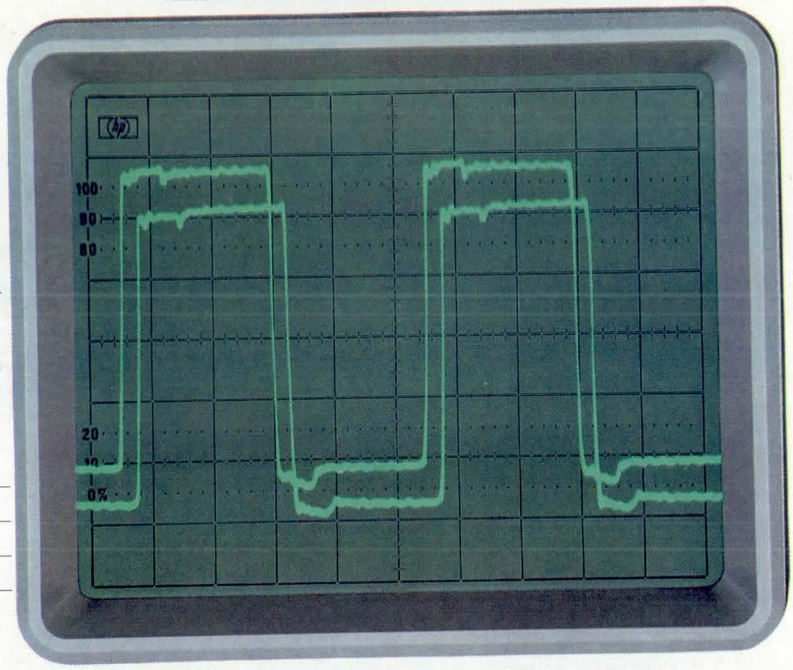
For the first time...an oscilloscope to match the timing accuracy demands of today's fastest technologies.

Laboratory quality timing accuracy plus the convenience of a portable oscilloscope.

If the accuracy of your timing measurements must keep pace with the latest technology, the HP 1726A Time Interval Oscilloscope is your best solution. It can handle tough timing problems. Although most general-purpose, laboratory oscilloscopes solve a variety of problems, their timing accuracy is typically design limited to ±500 picoseconds. This simply is not adequate for designing and producing many of today's products.

Introducing the 50 ps scope.

HP's 1726A time-interval oscilloscope solves this timing limitation with a revolutionary approach. Its new method of making timing measurements is based on combining HP counter technology with HP's advanced oscilloscope triggering circuits. The results? New levels of accuracy (±50 ps), resolution (±10 ps), and repeatability (±30 ps). All this in a portable package that won't clutter your bench or test station. Typically, the 1726A's accuracy is a factor of ten improvement over most laboratory scopes, including the one you're probably using or planning to purchase.



TIME-INTERVAL MEASUREMENT

TIME INTERVAL	500 ps	5 ns	1.2 μs
1726A Accuracy	±50 ps	±50 ps	±50 ps
1726A Resolution	±10 ps	±10 ps	±10 ps

Also, it provides accurate first-pulse measurements...and it's easy to use.

Check the time interval table.

With the 1726A, your time-interval answers are consistently accurate...and oscilloscope timing calibration is preserved even with its Time/Div vernier out of detent. In fact, intervals as long as 1.2 μs can be measured with ±50 ps accuracy.

For unprecedented convenience and ±30 ps repeatability, dial in start/stop trigger levels with 1 mV resolution, position the on-screen markers, and read the answer on the 1726A's LED display. You get fast, convenient, results you can trust...time after time.

Meeting the needs of today's technology.

With continuing IC advances, you'll need the capabilities of the 1726A in your lab or production area. Use it to uncover 400 ps clock skew in computer mainframes. Determine 200 ps propagation delays in IC's or hybrids. With the 1726A's 50 ps accuracy, observe the 20 ns round-trip delay of a test signal within a test system. Or, tie the 1726A to your data-logging system through its HP-IB interface. And with its time-interval module turned off, you'll find the 1726A to be a high-quality, general-purpose, dual-channel 275 MHz oscilloscope.

Get all the details by calling your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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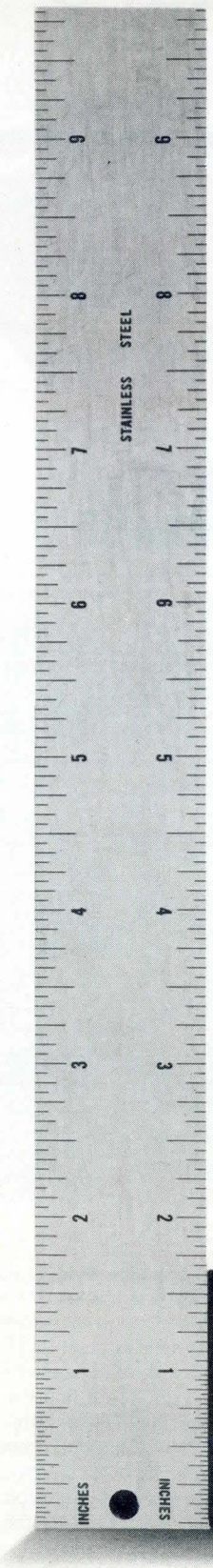
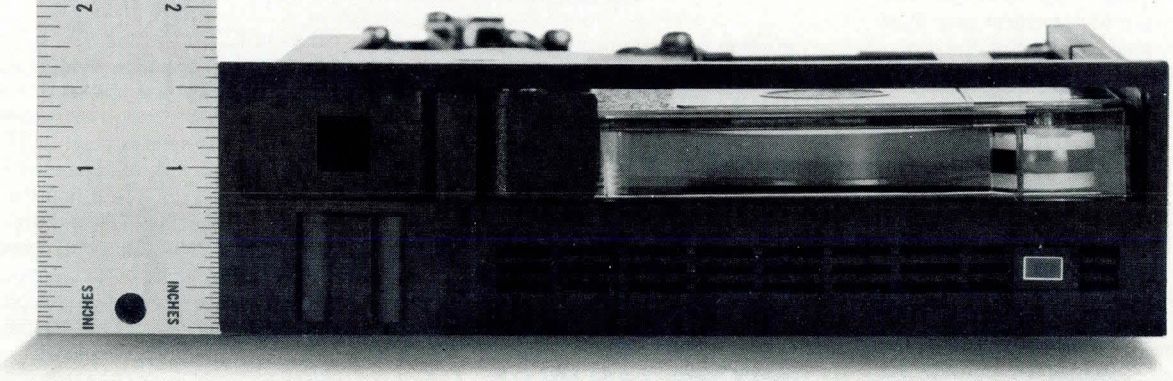
CIRCLE 127

THE 5¼" STREAMER TO MEASURE



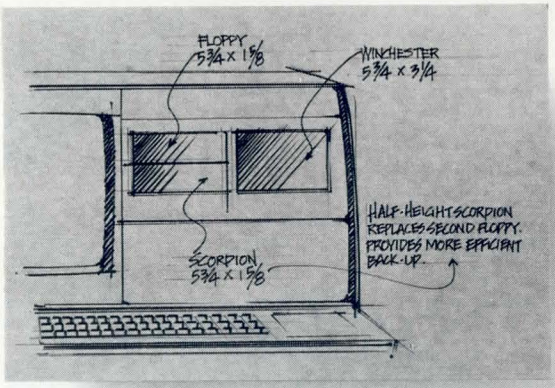
Find out what Archive has cooked up for Comdex at Booth 558.



OTHERS WILL HAVE DOWN TO.

Introducing the Scorpion™ half-height 5¼" mini streamer.

Once again, Archive has the Winchester back-up others will have to measure up to. Only this time, they also have to measure down. Because the Scorpion is only 1.625" high.



It fits the footprint of half-height floppy disk drives. So no change in existing cabinetry is necessary. Yet it still gives you up to 60MB of storage.

Now system designers can choose from a wider variety of storage combinations. For example, half-height Scorpion, half-height floppy and 5¼" Winchester.

And our standards meet your standards. The standard Archive (QIC-02) interface and QIC-24 format are both incorporated in the Scorpion.

But that's only part of the story. Thanks to Archive's advanced LSI technology, the half-height Scorpion gives you higher capacity and more functions than many 8" streaming tape drives. Yet it has fewer parts, uses less power and is competitively priced.

For complete details and a free copy of our 176-page streaming handbook, return the coupon. Or call Archive today.

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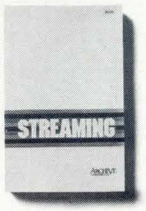

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CIRCLE 128

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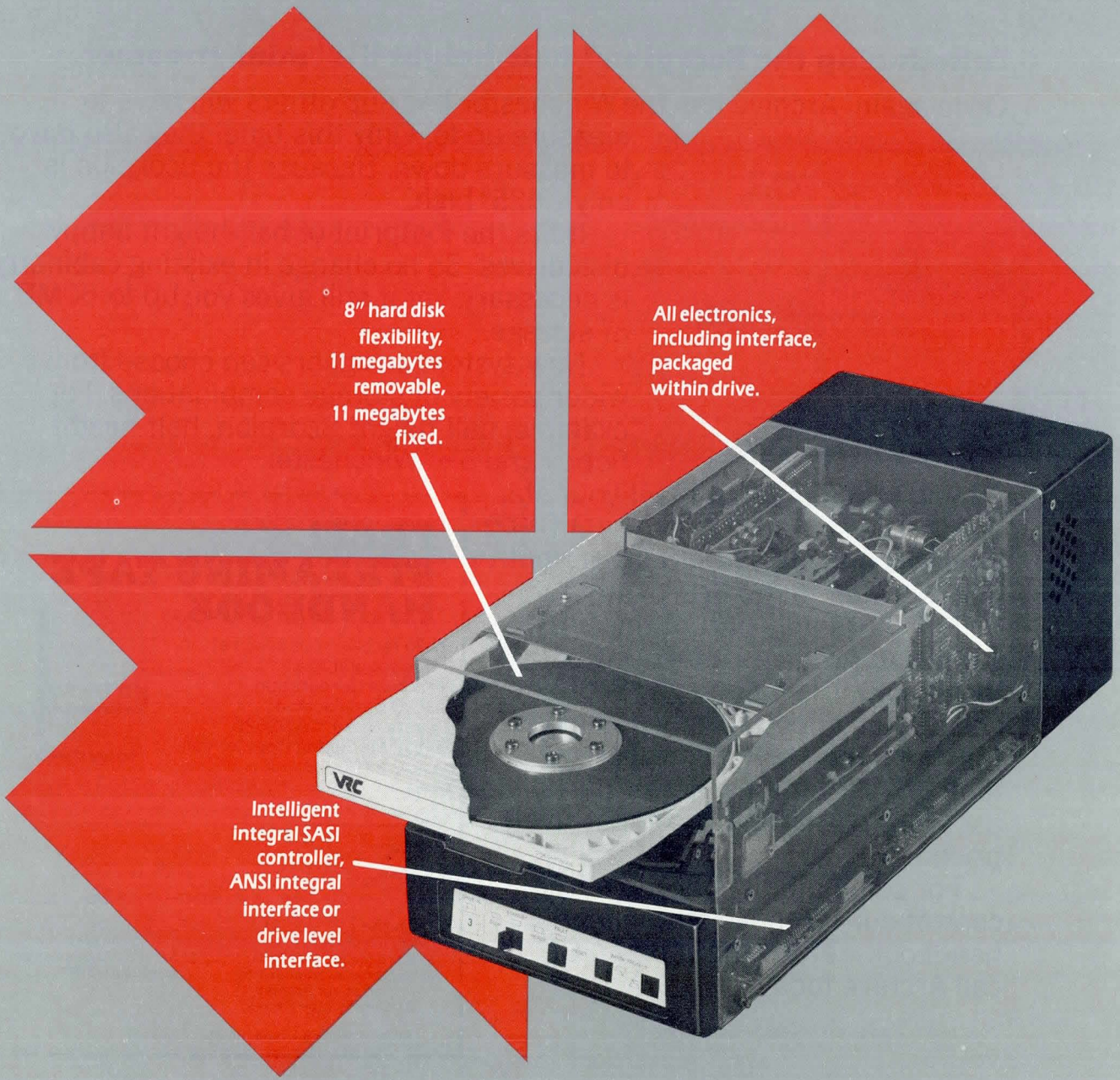
A compact drive package which includes all drive electronics, power supply and SASI controller within 8.5" wide by 7" high by 19.4" deep. The VRC 8520 gives you 11 megabytes of removable storage on a standard ANSI 8" cartridge, and 11 megabytes on a fixed disk in a one-over-one configuration. Designed to fit practically anywhere, the VRC 8520 is ideal to produce backup files on a single peripheral. It can also accommodate an ANSI standard interface. Disk drive, controller and fully-integrated power supply are contained in a small, high-performance package designed for hostile environments. With the VRC 8520, you eliminate design costs for mounting enclosures, the costs of a separate controller and power supply and messy interconnecting wiring which radiates noise.

For more information about the VRC 8520 or the VRC 8010 — a single, removable disk drive with 11 megabytes of storage, contact Vermont Research Corporation, Precision Park, North Springfield, VT 05150, Tel: 802/886-2256. TWX: 710/363-6533. In Europe call or write: Vermont Research Ltd., Cleeve Road, Leatherhead, Surrey, England, Tel: Leatherhead 376221. TLX: 23280.



VRC

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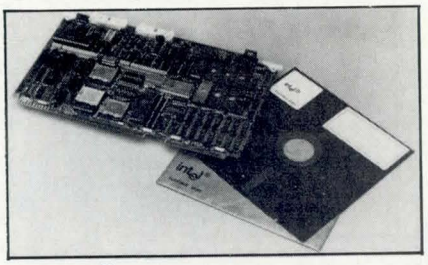
Memory Products for Systems That Can't Stand Failure

CIRCLE 129

Networking single-board computer



The iSBC®186/51 COMMputer board combines a single-chip micro, data communications capabilities, and industry std networking software. Board includes iAPX 186 central processor, 80130 operating system firmware, 82586 LAN coprocessor, and 82501 Ethernet serial interface. Device can run user programs, handle communication tasks, and operate as an intelligent front end. The board has 128K bytes of dual-ported RAM expandable to 256K bytes using a multimode board. Board sells for $3000; network software sells for $5000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 288**

High speed, 68000-compatible micro

The 12.5-MHz version of the 16-bit HD68000 micro, designated HD68000-12, is available in a 64-pin cerDIP, 68-pin pin-grid array, and 68-pin LCC. It is both pin- and software-compatible with the MC68000L12. Minimum instruction execution time is 0.32 μs, which was achieved by optically shrinking the circuit pattern of the 8-MHz version. The micro is fabricated using high speed, NMOS process, and minimum 2.6-micron line width. Prices in lots of 1000 range from $73.17 to $85.36. **Hitachi, Ltd,** No 5-1, 1-Chome, Marunouchi, Chiyodaku, Tokyo, Japan. **Circle 289**

Microprocessor system

The CD68K microprocessor system board features four serial ports, clock/calendar, and hardware dynamic RAM refresh with DMA capability to local memory. Up to two, 1M-byte local memory boards can be used per CPU board. Because local memory is accessible through a P2 connector bus, no wait states are incurred. The board uses a CMOS realtime clock/RAM chip that, when connected to a battery backup, retains system information during power failures. A 2-level memory management architecture has separate segment and page maps with a context selection register for simultaneous mapping of 16 process contexts. **Callan Data Systems,** 2637 Townsgate Rd, Westlake Village, CA 91361. **Circle 290**

VMEbus-based computer

Designed for implementing new operating systems on the VMEbus using the 68000 processor family, the Eurocom 3-1./68K is a single-board computer. Onboard features include 1M byte of RAM, floppy controller, and realtime clock. Serial I/O channels are used for normal async protocols as well as HDLC/SDLC. Encoding can be either FM, NRZ, NRZI, or Manchester codes for speeds up to 1M bps. Operating system support includes CP/M-68K and Unix. VMEbus interface can be used as a bus master or bus slave with address modifiers. **Eltec Elektronik** GmbH, Galileo-Galilei-StraBe 2, D-6500 Mainz 42, West Germany. **Circle 291**

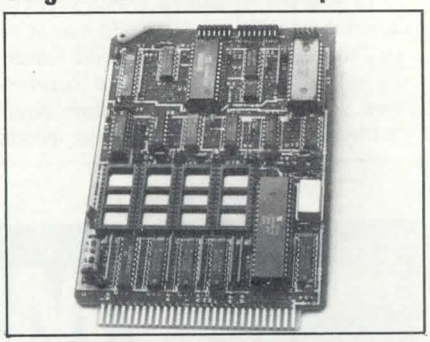
Winchester cartridge for S-100

Super Star, an S-100-based computer system, is equipped with a 5¼", 5M-byte fixed, 5M-byte removable Winchester. The std CP/M operating system permits the user to access the library of available software programs. Features include a 5¼" half-height 48-tpi, floppy disk drive (Osborne format compatible), 6-slot motherboard, S-100 IEEE std compatibility, switch-selectable 110/220-V power supply, and a 1-year warranty. The system is priced at $5000. **Advanced Digital Corp,** 5432 Production Dr, Huntington Beach, CA 92649. **Circle 292**

S-100/memory combination

The P-286 CPU module is designed around Intel's 80286 micro, allowing it to execute software developed for the 8086/8088. Onboard resources include a socket for the optional 80287 math coprocessor, three 16-bit programmable and cascadable system timers, programmable interrupt controller, and sockets for 64K bytes of EPROM/ROM. The P-128 is a 128K-byte static RAM board that features 8K x 8 CMOS RAM chips for low power consumption. The boards interface via an IEEE 696 interface and a private access bus for no wait states. Initially offered as a pair, the boards are priced at $3000. **Performics Inc,** PO Box 3207, Nashua, NH 03061. **Circle 293**

Single-board STD bus computer



For industrial applications, the SB8010 single-board STD bus computer can operate as a self-contained controller or in a multicard system. The board contains a Z80 or Z80A, up to 32K bytes of memory, an RS-232-C port, and a counter/timer/interrupt controller. Memory system allows a mix of up to four 28-pin, JEDEC pinout RAM, ROM, or EPROM and flexible memory mapping allows any memory device to be placed within any 2K-byte boundary. In quantities of 10 to 24, prices range form $365 to $415. **Micro/sys,** 1367 Foothill Blvd, La Canada, CA 91011. **Circle 294**

PC-compatible CP/M board

DS2 is a coprocessing micro system that plugs into the IBM PC and allows users to run CP/M software or PC-DOS on the PC. The board consists of a Z80B processor, 64K bytes of RAM, and one serial port. The port can be used in one of three modes: RS-232, RS-422, or IBM's implementation of a 20-mA current loop. The DS2S board has all DS2 capabilities but four sync/async ports replace the serial port. It contains sockets for EPROM and/or EEPROM-stored programs. **BYAD, Inc,** 95 W Algonquin Rd, Arlington Heights, IL 60005. **Circle 295**

STD bus CPU card

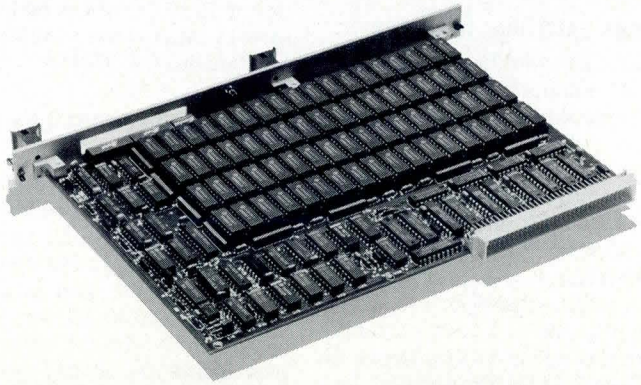
CPU-100, a 6502-based micro CPU card, is specifically designed for STD bus applications. Built-in EIA RS-232 interface provides direct terminal/printer connection. Board has up to 8K bytes of memory space available in RAM, ROM, or a combination of both. Also included are two interval timers, serial to parallel and parallel to serial shift registers, and two bidirectional 8-bit data ports. The board functions as the CPU of a multiboard system with memory expansion to 65K bytes. Computer is priced at $200. **Techno, Inc,** 14 Crandall Ave, Pompton Lakes, NJ 07442. **Circle 296**

Switching power supplies

The CE-35-103 40-W switching power supply features outputs of 5 V at 3.5 A, −12 V at 0.4 A, and 12 V at 2.5 A. User selectable inputs are 90 to 135 Vac or 180 to 270 Vac at 47 to 440 Hz. Std features include printed circuit board construction, onboard emi filter, short circuit proteciton, and 5-V overvoltage protection. In addition, there is a 1 cycle holdup time, inrush current limiting, and typ efficiency >70%. The unit's dimensions are 6.30″ x 3.94″ x 1.75″ (16.00 x 10.01 x 4.44 cm). In 1000 piece quantities, the supply is $32.50. **General Instrument Corp, Computer Products Div,** 1401 Lomaland Dr, El Paso, TX 79935.
Circle 297

VMEbus MEMORIES

512K BYTES NOW... 2M BYTES LATER



Compatible with the VME/10 microcomputer system and MVME210 memory board, the MM-6000D is a high density memory that can employ either 64K or 256K DRAMs. A jumper option selects either 64K or 256K DRAM operation.

Reliability is ensured by burn-in and running memory diagnostics that check operation for 48 hours while temperature-cycling boards between 0 and 65°C.

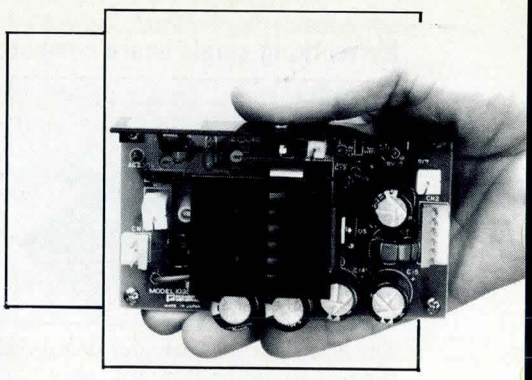
FEATURES

- Capacity:
  512K, 256K, 128K Bytes (64K DRAM)
  2M, 1.5M, 1M Bytes (256K DRAM)
- Cycle Time: 330 nsec
- Access Time: 210 nsec
- Parity generation and checking
- Module selection on 1000_H boundaries in the 16M bytes address field
- Single +5V supply
- Jumper option for battery backup
- 1-year warranty on parts and labor

First in add-in memories for microprocessor systems

micro Memory Inc
9436 Irondale Ave.
Chatsworth, California 91311
Telephone: (213) 998-0070

Printer power supplies



Models 1035-1/2/3/4/5 switchers provide a single-rated output of 35 W. Full-rated output is provided over an ambient temp range of 0 to 40 °C with a 2% derating to 70 °C. Models include outputs of 5 Vdc at 7 A and 24 Vdc at 1.5 A. Power supply input offers pin-strappable voltage ranges of either 90 to 130 Vac, or for European applications 180 to 260 Vac at 47 to 440 Hz. Other specs include 70% efficiencies, holdup time of 16 ms, and input to output isolation of 1500 Vac. Convection cooling is std. All models are $75. **Power General,** 152 Will Dr, PO Box 189, Canton, MA 02021.
Circle 298

Micro power modules

Models 3.12.1000 and 3.15.1000 are triple-output power supplies designed for PC boards. The 3.15.1000 has ±15 V at 100 mA and 5 V at 1 A. The 3.12.1000 has ±12 V at 120 mA and 5 V at 1 A. Each unit has digital and analog outputs. A high efficiency regulator for the 5-V output helps it run cooler when fully loaded (up to 50 °C ambient temp). Additional features are low noise level, isolated analog and digital grounds within each unit, and protection for all outputs against shorts. The supplies are priced as $119 each, or $101.15 at the 100-piece level. **Calex Manufacturing Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.
Circle 299

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- WHAT EQUIPMENT DO YOU HAVE EXPERIENCE WITH &/OR ACCESS TO &/OR PLAN TO BUY?

  ☐ MAINFRAME ☐ MINI ☐ MICRO ☐ DESIGN/R&D

  BRAND NAME(S): ☐ IBM ☐ XEROX ☐ APPLE ☐ TI

  ☐ COMMODORE ☐ RADIO SHACK ☐ ATARI ☐ OSBORNE

  ☐ TIMEX/SINCLAIR ☐ NORTH STAR ☐ HEWLETT PACKARD

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  ☐ LEGAL ☐ VOICE ☐ MEDICAL ☐ APPLIANCE (HOME) CONTROL

  ☐ ROBOTICS ☐ GAMES ☐ MUSIC ☐ R&D ☐ OTHER _____

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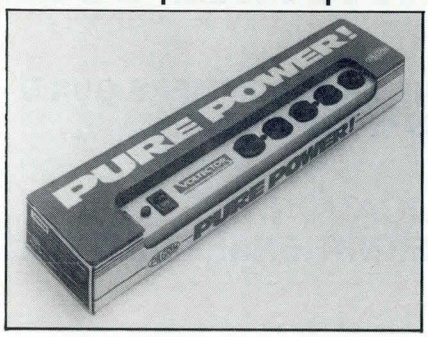
CIRCLE 131

Interference-protected strip



The Voltector® series 10 conditioned power strip protects computer equipment from lightning-induced transient surges and high frequency ac line noise. Each receptacle is rf isolated from the power line to prevent crosstalk and to enable reliable side by side performance without mutual interference. The series eliminates the need to plug individual peripherals into separate wall outlets to achieve power-cord isolation. It also eliminates a dedicated circuit. Four outlet models are priced at $146.40, six outlets at $152.90, and eight outlets at $159.40. **Pilgrim Electric Co,** 29 Cain Dr, Plainview, NY 11803.

Circle 300

Triple output converters

The ES series of isolated triple output dc-dc converters provides 15-W total output power. The series consists of 12 models providing isolated dc outputs of 5 and ±12 V; 5 and ±15 V; 5 V, 12 V and −5 V; and 5 V, 15 V and −5 V. Models are available for inputs of 12, 24, or 48 Vdc. All models contain a MOSFET circuit with 100-kHz switching frequencies. They are available with input ranges of 9 to 18 Vdc, 18 to 36 Vdc, and 35 to 72 Vdc. The converters are priced at $119 (one to nine pieces) and $83.30 in quantities of 100. **Stevens-Arnold, Inc, a sub of Computer Products, Inc, Power Products Div,** 2801 Gateway Dr, Pompano Beach, FL 33060.

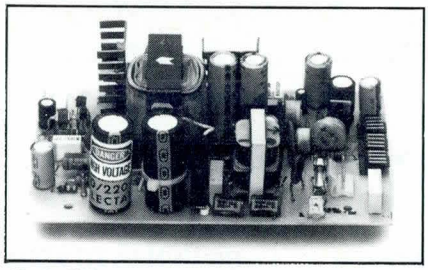
Circle 301

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? Turn to the Editorial Score Box on the Reader Inquiry Card.

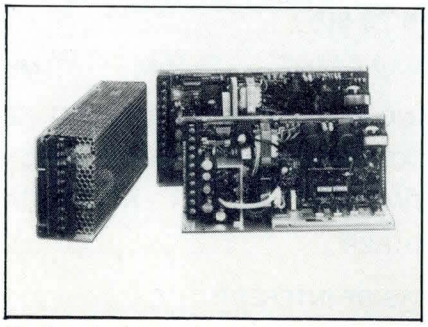
A 3-output switcher

The XL40-3601 40-W, 3-output power supply is UL and CSA approved. It meets VDE 0806, IEC 380, and FCC and VDE level B noise requirements. A proprietary current-controlled feedback network achieves tight regulation and fast transient response. Std features include 110/220-Vac user selectable input voltage, input surge protection, power limit, and short circuit protection. In 100-piece quantities, each unit sells for $60. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.



Circle 302

Winchester power supplies



Designed for Winchester disk drive applications, the KS100-05/06 and the KS130-05/06 provide 100- or 130-W switching power, respectively. Units have a second 12-V output that allows two 12-V outputs to be put in parallel, thereby doubling the current. This feature accommodates hard disk drives that require high surge current at startup and higher continuous current during operation. In 1- to 9-unit quantities, the KS100 is $188; the KS130 is $205. **KEC Electronics,** 20817 Western Ave, Torrance, CA 90501.

Circle 303

Multi-output 100-W switchers

MOV-100 series has three multi-output open-frame switching power supplies. These supplies can power logic, memory, interfaces, disk drives, and printers in micro-based systems. Second output is 12 Vdc at 1.5A, and third output is −12 Vdc at 1 A. User has a choice of 24 Vdc at 4 A peak or 12 Vdc at 5 A peak for the fourth output. Control loop regulates the line and load of the 5-V output to ±1%. Vac input can be 90 to 132 V or 180 to 264 V, 47 to 63 Hz. The MOV-100 series is priced at $172 in quantities of 1 to 100. **Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717.

Circle 304

PERIPHERALS

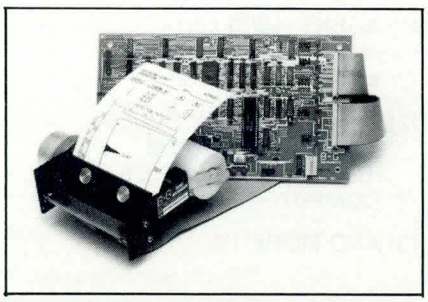
Hard copy from video interface

VGR 4000 RGB interface makes high resolution monochrome hard copy from full-color raster scan video sources. It accepts red, green, and blue signals that are mixed to produce a monochrome hard copy. Features include BNC cable interconnect, single BNC monochrome video source input through the green channel, and internal, independent adjustment for color mix. In addition, no system programming is required. System produces black and white (with 16 shades of gray) or continuous-tone images. **Honeywell, Inc, Test Instruments Div,** PO Box 5227, Denver, CO 80217.

Circle 305

Smart/small printer/plotter

DataPlot 401 is a smart printer/plotter and instrument logic system that uses fixed-dot printing on 4.5″ thermal paper. It prints X- and Y-axis legends concurrently with graphics and data, enabling it to produce printouts with a single paper pass. System delivers the std set of 64 ASCII chars, plus 32 special chars on both axes. Software commands permit convenient programming for printing, mixed with line and dot graphics. Unit can also perform arithmetic and logic functions. Both serial RS-232-C and parallel ASCII interfaces are supplied. **B-G Instruments,** PO Box 67, Alta Loma, CA 91701.



Circle 306

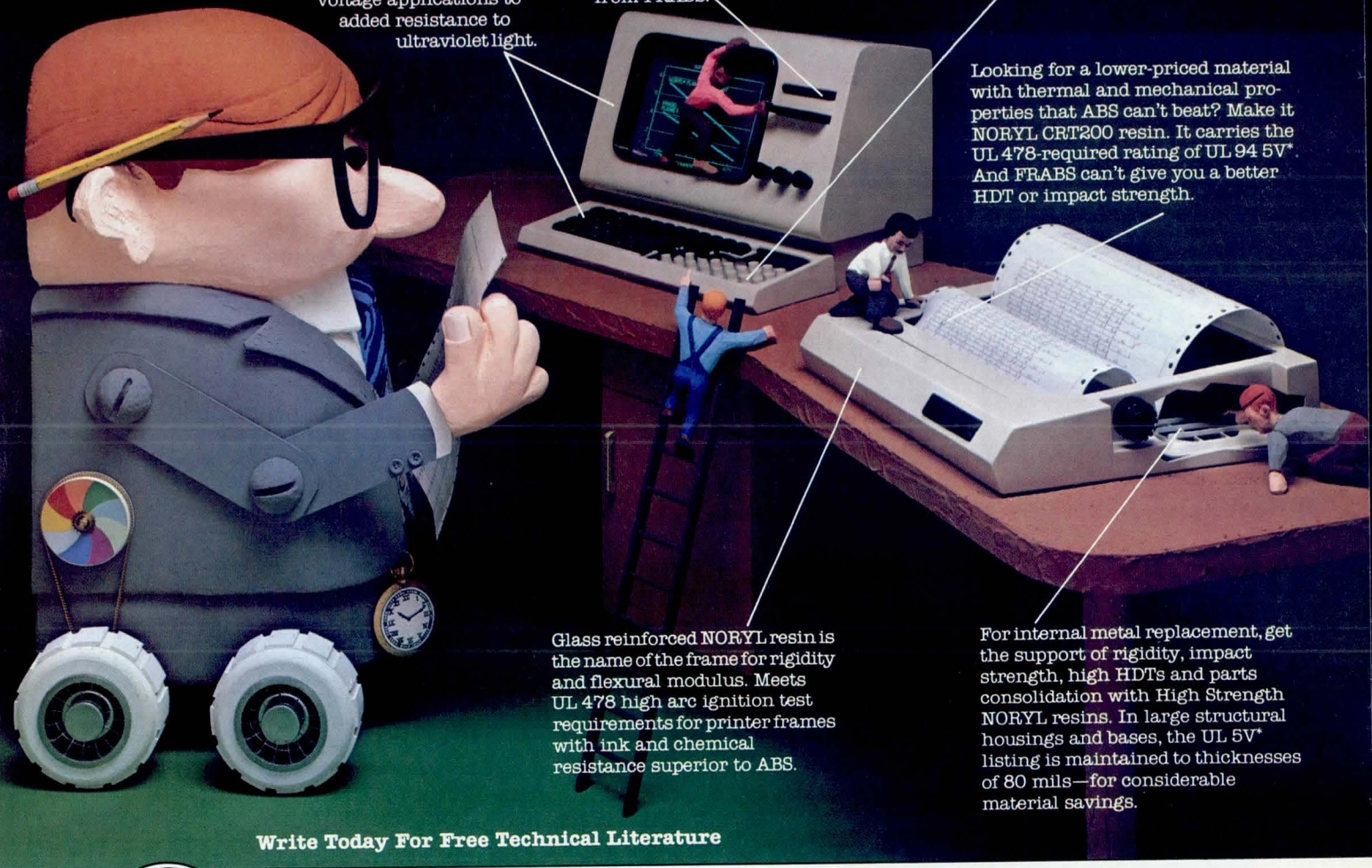
For the one material that means business inside and out,

Make it NORYL® resin

The new family of versatile moldable, formable, extrudable NORYL resins was developed expressly for computers and business equipment, to terminate ABS's usefulness. Design-in just the UL requirement you need, for greater performance at a cost lower than or comparable to FRABS. Everything from low voltage applications to added resistance to ultraviolet light.

The inferior tensile and impact strengths of FRABS need only be an unhappy memory. NORYL PC180 resin meets UL requirements for personal computers. And with NORYL PC180 resin's lower specific gravity and lower price, your part will weigh less and cost less than one molded from FRABS.

The dimensional stability, heat resistance and UL ratings of NORYL resin will get you in touch with cost-effective keyboard frames that outperform ABS.



Looking for a lower-priced material with thermal and mechanical properties that ABS can't beat? Make it NORYL CRT200 resin. It carries the UL 478-required rating of UL 94 5V*. And FRABS can't give you a better HDT or impact strength.

Glass reinforced NORYL resin is the name of the frame for rigidity and flexural modulus. Meets UL 478 high arc ignition test requirements for printer frames with ink and chemical resistance superior to ABS.

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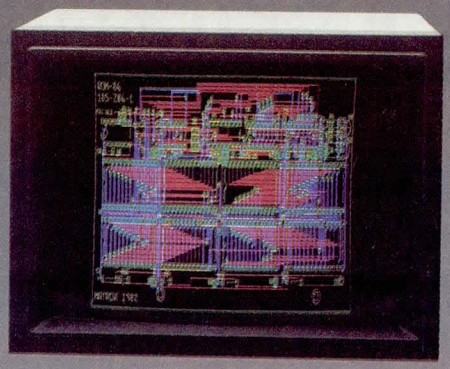
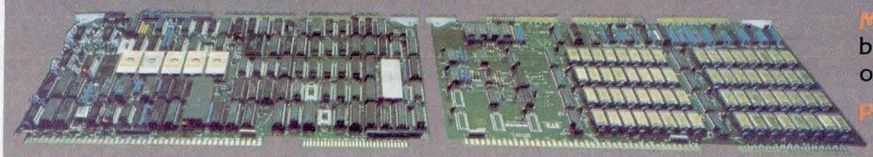
CIRCLE 132

COLOR GRAPHICS BOARDS 1024 X 1024





DISPLAY RESOLUTION: 1024 x 768 pixels non-interlaced at 60Hz or up to 1600 x 1200 pixels interlaced at 30Hz

READ/WRITE AREA: 1024 x 1024 x 4 bits/pixel expandable to 1024 x 1024 x 16 or 2048 x 2048 x 4

SPEED: Four on-board processors draw graphics primitives at 50 to 800 nsec/pixel

COLOR: 16 display colors from a palette of 256

SOFTWARE: On-board 16 bit CPU with resident graphics software interprets over 256 commands

MODULARITY: GXB-1000 is fully Multibus compatible (IEEE-796), and requires only + 5V

PRICE: $3225.00 complete*

MATROX GXB-1000 - The complete color graphics solution.

The GXB-1000 is a complete color graphics display system implemented on two Multibus boards. The system executes a display file containing high level graphics commands, generated by the user's host CPU. The GXB-1000 includes all the necessary hardware and software to draw lines, polygons, circles, characters, etc.

The unmatched performance and low cost of GXB-1000 make it the perfect solution for OEM color graphic displays. Additionally, Matrox can provide RGB monitors, CPU boards, memory boards, cardcages and keyboards for complete display system requirements.

Multibus - TM Intel, *QTY 100

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EUROPE
Herengracht 22, 4924 BH Drimmelen, Holland
Tel.: 01626-3850 Telex: 74341 MATRX NL

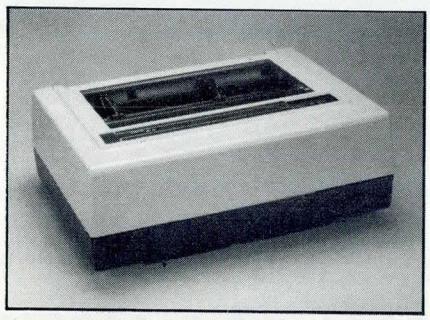
CIRCLE 175

SYSTEM COMPONENTS/ PERIPHERALS

Plotters/printers

Plot 10 plotters/printers are versions of the 4542 2-color and 4544 multicolor printers. They can switch from graphic functions (gray scale scanning) to data processing text printing, and can mix both modes. The plotters/printers feature the 5162 frontend processor and the stored force Flexhammer printhead. The 4542 plotter/printer produces graphics in black and red. The 4544 version can produce hues in the entire color spectrum by mixing its cyan, magenta, yellow, and black basic colors. The 4542 is $3900 and the 4544 is $4600. **Facit, Inc,** 235 Main Dunstable Rd, Nashua, NH 03061.

Circle 355



Bar-code readers for portables

Self-contained bar-code readers are available for the TRS-80 model 100 and the Epson HX-20 portable computers. Devices allow users to read industry std 3 of 9 code and store the results in computer memory. Reader features a push to read switch and a scanner rate up to 76 cm/s. It will read lines as small as 0.3 mm. The unit does not require additional hardware or software to operate. User interface to exisitng programs is easily accomplished. Each unit comes with software and bar-code reader and is priced at $279.95. **Bi-Tech Enterprises, Inc,** 10B Carlough Rd, Bohemia, NY 11716.

Circle 356

Floating point hardware

The S-100/IEEE 696 bus-compatible plug-in floating point accelerator (SKYFFP-S) is designed for MC68000-based systems. The single-bus card is capable of a 3-μs, 32-bit floating point multiply. Processor operates on data in 32-bit single-precision and 64-bit double-precision IEEE std floating point formats. Std processor configuration contains 4K bytes of RAM. The board performs format conversion, square root, log and trig functions, complex arithmetic, and pivot operations for matrix work. Price is $2600. **Sky Computers, Inc,** Foot of John St, Lowell, MA 01852.

Circle 357

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Other system designers face the same problems you've already solved. You could help them by writing a technical article for Computer Design. For a free copy of our Author's Guide, circle **503** *on the Reader Inquiry Card.*

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Feature Comparison Chart *

Feature	ADDS 60	**VISUAL 50**	TeleVideo® 925	Zenith 19	Wyse 100
Style	4	**4**	4	3	5
Overall Quality	2	**5**	3	4	3
Keyboard	3	**5**	2	4	2
Rollover/false keying	5	**5**	3	4	4
Video Quality	1	**5**	4	4	3
No. of attributes	5	**5**	5	2	5
Attribute method	2	**5**	2	4	2
Suitability for micros	2	**5**	3	5	3
	24	**39**	26	30	27
List Price	$895	**695**	995	895	995

*MICROSYSTEMS—March 1983
**THE ERGONOMICS NEWSLETTER—August 1982

Meet the VISUAL 55

The VISUAL 50, widely acclaimed as the best performing low cost terminal in the industry, is a tough act to follow. But the new VISUAL 55 extends its predecessor's performance even further by adding 12 user-programmable non-volatile function keys, extended editing features and selectable scrolling regions ("split screen").

Both the VISUAL 50 and VISUAL 55 offer features you expect only from the high priced units. For example, the enclosure is ergonomically designed and can be easily swiveled and tilted for maximum operator comfort. A detached keyboard, smooth scroll, large 7 x 9 dot matrix characters and non-glare screen are only a few of the many human engineering features.

Another distinctive feature of the VISUAL 50 and VISUAL 55 is their emulation capability. Both terminals are code-for-code compatible with the Hazeltine Espirit,™ ADDS Viewpoint,® Lear Siegler ADM3A and DEC VT52.® In addition, the VISUAL 55 offers emulations of the Hazeltine 1500/1510 and VISUAL 200/210. Menu-driven set-up modes in non-volatile memory allow easy selection of terminal parameters.

And you're not limited to mere emulation. Unbiased experts rate the combination of features offered by the VISUAL 50/55 family significantly more attractive than competitive terminals.

Both VISUAL terminals are UL and CSA listed and exceed FCC Class A requirements and U.S. Government standards for X-ray emissions.

Call or write for full details.

VISUAL See for yourself

Visual Technology Incorporated
540 Main Street, Tewksbury, MA 01876
Telephone (617) 851-5000. Telex 951-539

CIRCLE 133

Flexible Solutions to Your Rigid Requirements

When it comes to membranes, Cherry has layers of expertise... to give you unlimited options. Which means your Cherry membrane can have any shape, any key arrangement, color or legend. Encoded or non-encoded. With or without tactile feel, static or RFI shielding.

Any special pattern, surface effect or color combination graphics you specify, Cherry will produce. Screened or extruded textures, embossed keys, gloss or matte finish.

Custom design, a modified standard or an off-the-shelf standard, Cherry has them all. **Complete system designs, too.** For communications interface, alphanumeric lighted displays or other keyboard-associated subsystems. Working from your schematic... or creating a custom design to your specific task objectives.

All this and unbiased application engineering assistance. Because we're expert in **all** the most cost-effective keyswitch technologies... membrane, gold crosspoint and capacitive. A good reason to make Cherry your key source for linking man and machine.

Send for your free Cherry Keyboard Kit. Then let us suggest the solution that's right for your application.

SEE Us At WESCON San Francisco Nov. 8-10 Cherry Booths 2028-2034

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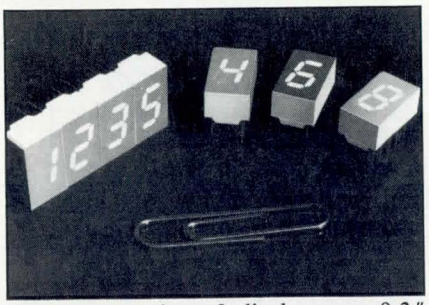
CIRCLE 134

Mini LEDs



The HDSP series of displays are 0.3″ (7.6-mm) 7-segment LEDs. They are available in std red, high efficiency red, yellow, and green. LEDs feature bright, evenly lighted segments for high ambient light viewing, which can be increased up to 50% when the displays are driven at currents of 5 to 10 mA. A low drive current achieves the same brightness as HP's existing family of 0.3″ LEDs, with 25% less current and viewing distances up to 10′ (3 m). In quantities of 1k, the LEDs are priced between $1.25 and $2.00. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 307

High sensitivity optocoupler/isolator

Operating with an input current of 1 mA, the MOC8100 optocoupler consists of a gallium-arsenide LED coupled to a silicon phototransistor. It has a guaranteed minimum current transfer ratio of 50% and can be directly driven from low level logic and telecommunication circuits. Device has 7500-V isolation voltage and UL recognition. Coupler/isolator has applications in low power drain computers and telecommunications. The 100- to 999-quantity price is $1.20. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036. **Circle 308**

Thin-film network

TDP1401 (14 pins) and TDP1601 (16 pins) are circuit configurations of precision thin-film resistor networks. Circuit is available with 13 or 15 nominally equal resistors, each connected between a common pin and a discrete board pin. All networks feature an epoxy-molded package for auto-insertion ease. Std electrical characteristics include tolerances of 1%, 0.5%, and 0.1% with ±0.05% ratio tolerance. Typ price, in 100s, is $2.59. **Dale Electronics, Inc,** Dept 860, Box 609, Columbus, NE 68601. **Circle 309**

STD bus enclosure

A tabletop and rackmountable enclosure for STD bus systems, the VP200 consists of a prewired 16-slot motherboard, card rack, four voltage-level switching power supply, and cooling fan. Front-panel controls include a lighted reset switch and key operated power switch. Side walls and front panel are 0.08″ (0.20-cm) clear aluminum. The 90-W supply provides 5 V at 10 A, −5 V at 1 A, 12 V at 2 A, and −12 V at 1 A. Rear panel has four DB25 cutouts, two DB50 cutouts, two Centronic cutouts, and a BNC cutout. The VP200 is priced at $750. **Vector Electronic Co, Inc,** 12460 Gladstone Ave, Sylmar, CA 91342. **Circle 310**

Disk rotor step motor

SynchroStep is a step motor with an ironless disk rotor. Its magnetic circuit has low losses and negligible mutual inductance. The unit can operate in an overpower condition without significant saturation. This results in reduced torque ripple at high output levels. The motor is available with field windings in series or parallel, depending on drive requirements and operates at 3.6° and 1.8° per step. Model USS-52 has a 0.3-ms mechanical time constant, 158k-rads/s^2 theoretical acceleration, a 260-Hz resonant frequency, and a 30-kW/s power rate. **PMI Motors, Inc, a div of Kollmorgen Corp,** 5 Aerial Way, Syosset, NY 11791. **Circle 311**

Sealed filters and capacitors

Hermetically-sealed emi/rfi filters and capacitors feature a glass to metal seal at both ends of the case. The case meets the requirements of a fine leak test. Four circuit configurations are available (feed-through capacitors, L, Pi, or T) for ease in design implementation. Threaded mount units have an ac voltage rating from 125 V to 240 V at frequencies to 400 Hz over the full temp range of −55 to 125 °C. Effective filtering begins below 50 kHz and continues through 10 GHz. **Spectrum Control, Inc,** 2185 W Eighth St, Erie, PA 16501.
Circle 312

Step motor systems

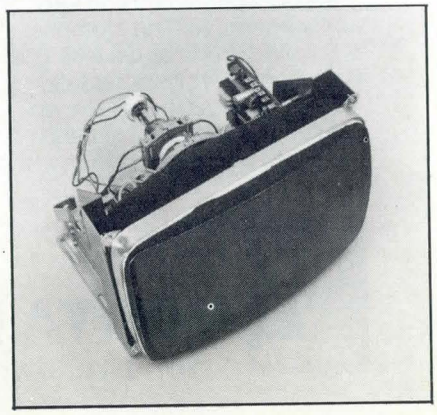
High power step motor systems provide torques from 1450 to 5100 in-oz (10.2 to 36 N-m) with a std resolution of 1k steps/revolution. Users must provide power and wiring between system components. Each system consists of a motor, motor translator, and power transformer. Motor translators are controlled by a pulse generator, or by preset indexes. The indexes give optional motor control through a programmable controller or computer. Step and direction inputs operate at step rates up to 50 kHz (50 revolutions/s at 1k pulses/revolution). **Compumotor Corp,** 1310 Ross St, Petaluma, CA 94952.
Circle 313

Keyboard assembly

The series 2571 keyboard assembly is a low profile, 3- x 4-keyboard array. It features front-panel mounting and 3-piece unitized construction. Keyboard has four 0.1″ (0.254-cm) diameter posts that are 0.24″ (0.61 cm) in length for flush mounting. Std output configurations are single pole/common bus, X-Y matrix, and two of seven. Conductive rubber contacts are rated 5 mA at 12 Vdc with a 200-Ω resistance. Key and switch mechanism offers soft-click tactile feedback, and a contact and legend life of over 1M switch actuations. In 100-piece quantities, price is $4.24. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.
Circle 314

High resolution video displays

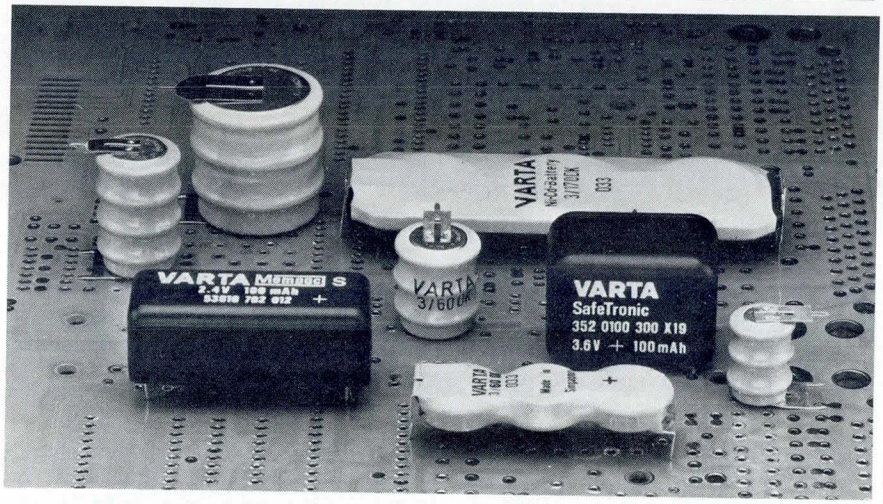
Intended for high resolution OEM applications, the 1200 and 1500 series are 110° monochrome monitors. Horizontal scanning frequencies are increased to 32 kHz and video bandwidths to 32 MHz. The 1200 and 1500 have 12″ and 15″ screens, respectively. Each is available with switching power supplies for terminal and monitor logic. Featured is a built-in digital brightness control. Displays can be supplied with any registered phosphor. **Computer Displays International, Inc,** 859 S Rte 53, Addison, IL 60101.



Circle 315

Push-button/indicator series

Series 50 line of lighted push buttons and indicators are interchangeable with the Micro Switch AML line. They feature momentary, alternate action switches and lighted indicators; solid state or electromechanical design; and incandescent and LED lighting. The devices are UL approved and CSA certified. VDE approvals are pending on several versions. Silver or gold contacts are available with a 100k cycle life on mechanical switches. A wide selection of lens caps, button heights, full- and split-screen displays, colors, and square or rectangular shapes are available. **ITW Switches, An Illinois Tool Works Co,** 6615 W Irving Park Rd, Chicago, IL 60634. **Circle 316**



These batteries put 40% more capacity in less board space.

Varta Ni-Cd rechargeable batteries have major advantages over cylindrical competition. Their unique mass-plate construction provides more available capacity and longer standby life in less board space—frequently at a cost saving.

Better packaging: To match your needs, we offer four configurations: (1) The sleeve-wrapped DK is compact—a 3.6-volt CMOS-backup unit takes, for example, just .71 sq. in. versus competition's 1.2 sq. in; (2) The Flat-Pack—less than 0.4"-thick—fits between boards on very tight centers; (3) The Mempac S is a pin-for-pin equal to G.E.'s Data Sentry, while providing 40% more capacity; (4) The encapsulated Safetronic takes even less board space than the Mempac S.

Higher capacity: Our 100 mAh memory-protection batteries provide 40% higher capacity than the competitive 60 mAh units they typically replace.

Better charge retention: Restricting internal losses, Varta mass-plate batteries, at 20°C, retain 63% capacity after five months versus 15% for cylindricals.

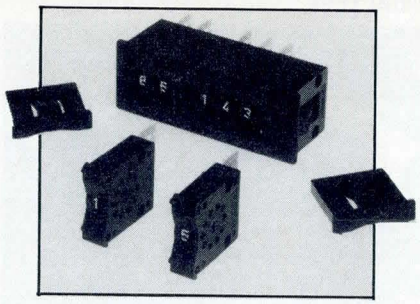
Lower charging rate: These batteries can be charged at rates as low as 1 mA (C/100); competition typically requires 4-7 mA. Charging power can be less.

Varta mass-plate batteries are available in 10-1000 mAh capacities. For information on Varta DK's, Flat-Packs, Mempacs or Safetronics please contact Varta Batteries Inc., 150 Clearbrook Road, Elmsford, N.Y. 10523. 914 592-2500.

VARTA

VARTA Batteries, Inc.
World-renowned battery specialists.

Snap-in thumbwheel switch

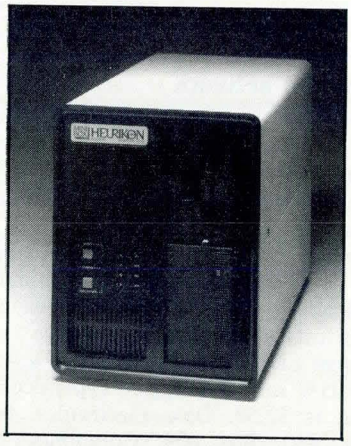


The Interswitch type V thumbwheel switch is a small front-mounted unit designed to snap into a front-panel cutout. It is held in place by springs that are parts of the end plates. Switches and end plates snap together so that no rods or nuts are required to hold the assembly together. Specs include 50-Vac or dc rated voltage, dielectric strength of 500 V, 75-mA contact rating for switching, and a 1-A thermal current. The switches are available in black or tan. **Interswitch,** 770 Airport Blvd, Burlingame, CA 94010. **Circle 317**

COMPUTERS

Unix workstation

Minibox is a multi-user Unix workstation based on the MC68000. It has a built-in C compiler, four or six Multibus card slots, single- or dual-floppy disk drives, and 31.2M to 140M bytes of Winchester storage (expandable to 420M bytes). Workstation is built around the HK68 micro that provides CPU, floppy disk drive controller, Winchester and tape interfaces, four to eight serial ports, and 750K bytes of RAM, all in two of the Multibus card slots. **Heurikon Corp,** 3001 Latham Dr, Madison, WI 53713.



Circle 318

FREE VAX

OR DATA GENERAL MV

If you're trying to support more than 4 programmers doing 8086- or 8080-family software with stand-alone microprocessor development systems, here's a way to increase your productivity 25%:

Buy our MicroSET-86™ or MicroSET-80™ software cross-development tools and a DEC VAX or DG MV/Family system to run them on. You'll save enough on your first major project to pay for the computer system.

Of course, if you already have access to a VAX (or MV or any IBM-compatible mainframe), you're that much further ahead.

People with experience in cross-development know it's the best way to tackle big software projects. And only First Systems' MicroSET gives you the industry's most complete, most powerful cross-development tools, plus your choice of five efficient systems implementation languages.

THE ONLY COMPLETE MULTILINGUAL DEVELOPMENT SYSTEM FOR THE 8086 FAMILY

MicroSET-86 lets you program in four powerful high-level languages: Pascal, C-86, FORTRAN-86, and PL/M-86.

An assembler is also available, although First Systems compilers generate such fast, compact code that you may find you have little need for it (benchmark data available on request). You also get a linker/locater that allows combining modules written in different languages.

Using our high-level Cross-Debugger to control execution on the target system, you can locate, fix, and re-test an erroneous line of code in a fraction of the time it takes using other methods. It's no wonder that MicroSET users routinely shave months off typical development schedules — while producing more reliable, more maintainable systems.

MicroSET-86 supports the entire 8086 family: 8086/8088/186/286 and 8087. It works with in-circuit emulators you may already own, and has a complete set of host-target communication programs and other valuable utilities not available elsewhere.

ANNOUNCING NEW LANGUAGE-COMPATIBLE 8-BIT TOOLS

First Systems now supports cross-development of 8080/8085/Z-80 software with MicroSET-80, consisting of PL/M-80 compiler, assembler, linker/locater, cross-debugger, plus utilities.

Request complete information today. And take the first step toward your own free computer.

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CIRCLE 136

Multibus and CP/M-86 system

Model 95/36A CP/M system is a family of Multibus CP/M-86 micro systems. Units come housed in a single integrated chassis providing three 8″ peripheral slots and nine Multibus card slots, or in a 2-part modular chassis, one with two 8″ peripheral slots and a second with nine Multibus card slots. Memory choices include 128K, 256K, or 512K bytes of RAM with parity. Drive options include one or two half-height 1M-byte floppy diskette drives and 10M-, 20M-, or 40M-byte Winchester disk drives. Universal development interface allows CP/M-86 systems to run Intel series III compilers and utilities. Std model is $8545. **Zendex Corp,** 6644 Sierra Lane, Dublin, CA 94568. **Circle 319**

Automated testing computer

The model 600 instrumentation computer features minicomputer architecture and performance. It uses the MC68000 with parallel processing and multitasking, 150K bytes of memory with parity std, and full high speed dot-addressable graphics. In addition, the unit has six slots for expansion, high speed GPIB, and enhanced Basic with more structured programming. The computer operates with dual 5¼″ double-density floppy (300K-byte) disks. Keyboard is detachable and includes a numeric pad with arithmetic functions. Programming and editing keys are std. The instrument is priced at $7950 with 384K bytes of memory. **Wavetek,** 9045 Balboa Ave, San Diego, CA 92123. **Circle 320**

SOFTWARE

C cross compiler

Combining the NS16000 with the C language, a C cross compiler eliminates the need for almost all assembly language programming. The software consists of a native code generator for the host development system, and a code generator for the NS16032. The package also includes a cross assembler that optionally produces complete assembly listings. In addition, a cross linker provides for construction of RAM/ROM combination systems. Initially available for the VAX/VMS, RSX-11M, Unix, and Idris host computer systems, the software costs $2500. **JMI Software Consultants, Inc,** 1422 Easton Rd, Roslyn, PA 19001. **Circle 321**

IBM PC cross assembler

Micro cross assemblers for the IBM PC and 8086/8088-based systems are available under both the MS-DOS (PC-DOS) and CP/M-86 operating systems. Cross assemblers allow small computers to be used as software development systems. The assemblers presently cover 11 microprocessor families: 6805, 6809, 1802/1805, 8048/8041, 8051, 6502, 6800/6801/6301, NEC7500, F8/3870, COP400, and Z8. Applications for the assemblers include machine tools, medical instruments, and navigational equipment. Software ranges in price from $250 to $500. **Avocet Systems, Inc,** 804 S State St, Dover, DE 19901. **Circle 322**

Compiler for 8080/8085 and Z80

The C cross compiler for the 8080/8085 and Z80 micros is a portable program that can be licensed in both source code and binary versions. Full C language is acceptable, as well as extensions such as identifiers of any length, all characters of nonexternal identifiers are significant, and arithmetic operation on Char data are performed without conversion to integers. Software permits executable code and constants to be located in one memory section while data are in another section. License fees will range between $2000 and $8500. **Microtec Research, Inc,** PO Box 60337, Sunnyvale, CA 94088. **Circle 323**

Structured macro cross assembler

REX-SMA/186 is a relocatable macro cross assembler software package supporting developments for Intel iAPX 86/87/88/186/188 microprocessor applications. Package contains five utility programs including a macro assembler, a cross linker, an absolute object-code locater, an object-code librarian, and a menu-driven computer interface. The assembler supports type checking, structures, records, and macro processing language. Additionally, it supports 8087 program development. Any object code modules and object-code libraries from Intel language processors can be linked and located using the cross assembler package. Software can be ordered to run on the PDP-11, LSI-11, or the VAX-11. Prices start at $3250. **Systems & Software, Inc,** 3303 Harbor Blvd, Costa Mesa, CA 92626. **Circle 324**

Network operating system

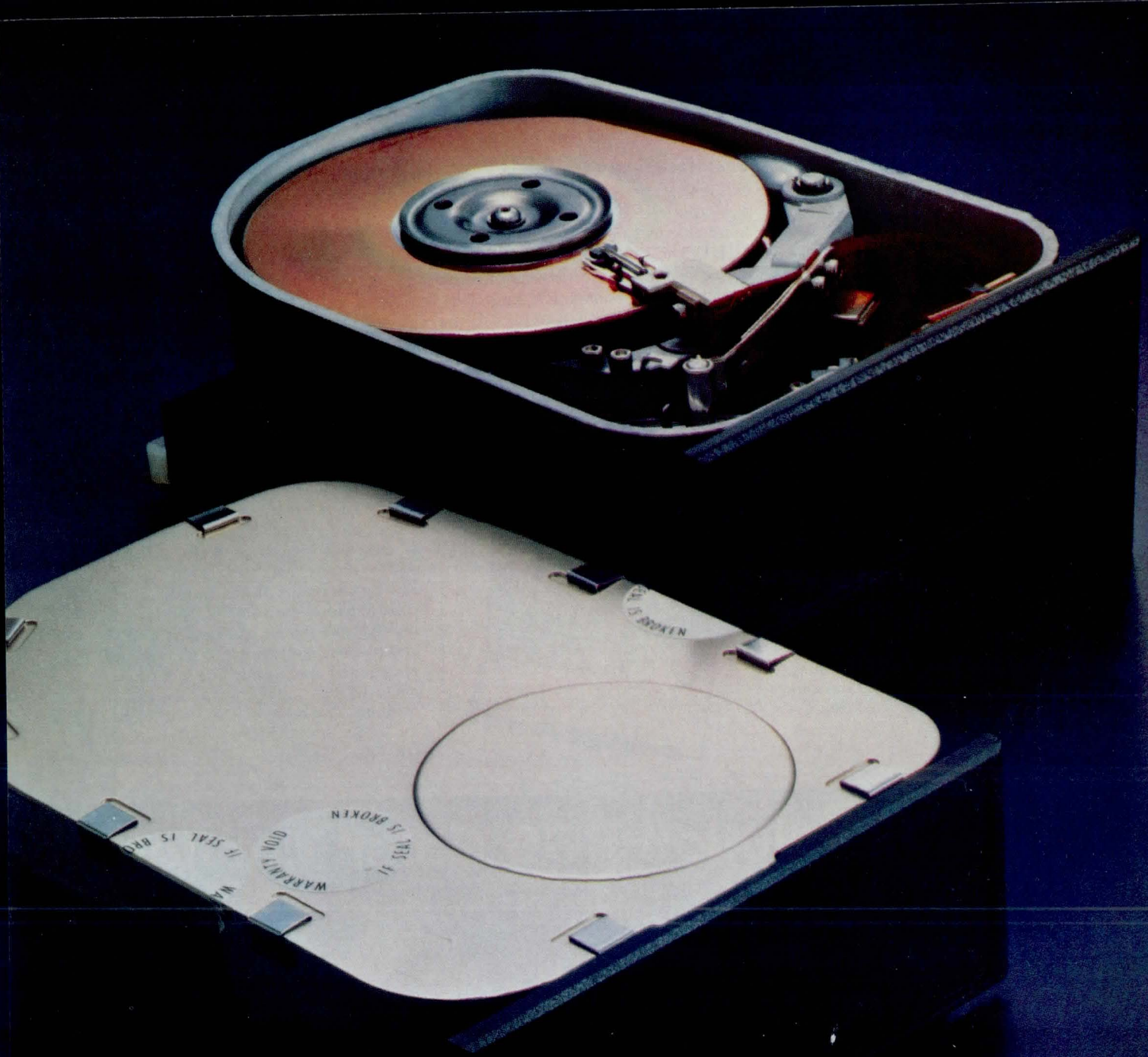
MmmOST 2.11 is an enhanced operating system for multi-user, multiprocessor network systems. Benefits include 8- and 16-bit personal workstations on the same network, enhanced print spooling, and tape backup capabilities for the TS 806/20 computer. Programs can run at the same time that files are being printed. Operating system provides simultaneous execution of CP/M and CP/M-86 application software. Each workstation contains its own CPU and RAM. System allows documents to be queued for printing with one command. Backup is also available. Operating system is priced at $200. **TeleVideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086. **Circle 325**

Software package combination

DT-DATS is an integrated software package that combines data acquisition, signal processing, and graphical display. It supports both menu-driven interactive programming and batch-type JOB processing as well as linkages to user written FORTRAN programs. Each separate activity is implemented as a program module that carries out one definable function. The 40 menu-driven programming modules prompt the user for required inputs. Many parameters have default values to speed programming. The software package's initial license fee is $15,000 for either RSX-11 or VMS operating systems. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 326**

CP/M-86 and MS-DOS compiler

Basic compiler can be used on 8086- or 8088-based systems. It runs under CP/M-86, MS-DOS, and IBM PC-DOS. SuperSoft Basic is compatible with Microsoft Basic and follows ANSI stds. It is a native code compiler, not an intermediate code interpreter, and its implementation is a superset of std Basic that supports numerous extensions. This Basic uses BCD math routines for greater accuracy and prevention of decimal round-off errors. Other features include four variable types, formatted output, long variable names, error trapping, and matrices with up to 32 dimensions. Compiler requires 128K bytes of memory (minimum) and sells for $300. **SuperSoft Inc,** 1713 S Neil St, PO 1628, Champaign, IL 61820. **Circle 327**



AT OTARI, THE DRIVE IS TO EXCEL

Otari has excelled in the design and manufacture of magnetic tape handling equipment for over twenty years.

Now Otari redefines excellence in another magnetic medium with the introduction of extraordinarily reliable, high performance 5¼" Winchester disk drives.

Otari's new series of drives, with capacities of 5, 10, 15, and 20 MB (formatted), feature a fast 77 msec average access time, microprocessor controlled servo positioning, low power consumption, and low weight.

Both full and half height drives are built at Otari's sophisticated production facilities in Japan, where the commitment to quality control is absolute. Every phase of production, from base plate machining and Class 100 clean room assembly to burn-in and final testing, is accomplished under one roof.

Standing behind the excellent specs are the Otari name and Otari resources: Resources that ensure a steady supply of the drives you need, when you need them. The name that sets the stardard for reliability and quality in small Winchester drives.

Call or write for full details about Otari's excellent new line of full and half height 5¼" disk drives.

Otari Electric Co. Ltd. 4-29-18 Minami-Ogikubo, Suginami-ku, Tokyo 167. Phone: (03) 333-9631, Fax: (03) 331-5802, Telex: J26604

Otari Singapore Pte., Ltd. Golden Mile Complex, 5001 Beach Rd. #03-50, Singapore 0719 Phone: 294-5370, Telex: RS36935 OTARI

OTARI®

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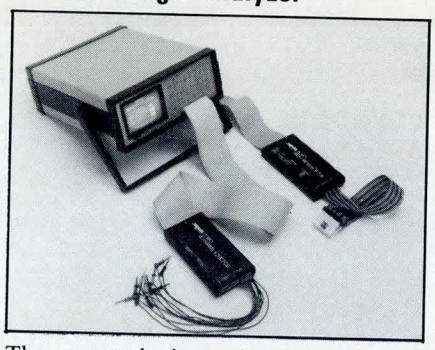
CIRCLE 137

Low cost logic analyzer

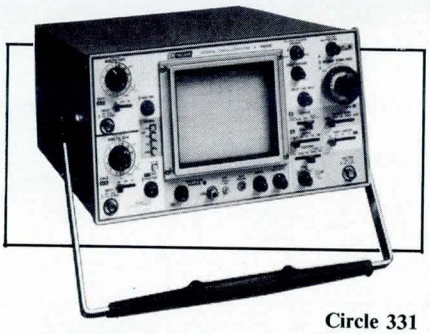


The ML4100 logic analyzer operates at speeds up to 100 MHz, has data widths up to 32 channels, and memory depth up to 8k samples/channel. Analyzer has a built-in, 5″, green screen CRT on which 12 channels of timing diagram can be displayed. The state display can be formatted and reformatted to achieve any digit combination in binary, octal, hex, or ASCII. Data and clock qualifiers can trigger delay of up to 50k clocks. Special pods provide 1-clip connection to most micros. Device is priced at $2195. **Arium Corp,** 1931 Wright Circle, Anaheim, CA 92806.

Circle 328

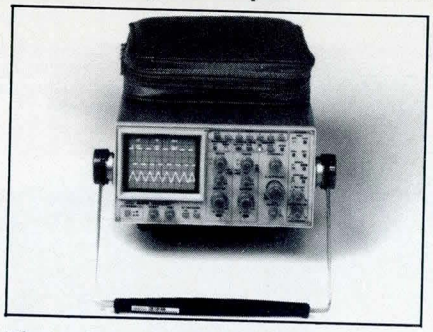
Dual-trace/time base scope

Model 1540 oscilloscope features 5-mV/div vertical sensitivity to 40 MHz (selectable to 1-mV/div sensitivity to 15 MHz). The dual-trace, dual-time base device includes a 5″ rectangular CRT with graticule, scale illumination, and 12-kV accelerating voltage. Trigger sources are CH1, CH2, line, external, and V mode for displaying two signals unrelated in frequency. Other features are front-panel X-Y operation, Z-axis input, sum and difference capability, gate and sweep output, and single-sweep operation. Scope is priced at $950. **B&K Precision/ Dynascan Corp,** 6460 W Cortland Ave, Chicago, IL 60635.



Circle 331

Portable digital scopes



The 336 is a combination nonstorage and digital storage oscilloscope. It measures signals to 50-MHz equivalent time bandwidth (in store mode) with memory length of 8 x 1024. In nonstorage mode it measures signals to 50-MHz bandwidth for analyzing and storing low rep rate signals on the digital channel. Micro control allows users to add, subtract, or multiply the signals of channels 1 and 2 and to calculate rms, pk to pk, and avg of acquired waveforms. The scope has a menu system and alphanumeric CRT readout. The price of the 336 is $4500. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 333

High Resolution RGB Color Monitor

CRT	12″ Diagonal, 76 Degree, in-Line Gun, .31 mm dot pitch black matrix, non-glare surface *(NEC 320CGB22)*
Input Signals	R,G,B channels, Horz Sync, Vert Sync, Intensity — all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal – 15.75 KHz Vertical – 60 Hz
Misconvergence	Center: 6 mm max, Corner: 1.1 mm max
Display Size	215 mm X 160 mm
Resolution	Horizontal – 690 dots Vertical – 240 lines *(not interlaced)* 480 lines *(interlaced)*

OEM inquiries invited, contact PGS for complete technical data, pricing and delivery.

80 character display

PGS **Princeton Graphic Systems**

1101-I State Road ☐ Princeton, New Jersey 08540 ☐ (609) 683 1660 ☐ TLX: 685 7009 PGS Prin.

CIRCLE 181

THERE IS MORE THAN ONE GOOD REASON TO CALL HEURIKON

Make HEURIKON your source for Multibus microcomputers and sytem components.

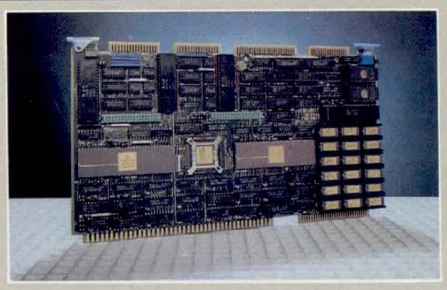
Since 1972 Heurikon has been working hard to make life a little easier for those who "put it all together." Powerful Z-80™ and MC68000™ based Multibus™ microcomputers like MLZ-92A and HK68 have helped Heurikon customers find economical solutions for their problem applications.

MLZ-90A single board microcomputer with nine byte-wide memory sockets for use with RAM or ROM (AM9511 and floppy disk drive controller optional).

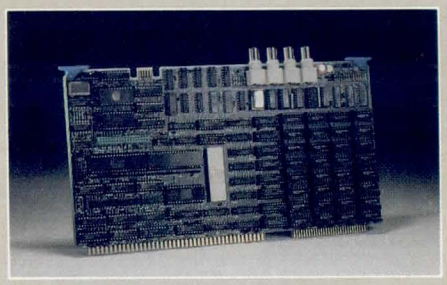
MLZ-91A single board CP/M™ system with on-card floppy disk drive controller, winchester interface, optional AM9511, streamer tape interface, two serial ports, one parallel port, 64K bytes RAM with parity, two EPROM sockets, and GPIB CONTROLLER.

MLZ-92A single board CP/M™ system with four serial ports on-card, floppy disk drive controller, winchester interface, optional AM9511, Centronics printer interface, 64K bytes of RAM with parity, and two EPROM sockets.

MLZ-93A single board CP/M™ system with 128K bytes of dual ported RAM, four EPROM sockets, floppy disk drive controller, optional AM9511 and powerful serial port features including SDLC and HDLC protocol support and modem controls.



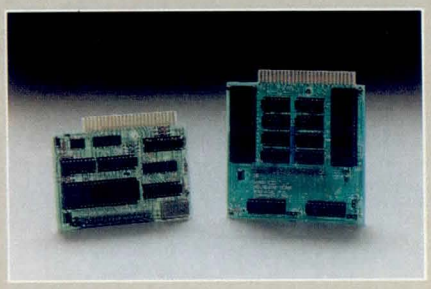
HK68™ powerful and versatile single board UNIX™ or CP/M-68K™ system with MC68000 CPU, MMU, quad channel DMA, four serial ports, 128K or 256K bytes of on-board RAM with parity (expandable to 1M byte on-board!), and two iSBX™ connectors for I/O expansion.



MLZ-VDC intelligent 640 x 480 x 4 color graphic controller based on the NEC 7220 controller chip with on-board Z-80 CPU, DMA controller, and user definable FIFO interface to Multibus.™ Users may display up to 16 colors from a 4K palette. Up to 1024 x 1024 x 3 interlaced also available.

iSBX Expansion Models
Heurikon also stocks iSBX™ modules for I/O expansion on its HK68 and MLZ-VDC. These modules may be used on any other board complying with Intel iSBX specifications.

Presently available are the SBX-FDIO floppy disk controller module and the SBX-SIO serial port expansion module.



The SBX-FDIO can control up to four single or double sided, single or double density 5¼ inch or 8 inch floppy disk drives. A software toggle allows both 5¼ inch and 8 inch drives to be intermixed on the same cable!

The SBX-SIO is a quad serial port expansion module utilizing Zilog SCC controller chips with built in baud rate generators. The SBX-SIO is available in synchronous and asynchronous models.

Systems
Heurikon also supplies completely integrated systems with your choice of CP/M-80™, MP/M-80™, CP/M-68K™, and "Berkeley enhanced" Unix operating systems.

Systems are available with four, six, and fourteen slot enclosures with 5¼ inch or 8 inch dual floppy or floppy winchester drive combinations.

HEURIKON CORP.

3001 Latham Dr. Madison, WI 53713 Telex 469532

See Tekelec Airtronics Hall 14 Booth 14005/14102

Call Heurikon Direct 1 800 356•9602 In Wisconsin 1 608 271•8700

Z-80 is a trademark of Zilog Corp. Multibus & iSBX are trademarks of Intel Corp. UNIX is a trademark of Bell Lab. CPM 68000 is a trademark of Digital Research. HK 68 is a trademark of Heurikon Corp.

CIRCLE 139

Announcing
Retro-Graphics®, DEC ReGIS, and Tek 4010/4014.

ReGIS™ or 4010/4014 graphics capability?

The one, Tektronix® 4010/4014, is the industry standard for scientific and engineering graphing. While the other, ReGIS, developed and fully backed by DEC™, is a front-runner both in business graphing — and as a protocol with a big future.

Until now, developing graphics meant a choice between the two.

Retro-Graphics makes the decision for you.

Our DQ650-Series Retro-Graphics — with new ReGIS option — now delivers both 4010/4014 and ReGIS compatibility. In 800-by-480 resolution. On DEC's family of VDTs, including the VT100™ and VT102™. With full backing by DEC field service.

In short, with your Retro-Graphics updated DEC terminal, you have a bit-map graphics display that is compatible with your existing Tek® software library or any operating program that contains ReGIS protocol.

Retro-Graphics. Now backed by DEC field service.

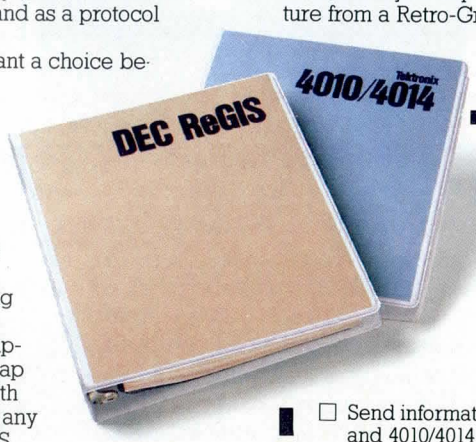
Installed in more than 25,000 sites, Retro-Graphics has been delivering Tek features to DEC terminals for years.

In fact, the popularity of Retro-Graphics is so widespread, domestic DEC field service is offering a variety of service programs for Retro-Graphics updated DEC displays.

This means the level of support available for your upgraded DEC terminal is now superior to any offered by DEC-terminal emulators and independent graphics-terminal manufacturers.

Simply put, the only decision to make is Retro-Graphics. With ReGIS and 4010/4014 compatibility and DEC field support.

Call today or clip and mail the coupon for the full picture from a Retro-Graphics dealer.



CD10/83

CLIP AND MAIL TO:
Digital Engineering
630 Bercut Drive
Dept. 217
Sacramento, CA 95814

☐ Send information on Retro-Graphics with ReGIS and 4010/4014 compatibility

☐ Arrange an informative demonstration

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

TELEPHONE ( ) _____

See Us At Comdex Booth #2236

DIGITAL ENGINEERING

630 Bercut Drive, Sacramento, CA 95814
(916) 447-7600 Telex: 910-367-2009

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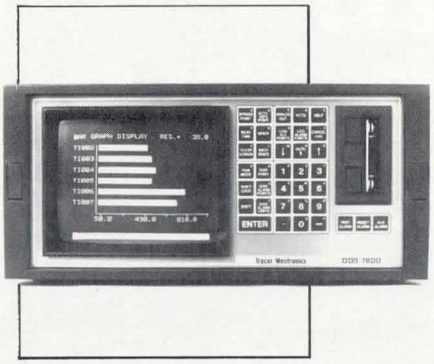
CIRCLE 140

Paperless recorder

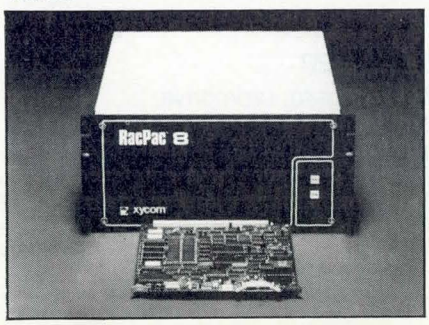


DDS7800 paperless recorder is a microprocessor-based data acquisition system. It includes a 9″ CRT, dust-resistant keyboard, and menu programming. Data cartridge mass storage and software provides alphanumeric tag numbers, bar graphs, math functions, 32-char descriptive phrases, and four levels of alarm/point. The recorder uses a peripheral printer to record data rather than having dedicated stripchart recorders. RS-232-C and 20-mA current loop interfaces are available. **Tracor Westronics**, 2441 Northeast Pkwy, Fort Worth, TX 76106.

Circle 336

Two industrial control systems

Two micro systems, designated 3940 and 3941 RacPac Industrial Basic II, are suitable for applications requiring rapid system start up. Both systems include the 1874+ board, RS-232-C communication adapter, 2-channel communication controller cable, and documenation. Onboard CPU contains 80K bytes of user memory. In addition, the systems have a battery-backed time-of-day clock for realtime operations, an APU, and two serial communication channels. Industrial Basic II is a programming language with extensions that supports interrupt and power-fail handling, I/O commands, and flexible program and data storage. Both systems are expandable and support additional 180+ bus boards. **Xycom, Inc**, 750 N Maple Rd, Saline, MI 48176.



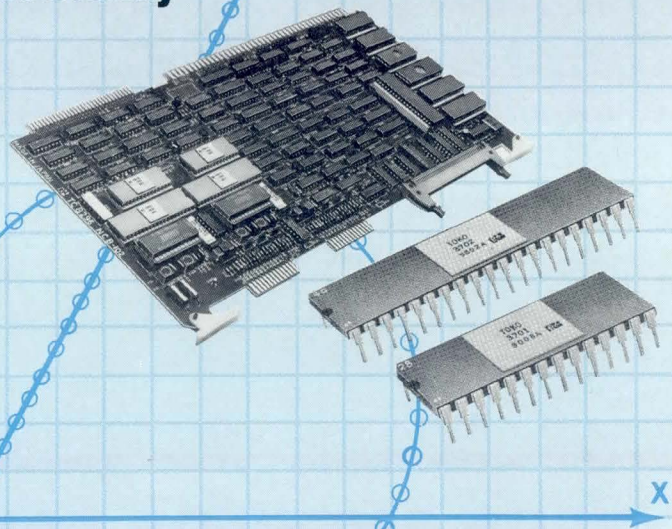
Circle 337

Industrial single-board computer

The PPM 86-50 is a Multibus single-board computer for industrial control. Features include a 5-, 8-, or 10-MHz 8086 or 80C86 max mode micro, a CP/M-86 1.1 operating system in silicon, 128K bytes of EPROM in 32K-byte increments, and 128K bytes of CMOS static RAM in 16K-byte increments. In addition, there are 96 buffered I/O lines, a 19.2k-baud (max) RS-232-C async port, and a realtime calendar/clock. For number crunching, the proposed IEEE floating point standard is implemented in hardware. Base price for the 5-MHz version is $695. **PPM Inc**, 23945 Mercantile Rd, Cleveland, OH 44122.

Circle 338

Toko America's Numerical Control Board – LSIs Combine For Improved CPU Efficiency



Advanced Numerical Control Module NCB-102 – using LSIs KM3701/KM3702 – offer easy, low-cost development of a wide variety of NC systems . . .for function generation; positioning control.

- Directly pin compatible with IEEE 796; 8 bit microprocessor monitors multibus lines, drives interpolation pulse generator when addressed.
- Linear and circular interpolation
- NCB-102 eliminates interpolation logarithmic development . . . reduces softwear, debugging time & costs.
- KM3701 LSI efficiently generates interpolation pulses for X and Y axes as instructed by CPU.
- KM3702 precisely monitors input pulse; generates required pulses for D/A converter.
- Simultaneous 2-axis control . . .3 and 4 axes control possible.
- Built-in microprocessor, automatic acceleration/deceleration control eases overall operation.

Send for complete information on NCB-102 module – Circle 171

For data on LSIs – Circle 176

TOKO AMERICA INC.

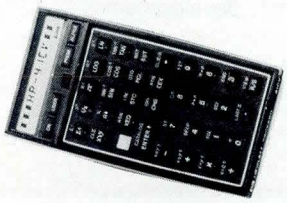
5520 W. Touhy Ave. Skokie, IL. 60077 Tel: 312/677-3640 Telex: 23-0724372

YOUR ANSWERS TO THESE QUESTIONS HELP US SERVE YOU BETTER

YOUR ANSWERS ARE IMPORTANT. The results of these surveys help our editors select topics, features and technical data that will be on target with your design activities. Your inputs also alert manufacturers to your needs and can result in the development of product speeds, ranges, capacities, and other specs that you require.

YOUR ANSWERS CAN ALSO WIN YOU A VALUABLE PRIZE!

Each questionnaire returned gives you a chance to win a special prize. Drawings are made after each issue, with a grand prize drawing at year end.



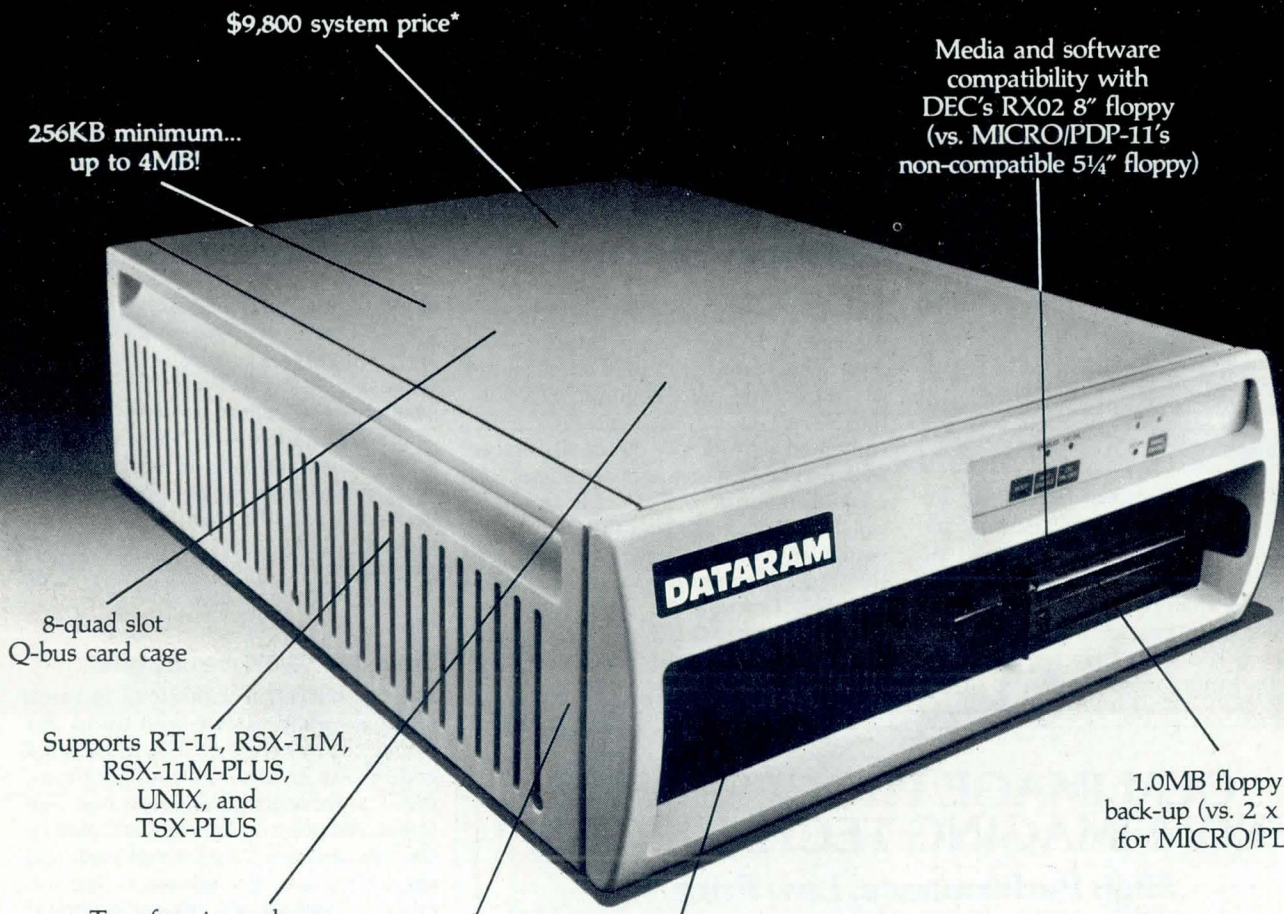
***MONTHLY DRAWING* — HP 41CV PROGRAMMABLE CALCULATOR**

The HP 41CV offers advanced problem-solving power yet is easy to use. Communicates in words as well as numbers. Can be programmed to meet your specific needs. Fifty-eight popular functions, 130 total functions in program library. Memory expandable to almost 6,500 bytes.

***ANNUAL DRAWING* — HP 85 DESK TOP COMPUTER**

This portable (20 lb.) unit includes an alphanumeric keyboard, tape drive, thermal printer, built-in 56K byte memory, CRT screen, and 150 built-in BASIC language commands. You can add peripheral and software packages to expand system capability. A $2800 value!

Like DEC's.



Only better.

CD/10/83

By paying a little more than you would for a MICRO/PDP-11, you can get a lot more! Like an 8" RX02-compatible floppy. 10MB or 20MB 5¼" Winchester and space for a 5¼" cartridge tape. Two fans provide push-pull air flow in the card cage area.

The A22 with LSI-11/23, 256KB, 10MB Winchester, and 8" floppy is only $9,800. 30-day delivery.

For more information, forward this coupon to us, or, for faster response, call (609) 799-0071.

☐ Send information. ☐ Contact me immediately.

Name

Company

Address

City State Zip Phone

Return to:
Dataram Corporation, Princeton Road, Cranbury, NJ 08512

*$9,800 is single-quantity domestic price for A22 with LSI-11/23, 256KB, 10MB Winchester and RX02-compatible 8" floppy.

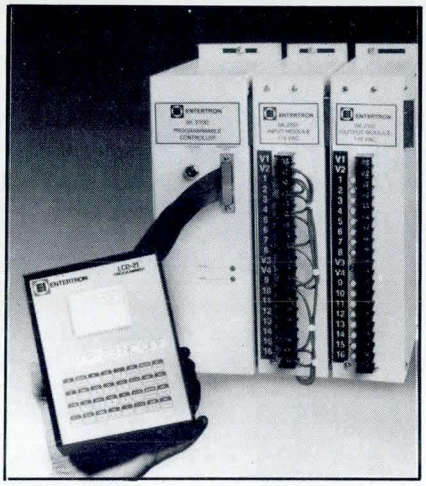
DEC, LSI-11, PDP, RSX, and RT-11 are trademarks of Digital Equipment Corporation.
TSX-PLUS is a trademark of s&h computer systems, inc.
UNIX is a trademark of Bell Laboratories.

CIRCLE 141

DATARAM

Dataram Corporation □ Princeton Road □ Cranbury, New Jersey 08512 □ Tel: 609-799-0071 □ TWX: 510-685-2542

Controller and programmer



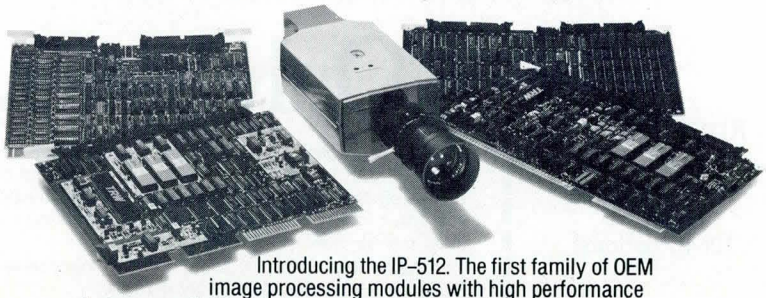
Programmable controller (model SK-2100) and programmer (model LCD 21) are designed for electronic control of sequential operations. Modular design features a mainframe for 16 plug-in modules. Each module has 16 optically isolated I/Os on one strip for a total of 256 I/Os in any mix. Controller offers arithmetic capabilities (add and subtract), numerical data handling, 240 timers/counters, and shift registers in definable range. Programmer features a LCD for ladder diagram, programming in relay symbols, and membrane keyboard. **Entertron Industries Inc,** 3857 Orangeport Rd, Gasport, NY 14067.
Circle 339

Motion control Apple boards

Two plug-in boards for the Apple II/IIe allow the computers to be used in industrial motion control applications. The A6 T/D board provides high speed pulse generation and pulse counting capabilities. The device can then interface to the computer with stepper motor drivers as well as receive rotary encoder pulses for position indication. The A32 is an opto-isolated digital I/O board that can be used in any combination of I/O channels. Both boards come with utility programs that link functions to Basic software. **Rogers Laboratories, Inc,** 2710 Croddy Way, Santa Ana, CA 92704.
Circle 340

OEM IMAGE PROCESSORS FROM IMAGING TECHNOLOGY.

High Performance, Low Price.



Introducing the IP-512. The first family of OEM image processing modules with high performance features available only on systems costing much, much more.

The IP-512 is a real-time image processor that's plug compatible with the INTEL MULTI-BUS and DEC Q-BUS.

It interfaces with any standard video source, stores images in single or multiple **512×512** frame buffers with up to 24 bits/pixel and includes a **pipeline ALU** for real-time image averaging, summation, subtraction and convolutions.

The modules include programmable I/O Transformation Tables and provide for B&W and RGB output.

Specialized applications include **image analysis, factory inspection, medical imaging, industrial radiography, robotic vision** and **teleconferencing**, among others.

For details call, (617) 938-8444. Or write to:
Imaging Technology Incorporated
400 West Cummings Park, Suite 4350, Woburn, MA 01801

IMAGING
Imaging Technology, Inc.

*MULTI-BUS is a trademark of INTEL CORP.
*Q-BUS is a trademark of Digital Equipment Corp.

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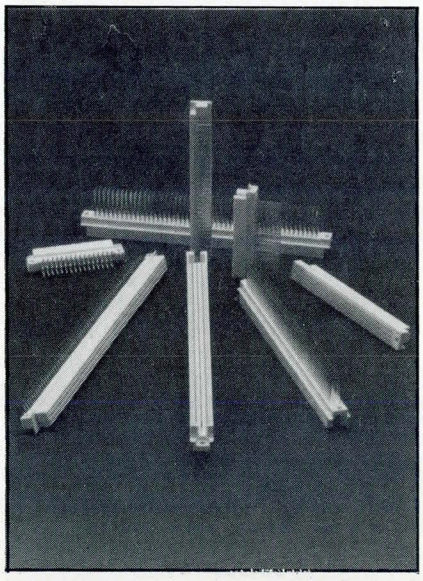
INTERCONNECTION & PACKAGING

Shielding compound

Developed for emi/rfi shielding, the Meta-Shield 1234 is conductive coated for shielding plastic-molded housings. The material is formulated with a corrosion- and oxidation-resistant copper particulate. It adheres to bondable substrates and coats structural foam as well as dense molded plastics, and is polycarbonate compatible. Attenuation values and humidity resistance exceed those attainable with other solvent paints or lacquer systems based on nickel or other conductive particulates. Price is $75 to $125 and it is available in various packaging sizes. **Mereco, div of Metachem Resins Corp,** 1505 Main St, West Warwick, RI 02893.
Circle 341

Expanded VG/DIN connectors

VG/DIN connectors with metal to metal reliability are available with up to 201 contacts (three rows of 67). In both std and inverse gender DIN configurations, they feature select plating, low insertion forces, and positive alignment and mating. Connectors meet VG 95324, DIN 41612, and MIL-C-55302 stds. In addition to typ termination options, the inverse expanded DIN is offered in a preassembled compliant pin connector with application tooling. **Elco Corp, Connector Div,** Huntingdon Industrial Park, Huntingdon, PA 16652.



Circle 342

Don't take no for an answer!

WINCHESTER CARTRIDGE DISK DRIVES FOR MICROCOMPUTERS

Feature	**DMA Systems 5¼" Drives**	3.9" Drives	Other 5¼" Drives
Now in production	yes	no	no
Data interchange	yes	no	no
Contamination control	yes	no	no
Retractable heads	yes	no	no
Standard cartridge	yes	no	yes
40 ms access time	yes	no	no
5 Mb capacity (formatted)	yes	yes	yes
Capacity growth capability	yes	no	no
Removable-only drive	yes	yes	yes
Fixed/Removable drive	yes	no	no

A comparison of Winchester cartridge disk drives shows there's really no comparison.

Only DMA Systems allows you to interchange data between drives.

Only DMA Systems has a unique retractable head that ensures data integrity by never touching the disk.

Only DMA Systems has a self-sealing clean air system that prevents contaminants from reaching the data—even after thousands of insertions.

And only DMA Systems gives you a choice of fixed/removable or removable-only drives. Both models match mini-floppy front panel dimensions and adapt to existing 5¼" Winchester drive controllers.

What's more, DMA Systems is the only manufacturer delivering microcomputer Winchester cartridge disk drives.

But DMA Systems drives don't just outperform other cartridge systems. They outperform all other types of microcomputer backup.

Consider the alternatives...

Floppies have low capacity, poor reliability and slow access time.

Streamers are unreliable and can't provide random access.

There's only one drive manufacturer who can answer "yes" to all of your needs: DMA Systems.

For more information write DMA Systems, 601 Pine Avenue, Goleta, CA 93117. Or call (805) 683-3811, Telex 658341.

DMA SYSTEMS

The Removable Winchester Company.

CIRCLE 142

Micro-based interface

Q-3024 interface unit uses the ASCII format over a serial link to interconnect analog inputs to a serial-ported mainframe or small computer. Basic can be used for control programming in almost every case. Unit has two 12-bit analog inputs coupled with four digital outputs to monitor industrial processes, motor control positioning, and lab experiments. Additional space in the interface allows stand-alone applications with any mix of analog inputs and serial/parallel digital outputs. Units sell for $395. **Quasitronics, Inc,** 211 Vandale Dr, Houston, PA 15342.
Circle 343

HP-compatible comm interface

Designed for use with Hewlett-Packard 85, 86, and 87 computers, the COM-80 communications interface provides cost-efficient data communications. The interface features a multiport enabling the user to collect, edit, store, and forward data from an ASCII device to a host computer without recabling. One card allows async and bisync communications on multiple ports; three serial devices can be interfaced without modification. Std baud rates are 110 to 9.6k and multicable configurations are available. With the interface, users can emulate Hasp workstations via 2780/3780 terminal emulation. **Corporation for Distributed Systems,** 17440 Dallas N Pkwy, Dallas, TX 75252.
Circle 344

Interface card

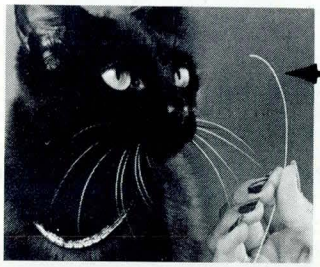
The BUS-65400, a dual redundant remote terminal unit card assembly, complies with MIL-STD-1553. The card contains isolation resistors, BUS-25679 transformers, BUS-63115 transceivers, and an LSI chip set. The LSI chip set includes encoder/decoders, protocol sequencer, and a 32-word FIFO. Dual watchdog timeout circuits and a clock generator are also included. The device interfaces directly to a dual redundant MIL-STD-1553B MUX BUS on one side and a subsystem parallel tri-state data highway on the other. The price is $2499. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.
Circle 345

STD bus card series

Five low power CMOS STD cards (series MSI-C000) are designed for industrial applications. The MSI-C850 CPU card is based on the NSC800 and provides up to 32K bytes of PROM or RAM using 27C16-, 27C32-, or 27C64-type memories. Card is available for 1-, 2.5-, and 4-MHz clock frequencies. MSI-C764 provides 64K bytes of PROM or RAM and optional battery backup for RAM. I/O cards include the MSI-C540 with 24 general purpose programmable I/O lines and selectable output buffer ICs. A 50-pin I/O connector is compatible with industry std. Additional cards provide parallel I/O. Prices range from $150 to $350 for the various modules. **Microcomputer Systems, Inc,** 1814 Ryder Dr, Baton Rouge, LA 70808.
Circle 346

Special Edition Preview—
Portable computers—in late October.

ZEUS SUB-LITE-WALL™ HEAT-SHRINK TUBING



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THE WORLD'S SMALLEST TUBING FOR ADVANCED MICRO-TECHNOLOGY!

Inert! Highly dielectric. Slippery. Abrasion-proof. Permanent. Stands temps to 500°F. Uniform ID's down to .001"; thin-walls to 2.5 mils. Heat-shrinkable or permanently extruded around wires to AWG 44. Available expanded to heat-shrink ratios of 4 to 1 around irregular shapes, delicate equipment, to encapsulate against damage or corrosion. Special requirements welcome. IF YOU CAN USE IT, ZEUS MAKES IT!

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CIRCLE 143

LITHIUM BATTERY HOLDERS IN 2 STYLES

COIN HOLDER
BH906*

Fits all coin type cells up to 23mm x 3.2mm.

CYLINDER HOLDER
BH2/3A*

Fits all standard type cells style 2/3A. (Dustcover available).

Memory Protection was Never Easier.

Now you can permanently solder MPD's new coin or horizontal battery holder right on your PC board. Standard 3 volt lithium cells for reliable memory back-up systems clip right in...

• Sturdy, high-temp UL94V-0 Valox® material • Stainless steel nickel plated contacts • Easy insertion and removal of batteries • Efficient, economical • *Custom battery holders available on request.*

*Patent Pending

For all the details, call or write today.

Memory Protection Devices Inc.

320 Broad Hollow Road, Farmingdale, NY 11735 • 516-454-0340

CIRCLE 144

LEXIDATA·3700

The Lexidata 3700 has the speed and performance you've come to expect from the leader in high resolution displays.

In terms of speed, the 3700 writes in pixel blocks automatically (e.g. for fills and horizontal vectors). This is continuous speed, not burst speed, at 42 million pixels per second.

Its pixel-by-pixel rate is also continuous and fast. Fast when you're generating vectors. Fast for individual pixel update–crucial for imaging applications.

This speed is augmented by state-of-the-art 1280 x 1024 color at a flicker free 60hz refresh.

In terms of performance, the 3700 comes standard with Writable Control Store (WCS), enabling the user to implement his own high speed routines. Additionally, WCS also gives direct access to the main processor, so even complex functions run fast. There's also separate storage for over 1000 characters in user-definable fonts.

42 million pixels per second

Remember, too, that the 3700 stems from the 3000 family, the most popular high-performance line ever developed. The 3700 is a *complete* performance package offering speed and features that live up to your expectations.

The Lexidata 3700. Fasten your seat belts.

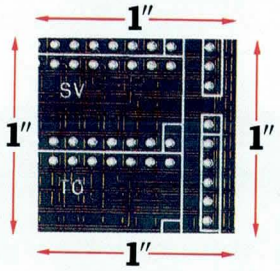
For quick response call 1-800-472-4747 (in Massachusetts, call 617-663-8550) or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

LEXIDATA

The clear choice in raster graphics.

CIRCLE 167

GIVE US AN INCH. WE'LL WIRE A MILE.



The board section above is for a Burroughs computer using TTL and ECL devices, some packaged in pin grid arrays. 4 mil wire is routed on a 14 mil grid, with three wires between holes. Component density exceeds 2.5 DIPs per in. sq. (14-pin DIP equivalent).

You may be facing stiff technical challenges like this as you design your next generation of product. Challenges that are difficult to meet using traditional circuit board technologies.

That's when Multiwire® can help. We've successfully solved a variety of customer problems involving high-speed logic applications in advanced Schottky and ECL, high pin-count packages and dense component packaging.

At our Advanced Manufacturing Group, we've provided boards for surface mountable devices and employed alternative substrates such as metal core and polyimides to meet special customer needs.

Multiwire works with you from your initial design stage to finished boards. We can design your board from a schematic or several other design options. So we provide single-source responsibility for your project from start to finish. And we deliver boards routinely in four to six weeks.

We'd like to send you more information on Multiwire. Just return the coupon below or call our nearest facility.

MULTIWIRE
10 Andrews Rd., Hicksville, NY 11801

- ☐ Please send me your 8-page brochure.
- ☐ Please send information on using Multiwire in ECL design.
- ☐ Please send more information about the Advanced Manufacturing Group.
- ☐ Please call me.

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MULTIWIRE® DIVISION
KOLLMORGEN CORPORATION

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MULTIWIRE/WEST 3901 East La Palma Ave., Anaheim, California 92807 (714) 632-7770; MULTIWIRE/ADVANCED MANUFACTURING GROUP 10 Andrews Rd., Hicksville, NY 11801 (516) 938-2000
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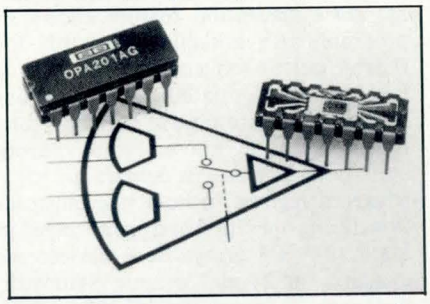
CIRCLE 145

Switchable input op amp



A precision, low power op amp, the OPA201 has two switchable input stages. Switching function is controlled by a digital TTL signal. Performance specs include 100-μV offset voltage, 1-μV/°C max offset voltage drift vs temp, 25-nA bias current, and < 500-μA max current consumption. The op amp is suitable for instrumentation and data acquisition applications. It is housed in a 14-pin hermetic DIP. Prices, in 100s, range from $8.50 to $16.50, depending on grade. **Burr-Brown Corp, Analog Products Div,** PO Box 11400, Tucson, AZ 85734.
Circle 347

Analog to digital converter

The MC14442 28-pin CMOS parallel bus-compatible ADC has a 32-machine cycle conversion and allows either 11 analog or 6 digital inputs. Resolution is a full 8 bits with a relative accuracy of ±½ LSB across voltage. The converter operates from a single 5-V supply and provides interface to the MPU data bus used by all M68XX family parts. It has a 32-μs conversion time at $f_E = 1$ MHz, TTL-compatible inputs, and is fully programmable. Parts are priced in 100s at $14.23 in plastic and $18.41 in ceramic. **Motorola Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 348

A 16K, 35-ns static RAM

IMS1400-35 16K x 1 MOS static RAM has a 35-ns access time and dissipates 660-mW max active power, 110-mW max standby. Manufactured with N-channel MOS, the device can compete with the more expensive and power-hungry ECL devices. The chip is available in plastic and ceramic DIPs and ceramic chip carriers. Prices for the devices in 100-piece quantities are $23.50, $28.20, and $33.80, respectively. Lead times range from eight weeks for plastic and ceramic DIPs to 12 weeks for ceramic chip carriers. **Inmos Corp,** PO Box 16000, Colorado Springs, CO 80935.
Circle 349

Fast low power static RAM

HM-65162 is an async 2K x 8 static CMOS RAM with access times as low as 55 ns. Control signals include chip enable, write enable, and output enable for micro applications. Standby power dissipation is 550 μW (100-μA standby current). Enable power supply currents are guaranteed at 70/80 mA max. Gated address, data, and control line inputs eliminate pull up/down resistors. These inputs also lower the operating current. In quantities of 100 cerCIPs, the chip ranges from $12.36 to $97.42. **Harris Corp, Semiconductor Sector,** PO Box 883, Melbourne, FL 32901.
Circle 350

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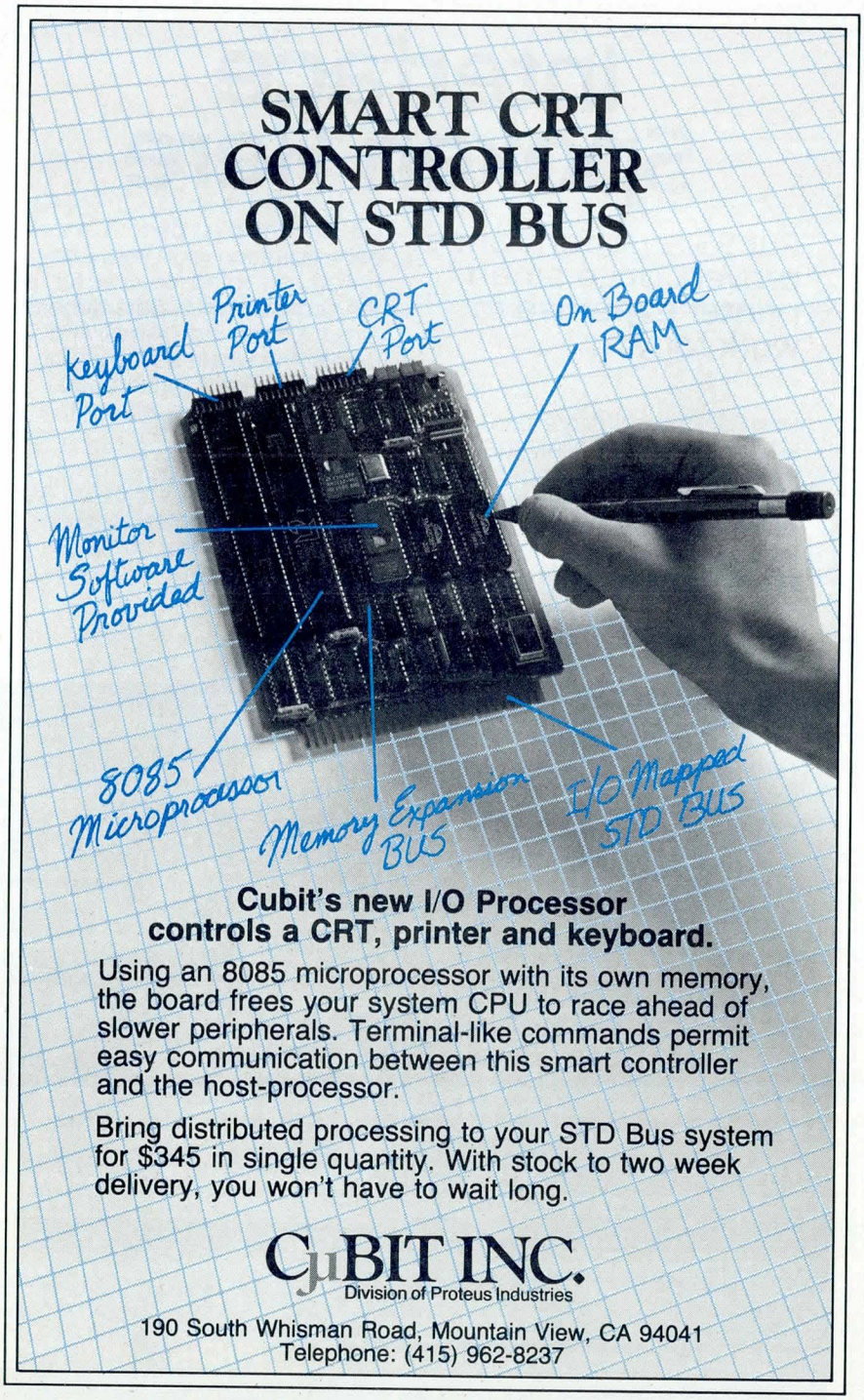
CIRCLE 146

Uncommitted array

Model TMG5001 uses low power, CMOS uncommitted array technology with high voltage open drain transistors. The monolithic array uses 5- to 10-V silicon-gate CMOS logic and 300-V lateral-DMOS output transistors. The device contains 338 uncommitted gates (169, 2-input and 169, 3-input units) and 40 prewired flip-flops with eight open drain transistors. The transistors feature 750 Ω ON resistance and 2-mA drain current, while the CMOS logic has a 5-ns (typ) gate delay. Additional array features are 18 CMOS or TTL buffers, and seven groups of P- and N-channel high impedance transistors. Inputs are TTL and CMOS compatible and the 37 I/O pads have static protection. **Telmos Inc,** 740 Kifer Rd, Sunnyvale, CA 94068. **Circle 351**



Synchronous PROMs

The 63RS881A and 63RS881 PROMs provide clock-to-output times of 15 to 25 ns (worst case) and setup times of 30 to 35 ns. An initialization feature allows 16 programmable initialization words for flexible startup sequencing. These words can force or alternate interrupts, establish a known state at power up, or return the CPU to a known state during operation. The PROMs contain an edge-triggered register to hold microinstruction during operation and are arranged in a std 1024 x 8 array. Both devices are available in 24-pin ceramic Skinnydip packages. In quantities of 100 to 999, prices range from $22.05 to $30.45. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050. **Circle 352**

Nonvolatile fuse link PROM

Configured as 2K x 8, the HM-6616 is a CMOS 16K-byte fuse link PROM. The chip provides a 2716-type industry std compatible pinout to allow existing system upgrade where high speed and low power are critical. Onchip latches eliminate need for extended latches in nonvolatile memory design. The PROM uses the scaled SAJI IV CMOS process which allows high speed operation with a 120-ns chip enable access time. Polysilicon fuses for data storage provide permanent, stable storage over a wide temp range. A 24-pin cerDIP, slimline cerDIP, and 32-pad LCC packages are available. In quantities of 1000, prices range from $18 to $54. **Harris Corp, Semiconductor Sector,** PO Box 883, Melbourne, FL 32901. **Circle 353**

Three static RAM versions

A 16K-byte CMOS static RAM is available in three different pinouts allowing interface options. Models CDM6116, CDM6117 and CDM6118 differ in the function of pin 20. On the 6116, the pin is an output enable that gates only the output buffers and not the input addresses. On the 6117, the pin is a chip select that deselects the memory device but does not inhibit precharge or power. On the 6118, the pin is a chip enable that gates the addresses and controls the device's total power consumption. Devices have a max access time of 200 to 250 ns, and a max standby current of 30 to 100 μA. In quantities of 1 to 99 pieces, prices range from $12.93 to $14.85. **RCA, Solid State Div,** Rte 202, Somerville, NJ 08876. **Circle 354**

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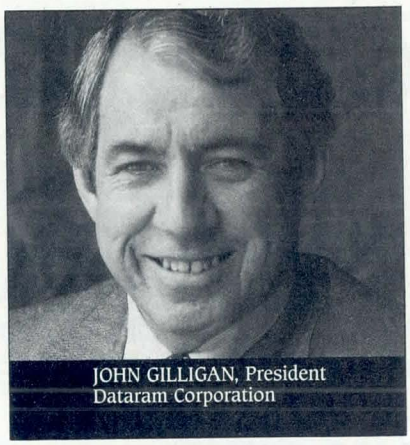

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CIRCLE 148

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CONFERENCES

OCT 31-NOV 3—Internat'l Conf on Computer Design: VLSI in Computers, Rye Town Hilton, Port Chester, NY. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

OCT-NOV—Invitational Computer Confs, King of Prussia, Pa: Vienna, Va; Houston, Tex; and Dallas, Tex; various dates. INFORMATION: B. J. Johnson & Assocs, Inc, 3151 Airway Ave, Suite C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

NOV 1-3—Federal Office Automation Conf, Washington Convention Ctr, Washington, DC. INFORMATION: National Council for Education on Information Strategies, PO Box N, Wayland, MA 01778. Tel: 617/358-5356; 800/343-6944 (outside Mass)

NOV 1-3—Symposium on Application and Assessment of Automated Tools for Software Development, San Jose, Calif. INFORMATION: Ez Nahouraii, IBM General Products Div, Programming Ed, 555 Bailey Ave, San Jose, CA 95150

NOV 5-6—San Diego Computer Fair, Scottish Rite Ctr, San Diego, Calif. INFORMATION: Barbara E. Sack, San Diego Computer Society, PO Box 81537, San Diego, CA 92138. Tel: 619/565-8720

NOV 6-10—Conf on Robot Vision and Sensory Controls, Cambridge, Mass. INFORMATION: SPIE, PO Box 10, Bellingham, WA 98225. Tel: 206/676-3290

NOV 7-9—Computer Security Conf, New York Penta Hotel, New York, NY. INFORMATION: Pat Michaud, Computer Security Institute, 43 Boston Post Rd, Northborough, MA 01532. Tel: 617/845-5050

NOV 7-11—IECON (IEEE Conf on Industrial Applications of Mini and Microcomputers), Hyatt Regency, San Francisco, Calif. INFORMATION: Patrick P. Fasang, Siemens Corp, 105 College Rd E, Princeton, NJ 08540. Tel: 609/452-7070

NOV 8-11—Mini/Micro-West, Brooks Hall, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 8-11—Magnetism and Magnetic Materials Conf, Hilton Hotel, Pittsburgh, Pa. INFORMATION: R. W. Cochrane, Dept of Physics, Univ of Montreal, Montreal, Quebec, Canada. Tel: 514/343-7423

NOV 8-11—Wescon, Moscone Ctr and Civic Auditorium, San Francisco, Calif. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 14-16—Connectors and Interconnections Technology Symposium, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

NOV 14-17—Autofact 5 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: CASA/SME Public Relations, PO Box 930, Dearborn, MI 48128. Tel: 313/271-0777

NOV 17-19—Northeast Computer Show and Software Exposition, Hynes Auditorium, Boston, Mass. INFORMATION: Northeast Expositions, Inc, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/841-7000 (outside Mass)

NOV 28-DEC 2—Comdex/Fall, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

DEC 5-6—Internat'l Electron Devices Meeting, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Assocs, 1629 K St NW, Washington, DC, 20006. Tel: 202/296-8100

DEC 7-9—Realtime Systems Symposium, Crystal City Marriott, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 12-14—Computer Networking Symposium, Sheraton Hotel, Silver Spring, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 15-17—Internat'l Conf on Information Systems, Houston, Tex. INFORMATION: Maryam Alavi, Mgmt Dept, Univ of Houston, Houston, TX 77004. Tel: 713/749-3727

JAN 17-19—Mini/Micro-Southeast, Orange County Convention and Civic Ctr, Orlando Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JAN 17-19—Southcon, Orange County Convention and Civic Ctr, Orlando, Fla. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

JAN 31-FEB 2—Communication Networks Conf & Exposition, Washington Convention Ctr, Washington, DC. INFORMATION: Judie McDaid, Hajar Assocs, 280 Hillside Ave, Needham Heights, MA 02194. Tel: 617/444-3946

FEB 21-23—Softcon, Superdome, New Orleans, La. INFORMATION: Peggy Kilburn, Northeast Expositions, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

FEB 22-24—ISSCC (IEEE Internat'l Solid-State Circuits Conf), San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 22-28—Imprinta (Internat'l Congress and Exhibition for Communications Techniques), Dusseldorf, West Germany. INFORMATION: Borman/Williams Inc, 222 Park Ave S, New York, NY 10003. Tel: 212/254-5400

WORKSHOPS

NOV-FEB—Hands-on Pascal Workshop, Boston, Mass; Washington, DC; Los Angeles, Calif; and Palo Alto, Calif; various dates. INFORMATION: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Pl, Los Angeles, CA 90045. Tel: 213/450-2060

NOV 7-8—IEEE Workshop on Languages for Automation, Chicago, Ill. INFORMATION: Shi-Kuo Chang, Dept of Electrical Engineering, Illinois Institute of Technology, Chicago, IL 60616. Tel: 312/567-3401

DEC 6-8—Software Maintenance Workshop, Naval Postgraduate School, Monterey, Calif. INFORMATION: Janice Thill, Code 54Ss Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-3212

DEC 11-13—Computer Aided Graphic Arts and Visual Communications, Essex House, New York, NY. INFORMATION: Barbara Jeffe, Pratt Ctr, 505 White Plains Rd, Tarrytown, NY 10591. Tel: 914/631-8772

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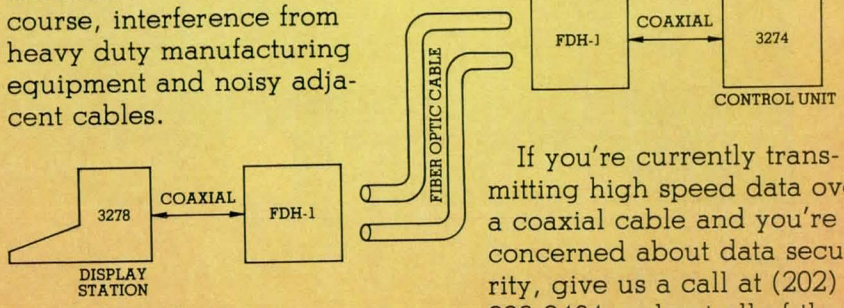

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CIRCLE 151

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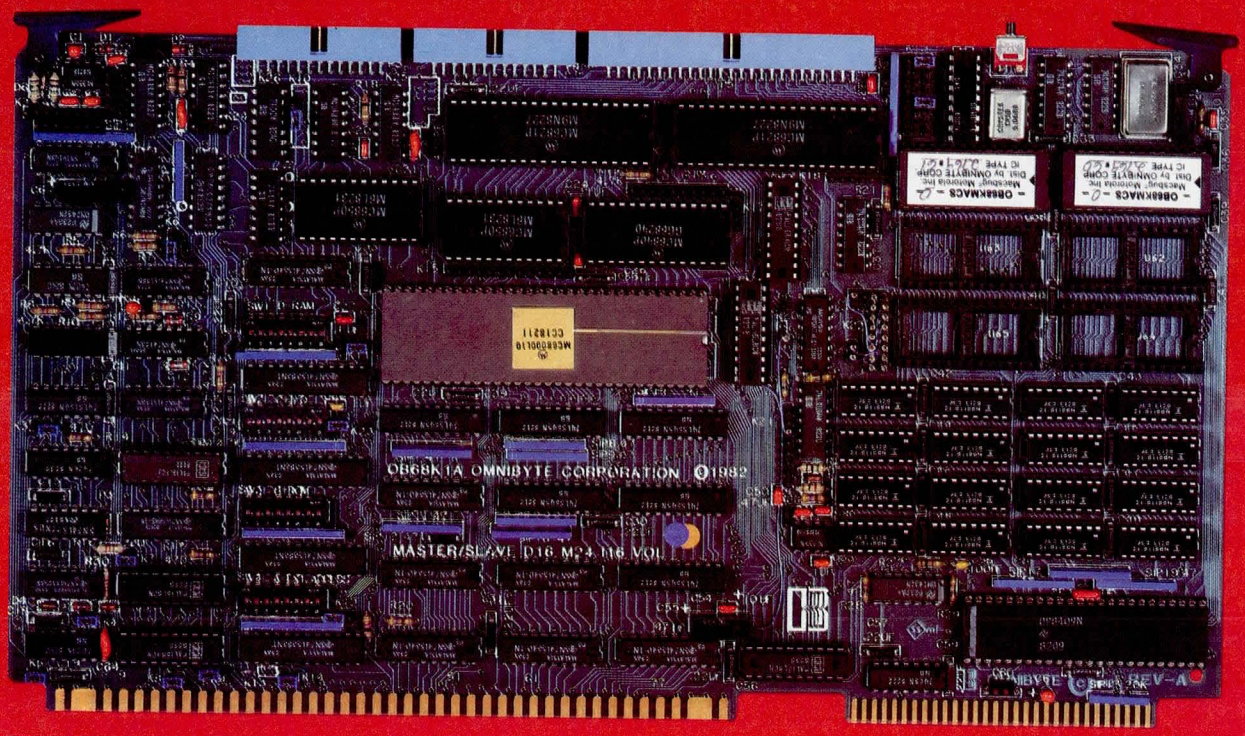
OB68K1A



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SOFTWARE SUPPORT

A variety of software packages are available for the OB68K1A. They range from the optional MACSBUG monitor/ debugger to Realtime Executives and Target Operating Systems in silicon. Four commercial software manufacturers have complete operating systems, including development tools and high level languages.

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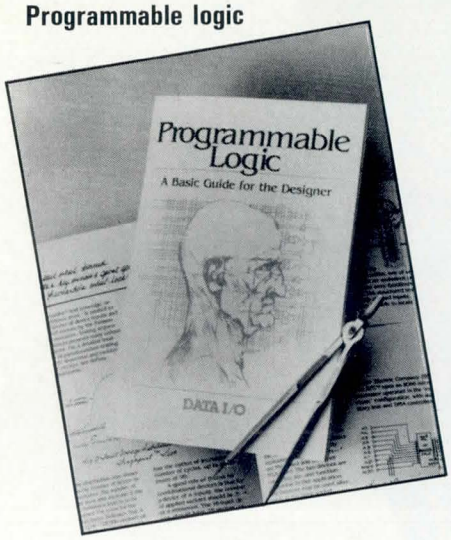
Programmable logic



Guide explains advantages of programmable logic over fixed-function LSI/MSI and custom logic; it details a design problem, showing how equations are generated and translated into fuse tables, and how a PLA or IFL device is programmed and functionally tested. **Data I/O**, Redmond, Wash. **Circle 410**

Microcomputer development data

Manual supplies information on PIC architecture, instruction set, commonly used software routines, key application information, and development production cycles. **General Instrument Corp, Microelectronics Div**, Hicksville, NY.
Circle 411

Displays, switches, and keyboards

Foldout outlines design and production capabilities of digital displays, touch switches, and keyboards. **Refac Electronics Corp**, Winsted, Conn.
Circle 412

Minimizing DAC output glitch

Application note describes and illustrates principal sources of unwanted transient energy and its effect on CRT displays, then examines how reconstructing signal circuitry with a DAC and a deglitcher can improve display image. **ILC Data Device Corp**, Bohemia, NY.
Circle 413

Fiber optic journal

Special issue of *Innovators* reprints 6 articles on the basics and applications of fiber optic cables, connectors, and testing, as well as eye pattern testing in fiber optic systems. Write to Manager, Marketing Communications, **Belden**, 2000 S Batavia Ave, Geneva, IL 60134.

Electronic spreadsheet

Leaflet provides specs and photos of the MegaCalc and its advanced worksheet and screen-splitting capabilities; standardized language capability is also described. **The Mega Group, Inc**, Irvine, Calif. **Circle 414**

Environmental test rooms

Folder presents features and optional accessories for tailor-made temperature/humidity-controlled walk-in rooms. **Tenney Engineering, Inc**, Union, NJ.
Circle 415

Quarter-inch drive

Foldout specifies and describes features of the Qic-Stor Mark II QIC-2/24-compatible streaming tape drive, and includes a cutaway illustration of the drive's interior mechanisms. **Tandberg Data, Inc, Data Storage Div**, Orange, Calif.
Circle 416

Integrated circuit interface

Guide for interfacing ICs to peripheral power and display driver applications contains a list of current-sink and current-source drivers for use with various displays, inductive loads, and thermal/electrosensitive printers. **Sprague Electric Co**, North Adams, Mass.
Circle 417

Local area network

Data sheet overviews the Cinchnet LAN, which interfaces directly to an IBM PC via an RS-232-C link; application note describes no-polling access technique for 124 primary automation controllers over 4000′ at 28.8k baud. **Inconix Corp**, Natick, Mass.
Circle 418

Lighted pushbuttons

Series KB and LB panel-mounted switches are featured in data sheet, including mechanical drawings, specs, materials, LED and incandescent lamp choices, filters, diffusers, and standard mounting hardware. **NKK Switches of America Inc**, Scottsdale, Ariz.
Circle 419

Small impact printer

Brochure profiles 16-column, panel-mounted NAP-16-I printers, giving specs, dimensions, and ordering information for BCD, RS-232-C, 20-mA current loop, and 8-bit parallel ASCII interface. **Keltron Corp**, Waltham, Mass.
Circle 420

Line monitor power conditioners

Guide features electrical spike and noise suppressor units. **SGL Waber Electric**, Westville, NJ. **Circle 421**

Computer peripherals

Catalog covers specs and features for dot matrix printers, cartridge tape drives and storage systems, and tape communication terminals; specific sections are devoted to high density tape drives and data loaders/loggers with RS-232 and ARINC compatibility. **North Atlantic Industries, Qantex Div**, Hauppauge, NY.
Circle 422

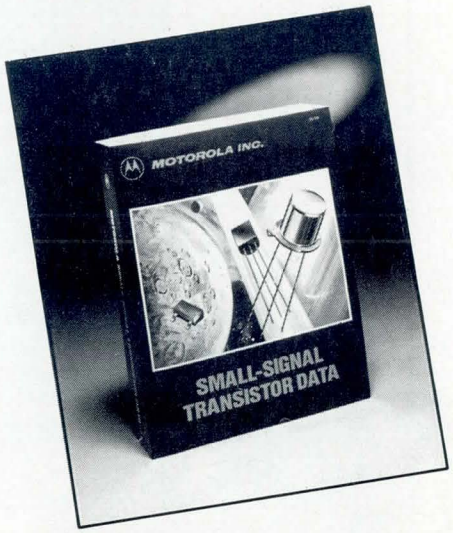
Software packages for VAX

Digest on the Abaqus approach to advanced engineering analysis gives applications and discusses architecture; software referral catalog abstracts over 700 additional VAX engineering applications. **Digital Equipment Corp**, Marlboro, Mass.
Circle 423

Analog-digital interface

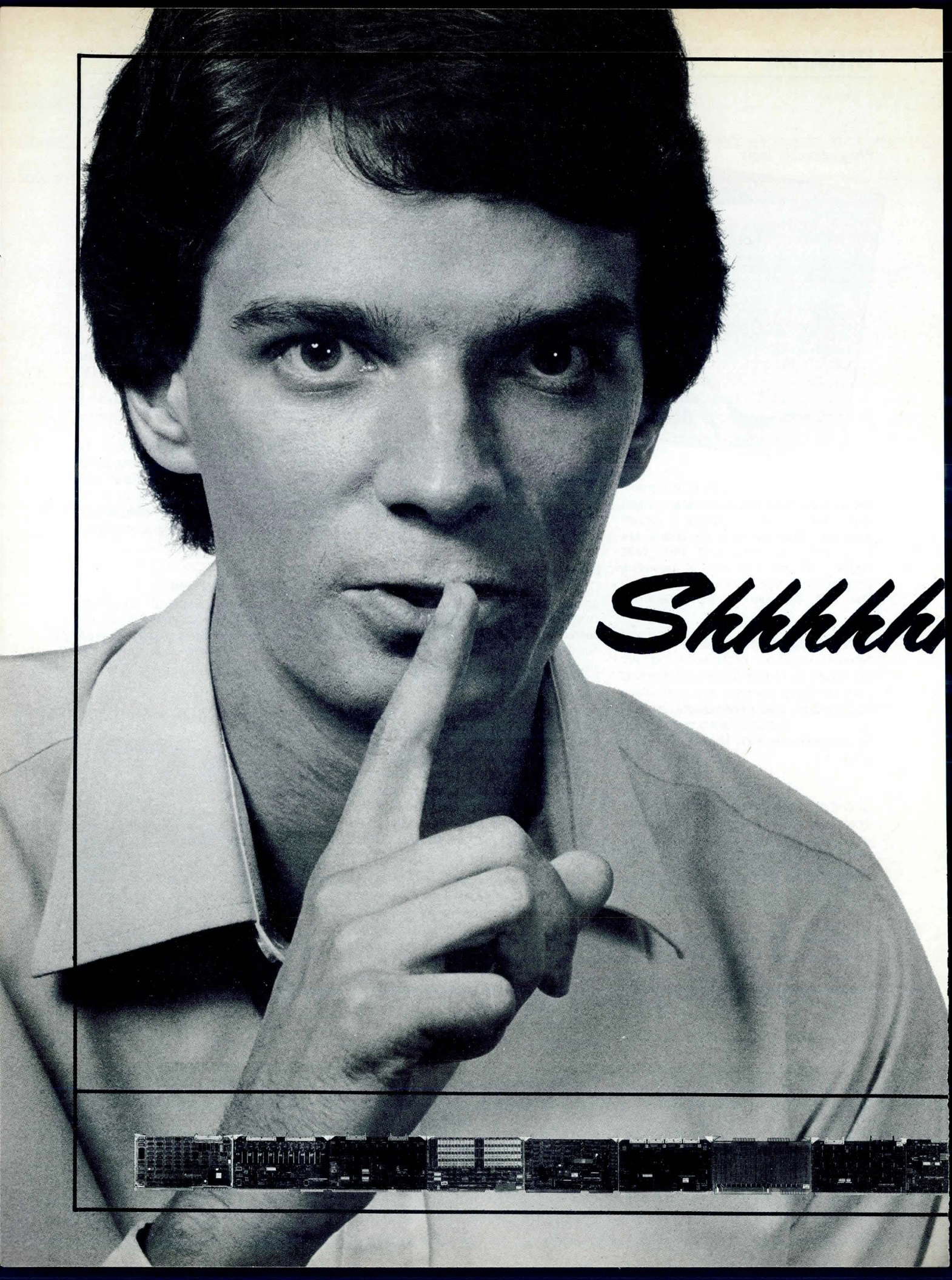
Application note explains interrupt-driven data transfer scheme for an 8080/8255-based microprocessor data acquisition system. **Teledyne Semiconductor**, Mountain View, Calif.
Circle 424

Small-signal transistors



Small-signal transistors

Data book presents technical information for bipolar and field-effect transistors, with package outline drawings; plastic-encapsulated, microminiature, metal, multiple, and rf versions are covered. **Motorola Semiconductor Products, Inc**, Phoenix, Ariz.
Circle 425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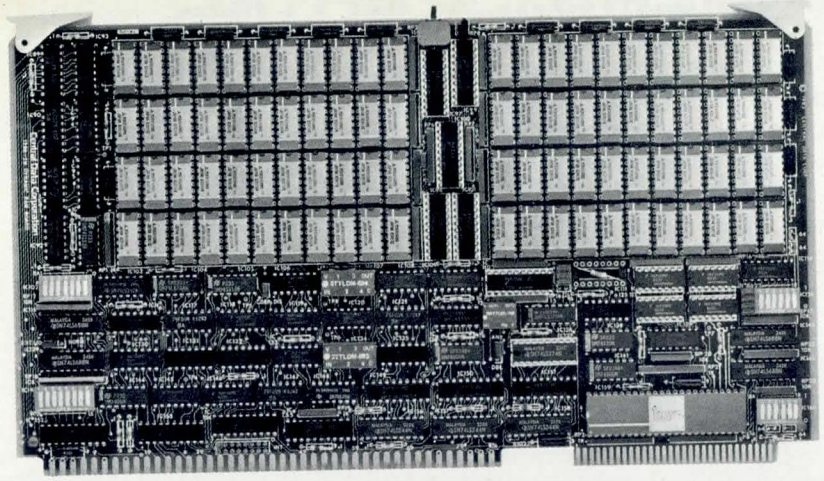

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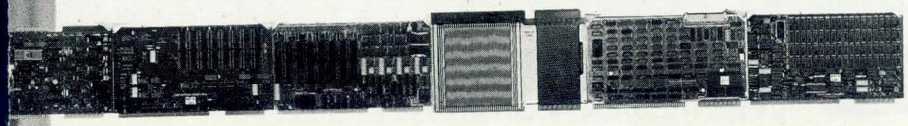

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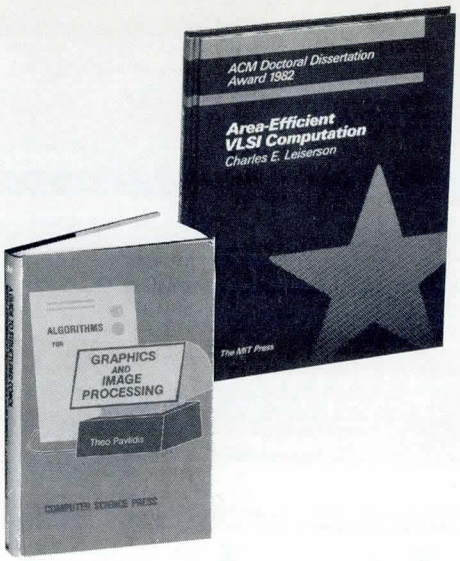

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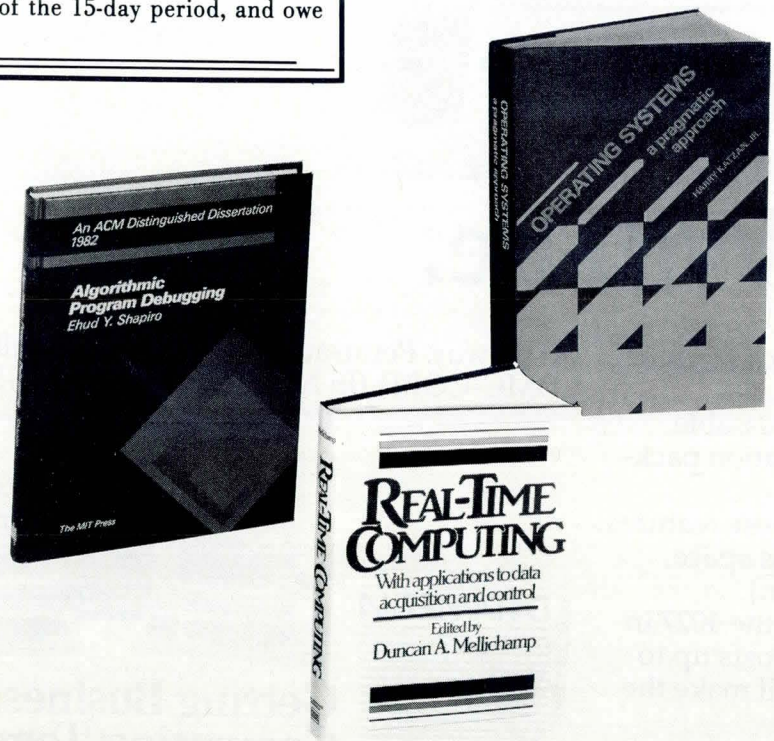

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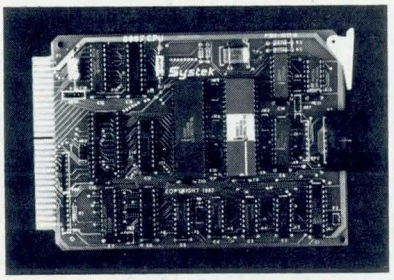

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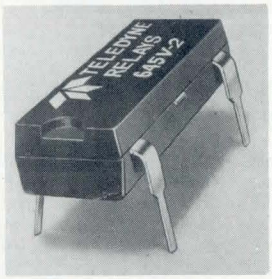

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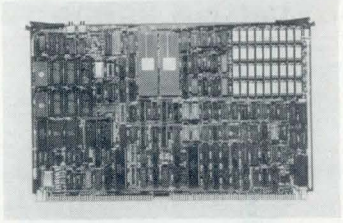

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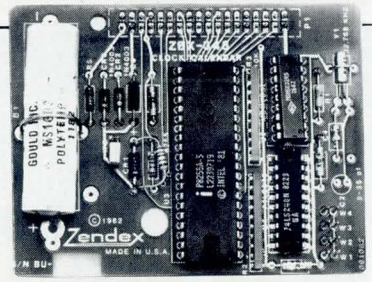

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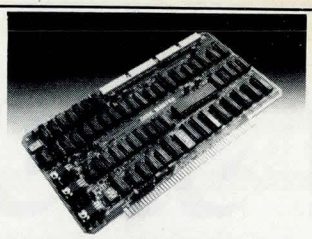

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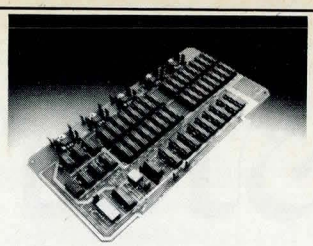

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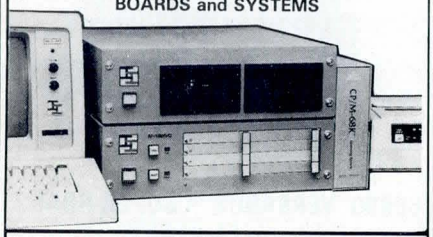

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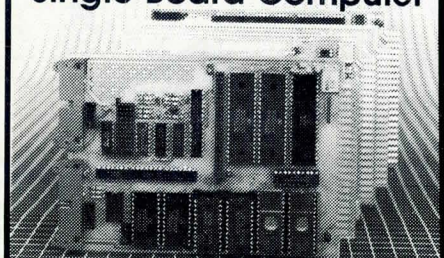

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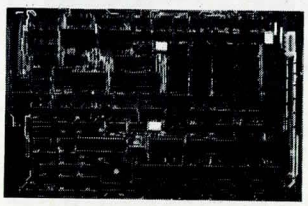

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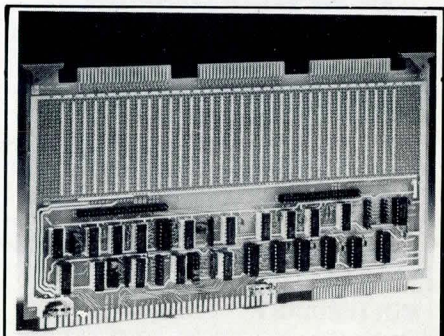

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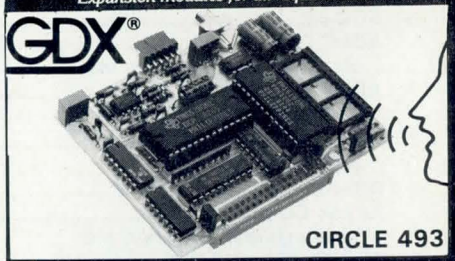

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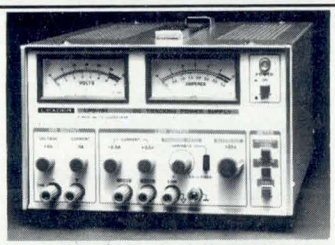

TRIPLE OUTPUT DC POWER SUPPLIES

The Leader LPS-151 and LPS-152 are two new triple output, dc power supplies featuring individual voltage and current meters, independent adjustable current limiting, automatic overload recovery and auto tracking. Adjustable output voltages: 0 to 6 V, 0 to + 25 V and 0 to − 25 V dc. LPS-151 list price $395; LPS-152 $495. Available from stock.

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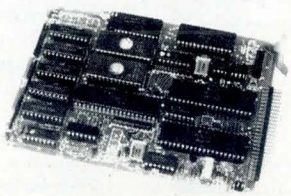

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uses 6809 (E)MPU. Provides cost effective multicard capability—2K CMOS RAM may be battery backed (power fail/interrupt on board), sockets for 28 pin EPROM/EEPROM, RS232/423 serial I/O, 32 lines parallel I/O, 4 timers. Other **10000 SERIES MICROCOMPUTER MODULES** include 10812 6502 SCC/C, 10764 Universal Non-volatile Memory, 10701 Non-volatile RAM. Custom design/mfg. to your requirments. Call today. **ENTERPRISE SYSTEMS CORP,** Box 698 Dover, NH 03820. Tel: (603) 742-7363.

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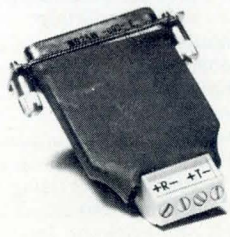

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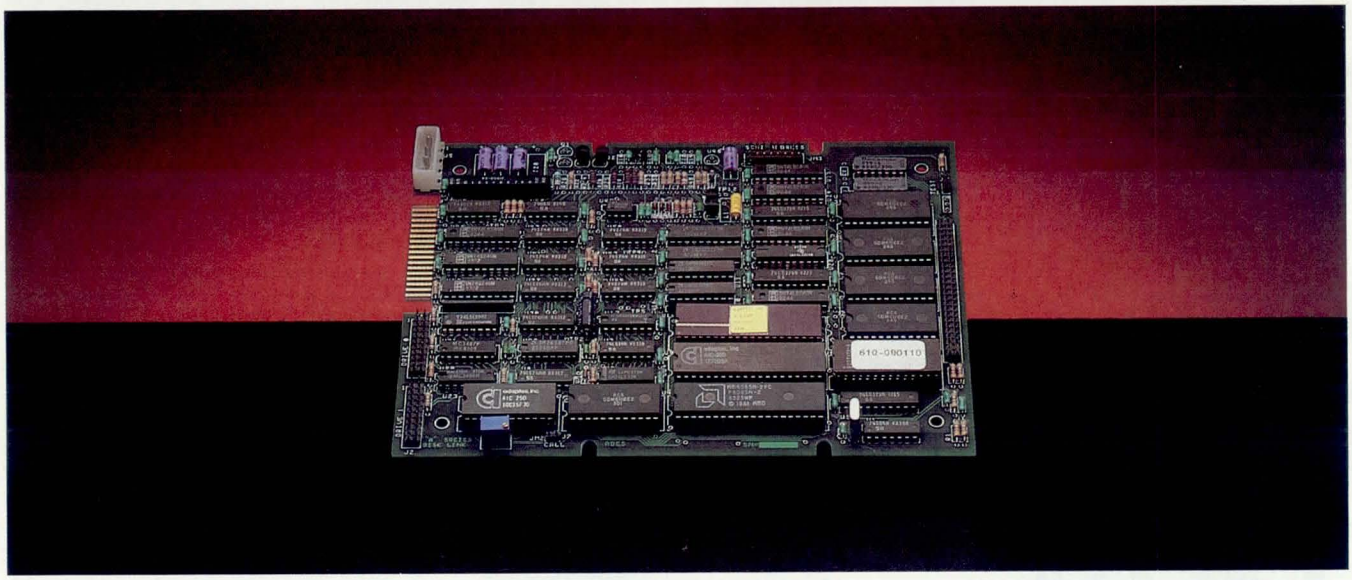
Now Adaptive Data Offers XEBEC 1410 Users a Better Choice:

A Plug Compatible Disk Controller With Significantly Greater User Benefits



Our Winchester disk controllers offer a better interleaving capability, resulting in better systems throughput than XEBEC's controllers.

That's because our controllers have one-to-one interleaving. In other words, the ability to read every sector on the disk in just one pass. Just one quick revolution of the media.

So that means that your system will have the option to access the data from the disk at a faster rate. Because our controllers will read the data into an on-board buffer in just one revolution. And then give it to you at a speed you specify.

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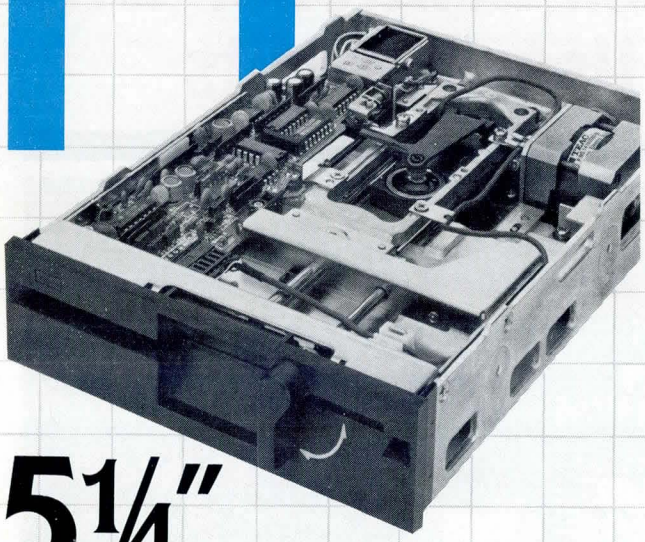
HALF HIGH



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• 40 track	• 40 track	• 80 track	• 80 track
• 250KB	• 500KB	• 500KB	• 1MB
• single side	• double side	• single side	• double side

Power Requirements:
DC +12V ±5% 0.3A typical, 0.7A max.
DC + 5V ±5% 0.5A typical, 0.7A max.

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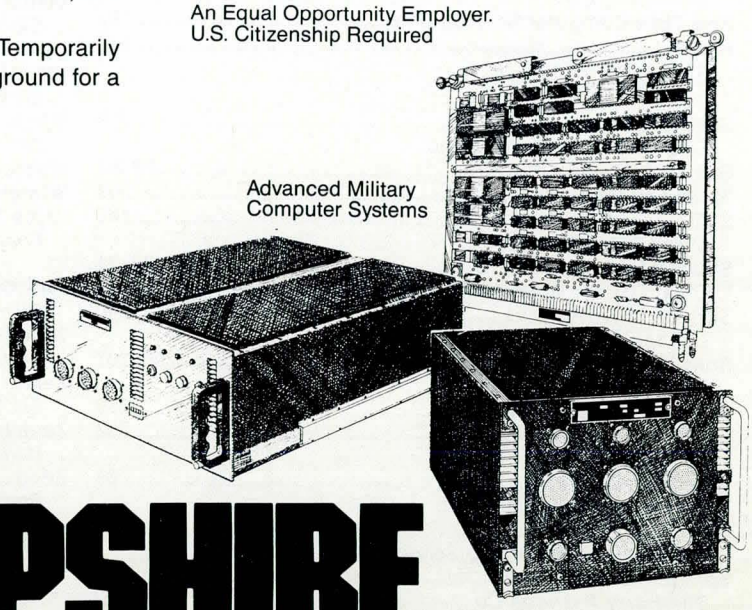

Advanced Military Computer Systems

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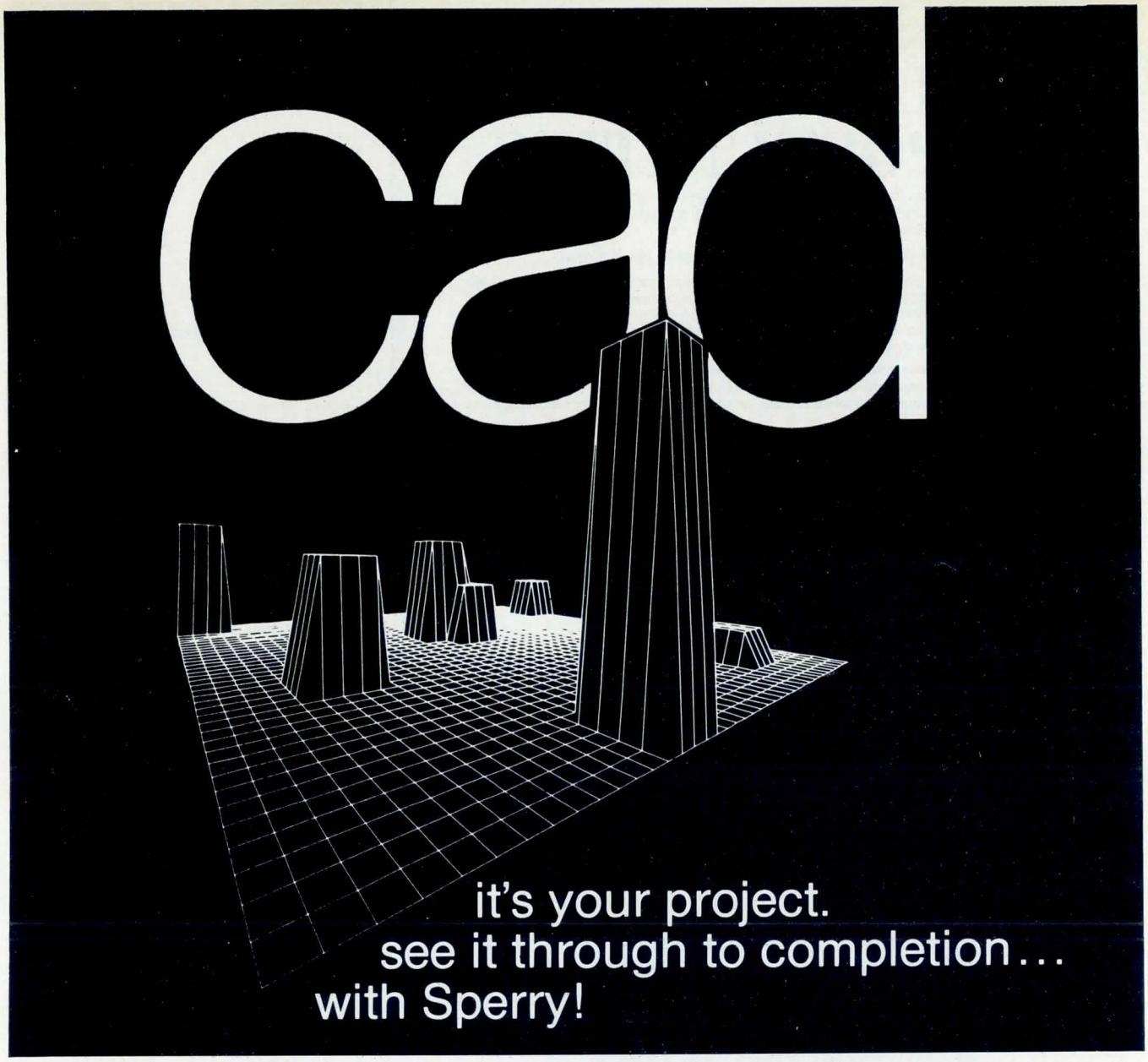

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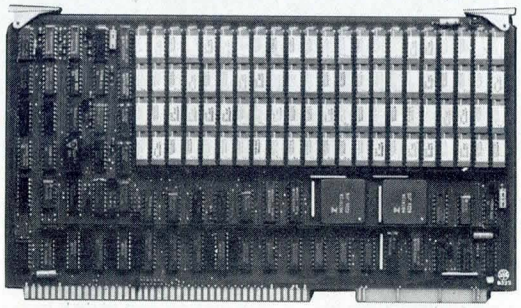
CI-796 EDC



- Up to 2MB in one option slot
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- Error Detection and Correction
- Addressable in 16K byte blocks
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CIRCLE 163

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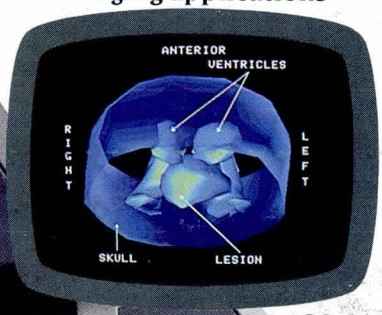
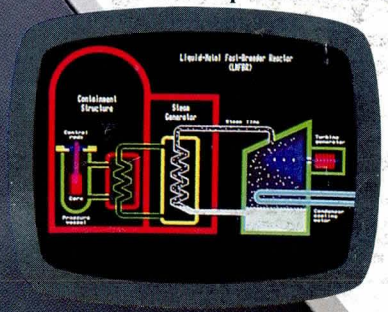


C&C and process control



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