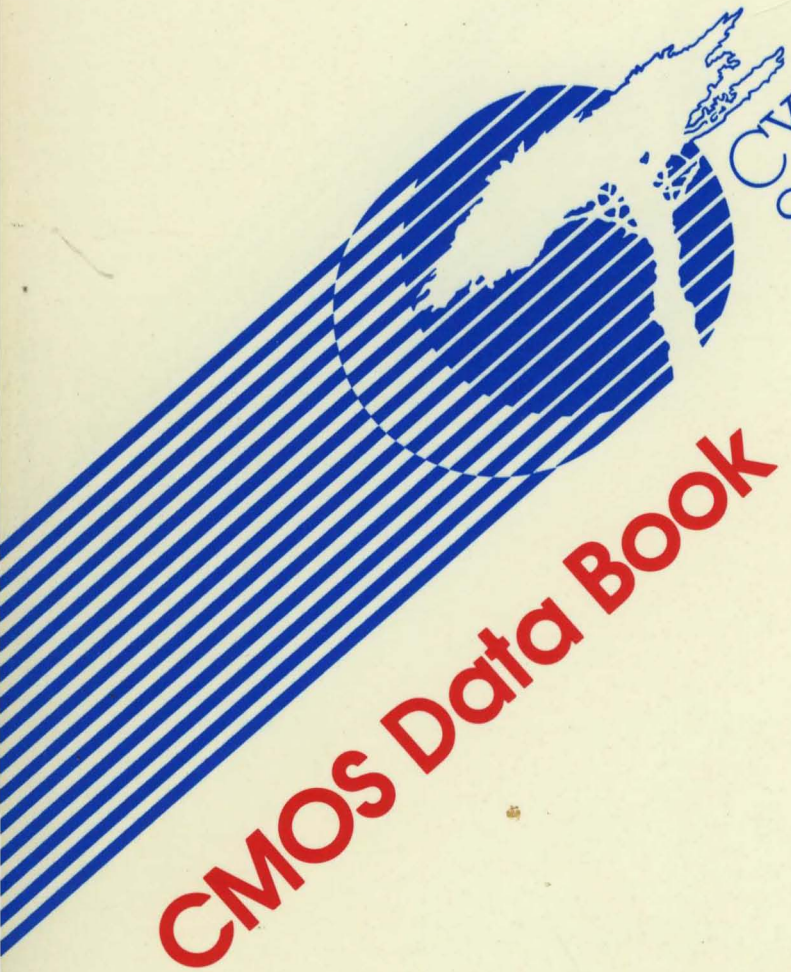
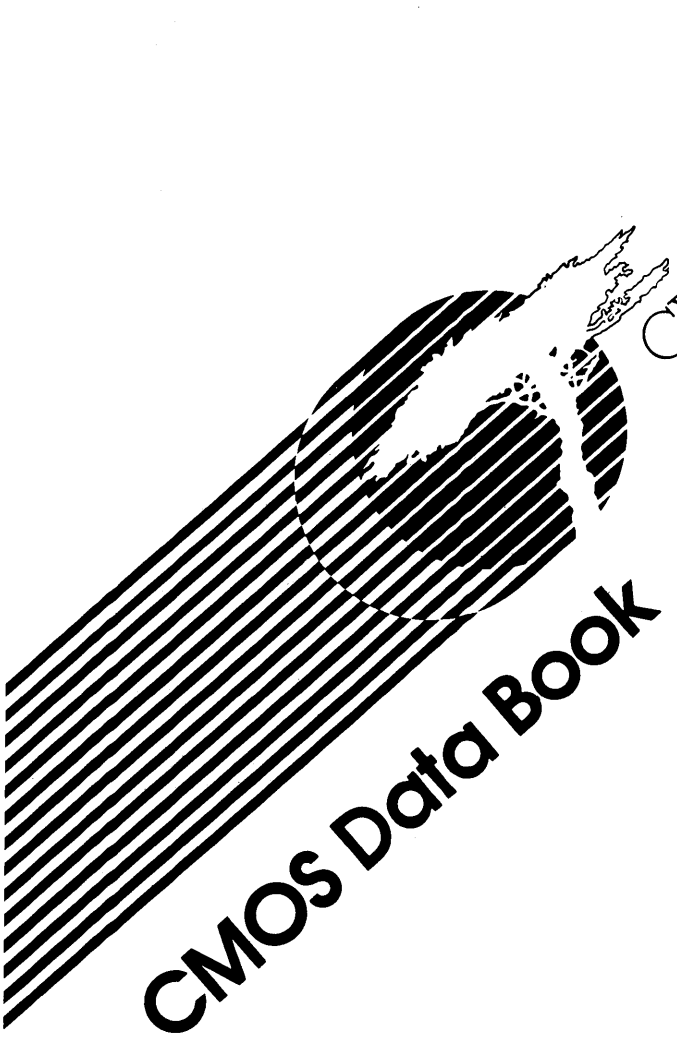


CYPRESS SEMICONDUCTOR

CMOS Data Book



CYPRESS SEMICONDUCTOR™

CMOS Data Book

Cypress Semiconductor 3901 North First St. San Jose, CA 95134 (408) 943-2600, Telex: 821032, TWX: 910 997 0753

How To Use This Book

This book has been organized by product type, beginning with Product Information. The products then follow, beginning with RAMs, then PROMS, PALs, and finally LOGIC. FIFO products are included in the LOGIC section. The Appendix A covers Packages, and Thermal Data. Appendix B covers Cypress Quality and Reliability aspects, and Appendix C is a compilation of various Application Briefs.

A Numeric Device Index is included after the Table of Contents that identifies products by numeric order, rather than by device type which is how the manual is set up. To further help you in identifying parts, a Product Line Cross Reference is in Product Information. Use it to find the Cypress part number that is comparable to another manufacturer's part number.

CYPRESS SEMICONDUCTOR

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PROMs (Programmable Read Only Memory)

PALs (Programmable Array Logic)

LOGIC

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General Product Information

Page Number

Cypress Semiconductor Background

Cypress Semiconductor was founded in April of 1983 and has quickly emerged as a leader of high performance CMOS products. The Cypress CMOS product line is targeted to replace slower bipolar and NMOS products with reliability, high speed and low power.

Cypress products fall into three families: High Speed Static RAMs, Programmable Products, and Logic. Initial members of the Static RAM family include devices in densities of 64 bits to 16K bits and performance from 15 to 35 ns. The various organizations from 16 x 4, 256 x 4 through 16K x 1, 2K x 8, and 4K x 4 provide field applications in large mainframes, high speed controllers, communications, and graphics display.

Cypress Programmable Products consist of high speed CMOS PROMs and Programmable Array Logic (PAL), both employing an EPROM programming element. Like the High Speed Static RAM family, these products are the natural choice to replace older devices manufactured in bipolar technology because they provide superior performance at one half of the power consumption.

Logic products beginning with the 7C901 Four Bit Slice, include a family of FIFO's (First In First Out buffers). FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed while the results may be processed or distributed at a speed commensurate with need.

Cypress's semiconductors are 100% "Made in USA". Situated in California's Silicon Valley, Cypress houses R&D, design, wafer fabrication, assembly, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. In many other semiconductor facilities, wafers are fabricated in Class 100 environments, often under laminar flow hoods only. At Cypress the entire wafer fabrication area is a Class 10 environment. This means that the ambient air has less than 10 particulates of greater than 0.2 micron in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ± 0.2 degree Fahrenheit tolerance; filtered air is completely exchanged 10 times each minute throughout the fab; critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is just as critical. Assembly is done in a Class 100 clean room until the silicon die is sealed in a package. Lead frames are handled in carriers or cassettes through the entire operation. Automated robots remove and replace parts into cassettes. Using sophisticated automated equipment, parts are assembled and tested in less than five days. The Cypress assembly line is the most flexible, automated line in the United States.

The Cypress motto has always been "only the best". The best facilities, the best equipment, the best employees ... all striving to make the best CMOS product. Cypress has grown very quickly to become "the best".

Cypress CMOS Technology

In the last decade, there has been a tremendous need for high performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor has overcome the classically held perceptions that CMOS is a moderate performance technology. That places its product lines ahead of its bipolar competitors in all three areas.

The Cypress process is a 1.2 micron "N" well technology with double layer poly, single layer metal and an EPROM capability. The process employs lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latchup characteristics associated with the older CMOS technologies.

To further enhance the technology from the reliability direction, improvements have been incorporated in the process and design minimizing electrostatic discharge and input signal clipping problems.

Finally, although not a requirement in the high performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages, without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latchup have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high performance MOS and bipolar products. Although in its earliest years MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2 micron CMOS process technology. All Cypress products are designed to withstand voltage and energy levels in excess of 2000 volts and 0.4 milli-joules, more than twice the energy level specified by MIL STD 883C.

Latchup, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures, and care in the physical layout of the products.

The Cypress CMOS technology has been carefully designed, creating products that are "only the best" in high speed, excellent reliability, and low power.

Product Line Cross Reference

CYPRESS	CYPRESS
2147-35C	7C147-35C
2147-45C	2147-35C
2147-45C	7C147-45C
2147-45M	7C147-45M
2147-55C	2147-45C
2147-55M	2147-45M
2148-35C	7C148-35C
2148-35C	21L48-35C
2148-35M	7C148-35M
2148-45C	2148-35C
2148-45C	21L148-45C
2148-45M	7C148-45M
2148-45M	2148-35M
2148-55C	21L48-55C
2148-55C	2148-45C
2148-55M	2148-45M
2149-35C	7C149-35C
2149-35C	21L49-35C
2149-35M	7C149-35M
2149-45C	21L49-45C
2149-45M	7C149-45M
2149-45M	2149-35M
2149-55C	21L49-55C
2149-55C	2149-45C
2149-55M	2149-45M
21L48-35C	7C148-35C
21L48-45C	21L48-35C
21L48-45C	7C148-45C
21L48-55C	21L48-45C
21L49-35C	7C149-25C
21L49-45C	7C149-45C
21L49-45C	21L49-35C
21L49-55C	21L49-45C
27S03AC	7C189-18C
27S03AC	7C189-25C
27S03AM	7C189-25M
27S03C	27S03AC
27S03C	74S189C
27S03M	27S03AM
27S03M	54S189M
27S07AC	7C190-18C
27S07AM	7C190-25M
27S07C	27S07AC
27S07C	7C190-25C
27S07AC	7C190-25C
27S07M	27S07AM
27S07M	7C190-25M
2901BC	7C901-31C
2901BM	7C901-32C
2901CC	79901-69C
2901CC	2901BC
2901CM	7C901-88M

CYPRESS	CYPRESS
2901CM	2901BM
3341C	7C401-10C
54S189M	27S03M
74S189C	27S03C
7C122-35C	7C122-25C
7C122-35M	7C122-25M
7C128-45C	7C128-35C
7C128-55C	7C128-45C+
7C128-55M	7C128-45M
7C129-45C	7C129-35C
7C129-55C	7C129-45C+
7C129-55M	7C129-45M+
7C147-35C	7C147-25C
7C147-45C	7C147-35C
7C147-45M	7C147-35M
7C148-45C	7C148-35C
7C148-45M	7C148-35M
7C149-45C	7C149-35C
7C149-45M	7C149-35M
7C150-35C	7C150-25C
7C167-45C	7C167-35C
7C167-45M	7C167-35M
7C168-35C	7C168-25C
7C168-45C	7C168-35C
7C168-45M	7C168-35M
7C169-35C	7C169-25C
7C169-40C	7C169-35C
7C169-40M	7C169-35M
7C170-35C	7C170-25C
7C170-40C	7C170-35C
7C170-40M	7C170-35M
7C187-35C	7C187-25C
7C187-45C	7C187-35C
7C187-45M	7C187-35M
7C225-40C	7C225-30C
7C225-40M	7C225-35M
7C235-40C	7C235-30C
7C245-45C	7C245-35C
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7C282-45C	7C282-30C
7C291-50C	7C291-35C
7C292-50C	7C292-35C
7C401-10C	7C401-15C
7C401-10M	7C401-15M
7C402-10C	7C402-15C
7C402-10M	7C402-15M
7C403-10C	7C403-15C
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7C403-15C	7C403-25C
7C404-10C	7C404-15C
7C404-10M	7C404-15M
7C404-15C	7C404-25C

CYPRESS	CYPRESS
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7C901-88M	7C901-32M
9122-25C	7C122-15C
9122-25C	91L22-25C
9122-35C	9122-25C
9122-35C	91L22-35C
9122-45C	93L422-C
91L22-25C	7C122-25C
91L22-35C	7C122-35C
91L22-45C	93L422AC
93422AC	9122-35C
93422AC	7C122-35C
93422AM	7C122-35M
93422C	93L422AC
93422M	93422AM
93422M	93L422AM
93L422AC	7C122-35C
93L422AC	91L22-45C
93L422AM	7C122-35M
93L422C	93L422AC
93L422M	93L422AM
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PAL16L8A-2M	PALC16L8AM
PAL16L8AC	PALC16L8AC
PAL16L8AM	PALC16L8AM
PAL16R4A-2C	PALC16R4AC
PAL16R4A-2M	PALC16R4AM
PAL16R4AC	PALC16R4AC
PAL16R4AM	PALC16R4AM
PAL16R6A-2C	PALC16R6AC
PAL16R6A-2M	PALC16R6AM
PAL16R6AC	PALC16R6AC
PAL16R6AM	PALC16R6AM
PAL16R8A-2C	PALC16R8AC
PAL16R8A-2M	PALC16R8AM
PAL16R8AC	PALC16R8AC
PAL16R8AM	PALC16R8AM
PALC22V10C	PALC22V10AC
PALC22V10M	PALC22V10AM
PALC32V10C	PALC32V10AC
PALC32V10M	PALC32V10AM

AMD	CYPRESS
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SUFFIX: D	SUFFIX: D
SUFFIX: F	SUFFIX: F
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
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2147-45C	2147-45C

AMD	CYPRESS
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2147-55M	2147-55M
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2147-70M	2147-55M
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2149-45C	2149-45C
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2149-55C	2149-55C
2149-55M	2149-55M
2149-70C	2147-55C
2149-70M	2147-55M
2167-35C	7C167-35C
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2167-45C	7C167-45C
2167-45M	7C167-45M
2167-55C	7C167-45C
2167-55M	7C167-45M
2167-70C	7C167-45C
2167-70M	7C167-45M
2168-45C	7C168-45C
2168-55C	7C168-45C
2168-55M	7C168-45M
2168-70C	7C168-45C
2168-70M	7C168-45M
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2169-40M	7C169-40M
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2169-50M	7C169-40M
2169-70C	7C169-40C
2169-70M	7C169-40M
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21L48-55C	21L48-55C
21L48-70C	21L48-55C
21L49-45C	21L49-45C
21L49-55C	21L49-55C
21L49-70C	21L49-55C
22V10AC	PALC22V10AC
22V10AM	PALC22V10AM
22V10C	PALC22V10C
22V10M	PALC22V10M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent

Product Line Cross Reference (Continued)

AMD	CYPRESS
27PS181AC	7C282-45C
27PS181AM	7C282-45M+
27PS181C	7C282-45C
27PS181M	7C282-45M+
27PS191AC	7C292-50C
27PS191AM	7C292-50M+
27PS191C	7C292-50C
27PS191M	7C292-50M+
27PS281AC	7C281-45C
27PS281AM	7C281-45M+
27PS281C	7C281-45C
27PS281M	7C281-45M+
27PS291AC	7C291-50C
27PS291AM	7C291-50M+
27PS291C	7C291-50C
27PS291M	7C291-50M+
27S03AC	27S03AC
27S03AM	27S03AM
27S03C	27S03C
27S03M	27S03M
27SO7AC	27SO7AC
27S07AM	27S07AM
27S07C	27S07C
27S07M	27S07M
27S181AC	7C282-30C
27S181AM	7C282-45M
27S181C	7C282-45C
27S181C	7C282-45C
27S181M	7C282-45M
27S191AC	7C292-35C
27S191AM	7C292-50M
27S191C	7C292-50C
27S191M	7C292-50M
27S25AC	7C225-30C
27S25AM	7C225-35M
27S25C	7C225-40C
27S25M	7C225-40M
27S281AC	7C281-30C
27S281AM	7C281-45M
27S281C	7C281-45C
27S281M	7C281-45M
27S291AC	7C291-35C
27S291AM	7C291-50M
27S291C	7C291-50C
27S291M	7C291-50M
27S35AC	7C235-30C
27S35AM	7C235-40M
27S35C	7C235-40C
27S35M	7C235-40M
27S45AC	7C245-35C
27S45AM	7C245-45M
27S45C	7C245-45C

AMD	CYPRESS
27S45M	7C245-45M
2841AC	3341C+
2841C	3341C+
3341C	3341C+
54S189M	54S189M
74S189C	74S189C
9122-25C	9122-25C
9122-25M	7C122-25M
9122-35C	9122-35C
9122-35M	7C122-35M
9150-25C	7C150-25C
9150-35C	7C150-35C
9150-35M	7C150-35M
9150-45C	7C150-35C
9150-45M	7C150-35M
91L22-35C	91L22-35C
91L22-35M	7C122-35M
91L22-45C	91L22-45C
91L22-45M	7C122-35M
91L22-60C	7C122-35C+
93422AC	93422AC
93422AM	93422M
93422C	93422C
93422M	93422M
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93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
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99[L]68-70M	7C168-45M*
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PAL16L8M	PAL16L8A-2M
PAL16L8AC	PAL16L8AC
PAL16L8AM	PAL16L8AM
PAL16L8LC	PAL16L8A-2C
PAL16L8LM	PAL16L8A-2M
PAL16R4LC	PAL16R4A-2C
PAL16R4LM	PAL16R4A-2M
PAL16R4AC	PAL16R4AC
PAL16R4AM	PAL16R4AM
PAL16R4C	PAL16R4A-2C
PAL16R4M	PAL16R4A-2M
PAL16R6AC	PAL16R6AC
PAL16R6AM	PAL16R6AM
PAL16R6C	PAL16R6A-2C
PAL16R6M	PAL16R6A-2M
PAL16R6LC	PAL16R6A-2C
PAL16R6LM	PAL16R6A-2M
PAL16R8LC	PAL16R8A-2C

AMD	CYPRESS
PAL16R8LM	PAL16R8A-2M
PAL16R8AC	PAL16R8AC
PAL16R8AM	PAL16R8AM
PAL16R8C	PAL16R8A-2C
PAL16R8M	PAL16R8A-2M

FAIRCHILD	CYPRESS
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SUFFIX: F	SUFFIX: F
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
SUFFIX: QB	SUFFIX: B
3341AC	3341C+
3341C	3341C+
54F189	7C189-25M−
54F219	7C190-25M−
54F413	7C401-15M
54S189M	54S189M
74F189	7C189-25C−
74F219	7C190-25C−
74F413	7C401-15C
74S189	74S189C
93422AC	93422AC
93422AM	93422M
93422C	93422C
93422M	93422M
93475C	2149-45C
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
93Z451AC	7C282-30C
93Z451AM	7C282-45M
93Z451C	7C282-45C
93Z451M	7C282-45M
93Z511C	7C292-35C
93Z511M	7C292-50M

FUJITSU	CYPRESS
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PREFIX: MBM	PREFIX: CY
SUFFIX: F	SUFFIX: F
SUFFIX: M	SUFFIX: P
SUFFIX: Z	SUFFIX: D
2147H-35	2147-35C
2147H-45	2147-45C
2147H-55	2147-55C
2147H-70	2147-55C
2148-55L	21L48-55C
2148-70L	21L48-55C
2149-45	2149-45C
2149-55L	21L49-55C
2149-70L	21L49-55C
7132E	7C282-45C
7132E-SK	7C281-45C
7132E-W	7C282-45M
7132H	7C282-45C
7132H-SK	7C281-45C
7132Y	7C282-30C
7132Y-SK	7C281-30C
7138E	7C292-50C
7138E-SK	7C291-50C
7138E-W	7C292-50M
7138H	7C292-35C
7138H-SK	7C291-35C
7138Y	7C292-35C
7138Y-SK	7C291-35C
8167A-45	7C167-45C
8167A-55	7C167-45C
8167A-70	7C167-45C
8168-55	7C168-45C
8168-70	7C168-45C

HARRIS	CYPRESS
PREFIX: 1	SUFFIX: D
PREFIX: 3	SUFFIX: P
PREFIX: 4	SUFFIX: L
PREFIX: 9	SUFFIX: F
PREFIX: HM	PREFIX: CY
PREFIX: HPL	PREFIX: CY
SUFFIX: −8	SUFFIX: B
6-76161-2	7C291-50M
6-76161-5	7C291-50C
6-76161A-5	7C291-50C
6-76161B-5	7C291-35C
6-7681-5	7C281-45C
6-7681A-5	7C281-45C
76161-2	7C292-50M
76161-5	7C292-50C
76161A-5	7C292-50C
76161B-5	7C292-35C
7681-2	7C282-45M
7681-5	7C282-45C
7681A-5	7C282-45C
77209-2	PAL16L8A-2M
77209-5	PAL16L8A-2C
77210-2	PAL16R4A-2M
77210-5	PAL16R4A-2C
77211-2	PAL16R6A-2M
77211-5	PAL16R6A-2C
77212-2	PAL16R8A-2M
77212-5	PAL16R8A-2C

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* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
− = functionally equivalent

Product Line Cross Reference (Continued)

HITACHI	CYPRESS
PREFIX: HM	PREFIX: CY
PREFIX: HN	PREFIX: CY
SUFFIX: CG	SUFFIX: L
SUFFIX: G	SUFFIX: D
SUFFIX: P	SUFFIX: P
25089	7C282-45C
25089S	7C282-45C
25169S	7C292-50C
4847	2147-55C
4847-2	2147-45C
4847-3	2147-55C
6116ALS-12	7C128-45C*
6116ALS-15	7C128-45C*
6116ALS-20	7C128-45C*
6116AS-12	7C128-45C+
6116AS-15	7C128-45C+
6116AS-20	7C128-45C+
6147	7C147-45C*
6147-3	7C147-45C*
6147H-35	7C147-35C
6147H-45	7C147-45C
6147H-55	7C147-45C
6148	7C148-45C
6148-6	7C148-45C
6148H-35	21L48-35C
6148H-45	7C148-45C
6148H-55	7C148-45C
6148HL-35	21L48-35C*
6148HL-45	7C148-45C*
6148HL-55	7C148-45C*
6148L	7C148-45C*
6148L-6	7C148-45C*
6167	7C167-45C
6167-6	7C167-45C
6167-8	7C167-45C
6167H-45	7C167-45C
6167H-55	7C167-45C
6167HL-45	7C167-45C*
6167HL-55	7C167-45C*
6167L	7C167-45C*
6167L-6	7C167-45C*
6167L-8	7C167-45C*
6168H-45	7C168-45C
6168H-55	7C168-45C
6168H-70	7C168-45C
6168HL-45	7C168-45C*
6168HL-55	7C168-45C*
6168HL-70	7C168-45C*
6267-35	7C167-35C
6267-45	7C167-45C
6287-55	7C187-45C
6287-70	7C187-45C

HITACHI	CYPRESS
6287L-55	7C187-45C*
6287L-70	7C187-45C*

IDT	CYPRESS
PREFIX: IDT	PREFIX: CY
SUFFIX: B	SUFFIX: B
SUFFIX: D	SUFFIX: D
SUFFIX: F	SUFFIX: F
SUFFIX: L	SUFFIX: L
SUFFIX: P	SUFFIX: P
6116L120T	7C128-45C*
6116L120TB	7C128-45M*
6116L150T	7C128-45C*
6116L150TB	7C128-45M*
6116L90T	7C128-45C*
6116L90TB	7C128-45M*
6116S120T	7C128-45C
6116S120TB	7C128-45M
6116S150TB	7C128-45M
6116S70T	7C128-45C
6116S90T	7C128-45C
6116S90TB	7C128-45M
6167L45	7C167-45C*
6167L45B	7C167-45M*
6167L55	7C167-45C*
6167L55B	7C167-45M*
6167L70	7C167-45C*
6167L70B	7C167-45M*
6167L85	7C167-45C*
6167L85B	7C167-45M*
6167S45	7C167-45C
6167S45B	7C167-45M
6167S55	7C167-45C
6167S55B	7C167-45M
6167S70	7C167-45C
6167S70B	70C167-45M
6167S70B	7C167-45M
6167S85	7C167-45C
6167S85B	7C167-45M
6168L45	7C168-45C*
6168L45B	7C168-45M*
6168L55	7C168-45C*
6168L55B	7C168-45M*
6168L70	7C168-45C*
6168L70B	7C168-45M*
6168L85	7C168-45C*
6168L85B	7C168-45M*
6168S45	7C168-45C
6168S55	7C168-45C
6168S55B	7C168-45M
6168S70	7C168-45C
6168S70B	7C168-45M

IDT	CYPRESS
6168S85	7C168-45C
6168S85B	7C168-45M
7187L45	7C187-45C*
7187L55	7C187-45C*
7187L55B	7C187-45M*
7187L70	7C187-45C*
7187L70B	7C187-45M*
7187L85B	7C187-45M*
7187S45	7C187-35C
7187S55	7C187-45C
7187S55B	7C187-45M
7187S70	7C187-45C
7187S70B	7C187-45M
7187S85B	7C187-45M

INMOS	CYPRESS
PREFIX: IMS	PREFIX: CY
SUFFIX: B	SUFFIX: B
SUFFIX: P	SUFFIX: P
SUFFIX: S	SUFFIX: D
SUFFIX: W	SUFFIX: L
1400-35	7C167-35C
1400-35M	7C167-35M
1400-45	7C167-45C
1400-45M	7C167-45M
1400-55	7C167-45C
1400-55M	7C167-45M
1400L-10	7C167-45C
1400L-10M	7C167-45M
1400L-70	7C167-45C
1400L-70M	7C167-45M
1420-45	7C168-35C
1420-55	7C168-45C
1420-55M	7C168-45M
1420-70M	7C168-45M
1420L-10	7C168-45C
1420L-70	7C168-45C
1421-40	7C169-40C
1421-40M	7C169-40M
1421-50	7C169-40C
1421-50M	7C169-40M
1423-35	7C168-35C
1423-45	7C168-45C
1600-45	7C187-35C
1600-55	7C187-45C
1600-55M	7C187-45M
1600-70	7C187-45C
1600-70M	7C187-45M
1600-85M	7C187-45M

INTEL	CYPRESS
PREFIX: D	SUFFIX: D

INTEL	CYPRESS
PREFIX: L	SUFFIX: L
PREFIX: P	SUFFIX: P
SUFFIX: /B	SUFFIX: B
2147H	2147-55C
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147HL	7C147-45C
2148H	2148-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148HL	21L48-55C
2148HL-3	21L48-55C
2149H	2149-55C
2149H-1	2149-35C
2149H-2	2149-55C
2149H-3	2149-55C
2149HL	21L49-55C
51C67-35	7C167-35C
M2147H	2147-55M
M2147H-3	2147-55M
M2148H	2148-55M
M2149H	2149-55M
M2149H-2	2149-45M
M2149H-3	2149-55M

MMI	CYPRESS
SUFFIX: 883B	SUFFIX: B
SUFFIX: F	SUFFIX: F
SUFFIX: J	SUFFIX: D
SUFFIX: L	SUFFIX: L
SUFFIX: N	SUFFIX: P
5381-1	7C282-45M
5381-2	7C282-45M
5381S-1	7C281-45M
5381S-2	7C281-45M
53S1681	7C292-50M
53S1681A	7C292-50M
53S1681AS	7C291-50M
53S1681AS	7C291-50M
57401	7C401-10M
57401A	7C401-10M
57401B	7C403-25M
57401D	7C403-25M
57402	7C402-10M
57402A	7C402-10M
57402B	7C404-25M
57402D	7C404-25M
6381-1	7C282-45C
6381-2	7C282-45C
6381S-1	7C281-45C
6381S-2	7C281-45C

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Product Line Cross Reference (Continued)

MMI	CYPRESS
63S1681	7C292-50C
63S1681A	7C292-35C
63S1681AS	7C291-50C
63S1681AS	7C291-35C
67401	7C401-10C
67401A	7C401-15C
67401B	7C403-25C
67401D	7C403-25C
67402	7C402-10C
67402A	7C402-15C
67402B	7C404-25C
67402D	7C404-25C
67L401	7C401-10C
67L402	7C402-10C
C57401	7C401-10M
C57401A	7C401-10M
C57401B	7C403-25M
C57402	7C402-10M
C57402A	7C402-10M
C57402B	7C404-25M
C67401	7C401-10C
C67401A	7C401-15C
C67401B	7C403-25C
C67402	7C402-10C
C67402A	7C402-15C
C67402B	7C404-25C
PAL16L8A-2C	PAL16L8A-2C
PAL16L8A-2M	PAL16L8A-2M
PAL16L8AC	PAL16L8AC
PAL16L8AM	PAL16L8AM
PAL16L8C	PAL16L8A-2C
PAL16L8M	PAL16L8A-2M
PAL16R4A-2C	PAL16R4A-2C
PAL16R4A-2M	PAL16R4A-2M
PAL16R4AC	PAL16R4AC
PAL16R4AM	PAL16R4AM
PAL16R4C	PAL16R4A-2C
PAL16R4M	PAL16R4A-2M
PAL16R6A-2C	PAL16R6A-2C
PAL16R6A-2M	PAL16R6A-2M
PAL16R6AC	PAL16R6AC
PAL16R6AM	PAL16R6AM
PAL16R6C	PAL16R6A-2C
PAL16R6M	PAL16R6A-2M
PAL16R8A-2C	PAL16R8A-2C
PAL16R8A-2M	PAL16R8A-2M
PAL16R8AC	PAL16R8AC
PAL16R8AM	PAL16R8AM
PAL16R8C	PAL16R8A-2C
PAL16R8M	PAL16R8A-2M

MOTOROLA	CYPRESS
PREFIX:MCM	PREFIX:CY
SUFFIX:P	SUFFIX:P
SUFFIX:S	SUFFIX:D
SUFFIX:Z	SUFFIX:L
2016H-45	7C128-45C
2016H-55	7C128-55C
2016H-70	7C128-55C
2167H-35	7C167-35C
2167H-45	7C167-45C
2167H-55	7C167-45C
61[L]47-55	7C147-45C*
61[L]47-70	7C147-45C*
76161	7C292-50C
76161A	7C292-50C
7681	7C282-45C
7681A	7C282-45C
93422	93422C
93422A	93422AC
93L422	93L422C
93L422A	93L422AC

NATIONAL	CYPRESS
PREFIX:DM	PREFIX:CY
PREFIX:IDM	PREFIX:CY
PREFIX:NMC	PREFIX:CY
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
2147H	2147-55C
2147H	2147-55M
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147H-3	2147-55M
2147H-3L	7C147-45C
2148H	2148-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148H-3L	21L48-55C
2148HL	21L48-55C
54S189	54S189M
54S189A	7C189-25M
74S189	74S189C
74S189A	27S03AC
75S07	7C190-25M
75S07A	27S07AM
77LS181	7C282-45M
77S181	7C282-45M
77S181A	7C282-45M
77S191	7C292-50M
77S191A	7C292-50M
77S191B	7C292-50M
77S281	7C281-45M

NATIONAL	CYPRESS
77S281A	7C281-45M
77S291	7C291-50M
77S291A	7C291-50M
77S291B	7C291-50M
77S401	7C401-10M
77S401A	7C401-10M
77S402	7C402-10M
77S402A	7C402-10M
77SR181	7C235-40M
77SR25	7C225-40M
77SR25B	7C225-40M
77SR476	7C225-40M
77SR476B	7C225-40M
85S07	27S07C
85S07A	27S07AC
87LS181	7C282-45C
87S181	7C282-45C
87S181A	7C282-45C
87S191	7C292-50C
87S191A	7C292-35C
87S191B	7C292-35C
87S281	7C281-45C
87S281A	7C281-45C
87S291	7C291-50C
87S291A	7C291-35C
87S291B	7C291-35C
87S401	7C401-10C
87S401A	7C401-15C
87S402	7C402-10C
87S402A	7C402-15C
87SR25	7C225-40C
87SR25B	7C225-30C
87SR476	7C225-40C
87SR476B	7C225-30C
PAL16L8AC	PAL16L8AC
PAL16L8AM	PAL16L8AM
PAL16L8C	PAL16L8A-2C
PAL16L8M	PAL16L8A-2M
PAL16R4AC	PAL16R4AC
PAL16R4AM	PAL16R4AM
PAL16R4C	PAL16R4A-2C
PAL16R4M	PAL16R4A-2M
PAL16R6AC	PAL16R6AC
PAL16R6AM	PAL16R6AM
PAL16R6C	PAL16R6A-2C
PAL16R6M	PAL16R6A-2M
PAL16R8AC	PAL16R8AC
PAL16R8AM	PAL16R8AM
PAL16R8C	PAL16R8A-2C
PAL16R8M	PAL16R8A-2M

NEC	CYPRESS
PREFIX:uPD	PREFIX:CY
SUFFIX:C	SUFFIX:P
SUFFIX:D	SUFFIX:D
2147-2	2147-55C
2147-3	2147-55C
2147A-25	7C147-25C
2147A-35	2147-35C
2147A-45	2147-45C
2149	2149-55C
2149-1	2149C-45C
2149-2	2149-35C
2167-2	7C167-45C
2167-3	7C167-45C

RAYTHEON	CYPRESS
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
29631AC	7C282-45C
29631AM	7C282-45M
29631ASC	7C281-45C
29631ASM	7C281-45M
29631C	7C282-45C
29631M	7C282-45M
29631SC	7C281-45C
29631SM	7C281-45M
29633AC	7C282-45C+
29633AM	7C282-45M+
29633ASC	7C281-45C+
29633ASM	7C281-45M+
29633C	7C282-45C+
29633M	7C282-45M+
29633SC	7C281-45C+
29633SM	7C281-45M+
29681AC	7C292-50C
29681AM	7C292-50M
29681ASC	7C291-50C
29681ASM	7C291-50M
29681C	7C292-50C
29681M	7C292-50M
29681SC	7C291-50C
29681SM	7C291-50M
29683AC	7C292-50C+
29683AM	7C292-50M+
29683ASC	7C291-50C+
29683ASM	7C291-50M+
29683C	7C292-50C+
29683M	7C292-50M+
29683SC	7C291-50C+
29683SM	7C291-50M+

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Product Line Cross Reference (Continued)

SIGNETICS	CYPRESS
PREFIX:N	PREFIX:CY
PREFIX:S	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:D
SUFFIX:G	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:R	SUFFIX:F
N74S189	74S189C
N82LS181	7C282-45C
N82S181	7C282-45C
N82S181A	7C282-45C
N82S181B	7C282-45C
N82S191A__3	7C291-50C
N82S191A__6	7C292-50C
N82S191B__3	7C291-35C
N82S191B__6	7C292-35C
N82S191__3	7C291-50C
N82S191__6	7C292-50C
S54S189	54S189M
S82LS181	7C282-45M
S82S181	7C282-45M
S82S181A	7C282-45M
S82S191A__3	7C291-50M
S82S191A__6	7C292-50M
S82S191B__3	7C291-50M
S82S191B__6	7C292-50M
S82S191__3	7C291-50M
S82S191__6	7C292-50M

SYNERTEK	CYPRESS
PREFIX:D	SUFFIX:D
PREFIX:L	SUFFIX:L
PREFIX:P	SUFFIX:P
PREFIX:SY	PREFIX:CY
SUFFIX:/B	SUFFIX:B
2147H	2147-55C
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147HL	7C147-45C
2147HL-3	7C147-45C
2148H	2148-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148HL	21L48-55C
2148HL-3	21L48-55C
2149H	2149-55C
2149H-2	2149-55C
2149H-3	2149-55C
2149HL	21L49-55C
2149HL-3	21L49-55C
2167	7C167-45C

SYNERTEK	CYPRESS
2167-3	7C167-45C
2168	7C168-45C
2168-3	7C168-45C
2169	7C169-40C
2169-3	7C169-40C
M2147H	2147-55M
M2147H-2	2147-45M
M2147H-3	2147-55M
M2148	2148-55M
M2148H-3	2148-55M
M2148H-6	2148-55M
M2149H	2149-55M
M2149H-3	2149-55M
M2149H-6	2149-55M
M2167	7C167-45M
M2167-3	7C167-45M
M2168	7C168-45M
M2169	7C169-40M
M2169-3	7C169-40M

TI	CYPRESS
PREFIX:JBP	PREFIX:CY
PREFIX:SN	PREFIX:CY
PREFIX:TBP	PREFIX:CY
PREFIX:TIB	PREFIX:CY
SUFFIX:F	SUFFIX:L
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
28L166W	7C292-50C
28L86AMW	7C282-45M
28L86AW	7C282-45C
28S166W	7C292-50C
28S86AMW	7C282-45M
28S86AW	7C282-45C
54LS189A	7C189-25M+
54LS219A	7C190-25M+
54S189A	54S189M
74LS189A	7C189-25C
74LS219A	7C190-25C
74S189A	74S189C
PAL16L8A-2C	PALC16R6AC
PAL16L8A-2M	PAL16L8A-2M
PAL16L8AC	PAL16L8AC
PAL16L8AM	PAL16L8AM
PAL16R4A-2C	PALC16R4AC
PAL16R4AC	PAL16R4AC
PAL16R4AM	PAL16R4AM
PAL16R6A-2C	PALC16R6AC
PAL16R6AC	PAL16R6AC
PAL16R6AM	PAL16R6AM
PAL16R8A-2C	PALC16R8AC
PAL16R8AC	PAL16R8AC

TI	CYPRESS
PAL16R8AM	PAL16R8AM

TOSHIBA	CYPRESS
PREFIX:D	SUFFIX:D
PREFIX:P	SUFFIX:P
PREFIX:TMM	PREFIX:CY
2018-45	7C128-45C
2018-55	7C128-55C
2019-35	7C128-35C
2068-45	7C168-45C
2068-55	7C1168-45C
2069-35	7C169-35C
315	2147-55C
315-1	2147-55C
5561-55	7C187-45C

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Product Selection Guide

	Size	Organization	Pins	Cypress			Closest Competitor		
				Part Number	Speed (ns)	I_{CC} (mA @ ns)	Part Number	Speed (ns)	I_{CC} (mA @ ns)
SRAMs	64	16 x 4—Inverting	16	CY7C189	t_{AA} = 18, 25	55 @ 25	27S07A	t_{AA} = 25, 35	100 @ 25
	64	16 x 4—Non-Inverting	16	CY7C190	t_{AA} = 18, 25	55 @ 25	27S03A	t_{AA} = 25, 35	100 @ 25
	64	16 x 4—Inverting	16	CY74S189	t_{AA} = 35	90 @ 35	74S189	t_{AA} = 35	110 @ 35
	64	16 x 4—Inverting	16	CY27S03A	t_{AA} = 25, 35	90 @ 25	27S07A	t_{AA} = 25, 35	100 @ 25
	64	16 x 4—Non-Inverting	16	CY27S07A	t_{AA} = 25, 35	90 @ 25	27S03A	t_{AA} = 25, 35	100 @ 25
	1024	256 x 4	22	CY7C122	t_{AA} = 15, 25, 35	80 @ 25	9122/91L22	t_{AA} = 25, 35, 45	120 @ 25
	1024	256 x 4	22	CY9122/91L22	t_{AA} = 25, 35, 45	120 @ 25	9122/91L22	t_{AA} = 25, 35, 45	120 @ 25
	1024	256 x 4	22	CY93422A/93L422A	t_{AA} = 35, 45, 60	80 @ 45	93422/L422	t_{AA} = 35, 45, 60	80 @ 45
	4096	4096 x 1—$\overline{CS}$ Power Down	18	CY7C147	t_{AA} = 25, 35, 45	60/10 @ 35	2147	t_{AA} = 35, 45, 55, 70	125/15 @ 45
	4096	4096 x 1—$\overline{CS}$ Power Down	18	CY2147/21L47	t_{AA} = 35, 45, 55	120/10 @ 35	2147	t_{AA} = 35, 45, 55, 70	125/15 @ 45
	4096	1024 x 4—$\overline{CS}$ Power Down	18	CY7C148	t_{AA} = 25, 35, 45	80/10 @ 35	2148	t_{AA} = 35, 45, 55, 70	180/30 @ 35
	4096	1024 x 4—$\overline{CS}$ Power Down	18	CY2148/21L48	t_{AA} = 35, 45, 55	120/20 @ 35	2148	t_{AA} = 35, 45, 55, 70	125/20 @ 45
	4096	1024 x 4	18	CY7C149	t_{AA} = 25, 35, 45	80 @ 35	2149	t_{AA} = 35, 45, 55, 70	125 @ 45
	4096	1024 x 4	18	CY2149/21L49	t_{AA} = 35, 45, 55	120 @ 35	2149	t_{AA} = 35, 45, 55, 70	125 @ 45
	4096	1024 x 4—Separate I/O	24S	CY7C150	t_{AA} = 25, 35, 45	90 @ 25	9150	t_{AA} = 25, 35, 45	180 @ 25
	16384	2048 x 8—$\overline{CS}$ Power Down	24S	CY7C128	t_{AA} = 35, 45, 55	90/20 @ 45	2016H/2018	t_{AA} = 45, 55, 70	150/20 @ 45
	16384	2048 x 8	24S	CY7C129	t_{AA} = 35, 45, 55	90 @ 45	2019	t_{AA} = 35	180 @ 35
	16384	16384 x 1—$\overline{CS}$ Power Down	20	CY7C167	t_{AA} = 25, 35, 45	100/20 @ 35	2167/1400	t_{AA} = 35, 45, 55	120/20 @ 35
	16384	4096 x 4—$\overline{CS}$ Power Down	20	CY7C168	t_{AA} = 25, 35, 45	90/20 @ 35	2168/1420	t_{ACS} = 45, 55, 70	110/30 @ 45
	16384	4096 x 4	20	CY7C169	t_{AA} = 25, 35, 40	90 @ 35	2169/1421	t_{AA} = 40, 50, 70	110 @ 40
	16384	4096 x 4—Output Enable	22	CY7C170	t_{AA} = 35, 45	90 @ 35			
	65536	65536 x 1—$\overline{CS}$ Power Down	22	CY7C187	t_{AA} = 35, 45	115/20 @ 35	7187/1600	t_{AA} = 45, 55, 70	TBD
FIFOs	256	64 x 4—Cascadable	16	CY7C401	10, 15 MHz	75	C67401	10, 15, 16.7 MHz	160, 170, 180
	320	64 x 5—Cascadable	18	CY7C402	10, 15 MHz	75	C67402	10, 15, 16.7 MHz	180, 190, 200
	256	64 x 4—Cascadable/$\overline{OE}$	16	CY7C403	10, 15, 25 MHz	75			
	320	64 x 5—Cascadable/$\overline{OE}$	18	CY7C404	10, 15, 25 MHz	75			
	256	64 x 4—Cascadable	16	CY3341	1.2 MHz	45	3341/A	0.7, 1.0 MHz	~90
PROMs	4096	512 x 8—Registered	24S	CY7C225	t_{SA}/CO = 30/15, 40/25	90		t_{SA}/t_{CO} = 30/20, 50/27	185
	8192	1024 x 8—Registered	24S	CY7C235	t_{SA}/CO = 30/15, 40/20	90		t_{SA}/t_{CO} = 35/20, 40/25	185
	8192	1024 x 8	24S	CY7C281	t_{AA} = 30, 45	90		t_{AA} = 35, 50, 60, 65	170
	8192	1024 x 8	24	CY7C282	t_{AA} = 30, 45	90		t_{AA} = 35, 50, 60, 65	135
	16384	2048 x 8—Registered	24S	CY7C245	t_{SA}/CO = 35/15, 45/25	90		t_{SA}/t_{CO} = 40/20, 45/25	185
	16384	2048 x 8	24S	CY7C291	t_{AA} = 35, 50	90		t_{AA} = 35, 50, 65	175
	16384	2048 x 8	24	CY7C292	t_{AA} = 35, 50			t_{AA} = 35, 50, 65	175
PALs		16L8	20	CYPALC16L8A	t_{PD} = 25	90			
		16R8	20	CYPALC16R8A	t_S/CO = 20/15	90			
		16R6	20	CYPALC16R6A	$t_{PD}/S/CO$ = 25/20/15	90			
		16R4	20	CYPALC16R4A	$t_{PD}/S/CO$ = 25/20/15	90			
		16L8	20	CYPAL16L8A	t_{PD} = 25	155	PAL16L8A	t_{PD} = 25	180
		16R8	20	CYPAL16R8A	t_S/CO = 20/15	155	PAL16R8A	t_S/CO = 20/15	180
		16R6	20	CYPAL16R6A	$t_{PD}/S/CO$ = 25/20/15	155	PAL16R6A	$t_{PD}/S/CO$ = 25/20/15	180
		16R4	20	CYPAL16R4A	$t_{PD}/S/CO$ = 25/20/15	155	PAL16R4A	$t_{PD}/S/CO$ = 25/20/15	180
		16L8	20	CYPAL16L8A-2	t_{PD} = 35	90	PAL16L8A-2	t_{PD} = 35	90
		16R8	20	CYPAL16R8A-2	t_S/CO = 30/25	90	PAL16R8A-2	$t_S/20$ = 30/25	90
		16R6	20	CYPAL16R6A-2	$t_{PD}/S/CO$ = 35/30/25	90	PAL16R6A-2	$t_{PD}/S/CO$ = 35/30/25	90
		16R4	20	CYPAL16R4A-2	$t_{PD}/S/CO$ = 35/30/25	90	PAL16R4A-2	$t_{PD}/S/CO$ = 35/30/25	90
		22V10	24S	CYPALC22V10	$t_{PD}/S/CO$ = 30/25/15	120	22V10	$t_{PD}/S/CO$ = 25/25/15	180
		32V10	24S	CYPALC32V10	$t_{PD}/S/CO$ = 30/25/15	120			
LOGIC		2901—4 Bit Slice	40	CY7C901	t_{CLK} = 31, 69	70	2901	B, C	265
		2901—4 Bit Slice	40	CY8C901	t_{CLK} = 31, 69	26.5	2901	B, C	265
		2901—4 Bit Slice	40	CY2901	B, C	140	2901	B, C	265
		2909/2911—Sequencer	40	CY7C909/911	t_{CLK} = 30, 40	55	2909/2911	A	130
		2909/2911—Sequencer	40	CY2909/2911	A	110	2909/2911	A	130
		2910—Controller	40	CY7C910	t_{CLK} = 50, 93	100	2910	A	344
		2910—Controller	40	CY2910	A	200	2910	A	344

Note:

The above specifications are for the commercial temperature range of 0° to 70° Celsius.

Military temperature range (−55° to +125° Celsius) product is also available. Speed and power selections may vary from those above.

Commercial grade product is available in PLASTIC, CERDIP, or LCC. Military grade product is available in CERDIP or LCC.

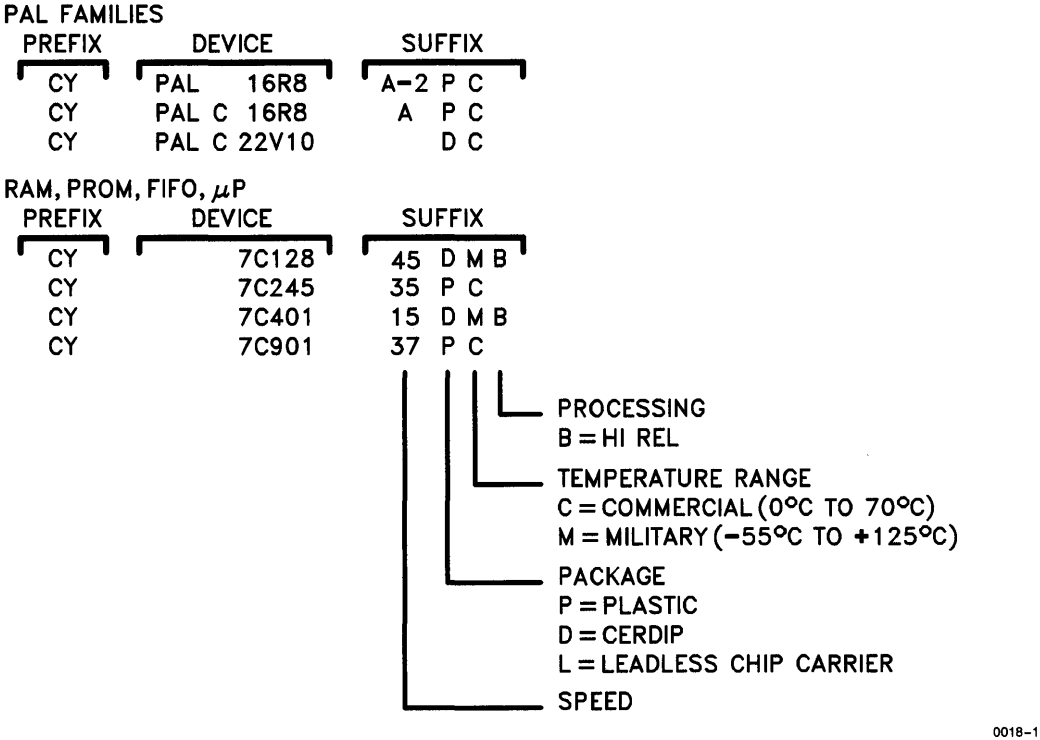
All outputs are three-state.

All power supplies are V_{CC} = 5V ±10%.

24S stands for 24-pin 300 mil.

Ordering Information

Specific ordering codes are indicated in the detailed 7CXXX data sheets. In general, the product codes follow the format below:



0018-1

i.e. CY7C128-35PC, CY PALC16R8APC

Cypress FSCM #7Z018

CYPRESS SEMICONDUCTOR

Section Contents

Static RAMs (Random Access Memory)

CYPRESS SEMICONDUCTOR

CY2147

4096 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  — 35 ns
- **Low active power**
  — 690 mW (commercial)
  — 770 mW (military)
- **Low standby power**
  — 140 mW
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

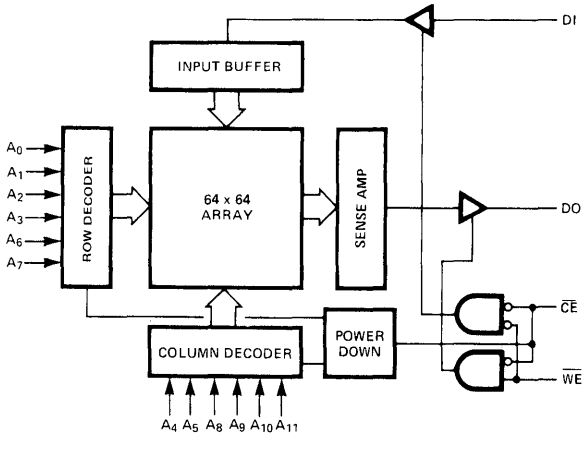
The CY2147 is a high performance CMOS static RAM organized as 4096 x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY2147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

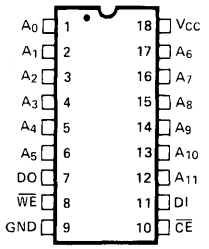
The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



0013-1

Pin Configuration



0013-2

2

Selection Guide (For higher performance and lower power refer to CY7C147 data sheet.)

		2147-35	2147-45	2147-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	125	125	125
	Military		140	140
Maximum Standby Current (mA)	Commercial	25	25	25
	Military		25	25

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		125	mA
			Military		140	
I_{SB_1}	Automatic $\overline{CE}$[3] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		25	mA
			Military		25	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute air flow.
2. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested on a sample basis.

AC Test Loads and Waveforms

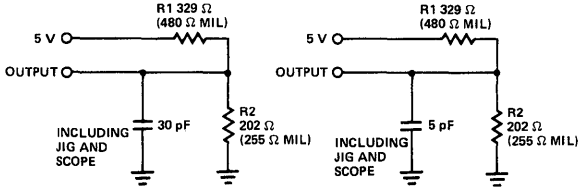
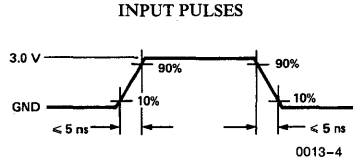


Figure 1a

Figure 1b

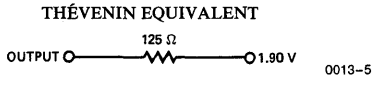
0013-3



0013-4

Figure 2

Equivalent to:



0013-5

Switching Characteristics Over Operating Range[5]

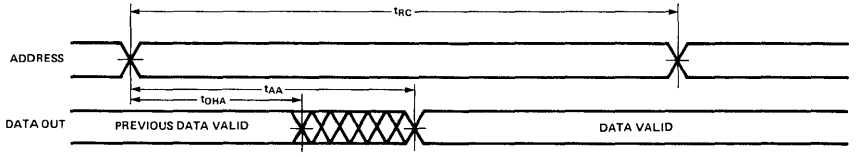
Parameters	Description	2147-35		2147-45		2147-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		30		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		20	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		45		45		ns
t_{AW}	Address Set-up to Write End	35		45		45		ns
t_{HA}	Address Hold from Write End	0		0		10		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-up to Write End	20		25		25		ns
t_{HD}	Data Hold from Write End	10		10		10		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low[7]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	0	20	0	25	0	25	ns

Notes:

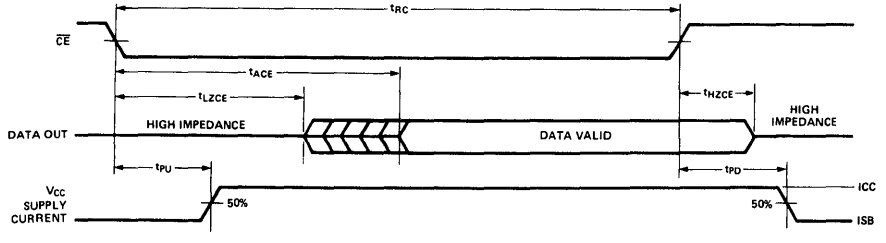
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 9, 10)

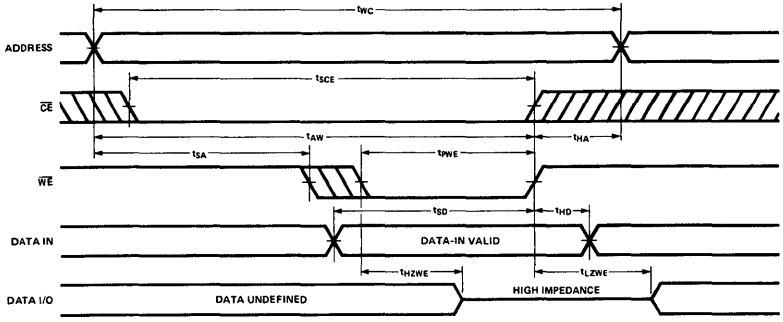


Read Cycle No. 2 (Notes 9, 11)



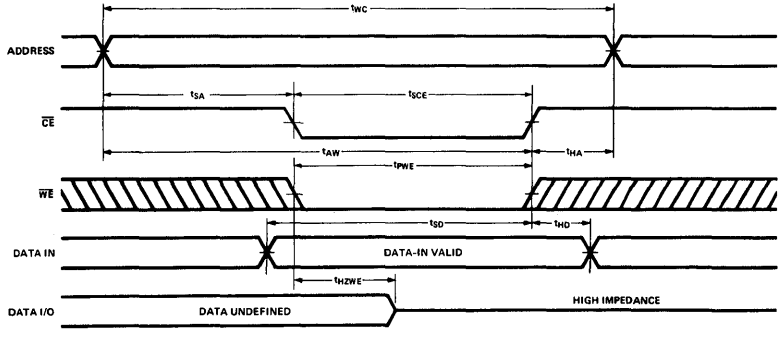
Switching Waveforms (Continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 8)



0013-8

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 8)



0013-9

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2147-35 PC	P5	Commercial
	CY2147-35 DC	D6	
45	CY2147-45 PC	P5	Commercial
	CY2147-45 DC	D6	
	CY2147-45 DMB	D6	Military
55	CY2147-55 PC	P5	Commercial
	CY2147-55 DC	D6	
	CY2147-55 DMB	D6	Military

CY2148/CY21L48
CY2149/CY21L49

CYPRESS SEMICONDUCTOR

1024 x 4 Static R/W RAM

Features

- **Automated power-down when deselected (2148)**
- **CMOS for optimum speed/ power**
- **Low power**
  — 660 mW (commercial)
  — 770 mW (military)
- **5 volt power supply ±10% tolerance both commercial and military**
- **TTL compatible inputs and outputs**

Functional Description

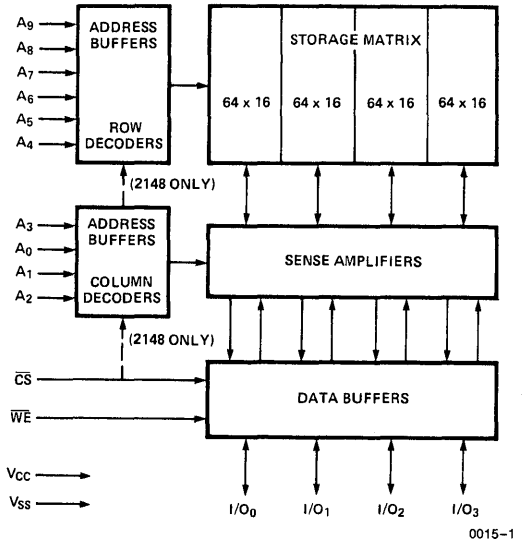
The CY2148 and CY2149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}$) input, and three-state outputs. The CY2148 and CY2149 are identical except that the CY2148 includes an automatic ($\overline{CS}$) power-down feature. The CY2148 remains in a low power mode as long as the device remains unselected, i.e. ($\overline{CS}$) is high, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY2149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

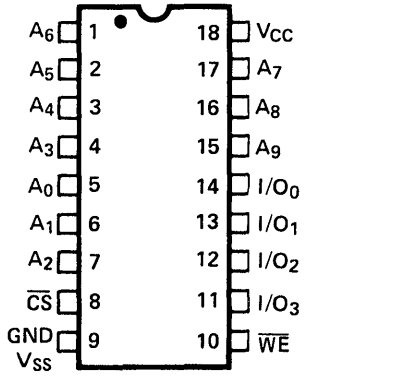
Reading the device is accomplished by selecting the device, ($\overline{CS}$) active low, while ($\overline{WE}$) remains inactive or high. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins (I/O_0 through I/O_3) remain in a high impedance state unless the chip is selected, and write enable ($\overline{WE}$) is high.

Logic Block Diagram



Pin Configuration



Selection Guide (For Higher Performance and Lower Power Refer to CY7C148/9 Data Sheet)

		2148/9-35	21L48/9-35	2148/9-45	21L48/9-45	2148/9-55	21L48/9-55
Maximum Access Time (ns)		35	35	45	45	55	55
Maximum Operating Current (mA)	Commercial	140	120	140	120	140	120
	Military			140		140	

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[11]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		21L48/9 Min.	21L48/9 Max.	2148/9 Min.	2148/9 Max.	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	T_A = 70°C	8		8		mA
			T_A = 125°C			8		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$			10		10	µA
I_{OZ}	Output Leakage Current	GND ≤ $V_O \le V_{CC}$ Output Disabled	T_A = −55°C to +125°C	−50	50	−50	50	µA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0V, V_{CC} = 5V			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \le V_{IL}$ Output Open	T_A = 0°C to +70°C		120		140	mA
			T_A = −55°C to +125°C				140	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, $\overline{CS} \ge V_{IH}$ 2148 only	T_A = 0°C to +70°C		20		30	mA
			T_A = −55°C to +125°C				30	
I_{PO}	Peak Power-On Current	Max. V_{CC}, $\overline{CS} \ge V_{IH}$[3] 2148 only	T_A = 0°C to +70°C		30		50	mA
			T_A = −55°C to +125°C				50	
I_{OS}	Output Short Circuit Current	GND ≤ $V_O \le V_{CC}$[10]	T_A = 0°C to +70°C		±275		±275	mA
			T_A = −55°C to +125°C				±350	

Notes:

1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise current will exceed values given (CY2148 only).
4. Chip deselected greater than 55 ns prior to selection.
5. Chip deselected less than 55 ns prior to selection.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in *Figure 1b*. These parameters are sampled and not 100% tested.
7. $\overline{WE}$ is high for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition low.
10. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
11. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

AC Test Loads and Waveforms

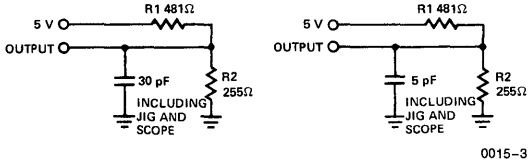
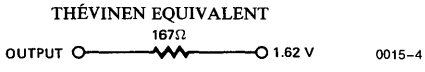


Figure 1a **Figure 1b**

Equivalent to:



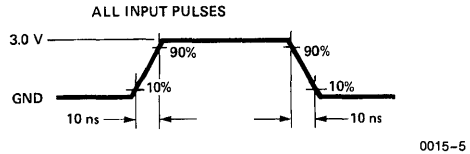


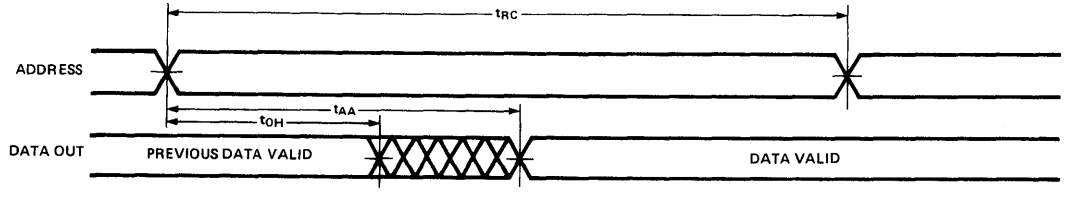
Figure 2

Switching Characteristics

Parameters	Description		2148/9-35		2148/9-45		2148/9-55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55	ns
t_{ACS1}[4]	Chip Select Low to Data Out Valid (CY2148 only)			35		45		55	ns
t_{ACS2}[5]				45		55		65	
t_{ACS}	Chip Select Low to Data Out Valid (CY2149 only)			15		20		25	ns
t_{LZ}[6]	Chip Select Low to Data Out On	2148	10		10		10		ns
		2149	5		5		5		
t_{HZ}[6]	Chip Select High to Data Out Off		0	20	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		5		5		ns
t_{PD}	Chip Select High to Power-Down Delay	2148		30		30		30	ns
t_{PU}	Chip Select Low to Power-Up Delay	2148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		ns
t_{WP}[2]	Write Enable Low to Write Enable High		30		35		40		ns
t_{WR}	Write Enable High to Address		5		5		5		ns
t_{WZ}[6]	Write Enable Low to Output in High Z		0	10	0	15	0	20	ns
t_{DW}	Data in Valid to Write Enable High		20		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable Low		0		0		0		ns
t_{CW}[2]	Chip Select Low to Write Enable High		30		40		50		ns
t_{OW}[6]	Write Enable High to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		30		35		50		ns

Switching Waveforms

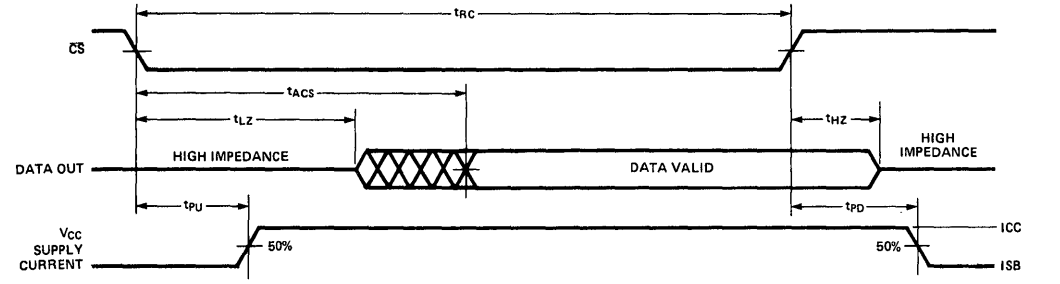
Read Cycle No. 1 (Notes 7, 8)



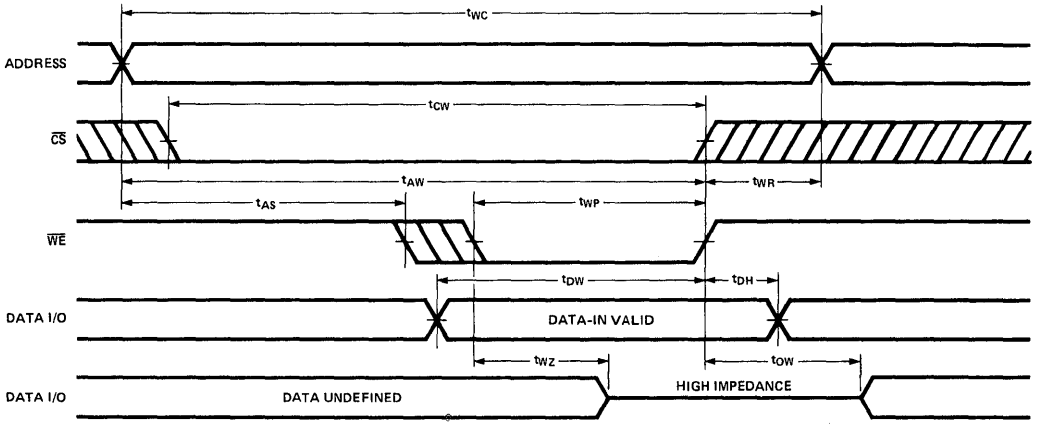
0015-6

Switching Waveforms (Continued)

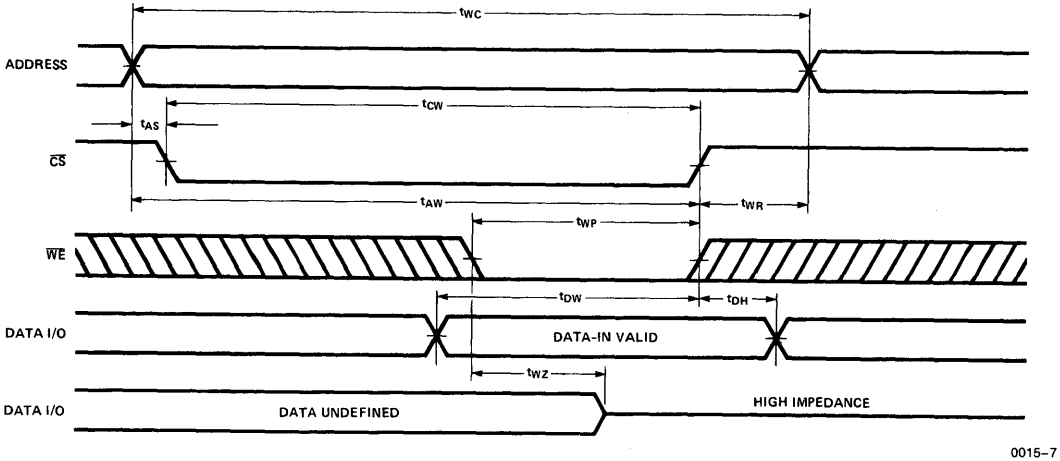
Read Cycle No. 2 (Notes 7, 9)



Write Cycle No. 1 ($\overline{WE}$ Controlled)



Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2148-35 PC CY2149-35 PC	P3	Commercial
	CY2148-35 DC CY2149-35 DC	D4	
	CY21L48-35 PC CY21L49-35 PC	P3	Commercial
	CY21L48-35 DC CY21L49-35 DC	D4	
45	CY2148-45 PC CY2149-45 PC	P3	Commercial
	CY2148-45 DC CY2149-45 DC	D4	
	CY2148-45 DMB CY2149-45 DMB	D4	Military
	CY21L48-45 PC CY21L49-45 PC	P3	Commercial
	CY21L48-45 DC CY21L49-45 DC	D4	
55	CY2148-55 PC CY2149-55 PC	P3	Commercial
	CY2148-55 DC CY2149-55 DC	D4	
	CY2148-55 DMB CY2149-55 DMB	D4	Military
	CY21L48-55 PC CY21L49-55 PC	P3	Commercial
	CY21L48-55 DC CY21L49-55 DC	D4	

CYPRESS SEMICONDUCTOR

CY7C122

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 330 mW (commercial)**
  - **— 495 mW (military)**
- **Separate inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2000V static discharge**
- **TTL compatible inputs and outputs**

Functional Description

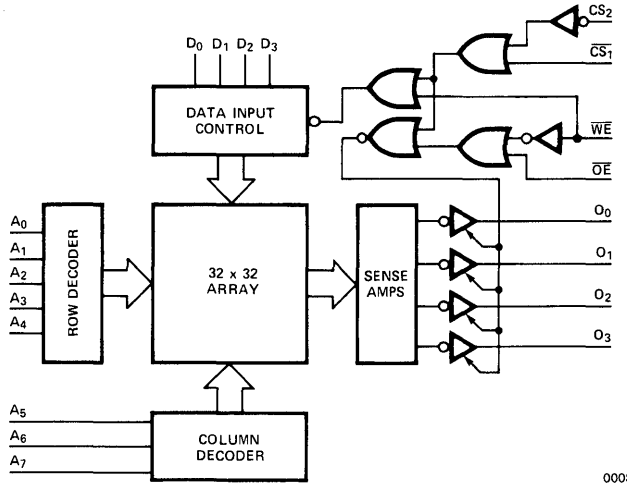
The CY7C122 is a high performance CMOS static RAM organized as 256 words x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

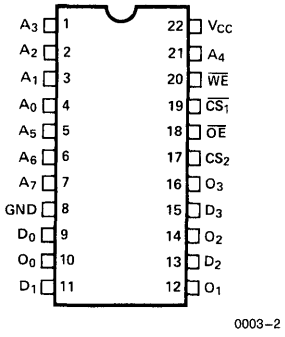
Reading is performed with the chip select one ($\overline{CS_1}$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C122-15	7C122-25	7C122-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military	NA	25	35
Maximum Operating Current (mA)	Commercial	90	60	60
	Military	NA	90	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential Pin 22 to Pin 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[7]	−55°C to +125°C	5V ±10%

Logic Table

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	D_0–D_3		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0–O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

Notes: H = HIGH Voltage L = LOW Voltage X = Don't Care
High Z = High Impedance

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C122-15		7C122-25 7C122-35		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			10		10	μA
V_{CD}	Input Diode Clamp Voltage				Note 2		Note 2	V
I_{OZ}	Output Current (High-Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH} Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current (Note 1)	V_{CC} = Max., V_{OUT} = GND	Commercial		−70		−70	mA
			Military		−80		−80	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		60	mA
			Military		NA		90	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. The CMOS process does not provide a clamp diode. However, the CY7C122 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. Tested on a sample basis.

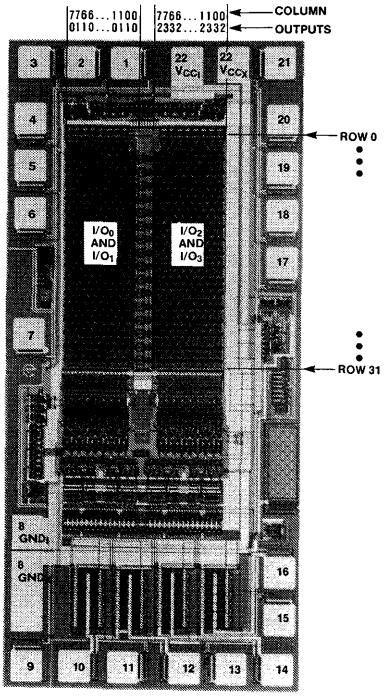
Switching Characteristics Over the Operating Range[5]

Parameters	Description	Test Conditions	CY7C122-15		CY7C122-25		CY7C122-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		15		25		35		ns
t_{ACS}	Chip Select Time			8		15		25	ns
t_{ZRCS}	Chip Select to High-Z	Note 6		12		20		30	ns
t_{AOS}	Output Enable Time			8		15		25	ns
t_{ZROS}	Output Enable to High-Z	Note 6		12		20		30	ns
t_{AA}	Address Access Time			15		25		35	ns
WRITE CYCLE									
t_{WC}	Write Cycle Time		15		25		35		ns
t_{ZWS}	Write Disable to High-Z	Note 6		12		20		30	ns
t_{WR}	Write Recovery Time			12		20		25	ns
t_W	Write Pulse Width	Note 4	11		15		25		ns
t_{WSD}	Data Setup Time Prior to Write		0		5		5		ns
t_{WHD}	Data Hold Time After Write		2		5		5		ns
t_{WSA}	Address Setup Time	Note 4	0		5		10		ns
t_{WHA}	Address Hold Time		4		5		5		ns
t_{WSCS}	Chip Select Setup Time		0		5		5		ns
t_{WHCS}	Chip Select Hold Time		2		5		5		ns

Notes:

4. t_W measured at t_{WSA} = min.; t_{WSA} measured at t_W = min.
5. Test conditions assume signal transition times of 5 ns or less for the −15 product and 10 ns or less for the −25 and −35 product. Timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in *Figure 1a.*
6. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input with load shown in *Figure 1b.*
7. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

Bit Map



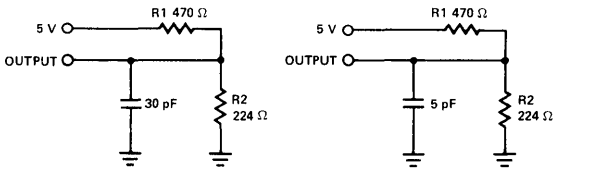
0003-3

Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	4
A_1	AX1	3
A_2	AX2	2
A_3	AX3	1
A_4	AX4	21
A_5	AY0	5
A_6	AY1	6
A_7	AY2	7

AC Test Loads and Waveforms

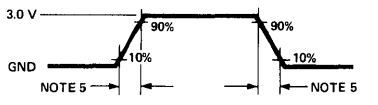
AC Test Loads



0003-4

Figure 1a **Figure 1b**

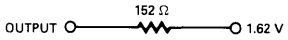
Input Pulses



0003-5

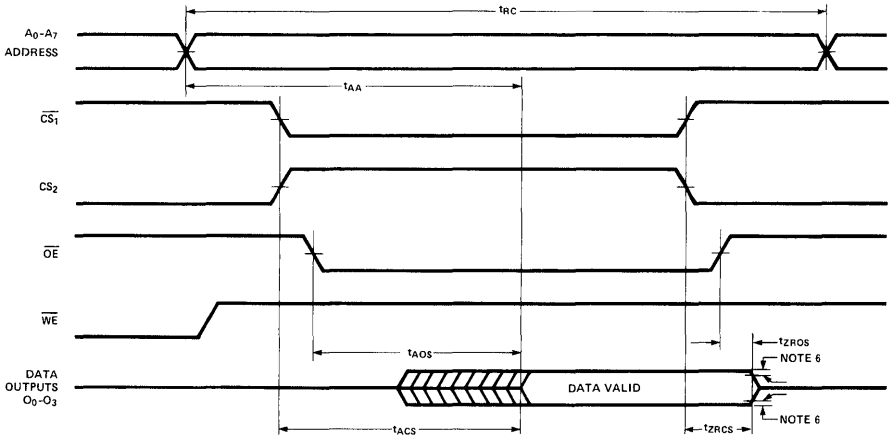
Figure 2

Equivalent to: THÉVENIN EQUIVALENT



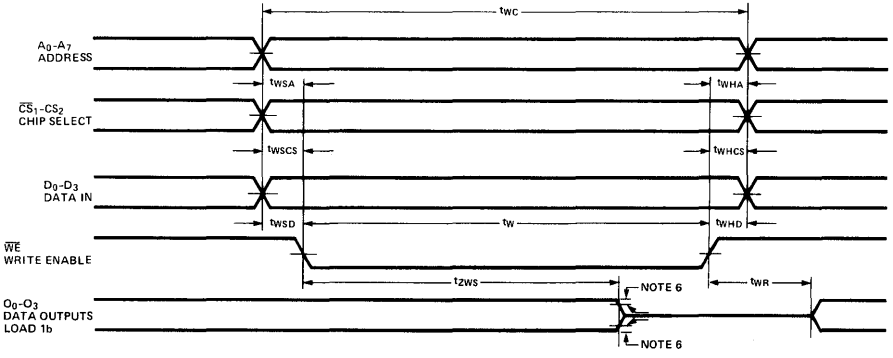
0003-6

Read Mode



0003-7

Write Mode



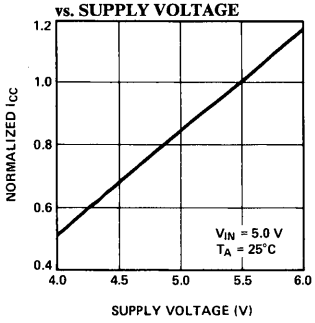
0003-8

(All above measurements referenced to 1.5V unless otherwise stated.)

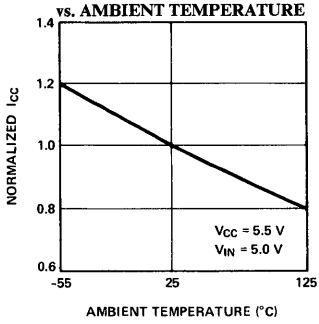
Note:
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

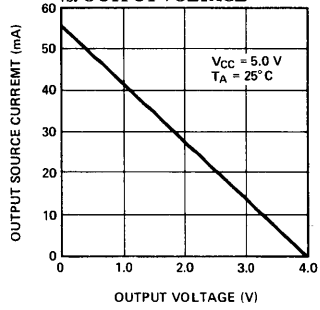
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



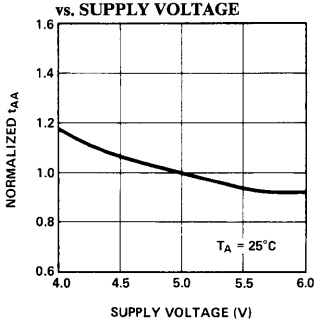
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



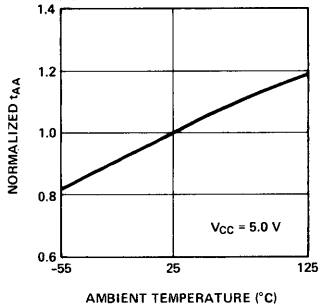
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



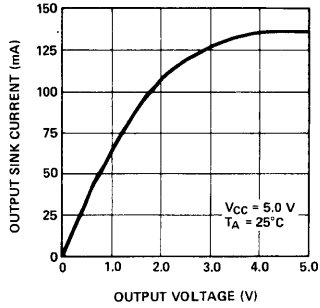
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



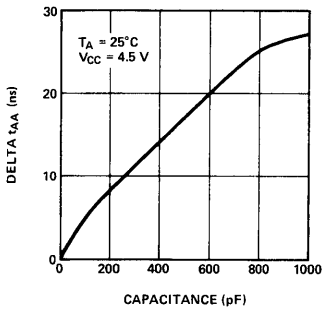
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



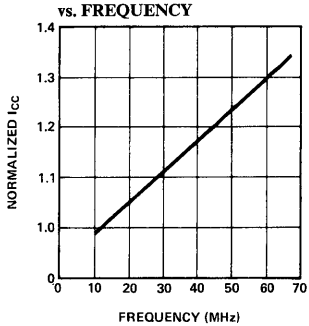
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0003-9

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C122-15PC	P7	Commercial
	CY7C122-15DC	D8	Commercial
25	CY7C122-25PC	P7	Commercial
	CY7C122-25DC	D8	Commercial
	CY7C122-25DMB	D8	Military
35	CY7C122-35PC	P7	Commercial
	CY7C122-35DC	D8	Commercial
	CY7C122-35DMB	D8	Military

CY7C128
CY7C129

CYPRESS SEMICONDUCTOR

2048 x Static R/W RAM

Features

- **Automatic power-down when deselected (7C128)**
- **CMOS for optimum speed/power**
- **High speed—35 ns**
- **Low active power**
  — 660 mW (commercial)
  — 715 mW (military)
- **Low standby power**
  — 110 mW (7C128)
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

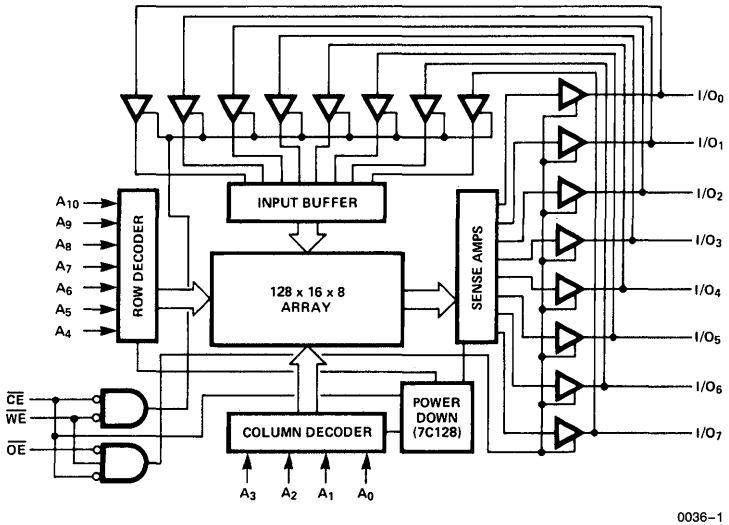
Functional Description

The CY7C128 and CY7C129 are high performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

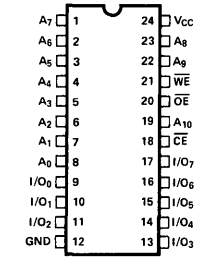
The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is high.

Logic Block Diagram

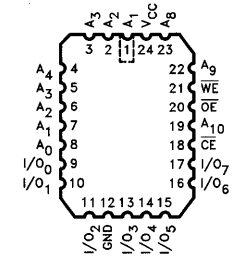


0036-1

Pin Configurations



0036-2



0036-3

Selection Guide

		7C128-35	7C128-45	7C128-55	7C129-35	7C129-45	7C129-55
Maximum Access Time (ns)		35	45	55	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	90	120	120	90
	Military		130	100		130	100
Maximum Standby Current (mA)	Commercial	20	20	20			
	Military		20	20			

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C128-35, 45 7C129-35, 45		7C128-55 7C129-55		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−40	40	−40	40	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120		90	mA
			Military*		130		100	
I_{SB} (7C128)	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		20		20	mA
			Military*		20		20	

*45 ns and 55 ns only

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

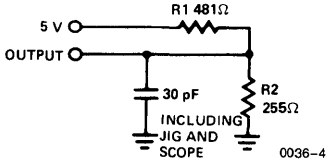


Figure 1a

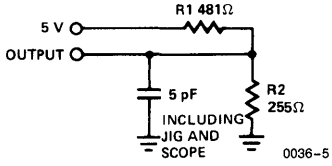


Figure 1b

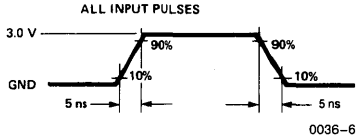
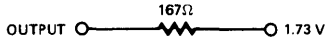


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

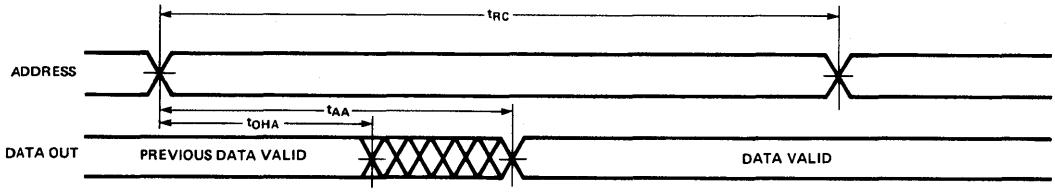
Parameters	Description		7C128-35 7C129-35		7C128-45 7C129-45		7C128-55 7C129-55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		35		45		55		ns
t_{AA}	Address to Data Valid			35		45		55	ns
t_{OHA}	Data Hold from Address Change		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	7C128		35		45		55	ns
		7C129		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid			15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]			15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	7C128	5		5		5		ns
		7C129	0		0		0		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]			15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down			20		25		25	ns
WRITE CYCLE[7]									
t_{WC}	Write Cycle Time		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		30		40		50		ns
t_{AW}	Address Set-up to Write End		30		40		50		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		ns
t_{PWE}	WE Pulse Width		20		20		25		ns
t_{SD}	Data Set-up to Write End		15		20		25		ns
t_{HD}	Data Hold from Write End		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z			15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		0		0		0		ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b.* Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for all devices. These parameters are sampled and not 100% tested. (7C128 only.)
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 8, 9)



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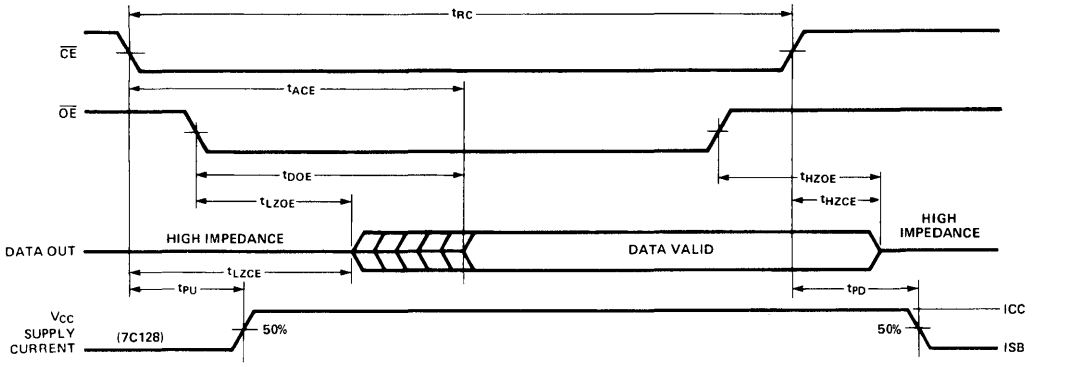
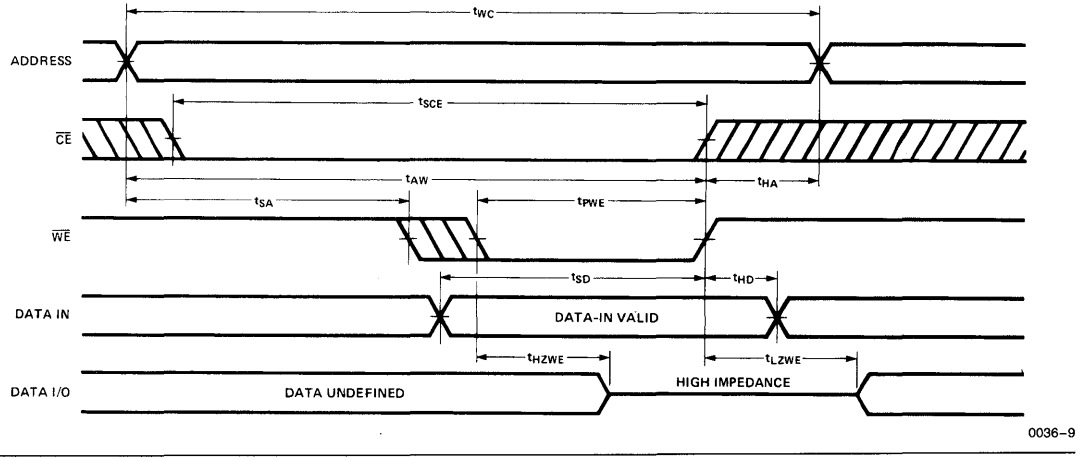
Switching Waveforms (Continued)

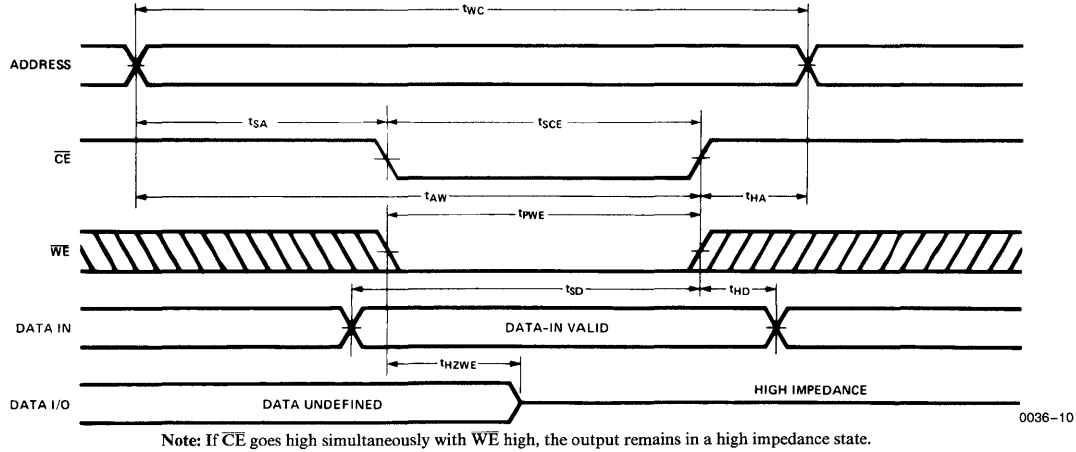
Read Cycle No. 2 (Notes 8, 10)



Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)



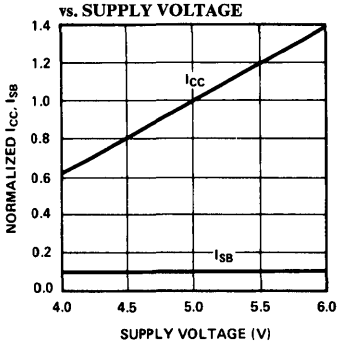
Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 7)



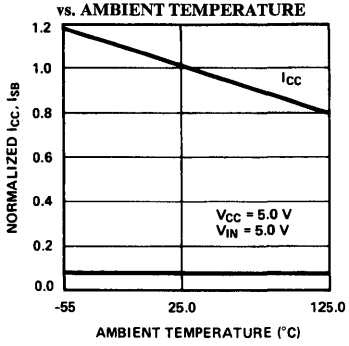
Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

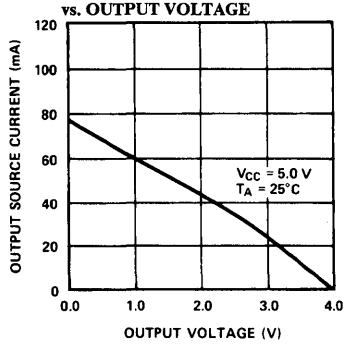
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



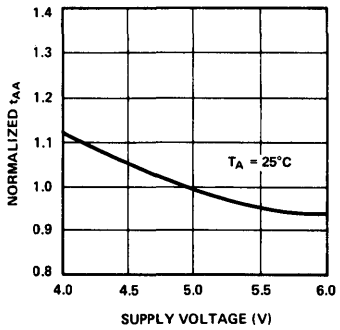
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



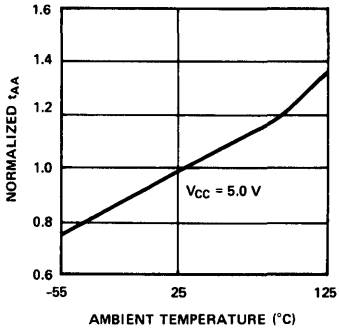
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



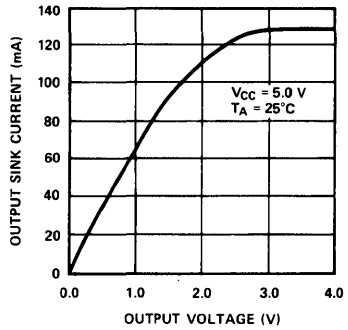
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



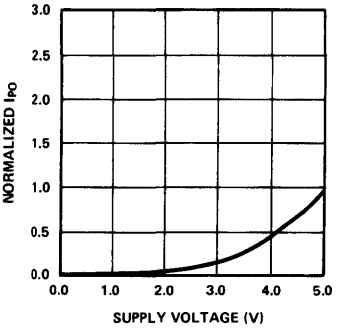
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



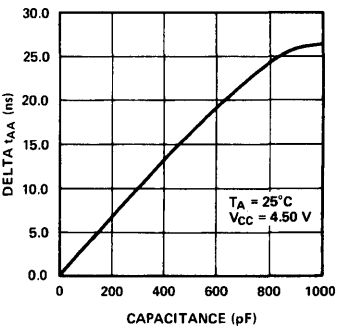
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



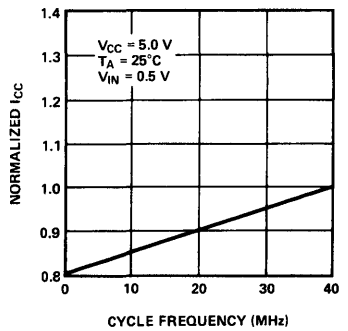
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



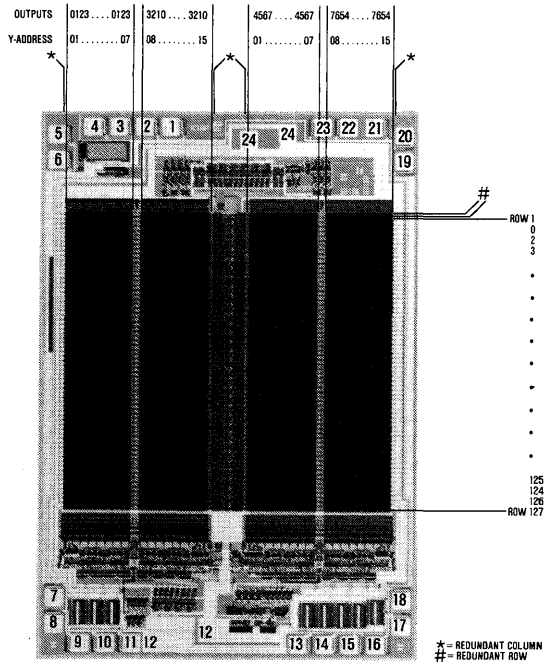
0036-11

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C128-35PC	P13	Commercial
	CY7C128-35DC	D14	Commercial
	CY7C128-35LC	L53	Commercial
45	CY7C128-45PC	P13	Commercial
	CY7C128-45DC	D14	Commercial
	CY7C128-45LC	L53	Commercial
	CY7C128-45DMB	D14	Military
	CY7C128-45LMB	L53	Military
55	CY7C128-55PC	P13	Commercial
	CY7C128-55DC	D14	Commercial
	CY7C128-55LC	L53	Commercial
	CY7C128-55DMB	D14	Military
	CY7C128-55LMB	L53	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C129-35PC	P13	Commercial
	CY7C129-35DC	D14	Commercial
	CY7C129-35LC	L53	Commercial
45	CY7C129-45PC	P13	Commercial
	CY7C129-45DC	D14	Commercial
	CY7C129-45LC	L53	Commercial
	CY7C129-45DMB	D14	Military
	CY7C129-45LMB	L53	Military
55	CY7C129-55PC	P13	Commercial
	CY7C129-55DC	D14	Commercial
	CY7C129-55LC	L53	Commercial
	CY7C129-55DMB	D14	Military
	CY7C129-55LMB	L53	Military

Bit Map



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Address Designators

Address Name	Address Function	Pin Number
A_0	Y_3	8
A_1	Y_2	7
A_2	Y_1	6
A_3	Y_0	5
A_4	X_2	4
A_5	X_4	3
A_6	X_3	2
A_7	X_0	1
A_8	X_5	23
A_9	X_6	22
A_{10}	X_1	19

CYPRESS SEMICONDUCTOR

CY7C147

4096 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power**
  - **— 55 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

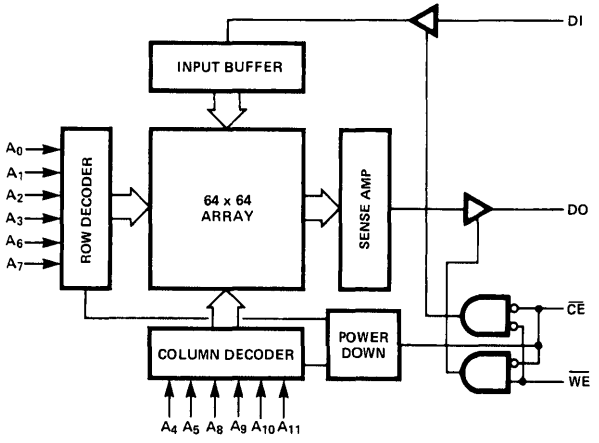
The CY7C147 is a high performance CMOS static RAM organized as 4096 x 1 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



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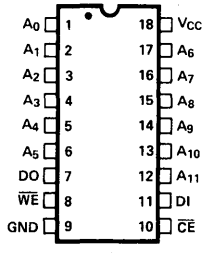
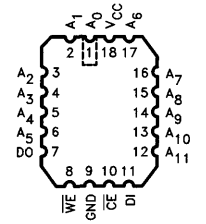
Pin Configurations



0019-2



0019-3

Selection Guide

		7C147-25	7C147-35	7C147-45
Maximum Access Time (ns)	Commercial	25	35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial	90	80	80
	Military		110	110
Maximum Standby Current (mA)	Commercial	15	10	10
	Military		10	10

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C147-25		7C147-35, 45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	−50	+50	μA
I_{OS}	Output Short[2] Circuit Current	V_{CC} = Max.	V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90		80	mA
			Military				110	
I_{SB_1}	Automatic $\overline{CE}$[3] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		15		10	mA
			Military				10	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested on a sample basis.

AC Test Loads and Waveforms

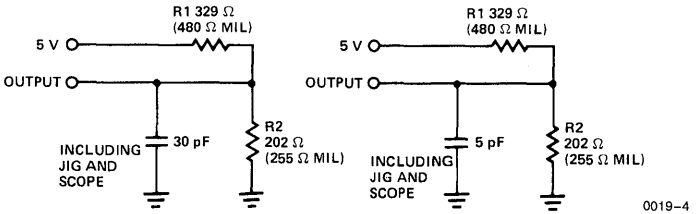


Figure 1a

Figure 1b

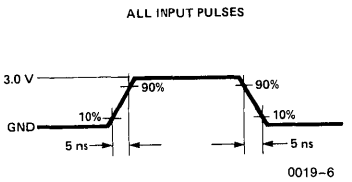
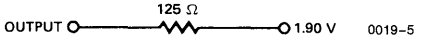


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[5]

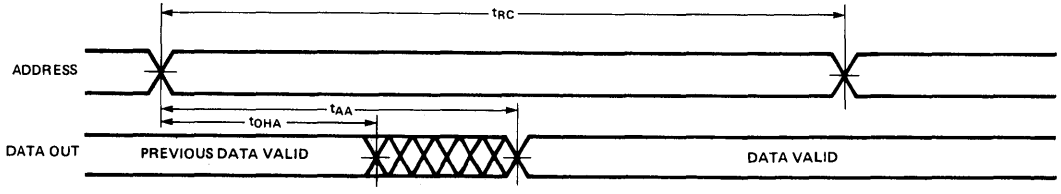
Parameters	Description	7C147-25		7C147-35		7C147-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACE}	$\overline{CS}$ Low to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$HIGH to High Z[6, 7]		20		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		20	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		35		45		ns
t_{AW}	Address Set-up to Write End	25		35		45		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		10		10		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		15		20		25	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 9, 10)



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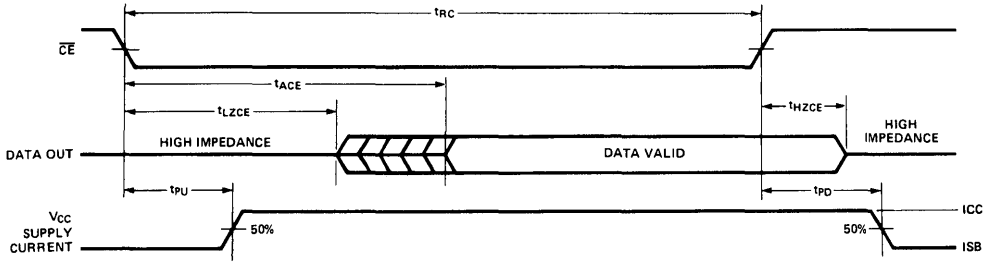
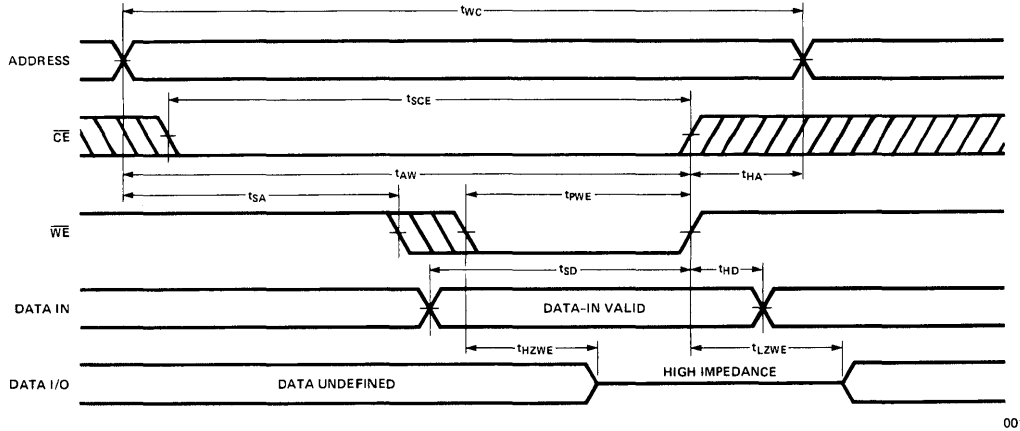
Switching Waveforms (Continued)

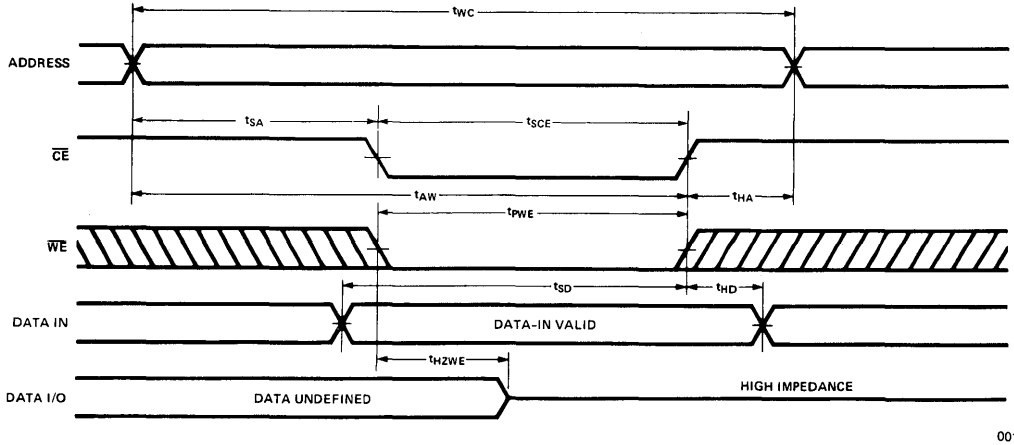
Read Cycle No. 2 (Notes 9, 11)



Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 8)



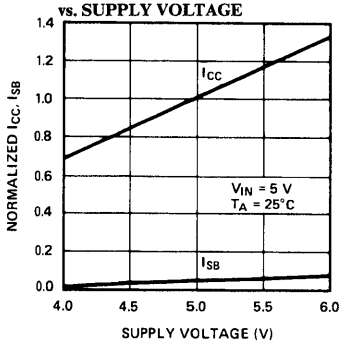
Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 8)



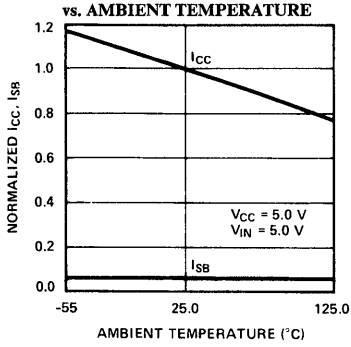
Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

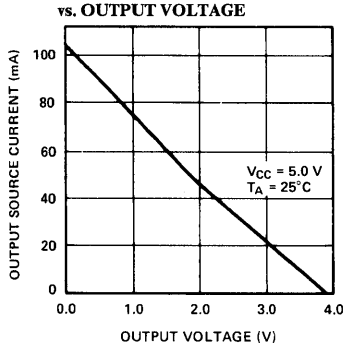
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



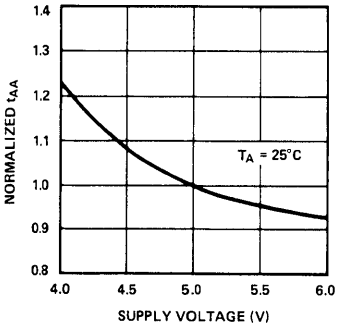
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



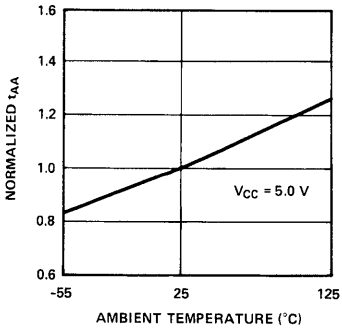
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



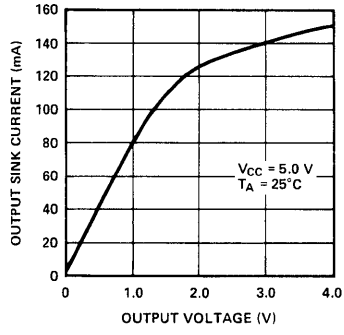
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



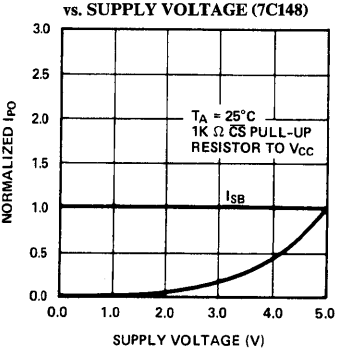
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



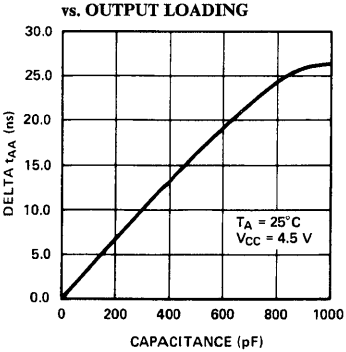
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



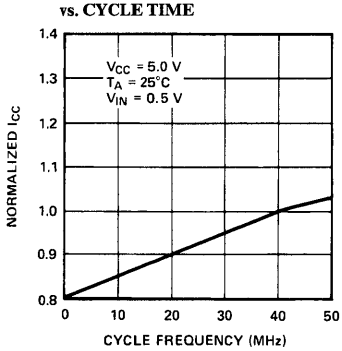
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



0019-11

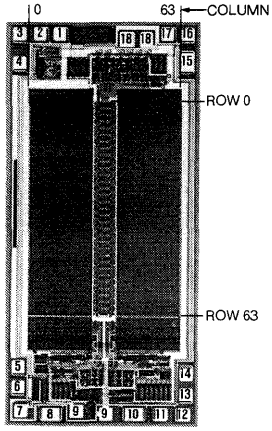
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C147-25PC	P3	Commercial
	CY7C147-25DC	D4	Commercial
	CY7C147-25LC	L50	Commercial
35	CY7C147-35PC	P3	Commercial
	CY7C147-35DC	D4	Commercial
	CY7C147-35LC	L50	Commercial
	CY7C147-35DMB	D4	Military
	CY7C147-35LMB	L50	Military
45	CY7C147-45PC	P3	Commercial
	CY7C147-45DC	D4	Commercial
	CY7C147-45LC	L50	Commercial
	CY7C147-45DMB	D4	Military
	CY7C147-45LMB	L50	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	1
A_1	X_1	2
A_2	X_2	3
A_3	X_3	4
A_4	Y_0	5
A_5	Y_1	6
A_6	X_4	17
A7	X_5	16
A_8	Y_2	15
A_9	Y_3	14
A_{10}	Y_4	13
A_{11}	Y_5	12

Bit Map



0019-12

CY7C148
CY7C149

CYPRESS SEMICONDUCTOR

1024 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25 ns access time**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power (7C148)**
  - **— 82.5 mW (25 ns version)**
  - **— 55 mW (all others)**
- **5 volt power supply ±10% tolerance both commercial and military**
- **TTL compatible inputs and outputs**

Functional Description

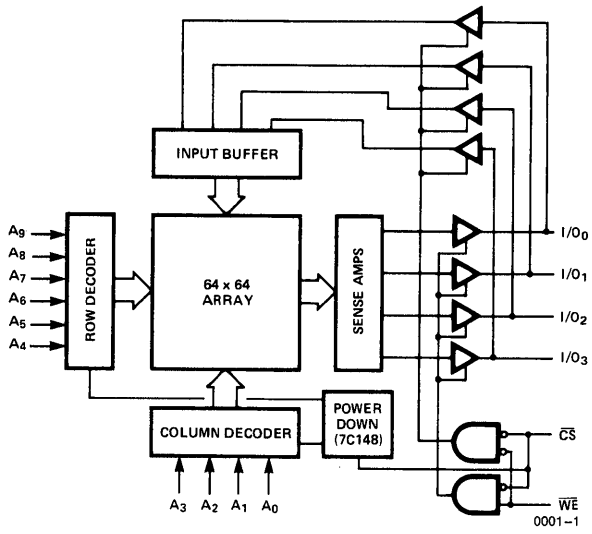
The CY7C148 and CY7C149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input, and three-state outputs. The CY7C148 and CY7C149 are identical except that the CY7C148 includes an automatic ($\overline{CS}$) power-down feature. The CY7C148 remains in a low power mode as long as the device remains unselected, i.e. ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

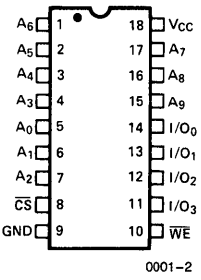
Reading the device is accomplished by selecting the device, ($\overline{CS}$) active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O_0 through I/O_3).

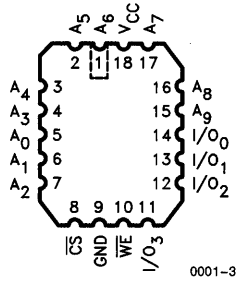
The input/output pins (I/O_0 through I/O_3) remain in a high impedance state unless the chip is selected, and write enable ($\overline{WE}$) is high.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C148-25	7C148-35	7C148-45	7C149-25	7C149-35	7C149-45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage (Per MIL-STD-883 Method 3015.2)..... >2001V

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[11]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C148/9-25 Min.	7C148/9-25 Max.	7C148/9-35, 45 Min.	7C148/9-35, 45 Max.	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8		8		mA
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz, T_A = 25°C, All Pins at 0V, V_{CC} = 5V			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS}$ ≤ V_{IL}, Output Open	Commercial		90		80	mA
			Military				110	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH} 7C148 only	Commercial		15		10	mA
			Military				10	
I_{PO}	Peak Power-On Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}[3] 7C148 only	Commercial		15		10	mA
			Military				10	
I_{OS}	Output Short Circuit Current	GND ≤ V_O ≤ V_{CC}[10]	Commercial		±275		±275	mA
			Military				±350	

Notes:

1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise current will exceed values given (CY7C148 only).
4. Chip deselected greater than 25 ns prior to selection.
5. Chip deselected less than 25 ns prior to selection.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in *Figure 1b*. These parameters are sampled and not 100% tested.
7. $\overline{WE}$ is high for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition low.
10. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
11. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

AC Test Loads and Waveforms

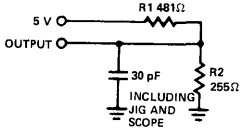
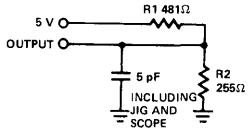


Figure 1a

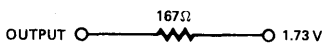


0001-4

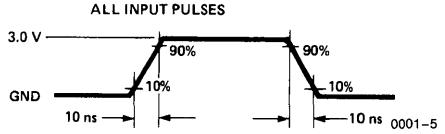
Figure 1b

Equivalent To:

THÉVENIN EQUIVALENT



0001-12



0001-5

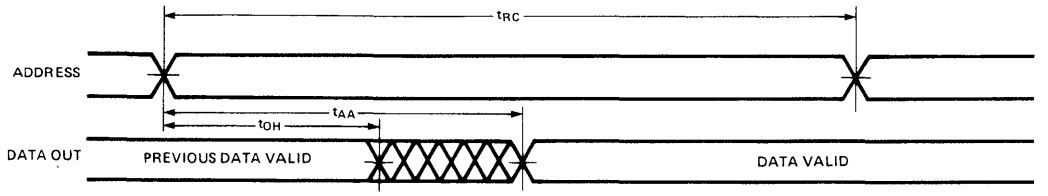
Figure 2

Switching Characteristics Over Operating Range (Note 1)

Parameters	Description		7C148/9-25		7C148/9-35		7C148/9-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1}	Chip Select Low to Data Out Valid (CY7C148 only)			25[4]		35		45	ns
t_{ACS2}				30[5]		35		45	
t_{ACS}	Chip Select Low to Data Out Valid (CY7C149 only)			15		15		20	ns
t_{LZ}[6]	Chip Select Low to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[6]	Chip Select High to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select High to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select Low to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[2]	Write Enable Low to Write Enable High		20		30		35		ns
t_{WR}	Write Enable High to Address		5		5		5		ns
t_{WZ}[6]	Write Enable to Output in High Z		0	8	0	10	0	15	ns
t_{DW}	Data in Valid to Write Enable High		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable Low		0		0		0		ns
t_{CS}[2]	Chip Select Low to Write Enable High		20		30		40		ns
t_{OW}[6]	Write Enable High to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

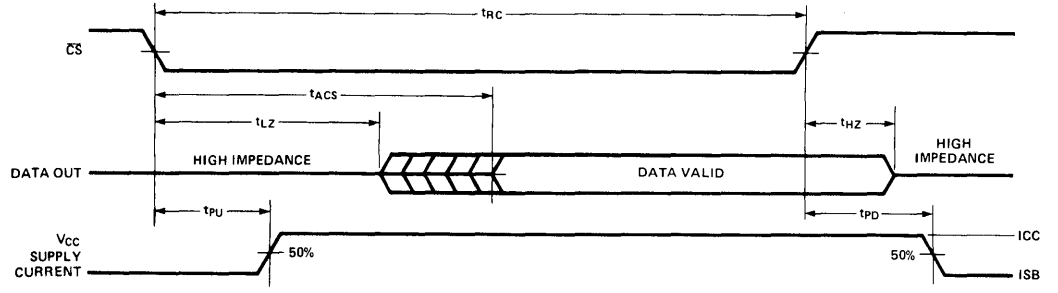
Switching Waveforms

Read Cycle No. 1 (Notes 7, 8)

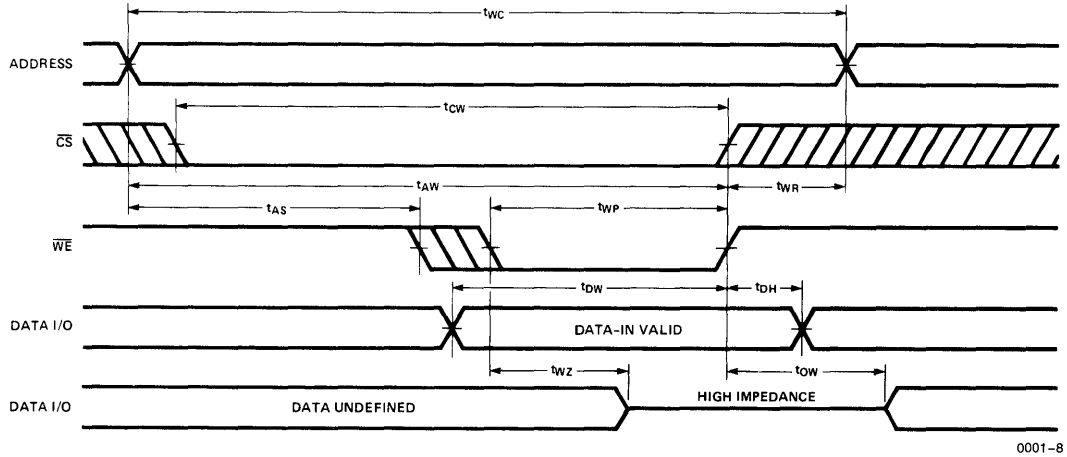


Switching Waveforms (Continued)

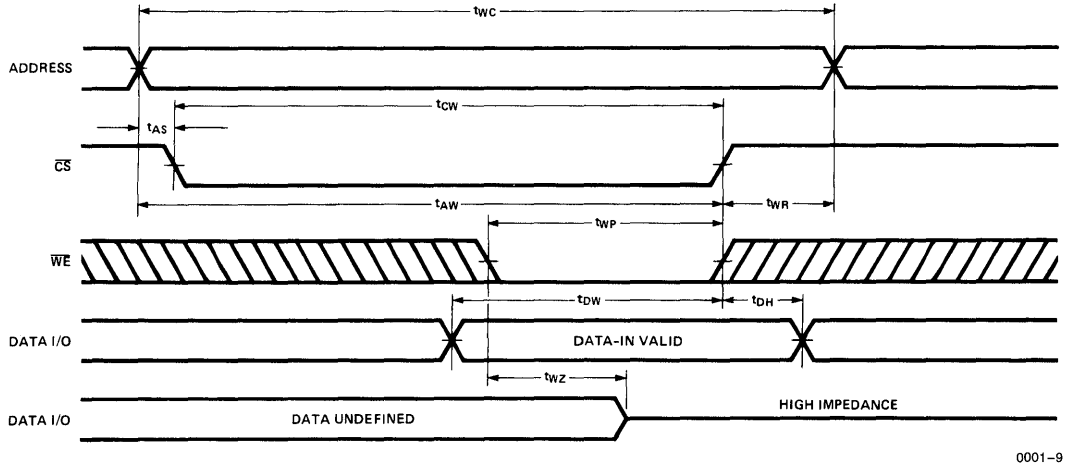
Read Cycle No. 2 (Notes 7, 9)



Write Cycle No. 1 ($\overline{WE}$ Controlled)



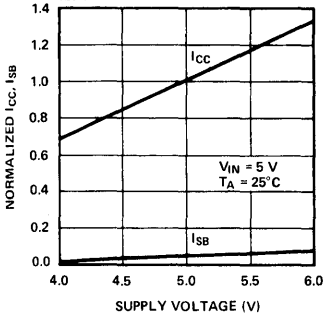
Write Cycle No. 2 ($\overline{CS}$ Controlled)



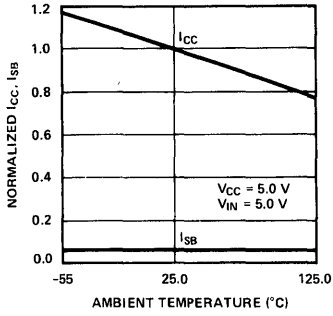
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

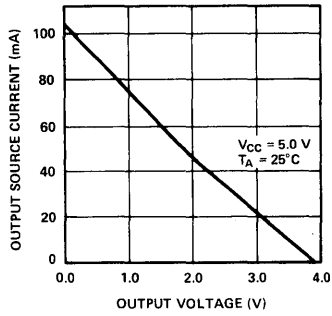
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



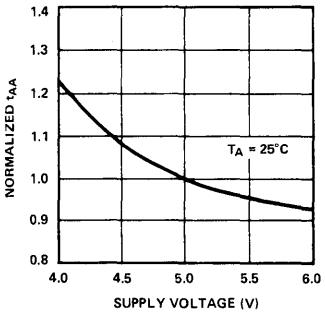
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



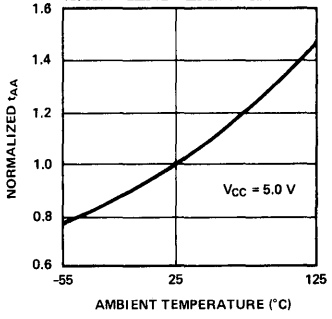
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



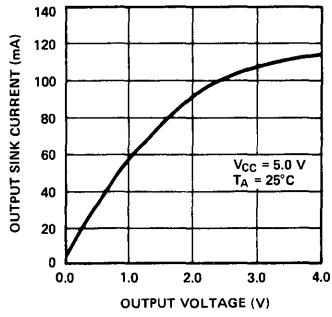
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



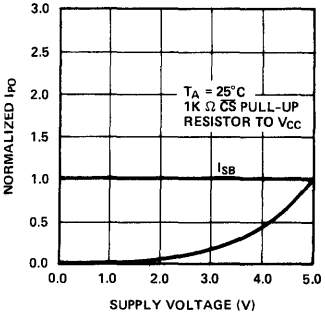
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



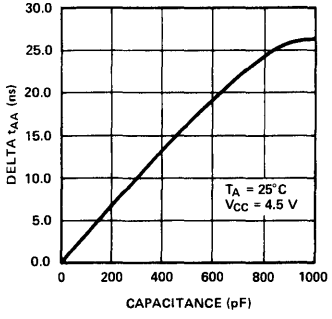
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



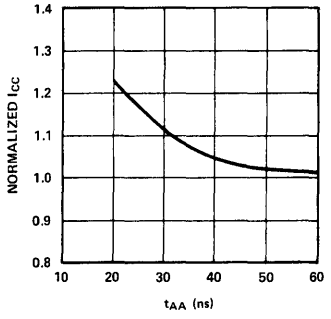
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. ACCESS TIME



0001-10

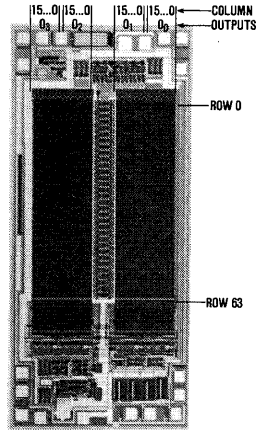
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C148-25PC CY7C149-25PC	P3	Commercial
	CY7C148-25DC CY7C149-25DC	D4	
	CY7C148-25LC CY7C149-25LC	L50	
35	CY7C148-35PC CY7C149-35PC	P3	Commercial
	CY7C148-35DC CY7C149-35DC	D4	
	CY7C148-35LC CY7C149-35LC	L50	
	CY7C148-35DMB CY7C149-35DMB	D4	Military
	CY7C148-35LMB CY7C149-35LMB	L50	
45	CY7C148-45PC CY7C149-45PC	P3	Commercial
	CY7C148-45DC CY7C149-45DC	D4	
	CY7C148-45LC CY7C149-45LC	L50	
	CY7C148-45DMB CY7C149-45DMB	D4	Military
	CY7C148-45LMB CY7C149-45LMB	L50	

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_0	5
A_1	Y_1	6
A_2	Y_2	7
A_3	Y_3	4
A_4	X_0	3
A_5	X_3	2
A_6	X_2	1
A_7	X_5	17
A_8	X_4	16
A_9	X_1	15

Bit Map



0001-11

CYPRESS SEMICONDUCTOR

PRELIMINARY **CY7C150**

1024 x 4 Static R/W RAM

Features

- **1024 x 4 static RAM for control in high speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Separate inputs and outputs**
- **Memory reset function**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2000V static discharge**
- **TTL compatible inputs and outputs**

Functional Description

The CY7C150 is a high performance CMOS static RAM organized as 1024 words x 4 bits. Easy memory expansion is provided by active LOW chip select ($\overline{CS}$) and output enable, ($\overline{OE}$) inputs and three-state outputs.

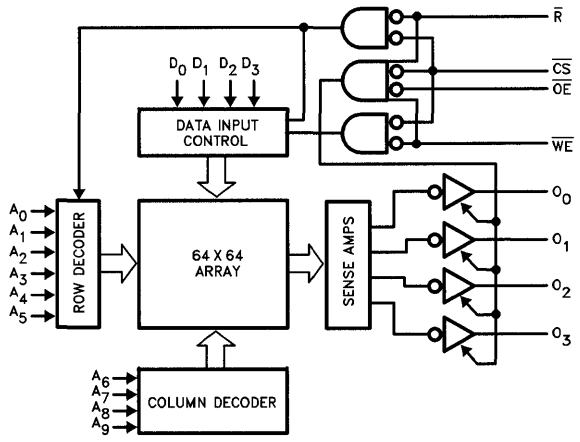
An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are LOW, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete.

Reading is performed with the chip select ($\overline{CS}$) input LOW, and the write enable ($\overline{WE}$) input HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

The outputs of the memory go to an active high impedance state whenever chip select ($\overline{CS}$) is HIGH, output enable ($\overline{OE}$) is HIGH, or during the writing operation when WRITE ENABLE ($\overline{WE}$) is LOW.

The entire memory can be reset to a logical LOW by taking $\overline{RESET}$ (R) LOW when chip select ($\overline{CS}$) is LOW and WRITE ENABLE is HIGH.

Logic Block Diagram



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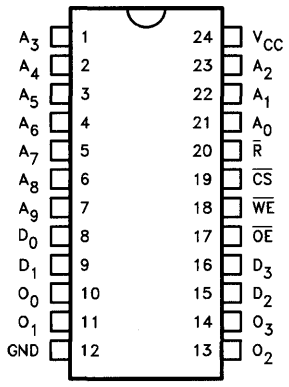
Pin Configuration



0028-2

Selection Guide

		7C150-25	7C150-35
Maximum Access Time (ns)	Commercial	25	35
	Military		35
Maximum Operating Current (mA)	Commercial	120	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C150-25		7C150-35		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4		0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Volage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	−50	+50	μA
I_{OS}	Output Short[2]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		120		90	mA
			Military				120	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

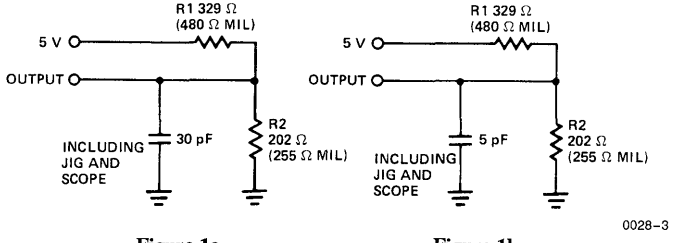


Figure 1a

Figure 1b

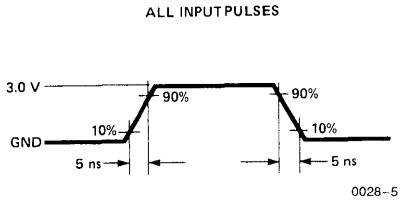
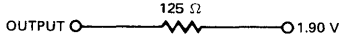


Figure 2

Equivalent To:

THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range

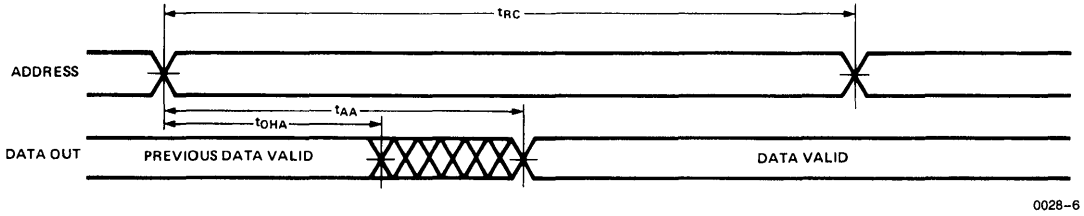
Parameters	Description	7C150-25		7C150-35		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]	0	20	0	25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5,6]	0	20	0	25	ns
WRITE CYCLE[7]						
t_{WC}	Write Cycle Time	25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		20		ns
t_{AW}	Address Set-up to Write End	20		30		ns
t_{HA}	Address Hold from Write End	5		5		ns
t_{SA}	Address Set-up to Write Start	5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-up to Write End	15		20		ns
t_{HD}	Data Hold from Write End	5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5,6]	0	20	0	25	ns
RESET CYCLE						
t_{RRC}	Reset Cycle Time	50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		ns
t_{PR}	Reset Pulse Width	20		30		ns
t_{HCSR}	Chip Select Hold after End of Reset	0		0		ns
t_{HWER}	Write Enable Hold after End of Reset	30		40		ns
t_{HAR}	Address Hold after End of Reset	30		40		ns
t_{LZR}	Reset HIGH to Output in Low Z[6]	0		0		ns
t_{HZR}	Reset LOW to Output in High Z[5,6]	0	20	0	25	ns

Notes:

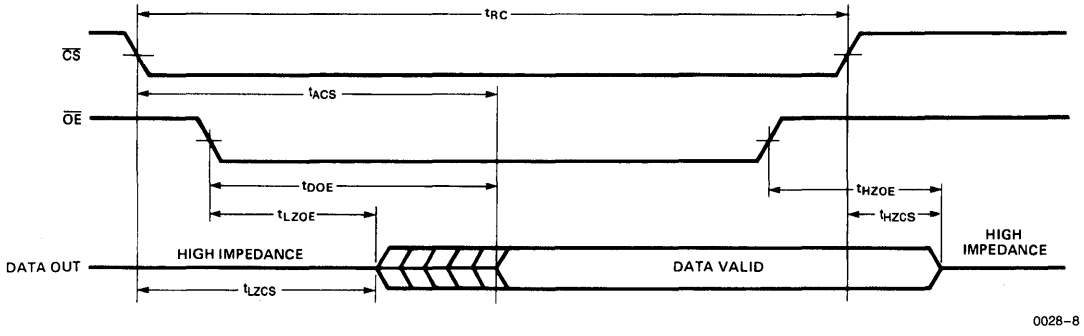
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCS}, t_{HZOE}, t_{HZR} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CS}$ and $\overline{OE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.

Switching Waveforms

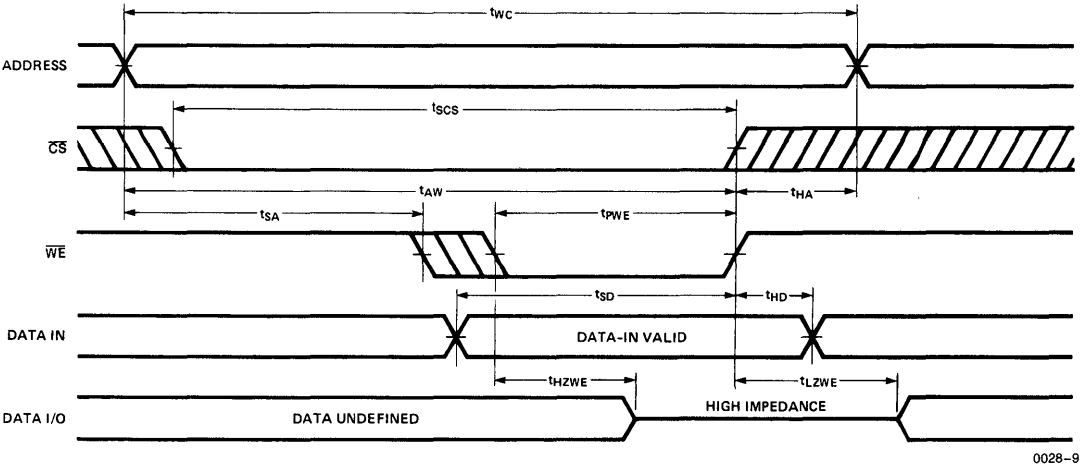
Read Cycle No. 1 (Notes 8, 9)



Read Cycle No. 2 (Notes 8, 10)



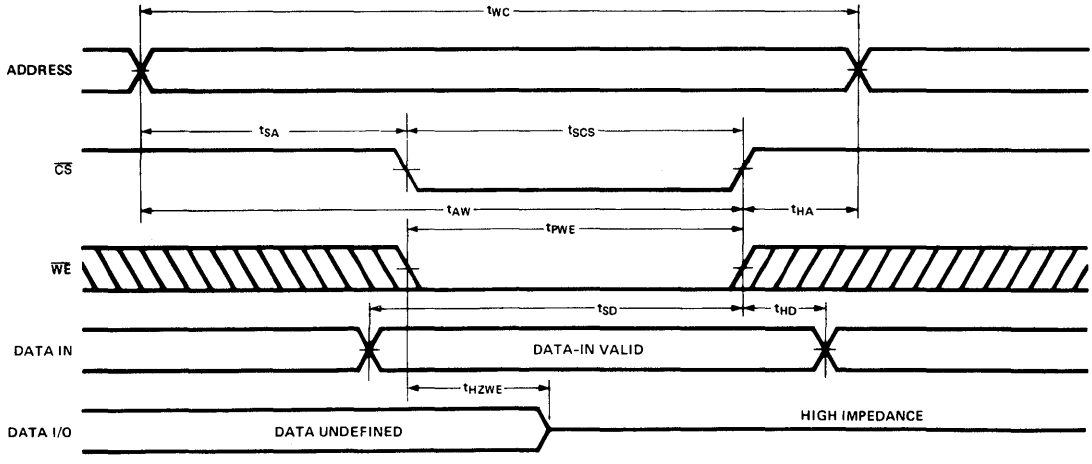
Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)



2

Switching Waveforms (Continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled) (Note 7)



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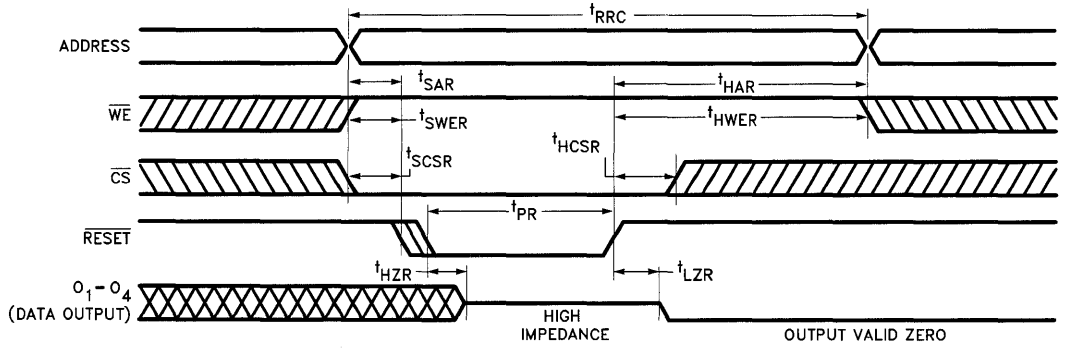
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Reset Cycle



0028–11

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C150-25PC	P13	Commercial
	CY7C150-25DC	D14	Commercial
35	CY7C150-35PC	P13	Commercial
	CY7C150-35DC	D14	Commercial
	CY7C150-35DMB	D14	Military

CYPRESS SEMICONDUCTOR

CY7C167

16,384 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed—25 ns**
- **Low active power**
  - **— 275 mW (commercial)**
  - **— 275 mW (military)**
- **Low standby power**
  - **— 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

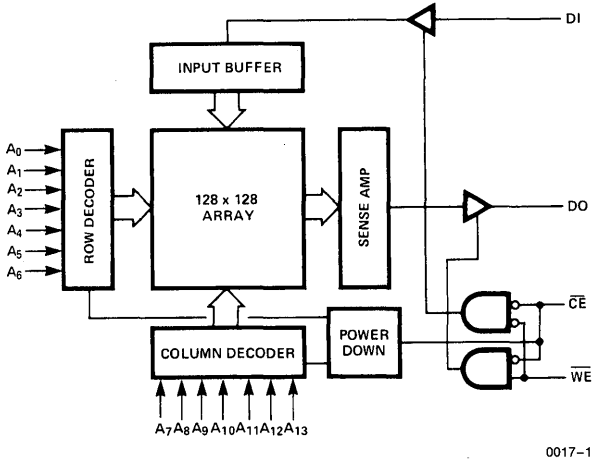
The CY7C167 is a high performance CMOS static RAM organized as 16,384 x 1 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

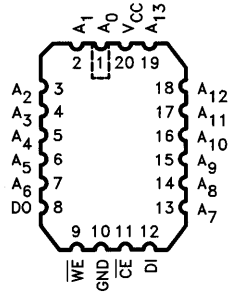
The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram

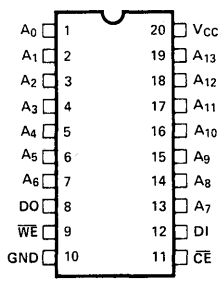


0017-1

Pin Configurations



0017-2



0017-3

Selection Guide

		7C167-25	7C167-35	7C167-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	70	70	50
	Military		70	50
Maximum Standby Current (mA)	Commercial	20	20	15
	Military		20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C167-25, 35		7C167-45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4		0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	−50	+50	μA
I_{OS}	Output Short[2] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70		50	mA
			Military*		70		50	
I_{SB}	Automatic $\overline{CE}$[3] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		20		15	mA
			Military*		20		20	

* −35 and −45 only

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		6	
C_{CE}	Chip Enable Capacitance		5	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested on a sample basis.

AC Test Loads and Waveforms

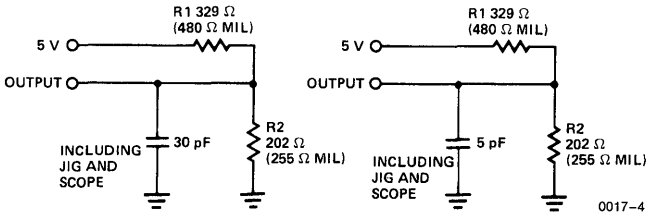


Figure 1a

Figure 1b

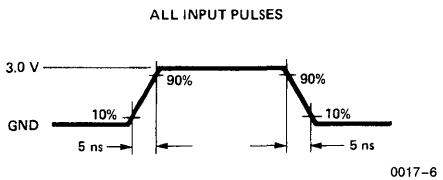
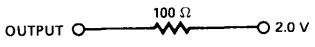


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[5]

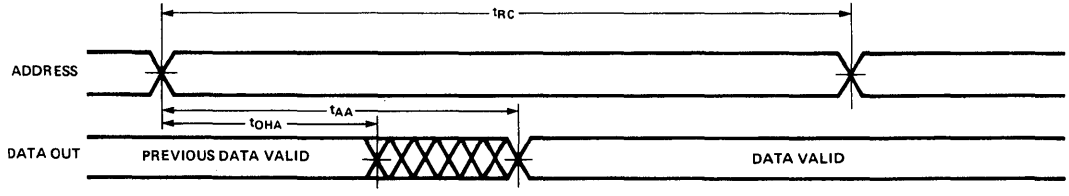
Parameters	Description	7C167-25		7C167-35		7C167-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time (Commercial)	25		30		40		ns
t_{RC}	Read Cycle Time (Military)			35		40		ns
t_{AA}	Address to Data Valid (Commercial)		25		30		40	ns
t_{AA}	Address to Data Valid (Military)				35		40	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		25		30	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		40		ns
t_{AW}	Address Set-up to Write End	25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	15		20		20		ns
t_{SD}	Data Set-up to Write End	15		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	0	15	0	20	0	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	0	15	0	20	0	25	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 9, 10)



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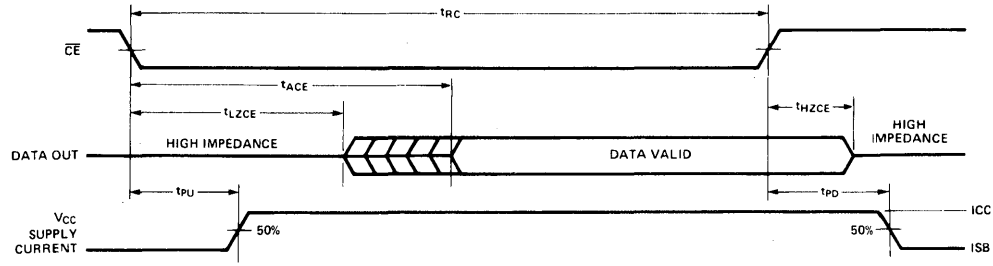
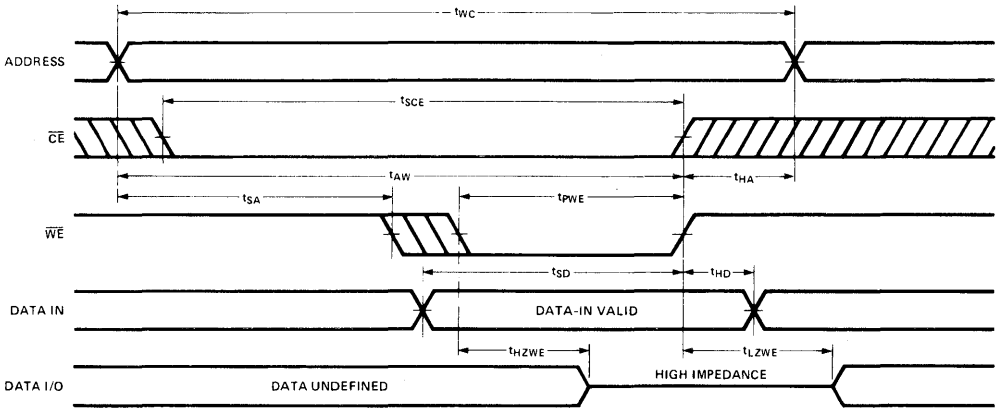
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 9, 11)



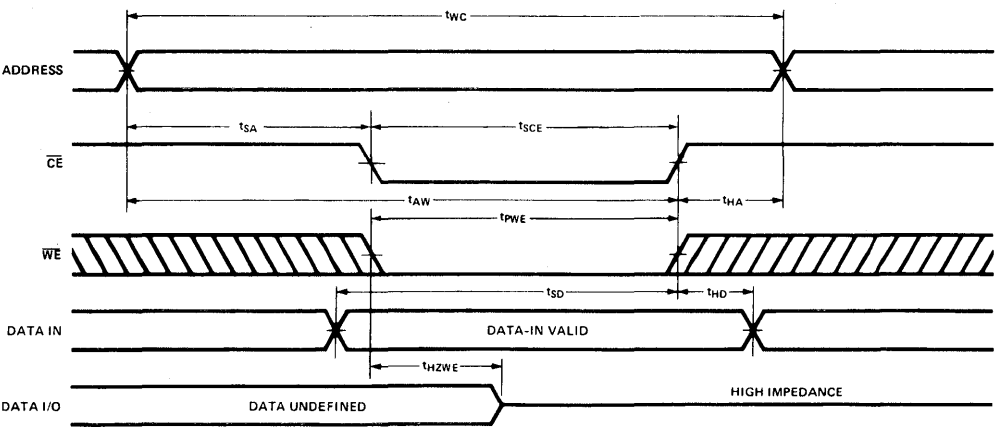
0017-8

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 8)



0017-9

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 8)

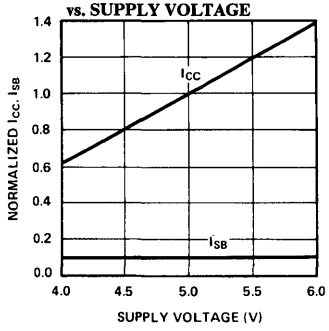


0017-10

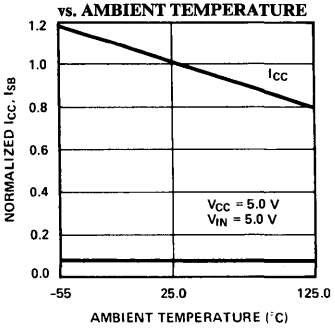
Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

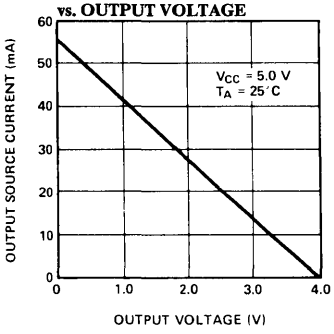
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



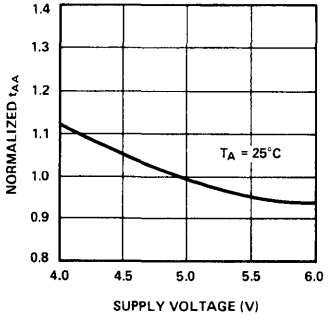
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



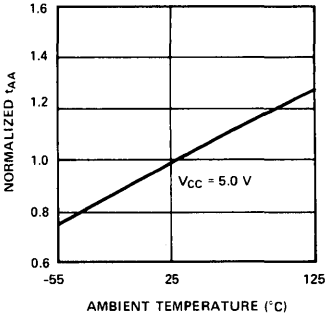
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



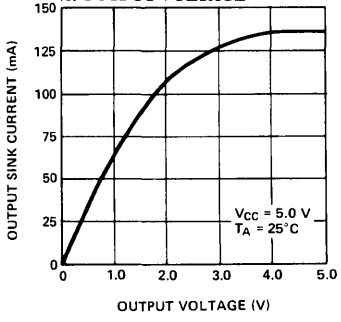
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



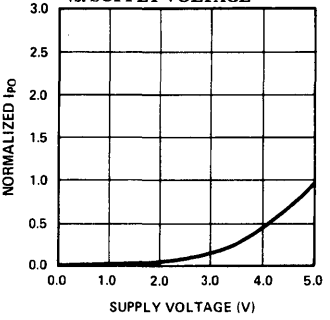
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



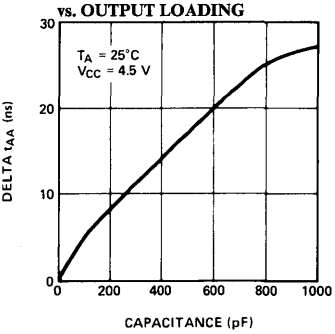
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



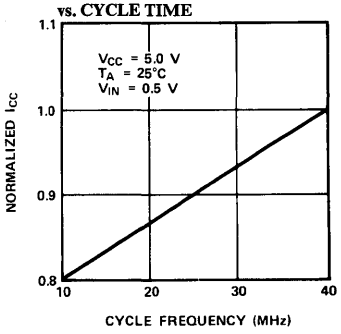
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



0017–11

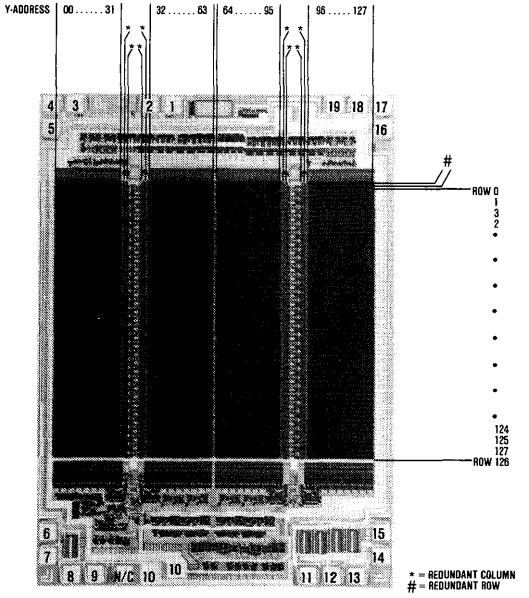
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C167-25PC	P5	Commercial
	CY7C167-25DC	D6	
	CY7C167-25LC	L51	
35	CY7C167-35PC	P5	Commercial
	CY7C167-35DC	D6	
	CY7C167-35LC	L51	
	CY7C167-35DMB	D6	Military
	CY7C167-35LMB	L51	
45	CY7C167-45PC	P5	Commercial
	CY7C167-45DC	D6	
	CY7C167-45LC	L51	
	CY7C167-45DMB	D6	Military
	CY7C167-45LMB	L51	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	16
A_1	X_3	17
A_2	X_4	18
A_3	X_1	19
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8
A_{12}	Y_5	14
A_{13}	Y_6	15

Bit Map



0017-12

CY7C168
CY7C169

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected (7C168)**
- **CMOS for optimum speed/power**
- **High Speed**
  - **— 25 ns t_{AA}**
  - **— 15 ns t_{ACE} (7C169)**
- **Low active power**
  - **— 385 mW (commercial)**
  - **— 385 mW (military)**
- **Low standby power (7C168)**
  - **— 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

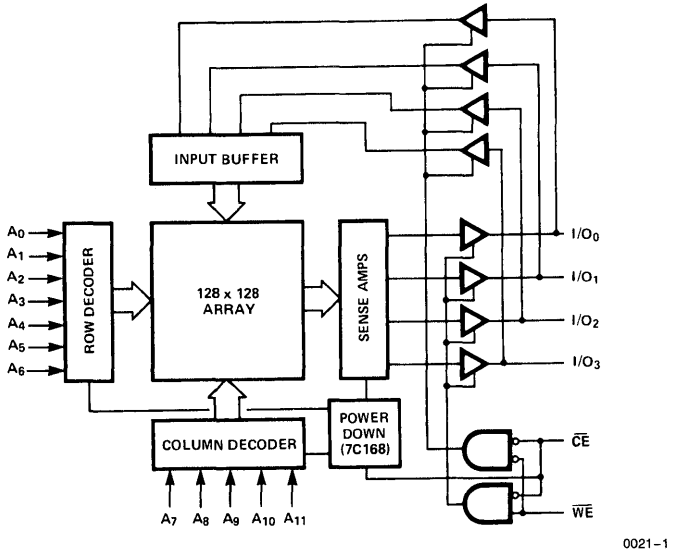
The CY7C168 and CY7C169 are high performance CMOS static RAMs organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 85% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

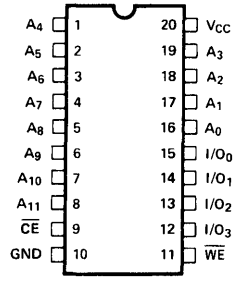
The I/O pins stay in high impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram

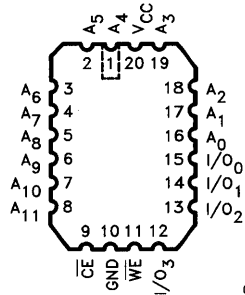


0021-1

Pin Configurations



0021-2



0021-3

Selection Guide

		7C168-25	7C168-35	7C168-45	7C169-25	7C169-35	7C169-40
Maximum Access Time (ns)		25	35	45	25	35	40
Maximum Operating Current (mA)	Commercial	90	90	70	90	90	70
	Military		90	70		90	70
Maximum Standby Current (mA)	Commercial	20	20	15			
	Military		20	20			

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C168-25, -35 7C169-25, -35		7C168-45 7C169-40		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	−10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	−50	−50	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90		70	mA
			Military*		90		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, CE ≥ V_{IH}	Commercial		20		15	mA
			Military*		20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, CE ≥ V_{CC} − 0.3V	Commercial		11		11	mA
			Military*		20		20	

*−35 and −45 only

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

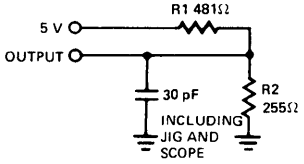


Figure 1a

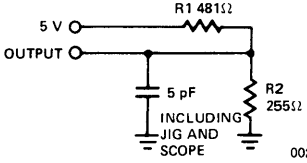


Figure 1b

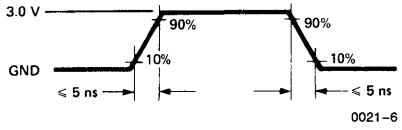
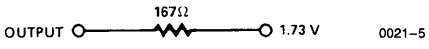


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

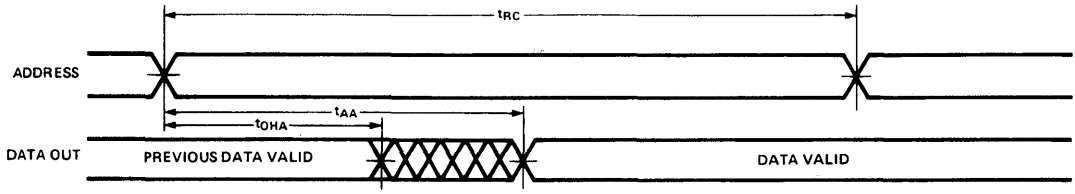
Parameters	Description		7C168-25 7C169-25		7C168-35 7C169-35		7C169-40		7C168-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
t_{RC}	Read Cycle Time		25		35		40		45		ns
t_{AA}	Address to Data Valid			25		35		40		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	7C168		25		35				45	ns
		7C169		15		25		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]			15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)		0		0				0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down (7C168)			25		25				30	ns
t_{RCS}	Read Command Set-up		0		0		0		0		ns
t_{RCH}	Read Command Hold		0		0		0		0		ns
WRITE CYCLE[7]											
t_{WC}	Write Cycle Time		25		35		40		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		35		30		35		ns
t_{AW}	Address Set-up to Write End		20		30		40		35		ns
t_{HA}	Address Hold from Write End		0		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		20		30		35		35		ns
t_{SD}	Data Set-up to Write End		10		15		15		15		ns
t_{HD}	Data Hold from Write End		0		0		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]		6		6		6		6		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]			10		15		20		20	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 8, 9)



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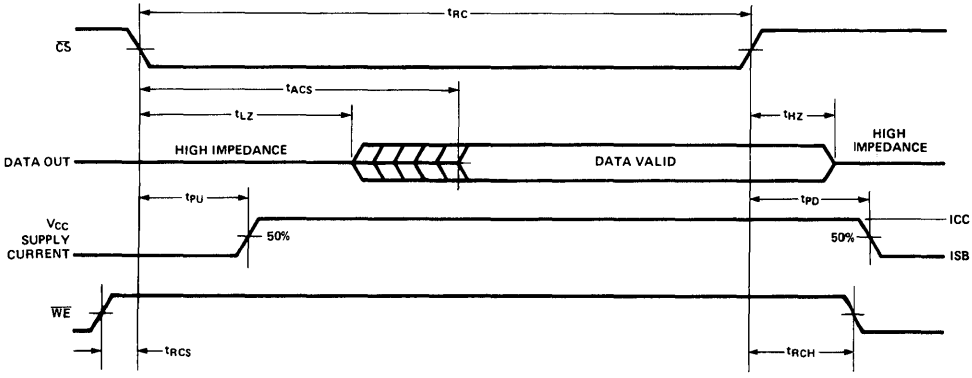
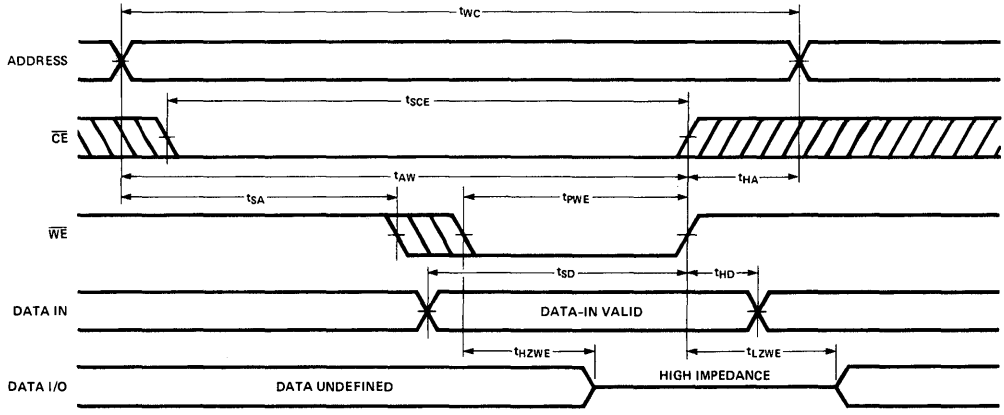
Switching Waveforms (Continued)

Read Cycle (Notes 8, 10)



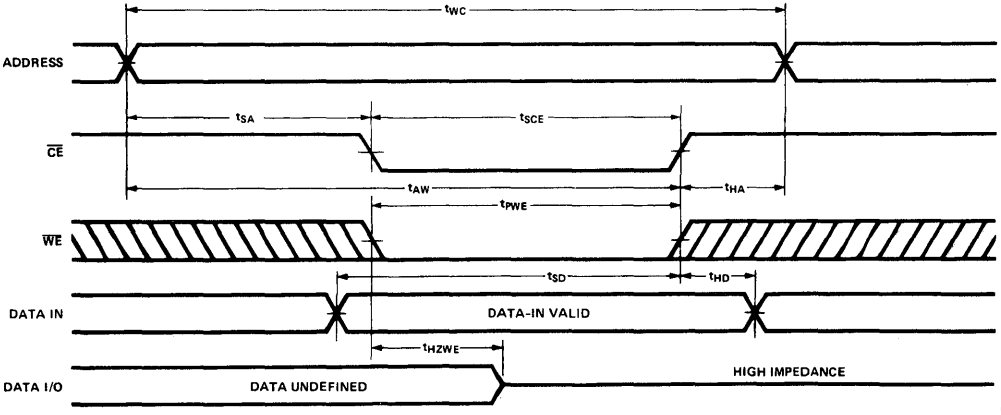
0021-8

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)



0021-9

Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 7)

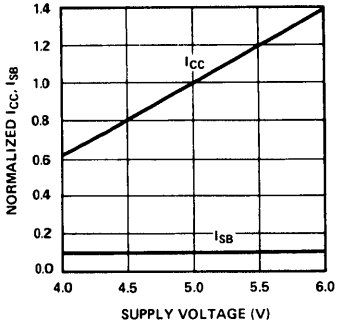


0021-10

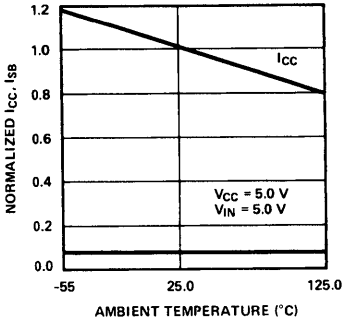
Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

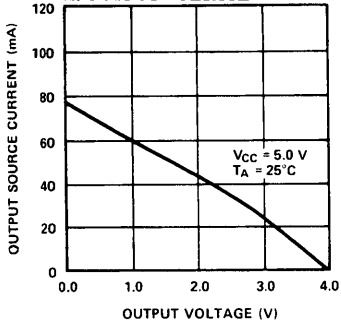
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



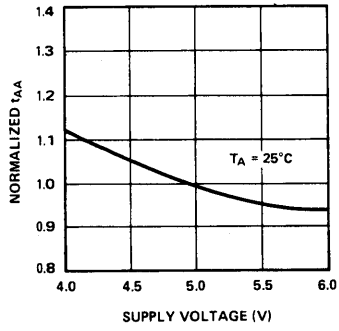
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



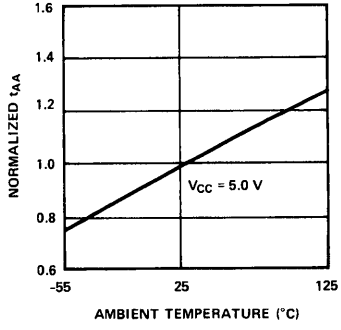
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



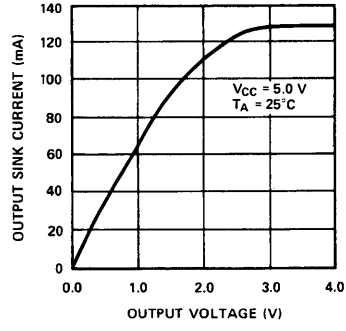
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



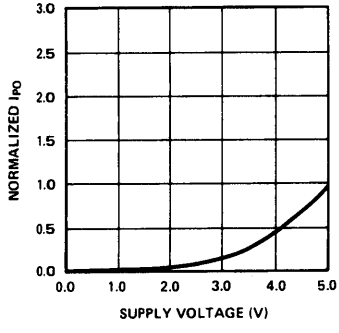
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



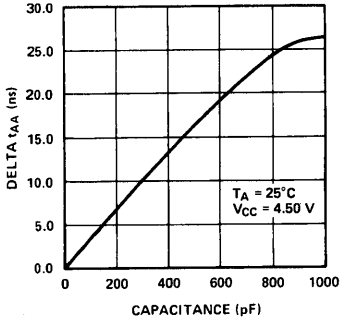
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



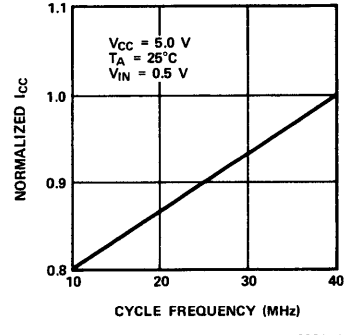
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



0021-11

Ordering Information

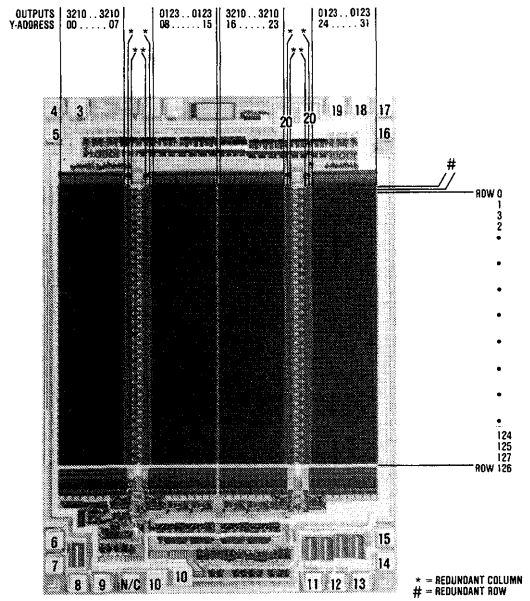
Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C168-25PC	P5	Commercial
	CY7C168-25DC	D6	
	CY7C168-25LC	L51	
35	CY7C168-35PC	P5	Commercial
	CY7C168-35DC	D6	
	CY7C168-35LC	L51	
	CY7C168-35DMB	D6	Military
	CY7C168-35LMB	L51	
45	CY7C168-45PC	P5	Commercial
	CY7C168-45DC	D6	
	CY7C168-45LC	L51	
	CY7C168-45DMB	D6	Military
	CY7C168-45LMB	L51	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C169-25PC	P5	Commercial
	CY7C169-25DC	D6	
	CY7C169-25LC	L51	
35	CY7C169-35PC	P5	Commercial
	CY7C169-35DC	D6	
	CY7C169-35LC	L51	
	CY7C169-35DMB	D6	Military
	CY7C169-35LMB	L51	
40	CY7C169-40PC	P5	Commercial
	CY7C169-40DC	D6	
	CY7C169-40LC	L51	
	CY7C169-40DMB	D6	Military
	CY7C169-40LMB	L51	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	16
A_1	X_3	17
A_2	X_4	18
A_3	X_1	19
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

Bit Map



0021-12

CYPRESS SEMICONDUCTOR

CY7C170

4096 x 4 Static R/W RAM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns t_{AA}**
  - **— 25 ns t_{ACE}**
- **Low active power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**
- **Output enable**

Functional Description

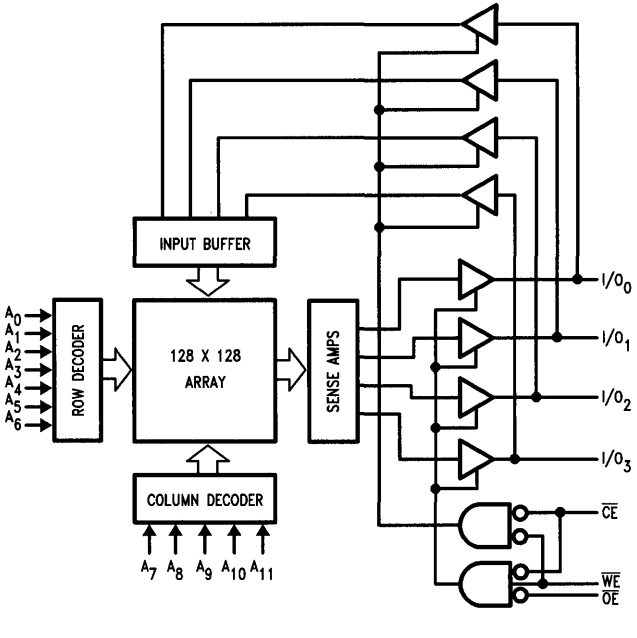
The CY7C170 is a high performance CMOS static RAM organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$), and three-state drivers.

Writing to the device is accomplished when the chip enable ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

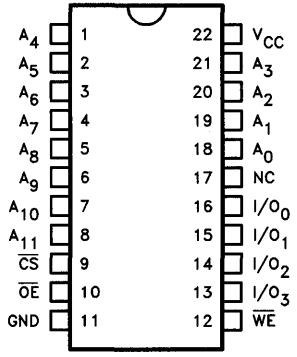
The I/O pins stay in high impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



0037-1

Pin Configuration



0037-2

Selection Guide

		7C170-35	7C170-45
Maximum Access Time (ns)		35	45
Maximum Operating Current (mA)	Commercial	90	90
	Military	120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) .....20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C170 Min.	7C170 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	+50	μA
I_{OS}	Output Short[2] Circuit Current	V_{CC} = Max., V_{OUT} = GND			−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90	mA
			Military		120	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

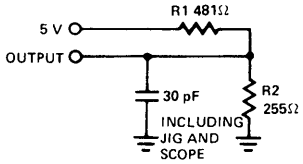
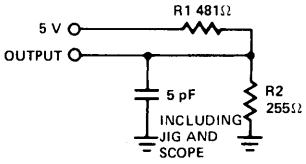


Figure 1a



0037-4

Figure 1b

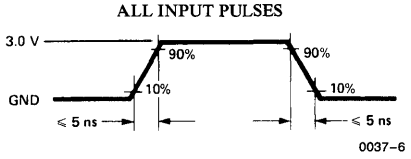
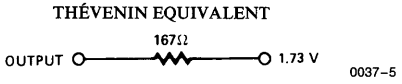


Figure 2

Equivalent to:



0037-5

Switching Characteristics Over Operating Range[4]

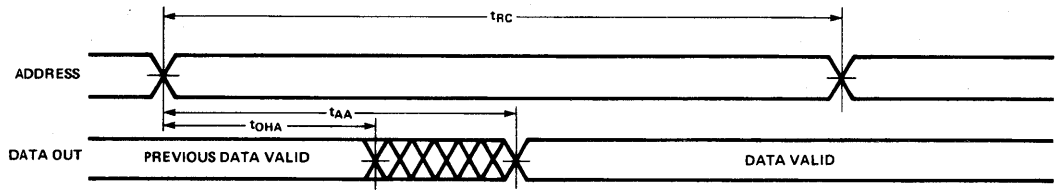
Parameters	Description	7C170-35		7C170-45		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35		45		ns
t_{AA}	Address to Data Valid		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACS}	$\overline{CS}$ Low to Data Valid		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		ns
t_{HZCS}	$\overline{CE}$ HIGH to High Z[5, 6]		20		25	ns
WRITE CYCLE[7]						
t_{WC}	Write Cycle Time	35		40		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	35		35		ns
t_{AW}	Address Set-up to Write End	30		35		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	30		35		ns
t_{SD}	Data Set-up to Write End	15		15		ns
t_{HD}	Data Hold from Write End	0		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	6		6		ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZOE}, t_{HZCS} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

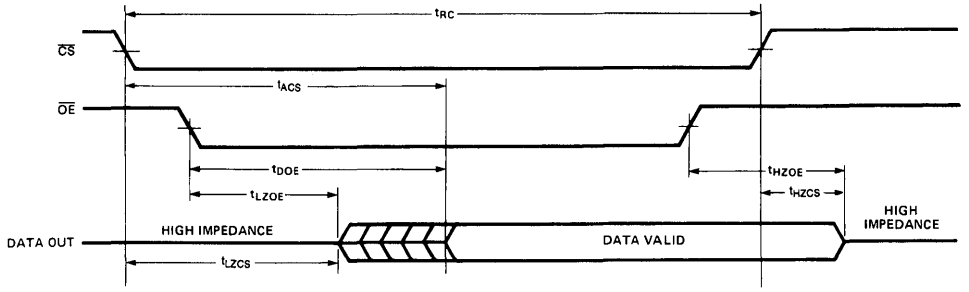
Read Cycle No. 1 (Notes 8, 9)



0037-11

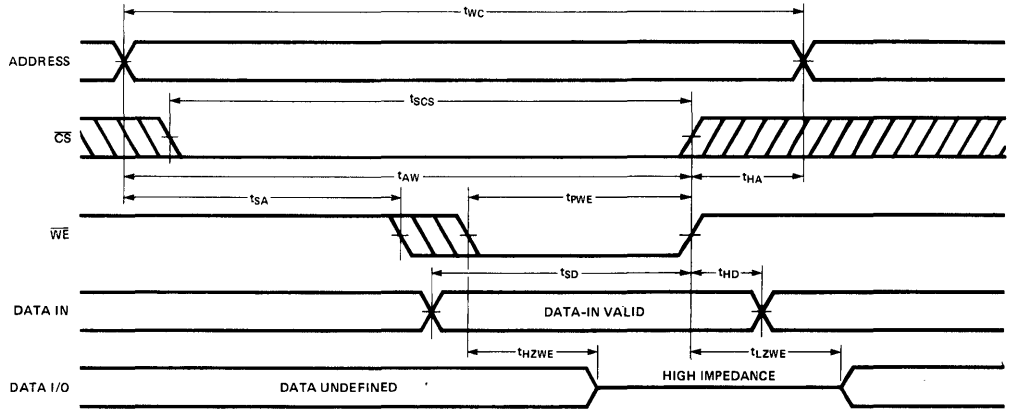
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 8, 10)



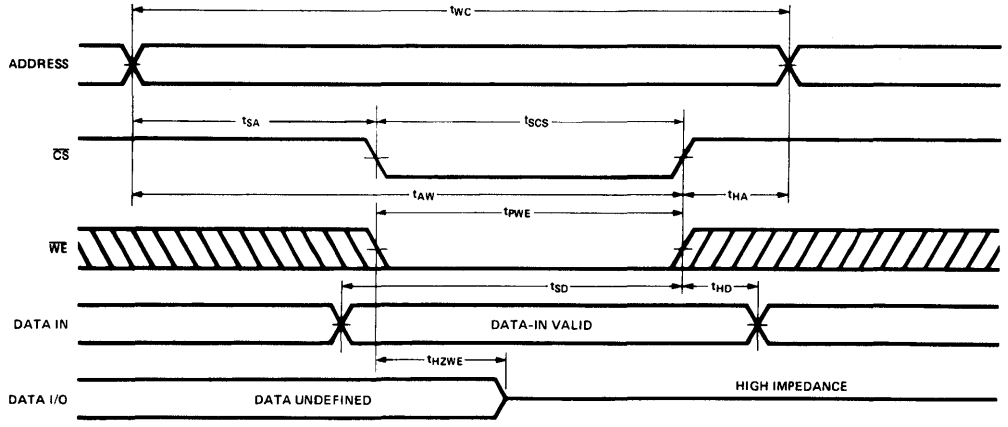
0037-7

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)



0037-8

Write Cycle No. 2 ($\overline{CS}$ Controlled) (Note 7)



0037-9

Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

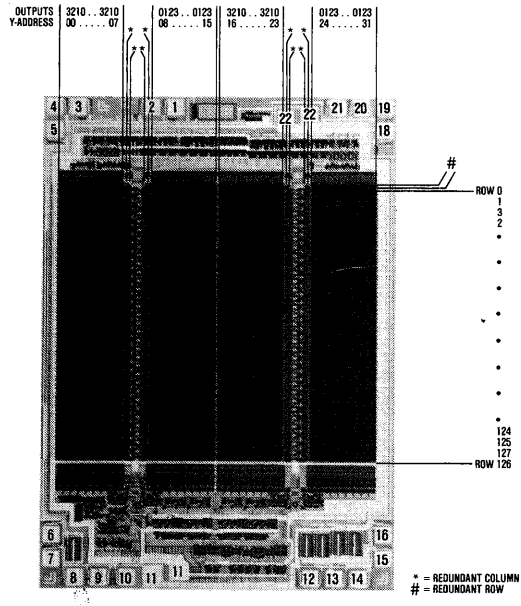
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C170-35PC	P9	Commercial
	CY7C170-35 DC	D10	
	CY7C170-35 DMB	D10	Military
45	CY7C170-45PC	P9	Commercial
	CY7C170-45 DC	D10	
	CY7C170-45DMB	D10	Military

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	18
A_1	X_3	19
A_2	X_4	20
A_3	X_1	21
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

Bit Map



0037-10

CYPRESS SEMICONDUCTOR

65,536 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/ power**
- **High speed — 25 ns**
- **Low active power**
  — 633 mW (commercial)
  — 688 mW (military)
- **Low standby power**
  — 110 mW
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

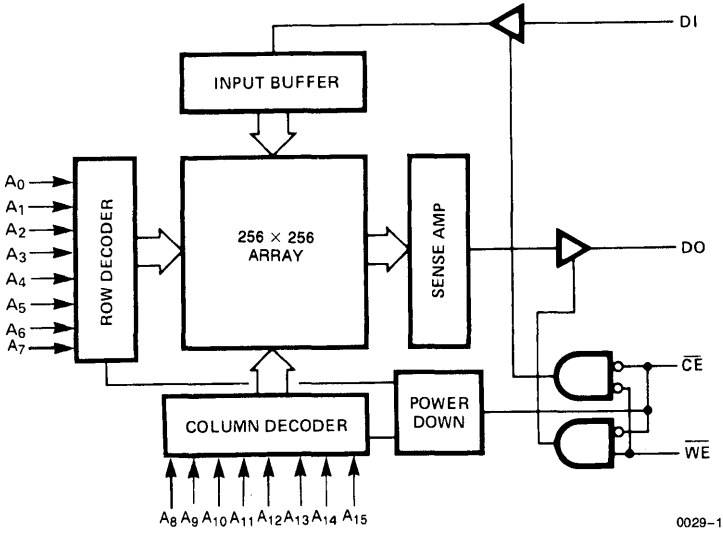
The CY7C187 is a high performance CMOS static RAM organized as 65,536 x 1 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 85% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

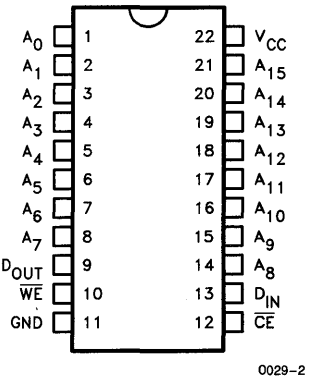
Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configuration



Selection Guide

			7C187-35	7C187-45
Maximum Access Time (ns)	Commercial		35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial		115	115
	Military		125	125
Maximum Standby Current (mA)	Commercial		20	20
	Military		30	30

CY7C189
CY7C190

CYPRESS SEMICONDUCTOR

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high speed CMOS RAMs**
- **Inverting outputs CY7C189**
- **Non-inverting outputs CY7C190**
- **High speed**
  - **— 18 ns and 25 ns commercial**
  - **— 25 ns military**
- **Low power**
  - **— 303 mW at 25 ns**
  - **— 495 mW at 18 ns**
- **Power supply 5V ±10%**
- **Advanced high speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2000V static discharge**
- **Three-state outputs**
- **TTL compatible interface levels**

Functional Description

The CY7C189 and CY7C190 are extremely high peformance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting (CY7C189) and non-inverting (CY7C190) outputs.

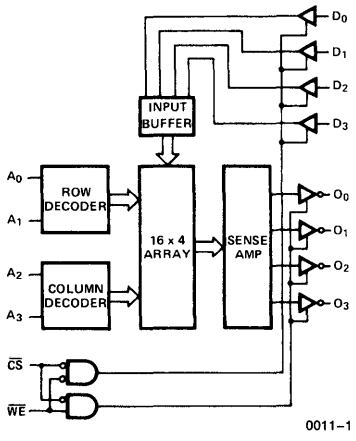
An active LOW write enable ($\overline{WE}$) signal controls the writing and reading of the memory. When the write enable ($\overline{WE}$) and chip select ($\overline{CS}$) are both LOW the information on the four data inputs (D_0–D_3) is written into the location addressed by the information on the address lines (A_0–A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0–O_3) when the write cycle is complete. This precondition operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is accomplished with an active LOW on the chip select line ($\overline{CS}$) and a HIGH on the write enable ($\overline{WE}$) line. The information stored is read out from the addressed location and presented at the outputs in inverted (CY7C189) or non-inverted (CY7C190) format.

During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

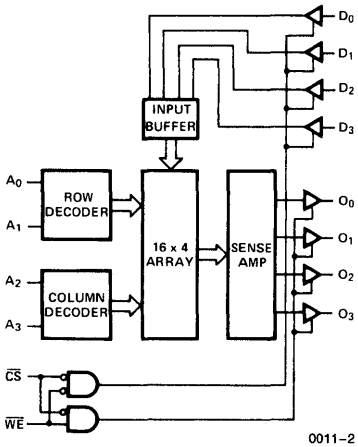
Logic Block Diagrams

CY7C189



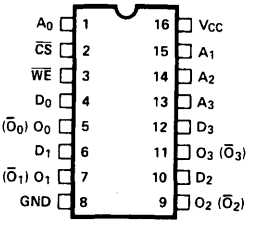
0011-1

CY7C190



0011-2

Pin Configuration



0011-3

(7C189)
7C190

Selection Guide

		7C189-18 7C190-18	7C189-25 7C190-25
Maximum Access Time (ns)	Commercial	18	25
	Military		25
Maximum Operating Current (mA)	Commercial	90	55
	Military		70

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potenial (Pin 16 to Pin 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C189-15 7C190-15		7C189-25 7C190-25		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45		0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage[2]							
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		55	mA
			Military				70	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. The CMOS process does not provide a clamp diode. However the CY7C189 and CY7C190 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 5 ns (measured at 50% points).
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recover glitch).
5. Tested on a sample basis.

2

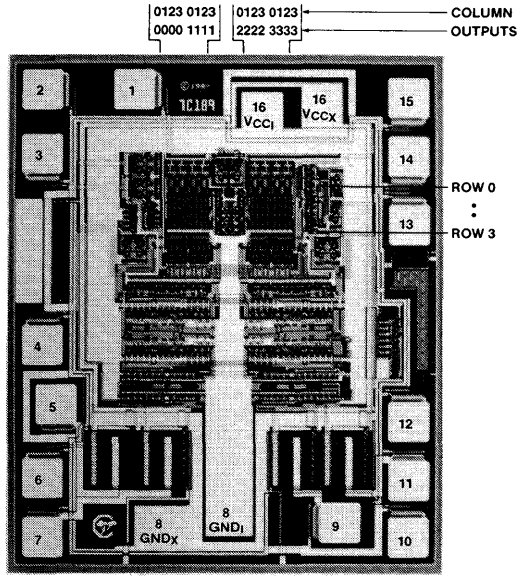
Switching Characteristics Over the Operating Range[6]

Parameter	Description	Test Conditions	7C189-15 7C190-15		7C189-25 7C190-25		Units
			Min.	Max.	Min.	Max.	
READ CYCLE							
t_{RC}	Ready Cycle Time		18		25		ns
t_{ACS}	Chip Select to Output Valid	Note 9		12		15	ns
t_{HZCS}	Chip Select Inactive to High Z	Note 8, 10		12		15	ns
t_{LZCS}	Chip Select Active to Low Z			12		15	ns
t_{OHA}	Output Hold from Address Change		5		5		ns
t_{AA}	Address Access Time	Note 9		18		25	ns
WRITE CYCLE[7]							
t_{WC}	Write Cycle Time		15		20		ns
t_{HZWE}	Write Enable Active to High Z	Note 8, 10		12		20	ns
t_{LZWE}	Write Enable Inactive to Low Z			12		20	
t_{AWE}	Write Enable Inactive to Output Valid	Note 9		12		20	ns
t_{PWE}	Write Enable Pulse Width		15		20		ns
t_{SD}	Data Setup to Write End		15		20		ns
t_{HD}	Data Hold from Write End		0		0		ns
t_{SA}	Address Setup to Write Start		0		0		ns
t_{HA}	Address Hold from Write End		0		0		ns

Notes:

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL} /I_{OH} and 30 pF load capacitance.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input.
9. t_{AA}, t_{ACS} and t_{AWE} are tested with C_L = 30 pF as in *Figure 1a*. Timing is referenced to 1.5V on the inputs and outputs.
10. t_{HZCS} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*.

Bit Map



0011-5

Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

AC Test Loads and Waveforms

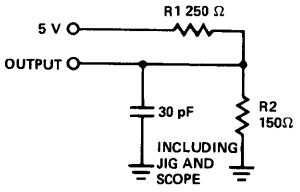
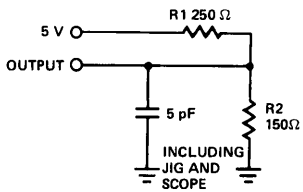
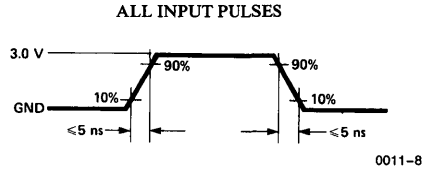


Figure 1a



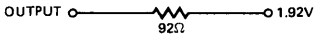
0011-6

Figure 1b



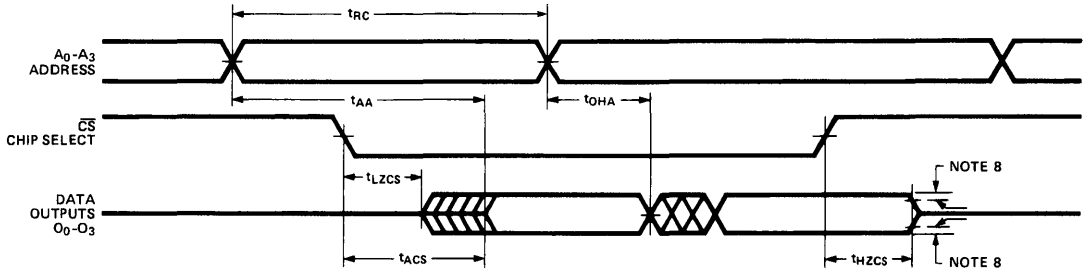
0011-8

Equivalent to: THÉVENIN EQUIVALENT



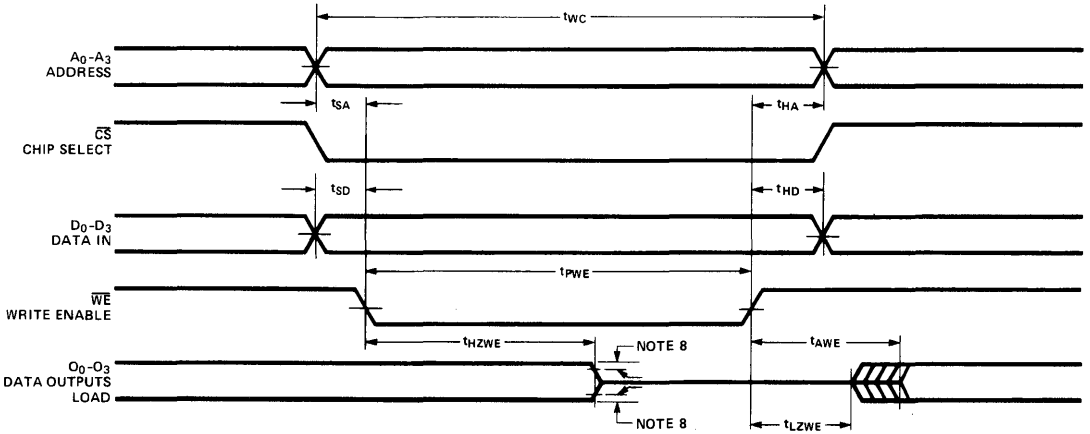
0011-7

Read Mode



0011-9

Write Mode



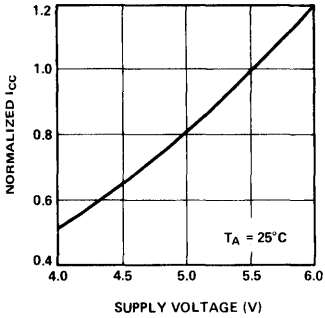
0011-10

(All above measurements referenced to 1.5V.)

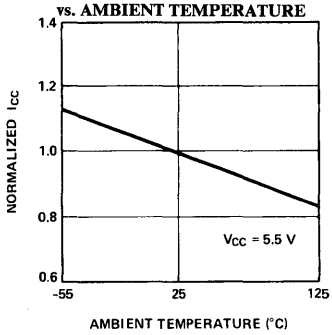
Note:
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

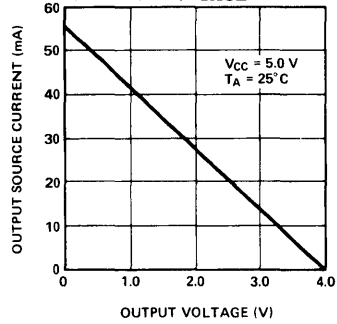
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



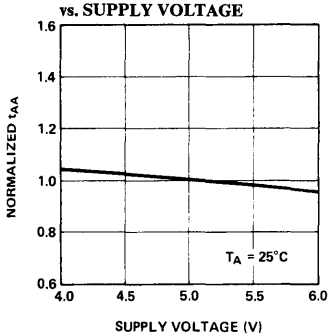
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



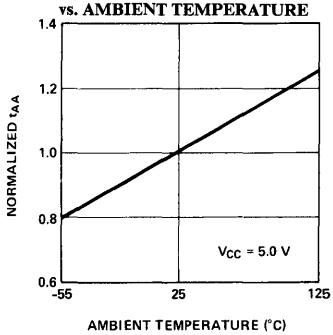
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



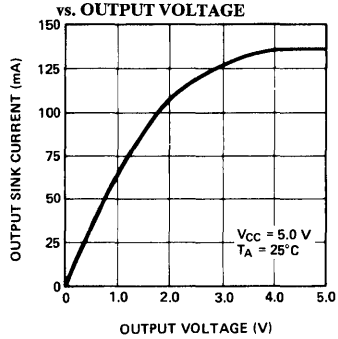
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



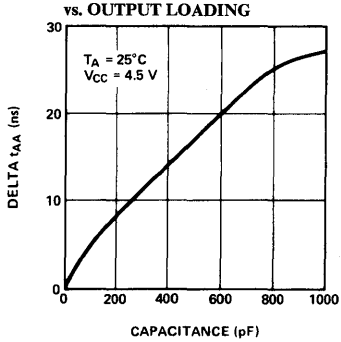
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



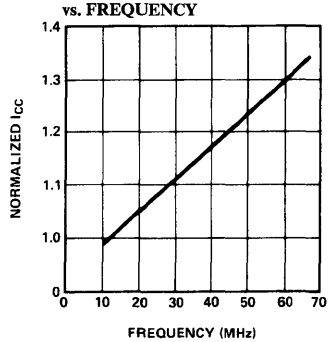
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY

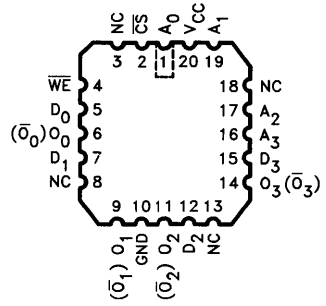


0011-11

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
18	CY7C189-18PC CY7C190-18PC	P1	Commercial
	CY7C189-18DC CY7C190-18DC	D2	
	CY7C189-18LC CY7C190-18LC	L61	
25	CY7C189-25PC CY7C190-25PC	P1	
	CY7C189-25DC CY7C190-25DC	D2	
	CY7C189-25LC CY7C190-25LC	L61	
	CY7C189-25DMB CY7C190-25DMB	D2	Military
	CY7C189-25LMB CY7C190-25LMB	L61	

Pin Configuration



0011-4

2

CY74S189, CY54S189
CY27S03, CY27S07

CYPRESS SEMICONDUCTOR

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high speed CMOS RAMs**
- **Inverting outputs 27S03, 74S189, 54S189**
- **Non-inverting outputs 27S07**
- **High speed — 25 ns**
- **Low power — 495 mW**
- **Power supply 5V ±10%**
- **Advanced high speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2000V static discharge**
- **Three-state outputs**
- **TTL compatible interface levels**

Functional Description

These devices are high performance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting and non-inverting outputs.

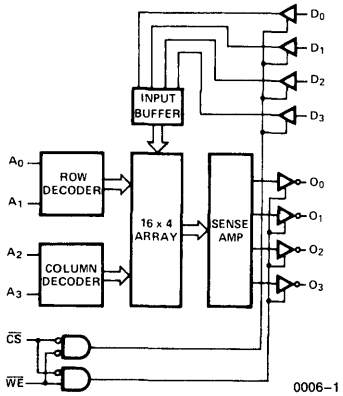
An active LOW write enable ($\overline{WE}$) signal controls the writing and reading of the memory. When the write enable ($\overline{WE}$) and chip select ($\overline{CS}$) are both LOW the information on the four data inputs (D_0–D_3) is written into the location addressed by the information on the address lines (A_0–A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0–O_3) when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is accomplished with an active LOW on the chip select line ($\overline{CS}$) and a HIGH on the write enable ($\overline{WE}$) line. The information stored is read out from the addressed location and presented at the outputs in inverted or non-inverted format.

During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

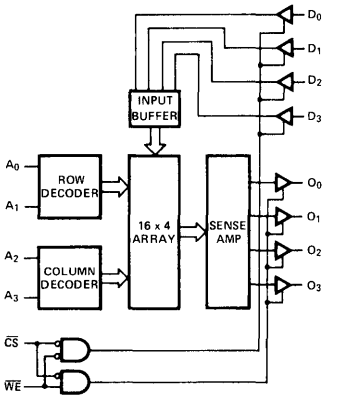
Logic Block Diagrams

27S03
74S189, 54S189



0006-1

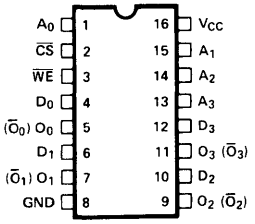
27S07



0006-2

Pin Configuration

27S07
(27S03, 74S189, 54S189)



0006-3

Selection Guide (For higher performance and lower power refer to CY7C189/90 data sheet.)

		27S03A 27S07A	27S03, 27S07 74S189, 54S189
Maximum Access Time (ns)	Commercial	25	35
	Military	25	35
Maximum Operating Current (mA)	Commercial	90	90
	Military	100	100

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 16 to 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) .....20 mA

Static Discharge Voltage.....>2001 V (per MIL-STD-883 Method 3015.2)

Latchup Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		Min.	Max.
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4	
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45
V_{IH}	Input HIGH Voltage			2.0	V_{CC}
V_{IL}	Input LOW Voltage			−3.0	0.8
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10
V_{CD}	Input Diode Clamp Voltage[2]				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		−40	+40
I_{OS}	Output Short Circuit Current [3]	V_{CC} = Max., V_{OUT} = GND			−90
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90
			Military		100

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. The CMOS process does not provide a clamp diode. However these devices are insensitive to −3V dc input levels and −5V undershoot pulses of less than 5 ns (measured at 50% points).
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Output is precoditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
5. Tested on a sample basis.

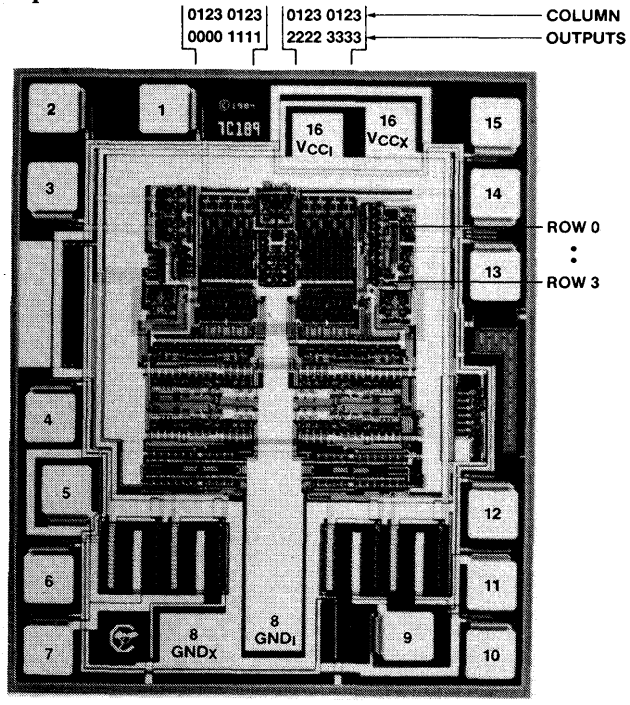
Switching Characteristics Over the Operating Range[6]

Parameters	Description	27S03A 27S07A		27S03 27S07		74S189 54S189		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		35		ns
t_{AA}	Address to Data Valid		25		35		35	ns
t_{ACS}	$\overline{CS}$ Low to Data Valid		15		17		22	ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[8, 10]		15		20		17	ns
WRITE CYCLE[6, 7]								
t_{WC}	Write Cycle Time	25		35		35		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SCS}	$\overline{CS}$ Set-up to Write Start					0		ns
t_{HCS}	$\overline{CS}$ Hold from Write End					0		ns
t_{SD}	Data Set-up to Write Start	20		25		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		20		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 10]		20		25		20	ns
t_{AWE}	$\overline{WE}$ HIGH to Output Valid		20		35		30	ns

Notes:

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to intiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. Transition is measured at steady state HIGH level −500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.
9. t_{AA}, t_{ACS} and t_{AWE} are tested with C_L = 30 pF as in *Figure 1a*. Timing is referenced to 1.5V on the inputs and outputs.
10. t_{HZCS} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*.

Bit Map



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Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

AC Test Loads and Waveforms

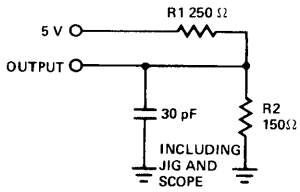


Figure 1a

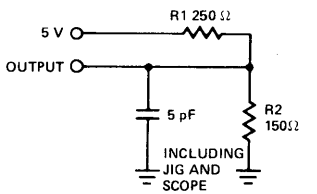
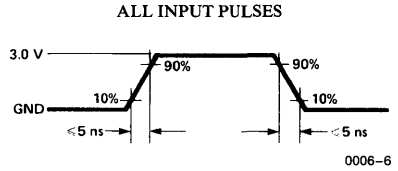
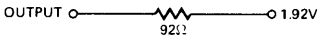


Figure 1b



Equivalent to: THÉVENIN EQUIVALENT



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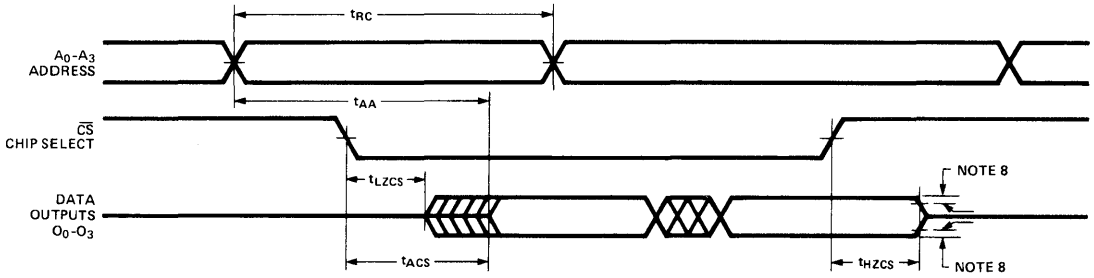
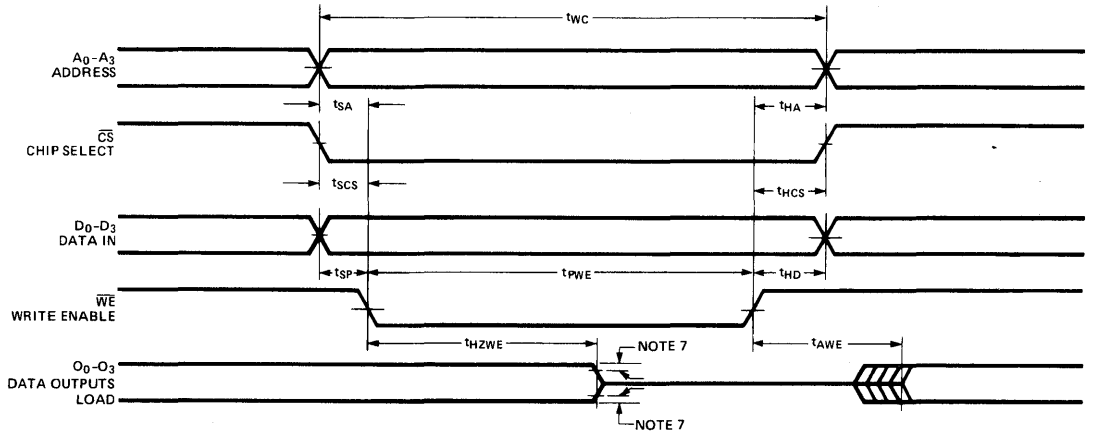
Read Mode



0006-7

Write Mode



0006-8

(All above measurements referenced to 1.5V)

Note: Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY27S03APC CY27S07APC	P1	Commercial
	CY27S03ADC CY27S07ADC	D2	
	CY27S03ADMB CY27S07ADMB	D2	Military
35	CY27S03PC CY27S07PC CY74S189PC	P1	Commercial
	CY27S03DC CY27S07DC CY74S189DC	D2	
	CY27S03DMB CY27S07DMB CY54S189DMB	D2	Military

CY93422A/93L422A
CY93422/93L422

CYPRESS SEMICONDUCTOR

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control stores in high speed computer**
- **Processed with high speed CMOS for optimum speed/power**
- **Separate inputs and outputs**
- **Low power**
  - **— Standard power:**
    660 mW (commercial)
    715 mW (military)
  - **— Low power:**
    440 mW (commercial)
    495 mW (military)
- **5 volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2000V static discharge**

Functional Description

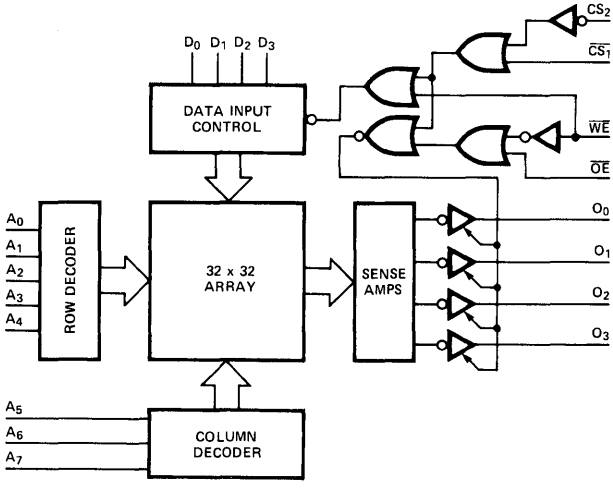
The CY93422 is a high performance CMOS static RAM organized as 256 x 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

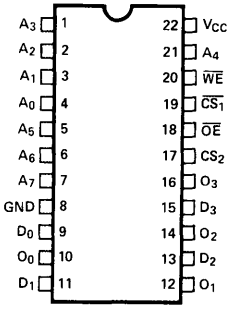
The outputs of the memory go to an active high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



0002-1

Pin Configuration



0002-2

Selection Guide (For higher performance and lower power refer to CY7C122 data sheet)

		93422A	93L422A	93422	93L422
Maximum Access Time (ns)	Commercial	35	45	45	60
	Military	45	55	60	75
Maximum Operating Current (mA)	Commercial	120	80	120	80
	Military	130	90	130	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs for High Output State ..... −0.5V to V_{CC} Max

DC Input Voltage ..... −0.5V to +5.5V

Output Current, into Outputs (Low) ..... 20 mA

DC Input Current ..... −30 mA to +5.0 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	V_{CC}	Ambient Temperature
Commercial	5V ±10%	0°C to +75°C
Military[5]	5V ±10%	−55°C to +125°C

Function Table

Inputs					Outputs	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Select
X	H	X	X	X	*HIGH Z	Not Select
H	L	H	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*HIGH Z	Write "0"
H	L	L	X	H	*HIGH Z	Write "1"

H = High Voltage Level L = Low Voltage Level X = Don't Care

*HIGH Z implies outputs are disabled or off. This condition is defined as a high impedance state for the CY93422.

DC Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions		93422 93422A		93L422 93L422A		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.45		0.45	V
V_{IH}	Input HIGH Level[1]	Guaranteed Input Logical HIGH Voltage for all Inputs		2.1		2.1		V
V_{IL}	Input LOW Level[1]	Guaranteed Input Logical LOW Voltage for all Inputs			0.8		0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40V			−300		−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5V			40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]			−90		−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.	T_A = 125°C		110		70	mA
			T_A = 75°C		110		70	
			T_A = 0°C		120		80	
			T_A = −55°C		130		80	
V_{CL}	Input Clamp Voltage			See Note 4		See Note 4		
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V			50		50	μA
		V_{OUT} = 0.5V, V_{CC} = Max.		−50		−50		
C_{IN}	Input Pin Capacitance	See Note 3			4		4	pF
C_{OUT}	Output Pin Capacitance	See Note 3			7		7	pF

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. Input and output capacitance measured on a sample basis at f = 1.0 MHz.
4. The CMOS process does not provide a clamp diode. However, the CY93422 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
5. Extended temperature operation guaranteed with 400 linear feet per minute air flow.

Commercial Switching Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +75°C (Unless Otherwise Noted)

Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[1] $t_{PHL(A)}$[1]	Delay from Address to Output (Address Access Time) (See *Figure 2*)		35		45		45		60	ns
t_{PZH} ($\overline{CS_1}$, CS_2) t_{PZL} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Active Output and Correct Data (See *Figure 2*)		25		30		30		35	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See *Figure 1*)		25		40		40		45	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data (See *Figure 2*)		25		30		30		35	ns
t_s (A)	Setup Time Address (Prior to Initiation of Write) (See *Figure 1*)	5		5		10		10		ns
t_h (A)	Hold Time Address (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s (DI)	Setup Time Data Input (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s ($\overline{CS_1}$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write (See *Figure 1*)	20		40		30		45		ns
t_{PHZ} ($\overline{CS_1}$, CS_2) t_{PLZ} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Inactive Output (HIGH Z) (See *Figure 2*)		30		40		30		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (HIGH Z) (See *Figure 1*)		30		40		35		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (HIGH Z) (See *Figure 2*)		30		40		30		45	ns

Notes:

1. t_{PLH} (A) and t_{PHL} (A) are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
2. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS_1}$, CS_2) and t_{PZH} ($\overline{OE}$) are measured with S_1 open, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS_1}$, $\overline{CS_2}$) and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$), t_{PHZ} ($\overline{CS_1}$, CS_2) and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, $C_L \leq 5$ pF and are measured between the 1.5V level on the input to the V_{OH} −500 mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS_1}$, CS_2) and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5V level on the input and the V_{OL} +500 mV level on the output.

2

Military Switching Characteristics V_{CC} = 5V ±10%, T_A = −55°C to +125°C (Unless Otherwise Noted)

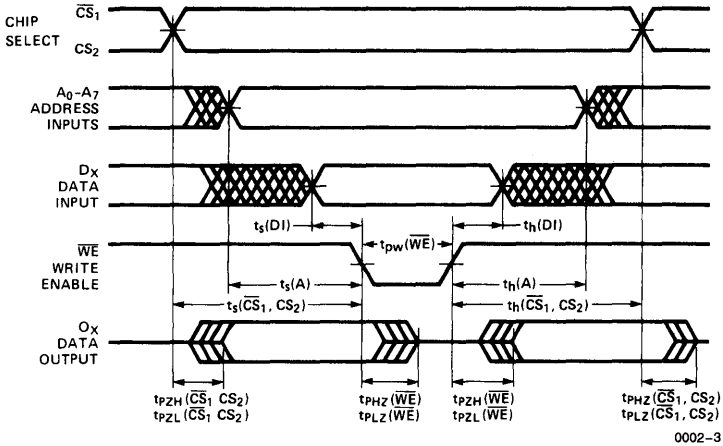
Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[1] $t_{PHL(A)}$[1]	Delay from Address to Output (Address Access Time) (See *Figure 2*)		45		55		60		75	ns
t_{PZH} ($\overline{CS_1}$, CS_2) t_{PZL} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Active Output and Correct Data (See *Figure 2*)		35		40		45		45	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See *Figure 1*)		40		45		50		50	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data (See *Figure 2*)		35		40		45		45	ns
t_s (A)	Setup Time Address (Prior to Initiation of Write) (See *Figure 1*)	5		10		10		10		ns
t_h (A)	Hold Time Address (After Termination of Write) (See *Figure 1*)	5		5		5		10		ns
t_s (DI)	Setup Time Data Input (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Termination of Write) (See *Figure 1*)	5		5		5		5		ns
t_s ($\overline{CS_1}$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write) (See *Figure 1*)	5		5		5		5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write) (See *Figure 1*)	5		5		5		10		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write (See *Figure 1*)	35		40		40		45		ns
t_{PHZ} ($\overline{CS_1}$, CS_2) t_{PLZ} ($\overline{CS_1}$, CS_2)	Delay from Chip Select to Inactive Output (HIGH Z) (See *Figure 2*)		35		40		45		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (HIGH Z) (See *Figure 1*)		40		40		45		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (HIGH Z) (See *Figure 2*)		35		40		45		45	ns

Notes:

1. t_{PLH} (A) and t_{PHL} (A) are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
2. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS_1}$, CS_2) and t_{PZH} ($\overline{OE}$) are measured with S_1 open, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS_1}$, CS_2) and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$), t_{PHZ} ($\overline{CS_1}$, CS_2) and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, $C_L \leq 5$ pF and are measured between the 1.5V level on the input to the V_{OH} − 500 mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS_1}$, CS_2) and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5V level on the input and the V_{OL} + 500 mV level on the output.

Switching Waveforms

Write Mode (with $\overline{OE}$ = Low)



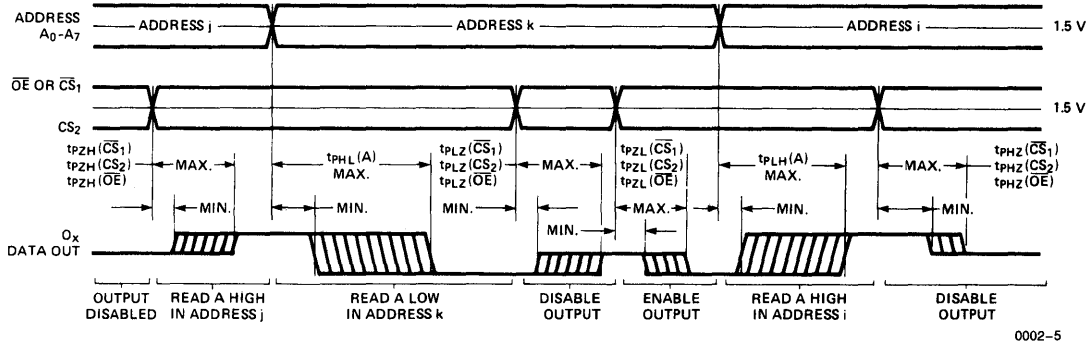
Key to Timing Diagram

Waveform	Inputs	Outputs
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care; any change permitted	Changing; state unknown
	Does not apply	Center line is high impedance "off" state

0002-4

Figure 1

Read Mode



Switching delays from address input, output enable input and the chip select inputs to the data output. The CY93422 disabled output in the "OFF" condition is represented by a single center line.

Figure 2

AC Test Load and Waveform

AC Test Load

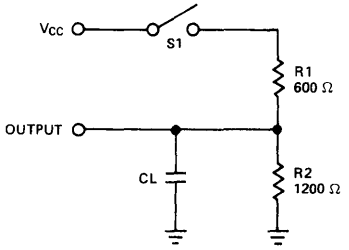


Figure 3

Input Pulses

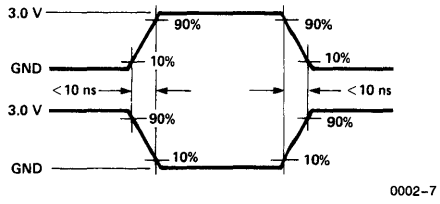


Figure 4

See Notes 1 and 2 of Switching Characteristics

Ordering Information

Speed (ns)	Ordering Code		Package Type	Operating Range
	Std. Power	Low Power		
35	CY93422APC CY93422ADC		P7 D8	Commercial
45	CY93422PC CY93422DC	CY93L422APC CY93L422ADC	P7 D8	Commercial
45	CY93422ADMB		D8	Military
55		CY93L422ADMB	D8	Military
60	CY93422DMB		D8	Military
60		CY93L422PC CY93L422DC	P7 D8	Commercial
75		CY93L422DMB	D8	Military

Section Contents

PROMs (Programmable Read Only Memory)

1: Product Line Overview

The Cypress family of CMOS PROMs consists of devices of three basic densities, two functional configurations and two package options. All devices are organized with byte wide outputs and are available in depths of 512, 1024 and 2048 bytes. All densities are available with registered outputs that operate in synchronous and asynchronous modes. Devices without registers are available in 1024 by 8 and 2048 by 8 configurations. These 8K and 16K non-registered devices are available in popular 0.3 inch and 0.6 inch wide dual inline packages as well as LCC varieties. Registered devices are available in 0.3 in dual inline packages as well as LCC.

All Cypress CMOS PROMs perform at or beyond the levels of the bipolar product that they replace at much reduced power levels. CMOS technology provides superior reliability, 10% power supply margins and is capable of withstanding greater than 2001 volts of electrostatic discharge.

2: Technology Introduction

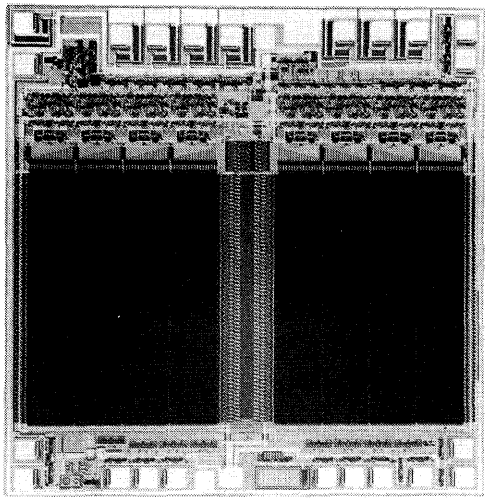
Cypress PROMs are executed in an "N" well 1.2 micron CMOS process. This process provides basic gate delays of 125 picoseconds for a fanout of one at a power consumption of 45 femto joules. This process provides the basis for the development of LSI products that outperform the fastest bipolar products currently available.

Although CMOS static RAMs have challenged bipolar RAMs for speed, CMOS EPROMs have always been a factor of three to ten times slower than bipolar fuse PROMs. There have been two major limitations on CMOS EPROM speed; 1) the single transistor EPROM cell is inherently slower than the bipolar fuse element, and 2) CMOS EPROM technologies have been optimized for cell programmability and density, almost always at the expense of speed. In the CMOS EPROM technology in production, both of the aformentioned limitations have been overcome to create CMOS PROMs with performance superior to PROMs implemented in bipolar technology.

Speed and programmability are optimized independently by separating the read and write transistor functions in a new FOUR TRANSISTOR DIFFERENTIAL EPROM CELL and by using a true differential sensing technique rather than the traditional dummy cell coupled with a differential sensing approach. Also, for the first time a substrate bias generator is employed in an EPROM technology to improve performance and raise latchup immunity to greater than 200 mA. Although the result is not a design technology that will challenge the high density EPROMs, it does more than compete in both performance and density with bipolar programmable technology utilizing fuses. Limitations of devices implemented in the bipolar fuse technology such as PROGRAMMING YIELD, POWER DISSIPATION and HIGHER DENSITY PERFORMANCE are eliminated or greatly reduced using Cypress CMOS EPROM technology.

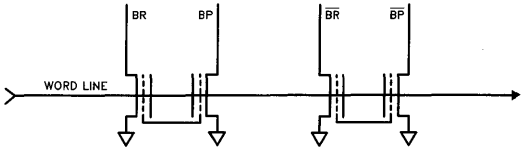
2.1: FOUR TRANSISTOR CELL AND DIFFERENTIAL DESIGN TECHNIQUES

The 16K PROM uses an N-Well CMOS technology along with a new differential four transistor EPROM cell that is optimized for speed. The area of the four transistor cell is 0.43 square mils and the die size is 19,321 square mils for the 2K by 8 PROM (*Figure 1*). The floating gate cell is optimized for high read current and fast programmability. This is accomplished by separating the read and program transistors (*Figure 2*). The program transistor has a separate implant to maximize the generation and collection of hot electrons while the read transistor implant dose is chosen to provide a large read current. Both the n and p channel peripheral transistors have self-aligned, shallow, lightly doped drain (LDD) junctions. The LDD structure reduces overlap capacitance for speed improvement and minimizes hot electron injection for improved reliability. Although common for NMOS static and dynamic RAMs, an on-chip substrate bias generator is used for the first time in an EPROM technology. The results are improved speed, greater than 200 mA latch-up immunity and high parasitic field inversion voltages during programming.



0034-1

Figure 1



0034-2

Figure 2. Non-volatile cell optimized for speed and programmability

Access times of less than 35 ns at 16K densities and 30 ns at 4K and 8K densities over the full operating range are achieved by using differential design techniques and by totally separating the read and program paths. This allows the read path to be optimized for speed. The X and Y decoding paths are predecoded to optimize the power-delay product. A differentail sensing scheme and the four transis-

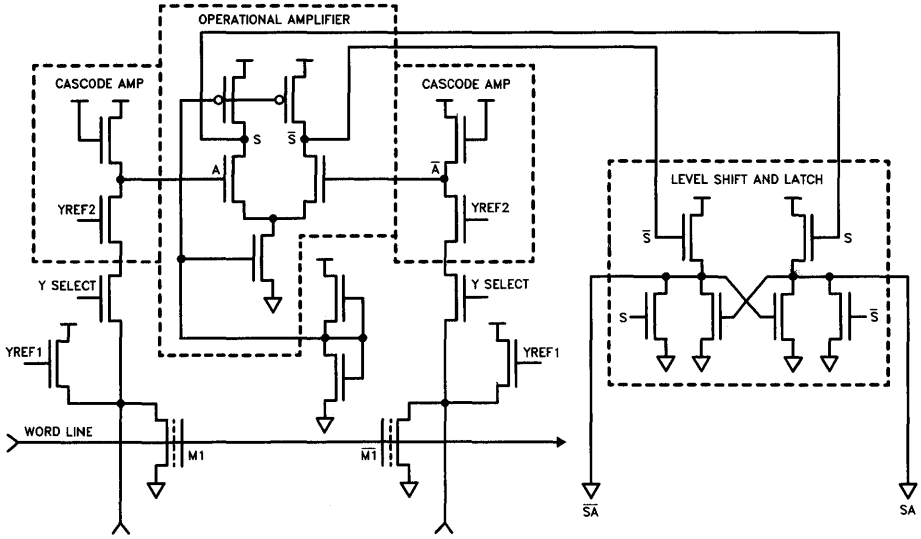


Figure 3. Differential sensing

tor cell are used to sense bit-line swings as low as 100 mV at high speed. The sense amplifier (*Figure 3*) consists of three stages of equal gain. A gain of 4 per stage was found to be optimum. The Cascode stage amplifies the bit line swings and feeds them into a differential amplifier. The output of the differential amplifier is further amplified and voltages shifted by a level shifter and latch. This signal is then fed into an output buffer having a TTL fan-out of ten.

2.2: PROGRAMMING

The 2K x 8 PROM is programmed a BYTE at a time by applying 13 to 14 volts on one pin and the desired logic levels to input pins. Unlike conventional programmable memories that default to a logic "ONE", both logic "ONE" and logic "ZERO" are programmed into the differential cell. A BIT is programmed by applying 13 to 14 volts on the control gate and 9 volts on the drain of the floating gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is enough to be determined as the correct logic state. Because an unprogrammed cell has neither a ONE nor a ZERO in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual BITs allowing the monitoring of the quality of programming during the manufacturing operation.

2.3: RELIABILITY

2.3.1: Programming and Functionality

The CMOS EPROM approach to PROMs has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed and erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each CMOS PROM contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged thus assuring the user that not only will every cell program, but that the product performs to the specification.

2.3.2: Product

Enhanced reliability in terms of DATA RETENTION is accomplished through the use of the fully differential sensing scheme. This technique allows the stored charge on the floating gate to discharge down to an equivalent fraction of a threshold voltage while still being sensed at the correct logic state. This feature not only enhances programming yield but also significantly improves the data retention time of the PROM over differential dummy-cell reference approaches. Data shows no failures after 450 hours at 250 degrees C. This is equivalent to 400,000 years at 70 degrees C (assuming 1.4 eV activation energy). The problem of injecting unwanted charge onto the floating gate during the read operation (read disturb) is also eliminated in this cell, since the read and program transistors are separate structures, and the program transistor drain is grounded during read operations.

CYPRESS SEMICONDUCTOR

CY7C225

512 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 30 ns max set-up**
  - **— 15 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered Common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

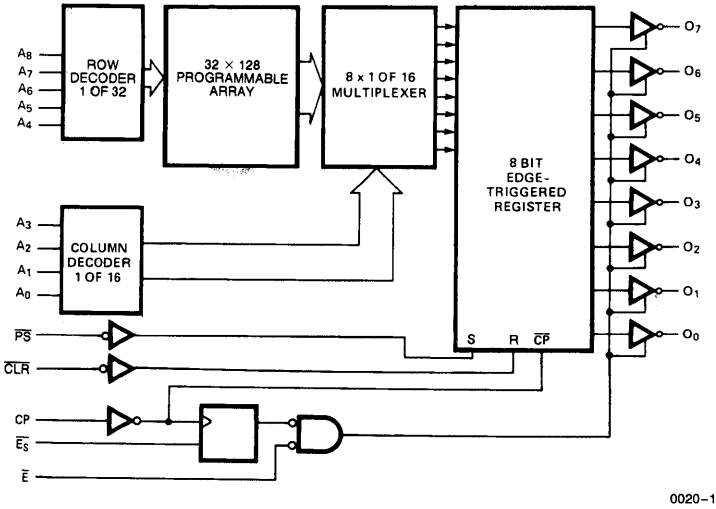
Product Characteristics

The CY7C225 is a high performance 512 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

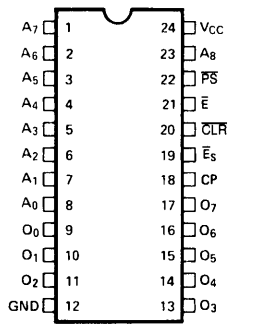
The CY7C225 has asynchronous PRESET and CLEAR functions.

Logic Block Diagram



0020-1

Pin Configuration



0020-2

Selection Guide

		7C225-30	7C225-35	7C225-40
Maximum Access Time (ns)		30	35	40
Maximum Clock to Ouput (ns)		15	20	25
Maximum Operating Current (mA)	Commercial	90		90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 6				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f= 1 MHz, V_{CC} = 5.0V	8	pF

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Input and output capacitance measured on a sample basis.
6. The CMOS process does not provide a clamp diode. However, the CY7C225 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).

Switching Characteristics Over Operating Range

Parameters	Description	7C225-30		7C225-35		7C225-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	10		10		10		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to Valid Output		20		20		20	ns
t_{RP}, t_{RC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery to Clock HIGH	20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width	20		20		20		ns
t_{LZC}	Active Output from Clock HIGH[1]		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		25		30	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		25		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level − 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms[5, 6, 7]

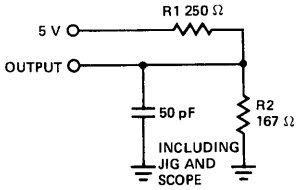


Figure 1a

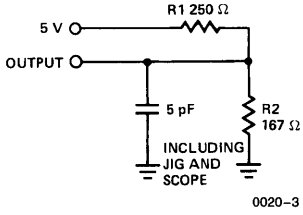


Figure 1b

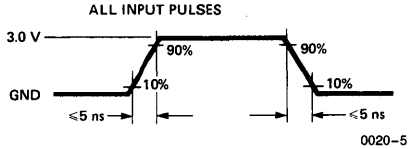
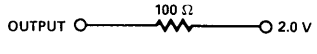


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



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Functional Description

The CY7C225 is a CMOS electrically Programmable Read Only Memory organized as 512 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables, and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address inputs (A_0–A_8) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

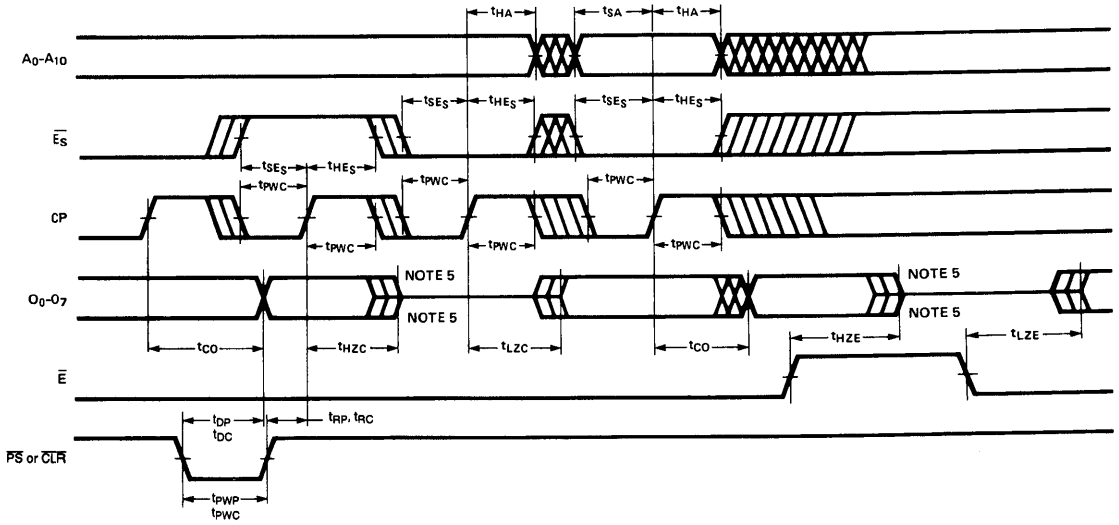
Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{E_S}$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225 has buffered asynchronous $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences.

Applying a LOW to the $\overline{\text{PRESET}}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{\text{CLEAR}}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



0020-6

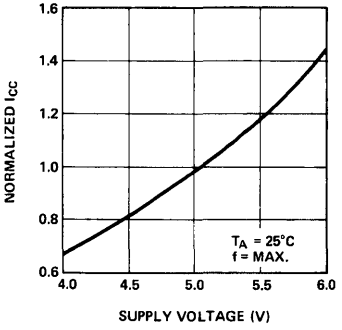
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

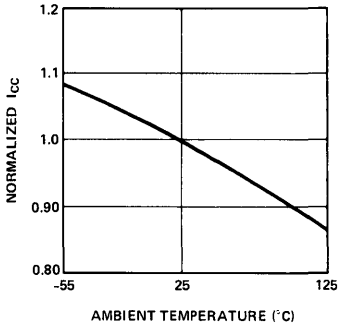
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level -500 mV or steady state LOW level $+500$ mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

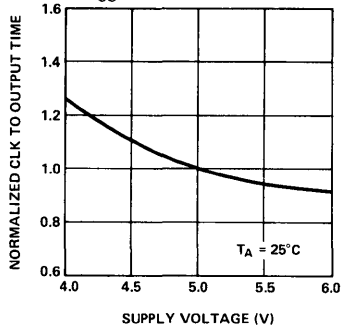
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



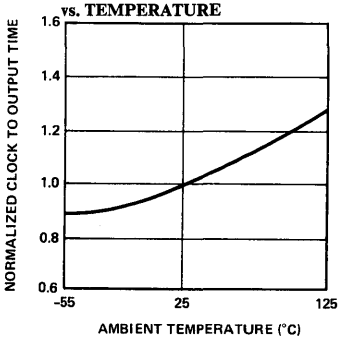
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



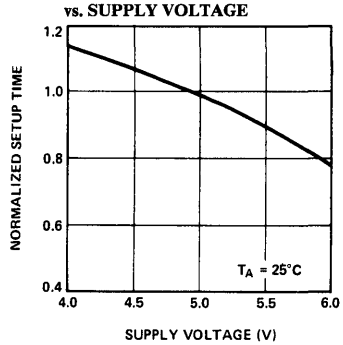
CLOCK TO OUTPUT TIME vs. V_{CC}



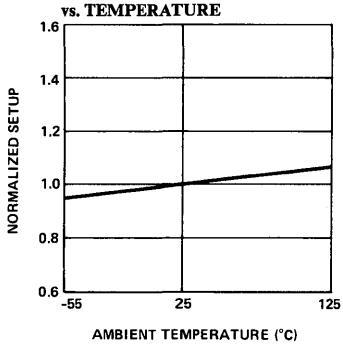
CLOCK TO OUTPUT TIME vs. TEMPERATURE



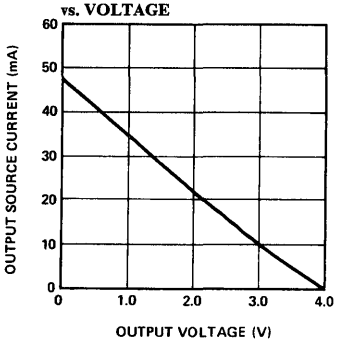
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



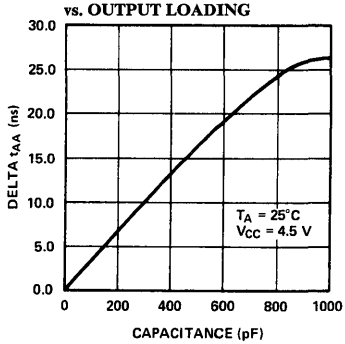
NORMALIZED SETUP TIME vs. TEMPERATURE



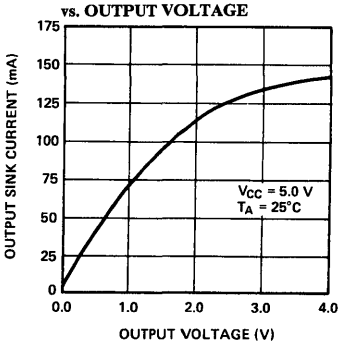
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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3

Device Programming

Overview:

There is a programmable function contained in the 7C225 CMOS 512 x 8 Registered PROM; the 512 x 8 array. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped.

The 512 x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	50		ns
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11,13–17)
	Read or Output Disable	CP	$\overline{E_S}$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	
	Pin	(18)	(19)	(20)	(21)	(22)	
Read[2,3]		X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out
Output Disable[5]		X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		X	X	V_{IH}	V_{IH}	V_{IH}	High Z
$\overline{CLEAR}$		X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
$\overline{PRESET}$		X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program[1,4]		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	V_{IHP}	Data In
Program Verify[1,4]		V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	Data Out
Program Inhibit[1,4]		V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	V_{IHP}	High Z
Intelligent Program[1,4]		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	V_{IHP}	Data In
Blank Check Ones[1,4]		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	Ones
Blank Check Zeros[1,4]		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

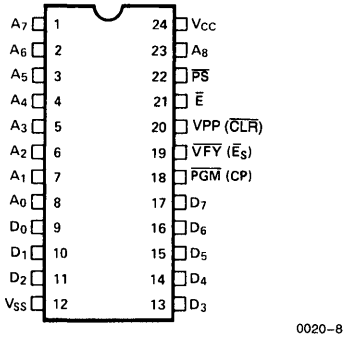

Figure 3. Programming Pinouts

The CY7C225 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

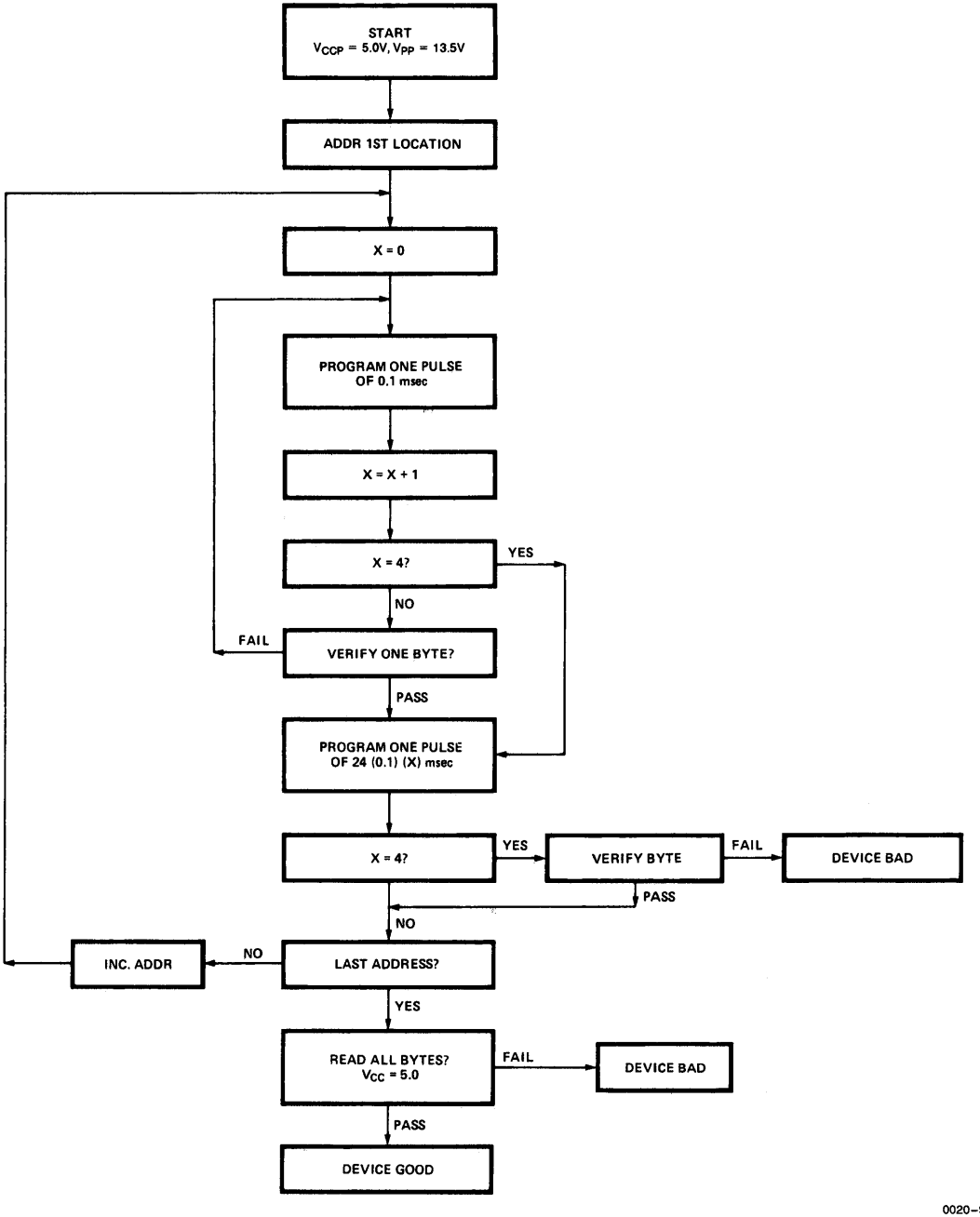

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Figure 4. Programming Flowchart

Programming Sequence 512 x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figure 5*. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 511. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

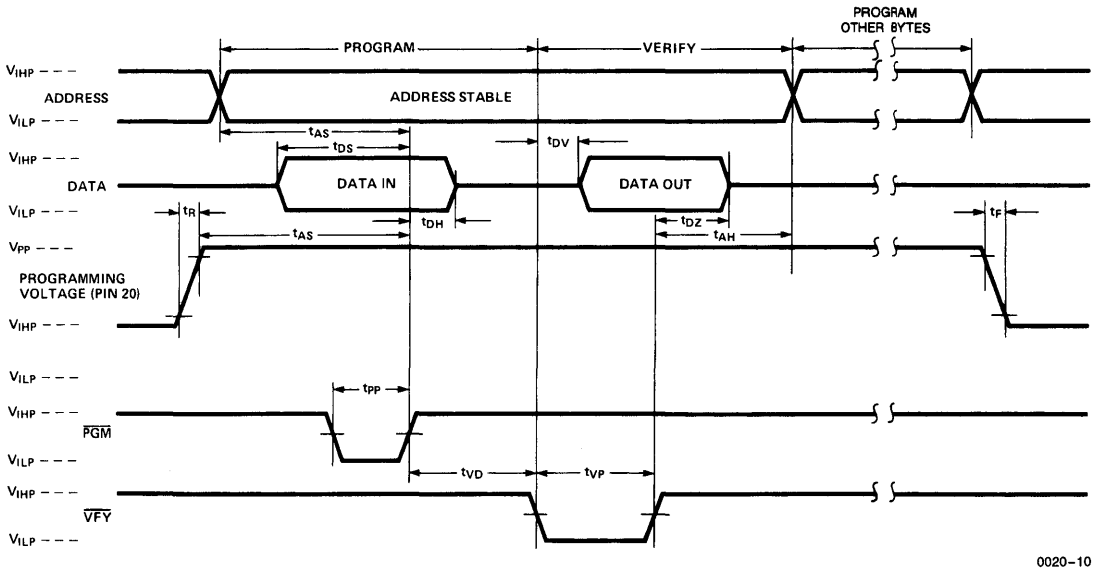


Figure 5. PROM Programming Waveforms

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
30	15	CY7C225-30PC CY7C225-30DC	P13 D14	Commercial
35	20	CY7C225-35DMB	D14	Military
40	25	CY7C225-40PC CY7C225-40DC CY7C225-40DMB	P13 D14 D14	Commercial Military

CYPRESS SEMICONDUCTOR

CY7C235

1024 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 30 ns max set-up**
  - **— 15 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

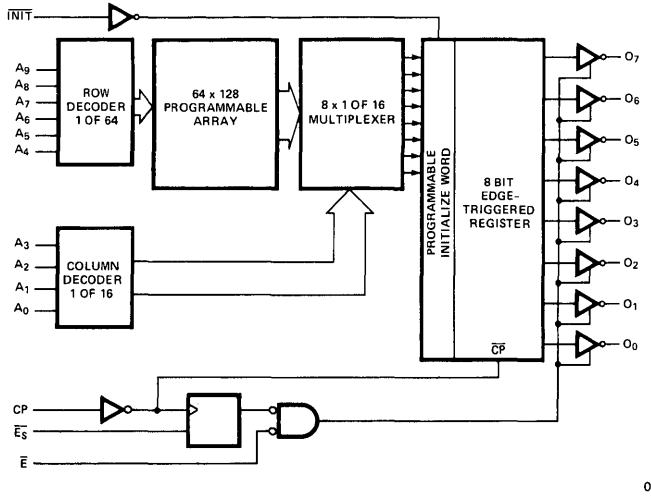
Product Characteristics

The CY7C235 is a high performance 1024 word by 8 bit Electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

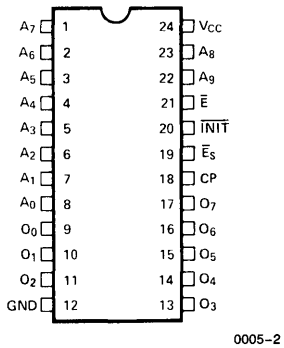
The CY7C235 has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 1025th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Logic Block Diagram



0005-1

Pin Configuration



0005-2

Selection Guide

		7C235-30	7C235-40
Maximum Set-up Time (ns)		30	40
Maximum Clock to Output (ns)		15	20
Maximum Operating Current (mA)	Commercial	90	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to + 125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Volume ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 6				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC}, V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Input and output capacitance measured on a sample basis.
6. The CMOS process does not provide a clamp diode. However, the CY7C235 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).

Switching Characteristics Over Operating Range

Parameters	Description	7C235-30		7C235-40		Units
		Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		ns
t_{CO}	Clock HIGH to Valid Output		15		20	ns
t_{PWC}	Clock Pulse Width	15		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	10		15		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	20		25		ns
t_{LZC}	Active Output from Clock HIGH[1]		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		25	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		25	ns

Notes:
1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms [5, 6, 7]

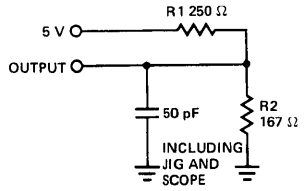


Figure 1a

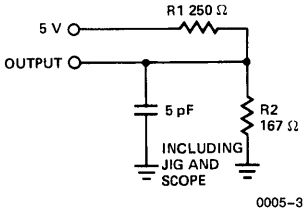


Figure 1b

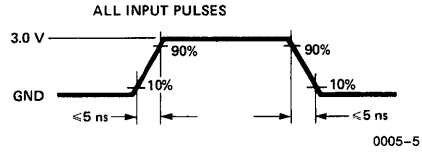
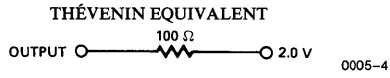


Figure 2

Equivalent to:



Functional Description

The CY7C235 is a CMOS Electrically Programmable Read Only Memory organized as 1024 word x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C235 incorporates a D-type, masterslave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{INIT}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address input (A_0–A_9) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

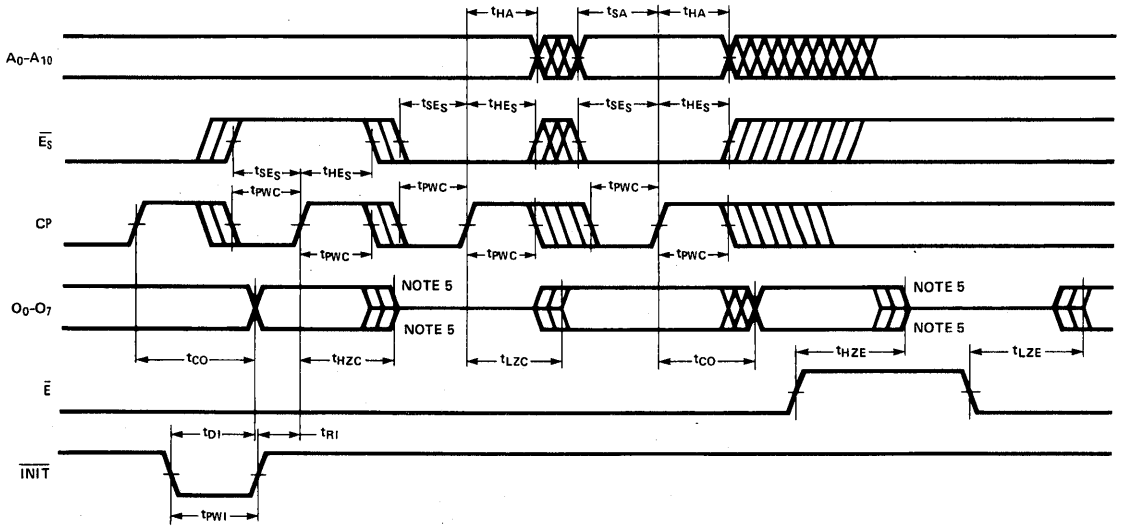
Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{E_S}$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



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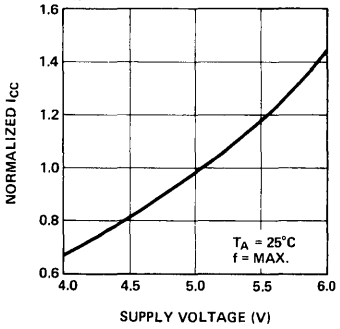
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

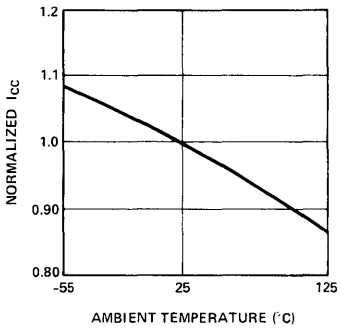
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

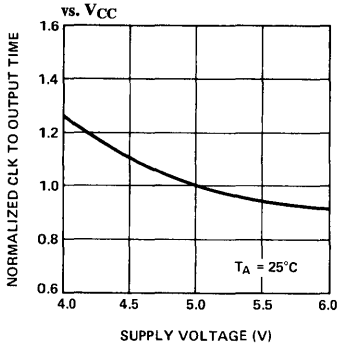
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



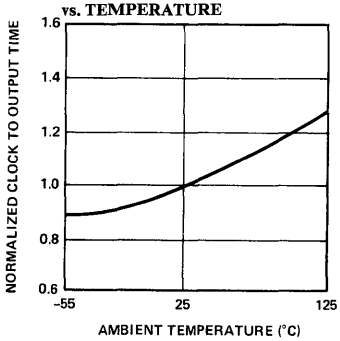
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



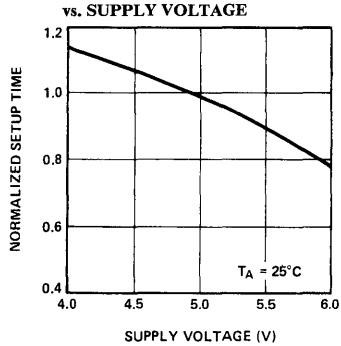
CLOCK TO OUTPUT TIME vs. V_{CC}



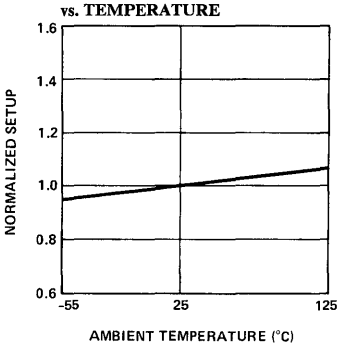
CLOCK TO OUTPUT TIME vs. TEMPERATURE



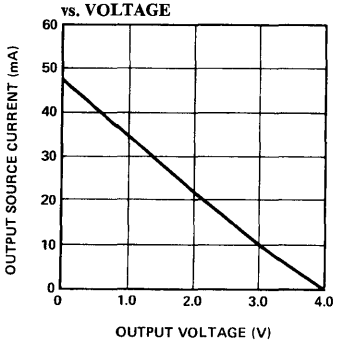
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



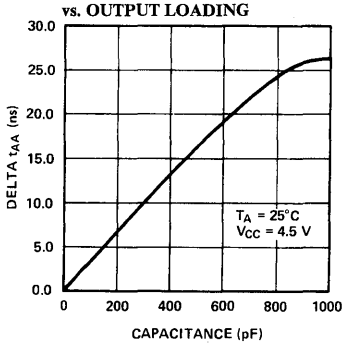
NORMALIZED SETUP TIME vs. TEMPERATURE



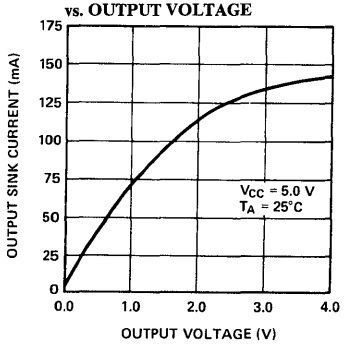
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0005-7

Device Programming

Overview:

There are two independent programmable functions contained in the 7C235 CMOS 1K x 8 Registered PROM; the 1K x 8 array, and the initial byte. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The 1K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R,t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function						Outputs (9–11, 13–17)
	Read or Output Disable	A_2	CP	$\overline{E}_S$	$\overline{INIT}$	$\overline{E}$	A_1	
	Other	A_2	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	A_1	
	Pin	(6)	(18)	(19)	(20)	(21)	(7)	
Read[2,3]		X	X	V_{IL}	V_{IH}	V_{IL}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	X	High Z
Output Disable		X	X	X	V_{IH}	V_{IH}	X	High Z
Initialize		X	X	X	V_{IL}	V_{IL}	X	1025th word
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	X	Data In
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	X	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

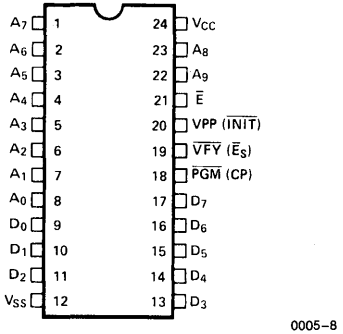


Figure 3. Programming Pinouts

The CY7C235 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

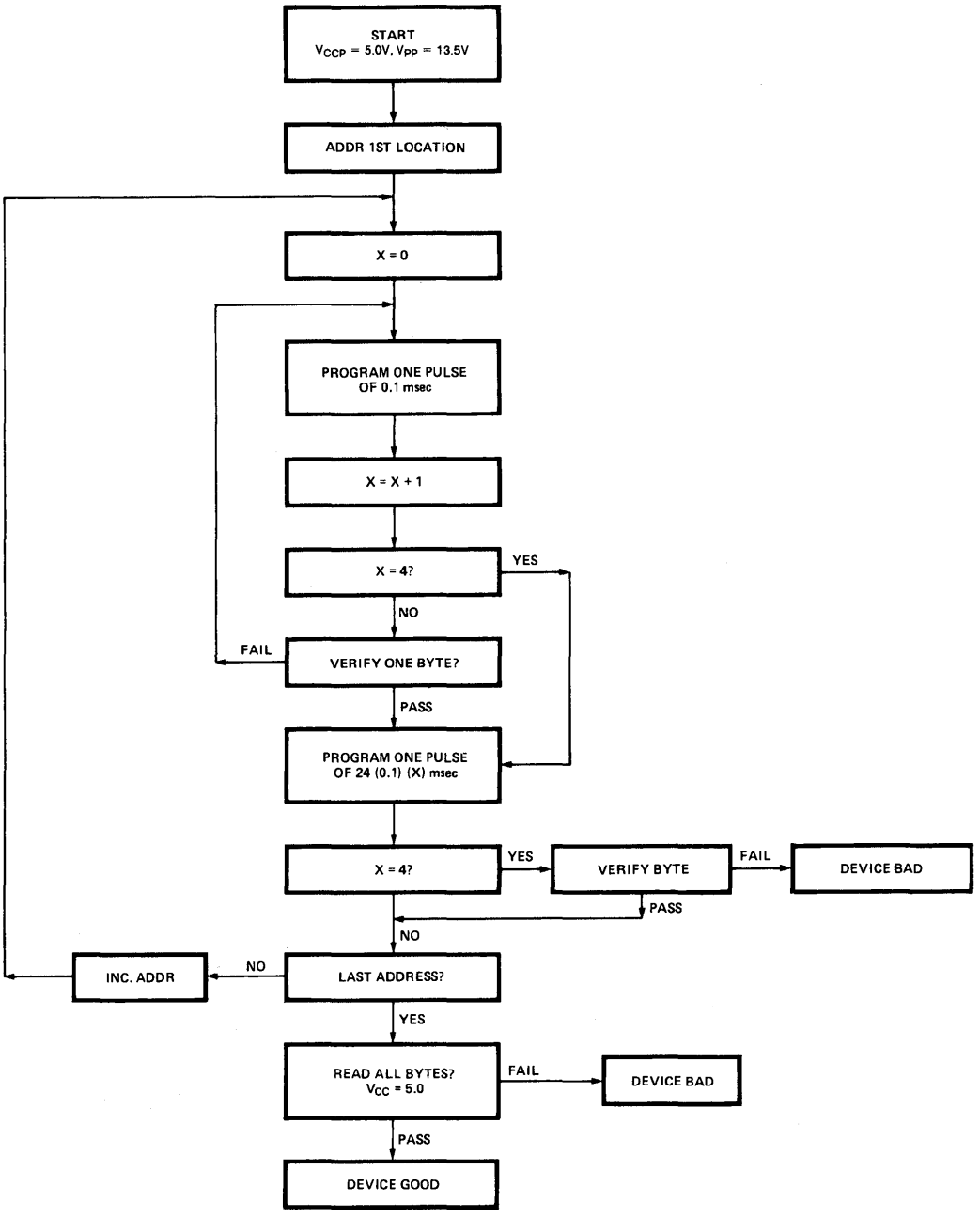


Figure 4. Programming Flowchart

Programming Sequence 1K x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 6* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 6* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

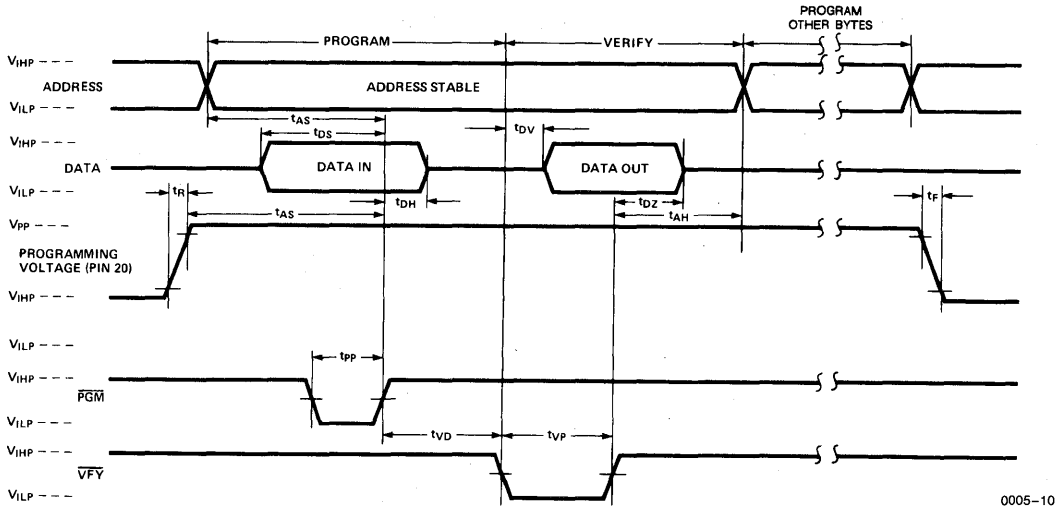


Figure 5. PROM Programming Waveforms

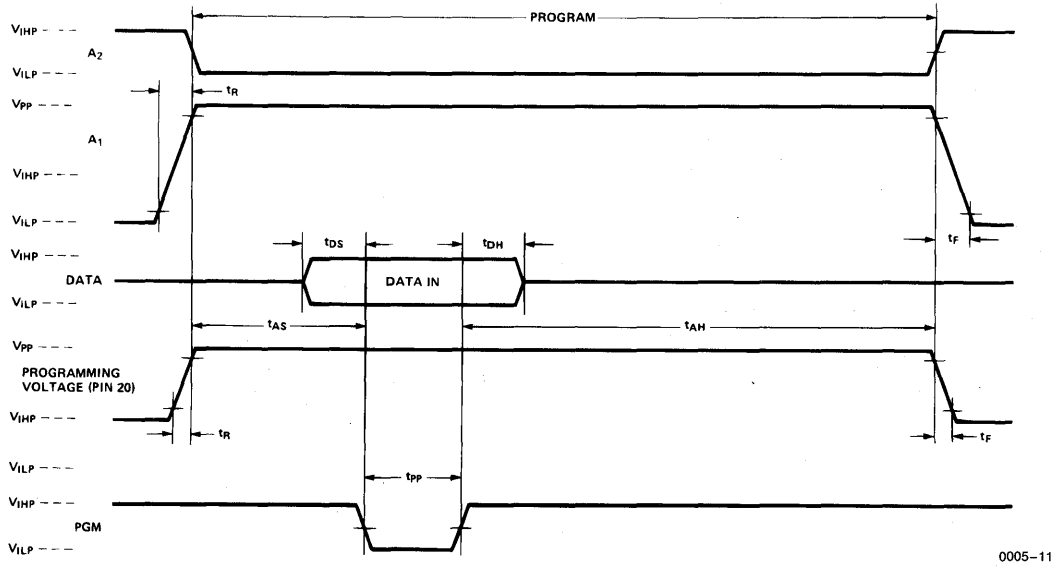


Figure 6. Initial Byte Programming Waveforms

Programming the Initial Byte

The CY7C235 registered PROM has a 1025th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 1025th byte. This byte is programmed in a similar manner to the 1024 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
30	15	CY7C235-30PC	P13	Commercial
		CY7C235-30DC	D14	
40	20	CY7C235-40PC	P13	Commercial
		CY7C235-40DC	D14	
		CY7C235-40DMB	D14	Military

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1's" and "0's" when addresses in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

CYPRESS SEMICONDUCTOR

CY7C245

2048 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns max set-up**
  - **— 15 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

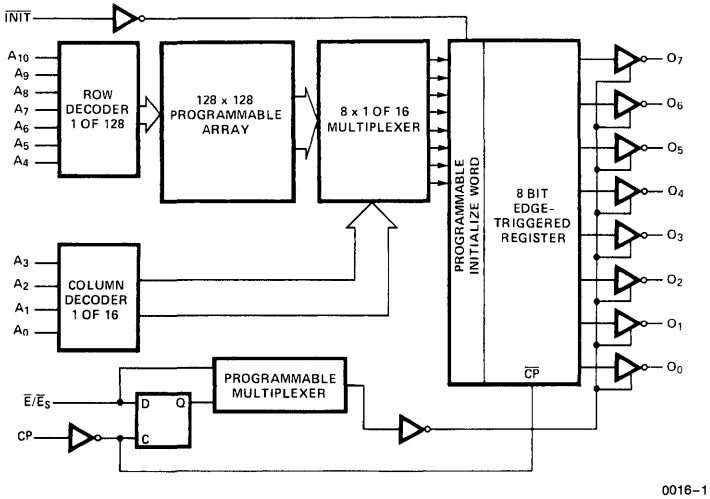
Product Characteristics

The CY7C245 is a high performance 2048 word by 8 bit Electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the super-voltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Logic Block Diagram



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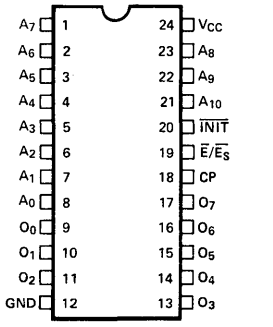
Pin Configuration



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Selection Guide

		7C245-35	7C245-45
Maximum Set-up Time (ns)		35	45
Maximum Clock to Output (ns)		15	25
Maximum Operating Current (mA)	Commercial	90	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 6				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Input and output capacitance measured on a sample basis.
6. The CMOS process does not provide a clamp diode. However, the CY7C245 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).

Switching Characteristics Over Operating Range

Parameters	Description	7C245-35		7C245-45		Units
		Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		ns
t_{CO}	Clock HIGH to Valid Output		15		25	ns
t_{PWC}	Clock Pulse Width	20		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	15		15		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		20		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	20		25		ns
t_{LZC}	Active Output from Clock HIGH[1]		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		30	ns
t_{LZE}	Active Output from $\overline{E}$ LOW[2]		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms[5, 6, 7]

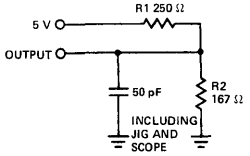


Figure 1a

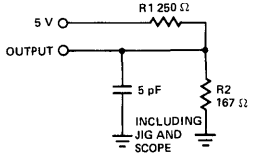


Figure 1b

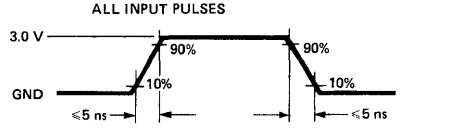
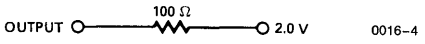


Figure 2

Equivalent to:



Functional Description

The CY7C245 is a CMOS Electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipe-lined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{INIT}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed-in, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a

Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

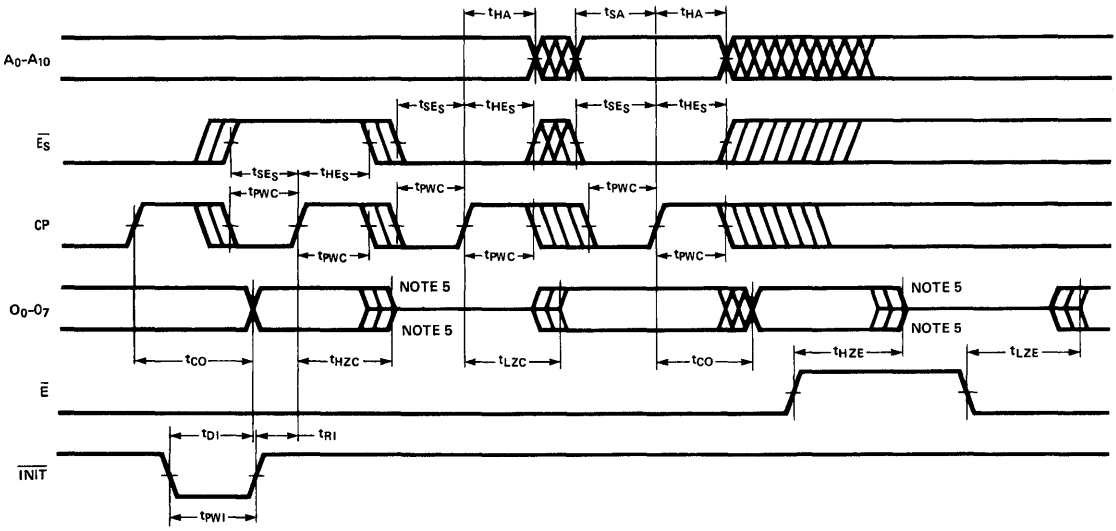
If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



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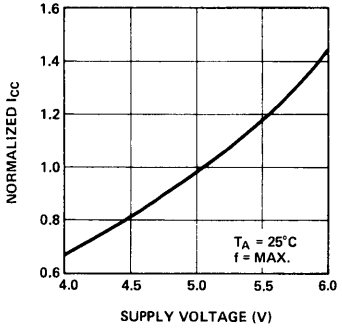
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

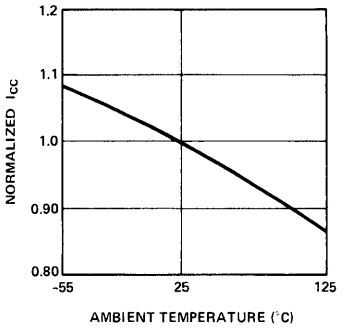
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

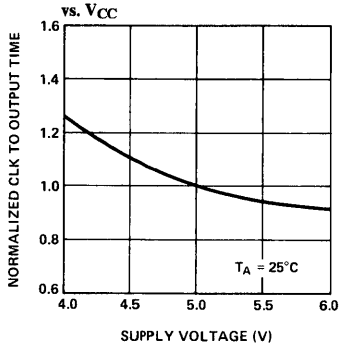
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



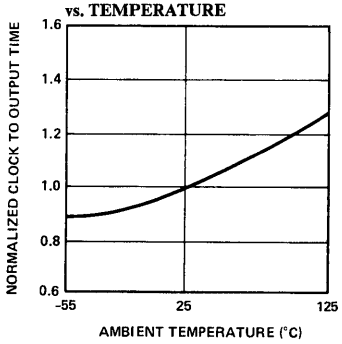
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



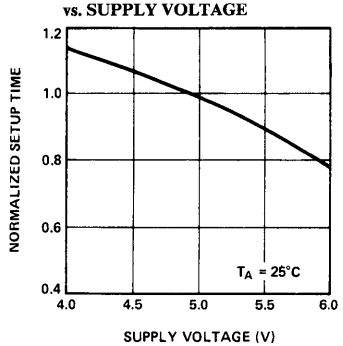
CLOCK TO OUTPUT TIME vs. V_{CC}



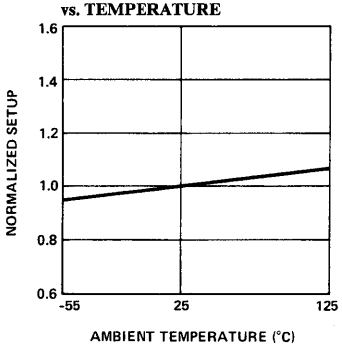
CLOCK TO OUTPUT TIME vs. TEMPERATURE



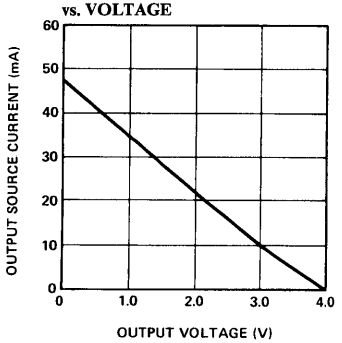
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



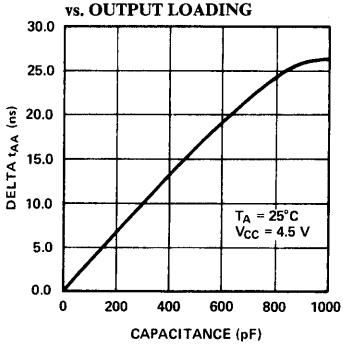
NORMALIZED SETUP TIME vs. TEMPERATURE



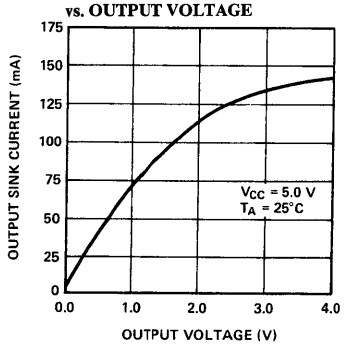
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0016-7

3

Device Programming

OVERVIEW:

These are three independent programmable functions contained in the 7C245 CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The 2K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11, 13–17)
	Read or Output Disable	A_2	CP	$\overline{E}/\overline{E}_S$	$\overline{INIT}$	A_1	
	Other	A_2	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	A_1	
	Pin	(6)	(18)	(19)	20	(7)	
Read[2,3]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	High Z
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Synch Enable[4]		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	X	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

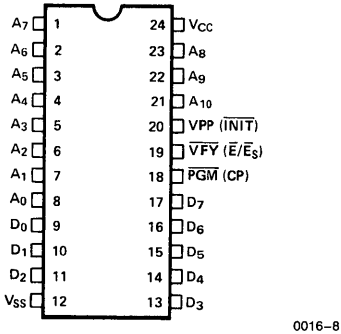


Figure 3. Programming Pinouts

The CY7C245 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

3

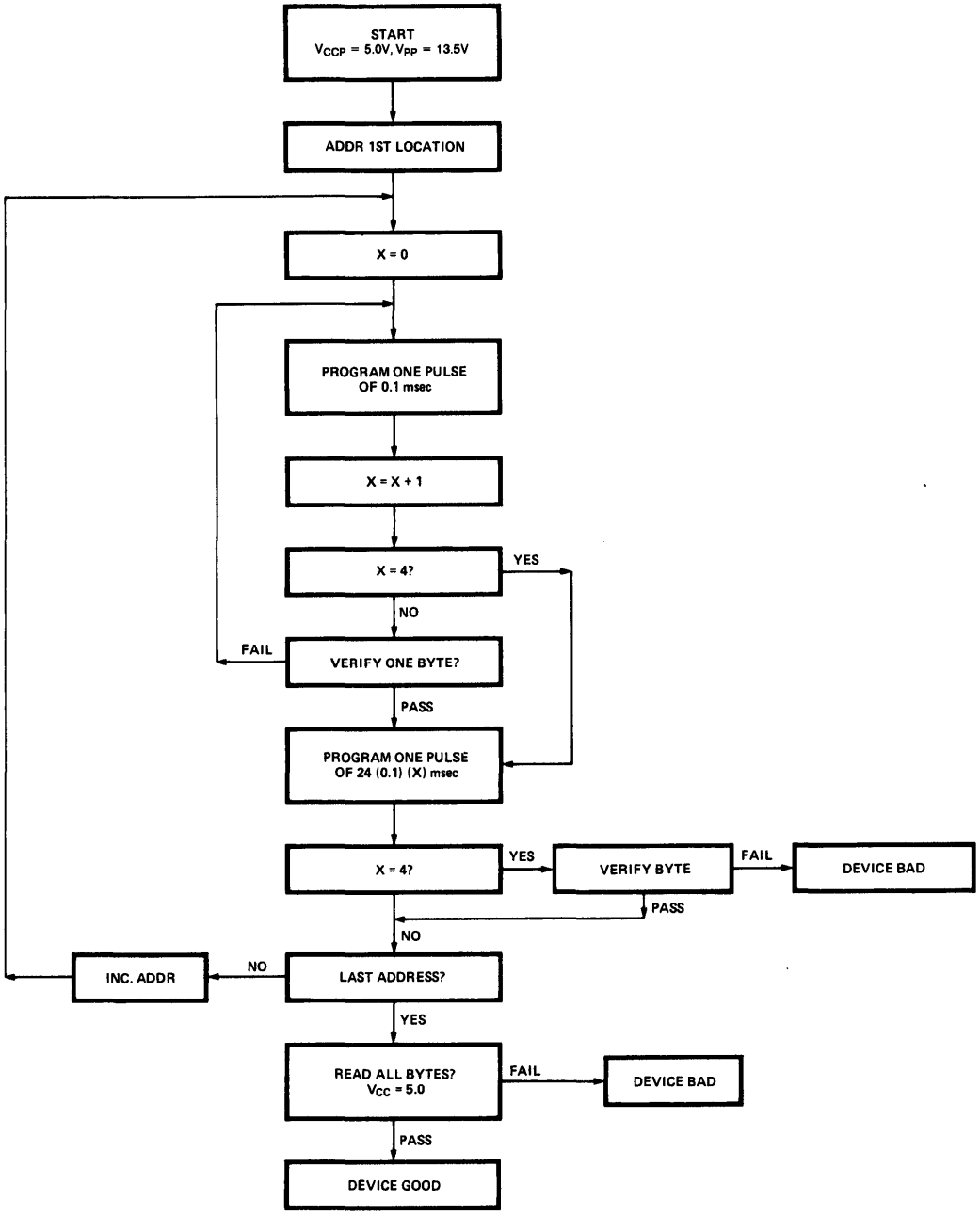


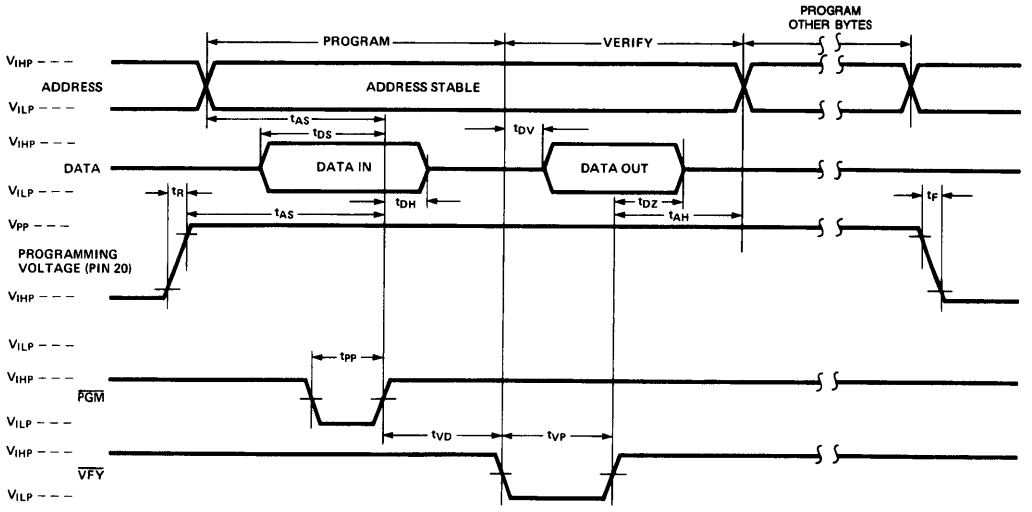
Figure 4. Programming Flowchart

Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 6* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 6* address program and verify one byte of data. Repeat this for each location to be programmed.

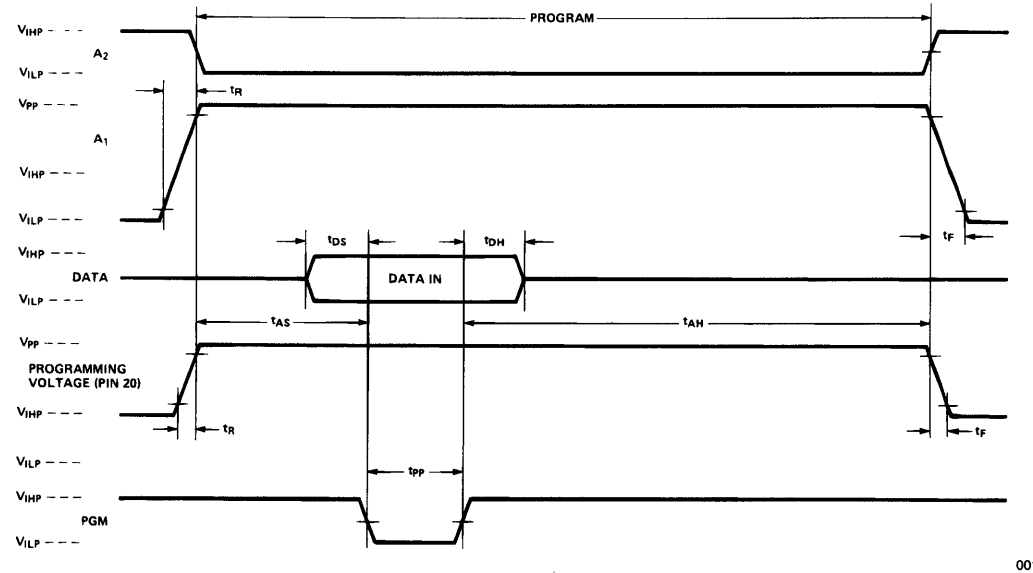
If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.



0016-10

Figure 5. PROM Programming Waveforms



0016-11

Figure 6. Initial Byte Programming Waveforms

Programming the Initial Byte

The CY7C245 registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Programming Synchronous Enable

The CY7C245 provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3, V_{PP} is applied to pin 7 (A_1) with pin 6 (A_2) at V_{IHP}. This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 ($\overline{PGM}$) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

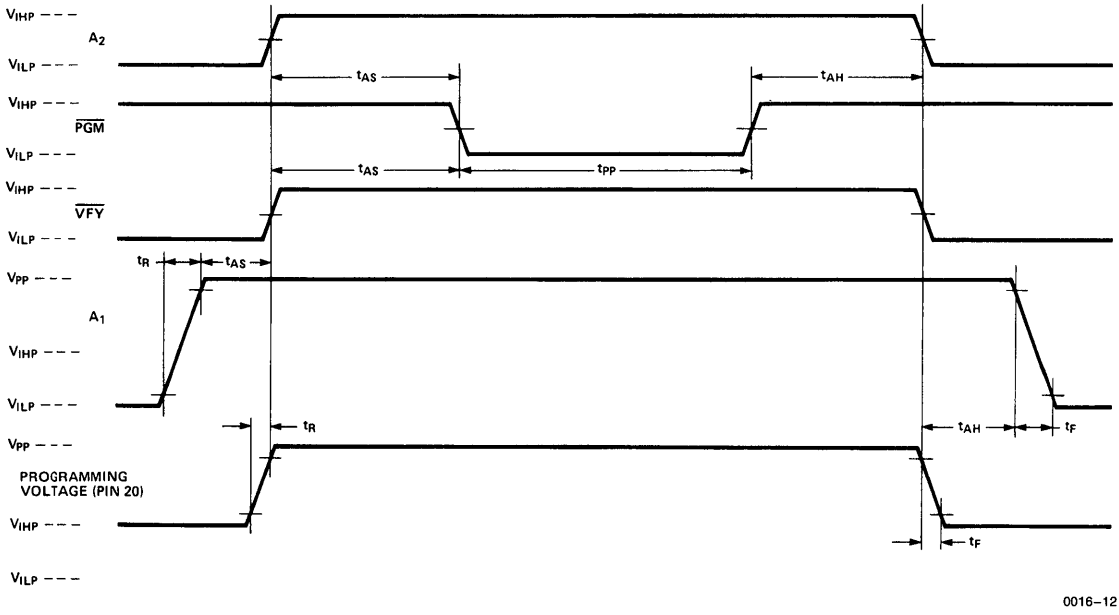


Figure 7. Program Synchronous Enable

Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at V_{IH}, cause clock pin 18 to transition from V_{IL} to V_{IH}. The output should be in a High Z state. Take pin 20, $\overline{ENABLE}$, to V_{IL}. The outputs should remain in a high Z state. Transition the clock from V_{IL} to V_{IH}, the outputs should now contain the data that is present. Again set pin 19 to V_{IH}. The output should remain driven. Clocking pin 18 once more from V_{IL} to V_{IH} should place the outputs again in a High Z state.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
35	15	CY7C245-35PC CY7C245-35DC	P13 D14	Commercial
45	25	CY7C245-45PC CY7C245-45DC CY7C245-45DMB	P13 D14 D14	Commercial Military

CYPRESS SEMICONDUCTOR

CY7C281
CY7C282
1024 x 8 PROM

Features

- **CMOS for optimum speed/ power**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 45 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding > 2000V static discharge**

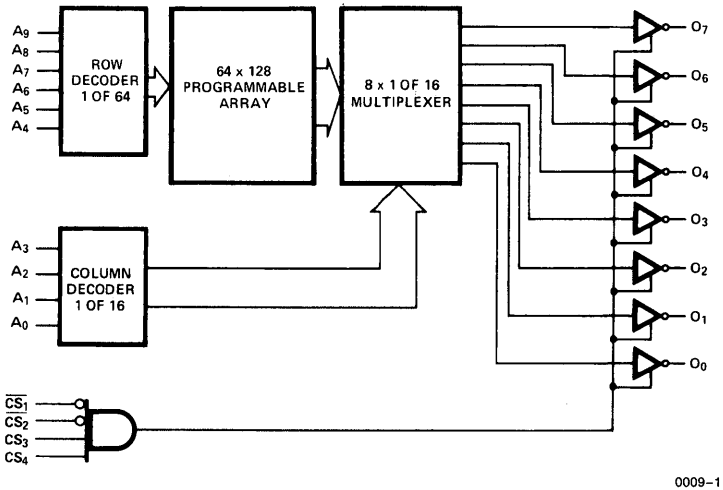
Product Characteristics

The CY7C281 and CY7C282 are high performance 1024 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

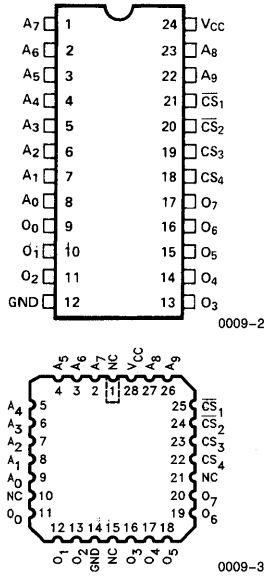
The CY7C281 and CY7C282 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active low signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active high signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0–A_9) will become available on the output lines (O_0–O_7).

Logic Block Diagram



Pin Configurations



Selection Guide

		7C281-30 7C282-30	7C281-45 7C282-45
Maximum Access Time (ns)		30	45
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C281-30 7C282-30		7C281-45 7C282-45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[2]			2.0		2.0		V
V_{IL}	Input LOW Level[2]				0.8		0.8	V
I_{IX}	Input Current	V_{CC} = Max., V_{CC} = GND		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Extended Temperature operation guarenteed with 400 linear feet per minute of air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. The CMOS process does not provide a clamp diode. However, the CY7C281 & CY7C282 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Measured on a sample base.

Switching Characteristics Over the Operating Range[6]

Parameters	Description	CY7C281-30 CY7C282-30		CY7C281-45 CY7C282-45		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z[7]		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		20		25	ns

AC Test Loads and Waveforms

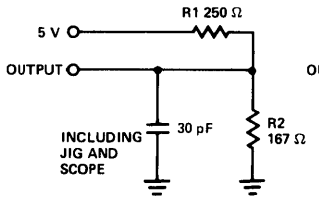


Figure 1a

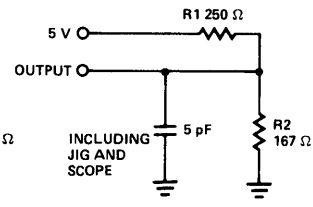


Figure 1b

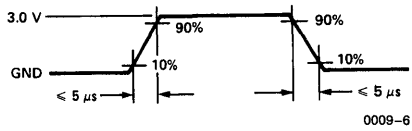
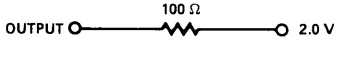
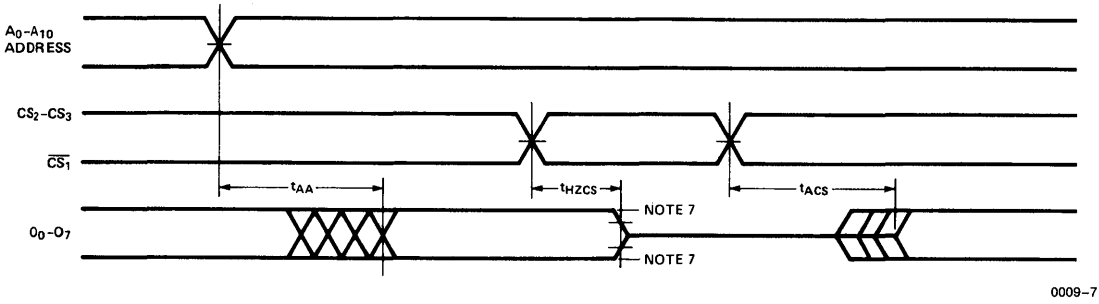


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



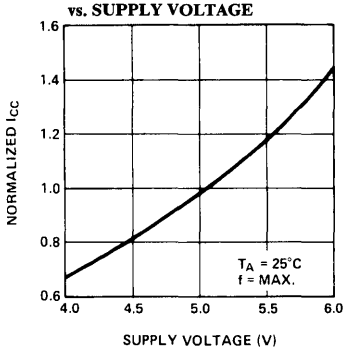


Notes:

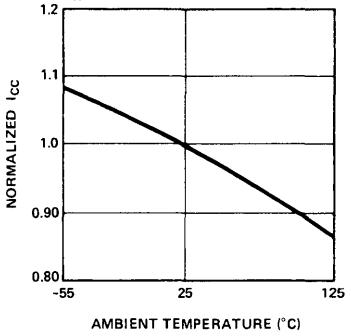
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
7. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level + 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

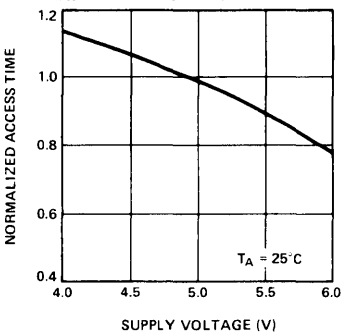
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



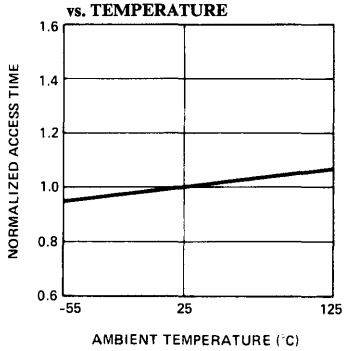
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



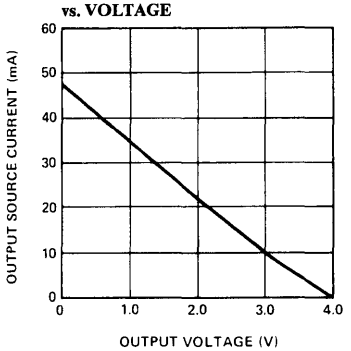
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



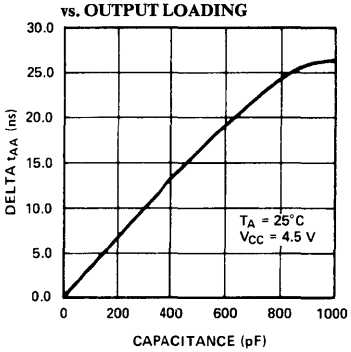
NORMALIZED ACCESS TIME vs. TEMPERATURE



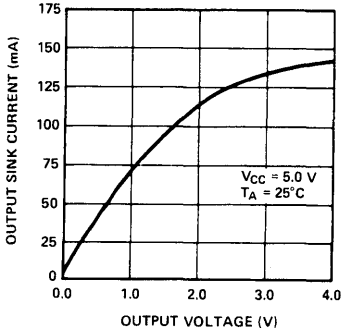
OUTPUT SOURCE CURRENT vs. VOLTAGE



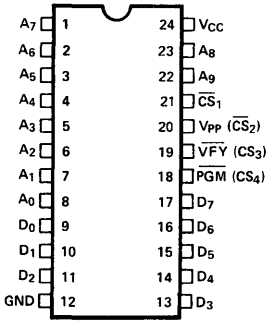
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



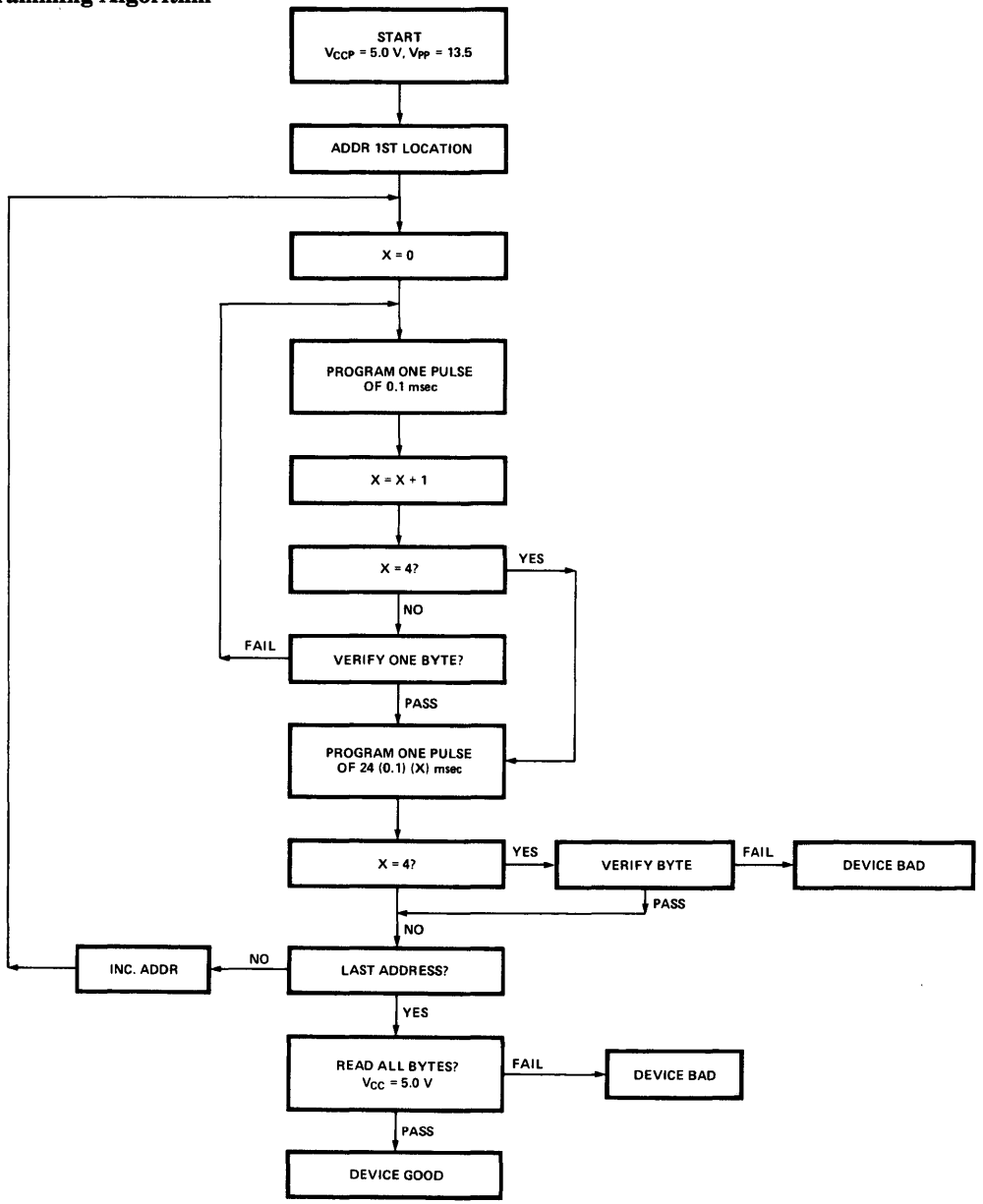
0009-8



0009-9

Figure 3. Programming Pinout

Programming Algorithm



0009-10

The CY7C281 and CY7C282 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CC} = 5.0. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C281 and 7C282 1K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMS are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is neccessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function				Outputs (9–11, 13–17)
	Read or Output Disable	CS_4	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS}_1$	
	Pin Number	(18)	(19)	(20)	(21)	
Read		V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	X	High Z
Output Disable[4]		X	V_{IL}	X	X	High Z
Output Disable[4]		V_{IL}	X	X	X	High Z
Output Disable[4]		X	X	X	V_{IH}	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	Zeros

Notes:

4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 1K x 8

Power the device for normal read mode operation with pin 18, 19, 20, and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Tables 3 and 4. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 × the sum of the previous programming pulses before advancing to the next address to repeat the process.

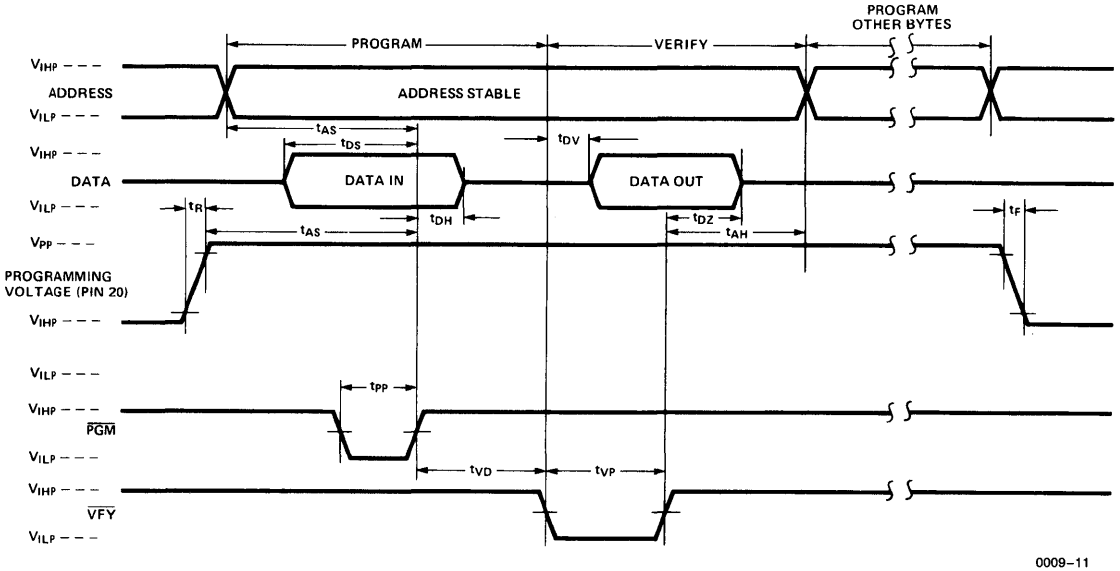


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30 ns	CY7C281-30PC	P13	Commercial
	CY7C282-30PC	P11	
	CY7C281-30DC	D14	
	CY7C281-30LC	L64	
	CY7C282-30DC	D12	
45 ns	CY7C281-45PC	P13	Commercial
	CY7C282-45PC	P11	
	CY7C281-45DC	D14	
	CY7C281-45LC	L64	
	CY7C282-45DC	D12	
45 ns	CY7C281-45DMB	D14	Military
	CY7C281-45LMB	L64	
	CY7C282-45DMB	D12	

CYPRESS SEMICONDUCTOR

CY7C291
CY7C292
2048 x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns (commercial)**
  - **— 50 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

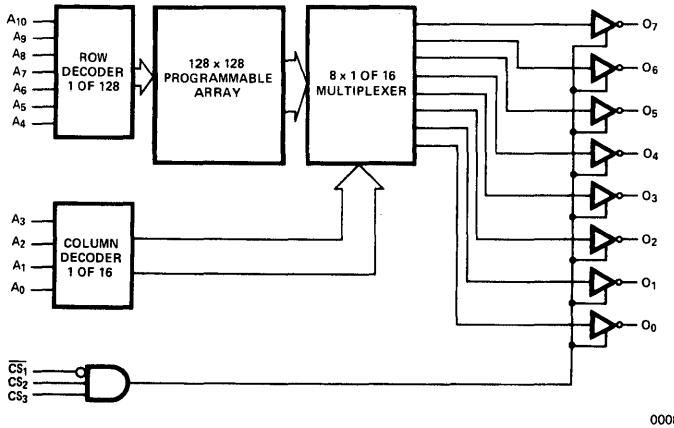
Product Characteristics

The CY7C291 and CY7C292 are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



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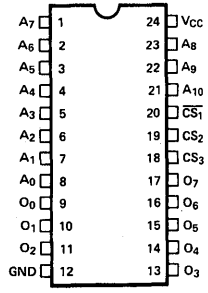
Pin Configurations



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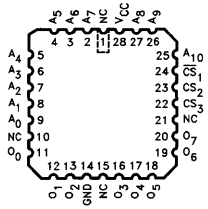

0008–3

Selection Guide

		7C291-35 7C292-35	7C291-50 7C292-50
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C291-35 7C292-35		7C291-50 7C292-50		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[2]			2.0		2.0		V
V_{IL}	Input LOW Level[2]				0.8		0.8	V
I_{IX}	Input Current	V_{CC} = Max., V_{CC} = GND		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. The CMOS process does not provide a clamp diode. However, the CY7C291 & CY7C292 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Measured on a sample basis.

3

Switching Characteristics Over the Operating Range[6]

Parameters	Description	CY7C291-35 CY7C292-35		CY7C291-50 CY7C292-50		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		35		50	ns
t_{HZCS}	Chip Select Inactive to High Z[7]		25		25	ns
t_{ACS}	Chip Select Active to Output Valid		25		25	ns

AC Test Loads and Waveforms

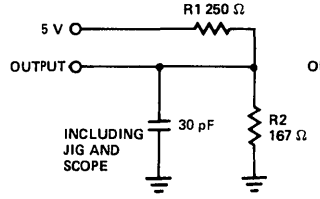

Figure 1a

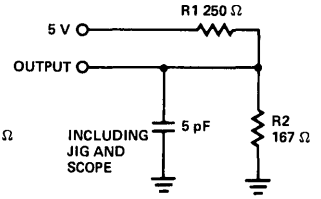

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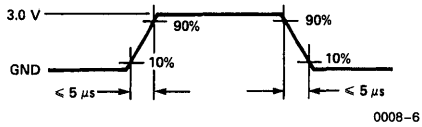
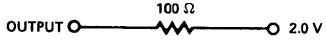
Figure 1b



0008-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



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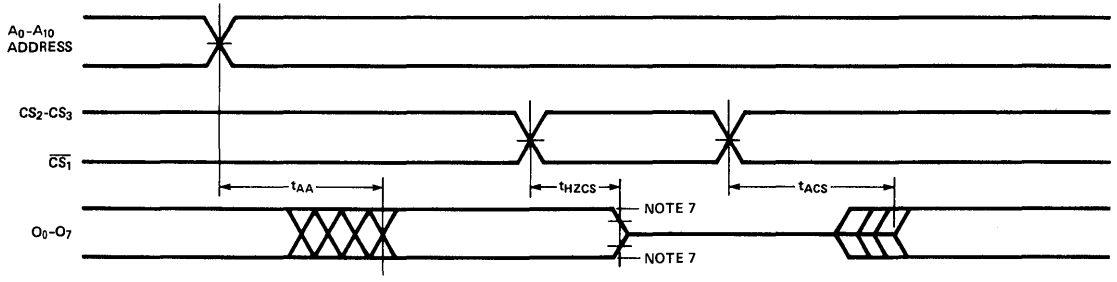


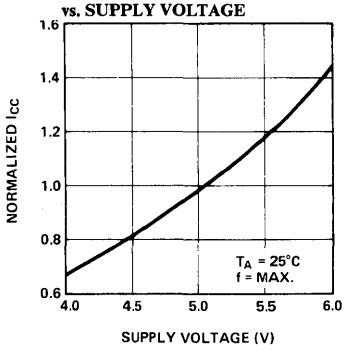
0008-7

Notes:

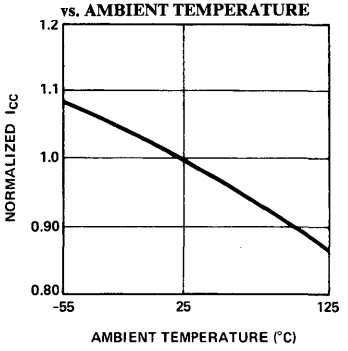
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figures 1a, 1b.*
7. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

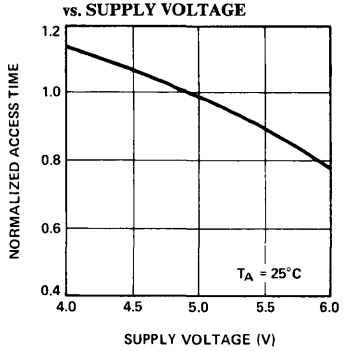
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



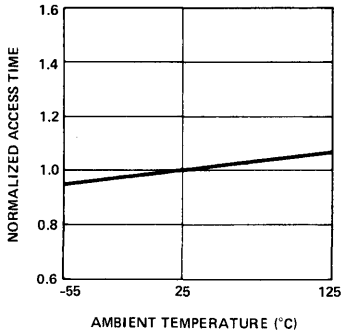
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



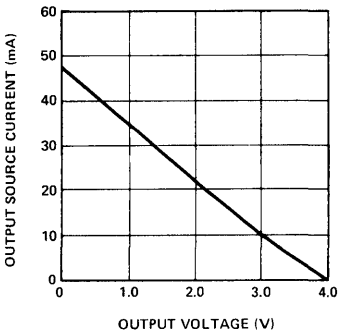
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



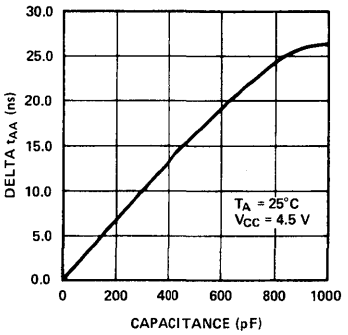
NORMALIZED ACCESS TIME vs. TEMPERATURE



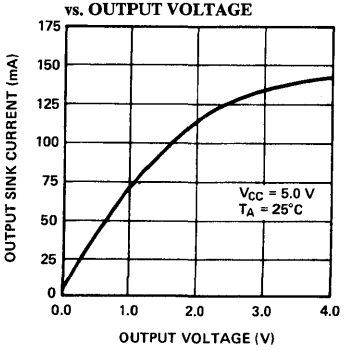
OUTPUT SOURCE CURRENT vs. VOLTAGE



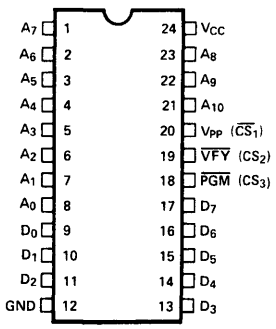
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



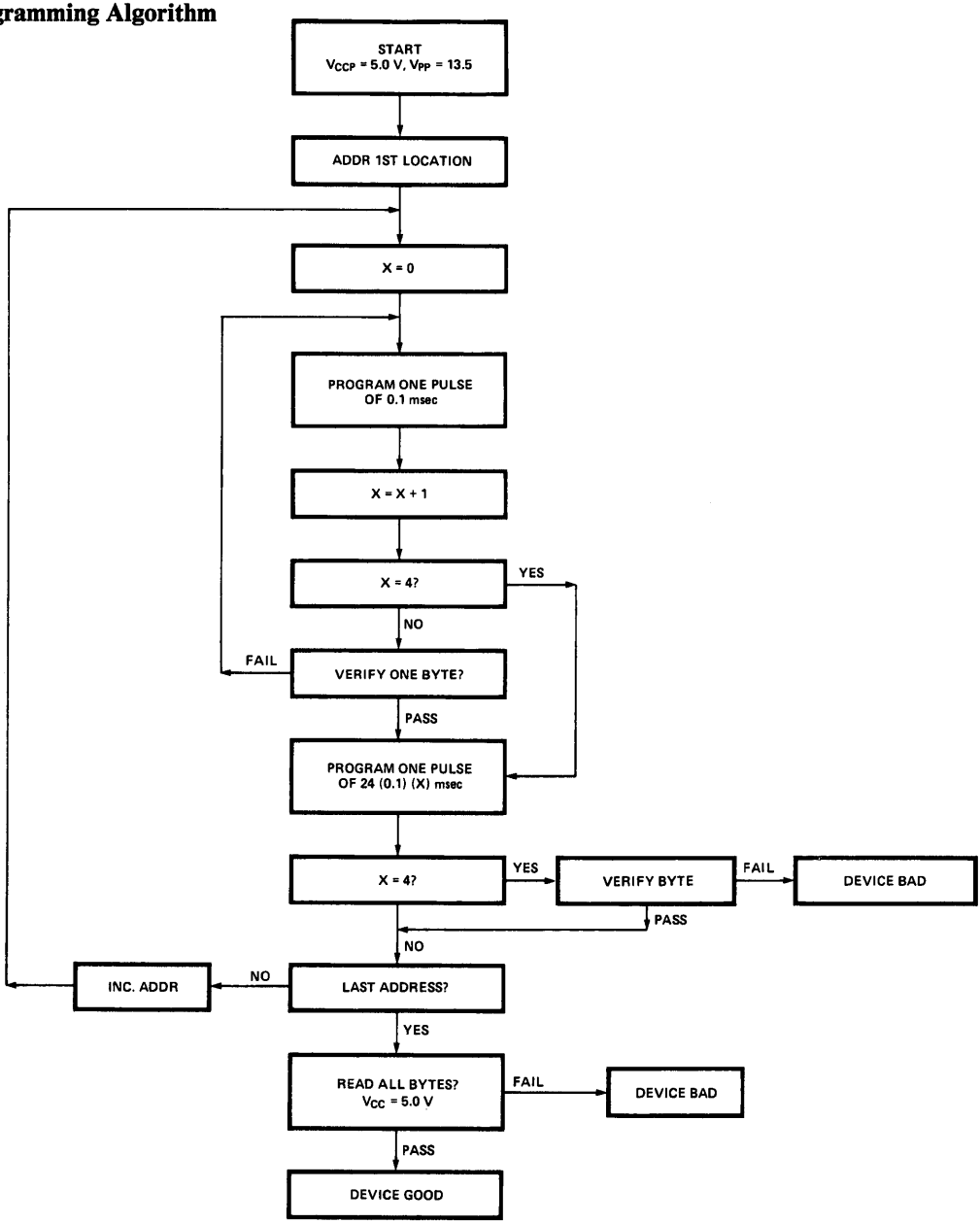
0008–8



0008–9

Figure 3. Programming Pinout

Programming Algorithm



0008-10

The CY7C291 and CY7C292 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C291 and 7C292 2K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

3

Mode Selection

Table 3

Mode		Pin Function			Outputs (9–11, 13–17)
	Read or Output Disable	CS_3	CS_2	$\overline{CS_1}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	
	Pin Number	(18)	(19)	(20)	
Read		V_{IH}	V_{IH}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	High Z
Output Disable[4]		X	V_{IL}	X	High Z
Output Disable[4]		V_{IL}	X	X	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	Zeros

Notes:

4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

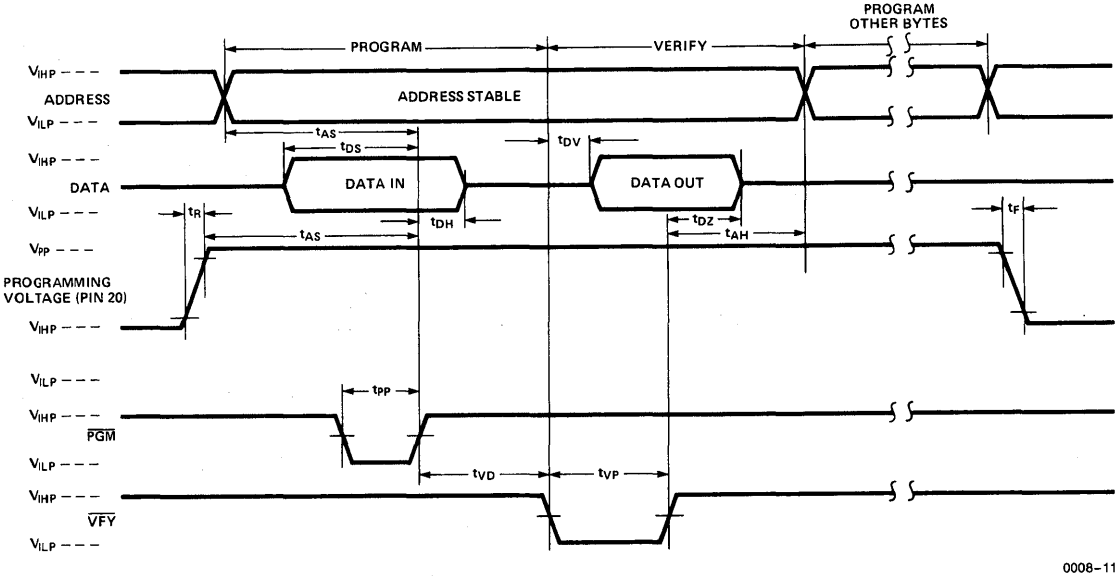


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35 ns	CY7C291-35PC CY7C292-35PC CY7C291-35DC CY7C291-35LC CY7C292-35DC	P13 P11 D14 L64 D12	Commercial
50 ns	CY7C291-50PC CY7C292-50PC CY7C291-50DC CY7C291-50LC CY7C292-50DC	P13 P11 D14 L64 D12	Commercial
50 ns	CY7C291-50DMB CY7C291-50LMB CY7C292-50DMB	D14 L64 D12	Military

PROM Programming Information

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970's and continue to provide the highest speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a Programming System. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance are easily identified. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the early 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point-of-view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of devices that program every time, and will perform as specified when programmed.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor, biasing it off.

Differential Memory Cells

A second area that high speed CMOS PROM design technology differs from conventional high density EPROM designs is in the area of differential cell/differential sensing versus single ended cell/differential sensing with a dummy cell.

In a conventional high density EPROM a single EPROM transistor is used to switch the input to one side of a differential sense amplifier. The other side of the sense amplifier is biased at an intermediate level with a dummy cell. An unprogrammed EPROM transistor will conduct and drive the sense amplifier to a logic "0". A programmed EPROM transistor will not conduct, and consequently drives the sense amplifier to a logic "1". A conventional EPROM cell therefore is delivered with a specific state "0" or "1" in it depending on the number of inversions after the sense amplifier and can always be programmed to the opposite state. Access time in this conventional approach is heavily dependent on the time the selected EPROM transistor takes to move the input of the sense amplifier from a quiescent condition to the threshold that the dummy cell is biasing the second input to the sense amplifier. This bias is several volts, and requires a significant delay before the sense amplifier begins to react.

Cypress PROMs employ a true differential cell approach, with EPROM cells attached to both inputs of the sense amplifier. As indicated above, the read transistor which is optimized for speed is actually the transistor attached to the sense amplifier. In the erased state, both EPROM transistors conduct when selected eccentrically biasing the input of the sense amplifier at the same level. If the inputs were at identical levels, the output of the sense amplifier would be in a mestastable condition or, neither a "1" nor "0". In actual practice the natural bias and high gain of the sense amplifier combine to cause the output to favor one or the other stable conditions. The difference between the two conditions is however only a few millivolts and the memory cell should be considered to contain neither a "1" nor a "0". As a result of this design approach, the memory cell must be programmed to either a "1" or a "0" depending on the desired condition and the conventional BLANK CHECK mechanism is invalid. The benefit of the approach however is that only a small differential signal from the cell begins the sense amplifier switching and the access time of the memory is extremely fast.

Programming Algorithim

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data out pins during the programming operation and the data is read from these same pins for verification that the byte has been programmed.

Blank Check

Since a differential cell contains neither a "1" nor a "0" before it is programmed, the conventional BLANK CHECK is not valid. For this reason, all Cypress CMOS PROMs contain a special BLANK CHECK mode of operation. Blank check is performed by separately examining the "0" and "1" sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes one comparing the "0" side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier and then repeating this operation for the "1"s side of the cell. The modes are called BLANK CHECK ONES, and BLANK CHECK ZEROS. These modes are entered by the application of a supervoltage to the device.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ and a WRITE pin in the programming mode. These are active low signals and cause the data on the output pins to be written into the addressed memory location in the case of the WRITE signal or read out of the device in the case of the READ signal. When both the READ and WRITE signals are high, the outputs are disabled and in a high impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the WRITE signal. Verification of data is accomplished by reading the information on the output pins while the READ signal is active.

The timing for actual programming is supplied in the unique programming specification for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable INITIAL BYTE and Programmable SYNCHRONOUS/ASYNCHRONOUS ENABLE available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner, using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

Programming Support

Programming support for Cypress CMOS PROMs is available from a number of programmer manufacturers some of which are listed below.

Data I/O
Programmer Model 29
Unipak II

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444

Stag
Programmer PPZ

Stag Microsystems
528-5 Weddell Dr.
Sunnyvale, CA 94089
(408) 745-1991

Sunrise Systems
Programmer Model Z-1000 B

Sunrise Systems
524 S. Vermont
Glendora, CA 91740
(818) 914-1926

Wavetek Digilec
Programmer Model 803

Wavetek Digilec
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089
(408) 745-0722

CYPRESS SEMICONDUCTOR

Section Contents

PALs (Programmable Array Logic)

Introduction to PALs

Cypress PAL Family Features

Cypress Semiconductor's PAL® family offers the user the next generation in Programmable Array Logic (PAL) devices that are based on our high performance 1.2μ CMOS process. These devices offer the user the power saving of a CMOS-based process, with delay times equivalent to those previously found only in bipolar devices. No fuses are used in Cypress' PAL family, rather all devices are based on an EPROM cell to facilitate programming. By using an EPROM cell instead of fuses, programming yields of 100% can be expected since all devices are functionally tested and erased prior to packaging. Therefore, no programming yield loss can be expected by the user.

The EPROM cell used by Cypress serves the same purpose as the fuse used in most bipolar PAL devices. Before programming, the AND gates or Product Terms are connected via the EPROM cells to both the true and complement inputs. When the EPROM cell is programmed, the inputs from a gate or Product Term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or Product Terms. This is similar to "blowing" the fuses of a bipolar device which disconnects the input gate from the Product Term. Selective programming of each of these EPROM cells enables the specific logic function to be implemented by the user.

The programmability of Cypress' PALs allows the user to customize every device in a number of ways to implement their unique logic requirements. Using PALs in place of SSI or MSI components results in more effective utilization of boardspace, reduced cost and increased reliability. The flexibility afforded by these PALs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The PAL family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output and product terms to the desired application.

PAL Notation

To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In *Figure 1*, an "x" represents an unprogrammed EPROM cell that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in *Figure 2* which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in *Figure 3*.

PAL® is a registered trademark of Monolithic Memories, Inc.

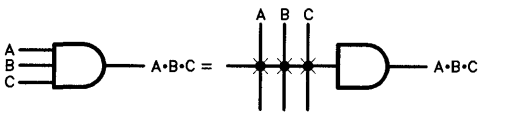


Figure 1

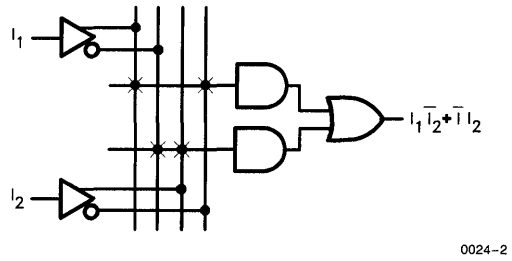


Figure 2

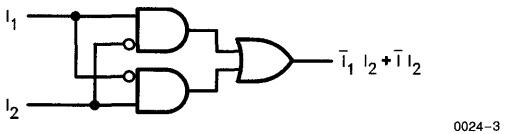


Figure 3

4

PAL Circuit Configurations

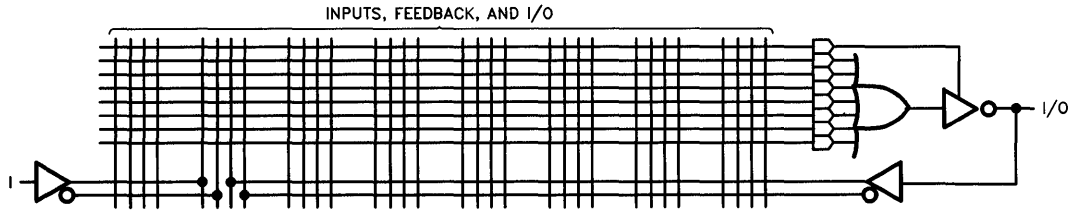
Cypress PALs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows the designer to select a PAL that best fits the needs of their application. An example of some of the configurations that are available are listed below.

Programmable I/O

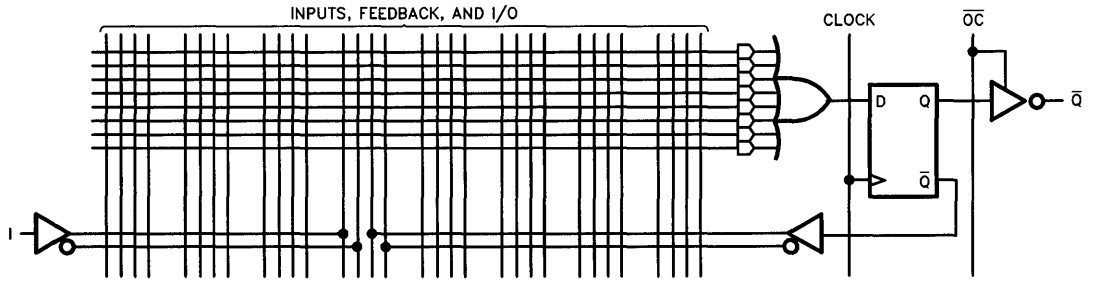
The programmable I/O offered in the Cypress PAL family allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PAL as an input to the array. This programmable I/O feature allows the PAL to drive the output pin when the three-state output is enabled or, the I/O pin can be used as an input to the array when the three-state output is disabled.

Registered Outputs with Feedback

The registered output offered on a number of the Cypress PALs allows this circuit to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PAL to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift and branch.



0024-4



0024-5

CYPRESS SEMICONDUCTOR

PAL 20A Series, PAL 20A-2 Series

16R8A, 16R6A, 16R4A, 16L8A, 16R8A-2, 16R6A-2, 16R4A-2, 16L8A-2

Features

- **Fast**
  - **— A Series: t_{PD} = 25 ns, t_{CO} = 15 ns, t_S = 20 ns max.**
  - **— A-2 Series: t_{PD} = 35 ns, t_{CO} = 25 ns, t_S = 30 ns max.**
- **Low power**
  - **— I_{CC} max.: 90 mA, A-2 series**
  - **— I_{CC} max.: 135 mA, A Series**
- **Commercial and military temperature range**
- **Low cost solution**
  - **— Faster design cycle**
  - **— Reduces board space/chip count**
  - **— Highly flexible design tool**
- **Highly reliable**
  - **— Uses proven EPROM technology**
  - **— Fully AC and DC tested**
  - **— Security feature prevents logic pattern duplication**
  - **— >2000V input protection for electrostatic discharge**
  - **— ±10% power supply voltage and higher noise immunity**

Functional Description

Cypress PAL® devices are high speed electrically programmable logic elements. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PAL Series 20 family uses an advanced 1.2 micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PAL device.

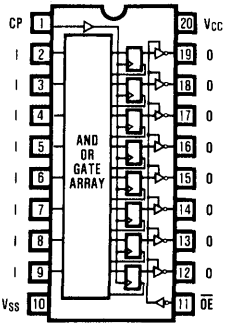
Cypress Pal devices are implemented with a sum-of-products (AND-OR) architecture. The Cypress PAL 20 family provides variable I/O configurations (the 16R4, 16R6 and 16R8) with either 4, 6, or 8 registered outputs with feedback. The purely combinatorial member is the 16L8.

The entire PAL family can be programmed on inexpensive conventional PROM/EPROM programmers with appropriate personality or socket adapters. Once the PAL device is programmed, one additional location can be programmed to prohibit logic pattern verification. This feature gives the user additional protection to safeguard his proprietary logic. This feature is highly reliable and due to EPROM technology makes it impossible to visually read the programmed cell locations.

PAL® is a registered trademark of Monolithic Memories Inc.

Logic Symbol and Pinout

16R8A/16R8A-2



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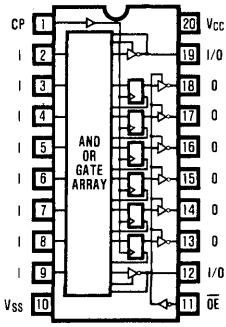
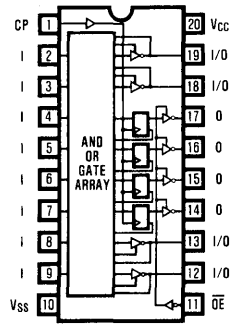
16R6A/16R6A-2



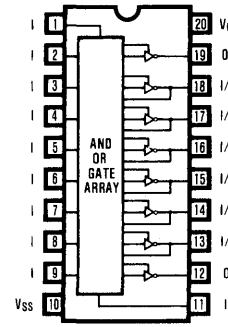
0010-2

16R4A/16R4A-2



0010-3

16L8A/16L8A-2



0010-4

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PAL Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC}	t_{PD} ns		t_S ns		t_{CO} ns	
				mA	COM	MIL	COM	MIL	COM	MIL
16L8A	(8) 7-wide AND-OR-Invert	Programmable	(6)Bidirectional (2) Dedicated	135	25	30	—	—	—	—
16R8A	(8) 8-wide AND-OR	Dedicated	Registered Inverting	135	—	—	20	25	15	20
16R6A	(6) 8-wide AND-OR	Dedicated	Registered Inverting	135	25	30	20	25	15	20
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional							
16R4A	(4) 8-wide AND-OR	Dedicated	Registered Inverting	135	25	30	20	25	15	20
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional							
16L8A-2	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	90	35	40	—	—	—	—
16R8A-2	(8) 8-wide AND-OR	Dedicated	Registered Inverted	90	—	—	30	35	25	25
16R6A-2	(6) 8-wide AND-OR	Dedicated	Registered Inverting	90	35	40	30	35	25	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional							
16R4A-2	(4) 8-wide AND-OR	Dedicated	Registered Inverting	90	35	40	30	35	25	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional							

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 24 mA

DC Programming Voltage 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[6]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[2] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[2] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$[1]			−10	10	μA
V_{PP}		Programming Voltage @ I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA	A Series			135	mA
			A-2 Series			90	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	μA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	4	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	7	

Switching Characteristics Over Operating Range[5]

HIGH SPEED PAL 20A SERIES

Parameters	Description	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		15		20	ns
t_S	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A	0		0		ns
t_P	Clock Period	35		45		ns
t_W	Clock Width	15		20		ns
f_{MAX}	Maximum Frequency		28.5		22	MHz

Switching Characteristics Over Operating Range[5]

STANDARD SPEED PAL 20A-2 SERIES

Parameters	Description	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		35		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		35		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4		35		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		25		25	ns
t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	30		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		ns
t_P	Clock Period	55		60		ns
t_W	Clock Width	20		25		ns
f_{MAX}	Maximum Frequency		18		16.5	MHz

4

Notes:

1. I_{IX} (Pin 1) = 25 μA Max., $V_{SS} \le V_{IN} \le 2.7V$. I_{IX} (Pin 1) = 1 mA Max., $2.7V \le V_{IN} \le V_{CC}$.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.
5. *Figure 1a* test load use for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
6. Extended temperature operation guaranteed with 400 linear feet per minute air flow.

AC Test Loads and Waveforms (Commercial)

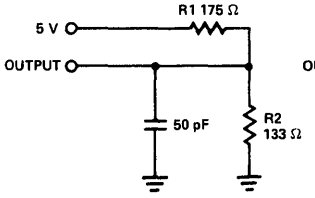
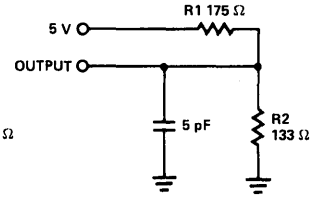


Figure 1a



0010-5

Figure 1b

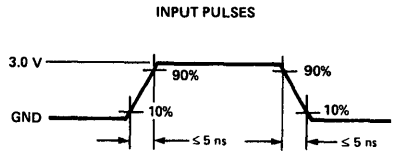
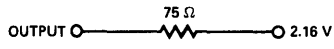


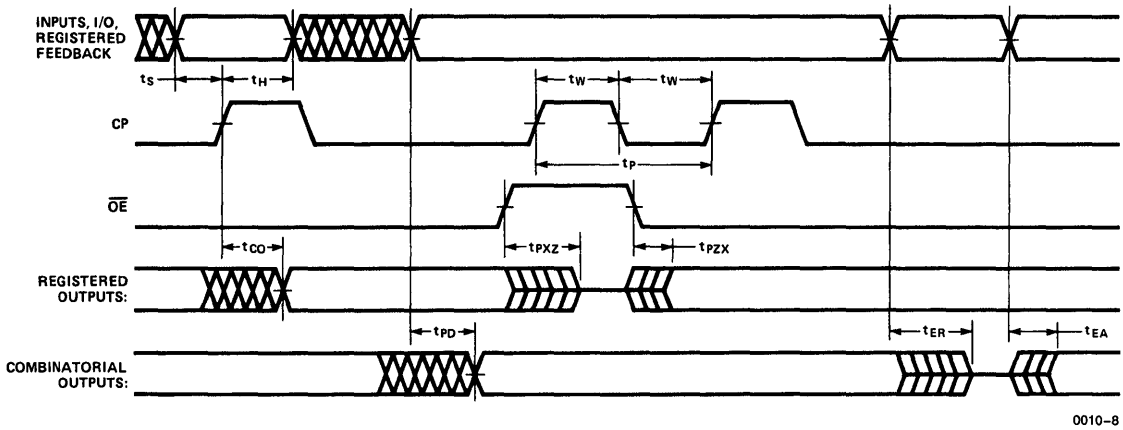
Figure 2

Equivalent to: THÉVENIN EQUIVALENT

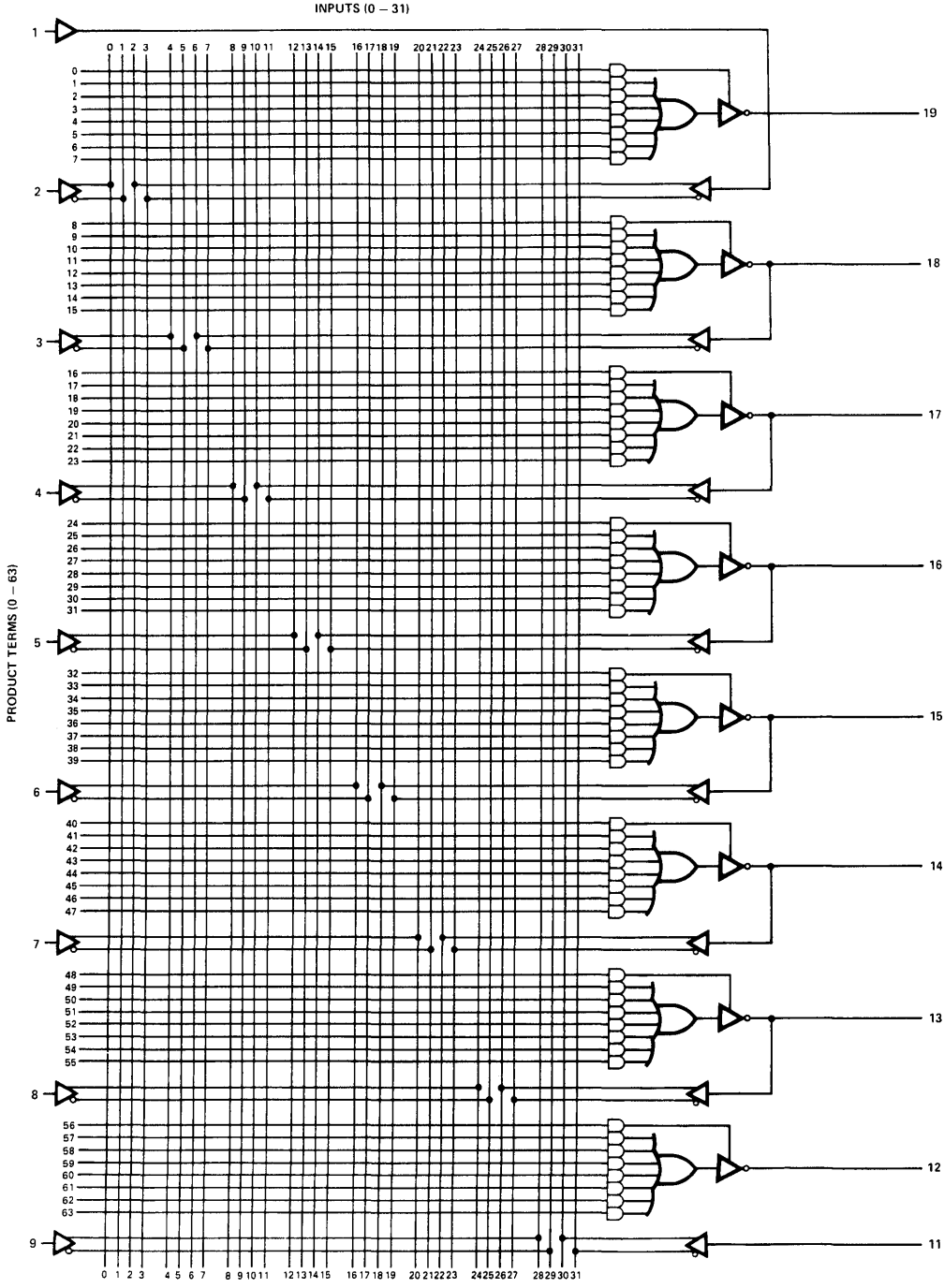


0010-6

Switching Waveforms

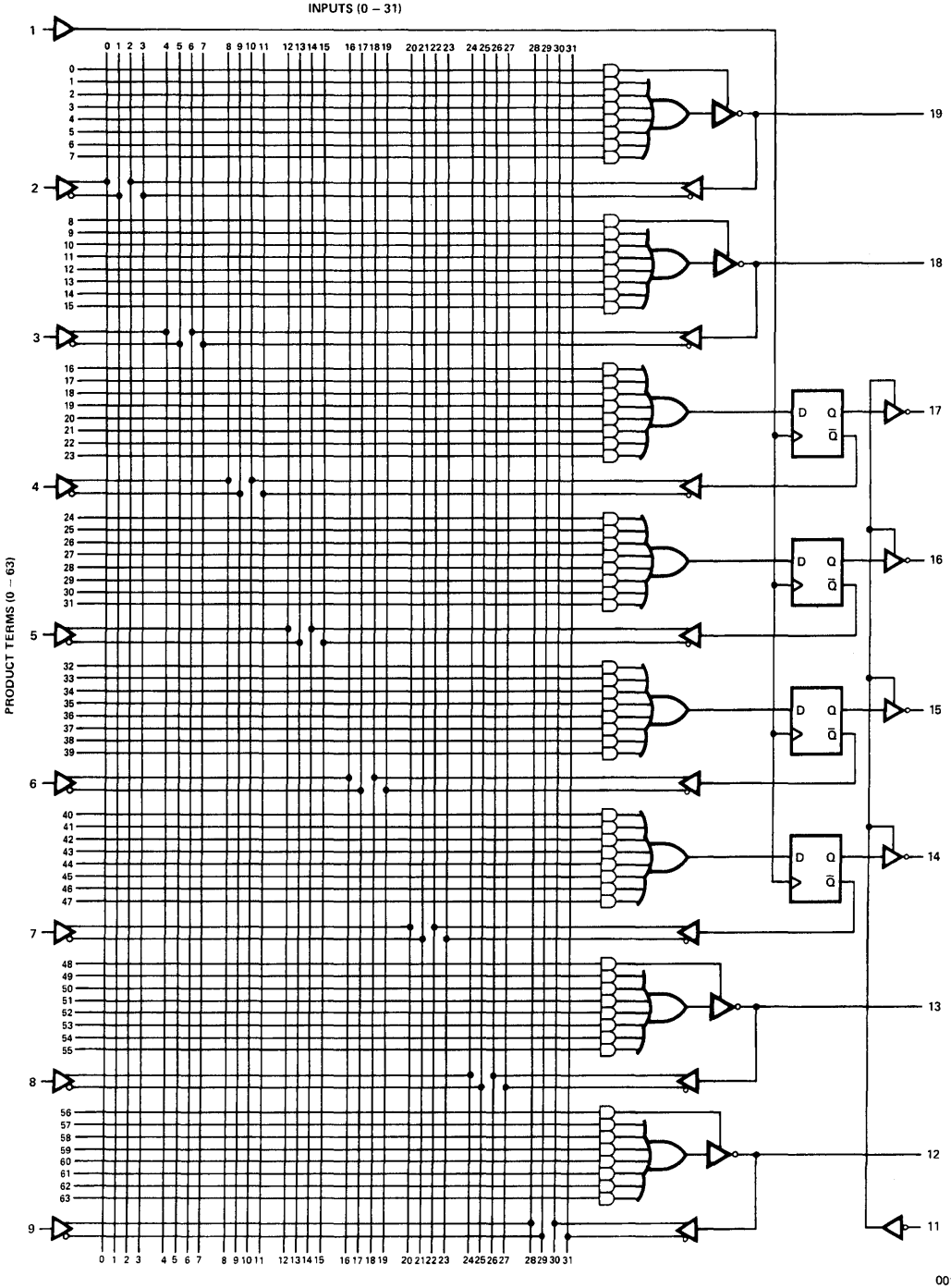


Logic Diagram PAL 16L8A, 16L8A-2



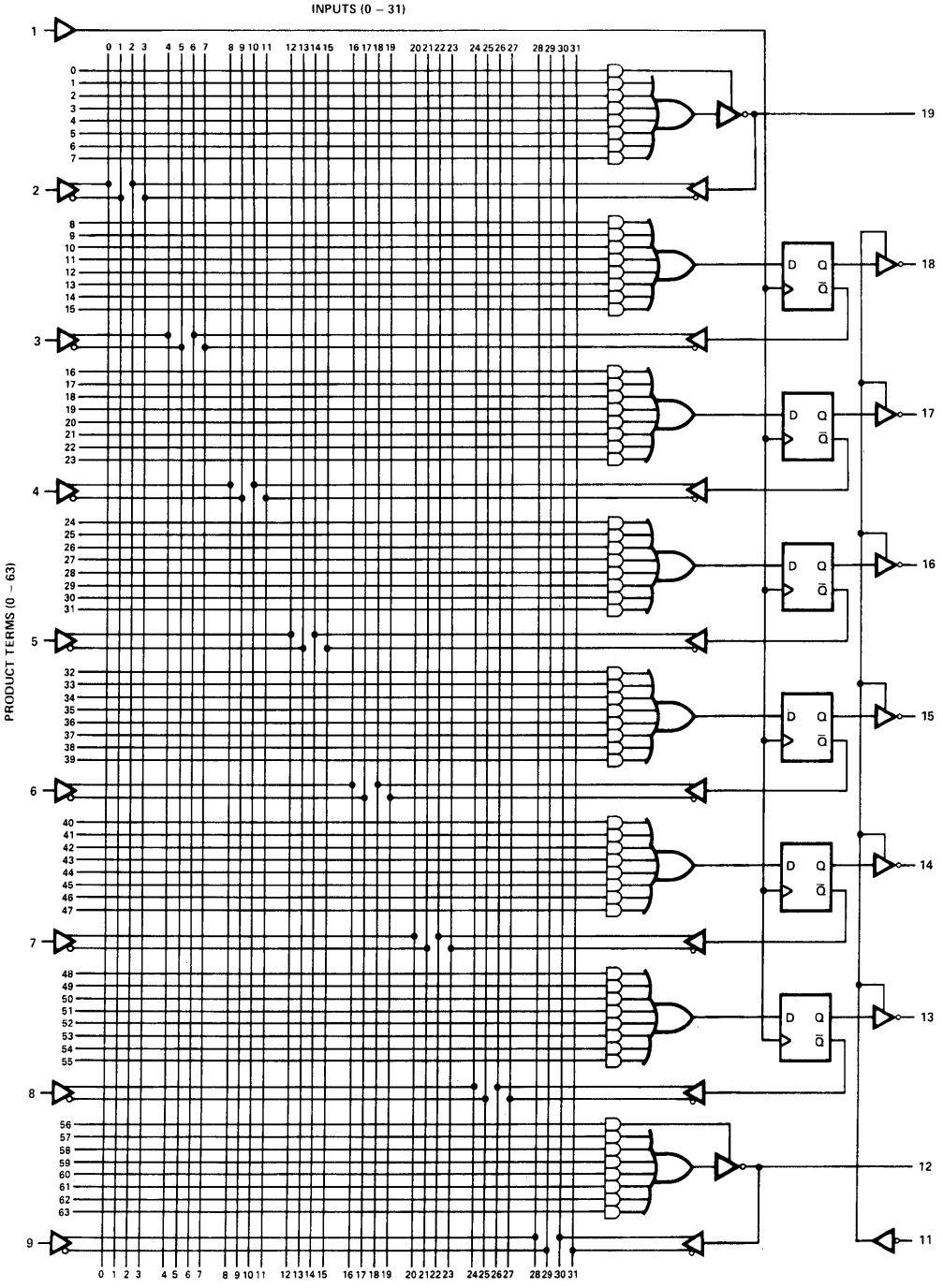
0010-9

Logic Diagram PAL 16R4A, 16R4A-2



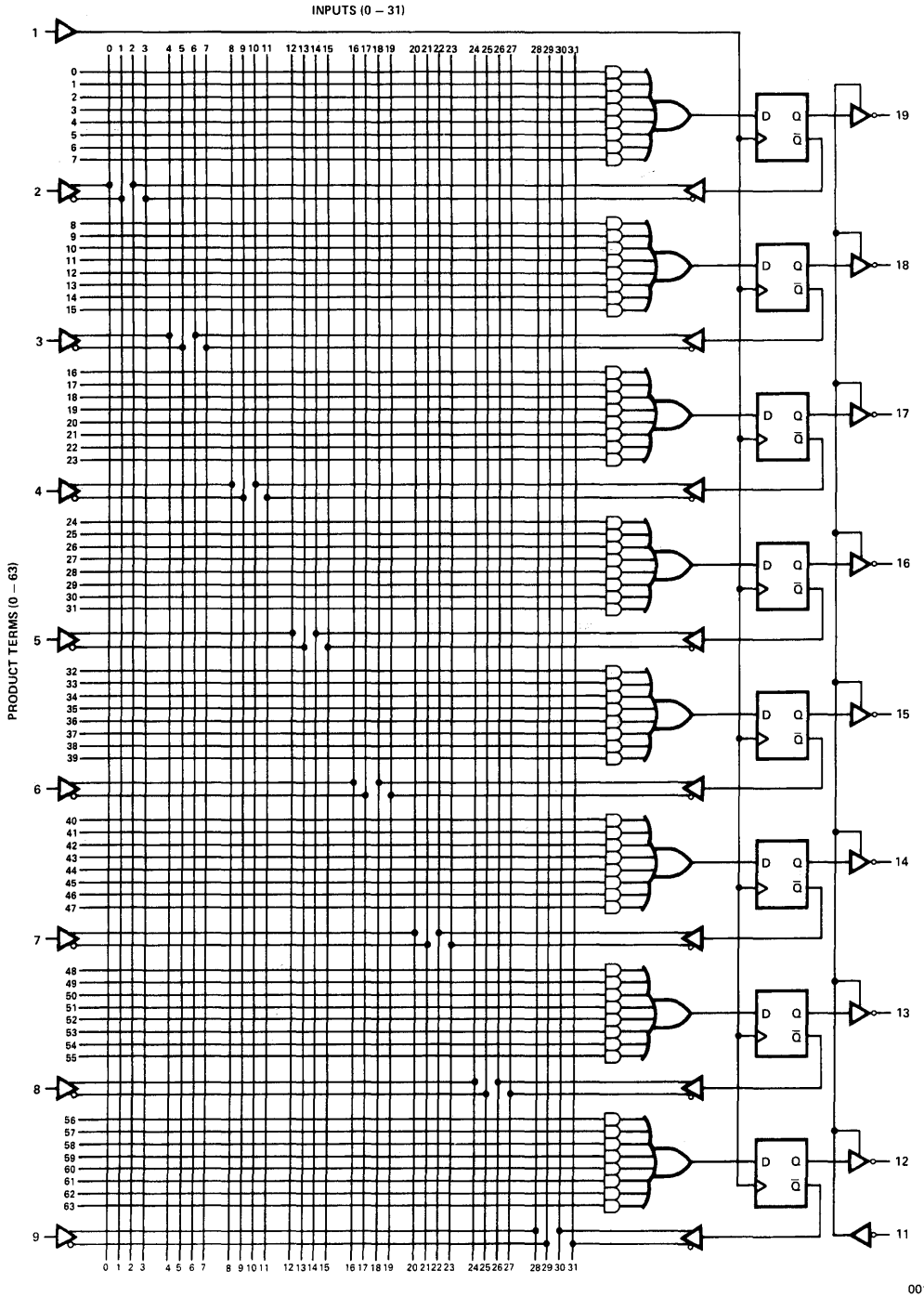
0010-10

Logic Diagram PAL 16R6A, 16R6A-2



0010-11

Logic Diagram PAL 16R8A, 16R8A-2



0010-12

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
135	25	—	—	PAL 16L8A PC	P5	Commercial
135	25	—	—	PAL 16L8A DC	D6	Commercial
135	30	—	—	PAL 16L8A DMB	D6	Military
135	—	20	15	PAL 16R8A PC	P5	Commercial
135	—	20	15	PAL 16R8A DC	D6	Commercial
135	—	25	20	PAL 16R8A DMB	D6	Military
135	25	20	15	PAL 16R6A PC	P5	Commercial
135	25	20	15	PAL 16R6A DC	D6	Commercial
135	30	25	20	PAL 16R6A DMB	D6	Military
135	25	20	15	PAL 16R4A PC	P5	Commercial
135	25	20	15	PAL 16R4A DC	D6	Commercial
135	30	25	20	PAL 16R4A DMB	D6	Military
90	35	—	—	PAL 16L8A-2PC	P5	Commercial
90	35	—	—	PAL 16L8A-2DC	D6	Commercial
90	40	—	—	PAL 16L8A-2DMB	D6	Military
90	—	30	25	PAL 16R8A-2PC	P5	Commercial
90	—	30	25	PAL 16R8A-2DC	D6	Commercial
90	—	35	25	PAL 16R8A-2DMB	D6	Military
90	35	30	25	PAL 16R6A-2PC	P5	Commercial
90	35	30	25	PAL 16R6A-2DC	D6	Commercial
90	40	35	25	PAL 16R6A-2DMB	D6	Military
90	35	30	25	PAL 16R4A-2PC	P5	Commercial
90	35	30	25	PAL 16R4A-2DC	D6	Commercial
90	40	35	25	PAL 16R4A-2DMB	D6	Military

CYPRESS SEMICONDUCTOR

CMOS PAL® C16R8A, PAL C16R6A, PAL C16R4A, PAL C16L8A

Features

- **"A" performance at A-2 power**
  - **— t_{PD} = 25 ns max**
  - **— t_S = 20 ns max**
  - **— t_{CO} = 15 ns max**
- **Commercial and military temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >2000V input protection from electrostatic discharge**
  - **— 100% AC/DC tested**
  - **— 10% power supply tolerances**
  - **— High noise immunity**
  - **— Security feature prevents pattern duplication**
  - **— 100% programming and functional testing**

Functional Description

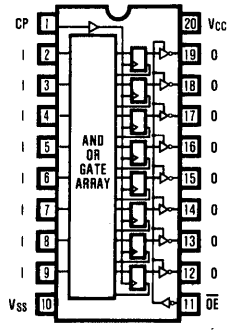
Cypress PAL C Series 20 devices are high speed electrically programmable logic devices produced in a proprietary "N" well CMOS EPROM process. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions serving unique requirements.

Before programming, AND gates or PRODUCT TERMS are connected via EPROM cells to both the TRUE and COMPLEMENT inputs. Programming an EPROM cell disconnects an INPUT TERM from a PRODUCT TERM. Selective programming of these cells allows a specific logic function to be implemented in a PAL C device. PAL C devices are supplied in four functional configurations, designated 16L8, 16R8, 16R6 and 16R4 at "A" level performance and "A-2" power as detailed in the balance of this specification. These devices have potentially 16 inputs and 8 outputs as configured by the user. Output configurations of 8 registers, 8 combinatorial, 6 registered and 2 combinatorial as well as 4 registered and 4 combinatorial are provided by the four functional variations of the product family.

All PAL C devices feature a SECURITY function which provides the user protection for the implementation of

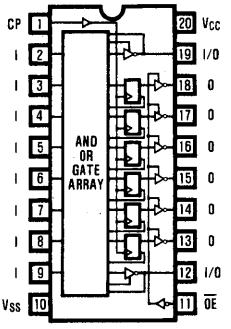
Logic Symbols and Pinouts

16R8A



0038-1

16R6A



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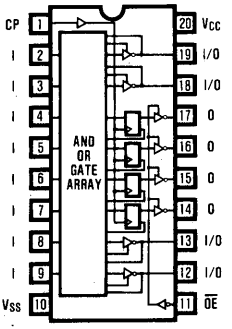
16R4A



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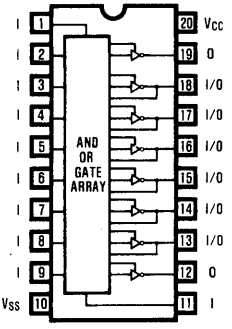
16RL8A



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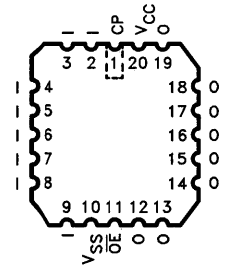

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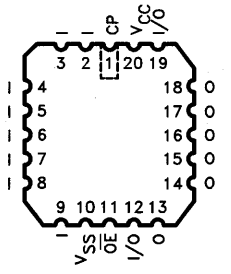
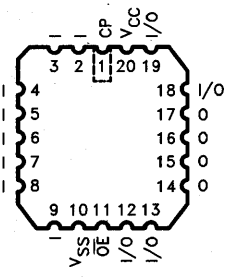
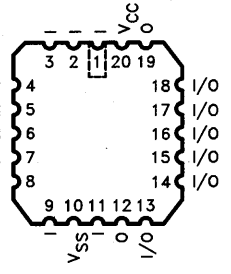


0038-6



0038-7



0038-8

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CYPRESS SEMICONDUCTOR is a trademark of Cypress Semiconductor Corporation.

Functional Description (Continued)

proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope. The PAL C device also contains a PHANTOM ARRAY used for functional and performance testing. The content of this array is always accessible, even when security is invoked.

Cypress PAL C products are produced in an advanced 1.2 micron "N" well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. The PHANTOM ARRAY and PHANTOM operating mode allow the device to be tested for functionality and performance after it has been packaged. Combining these inherent and designed-in features, an extremely high degree of functionality, programmability and assured AC performance are provided and testing becomes an easy task.

The REGISTER PRELOAD allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

The PHANTOM MODE of operation provides a completely separate operating mode where the functionality of the device along with its AC performance may be ascertained. The user need not be encumbered by programmed cells in the normal operating mode. This PHANTOM MODE of operation allows additional input lines to be programmed to operate the PAL C device, exercising the device functionally and allowing AC performance measurements to be made. The PHANTOM MODE of operation acknowledges only the INPUT TERMS shown shaded in the functional block diagrams. Likewise, the normal PHANTOM INPUT TERMS do not exist in the normal mode of operation. During the final stages of manufacturing, some cells in the PHANTOM ARRAY are programmed for final AC and functional testing. These cells remain programmed, and may be used at incoming inspection to verify both functional and AC performance.

PAL C Device Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} mA		t_{PD} ns		t_S ns		t_{CO} ns	
				COM	MIL	COM	MIL	COM	MIL	COM	MIL
16L8A	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	90	90	25	30	—	—	—	—
16R8A	(8) 8-wide AND-OR	Dedicated	Registered Inverting	90	90	—	—	20	25	15	20
16R6A	(6) 8-wide AND-OR	Dedicated	Registered Inverting	90	90	25	30	20	25	15	20
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4A	(4) 8-wide AND-OR	Dedicated	Registered Inverting	90	90	25	30	20	25	15	20
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 24 mA

DC Programming Voltage 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[6]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logic HIGH[2] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[2] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$[1]			−10	10	μA
V_{PP}		Programming Voltage @ I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA				90	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$			−100	100	μA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	4	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	7	

Switching Characteristics Over Operating Range[5]

High Speed PAL C 20A Series

Parameters	Description	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		15		20	ns
t_S	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A	0		0		ns
t_P	Clock Period	35		45		ns
t_W	Clock Width	15		20		ns
f_{MAX}	Maximum Frequency		28.5		22	MHz

Notes:

1. I_{IX} (Pin 1) = 25 μA Max., $V_{SS} \le V_{IN} \le 2.7V$. I_{IX} (Pin 1) = 1 mA Max., $2.7V \le V_{IN} \le V_{CC}$.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.
5. *Figure 1a* test load used for all parameters except t_{EA}, t_{ER} t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
6. Extended temperature operation guaranteed with 400 linear feet per minute air flow.

AC Test Loads and Waveforms

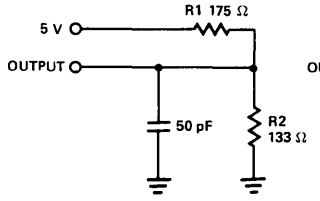
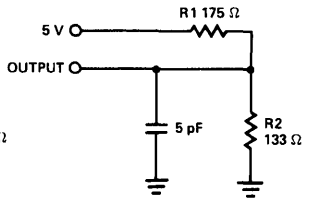


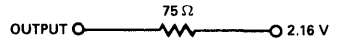
Figure 1a. Commercial



0038-11

Figure 1b. Commercial

Equivalent to:
THÉVENIN EQUIVALENT COMMERICAL



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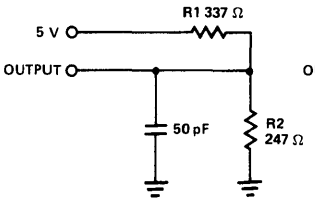
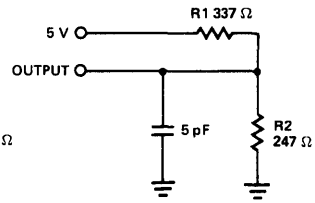


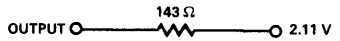
Figure 1c. Military



0038-9

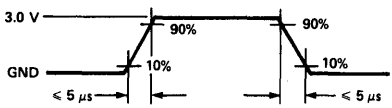
Figure 1d. Military

Equivalent to:
THÉVENIN EQUIVALENT MILITARY



0038-12

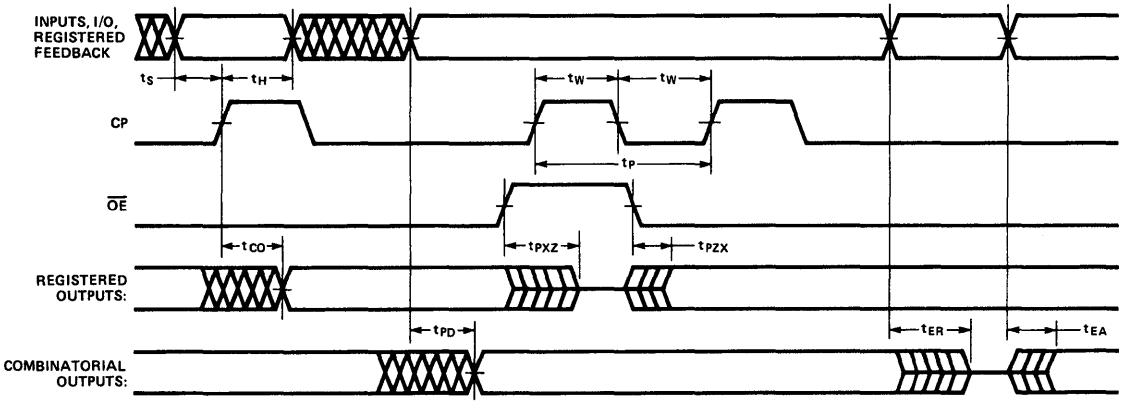
INPUT PULSES



0038-13

Figure 2

Switching Waveforms



0038-14

Figure 3

Programming

PAL C devices are programmed a BYTE at a time using a voltage to transfer electrons to a floating gate. The array programmed is addressed as memory of 256 bytes, using address Tables 4 and 5. These addresses are supplied to the device over Pins 2 through 9. The data to be programmed is supplied on data inputs D0 through D7 (Pins 19 through 12 inclusive). In the unprogrammed state, all inputs are connected to product terms. A "1" on a data line causes a cell to be programmed, disconnecting an INPUT TERM from a PRODUCT TERM. During verify, an unprogrammed cell causes a "1" to appear on the output, while a programmed cell will appear as a "0". Table 3 describes the operating modes of the device and the programming waveforms are described in *Figures 6* through *9*. The actual sequence required to program a cell is described in *Figure 5* and applies for programming either standard or phantom portions of the array. The security bit should be programmed using a single 10 ms pulse, and verified per *Figure 9*.

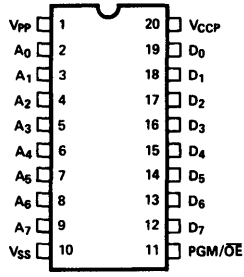


Figure 4. Programming Pin Configuration

DC Programming Parameters Ambient Temperature = 25°C

Table 1

Parameter	Description	Min.	Max.	Units	Notes
V_{PP}	Programming Voltage	13.0	14.0	V	
V_{CCP}	Supply Voltage During Programming	4.75	5.25	V	
V_{IHP}	Programming Input High Voltage	3.0		V	
V_{ILP}	Programming Input Low Voltage		0.4	V	
V_{OH}	Output High Voltage	2.4		V	1
V_{OL}	Output Low Voltage		0.4	V	1
I_{PP}	Programming Supply Current		50	mA	

AC Programming Parameters Ambient Temperature = 25°C

Table 2

Parameter	Description	Min.	Max.	Units	Notes
t_{PP}	Programming Pulse Width	100	10,000	μs	2
t_S	Setup Time	1.0		μs	
t_H	Hold Time	1.0		μs	
t_r, t_f	V_{PP} Rise and Fall Time	1.0		μs	2
t_{VD}	Delay to Verify	1.0		μs	
t_{VP}	Verify Pulse Width	2.0		μs	
t_{DV}	Verify to Data Valid	20.0		μs	
t_{DZ}	Verify to High Z		1.0	μs	

Table 3

Pin Name	V_{PP}	PGM/$\overline{OE}$	A1	A2	A3	A4	A5	D7–D0	Notes
Pin Number	(1)	(11)	(3)	(4)	(5)	(6)	(7)	(12–19)	
Operating Modes									
PAL	X	X	X	X	X	X	X	Programmed Function	3, 4
Program PAL	V_{PP}	V_{PP}	X	X	X	X	X	Data In	3, 5
Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	X	High Z	3, 5
Program Verify	V_{PP}	V_{ILP}	X	X	X	X	X	Data Out	3, 5
Phantom PAL	X	X	X	X	X	V_{PP}	X	Programmed Function	3, 6
Program Phantom PAL	V_{PP}	V_{PP}	X	X	X	X	V_{PP}	Data In	3, 7
Phantom Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	V_{PP}	High Z	3, 7
Phantom Program Verify	V_{PP}	V_{ILP}	X	X	X	X	V_{PP}	Data Out	3, 7
Program Security Bit	V_{PP}	V_{PP}	V_{PP}	X	X	X	X	High Z	3, 8
Verify Security Bit	X	X	Note 9	V_{PP}	X	X	X	High Z	3
Register Preload	X	X	X	X	V_{PP}	X	X	Data In	3, 10

Notes:

1. During verify operation
2. Measured at 10% and 90% points
3. $V_{SS} < X < V_{CCP}$
4. All "X" inputs operational per normal PAL function.
5. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 4 and 5.
6. All "X" inputs operational per normal PAL function except that they operate on the function that occupies the phantom array.
7. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 4 and 5. Pin 7 is used to select the phantom mode of operation and must be taken to V_{PP} before selecting phantom program operation with V_{PP} on Pin 1.
8. See *Figure 8* for security programming sequence.
9. The state of Pin 3 indicates if the security function has been invoked or not. If Pin 3 = V_{OL} security is in effect, if Pin 3 = V_{OH}, the data is unsecured and may be directly accessed.
10. For testing purposes, the output latch on the 16R8, 16R6 and 16R4 may be preloaded with data from the appropriate associated output line.

The programmable array is addressed as a basic 256 by 8 memory structure with a duplication of the phantom array located at the same addresses as columns 0, 1, 2 and 3. The ability to address the phantom array as differentiated from the first 4 columns of the normal array is accomplished by taking Pin 7 to V_{PP} and entering the phantom mode of operation as shown in Tables 3 and 5. In either case, phantom or normal, product terms are addressed in groups of 8 per Table 4. Notice that this is accomplished by modulo 8 selecting every eighth product term starting with 0, 8, 16, 24, 32, 40, 48 and 56 corresponding to PROGRAMMED DATA INPUT on D0 through D7 respectively and incrementing each product term by one until all 64 PRODUCT TERMS are addressed. Each of the INPUT TERMS is addressed 8 times corresponding to the 8 groups of individual product terms addressed before being incremented.

Table 4

Product Term Addresses										
Binary Addresses			Line Number							
Pin Numbers										
(4)	(3)	(2)								
V_{ILP}	V_{ILP}	V_{ILP}	0	8	16	24	32	40	48	56
V_{ILP}	V_{ILP}	V_{IHP}	1	9	17	25	33	41	49	57
V_{ILP}	V_{IHP}	V_{ILP}	2	10	18	26	34	42	50	58
V_{ILP}	V_{IHP}	V_{IHP}	3	11	19	27	35	43	51	59
V_{IHP}	V_{ILP}	V_{ILP}	4	12	20	28	36	44	52	60
V_{IHP}	V_{ILP}	V_{IHP}	5	13	21	29	37	45	53	61
V_{IHP}	V_{IHP}	V_{ILP}	6	14	22	30	38	46	54	62
V_{IHP}	V_{IHP}	V_{IHP}	7	15	23	31	39	47	55	63
			D0	D1	D2	D3	D4	D5	D6	D7
			Programmed Data Input							

Table 5

Input Term Addresses						Input Term Addresses					
Input Term Numbers	Binary Addresses					Input Term Numbers	Binary Addresses				
	Pin Numbers						Pin Numbers				
	(9)	(8)	(7)	(6)	(5)		(9)	(8)	(7)	(6)	(5)
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	18	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
1	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	19	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
2	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	20	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	22	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
5	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	23	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
6	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	24	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	25	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
8	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	26	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
9	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	28	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	29	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
12	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	30	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
13	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	P0	V_{ILP}	V_{ILP}	V_{PP}	X	X
15	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	P1	V_{ILP}	V_{IHP}	V_{PP}	X	X
16	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	P2	V_{IHP}	V_{ILP}	V_{PP}	X	X
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	P3	V_{IHP}	V_{IHP}	V_{PP}	X	X

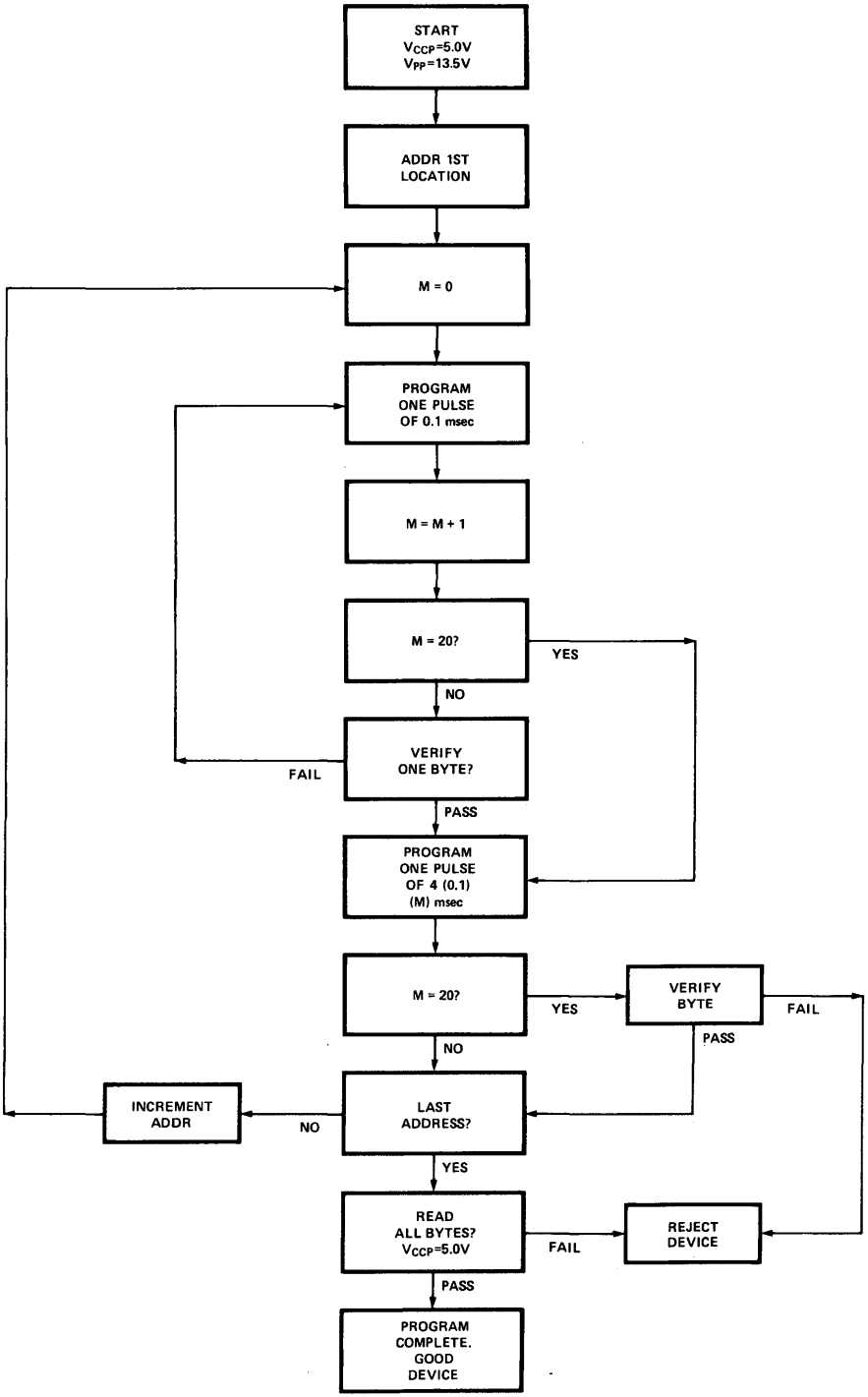


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Figure 5. Programming Flowchart

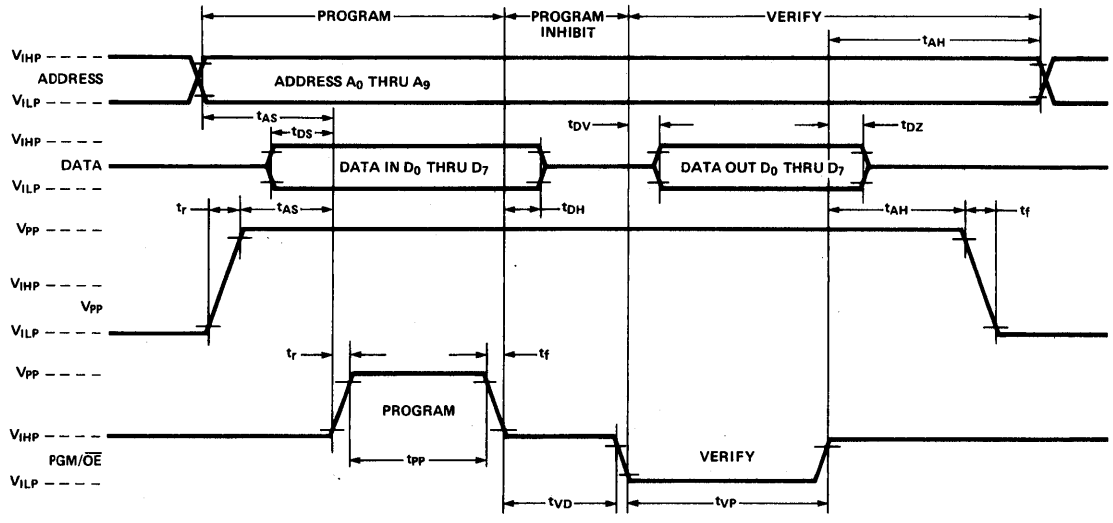


Figure 6. Programming Waveforms Normal Array

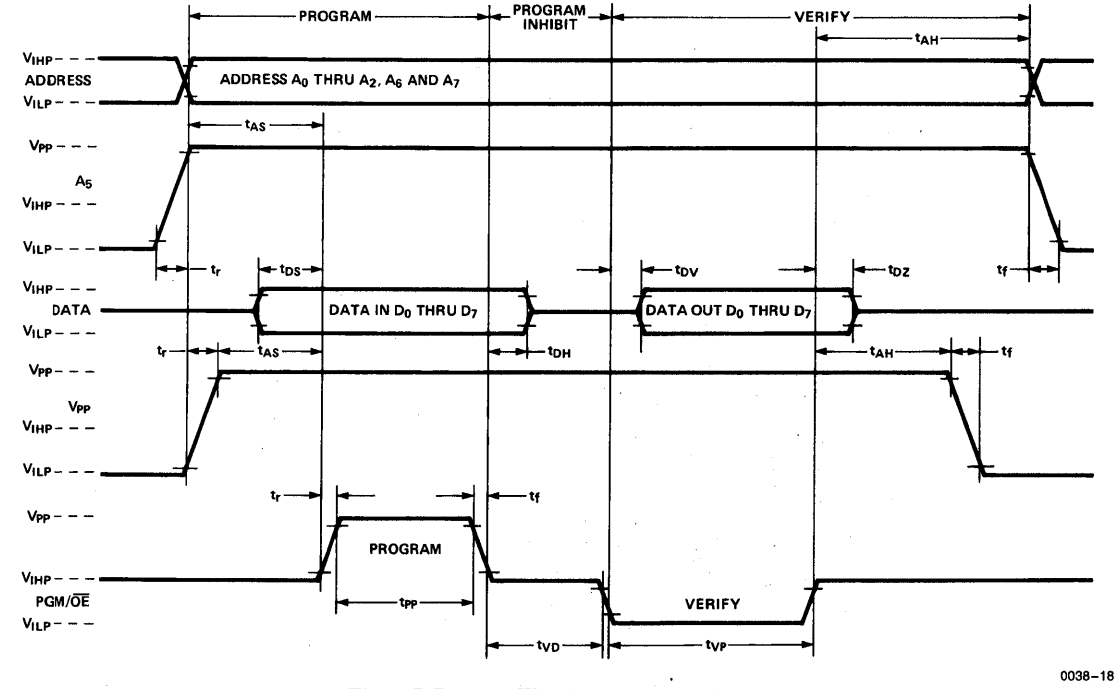


Figure 7. Program Waveforms Phantom Array

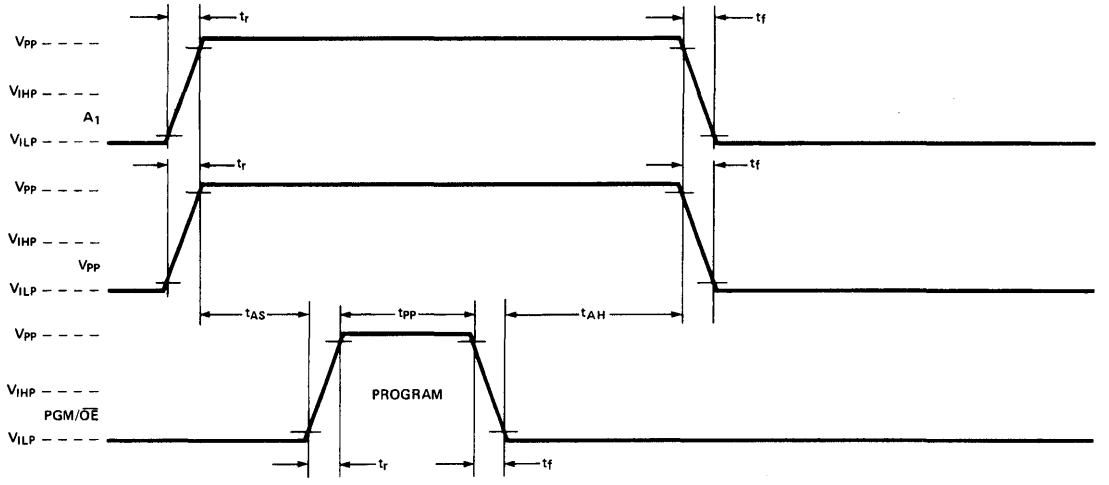


Figure 8. Activating Program Security

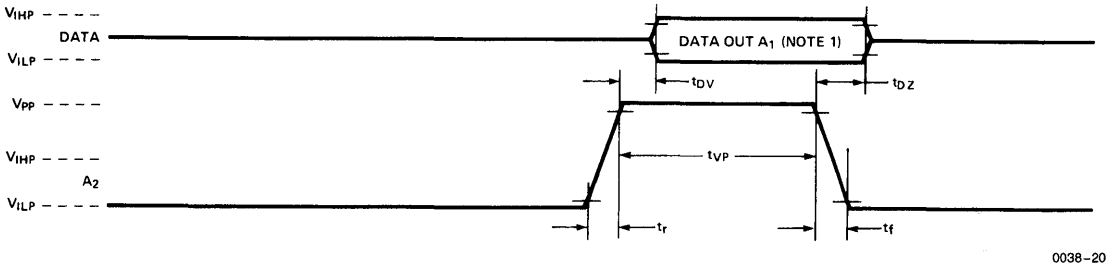
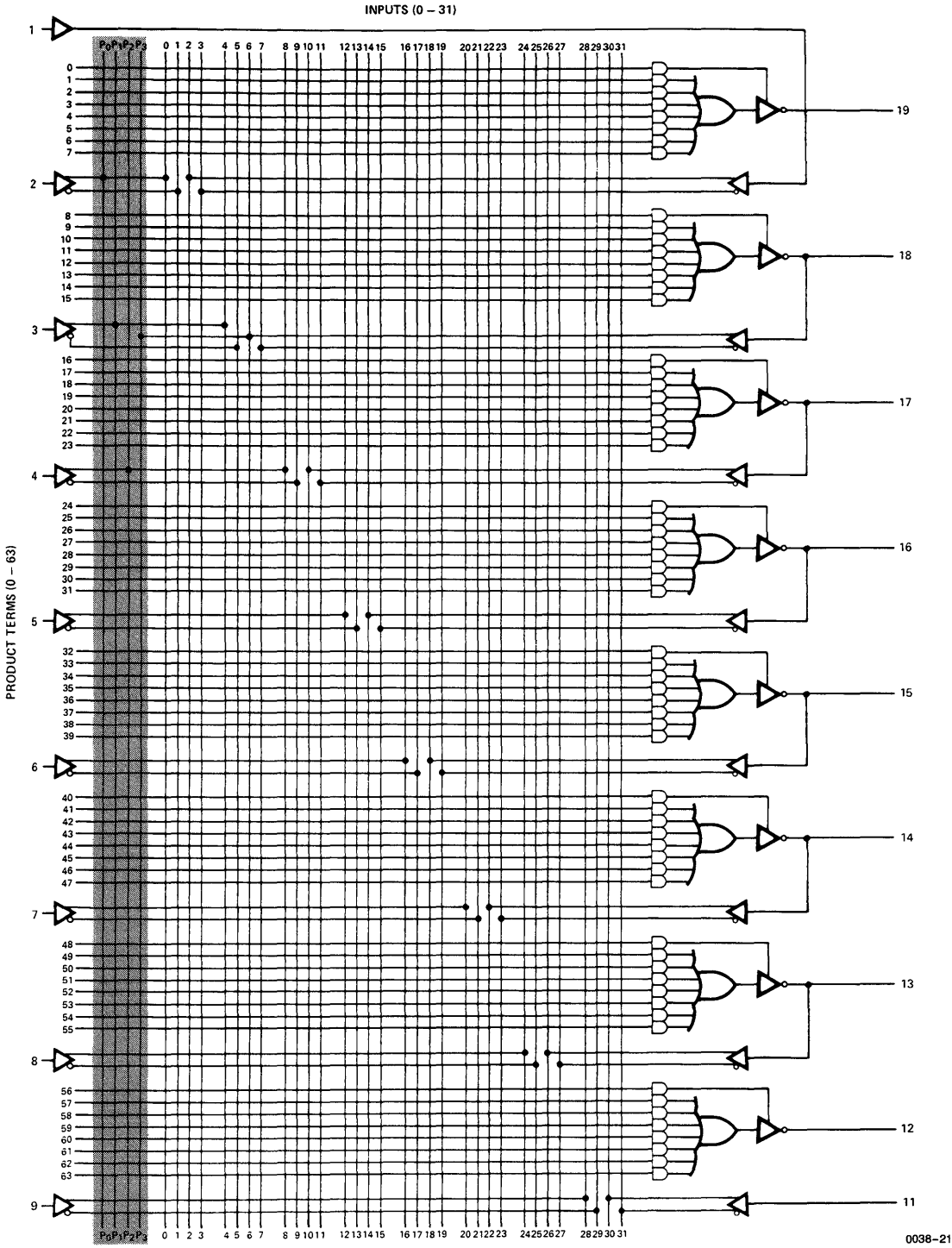
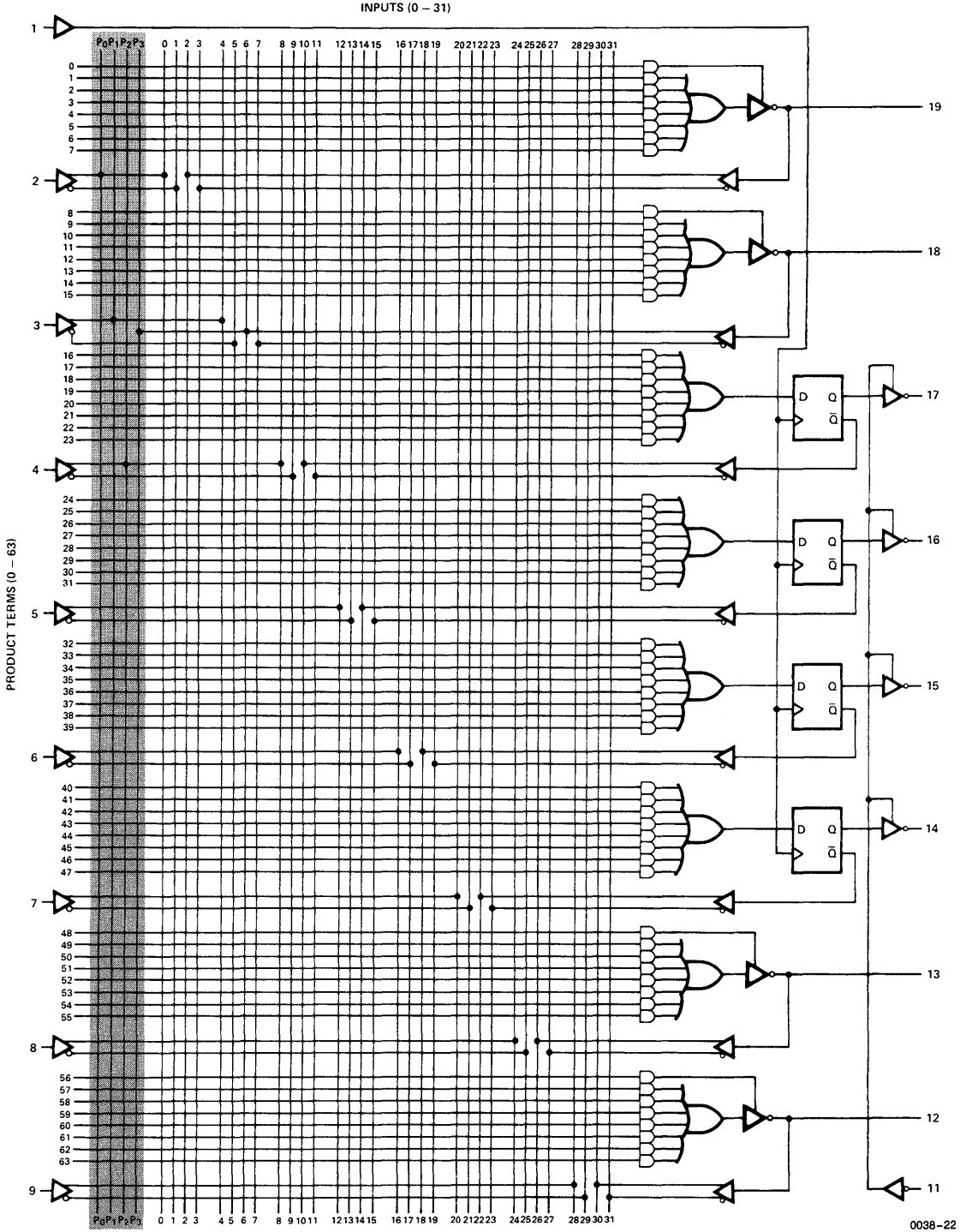


Figure 9. Verify Program Security

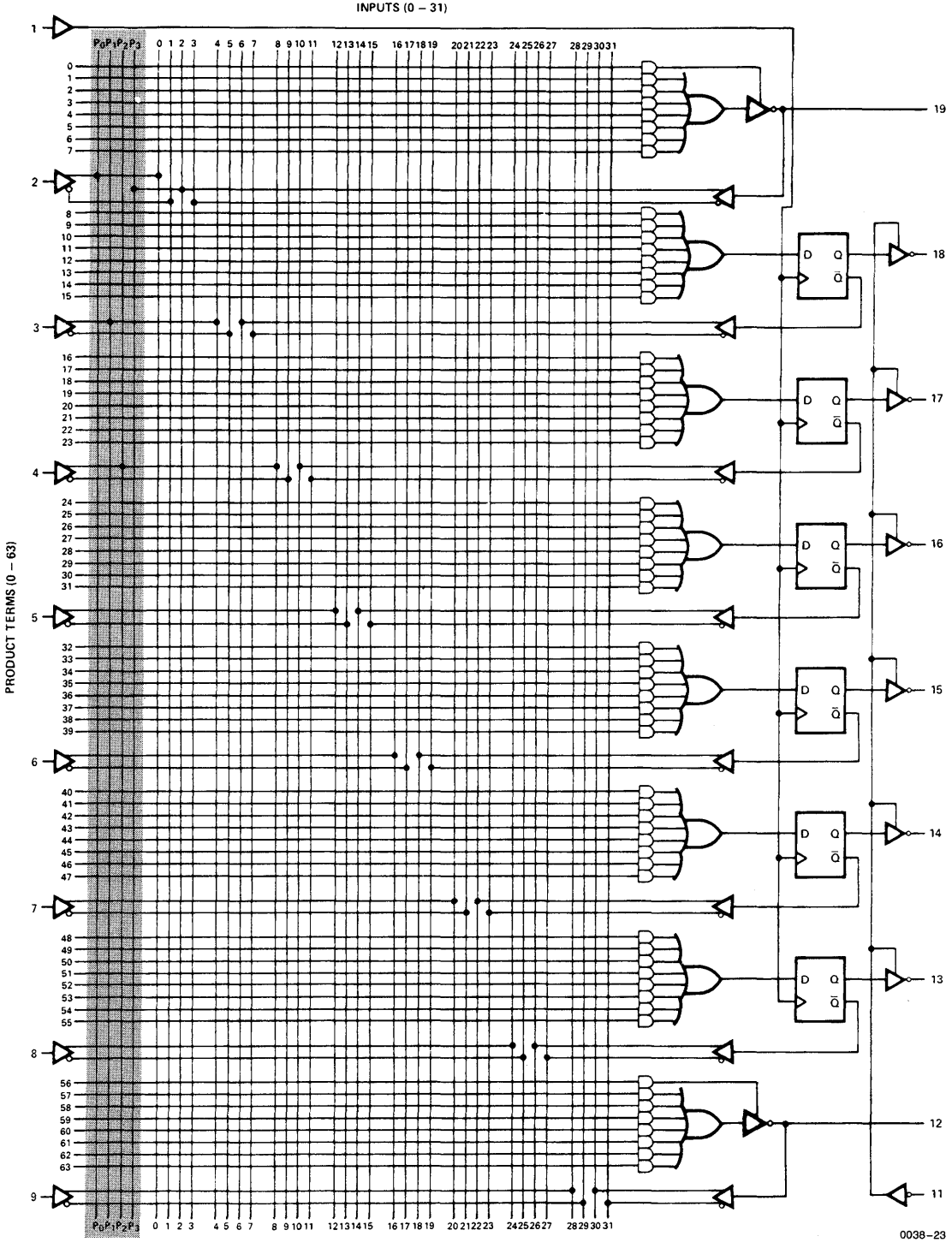
Functional Logic Diagram PAL C 16L8A



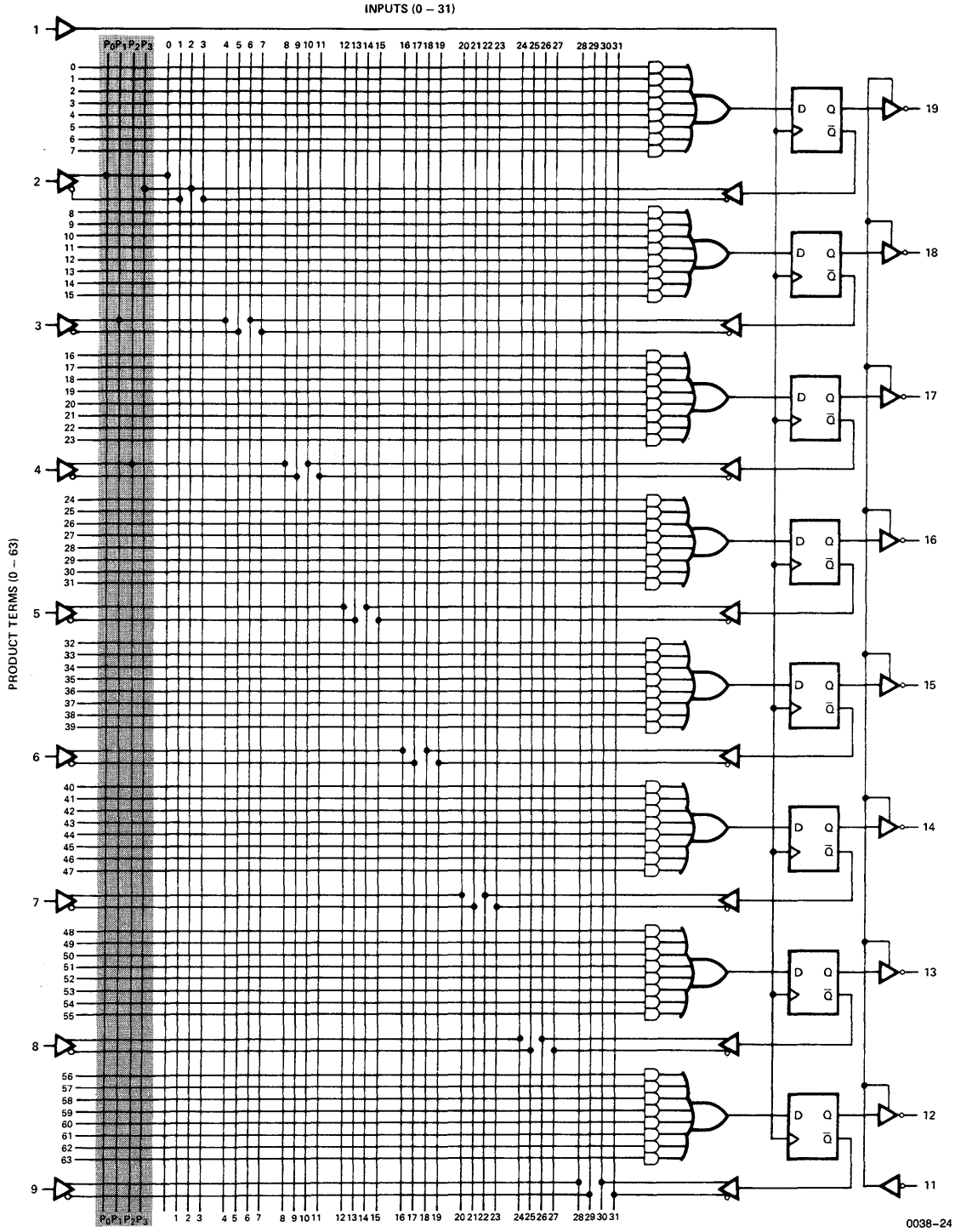
Functional Logic Diagram PAL C 16R4A



Functional Logic Diagram PAL C 16R6A

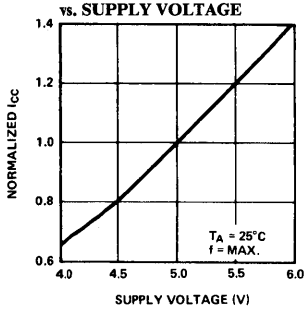


Functional Logic Diagram PAL C 16R8A

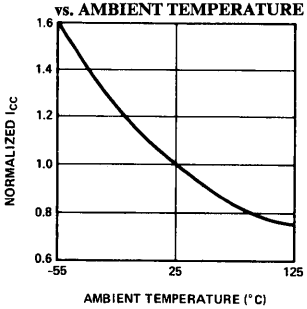


Typical DC and AC Characteristics

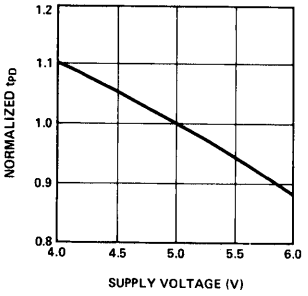
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



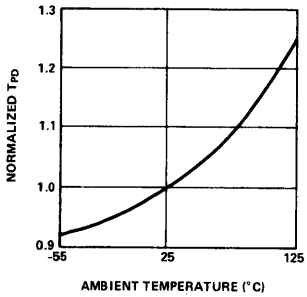
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



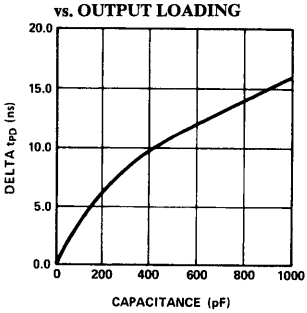
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



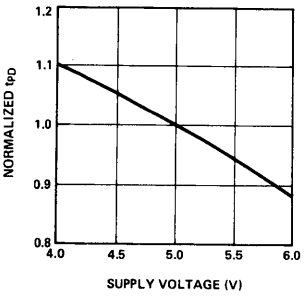
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



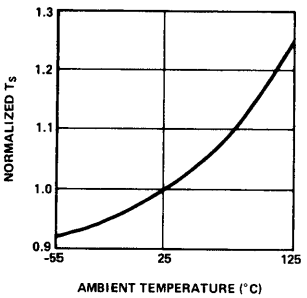
DELTA PROPAGATION TIME vs. OUTPUT LOADING



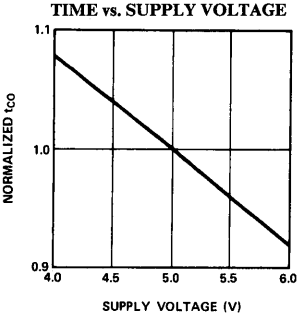
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



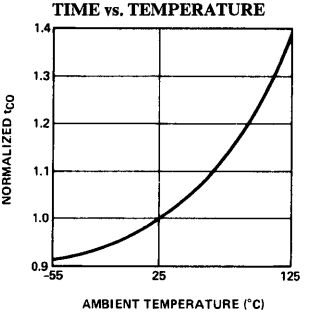
NORMALIZED SETUP TIME vs. TEMPERATURE



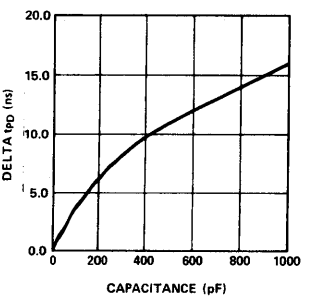
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



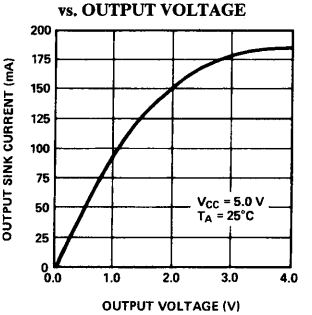
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



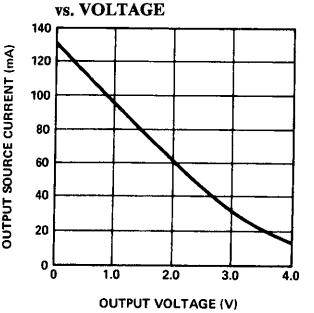
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



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Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
90	25	—	—	PAL C 16L8A PC	P5	Commercial
90	25	—	—	PAL C 16L8A DC	D6	Commercial
90	25	—	—	PAL C 16L8A LC	L61	Commercial
90	30	—	—	PAL C 16L8A DMB	D6	Military
90	30	—	—	PAL C 16L8A LMB	L61	Military
90	—	20	15	PAL C 16R8A PC	P5	Commercial
90	—	20	15	PAL C 16R8A DC	D6	Commercial
90	—	20	15	PAL C 16R8A LC	L61	Commercial
90	—	25	20	PAL C 16R8A DMB	D6	Military
90	—	25	20	PAL C 16R8A LMB	L61	Military
90	25	20	15	PAL C 16R6A PC	P5	Commercial
90	25	20	15	PAL C 16R6A DC	D6	Commercial
90	25	20	15	PAL C 16R6A LC	L61	Commercial
90	30	25	20	PAL C 16R6A DMB	D6	Military
90	30	25	20	PAL C 16R6A LMB	L61	Military
90	25	20	15	PAL C 16R4A PC	P5	Commercial
90	25	20	15	PAL C 16R4A DC	D6	Commercial
90	25	20	15	PAL C 16R4A LC	L61	Commercial
90	30	25	20	PAL C 16R4A DMB	D6	Military
90	30	25	20	PAL C 16R4A LMB	L61	Military

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION **PAL C 22V10**

CMOS PAL® Device

Features

- **Advanced second generation PAL architecture**
- **Up to 22 input terms and 10 outputs**
- **Variable product terms**
  - **— 2 × (8 thru 16) product terms**
- **User programmable macro cell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **Standard and high performance versions**
  - **— "A"**
  - **— 15 ns T_{co}**
  - **— 25 ns T_s**
  - **— 30 ns T_{pd}**
  - **— "STD"**
  - **— 25 ns T_{co}**
  - **— 35 ns T_s**
  - **— 35 ns T_{pd}**
- **Low power 120 mA max**
- **Commercial and military Temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >2000V input protection**
  - **— 100% programming and functional testing**

Functional Description

The Cypress PAL C 22V10 is a CMOS second generation Programmable Logic Array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macro Cell".

The PAL C 22V10 is executed in a 24 pin package and provides up to 22 inputs and 10 outputs. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.

The PAL C 22V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 22V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device also incorporates a power-up reset feature to guarantee that one unique condition on application of power results and the ability to preload the output registers for testing.

The PAL C 22V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled through the use of product terms. Any output pin may be permanently selected as an out-

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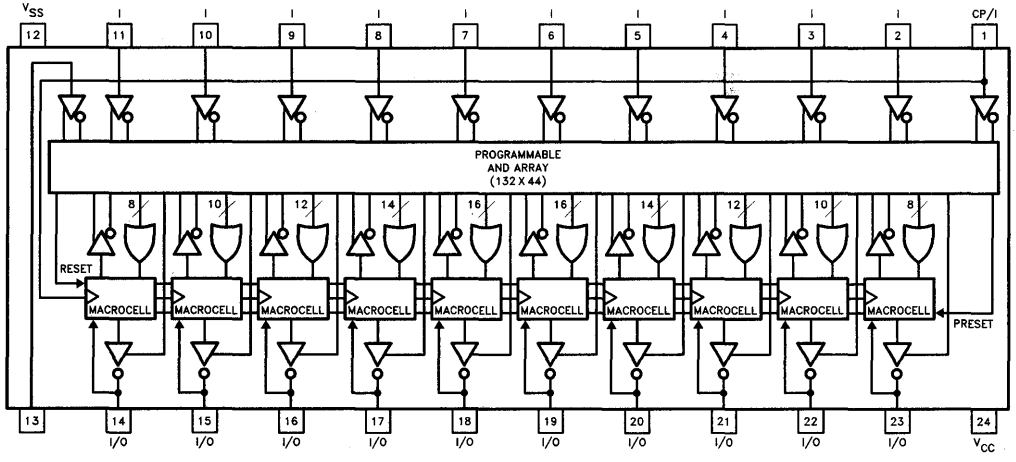
Logic Symbol and Pinout



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Functional Description (Continued)

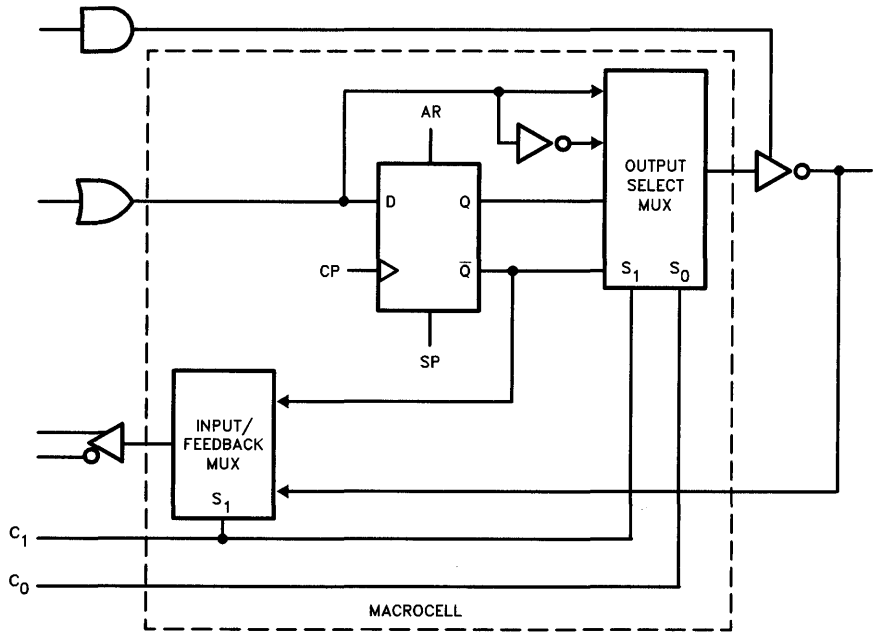
put or arbitrarily enabled as an output and an input thru the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. These macro cells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 22V10 provides lower power operation thru the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. This phantom array allows the 22V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 22V10 at incoming inspection before committing the device to a specific function through programming.

Configuration Table 1

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

Macrocell



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Selection Guide

Part Number	I_{CC} mA		T_{pd} ns		T_s ns		T_{co} ns	
	COM	MIL	COM	MIL	COM	MIL	COM	MIL
22V10A	120	120	30	35	25	30	15	20
22V10	120	120	35	40	35	40	25	25

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 24 mA

DC Programming Voltage 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	COM'L	2.4		V
			I_{OH} = −2 mA	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	COM'L		0.4	V
			I_{OL} = 12 mA	MIL			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_S \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$ Outputs Open				120	mA

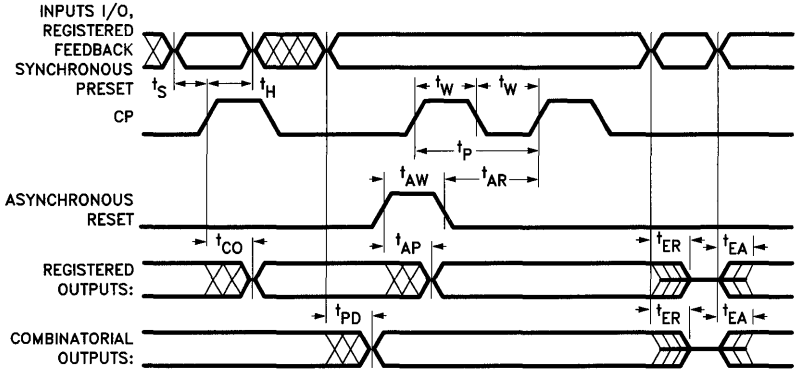
Capacitance

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

Switching Characteristics PAL C 22V10

Parameters	Description	Commercial				Military				Units
		"A"		"STD"		"A"		"STD"		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
T_{pd}	Input or Feedback to Non-Registered Output		30		35		35		40	ns
T_{ea}	Input to Output Enable		30		35		35		40	ns
T_{er}	Input to Output Disable		30		35		35		40	ns
T_{co}	Clock to Output		15		25		20		25	ns
T_s	Input or Feedback Setup Time	25		35		30		40		ns
T_h	Hold Time	0		0		0		0		ns
T_p	Clock Period ($T_s + T_{co}$)	40		60		50		65		ns
T_w	Clock Width	20		25		25		30		ns
F_{max}	Maximum Frequency		25		16.5		20		15	MHz
T_{aw}	Asynchronous Reset Width		25		35		30		40	ns
T_{ar}	Asynchronous Reset Recovery Time		25		35		30		40	ns
T_{ap}	Asynchronous Reset to Registered Output Reset		25		35		30		40	ns

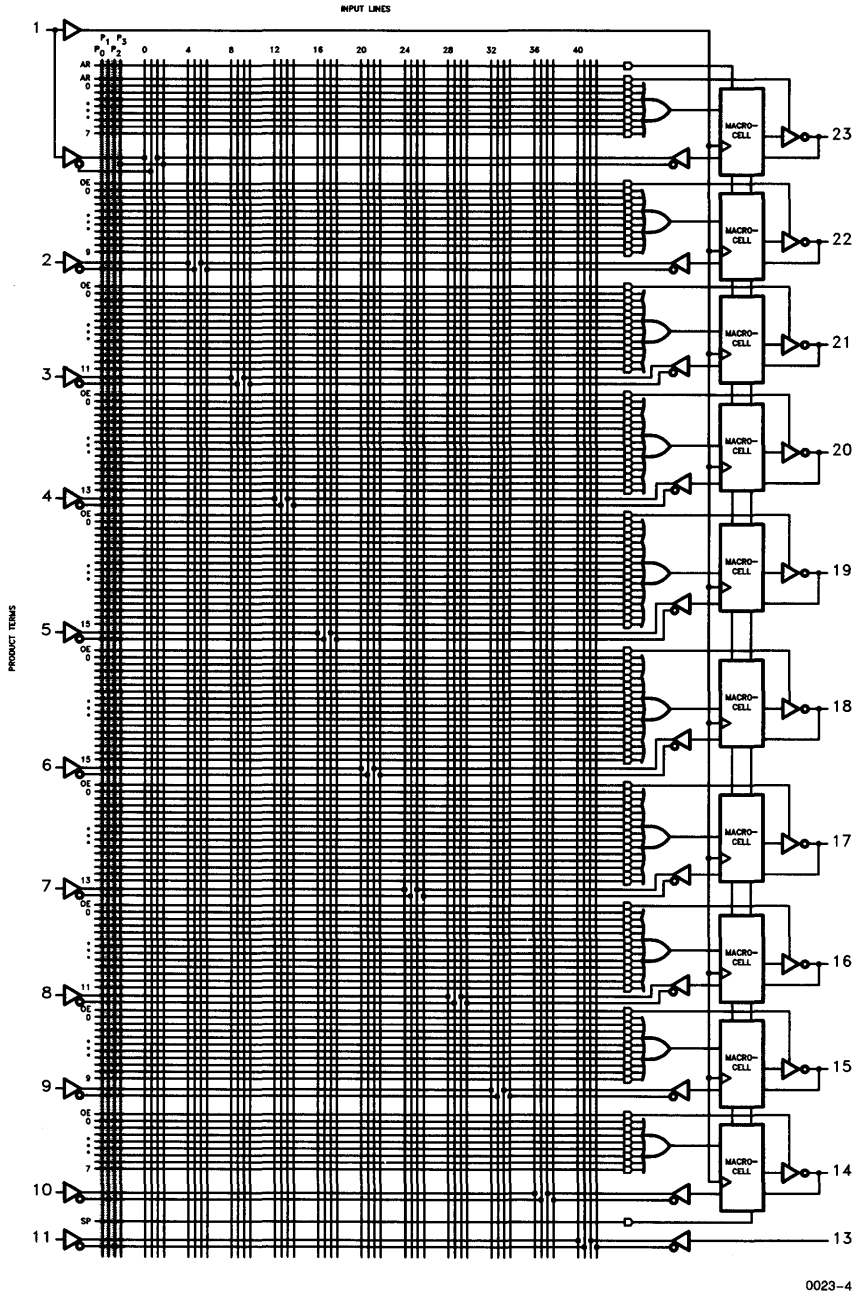
Switching Waveforms



0023-3

4

Functional Logic Diagram PAL C 22V10



CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION **PAL C 32V10**

CMOS PAL® Device

Features

- **Advanced second generation PAL architecture**
- **Up to 32 input terms and 10 outputs**
- **Variable product terms**
  - **— 2 × (8 thru 16) product terms**
- **User programmable macro cell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
  - **— Selectable output enable from array or external output enable**
  - **— Registered or combinatorial feedback**
  - **— Buried registers available when output pin is used for an input**
- **Standard and high performance versions**
  - **— "A"**
  - **— 15 ns T_{co}**
  - **— 25 ns T_s**
  - **— 30 ns T_{pd}**
  - **— "STD"**
  - **— 25 ns T_{co}**
  - **— 35 ns T_s**
  - **— 35 ns T_{pd}**
- **Low power 120 mA max**
- **Commercial and military temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >2000V input protection**
  - **— 100% programming and functional testing**

Functional Description

The Cypress PAL C 32V10 is a CMOS second generation Programmable Logic Array device utilizing an advanced macro cell. It is implemented with the familiar sum-of-products (AND-OR) logic structure, variable product terms and a macro cell that allows I/O pins associated with macro cell to be used without losing the use of the register in the macro cell and its feedback terms.

The PAL C 32V10 is executed in a 24 pin package and provides up to 22 inputs and 10 outputs to the package. Internally 32 inputs to the array are implemented. This is achieved by providing both an input from the I/O pin and either a feedback from the combinatorial path or from the register. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may also be individually selected allowing complete flexibility of output configuration.

Associated with each of the I/O macro cell combinations are two inputs to the programmable array. One comes directly from the I/O pin, bypassing the macro cell itself and allowing either feedback into the array of the state of the output or use of the pin as an input whenever the output buffer is in a high impedance condition. The second input into the array comes directly from the macro cell and may be either the output of the register or the combinatorial feedback that results from the sum of products associated with the specific macro cell. By providing both of these paths, the I/O pin may be used as an input and the register may still be used as a state register (buried state register).

Further configurability is provided by allowing the output buffers to be enabled either through the array or via an external input. Through an "ARRAY" configurable "OUTPUT ENABLE" each of the potential 10 outputs may be

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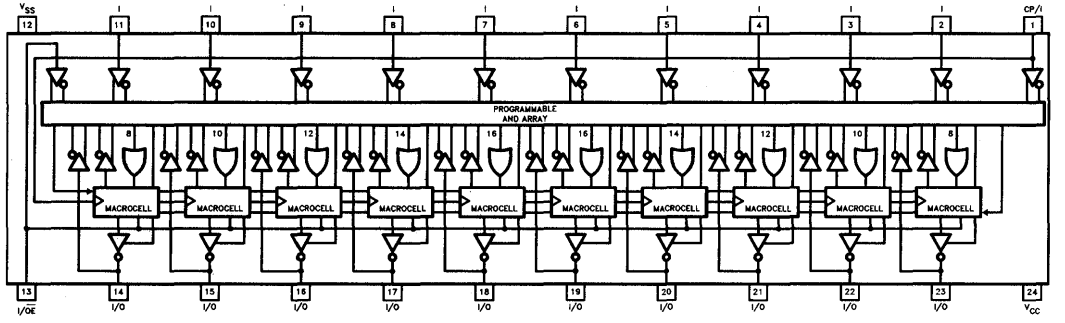
Logic Symbol and Pinout



Functional Description (Continued)

reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array. External output enables allow the external selection of the functions generated in the PAL device along with the shorter enable/disable times associated with direct control of the output buffers.

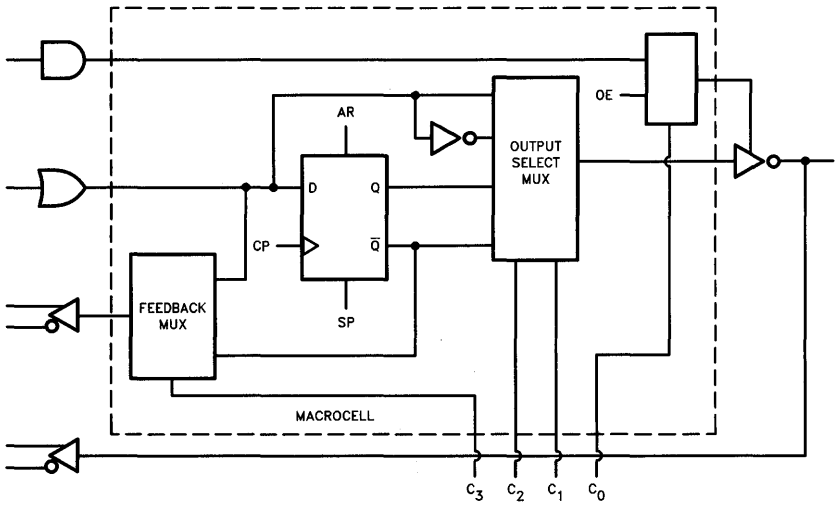
The PAL C 32V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 32V10 is optimized for the configurations found in a large majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 32V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device also incorporates a power-up reset feature to guarantee that one unique condition on application of power results and the ability to preload the output registers for testing.

The PAL C 32V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs and anywhere in between are possible. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input thru the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 32V10 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature, access to even buried registers for testing purposes and guaranteed AC performance through the use of a phantom array. This phantom array allows the 32V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 32V10 at incoming inspection before commiting the device to a specific function through programming.

Macrocell and Configuration Tables



0022-2

Output Enable

C_0	Configuration
0	External Output Enable
1	Internal Output Enable

Registered/Combinatorial

C_1	C_2	Configuration
0	0	Combinatorial Active High
0	1	Combinatorial Active Low
1	0	Registered Active High
1	1	Registered Active Low

Feedback

C_3	Configuration
0	Combinatorial Feedback
1	Registered Feedback

Selection Guide

Part Number	I_{CC} mA		T_{pd} ns		T_s ns		T_{co} ns	
	COM	MIL	COM	MIL	COM	MIL	COM	MIL
32V10A	120	120	30	35	25	30	15	20
22V10	120	120	35	40	35	40	25	25

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 24 mA

DC Programming Voltage 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	COM'L	2.4		V
			I_{OH} = −2 mA	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	COM'L		0.4	V
			I_{OL} = 12 mA	MIL			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_S \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$, Outputs Open				120	mA

Capacitance

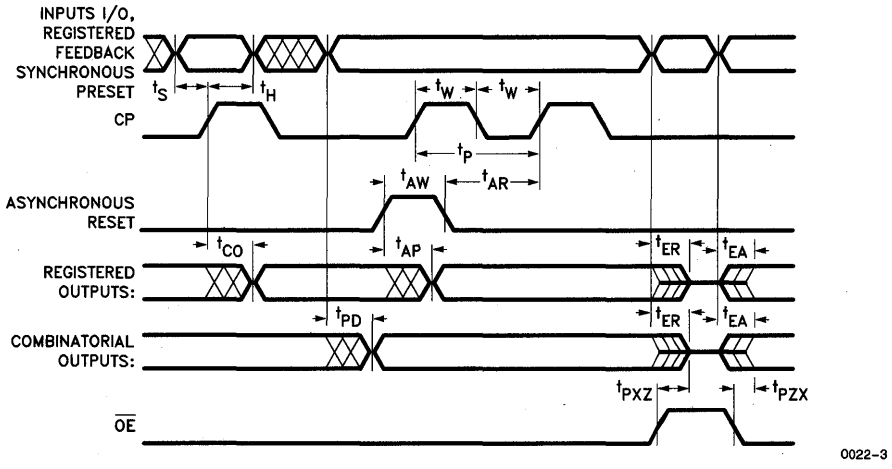
Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 5)		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 5)		8	pF

4

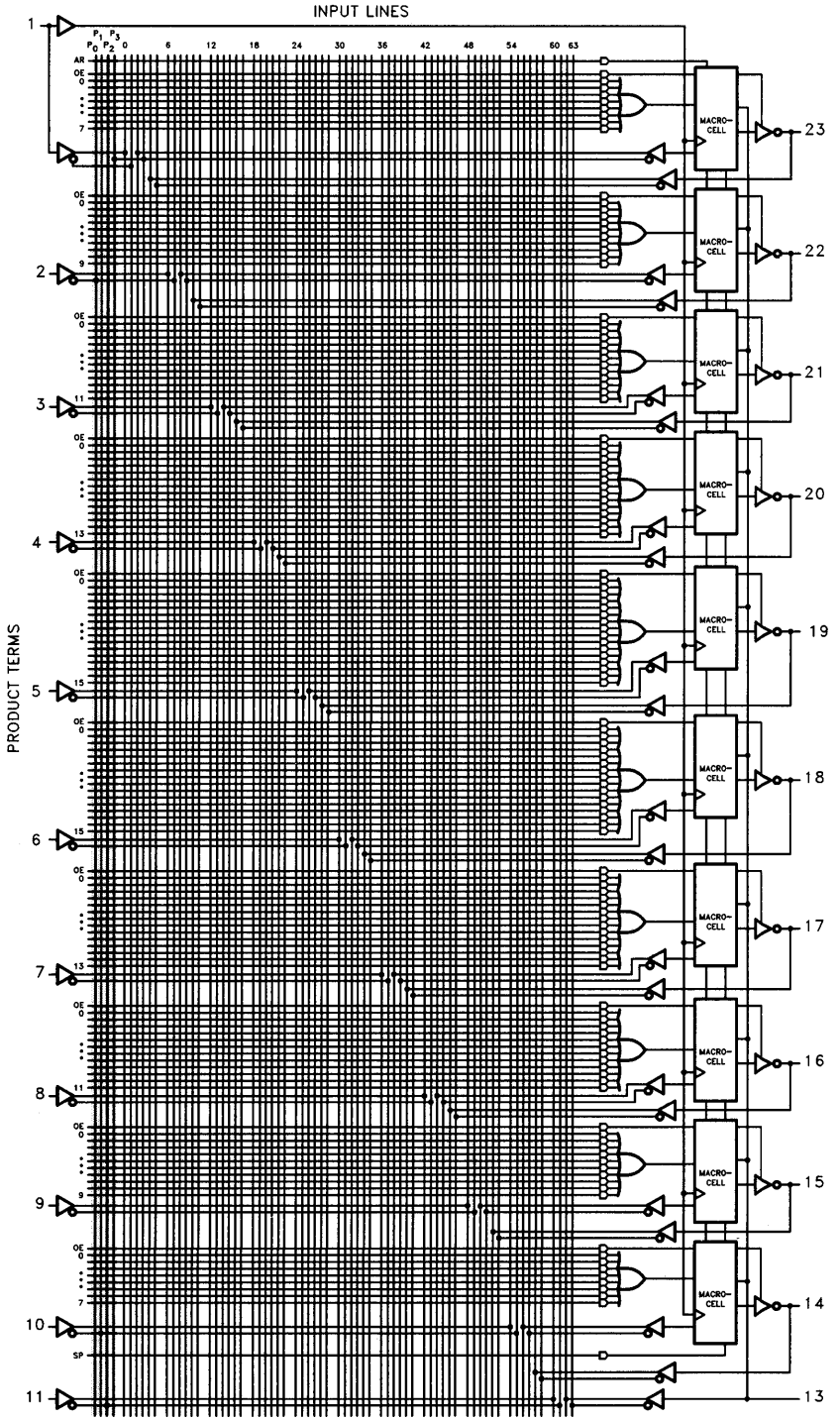
Switching Characteristics PAL C 32V10

Parameters	Description	Commercial				Military				Units
		"A"		"STD"		"A"		"STD"		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
T_{pd}	Input or Feedback to Non-Registered Output		30		35		35		40	ns
T_{ea}	Input to Output Enable		30		35		35		40	ns
T_{er}	Input to Output Disable		30		35		35		40	ns
T_{co}	Clock to Output		15		25		20		25	ns
T_s	Input or Feedback Setup Time	25		35		30		40		ns
T_h	Hold Time	0		0		0		0		ns
T_p	Clock Period ($T_s + T_{co}$)	40		60		50		65		ns
T_w	Clock Width	20		25		25		30		ns
T_{pzx}	External Output Enable		20		25		25		25	ns
T_{pxz}	External Output Disable		20		25		25		25	ns
F_{max}	Maximum Frequency		25		16.5		20		15	mhz
T_{aw}	Asynchronous Reset Width		25		35		30		40	ns
T_{ar}	Asynchronous Reset Recovery Time		25		35		30		40	ns
T_{ap}	Asynchronous Reset to Registered Output Reset		25		35		30		40	ns

Switching Waveforms



Functional Logic Diagram PAL C 32V10



Introduction

PALs or Programmable Array Logic provide an attractive alternative to logic implemented in discrete logic. Because the primary requirement of this logic is to provide the highest performance possible, in the past all programmable logic products had been implemented in a bipolar process technology. Bipolar technology uses a fuse for the programming mechanism. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a programming system. Since the fuses may only be blown or programmed once, they may not be programmed during test to determine that they will indeed program. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for three reasons.

First some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance, this fallout is easily identified. Second, material may fail because it does not function correctly even though it successfully programs and verifies correctly. This phenomena occurs because without programming each location in a device, the connection between the programmed cell and the logic that it drives cannot be 100% tested. This can sometimes be tested in some programmers by generating a unique set of test vectors for each pattern and testing each device with its test pattern immediately after programming. Additional material however is lost because it fails to perform even though it programs correctly and passes a functional test. This failure is normally due to the device being too slow. This is a much more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PALs use an EPROM programming mechanism. This technology has also been in use in MOS technologies since the early 1970s however, as with most MOS technologies its emphasis has been in density, not performance. CMOS at Cypress however is as fast as or faster than bipolar and coupled with EPROM becomes a viable alternative to bipolar programmable logic from a performance point of view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns the transistor off. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of only devices that not only will program every time, but that when programmed, will perform as specified.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

Programming Algorithm

Byte Addressing and Programming

All Cypress Programmable Logic Devices are addressed and programmed on BYTE or EXTENDED BYTE basis for programming, where an EXTENDED BYTE is a field that is as wide as the output path of the device. Each device or family of devices as a unique address map which is available in the product data sheet. Each BYTE or EXTENDED BYTE is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a "1" or HIGH is placed on the input pin and a "0" or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A "1" or HIGH during program verify operation indicates an unprogrammed cell, while a "0" or LOW indicates that the cell accessed has been programmed.

Blank Check

Before programming all Programmable Logic Devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a "1" or HIGH output indicates that the addressed cell is unprogrammed, while a "0" or LOW indicates a programmed cell.

Programming The Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ/WRITE pin in the programming mode. This signal causes a write operation when switched to a supervoltage, and a read operation when switched to a logic "0" or LOW. In the logic high state "1" the device is in a program inhibit condition and the output pins are in a high impedance state. During a WRITE operation, the data on the output pins is written into the addressed array location. In a READ operation the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location Verification of data is accomplished by examining the information on the output pins during a READ operation.

The timing for actual programming is supplied in the unique programming specification for each device.

Phantom Operating Modes

All Cypress Programmable Logic Devices contain a PHANTOM ARRAY for the purposes of post assembly testing. This array is accessed, programmed and operated in a special PHANTOM mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the PHANTOM ARRAY is connected. In normal operation the PHANTOM ARRAY is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging, if desired by the user before programming and use. The PHANTOM modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific data sheets for details.

Special Features

Cypress Programmable Logic devices depending on the device have several special features. For example the Security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access to the content. In advanced devices, the architecture bits allow the designer to tailor the basic function of the output to meet unique system requirements. These features take advantage of the EPROM cell for programming. Specific programming of these special features are depicted in the specific device data sheet.

Programming Support

Programming support for Cypress CMOS Programmable Logic Devices is available from a number of programmer manufacturers some of which are listed below.

Data I/O
Programmer Model 29
Logicpak

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444

Stag
Programmer PPZ
ZL30

Stag Microsystems
528-5 Weddell Dr.
Sunnyvale, CA 94089
(408) 745-1991

Wavetek Digilec
Programmer Model 803

Wavetek Digilec
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089
(408) 745-0722

Section Contents

LOGIC

CY2901B
CY2901C

CYPRESS SEMICONDUCTOR

CMOS Four-Bit Slice

Features

- **Pin compatible and functional equivalent to AMD AM2901B, C**
- **Low power**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Eight function ALU**
  Performs eight operations on two 4-bit operands
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Four status flags**
  Carry, overflow, negative, zero
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage

Functional Description

The CY2901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY2901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY2901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

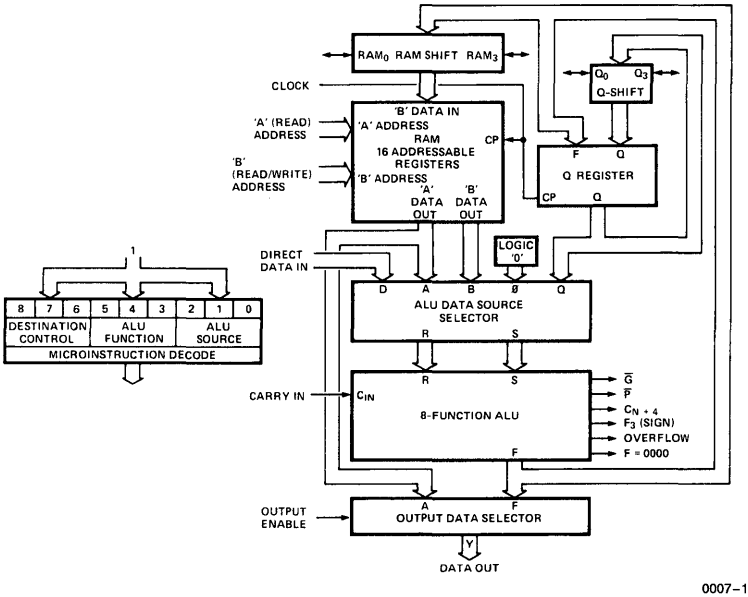
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from an instruction register.

The CY2901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full-look ahead carry or a ripple carry.

The CY2901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY2901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance at a low power dissipation.

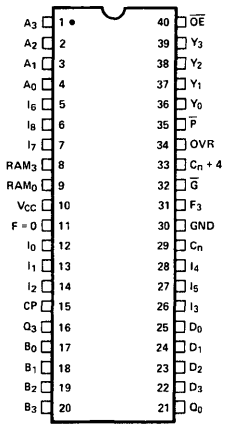
Logic Block Diagram



0007-1

Pin Configuration

Top View



0007-2

5

CYPRESS SEMICONDUCTOR

Microprogram Controller

Features

- **Twelve bits wide**
  - **— Addresses up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.**
- **Internal loop counter**
  - **— Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.**
- **Four address sources**
  - **— Microprogram address may be selected from microprogram counter, branch address bus, 9-level push/pop stack, or internal holding register.**
- **Sixteen powerful microinstructions**
  - **— Executes 16 sequence control instructions, most of which are conditional on external condition input, state of the internal loop counter, or both.**
- **Output enable controls for three branch address sources**
  - **— Built in decoder function to enable external devices onto branch address bus. Eliminates external decoder.**
- **Fast**
  - **— The CY2910 supports 100 ns cycle times.**

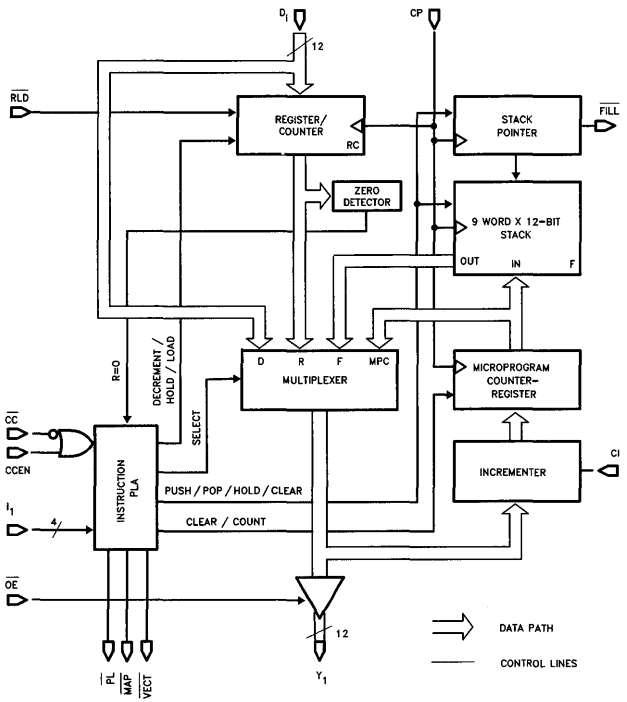
Functional Description

The CY2910 Microprogram Controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are nine levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (MPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (RC) retaining data loaded during a previous microinstruction; or 4) a nine-deep last-in, first-out stack (F).

The CY2910 is a pin compatible, functional equivalent, improved performance replacement for the AM2910 that is fabricated using an advanced 1.2 micron CMOS technology.

Block Diagram



CYPRESS SEMICONDUCTOR

CY3341

64 x 4 FIFO Serial Memory

Features

- **1.2 MHz data rate**
- **Fully TTL compatible**
- **Independent asynchronous inputs and outputs**
- **Direct replacement for PMOS 3341**
- **Expandable in word length and width**
- **CMOS for optimum speed/ power**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

The 3341 is a 64-word x 4-bit First-In First-Out (FIFO) Serial Memory. The inputs and outputs are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

Control signals are provided for both vertical and horizontal cascading.

The 3341 is manufactured using Cypress CMOS technology and is available in both ceramic and plastic packages.

Data Input

The four bits of data on the D_0 through D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH. This causes IR to go LOW but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus, data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

Data Output

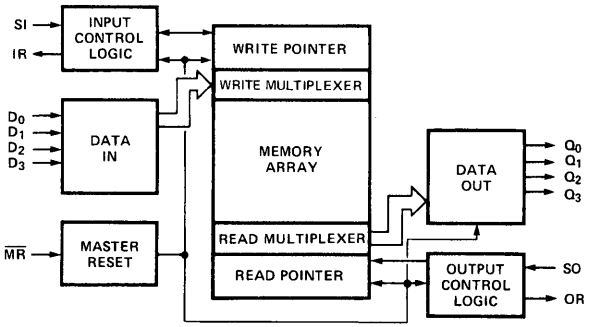
When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BT}) or completely empty (Output Ready stays LOW for at least t_{BT}).

Reset

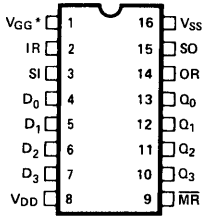
When Master Reset ($\overline{MR}$) goes LOW, the control logic is cleared, and the data outputs enter a LOW state. When $\overline{MR}$ returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW.

Logic Block Diagram



0004-1

Pin Configuration



0004-2

*Internally not connected

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 16 to Pin 8) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{SS}
Commercial	0°C to +70°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{SS} = Min., I_{OH} = −0.3 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{SS} = Min., I_{OL} = 1.6 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{SS}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{DD} \le V_I \le V_{SS}$	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{SS} = Max., V_{OUT} = V_{DD}		−90	mA
I_{DD}	Power Supply Current	V_{SS} = Max., I_{OUT} = 0 mA Commercial		45	mA
I_{GG}	V_{GG} Current			0	mA

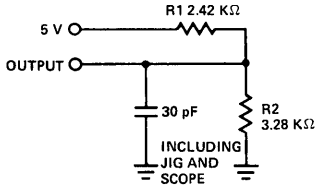
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V	10	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

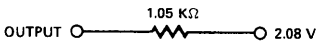
AC Test Loads and Waveforms



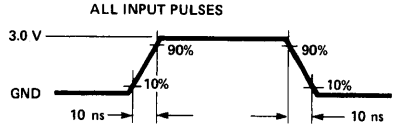
0004-3

Equivalent to:

THÉVENIN EQUIVALENT



0004-4



0004-5

Switching Characteristics Over the Operating Range[3]

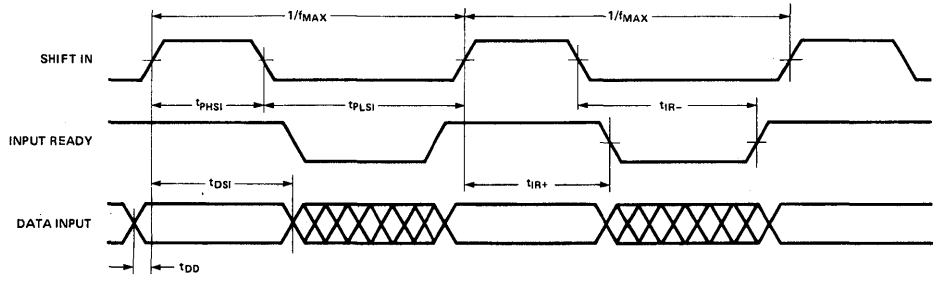
Parameters	Description	Test Conditions	Min.	Max.	Units
f_{MAX}	Operating Frequency	Note 4		1.2	MHz
t_{PHSI}	SI HIGH Time		80		ns
t_{PLSI}	SI LOW Time		80		ns
t_{DD}	Data Setup to SI		0		ns
t_{DSI}	Data Hold from SI		200		ns
t_{IR+}	Delay, SI HIGH to IR LOW		20	350	ns
t_{IR-}	Delay, SI LOW to IR HIGH		20	450	ns
t_{PHSO}	SO HIGH Time		80		ns
t_{PLSO}	SO LOW Time		80		ns
t_{OR+}	Delay, SO HIGH to OR LOW		20	370	ns
t_{OR-}	Delay, SO LOW to OR HIGH		20	450	ns
t_{DA}	Data Setup to OR HIGH		0		ns
t_{DH}	Data Hold from OR LOW		75		ns
t_{BT}	Bubble through Time			1	μs
t_{MRW}	$\overline{MR}$ Pulse Width		400		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		30		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			400	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			400	ns

Notes:

3. Test conditions assume signal transitions of 10 ns or less. Timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
4. $1/f_{MAX} > t_{PHSI} + t_{IR-}$, $1/f_{MAX} > t_{PHSO} + t_{OR-}$.

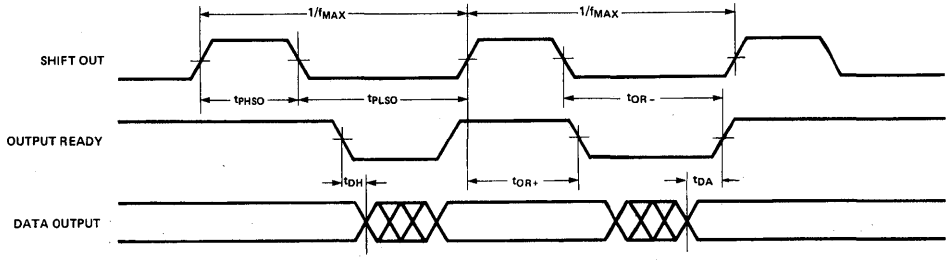
Switching Waveforms

Data In Timing Diagram



0004-6

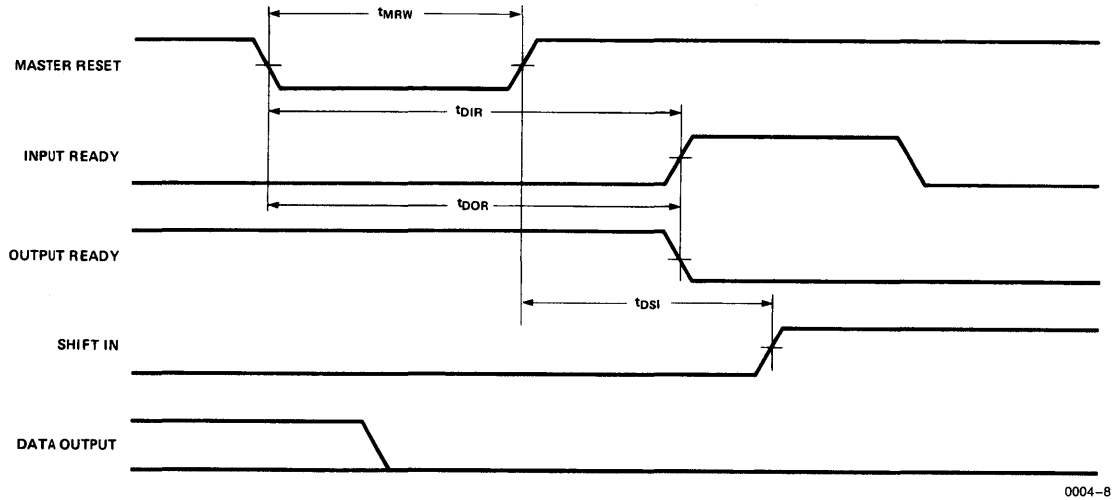
Data Out Timing Diagram



0004-7

Switching Waveforms (Continued)

Master Reset Timing Diagram



0004–8

Ordering Information

Ordering Code	Package Type	Operating Range
CY3341-PC CY3341-DC	P1 D2	Commercial

CY7C401/CY7C403
CY7C402/CY7C404

CYPRESS SEMICONDUCTOR

Cascadeable 64 x 4 FIFO and 64 x 5 FIFO

Features

- **64 x 4 (CY7C401 and CY7C403) 64 x 5 (CY7C402 and CY7C404) High speed first-in first-out memory (FIFO)**
- **Processed with high-speed CMOS for optimum speed/power**
- **25 MHz data rates available on CY7C403 and CY7C404**
- **50 ns bubble-through time— 25 MHz**
- **Expandable in word width and/or length**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Independent asynchronous inputs and outputs**
- **TTL compatible interface**
- **Output enable function available on CY7C402 and CY7C404**
- **Capable of withstanding greater than 2000V electrostatic discharge**
- **Pin compatible with MMI 67401A/67402A and NSC DM87S401A/DM87S402A**

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five bit words. Both the CY7C403 and CY7C404 have an Output Enable (OE) function.

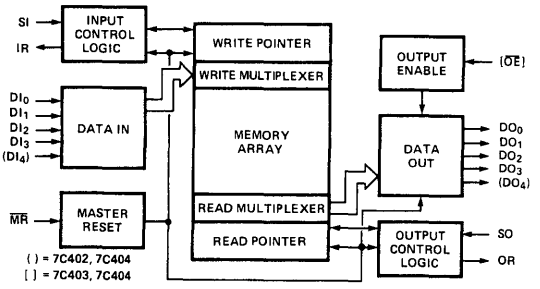
The devices accept 4/5 bit words at the data input (DI_0–DI_n) under the control of the Shift In (SI) input. The stored words stack up at the output (DO_0–DO_n) in the order they were entered. A read command on the Shift Out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The Input Ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The Output Ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

Parallel expansion for wider words is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

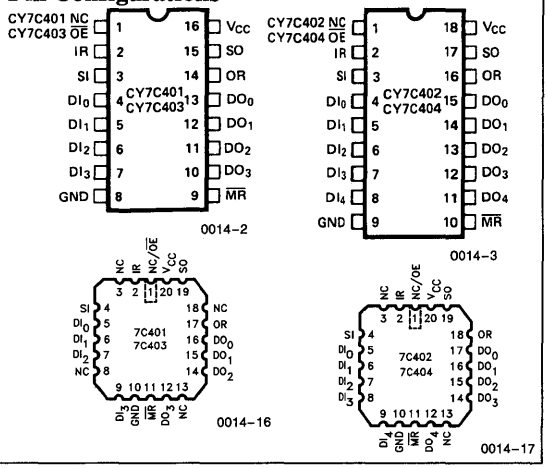
Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device is connected to the Shift In (SI) pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25 MHz operation makes these FIFOs ideal for high speed communication and controller applications.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C40X-10	7C40X-15	7C40X-25
Maximum Shift Rate (MHz)		10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75
	Military	90	90	90

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions		7C40X-10, 15, 25 Min.	7C40X-10, 15, 25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage[2]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

Capacitance

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute air flow.
2. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Load and Waveform

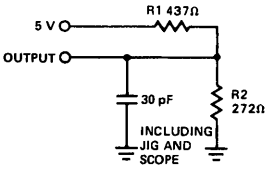
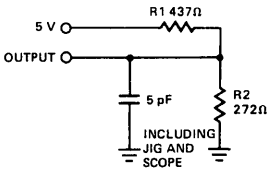
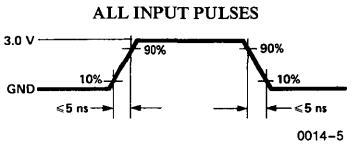


Figure 1a



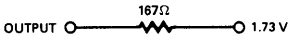
0014–4

Figure 1b



0014–5

Equivalent to: THÉVENIN EQUIVALENT



0014–6

Switching Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions	7C40X-10		7C40X-15		7C403-25 7C404-25		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		23		23		11		ns
t_{PLSI}	SI LOW Time		30		25		29		ns
t_{SSI}	Data Setup to SI	Note 6	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 6	40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			40		35		21	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			45		40		28	ns
t_{PHSO}	SO HIGH Time		23		23		11		ns
t_{PLSO}	SO LOW Time		25		25		29		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			40		35		19	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			55		40		34	ns
t_{SOR}	Data Setup to OR HIGH		2		2		2		ns
t_{HSO}	Data Hold from SO LOW		10		10		10		ns
t_{BT}	Bubble through Time		10	90	10	65	10	50	ns
t_{SIR}	Data Setup to IR	Note 7	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 7	30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		23		23		15		ns
t_{POR}	Output Ready Pulse HIGH		23		23		15		ns
t_{PMR}	MR Pulse Width		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			40		35		25	ns
t_{DIR}	MR LOW to IR HIGH			40		35		25	ns
t_{LZMR}	MR LOW to Output LOW	Note 8		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			35		30		20	ns
t_{HZOE}	Output HIGH-Z from OE HIGH	Note 9		30		25		15	ns

Notes:

4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a*.
5. $I/f_O > t_{PHSI} + t_{DHIR}$, $I/f_O > t_{PHSO} + t_{DHOR}$
6. t_{SSI} and t_{HSI} apply when memory is not full.
7. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble through (t_{BT}) conditions exist.
8. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
9. HIGH-Z transitions are referenced to the steady-state $V_{OH} - 500$ mV and $V_{OL} + 500$ mV levels on the output. t_{HZOE} is tested with 5 pF load capacitance as in *Figure 1b*.

5

Operational Description

CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The Output Enable ($\overline{OE}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs (DO_0–DO_n) will be in a LOW state.

SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

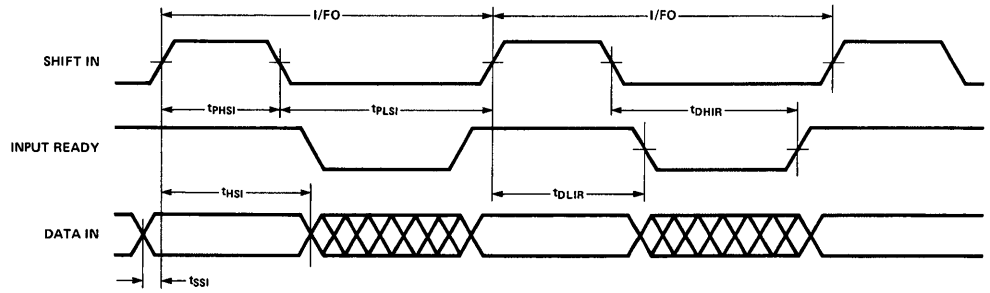
BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

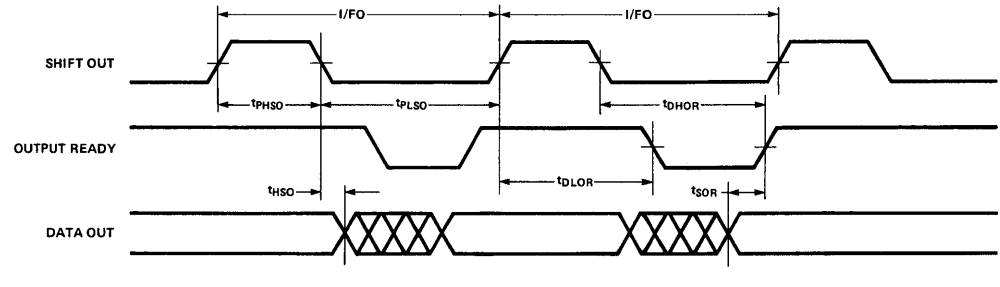
Switching Waveforms

Data In Timing Diagram



0014–7

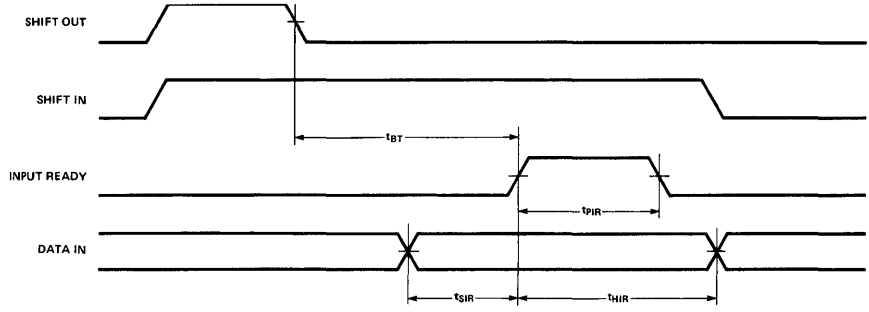
Data Out Timing Diagram



0014–8

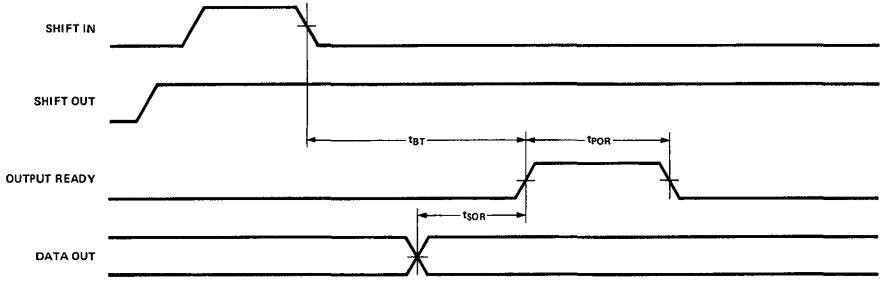
Switching Waveforms (Continued)

Bubble Through, Data Out To Data In Diagram



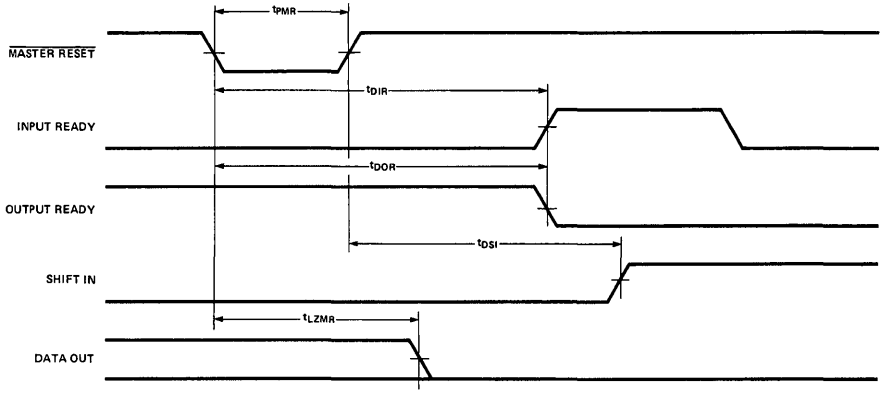
0014-9

Bubble Through, Data In To Data Out Diagram



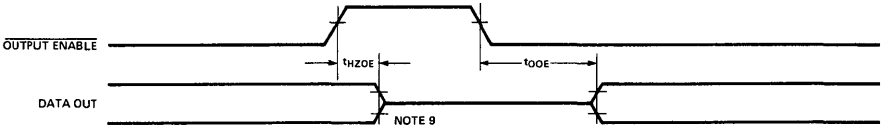
0014-10

Master Reset Timing Diagram



0014-11

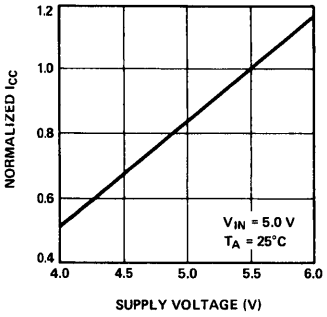
Output Enable Timing Diagram



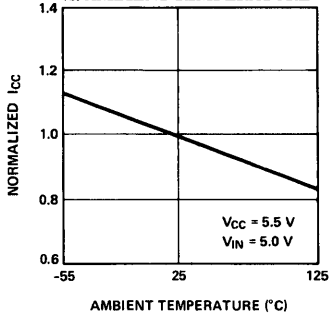
0014-12

Typical DC and AC Characteristics

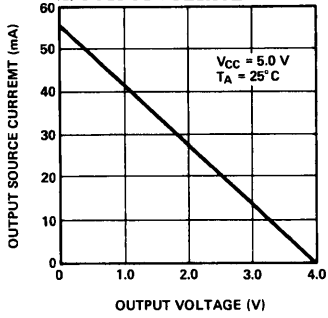
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



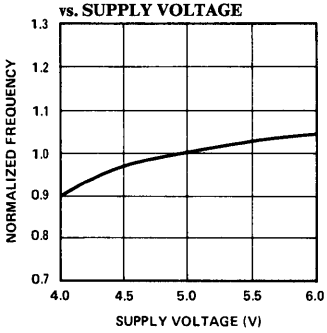
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



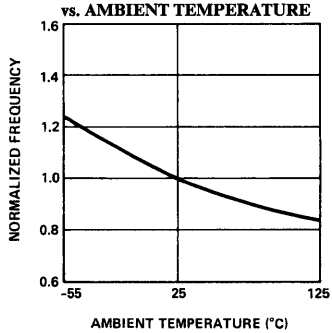
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



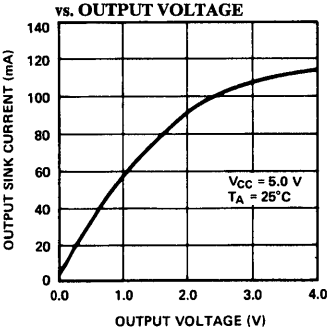
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



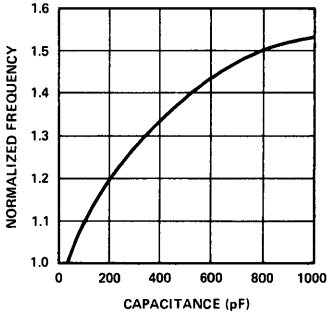
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



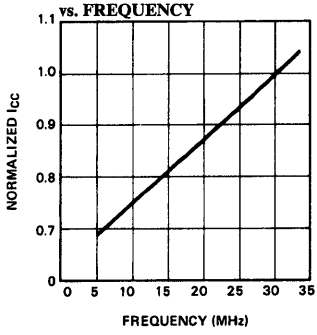
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



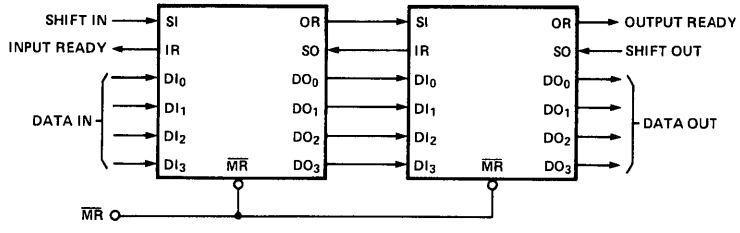
NORMALIZED ICC vs. FREQUENCY



0014–13

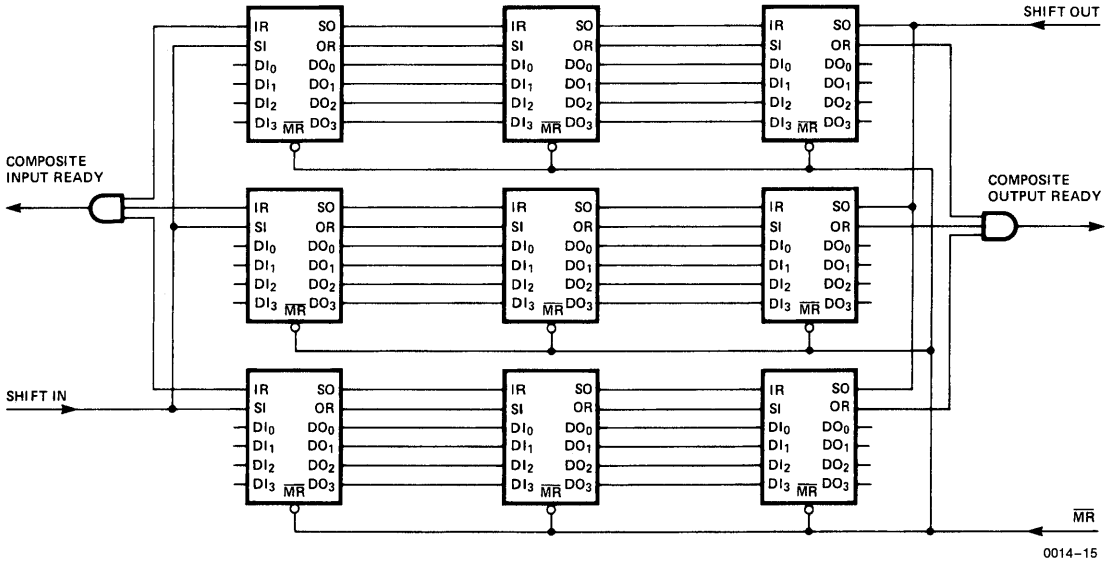
FIFO Expansion

128 x 4 Application



FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

192 x 12 Application



FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with pin-compatible FIFO's from other manufacturers.

Ordering Information

Ordering Code (25 MHz)	Package Type	Operating Range
CY7C403-25PC	P1	Com.
CY7C404-25PC	P3	
CY7C403-25DC	D2	
CY7C404-25DC	D4	
CY7C403-25LC	L61	
CY7C404-25LC	L61	
CY7C403-25DMB	D2	Mil.
CY7C404-25DMB	D4	
CY7C403-25LMB	L61	
CY7C404-25LMB	L61	

Ordering Code (15 MHz)	Package Type	Operating Range
CY7C401-15PC	P1	Com.
CY7C402-15PC	P3	
CY7C403-15PC	P1	
CY7C404-15PC	P3	
CY7C401-15DC	D2	
CY7C402-15DC	D4	
CY7C403-15DC	D2	
CY7C404-15DC	D4	
CY7C401-15LC	L61	
CY7C402-15LC	L61	
CY7C403-15LC	L61	
CY7C404-15LC	L61	
CY7C401-15DMB	D2	Mil.
CY7C402-15DMB	D4	
CY7C403-15DMB	D2	
CY7C404-15DMB	D4	
CY7C401-15LMB	L61	
CY7C402-15LMB	L61	
CY7C403-15LMB	L61	
CY7C404-15LMB	L61	

Ordering Code (10 MHz)	Package Type	Operating Range
CY7C401-10PC	P1	Com.
CY7C402-10PC	P3	
CY7C403-10PC	P1	
CY7C404-10PC	P3	
CY7C401-10DC	D2	
CY7C402-10DC	D4	
CY7C403-10DC	D2	
CY7C404-10DC	D4	
CY7C401-10LC	L61	
CY7C402-10LC	L61	
CY7C403-10LC	L61	
CY7C404-10LC	L61	
CY7C401-10DMB	D2	Mil.
CY7C402-10DMB	D4	
CY7C403-10DMB	D2	
CY7C404-10DMB	D4	
CY7C401-10LMB	L61	
CY7C402-10LMB	L61	
CY7C403-10LMB	L61	
CY7C404-10LMB	L61	

CYPRESS SEMICONDUCTOR

CY7C901

CMOS Four-Bit Slice

Features

- **Fast**
  CY7C901-31 has a 31 ns (Min.) Clock Cycle; Commercial
  CY7C901-32 has a 32 ns (Min.) Clock Cycle; Military
- **Low Power**
  I_{CC} (Max.) = 70 mA; Commercial
  I_{CC} (Max.) = 90 mA; Military
- **V_{CC} Margin**
  5V ±10%
  All parameters guaranteed over commercial and military operating temperature range
- **Eight Function ALU**
  Performs eight operations on two 4-bit operands
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Four Status Flags**
  Carry, overflow, negative, zero
- **ESD Protection**
  Capable of withstanding greater than 2000V static discharge voltage
- **Pin Compatible and Functional Equivalent to AM2901B, C**

Functional Description

The CY7C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

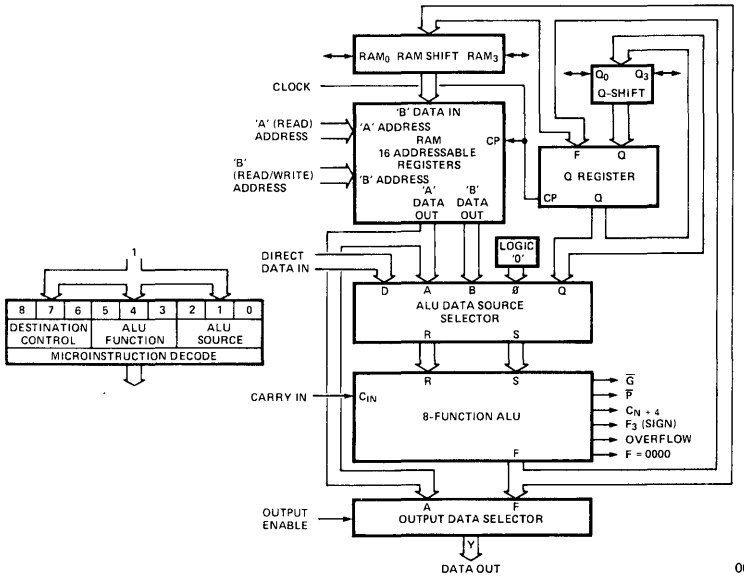
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from a microinstruction register.

The CY7C901 is expandable in 4-bit increments, has three-state data outputs as well as flag output, and can use either a full look ahead carry or a ripple carry.

The CY7C901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY7C901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance with low power dissipation.

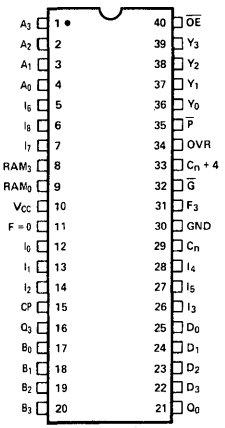
Logic Block Diagram



0030-1

Pin Configuration

Top View



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Selection Guide See last page for ordering information.

Clock Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
31	70	Commercial	CY7C901-31
32	90	Military	CY7C901-32
69	70	Commercial	CY7C901-69
88	90	Military	CY7C901-88

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) .....30 mA

Static Discharge Voltage .....>2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current (Outputs).....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
A_0–A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0–B_3	I	These 4 address lines select one of the registers in the stack and output is contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0–I_8	I	These 9 instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$) and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
D_0–D_3	I	These are 4 data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
Y_0–Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the Y_0–Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock Input. The LOW level of the clock write data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.
Q_3 RAM_3 (Cont.)	I/O	**Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM 3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}$, $\overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4-bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open collector output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.

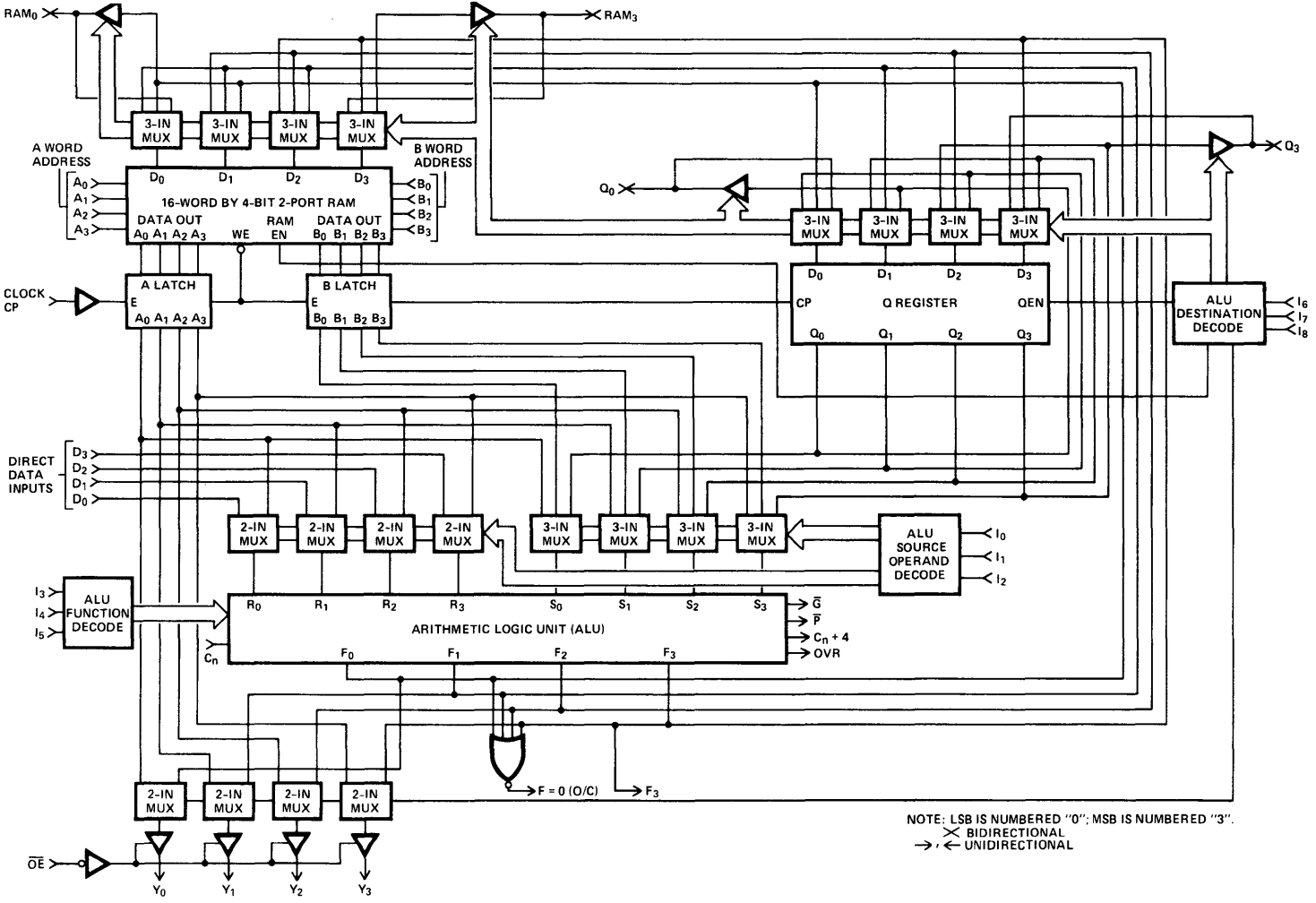


Figure 1. CY7C901 Block Diagram

Functional Tables

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R ⊻ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Figure 3. ALU Function Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	$\overline{F_0}$	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	$\overline{F_0}$	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
A = Register Addressed by A inputs.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control

	I_{210} Octal	0	1	2	3	4	5	6	7
Octal I_{543}	ALU Source / ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_{n+H}	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A⊻Q	A⊻B	Q	B	A	D⊻A	D⊻Q	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Figure 5. Source Operand and ALU Function Matrix

Description of Architecture

General Description

A block diagram of the CY7C901 is shown in *Figure 1.* The circuit is a 4-bit slice consisting of a register file (16 x 4 dual port RAM), the ALU, the Q register and the necessary control logic. It is expandable in 4-bit increments.

RAM

The RAM is addressed by two 4-bit address fields (A_0–A_3, B_0–B_3) that cause the data to appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

New data is written into the RAM location specified by the B address when the RAM write enable (RAM EN) is active and the clock input is LOW. Each of the four RAM inputs is driven by a 3-input multiplexer that allows the outputs of the ALU ($F_{0, 1, 2, 3}$,) to be shifted one bit position to the left, the right, or not to be shifted. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins.

For a shift left (up) operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. For a shift right (down) operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled.

The data to be written into the RAM is applied to the D inputs of the CY7C901 and is passed (unchanged) through the ALU to the RAM location addressed by the A or B word address.

The outputs of the RAM A and B ports drive separate 4-bit latches that are enabled (follow the RAM data) when the clock is HIGH. The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU ($R_{0, 1, 2, 3}$) and ($S_{0, 1, 2, 3}$) and the ($Y_{0, 1, 2, 3}$) chip outputs.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from four 2-input multiplexers whose inputs are from either the (RAM) A-port or the external data (D) inputs. The S inputs are driven from four 3-input multiplexers whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the $I_{0, 1, 2}$ inputs as shown in *Figure 2.* This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A, B, D, Q and "0" (unselected) inputs as 4-bits operands to the ALU. The logical and arithmetic operations performed by the ALU upon the data present at its R and S inputs are tabulated in *Figure 3.* The ALU has a carry-in (C_n) input, carry-propagate ($\overline{P}$) output, carry-generate ($\overline{G}$) output, carry-out ($C_n + 4$) and overflow (OVR) pins to enable the user to (1) speed up arithmetic operations by implementing carry look-ahead logic and (2) determine if an arithmetic overflow has occurred.

The ALU data outputs ($F_{0, 1, 2, 3}$) are routed to the RAM, the Q register inputs and the Y outputs under control of the $I_{6, 7, 8}$ control signal inputs as shown in *Figure 4.* In addition, the MSB of the ALU is output as F3 so that the user can examine the sign bit without enabling the three-state outputs. An open-collector output, $F = 0$, is provided that is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so that the user can determine when the ALU output is zero by wire ORing similar outputs together.

Q Register

The Q register functions as an accumulator or temporary storage register. Physically it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from four 3-input multiplexers under control of the $I_{6, 7, 8}$ inputs. The Q_0 and Q_3 I/O pins function in a manner similar to the RAM_0 and RAM_3 pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is LOW and transferred from master to slave (output) when the clock changes from LOW to HIGH.

ALU Source Operand and ALU Functions

The ALU source operands and ALU function matrix is summarized in *Figure 5* and separated by logic operation or arithmetic operation in *Figures 6* and *7*, respectively. The $I_{0, 1, 2}$ lines select eight pairs of source operands and the $I_{3, 4, 5}$ lines select the operation to be performed. The carry-in (C_n) signal affects the arithmetic result and the internal flags; not the logical operations.

5

Conventional Addition and Pass-Increment/ Decrement

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation.

Octal I_{543}, I_{210}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee Q$
60	EX-OR	$A \veebar Q$
61		$A \veebar B$
65		$D \veebar A$
66		$D \veebar Q$
70	EX-NOR	$\overline{A \veebar Q}$
71		$\overline{A \veebar B}$
75		$\overline{D \veebar A}$
76		$\overline{D \veebar Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Figure 6. ALU Logic Mode Functions

Subtraction

Recall that in two's complement coding -1 is equal to all ones and that in one's complement coding zero is equal to all ones. To convert a positive number to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Figure 7* the symbol $-Q$ represents the two's complement of Q so that the one's complement of Q is then $-Q-1$.

Octal I_{543}, I_{210}	C_n = 0 (Low)		C_n = 1 (High)	
	Group	Function	Group	Function
00	ADD	A+Q	ADD plus one	A+Q+1
01		A+B		A+B+1
05		D+A		D+A+1
06		D+Q		D+Q+1
02	PASS	Q	Increment	Q+1
03		B		B+1
04		A		A+1
07		D		D+1
12	Decrement	Q−1	PASS	Q
13		B−1		B
14		A−1		A
27		D−1		D
22	1's Comp.	−Q−1	2's Comp. (Negate)	−Q
23		−B−1		−B
24		−A−1		−A
17		−D−1		−D
10	Subtract (1's Comp.)	Q−A−1	Subtract (2's Comp.)	Q−A
11		B−A−1		B−A
15		A−D−1		A−D
16		Q−D−1		Q−D
20		A−Q−1		A−Q
21		A−B−1		A−B
25		D−A−1		D−A
26		D−Q−1		D−Q

Figure 7. ALU Arithmetic Mode Functions

Logic Functions for $\overline{G}$, $\overline{P}$, $C_n + 4$, and OVR

The four signals G, P, $C_n + 4$, and OVR are designed to indicate carry and overflow conditions when the CY7C901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to *Figure 2*.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_N+4	OVR
0	R+S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \veebar C_4$
1	S−R	←	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions		→
2	R−S	←	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions		→
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions		→
6	R ⊻ S	←	Same as $\overline{R \veebar S}$, but substitute $\overline{R_i}$ for R_i in definitions		→
7	$\overline{R \veebar S}$	$G_3+G_2+G_1+G_0$	$G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1P_0$	$\overline{G_3+P_3G_2+P_3P_2G_1}$ $+P_3P_2P_1P_0\,(G_0+\overline{C_n})$	See note

Notes:
$[P_2 + G_2P_1 + \overline{G}_2G_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \veebar [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$
+ = OR

Figure 8

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 20 mA Commercial I_{OL} = 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = V_{CC}			10	μA
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = V_{SS}			−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{OH} = 2.4V		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	Commercial Military	20 16		mA mA
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = V_{SS} − V_{CC}		 −40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V			−85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial Military		70 90	mA mA

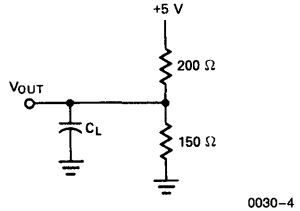
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f= 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

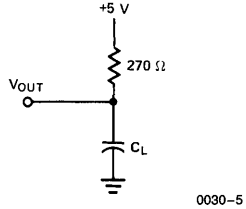
Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested on a sample basis.

Output Loads used for AC Performance Characteristics



All outputs except open drain



Open drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.

CY7C901-31 and CY7C901-69 Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See page 8 for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-31PC CY7C901-31DC CY7C901-31LC
CY7C901-69PC CY7C901-69DC CY7C901-69LC

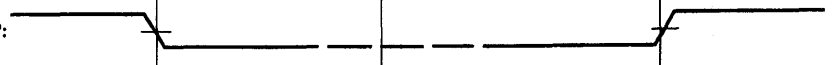
Cycle Time and Clock Characteristics

CY7C901-	31	69
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	31 ns	69 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz	16 MHz
Minimum Clock LOW Time	15 ns	30 ns
Minimum Clock HIGH Time	15 ns	30 ns
Minimum Clock Period	31 ns	69 ns

Combinational Propagation Delays. C_L = 50 pF

To Output / From Input	Y		F_3		$C_n + 4$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
CY7C901-	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**
A, B Address	40	60	40	61	40	59	37	50	40	70	40	67	40	71	—	—
D	30	38	30	36	30	40	30	33	38	48	30	44	30	45	—	—
C_n	22	30	22	29	20	20	—	—	25	37	22	29	25	38	—	—
I_{012}	35	50	35	47	35	45	37	45	37	56	35	53	35	57	—	—
I_{345}	35	51	35	52	35	52	35	45	38	60	35	49	35	53	—	—
I_{678}	25	28	—	—	—	—	—	—	—	—	—	—	26	35	26	35
A Bypass ALU (I = 2XX)	35	37	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↗	35	49	35	48	35	47	35	37	35	58	35	55	35	59	28	29

Set-up and Hold Times Relative to Clock (CP) Input



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C901-	**31**	**69**	**31**	**69**	**31**	**69**	**31**	**69**
A, B Source Address	15	20	1 (Note 3)	0 (Note 3)	30, 15 + t_{PWL} (Note 4)	69 (Note 4)	0	0
B Destination Address	15	15	← Do Not Change			→	0	0
D	—	—	—	—	25	51	0	0
C_n	—	—	—	—	20	39	0	0
I_{012}	—	—	—	—	30	56	0	0
I_{345}	—	—	—	—	30	55	0	0
I_{678}	10	11	← Do Not Change			→	0	0
$RAM_{0,3}, Q_{0,3}$	—	—	—	—	12	16	0	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C901-31	$\overline{OE}$	Y	23	23
CY7C901-69	$\overline{OE}$	Y	35	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

5

CY7C901-32 and CY7C901-88 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military ($-55°C$ to $+125°C$) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See page 8 for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-32DM CY7C901-32LM
CY7C901-88DM CY7C901-88LM

Cycle Time and Clock Characteristics

CY7C901-	32	88
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	32 ns	88 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31 MHz	15 MHz
Minimum Clock LOW Time	15 ns	30 ns
Minimum Clock HIGH Time	15 ns	30 ns
Minimum Clock Period	32 ns	88 ns

Combinational Propagation Delays C_L = 50 pF

To Output / From Input	Y		F_3		$C_n + 4$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
CY7C901-	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**
A, B Address	48	82	48	84	48	80	44	70	48	90	48	86	48	94	—	—
D	37	44	37	38	37	40	34	34	40	50	37	45	37	48	—	—
C_n	25	34	25	32	21	24	—	—	28	38	25	31	28	39	—	—
I_{012}	40	53	40	50	40	47	44	46	44	65	40	55	40	58	—	—
I_{345}	40	58	40	58	40	58	40	48	40	64	40	56	40	55	—	—
I_{678}	29	29	—	—	—	—	—	—	—	—	—	—	29	27	29	27
A Bypass ALU (I = 2XX)	40	50	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↗	40	53	40	50	40	49	40	41	40	63	40	58	40	61	33	31

Set-up and Hold Times Relative to Clock (CP) Input

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C901-	**32**	**88**	**32**	**88**	**32**	**88**	**32**	**88**
A, B Source Address	15	20	1 (Note 3)	0 (Note 3)	30, 15 + t_{PWL} (Note 4)	69 (Note 4)	0	0
B Destination Address	15	15	← Do Not Change			→	0	0
D	—	—	—	—	25	55	0	0
C_n	—	—	—	—	20	42	0	0
I_{012}	—	—	—	—	30	58	0	0
I_{345}	—	—	—	—	30	62	0	0
I_{678}	10	14	← Do Not Change			→	0	0
$RAM_{0,3}$, $Q_{0,3}$	—	—	—	—	12	18	0	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

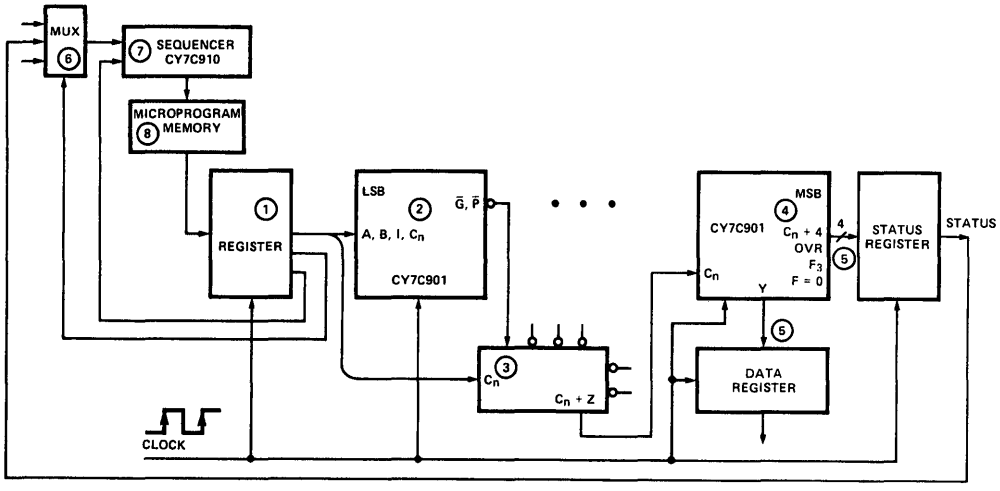
Device	Input	Output	Enable	Disable
CY7C901-32	$\overline{OE}$	Y	25	25
CY7C901-88	$\overline{OE}$	Y	40	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

Minimum Cycle Time Calculations for 16-bit Systems

Speed used in calculations for parts other than CY7C901 are representative for MSI parts.

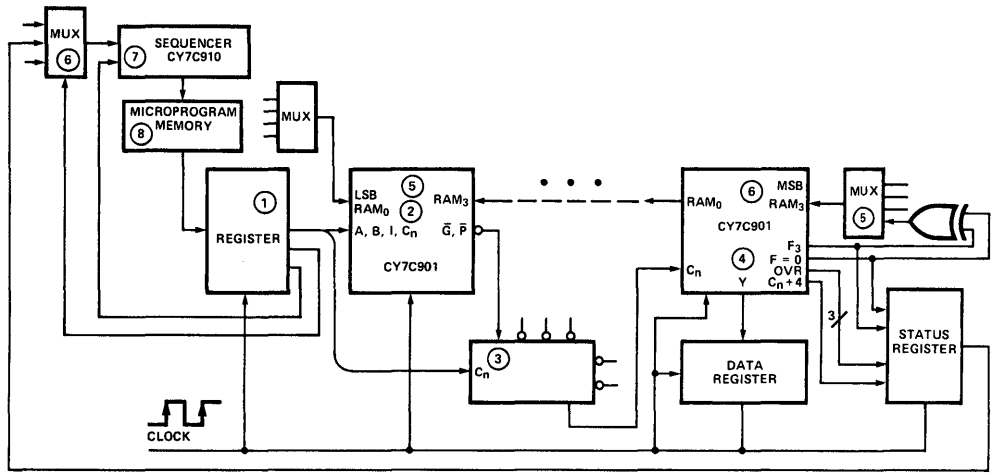


0030-7

Pipelined System. Add without Simultaneous Shift.

		Data Loop				Control Loop	
	① Register	Clock to Output	9		① Register	Clock to Output	9
+	② CY7C901	A, B to $\overline{G}$, $\overline{P}$	37	+	⑥ MUX	Select to Output	13
+	③ Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $C_n + Z$	10	+	⑦ CY7C910	CC to Output	45
+	④ CY7C901	C_n to $C_n + 4$, OVR, F_3, F = 0, Y	25	+	⑧ PROM	Access Time	35
+	⑤ Register	Set-up Time	2	+	① Register	Set-up Time	2
			83 ns				104 ns

Minimum Clock period = 104 ns



0030-8

Pipelined System. Simultaneous Add and Shift Down (RIGHT).

		Data Loop				Control Loop	
	① Register	Clock to Output	9		① Register	Clock to Output	9
+	② CY7C901	A, B to $\overline{G}$, $\overline{P}$	37	+	⑥ MUX	Select to Output	13
+	③ Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $C_n + Z$	10	+	⑦ CY7C910	CC to Output	45
+	④ CY7C901	C_n to F_3, OVR,	25	+	⑧ PROM	Access Time	35
+	⑤ XOR and MUX		21	+	① Register	Set-up Time	2
+	⑥ CY7C901	RAM_3 Set-up	12				104 ns
			114 ns				

Minimum clock period = 114 ns

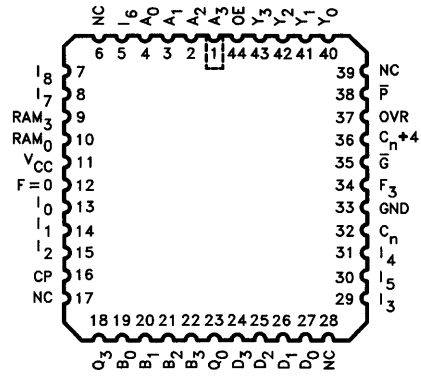
5

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
31	CY7C901-31PC	P17	Commercial
69	CY7C901-69PC	P17	Commercial
31	CY7C901-31DC	D18	Commercial
69	CY7C901-69DC	D18	Commercial
31	CY7C901-31LC	L67	Commercial
69	CY7C901-69LC	L67	Commercial
32	CY7C901-32DMB	D18	Military
88	CY7C901-88DMB	D18	Military
32	CY7C901-32LMB	L67	Military
88	CY7C901-88LMB	L67	Military

Pin Configuration

Top View



0030-9

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7C909
CY7C911

CMOS Micro Program Sequencers

Features

- **Fast**
  - **— CY7C909/11 has a 30 ns (min.) clock to output cycle time; commercial**
  - **— CY7C909/11 has a 40 ns (min.) clock to output cycle time; military**
- **Low Power**
  - **— I_{CC} (max.) = 55 mA; commercial**
  - **— I_{CC} (max.) = 55 mA; military**
- **V_{CC} margin**
  - **— 5 V ± 10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Expandable**
  Infinitely expandable in 4-bit increments
- **ESD Protection**
  Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2909A/AM2911A**

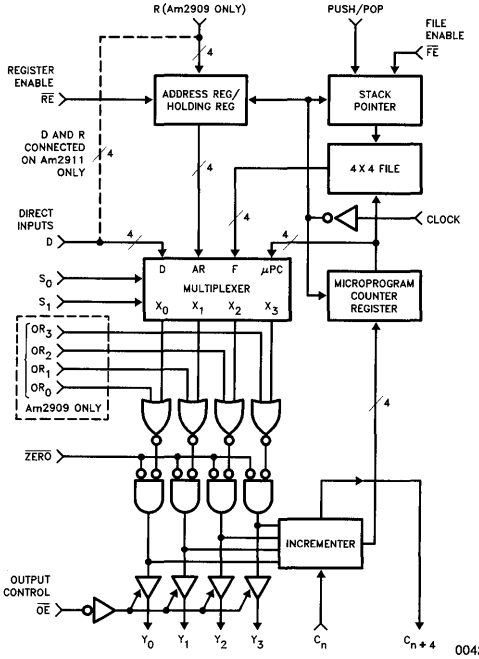
Description

The CY7C909 and CY7C911 are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY7C909 can select an address from any of four sources. They are: 1) a set of four external direct inputs (D_i); 2) external data stored in an internal register (R_i); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be OR'ed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable ($\overline{OE}$) input.

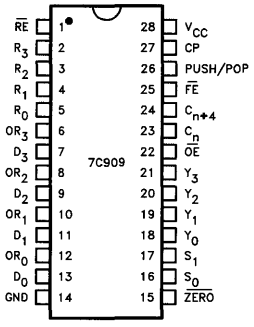
The CY7C911 is an identical circuit to the CY7C909, except the four OR inputs are removed and the D and R inputs are tied together. The CY7C911 is available in a 20-pin, 300-mil package.

Logic Block Diagram

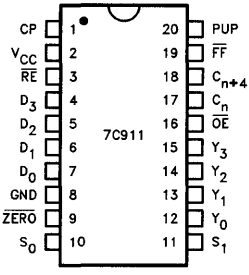


0042-1

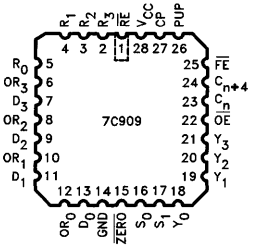
Pin Configurations



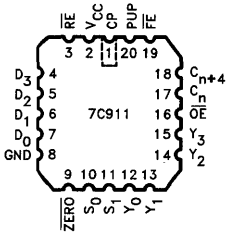
0042-2



0042-3



0042-4



0042-5

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.6 mA (Comm.)		2.4		V
		V_{CC} = Min., I_{OH} = −1.0 mA (Mil.)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−20	+20	μA
I_{OS}	Output Short[2] Circuit Current	V_{CC} = Max.	V_{OUT} = GND	−30	−85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		55	mA
			Military		55	
I_{CC_1}	V_{CC} Operating Supply Current	V_{CC} = Max. V_{IH} ≥ 3.0V, V_{IL} ≤ 0.4V	Commercial		35	mA
			Military		35	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

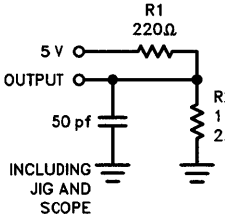
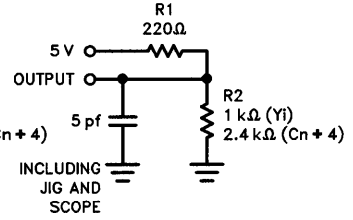
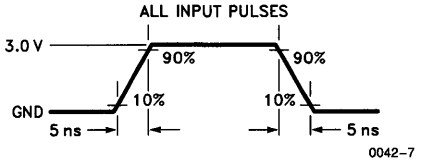


Figure 1a



0042-6

Figure 1b



0042-7

Figure 2

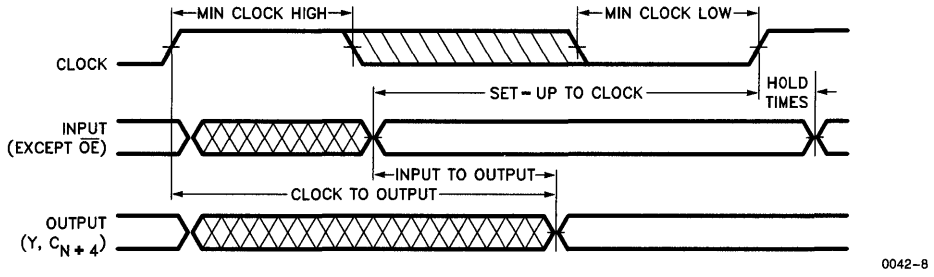
Switching Characteristics Over Operating Range

	7C909-30 7C911-30		7C909-30 7C911-30		7C909-40 7C911-40		7C909-40 7C911-40		Units
	Commercial		Military		Commercial		Military		
Minimum Clock Low Time	**15**		**15**		**20**		**20**		**ns**
Minimum Clock High Time	**15**		**15**		**20**		**20**		**ns**
MAXIMUM COMBINATIONAL PROPAGATION DELAYS									
From Input To:	Y	C_N + 4	Y	C_N +4	Y	C_N + 4	Y	C_N + 4	ns
D_i	16	17	18	20	17	22	20	25	ns
S_0, S_1	17	18	20	21	29	34	29	34	ns
OR_i (7C909)	14	16	16	18	17	22	20	25	ns
C_N	—	13	—	15	—	14	—	16	ns
$\overline{ZERO}$	15	16	17	18	29	34	30	35	ns
$\overline{OE}$ Low to Output	15	—	17	—	25	—	25	—	ns
$\overline{OE}$ High to High Z[4]	15	—	17	—	25	—	25	—	ns
Clock High, S_0, S_1 = LH	19	20	22	23	39	44	45	50	ns
Clock High, S_0, S_1 = LL	19	20	22	23	39	44	45	50	ns
Clock High, S_0, S_1 = HL	23	25	27	29	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)									
From Input	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	
$\overline{RE}$	10	0	11	0	19	4	19	5	ns
R_i [5]	10	0	11	0	10	4	12	5	ns
Push/Pop	10	0	11	0	25	4	27	5	ns
FE	10	0	11	0	25	4	27	5	ns
C_N	10	0	11	0	18	4	18	5	ns
D_i	14	0	16	0	25	0	25	0	ns
OR_i (7C909)	12	0	14	0	25	0	25	0	ns
S_0, S_1	14	0	16	0	25	0	29	0	ns
$\overline{ZERO}$	11	0	12	0	25	0	29	0	ns

Notes:

4. Output Loading as in *Figure 1b*.
5. R_i and D_i are internally connected on the CY7C911. Use R_i set-up and hold times for D_i inputs.

Switching Waveforms



Functional Description

The tables below define the control logic of the 7C909/911. Table 1 contains the Multiplexer Control Logic which selects the address source to appear on the outputs.

Table 1. Address Source Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS
0	L	L	Microprogram Counter (μPC)
1	L	H	Address/Holding Register (AR)
2	H	L	Push-Pop stack (STK)
3	H	H	Direct inputs (D_i)

Control of the Push/Pop Stack is contained in Table 2. FILE ENABLE ($\overline{FE}$) enables stack operations, while Push/Pop (PUP) controls the stack.

Table 2. Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Push current PC into stack increment stack pointer
L	L	pop stack, decrement stack pointer

Table 3 illustrates the Output Control Logic of the 7C909/911. The $\overline{ZERO}$ control forces the outputs to zero. The OR inputs are OR'ed with the output of the multiplexer.

Table 3. Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Table 4 defines the effect of S_0, S_1, $\overline{FE}$ and PUP control signals on the 7C909. It illustrates the Address Source on the outputs and the contents of the Internal Registers for every combination of these signals. The Internal Register contents are illustrated before and after the Clock LOW to HIGH edge.

Table 4

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μ PC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	0000	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End
N + 1	—	J + 1	K	Rb	Rc	Rd	Ra	—		Loop
N	0001	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up
N + 1	—	J + 1	K	J	Ra	Rb	Rc	—		Loop
N	001X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N + 1	—	J + 1	K	Ra	Rb	Rc	Rd	—		
N	0100	J	K	Ra	Rb	Rc	Rd	K	Use AR for Address;	End
N + 1	—	K + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	Loop
N	0101	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR;	JSR AR
N + 1	—	K + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	011X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N + 1	—	K + 1	K	Ra	Rb	Rc	Rd	—		
N	1000	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	RTS
N + 1	—	Ra + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	1001	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	
N + 1	—	Ra + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	101X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref
N + 1	—	Ra + 1	K	Ra	Rb	Rc	Rd	—		(Loop)
N	1100	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	End
N + 1	—	D + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	Loop
N	1101	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	JSR D
N + 1	—	D + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	111X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N + 1	—	D + 1	K	Ra	Rb	Rc	Rd	—		

J = Contents of Microprogram Counter
K = Contents of Address Register
R_a, R_b, R_c, R_d = Contents in Stack

Functional Description (Continued)

Two examples of Subroutine Execution appear below. *Figure 3* illustrates a single subroutine while *Figure 4* illustrates two nested subroutines.

The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the 7C909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to sub-routine at A". At the time T_2, this instruction is in the μWR, and the 7C909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. *Figure 4* is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_6	J+3	-
T_7	J+4	-
	-	-
	-	-
	-	-
	-	-
	-	-
T_3	A	I(A)
T_4	A+1	-
T_5	A+2	RTS
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	-	-	-	J+3	J+3	J+3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

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Figure 3. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_9	J+3	-
	-	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A+1	-
T_5	A+2	JSR B
T_7	A+3	-
T_8	A+4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	-	-	-	J+3	J+3	J+3	A+3	J+3	J+3	-
	STK1	-	-	-	-	-	-	J+3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

0042-10

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

5

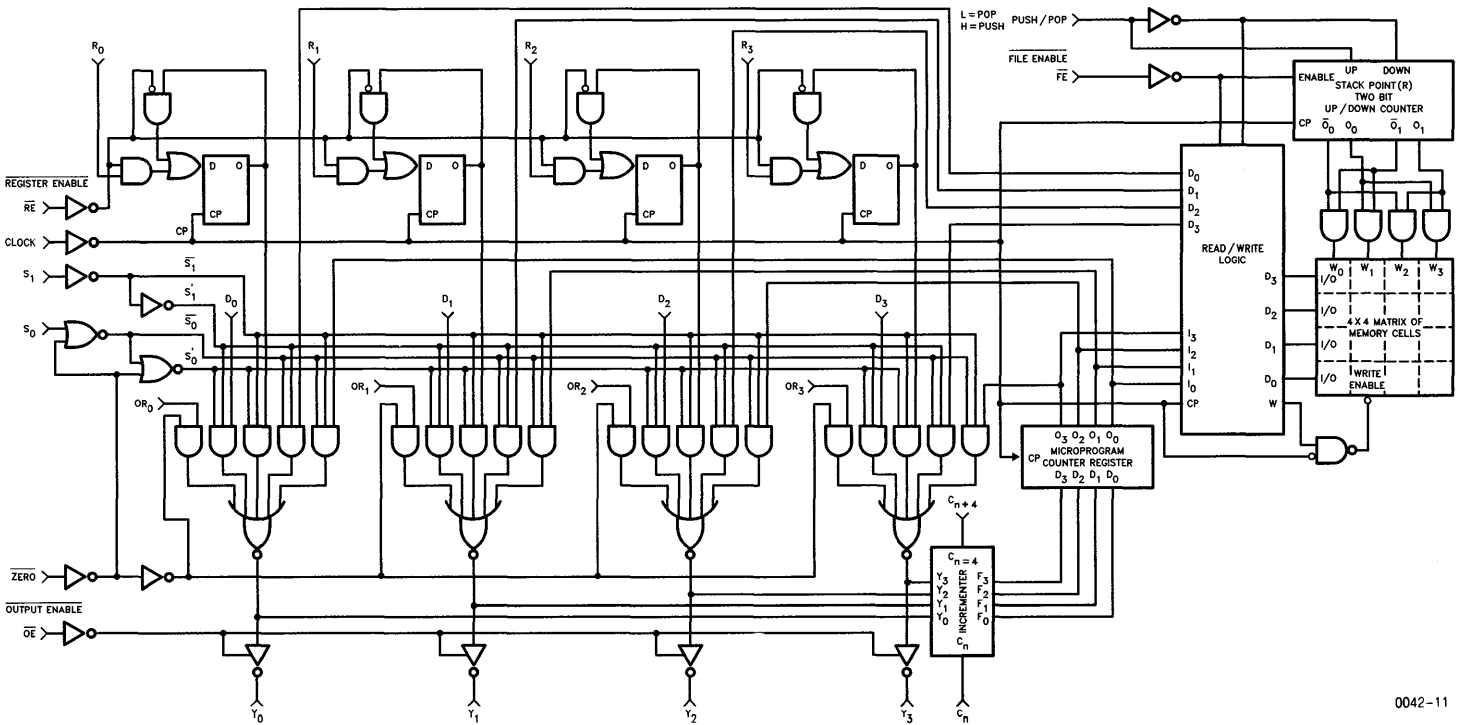


Figure 5. Microprogram Sequencer Block Diagram.

Note:
R_i and D_i connected together and OR_i Inputs removed on CY7C911

Functional Description (Continued)

Architecture

The CY7C909 and CY7C911 are CMOS microprogram sequencers for use in high speed processor applications. They are cascadable in 4-bit increments. Two devices can address 256 words of microprogram, three can address up to 4K words, and so on. The architecture of the CY7C909/911 is illustrated in the logic diagram in *Figure 5*. The various blocks are described below.

Multiplexer

The Multiplexer is controlled by the S_0 and S_1 inputs to select the address source. It selects either the Direct Inputs (D_i), the Address Register (AR), the Microprogram Counter (MPC), or the stack (SP) as the source of the next microinstruction address.

Direct Inputs

The Direct Inputs (D_i) allow addresses from an external source to be output on the Y outputs. On the CY7C911, the direct inputs are also the inputs to the Address Register.

Address Register

The Address Register (AR) consists of four D-type, edge-triggered flip-flops which are controlled by the Register Enable ($\overline{RE}$) input. When Register Enable is LOW, new data is entered into the register on the LOW to HIGH clock transition.

Microprogram Counter

The Microprogram Counter (μPC) is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has a Carry-in (C_n) input and a Carry-out ($C_n + 4$) output to facilitate cascading. The Carry-in input controls the microprogram counter. When Carry-in is HIGH the incrementer counts sequentially. The counter register is loaded with the current Y output plus one ($Y + 1 -> \mu PC$) on the next clock cycle. When Carry-in is LOW the incrementer does not count. The microprogram counter register is loaded with the same Y output ($Y -> \mu PC$) on the next clock cycle.

Stack

The Stack consists of a 4 x 4 memory array and a built-in Stack Pointer (SP) which always points to the last word written. The Stack is used to store return addresses when executing microsubroutines.

The Stack Pointer is an up/down counter controlled by File Enable ($\overline{FE}$) and Push/Pop (PUP) inputs. The File Enable input allows stack operations only when it is LOW. The Push/Pop input controls the stack pointer position.

The PUSH operation is initiated at the beginning of a microsubroutine. Push/Pop is set HIGH while File Enable is kept LOW. The stack pointer is incremented and the memory array is written with the microinstruction address following the subroutine jump that initiated the push.

The POP operation is initiated at the end of a microsubroutine to obtain the return address. Both Push/Pop and File Enable are set LOW. The return address is already available to the multiplexer. The stack pointer is decremented on the next LOW to HIGH clock transition, effectively removing old information from the top of the stack. The stack is configured so that data will roll-over if more than four POPs are performed, thus preventing data from being lost.

The contents of the memory position pointed to by the Stack Pointer is always available to the multiplexer. Stack reference operations can thus be performed without a push or a pop. Since the stack is four words deep, up to four microsubroutines can be nested.

The $\overline{ZERO}$ input resets the four Y outputs to a binary zero state. The OR inputs (7C909 only) are connected to the Y outputs such that any output can be set to a logical one.

The Output Enable ($\overline{OE}$) input controls the Y outputs. A HIGH on Output Enable sets the outputs into a high impedance state.

Definition of Terms

Name	Description
INPUTS	
S_1, S_0	Multiplexer Control Lines, for Access Source Selection
$\overline{FE}$	File Enable, Enables Stack Operation, Active LOW
PUP	Push/Pop, Selects Stack Operation
$\overline{RE}$	Register Enable, Enables Address Register Active LOW
$\overline{ZERO}$	Forces Output to Logical Zero
$\overline{OE}$	Output Enable, Controls Three-State Outputs Active LOW
OR_i	Logic OR Input to each Address Output Line (7C909 only)
C_n	Carry-In, Controls Microprogram Counter
R_i	Inputs to the Internal Address Register
D_i	Direct Inputs to the Multiplexer
CP	Clock Input

Definition of Terms (Continued)

Name	Description
OUTPUTS	
Y_i	Address Outputs
C_{N+4}	Carry-Out from Incrementer
INTERNAL SIGNALS	
μPC	Contents of the Microprogram Counter
AR	Contents of the Address Register
STK0- STK3	Contents of the Push/Pop Stack
SP	Contents of the Stack Pointer
EXTERNAL SIGNALS	
A	Address to the Counter Memory
1(A)	Instruction in Control Memory at Address A
μWR	Contents of the Microword Register at the Output of the Control Memory
T_N	Time Period (Cycle) n

CYPRESS SEMICONDUCTOR

CMOS Microprogram Controller

Features

- **Fast**
  - **— CY7C910–50 has a 50 ns (min.) clock cycle; commercial**
  - **— CY7C910–51 has a 51 ns (min.) clock cycle; military**
- **Low power**
  - **— I_{CC} (max.) = 100 mA**
- **V_{CC} Margin 5V ±10%**
  All parameters guaranteed over commercial and military operating temperature range
- **Sixteen powerful microinstructions**
  The CY7C910 implements 16 instructions that control the execution of the program
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
  The 12-bit wide address path allows 4096 memory locations to be addressed
- **Four sources for addresses**
  The microprogram address can be selected from the microprogram counter (MPC), the branch address bus, the 9-word stack, or the internal holding register
- **Internal loop counter**
  The on-chip, 12-bit, down-counter can be used to count loop iterations for loops of one to 4096 instructions
- **Internal 9-word by 12-bit stack**
  The internal stack can be used for subroutine return address or data storage
- **ESD protection**
  Capable of withstanding over 2000 volts static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2910A**

Functional Description

The CY7C910 is a standalone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

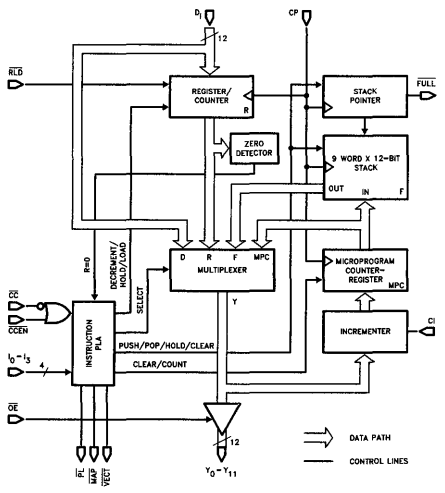
The CY7C910, as illustrated in the block diagram, consists of a 9-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0 to I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY7C910 is a pin compatible, functional equivalent, improved performance replacement for the AM2910A.

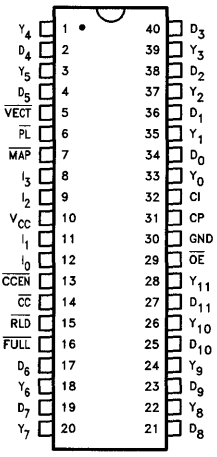
The CY7C910 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

Logic Block Diagram



0041–1

Pin Configuration



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Top View

Block Diagram

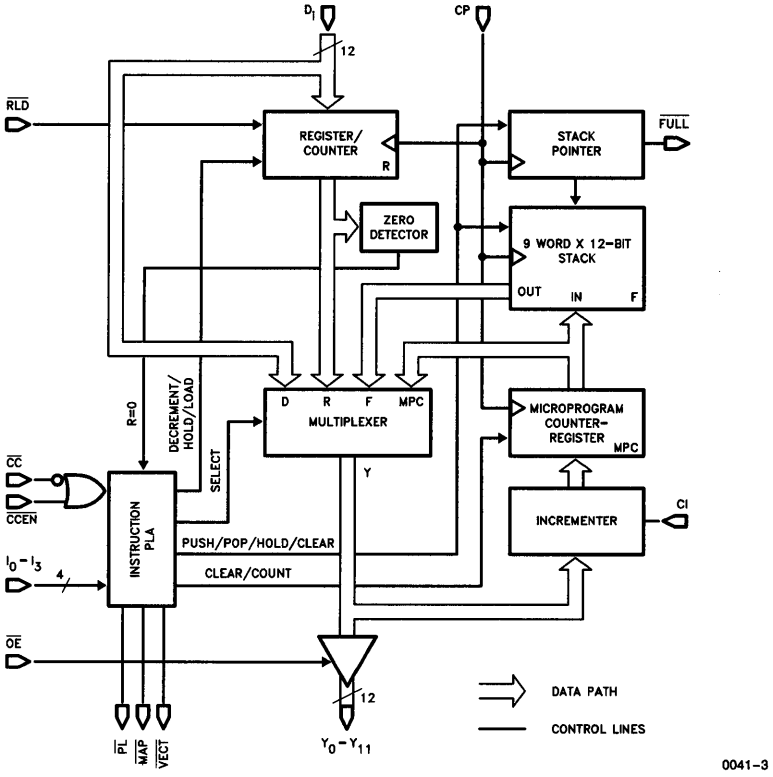


Figure 1

Pin Definitions

Signal Name	I/O	Description
D0–D11	I	Direct inputs to the RC (Register/ Counter) and multiplexer. D0 is LSB and D11 is MSB.
$\overline{\text{RLD}}$	I	Register load. Control input to RC that, when LOW, loads data on the D0–D11 pins into RC on the LOW to HIGH clock (CP) transition.
I0–I3	I	Instruction inputs that select one of sixteen instructions to be performed by the CY7C910.
$\overline{\text{CC}}$	I	Control input that, when LOW, signifies that a test has passed.
$\overline{\text{CCEN}}$	I	Enable for CC input. When HIGH CC is ignored and a pass is forced. When LOW the state of $\overline{\text{CC}}$ is examined.
CP	I	Clock input. All internal states are changed on the LOW to HIGH clock transitions.

Signal Name	I/O	Description
CI	I	Carry input to the LSB of the incrementer for the MPC.
$\overline{\text{OE}}$	I	Control for Y0–Y11 outputs. LOW to enable; High to disable.
Y0–Y11	O	Address output to microprogram memory. Y0 is LSB and Y11 is MSB.
$\overline{\text{FULL}}$	O	When LOW indicates that nine words are in the stack. i.e., the stack is full.
$\overline{\text{PL}}$	O	When LOW selects the pipeline register as the direct input (D0–D11) source.
$\overline{\text{MAP}}$	O	When LOW selects the Mapping PROM (or PLA) as the direct input source.
$\overline{\text{VECT}}$	O	When LOW selects the Interrupt Vector as the direct input source.

Architecture of the CY7C910

Introduction

The CY7C910 is a high performance CMOS microprogram controller that produces a sequence of 12-bit addresses that control the execution of a microprogram. The addresses are selected from one of four sources, depending upon the (internal) instruction being executed (I0–I3), and other external inputs. The sources are (1) the (external) D0–D11 inputs, (2) the RC, (3) the stack and (4) the MPC. Twelve bit lines from each of these four sources are the inputs to a multiplexer, as shown in *Figure 1*, whose outputs are applied to the inputs of the Y0–Y11 three-state output drivers.

External Inputs: D0–D11

The external inputs are used as the source for destination addresses for the jump or branch type of instructions. These are shown as Ds in the two columns in the Table of Instructions. A second use of these inputs is to load the RC.

Register Counter: RC

The RC is implemented as 12 D-type, edge-triggered flip-flops that are synchronously clocked on the LOW to HIGH transition of the clock, CP. The data on the D inputs is synchronously loaded into the RC when the load control input, RLD, is LOW. The output of the RC is available to the multiplexer as its R input and is output on the Y outputs during certain instructions, as shown by R in the Table of Instructions.

The RC is operated as a 12-bit down counter and its contents decremented and tested if zero during instructions 8, 9 and 15. This enables micro-instructions to be repeated many (up to 4096) times. The RC is arranged such that if it is loaded with a number, N, the sequence will be executed exactly N + 1 times.

The Stack and Stack Pointer: SP

The 9-word by 12-bit stack is used to provide return addresses from micro-subroutines or from loops. Intergal to it is a SP, which points to (addresses) the last word written. This permits reference to the data on the top of the stack without having to perform a POP operation.

The SP operates as an up/down counter that is incremented when a PUSH operation (instructions 1, 4 or 5) is performed or decremented when a POP operation (instructions 8, 10, 11, 13 or 15) is performed. The PUSH operation writes the return address on the stack and the POP operation effectively removes it. The actual operation occurs on the LOW to HIGH clock transition following the instruction.

The stack is initialized by executing instruction zero (JUMP TO LOCATION 0 or RESET). Every time a "jump to subroutine" instruction (1, 5) or a loop instruction (4) is executed, the return address is PUSHed onto the stack; and every time a "return from subroutine (or loop)" instruction is executed, the return address is POPed off the stack.

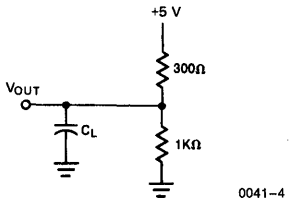
When one subroutine calls another or a loop occurs within a loop (or a combination), which is called nesting, the depth of the stack increases. The physical stack depth is 9-words. When this depth occurs, the $\overline{\text{FULL}}$ signal goes LOW on the next LOW to HIGH clock transition. Any further PUSH operations on a full stack will cause the data at that location to be over-written, but will not increment the SP. Similarily, performing a POP operation on a empty stack will not decrement the SP and may result in non-meaningful data being available at the Y outputs.

The Microprocessor Counter: MPC

The MPC consists of a 12-bit incrementer followed by a 12-bit register. The register usually holds the address of the instrution being fetched. When sequential instructions are fetched, the carry input (CI) to the incrementer is HIGH and one is added to the Y outputs of the multiplexer, which is loaded into the MPC on the next LOW to HIGH clock transition. When the CI input is LOW, the Y outputs of the multiplexer are loaded directly into the MPC, so that the same instruction is fetched and executed.

Output Load used for AC Performance Characteristics

All Outputs



Notes:
1. C_L = 50 pF includes scope probe, writing and stray capacitance.
2. C_L = 5 pF for output disable tests.

Selection Guide

CLOCK CYCLE (Min.) in ns	STACK DEPTH	OPERATING RANGE	PART NUMBER
50	9 words	Commercial	CY7C910-50
51	9 words	Military	CY7C910-51
93	5 words	Commercial	CY7C910-93
100	5 words	Military	CY7C910-100

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latchup Current (Outputs)..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 12 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = V_{SS}		−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{IH} = 2.4V	−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	12		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = V_{SS}-V_{CC}	−40	+40	μA μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	V_{CC} = Max.		100	mA

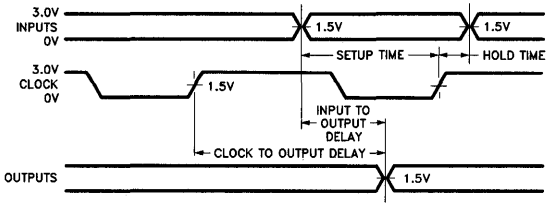
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
2. Tested on a sample basis.

Switching Waveforms



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Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY7C910 over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements (Note 1)

	Commercial		Military	
CY7C910-	50	93	51	100
Minimum Clock LOW	20	50	25	58
Minimum Clock HIGH	20	35	25	42
Minimum Clock Period I = 14	50	93	51	100
Minimum Clock Period I = 8, 9, 15 (Note 2)	50	113	50	114
		123		125

Combinational Propagation Delays. C_L = 50 pF

To Output	Commercial						Military					
From Input	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$	
CY7C910-	50	93	50	93	50	93	51	100	51	100	51	100
D0–D11	20	20	—	—	—	—	25	25	—	—	—	—
I0–I3	35	50	30	51	—	—	40	54	35	58	—	—
$\overline{CC}$	30	30	—	—	—	—	36	35	—	—	—	—
$\overline{CCEN}$	30	30	—	—	—	—	36	37	—	—	—	—
CP I = 8, 9, 15 (Note 2)	40	75	—	—	31	60	—	77	—	—	35	67
		85				60		98				67
CP All Other I	40	55	—	—	31	60	46	61	—	—	35	67
$\overline{OE}$	25	35	—	—	—	—	25	40	—	—	—	—
(Note 3)	37	30					30	30				

Minimum Set-up and Hold Times Relative to clock LOW to HIGH Transition. C_L = 50 pF

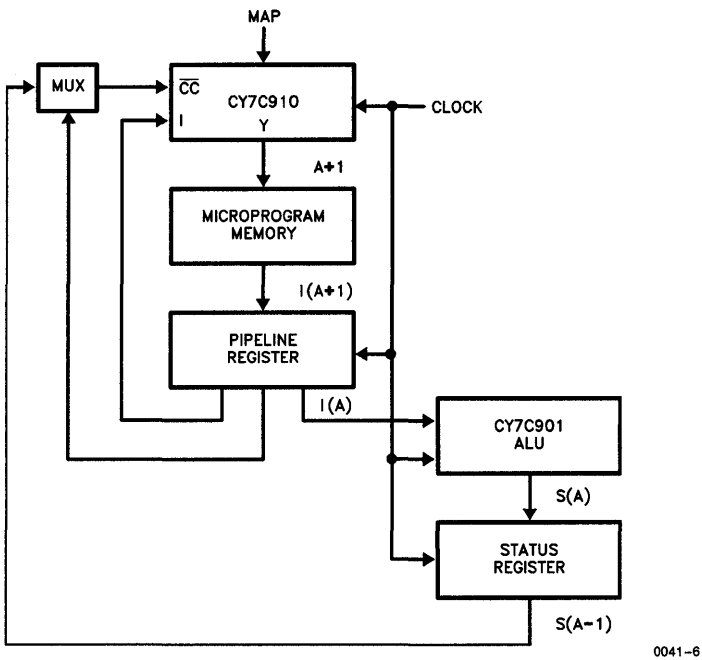
	Commercial				Military			
Input	Set-up		Hold		Set-up		Hold	
CY7C910-	50	93	50	93	50	93	50	93
DI → RC	16	24	0	6	16	28	0	6
DI → MPC	30	58	0	4	30	62	0	4
I0–I3	35	75	0	0	38	81	0	0
$\overline{CC}$	24	63	0	0	35	65	0	0
$\overline{CCEN}$	24	63	0	0	35	63	0	0
CI	18	46	0	5	18	58	0	5
$\overline{RLD}$	19	36	0	6	20	42	0	6

Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.
2. These instructions are dependent upon the register/counter. Use the shorter delay times if the previous instruction either does not change the register/counter or could only decrement it. Use the longer delay if the instruction prior to the clock was 4 or 12 or if RLD was LOW.
3. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C_L = 5 pF.

One Level Pipeline Based Architecture

(Recommended)



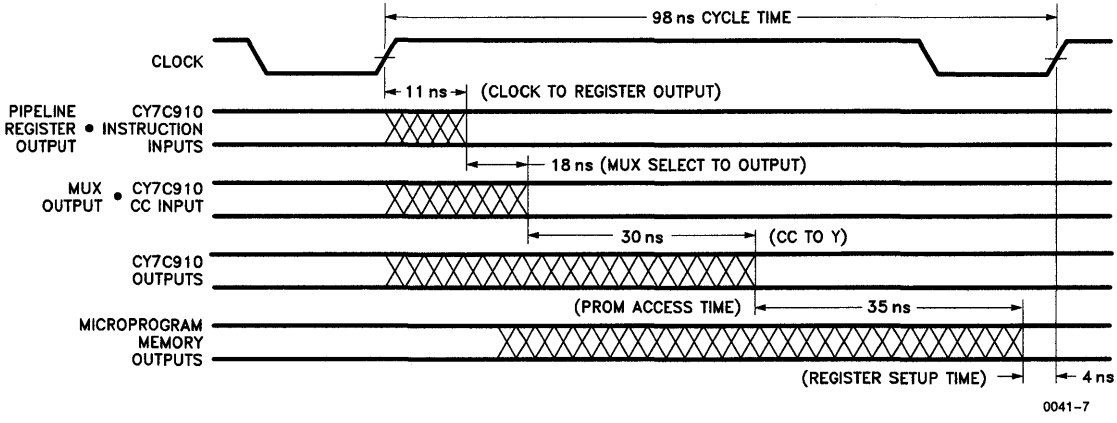


Table of Instructions

I_3–I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	RESULT					
				FAIL $\overline{CCEN}$ = L and $\overline{CC}$ = H		PASS $\overline{CCEN}$ = H or $\overline{CC}$ = L		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 1)	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	POP	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

Notes:
1. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load.

H = HIGH L = LOW X = Don't Care

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
50	CY7C910-50PC	P17	Commercial
93	CY7C910-93PC	P17	Commercial
50	CY7C910-50DC	D18	Commercial
93	CY7C910-93DC	D18	Commercial
50	CY7C910-50LC	L67	Commercial
93	CY7C910-93LC	L67	Commercial
51	CY7C910-51DMB	D18	Military
100	CY7C910-100DMB	D18	Military
51	CY7C910-51LMB	L67	Military
100	CY7C910-100LMB	L67	Military

CYPRESS SEMICONDUCTOR

Low Power CMOS Four-Bit Slice

Features

- **Fast**
  - **— CY8C901-31 has a 31 ns (min.) clock cycle**
- **Automatic standby mode**
- **Low power**
  - **— I_{CC} (max.) = 26.5 mA**
  - **— I_{CCSB} (max.) = 10 mA**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial 0°C to 70°C operating temperature range**
- **Eight function ALU**
  Performs eight operations on two 4-bit operands
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Four status flags**
  Carry, overflow, negative, zero
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2901B, C**

Functional Description

The CY8C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY8C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY8C901 is illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

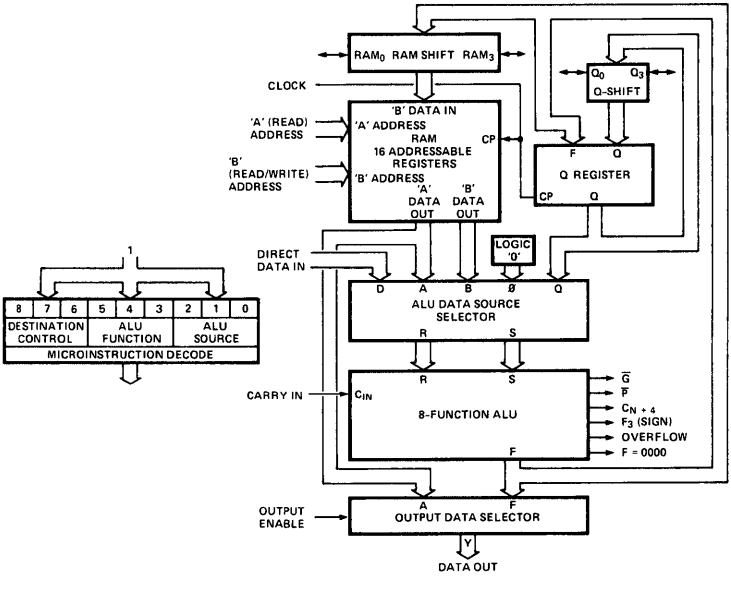
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from a microinstruction register.

The CY8C901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full-look ahead carry or a ripple carry.

The CY8C901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY8C901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance at a low power dissipation.

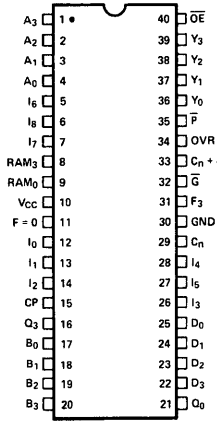
Logic Block Diagram



0039-1

Pin Configuration

Top View



0039-2

Selection Guide

Clock Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
31	26.5	Commercial	CY8C901-31
69	26.5	Commercial	CY8C901-69

Electrical Characteristics Over Commercial and Military Operating Range

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA	2.4		V
		I_{OH} = −100 μA	V_{CC}−1.2		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20 mA		0.4	V
V_{IH}	Input HIGH Voltage		V_{CC}−1.6	V_{CC}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = V_{SS}		−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V	−3.2		mA
		V_{OH} = V_{CC}−1.2V	−100		μA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	20		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = V_{SS}−V_{CC}	 −40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	V_{CC} = Max., V_{IH} ≥ V_{CC}−1.2V 10 MHz V_{IL} ≥ 0.4V		26.5	mA
I_{CCSB}	Standby Current	V_{CC} = Max. D.C., V_{IH} = V_{CC} V_{IL} ≤ 0.4V		10	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested on a sample basis.

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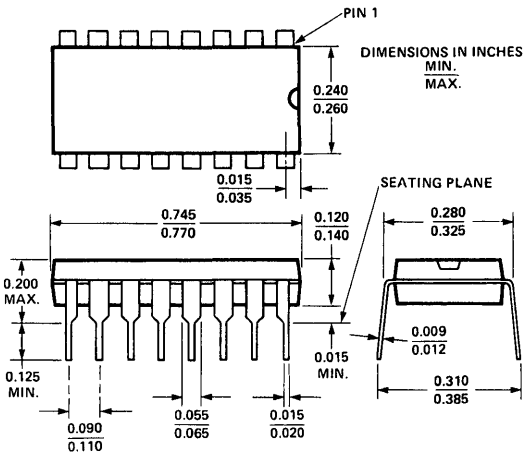
Section Contents

APPENDICES

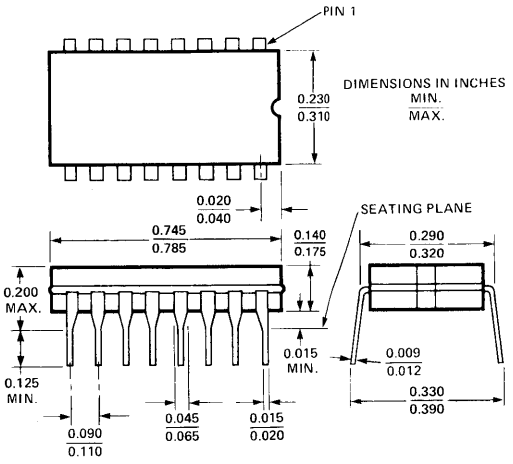
CYPRESS SEMICONDUCTOR

Appendix A: Package Diagrams

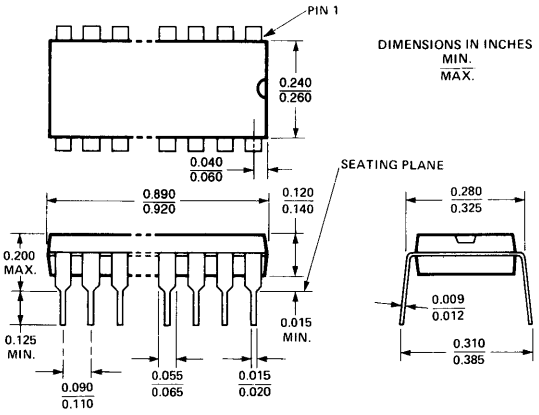
16 Lead (300 MIL) Molded DIP P1



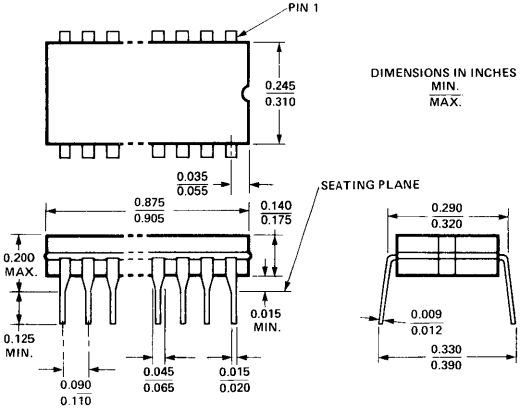
16 Lead (300 MIL) Cerdip D2



18 Lead (300 MIL) Molded DIP P3



18 Lead (300 MIL) Cerdip D4



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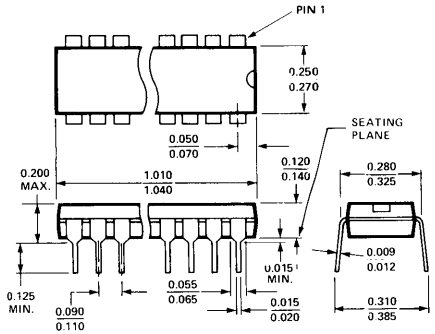
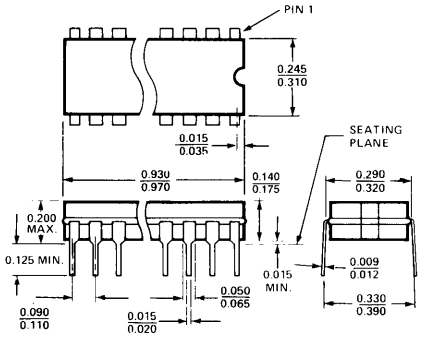
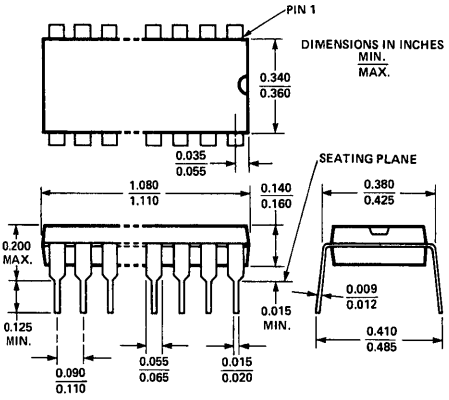
20 Lead Molded DIP P5



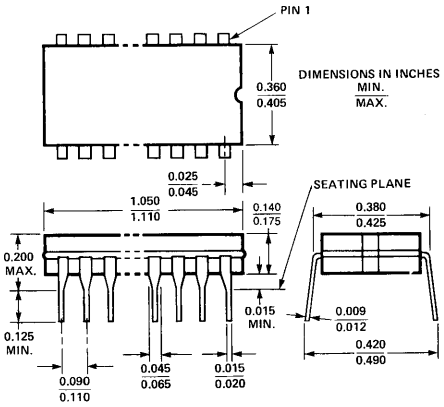
20 Lead Cerdip D6



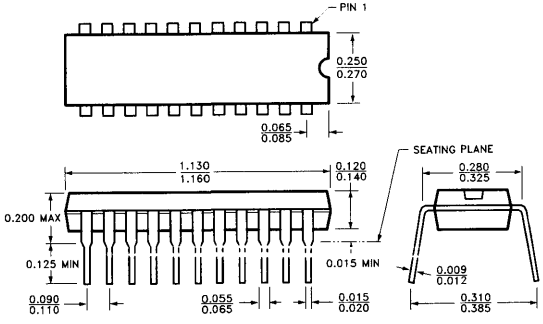
22 Lead (400 MIL) Molded DIP P7



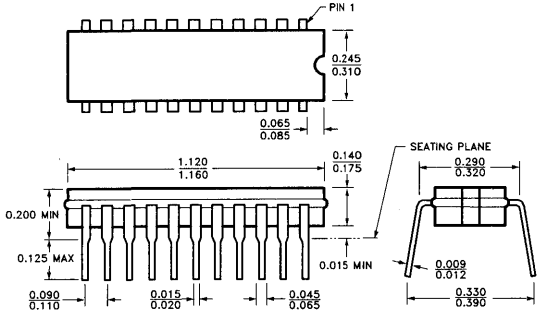
22 Lead (400 MIL) Cerdip D8



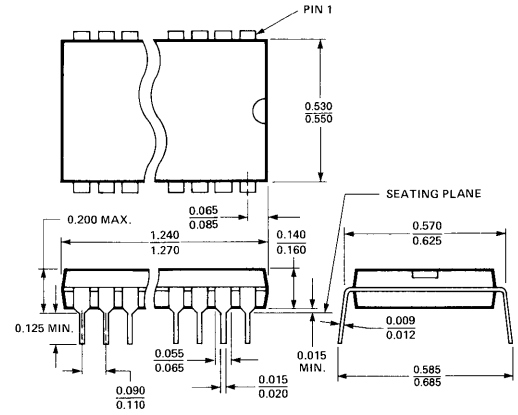
22 Lead (300 MIL) Molded DIP P9



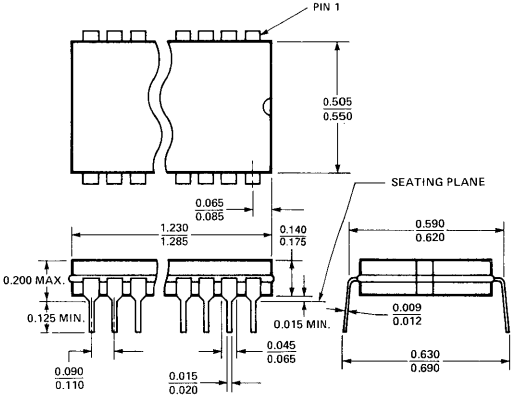
22 Lead (300 MIL) Cerdip D10



24 Lead (600 MIL) Molded DIP P11



24 Lead (600 MIL) Cerdip D12



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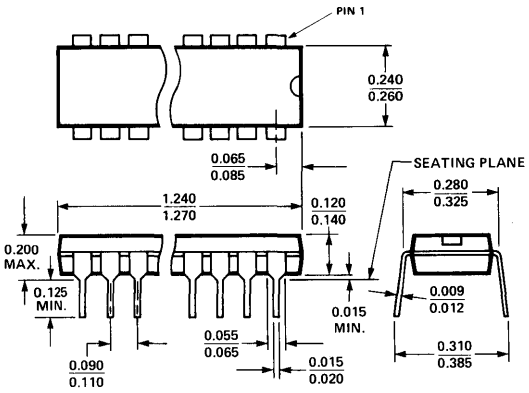
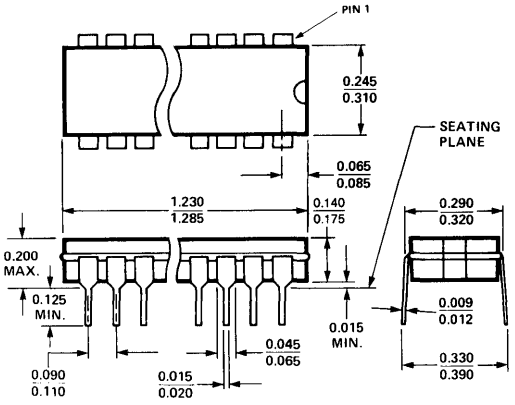
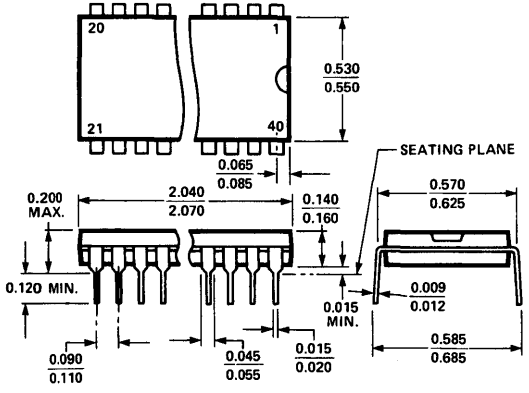
24 Lead (300 MIL) Molded DIP P13



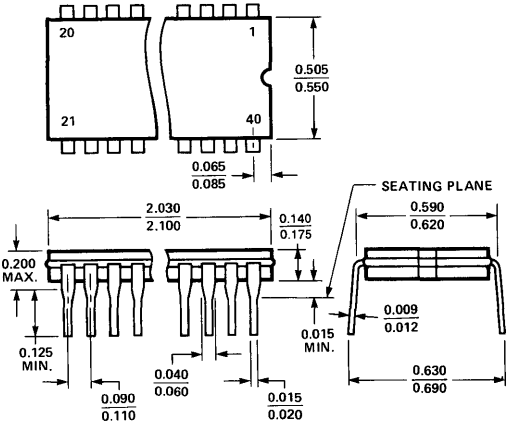
24 Lead (300 MIL) Cerdip D14



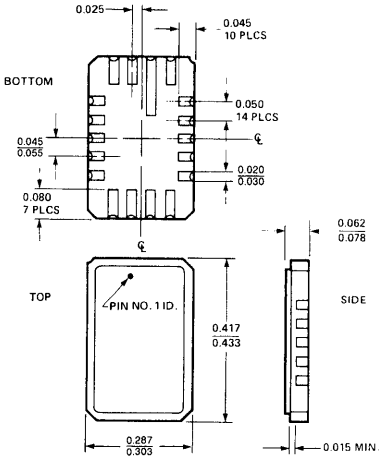
40 Lead Molded DIP P17



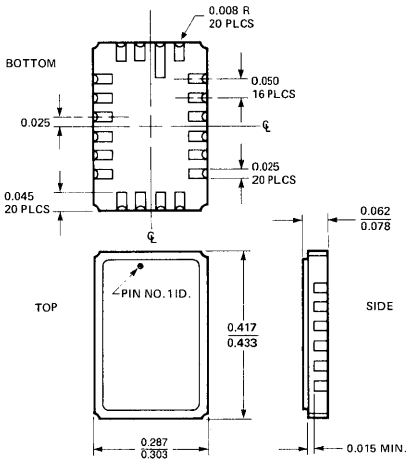
40 Lead Cerdip D18



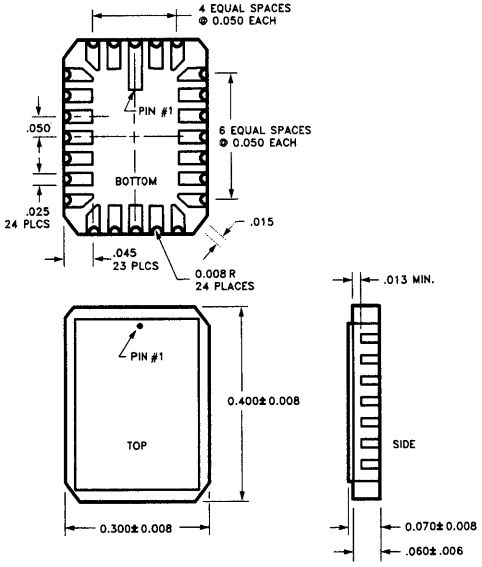
18 Pin Rectangular Leadless Chip Carrier L50



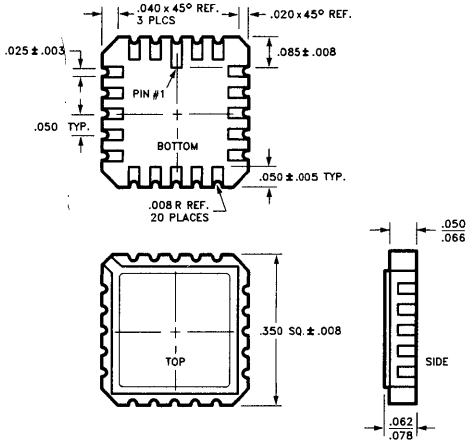
20 Pin Rectangular Leadless Chip Carrier L51



24 Pin Rectangular Leadless Chip Carrier L53



20 Pin Square Leadless Chip Carrier L61



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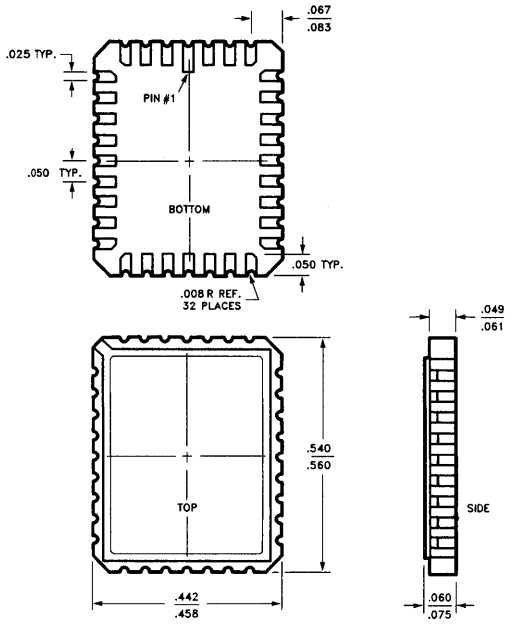
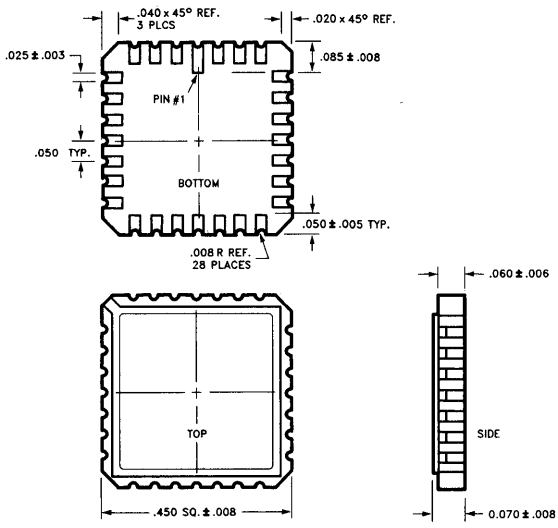
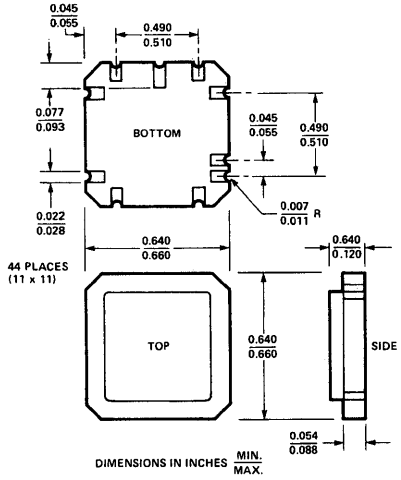
32 Pin Rectangular Leadless Chip Carrier L55



28 Pin Square Leadless Chip Carrier L64



44 Pin Square Leadless Chip Carrier L67



Thermal Management and its Importance

One of the key variables that determines the long term reliability of integrated circuits is the temperature of the device during its operation. In the operation of many semiconductor devices the effective dissipation of internally generated thermal energy is critical to both device performance and the component's reliability. A device's useful lifetime is an exponential function of junction temperature, decreasing by approximately a factor of two for every 10 degree C increase in temperature. Most of the failure mechanisms responsible for device failure are thermally activated, viz: electromigration, breakdown of packaging materials, Gold-Aluminum bond wire integrity...etc. Therefore, it is from this point of view that high reliability components need a careful control of the mean operating temperatures.

Thermal Resistance: Definitions and Terminologies

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as,

$$\theta_{Ja} = \frac{T_J - T_a}{P}$$

and θ_{Ja} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation:

$$T_J = T_a + P\,[\theta_{Ja}] = T_a + P\,[\theta_{Jc} + \theta_{ca}]$$

where:

$$\theta_{Jc} = \frac{T_J - T_c}{P} \text{ and } \theta_{ca} = \frac{T_c - T_a}{P}$$

T_a = Ambient temperature at which the device is operated; Most common standard temperature of operation = 70 deg. C
T_J = Junction temperature of the IC chip
T_c = Temperature of the case (package)
P = Power at which the device operates
θ_{Jc} = Junction to case thermal resistance
θ_{Ja} = Junction to ambient thermal resistance
θ_{ca} = Case to ambient thermal resistance

Cypress Plastic Packages Incorporate:

- High thermal conductivity copper lead frame.
- Molding compound with high thermal conductivity Silica fillers.
- Silver filled conductive epoxy as die attach material.
- Gold bond wires.

Cypress Cerdip Packages Incorporate:

- High conductivity Alumina substrates.
- Silver filled glass as die attach material.
- Alloy 42 lead frame.

Test Chip for Thermal Resistance Measurement

Thermal resistance measurements were carried out using a specially designed test chip.

A dedicated silicon test chip was designed. The chip contains a series of diffused resistors with a total resistance of 25 ohms. These resistors are utilized to generate heat by forcing a current through them.

The chip also has three diodes located at different positions and isolated from the main resistor circuit. The temperature measurements are made by measuring the forward voltage drop across the diode at a fixed current (50 μA). The diodes are calibrated prior to thermal measurements. The θ_{Ja} measurements are done in a natural convection environment (in a 1 cubic foot closed box) and θ_{Jc} measurements are done in a freon bath kept at a constant 30°C.

Thermal resistance values, θ_{Ja} and θ_{Jc}, for Cypress Cerdip and Plastic packages are presented in the following table.

Thermal Resistance Measurement

Pin Count	Pkg Width (Mils)	Theta JA Plastic Deg C/Watt	Theta JC Plastic Deg C/Watt	Theta JA Cerdip Deg C/Watt	Theta JC Cerdip Deg C/Watt
16	300	92	57	85	40
18	300	85	55	83	38
20	300	80	53	80	39
22	400	70	43	75	32
24	300	73	43	73	37
24	600	58	43	60	32
28	600	56	43	60	32

Note: The heat flow from the package can be greatly improved and thus θ_{Ja} can be drastically reduced by using artificial air and/or heat spreaders.

CYPRESS SEMICONDUCTOR

Appendix B: Quality, Reliability and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors; better designs, processes, controls and materials. Therefore, product quality and reliability is built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability starts at the initial design inception. It is built into every product design from the very start.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Guideline Documents

Cypress Semiconductor uses Mil-Std-883 and Mil-M-38510 as guideline documents by which to model our Test Methods, Procedures and General Specifications for semiconductors.

Commercial and Industrial users receive the benefit of a military patterned processing of all product at no additional charge.

Product Testing Categories

Two different testing categories are offered by Cypress.

1) Commercial operating range: 0°C to +70°C

2) Military operating range: −55°C to +125°C

Military operating range product are available on all devices manufactured by Cypress.

Standard Product Assurance Categories

Commercial devices produced to the above testing categories have two different classes of product assurance. Every device shipped, as a minimum meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be easily accomplished.

Level 2: For flight applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and burn-in screening to Method 1015.

Table 1 lists the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet the requirements of these programs.

Table 1. Cypress Product Screening Flows

Screen	MIL-STD-883 Method	Product Temperature Ranges				
		Commercial 0°C to +70°C				Military −55°C to +125°C
		Level 1		Level 2		Level 2
		Plastic	Hermetic	Plastic	Hermetic	Hermetic
Visual/Mechanical						
•Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%	100%
•High Temperature Storage	1008, Cond C	—	100%	—	100%	100%
•Temperature Cycle	1010, Cond C	—	—	—	—	100%
•Constant Acceleration	2001, Cond E, Y1 Orientation	n/a	—	n/a	—	100%
•Hermeticity Check: Fine/Gross Leak	1014, Cond A & B; Fine Leak Cond C; Gross Leak	n/a	LTPD 5; 77(1,2)	n/a	LTPD 5; 77(1,2)	100%
Burnin						
•Pre-Burn-in Electrical	Per Device Specification & Cypress Method 10009	—	—	100%	100%	100%
•Burn-in	Method 1015 Equivalent & Cypress Methods 10012, 10015			100%	100%	100%
Final Electrical		Cypress Datasheet Electrical Specifications				
•Functional, Switching, Dynamic (AC) and Static (DC) Tests	1) At 25°C and Power Supply Extremes	—	—	100%[1]	100%[1]	100%
	2) At Temperature and Power Supply Extremes	100%[3]	100%[3]	100%[3]	100%[3]	100%
Jan/Military Conformance Tests						
•Group A	See Tables 2–5 For Details	—	—	—	—	Sample
•Group B						Sample
•Group C						Sample
•Group D						Sample
Cypress Quality Lot Acceptance						
•External Visual	2009	0.65% AQL	0.65% AQL	0.65% AQL	0.65% AQL	0.65% AQL
•Final Electrical Conformance	Cypress Method 40021	0.1% AQL	0.1% AQL	0.1% AQL	0.1% AQL	(2)
•Fine & Gross Leak Conformance	1014, Cond A & B; Fine Leak Cond C; Gross Leak	n/a	LTPD = 5; 77(1,2)	n/a	LTPD = 5; 77(1,2)	LPTD = 5, 77(1,2)

Notes:
1) Electrical Test at 25°C is performed to facilitate PDA calculation.
2) Final electrical conformance tests are covered by Group A tests.
3) Hot Temperature Testing performed only.

Table 2. Group A Test Descriptions

Cypress uses a LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military products have a Group A sample test performed as outlined by the particular screen flow.

Subgroup	Description	LTPD	Sample Size/ Accept No.
1	Static Tests at 25°C	2	195/1
2	Static Tests at Maximum Rated Operating Temperature	3	129/1
3	Static Tests at Minimum Rated Operating Temperature	5	77/1
4	Dynamic Tests at 25°C	2	195/1
5	Dynamic Tests at Maximum Rated Operating Temperature	3	129/1
6	Dynamic Tests at Minimum Rated Operating Temperature	5	77/1
7	Functional Tests at 25°C	2	195/1
8	Functional Tests at Minimum and Maximum Temperatures	5	77/1
9	Switching Tests at 25°C	2	195/1
10	Switching Tests at Maximum Temperature	3	129/1
11	Switching Tests at Minimum Temperature	5	77/1

Table 3. Group B Quality Tests

Subgroup	Description	Quantity/(Accept #) or LTPD
1	Physical Dimensions, Method 2016	2/0
2	Resistance to Solvents, Method 2015	4/0
3	Solderability, Method 2003	15
4	Internal Visual/Mechanical, Method 2014	1/0
5	Bond Strength, Method 2011	15
6	Internal Water Vapor[1], Method 1018	3/0 or 5/1
7	Seal: Fine & Gross Leak[2], Method 1014	5
8	ESD Characteristics, Method 3015.2	15/0

Notes:

1) Internal Water Vapor is not performed since no desiccant is contained in the package
2) Fine and Gross Leak is not performed because a 100% screen is employed

Group B testing is performed on each inspection lot, which is defined as all product built in a 6 week seal period, for each package type and lead finish.

Table 4. Group C Quality Tests

Subgroup	Description	LTPD
1	Steady State Life Test, End Point Electricals, Method 1005	5
2	Temp Cycle, Constant Acceleration Seal: Fine & Gross Leaks, Visual Examination, End Point Electricals Methods 1010, 2001, 1014	15

Group C tests are performed on one device type or one inspection lot representing each technology. Sample tests are performed from each three months production of devices, which is based on the lot inspection identification codes.

Table 5. Group D Quality Tests (Package Related)

Subgroup	Description	Quantity/Accept # or LTPD
1	Physical Dimensions, Method 2016	15
2	Lead Integrity, Seal: Fine & Gross Leak, Methods 2004 & 1014	15
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 1011, 1010, 1004 & 1014	15
4	Mechancial Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 & 1014	15
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15
6	Internal Water-Vapor Content; 500 ppm maximum @ 100°C. Method 1018	3/0 or 5/1
7	Adhesion of Lead Finish, Method 2025	15
8	Lid Torque, Method 2024	5/0

Group D tests are performed on each package type from each six months production, based on lot identification codes.

Standard Product Screening Summary

Commercial Product

- Screened to Cypress Level 1 and Level 2 product flows
- Hermetic and Molded packages available
- Incoming Mechanical and Electrical performance guaranteed:
  - — 0.1% AQL Electrical Sample performed on every lot prior to shipment
  - — 0.65% AQL External Visual Sample also performed
- Electrically Tested to Cypress datasheet

Ordering Information

Level 1 Product

- Order Standard Cypress part number
- Parts Marked the same as ordered part number

Ex: CY7C122-15PC

Level 2 Product

- Burnin performed on all devices to Cypress detailed circuit specification
- Add "B" Suffix to Cypress standard part number when ordering to designate Burnin option
- Parts marked the same as ordered part number

Ex: CY7C122-15PCB

Military Product

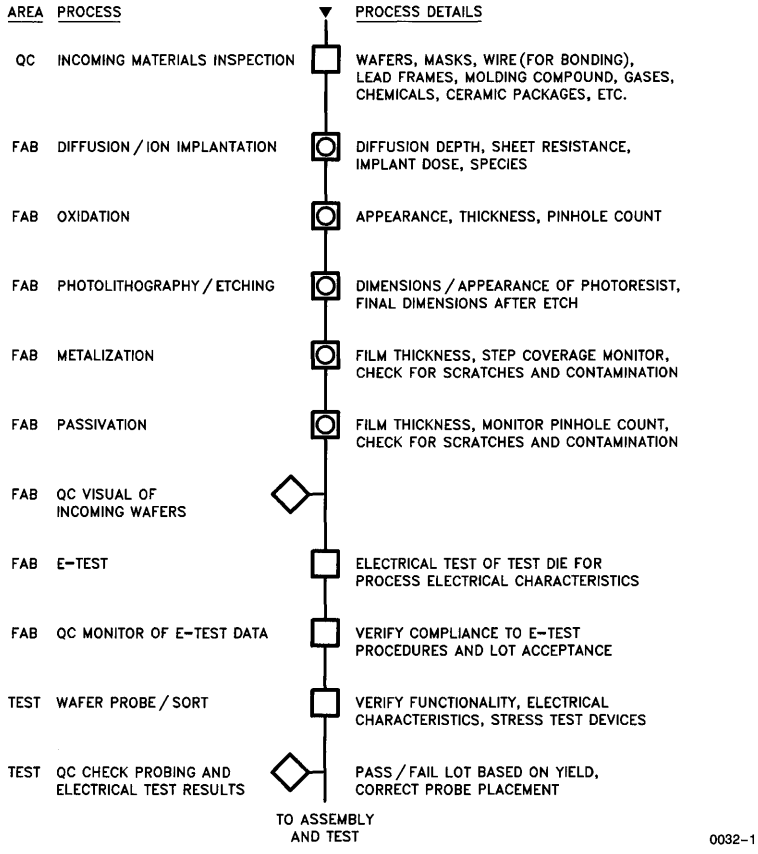
- Product processed per Cypress Level 2 Military product test flows
- Electrically tested to Cypress datasheet specifications
- All devices supplied in Hermetic packages
- Quality conformance assured: Groups A, B, C and D performed as part of the standard process flow
- Burnin performed on all to devices Cypress detailed circuit specification
- AC, DC, Functionally and Dynamically tested at 25°C as well as temperature and power supply extremes on 100% of the product in every lot

Ordering Information

- Order per Cypress standard part number with "B" suffix added to designate Burnin option
- Marked the same as ordered part number

Ex: CY7C122-25DMB

Commercial Product Quality Assurance Flow



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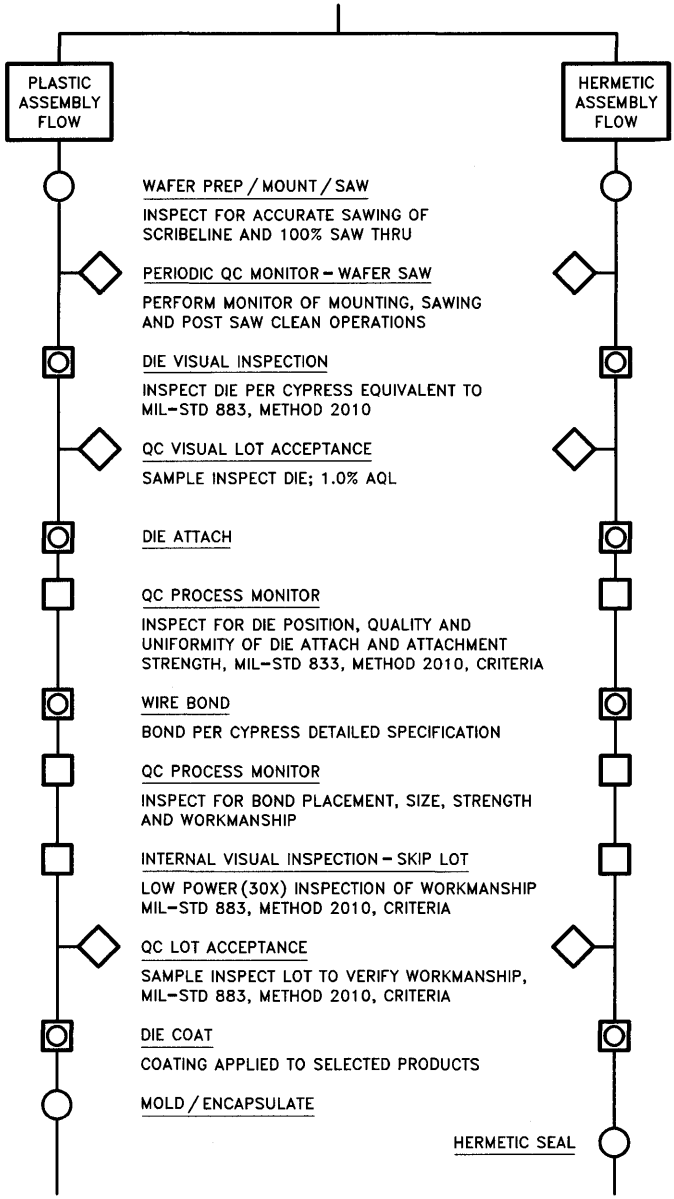
Commercial Product Quality Assurance Flow (Continued)



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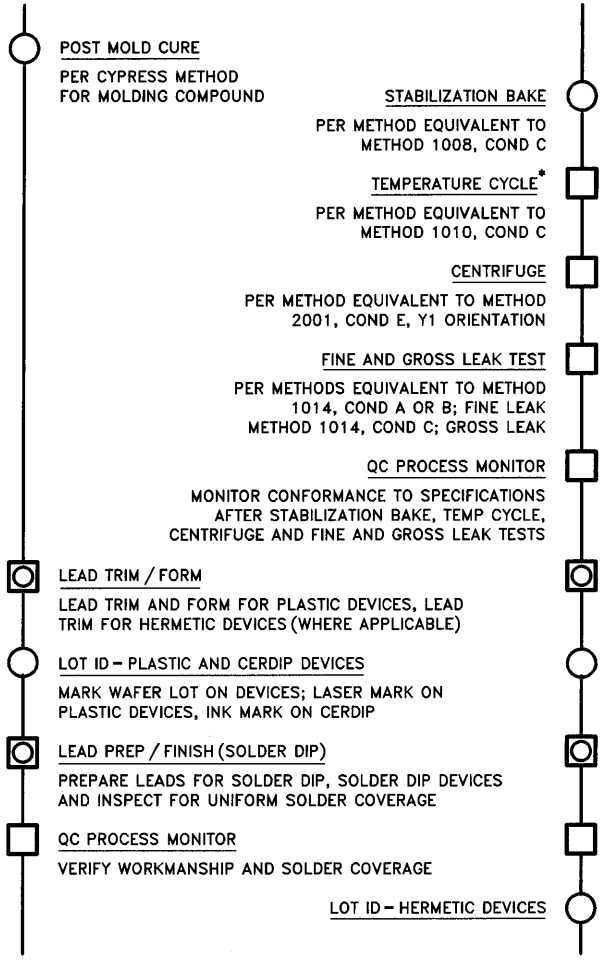
Commercial Product Quality Assurance Flow (Continued)



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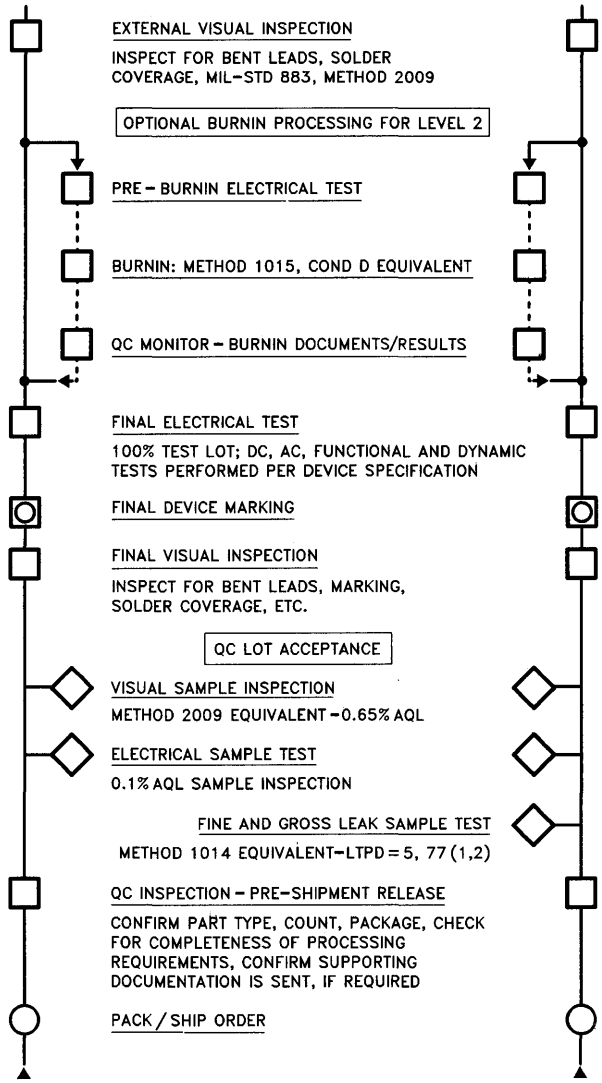
Commercial Product Quality Assurance Flow (Continued)



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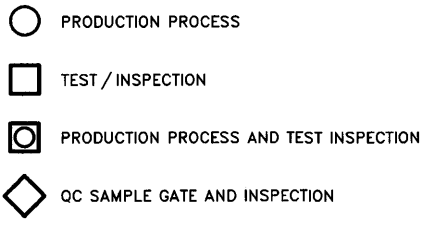
Key



0032-5

Reliability Testing

In order to determine the reliability of product being shipped to the end customer, Cypress's Quality and Reliability department samples products from normal production material. These samples are pulled on a random basis from a different device type and generic process. An example of this would be the 7C122 (256 × 4 SRAM) as the specific device type for the generic RAM process. The 7C245 (2K × 8 Registered PROM) would be used as a specific device type for the generic PROM/PAL process.

Sampling Plan for Reliability Testing

Tested Performed	LTPD	Sample Size/ Accept #	Periodicity*
HTOL, Method 1005, Cond D	5	105/2	monthly
Biased 85/85, Low Power Condition	7	55/1	monthly
Pressure Pot, 121°C, 15 Psig	7	55/1	bi-weekly
External Visual Examination; Method 2009	15	15/0	quarterly
Physical Dimensions; Method 2016	15	15/0	quarterly
Lead Fatigue; Method 2004, Cond B2	10	22/0	quarterly
Temperature Cycling; Method 1010	5	55/1	bi-weekly
Temperature Shock	5	55/1	quarterly
ESD Sensitivity; Method 3015	15	15/0	quarterly
Latchup Immunity		5/0	quarterly

* Maximum period between samples is listed. More frequent sampling may occur.

CYPRESS SEMICONDUCTOR

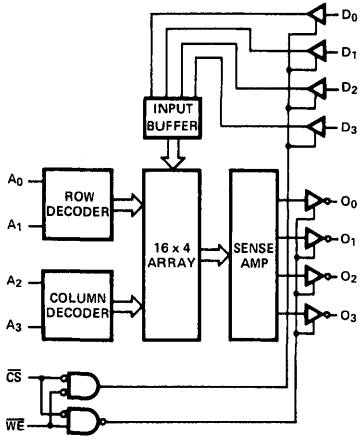
Appendix C: Application Briefs
RAM Input Output Characteristics

Introduction to Cypress RAMs

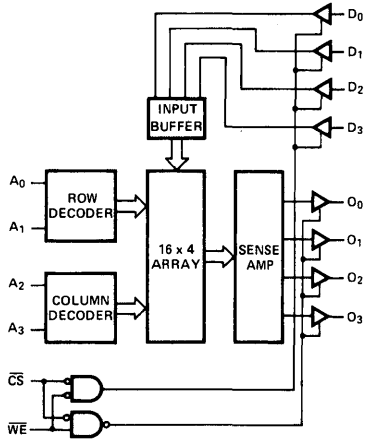
Cypress Semiconductor Corporation uses a speed optimized CMOS technology to manufacture high speed static RAMs which meet and exceed the performance of competitive bipolar devices while consuming significantly less power and providing superior reliability characteristics. While providing identical functionality, these devices exhibit slightly differing input and output characteristics which provide the designer opportunities to improve overall system performance. The balance of this application note describes the devices, their functionality and specifically their I/O characteristics.

PRODUCT DESCRIPTION

The five parts in *Figure 1* constitute three basic devices of 64, 1024 and 4096 bits respectively. The 7C189 and 7C190 feature inverting and non-inverting outputs respectively in a 16 x 4 bit organization. Four address lines address the 16 words, which are written to and read from over separate input and output lines. Both of these 64 bit devices have separate active LOW select and write enable signals. The 256 x 4 7C122 is packaged in a 22 pin DIP, and features separate input and output lines, both active LOW and active HIGH select lines, eight address lines, an active LOW output enable, and an active LOW write enable. Both the



7C189



7C190

Figure 1. RAM Block Diagrams

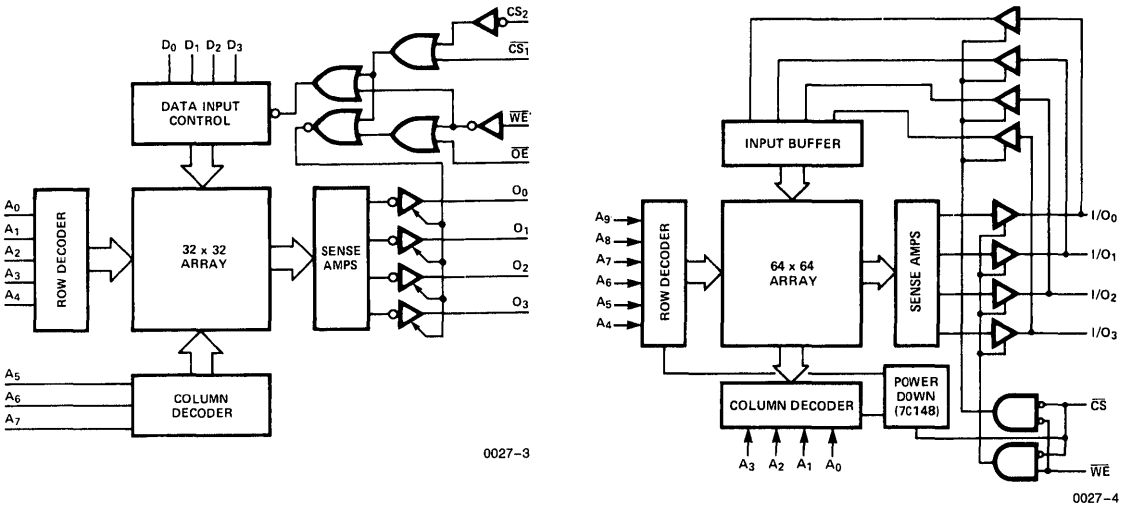


Figure 1. RAM Block Diagrams (Continued)

7C148 and 7C149 are organized 1024 x 4 bits and feature common pins for the input and output of data. Both parts have 10 address lines, a single active LOW chip select and an active LOW write enable. The 7C148 features automatic power down whenever the device is not selected, while the 7C149 has a high speed 15 ns chip select for applications which do not require power control. This family of high speed static RAMs is available with access times of 15 to 45 ns with power in the 300 to 500 mW range. They are designed from a common core approach, and share the same memory cell, input structures and many other characteristics. The outputs are similar, with the exception of output drive, and the common I/O optimization for the 7C148 and 7C149. For more detailed information on these products, refer to the available data sheets.

GENERIC I/O CHARACTERISTICS

Input and output characteristics fall generally into two categories, when the area of operation falls within the normal limits of V_{CC} and V_{SS} plus or minus approximately 600 mV, and abnormal circumstances when these limits are exceeded. Inputs under normal operating conditions are voltages that switch between logic "0" and logic "1". We will consider operation in a positive true environment and therefore a logic "1" is more positive than a logic "0". The I/O characteristics of the devices we are concerned with are what is considered to be TTL compatible. Therefore a logic "1" is 2.0V, while a logic "0" is 0.8V. The input of a device must be driven greater than 2.0V not to exceed V_{CC} + 0.6V to be considered a logic "1" and to less than 0.8V but not less than V_{SS} − 0.6V to be considered a logic "0".

Output characteristics represent a signal that will drive the input of the next device in the system. Since the levels we are dealing with are TTL, we may assume that the V_{IL} and V_{IH} values of 0.8 and 2.0V referenced above are valid. In consideration of noise margin however, driving the input of the next stage to the required V_{IL} or V_{IH} is not sufficient. Noise margins of 200 to 400 mV are considered more than adequate, and therefore the V_{OH} we deal with is 2.4V while the V_{OL} is 0.4V, providing a noise margin of 400 mV. Since the driven node consists of both a resistive and a capacitive component, output characteristics are specified such that the output driver is capable of sinking I_{OL} at the specified V_{OL}, and capable of sourcing I_{OH} at V_{OH}. Since the values of I_{OL} and I_{OH} differ depending on the device, these values are shown in Table 1. Outputs have one other characteristic that we need to be concerned with, Output Short Circuit Current or I_{OS}. This is the maximum current that the output will source when driving a logic "1" into V_{SS}. We need to be concerned for two reasons. First, the output should be capable of supplying this current for some reasonable period of time without damage, and second, this is the current that charges the capacitive load when switching the output from a "0" to a "1" and will control the output rise time.

Since memories such as these are often tied together, we are also concerned about the output characteristics of the devices when they are deselected. All of the devices in this family feature three state outputs such that in addition to their active conditions when selected, when deselected, the outputs are in a high impedance condition which does not source or sink any current. In this condition, as long as the input is driven in its normal operating mode, it appears as an open, with less than 10 μA of leakage. Thus to any other device driving this node, it is non-existent.

TECHNOLOGY DEPENDENCIES AND BENEFITS

Some of the products in this application note were originally produced in a BIPOLAR technology, some have since been re-engineered in NMOS technology and Cypress has now produced them in a speed optimized CMOS technology. There are both technology dependencies and benefits relative to the design of input and output structures that are associated with each technology. The designer who uses these products should be knowledgeable of these characteristics and how they can benefit or impede a design effort. One of the most obvious is that both NMOS and CMOS device inputs are high impedance, with less than 10 μA of input leakage. Bipolar devices, however, require that the driver of an input sink current when driving to V_{IL}, but appear as high impedance at V_{IH} levels. This is due to the fact that the input of a bipolar device is the emitter of a bipolar NPN type device with its base biased positive. The bias is what establishes the point at which the input changes from requiring current be sourced to high impedance and is 1.5V. This switching level is the reason that AC measurements are done at the 1.5V level. Although NMOS and CMOS device inputs do not change from low to high impedance, great care is taken to balance their switching threshold at 1.5V. To a system designer this allows fanout to consider only capacitive loading with MOS devices while bipolar has both a capacitive and DC component. The other input characteristic which differs from bipolar to MOS is the clamp diode structure. This structure exists in both MOS and bipolar, however in MOS that uses BIAS GENERATOR techniques, all high speed MOS devices, the diode does not become forward biased until the input goes more negative than the substrate bias generator +1 diode drop. Since the bias generator is usually about −3V this has the effect of removing the clamping effect.

I/O Parametrics

CMOS/NMOS/BIPOLAR INPUT CHARACTERISTICS

Although NMOS, CMOS and BIPOLAR technologies differ fairly widely, the I/O characteristics tend to fall into two areas. The traditional characteristics are the TTL derivatives that have been covered above, and are documented in Table 1. With the exception of the differences in input impedance between MOS and BIPOLAR devices all three technologies are used to produce TTL compatible products. The second camp is the true CMOS interface where signals swing from V_{SS} to V_{CC}. These interface specifications define a "1" as greater than V_{CC} − 1.5V and a "0" as less than V_{SS} + 1.5V. In addition, loads are primarily capacitive. Only devices produced in a CMOS technology are capable of behaving in this manner. CMOS devices can, however, handle both TTL and CMOS inputs. Devices such as the ones described in this application note have input characteristics depicted in *Figure 2.*

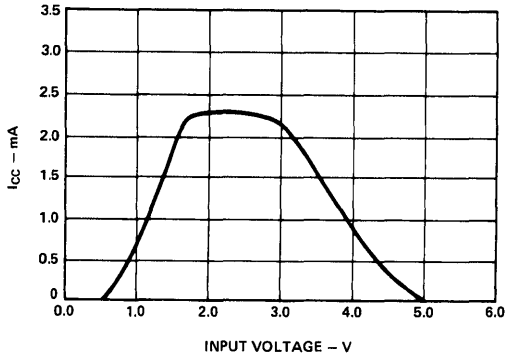


Figure 2. Input Voltage vs. Current

Table 1. DC Parameters

Parameters	Description	Test Conditions	7C122		7C148/9		7C189/90		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −5.2 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.1	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IL}	Input Low Current	V_{CC} = Max., V_{IN} = V_{SS}		10		10		10	μA
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}		10		10		10	μA
I_{OFF}	Output Current (High Z)	V_{OL} < V_{OUT} < V_{OH}, T_A = Max.	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., 0°C < T_A < 70°C		−70		−90		−275	mA
		V_{OUT} = V_{SS}, −55°C < T_A < 125°C		−80		−90		−350	mA

When operated in the TTL range, they perform normally. Operated in full CMOS mode, an additional benefit of power savings is realized as the current consumed in the input converter decreases as the input voltage rises above 3.0V, or falls below 1.5V. Since the input signal is in the 1.5 to 3.0V range only when transitioning between logic states, the power savings in a large array with true CMOS inputs can be significant. With input signals on over half of the pins of a device, significant savings in a large system can be realized by using CMOS input voltage swings even in TTL systems.

Switching Characteristics

Although this application note does not directly deal with the AC characteristics of high speed RAMs, the input and output characteristics of these devices have a great deal to do with the actual AC specifications. Conventionally, all AC measurements associated with high speed devices are done at 1.5V and assume a maximum rise and fall time. This eliminates the variations associated with the various configurations that the device will be used in as a figure of merit when testing the device, but does not mean that the designer can ignore these influences when designing a system. Maximum rise and fall time is usually found in the notes included on every data sheet. For the products referred to in this application note, a 10 ns maximum rise and fall time is specified for all devices with access times equal to or greater than 25 ns and a 5 ns maximum rise and fall time for all devices with access times less than 25 ns. The AC load and its Thévenin equivalent in *Figure 3* represent the resistive and capacitive components of load which the devices are specified to drive. With either of these loads, the device will be required to source or sink its rated output current at its specified output voltage. The capacitance stresses the ability of the device output to source or sink sufficient current to slew the outputs at a high enough rate to meet the AC specifications. The high impedance load is a convenience to testing when trying to determine how rapidly the output enters a high impedance condition. Once the output enters a high impedance mode, the resistive divider will charge the capacitance until equilibrium is reached. Allowing for noise margin, testing for a 500 mV change is normal. By using a smaller capacitance than normal, the change will occur more quickly, allowing a more accurate determination of entry into the high impedance state.

SWITCHING THRESHOLD VARIATIONS

Switching threshold variations along with input rise and fall times can have an effect on the performance of any device. Input rise and fall times are under the control of the designer, and are primarily affected by capacitive loading, the driver and bus termination techniques. Switching threshold is affected by process variations, changes in V_{CC} and temperature. Compensation of these variables is the territory of the manufacturer, both at the design stage and the manufacturing of the device. Combined threshold shifts over full military temperature ranges and process variations average less than 100 mV. This translates directly to V_{IL} and V_{IH} variations which track well within the noise margins of normal system design particularly since the V_{OL} and V_{OH} changes track to the same 100 mV.

Input Protection Mechanisms

THE ELECTROSTATIC DISCHARGE PHENOMENA

Because of their extremely high input impedance and relatively low (approximately 30V) breakdown voltage, MOS devices have always suffered from destruction caused by ESD (Electro Static Discharge). This has caused two actions. First, major efforts to design input protection circuits without impeding performance has resulted in MOS devices that are now superior to bipolar devices. Second, care in handling semiconductors is now common practice. Interestingly enough, bipolar products that once did not suffer from ESD have now suddenly become sensitive to the phenomena, primarily because new processing technology involving shallow junctions is in itself sensitive. MOS devices are in many cases now superior to bipolar products. A sampling of competitive BIPOLAR and NMOS 64 bit, 1K bit and 4K bit products reveals breakdown voltages as low as ±150V to greater than ±2001V magnitudes. The circuit in *Figure 4* is used to protect Cypress products against ESD. It consists of two thick oxide field transistors wrapped around an input resistor and a thin oxide device

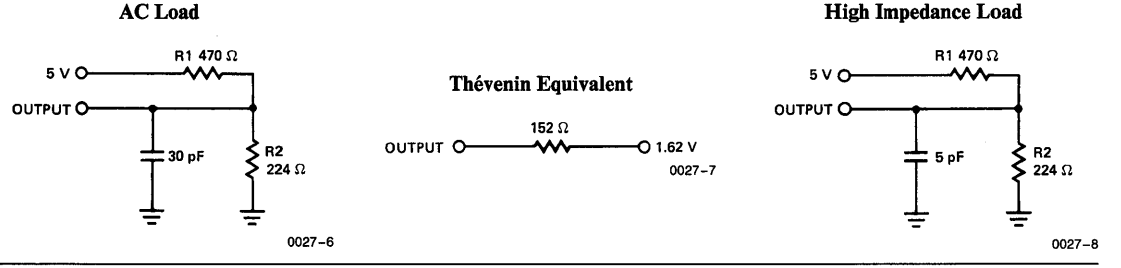


Figure 3. Test Loads

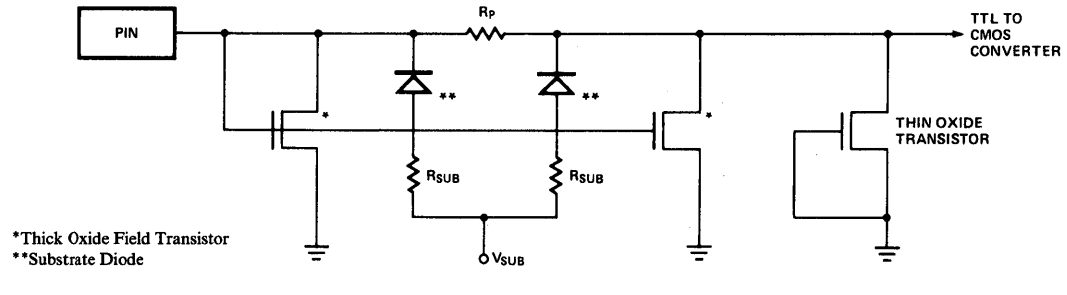


Figure 4. Input Protection Circuit

with a relatively low breakdown voltage of approximately 12V. Large input voltages cause the field transistors to turn on discharging the ESD current harmlessly to ground. The thin oxide transistor breaks down when the voltage across it exceeds the 12V level and it is protected from destruction by the current limiting of R_P. The combination of these two structures provides ESD protection greater than 2250V, the limit of the testing equipment available. In addition, repeated applications of this stress do not cause a degradation that could lead to eventual device failure as observed in functionally equivalent devices.

CMOS Latchup

The parasitic bipolar transistors shown in *Figure 5* result in a built-in silicon controlled rectifier illustrated in *Figure 6*. Under normal circumstances the substrate resistor R_{SUB} is connected to ground. Therefore, whenever the signal on the pin goes below ground by one diode drop, current flows from ground through R_{SUB} forward biasing the lower transistor in the effective SCR. If this current is sufficient to turn on the transistor, the upper PNP transistor is forward biased, the SCR turns on and normally destroys the device. Several solutions are obvious, decreasing the substrate resistance, or adding a substrate bias generator are two. The bias generator technique has several additional benefits, however, such as threshold voltage control which increases device performance and is employed in all Cypress products, along with guard rings which effectively isolate input and output structures from the core of the device and thus effectively decrease the substrate resistance by short circuiting the current paths. Latchup can potentially be induced at either the inputs or outputs. In true CMOS output structures as discussed above, the output driver has a PMOS pullup which creates additional vertical bipolar PNP transistors compounding the latchup problem. Additonal isolation using the guard ring technique can be used to solve this problem, at the expense of additional silicon

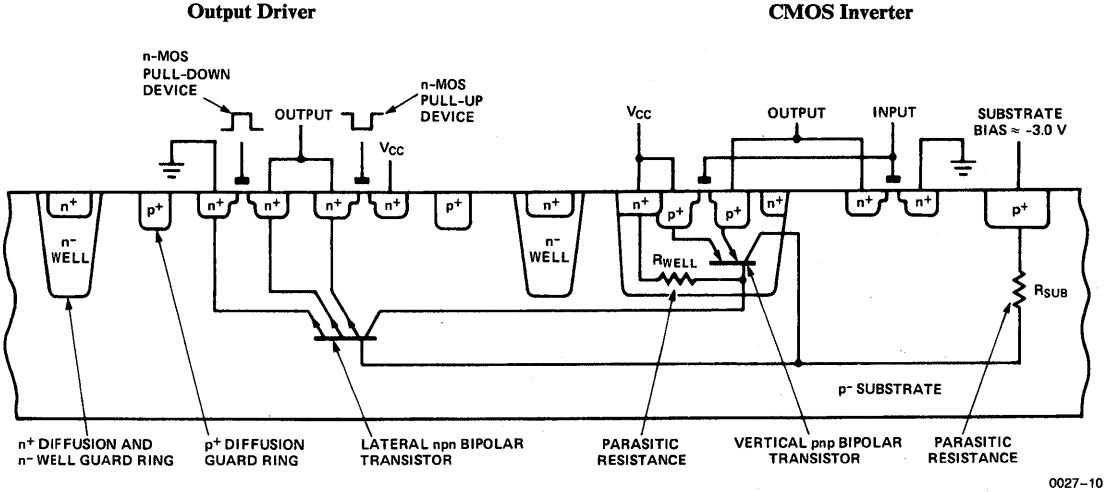


Figure 5. CMOS Cross Section and Parasitic Circuits

Substrate Bias Generator

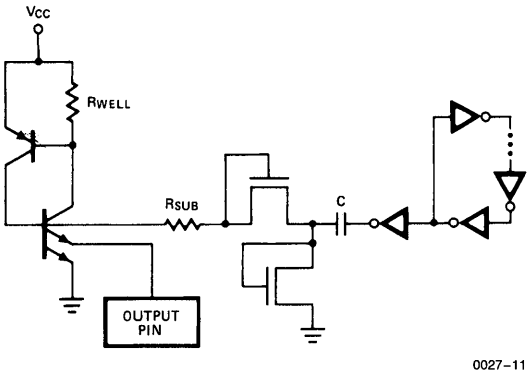


Figure 6. Parasitic SCR and Bias Generator

area. Since all of the devices of concern here require TTL outputs, the problem is totally eliminated through the use of an NMOS pullup.

LATCHUP CHARACTERISTICS

Inducing Latchup for Testing Purposes

Care needs to be exercised in testing for latchup since it is normally a destructive phenomena. The normal method is to power the device under test with a supply that can be current limited, such that when latchup is induced, insufficient current exists to destroy the device. Once this setup exists, driving the inputs or outputs with a current, and measuring the point at which the power supply collapses will allow non-destructive measurement of the latchup characteristics of the devices under question. In actual testing, with the device under power, individual inputs and outputs are driven positive and negative with a voltage and the current measured at which the device latches up. This provides the DC latchup data for each pin on the device as a function of trigger current.

Measurement of Latchup Susceptability

Actually measuring the latchup characteristics of devices should encompass ranges of reasonable positive and negative currents for trigger sources. Depending on the device, latchup can occur as low as a few mA to as high as several hundred mA of sink or source current. Devices which latch at trigger currents of less than 20 to 30 mA are in danger of encountering system conditions that will cause latchup failure.

Competitive Devices

Although there are few devices directly competitive with the Cypress devices covered in this application note, the latchup characteristics of the closest functionally similar devices were measured. The results show devices the latchup at as low as 10 mA all the way to devices that can sustain greater than 100 mA of trigger current without latchup. The Cypress devices covered in this document can sustain greater than 200 mA without incurring latchup, far more than is possible to encounter in any reasonable system environment.

Elimination of Latchup in Cypress RAMs

Since the latchup characteristic is one that inherently exists in any CMOS device, rather than change the laws of physics, we design to minimize its effects over the operating environment that the device must endure. These include temperature, power supply and signal levels as well as process variations. There are several techniques employed to eliminate the latchup phenomena. Two of them involve effectively moving the trigger threshold so far outside the operating range as to make it impossible to ever encounter. These are either using low impedance, epitaxial, substrates and/or a substrate bias generator. The use of a low impedance substrate has the effect of increasing the undershoot voltage required to generate the required trigger current that causes latchup. A substrate bias generator has two effects which help to eliminate latchup. First, by biasing the substrate at a negative, −3.0V, voltage, the parasitic diodes can not be forward biased unless the undershoot exceeds the −3V by at least one diode drop. Second, if undershoot is this severe, the impedance of the bias generator itself is sufficient to deter sufficent trigger from being generated. The bias generator has one additional noticeable characteristic, it effectively removes the input clamp diode. This is due to the anode of the diode connecting to the substrate which is at −3.0V. Therefore, even though the diode exists as shown in *Figure 4*, DC signals of −3.0V do not forward bias the diode and exhibit the clamp condition. The benefits of this are apparent in higher noise tolerance as substrate currents due to input undershoot do not occur.

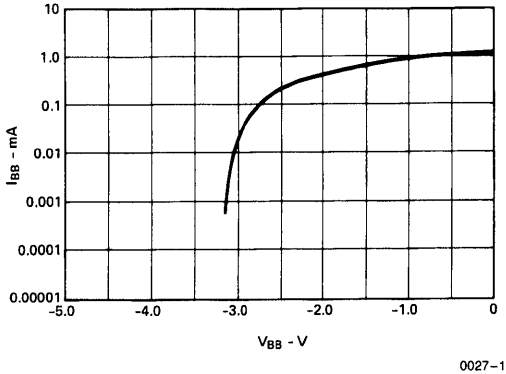


Figure 7. Bias Generator Characteristics

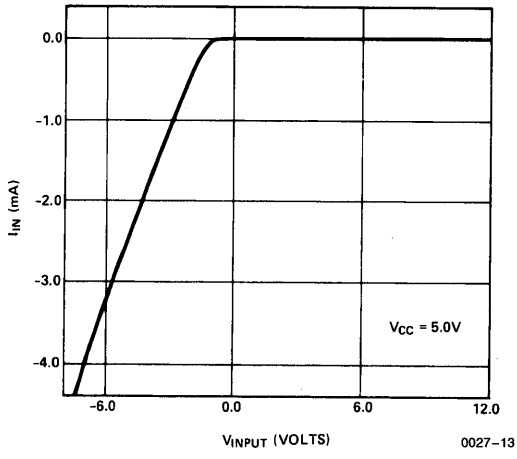
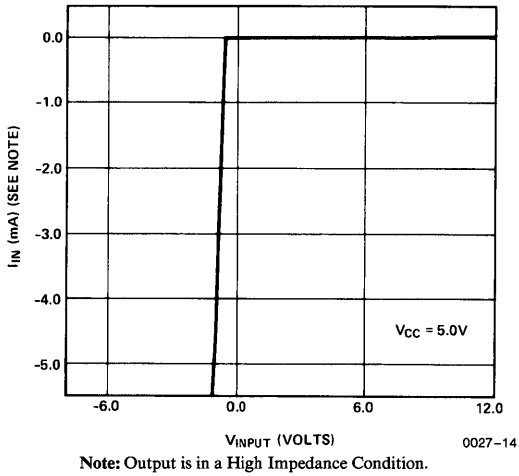


Figure 8. Input V/I Characteristics



Note: Output is in a High Impedance Condition.

Figure 9. Output V/I Characteristics

Figures 8 and *9* represent the voltage and current characteristics of the devices discussed in this application brief. *Figure 8* is characteristic of an input pin, and *Figure 9* an output pin in a high impedance state. In *Figure 8*, the input covers +12V to −6V, well outside the −3 to +7V specification. Referring to *Figure 4* to understand these characteristics, when the input voltage goes negative, the thin oxide transistor acts as a forward biased diode and the slope of the curve is set by the value of R_P. As the input voltage goes positive, leakage current only flows. The output characteristics in *Figure 9* show the same phenomena, with the exception that, since this is not an input, no protection circuit and therefore no R_P exists. An equivalent thin film device acts as a clamp diode which limits the output voltage to approximately −1V at −5 mA.

CYPRESS SEMICONDUCTOR

Understanding FIFOs

Introduction

FIFO is an acronym for First-In-First-Out.

In digital electronics, a FIFO is a buffer memory that is organized such that the first data entered into the memory is also the first data removed from the memory.

History of FIFOs

Software FIFOs

Software FIFOs have been (and are being) used extensively in computer programs where tasks are placed in queues waiting for execution. In the programmers' language the program (process) that puts data into the memory is a "producer" and the program that takes data out is a "consumer". Obviously the producer and the consumer cannot access the memory simultaneously. It is the responsibility of the programmer to insure that contention does not occur. Data transfer via a shared memory is a standard programming technique but it is not feasible to have the processor in the data path for data rates greater than 5 Megabytes per second (MB/s). For higher data rates DMA, FIFO, or some combination of the two techniques are used to transfer information.

Hardware FIFOs

In the design of systems, once procedures are standardized and verified in software, the software can be replaced with hardware. The benefits of doing this are improved performance, reduced software, ease of design and usually reduced costs.

Register Array

The first hardware FIFOs were of the "register array" architecture and included the serializer/deserializer (SERDES) within the IC. As they evolved, and due to the ubiquitous microprocessor, the parallel input and parallel output configuration became the standard. For applications that required SERDES users added external shift registers.

The method of transferring data from one register to another is called a "bucket brigade". The transfer is controlled by a "valid data" bit (one per word) that designates which words have been written into but not yet read from and combinatorial control logic. The time for this logic to propagate a word of data from the input to the output of an initially empty FIFO is called "fallthrough time".

Dual Port Ram

The "second generation" of FIFOs are of the "dual port RAM" architecture. In order to achieve truly independent, asynchronous operation of inputs and outputs, the capability to read and write simultaneously must be designed into the basic memory cell.

The fallthrough time present in the register array organization is eliminated by the RAM architecture. However, the RAM must be (internally) addressed, which requires two pointers. One points to the location to be written into and the other points to the location to be read from. In addition, a bit is required for every FIFO word to designate which words have been written to but not yet read.

Applications

FIFOs are used as building blocks in applications where equipment that are operating at different data rates must communicate with each other, i.e., where data must be stored temporarily or buffered.

These include:

- Word processing systems
- Terminals
- Communications systems; including Local Area Networks
- EDP, CPU, and peripheral equipment; including disk controllers and streaming tape controllers

The Ideal FIFO

The characteristics of an ideal FIFO are:

INPUTS

- Infinitely variable input frequency (0 to infinity)
- Infinitely variable input handshaking signals

OUTPUTS

- Infinitely variable output frequency
- Infinitely variable output handshaking signals

The Ideal FIFO (Continued)

BOTH

- Inputs and outputs are completely independent and asynchronous to each other, except that over-run or under-run are not possible.

STATUS INDICATORS

- Full/empty
- One-half full, ¼ full, ¼ empty

LATENCY

- The latency should be zero. In other words, the data should be available at the FIFO outputs as soon as it is written. In the empty condition this would be the next cycle.

EXPANSION

- Expandable word length and depth without external logic and without performance degradation.

NO FALLTHROUGH OR BUBBLETHROUGH TIME

Analysis of Present Architectures

Register Array

The first Integrated Circuit FIFOs were an extension of the simplest FIFO of all; a serial shift register.

Input Stage

As illustrated in *Figure 1*, the input stage is a one word by m-bit parallel shift register that is under control of the input handshaking signals SI (Shift In) and IR (Input Ready).

Output Stage

The output stage is also a one word by m-bit parallel shift register that is under control of the output handshaking signals OR (Output Ready) and SO (Shift Out).

Register Array

The middle N-2 X m-bit registers are controlled by signals derived from the preceding control signals.

Valid Data

A flag bit is associated with each word of the FIFO in order to tell whether or not the data stored in that word is valid. The usual convention is to set the bit to a one when the data is written and to clear it when the data is read.

Fallthrough and Bubblethrough

The preceding statements regarding input and output stages are not precisely correct under two special conditions, which occur when the FIFO is empty and full:

EMPTY CONDITION - FALLTHROUGH

In the empty condition the data must enter the input stage and propagate to the output stage. This is called Fallthrough time and it limits the output data rate.

FULL CONDITION - BUBBLETHROUGH

When the FIFO is full and one word is read, all of the remaining words must move down one word (or the empty word must propagate to the input). This is called Bubblethrough time and it limits the input data rate.

As we shall see, Bubblethrough time and Fallthrough time are usually equal because the same logic is used.

Dual Port RAM Architecture

The dual port RAM architecture refers to the basic memory cell used in the RAM. By adding read and write transistors to the conventional two transistor RAM cell, the read and write functions can be made independent of each other. Obviously this increases the size of the RAM cell, but doing this is more than compensated for by simpler control logic and improved performance.

The RAM requires two address pointers; one to address the location where data is to be written and the other to address where data is to be read. Comparators are used to sense the empty and full conditions and control logic is required to prevent over-run and under-run.

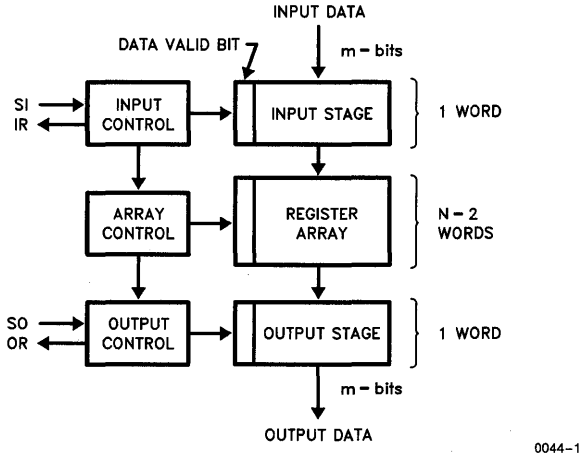


Figure 1. Register Array Architecture

Analysis of FIFOs

The procedure will be to first analyze the FIFO as a "black box" and then to compare the most important characteristics of a class of representative FIFOs with the characteristics of the CY7C401 FIFO.

The class of FIFOs chosen is the industry standard XXX401A and XXX402A that are available from Fairchild, National and Monolithic Memories. The 401 is 64 x 4 and the 402 is 64 x 5 with the same performance. Both are of the register array architecture. Both are expandable in depth (number of words), which is called cascadeable, without additional logic as well as expandable in word width (number of bits per word) with additional logic. The operation will first be analyzed in the standalone configuration.

Functional Description

Data Input - Refer to *Figures 2, 3*

After power on the Master Reset ($\overline{MR}$) input is pulsed low to initialize the FIFO. When the IR output goes high it signifies that the FIFO is able to accept data from the producer at the DI inputs. Data is entered into the input stage when the SI input is brought high (if IR is also high). SI going high causes IR to go low, acknowledging receipt of the data, which is now in the input stage.

When SI goes low (in response to IR going low) and if the FIFO is not full, IR will go back high, indicating that more room is available in the FIFO. At the same time SI goes low data is propagated to the next empty location, which may be the second location, but could be any location up to but not including the output stage.

Data Output - Refer to *Figures 4, 5*

Data is read from the DO outputs of the output stage under control of the SO and OR handshaking signals. The high state of OR indicates to the consumer that valid data is available at the outputs. When OR is high, data may be shifted out by bringing the SO line high (request), which causes the OR line to go low (acknowledge). Valid data is maintained on the outputs as long as SO is high. When SO goes low (in response to OR going low) and if the FIFO is not empty, OR will go back high, indicating that there is new valid data at the outputs. If the FIFO is empty OR will remain low and the data on the outputs will not change.

Empty/Full

If the FIFO is empty, OR will not go high within a fall-through time after SO goes low, so this condition may be sensed and used to indicate EMPTY.

Similarly, if the FIFO is full, IR will not go high within a bubblethrough time after SI goes low, so this condition may be sensed and used to indicate FULL.

Standalone Operation

Input Data Setup and Hold

The input data must be stable for an amount of time equal to the setup time (t_{IDS}) before the rising edge of SI and

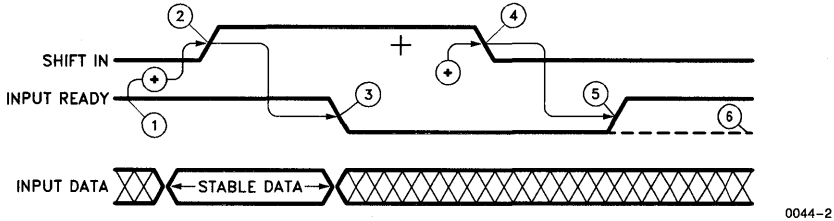


Figure 2. Method of Data Input

Notes:

Shift in pulses applied while Input Ready is LOW will be ignored.

⊕ External "producer" response time.

\+ SI pulse could be of fixed positive duration and would then not depend upon response time of producer.

① Input Ready HIGH indicates space is available and a Shift in pulse may be applied.

② Input Data is loaded into the first word.

③ Input Ready goes LOW indicating the first word is full.

④ The Data from the first word is released to propagate to the second word.

⑤ The Data from the first word is transferred to the second word. The first word is now empty as indicated by Input Ready HIGH.

⑥ If the second word is already full then the data remains at the first word. Since the FIFO is now full, Input Ready remains low.

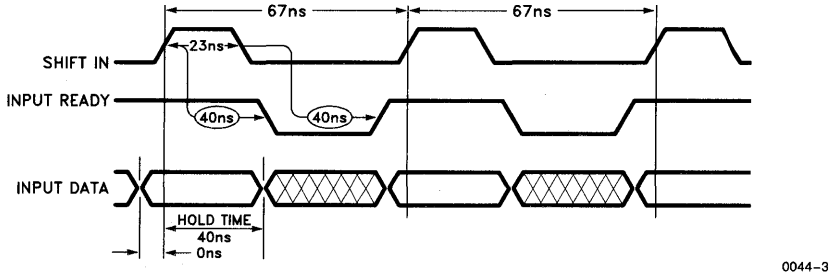


Figure 3. Input Timing for FIFO

Analysis of FIFOs (Continued)

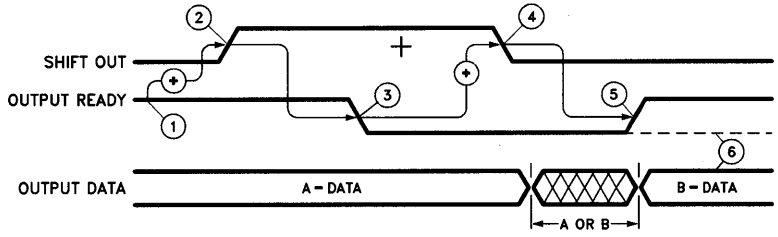


Figure 4. The Method of Shifting Data Out of the FIFO

Notes:

⊕ External "consumer" response time.

\+ SO pulse could be of fixed positive duration and would then not depend upon response time of consumer.

① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

② Shift Out goes HIGH causing the next step.

③ Output Ready goes LOW.

④ Contents of word 52 (B-DATA) is released to propagate to word 53.

⑤ Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

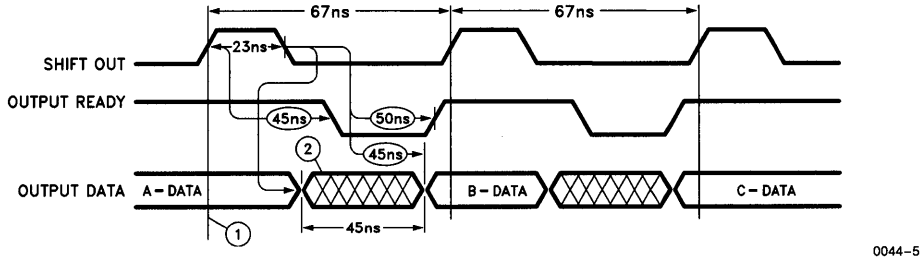


Figure 5. Output Timing for Register Array FIFO

Notes:

① The diagram assumes that, at this time, words 63, 62, 61 are loaded with A, B, C Data respectively.

② Data in the crosshatched region may be A or B Data.

remain stable for an amount of time equal to the hold time (t_{IDH}) after the rising edge of SI.

$t_{IDS} = 0$ ns

$t_{IDH} = 40$ ns

Input Timing

Figure 3 shows the timing relationships between the input data and the handshaking signals when operating at the maximum input data rate of 15 MHz. The Input Ready signal lags (follows) the rising edge of the Shift In signal by 40 ns (max.) for this two edge handshake.

Fallthrough Time

Figure 2 shows the method of entering data into the FIFO. The fallthrough time (*Figure 6*) is measured from the falling edge of the SI signal to the rising edge of the IR signal. This time is specified as $t_{PT} = 1.6$ μs (microseconds) on the data sheet.

Register Array Propagation Delay Time

The register array propagation delay time may be approximated by using the delay from the falling edge of the SO signal to the rising edge of the OR signal as being representative of the data propagation delay through the output stage and subtracting this from the fallthrough time.

Reg. Prop. Delay =

Fallthrough time − Output Prop. Delay Time

The delay per stage is then calculated by dividing the register array propagation delay time by the number of stages the data propagates through.

$$\text{Reg. Prop. Delay} = 1.6\ \mu s - 50\ ns$$
$$= 1.55\ \mu s$$
$$\text{Delay per stage} = \frac{1.55\ \mu s}{64 - 2}$$
$$= 25\ ns$$

Analysis of FIFOs (Continued)

Output Timing

Figure 5 shows the timing relationships between the output data and handshaking signals when operating at the maximum output data rate of 15 MHz. The Output Ready signal lags the Shift Out signal by 45 ns (max.) for this two edge handshake. Data is shifted to the output stage on the falling edge of SO, but does not stabilize until 45 ns later. OR goes low in response to SO going high (45 ns later) and then goes back high 50 ns (max) after the high to low transition of SO.

The reader may assume that the (new) output data is valid 50 – 45 = 5 ns before the rising edge of the OR signal, but this is incorrect. The data sheet specifies these two numbers only as maximums and not also as minimums. Evaluation of these FIFOs has revealed that the data may change several nanoseconds AFTER the rising edge of the OR signal.

The consumer is responsible for delaying the rising edge of the SO signal in order to satisfy his data setup time requirements, which may further reduce the throughput.

Full Condition

The maximum propagation delay from SI going low until IR goes high is 40 ns (*Figure 3*). The bubblethrough time for the full condition is illustrated in *Figure 7*. This time, t_{PT}, is specified as 1.6 μs on the data sheet. The delay per stage is calculated by subtracting 40 ns from 1.6 μs and dividing by the number of stages (64 − 2).

$$\text{Delay per stage} = \frac{\text{Bubblethrough time} - \text{Output Delay time}}{\text{Number of stages}}$$

$$= \frac{1.6\ \mu s - 0.04\ \mu s}{64 - 2}$$

$$= 25.16\ \text{ns}$$

Bubblethrough Time

The bubblethrough timing is illustrated in *Figure 7*. It is seen to be equal to the fallthrough time.

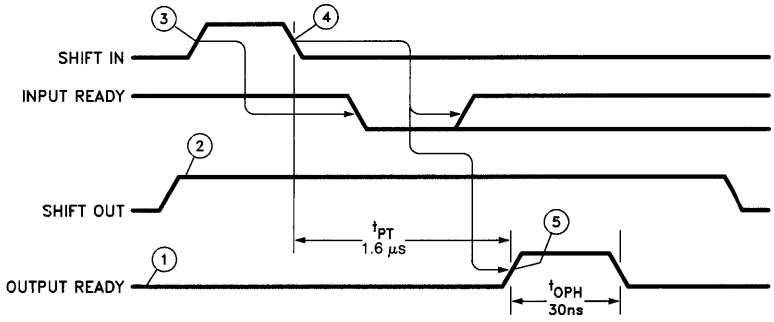


Figure 6. Fallthrough Timing

Notes:
① FIFO initially empty.
② Consumer requests data.
③ Producer enters data.
④ Data enters internal register array.
⑤ Data is available at output.

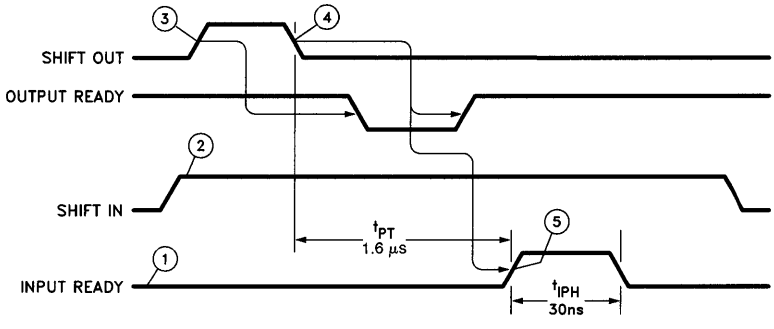


Figure 7. Bubblethrough Timing

Notes:
① FIFO is initially full.
② Shift In held HIGH.
③ Consumer reads data.
④ Empty location begins to propagate to input.
⑤ Empty location reaches input.

Analysis of FIFOs (Continued)

Maximum Throughput Calculations

The maximum throughput of the FIFO is seen to be limited by the fallthrough time when it is empty and the bubblethrough time when it is full.

The "throughput period" corresponding to the "standalone period" (t_A) and the fallthrough time (t_F) is:

$$T_{max.} = t_A + t_F$$

Converting to frequency yields

$$\frac{1}{F_{max.}} = \frac{1}{F_A} + t_F$$

Rearranging and solving for F_{max} yields

$$F_{max} = \frac{1}{\frac{1}{F_A} + t_F} \qquad \text{EQ. 1}$$

The expressions for the throughput frequencies for the FIFO under the full and empty conditions are then;

EMPTY FIFO

$$F_{in} = F_{in\,(max.)}$$

$$F_{out} = \frac{1}{\frac{1}{F_A} + t_F}$$

FULL FIFO

$$F_{out} = F_{out\,(max.)}$$

$$F_{in} = \frac{1}{\frac{1}{F_A} + t_F}$$

The maximum throughput that can be handled by a "nearly empty" or a "nearly full" FIFO operating in the standalone mode is then:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + t_F}$$

$$F_{(max.)} = \frac{1}{\frac{1}{15\ MHz} + 1.6\ \mu s} = \frac{1}{1.667\ \mu s}$$

$$F_{(max.)} = 599.88\ kHz$$

Note that this is considerably less than the 15 MHz specified on the data sheet.

FULLNESS SENSITIVITY (STANDALONE)

The number of words written into the FIFO corresponding to the fallthrough time if the input data rate is at the maximum (15 MHz) is:

$$\frac{F_{in}}{F\ fallthrough} = \frac{15\ MHz}{\frac{1}{1.6\ \mu s}} = 24\ words. \qquad \text{EQ. 2}$$

Since the bubblethrough time is the same as the fallthrough time (in this case) the same number of words can be output at the maximum data rate from a full FIFO.

What this means is that the FIFO can operate at its maximum data rate (15 MHz) only when it is between 24 words and 64 – 24 = 40 words full. In order to NOT be sensitive to its fullness, the FIFO must be operated at a maximum frequency less than or equal to the frequency corresponding to the fallthrough/bubblethrough time (625 KHz).

I propose defining a Fullness Sensitivity (FS) figure of merit for FIFOs that is a measurement of the capacity range (or fullness) over which the FIFO can be operated at its maximum input rate AND its maximum output rate. The FS is normalized; one (1) is ideal and 1 > FS > 0.

$$FS = \frac{N - F_{IA}\,t_F - F_{OA}\,t_B}{N} \qquad \text{EQ. 3}$$

Where: FS = Fullness Sensitivity in words

N = The number of words in the FIFO

F_{IA} = Standalone maximum input frequency

t_F = Fallthrough time

F_{OA} = Standalone maximum output frequency

t_B = Bubblethrough time

As an example we will calculate FS for a typical register array FIFO.

$$F_{IA} = F_{OA} = 15\ MHz$$

$$t_F = t_B = 1.6\ \mu s$$

$$N = 64\ words$$

$$FS = \frac{64 - 15\times10^{6}\times1.6\times10^{-9} - 15\times10^{6}\times1.6\times10^{-9}}{64}$$

$$FS = \frac{64 - 24 - 24}{64}$$

$$FS = 0.25$$

If the partial products would have had fractional parts we would have rounded them up to the next highest integers.

FIFO Expansion

The interconnection of two 64 word FIFOs to form a 128 x 4 FIFO is shown in *Figure 8*. Observe that the OR output of the first FIFO becomes the SI input of the second FIFO and that the IR of the second becomes the SO input to the first.

What this means is that the bubblethrough/fallthrough times serially add when the FIFOs are cascaded.

The maximum throughput that can be handled by two FIFOs cascaded together is:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + 2\,t_F}$$

$$F_{(max.)} = 306\ KHz$$

Where, as before, F_A = 15 MHz, t_F = 1.6 μs.

Analysis of FIFOs (Continued)

In general, when N FIFOs are cascaded together, the maximum throughput of the combination is:

$$F_{(max.)} = \frac{1}{\frac{1}{F_A} + N\,t_F} \qquad \text{EQ. 4}$$

The FS is also affected by the cascading of FIFOs. If N FIFOs are cascaded together the number of words that can be output or input is N times that of the standalone condition.

$$\frac{F_{in}}{F\ \text{fallthrough}} = \frac{F_A}{N\,t_F} \qquad \text{EQ. 5}$$

If this number is greater than the actual (physical) FIFO depth it means that the FIFO cannot be operated at its maximum frequency.

To make a wider word, as well as a deeper FIFO, connect the FIFOs as illustrated in *Figure 9*. Composite IR and OR signals must be generated using two external AND gates (e.g., 74LS08) to compensate for variations in the propagation delay of these signals from device to device. The maximum throughput for this configuration is 205 KHz (N = 3 in preceding formula).

Cascadability Considerations

In order to guarantee the ability of multiple FIFOs to reliably cascade with each other using the handshaking method previously described, certain conditions must be met. These are now considered.

SI or OR Signal Compatability

In the cascaded configuration, the OR signal of the Nth FIFO must be specified such that it can be detected when it is applied to the SI input of the N+1th FIFO. See *Figure 8*. This means that the minimum high time (positive pulse width) of the OR output signal of the input FIFO must be able to be recognized at the SI input of the output FIFO.

IR and SO Signal Compatability

In the cascaded configuration, the IR output of the N+1th FIFO must be specified such that it can be detected when it is applied to the SO input of the Nth FIFO.

Minimum Delay Between SI and IR

The minimum delay between SI going HIGH and IR going LOW is an unspecified parameter in the industry standard

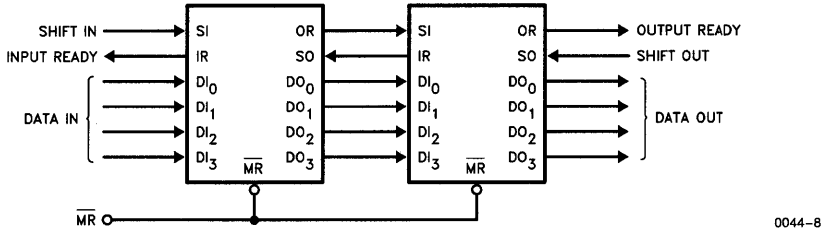


Figure 8. 128 x 4 FIFO

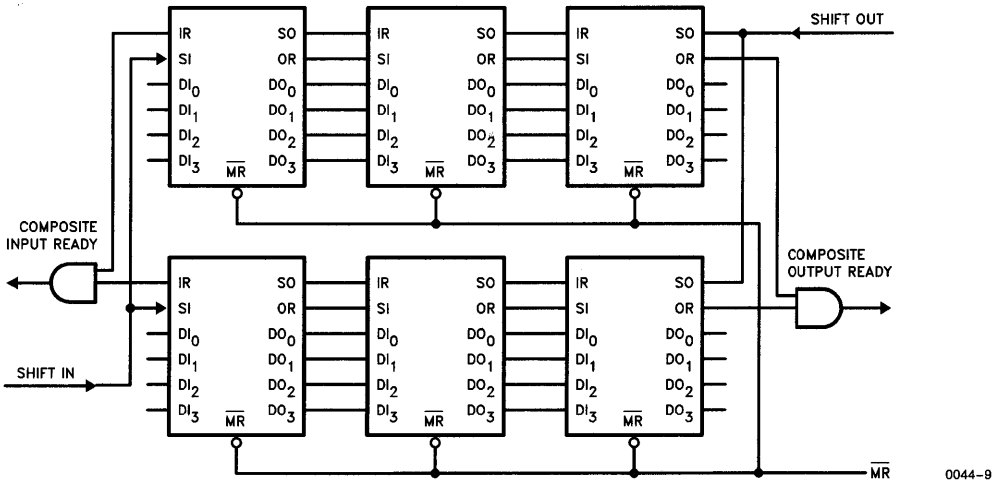


Figure 9. 192 x 8 FIFO

Analysis of FIFOs (Continued)

data sheets. The Cypress FIFO exhibits a 6 to 10 ns minimum delay. Care must be taken when mixing Cypress FIFOs and competitive FIFOs to insure that the parts will cascade with one another. In general, delaying the IR output of the Cypress FIFOs enables competitive parts to cascade with Cypress parts. The Cypress FIFO can always recognize the output of the competitive product.

Minimum Delay Between OR and SO

Another unspecified industry parameter is the delay between OR and SO. The minimum delay for Cypress FIFOs is 6 ns. A 500 pF capacitor added between the OR pin and ground and the IR pin and ground of all Cypress FIFOs will permit cascading with competitive FIFOs. These capacitors delay the signals the appropriate amount of time.

Cascading at the Operating Frequency

In order to operate at a given frequency, F_O, in the cascaded configuration the following relationship must be satisfied;

$$t_{SIH} + t_{IRH} < \frac{1}{F_O}$$

This condition is met by both the MMI and Cypress FIFOs.

Description of the CY7C401

A block diagram of the CY7C401 is shown in *Figure 10.* It is a direct, pin for pin, functional equivalent, improved performance, replacement for the register array FIFOs. The similarities and differences between the 401, 402, 403, and 404 are summarized in the table.

Product	Configuration	t_F	Package	Description
CY7C401	64 x 4	65 ns	16 pin DIP	INDUSTRY STANDARD
CY7C403	64 x 4	65 ns	16 pin DIP	Pin 1 is three-state output enable
CY7C402	64 x 5	65 ns	18 pin DIP	INDUSTRY STANDARD
CY7C404	64 x 5	65 ns	18 pin DIP	Pin 1 is three-state output enable

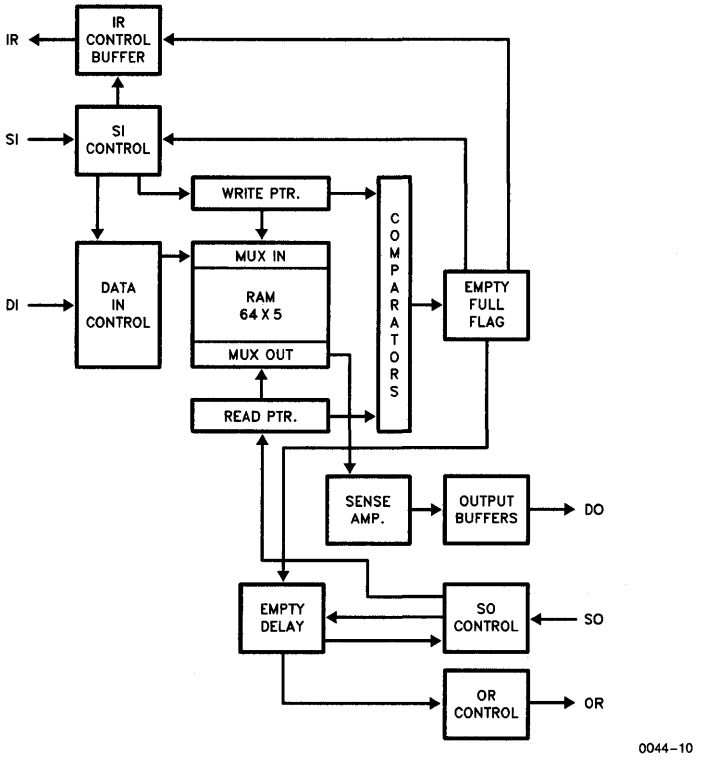


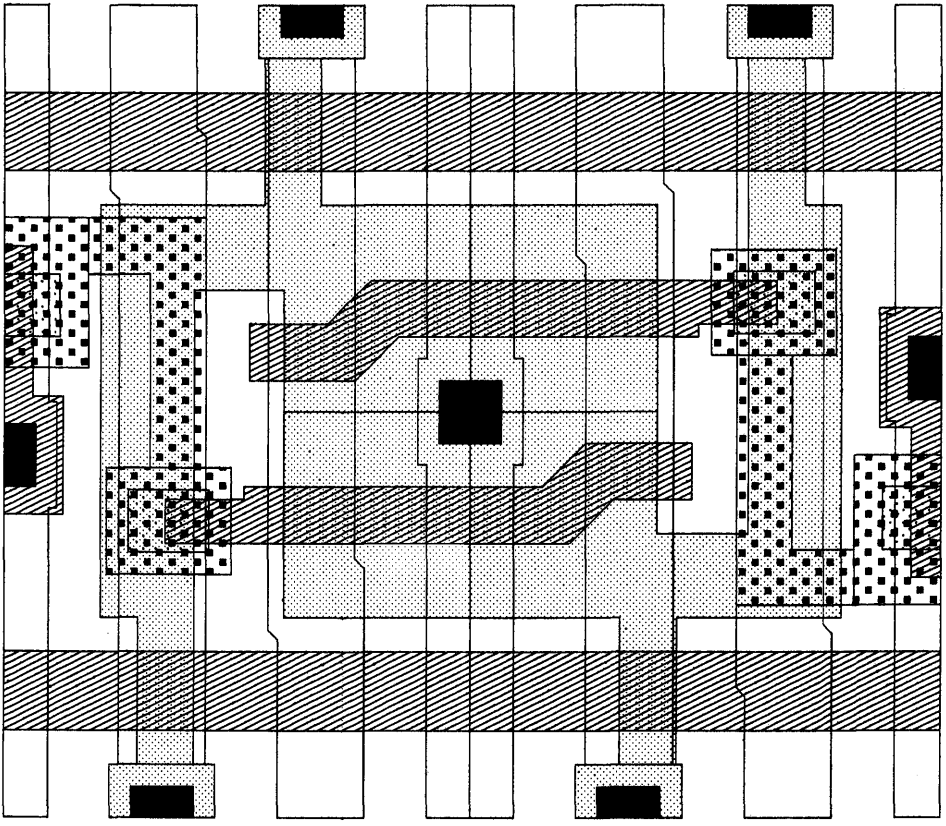
Figure 10. CY7C401 Block Diagram

Description of the CY7C401 (Continued)

Architecture Refer to *Figure 10*

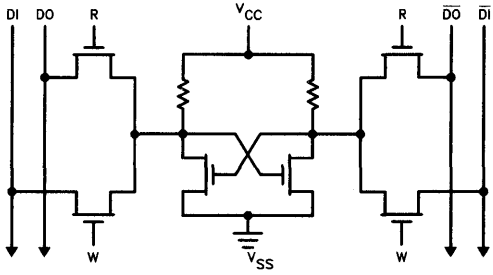
The architecture is that of a dual port RAM, which is accessed by two pointers; a read pointer and a write pointer. The input data and output data do not reside in input or output registers as in the register array architecture. Instead, the pointers address the memory locations of the input and output data. Comparators are used to control the IR and OR lines to prevent overflow and underflow. The key to this architecture is the dual port RAM cell, which is illustrated in *Figure 11*. It is only 1.2 square mils in area. Separating the read and write functions enables the memory cell to be read from and written to simultaneously and independently. This increases the basic cell size, but simplifies the overall architecture and improves the performance.

The bubblethrough time is greatly reduced (65 ns versus 1.6 μs) because it now represents the time required to update the pointers, not the time required for data to propagate through the memory array.



0044-11

Figure 11A. CY7C401 Ram Cell Layout



0044-12

Figure 11B. Cell Schematic

Description of The CY7C401 (Continued)

Functional Description

To the "outside world" the CY7C401 appears functionally equivalent to the register array FIFOs. All of the timing diagrams as well as the expansion diagrams of *Figures 8* and *9* apply.

Input data is sampled with the rising edge of the SI signal if the IR signal is high. The input (write) pointer is incremented on the falling edge of the SI signal.

Data is output with the falling edge of the SO signal if the OR signal is high. The output (read) pointer is incremented on the rising edge of the SO signal.

Output Timing

In the discussion on output timing it was pointed out that (for the register array FIFO) the way the timing of the data out with respect to OR, there is no guarantee that the data will be stable before the rising edge of OR. This time (t_{SOR}) is guaranteed to be a minimum of 5 ns on the CY7C401 data sheet.

Comparison of Register Array FIFOs and the CY7C401

Throughput

Using equation 4 the values in the following table were calculated and are plotted in *Figure 12.*

Fullness Sensitivity

Register Array FIFOs in the Standalone Mode

Equation 2 was used to calculate the number of words that could be input and output corresponding to the maximum frequency of 15 MHz. Subtracting these from the FIFO capacity (64) gives us the capacity range over which the FIFO can operate at its maximum rate. This was calculated to be between 24 and 40 words, or 32 ± 8 words. Equation 3 was used to calculate the FS and it was found to be 0.25.

Using equation 2 we have;

$$\frac{F_{in}}{F\ fallthrough} = \frac{F_A}{\frac{1}{t_F}}$$

$$= \frac{15\ MHz}{\frac{1}{67\ ns}} = 0.975\ words$$

The CY7C401 is seen to be much less sensitive to fullness than the register array FIFOs. Its capacity can range from 2 to 63 words, or 32 ± 31 words in the standalone mode.

The Fullness Sensitivities are plotted in *Figure 13.* They are also plotted in a slightly different form in *Figure 14.*

A little thought will convince the reader that Fullness Sensitivity is another way of quantifying the range of the difference between input and output data rates. The closer the FS is to 1 the greater the capacity of the FIFO to handle bursts of data.

Latency

The classic definition of latency is the difference, in elapsed time, between when a resource is requested and when it is granted. In disks, the worst case latency is the time required for one revolution of the disk. The average latency is then the time required for one-half a revolution. The assumptions are one head per track and no contention for the head.

Worst Case Latency - refer to *Figures 6* and *7*

The worst case latency for the consumer occurs when the FIFO is empty and for the producer when it is full. It is;

Where: $t_{in} + t_{out} + t_F$

t_{in} = period of the input frequency

t_{out} = period of the output frequency

t_F = Fallthrough time

Average Latency

If the FIFO is operated such that it is not sensitive to its fullness $t_F = 0$. In addition, if $t_{in} = t_{out}$ the average latency is one cycle. Otherwise, it is;

$$\frac{t_{in} + t_{out}}{2}$$

			Throughput		
	N	D	C67401A	CY7C401-5	CY7C401-25
F_A	—	—	15 MHz	15 MHz	25 MHz
t_F	—	—	1.6 μs	65 ns	65 ns
	1	64	600 KHz	7.57 MHz	9.52 MHz
	2	128	306 KHz	5.01 MHz	5.8 MHz
	4	256	155 KHz	3 MHz	3.3 MHz
	8	512	77.7 KHz	1.7 MHz	1.78 MHz
	16	1024	38.9 KHz	903 KHz	925.9 KHz
	32	2048	19.5 KHz	465.7 KHz	471 KHz

Comparison of Register Array FIFO's and the CY7C401 (Continued)

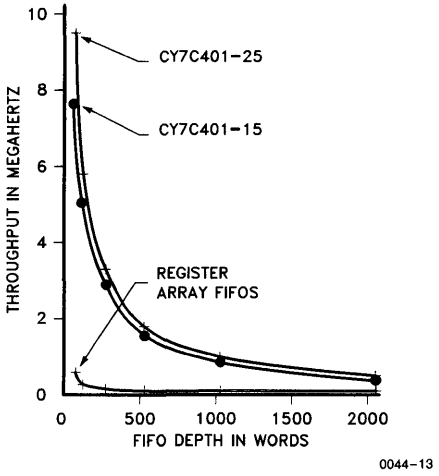


Figure 12. Maximum FIFO Throughput vs. Depth

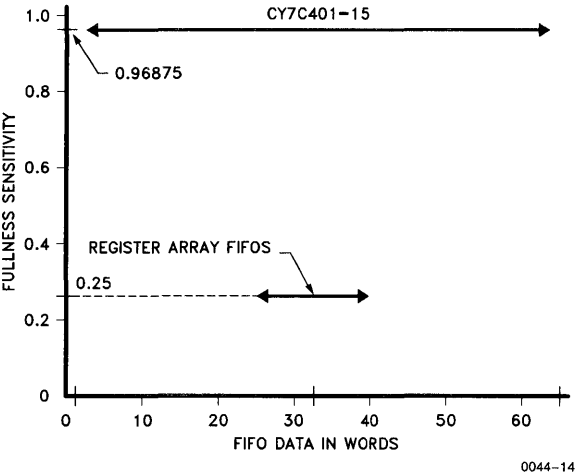


Figure 13. Fullness Sensitivity in the Standalone Mode

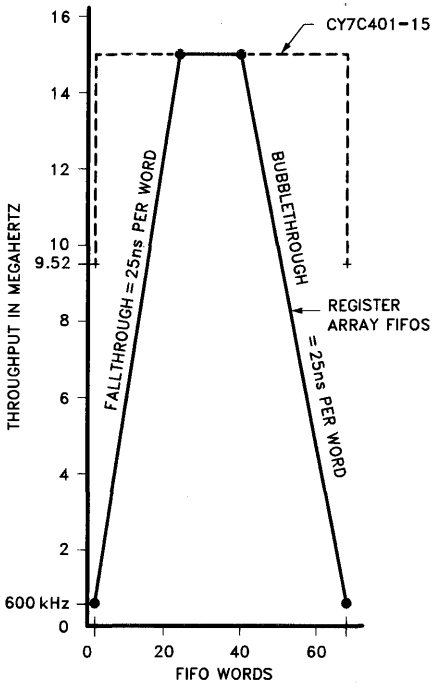


Figure 14. Standalone Throughput

Summary and Conclusions

In most systems where FIFOs are used they are neither full nor empty, except at the beginning or end of an operation. After analyzing the preceding two FIFOs the reader can understand why. Serious performance degradation occurs under these conditions, especially if the FIFO uses the register array architecture. To compensate for this, manufacturers have added one-half empty/full indicators (etc.), which has helped by alerting the system controller before the performance suffers.

A better solution to the performance problem is to use a FIFO that has the dual port RAM architecture, which has been shown to result in a superior performance FIFO.

LIST OF ILLUSTRATIONS

CYPRESS SEMICONDUCTOR

74F189 Application Brief

Introduction

There are available in the market a number of high speed 64 bit static RAMs organized 16 by 4 bits. Because of the various different manufacturers specifications, there is no apparent true second source for these products as each operates with some unique characteristics. The composite specifications contained in this applications brief will allow the interchangeable use of the Cypress CY7C189 with the 74F189 and the Cypress CY7C190 with the 74F219 with optimization for either power or performance.

Specifications

Depending on system requirements, the PERFORMANCE OPTIMIZED specification will allow the designer to select performance at the expense of power, and use either Cypress's CY7C189-18 or the 74F189 interchangeably. If, however, the major criteria is power the designer can achieve a 55 mA max power specification using the Cypress CY7C189-25 interchangeably with the 74F189 by designing with the POWER OPTIMIZED specification.

Electrical Characteristics Over the Operating Range

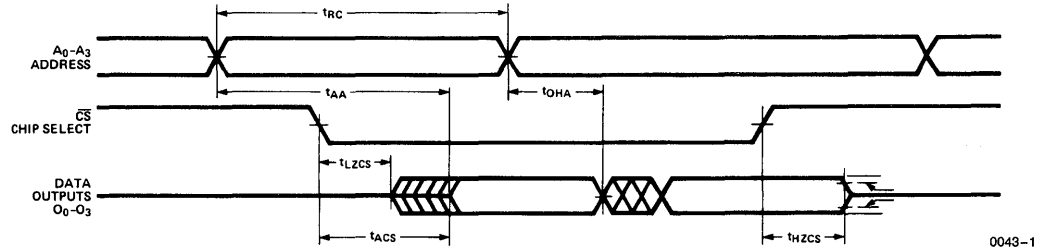
Parameters	Description	Test Conditions		Speed Optimized		Power Optimized		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.5		0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−600	+20	−600	+20	μA
V_{CD}	Input Diode Clamp Voltage							
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−150		−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		55	mA
			Military				70	mA

6

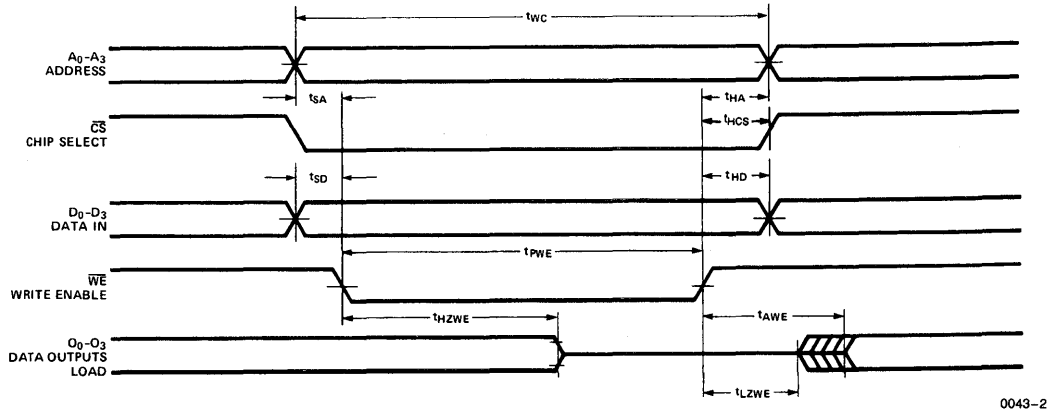
Switching Characteristics Over the Operating Range

Parameters	Description	Speed Optimized		Power Optimized		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	27		27		ns
t_{ACS}	Chip Select to Output Valid		14		15	ns
t_{HZCS}	Chip Select Inactive to High Z		12		15	ns
t_{LZCS}	Chip Select Active to Low Z		12		15	ns
t_{OHA}	Output Hold from Address Change	5		5		ns
t_{AA}	Address Access Time		27		27	ns
WRITE CYCLE						
t_{WC}	Write Cycle Time	15		20		ns
t_{HZWE}	Write Enable Active to High Z		14		20	ns
t_{LZWE}	Write Enable Inactive to Low Z		12		20	
t_{AWE}	Write Enable to Output Valid		29		29	ns
t_{PWE}	Write Enable Pulse Width	15		20		ns
t_{SD}	Data Setup to Write End	15		20		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{HCS}	Chip Select Hold from Write End	6		6		ns

Read Cycle



Write Cycle



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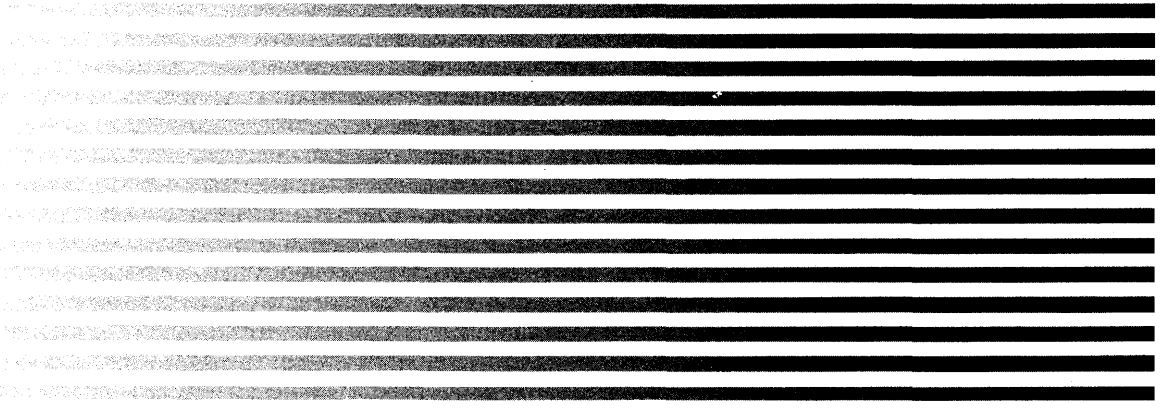

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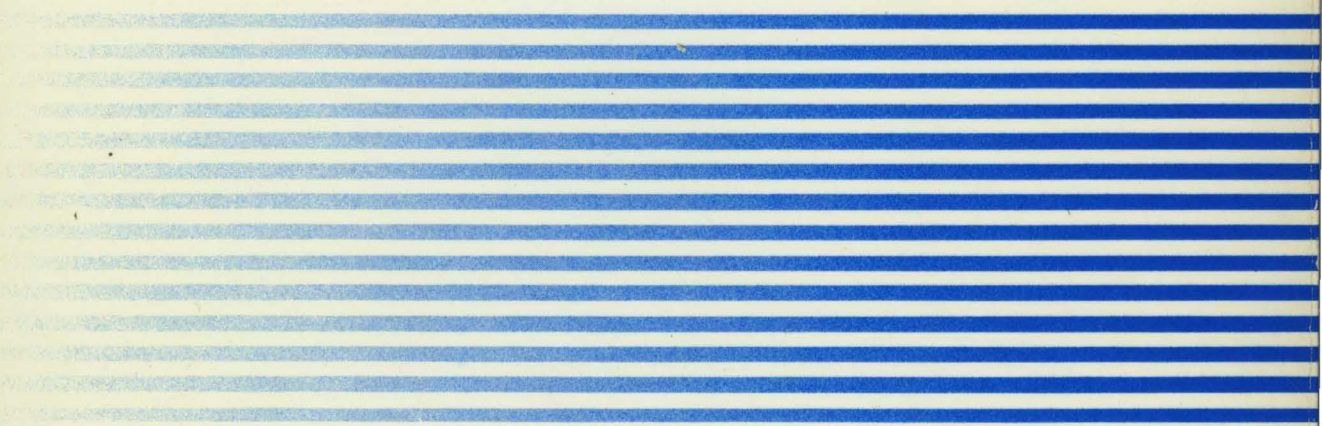

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