digital

computer interfacing accessories

and logic handbook

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contents

Foreword

This Computer Interfacing Accessories and Logic Handbook is your guide to the most extensive line of products offered by Digital Equipment Corporation for implementing logic designs. Whether you need a connector block or a cable, a general-purpose logic module or a complete interface, a computer expansion box or a cabinet for an entire system—check this handbook first. If you already know the part number of the product you need, the Index at the back is the best place to start. Otherwise go to the relevant chapter.

The major new products featured in this edition are the CHIPKIT series of integrated circuits. CHIPKITS allow exceptionally easy implementation of your interface designs for LSI-11 microcomputers, and we have included an extensive applications note in this handbook.

The largest single portion of this handbook describes our M series of TTL modules. This line ranges from basic logic gates through complete digital subsystems that make extensive use of MSI and LSI circuitry. New in this edition are the M7800 and M7860 asynchronous serial interfaces for the PDP-11 series UNIBUS.

Also featured in this handbook are the K series of high noise-immunity industrial-control modules, the A series of analog-related modules, and the W series of wire-wrappable modules, collage modules, and blank modules.

The products in this handbook, including the mounting hardware, cables, and cabinets described in the last two chapters, allow you to design and construct systems small or large, that are neat, modular, and compatible—with a minimum of lost time and effort.

If you need unique functions that you don't find covered in this handbook, contact your local DIGITAL sales office. The hardware product you need may be available as a non-standard item, or could be provided by our Custom Module Products Group or Custom Enclosures Products Group. These groups can design, manufacture, and test not only modules, but also the hardware, accessories, and enclosures to make a complete system.

A worldwide staff of DIGITAL sales engineers is prepared to respond to your technical and commercial needs. From a backlog of logic system design experience, DIGITAL may have a detailed solution to your application or interface requirement.

A separate price supplement booklet is available for various countries.

Please address any comments on this handbook, or inquiries concerning special services, to:

Digital Equipment Corporation
Logic Products Sales Support, MK1-2/E 13
Merrimack, NH 03054

DIRECT SALES CATALOG

We would also like to direct your attention to the latest concept in purchasing computer-related equipment—the DIGITAL Direct Sales Catalog. By ordering products directly through the Catalog, you may save substantial dollars. Many of the items (terminals, microcomputers, interface modules, hardware/accessories, etc.) in this Handbook are now available for purchasing through the Catalog. To find out if this Catalog program can benefit you, mail in now the post card attached elesewhere in this book. The Catalog program is applicable to ordering and shipping points in the U.S.A. only.

general information

LOGIC PRODUCTS FOR COMPUTER INTERFACING

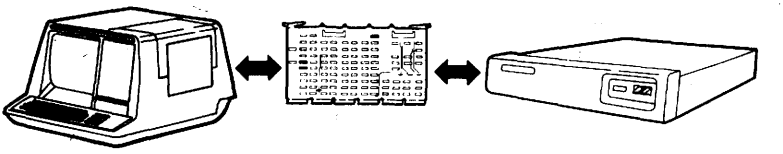


Figure 1 An Interface is a Bridge for Data Transfer

Whenever an "outside world" device such as a terminal, printer, or lab instrument is to be used with a computer, an intermediate unit called an interface (Figure 1) is needed as a bridge for data transfer. The interface formats and controls communication of data, sometimes in both directions, and performs many essential functions in the process. For example, consider a terminal keyboard being used for input to a PDP-11 series computer. A typical keyboard might send a few characters per second, in serial format at the 20 mA current-loop signal level. The PDP-11 UNIBUS, on the other hand, accepts only parallel data at TTL signal levels, and requires a specific sequence of signals—the handshaking routine—to be sent and received before any data can be accepted. Data must be stored for a short time, as the computer is normally busy with another task at the instant a key is struck. Further, the start and stop codes must be stripped off, and a keyboard device number, status, task priority, and interrupt vector must be supplied. All of these requirements for translating the keyboard output into computer-usable form can be met by the suitable UNIBUS input interface. Interfaces also perform other functions in some cases, such as time-of-day clock generation.

Although the number of possible interfaces is nearly infinite, fortunately there are certain common elements in all interfaces intended for a particular computer bus structure. This allows DIGITAL to offer you functional logic modules for building the basic I/O bus portion of any needed interface, freeing you to concentrate on designing the part that is unique to your own application. And for the more-usual peripheral devices, like the terminal just mentioned, we offer complete, plug-in, ready-to-go interfaces—available off-the-shelf.

To see what interfaces and functional modules are available through this Handbook for your computer, check the appropriate Interface Selector chart:

PDP-11 UNIBUS page 50
PDP-8 OMNIBUS page 23
LSI-11 bus page 130

Product details are given right after the charts. If you need more technical information or applications assistance, call our toll-free Hot Line, 8:30AM to 5:00PM Eastern time, 800-258-1710. From New Hampshire locations, or places outside the continental U.S., call Merrimack, 603-884-6660. To order, see the How to Order section on Page 488.

Even if no product in this Handbook meets your requirements, DIGITAL may still be able to supply a suitable item—possibly a brand-new or non-standard product, or one custom designed and manufactured by our Custom Module Products Group or Custom Enclosures Products Group. Check with your DIGITAL Field Sales contact, or call the Customer Service desk at your nearest Field Sales office. They can advise you of the part number, price, delivery, and support literature for any available DIGITAL product, and route you to the person who can provide support in greater depth if needed. To discuss custom-designed hardware, contact Logic Products Sales Support at DIGITAL, MK1-2/E13, Merrimack, NH, 03054.

RELATED LITERATURE

Listed below are DIGITAL documents that supplement the material provided in this Handbook. These documents can be obtained from your nearest DIGITAL Field Sales office.

HARDWARE/ACCESSORIES CATALOG EK 04517
PDP-11 PERIPHERALS HANDBOOK EB 05961
PDP-11/04/34/45/55/60 PROCESSOR HANDBOOK EB 09430
PDP-8/E, 8/F, 8/M SMALL COMPUTER HANDBOOK EB 02546
MICROCOMPUTER HANDBOOK EB 07948
PDP-8/A MINIPROCESSOR HANDBOOK EB 06219

A wide range of hardware and software manuals, configuration guides, and application notes is also available.

BASIC HARDWARE NOMENCLATURE

Although DIGITAL nomenclature generally conforms to industry standards, a few terms are unique. These are presented in Figure 2, which shows a more-or-less typical subsystem that could contain several computer interfaces, assembled from products in this handbook.

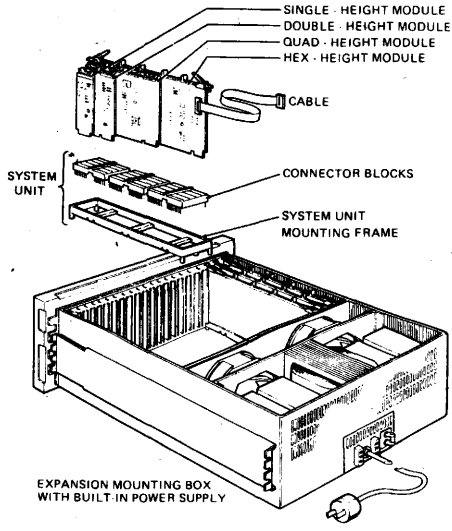


Figure 2 Typical Subsystem

MODULES are the heart of any system, and of this handbook. The term at DIGITAL refers to any plug-in printed circuit board, whether completely blank, provided with IC pads and connections, or fully assembled as a working entity. Physically, modules are available in four "heights," two "lengths," and three "widths," as defined on the next few pages.

A SYSTEM UNIT is a set of MODULE CONNECTOR BLOCKS in a MOUNTING FRAME which in turn mounts to an expansion mounting box or other support such as a rack panel. System units are available in several versions, four slots or nine slots wide, and with or without prewiring for power, ground and bus signals. The connector blocks and mounting frames are also available separately.

An EXPANSION MOUNTING BOX is a rack-mountable, fully enclosed chassis for circuitry that cannot be housed within a computer's own enclosure. Also known as expansion mounting chassis, they are available in several sizes and configurations. The example shown is the popular BA11-KE, used most often for expansion of PDP-11 systems. It has its own multivoltage power supply and cooling fans built in.

IMPORTANT NOTE

When you specify DIGITAL products, be sure to give the complete and correct type number. Prefixes and suffixes, where used, are highly significant.

MODULE CONTACT FINGER AND MODULE CONNECTOR BLOCK CONTACT IDENTIFICATION

DIGITAL plug-in (FLIP CHIP) modules have contact fingers either on one side (single-sided modules) or on both sides (double-sided modules). Modules with contact fingers on only one side always have them on side 2 (the solder side) (Figures 3, 4, 5, 6). DIGITAL module connector blocks have module slots with contacts either on one or on both sides. Modules with contact fingers on only one side can be plugged into connector blocks with contacts on both sides of the module slots; then electrical contact between the module and the connector block is only via module slot side 2 contacts. The module contact fingers and connector block contacts are identified by alphanumeric codes. These alphanumeric codes are used throughout this handbook, the HARDWARE ACCESSORIES CATALOG, the PERIPHERALS HANDBOOK, individual module data sheets, engineering drawings, and other DIGITAL publications. This coded numbering scheme must be understood to ensure proper system interconnections. Letters G, I, O, Q, W, X, Y, and Z are not used in this numbering scheme.

DIGITAL modules are SINGLE-HEIGHT, DOUBLE-HEIGHT, QUAD-HEIGHT, or HEX-HEIGHT; STANDARD LENGTH or EXTENDED LENGTH; and SINGLE-WIDTH or DOUBLE-WIDTH. Each DIGITAL module is a specific, fixed size; the size of each module is stated in the module description in the previously mentioned DIGITAL publications. DIGITAL SINGLE-HEIGHT and DOUBLE-HEIGHT modules are STANDARD LENGTH or EXTENDED LENGTH. DIGITAL QUAD-HEIGHT and HEX HEIGHT modules are usually EXTENDED LENGTH. Any DIGITAL module can be SINGLE-WIDTH, DOUBLE-WIDTH or TRIPLE-WIDTH; most, however, are SINGLE-WIDTH.

The height and length requirement is determined by the quantity and size of discrete components and integrated circuits located on side 1 of the module, and, to some extent, by the amount of etched printed circuitry on sides 1 and 2. The width requirement is determined by the distance the largest component extends from its mounting surface on the module.

All DIGITAL module connector blocks accommodate any height (standard or double) module. The length of the modules to be used in a logic system must, however, be considered when connector block mounting is being selected; enough space must be provided to accommodate the longest module. DIGITAL's STANDARD-LENGTH modules are 5.40/5.60 in. (13.72/14.22 cm) long and EXTENDED LENGTH modules are 8.84/9.04 in. (22.58/22.96 cm) long from the bottom of the contact fingers to the top of the attached handle(s).

All DIGITAL module connector blocks accommodate any width (single or double) module. The width of the module must be considered, however, when any connector block module slot is occupied by a DOUBLE-WIDTH module; this is because no module can be inserted into the module slot on the immediate right on the same connector block unless that connector block provides sufficient space between module slots for the mounted components, i.e., an H808 Module Connector Block. DIGITAL's SINGLE-WIDTH modules require 0.338/0.348 in. (0.859/0.884 cm) for conductive components and 0.370/0.380 in. (0.940/0.965 cm) for nonconductive components. DOUBLE-WIDTH modules require 0.820/0.839 in. (2.106/2.131 cm) for conductive components and 0.870/0.880 in. (2.210/2.235 cm) for nonconductive components. These component space requirements are the distance from the module's side 1 surface to the side 2 surface of the module mounted on the immediate right. Normal module spacing is on half-inch centers.

Connector blocks are available for SINGLE- and DOUBLE-HEIGHT modules. QUAD-HEIGHT modules require two connector blocks mounted end-to-end, and HEX-HEIGHT modules require three. Figure 7 shows modules in the various sizes as typically mounted in a system unit, and identifies the slots. Figure 8 gives the outline dimensions of the modules.

SINGLE-HEIGHT modules (Figure 3) are 2.417/2.452 in. (6.139/6.228 cm) high, and are available in both standard and extended length. They can be plugged into either row of a double-height connector block.

DOUBLE-HEIGHT modules (Figure 4) are 5.167/5.202 in. (13.124/13.213 cm) high, and are available in both standard and extended length. They occupy both slots of a double-height connector block, and a key on the block mates with a notch on the module to ensure that the module has been plugged in the correct way.

QUAD-HEIGHT modules (Figure 5) are 10.437/10.472 in. (26.510/26.599 cm) high, and are always of extended length. They occupy two slotted-end, double-height connector blocks, and are keyed to ensure correct insertion.
HEX-HEIGHT modules (Figure 6) are 15.668/15.693 in. (39.796/39.860 cm) high, and are always of extended length. They occupy three slotted-end, double-height connector blocks, and are keyed to ensure correct insertion.

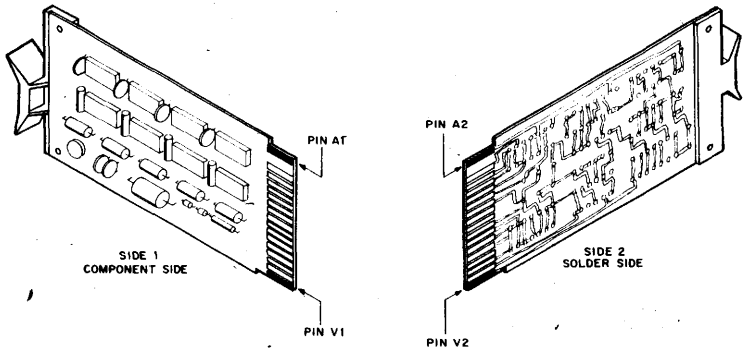


Figure 3 Single-Height Module

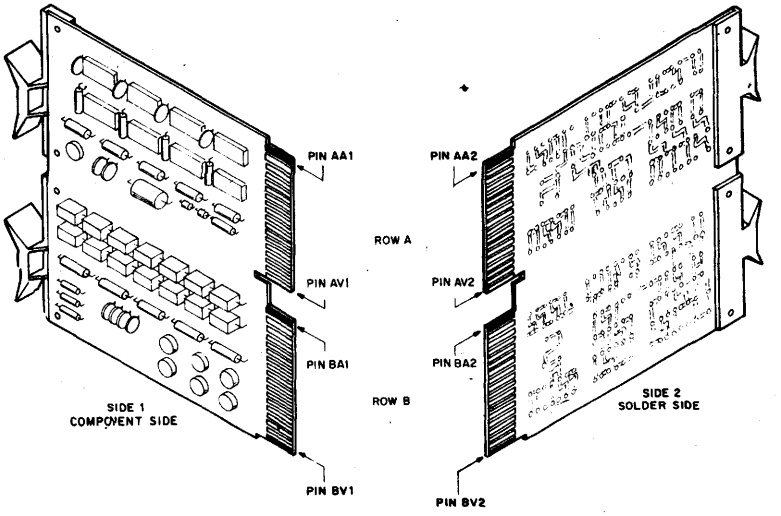


Figure 4 Double-Height Module

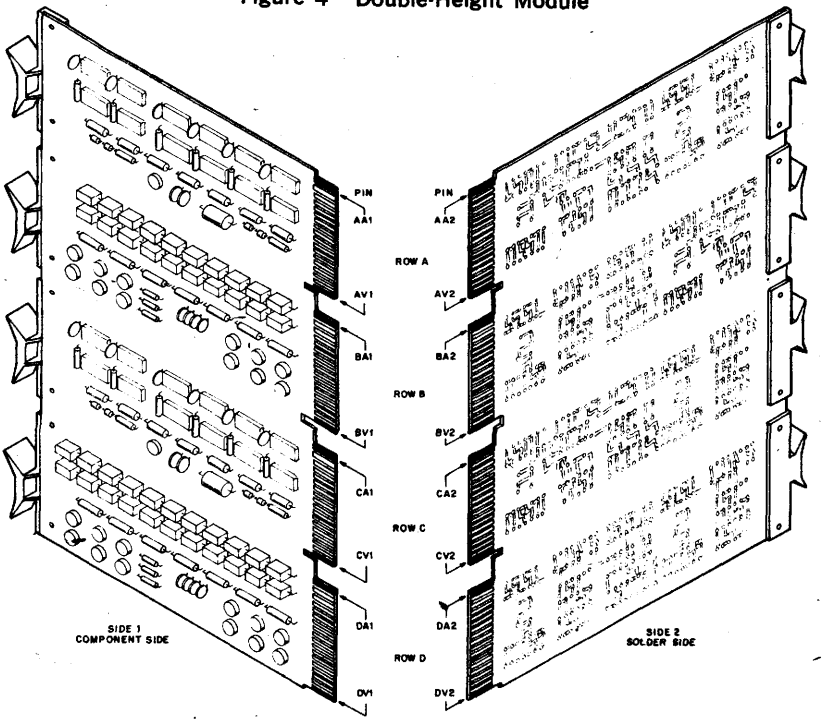


Figure 5 Quad-Height Module

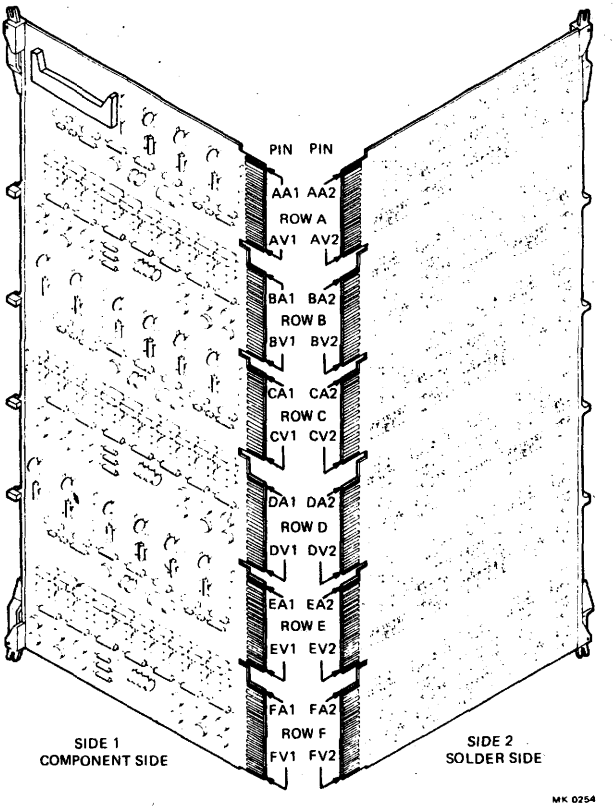


Figure 6 Hex-Height Module

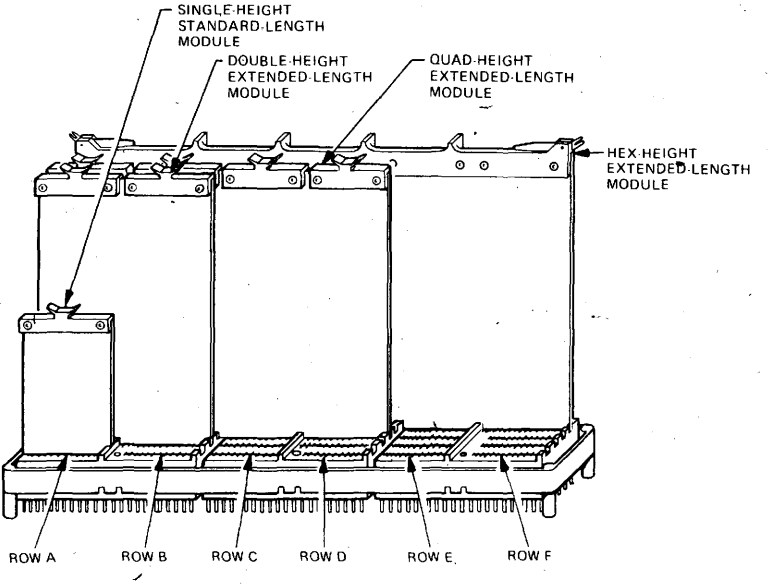


Figure 7 Connector Block Slot Identification

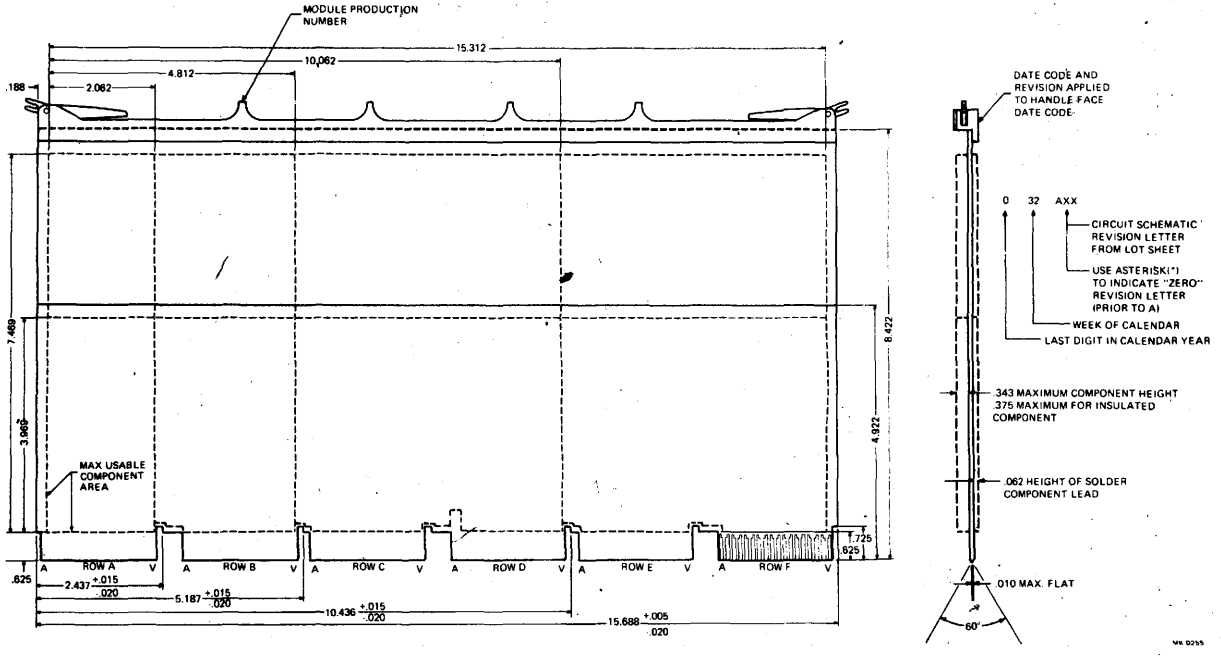


Figure 8 Module Dimensions

MODULE CLEANING

Occasionally, modules which have been in service for a long period of time may develop resistive coatings on their gold-plated fingers. This coating, if allowed to build up, can cause malfunctions by decreasing the noise margin of a circuit.

There are two types of foreign material coatings which can develop on the gold-plated fingers of a module. The first type is INORGANIC. This type of contamination results when copper "bleeds" through the gold plating and oxidizes. This oxidized layer builds up and can create contact resistances of significant consequence. Inorganic contamination is strictly a matter of time; however, extremely dirty environments will speed up the process. For this reason, care should be taken to locate modules and systems in an area as free from smoke, pollution, and other air-bound particles as possible.

The second form of contamination involves ORGANIC substances, which usually are a result of careless handling, and are mainly made up of fingerprints, salts, and oils deposited when the modules are handled by the gold-plated fingers. Contamination by organic substances can be greatly reduced by careful handling of the modules.

Although the backplane connectors are of the self-cleaning type (e.g. fingers and contacts clean upon insertion), it may become necessary to clean the module fingers to ensure reliable connection. When it has been determined that the module fingers are in need of cleaning, the following procedure is recommended.

Inorganic Contaminants

Immerse the fingers of the module in an ultrasonic bath of deionized water and a detergent, such as Liguinyx, for at least 30 seconds. Repeat with pure deionized water only.

It is now necessary to remove the water from the module fingers. This should be done immediately following the ultrasonic rinse since water will damage the module fingers if allowed to remain. The water can be removed by immersing the module fingers in an ethanol or methanol bath to the same depth used during the ultrasonic cleaning. Never wipe or use an abrasive cleaner on the module fingers. If wiping is necessary, the use of K-Dry is recommended.

Organic Contaminants

After inorganic contaminants and water have been removed, organic materials may be removed by immersion of the module fingers in trichloroethane for at least 30 seconds. The fingers can then be allowed to dry or may be wiped clean with a very fine, non-abrasive material such as K-Dry towels. In no case should an eraser ever be used on module fingers. **The use of abrasive cleaners or erasers on modules will be considered physical abuse to the module and may void the module warranty.**

SPECIAL SYMBOLS AND ABBREVIATIONS

Logic symbols used in this handbook conform, in general, to widely accepted MIL standards. All basic M Series logic symbols (AND, OR, NAND, NOR, Inverter, Flip-Flop) are described in the introduction to the M Series logic and control modules.

Input Loading and Output Drive

On the logic diagrams of this handbook, input and output loading, expressed in TTL unit loads, appear in boxes terminating each input or output signal line. In the 2-input NAND gate example of Figure 9, both inputs (pins A1 and B1) present one TTL unit load. The output (pin C1) is capable of driving 10 TTL unit loads. The aarrows indicate the direction of signal flow.

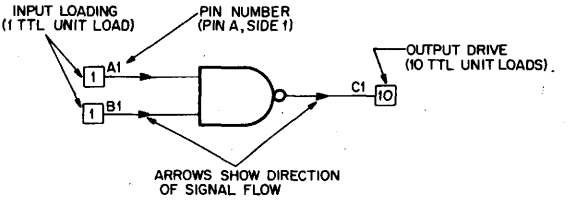
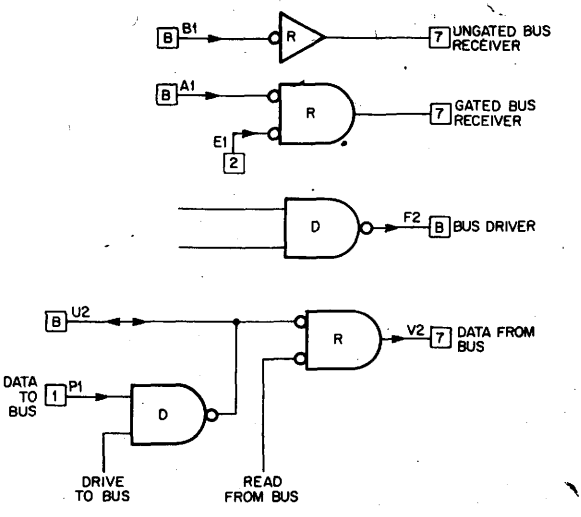


Figure 9 Logic Diagram Input Loading and Output Drive Symbols

Bus Drivers and Receivers

Drivers and receivers that transfer data along the bidirectional transmission lines of the PDP-8/e, 8/f, 8/m, 8/a OMNIBUS, the PDP-11 UNIBUS, or the LSI-11 bus differ somewhat from similar TTL NAND gates or inverters. Typical examples are shown in Figure 10. The "B" in the loading box indicates that the driver or receiver circuit is to be connected to a bus signal or control line. "R" identifies a line receiver and "D" identifies a line driver. Inputs to line receivers or drivers may also be standard TTL levels, in which case, TTL unit loads are shown as usual in the loading box.



TYPICAL BUS TRANSCEIVER ARRANGEMENT

Figure 10 Bus Driver and Receiver Symbols

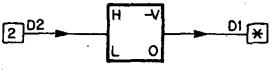
Electrical characteristics of these circuits are described in the introduction to M Series Computer Interfacing Modules.

Level Converters

Whenever logic levels are translated from one set of voltages to another, the conversion is shown taking place in a square level-converter symbol. Inside the box, the corresponding logic levels are related in a simple truth table.

The example of Figure 11 shows a level converter stage that accepts TTL levels (LOW and HIGH) and delivers DEC negative voltage levels (—3 V and ground).

Input loading is two TTL unit loads. Whenever loading is peculiar, it is defined in a note on the drawing as in the output of Figure 11.



*=SINKS 20mA AT GROUND

Figure 11 Typical Level Converter

Special Analog Symbols

Symbols used on analog circuit drawings to represent multiplex switches and operational amplifiers are shown in Figure 12. Loading boxes for analog inputs and outputs contain the letter "A"; do not connect such signals to logic levels.

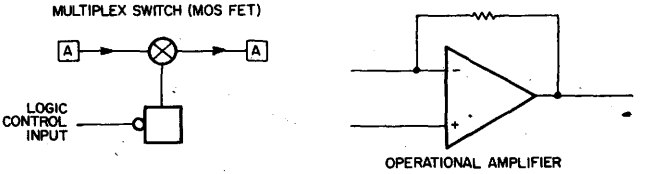


Figure 12 Special Aanalog Symbols

Signal and Function Names

Inputs and outputs of M Series logic modules may be assigned a signal name, a function name, or both. (See Figure 13.) Signal names appear *outside* blocks or logic symbols to identify typical input or output signals.

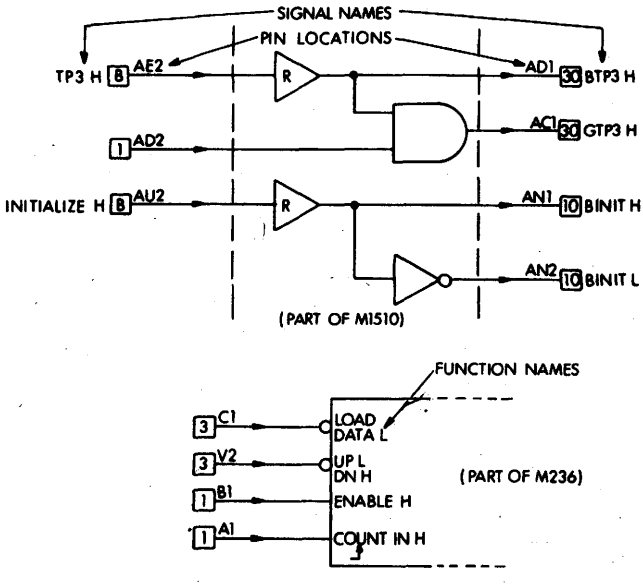


Figure 13 Signal and Function Names

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic, separated by a space. This letter indicates the asserted (true) state of the signal. An H means the signal is asserted when HIGH (+3 V) and an L means the signal is asserted when LOW (0 V). For example, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

On the logic diagrams of many computer interfacing modules in this handbook, signal names peculiar to one computer, such as the PDP-11, appear as an example of typical usage. Signal names may be changed to those of another computer or interfacing device if logically appropriate.

Function names appear *inside* the blocks of functional modules. They identify the *function* of input or output signals. The user may add his own signal names.

Abbreviations

Abbreviations used in signal and function names in this handbook are defined in Table 1.

Table 1—Abbreviations

ABBREVIATIONS	DEFINITION
ALTN	Alternate
AMPL	Amplifier
ANLG	Analog
BPS	Bits Per Second
CAP	Capacitor
CLR	Clear
CMPR	Compare
COM	Common
CONT	Control
CVRSN	Conversion
DAC	Digital to Analog Converter
EXT	External
GND	Ground
H	High (TTL + 2.0 to +5.0 V Logic Level)
INIT	Initialize
INT, INTR	Interrupt
INTL	Internal
L	Low (TTL 0.0 to 0.8 V Logic Level)
OUT	Output
P.I.	Program Interrupt
POT	Potentiometer
PRGM	Program
REF	Reference
RTN	Return
SER	Serial
S.H.	Sample and Hold
TRIG	Trigger

MINICOMPUTER INTERFACING MODULES
PDP-8, PDP-11 SERIES COMPUTERS—
INTERFACING SELECTOR GUIDE

M SERIES MODULES FOR COMPUTER INTERFACING

INTRODUCTION

Design and support of interfaces for PDP computers is a major function of M Series modules. This edition of the Logic Handbook emphasizes a collection of modules for interfacing to the following processors:

INTRODUCTION

Design and support of interfaces for PDP computers is a major function of M Series modules. This edition of the handbook emphasizes a collection of modues for interfacing to the following processors:

—PDP-8 Family
- PDP-8/A, 8/E, 8/F, 8/M (OMNIBUS)

—PDP-11 Family

This section consists of a separate subsection for each processor. Within each subsection there is a brief overview of interfacing theory, an Interface Selector chart, and individual descriptions of related modules.

PDP-8 FAMILY COMPUTER INTERFACING

The PDP-8 family of computers remains the undisputed leader in the minicomputer industry with over 20,000 installations to date. Since its inception in 1964, the PDP-8 has been continually improved. Each model has become more powerful, more efficient, and faster. At the same time, system cost and size have been reduced to less than 25 percent of original figures. More importantly, these improvements have been made without sacrificing software and hardware compatibility. Programs written for the earliest PDP-8 can be run on the newest PDP-8; peripheral devices that operated with earlier PDP-8s can be made to operate with the latest PDP-8.

This section contains hardware interfacing information and related I/O module descriptions for all PDP-8 models listed.

—OMNIBUS—PDP-8/A, 8/E, 8/F, 8/M

The non-OMNIBUS-related modules are contained in the Traditional Modules section.

PDP-8/A, 8/E, 8/F, 8/M (OMNIBUS) Interfacing

This subsection consists of general interfacing information for the PDP-8/A, 8/E, 8/F, and 8/M processors, followed by detailed descriptions of related modules.

General OMNIBUS Interfacing Principles

The PDP-8/A, 8/E, 8/F, and 8/M are the newest 12-bit word length processors offered by DIGITAL. These processors utilize the OMNIBUS concept for transferring commands and signals among modules within a system.

Physically, the OMNIBUS is an etched board with rows of module connectors soldered to the board. The pin assignment is the same on all connectors. The OMNIBUS consists of 96 signals which feed to 96 pins on the connectors. The user is generally only concerned with those signals that control data transfers, address memory, or contain the data to be transferred. However, the additional signals, such as timing, are readily available on the OMNIBUS to accommodate any tailor-made requirement in the event that the user

should design and build his own interface module. A single OMNIBUS assembly accommodates 20 PDP-8/A, 8/E, 8/F, or 8/M modules.

The OMNIBUS bus structure employs bidirectional data and control lines plus a few undirectional control signals. Each bus line is a matched and terminated transmission line that must be received and driven with devices designed for that specific application. All M Series modules designed for interconnections to the OMNIBUS employ special high-impedance bus driver and bus receiver circuits appropriate for such bus lines. All drivers (identified by a "D" in the logic symbol) are open-collector gates that control the bus through a wired-OR connection. All receivers (identified by the "R" in the logic symbol) are high-impedance gates that present a minimum of loading to the bus line.

A module may have unused bus driver or bus receiver circuits that can be used with TTL devices, provided the following loading rules are observed:

Receiver Loading: The bus receiver input presents two TTL unit loads (in the High state) to a TTL output and has a normal fan-out of 10.

Driver Sink Capability: The open-collector bus drivers are capable of sinking at least 50 mA, with a collector voltage of 0.8 volts or less. The collector voltage, when not sinking current, must be less than +6 volts. Leakage current (in the High state) is less than 25 μA. The input of a bus driver presents a single TTL unit load to a TTL output.

There are three types of data transfer: programmed data transfers, program interrupt transfers, and direct memory access transfers. Programmed data transfer is the easiest and most direct method of handling data I/O. Program interrupt transfers provide an extension of programmed I/O capabilities by allowing the peripheral device to initiate a data transfer. The data break system uses direct memory access for applications involving the fastest data transfer rates.

Table 1 lists and describes the signals on the OMNIBUS-related processors that are used for programmed and interrupt I/O control. More complete descriptions for these and data break transfer signals are contained in the SMALL COMPUTER HANDBOOK.

Table 1. OMNIBUS I/O Signal Summary

SIGNAL	DEFINITION
MDO-11	Contains the device select code for an I/O instruction. Bits 3-8 contain the device select code; bits 9-11 specify the operation select code within that device.
I/O PAUSE L	Asserted by the processor when the instruction is an I/O instruction ($6XXX_8$).
TP3H	TP3H is normally used to clock data into the output buffer of an output interface.
INTERNAL I/O L	INTERNAL I/O is asserted by the interface to indicate to the processor that the selected device is not on the External I/O Bus.

Table 1. OMNIBUS I/O Signal Summary (Continued)

SIGNAL	DEFINITION
DATA0-11	The 12 DATA lines called DATA BUS serve as a bidirectional bus for both input and output data between the AC register in the processor and the interface buffer register.
C lines C0, C1, C2	Signals C0, C1, C2 are asserted by the interface during I/O instructions to notify the processor whether data is to be placed onto the DATA BUS or received from the DATA BUS by the processor.
INT RQST L	INT RQST is the method by which the device signals the processor that it must be serviced. The processor will then branch to a subroutine which issues a skip IOT to each device to identify the one that is interrupting.
SKIP L	Asserted by the interface as the result of a skip IOT if an interrupt is being requested. Used to identify the interrupting device by causing the processor to skip the next instruction.
BUS STROBE L	BUS STROBE is used to load the AC and PC registers. Unless special I/O operations are being performed, the designer of an interface need not concern himself with BUS STROBE.
NOT LAST XFER L	A ground level on this line indicates to the processor that the next BUS STROBE does not terminate the I/O transaction. Typical I/O tranfers will not use this signal.
RUN L	When low, RUN indicates that the machine is executing instructions. Can be used to notify an interface that the processor has stopped.
TS1 L TS2 L TS3 L TS4 L TP1 H TP2 H TP3 H TP4 H	These are the internal machine cycle time states and time pulses. Each time state precedes its corresponding time pulse. Time states are always 200 ns or more in duration, and change 50 ns after the leading edge of the time pulse. Time pulses are 100-ns positive-going pulses. The exact spacing of the timing pulses is a function of fast or slow cycle. Only TP3H is used in the typical interface.
INITIALIZE H	INITIALIZE is a positive-going 600-ns pulse used to clear AC, LINK, and flags in peripherals. It is generated when power is first applied to the processor, by the Clear key on the console and by IOT 6007.

The following is a brief summary of the basic sequence of I/O transactions for programmed data transfers and interrupt data transfers. This information is provided here as a general reference aid; detailed descriptions are contained in the SMALL COMPUTER HANDBOOK and MINIPROCESSOR HANDBOOK.

For programmed data transfers, the computer program issues an input/output instruction to, first, select the desired peripheral and, second, direct the peripheral to generate certain operating control signals called IOTs. The input/output instructions are transmitted to the peripheral via the MD (Memory Data) lines 00 through 11. Each peripheral contains circuitry that monitors the MD lines. MD03 through MD08 carry a device selection code which is unique for each peripheral. Lines MD09 through MD11 carry command operate signals that the selected peripheral must translate into one of eight IOT functions for that device. Signal I/O PAUSE is also generated by the processor at this time. I/O PAUSE notifies all peripherals that the MD lines contain an I/O instruction. Note that the interface does not have to monitor MD lines 0-2 to detect a 6. I/O PAUSE occurs after the MD lines have settled and is used to actually gate the device select and the operation codes into the interface.

The IOT functions vary depending upon the type of peripheral but generally, they consist of sampling and clearing status flags and reading, loading, and clearing data buffers. For data inputs into the processor, the interface bus drivers are enabled by the appropriate IOT. For data outputs from the processor, the IOT is gated with TP3 H and the resulting signal is used to load the desired output register. The Control lines (C0, C1, C2) must be configured by the device interface during an I/O instruction to notify the processor of the type of transfer that will occur between the device and the processor. These lines control the data path within the processor and determine if data is to be placed onto the data lines (output) or received from the data lines (input). The INTERNAL I/O signal must also be generated to notify the processor that an extended cycle is not needed.

The interrupt facility is a more efficient method of I/O transfer. This method includes all of the above elements of programmed data transfers except the time of transfer. Instead of waiting for the processor to check the peripheral, the peripheral signals the processor that it has data to be serviced by asserting the INT RQST line. The processor interrupt system detects the INT RQST signal and enters a subroutine to determine the identity of the requesting device by sending an I/O instruction to each peripheral which causes the SKIP line to be asserted if the peripheral is asserting the interrupt signal. When this identity has been established, a servicing subroutine causes the peripheral to enter a normal programmed data transfer sequence.

PDP-8 OMNIBUS-RELATED INTERFACING MODULES

Table 2 summarizes the interfaces and related modules that are described in detail on the following pages.

Although each interfacing problem is likely to have some unique aspects, the steps to follow in general are:

1. Determine your interfacing requirements.
2. Match these requirements against the products listed in Table 2, then read the detailed descriptions.
3. Select suitable products if any are listed. If no listed products meet your requirements, contact your DIGITAL Field Sales office to find if any other DIGITAL products can perform the needed functions.
4. Add the power and mounting space requirements of all modules to be employed, and note the cables needed plus any prerequisites and restrictions that apply.
5. From the appropriate sections of this Handbook and the Hardware/Accessories Catalog, select the cables, power supplies, and mounting hardware to complete your system.

If you need technical assistance with any product in this Handbook, feel free to call DIGITAL's toll-free Hot Line, 8:30AM to 5:00PM Eastern time, 800-258-1710. From New Hampshire locations or places outside the United States, call Merrimack, 603-884-6660.

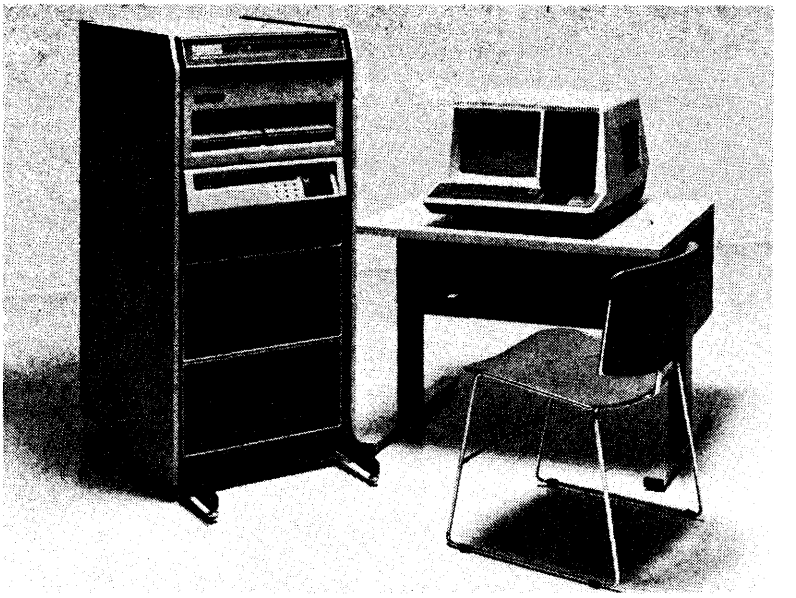


Table 2 Interface Selector Guide—PDP-8 OMNIBUS

DEVICE OR FUNCTION	MODULE OR OPTION	LOGIC H'BOOK PAGE[3]	POWER +5V AMPS[1]	MODULE SIZE L H W[2]		CABLE REQ'D	COMMENTS
2-word parallel input interface	DR8-ED		1.5	E Q S	1	BC04Z, BC07D, or BC08R	
1-word parallel input interface	M1703		.555	E Q S	1	BC04Z, BC07D, or BC08R	
2-word parallel output interface	M1705		1.15	E Q S	1	BC04Z, BC07D, or BC08R	
Interface foundation module	M1709		.830+	E Q S	1	BC04Z, BC07D, or BC08R	Can accept user ICs with up to 40 pins
Wire-wrappable module, no sockets	W966		—	E Q S	—	BC04Z, BC07D, or BC08R	Can accept up to 42 14- or 16-pin user ICs
Wire-wrappable module, with sockets	W967		—	E Q S	—		

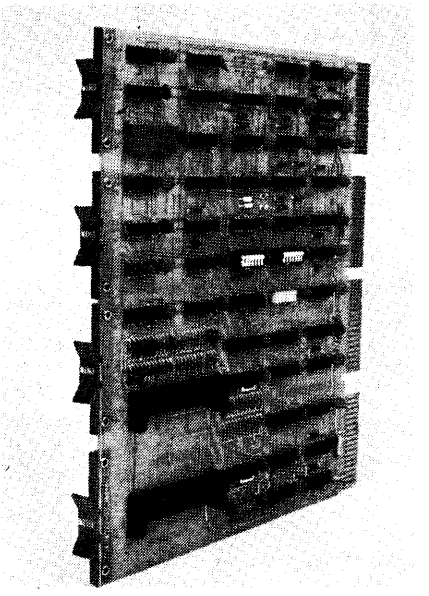
NOTES:
1. + means current required by user logic must be added to figure shown.
2. Module sizes are given as Length, Height, and Width, as defined in General Information.

DR8-ED
2-WORD INPUT INTERFACE

PDP-8/A, 8/E, 8/F or 8/M OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



DESCRIPTION

The DR8-ED is a complete, general purpose input interface used to transfer two independent 12-bit, parallel data words from a user's peripheral device to a PDP-8 computer system as shown on Figure 1. It is directly compatible with the OMNIBUS of a PDP-8/A, 8/E, 8/F, or 8/M and is designed for installation in any available OMNIBUS slot except 1, 2, and 3 of a PDP-8/A.

The DR8-ED consists of a device selector and IOT decoder logic, interrupt request and skip control, and two 12-bit Data Buffer Registers (DBRs)—one for each data word, and two independent Control and Status Registers (CSRs). One CSR is assigned to each input data word and provides status and control information during word transfers.

Two control and two status lines between the user's device and the module permit the establishment of a handshake routine to efficiently control the data transfers.

All input data, status and control signals from the user's device are diode protected for TTL operation. The Data Buffer Registers provide input latching capability for the 12 data lines from each device.

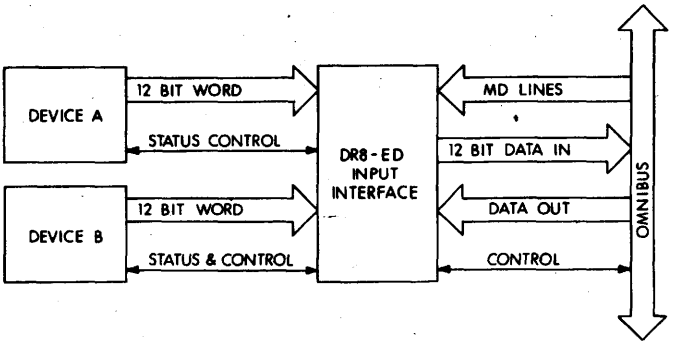


Figure 1 DR8-ED Interface

Two independent device select circuits are included on the module, one associated with each device. Each circuit contains six Dual In-Line Package (DIP) switches to allow the selection of a device address from the full complement of OMNIBUS device addresses. These switches facilitate the installation of the module by eliminating the need to solder or remove jumper leads for device address selection.

The DR8-ED is designed for user application and requires a minimum of external hardware to implement into a PDP-8 system. Two 40-pin connectors are conveniently mounted near the edge of the board to permit either one or two devices to be easily connected using BC08R or BC04Z flat cable assemblies available from DIGITAL. These cables have mating connectors premounted and can be supplied in any required length.

The interface module occupies one slot in the OMNIBUS or expander and is quad-height, extended-length, single-width board.

FUNCTIONS

The main elements of the DR8-ED input interface and the data control and status signal flow are shown on the block diagram. The module provides the complete interface logic necessary for the efficient transfer of data from a user's device to the PDP-8 OMNIBUS.

DATA BUFFER REGISTERS

Each of the two DBRs latch 12 bits of data from a user's device when the Data Ready signal is generated. The data is also latched into the DBR by the IOT command from the PDP-8 that reads in the data word. Input data is not required to be held by the device for the entire transfer operation, thereby permitting faster data transfers.

CONTROL STATUS REGISTERS

Each CSR is a 12-bit register used to supply control and status information to the user's device and to provide control and status indicators of the user's device and interface to the processor. The CSR also includes input latching for four extra data bits to allow the DR8-ED to interface with devices of up to 16 bits without the need of external multiplexing.

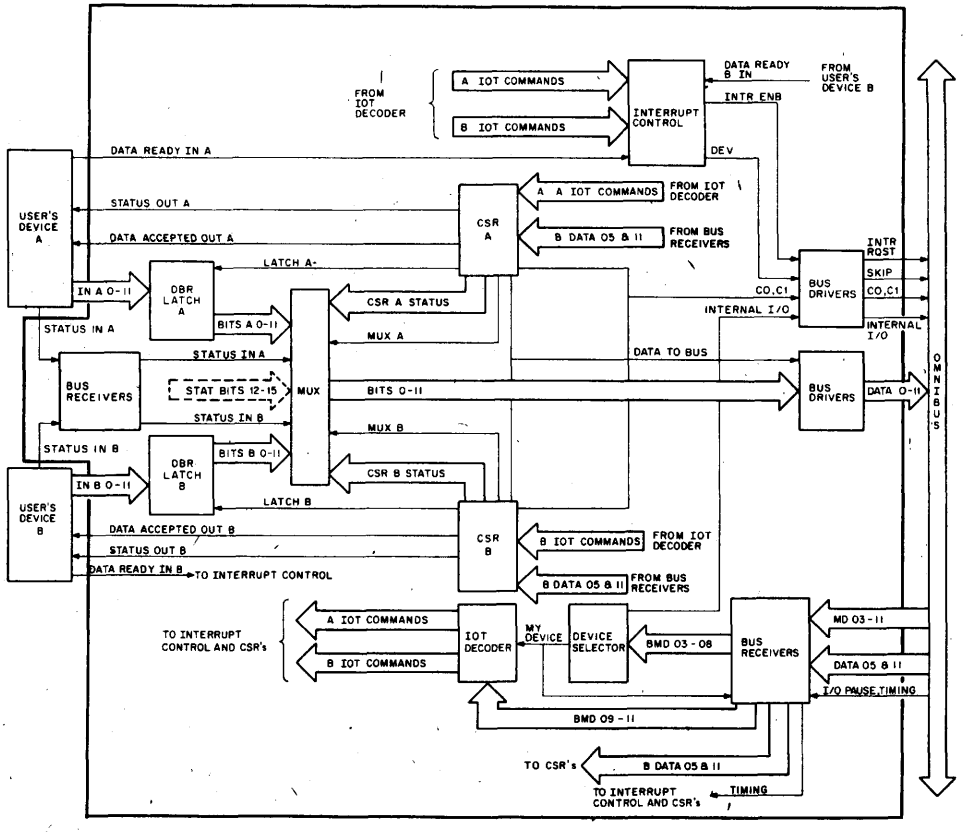


Figure 2 DR8-ED Functional Block Diagram

DATA/CSR MULTIPLEXER
The Data/CSR multiplexer is controlled by the commands from the IOT decoder to select either 12 bits of data from a DBR or 12 bits of status and control information from a CSR. When addressed by the processor or when an interrupt request is asserted, the selected output of the multiplexer is transferred to the processor through the bus drivers.

INTERRUPT CONTROL/SKIP LOGIC
The interrupt control logic produces an interrupt request to inform the processor that information is ready for transfer. The interrupt request signal is generated by the Data Ready signal when the user's device has data for transfer. The status of the Skip Flag is sampled by the processor during the interrupt routine to identify the interrupting device.

IOT DECODER
The IOT decoder logic produces eight IOT commands associated with each device address. Device A or B is selected by the decoded output of the device selector, and the function to be performed is determined by the three Buffered Memory Data bits (BMD) from the bus receivers. The following list describes the functions available for each device.

IOT	FUNCTION
0	Conditionally controls the Status Out signal depending on the state of data bit 05.
1	Sets the Interrupt Enable flag.
2	Resets the Interrupt Enable flag.
3	Transfers the status word to the PDP-8 accumulator.
4	Conditionally controls the Data Accepted Enable signal depending on the state of data bit 11.
5	Clears all flags .(Sets the Data Accepted Enable Flag.)
6	Transfers the device word to the PDP-8.
7	Tests the status of the DR-8ED Interrupt Request (SKIP IOT).

SWITCHABLE DEVICE SELECTION
The DR8-ED module contains two DIP switch banks used to conveniently select a device address for each 12-bit word. Six of the seven rocker switches on each bank provide the capability of selecting a unique address of 00_8-77_8 by setting the switches to a specified configuration. The remaining switch in each bank controls the setting of the interrupt request flag associated with each device. The interrupt request flags are set by either the leading or trailind edge of the Data Ready signal as determined by the switch position.

INTERFACE SIGNALS
OMNIBUS Signals—The input and output data, status and control signals conform to OMNIBUS signal specifications described in the PDP-8/E, PDP-8/M, and PDP-8/F Small Computer Handbook published by Digital Equipment Corporation. The DR8-ED module presents no more than one bus driver and/or receiver on any OMNIBUS signal line.
DEVICE SIGNALS—Data and Control Signals are transferred between devices and interface by two cables that attach to connectors J1 and J2. The location of the connectors is shown on Figure 3. Table 1 lists the pin assignments of each connector and signal loading and driving capability.

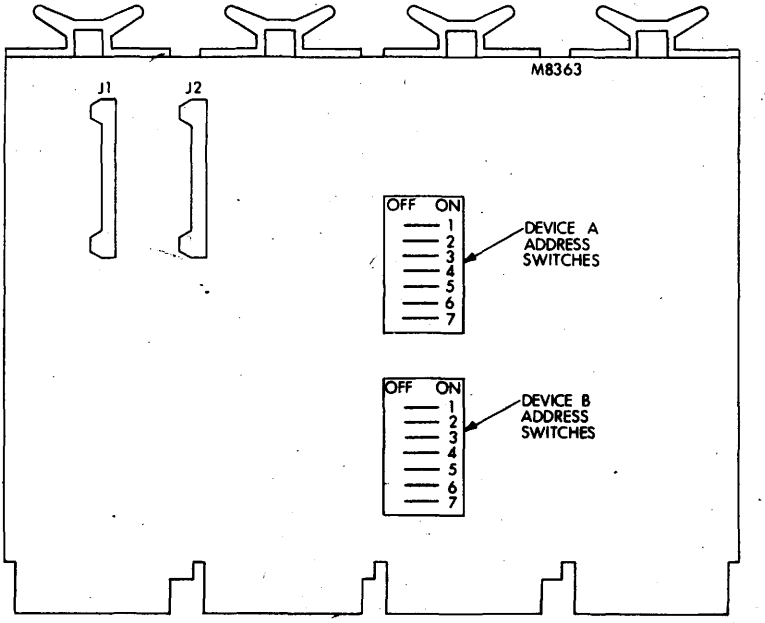


Figure 3 DR8-ED Connector and Switch Locations

Table I

*J1 and J2 Connector Pin	Signal Name	TTL Unit Load
B	STAT 15 H	4 (each)
D	STAT 14 H	
F	STAT 13 H	
J	STAT 12 H	
L	IN 0 H	2 (each)
N	IN 1 H	
R	IN 2 H	
T	IN 3 H	
Z	IN 4 H	
BB	IN 5 H	
DD	IN 6 H	
FF	IN 7 H	
JJ	IN 8 H	
LL	IN 9 H	
NN	IN 10 H	
RR	IN 11 H	
V	STATUS OUT L	20 (driving)
X	STATUS IN L	5
TT	DATA ACCEPTED OUT L	20 (driving)
VV	DATA READY IN L	5

*Remaining pins on J1 and J2 connect to logic GND on DR8-ED.

Four TTL-compatible signal lines connect between the interface module and each external device and can be used to establish a handshake routine for efficient control of the data transfers. Two lines from the CSR provide a Data Accepted handshake signal and a user defined status output bit to the user's device. A single line to the interrupt control logic produces an interrupt request when data is ready for transfer, and a status line to the Data/CSR multiplexer from the user's device provides user-defined status information for transfer to the OMNIBUS.

CABLE ASSEMBLY TYPES—Several device cable assemblies are available from DIGITAL for use with the DR8-ED. Table 2 lists some of the recommended cable types and the lengths available.

Table 2 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft)
BC07D-XX	H856 to open end	Two 20-conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

GENERAL SPECIFICATIONS

Input Data Configuration: Two parallel 12-bit data lines from a device

OMNIBUS Signals: Presents a maximum of one bus driver and/or one bus receiver on an OMNIBUS line.

Operating Temperature: 5°C (41°F) to 50°C (122°F)

Relative Humidity: 10% to 90%, without condensation

Size: Quad height—10.5 in. (26.67 cm); single width—0.5 in. (1.27 cm); extended length—8.5 in. (21.59 cm)

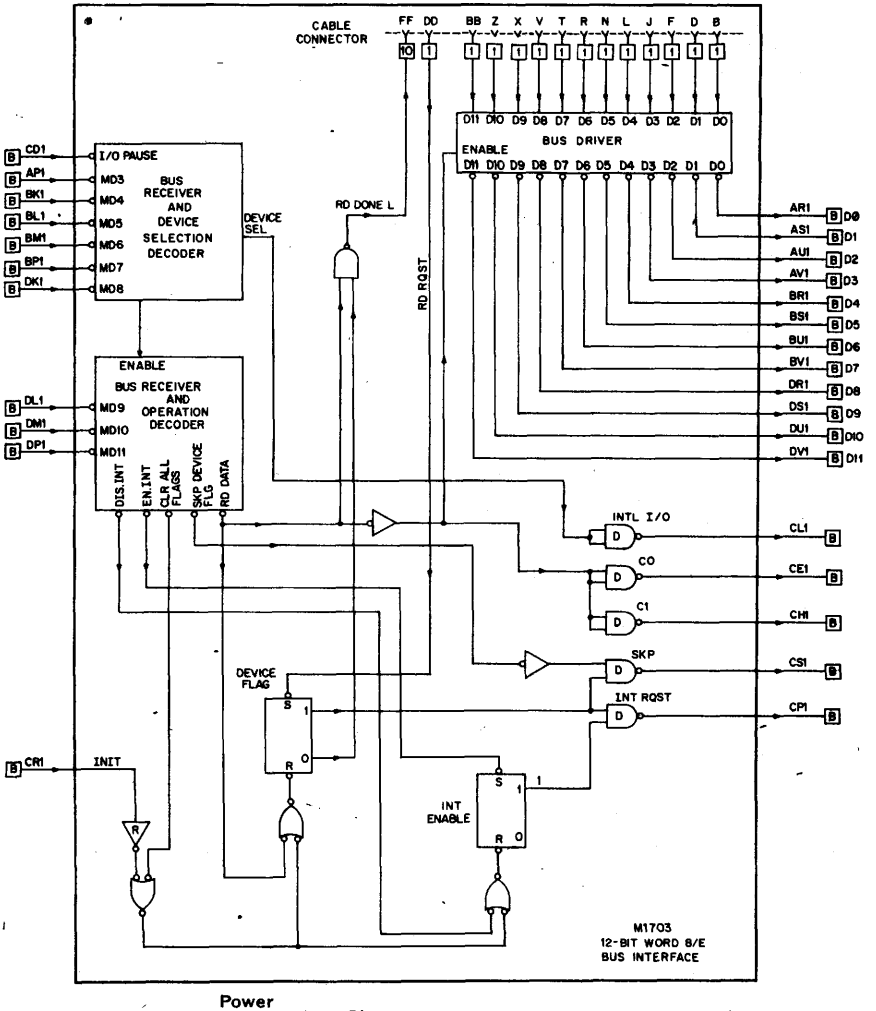
Power: +5V +5% at 1.5 A nominal

M1703
OMNIBUS INPUT INTERFACE

PDP-8/E, 8/M OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



Volts	Power mA (max.)	Pins
+5	555	AA2, BA2, CA2
GND		AC2, BC1, BC2, CC1, CC2, DC1, DC2
		AN1, AN2, BN1, BN2, CN1, CN2, DN1, DN2
		AT1, AT2, BT1, BT2, CT1, CT2, DT1, DT2
		AF1, AF2, BF1, BF2, CF1, CF2, DF1, DF2

DESCRIPTION

The M1703 provides, on a single quad-height module, a complete, self-contained interface that will input 12 bits of parallel TTL-level data to the PDP-8/A, 8/F, 8/E or 8/M OMNIBUS, under interrupt or programmed I/O control. The M1703 plugs directly into the OMNIBUS connector assembly, and the external device plugs into a 40-pin flat cable connector on the module itself. The module includes a device selector, an operation decoder, flags, and all control logic needed to request interrupt and respond to programmed I/O commands on the OMNIBUS. Command codes assigned to this module include:

ENABLE AND DISABLE INTERRUPT
CLEAR FLAGS
SKIP IF DEVICE FLAG SET
READ DATA

A device selection code of 14 (octal) is assigned to this module but the code can be changed by moving wire jumpers.

FUNCTIONS

Device Selection Decoder: The device is addressed through this decoder when I/O PAUSE is asserted and the octal device code for the decoder is received through <MD03:08>. The decoder output asserts the INT. I/O line and enables the operation decoder.

Operation Decoder: The select bits (MD09, 10 and 11) determine the type of operation to be performed when the operation decoder is enabled by the device selection decoder.

DATA <00:11>: Data from the external device is applied to the bus drivers on these lines. A READ DATA command enables the bus drivers and asserts C0 and C1, thereby entering the data into AC0-11 via corresponding OMNIBUS data lines.

READ RQST: When the external device is ready to input stable data, it applies a logic LOW for at least 50 ns on this control line, to set the DEVICE FLAG. READ DONE goes HIGH within 60 ns after READ RSQT goes LOW.

DEVICE FLAG: After being set by a LOW on the RD RQST line, this flag initiates an interrupt request (if INTERRUPT is enabled). This flag is sensed by the SKIP control line.

INTERRUPT RQST: When this line is asserted by the DEVICE FLAG, an interrupt request is sent to the computer which responds by executing a JMS0 instruction.

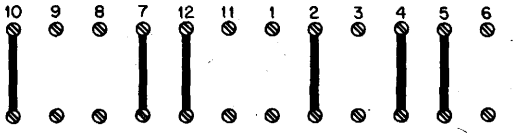
INTERRUPT ENABLE: This flip-flop is set to enable and cleared to disable the interrupt request function.

SKIP Control Line: If the device flag is set, the instruction SKIP ON DEVICE FLAG asserts the SKIP line, incrementing the contents of the computer's program counter.

READ DONE: This line stays HIGH as long as the DEVICE FLAG is set, and signals the end of a data transfer by going LOW after the end of a RD DATA pulse.

Changing the Device Code: The device selection decoder is preset for a device code of 14 octal. However, split lugs on this module permit the code to be changed by the user to any octal number from 00 to 77. To obtain the

desired octal number, jumper the split lug pairs that select the binary equivalent of the device code, as shown below:



A. PHYSICAL LAYOUT OF SPLIT LUGS
(SHOWING JUMPERS FOR DEVICE CODE 14 OCTAL)

ADD JUMPER AT:	DEVICE CODE					
	8^1			8^0		
	2^2	2^1	2^0	2^2	2^1	2^0
BIT = 1	1	3	5	7	9	11
BIT = 0	2	4	6	8	10	12

EXAMPLE

0	0	1	1	0	0	BINARY EQUIV. OF 14 OCTAL CODE
2	4	5	7	10	12	REQUIRED JUMPERS

B. DETERMINING JUMPERS FOR NEW CODE ASSIGNMENTS

IOT INSTRUCTION ASSIGNMENTS

Octal Code	Instruction	Purpose
6140	Disable Interrupt	Clears the INTERRUPT ENABLE flag to disable the INT RQST line
6141	Enable Interrupt	Sets the INTERRUPT ENABLE flag to enable the INT RQST line
6142	Clear Flags	Clears the DEVICE FLAG, asserts READ DONE and clears INTERRUPT ENABLE flag
6143	Skip-if Device Flag Set	Asserts the SKIP line if the DEVICE FLAG is set. The computer responds by incrementing the program counter so that the next instruction is skipped.
6144	Read Data	Transfers input data bits <00:11> to <AC00:11> through the OMNIBUS data lines. Also clears the DEVICE FLAG, allowing the RD DONE output to go LOW when the data transfer is complete.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
LOW on RD RQST input	RD DONE going HIGH	60

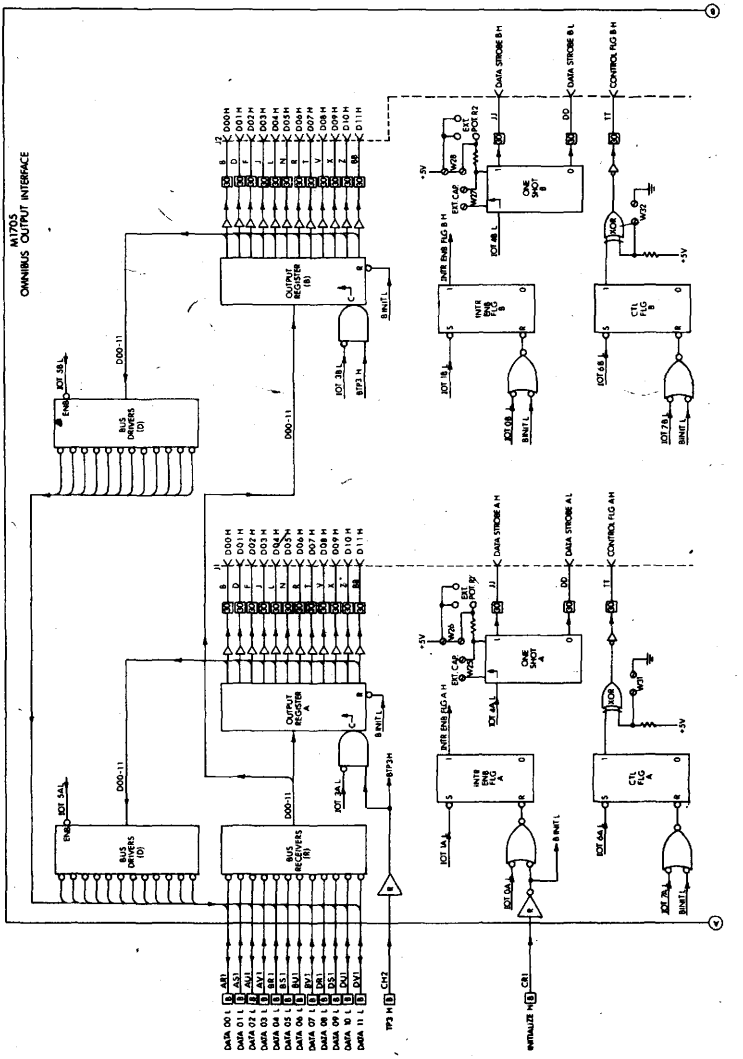
M1705
OMNIBUS OUTPUT INTERFACE

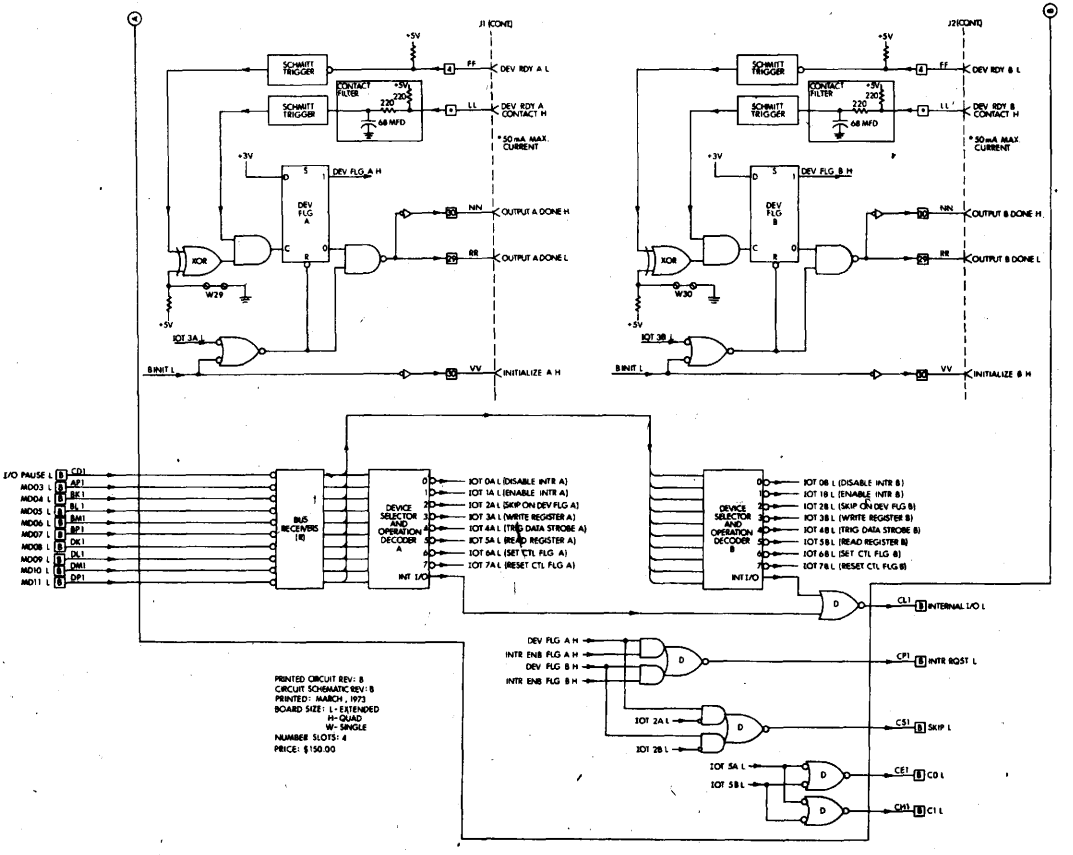
OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Volts	Power mA (max.)	Pins
+5	1.15A	AA2, BA2, CA2
GND		All pins F, T, N, AC2, BC1, BC2, CC1, CC2, DC1, DC2




J1 (CONT)
J2 (CONT)
SCHMITT TRIGGER
CONTACT FILTER
+5V
220
68 MFD
DEV RDY A L
DEV RDY A CONTACT H
DEV RDY B L
DEV RDY B CONTACT H
* 50 mA MAX CURRENT
+3V
DEV FLG A H
DEV FLG B H
DEV FLG A
DEV FLG B
XOR
W29
W30
OUTPUT A DONE H
OUTPUT A DONE L
OUTPUT B DONE H
OUTPUT B DONE L
IOT 3A L
IOT 3B L
B INIT L
INITIALIZE A H
INITIALIZE B H
I/O PAUSE L
MD03 L
MD04 L
MD05 L
MD06 L
MD07 L
MD08 L
MD09 L
MD10 L
MD11 L
BUS RECEIVERS (R)
DEVICE SELECTOR AND OPERATION DECODER A
DEVICE SELECTOR AND OPERATION DECODER B
INT I/O
IOT 0A L (DISABLE INTR A)
IOT 1A L (ENABLE INTR A)
IOT 2A L (SKIP ON DEV FLG A)
IOT 3A L (WRITE REGISTER A)
IOT 4A L (TRIG DATA STROBE A)
IOT 5A L (READ REGISTER A)
IOT 6A L (SET CTL FLG A)
IOT 7A L (RESET CTL FLG A)
IOT 0B L (DISABLE INTR B)
IOT 1B L (ENABLE INTR B)
IOT 2B L (SKIP ON DEV FLG B)
IOT 3B L (WRITE REGISTER B)
IOT 4B L (TRIG DATA STROBE B)
IOT 5B L (READ REGISTER B)
IOT 6B L (SET CTL FLG B)
IOT 7B L (RESET CTL FLG B)
INTERNAL I/O L
INTR RQST L
SKIP L
C0 L
C1 L
PRINTED CIRCUIT REV: B
CIRCUIT SCHEMATIC REV: B
PRINTED: MARCH, 1973
BOARD SIZE: L - EXTENDED
H - QUAD
W - SINGLE
NUMBER SLOTS: 4
PRICE: $150.00

DESCRIPTION

The M1705 is an output interface module that allows the PDP-8 computer to transfer data to, and control the operation of, remotely programmable instruments or similar digital devices. The function is to perform parallel transfers, under program or interrupt control, of 12-bit data words from the computer to peripheral devices.

The M1705 consists of duplicate logic sections. Each section includes device selection logic to address an external device, an operations decoder to determine the type of interface operation, a 12-bit storage register to buffer the output data, interrupt control logic, and bus drivers/receivers to allow operation on the OMNIBUS. Connection to the device(s) is made via standard cables that plug into a pair of connectors on the M1705 module board.

FEATURES

- Complete single-card OMNIBUS output interface
- Data storage registers
- Program interrupt capability
- Cable drivers on all output signals, diode-protected
- Compatible with M1703 OMNIBUS Input Interface
- TTL-compatible signals
- Diode-protection/pulse-shaping on all input signals
- Peripheral I/O cables plug directly onto M1705 card
- Variable pulse width control signals
- User-assigned device codes—jumper selected
- Many user-selected control functions—assertion levels, both TTL and contact closures.

APPLICATIONS

The M1705 OMNIBUS Output Interface is suitable for a variety of scientific and industrial applications which require parallel TTL-compatible data to be output from a PDP-8/E family computer. Its dual word (24-bit) digital output and data storage capability make it a natural for the remote programming of instruments such as digital voltmeters (DVMs), digital multimeters (DMMs), RLC bridges, programmable power supplies and many more.

The M1705 finds application in the scientific and industrial laboratory as a general-purpose digital (TTL) output interface. The control of experimental equipment and the driving of strip chart recorders are only two of the many possible laboratory uses.

Its cable-driving capabilities make the M1705 a fine choice for interprocessor communication. When used with the M1703 OMNIBUS Input Interface, the M1705 provides the capability of communicating at high speed with one or more PDP-8/E family computers. Additionally, the M1703 Input and M1705 Output Interfaces may be combined at one computer to form a general-purpose digital input/output interface system. The result is a very flexible, low-cost system that may be readily expanded. This type of system is often required for the control of, and collection of data from, programmable instruments, production line machinery, lab experiments, and custom peripheral devices (X-Y recorders, card readers, mag tape drivers, etc.).

FUNCTIONS

Device Selection Decoder (A, B)
External devices are addressed through one of two identical Device Selection Decoders. This allows external devices to be handled separately if desired. Each decoder is activated when I/O PAUSE is asserted by the processor and the octal device code for that decoder is received through bits MD03-MD08. Decoders A and B are factory-assigned octal device codes 15 and 16 respectively. However, any octal code from 01 to 77 is selectable by the user via split lug jumpers. The decoder output asserts the INTERNAL I/O line and enables an operation decoder.

Operation Decoder (A, B)
The Operation Decoder decodes the three operation bits MD09-MD11 from the OMNIBUS to determine the type of operation to be performed. The appropriate operation decoder (A or B) is enabled by its respective Device Selection Decoder (A or B).

Output Register (A, B)
The data from the processor accumulator (AC) is transferred to one of the two output registers (A or B) via OMNIBUS lines DATA-00-DATA-11. A binary 1 in the accumulator corresponds to a binary 1 in the output register and to a logic HIGH at the register's output. The register output (D00-D11) may be transferred, in parallel, to the device by a Data Strobe pulse. All bits of both output registers are reset to a logic LOW by assertion of the OMNIBUS signal INITIALIZE.

Device Flag (A, B)
This is a flip-flop which is set by the external device signal DEV RDY or DEV RDY CONTACT and reset by the INITIALIZE signal from the processor or by the appropriate IOT 3 (WRITE REGISTER) command). The status of the Device Flag can be interrogated by the IOT 2 (SKP ON DEV FLG) command. Setting this flip-flop initiates the interrupt request if the Interrupt Enable Flag flip-flop is set.

Interrupt Enable Flag (A, B)
This is a flip-flop which is set under program control to enable or disable the interrupt request function on the M1705 module.

Control Flag (A, B)
This is a spare flip-flop which may be used to perform any additional control function at the external device.

I/O Bus Drivers and Receivers
The OMNIBUS receivers and drivers contain special high-impedance circuitry to minimize bus loading.

PROGRAMMING

The following is a list of instructions that are available for use by the programmer.

Octal Code*	Name	Function
6150	Disable Interrupt A	Resets INTR ENB FLG A to disable the Interrupt Request function for Section A.
6151	Enable Interrupt A	Sets the INTR ENB FLG A to enable the Interrupt Request function for Section A.
6152	Skip on Device Flag A	Asserts the SKIP line if DEV FLG A is set.
6153	Write Register A	Clocks the contents of AC00-AC11 into Output Register A. Also, OUTPUT A DONE H becomes a logic HIGH and OUTPUT A DONE L becomes a logic LOW following completion of this instruction.
6154	Trigger Data Strobe A	The trailing edge of the pulse generated by this IOT initiates DATA STROBE A H and DATA STROBE A L pulses.
6155	Read Register A	Transfers the contents of Output Register A to AC00-AC11.
6156	Set Control Flag A	Sets the CTL FLG A flip-flop.
6157	Reset Control Flag A	Resets the CTL FLG A flip-flop.
6160	Disable Interrupt B	Resets INTR ENB FLG B to disable the Interrupt Request function for Section B.
6161	Enable Interrupt B	Sets the INTR ENB FLG B to enable the Interrupt Request function for Section B.
6162	Skip on Device Flag B	Asserts the SKIP line if DEV FLG B is set.
6163	Write Register B	Clocks the contents of AC00-AC11 into Output Register B. Also, OUTPUT B DONE H becomes a logic HIGH and OUTPUT B DONE L becomes a LOW following completion of this instruction.
6164	Trigger Data Strobe B	The trailing edge of the pulse generated by this IOT initiates DATA STROBE B H and DATA STROBE B L pulses.
6165	Read Register B	Transfers the content of Output Register B to AC00-AC11.
6166	Set Control Flag B	Sets the CTL FLG B flip-flop.
6167	Reset Control Flag B	Resets the CTL FLG B flip-Flop.

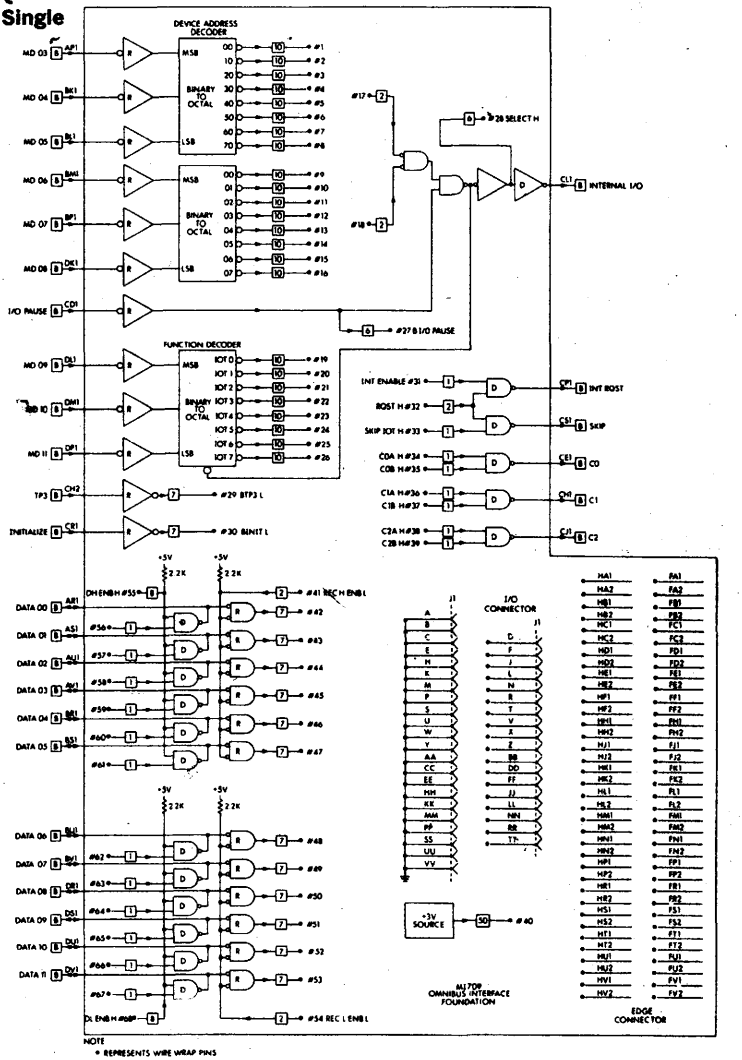
*Device codes 15_8 and 16_8 are factory-selected. Other codes may be chosen by changing jumpers on the M1705 module.

M1709
OMNIBUS INTERFACE FOUNDATION MODULE

OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



Volts	Power mA (max.)	Pins
+5	830	AA2, BA2, CA2
GND		All pins C, N, F, and T

DESCRIPTION

The M1709 OMNIBUS Interface Foundation module is a generalized OMNIBUS Interface card that is constructed to allow the user to build a custom design using integrated circuits (ICs). All required OMNIBUS interface logic, i.e., bus drivers/receivers, device selectors, and interrupt/skip circuitry is provided. IC mounting pads with wire wrappable pins are made available for custom circuitry. Pads accommodate all common types of Dual-In-Line Pack (DIP) ICs with up to forty pins.

Connection to user-equipment is made via standard cables (BC08R or BC04Z) that plug directly into the M1709 module board. The module cable connector allows several M1709 modules or W966/W967 wire wrappable modules to be strapped together to accommodate more extensive designs.

APPLICATIONS

Since both analog and digital circuitry are available in DIP form, quite complex systems may be built. Some of the typical applications for the M1709 module are:

- Multiword input and/or output
- Instrument interfaces
- Interprocessor communication
- Oscilloscope controller (D/A)
- Peripheral control (data terminals, etc.)
- Interfacing of:
  - A/D converters
  - Multiplexers
  - Counters
  - Shift registers
  - Read-Only Memories (ROMs)
  - Arithmetic Logic Units (ALU)

FUNCTIONS

The preassembled circuitry of the M1709 module can be classified into four categories: Device and Function Selection, Data Bus Interface, Interrupt and Skip Interface, and Control Line Interface.

Device and Function Selection: Device address decoding is performed with a pair of binary-to-octal decoders (3 to 8 line). OMNIBUS lines MD03 through MD08 are decoded and one output of each decoder is ANDed (by wire wrapping) to sense a "device selected" condition. Any code from 01_8 to 77_8 is selectable via wire wrap jumper selection.

The "device selected" condition is, in turn, ANDed with the I/O PAUSE signal to drive the OMNIBUS signal INTERNAL I/O. This signal is also made available at a wire wrap pin as SELECT H.

Function decoding is performed by a binary-to-octal decoder (3 to 8 line). OMNIBUS signals MD09 through MD11 are decoded to form the eight IOT 0 through IOT 7 signals. These TTL signals are made available at numbered wire wrap pins for ease of connection to user-installed IC logic.

Data Bus Interface: The 12 OMNIBUS Data Lines, DATA 00 through DATA 11, are received with special high-impedance circuitry and TTL signals are made available at wire wrap pins. In addition, each data line has a special BUS driver circuit assigned to it. Input to these drivers is available at wire wrap pins and is TTL-compatible for direct connection to user-installed IC logic.

Enabling inputs are provided for both data line receivers and drivers.

Interrupt and Skip Interface: BUS driver circuits are available for driving the OMNIBUS INT RQST and SKIP lines. The INT RQST driver has an enabling input which can be used to inhibit the interrupt request while maintaining the ability to test the interrupt condition via the SKIP facility. Input to these drivers is TTL-compatible and made via wire wrap pins.

Control Line Interface: BUS driver circuits are connected for asserting the three OMNIBUS data transfer mode signal lines—C_0, C_1, C_2. Input to these drivers is TTL-compatible and made via wire wrap pins.

Miscellaneous Interface Signals: OMNIBUS signals TP3 and INITIALIZE are received with high impedance circuits. These signals are made available in TTL-compatible form at wire wrap pins as BTP3 and BINIT, respectively. A source of +3 volts is made available at a wire wrap pin.

OMNIBUS Signals made Available to the User*
In addition to those OMNIBUS signals mentioned previously, the following 40 OMNIBUS signals are made available to the user at wire wrap pins. The complete set of signals available is sufficient to allow the user to accomplish all program transfer **and** data break interface operations.

OMNIBUS Signal Name	Pin
MA0	AD1
MA1	AE1
MA2	AH1
MA3	AJ1
MD0	AK1
MD1	AL1
MD	AM1
MD DIR	AK2
MA4	BD1
MA5	BE1
MA6	BH1
MA7	BJ1
MD6	BM1
MD7	BP1
INT STROBE	BD2
BRK IN PROG	BE2
MA, MS LOAD CONT	BH2
OVERFLOW	BJ2
BREAK DATA CONT	BK2
BREAK CYCLE	BL2
BUS STROBE	CK1

* These OMNIBUS signals (except ± 15 V) require high impedance/low leakage current driving and receiving circuitry. (Use DEC 8640 and 8881 ICs).

OMNIBUS Signal Name	Pin
NOT LAST XFER	CM1
CPMA DISABLE	CU1
MS, IR DISABLE	CV1
TP1	CD2
TP2	CE2
TP3	CH2
TP4	CJ2
TS1	CK2
TS2	CL2
TS3	CM2
TS4	CP2
LINK DATA	CR2
LINK LOAD	CS2
MA8	DD1
MA9	DE1
MA10	DH1
MA11	DJ1
+15 V	DA2
−15 V	DB2

SPECIFICATIONS

Signals to and from the OMNIBUS are received or driven with special high impedance circuitry to minimize bus loading.

CAUTION

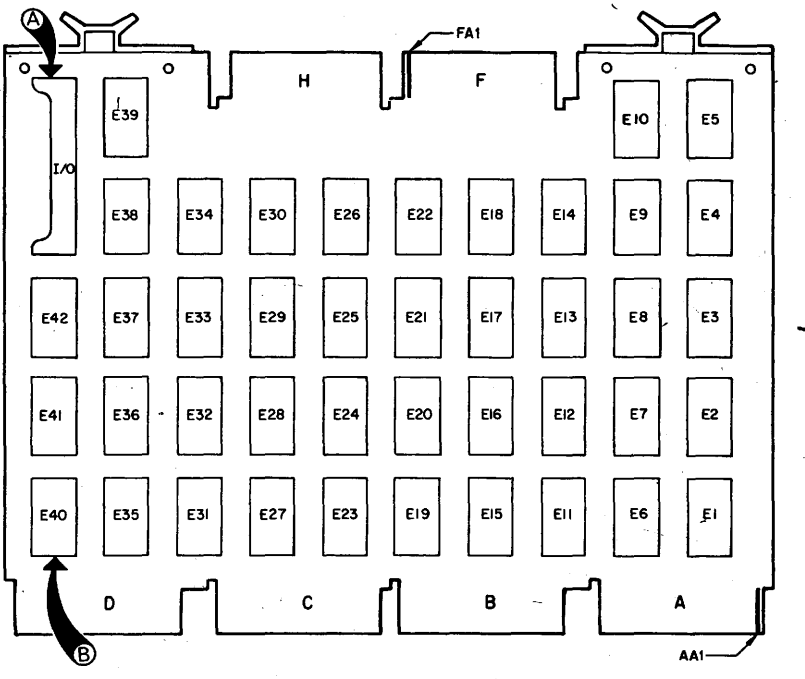
All requirements for timing should be in accordance with the PDP-8/e and -8/m Small Computer Handbook and the PDP-8/A Miniprocessor Handbook.

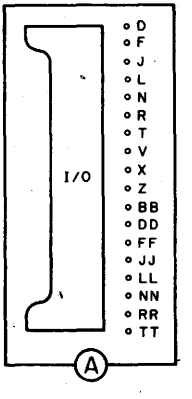
W966
WIRE WRAPPABLE MODULE

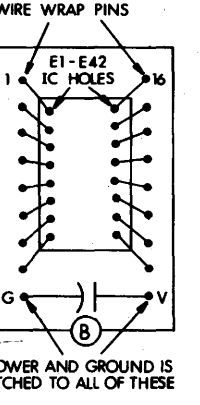
OMNIBUS

W SERIES

Length: Extended
Height: Quad
Width: Single







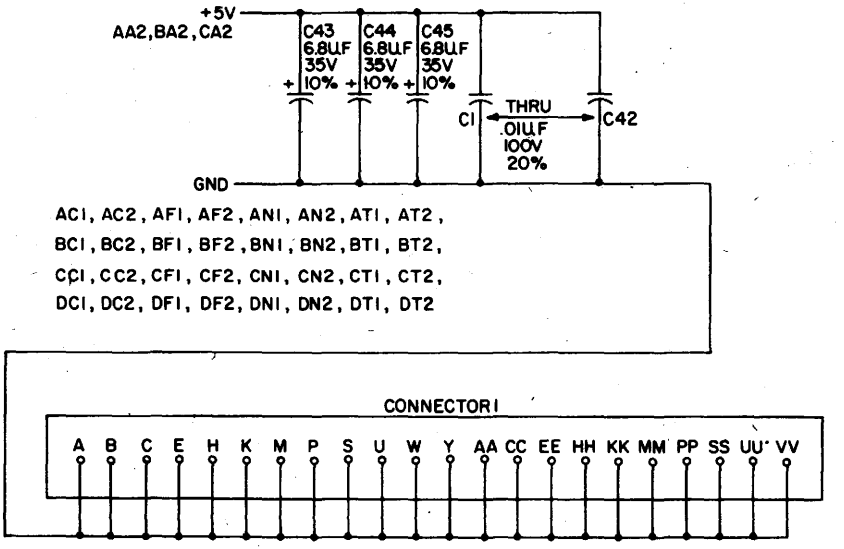
W966 Wire Wrappable Module

DESCRIPTION

The W966 Wire Wrappable Module is a PDP-8/A, 8/E, 8/M general-purpose module that provides for the construction of custom interface designs using integrated circuits (ICs) and wire wrapped interconnections. Up to 42 of 14- and/or 16-pin ICs can be easily mounted (with or without 16-pin sockets) onto the etched IC pads. (Sockets are not supplied.) Each wire wrap pin can accommodate two separate leads of 30-gauge wire. Discrete components may also be directly soldered onto the IC pads. Position E39 features a pad that can be used for mounting a potentiometer.

The W966 has 72 etched contact fingers at the handle end, with a wire wrap pin connected to each finger. When a W966 is located adjacent to another W966, signals can be bused from one module to the other via these contact fingers by using an H851 edge connector. One H851 can bus 36 signals; therefore, two H851s are required to bus all 72 signals. In addition, the standard 144 contact fingers at the connector end of the module are also connected to wire wrap pins.

An H854 40-pin I/O connector (male) is contained on the module to provide access to the "outside world"; it can accept any cable equipped with an H856 connector. Eighteen of these connector pins are connected to wire wrap pins.



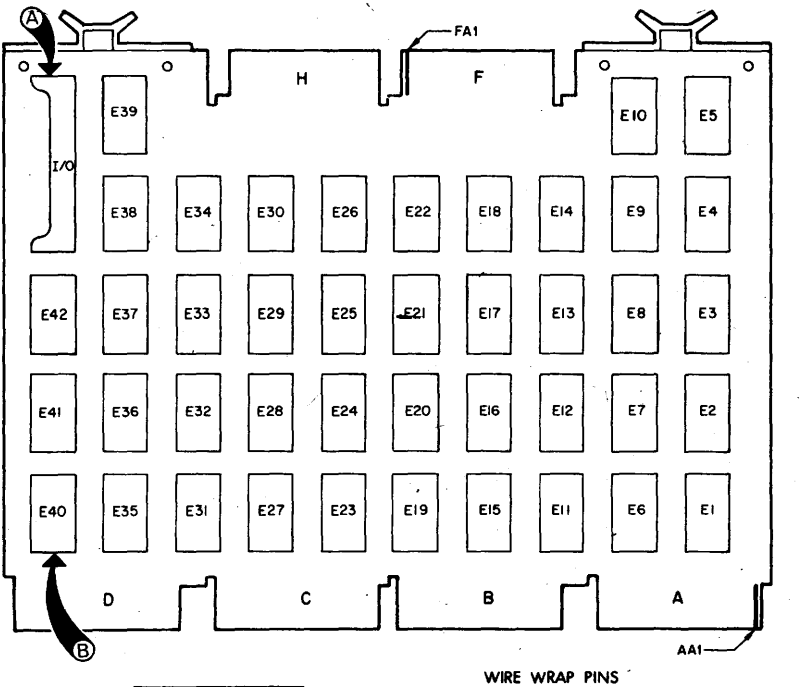
W966 Circuit Schematic

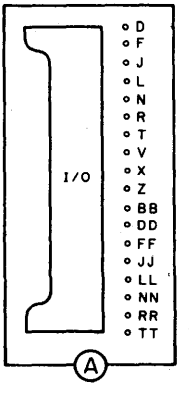
W967
WIRE WRAPPABLE MODULE

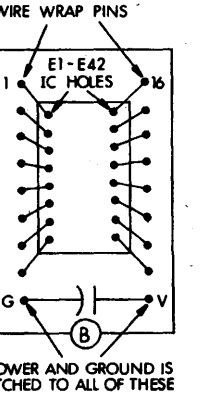
OMNIBUS

W SERIES

Length: Extended
Height: Quad
Width: Single







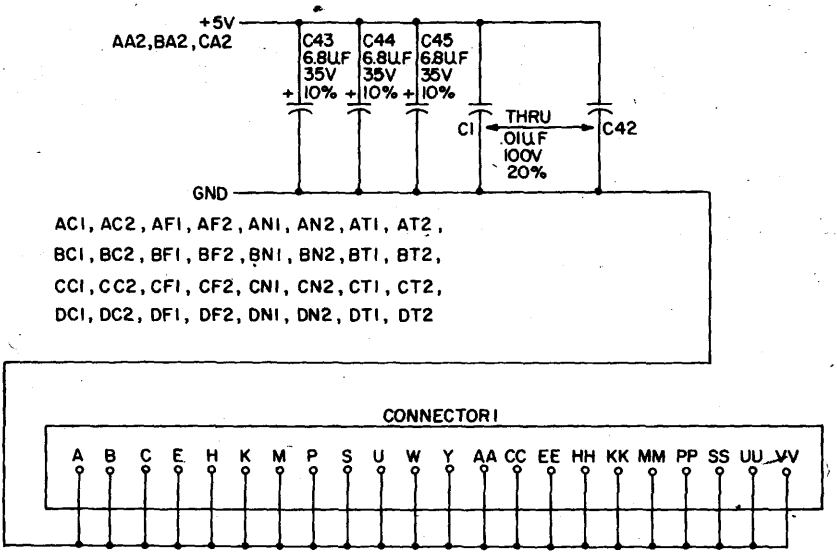
W967 Wire Wrappable Module

DESCRIPTION .

The W967 Wire Wrappable Module is a PDP-8/A, 8/E, 8/M general-purpose module that provides for the construction of custom interface designs using intergrated circuits (ICs). Featured on the board are 42 low-profile IC sockets which easily accommodate 14- and/or 16-pin ICs. Each wire wrap pin can accommodate two separate leads of 30-gauge wire. Discrete components may also be directly inserted into the sockets. Position E39 features a pad that can be used for mounting a potentiometer by removing the socket.

The W967 has 72 etched contact fingers at the handle end, with a wire wrap pin connected to each finger. When a W967 is located adjacent to another W967, signals can be bused from one module to the other via these contact fingers by using an H851 edge connector. One H851 can bus 36 signals; therefore, two H851s are required to bus all 72 signals. In addition, the standard 144 contact fingers at the connector end of the module are also connected to wire wrap pins.

An H854 40-pin I/O connector (male) is contained on the module to provide access to the "outside world"; it can accept any cable equipped with an H856 connector. Eighteen of these connector pins are connected to wire wrap pins.



W967 Circuit Schematic

PDP-11 INTERFACING

The PDP-11 family of computers are the most popular medium-sized systems in the industry. PDP-11s can be found in hundreds of applications, from real-time data acquisition and control to management information systems. All models of the PDP-11 family share one common feature: all signals between the processor, memory, and peripherals are transferred via the UNIBUS. This section is presented in two parts: (1) Basic UNIBUS Interfacing and (2) PDP-11 I/O Modules.

Basic UNIBUS Interfacing

The UNIBUS is a single, common path that connects the processor, memory, and peripherals. (See Figure 1.) Each register (data source or data destination) in each peripheral device is assigned an address to distinguish among the individual peripherals connected to the UNIBUS. This address is analogous to a memory location and permits instructions to act upon device registers as memory locations. There may be only one controlling device on the UNIBUS at any given time because of the system architectural configuration. This device is termed the Master and devices controlled by the Master are termed the Slaves. Devices may request Mastership by asserting either a Bus Request or a Non-processor Request to the Priority Arbitration Logic of the Processor. The request is honored if it is of a higher priority than any other request. The new Master assumes control of the bus when the current Master relinquishes Bus Mastership. The new Master may then request either to have the processor service the peripheral (BR only) or may initiate a data transfer without processor intervention (NPR or BR).

Interface Types

PDP-11 interfaces can be categorized into three distinct types:

1. Slave—This interface has no provision in its control logic to become Master. It will only transfer data onto and off the UNIBUS by command of a Master device.
2. Interrupt—This interface has the ability to gain Mastership of the bus (BR level) in order to give the Central Processor the address of a subroutine which the processor will use to service the peripheral.
3. DMA—This interface has the ability to gain Mastership of the Bus (NPR level) in order to transfer data between itself and some other peripheral.

A single interface may employ all three of the above types.

Signals on the UNIBUS that are used for programmed and interrupt I/O control are defined in Table 1. For complete information on UNIBUS interfacing, refer to the PDP-11 Peripheral Handbook.

Table 1. UNIBUS I/O Signal Summary

SIGNAL	DEFINITION
A <17:00>*	Address Lines. The 18 address lines are used by the master device to select the slave (a unique memory or device register address) with which it will communicate.
	Lines A <17:01> specify a unique 17-bit word and A00 specifies the byte being referenced.
	Peripheral devices are normally assigned an address from within the bus address allocations from 760000-777777 (program addresses, 160000-177777).

*Angle brackets enclose groups of lines; A <17:00> = A17 through A00 inclusive.

...GNAL	DEFINITION

D <15:00> Data Lines. The 16 data lines are used to transfer information between bus master and slave.

C <1:0> Control Lines. These two bus signals are coded by the master device to control the slave in one of four possible data transfer operations.

C1	C0	Operation
0	0	DATI—Data in
0	1	DATIP—Data In, Pause
1	0	DATO—Data Out
1	1	DATOB—Data Out, Byte

MSYN Master Synchronization. A control signal used by the master to indicate to the slave that address and control information is present.

SSYN Slave Synchronization. The slave's response to the master (response to MSYN).

PA, PB Parity Bit Low (PA) and Parity Bit High (PB). These signals are for devices on the UNIBUS that use parity checks. PB is the parity line for the high-order byte (on D <15:08>) and PA is the parity line for the low-order byte (D <07:00>).

PA and PB are generated by a slave and received by a master. They indicate parity error in a device. The slave negates PA and asserts PB to indicate a parity error on a DATI/P; PA and PB both negated indicates no parity error. PA asserted and PB asserted or negated are conditions reserved for future use. PA and PB are not defined in a DATO transaction. PA and PB may be used by the bus master's parity error logic.

The following table is a summary of the possible combinations of the parity error indicators.

PA	PB	
0	0	no error in a slave in DATI/P
0	1	error in slave in DATI/P
1	x	reserved

The protocol for PA and PB is the same as that for D<15:00>.

BR <7:4> Bus Request Lines. These four bus signals are used by peripheral devices to request control of the bus.

BG <7:4> Bus Grant Lines. These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.

SIGNAL	DEFINITION
NPR	Non-Processor Request. This signal is a bus request from a peripheral device to the processor, usually for a DMA transfer.
NPG	Non-Processor Grant. This signal is the processor's response to an NPR. It occurs at the end of a bus cycle.
SACK	Selection Acknowledge. SACK is asserted by a bus-requesting device that has received a bus grant. Bus control passes to this device when the current bus master completes its operation.
INTR	Interrupt. This signal is asserted by a peripheral device once it has become the bus master to start a program interrupt in the processor.
BBSY	Bus Busy. This signal is asserted by the master device to indicate bus is being used.
INIT	Initialization. This signal is asserted by the processor when power is first applied, when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. INIT may also be used to clear and initialize peripheral devices by means of the RESET instruction.
AC LO	AC Line Low. This signal starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss.
DC LO	DC Line Low. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply.

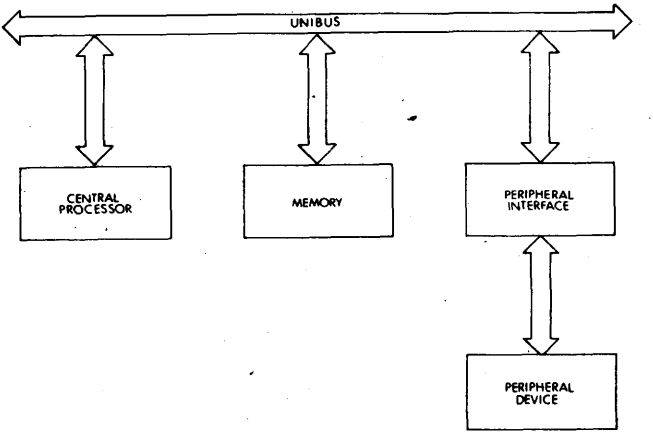


Figure 1. UNIBUS Connections

PDP-11 UNIBUS-RELATED INTERFACING MODULES

Table 2 summarizes the interfaces and related modules that are described in detail on the following pages or in the DIGITAL Direct Sales Catalog where noted.

Although each interfacing problem is likely to have some unique aspects, the steps to follow in general are:

1. Determine your interfacing requirements.
2. Match these requirements against the products listed in Table 2, then read the detailed descriptions.
3. Select suitable products if any are listed. If no listed products meet your requirements, contact your DIGITAL Field Sales office to find if any other DIGITAL products can perform the needed functions.
4. Add the power and mounting space requirements of all modules to be employed, and note the cables needed plus and prerequisites and restrictions that apply.
5. From the appropriate sections of this Handbook and the Hardware/Accessories Catalog, select the cables, power supplies, and mounting hardware to complete your system.

If you need technical assistance with any product in this Handbook, feel free to call DIGITAL's toll-free Hot Line, 8:30AM to 5:00PM Eastern time, 800-258-1710. From New Hampshire locations or places outside the United States, call Merrimack, 603-884-6660.

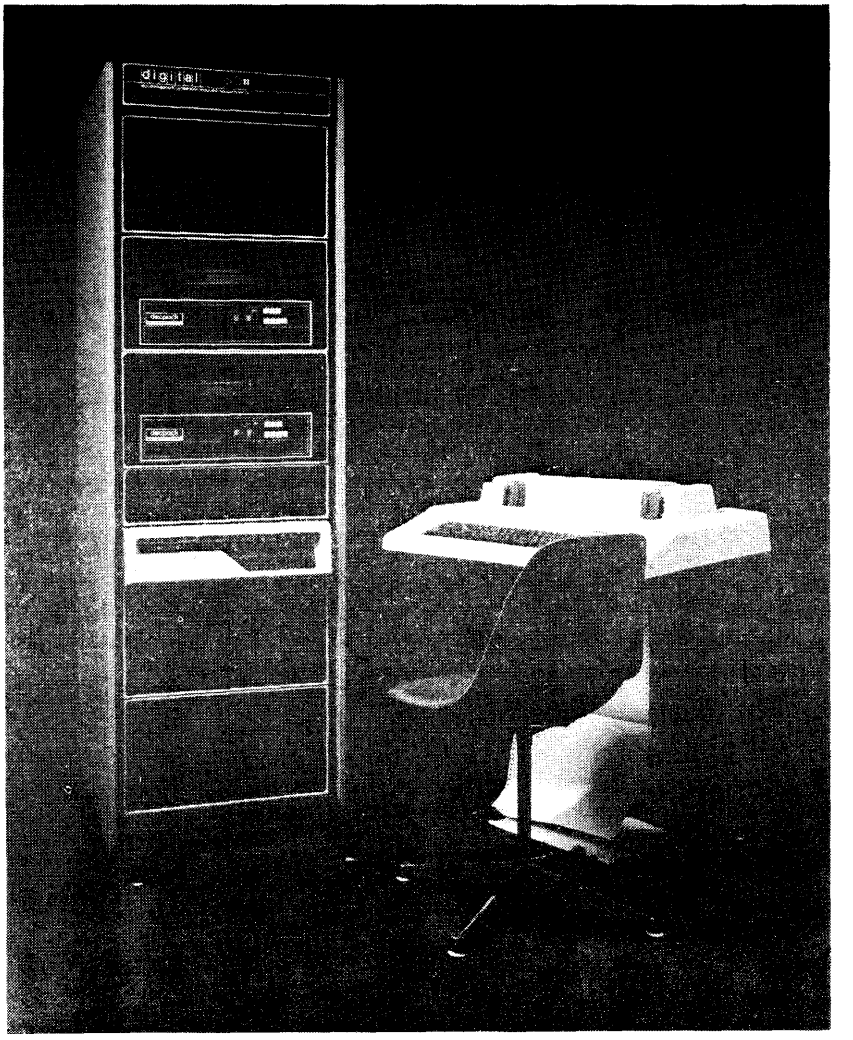
Table 2 Interface Selector Guide—PDP-11 UNIBUS

DEVICE OR FUNCTION	MODULE OR OPTION	LOGIC H'BOOK PAGE[2]	POWER +5V AMPS[1]	BUS LOADS	MODULE SIZE L H W[2]	CABLE REQ'D	FITS SPC SLOT?	COMMENTS
EIA RS232C serial devices, e.g.: LA35 printer LA36 printer terminal LA180 printer LS120 printer terminal VT52 CRT terminal VT55 CRT terminal	M7800		1.8	1	E Q S	BC05C-25	yes	Also requires −15V@.15A, +15V@.016A. One of four standard crystals must be specified at time of order. For complete option, see DL11-WB.
20 mA current loop serial devices, e.g.: LA35 printer LA36 printer terminal LA180 printer VT50 CRT terminal VT52 CRT terminal VT55 CRT terminal	M7800		1.8	1	E Q S	70-8360	yes	Also requires −15V@.15A, +15V@.016A. One of four standard crystals must be specified at time of order. For complete option, see DL11-WA.
General 20 mA serial asynchronous I/O interface	DL11-WA		2.0	1	E Q S	70-8360-1 supplied	yes	Also requires −15V@.15A, +15V@.05A. Crystal must be specified at time of order.
General EIA RS232C serial asynchronous I/O interface	DL11-WB		2.0	1	E Q S	BC05C-25 supplied	yes	Also requires −15V@.15A, +15V@.05A. Crystal must be specified at time of order.
A/D or D/A interface, 16-channel	AR11		5 max	1	E H S	BC11L-20	yes	May not be plugged into a modified UNIBUS slot.
2-word parallel input interface	DR11-L		1.5	1	E Q S		yes	Possible cables: BC07A, -7D, -8R, or -4Z.
2-word parallel output interface	DR11-M		1.5	1	E Q S		yes	
1-word parallel input/output interface	M7860		1.5	1	E Q S		yes	
Instrument remote-control interface	M1623		1.6	1	E Q S	special	no	
Instrument data input interface	M1621		.77	1	E Q S	special	no	
16-bit relay output interface	M1801		1.16	—	E Q S			
Direct Memory Access (DMA) interface	DR11-B		3.3	1	sys. unit		no	
DMA interface DECkit	KIT11-D		3.3	1	sys. unit		no	

Table 2 Interface Selector Guide—PDP-11 UNIBUS (cont.)

DEVICE OR FUNCTION	MODULE OR OPTION	LOGIC H'BOOK PAGE[2]	POWER +5V AMPS[1]	BUS LOADS	MODULE SIZE L H W[2]	CABLE REQ'D	FITS SPC SLOT?	COMMENTS
UNIBUS INTERFACE BUILDING BLOCKS:								
Interface foundation module	M1710		.79+	1	E Q S	BC07A or BC08R	yes	Has space for approx. 25 user ICs
Address selector module	M105		.338	1	E S S	—	yes	
Bidirectional bus interfacing gate module	M1500		.300	—	E S S	—	no	
But input interfacing driver module	M1501		.300	—	E S S	—	no	Not recommended for new designs.
Bus output interfacing driver module	M1502		.750	—	E D S	—	no	
Bus Request (BR)/Direct Memory Access (DMA) interrupt control module	M7821		.725	1	E S S	—	yes	
DMA word count/bus address module	M795		.600	—	E D S	—	no	
Master control module	M796		.180	—	E S S	—	no	
Bus driver module	M783		.070	—	E S S	—	no	
Bus driver module, non-inverting	M798		.320	—	S S S	—	no	
Bus receiver module	M784		.200	—	E S S	—	no	
Bus transceiver module	M785		.600	—	E S S	—	no	
Kit of ten DEC8640 bus receiver ICs	956		—	—	—	—	—	
Kit of ten DEC8881 bus driver ICs	957		—	—	—	—	—	
Wire-wrappable modules:								
Hex-height, no IC sockets	W9500		—	—	E H S		yes	
Hex-height, 84 16-pin IC sockets	W9503		—	—	E H S		yes	
Quad-height, no IC sockets	W9501		—	—	E Q S		yes	
Quad-height, 54 16-pin IC sockets	W9504		—	—	E Q S		yes	
Double-height, no IC sockets	W9502		—	—	E D S		yes	
Double-height, 24 16-pin IC sockets	W9505		—	—	E D S		yes	

NOTES:
1. + means current required by user logic must be added to figure shown.
2. Module sizes are given as Length, Height, and Width, as defined in General Information.
3. DSC = Direct Sales Catalog.


digital

DR11-L
2-WORD
INPUT INTERFACE OPTION

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

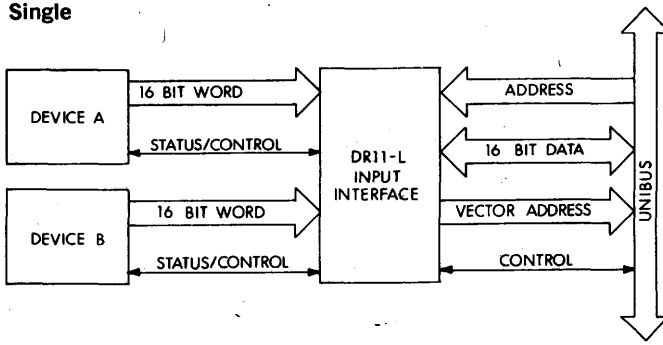


Figure 1 DR11-L Interface

DESCRIPTION

The DR11-L is a complete, self-contained input interface used to transfer two independent 16-bit, parallel data words from a user's peripheral device to the PDP-11 computer system as shown on Figure 1.

It is directly compatible with the PDP-11 UNIBUS and is designed for installation into any one of the available Small Peripheral Controller slots (SPC) of a BB11-M, DD11-A, or DD11-B System Interfacing Unit and the PDP-11 processor unit.

The DR11-L consists of address selection logic, interrupt control and priority level select logic, two Data Buffer Registers (DBRs), one for each word, and two independent Control/Status Registers (CSRs). One CSR is assigned to each input data word and provides status and control information during a word transfer.

Two control and two status lines between the user's device and the interface permit the establishment of a handshake routine to efficiently control the data transfers.

The input signal lines are TTL-compatible with high threshold receiver inputs and built-in hysteresis for both high and low threshold, providing substantial noise immunity. Input data lines are diode-clamped to +5 V and ground. Control lines from the user's device are diode-clamped to ground and pulled up to +5 V by a resistor.

All address selection, interrupt priority selection, and vector address selection is performed using Dual Inline Package (DIP) switches mounted on the

module. These switches facilitate the installation of the module by eliminating the need for soldering or removing jumper leads for address and vector selection.

The DR11-L is designed for user applications and requires a minimum of external hardware to implement into the PDP-11 system. Two 40-pin connectors are conveniently mounted near the edge of the board. These connectors permit either one or two external devices to be easily connected using BC08R or BC07D flat cables available from DIGITAL. These cables have the mating connectors premounted and are supplied in any specified length.

The interface module occupies one SPC slot and is a quad-height, extended-length, single-width module.

FUNCTIONS

DR11-L ELEMENTS AND SIGNAL FLOW

The main elements of the DR11-L interface module and the data, control, and status signal flow are shown on Figure 3. The module provides the complete interface logic necessary to allow the efficient transfer of data from user's device to the UNIBUS.

CONTROL/STATUS REGISTERS

Each CSR is a 16-bit register used to supply control and status information to the user's device and to provide control and status indicators of the user's device and interface to the processor. Each CSR is byte- or word-addressable.

DATA BUFFER REGISTER

Each DBR is used to store 16 bits of data from a device. The contents of the DBR are transferred to the processor under program control as a 16-bit data word or 8-bit byte. When addressed by the processor or when an interrupt request is asserted, the device data is latched into the DBR. Input data is not required to be held by the device for the entire transfer operation, thereby permitting faster data transfers.

DATA/CSR MULTIPLEXER

The multiplexer is controlled by the decoded device address and selects either 16 bits of data from a DBR or 16 bits of status and control information from a CSR for transfer to the UNIBUS. The selected output of the multiplexer is transferred to the processor under program control through the UNIBUS transceivers.

ADDRESS SELECTION LOGIC

The address selection logic decodes the addresses associated with each CSR and DBR and specifies the direction of data transfer.

INTERRUPT CONTROL LOGIC

The interupt control logic requests bus mastership on one of the four bus request lines of the UNIBUS, produces the interrupt request, and specifies the vector addresses of the interrupt routine pointers located in memory.

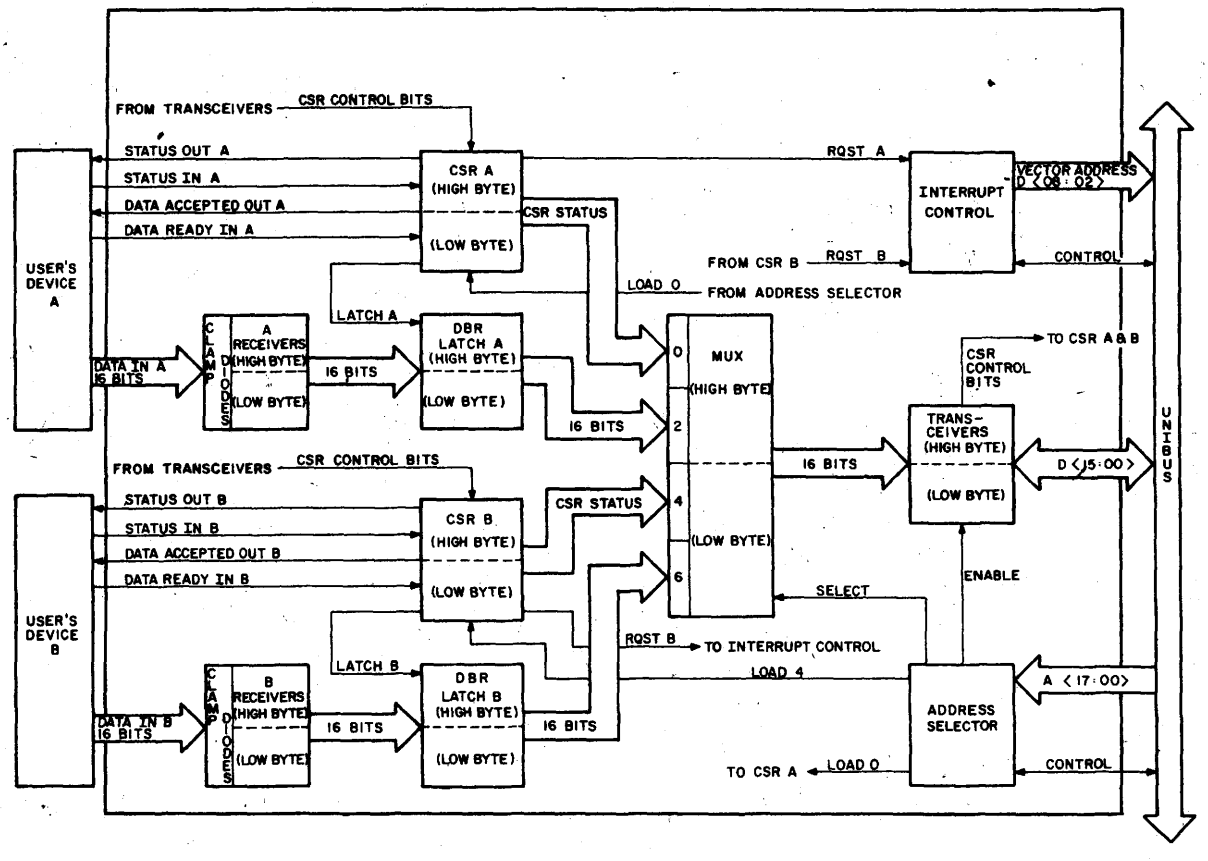


Figure 2 DR11-L Functional Block Diagram

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Page 58 does not exist in original

Page 59 does not exist in original

SWITCH PROGRAMMMABLE FUNCTIONS

The DR11-L module contains two DIP switch banks used to conveniently select the device address, the vector address, and the priority level of the interrupt requests.

Vector Address Switches—The vector address of the interrupt routine pointer located in memory is selected by six of the switches, allowing vectors up to 774_8 to be specified.

Priority Level—Switches: Two switches are provided to select one of the four Bus Request priority levels (BR4 through BR7) of the UNIBUS.

Device Address Switches—The address of the device is assigned with ten switches, allowing the module address to be located within the upper 4K address block dedicated to peripherals and user's devices.

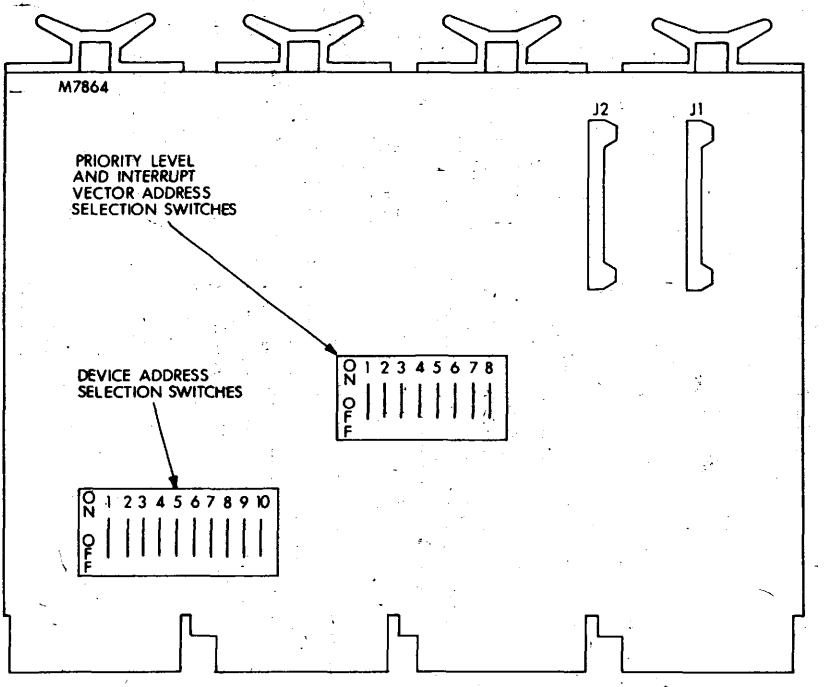


Figure 3 DR11-L Connector and Switch Locations

INTERFACE SIGNALS

UNIBUS Signals—The input and output data, control, and status signals conform to the UNIBUS signal specifications outlined in the PDP-11 Peripherals Handbook published by Digital Equipment Corporation. The DR11-L module presents no more than one unit load on any UNIBUS signal line.

DEVICE SIGNALS—Data and control signals are transferred between the devices and interface by two cables that attach to connectors J1 and J2. The location of the connectors on the module is shown on Figure 3. Table 1 lists the pin assignments of each connector and the signal drive or loading specification.

Table 1
Device Connector Signals

* J1 and J2 Connector Pin	Signal Name	TTL Unit Load
B	DATA IN 15 H	2 (each)
D	DATA IN 14 H	
F	DATA IN 13 H	
J	DATA IN 12 H	
L	DATA IN 11 H	
N	DATA IN 10 H	
R	DATA IN 09 H	
T	DATA IN 08 H	
V	STATUS OUT L	35 (driving)
X	STATUS IN L	5
Z	DATA IN 07 H	2 (each)
BB	DATA IN 06 H	
DD	DATA IN 05 H	
FF	DATA IN 04 H	
JJ	DATA IN 03 H	
LL	DATA IN 02 H	
NN	DATA IN 01 H	
RR	DATA IN 00 H	
TT	DATA ACCEPTED OUT B L	35 (driving)
VV	DATA READY IN B L	5

* Remaining pins of J1 and J2 connect to logic GND on DR11-L.

Four lines provide TTL-compatible signals between each CSR an dthe external device and can be used to establish a handshake routine for positive-control data transfers. Two lines can be used for status information to and from the processor, and two lines provide controlling information for data transfers utilizing program interrupts. The 8-bit byte or 16-bit data word from the device to the interface is supplied by the 16 Data In lines.

CABLE ASSEMBLIES—Several cable assemblies are available from DIGITAL for use with the DR11-L module. Table 2 lists some of the recommended cable types and standard lengths available.

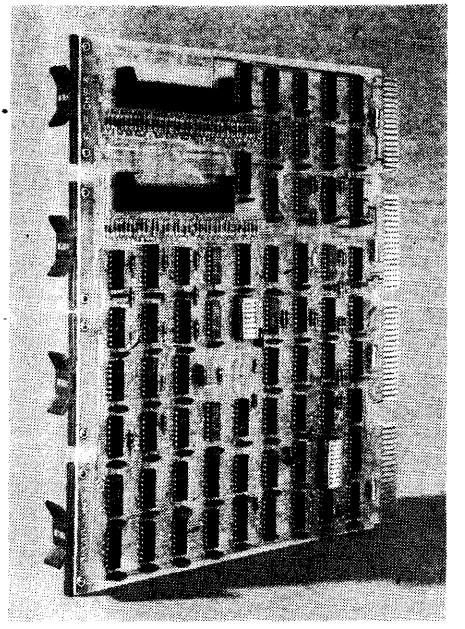
Table 2

Cable No.	Connectors*	Type	Standard Lengths (ft.)
BC07A XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

* The H856 connects directly to the DR11-L.

GENERAL SPECIFICATIONS

Input Data	
Configuration	Two parallel 16-bit data lines from a device.
UNIBUS Signals	Presents a maximum of one unit load on a UNIBUS line.
Operating Temperature	5°C (41°F) to 50°C (122°F)
Relative Humidity	10% to 90%, without condensation
Size	Quad height—10.5 in. (26.67 cm); single width—0.5 in. (1.27 cm); extended length—8.5 in. (21.59 cm)
Power	+5 V ±5% at 1.5 A nominal



DR11-L

DR11-M 2-WORD OUTPUT INTERFACE OPTION

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

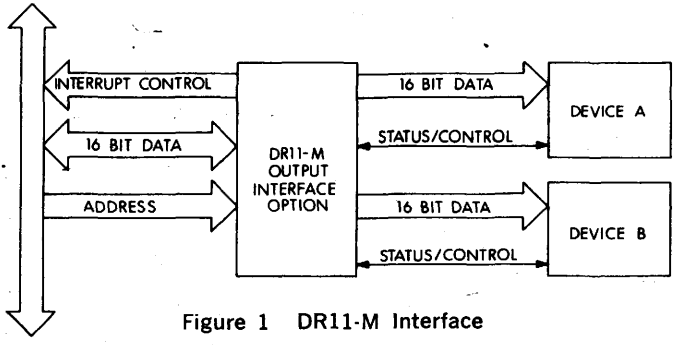


Figure 1 DR11-M Interface

DESCRIPTION

The DR11-M is a complete, self-contained output interface used to transfer two independent 16-bit, parallel data words from the PDP-11 computer system to a user's peripheral device. It is directly compatible with the PDP-11 UNIBUS and is designed for installation into one of the available Small Peripheral Controller slots (SPCs) of a BB11-M, DD11-A, DD11-B System Interfacing Unit or into the PDP-11 processor unit.

The DR11-M consists of address selection logic, interrupt control and priority level select logic, two Data Buffer Registers (DBRs), one for each word, and two independent Control/Status Registers (CSRs).

Each register is word or byte addressable, and the register contents can be read back into the processor under program control, allowing the full range of PDP-11 instructions to be used. Two control and two status lines between the user's device and the interface permit the establishment of a handshake routine to efficiently control the transfer of data.

Data, status, and control signals from the interface to the user's device are supplied from open collector output drivers capable of sinking 32 mA of load current. Each output is connected to +5 V through a pull-up resistor. This feature allows a variety of user devices to be directly connected to the interface without the need of external line drivers and discrete components.

All address selection, interrupt priority selection, and vector address selection is performed using Dual In-line Package (DIP) switches mounted on the module. These switches facilitate the installation of the module by eliminating

the need for priority plugs and soldering or removing jumper leads for address and vector selection.

The DR11-M is designed for user applications and requires a minimum of external hardware to implement into the PDP 11 system. Two 40-pin connectors are conveniently mounted near the edge of the board. These connectors permit either one or two external devices to be easily connected using BC08R or BC04Z flat cables available from DIGITAL. These cables have the mating connectors premounted and are supplied in any specified length.

The interface module occupies one SPC slot and is a quad-height, extended-length, single-width module.

FUNCTIONS

DR11-M ELEMENTS AND SIGNAL FLOW

The main elements of the DR11-M interface module and the data, control, and status signal flow are shown on Figure 2. The module provides the complete interface logic necessary to allow the efficient transfer of data from the UNIBUS to a user's device.

CONTROL/STATUS REGISTERS

Each CSR is a 16-bit register used to supply control and status information to the user's device and to provide control and status indicators of the user's device and interface to the processor. Each CSR is byte- or word-addressable.

DATA BUFFER REGISTERS

Each DBR is used to store 16 bits of data for transfer to the device. The DBR is a read/write register allowing the full range of PDP-11 instructions to be used.

DATA/CSR MULTIPLEXER

The multiplexer is controlled by the decoded device address and selects either 16 bits of data from a DBR or 16 bits of status and control information from a CSR for transfer to the UNIBUS. The selected output of the multiplexer is transferred to the processor under program control through the UNIBUS transceivers.

ADDRESS SELECTION LOGIC

The address selection logic decodes the addresses associated with each CSR and DBR and specifies the direction of data transfer.

INTERRUPT CONTROL LOGIC

The interrupt control logic requests bus mastership on one of the four bus request lines of the UNIBUS, produces the interrupt request, and specifies the vector addresses of the interrupt routine pointers located in memory.

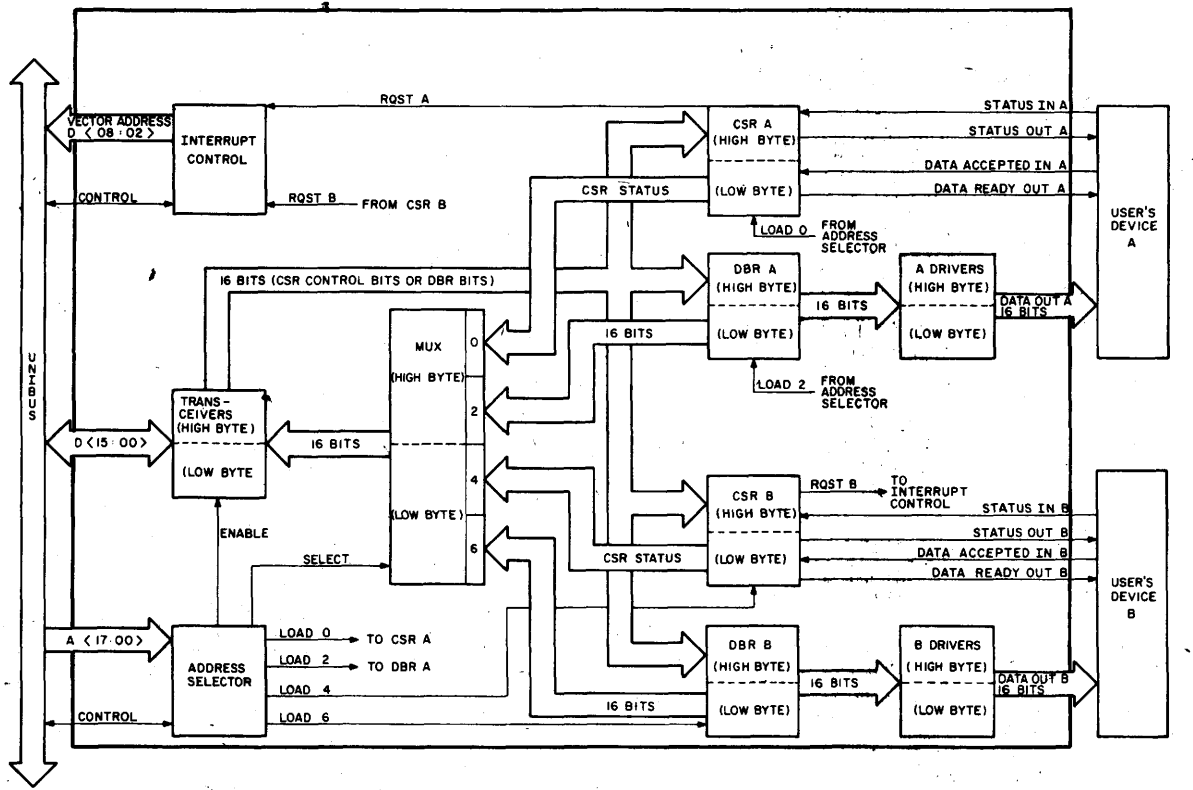


Figure 2 DR11-M Functional Block Diagram

SWITCH PROGRAMMABLE FUNCTIONS

The DR11-M module contains two DIP switch banks used to conveniently select the device address, the vector address, and the priority level of the interrupt requests.

Vector Address Switches—	The vector address of the interrupt routine pointer located in memory is selected by six of the DIP switches, allowing vectors of up to 774_8 to be specified.
Priority Level Switches—	Two switches are provided to select one of the four Bus Request priority levels (BR4 through BR7) of the UNIBUS.
Device Address Switches—	The address of the device is assigned with ten switches, allowing the module address to be located within the upper 4K address block dedicated to peripherals and user's devices.

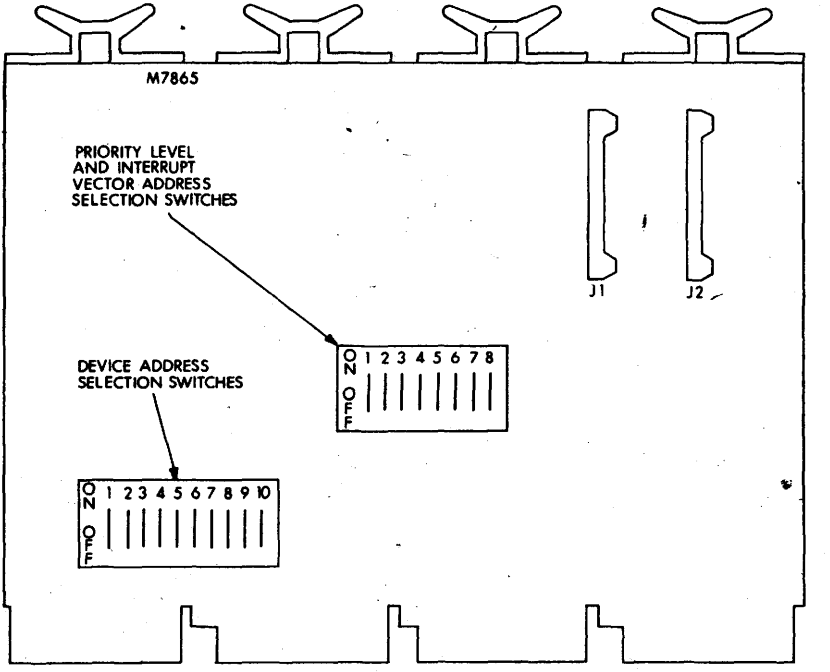


Figure 3 DR11-M Connectors and Switch Locations

INTERFACE SIGNALS

UNIBUS SIGNALS—The input and output data, control, and status signals conform to the UNIBUS signal specifications outlined in the *PDP-11 Peripherals Handbook* published by Digital Equipment Corporation. The DR11-M module presents no more than one unit load on any UNIBUS signal line.

DEVICE SIGNALS—Data and control signals are transferred between the devices and interface by two cables that attach to connectors J1 and J2. The location of the connectors on the module is shown on Figure 3. Table 1 lists the pin assignments of each connector and the signal drive or loading capability.

Table 1
Device Connector Signals

* J1 and J2 Connector Pin	Signal Name	TTL Unit Load
B	DATA OUT 15 H	20 (each)
D	DATA OUT 14 H	
F	DATA OUT 13 H	
J	DATA OUT 12 H	
L	DATA OUT 11 H	
N	DATA OUT 10 H	
R	DATA OUT 09 H	
T	DATA OUT 08 H	
V	STATUS IN L	5
X	STATUS OUT L	20
Z	DATA OUT 07 H	20 (each)
BB	DATA OUT 06 H	
DD	DATA OUT 05 H	
FF	DATA OUT 04 H	
JJ	DATA OUT 03 H	
LL	DATA OUT 02 H	
NN	DATA OUT 01 H	
RR	DATA OUT 00 H	
TT	DATA ACCEPTED IN L	5
VV	DATA READY OUT L	20

*Remaining pins on J1 and J2 connect to logic GND on DR11-M.

Four lines provide TTL-compatible signals between each CSR and the external device and can be used to establish a handshake routine for positive-control data transfers. Two lines can be used for status information to and from the processor, and two lines provide controlling information for data transfer utilizing program interrupts. The 8-bit byte or 16-bit data word from the interface to the device is supplied by the 16 Data Out lines.

CABLE ASSEMBLIES—Several cable assemblies are available from DIGITAL for use with the DR11-module. Table 2 lists some of the recommended cable types and lengths available.

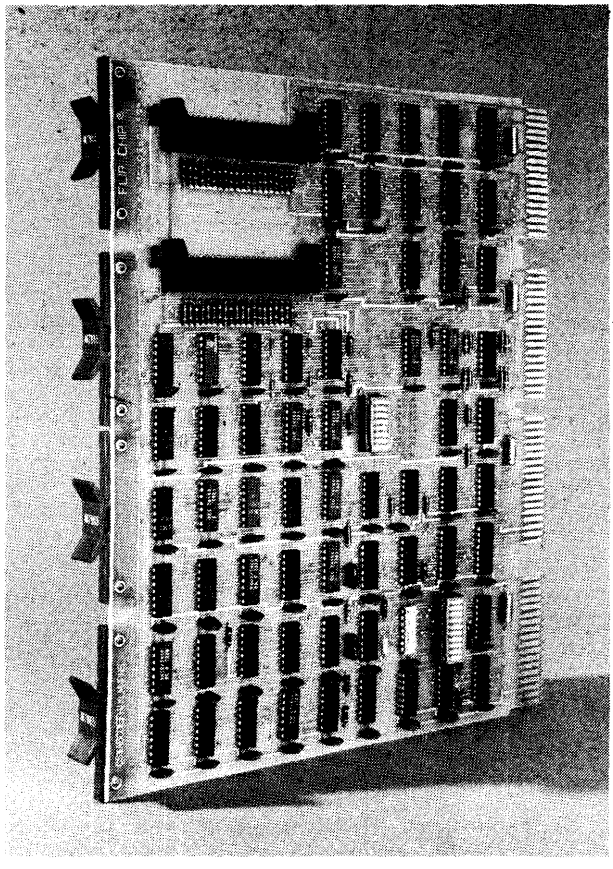
Table 2
Recommended Cable Assemblies

Cable No.	Connectors*	Type	Standard Lengths (ft.)
BC07A-XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

*The H856 connects directly to the DR11-M.

GENERAL SPECIFICATIONS

Output Data Configuration	Two parallel 16-bit data lines to a device providing TTL-compatible levels.
UNIBUS Signals	Presents a maximum of one unit load on a UNIBUS line.
Operating Temperature	5°C(41°F) to 50°C(122°F)
Relative Humidity	10% to 90%, without condensation
Size	Quad height—10.5 in. (26.67 cm); single width—0.5 in. (1.27 cm); extended length—8.5 in. (21.59 cm)
Power	+5V±5% at 1.5 A nominal



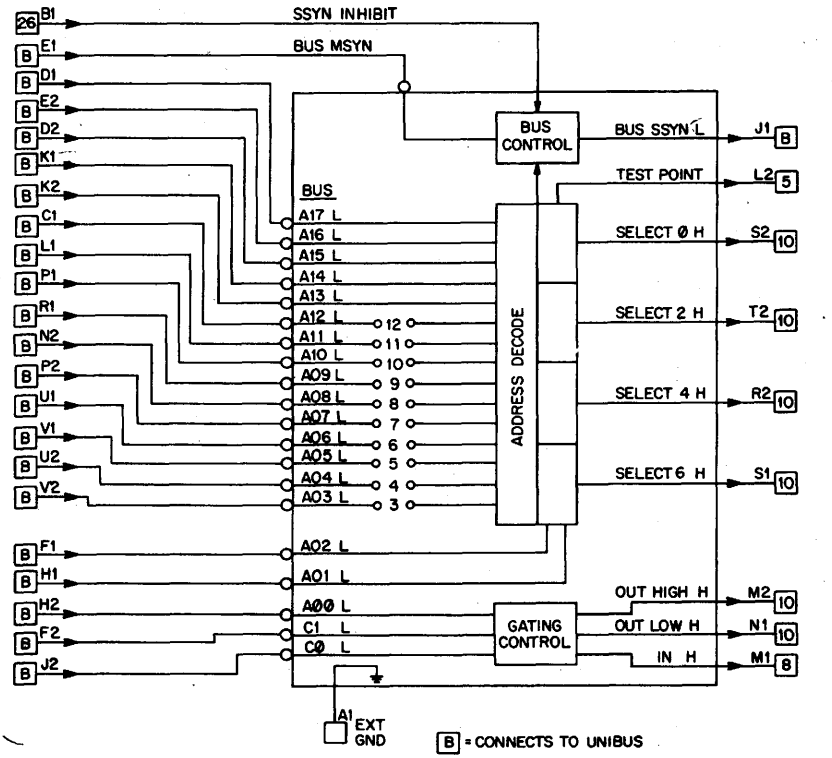
DR11-M

M105
ADDRESS SELECTOR

PDP-11
UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	338	A2
GND		C2, T1

The M105 is used in PDP-11 device interfaces to decode the UNIBUS Address and Control lines. It provides gating signals for up to four device registers that indicate a register is being referenced and three control signals that indicate the direction for data flow.

The selector decodes the 18-bit adress A <17:00> as follows: A <17:13> defines the section of the address map that is assigned to peripheral devices and must all be asserted. A <12.03> are determined by jumpers on the card.

When the jumper is "in" the selector will look for a zero in the binary equivalent of the register address on that address line. A02 and A01 are decoded to provide one of the four SELECT outputs. A00 is for byte control.

Signals for gating control are determined by decoding A00, C1, and C0. The signals obtained are: IN, OUT LOW, and OUT HIGH.

Instruction*	Corresponding M105 Output
DATI or DATIP	IN
DATO	OUT HIGH and OUT LOW
DATOB with A00 = 0	OUT LOW
DATOB with A00 = 1	OUT HIGH

*DATI, DATO, DATOB, DATIP are not PDP-11 instructions. They are names given to the various C-line combinations which are automatically configured by the processor for each instruction.

IN is used to gate data from a device register onto the bus. OUT LOW is used to gate D <07:00> from the bus into the low byte of a device register. OUT HIGH is used to gate D <15:08> into the high byte of a device register.

With respect to the bus master, the M105 is actually the "slave" in the relationship when a data transfer occurs on the UNIBUS.

SSYN is asserted whenever it sees its address being referenced and MSYN is asserted. SSYN is negated when MSYN is negated. There is an approximate 100 nsec delay between receiving MSYN and the assertion of SSYN to allow for decoding. Additional capacitance can be added to the delay circuit to increase this time, if desired. A practical maximum is a 1000 pf capacitor which will produce approximately 400 nsec of delay. If a longer delay is needed, the SSYN INHIBIT line can be grounded, which will prevent SSYN from being issued at all from the M105. The SSYN signal would then be generated from another source after the desired delay. SSYN INHIBIT can be left open when not used.

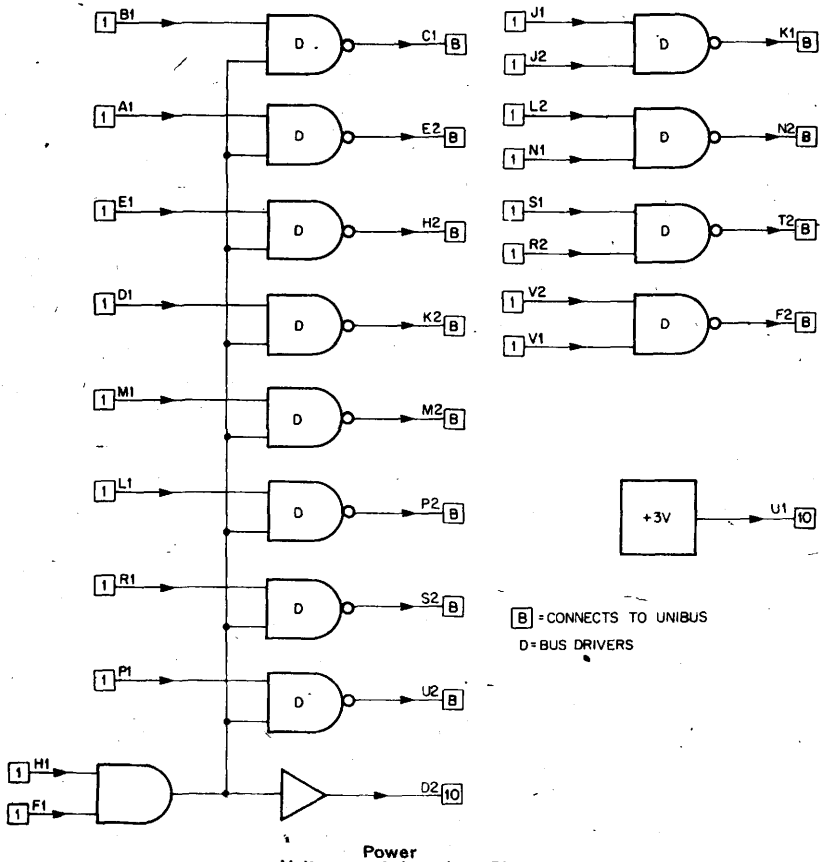
EXT GND is used for testing purposes and should be tied to ground in normal operation.

M783
UNIBUS DRIVERS

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

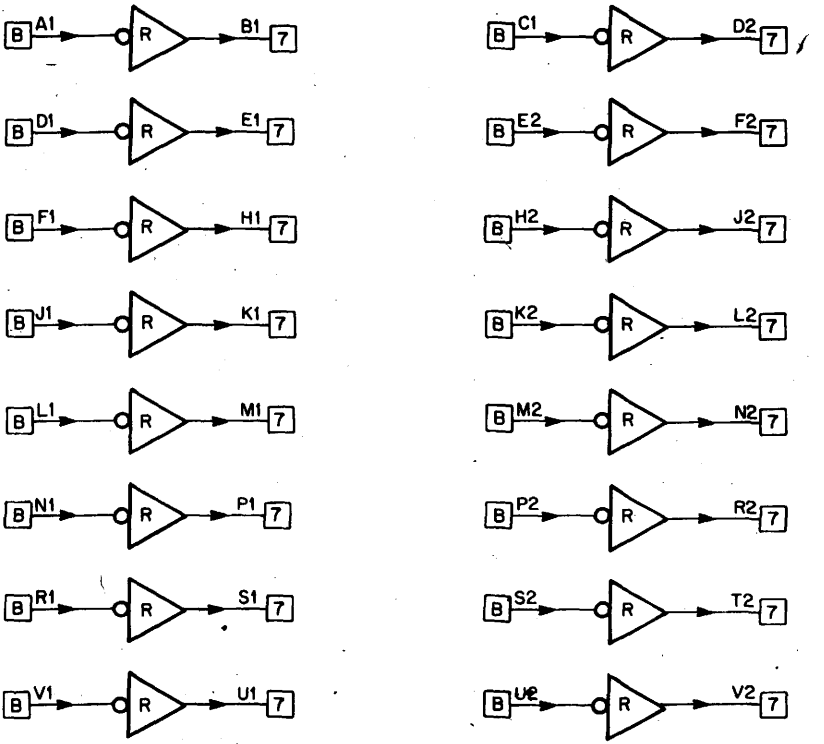
The M783 consists of 12 low-leakage bus drivers to be used as an input interface to the UNIBUS of the PDP-11. Each driver is open-collector and is capable of sinking 50 mA with a collector voltage of less than 0.8 volts. The output high leakage current is 25 microamperes maximum. Pin D2 is a TTL output that allows additional drivers to be controlled by the single enabling gate (inputs H1 and F1). Pin U1 provides +3 volts as a source of logic HIGH for 10 TTL loads.

M784
UNIBUS RECEIVERS

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	200	A2
GND		C2, T1

R= BUS RECEIVER
B=CONNECTS TO UNIBUS

The M784 consists of 16 high-impedance inverting bus receivers that are used as an output interface from the UNIBUS of the PDP-11.

SPECIFICATIONS

Input Loading: All inputs present one UNIBUS receiver load. (See UNIBUS description.)

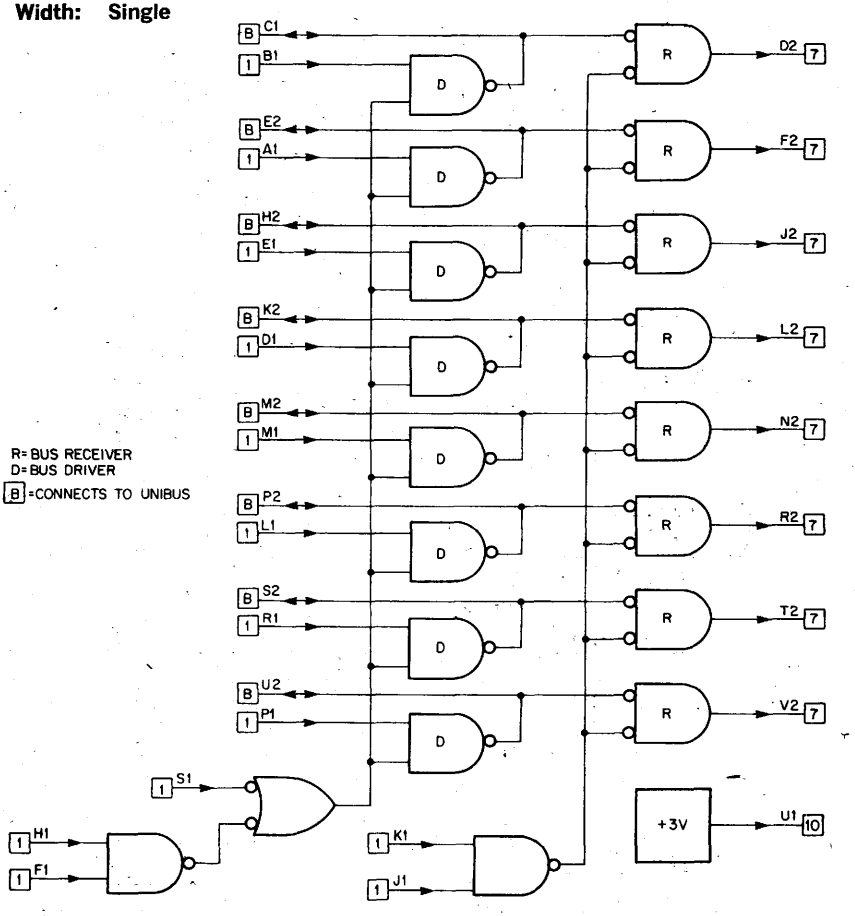
Output Drive: Each output has a fan-out capability of 7 standard TTL loads.

M785
UNIBUS TRANSCEIVER

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	118	A2
GND		C2, T1

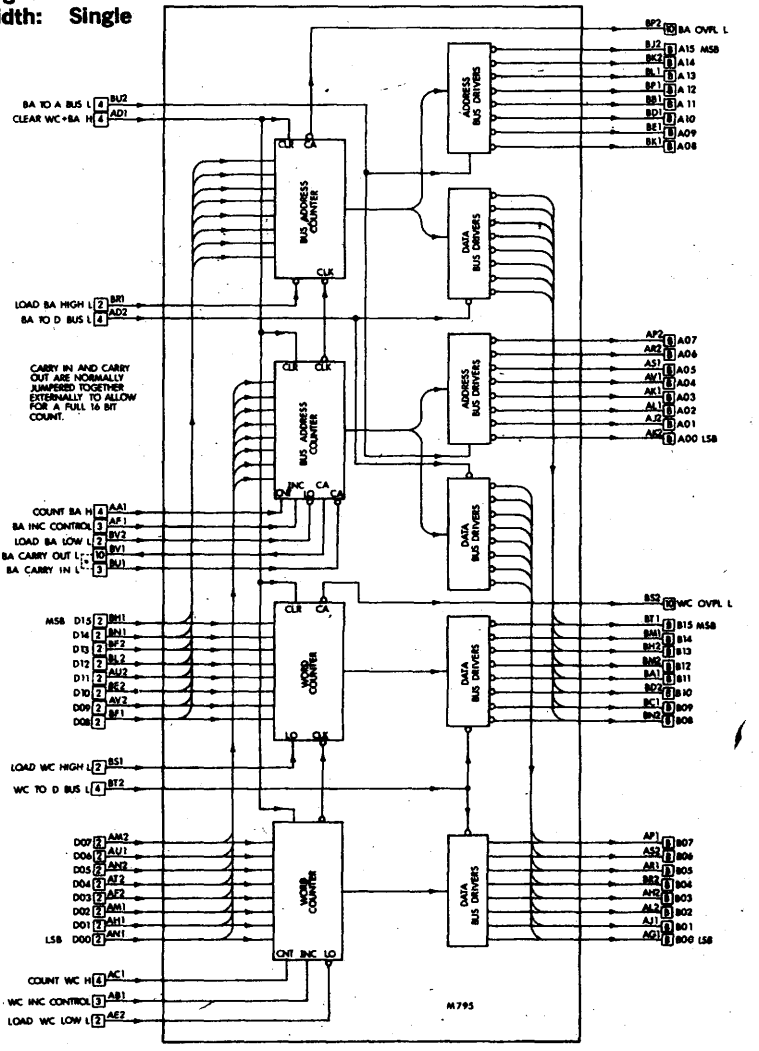
The M785 consists of eight drivers and eight receivers for use as a device interface with the PDP-11 UNIBUS. Pin U1 provides +3 volts and has an output capability of 10 TTL loads. Driver gates have open collectors and are capable of sinking 50 mA with a collector voltage of less than 0.8 volts. The output high leakage current is 2.5 microamperes maximum.

M795
WORD COUNT AND BUS ADDRESS MODULE

UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M795 Word Count and Bus Address Module can be used to provide two of the essential elements of an interface which connects Direct Memory Access (DMA) devices to the UNIBUS. This module contains two 16-bit counters. One counter is used to count the number of data transfers that occur. The other counter is used to specify sequential bus addresses for the sources and/or destinations of the data to be transferred.

FUNCTION

Word Counter

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is the transfer word count. Initially, this register (WC) is loaded by the computer with the 2's complement of the number of words to be transferred to or from memory. This number is clocked into the WORD COUNT register in two 8-bit bytes or one 16-bit word using the LOAD WC L (low byte) and LOAD WC + 1 L (high byte) inputs. After each data transfer is complete, the WC register is incremented by clocking the COUNT WC H input. When the new value of the WC register reaches 0, an overflow signal is generated at the WC OVFL L output, which would be used to inhibit further transfers and to signal that the transfer is complete. Information can be transferred in either words (16 bits each) or bytes (8 bits each), because the WC register may also be used as a byte counter.

Address Counter

The second parameter used in block transfers is the transfer address. Initially, a bus address register (BA Counter) is loaded by the computer with an address that specifies the memory location to or from which data is to be transferred. This address is loaded from the BUS DATA lines (D00-D15) in two 8-bit bytes or one 16-bit word using the LOAD BA L (low byte) and LOAD BA+1 L (high byte) inputs. The BA register is incremented after each transfer by clocking the CLOCK BA H input. The register continually "points" to sequential memory locations for block transfers.

BUS Drivers

Outputs of both the Word Counter and BA Counter are connected to a set of UNIBUS drivers so that the counter contents can be gated to the DATA BUS when the appropriate enable signals (BA TO BUS L and WC TO D BUS L) are asserted. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the ADDRESS BUS when the BA TO BUS L input is asserted.

Counter Increments

The BA register can be incremented by either 1 or 2 as a function of the BA INC CONTROL input (High=1, Low=2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the COUNT BA H input of the register. The carry between bits 03 and 04 is broken and brought out to pins BV1 (BA CARRY OUT L) and BU1 (BA CARRY IN L). Normally these pins are connected together externally to allow for a full 16-bit count. They can, however, be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse (BA OVFL L) is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of the WC INC CONTROL input (High=1, Low=2). The register increments on the trailing edge of a positive pulse applied to the COUNT WC H input of the register.

An overflow pulse is also available at pin BS2 (WC OVFL L). Both registers reset to 0's whenever the CLEAR WC+BA H signal is asserted.

The storage elements on the M795 module are not edge triggered devices. Data must be established and held for the duration of the loading pulse.

The data inputs to the registers are not bus receivers and can not be connected directly to the UNIBUS. Use the M784 or equivalent.

APPLICATIONS

This module is used to interface direct memory access (DMA) devices to the UNIBUS.

SPECIFICATIONS

Propagation Time:

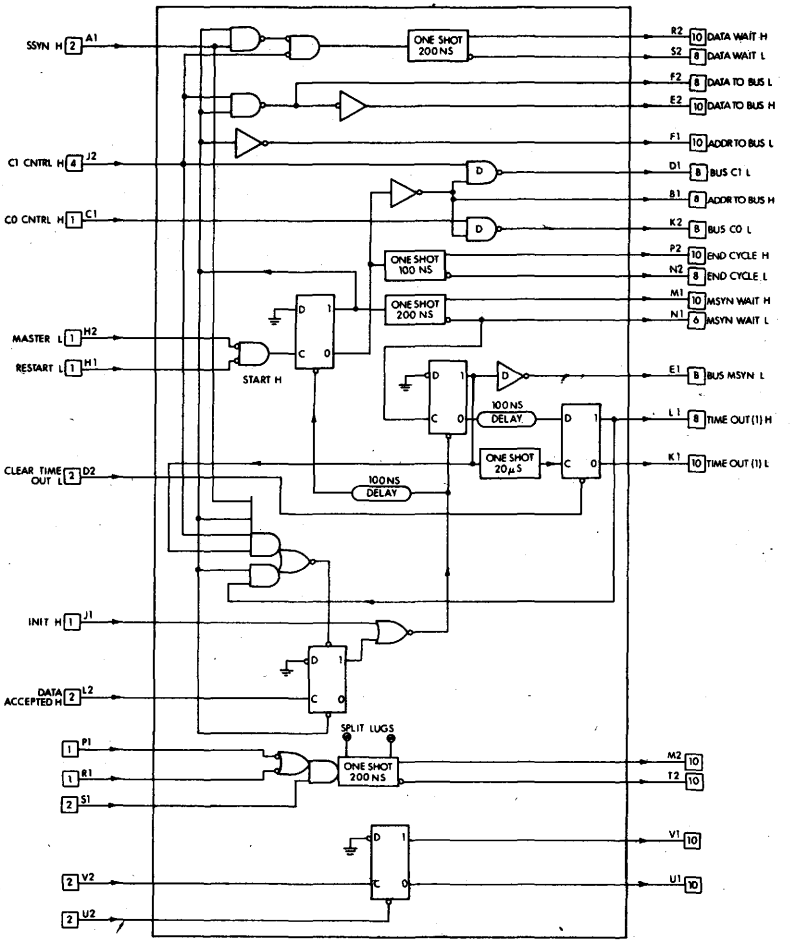
FROM	TO	ns (max.)
CLEAR WC+BA	WC+BA Outputs	125
LOAD WC L	WC Outputs	75
LOAD WX+1 L	WC Outputs	75
COUNT WC H	WC Outputs	60
LOAD BA L	BA Outputs	75
LOAD BA+1 L	BA Outputs	75
COUNT BA H	BA Outputs	60

M796
UNIBUS MASTER CONTROL

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M796 UNIBUS Master Control Module provides the necessary logic to enable a peripheral device to perform a bus cycle on the UNIBUS to transfer data. In addition to controlling the four transfer operations (DATI, DATIP, DATA, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles de-skewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used by the customer for special control functions.

Any device in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed independently of processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the UNIBUS is provided by the M7821 Interrupt Control module.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs data (either a word or byte) from memory or from another peripheral; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage) or is sending data to another peripheral; a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the M796 must set Bus CO and Bus C1 for the required type of data transfer, assert the MSYN signal, and then wait for the SSYN repsonse from the slave. Data must either be gated to the Bus data lines on a DATO cycle or be received and strobed at the proper time on a DATI cycle.

The Bus C1 and Bus CO outputs of the M796 can directly drive the UNIBUS and are asserted as a function of the control inputs C1 CNTRL H and CO CNTRL H. Table 1 lists the states of the control inputs for the four possible bus cycles. Note that for DATI or DATO, only C1 has to be varied while holding CO low.

Table 1. Control Line Input States for M796

C1	CO	Bus Cycle
L	L	DATI
L	H	DATIP
H	L	DATO
H	H	DATOB

The data transfer sequence is triggered by meeting the AND condition of the low state of both MASTER L (H2) and RESTART L (H1). Usually these two inputs are tied together and are connected to the MASTER L signal produced by the M7821 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both Bus C1 and Bus CO are asserted as determined by their respective control inputs. The ADRS to Bus signals are also asserted and are used to gate the address of the slave onto the bus address lines (Bus A 17:00). If an output cycle is specified (C1 = 1), the DATA TO BUS signals (both H and L) are also asserted and are used to gate data to

be transferred to the slave onto the bus data lines (Bus D 15:00). When the MSYN WAIT one-shot times out after 200ns, the BUS MYSN L signal is asserted. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN by the slave causes BUS MYSN to be negated immediately. After a 100-nanosecond delay, BUS C1, BUS C0, ADRS TO BUS and DATA TO BUS are negated. When these signals drop, the END CYCLE pulse appears and is usually used to release control of the bus.

In a data input cycle (DATI), the assertion of the SSYN input produces a 200-nanosecond pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necssary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED L causing BUS MSYN to be negated initially, followed by negation of ADDR TO BUS, BUS C1. and BUS C0 100 nanoseconds later.

A TIME-OUT flip-flop is set if a SSYN response fails to occur within 20 microseconds after BUS MSYN is asserted. When this flip-flop is set, the bus cycle is terminated and END CYCLE is issued. The TIME OUT signals are used to indicate an error condition. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME OUT L input.

The M796 module provides an extra flip-flop that has the clock (V2), reset (U2), 1 side (V1) and 0 side (U1) available to the customer. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true. The output pulse width at pins T2 and M2 is 150 nanoseconds but can be lengthened by adding capacitance across the pair of split lugs on the module. The following equation can be used to determine the approximate value of the added capacitance:

$$T_{pw} - 0.32 \text{ (RC}$$

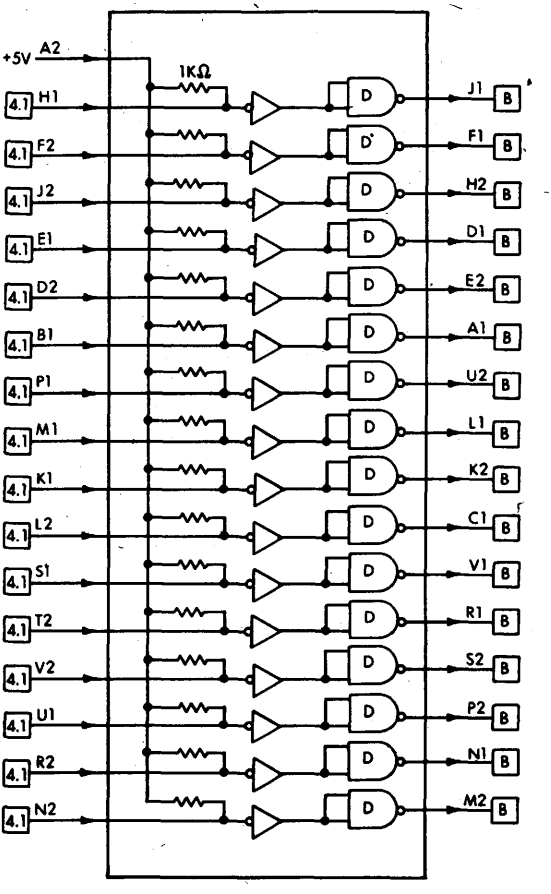
where T_{pw} is in milliseconds, R is in ohms, and C is in microfarads. (The internal resistance is 5.6 kilohms.)

Note that all times mentioned above represent nominal values with a tolerance of ± 25%. The delays and pulses provided by the module are controlled by simple RC circuits: therefore, if the user has any special requirements, part substitutions can be made to alter these time constants.

M798
UNIBUS DRIVERS

UNIBUS

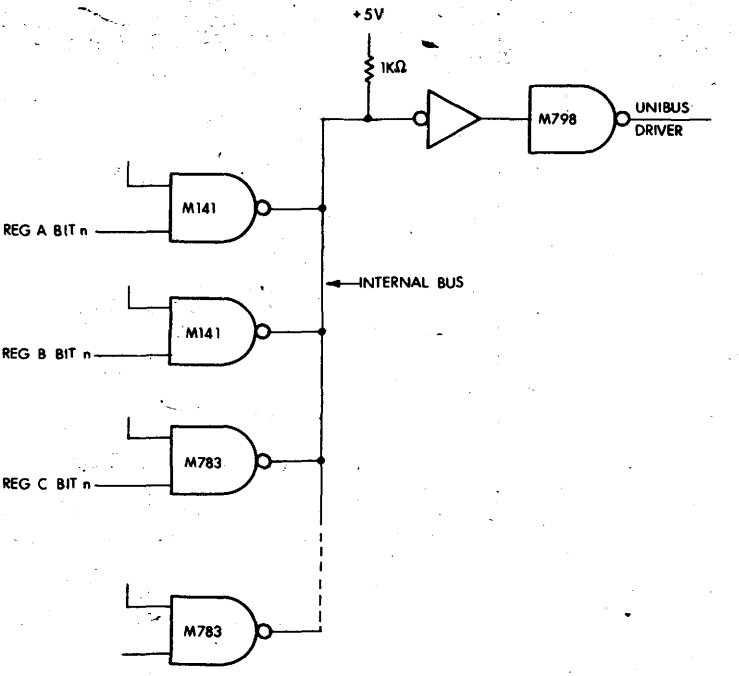
Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	320	A2
GND		C2, T1

This module consists of 16 noninverting UNIBUS drivers with pull-up resistors on the inputs. The module is used in device interfaces to minimize the loading effect caused by attaching several drivers to the same UNIBUS signal line, as in the case of a device containing multiple registers. Loading of signal lines on the UNIBUS is restricted to the equivalent of one UNIBUS receiver input and two UNIBUS driver outputs per device.

In addition, the M798 module allows the UNIBUS to be driven by standard open-collector TTL gates. The inputs to each M798 driver circuit are pulled up to +5 V through a 1-kilohm resistor. As shown below, an internal wired-OR multiplexer is created that is driven from standard open-collector gates or from UNIBUS drivers (such as the M1501 or M783).



Typical Use of M798

SPECIFICATIONS

Output Driver: The output Low voltage for each of the 16 outputs is 0.8 volts maximum with 50 mA current sink. The output High leakage current is 25 microamperes maximum.

Propagation Delay: The propagation delay between the 16 inputs and the driver outputs is 60 nanoseconds maximum.

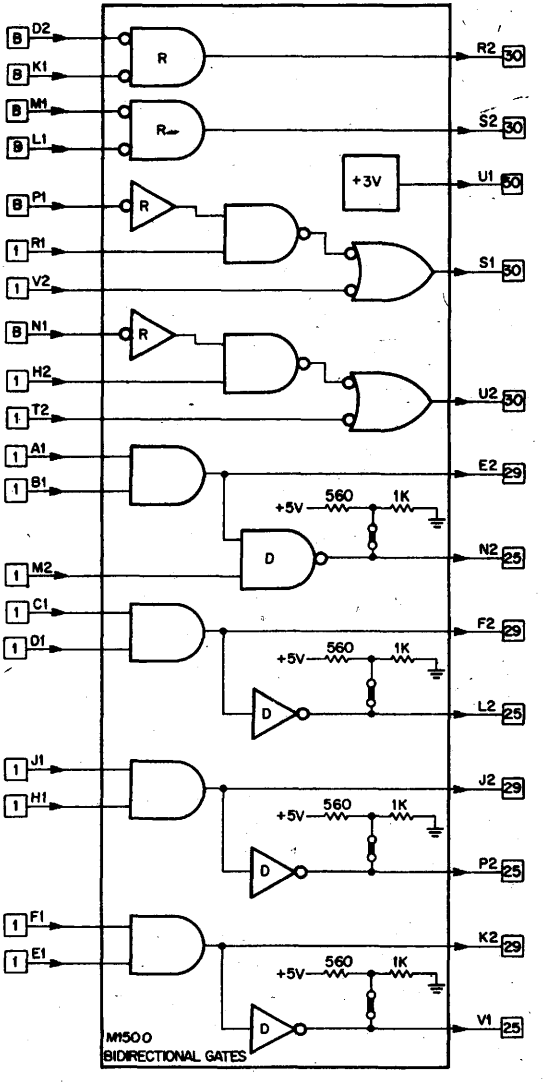
M1500
BIDIRECTIONAL BUS INTERFACING GATES

UNIBUS

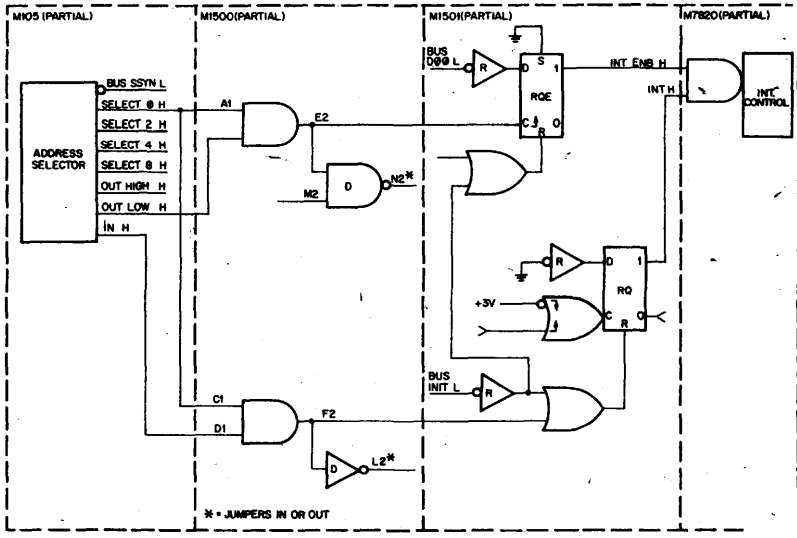
M SERIES

Length: Extended
Height: Single
Width: Single

Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1



This module provides gating arrangements useful for interfacing to the PDP-11 computer. It is designed specifically to provide additional gating and output drive when using the M1501-M1502 Input/Output modules. An example is shown in the following figure.



Using M1500 AND Gates with M1501 in PDP-11 Interfacing.

APPLICATIONS
PDP-11 Interfacing:

1. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to load registers
2. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to form set or reset pulses
3. Receiving the INIT (initialize) signal from the UNIBUS and distributing it via high-power drivers

General-Purpose Use:

1. Providing general-purpose high fan-out drivers
2. Providing a stage of inversion with high fan-out capability

FUNCTIONS
Inputs marked B present one bus receiver load to the UNIBUS. All other inputs are standard TTL; unit loads are shown on the logic diagram.

Output drivers marked D provide open collector outputs with jumpered-in pull-up resistors to enable their use in general logic applications. These outputs may be used to drive UNIBUS lines if the associated jumpers are cut by the user.

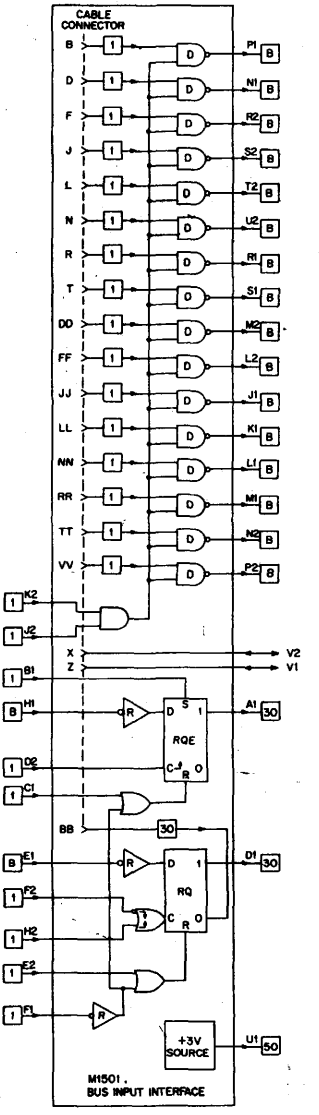
All other outputs provide standard TTL drive as shown on the logic diagram.

M1501
BUS INPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1

The M1501 contains 16 bus drivers for interfacing parallel input data to the PDP-11 UNIBUS. The module includes two control flags that can be used for interrupt request and enable. Data inputs from an external device enter a 40-pin flat cable connector mounted on the module itself. All inputs are diode-clamped to ground and +5 volts.

APPLICATIONS

Up to four M1501 modules (64 bits) can be controlled by one M105 Address Selector module, one M7821 Interrupt Control module, and one M1500 Bus Gates module.

FUNCTIONS

Input from Cable: Data is gated from the input connector to the bus when both enabling inputs (K2, J2) are HIGH.

Send/Receive Control Signal: Two additional lines are provided from the cable connector (Pins X and Z) to the module to allow communications between the device and the computer.

Flags: A request flag (RQ) and a request enable flag (RQE) are included on the M1501. Both flags can be cleared on start-up directly from the PDP-11 INITIALIZE bus line through pin F1. Both flag clock inputs are transition sensitive. The data input to each flag is buffered by a bus receiver; thus, status data can be entered directly from a bus line if desired. The request enable flag clock input responds to a HIGH going transition. The request flag has an input that is sensitive to a LOW going transition and an input that is sensitive to a HIGH going transition. (Whichever input is not used should be connected to the proper logic level to unassert it.) The user is given the maximum degree of freedom to use the request enable flag as a D flop or as an RS flop because all inputs are accessible.

The output of each flag is fully buffered (not shown in diagram) to protect the flag data as well as to provide high output drive.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
40-Pin Connector Inputs	Bus Data Outputs	50
Flag Clock Inputs	Flag Outputs	75

M1502
BUS OUTPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single

Volts	Power mA (max.)	Pins
+5	750	A2
GND		C2, T1

The M1502 is a versatile buffered output interface for up to 16 data bits, arranged in two 8-bit bytes. The module accepts data from the UNIBUS Data lines and stores it in a 16-bit register. Outputs are supplied both to a 40-pin flat ribbon connector and to the backplane. Open-collector output drivers with pull-up resistors are included on the module. Three flip-flops with type D as well as type RS inputs are provided as flags or synchronizing devices.

APPLICATIONS

Although intended for parallel data output this module may be used to drive indicators or small relays provided the voltage and current limits are not exceeded.

Up to four M1502 modules (64 bits) can be controlled by one M105 Address Selector module, one M7821 Interrupt Control module, and one M1500 Bus Gates module.

FUNCTIONS

Input from Bus: Data is loaded from the bus to the storage register on a positive transition of the loading inputs (AB1 and AA1), which loads the upper and lower bytes respectively providing the enabling input (AM1) is high.

Flags: Three edge-triggered flip-flops are provided. Two of the flags may be triggered by either negative or positive transitions; these supply buffered drive to 40-pin connector outputs. The third flag is triggered by positive-going transitions only. This flag provides an output to the blackplane only.

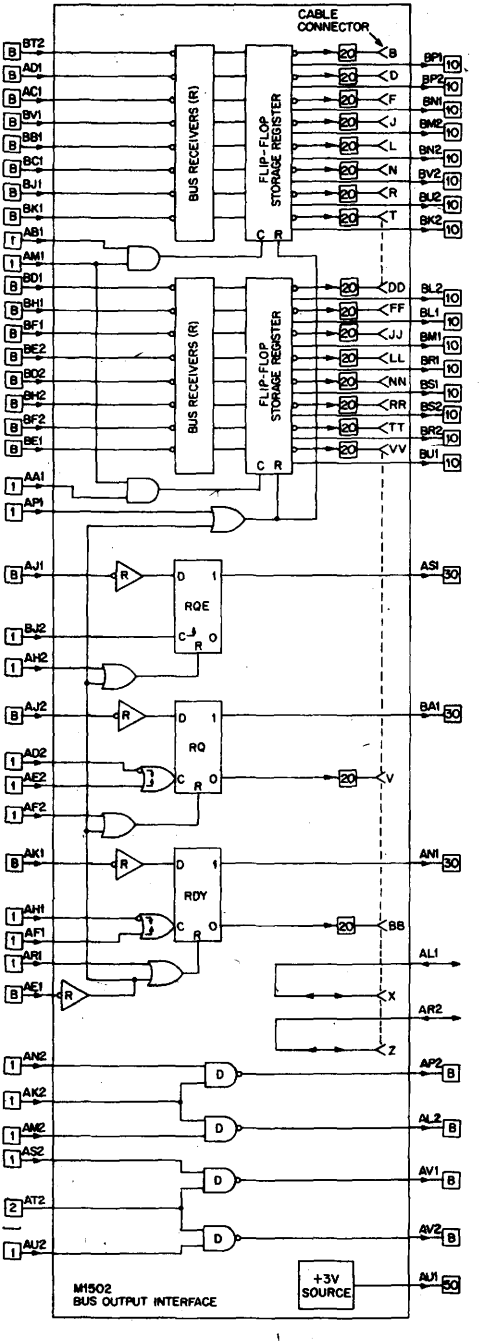
All flags have separate reset inputs and may also be cleared by a common reset line. The set and reset functions occur on logic HIGH levels. Unused inputs should be connected to a logic level that will unassert them. Spare bus drivers are also provided.

Spare Lines: Two additional lines are provided between the cable connector and the module for additional communication between the module and the external device. These lines are diode protected against voltage over shoot below —0.75 volts or above +5.75 volts.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
BUS DATA Input	40-Pin Output	100
FLAG CLOCK Input	40-Pin Output	150
FLAG SET or CLEAR Input	Backplane Output	100


CABLE CONNECTOR
BUS RECEIVERS (R)
FLIP-FLOP STORAGE REGISTER
RQE
RQ
RDY
+3V SOURCE
M1502
BUS OUTPUT INTERFACE

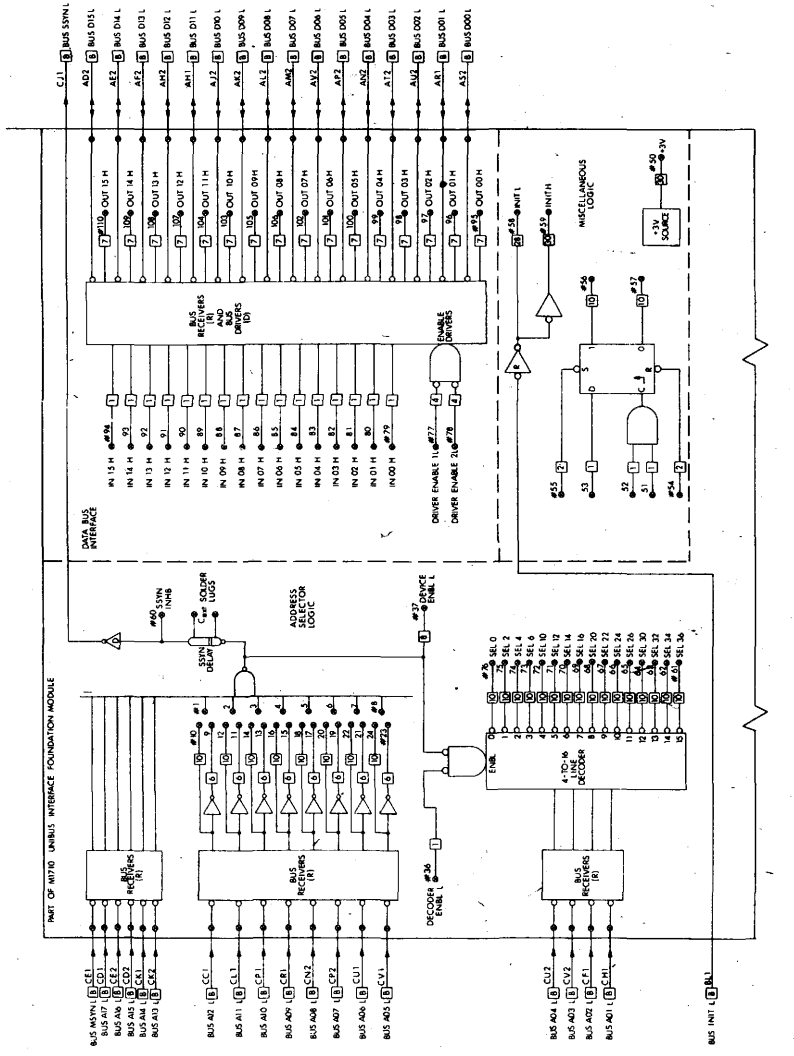
Output Drive: Oututs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors (1K ohm) included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many types of indicators and even relays. However, if inductive loads are driven, diodes should be wired across each load to bypass inductive kickback.

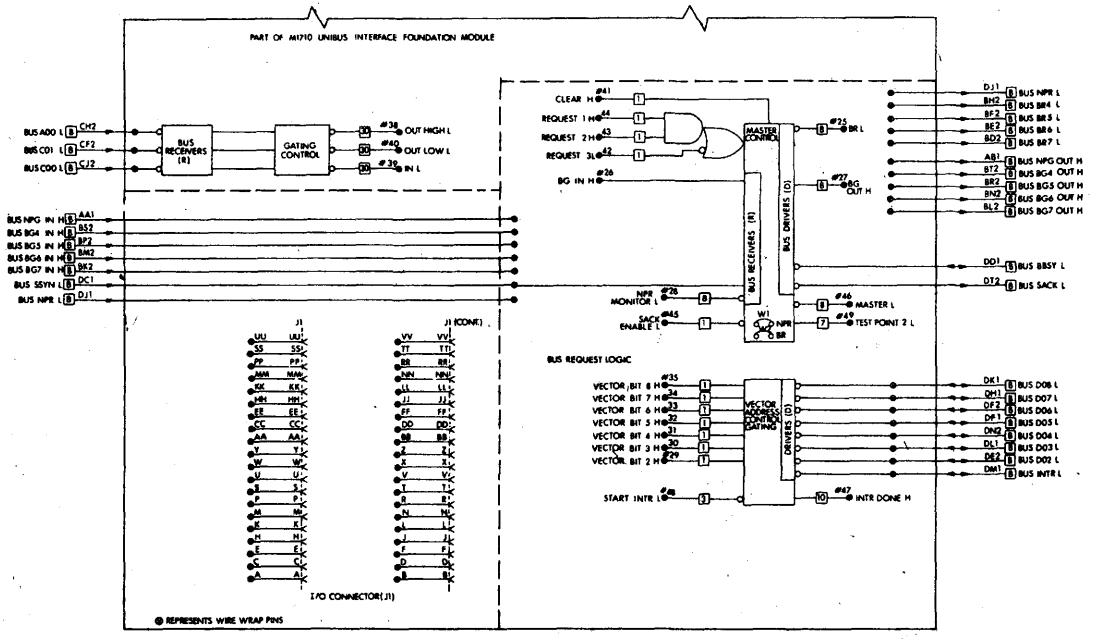
M1710
UNIBUS INTERFACE FOUNDATION MODULE

UNIBUS

M SERIES

	VOLTS	mA TYP	PIN
Length: Extended	+5 V @ ± 5%	790	AA2, BA2, CA2
Height: Quad	GND		All Pins C, T
Width: Single			




PART OF M1710 UNIBUS INTERFACE FOUNDATION MODULE
BUS A00 L
BUS C01 L
BUS C00 L
BUS RECEIVERS (R)
GATING CONTROL
OUT HIGH L
OUT LOW L
IN L
BUS NPG IN H
BUS BG4 IN H
BUS BG5 IN H
BUS BG6 IN H
BUS BG7 IN H
BUS SSYN L
BUS NPR L
CLEAR H
REQUEST 1 H
REQUEST 2 H
REQUEST 3L
BG IN H
MASTER CONTROL
BUS DRIVERS (D)
BUS RECEIVERS (R)
BR L
BG OUT H
BUS NPR L
BUS BR4 L
BUS BR5 L
BUS BR6 L
BUS BR7 L
BUS NPG OUT H
BUS BG4 OUT H
BUS BG5 OUT H
BUS BG6 OUT H
BUS BG7 OUT H
BUS BBSY L
BUS SACK L
NPR MONITOR L
SACK ENABLE L
W1
MASTER L
TEST POINT 2 L
BUS REQUEST LOGIC
VECTOR BIT 8 H
VECTOR BIT 7 H
VECTOR BIT 6 H
VECTOR BIT 5 H
VECTOR BIT 4 H
VECTOR BIT 3 H
VECTOR BIT 2 H
VECTOR ADDRESS CONTROL LOGIC
START INTR L
INTR DONE H
BUS DO8 L
BUS DO7 L
BUS DO6 L
BUS DO5 L
BUS DO4 L
BUS DO3 L
BUS DO2 L
BUS INTR L
J1
J1 (CONT.)
I/O CONNECTOR(J1)
REPRESENTS WIRE WRAP PINS

DESCRIPTION

The M1710 UNIBUS® Interface Foundation Module is a general-purpose board that provides for the construction of custom interface designs using integrated circuits (ICs). The M1710 lets users build their own interfaces between a wide variety of peripheral equipment and any PDP-11 processor. All essential UNIBUS logic, such as device address selection, interrupt circuitry, and bus receivers and drivers, is provided on the lower portion of the module. The remainder of the board contains IC mounting pads with wire-wrappable pins for custom logic designs. These pads accommodate combinations of all common type of DIP (dual-in-line-package) integrated circuits with up to 40 pins.

The M1710 is a versatile module, ideal for any type of application. The end user, such as a university laboratory familiar with ICs, will appreciate both the capabilities and cost-effectiveness of the module; no additional mounting panel or power supply is required. These features, coupled with the fact that the M1710 is capable of automatic wire wrapping, also should prove valuable to the Original Equipment Manufacturer (OEM) who requires many custom interfaces. And, in all cases, the module is easily adaptable to accommodate any changes in interface design.

The M1710 plugs into any Small Peripheral Controller (SPC) slot of a DECkit11-M Instrument Interface or DD11 Peripheral Mounting Panel. Additionally, it may be used in a system unit such as the BB11-A. Connection to user equipment is made via a cable connector mounted on the M1710 module.

FEATURES

- "Do-it-yourself" interfacing.
- Complete single-card interface.
- Plugs directly into Small Peripheral Controller (SPC) slot.
- Can be used with DECkit11-M Instrument Interface Kit.
- Saves hardware and building costs.
- Preassembled/pretested UNIBUS circuitry eliminates need to build the required bus interfacing functions.
- Wire-wrappable interconnections—compact, 30-gauge wiring used for all IC lead interconnections.
- I/O connection directly to module board—standard 40-conductor cables available.
- All accessories and tools available.
- Accepts all common Dual-in-Line Packages (DIPs); mounts up to 16 of the 14- or 16-pin type plus a multi-use pad set that mounts two 40-pin types, three 24-pin types, four 14- or 16-pin types, or combinations of these.
- Additional bus driver and bus receiver ICs available—special high-impedance devices: DEC 8881, DEC 8640.
- Includes source of +3 V—convenient for tying unused TTL inputs high, etc.

APPLICATIONS

Since more and more devices are becoming available in DIP form, quite complex systems can be built on the M1710. Some typical applications include:

- Multiword input and/or output.
- Programmable instrument interfaces.
- Interprocessor buffers.
- Custom peripheral controllers.
- Interfacing of:
  - Microprocessors
  - A/D converters
  - Multiplexers
  - Counters
  - Shift registers
  - ROM and RAM memories
  - Arithmetic logic units
  - Programmable logic arrays (PLA)

FUNCTIONS

The M1710 can be divided into four functional sections: address selector logic, bus request logic, data bus interface, and miscellaneous logic.

Address Selector Logic

The address selector logic provides gating signals for up to 16 full 16-bit device registers. Addresses which can be chosen by the user range from 760000_8 to 777777_8. The basic M1710 address selection is similar in function to the M105 Address Selector Module. The input signals for the address selector logic consist of: 18 address lines BUS A<17:00>; two bus control lines, BUS C<1:0>; and a master synchronization lines, BUS MSYN. The address selector decodes the 18-bit address on lines BUS A<17:00>; receives MSYN and issues SSYN.

Bus Request Logic

The M1710 contains the circuitry required to make a bus request and gain control of the bus at either the NPR level or at one of the BR levels. The module also includes circuitry required for transferring a vector address during an interrupt operation.

Data Bus Interface

The M1710 contains standard UNIBUS receivers which provide a buffered bus signal output for each of the 16 data lines OUT 00 H through OUT 15 H. Output drive capability of these receivers is seven TTL unit loads.

The module also includes 16 bus drivers which drive data lines IN 00 H through IN 15 H. Input loading to each driver is one standard TTL load. All 16 drivers have two common gate line enables (DRIVER ENABLE 1 and DRIVER ENABLE 2) which require a logic Low for assertion. Each enable represents four TTL unit loads.

Miscellaneous Logic

The following additional circuitry is also provided on the M1710:

- Inverted and noninverted buffered initialize outputs (pins 58 and 59) capable of driving 28 and 30 TTL unit loads respectively.
- A general-purpose flip-flop with all input and output pins available for wire wrap (pins 51 through 57).
- A +3-volt source (in 50) capable of driving 30 TTL unit loads.

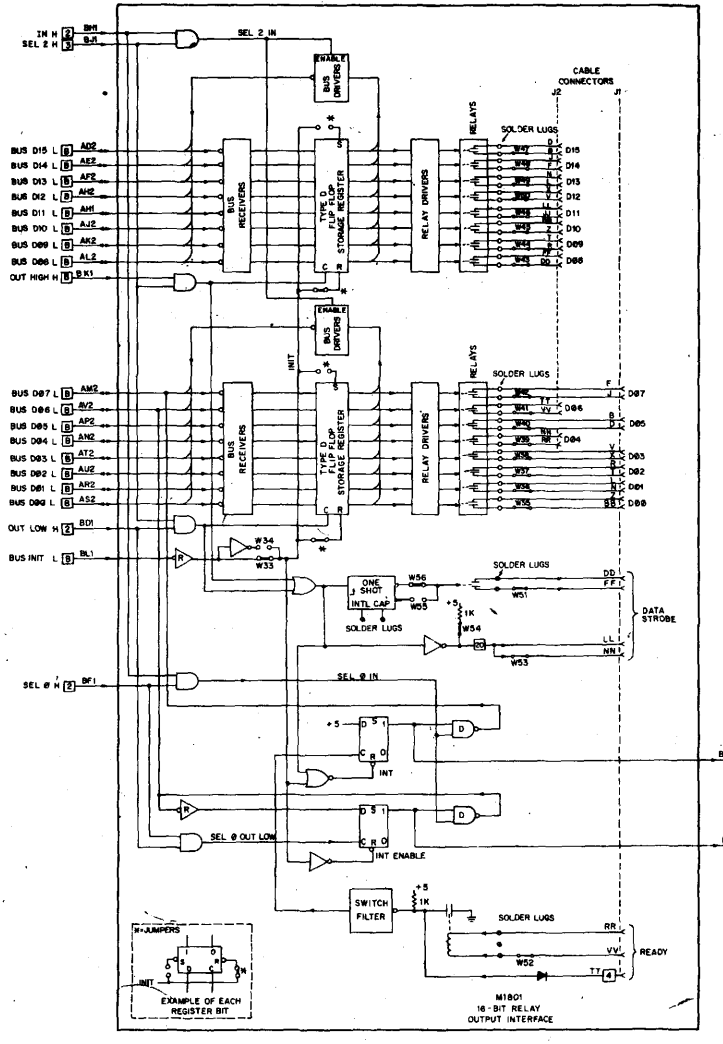
M1801
16-BIT RELAY
OUTPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Volts	Power mA (max.)	Pins
+5	1450	A2
GND	-	C2, T1



The M1801 is a PDP-11 interface module containing the bus receivers, relay drivers, and control logic needed to program 16 isolated single-pole relay contacts. The relay contact outputs are available at two 40-pin cable connectors mounted on the module.

APPLICATIONS

For interfacing to the PDP-11, the M1801 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1801 under program control. Interrupt circuitry is also built into the M1801 and can be used in conjunction with the M7821 or equivalent. An example of a typical PDP-11 interface is shown in the M1623 description.

FUNCTIONS

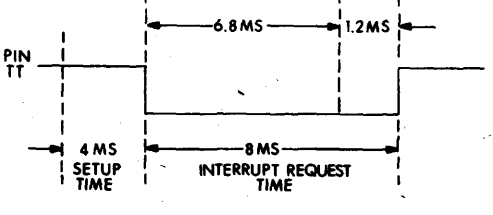
Registers: The M1801 contains two 8-bit read-write registers, both interfaced to the computer bus data lines by bus receivers. Data from the computer is clocked into the registers by strobing signals derived from an M105. The registers have read-back capability for PDP-11 instructions that require a DATIP-DATO sequence. The user has the option of strobing a single 16-bit word or two 8-bit bytes. A logic HIGH (binary ONE) loaded into a register bit activates the corresponding relay output. Each relay output has a jumper and split lugs which allow the user to insert contact filter circuits.

Data Strobe Outputs: Either of the register-loading input pulses will trigger the two DATA STROBE output circuits. One of these outputs is a transistor driver circuit capable of sinking 100 mA (clamped to +5 volts). If jumper W54 is removed, the user can switch up to 20 volts at this output.

The second DATA STROBE circuit contains a one-shot which drives a relay to provide a momentary contact closure. The one-shot has an internal potentiometer for pulse-width adjustment from 5 to 20 ms. External capacitance can be added to split lugs on the module to increase the contact closure time. Jumpers (W56 and W55) are provided which allow the user to choose whether the relay output will be energized on a HIGH or LOW logic level. Both DATA STROBE outputs are available at the 40-pin connector.

READY Relay and Level Inputs: When the interfaced device has received data, it can signal the M1801 that it is ready for another transfer by either energizing the READY relay or by applying a TTL low signal at pin TT of the edge connector J1. The relay has a 5-volt coil rating and pulls in at 4.2 volts. A jumper (W52) and split lugs are provided for users who want to add a voltage divider circuit.

The signal on pin TT must be in the form of a HIGH-to-LOW transition: must be HIGH for min. of 4 ms then go LOW for min. of 8 ms. Contact filtering (6.8 ms min.) is provided for either READY input to prevent false triggering due to contact bounce. The switch filter output sets the INTERRUPT flag, the output of which can be used to request an interrupt. Therefore, continuous interrupts can be made at 12 ms intervals. This timing relationship is shown in the following figure.



Flags: The INTERRUPT flag can be set by the READY signal from the external equipment. Interrupt capability is enabled by a second flag, INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags can be applied to an M7821 (or equivalent) for computer interrupt. The INTERRUPT flag is cleared by the register-loading signals from the M105; both flags are always cleared by computer power-ups.

Register Preset Jumpers: Each register bit on the M1801 has a jumper which causes that particular bit to clear on power-on. If the user wishes to have a particular bit set on power-on, he must remove the jumper provided and install the particular jumper which sets that bit. Care should be taken to insure that both the set and clear jumpers are not inserted simultaneously.

DATA Bit	Jumper to CLEAR	Jumper to SET
D00	W1	W2
D01	W3	W4
D02	W5	W6
D03	W7	W8
D04	W9	W10
D05	W11	W12
D06	W13	W14
D07	W15	W16
D08	W17	W18
D09	W19	W20
D10	W21	W22
D11	W23	W24
D12	W31	W32
D13	W29	W30
D14	W27	W28
D15	W25	W26

Status Gates: Status gates on the M1801 give the programmer the ability to check the states of hte INTERRUPT and INTERRUPT ENABLE flags. These gates are software-enabled through the address selector (M105).

CAUTION
When the high output voltage or current capabilities of the M1801 are used, the M1801 should be shielded from all computer circuitry.

SPECIFICATIONS
Relay Contact Ratings:

Voltage:	100 V max.
Current:	0.5 A max.
Power:	10 W max. resistive load
Insulation resistance:	1,000 megohms

Data Strobe Output:

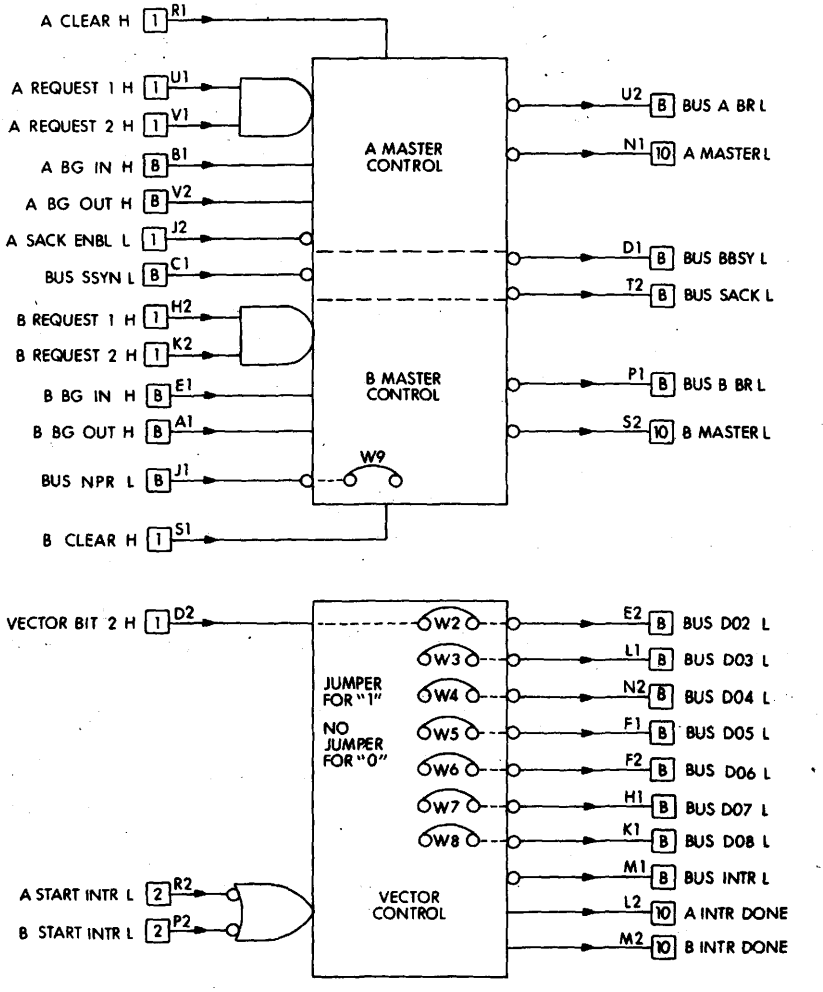
Current Sinking:	100 mA max.
Voltage:	20 V max.

M7821
INTERRUPT CONTROL MODULE

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	550	A2
GND		C2, T1

The M7821 Interrupt Control Module is used with the interface logic of a device in the PDP-11 systems. The M7821 allows one or two devices that request an interrupt to gain access to the UNIBUS and become bus master for one or more data transfers. It also provides a vector control circuit to enable the selection of an address in memory at which the device subroutine is stored.

The module consists of an A Master Control, B Master Control, and Vector Control logic. Either of the two master control circuits can be used to generate a Non-Processor Request (NPR) for direct data transfers to memory (DMA) or a Bus Request (BR) which interrupts the current processor program. The A Master Control, however, is normally used for generating the NPR and the B Master Control for the BR. When used as a DMA control, the A Master Control has the ability to perform a burst mode block transfer which allows more than one data cycle to be performed each time the device becomes bus master.

The B Master Control contains logic which can be implemented to allow the monitoring of the bus NPR line. This capability permits an NPR initiated by a device to be honored under certain conditions and the device to gain access to the bus even though a BR from another device has occurred prior to the NPR. A jumper lead can be removed from the module to disable this feature if the B half is used for NPR transfers.

The sequence of interrupt control signals between the M7821 and processor is similar for both the NPR and BR; however, an interrupt signal and vector address is generated after the device becomes master during a BR. The interrupt signal halts the operating program in the processor and the vector address specifies a location in memory where the starting address of the interrupt status routine and a status word is stored.

FUNCTION

The interrupt request generated by a device is received as a High level on either A REQUEST 1 or B REQUEST 1 input. The associated A REQUEST 2 and B REQUEST 2 inputs must be enabled with a High level to generate a bus request. A non-processor request is initiated by the A Master Control and the BUS A BR output is wired to the NPR bus line. The BUS A BR output becomes Low during the request interval. The processor responds to the NPR by issuing a high level to the A BG IN input. The A Master control issues a Low BUS SACK signal to the processor to acknowledge the A BG IN signal and the BUS BBSY signal is asserted Low as soon as the current bus master releases control of the bus to indicate the requesting device is bus master.

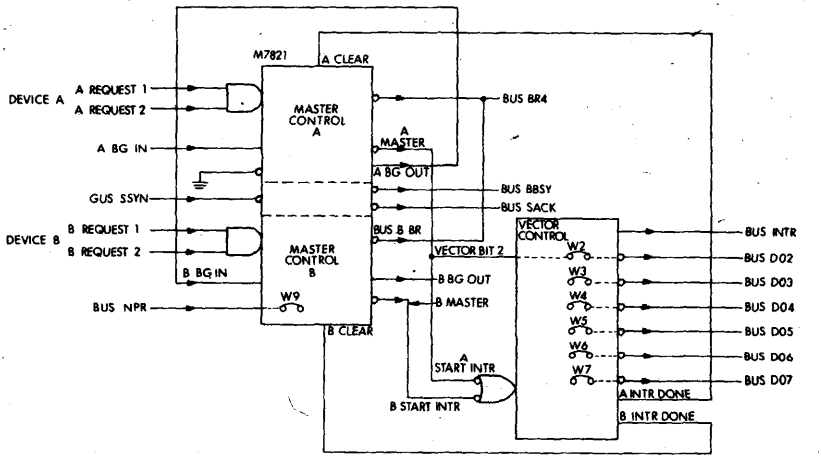
Normally, the BUS SACK signal is returned to a High level after BBSY becomes Low. If more than one data transfer (bus cycle) is required during the period that the device is bus master, the A SACK ENBL input can be connected to a level which remains High until just before the last bus cycle of the burst transfer is started. This level will prevent the processor from issuing a bus grant requesting device until the data transfers have been completed. This insures that the bus will be given to the highest priority requesting device at the end of the burst.

A bus request (BR) is issued by the B Master Control in a similar manner as the NPR. The BUS B BR output of the B Master Control connects to the assigned bus request priority line, BR4 through BR7. After the A Master Control issues a Low to the BUS BBSY line, the vector logic issues a Low BUS INTR signal to the bus interrupt line and transmits the vector address,

as preset by the jumper leads W2 through W7, to the data bus lines BUS D03 through D08. The data from the device which initiated the interrupt request is transferred to memory after the BUS BBSY has been issued by the processor.

APPLICATION

The following diagram shows a typical wiring configuration of the M7821 module. An interrupt request can be initiated from Device A to the A Master Control or by Device B to the B Master Control. The outputs of both master controls can be wired together as shown and connected to the BUS BR4 line; therefore, an interrupt request from either Device A or B will initiate a bus request at the same priority level. The A SACK ENBL input is connected to ground indicating that only one data transfer will be performed each time the device becomes bus master. The bus grant (A BG OUT) connects to the bus grant (B BG IN) where both master controls are connected to the same priority level of bus requests (BUS BR4).



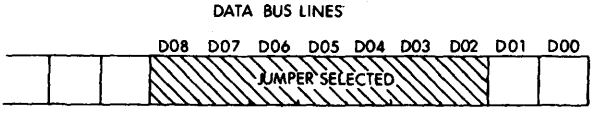
TYPICAL M7821 APPLICATION

All jumpers W2 through W7 are connected on the Vector Control section of the module. The A MASTER output connects to the VECTOR 2 input of the Vector Control circuit. When the A Master Control section of the module becomes bus master, the A MASTER output will be low and the resulting vector address on lines BUS D02 through BUS D08 will contain an octal 370. If the B Master Control is selected, the A MASTER output will be high, producing a vector address of an octal 374. The A MASTER output and the B MASTER output connect to the START INTR inputs of the Vector Control

or gate to initiate the interrupt request on the BUS INTR line. When the data transfer is complete, the INT DONE output of the Vector Control will clear the appropriate master control section previously selected.

WIRING CONFIGURATION

During a BR, the vector address is specified by the information on lines BUS D02 through BUS D08. The address format is indicated below:



JUMPERS	ADDRESS BITS
W2	D02*
W3	D03
W4	D04
W5	D05
W6	D06
W7	D07
W8	D08

*CONTROLLED BY VECTOR BIT 2 INPUT

When a jumper is present between the designated lugs W3 through W8 on the module, a logic ONE will result and when the jumper is removed, a logic ZERO will be present on the corresponding vector address bit. With jumper W2 installed, the state of address bit D02 is determined by the logic level present on the VECTOR BIT 2 input.

Jumper W9 is installed during manufacturing and must be removed when used with early PDP-11/15 and PDP-11/20 without the KH11 option.

M7821 SIGNALS

Inputs (X = A or B Master Controls)

X REQUEST 1 H, X REQUEST 2 H — Both signals must be asserted High to initiate a BR or NPR and remain High until the requesting device is through being bus master. Lowering either of these lines will cause BBSY to be removed. Prior to a new bus request, one signal must become Low before being reasserted.

X BG IN H — Asserted High by the processor in response to a request when the requesting device has the highest priority.

X SACK ENBL L — Connect to ground (Low) when only one data transfer by a device will be performed each time the device becomes bus master. When a burst mode block transfer is done, this line should be held High until just before the last transfer of the block.

BUS NPR L	With jumper W9 connected, a Low on the BUS NPR line from the processor will prevent the B Master Control from transferring a bus grant to another requesting device. Remove this jumper if this section is used for an NPR device.
X CLEAR H	A High transition causes the associated master control to remove the BUS BBSY signal and terminate bus mastership.
VECTOR BIT 2 H	A High input specifies an octal 4 in the least significant digit of the vector address. A Low specifies an octal 0.
X START INT L	A Low transition initiates an interrupt by loading the vector address onto the UNIBUS and producing a (Low) BUS INTR signal.

Outputs

BUS X BR L	Asserted Low when X REQUEST 1 and X REQUEST 2 are asserted to indicate that a device has initiated a BR or NPR. Connect to desired UNIBUS BR or NPR line.
X BG OUT H	Asserted High to transmit the bus grant to the next device on the same priority level.
BUS SACK L	Asserted Low to acknowledge to the processor that the requesting device has received the grant signal and is prepared to become the bus master when the current master releases the BUS BBSY signal.
BUS BBSY L	Asserted Low to indicate that the requesting device is bus master.
X MASTER L	Asserted Low when the associated master control has become bus master.
X INT DONE H	Asserted High at the completion of the interrupt (when BUS SSYN is received).
BUS D02—D08L	Specifies the vector address to the UNIBUS.
BUS INTR L	Asserted Low by the requesting device after it has become bus master to notify the processor that the data lines contain a vector address.

DECkit11-D

This kit is designed specifically for the PDP-11 owner who requires high I/O data transfer rates. Full 16-bit data words can be transferred between the PDP-11 memory and an external device at UNIBUS speeds. See Figure The DECkit11-D interface kit is physically and electronically compatible with all PDP-11 Family computers.

Parallel digital data is cabled directly to and from the interface kit; no additional logic or hardware is required to handle TTL-compatible data. External devices, such as lab instruments, mass storage units, displays, pre-processors, and other CPUs can communicate conveniently with the PDP-11 memory.

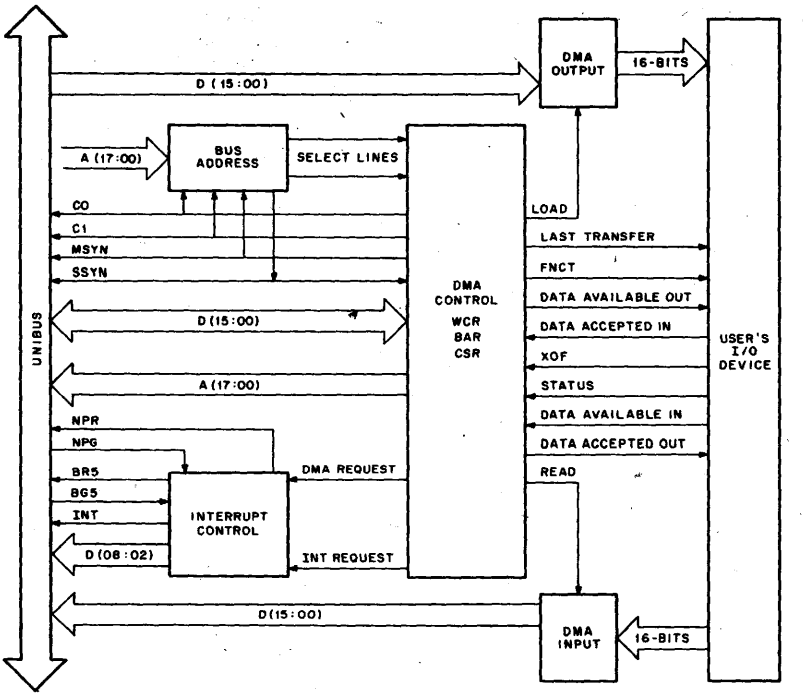
The prewired backplane includes five unused module slots that can be used for custom logic such as level shifters and counters. Even modules for simple processing logic can be utilized in these unused slots. Figure 2 is a module utilization diagram of a DECkit11-D.

DECkit11-D is valuable to the OEM and the end-user. The predesigned interface concept frees the system designer from the complex problems usually associated with UNIBUS interfacing and the end-user has available the flexibility and speed of the UNIBUS for data transfers.

SPECIFICATIONS

Transfer Types:	Direct Memory Access (DMA) via NPR programmed control
Data input to PDP-11 memory:	16-bit word Parallel TTL-compatible Up to 100 ft I/O cable Up to ½ million words/second*
Data output from PDP-11 memory:	16-bit word Parallel TTL-compatible, high-drive capability Up to 100 ft I/O cable Up to 2/5 million words/second*
Control and Status:	16-bit Control and Status Register (CSR) Handshaking control signals— Data Available Out Data Available In Data Accepted Out Data Accepted In Last Transfer External Overflow Status signals—Function/Out Status/In
Interrupts:	Word count overflow Nonexistent memory External overflow Input demand } Set by Priority Interrupt Plug; shipped at level 5. Interrupt enable/disable—CSR bit 06
Register assignments:	Word Count Register (WCR) 76xxx0** Bus Address Register (BAR) 76xxx2** Control and Status Register (CSR) 76xxx4** Data Buffer Register (DBR) 76xxx6**
I/O connection:	Several stranded cables available (BC08R, BC08S)
Power:	+5V, ±5% @ 3 A; normally available from system power supplies
Size:	One system unit
Weight:	4½ pounds (approximately)

* Depending on memory and other options chosen.
** User-selectable addresses.



* A17 and A16 are not used for data transfers. This implies that only the first 32K of a PDP-11 memory may be addressed.

Figure 1 DECkit11-D Block Diagram

Row / Slot	A	B	C	D	E	F
04	UNIBUS OUT		SPARE			
03	G772 POWER	M796	M7219			
02		M7821	M205	M116	M113	M112
01	UNIBUS IN		M660	M9100	M1502	

Figure 2 . DECkit11-D Module Utilization Diagram (Pin Side)

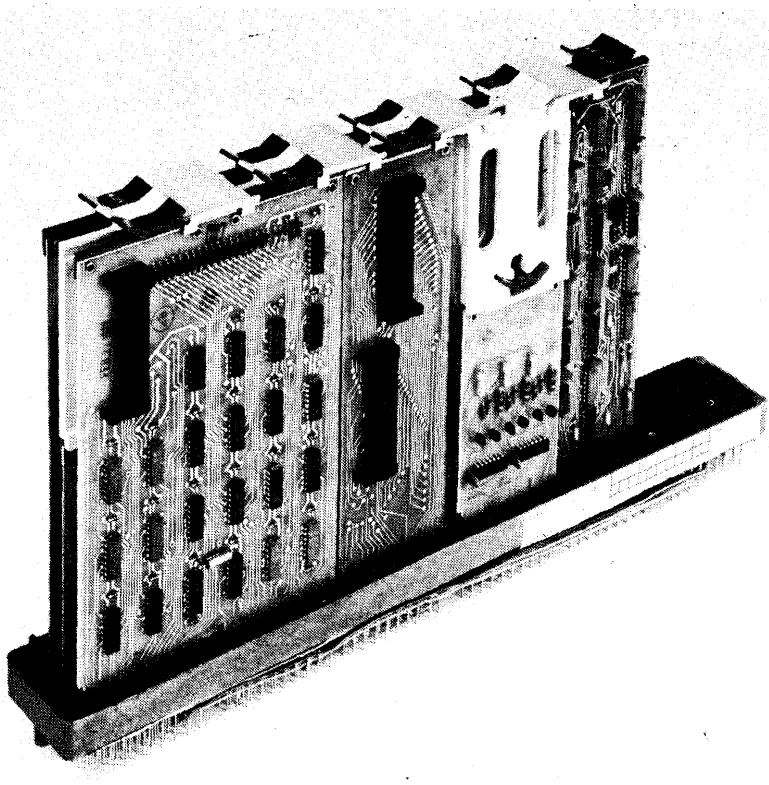
If mounting space is available in the existing PDP-11 processor mounting box, the DECkit can be installed there and jumpered to the existing panels by a UNIBUS Connector Module, M920. Power is supplied from the processor power supply, or from an additional H720 C or D Power Supply.

If the Interface Kit is installed in a separate mounting rack, the UNIBUS is extended to that rack with a BC11A cable. This cable is available in various standard lengths from 2 ft to 35 ft.

Input/Output Cables

Type	Connectors
BC08R-XX[1]	H856 to H856[2]
BC04Z-XX[1]	H856 to open-ended[2]
BC07A-XX[1]	H856 to open-ended[2]
BC07D-XX[1]	H856 to open-ended[2]

Notes: 1. XX is length in feet
2. H856 is a female connector



DECkit11-D

INTEGRATED CIRCUITS (ICs)
Two, 956 and 957, special ICs are available from Digital Equipment Corporation.

DEC8640 Unibus Receiver IC (Quad 2-Input NOR Gates)—956
The 956 is a package of ten 14-pin, dual-in-line package (DIP) DEC8640* integrated circuits (ICs). Each IC comprises four 2-input NOR gates. Each gate performs the Boolean function $X = A + B$. The DEC8640 gates are especially suitable as Unibus receivers because of their high impedance characteristics and, hence, minimal loading on the bus.

These NOR gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

DEC8881-1 Unibus Driver IC (Quad 2-Input NAND Gates)—957
The 957 is a package often 14-pin, dual-in-line package (DIP) DEC8881-1 integrated circuits (ICs). Each IC comprises four 2-input NAND gates. Each gate performs the Boolean function $X = AB$. The DEC8881-1 ICs are especially suitable as Unibus drivers because of their capability to sink 70 mA with a collector voltage of less than 0.8 V.

These NAND gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

*DEC8640 IC replaces DEC380 IC.

M7800 SINGLE ASYNCHRONOUS SERIAL LINE INTERFACES

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

DESCRIPTION

The M7800 is a highly-versatile single asynchronous serial line interface module. It formats and controls the transfer of data between the parallel PDP-11 UNIBUS and serial external devices. The module can be configured to interface with either 20 mA current loop devices (e.g., models LT33 and LT35 Teletypewriter, LA36 DECWRITER, display terminals) or EIA RS-232-C devices (e.g., EIA terminals or modems). The interface operates in either full or half duplex mode and performs serial-to-parallel and parallel-to-serial conversion of the transmitted data. When receiving data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the UNIBUS. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the external device. The two data transfer units (receiver and transmitter) are independent and capable of simultaneous two-way communication. The receiver and transmitter each operate through a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or the external device.

The module is directly compatible with the PDP-11 UNIBUS and is designed for installation into any one of the available Small Peripheral Controller slots of the BB11-M, DD11-A or DD11-B Interfacing Unit and the PDP-11 processor unit. It represents one unit load on the UNIBUS.

Configuration of the M7800 for a specific device involves selection of an appropriate crystal, addition of an appropriate cable, and making certain jumper selections on the module. A 40-pin BERG connector is mounted on the edge of the module for connection to the external device. Data rates of 36.7 Baud to 9600 Baud can be handled, and jumper changes can provide for 5, 6, 7, or 8 data bits, even, odd, or no parity, and 1, 1.5, or 2 stop bits. A full description of module configuration is given in DL11 Asynchronous Line Interface User's Manual, Document EK-0L11-OP-001, available from your local sales office.

FUNCTION

The serial-to-parallel and parallel-to-serial conversion of the device data is performed by a Universal Asynchronous Receiver Transmitter (UART). The UART is a 40-pin dual-in-line package and includes the circuits to double buffer the characters in and out, select the character length and stop code configuration, and indicate status information pertaining to each character.

Receiver

The receiver section performs serial-to-parallel conversion of the 8-level codes. Each character appears right justified in the Receiver Data Buffer Register (RBUF), stripped of start, stop, and parity bits.

A complete character is formed in the UART and is transferred to the Receiver Data Buffer Register (RBUF) at the time the center of the first stop bit is sampled. At that time, the Receiver Done Bit (Bit 7) is set in the Receiver Status Register (RCSR). If the Receiver Interrupt Enable Bit (Bit 6) is also set in RCSR, an interrupt request is generated. The BR level is set by jumper plug. BR4 is standard.

The program then reads the RBUF. The character appears right justified in bits 7-0 of RBUF, stripped of start, stop, and parity. The program has a full character time to remove the completed character from RBUF before the next character.

Transmitter

The transmitter section performs parallel to serial conversion of data supplied to it from the UNIBUS. The character length and stop code are the same as for the receiver section. The transmitter section is also fully double buffered. Any time the Transmitter Ready Bit (bit 7) is set in the Transmitter Status Register (XCSR), the program may load the low-order eight bits of the Transmitted Data Buffer Register (XBUF) with a right justified data character. The Transmitter Ready Bit will be set any time the XBUF is available, whether or not a character is currently being transmitted. This is a result of the double buffering. If a character is not currently being transmitted and XBUF is empty, the program may provide two characters in succession (within less than one character time) to the transmitter.

As the first character is loaded, it is immediately transferred to the serializer register internal to the UART, and the Transmitter Ready Bit (bit 7) in XCSR is set again. If the Transmitter Interrupt Enable Bit (bit 6) is set in XCSR, an interrupt request will be generated any time the Transmitter Ready Bit (bit 7) is set. The BR level for the transmitter is the same as for the receiver.

The transmitter supplies the start bit and the proper number of stop bits.

Some Typical Applications

Figure 1 is a block diagram of an M7800 module configured to interface with a Teletype, while Figure 2 shows the module working with an EIA communications modem such as the Bell Model 103 or 202.

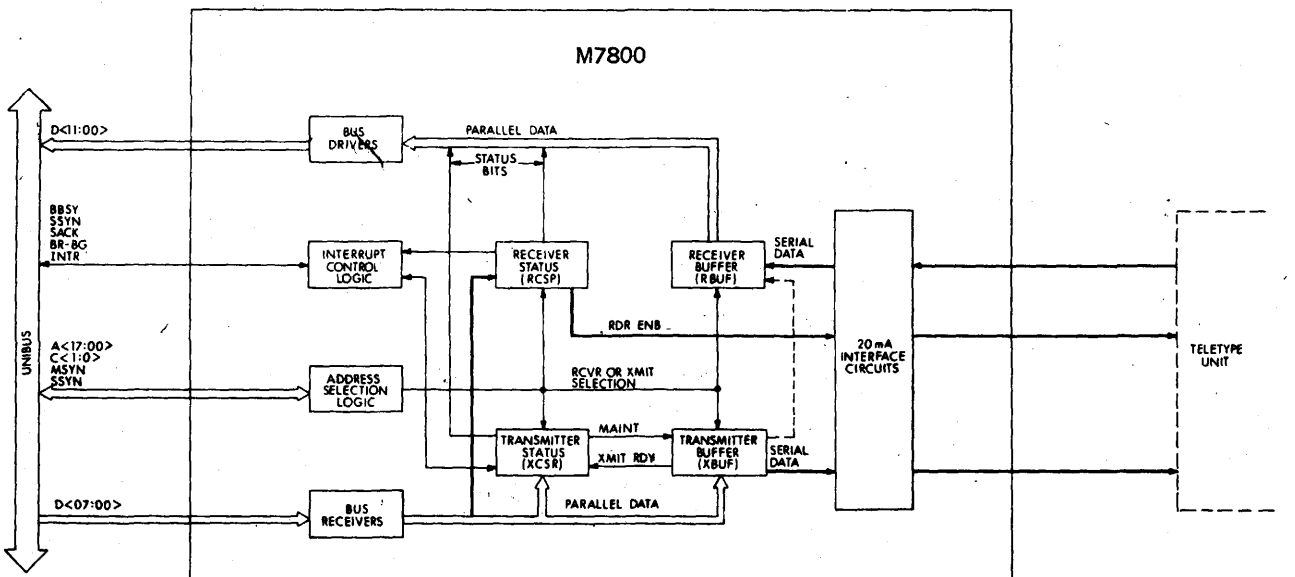


Figure 1 Block Diagram of M7800
Configured for 20 mA Current Loop Device

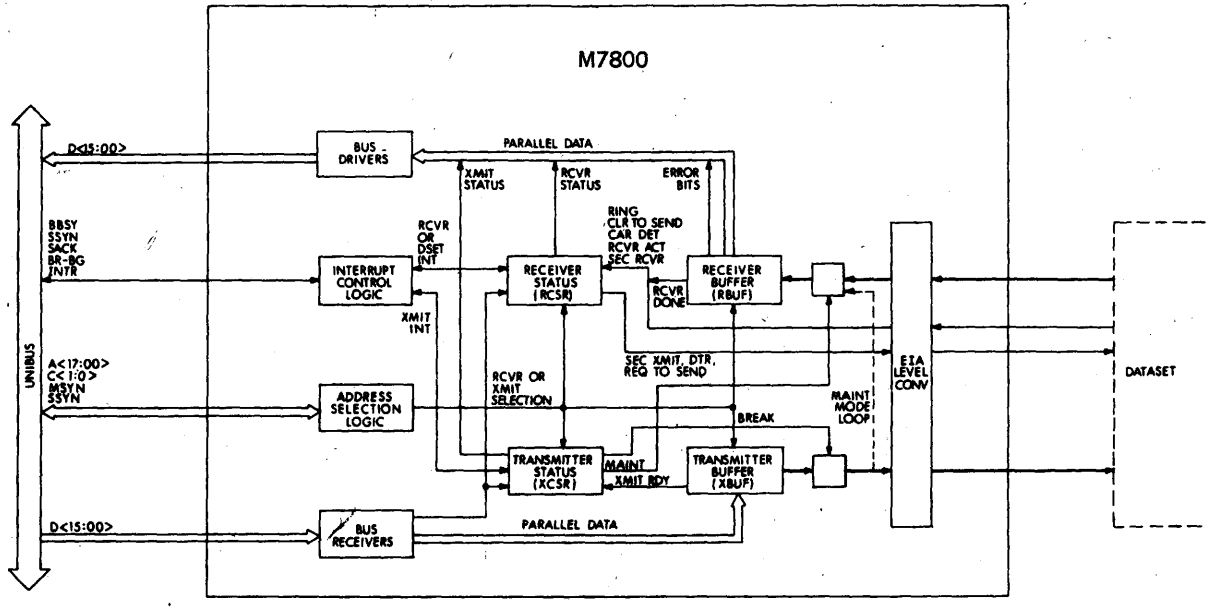


Figure 2 Block Diagram of M7800
Configured for EIA RS-232-C Device

Data Rates

The M7800 can operate over a wide range of standard data rates. The general range is determined by the crystal, which must be specified at the time of order. The specific rate, which can be different for receive and transmit if desired, is selected by the user via two rotary switches on the module. Table 1 lists the Baud rates available with the various crystals and switch settings.

Table 1 Baud Rates with Standard Crystals

Switch Position	Crystal #1 (844.8 kHz) 18-10245-01	Crystal #2 (1.03296 MHz) 18-05501-06	Crystal #3 (1.152 MHz) 18-05501-05	Crystal #4 (4.608 MHz) 18-05501-07
1	36.7	44.8	*50*	*200*
2	55	67.3	*75*	*300*
3	*110*	*134.5*	*150*	*600*
4	220	269	*300*	*1200*
5	440	538	*600*	*2400*
6	880	1076	*1200*	*4800*
7	1320	1614	*1800*	*7200*
8	1760	2152	*2400*	*9600*
9*	—	—	—	—
10*	—	—	—	—

*These switch positions are for external clock inputs and do not tap off the crystal oscillator.

NOTE: The baud rates in italics are the most commonly used.

PROGRAMMING

The interface between a program running in the PDP-11 processor and the M7800 is via four device registers: Receiver Status Register (RCSR); Receiver Data Buffer Register (RBUF); Transmitter Status Register (XCSR); and Transmitter Data Buffer Register (XBUF). Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction which references these addresses, with a few exceptions.

Detailed information on programming is contained in the DL11 Asynchronous Line Interface Users Manual, EK-DL11-OP-001, and in the Paper-Tape Software Programming Handbook, DEC-11-XPTSA-A-D.

GENERAL SPECIFICATIONS

Mechanical:	Consists of one quad module, extended length, single width.
Operating Mode:	Full or half duplex under program control.
Data Format:	Asynchronous, serial by bit. One start bit. One, 1.5, or two stop bits selectable by user. Even, odd, or no parity. A one (1) presented by the program to any bit in the Transmitted Data Register will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one (1) in the Received Data Register, and a Spacing condition will be presented as a zero (0).
Order of Bit Transmission:	Low order bit first.
Distortion:	The M7800 receiver will operate properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received data bits, and up to ± 4.5%, long-term speed distortion, provided the data format contains at least one and one-half stop units. If the data format contains only one stop unit, the speed tolerance is ± 4%. The M7800 transmitter operates with less than 3% bit-to-bit or long-term distortion.
Bus Loading:	One M7800 presents one unit load to the PDP-11 UNIBUS.
Electrical Interface:	M7800 provides a 20 mA active current loop for both send and receive leads for connection to local teleprinters such as the DIGITAL LA30-C and Teletype Models 33 and 35, and displays such as DIGITAL VT05 Terminal. It, by alternate selection of jumpers, provides a voltage level interface whose signal levels conform to Electronic Industries Association Standard RS-232-C and CCITT Recommendation V.24.
Power Requirements:	The M7800 requires 1.8 amps of + 5v., .05 amps of + 15v., and .15 amps of — 15v.

M7860
1-WORD INPUT/OUTPUT DEVICE INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

DESCRIPTION

The M7860 is a general-purpose interface between the PDP-11 UNIBUS and a user's peripheral. The M7860 provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device as shown on Figure 1.

It is directly compatible with the PDP-11 UNIBUS and is designed for installation into any one of the available Small Peripheral Controller slots (SPC) of a DD11-A, DD11-B or DD11-D System Interfacing Unit and the PDP-11 processor unit.

All data and control signals between the M7860 interface and device are TTL compatible.

The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions.

The M7860 interface module consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

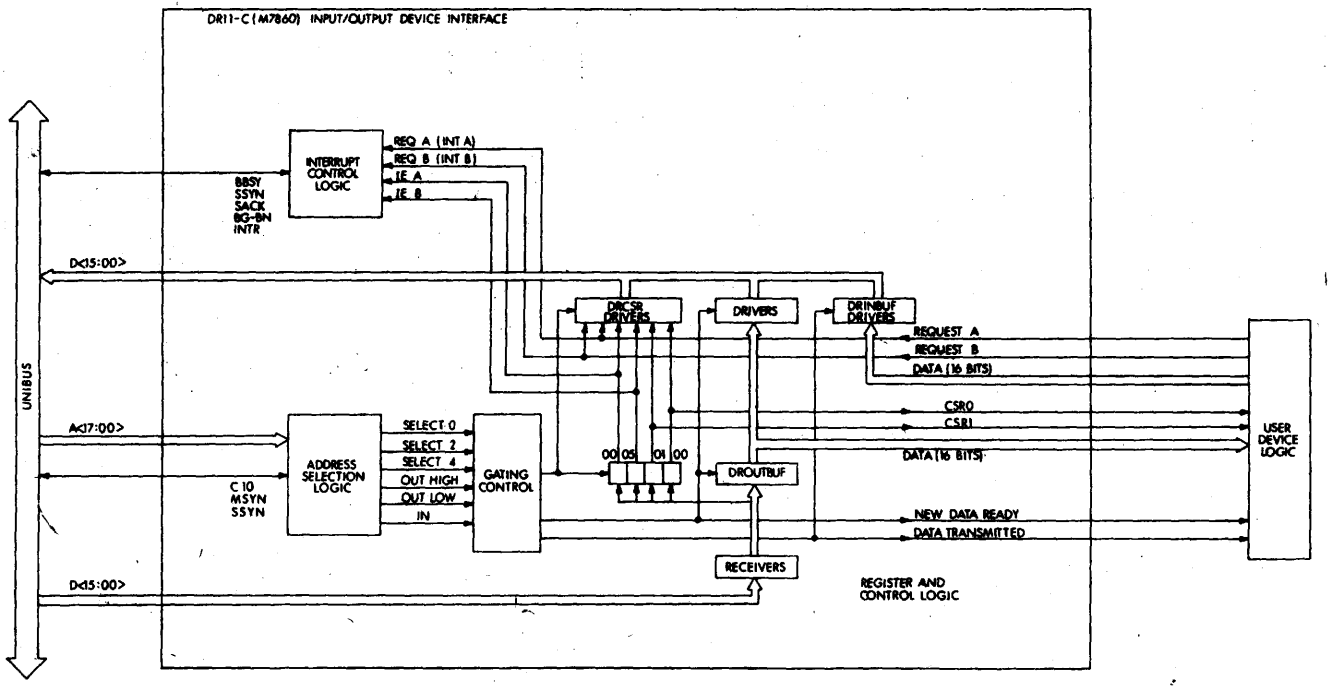
The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The M7860 interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the M7860 to specify the register and the type of operation to be performed.

The M7860 is designed for user applications and requires a minimum of external hardware to implement into the PDP-11 system. Two 40-pin connectors are conveniently mounted near the edge of the board. These connectors permit the external device to be easily connected using BC08R or BC04Z flat cables available from DIGITAL. These cables have the mating connectors premounted and are supplied in any specified length.

The interface module occupies one SPC slot and is a quad-height, extended length, single-width module.



M7860 Block Diagram

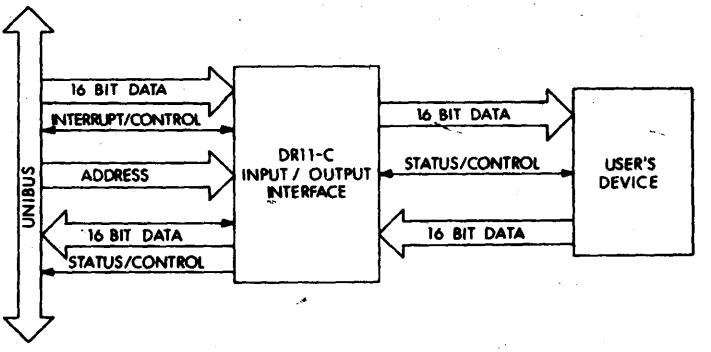


Figure 1 M7860 Interface

FUNCTION

If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, a NEW DATA READY control signal is supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

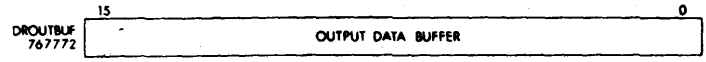
When an input operation is specified, the M7860 provides 16 lines of input to UNIBUS transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the maintenance mode, they are also used to check operation of the interface.

An optional maintenance cable, BC08R-1, permits checking of the M7860 logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The M7860 can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one M7860 connected to each processor bus and the two M7860s are cabled together, thereby permitting the two processors to communicate.

Output Buffer Register (DROUTBUF)—address selectable by user

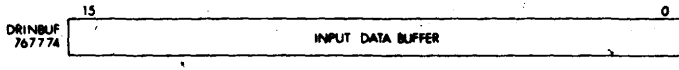


The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Information from the bus is loaded into this register under program control. At the time of loading, a pulsed signal (NEW DATA READY) is generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic. The DROUTBUF is cleared by INIT.

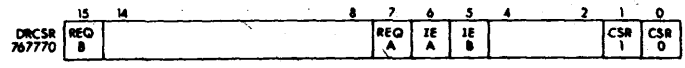
Input Buffer Register (DRINBUF)—address selectable by user



The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the UNIBUS. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the UNIBUS for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

Control and Status Register (DRCSR)—address selectable by user



The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT ENB (interrupt enable) bits which are under program control. Two other bits (CSR0 and CSR1) are controlled from the UNIBUS and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 7 for ready indications and both of these bits can generate interrupt requests. In addition, bit 0 is normally used for start or go commands.

INTERFACE SIGNALS

UNIBUS SIGNALS—The input and output data control, and status signals conform to the UNIBUS signal specifications outlined in the *PDP-11 Peripherals Handbook* published by Digital Equipment Corporation. The M7860 module presents no more than one unit load on any UNIBUS signal line.

DEVICE SIGNALS—Data and control signals are transferred between the devices and interface by two cables that attach to connectors J1 and J2. The location of the connectors on the module is shown on Figure 2. Table 1 lists the pin assignments of each connector and the signal drive or loading capability.

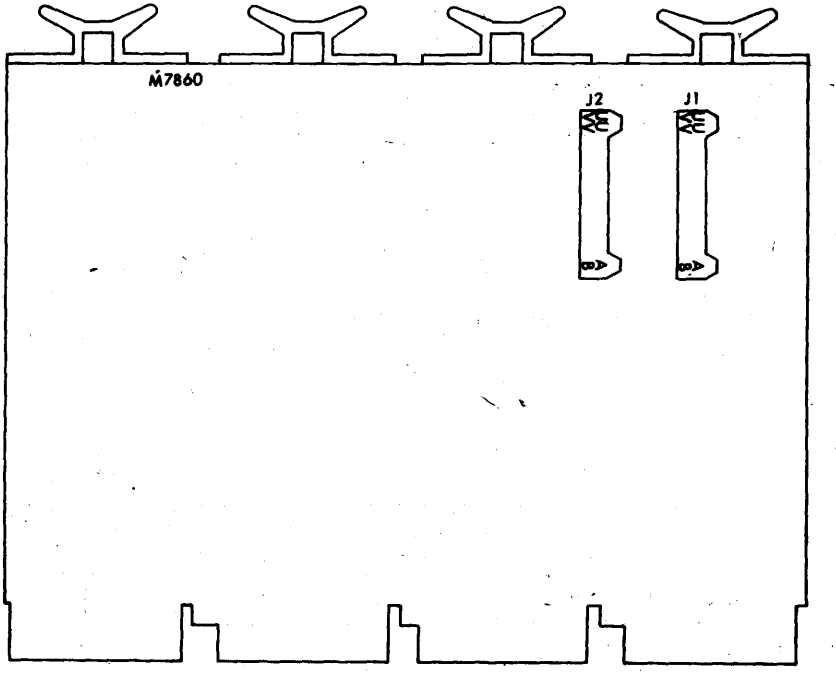


Figure 2 Connector Locations

Table 1
Input and Output Signals

Inputs			Outputs		
Signal	Connector	Pin*	Signal	Connector	Pin
IN00		TT	OUT00		C
IN01		LL	OUT01		K
IN02		H	OUT02		NN
IN03		BB	OUT03		U
IN04		KK	OUT04		L
IN05		HH	OUT05		N
IN06		EE	OUT06		R
IN07		CC	OUT07		T
IN08	J2	Z	OUT08	J1	W
IN09		Y	OUT09		X
IN10		W	OUT10		Z
IN11		V	OUT11		AA
IN12		U	OUT12		BB
IN13		P	OUT13		FF
IN14		N	OUT14		HH
IN15		M	OUT15		JJ
REQ A	J1	LL	NEW DATA DRY**		VV
REQ B	J2	S	DATA TRANS**	}	C
			CSR0	}	K
			CSR1	} J1	DD
			INIT	}	P
			INIT	J2	RR, NN

*Remaining pins on J1 and J2 are connected to logic GND on M7860.
**Pulse signals, approximately 400-ns wide. Width can be changed by user.

CABLE ASSEMBLIES—Several cable assemblies are available from DIGITAL for use with the M7860 module. Table 2 lists some of the recommended cable types and lengths available. Maximum allowable cable length for the M7860 is 25 feet.

Table 2

Cable No.	Connectors	Type	Standard Lengths (ft.)
BC07A-XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25

GENERAL SPECIFICATIONS

Device Data

Input/output levels: (user interface)	logic 1 = +3 V logic 0 = 0 V
Data Inputs:	16-bit word from the external device One standard TTL unit load; diode protection clamps to ground and +5V
Data Outputs:	16-bit word from the UNIBUS. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus. NEW DATA READY—drives 30 units, positive pulse, 400-ns wide unless width changed by an external capacitor. DATA TRANSMITTED—drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor. INIT (initialize)—common signal on both connectors driven by one 30 unit load driver.

UNIBUS Interface

Interrupt vector addresses:	floating, 2 needed for each M7860, selectable by user
Priority level:	BR5 (may be changed)
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot
Size:	quad module
Input Current:	1.5A at +5V (no current needed at −15V)

The M7860 is also available with the BC08R-1 maintenance cable and applicable documentation as the DR11-C.

TRADITIONAL MODULES

The modules described briefly in this section have been, for the most part, superseded by other products in this Handbook. They are presented here for reference purposes; detailed descriptions are contained in earlier editions of the Logic Handbook. Wherever possible, DIGITAL stocks and supports these older modules but, because of parts availability problems caused by state-of-the-art changes, some items may no longer be in production. Before ordering any of these modules, always check with the Logic Products Sales ordering any of these modules, always check with Logic Products Sales Support at DIGITAL Equipment Corporation, MK1-2/E13, Merrimack, NH 03054.

PDP-8 Non OMNIBUS

POSITIVE BUS

M101 Bus Data Interface
The M101 contains fifteen, two-input TTL NAND gates with input ground clamps arranged for convenient data strobing from the PDP8/I or PDP8/L positive bus.

M103 Device Selector
The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP-8/I and PDP-8/L.

M107 Device Selector
The M107 is a device selector which, by the use of extended decoding of the BMB lines 9 through 11, will provide seven discrete IOT pulses.

M108 Flag Module
The M108 contains three general-purpose clocked flip-flops for use in flag applications in I/O interfaces, etc. Gating is provided so that the flags can be individually set or gated to the program interrupt inputs of a positive-bus PDP-8 computer.

M623 Bus Driver
The M623 contains 12 two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. The output consists of an open collector NPN transistor.

M624 Bus Driver
The M624 contains 15 bus drivers intended for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L.

M730 Bus Interface
The M730 interface module provides extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer.

M732 Bus Interface
The M732 interface module provides extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer.

M734 I/O Bus Input Multiplexer
The M734 is a three-word multiplexer used for strobing 12-bit words on a positive voltage input bus, usually the input of the PDP-8/I or the PDP-8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector NPN transistors which allow these outputs to be directly connected to the bus.

M735 I/O Bus Transfer Register
The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

M736 Priority Interrupt Module
The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices.

M737 12-Bit Bus Receiver Interface
The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L.

M738 Counter/Buffer Interface
The M738 provides a 12-bit binary up-counter that can be read to the positive external I/O bus of a PDP-8/I or PDP-8/L. The counter can be cleared or present to a starting value by a jam transfer from an external device. When a count enable flag is set, the counter operates as an up-counter in response to external clock pulses. The content of the counter can be strobed to the I/O bus through data gates under program control.

M907 Diode Clamp Connector
The M907 is used to provide proper undershoot ground clamps for devices receiving PDP-8/I and PDP-8/L positive I/O bus signals that are not so protected.

NEGATIVE BUS

M051 Positive-to-Negative Logic Level Converter
The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and −3 volts.

M100 Bus Data Interface
The M100 Bus Data Interface contains fifteen circuits for convenient reception of data from the PDP-8, PDP-8/I negative voltage bus. It is pin compatible with the M101 Positive Bus Data Interface.

M102 Device Selector
The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative BMB bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs.

M502 High-Speed Negative Input Converter
The M502 contains two non-inverting high-speed signal converters which interface standard negative (—3 volts and ground) logic levels or pulses with M and K Series positive logic modules.

M506 Medium-Speed Negative Input Converter
The M506 contains six noninverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 ns to M and K Series positive logic levels of +3 volts and ground.

M632 Positive In/Negative Out Bus Driver
The M632 contains eight two-input AND gate bus drivers for convenient driving of the negative bus of the PDP-8/I or PDP-8/L.

M633 Negative Bus Driver
The M633 contains 12 bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/I. Each driver consists of an open collector PNP transistor. It is pin-compatible with the M623 positive voltage bus driver.

M650 Negative Output Converter
The M650 contains three noninverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 ns) of K and M Series to digital negative logic levels of —3 volts and ground.

M652 Negative Output Converter
The M652 contains two noninverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to digital negative logic levels of —3 volts and ground.

PDP-11 MODULES

M1621 DVM Data Input Interface
The M1621 is a PDP-11 interface module containing all the bus drivers and control logic needed to input TTL-level information from several types of digital voltmeters and multimeters. All inputs from the instruments enter a 40-pin cable connector mounted on the module.

M1623 Instrument Remote Control Interface
The M1623 is a PDP-11 interface module containing the bus receivers and control logic needed to remotely program several types of digital voltmeters and programmable power supplies. All outputs to the instrument are through a 40-pin cable connector mounted on the module.

PDP-15 MODULES

M500 Negative In/Positive Out Receiver
The M500 module is used to convert negative input signals to positive output signals. Each card contains eight converters and is pin compatible with the PDP-15 positive receiver card (M510).

M510 I/O Bus Receiver
The M510 is a positive input/output receiver card for use with the PDP-15. It contains 8 high-impedance input circuits of at least 27K ohms and input switching thresholds of about +1.5 V.

M622 8-Bit Positive I/O Bus Driver
The M622 contains 8 two-input AND gate bus drivers for convenient driving of the positive input bus of the PDP-15. The output consists of an open collector NPN transistor.

DECkits

DECkit11-H
The DECkit11-H, when fully configured, is capable of reading four 16-bit words from a peripheral device into a PDP-11. It is also capable of writing four 16-bit words, or eight 8-bit bytes, from a PDP-11 to a peripheral device. Each input word is supplied with an interrupt capability to signal the processor that the word should be read.

MICROCOMPUTER INTERFACING MODULES
LSI-11 SERIES COMPUTERS—
INTERFACING SELECTOR GUIDE

MICROCOMPUTER

LSI-11

This section describes the general characteristics of the LSI-11 Microcomputer—the newest in the popular DIGITAL PDP-11 computer family. Additional literature providing detailed information is available from your nearest DIGITAL sales office.

LSI technology enables DIGITAL to put an N-channel MOS central processor, 4096 (4K)-word random-access memory (RAM), vectored automatic interrupt logic, real-time clock input, and auto program start up logic, on one 8.5-by-10-inch printed-circuit board. On one board you get a versatile microcomputer—central processor, memory, and input/output bus port—micro in size and price, but mini in computing performance.

Features:

- A large, flexible instruction repertoire, including the 400-plus instructions of the basic PDP-11/40.
- A simplified, application-oriented bus structure for maximum ease in handling I/O and memory operations.
- Software and hardware training classes.
- Complete documentation, including user's programming, and maintenance manuals, Microcomputer handbook, product and option bulletins, configuration and installation guides.
- Off-the-shelf, plug-in interfaces.
- Off-the-shelf, plug-in core, RAM, and/or PROM/ROM expansion memories.
- Resident firmware debugging techniques and ASCII console routines.
- Operating system development on standard PDP-11/35, 11/40 or LSI-11.
- The unmatched resources of the DECUS user's library for PDP-11 application programs.

These tools give you complete flexibility in developing hardware and software. You can use the LSI-11 in its final, dedicated environment to optimize your system design under actual operating conditions or take advantage of the power, flexibility, and high-level programming languages available with large PDP-11/40 computers to reduce the time to develop your operating system.

PROCESSORS

Microcomputer module KD11-F

The 16-bit central processor functions are contained in four silicon gate N-channel metal oxide semiconductor (MOS), large-scale integration (LSI), integrated circuit chips. These chips provide all instructions, decoding, bus control, and arithmetic/logic unit functions of the processor. The central processor contains eight general registers which can serve as accumulators, index registers, autoincrement/autodecrement registers, or stack pointers.

4096-by-16 read/write MOS semiconductor memory is contained on the microcomputer module. This memory is composed of LSI dynamic random-access memory (RAM) chips that require little operating power, provide fast

access time, and are refreshed automatically by the processor's microcode, which is transparent to the user. A memory register on the KD11-F module addresses all onboard memory plus LSI-11 bus-compatible expansion memory up to 32K words or 64K bytes.

Multiplexed parallel I/O bus port -DMA operation. The LSI-11 bus is a high-speed, 38-line parallel bus containing data, address, control and synchronization lines. Sixteen lines are used for time multiplexing of data and addresses. All data and control lines are bidirectional, asynchronous, open-collector lines capable of providing a maximum parallel data transfer rate of 833K words per second under direct memory access operation.

Powerful PDP-11/40 basic instruction set. More than 400 powerful instructions make up the LSI-11's extensive basic instruction set. There are no separate memory, I/O or accumulator instructions. Thus the user can manipulate data in peripheral device registers as flexibly as in memory registers.

The basic operation code uses both single- and double-operand instructions for words or bytes, making it possible to perform such operations as adding, subtracting, or moving two operands in one step. This can reduce the number of instructions needed for many routines by as much as two-thirds. Much of the LSI-11's operating flexibility and processing power are derived from its wide variety of addressing techniques. Addressing can be direct, indirect, autoincrement, autodecrement, byte or word, indexing and stack-addressing. This flexibility means the LSI-11 can deal with data in the most efficient manner. The general registers can be used interchangeably as stack pointers, accumulators, and index registers. Address modification can be done directly in the general registers.

Extended instruction and floating-point instruction options provide fixed-point multiplication, division, and multiple shifting in single-precision arithmetic as well as floating-point addition, subtraction, multiplication and division.

Single-level, vectored, automatic priority interrupt provides for user-implementation of a priority-structured I/O interrupt system. Devices electrically closest to the microcomputer module receive highest priority, for either DMA or programmed I/O transfers. (DMA devices have a higher priority than programmed I/O devices). This structure allows nesting of interrupts to as many levels as there are devices connected to the LSI-11 bus. Upon receipt of an interrupt grant, the device directs the processor to an interrupt vector location which contains the starting address of the device interrupt service routine and the new processor status word.

Real-time clock input signal line functions as an external interrupt line. When connected to a frequency source, it can serve as a real-time processor interrupt. A jumper on the microcomputer module enables or disables this highest priority interrupt function.

Asynchronous operation of all system modules permits each to function at its highest possible speed.

Power fail/autostart provides jumper-selective restart through a power-up vector, a defined location, or an octal debugging technique (ODT) microcode.

ODT/ASCII console routine/bootstrap all are resident in microcode to provide automatic entry into the debugging mode, replacement of conventional programmers' panel lights and switches with any terminal device generating stan-

dard ASCII codes, and the ability to automatically commence operation through resident bootstrap routines.

8.5-by-10 inch board contains all of these features.

Microcomputer module KD11-J
Contains all the same features as the KD11-F except that it utilizes a 4K x 16 **core** memory. This microcomputer is contained on two 8.5" x 10" boards.

Microcomputer module KD11-R
Contains all the same features as the KD11-F except that Random Access Memory (RAM) size is increased to 16K. This microcomputer is contained on two 8.5" x 10" boards.

EXPANSION MEMORY MODULES

4K dynamic random-access memory—MSV11-B is a dual-size (8.5-by-5-inch) read/write memory module utilizing dynamic MOS semiconductor memory devices. The module capacity is 4096 words of 16 bits, with memory-select circuitry for operation on 4K address boundaries. Dynamic memory refresh is performed automatically every 1.67 milliseconds by microcode on the microcomputer module.

16K dynamic MOS memory—MSV11-CD is a quad-size (8.5-by-10-inch) read/write memory module with 16K words of 16 bits each. This module features 4K dynamic MOS technology, internal refresh, 4K bank memory addresses, and 750 nanosecond cycle time with 390 nanosecond access time. There are no special power requirements and memory contents can be protected in the event of a power loss by user-implemented battery back-up power source.

4K programmable read-only memory—MRV11-AA is a dual-size (8.5-by-5-inch) field programmable, read-only module utilizing either 256 x 4 or 512 x 4 fusible-link semiconductor devices. The module's maximum capacity is 2048 or 4096 words 16 bits (depending upon which device is used), and is expandable in 256- or 512-word increments. This module is configured with 32 sockets for mounting memory IC devices of the user's choice. PROM chips can be supplied as an option. A pin-compatible masked ROM chips is available for volume applications so that the lowest possible cost can be achieved. Board-mounted jumpers enable selection of the module's address.

4K core memory module—MMV11-A is a quad-size (8.5-by-10-inch) core, read/write memory module containing 4096 words of 16 bits, with memory address selection circuitry for starting operation on any 4K boundary. Core memory provides non-volatile read/write storage for applications requiring protection against power losses.

LSI-11 INTERFACING MODULES

Table 1 summarizes the interfaces and related modules that are described in detail on the following pages or in the DIGITAL Direct Sales Catalog where noted.

Although each interfacing problem is likely to have some unique aspects, the steps to follow in general are:

1. Determine your interfacing requirements.
2. Match these requirements against the products listed in Table 1, then read the detailed descriptions.
3. Select suitable products if any are listed. If no listed products meet your requirements, contact your DIGITAL Field Sales office to find if any other DIGITAL products can perform the needed functions.
4. Add the power and mounting space requirements of all modules to be employed, and note the cables needed plus any prerequisites and restrictions that apply.
5. From the appropriate sections of this Handbook and the Hardware/Accessories Catalog, select the cables, power supplies, and mounting hardware to complete your system.

If you need technical assistance with any product in this Handbook, feel free to call DIGITAL's toll-free Hot Line, 8:30AM to 5:00 PM Eastern time, 800-258-1710. From New Hampshire locations or places outside the United States, call Merrimack, 603-884-6660.

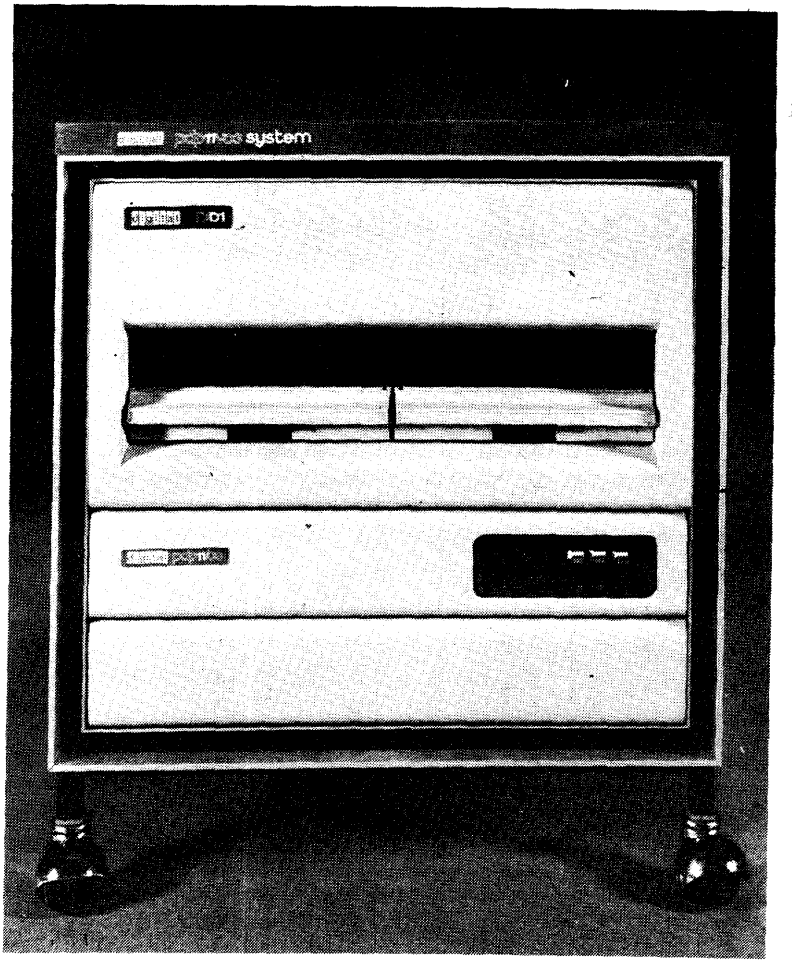
Table 1 Interface Selector Guide—LSI-11 BUS

DEVICE OR FUNCTION	MODULE OR OPTION	LOGIC H'BOOK PAGE[3]	POWER +5V AMPS[1]	POWER +12V AMPS	AC BUS LOAD	DC BUS LOAD	MODULE SIZE L H W[2]	CABLE REQ'D	COMMENTS
EIA RS232C serial devices, e.g.: LA35 printer LA36 printer terminal LA180 printer LS120 printer terminal VT52 CRT terminal VT55 CRT terminal	DLV11		1.6	.25	2.48	1	E D S	BC05C	
20 mA current loop serial devices, e.g.: LA35 printer LA36 printer terminal LA180 printer VT50 CRT terminal VT52 CRT terminal VT55 CRT terminal	DLV11		1.6	.25	2.48	1	E D S	BC05M	
Modem	DLV11-E		1.0	.2	1.65	1	E D S	BC05C	Supports EIA signals for modem.
A/D converter, 16-channel	ADV11-A		2.0	.45	3.25	1	E Q S	BC04Z	
D/A converter, 4-channel	AAV11-A		2.0	.45	1.91	1	E Q S	BC04Z	
Power fail/line time clock generator Same, with 120-ohm termination resistor	KPV11-A KPV11-B		.56	—	1.63	1	E D S	70-08612	Cable listed is for use with console front panel. 24V transformer required.
Real time clock, crystal controlled	KWV11-A		1.75	.01	3.41	1	E Q S	BC08R	
1-word parallel input interface 1-word parallel output interface 1-word parallel input/output interface	DRV11		.90	—	2.80	1	E D S	BC07D	Has separate input and output channels.
IEEE 488/1975 instrument bus	IBV11-A		1.5	—	1.77	1	E D S	BN11A-04 supplied	Cable BN01A-04 must be ordered for each instrument beyond the first.
Interface foundation module	DRV11-P		1 +	—	2.08	1	E Q S	BC04Z, BC07D, or BC08R	Can accept up to about 50 user ICs.
Direct Memory Access (DMA) interface	DRV11-B		1.9	—	3.30	1	E Q S	BC04Z	

Table 1 Interface Selector Guide—LSI-11 BUS (cont.)

DEVICE OR FUNCTION	MODULE OR OPTION	LOGIC H'BOOK PAGE[2]	POWER +5V AMPS[1]	POWER +12V AMPS	AC BUS LOAD	DC BUS LOAD	MODULE SIZE L H W[2]	CABLE REQ'D	COMMENTS
Designer's program control CHIPKIT	DCK11-AC		.74+	—	—	—	E D S	BC07D-10 supplied	
Designer's DMA CHIPKIT	DCK11-AD		1.22+	—	—	—	E D S	BC07D-10 supplied	CHECK WITH LOGIC PRODUCTS SALES SUPPORT BEFORE ORDERING!
Wire-wrappable modules:									
Quad-height, no IC sockets	W9511		—	—	—	—	E Q S		
Quad-height, 58 16-pin IC sockets	W9514		—	—	—	—	E Q S		
Double-height, no IC sockets	W9512		—	—	—	—	E D S		
Double-height, 25 16-pin IC sockets	W9515		—	—	—	—	E D S		

NOTES:
1. + means current required by user logic must be added to figure shown.
2. Module sizes are given as Length, Height, and Width, as defined in General Information.
3. DSC = Direct Sales Catalog.



INTERFACING MODULES

Serial line unit—DLV11 is a universal asynchronous receiver/transmitter serial interface module for use between the LSI-11 bus and serial devices. It is a dual-size (8.5-by-5-inch) module with the following features:

- Either optically isolated 20mA current loop or EIA interface.
- Selectable baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600.
- Jumper-selectable stop bits and data bits.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.

- Interrupt priority determined by electrical position along the LSI-11 bus.
- Control/status register (CSR) compatible with PDP-11 software routines. CSRs and receiver data buffer registers directly accessed via processor instructions.
- Plug, signal, and program compatible with PDP-11 DL 11-C.

Parallel line unit—DRV11 is a general-purpose, 16-bit parallel interface between the LSI-11 bus and the user's peripheral device. It is a dual-size (8.5-by-5-inch) module with the following features:

- 16 diode-clamped data input lines.
- 16 latched output lines.
- 16-bit word or 8-bit byte data transfers.
- Complete device address decoding user-assigned.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.
- Interrupt priority determined by electrical position along the LSI-11 bus.
- Control/status registers (CSR) compatible with PDP-11 software routines. CSR and receiver data buffer registers directly accessed via processor instructions.
- Plug, signal, and program compatible with PDP-11 DR11-C.
- Four control lines available to the peripheral device for output data ready, output data accepted, input data ready, and input data accepted logic operations.
- Can be used with TTL or DTL logic-compatible devices.
- Maximum data transfer rate of 90K words per second under program control.
- Maximum drive capability of 25 feet of cable.

Digital-to-Aanalog Converter—AAV11-A
The AAV11-A is a four-channel digital-to-analog converter that allows the user a wide variety of output voltage ranges that are jumper selectable. Each 12-bit D/A converter has its own holding register which can be separately addressed and can be written and read in either word or byte format.

AAV11-A Specifications

Packaging	one quad (10⅜" x 8.5") module
Number of D/A converters	4
Digital input	12 bits (binary encoded for unipolar mode; offset binary encoded for bipolar mode)
Digital storage	read-write, word or byte operable, single buffered
Output voltage range (jumper selected)	± 2.56V, ± 5.12V, ± 10.24V bipolar, OV to + 5.12V, OV to + 10.24V unipolar
Resolution	12 bits (1 part in 4096)
Gain accuracy	adjustable (factory set for bipolar ± 5.12V)
Gain temperature coefficient	10 ppm per degree C, max.
Offset temperature coefficient	20 ppm of full scale degree C, max.

Linearity	± ½ LSB max. non-linearity ± ½ LSB monotonic
Output impedance	1 ohm max.
Drive capability	± 6 mA max. per converter
Slewing speed	5V micro sec.
Power requirements	5V ± 5% @ 1.5A 12V ± 5% @ 0.4A

Bus load = 1

Analog-to-Digital Converter—ADV11-A

The ADV11-A is a 12-bit analog-to-digital converter with built-in multiplexer and sample-and-hold that allows the user the availability of 16 channels of A/D single-ended or 8 quasi-differential inputs and will convert an analog voltage from ±5.12V full scale bipolar.

The ADV11-A features a buffer register that allows data from one conversion to be transferred to the processor after a subsequent conversion begins. This buffering optimizes the throughput rate of the converter, enabling the ADV11-A to run at 25 KHz* throughput to memory. The auto-zeroing technique—another feature—uses a patented design that measures the sampled signal with respect to the offset of its own internal circuitry and thus effectively cancels out its own offset error contributions to the measurement. There are also three built-in signals for self-testing; they may be connected through a wrap-around BERG connector to any channel. The test signals are two d.c. levels, and one bipolar triangular waveform. The bipolar triangular wave can be used with diagnostic software to produce a data base for extremely thorough and precise analog linearity testing.

ADV11-A Specifications

Packaging	one quad (10⅜" x 8.5") module
Input voltage range	± 5.12V bipolar (full scale)
Resolution	12 bits (1 part in 4096)
Number of channels	16 single-ended, or 8 quasi-differential
Input impedence	100 megohms minimum
Input bias current	100 nA, maximum
Temperature stability	gain = 5ppm per degree C linearity = 2ppm of full-scale range per degree C
Throughput	25 KHz*
Data acquisition time	40 micro sec.
Power consumption	+ 5V d.c. ± 5% @ 1.75A + 12V d.c. ± 5% @ 350 mA

Bus load = 1

*Using an LSI-11 system under optimum programming and DMA refresh.

Real Time Clock—KWV11-A

The KWV11-A is a programmable real-time clock that offers the user several methods for measuring and counting intervals or events from 1 micro second to 650 seconds. It can also be used to synchronize external equipment to the processor. The KWV11-A is a 16-bit clock that will operate in one of four

programmable modes and can be selected to operate at one of five crystal-controlled frequencies.

KWV11 A Specifications

Packaging	one quad (10⅜" x 8.5") module
Programmable modes	single interval, repeated interval external event timing, external event timing from zero base.
Crystal controlled frequency	1 MHz, 100 KHz, 10 KHz, 100 Hz frequency
Accuracy	0.01%
Power requirements	+ 5V d.c. ± 5% @ 1.75 amps + 12V d.c. ± 5% @ 10 mA

Bus load = 1

NOTE

Detailed descriptions for LSI-11 options for DMA, power fail line clock generator, and LSI-11 bus foundation module are included at the end of this Microcomputer section.

HARDWARE/ACCESSORIES

Backplane Options

Two backplane options are available: the H9270 and the DDV11-B. The H9270 is a four-by-four slot LSI-11 bus-structured backplane/card guide assembly. It can accept the processor module and up to six options. Power is applied to the backplane via a screw-terminal block located on one end of the assembly.

The DDV11-B is an expanded version of the standard LSI-11 backplane (the H9270) for use when additional LSI-11 option module space and/or custom wire wrap space is required. A nine-by-four slot section of this backplane is LSI-11 bus-structured and will accept the processor module, up to 15 option modules, and one TEV11 bus terminator module. An additional nine-by-two slot section of the backplane is provided with power connections (+5 Vdc, ±12 Vdc, and ground), only; wire wrap pins allow the user to interconnect the slots with appropriate signals.

An optional card cage, type H0341, is available for use with the DDV11-B backplane. It provides physical protection to modules and serves as a card guide. The card cage completely surrounds the DDV11-B on the module side of the backplane.

Expander Box H909-C

The H909-C expander box provides a most convenient means for expanding the LSI-11 system. Each box includes the card guide and space for the DDV11-B and the power supply.

NOTE

Detailed descriptions of the above items (DDV11-B and H909-C) are contained in the HARDWARE/POWER SUPPLIES section of this Handbook.

Bus Accessory Options

Several LSI-11 bus accessory options are available for bus expansion, bus

termination, DMA refresh, bootstrap ROM, and combinations of the preceding. A summary of the options is provided below:

Module No.	Includes	System Functions
REV11-A	M9400-YA Module	120 Ω bus terminator, DMA refresh, bootstrap ROM.
REV11-C	M9400-YC Module	DMA refresh, bootstrap ROM.
TEV-11	M9400-YB Module	120 Ω bus terminator.
BCV1A-XX	Two BC05L-XX cables, one M9400-YD module, and one M9401 module.	Bus expansion: two expansion cables and two backplane connector modules (M9400-YD and M9401). Normally used for expansion from second to third backplane in 3-backplane systems. (A TEV11 or REV11-A 120 Ω terminator must be installed in the last device slot in backplane 3.)
BCV1B-XX	Two BC05L-XX cables, one M9400-YE module, and one M9401 module.	Bus expansion: 250 Ω terminator (M9400-YE), two expansion cables, backplane connector (M9401). Normally used for expansion from first to second backplane in 2 or 3 backplane systems.

NOTE

The -XX in BCV1A-XX and BCV1B-XX options denotes cable lengths. Options are available with cable lengths of 2, 4, 6, and 10 ft. For example, a BCV1A-06 includes two 6-ft cables. When the BCV1A and BCV1B options are used in a three backplane system their lengths should differ by 4 ft. so that any transients will occur on the cables and not on the backplane.

The REV11-A and REV11-C options contain programs stored in the ROM. These programs include processor and memory diagnostics, bootstrap programs for the RV11 floppy disk system, and absolute loader programs for paper tape readers.

TEV11 (or REV11-A), BCV1A, and BCV1B options are used for system expansion in multiple backplane systems. In addition, the REV11-A or TEV11 can be used to terminate the DDV11-B backplane (required when more than six option modules are installed on the backplane).

LSI-11 SOFTWARE

The LSI-11 software consists of a paper tape software (QJV10-AB) operating package available with the LSI-11 as a basic utility package and an Editor, which allows the user to create and modify ASCII source files to be used as input to other system programs; an Assembler, which allows the user to translate assembly language programs into executable machine-coded programs; a Loader, which allows the user to input programs and data from various media into the machine; an On-line Debugging Technique (ODT) Package, which allows the user to debug assembled and linked programs; an

Input/Output Executive, which allows the user to control the flow of data to and from devices under program control.

LSI-11 Systems Software include a paper tape software operating package, a variety of operation systems, programming languages, diagnostic software, paper tape software and special software options.

Real-Time Operating System RT-11
RT-11 is a floppy disk based, single-user, foreground/background system that can support a real-time job execution in the foreground and an interactive or batch program development job in the background. It is a high performance system which combines fast, on-line access with high level programming language capabilities and user-beneficial features such as stack processing and vectored interrupts.

Resource-Sharing Operating System RSX-11S
RSX-11S is an execute-only operating system designed to provide the most efficient resource-sharing environment for multiple real-time activities without a mass storage device. This operating system features multi-programming, priority scheduling, contingency exist, and power-fail shut-down and auto-restart.

RT-11 Programming Languages
MACRO-11, the assembler, provides full macro programming capabilities in systems with 8K of memory. It has facilities for maintaining and using a macro library and performing conditional assembly.

Multi-user BASIC is a fast incremental compiler developed by DIGITAL using a conversational programming language developed at Dartmouth. It provides on-line time-shared access to the LSI-11. Several users simultaneously can develop programs, enter and retrieve data, examine files, and communicate. It is one of the easier programming aids to master, yet it offers extremely sophisticated techniques for complex manipulations and efficient problem-solving.

FORTRAN-IV is an updated, improved version of a widely accepted scientific problem-solving language and compiler, contained in 8K words of memory. It can be used to perform integer, real and double precision operations. Both program execution and compilation is much faster using this version. Input and output can be accessed directly, and all RT-11 monitor functions are completely accessible through callable subroutines. Object programs are put out in run time format without any intermediate assembly.

PROM Formatter QJV11-CB
This software generates formatted tape from which a PROM chip can be blasted.

LSI-11 Paper Tape Diagnostics ZJV01-RB
These tapes test the processor, exercise the memory, isolate problem modules and exercise the I/O devices.

DRV11-B Direct Memory Access (DMA) Interface

LSI-11

M SERIES

Length: Extended
Height: Quad
Width: Single

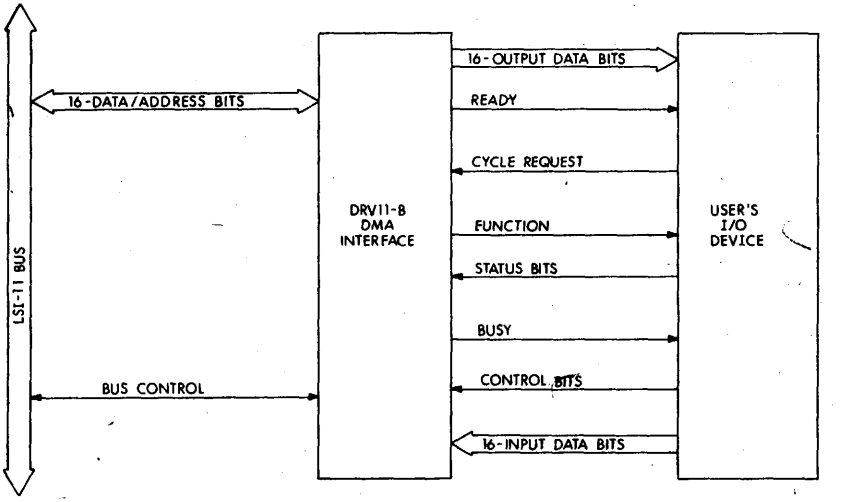


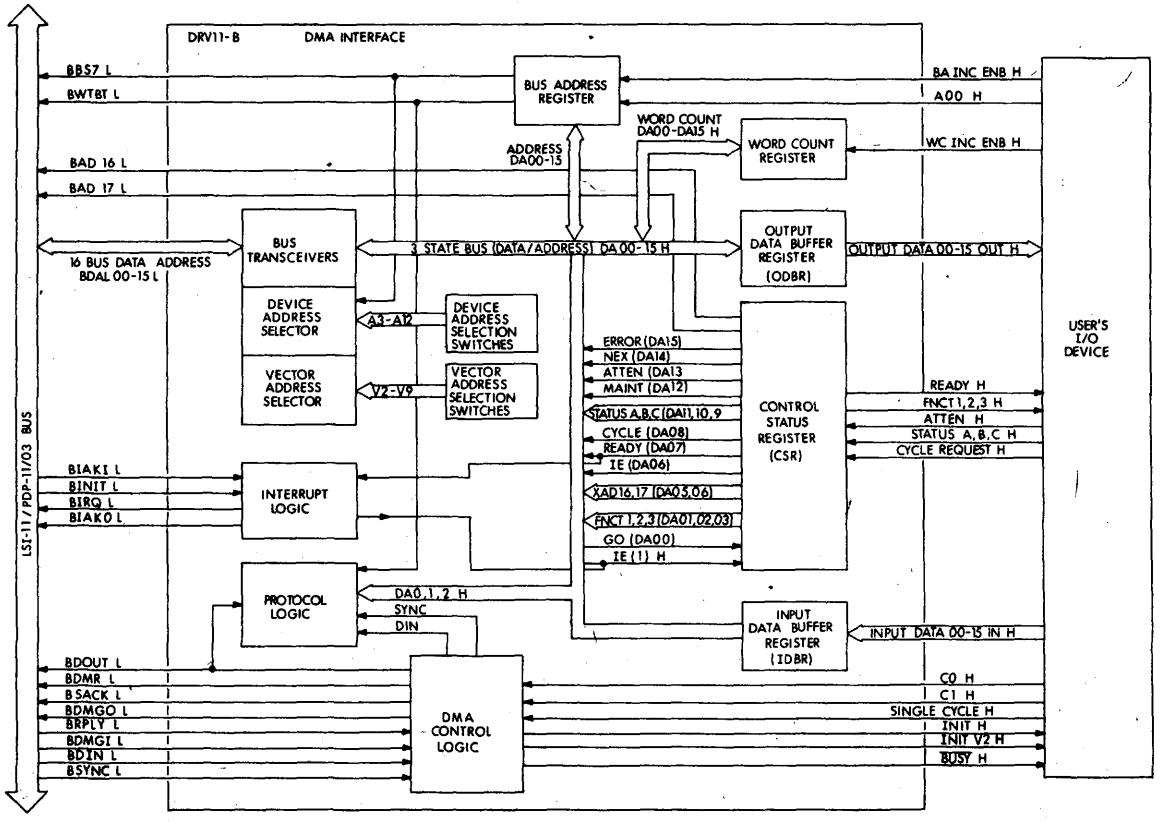
Figure 1. DRV11-B Interface Diagram

DESCRIPTION

The DRV11-B is a general purpose Direct Memory Access (DMA) interface used to transfer data directly between the LSI-11 system memory and an I/O device as shown on Figure 1. The interface is programmed by the processor to move variable length blocks of 16-bit data words to or from specified locations in memory by means of the LSI-11 bus. Once programmed, no processor intervention is required. The DRV11-B can transfer up to 250K, 16-bit words per second and is capable of operating in burst modes, with byte addressing. The control structure also allows read-modify-restore operations.

The interface consists of five registers: Word Count Register (WCR), Bus Address Register (BAR), Control Status Register (CSR), Input Data Buffer Register (IDBR), and Output Data Buffer Register (ODBR). The module also includes bus transceivers and logic for interrupt requests, address control and protocol, and DMA requests.

The DRV11-B contains one switch bank used to assign an appropriate device address to the DMA interface and one switch bank to select an interrupt vector address in the LSI-11 memory where the DMA routine is stored.


DRV11-B DMA INTERFACE
LSI-11/PDP-11/03 BUS
BBS7 L
BWTBT L
BAD 16 L
BAD 17 L
16 BUS DATA ADDRESS BDAL 00-15 L
BUS TRANSCEIVERS
DEVICE ADDRESS SELECTOR
A3-A12
DEVICE ADDRESS SELECTION SWITCHES
VECTOR ADDRESS SELECTOR
V2-V9
VECTOR ADDRESS SELECTION SWITCHES
BIAKI L
BINIT L
BIRQ L
BIAKO L
INTERRUPT LOGIC
PROTOCOL LOGIC
BDOUT L
BDMR L
BSACK L
BDMGO L
BRPLY L
BDMGI L
BDIN L
BSYNC L
DMA CONTROL LOGIC
BUS ADDRESS REGISTER
ADDRESS DA00-15
WORD COUNT DA00-DA15 H
WORD COUNT REGISTER
3 STATE BUS (DATA/ADDRESS) DA 00-15 H
OUTPUT DATA BUFFER REGISTER (ODBR)
OUTPUT DATA 00-15 OUT H
ERROR (DA15)
NEX (DA14)
ATTEN (DA13
MAINT (DA12)
STATUS A,B,C (DA11,10,9
CYCLE (DA08)
READY (DA07)
IE (DA06)
XAD 16,17 (DA05,06)
FNCT 1,2,3 (DA01,02,03)
GO (DA00)
IE (1) H
CONTROL STATUS REGISTER (CSR)
DA0,1,2 H
SYNC
DIN
INPUT DATA BUFFER REGISTER (IDBR)
INPUT DATA 00-15 IN H
BA INC ENB H
A00 H
WC INC ENB H
READY H
FNCT 1,2,3 H
ATTEN H
STATUS A,B,C H
CYCLE REQUEST H
C0 H
C1 H
SINGLE CYCLE H
INIT H
INIT V2 H
BUSY H
USER'S I/O DEVICE

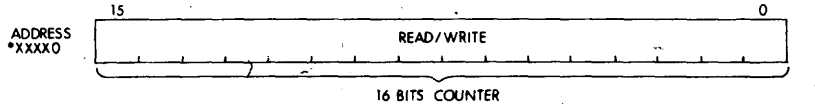
Two 40-pin connectors, mounted near the edge of the module, facilitate the connection of the I/O device with the DMA, using any two of several cable assemblies available from DIGITAL. The module may be inserted into any available slot of the LSI-11 backplane or backplane extenders according to the rules and restrictions as described in the LSI-11, PDP-11/03 User's Manual.

REGISTERS

Each of the five registers can be addressed by the processor. The IDBR and ODBR are assigned the same address, and are read-only and write-only, respectively.

The register bit format and functions are described as follows.

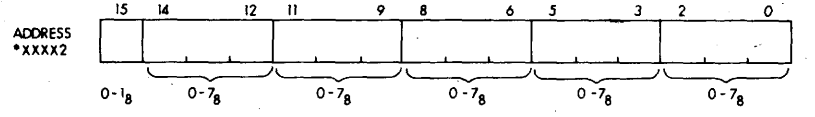
Word Count Register (WCR)



*All logic "ones" decoded by bus master to assert BBS7 L signal

The WCR is a 16-bit read/write counter which is loaded by the program with the two's complement of the number of words or bytes to be transferred at one time between memory and the I/O device. At the end of each transfer, the WCR is incremented. When the count becomes zero (all 16 bits = 0), the DMA generates an interrupt request. The contents of the WCR can be monitored by the processor program.

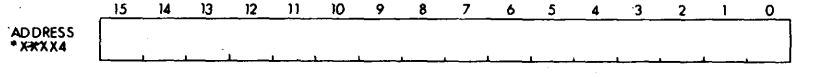
Bus Address Register (BAR)



*All logic "ones" decoded by bus master to assert BBS7 L signal

The BAR is a 15-bit read/write register used to generate the bus address which specifies the location to or from which data is to be transferred. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the control status register. Bus address bit 00 is driven by the user device.

Control and Status Register (CSR)



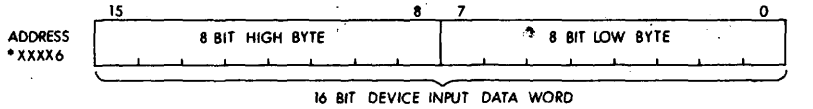
*All logic "ones" decoded by bus master to assert BBS7 L signal

The CSR contains 16 bits of information used to control the function and monitor the status of the DMA transfers. The information in the CSR can be modified or read by the processor program in either 8-bit bytes or 16-bit words. Table 1 lists and defines each of the 16 bits.

Table 1 Control Status Register Bit Description

BIT	NAME	DESCRIPTION
15	Error (Read Only)	1. Indicates a special condition. a. NEX (bit 14) b. ATTN (bit 13) 2. Sets READY (bit 7) and causes interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition. a. NEX is cleared by writing to zero. b. ATTN is cleared by the user device.
14	NEX (Read/Write Zero)	1. Non existent memory indicates that as bus master, the DRV11-B did not receive BRPLY or that a DATIO cycle was not completed. 2. Sets Error (bit 15). 3. Cleared by INIT or by writing to zero.
13	ATTN (Read Only)	1. Indicates the state of the ATTN user signal. 2. Sets Error (bit 15).
12	MAINT (Read/Write)	1. Maintenance bit used with Diagnostic Program.
11	STAT A (Read Only)	1. Device Status bits that indicate the state of the DSTAT A, B, and C user signals. 2. Set and cleared by user control only.
10	STAT B (Read Only)	
09	STAT C (Read Only)	
08	CYCL (Read/Write)	1. Cycle is used to prime a DMA bus cycle.
07	READY (Read Only)	1. Indicates that the DRV11-B is able to accept a new command. Requests an interrupt if IE (bit 06) is set. 2. Set by INIT.
06	IE (Read/Write)	1. Enables interrupts to occur when READY (bit 07) is set. 2. Cleared by INIT.
05	XAD 17 (Read/Write)	EXTENDED Address bit 17, cleared by INIT.
04	XAD 16 (Read/Write)	EXTENDED Address bit 16, cleared by INIT.
03	FNCT 3 (Read/Write)	1. Three bits made available to the user device. User defined. 2. Cleared by init.
02	FNCT 2 (Read/Write)	
01	FNCT 1 (Read/Write)	
00	GO (Write Only)	1. Causes "NOT READY" to be sent to the user device indicating a command has been issued. Clears READY (bit 07). Enables DMA transfers.

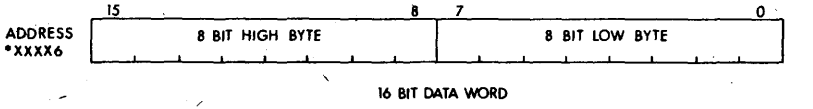
Input Data Buffer Register (IDBR)



*All logic "ones" decoded by bus master to assert BBS7 L signal

The IDBR is used for read-only operations. Data is loaded into the register by the user's device. The data may be read from the IDBR as a 16-bit word, an 8-bit high byte or an 8-bit low byte. Transfers are usually via DATO or DATOB DMA bus cycles. The register input connects to J2 mounted on the module.

Output Data Buffer Register (ODBR)



*All logic "ones" decoded by bus master to assert BBS7 L signal

The ODBR is used during write-only operations. Data from the LSI-11 bus is loaded into the register under program control and read from the register by the user's device. The register can be loaded with a 16-bit data word or with an 8-bit high byte, or as an 8-bit low byte. Transfers are usually via DATI or DATIO DMA bus cycles. The output of the register connects to J1 on the module.

DEVICE AND VECTOR ADDRESS SELECTION

The address of the DRV11-B interface and the interrupt vector address in memory is selected by the position of the switches in switch bank S1 and S2, respectively. The location of the switches on the module is shown on Figure 2. The switches are set to the OFF position (open) to select a zero bit in the address format and the ON position (closed) to select a one.

Device Address Format

The DRV11-B decodes four address, one for each of the registers listed:

Register	Octal Address
WCR	*XXXX0
BAR	*XXXX2
CSR	*XXXX4
DBR	*XXXX6

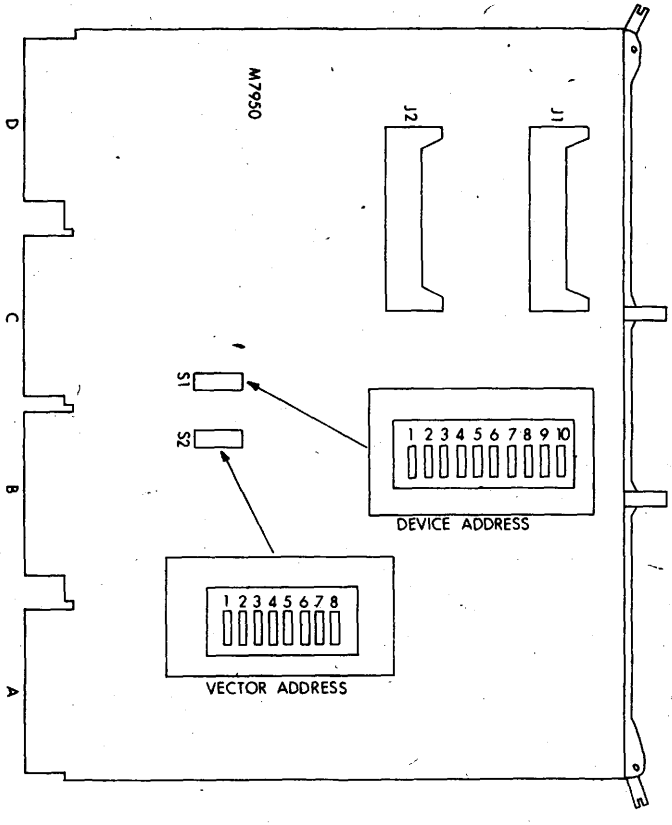


Figure 2 Connector and Switch Locations

Normally, the addresses assigned to the DMA start at 772410_8 and progress upward. Switches S1-1 through S1-10 select the base address as indicated by the X portion of the octal code and the individual registers are decoded by the DMA interface. The relationship between the address format and the switches are shown on Figure 3.

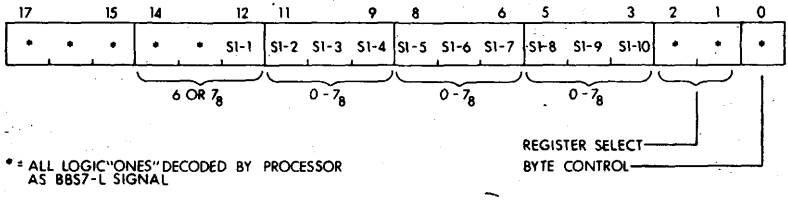


Figure 3 Device Address Switch (S1) Selection

Interrupt Vector Address Selection
The interrupt vector addresses for the LSI-11 systems are allocated memory locations from $0\text{-}774_8$. The recommended location assigned to the DRV11-B is 124_8. Switches S2-1 through S2-8 are used to select the octal address and the relationship between the switches and address format is shown on Figure 4.

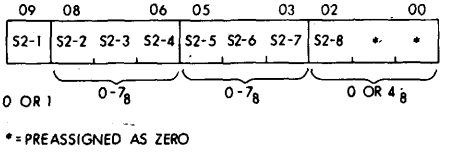


Figure 4 Interrupt Vector Address Switch (S2) Selection

FUNCTIONS
The DRV11-B interface operates as both a slave and master device. Prior to becoming bus master, all Data Transfers Out (DATO) or Data Transfer In (DATI) are in respect to the processor. Once DMA is granted bus mastership by the processor, all data transfers are in respect to the DMA.

DMA operation is initialized under program control by: (1) loading the WCR with the two's complement of the number of words to be transferred; (2) loading the BAR with the first address to or from which data is to be transferred; (3) loading the CSR with the desired function bits. After the interface is initialized, data transfers are under control of the DMA logic.

Program Control Transfers
Data transfers may be performed under program control by addressing the IDBR or ODBR and reading or writing data.

DMA Control Transfers
DMA input (DATI) or output (DATO) data transfers occur when the processor clears READY. For a DATO cycle (DRV11-B to memory transfer), the user's I/O device presets the CONTROL BITS [word count increment enable (WC INC ENB), bus address increment enable (BA INC ENB), C1, C0, A00, and ATTN], and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the CONTROL BITS are latched into the DRV11-B DMA control, and BUSY goes low. A DATI cycle—memory to DRV11-B transfer—is handled in a similar manner, except that the output data is latched into the output DBR at the end of the bus cycle.

When the DRV11-B becomes bus master, a DATO or DATI cycle is performed directly to or from the LSI-11 memory location specified by the BAR. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue until the WCR increments to zero, at which time READY goes high and the DRV11-B generates an interrupt (if interrupt enable is set) to the LSI-11 processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete transfer of the specified number of data words.

DEVICE CABLES AND SIGNALS

Data, status and control signals are transferred between the user's I/O device and DMA by an input and an output cable assembly. The input cable attaches to connector J2 and the output cable attaches to connector J1 as shown on Figure 2. Table 2 and 3 list the connector pin and designations for each signal. Table 4 lists several recommended cable assemblies that are available from DIGITAL in the lengths indicated. The H856 female connector mates with either J1 or J2 on the DRV11-B. To order cable assemblies in lengths not listed, contact a DIGITAL sales office.

GENERAL SPECIFICATIONS

Module Size

Quad-height, single-width, extended-length

Dimensions

8½ in. L, 10½ in. H, ½ in. W (21.6 cm L, 26.7 cm H, 1.27 cm W)

Weight

13 oz. (370 gr.)

User I/O Connections

Two 40-pin connectors

Table 2 Input Connector Signals

J2* Connector Pin	Signal Name	Unit Loads
B	BUSY H	10 (drive)
D	ATTN H	1
F	A00 H	1
J	BA INC ENB H	1
K, L	FNCT 3 H	10 (drive)
N	C0 4	1
R	FNCT 2 H	10 (drive)
T	C1 H	1
V	FNCT 1 H	10 (drive)
DD	08 IN H	
FF	09 IN H	
JJ	10 IN H	
LL	11 IN H	
NN	12 IN H	
RR	13 IN H	
TT	14 IN H	
VV	15 IN H	
CC	07 IN H	1
EE	06 IN H	
HH	05 IN H	
KK	04 IN H	
MM	03 IN H	
PP	02 IN H	
SS	01 IN H	
UU	00 IN H	

*All remaining pins connect in common to logic ground by board etch.

Table 3 Output Connector Signals

J1* Connector Pin	Signal Name	Unit Loads
B	CYCLE REQUEST H	1
D	INIT V2 H	10 (drive)
F	INI H	10 (drive)
J	WC INC ENB H	1
K	SINGLE CYCLE H	1
L	STATUS A	1
N	READY H	10 (drive)
R	STATUS B	1
T, V	STATUS C	1
DD	08 OUT H	
FF	09 OUT H	
JJ	10 OUT H	
LL	11 OUT H	
NN	12 OUT H	
RR	13 OUT H	
TT	14 OUT H	
VV	15 OUT H	
CC	07 OUT H	10 (drive)
EE	06 OUT H	
HH	05 OUT H	
KK	04 OUT H	
MM	03 OUT H	
PP	02 OUT H	
SS	01 OUT H	
UU	00 OUT H	

*All remaining pins connect in common to logic ground by board etch.

Table 4 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft.)
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25,50
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

Mounting Requirements
Plugs directly into LSI-11 backplane or LSI-11 expansion backplane.

Electrical
Logic Power Requirements: +5 V ±5% @ 1.9 A (nominal)

LSI-11 Bus Loading
Presents one (1) bus load

User Loading

Input Data Lines:
1 TTL unit load each
HIGH = logic one
LOW = logic zero

Input Control Lines:
1 TTL unit load each
HIGH = logic one
LOW = logic zero

Output Data Lines:
10 TTL unit loads (drive) each
HIGH = logic one
LOW = logic zero

Output Control Lines:
10 TTL unit loads (drive) each
HIGH = logic one
LOW = logic zero

Module Type
M7950

Operational

Transfer Mode: DMA or program-controlled without interrupts

Data Transfer: Up to 250,000 16-bit words per second

Environmental

Temperature:
Storage: —40° to 66°C (—40° to 150°F)
Operating: 5° to 50°C (41° to 122°F)

Relative Humidity: 10% to 95% non-condensing

DRV11-P
BUS FOUNDATION MODULE

LSI-11

M SERIES

Length: Extended
Height: Quad
Width: Single

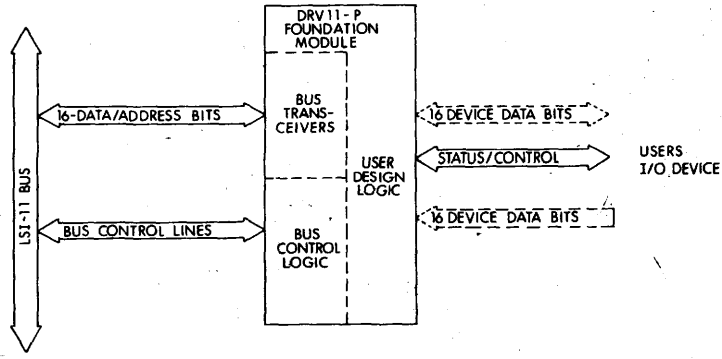


Figure 1. Typical DRV11-P Interface

DESCRIPTION

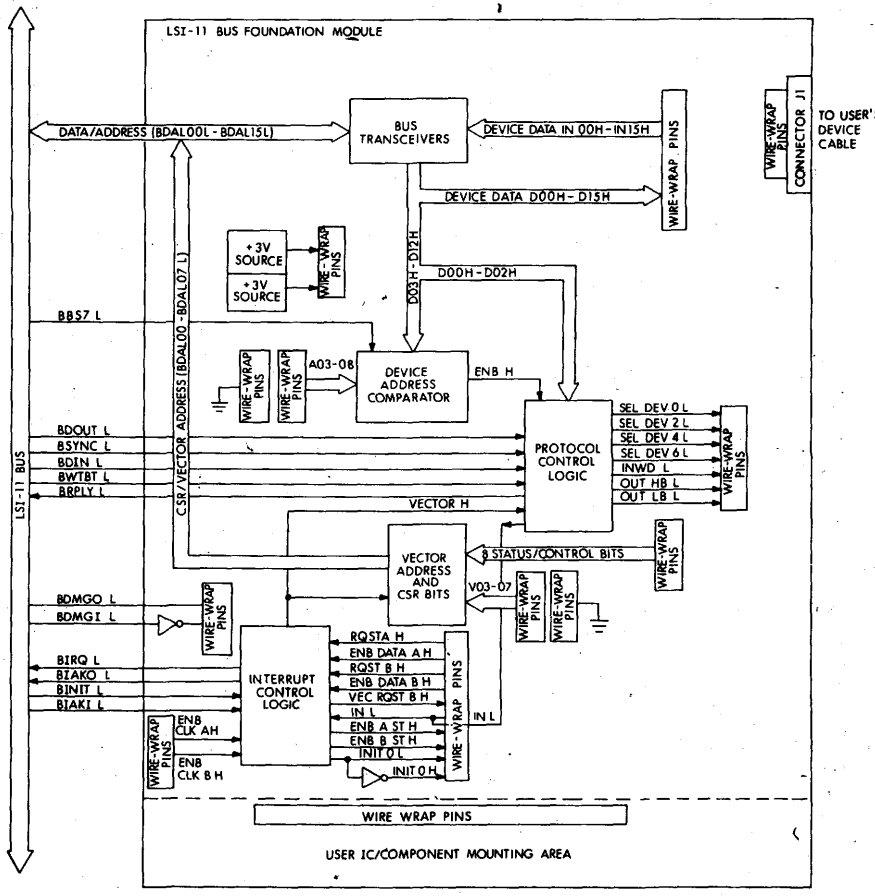
The DRV11-P is a versatile wire wrap module that contains the bus interface logic for operation with the LSI-11 or PDP-11/03 system and provides adequate board area for mounting and connecting integrated circuits (IC's) or discrete components. Because the bus interface logic is included, the module can be efficiently configured by the user to satisfy a variety of device interface logic applications.

A 40-pin connector, conveniently mounted at the board edge, facilitates the connection to a device through several cable assembly types available from DIGITAL.

Except for the bus interface connections, all signals and voltages are terminated to wire wrap pins for user connections. The bus control logic is provided with wire wrap test points for monitoring the internal signals. The test points are spaced at 0.1 in. (.254 cm) between pins to allow a 40-pin connector to be inserted over the wire wrap pins for automated test functions.

Approximately 2/3 of the surface area on the module consists of plated-through holes, each connected to a wire wrap pin. The user can mount three different types of dual-in-line IC's or a variety of discrete components into the holes and connect the proper voltages and signals by wire wrapping leads on the board.

The DRV11-P module can be inserted into any one of the available interface option locations of the LSI-11, PDP-11/03 backplane, or backplane extender unit. The module occupies four vertical slots. Refer to the LSI-11, PDP-11/03 User's Manual for detailed installation information.


LSI-11 BUS FOUNDATION MODULE
LSI-11 BUS
DATA/ADDRESS (BDAL00L - BDAL15L)
BUS TRANSCEIVERS
DEVICE DATA IN 00H - IN15H
DEVICE DATA D00H - D15H
WIRE-WRAP PINS
CONNECTOR J1
TO USER'S DEVICE CABLE
+3V SOURCE
+3V SOURCE
D03H - D12H
D00H - D02H
BBS7 L
CSR/VECTOR ADDRESS (BDAL00 - BDAL07 L)
A03-08
DEVICE ADDRESS COMPARATOR
ENB H
PROTOCOL CONTROL LOGIC
SEL DEV 0 L
SEL DEV 2 L
SEL DEV 4 L
SEL DEV 6 L
INWD L
OUT HB L
OUT LB L
BDOUT L
BSYNC L
BDIN L
BWTBT L
BRPLY L
VECTOR H
VECTOR ADDRESS AND CSR BITS
8 STATUS/CONTROL BITS
V03-07
BDMGO L
BDMGI L
BIRQ L
BIAKO L
BINIT L
BIAKI L
INTERRUPT CONTROL LOGIC
RQSTA H
ENB DATA A H
RQST B H
ENB DATA B H
VEC RQST B H
IN L
ENB A ST H
ENB B ST H
INIT 0 L
INIT 0 H
ENB CLK A H
ENB CLK B H
WIRE WRAP PINS
USER IC/COMPONENT MOUNTING AREA

FUNCTIONS

The DRV11-P contains 16 bus transceivers, device selection and vector address generation logic, interrupt control, and control and status register functions. The device data inputs and outputs of the bus transceivers and the device control signals are made available to user to complement control of up to four 16-bit registers.

Address Selection Logic

The address selection logic consists of a device address comparator and the protocol control logic. Up to four discrete addresses are made available with the existing logic on the DRV11-P and can be assigned to data registers, status and control registers, or word counters. By adding additional IC's, the user can increase the total number of addresses available. The main address of the DRV11-P is selected by monitoring the BBS7 bus line and decoding the address information D03-D12 from the bus. The main device address is assigned by the configuration of jumper leads (A03-A08) attached to wire wrap pins. When the selected and input bus addresses are the same, the device address comparatory provides an ENB H level to the protocol control logic. The protocol control logic receives bus signals and address bits D01-D02 to assert one of the four available output lines—SEL DEV 00, SEL DEV 2L, SEL DEV 4L, and SEL DEV 6L. In addition, the protocol control logic provides output signals to specify word or byte transfers.

Table 1 lists and defines the function of the control signals required or available for the user logic.

Table 1 Protocol Control Logic Signals

Signal	Function
SEL DEV 0L SEL DEV 2L SEL DEV 4L SEL DEV 6L	Select Device 0 through 4—One of four lines asserted by decoding the device address and available to select one of four user word registers.
OUT LB L OUT HB L	Out Low Byte, Out High Byte—Used to load (write) data into low byte (8 bits) or high byte (8 bits) or both bytes (16 bits) of the selected word register.
IN WD L	In Word—Used to gate (read) data from the selected word register to the bus.

The format for the device address selection is shown on Figure 2. A logic one is specified when no jumper lead is installed between the appropriate wire wrap pin from A3-A12. A logic zero is specified when a jumper lead is installed.

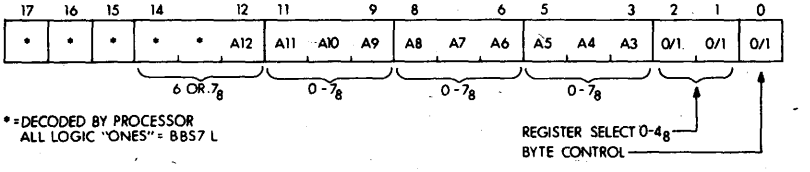


Figure 2. Device Address Selection

Interrupt Control Logic

The interrupt control provides the circuits necessary to allow a program interrupt transaction between the LSI-11 and device. Two interrupt channels (A and B) are available to the user with channel A assigned the highest priority. Table 2 lists and defines the user available signals associated with the interrupt control logic.

Table 2 Interrupt Control Logic Signals

Signal	Function
RQST A H	Interrupt Request A—Asserted by device logic and sets the channel A Interrupt Request flip-flop when the channel A Interrupt Enable flip-flop is set.
ENB DATA A H	Interrupt Enable A Data—Asserted by device logic and sets the channel A Interrupt Enable flip-flop when the ENB CLK A signal is asserted.
ENB CLK A	Interrupt Enable A Clock—Asserted by device logic to cause the channel A Interrupt Enable flip-flop to be set when ENB DATA A signal is asserted.
ENB A ST H	Interrupt Enable A Status—Indicates the status of the channel A Interrupt Enable flip-flop.
RQST B H	Interrupt Request B—Same as RQST A H signal except controls channel B interrupts.
ENB DATA B H	Interrupt Enable B Data—Same as ENB DATA A H signal except controls channel B interrupts.
ENB CLK B	Interrupt Enable B Clock—Same as ENB CLK A signal except controls channel B interrupts.
ENB B ST H	Interrupt Enable B Status—Same as ENB A ST H except controls channel B interrupts.
VECTOR H	Interrupt Vector Gate—Used by device logic to gate vector address onto the bus and to generate B RPLY signal.
VEC RQST B H	Vector Request—Asserted by device logic to specify that channel A vector address is required; negated to specify channel B vector address is required.
INIT O L	Initialize Out—Buffered B INIT L signal from bus used for general initialization.

Vector Address and CSR Logic

The vector address logic is used in conjunction with the interrupt control logic to generate a vector address on bus lines BDAL 00L-BDAL 07. The vector address is specified by the user and selected by installing jumper leads between wire wrap pins on the M7948 module. The addresses available are from 000_8 to 374_8. The vector address range can be increased from 000_8 to 774_8 with additional logic and wiring.

When the VECTOR H signal is asserted as a result of a device interrupt request, the vector address is placed on the bus lines.

Wire wrap pins V3 through V7 are used to assign the vector address. A jumper lead installed selects a logic "zero" address bit for its associated line and no lead selects a logic "one" address bit according to the format on Figure 3.

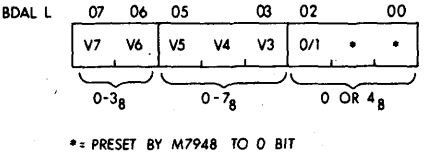


Figure 3. Vector Address Select Format

Bit BDAL 02 L can be connected to the device interrupt request signal RQST A signal to specify a separate vector address for channel A and channel B.

Status and control information can be multiplexed through the same logic used to generate the vector address. Up to eight status and control bits can be assigned by the user and transferred to bus lines BDAL 00 L-BDAL 07 L. The information can be gated onto the bus lines using a select level generated by the address decoding logic.

COMPONENT MOUNTING AREA

Twelve vertical areas (A-L) are available on the M7948 module for mounting integrated circuits or discrete components as shown on Figure 4. Each area has a double row of wire wrap pins that connect to an associated plated through hole located at 0.1 in. (.254 cm) vertical spacing. Area A is for multi-use and is capable of accepting IC's with pin centers at 0.3 in. (.762 cm), 0.4 in. (1.01 cm) or 0.6 in. (1.52 cm). Area K will also accept IC's with pin centers at 0.3 in. or 0.4 in. All remaining areas will only accept IC's with pin centers at 0.3 in.

Table 3 lists the total number of IC's with 0.3 in. spacing that can be mounted in the user areas of the module, A through L.

Table 3 IC MOUNTING

IC Type	Total Number
14 pin	60
16 pin	52
18-pin	44
20 pin	44

Connector Wire Wrap Pins

The 36 contact pins in row C and D at the edge of the module connect to a double row of wire wrap pins. These two rows are made available to the user for connecting signals and voltages from the backplane to the user installed logic circuits. The following pins of row C and D are normally dedicated to +5V and GND.

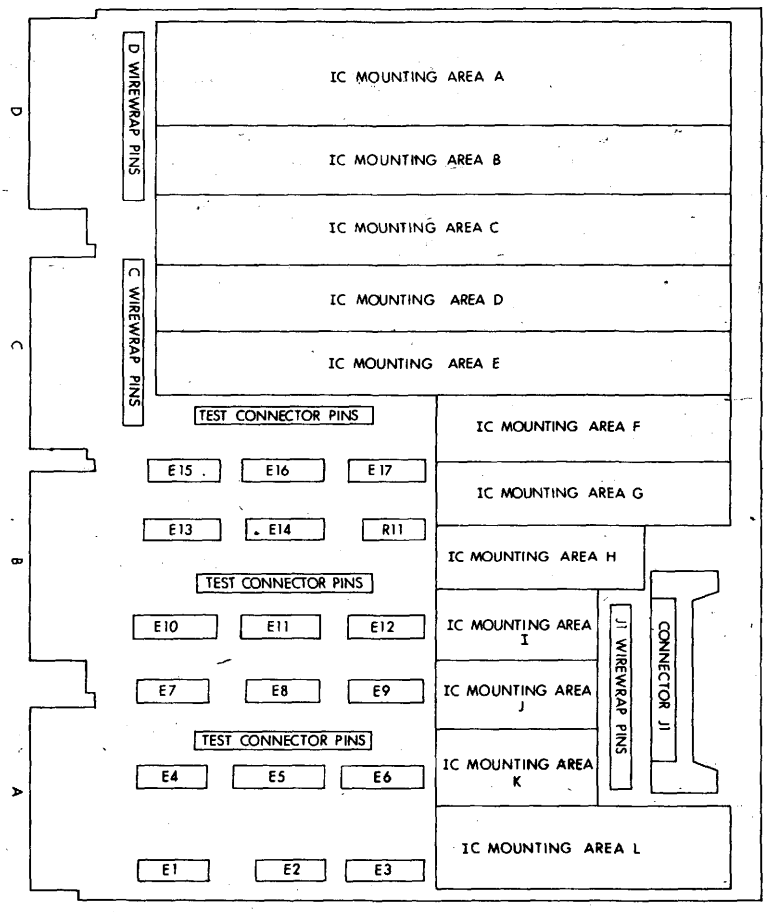


Figure 4 DRV11-P Component Mounting Locations

The user can connect the power to the IC or components using the row C and row D wire wrap pins.

+5 V	CA2, DA2
GND	CJ1, CM1, CT1 DJ1, DM1, DT1 CC2, DC2

Device Signals

Input and output data, status and control signals can be transferred between the device and the DRV11-P module using any one of several cable assemblies listed on Table 4 and available from DIGITAL. One end of each cable is terminated with a 40-pin female connector which mates with the 40-pin male connector J1 mounted on the M7948 module. The pins of J1 connect to the user installed logic through a series of wire wrap pins.

Table 4 Recommended Cable Assemblies

Cable No.	Connectors	Type	
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

GENERAL SPECIFICATIONS

Bus Input Loading:	Presents a maximum of one unit load on the LSI-11 bus.
Operating Temperature:	5°C (41°F) to 50°C (122°F)
Relative Humidity:	10% to 90%, without condensation
Power:	+5 V at 1.0 A (max); user logic not included
Size	Quad height— 10.5 in. (26.67 cm) Single width— 0.5 in. (1.27 cm) Extended length— 8.5 in. (21.59 cm)

OPTIONAL EQUIPMENT

Integrated Circuits (ICs)

Two special ICs are available from Digital Equipment Corporation for use in configuring custom interfaces with the DRV11-P.

DEC8640 Bus Receiver IC (Quad 2-Input NOR Gates)—956

The 956 is a package of ten 14-pin, dual-in-line package (DIP) DEC8640* integrated circuits (ICs). Each IC comprises four 2-input NOR gates. Each gate performs the Boolean function $X = A + B$. The DEC8640 gates are especially suitable as Unibus or LSI-11 bus receivers because of their high impedance characteristics and, hence, minimal loading on the bus.

These NOR gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

DEC8881-1 Bus Driver IC (Quad 2-Input NAND Gates)—957

The 957 is a package often 14-pin, dual-in-line package (DIP) DES8881-1 integrated circuits (ICs). Each IC comprises four 2 input NAND gates. Each gate performs the Boolean function $X = AB$. The DES8881-1 ICs are especially suitable as Unibus or LSI-11 bus drivers because of their capability to sink 70 mA with a collector voltage of less than 0.8 V.

These NAND gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

*DEC8640 IC replaces DEC380 IC.

KPV11-A Power Fail/Line Time Clock Generator

LSI-11

M SERIES

Length: Extended
Height: Double
Width: Single

DESCRIPTION

The KPV11-A Module (M8016) is an LSI-11 power fail/restore signal sequence and line time clock (LTC) generator. (See Figure 1). It is compatible with all LSI-11 component systems and LSI-11 backplane options. The KPV11-A is designed for installation in any LSI-11 bus-structured backplane or remote installation (not installed in a backplane) via an optional cable which connects the option to the LSI-11 backplane. An optional console panel (DEC Part No. 54-11808) is available for manual control of LTC and power signal generation and display of DC power on/off status and processor run/halt state.

FEATURES

Automatic generation of BPOK and BDCOK power-up/power-down signal sequence.

Automatic program restoration and starting when used with non-volatile memory and appropriate software routines.

The built-in line time clock is program compatible with the KW11-L. The KPV11-A is factory-configured for Line clocK Status (LKS) register address and operations.

Line time clock time reference can be provided by a signal source (user supplied) other than the power line.

Can be installed in the LSI-11 backplane or mounted remotely. An optional cable connects the KPV11-A to the LSI-11 backplane when mounted remotely.

Expandable with the 54-11808 console panel option.

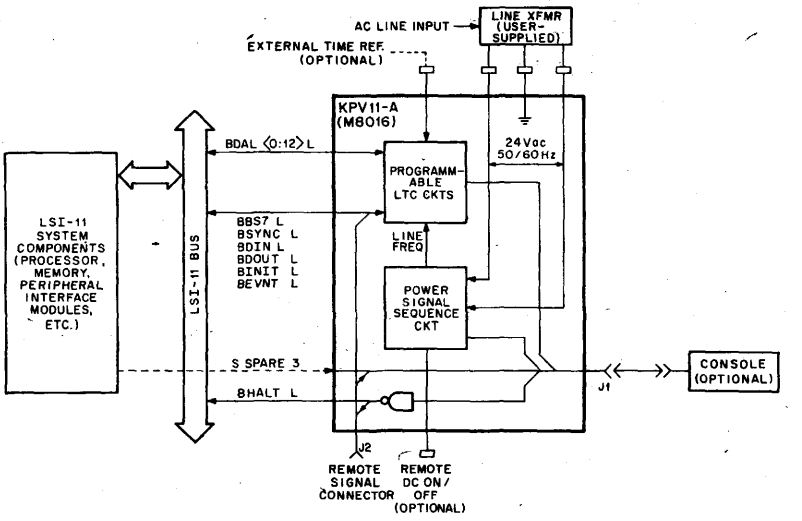


Figure 1 KPV11-A System Interface

CONFIGURING LTC JUMPERS

LTC jumpers are located on the M8016 module as shown in Figure 2 and are factory-configured for programmable operation with the LKS register address (177546) as shown in Figure 3. Normally, it will not be necessary to reconfigure LTC jumpers; however, it is possible to alter LTC operation as listed below and the LKS deviee address as shown in Figure 3.

Jumper	Installed	Removed
W12	Enable manual control or continuous LTC interrupt request operation. Do not install when W13 is installed.	*Disable continuous or manual operation.
W13	*LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.	LTC interrupt requests cannot be program controlled.
W14	*Console (optional) LTC ON/OFF switch enabled.	Console LTC ON/OFF switch disabled.
W15	*LTC signal occurs at the power line frequency.	LTC frequency is determined by an external source via EXT TIME REF etched pad on module.

* Factory-jumpered configuration.

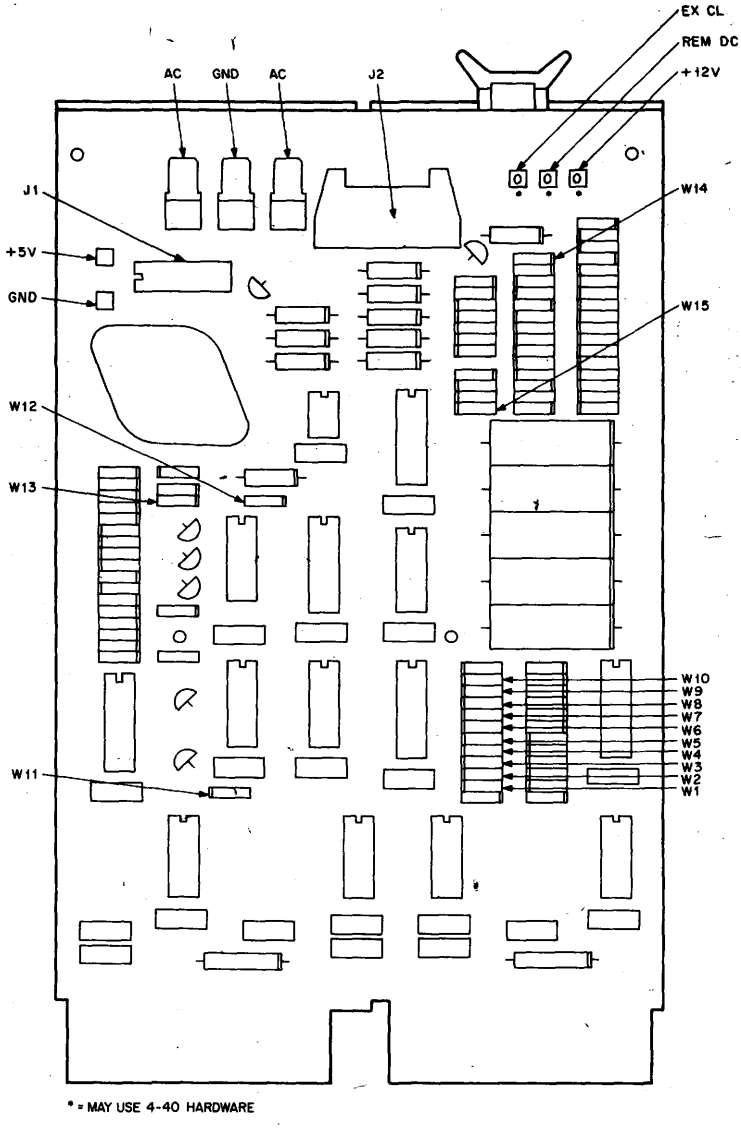


Figure 2 KPV11-A Jumper, Connector, and Pad Locations

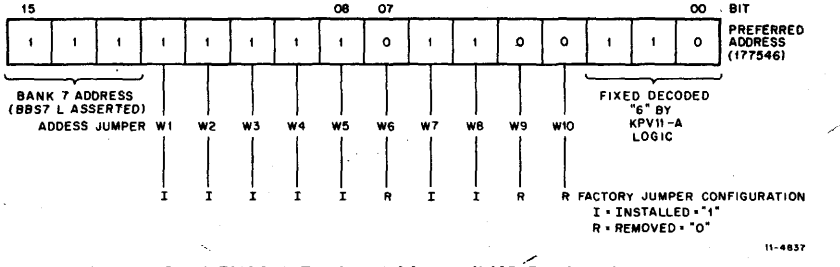


Figure 3 KPV11-A Device Address (LKS Register) Jumpers

KPV11-A MODULE INSTALLATION

BACKPLANE

The KPV11-A module can be installed in any LSI-11 structured backplane, such as the H9270 and DDV11-B.

REMOTE LOCATION

Mounting holes are provided in the KPV11-A module for remote location installation. (See Figure 4 for mounting details)

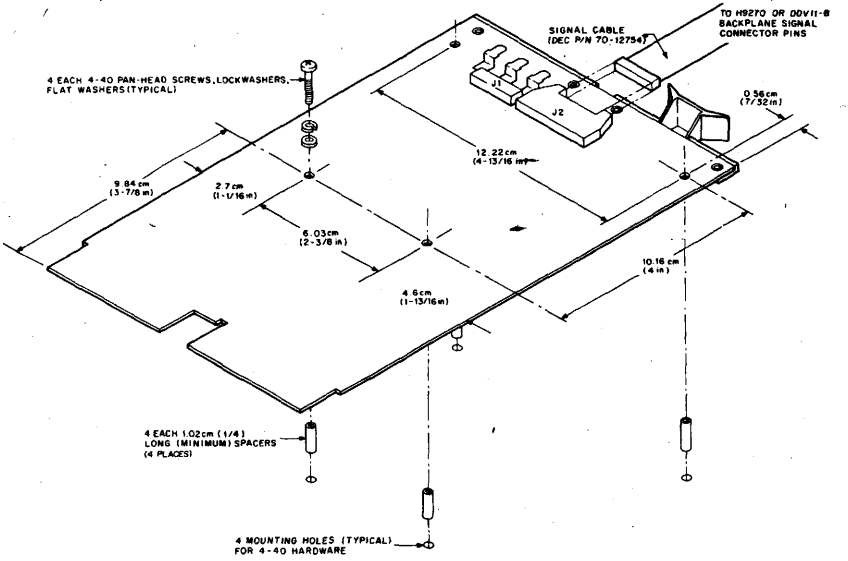


Figure 4 KPV11-A Remote Installation

NOTE

Program control of the LTC function is not possible when remote installation is used. However, manual control is available using the optional control panel.

The KPV11-A is electrically connected to the LSI-11 bus using an optional signal cable, (DEC Part No. 70-12754). This cable is inserted into the 10 pin connector on H9270 or DDV11-B backplane. (See Figure 4).

The +5V and +12VDC voltage sense input must be provided by the user when the KPV11-A is not installed in the LSI-11 backplane. Figure 2 illustrates the location of etched pads provided for the purpose of voltage connection to the module.

Power Sense Connection
The user is required to supply the 24Vac center tapped, 50 or 60Hz input voltage necessary to produce the DC operation voltage for the option. In addition, this voltage provides the 50 or 60Hz reference for the LTC function, and is the power fail monitor signal for the power signal sequence circuit. Illustrated in Figure 2 is the location of three tabs on the KPV11-A module provided for voltage connection.

CONSOLE PANEL
Electrical connections between the KPV11-A and the console panel are made via 16-pin dual-in-line integrated circuit sockets located on each assembly. The electrical connection between the sockets is made using a signal/power cable (DEC Part No. 70-08612).

In addition to the LTC ON/OFF and RUN/ENABLE switch functions, the console panel includes a DC ON/OFF switch. This switch, when in the OFF position, disables BDCOK H and BPOK H signal generation. If desired, this switch can also control the DC On/Off state of the user's power supply if it is capable of being controlled by a T^2L Signal.

Use of External Time Reference
The KPV11-A normally uses the 50 or 60Hz input (via the three power tabs on the module) for LTC signal generation. However, an external TTL Logic-compatible frequency source may be used for producing LTC signals at frequencies other than the power line frequency. An etched pad is provided for this purpose on the KPV11-A module.

LTC PROGRAMMING
The LSI-11 program communicates with the LTC function via the LKS register (Figure 5) contained in the KPV11-A logic circuits. The LKS register's device address is normally configured to 177546 for system software compatibility.

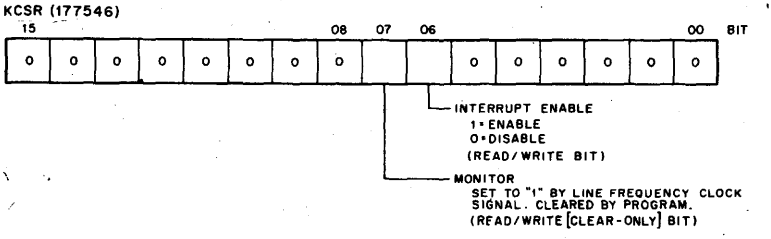


Figure 5 Line Time Clock Status Register (LKS)

LTC interrupts, when enabled (LKS bit 06 = 1), occur as an interrupt request (bus low assertion) on the BEVNT L signal line. This causes the processor to execute a service routine via vector address 100. Memory location 100 must contain the PC (starting address) for the LTC service routine;

similarly, memory location 102 must contain the PS (processor status word) for the service routine. As with all "external" interrupts, the LSI-11 processor will recognize the LTC interrupt request only when the current PS bit 07 is cleared. When PS bit 07 = 1, external interrupts, including the LTC interrupt, are ignored. The LTC interrupt has highest priority of all external interrupts and does not require a vector address bus transfer. An interrupt request via the BEVNT L bus signal line, as previously stated, always results in access to the service routine via vector address 100.

CONSOLE OPERATION

The console panel option* controls and indicators are shown in Figure 6 and described below:

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set on ON and proper dc output voltages are being produced by the user's power supply and sensed by the KPV11-A. If either the +5 V or +12 V output from the power supply is Low, the DC ON indicator will not illuminate.
RUN	LED indicator	Illuminates when the LSI-11 processor is in the run state (see ENABLE/HALT).
Spare	LED indicator	
DC ON/OFF	Two-position toggle switch	When set on ON, enables the dc outputs of the user's power supply (if connected for this function—see instructions for installing the console panel). The DC ON indicator will illuminate if the dc output voltages are of proper values. When set to OFF, the power supply dc outputs are disabled and the DC ON indicator is extinguished.
ENABLE/ HALT	Two-position toggle switch	When set to ENABLE, the B HALT L line to the processor is not asserted and the processor is in the run-enable mode (RUN indicator is illuminated only when the processor is executing a program). When set to HALT, the B HALT L line is asserted. The processor halts program execution and executes console ODT microcode. The RUN indicator is extinguished.
LTC ON/OFF	Two-position toggle switch	When set to ON, enables KPV11-A generation of LTC interrupts. When set to OFF, disables LTC interrupts (W14 must be installed).

* When used in conjunction with the KPV11-A.

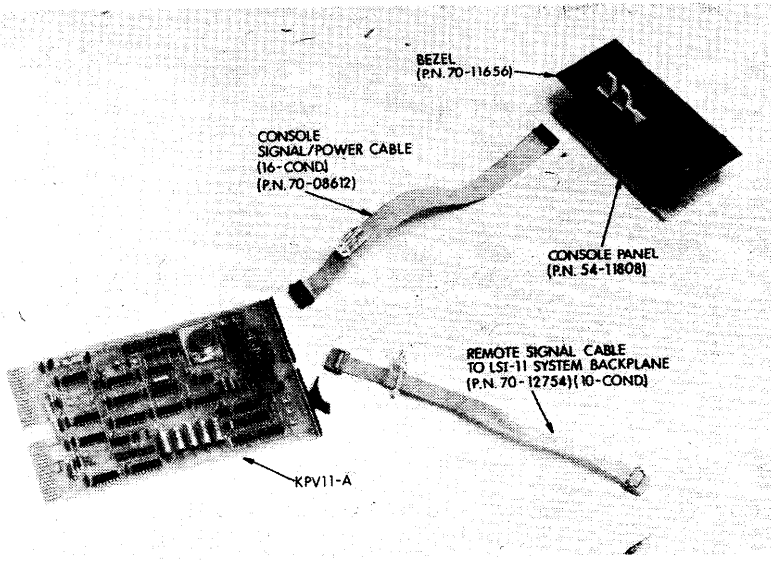


Figure 6 Console Panel, and Interconnection Cables

SPECIFICATION

Environmental

Operating temperature*: 5°C to 50°C (40°F to 122°F)

Relative humidity: 10% to 95% (no condensation)

* When operating at the maximum temperature (50°C or 122°F), air flow must maintain the inlet to outlet air temperature rise across the module to 7°C (12.5°F) maximum.

Electrical

Power requirements:

AC line voltage monitor input: 24 Vac with grounded center tap ±10%, 200 mA

DC operating power: +5 V ±5%, 560 mA

Options

Model/Part No.	Description
54-11808	Console panel (PC assembly)
70-11656	Console bezel
70-12754-2F	Remote signal cable
70-08612-4A	Console signal/power cable

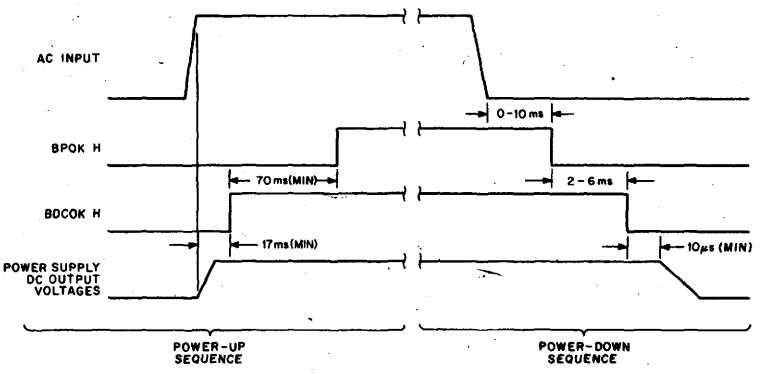
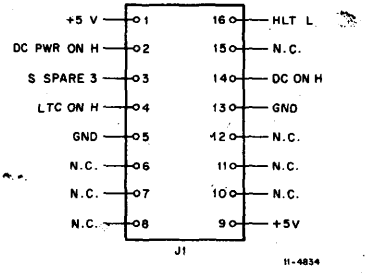


Figure 7 Power Signal Sequence Timing



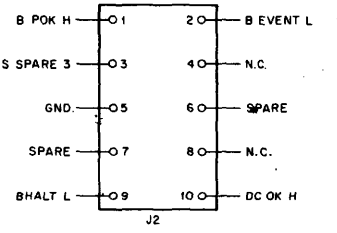


Figure 8 Remote Console (J1) and Backplane Sequel (J2) Connectors

KPV11-B POWER FAIL/LINE TIME CLOCK GENERATOR/TERMINATOR

LSI-11

M SERIES

Length: Extended
Height: Double
Width: Single

DESCRIPTION

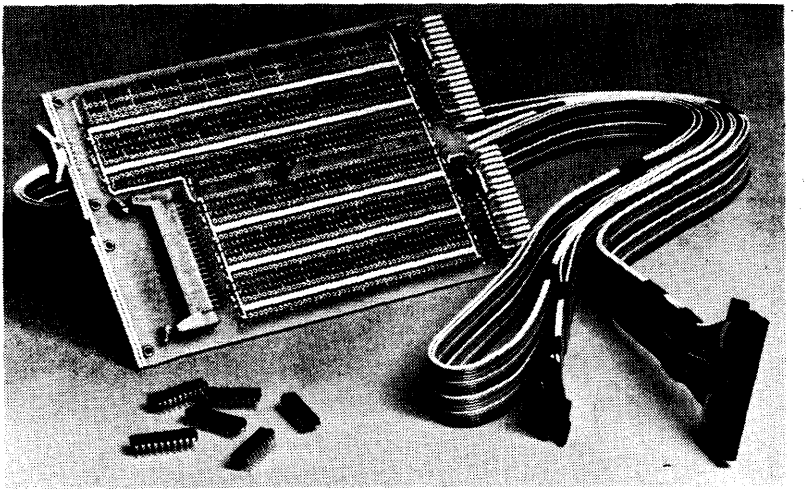
The KPV11-B Module (M8016-YB) is identical to the KPV11-A except that the —B includes 120Ω (nominal) bus termination resistors. Bus terminations are used when expanding the bus beyond the minimum system configuration (a single H9270 Backplane). Having the termination resistors on this module rather than on a separate one optimizes use of bus slots, saving valuable space.

Note that in order to use the bus-termination feature, this option must be installed in the backplane. Mounting the module off the backplane leaves the termination resistors out of the circuit.

DESIGNERS KITS FOR CUSTOM INTERFACES

LSI-11

CHIP KITS



DCK11-AC CHIPKIT includes 6 LSI IC chips, a wire wrappable board, and an interface cable.

The DCK11 series of proprietary LSI integrated circuits, developed by DIGITAL for its own use, is now available to LSI-11 users. These ICs, available in sets called CHIPKITS, make design of LSI-11 bus interfaces easier than ever. Prior to these kits, a designer of custom LSI-11 program control or Direct Memory Access (DMA) interfaces had two alternatives: modify a standard product or design from scratch. Now there is a third choice that will be the best in most cases—the CHIPKIT. The kits contain the ICs needed to build the foundation of nearly any LSI-11 interface, and are available either with or without a DIGITAL wire wrappable board and plug-in cable. For volume users, the individual ICs are available in tubes of 18 of one type.

The CHIPKITS minimize the chip count required to implement bus circuitry. This permits the designer to build an interface foundation on the double-height wire wrappable board provided, and still have ample room left for his special circuitry. The comparatively small chip count results in backplane space savings, increased system reliability, lower system cost, and a greater opportunity for value to be added by the CHIPKIT customer to the finished product.

The CHIPKITS in this program are:

DCK11-AC Designers Program Control Bus Interface CHIPKIT, consisting of:

- 1 DC003 Interrupt Chip
- 1 DC004 Protocol Chip
- 4 DC005 Transceiver/Address Decoder/Vector Select Chips
- 1 W9512 Double-height, extended-length, wire wrappable module
- 1 BC07D-10 ten-foot, 40-conductor plug-in cable

DCK11-AA $80 Program Control Bus Interface CHIPKIT, consisting of the six chips of the above DCK11-AC, but no module or cable.

These kits are ideal for building the foundations of program control bus interfaces to the LSI-11. They are functionally similar to the DRV11-P Bus Foundation Module, an assembled, ready-to-use option described elsewhere in this handbook.

DCK11-AD Designers DMA Bus Interface CHIPKIT, consisting of:

- 1 DC003 Interrupt Chip
- 1 DC004 Protocol Chip
- 4 DC005 Transceiver/Address Decoder/Vector Select Chips
- 2 DC006 Word Count/Bus Address Chips
- 1 DC010 DMA Control Chip
- 1 W9512 Double-height, extended-length, wire wrappable module
- 1 BC07D-10 ten-foot, 40-conductor plug-in cable

DCK11-AB DMA Bus Interface CHIPKIT, consisting of the nine chips of the above DCK11-AD, but no module or cable.

These kits are ideal for building the foundations of DMA bus interfaces to the LSI-11. They are functionally similar to the DRV11-B General Purpose DMA Interface Module, an assembled, ready-to-use option described elsewhere in this handbook.

IMPORTANT NOTE ON DMA CHIPKITS

The two DMA Bus Interface CHIPKITS, DCK11-AB and DCK11-AD, are new products being developed by DIGITAL, and are undergoing final applications testing and review as of the publication date of this handbook—July, 1978. Production quantities are expected about October, 1978. If you have a serious interest in using these CHIPKITS, contact us for the latest word on availability. Write DIGITAL, Logic Products Sales Support, MK 1-2/E13, Merrimack, NH 03054, or call us at the telephone number below.

Detailed specifications of the CHIPKIT components, together with applications suggestions, are in the CHIPKIT Preliminary Applications Note which follows.

Additional Information

To learn more about CHIPKIT applications, pricing, etc., call DIGITAL's toll-free Hot Line, 8:30 AM to 5:00 PM Eastern time: 800-258-1710. From New Hampshire locations, or places outside the continental United States, call Merrimack, 603-884-6660.

CHIPKIT APPLICATIONS NOTE (PRELIMINARY)

LSI-11

CHIPKITS

This Applications Note contains desciptions, specifications, and circuit diagrams for the five integrated circuits available in CHIPKITS for use in LSI-11 bus interfaces. The bus receiver and bus driver chips usually used with the LSI-11 are also covered, and the W9512 wire wrappable module included with the designers kits is described.

Bus Receivers and Bus Drivers

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 1. To perform the receiver and driver functions, DIGITAL Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 1. A typical bus driver circuit is shown in Figure 2. Note that 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package. Bus receiver (8640), bus driver (8881), and bus transceivers (8641) are shown in Figures 3, 4, and 5, respectively. IC 8640 is listed in this handbook as Type 956, and IC 8881 is listed as Type 957.

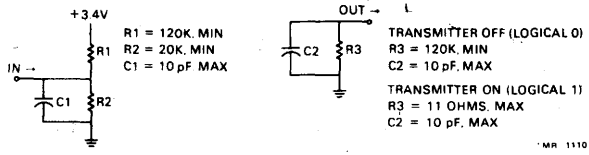


Figure 1 Bus Driver and Receiver Equivalent Circuits

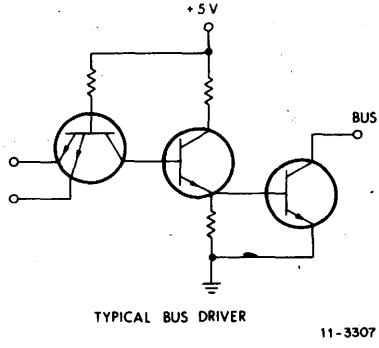


Figure 2 Typical Bus Driver Circuit

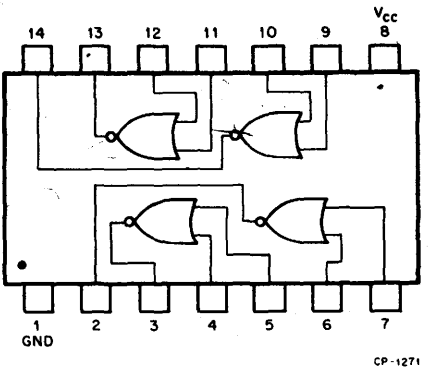


Figure 3 8640 Quad 2-Input NOR Gates
(Bus Receiver)

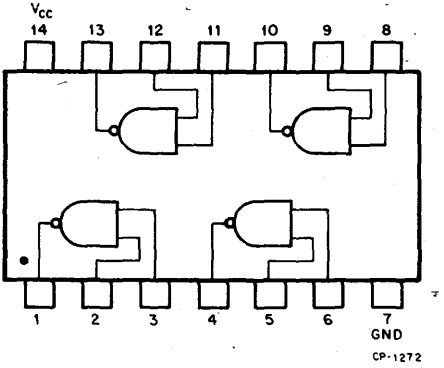


Figure 4 8881 Quad 2-Input NAND Gate
(Bus Driver)

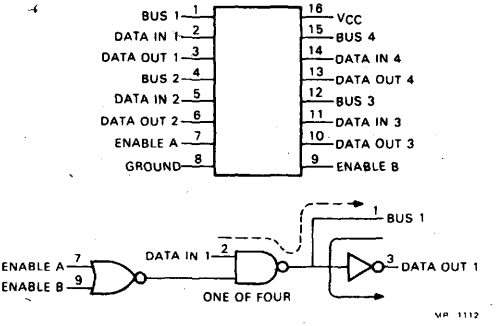


Figure 5 8641 Quad Unified Bus Transceiver
(Bus Receiver/Driver)

Table 1 LSI-11 Bus Driver, Receiver, Transceiver Characteristics

Device	Characteristic	Sym	Specifications	Notes
Receiver	Input high voltage	V_{IH}	1.7 V min	1
(8640)	Input low voltage	V_{IL}	1.3 V max	1
(8641)	Input current at 3.8 V	I_{IH}	80 μA max	1, 3
	Input current at 0 V	I_{IL}	10 μA max	1, 3
	Output high voltage	V_{OH}	2.4 V min	2
	Output high current	V_{OH}	(16 TTL loads)	2, 3
	Output low voltage	V_{OL}	0.4 V max	2
	Output low current	I_{OL}	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min 35 ns max	4, 5
	Propagation delay to low state	TPDL	10 ns min 35 ns max	1, 5
Driver	Input high voltage	V_{IH}	2.0 V min	
(8881)	Input low voltage	V_{IL}	0.8 V max	
(8641)	Input high current	I_{IH}	60 μA max	6
	Input low current	I_{IL}	–2.0 mA max	6
	Output low voltage 70 mA sink	V_{OL}	0.8 V max	1
	Output high leakage current at 3.5 V	I_{OH}	25 μA max	1, 3
	Propagation delay to low state	TPDL	25 ns max	1, 5
	Propagation delay to high state	TPDH	35 ns max	1, 5

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390 Ω to +5 V and 1.6 kΩ in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
5. Times are measured from 1.5 V level on input to 1.5 V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.

Bus receivers and drivers should be well grounded and use V_{CC} to ground bypass capacitors. These gates should be located as close as practical to the module fingers which plug into the backplane and all etch runs to the bus should be kept as short as possible. Attention to these cautions should yield a module design with minimum bus loading (capacitance).

Brief Specifications of CHIPKIT Integrated Circuits

Absolute Maximum Ratings:

Supply Voltage (Vcc)	+7V
Operating Temp. (Ta)	+32°F to +158°F (0°C to +70°C)
Storage Temp. (Ts)	−75° to +257°F (−60°C to +125°C)

Recommended Operating Conditions:

Supply Voltage (Vcc)	4.75V (Min), 5.0V (Norm), 5.25V (Max)
Supply Current (Vcc)	DC003: 140 mA (Max) DC004, DC005: 120 mA (Max) DC006: 160 mA (Max) DC010: 160 mA (Max)
Free Air Temperature	+32°F to +158°F (0°C to +70°C)
Relative Humidity	10% to 95%, noncondensing

Physical Dimensions:

DC003, 18-pin	0.3" center
DC004, 20-pin	0.3" center
DC005, 20-pin	0.3" center
DC006, 20-pin	0.3" center
DC010, 20-pin	0.3" center
W9512 Wire Wrappable Module	Double height, extended length, single width.
BC07D-10 Cable	10', 40-conductor ribbon cable, with 40-pin (female) mating connector (H856) installed on one end only; prestripped on other end.

Detailed specifications, circuit diagrams, pin/signal descriptions, and timing diagrams for each IC follow in this Application Note.

DC003 Interrupt Logic

The interrupt chip is an 18-pin, 0.762 cm center X 2.349 cm long (max) (0.3 in center X 0.925 in long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisy-chain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-current open collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{CC} supply is 140 mA.

Figure 6 is a simplified logic diagram of the DC003 IC. Figure 7 shows the timing for the "A" interrupt section, while Figure 8 shows the timing for both "A" and "B" interrupt sections. Table 2 describes the signals and pins of the DC003 by pin and signal name.

DC004 Protocol Logic

The protocol chip is in a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP device that functions as a register selector, providing the signals to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ± 20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{CC} supply is 120 mA.

Figure 9 is a simplified logic diagram of the DC004 IC. Signal timing with respect to different loads is shown in Table 3 and in Figure 10. Figure 11 shows the loading for the test conditions in Table 3. Signal and pin definitions for the DC004 are presented in Table 4.

DC005 Transceiver Logic

The 4-bit transceiver is a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high-drive (70 mA) open collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tri-state drivers. Data on this port is the logical inversion of the data on the bus side.

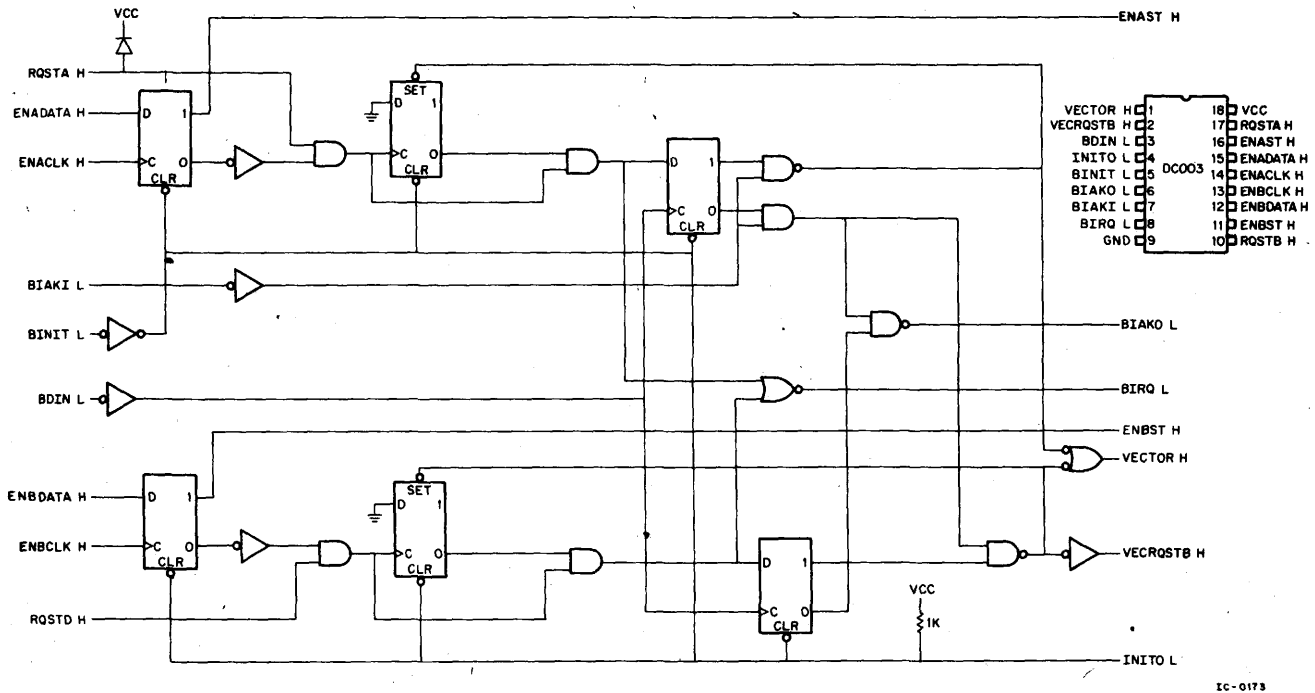


Figure 6 DC003 Simplified Logic Diagram

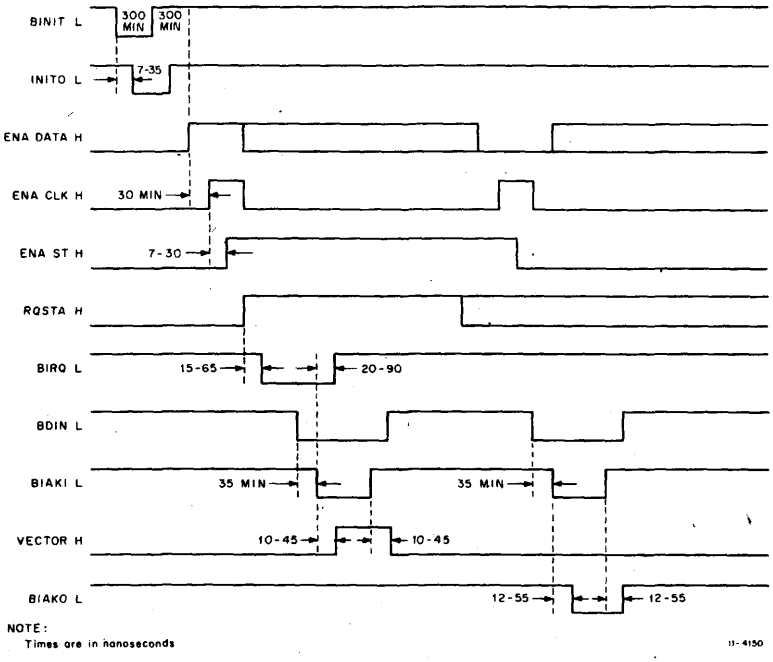


Figure 7 DC003 "A" Interrupt Section Timing Diagram

Table 2 DC003 Pin/Signal Descriptions

Pin	Signal	Group	Description
1	VECTOR H	I	Interrupt Vector Gating. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L.
2	VEC RQSTB H	I	Vector Request "B." When asserted, indicates RQST "B" service vector address is required. When unasserted, indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address; VEC RQST B H is normally bit 2 of the vector address.
3	BDIN L	III	Bus Data In. This signal, generated by the processor BDIN, always precedes a BIAK signal.

Table 2 DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
4	INITO L	I	Initialize Out. This is the buffered BINIT L signal used in the device interface for general initialization.
5	BINIT L	III	Bus Initialize. When asserted, this signal brings all driven lines to their unasserted state (except INITO L).
6	BIAKO L	II	Bus Interrupt Acknowledge (Out). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated.
7	BIAKI L	III	Bus Interrupt Acknowledge (In). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
8	BIRQ L	II	Asynchronous Bus Interrupt Request. This signal is from a device needing interrupt service. The request is generated by a false to true transition of the RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated interrupt enable or the removal of the associated request signal.
10 17	REQSTB H REQSTA H	III III	Device Interrupt Request. When asserted with the enable "A" flip-flop asserted, will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.
11 16	ENB ST H ENA ST H	I I	Interrupt Enable "A" Status. This signal indicates the state of the interrupt enable "A" internal flip-flop which is controlled by the signal line ENA DATA H and the ENA CLK H clock line.

Table 2 DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
12 15	ENB DATA H ENA DATA H	I I	Interrupt Enable "A" Data. The level on this line, in conjunction with the ENA CLK H signal, determines the state of the internal interrupt enable "A" flip-flop. The output of this flip-flop is monitored by the ENA ST H signal.
13 14	ENB CLK H ENA CLK H	I I	Interrupt Enable "A" Clock. When asserted (on the positive edge), interrupt enable "A" flip-flop assumes the state of the ENA DATA H signal line.

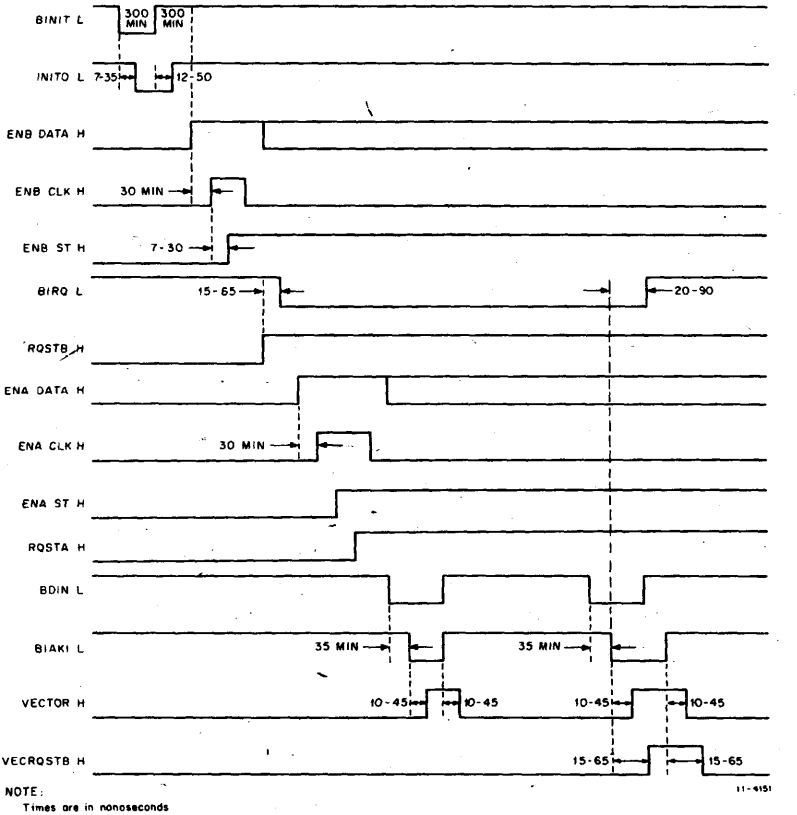


Figure 8 DC003 "A" and "B" Interrupt Sections Timing Diagrams

Table 3 DC004 Signal Timing vs Output Loading

	Signal	With Respect to	Signal	Output Being Asserted (ns) Min	Max	Output Being Negated (ns) Min	Max	Fig. 10 Reference
	SEL (0,2,4,6) L (Load B)		BSYNC L (Load B)	15	40	5	30	T5, T6
	OUTLB L (Load B)		BDOUT L (Load B)	5	30	5	30	T9, T10
	OUTHB L (Load B)		DBOUT L (Load B)	5	30	5	20	T9, T10
	INWD L (Load A)		BDIN L (Load B)	5	30	5	30	T11, T12
Pin 18 Connection RX = 1K ± 5% 330 Ω ± 5% 15 pF ± 5%	BRPLY L (Load A)		OUTLB L (Load B)	20	60	−10	45	T13, T14
	BRPLY L (Load A)		OUTHB L (Load B)	20	60	−10	45	T13, T14
	BRPLY L (Load A)		INWD L (Load B)	20	60	−10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	30	70	0	45	T13, T14

Table 3 DC004 Signal Timing vs Output Loading (Cont)

	Signal	With Respect to	Signal	Output Being Asserted (ns) Min	Max	Output Being Negated (ns) Min	Max	Fig. 10 Reference
Pin 18 Connection RX = 4.64K ± 1%	BRPLY L (Load A)		OUTLB L (Load B)	300	400	−10	45	T13, T14
	BRPLY L (Load A)		OUTHB L (Load B)	300	400	−10	45	T13, T14
CX = 220 pF ± 1%	BRPLY L (Load A)		INWD L (Load B)	300	400	−10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	330	430	0	45	T13, T14
Pin 18 Connection RX = 330 Ω ± 5% C = 15 pF ± 5%	RXCX H		OUTLB L	10	50	10	50	T15, T16
	RXCX H		OUTHB L	10	50	10	50	T15, T16
	RXCX H		INWD L	10	50	10	50	T15, T16
	RXCX H		VECTOR H	10	50	10	50	T15, T16

Table 4 DC004 Pin/Signal Descriptions

Pin	Signal	Group	Description
1	VECTOR H	I	Vector. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H.
2	BDAL2 L	II	Bus Data Address Lines. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
3	BDAL1 L	II	
4	BDAL0 L	II	
5	BWTBT L	II	Bus Write/Byte. While the BDOUT L input is asserted, this signal indicates a byte or word operation: Asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	II	Bus Synchronize. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	II	Bus Data In. This is a strobing signal to effect a data input transaction. Generates INWD L and BRPLY L through the delay circuit and INWD L.
8	BRPLY L	III	Bus Reply. This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or BDOUT L, and BSYNC L and latched ENB H.
9	BDOUT L	II	Bus Data Out. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWD L	I	In Word. Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L.
12	OUTLB L	I	Out Low Byte, Out High Byte. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.
13	OUTHB L	I	

Table 4 DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	I I I I	Select Lines. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted.
18	RXCX	III	External Resistor Capacitor Node. This node is provided to vary the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{CC} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	I	Enable. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

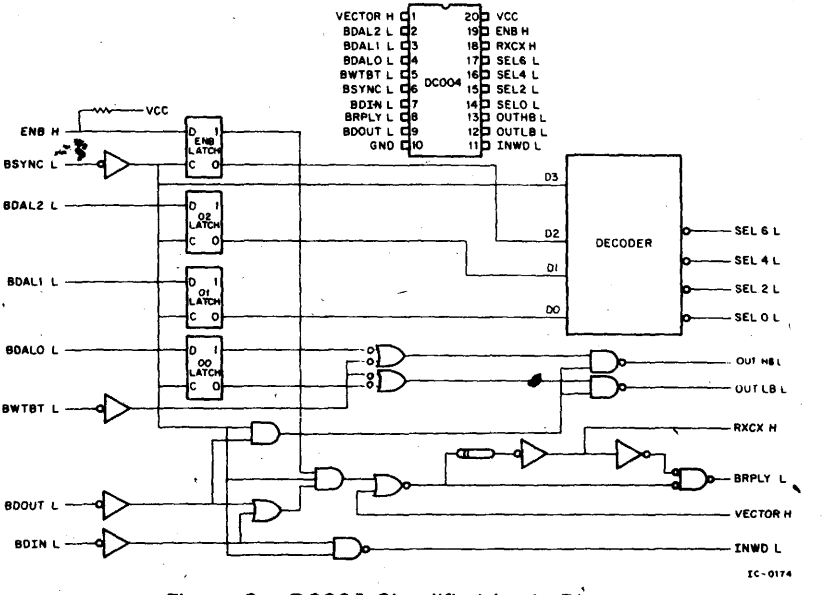


Figure 9 DC004 Simplified Logic Diagram

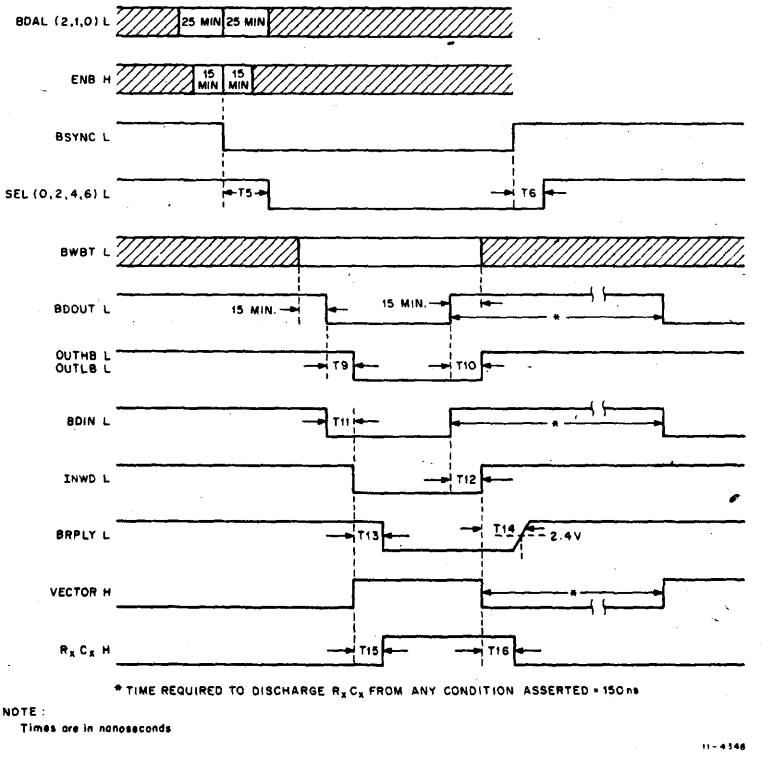


Figure 10 DC004 Timing Diagram

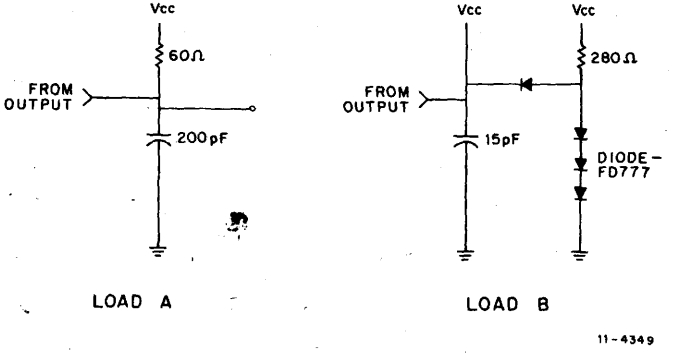


Figure 11 DC004 Loading Configurations for Table 5

Three address "jumper" inputs are used to compare against three bus inputs to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states: receive data, transmit data, and disable.

Maximum current required from the V_{CC} supply is 120 mA.

Figure 12 is a simplified logic diagram of the DC005 IC. Timing for the various functions is shown in Figure 5-13. Signal and pin definitions for the DC005 are presented in Table 5-5.

Table 5 DC005 Pin/Signal Descriptions

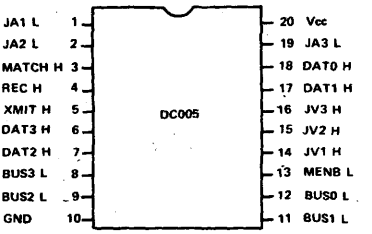
Pin	Signal	Group	Description
	BUS(3:0) L		
12	BUS0	II	Bus Data. This set of four lines constitutes
11	BUS1	II	the bus side of the transceiver. Open col-
9	BUS2	II	lector outputs; high-impedance inputs.
8	BUS3	II	Low = 1.
	DAT(3:0) H		
18	DAT0	I	Peripheral Device Data. These four tri-
17	DAT1	I	state lines carry the inverted received data
7	DAT2	I	from BUS (3:0) when the transceiver is in
6	DAT3	I	the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS (3:0). When in the disabled mode, these lines go open (HI-Z). High = 1.

Table 5 DC005 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
	JV(3:1) H		Vector Jumpers. These inputs, with internal pull-down resistors, directly drive BUS (3:1). A low or open on the jumper pin will cause an open condition on the corresponding bus pin if XMIT H is low. A high will cause a one (low) to be transmitted on the bus pin. Note that BUS0 L is not controlled by any jumper input.
14	JV1	V	
15	JV2	V	
16	JV3	V	
13	MENB L	II	Match Enable. A low on this line will enable the Match output. A high will force Match low, overriding the match circuit.
3	MATCH H	III	Address Match. When BUS (3:1) match with the state of JA (3:1) and MENB L is low, this output is open; otherwise it is low.
	JA(3:1) L		Address Jumpers. A strap to ground on these inputs will allow a match to occur with a one (low) on the corresponding BUS line; an open will allow a match with a zero (high); a strap to V_{CC} will disconnect the corresponding address bit from the comparison.
1	JA1 L	IV	
2	JA2 L	IV	
19	JA3 L	IV	
5	XMIT H	I	Control Inputs. These lines control the operation of the transceiver as follows.
4	REC H	I	

REC	XMIT	
0	0	DISABLE: BUS, DAT open
0	1	XMIT DATA: DAT → BUS
1	0	RECEIVE: BUS → DAT
1	1	RECEIVE: BUS → DAT

To avoid tri-state signal overlap conditions, an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode and delays tri-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.



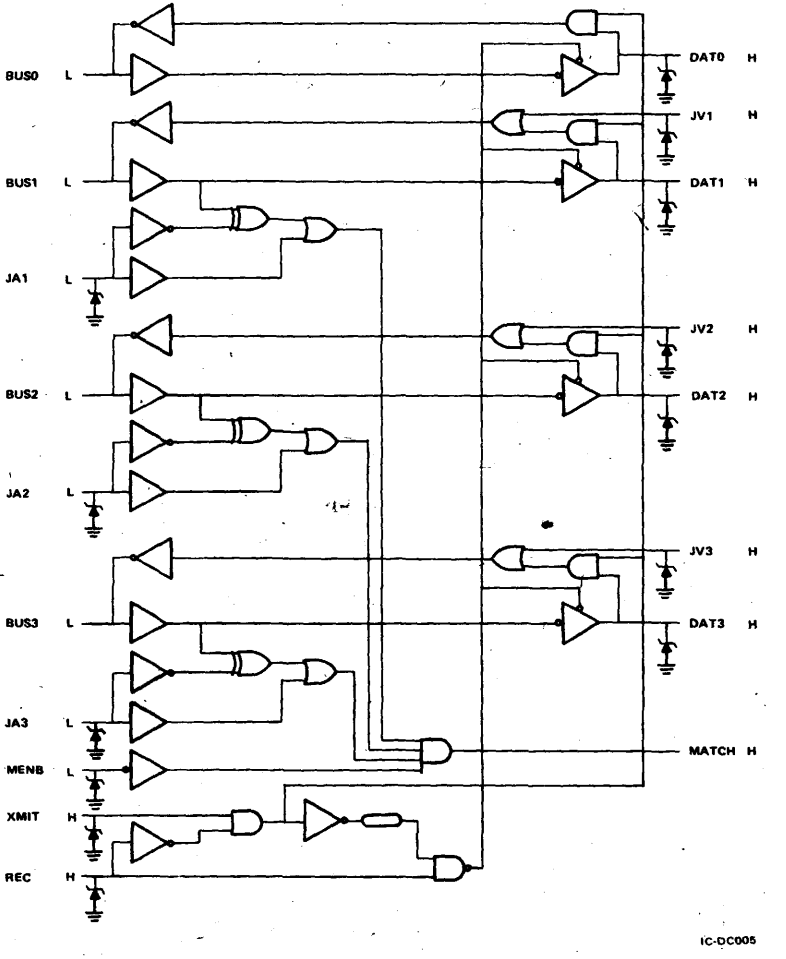


Figure 12 DC005 Simplied Logic Diagram

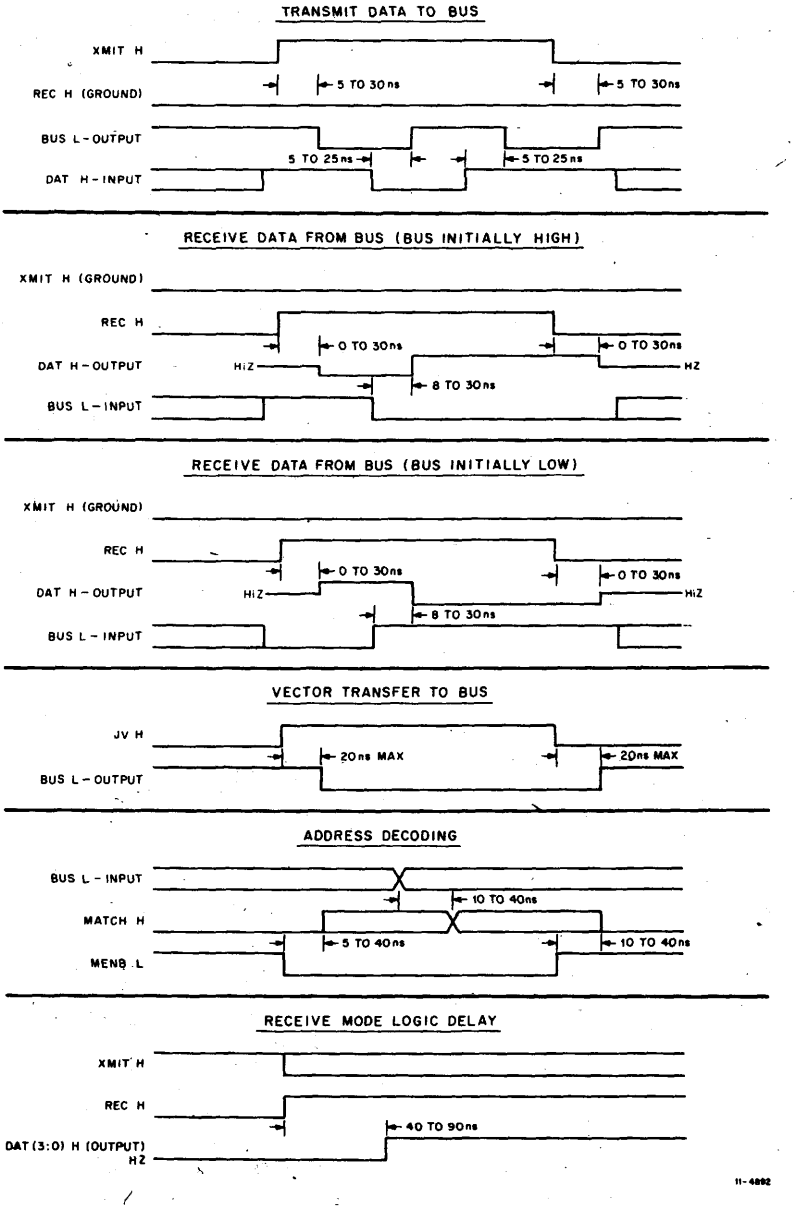


Figure 13 DC005 Timing Diagram

DC006 Word Count/Bus Address Logic

The word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the tri-state side of the DC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (byte) count and another for bus address. Two DC006 ICs may be cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters may be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word byte count) is always incremented by one; the A counter (bus address) may be incremented by one or two for byte or word addressing, respectively.

Data from the DC006 IC is placed on the tri-state bus via internal tri-state drivers. Each counter is separately read by RD and the corresponding select line.

Figure 14 is a block diagram of the DC006 IC while Figure 15 illustrates a simplified logic diagram. Figures 16 and 17 illustrate input and output voltage waveforms. Figure 18 shows the timing diagram of the DC006 while the setup time and pulse width switching characteristics are presented in Tables 6 and 7. The DC006 pin/signal description is presented in Table 8.

Table 6 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min
t_3	Pulse width (min)	S-C to S-A	50 ns
t_5	Setup time	D/F (7:0) to LD	10 ns
t_6	Setup time	S-C to LD	10 ns
t_7	Pulse width (min)	LD	90 ns
t_8	Setup time	S-C to RD	20 ns
t_{11}	Clock pulse width (min)	CLK-C (HI)	40 ns
t_{14}	Setup time	S-C to S-A	20 ns
t_{15}	Setup time	S-A to RD	10 ns
t_{16}	Clock pulse width (min)	CLK-A (HI)	40 ns
t_{18}	Setup time	CNT1A to CLK-A	45 ns
t_{21}	Setup time	RD to RD-A	15 ns
t_{24}	Clock off time (min)	CLK-A, CLK-C	40 ns
t_{25}	Data hold time	LD to DATA IN	20 ns

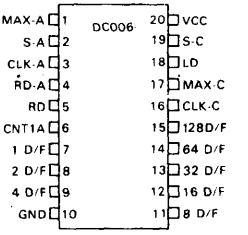
*V_{CC} = 5.0 ± 0.25 V.

TRUTH TABLES

WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE
Z = HIGH IMPEDANCE
. = HIGH TO LOW TRANSITION

READ CONTROL

INPUTS				OUTPUTS
LD – H		S-A	S-C	D/F<7:0>
RD-A	RD			
L	L	L	L	CLEAR A&C AND READ C
L	L	L	H	A<7:0>
L	L	H	L	C<7:0>
L	L	H	H	Z
L	H	X	X	Z
H	L	L	L	CLEAR A&C AND READ A
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	CLEAR A&C AND READ A
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>



WRITE CONTROL

INPUTS			FUNCTION
RD - A = L, RD = H	S-A	S-C	
LD			
↓	L	L	*ILLEGAL
↓	L	H	LOAD A<7:0>
↓	H	L	LOAD C<7:0>
X	H	H	WC/BA NOT SELECTED
H	L	L	CLEAR BOTH COUNTERS
H	L	H	LOADING DISABLED
H	H	L	LOADING DISABLED

* ILLEGAL CONDITION BECAUSE A LOAD OPERATION AND A CLEAR OPERATION IS ATTEMPTED SIMULTANEOUSLY

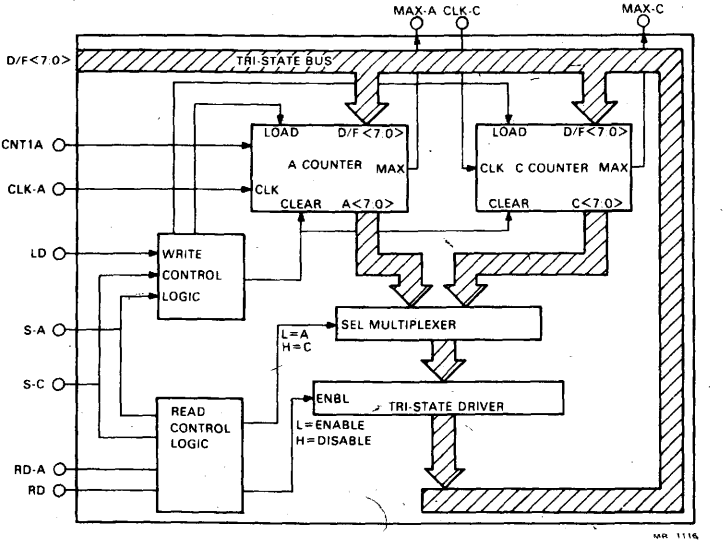


Figure 14 DC006 Truth Table, Logic Diagram, and Simplified Block Diagram

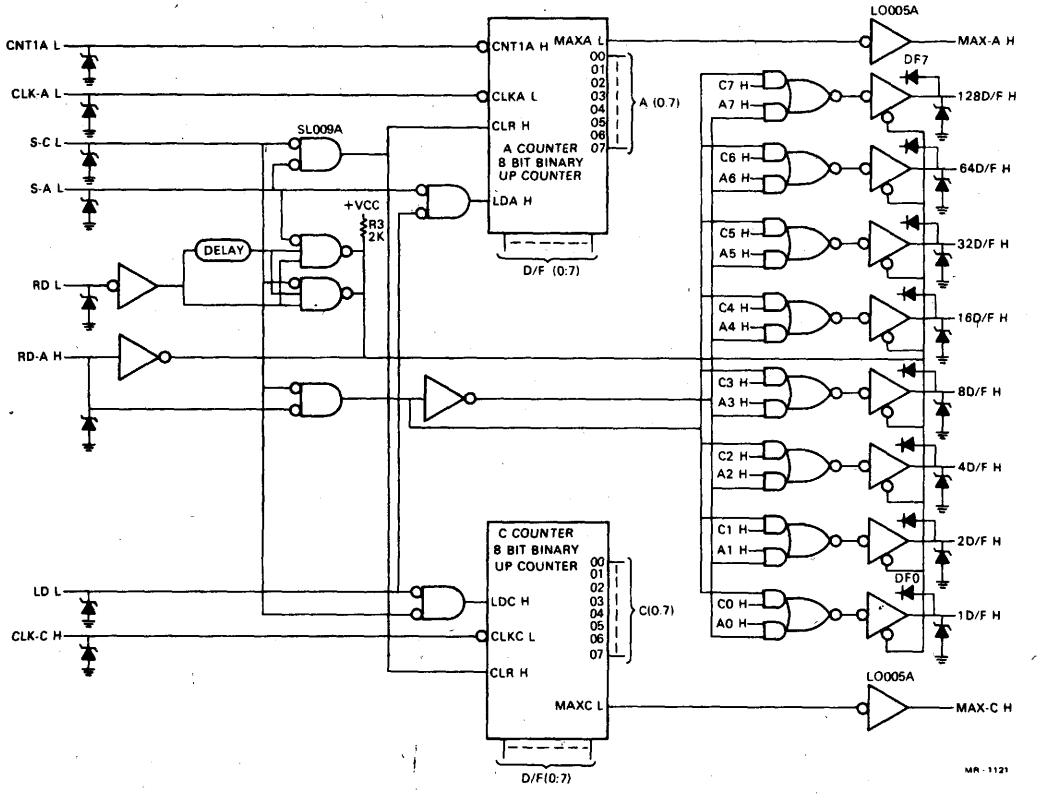


Figure 15 DC006 Simplified Logic Diagram

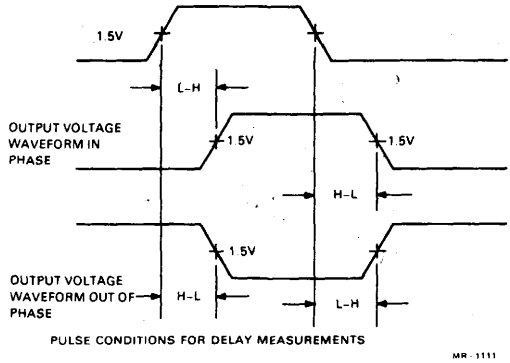
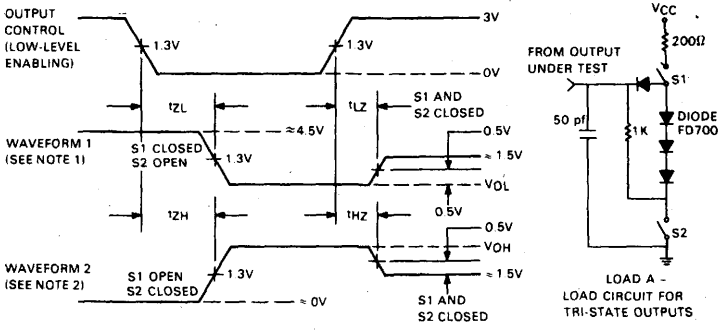


Figure 16 Input Voltage Waveform



NOTES:

1. WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.

2. WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.

Figure 17 Outputs Voltage Waveforms (Tri-State)

Table 7 Switching Characteristics*

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Max
t_1	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A=4 V (C Counter)	15	80
t_2	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A=4 V (A Counter)	15	80
t_4	RD	L-H	D/F (7:0)	D/F (7:0)-Z	Load A	10	30
t_9	RD	H-L	D/F (7:0)	Z-D/F (7:0)	Load A	34	80
t_{10}	CLK-C	H-L	D/F 1	L-H	Load A	18	55
t_{12}, t_{19}	CLK-C CLK-A	L-H	MAX-C MAX-A	L-H	Load B	10	30

*Loads are presented in Figure 10.

Table 7 Switching Characteristics* (Cont)

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Max
t_{13}	CLK-C	H-L	MAX-C	H-L	Load B	10	30
t_{17}	CLK-A	H-L	D/F 2	L-H	Load A	18	55
t_{20}	CLK-A	H-L	MAX-A	H-L	Load B	10	30
t_{22}	RD-A	L-H	D/F (7:0)	Z-L	Load A	10	30
				Z-H	Load A	10	30
t_{23}	RD-A	H-L	D/F (7:0)	L-Z	Load A	8	25
				H-Z	Load A	8	25

*Loads are presented in Figure 10.

Table 8 DC006 Pin/Signal Descriptions

Pin	Signal	Group	Description
6	CNT1A	I	Count A Counter by 1 (TTL Input). This signal controls the least significant bit of the A counter. When CNT1A is low, the A counter increments by one. When high, the LSB is prevented from toggling, hence the counter increments by two. When two counters are cascaded, CNT1A on the high-order counter should be grounded.
3	CLK-A	I	Clock A Counter (TTL Input). This clock signal increments the A counter on its negative edge. The counter is incremented by one or two, depending on CNT1A. CNT1A and LD must be stable while CLK-A is high.
16	CLK-C	I	Clock C Counter (TTL Input). This clock signal increments the C counter by one on its negative edge. LD must be stable while CLK-C is high.
2	S-A	I	Select A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 5-14).
19	S-C	I	Select C Counter (TTL Input). This signal allows the selection of the C counter according to the truth tables (Figure 5-14).
4	RD-A	I	Read A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 5-14).
5	RD	I	Read (TTL Input). This signal allows the read operation to take place according to the truth tables (Figure 5-14).
18	LD	I	Load (TTL Input). When this signal goes through a high-to-low transition, the load operation is allowed to take place according to the truth tables (Figure 5-14). No data changes permitted while LD is low.

Table 8 DC006 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
7–9 11–15	D/F (7:0)	I	Data Bus (Bidirectional, Tri-State Outputs/TTL Inputs). These eight bidirectional lines are used to carry data in and out of the selected counter.
1	MAX-A	I	Maximum A Count (TTL Output). This signal is generated by ANDing CLK-A and the maximum count condition of counter A (count 376 when counting by 2 or count 377 when counting by 1).
17	MAX-C	I	Maximum C Count (TTL Output). This signal is generated by ANDing CLK-C and the maximum count conditions of counter C (count 377).

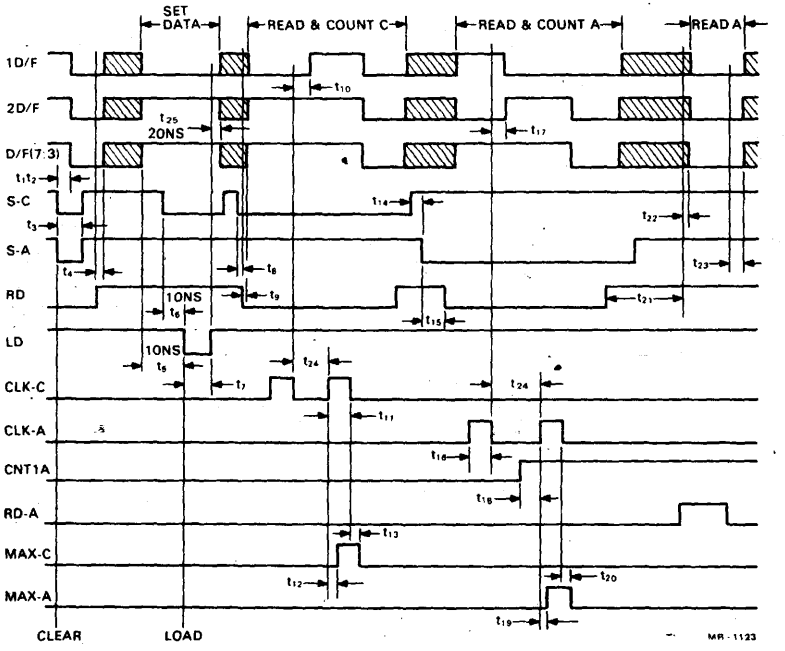


Figure 18 DC006 Timing Diagram

DC010 Direct Memory Access Logic

The direct memory access (DMA) chip is a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP, low-power Schottky device for primary use in DMA peripheral device interfaces using the LSI-11 bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DIN, DOUT, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up bus mastership.

Figure 19 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are presented in Figure 20 and the DC010 voltage waveforms are shown in Figure 21. Table 9 describes the signals and pins of the DC010 by pin and signal name. Figures 22 through 25 show the timing for the DC010 while the setup time and pulse width specifications are listed in Table 10. The switching characteristics are presented in Table 11.

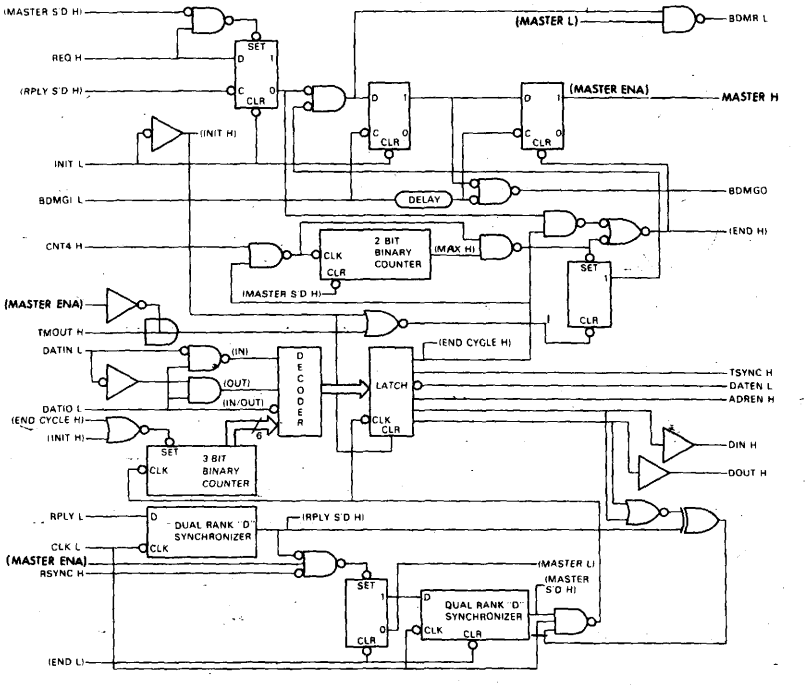


Figure 19 DC010 Simplified Logic Diagram

Table 9 DC010 Pin/Signal Descriptions

Pin	Signal	Group	Description*
1	REQ H	I	Request (TTL Input). A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L		DMA Grant Input (HI-Z Input). A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise, this signal is delayed and output as BDMGO.
16	CNT 4 H	I	Count Four (TTL Output). A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open, this pin will assume a high state.
14	TMOUT H	I	Time-Out (TTL Input/Open Collector Output). This I/O pin is low while SACK H is high. It goes into high impedance when SACK H is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been negated due to the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	I	Data In (TTL Input). This signal allows the selection of the type of transfers to take place according to the truth table (Figure 5-20).
2	DATIO L	I	Data In/Out (TTL Input). This signal allows the selection of the type of transfer to take place according to the truth table (Figure 5-20). During a DATIO transfer, this signal must be toggled in order to allow the completion of the output portion of the I/O transfer. If left open, this pin will assume a high state.

*Refer to Figures 22 through 25.

Table 9 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description*
12	RSYNC	I	Receive Synchronize (TTL Input). This signal allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
17	CLK L	I	Clock (TTL Input). This clock signal is used to generate all transfer timing sequences.
15	RPLY H	I	Reply (TTL Input). This signal is used to enable or disable the free clock signal according to the truth table (Figure 5-20). This signal also allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
19	INIT L	I	Initialize (TTL Input). This signal is used to initialize the chip to the state where REQ is needed to start a bus request transaction. When INIT is low, the following signals are negated; BDMRL, MASTER H, DATENL, ADRENL, SYNCH, DINH, DOUTH.
11	BDMR L	I	DMA Request (Open Collector Output). A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	I	Master (TTL Output). A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.
8	BDMGO L	I	DMA Grant Output (Open Collector Output). This signal is the delayed version of BDMGI if no request is pending; otherwise, it is not asserted. This output may be tied directly to the bus.

*Refer to Figures 22 through 25.

Table 9 DC010 Pin/Signal Descriptions (Cont)

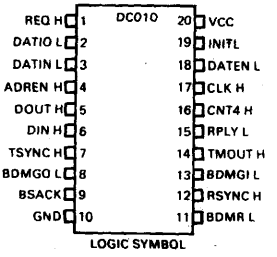
Pin	Signal	Group	Description*
7	TSYNC H	I	Transmit Synchronize (TTL Output). This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	I	Data Enable (TTL Output). This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	I	Address Enable (TTL Output). This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	I	Data In (TTL Output). This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	I	Data Out (TTL Output). This signal is asserted to indicate that the bus master device has output valid data.

*Refer to Figures 22 through 25.

Table 10 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min	Max
t_1	Pulse width (min)	INIT	35 ns	
t_4	Setup time	INIT to REQ.	25 ns	
t_6	Setup time	BDMR to BDMGI	35 ns	
t_9	Setup time	BDMR to BDMGI	0 ns	
t_{12}	Pulse width (min)	CLK (low)	60 ns	
t_{13}	Pulse width (min)	CLK (high)	60 ns	
t_{14}	Setup time	REQ to CLK	35 ns	
t_{18}	Setup time	DIN to RPLY	0 ns	
t_{22}	Setup time	DATIN, DATIO to CLK	60 ns	
t_{24}	Setup time	RPLY to CLK	30 ns	
t_{28}	Setup time	RPLY to DATIO	35 ns	
t_{29}	Pulse width	DATIO	30 ns	1 clock period
t_{30}	Setup time	DATIO to CLK	65 ns	
t_{32}	Pulse width (min)	REQ	35 ns	

*V_{CC} = 5.0 ± 0.25 V



TRUTH TABLE

WHERE: L = TTL LOW
H = TTL HIGH
X = DON'T CARE

INPUTS		TRANSFER TYPE
DATIN	DATIO	
X	L	DATIO
L	H	DIN
H	H	DOUT

MR-1115

Figure 20 DC010 Logic Symbol/Truth Table

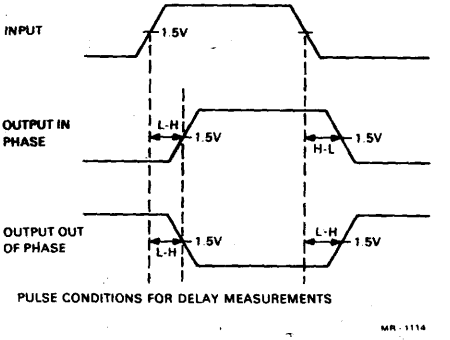


Figure 21 DC010 Voltage Waveforms

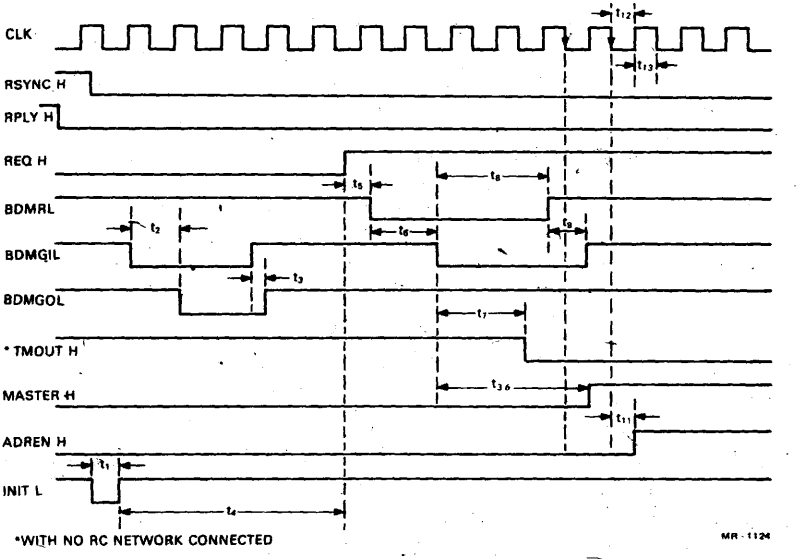


Figure 22 DC010 Timing Diagram, DMA Request/Grant

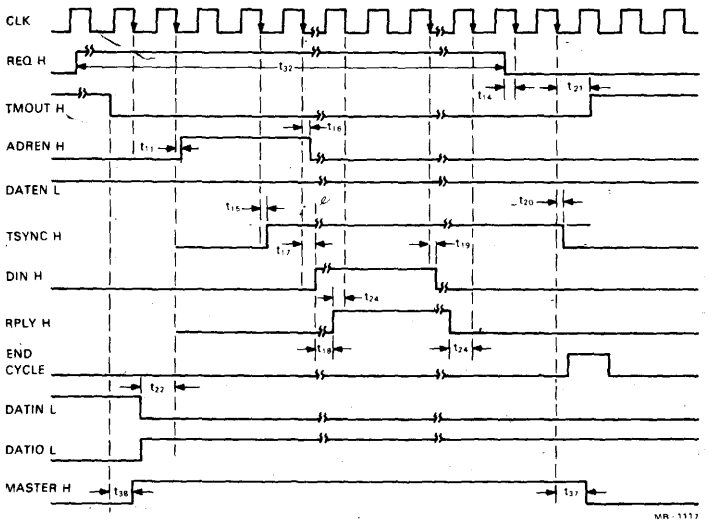


Figure 23 DC010 Timing Diagram (Sheet 1 of 2)

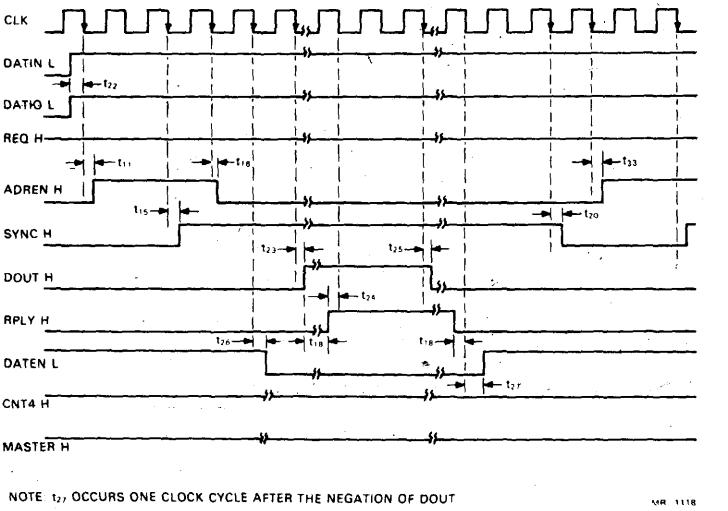


Figure 23 DC010 Timing Diagram (Sheet 2 of 2)

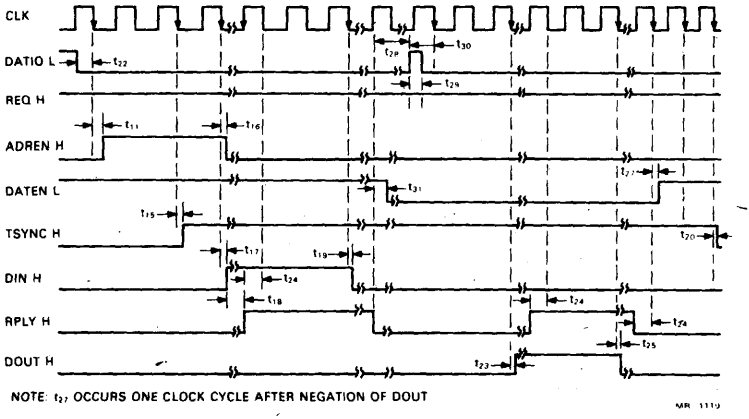


Figure 24 DC010 Timing Diagram (DATIO–Multiple Transfer)

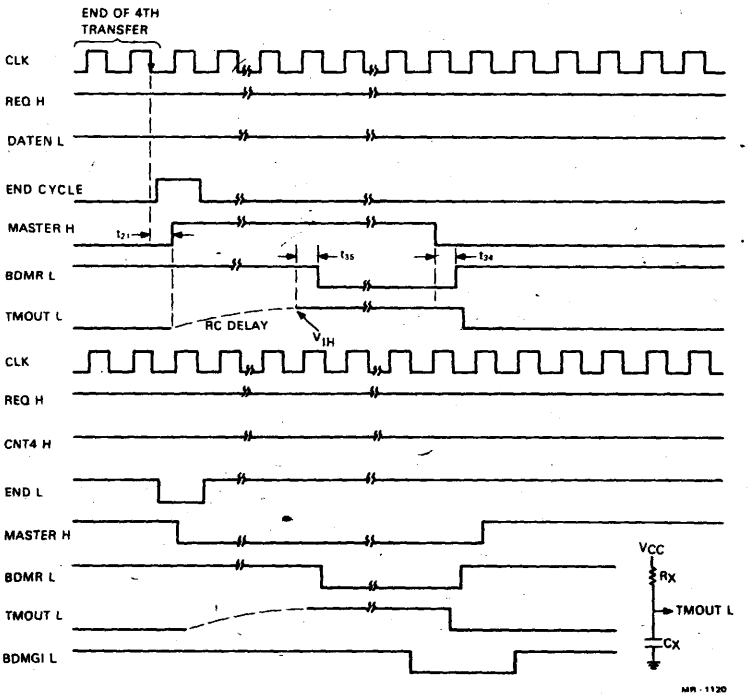


Figure 25 DC010 Timing Diagram (Time-Out)

Table 11 Switching Characteristics

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_2	BDMGI	H-L	BDMGO	H-L	Load A	95	220
t_3	BDMGI	L-H	BDMGO	L-H	Load A	20	60
t_5	REQ	L-H	BDMR	H-L	Load A	25	70
t_7	BDMGI	H-L	TMOUT	H-L	Load A	85	230
t_8	BDMGI	H-L	BDMR	L-H	Load A	117	306
t_{11}*	CLK	H-L	ADREN	L-H	Load B	15	60
t_{15}	CLK	H-L	SYNC	L-H	Load B	18	60†
t_{16}	CLK	H-L	ADREN	H-L	Load B	20	65†
t_{17}	CLK	H-L	DIN	L-H	Load B	18	60†
t_{19}	CLK	H-L	DIN	H-L	Load B	18	60
t_{20}	CLK	H-L	SYNC	H-L	Load B	18	60
t_{21}	CLK	H-L	TMOUT	L-H	Load B	30	90
t_{23}	CLK	H-L	DOUT	L-H	Load B	60	175
t_{25}	CLK	H-L	DOUT	H-L	Load B	20	65†
t_{26}	CLK	H-L	DATEN	H-L	Load B	20	65†

T_{11} represents the first time ADREN is asserted.
t_{33} represents the subsequent times that ADREN is asserted.

†These propagation delays meet the following requirements.

$t_{15}-t_{16} \leq 10$ ns
$t_{15}-t_{17} \leq 10$ ns
$t_{16}-t_{26} \leq 10$ ns
$t_{25}-t_{27} \leq 20$ ns
$t_{23}-t_{26} \leq 45$ ns
$t_8-t_{36} \geq 27$ ns

Table 11 Switching Characteristics (Cont)

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_{31}	RPLY	H-L	DATEN	H-L	Load B	20	65
t_{27}	CLK	H-L	DATEN	L-H	Load B	20	65†
t_{33}*	CLK	H-L	ADREN	L-H	Load B	18	60
t_{35}	TMOUT	L-H	BDMR	H-L	Load B	20	75
t_{36}	BDMGI	H-L	MASTER	L-H	Load B	90	242
t_{37}	CLK	H-L	MASTER	H-L	Load B	18	66
t_{38}	R SYNC or REPLY	H-L	MASTER	L-H	Load B	10	58

*t_{11} represents the first time ADREN is asserted.
t_{33} represents the subsequent times that ADREN is asserted.

†These propagation delays meet the following requirements.

$t_{15}-t_{16} \leqslant 10$ ns
$t_{15}-t_{17} \leqslant 10$ ns
$t_{16}-t_{26} \leqslant 10$ ns
$t_{25}-t_{27} \leqslant 20$ ns
$t_{23}-t_{26} \leqslant 45$ ns
$t_{8}-t_{36} \geqslant 27$ ns

Specifications

DC003 Electrical Characteristics

DC003 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current: at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V[2]		50	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V[3]		−0.55	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[4,5]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		140	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

[2]I_{IH} = 100 μA at pins 12 and 15.

[3]I_{IL} = −2.0 mA at pins 12 and 15.

[4]Not more than one output shall be shorted at a time and duration shall not exceed 1 second.

[5]Does not apply to pin 4.

DC003 Bus Driver
(Specification Group II – Open Collector)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
Output reverse current	I_{OR}	V_{CC} = 4.75 V V_{OH} = 3.5 V		25	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_{SINK} = 70 mA I_{SINK} = 16 mA		0.8 0.5	V V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC003 Bus Receiver
(Specification Group III – High Input Z)

Parameters			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V V_{CC} = 5.25 V	1.53 1.70		V V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V V_{CC} = 5.25 V		1.30 1.47	V V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA I_I = +18 mA (pins 10 and 17 only)		−1.2 6.25	V V
High-level input current	I_{IH}	V_I = 3.8 V V_{CC} = 0 V (Do not do for pins 10 and 17) V_{CC} = 5.25 V		40 40	μA μA
Low-level input current	I_{IL}	V_I = 0 V V_{CC} = 0 V (Do not do for pins 10 and 17) V_{CC} = 5.25 V		−10 −10	μA μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V[2]		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V[2]		50	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V		−0.70	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[3]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		120	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Limits for pin 19 are:
I_I = 1.40 mA; I_{IH} = −2.25 mA min, −3.85 mA max.
I_{IL} = −4.5 mA min, −800 mA max.
[3]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC004 Bus Receiver
(Specification Group II – High Input Z)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V	1.53		V
		V_{CC} = 5.25 V	1.70		V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V		1.30	V
		V_{CC} = 5.25 V		1.47	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = –18 mA		–1.2	V
High-level input current	I_{IH}	V_I = 3.8 V			
		V_{CC} = 0 V		40	μA
		V_{CC} = 5.25 V		40	μA
Low-level input current	I_{IL}	V_I = 0 V			
		V_{CC} = 0 V		–10	μA
		V_{CC} = 5.25 V		–10	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC004 Bus Driver
(Specification Group III – Open Collector)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
Output reverse current	I_{OH}	V_{CC} = 4.75 V V_{OH} = 3.5 V		25[2]	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V			
		I_{SINK} = 70 mA[3]		0.8	V
		I_{SINK} = 16 mA[3]		0.5	V
		I_{SINK} = 15 mA[4]		0.5	V

[1]Ambient operating temperature (T_A) = 0° to 70° C unless otherwise specified.

[2]65 μA for pin 18 (RXCX H).

[3]Applies to Pin 18 BUS RPLY only.

[4]Applies to Pin 18 RXCX only.

DC005 Electrical Characteristics

DC005 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	3.65		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V REC XMIT		 100 50	 μA μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V REC XMIT		 −2.2 −1.1	 mA mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[2]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		120	mA
Off state (high-impedance state) output current (DAT pins only)	$I_{O\ (OFF)}$	V_{CC} = 5.25 V V_I = 3.65 V V_I = 0.5 V		 100 −0.36	 μA mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC005 Bus Receiver
(Specification Group II – High Input Z)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V	1.53		V
		V_{CC} = 5.25 V	1.70		V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V		1.30	V
		V_{CC} = 5.25 V		1.47	V
Input clamp voltage	V_I	I_I = –18 mA, V_{CC} = 4.75 V		–1.2	V
High-level input current (includes open-collector leakage on bus pins)	I_{IH}	V_I = 3.8 V			
MENB		V_{CC} = 0 V		40	μA
		V_{CC} = 5.25 V		40	μA
BUS		V_{CC} = 0 V		65	μA
		V_{CC} = 5.25 V		65	μA
Low-level input current	I_{IL}	V_I = 0.5 V, V_{CC} = 0 V		–10	μA
		V_{CC} = 5.25 V		–10	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 Bus Driver
(Specification Group III – Open Collector)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level output current (reverse current – match output only[2]	I_{OH}	V_{CC} = 4.75 V, V_{OH} = 5.25 V		25	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V, I_{SINK} = 8 mA (Match)		0.5	V
		I_{SINK} = 70 mA (Bus)		0.8	V
		I_{SINK} = 16 mA (Bus)		0.5	V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

[2]For bus pins, see I_{IH} under specification group II.

DC005 (Specification Group IV – Ternary State Inputs)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
Low-level input voltage	V_{IL}			0.3	V
High-level input voltage	V_{IH}		4.75		V
Open circuit input voltage	V_{OP}	$4.75 < V_{CC} < 5.25$	1	2	V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 (Specification Group V – TTL Input with Pull-Down)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V −18 mA		−1.2	V
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.4 V		1.2	mA
Low-level input voltage forcing input current	V_{II}	V_{CC} = 4.75 V I_I = 0.1 mA		0.8	V
Input current at low-level	I_{IL}	V_{CC} = 5 V V_I = 0.4 V	50	200	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC006 Electrical Characteristics

DC006 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = Open I_I = –18 mA		–1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = –1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V			
Except tri-state				50	μA
Tri-state pin				55	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V			
CLKA, CLKC				–1.1	mA
CTNTIA				–1.7	mA
D/F(7:0)LD,RD, SC,SA				100	μA
RD-A				200	μA
Off-state high impedance state – output current tri-state only	$I_{O\ (OFF)}$	V_{CC} = 5.25 V V_O = 3.75 V		100	μA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[2]	–40	–100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		150	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C; V_{CC} = 5.0 ± 0.25 unless otherwise specified.

[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC010 Electrical Characteristics

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}		2.0		V
		V_{CC} = 4.75 V	1.53		V
		V_{CC} = 5.25 V	1.70		V
Low-level input voltage	V_{IL}			0.8	V
		V_{CC} = 4.75 V		1.30	V
		V_{CC} = 5.25 V		1.47	V
Input clamp voltage	V_I	V_{CC} = open I_I = −18 mA		1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = 1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V			
		I_O = 8 mA		0.5	V
		I_O = 70 mA		0.8	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1.0	mA
				1.5	mA
		V_{CC} = 0 to 5.25 V V_I = 3.8 V		40	μA
				65	μA
High-level input current	I_{IH}	V_{CC} = 5.25 V[3]			
		V_I = 2.7 V		50	μA
		V_I = 2.7 V[4]		300	μA
		V_I = 3.8 V		40	μA
		V_I = 3.8 V		65	μA
Low-level input current	I_{IL}	V_I = 0.5 V[3]			
		V_{CC} = 5.25 V		−1.4	mA
		V_{CC} = 5.25 V		−2.0	mA
		V_{CC} = 5.25 V		−10	μA
		V_{CC} = 5.25 V		−10	μA
Output leakage current	I_{OH}	V_{CC} = 4.75 V V_O = 5.25 V		25	μA
Short-circuit output current[2]	I_{OS}	V_{CC} = 5.25 V	15	60	mA
Supply current	I_{CC}	V_{CC} = 5.25 V	130	160	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.
[3]Except CNT4, DATIO.
[4]CNT4, DATIO.

TYPICAL APPLICATION

Figures 26, 29, and 30 show a typical application for the DC003, DC004, DC005, DC006, and DC010 integrated circuits. Figure 26 shows the LSI-11 bus interface circuits; Figure 29 depicts the DMA control, word count/bus address registers, and the output buffers; Figure 30 shows miscellaneous logic.

DC003, DC004, DC005 Application

Referring to Figure 26, four DC005 transceivers are used to handle the first 16 BDAL lines (BDAL 0–BDAL15) from the LSI-11 bus and to provide the interface to the internal tri-state bus. The transceivers are enabled to receive data from the LSI-11 bus when the REC H line is driven high. Similarly, the transceivers transmit data to the LSI-11 bus when the XMIT H line is driven high. Normally, the DC005s are in the receive state (REC H line asserted) and allow the transceivers to monitor the LSI-11 bus for device addresses.

Device address and vector switch inputs to the transceivers provide convenient address and vector selection.

Switches A3 through A12 are the device address selection switches, and switches V3 through V8 are for vector selection. Switches are ON (closed) for a 1 bit and are OFF (open) for a 0 bit. The switch settings for the device addresses and vector are shown in Figures 27 and 28 respectively. The addressable registers are:

Register	Bank 7 Octal Address
Bus Address Register	1XXXX0
Word Count Register	1XXXX2
Control/Status Register	1XXXX4
Output Buffers	1XXXX6

The user selects a base address for the bus address register and sets the device address selection switches to decode this address. The remaining register addresses are then properly decoded as sequential addresses beyond the bus address register.

The DC004 is the internal register selector. This integrated circuit monitors BDAL lines 0, 1, and 2 to determine which register address has been placed on the LSI-11 bus. The states of BDOUT and BDIN are also monitored to determine the type of transfer (DATO or DATI). When an address for an internal register is placed on the LSI-11 bus, one of the SEL outputs from the DC004 is driven low. This selects that particular register for the transfer of data. The direction of transfer (into or out of

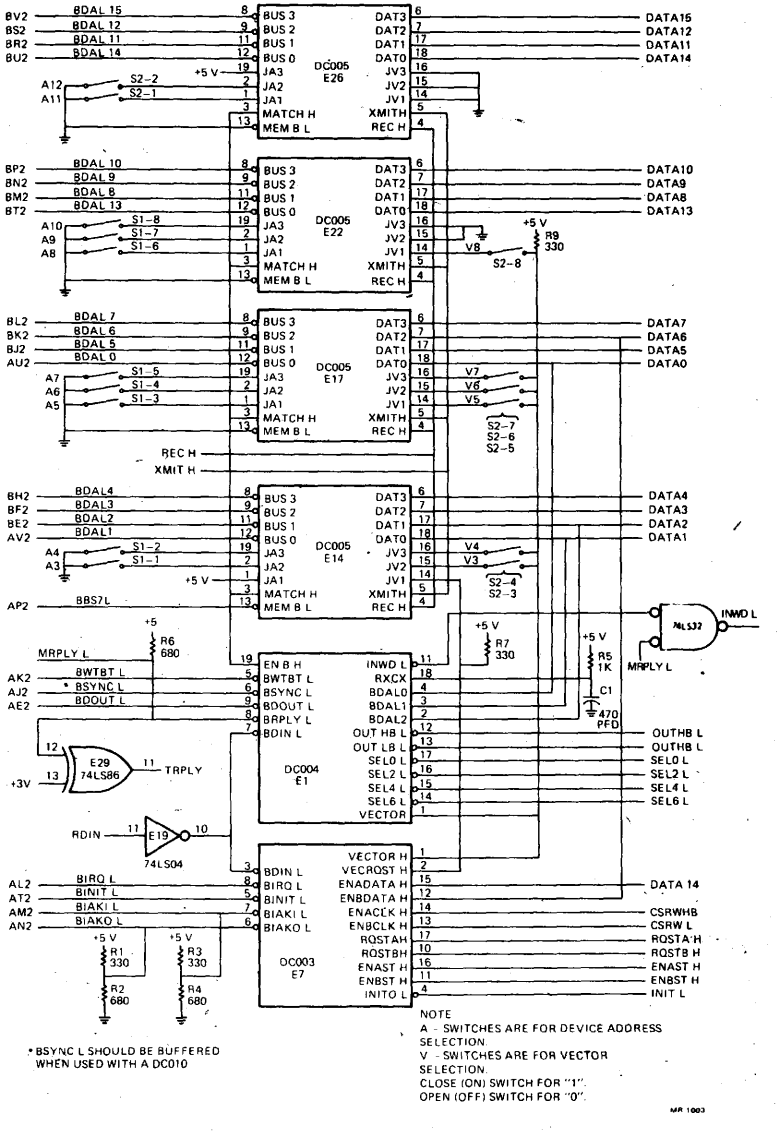


Figure 26 Typical Application (DC003, DC004, DC005)

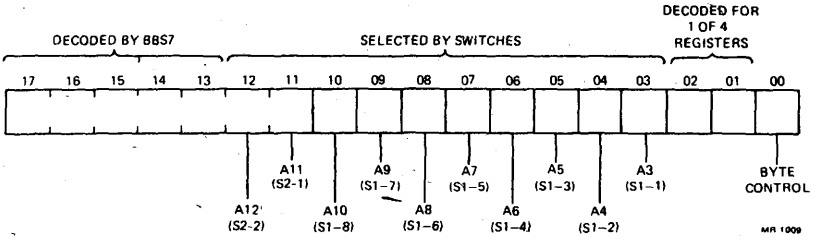


Figure 27 Device Address Select Format

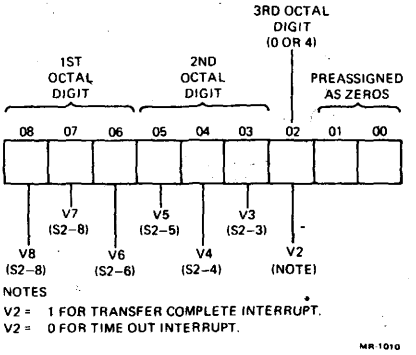


Figure 28 Interrupt Vector Select Format

the master device) is determined by the state of the OUTHB L, OUTLB L, or INWD L lines. Internal register selection is summarized as follows:

Control Line	Select	Register
INWD L (Read)	SEL 0 L	Bus Address Register
INWD L (Read)	SEL 2 L	Word Count Register
OUTHB L (Write High Byte)	SEL 0 L	Bus Address Register
OUTHB L (Write High Byte)	SEL 2 L	Word Count Register
OUTLB L (Write Low Byte)	SEL 0 L	Bus Address Register
OUTLB L (Write Low Byte)	SEL 2 L	Word Count Register
INWD L (Read)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write CSR High Byte)	SEL 4 L	Control/Status Register
OUTLB L and MRPLY L (Write CSR Low Byte)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write High Byte)	SEL 6 L	Output Buffer
OUTLB L and RMPLY L (Write Low Byte)	SEL 6 L	Output Buffer

Note that MRPLY L is the BRPLY L output of the DC004 and is used along with OUTHB L and OUTLB L to write either the high or low byte in the control/status register or the output buffers. Write byte selection for the bus address register and the word count register is controlled only by the OUTHB L and OUTLB L lines. Words can be written to the control/status register or the output buffer registers by driving both OUTHB L and OUTLB L to the low state at the same time.

The DC004 integrated circuit is designed to operate directly from the LSI-11 bus. However, since the introduction of the DC005, the DC004 is usually interfaced to the LSI-11 bus through the DC005. Bus signals (BDAL lines) passing through the DC005 are inverted. Therefore, BDAL 0, 1, and 2 signals applied to the DC004 are inverted. Because of this inversion, it is necessary to change the nomenclature on pins 12 through 17 on the DC004. The difference in nomenclature between DC004s operated directly from the LSI-11 bus and through a DC005 are as follows.

From Bus (Non-Inverted BDAL 0, 1, 2)		**From DC005 (Inverted BDAL 0, 1, 2)**	
Pin	**Signal**	**Pin**	**Signal**
12	OUTLB L	12	OUTHB L
13	OUTHB L	13	OUTLB L
14	SEL 0 L	14	SEL 6 L
15	SEL 2 L	15	SEL 4 L
16	SEL 4 L	16	SEL 2 L
17	SEL 6 L	17	SEL 0 L

It is recommended that when a DC005 is used, the DC004 be interfaced to the LSI-11 bus through the DC005 to avoid unnecessary bus loading.

The DC003 IC performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DC003 has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the DC003 must be set. This is accomplished by asserting (logic 1) the ENB DATA line to the DC003 (writing bit 14 or bit 6 to a one) and then clocking the enable flip-flop by asserting (positive transition) the DC003 ENB CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logic 1) RQST. RQST must be held asserted until the interrupt is serviced. When the RQST is asserted and the interrupt enable flip-flop is set, the DC003 asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L. This causes the DC003 to assert (logic 1) VECTOR H, which is applied to the DC005. VECTOR H at the DC005 causes the device vector to be placed on the BDAL lines to the processor. Interrupts are produced for bus time-outs (CSR bits 15 and 14) and at the completion of a block transfer (CSR bits 7 and 6).

DMA Application

Figure 29 shows the DMA control (DC010), the word count/bus address registers (both DC006), the output buffers (both 74LS273s), and the input drivers (74LS367s).

The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA non-processor request (NPR) data transfers. After becoming bus master, the DC010 produces the signals necessary to perform a DIN, DOUT, or DATIO bus cycle as specified by the control lines. An 8-MHz free-running clock is provided by E8. This clock is used by the DC010 to generate all transfer timing sequences. The actual clock frequency is not critical and can be any frequency up to 8.3 MHz. An RC time constant provided by resistor R14 and capacitor C2 provides a delay for the reassertion of BDMR to the LSI-11 bus. This allows other direct memory access devices to obtain the bus during the time the CNT4 logic releases the bus and re-requests the bus.

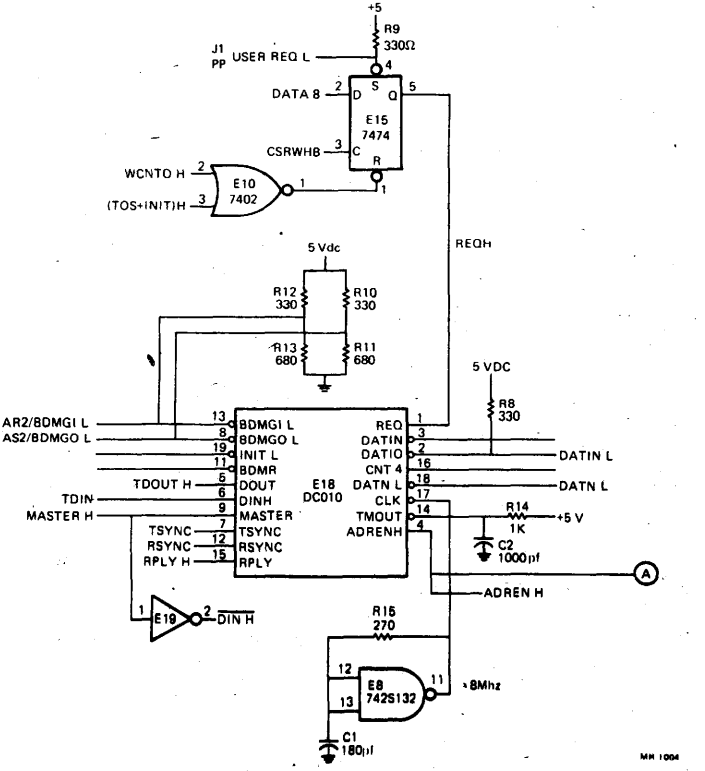


Figure 29 Typical Application (DC006, DC010, Output Delay, and Input Drives) (Sheet 1 of 2)

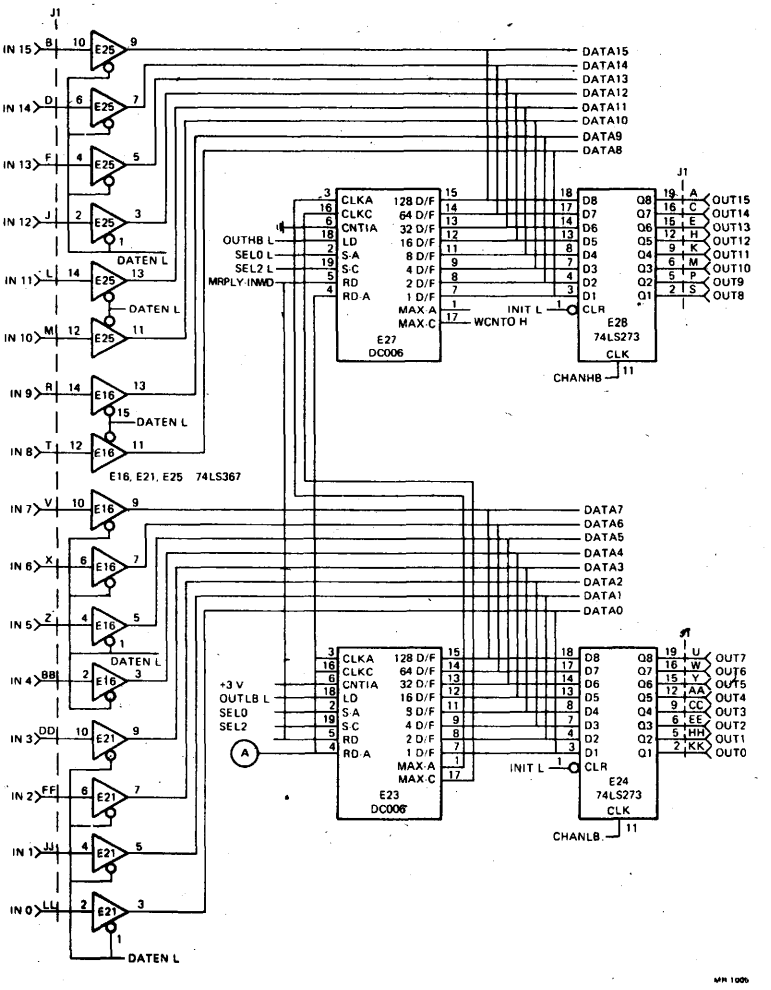


Figure 29 Typical Application (DC006, DC010, Output Delay, and Input Drives) (Sheet 2 of 2)

User devices initiate bus requests by driving the set input of the request flip-flop (E15) low. This asserts REQ to the DC010 and generates BDMR L to the LSI-11 bus. When the DC010 becomes bus master, it asserts ADREN H to the DC010 bus address registers. ADREN H allows the bus address registers to place the address of the slave (memory) onto the internal bus and, via the DC005 transceivers, onto the LSI-11 bus. The request flip-flop (E15) remains set until the DC006 word count overflows to zero (WCNT0). WCNT0 then resets the request flip-flop.

Two DC006 word count/bus address register ICs are used to provide 16 bits each of word count and bus address. The least significant bits of the word count and bus address are provided by DC006/E23; the most significant bits are provided by DC006/E27. Register A is the bus address register and register C is the word count register. Both registers can be read or written under program control from the LSI-11 bus. Registers are selected by:

• Read bus address register	SEL 0 L INWD L
• Write high byte of bus address register	SEL 0 L OUTHB L
• Write low byte of bus address register	SEL 0 L OUTLB L
• Read word count register	SEL 2 L OUTHB L
• Write high byte of word count register	SEL 2 L INWD L
• Write low byte of word count register	SEL 2 L OUTHB L

The bus address register is incremented by 2 for word transfers. To accomplish the increment by two, the CNT1A input to the least significant DC006 (E23) must be high, and the CNT1A input to the most significant DC006 (E27) must be grounded. Clocking for DC006 E23 is provided by the transition of the ADREN H line from the DC010. When bus address register DC006 E23 overflows, MAX-A goes high, thus clocking the DC006 E27 bus address register.

The word count register is incremented by one each time a word is transferred. Initially, the word count register is loaded under program control, with the 2's complement of the number of words to be transferred. As words are transferred, the word count register is incremented toward zero. When DC006 E23 overflows, MAX-C goes high. MAX-C clocks the DC006 E27 word count register until DC006 E27 overflows. When E27 overflows, WCNT0 H is generated; WCNT0 H then resets the request flip-flop (E15), thus terminating data transfers.

During DMA data transactions, input data from the DIN bus cycle is placed on the internal tri-state bus via the DC005 transceivers and is

applied to the 74LS273 (E28 and E24) output buffers. These buffers are then clocked by CHANHB and CHANLB, thus placing the data on the 16 OUT lines to the user's device.

For output data transfers (DOUT), the user's device places data on the 16 IN lines to the 74LS367 tri-state drivers. The drivers are enabled by DATEN L, which is asserted during a DOUT cycle. The data passes through the drivers, is applied to the internal tri-state bus and, via the DC005 transceivers, to the LSI-11 bus.

Miscellaneous Logic

Miscellaneous logic is shown in Figure 30. This logic includes CSR, output buffer and input driver control, non-existent address time-out, DC005 transceiver receive/transmit control, the control/status register (CSR), additional transceivers (8641s), and the "B" request flip-flop.

The CSR, output buffers, and input driver control receive INWD L, OUTHB L, OUTLB L, SEL 4 L, SEL 6 L, DATN H, and DIN H. These signals are gated to produce enable signals for the CSR, the output buffers, and the input drivers. CSR RD is produced by INWD L and SEL 4 L to enable the CSR data (DATA 5 through DATA 14) (Figure 5-29, sheet 2) to pass through the 74LS367 tri-state drivers and onto the LSI-11 bus via the DC005 transceivers. OUTHB L, OUTLB L, SEL 4 L, and MRPLY L produce either CSRWHB L or CRSWLB L for writing bit 8 of the CSR (7474 E15 on Figure 5-29, sheet 1), or for clocking the "B" request flip-flop. DATEN L is generated either by DATN H or by INWDL and SEL 6 L. DATEN L enables the 74LS367 tri-state input drivers (Figure 5-29, sheet 1) during an IN cycle. The CHANHB and CHANLB signals clock the 74LS273 output buffers during an OUT cycle. When bytes are transferred, OUTHB L, MRPLY L and SEL 6 L enable the high byte (CHANHB L asserted), while OUTLB L, MRPLY and SEL 6 L enable the low byte (CHANLB L). Both bytes are simultaneously transferred (word transfer) when DIN H is negated.

The non-existent address time-out provides a 10 μs time-out in the event that a non-existent address is requested on the LSI-11 bus during a DMA operation. This prevents hanging-up the LSI-11 bus for periods longer than 10 μs. When the DC010 becomes bus master, ADREN H is asserted and clocks the 10 μs one-shot (E11). Normally, RPLY from the LSI-11 bus goes low and the one-shot is cleared. However, if RPLY is high (no response from slave), the one-shot times out and clocks the 74LS74 flip-flop (E12). The flip-flop is set, generating (TOS + INIT) L; this signal is applied to the DC010 (Figure 5-29, sheet 1) clearing the internal synchronization circuit and releasing the LSI-11 bus. (TOS + INIT) H resets the request flip-flop (E15). The 74LS74 flip-flop (E12) can be set and reset with CSRW HB and DATA 15 (CSR bus time-out). This flip-flop is automatically reset during power-up.

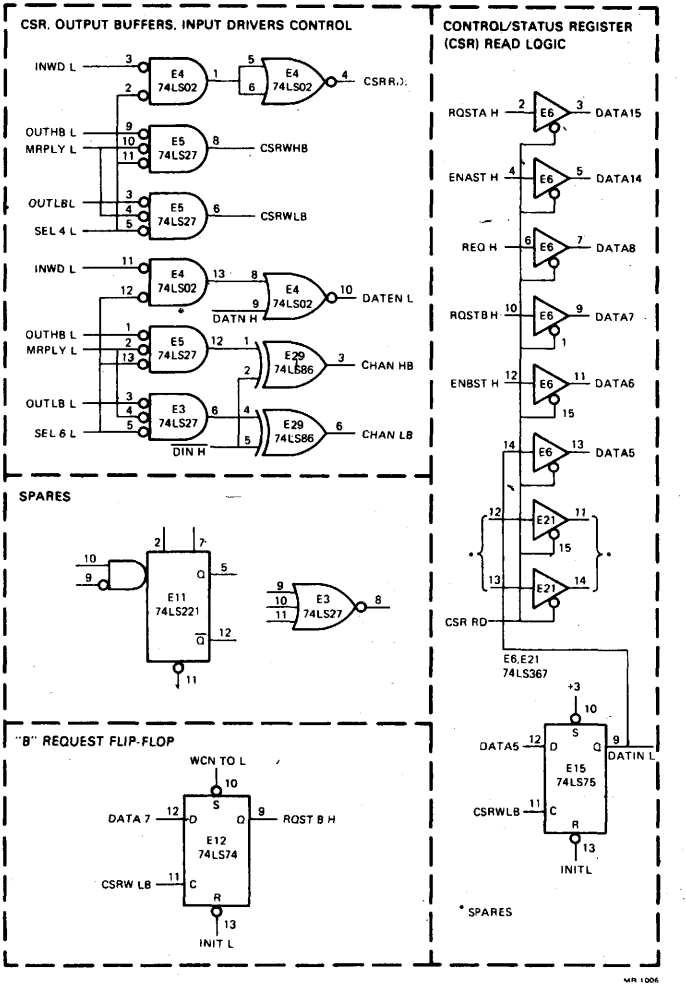


Figure 30 Typical Application (Miscellaneous Logic) (Sheet 1 of 3)

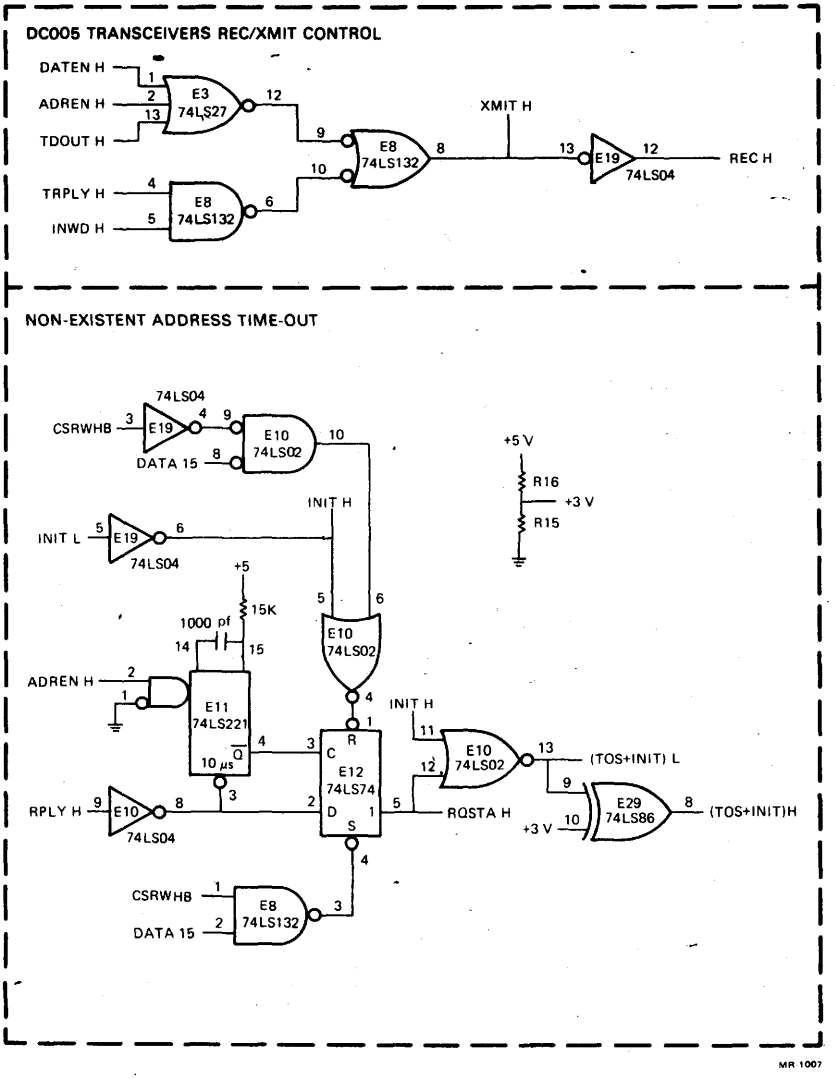
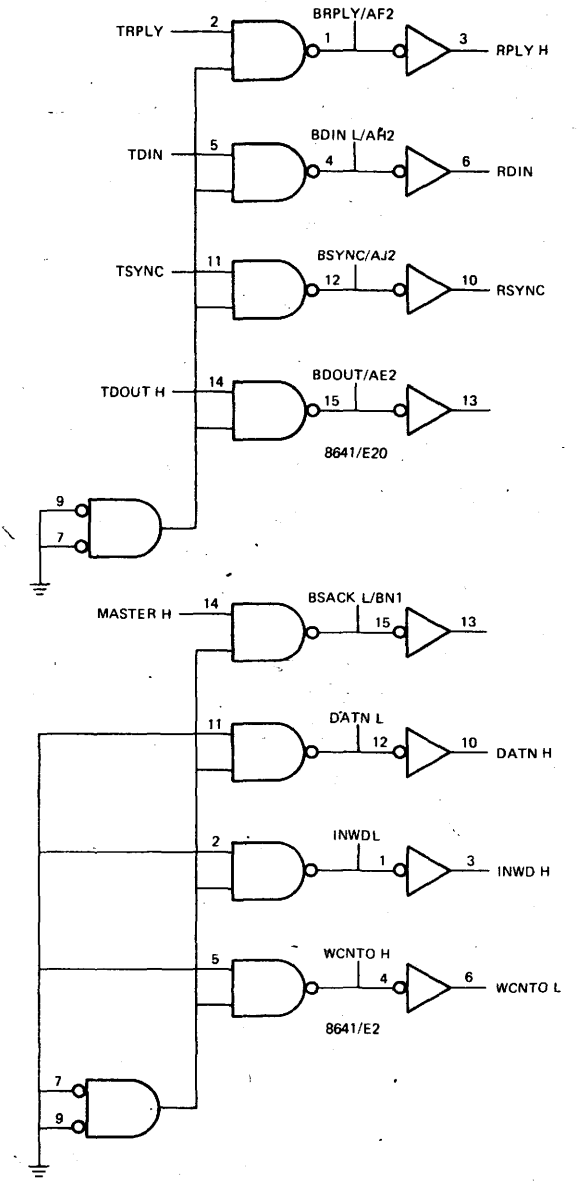


Figure 30 Typical Application (Miscellaneous Logic)
(Sheet 2 of 3)



MR-1008

Figure 30 Typical Application (Miscellaneous Logic)
(Sheet 3 of 3)

The DC005 transceiver receive/transmit control determines the state of the DC005 transceivers on Figure 26. Normally, the transceivers are in the receive state to accept device addresses from the LSI-11 bus. When REC H is asserted (high), XMIT is negated (low). XMIT is asserted (high) when transferring data to the LSI-11 bus (T DOUT, DATEN, and ADREN are high; TRPLY, INWD are low). REC is asserted (high) when receiving data from the LSI-11 bus (TDOUT, DATEN, and ADREN are low; TRPLY, INWD are high).

The control/status register (CSR) (Figure 29, sheet 2) has six active bits and is a read/write register comprised of 74LS367 tri-state drivers and flip-flops which are part of other logic circuits shown on Figure 29, sheet 1, and Figure 30, sheet 3. Figure 31 shows the CSR format. The CSR bits are described in Table 12.

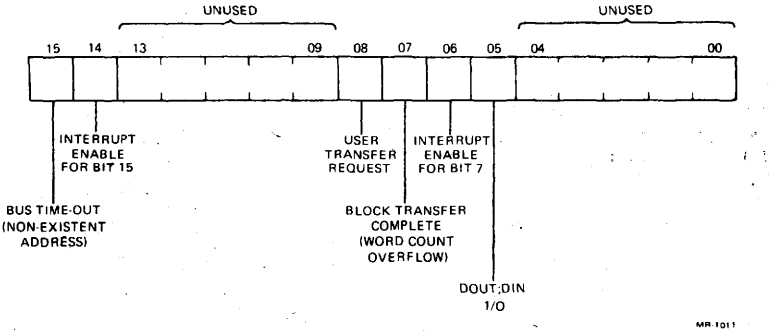


Figure 31 Control/Status Register (CSR) Format

The quad transceivers (8641) supplement the DC005 transceivers for interfacing to the LSI-11 bus. In this particular application, the 8641s are permanently enabled by grounding pins 7 and 9.

Table 12 CSR Bit Descriptions

Bit	Name	Description
00 01 02 03 04	Unused	
05	DOUT/DIN	When on a 1, indicate a DOUT cycle; when on a 0, indicate a DIN cycle.

Table 12 CSR Bit Descriptions (Cont)

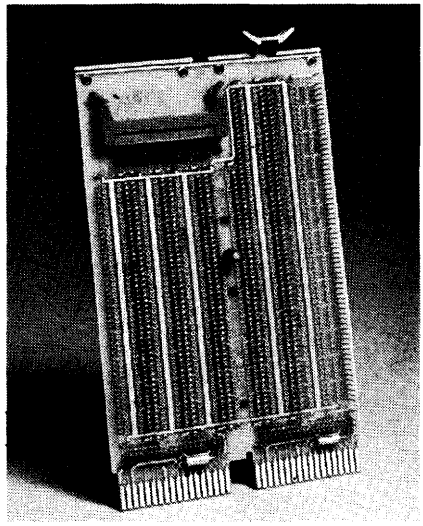
Bit	Name	Description
06	Interrupt enable for bit 7	This bit must be set (1) to enable the word count overflow; interrupt at the end of a block transfer. When on a 0, the interrupt is inhibited.
07	Block transfer complete	This bit sets (1) when the word count register overflows, providing bit 06 is set.
08	User transfer request	The user's device must set (1) this bit to make a bus request and transfer data. User REQ L (J1-PP) must be driven low (0) to set bit 08. This bit is always read as a zero. This is an example for test purposes.
09 10 11 12 13	Unused	
14	Interrupt enable for bit 15	This bit must be set (1) to enable the bus time-out interrupt. When on a 0, the interrupt is inhibited.
15	Bus time-out	This bit sets (1) when a slave on the LSI-11 bus does not respond with BRPLY within 10 μs after being addressed. Bit 14 must be set (1) to enable the bus time-out interrupt.

Wire Wrappable Module W9512

The W9512 module will accept a variety of IC package types and discrete components. The printed circuit on each board connects the appropriate edge connector pins to the Vcc plane on Side 2 of the board and the ground plane (GND) on Side 1. The remaining edge connector pins terminate to a double row of wire wrap pins for user designated functions. Each module also includes a premounted 40-pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire wrap pins. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and prevent shorting of wire wrap pins. The wire wrap pins and components are mounted on Side 2 of each module. The majority of the rows of predrilled holes accept IC packages with pin spacings of 0.3". However, a universal area on the W9512 module is the area which accepts IC packages with standard pin spacings of 0.3", 0.4" and 0.6".

Total IC capacity on the wire wrap module is as follows: 32 14-pin IC's or 27 16-pin IC's, 5 24-pin IC's, 3 40-pin IC's.

These capacities allow one pair of holes between each DIP for mounting additional decoupling capacitors. The W9512 module is supplied without IC sockets. IC sockets available through the handbook are the 954 (14-16 pins), the 961 (24 pins) and the 962 (40 pins).



W9512 wire wrappable board is quipped with 40-pin male interface connector.

IMPORTANT NOTE ON DMA CHIPKITS

The two DMA Bus Interface CHIPKITS, DCK11-AB and DCK11-AD, are new products being developed by DIGITAL, and are undergoing final applications testing and review as of the publication date of this handbook—July, 1978. Production quantities are expected about October, 1978. If you have a serious interest in using these CHIPKITS, contact us for the latest word on availability. Write DIGITAL, Logic Products Sales Support, MK1-2/E13, Merrimack, NH 03054, or call us on our toll-free Hot Line, 8:30 AM to 5:00 PM Eastern time: 800-258-1710. From New Hampshire locations or places outside the continental U.S., call 603-884-6660.

GENERAL PURPOSE LOGIC & CONTROL MODULES
M-SERIES, A-SERIES, K-SERIES—FOR INTERFACING, COMMUNICATIONS, AND SPECIAL APPLICATIONS

GENERAL PURPOSE LOGIC AND CONTROL MODULES

This section describes the computer industry's most extensive line of general purpose logic modules—modules used in DIGITAL's products and modules used by thousands of customers for computer interfacing, instrumentation, data gathering, and control. The module descriptions are organized into three main subsections: M Series, A Series, and K Series.

M Series high-speed monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) circuits which provide high speed, high fanout, large capacitance drive capability, and excellent noise margins.

In addition to the reduced cost of integrated circuits, DIGITAL's advanced manufacturing methods and computer-controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series modules.

A Series analog modules support the M Series by providing a two-way translation between continually varying real-world voltage measurements and the digital realm of control and computation.

K-Series industrial control modules offer exceptional immunity to electrical noise. In typical process-control applications, inputs are from limit switches, photocells, or the like; outputs are to control motor starters, relays, solenoids, or lamps. K-Series modules have many advantages over electromechanical control devices, and can also connect to a computer if a suitable high-speed TTL interface is used.

The associated hardware for these general purpose modules, such as module connector blocks, mounting panels, cabinets, and power supplies, is summarized elsewhere in this handbook and described in detail in the Hardware/Accessories Catalog, also published by DIGITAL.

M SERIES
GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board is double-sided providing 36-pins in a single height module. Mounting panels and 36-pin sockets are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Cabinets & Parts section of this handbook as well as the Hardware/Accessories Catalog published by DIGITAL.

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 Volts ± 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

LOGIC LEVELS AND NOISE MARGIN
A gate input will recognize 0.0 volts to 0.8 volts as logical LO and 2.0 volts to 5.0 volts will be recognized as a logical HI. An output is between 0.0 volts and 0.4 volts in the logical-LO condition. The logical HI output condition is between 2.4 volts and 5.0 volts. Figure 1 shows diagrammatically the acceptable transistor-transistor logic levels. The worst case noise margin is 400 millivolts, that is, an output would have to make at least a 400 millivolt excursion to cause an input which is connected to it to go into the indetermined voltage region. For instance if an output were at 0.4 volts (worst case logical LO) there would have to be a + 400 mv swing in voltage to cause inputs connected to it to go into their indetermined region.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1 state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

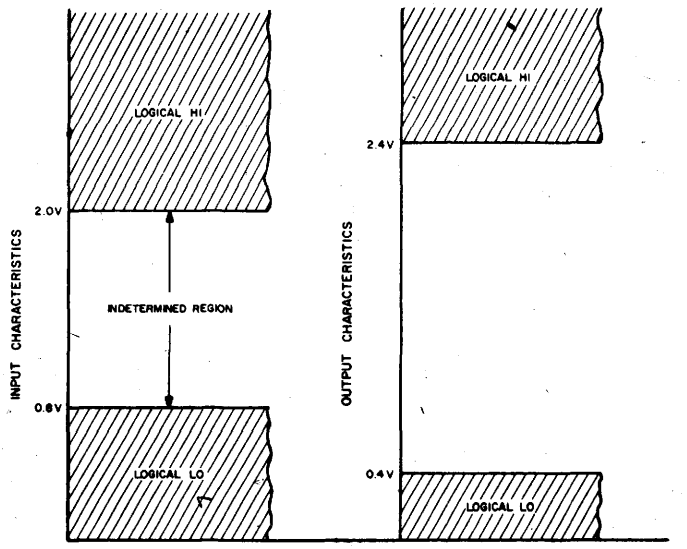
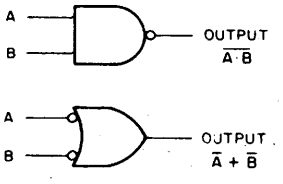


Figure 1 Logic Levels

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 2.



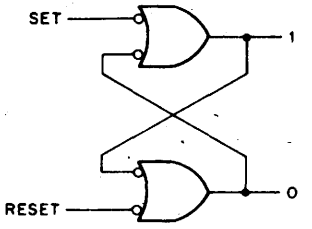
A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2 NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 3.



PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H*	H*
H	L	L	L	H*	H*

*Ambiguous state: In practice the input that stays low longest will assume control.

Figure 3 RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 4.) One of the inputs of each NAND is tied to a common clock or trigger line.

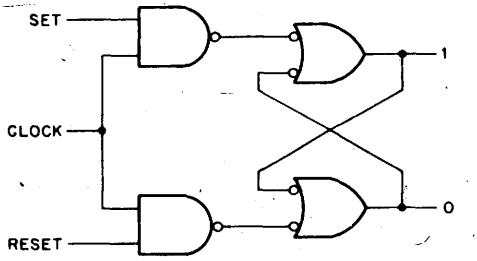
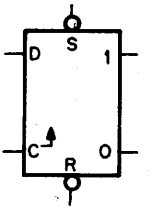


Figure 4 Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.



LOGIC SYMBOL

Figure 5

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 5. A low to high transition at the C input causes the 1 output to assume the state that the D input was at the time of transition. The 0 output will always assume the opposite state. In this way, the D flip-flop will store the signal level at the D input since subsequent changes at the D input will not affect the flip-flop's state until the C input is again clocked with a low to high transition. When the 1 output is high and the 0 output is low, the flip-flop is said to be set. When the 1 output is low and the 0 output is high, the flip-flop is said to be reset or cleared. The D flip-flop can be direct set by applying a low level or pulse to the S input. Likewise, it can be direct reset by applying a low level or pulse to the R input. Signals at the S and R inputs will override those at the C and D inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are high during the clock pulse, and B) if both the J and the K inputs are high during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, as the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior

to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

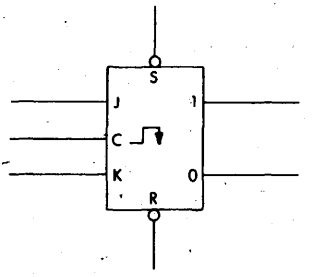


Figure 6. Master-Slave J-K Flip-Flop

Figure 7 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS OUTPUTS		INPUTS		FINAL CONDITIONS OUTPUTS	
1	0	J	K	1	0
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	L
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	L	H	H	L	H

Figure 7. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)
Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected.

To insure maximum noise immunity, it is necessary to connect these inputs to either ground or to a source of Logic 1 (high) depending on the situation. For instance, the unused inputs of a NAND gate would be connected to a Logic 1 source, while the unused inputs of a NOR gate would be grounded.

If a Logic 1 source is needed, it may be obtained in several ways.

1. Many M Series modules provide +3 volt sources for this purpose. Consult the module diagrams for pin numbers and fan-out capability.
2. Ground the inputs of an unused NAND gate or inverter and use the output as a +3 volt source.
3. Connect unused inputs to one of the active inputs on the same gate. However, this results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

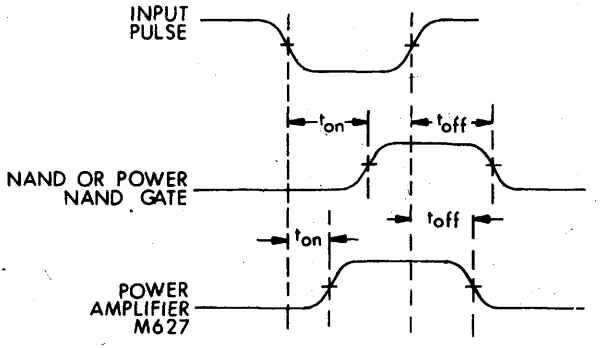
Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 8) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

TIMING CONSIDERATIONS
Delays introduced by inverting gates and high speed power gates power amplifiers are illustrated in Figure 8. (Delays are measured between threshold points.)



	DELAY (NANOSECONDS)			
	t_{on}		t_{off}	
	TYP	MAX	TYP	MAX
STANDARD GATES	18	29	8	15
HIGH SPEED GATES	7	—	5	—

Figure 8. NAND Gate and Power Amplifier Delays

GENERAL PURPOSE MODULES
FUNCTIONAL LISTING

FUNCTION	TYPE	PAGE
GATES		
Inverter	M111	245
Inverter/Buffers	M165	266
High-Speed Power Inverter	M611	315
2-Input NAND Gates	M113	247
3-Input NAND Gates	M115	247
4-Input NAND Gates	M117	247
8-Input NAND GATES	M119	247
High-Speed 2-Input NAND Gates	M133	252
High-Speed 3-Input NAND Gates	M135	253
High-Speed 4-Input Power NAND Gates	M137	254
High-Speed 8-Input NAND Gates	M139	255
4-Input Power NAND Gates	M617	316
High-Speed 4-Input NAND Gates	M627	317
AND/OR Gates	M121	251
NAND/OR Gates	M141	256
2-Input NOR Gates	M112	246
4-Input NOR Gates	M116	250
2-Input AND Gates	M1103	330
4-Input AND Gates	M1307	333
Exclusive-OR Gates	M1125	331
Logic Gate	K113	394
Logic Gate	K123	394
Logic Gate	K124	394
Inverter	K134	394
Inverter	K135	394
Inverter	K138	394
OPEN COLLECTOR GATES		
NAND/OR Gates	M141	256
2-Input NAND Gates	M1131	332
See also the following modules described in other sections of this handbook.		
Gated 80 mA High Impedance NAND Gates	M783	71
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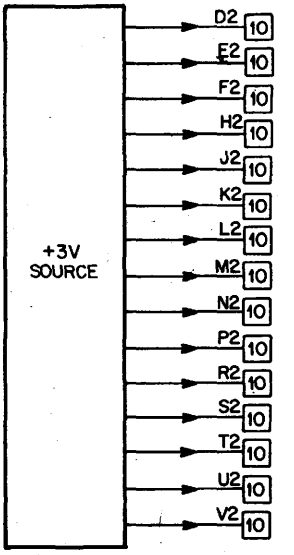
M002
LOGIC HIGH SOURCE

MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Single
Width: Single

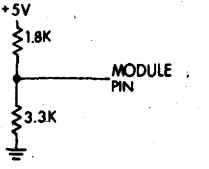


Volts	Power mA (max.)	Pins
+5	16	A2
GND		C2, T1

To hold unused M Series TTL gate inputs HIGH, the M002 provides 15 outputs at +3 volts (logic HIGH) on pins D2 through V2. Up to 10 unused M Series gate inputs may be connected to any one output.

The M002 can also be used as pull-ups for open-collector outputs in a wired-OR situation. If an M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 mA at ground.

The following diagram shows one of the 15 identical circuits.

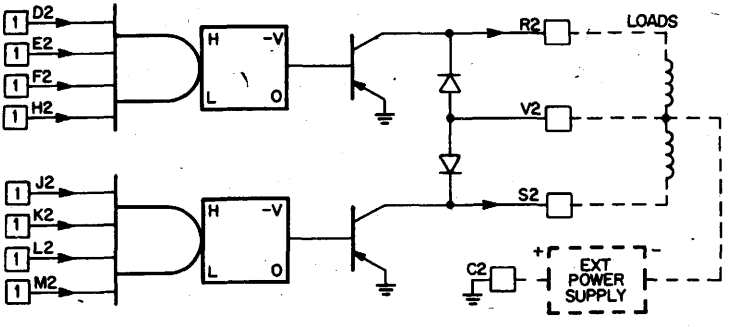


M040
SOLENOID DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	47	A2
GND		C2, T1
−15	9	B2

The M040 contains two identical negative high-voltage driver circuits. Each consists of a 4-input positive NAND gate that controls a PNP transistor switch. The switch is capable of sinking up to 600 mA of current to ground from an external power supply of up to −70 volts. One terminal of the load device (relay, etc.) must be connected to the external voltage, the other to the drive output. The positive terminal of the external supply connects to the module ground.

APPLICATIONS

The M040 can drive relays, solenoids, stepping motor windings and similar inductive loads.

Restrictions: Not recommended for incandescent lamps.

FUNCTIONS

ON Condition: Each driver sinks current from the external circuit when all four control inputs are HIGH. The amount of current is determined by the external voltage and load impedance. (The internal switch is a saturated PNP transistor.) Typical output voltage when sinking 0.6 A is −2 volts.

OFF Condition: When one or more control inputs is LOW, the internal switch is a high impedance and the output voltage approaches the external voltage source. The output circuit draws a small amount of leakage current (typically 100 μA for a 70-volt external supply).

Anti-Kickback: Pin V2 of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than three feet long, it may have to be bypassed at the module with an electrolytic capacitor to reduce the pulse overshoot caused by the inductance of the wire.

Improving Recovery Time: If pin V2 is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

PRECAUTIONS

Grounding: High current loads should be grounded directly at pin C2 of the M040, rather than at a frame or bus ground.

Parallel Operation: No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

SPECIFICATIONS

Current sinking capability: 600 mA per circuit, max.

External supply voltage: 70 V dc max.

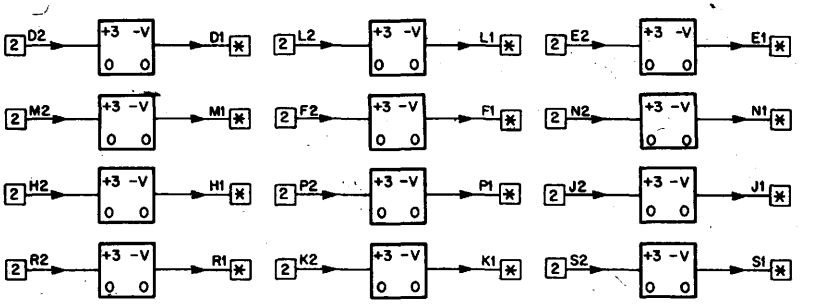
Circuit Delay: Typical propagation delay for each circuit is 5 μs (between 10% and 90% voltage points) for an external supply voltage of 70 volts.

M050
50 MA INDICATOR DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



* = 50 MA, -30V MAX.

Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
—15	16	B2

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel. A LOW level on the input of the driver causes current to flow in the output.

Restrictions: Do not use to drive inductive loads (relays, solenoids).

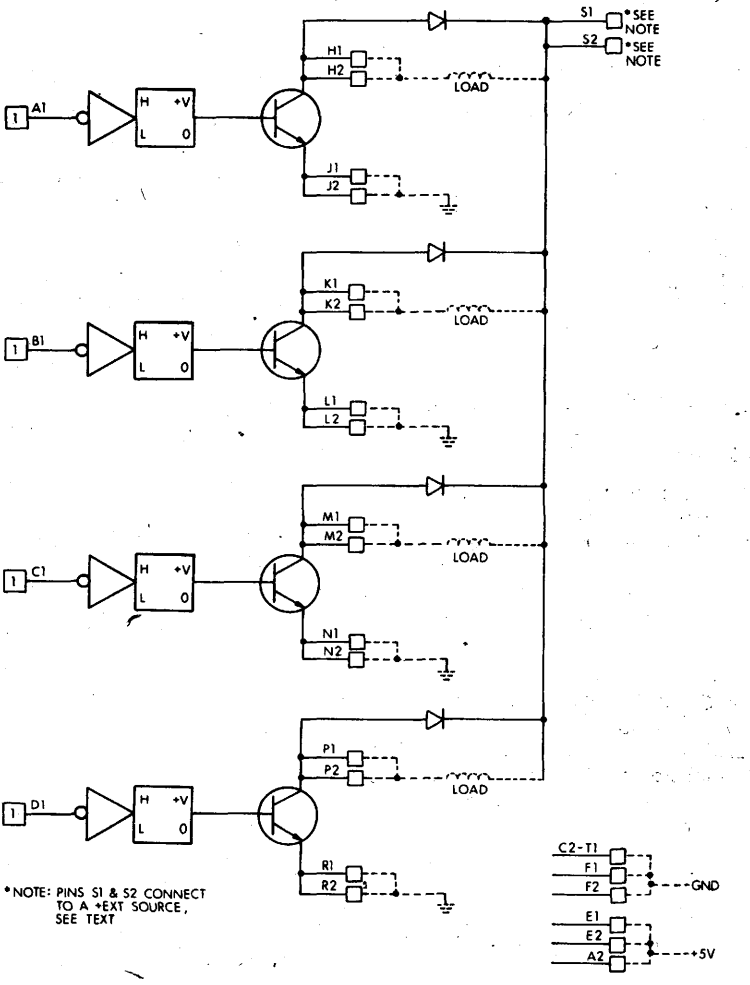
SPECIFICATIONS
Each output is able to drive 50 mA into an external load connected to any voltage up to —30 volts.

M060
SOLENOID DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80	A2, E1, E2, C2, T1, F1, F2
GND	See Text	S1, S2

The M060 module consists of four identical positive high-current driver circuits. Each circuit contains an inverting gate that controls an NPN transistor switch. A low level, at any input, will turn on the switch which is capable of driving loads up to 1.2 amps to ground with external power supply voltages of up to +75 V dc.

APPLICATIONS
The M060 module can be used to drive relays, solenoids, and any similar inductive loads requiring current of up to 1.2 amps.

It is not recommended for lamp-driving tasks; for this application, the M050 module should be utilized.

EXTERNAL POWER SUPPLY
An external power supply must be used to power the loads. This supply may be a maximum of 75 V dc. In connecting the power supply, the positive terminal should be connected to pins S1 and S2, and the negative terminal to ground.

One side of the load device must connect to the external supply and the other side to the driver output.

FUNCTIONS
ON Condition: Each switch activates the load device when the input is a logic Low, 0. In this condition, the circuit supplies current which is determined by the external power supply voltage and the load impedance.

OFF Condition: When the input is high, the switch is open and a high impedance exists. In this condition, there is a small amount of leakage current flow which is typically less than 100 μA for an external supply voltage of 75 V dc.

CONNECTIONS and PRECAUTIONS
Note that the emitter and collector on each transistor switch, and the external power supply inputs, each have two pin connections. These dual connections are required because of the high current capability of the circuit. In each case, the pins should be tied together as shown by the dotted lines on the diagram. It should also be mentioned that the emitter connections of each transistor switch must be connected to ground, preferably at pin C2 of the logic block.

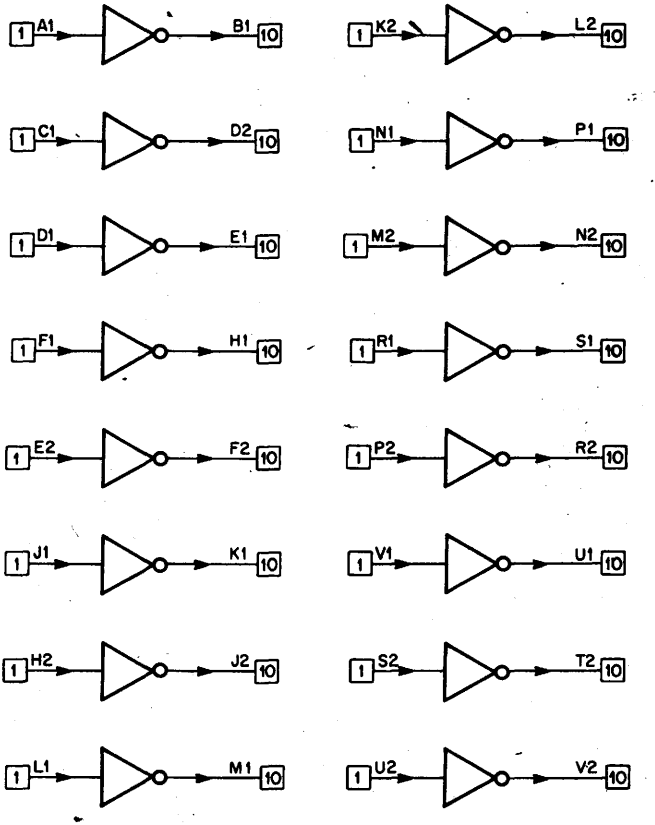
SPECIFICATIONS
Current Capability: 1.2 amps per circuit (max)
External Supply Voltage: 75 V dc (max)
Circuit Delay: 10 μs (typical)—15 μs (max)

M111
INVERTER

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



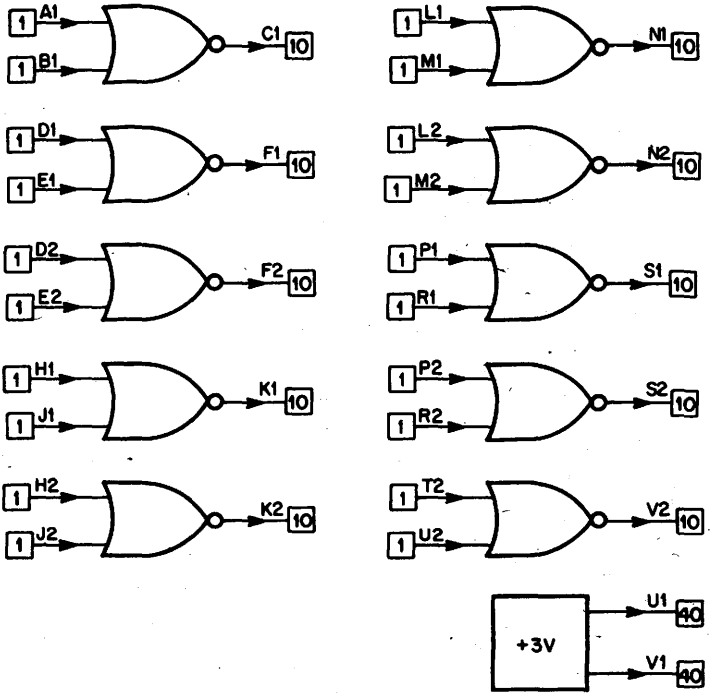
Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

M112
NOR GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



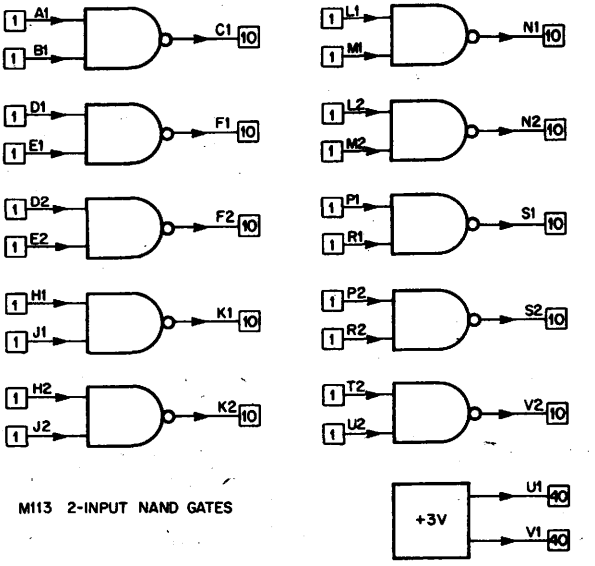
Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

M113, M115, M117, M119
NAND GATES

GATES

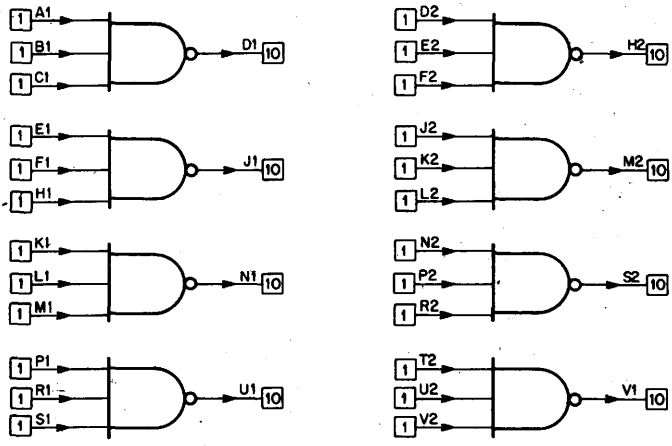
M SERIES

Length: Standard
Height: Single
Width: Single

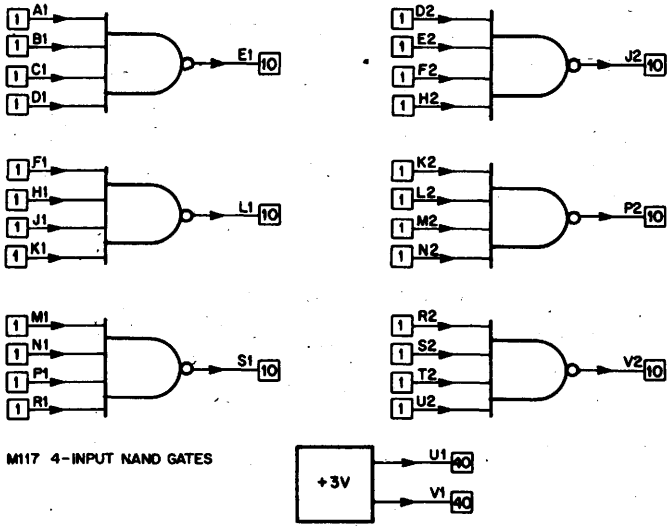


M113 2-INPUT NAND GATES

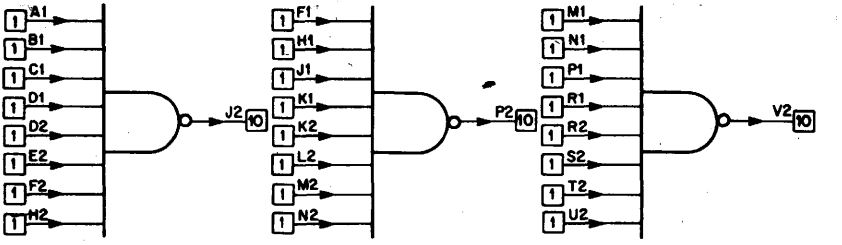
Volts	Power mA (max.)	Pins
+5	71 M113	A2
+5	41 M115	A2
+5	41 M117	A2
+5	19 M119	A2
GND		C2, T1



M115 3-INPUT NAND GATES



M117 4-INPUT NAND GATES



M119 8-INPUT NAND GATES

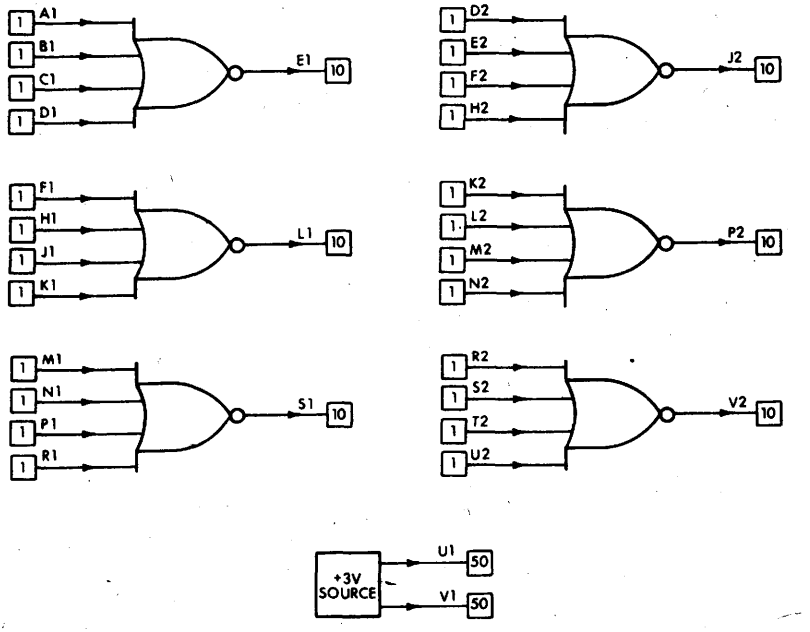
These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function ($\cdot B \cdot C \cdot \overline{\quad\quad} \overline{N}$), depending upon the number of inputs.

M116
6 4-INPUT NOR GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	30	A2
GND		C2, T1

The M116 module consists of six high-speed, 4-input NOR gates. Pins U1 and V1 provide separate logic HIGH sources (+3V), each capable of holding up to 50 unused M Series inputs HIGH.

SPECIFICATIONS
Maximum propagation delay to a logic HIGH or LOW is 10 ns.

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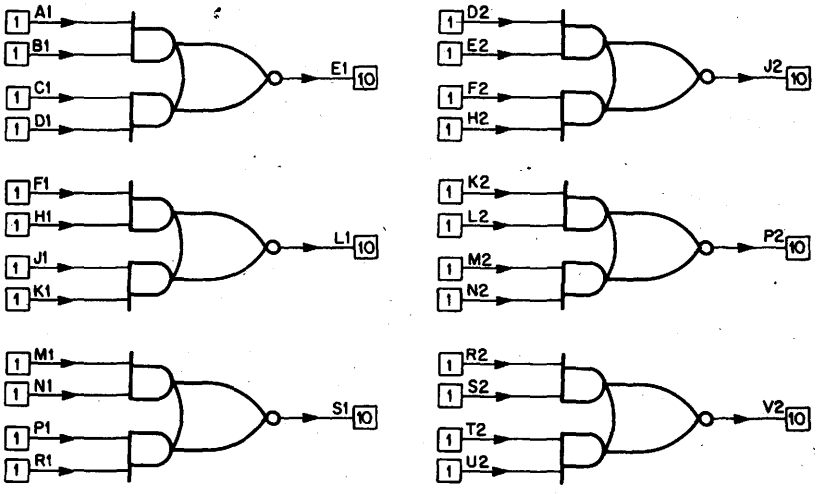
M121
AND/NOR GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M121 module contains six AND/NOR gates which perform the function $\overline{(A \cdot B + C \cdot D)}$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

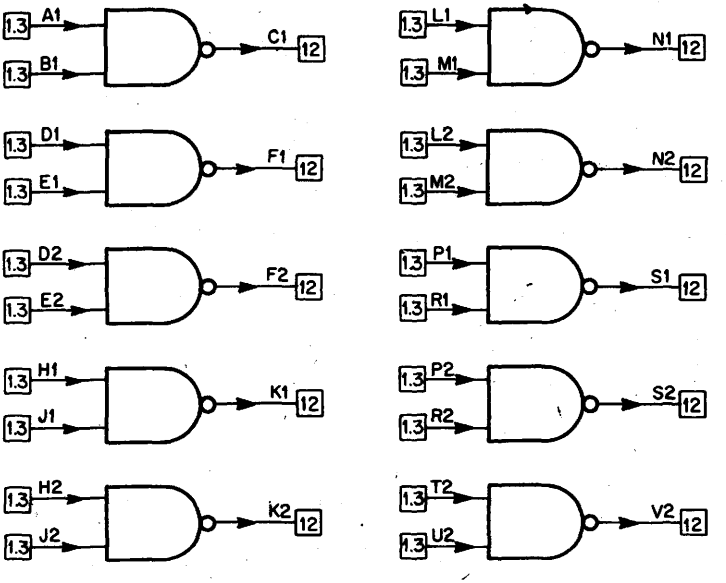
SPECIFICATIONS
Propagation Delay: Typically 15 ns

M133
TWO-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, T1

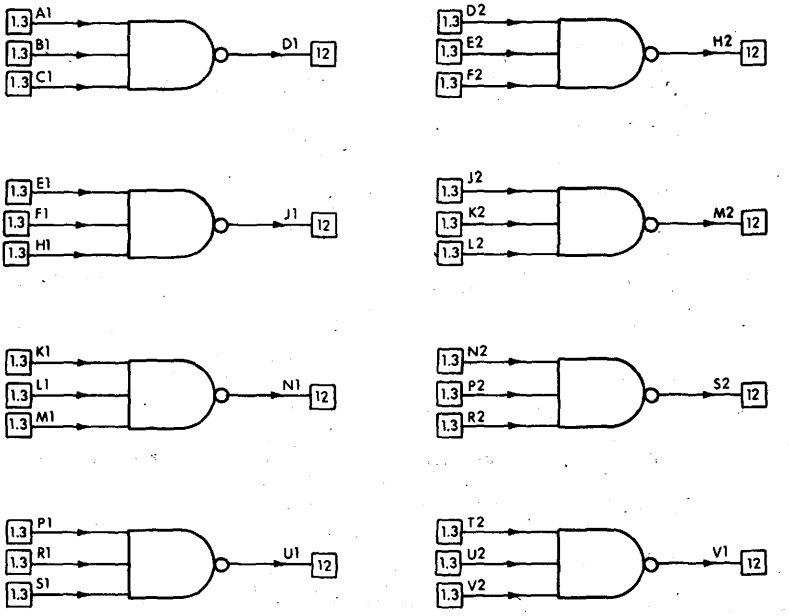
The M133 provides general-purpose high-speed NAND gating.

M135
8 3-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M135 module consists of eight high-speed, 3-input, positive logic NAND gates.

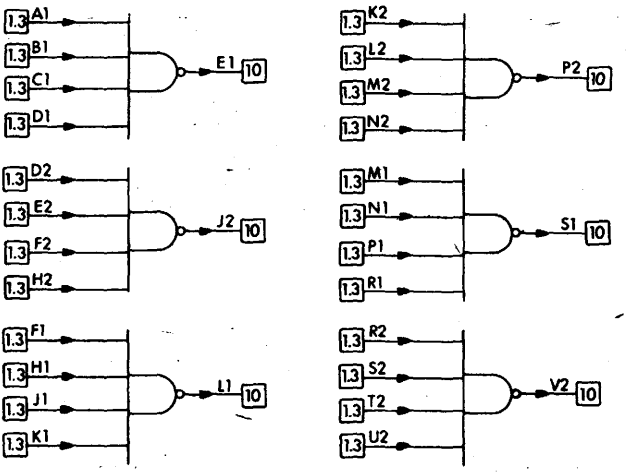
SPECIFICATIONS
Maximum propagation delay to a logic HIGH or LOW is 10 ns.

M137
SIX 4 INPUT NAND GATES

GATES

M SERIES

Length: Standard
Width: Single
Height: Single



Volts	Power mA (max.)	Pins
+5V	100 mA	A2
GND		C2, T1

The M137 Module consists of six high-speed, 4-input positive logic NAND gates.

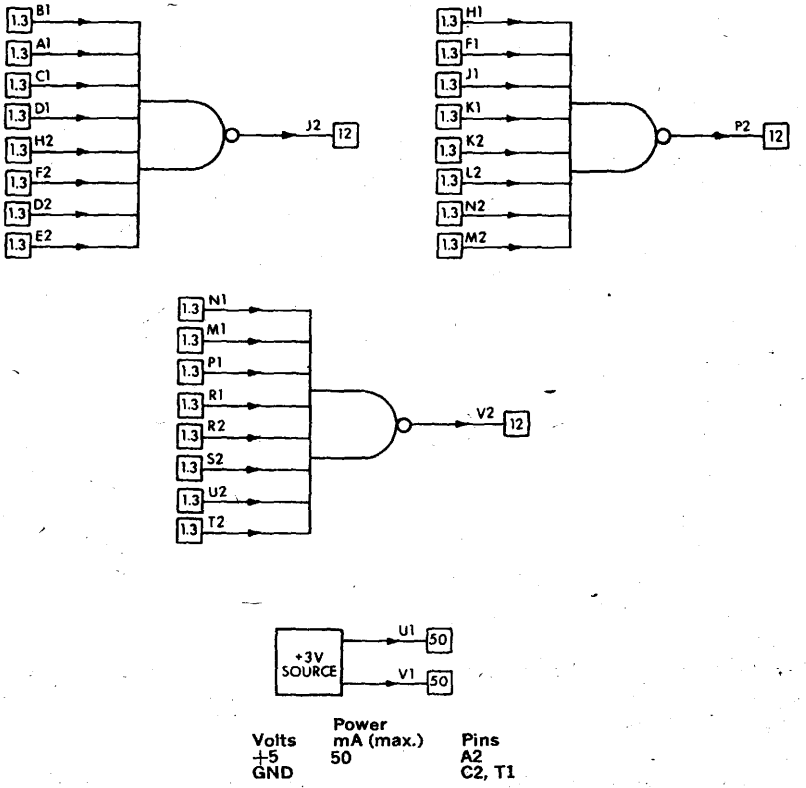
Maximum propagation delay to a logic High or Low is 10 ns.

M139
3 8-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M139 module consists of three high-speed, 8-input, positive logic NAND gates. Pins U1 and V1 provide two separate logic HIGH sources (+3 V,) each capable of holding up to 50 unused M Series inputs HIGH.

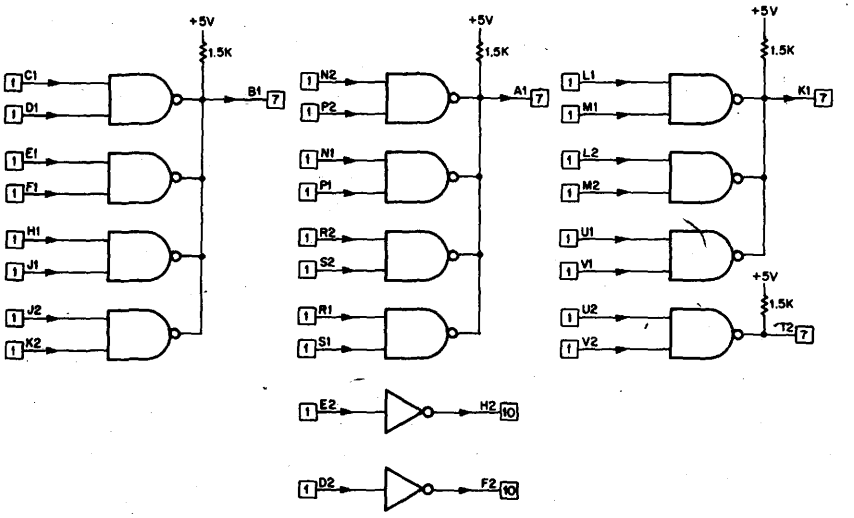
SPECIFICATIONS
Maximum propagation delay to a logic HIGH or LOW is 10 ns.

M141
NAND/OR GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	117	A2
GND		C2, T1

The M141 provides NAND/OR gates arranged in four groups consisting of 4, 4, 3, and 1 two-input NAND gates respectively. The outputs in each group are connected together to provide a wired OR for low levels.

A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together. The two-input NAND gate which is used in the M141 does not have the standard TTL ouput circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor.

SPECIFICATIONS
Propagation Delay: 70 ns max.

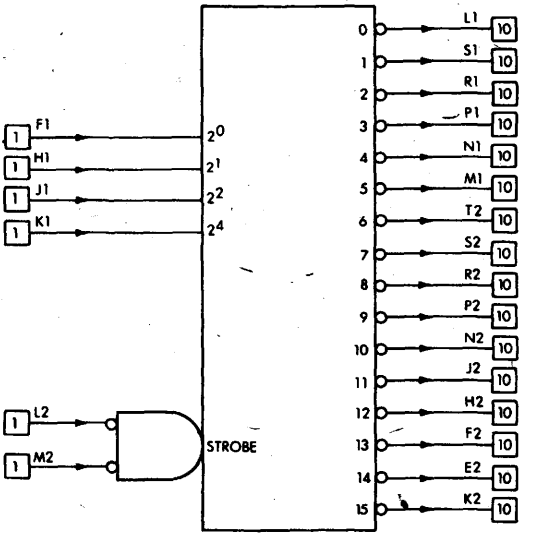
Loading: The load resistor of each output presents 2 unit loads when connected to another output. For example, when four groups are connected together, 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability.

M155
4-LINE TO 16-LINE DECODER

DECODERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M155 module decodes the binary value on the four input lines into one of sixteen mutually exclusive outputs when both STROBE inputs, L2 and M2, are Low. The demultiplexing function is performed by using the four input lines to address the output line. When either STROBE input is HIGH, all outputs are HIGH.

SPECIFICATIONS
Propagation Delay

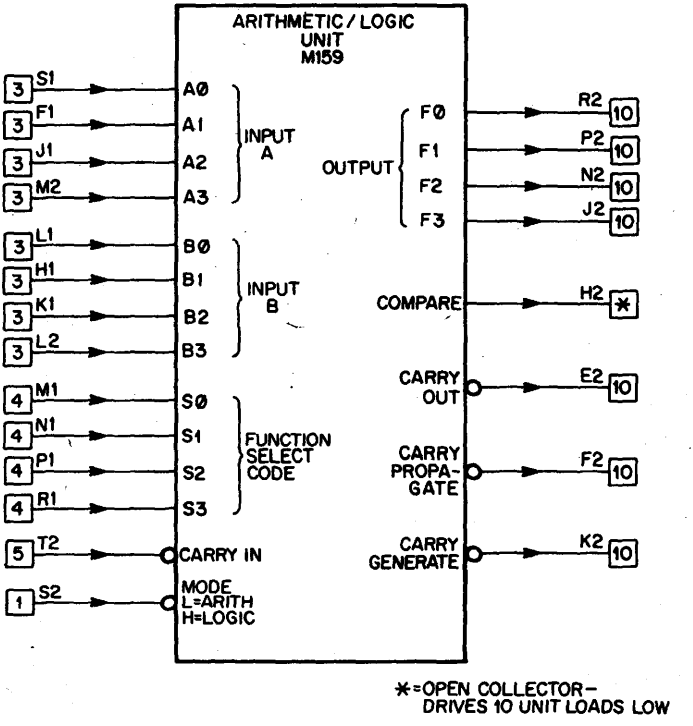
From:	To:
Data Inputs (L2 & M2 Low)	HIGH or LOW Output = 36 ns (max)
Either STROBE Input	HIGH or LOW Output = 30 ns (max)

M159
ARITHMETIC/LOGIC UNIT

ARITH-
METIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	150	A2
GND		C2, T1

The M159 can perform 16 word-oriented arithmetic operations and 16 bit oriented logic functions. Arithmetic operations are performed on two 4-bit input words and an input carry to produce one 4-bit output word and a carry out. In the logic mode the M159 looks like four 2-input functional gates. Where N indicates one out of four, the output F_N depends only on the inputs A_N, B_N, and the logic function code selected.

The M159 is fully cascadable. The CARRY OUT of the less significant M159 should be connected directly to the CARRY IN of the next more significant M159. The CARRY PROPAGATE and CARRY GENERATE output can be left unconnected or used with a carry look-ahead module. (See M191).

The COMPARE output goes High whenever all the "F" outputs go High. This output is open-collector so that it can be wire-AND connected when M159 modules are cascaded. An example of how this output can be used is shown in the table below.

When the arithmetic operation A minus B minus 1 is selected, the M159 can be used as a comparator.

A and B Data Inputs	COMPARE Output	CARRY OUT
$A > B$	0	0
$A = B$	1	1
$A < B$	0	1

The maximum propagation delay from the "A_N" or "B_N" bit input to the output bit "F_N" in the logic mode is 48 nsec. which does not change as M159's are cascaded. In the arithmetic mode, the maximum delay from the "A" or "B" word input to the "F" word output, CARRY OUT, or COMPARE is 50 nsec. which increases by 19 nsec. per additional cascaded M159 when carry look-ahead is not used. When carry look-ahead is used, the maximum additional delay is limited to 20 nsec. for up to three additional M159's.

Table of Logic Mode Operations

(MODE Input = 1)

(CARRY IN has no affect on Logic Mode Operations)

Function SELECTION CODE				**NOTE** that F_N is complemented when the Function Selection Code is complemented		Complemented Function SELECTION CODE			
S3	S2	S1	S0	Bit F_N Equals	Bit F_N Equals	S3	S2	S1	S0
0	0	0	0	$\overline{A}_N$	A_N	1	1	1	1
0	0	0	1	$\overline{A}_N$ AND $\overline{B}_N$	A_N OR B_N	1	1	1	0
0	0	1	0	$\overline{A}_N$ AND B_N	A_N OR $\overline{B}_N$	1	1	0	1
0	0	1	1	0	1	1	1	0	0
0	1	0	0	$\overline{A}_N$ OR $\overline{B}_N$	A_N AND B_N	1	0	1	1
0	1	0	1	$\overline{B}_N$	B_N	1	0	1	0
0	1	1	0	(A_N AND $\overline{B}_N$) OR ($\overline{A}_N$ AND B_N)	(A_N AND B_N) OR ($\overline{A}_N$ AND $\overline{B}_N$)	1	0	0	1
0	1	1	1	A_N AND $\overline{B}_N$	$\overline{A}_N$ OR B_N	1	0	0	0

Table of Arithmetic Mode Operations

(MODE Input = 0)

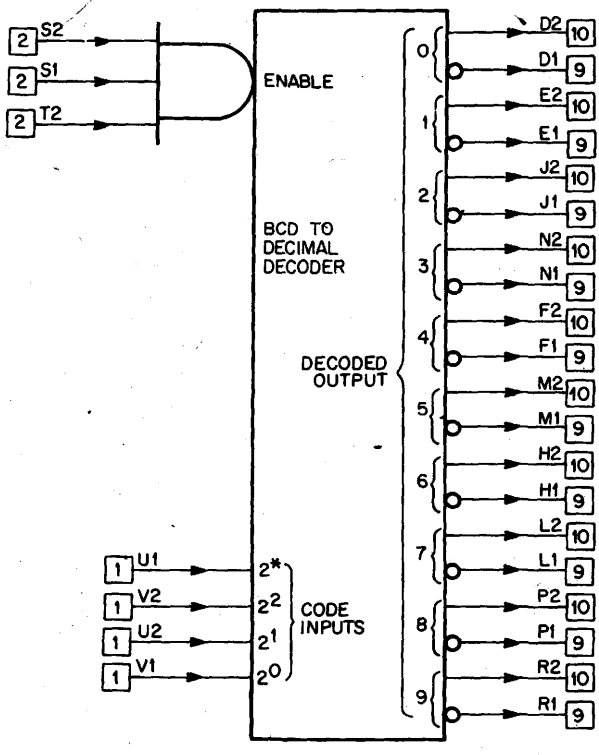
Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0	WORD A	WORD A plus 1
0	0	0	1	A OR B	A OR B plus 1
0	0	1	0	A OR $\overline{B}$	A OR $\overline{B}$ plus 1
0	0	1	1	Minus 1 (2's Comp.)	ZERO
0	1	0	0	A plus (A AND $\overline{B}$)	A plus (A AND $\overline{B}$) plus 1
0	1	0	1	(A OR B) plus (A AND $\overline{B}$)	(A OR B) plus (A AND $\overline{B}$) plus 1
0	1	1	0	A Minus B Minus 1	A Minus B
0	1	1	1	(A AND $\overline{B}$) minus 1	A AND $\overline{B}$
1	0	0	0	A plus (A AND B)	A plus (A AND B) plus 1
1	0	0	1	A plus B	A plus B plus 1
1	0	1	0	(A OR $\overline{B}$) plus (A AND B)	(A OR $\overline{B}$) plus (A AND B) plus 1
1	0	1	1	(A AND B) minus 1	A AND B
1	1	0	0	A Times 2	A Times 2 plus 1
1	1	0	1	(A OR B) plus A	(A OR B) plus A plus 1
1	1	1	0	(A OR $\overline{B}$) plus A	(A OR $\overline{B}$) plus A plus 1
1	1	1	1	A minus 1	A

M161
BINARY TO OCTAL/DECIMAL DECODER

DECODERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one octal or decimal digit. In the octal mode, the bit 2* input should be connected to ground, which automatically inhibits the 8 and 9 outputs. A HIGH and a LOW version of each output is provided.

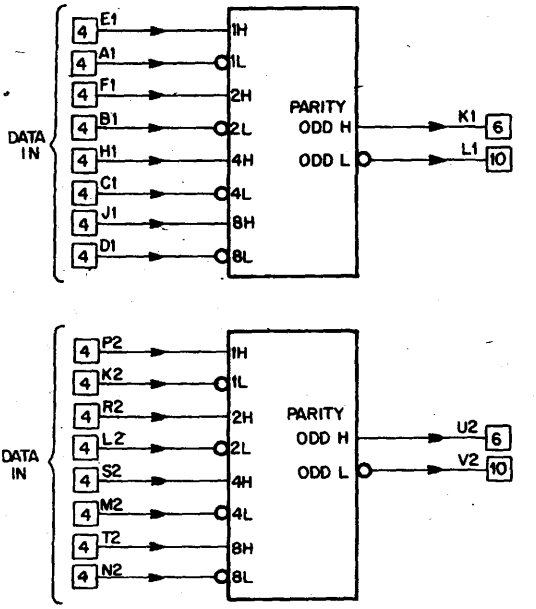
The 2* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.
The typically propagation delay through the decoder is 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2* have settled at least 50 nsec prior to the input pulse.

M162
PARITY CIRCUIT

MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	102	A2
GND		C2, T1

The M162 contains two parity detector circuits. Each circuit indicates whether the binary data presented to it contains an ODD or EVEN number of ONES.

APPLICATIONS

- Parity checking

FUNCTIONS

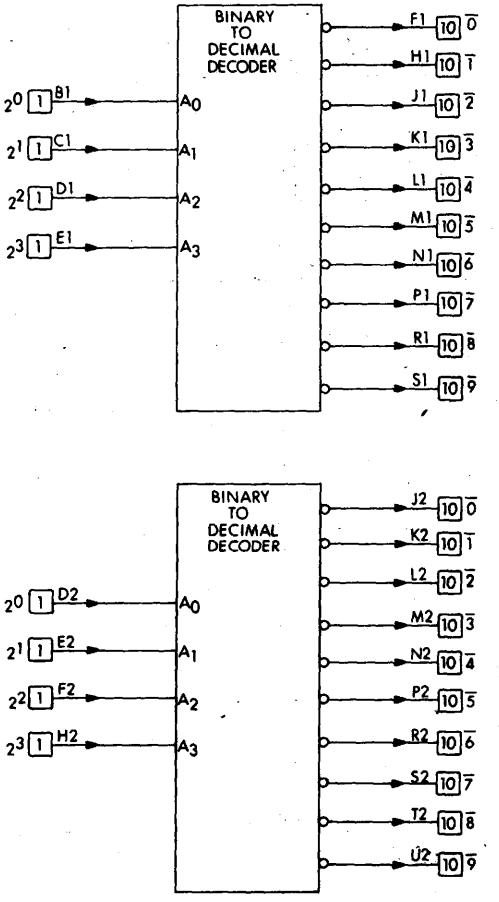
Indication of ODD PARITY is given by a HIGH level at pins K1 and U2 respectively. Pins L1 and V2, when HIGH, indicate EVEN PARITY or no input.

M163
DUAL BINARY-TO-DECIMAL DECODER

DECODERS

M SERIES

Length: Standard
Width: Single
Height: Single



Volts	Power mA (max.)	Pins
+5V	44	A2
GND		C2, T1

The M163 Module consists of two binary-to-decimal decoder circuits, each of which accepts four inputs and provides 10 mutually exclusive outputs. The most significant 2^3 input can be used as an enable function to allow the circuits to be used as a binary-to-octal decoder. Outputs $\overline{0}$ through $\overline{7}$ will remain HIGH as long as input 2^3 is HIGH.

APPLICATIONS

1-of-10 decoder or 1-of-8 decoder with selected output Low.

FUNCTION

Each of the decoder circuits on the M163 Module accepts four active High BCD inputs and provides 10 mutually exclusive active Low outputs. All outputs are High when binary codes greater than 9 are applied to the inputs. Refer to the truth table for input/output level sequences.

TRUTH TABLE (EACH SECTION)

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	L	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

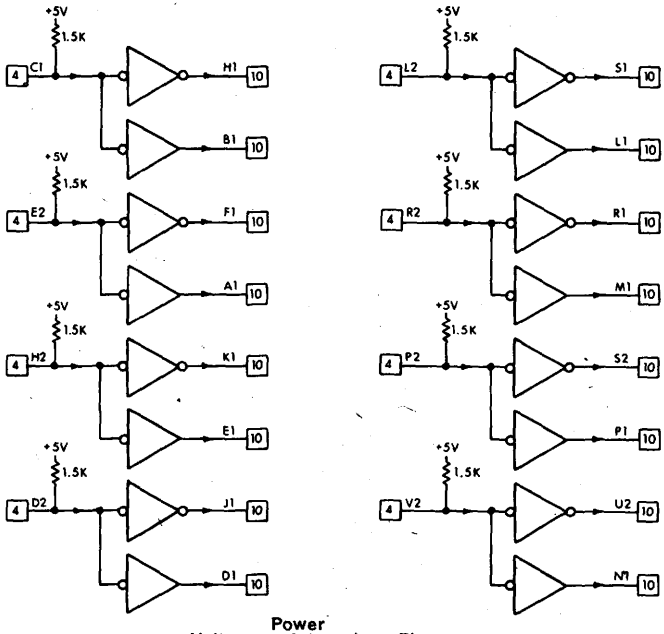
H = HIGH Voltage Level
L = LOW Voltage Level

M165
8 BUFFERS

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, F2, J2, K2, M2, N2, T1, T2

The M165 module is designed for use with circuits having open-collector output stages. The module provides a pull-up resistor for the open-collector stage and buffers the output through an inverting gate and a noninverting gate.

There are eight similar circuits on the M165 module. The value of the pull-up resistor on each input allows open-collector outputs which can sink at least 10 mA, and have a total leakage not exceeding 1.3 mA, to drive the M165 module, plus one other high-speed TTL load.

SPECIFICATIONS
Propagation Delay

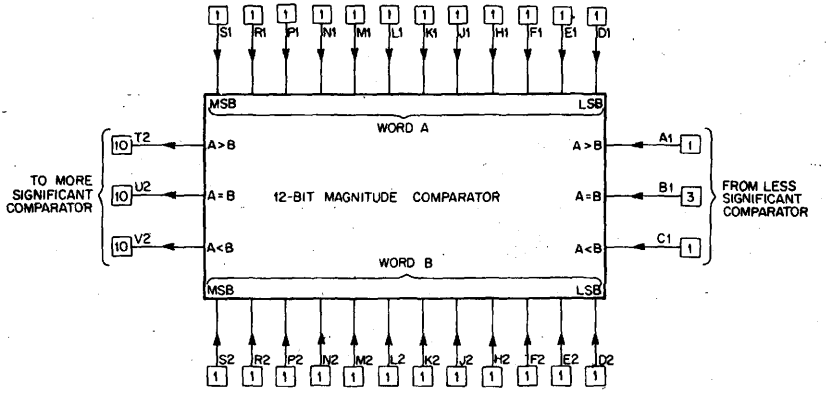
From:	To:
Input	Inverting Output, HIGH or LOW = 10 ns (max)
Input	Noninverting Output, HIGH or LOW = 15 ns (max)

M168
12-BIT MAGNITUDE COMPARATOR

ARITH-METIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	250	A2
GND		C2, T1

The M168 12-Bit Magnitude Comparator performs magnitude comparison of two 12-bit words. One of the three outputs, A > B, A = B or A < B will be high to indicate the relative magnitude of the two binary input words.

The M168 Comparator may be cascaded to compare longer words. The outputs T2, U2, and V2 should be connected to the corresponding inputs of the next comparator which are A1, B1, and C1 respectively. The inputs of the first comparator must all be made a logical "1".

The propagation delay time from Data (A and B) to outputs is 48 nsec typical and 72 nsec maximum for one unit.

When cascading the total typical time is 48 nsec plus 36 nsec per additional unit. The total maximum time is 72 nsec plus 54 nsec per additional unit.

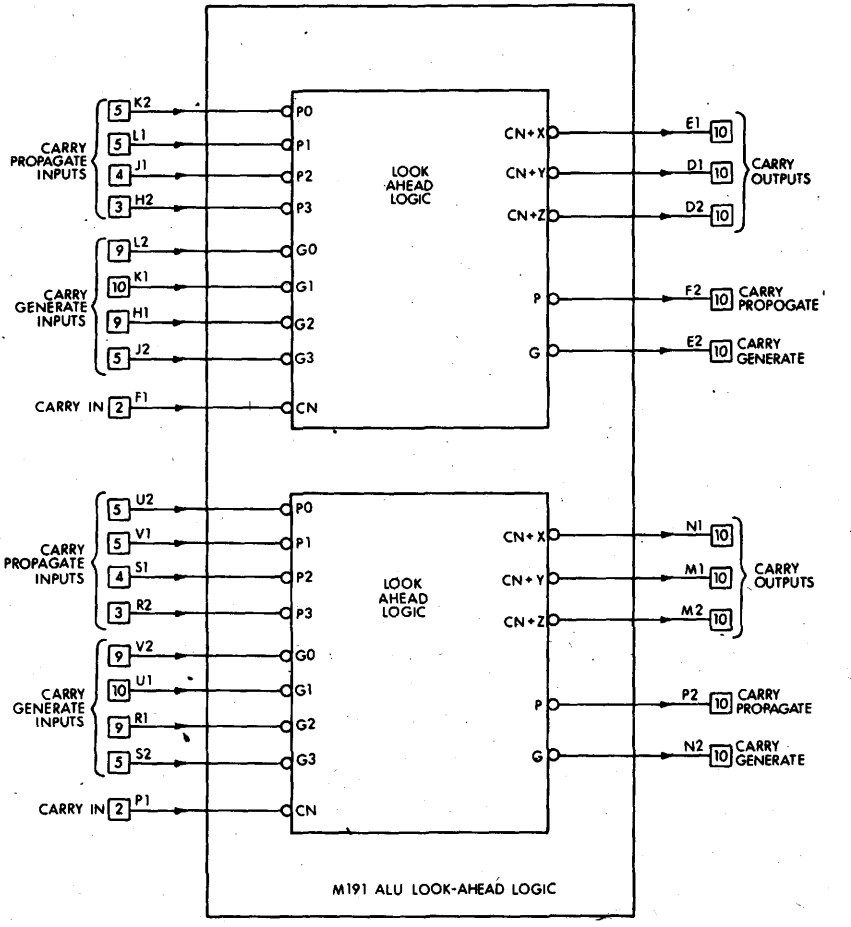
INPUTS				OUTPUTS		
A > B	A = B	A < B	Data	A > B	A = B	A < B
1	0	0	A > B	1	0	0
1	0	0	A = B	1	0	0
1	0	0	A < B	0	0	1
1 or 0	1	1 or 0	A > B	1	0	0
1 or 0	1	1 or 0	A = B	0	1	0
1 or 0	1	1 or 0	A < B	0	0	1
0	0	1	A > B	1	0	0
0	0	1	A = B	0	0	1
0	0	1	A < B	0	0	1

M191
ALU LOOK-AHEAD LOGIC

ARITH-METIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M191 contains two high-speed look-ahead units to be used to reduce the propagation delay of cascaded M159 Arithmetic Logic Units for Arithmetic Mode operations. The propagation delay is the maximum delay time from "A" to "B" word input to the "F" word output or COMPARE output. This time is 50 ns for one ALU and increases by 19 ns for each additional cascaded ALU without use of the M191. This increase is due to the 19-ns delay from 'A" or "B" word input to the first CARRY OUT and the added 19-ns delays to each succeeding CARRY OUT. However, when a look-ahead CARRY OUTPUT is substituted for an ALU CARRY OUTPUT, this time increase is only 7 ns per additional ALU. These advanced look-ahead CARRY OUTPUTS are determined by the states of the CARRY GENERATE, CARRY PROPAGATE and CARRY IN inputs.

APPLICATIONS

Figures 1 and 2 illustrate use of the module for up to 16-bit and 32-bit applications respectively.

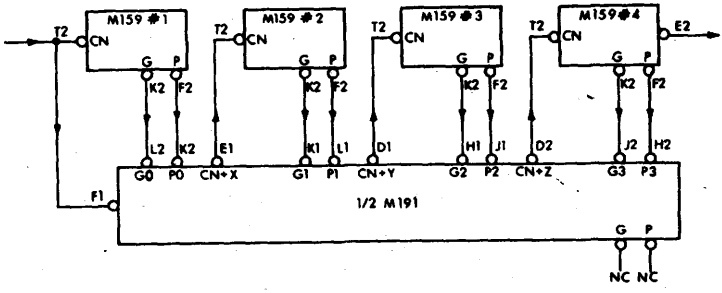


Figure 1. 16-Bit Application of M191 with M159.

NOTES:

1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns = 71 ns
2. CN+4 of most significant M159 (#4) becomes final CARRY OUT
3. For 12-bit application, M159 #4 not used; for 8-bit application, M159 #3 and #4 not used.

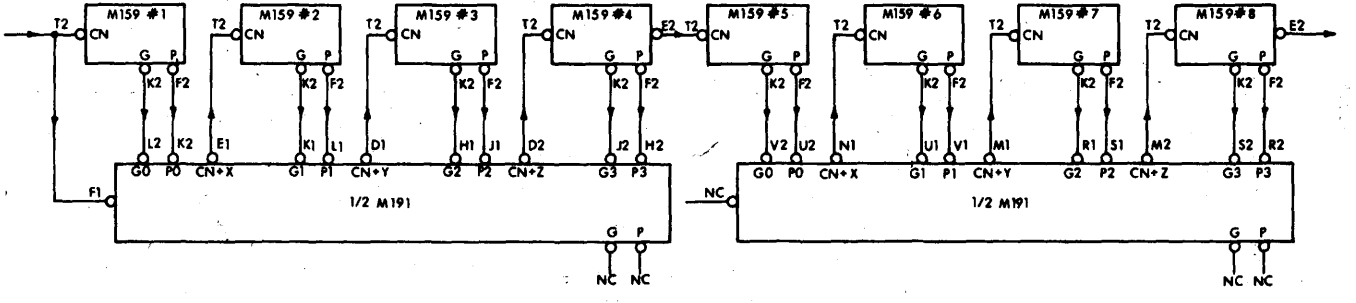


Figure 2. 32-Bit Application of M191 with M159.

NOTES:

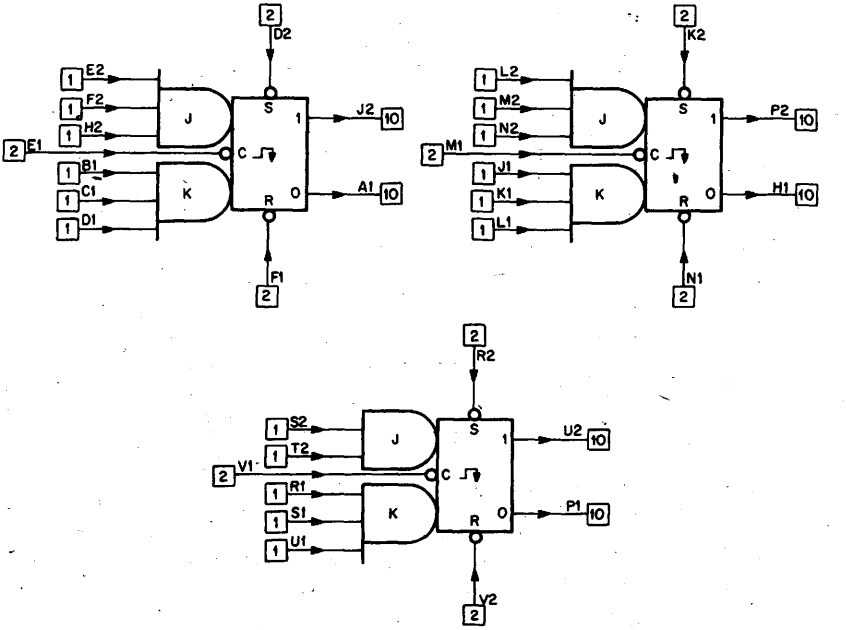
1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns + 19 ns + 7 ns + 7 ns + 7 ns = 110 ns
2. CN+4 of most significant M159 (#8) becomes final CARRY OUT
3. For 28-bit application, M159 #8 not used; for 24-bit application, M159 #8 and #7 not used, etc.

M202
TRIPLE J-K FLIP-FLOP

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	57	A2
GND		C2, T1

The M202 contains three J-K flip-flops augmented by multiple-input AND gates.

APPLICATIONS

- For general use as gated control flip-flops or buffers.

PRECAUTION

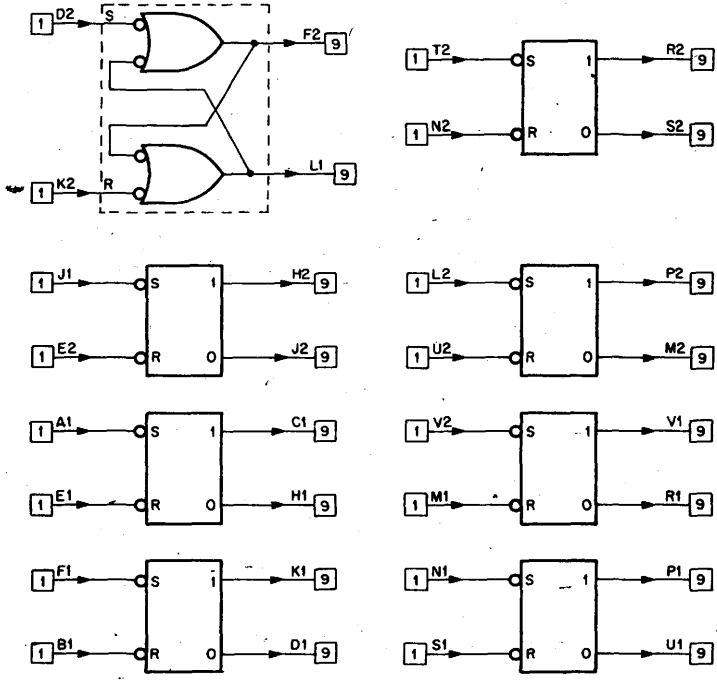
Set and clear lines should be tied to "1" level when not used.

M203
8 R/S FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M203 is made up of 8 R/S-type flip-flops. Each flip-flop is made up of two 2-input NAND gates with cross-coupled outputs.

APPLICATIONS

- R/S flip-flops provide an inexpensive method of storage.

PRECAUTIONS

Care must be taken not to place the SET and RESET inputs LOW at the same time. The last of the inputs to go HIGH will determine the final state of the flip-flop.

SPECIFICATIONS

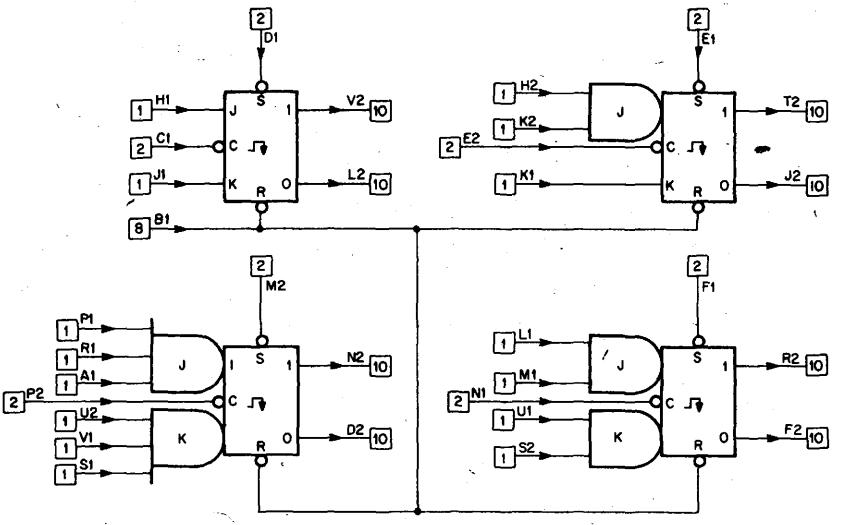
The propagation delay of the M203 is approximately 30 ns.

M204
GENERAL-PURPOSE BUFFER AND COUNTER

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	74	A2
GND		C2, T1

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, present, and input lines for each flip-flop are independent. A common CLEAR input is provided.

APPLICATIONS

- For general use as gated control flip-flops or buffers
- Counters
- Shift Registers

FUNCTIONS

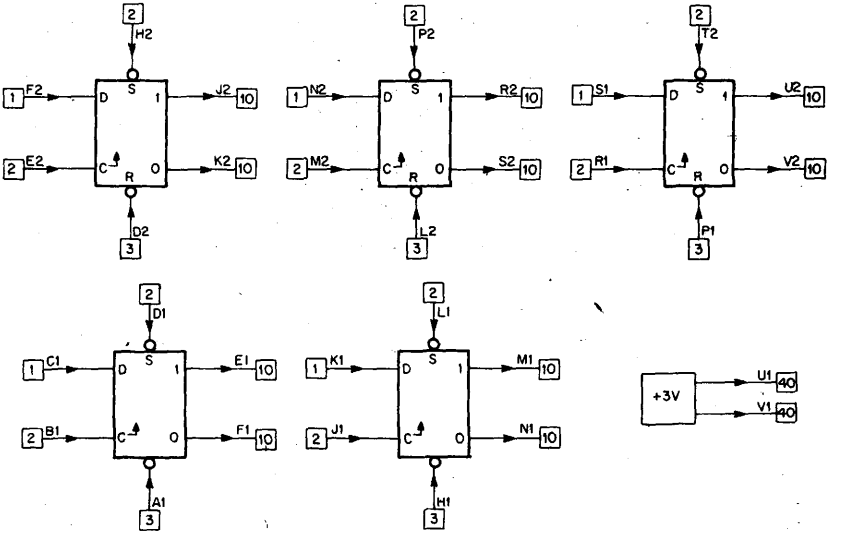
Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

M205
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	90	A2
GND		C2, T1

The M205 contains five separate D-Type flip-flops. Each flip-flop has independent gated data, clock, dc set, and dc reset inputs.

APPLICATIONS

- Storage Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse or level change.

SPECIFICATIONS

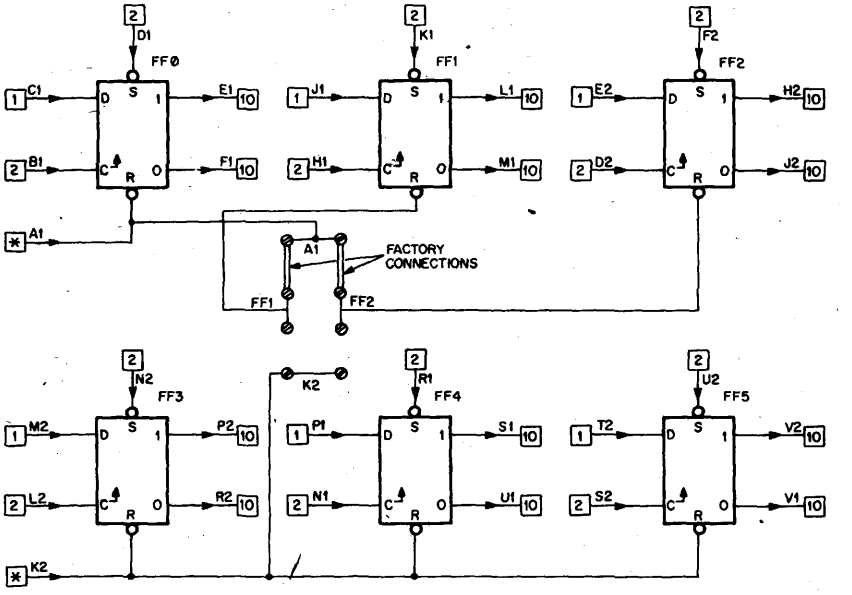
Information must be present on the D input 20 ns (max) prior to a standard clock pulse and should remain at the input at least 5 ns (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M206
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

APPLICATIONS

- Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows.

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1 & 2	FF3, 4, & 5		
2-4	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
1-5	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

A common CLEAR for all six flip-flops can be obtained by wiring pins A1 and K2 together externally.

PRECAUTION

Any unused SET or RESET input should be connected to a logic HIGH source.

Note that the loading of each CLEAR line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

SPECIFICATIONS

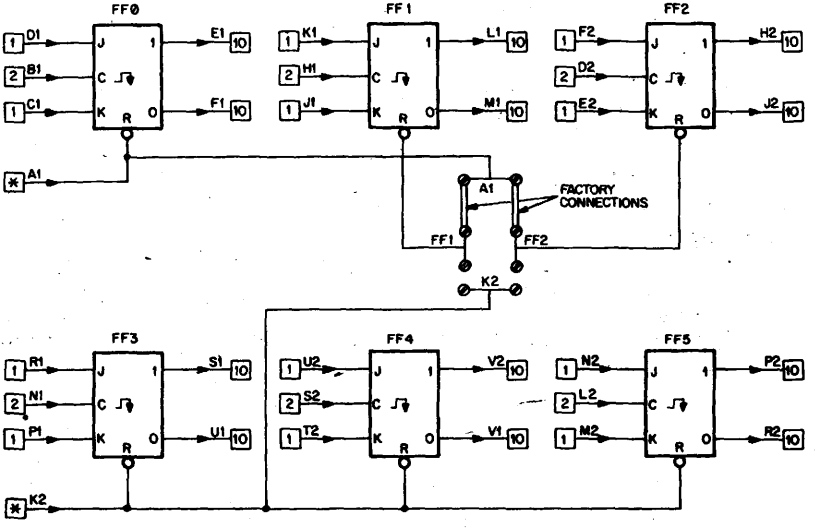
Information must be present on the D input 20 ns (min) prior to a standard clock pulse and should remain at the input at least 5 ns (min) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Minimum width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M207
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	96	A2
GND		C2, T1

The M207 contains six general-purpose J-K type flip-flops.

APPLICATIONS

- Buffers
- Control Flip-Flops
- Shift Registers
- Counters

FUNCTIONS

A truth table for clock set and reset conditions appears below. Note that when the J and K inputs are both HIGH, the flip-flop complements on each clock pulse. This makes the J-K flip-flop ideal for implementing ripple-counters by simply connecting the 1 output of one flip-flop to the C input of the next.

Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0. Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flop-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CON-FIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1 & 2	FF3, 4, & 5		
2-4	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
1-5	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF1 K2 to FF1

SPECIFICATIONS

J and K inputs must be stable during the leading-edge threshold of a standard CLOCK input and must remain stable during the positive state of the CLOCK. Data transferred into the flip-flop will be stable at the output within 30 ns (typical) of the CLOCK pulse trailing edge threshold (negative going voltage).

Application of a LOW level to an R input for at least 25 ns resets the flip-flop unconditionally.

PRECAUTION

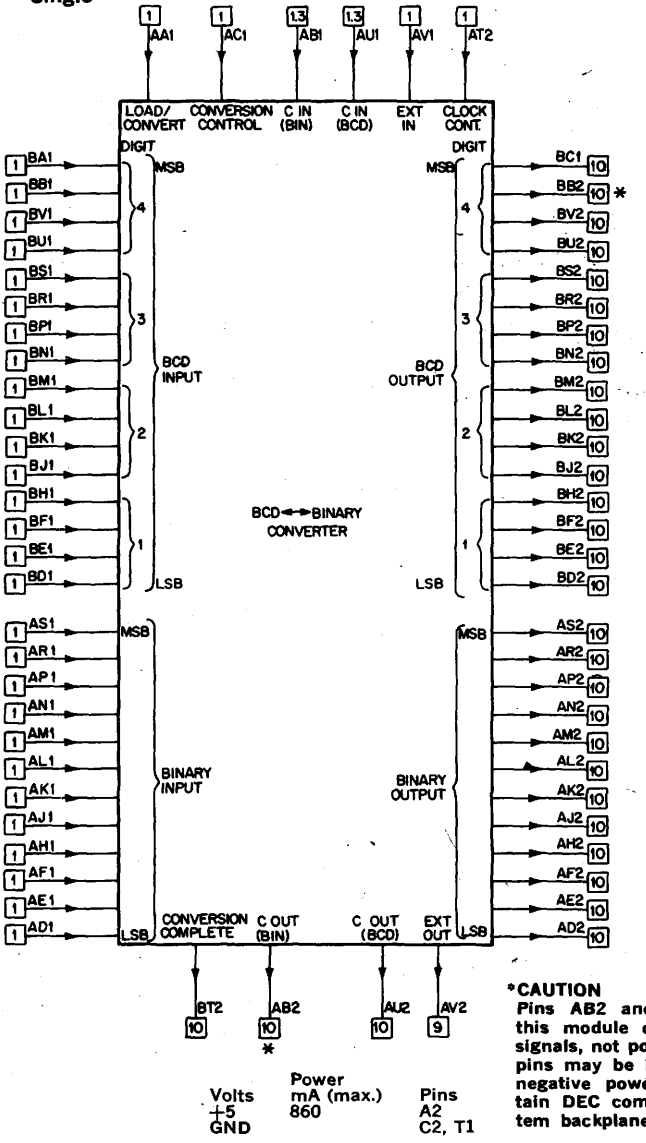
Any unused SET or RESET input should be connected to a logic HIGH source.

M230
BINARY TO BCD AND BCD TO BINARY CONVERTER

DECODERS

M SERIES

Length: Standard
Height: Double
Width: Single



***CAUTION**
Pins AB2 and BB2 on this module carry logic signals, not power; these pins may be bussed for negative power on certain DEC computer system backplanes.

The M230 converts a binary number to its binary coded decimal equivalent or a binary coded decimal number to its binary equivalent.

The maximum number that can be applied to the BCD input is 4095 which will result in all ones at the binary output. The maximum value of all ones applied to the binary input will result in the value 4095 at the BCD output. This converter utilizes a counting technique where the count frequency is typically 5 MHz. Therefore, the conversion time for the maximum number is typically 0.82 millisec.

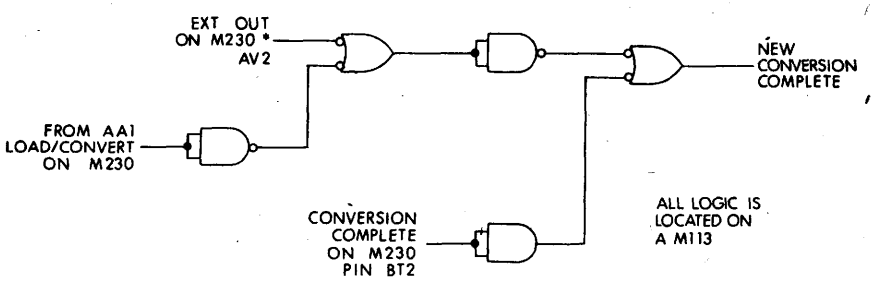
The M230 is fully cascadable. When using more than one M230 the C_{OUT} BIN. must be connected to the C_{IN} BIN. and the C_{OUT} BCD must be connected to the C_{IN} BCD of the next higher significant unit. C_{IN} BIN. and C_{IN} BCD of the least significant unit must be made a logic "1". C_{OUT} BIN. and C_{OUT} BCD of the most significant unit may be left open.

CONVERSION CONTROL on pin AC1 will cause a Binary to BCD conversion when connected to ground and a BCD to Binary conversion when connected to a logic "1" source. When cascading M230's, connect all CONVERSION CONTROL inputs in parallel.

LOAD/CONVERT on pin AA1 reads the input data when connected to a logic "1" level and starts the conversion when this input is returned to a logic "0" level. When cascading M230's, connect all LOAD/CONVERT inputs in parallel.

CONVERSION COMPLETE on pin BT2 goes High when the conversion process is finished.

There is no conversion complete signal when all low inputs are entered. This is because the circuit is designed to return the counters to a low state when load/convert signal goes high which initiates a low at all BCD and Binary inputs and the counters on the input side are always counting down to Zero. If it is likely that a circuit is required to convert Zero, use the following external configuration which utilizes the M113 Module (described elsewhere in this Handbook).



* WHEN M230 MODULES ARE CASCADED, THIS LINE CONNECTS TO THE MOST SIGNIFICANT MODULE

EXT. IN on pin AV1 and EXT. OUT on pin AV2 convey conversion finished information between cascaded M230's. This information travels from the most significant M230 to the least significant M230. Therefore, the EXT. IN of the most significant M230 **must** be connected to a logic "1" source. Each EXT. OUT is connected to the EXT. IN of the next less significant M230. The EXT. OUT of the least significant M230 is left unconnected.

CLOCK CONTROL on pin AT2 of the least significant M230 should be enabled by connecting it to a logic "1" source. All others should be connected to ground.

The following is an ordered summary for operating a single M230:

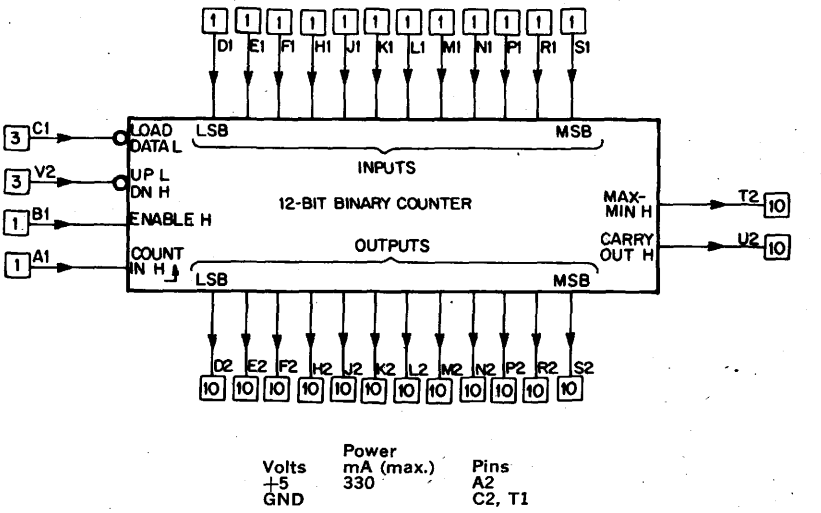
1. Make the conversion control (pin AC1) a logic "0" for converting Binary to BCD or a logic "1" for converting BCD to Binary.
2. When converting Binary to BCD, connect the Binary number to the BINARY INPUTS and ground the BCD INPUTS. Conversely, when converting BCD to Binary, connect the BCD number to the BCD INPUTS and ground the BINARY INPUTS.
3. C_{IN} BIN., C_{IN} BCD, EXT. IN, and CLOCK CONTROL inputs should be tied to a source of logic "1". The outputs C_{OUT} BIN., C_{OUT} BCD, and EXT. OUT should be left unconnected.
4. Pulse the LOAD/CONVERT input with a positive pulse of 150 nsec. minimum pulse width. There is no limit on the maximum width of this pulse. Conversion begins on the negative going edge of this pulse.
5. When converting Binary to BCD read the BCD OUTPUT for the BCD equivalent. For converting BCD to Binary read the BINARY OUTPUT for the Binary equivalent. The CONVERSION COMPLETE OUTPUT becomes a logic "1" when the conversion is through.

M236
12-BIT BINARY UP/DOWN COUNTER

COUNTERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M236 is a 12-bit synchronous binary up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M236 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one CARRY-OUT signal drives the COUNT IN input of the next M236.

APPLICATIONS

The programmability of the M236 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX-MIN output goes HIGH when all twelve bits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

CARRY OUT: When the counter has reached either the maximum up count state (4095 binary) or the minimum down count state (0000), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (4095 binary) or the minimum down count state (0000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

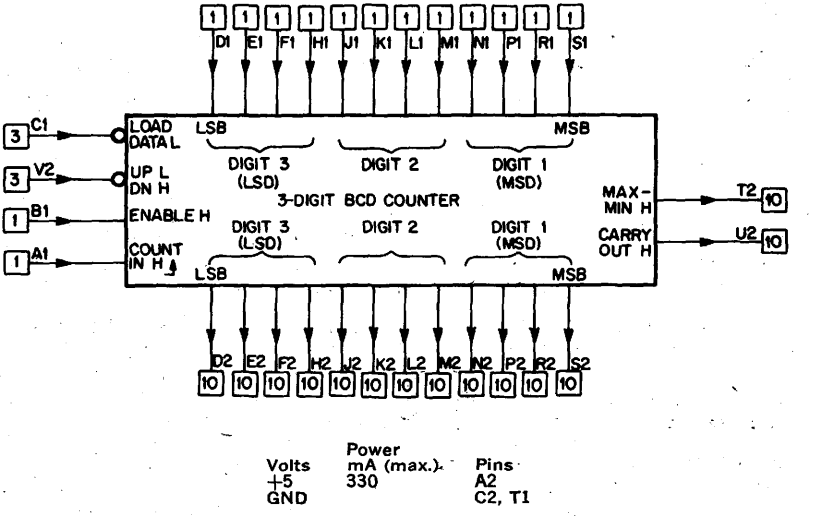
Cascading: When cascading M236's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

M237
3-DIGIT BCD UP/DOWN COUNTER

COUNTERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M237 is a 3-digit synchronous BCD up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M237 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one MAX/MIN signal drives the ENABLE input of the next M237.

APPLICATIONS

The programmability of the M237 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX/MIN output goes HIGH when all three digits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

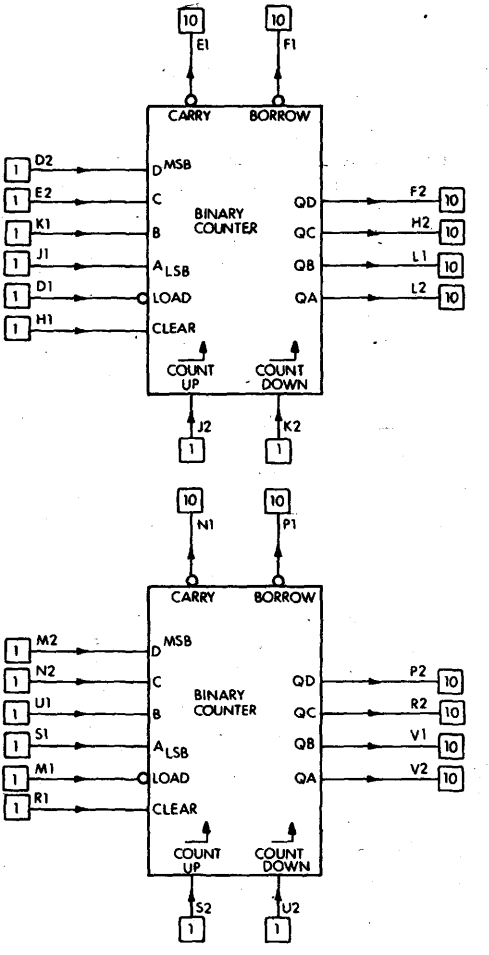
CARRY OUT: When the counter has reached either the maximum up count state (999) or the minimum down count state (000), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (999) or the minimum down count state (000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

Cascading: When cascading M237's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

M238
DUAL 4-BIT BINARY SYNCHRONOUS UP/DOWN COUNTER

Length: Standard
Width: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	180	A2
GND		C2, T1

The M238 module consists of two identical 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other.

The outputs are triggered by a LOW to HIGH level transition of either COUNT input. The direction of the counting is determined by which COUNT input is pulsed while the other COUNT input is High.

The counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the DATA inputs while the LOAD input is LOW. The output will change to agree with the DATA inputs independently of the COUNT pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the LOW level when a HIGH level is applied. The CLEAR function is independent of the COUNT and LOAD inputs.

These counters were designed to be cascaded without the need for any external circuitry. The counters can be cascaded by feeding the BORROW and CARRY outputs to the COUNT-DOWN and COUNT-UP iuputs respectively, of the succeeding counter.

CARRY L = (QA H, QB H, QC H, QD H) • (COUNT UP L)
BORROW L = (QA L, QB L, QC L, QD L) • (COUNT DOWN L)

SPECIFICATIONS
Refer to Table 1.

TABLE 1

Parameter	From Input	To Output	Max.
f max	—	—	10 MHz
t set up	—	—	25 ns
tp	Count-up	Carry	50 ns
tp	Count-down	Borrow	50 ns
tp	Either-Count	Q	50 ns
tp	Load	Q	50 ns
tp	Clear	Q	50 ns

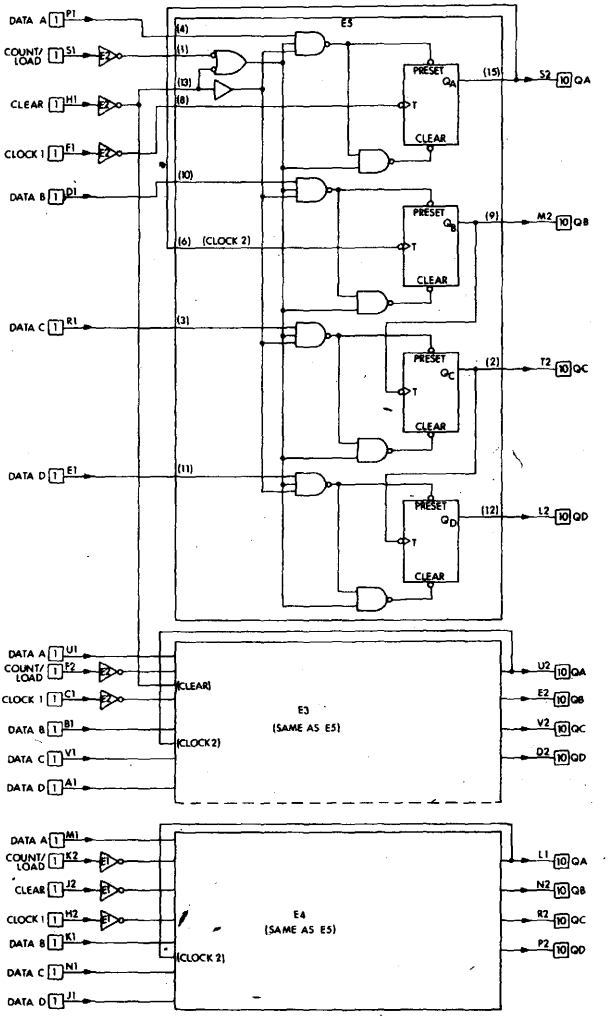
f max = Maximum Clock Freq.
tp = propagation delay time, for either a High-going or Low-going output change.

M239
THREE 4-BIT COUNTER/REGISTER

COUNTERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA	Pins
+5	70.0	A2
GND		C2, T1

The M239 Module consists of three high-speed, 4-flip-flop stage elements suitable for use as a storage register or a counter. Each of the 12 flip-flops has a data line input, and data information is entered by a COUNT/LOAD signal associated with each 4-bit stage. The output of the flip-flops assumes the logic state of the data inputs when the COUNT/LOAD input signal is High. When the COUNT/LOAD signal is Low, the data inputs are disabled, provided the clock inputs are inactive.

The Q_A output of each latch within a 4-stage element is connected to the toggle (T) input of the following latch. This allows the module to be used as a high-speed counter or serial-to-BCD converter.

The counters will accept frequencies of 0-50 MHz at the CLOCK 1 input, and the transfer of information to the outputs occurs at the positive-going edge of this clock pulse.

One CLEAR input is common to the eight latches in elements 1 and 2, and one CLEAR input is common to the four latches in the third element. When the CLEAR signal becomes a High logic level, all associated latch outputs will become Low regardless of the CLOCK 1 input level.

APPLICATIONS

Provides 12-bit data storage or a serial counter with 12-BCD outputs. All inputs and outputs are TTL or DTL compatible.

FUNCTION

When operated as a serial counter, the Q_D output of a 4-latch element must be connected to the CLOCK 1 input of the following 4-latch element. The separate CLEAR inputs may also be externally connected to reset all latch outputs using one CLEAR input signal (High transition). Output Q_A maintains 10 unit load capability in addition to driving the CLOCK 2 input. Refer to the Function Tables for the output levels of each count.

SPECIFICATIONS

Input Voltage (max.): 5.0 Volts ± 5%
Clock Frequency: 0-50 MHz

FUNCTION TABLE

CLOCK PULSE	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

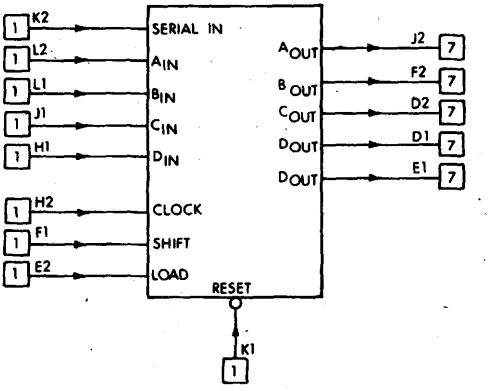
NOTE: Output count continues in sequence when Q_D output is connected to the clock 1 input of next 4-latch element.

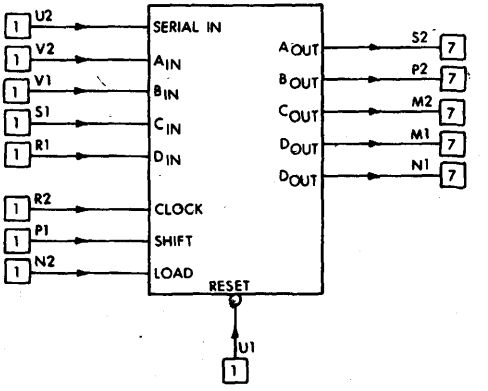
M245
DUAL 4-BIT
SHIFT REGISTER

SHIFT/ STORAGE REGISTERS

M SERIES

Length: Standard
Height: Single
Width: Single





Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M245 module consists of two 4-bit shift registers with both serial and parallel data entry capability. They are shift-right only registers; that is, the output data is shifted from A toward D.

Three control modes are possible: serial shift right, parallel enter mode, and no change or hold mode. These control modes are chosen by inputs at the SHIFT and LOAD lines as shown in the Truth Table.

In the serial mode of operation, data present at the SERIAL INput, when the SHIFT input is High, is loaded on the Low-going edge of the CLOCK pulse.

In the parallel entry mode, data present at the data inputs A IN through D IN, when the LOAD line is High, is loaded on the Low-going edge of the CLOCK pulse.

The hold mode is created by holding both the LOAD and SHIFT lines Low. By doing this, the CLOCK pulse will have no effect on the output, regardless of data present at the SERIAL INputs or DATA INputs.

A RESET line has been provided for the registers which will clear the internal flip-flop circuitry.

SPECIFICATIONS

Transfer Rate	= 10 MHz (max)
SHIFT Set-up Time	= 50 ns (min)
LOAD SET-up Time	= 50 (min)
DATA IN Set-up Time	= 25 ns (min)

Propagation Delay

From:	To:
CLOCK	Output (HIGH or LOW) = 50 ns (max)

TRUTH TABLE

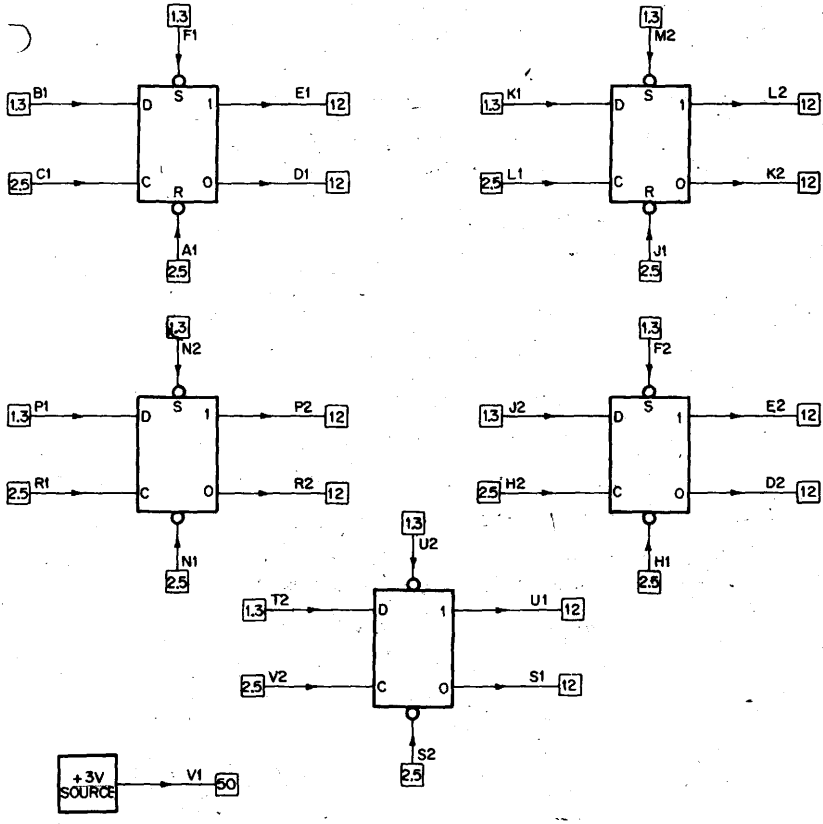
CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Serial Shift Right	L	H

M246
5 D-TYPE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, M1, T1

The M246 module contains five high-speed, general-purpose, D-type flip-flops. Each flip-flop has its SET(S), RESET(R), CLOCK(C), DATA(D), and outputs brought out to separate pins.

The information at the D or DATA input is transferred to the 1 output on the positive-going edge of the CLOCK pulse. The CLOCK-triggering occurs at a voltage level of the CLOCK pulse and is not directly related to the transition time of the positive-going pulse.

SPECIFICATIONS

Clock Freq	= 35 MHz (max)
CLOCK Pulse	= 15 ns (min)
SET Pulse	= 25 ns (min)
RESET Pulse	= 25 ns (min)
DATA Set-up Time	= 15 ns (min)

Propagation Delay Time

From:	To:
SET or RESET	LOW or HIGH Output = 20 ns (max)
CLOCK	LOW or HIGH Output = 20 ns (max)

TRUTH TABLE (Each Flip-Flop)

t_n	t_n+1	
INPUT D	OUTPUT 1	OUTPUT 0
L	L	H
H	H	L

where: t_n = bit time before CLOCK pulse

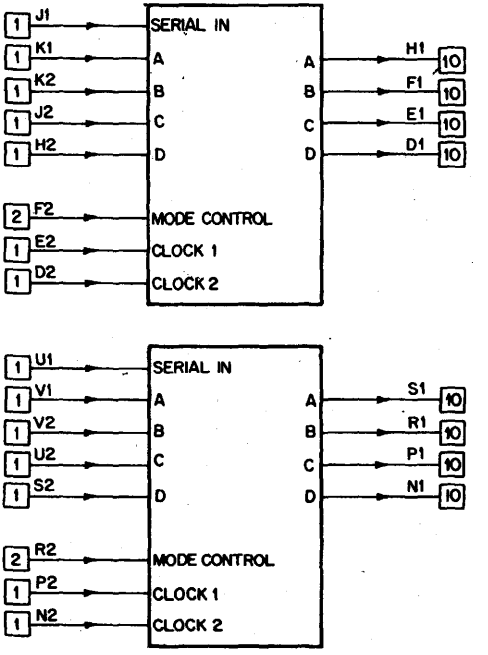
where: t_{n+1} = bit time after CLOCK pulse

NOTE: The M246 module also contains a +3V logic High source at pin V1 which can be used to tie up to 50 M Series inputs High.

M248
DUAL 4-BIT
MULTIPURPOSE SHIFT REGISTER

SHIFT/ STORAGE REGISTERS
M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M248 module consists of two 4-bit Shift registers—multipurpose in the fact that they are capable of either serial or parallel entry, shifting right, or with simple external connections, shifting left.

When a logic LOW is applied to the MODE CONTROL input, a shift right operation is performed by clocking at the CLOCK 1 input. In this mode, serial data is entered at the SERIAL INput. CLOCK 2 and parallel inputs A through D are inhibited.

When a logic HIGH is applied to the MODE CONTROL input, it allows entry of parallel data through inputs A through D and CLOCK 2. This mode permits parallel loading of the register or, with external interconnection, shift left operation. In this mode, shift left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop; that is, D output to C input, etc., and serial data is entered at input D.

Two clock inputs are available which permit separate clock sources to be used for the shift right and shift left modes. If both modes can be clocked from the same source, the clock input may be applied to both CLOCK 1 and CLOCK 2. The transfer of information to the output pins occurs when the clock input goes from a logic High to a logic Low.

SPECIFICATIONS

Shift Freq = 10 MHz (max)

Propagation Delay

From:	To:
CLOCKS	High or Low Output = 40 ns (max)

Set-up Time:

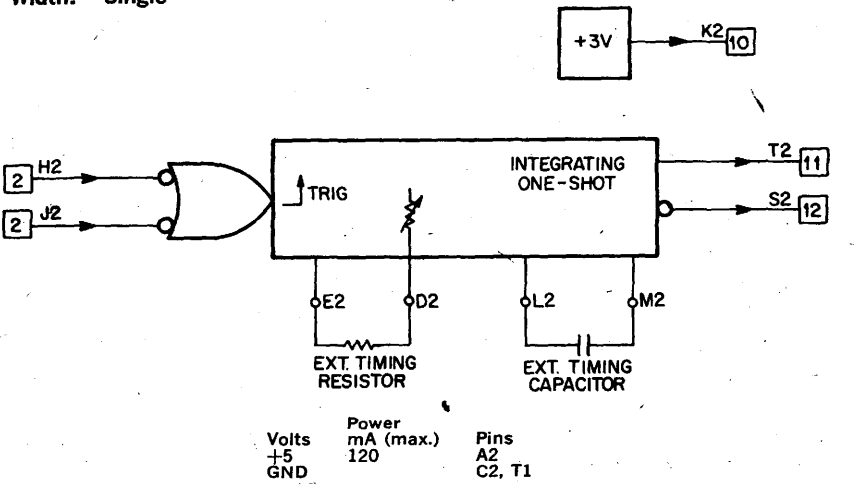
SERIAL Input A, B, C, D = 20 ns (min)
MODE CONTROL with respect to CLOCKS = 25 ns (min)

M306
INTEGRATING ONE SHOT

MULTI-VIBRATORS

M SERIES

Length: Standard
Height: Single
Width: Single

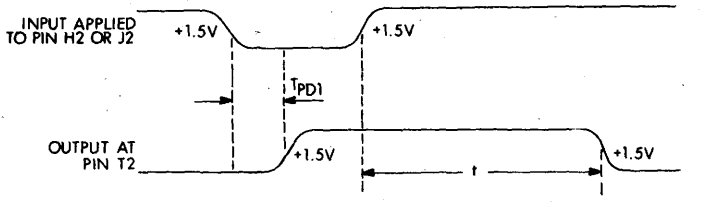


Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M306 is a zero-recovery-time integrating monostable multivibrator with complementary outputs. The M306 has the ability to respond to an input even while in the active state, so that successive inputs above a preset frequency can postpone the return to the inactive state indefinitely.

FUNCTIONS

The operation of the M306 is illustrated in the timing diagram shown below:



The integration period is measured from the trailing edge of the input pulse to the trailing edge of the output pulse. The approximate integration time may be calculated by the following:

$$t \sim .68\,(R + 800\ \Omega)\,(C + 75 \times 10^{-12}F) + 70 \times 10^{-9}\ \text{Sec.}$$

where R is in ohms and C is in farads. The integration time is independent of the width of the input pulse.

Timing Capacitors: Coarse adjustment of the integration period is accomplished by customer-supplied capacitors which may be attached to module pins L2 and M2. When using polarized capacitors, the positive terminal should be connected to pin L2. Two split lugs are provided on the module for those customers who would like to permanently install the capacitor on the module itself. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250K ohms.

Timing Resistance: Fine adjustment of the timing period may be accomplished by a multiturn potentiometer provided on the module. Provision is also made to allow the customer to connect an external timing resistor or potentiometer between pins D2 and E2. When an external potentiometer is used, care should be taken to prevent the coupling of externally generated electrical noise into the module. The maximum resistance of the timing resistance, including the 20K ohm internally provided potentiometer, should not exceed 25,000 ohms. If an external timing resistor is not used, pins D2 and E2 must be connected together.

SPECIFICATIONS

Trigger Duration: An input pulse of 30 ns will trigger the M306. TPD1 = 40 ns max.

Output Duration: The minimum pulse width is 225 ns and maximum pulse width is limited only by capacitor leakage (40 sec is a typical maximum).

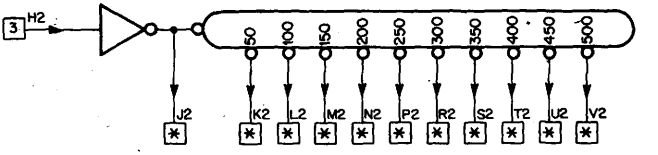
Stability: The inherent temperature stability of the M306 is normally —.06% per degree C, exclusive of the temperature coefficient of the timing capacitor.

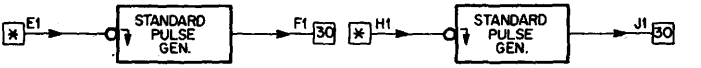
M310
DELAY LINE

MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Single
Width: Single





*=SEE TEXT

Volts	Power mA (max.)	Pins
+5	89	A2
GND		C2, T1

The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

APPLICATIONS

- Timing pulse trains
- Pulse spacing

FUNCTIONS

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yields the minimum delay and the tap V2 yields the maximum delay.

Loads J2-V2 designed to be loaded only by E1 or H1. They will not drive standard TTL loads.

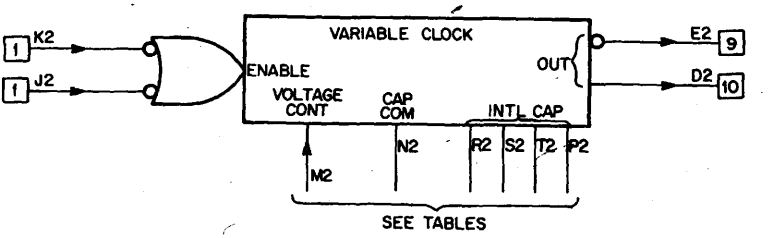
The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

M401
VARIABLE CLOCK

CLOCKS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80*	A2
GND		C2, T1

* using printed circuit board revision E or later

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

Repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A 0 to 10 volt control voltage will vary the frequency over about 30% of each frequency range.

APPLICATIONS
This module is intended for use as the primary source of timing signals in a digital system.

FUNCTIONS
Start Control: A two-input OR gating input is provided for start-stop control of the pulse train. A level change from HIGH to LOW with fall time less than 400 ns is required to enable the clock.

Frequency Range:

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz	(.01 μfd)	N2 — S2
1.75 KHz to 17.5 KHz	(0.1 μfd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 μfd)	N2 — P2

Fine Frequency Adjustment: Controlled by an internal potentiometer. No provision is made for any external connections. An external capacitor may be added by connection between pins N2 and C2.

Voltage Control of Frequency: The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision E or later. The voltage applied to pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 μF. If the voltage applied to pin M is dc or low frequency (below 1 kHz), pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10 volt P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to pin M, will yield a typical frequency excursion in excess of plus or minus 15% about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
				Output frequency in KHz

SPECIFICATIONS

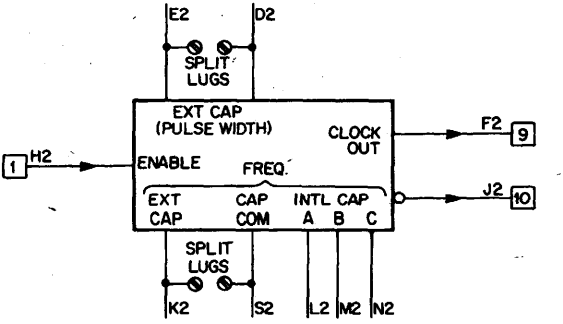
Maximum delay from enabling inputs to output E2 is 50 nanoseconds. The output pulse width is 50 nanoseconds.

M403
RC MULTIVIBRATOR CLOCK

CLOCKS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M403 is an RC Multivibrator Clock which produces standard 10-microsecond timing pulses at repetition rates adjustable from 1 kHz to 50 kHz in three ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control, while an internal potentiometer provides continuously variable adjustment within each range.

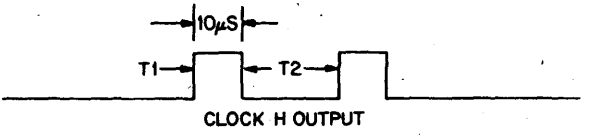
APPLICATIONS
This module can be used as a source of digital timing signals.

FUNCTIONS
ENABLE Input: The clock circuit is enabled by a HIGH level on pin H2. If a LOW level is applied to pin H2, the clock output at F2 will time out and return to ground and the output at pin J2 will time out and go HIGH. To prevent an erroneous count, pin H2 should not be retriggered for one complete period. This will allow the circuit to settle.

Selecting Frequency Range: The frequency range is selected by jumpers at backplane pins:

FREQUENCY RANGE	INTERCONNECTION REQUIRED
1 kHz to 5 kHz	N2 — S2
5 kHz to 20 kHz	M2 — S2
20 kHz to 50 kHz	L2 — S2

Lowering Frequency: If frequencies below the capabilities of this circuit are necessary, external capacitance can be added. Time 2 (see illustration) can be changd by installing capacitors to the split lugs provided or between pins K2 and S2. New timing values can be calculated using the following equation:



$T2 = 0.32\,RC\,(1 + 0.7/R)$

T2 is in seconds, R is in ohms, and C is in farads. The internal potentiometer varies between 5.1K and 50K ohms.

Increasing Pulse Width: Larger pulse widths can also be obtained by adding capacitance to the other set of split lugs provided or between pins E2 and D2. The same equation as above may be used for T1 with the following exception:

$$C = 4.7 \text{ picofarads} + \text{capacitance added}$$

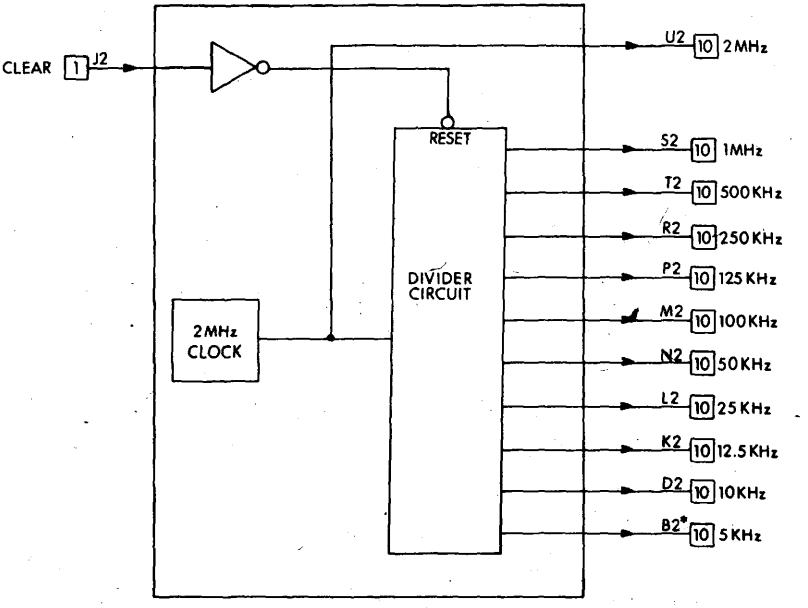
SPECIFICATIONS
Rise Time: 25 ns (max.)
Fall Time: 25 ns (max.)

M404
CRYSTAL CLOCK

CLOCKS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	535	A2
GND		C2, T1

***CAUTION**
This pin may connect to negative power on certain DEC computer system backplanes.

The M404 clock contains a 2 MHz crystal oscillator and frequency dividers.

A HIGH on the CLEAR input clears the frequency divider and all outputs go LOW except the 2 MHz output, which is not affected.

SPECIFICATIONS

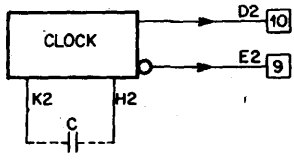
Accuracy: Maximum error from specified output frequency is 0.01% between 0 degrees C and +55 degrees C.

M405
CRYSTAL CLOCK

CLOCKS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M405 employs a crystal oscillator to provide a highly stable 10 MHz clock signal.

APPLICATIONS

- Stable clock frequencies

FUNCTIONS

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 50 ns pulses. Pulses at pins D2 and E2 are time shifted by one gate delay with the negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 ns. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 ns per 2.5 pF of additional capacitance.

SPECIFICATIONS

Frequency Stability: 0.01% of crystal value between 0 degrees C and +55 degrees C.

Standard Frequency: 10.000 MHz.

NOTE

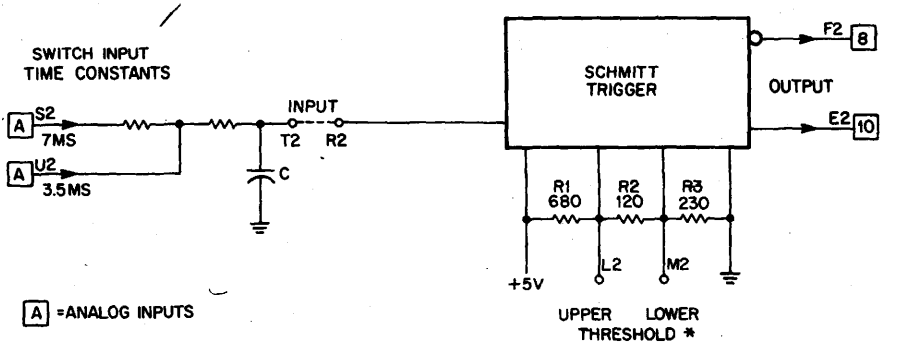
It is recommended that the M4050 be used in place of the M405 for all new designs in which frequencies of up to 5 MHz are required.

M501
SCHMITT TRIGGER

PULSE SHAPING

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	31	A2
GND		C2

The M501 is a Schmitt Trigger with variable thresholds and complementary positive logic outputs.

APPLICATIONS

- Switch Filter
- Pulse Shaper
- Threshold Detector

FUNCTIONS

The input on pin R2 is compared with the thresholds set on pins L2 and M2 UPPER and LOWER respectively.

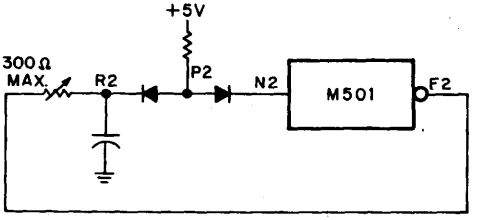
Pin F2 goes to LOW when the input on R2 rises above the UPPER THRESHOLD, having been below the LOWER THRESHOLD.

Pin F2 rises to +3 volts when the input on R2 falls below the LOWER THRESHOLD, having been above the UPPER THRESHOLD.

Pin E2 is the complement of F2.

Miscellaneous Input Functions: An integrator is provided on the input, allowing switches to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch time constants are provided. Inputs to pin S2 result in a 7 ms time constant, to pin U2 3.5 ms.

Oscillator Connection: Connecting a resistor from output pin F to input pin R with pin T tied to pin R forms an oscillator.



SPECIFICATIONS

Input Signal Swing: The voltage on pin R2 is limited to plus or minus 20 volts.

Thresholds: The UPPER and LOWER THRESHOLDS are preset at 1.7 and 1.1 volts. They may be modified by the addition of a resistor in parallel with the internal network; however, the UPPER THRESHOLD must not exceed 2.0 volts or the LOWER THRESHOLD fall below 0.8 volts.

R	IN	PARALLEL WITH	R2 — THRESHOLD CLOSER
R		PARALLEL	R1 — UPPER RISES
R		PARALLEL	R3 — LOWER FALLS

Input Pin R2 Loading: 2.7K ohms to +5 volts or 1.8 mA at ground.

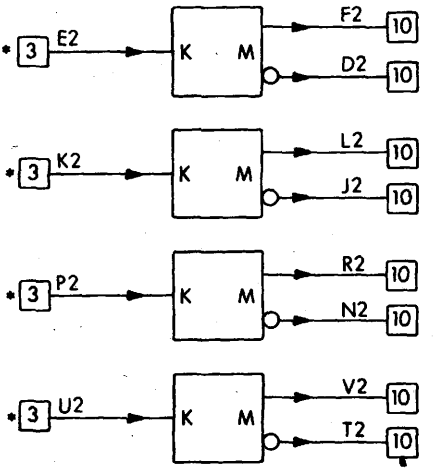
Pin	P2	AND EXPAND input
Pin	N2	OR EXPAND input
Pin	S2	RC SWITCH input filter 7 ms
Pin	U2	RC SWITCH input filter 3.5 ms
Pins	L2, M2	are available for threshold modification

M521
K TO M CONVERTER (SCHMITT TRIGGER)

PULSE SHAPING

M SERIES

Length: Single
Height: Single
Width: Single



*REPRESENTS 3K SERIES LOADS OR 2M SERIES LOADS

Volts	Power mA (max.)	Pins
+5	56	A2
GND		C2

The M521 K Series to M Series Converter contains four Schmitt Trigger circuits which can convert any K Series signal to complementing M Series signals.

APPLICATIONS

- Schmitt Trigger
- Rise Time Conversion — K to M Series

FUNCTIONS

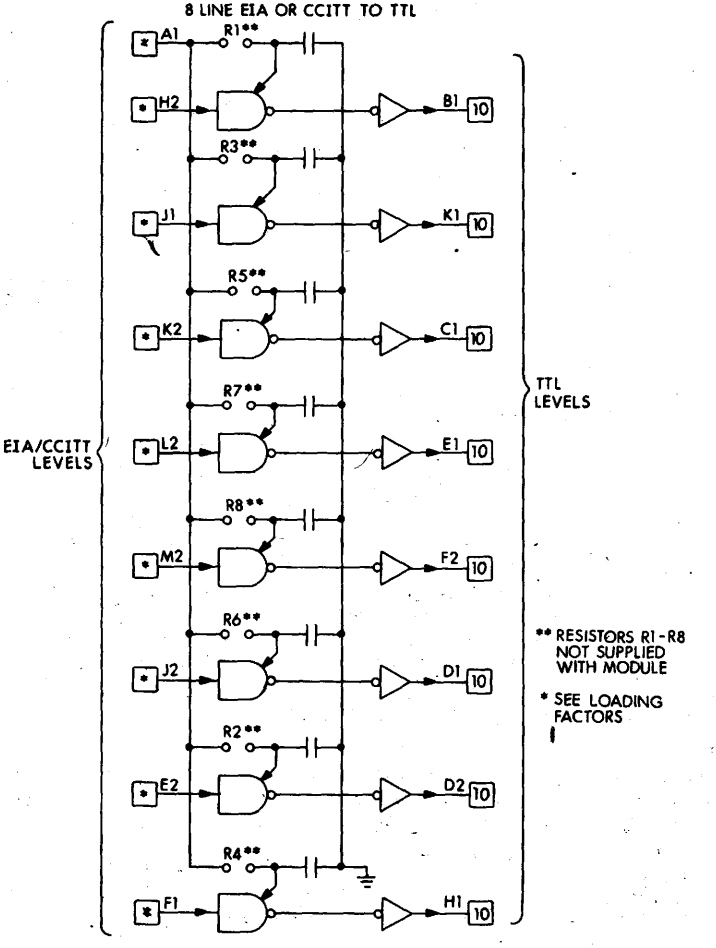
Typically, the output of a K Series gate would have a 7 μs rise time and a 1.5 μs fall time. The M521 speeds both these rise and fall times to approximately 15 ns. The input circuit has built-in hysteresis and is slowed to a maximum frequency of 100 KHz.

M594
EIA/CCITT LEVEL CONVERTER

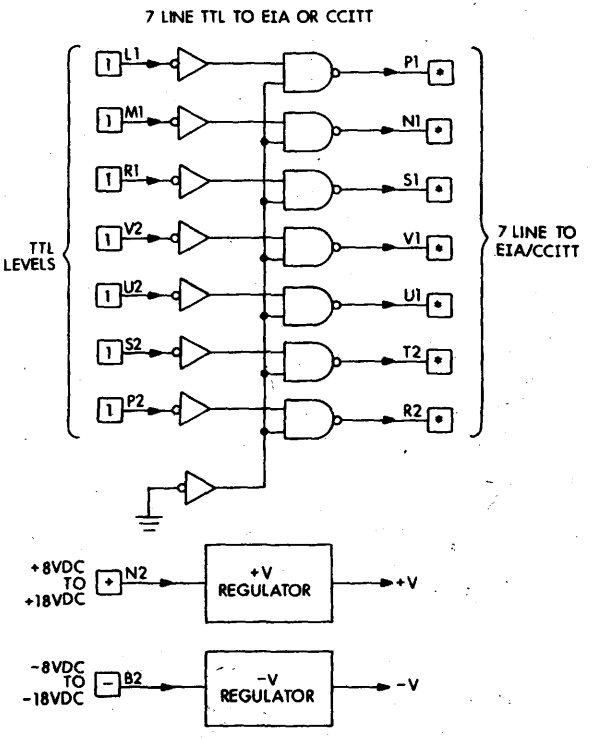
COMMUNICATIONS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	125	A2
GND		C2, T1
+15V	25	
−15V	25	



The M594 Module is used to convert the signal voltage levels between DIGITAL data processing terminal equipment such as the DF11 Modem and data communications equipment such as a Bell data set. The M594 provides circuits to convert a maximum of eight EIA or CCITT signal levels to eight DTL or TTL signals that are compatible with DIGITAL logic, and circuits to convert a maximum of seven DIGITAL, TTL, or DTL logic signal outputs to seven signals compatible with EIA or CCITT signal devices. Refer to EIA Standard RS-232-C for description of the selected signals.

FUNCTION

The eight-line EIA or CCITT to TTL converter receives input signals which can vary between +30 Vdc and −30 Vdc. Each input operates on a hysteresis curve or double threshold to prevent noise triggering. The threshold level is determined by the external bias voltage applied to pin A1 of the module and by the value of resistors R1 through R8. A LOW (mark) EIA/CCITT input voltage produces a LOW (0) TTL compatible level output and a HIGH (space) input level results in a HIGH (1) TTL compatible level output.

The seven-line TTL to EIA or CCITT circuits contain inverters and line drivers and can provide output signals which vary between a maximum of +10 Vdc and −10 Vdc from standard DTL or TTL logic inputs. Power to the line drivers is from two voltage regulator circuits contained on the M594. The positive external voltage supplied to the regulators can be any value between +8 Vdc

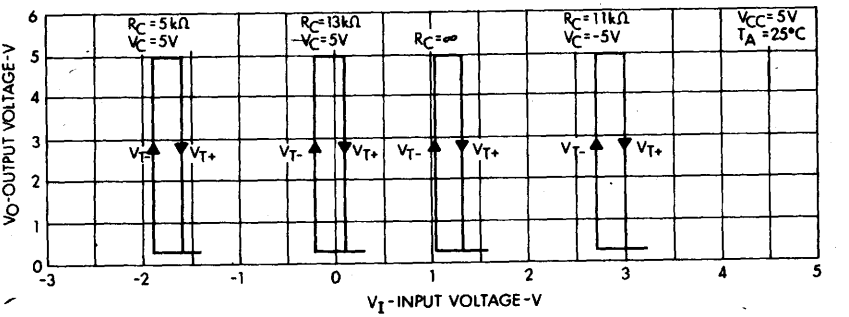
and +18 Vdc, and minus external voltage can be any value between −8 Vdc and −18 Vdc. A LOW (0) TTL compatible level input produces a LOW (mark) EIA/CCITT −10 Vdc level output and a HIGH (1) TTL compatible level input produces a HIGH (space) EIA/CCITT +10 Vdc output.

APPLICATIONS

Convert EIA or CCITT levels from Bell or Western Union Modems to TTL or DTL levels for data communications equipment.

Convert TTL or DTL compatible levels to Bell or Western Union modem signals.

Refer to the following curve for determining the value of resistors R1 through R8 which vary the input voltage threshold of the 8-line EIA/CCITT to DTL level converter. The input voltage threshold, without resistors R1 through R8 recounted, is ±1.0 V. With a V_{CC} of −15 V on pin A1 and a resistor value of 33K ohms in R1 through R8, the input voltage threshold is approx. ±2.5 V.



V_C applied to pin A1

LOADING FACTORS

EIA to TTL (Pins H2, J1, K2, L2, M2, J2, E2, F1)

Input Voltage (V_I)	High Level Input Current (I_{IH})
+25 V	8.3 mA (max.)
+3 V	0.43 mA (min.)
	Low Level Input Current (I_{IL})
−25 V	−8.3 mA (max.)
−3 V	−0.43 mA (min.)

TTL to EIA (Pins P1, N1, S1, V1, U1, T2, R2)
(Low level input voltage V_{IL} = 0.8V, Load Resistor R_L = 3KΩ)

V_{CC}+	V_{CC}−	High level output voltage V_{OH}
+9 V	−9 V	6 V (min.)
+13.2 V	−13.2 V	9 V (min.)

(High level input voltage V_{HL} = 1.9 V, Load Resistor 3KΩ

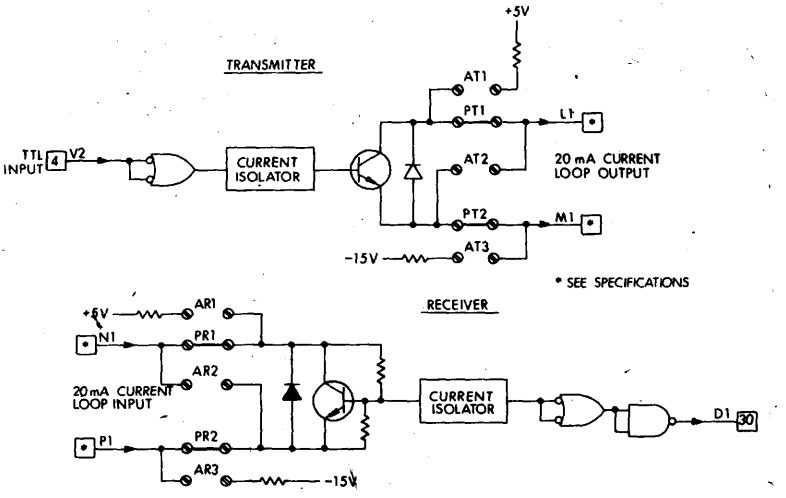
V_{CC}+	V_{CC}−	Low level output voltage V_{OL}
+9 V	−9 V	−6 V (max.)
+13.2 V	−13.2 V	−9 V (max.)

M598
1-CHANNEL TRANSMIT/RECEIVE OPTIC-COUPLED CURRENT ISOLATOR

COMMUNICATIONS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	100	A2
GND		C2, T1
−15V	40	B2

The M598 module contains a single-channel transmit and a single-channel receive circuit capable of converting the data signals between a Teletype ® or similar current loop device and TTL or DTL compatible logic circuits. The data signals transferred through each of the module circuits are optically-coupled to provide a maximum of 1500 V isolation between the current loop and the TTL logic. The transmitter receives serial TTL or DTL compatible levels and controls an output current loop with a maximum current of up to 80 mA.

The receiver circuit responds to input currents of a maximum of 80 mA from a Teletype or similar current loop device and provides serial TTL or DTL compatible signals at the output.

The M598 module is supplied with jumper leads installed to operate as a passive element providing no current to the current loop device. By rewiring the jumper leads on the transmitter and receiver circuits, the module can be an active element and supply current from a +5 Vdc or −15 Vdc source.

APPLICATIONS

Provides up to 1500 V isolation in the data and control lines between TTL or DTL compatible logic and a current loop device such as a TTY. As an active element the M598 performs signal level conversion without isolation.

FUNCTION

A High level at input pin V2 of the transmitter opens the transistor in the output current loop. A Low level causes the transistor to conduct. No current flow at the input of the receive circuit results in a High level at output pin D1 and current flow at the input results in a Low level at pin D1.

SPECIFICATIONS

Signals: The characteristics of the input and output levels and the current and voltage limits of the current loop are listed as follows. The maximum transfer rate of the transmitter or receiver is 4.8 K baud.

PIN	NAME	CHARACTERISTICS		
D1	Received Data, TTL levels	High output level = space = no current flowing in current loop.		
V2	Transmitted Data TTL Levels	High input level = space = no current flowing in current loop.		
			Min	Max
L1	Transmitted Data Most positive	Open circuit voltage	5.0 volts	80 V
		Transmitter voltage drop (marking)	0.5 volts	2.0 V
M1	Transmitted data, Most negative	Marking current	20 mA	80 mA
		Spacing current	0.5 mA	2.0 mA
			Min	Max
N1	Received Data, Most positive	Receiver voltage drop	—	2.5 volts
P1	Received Data Most negative	Marking current	15 mA	80 mA
		Spacing current	—	5.0 mA

Connect the jumpers as indicated on the following table.

CONNECT JUMPERS

	Active**	Passive*
Transmitter	AT1, AT2, AT3	PT1, PT2
Receiver	AR1, AR2, AR3	PR1, PR2

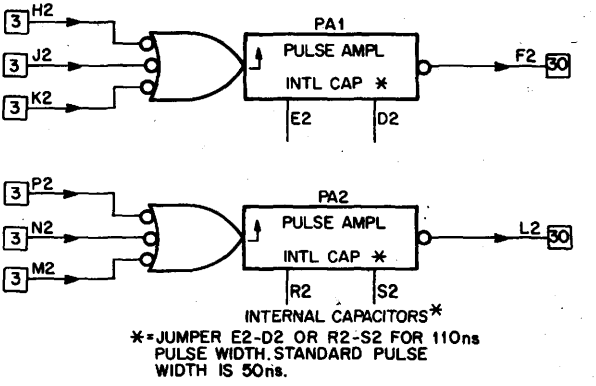
* Jumpers inserted during manufacturing
** Requires −15 V in this configuration

M602
PULSE AMPLIFIER

MULTI-VIBRATORS

M SERIES

Length: Standard
Height: Single
Width: Single



*=JUMPER E2-D2 OR R2-S2 FOR 110ns PULSE WIDTH. STANDARD PULSE WIDTH IS 50ns.

Volts	Power mA (max.)	Pins
+5	213	A2
GND		C2, T1

The M602 contains two pulse amplifiers which provide power amplification, and transform level changes into pulses.

FUNCTIONS

A negative pulse output is produced when the input is triggered by a transition from HIGH to LOW. An internal capacitor is brought out to pin connections to permit the standard 50 ns output pulse to be increased to 110 ns (nominal).

SPECIFICATIONS

Propagation Time: 30 ns max. between input and output thresholds.

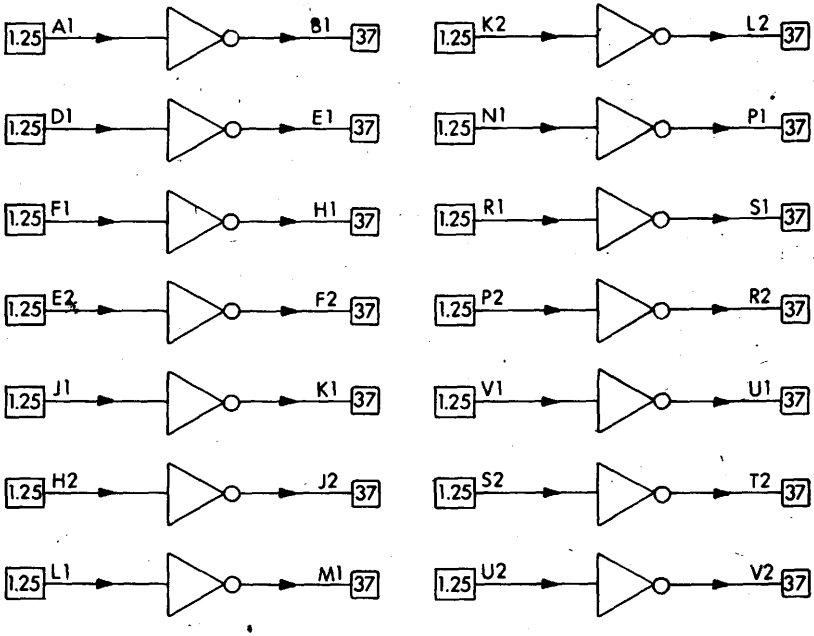
Recovery Time: Equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 ns and must remain below 0.8 volts for at least 30 ns. Maximum PRF is 10 MHz.

M611
HIGH SPEED POWER INVERTER

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	280	A2
GND		C2, T1, C1, M2, N2

Fourteen high speed Inverters with input/output connections as shown.

APPLICATIONS

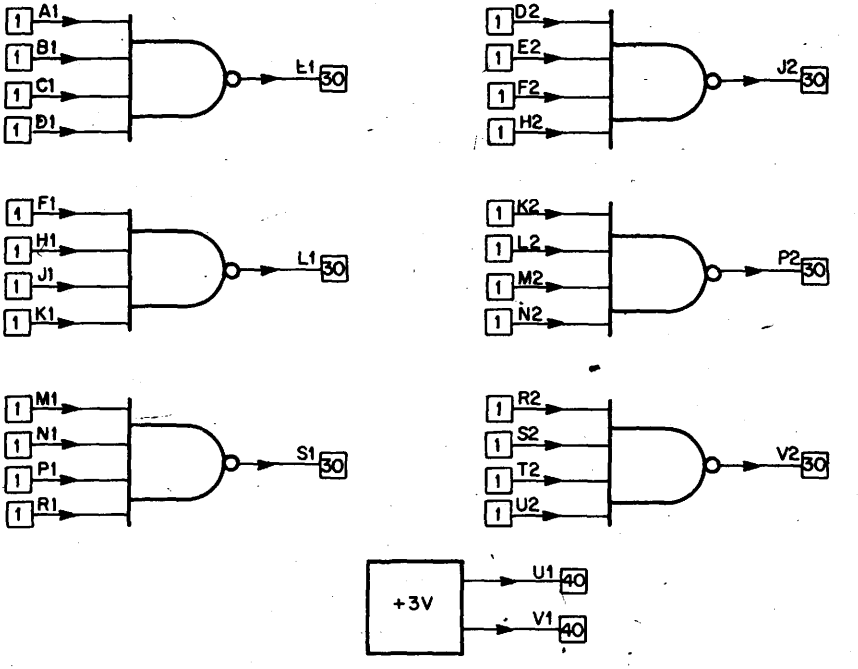
- Output Expansion
- Logical Inversion

M617
FOUR-INPUT POWER NAND GATE

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	97	A2
GND		C2, T1

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads.

FUNCTIONS
Physical configuration and logical operation are identical to the M117.

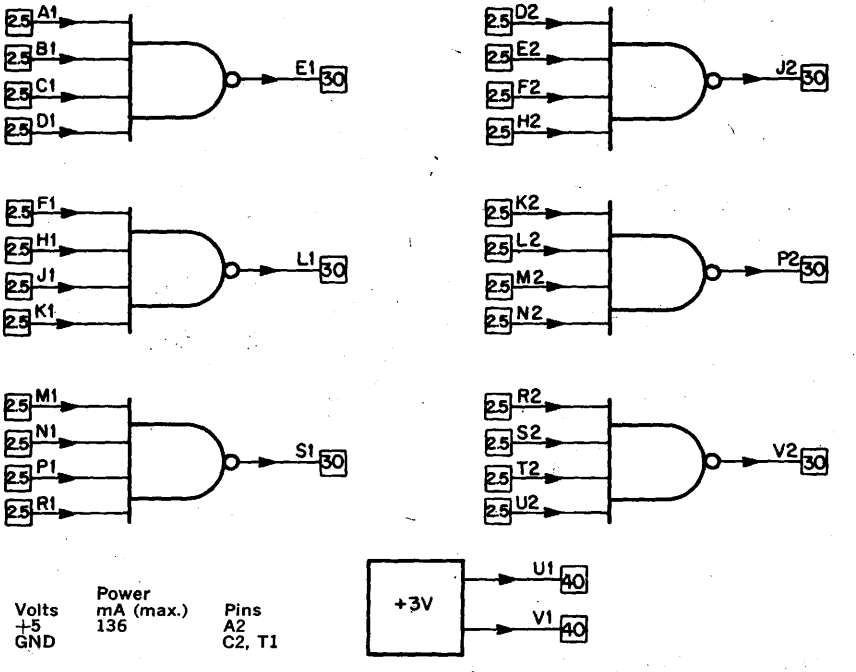
SPECIFICATIONS
Typical gate propagation delay is 15 ns.

M627
NAND POWER AMPLIFIER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	136	A2
GND		C2, T1

The M627 provides six 4-input NAND gates that combine power amplification with high-speed gating.

PRECAUTIONS

1. In pulse amplifier applications, unused inputs should be connected to the +3 volt pins provided.
2. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

SPECIFICATIONS

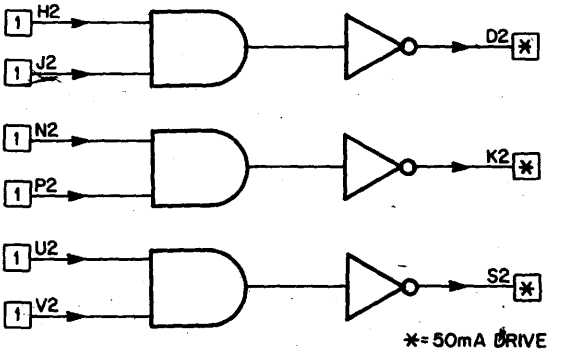
Propagation Time: Typically 6 ns between input and output transitions.

M660
POSITIVE LEVEL CABLE DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	71	A2
GND		C2

The M660 Cable Driver consists of three NAND gate circuits each of which will drive a 100-ohm terminated cable with M Series levels or pulses of duration greater than 100 ns. The output is not open-collector. It is a discrete transistor totem pole configuration similar to an IC gate providing high current drive in both the high and low directions.

SPECIFICATIONS

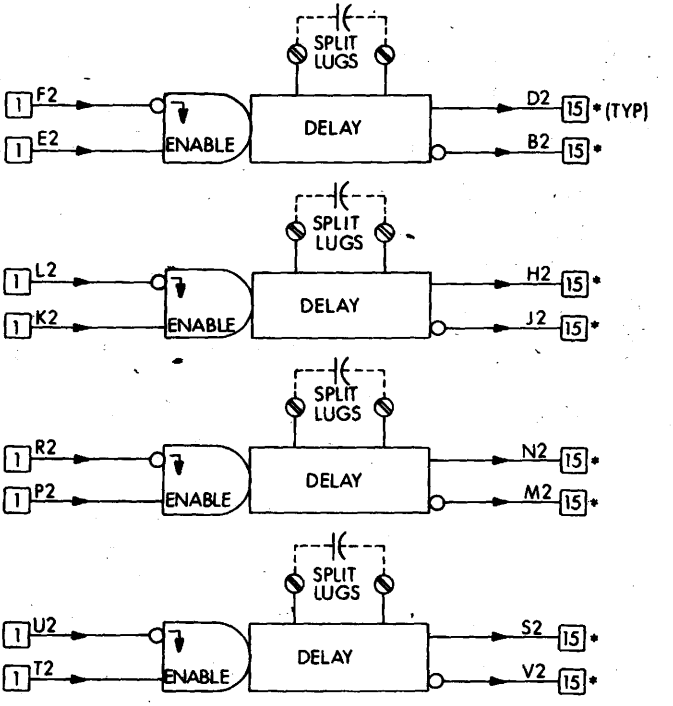
Outputs: Can sink 50 mA at a logic LOW, and can source 50 mA at a logic HIGH.

M671
M TO K CONVERTER
(ONE-SHOT)

MULTI-VIBRATORS

M SERIES

Length: Standard
Height: Single
Width: Single

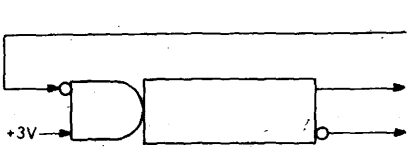


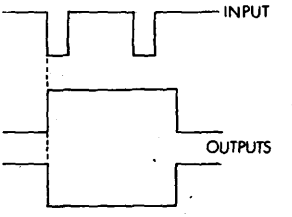
Volts	Power mA (max.)	Pins
+5	112	A2
GND		C2

The M671 M Series to K Series Converter contains four pulse stretching circuits which can convert an M Series input pulse of duration exceeding 50 ns to complementary K Series output pulses of 10 to 15 μs.

FUNCTIONS

Triggering: When the ENABLE input is HIGH, the delay is triggered by the negative-going edge of the trigger input pulse:





This circuit is insensitive to input transitions during its timeout period as shown in the example above.

Increasing Output Pulse Width: Non-electrolytic capacitors can be connected to the split lugs provided in each circuit if K Series output pulse widths longer than 15 μs are desired. Pulses of up to 40 seconds are possible using this technique. When capacitance is added, the output pulse width is increased by 6400 C seconds where C is the capacitance added in farads.

Precautions: Unused inputs should be connected to logic levels that will hold them in their unasserted states. Unused inputs that would be asserted High should be grounded. Unused inputs that would be asserted Low should be connected to a source of logic High. Also refer to "Unused Inputs" in the alphabetical index.

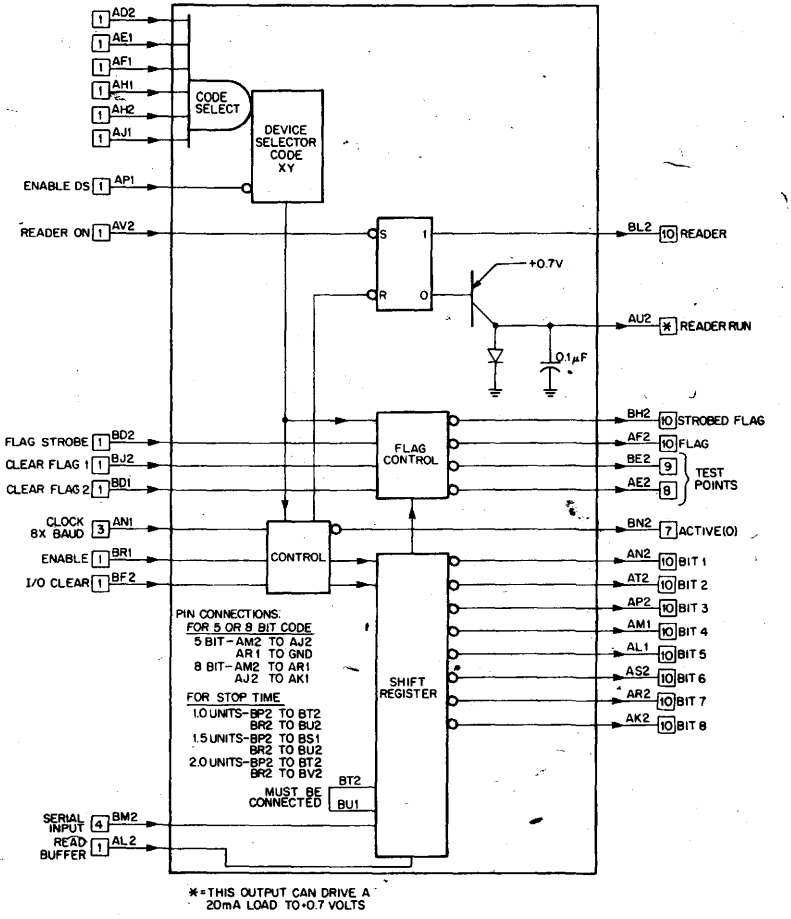
SPECIFICATIONS
Output drive: Each output is capable of driving a 15 mA load.

M706
TELETYPE RECEIVER

COMMUNI-CATIONS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	400	AA2, BA2
GND		AC2, AT1, BC2, BT1

NOTE: Refer to the M7390 module description as a possible substitute for the M706.

The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock)necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device. Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 Volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2. A low output will exist at pin BE2 if the M706 is addressed and the clear Flag 1 (pin BJ2) is high. A low output will exist at pin AE2 if the M706 is addressed and the Clear Flag 1 (pin BJ2) is high or if Clear Flag 2 (pin BD1) is high.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 Volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysterisis thresholds of nominally 1.0 and 1.7 Volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 Volts and undershoot below —0.9 Volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the ouput data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 Volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

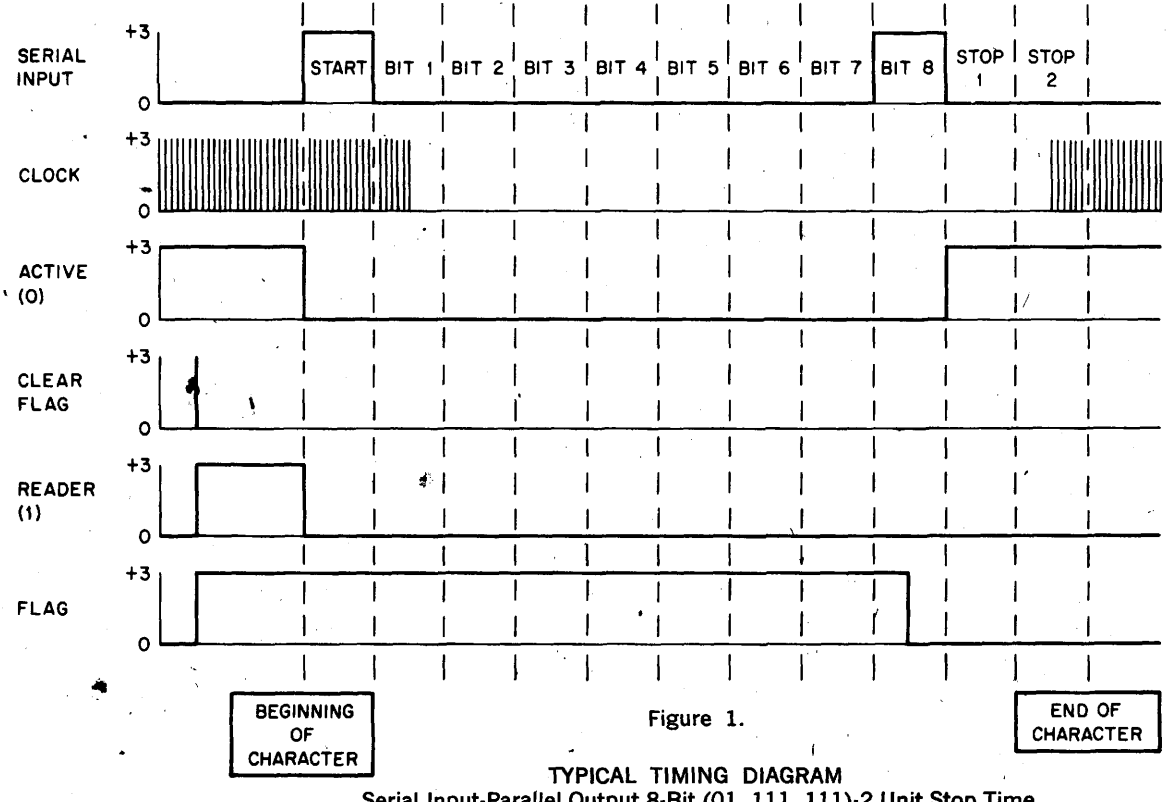


Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 Volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 Volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 Volts load. The common end of the load can be returned to any negative voltage not exceeding —20 Volts.

Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 Volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

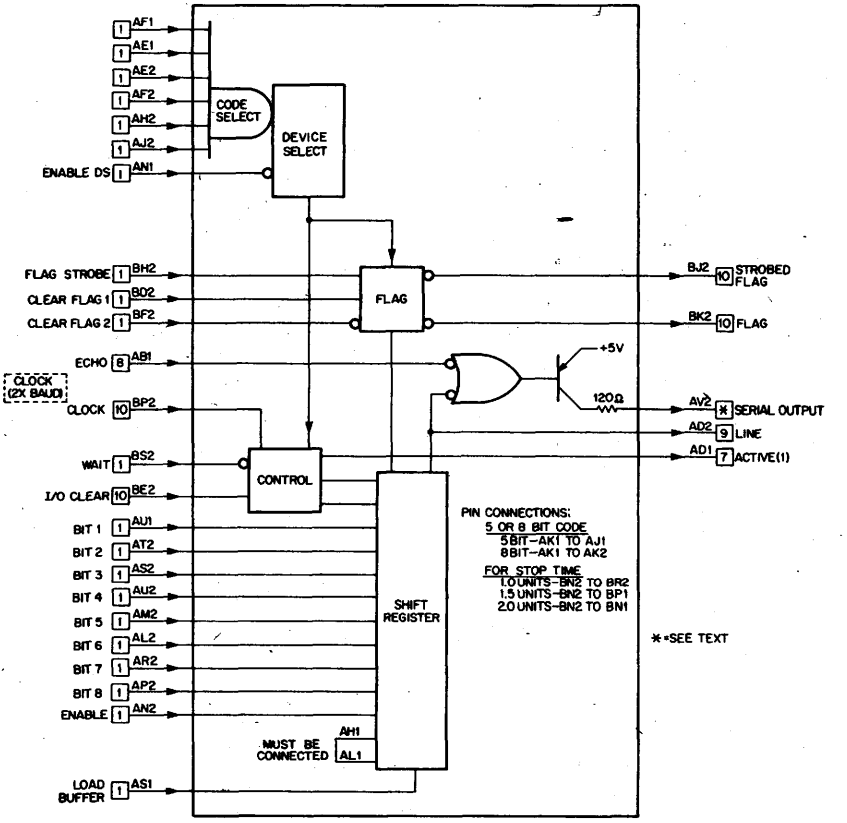
Pin BE2: This output is brought from +3 Volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

M707
TELETYPE TRANSMITTER

COMMUNICATIONS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	375	A2
GND		C2, T1

NOTE: Refer to the M7390 module description as a possible substitute for the M707.

The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary tot ransfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 Volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 Volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 Volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 Volts.

Serial Output: This open collector PNP transistor output can drive 20 mA into any load returned to a voltage between +4 Volts and −15 Volts. A logical output or mark is +5 Volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 Volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

Flag: This output falls from +3 Volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 Volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.
+3 Volts: Pin BJ1 can drive ten TTL unit loads at a +3 Volts level.

Power: +5 Volts at 375 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

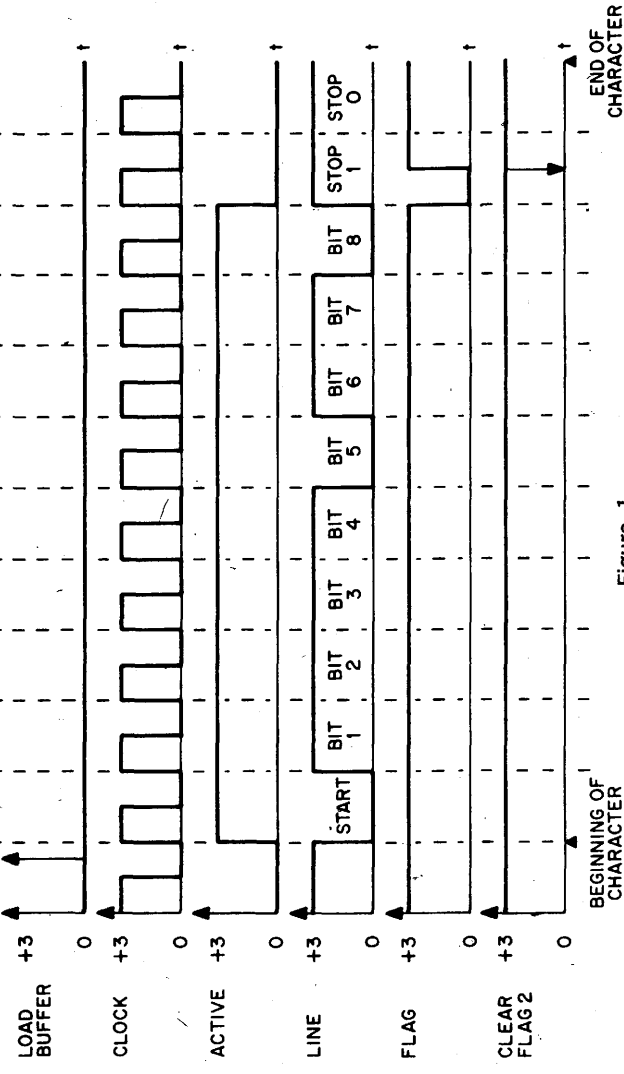


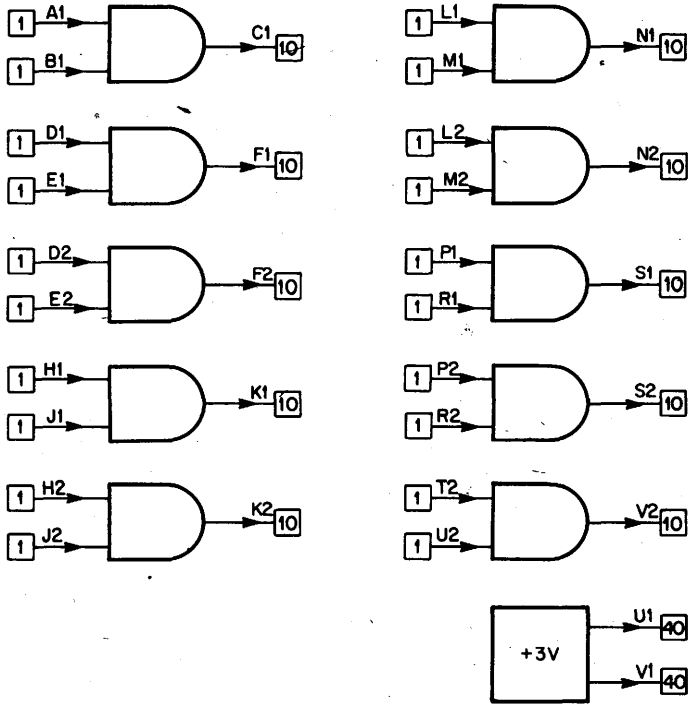
Figure 1.
Typical Timing Diagram, Parallel input, 8-Bit Character (11, 110, 110) With two bit Stop time.

M1103
TWO-INPUT AND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80	A2
GND		C2, T1

The M1103 contains ten 2-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

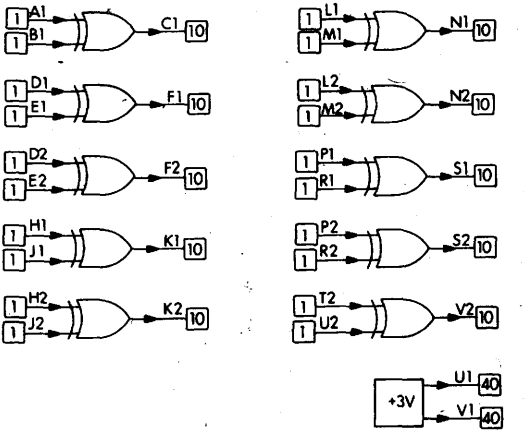
- Positive AND or negative OR gating

M1125
EXCLUSIVE OR GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	100.	A2
GND		C1, T1

The M1125 Module consists of ten 2-input exclusive OR gates and two +3 Vdc voltage divider sources. Each module circuit performs the X-OR function ($A \bullet \overline{B} + \overline{A} \bullet B$) according to the following truth table. Gate output is high when inputs are not the same.

TRUTH TABLE

INPUTS		OUTPUTS
L	L	L
L	H	H
H	L	H
H	H	L

SPECIFICATIONS

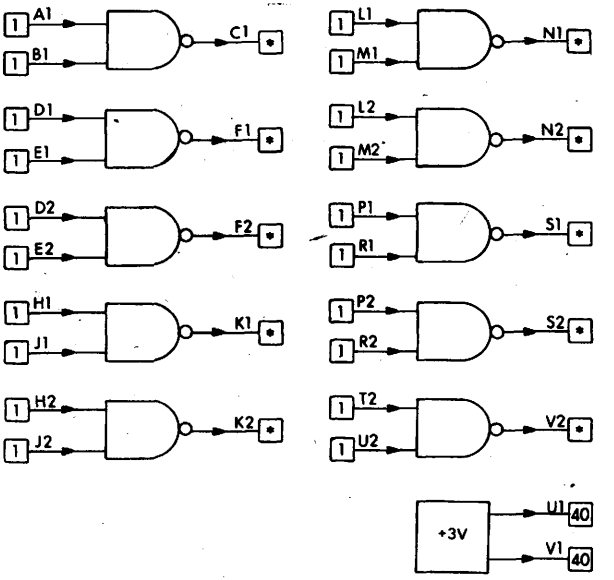
Typical propagation delay time of the M1125 is 12 ns.

M1131
2-INPUT OPEN COLLECTOR NAND GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



* In the logic low state, the output of this module will sink up to 16 mA per driver.

Volts	Power mA (max.)	Pins
+5	71	A2
GND		C2, T1

The M1131 module consists of ten high-speed, 2-input NAND gate circuits and a +3 Vdc source. Each of the NAND gates has an open collector output and the outputs can be paralleled for a wired OR function. Each gate input is a 1 unit load and each unparalleled output will drive up to 10 unit loads.

APPLICATIONS
Logic gating. Wired-OR multiplexing

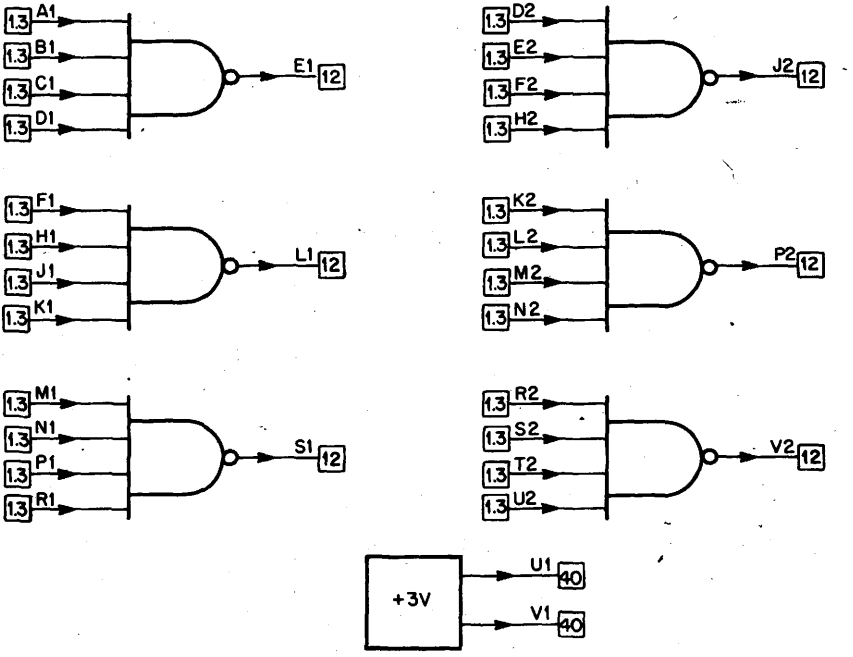
SPECIFICATIONS
Typical gate propagation delay time is 10 ns.

M1307
FOUR-INPUT AND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M1307 contains six high speed 4-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

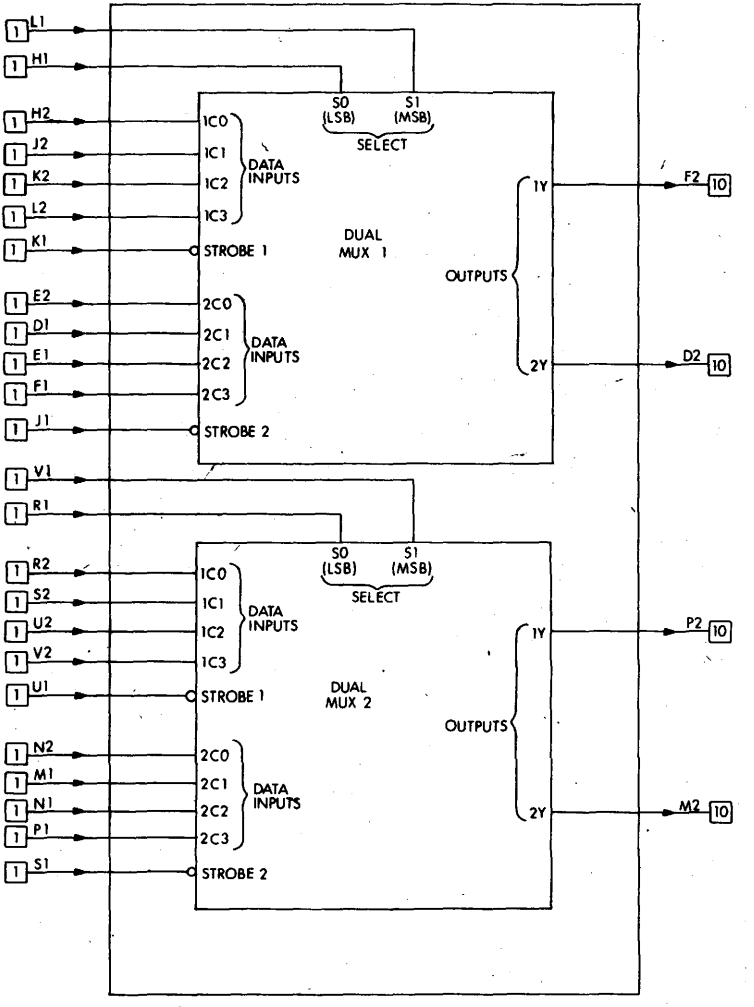
- Positive AND or negative OR gating

M1701
DATA SELECTOR

MULTI-PLEXERS

M SERIES

Length: Standard
Height:
Width: Single



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M1701 Data Selector contains two independent dual 4-line to 2-line multiplexers on a single-height module. Each dual multiplexer has two groups of DATA INPUTS, two STROBES, two OUTPUTS and common SELECT inputs. An OUTPUT becomes active for a DATA INPUT when the DATA INPUT is addressed by the SELECT lines and the corresponding STROBE brought LOW.

APPLICATIONS

- Multiplexing for parallel-to-serial conversion
- Timesharing
- Sampling

TRUTH TABLE

FUNCTIONS

SELECT		DATA INPUTS					
S1	S0	C3	C2	C1	C0	STROBE	OUTPUT Y
X	X	X	X	X	X	H	L
L	L	X	X	X	L	L	L
L	L	X	X	X	H	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
H	H	L	X	X	X	L	L
H	H	H	X	X	X	L	H

X = irrelevant

PROPAGATION DELAY TIMES

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	MAX	UNIT
t_{PLH}	Data	Y	25	ns
t_{PHL}	Data	Y	30	ns
t_{PLH}	Address	Y	40	ns
t_{PHL}	Address	Y	40	ns
t_{PLH}	Strobe	Y	35	ns
t_{PHL}	Strobe	Y	30	ns

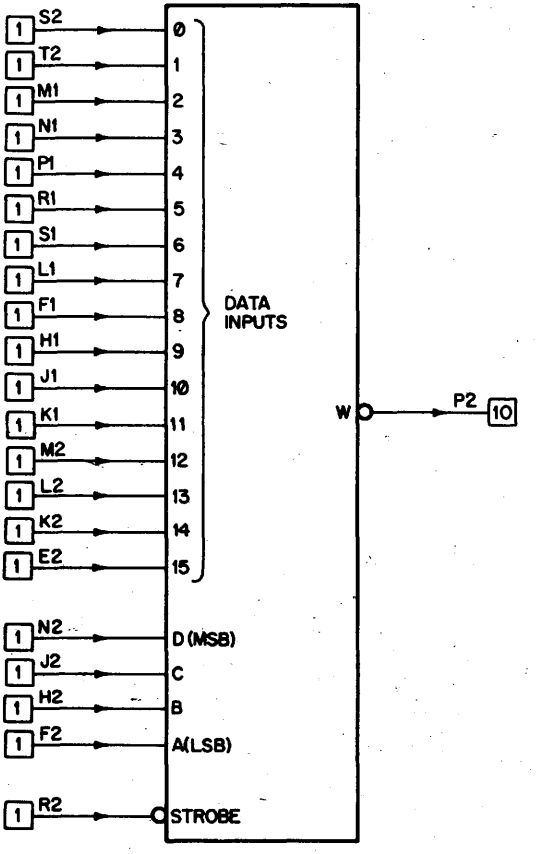
¶t_{PLH} = propagation delay time, Low-to-High-level output.
t_{PHL} = propagation delay time, High-to-Low-level output.

M1713
16-LINE TO 1-LINE DATA SELECTOR

MULTI-PLEXERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M1713 module is a 1-of-16 data selector/multiplexer. The binary code on inputs A-D defines which of the 16 data inputs will be connected to the output when STROBE is Low. Its operation is described by the following **TRUTH TABLE:**

					INPUTS															OUTPUT
D	C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	H
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	H
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	L
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	H
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	L
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	H
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	L
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	H
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	L
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	H
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	L
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	H
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	L
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	H
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	L
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	H
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	L
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	H
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	L
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	H
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	L
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	H
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	L

When used to indicate an input condition, X = High or Low

SPECIFICATIONS

Propagation Delay

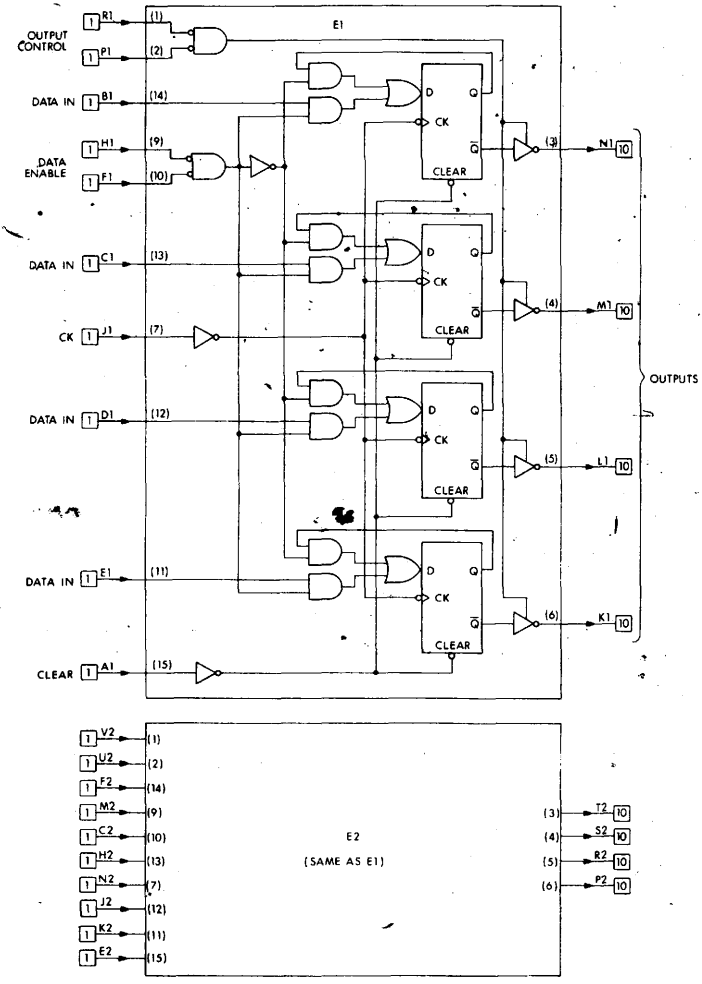
FROM:	TO:
Input A, B, C, D	Output W = 50 ns (max)
STROBE	Output W = 40 ns (max)
D0 through D15	Output W = 30 ns (max)

M2001
DUAL 4-BIT TRI-STATE REGISTERS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	200	A2
GND		C2, T1

The M2001 is a dual, 4-bit register module consisting of D-type flip-flops and input and output gating. Each of the module outputs contains a tri-state circuit capable of driving low-impedance, high-capacitance loads without the use of pull-up or interface components. The third state of the output is a high-impedance state and is selectable by logic levels to the input of the module. This state effectively disconnects the register outputs from the bus when no information transfer is required. Up to 128 of these outputs can be connected together in a wired-OR configuration.

Data is entered into each D-type flip-flop from an associated DATA IN line and is controlled by the DATA ENABLE gate. When both DATA ENABLE inputs are Low, the information on the data lines will be entered into the respective flip-flop on the next positive transition of the clock (CK) input.

The Q output from each flip-flop is inverted and controlled by the tri-state driver amplifier. Where either or both input to the output control gate is a High logic level, the outputs of the module are disabled to the high-impedance state; however, the sequential operation of the flip-flops are not affected.

When the CLEAR input to the logic element is High, each associated flip-flop is held in the reset condition, and the module outputs will remain in the Low state.

FUNCTION TABLE

DATA IN	CLOCK	CLEAR	DATA ENABLE 1	DATA ENABLE 2	OUTPUT
L	L to H	L	L	L	L
H	L to H	L	L	L	H
X	X	H	X	X	L
X	L	L	X	X	Qo
X	L to H	L	H	X	Qo
X	L to H	L	X	H	Qo

L = Low level (steady)
H = High level (steady)
L to H = Low to high level transition
X = Irrelevant of any input including transition
Qo = Level of module output before steady state input conditions were established.

APPLICATIONS
Provides a total of eight bits of data storage and outputs to interface directly to system bus. All input and output signals are through edge board connector.

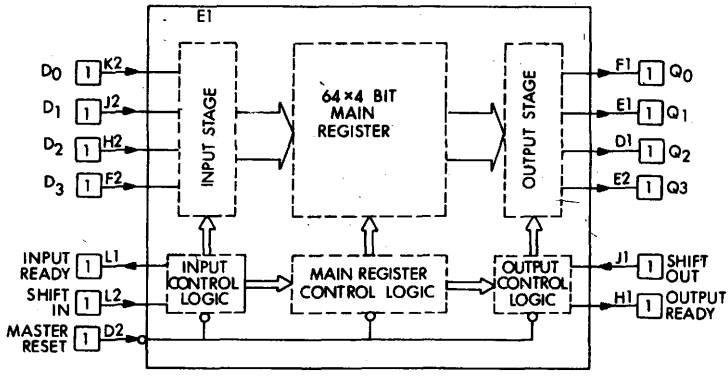
FUNCTION
Refer to Function Table for input and output signal and level requirements.

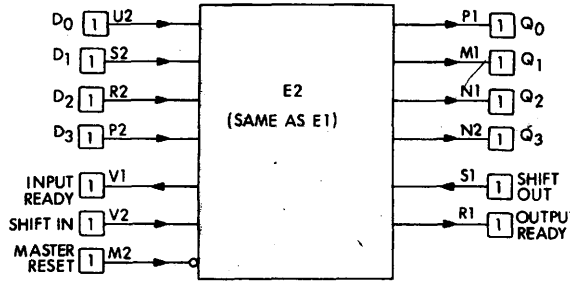
SPECIFICATIONS
Input Voltage — 4.5 Vdc (min.), 5.2 Vdc (max.)
Input Current — 72.0 mA (max.)
High Level Output Current — 5.2 mA (max.)
Low Level Output Current — 16 mA (max.)

M2500
DUAL 64 WORD X 4 BIT FIRST-IN FIRST-OUT SERIAL MEMORY

SHIFT/ STORAGE REGISTERS
M SERIES

Length: Standard
Height: Single
Width: Single





Volts	Power mA (max.)	Pins
+5	100	A2
−12	23	K1, U1
GND		C2, T1

The M2500 Module provides storage for 64 4-bit words in each of two memory elements. The words are stored and read asynchronously on a first-word-in, first-word-out basis. By series coupling the two memory elements, the total storage capacity can be increased to 128 4-bit words. The two memory elements can also be paralleled, using external logic, to form storage for 64 8-bit words.

FUNCTION

The first 4-bit word is entered into the memory register by initiating a High SHIFT IN pulse when the INPUT READY signal from the memory is High. With no data word previously stored in the first location of memory, the INPUT READY signal will be High. As the word enters the first memory location, the INPUT READY signal becomes Low and remains Low until the SHIFT IN pulse is brought Low. The Low transition of the SHIFT IN pulse transfers the first 4-bit word into the second memory location, and the INPUT READY signal again becomes High. The internal control logic then sequences the word to the first-out or 64th memory location which causes the OUTPUT READY signal to become High. This indicates that the first word entered is available to be read at the output. The second 4-bit word can then be entered into memory and is automatically stacked at the output. To read a word from memory and shift the next word to the output, a High SHIFT OUT pulse is required and causes the previously High OUTPUT READY signal to become Low. The data is shifted out by the trailing edge of the SHIFT OUT pulse when the OUTPUT READY signal is Low. The next 4-bit word is then automatically shifted to the 64th location causing the OUTPUT READY signal to again become High. When all locations are empty, OUTPUT READY will remain Low. When all the memory locations are full, the INPUT READY signal is held Low until a word is read, resulting in a vacant location.

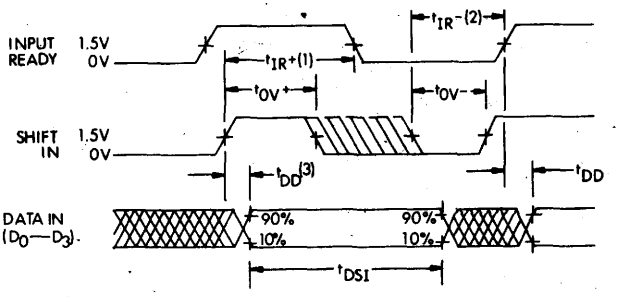
APPLICATIONS

The M2500 can be used as a synchronous or asynchronous serial storage device or as a buffer unit for data communication between devices operating at different data rates. The M2500 can be serial connected to increase the total number of 4-bit memory locations or connected in parallel to extend the word lengths. Both data and control inputs and outputs are direct TTL and DTL compatible.

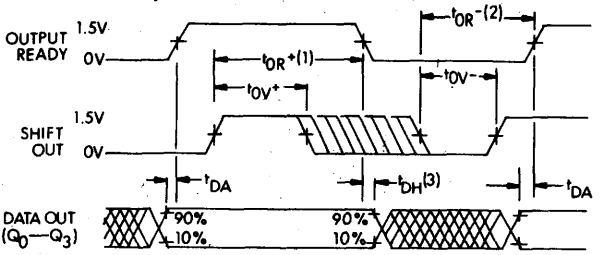
FUNCTION

The following input/output diagrams indicate the timing relationships and logic levels required to write into or read data from memory.

INPUT TIMING



OUTPUT TIMING



t_{IR}^+ (Input Ready HIGH Time)	300 ns (typ.)
t_{IR}^- (Input Ready LOW Time)	300 ns (typ.)
t_{OV}^+ (Control Overlap HIGH Time)	100 ns (min.)
t_{DSI} (Data Input Stable Time)	400 ns (min.)
t_{DD} (Data Input Delay Time)	25 ns (min.)
t_{OR}^+ (Output Ready HIGH Time)	300 ns (typ.)
t_{OR}^- (Output Ready LOW Time)	450 ns (typ.)
t_{DH}^- (Data Hold Time)	75 ns (min.)

NOTES:

t_{IR}^+ is referenced to the positive going edge of IR or SI, whichever occurs later.

t_{IR}^- is referenced to the negative going edge of IR or SI, whichever occurs later.

t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.

t_{OV}^+ is referenced to the positive going edge of IR or SI, whichever occurs later. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.

Data must be stable for t_{SDI} or t_{IR}^+, whichever is shorter.

Input data must remain stable during timing window t_{SDI}. Both SI and IR must be HIGH for t_{OV}^+.

t_{OR}^+ is referenced to the positive going edge of OR or SO, whichever occurs later.

t_{OR}^- is referenced to the negative going edge of OR or SO, whichever occurs later.

t_{DH} is referenced to the negative going edge of OR or SO, whichever occurs later.

t_{OV}^+ is referenced to the positive going edge of IR or SI, whichever occurs later.

Both SO and OR must be HIGH for t_{OV}^+.

Inputs

SHIFT IN	A High on this input causes INPUT READY to go Low and data to the shifted into the memory. Data will begin to shift to the last empty location when this input is brought Low again. Minimum pulse width is 100 ns. Data must be valid within 25 ns after SHIFT IN goes High. SHIFT IN must only be brought High when INPUT READY is High. Minimum Low time for SHIFT IN is 100 ns.
D0—D3	Data inputs. Data must be valid within 25 ns after SHIFT IN goes High and should remain valid for at least 400 ns.
SHIFT OUT	A High on this input initiates the output shifting process. Data will remain valid until 70 ns after both SHIFT OUT and OUTPUT READY have gone Low. Minimum pulse width is 100 ns. SHIFT OUT must remain Low for at least 100 ns.
MASTER RESET	Resets memory control logic.

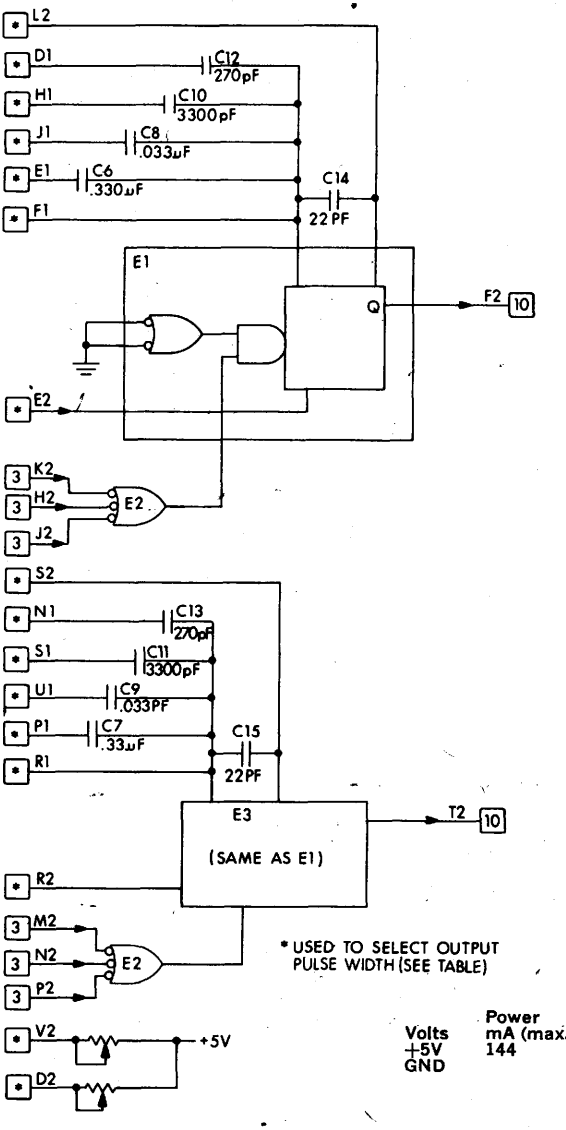
Outputs

INPUT READY	Indicates when data may be loaded into the memory. Goes Low 300 ns (typ) after the leading edge of SHIFT IN and goes High again when the next data word may be loaded. INPUT READY remains Low when the memory is full.
OUTPUT READY	Indicates when data is valid at the output of the memory. OUTPUT READY goes Low 300 ns (typ) after the leading edge of SHIFT OUT and goes High again when the next word has been shifted to the output. OUTPUT READY remains Low when the memory is empty.
Q0—Q3	Data outputs. Data is valid at the outputs whenever OUTPUT READY is High, even if SHIFT OUT is Low. Data will change 75 ns after OUTPUT READY goes Low. Typical propagation time from input to output of an empty memory is 10 μs.

M3020
DUAL DELAY MULTIVIBRATORS

MULTI-VIBRATORS

M SERIES



Volts	Power mA (max.)	Pins
+5V	144	A2
GND		C2, T1

The M3020 Module contains two monostable multivibrators, each of which is activated by the output of a Schmitt Trigger circuit. A low input transition on any one of the three inputs to the Schmitt Trigger circuit produces a positive output pulse and triggers the multivibrator. Minimum duration of a low pulse is 50 ns. The Schmitt Trigger input provides hysteresis which prevents the multivibrator from being triggered erroneously by noise signals at the input.

When activated, the multivibrator produces a positive pulse at the output. The width of the pulse is variable from 50 ns to 40 sec and is selected by the external connections to capacitors mounted on the M3020 and by the variable Vcc available.

The delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor.

APPLICATIONS

- Time delays
- Variable width pulses

FUNCTIONS

Delay Range: The basic DELAY RANGE is determined by an internal 22 pF capacitor. The delay range may be increased by selection of additional capacitance either by connecting various module pins (See Table) or by the addition of external capacitance between pins L2 and F1 or between pins S2 and R1. Potentiometers mounted on the module can be connected for fine delay adjustments within each range or an external resistance may be used between pins E2 or R2 and +5 Volts. If an external resistor is used, the resistance should be limited to 40,000 ohms.

Delay Range	Capacitor Value (Internal)	Interconnections Required	
		Delay E1	Delay E3
50 ns — 750 ns	22 pF	None	None
500 ns — 7.5 μs	270 pF	D1 — L2	N1 — S2
5 μs — 75 μs	3300 pF	H1 — L2	S1 — S2
50 μs — 750 μs	.033 μF	J1 — L2	U1 — S2
500 μs — 7.5 ms	.33 μF	E1 — L2	P1 — S2

Adjustable Delays: Connect pins D2 to E2 for delay 1 and V2 to R2 for delay 2 in order to add the potentiometers. NOTE: If the potentiometer or an external resistor is not used pins E2 and R2 must be connected to +5 volts (pin A2).

PRECAUTIONS

Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

SPECIFICATIONS

Trigger Input Fall Time: Must be less than 400 ns

Recovery Time: Defined as the time all inputs must remain HIGH before any input goes LOW to trigger the delay

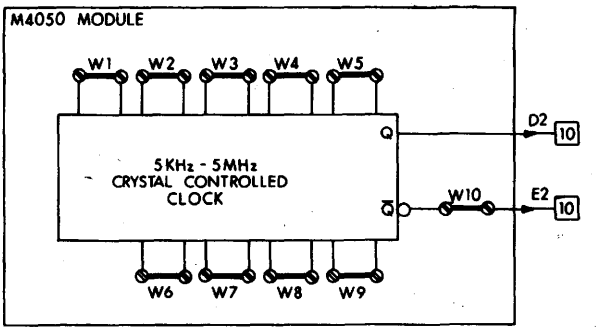
1. Without external capacitance: 30 ns min.
2. With external capacitance: 300 C ns min. where C is in nanofarads

M4050
Crystal Controlled Clock

CLOCK

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA	Pins
+5V	80	A2
GND		C2

DESCRIPTION

The M4050 is a crystal controlled clock module that provides both positive- or negative-going 80 ns pulses at a frequency range from 5 KHz to 5 MHz. (An M4050-YA module variation is also available and provides an output pulse width of 3.9 μs.) The module has a series of jumper leads mounted between split lugs on the board which can be removed to select four frequency ranges. Once the proper range has been selected, the output olock frequency is determined by a plug-in crystal. The module can be effectively used in applications requiring accurate pulses at stable frequencies.

FUNCTIONS

The D2 and E2 outputs of the M4050 are supplied from a monostable multibibrator. The pulses at D2 and E2 are positive and negative 80 ns pulses, respectively.

Frequency Range Selection

Jumpers W1 through W9, shown on Figure 1, are used to determine the frequency range of the output. The specific frequency is then determined by choice of a plug-in crystal, either one of the three offered by DIGITAL or one supplied by the user. Table 1 lists the jumper configuration for the four frequency ranges.

TABLE 1

Frequency Range	JUMPERS	
	IN	OUT
5 KHz – 38 KHz	W1 – W8	W9
38 KHz – 500 KHz	W1 – W6	W7 and W8
500 KHz – 1 MHz	W3 – W6	W1, W2, W7, W8
1 MHz – 5 MHz	W5, W6	W1 – W4, W7, W8

Output Selection
Jumper W10, shown on Figure 1, can be removed to disconnect the negative-going pulse output from the multivibrator to pin E2 of the module.

Ordering Information
The M4050 is available with any of the three standard crystals listed below. Be sure to list the crystal part number desired when ordering. Standard crystals:

1.333 MHz Part # 18-5501-02
2.0 MHz Part # 18-5501-09
5.0 MHz Part # 18-5501-08

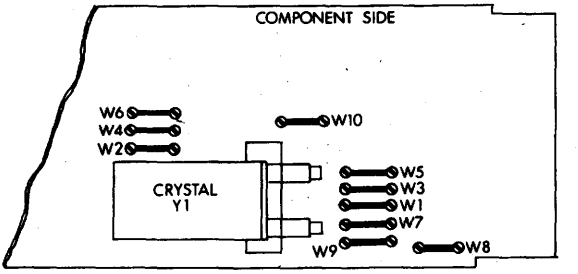


Figure 1 M4050 Jumper Lead Locations

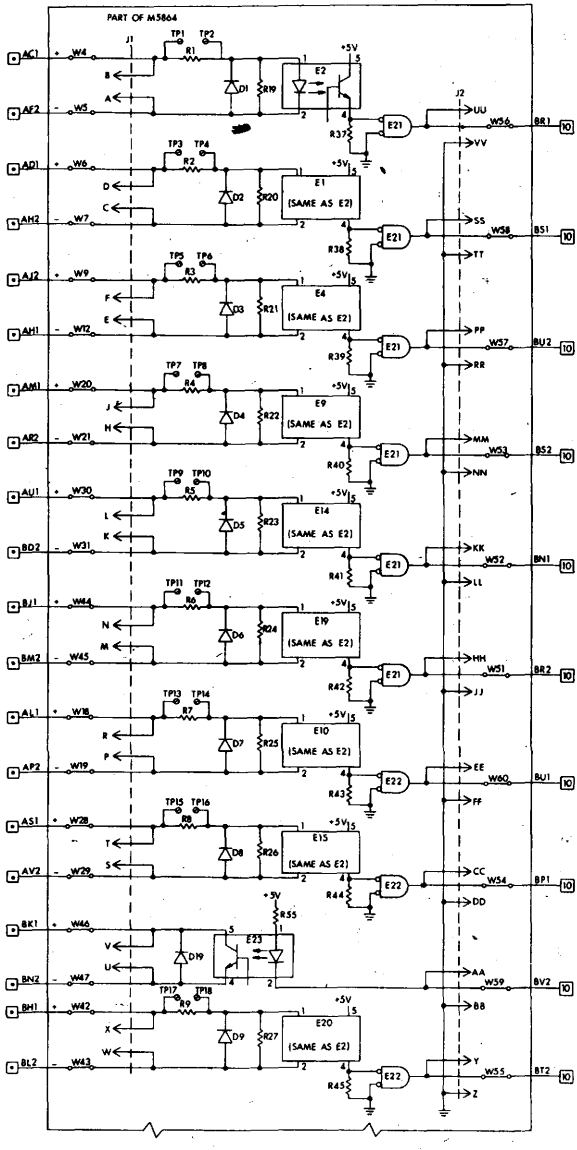
GENERAL SPECIFICATIONS

Frequency:
Range: 5 KHz – 5 MHz
Stability: 0.01% of specified value between 0°C and +55°C.
Power Requirements: +5V at 80 mA (max.)
Temperature Range: 0°C to +55°C

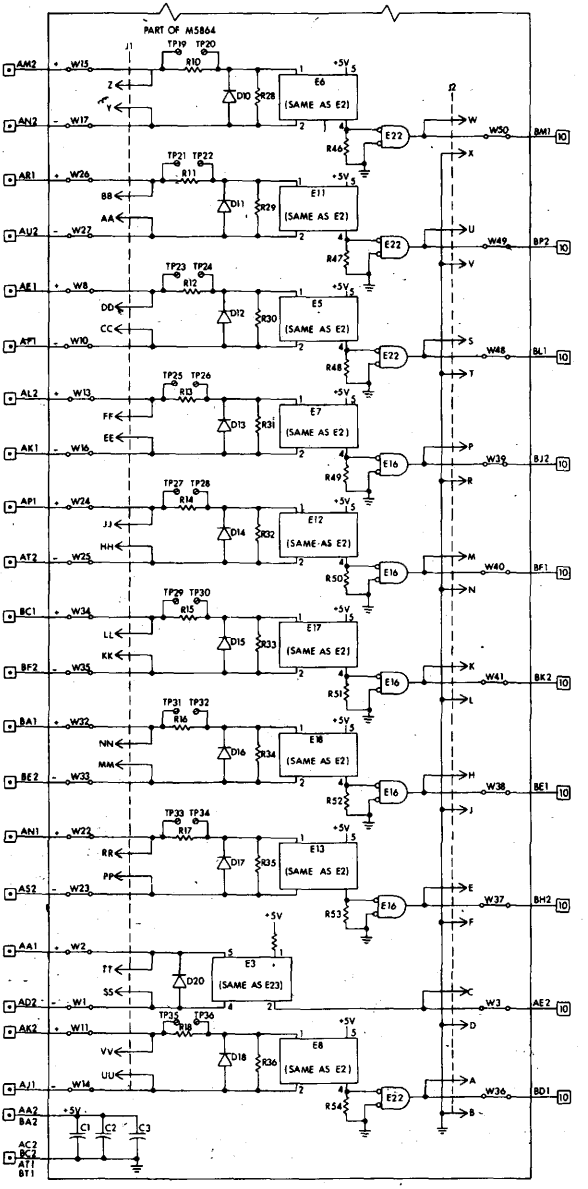
M5864
OPTIC ISOLATOR INPUT MODULE

ISOLATION/ LEVEL CONVERSION

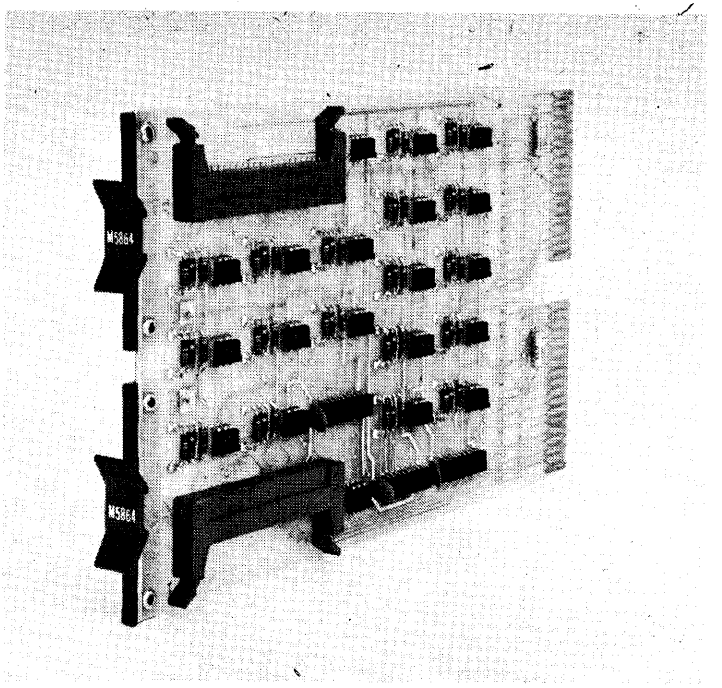
M SERIES



M5864 Optic Isolator Input Module



M5864 Optic Isolator Input Module (cont.)



The M5864 Optic Isolator Input Module is used to electrically isolate and/or convert signal levels between peripheral devices and a TTL-compatible interface of a processor or controller system. The M5864 can effectively be used in any application where signal conversion or voltage isolation is required.

The module contains 20 optically-coupled circuits, each of which provides signal isolation between the input and output of the module. The data signals transferred through each of the module circuits are optically-coupled to provide a maximum of 1500 V isolation between the current loop and the TTL logic. Eighteen input circuits accept levels from current-producing devices and convert these signals to TTL-compatible levels. The current-receiving inputs are protected against reverse voltage conditions by a diode shunted across the LED in each optic coupler. The conduction of the LED controls the conduction of the associated phototransistor also in the optic coupler. Two output circuits accept TTL-compatible levels from the interface and control the conduction of the floating transistor outputs. Each transistor output is capable of switching 8 mA of current.

Signals are transferred to and from the module through the module pins and backplane wiring or through cable assemblies that attach to the two 40-pin connectors located near the edge of the module. The module input and output circuits can be disconnected from the backplane of a system by removing jumper leads that are installed on the module board. This allows the module to be plugged into computer busses and other prewired backplanes for convenient mounting. Power and ground to the module will still be maintained through the module pins and backplane wiring.

Each signal pin on the 40-pin cable connector (J2) has an associated ground pin to enable proper shielding of the TTL levels.

The M5864 is a double-height, standard-length module and occupies two slots when inserted into a standard DIGITAL connector block.

FEATURES

- Complete electrical isolation between inputs and outputs.
- Signal transfer to and from module through module pins and backplane wiring or through cable and connectors.
- Floating transistor outputs, reverse voltage protected.
- Capable of isolating 16 data and 4 control lines.
- Device input voltages adjustable by adding resistors on board.
- Standard DIGITAL power and ground pin configuration.

GENERAL SPECIFICATIONS

The input to each of the optically isolated input circuits is the opto-isolator LED. A forward current of over 8 mA (30 mA max) will turn the LED on. The output of each input circuit is a standard TTL gate with a fanout of 10.

The input to each of the optically isolated output circuis is the opto-isolator LED which is pulled up on the module to +5 volts through a resistor. This input is TTL compatible and represents 10 unit loads. The output of each output circuit will drive one TTL load.

18—Input Circuits

Input (J1)	TTL Output (J2)
0—2 mA	HIGH (-400 mA at 2.4 V)
8—30 mA	LOW (16 mA at .4 V)

2—Output Circuits

Input (J2) (TTL Compatible)	Output (J1)
HIGH (100 μA at 4-7 V)	50 nA (max) at 10 V*
LOW (-16 mA at 0.4 V)	1.6 mA (min) at 0.5 V

* Maximum collector-emitter voltage = 30 V

Optic Isolators

Condition	Time	Diode Current
turn-on	15 μs (max)	16 mA
turn-off	15 μs (max)	0 mA

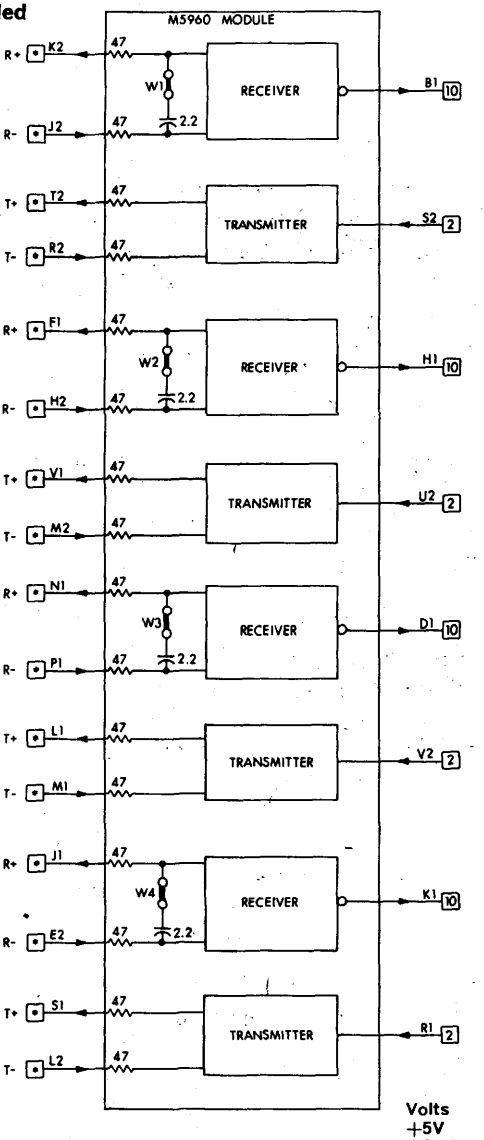
Size	Double height—5.187 in. (13.17 cm) Single width—0.5 (1.27 cm) Extended length—8.5 in. (21.59 cm)
Power	+5 V ±5% at 340 mA (max)
Operating Temperature	5°C (41°F) to 50°C (122°F)
Relative Humidity	10% to 95%, without condensation

M5960
20 mA Active Current Loop Interface

COMMUNICATIONS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	320	A2
−15V	200	B2
GND		C2

DESCRIPTION

The M5960 is a communications interface module used to convert 20 mA current loop information into TTL logic levels (receiver) and TTL logic levels into 20 mA current loop information (transmitter). The module is suitable for driving and sensing data on long current loop cables between the terminal and module at high baud rates. The M5960 consists of four differential current loop receiver circuits and four differential transmitter circuits, each capable of converting the serial data between terminal and logic system and allowing full duplex operation. The M5960 occupies a single vertical slot in an H803 connector block.

APPLICATION

Figure 1 is a typical application diagram showing four passive devices connected to the 20 mA current loops. Both the receiver and transmitter circuits can supply 20 mA of current to a total line/load resistance of up to 500 ohms.

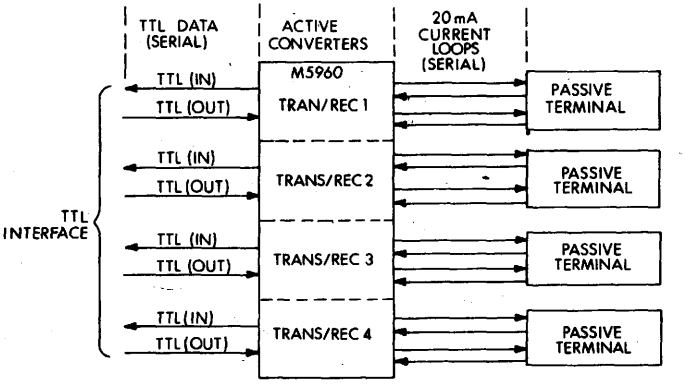


Figure 1 Typical M5960 Application Diagram

RECEIVERS

Each of the four receiver circuits consists of a differential current source circuit which senses the current flow in a passive terminal such as a teletypewriter keyboard or the collector of an optical isolator network. Jumpers W1—W4 shown on Figure 2 connect a capacitor across the 20 mA input circuit to provide high noise immunity at standard TTY data transmission rates of 110 baud. When used in applications requiring rates greater than 110 baud, the appropriate jumpers can be removed.

When current flow above approximately 10 mA is sensed at the 20 mA receiver circuit (R+ and R—), a low TTL output is produced. Current flow below approximately 10 mA results in a high TTL logic level at the output. Each receiver output is capable of driving 10 TTL unit loads.

TRANSMITTERS

Each of the four transmitter circuits provides a 20 mA current source used to drive a teletypewriter printer or similar passive device. The transmitter circuits receive TTL-compatible levels at the input to control the 20 mA current at the output (+T and —T). A low TTL level produces a 20 mA current flow at the output terminals to activate a relay or Light Emitting Diode (LED)

in an optical isolator network. A high TTL level at the input inhibits the 20 mA current from flowing at the output, and disables a relay or LED connected to the current loop circuit.

GENERAL SPECIFICATIONS

Receivers:

Input Current	**Output TTL**
15 mA (and over)	Low Level
5 mA (and under)	High Level
Transmission Rate:	9600 baud (max)
TTL Drive:	10 unit loads

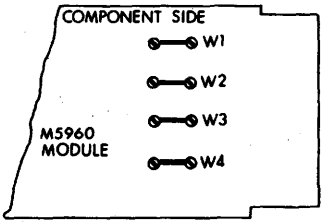


Figure 2 M5960 Jumper Lead Locations

Transmitters:

Input TTL	**Output Current**
Low Level	20 mA (max)
High Level	0 mA (approx.)
Transmission Rate:	9600 baud (max)
TTL Sink:	2 unit loads

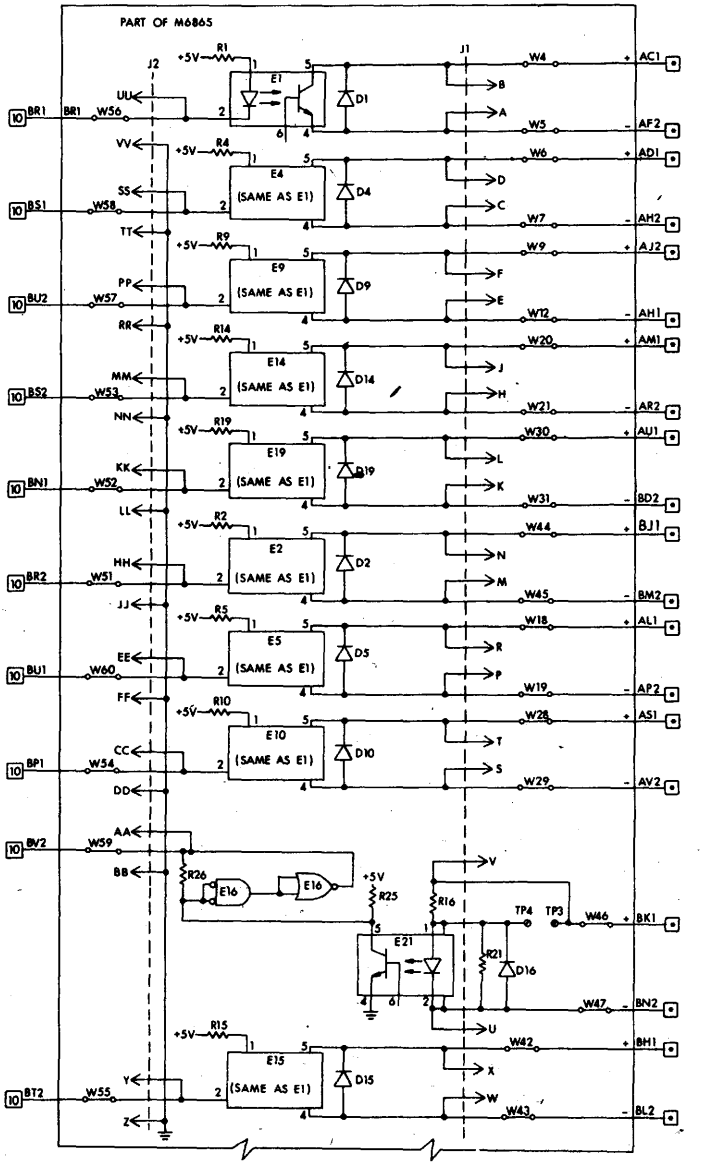
Power Requirements:

+5 Vdc	320 mA (max)
−15 Vdc	200 mA (max)
Operating Temperature:	5°C to 60°C, non-condensing

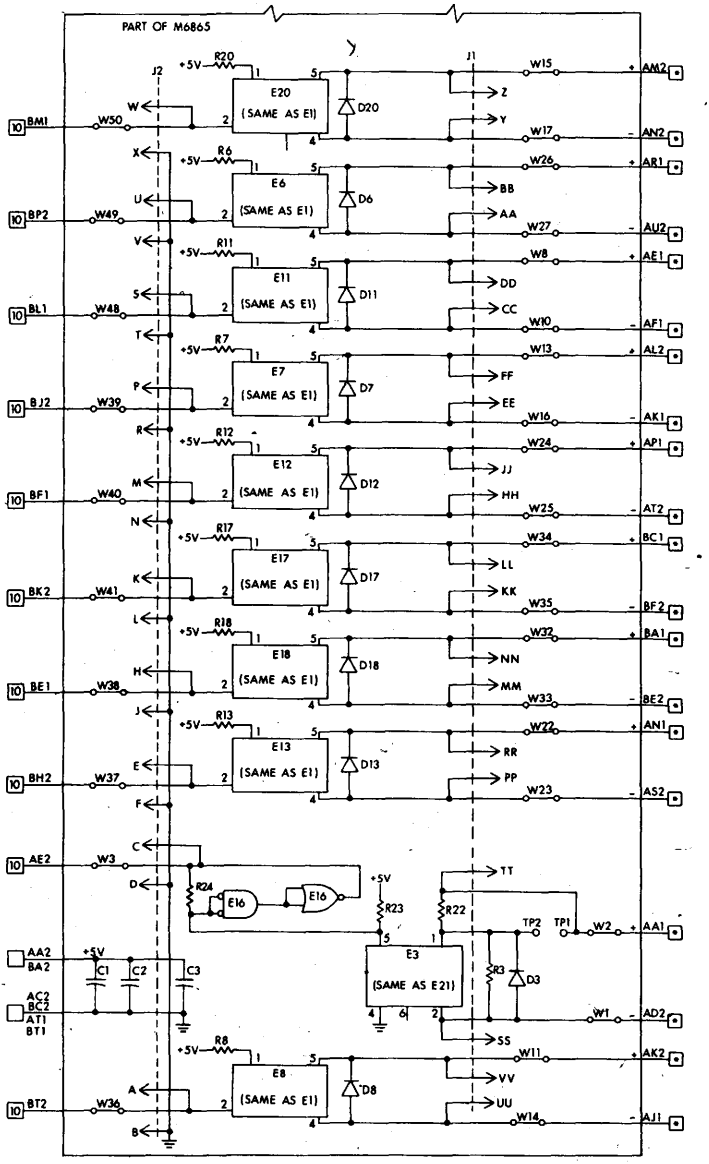
M6865
OPTIC ISOLATOR OUTPUT MODULE

ISOLATION/ LEVEL CONVERSION

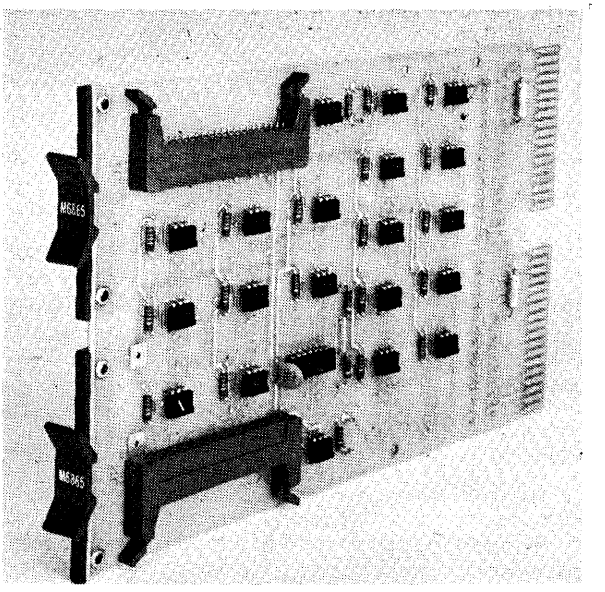
M SERIES



M6865 Optic Isolator Output Module



M6865 Optic Isolator Output Module (cont.)



INTRODUCTION

The M6865 Optic Isolator Output Module is used to electrically isolate and/or convert the signal levels between peripheral devices and a TTL-compatible interface of a processor or controller system. The M6865 can effectively be used in any application where conversion or isolation is required.

The module contains 20 optically-coupled circuits, each of which provides ac or dc signal isolation between the inputs and outputs of the module. The data signals transferred through each of the module circuits are optically-coupled to provide a maximum of 1500 V isolation between the current loop and the TTL logic. Eighteen output circuits accept TTL-compatible levels from the interface to control the conduction of the 18 floating transistors in the optic couplers. Each of the transistor outputs is capable of switching 1.6 mA of current. Two input circuits receive controlling signals from current-producing devices and convert these signals to TTL-compatible levels. Each of the two input circuits is protected against reverse voltage conditions by diodes which are shunted across the input terminals.

Signals are transferred to or from the module through the module pins and backplane wiring or through cable assembies that attach to two 40-pin connectors conveniently mounted near the edge of the module board. This allows the module to be inserted into computer busses and other prewired backplanes for convenient mounting. The module input and output circuits can be easily disconnected from the backplane of a system unit by removing the jumper leads that are installed on the module board.

Each signal pin on the 40-pin cable connector (J1) has an associated ground pin to enable proper shielding of the TTL levels.

The M6865 is a double-height, extended-length module and occupies two slots when inserted into a standard DIGITAL connector block.

FEATURES

- Complete electrical isolation between inputs and outputs.
- Signal transfer to and from module through module pins and backplane wiring or through cable and connectors.
- Floating transistor outputs, reverse voltage protected.
- Capable of isolating 16 data and 4 control lines.
- Device input voltages adjustable by adding resistors on board.
- Standard DIGITAL power and ground pin configuration.

GENERAL SPECIFICATIONS

The input of each of the two optically isolated input circuits is to a LED. A forward current of 8 mA (30 mA max) will activate the LED and cause the transistor to conduct. The output of each input circuit is a TTL level with a fanout capability of 10 unit loads.

The input of each of the 18 optically isolated output circuits is to a LED which is pulled up to +5 V through a resistor. These inputs are TTL compatable and represent 10 unit loads. Each output is capable of driving one unit load.

2—Input Circuits

Input (J1)	TTL Output
0—2 mA	HIGH (-400 μA at 2.4 V)
8—30 mA	LOW (16 mA at .4 V)

18—Output Circuits

TTL Input (J2)	Output (J1)
HIGH (100 μA at 4-7 V)	50 nA (max) at 10 V*
LOW (-16 mA at 0.4 V)	1.6 mA (min) at 0.5 V

*Maximum collector-emitter voltage=30 V

Optic Isolators

Condition	Time	Diode Current
turn-on	15 μs (max)	16 mA
turn-off	15 μs (max)	0 mA

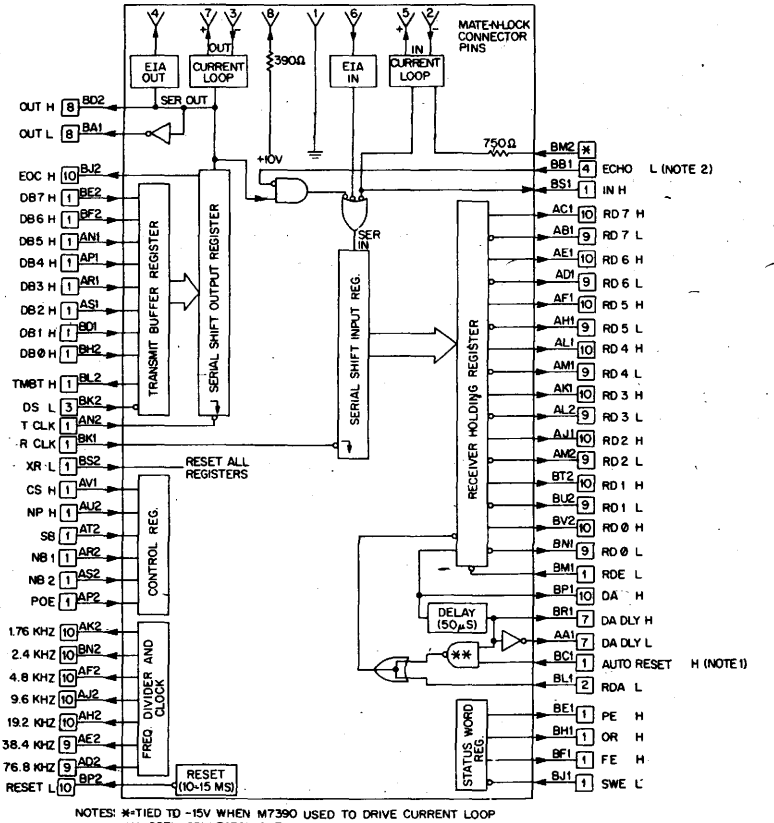
Size	Double height—5.187 in. (13.17 cm) Single width—0.5 in. (1.27 cm) Extended length—8.5 in. (21.59 cm)
Power	+5 V ±5% at 340 mA (max)
Operating Temperature	5°C (41°F) to 50°C (122°F)
Relative Humidity	10% to 95%, without condensation

M7390
ASYNCHRONOUS TRANSCEIVER

COMMUNI-CATIONS

M SERIES

Length: Extended
Height: Double
Width: Single



NOTES: *=TIED TO -15V WHEN M7390 USED TO DRIVE CURRENT LOOP
**=OPEN COLLECTOR OUTPUT
1. MUST BE TIED TO GROUND IF RDA L NOT USED
2. MAY BE LEFT OPEN IF ECHO NOT DESIRED

Volts	Power mA (max.)	Pins
+5	700	BA2
+10	3	AV2
GND		BC2
−12*	64	BR2
−15*	80	BB2

*Requires −12 V or −15 V only, not both.

DESCRIPTION

The M7390 asynchronous transceiver is a modular subsystem which provides asynchronous serial line compatibility for data communications applications. The M7390 combines input/output level converters, parallel-to-serial and serial-to-parallel conversion, and a crystal controlled clock, into one module.

APPLICATIONS

The M7390 can be used for computer terminal applications, data entry devices or any system which requires asynchronous serial line compatibility. The M7390 may also be used to drive modems conforming to EIA RS-232C specifications or current-operated devices such as Teletypes.

FUNCTIONS

There are three groups of functions on the M7390—error detection, data, and control.

Error Detection: The error function of the module allows three types of errors to be detected. These are:

1. Parity: If the received parity bit does not agree with the expected parity bit, the parity error flag is set.
2. Overrun: The receiver section of the M7390 is fully double buffered. Therefore, one full character time is allowed to remove the received data from the receiver buffer before a new character is assembled and transferred. If the character is not removed before a new one is loaded, the overrun flag is set.
3. Framing: Since the M7390 is asynchronous, the absence of a stop bit can be detected. For example, an eight bit data character would have one start bit, eight data bits, and one or two stop bits. Therefore, a stop bit is expected as the 10th bit to be received. If the 10th bit is in the logic TRUE (marking) condition no error is detected. However, if the 10th bit is a logic FALSE (spacing) condition, the framing error flag is set. The framing error flag is useful for detecting open lines or null characters.

Data Functions: The M7390 performs serial-to-parallel and parallel-to-serial conversion. The parallel side of the module is TTL compatible. The serial inputs and outputs are available as three signal sources: EIA, current loop or TTL. The current loop and EIA input and output are available only on the eight-pin MATE-N-LOK connector on the front of the module.

The EIA input corresponds to RS-232C specifications. In addition to the EIA signals RECEIVED DATA and TRANSMITTED DATA, the DATA TERMINAL READY signal and SIGNAL GROUND are also provided.

The current loop input/output is designed to operate on a 20 to 100 mA current loop. The M7390 uses optical couplers to provide 1500 volts of isolation between the M7390 ground and power and the driving source. The serial input will respond to a 20 mA current flow. Current flow is a marking condition (binary 1). The external source must not exceed 35 volts dc open circuit voltage or 100 mA current. The serial output is a transistor switch that can turn a current loop on or off. The open circuit voltage of the current source must not exceed 35 volts dc.

The TTL versions of the serial input and output signals are available on the module pins and may be used in place of the level converter signals.

Control: The M7390 provides full control of the receiver and transmitter sections. All control pulses must be greater than 250 ns in width. Data to be loaded into the module must be present 250 ns before the DATA STROBE pulse.

Receiver Control Signals:

DA	Data Available
DA DLY	Delayed Data Available
AUTO RESET	Allows DA to be automatically reset.
RDE	Receiver Data Enable. Places data and control signals on the pins of the module.
RDA	Reset Data Available

Transmitter Control Signals:

TBMT	Transmitter Buffer Empty
ECO	End of Character

Error Control and other Signals:

NP	No Parity
POE	Parity Odd or Even
SWE	Status Word Enable
CS	Control Strobe
NB1, NB2	Number of Bits in data word
SB	Number of Stop Bits (1 or 2)
XR	External Reset (clears all registers)
RESET	Negative pulse used for clearing module during power-up.
RCLK	Receiver Clock Input
TCLK	Transmitter Clock Input

PRECAUTIONS

1. EIA and current loop connections are available on an 8-pin MATE-N-LOK connector located in the handle position on the B half of the board.
2. Provision is made to power this module from either −15 or −12 volts dc. Do not use both simultaneously.
3. Current loop input and output circuits must not have more than 35 volts peak applied or greater than 100 mA current flow.
4. The M7390 contains an MOS LSI chip. Care must be taken in proper handling and grounding of the module to prevent damage to the MOS chip.
5. The +10 volt dc supply is required only if the EIA level converters are used, or if the module is going to be used as a current source.
6. If the M7390 is used as a current source, 20 mA additional current must be supplied by the −15 volt and the +10 volt power supplies.

SPECIFICATIONS

Data Format: Asynchronous, serial by bit, least significant bit first.
Input/Output Level (Serial):

1. EIA RS-232C: Binary 1 = −3 to −25 volts dc
   Binary 0 = +3 to +25 volts dc
2. Current Loop: Mark (Binary 1) = 20 to 100 mA current flow
   Space (Binary 0) = <3 mA current flow
3. TTL: Binary 1 = HIGH
   Binary 0 = LOW

Data Rates: (TTY Mode) 110, 150, 300 Baud
(EIA Mode) 110, 150, 300, 600, 1200, 2400, and 4800 Baud.

Character Format: One start, 5, 6, 7, 8 data, parity (if requested), one or two stop bits.

Clock Frequencies (kHz): 1.76, 2.4, 4.8, 9.6, 19.2, 38.4, 76.8

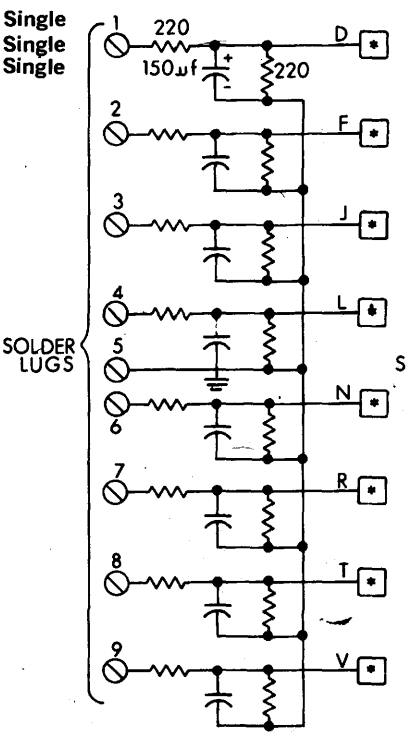
Input/Output Levels (Parallel): All TTL compatible.

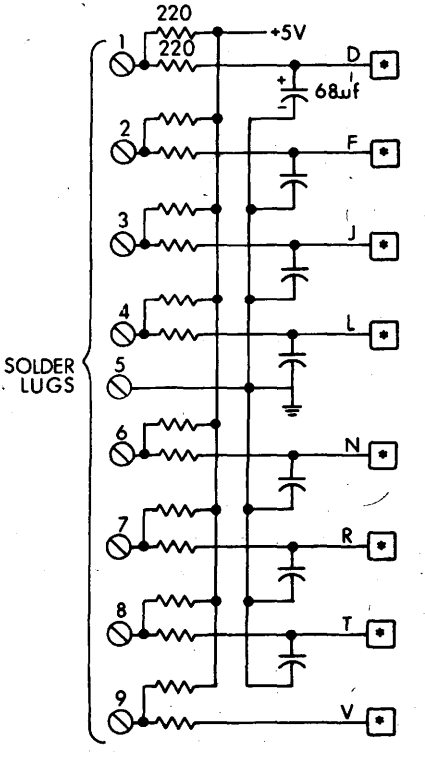
DRY CONTACT FILTERS

K580, K581

PULSE SHAPING

Length: Single
Height: Single
Width: Single

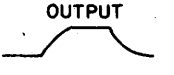


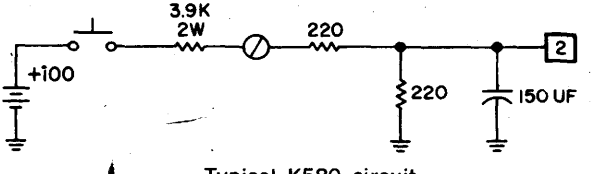


*Should be followed by a Schmitt trigger circuit for TTL logic.

K580

K581





Typical K580 circuit

These filters convert signals from dry or wiping contacts to logic levels. Primarily they are used with gold contacts such as encapsulated reed limit switches, thumbwheel switches, and the like. Those push-buttons or slide switches that provide good wiping action will also operate reliably with these filters.

Schmitt Triggers should be used on the outputs of both the K580 and K581 when they are used for one shot or timer inputs.

Access to K580 and K581 inputs is by solder lugs only. Strain relief holes are provided in the board (near handle) for a 9-wire cable. The avoidance of contact connectors on the logic wiring panel combined with heavy filtering guarantees noise isolation and protects modules by preventing accidental short circuits. Below is a summary of other characteristics.

	Contact Current	Contact Voltage	Output for Contact Closed	Time Delay on Closure	Time Delay on Opening
K580	22ma	See Table	high	10msec	30msec
K581	22ma	5V	low	20msec	20msec

(Time delay figures above are nominal, and assume connection to the input of a standard gate such as K113 or K123.)

The contact current for the K581 comes from the logic supply, making it very important to assure freedom from accidental high voltages on K581 inputs which could damage many logic modules by getting through to the system power supply. This hazard is not present with the K580, which uses an external source of +10 volts or more. The table below shows how external dropping resistors may be added to provide higher voltage operation.

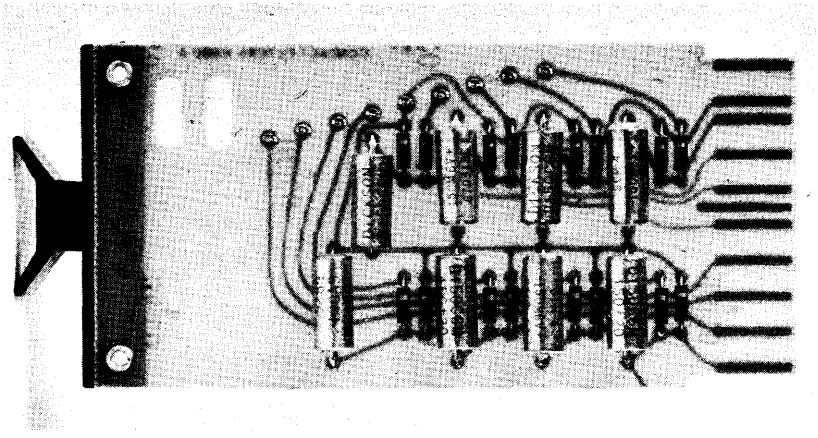
TABLE OF K580 VOLTAGE DROPPING RESISTANCES

CONTACT SUPPLY VOLTAGE	10	12	15	24	28	48	90	100	120
Dropping Resistance	0	82Ω	220Ω	620Ω	820Ω	1.8KΩ	3.6KΩ	3.9KΩ	4.7KΩ
Dissipation	—	0.05W	0.11W	0.3W	0.4W	0.85W	1.8W	2.0W	2.5W

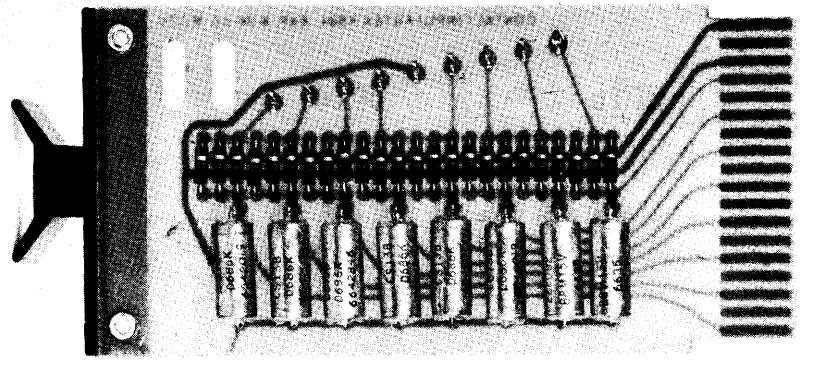
When using dropping resistors and higher voltage supplies, total tolerance of resistors and supply should be ±10% to insure high levels between +4 V and +6 V at the logic. Also observe that a handful of dropping resistors in 90 V or 120 V systems may dissipate more power than the entire logic system, and must be located so as not to cause excessive temperature rise in the logic system.

Note that these circuits may not be paralleled to obtain the wired OR or wired AND function, and that fanout is limited to 2 milliampers in order to maintain the low (zero) output voltage within normal specifications. Fanout to ordinary logic gates and diode expanders may be raised to 4 milliampers if some noise and contact bounce rejection can be traded off; but hysteresis inputs may not switch properly if the logic zero is allowed to rise much above +0.5 V.

Looking at the component side of both the K580 and K851, the solder lug connections are numbered 1 to 9 from pin end to handle end.



K580

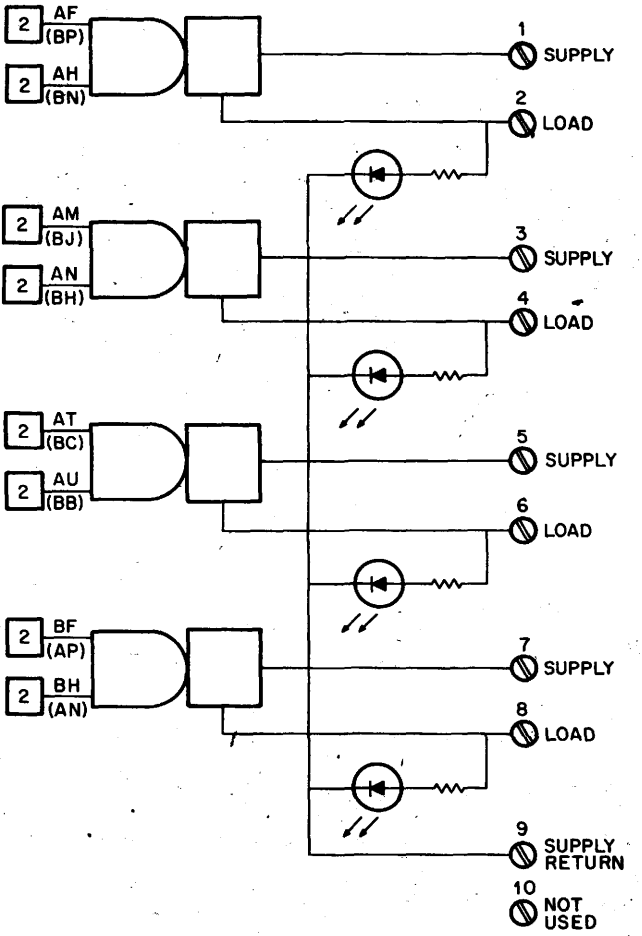


K581

ISOLATED AC SWITCHES
K616

LOGIC AMPLIFIERS

Length: Single
Height: Double
Width: Triple



Volts	Power mA (max.)	Pins
+5	100	AA1 AA2
GND		AC1 AC2

The K616 isolated ac switch module contains four isolated 120 Vac TRIAC output circuits. Each output is fused and has a light-emitting diode to indicate when the output is ON. The fuses can be changed from the terminal strip side of the module without removing field wiring or removing the module from the system. The K724 Interface Shell can be used to provide suitable mounting for the K616.

The K616 contains a 10-terminal nylon terminal strip with 3/8 spacing between terminals. The terminal strip meets NEMA and JIC specifications regarding barrier height and voltage breakdown. It has captive screws with wire clamps to accept 2-14 AWG wires and is color coded red for ac. Each terminal is marked according to its function: Supply (LINE), Switched Output (→) AC Return (NEUT), and Chassis Ground (GND).

SPECIFICATIONS

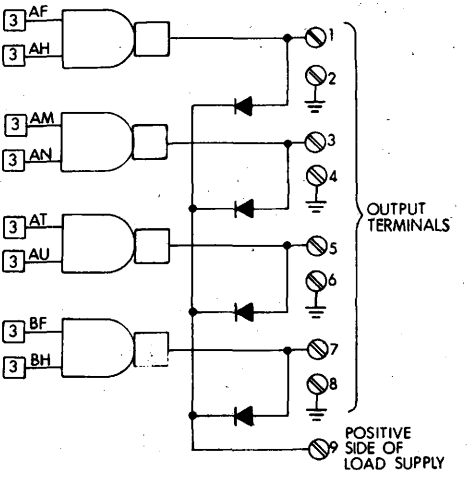
Output Turn On Time:	MIN: 1 μs MAX: 50 μs
Output Turn Off Time:	1/2 cycle of ac line maximum. (Turns off when output current goes through zero after removal of input)
Output Voltage:	12—140 V RMS AC, 50—400 Hz
Output Current:	0.030-5.0 A RMS AC
Output VA:	500 VA maximum per output, not to exceed 1000 VA for all four circuits.
Output Surge Current:	20 A for 1 cycle of AC line
Output Off State Leakage Current:	0.005 A maximum
Output Off State dv/dt:	Output will withstand a voltage change of at least 100 V/μs without turning on.
Output Indicator Light:	The LED indicator will indicate the presence of 80—140 Vac at the output terminal. It will be off if the output is off, or the fuse is open.
Fuse Protection:	5 A continuous Littlefuse type 275005
Temperature Range:	0°C to 70°C
Power Requirement:	+5 Vdc ±10% @ 100 mA MAX 70 mA TYP

DC DRIVER

K652

LOGIC AMPLIFIERS

Length: Single
Height: Double
Width: Triple



Volts	Power mA (max.)	Pins	
5V	*	AA2	
		BA2	* 10 mA with all circuits off
GND		AC2	160 mA additional per circuit on
		BC2	

K652 DC DRIVER

The K652 DC driver has four circuits each of which can deliver up to 2.5 amperes at up to 55 volts. Like the K578, K614, K656 and other modules, this unit has built-in clamp-type terminals for wires up to size 14. It can be mounted in the K724 interface shell, but does not have neon indicators across the output terminals as other shell mounted modules.

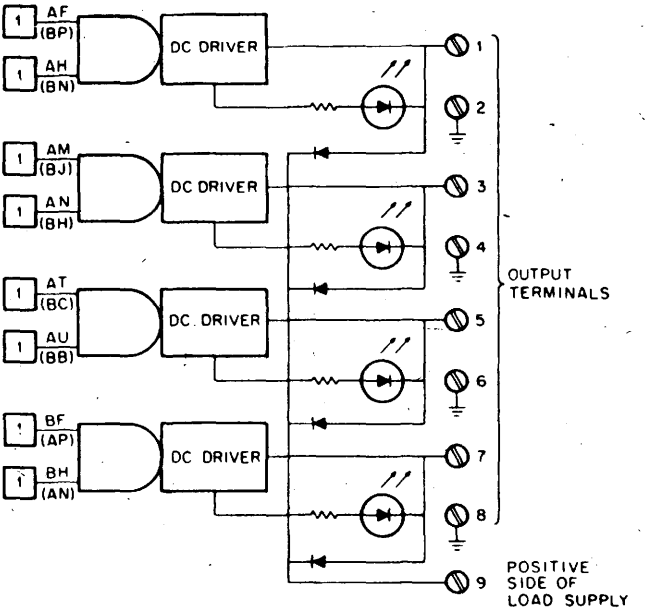
The positive side of the load supply should be connected to protect output transistors from damage due to turn-off transients. See the application section for further DC driver information.

Terminals 2, 4, 6 and 8 must be connected directly to the negative terminal of the load power supply or damage to the module will result from high currents.

DC DRIVERS
K657

LOGIC AMPLIFIERS

Length: Single
Height: Double
Width: Triple



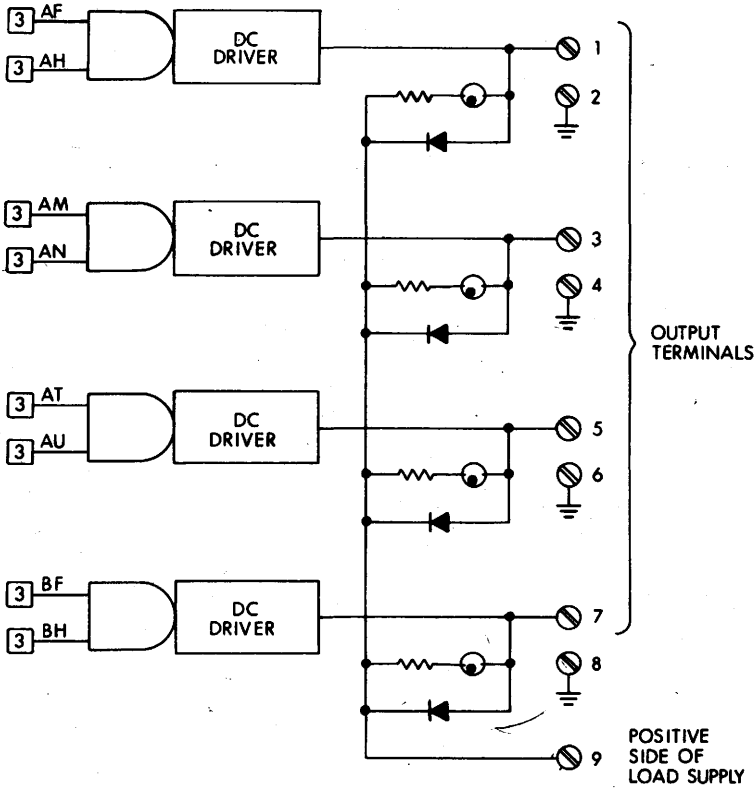
Volts	Power mA (max.)	Pins
+5V	*	AA2
GND		AC2

* 88 mA with all outputs off
130 mA with all outputs on.

The K657 DC Driver module contains four 250 Vdc drivers. Each circuit of this driver can switch to ground up to 1.0A at up to 250V The outputs will switch to ground whenever both AND gate inputs are high (logic 1).

DC DRIVER
K658

LOGIC AMPLIFIERS



Volts	Power mA (max.)	Pins
+5	*	AA2
GND		AC2

***10mA with all outputs off 350mA additional per circuit on.**

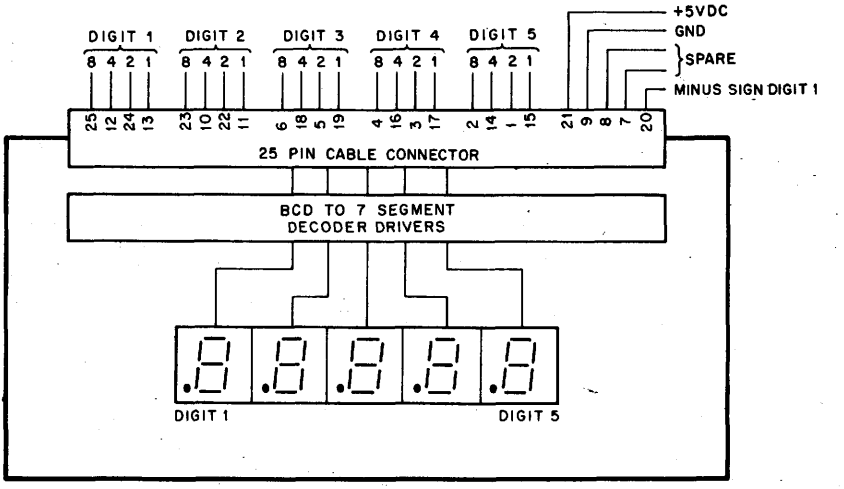
K658 4 AMP DRIVER

Each circuit of this versatile driver can deliver up to 4 amperes at up to 125 volts. This module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

Terminals 2, 4, 6 and 8 must be connected directly to the negative terminal of the load power supply or damage to the module will result from high currents.

5-DIGIT DISPLAY
K675

LOGIC AMPLIFIERS

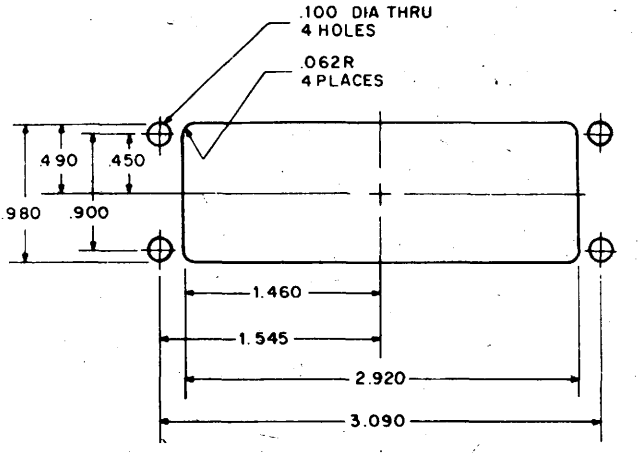


The K675 is a 5-digit display module designed to be panel mounted. Five digits of 7-segment LED readouts are housed in a plastic bezel with a lucite window which can be mounted through a panel cutout. The display is connected to the logic backplane wiring by a 10 foot, 25-conductor cable (BC14F) and a double height cable connector module, K783. Five digits of BCD-coded data, presented to the K783, will be displayed by the K675.

A blanking feature to suppress zeroes to the left of the last non-zero digit is controlled by a wire jumper on the display module. The display is pre-enabled for blanking but can be disabled by removing a wire jumper. If disabled, the K675 will display all BCD digits, including zeroes.

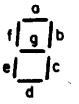
A decimal point is located to the left of each digit and can be controlled by jumpers W2 through W6. Removing a jumper will extinguish the corresponding decimal point.

Digit 1 can be used for a minus sign when displaying 4-digit negative numbers. When the minus sign is used, digit 1 is not available for displaying other numbers. The minus sign is illuminated by groundng pin 20 directly, or with a NAND gate or inverter.



Panel Cutout Dimensions

DISPLAY SEGMENTS

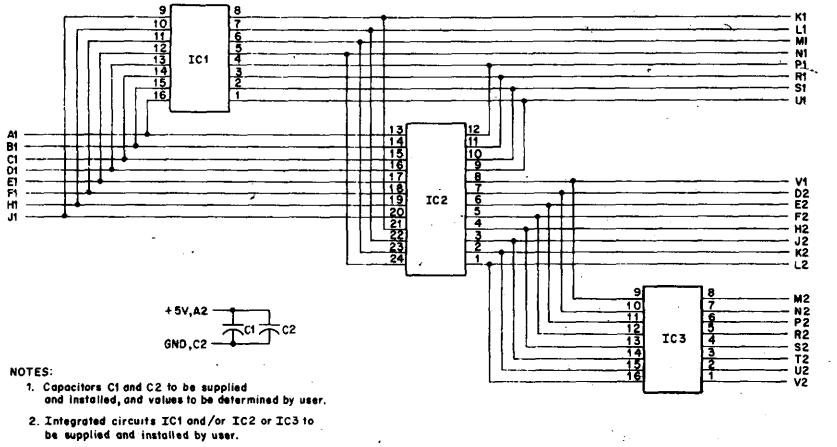


DECIMAL VALUE	BCD INPUTS 8 4 2 1	5082-7730/7731 SEGMENT OUTPUTS a b c d e f g	FONT
0	0 0 0 0	1 1 1 1 1 1 0	
1	0 0 0 1	0 1 1 0 0 0 0	
2	0 0 1 0	1 1 0 1 1 0 1	
3	0 0 1 1	1 1 1 1 0 0 1	
4	0 1 0 0	0 1 1 0 0 1 1	
5	0 1 0 1	1 0 1 1 0 1 1	
6	0 1 1 0	0 0 1 1 1 1 1	
7	0 1 1 1	1 1 1 0 0 0 0	
8	1 0 0 0	1 1 1 1 1 1 1	
9	1 0 0 1	1 1 1 0 0 1 1	
10	1 0 1 0	0 0 0 1 1 0 1	
11	1 0 1 1	0 0 1 1 0 0 1	
12	1 1 0 0	0 0 1 1 1 0 0	
13	1 1 0 1	1 0 0 1 1 0 1	
14	1 1 1 0	0 0 0 1 1 1 1	
15	1 1 1 1	0 0 0 0 0 0 0	

NOTE: 1 = Segment ON
0 = Segment OFF

W960
MSI MODULE BOARD

MISCELLA-
NEOUS



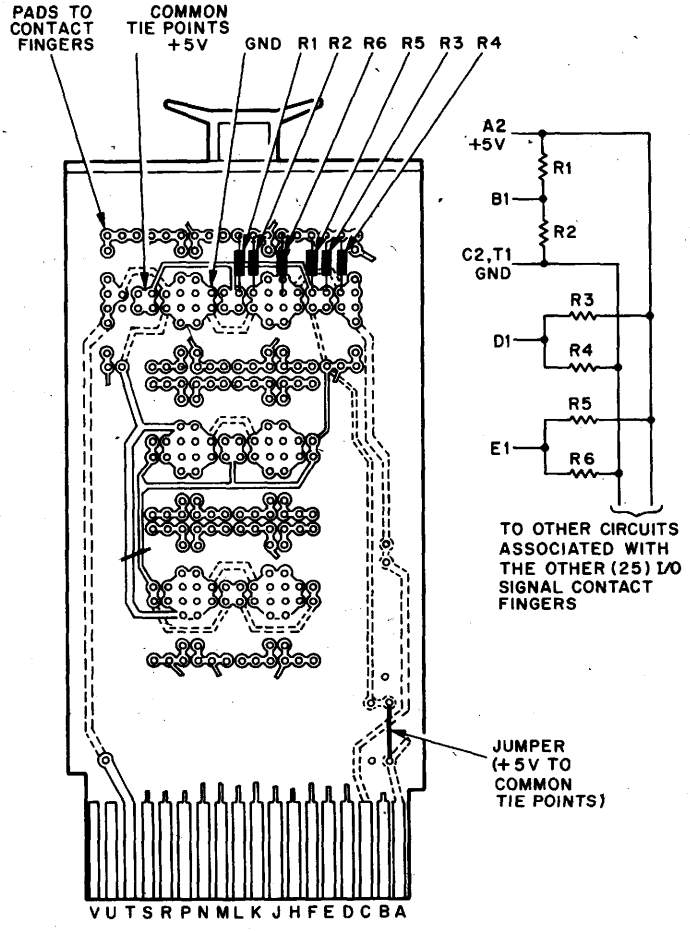
NOTES:

1. Capacitors C1 and C2 to be supplied and installed, and values to be determined by user.
2. Integrated circuits IC1 and/or IC2 or IC3 to be supplied and installed by user.

The W960 MSI Module Board is a single-height, standard length module board that can accommodate either two 14- or 16-pin dual-in-line package (DIP) integrated circuits (ICs) or one 24-pin DIP IC, either with or without sockets. All IC pin plated-through hole locations are identified with their associated board contact finger and are all brought out to the board contact fingers via printed circuit etching, as shown on the schematic diagram.

W964
UNIVERSAL TERMINATOR BOARD

MISCELLA-
NEOUS



NOTES:

1. All PC etch not shown; of that shown, side 1 etch shown with solid lines and side 2 etch shown with dashed lines.
2. Resistance values to be determined by user.
3. Resistors to be supplied by user.
4. Pull-up/termination network schematic diagram shows three typical networks (to contact fingers B1,D1, and E1)

W964 Component Layout Diagram
and Pull-Up Termination Schematic Diagram

The W964 Universal Terminator Board is a single-height, standard length module. It is an etched and drilled module that can be used for mounting user-selected and user-supplied discrete components to provide a variety of termination or voltage source circuits for up to 28 signal pins. Each signal pin can have two components connected to ground and one component connected to +5 volts. Any discrete component can be mounted on the W964 if the physical size is approximately the size of a 1/4-W resistor or disk capacitor. Three typical pull-up/termination network circuits are illustrated on the component layout and schematic diagram.

The 28 contact fingers (signal pins) that can be used for I/O signals are B1, D1, E1, F1, H1, J1, K1, L1, M1, N1, P1, R1, S1, D2, E2, F2, H2, J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The pads associated with the contact fingers are identified on the boards to facilitate mounting the discrete components. Contact fingers A2 and B2* are dedicated to voltage. Contact fingers C2 and T1 are dedicated to ground.

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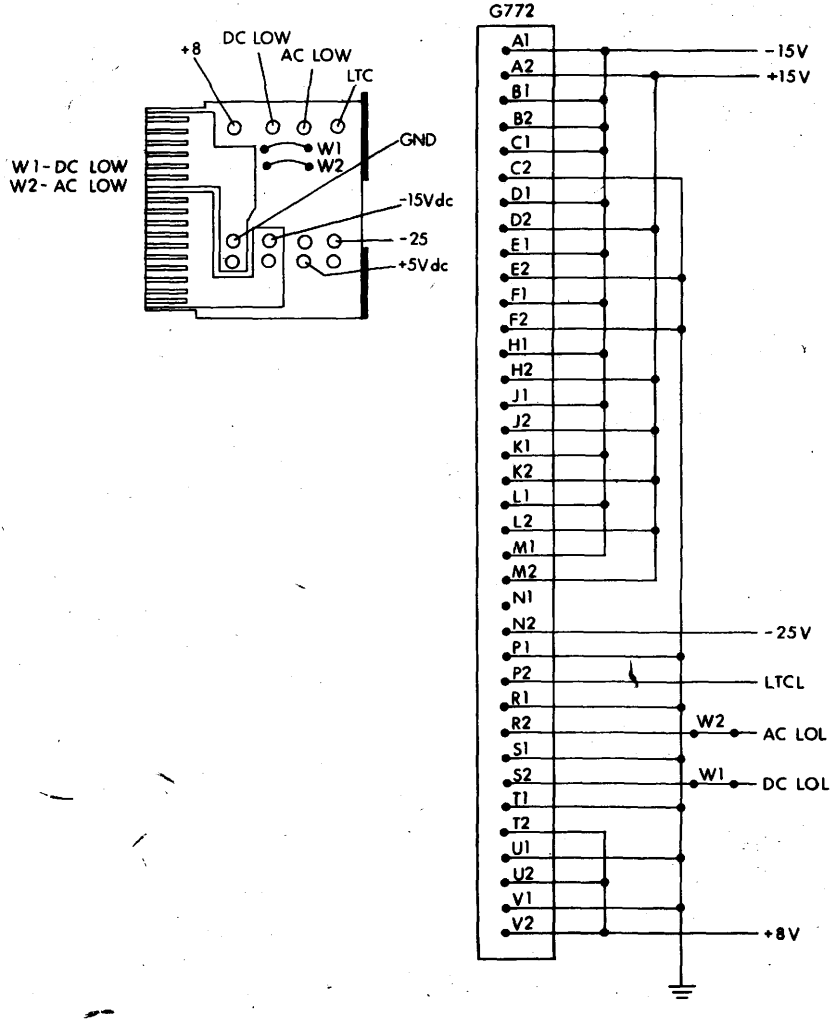
* In many systems, contact finger B2 is bused to −15 V.

G772
POWER CONNECTOR

MISCELLA-
NEOUS

The G772 is a single-width, single-height, short-length board used to connect power to a backplane assembly such as a BB11 or DD11.

G772 Typical Connector Assignments

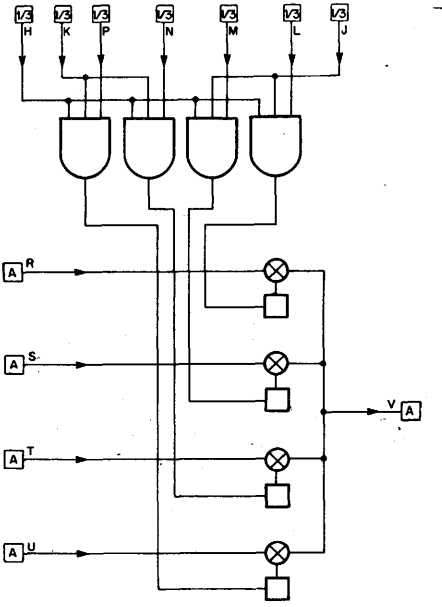


A123
FOUR-INPUT MULTIPLEXER

MULTI-PLEXERS

A SERIES

Length: Standard
Height: Single
Width: Single



A *ANALOG SIGNALS
(DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+10	18	D2
+5	45	A2
GND		C2, T1
−20	50	E2

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0V and +3V. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3V (or not connected) the two output terminals are connected together. If any digital input is at 0V, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10V and −10v, with currents up to 1 mA.

The positive power supply must be between +5V and +15V, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between −5 and −20v, and at least 10 Volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30V.

SPECIFICATIONS

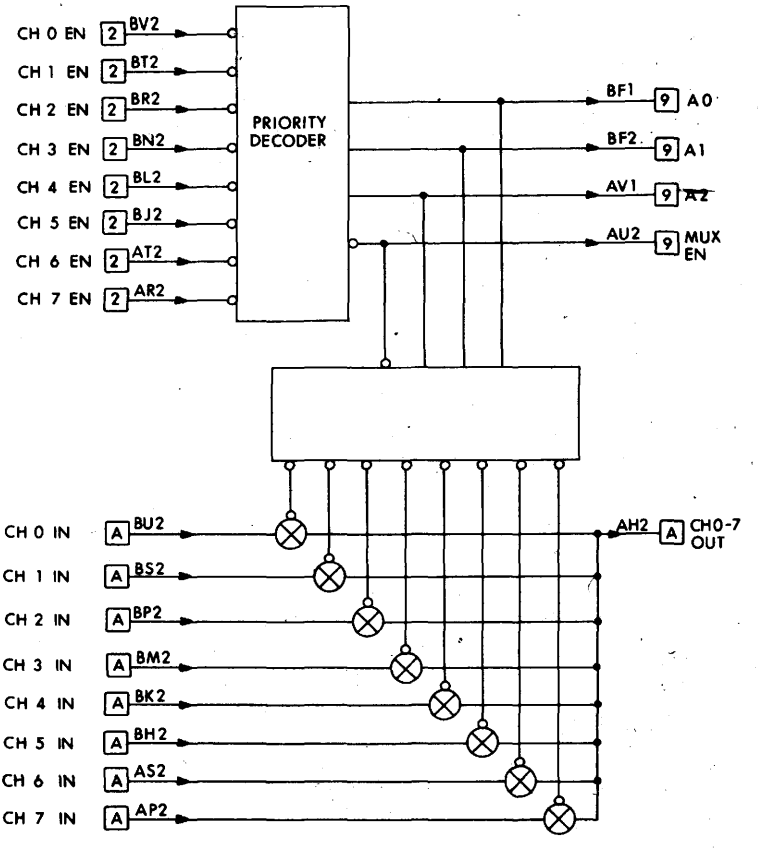
Digital Inputs	
Logic ONE:	+2.4v to +5.0V
Logic ZERO:	0.0v to +0.8V
Input loading:	0.5mA. at 0Volts
Analog Signal	
Voltage range:	+10v to −10v
Current (max.):	1 mA
Output Switch	
On resistance, max.:	1000 ohms
On offset:	0 Volts
Off leakage, capacitance:	10 nA, 10 pF
Turn on delay, max.:	0.2 μsec
Turn off delay, max.:	0.5 μsec

A126
8 CHANNEL HIGH IMPEDANCE MULTIPLEXER

MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5V±5%	100	AA2
+15V±5%	17	AD1, AD2
−15V±5%	12	AE1, AE2
*GND	LOGIC	AC2, AT1
*GND	ANALOG	AF1, AF2

*Analog GND must be connected to LOGIC GND

The A126 is an eight-channel, high-impedance multiplexer module with each channel controlled by an associated enable input. The conduction or non-conduction of each channel is controlled by FETs and the channel outputs are connected together to a common terminal. Each channel is capable of switching bipolar (±12 V) analog signals and is protected against random switching in the event of overvoltage and power down or loss of power conditions.

FUNCTIONS

The enable inputs, associated with each channel, are priority encoded to ensure that only one channel is connected to the output at a time. Therefore, more than one Channel enable input can be asserted at one time. Channel 0 is the highest priority and channel 7, the lowest priority. The enable signals required are TTL or DTL compatible levels. Three TTL outputs are provided for identifying the selected channel, and one TTL multiplexer enable output indicates that one of the eight channels has been selected. The selected channel number is specified by an octal code on lines A0-A2.

APPLICATIONS

The A126 can be used to multiplex up to eight signals from the analog inputs into buffer amplifiers or circuits with a minimum input impedance of 10 megohms.

SPECIFICATIONS

Analog Inputs:

CH0 (IN) — CH7 (IN)	8 single-ended channel inputs
Voltage Range	±15 V (max.)
Impedance (ON)	1040 ohms ± 10%
Analog switch turn-on	1.0 μsec (max.)
Analog switch turn-off	0.5 μsec (max.)
Analog switch current	2.0 mA (max.)
Jumper W1	(Not for customer use)

TTL Input Signals

CH0 (EN) — CH7 (EN)	8 enable inputs associated with each channel
Input Voltage	Low (enable) — 0.8 V (max.) High (disable) — 2.0 V (max.)

TTL Output Signals

A0 — A2	A 3 bit code identifying the channel that is currently enabled.
MUX EN	Asserted low whenever one or more channels is enabled.

TRUTH TABLE

TTL ENABLE INPUTS								OUTPUTS				
CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	MUX EN	A2	A1	A0	Analog Channel
H	H	H	H	H	H	H	H	H	H	H	H	NONE
H	H	H	H	H	H	H	L	L	H	H	H	7
H	H	H	H	H	H	L	X	L	H	H	L	6
H	H	H	H	H	L	X	X	L	H	L	H	5
H	H	H	H	L	X	X	X	L	H	L	L	4
H	H	H	L	X	X	X	X	L	L	H	H	3
H	H	L	X	X	X	X	X	L	L	H	L	2
H	L	X	X	X	X	X	X	L	L	L	H	1
L	X	X	X	X	X	X	X	L	L	L	L	0

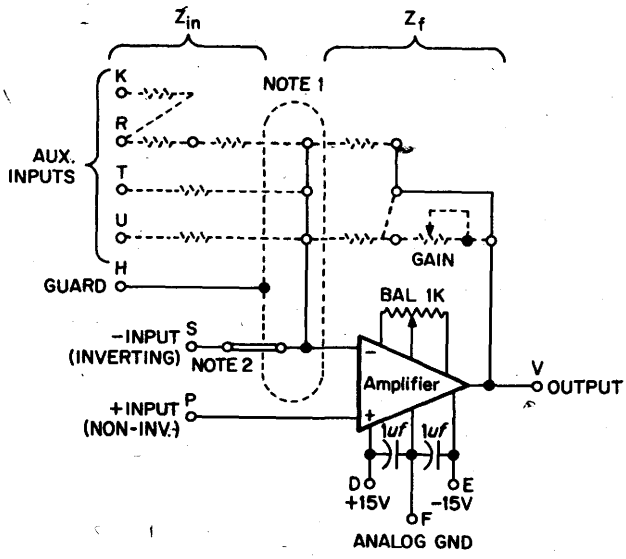
H = High Level L = Low Level X = Either High or Low

A207
OPERATIONAL AMPLIFIER

AMPLIFIERS

A SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+15	6	D2
GND	ANALOG	F2
−15	10	E2

NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time (5 μs to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

SPECIFICATIONS—At 25°C, unless noted otherwise.

		Pins L & M Differences with Pins Connected L & M Not Connected
Settling Time*		
Within 10 mV, 10V step input, typ:	3 μsec	6 μsec
Within 10 mV, 10V step input, max:	5 μsec	8 μsec
Within 1 mV, 10V step input, max:	7 μsec	10 μsec
Frequency Response		
Dc open loop gain, 670 ohm load, min:	15,000	100,000
Unity gain, small signal, min:	3 MHz	
Full output voltage, min:	50 kHz	
Slewing rate, min:	3.5v/μsec	
Overload recovery, max:	8 μsec	
Output		
Voltage, max:	±10V	
Current, max:	±15 mA	
Input Voltage		
Input voltage range, max:	±10 V	
Differential voltage, max:	±10V	
Common mode rejection, min:	10,000	
Input Impedance		
Between inputs, min:	100 k ohms	
Common mode, min:	5 M ohms	
Input Offset		
Avg. voltage drift vs. temp, max:	60 μV/°C	30 μV/°C
Initial current offset, max:	0.5 μA	
Avg. current drift vs. temp, max:	5 nA/°C	
Temperature Range	0°C to +60°C	

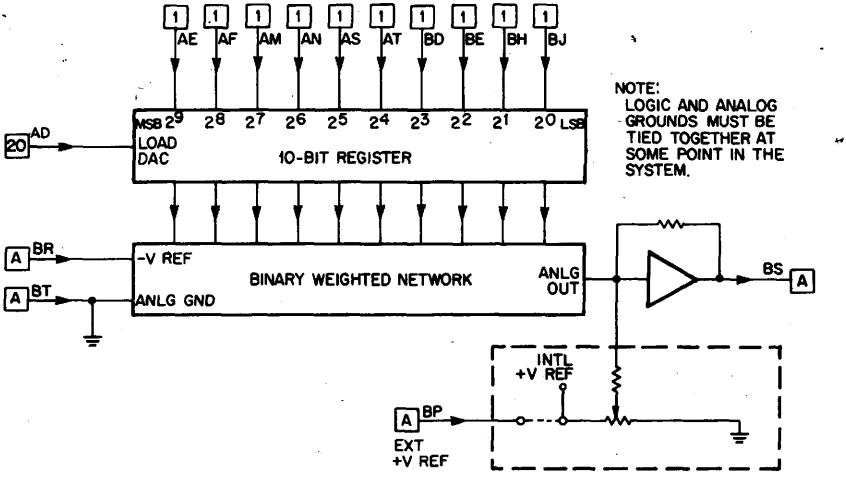
*Gain of 1, inverting or non-inverting configuration.

A619
10-BIT D/A CONVERTER
SINGLE BUFFERED

DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double



Volts	Power mA (max.)	Pins
+15	25**	BV2
+5	135	AA2
GND	LOGIC	AC2
GND	ANALOG	BT2
−10.06*	60	BR2
−15	35**	BU2
−15	50	AB2

* ref.
** plus output loading

The A619 Digital to Analog Converter (DAC) is complete with a 10-bit buffer register, level converter, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greater efficiency and optimum scale factor matching in multi-channel applications. The module is double width (1") in the B connector half.

The A619 DAC output voltage is bi-polar. Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard) A619
0000_8	−5V
0400_8	−2.5V
1000_8	0 Volts
1400_8	+2.5V
1777_8	+5V

A619 SPECIFICATIONS

OUTPUT:

Voltage:	±5 volts
Current:	10 mA. (max)
Impedance:	<0.1 ohm
Settling Time:	
(Full scale step, resistive load)	<5.0 μs
(Full scale step, 1000 pf)	<10.0 μs
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT

Level: 1 TTL Unit Load
Pulse: (positive)

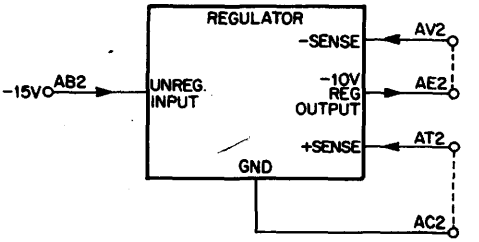
Input loading: 20 TTL Unit load	
Rise and Fall Time:	20 to 100 nsec
Width:	>50 ns
Rate:	10^6 Hz max.

Timing:

Data lines must be settled 40 ns before the "LOAD DAC" pulse (transition) occurs.

A704
REFERENCE SUPPLY

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
−15*	250	AB2
GND	ANALOG	AC2

* plus or minus 2 volts

The A704 Reference Supply converts an ordinary −15 volt logic supply voltage into a precisely adjustable regulated −10 volt reference source for A/D and D/A converters of up to 13 binary bits.

FUNCTIONS

Remote Sensing: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load.

When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μF should be connected across the load at the sensing point.

Preloading: The supply may be preloaded to ground or −15 volts to change the amount of current available in either direction. For driving DEC Digital/Analog Converter modules, −125 mA maximum can be obtained by connecting a 270-ohm plus or minus 5%, one-watt resistor from the reference output (pin AE2) to ground (pin AC2).

SPECIFICATIONS

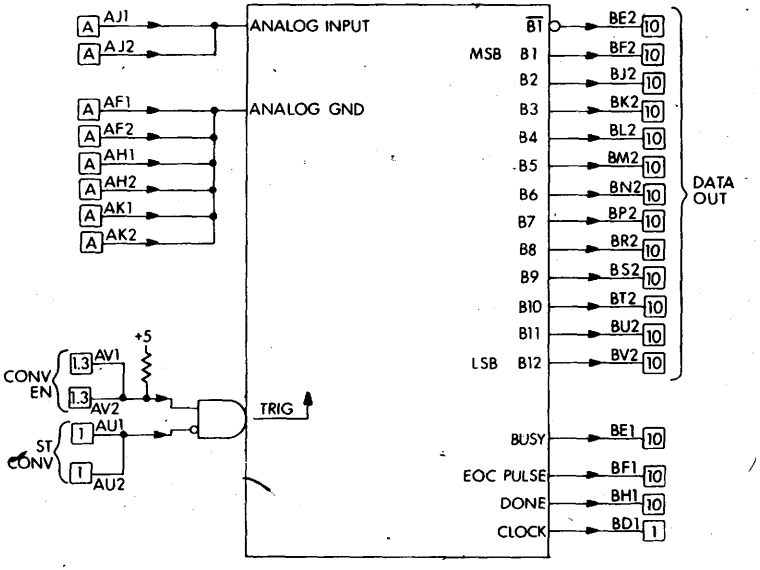
Input Power	−15 V
Use:	See text for sensing and preloading
Output:	−10 V
Current:	−90 to +40 mA
Regulation:	0.1 mV, no load to full load
Temperature Coefficient:	1 mV/8 hrs 1 mV/15 to 35 degrees C 4 mV/0 to 50 degrees C
Peak-to-Peak Ripple:	0.1 mV
Adjustment Resolution:	0.01 mV
Output Impedance:	0.0025 ohms

A866
HIGH-SPEED 12-BIT BIPOLAR A/D CONVERTER

ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (nominal)	Pins
+5V±10%	300	AA1, AA2, BA1, BA2
+15V±3%	75	AD1, AD2
−15V±3%	40	AE1, AE2
LOGIC GND		AC1, AC2, AT1, BC1, BC2, BT1

The A866 is a 12-bit general purpose analog-to-digital converter module which uses the successive approximation technique. The A866 is designed to accept unipolar or bipolar single-ended analog voltage as input and convert it to a 12-bit TTL-compatible, coded digital output. The coded digital output is parallel data and is available for application to a computer, terminal, display, or other logic device.

The selection of unipolar or bipolar and voltage range of the analog input is determined by jumper leads mounted on the module circuit board. The module has factory-installed jumpers that permit its use with bipolar, 10-volt full-scale extended-range inputs. By changing the jumper configuration, the user can select bipolar or unipolar, 5-volt or 10-volt full scale extended or nonextended input ranges.

The extended range is particularly useful when the output data is used in computations because the LSB is easily expressed as an integer submultiple of the full scale; i.e., full scale/2000_{10} rather than full scale/2048_{10} for a bipolar configured module and full scale/4000_{10} rather than full scale/4096_{10} for a unipolar configured model. Therefore, less rounding-off error occurs during the computations. In addition, extended range provides some overscale input capability; i.e., +0.2350 Volt and −0.2400 Volt (+10.2350 Volts and −10.2400 Volts full overscale inputs) for a bipolar configured module and +0.2375 Volt (+10.2375 Volts full overscale inputs) for a unipolar configured module. The coded output is 12-bit binary and two's complement using the MSB output and the MSB output respectively.

The A866 can be used wherever fast, accurate analog-to-digital conversions are required.

The high input impedance (100 megohms) at the analog inputs minimizes the signal source loading, and the fast conversion time permits an encoding rate at the output of 16,000 conversions per second.

The digital output data, the output control and status signals, and the input control signals are all TTL-compatible.

APPLICATIONS

The A866 Analog-to-Digital Module is suitable for use in scientific and industrial research applications. It provides fast, accurate analog-to-digital conversion from transducers, bridges, or similar instrumentation.

The A866 Module has factory-installed jumpers that permit its use with bipolar, 10-volt full scale extended range inputs where a change of 5.0 millivolts at the input corresponds to a change of 1 LSB at the output. The A866 Module may be reconfigured with jumpers by the user so that it will accept analog inputs of any of the following:

bipolar ± 10-Volt full scale extended range
bipolar ± 10-Volt full scale nonextended range
bipolar ± 5-Volt full scale extended range
bipolar ± 5-Volt full scale nonextended range
unipolar + 10-Volt full scale extended range
unipolar + 10-Volt full scale nonextended range
unipolar + 5-Volt full scale extended range
unipolar + 5-Volt full scale nonextended range

Table I

Bipolar ± 10 Volt Full Scale, Extended Range
Analog Input Output Code Conversion Chart

Analog Voltage Input	Two's Complement Output Code*		Scale
	Base 10	Base 8	
+10.2350 V	2047	3777	+Full Overscale
+10.2300 V	2046	3776	+Full Overscale — 1 LSB
+10.0000 V	2000	3720	+Full Scale
+ 7.5000 V	1500	2734	+¾ F.S.
+ 5.0000 V	1000	1750	+½ F.S.
+ 2.5000 V	500	0764	+¼ F.S.
+ 0.0050 V	1	0001	+1 LSB
0.0000 V	0	0000	Zero
— 0.0050 V	— 1	7777	—I LSB
— 2.5000 V	— 500	7014	—¼F.S.
— 5.0000 V	—1000	6030	—½ F.S.
— 7.5000 V	—1500	5044	—¾ F.S.
—10.0000 V	—2000	4060	—Full Scale
—10.2350 V	—2047	4001	—Full Overscale — 1 LSB
—10.2400 V	—2048	4000	—Full Overscale

Note: When an A866 module is jumpered to accept ±5 Volt full scale inputs, the inputs are exactly ½ of the input value shown in the above table.

* Using MSB output.

Table II

Bipolar ± 10 Volt Full Scale, Non-extended Range
Analog Input to Output Code Conversion Chart

Analog Voltage Input	Two's Complement Output Code**		Scale
	Base 10	Base 8	
+10.0000 V	Not Valid	Not Valid	+Full Scale
+ 9.9951*V	2047	3777	+F.S. — 1 LSB
+ 7.5000 V	1536	3000	+¾ F.S.
+ 5.0000 V	1024	2000	+½
+ 2.5000 V	512	1000	+¼
+ 0.0048*V	1	0001	+1 LSB
0.0000 V	0	0000	Zero
— 0.0048*V	— 1	7777	—1 LSB
— 2.5000 V	— 512	7000	—¼F.S.
— 5.0000 V	—1024	6000	—½ F.S.
— 7.5000 V	—1536	5000	—¾ F.S.
— 9.9951*V	—2047	4001	—F.S. — 1 LSB
—10.0000 V	—2048	4000	—Full Scale

Note: When an A866 module is jumpered to accept ±5 Volt full scale inputs, the inputs are exactly ½ of the input values shown in the above table.

* Rounded off value.
** Using MSB output.

SPECIFICATIONS

Analog Input

Type of Input	Single-ended
Impedance	>100 megohms
Input Bias Current	6 nanoamperes, (max.)
Overvoltage Limit	±18 volts, (max.)
Perturbations	The encoding process does not cause noise at the input

Encoding Process

Technique	Successive approximation
Quantizing Resolution	1 part in 4095 of full range
Encoding Word Time	15 microseconds, max. (includes Op-Amp settling time)
Encoding Word Rate	64,000 conversions/second, min.
Code	Binary and 2's complement (using MSB and complement of MSB)

Measurement Accuracy Uncertainty at 23°C

Warm-up Time	3 minutes
Absolute (Ref. to NBS STDS)	±1 LSB at full scale, max.

Stability

Overall Tempco	±1/20 LSB/°C, max.
Tempco of Clock Period	±0.1 percent/°C, max.
Long Term	±1/2 LSB/6 mos., max.

Sensitivity to Power Supply Voltage Changes

For the ±15 Volt Supply	0.002% % V, max., from dc to 1 MHz
For the ±5 Volt Supply	0.0003% % V, max., from dc to 1 MHz

FUNCTIONS

Analog Inputs

The single-ended dc analog input will accept unipolar or bipolar voltage with a maximum amplitude of 10 V.

Control Inputs

A high to low level change on either of the two ST CONV inputs when the CONV EN input is high or a low to high transition on either of the two CONV EN inputs when the ST CONV input is low will start the conversion process.

Data Outputs

The data outputs are 12 parallel bits plus the complement of B1 (MSB). Bit B12 is the LSB. The output code is available in a binary format when the B1 output is used and in two's complement when B1 output is used. The outputs are TTL-compatible levels.

Status Outputs

Three outputs are provided to indicate the status of the conversion process. The BUSY output becomes high and remains high while the conversion process is active. The BUSY output becomes low 50 ns after the data is available at the output and remains low until the next command to start the conversion.

The DONE output is the complement of the BUSY level.

The EOC PULSE output becomes a high level for 450 ±50 ns after the DONE output level goes high.

The CLOCK output is a series of 50 ns pulses (min.) generated when the A866 Module is performing an analog-to-digital conversion.

Detailed information on the module is available on the A866 A/D Converter Module (12-Bit, 15-Microsecond) data sheet available from Logic Products Sales Support, Accessories & Supplies Group, DIGITAL, MK1-2/E13, Merrimack, NH 03054.

K SERIES

K-Series modules are briefly described below. Detailed descriptions are contained in previous editions of the Logic Handbook, and can also be supplied by Logic Products Sales Support at DIGITAL Equipment Corporation, MK1-2/E13, Merrimack, NH 03054.

K003, K012, K026, K028 Gate Expanders
These inexpensive gate expanders offer great logic flexibility and versatility without a proliferation of module types. It must be understood that these gate expanders are merely expansions for other K Series gates and can never be used as separate AND or OR functions.

K113, K123, K124 Logic Gates
Together with the K003, K012, K026 or K028 expanders, these gates perform any desired logic function, including AND, OR, AND/OR, NAND, NOR, exclusive OR, and wired AND.

K134 Inverters
This module contains four inverters with AND expansion capability and an inhibit input. It may also be AND expanded by K003 Gate Expanders.

K135 Inverters
This module is designed for use in applications that require inverters with OR expandability. Four inverter circuits with OR expansion capability and as common enable pin are contained on the module.

K138 Inverters
The K138 contains eight inverter circuits that can be used to invert other K Series outputs to obtain both High (+5V) and Low (0V) levels.

K161 Binary-to Octal Decoder
Three-bit binary numbers at the input to this module will be decoded into eight one-at-a-time outputs.

K174 Digital Comparator
This module determines which of two 4-bit binary or one digit BCD quantities is larger or smaller.

K201 Flip-Flop
This superslow memory simplifies sequencing of machine motions, and finds other applications where the ultimate in noise isolation is needed and speed is no problem. Its 1 KHz maximum repetition rate makes this flip-flop noticeably more resistant to extremely noisy surroundings than faster types.

K202 Flip-Flop
This module performs shifting, complementing, counting, and other functions that are beyond the capabilities of simple set-reset flip-flops built up from logic gates.

K206 Flip-Flop Register
The 4-bit, set-reset flip-flop register can be used to buffer input signals, to store one BCD digit, or as a simple 4-bit memory.

K207 Flip-Flops
The K207 is a 4-bit, set-reset flip-flop buffer which can be used to manipulate or store data.

K210 Counter
The K210 is a binary or BCD counter that can be wired to return to zero after any number of input cycles from 2 to 6.

K211 Programmable Divider
The K211 is a binary counter that can be wired to produce a high to low output transition after any number of input cycles from 2 to 16. Count-up occurs on the high to low transition of the count gate output.

K220 Four-Bit BCD/Binary Up/Down Counter
The K220 Counter module provides all the circuitry necessary for binary and binary coded decimal up counting, down counting, presetting and clearing. This module is useful in many digital position readout and feedback applications.

K230 Shift Register
The K230 consists of a 4-bit shift register with a serial data input. Data at the input is shifted left with each high-to-low transition at the shift input gate.

K265 Reed Relay Drivers
The K265 has drive circuits for customer mounted relays. Up to five relays with Form A contacts can be mounted on the single height card. A logic 1 at each input energizes the relay to provide isolated contact outputs for special interfacing applications.

K281 Fixed Memory
This module is a diode board containing eight 4-bit words which can be used to construct read-only memories. Codes are stored by cutting out diodes where zeros are desired.

K282 Diode Memory
The K282 is a diode matrix module which initially contains eight 16-bit words.

K302 Dual Timers
The K302 module contains two independent timer circuits. Each circuit provides three delay ranges: Range one: 0.01 to 0.3 seconds; Range two: 0.1 to 3.0 seconds; Range three: 1.0 to 30 seconds.

K303 On/Off Delays
The K303 can be used for either an ON or OFF delay with a range of 10 μs to 30 seconds or can be interconnected to form a clock with a period covering the same range.

K323 One-Shots
This module contains three one-shots that provide output pulse widths from 10 μs to 30 seconds with either fixed or adjustable delays.

K371, K373, K374, K375, K376, K378 Timer Controls
Calibrated controls for timers, one-shots, and clocks are available in several ranges:

K371 Clock Control, 200 Hz to 6 KHz
K373 Clock Control, 20 Hz to 600 Hz
K374 Calibrated Timer Control, 0.01 sec. to 0.3 sec.
K375 Clock Control, 2 Hz to 60 Hz
K376 Calibrated Timer Control, 0.1 sec. to 3 sec.
K378 Calibrated Timer Control, 1 sec. to 30 sec.

All of the above controls mount on the K303 and K323 modules.

K501 Schmitt Trigger
The K501 can be used with the K580 or K581 to provide simultaneous true and complementary signals with full K series drive. Built in hysteresis and slowed outputs insure reliable operation in noisy signal environments.

K990 Timer Component Board
The K990 is a predrilled etched module for mounting up to six RC networks for K303 or K323 timer controls.

K579 Isolated AC Input Connecters
The K579 is used to convert 120 VAC inputs to 0 and + 5 Vdc logic levels. The module has eight transformer-isolated Schmitt trigger circuits that provide contact bounce rejection and cause a + 5V output when 120 VAC is applied to the corresponding input. Each input has an LED indicator to indicate when voltage is present.

K-to-M, M-to-K Converters
Module M 521 converts from K-series signal levels to M-series, and Module M 671 converts from M to K. Both are described elsewhere in this Handbook.

CABINETS AND PARTS

SYSTEM ENCLOSURES, MOUNTING HARDWARE, CONNECTORS, POWER SUPPLIES, OTHER DESIGN AIDS

CABINETS AND PARTS

This section is organized into several subgroups as follows:

1. Cabinets and Cabinet Accessories
2. Module System Enclosures
3. Power Supplies
4. 19-Inch Mounting Panels
5. Four-Slot System Units
6. Nine-Slot System Units
7. Module Connector Blocks
8. Blank Module Boards
9. Collage Module Boards
10. Module Extender Boards
11. Wire Wrappable Module Boards
12. Wire Wrapping Tools and Accessories
13. Integrated Circuit Sockets
14. Module Handles, Handle Extenders, and Module Holders
15. Bus Strips, Patch Cords and Accessories

CATALOG SALES

Now, many of the items described in this section are available at substantial savings through the DIGITAL Direct Sales Catalog. Send for your own free copy of the Catalog by filling out the post card included in this Handbook.

H960 SERIES EQUIPMENT CABINETS

This section describes DIGITAL's "standard" and "short" size basic equipment cabinets. Two additions to the cabinet line, the H984-B and H9800-A, are described following this section. The standard and short models accept panels or equipment designed to mount in standard 19-inch (48.26 cm) electronics cabinets or racks. Basic color of these cabinets is black. Gray is used for end panels and the border of the cover panels.

The cabinets can be placed individually or attached to form a multibay configuration. The accessories and hardware available include front and rear doors, panel mounting door frames and door skins, end panels, bezel and logo panels, blower fans, and power controllers.

Standard Size Cabinets and Accessories

Five basic cabinet configurations (H960-BC, H960-BD, H960-CA, H961-A, H961-AA) are available in the standard size cabinet series. The H961-A, -AA are intended primarily for add-on configurations. The standard size cabinet is 71.5 in. (181.61 cm) high and provides 63.0 in. (160.0 cm) of vertical mounting space at the front; an additional 63.0 in. of mounting space is available at the rear of the cabinet. These cabinets are configured to meet the requirements of most customer applications.

All standard size cabinets are configured around the basic H950-AA Cabinet Frame. These cabinet frames are drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings to accommodate equipment, panels, or devices which are designed to mount in standard 19-in. (48.26-cm) electronics cabinets or racks. Some of the cabinets contain an 861-A, 861-B, or 861-C Power Controller for distribution and control of the main power to the equipment installed. Six of the cabinet configurations include a rear mounting panel door frame, which is also drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings; this mounting panel door frame allows the equipment and devices mounted on it to be swung out for maintenance or adjustment. Optional accessories as specified by the customer can be added to any of the available configurations. The parts and accessories included with each of the four standard size cabinet configurations are listed in Table 1, which also lists the optional accessories that are available for use with these cabinets. All cabinets are completely assembled before shipment.

Figure 1 illustrates a typically configured standard size cabinet front. Figure 2 illustrates the installation of typical accessories on a standard size cabinet frame, and Table 2 identifies and describes these accessories. Complete descriptions of the H950-AA Cabinet Frame and the accessories for standard size cabinet frames are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Cabinet Assembly

Table 1
Standard Cabinets
H960-BC, H960-BD, H960-CA, H961-A, H961-AA

H960-BD	H960-BC	H960-CA	H961-A	H961-AA	Catalog No.	Description
1	1	1	1	1	H950-AA	Cabinet Frame, 19 in. wide, 69 in. high, 25 in. deep
1		1			H950-BA	Full Door (RH) (front or rear mounting)
					H950-CA	Full Door (LH) (front or rear mounting)
1	1	1		1	H950-DA	Mounting Panel Door Frame (RH) (rear mounting)
			1		H950-EA	Mounting Panel Door Frame (LH) (rear mounting)
1	1		1	1	H950-FA	Mounting Panel Door Skin
					H950-HA	Short Door (covers 21 in. mounting space)
					H950-HC	Short Door (covers 26¼ in. mounting space)
					H950-HD	Short Door (covers 31½ in. mounting space)
					H950-HF	Short Door (covers 42 in. mounting space)
					H950-HG	Short Door (covers 47¼ in. mounting space)
					H950-HH	Short Door (covers 52½ in. mounting space)
					H950-HK	Short Door (covers 63 in. mounting space)
					H950-JA	Short Door (covers 21 in. mounting space) (used with H952-BA installed)
					H950-LA	Logo Frame Panel (aluminum)
1	1	1	1	1	H950-LB	Logo Frame Panel (plastic)
					H950-PA	5¼ in. Bezel Cover Panel
5	5	5	6		H950-QA	10½ in. Bezel Cover Panel
1	1	1	1	1	H950-SA	Filter (for H952-BA or H952-CA)
2	2	2			H952-AA	End Panel (require 2 per cabinet)
1	1	1			H952-BA	Stabilizer Feet (pair)
1	1	1	1	1	H952-CA	Fan Assembly (top mounted) (115 Vac)
					H952-CB	Fan Assembly (top mounted) (230 Vac)
			1	1	H952-GA	Filter Strip Set (front and rear) (joining two cabinets)
					H950-G	Cabinet Table
					H952-HA	Free-Standing Table
1	1	1			74-06782	Kickplate (use with H952-BA)
			1	1	74-06793	Kickplate
					12-09154	Drawer Mounting Slides
					12-09703	Drawer Mounting Slides (tilt)
					861-A	Power Controller (90—130 Vac, two phase)
1					861-B	Power Controller (180—270 Vac, single phase)
	1	1		1	861-C	Power Controller (90—135 Vac, single phase)
					861-D	Power Controller (90—130 Vac, three phase)
					861-E	Power Controller (180—270 Vac, three phase)

Table 2
Standard Cabinet Frame H950-AA and Accessories

Figure 2 Item	Part No.	Description
1	H950-DA	Mounting Panel Door Frame (right hanging)
1	H950-EA	Mounting Panel Door Frame (left hanging)
2	H950-BA	Door, Front or Rear Mounting (right hanging)
2	H950-CA	Door, Front or Rear Mounting (left hanging)
3	H950-SA	Air Filter
4	74-06706	Fan, Cover Plate
5	H952-CA	Fan Assembly (115 Vac)
5	H952-CB	Fan Assembly (230 Vac)
6	H952-AA	End Panel (left or right side)
7	H952GA	Filler Strip Set (front or rear)
8	H950-LB	Frame Panel (plastic)
8	H950-LA	Frame Panel (aluminum)
9	H950-PA	Bezel Cover Panel, 5.25 in. (13.34 cm)
10	H950-QA	Bezel Cover Panel, 10.50 in. (26.67 cm)
11	H950-G	Tabletop Assembly
12	H950-HA	Short Door, covers 21.00 in. (53.34 cm) mounting space
12	H950-HC	Short Door, covers 26.25 in. (66.68 cm) mounting space
12	H950-HD	Short Door, covers 31.50 in. (80.01 cm) mounting space
12	H950-HF	Short Door, covers 42.00 in. (106.68 cm) mounting space
12	H950-HG	Short Door, covers 47.25 in. (102.02 cm) mounting space
12	H950-HH	Short Door, covers 52.50 in. (133.35 cm) mounting space
12	H950-HK	Short Door, covers 63.00 in. (160.02 cm) mounting space
13	H952-FA	Leveler Set (4)
14	74-06782	Kickplate (used with H952-BA stabilizer feet)
14	74-06793	Kickplate
15	H952-BA	Stabilizer Feet (pair)
16	H952-EA	Caster Set (4)
17	74-11606	Bottom Screen
18	H950-AA	Frame, 19.00 in. (48.26 cm) wide, 69.00 in. (175.26 cm) high, 25.00 in. (63.50 cm) deep

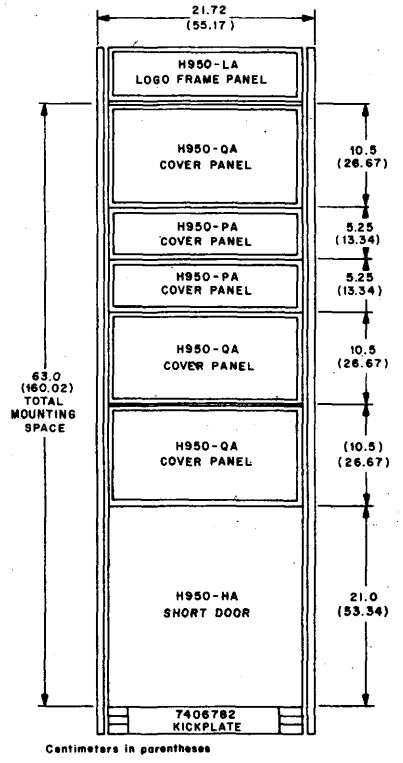


Figure 1. Typical Standard Cabinet Front Cover Panel and Short Door Configuration

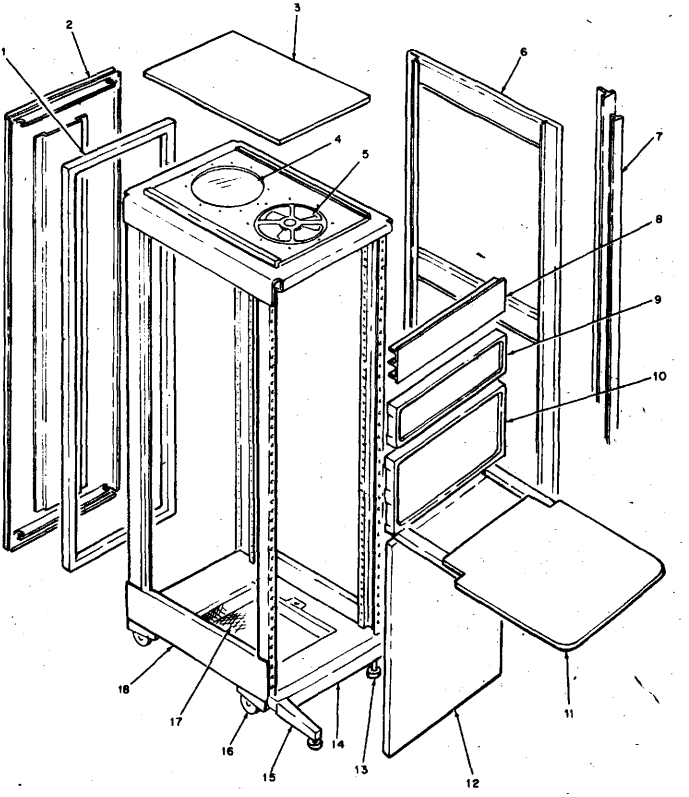
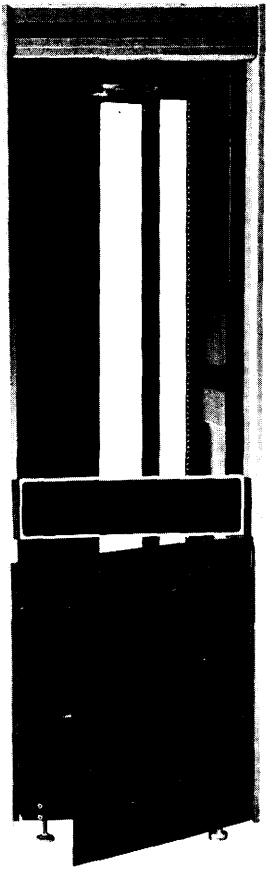
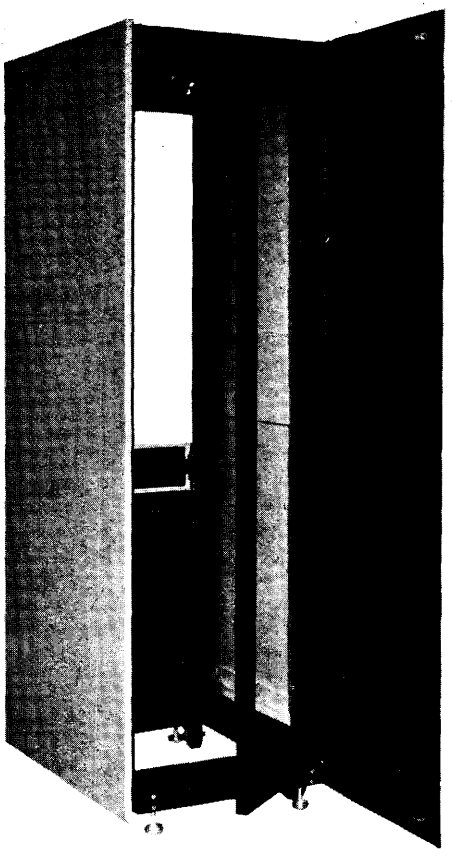


Figure 2. H950-AA Standard Cabinet Frame and Accessories



Front view of H950-AA frame with optional side panels, logo, fan, etc.



Rear view of H950-AA frame.

How to Order a Standard Size Cabinet Assembly

Determine if one of the five basic cabinet assembly configurations (H960-BC, H960-BD, H960-CA, H961-A, H961-AA, will fulfill your requirements by referring to Table 1 and comparing the items that comprise each configuration.

If one of these basic configurations will satisfy your requirements, you can order the completely assembled cabinet by specifying that cabinet assembly number; e.g., H960-BC, H960-BD, H960-CA, H961-A, H961-AA. In addition to the accessories included in the eight configurations, optional accessories are available, e.g., short doors, a cabinet table, and drawer mounting slides.

If one of the basic configurations will not fulfill your requirements, you can "build up" and order a cabinet that will suit your specific requirements by ordering an H950-AA standard size frame and the accessories (by specific part numbers) that you require. The frame and the accessories that you select will be shipped completely assembled.

Short Size Cabinet and Accessories

The short size cabinet (H967-BA or H967-BB) is 50.0 in. (127.0 cm) tall and provides 42.0 in. (106.7 cm) of vertical mounting space at the front; an additional 42.0 in. (106.7 cm) of mounting space is available at the rear of the cabinet.

Figure 3 illustrates a typically configured short size cabinet front. Figure 4 illustrates the installation of typical accessories on a short size cabinet frame, and Table 4 identifies and describes these accessories. Complete descriptions of the H957-AA Cabinet Frame and the accessories for short size cabinet frames are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

This short size cabinet is configured around the basic H957-AA Cabinet Frame. These cabinet frames are drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings to accommodate equipment, panels, or devices that are designed to mount in standard 19-in. (48.26-cm) electronics cabinets or racks. Optional accessories as specified by the customer can be added; table 3 lists the parts and accessories included. Table 3 also lists the optional accessories that are available for use with these cabinets. All cabinets are completely assembled before shipment.

Table 3
Short Cabinet, H967-BA and H967-BB

Cabinet Assembly				
H967-BB	H967-BA	Catalog No.	Description
1	1	H957-AA	Cabinet Frame, 19 in. wide, 47-8/16 in. high, 25 in. deep
1	1	H957-BA	Full Door (RH) (rear mounting)
		H957-CA	Full Door (LH) (rear mounting)
1	1	H957-DA	Mounting Panel Door Frame (RH)
		H952-HA	Free-Standing Table
		H970-BA	Free-Standing Table
		H970-CA	Free-Standing Table
		H950-HA	Short Door (covers 21 in. mounting space)
		H950-HC	Short Door (covers 26¼ in. mounting space)
		H950-HD	Short Door (covers 31½ in. mounting space)
		H950-HF	Short Door (covers 42 in. mounting space)
		H950-JA	Short Door (covers 21 in. mounting space) (used with H952-BA installed)
		H950-PA	Bezel Cover Panel, 5¼ in.
		H950-QA	Bezel Cover Panel, 10½ in.
1	1	H952-BA	Stabilizer Feet (pair)
		H950-G	Cabinet Table
1	1	H957-FA	End Panel (R end)
1	1	H957-FB	End Panel (L end)
		H957-GA	Filler Strip Set (top, front, and rear) (joining two cabinets)
1	1	H957-HA	Fan Assembly (front or rear mounting)
		H957-JA	Bottom Cover Plate
1	1	H957-LA	Logo Frame Panel
1	1	H957-SA	Filter (for H957-HA)
1	1	74-06782	Kickplate (use with H952-BA)
		74-06793	Kickplate
		12-09154	Drawer Mounting Slides
		12-09703	Drawer Mounting Slides (tilt)
		861-A	Power Controller (90—130 Vac, two phase)
1		861-B	Power Controller (180—270 Vac, single phase)
	1	861-C	Power Controller (90—135 Vac, single phase)
		861-D	Power Controller (90—130 Vac, three phase)
		861-E	Power Controller (180—270 Vac, three phase)

Table 4
Short Size Cabinet Frame H957-AA and Accessories

Fig. 4 Item	Part No.	Description
1	H957-BA	Full Rear Door (right hanging)
1	H957-CA	Full Rear Door (left hanging)
2	H957-SA	Air Filter
3	H957-DA	Mounting Panel Door Frame (right hanging)
3	H957-EA	Mounting Panel Door Frame (left hanging)
4	H957-HA	Fan Assembly
5	H957-FA	End Panel (right hanging)
5	H957-FB	End Panel (left hanging)
6	H957-GA	Filler Strip Set (top, front, and rear)
7	H957-LA	Logo Frame Panel (plastic)
8	H950-PA	Bezel Cover Panel, 5.25 in. (13.34 cm)
9	H950-QA	Bezel Cover Panel, 10.50 in. (26.67 cm)
10	H950-HA	Short Door, covers 21.00 in. (53.34 cm) mounting space
10	H950-HC	Short Door, covers 26.25 in. (66.68 cm) mounting space
10	H950-HD	Short Door, covers 31.50 in. (80.01 cm) mounting space
11	H952-BA	Stabilizer Feet (pair)
12	74-06782	Kickplate (used with H952-BA Stabilizer Feet)
12	74-06793	Kickplate
13	H952-EA	Caster Set (4)
14	H957-AA	Frame, 19.00 in. (48.26 cm) wide, 47.50 in. (120.65 cm) high, 25.00 in. (63.50 cm) deep

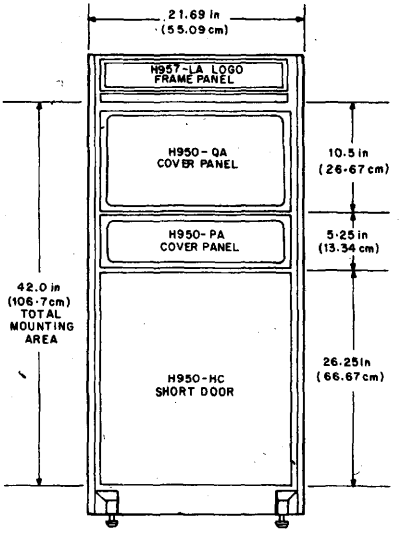


Figure 3. Typical Short Cabinet Front Cover Panel and Short Door Configuration

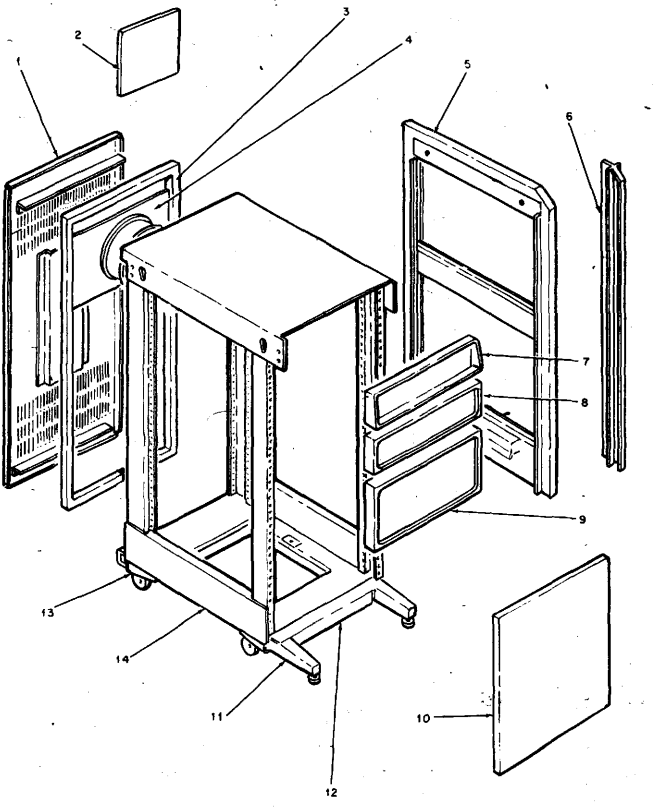


Figure 4. H957-AA Short Cabinet Frame and Accessories

How to Order a Short Size Cabinet Assembly

Determine if the basic cabinet assembly configuration (H967-BA or H967-BB) will fulfill your requirements by referring to Table 3 and comparing the items that comprise them.

If the basic configuration will satisfy your requirements, you can order the completely assembled cabinet by specifying that cabinet assembly number (H967-BA or -BB). In addition to the accessories included, optional accessories are available, e.g., short doors, a cabinet table, drawer mounting slides, etc.

If the basic configuration will not fulfill your requirements, you can "build up" and order a completely assembled cabinet that will suit your specific requirements by ordering an H957-AA short size frame and the accessories (by specific part numbers) that you require. The frame and the accessories that you select will be shipped completely assembled.

Cabinet Hardware

Digital Equipment Corporation offers a variety of cabinet hardware which can be used on existing system cabinets or installed on the basic standard size or short size cabinet configurations. This hardware can also be purchased as replacement parts.

TINNERMAN CLIP NUT AND PHILLIPS PAN HEAD SCREW COLLECTION—90-07786

This is a bagged collection of fifty 10-32 Tinnerman clip nuts, fifty 10-32 × 5/8-in. (1.5875-cm) Phillips pan head screws, and fifty size 10 lock washers.

LATCH—12-09224

The 12-09224 Latch is used to secure H950-PA or H950-QA Bezel Cover Panels to the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

THICK LATCH—12-11386

The 12-11386 Thick Latch is used to secure H950-PA or H950-QA Bezel Cover Panels to the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

SPACER—74-07789

The 74-07789 Spacer is used to maintain alignment of H950-PA or H950-QA Bezel Cover Panels on the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

KEY-LOCK STRIKE PLATE—74-09819

The 74-09819 Key-Lock Strike Plate is used on a short size H957-AA Cabinet Frame as a strike plate for the key lock on the H957-BA or H957-CA Full Door when an H957-DA or H957-EA Mounting Panel Door Frame is not installed. The 74-09819 can be mounted on the left vertical cabinet frame rail to accommodate a right-hanging full door, or it can be mounted on the right vertical rail to accommodate a left-hanging full door. All the required mounting hardware is supplied with the 74-09819 Key-Lock Strike Plate.

CABINET DOOR GROUND STRAP—90-06990

The 90-06990 Cabinet Door Ground Strap is used to electrically connect the cabinet door to the cabinet frame to ensure that the cabinet door is not isolated from earth ground. The cabinet door should be connected to earth ground to prevent operating personnel from electrical shock if a short circuit should occur in the logic system.

The 90-06990 Cabinet Door Ground Strap is a braided-copper bonding jumper; it is 4.875 in. (12.383 cm) long and has a terminal on each end. Each terminal is equipped with a hole sized to accept a No. 10 screw.

One ground strap terminal should be secured to the cabinet frame, at the door hinge side, with a No. 10 screw and nut, and the other terminal should be secured to the cabinet door with a No. 10 screw and nut.

CABINET FRAME GROUND STRAP—90-08887

The 90-08887 Cabinet Frame Ground Strap is used to electrically connect one cabinet frame to another cabinet frame to continue the common earth ground for the logic system cabinets.

The 90-08887 Cabinet Frame Ground Strap is a braided-copper bonding jumper; it is 11.00 in. (27.94 cm) long and has a terminal on each end. Each terminal is equipped with a hole sized to fit over an 0.313-in. (0.794-cm) diameter stud.

Each H950-AA and H957-AA Cabinet Frame is equipped with two threaded (5/16-18) copper studs, one on each side, inside the cabinet near the bottom panel. The ground strap should be installed on the threaded copper studs of two adjacent cabinet frames and a 5/16-18 nut should be used to secure each ground strap terminal. Each cabinet in a logic system should be connected to its adjacent cabinets to form a continuous path to an earth ground.

GENERAL PURPOSE LOW PROFILE CABINET

SPECIFICATIONS

Dimensions

Width:	23.50 inches (67.77 cm)
Depth:	28.06 inches (71.27 cm)
Height:	21.50 inches (54.73 cm)

Color:

Walnut grained top surface, beige side panels, chrome trim

Mounting Space

Width:	17.75 inches (45.08 cm)
Depth:	24.28 inches (61.67 cm)
Height:	17.56 inches (44.60 cm)

The H984-BA (115 VAC) and the H984-BB (230 VAC)are low profile cabinets equipped with a walnut grained, Formica covered top surface, and four ball type casters mounted on a supporting frame for ease of positioning on solid or carpeted surfaces. The cabinets are constructed of a beige steel enclosure and trimmed in flat black to make them compatible with the decor of the modern office or laboratory.

Each H984 provides mounting space for standard 19 inches (48.26 cm) panels or racks at both the front and rear of the unit. Two vertical angles at the front and rear opening of the enclosure contain pre-drilled holes at RETMA spacing. The angles can be laterally positioned within the cabinet to adjust for mounting units with varying depths. The right side of the steel enclosure contains ventilation ports to allow adequate cooling of the internal components.

A service leg with caster is located beneath the center of the unit and can be easily extended and retracted. The service leg provides stability to the cabinet when slide mounted chassis are withdrawn from the front of the cabinet. When not in use, the leg retracts into the channel.

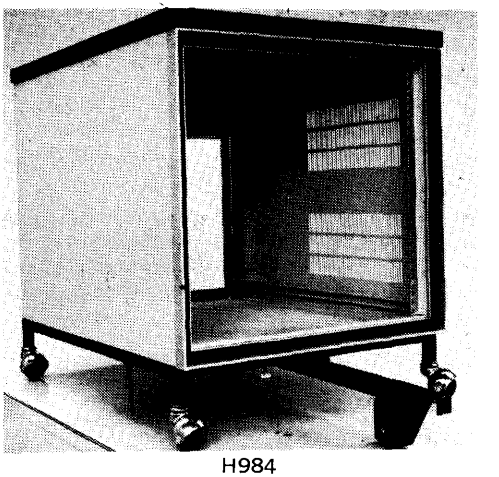
A 115 VAC or 230 VAC power control panel is supplied with the cabinet and is mounted at the top of the rear opening of the cabinet. The panel can be easily repositioned to accommodate internal chassis when required.

OPTIONAL EQUIPMENT

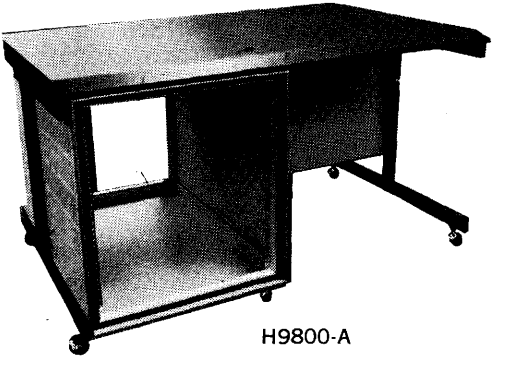
Fan Panel Assembly—A fan panel assembly with two enclosed rotary fans is available as an option and provides additional cooling for the electrical components in the cabinet. The assembly is pre-wired with a cord and male connector which can be inserted into one of the outlets on the power connector panel. The fan assembly is available for 115 VAC or 230 VAC. The panel is supplied with hardware for mounting.

Blank Connector Panel—The blank connector panel is designed to completely enclose the rear opening of the H984 when the blower fan assembly option is included. This provides a surface for mounting interface cable connectors or cable openings. The panel is supplied with hardware for mounting.

Description		Part No.
Low Profile Cabinet (115 VAC)		H984-BA
Low Profile Cabinet (230 VAC)		H984-BB
Optional Hardware		
Blower Fan	115 VAC	70-12438-0
	230 VAC	70-12438-1
Blank Connector Panel		74-17440
A flat black, plastic louvered cover panel 1.75 in. (4.45 cm) in height used to complete the covering at the front of the H984. The panel slots allow increased air flow through cabinet.		12-11474-0
A light grey blank metal cover panel, 3.5 in. (8.90 cm) in height used to complete the covering at the front of the cabinet. The color is the same as PDP-11/03 front panel and H984 cabinet.		H950-NC
A bracket set that attaches to the rear of the H909-C General Purpose logic enclosure and PDP-11/04,/34 enclosures when mounting in the H984.		74-16975



H984



H9800-A

H9800-A GENERAL PURPOSE SYSTEMS DESK

The H9800-A is a low-profile systems desk equipped with a walnut grained Formica top and color coordinated so as to fit into the modern office decor. The unit is equipped with six ball casters as standard equipment for easy positioning on carpeted surfaces.

The H9800-A is constructed of quality materials including a top constructed of 55 lb. particle board with a dark walnut Formica laminate. The "module" itself is constructed of 11 and 18 gauge steel with a maximum loading capacity of 400 lbs.

The H9800-A consists of a left-mounted rack enclosure offering 21" of usable height and 29" of usable depth in a standard 19" RETMA mount format. The right side offers knee space, a modesty panel, and a convenient work surface ideal for using terminals or typewriters.

SPECIFICATIONS

Dimensions (Overall):	48" W x 27.6" H x 32" D
Module Enclosure Mounting Space:	Standard 19" RETMA width 21" Usable height 29" Usable depth (adjustable)

MODULE SYSTEM ENCLOSURES AND EXPANSION MOUNTING BOXES

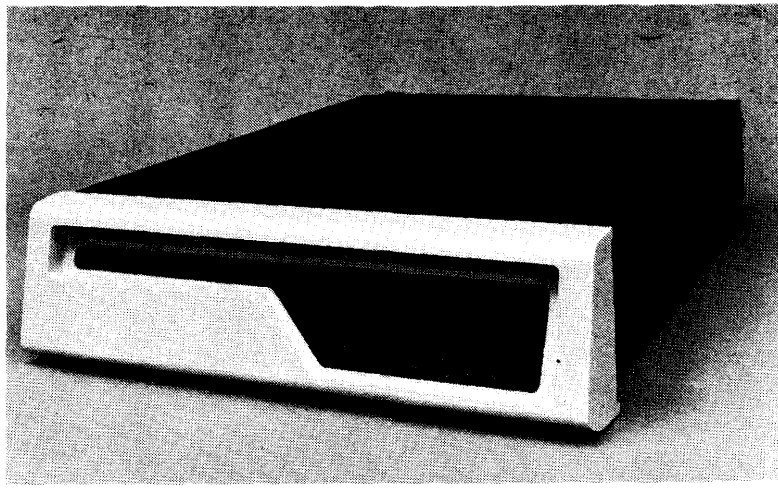
Module system enclosures are 19-in. (48.26-cm) rack-mountable boxes that provide mounting space for system units, module connector blocks, and power supplies. They provide enough space to accommodate medium-sized systems, and offer the convenience of easy access to the system for maintenance and testing.

Expansion mounting boxes are designed to house equipment that connects to the PDP-11 family UNIBUS. The boxes fit standard 19-in racks, and are suitable for memory, peripheral controllers, and standard or custom options. The several versions available offer great flexibility in layout plus easy access for maintenance and testing.

The following table summarizes the enclosures, expansion boxes, and associated hardware. Some of these are described in this section, and the rest are covered in the DIGITAL HARDWARE/ACCESSORIES Catalog which is available from Logic Products Sales Support, Accessories & Supplies Group, DIGITAL, Merrimack, NH 03054.

Part Number	Description
H909-C	General-purpose logic enclosure with PDP-11/34-type front panel. Described in this section.
H909-A	General-purpose logic enclosure with blank plastic front panel. Described in this section.
H909-BA	Same as H909-A, but includes H755 power supply and BC05H power control. Described in this section.
BA11-ES	Expansion mounting Box for UNIBUS equipment and H720-E Power Supply. Described in this section.
BA11-KE, -KF	Expansion mounting box for UNIBUS equipment. Has H765 Power System. The -KE is for 115V, and the -KF is for 230V. Described in this section.
K724	Interface shell for simple logic systems. Described in this section.
H035	Vertical system mounting frame that accommodates up to six 4-slot or three 9-slot system units. Accepts extended-length modules; mounts in 19-in. (48.26-cm) electronics rack. Described in HARDWARE/ACCESSORIES Catalog.
12-09154	Chassis slides that provide a 22-in. (55.88-cm) extension for a chassis mounted in an electronics rack. Non-tilting. Described in HARDWARE/ACCESSORIES Catalog.
12-09703	Chassis slides that provide a 22-in. (55.88-cm) extension for a chassis mounted in an electronics rack. Tilts 90 degrees up or down. Described in HARDWARE/ACCESSORIES Catalog.
12-10945	Chassis slides that provide a 19-in. (48.26-cm) extension for a chassis mounted in an electronics rack. The left side of these slides is comprised of two members, one of which can be removed (with the chassis remaining in the rack) to gain access to modules mounted in an H909 enclosure. Non-tilting. Described in HARDWARE/ACCESSORIES Catalog.

H909-C General Purpose Logic Enclosure



The H909-C is a general purpose logic box designed to accommodate any one of several different standard logic subsystems. In addition, with the use of compatible logic frames and connector blocks, it can house custom configured sub-assemblies. The box features a distinctive front panel that can be drilled for lights and switches as desired by the user. A fan is provided for cooling capability and ample room is reserved for power supply installation.

The box may be used either as a table-top enclosure or it can be rack mounted in any standard 19-inch cabinet. A card cage is included in the box to provide additional protection and support for the logic modules.

The H909-C has the capability to mount either one or two of the various standard four-by-six BB11 or DD11 type system units or one of the expanded nine-by-six slot system units. The frame castings associated with these system units, H033 and H034, respectively, can also be bolted in and used with the H8XX series of connector blocks for custom logic design requirements.

The H909-C will accommodate various configurations of single, double, quad, and hex size modules up to a maximum of nine hex size cards used with the appropriate system unit.

The following system units can be directly mounted in the H909-C without any additional hardware.

DDV11-B
H933 Series
BB11 Series
DD11 Series
Any DECkit11
H033 Frame Casting(s)
H034 Frame Casting

The following options are available for the H909-C:

12-10331-0	5" Blower Fan for power bay
H984-CA	Bracket set to mount H909-C in H984 cabinet. Attach to rear. Can also be used to mount a PDP-11/04 or /34.

SPECIFICATIONS

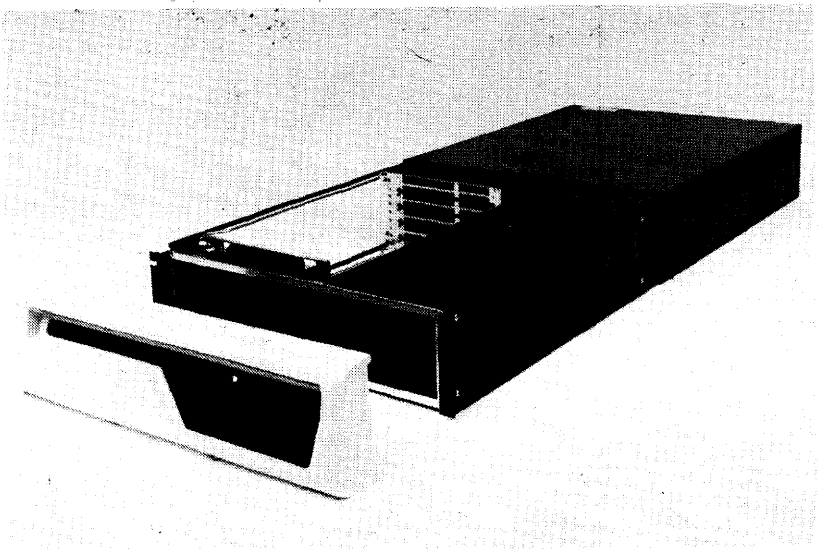
Width: 19 inches

Height: 5.25 inches

Depth: 24¾ inches, 27½ inches including bezel

Weight: 31 lbs.

Mounting space for power supplies: 5 x 6.25 x 20 inches



H909-C

NOTE

A detailed application note, "Assembling an LSI-11 Component System with a DDV11-B" describes the H909-C in depth. Order from Logic Products Sales Support, Accessories & Supplies Group, DIGITAL, MK1-2/E13, Merrimack, NH 03054.

H909-A General Purpose Logic Box

The H909-A General Purpose Logic Box is an enclosure designed to accommodate custom logic subsystems and power supplies and offer the convenience of easy access to the system for maintenance and testing. The box can be used either as a tabletop logic enclosure or, when equipped with optional chassis slides, as a rack mountable unit in any standard 19-inch cabinet. Included with the basic chassis is a top cover, side cover, card guides, cooling fan, cable restraints, and a front bezel.

Additional hardware is available to further increase the versatility of this box: chassis slides, power supply, and a choice of either a nine-slot system unit casting, a nine-slot system unit casting with connector blocks, or a nine-slot prewired unit with UNIBUS busing. These latter items utilize DEC connector blocks (e.g., H863) which, in turn, accommodate single-height through hex-height logic modules. However, the user can mount most any type of logic connector block that meets the dimensions of the H909-A.

Specifications

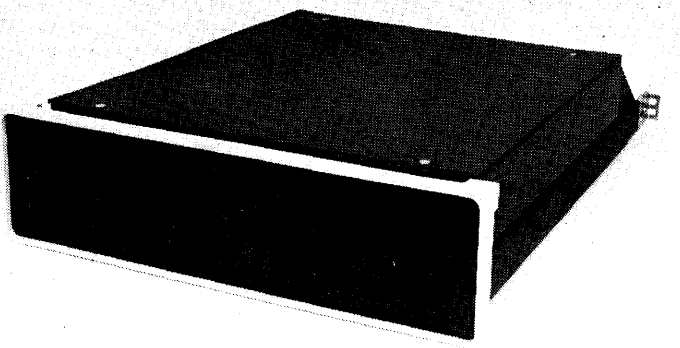
Width: 19 in. (48.26 cm)
Depth: 21 in. (53.34 cm)
Height: 5.25 in. (13.33 cm)
Color: Lamp black

Mounting space available for power supply:	Width —6.25 in. (15.87 cm) Depth —16 in. (40.64 cm) Height—4.75 in. (12.06 cm)

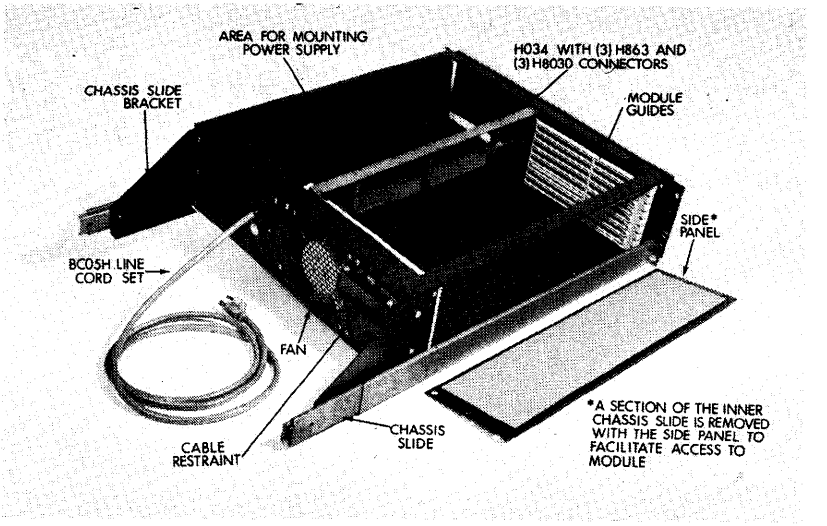
Optional Hardware	DEC Part No.
Chassis slides	12-10945
Required brackets for chassis slides	74-09459 (left) 74-09449 (right)
Nine-slot casting	H034
Nine-slot casting with six H863 and three H8030 Connector Blocks	H934-CB
Nine-slot unit with UNIBUS busing	BB11-B
Power Supply, +5 V @ 7 A (mounts on H034 casting, not included)	H726-B

H909-BA General Purpose Logic Box

The H909-BA General Purpose Logic Box is the same as the H909-A except that it is equipped with an H755 Power Suppy and BC05H Power Control. The H755 provides +15 Vdc @ 2 A, −15 Vdc @ 2 A, and +5 Vdc @ 13 A. The BC05H consists of a line cord and circuit breaker.



H909-A


AREA FOR MOUNTING POWER SUPPLY
H034 WITH (3) H863 AND (3) H8030 CONNECTORS
CHASSIS SLIDE BRACKET
MODULE GUIDES
SIDE* PANEL
BC05H LINE CORD SET
FAN
CABLE RESTRAINT
CHASSIS SLIDE
*A SECTION OF THE INNER CHASSIS SLIDE IS REMOVED WITH THE SIDE PANEL TO FACILITATE ACCESS TO MODULE

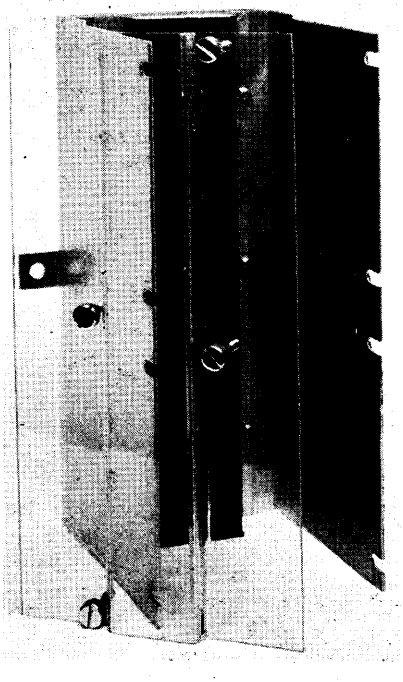
H909-A

K724 INTERFACE SHELL

The K724 Interface Shell provides the connectors and the mechanical support for self-contained interface modules K650, K652, and K658. Up to two K650, K652, or K658 modules may be installed, with eight module sockets remaining for decoding or gating modules. The limit of two DC Driver modules is due to the fact that they cannot be reversed in their connector sockets.

Convenient wiring channels are obtained between units if they are mounted on 12" centers vertically and 6" centers horizontally. This way a total of up to 32 input converters and 16 output converters fit in one square foot of panel space, along with up to 16 logic modules.

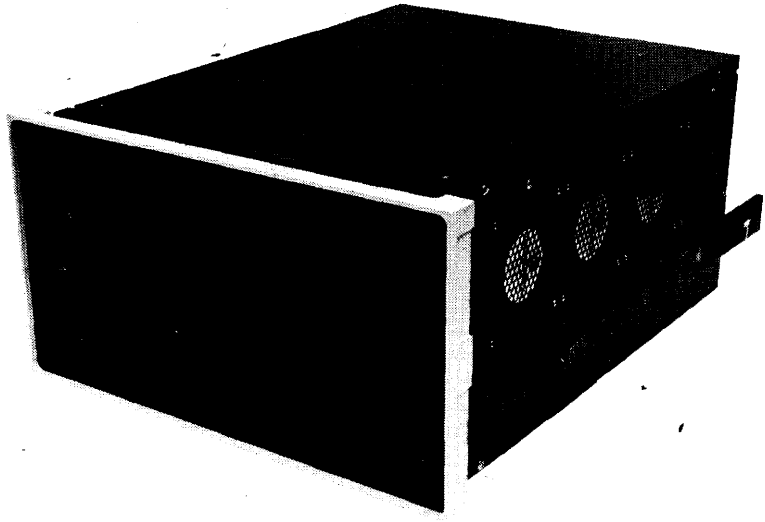
The K724 provides only logic power and ground connections between all but two sockets. It is primarily intended for very simple logic systems or for large systems where all input and output logic levels are connected to a separate logic unit by connector cables.



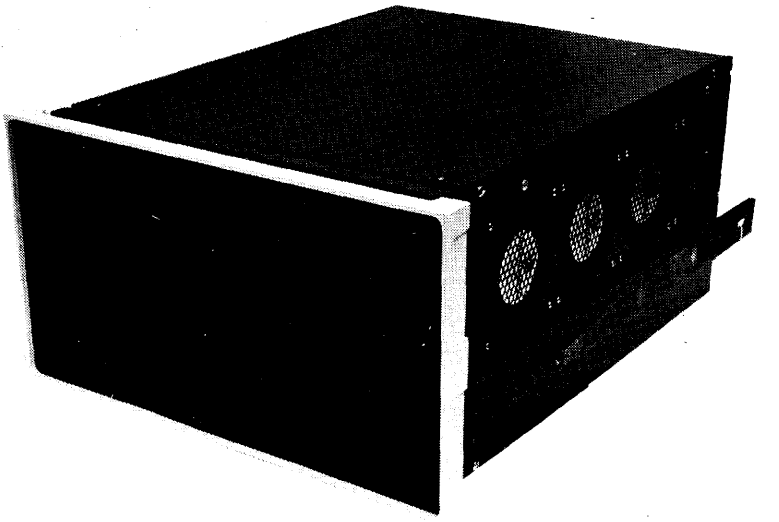
EXPANSION MOUNTING BOX — BA11-ES

The BA11-ES Expansion Mounting Box is a steel enclosure that is designed to house up to six four-slot or three nine-slot system units and an H720-E Power Supply. The BA11-ES enclosure consists of a chassis with brackets for mounting the system units and power supply; four side-mounted fans for forced air cooling; a removable top cover; two 12-09703 Tilting Chassis Slides; and an H950-QA Cover Panel. Included with the mounting box is an 8.5-ft. external I/O UNIBUS flat cable (BC11A-8F) used with PDP-11 Systems. An Internal power cable is contained within the box; the power cable distributes dc power and power signals from the power supply to each of the BB11 System Units installed. An access hole at the rear of the box provides clearance for the receptacles and controls on the H720-E Power Supply. The BA11-ES is 16.75W by 23.25D by 10.50"H, excluding the cover panel and slides.

The BA11-ES can be installed in any electronics cabinet or rack equipped with 19" mounting rails (front and rear) drilled at standard EIA spacings. The BA11-ES attaches to the cabinet frame by the two tilt slides mounted on each side of the unit. The tilt slides enable the unit to be pulled from the cabinet and tilted to facilitate servicing the system units or power supply.



BA11-ES



BA11-KE
BA11-KF

EXPANSION MOUNTING BOX — BA11-KE, BA11-KF

The BA11-KE and -KF Expansion Mounting Boxes are steel enclosures designed to house up to five single system units or the equivalent in a mix of single and double system units. Up to 16 hex and 6 quad module circuit boards could be accommodated. The H765 power system is included, which supplies multiple voltages to the circuit boards and can deliver up to 660 watts dc. The BA11-KE is for 115V operation, while the -KF is for 230V. Otherwise, the two are identical.

The BA11-KE and -KF chassis are 17.12"W by 25"D by 10.44"H with slides and power system but without cover panel. They can be installed in any electronics cabinet or rack equipped with 19" mounting rails (front and rear) drilled at standard EIA spacings. The units attach to the cabinet frame by the two tilt slides (included) which allow horizontal, 45°, and 90° positions (with front panel facing up). An H950-QA Cover Panel and UNIBUS cable are also included. The units are Underwriters Laboratories (UL) listed.

The H765 Power System contains two fans which also cool the modules by drawing air from front to rear. The entire Power System can be swung away from the main chassis for maintenance. Power outputs, through individual regulator modules are as follows:

two H744 regulators	+5V @25A (each)
one H745 regulator	−15V @10A
one H745 regulator	+20V @ 8A −5V @ 1A plus the current from the +20V output up to a total of 8A for both
one 54-11086 regulator	+15V @ 4A

POWER SUPPLIES, POWER CONTROLLERS, AND STEP-DOWN TRANSFORMERS

The electrical and mechanical features of a complete line of power supplies, power controllers, a step-down transformer, and power supply accessories are summarized in the following tables and paragraphs. These items are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. The following three paragraphs and tables summarize the power supplies according to their usual use. The fourth paragraph and table summarizes the power controllers and a step-down transformer. Power supply accessories are summarized in the fifth paragraph and table.

+5 Vdc POSITIVE LOGIC POWER SUPPLIES

These +5 Vdc positive logic power supplies are designed to provide V_{cc} (+5 Vdc) to the integrated circuits mounted on modules used in logic systems and interfaces. Many small systems and most interfaces comprise M-series gating, multiplexing, bus receivers, and bus transmitter modules that require only a V_{cc} power supply. The power supplies summarized in this table are ideal for these applications because of such features as overvoltage and short circuit protection, remote sensing, and input voltage ranges.

+5 Vdc Positive Logic Power Supplies

Part No.	Input Specs	Output Specs	Dimensions	Features
H716	120 Vac 240 Vac (47-63 Hz)	+5 Vdc @ 4.0 A, 3% regulation −15 Vdc @ 1.5 A, 5% regulation	5.25 in. long × 4.125 in. high × 12.00 in. deep (13.34 × 10.48 × 30.48 cm)	Floating output Short circuit proof Overvoltage protection for +5 Vdc output
H726-B	120/240 Vac (47-500 Hz)	+5 Vdc @ 7.0 A, 1% regulation	16.50 in. long × 2.23 in. high × 6.25 in. deep (41.91 × 5.66 × 15.88 cm)	Floating output Short circuit proof Overvoltage protection

SYSTEM POWER SUPPLIES

System power supplies are designed to provide V_{cc} (+5 Vdc) and reference voltages to an entire system or to a large interface when spare power is not available from the system supply. The power supplies summarized in this table are ideal for these applications because of their high current output capabilities and voltage output ranges.

System Power Supplies

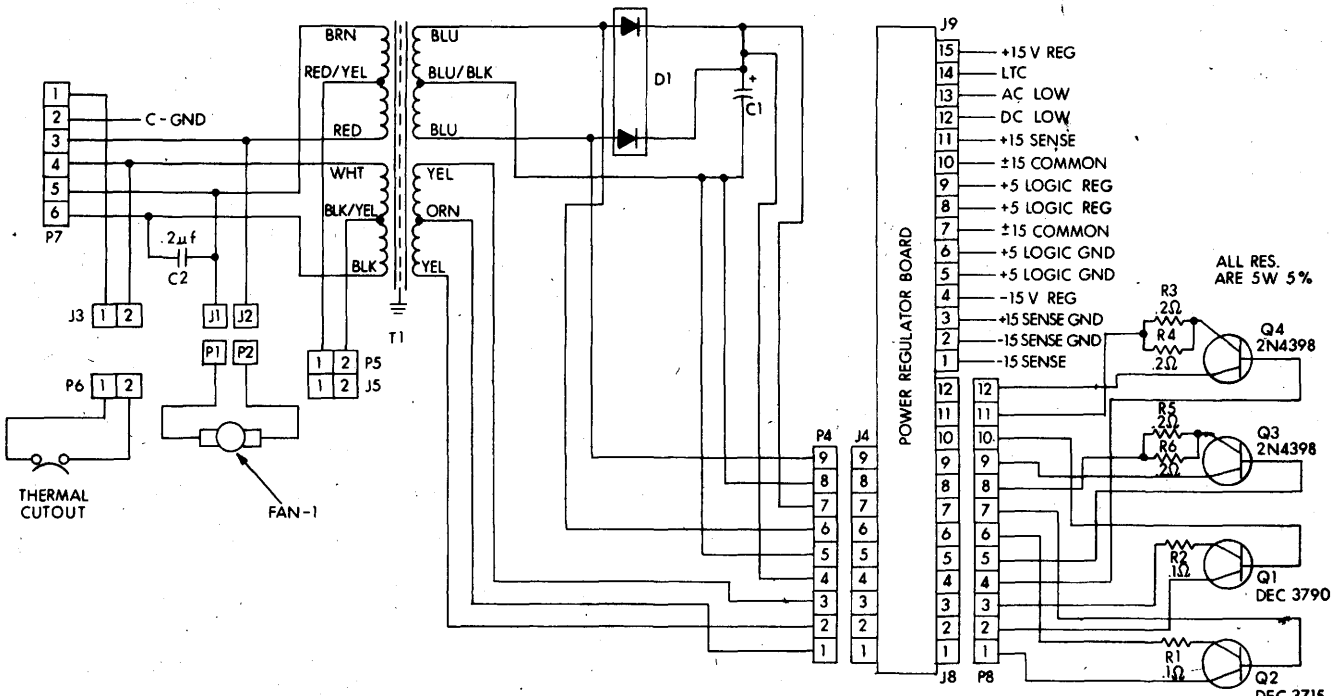
Part No.	Input Specs	Output Specs	Features
H720-E (BA11-ES Mounting Box)	120 Vac, 47-63 Hz	+5 V @ 22 A −15 V @ 10 A +8 V (avg) @ 1.5 A −22 V @ 1.5 A	Input frequency monitor Ac and dc low power detection Overvoltage and overcurrent protection
H720-F (Same as H720-E)	240 Vac 47-63 Hz	Same as H720-E	Same as H720-E
H740-D * 19-in. (48.26 cm) panel-mounted	115 Vac/ 230 Vac, 47-63 Hz	+5 V @ 17 A −15 V @ 5 A +15 V @ 1.0 A	Ac frequency monitor Ac and dc low voltage detection

* requires a BC05H for 115 Vac; a BC05J for 230 Vac

H755 POWER SUPPLY

The H755 is a versatile system power supply that provides outputs of +5 Vdc @ 13 A and ±15 Vdc @ 2 A. In addition, the H755 generates an AC LO output when the line voltage drops below 10 percent of its specified value; a DC LO output when dc out is insufficient to supply the load; and an LTC Line Frequency Signal which is available for time measurement purposes.

Included on the H755 are a fan and a thermostatic switch on the heat sink which provide overheat protection by opening the ac line at 220°F ±5°.



H755 POWER SUPPLY

SPECIFICATIONS

+5 Vdc: 4.75 to 5.25 Vdc at 0-13 A
Overvoltage protection at 7 Vdc maximum (5.7 Vdc minimum) is a crowbar with a fuse.
Current protection is a 15 A fuse and a 16 A foldback.
Regulation—line regulation of 1% or 50 mV, load regulation of 2% from no load to full load; maximum ripple is 50 mV P-P.

±15 Vdc: ±1% minimum at 2 A.
Current protection—3 A fuse and foldback.
Regulation—.03% and less than 5 mV P-P ripple.
Voltage sensing—remote, two wire per output.
Full load step change recovery: <50 μs.

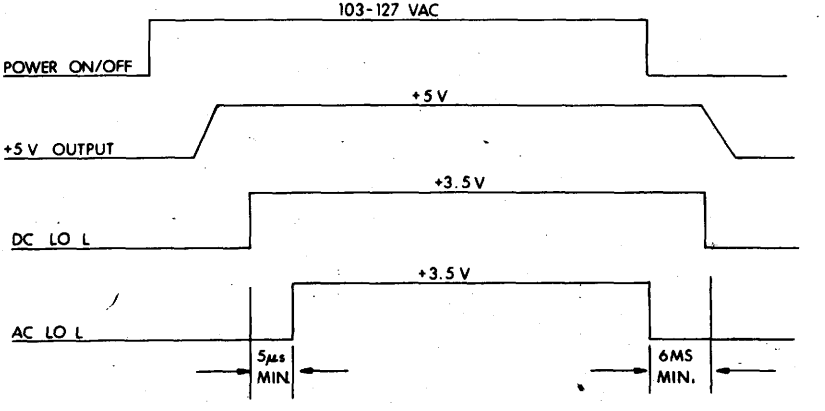
DC LO, AC LO: Rest state—25 μA (max) @ 3.5 V
Asserted—.8 V (max) @ 50 mA
Load Impedance—390Ω in parallel with .001 μf to +5 V

Line Frequency Signal (LTC): This signal is a square wave with a period at line frequency, a pulse height of 3.5 V, and a base line at .4 V maximum at 16 mA sink current.

Mechanical Dimensions

Length:	16¾ inches (42.54 cm)
Width:	4⅞ inches (12.26 cm)
Height:	5¼ inches (13.33 cm)

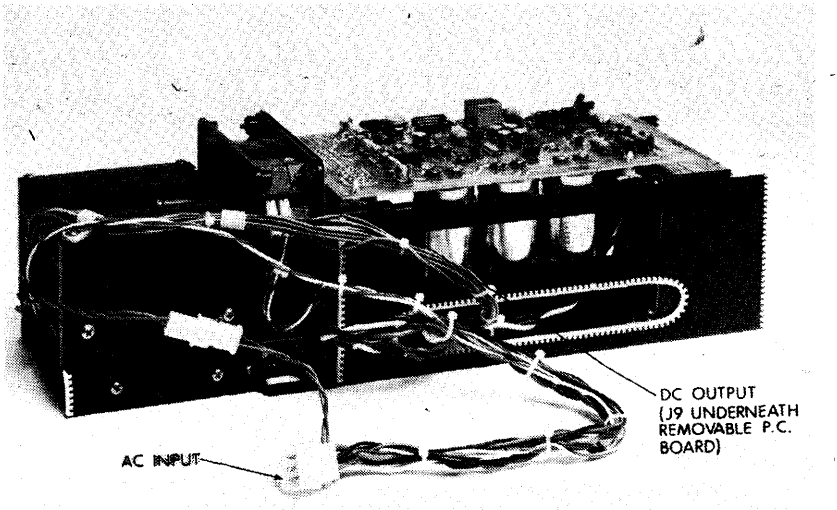
Signal Sequence



Related Products

DEC Part No.	Function
BC05H-6	Provides 115 Vac input to an H755; six-foot power cord
BC05J-6	Provides 230 Vac input to an H755; six-foot power cord
H909-A	Logic enclosure; accommodates an H755 supply and other logic.
12-09351-15	Cable Connector Housing (male); connects to DC output receptacle (J9)
12-09378-01	Pins for connector housing 12-09351-15

The above products are described elsewhere in this section.



H755

POWER CONTROLLER AND STEP-DOWN TRANSFORMER

A power controller and a power transformer are summarized in this table. The power controller is ideal for distributing ac power within a system; the power transformer is ideal for stepping down commercial power to 115 Vac for use within a system.

Power Controllers and Step-Down Transformer

Part No.	Input Specs	Output Specs	Features
861-A	90-130 Vac, 2 phase, 16 A/pole	90-130 Vac at 12 A (each ac outlet)	Local or remote control Four switched, dual receptacles
861-B	180-270 Vac, single phase, 16 A/pole	180-270 Vac at 12 A (each ac outlet)	Two unswitched, dual receptacles
861-C	90-130 Vac, single phase, 24 A/pole	90-130 Vac at 12 A (each ac outlet)	19-in. (48.26-cm) mounting-rail mounted
861-D	90-130 Vac, three phase, 24A	90-130 Vac at 12 A	19-in. mounting-rail mounted
861-E	180-270 Vac, three phase, 24A	180-270 Vac at 12 A	19-in. mounting-rail mounted
H722	115, 189, 200 217, 230, 245 Vac	115 Vac at 4.0 A	19-in. (48.26-cm) panel-mounted

Power Supply Accessories

Part No.	Use	Specifications
BC05H-6	Line set designed to connect 115 Vac input to Power Supply H740-D	115 Vac 6-ft. (1.8-m) power cord
BC05J-6	Line set designed to connect 230 Vac input to Power Supply H740-D	230 6-ft. (1.8-m) power cord
H322	Distribution panel designed to provide general-purpose signal, power, and ground distribution from one or more devices to one or more devices.	Fits 19-in. (48.26-cm) rack. Two 40-pin H854 and two 9-pin 12-09350-09 connectors and nine 10-screw terminal strips.

NINETEEN-INCH (48.26-cm) ELECTRONICS RACK MOUNTING PANELS

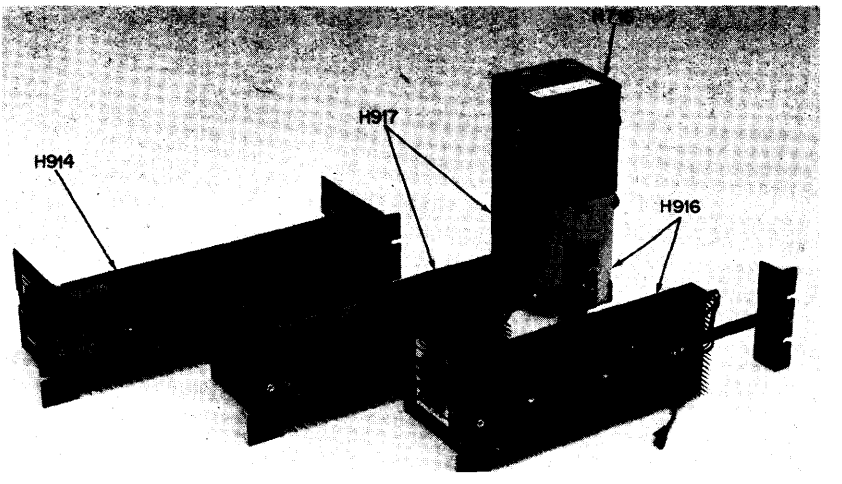
Mounting panels are designed to provide mounting space for module connector blocks and are usually used to expand a logic system. They are designed to mount in standard 19-in. (48.26-cm) electronics racks or cabinets.

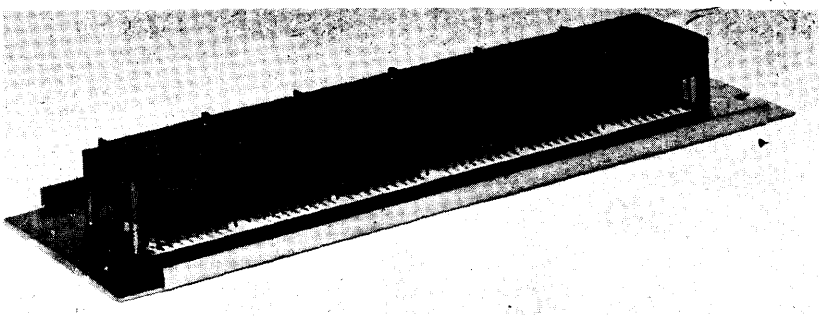
One (H020) of these mounting panels is a bare frame for mounting module connector blocks, some (H911-J, H911-K, H911-R, H911-S, K943-R, and K943-S) are equipped with connector blocks and are prebused for power and ground, others (H916 and H917) are equipped with connector blocks and a power supply and are prebused for power and ground, and one (H914) is a frame that is equipped with connector blocks but is not bused or wired for power or ground.

The following table summarizes the mounting panels; individual detailed descriptions of these mounting panels are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

19-In. Rack Mounting Panels

Part Number	Description
H020	Blank mounting panel that accommodates eight connector blocks; mounts in a standard 19-in. (48.26-cm) electronics rack.
H911-J	H020 equipped with eight H803 connector blocks to accommodate 64 single-height or 32 double-height, standard-length modules; bused for power and ground.
H911-K	Same as H911-J except wired and bused for power and ground.
H911-S	Same as H911-K except accommodates extended-length modules.
H914	H020 equipped with eight H808 connector blocks to accommodate 32 single-height or 16 double-height, standard-length modules.
H916	H020 equipped with an H716 Power Supply and six H803 connector blocks to accommodate 48 single-height or 24 double-height, standard-length modules; bused for power and ground.
K943-FP	H020 equipped with eight H800F connector blocks to accommodate 64 single-height or 32 double-height modules with contact fingers on only one side; bused for power and ground. Connector blocks equipped with solder-fork pins for 24 AWG wire. (Formerly designated K943-R.)
K943-WP	Same as K943-FP except equipped with eight H800W connector blocks that have wire wrap pins for 24 AWG wire. (Formerly designated K943-S.)



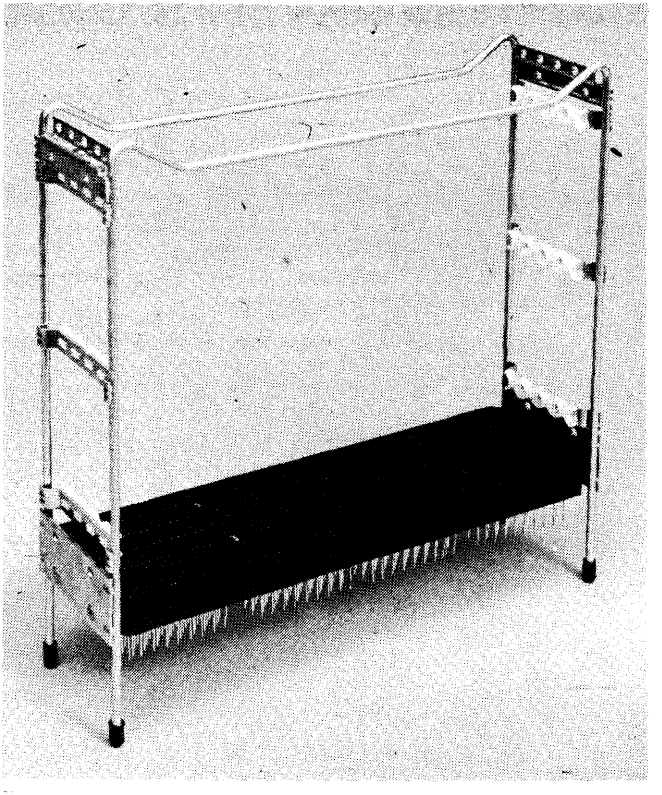


Typical System Unit Mounted On Casting Plate.

H9271 FOUR-BY-FOUR SLOT SYSTEM UNIT

The H9271 is a general purpose, four wide-by-quad height system unit mounted within an integral card cage assembly. Physically, the H9271 is identical to the H9270 LSI-11 backplane/card cage assembly with the exception that the LSI-11 etched board bus structure and power connector are omitted. This leaves the H9271 free to be used as a general purpose system unit for non-standard LSI-11 configurations or for virtually any other application requiring a compact, easily mountable logic rack. The system unit is manufactured and machined in such a way as to facilitate mounting in any plane or axes.

The H9271 consists of two H863 slotted connector blocks placed end to end for the mounting of four quad height, eight double height, or sixteen single height modules or any combination of the above totaling sixteen single slots. The blocks are mounted within a rectangular steel frame allowing easy access to the pin side of the blocks for wire wrapping, and the card cage surrounds the module insertion side of the logic rack.



H9271

NINE-SLOT SYSTEM UNITS

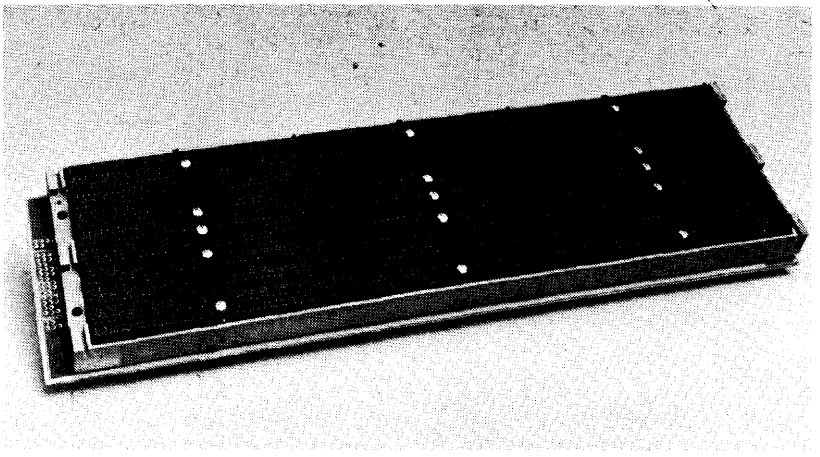
Nine-slot system units, like four-slot system units, are designed to provide mounting sockets (slots) for logic system modules. They, too, are designed to mount in the various module system enclosures offered by Digital Equipment Corporation. Nine-slot system units accept up to six four-slot and three one-slot module connector blocks mounted in three groups (one four-slot, one one-slot, and one four-slot module) mounted end-to-end. Since each of the module connector blocks used with these system units has two rows of slots, a fully complemented nine-slot system unit provides mounting facilities for 54 single-height, 27 double-height, or nine quad-height and 16 single- (or eight double-) height modules.

The following table summarizes three nine-slot system units; individual descriptions of these system units are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. Descriptions for the new LSI-11 compatible system unit and the DD11-D UNIBUS system unit follow this table.

Nine-Slot System Units

Part Number	Description
BB11-B	H034 equipped with six H863 and three H8030 connector blocks to accommodate 54 single-height modules, 27 double-height modules, or nine quad-height and eight double- (or 16 single-) height modules; prewired for UNIBUS, power, and ground. Used for general UNIBUS interfacing.
H034	Blank nine-slot system unit that can accommodate six H863 and three H8030 connector blocks; mounts in various module system enclosures.
H934-CB	Same as BB11-B except not prewired for UNIBUS, power, or ground.

DDV11-B NINE-BY-SIX SLOT LSI-11 SYSTEM UNIT



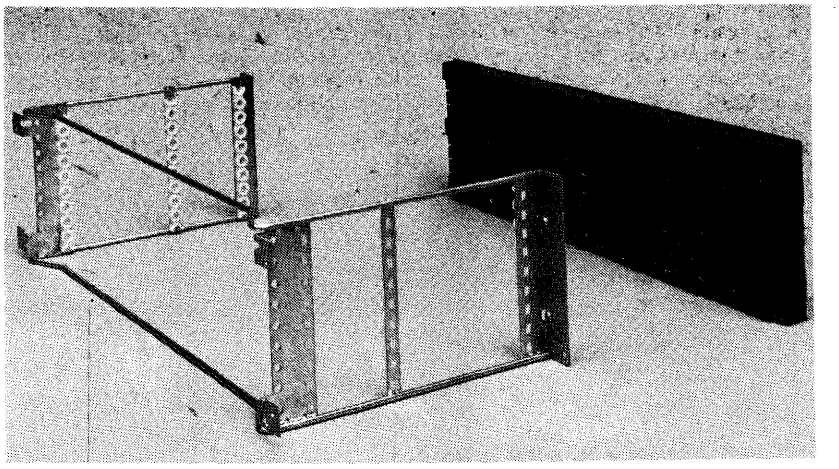
DDV11-B

The DDV11-B is an expanded version of the standard LSI-11 backplane for use when either more dedicated LSI-11 compatible logic space or non-LSI-11 compatible space for various other special purpose logic modules or both is required. A nine-by-four slot section (36 individual module slots) of this system unit is prebused specifically for LSI-11 bus signal, power and ground connections. The remaining nine-by-two slot section (18 slots) is provided with +5 Vdc and −12 Vdc power connections only; this leaves the remaining pins free for use with any special logic modules to be used in conjunction with the LSI-11 family of modules and bus requirements.

Physically, the DDV11-B consists of an H034 system unit mounting frame, six H863 and three H8030 connector blocks, and the etched board bus structure necessary for signal routing. The etched board completely overlays the entire pin side of all connector blocks and is recessed sufficiently to allow wire wrapping on those same pins with 30 AWG wire. Detailed descriptions of the frame and connector blocks are found in their respective sections of this Handbook and in the Hardware/Accessories Catalog.

An optional card cage, type H0341, is also available to provide protection against physical damage to modules and to serve as a logic card guide. This card cage completely surrounds the slot side of the system unit and is shown in the photograph.

A module slot assignment diagram is detailed in Figure 1 as viewed from the slot or module insertion side of the system unit.

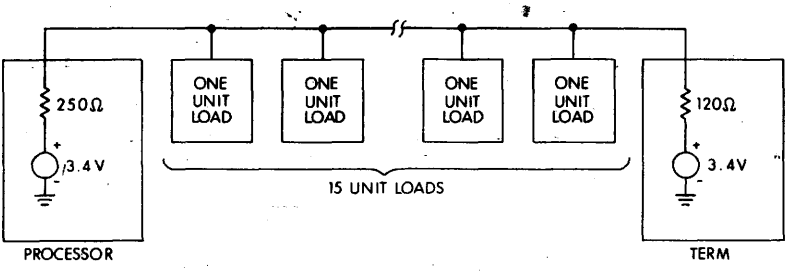


DDV11-B with H0341 Card Ass'y.

Rows E and F contain the 18 user-defined slots with power and ground connections provided.

Rows A, B, C, and D are dedicated to the LSI-11 bus. Any module meeting the LSI-11 bus specifications may be used in this portion of the DDV11-B. Slot number 1 in Rows A, B, C, and D is reserved for the LSI-11 processor module. The position numbers indicate the bus grant wiring scheme with respect to the processor module. The bus grant signals propagate through the slot locations in the position order shown in Figure 1 until they reach the requesting device. Any blank slots must be jumpered to provide bus grant signal continuity or it is recommended that unused locations occur only in the highest position numbered locations.

Bus Terminator—An additional 120 ohms of termination is required after six unit loads on each bus line as shown.



The TEV11 module provides the necessary 120 ohm bus terminators and should be installed into the next unused slot after the last module or into slot 9, row card C and D to maintain proper bus termination.

The backplane pin assignments of the DDV11-B are listed on Table 1.

If a system enclosure is required for the DDV11-B, an H909-C enclosure is available and was specifically designed for mounting the DDV11-B. The system unit has topped mounting holes to facilitate installation in the H909-C enclosure. The H909-C is described in this handbook and has space allocated for the installation of a power source.

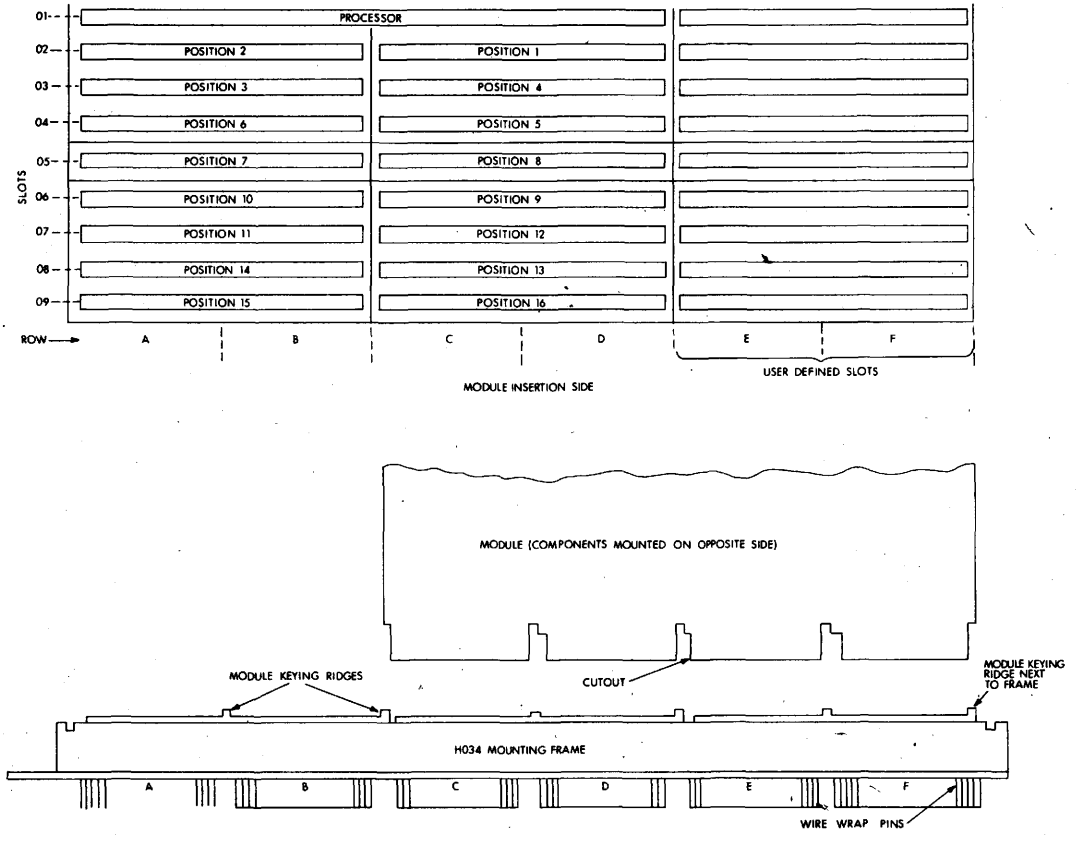


Figure 1 DDV11-B Module Slot Assignment Diagram

Table 1. DDV11-B Backplane Pin Assignments

SIDE	2	1	2	1	2	1	2	1
ROW	A & C	A & C	B & D	B & D	E	E	F	F
A	+5	BSPARE 1	+5	BDCOK H	+5	BLANK	+5	BLANK
B	−12	BSPARE 2	−12	BPOK H	−12	BLANK	−12	BLANK
C	GND	BAD 16	GND	SSPARE 4	GND	BLANK	GND	BLANK
D	+12	BAD 17	+12	SSPARE 5	BLANK	BLANK	BLANK	BLANK
E	BDOUT L	SSPARE 1	BDAL 2 L	SSPARE 6	BLANK	BLANK	BLANK	BLANK
F	BRPLY L	SSPARE 2	BDAL 3 L	SSPARE 7	BLANK	BLANK	BLANK	BLANK
H	BDIN L	SSPARE 3	BDAL 4 L	SSPARE 8	BLANK	BLANK	BLANK	BLANK
J	BSYNC L	GND	BDAL 5 L	GND	BLANK	BLANK	BLANK	BLANK
K	BWTBT L	MSPARE A	BDAL 6 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
L	BIRQ L	MSPARE A	BDAL 7 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
M	BIAK I L	GND	BDAL 8 L	GND	BLANK	BLANK	BLANK	BLANK
N	BIAK O L	BDMR L	BDAL 9 L	BSACK L	BLANK	BLANK	BLANK	BLANK
P	BBS7 L	BHALT L	BDAL 10 L	BSPARE 6	BLANK	BLANK	BLANK	BLANK
R	BDMG I L	BREF L	BDAL 11 L	BEVNT L	BLANK	BLANK	BLANK	BLANK
S	BDMG O L	PSPARE 3	BDAL 12 L	PSPARE 4	BLANK	BLANK	BLANK	BLANK
T	BINIT L	GND	BDAL 13 L	GND	BLANK	BLANK	BLANK	BLANK
U	BDAL 0 L	PSPARE 1	BDAL 14 L	PSPARE 2	BLANK	BLANK	BLANK	BLANK
V	BDAL 1 L	+5B	BDAL 15 L	+5	BLANK	BLANK	BLANK	BLANK

MODULE CONNECTOR BLOCKS

Digital Equipment Corporation offers a variety of module connector blocks to suit the requirements of almost any logic system. Most M-series systems use H803, 30 AWG, wire wrap blocks for modules with contact fingers on both sides. However, a system requiring 24 AWG interconnections, or using a large number of type 913 Patch Cords, might use H808 Connector Blocks because of the wider spacing of the connector pins. A system using K-series and certain A-series modules (i.e., contact fingers on only one side) can use H800 Connector Blocks. Connector blocks with slotted ends should generally be used in systems where the modules are quad height or larger. The following table summarizes the module connector blocks; individual detailed descriptions of these module connector blocks are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Module Connector Block Summary

Block Part No.	No. of Slots	Contacts Per Slot	No. of Contact Sides	Wire Wrap Pin Size	Bus Strip No.	Module Type	End
H800-W	8	18	1	24 AWG	932	All single- and double-height; single-sided	Unslotted
H802	1	18	1	24 AWG	932	All single-height single-sided	Unslotted
H803	8	36	2	30 AWG	933	All single- and double-height	Unslotted
H8030	2	36	2	30 AWG	933	All single- and double-height	Slotted
H807	1	36	2	30 AWG	933	All single-height	Unslotted
H808	4	36	2	24 AWG	939	All single- and double-height	Unslotted
H863	8	36	2	30 AWG	933	All single- and double-height	Slotted

BLANK MODULE BOARDS

Blank module boards provide a convenient method of breadboarding (mounting) experimental or prototype circuits, and they provide a low-cost method of producing limited runs of production modules with special circuitry. They are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy, blank module boards have etched and gold-plated contact fingers and all have handles attached. The attached handles are stamped with their Digital Equipment Corporation identification number (part number). The handles on copper-clad boards are attached with reusable nylon hardware. Blank handle 937, described elsewhere in this publication, is available; this blank handle can be user-titled and is, therefore, particularly useful for identifying user-etched, copper-clad module boards for limited production runs.

Blank module boards are available in three basic forms: plain, perforated, and copper-clad. The following table lists and describes the blank module boards that are available.

Plain blank module boards provide complete flexibility in the placement of components since they are not perforated (predrilled), and they permit easy changes to the circuitry since etching is not required. Component connections are made via hook-up wire. Plain blank boards are, therefore, ideal for experimental or prototype modules because they permit easy changes to the circuitry and nearly unlimited component placement, and yet they provide stability and security for the circuits and components. All sizes are available, and all have etched and gold-plated contact fingers.

Perforated blank module boards provide nearly the same advantage as plain blank module boards except they are predrilled with 0.052-in. (0.132-cm) diameter holes spaced 0.1 in. (0.254 cm) center-to-center horizontally and vertically. This eliminates the need for user drilling and only slightly reduces the choices of component placement. All sizes are available, and all have etched and gold-plated contact fingers.

Copper-clad blank module boards provide a method of producing limited runs of modules with special circuitry and components. A complete selection of copper-clad blank module boards is available: some may be user-etched on both sides and others may be user-etched on one side. All sizes are available, and all have etched and gold-plated contact fingers.

These blank module boards are described in the following table; each of these blank module boards is described in detail in the HARDWARE/ACCESSORIES CATALOG.

Blank Module Boards

Part No.	Type	Contact Fingers	Size	Description
W930	Plain	36	Single-height, extended length	Bare board with 36 feed-through eyelets. Printed circuit etching from the eyelets to the contact fingers.
W970	Plain	36	Single-height, standard length	Bare board with 36 plated-through holes in the printed circuit etching to the contact fingers.
W971	Plain	72	Double-height, standard length	Same as W970 except double-height and has 72 plated-through holes and two handles.
W972	Copper-clad	36	Single-height, standard length	Copper-clad on both sides.
W9720	Copper-clad	36	Single-height, extended length	Same as W972 except extended length.
W9721	Copper-clad	72	Double-height, extended length	Same as W9720 except double-height and has two attached handles.
W9722	Copper-clad	144	Quad-height, extended length	Same as W9720 except quad-height and has four attached handles.
W973	Copper-clad	72	Double-height, standard length	Same as W972 except double-height.
W974	Perforated	36	Single-height, standard length	Perforated board with 36 plated-through holes in the printed circuit etching to the contact fingers.
W975	Perforated	72	Double-height, standard length	Same as W974 except double-height and has 72 plated-through holes and two handles.

Blank Module Boards (Cont)

Part No.	Type	Contact Fingers	Size	Description
W990	Plain	18	Single-height, standard length	Bare board with 18 split-lug terminals. Printed circuit etching from the split-lugs to the contact fingers. This board has contact fingers on one side only.
W991	Plain	36	Double-height, standard length	Same as W990 except double-height and has 36 split-lug terminals and two handles.
W992	Copper-clad	18	Single-height, standard length	Same as W972 except copper-clad on one side only and has contact fingers on one side only.
W993	Copper-clad	36	Double-height, standard length	Same as W973 except copper-clad on one side only and has contact fingers on one side only.
W998	Perforated	18	Single-height, standard length	Same as W974 except has 18 plated-through holes and has contact fingers on one side only.
W999	Perforated	36	Double-height, standard length	Same as W975 except has 36 plated-through holes and has contact fingers on one side only.

COLLAGE MODULE BOARDS

Collage module boards provide a convenient, low-cost method of producing prototype or limited runs of production modules with special circuitry that uses 14- or 16-pin dual-in-line package (DIP) integrated circuits (ICs), with or without wire wrap sockets and/or solder sockets. Collage module boards are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy modules have +5 Vdc power and ground bused (printed circuit etch tracks) to plated-through holes at each IC location to facilitate connection of V_{cc} and ground to the appropriate IC pin.

These collage module boards are described in the following table; each of these collage module boards is described in detail in the HARDWARE/ACCESSORIES CATALOG.

Collage Module Boards

Part No.	Contact Fingers	Size	Description
W968	144	Quad-height, extended length	Accommodates up to seventy-two 14- or 16-pin DIP ICs with or without wire wrap sockets and/or solder sockets.
W969	72	Double-height, extended length	Same as W968 except accommodates 36 ICs.
W979	72	Double-height, standard length	Same as W968 except accommodates 18 ICs.

MODULE EXTENDER BOARDS

Module extender boards are usually used to extend system modules for test and/or maintenance. Module extender boards permit access to the system module circuits and components without breaking the electrical connections between the system module and the backplane or mounting panel wiring. Extended length module extender boards should be used when the system comprises extended length system modules. Double-height and quad-height module extender boards should be used when the system module to be extended is double or quad high; however, two single-height module extender boards could be used to extend a double-height system module, or two double-height (or four single-height) module extender boards could be used to extend a quad-height system module. The following table describes the module extender boards. The board contact fingers connect directly to the connector socket pins on a 1:1 basis except as noted in the "Description" column of the table.

Module Extender Boards

Part No.	Contact Fingers	Size	Description
W900	72	Double-height, extended length	Used in systems comprising extended length modules to extend a double-height, 72-pin module with +5 Vdc power at contact fingers AA2 and BA2 and with ground at contact fingers AC2, BC2, AT1, and BT1, i.e., most double-height M-series modules. This is a multilayer module: layer 2 is the ground plane and layer 3 is the +5 Vdc power plane.
W980	18	Single-height, standard length	Used in systems comprising standard length modules to extend a single-height, 18-pin (one side only) module, i.e., most A-, K-, and W-series modules. None of the contact fingers are interconnected.
W982	36	Single-height, standard length	Used in systems comprising standard length modules to extend a single-height, 36-pin module, i.e., single-height M-series modules. None of the contact fingers are interconnected.
W983	72	Double-height, standard length	Used in systems comprising standard length modules to extend a double-height, 72-pin module, i.e., double-height M-series modules. None of the contact fingers are interconnected.
W984	72	Double-height, extended length	The same as W983 except the W984 is an extended length module extender board and should be used to extend a system module located beside one, or between two, extended length modules.
W987	144	Quad-height, extended length	The same as W984 except the W987 is a quad-height module extender board and should be used to extend quad-height (144-pin) modules.

WIRE WRAPPABLE MODULE BOARDS

Wire wrappable modules provide a convenient, low-cost method of producing prototype or limited runs of production modules with special circuitry that utilizes, mainly, dual-in-line package (DIP) integrated circuits (ICs). They are completely compatible with the standard module mounting blocks summarized elsewhere in this production and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. This section describes the new additions to the wire wrap line: the W9500 series and the W9301 and W9302 modules. Further information regarding these new items can be obtained by contacting Logic Products Sales Support. Accessories & Supplies Group, DIGITAL, Merrimack, NH 03054.

In addition, a brief overview of DIGITAL's traditional wire wrappable modules is provided. These earlier boards are described in detail in the Hardware/Accessories Catalog published by DIGITAL.

W9500 SERIES

WIRE WRAPPABLE MODULES

DESCRIPTION

The W9500 series of wire wrappable modules enable a user to easily configure special interface logic for the LSI-11 computer systems and small peripheral controller (SPC) logic for the PDP-11 computer system. In addition, these modules are suitable for any system requirements and consists of double, quad, and hex height sizes. Each module is available with or without premounted Dual-In-Line packages (DIP) low profile socket.

The ten module types included in the W9500 series are listed with a description and preassigned power and ground pin connections in Table 1. Refer to the General Information section of this handbook for detailed information relating to module size dimension and edge connector pin coding.

The W9500 Series modules will accept a variety of IC package types and discrete components. The printed circuit on each board connects the appropriate edge connector pins to the Vcc plane on side 1 of the board and the ground plane (GND) on side 2. The remaining edge connector pins terminate to a double row of wire wrap pins for user designated functions. Each of the modules also includes a 40 pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire-wrap pins. The quad and hex height modules are provided with a space where a 40 pin cable connector (labelled J-2) can be inserted by the user. When a connector is not required, additional IC packages can be installed. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and prevent shorting of wire wrap pins.

The wire wrap pins and components are mounted on side 1 of each module. Rows of predrilled holes accept IC packages with pin spacings of 0.3 in. (0.76 cm) 0.4 in. (1.01 cm) and 0.6 in. (1.52 cm). Universal areas on the W9500 series modules are the areas which accept IC packages with standard pin spacings. These areas have four rows of predrilled holes spaced at 0.3, 0.4, and 0.6 inches. The W9500 hex height module also contains three areas which can accept IC packages with 0.3 and 0.4 inch spacing.

Table 1 W9500 Series Modules

Module Type	Description	Power & Ground Connections
W9500	Hex height, extended length, single width module with extractor bracket. No DIP sockets included. One 40 pin male cable connector mounted on board and space for additional 40 pin connector provided.	Vcc—AA2, BA2, CA2, DA2, EA2, FA2 GND—AT1, BT1, CT1, DT1, ET1, FT1, AC2, BC2, CC2, DC2, EC2, FC2
W9503	Same as W9500 except with 84 pre-mounted DIP sockets.	Same as W9500
W9501	Quad height, extended length, single width module with flip chip handles. No DIP sockets included. One 40 pin male cable connector premounted on board and space for additional 40 pin connector provided.	Vcc—AA2, BA2, CA2, DA2 GND—AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2
W9504	Same as W9501 except with 54 DIP sockets premounted.	Same as W9501
W9502	Double height, extended length, single width module with flip chip handles. No DIP sockets included. One 40 pin male cable connector premounted on board.	Vcc—AA2, BA2 GND—AT1, BT1, AC2, BC2
W9505	Same as W9502 except with 24 pre-mounted DIP sockets.	Same as W9502
W9511	Quad height, extended length, single width module with extractor handle. No DIP sockets included. One 40 pin male cable connector premounted on board and space for additional 40 pin connector provided.	Vcc—AA2, BA2, CA2, DA2 GND—AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2
W9514	Same as W9511 except with 58 pre-mounted DIP sockets.	Same as W9511
W9512	Double height, extended length, single width module with flip chip handle. No DIP sockets included. One 40 pin male connector pre-mounted on board.	Vcc—AA2, BA2 GND—AT1, BT1, AC2, BC2
W9515	Same as W9512 except with 25 pre-mounted DIP sockets.	Same as W9512

LSI-11 Compatible Modules

The LSI-11 compatible modules consist of quad height and double height modules. Two LSI-11 compatible modules are available without DIP sockets. The total IC compliment of 14 or 16 pin DIPS that can be installed are listed on Table 2. This table allows one pair of holes between each IC package for mounting additional decoupling capacitors.

Table 2 LSI-11 Compatible Modules (no sockets)

Module Type	IC Capacity (Total)			
	14 Pin	16 Pin	24 Pin	40 Pin
W9511	72	61	5	3
W9512	32	27	5	3

Two LSI-11 compatible modules are available with premounted 16 pin DIP sockets. One pair of holes is provided between each DIP socket for mounting additional decoupling capacitors. The total number of sockets mounted on the board is listed on Table 3.

Table 3

Module Type	16 Pin DIP Sockets
W9514	58
W9515	25

SPC Compatible Modules

The small peripheral controller (SPC) compatible modules consist of a hex height, quad height and double height boards.

Three boards are available without DIP sockets.

The total IC compliment of 14 or 16 pin DIP's is listed on Table 4. This table allows one pair of holes for mounting additional decoupling capacitors between each IC package.

Table 4 SPC Compatible Modules (no sockets)

Module Type	IC Capacity (Total)			
	14 Pin	16 Pin	24 Pin	40 Pin
W9500	128	114	10	6
W9501	72	61	5	3
W9502	40	38	5	3

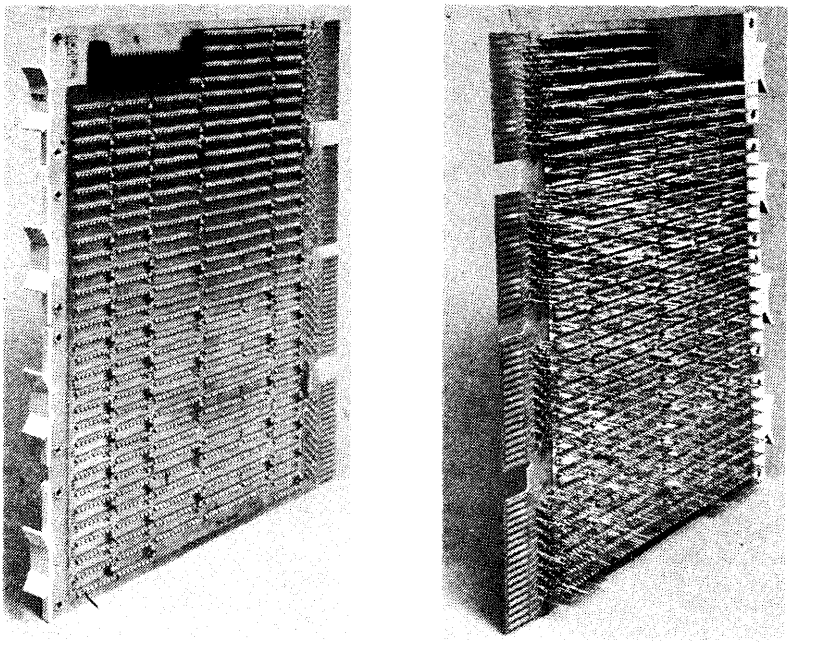
Three boards are available with premounted 16 pin DIP sockets. The total number of sockets mounted on the modules is listed on Table 5.

One pair of holes is allowed between each DIP socket and can be used to mount additional decoupling capacitors.

Table 5 SPC Compatible Modules (16 pin sockets)

Module Type	16 Pin DIP Sockets
W9503	84
W9504	54
W9505	24

W9301 HI-DENSITY WIRE WRAPPABLE MODULE



W9301

DESCRIPTION

The W9301 is a quad height, extended length, double wide, wire wrappable module suitable for user designed logic interface applications. The module accepts a variety of dual-in-line (DIP) integrated circuits (IC's) or discrete components which can be mounted to the module without the use of solder. The component or IC leads insert into specially designed socket terminals which have a wire wrap pin on the opposite end. The electrical interconnection of the wire wrap pins can be performed manually or by using automated wire wrapping techniques.

The W9301 board has four rows of 36 gold-plated contacts (18 contacts on each side of each row). Each contact is connected to a wire wrap pin by the board etch. A ground plane is etched on side 1 of the module and power (Vcc) plane is etched on side 2. Contact pin A2 of each of the four rows directly connects to the power plane, and contact pins C2 and T1 directly connect to the ground plane.

A total of 68 decoupling capacitors are provided premounted between Vcc and GND at each main IC location. The module occupies 2 slots of a standard DIGITAL system unit.

A 40 pin connector is mounted at the edge of the module to facilitate the attachment of a device cable assembly.

Wire Wrap Terminals
All wire-wrap terminals on side 2 of the module are located on a grid of 0.1 in. (0.254 cm) spacing to facilitate automatic point-to-point wire wrapping equipment. The connections to the pins are made using #30 gauge solid conductor insulated wire.

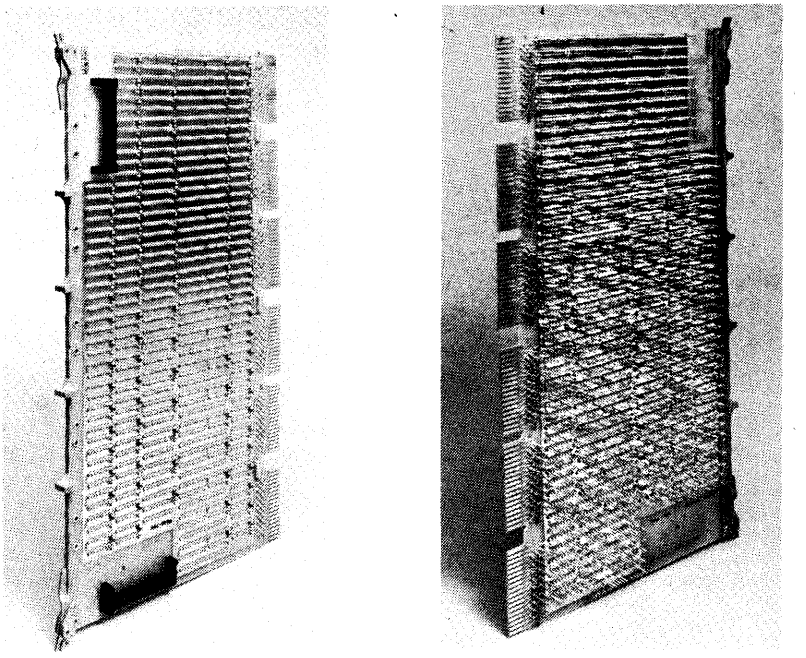
Total IC Complement
Up to 79 IC equivalents (14- or 16-pin DIP) can be mounted on the module. Areas are provided on the board for mounting DIP's with a center spacing of 0.3 in. (0.78 cm) 0.4 in. (1.0 cm) or 0.6 in. (1.5 cm). Table 1 lists the acceptable IC types and pin spacing.

Table 1 W9301 IC TYPES

Total Pins	Center Spacing (in.)
8, 14, 16, 18, 20	0.3
22	0.4
24, 28, 40	0.6

The W9301 module has three pin configuration areas assigned to 16-pin, 24 and 40 pin IC's. The 16 pin area consists of three rows of socket terminals and will accept a total of 47 IC's of the 8, 14, or 16 pin type and having a lead spacing of 0.3 in. The 24 pin area will accept a total of 10 IC's with up to 24 pins per IC, and having a lead spacing of 0.3, 0.4, or 0.6 in. The 40 pin area will accept a total of 11 IC's with up to 40 leads per IC and having a lead spacing of 0.6 in. or a total of 22 IC's with up to 16 leads per IC and having a lead spacing of 0.3 in.

W9302 HI-DENSITY WIRE WRAPPABLE MODULE



W9302

DESCRIPTION

The W9302 is a hex height, extended length, double wide, wire wrappable module suitable for user designed logic interface applications. The module accepts a variety of dual-in-line (DIP) integrated circuits (IC's) or discrete components which can be mounted to the module without the use of solder. The component or IC leads insert into specially designed socket terminals which have a wire wrap pin on the opposite end. The electrical interconnection of the wire wrap pins can be performed manually or by using automated wire wrapping techniques.

The W9302 board has six rows of 36 gold-plated contacts (18 contacts on each side of each row). Each contact is connected to a wire wrap pin by the board etch. A ground plane is etched on side 1 of the module and power (Vcc) plane is etched on side 2. Contact pin A2 of each of the six rows directly connects to the power plane, and contact pins C2 and T1 directly connect to the ground plane.

A total of 97 decoupling capacitors are provided premounted between Vcc and GND at each main IC location. The module occupies two slots in a standard DIGITAL system unit.

Two 40 pin connectors are mounted at the edge of the module to facilitate the attachment of device cable assemblies.

Wire Wrap Terminals
All wire wrap terminals on side 2 of the module are located on a grid of 0.1 in. (0.254 cm) spacing to facilitate automatic point-to-point wire wrapping equipment. The connections to the pins are made using #30 gauge solid conductor insulated wire.

Total IC Complement
Up to 114 IC equivalents (14- or 16-pin DIP's) can be mounted on the module. Areas are provided on the board for mounting DIP's with a center spacing of 0.3 in. (0.78 cm) 0.4 in. (1.0 cm) or 0.6 in. (1.5 cm). Table 1 lists the acceptable IC types and pin spacing.

Table 1 W9302 IC TYPES

Total Pins	Center Spacing (in.)
8, 14, 16, 18, 20	0.3
22	0.4
24, 28, 40	0.6

The W9302 module has three pin configuration areas assigned to 16-pin, 24-pin and 40-pin IC's. The 16 pin area consists of three rows of socket terminals and will accept a total of 65 IC's of the 8, 14, or 16 pin type and having a lead spacing of 0.3 in. The 24 pin area will accept a total of 15 IC's with up to 24 pins per IC, and having a lead spacing of 0.3, 0.4, or 0.6 in. The 40 pin area will accept a total of 17 IC's with up to 40 leads per IC and having a lead spacing of 0.6 in. or a total of 34 IC's with up to 16 leads per IC and having a lead spacing of 0.3 in.

Part No.	Contact Fingers	Size	Description
W940	144	Quad-height, extended length	Accommodates up to fifty 14- or 16-pin DIP ICs with or without sockets. (Sockets not included.)
W941	72	Double-height, extended length	Same as W940 except accommodates up to twenty-five 14- or 16-pin DIP ICs with or without sockets. (Sockets not included.)
W942	144	Quad-height, extended length	Same as W940 except equipped with 50 low-profile, 16-pin DIP IC sockets.
W943	72	Double-height, extended length	Same as W941 except equipped with 25 low-profile, 16-pin DIP IC sockets.
W950	144	Quad-height, extended length	Accommodates up to thirty 14- or 16-pin DIP ICs and up to eight 24-pin DIP ICs with or without sockets. (Sockets not included.)
W951	72	Double-height, extended length	Same as W950 except accommodates up to fifteen 14- or 16-pin DIP ICs and up to four 24-pin DIP ICs with or without sockets. (Sockets not included.) The four 24-pin locations can also accommodate four 14- or 16-pin ICs instead of the 24-pin ICs.
W952	144	Quad-height, extended length	Same as W950 except equipped with 30 low-profile, 16-pin DIP IC sockets and eight 24-pin DIP IC sockets.
W953	72	Double-height, extended length	Same as W951 except equipped with 15 low-profile, 16-pin DIP IC sockets and four 24-pin DIP IC sockets.

WIRE WRAPPING TOOLS AND ACCESSORIES

Wire wrapping provides positive, uniform electrical connections faster and more economically than solder connections. Digital Equipment Corporation has a complete line of tools and accessories for wire wrapping all of the wire wrappable module connector blocks and all of the wire wrappable module boards summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Pistol-Grip Wire Wrapping Tool Kit—H810(24), H810-A, H810-B
The H810(24) Pistol-Grip Wire Wrapping Tool Kit provides a pistol-grip mechanical wire wrapping tool and a sleeve and bit of the proper size to wrap 24 AWG wire wrap wire.

The H810-A is the same as the H810(24) except the sleeve and bit are the proper size for wrapping 30 AWG wire wrap wire.

The H810-B is a combination of H810(24) and H810-A. H810-B provides a pistol-grip mechanical wire wrapping tool and the bits and sleeves of the proper sizes for wrapping 24 AWG or 30 AWG wire wrap wire.

Battery-Powered Wire Wrap Gun—H810-C, H810-D
The H810-C, H810-D, and H810-E battery-powered wire wrap guns are equipped with rechargeable, nickel-cadmium batteries. They do not require ac connection while in use. Their ease of operation reduces user-fatigue and provides uniform wire wrap connections.

The H810-C battery-powered wire wrap gun is supplied with a bit and sleeve for wrapping 24 AWG wire wrap wire.

The H810-D is supplied with a bit and sleeve for wrapping 30 AWG wire wrap wire.

H813 bits and H814 sleeves can be used with any of these battery-powered wire wrap guns.

Hand Wire Wrapping Tool—H811(24), H811-A
The H811(24) and H811-A hand wire wrapping tools are especially useful for service and repair applications. They can also be used for producing limited numbers of prototype modules.

H811(24) is designed for 24 AWG wire wrap wire, and the H811-A is designed for 30 AWG wire wrap wire.

Hand Wire Unwrapping Tool—H812(24), H812-A
The H812(24) and H812-A hand unwrapping tools are ideal for unwrapping wire strapped terminals.

The H812(24) is designed for unwrapping 24 AWG wire, and the H812-A is designed for unwrapping 30 AWG wire.

Bit for Battery-Powered Wire Wrap Gun—H813(24), H813-A
The H813(24) and H813-A bits are replacement bits for battery-powered wire wrap guns H810-C, H810-D.

The H813(24) is designed for 24 AWG wire, and the H813-A is designed for 30 AWG wire.

Sleeve for Battery-Powered Wire Wrap Gun—H814(24), H814-A
The H814(24) and H814-A sleeves are replacement sleeves for battery-powered wire wrap guns H810-C, H810-D.

The H814(24) is designed for 24 AWG wire ,and the H814-A is designed for 30 AWG wire.

INTEGRATED CIRCUIT (IC) SOCKETS

IC Sockets—954, 961, 962

These integrated circuit (IC) sockets provide low-cost, reliable production packaging of 14 or 16-pin, 24-pin, and 40-pin dual-in-line package (DIP) integrated circuits (ICs). These low-profile IC sockets are especially useful for limited-production runs of special, user-designed circuitry using the blank or wire wrappable module boards (described in this section), which are available without factory-installed IC sockets.

The 954 accepts 14- or 16-pin ICs; 10 sockets/package.

The 961 accepts 24-pin ICs; 5 sockets/package.

The 962 accepts 40-pin ICs; 5 sockets/package.

MODULE HANDLES, MODULE HANDLE EXTENDERS, AND MODULE HOLDERS

Module Handle—937

The 937 (90-08337-08) is a package containing 25 blank, gray module handles and the eyelets to attach them to modules. These blank handles are generally user-attached to prototype or limited-production run modules that utilize blank copper-clad or wire wrappable modules. The blank handles provide a convenient method of identifying the prototype or limited-production run modules because the user can put his own identification on the handle. The handles are compatible with the handles of all Digital Equipment Corporation standard A-, K-, M-, and W-series modules. They have two 0.128-in. (0.325-cm) diameter mounting holes spaced 2.00 in. (5.08 cm) center-to-center.

Module Handle Extender—H850

The H850 Module Handle Extender mounts over the handle of a single-height, single-length module and physically extends the length to make a single-length module congruous with extended length modules. The H850, in addition to making removal and insertion of single-length modules easier when the system predominantly utilizes extended length modules, adds to the appearance of the system by making the modules the same length.

The H850 is manufactured from durable, U.L. Standard No. 94 recognized material and is sized to fit over Digital Equipment Corporation's standard module handle. It is sold in lots of ten.

Module Holder Clips—H852, H853

The H852 and H853 Module Holders are used to maintain rigidity of the modules in a system. Each module holder fits over the top (handle end) of modules of the same length in adjacent slots of a system unit. The H852, a ribbed type holder, fits between handles of modules in the same connector block; the H853, a nonribbed type holder, fits between the handles of modules in adjacent (end-to-end) connector blocks. For example, on quad-high modules, an H852 fits between handles 1 and 2, an H853 fits between handles 2 and 3, and an H852 fits between handles 3 and 4.

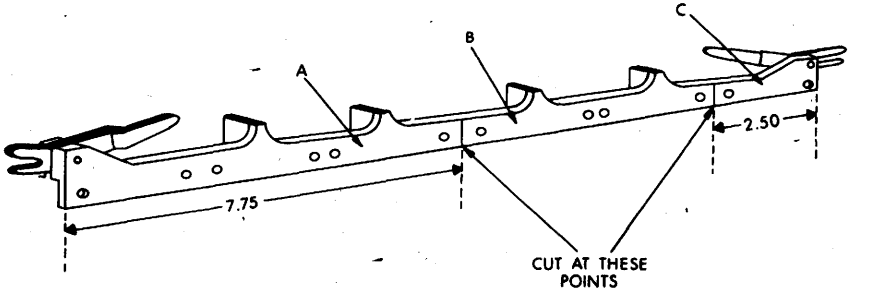
The H852 and H853 are manufactured from durable plastic material that is nonconductive. They are sold in lots of 25 each.

Hold-Down Bracket 12-10711-02

The 12-10711-02 module hold-down bracket serves as a mechanical combination handle and hold-down bracket for Hex-size modules when used with the appropriate cards guides such as an H0341. This bracket can also be used as a hold-down bracket for LSI-11 compatible modules (quad-size) but must be modified as shown in the accompanying drawing. Eyelets for attachment to the module are included.

LSI-11 HOLDOWN 12-10711-02

1. CUT BRACKET AT POINTS DESIGNATED ON DRAWING BELOW.
2. DISCARD CENTER SECTION "B".
3. MOUNT SECTIONS "A" AND "C" ON BOARD AS DESIRED.



BUS STRIPS

Bus Strips—932, 933, 939

Bus strips 932, 933, and 939 provide a convenient method of interconnecting all wire wrap pins in a system that are assigned identical control signals, power, or ground. These bus strips are flat, narrow conductors with holes that correspond to the connector block pin size and spacing. When a bus strip is placed over the pins and soldered to each, it will interconnect all of the pins with the same pin number for as many module slots as desired. After the modules have been selected and the slots of the mounting panel have been assigned to the modules, identical control signal, power, and ground pins can be bused with the bus strips.

Bus strip 932 can be used to bus systems using H800 Module Connector Blocks. Bus strip 933 can be used to bus systems using H803, H8030, and H863 Module Connector Blocks. Bus strip 939 can be used to bus systems using H808 Module Connector Blocks. Module connector blocks are summarized elsewhere in this publication and are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Length: 932 — 13.5 in. (39.4 cm)
933 — 21.5 in. (54.6 cm)
939 — 21.5 in. (54.6 cm)

PATCH CORDS AND ACCESSORIES

Grip-Clip Connectors for Slip-on Patch Cords—H820, H821

The H820 and H821 grip-clip connectors are identical to the connectors used on each end of 913 and 915 patch cords, respectively. These grip clips permit the fabrication of patch cords of any length.

H820 grip-clip connectors accept 24 to 20 AWG wire; they slip on wire wrap terminals that are sized for 24 AWG wire wrap wire, 0.031 by 0.062 in. (0.079 by 0.158 cm). H821 grip-clip connectors accept 30 to 24 AWG wire; they slip on wire wrap terminals that are sized for 30 AWG wire wrap wire, 0.025 in. (0.064 cm) square.

H820 and H821 grip-clip connectors are shipped in quantities of 1000 of one size.

Patch Cords—913, 915

The 913 and 915 patch cords provide slip-on connections at the wire wrap pins of FLIP-CHIP modules and module connector blocks. They are ideal for breadboarding prototype modules and making temporary or semipermanent jumpers at a system backplane. They are available in 11 color-coded lengths from 2 to 64 inches (5.04 to 162.56 cm).

Patch cord 913 is 24 AWG stranded wire with IPVC insulation, and is equipped on each end with an H820 grip-clip connector; H820 connectors fit on wire wrap pins that are sized for 24 AWG wire wrap wire, 0.031 by 0.062 in. (0.079 by 0.158 cm).

Patch cord 915 is 26 AWG stranded (7/34) with IPVC insulation, and is equipped on each end with an H821 grip-clip connector; H821 connectors fit on wire wrap pins that are sized for 30 AWG wire wrap wire, 0.025 in. (0.064 cm) square.

Patch cords 913 and 915 are available in quantities of 100 of the same length and same gauge, and in quantities of 100 of assorted lengths and the same gauge. The following chart lists the part number, length, and color code for 913 and 915 patch cords.

Part Number		Length in Inches	
24 AWG	26 AWG	(Centimeters)	Color
913-2	915-2	2 (5.08)	BRN
913-3	915-3	3 (7.62)	BRN/WHT
913-4	915.4	4 (10.16)	RED
913-6	915-6	6 (15.24)	RED/WHT
913-8	915-8	8 (20.32)	ORN
913-12	915-12	12 (30.48)	ORN/WHT
913-16	915-16	16 (40.64)	YEL
913-24	915-24	24 (60.96)	YEL/WHT
913-32	915-32	32 (81.28)	GRN
913-48	915-48	48 (121.92)	GRN/WHT
913-64	915-64	64 (162.56)	BLU
913-AF	915-AF	Assorted*	Assorted

* 913-AF and 915-AF comprise the following assorted patch cords: 30 BRN/WHT (-3); 25 RED/WHT (-6); 25 ORN (-8); 10 YEL/WHT (-24); 5 GRN (-32); and 5 BLU (-64).

When ordering, please specify part number 913 or 915 and the appropriate *dash* number.

Power Patch Cord—914-7, 914-19

The 914 power patch cords provide interconnections between power supplies and mounting panels that are equipped with Faston (TM) terminals, series 250. The 914 power patch cord is stranded wire with IPVC insulation and is equipped on each end with Faston receptacles, series 250. Power patch cord 914 is available in two lengths—7 inches and 19 inches (18 cm and 48 cm)—and is available in packages of ten of the same length. The 914-7 is a package of ten 7-inch (18-cm) patch cords. The 914-19 is a package of ten 19-inch (48-cm) patch cords.

(TM) Faston is a trademark of AMP, Inc.

Daisy Chain—917-2.5

The 917 daisy chain is a continuous length of stranded insulated wire on a reel with 250 gold-plated and insulated terminals crimped at 2.5-in. (6.4-cm) intervals. A prototype system is easily and quickly hand patched when the 917 daisy chain is used.

The terminals are designed to fit on module connector blocks that have wire wrap pins sized for wrapping with 30 AWG wire [0.025/0.026 in. (0.064/0.066 cm) square] e.g., module connector blocks H803, H8030, H807, and H863, summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

The dependable 917 daisy chain push-on terminals are easily removed from the connector block wire wrap terminals; this provides an ideal wiring technique in systems where unwiring and rewiring for changing system requirements are essential. If an additional lead is ever required on a wire wrap terminal, a 915 patch cord can be used; a 915 patch cord can be placed on the terminal after the wire wrap connection and before the 917 termination.

The 917-2.5 daisy chain has 250 terminals at 2.5-in. (6.4-cm) intervals.

CABLES
COMPLETE ASSEMBLIES AND PARTS

Digital offers a complete and comprehensive line of pre-assembled cable assemblies compatible with most computer products offered.

In addition, Digital also offers a complete line of cable accessories and parts for users who wish to construct their own cables.

This CABLE section is divided into two subsections:

1. Cables (assembled)
2. Cable Accessories (raw cabling, connectors)

The pre-assembled cables subsection represents a listing of the most popular cable types and the most popular lengths available.

The other subsection describes cable components such as terminators, connectors, raw cable, and related cable accessories.

Many of the cables supplied by DIGITAL are also available in non-standard custom lengths. For information on price and delivery either call your nearest sales office or Logic Products Sales Support, Accessories & Supplies Group, DIGITAL, MK1-2/E13, Merrimack, NH 03054.

CABLE WARRANTY NOTE

All standard and custom length cables are guaranteed against defects in material and workmanship for a period of 90 days from date of shipment.

Digital Equipment Corporation neither expresses or implies that custom length cables will function satisfactorily if the electrical performance specification (e.g., drive length) for the application is exceeded.

CABLE TYPE	DESCRIPTION (Principal Use)	CONNECTIONS
BC01R-25	M970 PLUS BC05C-25	M970 TO RS232
BC01V-25	EIA DATA CABLE	12-5886 TO 12-5885
BC04Z-06	MULTI-USE	H856 TO OPEN
BC04Z-10	MULTI-USE	H856 TO OPEN
BC04Z-25	MULTI-USE	H856 TO OPEN
BC05C-25	DL11 CABLE	H856 TO RS232-M
BC05C-50	DL11 CABLE	H856 TO RS232-M
BC05D-10	MULTI-USE	RS232-M TO RS232-F
BC05D-25	MULTI-USE	RS232-M TO RS232-F
BC05H-06	60 HZ LINE CORD	AC INPUT BOX H400-A
BC05J-06	50 HZ LINE CORD	AC INPUT BOX H400-B
BC05M-2C	TTY CABLE	12-9340 TO H856
BC05M-04	TTY CABLE	12-9340 TO H856
BC06R-06	MASS BUS (FLAT)	H855 TO H855
BC06R-10	MASS BUS (FLAT)	H855 TO H855
BC06R-25	MASS BUS (FLAT)	H855 TO H855
BC06R-50	MASS BUS (FLAT)	H855 TO H855
BC06S-10	MASS BUS (ROUND)	12-11591 TO 12-11591
BC06S-25	MASS BUS (ROUND)	12-11591 TO 12-11591
BC06S-40	MASS BUS (ROUND)	12-11591 TO 12-11591
BC07A-10	MULTI-USE 20TWP	H856 TO OPEN
BC07A-15	MULTI-USE 20TWP	H856 TO OPEN
BC07A-25	MULTI-USE 20TWP	H856 TO OPEN
BC07B-10	MULTI-USE 11TWP	H856 TO OPEN
BC07B-25	11TWP	H856 TO OPEN
BC07D-10	20-COND	H856 TO OPEN
BC07D-15	20-COND	H856 TO OPEN
BC07D-25	MULTI-USE	H856 TO OPEN
BC08A-03	MULTI-USE 20-COND	M904 TO M904
BC08A-05	MULTI-USE	M904 TO M904
BC08A-10	MULTI-USE	M904 TO M904
BC08J-06	PDP-8E 40-COND	H856 TO M953
BC08J-10	PDP-8E 40-COND	H856 TO M953
BC08M-0M		H859 TO H859
BC08R-01	MULTI-USE	H856 TO H856
BC08R-03		
BC08R-06		
BC08R-10		
BC08R-20		
BC08R-25	MULTI-USE	H856 TO H856
BC08R-50	MULTI-USE	H856 TO H856
BC11A-02	MULTI-USE, UNIBUS	M929 TO M919
BC11A-05		
BC11A-10		
BC11A-15		
BC11A-25		
BC11A-8F	MULTI-USE, UNIBUS	M929 TO M919
BC11K-25	DR11-C	H856 TO OPEN
BC11S-25	MULTI-USE	H856 TO H856

CABLE TYPE	DESCRIPTION (Principal Use)	CONNECTIONS
BC11S-50	MULTI-USE	H856 TO H856
BC11S-A0	MULTI-USE	H856 TO H856
70-8360	DL11	12-9340 TO H856
70-11212-25	LP11	
70-11212-50	LP11	
70-11212-A0	LP11	

Wire

91-05740	30 AWG Wire Wrapping Wire, 1000-ft/spool (formerly designated 935)
91-07688	24 AWG Wire Wrapping Wire, 1000-ft/spool (formerly designated 934)

CABLE CONNECTORS

Cable connectors are grouped into eight general classifications according to the type cable they accommodate and their use: flat ribbon cable, flat mylar cable, flat coaxial cable, round coaxial cable, flat shielded cable, round cable, bus interconnection and termination, and miscellaneous connectors. Most of the connectors described in this section are general-purpose connectors; some, however, are specific-use connectors. These connectors are described relative to the specific use. The descriptions of some of the general-purpose connectors cite application examples; the cited examples are popular, widely used applications and are not intended to imply that a particular connector cannot be used with other equipment.

Frequently Digital Equipment Corporation preassembled cable assemblies are available to fulfill your cabling requirements and eliminate the need for you to fabricate a cable assembly. Many preassembled cable assemblies are described in this handbook. Additional preassembled cable assemblies are described in the CABLE PRICE LIST AND CROSS-REFERENCE GUIDE published by Digital Equipment Corporation.

Digital Equipment Corporation also fabricates unique, special-purpose cables according to the customer's specifications to suit almost any requirement. These specially built cable assemblies are completely assembled and tested. Details on special-purpose cables are available from your local DIGITAL sales office or from Logic Products Sales Support, Accessories & Supplies Group, DIGITAL, MK1-2/E13, Merrimack, NH 03054.

A cable clamp and two eyelets are supplied with each cable connector. The cable clamp desired should be specified in each order for cable connectors; if cable clamps are not specified, the cable clamp that is usually used with the cable connector will be supplied. Cable clamps are described elsewhere in this publication.

The following tables summarize the cable connectors; individual detailed descriptions and schematic diagrams of these cable connectors are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Flat Ribbon Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M908	36	2	Single-height, standard length	No contact fingers dedicated to ground; 10-ohm resistors in series with four contact fingers. Split-lug terminals. Similar to M901.
M933	20	1	Single-height, standard length	Twenty signal contact fingers, two ground contact fingers, three power contact fingers. Resistors, capacitors, and jumpers may be installed by user at all signal contact fingers to provide pull-up capabilities to any one of three jumper-selectable voltage fingers, or resistors may be installed by user to provide shunt-to-ground (termination) capabilities at all signal contact fingers. Split-lug terminals for cable conductors and voltage jumpers.
M957	36	2	Single-height, extended length	No contact fingers are dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers. Split-lug teminals.
M976	120	2	Double-height, short length	Unibus cable connector. Fifty-six signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Usually used to connect the Unibus to a system unit in an external drawer or cabinet or to a peripheral device. Similar to M919.
W011	18	1	Single-height, short length	Nine contact pins dedicated to ground; nine contact pins for signal use. Can be wired for alternate signal/ground configuration. Nineteen split-lug terminals.

*Cable conductor connections.

Flat Ribbon Cable Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
W021	18	1	Single-height, single length	Nine contact pins dedicated to ground; nine contact pins for signal use. Can be wired for alternate signal/ground configuration. Nineteen split-lug terminals.
W023	18	1	Single-height, single length	All 18 contact pins can be assigned to signals; none are dedicated to ground. Eighteen split-lug terminals. Two jumpers or resistors must be user-installed in series with contact pins A and B.
W027	18	1	Single-height, single length	All 18 contact pins can be assigned to signals; none are dedicated to ground. A 3000-ohm resistor is in series with each pin. Eighteen split-lug terminals.

*Cable conductor connections.

Flat Mylar * Cable Connectors

Module	No. of Pins**	No. of Cables	Size	Description
M901	36	2	Single-height, standard length	No contact fingers dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers. PC solder. Similar to M908 and M922.
M903	36	2	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Similar to M904 and M943.
M918	36	2†	Single-height, standard length	No contact fingers dedicated to ground. Jumpers in series with contact fingers U1 and V1; installation of jumpers or resistors required at contact fingers A2 and B2. PC solder.
M922	36	2	Single-height, standard length	No contact fingers dedicated to ground. Jumpers in series with four contact fingers. PC solder. Similar to M901.
M943	32	2†	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Similar to M903.
W033	18	1	Single-height, single length	All 18 contact fingers can be assigned to signals; none are dedicated to ground.

**Cable conductor connections.
†Cables enter at right angles to the board.

* Mylar is a registered trademark of E.I. duPont de Nemours & Co.

Flat Coaxial Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M904	26	2	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Twenty-six split-lug terminals, eight dedicated to ground. Similar to an M903; similar to ½ of an M912.
M917	30	2†	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Thirty split-lug terminals, 12 dedicated to ground.

Round Coaxial (TWP) Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M912	72	2	Double-height, standard length	Thirty-six signal contact fingers, 28 ground contact fingers. Split-lug terminals. Alternate signal/ground cable conductors. Each slot similar to M904.
M927	27	1†	Single-height, standard length	Sixteen signal contact fingers, 16 ground contact fingers. Split-lug terminals. Similar to M925.
W024	18	1	Single-height, short length	Sixteen signal contact fingers, two ground contact fingers. Thirty-three split-lug terminals. Can be wired for alternate signal/ground configuration.
W028	18	1	Single-height, single length	Same as W021 except with split-lug terminals for series or shunt resistors/capacitors in signal leads.

*Cable conductor connections (includes shields).
†Cables enter at right angles to the board.

Flat Shielded Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M953	40	1	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. Equipped with a connector for solderless connection of the cable.
M954	80	2	Single-height, standard length	None of the contact fingers are dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers: U1, V1, A2, and B2. Alternate signal/ground cable conductors possible. Equipped with two connectors for solderless connection of the cables.
M955	40	1	Single-height, standard length	None of the contact fingers are dedicated to ground; 16 signal contact fingers; 10-ohm resistors in series with two contact fingers. Alternate signal/ground cable conductors possible. Equipped with a connector for solderless connection of the cable.

*Cable conductor connections.

Bus Interconnection and Termination Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M920	N/A	N/A	Double-height, short length dual circuit board	Unibus jumper module.
M930	N/A	N/A	Double-height, short length	Unibus terminator module. Terminates all UNIBUS signals.
M935	N/A	N/A	Double-height, short length dual circuit board	Omnibus jumper module.
M981	N/A	N/A	Double-height, standard length, dual circuit board	Unibus terminator module. Terminates all Unibus signals except AC LO L, DC LO L, BG7 H, BG6 H, BG5 H, BG4 H, and NPG H.

*Cable conductor connections.

Miscellaneous Connectors

Connector	No. of Pins*	No. of Cables	Size	Description
12-09340-00	8	See Description column	2.3 × 0.85 × 0.3 in. (5.8 × 2.2 × 0.8 cm) nominal	Female connector with up to eight female pins to provide termination for up to eight 20-14 AWG conductors. Equipped with two mounting holes and is usually mounted on a connector board or on the equipment. Requires 12-09379-01 pins. Mates with 12-09340-01 connector. Usually used with TTY and other serial devices.
12-09340-01	8	See Description column	2.2 × 1.5 × 0.3 in. (5.5 × 3.7 × 0.8 cm) nominal	Male connector that mates with 12-09340-00 connector and is usually used to terminate a cable with up to eight 20-14 AWG conductors. Requires 12-09378-01 pins. Usually used with TTY and other serial devices.
12-09350-03, -04,-06,-09, -12, -15	3, 4, 6, 9, 12, or 15	Refer to 12-09350 description in this section	Refer to 12-09350 description in this section	Female connectors that accommodate 3, 4, 6, 9, 12, or 15 female pins to provide termination for 26-14 AWG conductors. Usually bulkhead mounted. Requires 12-09879-01 pins. Mates with 12-09351-03, -04, -06, -09, -12, or -15 connectors. Usually used with TTY and other serial devices.
12-09351-03 -04, -06, -09, -12, -15	3, 4, 6, 9, 12, or 15	Refer to 12-09351 description in this section	Refer to 12-09351 description in this section	Male connectors that mate with 12-09350-03, -04,-06,-09, -12, or -15 connectors and are usually used to terminate a cable with 26-14 AWG conductors. Usually used with TTY and other serial devices.

*Cable conductor connections.

Miscellaneous Connectors (Cont)

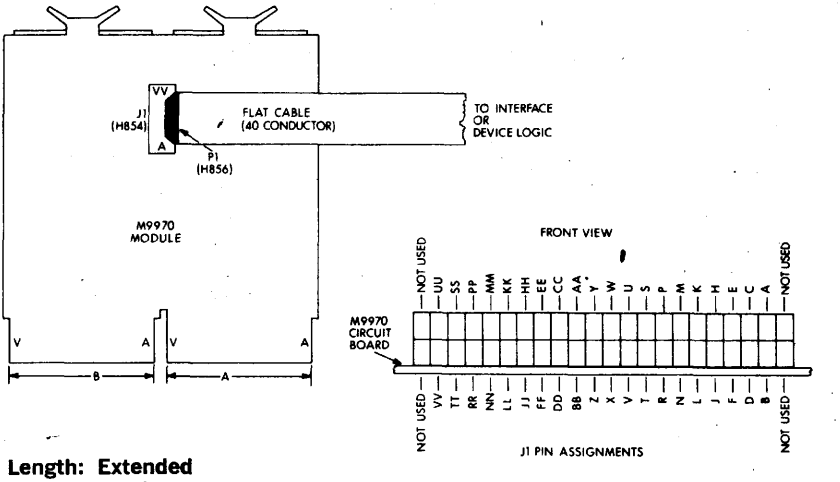
Connector	No. of Pins*	No. of Cables	Size	Description
H851	N/A	1	Two adjacent slots accommodate 36 single-height contact fingers	Edge connector providing busing of 36 signals of two adjacent modules equipped with top (handle end) contact fingers.
H854	40	1	2.5 × 0.75 × 0.3 in. (4.6 × 1.89 × 0.8 cm) nominal	A 40-pin connector designed to be mounted on a printed circuit board. The pins form right angles to intersect the printed circuit tracks. Mates with H856 connector.
H856	40	1	2.205 × 0.545 × 0.200 in. (5.600 × 1.384 × 0.508 cm) nominal	Designed to terminate a cable and mate with H854 connector. (Referred to as a "Berg connector.")
M9100	80 at H854s	2	Single-height, extended length	Printed circuit cable connector with two 40-pin H854 connectors that mate with cables equipped with H856 connectors. The two H854 connectors and the board contact fingers form a "T" type connector. Thirty-two independent lines available at contact fingers with the remaining contact fingers, usually associated with ground, connected in common.

*Cable conductor connections.

Miscellaneous Connectors (Cont)

Connector	No. of Pins*	No. of Cables	Size	Description
M971	40 at one H854	1	Single-height, standard length	Printed circuit cable connector with a 40-pin H854 connector that mates with a cable equipped with an H856 connector. Forty pins of the H854 in series with 36 board contact fingers; i.e., 32 pins of the H854 in series with 32 contact fingers (four with 10-ohm resistors in series) and eight pins of the H854 in series with four contact fingers. No contact fingers dedicated to ground.
M973	4	1	Single-height, standard length	Printed circuit cable connector with a 12-09340-00 connector equipped with four pins. The connector mates with a cable equipped with a 12-09340-01 connector. Normally used as a TTY cable connector.
M975	80 at two H854s	2	Double-height, short length	Printed circuit cable connector with two 40-pin H854 connectors that mate with cables equipped with H856 connectors. Eighteen pins of each H854 in series with 18 board contact fingers; the two H854 connectors are not electrically connected. Six contact fingers and 44 H854 pins dedicated to ground. Alternate signal/ground cable conductors.

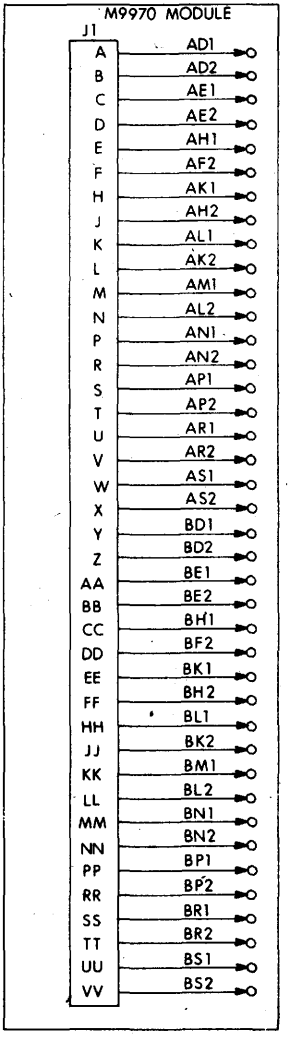
*Cable conductor connections.



Length: Extended
Height: Double
Width: Single

M9970 H854-TO-BACKPLANE ADAPTER

The M9970 is a double-height, extended-length module with an H854 Male Connector permanently mounted to the board. Each of the 40 pins of the H854 connect to the edge board contacts of the module through printed circuit wiring. The H854 will accept any standard or special flat cable with an H856 Plug mounted on the cable end. The module can be used as an adapter to transfer signals and levels to or from a device or interface logic and the backplane wiring of a system unit or connector block. To facilitate installation with DIGITAL systems, none of the signal lines of the M9970 Module connect to the standard power or ground pins normally assigned to the FLIP CHIP modules.


M9970 MODULE
J1
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UU
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AK1
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BD2
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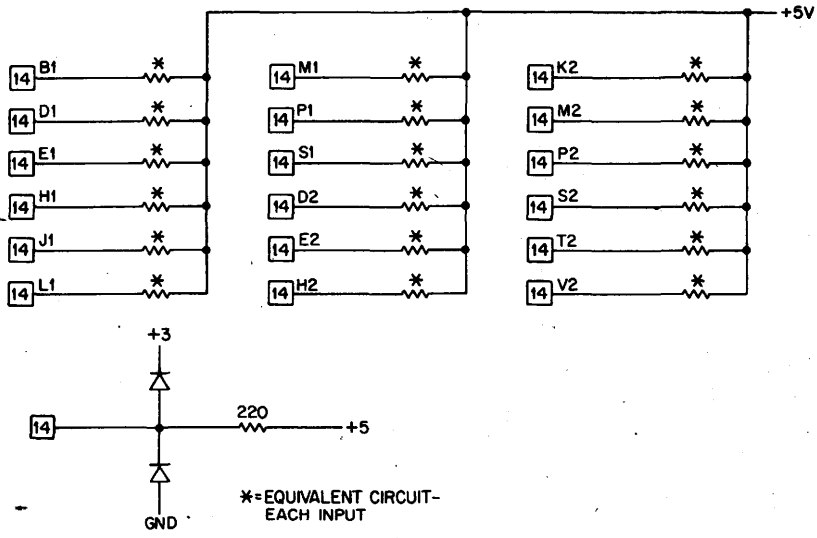
BF2
BK1
BH2
BL1
BK2
BM1
BL2
BN1
BN2
BP1
BP2
BR1
BR2
BS1
BS2

M906 CABLE TERMINATOR

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	440*	A2
GND**		A1, C1, F1, K1, N1, R1, T1 C2, F2, J2, L2, N2, R2, U2

* all signal lines grounded
** all ground pins must be grounded

The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3 volts and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

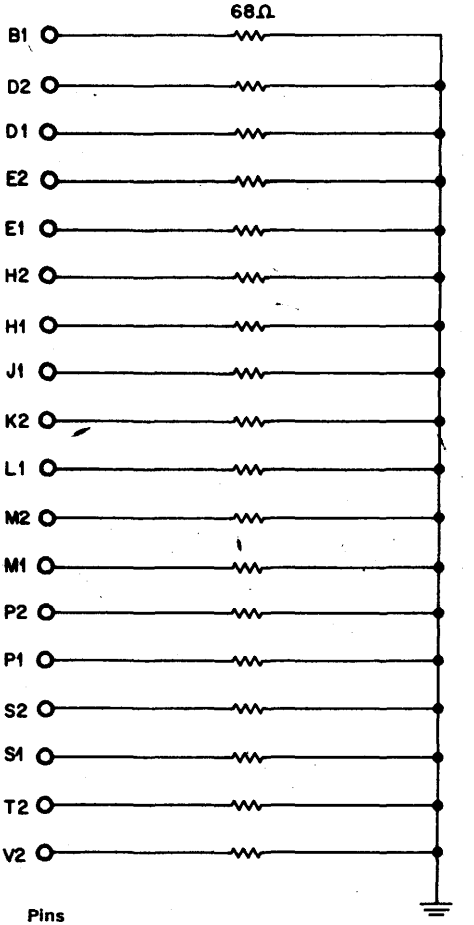
APPLICATIONS

The M906 may be used to terminate inputs. In this configuration M906 and M111 are a good combination.

This module is normally used with standard M Series levels of 0 and +3 volts to partially terminate 100-ohm cable. It presents a load of 22.5 mA or 14 TTL unit loads at ground and, therefore, must be driven from at least an M116-type circuit or, preferably, a cable driver.

M909 TERMINATOR

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	NONE	
GND		A1, C1, C2, F1, J2, K1 L2, N1, N2, R1, R2, T1, U2

The M909 module contains eighteen 68-ohm resistors tied to ground through a common bus.

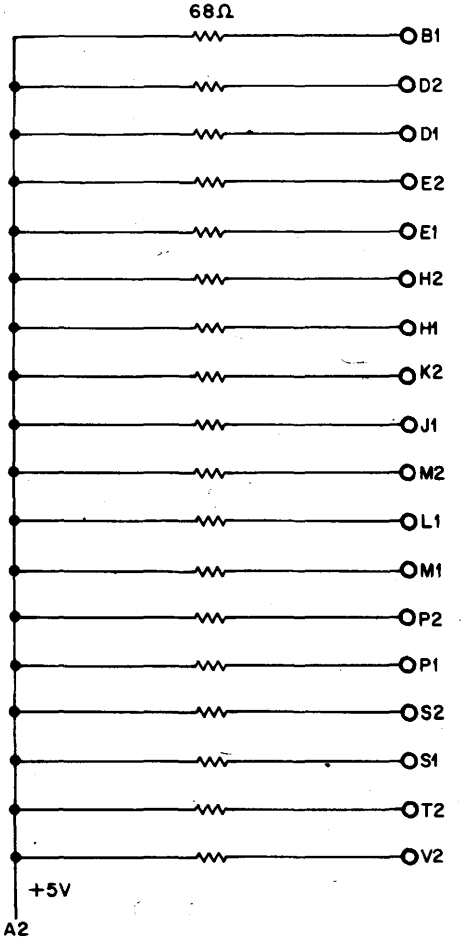
APPLICATIONS

This module is intended to be used with the M910 to form half of the biasing circuit used in the driving network of the M622.

M910 TERMINATOR

Length: Standard
Height: Single
Width: Single

Volts	Power mA (max.)	Pins
+5	1350	A2
GND		A1, C1, C2, F1, F2, J2, K1 L2, N1, N2, R1, R2, T1, U2



The M910 module contains eighteen 68-ohm resistors tied to a common +5 volt bus.

APPLICATIONS

This module is intended to be used with the M909 to form half of the biasing circuit used in the driving network of the M622.

CABLE CLAMPS

Cable clamps provide strain relief where a cable enters a cable connector. Cable clamps are available for both flat and round cables.

Cable Clamp—12-09764

The 12-09764 cable clamp can be used with flat cable up to 4.562 in. (11.587 cm) wide. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 4.750 in. (12.065 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—12-09925

The 12-09925 cable clamp can be used with module connector block H807 and a round cable. An H807 connector block and a round cable provide a convenient method of terminating a single-height module at a remote location. The 12-09925 cable clamp protects the solder connections of the cable and the connector pins; it also prevents excessive strain on the cable when the module is inserted into or removed from the module connector. The 12-09925 will accommodate cables from 0.290 in. (0.737 cm) to 0.390 in. (0.813 cm) in diameter.

The body of the 12-09925 is equipped with two 6-32 threaded inserts so that the cover of the 12-09925 can be secured to the body.

Cable Clamp—940

The 940 cable clamp can be used with flat cable up to 1.75 in. (4.45 cm) wide. The cable slot is 0.080 in. (0.203 cm) deep. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—941

The 941 cable clamp can be used with round cable that is 0.281 to 0.438 in. (0.714 to 1.113 cm) in diameter. The 941 cable clamp can also be used where cables require strain relief at the entry point to panels and cabinets. Two 0.136-in. (0.345-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector, panel, or cabinet; nylon mounting hardware (No. 4 screw and nut) is recommended.

about digital equipment corporation

In approximately 21 years, DIGITAL EQUIPMENT CORPORATION has grown from three employees and one floor of production space in a converted woolen mill, to a major international corporation. DIGITAL now employs more than 38,000. Our products are manufactured worldwide, and are sold and serviced from customer support centers in the United States, Canada, Japan, Australia and several European countries.

We produce a wide variety of computer and control products ranging from logic modules to large time sharing computer systems. In addition to those logic modules and associated equipment detailed in this handbook, DIGITAL also manufactures 12-, 16-, 18- and 36-bit computers, peripheral devices, special systems, accessories, programmable controllers and a wide variety of software.

DIGITAL first began manufacturing computer-related equipment in 1957 when we introduced a line of solid state logic modules. These were initially used to test and build other manufacturers' electronic equipment. The logic module product lines have been continually broadened, and DIGITAL now ranks as the world's largest manufacturing supplier of digital logic modules, producing more than three million per year.

Our first computer, the PDP-1 was introduced over a decade ago, selling for $120,000 while competitive machines were priced over $1 million. Ever since the PDP-1, DIGITAL has specialized in on-line, real-time computers.

The PDP-5, introduced in 1963, was the first truly small computer. The PDP-8 series, the PDP-5 successor announced in 1965, is one of the most popular and successful families of computers ever produced.

The PDP-11 sixteen-bit computer also ranks as the industry leader of medium-sized systems.

DIGITAL is a leading force in small computers, but it also has been a pace-setter in other parts of the industry. For example, one of the first time sharing systems ever built incorporated a PDP-1. DIGITAL introduced the first large-scale, commercially available time sharing system in 1965—the PDP-6. Its successor, the DECsystem-10, can do more at a price well under $1 million than competitive systems costing several times as much.

In industry, DIGITAL computers provide engineers with a powerful control and testing tool. They control blast furnaces and open hearths, monitor slab mills and finishing mills, and control and monitor a variety of machine tools, transfer and material handling equipment. DIGITAL computers can be found

controlling a busy section of the New Jersey Turnpike and providing typesetting and copy production for many newspapers and publishing firms.

In science, our computers have cut the researchers experiment time with direct, on-line data reduction. DIGITAL computers control and monitor powerful nuclear reactors, control X-ray diffractometers, analyze nuclear spectroscopy data, and assisted in the analysis of lunar rock samples. They are used extensively in environmental research and pollution control.

In virtually all DIGITAL computer installations, DIGITAL solid state logic is used for interfacing or control application.

GENERAL INFORMATION

FINANCIAL RESULTS (Fiscal Year)

Total Sales (in millions)		Net Income (in millions)	
1977	$1,058.6	1977	$108.5

DIGITAL EQUIPMENT CORPORATION

DIGITAL COMPUTER SPECIAL SYSTEMS FACILITIES

AUSTRALIA
Sydney
CALIFORNIA
Santa Ana
CANADA
Kanata (Ottawa)
FRANCE
Annecy
GERMANY
Munich
JAPAN
Tokyo
NEW HAMPSHIRE
Nashua
SWEDEN
Solna (Stockholm)
UNITED KINGDOM
Reading

DIGITAL MANUFACTURING FACILITIES

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CANADA
Kanata
COLORADO
Colorado Springs
HONG KONG
IRELAND
Galway
MAINE
Augusta
MASSACHUSETTS
Acton
Marlborough
Maynard
Natick
Springfield
Westboro
Westfield
Westminster
NEW HAMPSHIRE
Derry
Nashua
Salem
NEW MEXICO
Albuquerque
PUERTO RICO
Aguadilla
San German
SCOTLAND
Ayr
TAIWAN
VERMONT
South Burlington

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CANADA
Kanata (Ottawa)
DISTRICT OF COLUMBIA
Washington (Lanham, Md.)
FRANCE
Rungis (Paris)
GERMANY
Munich
ILLINOIS
Rolling Meadows (Chicago)
ITALY
Milan
JAPAN
Tokyo
MASSACHUSETTS
Marlborough
Maynard
NETHERLANDS
Utrecht
NEW YORK
New York City
SPAIN
Madrid
SWEDEN
Solna
SWITZERLAND
Zurich
UNITED KINGDOM
Reading

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TWX: 610-562-8732

TOTAL EMPLOYEES 38,000

GENERAL DESCRIPTION OF DIGITAL PRODUCTS
(Excluding those discussed in this Handbook)

COMPUTERS

PDP-8E, PDP-8F, PDP-8M, PDP-8/A, the lower cost successors to the PDP-8/I and PDP-8/L. They are the outgrowth of the largest concentration of minicomputer engineering, programming and user expertise in the world. Among the PDP-8/E features are: a unique internal bus system called OMNIBUS™, which allows the user to plug memory and processor options into any available slot location; the availability of 256 words of read only or read/write memory; a 1.2 microsecond memory cycle time; the use of TTL integrated circuitry with medium scale integration; expansion to 32,768 12-bit words; low cost mass storage expansion with DECdisk, DECtape, or the DECcassette.

PDP-11 A family of expandable general purpose computers with 4,096 16-bit words of standard core memory. Memory cycle time is 1.2 microseconds. Machine uses integrated circuitry and has some medium-scale integration in central processor. Models are PDP-11/03, 04, 34, 45, 55, 60, and 70.

VAX-11/780 A compatible upward extension of the PDP-11 family, this computer features a 32-bit word length, a large virtual-memory operating system, and a very extensive instruction set especially suited for efficient high-level language programs.

PDP-12 Laboratory computer system capable of executing PDP-8 and LINC-8 programs. It has basic 4,096-word core memory. Each word is 12 bits in length. Basic laboratory system includes interactive graphics capability, magnetic tape storage, A/D converter, and prewired, real-time clock.

PDP-15 A medium-scale series with an 18-bit word length, available in 5 complete software operating systems and 8 applications packages.

DECSYSTEM-20 Family of outstandingly low-cost medium-scale mainframes with 36-bit word length, fully software-compatible with each other and with the rest of the Digital mainframe line. Models are 2020, 2040, 2050, and 2060.

DECSYSTEM-10 General purpose 36-bit word large computer that will handle up to 63 time-sharing users simultaneously with batch and real-time jobs at the same time.

COMPUTER-BASED SYSTEMS

Industrial Products. Digital's industrial computer systems are based on PDP-8 and PDP-11 processors and encompass a range of power and capability. Products designed specifically for the industrial user include programmable controllers, environmental computer enclosures industrial control subsystems and power demand control equipment.

Business Systems. Digital's business-oriented computer systems, called DEC DATASYSTEMS, are based on the PDP-8 and PDP-11 minicomputer families and configured with appropriate terminals and storage devices. They function as complete stand-alone data-handling systems or as intelligent terminals in a large network. A new addition is the VT78 DECstation, the company's lowest-priced full computer system.

Education Products. These systems include a variety of applications software and vary from small stand-alone single-user systems to large, multi-user

timesharing configurations capable of handling computer-aided instruction as well as administrative data processing.

Data Communications. The data communications capability of the computer is enhanced by the special products—data handlers, front-end preprocessors, data loggers, modems—as well as the software and services of Digital's DECcomm group.

Laboratory Data Products include the DECgraphic-11 series of interactive, stand-alone computer-based graphics systems, DEClab-11 laboratory data handling systems, the Gamma-11, designed for use in nuclear medicine, MUMPS-11 data base management system for the hospital environment, PHA-11 pulse height analysis systems designed specifically for nuclear and x-ray spectroscopy in low-energy physics and radiochemistry applications, and the PDL programmable data logger, an easy-to-use laboratory data acquisition system.

Computerized Typesetting. Computer-based systems for setting type, including justification and hyphenation, text storage and editing, classified ad handling and related business applications, are available in a range of size and capability—Typeset-8, Typeset-11, Typeset-10—depending on the Digital computer system.

Word Processing. Digital's family of video-display word processing products includes both stand-alone and multi-terminal, shared-logic systems. They can interact with PDP-11-based systems also.

Original Equipment Manufacturing. Digital serves the OEM with a complete range of products and services designed to enhance the capability and profitability of both the manufacturer and the end user.

Components. The same quality components found in Digital products are available to the high-volume user, in quantity, without the normal Digital supporting services.

Peripherals. Digital offers a wide range of peripheral equipment and accessory devices for the computer user. Among them: analog/digital converters, display and plotting equipment, drums and disks, magnetic tape equipment, card, equipment, lineprinters.

Graphic Systems. Digital's GT series interactive graphic terminal systems function as complete stand-alone graphics systems or as part of a larger system configuration.

Special Systems. Digital maintains a special systems group with the capability to custom-build hardware and software systems to fulfill specific applications.

Software. A comprehensive selection of software complements Digital hardware. Assemblers, debugging routines, editors, monitors, floating point packages, mathematical routines, and diagnostic programs are available, as are conversational, interpretive languages developed for use in specific application areas.

Supplies and Accessories. Digital also provides power supplies, cabinetry, mounting hardware, tape, tape reels, storage racks, teleprinter ribbon and paper.

WARRANTY

A. All Products (except Software) listed in this Handbook are warranted as stated below for a period of ninety (90) days from date of initial delivery, except that the warranty period for W, M, K, and A Series modules is one (1) year.

B. All Products (except Software) are warranted against defects in material and workmanship under normal and proper use and in their original unmodified condition for the period set forth in Clause A above. If found defective by DIGITAL within the terms of this warranty, DIGITAL's sole obligation shall be to repair or replace (at its option) the defective Product. If DIGITAL determines that the Product is not defective within the terms of this warranty, Customer shall pay all costs of handling and return transportation. All replaced Products become the property of DIGITAL. As a condition of this warranty, Customer must obtain a DIGITAL Return Authorization Number, and must return all Products, transportation prepaid and insured, to:

Digital Equipment Corporation
Logic Products Services
Repair Section
Cotton Road
Nashua, NH 03061

C. Transportation charges for the return to Customer shall be paid by DIGITAL within the contiguous United States only. These warranties outside the contiguous United States are limited to repair or replacement only and exclude all costs of shipping, Customs clearance, and other related charges.

D. Premium methods of shipment are available at customer expense and will be used only when specifically requested. DIGITAL maintains a factory repair service for customer convenience and will repair equipment beyond the warranty at then current prices as long as repair components are available.

E. EXCEPT FOR THE EXPRESS WARRANTIES STATED ABOVE, DIGITAL DISCLAIMS ALL WARRANTIES ON PRODUCTS, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of DIGITAL for damages, including but not limited to special, indirect, or consequential damages arising out of or in connection with the use or performance of the Products.

HOW-TO-ORDER
All products described in this Handbook can be ordered by telephone, TELEX, TWX, or mailed to your local DIGITAL sales office. When placing an order, please provide specific information regarding part number full description, quantity, ship-to and bill-to addresses. Please state on your purchase order that "DIGITAL's Standard Terms & Conditions govern this order." Prices are listed in the Price Supplement booklet, and do not include applicable state and local taxes or shipping charges.

Also, by using the DIGITAL **Direct Sales Catalog,** you can order direct from the factory and realize significant savings on many items in this Handbook. Order your copy of the **Direct Sales Catalog** by filling in the postcard attached in this Handbook, or call toll-free 8:30 AM to 5:00 PM Eastern time 800-258-1710. From New Hampshire locations or places outside the continental U.S., 603-884-6660.

MINIMUM ORDER SIZE
A minimum order size of $35 is required. Customers will be billed the full $35 for orders not meeting the minimum size.

CANCELLATION POLICY
All orders placed with Logic Products and scheduled for shipment, if cancelled by customer in whole or in part, are subject to a cancellation charge if cancelled before or after the scheduled shipping date. The cancellation charge is $25 for any cancellation within sixty (60) days of the scheduled delivery date. Custom variations are considered non-cancellable after the order is acknowledged.

ALPHANUMERICAL PRODUCT INDEX
HOW TO ORDER,
WARRANTEE

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digital

DIGITAL EQUIPMENT CORPORATION, Corporate Headquarters: Maynard, Massachusetts 01754, Telephone (617) 897-5111—SALES AND SERVICE OFFICES; UNITED STATES—ALABAMA, Birmingham and Huntsville • ARIZONA, Phoenix and Tucson • CALIFORNIA, Los Angeles, Oakland, Sacramento, San Diego, San Francisco, Santa Ana, Santa Barbara, Santa Clara, Sunnyvale • COLORADO, Denver • CONNECTICUT, Fairfield and Meriden • DISTRICT OF COLUMBIA, Washington, D.C. (Lanham, MD) • FLORIDA, Miami, Orlando, Tampa • GEORGIA, Atlanta • HAWAII, Honolulu • ILLINOIS, Chicago, Peoria, Rolling Meadows • INDIANA, Indianapolis • IOWA, Bettendorf • KENTUCKY, Louisville • LOUISIANA, New Orleans • MASSACHUSETTS, Springfield and Waltham • MICHIGAN, Detroit • MINNESOTA, Minneapolis • MISSOURI, Kansas City and St. Louis • NEBRASKA, Omaha • NEW HAMPSHIRE, Manchester • NEW JERSEY, Cherry Hill, Fairfield, Princeton, Somerset • NEW MEXICO, Albuquerque • NEW YORK, Albany, Buffalo, Long Island, Manhattan, Rochester, Syracuse • NORTH CAROLINA, Charlotte and Durham/Chapel Hill • OHIO, Cincinnati, Cleveland, Columbus, Dayton • OKLAHOMA, Tulsa • OREGON, Portland • PENNSYLVANIA, Harrisburg, Philadelphia (Blue Bell), Pittsburgh • RHODE ISLAND, Providence • SOUTH CAROLINA, Columbia • TENNESSEE, Knoxville and Nashville • TEXAS, Austin, Dallas, El Paso, Houston • UTAH, Salt Lake City • VIRGINIA, Richmond • WASHINGTON, Seattle • WEST VIRGINIA, Charleston • WISCONSIN, Milwaukee • INTERNATIONAL—ARGENTINA, Buenos Aires • AUSTRALIA, Adelaide, Brisbane, Canberra, Melbourne, Perth, Sydney • AUSTRIA, Vienna • BELGIUM, Brussels • BOLIVIA, La Paz • BRAZIL, Rio-de Janeiro and Sao Paulo • CANADA, Calgary, Edmonton, Halifax, London, Montreal, Ottawa, Toronto, Vancouver, Winnipeg • CHILE, Santiago • DENMARK, Copenhagen • EGYPT (A.R.E.), Cairo • FINLAND, Espoo • FRANCE, Lyon, Paris, Puteaux • HONG KONG • INDIA, Bombay • INDONESIA, Djakarta • IRAN, Tehran • IRELAND, Dublin • ISRAEL, Tel Aviv • ITALY, Milan, Rome, Turin • JAPAN, Osaka and Tokyo • MALAYSIA, Kuala Lumpur • MEXICO, Mexico City • NETHERLANDS, Amstelveen, Rijswijk, Utrecht • NEW ZEALAND, Auckland and Christchurch • NORTHERN IRELAND, Belfast • NORWAY, Oslo • PUERTO RICO, San Juan • SINGAPORE • SOUTH KOREA, Seoul • SPAIN, Madrid • SWEDEN, Gothenburg and Stockholm • SWITZERLAND, Geneva and Zurich • TAIWAN, Taipei • UNITED KINGDOM, Birmingham, Bristol, Ealing, Epsom, Edinburgh, Leeds, Leicester, London, Manchester, Reading • VENEZUELA, Caracas • WEST GERMANY, Berlin, Cologne, Frankfurt, Hamburg, Hannover, Munich, Nurnberg, Stuttgart • YUGOSLAVIA, Belgrade and Ljubljana •

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